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TECHNICAL MANUAL FOR

AM-210

FLOPPY DISK CONTROLLER CIRCUIT BOARD

DWM-00210-00

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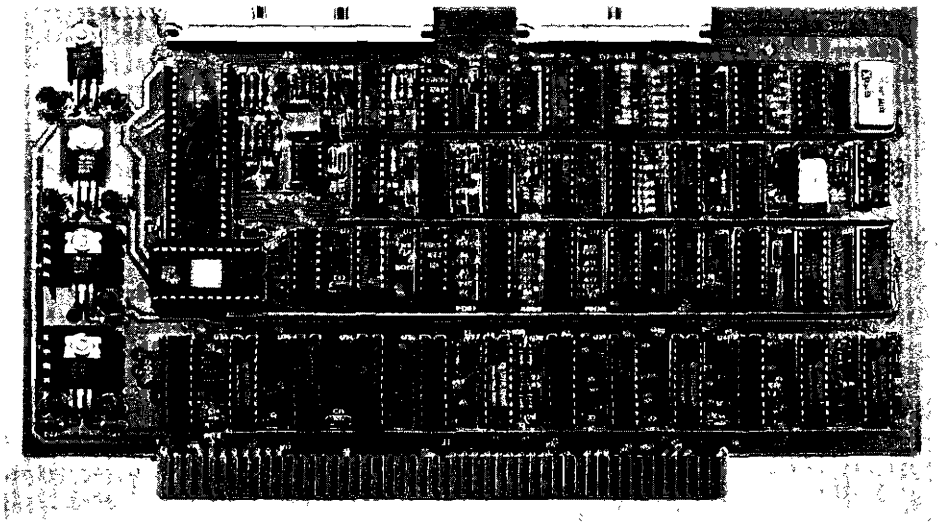

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SECTION 1

GENERAL DESCRIPTION

1.0 INTRODUCTION

This manual provides operating and maintenance instructions for the AM-210 Floppy Disk Controller circuit board manufactured by Alpha Microsystems located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION

The AM-210 circuit board provides interface capability between the S-100 Bus system and several of the popular eight inch and five inch floppy disk drives. A floppy controller microprocessor and a 1024 x 8 bit Random Access Memory (RAM) provide block transfers of data between the system and up to eight floppy drives. A Read Only Mem (ROM) is contained on the board to provide an optional boot load progra

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section 4 of this manual.

1.2 APPLICATION

The AM-210 is fully compatible with the standard S-100 Bus system and the Alpha Micro 8 and 16-bit bus systems. Jumpers on the circuit board that provide for user selected features are described in Section 2. The AM-210 controls both the standard 8" floppy and the 5" mini-floppy drives. Both single and double density formats are accommodated with both single and double sided disk. Specific configurations of the AM-210 are as follows:

AM-210-01	PerSci 277 Drive
AM-210-02	Wangco/Shugart Drives
AM-210-03	Mini-floppy Drives
AM-210-04	PerSci 299 Drive
AM-210-05	CDC 9406-3 Drives

SECTION 2
OPERATING DATA

2.0 INTRODUCTION.

This section contains information on the use of the AM-210 Floppy Disk Controller circuit board. Capabilities, specifications, interface wiring and user options are described for the successful integration of the board into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board operates from the standard S-100 Bus structure and the Alpha Micro 16-bit Bus to provide interface capability to several of the popular floppy disk drives. The AM-210 operates as a programmed I/O device to transfer data between floppy disk drives and system memory under CPU control. Specifications for the AM-210 circuit board are contained in Table 2-1.

2.2 INTERFACE DESCRIPTION AND WIRING.

The AM-210 Floppy Disk Controller provides interface capability between the standard S-100 Bus and floppy disk drives.

2.2.1 S-100 BUS INTERFACE.

The AM-210 circuit board is fully S-100 Bus compatible. The board and its associated floppy disk drives are addressed through the standard address lines and data is transferred through the standard data in and data out lines. The S-100 Bus connections are made via the bottom edge connector and are listed in Table 2-2. For a complete description of these signals and their operation in the AM-210, see Section 4.1 of this manual.

Table 2-1. AM-210 Specifications

PARAMETER	SPECIFICATIONS
System Interface	Standard S-100 Bus or Alpha Micro Bus for CPU and system memory.
Disk Interface	Compatible with most 8" floppy disk drives. Separate connector interfaces with 5" minifloppy drives.
Number of Drives	Up to eight drives can be controlled by one AM-210 circuit board.*
I/O Ports	Eight I/O ports utilized for data and control.
Disk Formats	Accommodates single and double density formats: IBM 3740 Single Density (FM) IBM 34 Double Density (MFM)
Disk Types	Compatible with single or double sided disks.
Step Rate	Variable step rate including software programmable.
Bootstrap Program	8 x 1024 bit PROM containing bootstrap program. Jumper block provides for boot-no boot option.
Interrupts	Multiple level interrupt capability, user selected.

*Eight drives with binary drive selection, four with radial drive selection. Refer to drive manual for information.

Table 2-1 (Cont.). AM-210 Secifications

PARAMETER	SPECIFICATIONS
Read Capability	Partial or full sector read capability.
Data Buffer	Contains 1024 x 8 RAM memory for data transfer operations.
Data Separator	PLO data separator-software programmable for both single and double density formats in both standard and mini-floppy configurations.
Write Precompensation	Contains write precompensation circuitry that is jumper selectable for delays from 50 to greater than 500 nanoseconds.
Memory Control	Software control of PROM and system memory contained in the same address space.

Table 2-2. S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A3	Address 3	31
A4	Address 4	30
A5	Address 5	29
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A9	Address 9	34
A10	Address 10	37

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN
A11	Address 11	87
A12	Address 12	33
A13	Address 13	85
A14	Address 14	86
A15	Address 15	32
DATAIN 0	Input Data Bit 0	95
DATAIN 1	Input Data Bit 1	94
DATAIN 2	Input Data Bit 2	41
DATAIN 3	Input Data Bit 3	42
DATAIN 4	Input Data Bit 4	91
DATAIN 5	Input Data Bit 5	92
DATAIN 6	Input Data Bit 6	93
DATAIN 7	Input Data Bit 7	43
DATAOUT 0	Output Data Bit 0	36
DATAOUT 1	Output Data Bit 1	35
DATAOUT 2	Output Data Bit 2	88
DATAOUT 3	Output Data Bit 3	89
DATAOUT 4	Output Data Bit 4	38
DATAOUT 5	Output Data Bit 5	39
DATAOUT 6	Output Data Bit 6	40
DATAOUT 7	Output Data Bit 7	90
PDBIN	Data Bus In	78
PHANTOM	Phantom	67
PRDY	Ready	72
$\overline{\text{PWR}}$	Write Strobe	77

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN
$\overline{\text{PRESET}}$	Reset	75
SINP	I/O Input Cycle	46
SOUT	I/O Output Cycle	45
$\overline{\text{VI0}}$	Interrupt 0	4
$\overline{\text{VI1}}$	Interrupt 1	5
$\overline{\text{VI2}}$	Interrupt 2	6
$\overline{\text{VI3}}$	Interrupt 3	7
$\overline{\text{VI4}}$	Interrupt 4	8
$\overline{\text{VI5}}$	Interrupt 5	9
$\overline{\text{VI6}}$	Interrupt 6	10
$\overline{\text{VI7}}$	Interrupt 7	11
Ø2	Phase 2 clock	24
+8VDC	+8VDC	1,51
+16VDC	+16VDC	2
-16VDC	-16VDC	52
GND	Ground	50, 100

2.2.2 FLOPPY DRIVE INTERFACE.

The AM-210 accommodates a maximum of up to four floppy disk drives. The interface lines are TTL level and require the industry standard floppy termination requirements. Additional drives in a daisy-chain hookup require that the termination resistors be removed except for the last drive in the chain. Overall cable length must not exceed 20 feet. Standard 8" floppy drives interface through J2, and 5" mini-drives interface through J3. Floppy drive interface signals are listed in Table 2-3. For a complete description of these signals and their operation in the AM-210, see Section 4.1 of this manual.

Table 2-3. AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN J2	PIN J3
$\overline{DS0}$	Drive Select 0	26	10
	Rtn	25	9
$\overline{DS1}$	Drive Select 1	28	12
	Rtn	27	11
$\overline{DS2}$	Drive Select 2	30	14
	Rtn	29	13
$\overline{DS3}$	Drive Select 3	32	6
	Rtn	31	5
$\overline{HEADLOAD}$	Head Load	18	-
	Rtn	17	-

Table 2-3 (Cont.). AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	
		J2	J3
$\overline{\text{INDEX}}$	Disk Index For Drive Selected	20	8
	Rtn	19	7
$\overline{\text{INWARDS}}$	Direction Select	34	18
	Rtn	33	17
$\overline{\text{MOTORON}}$	Motor On	-	16
	Rtn	-	15
$\overline{\text{RDATA}}$	Disk Output Data	46	30
	Rtn	45	29
$\overline{\text{READY}}$	Ready For Drive Selected	22	-
	Rtn	21	-
$\overline{\text{SEEK COMPLETE}}$	Seek Operation Complete	12	-
	Rtn	11	-
$\overline{\text{SEPCLOCK}}$	Separated Clock	50	-
	Rtn	49	-
$\overline{\text{SEPDATA}}$	Separated Data	48	-
	Rtn	47	-
$\overline{\text{SIDESEL}}$	Side Select	14	32
	Rtn	13	31

Table 2-3 (Cont.). AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	
		J2	J3
$\overline{\text{STEP}}$	Step Pulses	36	20
	Rtn	35	19
$\overline{\text{TG43}}$	Track Greater Than 43	2	-
	Rtn	1	-
$\overline{\text{TRACK 0}}$	Track 0	42	26
	Rtn	41	25
$\overline{\text{TWOSIDED}}$	Two Sided Disk	10	-
	Rtn	9	-
$\overline{\text{WDATA}}$	Write Data	38	22
	Rtn	37	21
$\overline{\text{WG}}$	Write Gate	40	24
	Rtn	39	23
$\overline{\text{WP}}$	Write Protect	44	28
	Rtn	43	27

.3 USER OPTIONS.

Several features on the AM-210 circuit board can be jumper selected at the user's option. Some optional features are etched for the selection most commonly used and the etch can be easily cut and jumpers added to change the selection.

2.3.1 BOOTSTRAP HEADER OPTION.

The bootstrap PROM address is placed in circuit etch for :FC00. This can be easily altered by cutting the appropriate address line and jumpering it to the +5 volt or ground pad provided.

In addition, a jumper block is provided for quick switching between a boot from the AM-210 setup to an NB (no-boot) process. Re-orient the jumper block for the desired operation.

2.3.2 I/O PORT ADDRESS.

The I/O address is placed in circuit etch for :F0. This can be easily altered by cutting the appropriate address header line and jumpering it to either the +5 volt or ground pad provided.

2.3.3 MASTER CLOCK FREQUENCY OPTION.

To allow for the controller chip U1 to function in either a standard or mini-floppy configuration, the master clock frequency is jumper selectable. Those presently available are 8 Mhz, 4 Mhz, 2 Mhz, and 1 Mhz. Typical 8" drives require 2 Mhz which is provided in etch for the standard version. Five inch drives require 1 Mhz which can be selected by cutting the etch at the 2M pad near U9 and jumpering the 1M pad to "CLK" as provided.

2.3.4 VECTORED INTERRUPT OPTION.

The 8 vectored interrupt lines presently allocated by the AM-100 are available for jumper selection on the AM-210.

Jumper the appropriate VI0 through VI7 line to the pad labeled INTR as provided near J1 component side.

2.3.5 SEEK COMPLETE INTERFACE LINE OPTION.

For those drives generating a seek complete signal for normal operation, jumper the SC pad near U41 to the SC pad at the top of U1 near the connector J2.

2.3.6 SOFTWARE CONTROL STEP RATE OPTION.

For those drives requiring a step rate that is not programmable via controller module U1, a data line is provided to software step the drives from the CPU. This is selected by cutting the etch above SS near U15 and jumpering U14-13 (pad closest to U14) to the pad labeled SS.

2.3.7 DATA SEPARATOR TIMING OPTION.

To accommodate both 5" and 8" floppies in both a single and double density format, two options are provided:

1. Phase-lock oscillator (PLO) frequency control option. To provide for chip-to-chip variations in the 74LS324, trim-pot R39 can be added in place of R10, R11. This is typically factory chosen and set and should not be changed unless U2 is replaced.

   CAUTION

   Trim-Pot R38 is a factory adjustment and must not be changed.

2. To facilitate the change from standard to mini-floppy interface, a jumper option is provided near U23. For standard operation, pads MS and MB are jumpered together in etched circuitry. For mini-floppies, cut the etch from MS to MB and jumper MN to MB. The PLO circuitry should not need any re-adjustment after this change.

2.3.8 WRITE PRE-COMPENSATION OPTIONS.

For double density formats, data transfer rate is realized as maximum error free when pre-compensation is provided with particular data patterns. The selection of the On Time, Late, or Early write data bit is selected by the controller module U1. However, the amount of compensation is drive dependent. This can be selected by jumpering appropriate pads for the selected delay time.

The actual delays are varied by jumpering one of the outputs of U6 (labeled 50-250) to either the E, L, or T pads at U17. The standard set-up allows for 150 nSec jumpered to T (etched circuitry); 250 nSec jumpered to L; and E jumpered to B for no delay. Note that the -05 version board utilizes a delay module in which these times are doubled. The the over-all delay becomes 100-500. The standard setup then allows for 300 nSec jumpered to T and 500 nSec jumpered to L.

SECTION 3
PROGRAMMING

3.0 INTRODUCTION.

This section describes the programming requirements for the AM-210 circuit board. Circuit board addressing, diskette formatting, interrupts and bootstrap loader are described for complete system compatibility.

3.1 ADDRESSING.

The AM-210 and its associated disk drives are addressed through the S-100 Bus address lines. The circuit board address is jumper selectable but is etched for address F0. See Section 2 of this manual for address option instructions.

Eight I/O ports are required by the AM-210 controller as described in Table 3-1. Note that the first four I/O addresses are contained in the floppy controller IC, U1. See paragraph 4.2.1 for more detailed information on the floppy controller module.

3.2 EXTERNAL CONTROL REGISTERS.

In addition to the registers contained in the floppy control module, there are other registers which must be programmed for proper operation. These are as follows:

1. External Control Register No. 1. See Tables 3-2 and 3-3 for a description of control bits.

2. External Control Register No. 2. See Table 3-4 for a description of control bits.

3. Random Access Memory (RAM) port. See paragraph 3.3 for a description of RAM requirements.

Table 3-1. I/O Port Definitions

I/O PORT ADDRESS*	INPUT	OUTPUT	COMMENT
X0	Status Register	Command Register	See FD1791 spec attached.
X1	Track Register	Track Register	See FD1791 spec attached.
X2	Sector Register	Sector Register	See FD1791 spec attached.
X3	Data Register	Data Register	See FD1791 spec attached.
X4	RAM Port	RAM Port	I/O port access for 1024 byte on-board RAM.
X5		Reset RAM address Register	
X6	External Status Register	External Control Register #1	See Table II
X7		External Control Register #2	See Table III

*I/O Port Address is jumper programmable to any even block of eight I/O addresses.

Table 3-2. External Control Register No. 1 Output Functions (X6)

BIT	FUNCTION	COMMENTS
0 1 2 3	Select Drive 0 Select Drive 1 Select Drive 2 Select Drive 3	Selects drive for read/write operations.
4	Select Side 1	Side 0 is standard.
5	Motor ON	Controls mini-floppy motor drive.
6	Step Command	Can be used to control floppy disk track stepping rate instead of using the STEP signal from FD1791.
7	Double Density Mode	Selects Double Density mode of operation.

020 SDX

Table 3-3. External Control Register No. 1 Input Functions (X6)

BIT	FUNCTION	COMMENTS
0	Data Request	Used during formatting of diskettes to signal processor that controller requires data. This bit must be serviced within 48 usec. This same bit appears as Bit 1 in the FD1791 status register.
1	Interrupt Bit	This bit is a copy of the interrupt signal from the FD1791. It can be used by processors which are not interrupt driven to sense when a command has been completed.
2	$\overline{\text{Two-sided Drive}}$	When high, indicates single drive.
3	$\overline{\text{Seek Complete}}$	Indicates drive has not completed seek command (option only).

Note: This register may be READ without affecting any command which may be in progress (excluding WRITE TRACK). During a READ or WRITE sector command, this register must be examined to check for command completion (Bit 1) if the CPU is not interrupt driven.

Table 3-4. External Control Register No. 2 Functions (X7)

OUTPUT FUNCTION		COMMENTS
BIT	FUNCTION	
0	Phantom	When set, this bit disables the on-board Bootstrap PROM and enables any system memories controlled by the Phantom line.
1	Interrupt Enable	
2	Write to Floppy	Indicates to the internal I/O logic whether to read from or write to the floppy drive.
3	Format	When set, block I/O data transfers are expected to the Data Register in the FD1791. The controller, by holding PRDY, will control the data rate from the processor.

3.3 RANDOM ACCESS MEMORY.

A 1024 byte RAM is contained in the AM-210 and used as a sector buffer between the floppy drive and system memory. In order to read the contents of the RAM buffer, the following sequence of operations must take place:

1. The RAM address register must be reset to zero. (Issue an output command to I/O port X5.)

2. Read I/O port X4 to get the first byte of data.

3. Subsequent reads to I/O port X4 will automatically increment the RAM address register and provide the next byte of data.

4. When reading is complete, reset the RAM address register to zero as in Step 1.

In order to write into the on-board RAM buffer, the following sequence of operations must take place:

1. The RAM address must be reset to zero. (Issue an output command to I/O port X5.)

2. Write to I/O port X4 to write the first byte of data.

3. Subsequent writes to I/O port X4 will result in data being written into consecutive RAM buffer addresses.

4. When writing is complete, reset the RAM address register to zero as in Step 1.

3.4 DISKETTE FORMATTING.

Since the on-board RAM buffer is only 1024 bytes deep, formatting a track must be done by a block I/O command from the processor. Data is required by the controller at approximately 16 usec/byte rate in double density. This can be accomplished by setting the FORMAT bit (see Table 3-4) in External Control Register No. 2. When this bit is set, and a WRITE TRACK command is issued to the controller, the PRDY Line is forced low which inhibits any more processor activity. This line is reset by BDRQ which indicates that U1 has initialized and is ready for data transfer. Once the DRQ line is set by U1, it allows for 3 byte times (= 48 microsec.) for the first byte of the block move command to be assembled in the data register of U1. (This signal indicates the request for more data.) When this condition exists, the WRITE DATA TRACK must be BLOCK MOVED to I/O port X3 (module Data Register). As long as the processor transfer byte rate is 16 usec/byte or greater, the controller will govern the exact timing required. When the floppy drive has received all the required data, it sets the interrupt bit and writing ceases. Even if more than the required data is transferred to the Data Register, it only sends to the floppy drive what is required. When the External Status Register is checked for Bit No. 1 true, the transfer is complete. The Interrupt Bit is then reset when the module Status Register is next read for the status of the Write Track sequence.

3.5 INTERRUPTS

Interrupt operation is supported by the Dual Density Floppy controller. Interrupt operation is enabled by Bit 1 of external Control Register No. 2. If enabled, an interrupt is generated at the completion or termination of any operation performed by the module and is reset when a new command is loaded into the command register, or the status register is read.

3.6 BOOTSTRAP PROM

A 512 byte PROM is contained on the Dual Density Floppy Controller, and is controlled by Bit 0 of External Register No. 2. When set, this bit disables the PROM and enables system memory contained in the same address space. At power-up time, this bit is reset to enable the bootstrap PROM. The base address of the PROM is programmable via board etched jumper circuitry.

SECTION 4
FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION.

The AM-210 Floppy Disk Controller circuit board contains integrated circuit elements for the necessary data processing for the performance of the functions as described in Sections 1, 2, and 3 of this manual. This section describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

This circuit board provides control and interface capability between the S-100 Bus and most popular floppy disk drives. The functional block diagram of the circuit board is shown in Figure 4-1, and the circuit board schematic is contained in Section 6 of this manual. Table 4-1 contains a list of the signals used in this circuit board with descriptions of their functions. For S-100 Bus interface signals see Table 4-2. For floppy disk interface signals, see Table 4-3.

Table 4-1. AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
B02	Board Clock	3	AM-210 board clock driven from Bus Ø2 clock.
$\overline{\text{BDACT}}$	Board Active	3	Enables the command register U29 with $\overline{\text{BDSEL}}$ and address line A2.
BDRQ	Data Request	6	Floppy controller module output indicating that the module data register contains assembled data in read operations or is empty in write operations.
$\overline{\text{BDSEL}}$	Board Select	3	Output of the I/O address comparator U25 asserted when address lines A3-A7 compare with the address code on the address block.
BINTR	Board Interrupt Request	6	Floppy controller module output set at the completion of any operation and reset when a new command is loaded into the module command register or the module status register is read.
$\overline{\text{CE}}$	Chip Enable	3	Formatter/controller module input for chip select to enable the module.
CLK	Clock	5	1 Mhz or 2 Mhz system clock (depending on jumper to U9).
$\overline{\text{CRAMCS}}$	RAM chip select	3	Provides enable for the RAM modules U30 and U31 (chip select).
DAL0-7	Data and Address Lines	3	Tri-state bus data lines to provide data paths within the circuit board.
$\overline{\text{DBIN}}$	Data Bus In	3	Read Enable driven by PDBIN from S-100 Bus. Used by bus master to request addressed slave to place data on input port.

Table 4-1 (Cont.). AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{DD}$	Double Density	6	Formatter/Controller module input to select either single or double density operation. $\overline{DD}$ = 0 for double density, $\overline{DD}$ = 1 for single density.
DIR	Direction	6	Formatter/Controller module output for direction motor control. Active high when stepping in, active low when stepping out.
$\overline{DRQEN}$	Data Request Enable	4	Enables outputs of the data register (U43) in the DRQ Processor Logic which selects PROM, U19.
EARLY	Early Precompensation	6	Formatter/Controller module output to indicate that the write data pulse occurring while EARLY is active (high) should be shifted early for write precompensation.
$\overline{FORMAT}$	Format	6	Output of external control register 2 from DATAOUT bit 3. When asserted, block I/O data transfers are expected.
HLD	Head Load	6	Output to cause the disk to be placed in close proximity to the Read/Write head.
HLT	Head Load Timing	6	Formatter/Controller module input indicating that the read/write head is engaged.
$\overline{INIT}$ INIT	Initialize	3	Board reset signal driven from S-100 Bus $\overline{PRESET}$ signal.
INTEN	Interrupt Enable	6	Output of External control register 2 from BDOUT bit 1 to enable AND gate so that BINTR from floppy controller module will generate INTR.

Table 4-1 (Cont.). AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
INTR	Interrupt	6	Output of interrupt gate (BINTR and INTEN) jumper selectable to vectored interrupts VI0-VI7.
LATE	Late Precompensation	6	Formatter/Controller module output to indicate that the write data pulse occurring while LATE is active (high) should be shifted late for write precompensation.
$\overline{\text{LDCR1}}$	Load Control Register 1	3	Command generator output to load External Control Register 1 (U34) from CPU output data (BDOUT0-7).
$\overline{\text{LDCR2}}$	Load Control Register 2	3	Command generator output to load External Control Register 2 (U35) from CPU output data (BDOUT0-7).
$\overline{\text{LDRAM}}$	Load RAM	3	Write enable to RAM (U30, U31) generated from LDRAM1 from the command generator or from RAMWR from the DRQ processor.
$\overline{\text{LDRAM1}}$	Load RAM 1	3	Command Generator output to generate $\overline{\text{LDRAM}}$ to write data into the AM-210 Random Access Memory.
$\overline{\text{LOBDSEL}}$	Low Board Select	3	Selects the registers internal to the Formatter/Controller module.
$\overline{\text{MOTORON}}$	Motor On	6	Output to mini-floppy drives to turn on drive motor.
$\overline{\text{PHANTOM1}}$	Phantom	6	External control register output from DATAOUT 0 to disable the on board boot PROM and enable system memories controlled by the PHANTOM line.
$\overline{\text{PROMEN}}$	PROM Enable	3	Output of the Boot Comparator to enable the Boot PROM and enable the data in port U40.

Table 4-1 (Cont.). AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{PSTR}}$	PRDY Stretch	4	Enables $\overline{\text{WDWE}}$ (module write enable) from PWR (bus write strobe) generated by PRDY control logic.
$\overline{\text{RAMCS}}$	RAM Control Signal	4	Enable signal for the RAM address counter.
$\overline{\text{RAMWR}}$	RAM Write	4	Output of DRQ processor to generate $\overline{\text{LDRAM}}$ to enable the write inputs of the RAM.
RCLK	Read Clock	6 (7)	Formatter/Controller module clock input from the data separation circuit phased to the $\overline{\text{RDATA}}$ input.
$\overline{\text{RDATA}}$	Read Data	6	Formatter/Controller module data input directly from the disk drive. Negative pulse for each recorded flux transition.
RDCR	Read Status Register	3	Output of the command generator to enable the external status register to transfer data to DATIN 0-3.
$\overline{\text{RDRAM1}}$	Read RAM	3	Reads AM-210 Random Access Memory.
RG	Read Gate	6	Not used.
$\overline{\text{RSTAR}}$	Reset RAM Address Register	3	Resets binary counters used for RAM address register.
$\overline{\text{SEEKCOMP}}$	Seek Complete	6	Jumper selectable to disk drives that have seek complete feature.
SEL0-3		6	Output of external control register to generate outputs to floppy drives $\overline{\text{DS0}}$ - $\overline{\text{DS3}}$ from DATAOUT0-3.

Table 4-1 (Cont.). AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
SIDE 1		6	Output of external control register to generate outputs to floppy drives $\overline{\text{SIDESEL}}$ from DATAOUT4.
$\overline{\text{SINP}}$	I/O Input Cycle		Indicator driven from S-100 Bus signal SINP indicating I/O input operation.
$\overline{\text{SOUT}}$	I/O Output Cycle	3	Indicator driven from S-100 Bus signal SOUT indicating I/O output operation.
STEP	Step	6	Formatter/Controller module output for step motor control that contains a pulse for each step.
TG43	Track Greater Than 43	6	Formatter/Controller module output to inform the drive that the Read-Write head is positioned between 44-76. Output valid only during read and write commands.
WD	Write Data	6	Write Data output of the Formatter/Controller module. Contains address marks as well as data.
WDA0	Module Address 0	3	Formatter/Controller module address line zero for accessing the active registers with active $\overline{\text{CE}}$, $\overline{\text{WDRE}}$, and $\overline{\text{WDWE}}$.
WDA1	Module Address 1	3	Formatter/Controller module address line one for accessing the active registers with active $\overline{\text{CE}}$, $\overline{\text{WDRE}}$, and $\overline{\text{WDWE}}$.
$\overline{\text{WDRE}}$	Module Read Enable	3	Formatter/Controller module input to initiate the read mode.
$\overline{\text{WDRE1}}$	Module Read 1	3	Generated from bus signal PDBIN to generate module read enable $\overline{\text{WDRE}}$ and enable the data-in port.

Table 4-1 (Cont.). AM-210 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{WDRE2}}$	Module Read 2	4	Generated from DRQ processor to generate module read enable $\overline{\text{WDRE}}$.
$\overline{\text{WDWE}}$	Module Write Enable	4	Formatter/Controller module input to set the write mode with active chip select ($\overline{\text{CE}}$) signals.
WG	Write Gate	6	Write gate output of Formatter/Controller module to floppy disk drive.
WR	Write Strobe	3	AM-210 signal driven by S-100 Bus signal $\overline{\text{PWR}}$ generated by bus masters as write command to slaves.
WRTFLOPPY	Write Floppy	6	External control register output from DATAOUT2 indicating whether to read from or write to the floppy drive.

Table 4-2. S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
A0	Address 0	79	16 Bits of S-100
A1	Address 1	80	Addressing.
A2	Address 2	81	
A3	Address 3	31	
A4	Address 4	30	
A5	Address 5	29	
A6	Address 6	82	
A7	Address 7	83	
A8	Address 8	84	
A9	Address 9	34	
A10	Address 10	37	
A11	Address 11	87	
A12	Address 12	33	
A13	Address 13	85	
A14	Address 14	86	
A15	Address 15	32	
DATAIN 0	Input Data Bit 0	95	Data Input Port.
DATAIN 1	Input Data Bit 1	94	Bus Master Input from
DATAIN 2	Input Data Bit 2	41	Slaves.
DATAIN 3	Input Data Bit 3	42	
DATAIN 4	Input Data Bit 4	91	
DATAIN 5	Input Data Bit 5	92	
DATAIN 6	Input Data Bit 6	93	
DATAIN 7	Input Data Bit 7	43	
DATAOUT 0	Output Data Bit 0	36	Data Output Port.
DATAOUT 1	Output Data Bit 1	35	Bus Master Output to
DATAOUT 2	Output Data Bit 2	88	Slaves.
DATAOUT 3	Output Data Bit 3	89	
DATAOUT 4	Output Data Bit 4	38	
DATAOUT 5	Output Data Bit 5	39	
DATAOUT 6	Output Data Bit 6	40	
DATAOUT 7	Output Data Bit 7	90	

Table 4-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
PDBIN	Data Bus In	78	Read enable. Used by bus master to request addressed slave to place data on input port.
$\overline{\text{PHANTOM}}$	Phantom	67	Disables phantom controlled memories when asserted.
PRDY	Ready	72	AM-210 I/O signal to allow extensions of bus timing.
$\overline{\text{PWR}}$	Write Strobe	77	Write strobe generated by bus masters as write command to slaves.
$\overline{\text{PRESET}}$	Reset	75	AM-210 reset input from bus.
SINP	I/O Input Cycle	46	AM-210 I/O signal indicating I/O input operation.
SMEMR	Memory Cycle Input Status Line	47	Current bus cycle is a bus master input from a memory address.
SOUT	I/O Output Cycle	45	AM-210 I/O signal indicating I/O output operation.
$\overline{\text{VI0}}$ $\overline{\text{VI1}}$ $\overline{\text{VI2}}$ $\overline{\text{VI3}}$ $\overline{\text{VI4}}$ $\overline{\text{VI5}}$ $\overline{\text{VI6}}$ $\overline{\text{VI7}}$	Interrupt 0 Interrupt 1 Interrupt 2 Interrupt 3 Interrupt 4 Interrupt 5 Interrupt 6 Interrupt 7	4 5 6 7 8 9 10 11	Jumper selected interrupts. Used for both interrupt requests and DMA requests. Normal configuration: VI6 used for DMA request.

Table 4-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
Ø2	Phase 2 clock	24	Phase 2 clock from CPU.
+8VDC	+8VDC	1, 51	+8V power.
+16VDC	+16VDC	2	+16V power.
-16VDC	-16VDC	52	-16V power.
GND	Ground	50, 100	System Ground

Table 4-3. AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN J2	PIN J3	DESCRIPTION
$\overline{DS0}$	Drive Select 0	26	10	AM-210 output selects disk drive No. 0.
	Rtn	25	9	
$\overline{DS1}$	Drive Select 1	28	12	AM-210 output selects disk drive No. 1.
	Rtn	27	11	
$\overline{DS2}$	Drive Select 2	30	14	AM-210 output selects disk drive No. 2.
	Rtn	29	13	
$\overline{DS3}$	Drive Select 3	32	6	AM-210 output selects disk drive No. 3.
	Rtn	31	5	
$\overline{HEADLOAD}$	Head Load	18	-	AM-210 output. A low active signal causes the read/write head to load against the disk provided $\overline{READY}$ is active.
	Rtn	17	-	
$\overline{INDEX}$	Disk Index 0	20	8	AM-210 input. One ms negative going pulse occurs for each revolution of the selected disk.
	Rtn	19	7	
$\overline{INWARDS}$	Direction Select	34	18	AM-210 output. Defines direction of motion of the head positioner when the step line is pulsed. Low = inward (higher track number). High = outward (lower track number - away from center).
	Rtn	33	17	

Table 4-3 (Cont.). AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN J2	PIN J3	DESCRIPTION
$\overline{\text{MOTORON}}$	Motor On	-	16	
	Rtn	-	15	
$\overline{\text{RDATA}}$	Disk Output Data	46	30	AM-210 input. Clock and data output of selected head. Each flux transition produces negative pulse.
	Rtn	45	29	
$\overline{\text{READY}}$	Ready 0	22	-	AM-210 input. A low level indicates that a diskette is loaded in selected drive and is within 90% of its operating speed.
	Rtn	21	-	
$\overline{\text{SEEK COMPLETE}}$	Seek Operation Complete	12	-	AM-210 input. Low level indicates that a seek or restore operation has been completed (jumper connection in AM-210).
	Rtn	11	-	
$\overline{\text{SEPCLOCK}}$	Separated Clock	50	-	AM-210 input. Separated clock data from read data (jumper connection in AM-210).
	Rtn	49	-	
$\overline{\text{SEPDATA}}$	Separated Data	48	-	AM-210 input. Separated data from read data (jumper connection in AM-210).
	Rtn	47	-	

Table 4-3 (Cont.). AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN J2	PIN J3	DESCRIPTION
$\overline{\text{SIDESEL}}$	Side Select	14	32	AM-210 output. A low signal selects side 1 surface for reading and writing and a high signal selects side 0.
	Rtn	13	31	
$\overline{\text{STEP}}$	Step Pulses	36	20	AM-210 output. Low level of one pulse for each track crossed by the head for a seek to a new address.
	Rtn	35	19	
$\overline{\text{TG43}}$	Track Greater Than 43	2	-	AM-210 output. Active low reduces writing current when on tracks 44-76.
	Rtn	1	-	
$\overline{\text{TRACK 0}}$	Track 0	42	26	AM-210 input. Low level indicates heads are positioned over track 0.
	Rtn	41	25	
$\overline{\text{TWOSIDED}}$	Two Sided Disk	10	-	AM-210 input indicates a two-sided diskette is rotating in the drive.
	Rtn	9	-	
$\overline{\text{WDATA}}$	Write Data	38	22	AM-210 output. Write data to disk. Write current changes polarity for each positive to negative transition on this line.
	Rtn	37	21	

Table 4-3 (Cont.). AM-210 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN		DESCRIPTION
		J2	J3	
$\overline{WG}$	Write Gate	40	24	AM-210 output. Low level turns on write current.
	Rtn	39	23	
$\overline{WP}$	Write Protect	44	28	AM-210 input. Low level indicates that the selected disk is write protected.
	Rtn	43	27	

4.1.1 DATA OUT PORT.

The data out port consists of tri-state buffers to interface the AM-210 circuit board with CPU output data. One set of buffers (U36) interfaces the DATAOUT0-7 system bus with the AM-210 internal tri-state bus to transfer data to the external control register on U34 and U35. The other set of buffers (U39) interfaces the DATAOUT0-7 system bus to the internal tri-state bus to transfer data to the internal Random Access Memory (RAM) and the floppy controller module U1. The buffers on U39 are gated with the board select signal (BDSEL) from the AM-210 I/O address comparator and I/O output cycle signal (SOUT) from the bus. Data is transferred from the CPU when this board is addressed for an I/O output cycle by the CPU.

4.1.2 DATA IN PORT.

The data in port consists of tri-state buffers to interface the AM-210 circuit board with CPU input data. One set of buffers interfaces the internal tri-state bus (DAL0-7) to transfer data from the internal RAM or the floppy controller module. These buffers are gated by logic in the command generator. The other part of the data in port is the external status register that transfers status information to the system data bus (DATAIN0-3) from the floppy controller module (interrupt or data request, BINTR or BRQ) and the disk drive. These buffers are gated by a read command ($\overline{\text{RDCR}}$) from the command generator.

4.1.3 BOOTSTRAP CIRCUITRY.

The AM-210 PROM (U21) contains a bootstrap load routine addressed from boot comparator U26. With the correct address on lines A10-A15 and memory cycle line SMEMR active, the boot PROM is enabled by $\overline{\text{PROMEN}}$ and the boot program is transferred through the data in port. This is an optional feature that can be disabled by jumpering the no-boot pads together as described in Section 2.

The Phantom can be disabled after the boot routine has occurred by programming external control register No. 2 bit 0. This enables any system memories presently controlled by the Phantom Line.

4.1.4 I/O ADDRESS CIRCUITRY.

The AM-210 I/O addressing takes place through I/O comparator U25 to generate $\overline{\text{BDSEL}}$ and through the command generator. The command generator decodes whether the floppy controller module is being selected by address line A2. This generates the controller module read and write lines, and address lines WDA0 and WDA1. Chip enable (CE) is derived from a non-format mode and any activity to/from the floppy controller module.

4.1.5 COMMAND GENERATOR.

This octal register decodes the activity of the board via address lines A0, A1, A2 and the bus master input SINP. When the CPU is outputting to the AM-210, SINP is high; and the selectable operations are:

1. Resetting the RAM address register ($\overline{\text{RSTAR}}$).
2. Loading the RAM (LDRAM1).
3. Loading the control register (LDCR1, LDCR2).

When SINP is active low, the available operations are:

1. Reading RAM (RDRAM1).
2. Reading the external status register (RDCR).

4.1.6 RAM AND CONTROL CIRCUITRY.

The 1024 byte RAM provides temporary storage of data to and from the floppy disk drives. The data transfers eight bits at a time into the RAM until a full sector is complete. The data is then transferred through the data-in port to the CPU.

Addressing of this data is accomplished by a series of 4-bit binary counters. To access RAM, the binary counters are first reset to zero via Port X5 (RSTAR). Then with each sequential READ or LOAD RAM command, the address lines are incremented by one up to 1023. After reading or writing is completed, the binary counters are reset to zero in preparation for the next activity.

4.1.7 EXTERNAL STATUS AND CONTROL REGISTERS.

External Control Register No. 1 is loaded via the LDCR1 command by the command generator. This register selects the drive unit number, side selection, and double density mode. In addition, signals are provided for MOTOR ON for mini-floppy interfaces, and a STEP bit for software control of Head Step Rates that cannot be provided by the floppy controller module.

External Control Register No. 2 provides the on-board logic circuitry with selection of the Format mode, Phantom memory disable, Interrupt Enable, and the Write to Floppy mode. This register is loaded from the LDCR2 command from the command generator (Port X7).

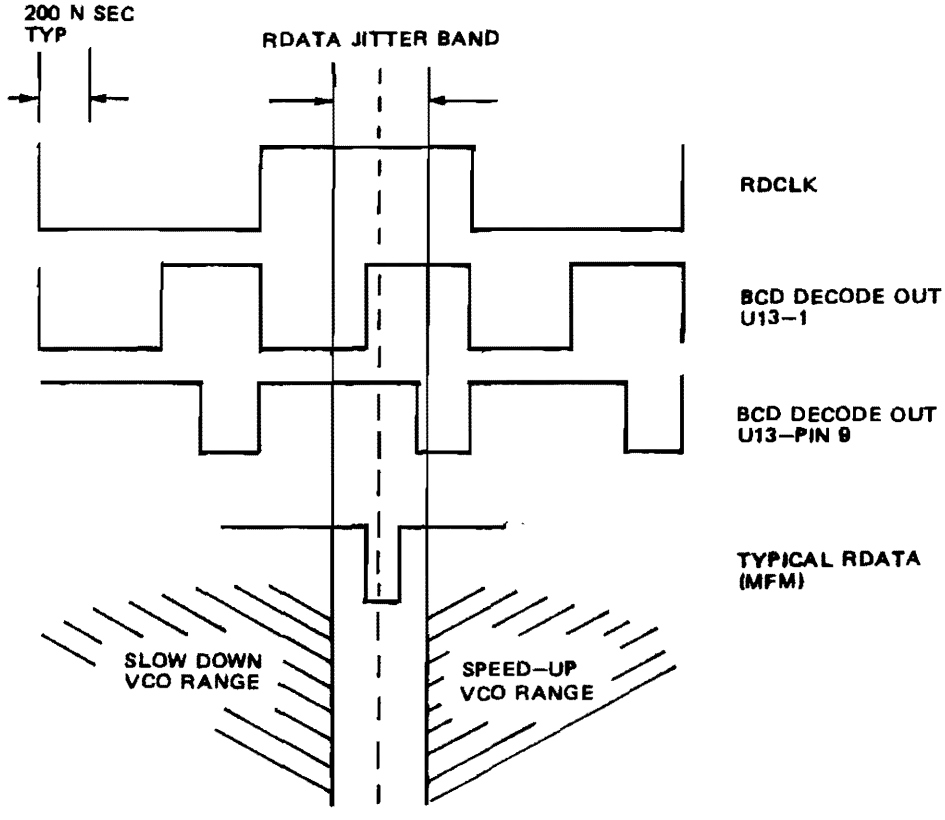
The External Status Register provides 4 bits of information back to the Processor. For optional drives it indicates whether a two-sided diskette is installed (TWOSIDED). It also indicates a Seek Complete (SEEK COMP) activity for the selected drive.* In addition, the Data Request (DRQ) and Interrupt (INTR) bits of the floppy controller module are included for software inspection.

4.1.8 DATA-CLOCK SEPARATOR.

The AM-210 utilizes a phase-lock oscillator circuit to provide the synchronization of raw data to the read clock signal for

*SEEK COMP is an optional signal available on only a few drives.

the floppy controller module. This logic uses a voltage controlled oscillator to provide the master clock for the data separator circuit. The clock is then divided down by either eight or four depending on whether the board is operating in single or double density mode. A BCD to decimal decoder is then used to synchronize the RAM data coming from the drive. It sets up a Speed-up and Slow-down range that the oscillator maintains in order to lock to the data signal. This allows for maximum data transfer with minimal lost data. This circuitry also includes a tuned low-pass filter as well as a linear operational amplifier for noise isolation. See Figure 4-2 for the data separator timing.



NOTE: TYPICAL JITTER OCCURS ON RDATA FROM MULTI–READS f DISK ROTATION.

JITTER USUALLY INCREASES AT THE HIGHER TRACKS (DENSITY INCREASES).

Figure 4-2. Data Separator Timing

4.1.9 WRITE PRE-COMPENSATION

Bit shift during read operations can be reduced by the use of write pre-compensation circuitry and a logical algorithm to analyze the data pattern for predictable bit shift patterns. Thus if a pattern causes late bit shift, the bits are written early; if the bit shift is early, the bits are written late. Then during the read process, the bits appear more nearly on time within the Phase Lock Oscillator window.

The algorithm which determines the bit patterns is internal to the floppy controller module. It provides two outputs based on this pattern labeled Early and Late. The Late and Early signals are then latched for each write data pattern by U16 (746574). The Write data output of the floppy module is delayed via a dual in-line delay circuit with up to 500 nSec of delay. U17 (a three of one decoder) is then used to determine which write bit is to be chosen: one which is early (no delay) or late (maximum delay) or on time (theoretically no delay, but typically 150 nSec).

4.1.10 PRDY CONTROL LOGIC

This circuitry provides for the timing variations among floppy drives and the actual processor set.

During formatting, the actual data transfer rate is governed by the need for the floppy controller module for more data. As the timing diagram in Figure 4-3 indicates, any board activity to the floppy controller module fires the one shot for approximately 1200 nSec. When in the format mode, the JK flipflop (U8) is prepared to be reset by the above described one shot and set by DRQ. Thus, when a WRITE TRACK command is sent to the floppy controller module, the PRDY line is pulled low until all of the data register is transferred to floppy as indicated by BDRQ. When BDRQ is fired, the JK flipflop (U8) is once again set and PRDY is released. Thus the timing is totally controlled by the data transfer of the floppy module. The PRDY stretch signal (PSTR) is used to ensure that the write command (WDWE) to the floppy controller module will only occur during bus-active time. See Figure 4-3 for PRDY control logic timing.

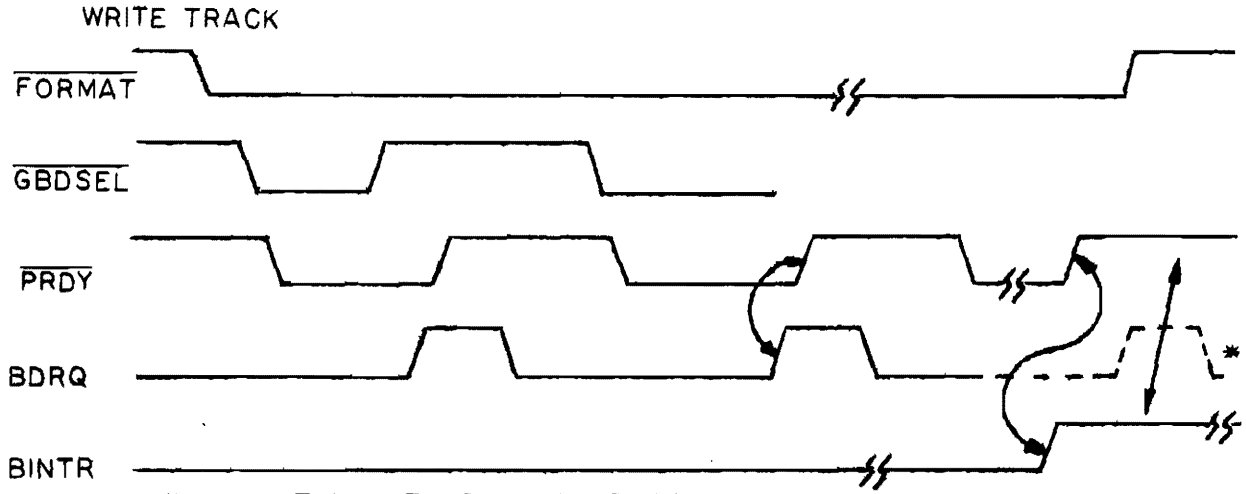


Figure 4-3. PRDY Control Logic Timing

During Data Transfer, PRDY is sent Active Low by the Write Track CMD to the module. Each subsequent BDRQ then signals the processor that the data transfer is complete. This sets PRDY back to the Inactive (high) state. Thus PRDY is essentially controlled by GBDSEL (floppy controller module active via DRQ Processor) and BDRQ (request for data).

When BINTR is sent Active High, PRDY is sent in the inactive state (high). Even if additional BDRQ are generated, the controller module h interrupted out and will not write additional data. BINTR remains Active (high) until the Status Register of the floppy controller modul is read. The format bit is then reset (high) and the process complete

4.1.11 DRQ PROCESSOR.

This logic is composed of an 8 x 32 ROM (U19) used to conveniently control the floppy controller module during normal read and write operations. The ROM is essentially halved for reading from, or writin to, the floppy controller module.

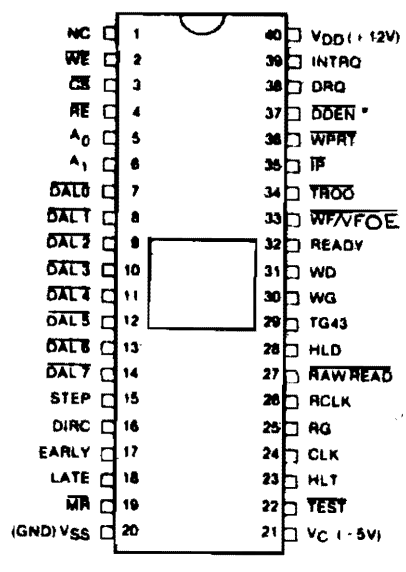
During the read operations, the ROM begins at the address of 00111 which is the REST state. Upon the occurrence of the first BDRQ, the data register of the controller module is read. The next address selection of the ROM allows for RAM write of the module data. After the last DRQ and the controller module has interrupted out (BINTR set), the octal flipflop (U43) is disabled and the DRQ processor is essentially stopped. The write mode is similar. The signals controlled are RAM chip select (RAMCS), RAM write (RAMWR), and module read enable (WDRE2), and write enable (WDWE).

4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit packages (DIPS) contained on the AM-210 circuit board. Most of the data processing is handled by the Floppy Disk Formatter/ Controller module so it is described in detail. The control logic and interface modules are also described with logic and connection diagrams for each one.

4.2.1 FLOPPY DISK FORMATTER/CONTROLLER DESCRIPTION (U1).

This device performs the function of interfacing a processor to a flexible (Floppy) diskette drive. It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data can be stored in a data entry format compatible with the IBM 3740 single density or IBM System 34 double density formats. In either format, all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header. Module pin connections are shown in Figure 4-4 and signals are described in Table 4-4.



* PIN 37 MUST BE LEFT OPEN

Figure 4-4. Floppy Disk Formatter/Controller Pin Connections

Table 4-4. Floppy Disk Formatter/Controller Signal List

PIN	SIGNAL	FUNCTION
1	VBB	-5V power input.
2	$\overline{WE}$ $\overline{WRITE\ ENABLE}$	Sets the DAL in the write mode with an active $\overline{CS}$ (Chip Select) signal.
3	$\overline{CS}$ $\overline{CHIP\ SELECT}$	Active low selects the module and enables CPU communication with the device.
4	$\overline{RE}$ $\overline{READ\ ENABLE}$	Initiates the Read mode to search for a track and sector code in the ID field equal to that in the track and sector registers.
5	A0 REGISTER ADDRESS 0	Register address line 0 for accessing the active registers with $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$. See Table 4-5.
6	A1 REGISTER ADDRESS 1	Register address line 1 for accessing the active registers with $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$. See Table 4-5.
7-14	$\overline{DAL0}$-$\overline{DAL7}$ DATA ACCESS LINES	Data Access Lines Bits 0-7.
15	STEP STEP	Step motor control that contains a pulse for each step.
16	DIRECTION DIRECTION	Direction motor control. Active high when stepping in, active low when stepping out.
17	EARLY EARLY	Indicates that the write data pulse occurring while EARLY is active (high) should be shifted early for write pre-compensation.

Table 4-4 (Cont.). Floppy Disk Formatter/Controller Signal List

PIN	SIGNAL	FUNCTION
18	LATE LATE	Indicates that the write data pulse occurring while LATE is active (high) should be shifted late for write pre-compensation.
19	$\overline{\text{MR}}$ $\overline{\text{MASTER}}$ $\overline{\text{RESET}}$	A logic low on this input resets the device and loads hex 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, hex 01 is loaded into sector register.
20	(GND) VSS	Ground.
21	VCC	+5V power input.
22	TEST	For testing only.
23	HLT HELD LOAD TIMING	A logic high indicates that the read/write head is engaged.
24	CLK	Jumper selected clock.
25	RG READ GATE	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered and is used for synchronization.

Table 4-4 (Cont.). Floppy Disk Formatter/Controller Signal List

PIN	SIGNAL	FUNCTION
26	RCLK READ CLOCK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAWREAD}}$ $\overline{\text{RAW}}$ $\overline{\text{READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HLD HEAD LOAD	Output to cause the storage element to be placed in close proximity to the Read/Write head.
29	TG43 TRACK GREATER THAN 43	This output informs the drive that the Read-Write head is positioned between the 44-76. This output is valid only during Read and Write Commands.
30	WG WRITE GATE	Write Gate output to floppy disk drive.
31	WD WRITE DATA	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data in both FM and MFM formats.
32	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.

Table 4-4 (Cont.). Floppy Disk Formatter/Controller Signal List

PIN	SIGNAL	FUNCTION
33	$\overline{WF}/\overline{UFOE}$ WRITE FAULT	This input detects writing faults indications from the drive. When WG = 1 and $\overline{WF}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{WF}$ input sould be made inactive (high) when WG becomes inactive. When WG = 0, this pin functions on a VFO enable output. $\overline{VFOE}$ is made active when the head is fully engaged and data is being inspected from the diskette.
34	$\overline{TROO}$ TRACK ZERO	Indicates that the Read/Write head is over track zero (logic low).
35	$\overline{IP}$ INDEX PULSE	Input signal to indicate when the index mark is encountered - once per revolution of the disk.
36	$\overline{WPRT}$ $\overline{WRITE}$ $\overline{PROTECT}$	This input is sampled whenever a Write Command is received. A logic low terminated the command an set the Write Protect Status bit.
37	$\overline{DDEN}$ DOUBLE DENSITY	This pin selects either single or double density operation. When DDEN=0, double density is selected. When DDEN=1, single density is selected.
38	DRQ DATA REQUEST	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively.
39	INTRQ INTERRUPT REQUEST	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read.
40	VDD	+12V power input.

Table 4-5. AM-210 Register Addresses

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Rgstr	Command Rgstr
0	1	Track Rgstr	Track Rgstr
1	0	Sector Rgstr	Sector Rgstr
1	1	Data Rgstr	Data Rgstr

4.2.1.2 ORGANIZATION.
The Floppy Disk Formatter block diagram is illustrated in Figure 4-5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register. This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register. This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated into the DAL under processor control.

Track Register. This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one

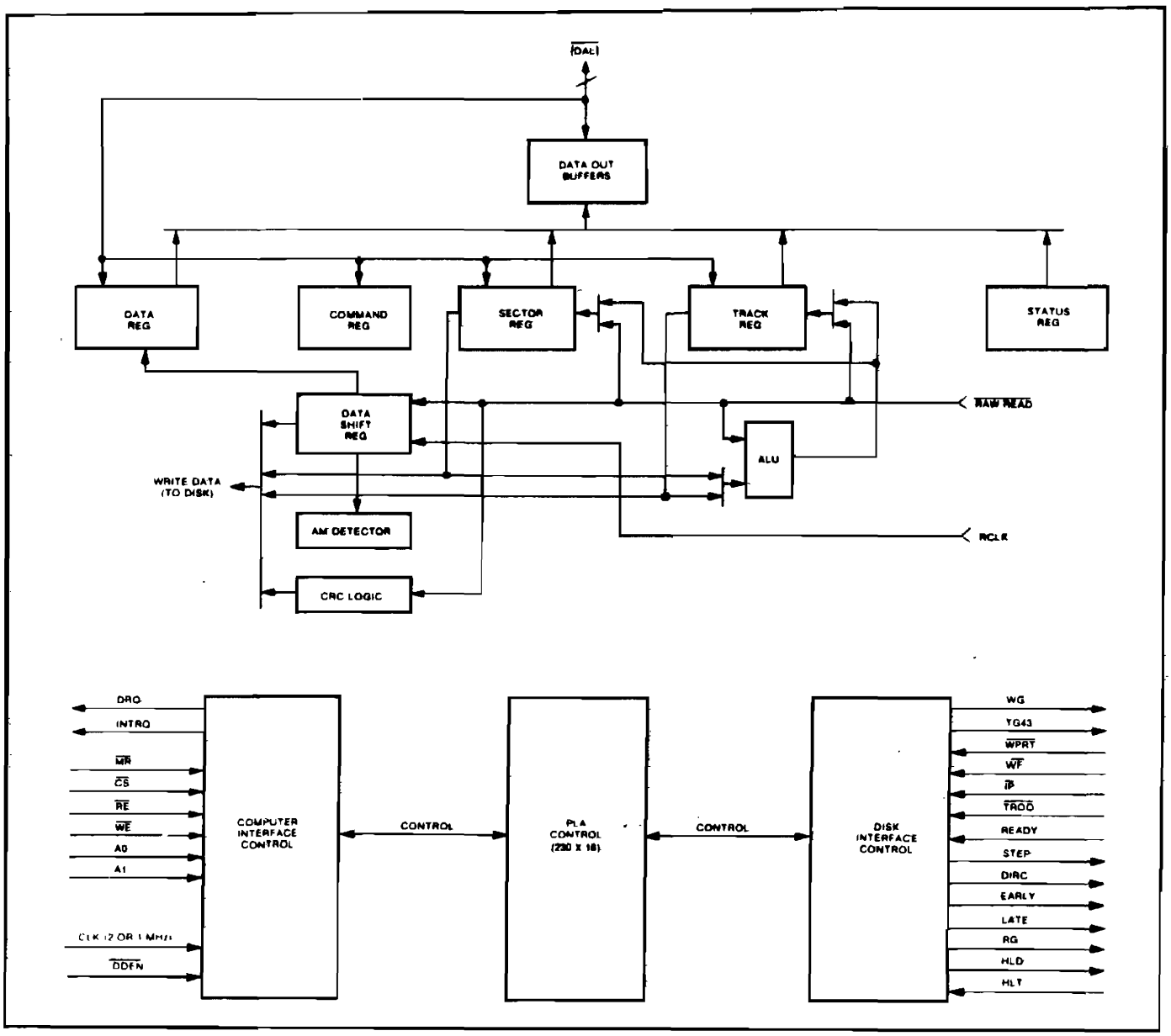


Figure 4-5. Floppy Disk Formatter/Controller Module Block Diagram

every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR). This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR). This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR). This 8-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic. This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC) The polynomial is: $G(x) = x^{16} + X^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU). The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control. All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The module has two different modes of operation according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}}$ = 0, double density (MFM) is assumed. When $\overline{\text{DDEN}}$ = 1, single density (FM) is assumed.

AM Detector. The address mark detector detects ID, data and index address marks during read and write operations.

4.2.1.3 PROCESSOR INTERFACE.

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{\text{DAL}}$) and associated control signals. The $\overline{\text{DAL}}$ are used to transfer Data, Status, and Control words out of, or into the module. The $\overline{\text{DAL}}$ are three state buffers that are enabled as output drivers when $\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$) and Read Enable ($\overline{\text{RE}}$) are active (low logic state) or act as input receivers when $\overline{\text{CS}}$ and $\overline{\text{Write Enable}}$ ($\overline{\text{WE}}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{\text{CS}}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{\text{RE}}$ during a Read operation or $\overline{\text{WE}}$ during a Write operation, are interpreted as selecting the following registers:

A1-A0	READ ($\overline{\text{RE}}$)	WRITE ($\overline{\text{WE}}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the module and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command, an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

4.2.1.4 FLOPPY DISK INTERFACE.

The module has two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 Mhz. However, when interfacing with the mini-floppy, the CLK input is set at 1 Mhz for both single density and double density. When the

clock is at 2 Mhz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 Mhz, these times are doubled.

4.2.1.5 HEAD POSITIONING.

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the rate field in bits 1 and 0 of the command word (r0, r1). After the last directional step, an additional 15 milliseconds of head setting time takes place if the Verify flag is set in Type 1 commands. Note that this time doubles to 30 ms for a 1 Mhz clock. If $\overline{\text{TEST}}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type 2 or 3 command. (See paragraph 4.2.1.9 for a description of command types.)

The rates (shown in Table 4-6) can be applied to a Step-Direction Motor through the device interface.

Table 4-6. Stepping Rates

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{\text{DDEN}}$	0	1	0	1	x	x
R1 R0	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=0	$\overline{\text{TEST}}$=0
0 0	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
0 1	6 ms	6 ms	12 ms	12 ms	200 µs	400 µs
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	15 ms	15 ms	30 ms	30 ms		

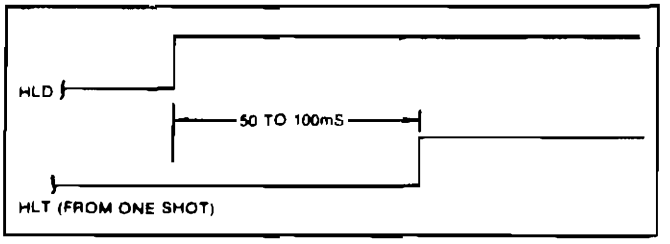
Step. A 2 µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC). The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 µs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The module must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise, the seek error is set and an INTRQ is generated.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type 1 command if the h flag is set (h = 1), at the end of the Type 1 command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active, it remains active until either a Type I command is received with (h = 0 and V = 0); or if the module is in an idle state (non-busy) and 15 index pulses have occurred, it is reset.

Head Load Timing (HLT) is an input to the module which is used for the head engage time. When HLT = 1, the module assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on the drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the module.



HEAD LOAD TIMING

When both HLD and HLT are true, the module reads from or writes to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled, nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the module waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the module then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

4.2.1.6 DISK READ OPERATIONS.

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector Length byte in the ID field is zero, then the sector length is 128 bytes. If 01, then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the module is concerned can be from 1 to 255 sectors. The number of tracks as far as the module is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

For read operations, the module requires $\overline{\text{RAW}}$ $\overline{\text{READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives; but if not, it may be derived externally by Phase lock loop, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which informs some phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The module must find an address mark within the next 10 bytes; otherwise, RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the module is deriving any useful information from the data stream. Similarly for MFM, RG is made active true when 4 bytes of "00" or "FF" are detected. The module must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

4.2.1.7 DISK WRITE OPERATION.

When writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the module before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault, the module terminates the current command, and sets the Write Fault bit

(bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

For write operation, the module provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$=1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$=0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write pre-compensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on Pin 30 is to be written early. EARLY is valid for the duration of the pulse. LATE is active true when the WD pulse is to be written late. If both are low when a WD pulse is present, the WD pulse is to be written at nominal. Since write pre-compensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several delay lines which are located external to the module. The write pre-compensation signals EARLY and LATE are valid in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received, the module samples the Ready input. If this input is logic low, the command is not executed and an interrupt is generated. The Seek or Step Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

4.2.1.8 COMMAND DESCRIPTION.

The module accepts eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status

bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 4-7.

Table 4-7. Command Summary

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	X	E	0	0
II	Write Sector	1	0	1	m	X	E	X	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	X
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

X = Don't care Note: Bits shown in TRUE form.

4.2.1.9 TYPE I COMMANDS.

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 4-6. See Figure 4-6 for Type I command flow.

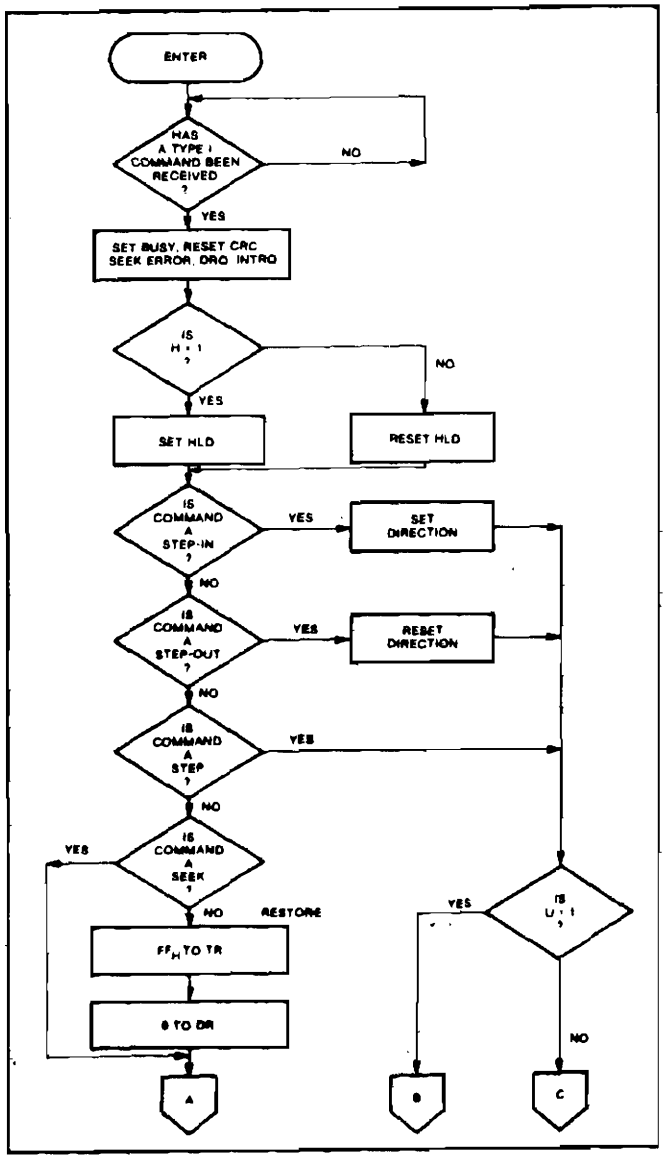


Figure 4-6. Type I Command Flow (Sh 1 of 2)

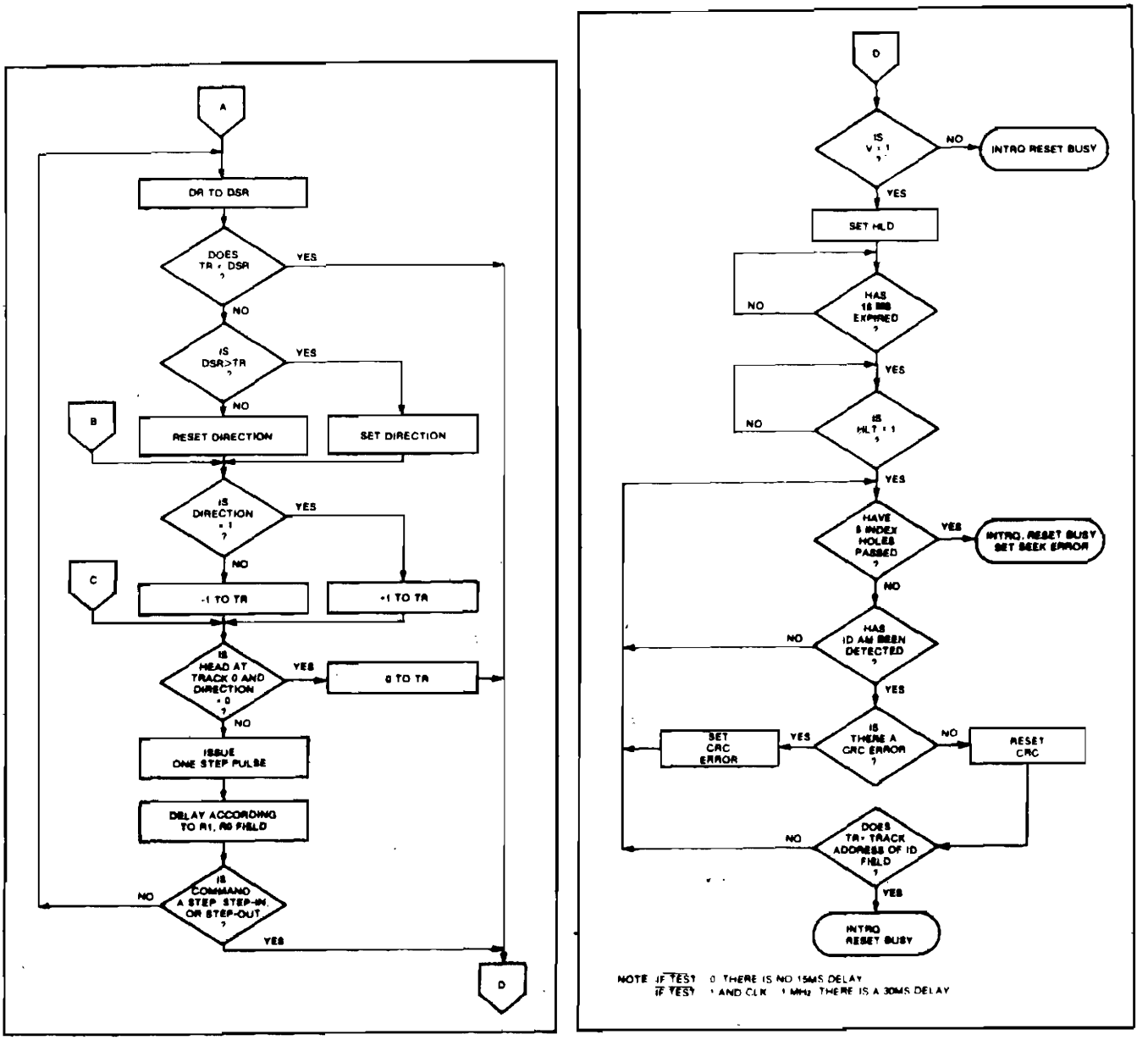


Figure 4-6. Type I Command Flow (Sh 2 of 2)

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head remains engaged until the module receives a command that specifically disengages the head. If the module is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive). See Table 4-8 for a summary of flags for Type I commands.

Table 4-8. Flag Summary Type I Commands

h = Head Load Flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Unload head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 4- for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed; if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field and the track address of the ID field is read off the disk. The track address

of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is a valid ID CRC, an interrupt is generated; and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the module terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-in, and Step-out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

Restore (Seek Track 0). Upon receipt of this command, the Track 00 ($\overline{\text{TR00}}$) input is sampled. If $\overline{\text{TR00}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not active low, stepping pulses (pins 15 to 16), at a rate specified by the r_1r_0 field, are issued until the $\overline{\text{TR00}}$ input is activated. At this time, the TR is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TR00}}$ input does not go active low after 255 stepping pulses, the module terminates operation, interrupts, and sets the Seek error status bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

Seek. This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number.

The module updates the Track register and issues stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step. Upon receipt of this command, the module issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-in. Upon receipt of this command, the module issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-out. Upon receipt of this command, the module issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

4.2.1.10 TYPE II COMMANDS.

The Type II Commands are the Read Sector(s) and Write Sector(s) commands. See Figure 4-7 for Type II Command flow. See Table 4-9 for Flag Summary. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown below.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

Table 4-9. Flag Summary Type II Commands

TYPE II
m = Multiple Record flag (Bit 4)
m = 0, Single Record
m = 1, Multiple Records
a_0 = Data Address Mark (Bit 0)
a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)
E = 15 ms Delay
E = 1, 15 ms delay
E = 0, no 15 ms delay

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

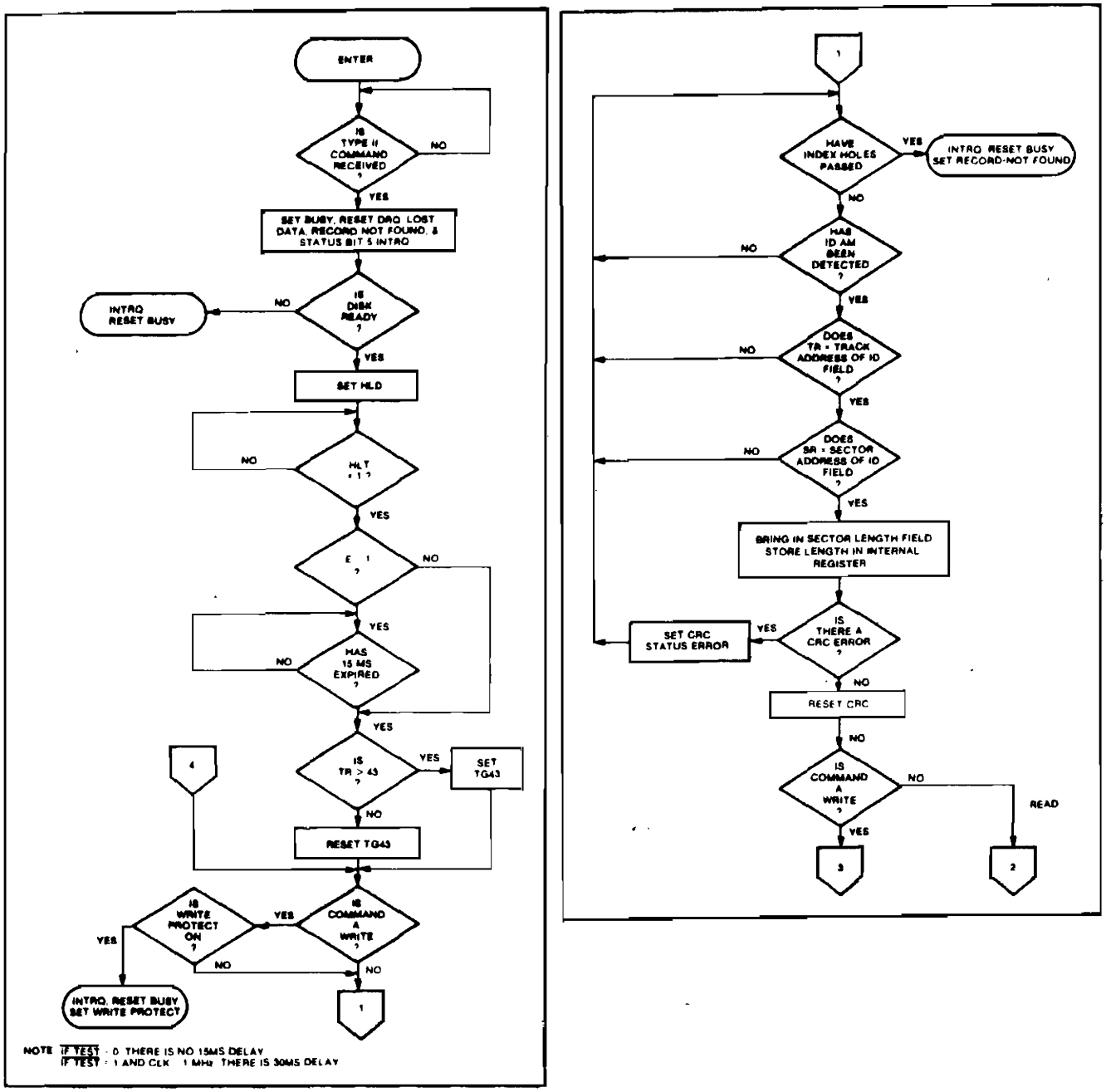


Figure 4-7. Type II Command Flow (Sh 1 of 2)

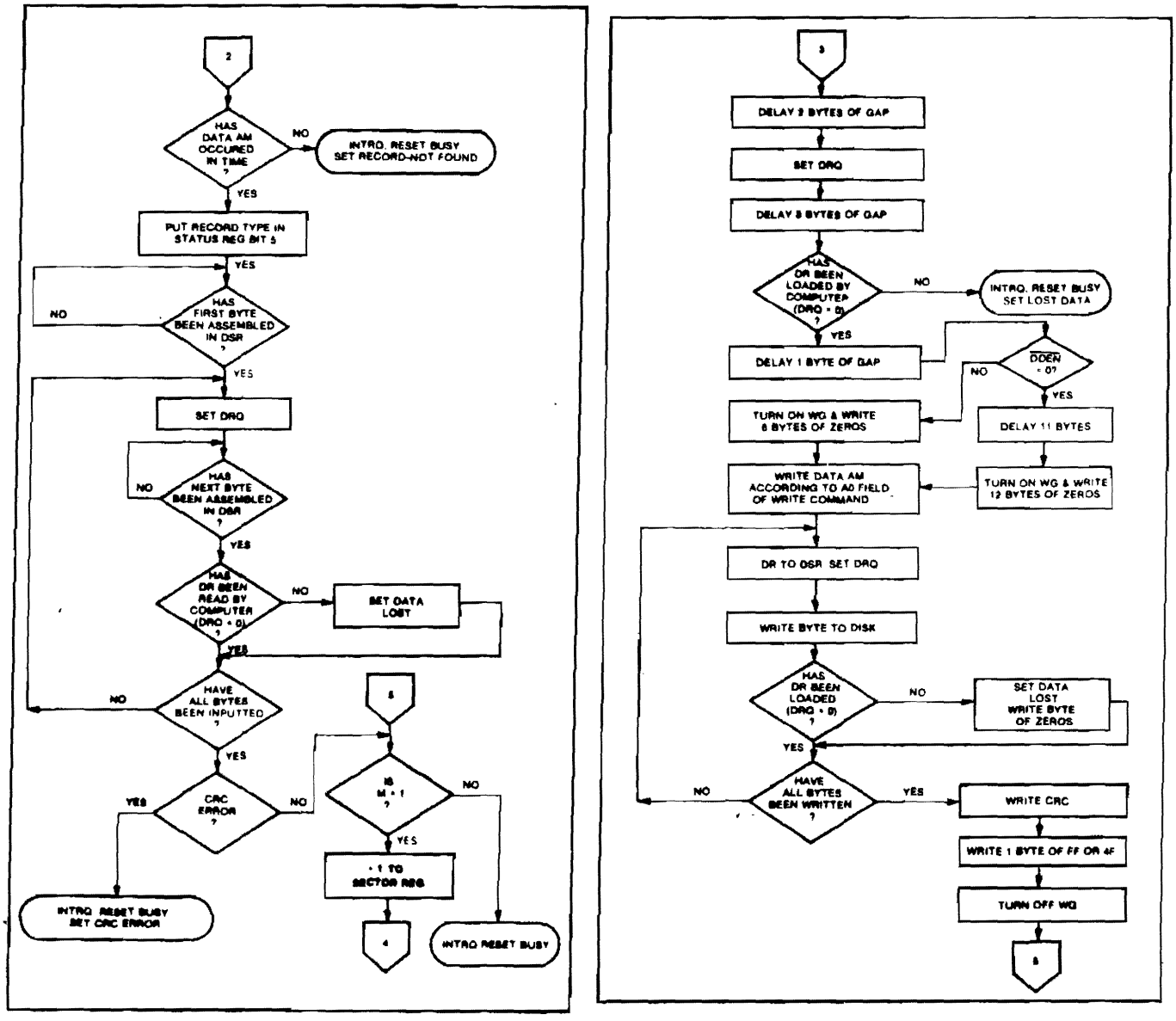


Figure 4-7. Type II Command Flow (Sh 2 of 2)

When an ID field is located on the disk, the module compares the Track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The module must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status Bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The module continues to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

Read Sector. Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set; and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte. If not, the RECORD Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector. Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The module counts off 11 bytes in single density and 22 bytes in double density from the CRC field, and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time, the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The module then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or 4F in MFM. The WG output is then deactivated.

4.2.1.11 TYPE III COMMANDS.

Read Address. Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 2	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the module checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation, an interrupt is generated and the Busy Status is reset.

Write Track. Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the

interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in Table 4-10. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. See Figure 4-8 for flow diagrams for Command Write Track.

Table 4-10. Control Bytes for Initialization

DATA PATTERN IN DR (HEX)	FD1791 INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with Clk = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5
**Missing clock transition between bits 3 and 4

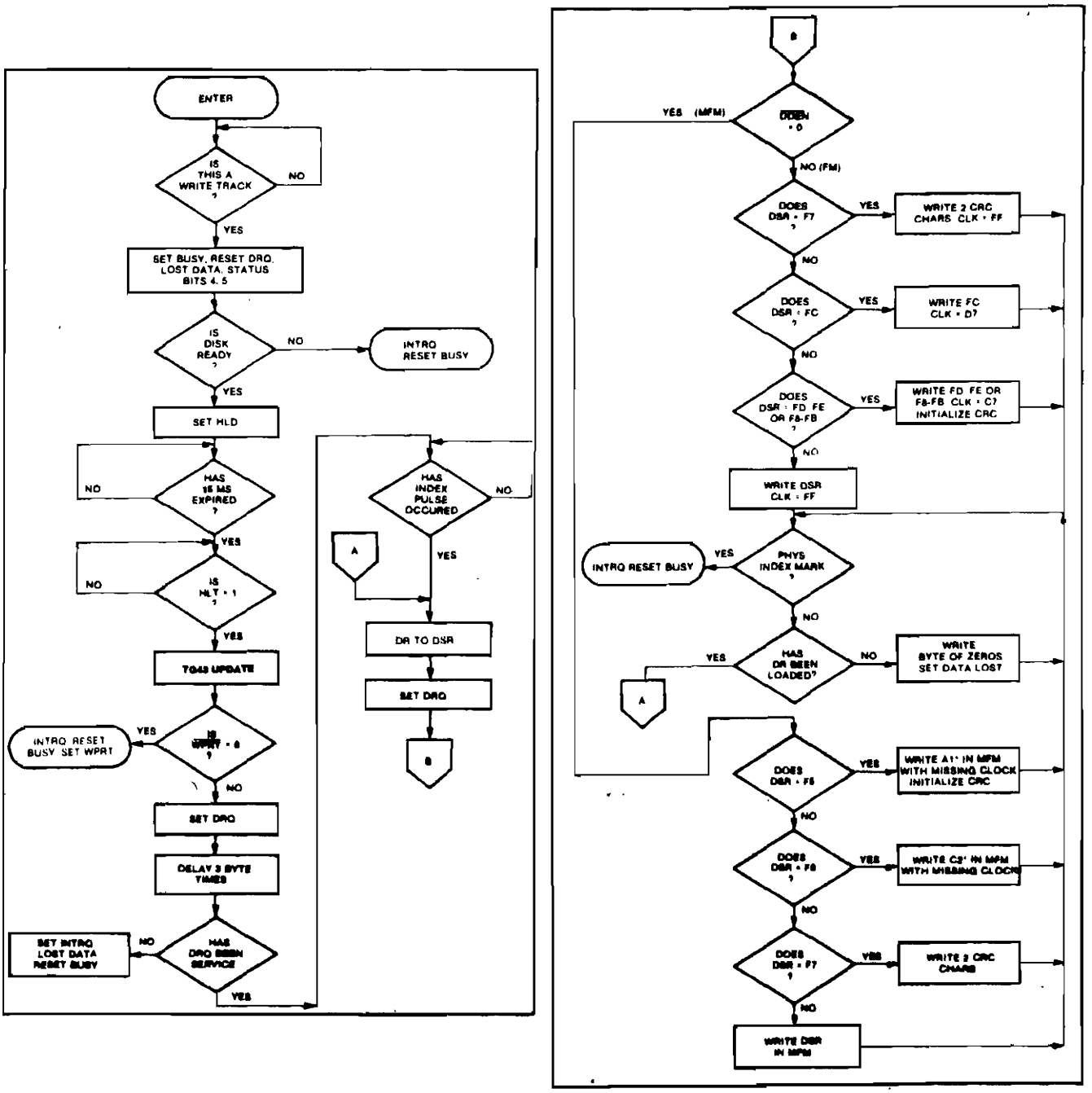


Figure 4-8. Type III Command Write Track

4.2.1.12 TYPE IV COMMAND.

Force Interrupt. This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

4.2.1.13 STATUS DESCRIPTION.

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4-11. Tables 4-12 and 4-13 show status bits for Type 1, 2 and 3 commands.

Table 4-11. Status Register Summary

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	0	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Table 4-12. Status for Type I Commands

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

Table 4-13. Status Bits for Type II and III Commands

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

4.2.1.14 FORMATTING THE DISK.
(Refer to Figure 4-8 for Type III flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the module raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever

data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the module detects a data pattern on F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM, an FE pattern is interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes. See Figure 4-9 for IBM Track format.

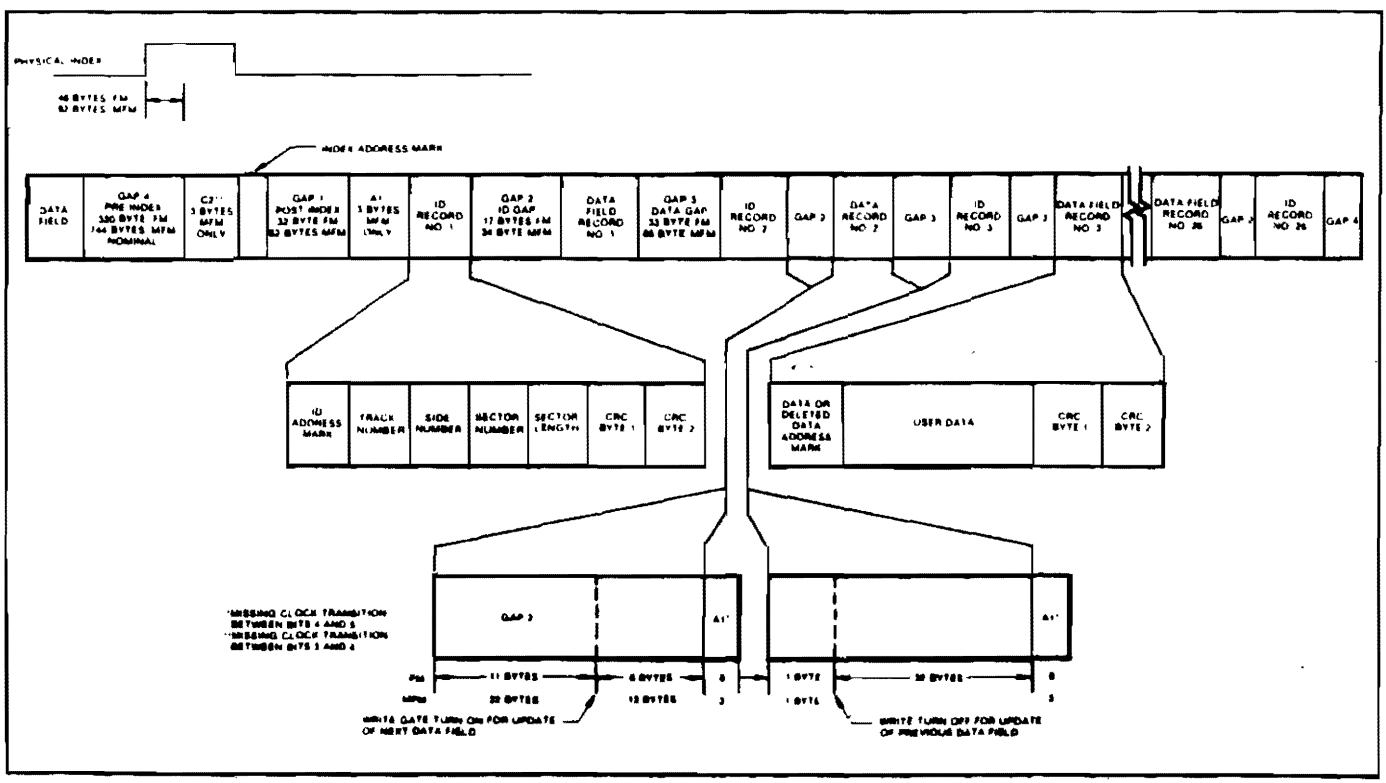


Figure 4-9. IBM Track Format

16 SECTORS X2 SIDES X77 TRACKS = 2464
X512 = 1.26 M

4.2.1.15 IBM 3740 FORMAT - 128 BYTES/SECTOR.

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF
6	00
1	FC (Index Mark)
26	FF
* 6	00
1	FE (ID Address Mark)
1	Track Number
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF
247**	FF

*Write bracketed field 26 times.

**Continue writing until module interrupts out.
Approx. 247 bytes.

4.2.1.16 IBM SYSTEM 34 FORMAT - 256 BYTES/SECTOR.

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES		HEX VALUE OF BYTE WRITTEN
	80	4E
	12	00
	3	F6
	1	FC (Index Mark)
	50	4E
*	12	00
	3	F5
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	Side Number (0 or 1)
	1	Sector Number (1 thru 1A)
	1	01
	1	F7 (2 CRCs written)
	22	4E
	12	00
	3	F5
	1	FB (Data Address Mark)
	256	DATA
	1	F7 (2 CRCs written)
	54	4E
	598**	4E

*Write bracketed field 26 times.

**Continue writing until module interrupts out.
Approx. 598 bytes.

4.2.1.17 NON-IBM FORMATS.

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512 or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the module.

	FM	MFM
Gap I	16 bytes FF	16 bytes 4E
Gap II *	11 bytes FF 6 bytes 00	22 bytes 4E 12 bytes 00 3 bytes A1
Gap III **	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

4.2.1.18 TIMING CHARACTERISTICS.

T_A=0°C to 70°C, V_{DD}=+12V ±.6V, V_{SS}=0V, V_{CC}=+5V ±.25V.

NOTE: Timings are given for 2 Mhz Clock. For those timings noted, values will double when chip is operated at 1 Mhz.

Read Operations. For timing characteristics see Table 4-14 and Figure 4-10.

Table 4-14. Read Operations Timing

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	0			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

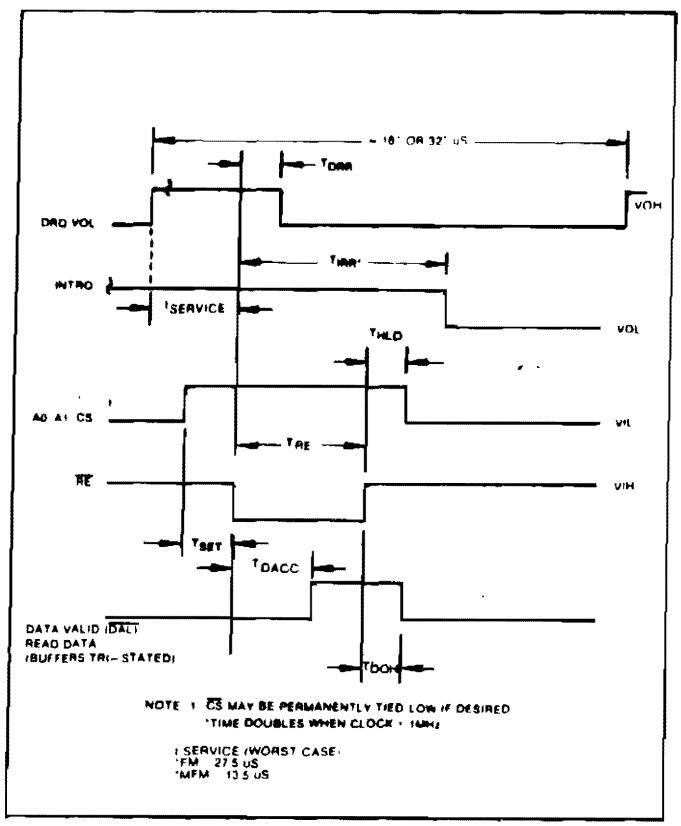


Figure 4-10. Read Enable Timing

Write Operations. For timing characteristics see Table 4-15 and Figure 4-11.

Table 4-15. Write Operations Timing

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

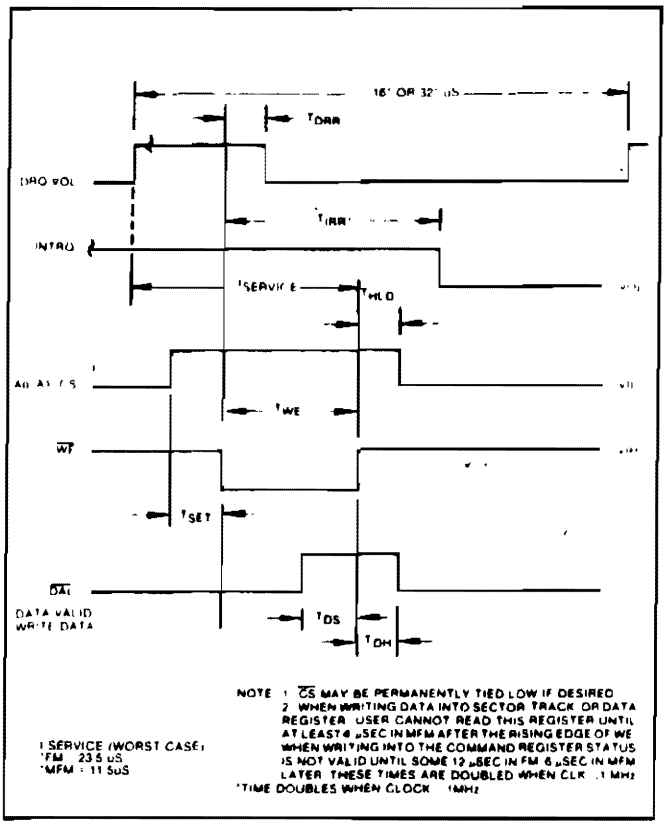
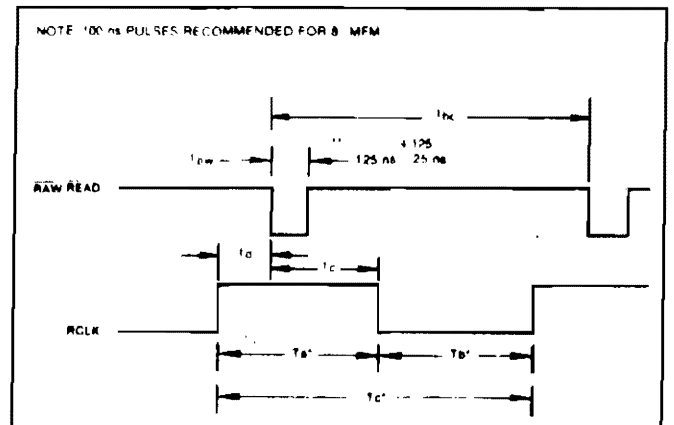


Figure 4-11. Write Enable Timing

Miscellaneous Timing. See Table 4-16 and Figures 4-12 and 4-13 for timing characteristics.

Table 4-16. Miscellaneous Timing

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230			nsec	
TCD_2	Clock Duty (high)	200			nsec	
TSTP	Step Pulse Output	2 or 4			µsec	
TDIR	Dir Setup to Step	12			µsec	See Note
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	10			µsec	



				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a*	T_b*	T_c*
8"	MFM	0	2 MHz	1 µs	1 µs	2 µs
8"	FM	1	2 MHz	2 µs	2µs	4 µs
5"	MFM	0	1 MHz	2 µs	2µs	4 µs
5"	FM	1	1 MHz	4 µs	4 µs	8 µs

Figure 4-12.
Input Data Timing

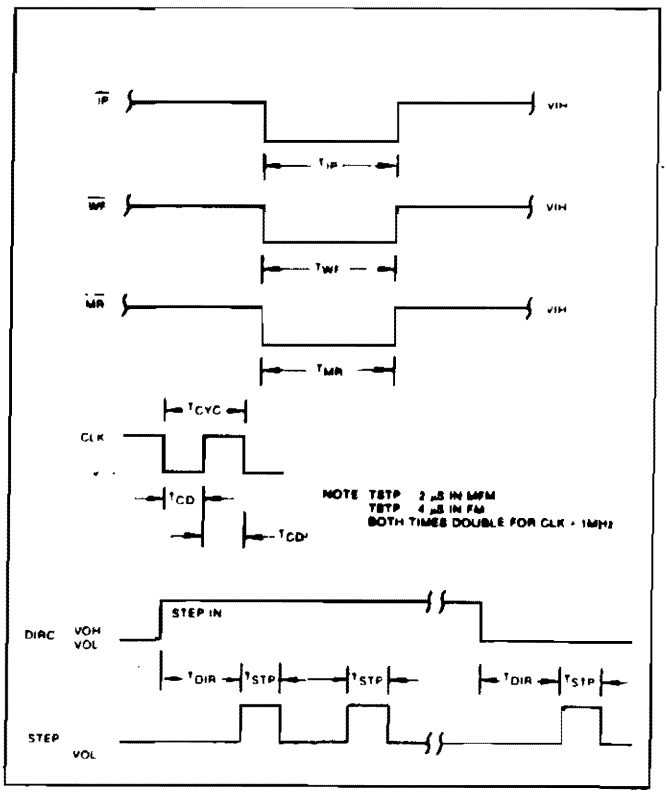


Figure 4-13.
Miscellaneous Timing

NOTES:

1. Pulse width on $\overline{\text{RAW READ}}$ (p.27) is normally 125 $^{+125}_{-25}$ ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. When flux reversals are totally nonexistent, the external separator should insure $\overline{\text{RAW READ}}$ = 1. Also, RCLK should be free running at all times.
3. t_{bc} (see input data timing) should be 2, 3, or 4 μs nominal in MFM and 2 or 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. In MFM, the EARLY and LATE signals are valid at least 125 ns from either edge of WD.

4.2.2 1024 x 4 BIT STATIC RAM (U30, U31).

This device is a 4096-bit static Random Access Memory (RAM) organized as 1024 words by four bits. It uses fully DC stable (static) circuitry throughout and requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. For logic and connections, see Figure 4-14. For Read and Write Timing, see Figure 4-15.

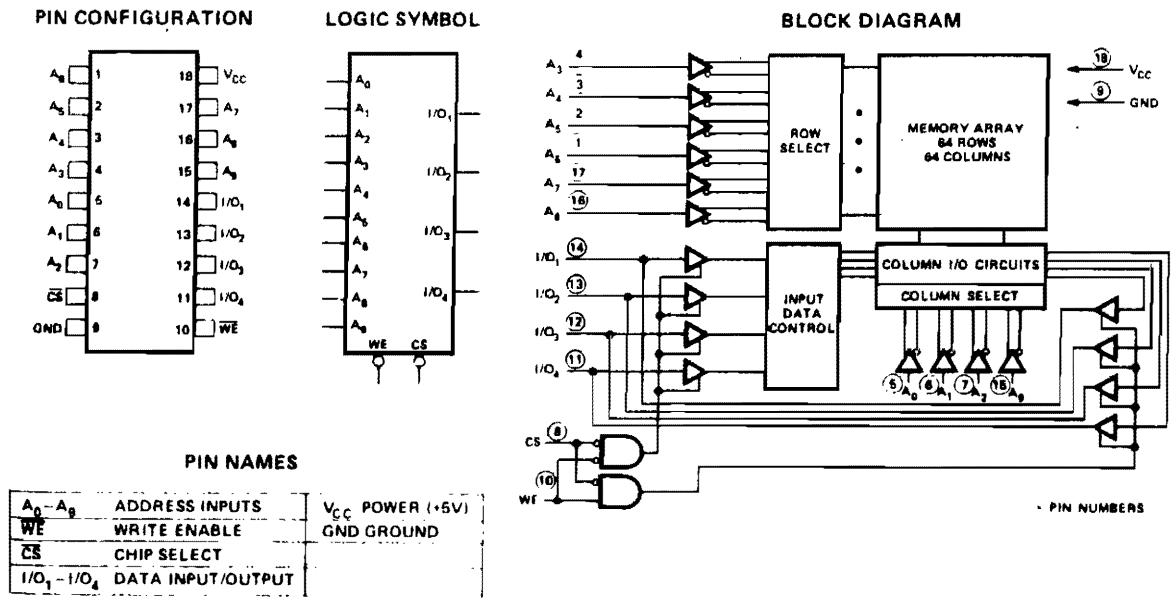
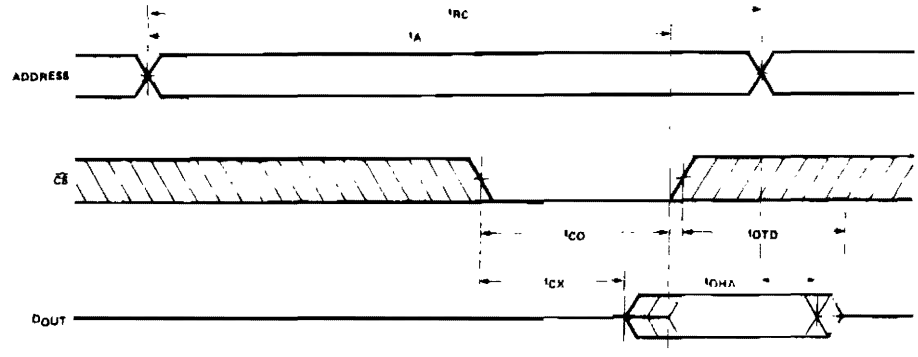
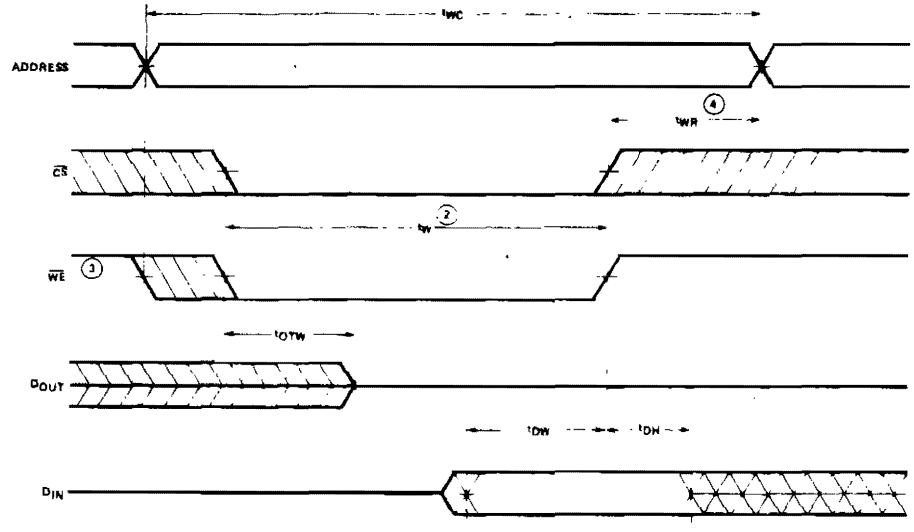


Figure 4-14. Static RAM Connections

READ CYCLE ①



WRITE CYCLE



NOTES:
① $\overline{WE}$ is high for a Read Cycle.
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to $\overline{WE}$ going high.
③ $\overline{WE}$ must be high during all address transitions.
④ t_{WR} is referenced to the high transition of $\overline{WE}$.

Figure 4-15. RAM Read and Write Timing

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the address, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be affected by $\overline{WE}$, the addresses, nor the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself - or in conjunction with the other - can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time - defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

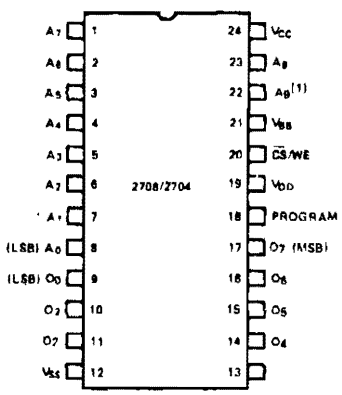
Internal delays on the 2114 are established such that address decoding propagates ahead of data inputs (keyed by the Write time). Therefore, it is permissable to establish the addresses coincident to the selection of a Write time, but no later. If the Write time precedes the addresses, the data in the previously addressed locations, or some other location, may be inadvertently changed.

While it is important that the addresses remain stable for the entire Write cycle, the data inputs are not required to remain stable. Appropriate voltage levels will be written into the cells as long as the data is stable for t_{DW} at the end of the Write time.

4.2.3 8K UV ERASABLE PROM (U21).

This device is a 1K x 8 (8192) bit ultraviolet light erasable and electrically reprogrammable EPROM. The outputs are three-state, allowing direct interface with common system bus structures. Device connections are shown in Figure 4-16 and timing is shown in Figure 4-17.

PIN CONFIGURATION

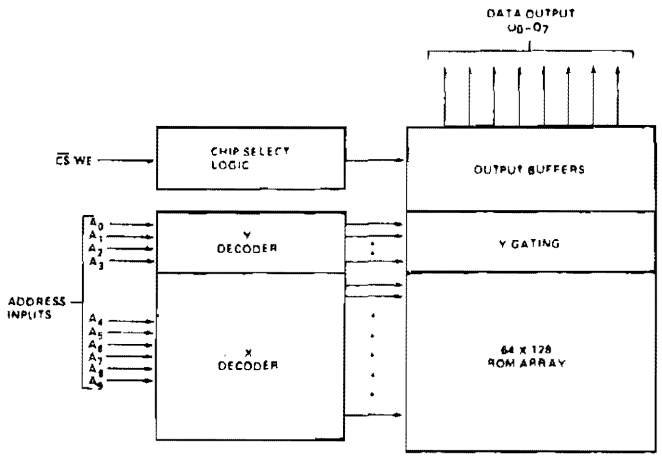


NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704

PIN NAMES

A_0 A_9	ADDRESS INPUTS
O_1 O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9 11, 13 15	ADDRESS INPUTS 1 8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

Figure 4-16. 8K UV Erasable PROM Connections

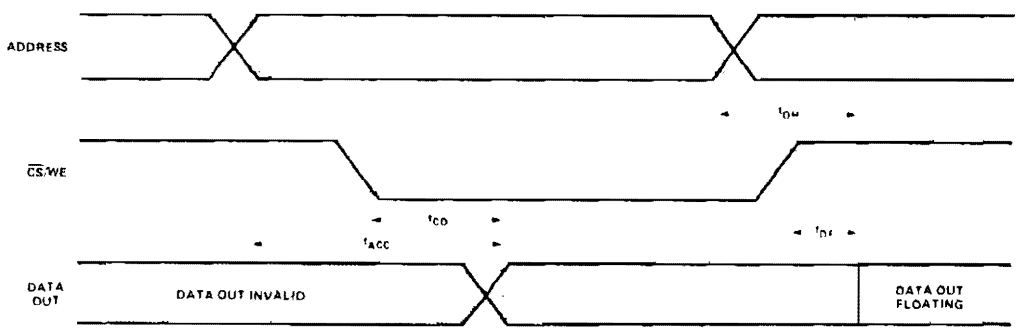


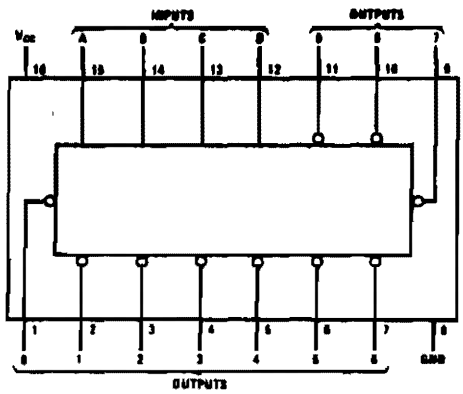
Figure 4-17. 8K UV Erasable PROM Timing

Erasure Characteristics. The erasure characteristics of this device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000A range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If this device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available which should be placed over the window to prevent unintentional erasure.

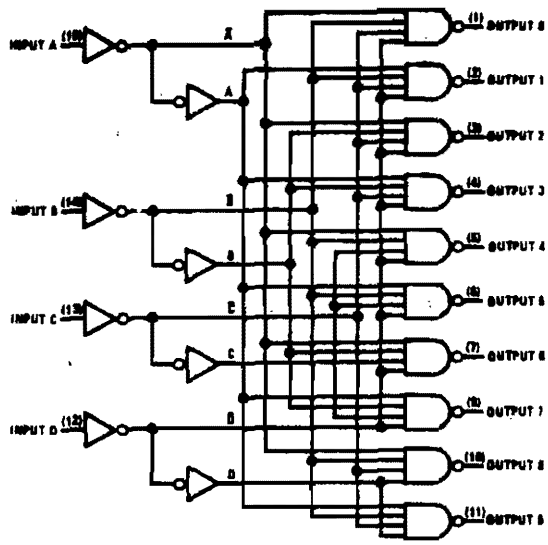
4.2.4 BCD/DECIMAL DECODER/DRIVER (U13).

This device consists of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. For logic and truth table, see Figure 4-18.

Connection Diagram



Logic Diagram



Truth Table

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

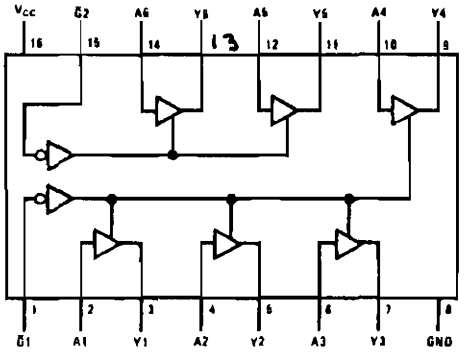
H = High Level (Off), L = Low Level (On)

Figure 4-18. Decoder/Driver Logic and Connections

4.2.5 TRI-STATE BUFFERS (U16).

These devices provide six, two-input buffers in each package. One of the two inputs to each buffer is used as a control line to gate the output onto the high-impedance state, while the other input passes the data through the buffers. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. Logic and connections are shown in Figure 4-19.

Logic and Connection Diagram



Truth Table

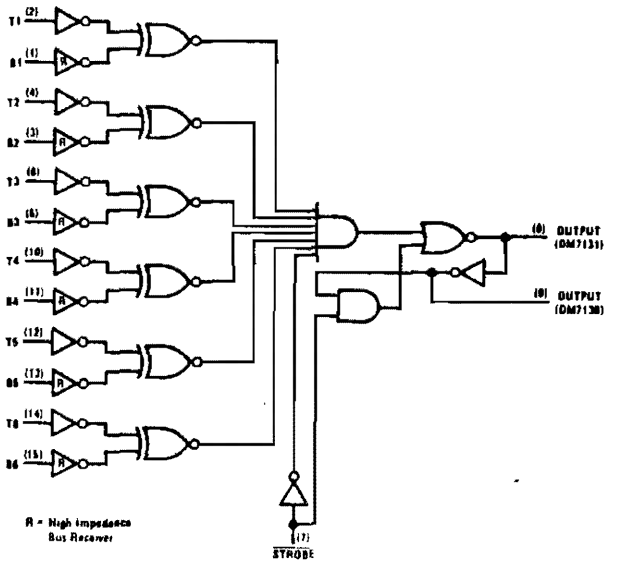
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

Figure 4-19. Tri-State Buffer Connections

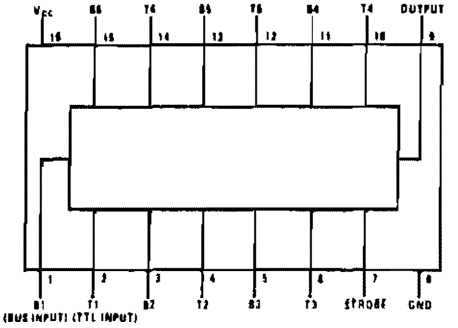
4.2.6 BUS COMPARATOR (U25, U26).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logical 1 to a logical 0 state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logical 1 level, without affecting the state of the output. Logic and connections are shown in Figure 4-20.

Logic Diagram



Connection Diagram



Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	L
T ≠ B	L	H

*Latched in previous state

Figure 4-20. Bus Comparator Connections

4.2.7 D POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR (U12) (U16).

Truth Table

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

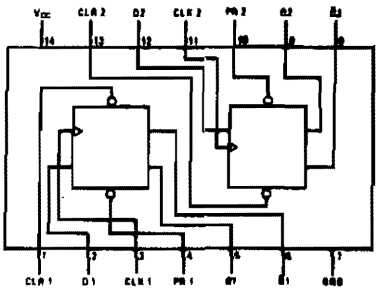
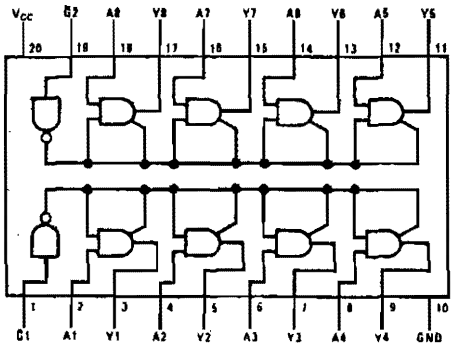


Figure 4-21. D Flip-Flop Connections

4.2.8 TRI-STATE OCTAL BUFFERS (U36).

This device provides six, two-input buffers in each package. One of the two inputs is used as a control line to gate the output into a high impedance state, while the other passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. See Figure 4-22 for logic diagram and truth table.

Logic Diagram



Truth Table

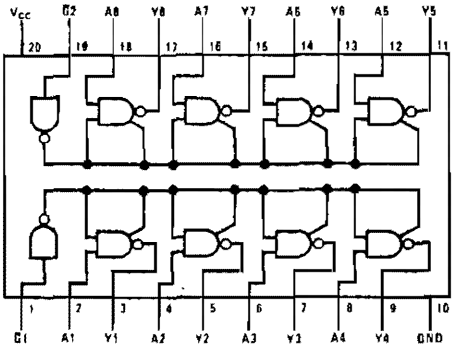
INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Z
L	H	H
L	L	L

Figure 4-22. Tri-State Octal Buffer Connections

4.2.9 TRI-STATE BUFFERS (U39).

This device provides eight, two-input buffers in each package that employs low power Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the enable pins. See Figure 4-23 for logic diagram and truth table.

Logic and Connection Diagram



Truth Table

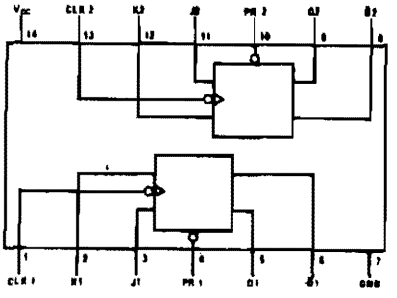
INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Figure 4-23. Tri-State Buffer Connections

4.2.10 DUAL J-K NEGATIVE-EDGE TRIGGERED FLIP-FLOPS WITH PRESET (U8).

See Figure 4-24 for logic diagram and truth table.

Connection Diagram



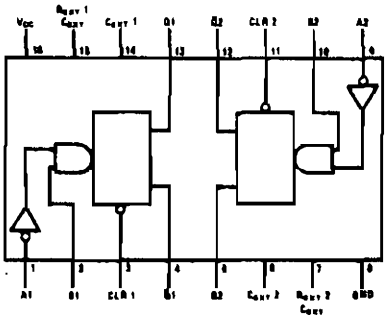
Truth Table

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

Figure 4-24. J-K Flip-Flop Connections

4.2.11 DUAL RETRIGGERABLE ONE-SHOTS WITH CLEAR (U14, U18). See Figure 4-25 for logic diagram and truth table.

Logic Diagram



Truth Table

INPUTS			OUTPUTS	
A	B	CLR	Q	$\bar{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

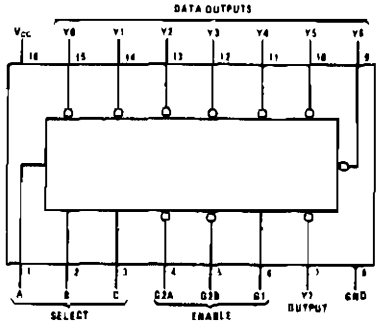
Notes: ⎍ = one high-level pulse, ⎎ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

Figure 4-25. One-Shot Connections

4.2.12 DECODER (U29).

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines, based on the conditions at the three binary select inputs and the three enable inputs. See Figure 4-26 for logic diagram and truth table.

Connection and Logic Diagram



Truth Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

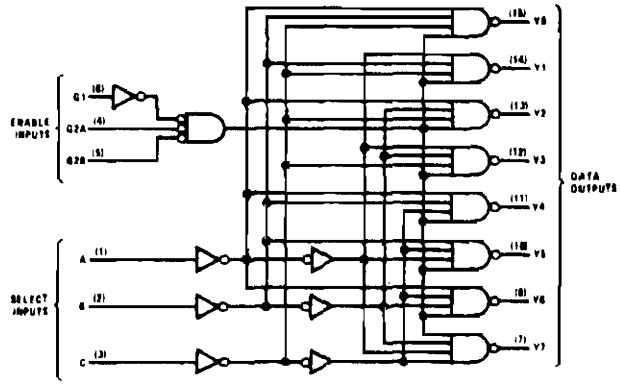
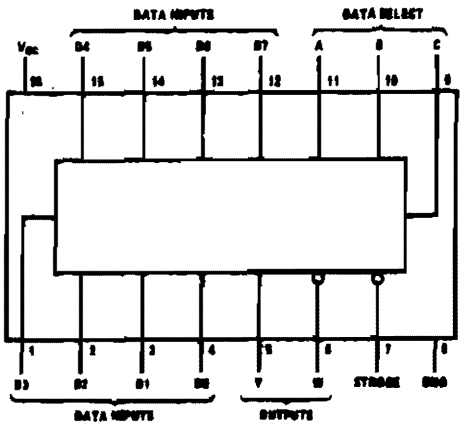
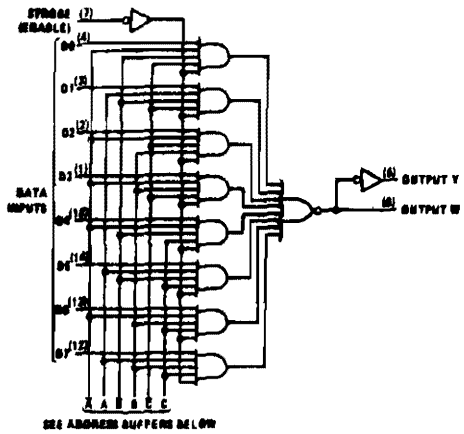


Figure 4-26. Decoder Connections

4.2.13 DATA SELECTOR/MULTIPLEXER (U17).

This device contains decoding and multiplexing to select one of eight data sources. A strobe input must be set at a low logic level to enable the device. A high level at the strobe forces the W output high and the Y output low. For logic and truth table, see Figure 4-27.





INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

D0, D1 . . . D7 = the level of the respective D input

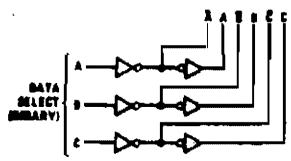


Figure 4-27. Data Selector/Multiplexer Connections

4.2.14 TRI-STATE INVERTER BUFFER (U33, U40).
This device is an octal inverter buffer for interface between tri-state busses. See Figure 4-28 for connections and truth table.

Pin Configuration

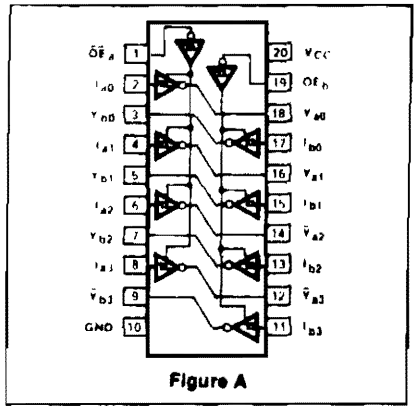


Figure A

Truth Table

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

Figure 4-28. Tri-State Inverter Buffer Connections

4.2.15 TRI-STATE OCTAL BUFFER (U41).
This device is a non-inverting octal buffer for interface between tri-state busses. See Figure 4-29 for connections and truth table.

Pin Configuration

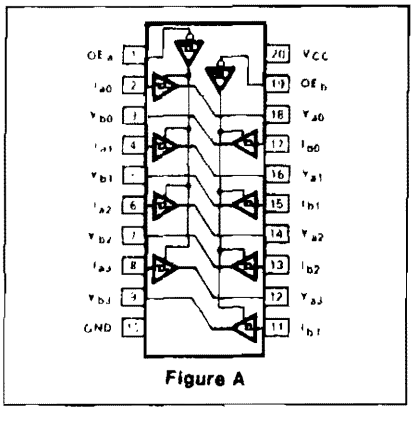


Figure A

Truth Table

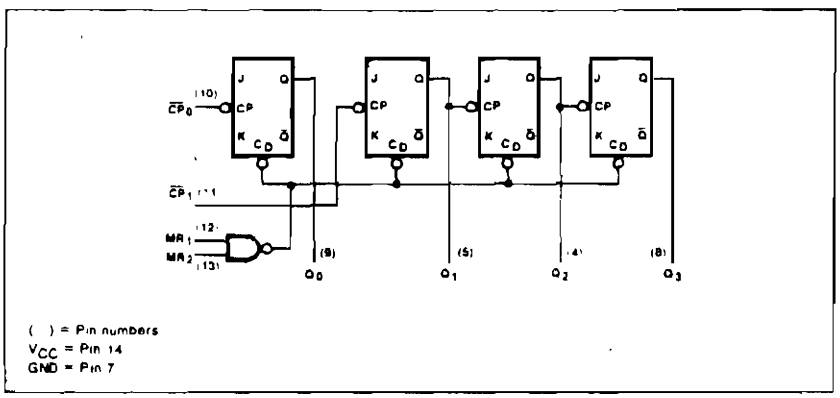
INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

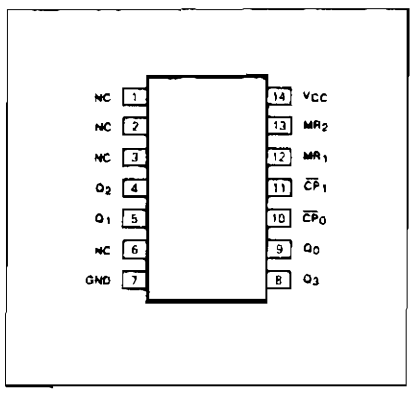
Figure 4-29. Tri-State Buffer Connections

4.2.16 FOUR-BIT BINARY RIPPLE COUNTER (U23).
This device is a high-speed four-bit ripple type counter divided into two sections. The counter has a divide-by-two section and a divide-by-eight section which are triggered by high-to-low transitions on the clock inputs. Either section can be used separately or tied together (Q_0 to CPI) to form a modulo-16 counter. The counter has a two-input gated master reset (clear). See Figure 4-30 for logic diagram and truth table.

Logic Diagram



Pin Configuration



Truth Table

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to input $\overline{CP}_1$

Mode Selection

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H HIGH voltage level
L LOW voltage level
X Don't care

Figure 4-30. Four-Bit Binary Ripple Counter Connections

4.2.17 VOLTAGE CONTROLLED OSCILLATOR (U12).

This device is a voltage controlled oscillator with range control and complementary outputs. The output frequency is established by a single external component, either a capacitor or a crystal, in combination with the voltage-sensitive inputs; one for frequency control and the other for frequency range. These inputs can be used to vary the output frequency by changing the voltage applied to them. An enable input provides control of the device output. A low enable input enables the output and a high enable produces a high output for Y and a low for Y. See Figure 4-31 for device connections.

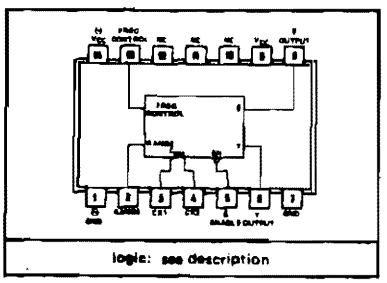
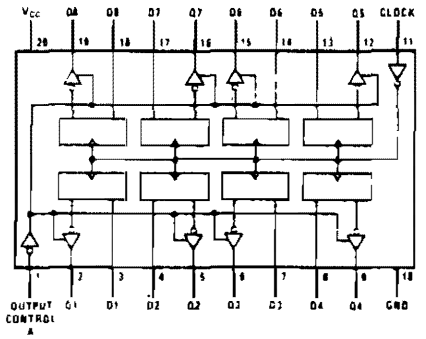


Figure 4-31. Voltage Controlled Oscillator Connections

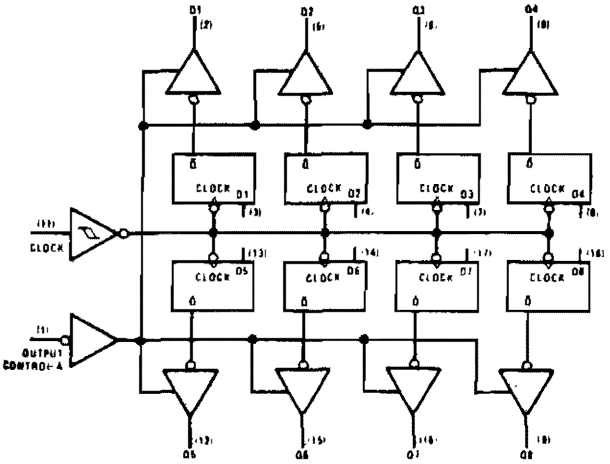
4.2.18 TRI-STATE D FLIP-FLOPS (U43).

These 8-bit registers contain D-Type flip-flops with totem-pole tri-state outputs capable of driving highly capacitive or low impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. See Figure 4-32 for logic diagram and truth table.

Connection Diagram



Logic Diagram



Truth Table

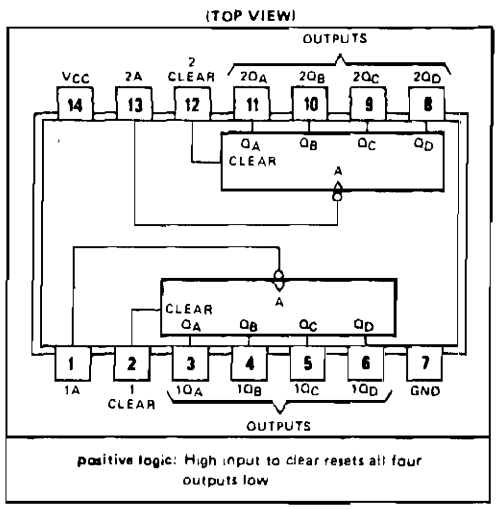
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

Figure 4-32. Tri-State D Flip-Flop Connections

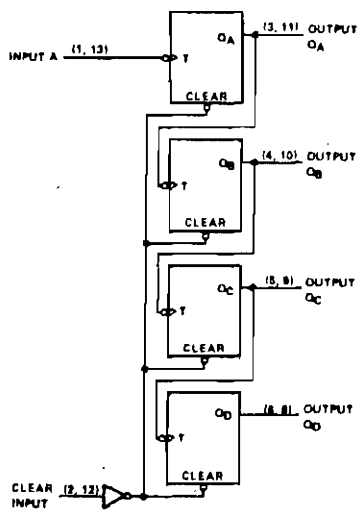
4.2.19 DUAL 4-BIT BINARY COUNTER (U9, U20).

These devices contain eight master-slave flip-flops and additional gating to implement two individual four bit counters in a single package, each with a clear and clock input. Parallel outputs are available from each counter so that any submultiple of the input count frequency is available. See Figure 4-33 for logic diagram and truth table.

Connection Diagram



Logic Diagram



Truth Table

COUNT SEQUENCE (EACH COUNTER)

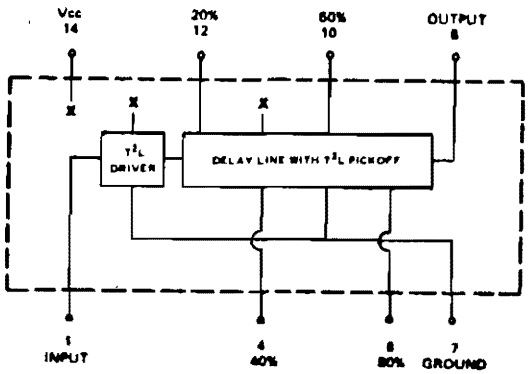
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 4-33. 4-Bit Binary Counter Connections

4.2.20 LOGIC DELAY MODULE (U6).

This device is a logic delay module that provides tapped delays with required driving and pick-off circuitry contained in one package. The taps are provided at 20% increments of total delay. The device accepts either a logic one or zero inputs and reproduces the logic at the selected output tap without inversion. Block diagram and connections are shown in Figure 4-34.

Block Diagram



Connections

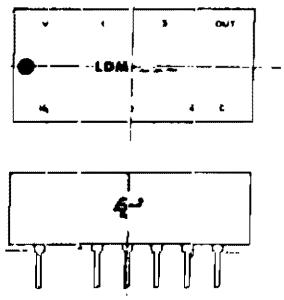


Figure 4-34. Logic Delay Module Diagram and Connections.

4.2.21 PROGRAMMABLE READ-ONLY MEMORY (U19).

This device is a Programmable Read-Only Memory (PROM) that features full Schottky clamping and tri-state outputs. The device can be programmed at any bit location and is irreversible, once altered. An active level at the chip select input enables all of the outputs. An inactive level at the chip select input causes all outputs to be off. Capacity is 256 bits or 32 words by 8 bits. Connections and I/O circuits are shown in Figure 4-35.

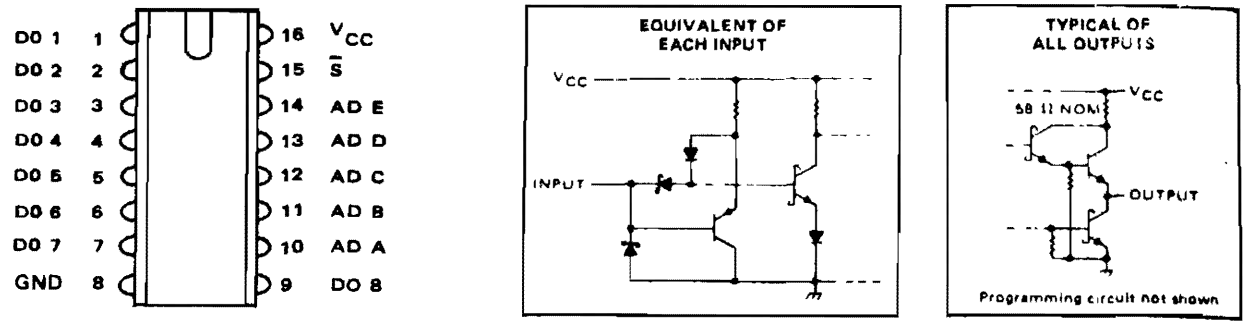
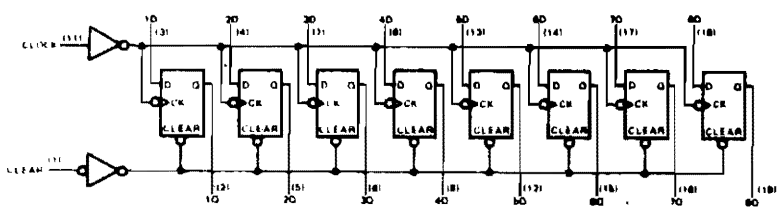


Figure 4-35. PROM Connections and I/O Circuits

4.2.22 OCTAL D-TYPE FLIP-FLOP WITH CLEAR (U34, U35). These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-36.

Logic Diagram



Truth Table

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Connections

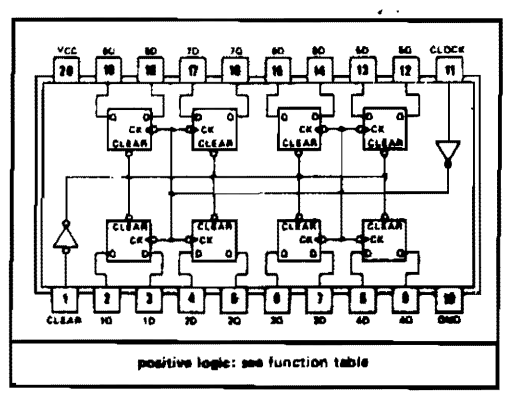


Figure 4-36. D Flip-Flop Connections

SECTION 5
MAINTENANCE AND TROUBLESHOOTING

5.0 INTRODUCTION.

The AM-210 circuit board performs to full capability with a minimum of maintenance. This Section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-210 circuit board was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections Two and Three of this manual are met. Should a problem arise after the circuit card has been in operation, use the following procedures to identify and locate the fault.

1. Check all cabling for proper seating of connectors.

2. Check the circuit board for proper seating in the slot.

3. Check all power connections for correct voltages.

4. Check jumper options to ensure correctness of application.

5. Verify that the fault is in the AM-210 and not in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board.

6. Perform the diagnostics tests included with the circuit board as described in paragraph 5.3.

5.2 WARRANTY PROCEDURES.

This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support Services Group for information.

5.3 TROUBLESHOOTING PROCEDURES.

Diagnostic testing software is included with the AM-210 circuit board and should be used for troubleshooting and to verify proper operation. The diagnostic tests check all aspects of the AM-210 Floppy Disk Controller circuit board. When this diagnostic is successfully performed with a disk drive that is known to be good, all aspects of the AM-210 circuit board can be qualified as operational. Diagnostic operating procedures and a description of the tests are contained in the following paragraphs.

5.3.1 OPERATIONAL TEST.

The following procedure can be performed as an overall operational test. If successfully performed with a known good disk drive, the circuit board can be considered fully operational.

1. FORMAT a new floppy diskette.

2. Perform a SYSACT to initialize.

3. Perform a COPY from another diskette in the other drive.

4. When the copy is complete with no errors, type DSKANA for the new diskette and verify no errors.

This test, with the full diagnostic tests, checks all major portions of the AM-210 circuit board except the output register connecting the available input signals to the floppy drive.

5.3.2 DIAGNOSTIC PROCEDURES.

This diagnostic test contains five separate sections. The first two diagnostics do not require any floppy drives connected to the AM-210. The five sections are called:

A. DDTST - Initial register check.
B. 1791T - FDC chip test.
C. SEEK - Floppy drive seek test and data separator calibration.
D. FTST - Floppy interface drive test.
E. EVAL - Final system evaluation procedures.

To begin this diagnostic, locate the major portion of the diagnostic called AM-210.RUN. LOG into that particular PPN and type the following:

RUN AM210

To do this correctly you will have to verify that the SYSTEM.INI file allows for loading into system memory BASIC.PRG and RUN.PRG. Accomplish this by using VUE and altering the SYSTEM.INI file. Consult the USER'S MANUAL before attempting this.

Because of the large size of this diagnostic, it is composed of five CHAIN files which minimize the necessary amount of memory. You may load any singular file in by typing RUN followed by any one of the following names:

DDTST
1791T
SEEK
FTST

The five separate files are described here in detail as to their purpose and typical error messages. Consult the particular file of interest by comparing the title block to the file name described earlier.

5.3.2.1 INITIAL REGISTER CHECK (DDTST).
Refer to the circuit board block diagram shown on sheet 2 of the schematic diagram located in Section 6 of this manual.

The system blocks are:

1. I/O Address Compare
2. Command Generator
3. Data-In Port
4. Data-Out Port
5. 1K On-Board RAM
6. RAM Address Counter

This routine writes three different data patterns to the on-board RAM. Each pattern is read back and checked for errors. If any occur, the actual data will be listed as well as the RAM location and the expected pattern. The three patterns written are 0, 85, 170 DECIMAL. Note that in binary code, these patterns are as shown below:

0	0 0 0 0 0 0 0 0
170	1 0 1 0 1 0 1 0
85	0 1 0 1 0 1 0 1

This allows for testing adjacent data lines for shorts as well as each data line for a supply short (+5 or ground).

If an error should occur, the CRT responds with all necessary error information. A sample error printout would be the following:

ERROR AT LOCATION 1009 WAS 171 EXPECTED 170

This example shows the possible shorting between data lines 0 and 1.

The second portion of this test writes a unique data pattern into each RAM cell. The data pattern is the actual address (or multiple thereof) of the RAM cell selected. Thus, for the first 255 RAM cells, the data pattern is 0 through 255. Some examples are given below:

Address	Data Pattern
0	0
17	17
1	1
256	0

Note that each data pattern is unique up to 255. At this point, the data pattern returns to zero. A binary representation of the pattern will clarify its correlation to the unique RAM address.

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
512	256	128	64	32	16	8	4	2	1	
		0	0	0	0	0	0	0	0	ADDR 0
	1	0	0	0	0	0	0	0	0	ADDR 256
1	0	0	0	0	0	0	0	0	0	ADDR 512

In all three cases the address lines A0 - A7 are all 0. Because the data bus is only 8 lines wide, the maximum number is 2^8 or 255. Thus at 256, the data pattern returns to 0. Because on-board RAM is 1024 deep, each data pattern is essentially written in four cells. As in the above described error printout, the error is listed as the actual data and the RAM cell in which the error occurred.

5.3.2.2 FLOPPY CONTROLLER CHIP TEST (1791T).
This routine checks three of the FDC registers and verifies that data can be read from and written into each one. It writes data patterns from 0 to 255. Each data pattern is individually checked against the expected results and a tabulation of the errors is stored and later printed out.

This routine tests the track, sector, and data registers. The status register and the command register can only be tested during functional operations. For a pattern read, the printout reads the following:

```
TRACK    DATA   PATTERN   OF   15   NO   ERRORS
SECTOR   DATA   PATTERN   OF   15   NO   ERRORS
DREQ     DATA   PATTERN   OF   15   NO   ERRORS
                                         PASS #15 COMPLETE
```

If an error occurs, the printout appears as:

```
TRACK    WAS    255    EXPECTED    15
SECTOR   DATA   PATTERN   OF   15   NO   ERRORS
DREQ     DATA   PATTERN   OF   15   NO   ERRORS
                                         PASS #15 COMPLETE
```

The total errors accumulated at the end of the test for each register appear as the example below shows:

```
TRACK    ERRORS   TOTALLED   12
SECTOR   ERRORS   TOTALLED   2
DREQ     ERRORS   TOTALLED   0
```

This test also diagnoses any data line faults that may not have been discovered during the running of the initial register check (DDTEST).

The user of this diagnostic should also use this portion to verify that the oscillator circuit and the 4 bit counter (clock divider) are checked for errors. This can be accomplished by attaching a scope probe to U9 and checking the following pins for the indicated pulse periods:

U9-1	16 Mhz	- 0.0625	µSec
U9-3	8 Mhz	- 0.125	µSec
U9-4	4 Mhz	- 0.25	µSec
U9-5	2 Mhz	- 0.5	µSec
U9-6	1 Mhz	- 1	µSec

If no pulses are occurring, probe U10-8 for a 16 Mhz pulse. Also, check U10-7 for ground and U10-14 for +5 volts.

5.3.2.3 FLOPPY DRIVE SEEK TEST AND DATA SEPARATOR CALIBRATION (SEEK).

This routine is used as an aid to checking and calibrating the data-clock separator circuit. This test checks all of the following system blocks:

1. FDC chip - partial check on floppy drive interface lines.

2. External control register No. 1 - partial check on drive select signals and double density state signal.

3. External status register - partial check on status signals.

4. Data separator circuit - calibration and check routine.

5. Step pulse O/S and head load O/S check routine. Allows for checking one-shot (O/S) pulse widths for these two signals going to the floppy drive.

NOTE:

This test should not be run until the prior two routines (DDTEST, 1791T) are passing with no indicated errors.

The initial selection of this routine will ask the user if double density diskettes are installed. It is important that this question be answered correctly. This does allow the user to optionally select double density diskettes for the all important data separator calibration.

For the first run-through for this test, it is recommended that a single density diskette be used for calibration purposes. Select the restore function and verify that the selected drive is at TRACK 0. This should be tested in the following three ways:

1. Physically inspect the drive selected and note that the head mechanism is positioned at TRACK 0 (outermost portion of the floppy diskette).

2. Scope U1-34 and verify that it is low.

3. Read the information indicated on the CRT screen and note the status read. It should read:

STATUS IS 4
TRACK IS 0
SECTOR IS 0

This proves the Track and Sector registers of the FDC chip have been initialized to 0. The status indicates that TRACK 0 has been detected. For any other status values received, refer to paragraph 4.2.1.

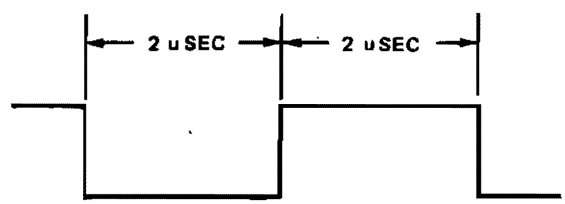
If no head motion has occurred, check the drive select lines as well as the step rate one-shot (U14). This output should be high for about 10 usec. for every step pulse delivered. The restore routine by the FDC chip is handled by sending step commands in the outward direction (U1-16 should be low) until TRACK 0 is detected. No head loading occurs in a restore function for this diagnostic.

Select the same drive again and do a Restore and Seek function (#2). The CRT prints out after the Restore function is complete with a Step Rate Selection (3, 6, 10, 15 usec). This can be varied for the appropriate drive selected. For Wangco's, use 10; for Shugart's or compatible version, use 6 or 3. Note that this diagnostic will not function on a PERSCI or a mini-floppy since the step rates involved are not capable of being selected.

Connect a scope probe of channel one to the pad labeled RCLK near U1. This can also be connected via U12, pin 5. This pulse period should be approximately 4 usec. (The pulse width is approximately 2 usec.).

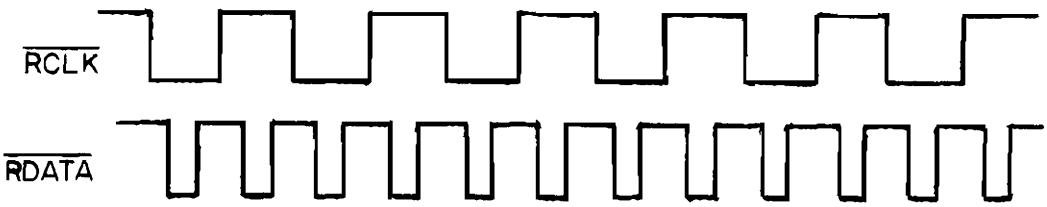
Use channel 1 as the trigger source and sync the scope on the normal mode with this signal. Take the channel two probe and check U2-2. This point should be approximately a 2 volt signal. The output (U2-6) should be pulsing at about a 4 Mhz rate. Connect the channel two probe to U3-6 with a dip clip. This is the RDATA signal from the floppy drive. If no drive is selected or enabled, this line will be typically high (+5 volts).

Select the appropriate step rate from the CRT screen and press return. Using a non-metalized trim pot adjusting tool, adjust R38 until the RCLK signal is approximately 4 uSec. (Select pulse width for 2 uSec). See figure below:



When the trim pot is correctly adjusted, the floppy responds by printing out a status of 32 for each track selected. Any other status (typical errors show a status of 48) is a non-functional setup.

When the board is properly adjusted, the RCLK signal and the RDATA signal appear locked up in a pattern illustrated below:



Note that RCLK will "shift" depending on the similar shift in RDATA. However, the entire trace is effectively stable when the PLO circuitry is adjusted correctly.

This calibration should be checked further by installing a double density diskette. All factors are similar except that RCLK time is now halved; each pulse width is 1 uSec in duration for a 2 uSec pulse period.

The Head Load O/S should also be checked for proper timing. Connect channel one to U14-12 and set for a negative-going pulse duration for 5 mSec per division. Each time the drive is initially selected and the head is to be loaded, this output should go low for approximately 40 mSec. This is defined for -01, -02, -04, -05 revision level boards only.

Complete this routine by installing either two single or two double density diskettes in a dual drive system and selecting option #3 (Automatic Test). This tests two consecutive drives starting at the drive select number requested. For example a dual Wangco system would typically be drive 0 and drive 1. A dual Shugart system would be drive 1 and drive 2 (there are

four separate drive lines for selecting any drive). The Wangco system uses a binary representation of these lines for drive selection. Thus, the first drive is drive 0 and is a binary zero; drive one is the second drive and is a binary 0001. Shugart systems use a different scheme. Each drive is selected by putting a "one" on each individual line. Thus, the first drive is drive one and selected by sending a binary 0001. The second drive is two and is selected by sending a binary 0010. To keep a consistency between this radial selection technique and the binary selection, this system allows for using both. For physical drive numbers and actual numbers, a list is illustrated below:

DRIVE	WANGCO	SHUGART
0	0 (0000)	1 (0001)
1	1 (0001)	2 (0010)
2	2 (0010)	4 (0100)
3	3 (0011)	8 (1000)

The step routine for dual drives (#3) can be selected for as many passes as desired. At the end of the passes, the total number of errors for each drive are totalled and listed. (This is essentially done by checking each step position for a status of 32 and then recording the number of passes that showed a status other than 32.) These total errors are accumulated at the end of the selected number of passes.

5.3.2.4 FLOPPY INTERFACE DRIVE TEST (FTST).
This routine checks the following system blocks:

1. DRQ processor
2. Command generator/data ports
3. FDC chip
4. External control register No. 1
5. External status register

6. External control register No. 2
7. Data separator
8. Write pre-compensation circuitry
9. On-board RAM and associated logic

The complete passing of this diagnostic will be a strong indication of satisfactory operation of the AM-210 circuit board.

It will essentially check all system block functions except the PRDY control logic and the bootstrap logic. A command list allows for each individual function to be tested individually and checked for errors. It checks all interface lines between the AM-210 and a Shugart standard floppy drive.

The command list for this portion of the diagnostic appears as the following:

SET VALUES
SEEK ONLY
GET STATUS
RESTORE
READ SECTOR
PRINT ON-BOARD RAM
FILL RAM
WRITE SECTOR
RETURN TO MAIN MENU

These commands allow for specific functions to occur to/from the AM-210 and the floppy drive. After each function has been completed, the diagnostic returns once again to this command list to begin the next desired activity. At any time, the user may type a 9, and with the carriage return key depressed, can return to the main program to select one of the other linked routines. In order to properly run this routine, the user must first "set values" of the drive. This routine asks the following questions which can be answered optionally by the user.

Input Drive Number?_____

Select a drive to be tested; i.e., 1.

Select Side (0,1)?_____

Normal selection will be side 0. For double-sided diskettes, the user may select side 0 or 1. (Note: Wangco's do not allow for double-sided diskettes.)

Step Time (3, 6, 10, 15 ms)?_____

Refer to Section 5.3.4 of this manual for a detailed explanation of selecting step time. Wangco typically should be set for 10. Shugart and similar drives are usually set for 6.

Double Density Mode (Y,N)?_____

For double density diskettes, type a "Y" for yes. Standard diskettes type an "N" for no.

Load Heads (Y,N)?_____

This selects whether the heads are to be loaded during the seek operations. To verify the position via the track address mark on the diskette, select yes. (Most cases should always select a Yes for this routine.)

AM-210 Board Number (0, 1, 2)?_____

Normal operation selects board 0. For systems in which more than one AM-210 is installed, use the appropriate Board Number for checking the appropriate floppy drive.

The following functions can be performed by the indicated procedure:

1. Restore the Selected Drive (3)

   This issues the command for the selected drive to step outwards until the track 0 indicator (LED) is enabled. The system responds by typing the status of the drive on the CRT. A status of 4 indicates that the drive is restored correctly. A status of 128 is an error and indicates the drive was not ready. The status lines are illustrated in paragraph 4.2.1.

2. Seek to Desired Track, Sector (2)

   Any one of the 77 tracks, 26 sectors can be selected and the drive will seek to the desired position. After entering the seek routine (2), the CRT queries the track and sector number. The track number can be any number from 0 to 76. The CRT next asks for the sector number. The user may select from 1 to 26. The system then seeks to this desired position and verifies the correct location by checking the address mark on the diskette. A status is printed out on the screen. A #32 status is no errors; a status of #48 is typically an error. Note that a seek routine, as well as a restore are both considered TYPE I Commands for the FDC chip.

3. Read a Sector (5)

   The user must first seek to the desired location to be read, by doing the Seek Only (2) routine as described previously. By entering the Read Sector (3) command, the system reads the data as located at the track and sector register prescribed. The CRT indicates the status of the READ command as well as the track and sector register it is reading from.

Note that a status of 0 is no errors. All other status indications can be found in paragraph 4.2.1. Note also, that Read, Write Sectors are considered TYPE II Commands and the status register information must be checked for a TYPE II routine.

For single density, the read sector transfers 128 bytes of data into the on-board RAM. This can be viewed for comparison by selecting the Print on-Board RAM routine.

4. Write Sector (8)

By seeking (2) to a desired sector and track, the user can transfer any data desired to the prescribed location. In single density, this is 128 bytes of data and is chosen as the first 128 bytes of on-board RAM. The system prints out the actual location and the status of the Write command. Note that the data pattern indicated illustrates the last data pattern selected to be written into the on-board RAM. Thus, this register is not updated until another data pattern is chosen for RAM.

A status of 0 indicates no errors. The actual meaning for each status bit is defined in paragraph 4.2.1.

5. Print on Board RAM (6)

This routine allows the user to examine up to 1024 bytes of data of the on-board RAM. The user may select "how much" RAM to be viewed. The system then prints in decimal each byte of data discovered. This is a convenient addition to Reading a Sector (5) in that the data transferred to RAM from the floppy can be inspected.

6. Fill RAM (7)

The user may select any decimal value from 0 to 255 to be stored in the on-board RAM. Up to 1024 addressed cells can be written into. This routine conveniently allows the user to fill on-board RAM with a desired data pattern and then Write it out to a desired sector, track location. By clearing RAM to zeros (fill RAM with 0), the user may read the sector track previously written into, and then print RAM (6) to verify that the data transfer has actually occurred.

The filling of RAM can only be a continuous routine and it must start at address 0. Thus the user cannot choose to fill RAM with 200 from 100 to 200, but will rather fill RAM with 200 from 0 to 200. The entire purpose behind the on-board RAM is for temporary storage of data records to/from the floppy drive.

5.3.2.5 EVALUATION PROCEDURE.

In order to finalize all aspects of the AM-210, it is necessary to perform system command routines which exercise all portions of the AM-210. In addition, this procedure is the ONLY method to easily investigate the following system blocks for their functionality:

1. Bootstrap Logic
2. PRDY Control Logic

The CRT screen produces a procedural list which should be followed in order to test the system blocks as indicated. This routine is concerned largely with the data transfer that occurs during a format procedure. In this routine, all data is transferred from system memory to the data register of the FDC chip via a block move command. The on-board RAM is not utilized for

this method. The actual data transfer timing is governed by the Data Request signal and the Write Track command. See section 3.4 for diskette formatting.

The boot routine logic is easily tested by installing the necessary boot PROM and jumpering the AM-210 for the "BOOT ROUTINE." It is recommended that a known good PROM be used to test the rest of the circuitry.

SECTION 6

SCHEMATIC AND PARTS LIST

Table 6-1. Component Cross-reference List

REF DESIG.	MFG. TYPE	PARAGRAPH NO. OF DESCRIPTION	REF DESIG.	MFG. TYPE	PARAGRAPH NO. OF DESCRIPTION
U1	FD1791	4.2.1	U25	8131	4.2.6
U2	LS324	4.2.17	U26	8131	4.2.6
U6	LDM250	4.2.20	U29	LS138	4.2.12
U6	LDM500	4.2.20	U30	2114	4.2.2
U8	74LS113	4.2.10	U31	2114	4.2.2
U9	LS393	4.2.19	U33	LS240	4.2.14
U12,16	LS74	4.2.7	U34	LS273	4.2.22
U13	7445	4.2.4	U35	LS273	4.2.22
U14	26LS123	4.2.11	U36	81LS97	4.2.8
U16	8097	4.2.5	U39	81LS98	4.2.9
U17	LS151	4.2.13	U40	LS240	
U18	26LS123	4.2.11	U41	LS244	4.2.15
U19	LS288	4.2.21	U43	LS374	4.2.18
U20	LS393	4.2.19			
U21	2708	4.2.3			
U23	LS293	4.2.16			

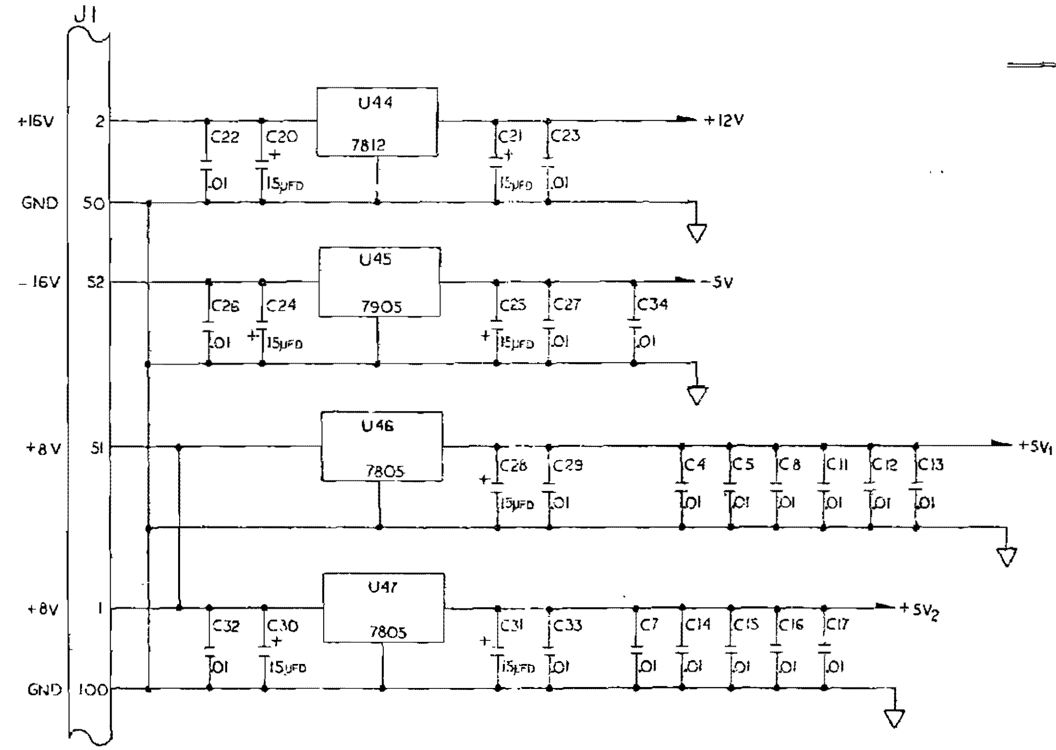
FBILL # DWB-00210-05

REV.F03

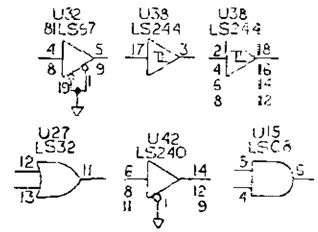
11 AUG,1980

DESCRIPTION ASSY,DISK CONT DBL DEN-CDC 9406-3:

	PART NUMBER	DESCRIPTION	QTY
1	DWF-00210-00	PCB DOUBLE DENSITY FLOPPY AM-210	1
2	DWB-00211-01	ASSY ROM AM-210	1
3	IC1-74393-01	IC DUAL 4 BIT BINARY COUNTER	2
4	ICS-01791-00	IC DOUBLE DENSITY FLOPPY DISK CONT	1
5		*** DELETED PART ***	0
6	IC1-74151-01	IC 8 INPUT MULTIPLEXER	1
7	IC1-74293-01	IC 4 BIT BINARY COUNTER	1
8	IC1-07445-00	IC BCD DECIMAL DECODER	1
9	IC1-74624-01	IC VOLTAGE CONTROLLED OSCILLATOR	1
10	TRP-03906-00	TRANSISTOR PNP	1
11	TRN-03904-00	TRANSISTOR NPN	1
12	RSV-00104-00	RESISTOR TRIM POT MULTITURN 100K	1
13	ICS-00002-00	IC OSCILLATOR 16MHZ	1
14	ICL-00301-00	IC AMPLIFIER OPERATIONAL	1
15	CNS-00014-00	SOCKET 14 PIN DIP	17
16	CNS-00016-00	SOCKET 16 PIN DIP	8
17	CNS-00018-00	SOCKET 18 PIN DIP	2
18	CNS-00020-00	SOCKET 20 PIN DIP	12
19	CNS-00024-00	SOCKET 24 PIN DIP	1
20	CNS-00040-00	SOCKET 40 PIN DIP	1
21	IC1-07400-01	IC QUAD 2 INPUT NAND GATE	2
22	IC1-07402-01	IC QUAD 2 INPUT NOR GATE	2
23	IC1-07408-01	IC QUAD 2 INPUT AND GATE	2
24	IC1-07416-00	IC HEX INVERTER /DRIVER OC	2
25	IC1-07432-01	IC QUAD 2 INPUT OR GATE	1
26	IC1-08131-00	IC COMPARATOR 6 BIT	2
27	IC1-08197-01	IC BUFFER OCTAL	2
28	IC1-08198-01	IC INVERTER OCTAL	1
29	IC1-26123-00	IC DUAL ONE SHOT	2
30	IC1-74113-01	IC DUAL J-K FLIPFLOP	1
31	IC1-74138-01	IC DECODER 3 TO 8 LINE	1
32	IC1-07474-01	IC DUAL D FLIPFLOP	2
33	IC1-74240-01	IC OCTAL BUS DRIVER INVERTING	4
34	IC1-74244-01	IC OCTAL BUS DRIVER NONINVERT	2
35	IC1-74273-01	IC OCTAL D REGISTER W/RESET	2
36		*** DELETED PART ***	0
37	IC1-74374-01	IC OCTAL D FLIPFLOP	1



SPARES



TABULATION BLOCK

DASH	DESCRIPTION
-01	PERSCI - 277
-02	WANGCO/SHUGART
-03	SHUGART 5" DR.
-04	PERSCI - 270
-05	CDC 9406-3

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	E01	REVISED PER ENG[illegible]		
	E01	[illegible]		
	F00	REVISED PER ENG0220		
	F01	REVISED PER ENG0263		

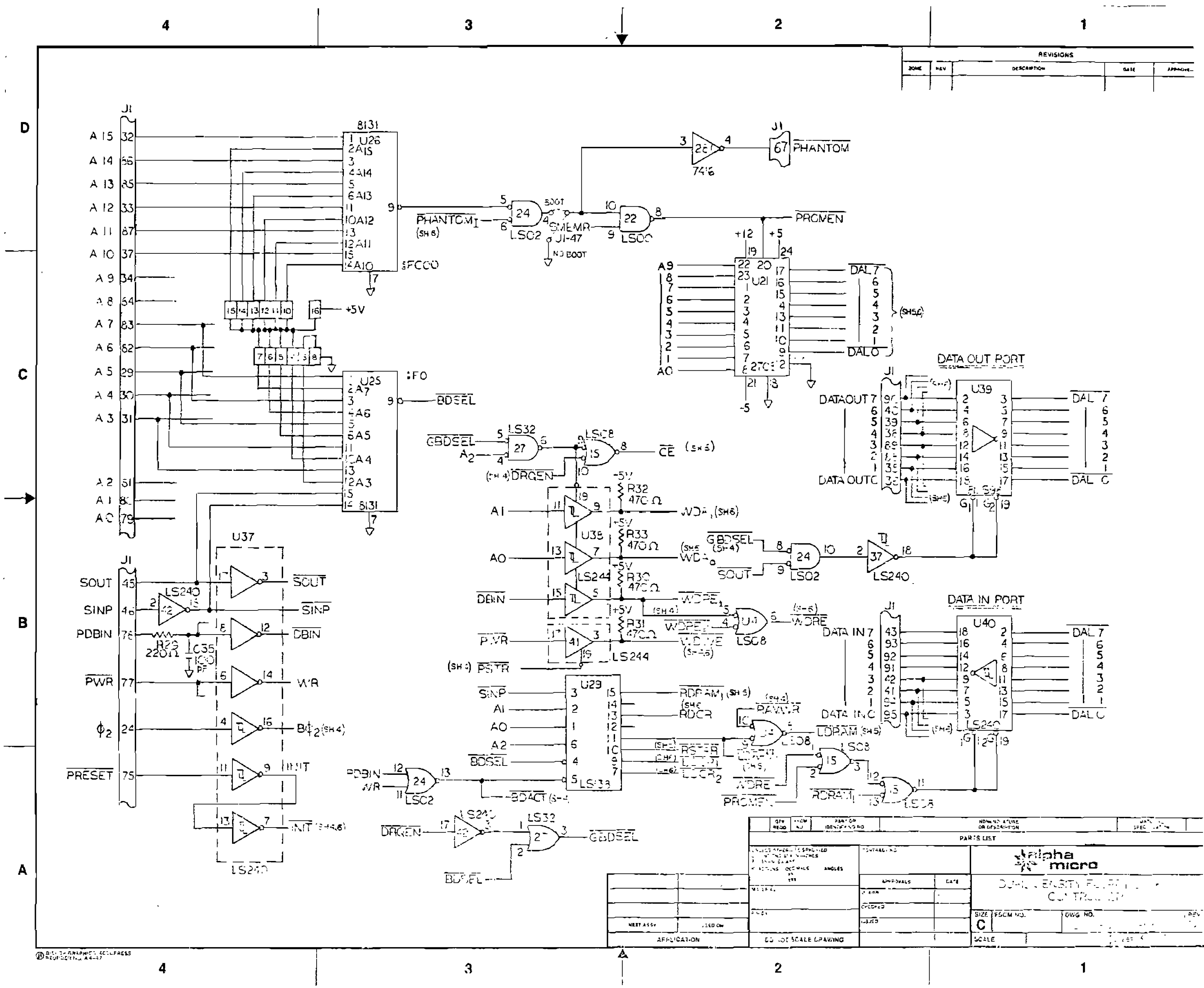
PARTS LIST

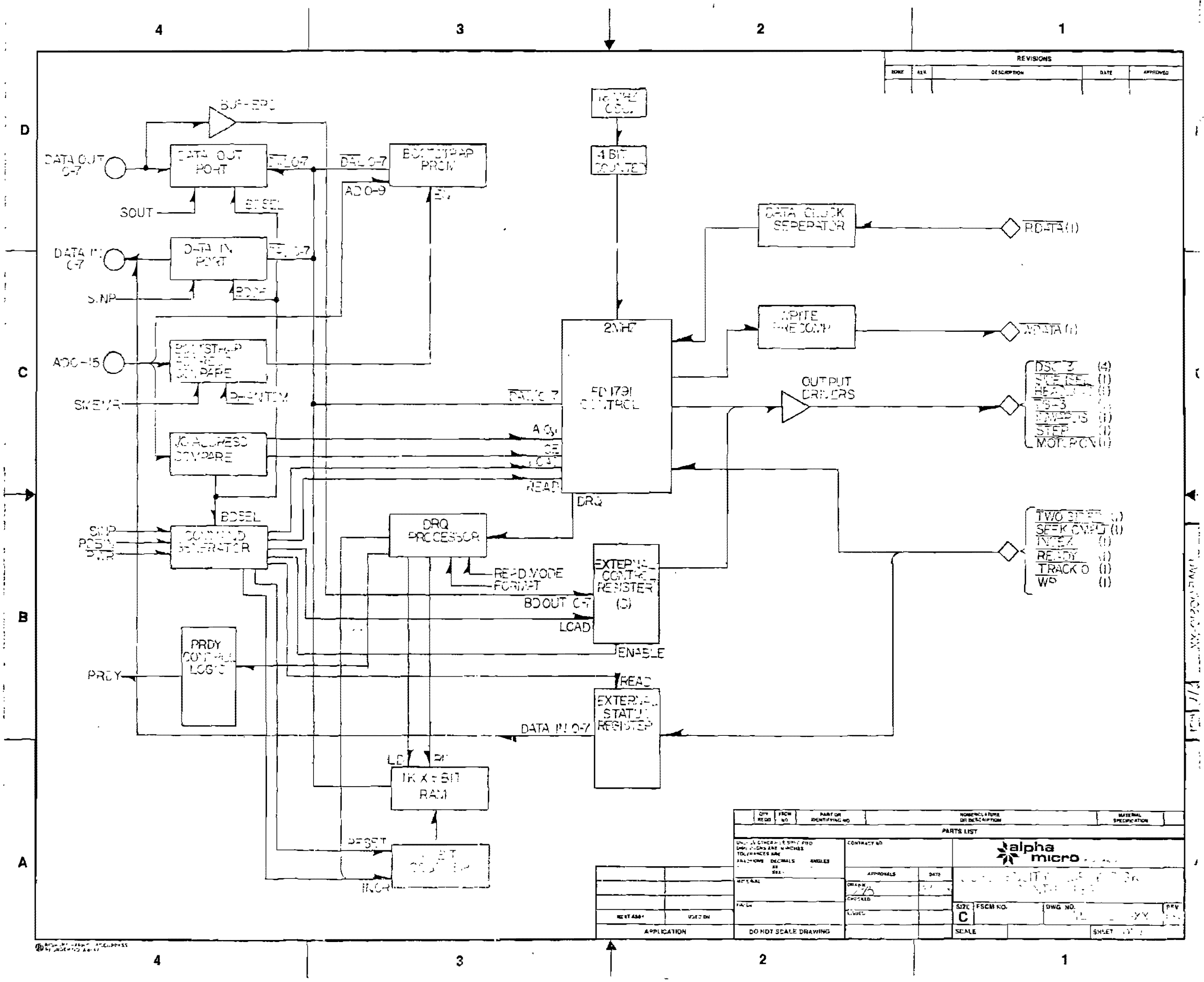
alpha micro

DUAL DENSITY FLOPPY DISK CONTROLLER

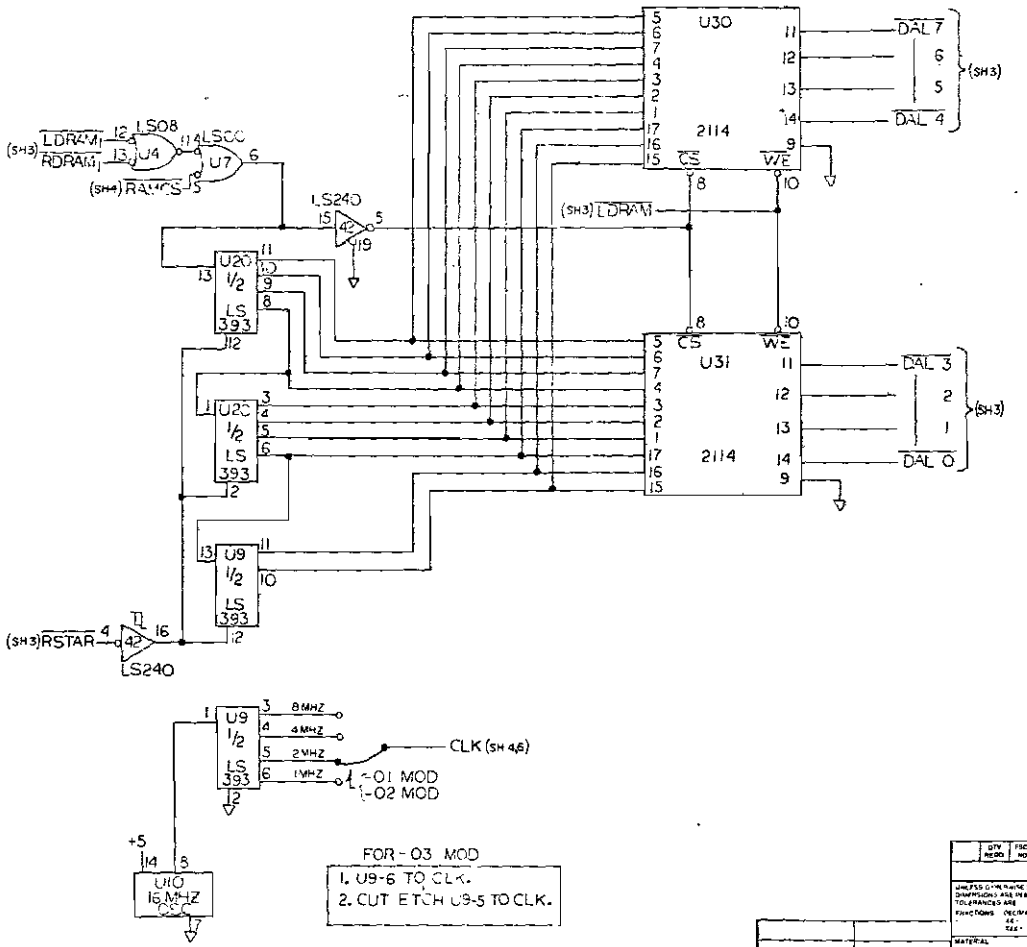
SIZE C

DO NOT SCALE DRAWING


REVISIONS
J1
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
8131
U26
SFC00
U25
FF0
BDSEL
PHANTOM
LS02
BOOT
SMEMR
J1-47
NO BOOT
LS00
74I6
PROMEN
U21
2708
DAL 7
DAL 0
DATA OUT PORT
U39
DATAOUT 7
DATA OUT 0
LS244
GBDSEL
LS32
DRGEN
LS08
CE
R32 470Ω
R33 470Ω
R30 470Ω
R31 470Ω
WDA
U35
LS244
DBIN
WDPE
WDRE
PWR
WRITE
PSTR
U37
SOUT
SINP
PDBIN
R29 220Ω
C35 100 PF
WR
Bϕ2
PRESET
INIT
LS240
U29
RDRAM
RDCR
LDRAM
RSTER
PRAWR
BDACT
LS138
DATA IN PORT
U40
DATA IN 7
DATA IN 0
PARTS LIST
alpha micro
SIZE C
DWG NO.
SCALE
DO NOT SCALE DRAWING
APPLICATION
NEXT ASSY
USED ON



4
3
2
1
D
C
B
A
REVISIONS
DATA OUT 0-7
DATA OUT PORT
SOUT
BD SEL
DATA IN 0-7
DATA IN PORT
SINP
AD 0-9
EN
BOOTSTRAP PROM
A0-15
SMEMR
PHANTOM
I/O ADDRESS COMPARE
BDSEL
SINP
PDBIN
PWR
CONTROL GENERATOR
4 BIT COUNTER
2MHZ
FD1791 CONTROL
CE
READ
DRQ
DRQ PROCESSOR
READ MODE
FORMAT
BD OUT 0-7
LOAD
ENABLE
EXTERNAL CONTROL REGISTER (8)
READ
EXTERNAL STATUS REGISTER
DATA IN 0-7
PRDY
PRDY CONTROL LOGIC
1K X 8 BIT RAM
RESET
INCR
DATA CLOCK SEPERATOR
WRITE PRECOMP
OUTPUT DRIVERS
STEP
MOTOR ON
TWO SIDED
SEEK CMPLT
INDEX
READY
TRACK 0
WP
PARTS LIST
alpha micro
APPLICATION
DO NOT SCALE DRAWING
SIZE C
SCALE
SHEET



REVISIONS

ZONE	REV	DESCRIPTION	DATE	APP'D

PARTS LIST

QTY REQD	FSCM NO	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO.

	APPROVALS	DATE
MATERIAL	DRAWN	
FINISH	CHECKED	
NEXT ASSY	ISSUED	
USED ON		

APPLICATION

DO NOT SCALE DRAWING

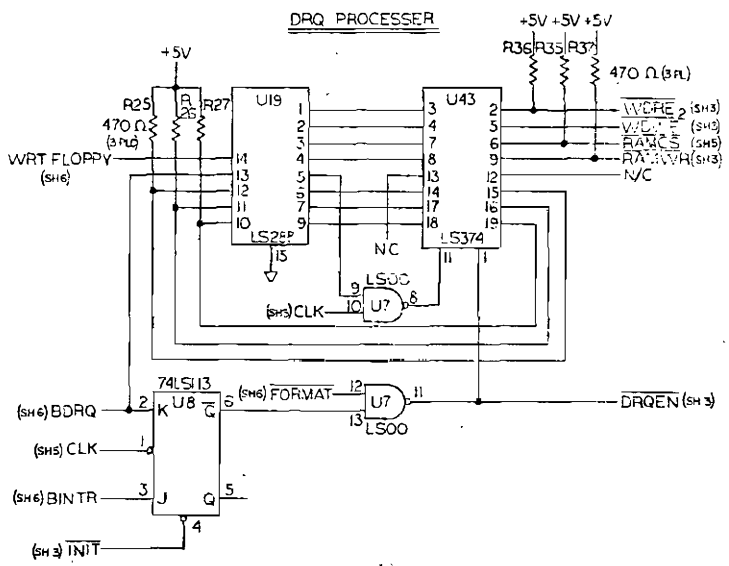
alpha micro

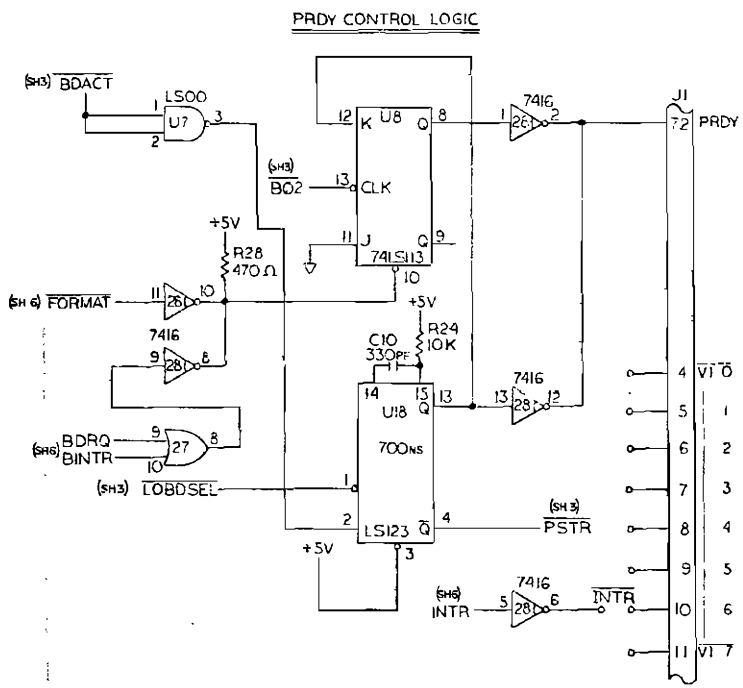
DUAL DENSITY FLOPPY DISK CONTROLLER

SIZE	FSCM NO.	DWG NO.	REV.
C		[illegible]-0210-XX	[illegible]

SCALE —

SHEET 5 OF [illegible]





REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

QTY PER DO	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX

CONTRACT NO

	APPROVALS	DATE
MATERIAL	DRAWN	
FINISH	CHECKED	
NEXT ASSY USED ON	ISSUED	

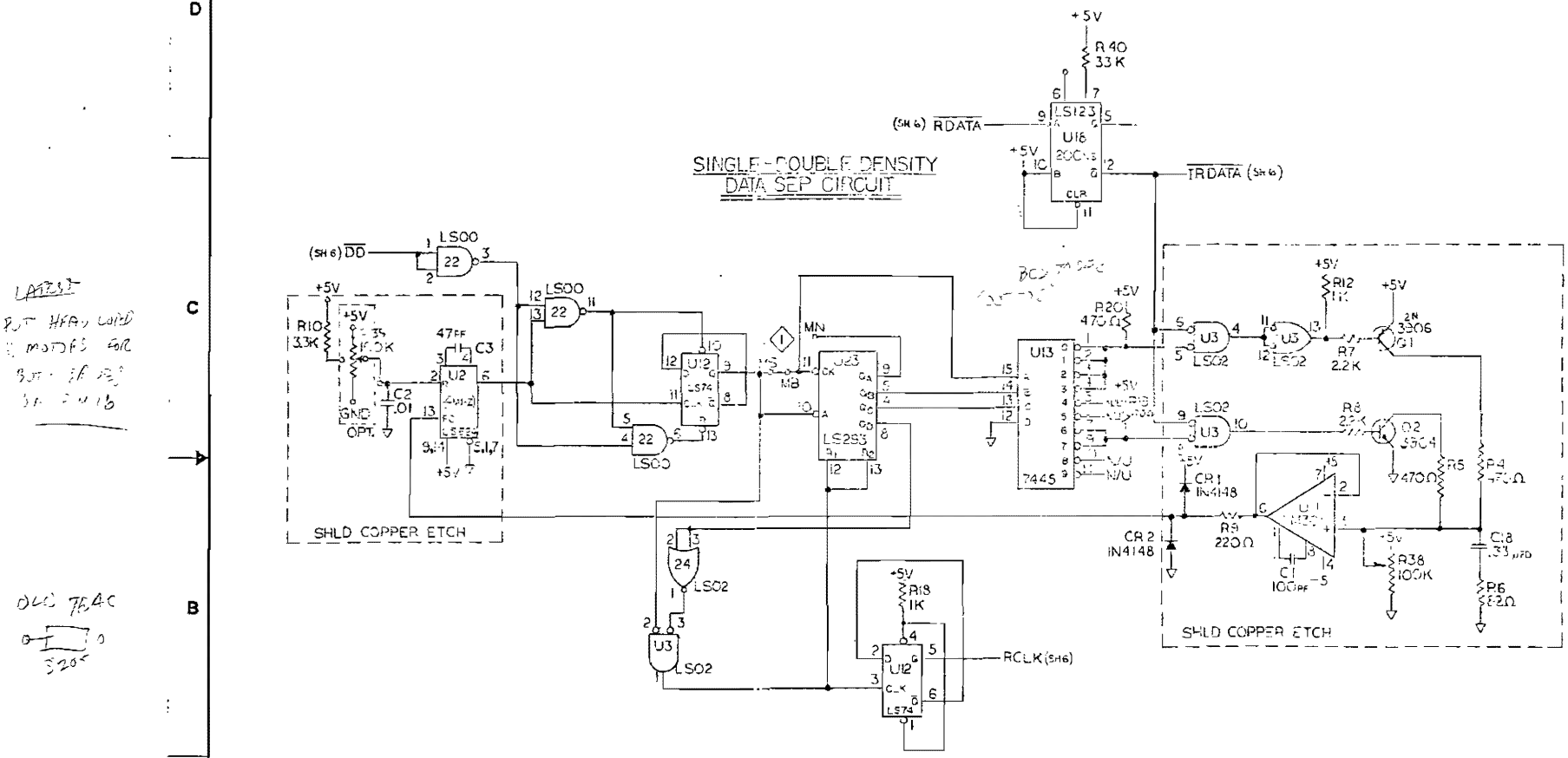
APPLICATION DO NOT SCALE DRAWING

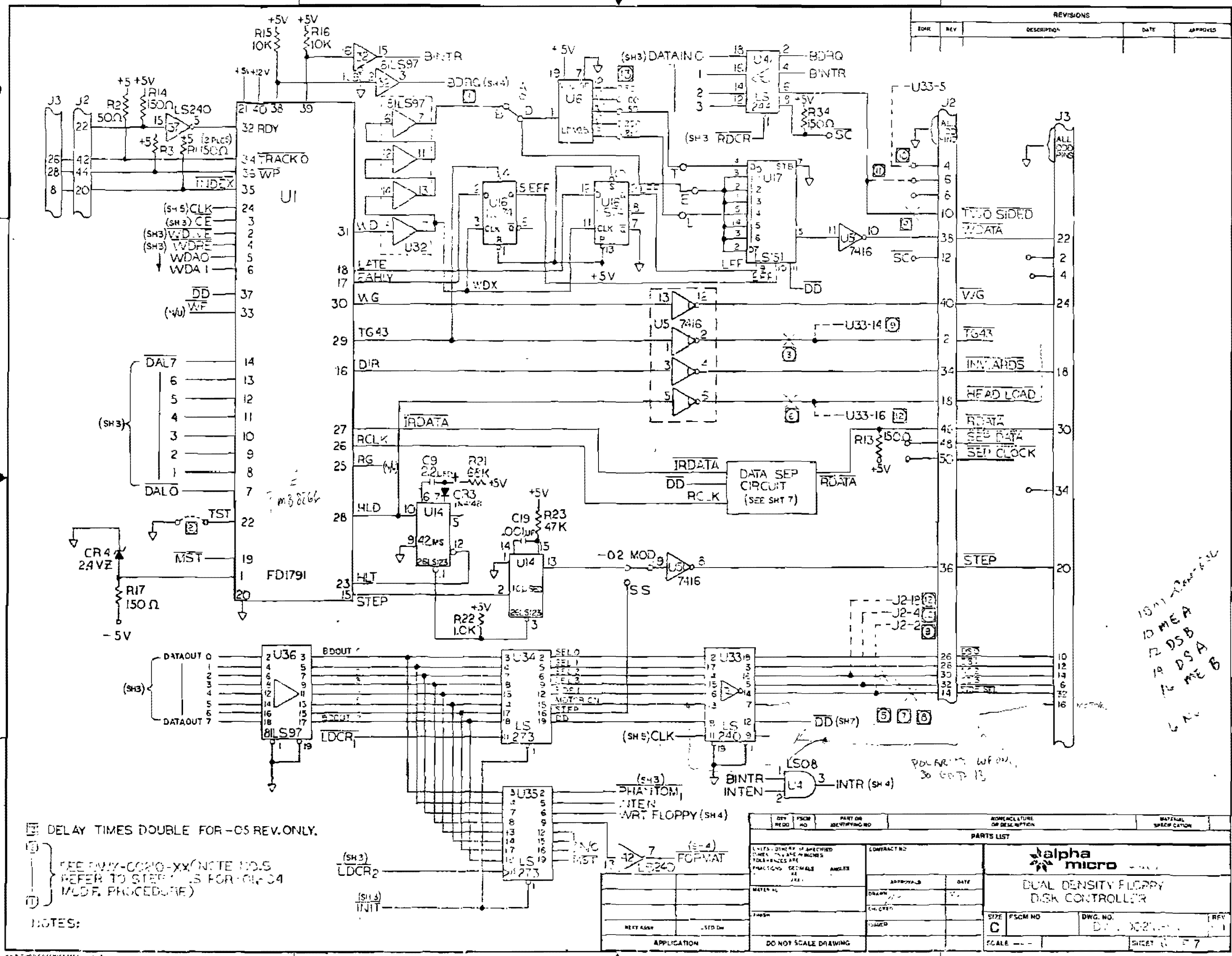
alpha micro

DUAL DENSITY FLOPPY DISK CONTROLLER

SIZE C | FSCM NO. | DWG. NO. [illegible] | REV

SCALE —— SHEET [illegible]


SINGLE - DOUBLE DENSITY
DATA SEP CIRCUIT
+5V
R40
33K
(SH 6) RDATA
LS123
U16
RDATA (SH 6)
CLR
(SH 6) DD
LS00
R10
33K
10K
47PF
C3
C2
.01
U2
GND
OPT.
SHLD COPPER ETCH
MN
MB
U23
LS293
U13
7445
R20
470Ω
U3
LS02
2N
3906
Q1
R7
2.2K
R12
1K
R8
2.2K
Q2
3904
R5
470Ω
R4
470Ω
CR1
IN4148
CR2
IN4148
R9
220Ω
U1
LM339
C1
100PF
R38
100K
C18
.33 MFD
R6
82Ω
SHLD COPPER ETCH
R18
1K
U12
LS74
RCLK(SH6)
FOR 03MOD: REMOVE MB TO MN JUMPER.
INSTALL MN TO MB JUMPER.
NOTES:
Alpha micro
APPLICATION
DO NOT SCALE DRAWING
SCALE
SIZE C



U1
FD1791
32 RDY
TRACK 0
WP
INDEX
CLK
CE
WDAO
WDA 1
DD
WF
DAL7
DALO
TST
MST
CR4
24VZ
R17
150 Ω
-5V
LATE
EARLY
WDX
WG
TG43
DIR
IRDATA
RCLK
RG
HLD
HLT
STEP
BINTR
BDRQ
DATA SEP CIRCUIT (SEE SHT 7)
RDATA
TWO SIDED
WDATA
IN/WARDS
HEAD LOAD
SEP DATA
SEP CLOCK
-02 MOD
S S
DATAOUT 0
DATAOUT 7
BDOUT
LDCR1
LDCR2
PHANTOM
INTEN
WRT FLOPPY (SH4)
FORMAT
INIT
INTR (SH 4)
DELAY TIMES DOUBLE FOR -05 REV. ONLY.
NOTES:
REVISIONS
PARTS LIST
alpha micro
DUAL DENSITY FLOPPY DISK CONTROLLER
DO NOT SCALE DRAWING
APPLICATION

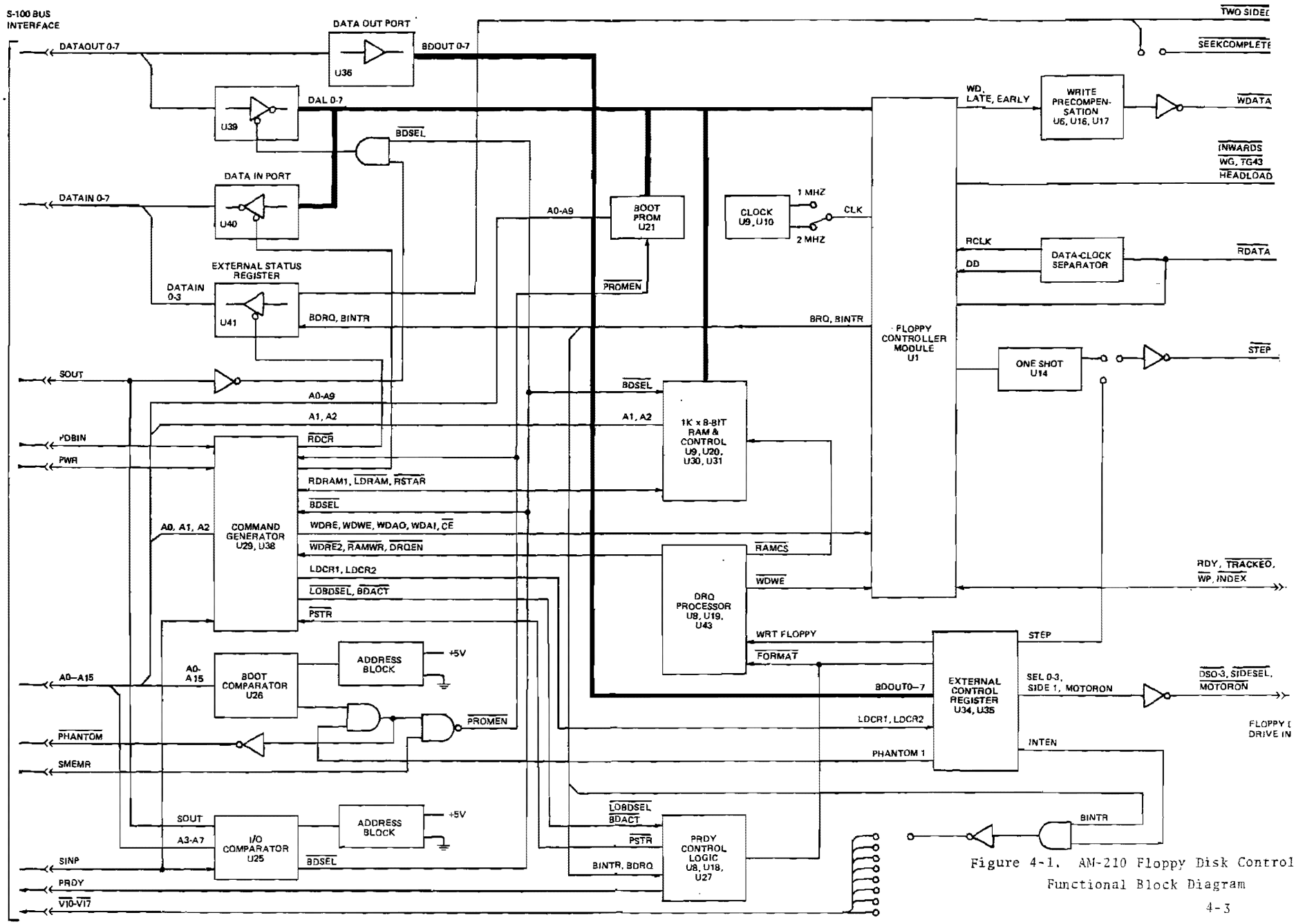


Figure 4-1. AM-210 Floppy Disk Control Functional Block Diagram

BILL # DWB-00210-05 REV.F03 DESCRIPTION ASSY,DISK CONT DBL DEN-CDC 9406-3:

	PART NUMBER	DESCRIPTION	QTY
38	ICM-02114-04	RAM 1K X 4 BIT STATIC	2
39	ICL-07805-00	IC REGULATOR + 5V	2
40		*** DELETED PART ***	0
41	ICL-07812-00	IC REGULATOR +12V	1
42	ICL-07905-00	IC REGULATOR - 5V	1
43	HDM-00007-00	HEAT SINK .750WI .375HT .750LG	2
44	HDS-00632-01	SCREW 6-32 X .250	3
45	HDN-00632-01	NUT HEX 6-32 STL SM PATTERN	3
46	HDW-00632-01	WASHER LOCK 6-32	3
47	HDS-00632-03	SCREW 6-32 X .750 NYL	1
48	HDN-00632-02	NUT HEX 6-32 NYL SM PATTERN	1
49	HDM-00004-00	MICA PAD TO 220	1
50	CNF-00002-11	HEADER 50 PIN W/O EJC RT ANGLE	1
51	CNF-00006-01	HEADER 26 PIN W/O EJC RT ANGLE	0
52	CPN-00470-01	CAPACITOR 47 PF	1
53	CPN-00101-01	CAPACITOR 100 PF	2
54	CPN-00102-01	CAPACITOR 1000 PF	1
55	CPN-00103-01	CAPACITOR .01 UF	20
56	CPN-00334-01	CAPACITOR 33 UF 50V	1
57	DIO-04148-00	DIODE SIGNAL 1N4148	3
58	RS2-00102-00	RESISTOR 1 K 1/4W 5% CAR	3
59	RS2-00103-00	RESISTOR 10 K 1/4W 5% CAR	3
60	RS2-00151-00	RESISTOR 150 OHM 1/4W 5% CAR	7
61		*** DELETED PART ***	0
62	RS2-00332-00	RESISTOR 3.3 K 1/4W 5% CAR	1
63	RS2-00221-00	RESISTOR 220 OHM 1/4W 5% CAR	2
64	RS2-00471-00	RESISTOR 470 OHM 1/4W 5% CAR	15
65	RS2-00473-00	RESISTOR 47 K 1/4W 5% CAR	1
66	RS2-00820-00	RESISTOR 82 OHM 1/4W 5% CAR	1
67	HDM-00003-09	BUS BAR PC MOUNT 9 POSITION	2
68	HDM-00003-11	BUS BAR PC MOUNT 11 POSITION	2
69	CNS-00008-00	SOCKET 8 PIN DIP	1
70	CPP-00225-01	CAPACITOR TANT 2.2 UF 20V	1
71	CPP-00156-01	CAPACITOR 15 UF 20V	7
72	CPN-00331-01	CAPACITOR 330 PF 200V 10%	1
73	CNA-00006-00	CONN RECEPTACLE SHORTING 2CONT BLK	1
74	CNF-00033-02	HEADER STRIP LINE PLUG MALE	2
75	RS2-00222-00	RESISTOR 2.2 K 1/4W 5% CAR	2
76	HDM-00013-00	VARNISH INSULATING SEALING	0
77	HDM-00012-00	THERMAL GREASE	0
78	DWL-00210-XX	LOGIC DBL DENSITY FLOPPY DISK CONT	0
79	DWS-00210-00	SPEC FLOPPY DISK CONT SUBSYSYTEM	0
80	DWT-00210-00	TEST SPEC DIAGNOSTIC AM-210	0
81		*** DELETED PART ***	0
82	DWI-00210-02	INST INSTR WANGCO AM-210	0
83	DWI-00210-03	INST INSTR SHUGART AM-210	0
84	RS2-00683-00	RESISTOR 68 K 1/4W 5% CAR	1
85	ICS-00500-00	IC DIGITAL DELAY LINE 500 NS	1
86	DIO-05221-00	ZENER 24V ZENES CIRCUIT 20MT	1
87	CBW-00026-15	WIRE 26AWG SLD GREEN TEF	1
88	RS2-00333-00	RESISTOR 33 K 1/4W 5% CAR	1
89	LBL-00002-00	LABEL WARRANTY VOID	2
90	LBL-00018-06	LABEL PCB SERIAL I.D. AM-210	1

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