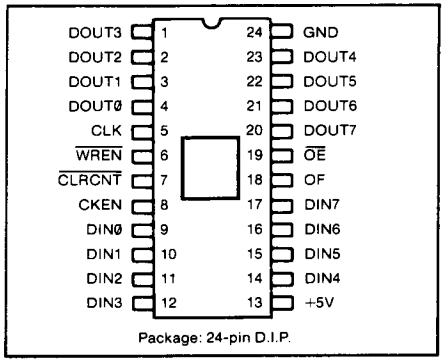
Single Row Buffer
SRB

FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 3.3MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



Package: 24-pin D.I.P.

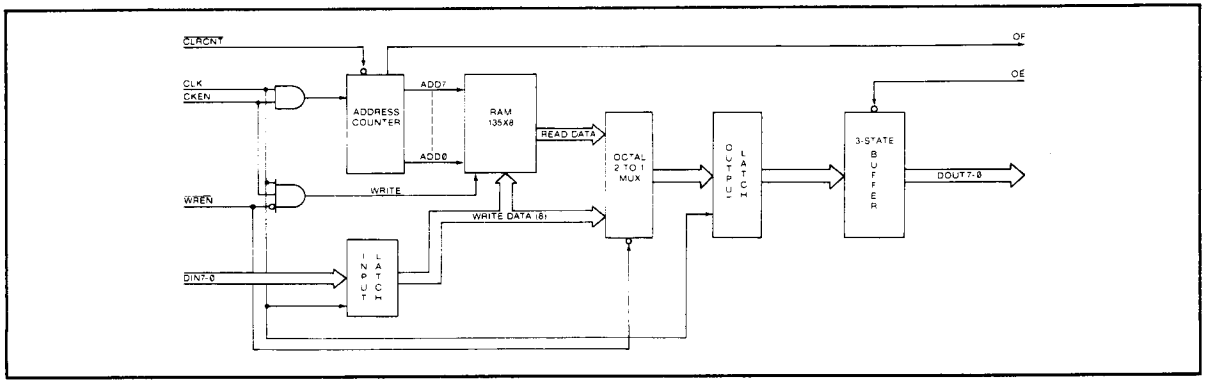
APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION V

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{WREN}$) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-4	DATA OUTPUTS	DOUT3-DOUTØ	Data Outputs from the internal output latch.
5	CLOCK	CLK	Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter.
6	WRITE ENABLE	$\overline{WREN}$	When $\overline{WREN}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM.
7	CLEAR COUNTER	$\overline{CLRCNT}$	A negative transition on $\overline{CLRCNT}$ clears the RAM address counter. $\overline{CLRCNT}$ is normally asserted low near the beginning of each scan line.
8	CLOCK ENABLE	CKEN	When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM.
9-12	DATA INPUTS	DINØ-DIN3	Data Inputs from system memory.
13	POWER SUPPLY	V_{CC}	+5 Volt supply.
14-17	DATA INPUTS	DIN4-DIN7	Data Inputs from system memory.
18	OVERFLOW FLAG	OF	This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip.
19	OUTPUT ENABLE	$\overline{OE}$	When $\overline{OE}$ is low, the data outputs DOUTØ-DOUT7 are enabled. When $\overline{OE}$ is high, DOUTØ-DOUT7 present a high impedance state.
20-23	DATA OUTPUTS	DOUT7-DOUT4	Data Outputs from the internal output latch.
24	GROUND	GND	Ground.

OPERATION

For CRT operation, the Write Enable ($\overline{WREN}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{CLRCNT}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{CLRCNT}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{WREN}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... -55° C to + 150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS ($T_A = 0°$ C to 70° C, $V_{CC} = +5 \pm 5\%$, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	$I_{OL} = 2mA$
High Level V_{OH}	2.4			V	$I_{OH} = -100\mu A$
Input Current Leakage, I_{IL}			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output '1' Leakage			10	μA	
Output '0' Leakage (Off State)			10	μA	
Input Capacitance					
CLK		30	45	pF	
All other inputs		10	15	pF	
Power Supply Current					
I_{CC} (SRB-135)			115	mA	
I_{CC} (SRB-83)			100	mA	
AC CHARACTERISTICS					
t_{cy}					
(SRB135)	300	250		ns	
(SRB83)	400	330		ns	
t_{CKL}					
(SRB135)	240	190	DC	ns	
(SRB83)	320	250	DC	ns	
t_{CKH}					
(SRB135)	28		5000	ns	
(SRB83)	34		5000	ns	
t_{CKR}					
(SRB135)			10	ns	$t_{CKH} = 28ns$
(SRB83)			10	ns	$t_{CKH} = 34ns$
t_{CKF}					
(SRB135)			10	ns	$t_{CKL} = 240ns$
(SRB83)			10	ns	$t_{CLK} = 320ns$
t_{DSET}	65			ns	
t_{DHOLD}	5			ns	
t_{ENCKP}	0			ns	
t_{ENCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{ENHOLD}	0			ns	
t_{WRCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{WENHLD}	0			ns	
t_{DOUT}			175	ns	$C_L = 50pF$
t_{TSON}			175	ns	
t_{TSOFF}			175	ns	
t_{OFON}			175	ns	$C_L = 30pF$
t_{CLRS}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{CLRH}	0			ns	

SECTION V

FIGURE 1: AC CHARACTERISTICS

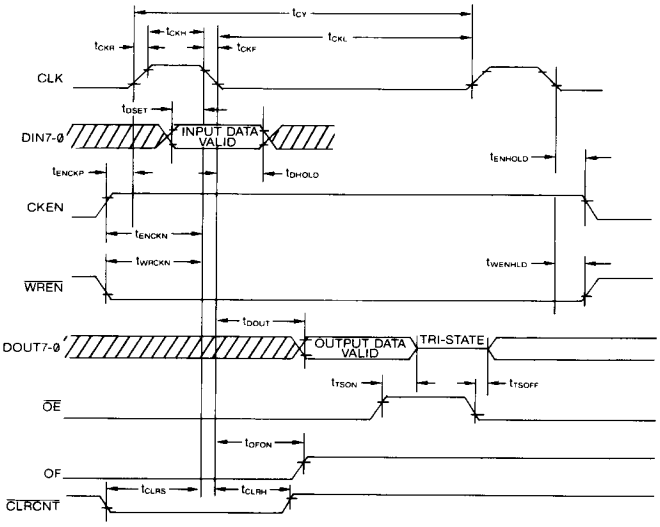


FIGURE 2: SINGLE ROW BUFFER READ TIMING

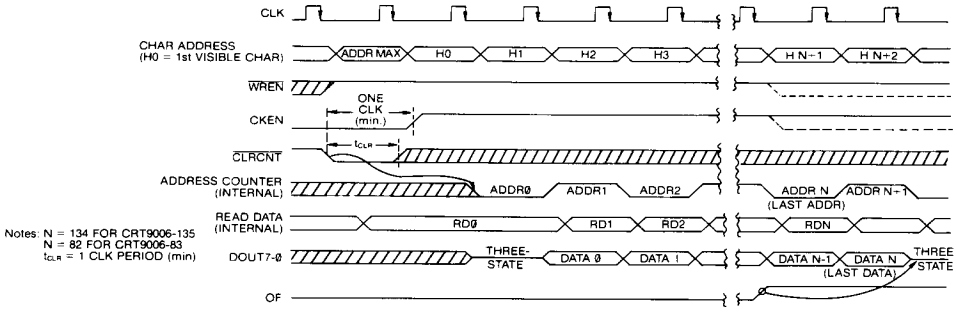
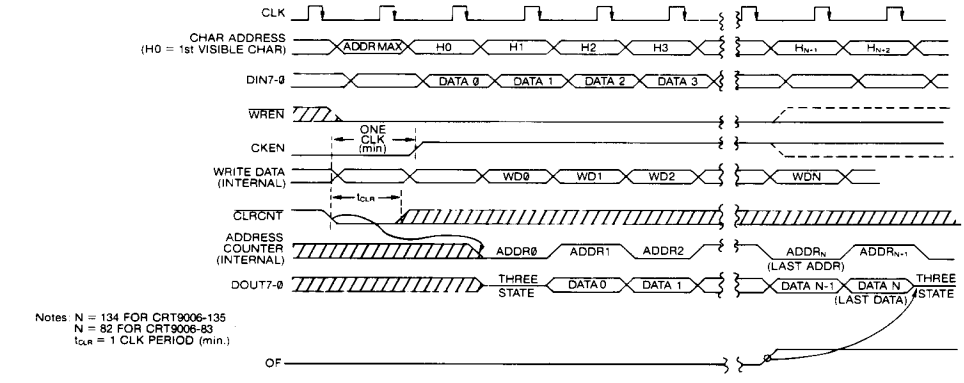


FIGURE 3: SINGLE ROW BUFFER WRITE TIMING



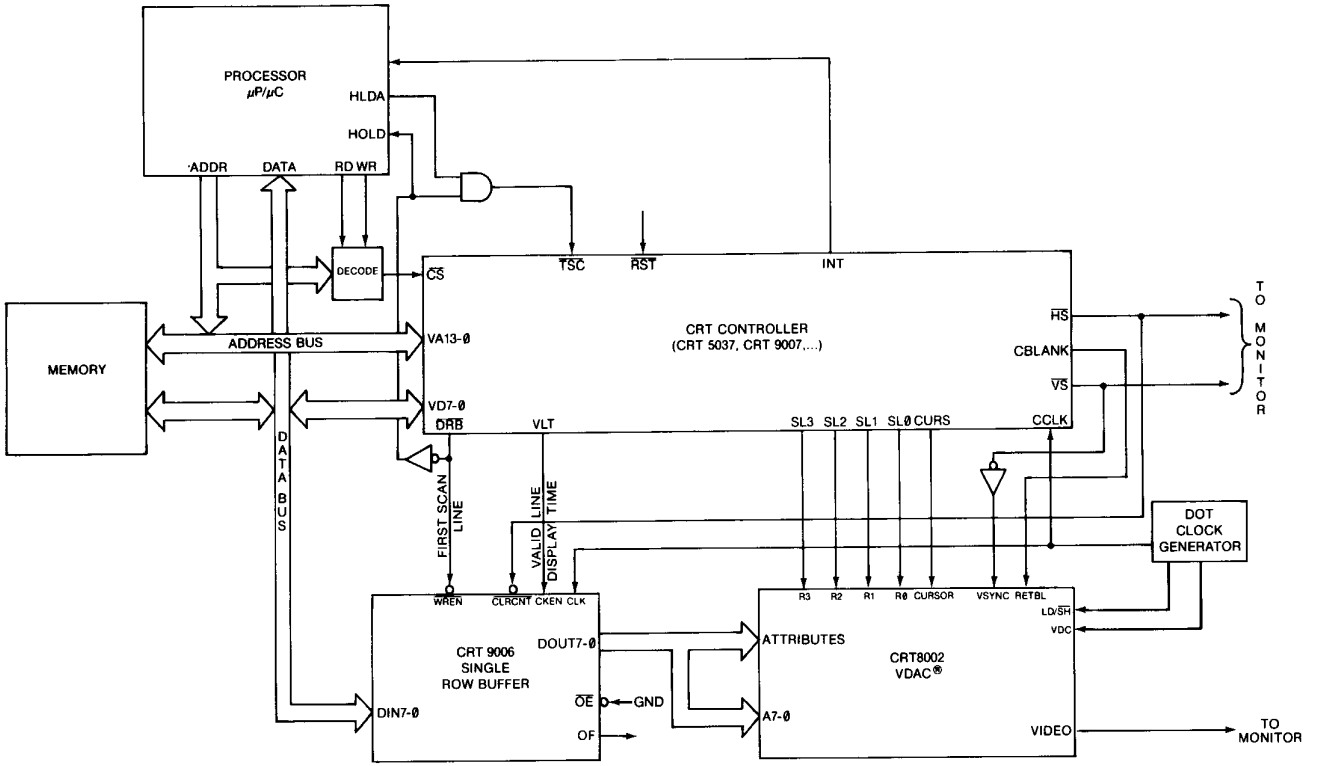
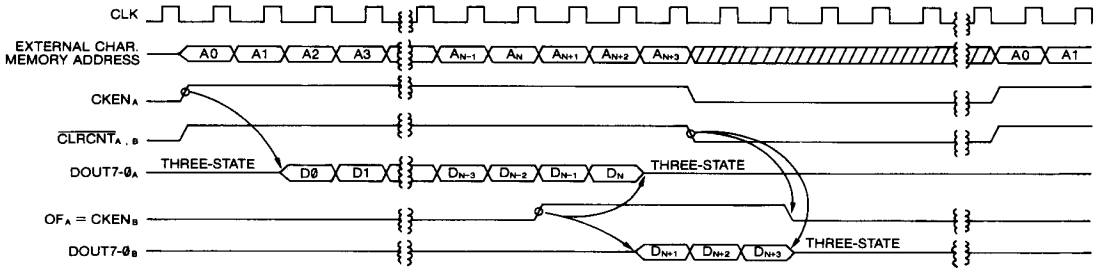


FIGURE 2: TYPICAL CRT CONTROLLER CONFIGURATION WITH SINGLE ROW BUFFER

FIGURE 4:
TYPICAL READ TIMING FOR SRB CASCADED CONFIGURATION



Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
EXAMPLE IS FOR N+3 CHARACTERS TOTAL
A, B REFER TO DEVICES A&B IN FIGURE 5

FIGURE 5:
TYPICAL CASCADE OF SINGLE ROW BUFFERS—270 BYTES TOTAL