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PROCUREMENT SPECIFICATION STORAGE MODULE DRIVE

DWG NO.

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### 1.2 Standard Equipment

The drive shall be a $3600 \mathrm{rpm}, 9.677 \mathrm{MHz}$ data rate, random-access mass memory device consisting of a disk pack spindle, drive motor and brake, a voice coil positioner and servo; a logic chassis with read/write, fault and transmitter/receiver electronics; an air supply and filter; and a DC power supply.

Standard features shall include a phased-lock data separator, NRZ-to-MFM data conversion, variable sector (address mark), organization capability, track-following servo and daisy-chain interface capability. These are defined in detail in this specification.

A hinged shroud cover on top of the drive shall allow access to the spindle for pack installation and removal. A separate enclosure cover shall provide access to the electronics, heads and actuator, linear motor, DC power supply and spindle motor, to perform maintenance procedures. Each major subassembly shall be removabie as an entity. Each drive shall come equipped with all the accessories as described in Section 10, i.e. all cables, terminators $\ddagger$ documentation
1.3 Configurations

### 1.3.1 Single Spindle

The 80 M-Byte device shall be housed in a desk-height acoustic cabinet. Space for mounting a second spindle shall be available in the cabinet base.

### 1.3.2 Dual Spindle

The 160 M-Byte Dual Spindle device shall be configured by placing the second spindle in the acoustic base cabinet. The second spindle shall be identical to the first one, except that it will be mounted on slides. Hardware, slides, ballast weight and filler panels shall be included.

NOTE: Each drive shall be delivered with a Cable Configuration and cables as specified on P.O., and shall meet all regulatory body (including U.L.) requirements for disk drives.

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### 2.0 GENERAL DESCRIPTION

### 2.1 Product Description

### 2.1.1 Logic Assembly

The standard logic building blocks shall be dual-in-line TTL integraded circuits, ECL integrated circuits shall be used in critical read/write timing areas. The logic chassis is cooled by forced air.

### 2.1.2 Positioner

Head positioning shall be performed by a closed loop proportional servo system. The carriage shall be driven by a voice-coil linear actuator with position feedback signal provided from the disk pack servo surface. The servo shall operate in two modes: A seek mode and a track-following mode. The linear motor shall be cooled by forced filtered air.
2.1.3 Disk and Spindle

A rigid, one-piece cast-aluminum deck-plate, spindle motor and special spindle assembly shall be used to preserve the dimensional and speed integrity necessary for the recording system. A dynamic spindle brake shall allow pack changes in less than one minute.

### 2.1.4 Air Supp1y

An enclosed air supply and filtering system shall be provided to meet the reliability requirement necessary for high density recording. Air shall be taken in through the bottom of the acoustic cabinet and discharged through the rear. The air passing over the disks, head-assembly and linear motor shall be filtered air.

### 2.1.5 Compatibility

The term "compatibility", when used in reference to this family of 3600 rpm drives refers to disk pack interchangeability between spindles. A disk pack written on one drive may be read on another similiar drive within the specified error rate. An industry standard spindle interface will assure disk pack interchangeability for procurement from multiple vendor sources.

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### 3.0 TECHNICAL DESCRIPTION

### 3.1 Disk Organization

The disk shall be an industry standard $14^{\prime \prime}$, 5-platter oxide=coated disk. The two outer disks shall be cover disks for protection, and the three inner disks shall have 5 data surfaces and one servo surface. The servo surface shall be pre-recorded with all the relevant servo-data.

The disk shall have an unformatted capacity of $82,152,000$ bytes.
Following are the specifications for disk-organization:
Total number of disks 5
Cover disks 2
Recording disks 3
Servo Surface 1
Data Surfaces 5
Sectors/track 64
Tracks/Cylinder 5
Cylinder/Spindle 823
Spare Cylinders/Spindle 15
Disk Diameter in inches 14"
Servo Head 1
Recording Heads 5
Rotational Speed $\quad 3600 \mathrm{tpm}+2.5 \%,-3.5 \%$
Data-Transfer rate $\quad 9.677 \mathrm{MHz}$
Data Capacity (unsectored, unformatted)
Data Bytes ./track 20,160
Data Bytes/Cylinder $\quad 100,800$
Data Bytes/Spindle 81,446,400
(excluding spare cyls.)
Data Capacity (Electronically sectored, formatted)
Sectors/track64

Data Bytes/Sector 256
Data Bytes/track 16,384
Data Bytes/Cylinder 81,920
Data Bytes/Spindle 66,191,360


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### 3.3.2 (Continued)

The maximum positioning time shall be 55 ms . This is defined as the time to move the head from track 0 to track 814 , or vice-versa.

The maximum single-track positioning time shall be 6 ms . This is defined as the time to move between any pair of adjacent tracks.

The maximum average positioning time shall be 30 ms . This is defined as the time taken to make all possible moves divided by the number of all possible moves.

### 3.3.3 Latency Time

The average latency time is 8.33 ms , based on a nominal disk speed of 3600 rpm .

The maximum latency shall be 17.3 ms , based on a maximum disk speed of 3474 rpm ( $3600-3.5 \%$ ).
Latency time is defined as the time required to reach a particular location on a track after positioning is complete.

### 3.3.4 Head-Selection Time

Between the deselection of one head and the selection of another head, there shall be no more than $5.0 \mu \mathrm{~s}$ delay within the drive.
3.3.5 Read-Amplifier Stabilization

The maximum time for head-amplifier stabilization after Readselection is complete, shall be $10 \mu \mathrm{~s}$.

### 3.3.6 Read-Initialization Time

The time from the initiation of a head change until data can be read with a selected head without error shall be $24 \mu$ s maximum, ( $5.0 \mu \mathrm{~s}$ for head selection, $10.0 \mu \mathrm{~s}$ for read-amplifier stabilization and $9.0 \mu \mathrm{~s}$ for phase-lock synchronization).

### 3.3.7 Write-To-Read Recovery Time

Assuming head-selection is stabilized. the time lapse required by drive for read gate to be enabled after switching the gate off shall not exceed $15 \mu \mathrm{~s}$.

### 3.3.8 Read-to-Write Recovery Time

Assuming head-selection is stabilized, the time lapse required by drive from dropping read gate to enabling write gate shall not exceed $1.0 \mu \mathrm{~s}$.


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### 3.3.2 (Continued)

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### 3.3.8 Read-to-Write Recovery Time

Assuming head-selection is stabilized, the time lapse required by drive from dropping read gate to enabling write gate shall not exceed $1.0 \mu \mathrm{~s}$.

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3.3.9 Offset Timing

Whenever an offset command is issued from nominal position, On-Cylinder and Seek-end signals shall go false for no more than 3.2 ms .

The maximum time for the carriage to move from forward to reverse offset or vice versa shall not exceed 7 ms . Data shall not be written while in the offset mode.

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|  | Data Errors <br> The following error rates assume that the drive is adjusted to specification, that the appropriate disk pack is being used and the errors caused by media defects or equipment failures are excluded. To minimise errors caused by media defects, only the media from manufacturer-approved vendors shall be used for determination of data integrity and reliability. <br> 3.4.1 Read Errors <br> Prior to determination of a Read Error Rate, the data shall have been verified as written correctly and all media defects flagged. <br> a. Recoverable Read Error Rate <br> A recoverable error is one which may be corrected by no more than 3 attempts to read the record at zero offset and nominal strobe, 3 attempts each at zero offset position with early and late strobes and 3 attempts each at each offset position with early, nominal and late strobes - - ( 27 reads). Any combination of Seek-Write, Seek-Read, Seek-Restore shall be allowed without limitation of combination and duty cycle. Data patterns and Track position shall not affect Data Error Rate performance. <br> The Recoverable Read Error Rate shall be less than one error in $10^{10}$ bits. <br> b. No Recoverable Read Error Rate <br> A non-Recoverable Read Error is one which remains after the 27 attempts (described above) to read the record in which the error is located. <br> The Non-recoverable Read Error Rate shall be considered as failures affecting MTBF. |  |  |  |
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When operating at a low effective data transfer rate, e.g. random access of single short records, the effective error rate may be expected to exceed the above limits only due to external environmental interference. The resulting Recoverable Read Error Rate shall be less than one error in 8 hours of operation.

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|  | 3.5 Data Security and Integrity <br> 3.5.1 Data Security <br> Under no circumstances of normal controller I/O operation, shall it be possible to write a pattern not corresponding to that on the write data lines. It shall be possible to alter the bit pattern only when the drive signifies an On-Cylinder Status, and then only upon specific drive selection. <br> Data shall be protected by inhibiting Write Gate in all fault conditions including a loss of On-Cylinder, Seek-error, or LowVoltage. <br> Under any of the following conditions, an emergency retract of the heads shall be performed, so that data is protected by either the above mentioned fault conditions, or by switching of the voltage required to write. These conditions are: <br> 1. Loss of AC line power. <br> 2. Loss of speed <br> 3. Loss of any DC voltage. <br> 3.5.2 Data Integrity <br> Errors attributed to operator mishandling of the data pack which may be detected and flagged during the initialization of the pack are not included in determination of the error rates. |  |  |  |  |
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### 4.0 INTERFACE

The interface shall consist of two flat cables.

1. "A" Cable - shall be a bussed cable, connected to all drive in a daisy-chain fashion.
2. "B" Cable - shall be a radial cable connected between the controller and each drive. Thus, for an 8 -drive subsystem, there shall be 8 "B' cables.

The A cable shall carry all the signals that are used by only one drive at a time, so that only a selected drive shall be able to communicate with the controller via "A" cable.

The "B" cable shall carry data and clock signals (transmission bandwidth sensitive signals) as well as those logical signals which all the drives must use at all times.

See Figure $\overline{1}$ for Cable Configuration

### 4.1 Interface Electrical Description

All input and output signals shall be digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noisy environment.

Transmitters and Receivers of the industry standard type 75110A and 75108 or equivalent shall be used to provide a terminated, balanced transmission system. Each signal shall have two lines assigned to it, unless otherwise specified: Active high and active low. Generally, the higher order pin of the two pins shall carry the high signal.

### 4.1.1 Line Transmitter Characteristics

The controller input amplifier shall be compatible with the transmitter described below, which shall be used on drive-output lines. Furthermore, Controller line transmitter shall also follow the same characteristics.

## a. Output Line Polarity

Control Signals. The transmitter shall be connected to the $I / O$ line such that the output, labeled active low shall correspond with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B (active low), except for the Unit Selected line, which shall be connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver.

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b. Output Propagation Delay

The transmitter propagation delay shall typically be 15 ns in the direction of the logical 1 and 15 ns in the direction of the logical 0 .
4.1.2 Line Receiver (Input Amplifier) Characteristics

The Controller Line Transmitter shall be compatible with the Input Amplifier described below, which shall be used on drive input lines. Furthermore, Controller input amplifier shall also follow the same characteristics.

## a. Receiver Input Polarity

Control Signals: The Receiver shall be connected to the $I / 0$ line such that the input, labeled B (active low) shall correspond with the low order pin number of the pair of pins assigned to the signal, and in turn connect to transmitter pin labeled $Z$ (active low), except for the Unit Selected line, which shall be connected in the opposite manner.

## b. Receiver Propagation Delay

The receiver propagation delay shall typically be 17 ns in the direction of the logical 1 and 17 ns in the direction of the logical 0.
4.1.3 Recommended Line Receivers (Input Amplifiers) and Transmitters (Output Drivers)

Line Receivers

| National | SN75107A |
| :--- | :--- |
| Signetics | SN75107A |
| National | DS75108 |
| Signetics | SN75108 |

Line Drivers
Texas Instruments
SN75110J
Fairchild
SN75110J

### 4.1.4 Flat Cable Characteristics

Each drive shall be delivered with a Cable Configuration and Cables as specified on P.O. and shall meet all regulatory body requirements for disk-drives by jacketing the cables, if necessany.
A. Bussed or Signal Cable (Cable "A")

Type $\quad 30$ twisted-pair twist-and-flat cable.

Wire Size
Impedance
Termination
High Level
Low Level
Logical States
Maximum Cable Length
Voltage Rating
B. Radial or Data Cable (Cable "B")

Type
Wire Size
Impedance
Termination
High Level
Low Level
Logical States
Maximum Cable Length
Voltage Rating
4.1.5 Termination

26 per connector ribbon flat cable w th ground plane and drain wire.
No. 28 AWG, 7 strands
130 OHMS, +15 OHMS
82 OHMS, $\pm 5 \%$ (See figure 3)
OV Ground
-0.62 V Max., -0.26V Min at Receiver (includes Max Line Loss)
P Line High, M Line Low - Logic 1)
P Line Low; M Line High - Logic 0
50 ft .
300 V RMS
A. "A" Cable Termination (Bussed Signal Cable)

A termination resistance of $56 \Omega$ as shown in figure 2 is required at the transmitter and receiver end of each transmission line of the "A" cable. The resistance shall be provided on the unit by the terminator assembly.

A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect Line. See paragraph 4.3.2.A.4. No termination resistance is used on the Power Sequence lines in the "A" cable.
B. "B" Cable Termination (Radial Data Cable)

A termination resistance of $82 \Omega$ as shown in figure 3 is required at the transmitter and receiver end of each "B" cable transmission line. This resistance shall be provided on the unit by the Receiver logic card.


Fig. 2 Bussed (Signal) Cable Driver/Receiver Cable Termination Circuit (A Cable)

50 Ft. Max. of Flat Cable having $130 \pm 13$ Ohms Characteristic Impedance.


Fig. 3 Radial (Data) Cable Driver/Receiver Cable Termination Circuit (B Cable)


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### 4.3 Interface Logic Description

4.3.1 Logic Signal Tables
4.3.1.A "A" Cable (Bussed Signal Cable)

| M Line (Active Low) |  | P Line (Active High) |  | SIGNAL | SOURCE |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | = DRIVE) |
| $\underline{\text { PIN NO. }}$ | MNEMONIC | PIN NO. | MNEMONIC | NAME | C | = CONTROLLER) |

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2

| UNITSELO/ | 52 | UNITSELO/ |
| :---: | :---: | :---: |
| ITAG1/ | 31 | ITAG1 |
| ITAG2/ | 32 | ITAG2 |
| ITAG3/ | 33 | ITAG3 |
| IBUSO/ | . 34 | IBUSO/ |
| IBUS1/ | 35 | IBUS1 |
| IBUS2/ | 36 | IBUS2 |
| IBUS3/ | 37 | IBUS3 |
| IBUS4/ | . 38 | IBUS4 |
| IBUS5/ | 39 | IBUS5 |
| IBUS6/ | 40 | IBUS6 |
| IBUS7/ | 41 | IBUS7 |
| IBUS8/ | 42 | IBUS8 |
| IBUS9/ | 43 | IBUS9 |
| IUNITSEL1/ | 53 | IUNITSEL1 |
| IUNITSEL2/ | 54 | IUNITSEL2 |
| IUNITSEL4/ | 56 | IUNITSEL4 |
| IUNITSEL8/ | 57 | IUNITSEL8 |
| IINDEXM/ | 48 | IINDEXP |
| ISECTORM/ | 55 | ISECTORP |
| IFAULTM/ | 45 | IFAULTP |
| ISEEKERRORM/ | 40 | ISEEKERRORP |
| ION CLLINDERM/ | 47 | IONCYLINDERP |
| ICABLEIN/ | 44 | ICABLEIN |
| IUNITREADYM/ | 49 | IUNITREADYP |
| IAMDETM/ | 50 | IAMDETP |
|  | 58 |  |
| IPICK |  |  |
| IHOLD |  |  |
|  | $\begin{aligned} & 60 \\ & 51 \end{aligned}$ |  |


| Unit Select Tag | C |
| :---: | :---: |
| TAG 1 (Set Cylinder) | C |
| TAG 2 (Set Head) | C |
| TAG 3 (Control) | C |
| BUS BIT 0 | C |
| BUS BIT 1 | C |
| BUS BIT 2 | C |
| BUS BIT 3 | C |
| BUT BIT 4 | C |
| BUS BIT 5 | C |
| BUS BIT 6 | C |
| BUS BIT 7 | C |
| BUS BIT 8 | C |
| BUS BIT 9 | C |
| UNIT SELECT 1 | C |
| UNIT SELECT 2 | C |
| UNIT SELECT 4 | C |
| UNIT SELECT 8 | C |
| INDEX | D * |
| SECTOR | D |
| FAULT | D |
| SEEK ERROR | D * |
| ON CYLINDER | D |
| OPEN CABLE DETECTOR | C |
| UNIT READY | D |
| ADDRESS MARK FOUND | D |
| WRITE PROTECTED | D |
| POWER SEQUENCE PICK | C |
| POWER SEQUENCE HOLD | C |
| NOT USED (SPARE) |  |
| NOT USED (SPARE) |  |

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4.3.1.B "B" Cable (RADIAL DATA CABLE)

| M Line | (Active Low) | P Line | Active High) | SIGNAL | SOURCE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PIN NO. | MNEMONIC | PIN NO. | MNEMONIC | NAME | $\begin{aligned} & (\mathrm{D}=\overline{\mathrm{DRIVE})} \\ & (\mathrm{C}=\text { CONTROLLER }) \end{aligned}$ |
| 8 | IWRITEDATAM/ | 20 | IWRITEDATAP | WRITE DATA | C |
| 2 | ISERVCLKM/ | 14 | ISERVCLKP | SERVO CLOCK | D |
| 3 | IRDDATAM/ | 16 | IRDDATAP | READ DATA | D |
| 5 | IRDCLKM/ | 17 | IRDCLKP | READ CLOCK | D |
| 6 | IWRTCLKM/ | 19 | IWRTCLKP | WRITE CLOCK | C |
| 10. | ISEEKENDM/ | 23 | ISEEKENDP | SEEK END | D |
| 22 | IUNITSELECTM/ | 9 | IUNITSELECTP | UNIT SELECTED | D |
| 12. |  | 24 |  | RESERVED (INDEX) | D |
| 13 |  | 26 |  | RESERVED (SECTOR) | D |
|  |  | 7 |  | GROUND |  |
|  |  | 18 |  | GROUND |  |
|  |  | 1 |  | GROUND |  |
|  |  | 15 |  | GROUND |  |
|  |  | 4 |  | GROUND |  |
|  |  | 21 |  | GROUND |  |
|  |  | 11 |  | GROUND |  |
|  |  | 25 |  | GROUND |  |

NO SIGNALS GATED BY UNIT SELECTED.

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| 4.3.2 Logic Signal Description <br> 4.3.2.A "A" Cable (Bussed Signal Lines) <br> Following are the signal lines on the A-Cable <br>  <br> A Power Sequencing scheme shall be used for starting one drive at a time when several drives are daisy-chained together. Such Power-sequencing requires, $A C$ and DC power on for all the active drives, (i.e. Those drives slated for power-up) in the chain. Furthermore on each drive, the START indicator shall be ON, and REMOTE START SWITCH (Switch Selectable in drive) shall be in the REMOTE position. <br> PICK and HOLD signals when activated shall cause the first drive in the sequence to power-up. PICK shall be held active low for a minimum of 250 milliseconds after the signal HOLD is asserted, if only one drive is under control. <br> In multiple-drive daisy-chain, the PICK signal is transferred to the next active drive in the chain, once a drive is powered-up. NOTE that any intermediate drive in the chain may not be active : AC or DC power may not be ON, or start indicator may not be ON or Remote Switch may not be in REMOTE position. Such inactive drive shall transfer the PICK signal immediately to the next drive in the chain. This procedure shall be repeated until all the drives are powered up. Individual drives may be started or stopped independently once power sequencing has completed. <br> When several drives are daisy-chained, it shall be necessary to hold the signal PICK active low until all the drives in the chain have powered up, since the signal PICK is passed-on down the chain only after a drive comes up to speed. Hence, PICK must be held active low for 20 n seconds (typically), when " $n$ " drives are daisy-chained together. <br> The PICK signal may be taken into an inactive high state after this initialization sequence. <br> The HOLD signal used in conjunction with the PICK signal, shall be held active low for the entire duration of a time that a controller expects a drive to remain powered up. The HOLD signal simply loops from one drive to the next when a daisy-chain configuration is employed. When the HOLD signal is taken into an inactive high state by the Controller, every drive in the daisy chain shall be sequenced down. |  |  |


| SHT 24 | REV |
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REV

### 4.3.2.A. 1 (Continued)

Once a drive daisy-chain is sequenced down, it shall be necessary to issue both the PICK and HOLD signals to cause a drive to sequence up.

A power-failure shall necessitate a new power-up sequence.
When in the LOCAL START mode, each drive shall be able to start independently by its respective START switch.

The active low signal for HOLD and PICK lines is at ground potential. This ground must sink 0.5 MA per unit, With 15 units on a system, the current is 7.5 MA . The controller may provide this ground either through a mechanical contact (relay or switch) or through an electronic circuit.
4.3.2.A. 2 Unit Select Tag - Pins 22 and 52

This signal shall gate, the desired logical unit number transmitted over the 4 Unit Select Lines into the Logical Address Compare Circuit. The unit shall be selected internally within 600 ns of the leading edge of this signal. Note that this function must be edge-triggered.
4.3.2.A. 3 Unit Select $1,2,4 \&, 8$ - Pins $23,24,25,26$ and $53,54,55,56$

These four lines are binary coded to select one of 15 logical drive units ( $0-14$ ). Ths unit number ( $0-14$ ) shall be selected by means of an address selector plug inserted into the operator control panel of each individual unit. Removal of the plug shall be decoded as logical address 15 , which shall not be allowed for normal operations, but may be used as maintenance select. The operator must verify that no duplicate plugs are installed in drives on the same control bus.
4.3.2.A. 4 Open Cable Detector - Pins 14 and 44

The Open Cabel Detector signal, when active, shall indicate an open "A" Cable (bussed signal cable), or loss of controller power, whereupon the interface at the drive (receivers and transmitters) shall be disabled.

The controller circuitry shall have sufficient voltage margins and interlocks to prevent operation on the drive
(i) before controller is ready or
(ii) prior to impending controller power failure.

If 75110A transmitters are used to drive the Open Cable Detect line from the controller, then two transmitters shall be paralleled, and no $56 \Omega$ termination resistance to ground shall be used at the controller end.

DWG NO.

| SHT | 25 | REV |
| :--- | :--- | :--- |

### 4.3.2.A. 5 Unit Ready - Pins 19 and 49

When active and the unit is selected, this line shall indicate that the unit is up to speed, the heads are loaded, and no fault condition exists within the drive. If after a load sequence, servo dibits are not sensed within 350 ms , the heads shall unload, the fault light shall be indicated, and Unit Ready shall be dropped. Further load attempts shall require operator intervention to depress FAULT CLEAR, whereupon heads shall be loaded.

### 4.3.2. A. 6 Fault - Pins 15 and 45

When active, this line shall indicate that at least one of the following error conditions is active in the drive.
(a) DC Voltages unsafe - below normal voltage from the positive or negative power supply
(b) Head Select Fault - i.e., Read or Write with more than one amplifier head selected
(c) Write fault - Low (or absence of) write current or absence of write data
(d) Offset fault - write with offset active
(e) Read Gate and Write Gate active simultaneously
(f) Read or Write while off cylinder
(g.) Write Protect fault - Write attempt with Write Protect activated.
(h) Write Current on but no write gate.

A fault condition shall immediately inhibit the writer to prevent data destruction.

This line may be cleared by Control Select, or Fault Clear on the Operator Panel, or Master Fault Clear Switch provided within Drive electronics, (provided the fault condition no longer exists). Faults shall be stored in individual flip-flops as a maintenance aid, and may be cleared only by one of the above means or by powering down DC power.

### 4.3.2.A. 7 Write Protected - Pins 28 and 58

Write Protect function can be activated from a switch on the Operator's panel of an individual unit. When this function is activated, the Write Protected line shall become active, a front panel indicator shall be illuminated and the writer shall be inhibited under all conditions. Attempting to write while protected shall cause a fault to be issued.



| SHT | 28 | REV |
| :--- | :--- | :--- |

### 4.3.2.A. 8 (Continued)

(7) BUS 6 - RTZ - Return to Zero

If the heads are loaded on the disk, then a 250 ns minimum, 1 ms maximum pulse on this signal line, shall cause the actuator to reposition the heads to cylinder zero, reset the head-register and reset the following conditions.
(a) Seek Incomplete
(b) Illegal Cylinder Address
(c) Illegal Head Address
(8)

BUS 7 - Data Strobe Early
When this signal is held true, the drive PLO separator shall strobe the data at a time earlier than nominal. When the signal line goes false, nominal strobe-timino shall be returned. This function shall be available only for recovery of data, and not for writing data on the disk.
(9) Bus 8 - Data Strobe Late

When this signal is held true, the above PLO separator shall strobe the data at a time later than nominal. When the signal line goes false, nominal stroke-timing shall be returned. This function shall be available only for recovery of data, and not for writing data on the disk.

Note: The Data Strobe and Carriage offset signals are intended to be used as an aid to recover marginal data. The carriage and data strobe position return to nominal when the respective signals go false.

A carriage offset shall result in loss of On-Cylinder and Seek-End signals for a period of 3.2 ms maximum. The maximum time for the carriage to move from forward to reverse offset or vice-versa will not exceed 7 ms . Data shall not be written while in the offset mode.

When dropping offset Forward or Reverse, a 4 ms delay shall de required before a Read or Write can be initiated

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| SHT | 29 |
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### 4.3.2.A. 9 INDEX - Pins 18 and 48

The INDEX signal shall be a $2.5+0.3 \mu \mathrm{sec}$ wide pulse. It shall go active once per evolution, and shall indicate the starting point of data track (and sector zero) with its leading edge. Timing integrity shall be retained throughout seek operations.
4.3.2.A. 10 SECTOR - Pins 25 and 55

The SECTOR signal shall be a $1.24 \pm 0.24 \mu_{\text {sec }}$ wide pulse, and shall indicate the start of a sector with the leading edge. The sector mark shall be derived from the servo track, Timing integrity shall be maintained throughout seek operations.
The number of sectors per revolution shall be switch-selectable and switch-setting shall be determined by counting dibits/sector. Each dibit shall be equivalent to 12 data bits and number of dibits/ revolution shall be 13440 . The switches shall be located on a card within the logic chassis, and shall be binary coded, so that each switch shall represent a fixed number of dibits (a power of 2) when closed.
$\begin{array}{lllllllllllll}\text { Switch } & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11\end{array}$
No, of
Dibits $1 \begin{array}{llllllllllll}2 & 4 & 8 & 16 & 32 & 64 & 128 & 256 & 512 & 1024 & 2048\end{array}$
Thus, switch n shall represent $2^{\mathrm{n}}$ dibits when closed.
To calculate the paper switch positions for the number of sectors desired, following formula shall be used:
$\frac{\text { Dibits/revolutions }}{\text { No. of Sectors }}-1=$ Dibits Count/Sector
Example of 8 Sectors: $\quad \frac{13440}{8}-1=1679$

| Close Switch 10 | $=$ | 1024 |  |
| :--- | :--- | :--- | ---: |
| 9 | $=$ | 512 |  |
| 7 | $=$ | 128 |  |
| 3 | $=$ | 8 |  |
| 2 | $=$ | 4 |  |
|  | 1 | $=$ | 2 |
|  | 0 | $=$ | 1 |

One dibit from
Sector-Mark
Counter Reset
$\frac{1}{1680}$ Dibits/Sector

The drives shall be shipped with the sector switches set for 64 Sectors/track.

## 4.3,2.A.11 SEEK ERROR - Pins 16 and 46

When SEEK ERROR signal is active, it shall indicate that a seek error has occured, due to one of the following conditions.
(i) The actuator unit was unable to complete a servo operation within 500 ms .
(ii) The carriage has moved to a position outside the recording field.
(iii) A cylinder address greater than 823 was issued. (In this case, the Seek Error signal shall go true within 100 ns of the Cylinder Select Tag, and the carriage movement is inhibited to no more than one track).
The SEEK ERROR signal shall be reset only by a Return-to-Zero command or Manual Restart.
4.3.2.A. 12 On-Cylinder $=$ Pins 17 and 47
When "On Cylinder" is active, it shall indicate that the servo has positioned $\mathrm{R} / \mathrm{W}$ heads over a track. On Cylinder shall go inactive with any Seek instruction causing carriage movement (including a Return-to-Zero command). An offset command shall cause On-Cylinder to go inactive for 2.75 milliseconds. For a zero track-seek, on-cylinder shall drop for $30 \mu \mathrm{sec}$ (nominal). 4.3.1.A. 13 Address Mark Found - Pin 20 and 50
Address Mark Found shall be a $7.0 \mu_{\mathrm{s}}$ (nominal) pulse which is sent to the Controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern, if address Mark Enable and Read Gate signals are active.
The Controller shall drop the Address Mark Enable Signal within $1 \mu s$ of receiving Address Mark Found (AMF) and valid data shall be presented by the drive on the $I / 0$ lines following the AMF pulse.

DWG NO.

| SHT | REV |
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## REV

4.3.2.B "B" Cable (Radial Data Bus)

B Cable signals shall be those signals, which are continuousiy required by the Controller at all times and/or those signals which are required for data-channel operations. No signals on the " $B$ " cable is gated by unit select condition.
Following are the signals on the Radial Data Bus:
4.3.2.B. 1 Wríte Data- Pins 8 and 20

This line shall carry NRZ Write data from the Controller to the drive to be written on the Disk Pack.
4.3.2.B. 2 Servo Clock - Pins 2 and 14

Servo Clock shall be $9.677 \mathrm{MHz} \pm \%$ of Speed Variation clock generated from and phase-locked to servo-track dibits. Servo clock shall be available to the Controller at all times (not gated with Unit Select) and shall be used to form Write Clock
4.3.2.B. 3 Read Data - Pins 3 and 16

This line shall carry recovered data from disk pack as NRZ Read data from the drive to the controller.

### 4.3.2.B. 4 Read Clock - Pins 5 and 17

Read clock shall be an internally derived clock signal at 9.677 MHZ $\pm \%$ speed variation, which is phased-locked to the detected data. This signal shall be transmitted continuously and shall be in phase-sync with the detected data within $9 \mu_{s}$ after Read Gate becomes active.

### 4.3.2.B.5 Write Clock - Pins 6. and 19

The Write Clock shall be the servo-clock retransmitted to the drive by the controller, during a write operation. The NRZ Write data shall be synchronized to the Write Clock by the controller. The write clock need not be transmitted continuously, but shall be transmitted at least 250 ns prior to Write Enable.

$$
\text { 4.3.2.B. } 6 \text { Unit Selected }- \text { Pins } 22 \text { and } 9
$$

When active, Unit Selected signal shall indicate the drive is selected. When the Unit Select bit lines compare with the logic plug on the control panel of the drive (drive address), and the degate switch is in the normal operating position, then within 400 ns of the leading edge of the Unit Select Tag, the Unit Selected Line shall become active.



| $A \operatorname{sunNTVALE}^{\text {CALIFORHIA }}$ | dWG No. |  |  |
| :---: | :---: | :---: | :---: |
|  | SHT | 34 | REV |

(a) Beginning-of-Record Tolerance

This tolerance shall be provided to allow for worst-case conditions of head skew and circuit tolerances which may accrue during pack interchange.

This gap shall be written with a minimum of 16 bytes of zeros, which is minimun 13.23 us at $9.677 \mathrm{Mbits} / \mathrm{sec}$. Thus, this gap shall also be sufficient for Read Amplifier Stabilization ( $10 \mu \mathrm{~s}$ ).
(b) Read PLO Synchronization

The synchronization time needed to allow the phase-1ocked oscillator to synchronize shall be 9 is of zeros.
(c) Sync Pattern

The sync pattern shall consist of "one" bits indicating the beginning of the ID, Address or Data area. (Minimum of one "one" bit is required).
(d) Write Driver Turn-On

The Write Driver Turn-on time is about $0.8 \mu s$ or one byte. This time has to be accounted for to know where possible splice areas are located.

This turn-on time is included in the beginning-of-Record Tolerance.
(e) Write-Driver Turn-off time

The write driver turn-off time is also about $0.8 \mu \mathrm{~s}$ or one byte, and is provided for by a one byte long write-gap pad at the end of Data and Check portion of a record.
(f) End-of-Record Tolerance Gap

This tolerance is an eight-byte pad of zeros, which eliminates, the possibility that the end of a record written with a late displacement head may get destroyed by writing of an adjacent succeeding sector with an early displacement head on another pack, or vice versa.

The disk pack shall be formatted with 64 sectors per track on 823 cylinders containing 5 heads per cylinder physically. Each sector shall consist of 315 bytes, and this number shall be strapped into the sector jumper plugs as outlined in Section 4.3.2.A.10:

DWG NO.

| DWG NO. |  |  |
| :--- | :--- | :--- |
| SHT | 35 | REV |

REV
5.2.1 (Continued)

SECTOR FORMAT


Figure 4

### 5.2.2 Write Format Procedure

Provisions shall be made within the Controller to format the disk. The following procedure shall be followed for the above fixed sector format.

## PROCEDURE

(a) Select Desired unit, cylinder, head and sector.
(b) The controller shall provide a minimum $5 \mu \mathrm{~s}$ delay between selecting a head and initiating a search for leading edge of a sector. The delay shall ensure that the unit will be ready to write when the sector leading edge is detected.
(c) Search for leading edge of desired sector. - by counting the sector pulses after an index pulse.
(d) Detect leading edge of selected sector.
(e) Immediately bring up Write Gate and start writing zeros.
(f) Write all zeros for head-scatter and PLO Sync bytes (27 bytes).
(g) Write a Sync Pattern, the Header field, the Data field, the Header-Data field Checkword and the one byte pad at the end of the checkword. The data field shall be written with all one's or preferably a worst-case pattern.
(h) The End-Tolerance Gap is the only part of the format where there may be erased areas with no write data.
(i) If the next sector of the same track is to be formatted and the head is not deselected, the write gate may be left on, otherwise, it should be turned off. If the Write Gate is left on, the controller should write all zeros in the tolerance gap.

## DWG NO.

| SHT | 36 |
| :---: | :---: |
|  | REV |

5.2.3 Control Timing \& Procedure (Write and Read)
(a) Write

The Control line associated with a Write Operation is Write Gate.
The sector address from the header field shall always be read and verified prior to writing the data field, except while formatting.

Writing the data field shall always be preceded by writing the PLO Sync field and the Sync pattern.

The controller shall provide a three bit internal delay (approx. $0.3 \mu \mathrm{~s}$ ) between the trailing edge of the Read Gate Signal and the leading edge of the Write Gate Signal. This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the Unit.

Writing the data field shall always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, write Gate shall be raised immediately upon sensing index or sector. During a record update, Write Gate shall be raised within two bit time of sensing the selected sector-address.
(b) Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate shall force the phase-locked oscillator (PLO) to synchronize on an all zeros pattern. Read gate shall enable the output of the data separator into the $1 / 0$ lines after a lock-to-data internal time-out. Read Gate shall be dropped and raised again after going through a splice area. Read Gate may be enabled $60 \pm 4$ clock counts after the leading edge of index or sector.

The sync-pattern search may begin 88 servo clocks counts after the leading edge of Read-Gate.

Head Switching (5.0us), and Read-Amp1ifier Stabilization (10.0 s ) times determine the latest acceptable time at which a head can be selected in order to read the next successive sector.

Data $1 / 0$ lines may not have valid data until $9 \mu \mathrm{~s}$ from leading edge of Read Gate, due to phase-lock Synchronizing time. However, they must be valid after this period of $9 \mu \mathrm{~s}$.

There shall be no splice area after the Read Gate is brought up under worst case pack interchange conditions.

DWG NO.
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### 5.3 Error Correction

Two methods for recovering temporary errors shall be provided. The heads may be positioned slightly off-track in either direction and the data may be strobed early or late. Once an error is detected, two additional attempts shall be made to reach the record at zero offset and nominal strobe. The Strobe shiall then be varied at zero offset and at each offset position, (two attempts at each setting). Thus, a total of 27 attempts shall be made at reading the record , as follows:

| 3 attempts | zero offset, | nominal strobe |
| :--- | :--- | :--- |
| 3 attempts | zero offset, | early strobe |
| 3 attempts | zero offset, | late strobe |
| 3 attempts | plus offset, | nominal strobe |
| 3 attempts | plus offset, | early strobe |
| 3 attempts | plus offset, | late strobe |
| 3 attempts | minus offset | nominal strobe |
| 3 attempts | minus offset | early strobe |
| 3 attempts | minus offset | late strobe |

When an error cannot be corrected by this procedure, it shall be considered a permanent error.

### 5.4 Diagnostic Aids

### 5.4.1 Fault Indicator

The following illegal conditions shall light the fault indicators:
(a) DC Voltages unsafe - below normal voltage from the positive or negative power supply
(b) Head Select Fault
(c) Write fault
(d) Offset fault
(e) Read Gate and

Write Gate active simultaneously.
(f) Read or Write while Off-Cylinder
(g) Write Protect - Write attempt with Write Protect fault

- i.e., Read or Write with more than one amplifier head selected, or no amplifier head selected
- Low (or absence of) write current or absence of write data
- Write with offset active activated
(h) Write Current On but no write gate
(a)




### 6.3.1.1 Write Fault Indicator:

This light shall indicate that a write fault has occurred.

### 6.3.1.2 Head Select Fault Indicator:

This light shall indicate that a Multiple Head Select fault has occurred.

### 6.3.1.3 Write and Read Fault Indicator:

This light shall indicate that write and read conditions existed simultaneously.
6.3.1.4 Write or Read and Off Cy1. Fault Indicator:

This light shall indicate that write or read conditions existed during a seek operation (off cylinder).

### 6.3.1.5 Voltage Fault Indicator:

This light shall indicate that a below normal voltage had existed.
6.3.1.6 Fault Clear Switch:

This switch shall Master Clear all fault indicators and the associated fault flip-flops, provided such fault no longer exists.

7.5 Vibration and Shock:

Equipment Operational:
Equipment, as normally installed and positioned, shall meet the full specified performance while subject to the following conditions injected from the floor in a vertical direction.
a Continuous vibration as indicated in Figure 5, "Operating" Curve A.
b Intermittent shocks of up to 2 g and not exceeding 10 ms in duration. The time between consecutive shocks shall not be less than 0.5 seconds.

Equipment Non-operational (In transit - as packaged for shipment):
Equipment in its normal upright position, shall withstand the following conditions of vibration and shock injected from the floor in the three major mutually perpendicular axes:
a Continuous vibration, as shown in Figure 5, "Non-operating" Curve C.
b Shocks of up to 5 g , and not exceeding 10 ms in duration. The time between consecutive shocks shall not be less than 5 seconds.
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FIGURE 5 VIBRATION LEVELS


The folliwing specifications shall be met with the equipment operating and under conditions which cause even and steady noise with short iterations and devoid of discontinuity, so that consistent measurements can be made. Measurements shall be made on all points suggested in here and in ISO recommendations 495 and 1680.

### 7.7.1 Sound Leve1 A

These measurements shall be made both in slow and impulse mode using sound level meter (with "A" weighing network) complying with the specifications of the IEC (Integrated Equip. Components) Publication No. 123 "Sound Level Meters", or No. 179 "Precision Sound Level Meters'".

The Sound Pressure level dba shall not exceed 80 dbA when measured by above sound level meters set for the response. When measured by impulse sound-level meters, dbA shall not exceed at any point by more than 5 db above slow response measurement curve.

### 7.7.2 Sound Level A -Operator's Position

This specification shall be for these situations where a diskdrive will be close to an operator's station. Sound level and the Impulse Sound level measurement shall be taken at a distance of 0.50 m ( 20 in. ) from the work-place, and at a height of 1.20 m ( 47.25 in.) by methods suggested above and shall meet the specifications mentioned above.

### 7.7.3 Sound Leve1 NC - curves

Sound pressure level criterion curves for the $1 / 3$ rd octave band with the center frequencies of $10,12.5,16,20,25,31.5,40,50$, $63,80,100,125,160,200,250,320,400,500 \mathrm{~Hz}$ etc. shall be plotted and shall meet the NC60 curve specified per ISO/TC43/ N428 specification. These measurements could be taken using Octave Band Noise Analyzer such $a=$ GENRAD1564A.
8.0 PHYSICAL SPECIFICATIONS AND INSTALLATIONS

### 8.1 Physical Specifications

The following dimensions and weights do not include the shipping container or packaging.

### 8.1.1 Single Spindle

| Height | 36.2 | inches | $(920 \mathrm{~mm})$ |
| :--- | ---: | :--- | :--- |
| Depth | 36.0 | inches | $(914 \mathrm{~mm})$ |
| Width | 22.0 | inches | $(559 \mathrm{~mm})$ |
| Weight | 340.0 | lbs. | $(154.5 \mathrm{KG})$ |
| Floor Load @ | 85.0 | lbs. | $(38.6 \mathrm{KG})$ |

8.1.2 Dual Spindle

| Height | 36.2 | inches | $(920 \mathrm{~mm})$ |
| :--- | ---: | :--- | :--- |
| Depth | 36.0 | inches | $(914 \mathrm{~mm})$ |
| Width | 22.0 | inches | $(559 \mathrm{~mm})$ |
| Weight | 567.0 | lbs. | $(257.5 \mathrm{KG})$ |
| Floor Load @ | 141.75 | lbs. | $(64.4 \mathrm{KG})$ |
| each rest-pad |  |  |  |

8.2 Installation

The required connections to the device shall be power (dependent upon options selected), signal cables and a system ground, consistent with normal peripheral equipment grounding practices. The physical requirements dictate adequate clearances for maintenance and air intake/exhaust.
8.2.1 Power Requirements
8.2.1. A AC Power

The primary voltage and current requirements are shown below:
Primary Voltage Requirements:

| VOLTAGE (VAC) | TOLERANCE (VAC) | FREQUENCY (Hz) | TOLERANCE ( Hz ) |
| :---: | :---: | :---: | :---: |
| 100 | +10,-10 | 60 | +0.6,-1.2 |
| 120 | + 8,-18 | 60 | +0.6,-1.0 |
| 100 | +10,-10 | 50 | +0.5,-1.0 |
| 220 | +15,-25 | 50 | +0.5,-1.0 |
| 240 | +17,-27 | 50 | +0.5,-1.0 |






[^0]:    * GATED BY UNIT SELECTED

