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Am95/3310 Communication I/O Expansion Board

User's Manual

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PREFACE

This manual provides general information, an installation and interface guide, programming information, principles of operation, and service information for the Advanced Micro Computers Am95/3310 Communication I/O Expansion Board. Additional information can be obtained from the following documents:

- Bell System Technical Reference
  - Data Auxiliary Set 801C (Automatic Calling Unit)
  - Interface Specification (PUB41601)
- Intel Multibus† Specification (9800683)
- The 8080A/9080A MOS Microprocessor Handbook
- Using the 8259A Programmable Interrupt Controller (AP-59)

In this manual both active-high (positive true) and active-low (negative true) signals appear in the text. To eliminate confusion and simplify presentation, the following convention is adhered to: whenever a signal is active-low (negative true), its mnemonic is followed by an asterisk (*) (i.e., MEMR* denotes an active-low signal). For a signal that is active-high, the asterisk is omitted (i.e., IORW denotes an active-high signal).

†Multibus is a registered trademark of Intel Corporation.

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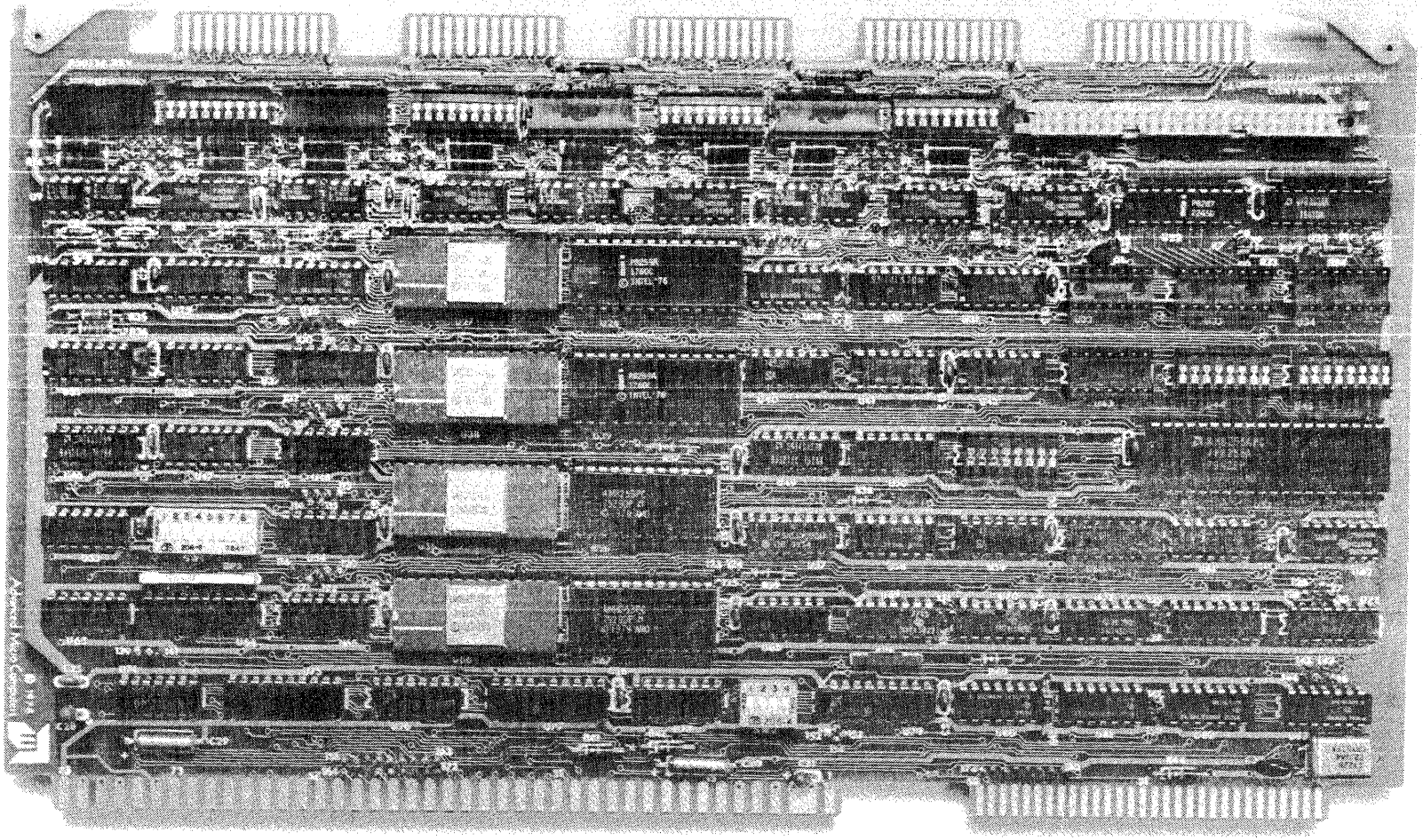


CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The Am95/3310 Communication I/O Expansion Board is designed to enhance AMC's MonoBoard products and Multibus compatible 8-bit and 16-bit microcomputer systems by providing an expansion of system serial and parallel communications, and a capability of being directly compatible with Bell 801 Automatic Calling Unit (ACU). The Am95/3310 programmable synchronous and asynchronous communications interface includes four serial I/O ports with jumper-selectable RS232C or current-loop buffering with optional Opto-isolation for TTY drivers/receivers, and independently programmable baud rate generator/timers. The programmable parallel interface has 24 software configurable parallel lines for supporting Bell 801 ACU or parallel I/O ports; sockets are provided for interchangeable line drivers/receivers, or terminators.

The 95/3310 interfaces directly to the Multibus and conforms with Multibus specifications in every respect. Major features are:

- Four Serial I/O Ports, RS232C Buffered
- 20 MA Current-Loop Interface for the four serial I/O ports (jumper block selectable) with sockets for Opto-isolators.
- 24 Line Parallel I/O Channel, RS232C or TTL Buffered
- Multibus Compatible Interface
- Directly Compatible with Bell 801 ACU
- 16 Interrupt Request Lines with Programmable Priority Processing Algorithm
- Sockets for interchangeable Line Drivers/Receivers in the Parallel Interface (8303 Octal Tri-State Inverting Bidirectional Transceivers or 8304 Octal Tri-State Bidirectional Transceivers)
- Six independently Programmable Baud-Rate Generators/ Timers
- 8 or 16-bit Multibus I/O Address Capability
- Switch-Selectable I/O Address Base Assignment

1-2. PHYSICAL DESCRIPTION

The Am95/3310 circuit components are mounted on a two layer printed circuit board as shown in Figure 1-1. Seven edge connectors and one flat cable connector provide bus and peripheral interfacing. Edge connector P1 interfaces to the Multibus which provides addresses, control signals, data transfers, and power requirements for board operation. P1 pin assignments are listed in table 2-1. Connector P2 is unassigned. Connectors P3 through P6 interface to the serial I/O ports (P3 interfaces Port 0, P4 interfaces Port 1, etc). Connectors P3

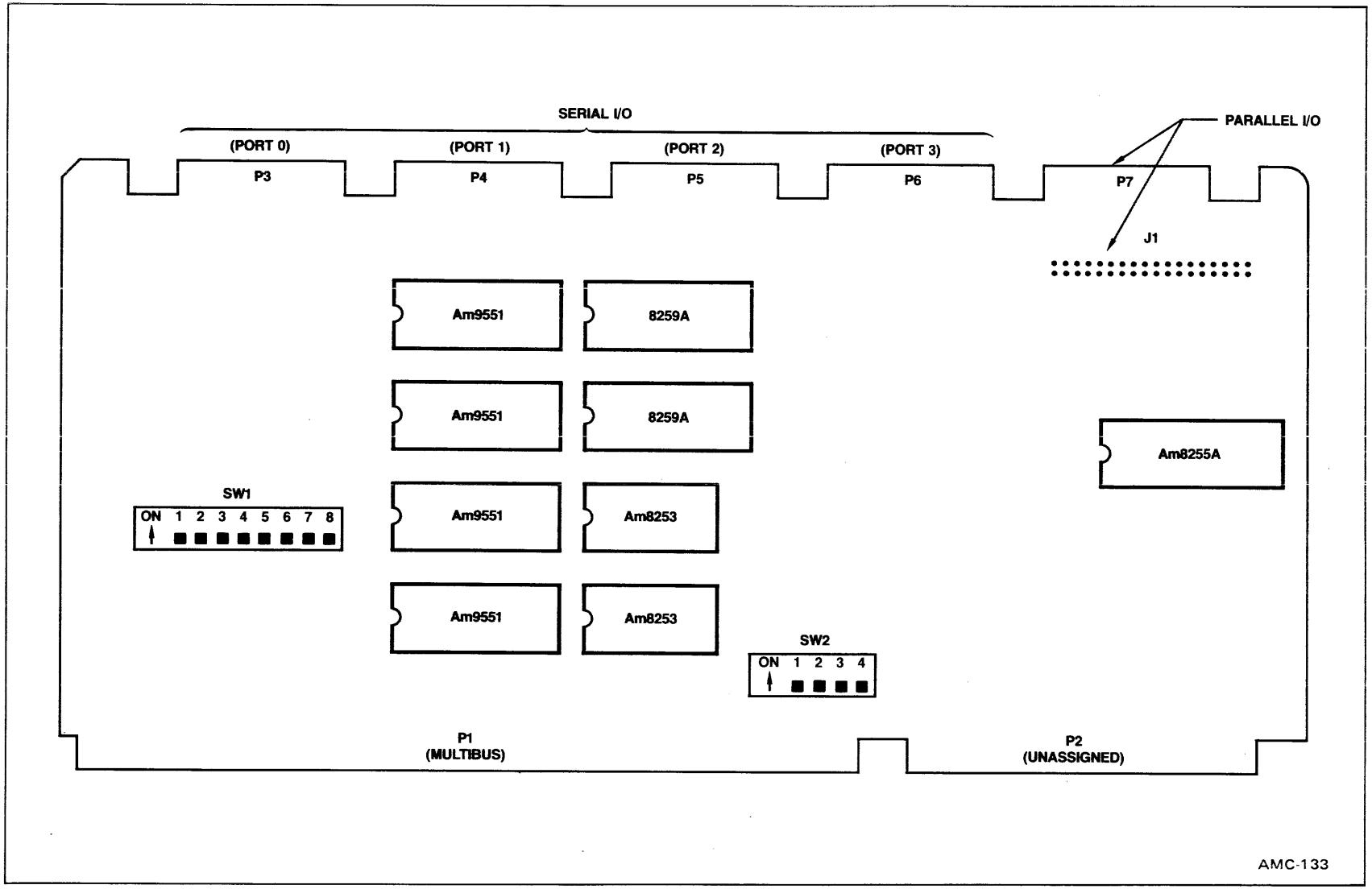


Figure 1-1. Am95/3310 Physical Block Diagram

through P6 pin assignments and signal names are listed in table 2-2. Connectors P7 and J1 interface to the parallel I/O ports. Connectors P7 and J1 pin assignments are listed in tables 2-3 and 2-4, respectively.

The Am95/3310 hardware consists of one Am8255A Programmable Peripheral Interface, two 8253 Programmable Interval Timers, two 8259A Universal Interrupt Controllers, four Am9551 Universal Synchronous/Asynchronous Receiver Transmitters, associated support circuitry, and Multibus interface circuitry.

On-board switches and jumpers establish address boundary, interrupt level, interval timer configuration, serial I/O clock selection, RS232C or current-loop operation, and parallel I/O port configuration.

1-3. FUNCTIONAL DESCRIPTION

The Am95/3310 communicates with 8-bit or 16-bit CPUs via the Multibus (system-bus). Addresses on the system-bus are monitored for an address that matches the on-board switch settings; only an address that matches is decoded into board functions and chip-selects. Using I/O commands, a CPU can initialize, read from, or write to the Am95/3310. In return, the Am95/3310 supplies status and data.

Each of the serial I/O ports is RS232C plug compatible and controlled by an Am9551 USART (Universal Synchronous/Asynchronous Receiver/Transmitter). All of the serial I/O ports are wired for RS232 Data Communication Equipment (DCE) protocol. The USARTs can be individually programmed for both synchronous and asynchronous serial data transmission formats.

In the synchronous mode the following are programmable:

- Character length
- Sync character (or characters)
- Parity

In the asynchronous mode the following are programmable:

- Character length
- Baud rate factor (clock divide ratios of 1, 16, or 64)
- Stop bits
- Parity

In both the synchronous and asynchronous modes, each serial I/O port features half or full-duplex, double-buffered transmit and receive capability. In addition, USART error detection circuits can check for parity, overrun, and framing errors. The USART transmit and receive clock rates are derived from six independently programmable Baud rate/time generators.

Each serial I/O port supports input and output that require isolated current-loops. The Am95/3310 can supply 20mA to an external loop.

The parallel interface has 24 I/O lines which can be jumpered for either TTL or RS232C compatibility. It can be jumpered to interface automatic calling units similar to Bell 801C or for any general purpose or auxiliary functions.

Two Am8253 Programmable Interval Timer (PIT) chips provide six time/rate generators that can be independently programmed, to generate baud rate clocking for each USART. As shipped, four of the timers are used as baud rate clocks; the remaining two can be used for miscellaneous functions such as transmit and receive clocks or real-time interrupt.

Two 8259A Universal Interrupt Controllers (PICs) manage up to 16 maskable interrupt request inputs, resolve priorities, and provide bus vectoring information for each interrupt. The PICs are set-up by the initialization routine to call the service routines at the proper location, and service the interrupts on either a fixed or rotating basis in either an interrupt or polled mode, allowing flexibility to establish interrupt service priorities. When an Am8259A receives an interrupt request, an interrupt output is issued onto the multibus. When the interrupt is acknowledged, the master Am8259A on the CPU board issues the CALL CODE and the interrupting slave Am8259A issues the appropriate 16-bit branching address. After an interrupt has been serviced, the software resets the corresponding bit-flag.

1-4. SPECIFICATIONS

Physical, environmental, and technical specifications for the Am95/3310 board are listed in table 1-1.

TABLE 1-1. SPECIFICATIONS

PHYSICAL

Board Dimensions:

WIDTH	30.48 cm (12 inches)
DEPTH	17.15 cm (6.75 inches)
THICKNESS	1.50 cm (0.60 inches)

ENVIRONMENTAL

Operating Temperature:	0°C to 55°C
Relative Humidity:	Up to 90% without condensation
Storage Temperature:	-40°C to 75°C

POWER

VOLTAGE	TYPICAL CURRENT	MAXIMUM CURRENT
V_{CC} = +5V	1.35A	1.90A
V_{DD} = +12V	0.19A	0.27A
V_{AA} = -12V	0.18A	0.25A

TECHNICAL

Interface:	RS232C or 20mA Current Loop or TTL
Number of Ports:	4 Serial and 3 Parallel
Transmission Type:	Synchronous or Asynchronous
Transmission Mode:	Full or Half-Duplex
Asynchronous Format:	5 to 8-bit Characters Break Character Generation 1, 1.5, or 2 Stop-bits False Start-bit Detector
Synchronous Format:	5 to 8-bit Characters 1 or 2 Sync Characters Automatic Sync Insertion
Serial Baud Rate:	Programmable
Serial I/O Address:	See table 3-1
Parallel I/O Address:	See table 3-1
Interrupt Controller Address:	See table 3-1
Programmable Interval Timers Addresses:	See table 3-1

TABLE 1-1. SPECIFICATIONS (Cont.)

TECHNICAL (continued):

I/O Addressing: The USART, Interval Timer, Interrupt Controller, and Parallel Interface registers are configured as a block of 24 I/O address locations. The location of this block is jumper-selectable to begin at any 32-byte I/O address boundary (i.e. 00H, 20H, 40H, ... E0H).

I/O Access Time: 375 nanoseconds, typical

Compatible Connectors/Cable:

INTERFACE	NO. OF PINS	CENTERS (INCHES)	CONNECTOR CONNECTOR	PART NUMBER
MULTIBUS	86	0.156	Solder	VPB01E43D00A1 MP-01560430BW4 2VH43AV5
Serial and 801C Edge Connectors	26	0.1	Flat Crimp Wirewrap	609-2615 88106-1 3462-0001 Crimp SD6726 Series H311113
Parallel I/O Flat Cable Connector	50	0.1	----------	3M Δ3496

Sample Baud Rate:

FREQUENCY[1] (kHz, SOFTWARE SELECTABLE)	BAUD RATE (Hz)[2]		
	SYNCHRONOUS	ASYNCHRONOUS	
		÷ 16	÷ 64
153.60	----------	9600	2400
76.80	----------	4800	1200
38.40	38400	2400	600
19.20	19200	1200	300
9.60	9600	600	150
4.80	4800	300	75
6.98	6980	-----	110

NOTES: 1. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

2. Baud rates shown here are only a sample subset of possible software programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as frequency divider).

TABLE 1-1. SPECIFICATIONS (Cont.)

INTERVAL TIMER AND BAUD RATE GENERATOR

Input Frequency: 1.2288 MHz ±0.1% for 8253 PIT input; 0.814 microsecond period, nominal.

Output Frequencies:

FUNCTION	SINGLE TIMER		DUAL TIMERS (TWO TIMERS CASCADED)	
	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
Real-Time Interrupt Interval	1.63 micro seconds	53.3 milli seconds	3.26 micro seconds	58.22 minutes
Rate Generator (Frequency)	18.76 Hz	613.4 kHz	0.00029 Hz	306.7 kHz

INTERFACE COMPATIBILITY

Serial I/O: EIA Standard RS232C signals provided and supported:

Carrier Detect	Receive Data
Clear to Send	Ring Indicator
Data Set Ready	Secondary Receive Data
Data Terminal Ready	Secondary Transmit Data
Request to Send	Transmit Clock
Receive Clock	Transmit Data

Parallel I/O: The board has three programmable bidirectional 8-bit I/O ports with TTL drivers and receivers controlled by an 8255A Programmable Peripheral Interface device or optionally can be configured to be Bell 801C compatible with RS232C drivers and receivers.

System Bus: Compatible with Multibus

CHAPTER 2
INSTALLATION AND INTERFACING

2-1. INTRODUCTION

This chapter describes procedures for installing the Am95/3310 Communication Controller. These include unpacking and inspection, power and cooling requirements, bus interface requirements, jumper configurations, current-loop considerations, and device cabling.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

Do not attempt to service a product damaged in shipment, this will void warranty. For any repairs or replacements, contact AMC Customer Service for further instructions. It is also suggested that salvageable shipping cartons and packing materials be saved for future use in the event the product must be shipped.

2-3. POWER REQUIREMENTS

The Am95/3310 requires +5V, +12V, and -12V power supply inputs. The current required from these supplies are listed in table 1-1. Ensure that the power supply has sufficient current to accommodate the Am95/3310 requirements.

2-4. COOLING REQUIREMENTS

The Am95/3310 must have adequate air circulation to prevent a temperature rise above 50°C (131°F).

2-5. BUS INTERFACE REQUIREMENTS

The Am95/3310 has seven edge connectors and one flat cable connector providing bus interfacing. Edge connector P1 (86-pin) pin assignments

are listed in table 2-1. P2 connector is unassigned. P3 through P6 (26-pin connectors) pin assignments are listed in table 2-2. P7 (26-pin) and J1 (50-pin) pin assignments are listed in table 2-3 and 2-4, respectively.

2-6. USER SELECTABLE OPTIONS

The Am95/3310 is shipped from the factory jumpered as required by the option(s) ordered. The address is set to respond to an 8-bit I/O address starting at 80H. On-board jumpers can be used to select interval timer configuration, two group-type interrupt connections, serial I/O clock selection, RS232C or current-loop operation, and parallel I/O port configuration.

2-7. I/O ADDRESS BASE

The block of 24 I/O addresses is switch-selectable to begin on any 32-byte I/O address boundary within an 8-bit or 16-bit I/O address space. As shipped from the factory, the Am95/3310 is assigned to an 8-bit I/O address space at 80H and will respond to addresses 80H through 97H. If some other address boundary is desired, change SW2 and SW1 settings as listed in table 2-5.

2-8. TRANSFER ACKNOWLEDGE (XACK*)

XACK* is issued 375 nanoseconds, typically, after the receipt of an I/O command. Best case XACK* response is 350 nanoseconds; worst case is 400 nanoseconds. No jumpers are required.

2-9. SYSTEM INTERRUPT CONFIGURATION

The Am95/3310 has an interrupt pad that can connect the two Programmable Interrupt Controllers (PICs) interrupt outputs to any of the eight Multibus interrupt lines, IRQ0* through IRQ7*. As shipped, interrupts from PIC0 and PIC1 are jumpered to IRQ6 and IRQ7, respectively. Table 2-6 lists source and destination jumpers.

TABLE 2-1. P1 PIN ASSIGNMENTS

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND		44	ADRF*	
2	GND	GROUND	45	ADRC*	
3	+5VDC		46	ADRD*	
4	+5VDC		47	ADRA*	
5	+5VDC		48	ADRB*	
6	+5VDC	POWER INPUT	49	ADR8*	
7	+12VDC		50	ADR9*	ADDRESS
8	+12VDC		51	ADR6	BUS
9	------		52	ADR7*	
10	------		53	ADR4*	
11	GND		54	ADR5*	
12	GND	GROUND	55	ADR2*	
13	------		56	ADR3*	
14	INIT*	SYSTEM INITIALIZE	57	ADR0*	
15	------		58	ADR1*	
16	------		59	-------	
17	------		60	-------	
18	------		61	-------	
19	------		62	-------	
20	------		63	-------	
21	IORC*	I/O READ COMMAND	64	-------	
22	IOWC*	I/O WRITE COMMAND	65	-------	
23	XACK*	TRANSFER ACKNOWLEDGE	66	-------	
24			67	DAT6*	
25			68	DAT7*	
26			69	DAT4*	
27			70	DAT5*	DATA
28			71	DAT2*	BUS
29			72	DAT3*	
30			73	DAT0*	
31			74	DAT1*	
32			75	GND	GROUND
33	INTA*	INTERRUPT ACKNOWLEDGE	76	GND	
34					
35	IRQ6*	INTERRUPT REQUEST ON LEVEL 6	77		
36	IRQ7*	INTERRUPT REQUEST ON LEVEL 7	78	-12VDC	
37	IRQ4*	INTERRUPT REQUEST ON LEVEL 4	79	-12VDC	
38	IRQ5*	INTERRUPT REQUEST ON LEVEL 5	80	+5VDC	POWER
39	IRQ2*	INTERRUPT REQUEST ON LEVEL 2	81	+5VDC	INPUT
40	IRQ3*	INTERRUPT REQUEST ON LEVEL 3	82	+5VDC	
41	IRQ0*	INTERRUPT REQUEST ON LEVEL 0	83	+5VDC	
42	IRQ1*	INTERRUPT REQUEST ON LEVEL 1	84	GND	
43	ADRE*	ADDRESS BUS	85	GND	GROUND

All unassigned pins are reserved.

TABLE 2-2. P3-P6 PIN ASSIGNMENTS

PIN	SIGNAL	RS232C PIN NUMBER	PIN	SIGNAL	RS232C PIN NUMBER
1	Chassis GND	1	2	Secondary Transmit Data	14
3	Receive Data	2	4	DCE TxC (Transmit Clock)	15
5	Transmit Data	3	6	Secondary Receive Data/ TTY RDR Control (Note)	16
7	Clear to Send	4	8	DCE RxC (Receive Clock)	17
9	Request to Sent	5	10	Not Used	18
11	Data Terminal Ready	6	12	Not Used	19
13	Signal GND	7	14	Data Set Ready	20
15	Carrier Detect	8	16	TTY RDR Control RET (Note)	21
17	TTY Tx IN (+)	9	18	Ring Indicator	22
19	TTY Rx OUT (-)	10	20	-V	23
21	+V	11	22	DTE TxC/TTY Rx RET	24
23	TTY Rx	12	24	TTY Tx RET	25
25	TTY Tx	13	26	Signal GND	-------

Note: TTY RDR Control, TTY RDR Control RET are only for Serial I/O Port 3 (P6)

TABLE 2-3. P7 PIN ASSIGNMENTS

PIN	SIGNAL	RS232C PIN NUMBER	PIN	SIGNAL	RS232C PIN NUMBER
1	Frame GND	1	2	NB1	14
3	Digit	2	4	NB2	15
5	Abandon Call & Retry	3	6	NB4	16
7	Call Request	4	8	NB8	17
9	Present Next Digit	5	10		18
11	Power Indication	6	12		19
13	Signal GND	7	14		20
15	Auxiliary 3	8	16		21
17		9	18	Data Line Occupied	22
19		10	20		23
21	Auxiliary 4	11	22	Auxiliary 2	24
23	Auxiliary 5	12	24	Auxiliary 1	25
25	Data Set Status	13	26		--

TABLE 2-4. J1 PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	PB7	27	PC5	2		26	
3	PB6	29	PC6	4		28	
5	PB5	31	PC7	6		30	
7	PB4	33	PA7	8		32	
9	PB3	35	PA6	10		34	
11	PB2	37	PA5	12	Signal	36	
13	PB1	39	PA4	14	GND	38	Signal
15	PB0	41	PA3	16		40	GND
17	PC3	43	PA2	18		42	
19	PC2	45	PA1	20		44	
21	PC1	47	PA0	22		46	
23	PC0	49	Unassigned	24		48	
25	PC4					50	

2-10. SERIAL I/O CLOCK SELECTION

The two Am8253 Programmable Interval Timers (PIT0 and PIT1) provide six independent Baud-Rate clocks as follows:

(TIMERS)	(COUNTER)	(OUTPUT)	(DESCRIPTION)
PIT0 (U56)	0	BRCLK0	Baud-rate clock,Port 0.
PIT0 (U56)	1	BRCLK1	Baud-rate clock,Port 1.
PIT0 (U56)	2	BRCLK2	Baud-rate clock,Port 2.
PIT1 (U67)	0	BRCLK3	Baud-rate clock,Port 3.
PIT1 (U67)	1	TIM0	User available Auxiliary clock or timer 0.
PIT1 (U67)	2	TIM1	User available Auxiliary clock or timer 1.

These clocks may be at the same frequency or at different frequencies. Clock signals BRCLK0 through BRCLK3, TIM0, and TIM1 can be programmed for any integer submultiple of the clock frequency range from 18.75 Hz to 614.4 KHz. When the two auxiliary timers are connected in series (jumper 123 connected to 125), the output from PIT 1, timer 1 (TIM0) provides clock input for PIT 1 timer 2 (TIM1). Series connection permits lower clock rates or longer time intervals. Thus, clock frequencies from 0.00029 Hz to 306.7 KHz can be realized.

2-11. SERIAL INTERFACE

The four Am9551 USARTs used in the serial I/O circuits can be independently configured to function with data sets, data processing terminals, or optically-isolated current-loop devices. Each RS232 port is wired to look like an RS232C DCE (Data Communications Equipment). To implement this flexibility, the Am95/3310 is shipped with four universal headers. These headers must be installed in U1, U3, U5, and U7 for the respective channel to operate as a 20mA current-loop interface and in U2, U4, U6, and U8 for the respective channel to operate as an RS232C interface. To use the headers in standard RS232C or current-loop applications, clip the jumper connected between adjacent header pins. (This makes the header function as a straight across jumper.) When the RS232C interface is being used with a terminal that does not return CTS (Clear To Send) in response to RTS (Request To Send), the header must be configured differently. To configure the header so that the RTS signal is turned around as the CTS signal, remove all adjacent inter-pin jumpers except the one between pins 5 and 6. (This configures the header so that all pins including 5 and 6 are connected straight across; in addition, pins 5 and 6 are shorted together.)

TABLE 2-5. I/O ADDRESS BOUNDARY SELECTION

SWITCH SW1 †† (UPPER 8-BIT ADDRESS FOR 16-BIT I/O ADDRESS ONLY)								SWITCH SW2 (8-BIT I/O ADDRESS)			I/O ADDRESS BOUNDARY SELECTED
8	7	6	5	4	3	2	1	4	3	2	X
ADF	ADE	ADD	ADC	ADB	ADA	AD9	AD8	AD7	AD6	AD5	
0	0	0	0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	0	0	0	1	20H
.	.	.	.	.	.	.	.	0	1	0	40H
.	.	.	.	.	.	.	.	0	1	1	60H
.	.	.	.	.	.	.	.	1	0	0†	80H†
.	.	.	.	.	.	.	.	1	0	1	A0H
0	0	0	0	0	0	0	0	1	1	0	C0H
0	0	0	0	0	0	0	0	1	1	1	E0H

† As shipped = 80H where 1 = Open, 0 = Closed

†† These bits are ignored when configured as shipped. To configure the board to respond to a 16-bit address, remove jumper 151-154 and add jumper 151-152.

TABLE 2-6. INTERRUPT SELECTION

SOURCE OF INTERRUPT	JUMPER	JUMPER	DESTINATION
PIC0	162	171	IRQ0
PIC1	180	172	IRQ1
		169	IRQ2
		170	IRQ3
		167	IRQ4
		168	IRQ5
		165	IRQ6
		166	IRQ7

2-12. TRANSMIT/RECEIVE CLOCK SELECTION

Jumpers are used to select the Transmit Clock (TxC) and Receive Clock (RxC) sources. Tables 2-7 and 2-8 list source, jumper and connection, signal name, and destination for TxC and RxC. As shipped, each baud rate generator is connected to it's respective channel's TxC or RxC.

TABLE 2-7. FACTORY INSTALLED TxC and RxC

FROM	JUMPER	JUMPER	TO	SIGNAL	USART
PIT0	120	121	(TxC)	BRCLK0	0
PIT0	120	122	(RxC)	BRCLK0	0
PIT0	113	114	(TxC)	BRCLK1	1
PIT0	113	115	(RxC)	BRCLK1	1
PIT0	104	107	(TxC)	BRCLK2	2
PIT0	104	108	(RxC)	BRCLK2	2
PIT1	97	100	(RxC)	BRCLK3	3
PIT1	97	101	(TxC)	BRCLK3	3

TABLE 2-8. OPTIONAL TxC and RxC SOURCES

USART	OPTIONAL SIGNAL	JUMPER	JUMPER	USART SIGNAL
0	TIM0	117	122	RxC
	TIMI	119	121	TxC
	DCE XMIT CLK, PORT 0	116		
	DCE RCV CLK, PORT 0	118		
1	TIM0	110	115	RxC
	TIMI	112	114	TxC
	DCE XMIT CLK, PORT 1	109		
	DCE RCV CLK, PORT 1	111		
2	TIM0	102	108	RxC
	TIM1	105	107	TxC
	DCE XMIT CLK, PORT 2	103		
	DCE RCV CLK, PORT 2	106		
3	TIM0	99	100	RxC
	TIM1	98	101	TxC
	DCE XMIT CLK, PORT 3	96		
	DCE RCV CLK, PORT 3	95		

2-13. SERIAL I/O PORT CURRENT/LOOP CONFIGURATION

The four serial interface current-loop circuits can be jumpered for use with optically isolated current-loop devices. A block diagram of the basic current-loop circuit shown in figure 2-1 consists of a receive isolator, transmit isolator, and a current source. The current-loop circuitry in each serial I/O interface can be connected in one of two basic configurations: a separate (double) loop shown in figure 2-2 or a series (single) loop shown in figure 2-3. A simplified diagram of the jumpers used to configure port 0 is shown in figure 2-4. The voltage source, current sorce, and loop configuration jumpers are installed in port 0 as follows:

- Voltage Source - to use the internal ±12 V source, connect jumpers between jumper pins 11-12 and 13-14. To use an external ±12 V source, connect jumpers between jumper pins 8-12 and 13-17.

- Current Source - voltage for current source operation can be connected internally or externally. To connect the current source voltage internally, connect a jumper between jumper pins 9-10 and 15-16. To use a voltage source supplied by the external transmitter/receiver, no jumpers should be connected between jumper pins 9-10 and 15-16.

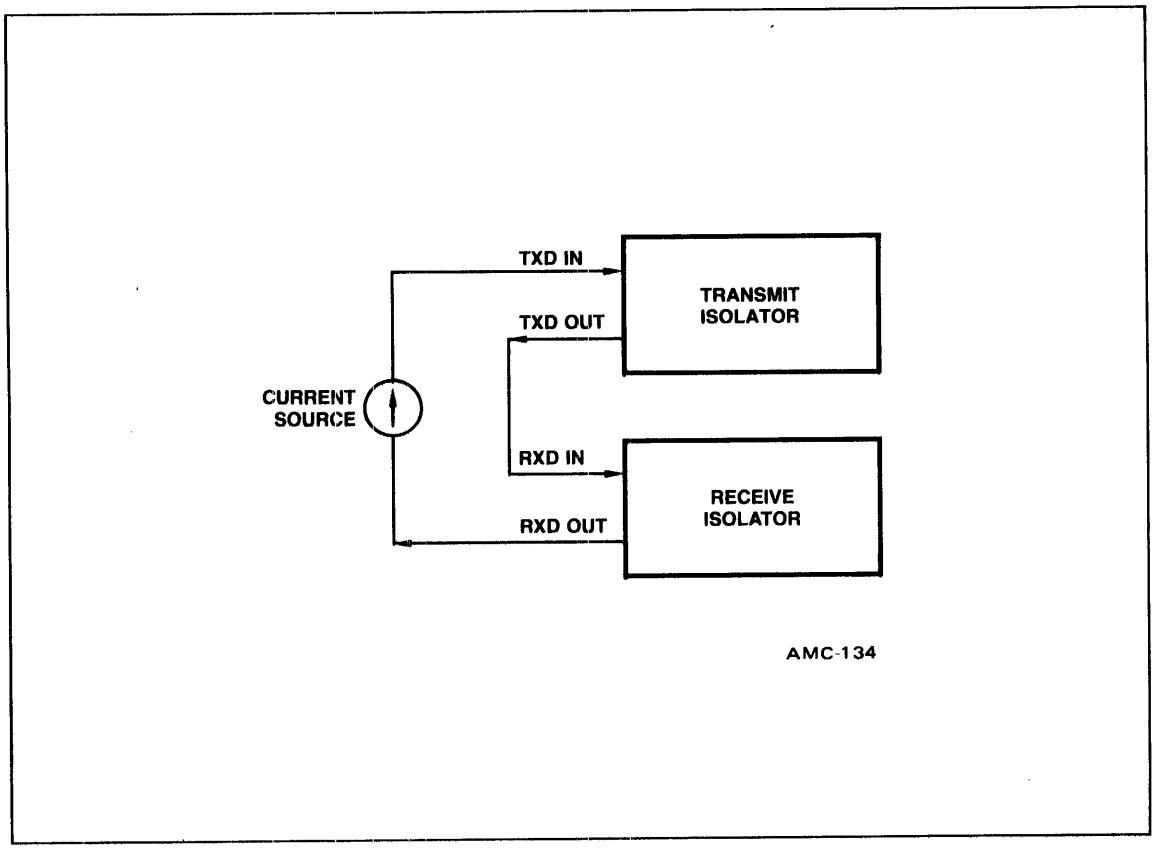


Figure 2-1. Basic Isolator Current-Loop Circuit

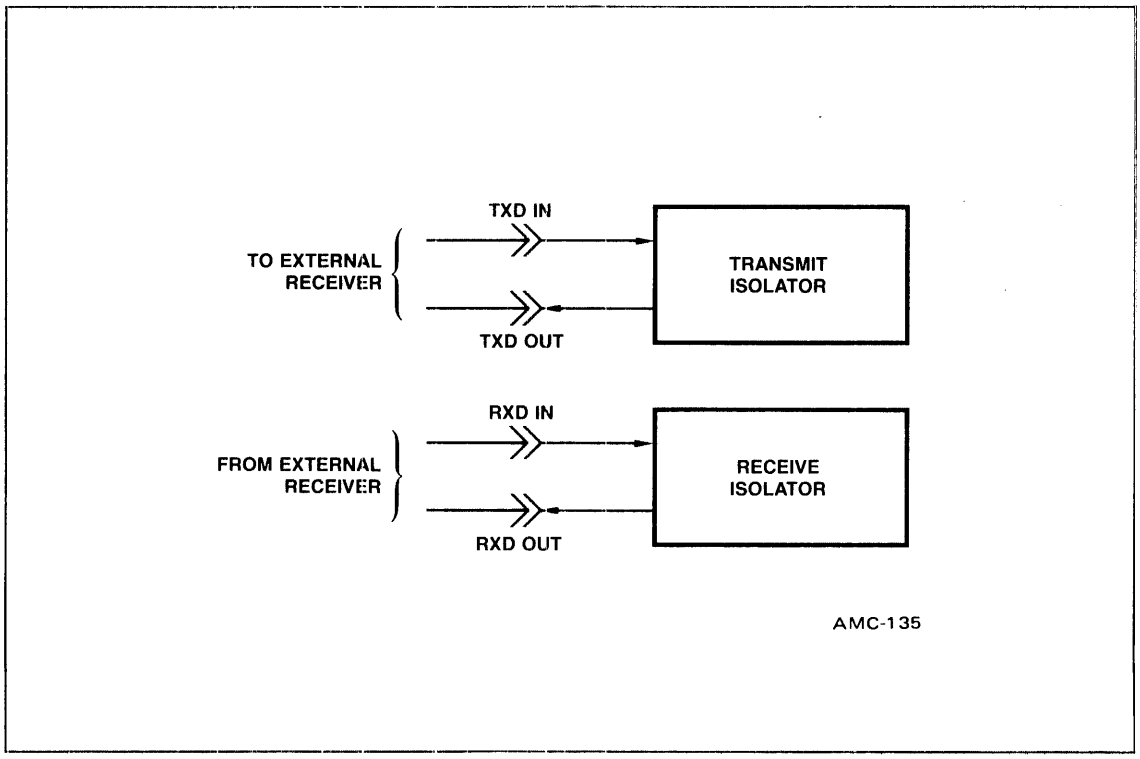


Figure 2-2. Basic Separate (or Double) Loop Circuit for Single Port

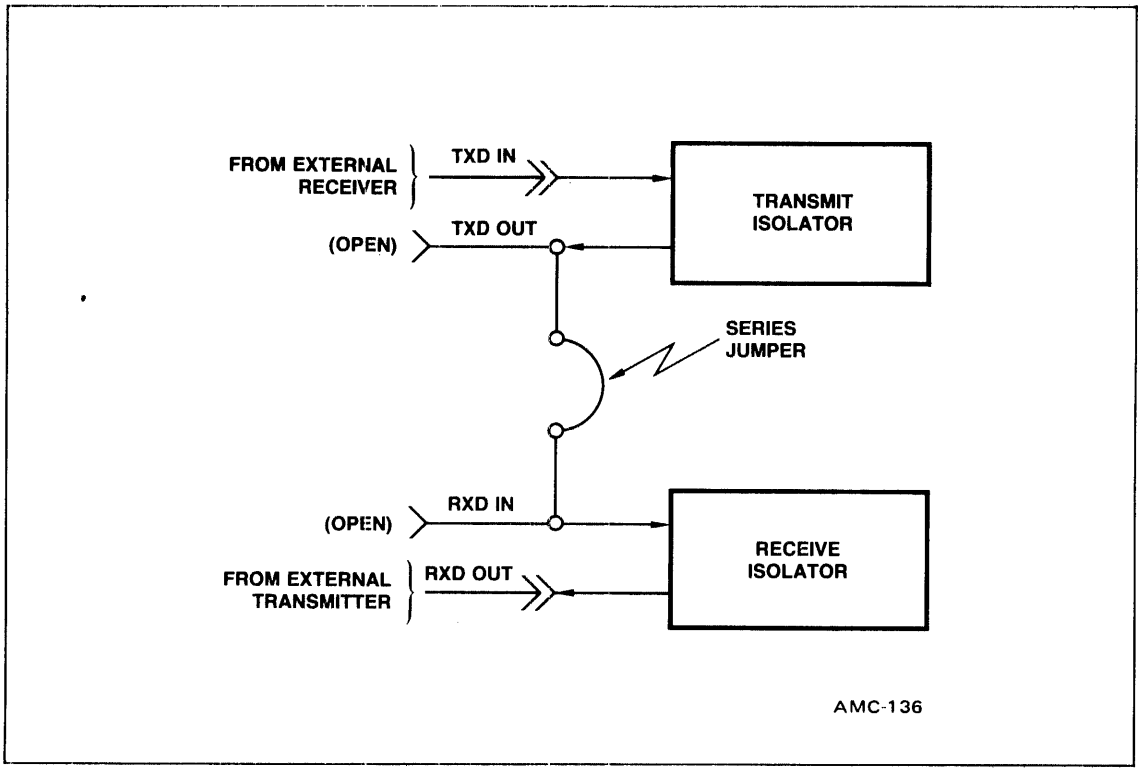


Figure 2-3. Basic Series (or Single) Loop Circuit for Single Port

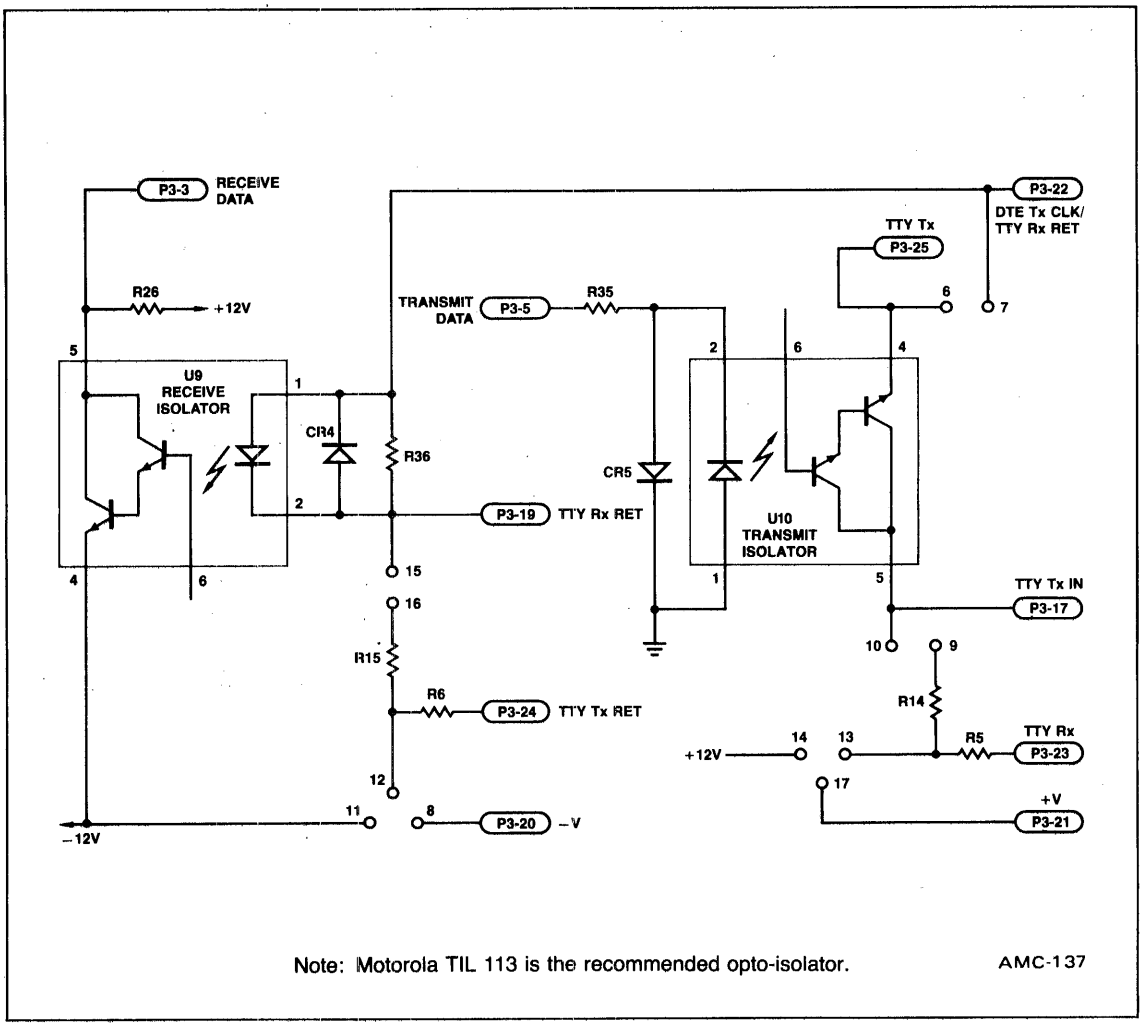


Figure 2-4. Simplified Current Loop Jumper Circuit for Port 0

- Loop Configuration - a jumper must, or must not, be connected between jumper pins 6 and 7, depending on the current loop configuration being used. Leave jumper open for separate (double) loop and series (single) loop with internal current source configurations. Connect a jumper between jumper pins 6 and 7 for series (single) loop with external current source configurations.

Jumper connections for ports 1, 2, and 3 are the same as for port 0 except for jumper pin numbers. Table 2-9 shows the correspondence between port 0 jumpers and the jumpers for port 1, 2, and 3. The on-board (internal) ±12V supply will provide 20mA (minimum) to a single or double current-loop with one receiver and one transmitter in the external loop. External voltage sources are recommended for single loops with more than one external element in each loop, or for double loops with more than two external element.

TABLE 2-9. CURRENT LOOP JUMPERS

PORT	VOLTAGE SOURCE		INTERNAL CURRENT SOURCE	SINGLE LOOP WITH EXTERNAL CURRENT SOURCE
	INTERNAL	EXTERNAL		
0	13-14 11-12	13-17 8-12	9-10 15-16	6- 7
1	25-26 23-24	25-27 20-24	21-22 28-29	18-19
2	38-39 33-37	40-39 32-37	34-35 36-41	30-31
3	50-51 49-45	51-52 44-45	46-47 48-53	42-43

2-14. PARALLEL INTERFACE CONFIGURATION

An 8255A controls the parallel interface. The parallel interface can be configured as 24 TTL compatible inputs or outputs; Or, it can be configured as 16 RS232C buffered inputs and 8 RS232C buffered outputs. The RS232C buffered lines are compatible with a Bell 801C Automatic Calling Unit. As shipped, the Am95/3310 is configured to support The Bell 801C Automatic Calling Unit.

2-15. TTL BUFFERED I/O

The Am95/3310 is shipped with the parallel port lines configured to support RS232C receiver/drivers. To configure the parallel port lines for TTL receiver/drivers, remove the headers from locations U44, U45, and U51; install the headers in locations U33, U34, and U60. In addition, sockets are provided for driver/receivers for ports PA, PB, and PC. The sockets for ports PA and PB (U23 and U22, respectively) must be loaded with user-supplied 8304 non-inverting 8-bit bidirectional data buffers or 8303B inverting buffers. Port PC (sockets V43 and V32) must be loaded with one of the various 4-bit driver/terminators shown in Table 2-10. As shipped, Ports PA and PB are jumpered for input by the jumpers between 92 and 93 on U23 and between 88 and 89 on U22; PA and PB can be used as outputs when these jumpers are removed. When jumpers are installed between 93 and 94 on U23 and between 89 and 90 on U22, port PC bits PC5 and PC6 control the direction of bidirectional transfers.

2-16. RS232C BUFFERED I/O

The Am95/3310 is shipped from the factory configured with RS232C driver/receivers for the parallel port lines. To support the Bell 801C Automatic Calling Unit. When the board configuration has been modified and RS232C support is desired, remove the headers from locations U33, U34, and U60. Reinstall the headers in locations U44, U45, and U51. Port B lines PB0 through PB4 support PND (Present Next Digit), ACR (Abandon Call; Retry), DLO (Data Line Occupied), DDS (Data Set Status), and PWI (Power Indication) signals from the ACU. Carrier Detect Interrupts (CDINTO though CDINT3) and Ring Indicators (RIO through RI3) are supported with port PA. Port PC bits PCO through PC5 support the ACU number bit lines (NB1, NB2, NB4, and NB8), DPR, and CRQ signals. In addition, three bits of PB can be connected to any of the Secondary Receive Data (SRxDO through SRxD3) from the serial ports, or to auxiliary inputs (AUX1 through AUX3) using jumpers 67 through 73, 75, 78, and 86. Table 2-11 lists jumper connections when configuring PB for RS232C input. Port PC bits PC6 and PC7 can be connected to any of the Secondary Transmit Data lines (STxDO through STxD3) of the serial ports with jumpers listed in table 2-12.

TABLE 2-10. PARALLEL I/O SOCKET DEVICES

DEVICE	CHARACTERISTIC
7438	Driver,I,OC,48mA
7437	Driver,I,48mA
7432	Driver,NI,16mA
7426	Driver,I,OC,16mA
7409	Driver,NI,OC,16mA
7408	Driver,NI,16mA
7403	Driver,I,OC,16mA
7400	Driver,I,16mA
iSBC-901	Terminator,220/330,Intel
BLC-901	Terminator,220/330,National
iSBC-902	Pull-up,1K,Intel
BLC-902	Pull-up,1K,National

NOTE: I=inverting
NI=non-inverting
OC=open collector

TABLE 2-11. PARALLEL INPUT PORT

SOURCE			DESTINATION	
SIGNAL	FROM	JUMPER	JUMPER	TO
SRxD0	P3- 6	67	71	U44-11
SRxD1	P4- 6	69	75	U44-10
SRxD2	P5- 6	68	72	U44- 9
SRxD3	P6- 6	70		
AUX1	P7-24	78		
AUX2	P7-22	86		
AUX3	P7-15	73		

TABLE 2-12. PARALLEL OUTPUT PORT

FROM	VIA JUMPER	TO	SIGNAL NAME	CONNECTOR
U62- 8	84	81	STxD0	P3- 2
U62-11	85	83	STxD1	P4- 2
		79	STxD2	P5- 2
		80	STxD3	P6- 2
		74	AUX4	P7-21
		82	AUX5	P7-23

CHAPTER 3
OPERATION AND PROGRAMMING

3-1. INTRODUCTION

The Am95/3310 Communication Controller includes nine programmable device as follows:

- Four Am9551 Universal Synchronous/Asynchronous Receiver/ Transmitter *USART) chips that control the four serial I/O ports.
- Two 8259A Programmable Interrupt Controller chips (PIC) that control the interrupt functions.
- One Am8255A Programmable Peripheral Interface chip (PPI) that controls the parallel I/O ports.
- Two Am8253 Programmable Interval Timer chips (PIT) that control frequency and timing functions.

3-2. I/O BASE ADDRESS ASSIGNMENT

A CPU communicates with the Am95/3310 through a sequence of I/O Read and I/O Write commands. The I/O addresses used for these commands are relative to an I/O base address that is a multiple of 32. The only consideration to be taken in assigning the I/O address base is to ensure that no two boards in the system share the same block of I/O addresses. The block of 24 I/O addresses is jumper-selectable to begin on any 32-byte I/O address boundary (i.e. 0000H, 0020H, 0040H, etc.) The I/O address base is assigned at the factory as 80H through 97H.

3-3. ADDRESS ASSIGNMENTS

The Am95/3310 is mapped into the CPU address space as 24 I/O addresses shown in table 3-1. The first 8 addresses (80H through 87H) are assigned to the four serial I/O ports 0 through 3. The next four addresses (88H through 8BH) in the sequence are assigned to the interrupt controllers. The parallel ports A, B, and C are assigned addresses 8CH through 8FH. The last 8 addresses (90H through 97H) are assigned to the two programmable interval timers.

TABLE 3-1. I/O ADDRESS ASSIGNMENTS

EDGE CONNECTOR	DEVICE (PORT)	FUNCTION	I/O ADDRESS
P3	USART 0, PORT 0 (CSUSART0*)	Data	80H*
		Control	81H
P4	USART 1, PORT 1 (CSUSART1*)	Data	82H
		Control	83H
P5	USART 2, PORT 2 (CSUSART2*)	Data	84H
		Control	85H
P6	USART 3, PORT 3 (CSUSART3*)	Data	86H
		Control	87H
	PIC 0 (CSUIC0*)	Command	88H
		Data	89H
	PIC 1 (CSUIC1*)	Command	8AH
		Data	8BH
J1/P7	PPI (CSPPI*) (PORT A)	Data	8CH
	(PORT B)	Data	8DH
	(PORT C)	Data	8EH
		Control	8FH
	PIT 0 (CSPIT0*)	BRCLK 0	90H
		BRCLK 1	91H
		BRCLK 2	92H
		Control	93H
	PIT 1 (CSPIT1*)	BRCLK 3	94H
		TIM 0	95H
		TIM 1	96H
		Control	97H

* As shipped BASE ADDRESS = 80H

3-4. Am95/3310 INITIALIZATION

After the Am95/3310 has been installed, use the following steps to initialize the board:

a. Disable system interrupts. For systems based on Am8080/ Am8085 microprocessors, use DI instruction.

b. Initialize 8259A chip.

c. Select baud rate for the four serial I/O ports.

d. Initialize 8253A chips.

e. Initialize USARTs 0 through 3 for serial I/O ports 0 through 3, respectively.

f. Initialize 8259A chips. Set up mode and interrupt mask bits as appropriate.

g. Enable system interrupts. For systems based on Am8080 and Am8085 microprocessors, use EI instruction.

If appropriate subroutines have been written, the initialization procedure consists simply of calling subroutines.

3-5. SERIAL I/O INTERFACE PROGRAMMING

Each of the four serial I/O ports is controlled by an Am9551 USART. The USART converts parallel data to serial data format for half or full-duplex operation. The USART also converts serial input data to parallel data format. Operating modes are selected by a mode instruction and a command instruction word. When reset is activated, it forces the Am9551 into an idle mode in which data is neither transmitted nor received. Following reset, a new set of mode and command words must be output by the CPU to the USARTs before operations can resume. The USARTs should be reset after power is first applied.

3-6. Am9551 ADDRESSING

Each Am9551 uses two consecutive addresses. The lower address is used to read or write data; the upper address is used to write mode and command words and to read the USART status. Refer to table 3-1.

3-7. Am9551 INITIALIZATION

Each Am9551 is initialized as follows:

a. Reset the USART to Mode instruction format by writing a command word with bit 6 (IR) set address 81H, 83H, 85H, or 87H.

b. Write a Mode Control Word to address 81H, 83H, 85H, or 87H.

NOTE

After initialization, always check the status of the TxRDY bit prior to writing data or a new command word to the Am9551. The TxRDY bit must be true to prevent overwriting and subsequent loss of commands or data. The TxRDY is inactive until initialization has been completed.

Once initialized, it is not necessary for a command instruction to precede all data transactions--only those transmissions that require a change in the command instruction.

To change the Mode Control Word, the USART must receive a Reset Command. The next word written to the USART after a Reset Command is assumed to be a Mode Control Word. Similarly, for sync mode, the next word after a Mode Control Word is assumed to be one or two sync characters. All controls words writtten into the USARTs after Mode Control Word, are assumed to be command instructions. An individual USART can be reset by bit 6 in the Command Instruction Word, all four can be reset by a system reset.

3-8. MODE INSTRUCTION WORD

The Mode Instruction Word defines the general characteristics of the USART and must follow a reset operation. Once the Mode Instruction Word has been written, Sync Characters or Command Instruction Words may be inserted. The Mode Instruction Word defines the following:

- Synchronous Mode
  - Character length
  - Parity enable
  - Even/odd parity generation and check
  - External sync detect (not supported by 95/3310)
  - Single or double character sync

- Asynchronous Mode

  - Baud rate (multiplier x1, x16, x64)
  - Character length
  - Parity enable
  - Even/odd parity generation and check
  - Number of stop bits

The mode instruction word formats for synchronous and asynchronous mode are shown in figures 3-1 and 3-2 respectively.

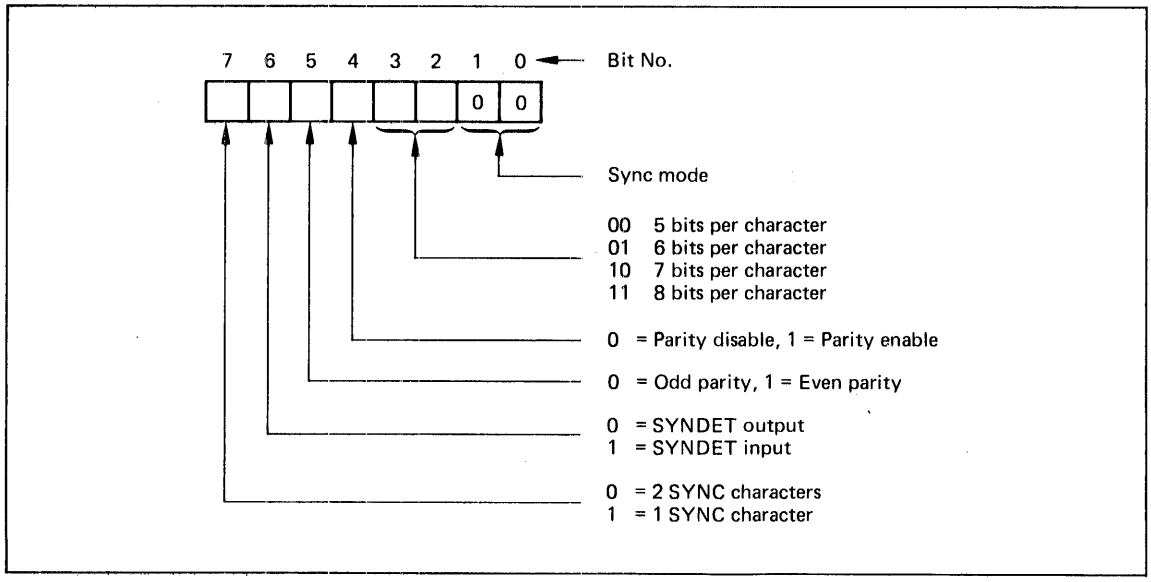


Figure 3-1. Am9551 Synchronous Mode Control Code

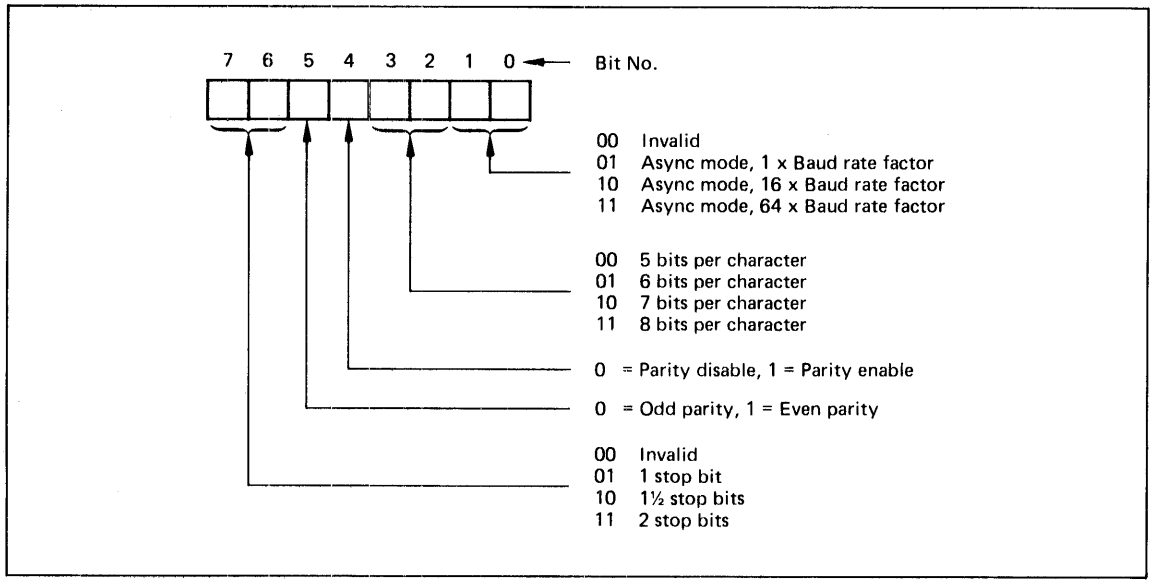


Figure 3-2. Am9551 Asynchronous Mode Control Code

3-9. COMMAND INSTRUCTION WORD FORMAT

The Command Instruction Word shown in figure 3-3 controls the operation of the addressed USART. A Command Instruction Word must follow the mode and/or sync words. Once the Command Instruction Word is written, data can be transmitted or received by USART. It is not necessary for a Command Instruction Word to precede all data transactions; only those transmissions that require a change in the Command Instruction Word.

3-10. Am9551 STATUS READ

The CPU can determine the status of a USART by issuing an I/O Read Command to address 81H, 83H, 85H, or 87H. The format of the status byte is shown in figure 3-4.

The definition of the status bits is as follows:

TxRDY — Transmitter Ready indicates the Am9551 is ready to accept a data character or command.

RxRDY — Receiver Ready indicates the Am9551 has received a character on its serial input and is ready to transfer it to the CPU.

TxE — Transmitter Empty signals the processor that the transmit register is empty. TxE is not supported by the 95/3310.

PE — Parity Error indicates the character stored in the receive character buffer was received with an incorrect number of binary 1 bits.

OE — Overrun flag is set when a byte stored in the receiver character register is over written with a new byte before being transferred to the processor.

FE — Framing Error indicates the asynchronous mode byte stored in the receiver character buffer was received with incorrect character bit format.

SYNDET — When Sync Detect is set for internal sync detect, this bit indicates character sync has been achieved and the Am9551 is ready for data. SYNDET is not supported by the 95/3310.

DSR — Data Set Ready is set by the external Data Set Ready Signal to indicate the communications data set is ready.

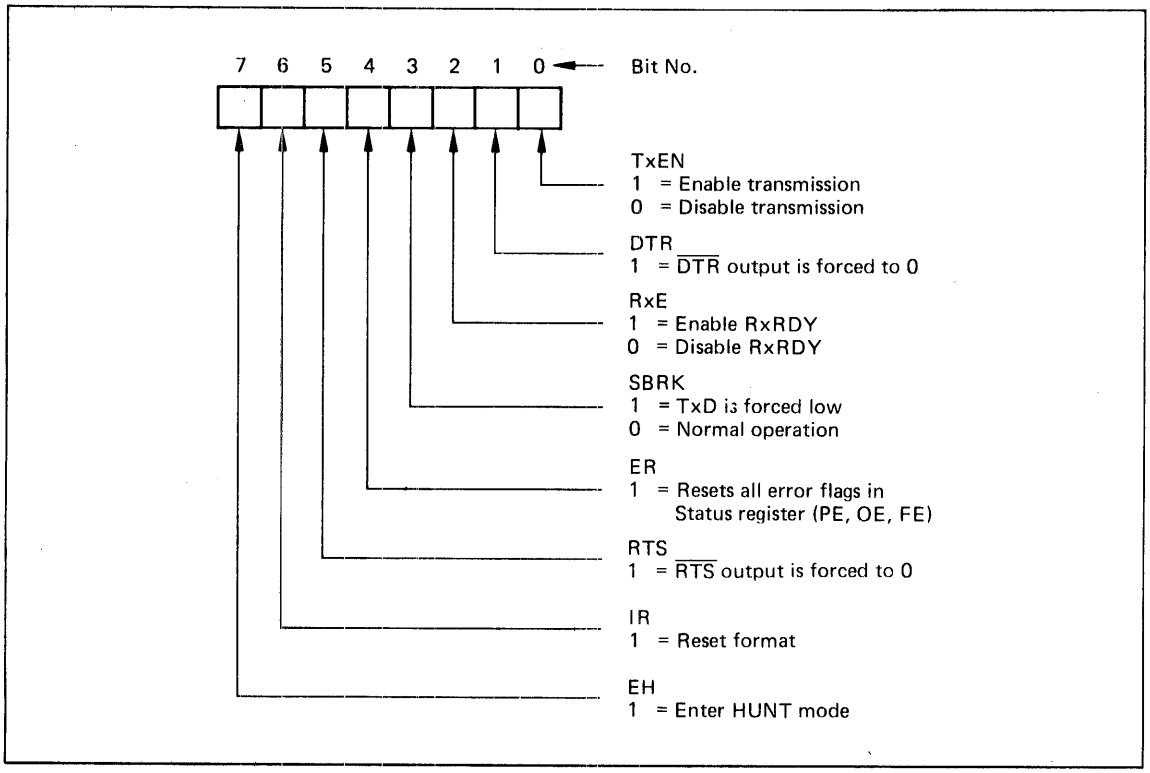


Figure 3-3. Am9551 Command Instruction Word Format

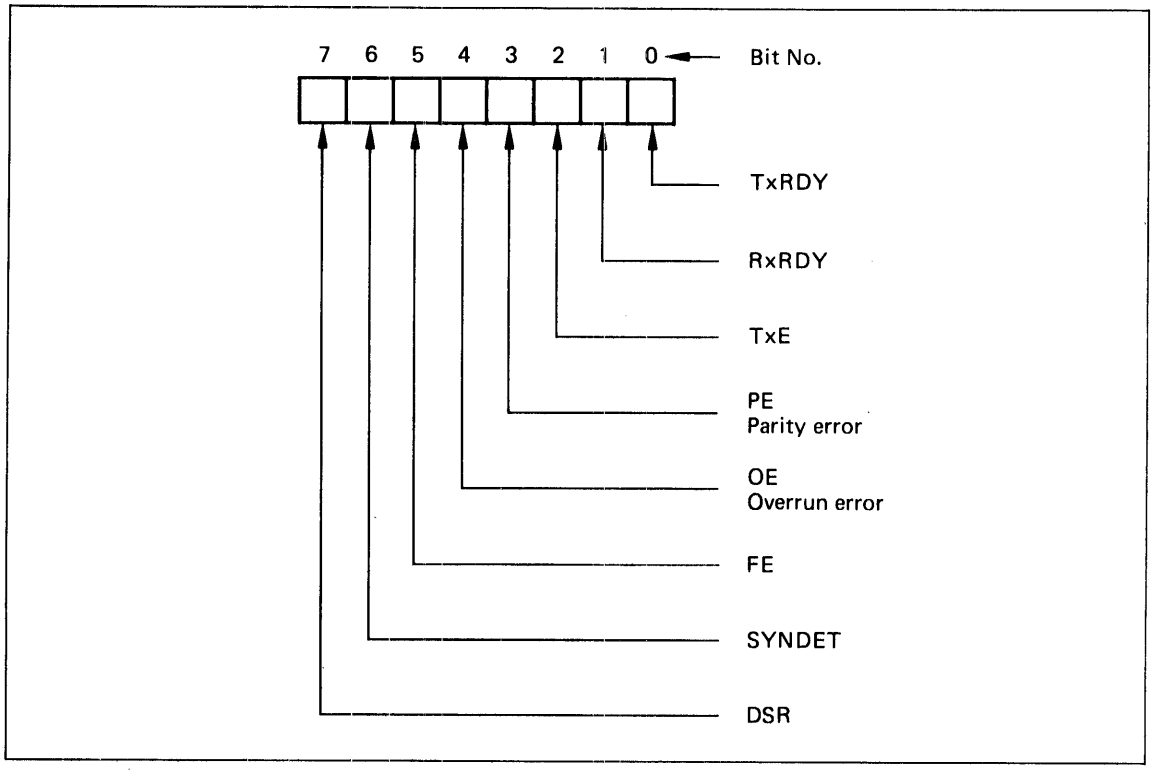


Figure 3-4. Am9551 Status Word Format

3-11. Am9551 DATA INPUT/OUTPUT

A data receive or transmit operations requires a read or write, to the desired USART.

During normal transmit operation, each USART generates a Transmit Ready (TxRDY) signal that indicates that the USART is ready to accept a data character for transmission. TxRDY is automatically reset when a character is loaded into the USART.

Similarly, during normal receive operation, each USART generates a Receive Ready (RxRDY) signal that indicates that a character has been received. RxRDY is automatically reset when a character is read.

The TxRDY and RxRDY outputs of each USART chip are connected to a Programmable Interrupt Controller chip (PIC 0), which resolves priority in case of simultaneous inputs and generates an interrupt for the multibus.

3-12. PARALLEL I/O INTERFACE PROGRAMMING

The PPI provides three 8-bit ports (A, B, and C). Each port can be configured as either input or output, and port C is used to control ports A and B in some modes. The operating modes of the ports are controlled by outputting either an operation control word or a bit set/reset control word. Signals interfaced to the PPI are listed in table 3-2.

Parallel I/O ports B and C can be configured to interface directly with a Bell 801 Automatic Calling Unit (ACU).

3-13. Am8255A INITIALIZATION

The PPI chip is initialized by writing 92H to 8FH. Notice in figure 3-5 that this initializes PPI as follows:

- Operation Control Word Active
- Mode 0 Selected
- Port A Input
- Port B Input
- Port C Output

TABLE 3-2. PPI INTERFACE SIGNALS (FACTORY CONFIGURATION)

PORT B INPUTS		PORT A INPUTS		PORT C OUTPUTS	
BIT	SIGNAL	BIT	SIGNAL	BIT	SIGNAL
0	PND	0	RI0 (PORT 0)	0	NB1
1	ACR	1	RI1 (PORT 1)	1	NB2
2	DLO	2	RI2 (PORT 2)	2	NB4
3	DSS	3	RI3 (PORT 3)	3	NB8
4	PWI	4	CD0 (PORT 0)	4	DPR
5	SRxD0, SRxD1	5	CD1 (PORT 1)	5	CRQ
6	SRxD2, SRxD3	6	CD2 (PORT 2)	6	STxD0,STxD1
7	AUX1,AUX2, or AUX3	7	CD3 (PORT 3)	7	STxD2,STxD3 AUX4, or AUX5

NOTES:

- PND, R1, and CD signals are connected to the interrupt controllers.
- RI AND CD are from serial I/O ports, which do not support these signals.
- Multiple inputs (e.g. bits 5-7 of port B) are jumper wired (See tables 2-11 and 2-12).

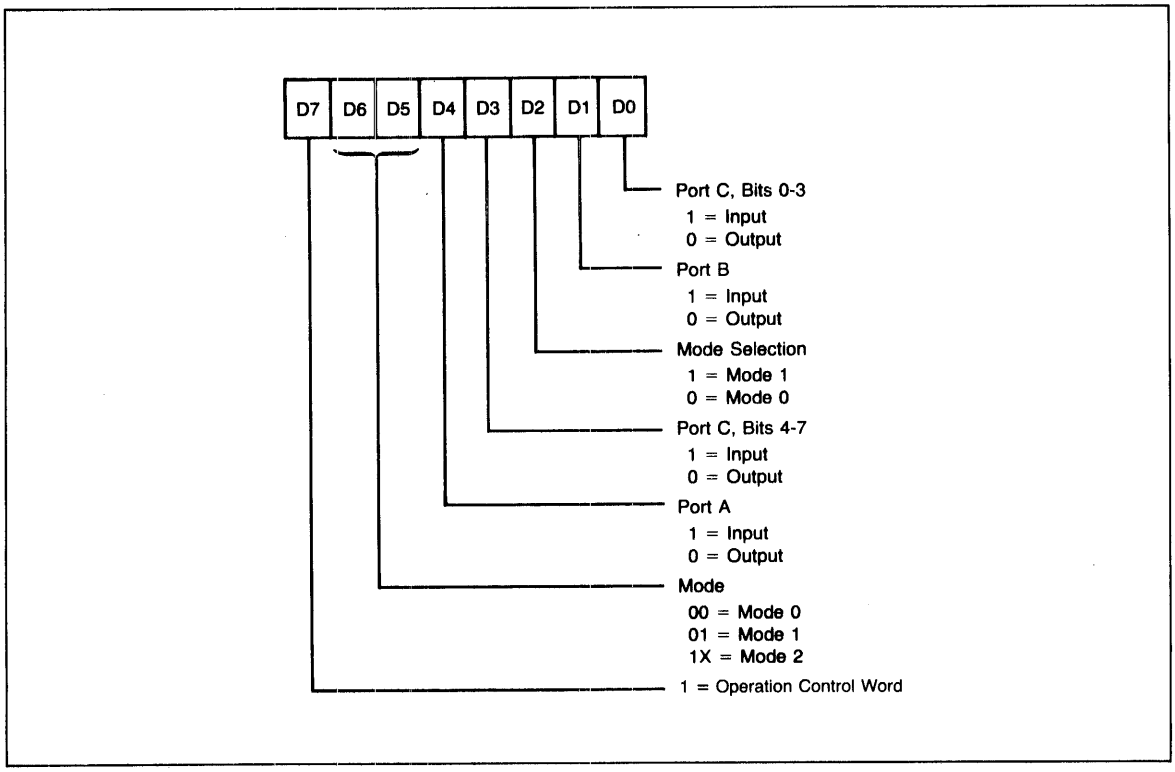


Figure 3-5. Am8255A Operation Control Word Format

3-14. Am8255A ADDRESSING

The PPI uses four consecutive I/O addresses (8CH through 8FH) for transferring data, obtaining Port C status and for device control. Refer to table 3-1 for port addresses and functions.

3-15. Am8255A CONTROL WORD FORMAT

The control word shown in figure 3-5 defines the three operating modes of the ports; Modes 0, which is basic input/output; Mode 1, strobed input/output; and Mode 3, bidirectional bus. The modes for Ports A and B can be separately defined, while port C is divided into two 4-bit ports.

3-16. Am8255A PORT A AND B DATA

Data from Ports A and B are obtained by performing a I/O read of 8CH and 8DH, respectively. Bit definitions for Ports A and B (if Auto Call option is used) are given in Figure 3-6. If Auto Call option is not being used these bits come from parallel port connector J1.

3-17. Am8255A PORT C DATA

Data is written to Port C or a call is placed with the ACU by performing a write to 8EH. Bit definitions for Port C (if Auto Call option is used) are given in figure 3-7. If Auto Call option is not being used these bits come from the parallel port connector J1.

3-18. PROGRAMMABLE INTERVAL TIMER PROGRAMMING

The timing functions on-board are provided by two 8253 Programmable Interval Timers (PITs) driven by a 1.2288 MHz clock signal. Each PIT has three independent 16-bit interval timers. Four of the timers, PIT0 output 0 through 2 and PIT 1, output 0, are connected to the four USARTs transmit and receive clocks BRCLK0 through BRCLK3. The remaining two (PIT1 outputs 1 and 2) can be programmed to generate separate clock signals or real-time interrupt intervals.

A set of control words must be sent by the CPU to initialize each PIT counter with the desired mode. The control words program the mode, loading sequence and selection of binary or BCD counting. Refer to figure 3-8 for PIT control word format.

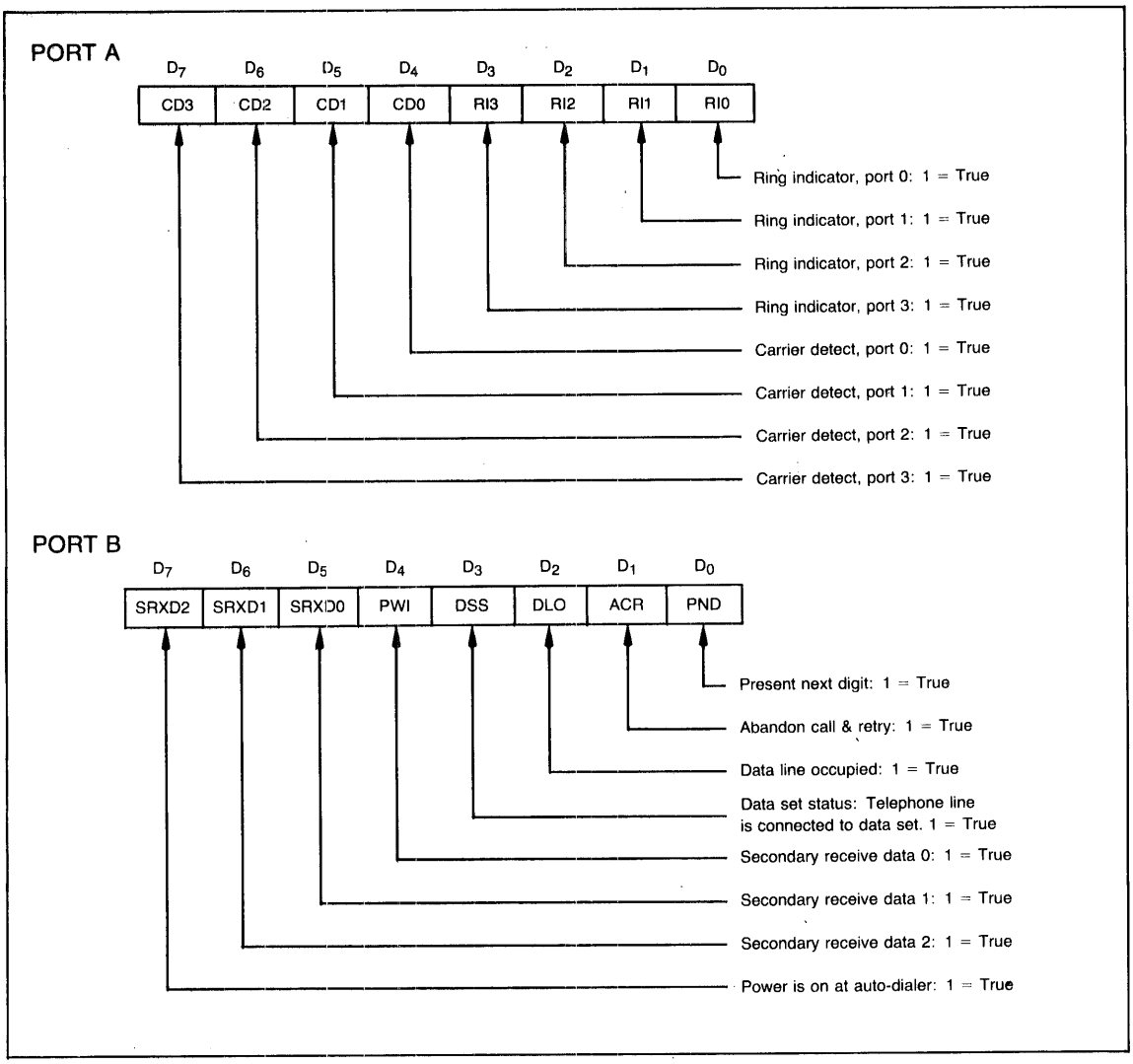


Figure 3-6. PPI Port A and B Bit Definitions

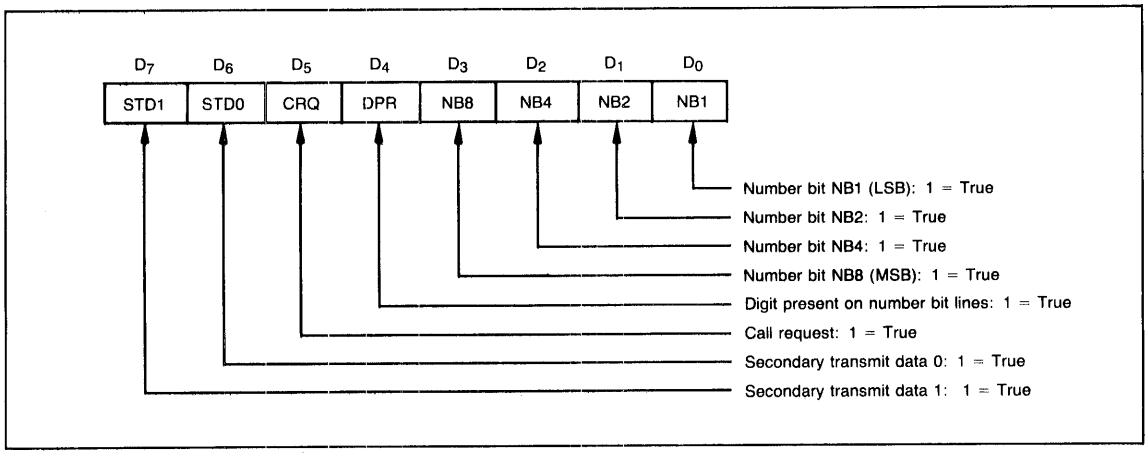


Figure 3-7. PPI Port C Bit Definitions If Auto Call Option is Used

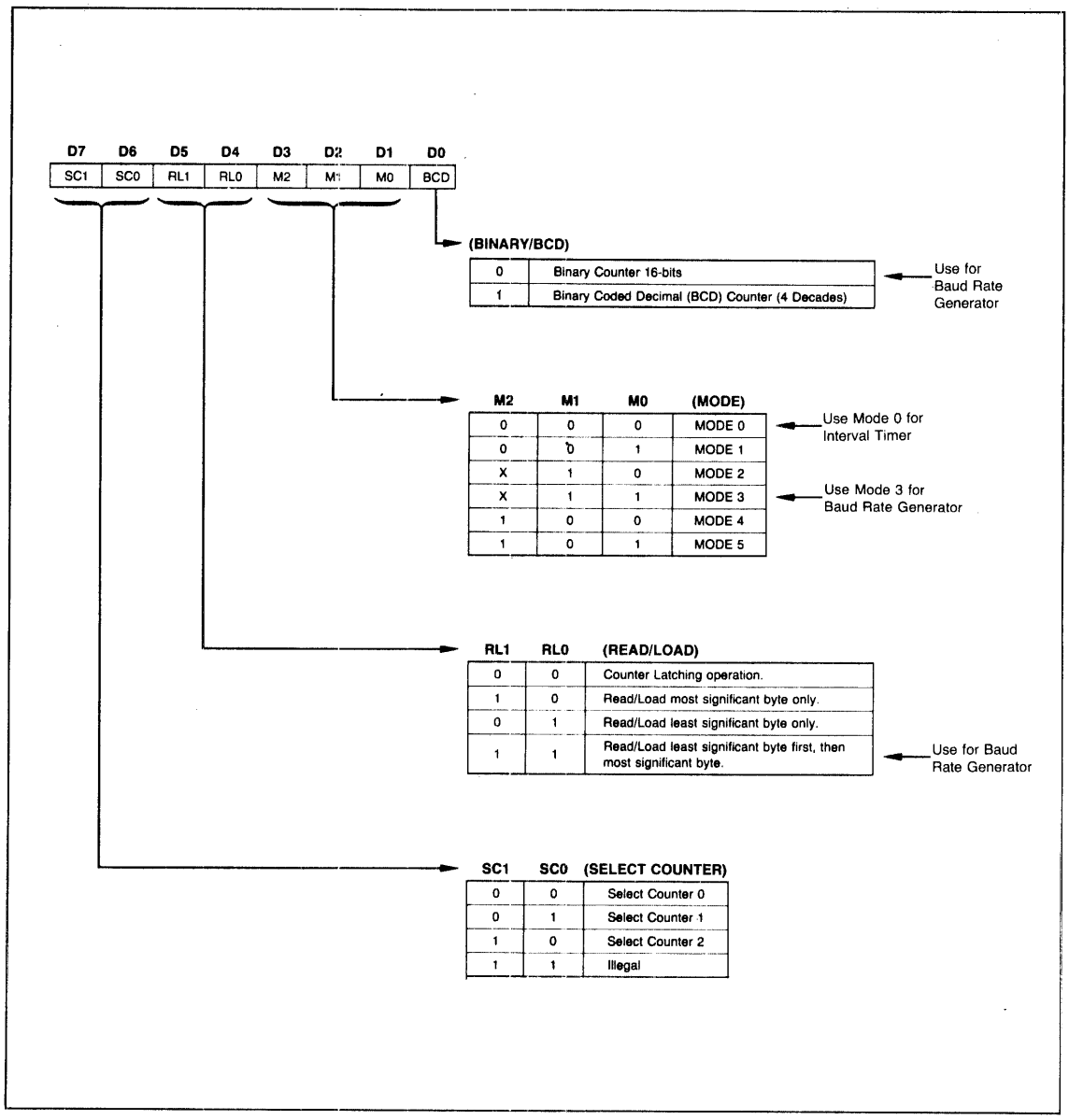


Figure 3-8. PIT Control Word Format

3-19. Am8253 INITIALIZATION

To initialize the Programmable interval timer for baud rate generation, perform the following:

a. Write mode control word for PIT 0 Counter 0 to 93H.

NOTE

All mode control words for PIT 0 are written to 93H, since the mode control word must specify which counter is being programmed. Refer to figure 3-8.

b. Assuming mode control word has selected a 2-byte load, load least-significant byte of count into Counter 0 at 90H.

c. Load most-significant byte of count into Counter 0 at 90H.

NOTE

Be sure to enter the down-count in two bytes ifthe counter was programmed for a two-byte entry in the mode control word. Similarly, enter the down-count value in BCD if the counter was so programmed.

d. Repeat steps a, b, and c for PIT 0 Counters 1 and 2 and for PIT 1 Counter 0. Refer to table 3-1 for control addresses.

3-20. Am8253 OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divide/ratio selection, and interrupt timer counter selection.

3-21. Am8253 Counter Read

For Mode 3 operation, there usually is no requirement to reset or read the counters; however, it is possible to do so at any time. If a count register is reloaded during counting in Mode 3, the new value is reflected immediately following the output transition of the current count. For Mode 0 (interrupt on terminal count), reloading during counting has the following results:

a. Loading first byte stops current count.

b. Loading second byte starts new count.

If desired, it is possible to read the count register during the down count. The recommended procedure is to write a mode control word (shown in figure 3-9) to latch the contents of the count register, this ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

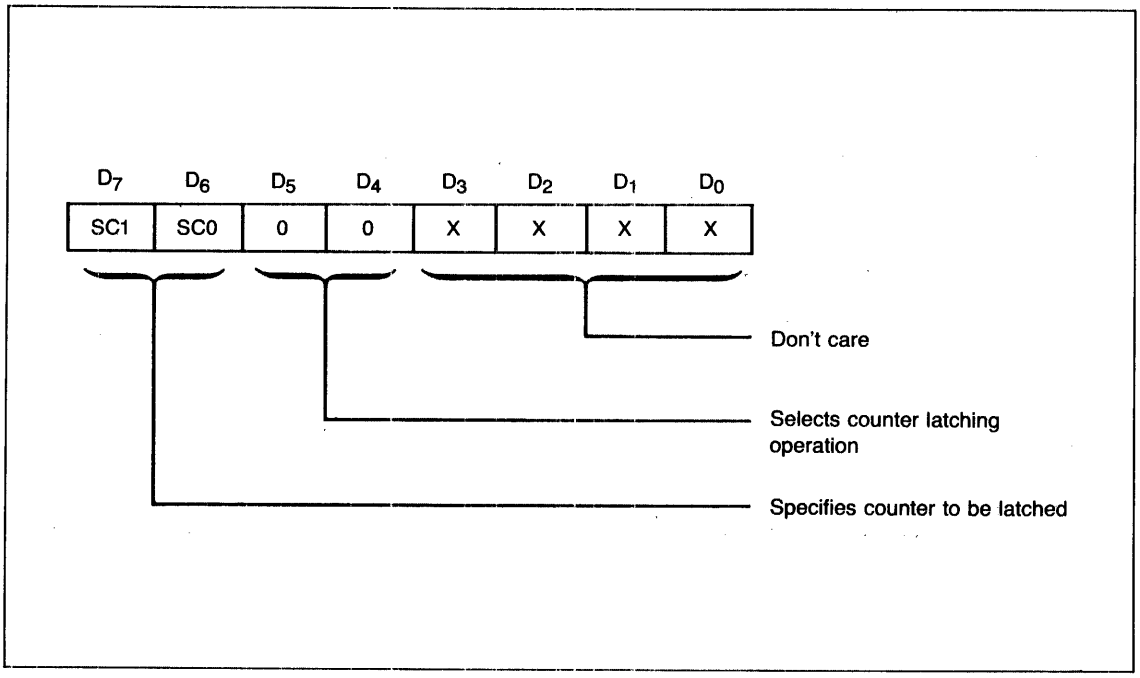


Figure 3-9. PIT Control Word Format for Counter Register Latch

3-22. Am8253 Clock Frequency/Divide Ratio Selection

All of the modes for each counter are programmed by the system software using I/O operation. Each counter must be programmed with a down-count number, or count value N. When count value N is loaded into a PIT counter, it becomes the clock divisor. To derive N for either synchronous or asynchronous operation, use the procedures described in the following paragraphs.

3-23. Synchronous Mode - In the synchronous mode, the TxC and/or RxC rates equal the Baud rate. Therefore, the count value is determined by:

$$N = C/B$$

Where: N is the count value,
B is the desired Baud rate, and
C is 1.2288 MHz, the input clock frequency.

3-24. Asynchronous Mode - In the asynchronous mode, the TxC and/or RxC rates equal the Baud rate times of the following multipliers: X1, X16, or X64. Therefore, the count value is determined by:

N = C/BM

where: N is the count value,
B is the desired Baud rate,
M is the Baud rate multiplier (1, 16, or 64), and
C is 1.2288 MHz, the input clock frequency.

NOTE

During initialization, be sure to load the count value (N) into the appropriate PIT counter and the Baud rate multiplier (M) into the USART.

NOTE

When using 20 mA current loop, maximum baud rate is 110 baud due to the performance of the opto-isolators.

Count values (N) versus rate multiplier (M) for each Baud rate are listed in table 3-3.

TABLE 3-3. PIT COUNT VALUE vs. RATE MULTIPLIER FOR EACH BAUD RATE

BAUD RATE (B)	*COUNT VALUE (N) FOR		
	M = 1	M = 16	M = 64
75	16384	1024	256
110	11171	698	175
150	8192	512	128
300	4096	256	64
600	2048	128	32
1200	1024	64	16
2400	512	32	8
4800	256	16	4
9600	128	8	-
19200	64	4	-
38400	32	2	-

*Count Values (N) assume clock is 1.2288 MHz. Count Values (N) and Rate Multipliers (M) are in decimal.

3-25. Rate Generator/Interval Timer

Table 3-4 shows the maximum and minimum timer intervals when counters 1 and 2 of PIT 1 are connected in parallel or series. These counters generate signals TIM 0 and TIM 1, which can be used either as auxiliary clock counters or to generate interrupt intervals.

TABLE 3-4. PIT RATE GENERATOR FREQUENCIES AND TIMER INTERVALS

FUNCTION	SINGLE TIMER (TIM0 and TIM1 Used independently)		DUAL TIMER (TIM0 AND TIM1 Jumpered In Series)†	
	Minimum	Maximum	Minimum	Maximum
Rate Generator (Frequency)	18.76Hz	613.4 kHz	0.00029Hz	306.7 kHz
Real-Time Interrupt (Interval)	1.63 micro seconds	53.3 milli seconds	3.26 micro seconds	58.22 minute

† Refer to Chapter 2 for Serial I/O clock selection jumpering information.

3-26. Interrupt Timer

To program an interval timer for a terminal count interrupt, program the appropriate PIT for the correct operating mode in the control word. Then load the count value (N), which is derived by:

$$N = TC$$

where: N is the timer counter value,
T is the desired interrupt time interval in seconds, and
C is the input clock frequency (Hz).

Table 3-5 shows the count value (N) required for several time intervals (T) that can be generated for outputs TIM0 and TIM1.

3-27. PROGRAMMABLE INTERRUPT CONTROLLER

The Am95/3310 is designed to be operated in an interrupt driven environment. The two 8259A Programmable Interrupt Controllers (PICs) can be programmed to operate independently or in a slave mode to accept 16 interrupt requests originating in the parallel I/O ports, serial I/O ports, and programmable interval timers. The 8259A PIC selects the highest priority interrupt request and generates a multibus interrupt. When the PIC is programmed as a slave, it will output one or two response bytes, one after the other, onto the system bus.

The key elements of an 8259A are shown in the functional block diagram given as figure 3-10. The priority assignments and algorithms can be changed or reconfigured dynamically at any time. Since the response bytes are programmable, any instruction or vectoring protocol appropriate for the CPU can be used.

TABLE 3-5. PIT TIME INTERVALS vs TIMER COUNTS

T	N*
10 Micro seconds	12
100 micro seconds	123
1 milli second	1229
10 milli seconds	12288
50 milli seconds	61440
*Count Values (N) assume clock is 1.2288 MHz. Count Values (N) are in decimal.	

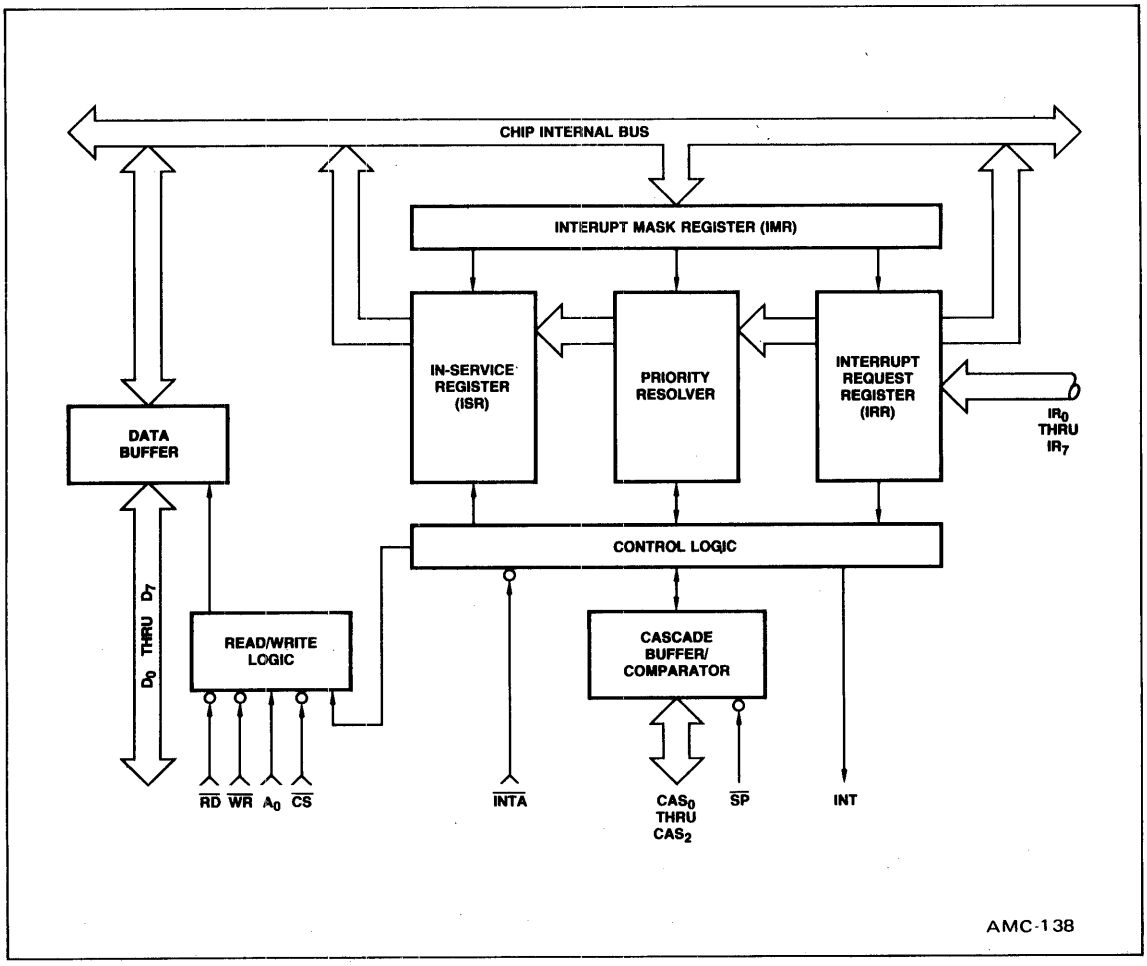


Figure 3-10. 8259A Functional Block Diagram

3-28. 8259A INTERRUPT REQUEST REGISTER

The IRR stores the interrupt level(s) requesting service. A bit is set when the corresponding interrupt request input becomes active and is automatically cleared when it is acknowledged. All bits are cleared by a reset function.

3-29. 8259A IN-SERVICE REGISTER (ISR)

The ISR is used to keep track of a pending interrupt that has been acknowledged and to mask lower priority interrupts. When a bit is set in the ISR, the corresponding IRR bit is cleared. All ISR bits are cleared by a reset function.

3-30. 8259A PRIORITY RESOLVER

The Priority Resolver determines the highest priority unmasked pending request and strobes the corresponding bit in the ISR when the request is acknowledged.

3-31. 8259A INTERRUPT MASK REGISTER (IMR)

The IMR enables or disables the individual interrupt inputs and all eight may be enabled or disabled in parallel. A reset function sets all eight mask bits, disabling all interrupt requests. A mask bit which is set does not disable the IRR, and an interrupt request which arrives while a corresponding mask bit is set will cause an interrupt later when that mask bit is cleared.

3-32. 8259A READ/WRITE LOGIC

The Read/Write Logic contains the Initialization Command Word (ICW) Register and Operation Command Word (OCW) Register which store the various control formats for device operation. It accepts output commands from the CPU and transfers status of the 8259A via data bus.

3-33. 8259A CASCADE BUFFER/COMPARATOR

The Cascade Buffer/Comparator stores the PIC address code which enables the PIC to recognize when it is being addressed for a request for the response bytes. The cascade bus CAS0 through CAS2 are tied directly to the multibus address lines ADR8 through ADRA. These contain the PIC address code from the trailing edge of the first multibus INTA pulse to the trailing edge of the third multibus INTA pulse. The corresponding PIC is enabled during byte 2 and 3 of INTA (Byte 2 only for MCS-86 mode).

3-34. 8259A DATA BUS BUFFER

The 8-bit tri-state, bidirectional data bus buffer is used to transfer control words and status information between the 8259A and the system data bus. The direction of transfer is controlled by a read or write input signal.

3-35. 8259A LEAST-SIGNIFICANT ADDRESS BIT ABO

ABO is the least-significant address bit output from the CPU and is used with the read (RD) and write (WR) signals to read status registers or write commands into command registers. ABO is tied directly to the on-board address line ADR0.

3-36. 8259A ADDRESSING

Each 8259A user two consecutive I/O addresses for writing commands and vector data and reading status. The addresses and their functions are shown in table 3-1.

3-37. 8259A INITIALIZATION

Initializing a PIC requires writing Initilization Command words (ICWs); to the PIC. The following description explains the general ICW formats shown in figure 3-11.

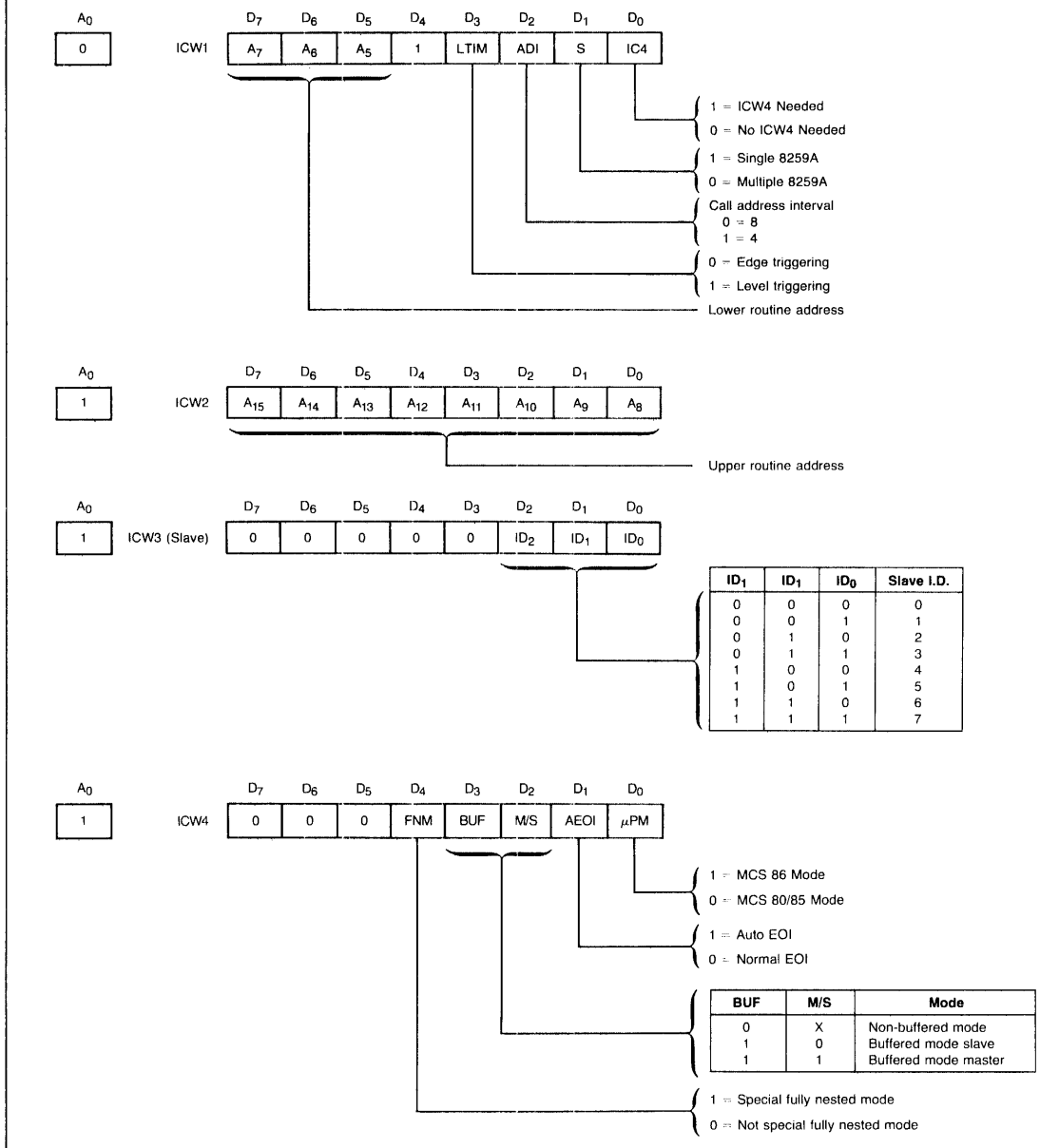


Figure 3-11. 8259A Initialization Command Word (ICW) Format

- ICW1 and ICW2 - The functions of the ICW1 control bits are:

  IC4 - When IC4=1, an ICW4 word is required; IC4=0 when none of The ICW4 functions are required.

  S - Specifies whether or not the 8259A is to be used as a slave. Set S=0 for slave operation; S=1 otherwise.

  ADI - Specifies the address interval for the MCS 80/85 mode when the 8259A is to be used as a slave. Set ADI=0 for an 8-byte interval; ADI=1 for a 4-byte interval.

  LTIM - Selects interrupt request input Trigger mode. Set LTIM=1 for level Triggering; LTIM=0 for edge Triggering

  A5-A15 - Specify the 16-bit interrupt vector address (The CALL routine address) in the MCS 80/85 mode. There are two modes for specifying the vector, depending on the value of ADI.

  ADI=1: 4-byte interval mode. In this mode the 8259A specifies the 16-bit vector as follows:

  A0-A1 = 0
  A2-A4 = 3-bit code specifying one of the eight IR0 through IR7 inputs.
  A5-A15 = User programmed

  ADI=0: 8-byte interval mode.

  A0-A2 = 0
  A3-A5 = IR0 through IR7 code
  A6-A15 = User programmed.

  When in the MCS86 mode, the ADI control bit is ignored and the interrupt vector is an 8-bit pointer. Only the high byte of the address bits is sent out by the 8259 using address bits as follows:

  A8-A10 = IR0 through IR7 code.
  A11-A15 = User programmed

  ICW3 -

  Used only when the 8259A is programmed for slave mode. Bits ID0 through ID2 identify the slave. This slave identifier should correspond to the IR input of the 8259A master to which the GINT output of the 8259A is connected. The 8259A master typically resides on a multibus CPU board such as the Am95/4006 MonoBoard computer.

ICW4 — Used only when ICW1 bit IC4=1. When ICW4 is not used, the modes offered by ICW4 default to the mode selected by all bits in ICW4=0. ICW4 is used to select the following modes:

μPM - 0 = MCS 80/85 mode.
1 = MCS 86 mode

AEOI - 0 = Normal EOI. An EOI command must be issued during the interrupt service routine.
0 = Automatic EOI. An EOI is automatically generated when the interrupt is acknowledged.

BUF-M/S - 0X = Non-buffered mode. Used when the 8259A is not a slave.
10 = Buffered mode. Used when the 8259A is a slave.
11 = Not applicable to the 8259A as used on the Am95/3310 board.

FNM - 0 = Not special fully nested mode. This mode should always be used for the Am95/3310 board.
1 = Never used for the Am95/3310 board.

There are two basic configurations, independent and slave, in which the 8259A can be used on the Am95/3310. The independent configuration must be used in systems that do not support multibus bus-vectored interrupts. In these systems, a bus master (usually a CPU board) receives an interrupt from an 8259A on the Am95/3310 via one of the multibus IREQ lines. The master must then poll the the appropriate 8259A to determine which of the eight interrupt inputs is currently in service. An EOI command must then be issued to clear the interrupt in service.

The slave configuration can be used in systems which support multibus bus-vectored interrupts. In these systems, a bus master receives an interrupt from an 8259A on the Am95/3310 via one of the multibus IREQ lines. The master then issues a series of multibus interrupts (INTA). On the first INTA, the 8259A on the Am95/3310 compares the slave identifier (put on the multibus by the master) with the slave I.D. programmed into the 8259A. When there is no match, the 8259A ignores subsequent INTAs. When there is a match, the 8259 outputs one or two interrupt vector bytes (MCS86 or MCS80/85 mode, respectively) upon receiving one or two additional INTAs. When in EOI mode, the 8259A interrupt in service is cleared following the last INTA. Otherwise, and EOI command must be issued to clear the interrupt in service.

The recommended 8259A initialization sequence for the two configurations is shown in figure 3-12.

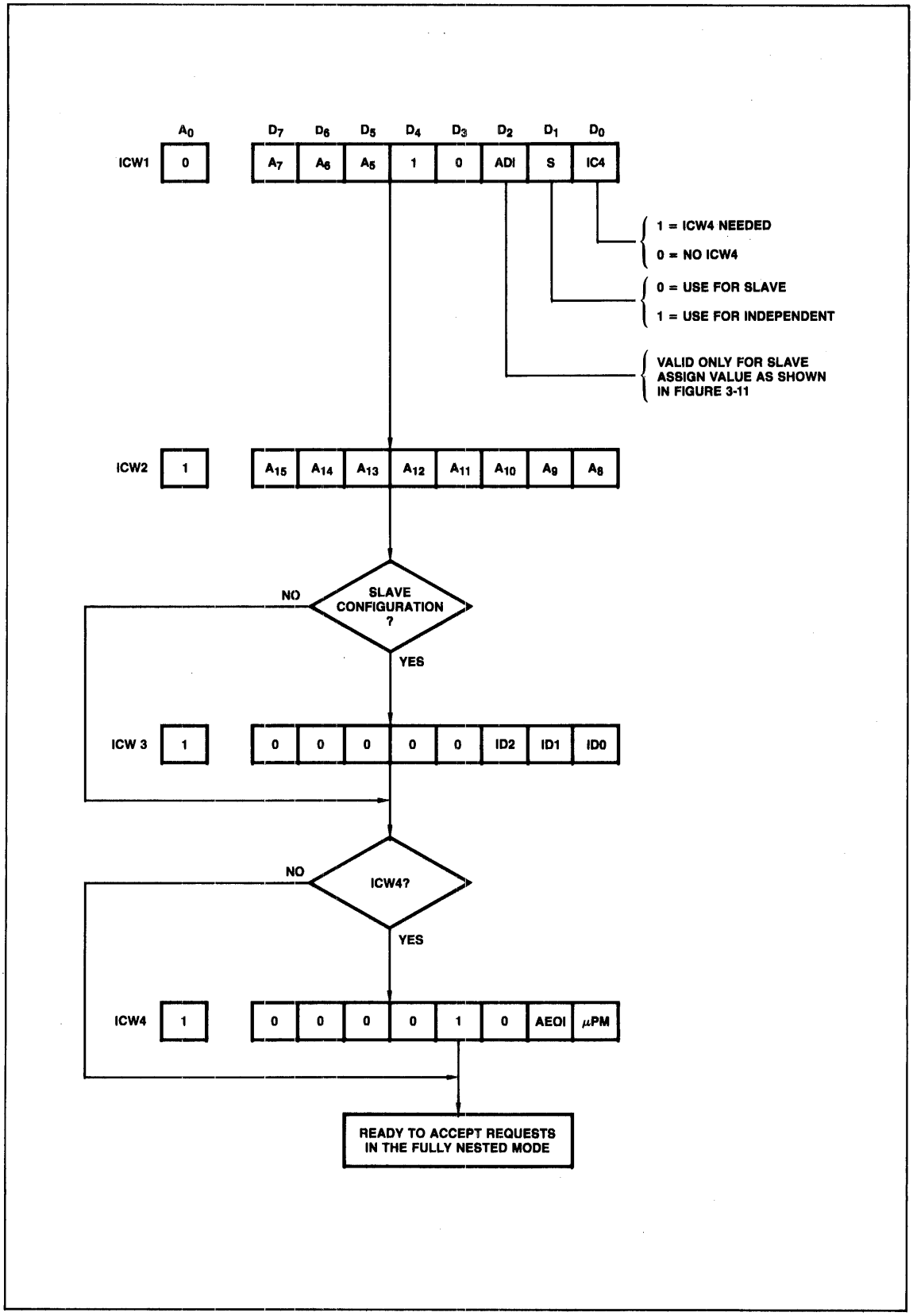


Figure 3-12. Am95/3310 8259A Initialization Sequence

After initialization, the PICs can be programmed for the following operations:

- Auto-rotating priority.
- Specific rotating priority.
- Status read of Interrupt Request Register (IRR).
- Status read of In-Service Register (ISR).
- Interrupt mask bits set, reset, or read.
- Special mask mode set or reset.

3-38. 8259A OPERATION COMMAND WORDS (OCWs)

The PICs can be programmed after initialization for various operations and modes. The OCW formats are shown in figure 3-13.

3-39. 8259A OPERATION MODES

Each PIC resolves interrupt requests priority in one or four modes of operation: rotating, fully-nested, special mask, or polled mode. The rotating mode is used in applications of interrupt devices having equal priority (e.g. communication channels). There are two variations of the rotating mode:

- Auto-Rotating. In this mode the interrupt priority rotates after a given input is serviced and that interrupt assumes the lowest priority. If there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order.

To Set:	In OCW2, write a Rotate Priority at EOI command (A0H) to 88H (PIC0) or 8AH (PIC1).
To Terminate Interrupt and Rotate Priority:	In OCW2, write EOI command (20H) to 88H (PIC0) or 8AH (PIC1).

- Specific Rotating. In this mode the user can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority (e.g. if IR5 is assigned the bottom priority, IR6 assumes the highest priority).

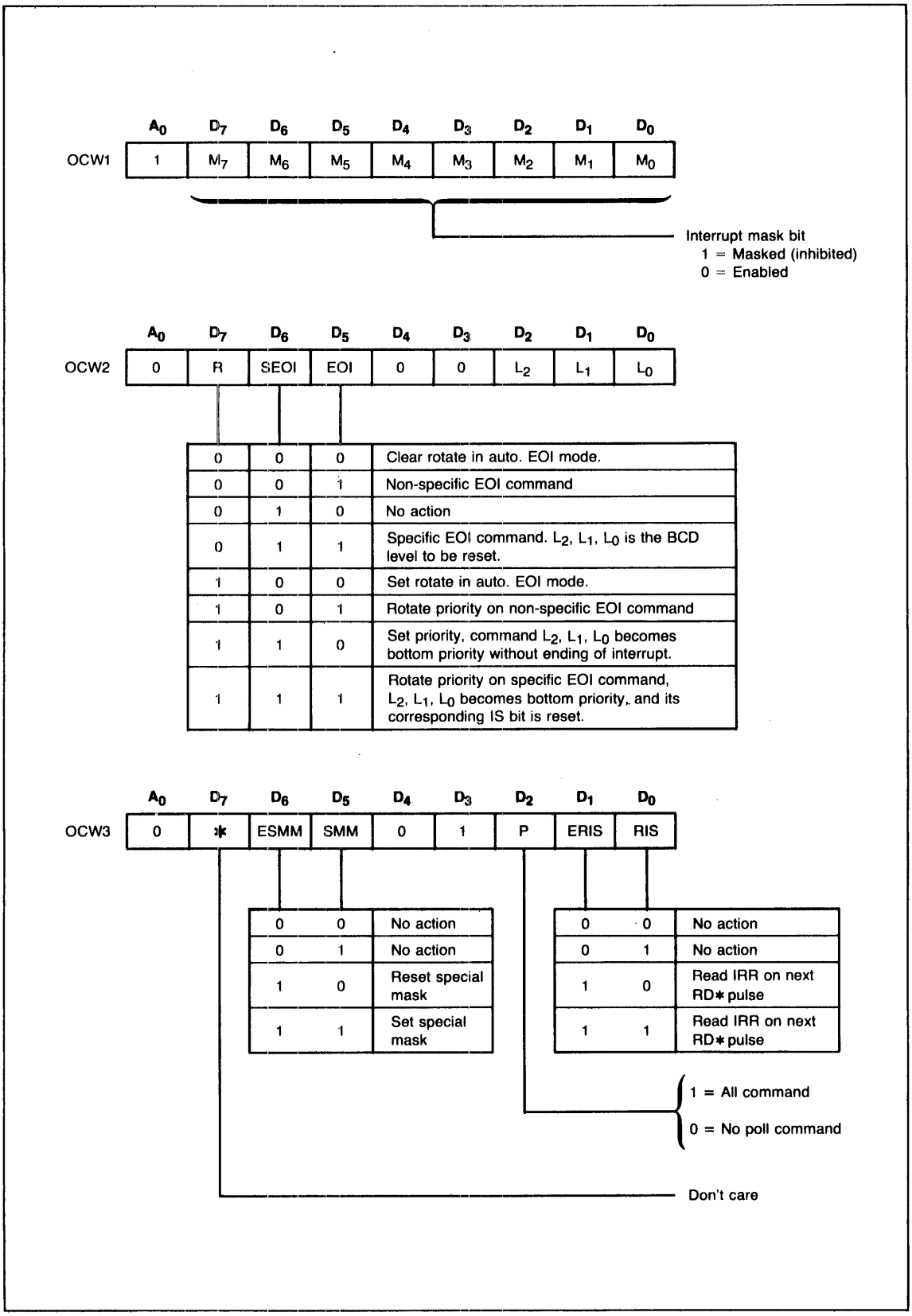


Figure 3-13. 8259A Operation Command Word (OCW) Format

To Set:

In OCW2, write a Rotate Priority at specific end of interrupt (SEOI) command in the following format to 88H (PIC0) or 8AH (PIC1):

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	L2	L1	L0

L2-L0 is the BCD identifier of the interrupt input line to be reset and/or put into lowest priority.

To Terminate and Rotate Priority:

In OCW2, write an SEOI command in the following format to 88H (PIC0) or 8AH (PIC1):

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	L2	L1	L0

L2-L0 is the BCD identifier of the in service register bit to be reset.

To Set Priority Without EOI:

In OCW2, write a command word in the following format to 88H (PIC0) or 8AH (PIC1).

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	L2	L1	L0

L2-L0 is the BCD identifier of the bottom priority interrupt input line.

In the Fully-Nested Mode, the PIC(s) input signals are assigned priority from 0 through 7. The PICs operate in this mode unless specifically programmed otherwise (e.g. interrupt input IR0 has the highest priority and IR7 has the lowest priority). The End-of-Interrupt (EOI) command from the CPU is required to reset the PIC(s) for the next interrupt.

The Special Mask Mode is used in applications requiring a service routine to inhibit lower priority requests for a portion of its execution and enables all others that are not masked for a portion of its execution.

- In OCW3. To set, write 68H to 88H (PIC0) or 8AH (PIC1)
- To clear, Write 48H to 88H (PIC0) or 8AH (PIC1)
- To specify the mask bits, write to OCW1 at 89H (PIC1) or 8BH (PIC1) with the format shown in figure 3-13.

The Polled Mode is used when there is a number of interrupt request levels sharing a common routine command or when the number of priority levels are expanded to more than 64. To conduct a Poll, use OCW3, write OCH to 88H (PICO) or 8AH (PIC1). Then execute a read command to 88H (PICO) or 8AH (PIC1). If an interrupt is active, the most-significant data bit will be set and the three least-significant data bits D2, D, DO will be the BCD code of the highest pending priority interrupt.

3-40. END-OF-INTERRUPT AND SPECIFIC END-OF-INTERRUPT COMMANDS

An End-of-Interrupt (EOI) or a Specific End-of-Interrupt (SEOI) Command is required at the end of each interrupt service routine to reset the active bit of the In-Service Register. The EOI command is used in the fully-nested and auto-rotating priority modes and the SEOI command which specifies the bit to be reset, is used in the specific rotating priority mode.

3-41. 8259A STATUS READ

The input status of the following internal registers can be read:

- Interrupt Request Register (IRR)
- In-Service Register (ISR)
- Interrupt Mask Register (IMR)

The ISR stores a logical one in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR:

1. Write an OCW3 of OBH to 88H (PICO) or 8AH (PIC1).
2. Read 88H (PICO) or 8AH (PIC1). Status format is:

	D7	D6	D5	D4	D3	D2	D1	DO
IR Line:	7	6	5	4	3	2	1	0

Be sure to reset the ISR bit with a specific end-of-interrupt command when in the specific EOI mode. The ISR bit is automatically reset in the non-specific EOI mode. To reset the ISR bit, write an OCW2, of:

D7	D6	D5	D4	D3	D2	D1	DO
0	1	1	0	0	L2	L1	L0

L2-L0 is the BCD identifier of the ISR bit to be reset.

To read the mask bits, read OCW1 from 89H (PIC0) or 8BH (PIC1). The mask byte has the following format:

	D7	D6	D5	D4	D3	D2	D1	D0
IR Bit Mask: 1=Mask Set, 0=Mask Reset	M7	M6	M5	M4	M3	M2	M1	M0

The IRR stores a logical one in the associated bit for each IR input line that is requesting an interrupt. To read the IRR:

1. Write 0AH to 88H (PIC0) or 8AH (PIC1)
2. Read 88H (PIC0) or 8AH (PIC1). Status format is:

	D7	D6	D5	D4	D3	D2	D1	D0
IR Line:	7	6	5	4	3	2	1	0

CHAPTER 4
THEORY OF OPERATION

4-1. INTRODUCTION

The Am95/3310 has five major circuit areas; Bus Interface, Baud-Rate Generator/Timer Logic, Interrupt Control Logic, four Serial I/O ports, and three Parallel I/O ports. Each of these circuits are described in this chapter. For detailed circuit information use the schematic diagrams provided in Chapter 5. To facilitate this description, figure 4-1, the 95/3310 block diagram is divided up into five circuit areas.

4-2. BUS INTERFACE

These circuits buffers the Multibus signals DAT0* through DAT7* and ADR0* through ADRF*; compare ADR5* through ADR7* for 8-bit CPUs and ADR8* through ADRF* for 16-bit CPUs to determine board selection, and board control; decodes ADR0* through ADR4* for chip-select; and generate transfer acknowledge (XACK*) signals.

4-3. DATA BUFFERS

Two Am8226s (U76 and U78) buffer the multibus data (DAT0* through DAT7*) from connector P1. The outputs of U76 and U78 are internal data bits DB0 through DB7.

4-4. ADDRESS BUFFERS

Two Am74LS240s (U75 and U77) buffer and invert the input address ADR0* through ADRF* from P1 connector. The outputs of U75 and U77 are used for determining board control and chip-selects.

4-5. BOARD SELECTION

Address bits ADR5* through ADR7* (8 bit CPU) or ADR5* through ADRF* (16 bit CPU) from Multibus are compared with switch settings of SW2 and SW1, respectively. An equal causes U79 and U64 (eight bit comparators) 19 to go low to enable the chip-select logic.

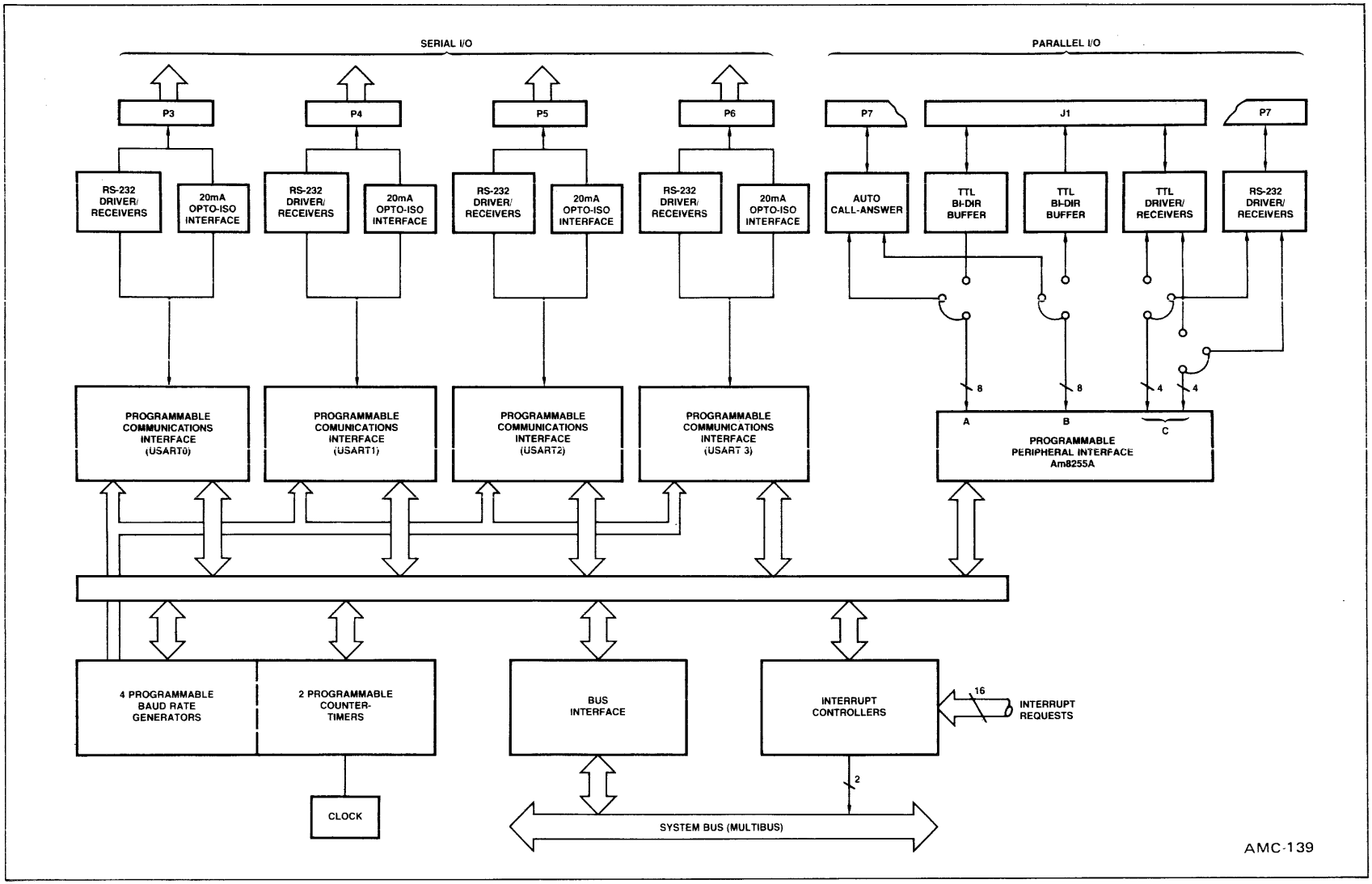


Figure 4-1. Am95/3310 Communication Expansion Board Function Diagram

4-6. CHIP-SELECT LOGIC

The Chip-Select Logic U46 and U49 decodes ADR1* through ADR4* to produce the chip-selects of the nine programmable chips. U46 and U49 are enabled by U79 (board select, BS*) and ADR4*.

4-7. BOARD READ/WRITE LOGIC

The inputs to Read/Write Logic,(U82, U83, U52, and U53) are IOWC* and IORC* from Multibus and BS* from the address comparator (U79). These signals are used to generate internal read/write (RD*/WRT*) signals.

4-8. ACKNOWLEDGE LOGIC

The Acknowledge Logic (U72) generates the Transfer Acknowledge signal XACK*. The 19.6608 MHz OSC output of U80 drives the clock input of U72. The multibus IOR or IOW command is synchronized to the 19.6608 MHz clock by U59, then delayed about 50 nsec (1 clock) to allow the address to be set up for the LSI chips. This delayed command is applied to U72, which shifts the high on input 1D to output 6Q. Output 6Q going high causes XACK* to be generated about 300 nsec after the delayed command. The delay from the multibus IOR or IOW command to XACK* varies from 350 nsec to 400 nsec due to the synchronization.

4-9. BOARD CLOCK LOGIC

The Board Clock Logic (U73) controlled by U80 (a 19.6608 MHz Crystal Oscillator) has one output; 02TTL (2.4576 MHz on Pin 12). The 19.6608 MHz output drives the clock input of U72. The U57 divides the 2.4576 MHz by two to provide the clock input (1.2288 MHz) for the two Am8253 PITs (U56 and U67).

4-10. BAUD RATE GENERATOR/TIMER LOGIC

Two Am8253s (U56 and U67) generate four Baud-Rate Clocks, BRCLK0 through BRCLK3, and two additional signals (TIM0 and TIM1) which can be used as auxiliary generators or timers.

The 95/3310 is shipped with four of the six independent timers connected by jumpers to the USARTs (U66, U55, U38, and U27) and to each Data Terminal Equipment Transmit Clock/Teletype Receive Return (DTE Tx CLK/TTY Rx RET) output. The two remaining outputs, TIM0 and TIM1, are user-selected options.

4-11. INTERRUPT CONTROL LOGIC

The Am95/3310 interrupt control logic consists of two 8259A Programmable Interrupt Controllers (PICs), U39 and U28. Each PIC has eight interrupt request inputs. The function of the PICs is resolving priorities among two or more simultaneous interrupt request inputs and providing interrupt vectors. The interrupt output of each PIC is connected via jumpers to the system bus interrupt lines IRQ6 and IRQ7. The 8259A programming and function are described in chapter 3.

4-12. SERIAL I/O PORTS

The 95/3310 has four completely independent serial I/O ports as shown in figure 4-1. Each serial port uses a single Am9551 USART chip. The programmable functions are described in Chapter 3. In addition to the serial capabilities, each port has an additional circuit feature:

4-13. CURRENT-LOOP CIRCUITS

Each USART port has the capability to operate with opto-isolators for optical isolated data transmit and data receive signals (TxD and RxD). See Chapter 2 for a description of current-loop circuits.

4-14. CLOCK CONNECTION

The USART at each of the four ports requires two clock signals: RxC and TxC. Each USART chip has a jumper matrix with five clock input signals. All ports are supplied with clock signals BRCLK, TIM0 and TIM1. The only difference between Port 0 and the other ports is that the Port 0 jumper matrix receives clock signal BRCLK0, while Port 1 receives BRCLK 1, etc. Each port also receives the transmit clocks and the receive clock inputs from the four serial I/O port connectors. Similarly, the transmit clock rate is available at the data terminal transmit clock output (DTE Tx CLK/TTY Rx RET).

4-15. PARALLEL I/O PORT

The parallel I/O port supports general purpose parallel operations via connector J1, and automatic calling units, such as the Bell Model 801 (via connector P7). The primary circuit in the parallel I/O port is an 8255A Programmable Peripheral Interface (PPI). As shipped, ports A and B are used as input ports, and port C is used as an output port. Port B supports either auxiliary inputs or an Automatic Calling Unit (ACU); Port A receives carrier detect (CD) and ring indicator (RI) signals.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides service diagrams and information on service and repair assistance for AMC product lines.

5-2. SERVICE AND REPAIR ASSISTANCE

Service and repair assistance can be obtained from Advanced Micro Computers by contacting the AMC Field Service Department in Santa Clara, California at one of the following numbers:

Telephone: (408) 988-7777

Toll Free: (800) 672-3548 California

(800) 538-9791 U.S.A. (except California)

If it is necessary to return a product to Advanced Micro Computers for service or repair, contact the Field Service Department at the previously listed telephone number. A Return Material Authorization number will be provided along with shipping instructions and other important information that will help AMC provide you with fast, efficient service. When reshipment is due to the product being damaged during shipment from AMC, or when the product is out of warranty, a purchase order is required for the AMC Field Service Department to initiate the repair.

Prepare the product for shipment by repackaging it in the original factory packaging material, if available. When the original packaging is not available, wrap the product in a cushioning material (such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, New Jersey) and enclose in a heavy-duty corrugated shipping carton. Seal the shipping carton securely, mark it FRAGILE, and ship it to the address specified by the AMC Field Service Department.

Customers outside of the United States can contact an AMC Sales Office or Authorized AMC Distributor for directions on obtaining service or repair assistance.

5-3. SERVICE DIAGRAMS

The Am95/3310 component locations are shown on the assembly diagram in figure 5-1. Schematic diagrams of the Am95/3310 are shown in figures 5-2 through 5-12.

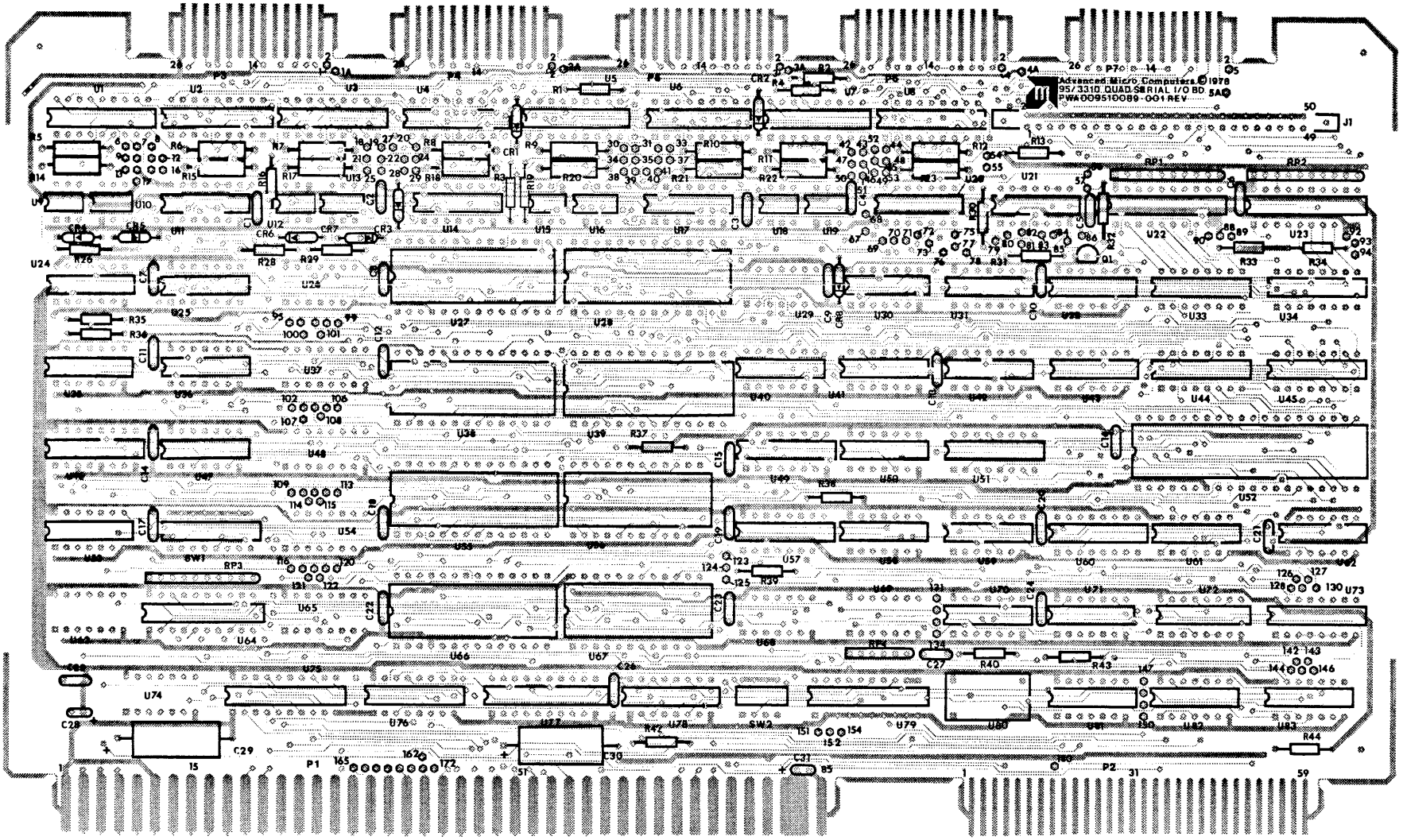
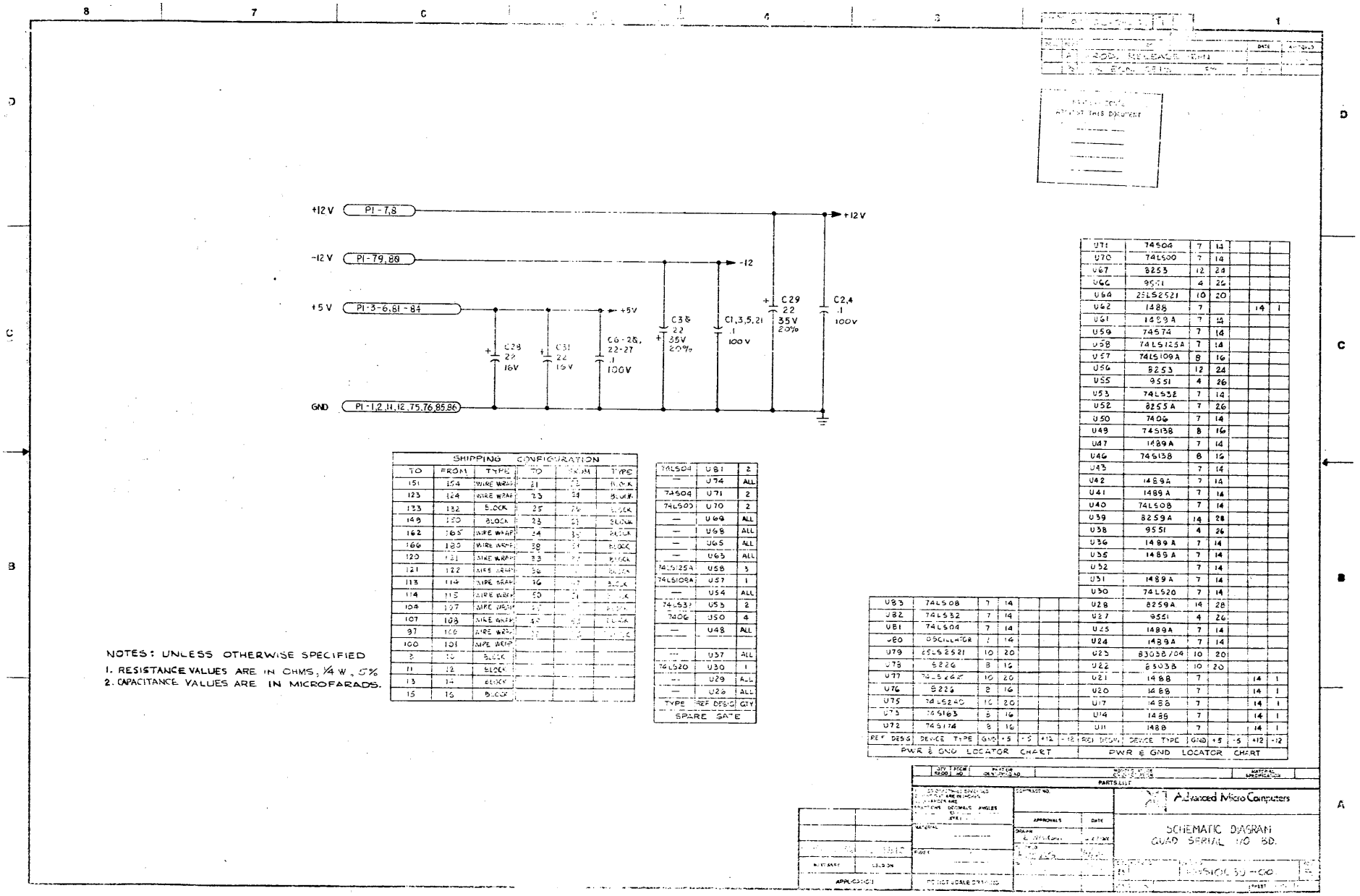


Figure 5-1. Am95/3310 Components Location Diagram



SHIPPING CONFIGURATION					
TO	FROM	TYPE	TO	FROM	TYPE
151	154	WIRE WRAP	21	22	BLOCK
123	124	WIRE WRAP	23	24	BLOCK
133	132	BLOCK	25	26	BLOCK
149	150	BLOCK	33	34	BLOCK
162	165	WIRE WRAP	34	35	BLOCK
166	180	WIRE WRAP	39	40	BLOCK
120	121	WIRE WRAP	33	32	BLOCK
121	122	WIRE WRAP	36	37	BLOCK
113	114	WIRE WRAP	16	17	BLOCK
114	115	WIRE WRAP	50	51	BLOCK
104	107	WIRE WRAP	52	53	BLOCK
107	108	WIRE WRAP	55	56	BLOCK
97	100	WIRE WRAP	57	58	BLOCK
100	101	WIRE WRAP			
9	10	BLOCK			
11	12	BLOCK			
13	14	BLOCK			
15	16	BLOCK			

74LS04	U81	2
—	U74	ALL
74S04	U71	2
74LS03	U70	2
—	U69	ALL
—	U68	ALL
—	U65	ALL
—	U63	ALL
74LS125A	U58	3
74LS109A	U57	1
—	U54	ALL
74LS32	U53	2
7406	U50	4
—	U48	ALL
—	U37	ALL
74LS20	U30	1
—	U29	ALL
—	U26	ALL
TYPE	REF DES'G	QTY
SPARE GATE		

REF DES'G	DEVICE TYPE	GND	+5	-5	+12	-12
U71	74S04	7	14			
U70	74LS00	7	14			
U67	8253	12	24			
U66	9551	4	26			
U64	25LS2521	10	20			
U62	1488	7			14	1
U61	1489A	7	14			
U59	74S74	7	14			
U58	74LS125A	7	14			
U57	74LS109A	8	16			
U56	8253	12	24			
U55	9551	4	26			
U53	74LS32	7	14			
U52	8255A	7	26			
U50	7406	7	14			
U48	74S138	8	16			
U47	1489A	7	14			
U46	74S138	8	16			
U43		7	14			
U42	1489A	7	14			
U41	1489A	7	14			
U40	74LS08	7	14			
U39	8259A	14	28			
U38	9551	4	26			
U36	1489A	7	14			
U35	1489A	7	14			
U32		7	14			
U31	1489A	7	14			
U30	74LS20	7	14			
U28	8259A	14	28			
U27	9551	4	26			
U25	1489A	7	14			
U24	1489A	7	14			
U23	83038/04	10	20			
U22	8303B	10	20			
U21	1488	7			14	1
U20	1488	7			14	1
U17	1488	7			14	1
U14	1488	7			14	1
U11	1488	7			14	1

PWR & GND LOCATOR CHART

REF DES'G	DEVICE TYPE	GND	+5	-5	+12	-12
U83	74LS08	7	14			
U82	74LS32	7	14			
U81	74LS04	7	14			
U80	OSCILLATOR	7	14			
U79	25LS2521	10	20			
U78	8226	8	16			
U77	74LS244	10	20			
U76	8226	8	16			
U75	74LS240	10	20			
U73	74S163	8	16			
U72	74S174	8	16			

PWR & GND LOCATOR CHART

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS, ¼ W, 5%
2. CAPACITANCE VALUES ARE IN MICROFARADS.

PARTS LIST

Advanced Micro Computers

SCHEMATIC DIAGRAM
QUAD SERIAL I/O BD.

Figure 5-2. Am95/3310 Schematic Diagram Sheet 1

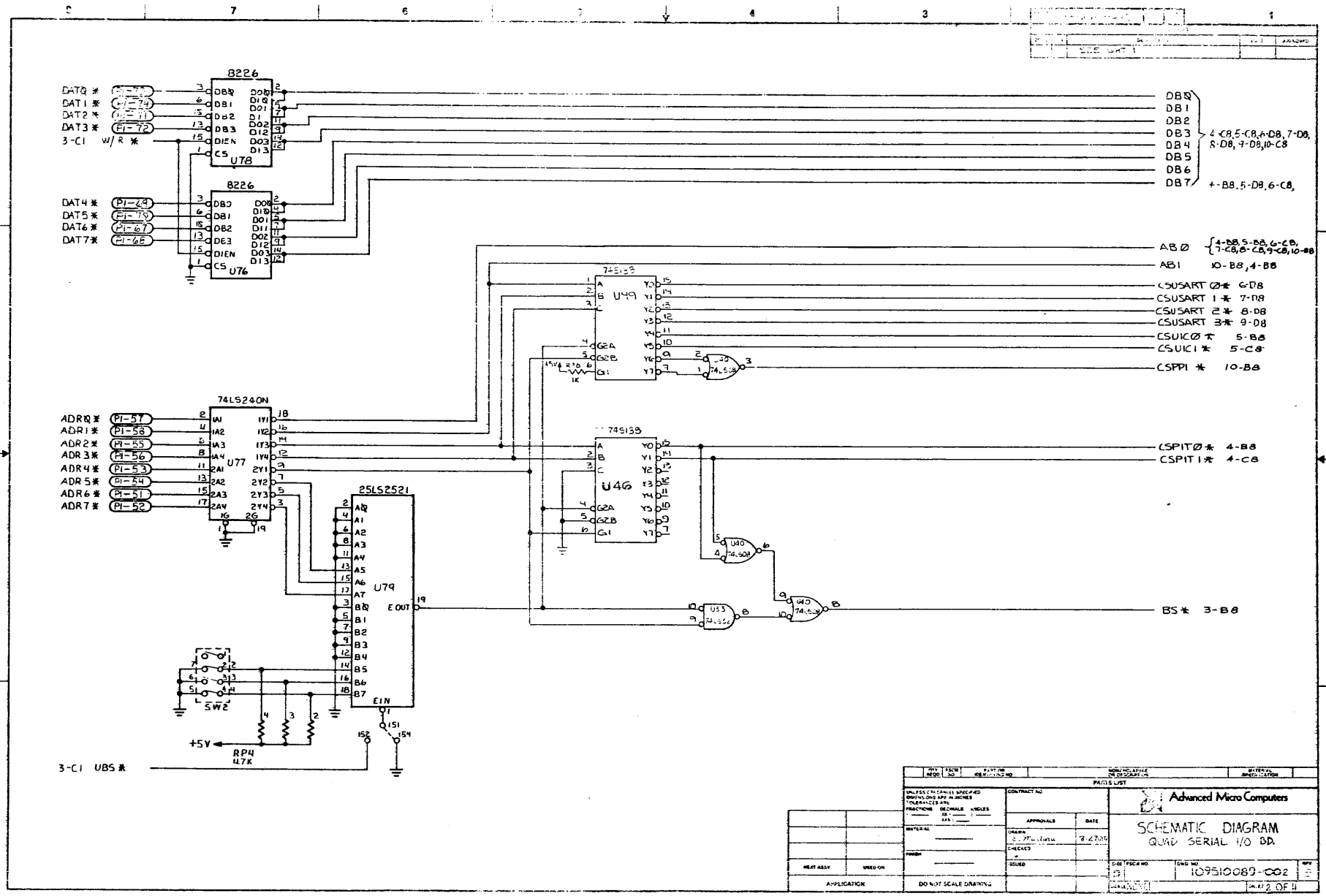


Figure 5-3. Am95/3310 Schematic Diagram Sheet 2

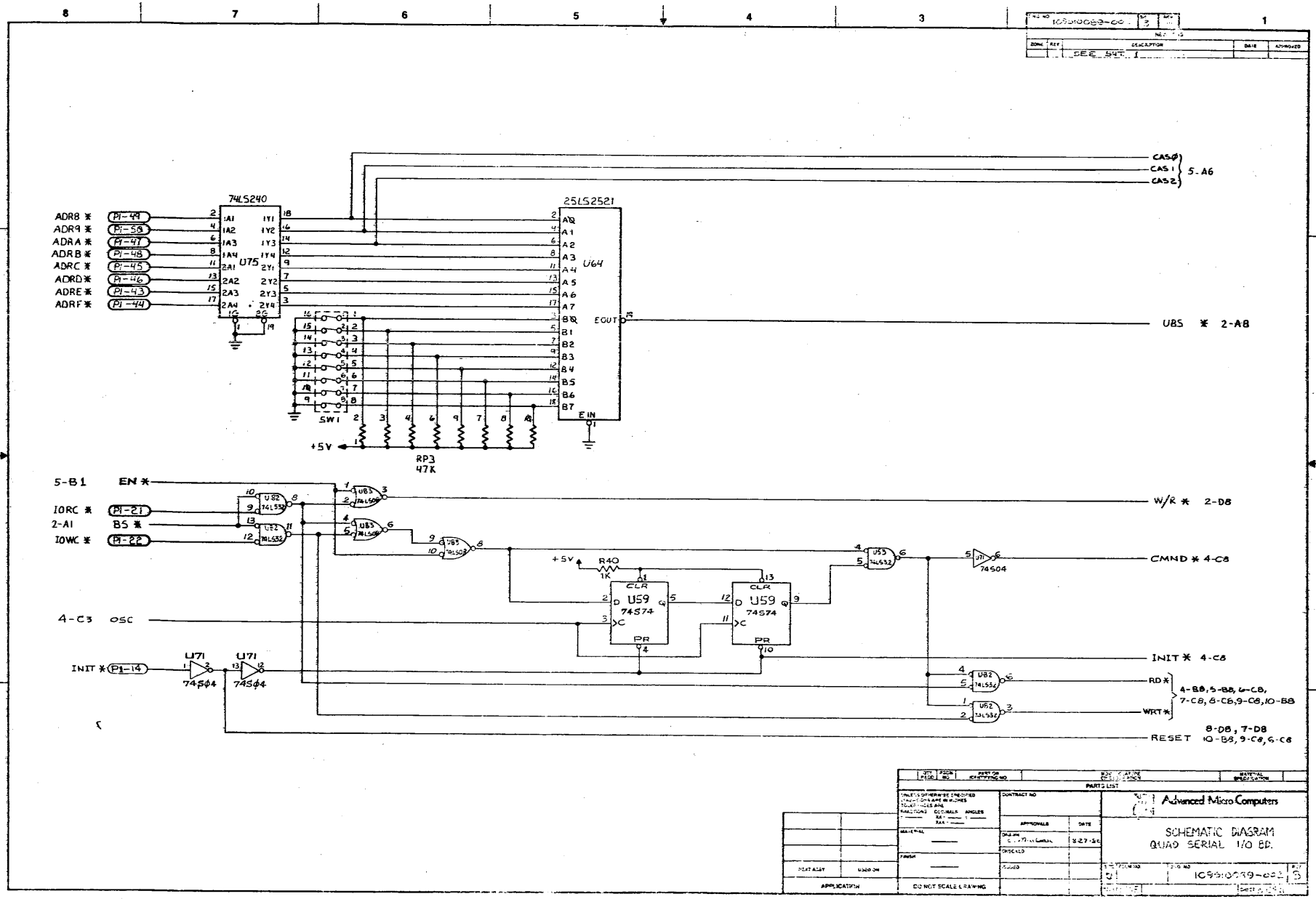


Figure 5-4. Am95/3310 Schematic Diagram Sheet 3

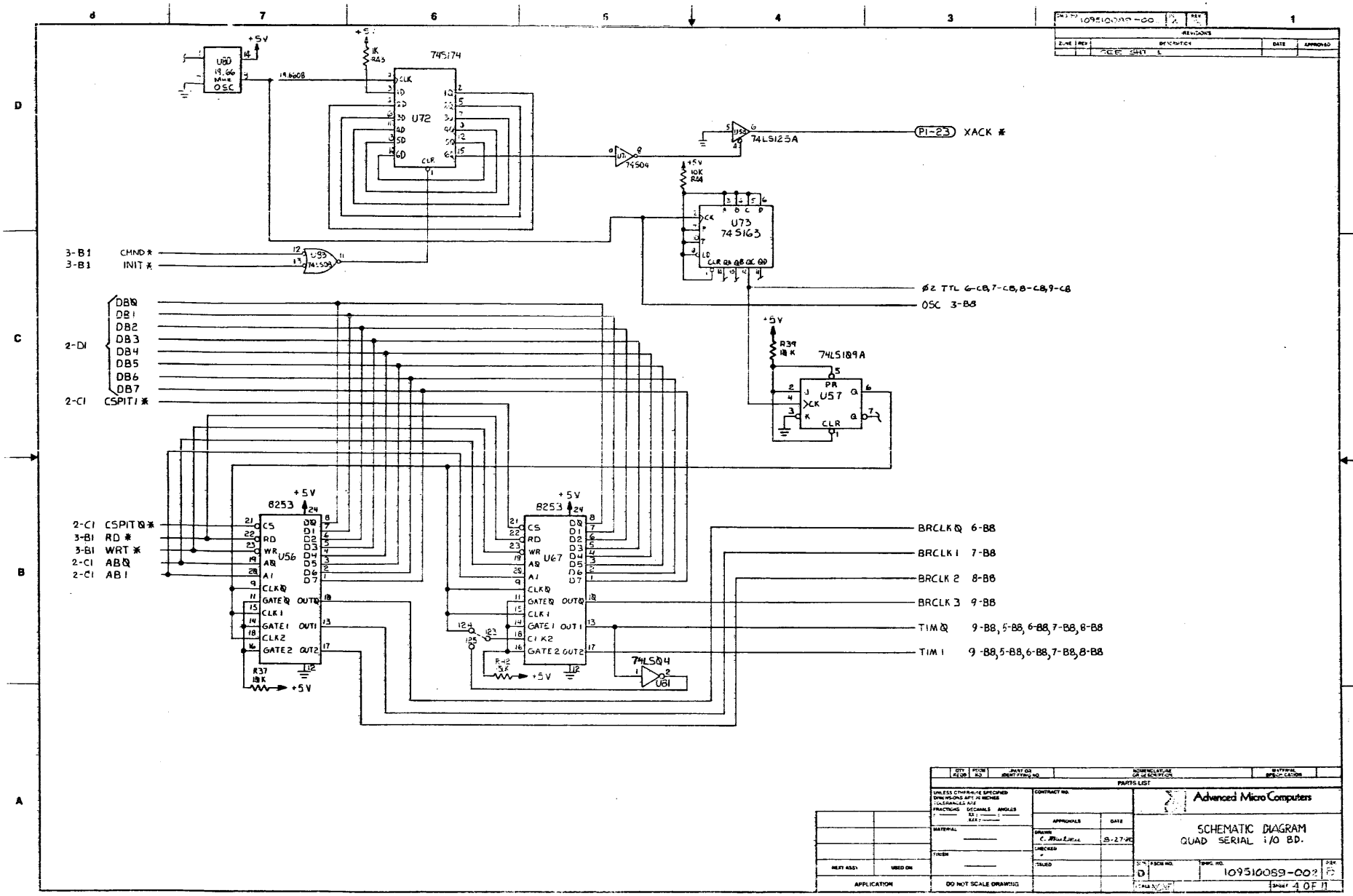


Figure 5-5. Am95/3310 Schematic Diagram Sheet 4

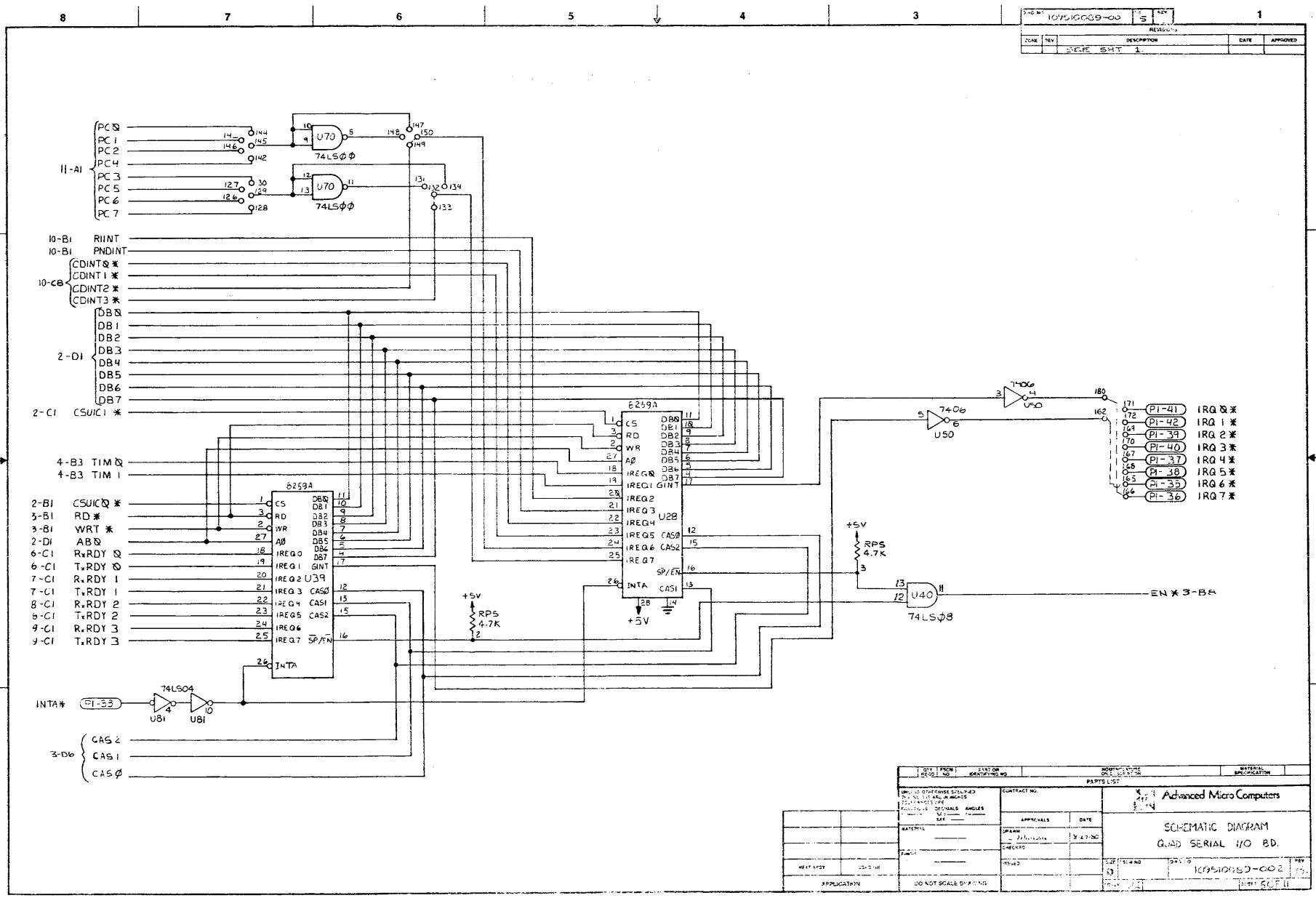


Figure 5-6. Am95/3310 Schematic Diagram Sheet 5

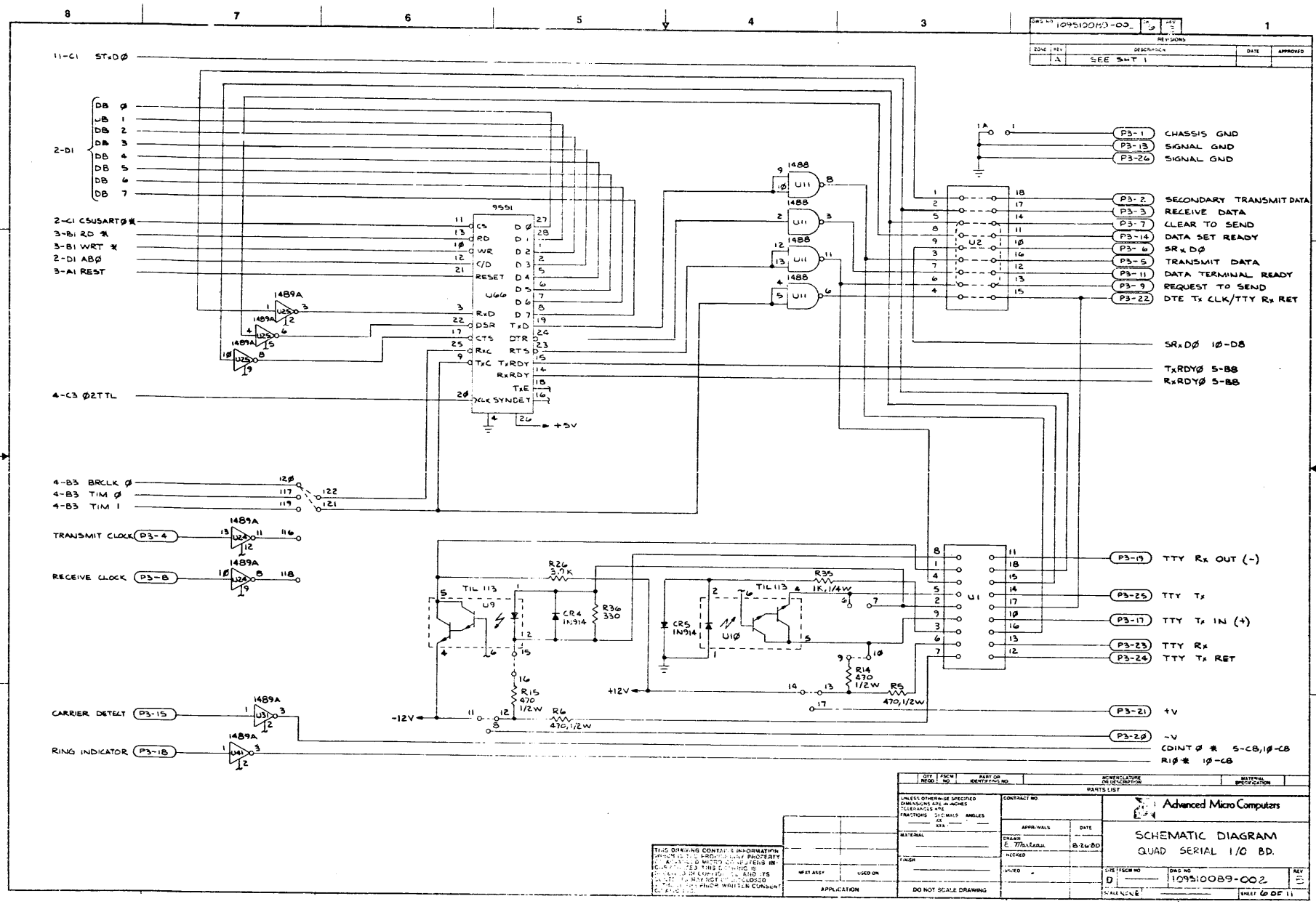


Figure 5-7. Am95/3310 Schematic Diagram Sheet 6

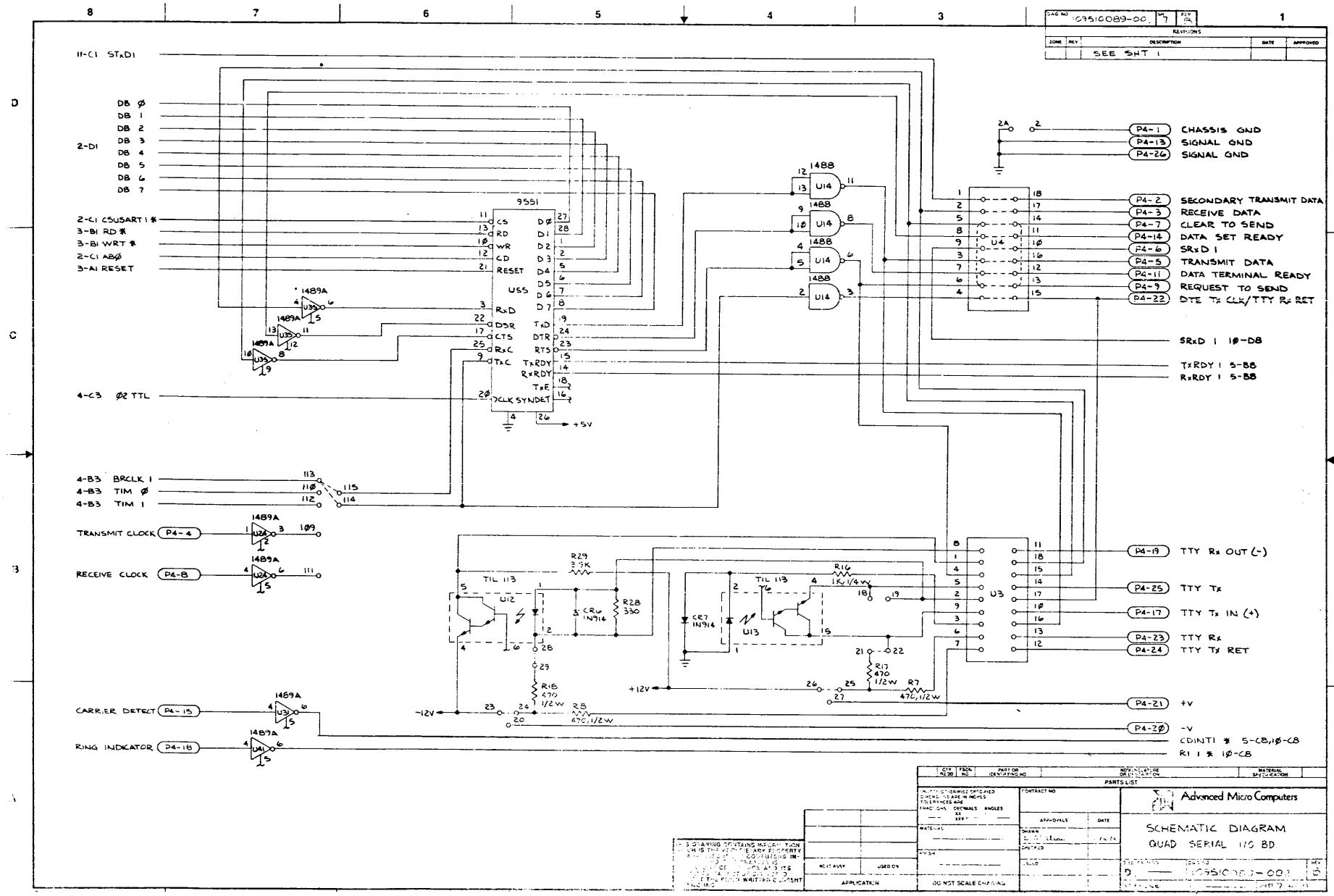


Figure 5-8. Am95/3310 Schematic Diagram Sheet 7

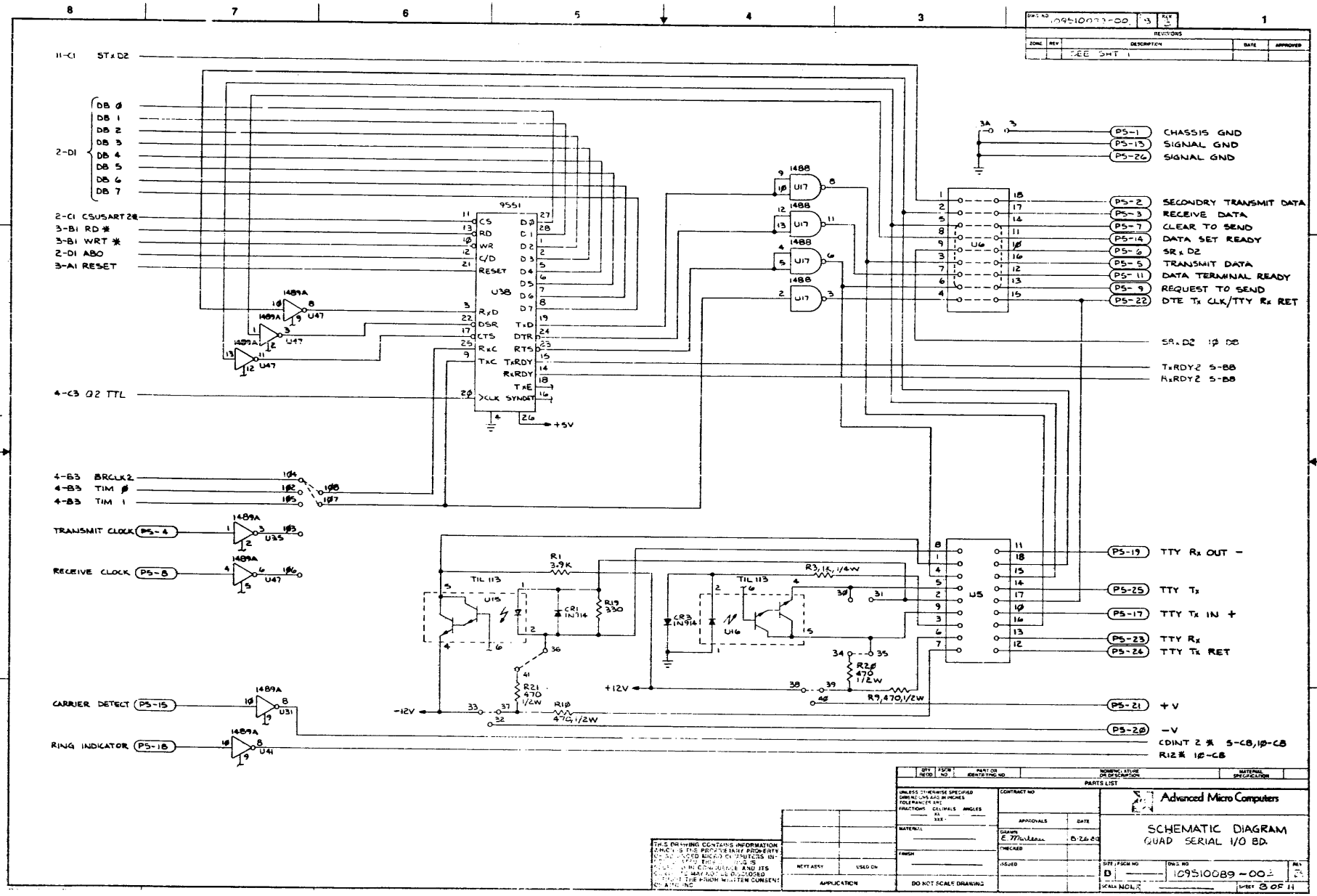


Figure 5-9. Am95/3310 Schematic Diagram Sheet 8

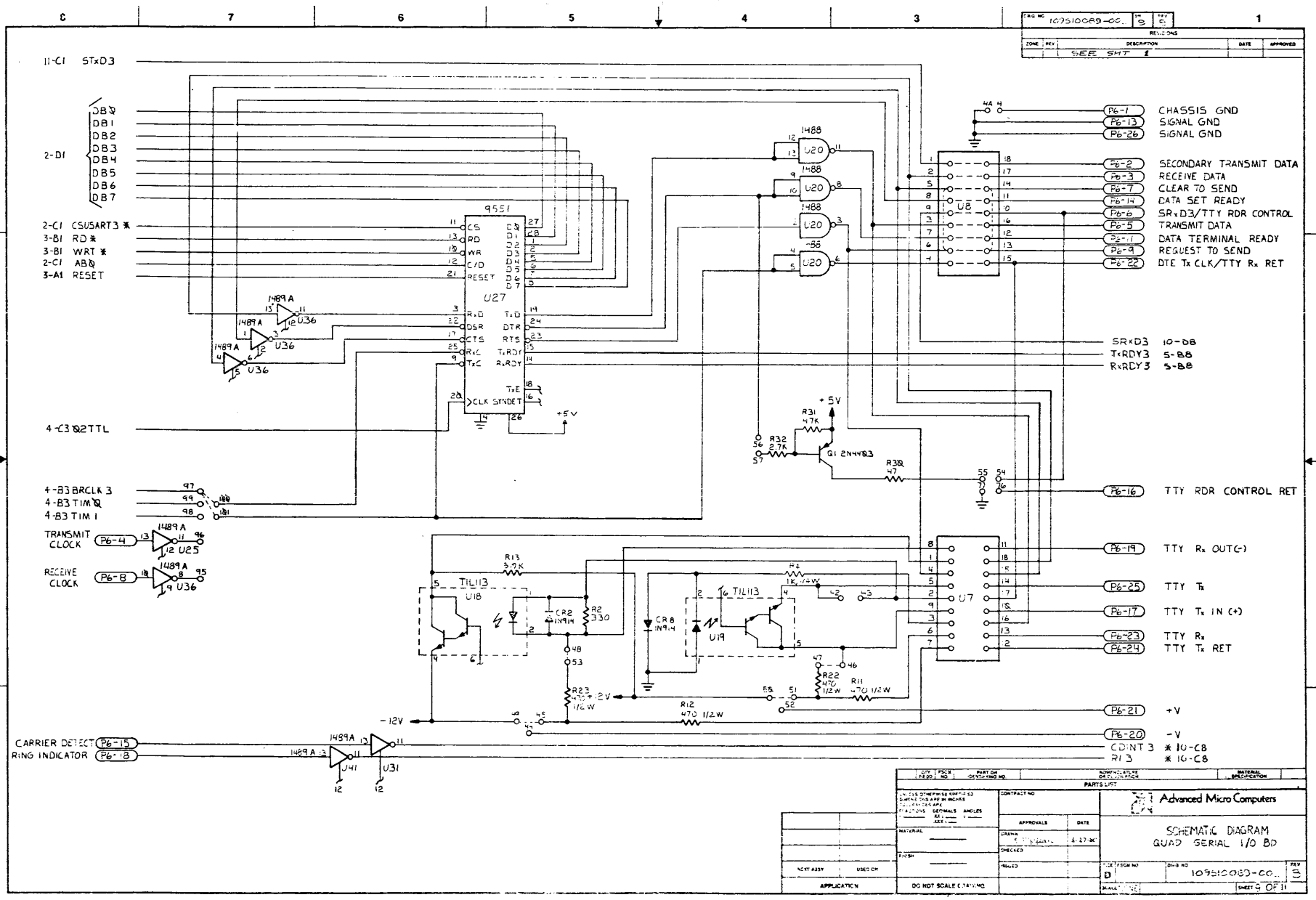


Figure 5-10. Am95/3310 Schematic Diagram Sheet 9

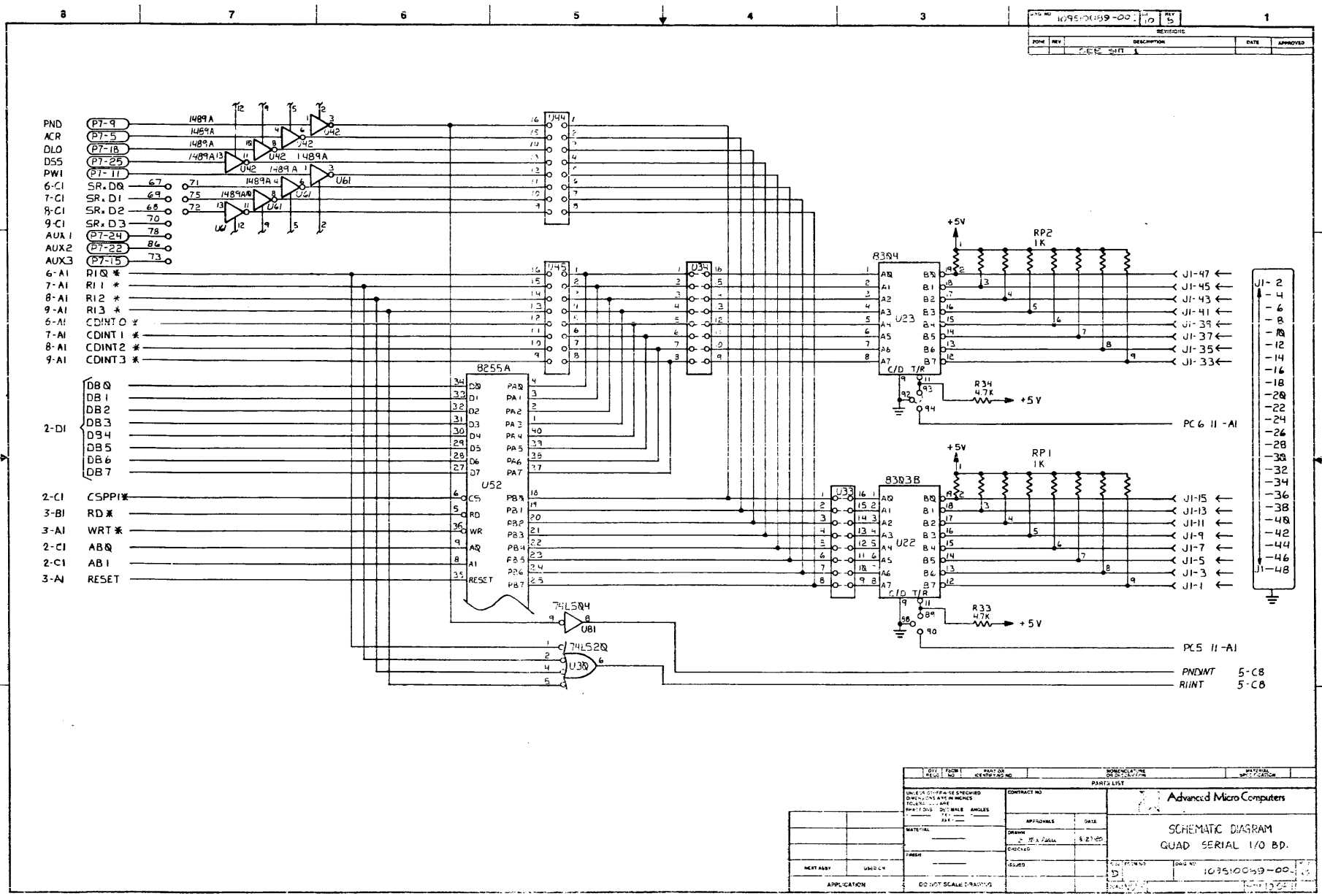


Figure 5-11. Am95/3310 Schematic Diagram Sheet 10

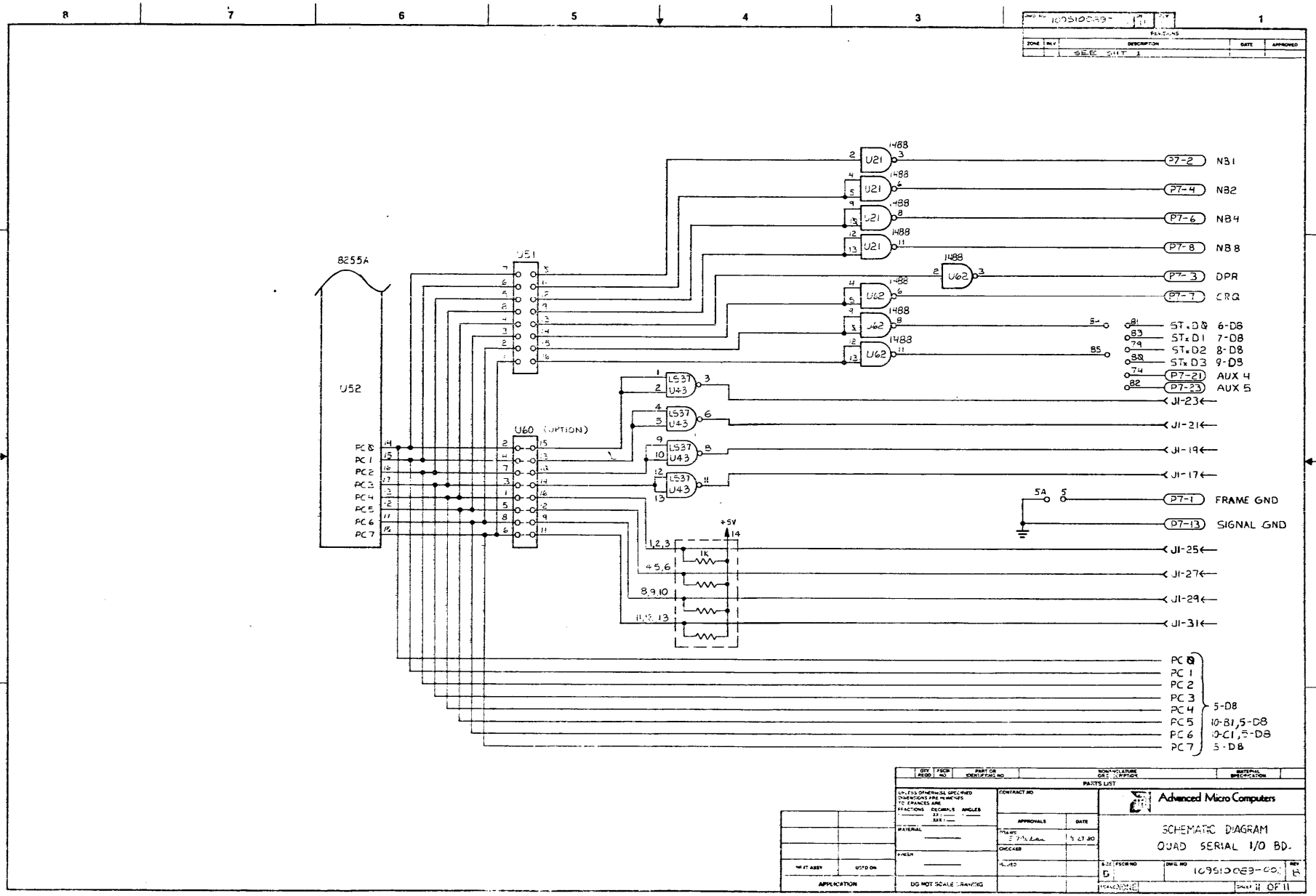


Figure 5-12. Am95/3310 Schematic Diagram Sheet 11

COMMENT SHEET

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