AMPEX

AMPEX 230/219
VIDEO DISPLAY TERMINALS
SERVICE MANUAL

3515021–01

JUNE 1985

AMPEX MEMORY PRODUCTS DIVISION

AMPEX

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Ampex Corporation, Computer Products Division
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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions in this book, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION I
OVERVIEW

1.1 PURPOSE AND SCOPE

This manual provides installation and maintenance information for the Ampex 230/219 Video Display Terminals. General information about the terminal, including specifications, is provided in this section. Installation procedures are explained in Section II. Section III is the general theory of operation. Maintenance information, including testing, definitions of error messages, adjustment procedures, and troubleshooting is included in Section IV. Section V provides removal and replacement procedures of the major components of the terminal. Appendix A gives installation instructions for user-installable options. Reference drawings and schematics are provided in Appendix B.

1.2 REFERENCES

Operation Manuals for the Ampex 230/219 terminals are available from Ampex. The part number for the Ampex 230 manual is 3515332-01, Rev B. The part number for the Ampex 219 manual is 3515453-01.

1.3 GENERAL DESCRIPTION

The Ampex 230/219 Video Display Terminals (henceforth referred to as the terminal) are a series of microprocessor-controlled, computer input/ output peripherals. The terminals operate in either full-duplex or half-duplex; conversation, block, or line transmission modes, or local (non-transmission) mode.

Physically, the terminal is composed of three major subassemblies: display unit, keyboard, and pedestal unit (Figure 1-1). The display unit is a two-piece molded plastic case housing a cathode ray tube (CRT) and the electronic circuitry necessary to perform the display functions. The pedestal unit is also a two-piece plastic case. In it, are housed the circuitry necessary to perform the required interfacing and data communications functions of a video display terminal. The keyboard unit provides the interface between the terminal operator and the display/pedestal units. A single, coiled cable connects the keyboard to the pedestal unit.

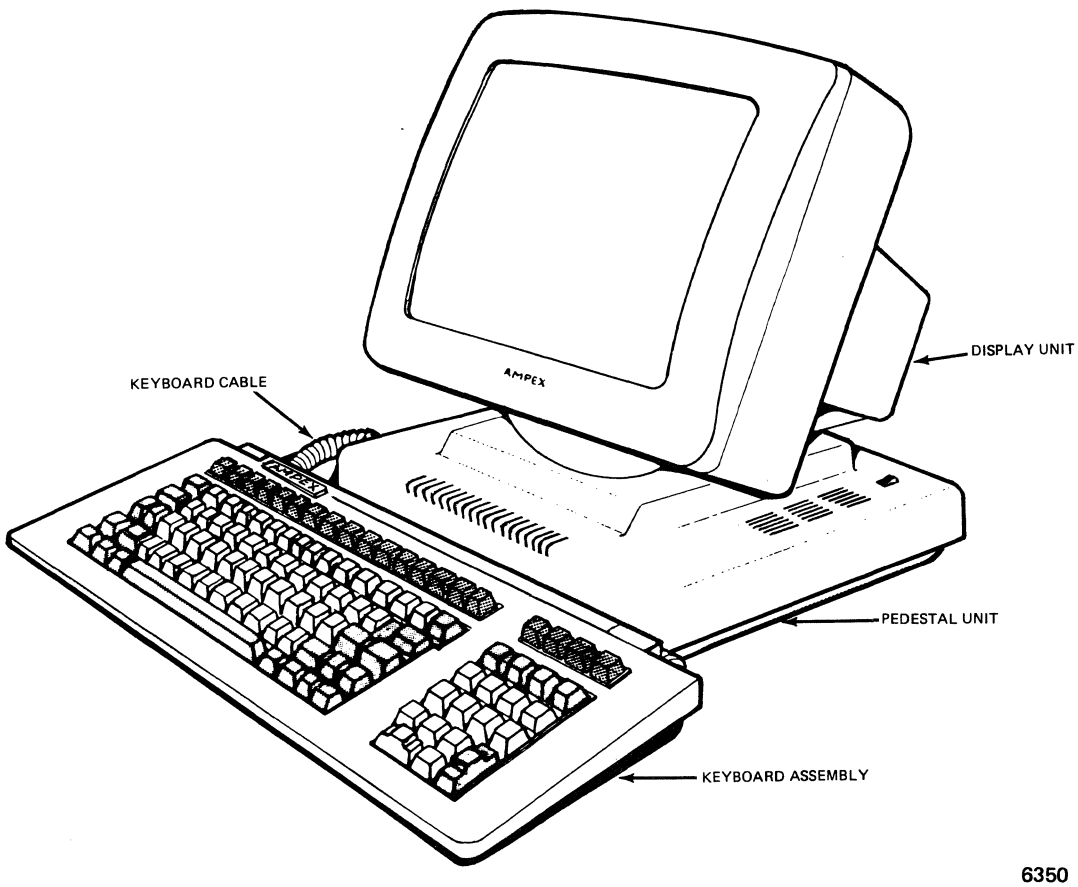


Figure 1-1. Ampex 230/219 Video Display Terminal (Major Subassemblies)

1.4 AMPEX 230 SPECIFICATIONS

The following is a list of operating characteristics and specifications for the Ampex 230 terminal.

Display Screen
14-inch nonglare screen
Green or amber phosphor
60 or 65 Hz refresh rate (operator-selectable)

Displayed Character Set
238 displayable characters
96 ASCII characters
32 control characters
15 line graphic characters
64 block graphic characters
31 national characters
24 data lines; 1 status line; 1 user-programmable line
2 display pages standard (optional 3rd and 4th pages)

Character Typestyle
7 x 10 dot matrix in a 9 x 12 dot field

National Character Sets
United States/United Kingdom
German
French
Swedish
Danish
Norwegian
Italian
Spanish

Video Attributes
Flash
Blank (security)
Reverse video
Underline
Half-intensity

Cursor
Block or underline
Flashing or Steady
No cursor
Readable and addressable

Cursor Control Keys
↑, ↓, ←, →, Home, Tab, Back Tab, Return,
Linefeed, Backspace

Keyboard
Low profile 30 mm DIN Standard
16 programmable function keys (32 shifted)
Audible keyclick (selectable on/off)
Adjustable slope of 7, 11, and 15 degrees
Detached, with coiled cable
Separate numeric keypad
Separate editing keys
Step-sculptured, selectric-type layout

Edit Keys
Line insert/delete
Character insert/delete
Erase to end of line
Erase to end of page

Emulations
Ampex 230, 210, D175, D150E, D150, D125, D80, D81, D30
TeleVideo 950, 925, 924/914
Wyse WY-50

Operating Modes
Full-duplex/half-duplex
Conversation, block, local
Protect, write protect
Programmable Function Key
Monitor
Set-up (operator-selectable operating parameters via status line displays)
Split Screen
Extended Page
132-column
Double-size characters
Jump Scroll
Smooth Scroll (4 speeds)
Auto-Flip

Primary Port and Printer Port Data Transmission Rates (Independently-selectable)
50, 75, 110, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19,200, and 38,400 bits per second

Interfaces
Primary Port - RS232C (Standard) serial port
RS422 (customer-installable option)
Current Loop (customer-installable option)
Auxiliary Port - RS232C serial port

Regulatory Compliance
FCC Class A (United States)
UL (United States)
CSA (Canada)

Printer Functions
Local print (page print)
Transparent print
Extension (copy) print
Unformatted print
Bidirectional port on/off

Operating Environment
Temperature: 32°F to 104°F (0°C to 40°)
Humidity: 5% to 95%

Physical Dimensions

	Display Unit	Keyboard
Width:	13.5 in. (343 mm)	19.0 in. (483 mm)
Depth:	13.5 in. (343 mm)	7.5 in. (191 mm)
Height:	14.5 in. (369 mm)	1.5 in. (38 mm)
Weight:	19.4 lb (8.7 kg)	2.0 lb (0.9 kg)

Power Requirements
115 vac (+10%, -15%) at 0.5 amp, 60 Hz
230 vac (+10%, -15%) at 0.25 amp, 50 Hz

Transmission Protocol
XON/XOFF
DTR High/DTR Low

1.5 AMPEX 219 SPECIFICATIONS

The following is a list of operating characteristics and specifications for the Ampex 219 terminal.

Display Screen
14-inch nonglare screen
Amber or green phosphor
60 or 65 Hz refresh rate (operator-selectable)

Displayed Character Sets
174 displayable characters
96 ASCII characters
32 control characters
32-special character and line graphic set
24 data lines; 1 user line; 1 status line
2 display pages standard (optional 3rd and 4th pages; user-installable)
Double-high/double-wide characters

Character Typestyle

7 x 10 dot matrix in a 9 x 12 dot field

National Character Sets
United States
Denmark
France
Germany
Italy
Norway
Spain
Sweden
United Kingdom

Video Attributes
Blink, Reverse Video
Half-intensity, Underline (combination)

Cursor
Block or underline
Flashing or steady
Cursor On/Off
Readable and addressable

Keyboard
Low profile 30mm DIN Standard
16 programmable function keys
Audible keyclick (selectable on/off)
Adjustable slope of 7, 11, and 15 degrees
Detached, with coiled cable
Separate numeric keypad
Separate editing keys (VT-131 compatible)
Step-sculptured, selectric-type layout
4 PF keys (general purpose function keys)

Cursor Control Keys
↓, ↑, ←, →, Home, Tab, Back Tab, Return, Linefeed, Backspace, Enter

Edit Keys
Line Insert/Delete
Character Insert/Delete

Emulations
Ampex 219
DEC VT131, VT100/VT102, VT52
WY-75

Operating Modes
Full-duplex/half-duplex
Conversational, block (edit), local
Set-up, monitor

Display Format
80 or 132 column display
24-48 lines/page (96 lines/page optional)
Split screen
Auto-paging
Jump Scroll
Smooth Scroll (4 speeds)

Primary Port and Printer Port Data Transmission Rates (Independently-selectable)
50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19,200, 38,400 bits per second

Interfaces
Primary Port - RS232C (Standard) serial port
  RS422 port (customer-installable option)
  Current loop interface (customer-installable option)
Auxiliary Port - RS232C serial port

Printer Functions
Print screen
Auto print
Transparent print (Printer Controller)
Print cursor line

Operating Environment
Temperature: 32°F to 104°F (0°C to 40°C)
Humidity: 5% to 95%

SECTION II
INSTALLATION

2.1 INTRODUCTION

The Ampex 230/219 Video Display Terminals may be operated in a wide variety of physical environments. The remainder of this section provides explanations and diagrams to assist the user during installation of these terminals.

2.2 SERIAL PORT INTERFACE

The Ampex 230/219 terminals use standard RS232C serial port interfaces for both the primary and printer ports.

2.2.1 Primary Port Interface

Table 2-1 provides interface pin signal assignments of the primary port.

Table 2-1. Primary Port Pin Signal Assignments

Pin No.	Signal Name	Signal Direction
1	Chassis ground	
2	Transmit Data Output	From Terminal
3	Receive Data Input	To Terminal
4	Request-to-Send Output	From Terminal
5	Clear-to-Send Input	To Terminal
6	Data-Set-Ready Input (optional)	To Terminal
7	Signal Ground	
8	Data Carrier Detect	To Terminal
20	Data-Terminal-Ready Output	From Terminal

Definitions Of The Primary Port Pins - The primary port conforms to the RS232C standard set forth by the EIA for a DTE.

Pin 20 - Data Terminal Ready - This pin is made active by the terminal when it is ready to receive or transmit data. If DTR handshaking protocol is selected via the Set-up menu, then Pin 20 can be used to control the flow of data from the host. Pin 20 becomes inactive when the input buffer is 50% full.

Pin 6 = Data Set Ready - The terminal expects this pin to be active before data can be either transmitted or received.

Pin 5 = Clear to Send - The terminal expects this pin to be active before data can be transmitted.

Pin 8 = Data Carrier Detect - The terminal expects this pin to be active before data can be received.

Pin 2 = Transmit Data Output - The terminal uses this pin to transmit data to the host.

Pin 3 = Receive Data Input - The terminal uses this pin to receive data transmitted by the host.

Pin 4 = Request to Send - The terminal makes this pin active prior to the transmission of data to the host in half-duplex mode. In full-duplex mode, this pin is kept active at all times.

Pin 7 = Signal Ground - The terminal uses this pin as a reference by where the other pins are judged active or inactive.

NOTE: If a pin is not connected it will be considered active.

2.2.2 Printer Port Interface

Table 2-2 provides pin signal assignments for the printer port.

Table 2-2. Printer Port Pin Signal Assignments

Pin No.	Signal Name	Signal Direction
1	Chassis ground	
2	Transmit Data Output	To Terminal
3	Receive Data Input	From Terminal
4	Request-to-Send Output	To Terminal
5	Clear-to-Send Input	From Terminal
6	Data-Set-Ready Input	From Terminal
7	Signal Ground	
8	Data Carrier Detect	From Terminal
20	Data Terminal Ready	To Terminal

Definitions of the Printer Port Pins - The printer port conforms to the RS232C standard set forth by the EIA for a DCE.

Pin 20 = Data Terminal Ready - The terminal will transmit/receive data to/from the printer port device when this pin is made active by the printer port device.

Pin 2 = Transmit Data Output - The terminal expects to receive data transmitted by the printer port device.

Pin 3 = Receive Data Input - The printer port device receives data transmitted by the terminal/host.

Pin 7 = Signal Ground - The terminal uses this pin as a reference by where the other pins are judged active or inactive.

2.3 USER-INSTALLABLE OPTIONS

The Ampex 230/219 allow alternatives to the standard RS232C interface at the primary port. These user-installable options are:

RS422 Interface
Current Loop Interface

These options are available in kits provided by Ampex and may be ordered through your Ampex Sales Representative. Part numbers for these kits are as follows:

RS422 Interface Kit - Ampex Part No. 3515412-02A
Current Loop Interface Kit - Ampex Part No. 3515413-02A

Refer to Appendix A for installation instructions on these user-installable options.

2.4 INSTALLATION REQUIREMENTS

The Ampex 230/219 terminals are designed to be placed on a flat, hard surface such as a desk or table top capable of supporting at least 22 pounds (10 kg). Ambient temperature of the operating environment must be within 32° F to 104° F (0° to 40° C) range.

CAUTION

Do not block any of the air vents on the unit. All air vents of the terminal case must be kept clear in order to provide proper cooling during operation.

2.4.1 Space Allocation

The detached keyboard permits considerable flexibility in positioning the unit for use. Figure 2-1 illustrates the terminal's overall dimensions as well as the minimum surface area required for installation.

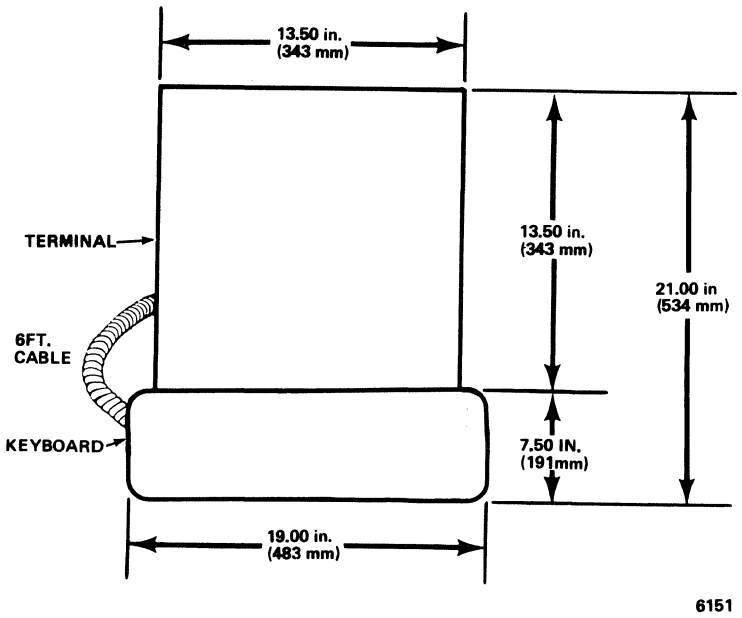


Figure 2-1. Overall Dimensions

2.4.2 Input Power

The Ampex 230/219 are configured at the factory for either 115 or 230 volts alternating current (vac). Installation site power requirements for both versions are listed in Table 2-3.

Table 2-3. Input Power Requirements

Version	Phasing	Frequency	Current
115 vac +10% -15%	Single Phase	60 Hz ±3%	0.50 A
230 vac +10% -15%	Single Phase	50 Hz ±3%	0.25 A

WARNING

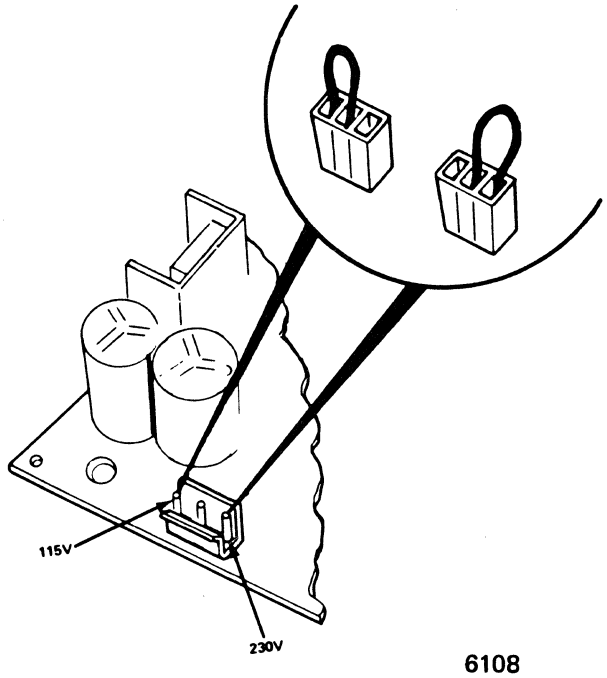
High voltage is present within the case when power is on. Remove the power cable from the ac receptacle before removing the top cover. Only authorized service personnel should open the case.

The Ampex 230/219 may be strapped for 115 or 230 volts. Figure 2-2 contains drawings showing the two versions of the strapping plug. Refer to these drawings when changing the voltage from 115 volts (applicable in the United States) to 230 volts (applicable outside the United States) or vice versa.

NOTE

The fuse, located in the fuseholder on back panel of the display unit (Figure 2-3), must be changed when the voltage is changed. For:

115 volts - Use a 2A fuse
230 volts - Use a 1A fuse



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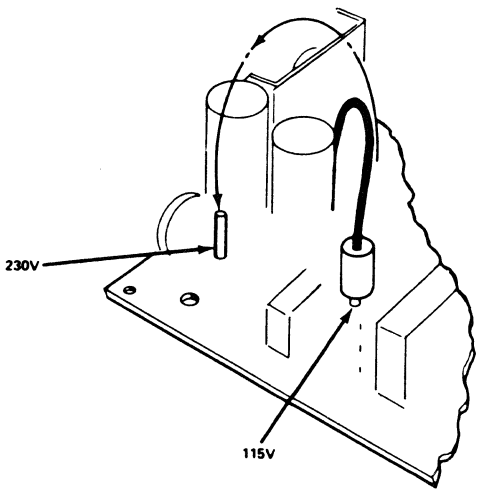
Version 1



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Version 2

Figure 2-2. Voltage Strapping Plug (Versions 1 and 2)

2.4.3 AC Power Cord and Plug

Each terminal is shipped with either a 115 vac/60 Hz power plug (for use in the United States) or a 230 vac/50 Hz power plug (for use outside the United States). Ampex 230/219 terminals in the United Kingdom and Australia may need customized power plugs to fit the receptacles in these countries.

WARNING

Electric shock may result if the power cord is connected to AC power when the plug is cut off for Be sure to disconnect the cord from AC power before customizing the power plug.

2.4.4 Interface Cable Connections

Figure 2-3 is a view of the back panel of the Ampex 230/219 Video Display Terminals. Refer to this figure when attaching the primary port (to computer) and the auxiliary port (to printer) interface cables.

2.4.5 Keyboard Port Connection

Figure 2-4 shows the location of the keyboard cable port. Refer to this figure when attaching the keyboard cable to the display terminal.

CAUTION

Do not connect or disconnect the keyboard to or from the display unit when the power is on. Erratic performance may result.

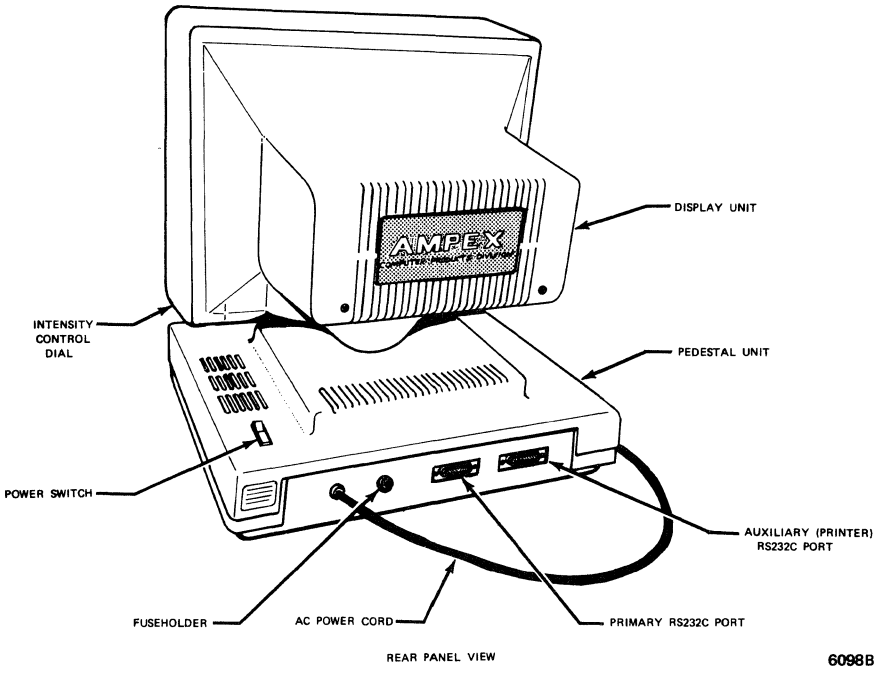


Figure 2-3. Ampex 230/219 Video Display Terminal (Back Panel View)

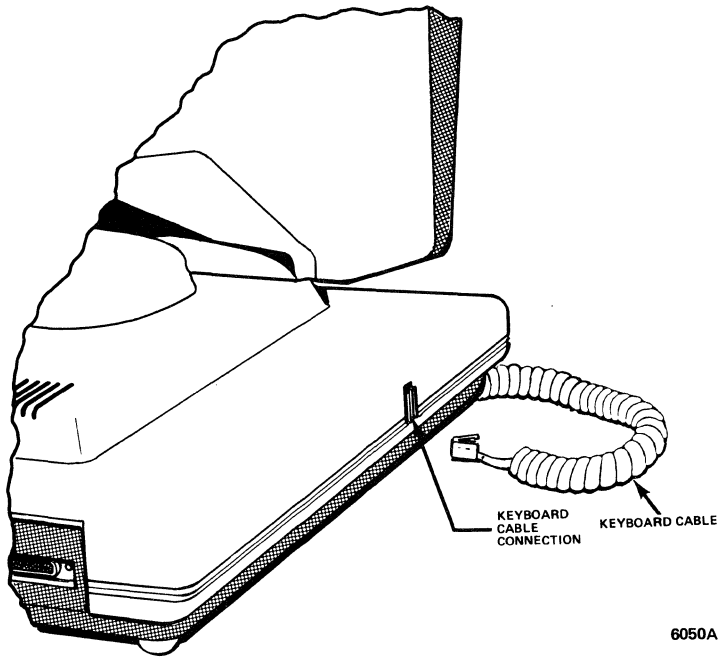


Figure 2-4. Keyboard Port on Display Terminal

2.5 POWER-ON AND RESET

To power on the terminal:

1. Make sure all interface cables are connected properly to their respective ports (refer to 2.4.4 Interface Cable Connections and 2.4.5 Keyboard Port Connection).

2. Make sure the power cable is plugged into the proper outlet (refer to 2.4.3 AC Power Cord and Plug).

3. Set the on/off switch to on.

4. Within seconds, the unit undergoes its self-test.

5. After the self-test is completed, a "beep" will sound and the cursor will appear in the top left-hand corner of the screen.

6. Adjust the intensity by rotating the intensity control dial, located underneath the right-hand portion of the display unit.

7. The terminal is now ready to begin performing the operations described in the remaining sections of this manual.

To reset the terminal while performing normal operations, press CTRL/SHIFT/RESET.

2.6 SELF-TEST

The self-test feature is activated each time the terminal is powered on. For the most part, the test pattern on the screen cannot be viewed at initial power-on. To view the test pattern, initiate a self-test while the terminal is already "on" by entering Set-up mode (refer to Section IV) and typing "1".

The self-test operation checks the following:

CMOS RAM (a check sum of the terminal set-up information)
DATA RAM
DISPLAY RAM
ROM
VISUAL ATTRIBUTES (displays on the test pattern)

Result of Terminal Self-Test

A test pattern will display, showing all character sets, visual attributes, firmware version number, and copyright information. If any component errors are detected, a message will display in the lower portion of the screen.

NOTE

Some characters may display which are not accessible using the standard firmware.

Possible error messages are:

CMOS CHECKSUM ERROR
DATA RAM ERROR
DISPLAY RAM ERROR
ROM ERROR

If any of the above error messages display on the screen:

1. Press CTRL/SHIFT/RESET to reset the terminal.

2. Enter Set-up mode and set the parameters. Press SHIFT/S to save the parameters and exit Set-up mode.

3. Enter Set-up mode again. Type: 1
   (System will undergo another self-test procedure.)

4. Verify any error messages:

   a. If the error message no longer displays, the terminal is ready to operate.

   b. If the error message still displays, contact an Ampex service location immediately. Do not attempt to correct the problem.

5. Press CTRL/SHIFT/RESET to reset the terminal and clear the screen.

NOTE: Ampex service locations are listed on the Warranty Information sheet included in the box with the terminal.

SECTION III
THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the theory of operation of the major subassemblies of the Ampex 230/219 terminals.

3.2 GENERAL DESCRIPTION

The basic block diagram in Figure 3-1 illustrates signal flow between the subassemblies of the terminal. The following paragraphs discuss the interfacing of subassemblies.

3.3 OPERATION AND COMPONENTS OF THE TERMINAL CONTROLLER PWBA

The hardware and circuitry of the controller PWBA is composed of the major functional blocks, input/output mapping, and interface buses shown in Figure 3-2.

Functional sections of the terminal are controlled by the Central Processing Unit (CPU) via a system data bus, an address bus, and control lines. Display and communications sections have some circuitry that run independently of the CPU. The display section, for example, refreshes video continuously and automatically once initiated by the CPU.

The host computer communicates with the terminal via an RS232C interface. The CPU receives serial data from the keyboard via a keyboard interface circuit resident in the Cathode Ray Tube (CRT) controller chip.

The CPU is a Z80A microprocessor with fully-enhanced 8080-like instruction set. The hardware, as designed, uses Input/Output (I/O) instructions to access the I/O ports.

There are two interrupt sources. The maskable interrupt is generated by a Z80A DART chip and the non-maskable interrupt is generated by a PVTC (Programmable Video Timing Controller) chip.

The data/address buses and control lines allow the CPU to access the program ROM, the scratch pad RAM, and all of the I/O ports. Depending on firmware requirements, 16K to 32K bytes of program P/ROM can be installed.

The CPU's scratch-pad and data memory consists of a 2K x 8 CMOS RAM and provides nonvolatile storage of all of the set-up parameters including optional modes, communication parameters, emulation parameters, etc., through the use of a 3V lithium battery.

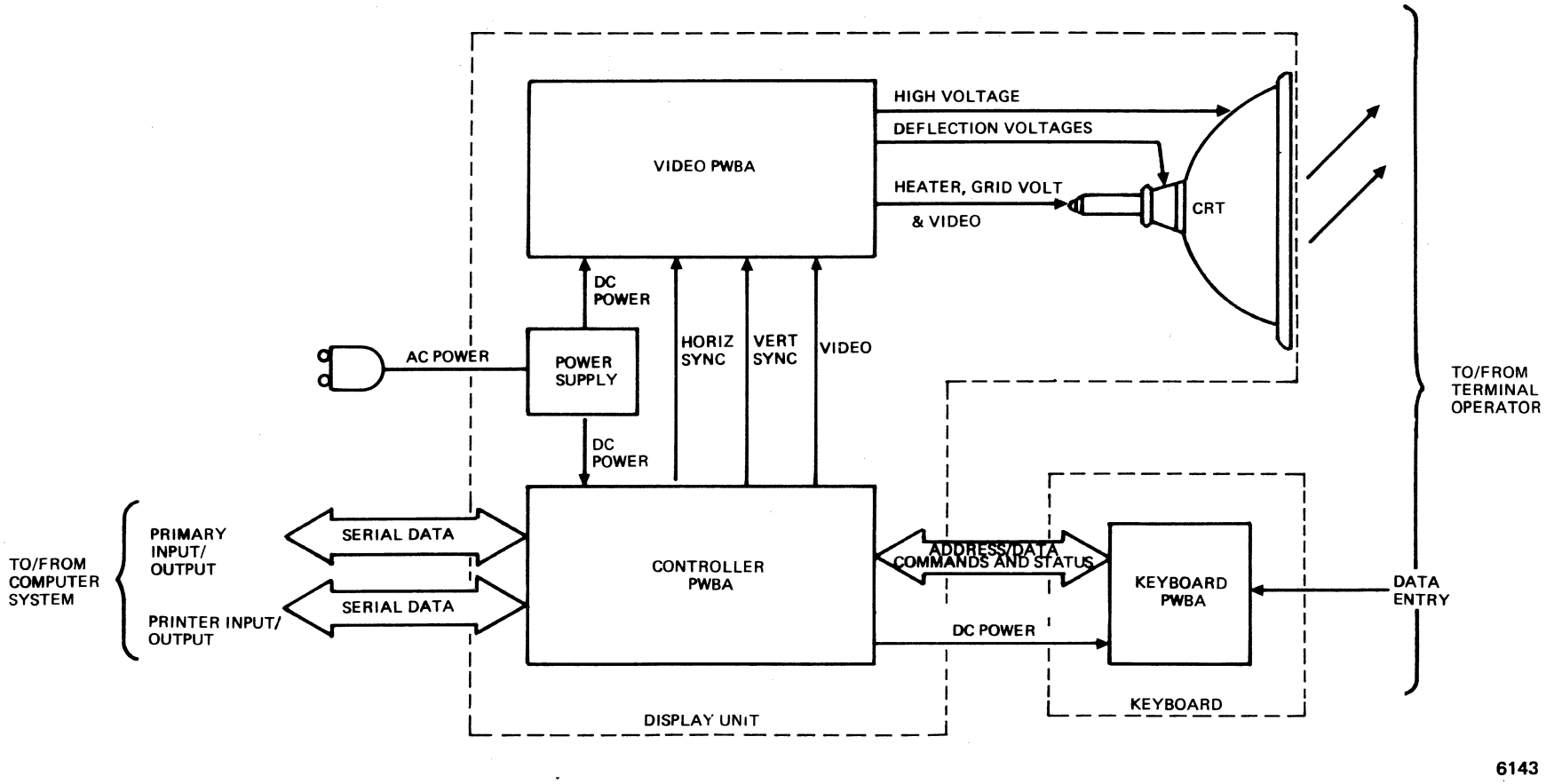


Figure 3-1. Terminal Basic Block Diagram

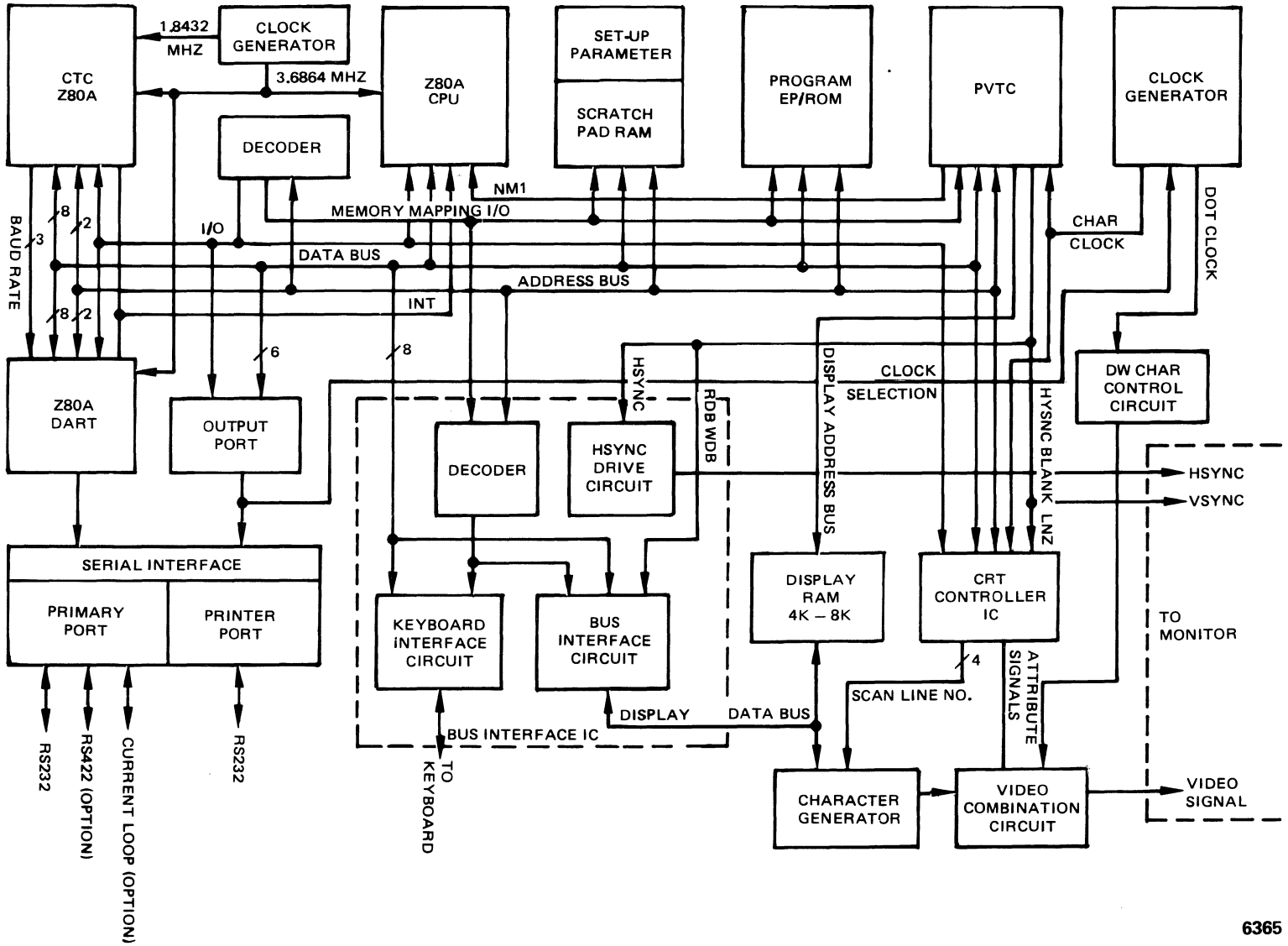


Figure 3-2. Controller PWBA Block Diagram

3.3.1 Input/Output Mapping and the CPU

Through I/O mapping, the CPU interfaces with:

PVTC chip
Z80A DART chip and other communications-related circuitry
Keyboard (via bus interface chip)
CRT controller chip
Bus interface chip
Z80A-CTC chip

3.3.1.1 Display I/O

Display I/O gives the CPU control over the PVTC chip (including initializing the PVTC chip, reading/writing cursor position, flashing clock, and scrolling).

Once initialized by the CPU, the PVTC chip subsequently performs the continuous refreshing required of the PVTC by generating the video, horizontal drive, and vertical sync signals required by the CRT monitor.

3.3.1.2 Communication I/O

The communication I/O gives the CPU control over the Z80A DART chip (including sending/receiving characters on the word level and checking Z80A DART status) and other communications circuitry (including primary/printer port selection and bidirectional/extension printer port selection).

Once initialized by the CPU, the Z80A DART chip and other communications circuitry subsequently perform the parallel-to-serial, serial-to-parallel, and signal level conversions required for serial port interfacing.

A Z80A-CTC chip is needed to generate the baud rate for the Z80A DART.

3.3.1.3 Keyboard I/O

The keyboard I/O allows the CPU via the bus interface chip to transmit and receive data to and from the keyboard.

3.3.2 Central Processing Unit

The CPU is the control center of the terminal controller. The following paragraphs describe the functions of the CPU, the buses, and memory interfaces used to control other parts of the system.

3.3.2.1 Functions of the CPU

As mentioned earlier, the CPU is a Z80A microprocessor. It contains circuitry for program execution as well as the program registers:

Clock - The CPU clock is a 3.6864 MHz generated from a 3.6864 MHz crystal. The clock input to the Z80A requires special high level generation by a 74LS04 driver (U32) and a 1K ohm resistor (R34).

Reset - The CPU is reset by the power-up reset circuit or power-down reset circuit.

Memory Request (MREQ) - At the beginning of each cycle, an MREQ is issued. The MREQ is used to enable the decoding circuitry (U46) to generate chip select signals.

Read/Write Signals - Following the MREQ for each memory-mapped I/O read/write cycle, a Bus read or write signal occurs when a byte is to be read from or written to memory or memory-mapped I/O.

Input/Output Request (IORQ) - The IORQ is used to enable the I/O port function.

Maskable Interrupt - Maskable interrupt of the CPU is generated by the Z80A DART chip. There are three types of maskable interrupts: Receive Data Register Full, Transmit Data Register Empty, or External/Status interrupt.

Non-maskable Interrupt - Non-maskable interrupt input of the CPU is generated by the PVTC chip. There are two possible causes of non-maskable interrupts: Vertical Blank or Line Zero.

3.3.2.2 Buses Used for Interfacing

During the CPU's read memory or write memory, the Data/Address bus signal lines carry address information to the other components and data information to or from those components.

Data Bus - The CPU's eight data lines, D7 through D0, carry the data between the CPU and all of the memories and I/O devices.

Address Bus - There are sixteen address lines, A0 through A15, used to address the memories and I/O ports. In general, the lower address lines are used to address specific bytes in the program P/ROM and the data RAM. The highest address bits select between the system entities.

3.3.2.3 Memory Interfaces

The following paragraphs contain descriptions of the various memory interfaces:

Program ROM/PROM - The program instruction memory can be configured out of various types of numbers of ROMs/PROMs. The total memory space is 32K. Table 3-1 shows the various jumper settings and IC (Integrated Circuit) locations for select memory capacity.

Table 3-1. Program Instruction Memory Configurations

Jumper Settings	Total Memory	Address Ranges for Access	IC Location	IC Type	Memory for each IC
W16-W17 W20-W21	16K	0 - 3FFF	U34	27128/23128	16K
W16-W17 W20-W21	20K	0 - 3FFF 4000 - 4FFF	U34 U35	27128/23128 2732/2332	16K 4K
W16-W17 W20-W21	24K	0 - 3FFF 4000 - 5FFF	U34 U35	27128/23128 2764/2364	16K 8K
W16-W17 W20-W21	32K	0 - 3FFF 4000 - 7FFF	U34 U35	27128/23128 27128/23128	16K 16K
W17-W18 W19-W20	32K	0 - 7FFF	U34	27256/23256	32K

Data RAM - Depending on terminal configuration, the data RAM can consist of 2K or 8K bytes static CMOS random-access memory.

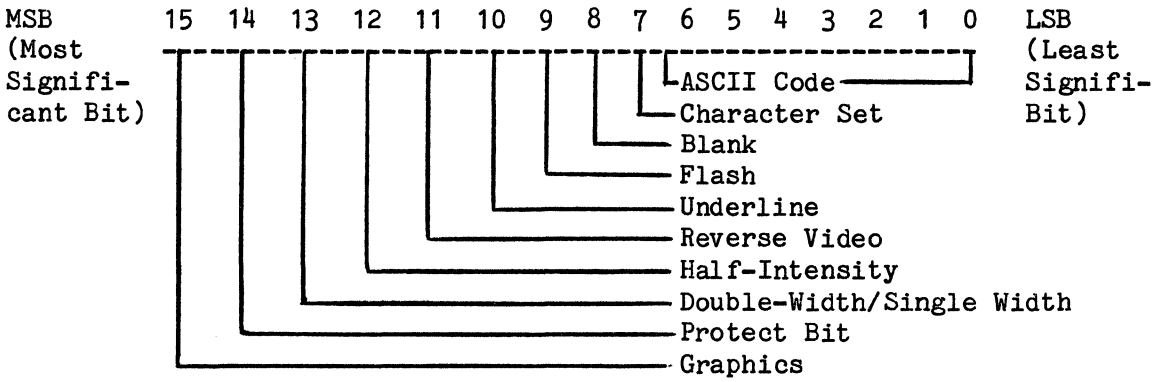
Jumper Settings	Address Ranges for Access	IC Type	Memory for each IC
W11 - W12	C000 - C7FF	5517	2K
W10 - W11	C000 - DFFF	5565	8K

The data RAM is split into two different regions. The first region is used as memory for the programmable function keys and as software switches defining the terminal's default states. The second region is used as the CPU's scratch-pad RAM.

Display RAM - Depending on terminal configuration, there are either two or four pages of display memory. Jumper settings are as follows:

Total Pages	Jumper Settings	Address Ranges for Access	IC Location	IC Type	Memory for each IC
(For PCB 3515400)					
2	W7 - W9 W2 - W3 W5 - W6	0 - 07FF 800 - 0FFF	U17, U23 U18, U24	2016 2016	2K 2K
4	W8 - W9 W1 - W2 W4 - W5	0 - 1FFF	U17, U23	5565	8K
(For PCB 3515455)					
2	W7 - W8 W1 - W2 W4 - W5	0 - 7FF 800 - 0FFF	U17, U23 U18, U24	2016 2016	2K 2K
4	W7 - W9 W2 - W3 W5 - W6	0 -1FFF	U17, U23	5565	8K

Each character contains 16 bits:



The seven least significant bits contain the ASCII character to be displayed in that character position. The other nine bits affect how that character is actually displayed: one bit selects the graphic character set, one bit represents protected data, one bit determines the character size, and five bits determine the visual attributes.

In field (or embedded) attribute emulation, bits 11 through 8 are not used. For the attribute delimiter, the pattern of bits 15, 14, 7, 6, and 5 should be 01000. When a TeleVideo terminal is being emulated, bit 4 should be 0. Visual attributes are activated when the corresponding bit; 4, 3, 2, 1, or 0 is set to "1." Table 3-2 defines each bit of an attribute delimiter.

Table 3-2. Attribute Delimiter Bits

Bit	Definition
4	Half-Intensity (Wyse WY-50 emulation)
3	Underline
2	Reverse Video
1	Flash
0	Blank

Transfer of data between the CPU and the display RAM is accomplished via the memory interface circuit resident in the bus interface chip and is controlled by the PVTC signals: Read Data Buffer and Write Data Buffer.

3.3.3 Operation of CPU Memory

The general theory of operation of the hardware for program memory is described in the following paragraphs.

3.3.3.1 Program ROM/PROM

The program ROM/PROMs are static and begin their access time as soon as the address lines are valid (i.e., they access continuously). The ROM/PROM drive the main data bus directly so that the access time from address valid to data out is 350 nsec, maximum. The upper memory address bits are used to select and enable the specific ROM/PROM's data outputs using pin 20 of the selected IC.

3.3.3.2 Data RAM

The CMOS RAM is used together with a long life (10 years minimum) 3.4V lithium battery for nonvolatile storage of modes of operation. The CMOS RAM write enable pin goes directly to the CPU's WR pin (U24-U22). When AC power is off, the CMOS RAM will draw standby current from the 3.4V battery. When AC power is on, the CMOS RAM will draw current from the +5V supply.

3.4 OPERATION OF DISPLAY CIRCUITRY

The following paragraphs discuss the operation of programmable video timing controller and display circuitry. Figure 3-3 is a block diagram of the Video PWBA.

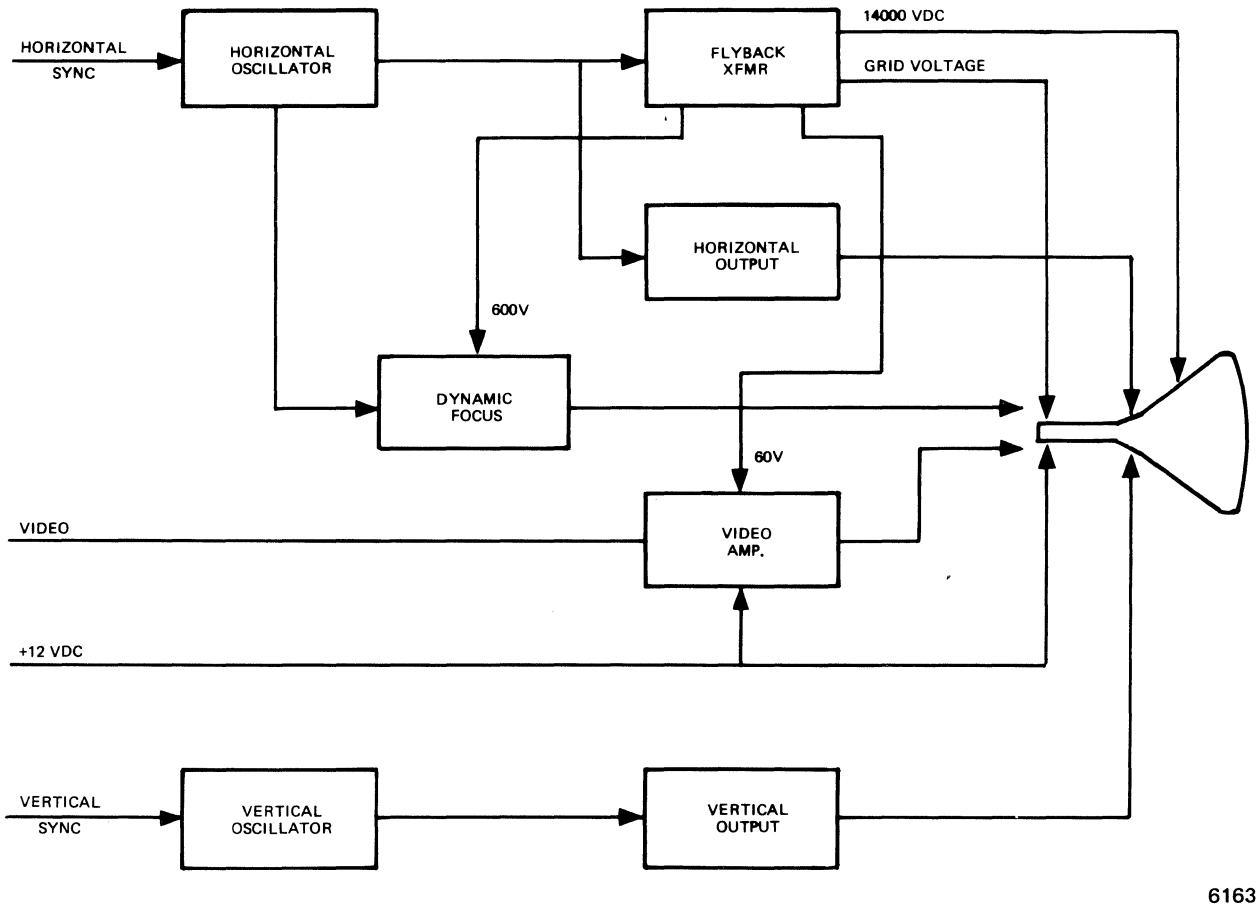


Figure 3-3. Video PWBA Block Diagram

3.4.1 General Information

The characters displayed on the screen are accessed (read and written) by the CPU via the display RAM. Memory can be two or four pages of 1,920 sixteen-bit words each and separate status and user lines of 80 sixteen-bit words each. In the 16 bits of display RAM location, five bits determine the attribute (underline, flash, blank, reverse video, or half-intensity), one bit determines the character size, one bit represents the protect flag, and one bit selects the international character set for each corresponding character as defined in the remaining eight bits.

The display RAM requires that the Programmable Video Timing Controller (PVTC) be properly controlled by the CPU for transferring data to and from the display RAM.

3.4.2 Operation of the PVTC Chip

The Programmable Video Timing Controller (PVTC) chip is accessed by three control strobes: Chip enable, CPU read, and CPU write signals. The 8000H decode output of the upper address lines provide the chip select for the PVTC. The lower three address lines (A0-A2) and read/write signals go to the PVTC chip for initialization register selection.

In order to attain the 26 data lines at 60 or 65 Hz refresh rate, the initialization registers (IR0-IR10) are loaded by the firmware as shown in Table 3-3.

Table 3-3. PVTC Chip Initialization Register Selection

Initialization Registers	Value (In Hex)			
	60 Hz		65 Hz	
	80 Col	132 Col	80 Col	132 Col
IR0	58	58	58	58
IR1	1D	1D	1D	1D
IR2	21	60	21	60
IR3	8C	8C	26	26
IR4	19	19	19	19
IR5	4F	83	4F	83
IR6	0B	0B	0B	0B
IR7	2B	2B	2B	2B
IR8	00	00	00	00
IR9	40	40	40	40
IR10	99	99	99	99

Note that there are 11 initialization registers which are accessed sequentially via a single address (08000). The PVTC maintains an internal pointer to these registers which is incremental after each write at this address until the last register (IR10) is accessed. This internal pointer can also be preset to any register of the group by loading a value from 10H to 1AH to PVTC command register (08001).

3.4.3 Initialization Register Parameters

Parameters of the initialization register values indicated in Table 3-3 are:

Initialization Register 0 (IR0)

Bit 7, not used (=0)
Bits 6 - 3 = N; Scan lines/character row (where scan lines/character row = N + 1)
Bit 2 = 0; sync select (VSYNC)
Bit 1 - 0 = 00; buffer mode select (independent mode)

Initialization Register 1 (IR1)

Bit 7 = 0; non-interlace
Bits 6 - 0 = N; equalizing constant (where equalizing constant = N + 1)

Initialization Register 2 (IR2)

Bit 7 not used (=0)
Bits 6 - 3 = N; horizontal sync width (where horizontal sync width = 2 * N + 2)
80 Col - horizontal sync width = 2 * 4 + 2 = 10 CCLK
132 Col - horizontal sync width = 2 * 12 + 2 = 26 CCLK
Bits 2 - 0 = T; horizontal back porch (where horizontal back porch = 4 * T + 1)
80 Col - horizontal back porch = 4 * 1 + 1 = 5 CCLK
132 Col - horizontal back porch = 4 * 0 + 1 = 1 CCLK

Initialization Register 3 (IR3)

Bits 7 - 5 = N; vertical front porch (where vertical front porch = 4 * N + 4)
60 Hz: vertical front porch = 4 * 4 + 4 = 20 (scan lines)
65 Hz: vertical front porch = 4 * 1 + 4 = 8 (scan lines)
Bits 4 - 0 = T; vertical back porch (where vertical back porch = 2 * T + 4)
60 Hz: vertical back porch = 2 * 12 + 4 = 28 (scan lines)
65 Hz: vertical back porch = 2 * 6 + 4 = 16 (scan lines)

Initialization Register 4 (IR4)

Bit 7 = 0; character blink rate = 1/16 VSYNC
Bits 6 - 0 = N; character row/screen (where character row/screen = N + 1)

Initialization Register 5 (IR5)

Bits 7 - 0 = N; character/row (where character/row = N + 1)
80 Col - character/row = 4F (H) + 1 = 50 (H) = 80
132 Col - character/row = 83 (H) + 1 = 84 (H) = 132

Initialization Register 6 (IR6)

Bits 7 - 4 = N; first line of cursor (scan line 0)
Bits 3 - 0 = T; last line of cursor (scan line 11)

Initialization Register 7 (IR7)

Bits 7 - 6; not used (=0)
Bit 5 = 1; cursor blinking
Bit 4 = 0; normal size character
Bits 3 - 0 = N; underline position (scan line 11)

Initialization Register 8 (IR8)

Bits 7 - 0 = display buffer first address Least Significant Bits
= 00H

Initialization Register 9 (IR9)

Bits 7 - 4 = N; display buffer last address (where display buffer
last address = 1024 x N + 1023)
Bits 3 - 0 = display buffer first address Most Significant Bits = 0

Initialization Register 10 (IR10)

Bit 7 = 1; cursor blink rate = 1/32 VSYNC
Bits 6 - 0 = N; split screen interrupt row = 19 (H) = 25

3.4.4 Valid Address/Blanking and Sync Signals Relationship

Figures 3-4 and 3-5 illustrate the timing of a frame (80 columns and 132 columns respectively) showing the relationship between the valid character address and the blanking and sync signals. The left and right edges correspond to the start of the horizontal sync and the top and bottom edges (different for 60 and 65 Hz) correspond to the start of the vertical sync.

The inner solid-lined rectangle (26 character rows x 80/132 characters) represents the time during which the PVTC chip outputs valid address on DADD0 - DADD12. The DADD0 - DADD12 lines range from 0 to 79/131 on each scan across the 80/132 character positions counting out the 26 character rows, covering rows 0 through 25 on each frame. The CRT controller IC presents the scan line number or LA0 - LA3, covering all rows 0 through 25 on each frame.

The positive-true blanking signal is emitted with no character time delays after the end of the last character to the beginning of the first character address, as well as continuously from the end of the last character row until the beginning of the first character row.

3.4.4.1 Horizontal Sync

The horizontal sync (HSYNC) is delayed by five characters (as blanking) and additionally has a "back porch" of five characters (for 80 columns) or one character (for 132 columns) after the HSYNC ending. The HSYNC signal width is ten characters long for 80-column display or 26 characters long for 132-column display.

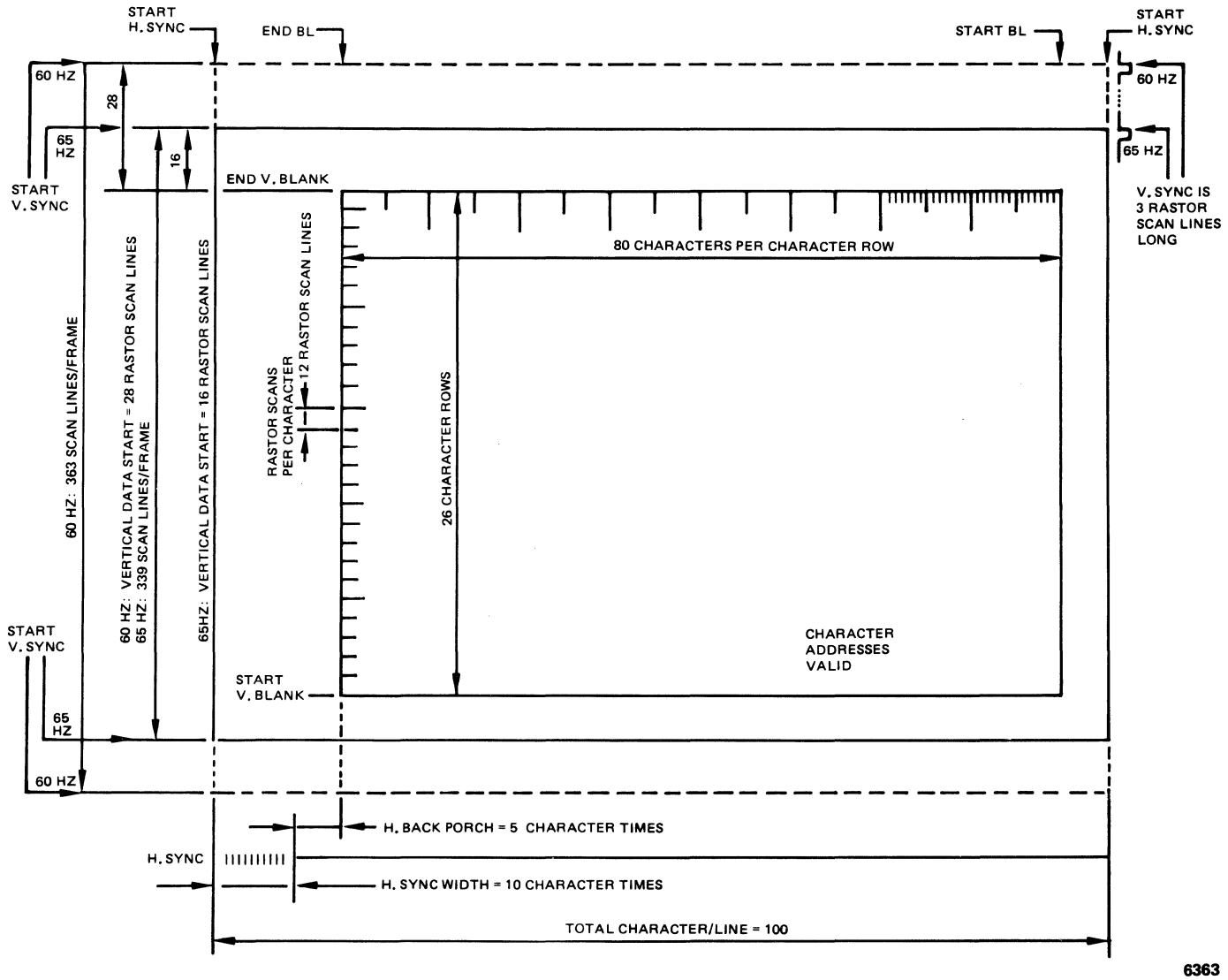


Figure 3-4. PVTC Chip Timing Frame (80 Column x 26 Lines)

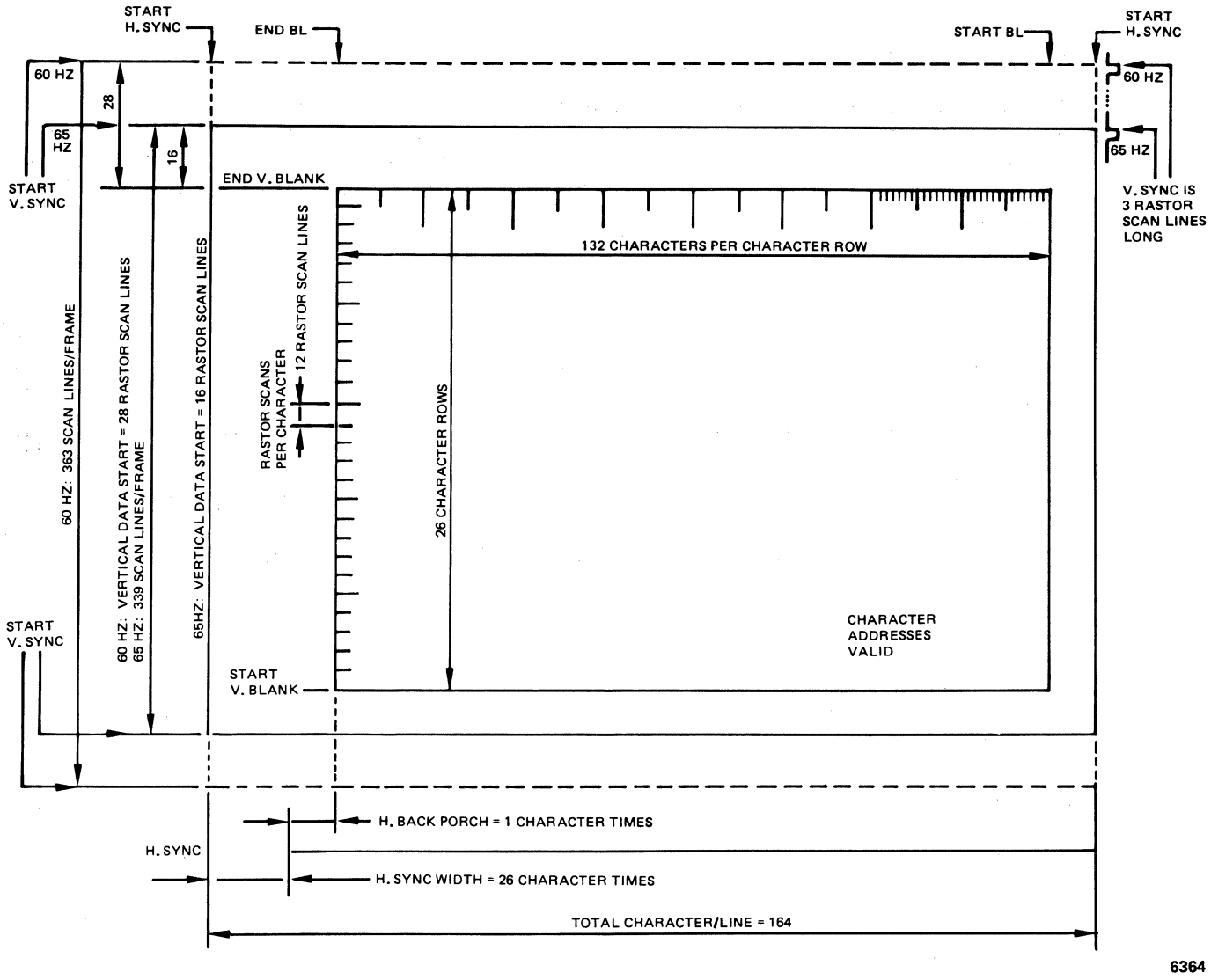


Figure 3-5. PVTC Chip Timing Frame (132 Columns x 26 Lines)

3.4.4.2 Vertical Sync

The vertical sync (VSYNC) starts after the last scan line of the frame and continues for three horizontal scan lines. The programming of the total scan lines per frame determines whether there are 60 or 65 frames per second. Following the last scan line (at the same time the VSYNC starts), the vertical character row start is delayed by 28 scan lines for 60 Hz and 16 scan lines for 65 Hz. This variation provides for approximately the same vertical centering for both 60 Hz and 65 Hz.

3.4.4.3 Cursor Signal

The cursor signal is emitted during the time when the internal cursor address matches the screen address (DADD0 - DADD12).

3.5 OPERATION OF THE DISPLAY RAM

Displayed characters and attribute control characters are stored in and received from either 2K x 8 or 8K x 8 S/RAMs. The PVTC chip generates three control signals: Buffer Chip Enable, Write Data Buffer, and Read Data Buffer. These signals provide the transfer of data between the CPU and the display RAM (via the interface circuits resident in the Bus Interface chip).

3.6 CHARACTER GENERATOR

The four least significant address bits of the character generator are derived from the scan line address bits of the CRT controller IC chip. During actual display, the seven ASCII bits address a "character generator ROM" which allows the specifications of a 7 x 10 dot matrix to be displayed within the 9 x 12 field as shown below. Thus, each 9-bit data word can select any one of 512 character-generated ROM patterns to fill in the 7 x 10 dot matrix.

The display character field has the following format:

	COLUMN									
ROW	0	1	2	3	4	5	6	7	8	
0	X	X	X	X	X	X	X	X	X	Blank*
1	X	A	A	A	A	A	A	A	X	Top Scan Row
2	X	A	A	A	A	A	A	A	X	Character Scan Row
3	X	A	A	A	A	A	A	A	X	"
4	X	A	A	A	A	A	A	A	X	"
5	X	A	A	A	A	A	A	A	X	"
6	X	A	A	A	A	A	A	A	X	"
7	X	A	A	A	A	A	A	A	X	"
8	X	A	A	A	A	A	A	A	X	"
9	X	A	A	A	A	A	A	A	X	"
10	X	A	A	A	A	A	A	A	X	Bottom Scan Row
11	-	-	-	-	-	-	-	-	-	Blank **

*Row 0 is always blank, except for graphics.
**Row 11 is always blank, except for graphics and underlines.

The bit maps for character scan line display matrices have this format:

For normal characters:	B	D7	D6	D5	D4	D3	D2	D1	B	0 (00=0)
For graphics characters:	D7	D7	D6	D5	D4	D3	D2	D1	D1	1 (D0=1)

3.7 GENERATION OF VIDEO SIGNALS

At the end of each character generator access, the dot data are loaded into a shift register in order to begin displaying the scan line of the character. The basic video "dots" emanate from the shift register.

3.7.1 Basic Video

For normal (non-graphics) characters, the first and last dot positions are always blanked. For graphics characters, the first dot position has the same value as the next dot position. This allows the horizontal line graphics characters to extend all the way to the adjacent character fields for producing multicharacter solid horizontal lines.

If blank video is desired, the video "dots" will be blanked. If reverse video is desired, the video "dots" will be driven onto a two-level video point where there is a half or full intensity before being driven onto the monitor for display.

3.7.2 Attribute Control Signals

Attribute data become active as the shift register is loaded. They are loaded into the final pipeline register. The attribute bits are held constant throughout the display character's dots for the scan line in progress.

During field attribute emulation, the attributes are all loaded into the attribute hold register as the attribute delimiter is encountered. These attributes remain constant until another attribute delimiter is encountered.

The half-intensity bit, when enabled, causes the two-level video point to be loaded down, thereby lowering the video intensity level.

The inverse video bit complements video polarity. It effectively follows character and scan line blanking controls and reverses the background intensity level.

The blank attribute bit blanks the character's video level causing the character to recede into the background. The blinking bit causes the video to alternate between the normal and blanked-to-background states. The blinking rate is under program control.

3.8 OPERATION OF SERIAL INTERFACE CIRCUITRY

Operation of Z80A-CTC - The Z80A-CTC (Counter/Timer Circuit) is a programmable component with four independent channels that provide the transmitter and receiver clocks for the primary and printer ports. Channels 0 and 1 are primary port transmitter and receiver baud rates, respectively. Channel 3 is the printer port baud rate.

Operation of Z80A-DART - The Z80A-DART (Dual Asynchronous Receiver/Transmitter) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets.

3.9 DRIVER-RECEIVER OPERATION

The primary port can transmit and receive data via RS232C, current loop, or RS422 lines. The printer port is a bidirectional RS232C serial port.

3.9.1 Primary Port - RS232C Interface

When the RS232C interface is used, data will be transmitted via RS232C circuit BA and data input via RS232C circuit BB. RS232C control lines are controlled or sensed by the CPU according to the EIA RS232C specification. The RS232C interface is configured such that the terminal controller becomes a Data Terminal Equipment (DTE).

Table 3-4 lists the RS232C pin signal assignments.

Table 3-4. RS232C Pin Signal Assignments

Pin No.	RS232C Circuit	Definition
1	AA	Protective Ground
2	BA	Transmit Data to Modem/Host
3	BB	Receive Data from Modem/Host
4	CA	Request-to-Send
5	CB	Clear-to-Send
6	CC	Data Set Ready
7	AB	Signal Ground
8		Data Carrier Detect
20	CD	Data Terminal Ready

3.9.2 Primary Port - Current Loop Interface (Option)

If the Current Loop interface option board is installed, the transmitter current loop is always active on the port connector pins, J4, 6-13 and J4, 6-25. The receiver current loop is always active on the port connector pins, J4, 6-4 and J4, 6-12. Table 3-5 lists current loop interface pin signal assignments.

Table 3-5. Current Loop Pin Signal Assignments

Pin No.	Definition
9	20 mA Source
12	Current Loop Receive (+)
13	Current Loop Transmit (-)
14	20 mA Source
24	Current Loop Receive (-)
25	Current Loop Transmit (+)

3.9.3 Primary Port - RS422 (Option)

If the RS422 interface option board is installed, data will be transmitted and received according to EIA RS422 specifications. Table 3-6 lists the RS422 pin signal assignments.

Table 3-6. RS422 Pin Signal Assignments

Pin No.	Definition
15	Receive Data (+)
17	Receive Data (-)
19	Transmit Data (+)
25	Transmit Data (-)

3.9.4 Printer Port

The printer port's data and control signals are directly connected to the primary port via a multiplex circuit. This allows the printer port to functions as a bidirectional printer port.

3.10 OPERATION OF BUS INTERFACE CHIP

The bus interface IC includes:

a. Bus interface circuit
b. HSYNC drive circuit
c. Keyboard interface circuit

a. The bus interface circuit provides the necessary circuitry for the CPU to access the display RAM data bus.

b. The HSYNC drive circuit extends the HSYNC pulse to fit the video board requirement.

c. The keyboard interface circuitry uses two shift registers to convert the serial data to parallel data. The clock of shift registers is derived from a sixteen-divided counter from HSYNC. The counter starts counting from VSYNC and stops when 12 data bits are received. Since the data stored in the shift register will clear as VSYNC occurs, the CPU should read the data before then and answer the keyboard by accessing the appropriate I/O port.

SECTION IV
MAINTENANCE

4.1 INTRODUCTION

This section contains maintenance information for the Ampex 230/219 Video Display Terminals. Corrective action for field repair of the terminal should be limited to removal and replacement of subassemblies (Section VI). Procedures involving maintenance adjustments and repairs should be performed by service personnel familiar with data terminal and video equipment.

WARNING

Exercise caution while working on the energized video or power supply sections. Avoid physical contact with high voltage leads and connections.

4.2 TEST EQUIPMENT

A list of test equipment (equivalent items may be substituted) for use during adjustment and troubleshooting is provided in Table 4-1. In addition to the items listed, hand tools commonly used in the repair of electronic equipment will be required.

Table 4-1. Test Equipment

Test Equipment	Manufacturer	Model or Part No.
AC Current Probe	Tektronix	P6021
Termination for AC Current Probe	Tektronix	011-0105-00
Oscilloscope	Tektronix	485B
Digital Voltmeter	Fluke	8020A

4.3 PERFORMANCE TESTING

The procedures described below can provide an evaluation of terminal performance.

4.3.1 Power On Self Test

1. Detach the interface cables connected to the primary port and printer port.
2. Apply power to the terminal. Verify the following:
   a. Alarm (beep) sounds within 5 seconds.
   b. User line and cursor appear within 15 seconds.
   c. No bad component error messages are indicated on the status line. Bad component error messages are explained in Table 4-2.

Table 4-2. Bad Component Error Messages

Message	Explanation	Corrective Action
CMOS CK ERROR	CMOS CHECK SUM FAILURE	Replace Controller PWBA
DATA RAM ERROR	DATA MEMORY FAILURE	Replace Controller PWBA
DISPLAY RAM ERROR	DISPLAY MEMORY FAILURE	Replace Controller PWBA
ROM ERROR	PROGRAM MEMORY FAILURE	Replace Controller PWBA

NOTE: Clear bad component error indicators by resetting the terminal.

4.3.2 Test Pattern

1. Apply power to the terminal.
2. Enter Set-up mode.
3. Press the number, 1.

4. Verify the following:

   a. The terminal's model number and firmware revision level are displayed on line 1.

   b. Reverse video, half intensity, underlining, and flashing character visual attributes are displayed.

   c. All alphanumeric characters, national characters and symbols, and monitor mode facsimile symbols are displayed.

   d. Block and line graphics are displayed.

4.3.3 Keyboard Test

1. Apply power to the terminal or press CTRL/SHIFT/RESET to reset the terminal if power is already on.

2. Place the terminal in local mode (enter Set-up mode).

3. Starting at the upper left corner of the keyboard, press each symbol, number, and letter key (shifted and unshifted) in sequence.

4. Verify that:

   a. Keys do not stick.

   b. Characters appear on the screen as keys are pressed.

   c. Appropriate character appears on screen for corresponding key (depends upon character set; selectable in Set-up mode).

   d. Only one character appears on the screen when each key is pressed and released once.

4.4 VIDEO ADJUSTMENTS

Seven adjustments on the Video PWBA, as shown in Figure 4-1, permit adjustment of the brightness, focus, vertical size, vertical linearity, and horizontal size. Note that brightness (paragraph 4.4.1) should be adjusted prior to performing the other adjustments.

4.4.1 Brightness

1. Apply power to the terminal. Place the terminal in local mode (enter Set-up mode).

2. Select a reverse video background (Status Line 2 in Set-up mode).

3. Enter SHIFT/S to generate a reverse video display.

4. Turn the intensity control dial (under lower-right corner of display screen on exterior of case) to maximum intensity (refer to Figure 2-3).

5. Remove the top cover (see paragraph 6.3.1).

6. Adjust brightness (VR301 on Video PWBA: see Figure 4-1) so that CRT display is at maximum brightness but no raster is visible.

7. Using the intensity control dial, lower the CRT brightness to a comfortable viewing level.

8. Remove power from the terminal.

9. Replace the top cover.

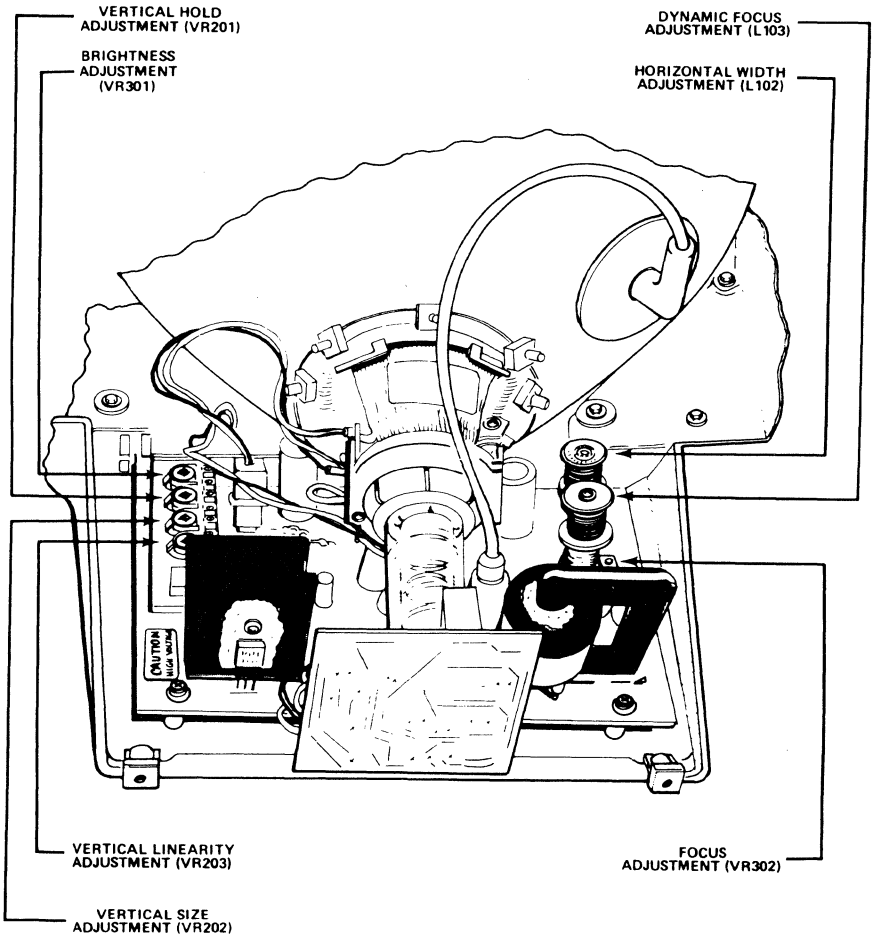


Figure 4-1. Video Adjustments

4.4.2 Focus

1. Apply power to the terminal. Place the terminal in local mode (enter Set-up mode).
2. Fill the screen with exclamation marks (!).
3. Remove the top cover.
4. Adjust Focus (VR302 on Video PWBA for center focus; focus coil L103 for edge focus: see Figure 4-1) so that the dot of every exclamation mark (in both center and edge areas of the screen) is clearly separated.
5. Remove power from the terminal.
6. Replace the top cover.

4.4.3 Vertical Size

1. Apply power to the terminal.
2. Enter Set-up mode and place terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust the vertical dimension of the video display (VR202 on Video PWBA: see Figure 4-1) to 172mm (±3mm).
6. Remove power from the terminal.
7. Replace the top cover.

4.4.4 Horizontal Size

1. Apply power to the terminal.
2. Enter Set-up mode and place the terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust the horizontal dimension of the video display (L102 on Video PWBA: see Figure 4-1) to 239 mm (±5mm).
6. Remove power from the terminal.
7. Replace the top cover.

4.4.5 Vertical Linearity

1. Apply power to the terminal.
2. Enter Set-up mode and place the terminal in local mode.
3. While still in Set-up mode, type the number "0" to generate an alignment pattern.
4. Remove the top cover.
5. Adjust vertical linearity (VR203 on Video PWBA: see Figure 4-1) so that typical dimensions of any "E" character are within 15 percent of the dimensions illustrated in Figure 4-2.
6. Remove power from the terminal.
7. Replace the top cover.

4.5 TROUBLESHOOTING

Figure 4-3 is an interconnection diagram of the terminal. The waveforms provided in Figures 4-4 through 4-8 are representative of typical oscilloscope CRT displays.

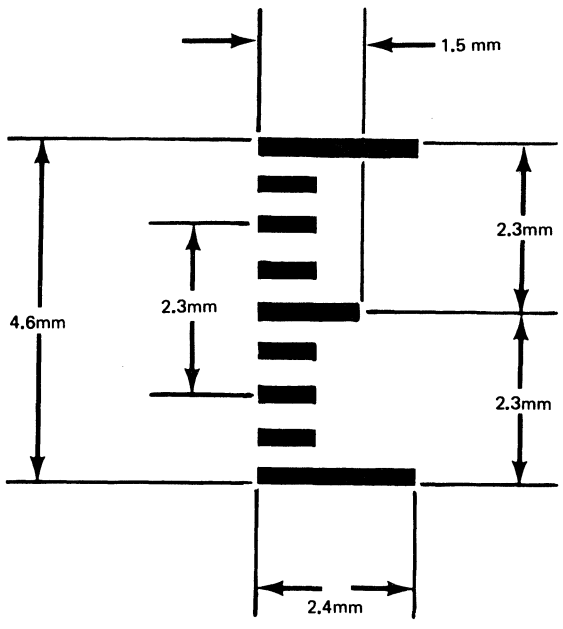


Figure 4-2. Dimensions of E Character

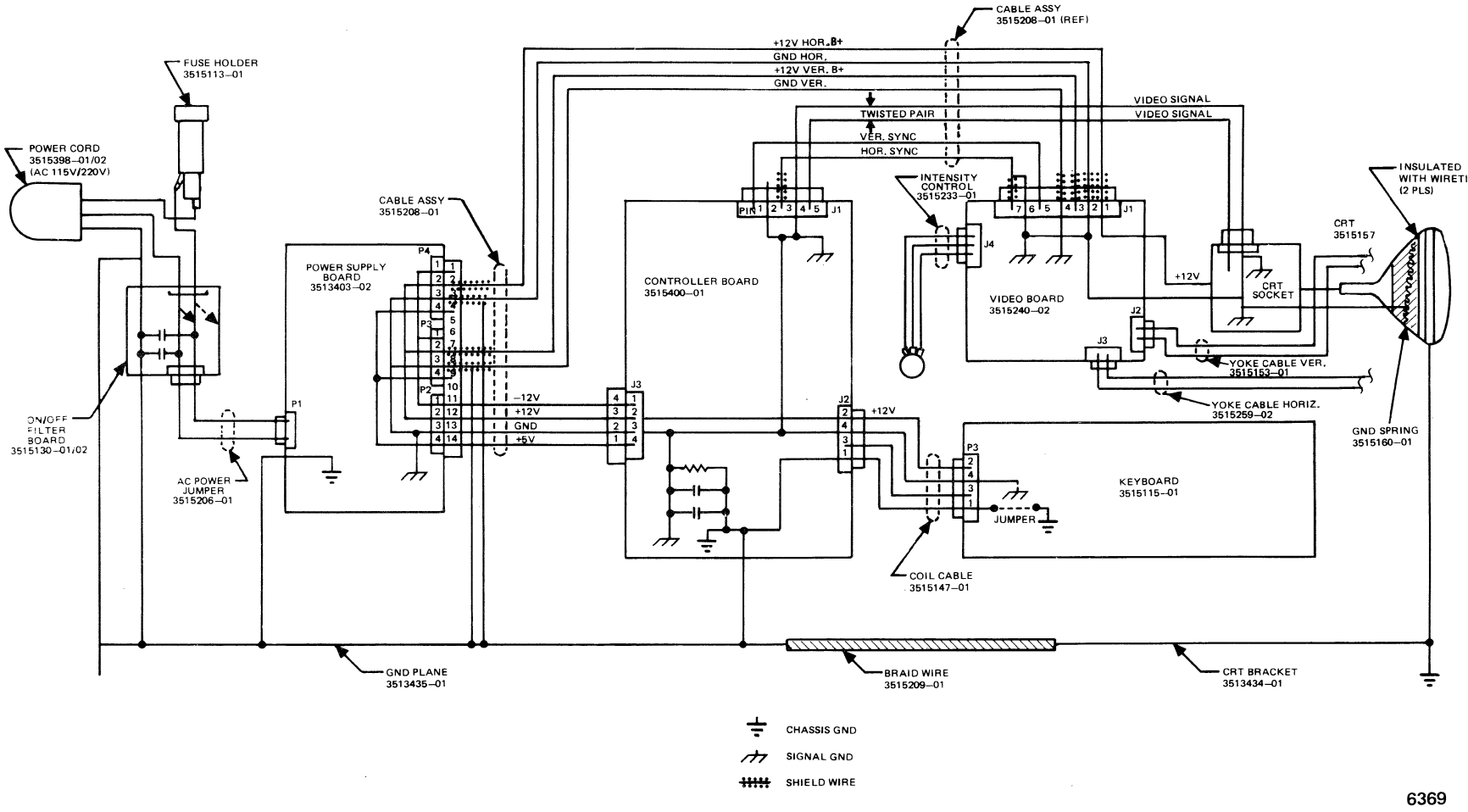


Figure 4-3. Interconnection Diagram

1. Dot Rate is 19.6 MHz in 80 Columns;
   32.14 MHz in 132 Columns

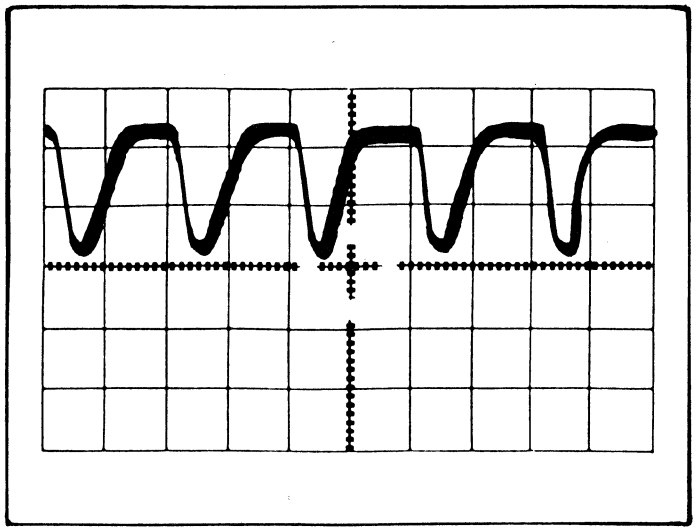


Figure 4-4. Video Waveform

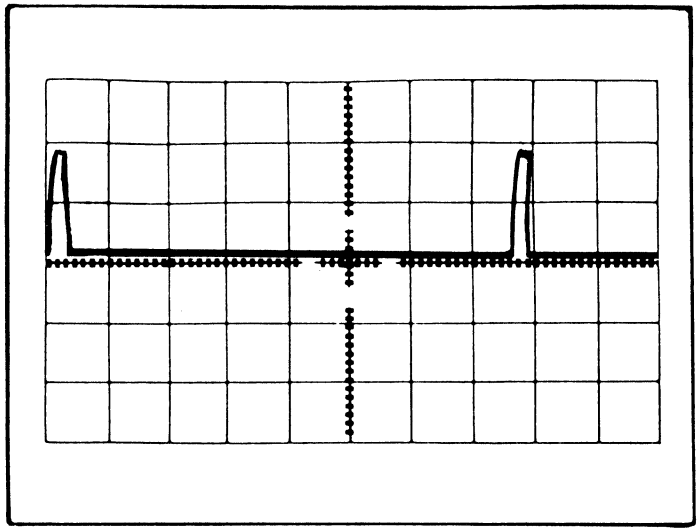
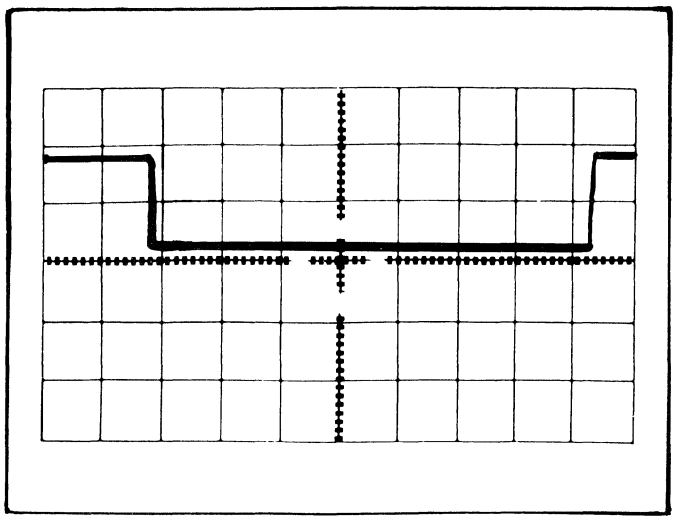


Figure 4-5. Vertical Sync Waveform

1. HORIZONTAL RATE IS 21.778KHz
2. HORIZONTAL DRIVE PULSE WIDTH IS 12 Ms

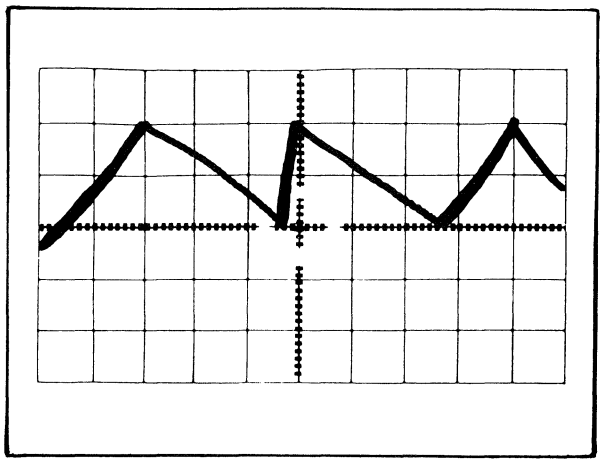


TEST POINT
J1-7-③

2V/DIV @ 5 MICROSECONDS

6203A

Figure 4-6. Horizontal Sync Waveform



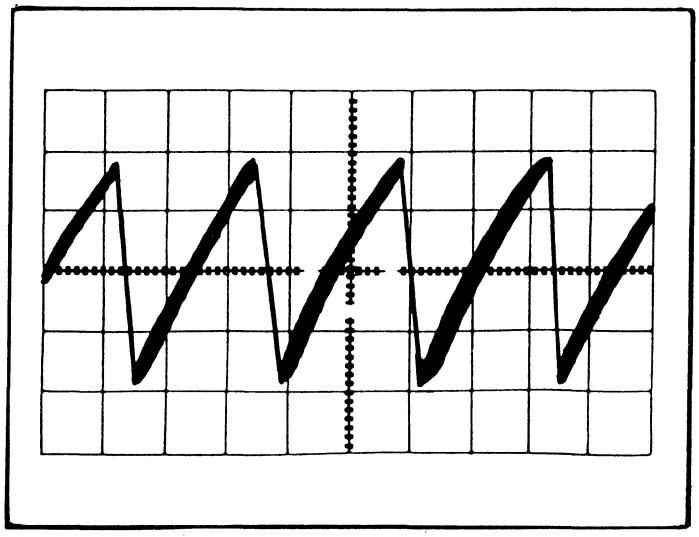
TEST POINT
J2-④

200 MA/DIV @ 5 MILLISECONDS

6204A

Figure 4-7. Vertical Deflection Waveform

1. Horizontal Deflection current is 21.78 KHz



TEST POINT
J3-5

2A/DIV. @ 20 MICROSECONDS

6205

Figure 4-8. Horizontal Deflection Waveform

SECTION V
REMOVAL AND REPLACEMENT

5.1 INTRODUCTION

This section provides instructions for the removal and replacement of the terminal's major replaceable parts.

WARNING

There are hazardous voltages inside the pedestal and display units. Extremely high voltages are present on the CRT. The CRT may retain a charge for an indefinite period of time if not discharged. Always discharge the CRT before replacing it or working near it.

5.2 SUBASSEMBLY/PARTS LOCATION

Table 5-1 provides a list of removable parts and subassemblies for the Ampex 230/219 terminals. Figure 5-1 is an exploded view of the location of those parts and subassemblies.

Table 5-1. Subassembly and Parts List

Ref Fig. 5-1	Subassembly/Part	Part No.
A	Pedestal Assembly	3515333
B	CRT Housing, Bottom	3513426
	Ground Spring Assembly	3515160
C	Video, PWBA	3515240
D	CRT Housing, Top	3513427
E	Video, PWBA (hard-wired to major board)	3515240
F	Pedestal Unit, Top	3513425
G	CRT Amber	3515151
	CRT Green	3515151
	Intensity Control Assembly	3515233
H	Yoke/Cable Assembly	3515158
I	Controller, PWBA	3515400, 3515455
J	ON/OFF Switch/Filter	3515385
K	Power Supply, PWBA	3513403
	Choke Assembly	3515230
L	Keyboard Cable Connector to Keyboard Assembly	3515334
	Keyboard Cover	3513420
	Keyboard Base	3513421
	Coil, Cable 6-ft	3515147

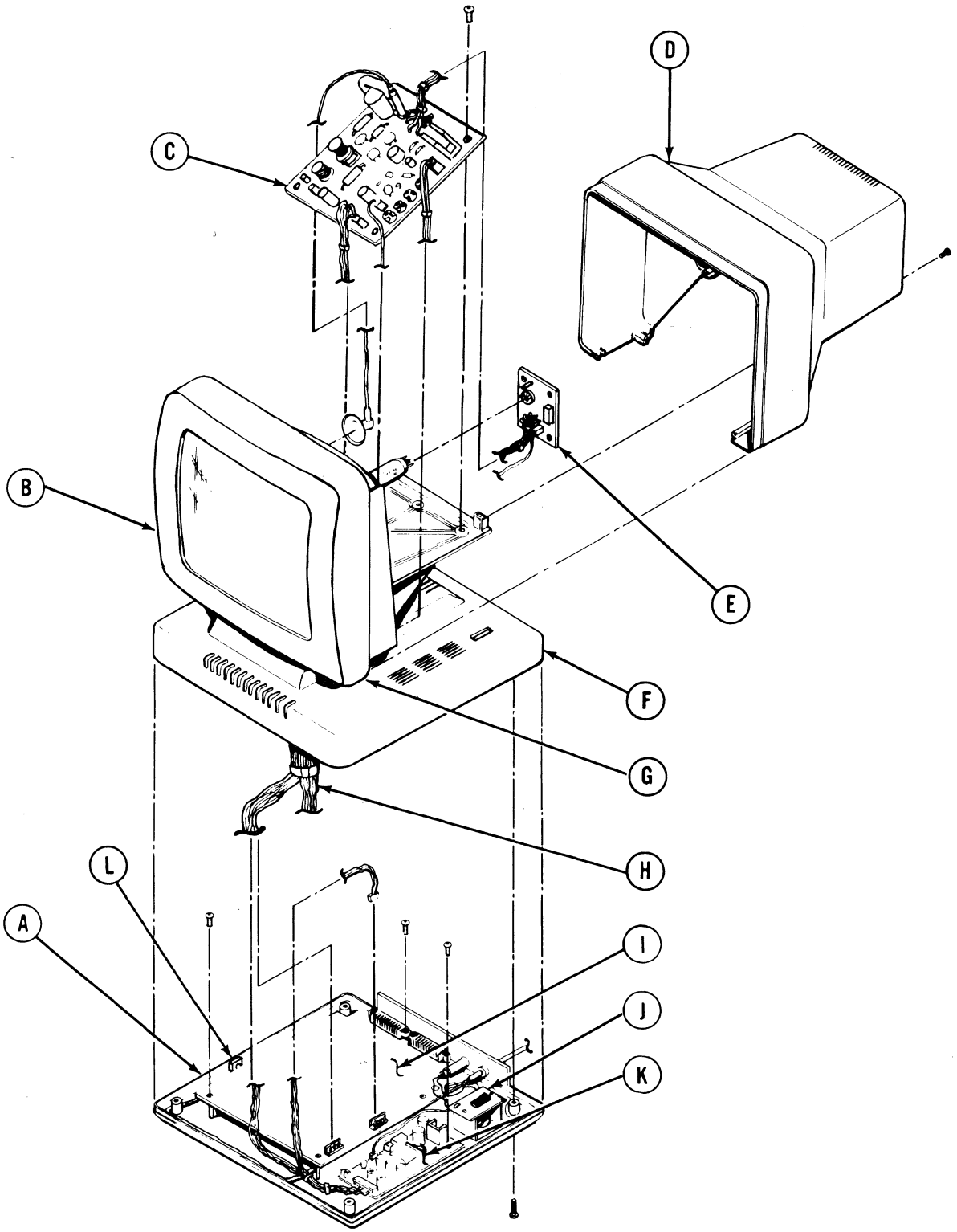


Figure 5-1. Subassembly Location Diagram

5.3 PRELIMINARY PROCEDURE

Before removing or replacing any of the parts of the terminal, turn the power off and unplug power cord. Disconnect the keyboard cable from the display unit. When removing parts with cable or wire connections, it is recommended that the cables or wires are tagged in order to ensure correct replacement.

5.3.1 Display (Bezel) Cover Removal And Replacement

Using a Phillips screwdriver, remove the two screws at the rear of the display unit. Carefully slide the cover away from the screen (Figure 5-2). When cover will slide no further, gently tilt cover up and lift off.

Replacement is the reverse of removal. Ensure that the sides of the cover slide into place before replacing the two screws at the rear of the cover.

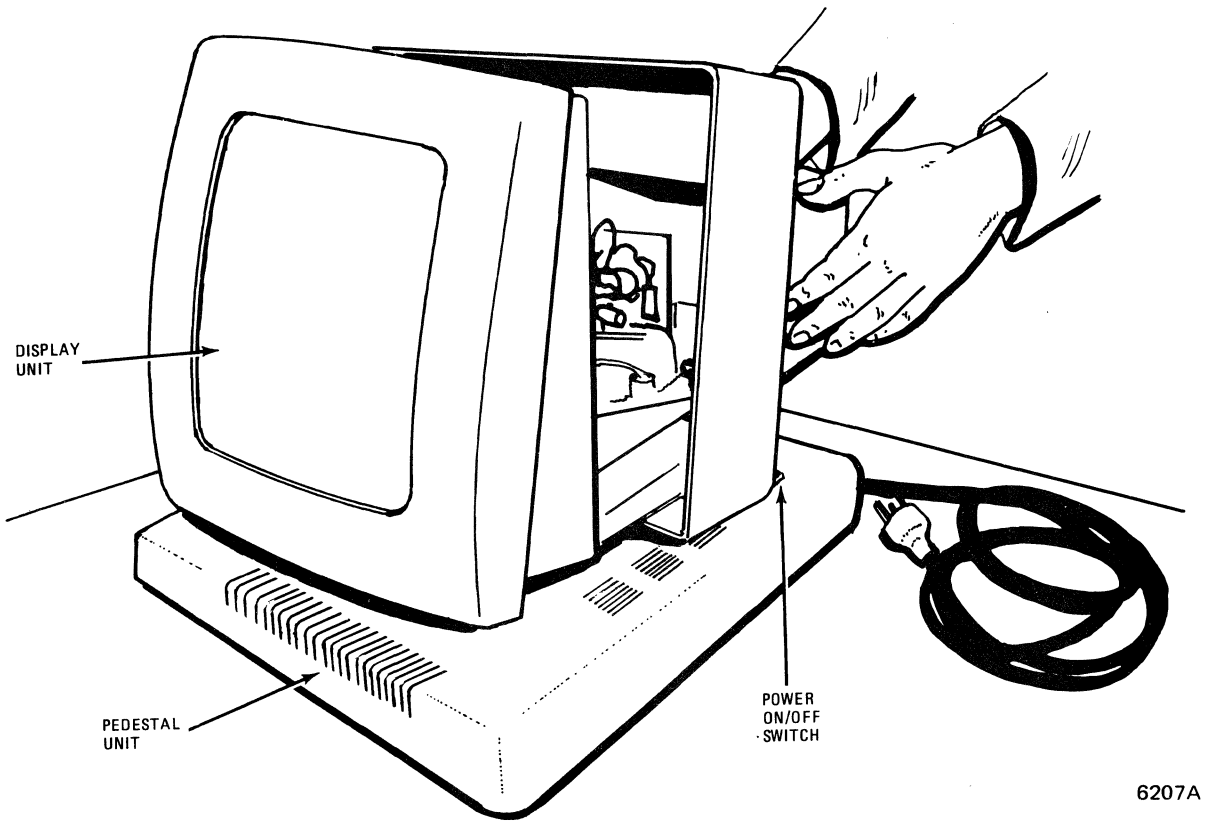


Figure 5-2. Removing the Display Cover

5.3.2 Pedestal Cover Removal And Replacement

Tilt the display assembly until the unit is resting on its side.

Using a Phillips screwdriver, remove the four screws on the underside of the pedestal unit. Gently force the bottom cover away from the display (Figure 5-3).

Replacement is the reversal of removal. Make sure that the bottom cover is in place before replacing the four screws.

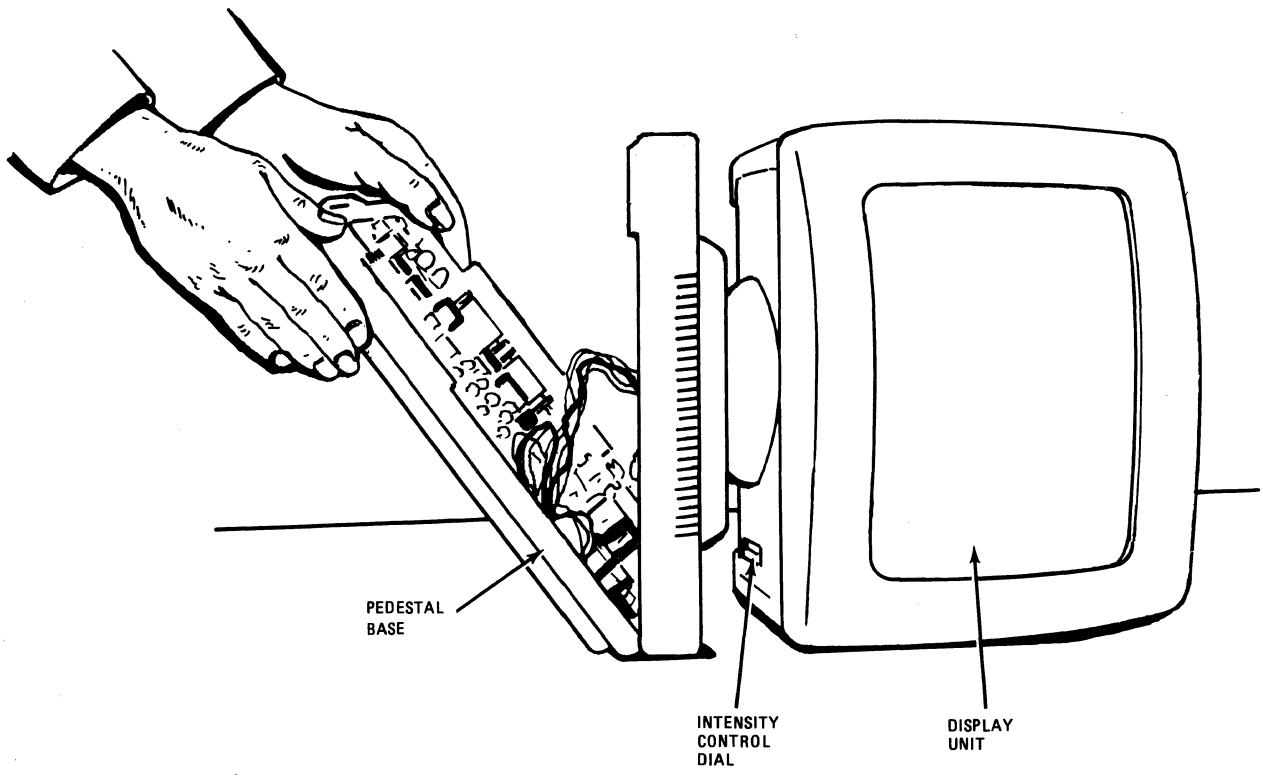


Figure 5-3. Removing the Pedestal Cover

5.3.3 Controller PWBA Removal And Replacement

The Controller printed wiring board assembly (PWBA) is located in the pedestal unit (refer Figure 5-1).

1. Using a Phillips screwdriver, remove the screws holding the board in place.

2. Tag and disconnect any cables connected to the board.

3. Slowly slide the board away from the two RS232C serial ports. When the serial connectors are free of their ports, lift the board up and out of the unit.

To replace the board, reverse the procedure. Make sure the board is firmly seated before replacing the screws.

5.3.4 Power Supply PWBA Removal And Replacement

The power supply PWBA is located in the pedestal unit (see Figure 5-1).

1. Using a Phillips screwdriver, remove the four screws holding the power supply board in place.

2. Tag and disconnect any cables connected to the board.

3. Slowly pull the board up and out of the pedestal unit.

To replace the power supply board, reverse the procedure. Make sure the board is firmly seated before replacing the screws.

5.3.5 Discharging The CRT

WARNING

The CRT Anode may stay charged at an extremely high voltage for a long time after the power is removed from the terminal. Be sure to follow the CRT discharging procedure carefully. Make sure that a good discharge path is made between the ground wire around the CRT and anode connector beneath rubber cover.

1. Make sure that power is off and that the power cord is disconnected from the ac power outlet.

2. Using a wire lead with an alligator clip on each end, connect one alligator clip to ground screw and the other clip to a flat-blade screwdriver with an insulated, rubber handle (Figure 5-4).

3. Hold the screwdriver by the insulated handle with one hand and move the other hand away from the unit.

4. Slip the screwdriver blade under the rubber anode cover and touch the end of the anode lead. This action should discharge the CRT through the ground wire.

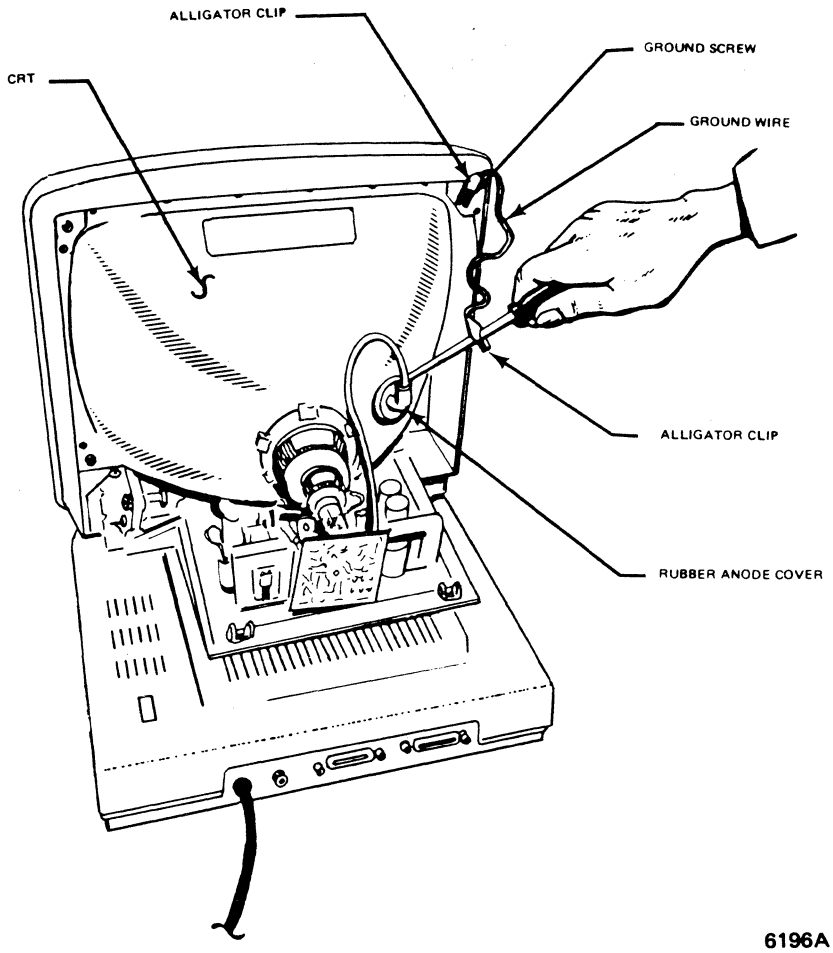


Figure 5-4. Discharging the CRT

5.3.6 Video PWBA Removal and Replacement

The video PWBA (board) is located in the display (bezel) unit (see Figure 5-1). Make sure the CRT has been discharged before removing the video board.

1. Pull up on the two black plugs in the corners of the video board until they pop out.

2. Tag and disconnect any cables attached to the board.

3. Gently slide board away from the screen. Then lift up and remove from the bottom of the unit.

To replace the board, reverse the procedure. Make sure the board is firmly seated before replacing the cover of the display unit.

APPENDIX A
INSTRUCTIONS FOR INSTALLING USER-INSTALLABLE OPTIONS

RS422 INTERFACE INSTALLATION PROCEDURE

1. Install four snap-on plastic mounting clips (P/N 283-339) into four mounting holes on Controller board (P/N 3515400) as shown in Figure 1. Make sure wings of each clip do not interfere with components of Controller board.

2. Install RS422 Interface board (P/N 3515435) to Controller board over the four newly installed snap-on clips with U1 on RS422 Interface board towards left side of Controller board as shown in Figures 1 and 2.

3. Install cable assembly (P/N 3515517 *) between U1 of Interface board and U40** of Controller board. Align pin 1 on both ends of cable to pin 1 of U1 and pin 1 of U40.

4. Make sure both ends of cable are seated into U1 and U40 properly.

*If alternate cable assembly is used (P/N 636-215), use wire tie (P/N 302-335) to secure excess cable to lower-left side mounting clip.

**If Controller board is a 4-layer board (P/N3515455), one end of the cable assembly should be installed into U46 position.

Part No. 3515412-02A

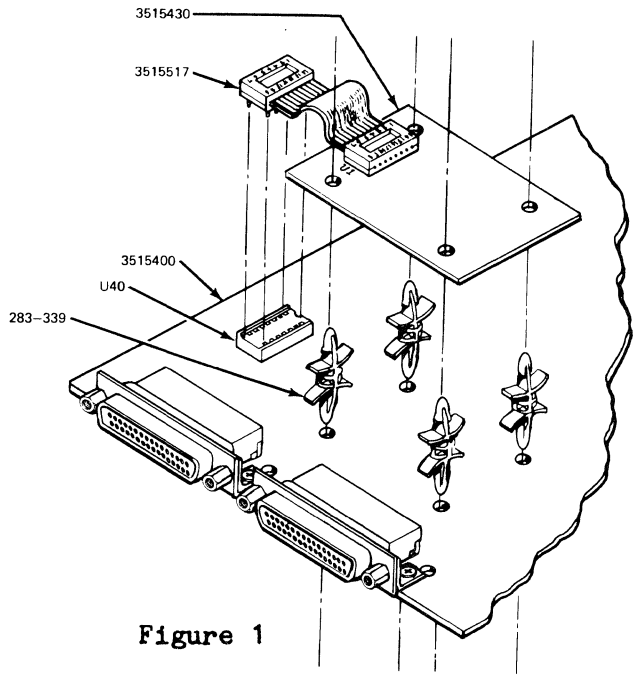


Figure 1

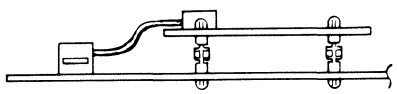


Figure 2

6904

5. Pin signal assignments for the RS422 port are:

15	REC Data (+)
17	REC Data (-)
19	XMIT Data (+)
25	XMIT Data (-)
7	Ground
1	Chassis Ground

CURRENT LOOP INSTALLATION PROCEDURE

1. Install four snap-on plastic mounting clips (P/N 283-339) into four mounting holes on Controller board (P/N 3515400) as shown in Figure 1. Make sure wings of each clip do not interfere with components of Controller board.

2. Install Current Loop board (P/N 3515430) to Controller board over the four newly installed snap-on clips with U1 on Current Loop board towards left side of Controller board as shown in Figures 1 and 2.

3. Install cable assembly (P/N 3515517 *) between U1 of Current board and U40** of Controller board. Align pin 1 on both ends of cable to pin 1 of U1 and pin 1 of U40.

4. Make sure both ends of cable are seated into U1 and U40 properly.

*If alternate cable assembly is used (P/N 636-215), use wire tie (P/N 302-335) to secure excess cable to lower-left side mounting clip.

**If Controller board is a 4-layer board (P/N3515455), one end of the cable assembly should be installed into U46 position.

Part No. 3515413-02A

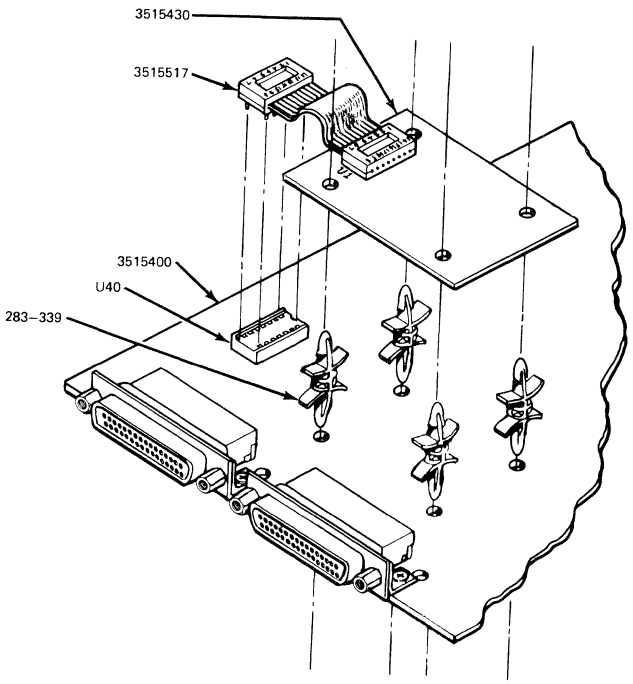


Figure 1

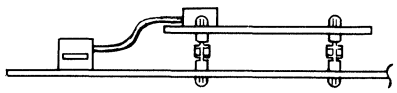


Figure 2

6904

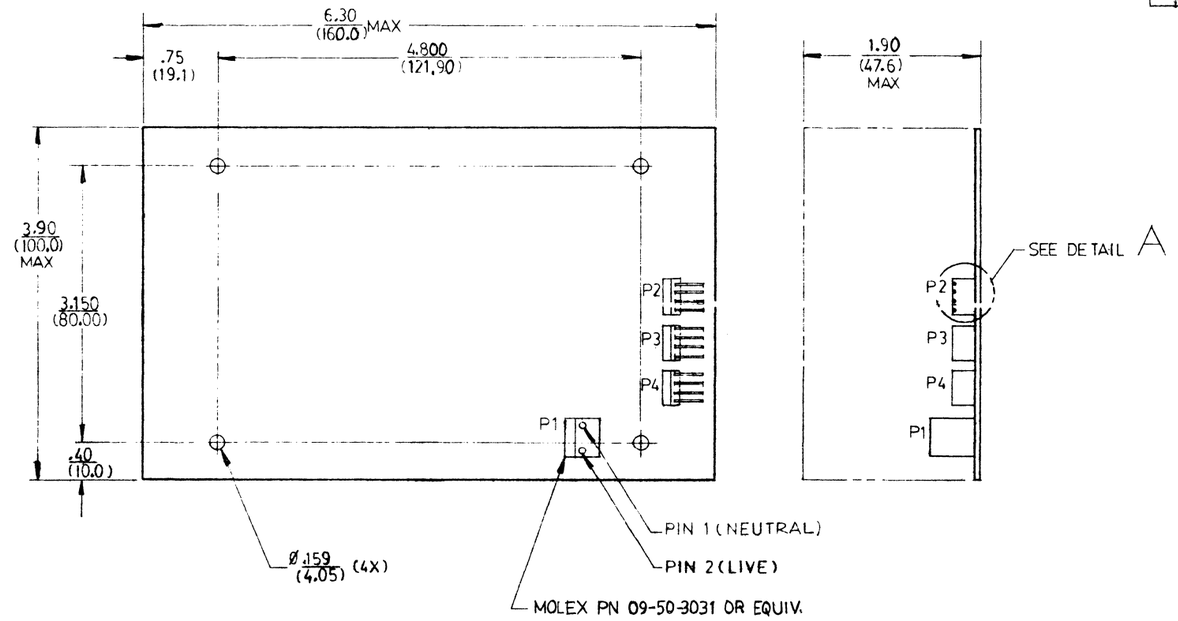
5. Pin signal assignments for the current loop option are:

9	20 MA Source
14	20 MA Source
13	XMIT Current (-)
25	XMIT Current (+)
12	REC Current (+)
24	REC Current (-)
7	Ground
1	Chassis Ground

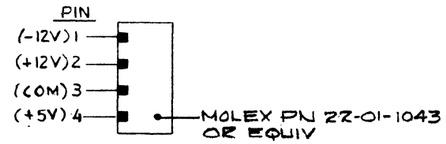
APPENDIX B
REFERENCE DRAWINGS

Drawing No.	Title
3513403	PWBA - Power Supply
3515113	Fuse Holder Assembly
3515115	PWBA - Keyboard
3515156	Yoke/Tube Assembly
3515158	Yoke/Cable Assembly
3515233	Intensity Control Assembly
3515240	PWBA - Video Board
3515319	Cable Assembly - AC Power Jumper
3515333	Pedestal Assembly
3515334	Keyboard Assembly
3515335	Key Assembly
3515385	PWBA On/Off Switch/Filter
3515398	PWBA - Power Supply
3515400	PWBA Terminal Controller
3515455	PWBA Terminal Controller

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0300 (PROTO)			
B		ERN 0305 (PROTO) ADDED -02			12-9-83
B		ERN 0307 CONT	AG	AG	3-13-84



VERSION TABLE		
PART Nº	VENDOR P/N	REMARKS
3513403-01	AC8151 (5)	NON-VDE APPROVED
3513403-02	AC8151-01 (5)	VDE-APPROVED



DETAIL A (DC OUTPUT)
TYP P2, P3, P4

(5) PART MAYBE PURCHASED FROM:
A) ASTEC CO, HONG KONG

4. DIMENSIONS IN PARENTHESIS ARE MM.
TOL: .X = .8 MM, .XX = .25 MM
3. FOR POWER SUPPLY SPECIFICATION SEE DRAWING 3513401.
2. MARK PART WITH PART NO. AND LATEST REV. LTR PER AMPEX SPEC 3124500, PARA 3.1. LOCATE PER VENDOR OPTION.
1. PART NO. TO BE PER VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

SPECIFICATION CONTROL DRAWING

PARTS LIST ☐ MFG R&B

3515150 NEXT ASSY	ORION USED ON
APPLICATION	

NOTICE

THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL .03 | 3 PL .010 | ANLR
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER ANSI 10387
INTERPRET DRAWING PER ANSI Y14.5

SIGNATURE		DATE
DRAWN BY		10-19-83
CHK BY		10-20-83
DFTG APVD		
ENGRG APVD		10-21-83
AUTH BY	S. Lee	10-21-83

MATERIAL: (5)
FINISH:

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

POWER SUPPLY (ORION)

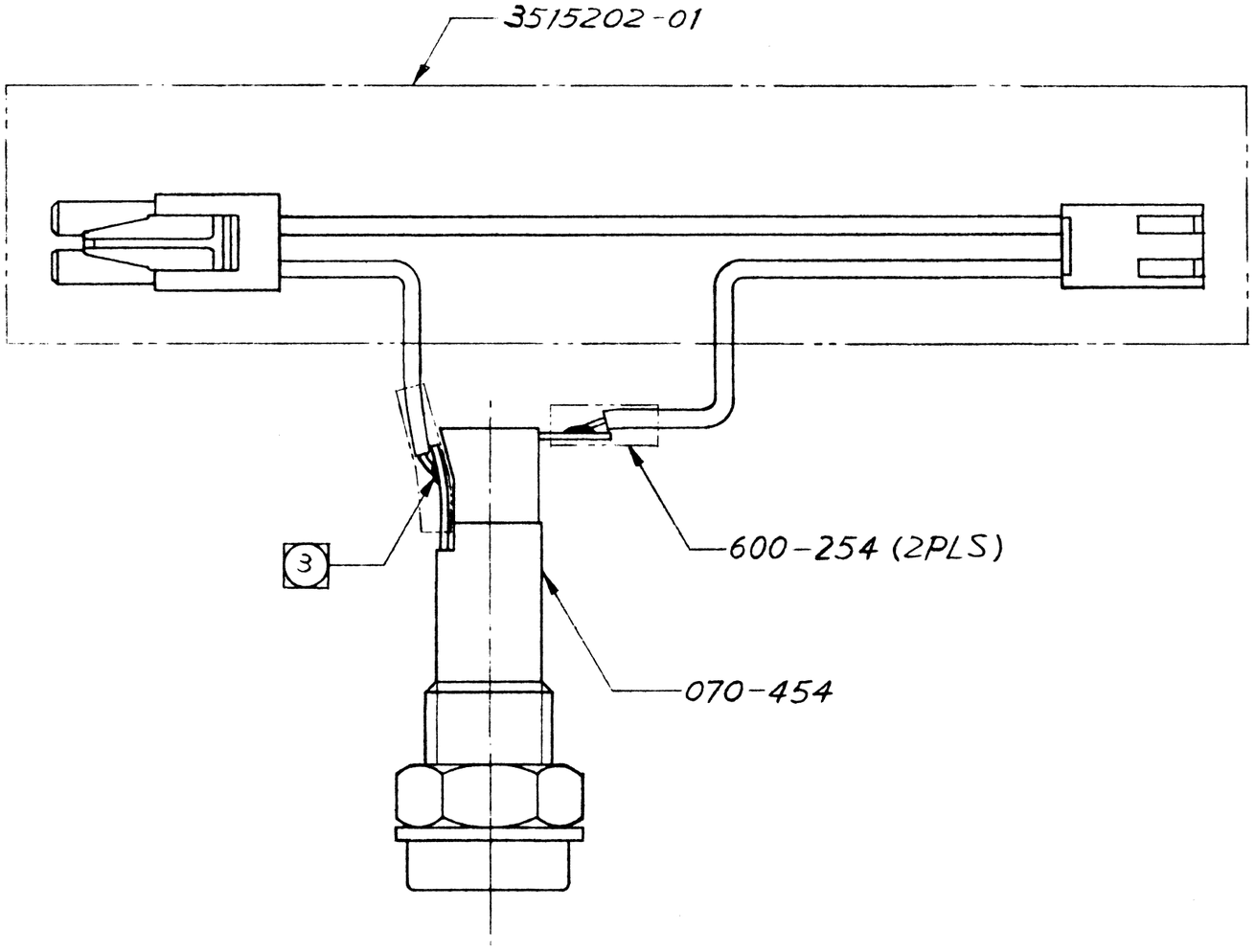
SIZE	CODE IDENT NO.	
C	09150	3513403

SCALE — DO NOT SCALE THIS PRINT. SHEET 1 OF 1

UC-3553-05 (REV NOV 72) PRINTED IN U.S.A.

3515113

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A	NEVER REL			
B	ERN 0011	11-8-83	11-8-83	11-8-83
B	ERN 0024 (CONT.)	2-24-84	3-2-84	3-2-84



4 METRIC ENGRG & DFTG PRACTICES PER AMPEX STD MB-3.

(3) ASSEMBLE PER AMPEX STANDARDS, HC2-5.

2 IDENTIFY PART NO. & ISSUE LTR. PER AMPEX SPEC 3124500, PARA 3.2 .

1 PART NO. TO BE 3515113-01.

NOTES UNLESS OTHERWISE SPECIFIED

PARTS LIST ☒

3515150	ORION
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISH.

TOL ±		2 PL	3 PL		ANLR
		—	—		—

REMOVE BURRS AND SHARP EDGES

DRILL TOL PER AND 10387

INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

SIGNATURE		DATE
DRAWN BY	Lisa Kim	11-8-83
CHK BY	B. Reich	11-8-83
DFTG APVD	B. Reich	11-8-83
ENGRG APVD	[illegible]	11-8-83
AUTH BY	[illegible]	11-8-83

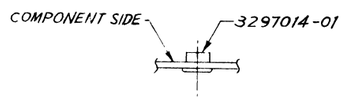
AMPEX — COMPUTER PRODUCTS DIVISION, Marina del Rey, California 90291

FUSE HOLDER ASSY

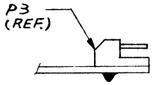
SIZE	CODE IDENT NO.	
B	09150	3515113

SCALE | DO NOT SCALE THIS PRINT | SHEET OF

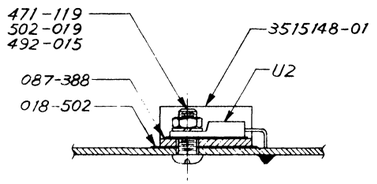
REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
G		ERN 0304 (PROTO)			
G		ERN 0024 (CONT.)			
H		ECN 42031			
J		ECN 42039			
K		ECN 42147			



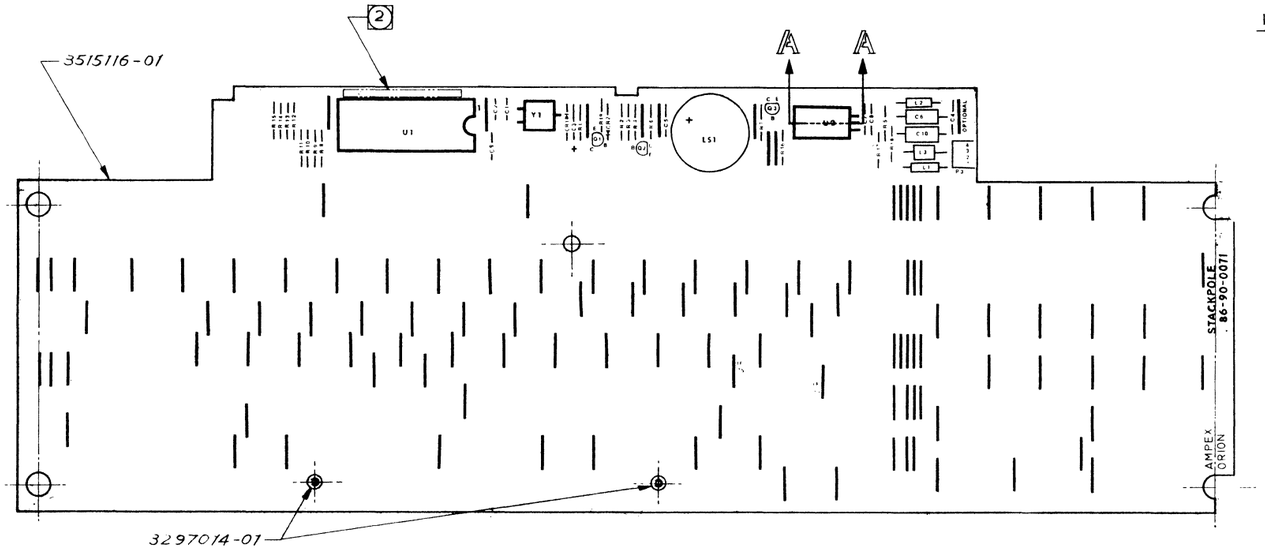
MTG. FOR SPACER



MTG. FOR P3



VIEW: A-A
MTG FOR U2



COMPONENT SIDE

REFERENCE DESIGNATION TABLE

ITEM	PART. NO	DESCRIPTION		REMARK
1	3515116-01	PWB KEYBOARD		
2	587-438	U2	VOLTAGE REGULATOR	IC 7805
3	580-647	Q1, Q2	TRANSISTOR	2N3904
4	580-800	Q3	TRANSISTOR	2N5550
5	017-238	Y1	CRYSTAL	4.9152 MHz
6	650-333	LS1	BUZZER	PIEZOELECTRIC
7	066-668	R1, R3, R6.	RESISTOR	4.7KΩ, 1/4W, ±5%
8	066-830	R2, R8--R17, R19.	"	10KΩ, 1/4W, ±5%
9	066-664	R4, R7.	"	510Ω, 1/4W, ±5%
10	066-677	R5	"	68Ω, 1/4W, ±5%
11	066-839	R18	"	560Ω, 1/4W, ±5%
12				
13	063-460	C10	CAP. LYTIC	47u, 16V, +75 -10 %
14	064-937	C1, C2	CAP. DISK ALTERNATE: 064-460	22P, 50V, ±5%
15	3512886-01	C4, C5	CAP. MONO	330P, 50V, ±5%
16	063-456	C3	CAP. LYTIC	1u, 50V, +75 -10 %
17	063-458	C6	CAP. LYTIC	10u, 35V, +75 -10 %
18	064-941	C7~C9	CAP. MONO ALTERNATE: 064-458	0.1u, 50V,
19				
20	581-105	CR1, CR2	DIODE, SWITCHING ALTERNATE: 581-403	1N4148

ITEM	PART. NO.	DESCRIPTION		REMARK
21	068-303	L2	CHOKE	33 uH. 200MA, ±10%
22	068-304	L1	CHOKE	22 uH. 190MA, ±10%
23	068-305	L3	CHOKE	25mH. 200MA, ±10%
24				
25	615-012	WIRE,	SOLID, BARE	A.W.G. #20
26	135-549	P3	RT. ANGLE HEADER	4 PIN
27	164-168	DECOUPLING CAP, CERAMIC		0.1uF ALT: 164-169 164-163
28				
29				
30	3515148-01	HEAT SINK		
31	3297014-01	SPACER		
32				
33				
34				
35				
36				
37				
38				
39				
40				

7 MAX. LEAD PROTRUSION OF COMPONENTS ON SOLDER SIDE IS 1.6 MM .
6 COMPONENT DESIGNATIONS ARE FOR REF. ONLY.
5 COMPONENT MUST NOT EXTEND BEYOND OUTLINE OF BD.
4. ASSEMBLE PER AMPEX STD.
3. FOR LOGIC DIAGRAM SEE SH. 2 .
[2] MARK ISSUE LTR. AND SERIAL NO. PER AMPEX SPEC. 3124500 PARA 3.1.
1. PART NO. TO BE 3515115-01.

NOTES: UNLESS OTHERWISE SPECIFIED

3515115

NEXT ASSY	ORION
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL — | 3 PL — | ANLR —
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY		
CHK BY		
DFTG APVD		
ENGRG APVD		
AUTH BY		

MFG Engr. PARTS LIST ☒

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

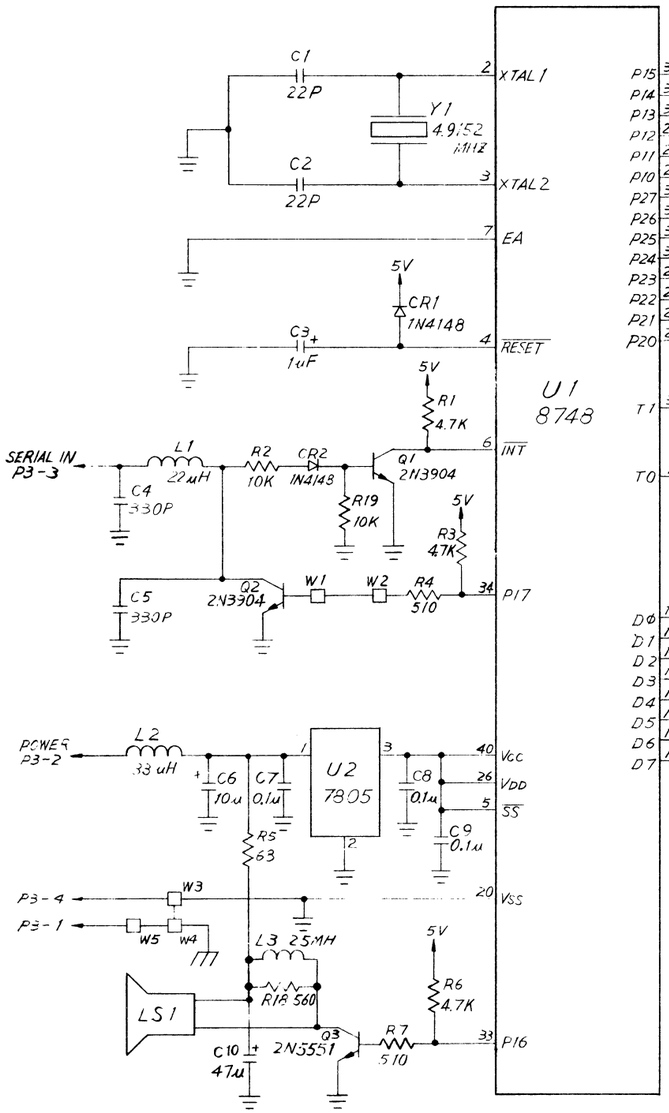
PWBA-KEYBOARD

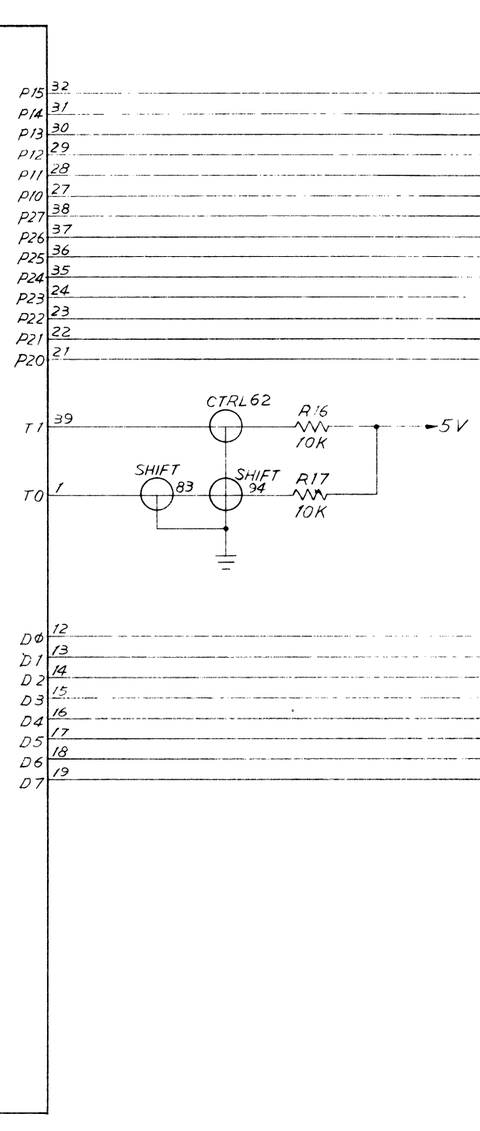
SIZE	CODE IDENT NO.	
D	09150	3515115
SCALE	DO NOT SCALE THIS PRINT	SHEET 1 OF 2

UC-3604-08 (REV JAN 82) PRINTED IN U.S.A.

3515115

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
K		SEE SH. 1	11/20/73	11/20/73	11/20/73





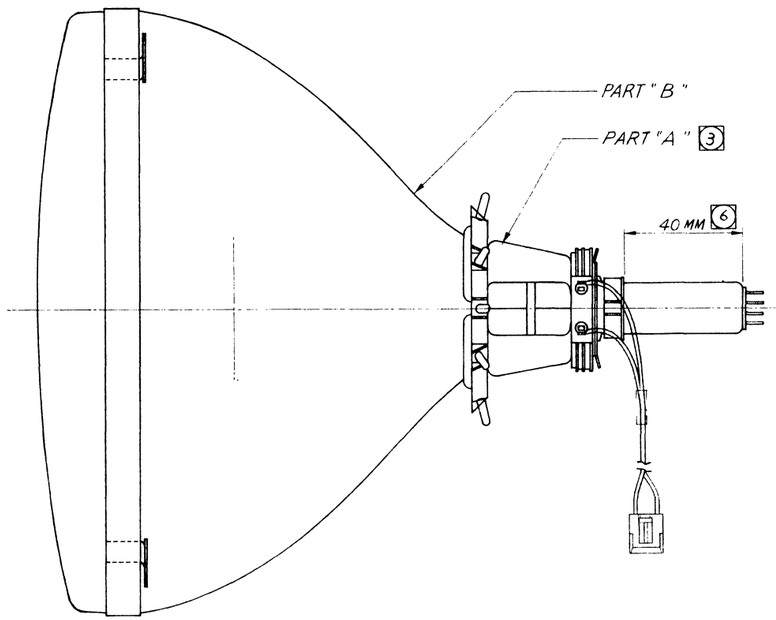
	R8 10K	R9 10K	R10 10K	R11 10K	R12 10K	R13 10K	R14 10K	R15 10K
P15 32	19	40	59	79	88	87	86	89
P14 31	18	39	58	78	105	92	91	90
P13 30	17	38	57	77	9	30	49	69
P12 29	16	37	56	76	8	29	48	68
P11 28	15	36	55	75	7	28	47	67
P10 27	14	35	54	74	6	27	46	66
P27 38	110	111	98	97	96	95	108	109
P26 37	112	101	100	99	107	93	106	
P25 36	21	42	61	81	103	102	82	
P24 35	20	41	60	80	84	85	104	113
P23 24	13	34	53	73	5	26	45	65
P22 23	10	31	50	70	1	22	43	63
P21 22	11	32	51	71	2	23	3	24
P20 21	12	33	52	72	4	25	44	64

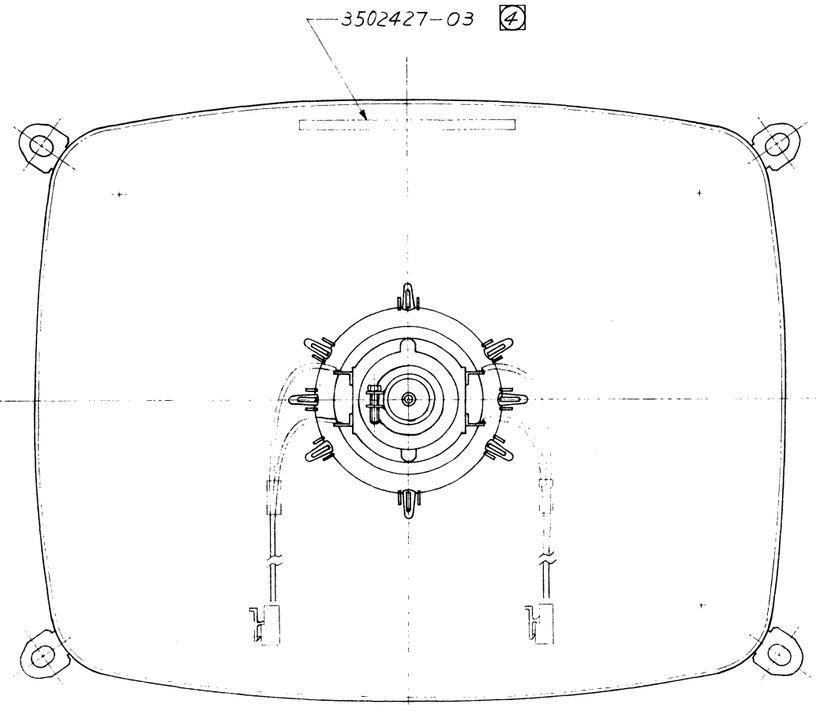
3515115

SIZE	CODE IDENT NO.	
D	09150	3515115
SCALE NONE		SHEET 2 OF 2

UC-2504A-08 (REV. DEC. 73)
PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION		SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0009				
B		PCR 42010				
B		ERN 0024	(CONT.)			
C		ERN 0064	(ADD-03)			





6 APPLY 225-527 TAPE TO NECK OF TUBE UNDER YOKE CLAMP. TAPE APPROX 3/4 TO 9/10 OF A COMPLETE TURN AROUND NECK LOCATE APPROX 40 MM FROM END OF TUBE.

5 FOR ALIGNMENT PROCEDURE SEE DWG. 3515186.

4 INSTALL WARNING LABEL ON THE TOP OF THE CRT.

3 INSTALL 3515158 AS FAR AS POSSIBLE ON NECK OF CRT (PART "B"). FOR YOKES WITH RADIAL POSTS, MAGNETS 029-025 AND 029-026 MAY BE USED TO FACILITATE ALIGNMENT.

2 ASSEMBLE PER AMPEX STANDARDS.

1 PART NO. TO BE PER VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

SI metric

VERSION TABLE			
3515156-03	3515158-01	3515157-06	GREEN
3515156-02	3515158 01	3515157-02 (ALTERNATE 3515157-04)	GREEN
3515156-01	3515158-01	3515157-03 (ALTERNATE 3515157-05)	AMBER
PART NO	PART "A" (YOKE)	PART "B" (TUBE)	COLOR

THIRD ANGLE PROJECTION

[redacted] 3515152 ORION

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN ~~INCHES~~ AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

TOL ± | 2 PL -- | 3 PL — | ANLR —

REMOVE BURRS AND SHARP EDGES

DRILL TOL PER ANSI B89.1

INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

SIGNATURE		DATE
DRAWN BY	Hugo K M	9-9-83
CHK BY	B. Vogel	11-7-83
DFTG APVD	B. Vogel	11-7-83
ENGRG APVD	[illegible]	11-3-83
AUTH BY	[illegible]	11-3-83

PARTS LIST ☐

AMPEX

MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

YOKE / TUBE ASSY

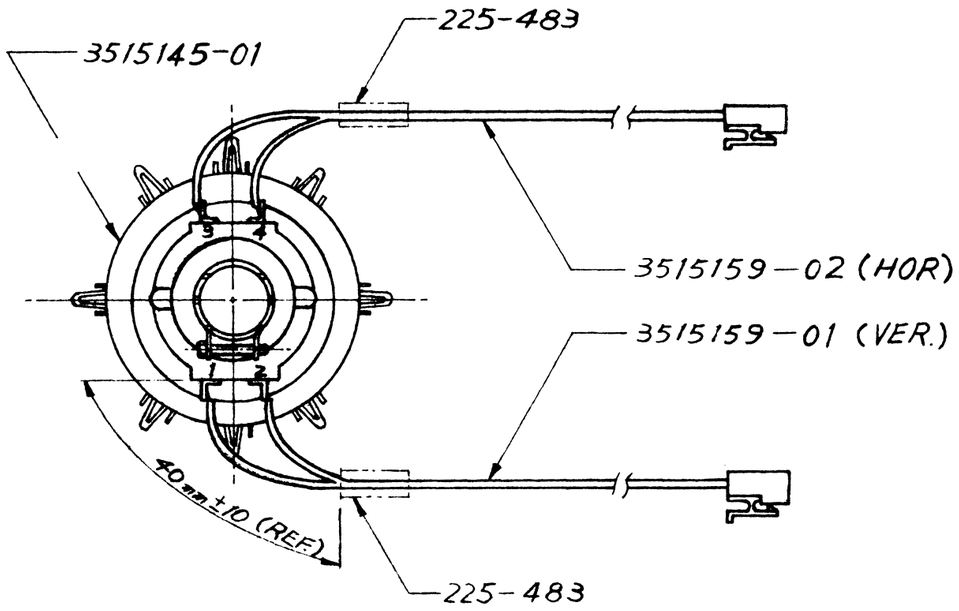
SIZE	CODE IDENT NO.	
D	09150	3515156

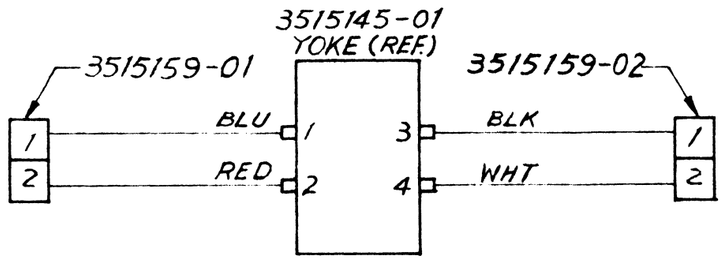
SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

MC-1004B (REV. NOV 78)
PRINTED IN U.S.A.

3515158

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE		
		DFTG	CHK	ENGRG
A	ERN0011	9-10-83	11-8-83	11-8-83
A	ERN0024 (CONT.)	2-24-84	3-2-84	3-2-84





WIRING DIAGRAM

4. METRIC ENGRG AND DFTG PRACTICES PER AMPEX STD MB1-3.
3. IDENTIFY PART NO, ISSUE LTR PER AMPEX SPEC 3124500, PARA 3.2
2. ASSEMBLE PER AMPEX STANDARDS, HC2-5.
1. PART NO. TO BE 3515158-01.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST [X]

3515156	ORION
NEXT ASSY	USED ON
APPLICATION	

NOTICE

THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT.

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN ~~INCHES~~ AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISH.

TOL ±		2 PL	3 PL		ANLR
		—	—		—

REMOVE BURRS AND SHARP EDGES

DRILL TOL PER AND 10387

INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

SIGNATURE		DATE
DRAWN BY	Jim M 71	9-10-83
CHK BY	B. Hatch	11-8-83
DFTG APVD	B. Hatch	11-8-83
ENGRG APVD	[illegible]	11-8-83
AUTH BY	[illegible]	11-8-83

AMPEX

COMPUTER PRODUCTS DIVISION
Marina del Rey, California 90291

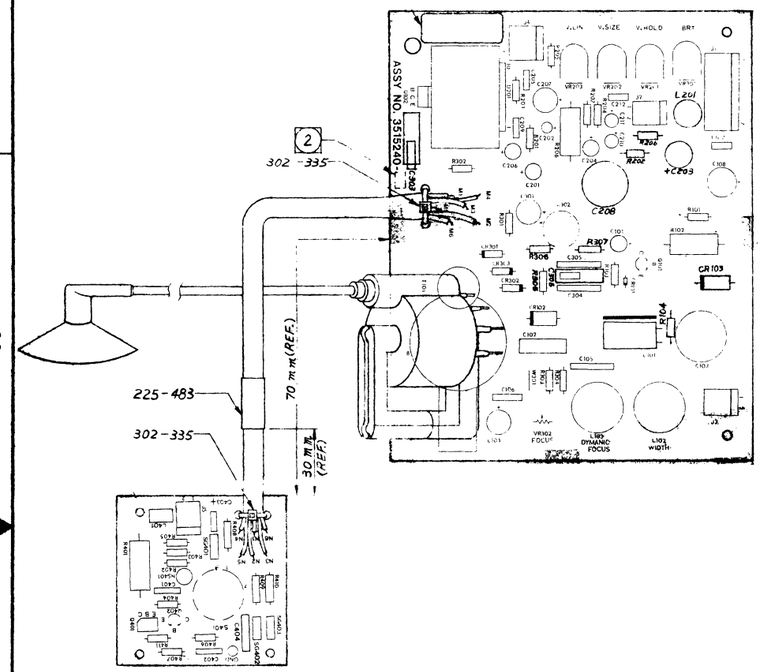
YOKE / CABLE ASSY

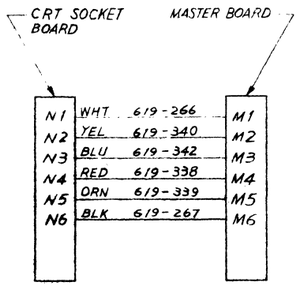
SIZE	CODE IDENT NO.	
B	09150	3515158

SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

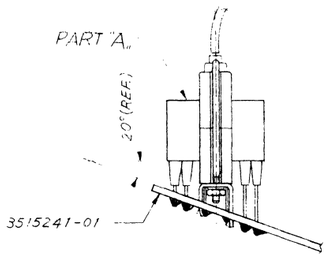
UC-3508-08 (REV NOV 72) PRINTED IN U.S.A.

3515240

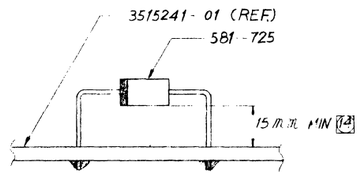




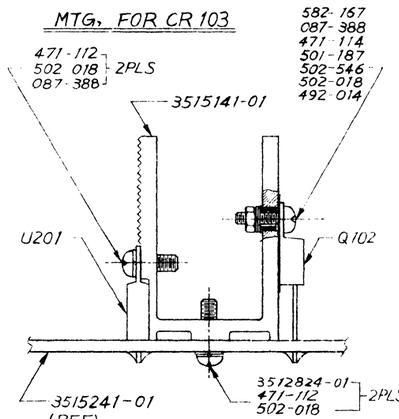
WIRING DIAGRAM FOR REF.



MTG. FOR T101



MTG. FOR CR103



VIEW : A-A

REVISIONS			SIGNATURE AND DATE		
LTR	ZONE	DESCRIPTION	DFTG	CHK	ENGRG
X		ECN 42105			
Y		ECN 42109			
Z		ECN 42113			
A1		ECN 42122			
AB		ECN 42134			
AC		ECN 42149			

REVISIONS			SIGNATURE AND DATE		
LTR	ZONE	DESCRIPTION	DFTG	CHK	ENGRG
A		NEVER RELEASE	—	—	—
B		NEVER RELEASE	—	—	—
C		NEVER RELEASE	—	—	—
D		NEVER RELEASE	—	—	—
E		ERN 0016	12-15-82	12-21-82	12-21-82
F		PCR 42010	12-20-82	12-20-82	12-20-82
G		PCR 42014	1-19-83	1-19-83	1-19-83
H		PCR 42015	2-14-83	2-16-83	2-16-83
H		ERN 0024 (CONT.)	2-16-83	2-16-83	2-16-83
J		ECN 42024	3-2-83	3-2-83	3-2-83
K		ECN 42038	4-11-83	4-11-83	4-11-83
L		ECN 42047	5-26-83	5-26-83	5-26-83
M		ECN 42057	6-16-83	6-16-83	6-16-83
N		ECN 42063	7-1-83	7-1-83	7-1-83
P		ECN 42068	7-27-83	7-27-83	7-27-83
R		ECN 42072	8-5-83	8-5-83	8-5-83
S		ERN 0054 (ADD-02)	8-5-83	8-5-83	8-5-83
T		ECN 42083	8-31-83	8-31-83	8-31-83
U		ECN 42085	9-2-83	9-2-83	9-2-83
V		ECN 42090	9-27-83	9-27-83	9-27-83
W		ECN 42102	10-28-83	11-9-83	11-9-83

(15) CUT TRACE BETWEEN LEADS OF L401. (FOR 3515240-02 ONLY)

(14) CLEARANCE BETWEEN BUTTOM SIDE OF CR103 AND BOARD IS 15 m m MIN.

13 MAX. LEAD PROTRUSION ON SOLDER SIDE IS 3.2 m m.

(12) ADHERE 3505530-01 APPROX AS SHOWN.

11 APPLY HOT MELT (018-531) TO HOLD PARTS Q401, C208, C302, C103, L101. TO PWBA RIGIDLY.

~~(10) AFTER FLYBACK SEATING IN PROPER POSITION TWIST 4 TABS OF FLYBACK MOUNTING BRACKET TO CONSOLIDATE FLYBACK ON BOARD.~~

9 METRIC ENGRG & DFTG PRACTICES PER AMPEX STD. MBI-3

8 ADHERE 3505530-01 APPROX AS SHOWN.

7 HEAVY LINE ON DIODE DENOTES CATHODE END.

6 PLUS SIGN ON CAPACITORS DENOTES POSITIVE END.

5 FOR SCHEMATIC SEE SH 3.

4 COMPONENT REF. DESIGNATIONS ARE FOR REF ONLY.

3 ASSEMBLY PER AMPEX STANDARDS, HC 2-5.

(2) MARK DASH NO., SERIAL NO. AND ISSUE LTR PER AMPEX SPEC 3124500, PARA 3.1.

1 PART NO. TO BE PER VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

SI metric

PARTS LIST ☐

3515152 ORION
NEXT ASSY USED ON
APPLICATION

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN ~~INCHES~~ AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL | 3 PL | | ANLR
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387.
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY	Leo Mc	11-25-83
CHK BY	E. Shiel	11-28-83
DFTG APVD	E. Shiel	11-28-83
ENGRG APVD	C. N. Hurst	11/28/83
AUTH BY	C. N. Hurst	11/28/83

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

PWBA - VIDEO BOARD

SIZE D | CODE IDENT NO. 09150 | 3515240
SCALE NONE | DO NOT SCALE THIS PRINT | SHEET 1 OF 3

3515240

LE-3284-00 (REV. NOV 72) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
AC		SEE SH. 1	—	—	—

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARKS	Q'TY
1	3515141-01		HEATSINK HOR/VER.	1
2	PART "A"	T101	X'FORMER HOR. OUTPUT	1
3	3515143-01	L103	COIL. FOCUS	1
4	3505211-01	L102	COIL, HOR. WIDTH	1
5	3515248-01	L101	COIL. HOR LINEARITY	1
6	PART "B"	L401 (FOR 02 ONLY)	COIL PEAKING	1
7	581-681	CR301	1N4003	1
8	013-871	CR302, CR303	1N4006	2
9	581-725	CR103	MR852/GI852	1
10	581-485	CR102	MR854/GI854	1
11	581-403	CR101	SWITCHING	1
12				
13	579-048	Q101	MPS9434J	1
14	580-647	Q402	2N3904	1
15	579-151	Q401	2N6553	1
16	579-154	Q102	BU806	1
17				
18	002-036	U201	μPC1031H2/LA1385	1
19				
20	075-364	VR203	2KΩ	1
21	075-365	VR202	20KΩ	1
22	075-366	VR201	50KΩ	1
23	075-367	VR301	500KΩ	1
24	075-376	VR302	2MΩ. X-201-RS	1
25				
26	066-834	R407, R103	33Ω. 5%. 1/4W	2
27	066-938	R411	47Ω. " " "	1
28	PART "C"	R406	SEE VERSION TABLE	1
29	066-835	R207	82Ω. " "	1
30	066-663	R402.	220Ω. " " "	1
31	066-814	R301	270Ω. " " "	1
32	066-665	R101. R208. R403	1KΩ. " " "	3
33	066-675	R404	1.8KΩ. " " "	1
34	066-666	R203	2.7KΩ. " " "	1
35	066-829	R201. R204. R205	6.8KΩ. " " "	3
36	066-847	R202	33KΩ. " " "	1
37	066-913	R304. R305. R307	220KΩ. " " "	3
38	066-673	R303	1MΩ. " " "	1
39	062-182	R408	1KΩ. " " 1/2W	1
40	062-199	R410. R409	10KΩ. " " 1/2W	2
41	079-425	R206	1Ω. " " 1W	1
42	079-427	F102	100Ω. " " 2W	1
43	059-885	R401	820Ω. " " 4W	1
44	066-560	R306	56Ω. " " 1/4W	1
45	PART "D"	R405	SEE VERSION TABLE	1

ITEM	PART NO.	DESCRIPTION	REMARKS	Q'TY
46	064-993	C402	120PF. 50V. ±5%	1
47	064-975	C107, C401	0.1μF. 50V. +80 -20 %	2
48	030-299	C106	0.001μF. 1KV. 20%	1
49	030-129	C105. C304. C305. C404	0.01μF. 1KV. 20%	4
50	064-410	C212. C209. C205	0.047μF. 50V. 20%	3
51	3515584-01	C303, C306	0.33μF. 250V. 20%	2
52	3512840-03	C102	0.022μF. 400V. 5%	1
53	037-493	C202	1μF. 15V. 20%	1
54	067-116	C210, C211	22μF. 10V. 10%	2
55	063-459	C101. C201. C204	10μF. 16V. 20%	3
56	063-552	C207	100μF. 10V. 10%	1
57	063-460	C206	47μF. 16V. +50 -75 %	1
58	063-461	C108. C203	220μF. 16V. +10 -75 %	2
59	063-462	C208	2200μF. 16V. +10 -75 %	1
60	063-553	C104	100μF. 25V. +10 -75 %	1
61	063-554	C302	100μF. 80V. +10 -75 %	1
62	063-551	C403	10μF. 100V. +10 -75 %	
63	3515299-01	C103	6.8μF. 25V. 20%	1
64	063-564	C301	10μF. 160V. +10 -50 %	1
65				
66	064-984	SG402. SG403	SPARK GAP 1KV. GAP-R75	2
67				
68	060-049	NS401 NS402	NEON LIGHT. 105VAC. 2mA	2
69	012-270	S401	SOCKET. 7P. CRT BASE	1
70				
71	135-534	J1	HEADER. 7P	1
72	135-530	J2. J3. J5	HEADER. 2P	3
73	135-531	J4	HEADER. 3P	1
74				
75	177-352	GND	PIN DISCONNECT	1
76	615-012	W301	WIRE SOLID BARE #20	1
77				
78	066-838	R104	330Ω 5% 1/4W	1
79	066-590	R302	68KΩ 5% 1/4W	1
80	3515538-01	L201. CHOKE		1
81				
82				
83				
84				
85				
86				
87				
88				
89				
90				

PWBA VERSION	PART "A"	PART "B"	PART "C"	PART "D"
3515240-02	3515142-02	3515296-01 (15)	066-855 1/4W, 39 OHM	066-838 1/4W, 330 OHM
3515240-01	3515142-01	— — —	066-938 1/4W, 47OHM	066-663 1/4W 220 OHM

VERSION TABLE

3515240

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
AC		SEE SH. 1			

HV 14 KV

T101 (PART "A")

CR 301 IN4003 · R301 270 · (-90V) · R302 68K · J4-3 BRI CONTRL 500 K · J4-2 · J4-1

C301 10u/160V

CR302 IN4006 (+600V)

55V

CR306 IN4006 · R306 56 · C306 .33 250V · C302 100u/80V · R307 220K

VR301 500K · C303 .33u/250V · TO J1-1 +12V

J1-1 +12V, HOR. · M5

R102 100/2W · C108 220u 16V · C107 .1u · C101 10u/16V

R101 1K · Q101 MPS 9434J · CR101 SWITCHING · R103 33 · Q102 BU807 · CR102 MR 854 OR G1854 · C102 .022u

J1-7 SYNC HOR · J1-6 GND, HOR SYNC · J1-2 GND, HOR

CR103 MR852 OR G1852 · +12V · C104 100u/25V · C105 .01u/1KV

L103 DYMANIC FOCUS · L102 WIDTH · L101 H. LIN

C103 6.8u/25V NON-POLOR · R104 330

R305 220K · R303 1M · C304 .01u/1KV · C305 .01u/1KV · C106 .001u 1KV · VR302 2M FOCUS. · R304 220K · W301

M1 · M2 · M3 · M6

N1 · N2 · N3 · N6

R408 1K ½W · NS402 · E1

R410 10K ½W · SG402 · C404 .01/1KV · E6

R409 10K ½W · SG403 · E7

CRT GND

E3

E4 HEATER CATHODE NS401 · E2

L401 (PART "B")

+60V · N4 · C403 10u/100V · R401 820/4 W · R402 220

+12V · N5 · R403 1.0K · Q401 2N6553 · R404 1.8K · C401 .1/50V

VIDEO · R411 47 · Q402 2N 3904 · R405 (PART "D") · R406 (PART "C") · R407 33 · C402 120P 5%

VIDEO GND

J5-2 · J5-1

J1-3 +12V, VER · L201

J1-5 SYNC, VER

(V.HOLD) VR201 50K · C203 220u/25V · C201 10u/10V · R202 33K · R201 6.8K · C202 1u/25V · R203 2.7K

μPC 1031H2 U201 (TAB)

R205 6.8K · R206 1/1W · C207 100u/10V · C208 2200u/16V · C206 47u/10V · V. LIN VR203 2KB · C209 .047/50V · R207 82 · C211 22u/10V · C212 .047/50V · R208 1K

C204 10u/10V · VR202 20KB (V SIZE) · R204 6.8K · C210 22u/10V · C205 .047u

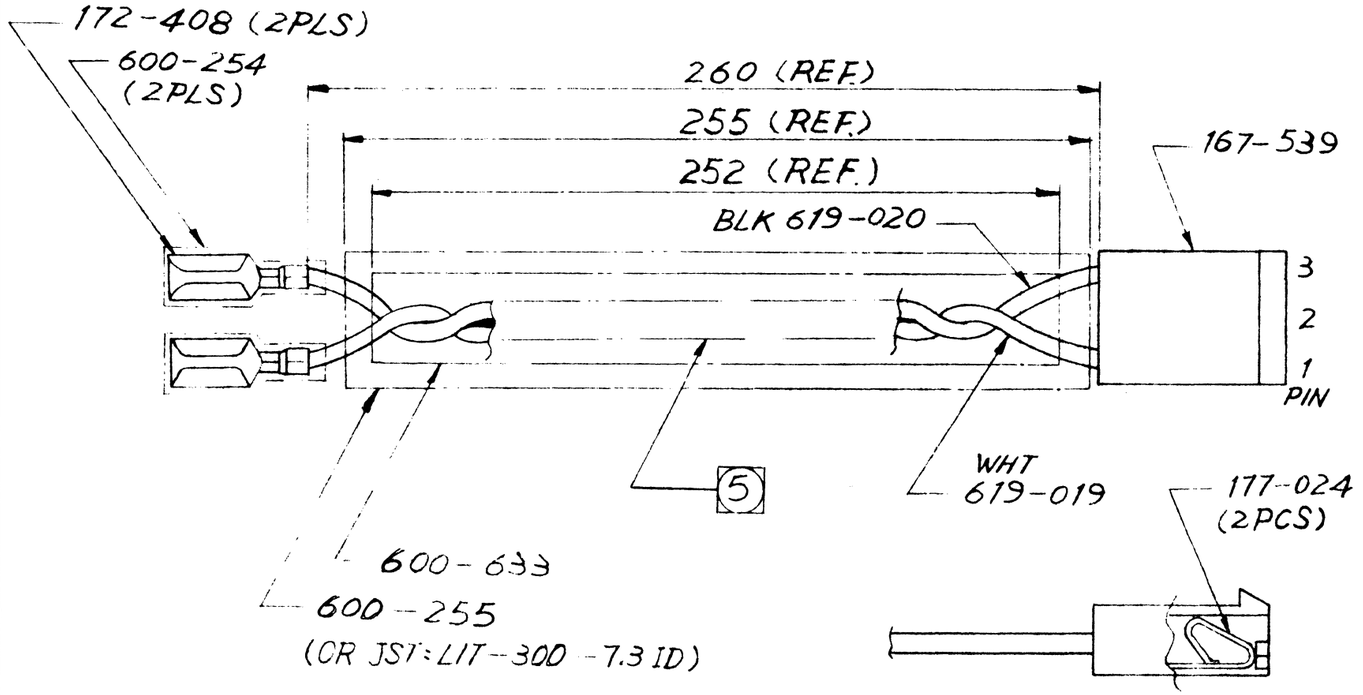
J1-4 GND, VER

J3-1 · J3-2 · J2-1 · J2-2

SIZE	CODE IDENT NO	
D	09150	3515240
SCALE NONE		SHEET 3 OF 3

PRINTED IN U.S.A.

[3515318]



REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE		
		DFTG	CHK	ENGRG
A	ERN 0067 (CONT.)	SY 10-30-84	B. Keith 10-30-84	C N Hsieh for 10-30-84
B	ECN 42141	SY 3-22-85	B. Keith 3-22-85	3-22-85

5 TWIST PAIR SHOULD BE 24 TURNS MIN. FOR ALLOVER LENGTH WIRES ARE 260 mm LG. AFTER TWISTING.

4 METRIC ENGRG & DFTG PRACTICES PER AMPEX STD. MB 1-3.

3 ASSEMBLE PER AMPEX STANDARDS, HC2-5.

2 IDENTIFY PART NO. & ISSUE LTR PER AMPEX SPEC 3124500 PARA 3.2.

1 PART NO. TO BE 3515318-01.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST ☐

3515130	ORION
NEXT ASSY	USED ON
APPLICATION	

NOTICE

THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT.

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISH.

TOL ±		2 PL	3 PL		ANLR
		----	----		----

REMOVE BURRS AND SHARP EDGES

DRILL TOL PER AND 10387

INTERPRET DRAWING PER ANSI Y14.5

MATERIAL: ———

FINISH: ———

SIGNATURE		DATE
DRAWN BY	SY	10-30-84
CHK BY	B. Keith	10-30-84
DFTG APVD	B. Keith	10-30-84
ENGRG APVD	C N Hsieh for SY	10-30-84
AUTH BY	C N Hsieh for	10-30-84

AMPEX — COMPUTER PRODUCTS DIVISION, Marina del Rey, California 90291

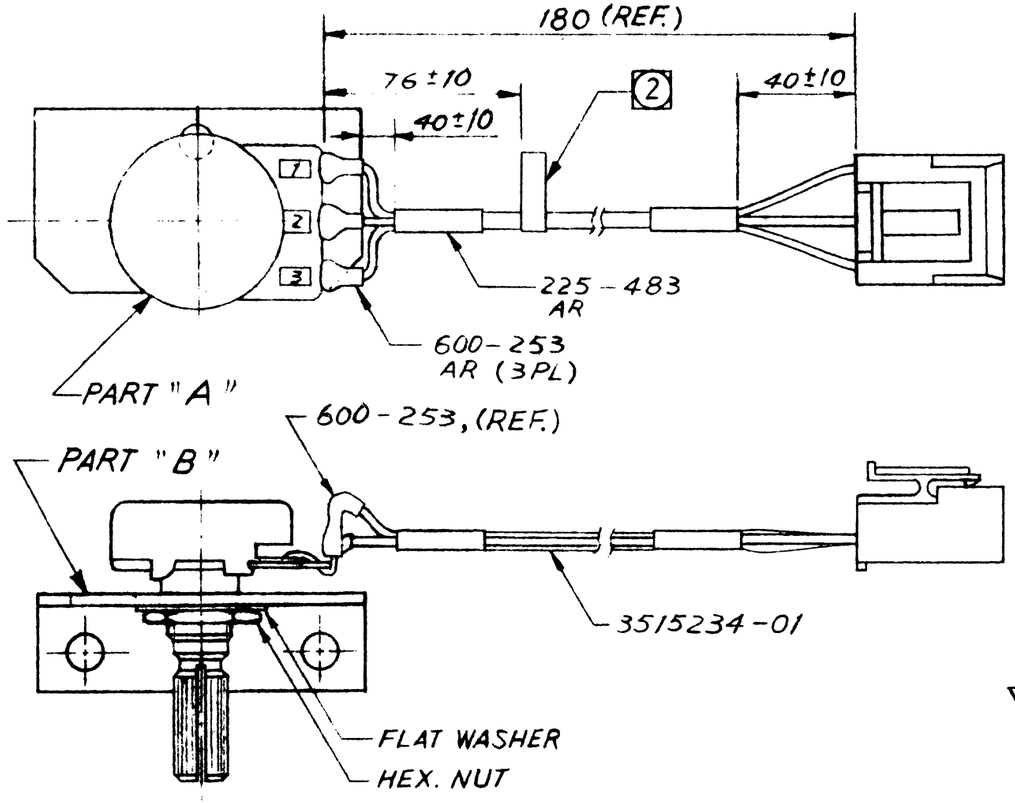
CABLE ASSY — A.C POWER JUMPER

SIZE	CODE IDENT NO.	
B	09150	3515318

SCALE NONE — DO NOT SCALE THIS PRINT — SHEET 1 OF 1

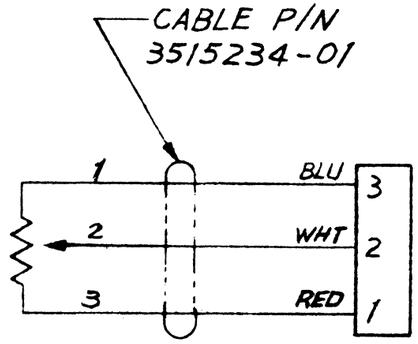
3515233

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A	NEVER REL			
B	ERN 0011	11-8-83	11-8-83	11-8-83
C	PCR 42010	12-20-83	12-20-83	12-20-83
C	ERN 0024 (CONT.)	2-24-84	2-2-84	3-3-84
D	ECN 42031	3-19-84	3-19-84	3-19-84
E	ERN 0069 (ADD-02)	11-20-84	11-20-84	11-20-84



4. METRIC ENGRG AND DFTG. PRACTICES PER AMPEX STD MB1-3
3. ASSEMBLE PER AMPEX STANDARDS, HC2-5.
(2) IDENTIFY PART NO. AND ISSUE LTR. PER AMPEX SPEC 3124500, PARA 3.1 .
1. PART NO. TO BE PER VERSION TABLE.

NOTES. UNLESS OTHERWISE SPECIFIED



SCHEMATIC DIAGRAM

PART NO.	PART "A"	PART "B"	REMARKS
3515233-02	3515309-01	3515380-01	
3515233-01	075-316	3513439-01	

VERSION TABLE

PARTS LIST (X)

3515152	ORION
NEXT ASSY	USED ON
APPLICATION	

NOTICE

THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISH.
TOL ± | 2 PL | 3 PL | ANLR
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY	Lino M 11	10-29-83
CHK BY	B. Hall	11-8-83
DFTG APVD	B. Hall	11-8-83
ENGRG APVD	[illegible]	11-8-83
AUTH BY	[illegible]	11-8-83

AMPEX
COMPUTER PRODUCTS DIVISION
Marina del Rey, California 90291

INTENSITY CONTROL ASSY

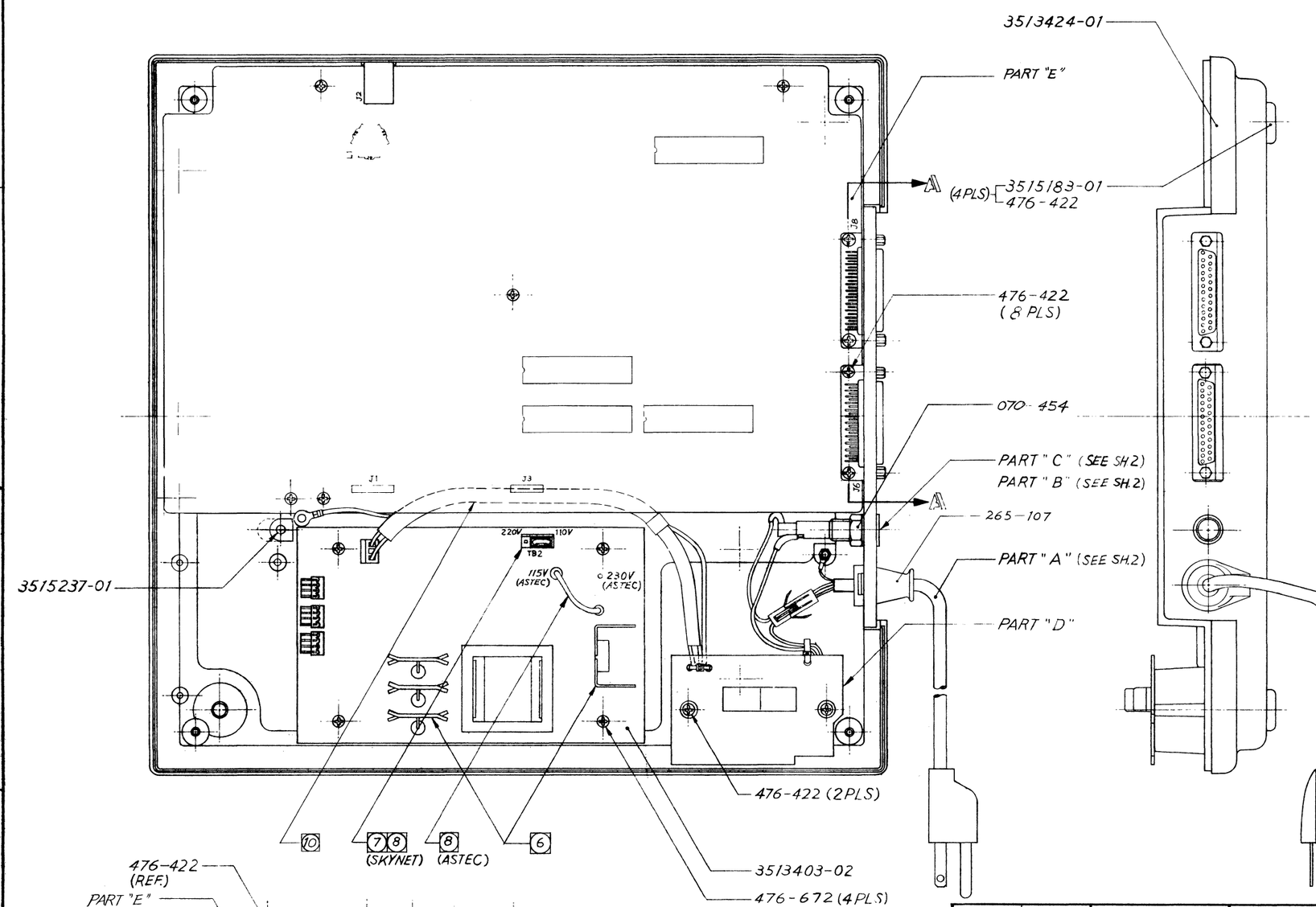
SIZE	CODE IDENT NO.	
B	09150	3515233

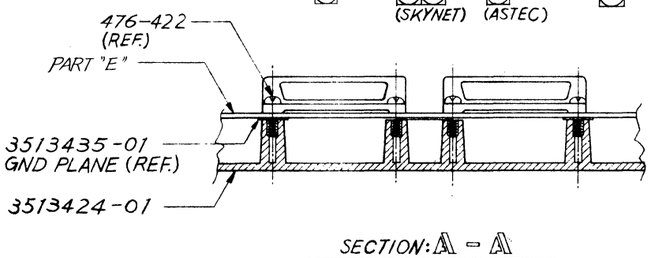
SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

UC-3502-08 (REV NOV 72) PRINTED IN U.S.A.

3515333

REVISIONS					
LTR	ZONE	DESCRIPTION	DATE	CHK	APVD
A		ERN 0052 (CONT.)			
B		ECN42082			
C		ECN42089			
D		ECN 42092			
E		ECN42100			
F		ECN42103			
G		ECN 42106			
H		ECN 42120			
J		ECN42153			





SECTION: A - A

(10) DRESS AC POWER JUMPER WIRES UNDER CONTROL BOARD & AS CLOSE TO GROUND PLANE AS POSSIBLE.

(9) AC POWER CONNECTION :
FOR 115V – SEE SH.1 ZONE B-5 & SH.2 AC WIRING DIAGRAM.
FOR 220V – SEE SH.2 ZONE D-2 VIEW E-E & AC WIRING DIAGRAM.

(8) FOR 220V APPLICATION . SHIFT 3P CONNECTOR OF TB2 TO LEFT SIDE 1 POSITION AS SHOWN IN SH1 ZONE B-6 WHEN USE SKYNET P/S PWBA ; PULL AND INSERT SINGLE PIN CONNECTOR FROM 115V PIN POSITION TO 230V PIN POSITION AS SHOWN IN SH1 ZONE B-6 WHEN USE "ASTEC" P/S PWBA .

(7) DRESS AC POWER JUMPER WIRES THREAD THRU WIRE LOOP OF TB2 CONNECTOR OF SKYNET P/S PWBA TO KEEP WIRES AWAY FROM HEAT SINKS .

(6) DRESS ALL WIRES AWAY FROM HEAT SINKS OF P/S PWBA.

(5) ADHERE GROUND PLANE INSULATOR TO GROUND PLANE . PROPERLY AS SH. 2 DOT LINES SHOWN WITH "3M" DOUBLE SIDE ADHESIVE TAPE "400 ½" TO AVOID LIFT UP.

4 METRIC ENGRG & DRAFTING PRACTICES PER AMPEX STD. MBP1

3 MARK PART NO., ISSUE LTR . SERIAL NO PER AMPEX SPEC. 3124500 PARA 3.1 .

2 ASSEMBLE PER AMPEX STD.

1 PART NO. TO BE PER VERSION TABLE . (SEE SH.2)

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST [X]

THIRD ANGLE PROJECTION

3515331	ORION
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL | 3 PL | ANLR
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:
FINISH:

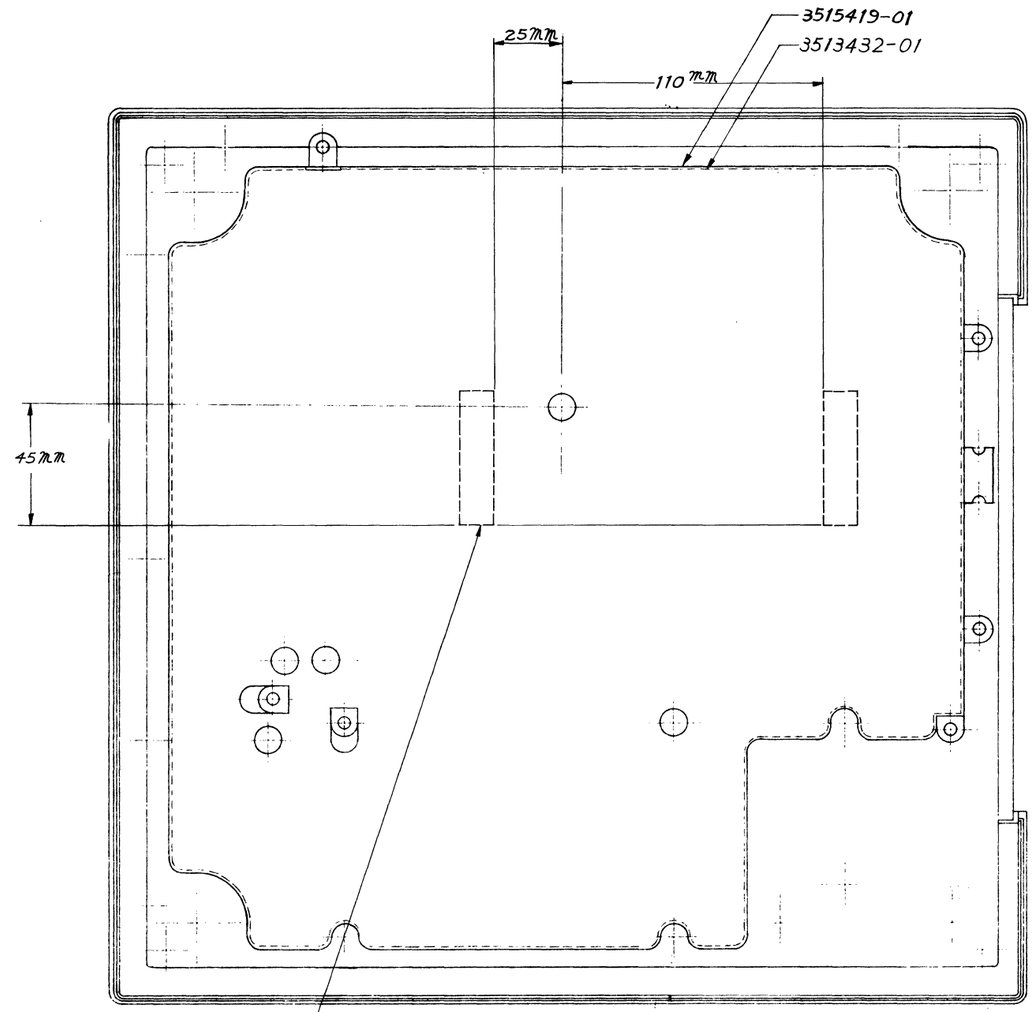
SIGNATURE		DATE
DRAWN BY		7-31-84
CHK BY		7-31-84
DFTG APVD		7-31-84
ENGRG APVD		7-31-84
AUTH BY		7-31-84

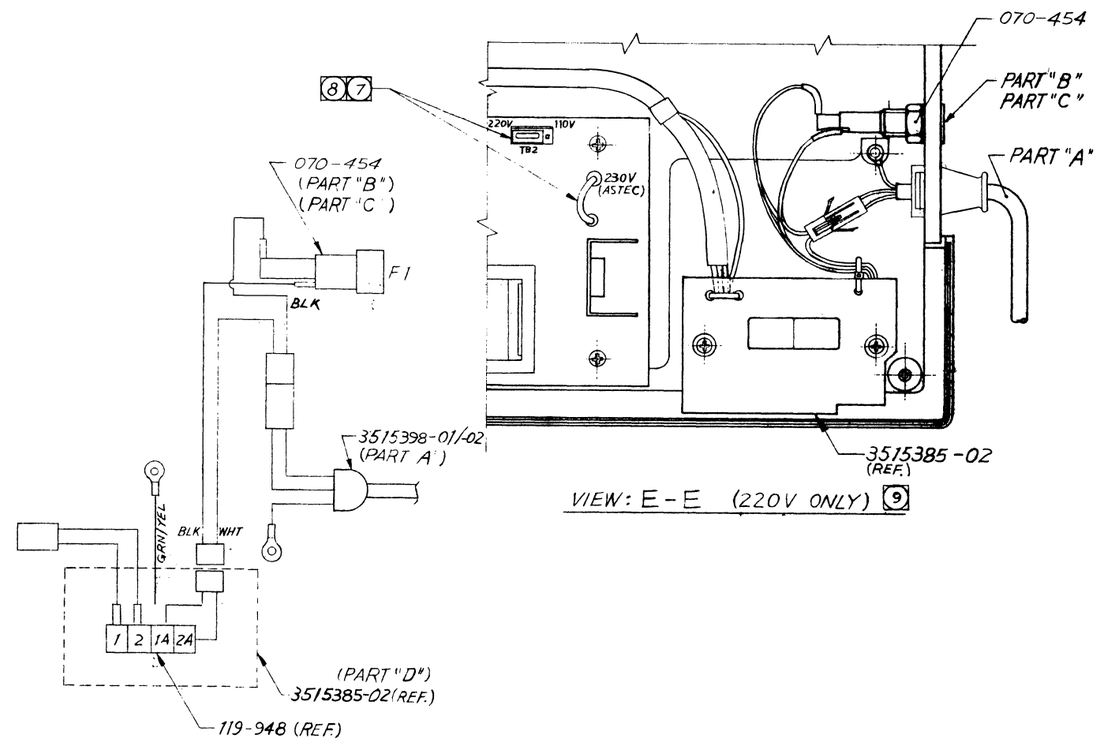
AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

PEDESTAL ASSY

SIZE	CODE IDENT NO.	
D	09150	3515333
SCALE	DO NOT SCALE THIS PRINT	SHEET 1 OF 2

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFTG	CHK	ENGRG
H		SEE ST.1			





VIEW: E-E (220V ONLY) 9

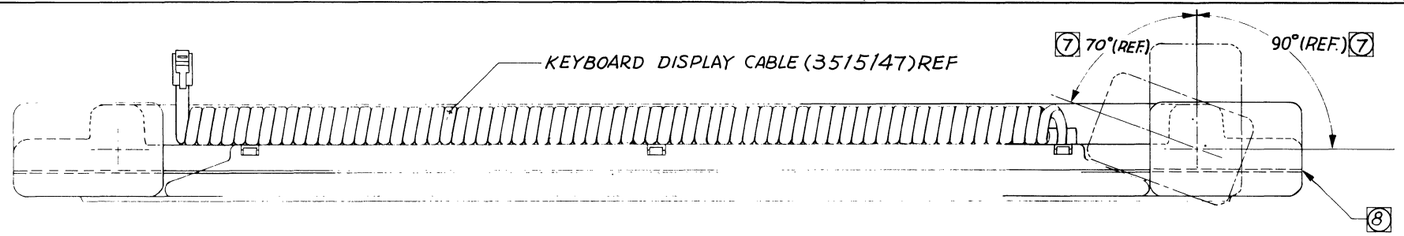
AC / WIRING DIAGRAM 9

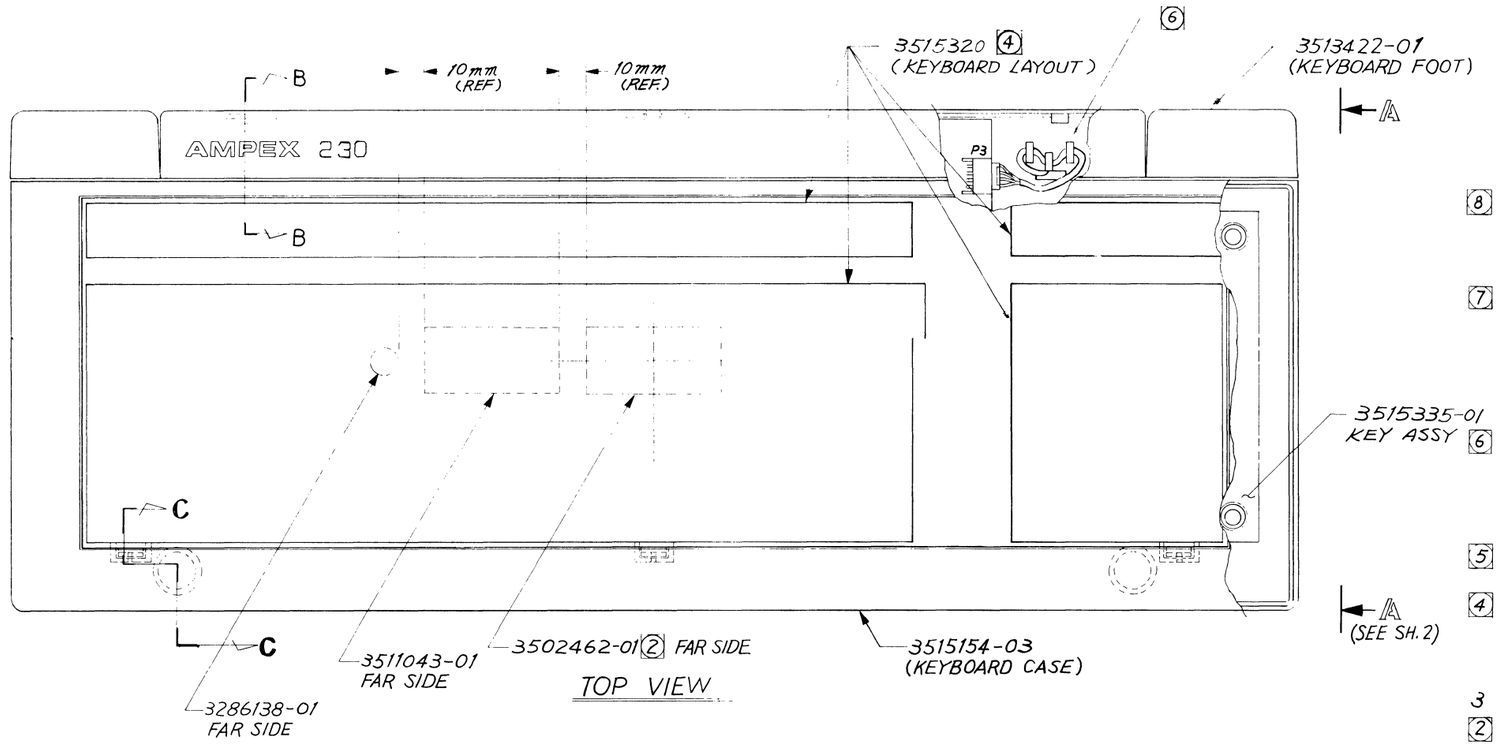
PART NO.	PART "A" AC POWER CORD	PART "B" FUSE PART CAP	PART "C" FUSE	PART "D" PWBA-ON-OFF SWITCH /FILTER	PART "E" CONT. PWBA	REMARK
3515333-02	3515398-02	070-413	070-467 ALTERNATE 070-471	3515385-01	3515400-02	220V
3515333-01	3515398-01	070-412	070-312	3515385-01	3515400-05	115V

VERSION TABLE

SIZE	ZONE IDENT NO	3515333
D	09150	
FSCM NO.		SHEET 2 OF 2

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0052 (CONT.)	7-31-86	7-31-86	
B		ERN 0087 (ADD -02 ~ -09)	7-31-86	7-31-86	





8 THE MECHANICAL ALIGNMENT MUST ALLOW THE KEYBD BASE TO FIT INTO COVER ASSEMBLY TO INSURE 1.02 mm MATE (ACCENT) LINE IS CONSISTANT ALL AROUND.

7 ROTATE BOTH KEYBOARD FOOTS 90° AND 70° AS SHOWN TO INSURE ROTATION & HEIGHT ARE CONSISTENT, THEN ROTATE THEM BACK TO HORIZONTAL POSITION.

6 DRESS KEYBOARD DISPLAY CABLE INTO 3 PLASTIC HOOKS OF INSIDE KEYBOARD BASE PROPERLY AND PULL CABLE FROM OUTSIDE TO INSURE NO LOOSEN CABLE.

5 MOUNT BUMPER FOOT (P/N. 250-155) AS SHOWN

4 ALIGN KEY ASSEMBLY INTO TOP PLATE SO THAT ALL KEYS ARE FREE TO MOVE WITH .05 mm CLEARANCE MIN. AFTER ASSEMBLY.

3 ASSEMBLE PER AMPEX STANDARDS.

2 IDENTIFY PART NO, ISSUE LETTER AND SERIAL NO. PER AMPEX SPEC 3124500 LOCATE LABEL APPROX WHERE SHOWN.

1 PART NO. TO BE PER VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

3515334

PARTS LIST ☐

FINAL ASSY	A 230
NEXT ASSY	USED ON
APPLICATION	

NOTICE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN ===== AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOL ± | 2 PL — | 3 PL — | ANLR —
REMOVE BURRS AND SHARP EDGES DRILL TOL PER AND 1038
INTERPRET DRAWING PER ANSI Y14.5

SIGNATURE		DATE
DRAWN BY	Lisa MM	7-31-86
CHK BY	Bob	7-31-86
DFTG APVD		7-31-86
ENGRG APVD		
AUTH BY		

MATERIAL:
FINISH:

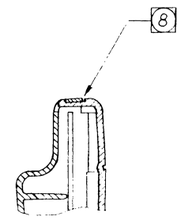
AMPEX — MEMORY PRODUCTS DIVISION, 200 N Nash Street, El Segundo California 90245

CRT KEYBOARD ASSY
(BASIC DWG.)

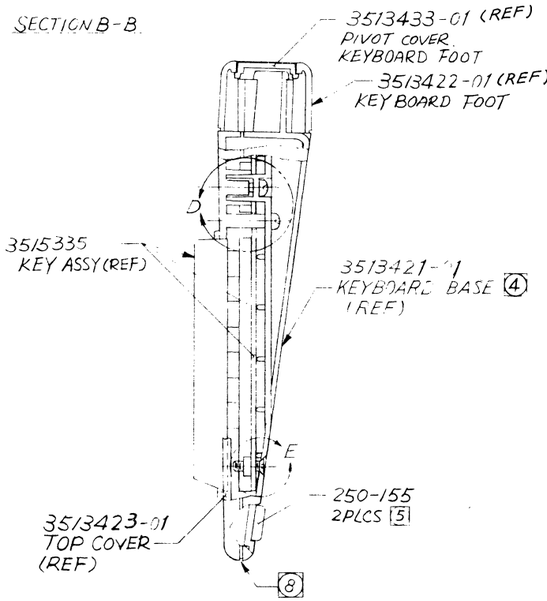
SIZE	CODE IDENT NO	
D	09150	3515334

SCALE — 1/2

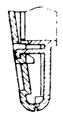
REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
B		SEE SH.1	—	—	—



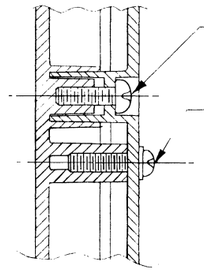
SECTION B-B



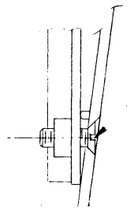
VIEW: A-A (SEE SH.1)



SECTION C-C



VIEW: D



VIEW: C

VERSION TABLE				
FINAL ASSY PART NO.	KEY ASSY		LANGUAGE	REMARKS
3515334-01	3515335-01		USA/U.K	A230
3515334-02	3515335-02		USA/U.K	A219
3515334-03	3515335-03		SWEDISH	A230
3515334-04	3515335-04		SPANISH	A230
3515334-05	3515335-05		ITALIAN	A230
3515334-06	3515335-06		NORWEGIAN	A230
3515334-07	3515335-07		GERMAN	A230
3515334-08	3515335-08		FRENCH	A230
3515334-09	3515335-09		DANISH	A230

3515334

SIZE	CODE IDENT NO.	
D	09150	3515334
SCALE NONE		SHEET 2 OF 2

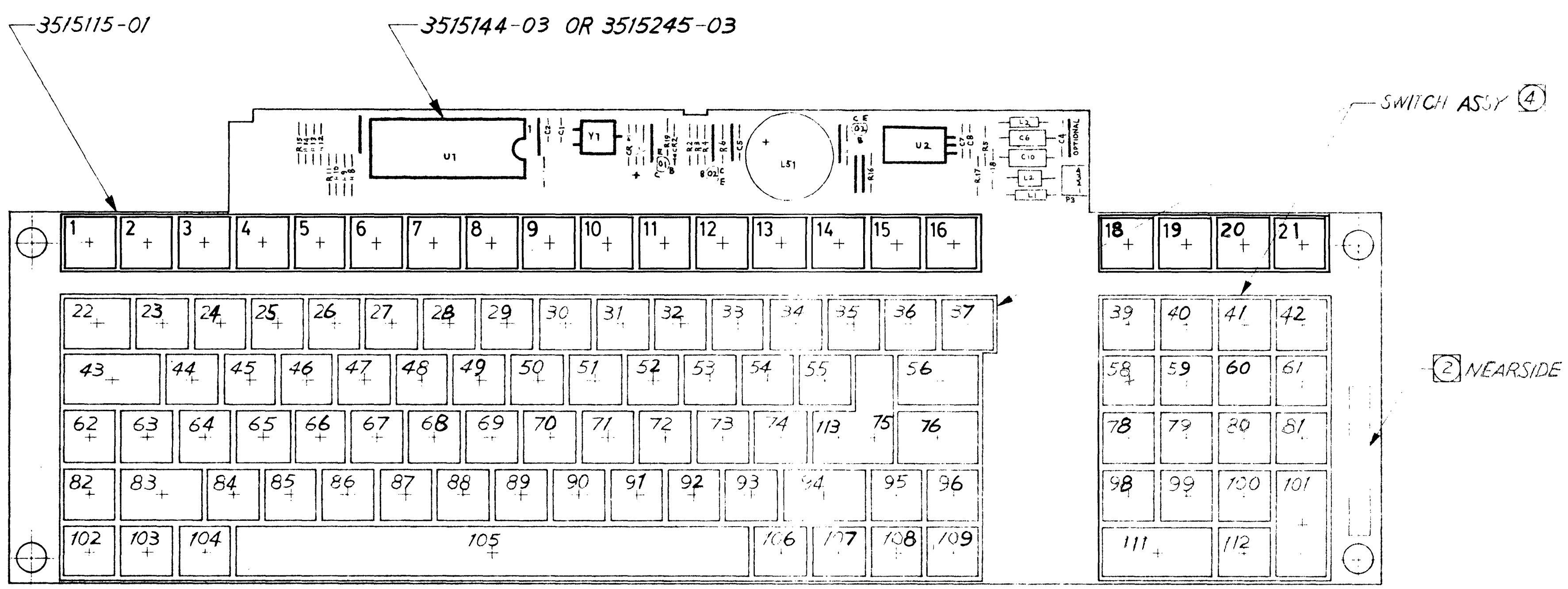
US 2004-08 (REV. DEC. 71)
PRINTED IN U.S.A.

3515335

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0049 (CONT.)	L. Hwang 7-3-84	B. Keith 7-3-84	7-3-84
B		ECN42075	8-17-84	B. Keith 8-17-84	8-17-84
C		ERN 0087 (ADD-02~-09)	SY Huang 3-1-85	3-1-85	3-1-85

VERSION TABLE

PART NO.	SWITCH ASSY	KEYTOP LEGEND	REMARK
3515335-01	3513458-01	3515320	
3515335-02	3513458-01	3515530	
3515335-03	3513458-01	3515321	
3515335-04	3513458-01	3515322	
3515335-05	3513458-01	3515323	
3515335-06	3513458-01	3515324	
3515335-07	3513458-01	3515325	
3515335-08	3513458-01	3515326	
3515335-09	3513458-01	3515327	



4 KEYTOP LEGEND PER VERSION TABLE.

3 PART NO. TO BE PER VERSION TABLE

2 MARK PART NO AND ISSUE LETTER PER AMPEX SPEC 3124500 PARA 3.1.

1 PLACEMENT OF COMPONENTS SHOWN FOR REF ONLY. ACTUAL PLACEMENT MAY VARY

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST X

APPLICATION	
NEXT ASSY	USED ON
3515334	II

NOTICE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

TOL		2 PL	3 PL		ANLR
±		---	---		---

REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

	SIGNATURE	DATE
DRAWN BY	L. Hwang	7-3-84
CHK BY	Hsiao KN	7-3-84
DFTG APVD	B. Keith	7-3-84
ENGRG APVD		7-3-84
AUTH BY		7-3-84

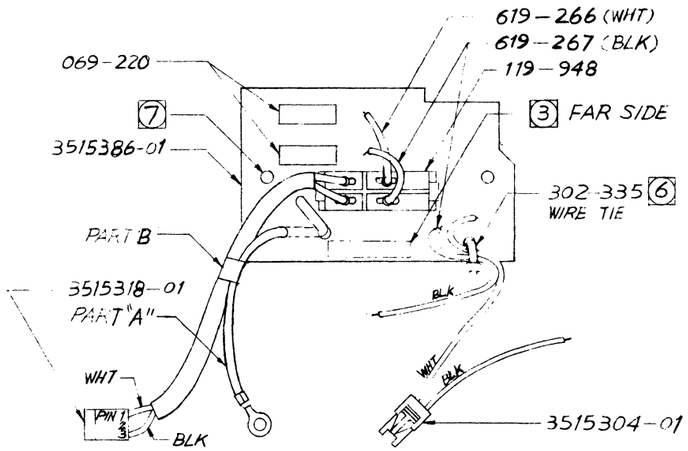
AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo California 90245

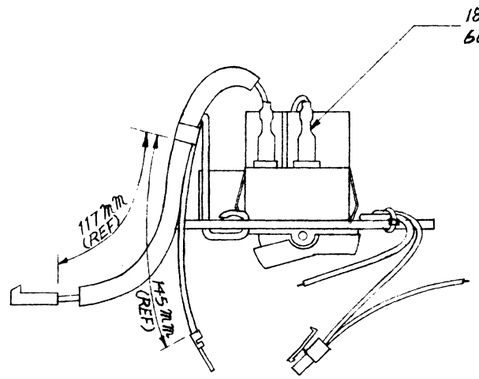
SIZE	CODE IDENT NO.	
D	09150	3515335

SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

3515335

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0072 (CONT.)	SY Huang 12-7-84	B. Nail 12-7-84	12-7-84





7 ADD SOLDER AROUND COPPER PAD OF MTG HOLE.

6 MAKE SURE BOTH BLACK & WHITE WIRES NOT TO TOUCH BOARD SHARP EDGE. WIRES SHOULD BE WRAPPED TO BOARD SURFACE TIGHTLY ENOUGH.

5 COMPONENT REF. DESIGNATIONS ARE FOR REF. ONLY.

4 METRIC ENGRG & DFTG PRACTICES PER AMPEX STD MB 1-3.

3 IDENTIFY P/N & ISSUE LTR. PER AMPEX SPEC 3124500 PARA 3.1.

2. ASSEMBLE PER AMPEX STD. HC 2-5

1. PART NO. SEE VERSION TABLE.

NOTES: UNLESS OTHERWIES SPECIFIED

PART NO.	PART "A"	PART "B"
3515385-02	———	———
3515385-01	3515205-01	225-487

VERSION TABLE

PARTS LIST ☐

NEXT ASSY	USED ON
	ORION

APPLICATION

NOTICE

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UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.

TOL ±		2 PL	3 PL		ANLR
		—	—		—

REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387

INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:

FINISH:

SIGNATURE		DATE
DRAWN BY	SY Huang	12-6-84
CHK BY	B. Nail	12-7-84
DFTG APVD	B. Nail	12-7-84
ENGRG APVD	[illegible]	12-7-84
AUTH BY	[illegible]	12-7-84

AMPEX

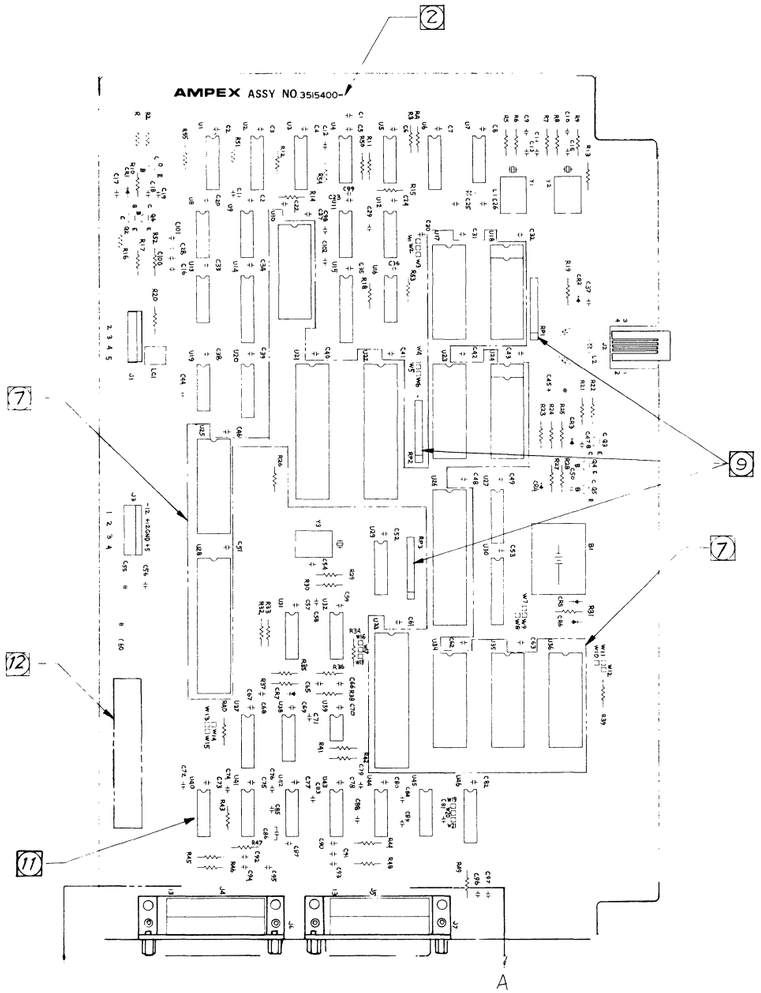
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

PWBA-ON-OFF SWICH / FILTER

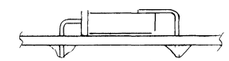
SIZE	CODE IDENT NO.	
C	09150	3515385

SCALE NONE | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

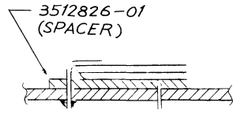
REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		ERN 0063 (CONT.)	SY 10-1-84	Jam 10-1-84	CNH 10-1-84
D		ECN 42104	SY 12-12-84	[illegible] 12-12-84	[illegible] 12-12-84
E		ERN 0073 (ADD-02)(CONT.)	SY 12-17-84	[illegible] 12-17-84	[illegible] 12-17-84
F		ECN 42114	SY 12-21-84	[illegible] 12-21-84	[illegible] 12-21-84
G		ECN 42117	SY 1-3-85	[illegible] 1-3-85	[illegible] 1-3-85
H		ECN 42119	SY 1-8-85	[illegible] 1-8-85	[illegible] 1-8-85
J		ERN 0075 (ADD-03)	SY 1-8-85	[illegible] 1-8-85	[illegible] 1-8-85
K		ECN 42131	SY 1-31-85	[illegible] 1-31-85	[illegible] 1-31-85
L		ECN 42138	SY 2-5-85	[illegible] 2-5-85	[illegible] 2-5-85
M		ECN 42150	SY 2-19-85	[illegible] 2-19-85	[illegible] 2-19-85
N		ECN 42151	SY 2-21-85	[illegible] 2-21-85	[illegible] 2-21-85
P	☆	ERN 0095 (ADD-04,-05,-06)	SY 5-20-85	[illegible] 5-20-85	[illegible] 5-20-85



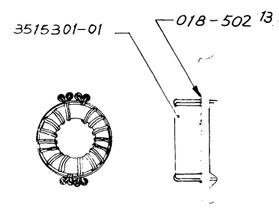
SECTION : A-A



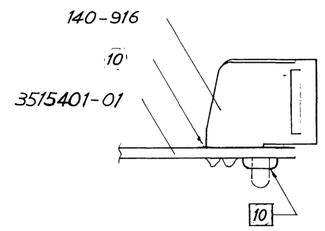
MTG FOR Y1, Y2, Y3



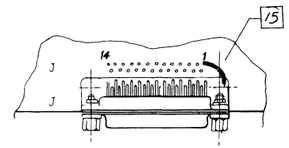
MTG FOR B1 (G.E. BATTERY)



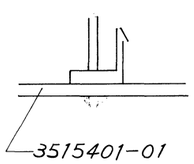
MTG FOR L2 (3515301-01)



MTG. FOR J2



VIEW: B 15



MTG FOR J1, J3

18 FOR REWORK INSTRUCTIONS TO PWBA'S USING "A" ISSUE A/W SEE ECN 42104.

17 HAND SOLDER THESE HOLES AFTER FLOW SOLDERING.

16 WHEN USE ALTERNATE PARTS 579-161 SHOULD BE INSTALLED IN Q6 (SEE SH. 2)

15 FOR DDK STYLE RS232 CONNECTOR (P/N 140 900) ADD ONE SOLID JUMPER WIRE BETWEEN MTG. SCREW & PIN1 HOLE OF J6 & J7 AS SHOWN. (SEE VIEW: "B")

14 OBSERVE "STATIC CHARGE" PRECAUTION WHEN HANDLING SEMICONDUCTOR DEVICES.

13 ASSEMBLE PER AMPEX STANDARDS HC-2-17.

12 ADHERE MASR LABEL TO THIS AREA AFTER MARKING PART NO & REV. LETTER .

11 FOR CURRENT LOOP USE ONLY.

10 HEAT SEAL 2 PLASTIC INTERLOCKER OF J2 TO CONSOLIDATE J2 TO BOARD. OR BOND IT TO BOARD WITH 018-502 ADHESIVE

9 PIN1 OF RESISTOR PACK SHOULD BE ORIENTED ON BOTTOM SIDE.

8 UNUSED IC POSITIONS : ARE TO BE KEPT FREE OF SOLDER.

7 FOR INSTALLATION OF EPROM OR ROMS AT : U10, U34, U35, SEE VERSION TABLE. (SH. 2) SOCKETS ARE PROVIDED AT : U10, U17, U23, U33 ~ U36, U40 ,

6 MAX. LEAD PROTRUSION ON SOLDER SIDE IS 2.3 mm

5 ASSEMBLE PER AMPEX STANDARDS.

4 COMPONENT DESIGNATION ARE FOR REFERENCE ONLY.

3 FOR SCHEMATIC DIAGRAM SEE SHEET 3 THRU 6 .

2 MARK DASH NO. SERIAL NO. AND ISSUE LETTER PER AMPEX SPEC 3124500 PARA, 3.1 .

1 PART NO. SEE VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

3515333 ORION II
NEXT ASSY USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL | 3 PL | ANLR
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

	SIGNATURE	DATE
DRAWN BY	SY	10-1-84
CHK BY	[illegible]	10-1-84
DFTG APVD	[illegible]	10-1-84
ENGRG APVD	CNH	10-1-84
AUTH BY	CNH	10-1-84

PARTS LIST ☐

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

PWBA TERMINAL CONTROLLER

SIZE	CODE IDENT NO.	
D	09150	3515400
SCALE	DO NOT SCALE THIS PRINT	SHEET 1 OF 6

UC-35408 (REV NOV 77)
PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
P		SEE SH.1			

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARK
1			
2			
3	590-244	U25	Z80A CTC
4	589-619	U33	Z80A CPU
5	003-206	U28	Z80A DART
6	001-908	U36 ALTERNATE: 003-200, 003-205, 003-168	CMOS SRAM
7	590-983	U17, U18, U23, U24	SRAM
8	PART "C"	U10	CHARGEN MROM
9	PART "A"	U34	SYSTEM ROM1
10	PART "B"	U35	" " 2
11	3515348-01	U22	BUS INTERFACE
12	3515495-01	U21 ALTERNATE: 3515349-01	CRT CONTROLLER
13	003-136	U26	SCN2672AC4N40
14	589-537	U14, U15, U30	74 LS 374
15	003-119	U6 ALTERNATE 003-203	74 AS 163
16	587-410	U46	74 LS 139
17	587-534	U13, U45	74 LS 08
18	587-523	U11, U19, U38, U47	74 LS 32
19	586-830	U7 ALTERNATE 590-935	74 S 00
20	586-831	U12	74 S04
21	587-533	U32	74 LS04
22	587-751	U4	74 S08
23	587-158	U1 ALTERNATE: 589-937	74 S174
24	590-108	U42, U44	75188
25	587-856	U41, U43	75189
26	587-291	U39	NE555 TIMER
27	586-752	U16 ALTERNATE 586-690	7416
28	587-746	U8	74LS86
29	587-770	U20, U27	74 LS174
30	587-924	U2, U3	74 S 194
31	589-362	U37 ALTERNATE 589-825	74 LS 257
32	587-510	U9	74LS00
33	587-387	U31	74 LS 74
34	587-095	U5 ALTERNATE 003-111	74 S 74
35	587-279	U29	74 LS 138
36			
37			
38			
39			
40			
41	066-661	R18	120 OHM, ¼W, 5%
42	066-663	R5, R6.	220 " " "
43	066-834	R33	33 " " "
44	066-668	R4, R11, R19, R32, R41~R48, R51	4.7K " " "
45	066-814	R14	270 " " "
46	066-849	R35, R37	100K " " "
47	066-838	R10, R16, R20	330 " " "
48	066-830	R31, R39, R49	10K " " "
49	066-665	R1, R7, R9, R15, R22, R23, R28, R34	1K " " "
50	066-689	R25, R36	2.2K " " "
51	066-675	R27,	1.8K " " "
52	076-004	R2, R24,	180 " " "
53	066-820	R21	750 " " "
54	066-673	R38	1M " " "
55	066-821	R17, R29, R30	820 " " "
56	066-824	R8, R13	1.5K " " "
57	066-720	R40	3.3K " " "
58			
59	3512803-01	RP1, RP2, RP3 NTWK SIP 8 RES	22K OHM, ¼W, 5%
60			

REFERENCE DESIGNATION TABLE

ITEM	PART NO.	DESCRIPTION	REMARK
61	064-997	C22, C29, C37, C74, C90~C95	
62	" "	ALTERNATE 064-983 CERAMIC DISC	330PF, 50V, ±20%
63	064-939	C58 , ALTERNATE 030-977 CERAMIC DISC	0.001UF, 50V, 20%
64	064-444	C56, C61, CERAMIC MONO	1UF, 50V, 20%
65	064-116	C9, C47, C50, C96 " DISC	.01UF, 50V, "
66	064-937	C13, C15, C16, C54, C44, " "	22PF, 50V 5%
67	063-391	C45, C55, C60 LYTIC	100UF, 16V
68	064-462	C10, CERAMIC MONO	47PF, 100V
69	064-998	C67 CERAMIC DISC	2000PF, 50V, 20%
70	064-464	C14, C26	100PF, 100V
71	" "	ALTERNATE: 064-996 CERAMIC MONO	
72	164-004	C2~8, C20, C21, C23, C24, C27, C31~35	0.1UF, 25V
73	" "	C38~43, C46, C48, C49, C51~53, C57	" "
74	" "	C62, C63, C65, C66, C71, C75, C78~80, C82	" "
75	" "	C68 ALTERNATE: 064-456, 064-947	" "
76			
77			
78	579-156	Q2 XSTR ALTERNATE 579-161	2SC1730 (16)
79	014-889	Q3, Q5 XSTR	2N3643
80	014-772	Q1, Q4 XSTR	2N3644
81			
82	013-599	CR1~CR7 ALTERNATE 581-403, 581-105	DIODE IN4531
83			
84	080-060	B1 BATTERY	3V LITHIUM
85	3515498-01	FB1~FB16	FERRITE BEAD
86	582-203	XU33 ALTERNATE 582-387 IC SOCKET	40PIN
87			
88			
89	582-191	XU40 IC SOCKET	14PIN
90	582-202	XU10, XU17, XU23, XU34~XU36	28PIN
91	" "	IC SOCKET ALTERNATE 582-386	
92	3515139-01	Y3 CRYSTAL	3.6864 MHZ
93	3515382-01	Y2 "	19.6 MHZ
94	3515389-01	Y1 "	32.147 MHZ
95	135-533	J1 CONNECTOR	5PIN VIDEO
96	135-532	J3 "	4PIN POWER
97	140-900	J4, J5 "	25PIN RS232C
98	140-916	J2 "	4PIN KEYBD
99	3515301-01	L2	CHOKE ASSY
100	052-036	LC1	EMI FILTER

PART NO	COMPONENTS
3515400-01 3515400-03 3515400-04 3515400-06	INSTALL ALL COMPONENTS SHOWN IN REFERENCE DESIGNATION TABLE EXCEPT : C83~C89, C36, C25, C30, C98, C59, C69, C70 C72, C73, C76, C77, C81, , R26, J6, J7 Q6, CR8, CR9, L1
3515400-02 3515400-05	C83~C89, C98, C25, C30, C16, C59, C69, C70, C72 C73, C76, C77, C81, C36, C97. R26. J6, J7 Q6 L1, CR8, CR9, XU35.

PART "A"	PART "B"	PART "C"	REMARK
3515400-06	3515510-01	3515511-01	3515512-01 ALT: 3515513-01	
3515400-05	3515414-01	———	3515339-01 ALT: 3515345-01	
3515400-04	3515346-02	3515347-02	3515339-01 ALT: 3515345-01	
3515400-03	3515510-01	3515511-01	3515512-01 ALT: 3515513-01	
3515400-02	3515414-01	———	3515339-01 ALT: 3515345-01	
3515400-01	3515346-02	3515347-02	3515339-01 ALT: 3515345-01	

VERSION TABLE

———	W16 — W17	W17 — W18	———
———	W20 — W21	W19 — W20	———
COMP. SIDE	SOLDER SIDE	COMP. SIDE	SOLDER SIDE
CUT TRACE		ADD JUMPER (P/N 615-004)	

CUT TRACE AND JUMPER WIRE LIST (FOR-02,-05)

SIZE	CODE IDENT NO.	
D	09150	3515400
SCALE		SHEET 2 OF 6

3515400

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFTG	CHK	ENGRG
N		SEE SH. 1			

REFERENCE DESIGNATION		
COMPONENT	LAST USED	NOT USED
I.C	U47	
CAPACITOR	C99	C64, C17, C18
RESISTOR	R53	
RESISTOR PACK	RP3	
DIODE	CR7	
TRANSISTOR	Q6	
CRYSTAL	Y3	
JUMPER HOLE	W21	
INDUCTOR	L2	
BATTERY	B1	
JACK CONNECTOR	J7	
EMI FILTER	LC1	
FERRITE BEAD	FB16	

SIZE	CODE IDENT NO.	3515400
D	09150	
SCALE		SHEET 3 OF 6

UC-3004-08 (REV DEC 71)
PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
N		SEE SH.1			

SDϕ~SD7

U26 SCN2672 AC4N40

U27 LS174

U30 LS374

U23 U24 U17 U18

U22 3515348-01

U21 3515349-01

U25 Z80A CTC

U20 LS174

U11 LS32

U12 S04

U45 LS08

RP1 22K

RP2 22K

RP3 22K

J3

-C60 +100u

-C55 +100u

C56 1u

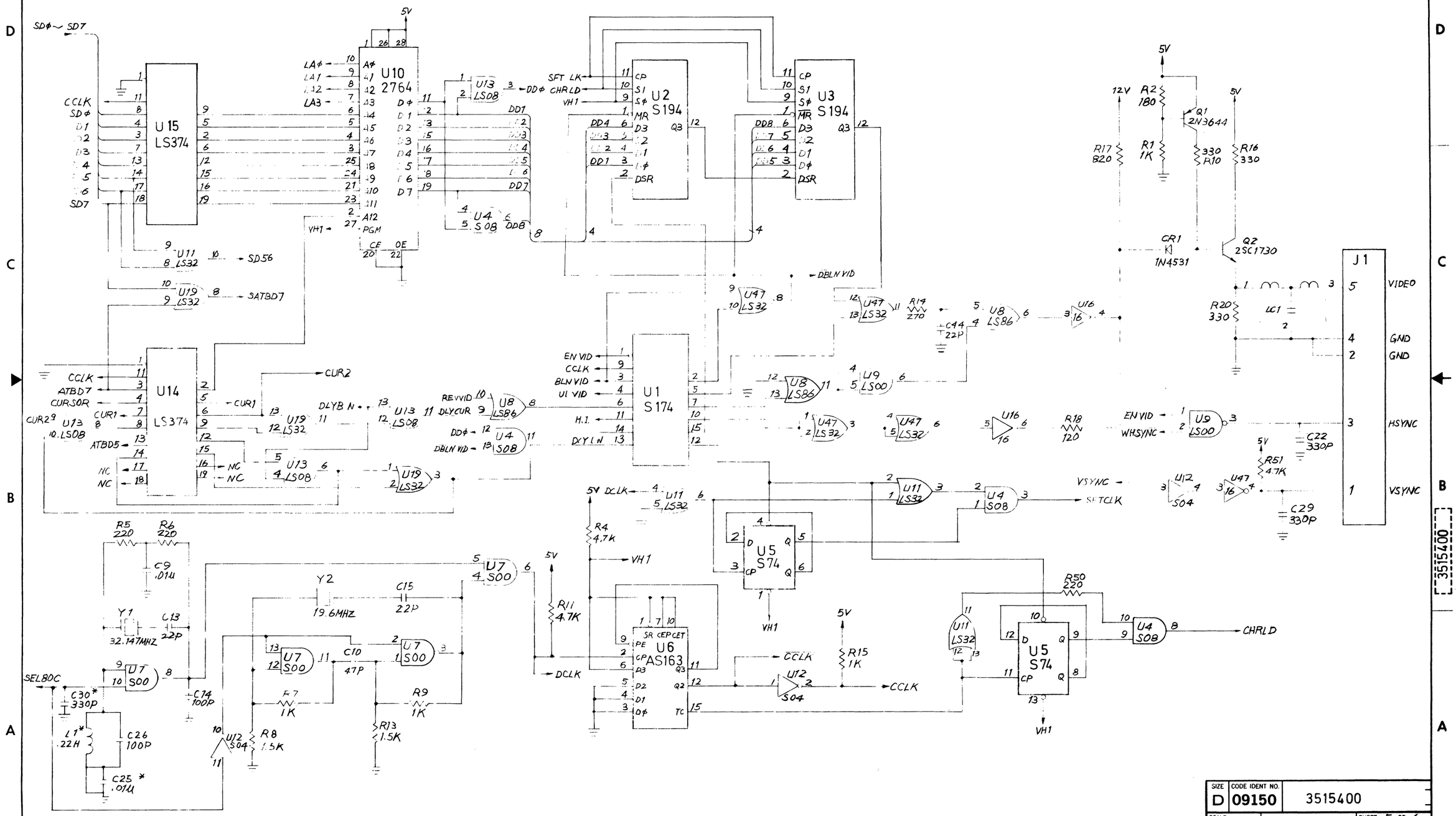
ATBDϕ~ATBD7

3515400

SIZE	CODE IDENT NO.	
D	09150	3515400
SCALE		SHEET 4 OF 6

UC-3984A-08 (REV DEC 77) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
P		SEE SH. 1			



SIZE	CODE IDENT NO.	
D	09150	3515400
SCALE		SHEET 5 OF 6

3515400

11-35-4A-38 REV DEC 73
PRINTED IN U.S.A.

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	APPD
P		SEE SH.1		

J4 J6 — DSR CTS RXD DCD — 6 5 3 8

J5 J7 — RTS DTR TXD — 4 20 2

5V FB4 R43 4.7K FB5 R45 4.7K FB6 R46 4.7K FB1 R47 4.7K FB14 R44 4.7K FB11 R48 4.7K FB16

U41 1489 U43 1489

C74 330P C92 330P C94 330P C95 330P C90 330P C93 330P C91 330P

U38 LS32

U32 LS04

R40 3.3K

XU40

5V 14, 12V 1

11	REC DATA (+)
10	REC DATA (−)
9	XMIT DATA (+)
8	20MA SOURCE
12	20MA SOURCE
5	REC CURRENT (+)
6	REC CURRENT (−)
3	XMIT CURRENT (−)
4	XMIT CURRENT (+)
13	XMIT DATA (−)
2	
7	GND

J4, J6

FB3

-12V 12V

U45 LS08

U38 LS32

U42 1488

FB8 C83* 330P

FB2 C87* 330P

FB7 C86* 330P

FB9 C85* 330P

1	CHASSIS GND
2	TXD
20	DTR
4	RTS

J5, J7

U44 1488

FB15 C88* 330P

FB13 C89* 330P

FB10 C84* 330P

FB12

C97* 1U C96 .01U R49 10K

5	CTS
3	RXD
6	DSR
8	DCD
7	GND
1	CHASSIS GND

U28 Z8470APS

5V VCC 9

CLK 4 — 13 RXCA
CLK 1 — 14 TXCA
CLK 2 — 27 RXTXCB
A 1 — 33 C/D
A 1 — 34 B/A
DART — 35 CE
IORQ — 36 IORQ
M1 — 6 M1
RD — 32 RD
φ — 20 CLK
RESET — 21 RESET
VH2 — 6 IEI
CTC IEI — 7 IEO
D 0 — 40 D0
D 1 — 39 D1
D 2 — 2 D2
D 3 — 38 D3
D 4 — 3 D4
D 5 — 37 D5
D 6 — 4 D6
D 7 — D7

RXDA 12, TXDA 15, DCDA 19, CTSA 18, RIA 11, DTRA 16, RTSA 17, RTSB 24, RIB 29, CTSB 23, DTRB 25, TXDB 26, RXDB 28, DCDB 22, W/RDYA 10 → N.C., W/RDYB 30 → N.C., INT 5 → INT, GND 31

U37 LS257

1A 2, 1B 3, 2A 5, 2B 6, 3A 11, 3B 10, 4A 14, 4B 13, SEL 1, E 15

1Y 4, 2Y 7, 3Y 9, 4Y 12

BIDIR

W13 W14 W15

U16 7416 — KB OUT

U12 S04 — KBIN

5V R19 4.7K CR2 IN4531

C37 330P

C45 + 100U

12V

L2

J2

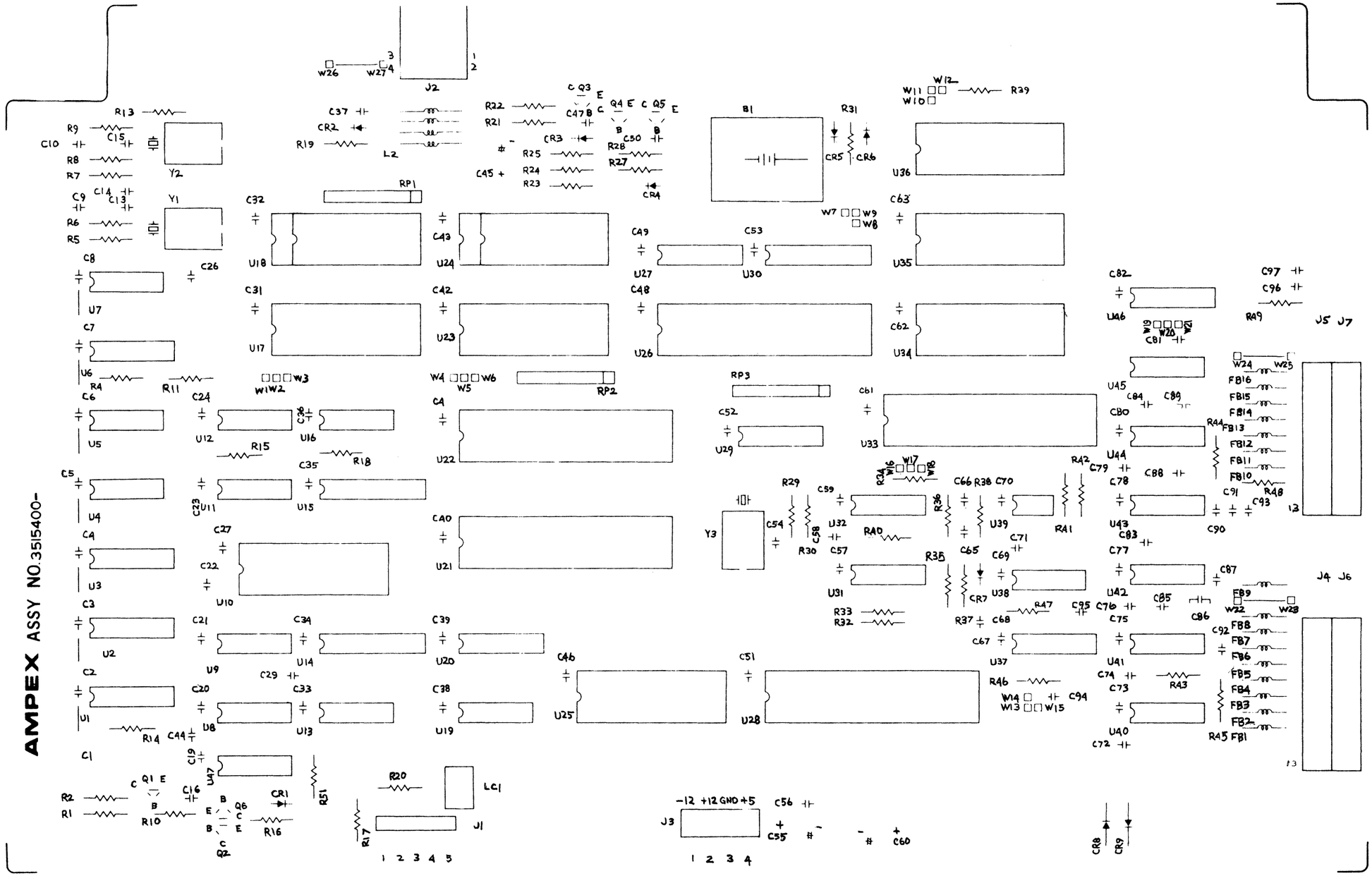
1	CHASSIS GND
3	DATA
4	GND
2	POWER

SIZE	CODE IDENT NO.	
D	09150	3515400

SCALE

SHEET 2 OF 5

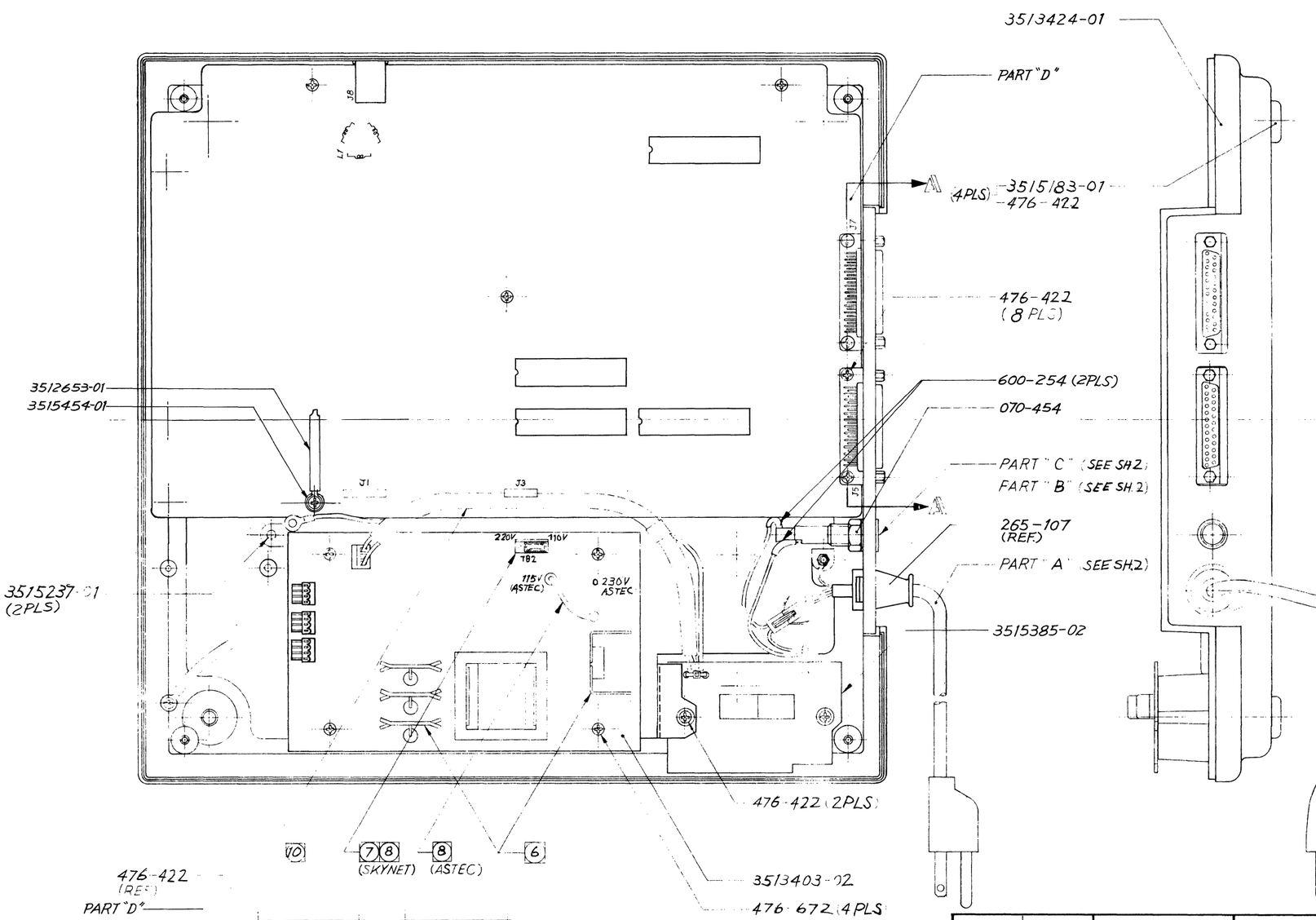
UC-3504A-08 (REV DEC 71)
PRINTED IN U.S.A.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECN 42068 ONT	11-5-84	
	B	ECN 42110	12-5-84	
	C	ECN 42115	1-22-85	
	D	ECN 42121	1-1-85	
	E	ECN 42135	2-21-85	
	F	ECN 42146	3-6-85	

3515-01 ORION II			AMPEX
NEXT ASSY			SILKSCREEN - CONTROL BD.
APPLICATION	DO NOT SCALE DRAWING	DRAWN R.C Chang	SIZE C | CODE IDENT NO 09150 | DRAWING NO 3515403
			SCALE 1/1 | SHEET 1 OF 1

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 0089 (CONT.)	SY 3-4-85		CN PER SH 1 5-9-85
B		ECN 42153			



(10) DRESS AC POWPER JUMPER WIRES UNDER CONTROL BOARD & AS CLOSE TO GROUND PLANE AS POSSIBLE.

(9) AC POWER CONNECTION:
FOR 115V – SEE SH 1 ZONE B-5 & SH.2 AC WIRING DIAGRAM.
FOR 220V - SEE SH.2 ZONE D-2 VIEW E-E & AC WIRING DIAGRAM.

(8) FOR 220V APPLICATION. SHIFT 3P CONNECTOR OF TB2 TO LEFT SIDE 1 POSITION AS SHOWN IN SH 1 ZONE B-6 WHEN USE SKYNET P/S PWBA; PULL AND INSERT SINGLE PIN CONNECTOR FROM 115V PIN POSITION TO 230V PIN POSITION AS SHOWN IN SH 1 ZONE B-6 WHEN USE "ASTEC" P/S PWBA.

(7) DRESS AC POWER JUMPER WIRES THREAD THRU WIRE LOOP OF TB2 CONNECTOR OF SKYNET P/S PWBA TO KEEP WIRES AWAY FROM HEAT SINKS.

(6) DRESS ALL WIRES AWAY FROM HEAT SINKS OF P/S PWBA.

(5) ADHERE GROUND PLANE INSULATOR TO GROUND PLANE PROPERLY AS SH 2 DOT LINES SHOWN WITH "3M" DOUBLE SIDE ADHESIVE TAPE "400 1/2" TO AVOID LIFT UP.

4 METRIC ENGRG & DRAFTING PRACTICES PER AMPEX STD MBI-3

3 MARK PART NO., ISSUE LTR. SERIAL NO. PER AMPEX SPEC 3124500 PARA 3.1.

2 ASSEMBLE PER AMPEX STD.

1 PART NO. TO BE PER VERSION TABLE. (SEE SH.2)

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST X

3515451	A219	
NEXT ASSY	USED ON	
	APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL — | 3 PL — | ANLR —
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5

MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY	Leon K. N.	3-4-85
CHK BY		3-4-85
DFTG APVD		3-4-85
ENGRG APVD		3-4-85
AUTH BY		3-4-85

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

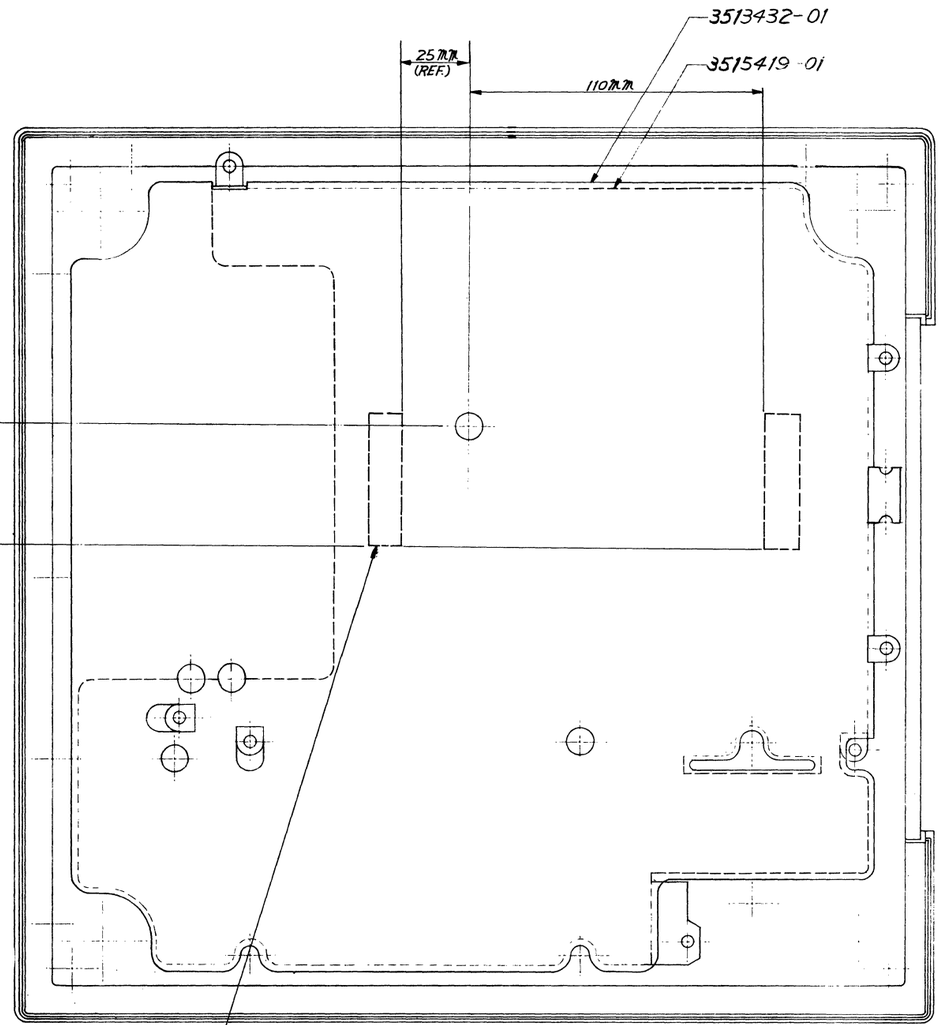
PEDESTAL ASSY

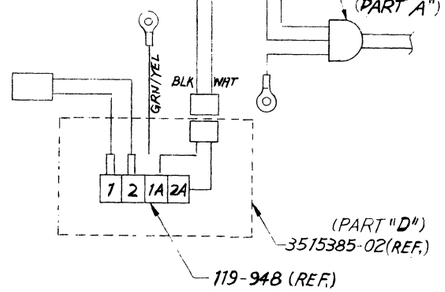
SIZE	CODE IDENT NO.	
D	09150	3515452

SCALE | DO NOT SCALE THIS PRINT | SHEET 1 OF 2

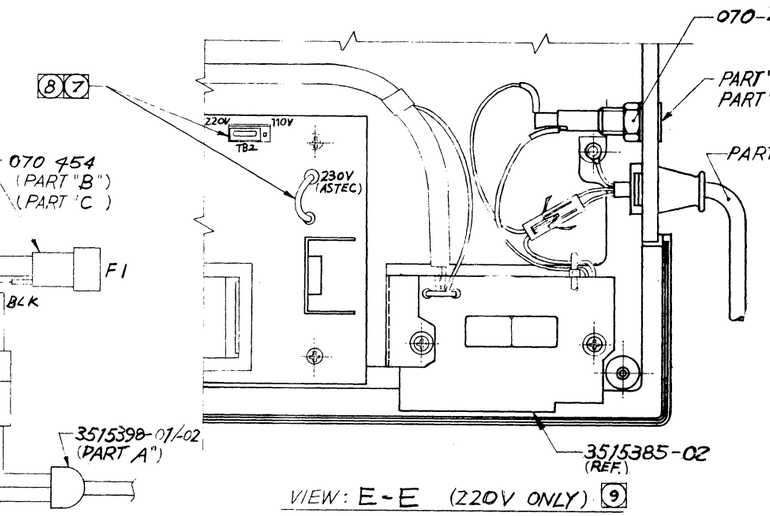
3515452

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGR'G
B		SEE SH.1			





AC / WIRING DIAGRAM 9



VIEW: E-E (220V ONLY) 9

PART NO.	PART "A" AC POWER CORD	PART "B" FUSE PART CAP	PART "C" FUSE	PART "D" PWBA-CONT. BOARD	REMARKS
3515452-02	3515398-02	070-413	070-467 ALTERNATE 070-471	3515400-03	220V
3515452-01	3515398-01	070-412	070-312	3515400-06	115V

VERSION TABLE

SIZE	CODE IDENT NO.	
D	09150	3515452
SCALE NONE		SHEET 2 OF 3

AMPEX CORPORATION, MEMORY PRODUCTS DIVISION 200 N. NASH STREET EL SEGUNDO, CALIFORNIA 90245