PRELIMINARY DRAFT

proposed

AMERICAN NATIONAL STANDARD

ENHANCED INTELLIGENT PERIPHERAL INTERFACE

DEVICE-SPECIFIC COMMAND SET FOR

MAGNETIC DISK DRIVES

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

Draft International Standards adopted by the technical committees are circulated to the member bodies for approval before their acceptance as International Standards by the ISO Council. They are approved in accordance with ISO procedures requiring at least 75 % approval by the member bodies voting.

Users should note that all International Standards undergo revision from time to time and that any reference made herein to any other International Standard implies its latest edition, unless otherwise stated.

Introduction

This part of ISO/IEC 9318 does not replace any existing standard, but it does complement other Intelligent Peripheral Interface (IPI) standards (see clause 2).

This part of ISO/IEC provides a additional capabilities not present in ISO/IEC 9318-2 and uses Physical Interface defined in ISO/IEC 9318-6. ISO/IEC 9318-2 uses Physical Interface defined in ISO/IEC 9318-1.

This part of ISO/IEC 9318 provides a definition of the physical interface portion of a series of standards called the Intelligent Peripheral Interface (IPI) ISO/IEC 9318, a high performance, general-purpose parallel peripheral interface. This part of ISO/IEC 9318, responds to an industry market need (expressed both by users and manufacturers) to limit the increasing costs in hosts associated with changes in peripherals.

Information processing systems — Intelligent Peripheral Interface

Enhanced Device Specific Command Set for Magnetic Disk Drives

1 Scope

This International Standard was prepared under the auspices of JTC/1 SC25 WG 4 (Joint Technical Committee One Subcommittee 25, Working Group 4), and describes the Enhanced Logical Level 2 (device level) Interface for disk drives. See Chapter 6 of ISO/IEC 9318-6:199x, the International Standard for Information Processing Systems — Intelligent Peripheral Interface — Enhanced Physical Level, for an explanation of the levels.

The physical, electrical, and configuration characteristics and the transmission protocol of this interface are in accordance with ISO/IEC 9318-6.

The purpose of this International Standard is to facilitate the development and utilization of a device level interface which permits the interconnection of disk slave peripherals to a controller.

This part of ISO/IEC does not replace any existing standard, but it does complement other Intelligent Peripheral Interface (IPI) standards (see Clause 2).

This part of ISO/IEC provides a definition of the enhanced device specific portion of a family of standards called the Intelligent Peripheral Interface (IPI), a high performance, general-purpose parallel peripheral interface. This International Standard responds to an industry market need (expressed both by users and manufacturers) to limit the increasing costs in hosts associated with changes in peripherals.

The intent of the IPI is to isolate the host (CPU), both hardware and software, from changes in peripherals by providing a "function generic" command set to allow the connection of multiple types of peripherals (disks and tapes). To smooth the transition from the current methods to the generic approach, the IPI supports device-specific command sets, such as this one, to aid in bridging the gap between the two approaches.

To accomplish this set of goals, the design of the IPI includes device-specific and device-generic command sets, both utilizing a common physical bus. The device-specific command set provides:

- Device-oriented control;
- Physical Addressing of Data;
- Timing Critical Operations;
- Lower Device Cost.

The device-generic command set provides a higher level of functionality and portability. It includes:

- Host/Device Independence;
- Logical Addressing of Data;
- Timing Independence;
- Command Queuing Capability.

A system is not restricted to the use of one level of command set or the other. It is possible that both levels of command sets may be utilized with a given system's architecture to balance such parameters as system performance, cost, and peripheral availability. It is also possible for the host to provide for migration from device-specific to device-generic levels while still retaining the same physical interface.

2 Normative references

The following standards contain provisions which, through reference in this text, constitutes provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO646:1983, Information processing - ISO 7 bit coded character set for information interchange.

ISO/IEC 9318-6:199X - *Intelligent Peripheral Interface*
Physical Level

ISO/IEC 9318-2:1990 - *Intelligent Interface - IPI-2*
- *ANSI X3.130-1986 Device Specific Command Set for Magnetic Drives*

3 Definitions and conventions

3.1 Definitions

For the purpose of this International Standard the following definitions apply:

3.1.1 Accepted: This word is to be used to indicate that the slave has successfully completed the operation defined by an Information Transfer Sequence without the occurrence of an exception.

3.1.2 Active/Not Active: This status word is to be used in the text when referring to the present status of a mode of operation. Examples - Reserve active, Selection active, Spindle Sync Offset active.

3.1.3 Allegiance: If common resources are dedicated to a port, then the port has a Allegiance and only this port shall be allowed to process bus controls and access common resources of Dual Port feature.

3.1.4 Assert/Negate: These conditioning words are to be used in the text when referring to the conditioning of the physical interface lines. Examples - assert ATTENTION IN, negate SLAVE IN.

3.1.5 Asynchronous Solicited Exception: This type of exception may occur after the completion of the Information Transfer Sequence and results in a Status Pending Interrupt.

3.1.6 Buffer Mode: When a slave is operating in Buffer Mode, it is transferring data to and from the media through a buffer.

3.1.7 Bus Control: The physical-level octet placed on BUS A by the master during the Bus Control Sequence. It is used to define the bus configuration and information type for the subsequent Information Transfer. The three Bus Control types are: Command Control, Response Control, and Data Control.

3.1.8 Bus Exchange: The Bus Control Sequence and the Ending Status Sequence. A Bus Exchange is used to frame an Information Transfer.

3.1.9 Busy: Busy indicates that the slave is unable to complete an Information Transfer Sequence. It may be reported at the Selection Sequence, at the Ending Status Sequence, at a Request Slave Interrupts Sequence, or at a Request Interrupts Sequence.

3.1.10 Byte: Byte means octet for this standard.

3.1.11 Command Control: A Bus Control that specifies that command information may be transferred from the master to the slave during the Information Transfer and identifies the command control type.

3.1.12 Data Control: A Bus Control that specifies that data information may be transferred during the Information Transfer, and identifies the data control type.

3.1.13 Default Value: This term is used at the parameter definitions to identify the value set during the Power-on Reset operation and Slave Reset operation.

3.1.14 Defect Map: A list of the defects recorded by the drive manufacturer on the slave.

3.1.15 Enable/Disable: These conditioning words are to be used in the text when referring to the conditioning/condition of the modes of operation.

3.1.16 End of Cylinder: The end boundary of the Auto Head Step Sector (see 6.13.8) located at the last head as managed by the slave during Buffer Mode. **If Buffer Across Cylinder Boundaries mode is set the End of Cylinder refers to the end boundary on the Last Buffer Operation Cylinder.**

3.1.17 Exception: An exception is an event that may require recovery action. Exception bits are used to inform the master that the event occurred. These bits are located in the Slave Status and the Status Response.

3.1.18 Format Specification: An ordered list of parameters that specify the organization of sectors and the number of sectors per track.

3.1.19 Idle: When all the control signals are inactive, the interface is in the IDLE state. Abnormal entries to this state shall occur whenever the master and slaves recognize an undefined state or state transition. The buses are released prior to entering the IDLE state except during the Request Interrupts and Master Reset sequences.

3.1.20 Information Transfer: The transfer of data that is framed by a Bus Exchange.

3.1.21 Information Transfer Sequence: The combination of the Bus Control Sequence, the Information Transfer, and the Ending Status Sequence.

3.1.22 Index: It is a reference point defined by the slave indicating beginning of a track and occurs once per revolution.

3.1.23 Level 2: A device-level-protocol interface in which the master may obtain and be aware of the specific characteristics of the device under its control.

3.1.24 Level 3: An intelligent interface oriented to the generic characteristics unique to the device.

3.1.25 Logical Interface: All protocols above the physical interface.

3.1.26 LSB: Least Significant bit.

3.1.27 Master Status: The status placed on BUS A by the master during the Ending Status Sequence after the Information Transfer.

3.1.28 MSB: Most Significant bit.

3.1.29 Operation: The events that occur in the slave as a result of an Information Transfer Sequence.

3.1.30 Out Of Context: If the master transfers bus control sequences to the slave without following proper order of sequences, then the slave regards this error as Out of Context (Bus Control or Function code).

3.1.31 Parameter: The information octets transferred after a Command Control or Response Control. Command parameters further define a command or contain specific information about a command, such as head number, cylinder number, etc. Response parameters contain information on the state of the slave, such as status, current head, current cylinder, etc.

3.1.32 Physical Interface: The mechanical, electrical, and bus protocol characteristics defined in ISO/IEC 9318-6.

3.1.33 Physical Sector: This term refers to the sectors identified by the disk drive, relative to index, with zero as the first.

3.1.34 Reject: This word is to be used to indicate that an exception occurred and the slave has not successfully completed the operation defined by the Information Transfer Sequence.

3.1.35 Response Control: A Bus Control that specifies that response information may be transferred from the slave to the master during the Information Transfer and identifies the response control type.

3.1.36 Reserved, set to zero: The transmitter is responsible for setting to zero. The receiver may check for zero.

3.1.37 RPS: This is an abbreviation for Rotational Position Sensing, which is a means for the slave to report to the master the rotational position of the head relative to the Target Sector.

3.1.38 RPS Pulse: The time, defined by the master in Load Position or Load Target Address commands, during which the Class 2 RPS Interrupt is set.

3.1.39 Set/Clear: These conditioning words are to be used in the text when referring to the conditioning of a bit, octet, name of a bit,or name of an octet that can be transferred across a data bus. In the case of a bit, set equals 1 and clear equals 0. In the case of an octet, set means a non-zero value and clear means an octet has a value of zero. Examples -set RPS Interrupt bit to 1, clear Class 1 , set Request Interrupts octet to 40h or 0100 0000b.

3.1.40 Slave Status: The status placed on the BUS B by the slave during the Ending Status Sequence after an Information Transfer.

3.1.41 Status Response: The status transferred by the slave during a Read Status Response.

3.1.42 Target Sector: The physical sector specified by the Target Address parameter.

3.2 Conventions

Certain terms used herein are proper names. These are printed in uppercase to avoid possible confusion with other uses of the same words; e.g., ATTENTION IN. Any lowercase uses of these words have the normal American-English meaning.

A number of conditions, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lowercase; e.g., In, Out, Selective Reset, Bi-directional, Bus Control, Operation Response. Any lowercase uses of these words have the normal American-English meaning.

Hexadecimal numbers are noted as follows:
12C4h where h indicates the previous character string is a Hexadecimal value.

Binary numbers shall be noted as follows:
0101 0101b where b indicates a binary value. Spaces may be included for better identification. In the case of a single binary value this convention may not be used. Examples - set to one or zero, clear to one or zero.

If "-" is used within parenthesis, it acts as numerical operator.
Example - (n-1) indicates n minus 1.

Undefined values shall be indicated by a lower case:
00x1b, 12x4h

ASCII string values shall be inside quotation marks with the dash equal to a space character:
"--IPI2--" is an 8 character string with 4 spaces.

Parameters designated as ISO/ASCII are left justified and padded with space (20h). Unsupported ASCII parameters are filled with nulls (00h).

A value F....Fh, unless specified, indicates the parameter is not supported.

4 General description

4.1 Application environment

The master (controller) may control one to eight slaves (disk drives) with a device level 2 command set and Level 1 physical sequences. The master and slave of a Level 2 environment are the slave and facility of a Level 3 environment. There are no facilities in the Level 2 environment.

4.2 Logical Interface Characteristics

4.2.1 Slave Control

The control of a slave is initiated by the master through the Bus Controls. The Bus Controls incorporate coding that identifies the particular command, response, or data type. The Command Control codes specify the command type being transferred to the slave, whereas the Response Control codes specify the response to be transferred from the slave. The Data Control codes specify the type of operation on fields or sectors.

4.2.2 Information Transfer

The interface uses the Double Octet mode to transfer 16-bit information. The Information Transfer during a Data Control is transferred in the Data Streaming mode; the Information Transfer during a Command Control and Response Control are transferred in the Interlocked mode.

Wider bus (32 bit, 64 bit, etc.) implementations listed in ISO/IEC 9318-6 are not supported.

4.2.3 Data Transfers

4.2.3.1 Non-Buffer Mode

The master writes to and reads from media by transferring Data Controls while staying synchronized with the rotation of the disk.. Data Controls define operations on fields or sectors and include read, write, verify, and skip operations.

4.2.3.2 Buffer Mode

During writes, the master may transfer data into the buffer at speeds exceeding the disk transfer rate and then may deselect the slave to select other slaves on the string. Meanwhile, the slave can empty the buffer at the slower disk transfer rate and then set the Buffer Available Interrupt when the buffer has space for more data.

During reads, the slave can fill its buffer when it reaches the target sector. The master may control the delay of the setting of the Buffer Available Interrupt, to allow the buffer to partially fill, or allow the setting of the Buffer Available Interrupt as soon as data is available.

Data Controls are limited in Buffer Mode.

4.2.4 The Format Control

The organization of sectors and the number of sectors per track is controlled by a Format Specification, which may be mutually derived by both the slave and the master.

4.3 Responsibility

4.3.1 Master

The master is responsible for the following functions:

- Bus Control Coding;
- Command Information;
- Data information management;
- Defect management;
- Error detection and/or correction - Retries, ECC, CRC;
- Sector organization (Format);
- Header information management.

4.3.2 Slave

The slave is responsible for the following functions:

- Bus Control Decoding;
- Response generation;
- Sector management;
- Gap management - Inter-field gaps;
- Header information verification during verify write;
- Information Transfer Clocking and length;
- Read Gate and Write Gate control.

Optionally:

- **Buffer Management**
- **ECC/CRC**
- **Retries**

4.3.3 Data Integrity

The master is responsible for data integrity. The physical interface provides byte-parallel parity, and the slave is required to detect and report parity errors. The master should provide ECC and/or CRC coverage for errors related to the slave storage media, and for errors on the physical interface that exceed the detection capability of the simple parity provided. The slave may optionally provide ECC and/or CRC coverage for errors related to the storage media, however, the master is still responsible for errors related to the physical interface.

5 Physical Interface considerations

The Physical Interface is defined in ISO/IEC 9318-6, with the interpretations and additions defined in the following clauses.

5.1 Information Transfer

5.1.1 Octet mode

All Information Transfers (Commands, Responses, and Data) are transferred in the double octet (16-bit) mode. Even-numbered octets are transferred on BUS A and odd-numbered octets are transferred on BUS B; i.e., the octet on BUS A is considered as being transferred before the octet on BUS B.

For Command and Response information transfers, bit 7 of an octet is the Most Significant Bit (MSB) and bit 0 is the Least Significant Bit (LSB). The most significant octets are transferred first in multioctet numeric parameters.

For data information, there is no definition of significance to the ordering of bits or octets. The order in which the octets are read is the same as that in which they are written.

Bit 7 on BUS A is the first recorded bit on the disk.

5.1.2 Transfer mode

Command/Response information is always transferred in the Interlocked mode. Data information is always transferred in the Data Streaming mode. The transfer modes cannot be changed.

The Request Transfer Settings octet response specifies the capabilities and settings of command/ response transfers in Double Octet and Interlocked modes. The Odd Octet transfer mode is not supported by the slave.

5.1.3 Termination of Transfers

The Information Transfer Sequence may be terminated by either the Master or the Slave, in accordance with ISO 9318-6.

5.1.3.1 Master Initiated Termination of Command Controls

When a Master initiated termination is detected by the Slave during a Command Control that does not incorporate "Octets to Follow" as the first command parameter, the Slave shall terminate the Information Transfer with Successful Information Transfer set at Slave Status. The values of whole or partial parameters not transferred shall not be affected. If the termination results in partial transfer of a parameter, Invalid Parameter will be set at the Status Response.

When a Master initiated termination is detected by the Slave during a Command Control that incorporates "Octets to Follow" as the first command parameter, the Slave shall set Successful Information Transfer at the Slave Status. The operation of the Slave on any transferred parameters is not defined.

5.1.3.2 Master Initiated Termination of Response Controls

When a Master initiated termination is detected by the Slave during a Response Control, the Slave shall terminate the Information Transfer with Successful Information Transfer set at the Slave Status.

5.1.3.3 Master Initiated Termination of Read or Verify Operation

When a Master initiated termination is detected by the Slave during a read or verify operation, the slave shall terminate the information transfer and immediately present the Slave Status with Successful Information Transfer set. Orientation is not lost. Buffer mode is not disabled by a Master Initiated Termination.

5.1.3.4 Master Initiated Termination of Write Operation

When a Master initiated termination is detected by the Slave during a write operation (**buffered or unbuffered**), the Slave shall stop requesting data from the Master. The Slave shall continue writing to the end of the field with a Slave-specific fill pattern, and then set Successful Information Transfer at the Slave Status, and orientation is not lost. If ECC/CRC is enabled at the Format Specification, the slave shall also write incorrect CRC or uncorrectable ECC. Buffer mode is not disabled by a Master Initiated Termination. **If the master terminates the header field on a Verify/write operations the results of the verify are unpredictable.**

5.1.3.5 Master Initiated Termination of Step Head data controls

When a Master initiated termination is detected by the Slave during a data control with the Step Head bit set, the Slave shall not advance the head counter but shall set the Successful Information Transfer in the Slave Status if the master has indicated Successful Information Transfer.

5.1.4 Data streaming

Data Streaming works differently for the Buffer Mode feature and the Non-Buffer Mode operation.

5.1.4.1 Data Streaming (Non-Buffer Mode)

Data streaming enables high transfer rates over long cables and is well suited to data transfers by a synchronous disk. This is accomplished by not interlocking the SYNC IN and SYNC OUT, which eliminates a round-trip transfer delay. Data streaming shall be used for data transfers as defined in ISO/IEC 9318-6, with the following interpretations:

- The SYNC IN pulses occur at the data rate of the disk and are asserted at the rate of one per double octet.
- The nominal duty cycle of the SYNC IN is 50 percent.
- Upon recognizing a SYNC IN, the master returns a SYNC OUT after a delay not exceeding one double octet time measured at the **master** connector.

During data output transfers, the slave shall prefetch data by initiating the SYNC IN pulses n octet times prior to the writing of the first data octet on the disk in order to account for transfer and master delays.

The value of n is dependent on master, slave, and transfer delays and the interface rate of the slave. The slave shall require at least an n-octet first in, first out (FIFO) buffer to account for delays less than maximum (n octet times). If data is not available in the slave when it must be written on the media, a data underrun condition exists, the transfer is terminated and the Successful Information Transfer bit in the Slave Status octet shall be set to zero and the Encoded Status shall be set to Underrun.

Slaves that support ECC/CRC and have that feature enabled shall complete the sector and write uncorrectable ECC/CRC if a data underrun condition occurs during a disk write.

5.1.4.2 Data Streaming (Buffer Mode)

Data streaming enables high transfer rates over long cables. This is accomplished by not interlocking the SYNC IN and SYNC OUT, which eliminates a round-trip transfer delay. Data streaming shall be used for data transfers as defined in ISO/IEC 9318-6, with the following interpretations:

- The SYNC IN pulses occur at the agreed to Interface Transfer Rate and are asserted at the rate of one per double octet.
- The nominal duty cycle of the SYNC IN is 50 percent.
- Upon recognizing a SYNC IN, the master returns a SYNC OUT or may optionally delay SYNC OUT if the master decides to throttle the Interface Transfer Rate.

If the master decides to throttle, it shall accept n octets of data and the value of n is defined as shown below for the different transfer rates:

- The value of n is 32 for transfer rate greater than 25 Mbyte/sec and less than 50 Mbyte/sec.
- The value of n is 16 for 25 Mbyte/sec transfer rate.
- The value of n is 16 for transfer rate greater than 10 Mbyte/sec and less than 25 Mbyte/sec.
- The value of n is 8 for transfer rate less than 10 Mbyte/sec.

If data is not available in the slave when it must be written on the media, a data underrun condition exists, the transfer is terminated and the Successful Information Transfer bit in the Slave Status octet shall be set to zero and the Encoded Status shall be set to Underrun.

Slaves that support ECC/CRC and have that feature enabled shall complete the sector and write uncorrectable ECC/CRC if a data underrun condition occurs during a disk write.

Interface Transfer Rates may be lower or higher than disk transfer rate. The master shall be capable of receiving at least n/2 SYNC IN pulses at the agreed to transfer rate. The master can throttle the transfer by slowing the SYNC OUT rate. If the master is throttling during the Write Buffer Mode or the Verify Buffer Mode and "Full Sector Transfer Attribute" bit is not set in the **Load** Buffer Control command, the Interface Transfer Rate can not be lower than the disk transfer rate **as this could cause an underrun condition. In Full Sector Transfer mode an underrun condition is not possible because the slave will not start transferring data to the media until a full sector is in the buffer.** The slave shall adjust the SYNC IN rate to ensure that no more than n/2 SYNC OUT pulses are outstanding at any point in the transfer. **The slave must receive a sync-out within 25 ms or slave initiates the Ending Status Sequence.**

5.2 Bus octets

The bus octets in double-octet mode defined in ISO/IEC 9318-6 shall be used as described, with the additions described in this clause. All valid state transitions shall be implemented by the slave.

5.2.1 Unsupported bus octets

The following bus octets are not supported:

- Facility Selection. The Slave does not acknowledge selection.
- Request Facility Interrupts. The Slave does not acknowledge request for facility interrupts.
- Bus Acknowledge. The Slave transfers zeroes on BUS B with correct parity.

5.2.2 Bus Control octet

The Bus Control octets define the direction and type of information transfer in bits 7-6 and the encoded Bus Controls in bits 5-0.

Bit	Label	Definition
7	Bus Control Type	0 = Operation Command or Operation Response 1 = Data
6	Direction	0 = Information Out 1 = Information In
5-0	Encoding	Encoded Bus Control Command and Response Controls. See 7.1 Data Controls. See 7.2.

5.2.3 Master Status octet

If the Master Status octet indicates an unsuccessful information transfer following a Read Status Response, the slave shall not clear the pending Status Response conditions.

Bit	Label	Definition
7	SIT	Successful Information Transfer Sequence
6	BPE	Bus Parity Error
5-0		0

5.2.4 Slave Status octet

The Slave Status provides information to the master on the results of the preceding Information Transfer Sequence. See 8.1 for further detail on the Slave Status octet.

Bit	Label	Definition
7	SIT	Successful Information Transfer
6	BPE	Bus Parity Error
5		0
4	TDO	Time-Dependent Operation
3-0	ES	Encoded Status

5.2.5 Request Interrupts octet

The slave shall respond to a Request Interrupts octet with a bit-significant Address Octet Response according to 5.2.6 provided it is operational (see 6.3).

The organization of the Request Interrupts octet is as follows:

Bit	Label	Definition
7		Zero
6	Report Busy Status	All slaves that are Busy shall set their bit-significant Address Octet Response on BUS B.
5	Report Ready Status	All slaves that are Ready shall set their bit-significant Address Octet Response on BUS B.
4	Master Power Fail Alert	The master is informing the slaves that it has detected that power is failing. The slaves shall acknowledge by placing their bit-significant Address Octet Response on BUS B after they have taken appropriate action to permit a graceful termination of activity.
3	Power On Status Request	All slaves that are operational shall set their bit-significant Address Octet Response on BUS B within 2 seconds after the master transfers Selective Reset Octet to the slave.
2	Status Pending Interrupt	Slaves with Class 3 Interrupt pending shall respond by setting their bit-significant Address Octet Response on BUS B.
1	RPS or Buffer Available Interrupt	Slaves with Class 2 Interrupt pending shall respond by setting their bit-significant Address Octet Response on BUS B.
0	Command Completion Interrupt	Slaves with Class 1 Interrupt pending shall respond by setting their bit-significant Address Octet Response on BUS B.

5.2.6 Address octet Response

The slave shall respond to a Request Interrupts octet or Selection octet with a bit-significant Address octet Response that has the following organization:

Bit	Label	Definition
7	Slave 7	Slave 7 bit significant response
6	Slave 6	Slave 6 bit significant response
5	Slave 5	Slave 5 bit significant response
4	Slave 4	Slave 4 bit significant response
3	Slave 3	Slave 3 bit significant response
2	Slave 2	Slave 2 bit significant response
1	Slave 1	Slave 1 bit significant response
0	Slave 0	Slave 0 bit significant response

5.2.7 Selective Reset octet

The receipt of this octet causes a Selective Reset of the type defined in bits 3-0. The following Reset Controls are defined:

Bit	Label	Definition
7	Indicates Selective Reset Octet	1
6-4	Slave address	Slave Address (bit 4 is the LSB)
3	Slave Release	The slave shall release its interface drivers in the same manner as it would upon recognition of the MAINT state. The drivers are to remain released on the port over which the Reset was transferred until recognition of another Reset with this bit cleared.
2	Slave Reset	The slave shall be reset to its power on condition (see 6.4.1).
1	Logical Reset	The Logical Interface for the port shall be reset (see 6.4.1).
0	Physical Reset	The Physical Interface for the port shall be reset (see 6.4.1).

5.2.8 Selection octet

The Priority Hold (PH) and Priority Select (PS) shall be supported by the slave.

The organization of the Selection octet is as follows:

Bit	Label	Definition
7		0
6-4	Slave Address	Slave Address (bit 4 is the LSB)
3-2		0
1	PH	Priority Hold
0	PS	Priority Select

The following Table shows allegiance of the slave to one port at a time based on existing condition at Port A and new condition at Port B.

Table 1 — Priority Hold and Priority Select

Existing condition at Port A		New condition at Port B			
	PH PS	PH PS 0 0	PH PS 0 1	PH PS 1 0	PH PS 1 1
Port A not selected and not reserved	0 0	B	B	B	B
	0 1	B	B	B	B
	1 0	A	A	A	B
	1 1	A	A	A	A
Port A Selected and not reserved	0 0	A	B	A	B
	0 1	A	B	A	B
	1 0	A	A	A	B
	1 1	A	A	A	A
Port A not selected and reserved	0 0	A	B	A	B
	0 1	A	B	A	B
	1 0	A	A	A	B
	1 1	A	A	A	A
Port A Selected and reserved	0 0	A	B	A	B
	0 1	A	B	A	B
	1 0	A	A	A	B
	1 1	A	A	A	A

5.2.8.1 Priority Hold

When bit 1 = 1 and a selection is established, the slave shall maintain an explicit allegiance after deselection to this port until:

a) A subsequent selection is established without the Priority Hold bit set in the Selection octet or;
b) A selection by an alternate port is established with both the Priority Hold and Priority Select bits set in the Selection octet or;
c) An appropriate Slave Reset operation is completed by the slave.

5.2.8.2 Priority Select

When bit 0 = 1, the specified slave shall release the current port to which it has allegiance, provided that an alternate port does not have a Priority Hold in effect, and shall respond to the requesting master.

A successful selection with the Priority Select bit set in the Selection octet shall cause an alternate port with a selection established and not in the SELECT state during a Selection sequence to terminate its selection. The termination may be orderly or abrupt depending on the slave's implementation.

5.2.8.3 Priority Hold and Priority Select

When both bit 1 = 1 and bit 0 = 1, the specified slave shall release the current port to which it has allegiance, regardless of its previous condition, provided that the alternate port had not previously established selection with both of the bits set.

The specified slave shall maintain allegiance to the selected port after deselection until:

a) A subsequent selection is established without the Priority Hold and Priority Select bits set or;
b) An appropriate Slave Reset is completed by the slave.

5.2.9 Request Transfer Settings octet

The slave shall respond with a Transfer Settings octet when it receives a Request Transfer Settings octet that has the following organization:

Bit	Label	Definition
7		1
6-4	Slave Address	Slave Address (Bit 4 is the LSB)
3-0		0

5.2.10 Slave Transfer Settings octet

The slave shall respond to a Request Transfer Settings octet from the master with a Transfer Settings octet that has the following organization:

Bit	Label	Definition
7		0 = Transfer Settings Octet
6		0/1 = Maintenance Mode 1/2
5		1 = Double Octet Mode
4		0 = Interlocked Transfer
3		0 = Slave is not capable of Data Streaming transfers
2		1 = Slave is capable of Interlocked transfers
1		1 = Slave is capable of transferring in Double Octet Mode
0		0 = Slave is not capable of transferring in Single Octet Mode

The transfer settings reported are those reflecting the capabilities and settings for the slave during Command/Responses Information Transfers.

5.2.11 Request Slave Interrupts octet

The slave shall respond with a Slave Interrupts octet when it receives a Request Slave Interrupts Octet. The organization of a Request Slave Interrupts octet shall be as follows:

Bit	Label	Definition
7		1
6-4		Slave address
3		1
2-0		0

5.2.12 Slave Interrupts octet

The slave shall respond with a Slave Interrupts Octet when it receives a Request Slave Interrupts Octet. The organization of the Slave Interrupts Octet shall be as follows:

Bit	Label	Definition
7	Reserved, set to zero	0
6	Busy Status	If Busy is set this indicates that the slave is unable to respond to the master's request; i.e., it is currently completing a Bus Control (previously issued from this port or the alternate port), or has allegiance to the alternate port, or an internal operation is being completed.
5	Ready Status	If Ready is set this indicates that the slave is operational and able to accept any supported Command or Data Bus Control code that is in context.
4	Priority Hold Status	This bit shall be set when the slave has a Priority Hold established at the Alternate Port.
3	Priority Select Status	This bit shall be set when a successful Priority Select has occurred during selection of the alternate port. This bit shall be cleared at the end of the Request Slave Interrupts sequence during which it was reported or with a Read Status Response Control.
2	Class 3 Interrupt	This bit shall be set when there is a status exception to be reported in the Status Response.
1	Class 2 Interrupt	This bit shall be set during the time on each disk revolution that the RPS Pulse is valid (the data heads are over the RPS Pulse defined by the Target Address) **in non-buffered mode or whenever the** Buffer Available Interrupt is **set in buffered mode** (see 6.5.2).
0	Class 1 Interrupt	This bit shall be set when a command, previously transferred with the Time-Dependent Operation bit set in the Slave Status octet, completes successfully. The Command Completion Interrupt is not set on a Load Position command that includes a valid Target Address parameter (see 6.5.1), unless the Target Address parameter is all ones.

5.3 ATTENTION IN signal

The ATTENTION IN signal shall be asserted by an unselected slave. See 6.5 for a description of interrupts.

The Load Slave Function command provides for enabling and disabling the individual interrupts from asserting ATTENTION IN, on a port basis. All ATTENTION IN assertions shall be enabled upon power-on Reset or Slave Reset.

6 Slave Implementations/Features

All the implementations and optional features are described in this section. All optional features are listed in the Read Configuration (41h). If the slave supports a feature, then feature shall be indicated in the Read Configuration (41h). All the bus controls and function codes related to the supported feature are mandatory.

6.1 Disk Format

There are two possible disk format types: Fixed Block Format, Single Zone and Fixed Block Format, Multi-Zone. Each format allows the slave to operate in one of the following two sector modes:

- Sector Mode 1 - Every sector is the same length and organization, which is fixed by the slave.
- Sector Mode 2 - Every sector is of the same length and organization, but the length and organization is programmable for both Format types. In the Multi-Zone Format type, data size stays the same but sector length changes because gap size changes from zone to zone.

6.1.1 Fixed Block Format, Single Zone

This Format type allows slave to be formatted with a variable number of identical sectors per track. The length and organization of a fixed block sector shall be determined by the Fixed Block Format Specification.

6.1.2 Fixed Block Format, Multi-Zone

This Format type allows Zoned Disk slave to be formatted with a Fixed Block Format Specification to a fixed number of zones per surface. The length and organization of a zoned disk sector shall be determined by the disk Format Specification. Each zone shall have a defined Fixed Block Format Specification.

6.1.3 Format Control

The slave shall be responsible for format control. It shall be capable of performing the following functions in meeting the requirements of the appropriate Format Specification:

- Determining the start of each sector on the track
- Determining the start of each field within a sector
- Counting the number of octets in each field of a sector
- Activating Read Gate and Write Gate in accordance with the current Data Control and the Format Specification
- Acquiring PLO, bit, and octet synchronization on read operations
- Writing of PLO, bit, and octet synchronization patterns
- Supporting the data interleave factor

6.2 Format Specification

The Format Specification is an ordered list of parameters that define for the slave how the tracks and sectors of the disk are to be organized. It is transferred to the slave by the Load Format Specification command control, and the master may retrieve it by the Read Format Specification response control. Both the master and the slave may establish the parameters during the initialization of the Format Specification.

6.2.1 Format Specification Initialization

The Format Specification is not initialized when the slave is powered on, unless the slave has implemented the option to save the Last Format Specification. The master may also save a number of Format Specifications on the disk media (See Annex C).

A Load Format Specification command control clears the Initialized bit unless the Save Last Format Specification option has been implemented. If no exception occurs, the hardware is initialized by the slave to the parameters transferred with the Load Format Specification command control, and then the Initialized bit is set. If the Save Last Format Specification option is implemented and the transferred Format Specification is not valid, the Initialized bit remains set in the existing Format Specification. **If the Initialized bit is not set drive shall not accept any data controls because without an Initialized Format Specification, the Data Controls are "Out of Context".**

The master may confirm the values of the Format Specification with the Read Format Specification response control.

If the Initialized bit is cleared in the Read Format Specification response, the parameter values transferred may be the Format Specification previously accepted by the slave.

The slave shall set the Class 3 interrupt and the Alternate Port Format Specification Change bit at the alternate port any time the Format Specification is changed. If the slave changes the Format Specification on its own it shall set Class 3 interrupts and Alternate Port Format Changed bits for both ports.

The master has two options for the transfer of parameters with the Load Format Specification command control.

6.2.1.1 Option 1 - Master transfers all parameter values

In this option the master shall transfer the Load Format Specification command with all parameters defined. The Slave has the responsibility to confirm the parameter values of the Format Specification for initialization at the slave hardware. The master shall transfer the value of the Initialized bit equal to 1 to indicate this option and, if no exception occurs, the slave shall initialize the hardware and set the Initialized bit at the Format Specification.

It is recommended that the master compare the values of the Format Specification to its intended requirements using the Read Format Specification response control.

6.2.1.2 Option 2 - Master requests the slave to calculate one or more parameter values

The master has the option to set a parameter, transferred with the Load Format Specification command, to FF..FFh to indicate a request for the slave to calculate the parameter value. If the slave does not support the calculation of the parameter, an exception shall be transferred by the slave. The master shall transfer the value of the Initialized bit equal to 0 to indicate this option and, if no exception occurs, the slave shall initialize the hardware and set the Initialized bit in the Format Specification.

To use this option the following are required by the master:

(1) The master shall set the number of physical octets per sector to a value of FF..FFh.

(2) The master shall set the following parameters to a value other than FF..FFh and within the limits of the slave:
- Number of octets following
- Interleave/Format code
- Flag (Note - Initialized bit shall be cleared)
- Number of beginning header octets to be skipped during header verify
- Number of fields per sector
- Number of octets per field
- Master Status Time

(3) The master shall **perform** one or more of the following:
- **Set bit 1** of the **Flag octet**
- **Set the number** of sectors per Head Address **to FF..FFh**

The slave shall calculate the values set to FF..FFh and, if no exception occurs, the slave shall initialize the hardware and set the Initialized bit at the Format Specification upon completion of the calculations. It is recommended that the master compare the values of the Format Specification to its intended requirements using the Read Format Specification response control.

6.2.2 Manufacturer's Format Specification

The slave shall have a built-in Manufacturer's Format Specification, which is used primarily to read the Defect Map. It shall be invoked by the Load Format Specification command control with bit 6 of the Flag Octet set, and shall remain in effect until another Load Format Specification command control is accepted by the slave. It may be read by a Read Format Specification response control.

The format shall provide for a header and one data field not to exceed 1024 octets in length. The header contents, the CRC, and the ECC are not specified. The format shall be organized to allow for either sector type or field type data controls. There shall be no sector interleaving.

The master shall be capable of recovering the data from data fields formatted with this specification, without the use of the header contents. Sectors shall be read in their physical order starting with sector zero.

6.2.3 Fixed Block Format Specification

The Fixed Block Format Specification allows for sectors of any number of fields, as supported by the slave, and all sectors shall have the same organization. The master shall transfer these parameters with the Load Format Specification command control during the Format Initialization operation with the slave. The slave shall transfer these parameters with the Read Format Specification response control for the master to confirm.

The Fixed Block Format Specification has the following format:

Octet	Bit	Description
0h-1h		Number of octets following: equals n - 1 (Note 1)
2h		Data Interleave Factor and Format Type
	7-3	Data Interleave Factor
	2-0	Format Type Code: 011b = Fixed Block Format, Multi-Zone 001b = Fixed Block Format, Single Zone
3h		Flag Octet
	7	Initialized (Format Specification Initialization complete)
	6	Initialize the Manufacturer's Default Format Specification
	5	Head Switch at end of a sector
	4	Read after Write at end of sector
	3-2	Encoded ECC/CRC Operation Bit 3 Bit 2 Operation 0 0 No ECC/CRC 0 1 Use Slave ECC in Data Fields and Field 0 1 0 **Invalid** 1 1 Use Slave ECC in Data Fields and Use Slave CRC in Field 0
	1	**Evenly distribute unused bytes on track**
	0	Condition for the master to use Field Data Controls
4h-5h		Number of beginning header octets to be skipped during header verify
6h-7h		Master Status Time (50 ns increments)
8h-9h		Number of fields per sector (m_{max}) (Note 2)
		FIELD DESCRIPTOR (Note 3, Note 4)
0h:3h		Number of octets per field, field (m)
4h:5h		Master Turnaround Delay, field (m) (50 ns increments)
0h-1h		Number of Zones (Note 5)
		ZONE DESCRIPTOR (Note 3, Note 6)
0h-1h		Zone Number z
2h-3h		Number of sectors per Head Address Zone z
4h-7h		Number of physical octets per sector Zone z

NOTES
1 n is the octet number of last octet transferred.
2 Number of Fields per sector is equal to the last field number plus 1. Fields are numbered starting from zero.
3 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.
4 Parameters in the FIELD DESCRIPTOR are repeated as specified by the value in the Number of Fields per Sector.
5 Number of Zones is equal to the last zone number plus 1. Zones are numbered starting from zero.
6 Parameters in the ZONE DESCRIPTOR are repeated as specified by the value in Number of Zones parameter.

6.2.3.1 Number of octets following (0h-1h)

This parameter contains the number of octets to follow. It does not include itself in the octet count. This value is used by the slave to control the length of the transfer. See Termination of Transfers (5.1.3).

6.2.3.2 Data Interleave Factor and Format Type (2h)

This parameter contains the Data Interleave Factor and Format Type code.

6.2.3.2.1 Data Interleave Factor (Bits 7-3)

The Data Interleave Factor specifies how the data, transferred on the interface, is organized at each head of a Parallel Head slave. For non-Parallel head slaves the bits 7-3 shall be set to zero.

The Data Interleave factor has bit granularity (1-32 bits). The Data Interleave Factor +1, determines the number of bits organized at the first ordered head of each Head Address. The next, same number of bits, are organized at the next ordered head, and so on for more heads in parallel.

6.2.3.2.2 Format Type (Bits 2-0)

The Format Type code shall be equal to 001b for the Fixed Block Format, Single Zone and 011b for Fixed Block Format, Multi-Zone.

6.2.3.3 Flag octet (3h)

This parameter contains the flag information.

6.2.3.3.1 Bit 7 - Initialized (Bit 7)

The initialized bit in the Read Format Specification response control is controlled by the slave and shall be set after the slave has initialized its hardware to the parameters transferred in the Load Format Specification command control.

The master should set the initialized bit in the Load Format Specification command control, if the master transfers all values completely defined, as the slave has the final reporting of the Initialized bit in the Read Format Specification response control.

6.2.3.3.2 Bit 6 - Manufacturer's Format Specification (Bit 6)

The Manufacturer's Format Specification bit shall be set by the master in the Load Format Specification command control to command the slave to initialize the Manufacturer's Format Specification. If the Manufacturer's Format bit is set in the Load Format Specification command, the slave shall ignore the remaining bits of the Flag Octet and all other parameters of this command. The Manufacturer's Format bit shall be set by the slave at Read Format Specification response to indicate to the master the Manufacturer's Format Specification.

6.2.3.3.3 Head Switch at end of a sector (Bit 5)

The master shall set bit 5 to inform the slave that Head Switch at the end of sector is desired. When this bit is set, if necessary, the slave shall add to the MTD (field m_{max-1}) to cover for it's own internal overhead to support this feature. If this bit is set, the master shall provide a valid non-zero Master Status Time parameter in this Format Specification.

6.2.3.3.4 Read after Write at end of sector (Bit 4)

The master shall set bit 4 to inform the slave that Read after write at the end of sector is desired. When this bit is set, if necessary, the slave shall add to the MTD (field m_{max-1}) to cover for it's own internal overhead to support this feature.

6.2.3.3.5 Encoded ECC/CRC Operation (Bits 3-2)

Bit 3	Bit 2	Operation
0	0	No ECC/CRC
0	1	Use Slave ECC in Data Fields and Field 0
1	0	Invalid
1	1	Use Slave ECC in Data Fields and Use Slave CRC in Field 0

The slave shall add to the post gaps the number of bytes specified in the Read Disk Specifications for the support of ECC or CRC.

6.2.3.3.6 Evenly distribute unused bytes on track (Bit 1)

The master shall set bit 1 to inform the slave to distribute any unused bytes on the track into the gaps as evenly as possible. When bit 1 is not set the slave shall place any unused bytes into an unusable stub sector located at the end of the track.

6.2.3.3.7 Condition for the master to use field Data Controls (Bit 0)

Bit 0, shall be set by the master in the Load Format Specification command control to inform the slave that Field Data Controls are to be used. The slave **shall provide sufficient time in the pre- and post- gaps to accommodate a bus control sequence.**

If bit 0 is clear, the slave shall reject a Field Data Control as Out of Context.

6.2.3.4 Number of beginning octets to be skipped during header verify (4h-5h)

This parameter specifies the number of octets, starting from the beginning of the header, to be skipped in the transfer of data and the slave's verification of the header during the completion of a Verify Header Data Control. The octets skipped are limited to even sizes. The skipped octets are not transferred by the master.

6.2.3.5 Master Status Turnaround (50 ns Increments)(6h-7h)

This parameter is the master required protocol overhead to transfer an ending status to the slave at the end of Sector. This parameter shall also provide for two round trip cable delays that are associated with the Ending Status Sequence. The slave utilizes this parameter in order to calculate its own internal Head Switch overhead. The master shall set this parameter to zero if the Flag Octet bit 5 is cleared in this Format Specification.

6.2.3.6 Number of fields per sector (m_{max}) (8h-9h)

This double-octet parameter shall be set to a value by the master to specify the number of fields per sector. Zero is not a valid value.

6.2.3.7 Number of octets per field

This parameter specifies the number of physical octets per field and it is limited to even sizes. Zero is not a valid value. Master-managed ECC and CRC, if used by the master, shall be included by the master in the value. This parameter is repeated for each field.

6.2.3.8 Master Turnaround Delay (50 ns increments)

This parameter specifies the Master Turnaround Delay and should be set by the master. The Master Turnaround Delay is the time, measured in 50 ns increments, required by the master between fields to handle the **transfer of the** Data Control intended to operate on the next field. It is the master's responsibility to account for the following in this value as required for the master's use of the slave:

- Transmission Delays
- Controller Internal Overhead/Delays
- Data Control Sequence Initiation
- Optionally:
  - Head Switch Delay
  - Write-to-Read Recovery Delay
  - **Master Status Turnaround**

The value transferred in the Read Format Specification is the set value of the Master Turnaround delay. The total gap used by the slave between fields is the slave's post-gap and pre-gap (see Figure 1). The slave gaps may include the following:

- Read Propagation Delay
- Transfer Termination Time
- Slave Status Turnaround Time
- Data Control Decoding
- **Master Turnaround Delay**

If a Data Control operation is not required by the master on the next field, the Master Turnaround Delay value may be set to zero. The Master Turnaround Delay parameter is repeated for each field. **FF..FFh is not a valid value for Master Turnaround Delay.**

6.2.3.9 Number of Sectors per Head Address

This parameter should be set to the number of Sectors per Head Address. This parameter may be set to FFFFh (see 6.2.1.2). Zero is not a valid value.

6.2.3.10 Number of physical octets per sector

The number of physical octets per sector shall include the octets used for pre-gap and post-gap. See Figure 1. This parameter should be set to FFFF FFFFh (see 6.2.1.2). This parameter may be set to the number of physical octets per sector. Zero is not a valid value.

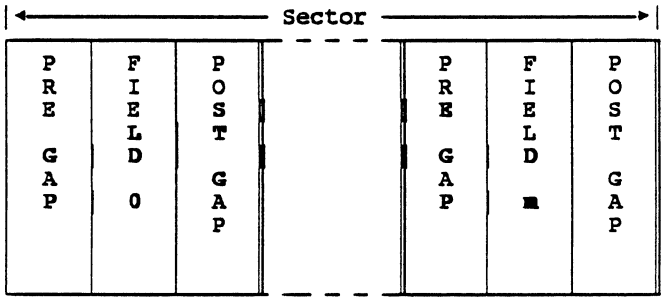


Figure 1 — Sector Format (Non-Buffer Mode)

6.3 Slave conditions

The manner in which a slave responds to sequences and commands is determined by it's condition. The condition of a slave is affected by essential as well as operational characteristics. The conditions are classified as follows:

Not Operational: The slave does not respond on the Physical Interface. Bus Sequences are not operational.

Operational: If not physical busy, the slave recognizes Bus Sequences and shall accept any supported Bus Control that is in context. It recognizes Selection, Deselection, Bus Control, and Ending Status Sequences. The slave shall respond to Master Reset, Selective Reset, Request Interrupts, Request Slave Interrupts, and Request Transfer Sequences. All Data Bus Controls and the following Command/Response Bus Controls that access to the Head/Disk Assembly (HDA) are rejected as Bus Control Context:

- Load Cylinder Address
- Load Head Address
- Load Target
- Load Position
- Load End of Write
- Read Position
- Read Current Sector Address

Ready: The slave is operational and able to accept any supported bus control that is in context. Data controls are accepted provided Initialized bit is set at the Format specification Flag Octet.

Status Pending: The Status Pending Interrupt (Class 3) has been set, and the master shall read the Status response. The Read Status Response Bus Control must complete successfully before slave accepts any other Bus Control.

Busy: The slave is not able to accept Bus Controls because it is currently completing a Bus Control issued from either port, has allegiance to the Alternate port, or it is completing an internal operation.

The slave provides information on it's condition through the Request Interrupts Sequence. A slave that is busy shall either not respond with it's bit significant Address Response during a selection Sequence or shall set busy at the Slave Status Octet.

Slave Conditions are listed in the Following table and they are determined by response to the Request Interrupt Sequence..

Table 2 — Slave Conditions

Request Interrupt Octet			
Power	Ready	Busy	Condition
0	0	0	Not operational (Note 1)
0	x	1	Illegal Condition
0	1	x	Illegal Condition
1	0	0	The slave is Operational but Not Ready.
1	0	1	The slave is operational and Busy (Note 2)
1	1	0	Ready
1	1	1	Ready and Busy

NOTES
1 This condition may occur up to 2 seconds after a Slave Reset.
2 This condition may occur as a result of a Slave Reset.

6.4 Reset

6.4.1 Interface Reset

An Interface Reset, in the form of a Master Reset or a Selective Reset transferred over the Physical Interface, may be presented by the master at any time regardless of the condition of the slave. It shall affect the port over which it is transferred if the slave is operational and does not have allegiance to the alternate port. (See Selective Reset 5.2.7).

The Master Reset and the Physical Reset resets the Physical Interface of the port over which they are transferred and do not affect logical conditions. (e.g., Reservation, pending interrupts, Format Specification, or RPS parameters).

The Logical Reset clears the interrupts, disables the Buffer Mode and resets the physical interface to IDLE mode.

The Slave Reset resets the entire slave to its power-on condition and all parameters are set to the default values. The Slave Reset does not affect the condition of the spindle motor. Following the Slave Reset, the slave enters the Operational condition, except when precluded from doing so by conditions that force it into a Not Operational condition. The Slave Reset does not affect the conditions set by the Local Control features.

6.4.2 Unsolicited Reset

When a slave Unsolicited Reset occurs, an Unsolicited Exception Status bit is set and the Status Pending Interrupt is set.

6.5 Interrupts

The slave shall support the three interrupt classes defined in ISO/IEC 9318-6. The setting of interrupt bits upon transfer of a Request Interrupts or Request Slave Interrupts sequence shall not be disabled by the Load Slave Functions. The reporting may be controlled with the Load Port Control command.

6.5.1 Class 1 Command Completion Interrupt

This interrupt is set when a command completes successfully and the Time-Dependent Operation bit of the Slave Status in the information transfer sequence was set. The Command Completion Interrupt is not set if an RPS Target Address, other than all ones, is accepted **and the RPS Pulse Width is not equal to 0, if the command was a Load Cylinder, Load Head, Load Target, or Load Position.** The Command Completion Interrupt is cleared by any of the following:

- Slave accepts any Bus Control.
- Slave is reset with a Logical Reset from this port.
- Slave is reset with a Slave Reset from either port.

If a status exception occurs for the TDO operation, the slave shall present only the Class 3 Interrupt to the master after the command completion.

6.5.2 Class 2 Interrupt

The Class 2 Interrupt has a different meaning for the slave when in the Buffer Mode.

6.5.2.1 Class 2 RPS Interrupt (Non-Buffer Mode)

This interrupt is set on each disk revolution during the time specified by the Load Position command control or Load Target Address command control. If an RPS Interrupt is set, it shall be cleared by any of the following:

- Setting all ones as the Target Address parameter;
- Slave accepts a Data Control;
- Slave accepts a Load Format Specification;
- Logical Reset from this port if there is no allegiance at the alternate port;
- Slave Reset from either port.

If the slave completes the operation during the rotational time of the defined RPS pulse, the RPS interrupt is set for the remaining time of the defined RPS Pulse.

6.5.2.2 Class 2 Buffer Available Interrupt (Buffer Mode)

When in Buffer Mode the Class 2 Interrupt is defined as the Buffer Available Interrupt.

6.5.2.2.1 Read Buffer Mode

The Buffer Available Interrupt is set when the number of sectors contained in the buffer is equal to or greater than the number of sectors (other than zero) specified in the Buffer Available Interrupt Delay Parameter in the position commands. The Buffer Available Interrupt is cleared when the number of sectors contained in the buffer is less than the number of sectors (other than zero) specified in the Buffer Available Interrupt Delay Parameter.

If the value specified in the Buffer Available Delay Parameter is zero, the Buffer Available Interrupt is set when at least two octets of data is in the buffer and it is cleared when less than two octets of data is in the buffer. The maximum size of Buffer Available Interrupt is related to buffer size in sectors. If the master sets the Buffer Available Interrupt greater than the buffer size, the slave shall reject with the invalid parameter in the Status Response.

6.5.2.2.2 Write Buffer Mode and Verify Buffer Mode

The Buffer Available Interrupt is set when there is enough space in the buffer for the number of sectors (other than zero) specified in the Buffer Available Interrupt Delay **Parameter in** the position commands. The Buffer Available Interrupt is cleared when there is not enough space in the buffer for the number of sectors (other than zero) specified in the Buffer Available Interrupt Delay Parameter.

If the value specified in the Buffer Available Interrupt Delay Parameter is zero, the Buffer Available Interrupt is set when space for at least two octets of data in the buffer is available and it is cleared as soon as space in the buffer is less than two octets of data.

6.5.2.2.3 Clearing Buffer Available Interrupt

The Buffer Available Interrupt shall be cleared by any of the following:

- Logical Reset from this port if there is no Allegiance at alternate port.
- Slave Reset from either port.

6.5.3 Class 3 Status Pending Interrupt

There are two types of Class 3 Interrupt:

1. Asynchronous Unsolicited Class 3 Interrupt (e.g., Fault Exception at IDLE after TDO Slave Status.
2. Asynchronous Solicited Class 3 Interrupt (e.g., Invalid parameter after TDO Slave Status)

Class 3 Status Pending Interrupt is cleared by any of the following:

- Read Status Response with a Successful Information Transfer bit set in the Master Status;
- Logical Reset from this port if no Allegiance at the Alternate port;
- Slave Reset from either port.

If a status exception occurs for a TDO operation, the slave shall present only the Class 3 Interrupt to the master.

It is possible for a Class 1 and a Class 3 interrupt to occur concurrently. This occurs when a status is generated as the result of the normal completion of a command. For instance, Not-Ready to Ready status is generated as the result of a Spin-Up command. A Class 1 interrupt is generated for the completion of the command and a Class 3 interrupt is generated indicating status is available in the status block.

6.6 Head Address Control

The slave's head addressing is controlled by the Load Head Address and Load Position bus controls.

The head address shall be incremented at the end of an accepted information transfer sequence, if bit 4 of a Fixed Block Data Control is set. An accepted information transfer sequence requires that the Successful Information Transfer bit be set in both the Master Status and the Slave Status. The head address shall advance immediately upon receiving the Master Status octet. The head address register may be advanced unconditionally by the Step Head Data Control. If there is an active Target Modifier, the Data Control may have the TDO bit set in the Slave Status.

The address of the first head shall be zero and the address of the last head shall be one less than the number of heads specified in the Read Configuration response. The counter increments to zero after the last head address.

The head address is incremented automatically by the slave while in the Buffer Mode (see 6.13.7).

6.7 Rotational Position Sensing (RPS)

The RPS option provides the ability for the slave to assert (Class 2) RPS Interrupts.

6.7.1 Target Address

See 7.1.6.2

6.7.2 RPS Interrupt

See 6.5.2.1

6.7.3 RPS Parameters

The format of the Load Target Address command is as follows:

Octet (Hex)	Parameters
0 - 1	Target Address
2 - 3	Extension
4 - 7	Pulse Width
8 - B	Skew

RPS parameters, not transferred, shall remain at the previous value.

The Load Target Address Command causes the slave to initiate the following operations:

(1) The slave shall set the physical sector to be used for the "at Target Sector Address type" Data Controls equal to the sector specified in the Target Address parameter. The other RPS parameters do not affect the "at Target" physical sector.

The RPS Interrupt (Class 2) is cleared if the Target Address is set to all ones. Target Address value is set to all ones at power on, after the receipt of a Slave Reset or after the acceptance of a Load Format Specification.

Following this command the RPS Interrupt is set during the time the heads are over the RPS Pulse. This RPS Pulse shall be located at the Target Address sector unless modified by the RPS parameters.

(2) The slave shall set the pulse width to the RPS Pulse as specified with the Extension value and the Pulse Width to the number of octets per sector defined by one of the following:

1. Manufacturer's Format Specification, or
2. The last saved Format Specification if implemented, or
3. New Format Specification if accepted by the slave.

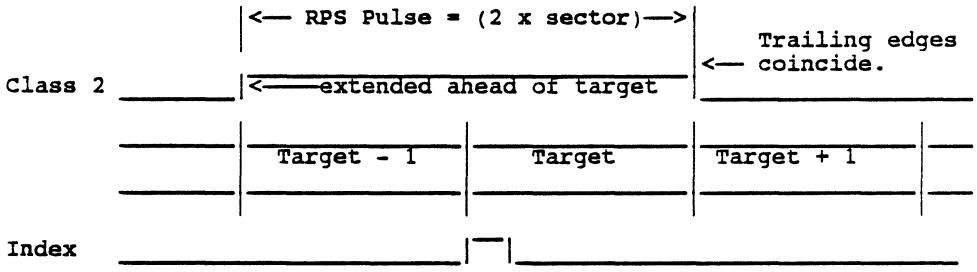
The trailing edge of the RPS Pulse shall coincide with the trailing edge of the sector specified by the Target Address parameter unless the Skew is set to a value greater than 0000h. See Figure 2..

(3) The slave shall skew the entire RPS Pulse ahead of the sector's trailing edge specified by the Target Address the number of octets specified with the Skew parameter. See Figure 3 and 4.

The Skew is set to 0000h at power-on Reset or with a Slave Reset and shall be reset to 0000h if a Load Format Specification is accepted by the slave.

(4) The slave rejects the command if the Target Address does not equal a valid sector address (0000h to the number of sectors per track minus 1). The number of sectors per track is specified in the Read Format Specification Response.

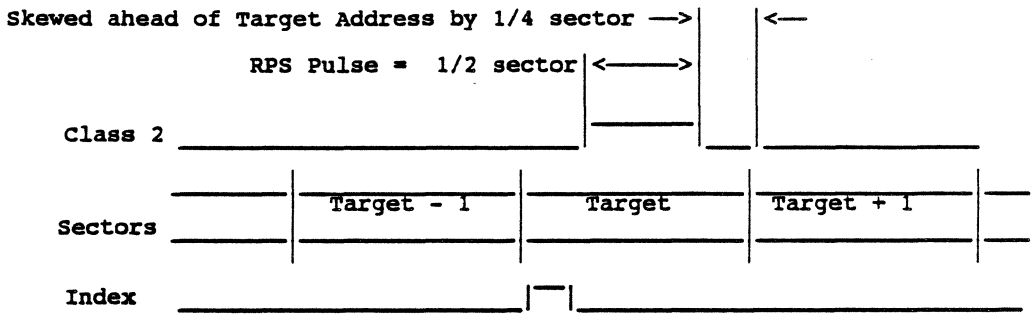
The slave sets Bus Control Exception, Invalid Parameter, and then reports Operation Exception in Slave Status.



Target Address = 0000h
Extension = 0001h
Pulse Width = Number octets per sector (last valid format)
Skew = 0000h

RPS Pulse = (Extension value + 1) x (Pulse Width)

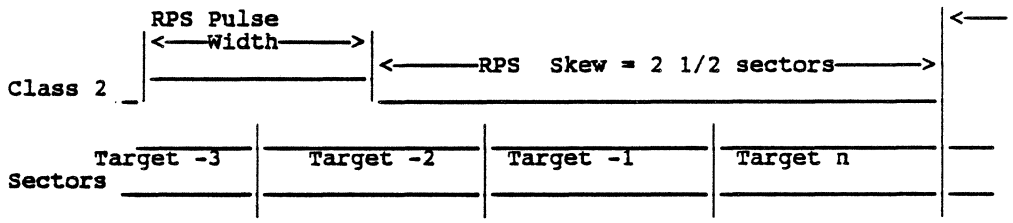
Figure 2 — RPS Pulse with extension Example



Target Address = 0000h
Extension = 0000h
Pulse Width = (octets per sector) / 2
Skew = (octets per sector) / 4

RPS Pulse = (Extension value + 1) x (Pulse Width)

Figure 3 — RPS Pulse with width and skew Example



Target Address = n
Extension = 0000h
Pulse Width = octets per sector
Skew = 2.5 x (octets per sector)

RPS Pulse = (Extension value + 1) x (Pulse Width)

Figure 4 — RPS Pulse with skew Example

6.8 Slave ECC/CRC

A slave may optionally implement data error detection and/or correction codes. CRC (Cyclic Redundancy Code) provides for detection of data errors, and ECC (Error Correction Code) provides correction as well as detection capability for data errors. The feature is indicated in the Read Configuration response (41h) and provides different capabilities in buffer and non-buffer mode. For non-buffer mode, the feature permits detection and reporting of ECC/CRC errors at the Slave, and generation of ECC correction vectors at the Slave for use by the master. For buffer mode, the feature permits the detection and reporting of errors, and correction of errors by the Slave. The master directs the slave to append ECC/CRC octets to Field 0 and data fields with the Encoded ECC/CRC Operation parameter in the Format Specification Flag octet. Either ECC or CRC for Field 0 may be selected by the Master, only ECC may be selected for data fields. Slave ECC or CRC may not be selected for Field 0 by itself, however, ECC may be selected for data fields without selecting ECC/CRC for Field 0.

A slave operating in buffer mode with Slave ECC/CRC selected shall only operate in Full Sector Transfer attribute. If ECC/CRC is enabled at the Format Specification, a Load Buffer Control command without Full Sector Transfer attribute set is rejected as Bus Control Context.

Slave operation during reads is controlled using the Load Slave Function bus control (01h). When enabled with the Enable Slave ECC/CRC Function code (2Dh), ECC and CRC errors detected during non-buffer mode are reported to the Master in the Slave Status. Detection of uncorrectable ECC errors in data fields are also reported at the Slave Status. The slave shall terminate after the field in which a CRC or ECC error is detected. If the Slave Status octet indicates a correctable ECC error occurred, the master may obtain the correction vectors using the Read Correction Vectors bus control (45h). No correction vectors are available for CRC errors or uncorrectable ECC errors.

During buffer mode, the slave may be set to only report detected errors, or correct ECC correctable errors. The correction of ECC errors occurs in the Slave buffer, and is reported to the Master in the Slave Status. The detection of CRC errors or uncorrectable ECC errors during buffer mode is also reported at the Slave Status. When a Slave detects a CRC error or uncorrectable ECC error, or if reporting but not correction of ECC errors is enabled, the slave shall transfer the data to the Master, and present the Slave Status after the transfer of the field in which the error was detected. The Read Buffer Mode is not disabled, the master may either continue reading remaining data, or terminate the transfer and enter a Data Recovery Procedure. During the Verify Buffer Mode, the master shall specify either Stop on Exception or Continue on Exception for CRC or uncorrectable ECC errors, or if a correctable ECC error is detected, but correction is not enabled, on the header (field 0). Buffer Mode reporting and correction are enabled using the Enable Slave ECC/CRC Function Code (2Dh).

Reporting of ECC/CRC and buffer correction of ECC errors are disabled using the Disable Slave/ECC function Code (2Ch).

The slave operation for non-buffered mode is shown below:

Encoded ECC/CRC in Format Spec		Field 0 post-gap	Field n-1 post-gap	Function code 2Dh	Slave Action
0	0			enabled	reject function code (note 1)
		none	none	disabled	
0	1	ECC	ECC	enabled	report errors
		ECC	ECC	disabled	don't report errors
1	0			-	reject format spec (note 2)
1	1	CRC	ECC	enabled	report errors
		CRC	ECC	disabled	don't report errors
NOTES 1 Out of Context 2 Invalid Parameter					

The slave operation for buffer mode is shown below:

Encoded ECC/CRC in Format Spec		Field 0 post-gap	Field n-1 post-gap	Function code 2Dh	Function code 21h	Slave Action
0	0			-	**en**	**reject** bus control (note 1)
				en	-	reject bus control (note 1)
		none	none	dis	dis	
0	1	ECC	ECC	en	**en**	**report errors/correct errors**
		ECC	ECC	dis	**en**	**no report/correct** errors
		ECC	ECC	en	**dis**	report/no correct
		ECC	ECC	dis	**dis**	no report/no correct
1	0					reject format spec (note 2)
1	1	CRC	ECC	en	**en**	**report errors/correct errors**
		CRC	ECC	dis	**en**	**no report/correct** errors
		CRC	ECC	en	**dis**	report/no correct
		CRC	ECC	**dis**	**dis**	no report/no correct
NOTES 1 Out of Context 2 Invalid Parameter						

The following Command/Response bus control codes contain parameters related to Slave ECC/CRC.

Bus Control Code (Hex)	Command/Response Control
01	Load Slave Function Function code (hex): 21 Enable Slave ECC Correction 2C Disable Slave ECC/CRC 2D Enable Slave ECC/CRC
02	Load Format Specification Encoded ECC/CRC Operation
0C	Load Buffer Control Full Sector Transfer attribute
41	Read Configuration Slave ECC/CRC Buffer Mode
44	Read Status ECC/CRC Fault
45	Read Correction Vectors
48	Read Extended Status Slave ECC/CRC Enabled

6.9 Spin up sequencing

A master can manage the power line surge current while the slaves are reaching operating speed through the use of spin up sequencing. Spin up sequencing can be done by issuing the Spin up function code to sequentially start the spindle motors. The Command Completion interrupt for the Spin up function shall not occur until the slave is up to speed.

The Spin up function code is optional and alternative means may be provided to manage the power line surge current. If Spin-up function code is supported by the slave and is enabled, the slave shall not turn on its motor when power is applied.

6.10 Enhanced Mode

The slave is required to be in the Enhanced Mode for the master to use the enhancements described in this standard. The purpose of Enhanced Mode is to allow a transition period for controllers to implement the enhancements described in this standard. An IPI-2 slave that supports the ISO/IEC 9318-2 standard only, shall reject the Load Function code (17h), Enable Enhanced Mode. After Power-on or Slave Reset, depending on the slave configuration type (see 6.10.1), the slave may be in the ISO/IEC 9318-2 or the Enhanced Mode described by this standard. The slave shall support one mode only at both ports. A slave may support one or more enhancements. After the slave is in the Enhanced Mode, the enhancements supported shall be transferred in the Read Configuration response described in this standard.

6.10.1 Configuration types

The slave may support one of the following configuration types.

6.10.1.1 Type A

The Type A slave shall have the capability to support the ISO/IEC 9318-2 mode and the Enhanced Mode. After Power-on, the Type A slave is in the ISO/IEC 9318-2 mode. The Type A slave shall accept a Load Function code (17h). The Type A slave shall support the ISO/IEC 9318-2 mode until acceptance of the Load Function code (17h) at a port. After acceptance of (17h), both ports shall operate in the Enhanced Mode described in this standard.

6.10.1.2 Type B

The Type B slave shall only support the Enhanced Mode. After Power-on, the Type B is in the Enhanced Mode. The Type B slave shall accept a Load Function code (17h). This is a no operation as the slave is always in the Enhanced Mode. The Type B slave is not required to support connection to a master not implementing the Enhanced Mode of operation.

6.11 Spindle Synchronization

The Spindle Synchronization feature allows a means for the master to synchronize the spindles of the slaves in a string to a Sync Reference Signal. The Sync reference signal shall be provided only by the master or one of the slaves. The slave shall be capable of providing the sync reference signal.

Index Offset allows the master to set an offset angular delay.

Local Spindle Sync is an optional sub-feature and it is described in 6.11.1.

The following Command/Response bus control codes contain parameters related to Spindle Synchronization, Index Offset and Local Spindle Sync.

Bus Control Code (Hex)	Command/Response Control
01	Load Slave Function Function code (Hex): 2E Disable Spindle Sync Reference Signal 2F Enable Spindle Sync Reference Signal 30 Disable Spindle Sync Transition Status 31 Enable Spindle Sync Transition Status 32 Disable Spindle Sync 33 Enable Spindle Sync 34 Spindle Re-Sync
09	Load Index Offset
41	Read Configuration Spindle Sync Local Spindle Sync
44	Read Status Spindle Sync Transition, Unlocked to Locked Spindle Sync Transition, Locked to Unlocked Spindle Sync Fault
48	Read Extended Status Spindle Sync Enabled Spindle Sync Transition Status Enabled Spindle Offset Active Spindle Sync Reference Source Enabled Spindle Sync Locked Local Spindle Sync Enabled

6.11.1 Local Spindle Sync

The Local Spindle Sync sub-feature provides a mechanism (switches or jumpers) to control the spindle Sync feature and it is indicated in Read Configuration.

The Local Spindle sync implementation is vendor unique but interrupt and status structure of the Spindle Sync shall be supported.

If Local Spindle Sync is enabled by the slave's local mechanism, the slave shall report the condition in the Read Extended Status. When the Local Spindle Enabled bit is set in Read Extended Status, the slave may accept Spindle Sync related commands depending on the conditions of the Local Spindle Sync control mechanism.

Command/Response bus control codes and parameters related to the Local Spindle Sync sub-feature are shown in 6.11.

6.12 Parallel Heads

The Parallel Heads feature provides a method whereby data is written to and read from multiple heads simultaneously thus increasing the streaming data transfer rate on the IPI-Physical interface. Also, the track length (octets per head address) is increased, providing a longer sustained data transfer before a head switch or seek is required.

The way in which data is organized on parallel heads (data interleave factor) is defined by octet 2, bits 7 through 3 in the Format Specification. An example is octet interleave (00111b). In this mode, the first octet transferred across the interface (Bus A) is written to the first ordered head of the head address, the second octet (Bus B) to the second ordered head of the same head address, the third octet (Bus A) to the third ordered head of the same head address, and so on. Octets 22h-25h in the Read Configuration define what interleaves are supported by the slave.

The following Command/Response bus control codes contain parameters related to Parallel Heads.

Bus Control Code (Hex)	Command/Response Control
02	Load Format Specification Data Interleave Factor
41	Read Configuration Parallel Heads Supported Interleave

6.13 Buffer Mode

The Buffer Mode co-exists with Non-Buffer Mode unless it is the Buffer Mode Only slave. The Load Position and Load Target Address commands are used to switch slave from Non-Buffer Mode to the Buffer Mode. The Buffer Mode supports reading and writing from or to the slave using sector type data controls. If supported, this feature shall be indicated in the Read Configuration response. A value is set in the Encoded Buffer Mode parameter of the Load RPS Target Address and Load Position commands to indicate Buffer Mode.

The following Buffer Modes are supported:

1. Write Buffer Mode: Stop on Exception
2. Verify Buffer Mode:
    a. Stop on Exception
    b. Continue on Verify Miscompare
    c. Continue on Missed Sync Byte
    d. Continue on Missed Sync Byte or Verify Miscompare
    e. Continue on CRC/ECC error
    f. Continue on Verify Miscompare or CRC/ECC error
    g. Continue on Missed Sync Byte or CRC/ECC Error
    h. Continue on Missed Sync Byte or Verify Miscompare or ECC error
3. Read Buffer Mode:
    a. Stop on Exception
    b. Continue on Missed Sync Byte
    c. Continue on ECC error
    d. Continue on Missed Sync Byte or ECC error
4. Read Immediate Buffer Mode :
    a. Stop on Exception
    b. Continue on Missed Sync Byte
    c. Continue on ECC error
    d. Continue on Missed Sync Byte or ECC error

The Continue on Exception mode of operation supports the sector slipping method of defect management, which is described in annex G.

6.13.1 Transfer Rate and Buffer size

The Buffer Mode supports the enhanced IPI transfer rate and the disk transfer rate. The master specifies the desired interface transfer rate in the Load Buffer Control command. If the slave can not support it, the slave shall change to the closest possible transfer rate (not greater than the specified maximum transfer rate). The master may perform a Read Buffer Control response to determine the agreed transfer rate.

6.13.2 Attributes of Buffer Mode

There are two attributes of the Buffer Mode feature and both can be set for any one of the Buffer Modes. The slave shall support all attributes.

6.13.2.1 Buffer Across Cylinder Boundaries Attribute

Normally buffer operation is performed within a cylinder and if End of Cylinder is reached or Buffer Exception Maximum Count equals zero, the slave reports Operation Exception error with End of Cylinder in Status Response. If buffer operation across cylinder boundaries is desired by the master, then master is required to set "Buffer Across Cylinder Boundaries" attribute bit (in the Load RPS Target Address or Load Position commands) and specify "Address of Last Buffer Operation Cylinder" in the Load Buffer Control command. The master may optionally provide a Cylinder Slip table to the slave via the Load Cylinder Slip table command. The Cylinder Slip table size is available in the Read Disk Specification response. The slave checks for cylinder slippage information before performing an internal seek during cylinder crossing.

The sector slipping technique of defect management is fully supported in this mode. The use of cylinder slipping is up to the master. If the master does not want to use cylinder slipping, it shall set the first entry of the Cylinder Slip Table to FF..FFh. The slave shall automatically reload the Buffer Exception Maximum Count when crossing a cylinder boundary. The cylinder slip table is not used by the slave to translate the cylinder address of a Load Position or Load Cylinder command. The master shall keep its own defective cylinder table so that it can calculate the proper physical cylinder address to issue to the slave.

The master may choose to enable and disable buffering across cylinder boundaries on the fly based on the expected size of the data transfer associated with a Load Position command. Higher performance can be achieved with this attribute turned off for short transfers and turned on for long transfers. Turning this attribute off for short transfers prevents the slave from performing an internal seek which might delay a subsequent positioning operation requested by the master.

Buffering across cylinder boundaries for the Read Buffer Mode and the Write Buffer Mode is explained in the following sections.

6.13.2.1.1 Writing Across Cylinder Boundaries

The master transfers a Load Position command specifying Write Buffer Mode with the Buffer Across Cylinder Boundaries attribute bit set. The slave starts requesting data from the master and writes it to the media. When the slave reaches the end of the cylinder, the slave performs an internal single track seek (assuming it is not already on the Last Buffer Operation Cylinder). The slave continues to write data on the new cylinder until it runs out of data or a Load End of Write command is transferred. Defective cylinders can automatically be skipped over.

6.13.2.1.2 Verifying Across Cylinder Boundaries

The master transfers a Load Position command specifying Verify Buffer Mode with the Buffer Across Cylinder Boundaries attribute bit set. The slave starts requesting data from the master and writes it to the media at the appropriate verified sectors. When the slave reaches the end of the cylinder, it may get verify miscompares on the spare sectors at the end of the cylinder. As long as the end of the cylinder is reached before or coincident with the Buffer Exception Maximum Count the slave performs an internal single track seek (assuming it is not already on the Last Buffer Operation Cylinder). The slave continues to verify headers and writes data on the new cylinder until it runs out of data or a Load End of Write command is transferred. Defective cylinders can automatically be skipped over as described above.

6.13.2.1.3 Reading Across Cylinder Boundaries

The master transfers a Load Position command specifying Read Buffer Mode and a target sector with the Buffer Across Cylinder Boundaries attribute bit set. The slave starts filling the buffer at the target sector and continues filling the buffer (as long as it is not full) until it reaches the end of the cylinder (the logical head switch sector on the last head). All sectors including spare sectors are read into the buffer. The master shall discard the unused spares by master terminating the transfer or by reading the data and ignoring it. When the slave reaches the end of the cylinder, it does an internal single cylinder seek to the next available cylinder (unless it is already on the Last Buffer Operation Cylinder) and continues reading based on the cylinder sector offset (CSO) and the zone sector offset (ZSO). Defective cylinders, as defined by the master with the Load Cylinder Slip Table command, are skipped over.

6.13.2.1.4 Read Immediate Across Cylinder Boundaries

The master transfers a Load Position command specifying Read Immediate Buffer Mode with the Buffer Across Cylinder Boundaries attribute bit set. The slave starts reading from the media at the first available sector and reads the entire first track. The slave continues to read and fill the buffer (as long as it is not full) until it reaches the end of the cylinder (the logical head switch sector on the last head). All sectors including spare sectors are read into the buffer. The master shall discard the unused spares by master terminating the transfer or by reading the data and ignoring it. When the slave reaches the end of the cylinder, it does an internal single cylinder seek to the next available cylinder (unless it is already on the Last Buffer Operation Cylinder) and continues reading based on the cylinder sector offset (CSO) and the zone sector offset (ZSO). Defective cylinders, as defined by the master with the Load Cylinder Slip Table command, are skipped over.

6.13.2.2 Full Sector Transfer Attribute

If the master desires to transfer only full sectors of data in buffered mode, The Full Sector transfer Attribute bit in the Load Buffer Control shall be set by the master. If ECC/CRC is enabled by the master in the Format Specification, Full Sector Transfer Attribute shall be set.

6.13.2.2.1 Full Sector Mode During Writes

The drive will not attempt to write a sector of data to the media unless the entire sector of data is in the buffer. The host is allowed to throttle the transfer or select a slower interface transfer rate than drive transfer rate without risk of a data underrun. The drive will internally slip revolutions in the absence of a full sector of data to write to the media.

6.13.2.2.2 Full Sector Mode During Reads

The drive will only release a sector of data to the host when a full sector of data is in the buffer. The drive will report logical busy status for any data control that is issued when less than a full sector of data is in the buffer. The interface transfer rate will never change to the native drive rate in this mode of operation. The host is still allowed to throttle the transfer during full sector mode reads. The agreed transfer rate can be set to anything supported by the drive without risk of an overrun.

6.13.3 Write Buffer Mode

When the master transfers a Load Position or Load Target Address command, specifying the Write Buffer Mode, the slave shall set a Class 2 Buffer Available Interrupt as soon as it is able to start filling its buffer. The master can then transfer data into buffer at the previously agreed to transfer rate and then disconnect from the slave to manage other drives on the string. Meanwhile, the slave shall empty the buffer at the disk rate and then set another Class 2 Buffer Available Interrupt when the buffer has space for more data. If there is no space for more data based on Attribute in Buffer Control, the slave shall set logical busy (81h) to a sector Data Control and accept In Context bus controls (e.g., End of Write, Modify Buffer Available Interrupt Delay). The master is allowed to transfer as many data controls and as much data as the buffer can hold. When the master is finished **transferring** write data to the slave, a Load End of Write command is transferred. The slave generates a TDO Slave Status for this command and finishes writing the data to media from the buffer. If data is not available while writing a sector on the media, write operation shall be disabled and Buffer Operation Exception shall be reported with the Write to Buffer Late bit set in the Status Response. If data is not available between sectors and Load End of Write has not been transferred, the slave shall slip revolutions until more data is available in the buffer **and then continue the write to media operation at the next ordered sector.** If the write completes without an

exception the slave sets a Class 1 Interrupt. If an exception occurs during the Write Buffer Mode, the slave sets a Class 3 Interrupt and sets the exception bits in the Status Response indicating the type of exception.

The Write Buffer Mode shall be disabled but write to media may continue for any of the following conditions unless specified otherwise:

(1) End of Cylinder (EOC) and Buffer not empty - The slave detects End of Cylinder during Write Buffer Mode and data is in the buffer, the Write Buffer Mode and write to media shall be disabled. **In Buffer Across Cylinder Boundaries mode of operation EOC means the end of the last buffer operation cylinder.** The following table shows the Slave Status, the Interrupt, a TDO and the Status Response.

Table 3 — End of Cylinder

Conditions	Slave Status	Interrupts	TDO	Status Response
EOC before or during data control	99h	3	Y	EOC, Residual Count
Bus Control after 99h and before class 3 Int	89h	3		EOC, Residual Count
*Bus Control after 99h and after class 3 Int	8Ch	3		EOC, Residual Count
* Exception - Read Status Bus Control Note — Class 3 Interrupt for Write and Verify Buffer Mode is considered as Asynchronous Solicited Class 3 Interrupt and the master is required to read Status Response.				

(2) Any Out of Context bus control- If the master transfers a bus control other than Load EOW, Write Buffer Mode shall be disabled but write to media continues. A TDO bit shall be set along with Operation Exception bit in the Slave Status. The slave also sets Bus Control Context in the Status Response. When write to media operation is complete without an exception, the slave sets the Class 3 Interrupt to report the Bus Control Context and indicate Command Completion to the master. The following table shows the Slave Status, the Interrupt, a TDO and the Status Response.

Table 4 — Out of Context Bus Control

Conditions	Slave Status	Interrupts	TDO	Status Response
Before or After EOW	98h	3	Y	Bus Control Context
Bus Control after 98h and before class 3 Int	89h	3		Bus Control Context
*Bus Control after 98h and after class 3 Int	8Ch	3		Bus Control Context
* Exception - Read Status Bus Control Note — Class 3 Interrupt for Write and Verify Buffer Mode is considered as Asynchronous Solicited Class 3 Interrupt and the master is required to read Status Response.				

(3) Logical reset from the port - If Logical Reset is issued from the either port, provided there is no allegiance at the alternate port, the Write to Buffer Mode and write to media shall be disabled at the end of current field. **The slave may not guarantee the completion of the write to media.**

(4) Parity error -

Not Full Sector Mode - If an interface parity error occurs during the Write Buffer Mode shall be disabled but write to media continues **to the end of the field.** A TDO bit shall be set along with Bus Parity Error in the Slave Status. When write to media operation is complete, the slave sets Class 1 Interrupt to report Command Completion to the master.

Full Sector Mode - **An** interface parity error **causes** the Write Buffer Mode and write to media **to be disabled. All sectors prior to the sector with the parity error shall be written to the media.** The slave shall not write **the** bad sector **of** data **from the** buffer to **the** media.

The following table shows the Slave Status, the Interrupt, a TDO and the Status Response.

Table 5 — Parity Error

Conditions	Slave Status	Interrupts	TDO	Status Response
Interface parity Error	50h	1	Y	n/a
Bus Control after 50h and before class 1 Int	81h	1		

(5) Master unsuccessful transfer - If the Master Status indicates an unsuccessful transfer, the Write Buffer Mode shall be disabled but write to media continues if the Full Sector Transfer attribute is not set. A TDO bit shall be set in the Slave Status. When write to media operation is complete, the slave sets Class 1 interrupt to report Command Completion. If the Master Status indicates an unsuccessful transfer, the Write Buffer Mode and write to media shall be disabled if Full Sector Transfer attribute is set. The slave shall not write bad sector data from buffer to media if Full Sector Transfer attribute is set. The following table shows the Slave Status, the Interrupt, a TDO and the Status Response.

Table 6 — Master Unsuccessful Transfer

Conditions	Slave Status	Interrupts	TDO	Status Response
Unsuccessful Transfer	10h	1	Y	n/a
Data control after 10h and before Class 1 Int	81h	1		

Notes
1. If the master status indicates unsuccessful transfer and Full Sector Mode is set, the slave shall not write data on media.
2. If the master status indicates unsuccessful transfer and Full Sector Mode is not set, the slave shall write data on media.

The Write Buffer Mode and write to media shall be disabled immediately for one of the following conditions:
(1) Slave Reset
(2) Buffer Fault (Hardware error)

See 7.2.1.7.2 for supported data controls in the Write Buffer Mode.

It is implied in the Buffer Mode that the first write data control after a Load Position command shall operate at Target Sector. Step Head increment is not allowed in the Buffer Mode of operation as the slave does automatic step head.

6.13.4 Verify Buffer Mode

When the master transfers a Load Position or Load Target Address command, specifying the Verify Buffer Mode, the slave shall set a Class 2 Buffer Available Interrupt as soon as it is able to start filling its buffer. The master can then transfer data into buffer at the previously agreed to transfer rate and then disconnect from the slave to manage other drives on the string. Meanwhile, the slave shall empty the buffer at the disk rate and then set another Class 2 Buffer Available Interrupt when the buffer has space for more data. If there is no space **in the buffer** for more data the slave shall set logical busy (81h) to a sector Data Control and accept In Context bus controls (e.g., End of Write, Modify Buffer Available Interrupt Delay). The master is allowed to transfer as many data controls and as much data as the buffer can hold. When the master is finished **transferring** write data to the slave, a Load End of Write command is transferred. The

slave generates a TDO Slave Status for this command and finishes writing the data to media from the buffer. If data is not available while writing a sector on the media, write operation shall be disabled and Buffer Operation Exception shall be reported with the Write to Buffer Late bit set in the Status Response. If data is not available between sectors and Load End of Write has not been transferred, the slave shall slip revolutions until more data is available in the buffer **and then continue the write to media operation at the next ordered sector.** If the write completes without an exception the slave sets a Class 1 Interrupt. If an exception occurs during the Verify Buffer Mode, the slave sets a Class 3 Interrupt and sets the exception bits in the Status Response indicating the type of exception. **See 6.13.2.1.2 for an explanation of the Verify operation while Buffer Across Cylinder Boundary mode is set.**

Verify Buffer Mode shall be disabled and write to media may continue for one of the following conditions:

(1) End of Cylinder and Buffer not empty - See 6.13.3 for description.

(2) End of Cylinder and Verify Miscompare - The slave reaches End of Cylinder while verifying headers without successful verification. The following table shows the Slave Status, the Interrupt, a TDO and the Status Response.

Table 7 — End of Cylinder and Verify Miscompare

Conditions	Slave Status	Interrupts	TDO	Status Response
EOC and verify miscompare	99h	3	Y	EOC, Residual Count
Bus Control after 99h and before class 3 Int	89h	3		EOC, Residual Count
*Bus Control after 99h and after class 3 Int	8Ch	3		EOC, Residual Count
* Exception - Read Status Bus Control Note — Class 3 Interrupt for Write and Verify Buffer Mode is considered as Asynchronous Solicited Class 3 Interrupt and the master is required to read Status Response.				

(3) Any Out of Context bus control- See 6.13.3 for description.

(4) Logical reset from the port - If Logical Reset is issued from the either port, provided there is no allegiance at the alternate port, the Verify Buffer Mode and write to media shall be disabled at end of current field.

(5) Parity error - See 6.13.3 for description.

(6) Master unsuccessful transfer - See 6.13.3 for description.

The Verify Buffer Mode shall terminate immediately if one of the following conditions occur:

(1) Slave reset from the master

(2) Buffer Fault (Hardware error)

Stop on Exception:

(1) Missed Sync Byte: If Missed Sync Byte is detected during Verify Buffer Mode, the slave stops verifying headers and sets Class 3 Interrupt to report a status exception. The slave also reports Buffer Operation Exception along with Buffer Operation Sync Byte error in Status Response.

(2) Verify Header Miscompare: If Verify Header Miscompare occurs during write, the slave sets Class 3 Interrupt to report a status exception. The slave also reports Buffer Operation Exception along with Buffer Operation Verify Header Miscompare in Status Response.

Continue on Exception:

(1) Missed Sync Byte: If Missed Sync Byte is detected during Verify Write Mode, the slave continues to verify subsequent headers until verification occurs or Buffer Exception Maximum Count equals zero or detects End of Cylinder. There shall not be loss of orientation because of Sync Byte Error. The slave sets Class 3 interrupt to report a status exception if Buffer Exception Maximum Count equals zero and reports Buffer Operation Exception along with Buffer Operation Sync Byte Error in the Status Response.

(2) Verify Header Miscompare: If verify Header Miscompare occurs during write, the slave continues to verify header on subsequent headers at disk until header compares or it reaches Buffer Exception Maximum Count or detects End of Cylinder. The slave sets class 3 interrupt to report a status exception if it reaches End of Cylinder and reports Buffer Operation Exception along with Verify Header Miscompare in the Status Response.

See 7.2.1.7.3 for supported data controls in Verify Buffer Mode.

It is implied in the Buffer Mode that the first write data control after a Load Position command shall operate at the Target Sector Address. Step Head Data Controls are not allowed in the Buffer Mode of operation as the slave does automatic step head.

6.13.5 Read Buffer Mode

When the master transfers a Load Position or Load Target Address command, specifying Read Buffer Mode, the slave shall start to fill the buffer when it reaches the specified target sector and minimum space for a sector is available unless the data is already in the buffer. Data is no longer in the buffer once Slave Status is presented to the master. If the master transfers a Load Position command for the previously transferred data, the slave shall read from media and fill the buffer. The master can delay the Class 2 Buffer Available Interrupt to allow the buffer to partially fill with data or the Class 2 Buffer Available Interrupt can be sent as soon as data is available. The slave shall continue to fill the buffer as long as there is space for a sector in the buffer and it has not detected the End of Cylinder or until a bus control is transferred that clears the buffer. If the slave fills the buffer and the master is not ready to transfer data from the buffer, the slave shall slip revolutions until there is space in the buffer. The master may interrupt the data transfer between sectors and resume data transfer at a later time with no loss of data. If the master catches up with the buffer during the Read Buffer Mode causing the buffer to go empty, the slave shall transfer the remaining data at the disk rate. All sector type Read Data Controls except Step Head and at Target type data controls shall be supported. During the Read Buffer Mode with Sector Data Control, first Missed Sync Byte detected in a sector shall be the Slave Status for the end of the sector, however Ending Status Sequence shall occur at the field of occurrence.

The Read Buffer Mode shall be disabled for one of the following conditions:

(1) Any Out of Context bus control - If the master transfers bus control other than Read during the Read Buffer Mode, the Read Buffer Mode shall be disabled and Operation Exception bit shall be set in the Slave Status. The slave shall also set a Bus Control Context bit in the Status Response.
(2) Logical reset from either port provided there is no allegiance from the alternate port.
(3) Parity error - If parity error occurs on the interface, slave to master transfer shall terminate and Parity Error shall be set in the Slave Status.
(4) Master unsuccessful transfer - If the Master Status indicates an unsuccessful transfer, Read Buffer Mode shall be disabled.

The read from the media shall be disabled immediately for one of the following conditions:

(1) Slave Reset
(2) Buffer Fault (Hardware fault)

Stop on Missed Sync Byte: If Missed Sync Byte is detected during the Read Buffer Mode, the slave stops reading from the media and reports Data Exception, Missed Sync Byte in the Slave Status when the master transfers the sector.

Continue on Missed Sync Byte: If Missed Sync Byte is detected during the Read Buffer Mode, the slave continues read operation. If master requests for this data, the slave reports Data Exception, Missed Sync Byte in the Status Response.

See 7.2.1.7.4 for supported data controls in the Read Buffer Mode.

It is implied in the Buffer Mode that the first read data control after a Load Position or Load Target commands shall operate at Target sector. Step Head increment is not allowed in the Buffer Mode of operation as the slave does automatic step head.

6.13.6 Read Immediate Buffer Mode

Read Immediate Buffer Mode provides improved performance (by reducing latency) by having the slave start reading data off the media at the first available sector it encounters after the Read Immediate Buffer Mode command is transferred to the slave. The slave reads an entire track of data into the buffer starting at the first available sector and then performs a head switch. The slave continues to read data into the buffer using the Track Sector Offset (TSO), Cylinder Sector Offset (CSO) and Zone Sector Offset (ZSO) values as defined by the master. For instance if TSO is set to 2, the slave shall delay 2 sectors each time it performs a head switch before continuing to read data into the buffer. The data is then transferred to the master in the same order as it was read into the buffer (which of course would be out of order). The master shall reorder the data using information contained in the header of each sector to determine the proper order.

The master must determine if it makes sense to use the Read Immediate mode of operation based on the position on the track of the desired target sector and the amount of data to be read. It is not desirable to use the Read Immediate Buffer Mode if the target sector is towards the end of the track or the desired transfer is substantially less than a track. It is better to use the Read Buffer Mode in this situation. The master should make this determination on the fly and transfer the appropriate buffered read command to optimize performance.

The Target Address has no meaning to the slave when in the Read Immediate Buffer Mode.

Note - The master must set the Target Address to a valid value other than F..F's when conditioning for a Read Immediate operation as F..F's indicates the Diagnostic mode (see 7.1.6.2.1)

6.13.7 Auto Step Head - Buffer Mode

The slave manages the automatic step head at the track boundaries (track boundary does not necessarily occur at index) because the slave continues to fill the buffer with next contiguous sectors.

6.13.8 Sector Order Management

This standard supports a mechanism for operating on contiguous sectors in a repeatable specific order as controlled by the master via the Track Sector Offset, Cylinder Sector Offset and Zone Sector Offset Parameters. The values for all three parameters represent the sector times used by the master, while in the Non-Buffer Mode, to allow contiguous sector transfer, without loss of a revolution, across track, cylinder and zone boundaries.

In Non-Buffer Mode, Step Head Control is provided by the master for head switch. In Buffer Mode, the master is not allowed to issue Step Head Control and the head switching is done automatically by the slave. The Zone Sector Offset, Cylinder Sector Offset and Track Sector Offset are required by the slave to calculate the Starting Sector for head switch. After head switch, normally sector following index is the Starting Sector but in Buffer Mode waiting for index may result in loss of a revolution. When the slave reaches End of Cylinder, the master transfers another Load Position command and in the mean time the slave calculates the Starting Sector position for head switch.

6.13.8.1 Auto Head Step Sector (AHSS)

The Auto Head Step Sector is the sector where the slave, during Buffer Mode, shall step the head following the transfer of the sector to or from the disk (modifies the data control at the Auto Head Step Sector to a Step Head Type). The Auto Head Step Sector (AHSS) shall be the last sector of the Head Address (track) to be transferred to or from the disk. It is the slave's responsibility to locate the starting sector position following the Auto Head Step Sector before transfer of the first sector of the new Head Address.

The location of the Auto Head Step Sector shall be managed by the slave for each Head Address, Cylinder Address, and Zone using the values transferred for the Track sector Offset, Cylinder Sector Offset, and Zone Sector Offset. There shall be a Track Sector Offset, Cylinder Sector Offset and Zone Sector Offset value transferred for each zone.

The slave's power-on reset condition shall set the Track Sector Offset, Cylinder Sector Offset and Zone Sector Offset values to zero.

When the Track Sector Offset, Cylinder Sector Offset and Zone Sector Offset values are set to zero, the slave shall locate the Auto Head Step Sector (AHSS) at the last sector of all tracks.

The first reference Auto Head Step Sector is located at the last sector of Cylinder Address 0 and Head Address 0 of Zone 0. The first sector transferred at Zone Address 0, Cylinder Address 0 and Head Address 0 shall be Sector Address 0.

6.13.8.2 Track Sector Offset (TSO)

Each Increasing Head Address (track) may have its associated Auto Head Step Sector location modified with reference to the Auto Head Step Sector of the previous Head Address by a number of sectors defined by the value assigned to Track Sector Offset. This offset is to account for the sector times required for the Head Switch Time. This value may be equal to zero if Head Switch Time is accounted for in the drive's Format Specification.

6.13.8.3 Cylinder Sector Offset (CSO)

Each increasing Cylinder Address shall have its associated Auto Head Step Sector location modified with reference to the Auto Head Step Sector of the last Head Address of the previous Cylinder by a number of sectors defined by the value assigned to Cylinder Sector Offset. This offset is to account for the sector times required for a load Position Command time and Single Cylinder Seek time and may include the Head Switch time if not done concurrently with the seek. **Cylinders that are skipped over using the Cylinder Slip table are still counted in the AHSS calculation.**

6.13.8.4 Zone Sector Offset (ZSO)

At the increasing Zone boundary, the First Cylinder Address and Head Address 0 shall have its associated Auto Head Step Sector location modified with reference to the Index (start of Sector 0) by a number of sectors defined by the value assigned to Zone Sector Offset of the increasing Zone. This offset is to account for the sector times required for overhead time (Zone Switch Time) associated with Zone management and may include the Load Position Command time, Single Cylinder Seek time and Head Switch time to next Zone if not done concurrently. **The value of ZSO is defined separately for each zone as an offset from index and is not cumulative.**

6.13.8.5 Starting Sector (SS)

The Starting Sector is the first sector of the next sequential track to be transferred. Within a cylinder the Starting Sector is calculated each time a head switch occurs. When Buffer Across Cylinder Boundaries mode is set the Slave also calculates the Starting Sector each time the slave performs an internally initiated seek.

Formula for calculating the Starting Sector (SS) is shown below.

$$SS = \text{Remainder of } \frac{[(ZCN \times [CSO + ([\#HDS - 1] \times TSO)]) + (HD\# \times TSO) + ZSO]}{\text{Sectors per Track}}$$

Where:
ZCN = Zone Cylinder Number (Cylinder # - Starting Cylinder # in the same zone)
CSO = Cylinder Sector Offset
TSO = Track Sector Offset
HD# = **Head Number**
#HDS = Number of Heads **per Cylinder**
ZSO = Zone Sector Offset **for the Current Zone**

Examples of TSO, CSO and ZSO are shown in Annex A.

6.13.9 Buffer Diagnostics

The ability to perform read and write operations to the buffer only, which are necessary functions for diagnostic operations can be performed by setting the Target Address equal to FFFFh. The purpose of the diagnostic operation is to write data patterns into the buffer and read data from the buffer for the buffer verification.

6.13.9.1 Write Buffer Mode

When the Encoded Buffer Mode is set for the Write Buffer Mode, the buffer shall be set empty so the master can write data into the buffer. The Write Buffer Mode data controls can be used for the write buffer diagnostics. The Buffer Mode shall be disabled if one of the conditions is true from the Write Buffer Mode disable conditions list, which is described in 6.13.3.

6.13.9.2 Verify Buffer Mode

When the Encoded Buffer Mode is set for the Verify Buffer Mode, the buffer shall be set empty so the master can write data into the buffer. The Verify Buffer Mode data controls can be used for the Verify Buffer Mode diagnostics. The Buffer Mode shall be disabled if one of the conditions is true from the Verify Buffer Mode disable conditions list, which is described in 6.13.4.

When "Verify Header, Write Data" is transferred, the slave shall store the header and data in the buffer. If skip count is non-zero in the Format Specification, only the supplied data is stored and the data stored is unpredictable during a read back from buffer.

6.13.9.3 Read Buffer Mode

When the Encoded Buffer Mode is set for the Read Buffer Mode, the buffer shall be set full to allow a read operation. If the master performs a Read diagnostic before a Write or Verify diagnostic, slave shall accept the Read Buffer Mode and read data from the buffer, which may be undefined. The Read Buffer Mode data controls can be used for the Read Buffer Mode diagnostics. The Buffer Mode shall be disabled if one of the conditions is true from the Read Buffer Mode disable conditions list, which is described in 6.13.5.

6.13.10 Dual port - Buffer Mode

In a dual port implementation, data may be transferred to or from the port with allegiance. While performing a write, as **long as no explicit allegiance exists (the master has not reserved the port) the master can transfer part of the data through one port, deselect, and then select the alternate port and continue to transfer data to** the buffer. While performing a read operation, as **long as no explicit allegiance exists** the master can transfer **part of the data from one port and then switch to the alternate port and continue to transfer data. The master shall deselect from the slave only on sector boundaries.** Implicit Port switch during the Read Buffer Mode or the Verify Buffer Mode shall not disable the Buffer Mode of operation.

The buffer is a common resource for both ports and implicit or explicit allegiance to the port selected shall disallow an alternate port to disable the buffer with a Logical Reset.

6.13.11 Bus control codes related to Buffer Mode

The following Command/Response bus control codes contains parameters related to the Buffer Mode.

Bus Control Code (Hex)	Command/Response Control
0Bh	Load End of Write
0Ch	Load Buffer Control
	Flag and Attribute Octet
	Buffer Across Cylinder Boundaries attribute
	Full Sector Transfer Mode attribute
	Buffer Exception Maximum Count
	Buffer Size in Sectors
	Interface Transfer Rate (100 Kbytes/s)
	Inter-field Delay
	Track Sector Offset
	Cylinder Sector Offset
	Last Buffer Operation Cylinder
0D	Load Cylinder Slip table
41h	Read Configuration
	Buffer
44h	Read Status
	Buffer Operation exception
	Buffer Operation Sync Byte Error
	Buffer Operation Verify Header Miscompare
	Buffer Fault
	Residual Count
	End of Cylinder
	Write to Buffer Late
49h	Read Disk Specification
	Buffer Size in Octets
	Maximum Buffer Transfer Rate (100 Kbytes/s)
	Cylinder Slip table size
4C	Read Buffer Control
4D	Read Cylinder Slip table
Slave Status	Operation Exception and slave busy

6.14 Buffer Mode Only

Buffer Mode Only and Non-Buffer Mode can not co-exist in a slave. **A slave that supports the** Buffer Mode Only feature **operates in** Buffer Mode all the time. This type of slave accepts only Buffer Mode commands as it can not operate in the Non-Buffer Mode. At power on, this type of slave is in the Buffer Mode and can not be encoded to Non-Buffer Mode by the master. This feature allows the slave to support improved internal formatting. Higher format efficiency can be realized as gap timings are hidden from the master.

See 6.13 for following descriptions:

1. Transfer Rate and Buffer size
2. Attributes of Buffer Mode
3. Write Buffer Mode
4. Verify Buffer Mode
5. Read Buffer Mode
6. Read Immediate Buffer Mode
7. Auto Step Head
8. Sector Order Management
9. Buffer Diagnostics
10. Dual Port - Buffer Mode

6.14.1 Bus control codes related to Buffer Mode Only

The following Command/Response bus control codes contain parameters related to the Buffer Mode Only.

Bus Control Code (Hex)	Command/Response Control
0Bh	Load End of Write
0Ch	Load Buffer Control
	Flag and Attribute Octet
	Buffer Across Cylinder Boundaries Attribute
	Full Sector Transfer Mode Attribute
	Buffer Exception Maximum Count
	Buffer Size in Sectors
	Interface Transfer Rate (100 Kbytes/s)
	Inter-field Delay
	Track Sector Offset
	Cylinder Sector Offset
	Last Buffer Operation Cylinder
0D	Load Cylinder Slip table
41h	Read Configuration
	Buffer
	Buffer Mode Only
44h	Read Status
	Buffer Operation exception
	Buffer Operation Sync Byte Error
	Buffer Operation Verify Header Miscompare
	Buffer Fault
	Residual Count
	End of Cylinder
	Write to Buffer Late
49h	Read Disk Specification
	Buffer Size in Octets
	Maximum Buffer Transfer Rate (100 Kbytes/s)
	Cylinder Slip table size
4C	Read Buffer Control
4D	Read Cylinder Slip table
Slave Status	Operation Exception and slave busy

6.15 Modify Buffer Available Interrupt Delay

The Modify Buffer Available Interrupt Delay is a sub-feature of Buffer Mode. This sub-feature provides capability to the master to modify Buffer available Interrupt Delay without transferring a Load Position command or a Load Target Address command to the slave. This sub-feature allows the master to set a longer Buffer Available Interrupt Delay and modify to make it short as the request for data nears completion.

The master transfers "Modify Buffer Available Interrupt Delay" command to the slave during Verify Buffer Mode, Read Buffer Mode or Read Immediate Buffer Mode to vary Buffer Available Interrupt Delay. If parameters of this command control is set to FF..FFh, Buffer Available Interrupt Delay shall be disabled. If the master transfers this command when the slave is not in buffer mode, the slave shall reject this command with Operation Exception in Slave status and Bus Control Context in Status Response.

The following Command/Response bus control codes contain parameters related to the Modify Buffer Available Interrupt Delay sub-feature.

Bus Control Code (Hex)	Command/Response Control
0Eh	Modify Buffer Available Interrupt Delay
41h	Read Configuration
	Modify Buffer Available Interrupt Delay

6.16 Zoned Disk Drive

A Zoned Disk Drive stores more data compared to a conventional one zone disk drive. A Zoned Disk Drive has more than one zone. An outer zone has an increased capability of storing more data than an inner zone. Each zone requires a separate Format Specification and Format Specifications for all zones may be loaded with Load Format Command using format 3.

The following Command/Response bus control codes contain parameters related to Zoned Disk Drives.

Bus Control Code (Hex)	Command/Response Control
02h	Load Format Specification
	Format type code 3 = Zoned Disk Drive
41h	Read Configuration
	Zoned Disk Drive
49h	Read Disk Specification
	Zone Switch Time
	Number of Zones
4Bh	Read Slave Formatter Parameter
	Number of Zones
	Zone Number
	Address of first cylinder in zone
	Address of last cylinder in zone

6.17 Predictive Commands

The Predictive Commands feature provides a method to notify the slave to prepare for the specific data transfer operations. A slave may use this information to reduce seek times for some operations, optimally position a dual-element head, or prepare in another manner for specific data transfer operations. An Encoded Data Operation parameter occupies the most significant 2 bits of the most significant octet of the Load Cylinder Address, Load Head Address, Load Target Address, and Load Position bus parameters (see 7.1.4 for details), and specifies which of the following categories of Data Controls will follow:

- Read - Read Header/Read type sector data controls and Read type field data controls.
- Verify - Verify Header/Write Data type sector data controls and all field data controls which perform a read of field 0 and write of subsequent data fields. The Encoded Data Operation parameter is normally set to Verify when verify or read header/update data field type operations are performed.

- Write - Write Header/write Data type sector data controls and all write type field data controls. The Encoded Data Operation parameter is normally set to Write only when sectors are formatted (e.g., when headers are written).

The Read Current Position and Read Current Sector responses include the Encoded Data Operation parameter previously transferred to the slave (if any).

A slave shall reject any Write or Verify type sector data controls or Write type field data controls if the Encoded Data Operation parameter is set to Read. A slave shall not reject any Read or Verify type data controls if the Encoded Data Operation parameter is set to default, Verify or Write, however, increased occurrences of data errors and missing bytes may result. If a slave rejects a Data Controls that is out of context with the current Encoded Data Operation parameter, Bus Control Context shall be set at the Status Response.

Implementation Note for Buffer Mode: Predictive commands using the Encoded Data Operation parameter are not used for Buffered read and write operation, as the Encoded Buffer Mode parameter provides equivalent information to the slave. The Encoded Data Operation field is set to the default value (00) for Buffer Mode. If a slave supports both Buffer Mode and the Predictive Commands, the Encoded Data Operation parameter should be employed for any non-buffered read/write operations. The current Encoded Data Operation parameter is cleared by transfer of an Encoded Buffer Mode parameter.

Implementation Note for dual-element heads: The slaves that employ dual-element heads may have special positioning requirements. The Predictive commands feature provides the slave with the advance information necessary to center the proper head element over the track center. Specific positioning actions are implementation dependant.

The following Command/Response bus control codes contain parameters related to Predictive Commands feature.

Bus Control Code (Hex)	Command/Response Control
04h	Load Cylinder Address Encoded Data Operation
05h	Load Head Address Encoded Data Operation
06h	Load Target Address Encoded Data Operation
07h	Load Position Encoded Data Operation
41h	Read Configuration Predictive Commands
46h	Read Current Sector Address Encoded Data Operation
47h	Read Current Position Encoded Data Operation

6.18 Slave Data Recovery Levels

The Slave Data Recovery Levels feature allows Data Recovery actions to be implementation dependant at the slave while providing a generic command structure for the master. The order of the Data Recovery levels is arranged at the slave to use conditions first that provide highest likelihood of successful data recovery. The master uses the Load Slave Function Code 4Bh to instruct the slave to increment to the next Data Recovery Level. The master then issues the appropriate read type data controls. The response of a slave to a write type data controls is not defined. The Function Code 4Bh overrides any existing head offset or window strobe that was set by a prior specific Function code. The Slave Data Recovery Level is reset with the 4Ch Function code.

The following Command/Response bus control codes contain parameters related to the Slave Data Recovery Levels feature.

Bus Control Code (Hex)	Command/Response Control
01h	Load Slave Function
	Function code (hex)
	4Bh Increment Slave Data Recovery Levels
	4Ch Reset Data Recovery Levels
41h	Read Configuration
	Number of Slave Data Recovery Levels
48h	Read Extended Status
	Active Slave Data Recovery Level

6.19 Dual Port

The Dual Port consists of manual and programmed Enable/Disable controls for a port (static switching) and the logical constructs for dynamically switching of the slave between two ports. The switching of a slave to a port creates an allegiance of the slave's common resources to that port.

6.19.1 Port enable/disable

Ports may be individually enabled or disabled by command and by optional manual controls. When a port is disabled, it is not operational on the Physical Interface. The disabling of a port may be either orderly or destructive with the choice being implementation dependent. Both ports are enabled at power-on, if not disabled by manual means.

The orderly disabling of a port takes effect when the Physical Interface on that port is in the IDLE state and the slave is inactive. The destructive disabling of a port takes place immediately without regard to the state of the interface.

The enabling of a port takes effect when the Physical Interface on that port is in the IDLE state.

If a port is disabled by command, changing a manual port switch from Disable to Enable shall cause the port to be Enabled. However, the disabling of a port by a manual switch cannot be overridden by a command.

The disabling of a port, either by command or switch, shall cause any explicit or implicit Allegiance to be disabled and shall cause any solicited status associated with the disabled port to be cleared.

6.19.2 Slave accessibility

The slave may be in one or more of three conditions: Neutral, Implicit Allegiance or Explicit Allegiance.

6.19.2.1 Neutral

Following a power-on Reset or a Slave Reset, the slave enters the Neutral condition. While in the Neutral condition, the slave can be accessed via an enabled port and the Allegiance can be enabled either implicitly or explicitly.

6.19.2.2 Implicit allegiance (Physical)

An implicit allegiance occurs when a selection is initiated in accordance with the Physical Interface protocol described in ISO/IEC 9318-6 and the slave returns to the Neutral condition with de-selection.

6.19.2.2.1 Implicit Allegiance enable/disable

Implicit Allegiance is enabled at Selection and disabled after deselection.

6.19.2.2.2 Priority Implicit Allegiance

Priority Implicit Allegiance is enabled during the Selection sequence with the Priority Select bit = 1 in the Selection octet.

Priority Implicit Allegiance is disabled after deselection or if the alternate Port transfers a Selection sequence with the Priority Select bit = 1. The operation at the port may not be completed.

6.19.2.2.3 Status at the Alternate Port

After the occurrence of a Selection sequence that enables the Priority Implicit Allegiance, the Alternate Port Priority Selected bit is set in the Read Status Response and the Priority Select Status bit is set in the Slave Interrupts Octet.

The Priority Select Status bit in the Slave Interrupts Octet is cleared on the occurrence of a Request Slave Interrupts sequence or the acceptance of a Read Status response control at the Alternate Port.

6.19.2.2.4 Selective Reset

A Logical Reset at the Alternate Port does not effect the condition of Allegiance.

A Slave Reset at either port shall disable Allegiance. The operation at the port may not be completed.

6.19.2.3 Explicit allegiance (Physical and Logical)

An explicit allegiance occurs when a Reserve function code is accepted. The slave switches to that port. It remains in explicit allegiance until a Release function is accepted, the alternate port accepts a Priority Select, or the slave is reset with a Slave Reset at either port.

In addition, if a Priority Hold is transferred explicit allegiance occurs. The slave has explicit allegiance to the port selected. It remains in explicit allegiance until the alternate port is selected with a Priority Hold and a Priority Select, or this port is selected with Priority Hold cleared, or the slave receives a Slave Reset from either port.

6.19.2.3.1 Explicit Allegiance enable/disable

- An Explicit Allegiance remains enabled after deselection. An Explicit Allegiance may be controlled by the Physical (Selection sequence) method or the Logical (Function Code Transfer) method. Only one method is necessary and mixing is not recommended, however, both the physical and logical level Allegiance may be enabled at the same time.

- Physical Explicit Allegiance is enabled during the Selection sequence with the Priority Hold bit = 1 in the Selection octet.

  Physical Explicit Allegiance is disabled during the Selection sequence with the Priority Hold bit = 0 in the Selection octet or if the Alternate Port transfers a Selection sequence with both the Priority Hold and Priority Select bit = 1.

- Priority Physical Explicit Allegiance (Reservation) is enabled during the Selection sequence with the Priority Hold bit = 1 and the Priority Select bit = 1 in the Selection octet. Priority Physical Explicit Allegiance is disabled during the Selection sequence with the Priority Hold bit = 0 and the Priority Select bit = 0 in the Selection octet. The Alternate Port is not able to disable this allegiance.

- Logical Explicit Allegiance (Reservation) is enabled by the Load Function codes (14h - Reserve) during the Information Transfer Sequence.

  Logical Explicit Allegiance is disabled by the Load Function code (15h - Release) during the Information Transfer Sequence.

6.19.2.3.2 Mixing of Physical Explicit Allegiance and Logical Explicit Allegiance methods

- Physical Enable, Logical Enable.
  If the two methods are mixed and the Physical method is enabling while the Logical method is enabling, both the Physical Explicit Allegiance and the Logical Explicit Allegiance are enabled. (e.g., If Priority Hold bit = 1 and the Load Function Reserve is transferred.)

- Physical Disable, Logical Disable.
  If the two methods are mixed and the Physical method is disabling while the Logical method is disabling, both the Physical Explicit Allegiance and the Logical Explicit Allegiance are disabled. (e.g., If Priority Hold bit = 0 and the Load Function Release is transferred.)

- Physical Disable, Logical Enable.

If the two methods are mixed and the Physical method is disabling while the Logical method is enabling, the Logical Explicit Allegiance is enabled. (e.g., If Priority Hold bit = 0 and the Load Function Reserve is transferred.)

- Physical Enable, Logical Disable.
  If the two methods are mixed and the Physical method is enabling while the Logical method is disabling, the Physical Explicit Allegiance is enabled and the Logical Explicit Allegiance is disabled. (e.g., If Priority Hold bit = 1 and the Load Function Release is transferred.)

6.19.2.3.3 Physical Explicit Allegiance Status

When the Physical Explicit Allegiance is enabled or disabled, the following status bit is conditioned in the Slave Interrupt Octet:

Priority Hold Status

6.19.2.3.4 Logical Explicit Allegiance Status

When the Logical Explicit Allegiance is enabled or disabled, the following status bit is conditioned in the Read Extended Status:

Reserve Active

6.19.2.3.5 Effect of Selective Reset on Allegiance

A Logical Reset at the Alternate Port does not effect the condition of Allegiance.
A Slave Reset at either port shall disable Allegiance. The operation at the port may not be completed.

6.19.2.3.6 Effect of deselection on Physical Explicit Allegiance

Physical Explicit Allegiance remains after deselection, while Implicit Allegiance is lost after deselection.
An override at the Alternate Port results in a disabling of the Allegiance at the port. The operation at the port may not be completed.

Table 8 — Physical Explicit Allegiance

PORT NOT SELECTED							
Port A Select then De-Select		I=Implicit E=Explicit Physical Allegiance		Explicit is Cleared at Port A next Select with		Allegiance Override at Port B Select	
PH	PS			PH	PS	PH	PS
0	0	none		-	-	x	x
0	1	none		-	-	x	x
1	0	E		0	0	1	1
1	0	E		0	1	1	1
1	1	E		0	0	-	-
PORT SELECTED							
Port A Selected		I=Implicit E=Explicit Physical Allegiance				Allegiance Override at Port B Select	
PH	PS					PH	PS
0	0	I				x	1
0	1	I				x	1
1	0	I and E				1	1
1	1	I and E				-	-
PS = Priority Select bit, PH = Priority Hold bit, x = Don't Care							

6.19.2.3.7 Effect of deselection on Logical Explicit Allegiance

Logical Explicit Allegiance remains after deselection, while Implicit Allegiance is lost after deselection. An Override at the Alternate Port results in a disabling of the Allegiance at the port. The operation at the port may not be completed.

Table 9 — Logical Explicit Allegiance

PORT NOT SELECTED			
Port A transferred FC-14h then De-Select PH PS	L=Logical P=Physical Explicit Allegiance		Allegiance Override at Port B Select PH PS
0 0	L		x 1
0 1	L		x 1
1 0	P and L		1 1
1 1	P and L		- -
PORT SELECTED			
Port A transferred FC-14h Selected PH PS	L=Logical P=Physical Explicit Allegiance	Logical Explicit is Cleared when Port A transfers FC-15h	Allegiance Override at Port B Select PH PS
0 0	L	yes	x 1
0 1	L	yes	x 1
1 0	P and L	yes	1 1
1 1	P and L	yes	- -

PS = Priority Select bit, PH = Priority Hold bit
FC-14h = Function Code 14h, Reserve
FC-15h = Function Code 15h, Release

6.19.3 Dual port levels

The dual port level is a physical level.

6.19.3.1 Physical level

A **selection is not honored if a selection is active** at the alternate port, **unless the allegiance to the alternate port is overridden using a Priority Select.** The slave shall not report an interrupt for a port if an alternate port has an Allegiance. After the allegiance is disabled at the alternate port, the set interrupt shall be reported. The master can not service the interrupt, therefore interrupt shall not be reported to the master unless modified by the Load Port Control command. The reported interrupts for the physical level dual port are defined in Table **10.**

Table 10 — Interrupts Reported - Physical Level Dual Port

Port A Sel	Port A Resv	Port A Busy	Port B Sel	Port B Resv	Port B Busy	Port A Interrupt Reported	Port B Interrupt Reported
0	0	0	0	0	0	Yes	Yes
0	0	1	0	0	1	No	No
0	0	1	0	1	0	No	Yes
0	0	1	1	0	0	No	Note 1
0	0	1	1	1	0	No	Note 1
0	1	0	0	0	1	Yes	No
1	0	0	0	0	1	Note 1	No
1	1	0	0	0	1	Note 1	No
Note 1 — Interrupt octet is not presented while selected.							

6.19.4 Notification of Alternate Port exception condition

The occurrence of the following conditions on the alternate port shall be reported as an Unsolicited Exception in the Status Response:

- Priority Select;
- Format Specification changed;
- Reset complete;
- Receipt of the Notify Alternate Port of Format Complete Function Code (see 7.1.1.8).
- **Receipt of The Alternate Port Semaphore Function Codes (2Ah,2Bh)**

6.19.5 Busy

The slave can report busy by the Physical or Logical Busy method.

6.19.5.1 Physical Busy

Physical Busy is reported when the slave does not assert its Bit Significant Response at the Selection Sequence.

6.19.5.2 Logical Busy

Logical Busy is reported at Ending Status Sequence in the Slave Status Octet.

6.19.5.3 Allegiance and Busy

The slave shall report the Physical Busy at the Alternate Port when Allegiance is enabled to this port.

6.19.5.4 Busy and Dual Port

The slave shall report the Logical Busy only at the port that initiates the TDO operation.

The slave shall report the Physical Busy at the Alternate Port when the TDO operation is initiated at this port.

The slave can be configured to report a "No Longer Busy" interrupt as the result of a Physical Busy condition at the alternate port. The "No Longer Busy" interrupt is reported when the alternate port becomes available.

6.19.6 "No Longer Busy" attention

If a slave reports Physical Busy because it has Allegiance to an alternate port, then an ATTENTION IN shall be asserted when the slave becomes "No Longer Busy", if the "No Longer Busy" Attention is enabled.

6.19.7 Common Resources

Following are the common resources for both ports:

1. Class 2 Interrupts
2. Format Specification
   ECC\CRC
3. Buffer
4. HDA
5. Unsolicited Class 3 Interrupts

6.19.8 Bus control codes related to Dual Port

The following Command/Response bus control codes contain parameters related to Dual Port feature.

Bus Control Code (Hex)	Command/Response Control
41h	Read Configuration
	Dual Port
44h	Read Status
	Unsolicited Exception
	Alternate Port Priority Select
	Alternate Port Format Changed
	Alternate Port Target Modifier Change
48h	Read Extended Status
	Interface Flags
	Port Number 1
	Port Number 0
	Port 1 Enabled
	Port 0 Enabled

6.20 Port Control

The Port Control feature allows the master to disable the effect of an Allegiance at the alternate port. The slave shall support Dual Port in order to provide this feature.

When the Explicit (Reserve) Allegiance and the Implicit (Selection) Allegiance are not active at the alternate port, interrupts shall be reported.

After a Power-On Reset or Slave Reset, an active Explicit (Reserve) Allegiance or an active Implicit (Selection) Allegiance at the alternate port shall disable the reporting of interrupts.

The Load Port Control command disables the effect of an active Allegiance at the alternate port. The result is that the active Allegiance at the alternate port shall not effect the reporting of the indicated interrupt.

The Read Port Control response shall transfer the disabling conditions accepted by the slave in Load Port Control command.

The following Command/Response bus control codes contain parameters related to Port Control feature.

Bus Control Code (Hex)	Command/Response Control
41h	Read Configuration Port Control
0Ah	Load Port Control
4Ah	Read Port Control

6.21 Target Modifier

The Target Modifier feature provides a method to modify the target sector address without reissuing a Load Position or Load Target Address command. **This command is only available while operating in non-buffered mode. This command will be rejected as Out of Context if it issued while the slave is operating in buffered mode.**

The Load Target Modifier command control enables the step head data control to modify the target sector address and set a Class 2 interrupt at the RPS pulse following a data control with the step head control bit set. The modified target sector address is **computed as follows:**

(**number** of sector operated on with a data control with step head control bit set + **target modifier** + 1) modulo (the number of sectors per head address). See Target Modifier examples in Annex E.

The interrupt shall allow the master to re-establish orientation with the drive via a target type data control, read type control or verify header type data control. The Step Head control modification is disabled if the Target Modifier is equal to FFFFh.

If the step head control modification is supported, the Target Modifier is set to a value of FFFFh after a power-on Reset or a Slave Reset and shall be reset to FFFFh if a Format Specification is accepted by the slave.

The slave shall reject a Load Target Modifier command control if the Target Modifier is equal to one of the following:

(1) 0000h;
(2) A value greater than the number of fixed sectors per head address minus 1;
(3). A value less than the number of sectors it takes to perform a head switch.

The following Command/Response bus control codes contain parameters related to Target Modifier feature.

Bus Control Code (Hex)	Command/Response Control
08h	Load Target Modifier
41h	Read Configuration Target Modifier
4Fh	Read RPS parameters Target Modifier

6.22 Defect Map

The slave shall have a Defect Map containing a list of defects found by the manufacturer. This Defect Map is used by the master to reallocate defective storage when formatting the slave.

6.22.1 Location

The Defect Map shall be located on the last track of the cylinder identified in the Configuration Information as the Address of Last Defect Map Cylinder.

The Defect Map shall be recorded successively on each previous track until the map is complete.

6.22.2 Contents

A Defect Map may consists of more than one Defect Map Set. The number of sets and each is self identifying. Each data field in the Defect Map Sector shall be self-identifying. A Defect Map set consists of a Defect Map Sector repeated three times, with each data field of the Defect Map Sector identified as to whether it is the first, second, or third data field of a set. If a data field is not readable without errors at the factory, then it shall be identified. A set may consist of more than three Defect Map Sectors, being made up of three readable data fields and as many identified data fields that have read errors.

The tracks used for the Defect Map are formatted with the Manufacturer's Format Specification (see 6.2.2).

6.22.3 Formats

6.22.3.1 Defects

The locations of the defects is specified in terms of a Track Defect List. Each defect entry in the map is 12 octets long. The Track Defect List is used by the slaves that support a programmable sector size and the defect locations are specified in terms of octets from Index.

The defects in the Defect Map should be stored in order of increasing physical addresses. An exception may be made for those that are detected after the initial map was recorded and are added to the end of it by the manufacturer during final test. Any additions that are out of sequence should indicate this by setting the Flag bit within that data field.

The Offset of the Defect from Index is an offset value that specifies the location of a defect with respect to index and the ordered head that the data is read/written to. Any offset value less than the physical track length specifies the distance in octet from the Index of the defect on the first ordered head address (ordered head zero). For those slaves having more than one head per address, the defects for those heads (other than first ordered head) are identified by specifying an offset equal to the distance in octets from Index for that defect plus the ordered head number times the physical track length. (see Annex F)

6.22.3.2 Maps

The map is recorded with each data field recorded error free three times sequentially. Each data field in a set is identical to the other two. The following description describes the contents per data field, with the implicit understanding that each data field is physically recorded three times. Data field 0, the Header field, contains no Defect Map information.

Each data field of the map starts with a two octet count of the number of octets used in the field, not including itself. The first data octet is the bit significant Flag octet which is followed by the number of this data field within the set. All data fields within the Map shall either be identified by their data field number within a set, or set to FFh to be ignored.

The Number of sets in the Map, and the Number of this set Within the Map occupies the next two fields.

The first set in the Defect Map is numbered as 1. If there are no entries in the Defect Map the Number of Sets in the Map is set to zero in all three members of the set.

The following two fields provide the address of the first track at which the master may store Format Specifications or other information in the manufacturer's format.

All but the last two octets remaining are 12 octet entries containing defect information. The last 12 octet defect entry in a data field cannot be split, therefore any remainder of less than 12 shall be zeros. Similarly, the remainder following the last defect entry in the last data field of the Map shall be padded with zeros.

The last set of data fields in the Defect Map are identified by bit 7 of Octet 2 in each data field.

The contents of each data field in a set are identical except for the Data Field number within the set (Octet 3).

The format of each Defect Map sector is shown below:

Octet (Hex)	Bit	Description
00-01		Number of octets following: equals n-1 (Note 1)
02		Flag octet
	7	Last Data Field set of the Defect Map
	6	Defect Map continues on next lower cylinder
	5-4	Encoded Defect List
	3	Defect entries in this Data Field are out of sequence
	2-0	reserved, set to zero
03		Number of this Data Field within this Set
		00 = First
		01 = Second
		02 = Third
		03-FE = Illegal
		FF = Ignore
04-05		Number of Sets in the Defect Map
06-07		Number of this Set in the Defect Map
08-0B		Last Cylinder Address Available for Format Specification Storage
0C-0D		Last Head Address Available for Format Specification Storage
		DEFECT DESCRIPTOR (Note 2 and Note 3)
0h:3h		Cylinder address of the defect
4h:5h		Head address of the defect
6h:9h		Offset of defect from Index
Ah:Bh		Length of defect
(m+1):(n-2)		Zero (if any octets not filled by defect entries) (Note 4)
(n-1):n		CRC-16

Notes
1 n is the octet number of last octet transferred.
2 Defect Descriptor repeats as long as enough space (at least 12 octets per each defect for Defect Descriptor) is available.
3 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.
4 m is the octet number of the last octet (length of defect) of last Defect Descriptor loop.

6.22.3.2.1 Number of octets following (00h-01h)

This parameter contains the octet count for the **Defect Map.** It does not include itself in the octet count.

6.22.3.2.2 Flag octet (02h)

This parameter contains flag information for the **Defect Map.**

6.22.3.2.2.1 Last Data Field set of the Defect Map (Bit 7)

Bit 7 shall be set to indicate that this is the Last Data Field set of the Defect Map.

6.22.3.2.2.2 Defect Map continues on next lower cylinder (Bit 6)

Bit 6 shall be set to indicate that Defect Map continues on next lower cylinder.

6.22.3.2.2.3 Encoded Defect List (Bits 5-4)

Bit 5	Bit 4	
0	0	Track Defect List is used
0	1	Reserved for future use
1	0	Reserved for future use
1	1	Reserved for future use

6.22.3.2.2.4 Defect entries in this Data Field are out of sequence (Bit 3)

Bit 3 shall be set to indicate if Defect entries in this data field are out of sequence.

6.22.3.2.2.5 Bits 2-0 = 000b

6.22.3.2.3 Number of this Data Field within this set (03h)

This parameter specifies number of this data field within this set. 03h to FEh are illegal numbers and FFh should be ignored.

6.22.3.2.4 Number of sets in the Defect Map (04h-05h)

This parameter specifies the number of sets in the Defect Map.

6.22.3.2.5 Number of this set in the Defect Map (06h-07h)

This parameter specifies the number of this set in the Defect Map.

6.22.3.2.6 Last Cylinder Address Available for Format Specification Storage (08h-0Bh)

This parameter specifies the Last Cylinder Address Available for the master to store the Format Specification.

6.22.3.2.7 Last Head Address Available for Format Specification Storage (0Ch-0Dh)

This parameter specifies the Last Head Address Available for the master to store the Format Specification.

6.22.3.2.8 Cylinder Address of the defect (0Eh-11h)

This parameter specifies the Cylinder Address of the defect and it is repeated for each defect.

6.22.3.2.9 Head Address of the defect (12h-13h)

This parameter specifies the Head Address of the defect and it is repeated for each defect.

6.22.3.2.10 Offset of the defect from Index (14h-17h)

This parameter specifies the Offset of the defect from Index in octets if Track Defect List is used and it is repeated for each defect.

6.22.3.2.11 Length of defect (18h-19h)

This parameter specifies the length of defect bits and it is repeated for each defect.

6.22.3.2.12 CRC -16

This parameter specifies the CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and is considered part of the data area. It is the master's responsibility to check the CRC.

To calculate the CRC, the initial value of the seed shall be set to all ones (FFFFh)

To calculate the CRC correctly, the bits within each octet shall be recorded as bit 7 first i.e. on each double octet transferred, the first bit recorded to disk shall be bit 7 of BUS A and the last bit shall be bit 0 of BUS B. See Figure 6.

It is recommended that this same ordering be followed by the drive manufacturer for all data written to the media.

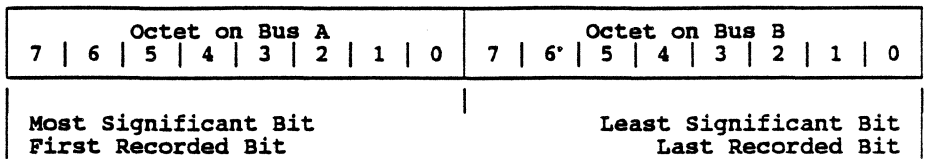


Figure 5 — Assignment of bits in Each Double Octet

6.22.4 Map Protection

It is recommended that the Defect Map be write protected by the manufacturer of the disk so that no action by the master can destroy the factory-supplied defect information. If the Defect Map is write protected by the manufacturer, the Address of Last Data Cylinder in Read Disk Specification response shall be less than the Address of Last Defect Map Cylinder.

7 Bus Controls

Bus Controls specify the condition of the bus and the information to be transferred. The three types of Bus Controls are: Command, Response, and Data. The Bus Control Code Octet has the following general form:

Bit	Description
7	1 = Data Control 0 = Command or Response Control
6	1 = Information In (Read) 0 = Information Out (Write)
5-0	Operation Specific

7.1 Command and Response Controls

The Command and Response Controls are Bus Controls that transfer command information to the slave and response information from the slave. The command and response information transferred consists of ordered lists of parameters. Parameters are transferred with the most significant octet first.

The valid Command and Response Controls are listed below and are described in 7.1.1 through 7.1.24. All other Command and Response Control codes (including 00h and 40h used in IPI Level 3) are rejected as being invalid.

If a slave does not support an optional feature, corresponding Bus Controls for the feature shall be rejected and Unsupported Bus Control shall be set in the Status Response. If a slave supports a feature, all Bus Controls associated with the feature are mandatory.

Bus Control Code	Command Control
01h	Load Slave Function
02h	Load Format Specification
03h	Load Slave Specific Information
04h	Load Cylinder Address
05h	Load Head Address
06h	Load Target Address
07h	Load Position
08h	Load Target Modifier
09h	Load Index Offset
0Ah	Load Port Control
0Bh	Load End of Write
0Ch	Load Buffer Control
0Dh	Load Cylinder Slip table
0Eh	Modify Buffer Available Interrupt Delay

Bus Control Code	Response Control
41h	Read Configuration
42h	Read Format Specification
43h	Read Slave Specific Information
44h	Read Status
45h	Read Correction Vectors
46h	Read Current Sector Address
47h	Read Current Position
48h	Read Extended Status
49h	Read Disk Specification Values
4Ah	Read Port Control
4Bh	Read Slave Formatter Parameter
4Ch	Read Buffer Control
4Dh	Read Cylinder Slip table
4Eh	Read TDO Response
4Fh	Read RPS Parameters

7.1.1 Load Slave Function (01h)

The Load Slave Function bus control code causes the slave to perform the action specified by the various function codes defined by this command. The function code is carried in both octets of the double-octet parameter transferred to the slave in the Information Transfer.

- If the two octets are not the same or the octets contain an invalid value, the command shall be rejected and the Invalid Parameter bit shall be set in the Status Response.
- If the two octets are same but the octets contain an invalid function code, the command shall be rejected and the Invalid Function Code bit shall be set in the Status Response.
- If the two octets are same but the octets contain an unsupported function code, the command shall be rejected and the Unsupported Function Code shall be set in the Status Response.

If a slave does not support an optional feature, the corresponding function codes for the feature shall be rejected and the Unsupported Function Code bit shall be set in the Status Response.

The format of the command shall be as follows:

Octet Parameters	Description
0	Function code
1	Function code repeated

The various functions and their hexadecimal codes are listed below and are described in 7.1.1.1 through 7.1.1.45. If a function code is related with a feature, the feature is indicated in parenthesis.

Function Code	Response Control
00h - 0Fh	Reserved for future use
10h	Disable Alternate Port (Dual Port)
11h	Enable Alternate Port (Dual Port)
12h	Disable Port (Dual Port)
13h	Reserved for future use
14h	Reserve (Dual Port)
15h	Release (Dual Port)
16h	Notify Alternate Port of Format Completion (Dual Port)
17h	Enable Enhanced Mode
18h	Disable successful Command Completion Interrupt (Class 1) attention
19h	Enable successful Command Completion Interrupt (Class 1) attention
1Ah	Disable RPS Interrupt (Class 2) attention
1Bh	Enable RPS Interrupt (Class 2) attention
1Ch	Disable status pending interrupt (Class 3) attention
1Dh	Enable status pending interrupt (Class 3) attention
1Eh	Disable "no longer busy" attention
1Fh	Enable "no longer busy" attention
20h	No operation
21h	Enable Slave ECC correction (Slave ECC/CRC)
22h	Spin up
23h	Spin down
24h	Load Heads (Load/Unload Heads)
25h	Unload Heads (Load/Unload Heads)
26h	Lock Carriage (Lock/Unlock Carriage)
27h	Unlock Carriage (Load/Unload Carriage)
28h	Recalibrate
29h	Perform Internal Diagnostic
2Ah	Set Alternate Port Semaphore 0)
2Bh	Set Alternate Port Semaphore 1
2Ch	Disable slave ECC/CRC Reporting (Slave ECC/CRC)
2Dh	Enable slave ECC/CRC Reporting (Slave ECC/CRC)
2Eh	Disable Spindle Sync reference signal (Spindle Sync)
2Fh	Enable Spindle Sync reference signal (Spindle Sync)
30h	Disable Spindle Sync transition status (Spindle Sync)
31h	Enable Spindle Sync transition status (Spindle Sync)
32h	Disable Spindle Sync (Spindle Sync)
33h	Enable Spindle Sync (Spindle Sync)
34h	Spindle Resync (Spindle Sync)
35h - 40h	Reserved for future use
41h	Reset offset
42h	Set positive offset 1
43h	Set negative offset 1
44h	Set positive offset 2
45h	Set negative offset 2
46h	Set positive offset 3
47h	Set negative offset 3
48h	Set normal strobe
49h	Set early strobe
4Ah	Set late strobe
4Bh	Increment Slave Data Recovery Level
4Ch	Reset Slave Data Recovery Level
4Dh - 7Fh	Reserved for future use
80h - 8Fh	Slave specific function
90h - FFh	Reserved for future use

7.1.1.1 Reserved for future use (00h-0Fh)

7.1.1.2 Disable Alternate Port (10h) (Dual Port)

This function code causes the slave to disable the Alternate Port, making it Unavailable at the Physical Interface.

7.1.1.3 Enable Alternate Port (11h) (Dual Port)

This function code causes the slave to enable the Alternate Port, thereby making it available at the Physical Interface.

7.1.1.4 Disable Port (12h) (Dual Port)

This function code causes the slave to disable the port over which this function was transferred, making it unavailable. This function takes effect when the master deselects from this port.

7.1.1.5 Reserved for future use (13h)

7.1.1.6 Reserve (14h) (Dual Port)

This function code causes the slave to be reserved to this port. The reserve remains in effect until released, until a Priority Reserve is performed by the alternate port, until a selection octet with the Priority Select bit or the Priority Select and Priority Hold bits set issued by the alternate port, or until the slave is reset with a Slave Reset from either port.

7.1.1.7 Release (15h) (Dual Port)

This function code causes the slave to be released from this port and to enter the Neutral Mode.

7.1.1.8 Notify Alternate Port of Format Completion (16h) (Dual Port)

This function code sets the Format Completed bit in the Status Response for the Alternate Port immediately.

7.1.1.9 Enable Enhanced Mode (17h) (Enhanced Mode)

This function code enables the Enhanced Mode of operation. See 6.10 for detailed description of the Enhanced Mode.

7.1.1.10 Disable successful Command Completion Interrupt (Class 1) attention (18h)

This function code causes the slave to disable the Command Completion Interrupt from asserting ATTENTION IN at this port.

7.1.1.11 Enable successful Command Completion Interrupt (Class 1) attention (19h)

This function code causes the slave to enable the Command Completion Interrupt to assert ATTENTION IN at this port. It is enabled after a power-on Reset or a Slave Reset.

7.1.1.12 Disable RPS or Buffer Available Interrupt (Class 2) attention (1Ah)

This function code causes the slave to disable the RPS or Buffer Available Interrupt from asserting ATTENTION IN at this port.

7.1.1.13 Enable RPS or Buffer Available Interrupt (Class 2) attention (1Bh)

This function code causes the slave to enable the RPS or Buffer Available Interrupt to assert ATTENTION IN at this port. It is enabled after a power-on Reset or a Slave Reset.

7.1.1.14 Disable Status Pending Interrupt (Class 3) attention (1Ch)

This function code causes the slave to disable the Status Pending Interrupt from asserting ATTENTION IN at this port.

7.1.1.15 Enable Status Pending Interrupt (Class 3) attention (1Dh)

This function code causes the slave to enable the Status Pending Interrupt to assert ATTENTION IN at this port. It is enabled after a power-on Reset or a Slave Reset.

7.1.1.16 Disable "No Longer Busy" attention (1Eh)

This function code causes the slave to disable the slave's "No Longer Busy" from asserting ATTENTION IN at this port.

7.1.1.17 Enable "No Longer Busy" attention (1Fh)

This function code causes the slave to enable the slave's "No Longer Busy" to assert ATTENTION IN at this port. It is enabled after a power-on Reset or a Slave Reset.

7.1.1.18 No operation (20h)

This function code performs no operation.

7.1.1.19 Enable Slave ECC Correction (Slave ECC/CRC) (21h)

This function code causes the slave to enable the correction of ECC errors. It is disabled after a Power on Reset or Slave Reset.

7.1.1.20 Spin-up (22h)

This function code causes the slave to spin up.

7.1.1.21 Spin down (23h)

This function code causes the slave to spin down.

7.1.1.22 Load Heads (24h) (Load/Unload Heads)

This function code causes the slave to load its heads.

7.1.1.23 Unload Heads (25h) (Load/Unload Heads)

This function code causes the slave to unload its heads.

7.1.1.24 Lock Carriage (26h) (Lock/Unlock Carriage)

This function code causes the slave to lock the carriage.

7.1.1.25 Unlock Carriage (27h) (Lock/Unlock Carriage)

This function code causes the slave to unlock the carriage.

7.1.1.26 Recalibrate (28h)

This function code shall cause the slave to position to cylinder 0, Head 0.

7.1.1.27 Perform internal diagnostic (29h)

This function code causes the slave to perform its built-in diagnostics.

7.1.1.28 Set Alternate Port Semaphore 0 (2h, bit 0) (2Ah)

This function code causes the slave to set Alternate Port Semaphore 0 Status bit in octet 2h of Status Response.

7.1.1.29 Set Alternate Port Semaphore 1 (2h, bit 1) (2Bh)

This function code causes the slave to set Alternate Port Semaphore Status bit in octet 2h of Status Response.

7.1.1.30 Disable slave ECC/CRC (2Ch) (Slave ECC/CRC)

This function code causes the slave to disable the slave ECC/CRC reporting and the slave ECC correction. The ECC/CRC functions are disabled after a power-on reset.

7.1.1.31 Enable slave ECC/CRC Reporting (2Dh) (Slave ECC/CRC)

This function code causes the slave to enable the reporting of detected ECC/CRC errors.

7.1.1.32 Disable Spindle Sync Reference Source (2Eh) (Spindle Sync)

This function code causes the slave to disable the Spindle Sync Reference Source. It is disabled after a power-on reset or a Slave Reset.

7.1.1.33 Enable Spindle Sync Reference Source (2Fh) (Spindle Sync)

This function code causes the slave to begin transferring its slave Spindle Sync Reference Source.

7.1.1.34 Disable Spindle Sync Transition status (30h) (Spindle Sync)

This function code causes the slave to disable the setting of interrupts with any change in Spindle Sync Transition locked status. It is disabled after a power-on reset or a Slave Reset.

7.1.1.35 Enable Spindle Sync Transition status (31h) (Spindle Sync)

This function code causes the slave to set a Class 3 status pending interrupt with Unsolicited Exception upon any change in the Spindle Sync Transition locked status.

7.1.1.36 Disable Spindle Sync (32h) (Spindle Sync)

This function causes the slave to disable the Spindle Sync at the slave. It is disabled after a power-on reset or a Slave Reset.

7.1.1.37 Enable Spindle Sync (33h) (Spindle Sync)

This function causes the slave to enable the Spindle Sync at the slave.

7.1.1.38 Spindle re-sync (34h) (Spindle Sync)

This function causes the slave to synchronize to the Spindle Sync Reference.

7.1.1.39 Reserved for future use (35h-40h)

7.1.1.40 Reset offset (41h)

This function code clears any head offset. If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.41 Set positive offset 1 (42h)

This function code causes the slave to offset its heads by a minimum value (slave dependent) in the positive direction (away from the spindle). If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.42 Set negative offset 1 (43h)

This function code causes the slave to offset its heads by a minimum value (slave dependent) in the negative direction (towards the spindle). If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.43 Set positive offset 2 (44h)

This function code causes the slave to offset its heads by a value greater than Positive Offset 1 (slave dependent) in the positive direction. If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.44 Set negative offset 2 (45h)

This function code causes the slave to offset its heads by a value greater than Negative Offset 1 (slave dependent) in the negative direction. If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.45 Set positive offset 3 (46h)

This function code causes the slave to offset its heads by a value greater than Positive Offset 2 (slave dependent) in the positive direction. If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.46 Set negative offset 3 (47h)

This function code causes the slave to offset its heads by a value greater than Negative Offset 2 (slave dependent) in the negative direction. If a slave does not support track offsets, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.47 Set normal strobe (48h)

This function code causes the slave to set normal data strobe. If a slave does not support early/late data recovery strobes, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.48 Set early strobe (49h)

This function code causes the slave to set an early data strobe. If a slave does not support early/late data recovery strobes, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.49 Set late strobe (4Ah)

This function code causes the slave to set a late data strobe. If a slave does not support early/late data recovery strobes, it shall respond immediately with Operation Completed bit set in the Slave Status upon receipt of this function code and set bits at Extended Status Response as if completed.

7.1.1.50 Increment Slave Data Recovery Level (4Bh)

This function code causes the slave to set conditions for the next sequential level of data recovery. If a slave does not support this function, it shall respond immediately with operation Completed bit set in the Slave Status. Any active head offset or window strobe that was specifically set by a previous function code (42h-4Ah) is cleared. When the last sequential recovery level supported by the slave is active, transfer of this function code shall cause the slave to activate the first sequential Data Recovery Level.

7.1.1.51 Slave Reset Data Recovery Level (4Ch)

This function code causes the slave to reset any active data recovery level. If a slave does not support this function, it shall respond immediately with Operation Completed bit set in the Slave Status.

7.1.1.52 Reserved for future use (4Dh-7Fh)

7.1.1.53 Slave specific function (80h-8Fh)

These function codes cause a slave-specific function to be performed.

7.1.1.54 Reserved for future use (90h-FFh)

7.1.2 Load Format Specification (02h)

The Load Format Specification command control transfers a Format Specification to the slave. The Format Specification is described in 6.2. The format of the command parameters shall be as follows:

Octet (Hex)	Parameters
0-1	Number of octets following: equals n - 1 (Note)
2-3	Format Type and Flag Octet
4-n	Remainder of Format Specification

Note — n is the octet number of the last octet transferred

If bit 6 of the Flag Octet is set, the Manufacturer's Format Specification is invoked and no more parameters need be supplied by the master.

7.1.3 Load Slave-Specific Information (03h)

The Load Slave-Specific Information command control transfers slave-specific information (e.g., diagnostics) to the slave. The format of the command parameters shall be as follows:

Octet (Hex)	Parameters
0-1	Number of octets following: equals n - 1 (Note)
2-n	Slave-specific information

Note — n is the octet number of the last octet transferred

7.1.4 Load Cylinder Address (04h)

The Load Cylinder Address command control causes the slave to seek to the cylinder specified in the four octets transferred to the slave. If predictive commands are supported, the slave shall also prepare for the data operation specified by the Encoded Data Operation parameter. RPS Interrupts, if enabled, are not set until the slave is on cylinder and prepared to operate on data controls. Any active head offset or data strobe or Data Recovery level is cleared.

For Slaves that do not support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	**7-0**	**Cylinder Address, bits 24-31**
1-3		**Cylinder address, bits 0-23**

For Slaves that support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	7-6	Cylinder Address, bits 30-31 or Encoded Data Operation
	5-0	Cylinder address, bits 24-29
1-3		Cylinder address, bits 0-23

The definition of the Encoded Data Operation (see 6.17) is as follows:

Bit 1	Bit 0	Function
0	0	Default, data operation not specified
0	1	Read **Operation Pending**
1	0	Verify **Operation Pending**
1	1	Write **Operation Pending**

If a slave does not support the Predictive commands feature, the Encoded Data Operation is not used, and the bits occupied by the Encoded Data Operation shall be used as the most significant bits of the Cylinder Address parameter. The Encoded Data Operation remains in effect until one of the following occur:

- A new Encoded Data Operation is transferred from the master;
- Slave Reset;
- Slave Internal Reset;
- Recalibrate function code.

7.1.5 Load Head Address (05h)

The Load Head Address command control causes the slave to select the head specified in the two octets transferred to the slave. If predictive commands are supported, the slave shall also prepare for the data operation specified by the Encoded Data Operation parameter. RPS Interrupts, if enabled, are not set until the slave is on cylinder and prepared to operate on data controls. Any active head offset or data strobe or Slave Data Recovery Level is cleared. The format of the command parameters shall be as follows:

For Slaves that do not support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	**7-0**	**Head Address, bits 8-15**
1		**Head address, bits 0-7**

For Slaves that support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	7-6	Head Address, bits 14-15 or Encoded Data Operation
	5-0	Head address, bits 8-13
1		Head address, bits 0-7

See 7.1.4 for a description of the Encoded Data Operation parameter.

7.1.6 Load Target Address (06h)

This Command Control has a different meaning for the Non-Buffer Mode and the Buffer Mode.

7.1.6.1 Load Target Address (Non-Buffer Mode)

The Load Target Address command control causes the slave to select the physical sector specified by the two octets transferred from the master. If predictive commands are supported, the slave shall also prepare for the data operation specified by the Encoded Data Operation parameter.

The Slave Status and Interrupt following Load Target Address bus control are shown in the following table.

Table 11 — Slave Status and Interrupt Table (Load Target Address)

Target Address	w/ valid Target		w/ Target = all ones or Pulse Width equal zero	
Slave Status (3)	80h	90h	80h	90h
Interrupt to follow (1)	RPS (2)	RPS(2)	-	CCI

NOTES
1 If an asynchronous exception occurs after the transfer of Slave Status and before the Interrupt is set, a status Pending Interrupt (class 3) shall be set.
2 If the slave completes the operation during the rotational time of the defined RPS pulse the RPS interrupt is set for the remaining time of the defined RPS Pulse.
3 If a Logical Reset is transferred to the slave following the setting of the TDO bit, the Slave shall not set the owed interrupt. The completion of the operation by the slave is not defined.

The RPS Interrupt is cleared if the Target Address parameter is equal to all ones or the Pulse Width is equal to zero. The slave shall terminate after the last parameter it supports. If the master chooses not to transfer all the parameters, the master shall be prepared to master-terminate after the last parameter it transfers.

If the RPS parameters are not supplied by the master, the values shall remain at their previous setting. The default value for the RPS Pulse Width is one sector for all zones. If the RPS parameters are supplied by the master, same parameters shall be used across all zones unless they are supplied for each zone.

For Slaves that do not support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	**7-0**	**Target Address, bits 8-15**
1		**Target Address, bits 0-7**
2-3		**Extension**
4-7		**Pulse Width**
8-B		**Skew**

For Slaves that support Predictive Commands the format of the command parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0	7-6	Target Address, bits 14-15 or Encoded Data Operation
	5-0	Target Address, bits 8-13
1		Target Address, bits 0-7
2-3		Extension
4-7		Pulse Width

8-B Skew

See 7.1.4 for a description of the Encoded Data Operation parameter.

7.1.6.1.1 Target Address

This parameter is the address of the physical sector. This physical location shall equal the RPS Pulse unless modified with the other RPS parameters.

The Target Address is set to a value of all ones at power-on Reset or Slave Reset and shall be set to all ones if a Format Specification is accepted by the slave.

7.1.6.1.2 Extension

This parameter specifies the number of sectors that the RPS pulse is extended in the direction ahead of the target and may be transferred in addition to the previous octets to extend the RPS Pulse. If this parameter contains a value of 0000h, then the RPS Pulse defaults to a length of one sector.

If the following Pulse Width parameter is used this parameter acts as a multiplier to produce the total RPS pulse width.

The Extension parameter is set to a value of 0000h after a power-on Reset or a Slave Reset and shall be reset to 0000h if a Format Specification is accepted by the slave.

7.1.6.1.3 Pulse Width

This parameter may be transferred in addition to the previous octets to define the RPS pulse width in octets. When this parameter is transferred the RPS Pulse is equal to:
(Extension + 1) x (Pulse Width).

After a power-on Reset or a Slave Reset, the Pulse Width parameter value is defaulted to the number of octets per sector defined by the Manufacturer's Format specification or the last saved Format Specification if implemented and shall default to the new octets per sector if a Load Format Specification command control is accepted by the slave.

The slave shall accept a Pulse Width parameter of zero value. If the Pulse Width parameter is zero:
- The Pulse Width is zero and RPS (Class 2) interrupt is cleared;
- The slave shall sets a Class 1 interrupt for a Load Position or Load Target Address command, for which the slave Status is transferred with the TDO bit set.

7.1.6.1.4 Skew

This parameter shall define a skew factor for the trailing edge of the RPS Pulse ahead of the trailing edge of the physical sector specified by the Target Address parameter. This skew factor should typically correspond to the master's estimated reconnect time in octets. In the case of large sectors, this allows the master to set the RPS Pulse immediately ahead of the desired sector and to define the number of octets prior to the desired sector the slave shall clear the RPS Pulse. When this parameter is used the master shall define the RPS pulse width in octets.

7.1.6.2 Load Target Address (Buffer Mode)

The Load Target Address command control causes the slave to select physical sector specified by the two octets transferred from the master. This command allows master to switch the slave into the Buffer Mode.

The master shall transfer all the parameters of this command control to the slave as there is no method to read the RPS parameters without disabling the Buffer Mode.

The format of the parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0-1		Target Address
2-3		Encoded Buffer Modes
4-7		Set to zero
8-B		Buffer Available Interrupt Delay

7.1.6.2.1 Target Address

This parameter is the address of the physical sector.

To perform read and write operations from and to the buffer during the Buffer Mode for diagnostic Buffer Mode, Target Address shall be set to FFFFh.

7.1.6.2.2 Encoded Buffer Modes

The Most Significant Octet is equal to FFh and the Least Significant Octet is coded as follows:

Bit	Description
7	1
6	1
5-4	Encoding

Bit 5	Bit 4	Buffer Mode
0	0	Write Buffer Mode
0	1	Verify Buffer Mode
1	0	Read Buffer Mode
1	1	Read Immediate Buffer Mode

3	Buffer Across Cylinder Boundaries Attribute
2	Continue on ECC error
1	Continue on Missed Sync Byte
0	Continue on Verify Miscompare

The following Buffer Modes are only considered as valid Buffer Modes.

Octet	Description
FFC0h	Write Buffer Mode, Stop on Exception
FFC8h	Write Buffer Mode, Stop on Exception, Buffer Across Cylinder Boundaries
FFD0h	Verify Buffer Mode, Stop on Exception
FFD1h	Verify Buffer Mode, Continue on verify Miscompare
FFD2h	Verify Buffer Mode, Continue on Missed Sync Byte
FFD3h	Verify Buffer Mode, Continue on Verify Miscompare or Missed Sync Byte
FFD4h	Verify Buffer Mode, Continue on ECC Error
FFD5h	Verify Buffer Mode, Continue on Verify Miscompare or ECC Error
FFD6h	Verify Buffer Mode, Continue on Missed Sync Byte or ECC Error
FFD7h	Verify Buffer Mode, Continue on Missed Sync Byte or ECC Error or Verify Miscompare
FFD8h | FFDFh	Same as above but with Buffer Across Cylinder Boundaries enabled
FFE0h	Read Buffer Mode, Stop on Exception
FFE2h	Read Buffer Mode, Continue on Missed Sync Byte
FFE4h	Read Buffer Mode, Continue on ECC error
FFE6h	Read Buffer Mode, Continue on Missed Sync Byte or ECC error
FFE8h	Read Buffer Mode, Stop on Exception, Buffer Across Cylinder Boundaries
FFEAh	Read Buffer Mode, Continue on Missed Sync Byte, Buffer Across Cylinder Boundaries
FFECh	Read Buffer Mode, Continue on ECC error, Buffer Across Cylinder Boundaries
FFEEh	Read Buffer Mode, Continue on Missed Sync Byte or ECC error, Buffer Across Cylinder Boundaries

FFF0h	Read Immediate Buffer Mode, Stop on Exception
FFF2h	Read Immediate Buffer Mode, Continue on Missed Sync Byte
FFF4h	Read Immediate Buffer Mode, Continue on ECC error
FFF6h	Read Immediate Buffer Mode, Continue on Missed Sync Byte or ECC error
FFF8h	Read Immediate Buffer Mode, Stop on Exception, Buffer Across Cylinder Boundaries
FFFAh	Read Immediate Buffer Mode, Continue on Missed Sync Byte, Buffer Across Cylinder Boundaries
FFFCh	Read Immediate Buffer Mode, Continue on ECC error, Buffer Across Cylinder Boundaries
FFFEh	Read Immediate Buffer Mode, Continue on Missed Sync Byte or ECC error, Buffer Across Cylinder Boundaries

If the buffer operation is indicated by setting any of the above modes and the Sector Address is set to FFFFh, the slave shall enable buffer diagnostic mode. The purpose of the buffer diagnostic mode is to support write data patterns into the buffer and read data from the buffer for buffer verification. During buffer diagnostic mode, the slave sets Buffer Available Interrupt (Class 2) so data can be transferred regardless of buffer empty or full status.

The Extension parameter value for the Non-Buffer Mode is saved before setting the value for the Buffer Mode. After leaving the Buffer Mode, the saved extension parameter value is restored for the Non-Buffer Mode.

7.1.6.2.3 Buffer Available Interrupt Delay

This parameter is defined in sectors. This parameter shall be used as the Class 2 Buffer Available Interrupt delay in sectors for the partially full buffer during read and the partially empty buffer during write. The Master may multiplex data transfers between multiple drives by managing the Class 2 Buffer Available Interrupt delay. Setting this parameter as FF..FFh disables Buffer Available Interrupt Delay.

The Skew parameter value for the Non-Buffer Mode is saved by the slave before setting the value for the Buffer mode. After leaving the Buffer Mode, the saved Skew parameter value is restored for the Non-Buffer Mode.

7.1.7 Load Position (07h)

This command control has a different meaning for the Non-Buffer Mode and the Buffer Mode.

7.1.7.1 Load Position (Non-Buffer Mode)

The Load Position command control causes the slave to seek to the physical cylinder specified by the Cylinder Address parameter, select the physical head specified by the Head Address parameter and select the physical sector specified by the Target Address. If the Predictive Commands feature is supported, the slave shall also prepare for the data operation specified by the Encoded Data Operation parameter. RPS Interrupts, if enabled, are not set until the slave is on cylinder and the specified head has been selected. Any active head offset, data strobe or Data Recovery Level is cleared.
The Slave Status of this command normally completes with the Time Dependent-bit set in the slave status. However if the command is already complete at Slave Status time, TDO need not be set. If the TDO bit is set and a valid Target Address other than all ones is accepted, the Command Completion Interrupt is not set but an RPS Interrupt is set.

If a data control transferred does not agree with the Encoded Data Operation specified in the previous Load Position command, the slave may reject the data control and set Out of Context.

The Slave Status and Interrupt following Load Position bus control are shown in the following table.

Table 12 — Slave Status and Interrupt Table (Load Position)

Actuator movement	motion	motion	no motion		no motion	
Target Address	with valid Target	with Target = all ones or zero Pulse Width	with valid Target		with Target = all ones	
Slave Status (note 4)	90h	90h	80h	90h	90h	90h
Interrupt to follow (note 1)	RPS (note 2)	CCI	RPS (note 3)	RPS (note 2)		CCI

NOTES
1 If an asynchronous exception occurs after the transfer of Slave Status and before the Interrupt is set, a status Pending Interrupt (class 3) shall be set.
2 If the slave completes the operation during rotational time of the defined RPS Pulse, an RPS interrupt is set for the remaining time of the defined RPS pulse.
3 If the slave completes the operation during the rotational time of the defined RPS Pulse, the TDO bit is not set at the Slave Status and the RPS interrupt is set for the remaining time of the defined RPS Pulse.
4 If a logical reset is transferred to the slave following the setting of the TDO bit, the slave shall not set owed interrupt. The completion of the operation by the slave is not defined.

If the master chooses not to transfer all the parameter, the master shall be prepared to master-terminate after the last parameter it transfers.

For slaves that do not support predictive commands the format of the command parameters for Non-Buffer Mode shall be as follows:

Octet (Hex)	Bit	Parameter
0	7-0	Cylinder Address, bits 24-31
1-3		Cylinder Address, bits 0-23
4	7-6	Zero
	5-0	Head Address, bits 8-13
5		Head Address, bits 0-7
6	7-6	Zero
	5-0	Target Address, bits 8-13
7		Target Address, bits 0-7
8-9		Extension
A-D		Pulse Width
E-11		Skew

For slaves that support predictive commands the format of the command parameters for Non-Buffer Mode shall be as follows:

Octet (Hex)	Bit	Parameter
0	7-6	Encoded Data Operation
	5-0	Cylinder Address, bits 24-29
1-3		Cylinder Address, bits 0-23
4	7-6	Zero
	5-0	Head Address, bits 8-13
5		Head Address, bits 0-7
6	7-6	Zero
	5-0	Target Address, bits 8-13
7		Target Address, bits 0-7
8-9		Extension
A-D		Pulse Width
E-11		Skew

See 7.1.4 for a description of the Encoded Data Operation parameter. See 7.1.6.1.1 - 7.1.6.1.4 for a description of the RPS parameters.

7.1.7.2 Load Position (Buffer Mode)

The Load Position command control causes the slave to seek to the physical cylinder specified by the Cylinder Address parameter, select the physical head specified by the Head Address parameter and select the physical sector specified by the Target Address. If the Predictive Commands feature is supported, the Encoded Data Operation field shall be set to default value (00b) as Buffer Mode provides equivalent information to the slave.

Any active head offset, data strobe or Data Recovery Level is not cleared if the Encoded Buffer Mode is set for Read Buffer Mode and Cylinder and Head Addresses are equal to the previous values. This allows the use of the buffer for data recovery reads.

The master should transfer all the parameters as there is no method to read the RPS parameters without disabling the Buffer Mode. The format of the parameters shall be as follows:

Octet (Hex)	Bit	Parameter
0-3		Cylinder Address
4-5		Head Address

See 7.1.6.2 for a description of the following parameters.

6-7		Target Address
8-9		Encoded Buffer Modes
A-D		Set to zero
E-11		Buffer Available Interrupt Delay

7.1.8 Load Target Modifier (08h)

The Load Target Modifier command control enables the step control modification which causes the slave to modify the target sector address and set a Class 2 interrupt at the RPS pulse following a data control with the step head control bit set. **This command is valid only in non-buffered mode. The slave will reject this command as Out of Context if issued while the slave is operating in buffered mode.**

The format of the command parameter shall be as follows:

Octet (Hex)	Parameter
0-1	Target Modifier

See 6.21 for detailed information on Target Modifier feature.

7.1.9 Load Index Offset (09h)

This command causes a slave which supports spindle sync offset capability to set its index to a specific offset angular delay. The two octet value sent with the command delays the position of the slaves' index relative to the master sync reference signal. This value shall be from 0 to 65535 (0000h to FFFFh). If this value is set to 0000h, there is no offset (i.e. index of the slave shall remain locked to the master sync reference). If the value is set to FFFFh, the offset delay is 1 LSB less **than a full revolution, where LSB is the offset resolution supported by the slave.**
If the slave cannot support an accuracy of 16 bits (1/65536 of a revolution) then the slave need only use those upper bits of the value that it can support to maintain the highest possible accuracy. For example, if a device capable of handling an accuracy of 8 bits (1/256 of a revolution) is sent a value of F000h, then by using the uppermost bits it attempts to locate to F0h. The accuracy is very close (less than 1%) as F000h/FFFFh = 0,9375 and F0h/FFh = 0,941.

At power on Load Index Offset value is set to 0000h. The format of the command parameter is:

Octet (Hex)	Parameter
0-1	Index Offset

7.1.10 Load Port Control (0Ah)

This command causes the slave to disable the effect of an active allegiance at the Alternate Port.

When the Explicit (Reserve) allegiance and the Implicit (Selection) allegiance are not active at the alternate port, interrupts shall be reported.

After a Power-On Reset or Slave Reset, an active Explicit (Reserve) allegiance or an active Implicit (Selection) allegiance at the alternate port shall disable the reporting of interrupts.

The Load Port Control command disables the effect of an active allegiance at the Alternate Port. The result is that the active allegiance at the alternate port shall not effect the reporting of the interrupt.

A bit set to one for an interrupt in Load Port Control, indicates to the slave to disable the effect of the active allegiance at the Alternate Port and report the interrupt.

The format of the command parameters shall be as follows:

Octet (Hex)	Bit	Definition
0		Disable the effect of the Explicit Allegiance and report the interrupt.
	7	Reserved, set to 0
	6	Reserved, set to 0
	5	Reserved, set to 0
	4	Reserved, set to 0
	3	Reserved, set to 0
	2	Report Class 3 Interrupt
	1	Report Class 2 Interrupt
	0	Report Class 1 Interrupt

Octet (Hex)	Bit	Definition
1		Disable the effect of the Implicit Allegiance and report the interrupt.
	7	Reserved, set to 0
	6	Reserved, set to 0
	5	Reserved, set to 0
	4	Reserved, set to 0
	3	Reserved, set to 0
	2	Report Class 3 Interrupt
	1	Report Class 2 Interrupt
	0	Report Class 1 Interrupt

7.1.11 Load End of Write (0Bh)

The Load End of Write command **shall** be transferred during Write Buffer Mode as the last command control and indicates to the slave that all data transfers have been completed from the master. **The slave shall reject any bus control sent by the master that is out of context between the time that Write Buffer Mode is set and when the Load End of Write command is sent. The Load End of Write command causes the slave to finish the write operation, perform any required internal house keeping and to exit Write Buffer Mode.**

No information is transferred with the Load End of Write command.

The Slave Status of this command normally completes with the Time-Dependent Operation bit set. However if write to media operation is already complete at slave status time, TDO need not be set.

7.1.12 Load Buffer Control (0Ch)

The slave shall set Bus Control Context in the Slave Status if the Format Specification is not initialized before this command is transferred.

This command transfers Buffer Control parameters. The master must initialize the Format Specification before transferring this command. If the master transfers this command and the Format Specification is not initialized, the slave shall set Bus Control Context in the Slave Status. The **Load** Buffer Control **data is not initialized when the slave is powered on, unless the slave has implemented the option to save the Last Format Specification.**

The Load Buffer Control command has the following parameter organization:

Octet (Hex)	Bit	Definition	
0h-1h		Number of octets following: equals n - 1 (Note 1)	
2h		reserved, set to 0	
3h		Flag and Attribute octet	
	7	Buffer Control Initialized	
	6	reserved, set to 0	
	5	reserved, set to 0	
	4	reserved, set to 0	
	3	reserved, set to 0	
	2	reserved, set to 0	
	1	reserved, set to 0	
	0	Full Sector Transfer Attribute	
4h-5h		Interface Transfer Rate (100 Kbytes/sec Increments)	
6h-7h		Inter-field Delay Time (50ns increments)	
8h-9h		Buffer Size (Sectors)	
Ah-Bh		Buffer Exception Maximum Count	
Ch-Fh		Address of Last Buffer Operation Cylinder	
10h-11h		Buffer Retry Count	
		ZONE DESCRIPTOR (Note 2, Note 3, Note 4)	
0h:1h		Zone Number z	
2h:3h		Track Sector Offset	Zone z
4h:5h		Cylinder Sector Offset	Zone z
6h:7h		Zone Sector Offset	Zone z

NOTES
1 n is the octet number of the last octet transferred.
2 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.
3 Parameters in the ZONE DESCRIPTOR are repeated as specified by the value in the Number of Zones.
4 Number of Zones is equal to the last Zone Number plus 1. Zones are numbered starting from zero. The number of Zones value is located in the initialized Format Specification.

7.1.12.1 Number of octets following (0h-01h)

This parameter contains octet count for Load Buffer Control command. It does not include itself in the octet count. See Termination of Transfers (5.1.3)

7.1.12.2 Reserved, set to zero (2h)

7.1.12.3 Flag and Attribute Octet (3h)

This parameter contains the flag and attribute information for the Buffer Control command.

7.1.12.3.1 Buffer Control Initialized (3h, bit 7)

This bit shall be set by the slave on the acceptance of the Load Buffer Control command and it shall be cleared by the slave during the Format Specification initialization. At power on this bit shall be set to zero unless the slave has implemented the option to save the **Last Format Specification.**

7.1.12.3.2 Reserved, set to zero (3h, bits 6-1)

7.1.12.3.3 Full Sector Transfer Attribute (3h, bit 0)

If ECC/CRC is enabled at the Format Specification, the Full Sector Transfer Attribute shall be set by the master in the Load Buffer Control Command.
This bit shall be set by the master if the Full Sector Transfer **mode of operation** is desired:

1. Full sector write during the Write Buffer Mode,
2. Full sector write during the Verify Buffer Mode, and
3. Full sector transfer from the buffer during the Read Buffer Mode.

If this bit is set and the master attempts transfer of data from the buffer before a full sector is in the buffer, the slave shall set busy in the Slave Status.

7.1.12.4 Interface Transfer Rate (4h-5h)

This parameter contains the Interface Transfer Rate in 100 kbytes/sec increments in the Buffer Mode. If the slave cannot support this transfer rate, then the slave shall change to the closest possible transfer rate (no greater than the specified maximum transfer rate) and transfer this value in the Read Buffer Control response. The master may set this value equal to FF..FFh to determine the highest transfer rate supported by the slave.

7.1.12.5 Inter-field Delay Time (6h-7h)

This parameter contains the Inter-field Delay Time in 50 ns increments. The **Inter-field Delay time may be used by the master to delay the sync-in pulses, between fields in a sector, to allow time for the master to make decisions.** If the master catches up with buffer during the Read Buffer Mode, then the Inter-field Delay Time shall be equal to the larger value **of the** drive gap time **or the Inter-field delay** time. See the following Figure for the position of the Inter-field Delay relative to a field. This time shall be less than the inter-field delays conditioned for the Non-Buffer Mode.

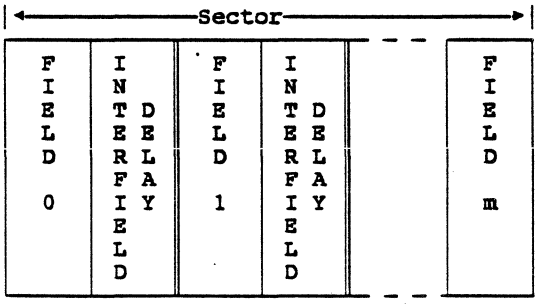


Figure 6 — Sector Transfer Format (Buffer Mode)

7.1.12.6 Buffer Size (8h-9h)

This parameter sets the size of buffer in units of sectors. The value may be set less than or equal to the capacity of the buffer. This parameter may be set to FFFFh (see 6.2.1.2). If it is set FFFFh, the slave calculates the value of buffer size based on the sector size defined by the initialized Format Specification.

7.1.12.7 Buffer Exception Maximum Count (Ah-Bh)

This parameter contains the Buffer Exception Maximum Count. This parameter is used when the slave is operating in one of the following Continue on Exception modes:

1. Continue with Missed Sync Byte
2. Continue with Verify Miscompare
3. Continue with Missed Sync Byte or Verify Miscompare
4. Continue on ECC error
5. Continue with Sync Byte or ECC error

During the Verify Buffer Mode, this count decrements with **each** miscompare or Missed Sync Byte during the verification of **the** Header. During the Read Buffer Mode or Read Immediate Buffer Mode, this count decrements with **each** Missed Sync Byte **or ECC error** at any field of occurrence. When the Buffer Exception **Maximum** Count equals zero, the slave disables the Buffer Mode and reports Buffer Operation Exception error with Buffer Exception Maximum Count and Buffer Operation Sync Byte or Buffer Operation Verify miscompare or Buffer Operation Uncorrectable ECC error set in the Status Response. **Values of 0..0h's or F..Fh's are not valid** for this parameter **and shall cause the Load Buffer Control command to be rejected. This parameter defaults to 1 after power on or Slave Reset unless the slave implements the option to save the last loaded format specification.**

7.1.12.8 Address of Last Buffer Operation Cylinder (Ch-Fh)

This parameter sets the last cylinder that is operated on the slave when the Buffer Across Cylinder Boundaries Attribute is set at the Load Buffer Control flag and attribute octet. The slave shall disable read from media or write to media when the End of Cylinder is detected. **This parameter defaults to zero unless the slaves implements the option to save the last loaded Format Specification.**

7.1.12.9 Buffer Retry Count

This parameter controls the number of times the slave will retry an operation exception condition caused by a media related error, **during Write or Verify Buffer mode,** before reporting operation exception. The slave will accept any value for this parameter but may reset this value to 0 if it does not support internal **retries.** This parameter is valid only if the Full Sector Transfer attribute is set. When this value is non-zero the slave will retry sync byte errors, **verify header miscompares, and uncorrectable ECC errors during** verify/writes. Errors are **retried** immediately when Stop on Exception is set. Errors are **retried** after the Buffer Exception Maximum count is reached when Continue On Exception is set.

7.1.12.10 Track Sector Offset (sectors)

This parameter contains the offset of the starting sector of the track from last sector of previous track in sectors. This parameter is repeated for each zone. **The default value for this parameter is 0 and the maximum allowed value is less than or equal to the number of sectors per track as defined in the Format Specification.** See Sector Order Management (6.13.8) for details.

7.1.12.11 Cylinder Sector Offset (sectors)

This parameter contains the offset of the starting sector of head 0 in sectors from Index. **The default value for this parameter is 0 and the maximum allowed value is less than or equal to the number of sectors per track as defined in the Format Specification.** See Sector Order Management (6.13.8) for details.

7.1.12.12 Zone Sector Offset (sectors)

This parameter contains the offset of the starting sector of head 0, of the first cylinder in a zone, in sectors from Index. This parameter is repeated for every zone. **The default value for this parameter is 0 and the maximum allowed value is less than or equal to the number of sectors per track as defined in the Format Specification.** See Sector Order Management (6.13.8) for details.

7.1.13 Load Cylinder Slip table (0Dh)

Load Cylinder Slip table command control causes the master to transfer Cylinder Slip table to the slave and it has the following parameter organization:

Octet (Hex)	Bit	Definition
0h-1h		Number of octets following: equals n - 1 (Note 1)
		ENTRY DESCRIPTOR (Note 2)
0h-3h		Cylinder Slip entry, entry number [(n-1)/4]

NOTES
1 n is the octet number of last octet transferred.
2 Entry Descriptor repeats (n-1)/4 times, where (n-1)/4 is the total number of entries for Cylinder Slip table.

7.1.13.1 Number of octets following (0h-1h)

This parameter contains the number of octets to follow. It does not include itself in the octet count. This value is used by the slave to control the length of transfer. This value shall not exceed the value of Cylinder Slip table size parameter in the Read Disk Specification.

7.1.13.2 Cylinder Slip Entry, Entry number [(n-1)/4]

This parameter contains address of defective cylinder and it repeats (n-1)/4 times to provide addresses of all defective cylinders. The value of (n-1)/4 is less than or equal to Cylinder Slip table size parameter in Read Disk Specification. The master may transfer FF..FFh for unused location in the Cylinder Slip table. Any Cylinder Address entry with FF..FFh indicates end of valid Cylinder Slip table entry. At power on the first entry in the Cylinder Slip table shall be set to FF..FFh.

7.1.14 Modify Buffer Available Interrupt Delay (0Eh)

Modify Buffer Available Interrupt Delay command control provides a means to the master to modify the Buffer Available Interrupt in the Buffer Mode operation.

The format for this transfer shall be as follows:

Octet (Hex)	Bit	Parameters
0-3		Buffer Available Interrupt Delay

This command shall only be accepted while the slave is in a Buffer Mode. This command shall not complete with the TDO bit set in Slave Status. Setting this parameter equal to FF..FFh clears the Buffer Available Interrupt but does not affect the Buffer Mode.

If this command is transferred prior to initiating a buffer transfer or after the buffer operation has been disabled, the slave rejects this command and sets the Bus Control Context in the Status Response.

7.1.15 Read Configuration (41h)

The Read Configuration control causes the slave to transfer configuration information to the master.

The format for this transfer shall be as follows:

Octet (Hex)	Bit	Parameters
0-1		Number of octets following: equals n-1 (Note)
2		Device class code 3 = Enhanced Disk
3		Slave Type Flag
	7	Non-removable disk
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Moving head disk
	2	Solid State Disk
	1	Reserved, set to zero
	0	Reserved, set to zero
4-B		Manufacturer Identification (ISO 646/ASCII)
C-13		Manufacturer model number (ISO 646/ASCII)
14-17		Manufacturer revision number (ISO 646/ASCII)
18-1F		Manufacturer unique unit ID (ISO 646/ASCII)
20		Features:
	7	Load/Unload Heads
	6	Lock/Unlock Carriage
	5	Zoned Disk Drive
	4	Parallel Heads
	3	Reserved, set to zero
	2	Fixed Block Mode, Sector Mode 2/Sector Mode 1
	1	Reserved, set to zero
	0	Reserved, set to zero
21		Features:
	7	Buffer
	6	Buffer Mode Only
	5	Modify Buffer Available Interrupt Delay
	4	Predictive Commands
	3	Field Data Controls
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Reserved, set to zero
22		Features:
	7	Spindle Sync
	6	Local Spindle Sync
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Reserved, set to zero

23 Features:
- 7 Reserved, set to zero
- 6 Target Modifier
- 5 Slave ECC/CRC
- 4 Reserved, set to zero
- 3 Slave responds to adjacent odd-even select addresses for dual actuators
- 2 Reserved, set to zero
- 1 Slave restores last loaded Format Specification, Load Buffer Control & Cylinder Slip Table
- **0 Reserved, set to zero**

24 Features:
- 7 Reserved, set to zero
- 6 Reserved, set to zero
- 5 Reserved, set to zero
- 4 Reserved, set to zero
- 3 Reserved, set to zero
- 2 Reserved, set to zero
- 1 Reserved, set to zero
- 0 Reserved, set to zero

25 Features:
- 7 Reserved, set to zero
- 6 Reserved, set to zero
- 5 Reserved, set to zero
- 4 Dual Port
- 3 Reserved, set to zero
- 2 Reserved, set to zero
- 1 Reserved, set to zero
- 0 Port Control

26 Supported Interleave:
- 7 32 bit interleave supported
- 6 31 bit interleave supported
- 5 30 bit interleave supported
- 4 29 bit interleave supported
- 3 28 bit interleave supported
- 2 27 bit interleave supported
- 1 26 bit interleave supported
- 0 25 bit interleave supported

27 Supported Interleave:
- 7 24 bit interleave supported
- 6 23 bit interleave supported
- 5 22 bit interleave supported
- 4 21 bit interleave supported
- 3 20 bit interleave supported
- 2 19 bit interleave supported
- 1 18 bit interleave supported
- 0 17 bit interleave supported

28 Supported Interleave:
- 7 16 bit interleave supported
- 6 15 bit interleave supported
- 5 14 bit interleave supported
- 4 13 bit interleave supported
- 3 12 bit interleave supported
- 2 11 bit interleave supported
- 1 10 bit interleave supported
- 0 9 bit interleave supported

29 Supported Interleave:

7	8 bit interleave supported
6	7 bit interleave supported
5	6 bit interleave supported
4	5 bit interleave supported
3	4 bit interleave supported
2	3 bit interleave supported
1	2 bit interleave supported
0	1 bit interleave supported

2A-2B	Manufacturer switch settings
2C-2D	Number of Slave Data Recovery Levels
2E-n	Manufacturer's defined parameters

Note — n is the octet number of the last octet transferred.

7.1.15.1 Number of octets following (0h-1h)

This parameter contains the octet count for the Configuration Response. It does not include itself in the octet count.

7.1.15.2 Device class code (2h)

This parameter contains the device class code. This international standard defines Device Class Code 3 as Enhanced Disk.

7.1.15.3 Slave type flag code (3h)

This parameter contains the slave type flag code. This parameter indicates whether the slave contains non-removable media or moving heads. This parameter also indicates if the Slave is a Solid State Disk. **The Flag bits are defined as follows:**

7.1.15.3.1 Non-removable disk (bit 7)

This bit indicates that the slave contains non-removable media.

7.1.15.3.2 Reserved, set to zero (bits 6-4)

7.1.15.3.3 Moving head disk (bit 3)

This bit indicates that the slave has movable heads, as opposed to fixed heads.

7.1.15.3.4 Solid state disk (bit 2)

This bit indicates that the slave contains solid state memory for storage of data. The master may need to alter its operation to make best use of the reduced latencies of solid state memory.

7.1.15.3.5 Reserved, set to zero (bits 1-0)

7.1.15.4 Manufacturer identification (4h-Bh)

This parameter contains the slave manufacturer's identification in ISO 646 (ASCII).

7.1.15.5 Manufacturer model number (Ch-13h)

This parameter contains the slave model number in ISO 646 (ASCII).

7.1.15.6 Manufacturer revision number (14h-17h)

This parameter contains the slave revision number in ISO 646 (ASCII).

7.1.15.7 Manufacturer unique unit ID (18h-1Fh)

This parameter contains the unit identification for the slave in ISO 646 (ASCII). The unit ID for each slave, which is provided by the manufacturer, shall either be different from the unit ID for any other slave of the same manufacturer, model, and revision number. If this parameter is not supported, it is set to all zeros.

7.1.15.8 Features (20h)

This parameter contains the device enclosure features.

7.1.15.8.1 Load/Unload Heads (Bit 7)

This bit indicates that the slave supports Load/Unload Heads feature. Function code 24h causes the slave to load its heads and function code 25h causes slave to unload its heads.

7.1.15.8.2 Lock/Unlock Carriage (Bit 6)

This bit indicates that the slave supports Lock/Unlock Carriage feature. Function code 26h causes the slave to lock the carriage and function code 27h causes slave to unlock the carriage.

7.1.15.8.3 Zoned Disk Drive (Bit 5)

This bit indicates that the slave supports Zoned Disk Drive feature. See 6.16 for detailed information on this feature.

7.1.15.8.4 Parallel Heads (Bit 4)

This bit indicates that the slave supports Parallel Heads feature. See 6.12 for detailed information on this feature.

7.1.15.8.5 Reserved, set to zero (Bit 3)

7.1.15.8.6 Fixed Block Mode, Sector Mode 2/Sector Mode 1 (Bit 2)

If this bit is set, it indicates that the slave supports the Fixed Block Mode, Sector Mode 2 feature where every sector is of the same length and organization but length and organization is programmable.

If this bit is not set, it indicates that the slave supports the Fixed Block Mode, Sector Mode 1 feature where every sector is of the same length and organization, which is fixed by the slave.

7.1.15.8.7 Reserved, set to zero (Bits 1-0)

7.1.15.9 Features (21h)

This parameter contains the slave read/write data controls features.

7.1.15.9.1 Buffer (Bit 7)

This bit indicates that the slave supports the Buffer Mode feature. See 6.13 for detailed information on this feature.

7.1.15.9.2 Buffer Mode Only (Bit 6)

This bit indicates that the slave supports the Buffer Mode Only feature. See 6.14 for detailed information on this feature.

7.1.15.9.3 Modify Buffer Available Interrupt Delay (Bit 5)

This bit indicates that the slave supports Modify Buffer Available Interrupt Delay sub-feature of Buffer Mode. See 6.15 for detailed information on this sub-feature.

7.1.15.9.4 Predictive Commands (Bit 4)

This bit indicates that the slave supports the Predictive Commands feature. See 6.20 for detailed information on this feature.

7.1.15.9.5 Field Data Controls (Bit 3)

This bit indicates that the slave supports the Field Data Controls in the Non-Buffer Mode. In Buffer Mode, the slave supports only Sector Data Controls.

7.1.15.9.6 Reserved, set to zero (Bits 2-0)

7.1.15.10 Features (Octet 22h)

This parameter contains the slave features.

7.1.15.10.1 Spindle Sync (Bit 7)

This bit indicates that the slave supports Spindle Sync feature. See 6.11 for detailed information on this feature.

7.1.15.10.2 Local Spindle Sync Mode (Bit 6)

This bit indicates that the slave provides a mechanism (switches or jumpers) to control the Spindle Sync feature. See 6.11 for detailed information on this feature.

7.1.15.10.3 Reserved, set to zero (Bits 5-0)

7.1.15.11 Features (23h)

This parameter contains the slave features.

7.1.15.11.1 Reserved,set to zero (Bit 7)

7.1.15.11.2 Target Modifier (Bit 6)

This bit indicates that the slave supports Target Modifier feature. See 6.21 for detailed information on this feature.

7.1.15.11.3 Slave ECC/CRC (Bit 5)

This bit indicates that the slave supports Slave ECC/CRC feature. See 6.8 for detailed information on this feature.

7.1.15.11.4 Reserved, set to zero (Bit 4)

7.1.15.11.5 Slave responds to adjacent odd-even select address for dual actuators (Bit 3)

This bit indicates that the slave supports this feature and responds to adjacent odd-even select address for dual actuators.

7.1.15.11.6 Reserved, set to zero (Bit 2)

7.1.15.11.7 Slave restores last loaded Format Data (Bit 1)

This bit indicates that the slave supports this feature and restores the last loaded Format Specification **the last loaded Load Buffer Control command data and the last loaded Cylinder Slip table. Only the last loaded Format Specification is saved in slaves that do not support the buffered mode of operation.**

7.1.15.11.8 Reserved, set to zero (Bit 0)

7.1.15.12 Features (24h)

Reserved, set to zero

7.1.15.13 Features (25h)

This parameter contains the slave features.

7.1.15.13.1 Reserved, set to zero (Bits 7-5)

7.1.15.13.2 Dual Port (Bit 4)

This bit indicates that the slave supports Dual Port feature. See 6.19 for detailed information on this feature.

7.1.15.13.3 Reserved, set to zero (Bits 3-1)

7.1.15.13.4 Port Control (Bit 0)

This bit indicates that the slave supports Port Control feature. The slave must support Dual Port in order to provide this feature. See 6.20 for detailed information on this feature.

7.1.15.14 Supported interleave (26h-29h)

This parameter contains all supported interleaves for parallel head operation.

7.1.15.15 Manufacturer switch settings (2Ah-2Bh)

This parameter contains the value of any switch settings the slave reports via the Configuration Response.

7.1.15.16 Number of Slave Data Recovery Procedure Levels (2Ch-2Dh)

This parameter contains the number of levels of Slave Data Recovery supported by the slave. If a slave does not support this function, the parameter shall be set to zero.

7.1.15.17 Manufacturer defined parameter (2Eh-n)

This parameter contains the manufacturer's defined values.

7.1.16 Read Format Specification (42h)

The Read Format Specification response control causes the slave to transfer the current Format Specification to the master (see 6.2 for a description of the Format Specification). The response shall have the following format:

Octet (Hex)	Parameters
0-1	Number of octets following: equals n - 1 (Note)
2-3	Format Type and Flag Octet
4-n	Remainder of Format Specification

Note — n is the octet number of the last octet transferred.

A Format Specification with the Initialized bit cleared indicates the slave hardware is not capable of accepting data controls.

7.1.17 Read Slave Specific Information (43h)

The Read Slave Specific Information response control causes the slave to transfer slave-specific information (e.g., diagnostics) to the master. The response shall have the following format:

Octet (Hex)	Parameters
0-1	Number of octets following: equals n - 1 (Note)
2-n	Slave-specific information

Note — n is the octet number of the last octet transferred.

7.1.18 Read Status (44h)

The Read Status Response Control instructs the slave to transfer up to 24 octets of status to the master with the following response format:

Octet (Hex)	Contents
0-1	Exception Status
2-5	Unsolicited Exception Status
6-7	Bus Control/Parameter Exception Status
8-B	Slave Exception Status
C-D	Buffer Exception Status
E-F	Buffer Exception Status - Residual Count
10-17	Vendor Unique Status

See 8.2 for detailed definition of the Status Response. The slave may terminate the transfer Sequence when the remaining octets are zeros.

7.1.19 Read Correction Vectors (45h)

The Read Correction Vectors response control causes the slave to transfer the ECC correction vectors to the master. If the slave ECC/CRC feature is not implemented, this control shall be rejected as unsupported. The format of the response shall be as follows:

Octet (Hex)	Parameters
0-1	The number of octets following: equals n - 1 (Note 1) VECTOR DESCRIPTOR (Note 2 and Note 3)
0h	Correction octet
1h:3h	Error octet location from start of last field transferred

Notes
1 n is octet number of the last octet transferred.
2 Vector Descriptor repeats for every vector.
3 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.

The exclusive-OR operation of the correction octet and the data octet at the specified location may be performed by the master.

7.1.19.1 The number of octets following (00h-01h)

This parameter contains the octet count for the Read Correction Vectors. It does not include itself in the octet count. This parameter shall equal zero if the slave status of the previous data control has set a Data Exception, ECC error.

7.1.19.2 Correction Octet

This parameter specifies the Error Pattern for the Error and it is repeated for each Vector.

7.1.19.3 Error Octet location from start of last field transferred

This parameter specifies the location of the Error from the start of the last field transferred and it is repeated for each Vector.

7.1.20 Read Current Sector Address (46h)

The Read Current Sector Address response control causes the slave to transfer the current physical sector to the master. The encoded data operation shall reflect the specific data operation the slave is prepared to perform (if any). The response shall have the following format:

Octet (Hex)	bit	Parameter
0	7-6	Current Sector Address, bits 14-15 or Encoded Data Operation
	5-0	Current Sector Address, bits 8-13
1		Current Sector Address, bits 0-7

See 7.1.4 for description of Encoded Data Operation.

If the slave cannot determine the Current Sector Address, the Current Sector Address is all ones. The Current Sector Address transferred by the master may differ from actual physical sector location because of the time required to transfer the response.

7.1.21 Read Current Position (47h)

The Read Current Position response control causes the slave to transfer the current position to the master. The Encoded Data Operation field shall reflect the specific data operation the slave conditioned to perform (if any).

The response shall have the following format when predictive commands are not supported.

Octet (Hex)	Bit	Parameters
0-3		Cylinder address
4-5		Head address
6-7		RPS Target Sector address
8-9		Current Sector address

The response shall have the following format when predictive commands are supported.

Octet (Hex)	Bit	Parameters
0	7-6	Encoded data operation
	5-0	Cylinder Address, bits 24-29
1-3		Cylinder Address, bits 0-23
4	7-6	Zero
	5-0	Head Address, bits 8-13
5		Head Address, bits 0-7
6	7-6	Zero
	5-0	Target address, bits 8-13
7		Target address, bit 0-7
8	7-6	Zero
	5-0	Current sector address, bits 8-13.
9		Current Sector Address, bits 0-7

See 7.1.4 for description of Encoded Data Operation.

When leaving Buffer Mode, the last sector position accessed in Buffer Mode should be reported.

If the RPS Interrupt is disabled, the Current Target Address shall be set to all ones. If the slave cannot determine the Current Sector Address, the Current Sector Address shall be set to all ones. The Current Sector Address transferred to the master may differ from the actual physical sector because of the time required to transfer the response.

7.1.22 Read Extended Status (48h)

The Read Extended Status response control causes the slave to transfer up to 20 octets of status to the master. The format of the response shall be as follows:

Octet (Hex)	Description
0-1	Interface Flags
2-3	Data Recovery Flags
4-7	Slave Status Flags
8-9	Slave Alarms
A-B	Slave Data Recovery Levels
C-D	Failure Detected and Pending Alarms
E-13	Vendor Unique Extended Status

See 8.3 for detailed definition of the Extended Status response. The slave may terminate the transfer at any point if the remaining octets are zeros.

7.1.23 Read Disk Specification Values (49h)

The Read Disk Specification Values response control causes the slave to transfer the parameter values related to the disk specification to the master.

Octet (Hex)	Parameters
0-1	Number of octets following: equals n-1 (Note 1)
2-5	Address of the last data cylinder
6-9	Address of the last defect list cylinder
A-B	Number of head addresses per cylinder
C-D	Number of heads per head address
E-11	Single cylinder seek time (microseconds) to read
12-15	Single cylinder seek time (microseconds) to write
16-19	Zone switch time (microseconds)
1A-1D	Maximum seek time (microseconds)
1E-21	Head switch time (microseconds) to read
22-25	Head switch time (microseconds) to write
26-29	Nominal rotation time (microseconds)
2A-2D	Write-to-read recovery time (microseconds)
2E-2F	Maximum Spindle Sync Accuracy + Tolerance (microseconds)
30-31	Maximum Spindle Sync Accuracy - Tolerance (microseconds)
32-33	**Maximum** Interrupt Response Time (IRT)
34-35	**Maximum TDO Response Time (seconds)**
36-37	Maximum defects per Head Disk Assembly (HDA)
38-39	**Maximum defects per Cylinder**
3A-3D	Buffer size in octets
3E-3F	Maximum Interface Transfer Rate (100 koctets/sec)
40-43	Cylinder Slip table size
44-45	Field 0 CRC byte count
46-47	ECC byte count
48-49	Number of zones (z+1)
	OCTETS PER HEAD ADDRESS DESCRIPTOR (Note 2 and Note 3)
0h-1h	Zone number (z)
2h-5h	Number of octets per head address
0h:n	Manufacturer's defined parameters

Notes
1 n is the octet number of last octet transferred.
2 Octet per head address descriptor is repeated for each zone.
3 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.

Seek, Head Switch, and Zone Switch times are to be measured at the Slave Connector for the purpose of reporting at the Read Disk Specification Response. The value actually measured at a particular slave may be less than, but not greater than, value reported.

If a TDO Slave Status is presented to a Load Cylinder Address, Load Head Address, or Load Position bus control, or to a data control with the step head bit set, the seek, Head Switch or Zone Switch time is measured from the setting of Slave status (Slave In asserted) to the presentation of the Command Complete Interrupt. If a TDO Slave Status is presented, the seek, Head Switch or Zone Switch time is measured from the transfer of the Master Status (Master Out Asserted) to the setting of Slave Status (Slave In Asserted). The Single Cylinder Seek and Zone Switch times reported shall include the time necessary to perform Step Head operation. The master need not add the reported Head Switch times to these values when calculating Sector Offset values at cylinder or zone boundaries.

For a Buffer Mode Only slave, all head switches in the middle of data transfers are managed by the slave. The Single Cylinder Seek, Head Switch and Zone Switch times reported at the Read Disk Specifications Response are used by the master for calculation of the Track Sector Offset parameter. The time reported must reflect the maximum time needed by the slave to complete the operation and be ready again for data transfer between the buffer and the media. The actual time required by the slave may be less than, but not greater than, value reported. The Single-Cylinder Seek and zone switch times reported shall include the time necessary to perform a Step Head operation. The master need not add the reported Head Switch times to these values when calculating the Cylinder Sector Offset and Zone Sector Offset parameters.

7.1.23.1 Number of octets following (0h-1h)

This parameter contains the octet count for the Read Disk Specification. It does not include itself in the octet count.

7.1.23.2 Address of the last data cylinder (2h-5h)

This parameter contains the address of the last data cylinder for this slave. The first cylinder has an address of zero.

7.1.23.3 Address of the last defect map cylinder (6h-9h)

This parameter contains the address of the last defect map cylinder for this slave.

7.1.23.4 Number of head address per cylinder (Ah-Bh)

This parameter indicates the number of heads for this slave.

7.1.23.5 Number of heads per head address (Ch-Dh)

This parameter indicates the number of parallel heads for this slave.

7.1.23.6 Single-cylinder seek time to read (Eh-11h)

This parameter contains the value of the single-cylinder seek time to read in microseconds for this slave.

7.1.23.7 Single cylinder time to write (12h-15h)

This four octet parameter contains the value of single cylinder seek time to write in microseconds for this slave.

7.1.23.8 Zone switch time (16h-19h)

This parameter contains the value of single cylinder seek time in microseconds at zone boundary.

7.1.23.9 Maximum seek time (1Ah-1Dh)

This parameter contains the value of the maximum seek time in microseconds for this slave.

7.1.23.10 Head switch time to read (1Eh-21h)

This parameter contains the value of the maximum head switching time to read in microseconds for this slave.

7.1.23.11 Head switch time to write (22h-25h)

This parameter contains the value of the maximum head switching time to write in microseconds for this slave.

7.1.23.12 Nominal rotational time (26h-29h)

This parameter contains the value of the nominal rotational time in microseconds for this slave.

7.1.23.13 Write-to-read recovery time (2Ah-2Dh)

This parameter contains the value of the maximum write-to-read recovery time in microseconds for this slave.

7.1.23.14 Maximum Spindle sync accuracy + tolerance (2Eh-2Fh)

This parameter contains the value of the maximum spindle sync accuracy + tolerance in microseconds for this slave.

7.1.23.15 Maximum Spindle sync accuracy - tolerance (30h-31h)

This parameter contains the value of the maximum spindle sync accuracy - tolerance in microseconds for this slave.

7.1.23.16 Maximum Interrupt Response Time (32h-33h)

This parameter contains the value of the **maximum time it takes, in microseconds, for the slave to respond to an** Interrupt **Request sequence. The value is measured from the masters assertion of Master Out to the slaves assertion of the Bit Significant Address. It is referenced at the slave end of the interface cable and does not account for interface delays.**

7.1.23.17 Maximum TDO Response Time (34h-35h)

This parameter contains the value of the maximum TDO Response Time in **seconds** for this slave. The TDO Response time is the maximum time it takes for the slave to return an interrupt after setting the TDO bit in slave ending status. The time reported is the time of the longest TDO command (i.e. most likely the spin up function).

7.1.23.18 Maximum defects per Head Disk Assembly (HDA) (36h-37h)

This parameter contains the maximum number of defects per Head Disk Assembly (HDA).

7.1.23.19 Maximum Defects per Cylinder (38h-39h)

This parameter contains the maximum number of defects per Cylinder.

7.1.23.20 Buffer size in octets (3Ah-3Dh)

This parameter contains the value of the buffer size in octets. The master shall use this information along with information from the Format Specification to determine the number of sectors buffer can hold.

7.1.23.21 Maximum Interface Transfer Rate (100 kbytes/sec) (3Eh-3Fh)

This parameter contains the maximum Interface Transfer Rate in 100 Kbytes/sec increments.

7.1.23.22 Cylinder Slip table size (40h-43h)

This parameter contains value of Cylinder Slip table size in octets.

7.1.23.23 Field 0 CRC byte count (44h-45h)

This parameter indicates the number of octets used by the slave for CRC in the field 0 post gap, if the Field 0 CRC is enabled in the Format Specification.

7.1.23.24 ECC byte count (46h-47h)

This parameter indicates the number of octets used for ECC in the Fields 1-n post-gap by the slave, if data field ECC is enabled at the Format Specification, and the number of octets used for ECC in the Field 0 post-gap by the slave, if Field 0 ECC is enabled at the Format Specification.

7.1.23.25 Number of zones (48h-49h)

This parameter contains the total number of zones and specifies the number of octets per head address descriptors that follow.

7.1.23.26 Zone number

This parameter contains the zone number. This parameter is repeated (along with the number of octets per head address parameter, see 7.1.23.25) once for each zone. Zones are numbered starting from 0.

7.1.23.27 Number of octets per head address

This parameter contains the number of octets per head address. This value is different for each zone.

7.1.23.28 Manufacturer's defined parameters

This is vendor unique and contains the manufacturer's defined values. These values should not be transferred if this parameter is not supported.

7.1.24 Read Port Control (4Ah)

This response causes the slave to transfer the disabling conditions accepted by the slave in the Load Port Control command.

After a Power-On Reset, an active Explicit (Reserve) Allegiance or an active Implicit (Selection) Allegiance at the alternate port shall disable the reporting of interrupts.

The format of the response parameters shall be as follows:

Octet (Hex)	Parameters
0	Disable the effect of the Explicit Allegiance and report the interrupt.
1	Disable the effect of the Implicit Allegiance and report the interrupt.

Octet details are same as 7.1.10 Load Port Control

7.1.25 Read Slave Formatter Parameters (4Bh)

The Read Slave Formatter Parameters causes the slave to transfer the values related to fixed gaps and the zone boundaries. See Figure 1 for pre-gap and post-gap positions relative to the data field. If the Format Specification is not initialized, this command shall be rejected with Bus Control Context in the Slave Status. The slave formatter parameters are valid after the format specification has been initialized.

Octet	Description
0h:1h	Number of octets following: equals (n-1) (Note 1)
2h:3h	Number of zones (z_{max}) (Note 2)
4h:5h	Number of fields per sector (m_{max}) (Note 3)
	READ ZONE DESCRIPTOR (Note 4 and Note 5)
0h:1h	Zone number (z)
2h:5h	Address of first cylinder in zone (z)
6h:9h	Address of last cylinder in zone (z)
	GAP OCTET DESCRIPTOR (Note 4 and Note 6)
0h:1h	Number of Pre-Gap octets for field (m)
2h:3h	Number of Post-Gap octets for field (m)

Notes
1 n is the octet number of the last octet transferred.
2 z_{max} is the zone number of the last zone plus 1. Zone numbers start from zero.
3 m_{max} equals the field number of the last field in a sector plus 1. Fields are numbered from zero.
4 The octet number of the DESCRIPTOR is a relative value to allow for repeating descriptors.
5 The read zone descriptor repeats z_{max} times.
6 The gap octet descriptor repeats m_{max} times within the Read Zone Descriptor.

7.1.25.1 Number of octets following

This parameter contains the octet count for the Read Slave Formatter Parameters. It does not include itself in the octet count.

7.1.25.2 Number of zones (z_{max})

This parameter contains the octet count for total number of zones for the slave and specifies the number of read zone descriptors to follow.

7.1.25.3 Number of fields per sector (m_{max})

This double-octet parameter contains the total count for all fields per sector.

7.1.25.4 Zone number (z)

This double-octet parameter contains the zone number.

7.1.25.5 Address of first cylinder in zone (z)

This four-octet parameter contains the address of first cylinder for this zone.

7.1.25.6 Address of last cylinder in zone (z)

This four-octet parameter contains the address of last cylinder for this zone.

7.1.25.7 Number of Pre-Gap octets for field (m)

This double-octet parameter contains the number of Pre-Gap octets for field (m).

7.1.25.8 Number of Post-Gap octets for field (m)

This double-octet parameter contains the number of Post-Gap octets for field (m).

7.1.26 Read Buffer Control (4Ch)

The Read Buffer Control response control causes the slave to transfer current parameters of the Buffer Control to the master for verification. The response shall have the following Format:

Octet (Hex)	Bit	Definition
0h-1h		Number of octets following: equals n - 1 (Note)
2h		reserved, set to 0
3h		Flag and Attribute octet
4-n		Remainder of Load Buffer Control Parameters (see 7.1.12)

NOTE — n is the octet number of the last octet transferred.

7.1.27 Read Cylinder Slip table (4Dh)

The Read Cylinder Slip table response control causes the slave to transfer current entries of the Cylinder Slip table to the master for verification. The response shall have the following Format:

Octet (Hex)	Bit	Definition
0h-1h		Number of octets following: equals n - 1 (Note)
2h-nh		Remainder of Cylinder Slip table

NOTE — n is the octet number of last octet transferred.

7.1.28 Read TDO Response (4Eh)

The Read TDO Response causes the slave to transfer information requested by the master at the previous Response type bus control that completed with a TDO ending from the slave. The format for this transfer shall be defined by the previously issued Response type bus control.

If another bus control is transferred by the master before the Read TDO Response, information for the previously issued Response type bus control may not be reported when the Read TDO Response is issued.

If the slave has not set TDO for a Response type bus control and the master issues a Read TDO Response bus control, the slave shall reject the bus control with a "Bus Control Context" bit set in the Slave Status.

7.1.29 Read RPS parameters (4Fh)

The Read RPS Parameters response control causes the slave to transfer the current RPS parameters to the master.

The RPS parameters are undefined for the Buffered Mode. After leaving the Buffer Mode, the values transferred at the Read RPS Pulse parameters shall be the last values assigned before invoking the Buffer Mode.

This command is not valid in buffered mode. Buffered mode only slaves will reject this command.

When default parameters are used the slave will modify the pulse width to match the current zone. When the master provides these parameters they remain the same for all zones.

The format of the response shall be as follows:

Octet (Hex)	Parameters
0-1	Extension
2-5	Pulse Width
6-9	Skew
A-B	Target Modifier

7.2 Fixed Block Data Controls

Fixed Block data controls enable the users to read and write on the disk in the Fixed Block Format. They specify the direction of the transfer, the fields to be involved, the orientation of the fields, and Head Advance control.

7.2.1 Definitions and use

7.2.1.1 Fixed Block Data Control types

There are two types of Fixed Block data controls: Field data controls and Sector data controls. Field data controls specify an operation on a single field or a pair of fields. Sector data controls are composite controls that specify operations on sectors having a header and data fields as required.

When using Field data controls, the previous field shall be operated on by a Field or Sector data control.

7.2.1.2 Head Advance Control

When bit 4 is set in a data control, the head counter advances at the end of a Information Transfer Sequence with Successful Information Transfer (SIT) in the Slave Status. The slave shall also advance the Head Counter if the Step Head Data Control is transferred (see 6.6). Head Counter shall not advance if Parity error occurs. The Buffer Mode does not support a Step Head Data Control and Data Controls with a Step Head Control bit set.

7.2.1.3 Orientation with the Disk

It is essential, while operating in non-buffered mode, that the master's transferring of Data Controls stays oriented with the disk so that no contiguous sector or field, which is intended to be operated on, is missed.

A non-orientation type Data Control that is not transferred in time for the slave to operate on the next sector or field, following the previous Information Transfer Sequence, causes orientation to be lost and is rejected.

To prevent the first Data Control of a command chain from being rejected when there is no orientation, both sector and field orientation shall be established by starting with one of the following orientation type Sector Data Controls:

At Target-type
Read Header-type
Verify Header-type

A Field Data Control that operates on the Header (Field 0), after sector orientation is set, shall again set the sector orientation.

After field orientation is set, a Field Data Control transferred in time, shall again set the field orientation.

Orientation is not lost by a Verify Miscompare or a master-initiated termination of the information transfer.

Orientation shall be lost if, after the transfer of an Head Advance type Data Control a field or sector is detected before completion of the operation or the Slave Status has the successful Information Transfer bit cleared. To allow the slave time to complete the Head Advance operation, it is recommended that the master conditions the Master Turnaround Delay in the Inter-field gap to allow for the Head Switch time. If the Head Switch time requires a large Inter-field gap and the slave supports the Target Modifier feature, the master should use the Target Modifier parameter to minimize the gap overhead.

The Step Head data control has no explicit effect on orientation.

When mixing the Sector Data Controls and Field Data Controls, field orientation shall not be lost at the field boundaries of the Sector Data Control and the slave shall accept an in context Data Control that is transferred in time to operate on the next field or sector.

Slave Status is presented following the field operated on by a field data control, or following the last field operated on by a sector data control. Field orientation is maintained if a field data control is transferred in time to operate on the next sequential field, and sector orientation is maintained if a sector data control is transferred in time to operate on the next sequential sector.

Examples of operations, when the Format Specification is initialized to a three field sector, are as follows:

1. A Read Header, Data Field 1 at Target is transferred followed by a Write Field.
The Read Header and Read Field 1 operation shall occur at Field 0 (Header) and Field 1 of the Target Sector.
The Write Field operation shall occur on Field 2 of the Target Sector.

2. A Read Header, Data Field 1 is transferred followed by a Write Header.
The Read Header and Read Field 1 operation shall occur at the first Field 0 (Header) and the following Field 1 that passes under the head.

The Write Header operation shall occur on the Header Field (Field 0) of the following sector.

7.2.1.4 Buffer Mode and Orientation with the Disk

While in a Buffer Mode it is not necessary that the master's transferring of Data Controls stays oriented with the disk. It is the slave's responsibility to manage conditions of orientation as the slave operates internally the write to media and read from media operations.

7.2.1.5 Target Sector

A group of read and write data controls operate on the Target Sector. The target sector is the sector identified by the master in a Load Target Address or Load Position command control.

7.2.1.6 Data control reject

Data controls shall be rejected for several reasons. Some examples are:

- The Format Specification is not initialized;
- The slave is active on the alternate port;
- The data control is a write or verify type and the slave is write protected;
- The orientation is lost;
- No space in the buffer - busy presented for write data control;
- No data in the buffer - busy presented for read data control;
- Buffer exception.

7.2.1.7 Data Control Coding

The Fixed Block data control has the following coding:

Bit	Description
7	1 = Data control 0 = Command/Response control
6	1 = Information In (Read) 0 = Information Out (Write)
5	0
4	Step Head control
3	Read/Write Header operation
2	Modifier bit Selects Target Sector Address for Read/Write operations Selects Verify Header for write operation Selects Skip Header for read operation
1	Data Field 2 operation
0	Data Field 1 operation

7.2.1.7.1 Data Controls in Non-Buffer Mode

The eight groupings of Data Controls plus a special control as shown in the following table are supported in this mode.

Bus Control Codes (Hex)	Data Control
80-83 91-93	Skip/Write Data Field
84-87 94-97	Verify Header, Write Data
88-8B 98-9B	Write Header, Write Data
8C-8F 9C-9F	Write Header, Write Data At Target Sector Address
C0-C3 D1-D3	Skip/Read Data Field
C4-C7 D4-D7	Skip Header, Read Data
C8-CB D8-DB	Read Header, Read Data
CC-CF DC-DF	Read Header, Read Data At Target Sector Address
90	Step Head
D0	reserved
A0-AF, B0-BF	reserved
E0-FF	reserved

7.2.1.7.2 Data Controls in Write Buffer Mode

Bus Control Codes (Hex)	Data Control
88	Write Header
89, 8A	Write Header and Write Field (1 or 2)
8B	Write Header and Write Fields (1 and 2)

7.2.1.7.3 Data Controls in Verify Buffer Mode

Bus Control Codes (Hex)	Data Control
84	Verify Header
85,86	Verify Header and Write Field (1 or 2)
87	Verify Header and Write Fields (1 and 2)

7.2.1.7.4 Data Controls in Read Buffer Mode

Bus Control Codes (Hex)	Data Control
C4	Skip Header
C5,C6	Skip Header and Read Field (1 or 2)
C7	Skip Header and Read Fields (1 and 2)
C8	Read Header
C9,CA	Read Header and Read Field (1 or 2)
CB	Read Header and Read Fields (1 and 2)

7.2.2 Sector Data Controls

Sector data controls are described separately for the Non-Buffer Mode and the Buffer Mode.

7.2.2.1 Sector Data Controls (Non-Buffer Mode)

Sector data controls operate on sectors consisting of a Header Field and one or more optional Data Fields. These data controls are described in 7.2.2.1 through 7.2.2.24. The first of the two hexadecimal codes is for no head advance; the second is for head advance.

No data is transferred during a Skip operation.

7.2.2.1.1 Verify Header (84h, 94h)

The Verify Header sector data control causes the slave to verify the next Header Field against data transferred from the master. If the header verifies, the slave shall set Operation Completed in the Slave Status. If the header does not verify, the slave shall disable the transfer after the header and indicate Verify Header Miscompare in the Slave Status.

7.2.2.1.2 Verify Header and Write Data Field 1 (85h, 95h)

The Verify Header and Write Data Field 1 sector data control causes the slave to verify the next Header Field against data transferred from the master. If the header verifies, the slave continues to write Data Field 1 with data transferred from the master. If the header does not verify, the slave shall disable the transfer after the header and indicate Verify Header Miscompare in the Slave Status.

7.2.2.1.3 Verify Header and Write Data Field 2 (86h, 96h)

The Verify Header and Write Data Field 2 sector data control causes the slave to verify the next Header Field against data transferred from the master. If the header verifies, the slave continues to write Data Field 2 with data transferred from the master. If the header does not verify, the slave shall disable the transfer after the header and indicate Verify Header Miscompare in the Slave Status.

7.2.2.1.4 Verify Header and Write Data Fields 1 and 2 (87h, 97h)

The Verify Header and Write Data Fields 1 and 2 sector data control causes the slave to verify the next Header Field against data transferred from the master. If the header verifies, the slave continues to write Data Fields 1 and 2 with data transferred from the master. If the header does not verify, the slave shall disable the transfer after the header and indicate Verify Header Miscompare in the Slave Status.

7.2.2.1.5 Write Header (88h, 98h)

The Write Header sector data control causes the slave to write the next Header Field with data transferred from the master.

7.2.2.1.6 Write Header and Data Field 1 (89h, 99h)

The Write Header and Data Field 1 sector data control causes the slave to write the next Header Field and Data Field 1 with data transferred from the master.

7.2.2.1.7 Write Header and Data Field 2 (8Ah, 9Ah)

The Write Header and Data Field 2 sector data control causes the slave to write the next Header Field and Data Field 2 with data transferred from the master.

7.2.2.1.8 Write Header and Data Fields 1 and 2 (8Bh, 9Bh)

The Write Header and Data Fields 1 and 2 sector data control causes the slave to write the next Header Field and Data Fields 1 and 2 with data transferred from the master.

7.2.2.1.9 Write Header at Target sector address (8Ch, 9Ch)

The Write Header At Target sector data control causes the slave to write the Header Field at the target sector with data transferred from the master.

7.2.2.1.10 Write Header and Data Field 1 at Target (8Dh, 9Dh)

The Write Header and Data Field 1 At Target sector data control causes the slave to write the Header Field and Data Field 1 at the target sector with data transferred from the master.

7.2.2.1.11 Write Header and Data Field 2 at Target (8Eh, 9Eh)

The Write Header and Data Field 2 At Target sector data control causes the slave to write the Header Field and Data Field 2 at the target sector with data transferred from the master.

7.2.2.1.12 Write Header and Data Fields 1 and 2 at Target (8Fh, 9Fh)

The Write Header and Data Fields 1 and 2 At Target sector data control causes the slave to write the Header Field and Data Fields 1 and 2 at the target sector with data transferred from the master.

7.2.2.1.13 Skip Header (C4h, D4h)

The Skip Header sector data controls causes the slave to skip the next Header Field. No data is transferred and the slave initiates the Ending Status Sequence at the end of the Header Field.

7.2.2.1.14 Skip Header and Read Data Field 1 (C5h, D5h)

The Skip Header and Read Data Field 1 sector data control causes the slave to skip the next Header and transfer Data Field 1 to the master.

7.2.2.1.15 Skip Header and Read Data Field 2 (C6h, D6h)

The Skip Header and Read Data Field 2 sector data control causes the slave to skip the next Header Field and transfer Data Field 2 to the master.

7.2.2.1.16 Skip Header and Read Data Fields 1 and 2 (C7h, D7h)

The Skip Header and Read Data Fields 1 and 2 sector data control causes the slave to skip the next Header Field and transfer Data Fields 1 and 2 to the master.

7.2.2.1.17 Read Header (C8h, D8h)

The Read Header sector data control causes the slave to transfer the next Header Field to the master.

7.2.2.1.18 Read Header and Data Field 1 (C9h, D9h)

The Read Header and Data Field 1 sector data control causes the slave to transfer the next Header Field and Data Field 1 to the master.

7.2.2.1.19 Read Header and Data Field 2 (CAh, DAh)

The Read Header and Data Field 2 sector data control causes the slave to transfer the next Header Field and Data Field 2 to the master.

7.2.2.1.20 Read Header and Data Fields 1 and 2 (CBh, DBh)

The Read Header and Data Fields 1 and 2 sector data control causes the slave to transfer the next Header Field and Data Fields 1 and 2 to the master.

7.2.2.1.21 Read Header at Target (CCh, DCh)

The Read Header at Target sector data control causes the slave to transfer the Header Field at the target sector to the master.

7.2.2.1.22 Read Header and Data Field 1 at Target (CDh, DDh)

The Read Header and Data Field 1 At Target sector data control causes the slave to transfer the Header Field and Data Field 1 at the target sector to the master.

7.2.2.1.23 Read Header and Data field 2 at Target (CEh, DEh)

The Read Header and Data Field 2 At Target sector data control causes the slave to transfer the Header Field and Data Field 2 at the target sector to the master.

7.2.2.1.24 Read Header and Data Fields 1 and 2 at Target (CFh, DFh)

The Read Header and Data Fields 1 and 2 At Target sector data control causes the slave to transfer the Header Field and Data Fields 1 and 2 at the target sector to the master.

7.2.2.2 Sector Data Controls (Buffer Mode)

Sector data controls operate on sectors consisting of a Header Field and one or more optional Data Fields. These data controls are described in 7.2.2.2.1 through 7.2.2.2.16.

No data is transferred during a Skip operation.

7.2.2.2.1 Verify Header (84h)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave verifies the Header Field read from media against data transferred from the buffer at later time.

If the header does not verify during the Buffer Mode with Stop on Exception, the slave shall disable the transfer. The slave sets the Verify Header Miscompare and residual count in the Status Response.

If the header does not verify during the Buffer Mode with Continue on Exception, the slave continues to verify headers until it reaches the Buffer Exception Maximum Count or the End of Cylinder. If the Buffer Exception Maximum Count is exceeded or the End of Cylinder is reached the slave shall disable the transfer after the header. The Status Response shall indicate Verify Header Miscompare, End of Cylinder and the Residual Count.

7.2.2.2.2 Verify Header and Write Data Field 1 (85h)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave verifies the Header Field read from media against data transferred from the buffer at later time. If the header verifies, the slave continues to write Data Field 1 with data transferred from the buffer.

If the header does not verify during the Buffer Mode with Stop on Exception, the slave shall disable the transfer. The slave sets the Verify Header Miscompare and residual count in the Status Response.

If the header does not verify during the Buffer Mode with Continue on Exception, the slave continues to verify headers until it reaches the Buffer Exception Maximum Count or the End of Cylinder. If the Buffer Exception Maximum Count is exceeded or the End of Cylinder is reached the slave shall disable the transfer after the header. The Status Response shall indicate Verify Header Miscompare, End of Cylinder and the residual count.

7.2.2.2.3 Verify Header and Write Data Field 2 (86h)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave verifies the Header Field read from media against data transferred from the buffer at later time. If the header verifies, the slave continues to write Data Field 2 with data transferred from the buffer.

If the header does not verify during the Buffer Mode with Stop on Exception, the slave shall disable the transfer. The slave sets the Verify Header Miscompare and residual count in the Status Response.

If the header does not verify during the Buffer Mode with Continue on Exception, the slave continues to verify headers until it reaches the Buffer Exception Maximum Count or the End of Cylinder. If the Buffer Exception Maximum Count is exceeded or the End of Cylinder is reached the slave shall disable the transfer after the header. The Status Response shall indicate Verify Header Miscompare, End of Cylinder and the residual count.

7.2.2.2.4 Verify Header and Write Data Fields 1 and 2 (87h)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave verifies the Header Field read from media against data transferred from the buffer at later time. If the header verifies, the slave continues to write Data Fields 1 and 2 with data transferred from the buffer.

If the header does not verify during the Buffer Mode with Stop on Exception, the slave shall disable the transfer. The slave sets the Verify Header Miscompare and residual count in the Status Response.

If the header does not verify during the Buffer Mode with Continue on Exception, the slave continues to verify headers until it reaches the Buffer Exception Maximum Count or the End of Cylinder. If the Buffer Exception Maximum Count is exceeded or the End of Cylinder is reached the slave shall disable the transfer after the header. The Status Response shall indicate Verify Header Miscompare, End of Cylinder and the residual count.

7.2.2.2.5 Write Header (88h)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave writes the next Header Field with data transferred from the buffer at a later time.

7.2.2.2.6 Write Header and Data Field 1 (89h)

The data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave writes Header Field and Data Field 1 with data transferred from the buffer at a later time.

7.2.2.2.7 Write Header and Data Field 2 (8Ah)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave writes the next Header Field and Data Field 2 with data transferred from the buffer at a later time.

7.2.2.2.8 Write Header and Data Fields 1 and 2 (8Bh)

This data control is transferred into the buffer and the slave sets Operation Completed in the Slave Status. Then the slave writes the next Header Field and Data Fields 1 and 2 with data transferred from the buffer at a later time.

7.2.2.2.9 Skip Header (C4h)

This data control causes the slave to skip next Header Field. No data is transferred and the slave initiates the Ending Status Sequence at the end of the Header Field.

7.2.2.2.10 Skip Header and Read Data Field 1 (C5h)

This data control causes the slave to skip the next Header Field and transfer Data Field 1 to the master from the buffer.

7.2.2.2.11 Skip Header and Read Data Field 2 (C6h)

This data control the slave to Skip Header and transfer Data Field 2 to the master from the buffer.

7.2.2.2.12 Skip Header and Read Data Fields 1 and 2 (C7h)

This data control the slave to Skip Header and transfer Data Field 1 and 2 to the master from the buffer.

7.2.2.2.13 Read Header (C8h)

The Read Header sector data control causes the slave to transfer the next Header to the master from the buffer. If Header is not in the buffer, the slave shall set Busy in the Slave Status.

7.2.2.2.14 Read Header and Data Field 1 (C9h)

The Read Header and Data Field 1 sector data control causes the slave to transfer the next Header and Data Field 1 to the master from the buffer. If Header Field is not in the buffer, the slave shall set Busy in the Slave Status.

7.2.2.2.15 Read Header and Data Field 2 (CAh)

The Read Header and Data Field 2 sector data control causes the slave to transfer the next Header and Data Field 2 to the master from the buffer. If the Header is not in the buffer, the slave shall set Busy in the Slave Status.

7.2.2.2.16 Read Header and Data Fields 1 and 2 (CBh)

The Read Header and Data Fields 1 and 2 sector data control causes the slave to transfer the next Header and Data Fields 1 and 2 to the master from the buffer. If the Header is not in the buffer, the slave shall set Busy in the Slave Status.

7.2.3 Field Data Controls

Field Data Controls are supported only for Non-Buffer Mode operation.

7.2.3.1 Field Data Controls (Non-Buffer Mode)

Field data Controls operate on a single field or a pair of fields and are described in 7.2.3.1 through 7.2.3.8.

No data is transferred during a Skip operation.

The first hexadecimal code is for no head advance; the second is for head advance.

7.2.3.1.1 Skip Field (80h)

The Skip Field data control causes the slave to skip the next field.

7.2.3.1.2 Skip two Fields (C0h)

The Skip Two Fields data control causes the slave to skip the next two fields.

7.2.3.1.3 Write Field (81h, 91h)

The Write Field data control causes the slave to write the next field with data transferred from the master.

7.2.3.1.4 Skip Field and Write Field (82h, 92h)

The Skip Field and Write Field data control causes the slave to skip the next field and then write the following field with data transferred from the master.

7.2.3.1.5 Write Two Fields (83h, 93h)

The Write Two Fields data control causes the slave to write the next two fields with data transferred from the master.

7.2.3.1.6 Read Field (C1h, D1h)

The Read Field data control causes the slave to transfer the next field to the master.

7.2.3.1.7 Skip Field and Read Field (C2h, D2h)

The Skip Field and Read Field data control causes the slave to skip the next field and then transfer the following field to the master.

7.2.3.1.8 Read Two Fields (C3h, D3h)

The Read Two Fields data control causes the slave to transfer the next two fields to the master.

7.2.3.1.9 Special Data Controls - Step Head (90h)

The Step Head data control causes the slave to advance to the next head address. No data is transferred. (see 6.6)

7.2.3.2 Field Data Controls (Buffer Mode)

Field Data Controls are not supported in Buffer Mode.

8 Status

8.1 Slave Status

The Slave Status Octet is transferred to the master during the Ending Status Sequence and is defined as follows:

Bit	Description
7	Successful Information Transfer Sequence
6	Bus Parity Error
5	0
4	Time-Dependent Operation
3-0	Encoded Status 0000b = Operation Completed 0001b = Logical Busy (see 6.19.5.2) 0010b = Overrun or underrun 0011b = SYNC IN or SYNC OUT miscount 0100b = Data Exception, Field 0 CRC 0101b = Data Exception, Missed Sync Byte 0110b = Data Exception, ECC error 0111b = Data Exception, Verify Header Miscompare 1000b = Operation Exception 1001b = Operation Exception and Slave Busy 1010b = Data Exception, uncorrectable ECC Error 1011b = reserved 1100b = Status Pending 1101b = reserved 1110b = reserved 1111b = reserved

8.1.1 Successful Information Transfer Sequence

This bit shall be set if the Information Transfer Sequence was successful.

8.1.2 Bus Parity Error

This bit shall be set if there is a Parity Error on the Bus Control Octet, any information transferred by the master, or Master Status Octet.

8.1.3 Time-Dependent Operation

This bit shall be set if the operation has not completed at the time this status is transferred to the master. This bit shall be set if the operation

(1) is not completed during the Information Transfer Sequence, or
(2) causes an Operation Exception for an existing Verify Buffer Mode or Write Buffer Mode that is pending completion.

Following a successful information transfer sequence one of the following shall occur:

(1) the Command Completion interrupt shall be set, or
(2) the RPS or Class 2 Buffer Available Interrupt shall be set, or
(3) the Status Pending interrupt shall be set, or
(4) if a Logical Reset is transferred by the master following the setting of TDO bit, the slave shall not set the owed interrupt. Operation by the slave on the **transferred** command is not defined.

8.1.4 Encoded Status

This four-bit value indicates the status of the attempted Information Transfer Sequence.

8.1.4.1 Operation Completed (0000b)

Encoded Status shall be set to 0000b if the operation has completed at the time this status is transferred to the master.

8.1.4.2 Logical Busy (0001b)

Encoded Status shall be set to 0001b if the slave is Logical Busy and can not perform the operation (see 6.19.5.2).

8.1.4.3 Overrun or Underrun (0010b)

Encoded Status shall be set to 0010b if, during a data control streaming transfer, the master could not assert SYNC OUT pulses in response to the Slave's assertion of SYNC IN pulses at the data rate required by the Slave (i.e. Read overrun or Write/Verify underrun).

8.1.4.4 SYNC IN or SYNC OUT miscount (0011b)

Encoded Status shall be set to 0011b if, at the end of a Data Control streaming transfer, the slave did not count the same number of SYNC OUT pulses from the master as the slave's SYNC IN pulses to the master.

8.1.4.5 Data Exception, Field 0 CRC (0100b)

Encoded Status shall be set to 0100b if the Slave detects a CRC error on Field 0 during operation of a read or verify type Data Bus Control. This encoded status is only presented if ECC/CRC is enabled by Function code 2Dh -Enable Slave ECC/CRC Reporting or Function code 21h - Enable ECC correction. No correction vectors are available for CRC errors.

8.1.4.6 Data Exception, Missed Sync Byte (0101b)

Encoded Status shall be set to 0101b if a failure to detect the sync byte pattern has occurred.

8.1.4.7 Data Exception ECC Error (option) (0110b)

This encoded status has different meanings for Buffer Mode and Non-Buffer Mode. In Non-Buffer Mode, the encoded Status shall be set to 0110b if the Slave detects a correctable ECC error. Correction vectors are available using the Read Correction Vectors Bus Control. This Encoded Status shall be set only if ECC/CRC reporting is enabled by the Function Code 2Dh - Enable Slave ECC/CRC Reporting. In Buffer mode, the Encoded Status shall be set to 0110b if the slave has detected an ECC error and ECC/CRC reporting is enabled by Function Code 2Dh - Enable slave ECC/CRC Reporting, or if the slave has corrected an ECC error and ECC correction is enabled by the Function Code 21h - Enable Slave ECC Correction.

8.1.4.8 Data Exception,Verify Header Miscompare (0111b)

Encoded Status shall be set to 0111b when there is a mismatch of data field 0 data and data transferred for field 0 from the master.

8.1.4.9 Operation Exceptions (1000b)

Encoded Status shall be set to 1000b if the attempted Information Transfer Sequence incurred an Operation Exception, and that the detail of this exception may be determined by transferring a Read Status Response Control.
This operation differs from Unsolicited Exception and the master may choose to ignore to transfer Read Status Response Control.

If the Status Response is ignored, it shall be cleared upon transfer of the next Information Transfer.

8.1.4.10 Operation Exception and Slave Busy (1001b)

Encoded status shall be set to 1001b if the Information Transfer Sequence is rejected due to an operation exception that can not be reported at this time because the slave is busy.

8.1.4.11 Data Exception, uncorrectable ECC error (1010b)

The Encoded Status shall be set to 1010b if the slave has detected an ECC error that it has determined to be uncorrectable. No correction vectors are available. The Encoded Status is only presented if ECC/CRC is enabled by Function Code 2Dh - Enable Slave ECC/CRC/Reporting, or the Function Code 21h - Enable ECC Correction.

8.1.4.12 Status Pending (1100b)

Encoded status of 1100b, indicates that the attempted Information Transfer Sequence was rejected because a Status is pending and the master shall read this status by transferring a Read Status Response Control before any other Bus Control shall be accepted.

8.2 Status Response

The status bits of the Status Response indicate exception conditions. Exception status bits are set at the time of occurrence. The setting of any exception status bit sets the Status Pending interrupt, unless previously indicated at Slave Status with a 1000b (Operation Exception) encoded status.

The slave transfers the Status Response to the master upon acceptance of a Read Status Response Control and clears all exception status bits if the Master Status Octet indicates a successful transfer. The exception status bits are also cleared by a Logical Reset. If there is no status pending interrupt, the Exception Status bits are cleared upon the acceptance of any Bus Control.

The Status Response octets shall have the following format:

Octet (Hex)	Bit	Description
0		Exception Status
	7	Reserved, set to zero
	6	Unsolicited Exception
	5	Bus Control/Parameter Exception
	4	Read Fault
	3	Write Fault
	2	Seek Fault
	1	Spindle Fault
	0	Completion Fault
1		Exception Status
	7	Idle Exception
	6	Buffer Operation Exception
	5	reserved, set to zero
	4	reserved, set to zero
	3	reserved, set to zero
	2	reserved, set to zero
	1	reserved, set to zero
	0	reserved, set to zero

2		Unsolicited Exception Status
	7	Slave Reset Complete
	6	Alternate Port Priority Selected
	5	Alternate Port Format Specification Changed
	4	Alternate Port Format Complete
	3	Alternate Port Target Modifier Change
	2	Alternate Port Buffer Control Change
	1	Alternate port Semaphore 1
	0	Alternate Port Semaphore 0
3		Unsolicited Exception Status
	7	Spindle Sync Transition, Unlocked to Locked
	6	Spindle Sync Transition, Locked to Unlocked
	5	Service Alarm
	4	Port Enabled
	3	Failure Pending Alarm
	2	Failure Detected Alarm
	1	Not Ready Transition
	0	Ready Transition
4		**Unsolicited Exception Status**
	7	**Spindle Sync Reference Signal Fault**
	6-0	**Reserved, set to 0**
5		Unsolicited Exception Status
		Reserved, set to zero
6		Bus Control/Parameter Exception Status
	7	Invalid Bus Control
	6	Invalid Parameter
	5	Unsupported Bus Control
	4	Bus Control Context
	3	Data Control Late
	2	Unsupported Function Code
	1	Invalid Function Code
	0	Function Code Context
7		Bus Control/Parameter Exception Status
	7	Write Protect Context
	6	Local Spin up Context
	5-0	Reserved, set to zero
8		Slave Exception Status
	7	Speed Fault
	6	Off Cylinder Fault
	5	Head Select Fault
	4	Spindle Sync Fault
	3	Fan Alarm
	2	Voltage Fault
	1	Logic Temperature Fault
	0	Actuator Temperature Alarm

9		Slave Exception Status
	7	Write Circuit Fault
	6	Write Current Fault
	5	Write Transition Fault
	4	Head Offset Fault
	3	Data Strobe Fault
	2	Data Recovery Level Fault
	1	ECC/CRC Fault
	0	Reserved, set to zero
A		Slave Exception Status
		Reserved, set to zero
B		Slave Exception Status
		Reserved, set to zero
C		Buffer Exception Status
	7	Reserved, set to zero
	6	End of Cylinder
	5	Write to Buffer Late
	4	Buffer Exception Maximum Count
	3	Reserved, set to zero
	2	Buffer Operation Missed Sync Byte Error
	1	Buffer Operation Verify Header Miscompare
	0	Buffer Fault
D		Buffer Exception Status
	7	Buffer Operation Field 0 CRC error
	6	Buffer Operation uncorrectable ECC error
	5	**Verify/Write Successful with Retries**
	4-0	Reserved, set to zero
E-F		Buffer Exception Status
		Residual Count
10-1F		Vendor Unique Status

8.2.1 Exception Status (0h)

8.2.1.1 Status Response (Bit 7)

This bit is always set to zero for a Status Response.

8.2.1.2 Unsolicited Exception (Bit 6)

This bit is set when the slave has incurred an Unsolicited Exception condition. At least one bit shall be set in octets 2-5 describing the exception type. This bit and bits in octet 2-5 can only be cleared (on a port basis) by transferring a Read Status Response Control followed by a Master Status Octet with the Successful Information Transfer bit set. As long as Status Pending condition exists for a port, the slave shall reject all Bus Controls, except Read Status Response Control, with Status Pending set in the Slave status octet.

8.2.1.3 Bus Control/Parameter Exception (Bit 5)

This bit shall be set when the slave rejects a Bus Control or a Parameter. At least one bit shall be set in octets 6-7 to describe the exception.

8.2.1.4 Read Fault (Bit 4)

This bit shall be set when the slave detects an error while performing a Read or Verify data control. At least one bit shall be set in octets 8h - 1Fh to describe the type exception related to the Read Fault.

8.2.1.5 Write Fault (Bit 3)

This bit shall be set when the slave detects an error while performing a Write Data control. At least one bit shall be set in octets 8h - 1Fh to describe the type of exception related to the Write Fault.

8.2.1.6 Seek Fault (Bit 2)

This bit shall be set when the slave detects a seek error while performing a seek command or data control. At least one bit shall be set in octets 8h - 1Fh to describe the type of exception related to the Seek fault.

8.2.1.7 Spindle Fault (Bit 1)

This bit shall be set when the slave detects a spindle error while performing a Spin Up function code, a Spin Down function code or a data control. At least one bit shall be set in octets 8h - 1Fh to describe the type of exception related to the Spindle Fault.

8.2.1.8 Completion Fault (Bit 0)

This bit shall be set when the slave detects a Completion fault other than Read, Write, Seek or Spindle Fault during the completion of a command or a Data Control. At least one bit shall be set in octet 8h - 1Fh to describe the type of exception related to the Completion Fault.

8.2.2 Exception Status (1h)

8.2.2.1 Alarm Exception (Bit 7)

This bit shall be set when the slave needs service. At least one bit shall be set in octets 8h - 17h to describe the type of exception.

8.2.2.2 Buffer Operation Exception (Bit 6)

This bit shall be set if an error occurs during read or write operation while slave is in the Buffer Mode. At Least one bit shall be set in octet 8h - 17h to describe the exception and the residual count in octets Eh - Fh may be valid.

8.2.2.3 Reserved for future use (Bit 5)

8.2.2.4 Reserved for future use (Bit 4)

8.2.2.5 Reserved for future use (Bit 3)

8.2.2.6 Reserved for future use (Bit 2)

8.2.2.7 Reserved for future use (Bit 1)

8.2.2.8 Reserved for future use (Bit 0)

8.2.3 Unsolicited Exception Status (2h)

8.2.3.1 Slave Reset Complete (Bit 7)

This bit shall be set when the slave has performed and completed a Slave Reset.

8.2.3.2 Alternate Port Priority Selected (Bit 6)

This bit shall be set when the alternate port completes a normal selection sequence, with the Priority Select bit set or the Priority Select and Priority Hold bits are set in the selection octet. This bit is not cleared with a Reset Slave Interrupts Sequence.

8.2.3.3 Alternate Port Format Specification Changed (Bit 5)

This bit shall be set when the alternate port has accepted a Format Specification.

8.2.3.4 Alternate Port Format Complete (Bit 4)

This bit shall be set when the alternate port receives a Load Slave function code 16h, Notify Alternate Port of Format Completion.

8.2.3.5 Alternate Port Target Modifier Change (Bit 3)

This bit shall be set when the alternate port accepts a Load Target Modifier.

8.2.3.6 Alternate Port Buffer Control Change (Bit 2)

This bit shall be set if alternate port has accepted a Load Buffer Control command.

8.2.3.7 Alternate Port Semaphore 1 (Bit 1)

This bit shall be set if the master transfers a Load Slave Function command control with Function code 2Bh.

8.2.3.8 Alternate Port Semaphore 0 (Bit 0)

This bit shall be set if the master transfers a Load Slave Function command control with Function code 2Ah.

8.2.4 Unsolicited Exception Status (3h)

8.2.4.1 Spindle Sync Transition, Unlocked to Locked (Bit 7)

This bit shall be set when the spindle sync transition goes from unlocked to locked condition.

8.2.4.2 Spindle Sync Transition, Locked to Unlocked (Bit 6)

This bit shall be set when the Spindle Sync Transition goes from locked to unlocked condition.

8.2.4.3 Service Alarm (Bit 5)

This bit shall be set when the slave requires service.

8.2.4.4 Port Enabled (Bit 4)

This bit shall be set when the port is enabled.

8.2.4.5 Failure Pending Alarm (Bit 3)

This bit shall be set when the slave has detected a pending internal failure. It is recommended that data be removed from the slave immediately. Field replacement units for this condition are identified in the Extended Status Response.

8.2.4.6 Failure Detected Alarm (Bit 2)

This bit shall be set when the slave has detected an internal failure. Field replacement units for this condition are identified in the Extended Status Response.

8.2.4.7 Not Ready Transition (Bit 1)

This bit shall be set when the slave goes from a ready to a not ready condition.

8.2.4.8 Ready Transition (Bit 0)

This bit shall be set when the slave goes from a not ready to ready condition.

8.2.5 Unsolicited Exception Status (4h, bits 7-0)

8.2.6 Unsolicited Exception Status (5h, bits 7-0)

8.2.7 Bus Control/Parameter Exception Status (6h)

8.2.7.1 Invalid Bus Control (Bit 7)

This bit shall be set when a Bus Control is transferred that is not defined in this standard.

8.2.7.2 Invalid Parameter (Bit 6)

This bit shall be set when a valid command Bus Control is transferred with an invalid parameter.

8.2.7.3 Unsupported Bus Control (Bit 5)

This bit shall be set when a valid Bus Control is transferred that is not supported by this slave.

8.2.7.4 Bus Control Context (Bit 4)

This bit shall be set when a valid Bus Control is transferred but can not be completed because it conflicts with the current context of the slave.

8.2.7.5 Data Control Late (Bit 3)

This bit shall be set when a valid Data Control is transferred too late for the slave to perform on the next field.

8.2.7.6 Unsupported Function Code (Bit 2)

This bit shall be set when a valid function code is transferred that is not supported by this slave.

8.2.7.7 Invalid Function Code (Bit 1)

This bit shall be set when a Function Code is transferred that is not defined in this standard.

8.2.7.8 Function Code Context (Bit 0)

This bit shall be set when a valid Function Code is transferred but cannot be completed because it conflicts with the current context of the slave.

8.2.8 Bus Control/Parameter Exception Status (7h)

8.2.8.1 Write Protect Context (Bit 7)

This bit shall be set if Write Protect Switch is active and Write Type Data Control is transferred by the master.

8.2.8.2 Local Spin up Context (Bit 6)

This bit shall be set if Local Spin up mode is active and function code for Spin up or Spin down is transferred by the master.

8.2.8.3 Reserved, set to zero (Bits 5-0)

8.2.9 Slave Exception Status (octet 8h)

8.2.9.1 Speed Fault (Bit 7)

This bit shall be set if the slave did not reach the required speed in the required time during the completion of a spin-up function code or loses speed during Data Control completion.

8.2.9.2 Off Cylinder Fault (Bit 6)

This bit shall be set if the slave did not come on cylinder in the required time during the completion of a seek, or loses "on cylinder" during Data Control completion.

8.2.9.3 Head Select Fault (Bit 5)

This bit shall be set if the slave detects an invalid head selection.

8.2.9.4 Spindle Sync Fault (Bit 4)

This bit shall be set if any fault occurs related to spindle synchronization.

8.2.9.5 Fan Alarm (Bit 3)

This bit shall be set if the slave detects any problem with the fan.

8.2.9.6 Voltage Fault (Bit 2)

This bit shall be set if the slave detects a voltage out of range.

8.2.9.7 Logic Temperature Fault (Bit 1)

This bit shall be set if the slave detects an over temperature condition in the slave electronics.

8.2.9.8 Actuator Temperature Fault (Bit 0)

This bit shall be set if the slave detects an over temperature condition in the slave servo actuator.

8.2.10 Slave Exception Status (9h)

8.2.10.1 Write Circuit Fault (Bit 7)

This bit shall be set if a Write circuit failure is detected during the completion of a data control which requires a write to media.

8.2.10.2 Write Current Fault (Bit 6)

This bit shall be set if write current was out of range during completion of a data control which requires a write to media.

8.2.10.3 Write Transition Fault (Bit 5)

This bit shall be set if no write transition is detected by the slave during the completion of a data control operation which requires a write to media.

8.2.10.4 Head Offset Fault (Bit 4)

This bit shall be set if the data heads were in an offset position when a Write type data control was transferred.

8.2.10.5 Data Strobe Fault (Bit 3)

This bit shall be set if the slave receives a Write type data control when early and late strobe is in effect.

8.2.10.6 Data Recovery Level Fault (Bit 2)

This bit shall be set if the slave receives a Write type data control while a slave Data Recovery Level condition is active.

8.2.10.7 ECC/CRC fault (Bit 1)

This bit shall be set if the slave has detected a CRC error or uncorrectable ECC error.

8.2.10.8 Reserved, for future use (Bit 0)

8.2.11 Slave Exception Status (Ah, bits 7-0)

8.2.12 Slave Exception Status (Bh, bits 7-0)

8.2.13 Slave Exception Status (Ch)

8.2.13.1 Reserved, set to zero (Bit 7)

8.2.13.2 End of Cylinder (Bit 6)

This bit shall be set if the slave is in a Buffer Mode, detects End of Cylinder when "Buffer Across Cylinder Boundaries Attribute" is not set or detects End of Cylinder on last buffer operation cylinder if "Buffer Across Cylinder Boundaries Attribute" is set and one of the following conditions exist:

(1) Missed Sync Byte and Continue on Exception.
(2) Verify Header Miscompare and Continue on Exception **and Buffer Retry count exhausted.**
(3) **Buffer** not empty during write to media.
(4) Read Data Control transferred after detection of End of Cylinder and the buffer is empty.

8.2.13.3 Write to Buffer Late (Bit 5)

This bit shall be set if an empty buffer is detected while writing to media from buffer during the Verify Buffer Mode or Write Buffer Mode. The slave shall not attempt writing to media unless it has partial sector in the buffer and expecting remaining data in the buffer before completion. If the master throttles the transfer rate after sector write to media has started, Write to Buffer Late bit shall be set.

8.2.13.4 Buffer Exception Maximum Count (Bit 4)

This bit shall be set if the slave reaches Buffer Exception Maximum Count specified in the Format Specification during Buffer Mode with Continue on Exception.

8.2.13.5 Reserved, set to zero (Bit 3)

8.2.13.6 Buffer Operation Sync Byte Error (Bit 2)

This bit shall be set if the slave detects a Missed Sync Byte while in a Buffer Mode and one of the following condition exist:

1. Buffer Mode is coded for Stop on Exception.
2. Buffer Mode is coded for Continue on Missed Sync Byte and the slave reaches the Buffer Exception Maximum Count **or End of Cylinder for read operations.**
3. **Buffer Mode is coded for Continue on Missed Sync Byte and the slave reaches the Buffer Exception Maximum Count or End of Cylinder and the Buffer Retry count is exhausted for Verify/Write operations.**

When this bit is set the slave shall disable the Buffer Mode, disable the operation to or from the media, and set the class 3 interrupt.

8.2.13.7 Buffer Operation Verify Header Miscompare (bit 1)

This bit shall be set if the slave detects a Verify Header Miscompare while in a Buffer Mode and one of the following condition exist:

1. Buffer Mode is coded for Stop on Exception.
2. Buffer Mode is coded for Continue on Verify Header Miscompare and the slave reaches the Buffer Exception Maximum Count or End of Cylinder and the Buffer Retry count is exhausted.

When this bit is set the slave shall disable the Buffer Mode, disable the operation to or from the media, and set the class 3 interrupt.

8.2.13.8 Buffer Fault (Bit 0)

This bit shall be set if the slave detects a Buffer hardware Fault while in a Buffer Mode. **Retries are disabled when this occurs since the data in the buffer may be corrupted.**

When this bit is set the slave shall disable the Buffer Mode, disable the operation to or from the media, and set the class 3 interrupt.

8.2.14 Buffer Exception Status (Dh)

8.2.14.1 Buffer Operation Field 0 CRC error (Bit 7)

This bit shall be set if the slave has detected a CRC error in Field 0 **and the Buffer Retry count is exhausted** (Retries **are only used on Verify/Write operations**). No correction vectors are available for CRC errors.

8.2.14.2 Buffer Operation uncorrectable ECC error (Bit 6)

This bit shall be set if the slave detects an ECC error that has been determined to be uncorrectable while in a Buffer Mode and one of the following condition exist:

1. Buffer Mode is coded for Stop on Exception.
2. Buffer Mode is coded for Continue on ECC error and the slave reaches the Buffer Exception Maximum Count for **Read operations.**
3. **Buffer Mode is coded for Continue on ECC error and the slave reaches the Buffer Exception Maximum Count and Retries are exhausted for Verify/write operations.**

When this bit is set the slave shall disable the Buffer Mode, disable the operation to or from the media, and set the class 3 interrupt.

8.2.14.3 Verify/Write Successful with Retries (Bit 5)

This bit shall be set if the slave **successfully recovers from an error during a Verify/Write operation by performing retries.**

8.2.15 Residual Count (Eh-Fh)

Residual Count MSB (octet Eh, bit 7), Residual Count LSB (octet Fh, bit 0)

Octets Eh and Fh contain the number of sectors remaining in the buffer when the slave disables transferring of data to the media because of a buffer exception. The Residual Count is incremented each time a Write or Verify/Write data control is accepted by the slave with 80h ending status. The residual count is decremented each time a sector of data is successfully written to the media.

8.2.16 Vendor Unique Status (10h-17h)

8.3 Extended Status Response

The slave transfers Extended Status Response to the master upon acceptance of a Read Extended Status Response Control. The Extended Status bits are dynamic indications of current flag states and slave conditions.

The Extended Status Response shall have the following format:

Octet (Hex)	Bit	Description
0		Interface Flags
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Port Number 1
	4	Port Number 0
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Port 1 Enabled
	0	Port 0 Enabled
1		Interface Flags
	7	Command Complete Interrupt Attention Enabled
	6	RPS Interrupt Attention Enabled
	5	Status Pending Interrupt Attention Enabled
	4	"No Longer Busy" Attention Enabled
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Target Modifier Present
	0	Reserve Active
2		Data Recovery Flags
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Slave ECC/CRC Enabled
3		Data Recovery Flags
	7	Offset Direction
	6	Positive/Negative Offset 3 Active
	5	Positive/Negative Offset 2 Active
	4	Positive/Negative Offset 1 Active
	3	Early Strobe Active
	2	Late Strobe Active
	1	Reserved, set to zero
	0	Reserved, set to zero
4		Slave Status Flags
	7	Write protected
	6	Spindle Power On
	5	Spindle Sync Transition Status Enabled
	4	Spindle Sync Enabled
	3	Spindle Sync Offset Active
	2	Spindle Sync Reference Source Enabled
	1	Spindle Sync Locked
	0	Local Spindle Sync Enabled

5		Slave Status Flags
	7	At Speed
	6	On Cylinder
	5	Heads Loaded
	4	Format Specification Present
	3	Local Spin Up Mode active
	2	Carriage Locked
	1	Head Disk Assembly (HDA) Ready
	0	Media Present
6		Slave Status Flags
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Reserved, set to zero
7		Slave Status Flags
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Reserved, set to zero
8		Slave Alarms
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Illegal Head Selected
	3	Reserved, set to zero
	2	Voltage Range Error Detected
	1	Logic Over Temperature Detected
	0	Actuator Over Temperature Detected
9		Slave Alarms
	7	Reserved, set to zero
	6	Reserved, set to zero
	5	Reserved, set to zero
	4	Reserved, set to zero
	3	Reserved, set to zero
	2	Reserved, set to zero
	1	Reserved, set to zero
	0	Reserved, set to zero
A-B	7-0	Slave Data Recovery Levels
C		Failure Pending Alarms
	7	Field Replacement Unit 7 failure pending
	6	Field Replacement Unit 6 failure pending
	5	Field Replacement Unit 5 failure pending
	4	Field Replacement Unit 4 failure pending
	3	Field Replacement Unit 3 failure pending
	2	Field Replacement Unit 2 failure pending
	1	Field Replacement Unit 1 failure pending
	0	Head-Disk Assembly failure pending
D		Failure Detected Alarms

7	Field Replacement Unit 7 failure detected
6	Field Replacement Unit 6 failure detected
5	Field Replacement Unit 5 failure detected
4	Field Replacement Unit 4 failure detected
3	Field Replacement Unit 3 failure detected
2	Field Replacement Unit 2 failure detected
1	Field Replacement Unit 1 failure detected
0	Head-Disk Assembly failure detected

E-13 7-0 Vendor Unique Extended Status

8.3.1 Interface Flags (0h)

8.3.1.1 Reserved, set to zero (Bit 7)

8.3.1.2 Reserved, set to zero (Bit 6)

8.3.1.3 Port Number 1 (Bit 5)

This bit shall be set for port 1.

8.3.1.4 Port Number 0 (Bit 4)

This bit shall be set for port 0.

8.3.1.5 Reserved, set to zero (Bit 3)

8.3.1.6 Reserved, set to zero (Bit 2)

8.3.1.7 Port 1 Enabled (Bit 1)

This bit shall be set if port 1 is enabled.

8.3.1.8 Port 0 Enabled (Bit 0)

This bit shall be set if port 0 is enabled.

8.3.2 Interrupt Flags (1h)

8.3.2.1 Command Complete Interrupt Attention Enabled (Bit 7)

This bit shall be set when the ATTENTION IN signal is enabled to be asserted following a Command Complete Interrupt being set on this port.

8.3.2.2 RPS Interrupt Attention Enabled (Bit 6)

This bit shall be set when the ATTENTION IN signal is enabled to be asserted following an RPS Interrupt being set on this port.

8.3.2.3 Status Pending Interrupt Attention Enabled (Bit 5)

This bit shall be set when the ATTENTION IN signal is enabled to be asserted following a Status Pending Interrupt being set on this port.

8.3.2.4 "No Longer Busy" Attention Enabled (Bit 4)

This bit shall be set when the ATTENTION IN signal is enabled to be asserted following a busy to not busy transition.

8.3.2.5 Reserved, set to zero (Bit 3)

8.3.2.6 Reserved, set to zero (Bit 2)

8.3.2.7 Target Modifier Present (Bit 1)

This bit shall be set if a Load Target Modifier command has been accepted.

8.3.2.8 Reserved, set to zero (Bit 0)

8.3.3 Data Recovery Flags (2h)

8.3.3.1 Reserved, set to zero (Bit 7)

8.3.3.2 Reserved, set to zero (Bit 6)

8.3.3.3 Reserved, set to zero (Bit 5)

8.3.3.4 Reserved, set to zero (Bit 4)

8.3.3.5 Reserved, set to zero (Bit 3)

8.3.3.6 Reserved, set to zero (Bit 2)

8.3.3.7 Reserved, set to zero (Bit 1)

8.3.3.8 Slave ECC/CRC Enabled (Bit 0)

This bit shall be set if the slave ECC/CRC feature is enabled.

8.3.4 Data Recovery Flags (3h)

8.3.4.1 Offset Direction (Bit 7)

If head offset is in effect, this bit indicates direction of offset. This bit is cleared when positive offset (away from the spindle) is in effect, and set when negative offset (towards the spindle) is in effect. If bits 6, 5 and 4 of this octet are cleared, then no head offset is in effect and bit 7 has no meaning.

8.3.4.2 Positive/Negative Offset 3 Active (Bit 6)

This bit shall be set if Positive/Negative Offset 3 is active. This offset is the highest level offset and when it is set, all the other offsets (bits 5 and 4) shall be set to zero.

8.3.4.3 Positive/Negative Offset 2 Active (Bit 5)

This bit shall be set if Positive/Negative Offset 2 is active. This offset is the middle level offset and when it is set, all the other offsets (bits 6 and 4) shall be set to zero.

8.3.4.4 Positive/Negative Offset 1 Active (Bit 4)

This bit shall be set if Positive/Negative Offset 1 is active. This offset is the lowest level offset and when it is set, all the other offsets (bits 6 and 5) shall be set to zero.

8.3.4.5 Early Strobe Active (Bit 3)

This bit shall be set if Early Data Strobe is active.

8.3.4.6 Late Strobe Active (Bit 2)

This bit shall be set if Late Data Strobe is active.

8.3.4.7 Reserved, set to zero (Bit 1)

8.3.4.8 Reserved, set to zero (Bit 0)

8.3.5 Slave Status Flags (4h)

8.3.5.1 Write Protected (Bit 7)

This bit shall be set if the slave is currently write protected.

8.3.5.2 Spindle Power On (Bit 6)

This bit shall be set while power is applied to the spindle.

8.3.5.3 Spindle Sync Transition Status Enabled (octet 4h bit 5)

This bit shall be set if the spindle sync transition status is enabled.

8.3.5.4 Spindle Sync Enabled (Bit 4)

This bit shall be set if the spindle sync is enabled.

8.3.5.5 Spindle Sync Offset Active (Bit 3)

This bit shall be set if the Load Index Offset command was accepted.

8.3.5.6 Spindle Sync Reference Source Enabled (Bit 2)

This bit shall be set if the slave is the Spindle Sync Reference Source.

8.3.5.7 Spindle Sync Locked (Bit 1)

This bit shall be set if spindle synchronization is locked.

8.3.5.8 Local Spindle Sync Enabled (Bit 0)

This bit shall be set when the slave has been enabled by the slave's local mechanism (switch or jumper).

When the Local Spindle Sync Enabled bit is set, the slave may reject Spindle Sync related commands depending on the conditions of the other Local Control mechanisms.

8.3.6 Slave Status Flags (5h)

8.3.6.1 At Speed (Bit 7)

This bit shall be set if the slave spindle is at operating speed.

8.3.6.2 On Cylinder (Bit 6)

This bit shall be set if the slave actuator is on cylinder.

8.3.6.3 Heads Loaded (Bit 5)

This bit shall be set if a Load Heads function code is in effect.

8.3.6.4 Format Specification Present (Bit 4)

The slave currently has an initialized Format Specification.

8.3.6.5 Local Spin Up Mode active (Bit 3)

This bit shall be set if the local spin up mode is in effect. The slave shall reject the spin down function code as out of context if this bit is set. During power on when the slave is spinning up, the slave shall report physical busy during the selection sequence until spin up is complete.

8.3.6.6 Carriage Locked (Bit 2)

This bit shall be set if a Lock Carriage function code is in effect.

8.3.6.7 Head Disk Assembly (HDA) Ready (Bit 1)

This bit shall be set when slave is at speed, the actuator is positioned at the addressed track, and the heads are capable of data operation.

8.3.6.8 Media Present (Bit 0)

This bit shall be set when slave media is present.

8.3.7 Slave Status Flags (6h, bits 7-0)

Reserved, set to zero

8.3.8 Slave Status Flags (7h, bits 7-0)

Reserved, set to zero

8.3.9 Slave Alarms (8h)

8.3.9.1 Reserved, set to zero (Bit 7)

8.3.9.2 Reserved, set to zero (Bit 6)

8.3.9.3 Reserved, set to zero (Bit 5)

8.3.9.4 Illegal Head Selected (Bit 4)

This bit shall be set when the slave detects that multiple heads are selected or no head is selected.

8.3.9.5 Reserved, set to zero (Bit 3)

8.3.9.6 Voltage Range Error Detected (Bit 2)

This bit shall be set when the slave has one or more voltages out of range.

8.3.9.7 Logic Over Temperature Detected (Bit 1)

This bit shall be set when the slave logic is over maximum operating temperature.

8.3.9.8 Actuator Over Temperature Detected (Bit 0)

This bit shall be set when the slave actuator is over maximum operating temperature.

8.3.10 Slave Alarms (9h, bits 7-0)

Reserved,set to zero.

8.3.11 Slave Data Recovery Levels (Ah-Bh, bits 7-0)

This parameter contains the number of the Slave Data Recovery Level currently active at the slave. If the slave does not support this function, or if no Data Recovery Level is currently active, the parameter shall be set to zero.

8.3.12 Failure Pending Alarms (Ch, Bits 7-0)

These alarms identify the vendor unique Field Replacement Units (FRU) in which the slave has detected a pending failure condition.

8.3.13 Failure Detected Alarms (Dh, Bits 7-0)

These alarms identify the vendor unique Field Replacement Units (FRU) in which the slave has detected a failure condition.

8.3.14 Vendor unique extended status (Eh-13h)

Annex A

(informative)

Examples of Track Sector Offset, Cylinder Sector offset, Zone Sector Offset and End of Cylinder

A.1 Buffer Mode

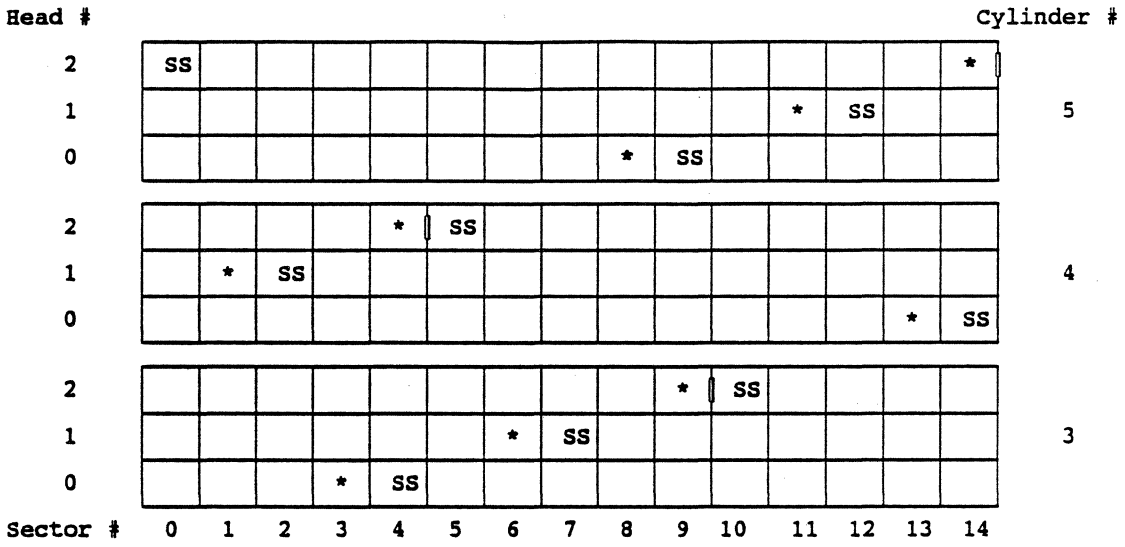
Formula for calculating Starting Sector (SS) is shown below.

$$SS = \text{Remainder of } \frac{[(ZCN \times [CSO + ([\#HDS - 1] \times TSO)]) + (HD\# \times TSO) + ZSO]}{\text{Sectors per Track}}$$

Key:

ZCN	= Zone Cylinder Number (Cylinder # - Starting Cylinder # in the same zone)
CSO	= Cylinder Sector Offset
TSO	= Track Sector Offset
HD#	= Head Number
#HDS	= Number of Heads per Cylinder
ZSO	= Zone Sector Offset of Current Zone

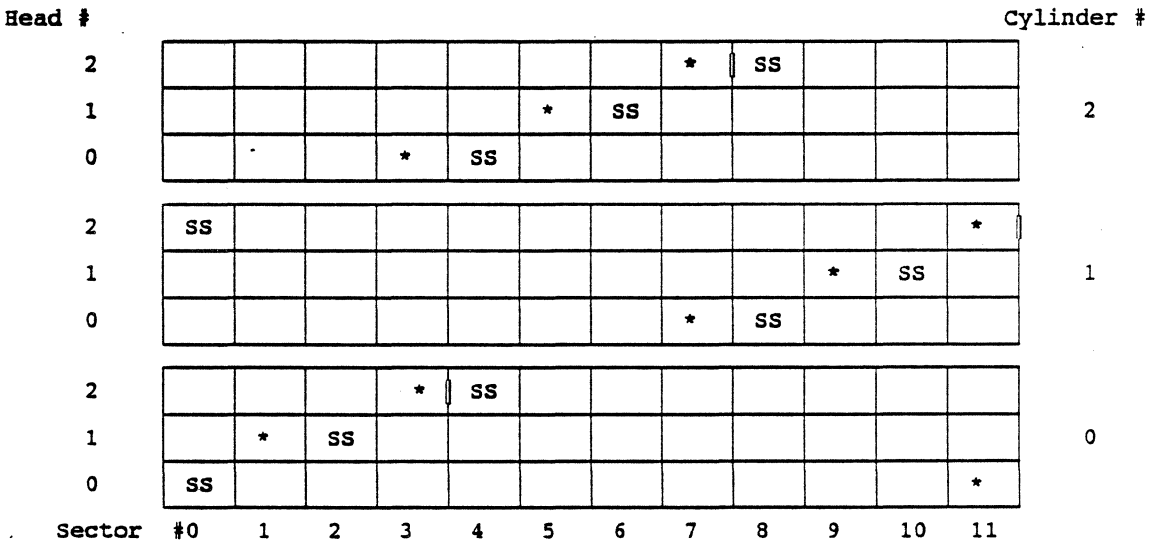
Examples showing Auto Head Step Sector using Track Sector Offset, Cylinder Sector Offset, Zone Sector Offset and End of Cylinder for Zone 0 and Zone 1 are shown below.



Key:
* = AHSS (Auto Head Step Sector)
SS = Starting Sector
| = End of Cylinder

Number of Cylinders = 3
Number of Sectors = 15
Number of Heads = 3
TSO = 3, CSO = 4, ZSO = 4

Figure A.1 — TSO, CSO, ZSO and EOC example for Zone 1



Key:
* = AHSS (Auto Head Step Sector)
SS = Starting Sector
| = End of Cylinder

Number of Cylinders = 3
Number of Sectors = 12
Number of Heads = 3
TSO = 2, CSO = 4, ZSO = 0

Figure A.2 — TSO, CSO, ZSO and EOC example for Zone 0

B.1 Read Immediate Buffer Mode

During the Read Immediate Buffer Mode Starting Sector (SS) position can not be calculated using the formula shown in annex A.1. SS position in this mode is the first available sector on a track. The slave reads an entire track of data into the buffer starting at first available sector and then performs a headswitch. The slave continues to read data into the buffer using TSO, CSO and ZSO values as defined by the master. SS position on a new track can be calculated as follows:

- TSO value is added to the last position after headswitch to determine SS position on a next track.
- TSO and CSO values are added to the last position after **cylinder switch** to determine SS position on a first track of the next cylinder.
- ZSO value is used after Zoneswitch to determine SS position on a first track of next zone.

The examples for TSO, CSO, ZSO and EOC are shown in Figures A.1 and A.2. For the Read Immediate Buffer Mode, it is implied for both figures that SS position in cylinder 0 head 0 is the first available sector on a track and not the target sector.

Annex B

(informative)

Bibliography

B.1 Informative References

The following parts of ISO/IEC are not essential for the completion of the requirements of this standard. They are intended to be used solely for explanation or clarification.

ISO/IEC 9318-3:1990 - *Information technology - Intelligent Peripheral Interface*
- *Part 3: Device-Generic Command Set for Magnetic and Optical Disks.*

ISO/IEC 9318-4:1990 - *Information technology - Intelligent Peripheral Interface*
- *Part 4: Device-Generic Command Set for Magnetic Tapes.*

B.2 Equivalent ANSI Standards

The following American National Standard Institute (ANSI) standards are the equivalent for International Standard Organization (ISO) standards.

ISO/IEC 9318-1:1990 - *Intelligent Peripheral Interface - IPI-0/1*
- *ANSI X.129 - 1986 Physical Level*

ISO/IEC 9318-2:1990 - *Intelligent Peripheral Interface - IPI-2*
- *ANSI X3.130-1986 Device-Specific Command Set for Magnetic Disk Drives*

ISO/IEC 9318-3:1990 - *Intelligent Peripheral Interface - IPI-3*
- *ANSI X3.132-1986 Device-Generic Command Set for Magnetic and Optical Disk Drives.*

ISO/IEC 9318-4:1989 - *Intelligent Peripheral Interface - IPI-3*
- *ANSI X3.147-1986 Device-Generic Command Set for Magnetic Tapes.*

ISO/IEC 9318-5:1990 - *Intelligent Peripheral Interface - IPI-2*
- *ANSI X3.176-1990 Device Specific Command Set for Magnetic Tapes.*

ISO/IEC 9318-6:199x - *Intelligent Peripheral Interface - IPI-0/1*
- *ANSI X.XXX - 1990 Enhanced Physical Level*

Annex C

(informative)

Storage of Format Specifications and Attributes.

A master typically has the need to store Format Specifications and Attributes on the disk.

The storage of the Format Specifications shall be the responsibility of the master. These specifications may be recorded anywhere on the media in the preferred format of the master. This recording follows the same style as the Defect Map with each Format Specification recorded three times in a set.

If the master wishes to record them in an area according to the Manufacturer's Format specification, the Last address available area is defined in each data field of the Defect Map.

The recommended format of each data field is as follows:

Octet Count (Hex)	(Dec)	Bit	Description
00-01	(1-2)		Number of octets following: equals n - 1
02	(3)		Flag octet
		7	Last Data Field set of storage
		6-0	reserved, set to zero
03	(4)		Number of this Data Field within a Set 00 = First 01 = Second 02 = Third 03-FE = Illegal FF = Ignore
04-05	(5-6)		Number of Sets in Format Specification
06-07	(7-8)		Number of this Set in the Format Specification
08	(9)		Partition
09	(10)		Alias address
0A-0D	(11-14)		Number of octets per Data Block
0E	(15)		Flags
		7	Data Block same size as Physical Block
		6	Data Block multiple of Physical Block
		5	Data Block non-multiple of Physical Block
		4-1	reserved, set to zero
		0	Interleaves performed by master
0F	(16)		Cylinder interleave factor
10	(17)		Head interleave factor
11	(18)		Sector interleave factor
12-13	(19-20)		Number of alternate cylinders per Partition
14	(21)		Number of spare sectors per track
15	(22)		Number of spare sectors per cylinder
16-19	(23-26)		Partition starting cylinder address
1A-1D	(27-30)		Number of cylinders in Partition
1E-1F	(31-32)		Number of octets in Format Specification: equals (m - 1)
20	(33)		Format Specification (see 6.2). Repeat octets 6 through (m+1A) for additional Partitions
(m+1A) through (n-2)	(m+24) through (n-2)		Zero (if any octets not filled by entries)
(n-1) through n	(n-1) through n		CRC-16

NOTE — If the slave is not used with an IPI Level 3 interface, octets 08-1D are not used and should be zeros.

Annex D

(informative)

Spindle Sync Reference Connector and Cabling

This signal for spindle synchronization is sent continuously to all slaves. It is treated like all other IPI signals in that it must be terminated at both ends of the cable and uses the same class of transceivers as the rest of the slaves.

This requires a separate cable to carry the slave sync reference information. To meet requirements for emissions and positive retention, a single 9 pin female D-sub connector per facility can be used. This then requires that the daisy chain for the slave sync interface be carried in the cable instead of through the slave.

By proper choice of signal pins in the slave sync connector it is possible to use mass terminate connectors to achieve this multidrop type cable. The **recommended** pinout for this spindle sync connector are:

Pin	Function
1	-sync reference signal
2	reserved
3	reserved
4	reserved
5	ground
6	+sync reference signal
7	reserved
8	reserved
9	reserved
shell	shield

An alternate choice of signals pins that has been shown to provide improved signal quality at the maximum cable lengths when using mass terminated ribbon cable are:

Pin	Function
1	**reserved**
2	**reserved**
3	**reserved**
4	**ground**
5	**-sync reference signal**
6	**+sync reference signal**
7	**ground**
8	**reserved**
9	**reserved**
shell	**shield**

These types of connections allows either an IPI Master (controller) to drive the Slave Sync signal or one of the slaves may also be specified as a master to drive this signal.

The slave should not ground or connect to any connector pins marked as reserved as they may be used at the master level for fault tolerance or master to master communication.

Always check vendor specifications for pinout to ensure compatibility.

Annex E

(informative)

Target Modifier Examples

A controller (master) reads configuration which gives head switch time in microseconds, rotational speed and number of sectors per head address. A simple calculation determines the number of sector times it takes for a head switch to complete. From this information the Target Modifier can be determined.

nominal rotation time: 3656 RPM (16400 usec)
number of fixed sectors per head address: 42 (1K sector size)
head switching time: 1696 usec

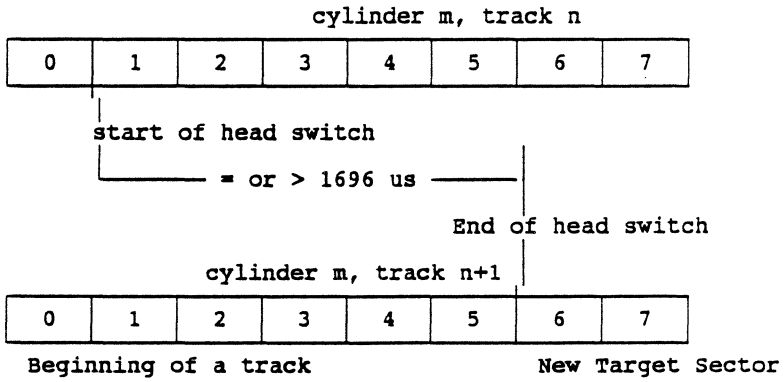
Sector time = nominal rotation time / # of sectors per head address
= 16400/42
= 390 usec

# of sectors for head switch = head switching / sector time
= 1696/390
= 4.3 or 5 sector times

Since the first sector that can be safely accessed is the sector following where the head settled, the sector offset value should therefore be a minimum of 6. **The Target Modifier should then be set to 5 (5+1=6).**

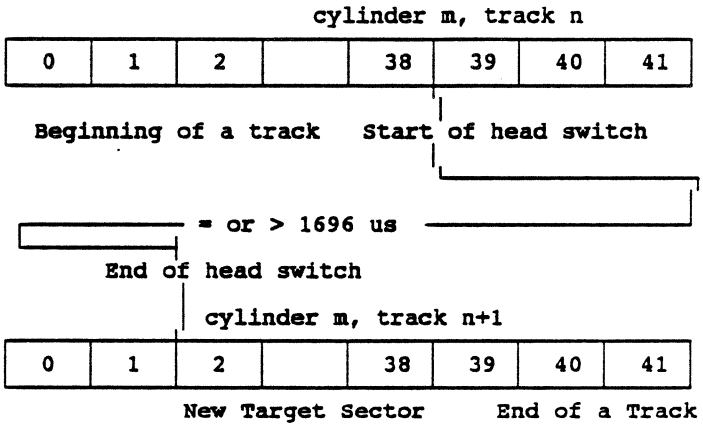
Example 1: Data Control with Step Head bit set during sector 0.

Modified Target Sector Address	=	(last sector operated on (0)
	+	target modifier **(0005h)**
	+	**1)**
	modulo	# sectors per head address (42)
	=	(0 + 5 + 1) MOD 42
	=	6 MOD 42
	=	6



Example 2: Data Control with Step Head bit set during sector 38 (near end of track).

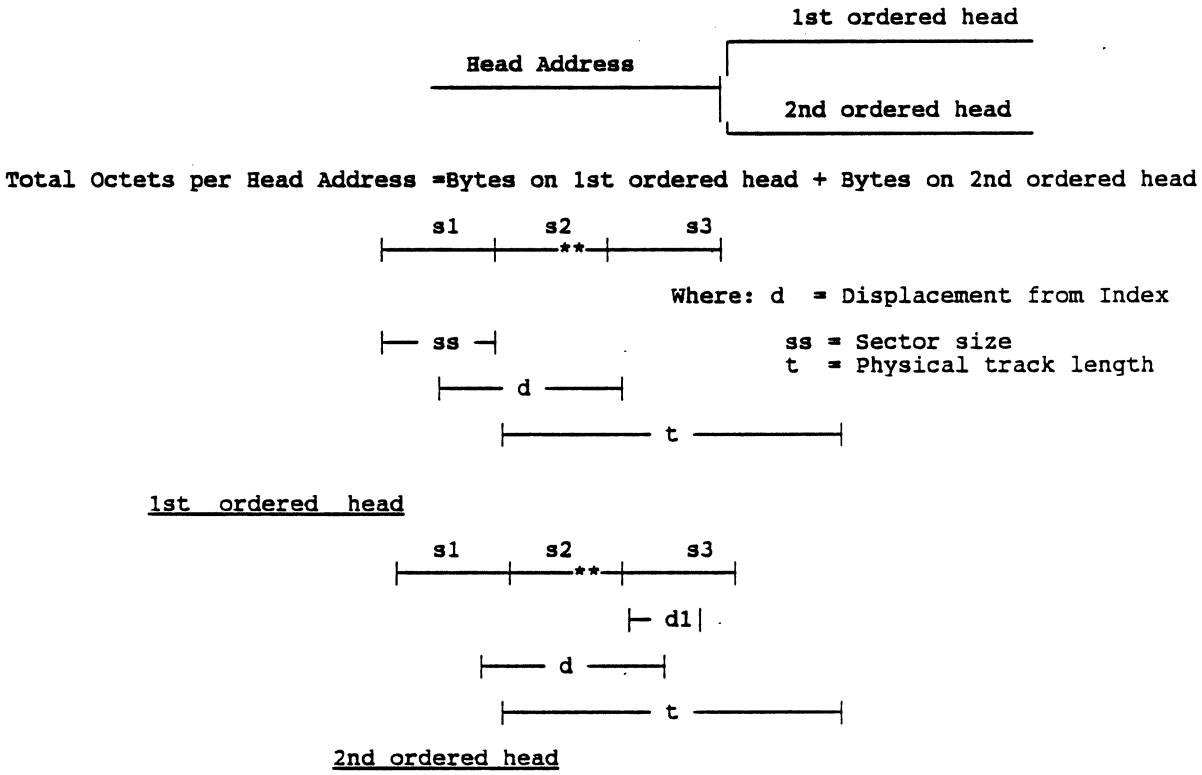
Modified Target Address = (38 + 5 + 1) MOD 42
= 44 MOD 42
= 2



Annex F

(informative)

The Defects in Parallel Heads



Head address contains two heads in parallel: 1. 1st ordered head 2. 2nd ordered head.

1. The Defect in 1st ordered head

   The offset of defect from Index = d

2. The defect in second ordered head

   The offset of defect from Index = d + t

Annex G

(informative)

Defect Management for Buffer Mode Operation

A sector slipping technique is described to manage defective sectors. Each cylinder would have a number of spare sectors reserved at the End of Cylinder. The headers would contain the cylinder address and a sector address within a cylinder instead of sector address within a track. No head address information would be contained in the header since a slipped sector address can move to a next sequential head. At the format time, defects that affect a header or a data field would cause that sector's header to be written so as to cause a verify miscompare error during a verify/write operation. Then, during a write, if the drive gets a header verify miscompare error it continues to verify headers for specified number of sectors in the format specification or it reaches the End of Cylinder. During reads the master would have to read each header and verify its slipped position in the cylinder before reading the data in the data field. The master has to slip an entire cylinder if the number of defects in the cylinder exceeds the number of spare sectors in that cylinder.

This Defect Management scheme is shown in a Defect Management example. Three spare sectors and two defective sectors are shown in the example. Sector 2 has a bad data field and sector 7 has a bad header field. Both of them have been written with an illegal code defined by the master at format time. Once a sector is slipped due to defective header field or data field, all good sectors (including spare sectors) following this sector, are assigned new position.

HEAD 0	H D * 0000 **0000	H D 0001 0001	bad H D 0002 XXXX	H D 0003 0002
HEAD 1	H D 0004 0003	H D 0005 0004	H D 0006 0005	bad H D 0007 XXXX
HEAD 2	H D 0008 0006	spare H D 0009 0007	spare H D 000A 0008	spare H D 000B unused

* Physical Address (Cylinder 00, Sector 00)
** Next Valid Sector in sequence
XXXX Forced miscompare header data
H Header field
D Data Field
Number of defective sectors : 2
Number of spares : 3
Number of heads : 3

Figure G.1 — Defect Management Example

REVISION HISTORY

INFORMATION DRAFT	IPI-2/054	20 Aug 1990
INFORMATION DRAFT	IPI-2/067	05 Sep 1990
INFORMATION DRAFT	IPI-2/068	16 Oct 1990
INFORMATION DRAFT	IPI-2/081	01 Nov 1990
INFORMATION DRAFT	IPI-2/083	03 Dec 1990
PRELIMINARY DRAFT	IPI-2/094	18 Feb 1991
PRELIMINARY DRAFT	IPI-2/094-R1	20 Mar 1991
PRELIMINARY DRAFT	IPI-2/145	17 Jun 1991
PRELIMINARY DRAFT	IPI-2/149	**18 Aug 1991**
PRELIMINARY DRAFT	**IPI-2/154**	**03 Sep 1991**