ECC INTERFACE

GENERAL DESCRIPTION:

PIN	SIGNAL NAME	I/O	FUNCTION
1	/WTGTBL	I	WRITE GATE-B (ACTIVE LOW) FROM CONTROLLER, WHICH INDICATES THAT WRITE DATA IS SHIFTING FROM CONTROLLER TO ECC FOR CHECK BYTES GENERATION. TOTAL NUMBER OF CHECK BYTES IS 6.
2	/ECCCLRL	O	ECC CLEAR IS AN OUTPUT TEST SIGNAL THAT INDICATES THE INTERNAL RESET OF SHIFT REGISTERS.
3	CRCWDATA	I	THIS IS AN INPUT SIGNAL FROM CONTROLLER THAT INCLUDES WRITE DATA AND 2 CRC CHECK BYTES. WRITE DATA AND CHECK BYTES ARE SYNCHRONIZED TO THE FALLING EDGE OF /RWCKA.
4	/RWCKA	I	READ/WRITE CLOCK-A IS AN INPUT SIGNAL THAT USE THE FALLING EDGE TO SYNCHRONIZE THE WRITE DATA FROM CONTROLLER THROUGH ECC TO DRIVE, AND TO SYNCHRONIZE THE READ DATA FROM DRIVE THROUGH ECC TO CONTROLLER. MAX FREQUENCY INPUT IS 12 MHZ..
5	RDATAH	I	READ DATA (ACTIVE HIGH) FROM DRIVE SYNCHRONIZED TO THE FALLING EDGE OF /RWCKA.
6	/ECCTESTL	I	ECC TEST IS A TEST INPUT THAT ALLOW READ/WRITE DATA TO PASS THROUGH ECC WITHOUT CHECK BYTES GENERATION OR CHECKING.
7	DR/W	I	THIS SIGNAL WHEN HIGH IS IN DATA READ MODE, WHEN LOW IS IN DATA WRITE MODE.
9	Y0	I	SEQUENCER INPUT BIT 0.
10	Y1	I	SEQUENCER INPUT BIT 1.
11	Y2	I	SEQUENCER INPUT BIT 2.
12	Y3	I	SEQUENCER INPUT BIT 3.

Y3,Y2,Y1,Y0	FUNCTION
0000	RESET
1111	RESET
0111	RESET
1001	RESET
1101	RESET
1100	ECC ENABLE
1110	ECC ENABLE
1010	ECC CHECK BYTES PROCESSING
0010	ECC DON'T CARE STATE

PIN	SIGNAL NAME	I/O	FUNCTION
13	/ECCWRTL	O	THIS SIGNAL IS AN OUTPUT TEST SIGNAL. WHEN IN DATA READ MODE, THIS SIGNAL WILL GO LOW WHEN CHECK BYTES ARE IN ERRROR CHECKING PROCESS. WHEN IN DATA WRITE MODE, THIS SIGNAL INDICATES CHECK BYTES GENERATION IS IN PROGRESS.

ECC INTERFACE

14   /ECCERR   0   ECC ERROR IS AN OUTPUT LATCHED SIGNAL THAT WILL GO LOW
WHEN READ DATA HAS AN ERROR. IT CAN BE PRESET BY SETTING
THE SEQUENCER INPUT TO ONE OF THESE RESET STATES:
$Y3,Y2,Y1,Y0=0000,1111,0111,1001,1101,1100$.
WHEN IN DATA WRITE MODE, /ECCERR IS IN DON'T CARE STATE.

15   ECCWDATA   0   ECC WRITE DATA IS AN OUTPUT SIGNAL. WHEN IN DATA WRITE
MODE, IT CONTAINS THE WRITE DATA, 2 CRC CHECK BYTES FROM
CONTROLLER AND 6 ECC CHECK BYTES. WHEN IN DATA READ
MODE, IT CONTAINS THE READ DATA, 2 CRC CHECK BYTES FROM
DRIVE, AND 6 BYTES OF ECC SYNDROME. THE SYNDROME BYTES
ARE ALL ZERO IF NO READ ERROR IS DETECTED.

16   VCC   I   5V POWER SUPPLY INPUT.
8   GND   I   LOGIC GROUND.

DC ELECTRICAL CHARACTERISTICS (TEMPERATURE=0 TO 70 C)

PARAMETERS		MIN.	TYP.	MAX.	UNITS	COMMENTS
VIL	INPUT LOW VOLTAGE	-0.3		0.8	V	IOL MAX.=-10 UA
VIH	INPUT HIGH VOLTAGE	2.0		VCC	V	IOH MAX.=+10 UA
VOL	OUTPUT LOW VOLTAGE			0.4	V	3 LSTTL=+1.2MA
VOH	OUTPUT HIGH VOLTAGE	2.4			V	3 LSTTL=-120 UA
VCC	POWER SUPPLY	4.75	5.00	5.25	V	50 MA MAX.

```
PAL16R8   ED KONG
PAL5
WIDGET
12/3/84


RWCKA Y0H Y1H Y2H Y3H DRWL WTGTBL STARTSYNL RDATAH GND
/OEL QAH QBH QCH Q0H Q1H Q2H /ECCWRTL /ECCCLRL VCC

ECCCLRL:=
  STARTSYNL
+/Y3H*/Y2H*/Y1H*/Y0H                            ;STATE 0
+ Y3H* Y2H* Y1H* Y0H                            ;STATE F
+/Y3H* Y2H* Y1H* Y0H                            ;STATE 7
+ Y3H*/Y2H*/Y1H* Y0H                            ;STATE 9
+ Y3H* Y2H*/Y1H* Y0H                            ;STATE D
+ Y3H* Y2H*/Y1H*/Y0H* DRWL*/RDATAH              ;STATE C
+ Y3H* Y2H*/Y1H*/Y0H*/DRWL                      ;STATE C

ECCWRTL:=
  Y3H*/Y2H* Y1H*/Y0H*/Q2H*/Q1H* Q0H* QCH* QBH* QAH*/DRWL;STATE A,1B,P7,WR
+ Y3H*/Y2H* Y1H*/Y0H* Q2H*/Q1H* Q0H* QCH* QBH* QAH* DRWL;STATE A,5B,P7,RD
+ ECCWRTL*/STARTSYNL

/Q2H:=
  Y3H*/Y2H* Y1H*/Y0H*/Q2H*/Q1H
+ Y3H*/Y2H* Y1H*/Y0H*/Q2H* Q1H*/Q0H
+ Y3H*/Y2H* Y1H*/Y0H*/Q2H* Q1H* Q0H*/QCH
+ Y3H*/Y2H* Y1H*/Y0H*/Q2H* Q1H* Q0H* QCH*/QBH
+ Y3H*/Y2H* Y1H*/Y0H*/Q2H* Q1H* Q0H* QCH* QBH*/QAH
+ Y3H*/Y2H* Y1H*/Y0H* Q2H* Q1H* Q0H* QCH* QBH* QAH

/Q1H:=
  Y3H*/Y2H* Y1H*/Y0H*/Q1H*/Q0H
+ Y3H*/Y2H* Y1H*/Y0H*/Q1H* Q0H*/QCH
+ Y3H*/Y2H* Y1H*/Y0H*/Q1H* Q0H* QCH*/QBH
+ Y3H*/Y2H* Y1H*/Y0H*/Q1H* Q0H* QCH* QBH*/QAH
+ Y3H*/Y2H* Y1H*/Y0H* Q1H* Q0H* QCH* QBH* QAH

/Q0H:=
  Y3H*/Y2H* Y1H*/Y0H*/Q0H*/QCH
+ Y3H*/Y2H* Y1H*/Y0H*/Q0H* QCH*/QBH
+ Y3H*/Y2H* Y1H*/Y0H*/Q0H* QCH* QBH*/QAH
+ Y3H*/Y2H* Y1H*/Y0H* Q0H* QCH* QBH* QAH

/QCH:=
 /QCH*/QAH      */STARTSYNL* Y3H*/Y2H* Y1H*/Y0H
+/QCH*/QBH      */STARTSYNL* Y3H*/Y2H* Y1H*/Y0H
+ QCH* QBH* QAH*/STARTSYNL* Y3H*/Y2H* Y1H*/Y0H

/QBH:=
 /QBH*/QAH*/STARTSYNL* Y3H*/Y2H* Y1H*/Y0H
+ QBH* QAH*/STARTSYNL* Y3H*/Y2H* Y1H*/Y0H

/QAH:=
  QAH */STARTSYNL    * Y3H*/Y2H* Y1H*/Y0H
```

DESCRIPTION   THIS PAL IS TO SET UP THE CONTROLLER INTERFACE FOR ERROR
               CORRECTION FUNCTION.
END

ECC PAL EQUATION

```
PAL16R6   ED KONG
PAL6
WIDGET
12/3/84


RWCKA YOH Y1H Y2H Y3H DRWL ECCWRT1L ECCWRTOL RDATAH GND
/OEL NC NC NC NC NC NC /ECCCLRL /ECCWRTL VCC


ECCWRTL=
  ECCWRTOL*/ECCWRT1L
+/ECCWRTOL* ECCWRT1L


ECCCLRL:=
 /Y3H*/Y2H*/Y1H*/YOH                          ; STATE 0
+ Y3H* Y2H* Y1H* YOH                          ; STATE F
+/Y3H* Y2H* Y1H* YOH                          ; STATE 7
+ Y3H*/Y2H*/Y1H* YOH                          ; STATE 9
+ Y3H* Y2H*/Y1H* YOH                          ; STATE D
+ Y3H* Y2H*/Y1H*/YOH* DRWL*/RDATAH            ; STATE C, RD
+ Y3H* Y2H*/Y1H*/YOH*/DRWL                    ; STATE C, WR


DESCRIPTION    THIS PAL IS TO SET UP THE CONTROLLER INTERFACE FOR
               ERROR CORRECTION FUNCTIONS.
END
```
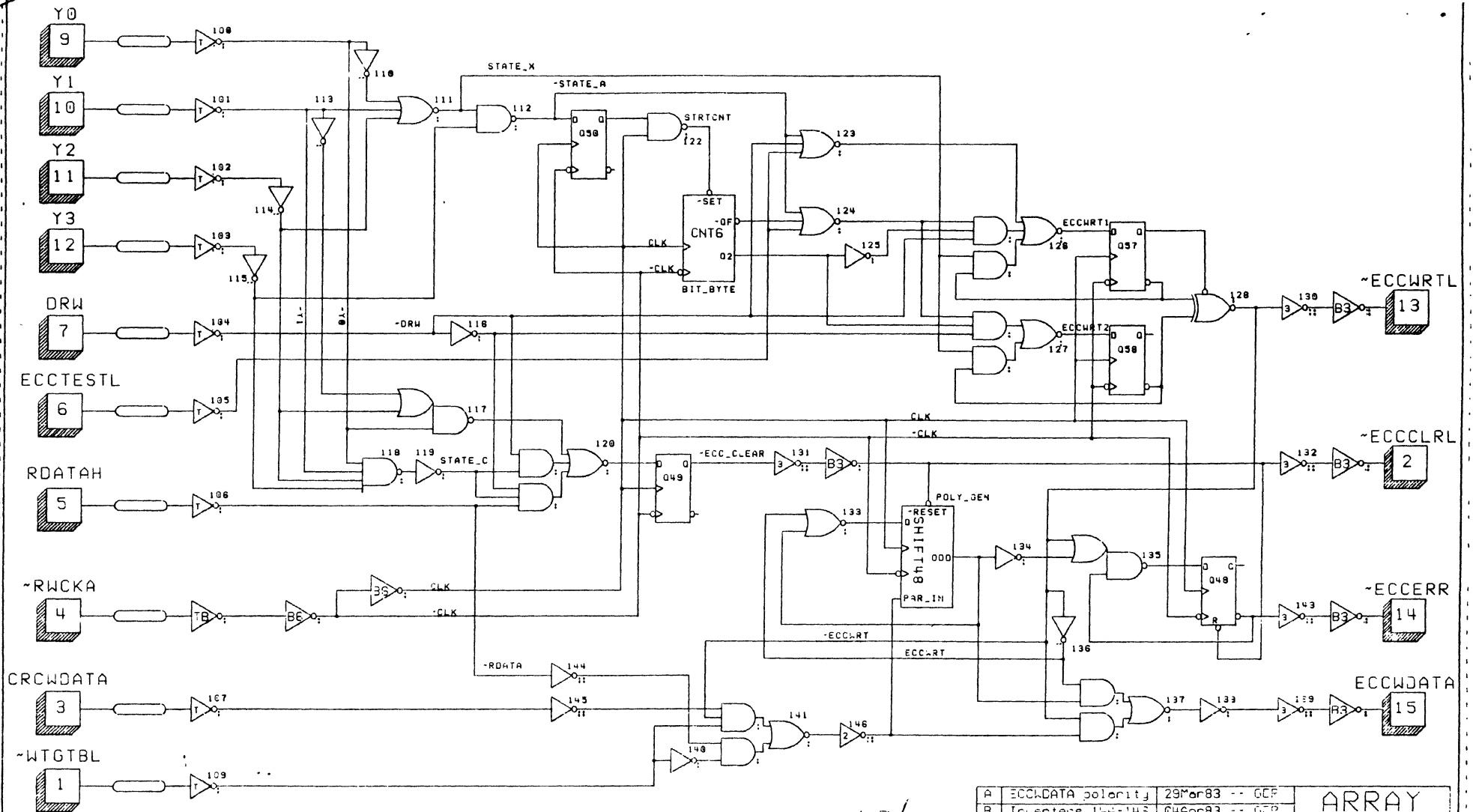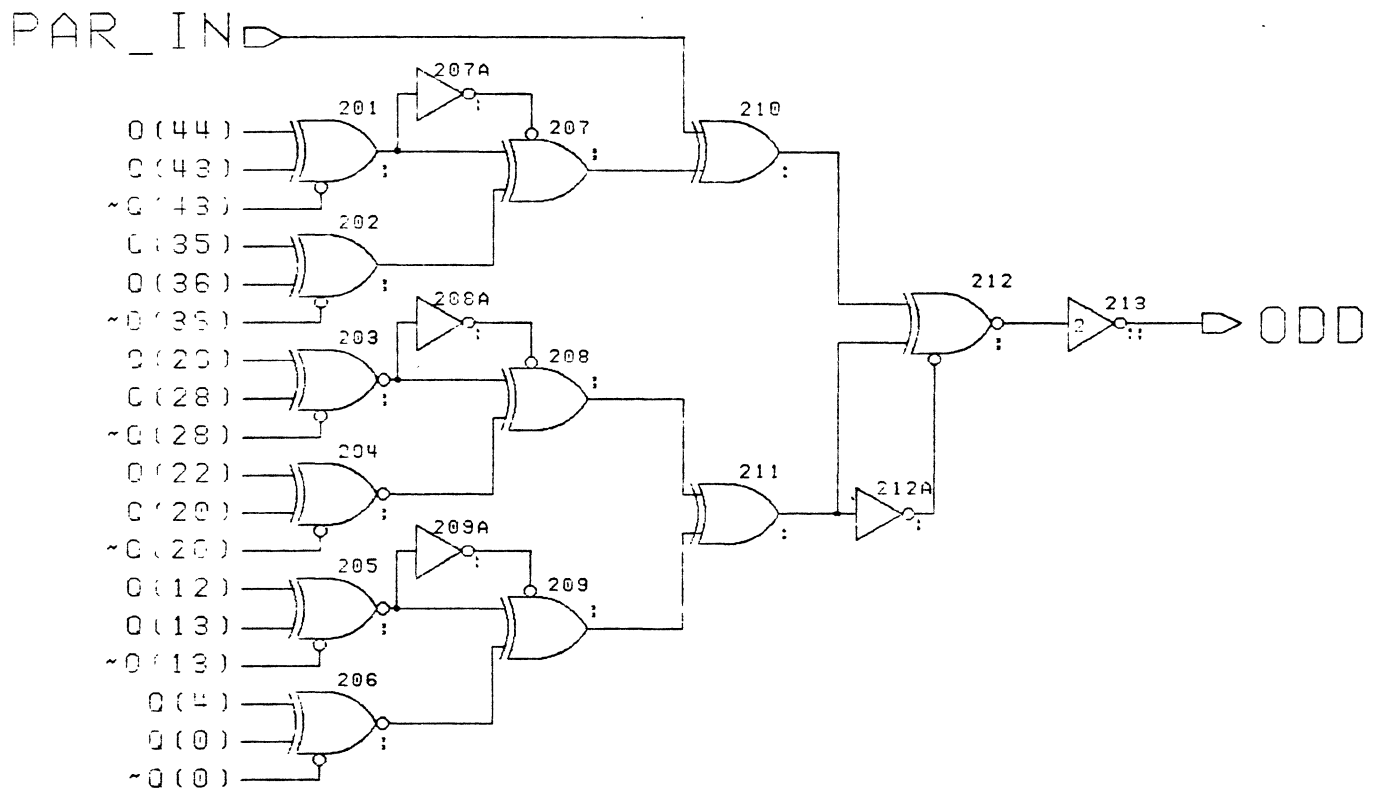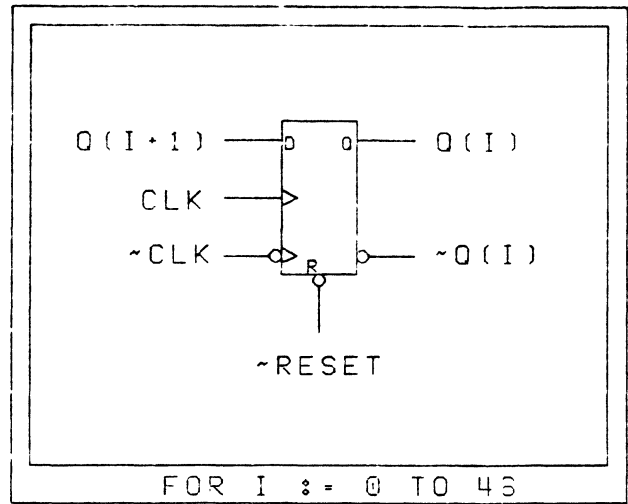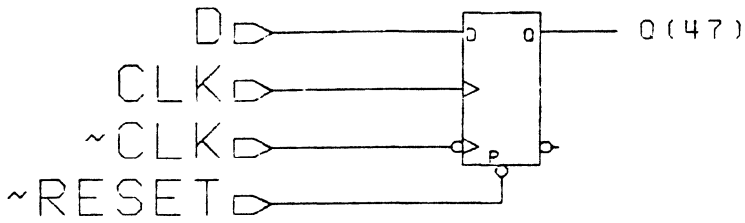
D

CLK

~CLK

~RESET

Q(47)

Q(I+1)   D   Q   Q(I)

CLK

~CLK   R   ~Q(I)

~RESET

FOR I := 0 TO 46

PAR_IN

Q(44)   201
Q(43)   207A
~Q(43)
            202   207   210
Q(35)
Q(36)
~Q(35)
Q(29)   203   208A
Q(28)
~Q(28)
            204   208
Q(22)
Q(20)   212   213
~Q(20)   211   ODD
Q(12)   205   209A
Q(13)
~Q(13)
            206   209   212A
Q(4)
Q(0)
~Q(0)

~QF

~SET

CLK

~CLK

Q2

```
6.1000 E   77   0   0   0   1
6.2000 E   77   0   0   0   1
6.3000 E   77   0   0   0   1
6.4000 E   77   0   0   0   1
6.5000 E   77   0   0   0   1
6.6000 E   77   0   1   0   1
6.7000 E   77   0   0   0   1
6.8000 E   77   0   0   0   1
6.9000 E   77   0   0   0   1
7.0000 E   77   0   1   0   1
7.1000 E   77   0   1   0   1
7.2000 E   77   0   0   0   1
7.3000 E   77   0   0   0   1
7.4000 E   77   0   0   0   1
7.5000 E   77   0   0   0   1
7.6000 E   77   0   1   0   1
7.7000 E   77   0   0   0   1
7.8000 E   77   0   1   0   1
7.9000 E   77   0   1   0   1
8.0000 E   77   0   1   0   1
```

Time ^Y   ^DRW
      ^BB_BUS   ^ECCTESTL
          ^ECCWDATA
          ^POLY_GEN/ODD

	Y
	DRW
	RDATAH
	~RWCKA
	CRCWDATA
	~WTGTBL
	BB_BUS
	~ECCWRTL
	~ECC_CLEAR
	~ECCERR
	ECCWDATA
	POLY_GEN/ODD
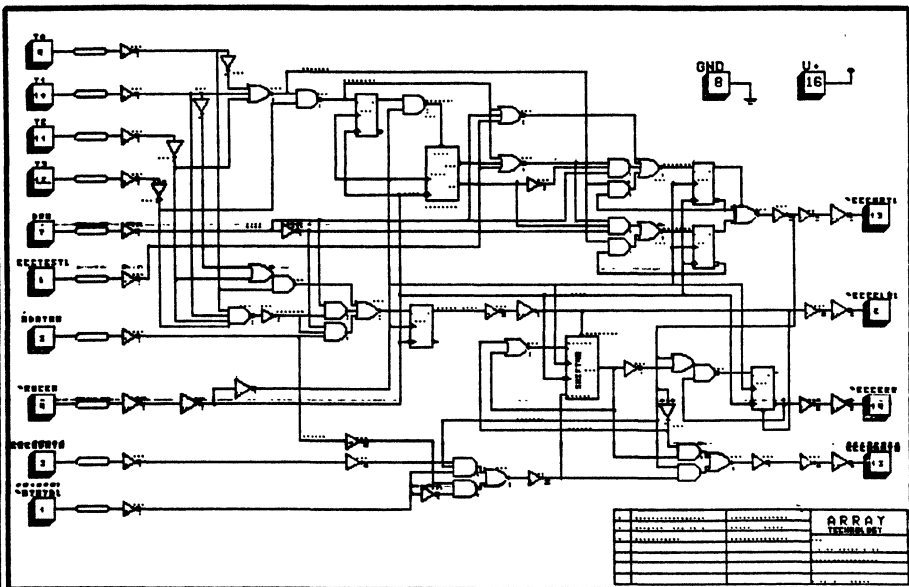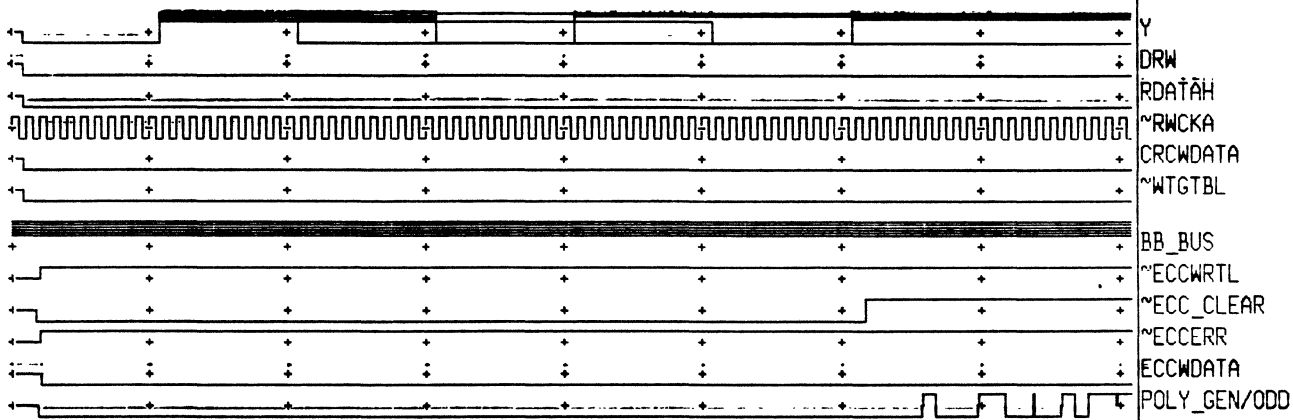
Time / Scale Division: 1:0000 Time: 8:0800

User time scale =   1000.0 Nsec,   Input radix = Hex

GROW Window
MARK -21.16,-13.53
GROW Window
VIEw ALL
HARDcopy

SIM
at top   Travel
Simulation   Display   Analysis
Environmental Imaging   Global

WRITE OPERATION, START (fine res^n).

Time					
7.0000 E	77	0	1	0	1
7.1000 E	77	0	1	0	1
7.2000 E	77	0	0	0	1
7.3000 E	77	0	0	0	1
7.4000 E	77	0	0	0	1
7.5000 E	77	0	0	0	1
7.6000 E	77	0	1	0	1
7.7000 E	77	0	0	0	1
7.8000 E	77	0	1	0	1
7.9000 E	77	0	1	0	1
8.0000 E	77	0	1	0	1
8.1000 E	77	0	1	0	1
8.2000 E	77	0	1	0	1
8.3000 E	77	0	1	0	1
8.4000 E	77	0	1	0	1
8.5000 E	77	0	0	0	1
8.6000 E	77	0	1	0	1
8.7000 E	77	0	0	0	1
8.8000 E	77	0	1	0	1
8.9000 E	77	0	1	0	1
9.0000 E	77	0	1	0	1
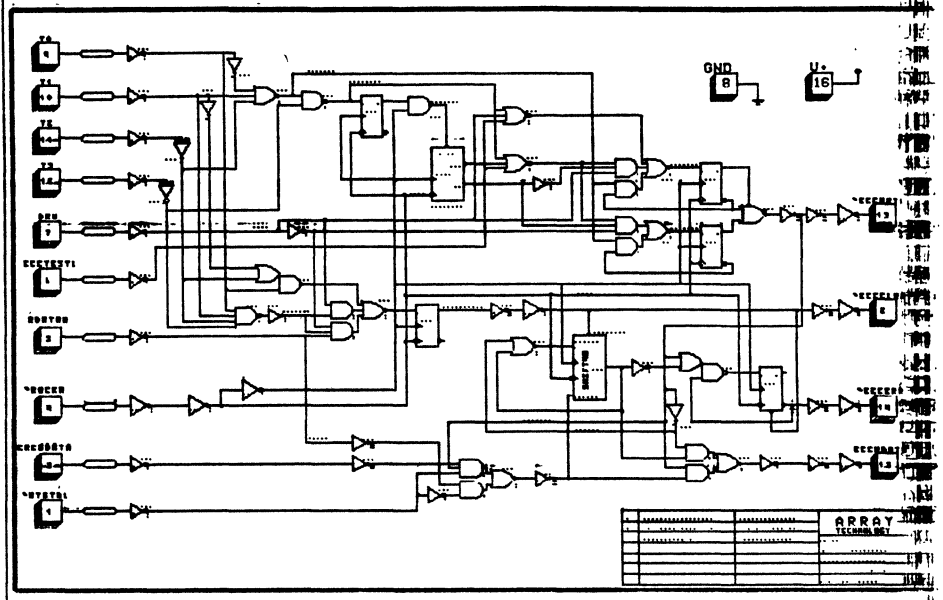
```
Time ^Y              ^DRW
      ^BB_BUS        ^ECCTESTL
          ^ECCWDATA
          ^POLY_GEN/ODD
```

Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL

BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division:	0.5000	Time:	9.0800
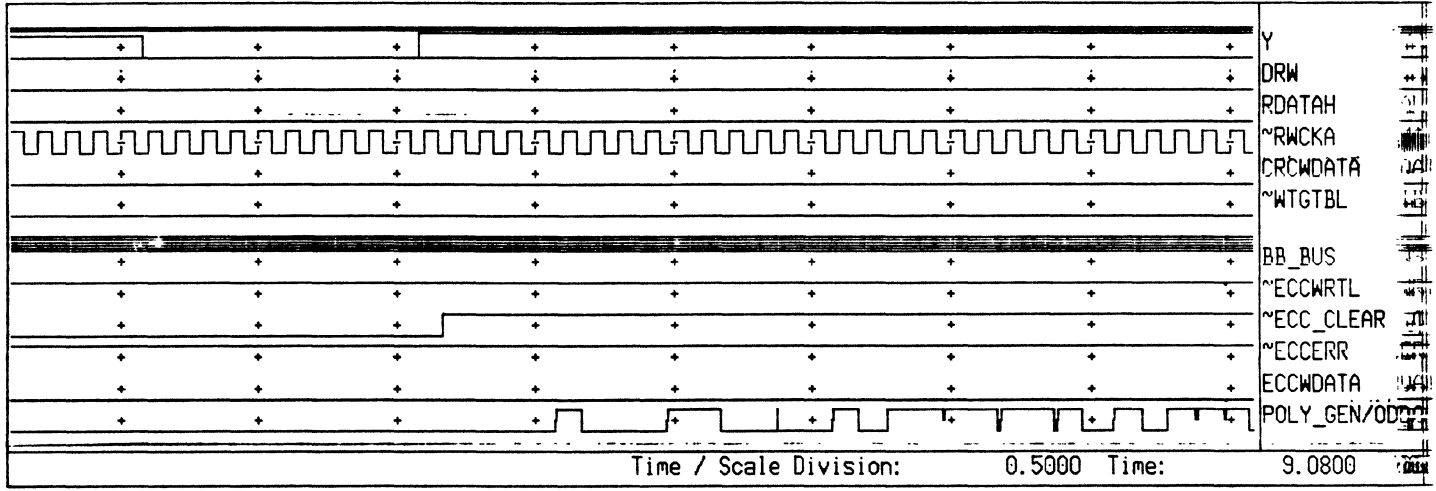
User time scale =   1000.0 Nsec,   Input radix = Hex

```
VIEw ALL
HARDcopy
SCAle TRace Time .5
RUN 1
HARDcopy
```

SIM

at top   Travel
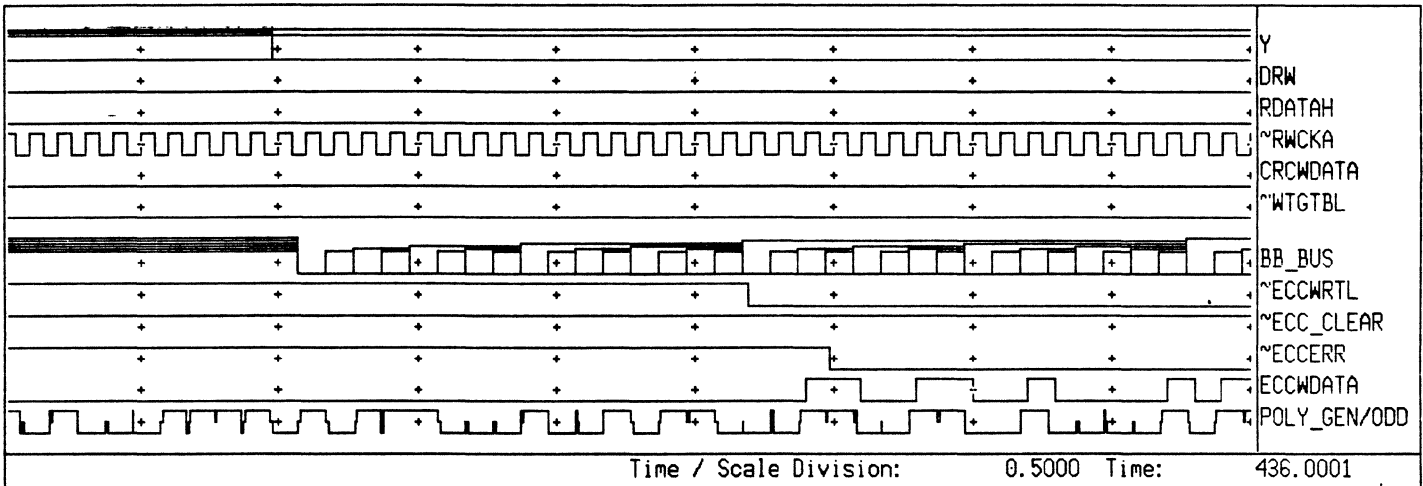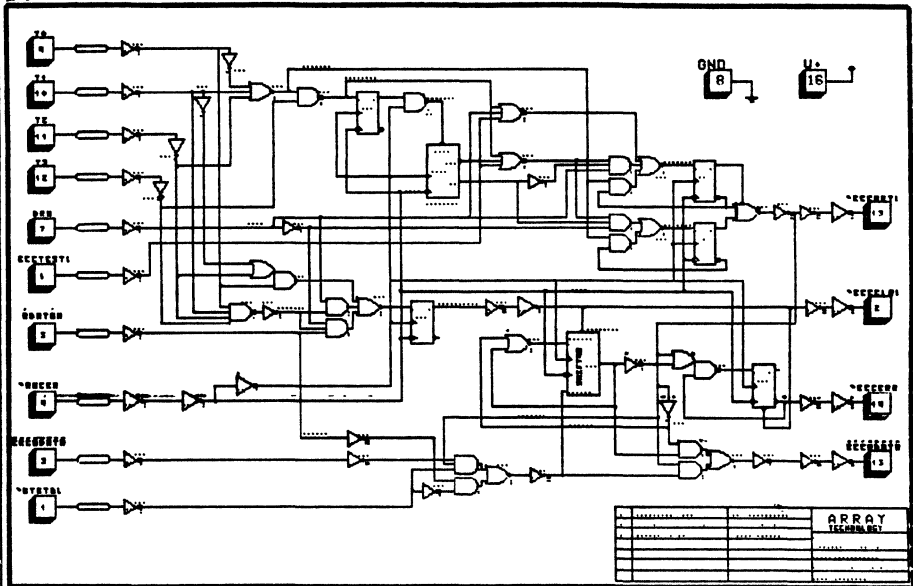Simulation   Display   Analysis
Environmental   Imaging   Global

WRITE - OPERATION, FINISH (Part 1)

```
432.1000 E 77  0  1  0  1
432.2000 E 77  0  1  0  1
432.3000 E 77  0  1  0  1
432.4000 E 77  0  1  0  1
432.5000 A 77  0  0  0  1
432.6000 A 00  0  1  0  1
432.7000 A 01  0  0  0  1
432.8000 A 02  0  1  0  1
432.9000 A 03  0  1  0  1
433.0000 A 04  0  1  0  1
433.1000 A 05  0  0  0  1
433.2000 A 06  0  1  0  1
433.3000 A 07  0  0  0  1
433.4000 A 10  0  1  0  1
433.5000 A 11  0  0  0  1
433.6000 A 12  0  0  0  1
433.7000 A 13  0  1  0  1
433.8000 A 14  0  0  0  1
433.9000 A 15  0  1  0  1
434.0000 A 16  0  1  0  1
```

```
      Time ^Y            ^DRW
           ^BB_BUS            ^ECCTESTL
              ^ECCWDATA
                 ^POLY_GEN/ODD
```


Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division: 0.5000   Time: 436.0001
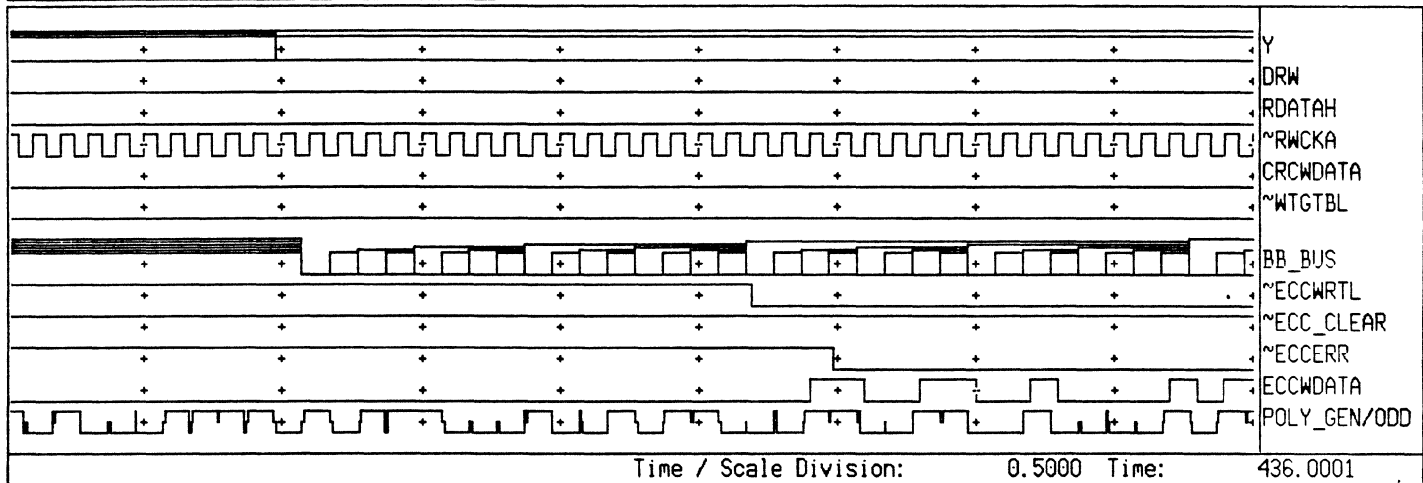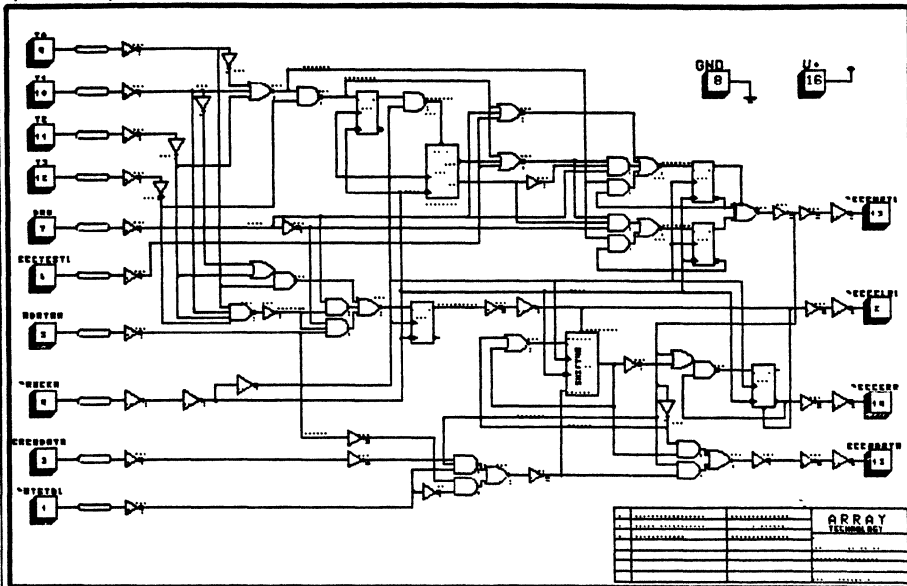
User time scale =   1000.0 Nsec,   Input radix = Hex

```
MARK
GROW Window 0,0
MARK
GROW Window
HARDcopy
```

SIM

at top
Simulation   Display   Analysis
Environmental   Imaging   Global

Travel

WRITE OPERATION, FINISH (part-2)

```
434.1000 A  17  0  0  0  1
434.2000 A  20  0  0  0  1
434.3000 A  21  0  0  0  1
434.4000 A  22  0  1  0  1
434.5000 A  23  1  1  0  1
434.6000 A  24  0  0  0  1
434.7000 A  25  0  0  0  1
434.8000 A  26  1  1  0  1
434.9000 A  27  1  1  0  1
435.0000 A  30  1  0  0  1
435.1000 A  31  0  0  0  1
435.2000 A  32  1  1  0  1
435.3000 A  33  0  0  0  1
435.4000 A  34  0  0  0  1
435.5000 A  35  0  0  0  1
435.6000 A  36  0  0  0  1
435.7000 A  37  0  1  0  1
435.8000 A  40  1  0  0  1
435.9000 A  41  1  1  0  1
436.0000 A  42  1  1  0  1
```

```
        Time ^Y              ^DRW
          ^BB_BUS        ^ECCTESTL
              ^ECCWDATA
                ^POLY_GEN/ODD
```

Waveform traces:

```
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD
```

Time / Scale Division: 0.5000   Time: 436.0001

User time scale =   1000.0 Nsec, Input radix = Hex

```
HARDcopy
VIEw Time Trace 436 -Absolute
VIEw Time List 436
VIEw Time List 436 -Absolute
HARDcopy
```
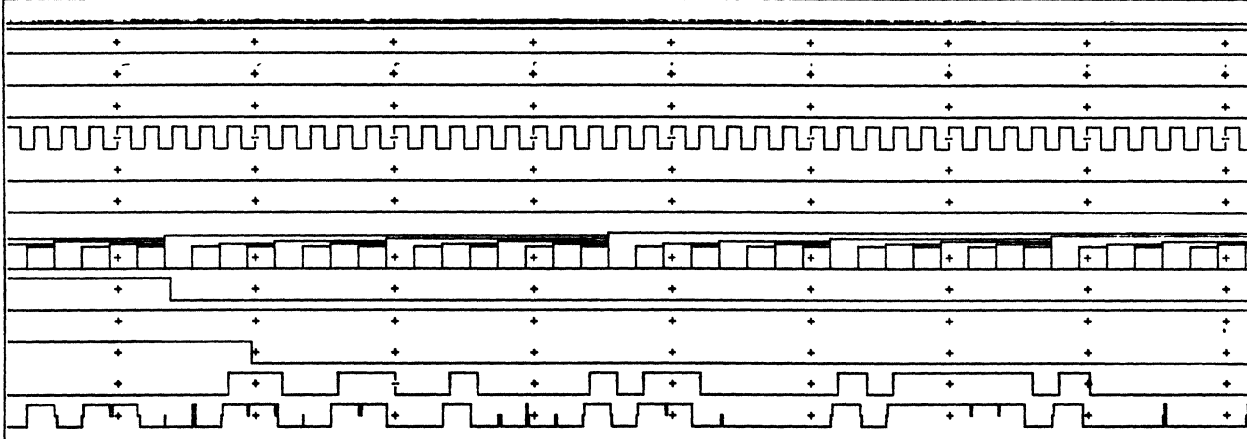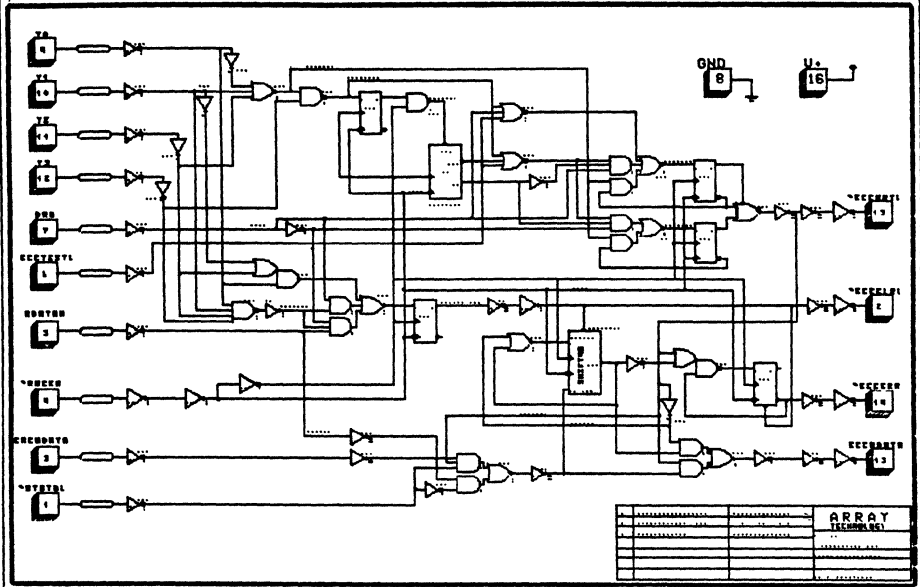
```
                              SIM
at top                                        Travel
   Simulation      Display         Analysis
   Environmental   Imaging         Global
```

WRITE OPERATION, FINISH (Part 3)

Time					
436.0000	A	42	1	1	0	1
436.1000	A	43	1	0	0	1
436.2000	A	44	0	0	0	1
436.3000	A	45	1	0	0	1
436.4000	A	46	0	0	0	1
436.5000	A	47	0	0	0	1
436.6000	A	50	1	1	0	1
436.7000	A	51	1	0	0	1
436.8000	A	52	1	1	0	1
436.9000	A	53	1	1	0	1
437.0000	A	54	1	1	0	1
437.1000	A	55	1	1	0	1
437.2000	A	56	1	1	0	1
437.3000	A	57	1	0	0	1
437.4000	A	60	1	1	0	1
437.5000	A	61	1	0	0	1
437.6000	A	62	0	0	0	1
437.7000	A	63	0	0	0	1
437.8000	A	64	0	0	0	1
437.9000	A	65	0	0	0	1
438.0000	A	66	0	0	0	1

```
Time ^Y               ^DRW
      ^BB_BUS         ^ECCTESTL
        ^ECCWDATA
          ^POLY_GEN/ODD
```


GND 8   U+ 16

ARRAY TECHNOLOGY

Waveform labels:
```
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD
```

Time / Scale Division: 0.5000   Time: 438.0800

User time scale =   1000.0 Nsec,   Input radix = Hex

```
SAVe STAte write.430
? Error: File already exists, use -Replace switch to overwrite (fr
SAVe STAte write.430 -Replace
RUN 8
HARDcopy
```

SIM

at top   Travel
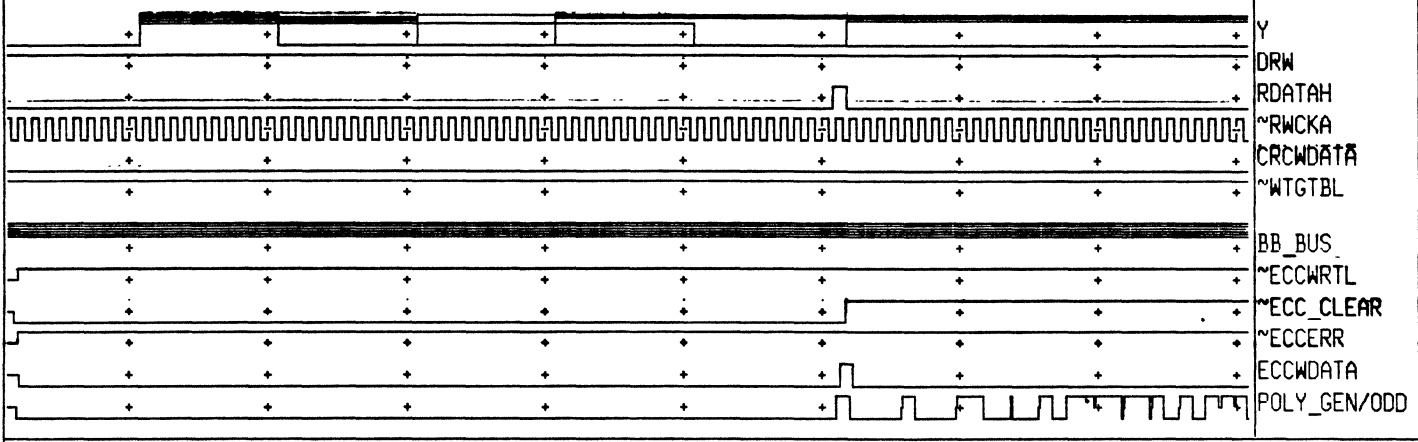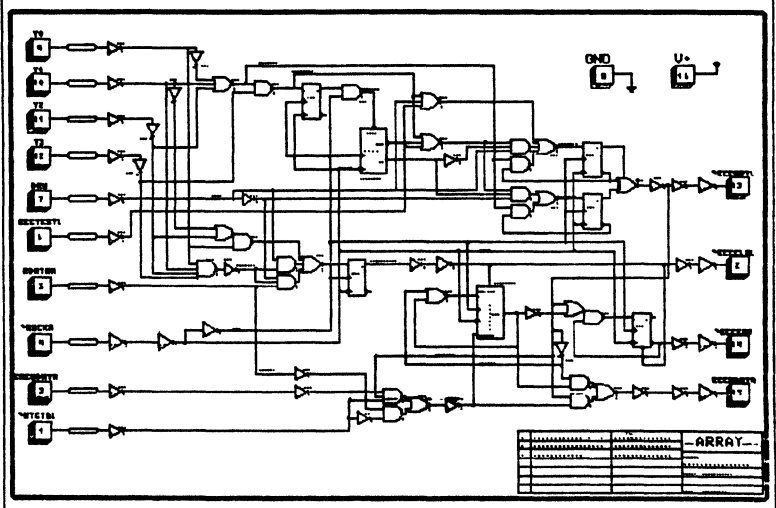Simulation   Display   Analysis
Environmental Imaging   Global

Job: V80.V.PETER.HARDCOPY

Enqueued: 4/08/1983 7:55 pm (pst)
Printed: 4/08/1983 7:56 pm (pst)

```
7.1000 E  77  0  1  1  1
7.2000 E  77  0  0  1  1
7.3000 E  77  0  0  1  1
7.4000 E  77  0  0  1  1
7.5000 E  77  0  0  1  1
7.6000 E  77  0  1  1  1
7.7000 E  77  0  0  1  1
7.8000 E  77  0  1  1  1
7.9000 E  77  0  1  1  1
8.0000 E  77  0  1  1  1
8.1000 E  77  0  1  1  1
8.2000 E  77  0  1  1  1
8.3000 E  77  0  1  1  1
8.4000 E  77  0  1  1  1
8.5000 E  77  0  0  1  1
8.6000 E  77  0  1  1  1
8.7000 E  77  0  0  1  1
8.8000 E  77  0  1  1  1
8.9000 E  77  0  1  1  1
9.0000 E  77  0  1  1  1
```

```
Time ^Y          ^DRW
   ^BB_BUS        ^ECCTESTL
       ^ECCWDATA
          ^POLY_GEN/ODD
```

Signal traces (right labels):
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division: 1.0000   Time: 9.0800

User time scale =   1000.0 Nsec,   Input radix = Hex

```
FORCe CRCWDATA 0 0
Note: Application windows cannot be displayed now.
     Try again by pressing RETURN. (from Idea/Queue manager 0003)
RUN 9
HARDcopy
```
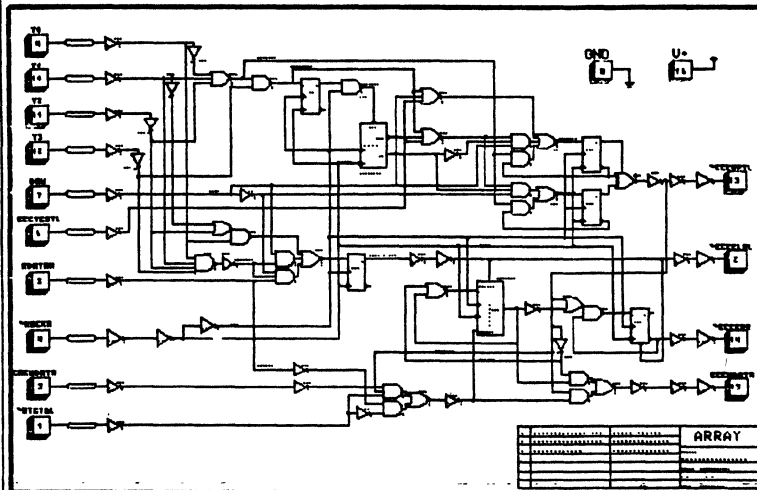
SIM

at top   Travel
Simulation   Display   Analysis
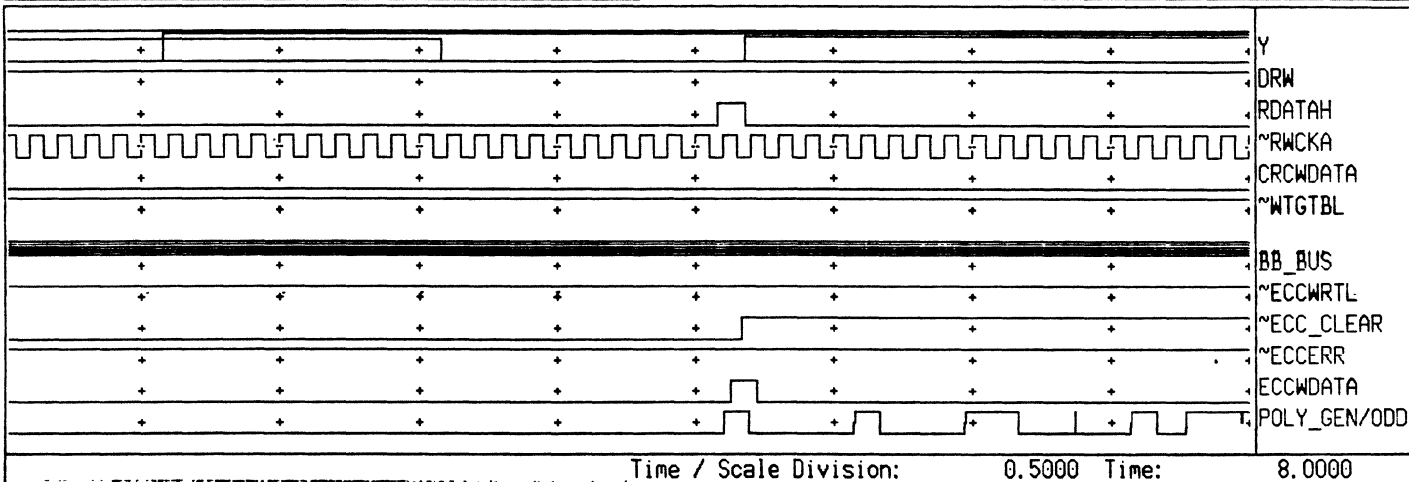Environmental   Imaging   Global

Job: V00.V.PETER.HARDCOPY

Enqueued: 4/08/1983 9:38 pm (pst)
Printed: 4/08/1983 9:39 pm (pst)

```
6.1000 C 77 0 0 1 1
6.2000 E 77 1 0 1 1
6.3000 E 77 0 0 1 1
6.4000 E 77 0 0 1 1
6.5000 E 77 0 0 1 1
6.6000 E 77 0 1 1 1
6.7000 E 77 0 0 1 1
6.8000 E 77 0 0 1 1
6.9000 E 77 0 0 1 1
7.0000 E 77 0 1 1 1
7.1000 E 77 0 1 1 1
7.2000 E 77 0 0 1 1
7.3000 E 77 0 0 1 1
7.4000 E 77 0 0 1 1
7.5000 E 77 0 0 1 1
7.6000 E 77 0 1 1 1
7.7000 E 77 0 0 1 1
7.8000 E 77 0 1 1 1
7.9000 E 77 0 1 1 1
8.0000 E 77 0 1 1 1
```

Time ^Y   ^DRW
    ^BB_BUS   ^ECCTESTL
      ^ECCWDATA
       ^POLY_GEN/ODD

ARRAY

Waveform labels (right side):
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division: 0.5000   Time: 8.0000

User time scale = 1000.0 Nsec,   Input radix = Hex

SAVe STAte write,430 -Replace
VIEw Time Trace 8
VIEw Time Trace 8 -Absolute
VIEw Time List 8 -Absolute
HARDcopy

SIM
at top   travel
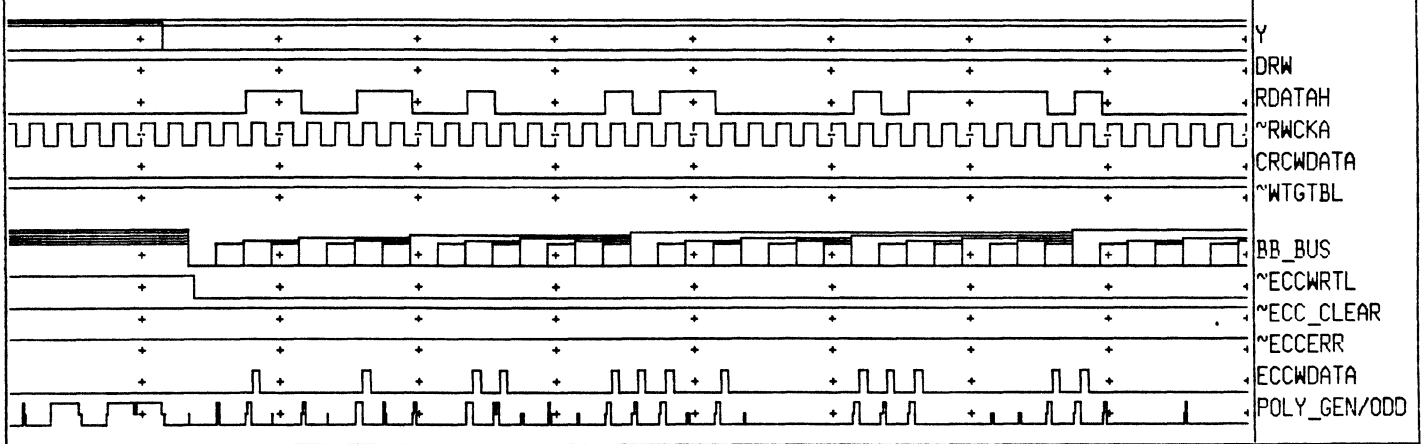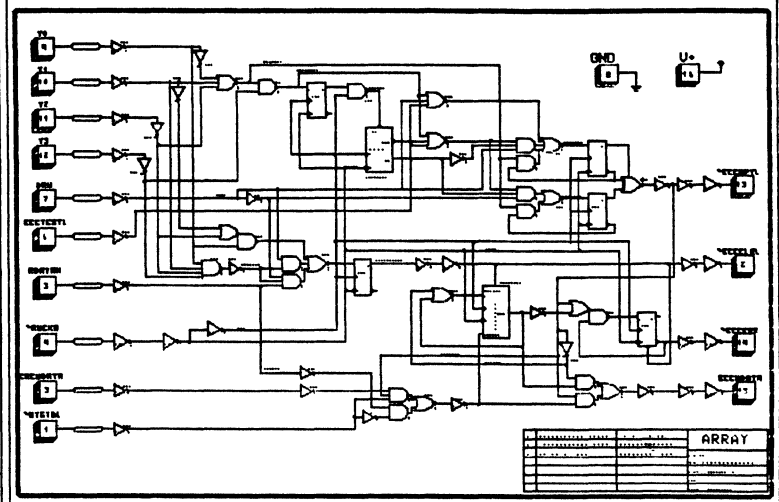Simulation   Display   Analysis
Environmental Imaging   Global

Job: V80.V.PETER.HARDCOPY

Enqueued: 4/08/1983 9:44 pm (pst)
Printed: 4/08/1983 9:45 pm (pst)

```
434.0000 E  77  0  1  1  1
434.1000 A  77  0  0  1  1
434.2000 A  00  0  0  1  1
434.3000 A  01  0  0  1  1
434.4000 A  02  0  0  1  1
434.5000 A  03  0  0  1  1
434.6000 A  04  0  0  1  1
434.7000 A  05  0  0  1  1
434.8000 A  06  1  0  1  1
434.9000 A  07  0  0  1  1
435.0000 A  10  0  0  1  1
435.1000 A  11  0  0  1  1
435.2000 A  12  1  0  1  1
435.3000 A  13  1  0  1  1
435.4000 A  14  0  0  1  1
435.5000 A  15  0  0  1  1
435.6000 A  16  0  0  1  1
435.7000 A  17  0  0  1  1
435.8000 A  20  1  0  1  1
435.9000 A  21  1  0  1  1
```

Time ^Y   ^DRW
    ^BB_BUS   ^ECCTESTL
     ^ECCWDATA
      ^POLY_GEN/ODD

Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division: 0.5000 Time: 438.0010

User time scale =   1000.0 Nsec, Input radix = Hex
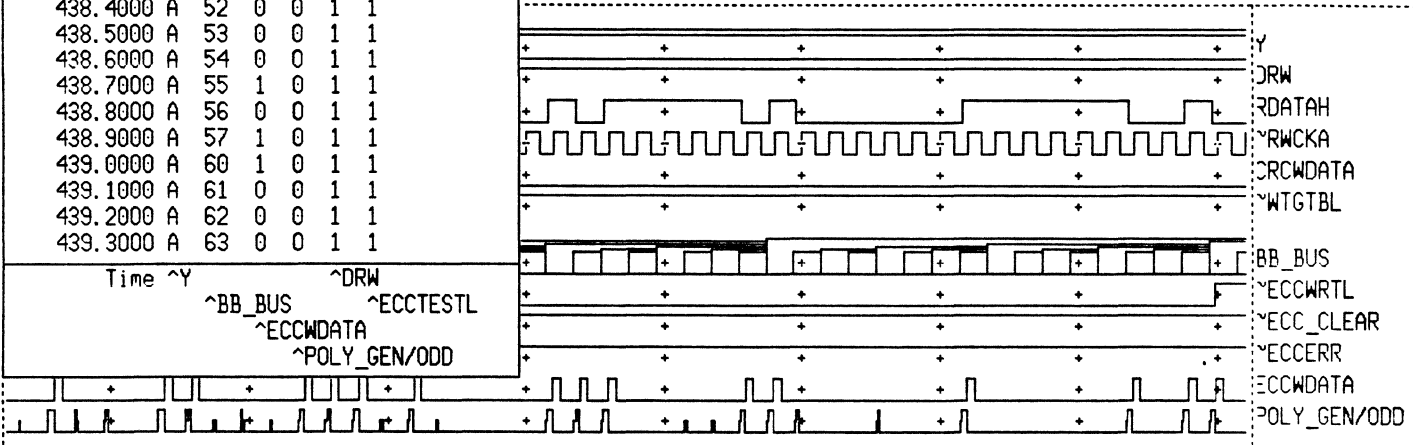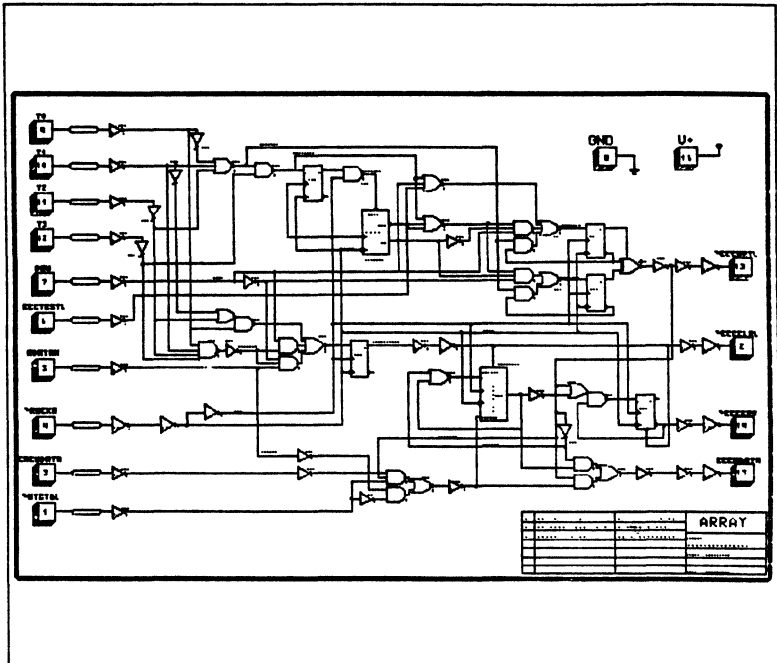
VIEw Time List 437
VIEw Time List 437 -Absolute
VIEw Time List 436 -Absolute
VIEw Time List -.1
HARDcopy

SIM
at top   Travel
 Simulation   Display   Analysis
 Environmental Imaging   Global

Job: V80.V.PETER.HARDCOPY

Enqueued: 4/08/1983 9:47 pm (pst)
Printed: 4/08/1983 9:48 pm (pst)

```
435.9000 A  21  1  0  1  1
436.0000 A  22  0  0  1  1
436.1000 A  23  1  0  1  1
436.2000 A  24  0  0  1  1
436.3000 A  25  0  0  1  1
436.4000 A  26  0  0  1  1
436.5000 A  27  0  0  1  1
436.6000 A  30  1  0  1  1
436.7000 A  31  1  0  1  1
436.8000 A  32  1  0  1  1
436.9000 A  33  0  0  1  1
437.0000 A  34  0  0  1  1
437.1000 A  35  0  0  1  1
437.2000 A  36  0  0  1  1
437.3000 A  37  1  0  1  1
437.4000 A  40  1  0  1  1
437.5000 A  41  0  0  1  1
437.6000 A  42  0  0  1  1
437.7000 A  43  0  0  1  1
437.8000 A  44  0  0  1  1
437.9000 A  45  0  0  1  1
438.0000 A  46  0  0  1  1
438.1000 A  47  1  0  1  1
438.2000 A  50  0  0  1  1
438.3000 A  51  0  0  1  1
438.4000 A  52  0  0  1  1
438.5000 A  53  0  0  1  1
438.6000 A  54  0  0  1  1
438.7000 A  55  1  0  1  1
438.8000 A  56  0  0  1  1
438.9000 A  57  1  0  1  1
439.0000 A  60  1  0  1  1
439.1000 A  61  0  0  1  1
439.2000 A  62  0  0  1  1
439.3000 A  63  0  0  1  1
```

```
Time ^Y              ^DRW
      ^BB_BUS           ^ECCTESTL
        ^ECCWDATA
           ^POLY_GEN/ODD
```


Trace labels (right side):
^Y
^DRW
^RDATAH
^RWCKA
^CRCWDATA
^WTGTBL
^BB_BUS
^ECCWRTL
^ECC_CLEAR
^ECCERR
^ECCWDATA
^POLY_GEN/ODD

Time / Scale Division: 0.5000 Time: 439.1010

User time scale =   1000.0 Nsec, Input radix = Hex

```
VIEw Time Trace 1
VIEw Time Trace .1
MARK
GROW Window 0,0
HARDcopy
```

SIM
at top   Travel
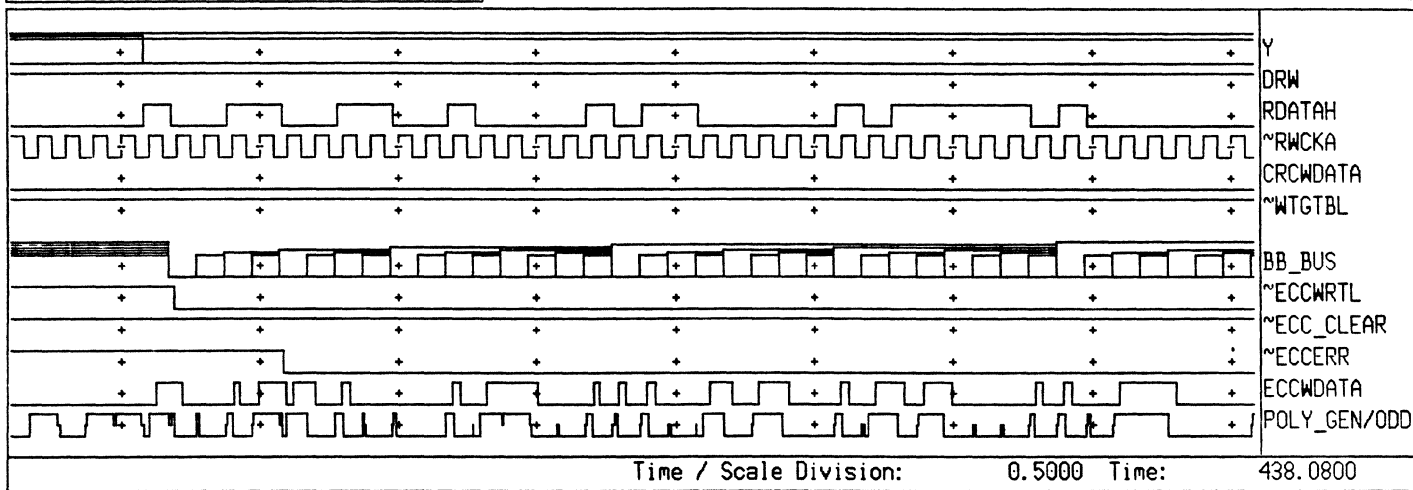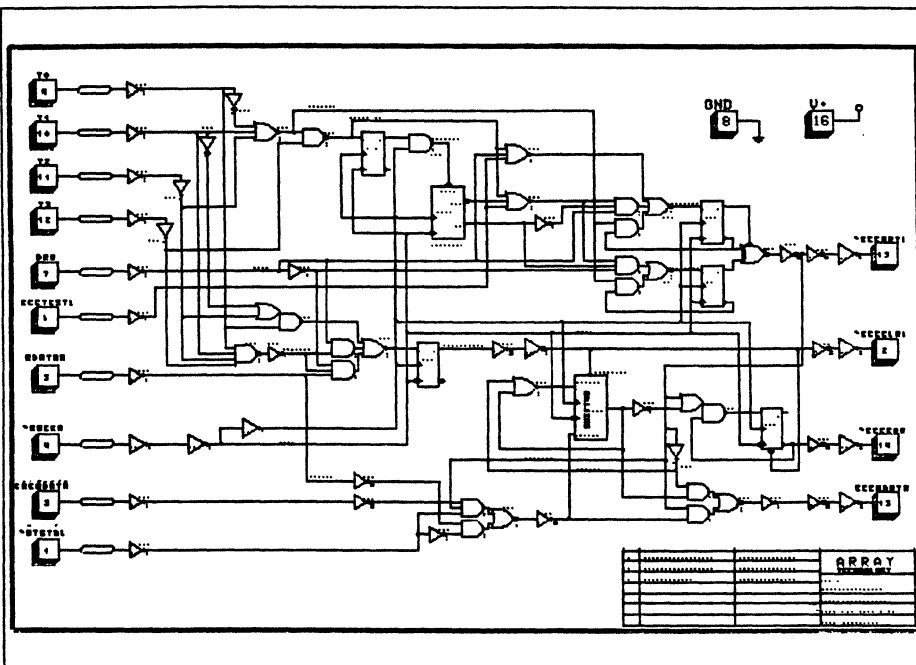Simulation   Display   Analysis
Environmental Imaging   Global

Job: V8Ø.V.PETER.HARDCOPY

Enqueued: 4/Ø8/1983 9:52 pm (pst)
Printed: 4/Ø8/1983 9:53 pm (pst)

```
439.7000 A 67 0 0 1 1
439.8000 A 70 0 1 1 1
439.9000 A 71 0 1 1 1
440.0000 A 72 0 0 1 1
440.1000 A 73 0 0 1 1
440.2000 A 74 0 0 1 1
440.3000 A 75 0 0 1 1
440.4000 A 76 0 1 1 1
440.5000 A 77 0 0 1 1
440.6000 A 00 0 1 1 1
440.7000 A 01 0 1 1 1
440.8000 A 02 0 1 1 1
440.9000 A 03 0 1 1 1
441.0000 A 04 0 1 1 1
441.1000 A 05 0 1 1 1
441.2000 A 06 0 1 1 1
441.3000 2 07 0 0 1 1
441.4000 2 77 0 1 1 1
441.5000 2 77 0 0 1 1
441.6000 2 77 0 1 1 1
441.7000 2 77 0 1 1 1
441.8000 2 77 0 1 1 1
441.9000 2 77 0 0 1 1
442.0000 2 77 0 1 1 1
```

Time ^Y   ^DRW
      ^BB_BUS   ^ECCTEST
        ^ECCWDATA
        ^POLY_GEN/ODD

Waveform labels (right side):
- Y
- DRW
- RDATAH
- RWCKA
- RCWDATA
- WTGTBL
- BB_BUS
- ECCWRTL
- ECC_CLEAR
- ECCERR
- ECCWDATA
- POLY_GEN/ODD

Time / Scale Division: 0.5000 Time: 442.0800

User time scale =   1000.0 Nsec, Input radix = Hex

```
GROW Window 0,0
MARK -21.95, -15.87
GROW Window
VIEw ALL
HARDcopy
```

SIM

at top   Travel
Simulation   Display   Analysis
Environmental Imaging   Global

Job: V80.V.PETER.HARDCOPY

Enqueued: 4/08/1983 10:07 pm (pst)
Printed: 4/08/1983 10:09 pm (pst)

434.2000	A	00	1	0	1	1
434.3000	A	01	0	0	1	1
434.4000	A	02	0	0	1	1
434.5000	A	03	1	1	1	1
434.6000	A	04	0	1	1	1
434.7000	A	05	1	0	1	1
434.8000	A	06	1	0	1	1
434.9000	A	07	0	0	1	1
435.0000	A	10	0	0	1	1
435.1000	A	11	0	0	1	1
435.2000	A	12	1	0	1	1
435.3000	A	13	0	1	1	1
435.4000	A	14	1	1	1	1
435.5000	A	15	1	0	1	1
435.6000	A	16	0	0	1	1
435.7000	A	17	0	0	1	1
435.8000	A	20	1	0	1	1
435.9000	A	21	1	0	1	1
436.0000	A	22	0	0	1	1
436.1000	A	23	0	1	1	1
436.2000	A	24	1	0	1	1

Time   ^Y   ^DRW
      ^BB_BUS   ^ECCTEST
        ^ECCWDATA
         ^POLY_GEN/ODD

Waveform labels:
- Y
- DRW
- RDATAH
- ~RWCKA
- CRCWDATA
- ~WTGTBL
- BB_BUS
- ~ECCWRTL
- ~ECC_CLEAR
- ~ECCERR
- ECCWDATA
- POLY_GEN/ODD

Time / Scale Division: 0.5000   Time: 438.0800

User time scale =   1000.0 Nsec,   Input radix = Hex

Current time =   430.0800
FORCe rdatah 1 434.08 -Absolute
FORCe rdatah 0 434.18 -Absolute
RUN 8
HARDcopy

SIM
at top   Travel
Simulation   Display   Analysis
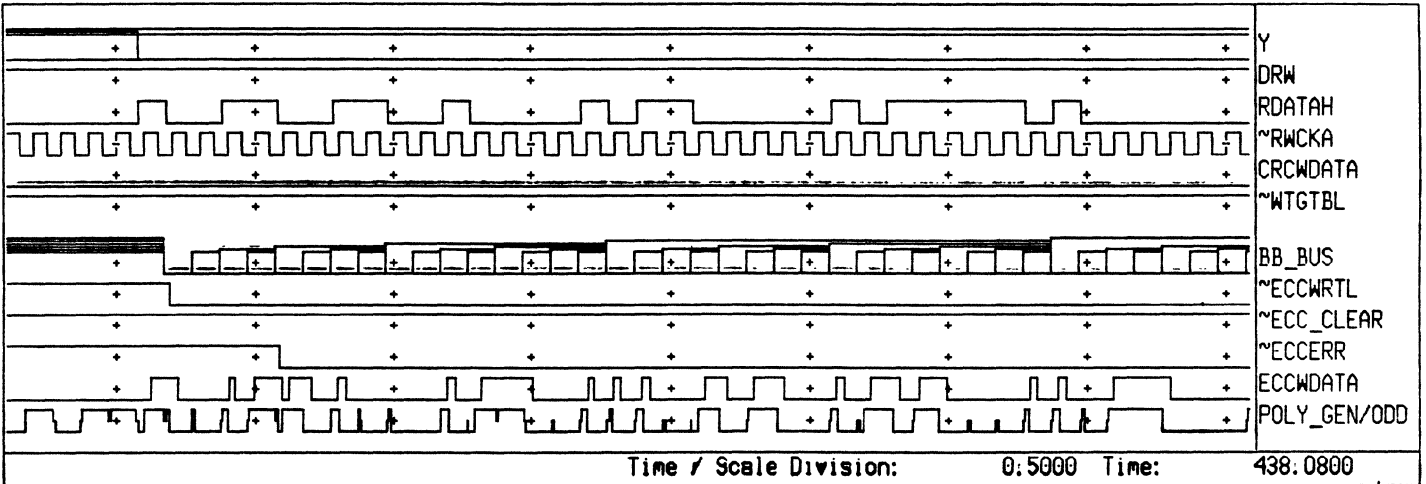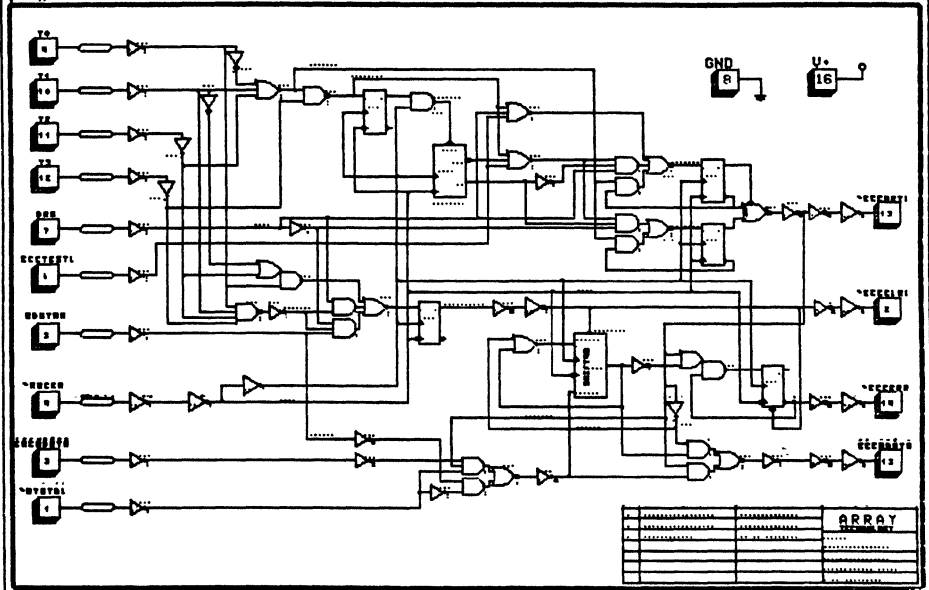Environmental   Imaging   Global

READ OPERATION, W ERROR in CRC byte, FINISH part 2.

436.ØØØØ A	22	Ø	Ø	1	1
436.1ØØØ A	23	Ø	1	1	1
436.2ØØØ A	24	1	Ø	1	1
436.3ØØØ A	25	1	1	1	1
436.4ØØØ A	26	1	Ø	1	1
436.5ØØØ A	27	Ø	Ø	1	1
436.6ØØØ A	30	1	Ø	1	1
436.7ØØØ A	31	Ø	1	1	1
436.8ØØØ A	32	1	Ø	1	1
436.9ØØØ A	33	1	1	1	1
437.ØØØØ A	34	Ø	Ø	1	1
437.1ØØØ A	35	Ø	Ø	1	1
437.2ØØØ A	36	Ø	Ø	1	1
437.3ØØØ A	37	1	Ø	1	1
437.4ØØØ A	40	1	Ø	1	1
437.5ØØØ A	41	Ø	Ø	1	1
437.6ØØØ A	42	1	1	1	1
437.7ØØØ A	43	1	1	1	1
437.8ØØØ A	44	1	Ø	1	1
437.9ØØØ A	45	Ø	Ø	1	1
438.ØØØØ A	46	Ø	Ø	1	1

```
        Time ^Y              ^DRW
            ^BB_BUS          ^ECCTEST
              ^ECCWDATA ----.----
                  ^POLY_GEN/ODD
```

Waveform labels:
```
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD
```

Time / Scale Division: Ø:5ØØØ Time: 438.Ø8ØØ

User time scale =   1ØØØ.Ø Nsec,   Input radix = Hex

FORCe rdatah 1 434.Ø8 -Absolute
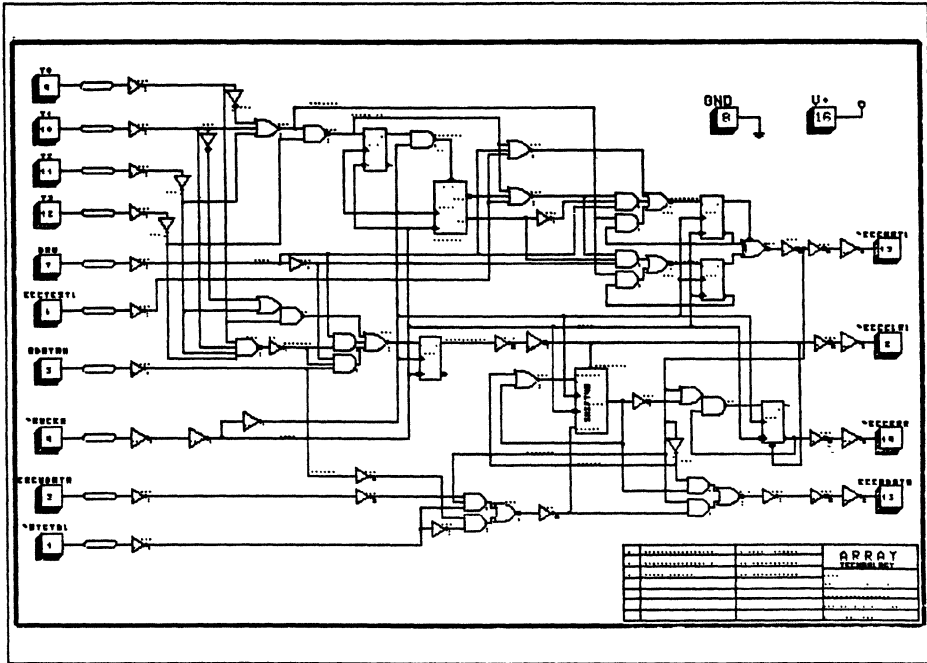FORCe rdatah Ø 434.18 -Absolute
RUN 8
HARDcopy
HARDcopy

SIM
at top   Travel
Simulation   Display   Analysis
Environmental   Imaging   Global

READ w CRC double error, FINISH, part 3

437.2000	A	36	0	0	1	1
437.3000	A	37	1	0	1	1
437.4000	A	40	1	0	1	1
437.5000	A	41	0	0	1	1
437.6000	A	42	1	1	1	1
437.7000	A	43	1	1	1	1
437.8000	A	44	1	0	1	1
437.9000	A	45	0	0	1	1
438.0000	A	46	0	0	1	1
438.1000	A	47	1	0	1	1
438.2000	A	50	0	0	1	1
438.3000	A	51	0	0	1	1
438.4000	A	52	0	0	1	1
438.5000	A	53	1	1	1	1
438.6000	A	54	0	0	1	1
438.7000	A	55	1	0	1	1
438.8000	A	56	0	0	1	1
438.9000	A	57	0	0	1	1
439.0000	A	60	1	0	1	1
439.1000	A	61	0	0	1	1
439.2000	A	62	0	0	1	1
439.3000	A	63	0	0	1	1
439.4000	A	64	0	1	1	1
439.5000	A	65	0	0	1	1
439.6000	A	66	0	0	1	1
439.7000	A	67	0	0	1	1
439.8000	A	70	0	1	1	1
439.9000	A	71	0	1	1	1
440.0000	A	72	0	0	1	1

Time ^Y   ^DRW
      ^BB_BUS   ^ECCTES
        ^ECCWDATA
          ^POLY_GEN/ODD
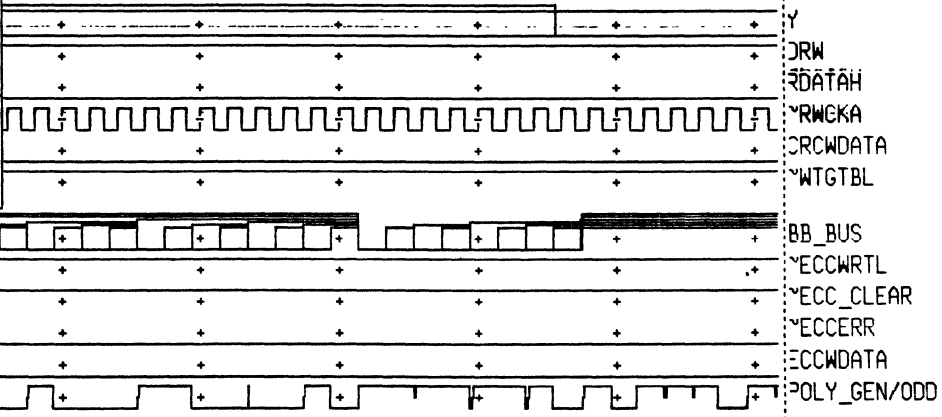
Y
DRW
RDATAH
RWCKA
CRCWDATA
WTGTBL
BB_BUS
ECCWRTL
ECC_CLEAR
ECCERR
ECCWDATA
POLY_GEN/ODD

Time / Scale Division: 0.5000 Time: 442.0800

User time scale =   1000.0 Nsec;   Input radix = Hex

GROW Window 0,0
VIEw Time List 438
VIEw Time List 438 -Absolute
VIEw Time List 440 -Absolute
HARDcopy

SIM
at top   Travel
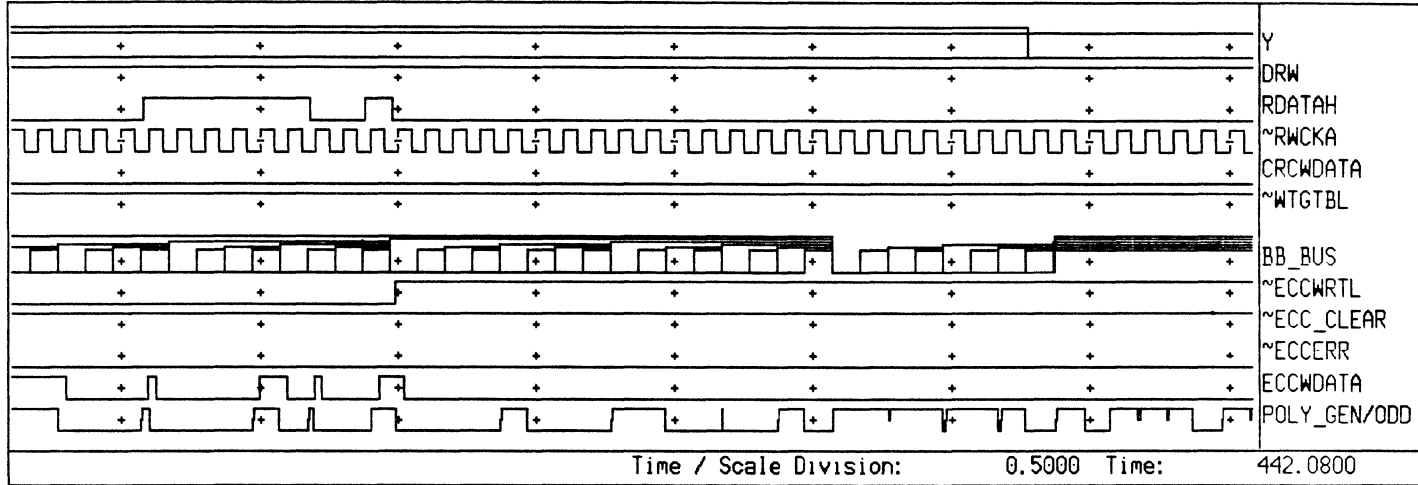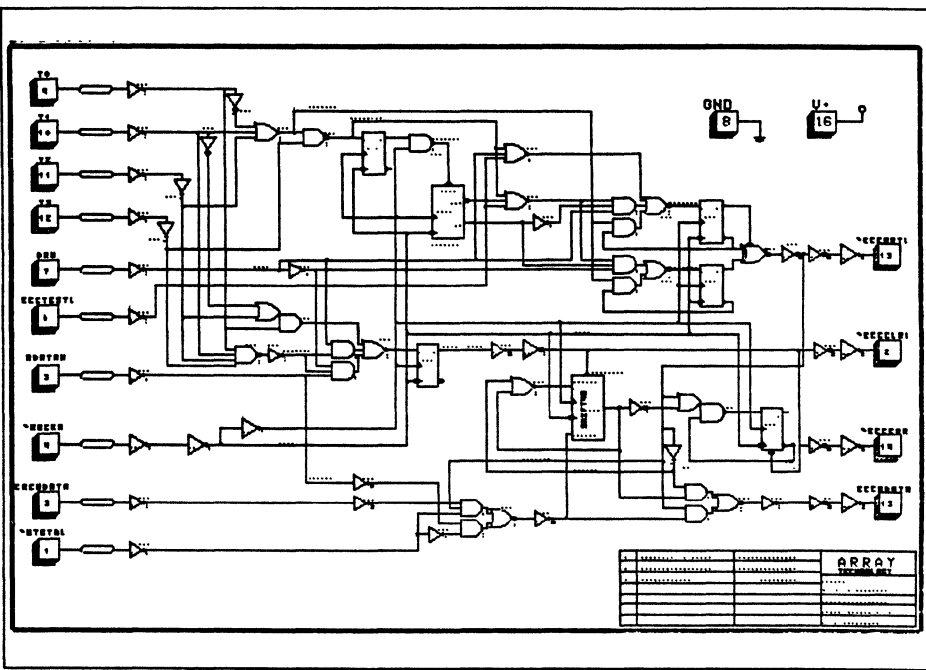Simulation   Display   Analysis
Environmental Imaging   Global

```
440.0000 A  72  0  0  1  1
440.1000 A  73  0  0  1  1
440.2000 A  74  0  0  1  1
440.3000 A  75  0  0  1  1
440.4000 A  76  0  1  1  1
440.5000 A  77  0  0  1  1
440.6000 A  00  0  1  1  1
440.7000 A  01  0  1  1  1
440.8000 A  02  0  1  1  1
440.9000 A  03  0  1  1  1
441.0000 A  04  0  1  1  1
441.1000 A  05  0  1  1  1
441.2000 A  06  0  1  1  1
441.3000 2  07  0  0  1  1
441.4000 2  77  0  1  1  1
441.5000 2  77  0  0  1  1
441.6000 2  77  0  1  1  1
441.7000 2  77  0  1  1  1
441.8000 2  77  0  1  1  1
441.9000 2  77  0  0  1  1
442.0000 2  77  0  1  1  1
```

```
    Time ^Y            ^DRW
      ^BB_BUS        ^ECCTEST
        ^ECCWDATA
        ^POLY_GEN/ODD
```


Waveform labels:
```
Y
DRW
RDATAH
~RWCKA
CRCWDATA
~WTGTBL
BB_BUS
~ECCWRTL
~ECC_CLEAR
~ECCERR
ECCWDATA
POLY_GEN/ODD
```

Time / Scale Division: 0.5000   Time: 442.0800

User time scale =   1000.0 Nsec,   Input radix = Hex

```
RUN 8
HARDcopy
HARDcopy
RUN 4
HARDcopy
```

                               SIM
at top   Travel
    Simulation   Display   Analysis
    Environmental   Imaging   Global
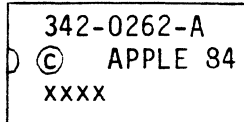
ENGINEERING SPECIFICATION

MAKE FROM: IC, Gate Array ECC,
             Apple Part Number 341-0262-A.
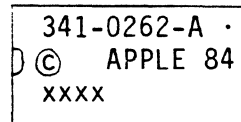
IC MANUFACTURING: Part is to be marked with part number 342-0262,
                    current revision level, copyright designator and
                    four digit date code.

BURN-IN/TEST HOUSE: Make parts from 341-0262. Mark parts with white
                      dots after post burn-in test.

EXAMPLE:

```
342-0262-A
) ©   APPLE 84
xxxx
```
IC Manufacturer

```
341-0262-A ·
) ©   APPLE 84
xxxx
```
Test House

Refer to part number 341-0262 for Specification Sheet.

REFERENCE SPEC: 062-2052 for Burn-In Test Procedure.

NOTE: Manufacturer's name, manufacturer's part number and four digit
        date code are also to be marked on to part.

CHECK PRINT
BY ___ FOR _____
2-17-84

PLEASE
REVIEW
TO _____

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DRAWN BY S. TRIEBES	DATE 2/84	apple computer inc.

DECIMALS   .X ± ___
            .XX ± ___
            .XXX ± ___
ANGLES   XX.X ± ___
FRACTIONS   ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
	CHECKED BY	DATE 2/84	

	APPROVED BY	DATE	TITLE IC, GATE ARRAY ECC, TESTED AND BURNED-IN
	RELEASED BY	DATE	
MATERIAL: _____			SIZE A · DRAWING NUMBER 342-0262-A
NEXT ASSY. · FINISH: _____			SCALE: ___ · SHEET 1 OF 1

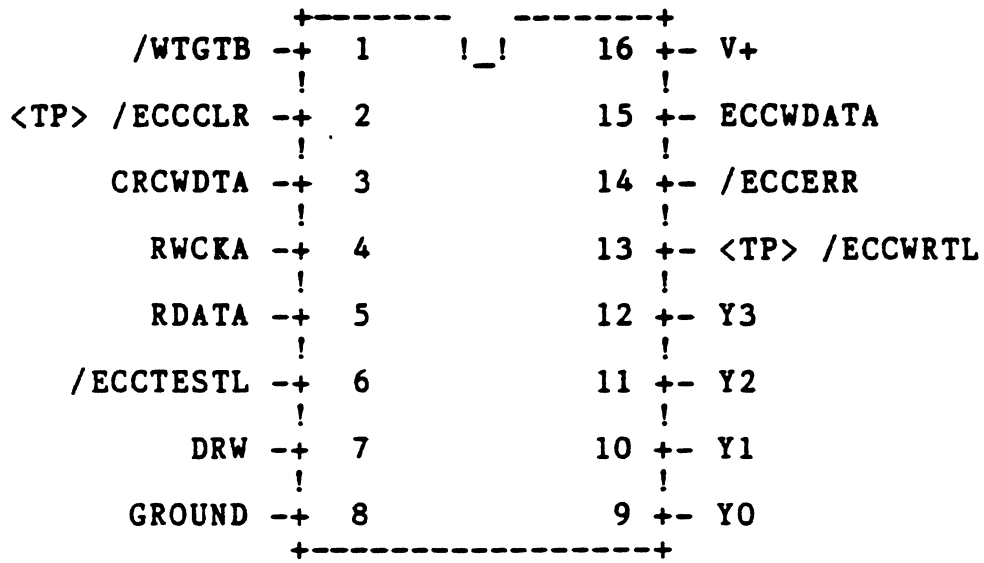| REV.	ZONE	ECO #	REVISION	APPD	DATE
A			INITIAL RELEASE		

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES

DECIMALS   .X ± _____
               .XX ± _____
              .XXX ± _____
ANGLES   XX.X ± _____
FRACTIONS   ± _____
DIMENSIONS IN PARENTHESIS
ARE IN MILLIMETERS.

DRAWN BY	DATE
S. TRIEBES	10/83
CHECKED BY	DATE
	2/84
APPROVED BY	DATE
RELEASED BY	DATE

apple computer inc.

TITLE
    IC, GATE ARRAY ECC

SIZE	DRAWING NUMBER
A	341-0262-A

MATERIAL: _____

FINISH: _____

NEXT ASSY.

SCALE: _____

SHEET 1 OF 5

Pinout diagram for AT-D-550-21 (MISTY)
24 Feb 83

```
                      +-------  -------+
        /WTGTB -+  1    !_!    16 +- V+
               !                  !
  <TP> /ECCCLR -+  2           15 +- ECCWDATA
               !                  !
       CRCWDTA -+  3           14 +- /ECCERR
               !                  !
         RWCKA -+  4           13 +- <TP> /ECCWRTL
               !                  !
         RDATA -+  5           12 +- Y3
               !                  !
     /ECCTESTL -+  6           11 +- Y2
               !                  !
           DRW -+  7           10 +- Y1
               !                  !
        GROUND -+  8            9 +- Y0
                      +----------------+
```

Standard 16-pin plastic DIP.

MARK:

```
 +----------------+
 |  APPLE (C) 83  |
 ) ATD-550-21A    |
 |  DATE CODE     |
 +----------------+
```
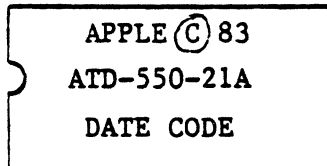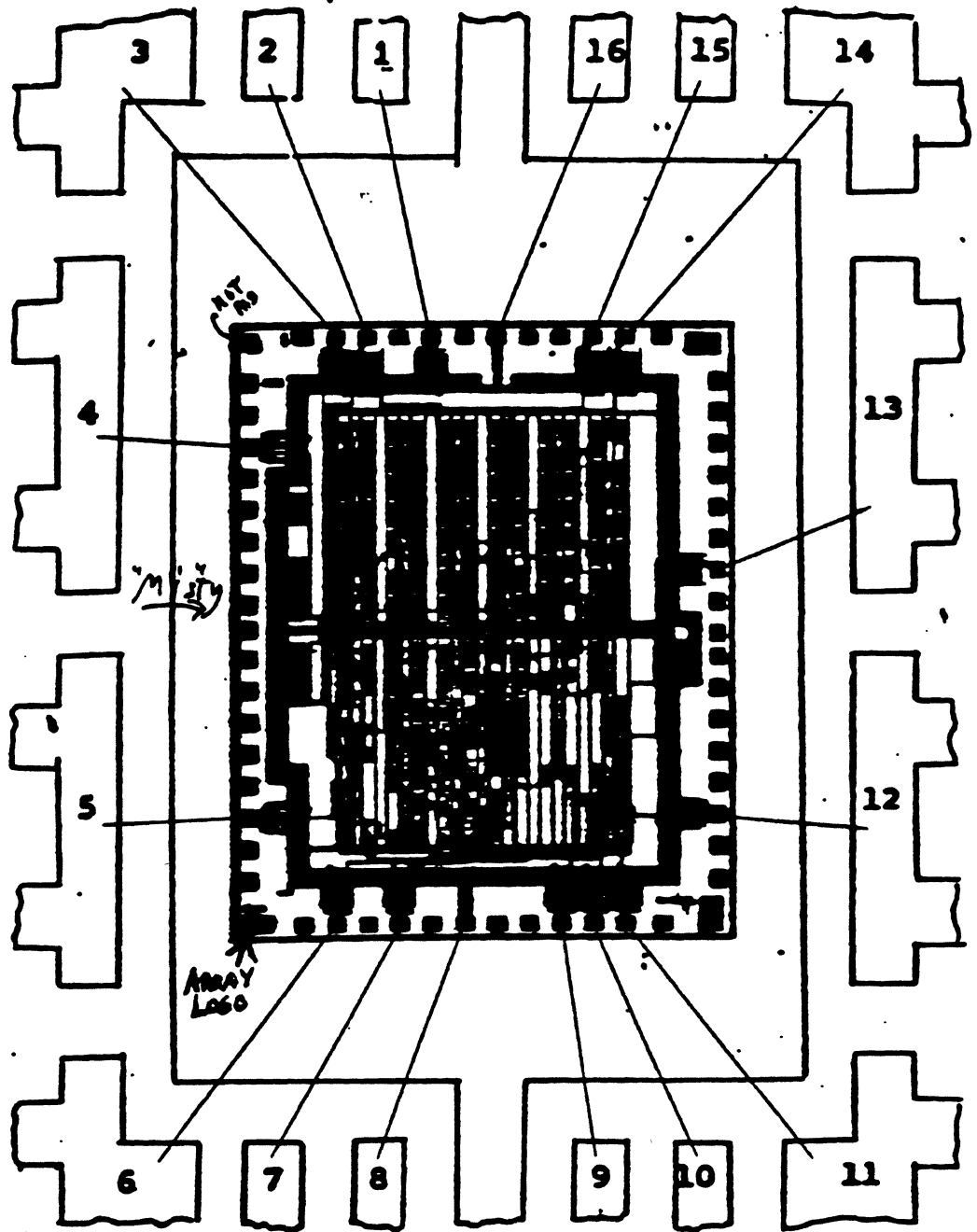
Mark:

APPLE © 83
ATD-550-21A
date Code

CUSTOMER: ARRAY TECHNOLOGY **APPROVALS:**

DEVICE TYPE: AT-D-550-21 **PROCESS:**_____

PACKAGE TYPE: 16 Leads **QA/QC :**_____

DIE SIZE:_____ **REDRAWN BY:**_____

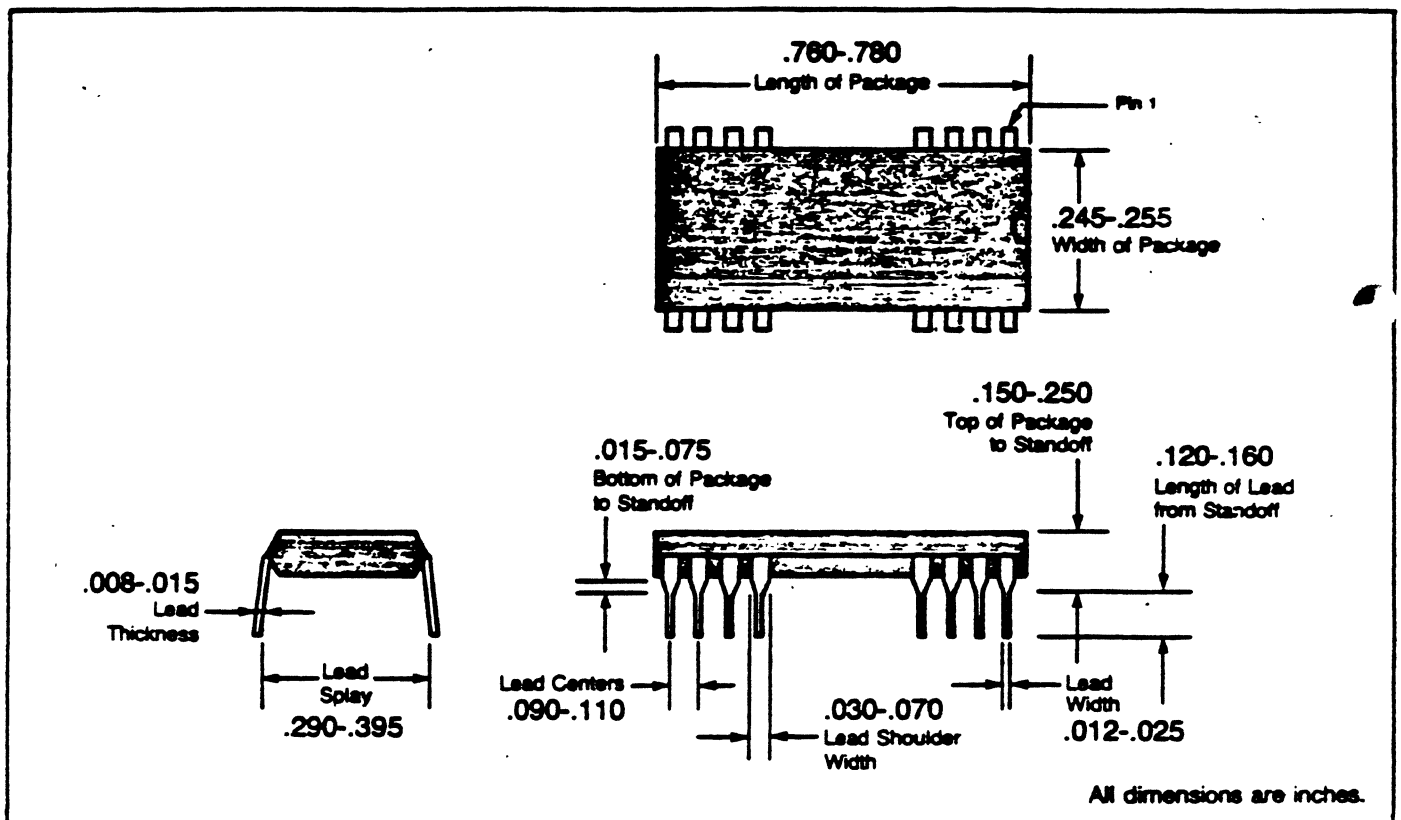**PAD SIZE:** 150. X 230 micron

BONDING DIAGRAM CONTROL NO.:_____

SCALE: 20X **PREFORM SIZE:**_____ **WIRE SIZE:**_____

342-0262-A

"Misty"

PLASTIC DEVICES　　　　　**MECHANICAL DATA**　　**16 Pin**

.760-.780
Length of Package

Pin 1

.245-.255
Width of Package

.150-.250
Top of Package
to Standoff

.015-.075
Bottom of Package
to Standoff

.120-.160
Length of Lead
from Standoff

.008-.015
Lead
Thickness

Lead
Splay
.290-.395

Lead Centers
.090-.110

.030-.070
Lead Shoulder
Width

Lead
Width
.012-.025

All dimensions are inches.
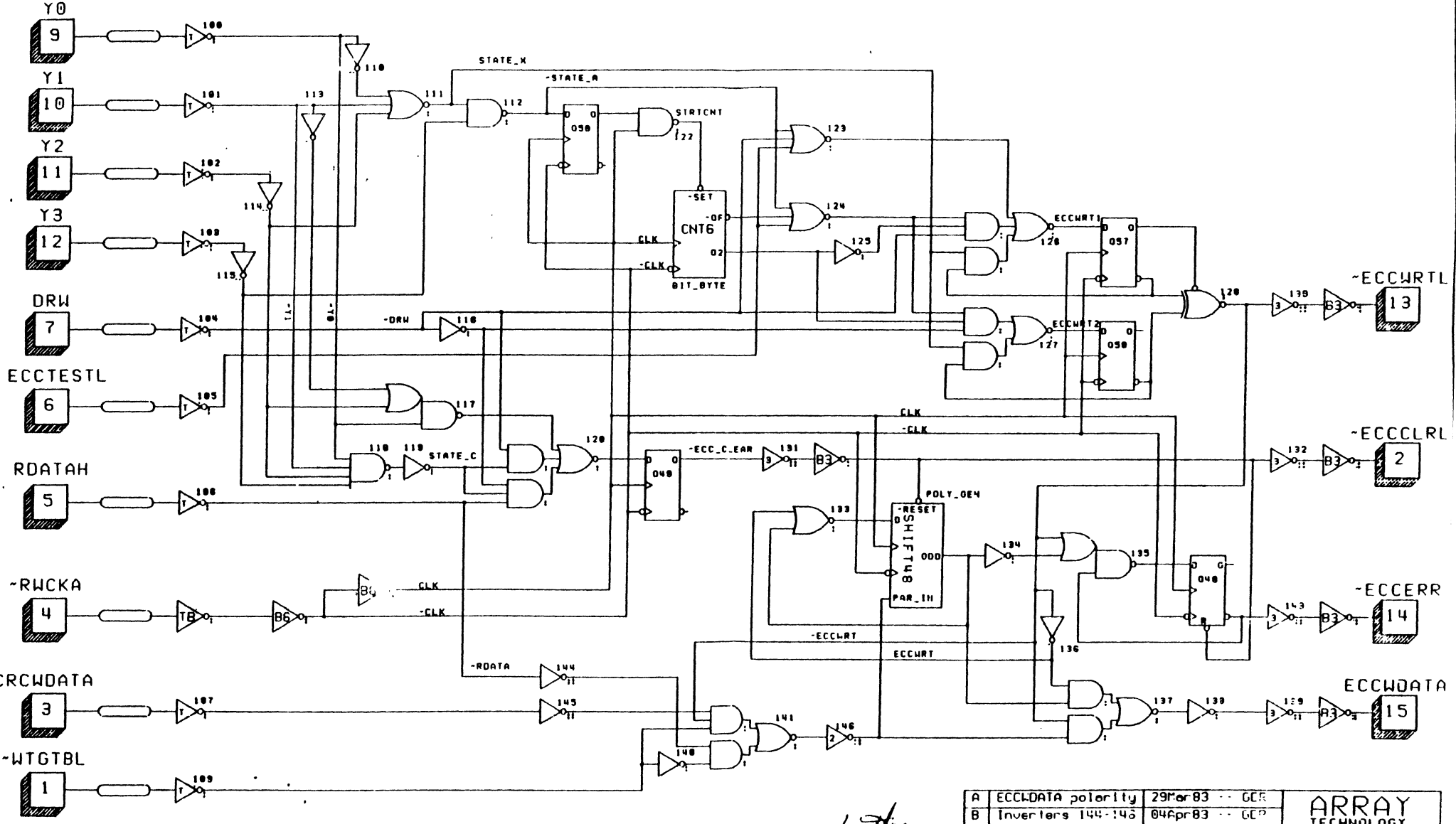
| A | ECCKDATA polarity | 29Mar83 | GCR |
| B | Inverters 144-146 | 04Apr83 | GCR |

ARRAY
TECHNOLOGY

TITLE:
MISTY Main Logic

PART: AT D 550-21
DR'N: Gary Robson
PG: 1 of 3

REV.	ZONE	ECO #	REVISION	APPD	DATE
A			INITIAL RELEASE		

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES

DECIMALS   .X ± _____
              .XX ± _____
              .XXX ± _____
ANGLES   XX.X ± _____
FRACTIONS   ± _____
DIMENSIONS IN PARENTHESIS
ARE IN MILLIMETERS.

DRAWN BY	DATE
S. TRIEBES	1/84
CHECKED BY	DATE
	2/84
APPROVED BY	DATE
RELEASED BY	DATE

 apple computer inc.

TITLE
SPECIFICATION, BURN-IN AND
TEST, GATE ARRAY AT-D-550-21

SIZE	DRAWING NUMBER
A	062-2052-A

MATERIAL: _____

NEXT ASSY.

FINISH: _____

SCALE: _____

SHEET 1 OF 4

APPLE COMPUTER GATE ARRAY AT-D-550-21 BURN-IN AND TEST SPECIFICATION

The following is a specification for burn-in and test procedures for Gate Array AT-D-550-21, Apple Part Number 342-0262. Any deviation from the designated procedures should be approved by the responsible design-components engineer.

THERMAL CYCLING (OPTIONAL - OMIT UNLESS SPECIFIED ON PURCHASE ORDER)

The vendor will temperature cycle all parts from -55 degrees Celsius to +125 degrees Celsius for 10 full cycles. The maximum transition time between environmental extremes shall be 5 minutes. Parts shall remain in each environmental extreme for a minimum of fifteen minutes.

LOADING AND BENCH TEST

The vendor will load the burn-in boards and bench test the loaded boards to detect any gross problems.

BURN-IN

The vendor will burn-in all parts at +125 degrees Celsius for 96 hours (optional times must be specified on purchase order). Components will be biased with 5.0 volts. The inputs and outputs will be configured as shown in the burn-in circuit. All options must be approved by design components engineer.

TESTING

Post burn-in testing must be completed within a 96 hour window after stress removal. If the components miss the 96 hour window, the components must be burned-in for an additional 24 hours and then tested within 96 hours.

The DC/parametric tests will be performed at 70 degrees Celsius within 24 hours after termination of burn-in. Refer to spec. 341-0262 for test specification.

LOT ACCEPTANCE

The post burn-in yield of a lot must meet or exceed 95% to be accepted.

MARKING

The vendor will mark each component that passes the above test with a white contrasting dot. The diameter of the dot must be at least 1.6 mm and the dot must be located near Pin 1. The marking must not obscure the manufacturer's marking.

LOT REPORT

The vendor will supply a certificate of compliance with this specification for the completed lot and a copy of the certificate should be attached to the manufacturing traveller for each lot.

PACKING FOR SHIPMENT

Components are to be boxed according to part number. The boxes shall be clearly marked on the outside with the Apple part number and the purchase order number.

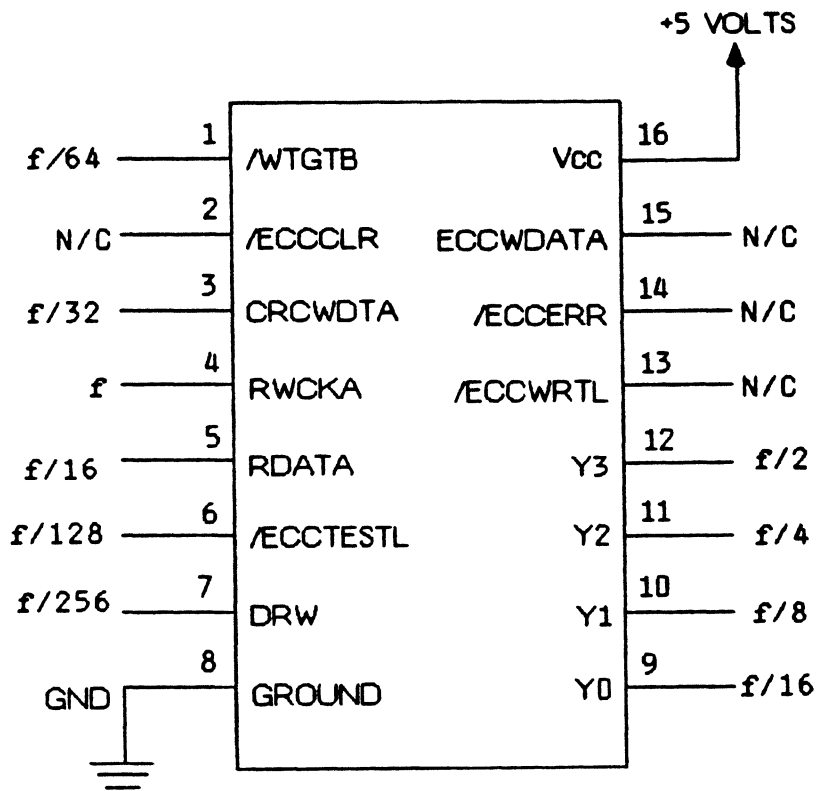The components shall be packed in anti-static rails.

COMPLIANCE

Apple reserves the right to inspect and audit the facilities of any vendor between the hours of 8:00AM and 5:00PM with advanced notice.

SUPPLIES

Unless specifically called out on the purchase order, the above specification is to be followed without any of the described out lines. Where the manufacturer specifies a more conservative limit than called out in this specification, the manufacturer's limit shall be observed, and the actual procedure used shall be described in the lot report.

BURN-IN SCHEMATIC FOR 342-0262

+5 VOLTS

f/64	1	/WTGTB	Vcc	16
N/C	2	/ECCCLR	ECCWDATA	15	N/C
f/32	3	CRCWDTA	/ECCERR	14	N/C
f	4	RWCKA	/ECCWRTL	13	N/C
f/16	5	RDATA	Y3	12	f/2
f/128	6	/ECCTESTL	Y2	11	f/4
f/256	7	DRW	Y1	10	f/8
GND	8	GROUND	Y0	9	f/16

1. f ⩾ 400 K MHz, 50% DUTY CYCLE

2. N/C = NO CONNECTION