Arix Systems Corporation

Functional specification for :

Asynchronous Communications Interface Adapter

Rev 1.1

by Dan Jones, 3 May 88

CONTENTS

Revision record

0.1	18 Jan 88	Dan Jones	Released for engineering review
0.2	21 Jan 88	Dan Jones	Parallel port added
1.0	25 Jan 88	Dan Jones	Released for general review
1.1	3 May 88	Dan Jones	Minor name changes

Document overview

This document describes the design for an Asynchronous Communications Interface Adapter PCB (ACIA) which will provide the device specific interface for a I/O Processor Module (IOPM). The basic configuration will be 16 Asynchronous Channels and one Centronics compatible parallel port. The ACIA supports a channel extender interface.

Reference documents

Arix : System 3000 Hardware Specification, May 4 ,1987
Arix : IOPM Hardware Specification, ver 1.0, Nov 5, 1987
Arix : System 3000 Generic I/O Programming Model, Nov 20, 1987
Eight-channel Universal Asynchronous Receiver/Transmitter, Octal UART, COM78808, Preliminary, 12/86-2.5M, Data Sheet

1. Introduction

The ACIA in combination with the IOPM is a high performance communications controller. The ACIA will provide the asynchronous channels and the character DMA and the IOPM will act primarily as the protocol and compute engine. The ACIA design will augment character throughput by offloading individual character handling from the IOPM as much as possible. This will be accomplished by providing the DMA engine with the ability to scan for special characters. (This deserves a good name: Scan DMA(tm), Observant DMA(tm), Smart DMA(tm), Macro DMA(tm),etc.) In addition, the ACIA will have a Centronics compatible parallel port.

The device board specified in this document is intended to be used with a IOPM in an ARIX 3000 system and, when so used, the IOPM controller and device board pair can either be installed in a main cabinet or an extension cabinet.

2. Hardware features

- 256 byte receive buffer for each channel
- 256 byte transmit buffer for each channel
- Programmable Scan DMA(tm): Character recognizer for receive DMA
- Programmable interrupts
  - Transmit
  - Receive
  - Special character(s)
  - Buffer threshold
  - End of buffer
  - Exception
- Interrupt ring buffer
- Eight-Channel Universal Asynchronous Receiver/Transmitters (Octal UART)

Asynchronous Interface :

- Up to 64 channels (with add-on extenders)
- Each channel is full duplex
- Pin compatible with existing Arix products
- Estimated to be able to handle twice the number of ports as the GC16 at equivalent, typical loads
- The baud rate of each channel is selectable: 50 to 19200 baud
- Modem status change detection

Parallel Interface :

- Centronics Compatible

3. Hardware description

The ACIA module will consist of two or four Eight-Channel Universal Asynchronous Receiver/Transmitters (Octal UART), a Counter/Timer and Parallel I/O Unit (CIO), transmit and receive buffers, a microsequencer that combines character DMA with a character recognizer, device bus interface and arbitration logic.

The Octal UART's allow for a reduction in chip count for the logic required to support eight asynchronous channels In addition, the UART design is regular across channels which simplifies the implementation of the microsequencer and the support logic. The UARTs will support all channels at full duplex and at baud rates up to 19,200 baud (new parts may take this to 38400 baud by 1989). The inherent simplicity of the Octal UARTs does have the drawback of requiring that the IOPM supply a significant amount of software support for data transfers and, for that reason, the more expensive Cirrus Logic Eight Channel Asynchronous Communications Controller (CL_CD180) has been considered. However, the improved features of the CL_CD180 are not sufficient to eliminate the need for a microsequencer and, since the microsequencer must be designed to offload most of the character handling overhead in any case, the cost differential of the CL_CD180 vs the Octal UART is not reduced by the elimination of any logic.

The microsequencer will play a major part in the expected performance improvement for asynchronous communications in this design. On the one hand, we can consider that all of the character processing is still being done in software and, therefore, for typical applications most of the throughput improvement over previous controller designs will come from the better, 68030-based, processing engine in the IOPM. However, it is expected that even software intensive transfers will benefit significantly either from a reduction in interrupt requests or from a simpler, more streamlined interrupt service routine. A significant interrupt reduction should derive from the Character-Scan DMA(tm) which can transfer a character without interrupting the main CPU. It follows that data transmissions such as uucp, which require less software processing on a per character basis, will really benefit in that the microsequencer will move data 2-5 times faster than a dedicated microprocessor.

The microsequencer will implement the following features:

Respond to UART Interrupts
Character DMA
Atomic Read-Modify-Write for control handshaking
Special Character Recognition
Programmable Function Enables
Buffer Threshold Checking
Buffer Limit Checking
Exception Checking

Buffer Interrupts
Identify Interrupting Device and Type:

Limit/Threshold
Special Character
Exception
Reserved

3.1 Asynchronous Interface

The device adapter board shall have sixteen ports for high speed ASYNC communication. In addition this device board will have capacitors on all RS232 signals to suppress RFI signal levels, so that unshielded external cables can be used. The each communication port will have two independent byte wide DMA channels for receive and transmit. DMA is restricted to transfers to or from the dual-ported buffer on the device board. The transmit DMA channels can be stopped at any time (e.g. XOFF received). Each receive channel will have a character recognizer that, depending on the value of the DMAed character, can be set to generate an interrupt when the character transfer completes. A separate 256 bit (32 byte) array for each receive channel will be used for the character recognizer. If a bit in a particular channel's array is set, then DMA of a character corresponding to that bit position in the array corresponding to the channel will generate an interrupt. What action the microsequencer take after the interrupt is posted will be under software control.

3.2 Parallel Interface

The ACIA will include one Centronics compatible, parallel port. The port will implemented with a buffer and a simple PROM state machine for DMA and handshake timing. The design, minus the CIO, will be "lifted" from the GC16.

3.3 Performance: Asynchronous communication

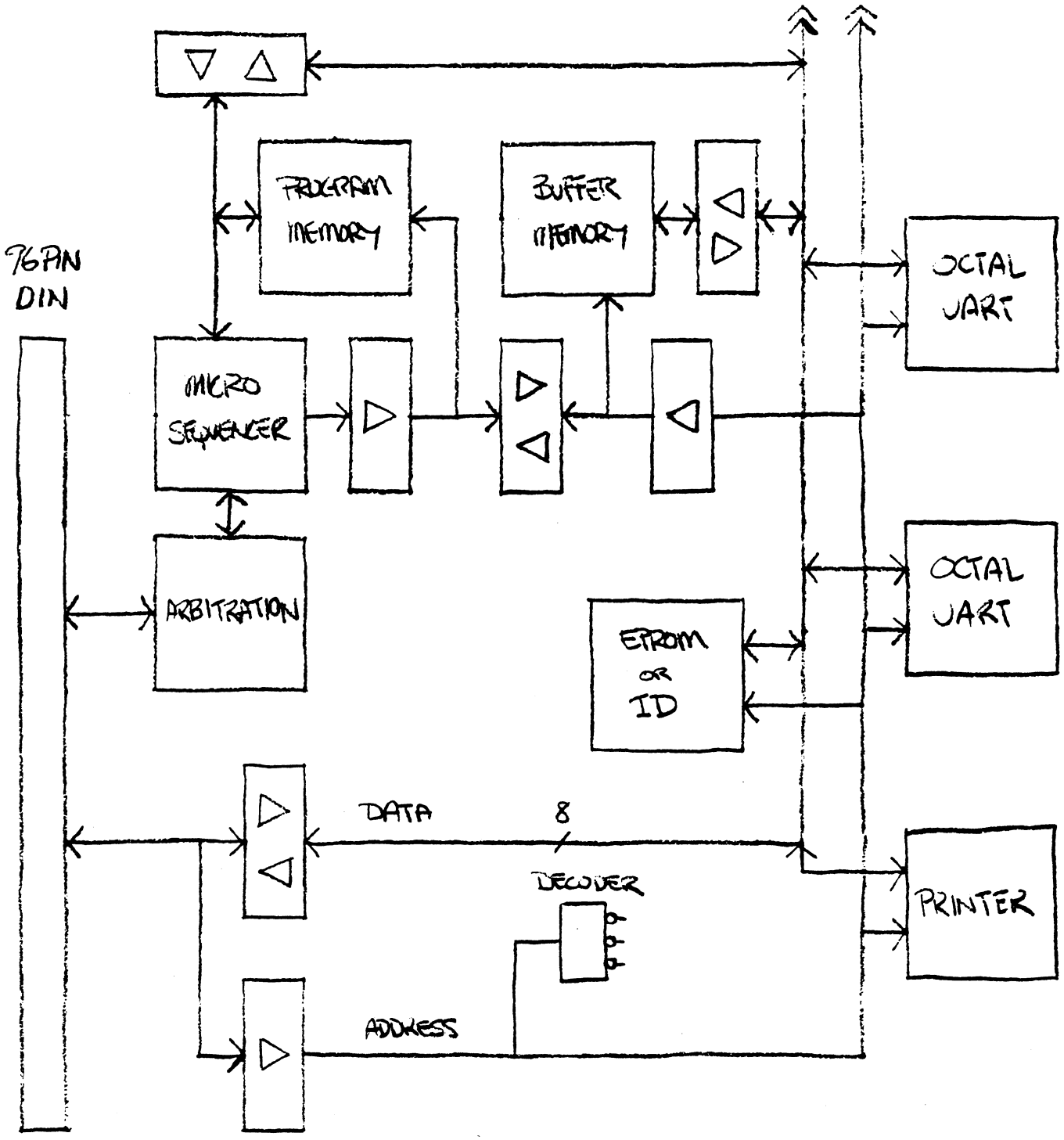
It is estimated that ACIA will be able to handle twice the number of asynchronous ports as the GC16 using typical transaction loads. The extimate is based on the expected performance increase of going to a more powerful microprocessor (i.e. 68020 ==> 68030) that is supported by character recognition. The performance improvement will vary depending upon the amount of processing that is required for each character transferred. The design goal is to design the ACIA microsequencer to be both flexible and fast enough to allow for future software or IOPM performance enhancements. At some point, the character DMA cycle time could be the limiting factor to data throughput assuming that the software processing time is either negligible or it is concurrent with and averages less than the character DMA. The microsequencer's cycle speed will depend upon the complexity of its interaction with the UARTs and component cost, however, a preliminary analysis indicates that the ACIA design should be able to sustain 9600 baud, full duplex on 32 channels i.e. a character transfer time of less than 16 usec/character. DISCLAIMER: The preceding analysis does not imply that the communications software running on the

IOPM will be able to handle a 16 usec/character rate now or in the future. A more likely rate, based on the latest analysis of the GC8, GC16 and IOPM, indicates a process speed improvement from 125 usec/character to 60-75 usec/character.

3.4 Performance: Printer Port

The main design goal of the Printer (Centronix) Interface will be to minimize CPU intervention. The design goal will be to support a 2000 lpm printer. Although, from the hardware point of view, the real limitation will be the amount of software support that will be necessary. The maximum burst transfer rate of the Centronics interface is 12 usec per character or 83 KByte/sec thus a 4KByte buffer could be emptied within a 50 msec burst. Assuming a worstcase average transfer rate of 132 character lines at 2000 lpm (which, incidently, is not how printers are specified) gives a more reasonable throughput of less than 5000 characters per second. If the CPU took 40 clocks (2 usec) to transfer each character to the buffer, then the bus load would be slightly less than 1% with an interrupt being generated and handled every second. Thus, the relative slowness of the printer interface makes it easy to achieve acceptable performance with a minimum of cost. In this case, a buffer of sufficient size (say 2 KByte to 8 KByte) and a DMA engine which can handle both the buffer DMA handshaking and the Centronix interface handshaking and return an interrupt upon error or transfer completion is all that is required.

4. Block Diagram



5. Connectors

One of the device boards will have a 96 pin, male DIN connector to interface to the IOPM. In addition there will be sixteen 6 pin RJ-12 connectors and one 25 pin DB connector on the ACIA PCB module. The electrical interface of the RJ-12 will use the same pin definitions as earlier ARIX communication products. The DB25 connector for the printer will be IBM PC compatible.

5.1 Asynchronous Interface: RJ-12 Connector

The RJ-12 electrical interface will have six pins.

Pin	Signal	Direction
1	Data Set Ready	<--
2	Transmitted Data	-->
3	Received Data	<--
4	Chassis Ground	
5	Data Terminal Ready	-->
6	Data Carrier Detected	<--

5.2 Parallel (Centronics) Interface: DB25 Connector

The DB25 is female and the pinout is as follows:

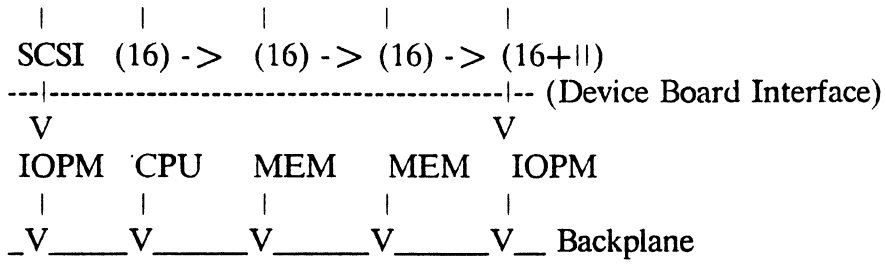
Pin	Signal	Direction
---	----------	---------
1	Data Strobe*	-->
2	Data Bit 0	-->
3	Data Bit 1	-->
4	Data Bit 2	-->
5	Data Bit 3	-->
6	Data Bit 4	-->
7	Data Bit 5	-->
8	Data Bit 6	-->
9	Data Bit 7	-->
10	Acknowledge*	<--
11	Busy	<--
12	Paper Empty	<--
13	Select	<--
14	GND	
15	Fault*	<--
16	Input.Prime*	-->
17-25	GND	

6. Power consumption

It is estimated that the 16 channel ACIA module will use a maximum of 1.5 Amps of 12VDC, 1.4 Amps of -12VDC, and 5 Amps of 5VDC.

7. Installation:

The ACIA will support asynchronous communications port extenders. The number of asynchronous ports may be increased in groups of 16. The first device board will be the only one which connects directly to the IOPM. It will have a connector (DB25) for the parallel port and 16 asynchronous connectors. The remaining boards, up to three, will be connected/stacked onto the original device board for port expansion. Since additional device boards can be added to increase the number of ports that connect to a single IOPM, other System 3000 Controllers (i.e. CPU's and Memory which do not have DIB connectors) can be placed in the backplane slots "behind" the added asynchronous device boards to increase configuration density:



8. Maintainability

The design will include local diagnostic capability at power-up and hardware support for fault isolation. The Asynchronous ports can be looped back for full testing up to the RS232 buffers.

9. Environmental

Meet or exceed Arix's System 3000 Environmental Specification.

10. Safety and Regulatory Agencies

Safety — The design will comply with UL 478, CSA C22.2-220, and IEC 950. The PCB laminate will meet flamability standards and neither the asynchronous or parallel connectors will have power connected directly to any of their pins.

Emissions — The design will comply with FCC Class A and VDE 871 Level B. Capacitors will be added to all of the asynchronous signal lines in order to suppress enough RFI so that unshielded external cables can be used. However, since the amount of RFI will be related to the speed and power of other logic within the same cabinet, this will require testing for verification.

11. Cost estimate

The ACIA will be an assembly of two different PCBs.

DESCRIPTION	COST	
Assembly	16 Async & Parallel	16 Async Extender
Octal UART (2)	35.00	35.00
96 pin DIN	3.75	
6 pin RJ-12 (14)	10.20	10.20
25 pin DB25	2.02	
CIO	4.00	
Parallel logic	10.00	
PROM	2.50	
SRAM Buffer 32X8 (2)	10.00	
SRAM Buffer 2X8 (3)	6.00	
Microsequencer	60.00	
Control logic	25.00	10.00
Drivers,Receivers	4.50	4.50
IOPM interface logic	10.00	
4 - layer board	64.00	32.00
InterPCB connection	5.00	5.00
Back plate	10.00	10.00
Caps and Resistors	20.00	10.00
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Total	282.47	117.70