WIRING DIAGRAM PACKAGE FOR M56 KEYBOARDS (56K224 AND 56K229) — 0607WDP

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
		SCHEMATIC DIAGRAMS	
4896SD	ALL	410896 CIRCUIT CARD ASSEMBLY	1
		CIRCUIT CARD ASSEMBLY	
410896	1	CIRCUIT CARD	1
		CIRCUIT DESCRIPTION	
4896CD	ALL	410896 CIRCUIT CARD ASSEMBLY	1

TELETYPE CORPORATION — 27715 R — NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP. — SHEET 1 OF 1

R&D FORM 361 (6-66)

SHEET INDEX AND ISSUE CONTROL

4896CD

CIRCUIT DESCRIPTION FOR THE 410896 AND 410967 CIRCUIT CARD ASSEMBLIES

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	5-24-83	27756R
2	5-24-83	27169
3	2-27-84	27753

SHEET NUMBER

1	2	3	4
1	1	1	1
2	2	2	2
2	3	2	2

SHEET ISSUE NUMBER

APPROVALS			ENG. SAH	DSGNR.	DRN.
PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	DATE	S-NUMBER	
		JJK	R&D FILE NO. G-18.184AA	E-NUMBER	

TELETYPE CORPORATION

4896CD

TC482-0579

CIRCUIT DESCRIPTION FOR THE 410896 AND 410967 KEYBOARD CIRCUIT CARD ASSEMBLIES

TABLE OF CONTENTS Sheet No.

SECTION I - GENERAL DESCRIPTION

1. BASIC FUNCTIONS

1.1 The 410896 and 410967 circuit card assemblies contain capacitive keyboard encoding logic and interfacing logic for the 56K224, 56K229 and 56K230 keyboards.

1.2 The keyboard functions as a serial device and obtains its power (+5V and -12V) from the associated controller.

1.3 The keyboard encoding and serial interface logic is resident in the Teletype Corporation MOS integrated circuit, ML.

1.4 Aside from the ML MOS circuit, the card assembly contains the following:

1.4.1 The serial receiver (MS IN) front end circuit consists of resistor R5 and capacitor C6. This network is a low pass filter arrangement. Its function is to reduce noise susceptibility and provide some protection from transients (such as electro-static discharge).

1.4.2 The serial driver (MS OUT) front end circuit consists of resistor R4 and capacitor C5. This network is a low pass filter arrangement. Its function is to reduce noise susceptibility and provide some transient protection.

1.4.3 Alarm output circuitry consisting of R2 variable load resistor (volume control) and A1 sounder.

1.4.4 The C3 swamp capacitor adds a fixed capacitance to the comparator input in ML and provides a reference with which to view the key capacitance.

1.4.5 The R3 resistor and C4 capacitor comprise the external reset network for the ML circuit. On power-up, when the capacitor charges up to a nominal of 2V, the ML circuit logic comes out of reset and begins its initialization procedures.

1.4.6 The C7 capacitor provides a constant capacitor load to simulate a depressed keyswitch and is scanned during self-test.

1.4.7 Drive to sense line coupling capacitors for sensing keyswitch state are in the form of a matrix array of circuit card split lands.

SECTION II - DETAILED DESCRIPTION

1. ASSOCIATED DOCUMENTS

4896 SD Schematic Drawing of the circuit card
410896 Circuit Card Assembly Drawing
410967 Circuit Card Assembly Drawing

2. THEORY OF OPERATION

2.1 Power-On Reset/Initialization:

The ML MOS circuit begins initialization on power-up after it comes out of reset. Initialization resets all internal registers and sets all keys released. The controller can also initialize the keyboard by sending the appropriate command in a serial control word.

2.2 Self-Test Sequence

The self-test mode can be entered in three ways. The controller can send the command in a serial control word; or the keyboard operator can initiate self-test by depressing specific keys on the keyboard; or on power-up after ML has initialized itself.

Self-test interrogates the presence of C7 capacitor in the keyboard matrix location, and if present, the test is good. If the test is done during power-up, the result affects the ~Ready bit in the status word to the controller. The tilde, ~, in a signal name indicates logical negation, i.e. the signal is active low. The tilde has the same meaning as a bar drawn over the name. If the test result is good the ~Ready bit is reset. If the self-test was initiated by a command (either from the controller or the keyboard), a good test rings the alarm for approximately one second. Status is sent after the self-test.

2.3 Alarm Operation

The alarm clock (approx. 3kHz) is generated within ML and is derived by dividing the input clock. The normal alarm output has a 4-level stepped decay amplitude and the full ring lasts for about 750 ms. The "chirp" alarm sounds for 16 cycles of the alarm clock at maximum level. The chirp alarm is sounded on all key depressions if the keyboard is optioned by a command from the controller.

2.4 Keyswitch Validation and Repeat Logic

Keyswitch validation is accomplished when the sense algorithm embodied in ML is satisfied for keyswitch depression and release. The keyswitch logic in ML scans the states of all the keys every 5.35 milliseconds. There are 10 drive lines (D1 through D10) and 13 scan lines (S1 through S13). The ML sends a 10V pulse on the selected drive line and senses the states of the keys on the 13 scan lines. A key must exhibit the same condition (whether depressed or released) for two consecutive scans in order to validate the keyswitch state.

2.4 Keyswitch Validation and Repeat Logic (Cont.)

The keyboard enters the repeat mode when a single sendable key is held down for one second or more. However, if a self-test command is received in the meantime, the one second timer services the self-test, since it has priority over usage of the timer.

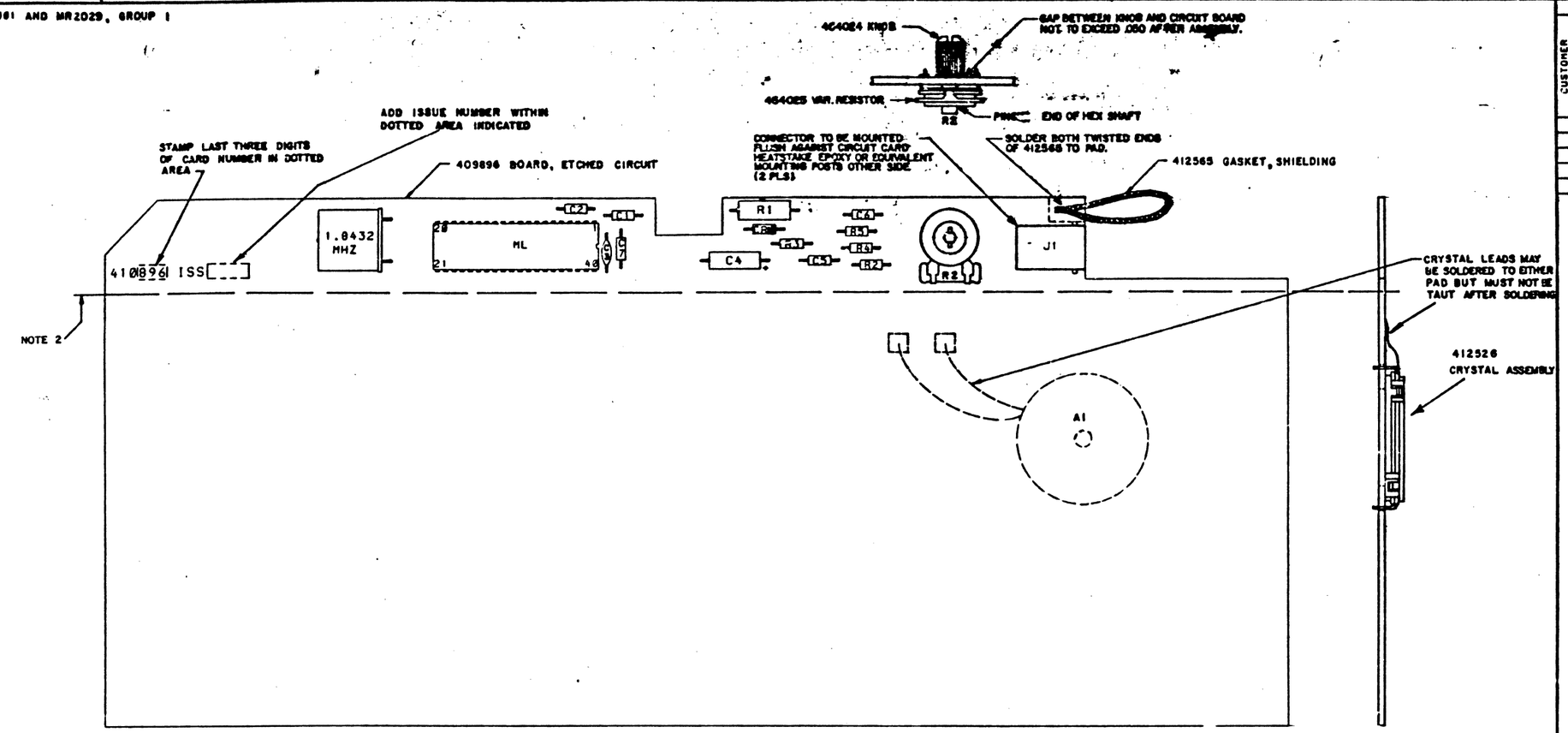
2.5 Sending Logic and Interface

When the keyswitch has been validated as depressed, ML will determine if the code is to be sent as character or if it is to modify the code of another keyswitch (e.g. if the keyswitch is Caps. Lock, Shift or Control, which are mode changes). If it is a character code, it will be sent as the appropriate serial data word to the controller. If it is a mode change, it will be sent in the appropriate serial status word to the controller. Control and shift key changes affect character code but do not initiate a status word.

3. POWER REQUIREMENTS

The circuit card requires +5V (±10%) at 105mA max. and -12V (±10%) at 100mA.

NOTE: MANUFACTURE PER MR2681 AND MR2029, GROUP 1



REF. DESIG.	PART NO REQ	*	DESCRIPTION
ML	416914		MOS, KDKE4P
C1	405324		CAPACITOR, 0.1 μF
C2			SAME AS C1
C3	328792		CAPACITOR, 100 pF
C4	333727		CAPACITOR, 6.8 pF
C5	335800		CAPACITOR, 330 pF
C6			SAME AS C5
C7	340238		CAPACITOR, 33 pF
R1	147953		RESISTOR, 100 OHMS, 3W
R2	454025		RESISTOR, VAR. 2.5K
R3	411298		RESISTOR, 220K
R4	411218		RESISTOR, 100 OHM
R5			SAME AS R4
XTAL	414554		CRYSTAL 1.8432 MHz
A1	412526		CRYSTAL ASSEMBLY
CR1	323810		DIODE, ZENER 5.1V
	454024		KNOB
	409896		ETCHED CIRCUIT BOARD
J1	412525		JACK
	412565		GASKET, SHIELDING

MANUFACTURING NOTES

1. ALL AREAS OF KEYSWITCH PADS WHICH MAKE UP KEYSWITCH CAPACITOR TO BE FREE OF FLUX.
2. COMPONENT PIN PROTRUSION THROUGH CIRCUIT BOARD ON NON-COMPONENT SIDE .045 MAXIMUM IN AREA ABOVE DASHED LINE.

CUSTOMERS NOTES:

1. CUSTOMER IDENTIFICATION ISSUE 2A, R-2 412552 CHANGED TO R-2 454025 VARIABLE RESISTOR WITH 464024 KNOB.
2. CUSTOMER IDENTIFICATION ISSUE 3A, ML CHANGED FROM 411881 KDKEY4 (1 SEC. REPEAT DELAY) TO 416914 KDKE4P(1/2 SEC. REPEAT DELAY).

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
1	A	—	1	3-15-83	27726R
1	A	—	2	2-4-84	27291
2	A	1	3	2-28-84	27793
3	A	2	4	12-14-84	28258
3	A	—	5	3-1-85	28256-1

CIRCUIT CARD ASSEMBLY

410896

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
JAC	1-3-85	

ENGR. P.H.B.	DSGNR. C.G.
DRAWN Y.W.K.	DATE 1-11-83
PROD. NO.	410896
SD-CO NO.	4896
R & D FILE NO.	G-18,366AA

TELETYPE CORPORATION
SKOKIE, ILLINOIS

410896

SIMILAR TO:

SCALE 1/0

TC661/05-0102

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX, SUPPORTING INFORMATION	A1	1	2	3	4																						A1
FS-1 KEYSWITCH AND INTERFACE LOGIC	B1	1	2	3	4																						B1
NOTES:	D1	1	2	2	2																						D1
BD-1 BLOCK DIAGRAM	H1	1	2	2	2																						H1

SUPPORTING INFORMATION

CATEGORY	NO.
KEYSWITCH AND INTERFACE LOGIC CIRCUIT DESCRIPTION	4896CD
CIRCUIT CARD ASSEMBLY DRAWING	410896 410967
LOGIC SYMBOLS, TRUTH TABLES AND GENERAL NOTES	9100WD

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)
2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-2-83	27720
2	5-24-83	27169
3	10-21-83	27397
4	2-27-84	27753

SCHEMATIC DIAGRAM FOR THE 410896, 410967 CIRCUIT CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFC. REL. COMPL.
AC		

ENGR. P.H.B. | DSGNR. P.H.B.

DRN. J.V.K. | DATE 1-20-83

R&D FILE G-18.366AA

S-NUMBER 626645

TELETYPE CORPORATION

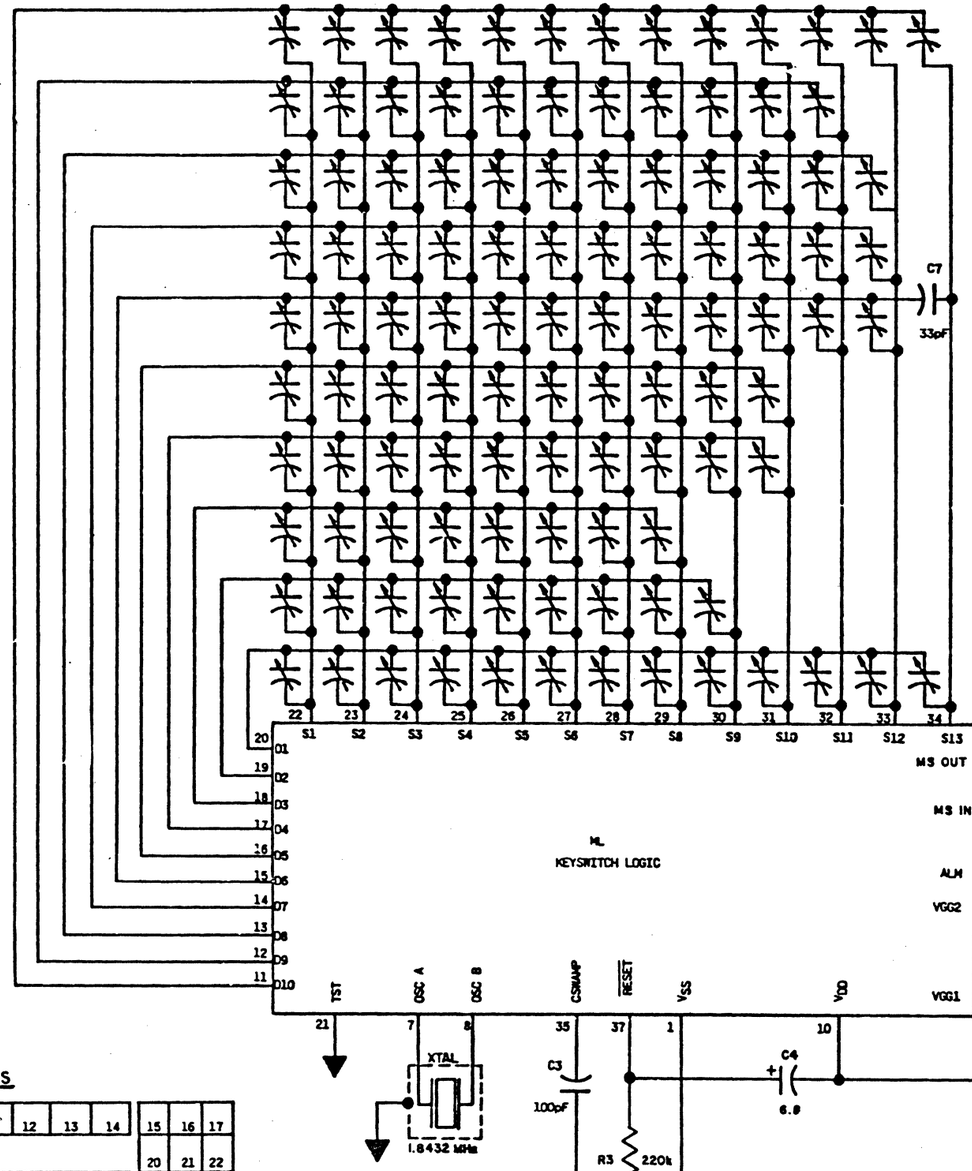
4896SD-A1

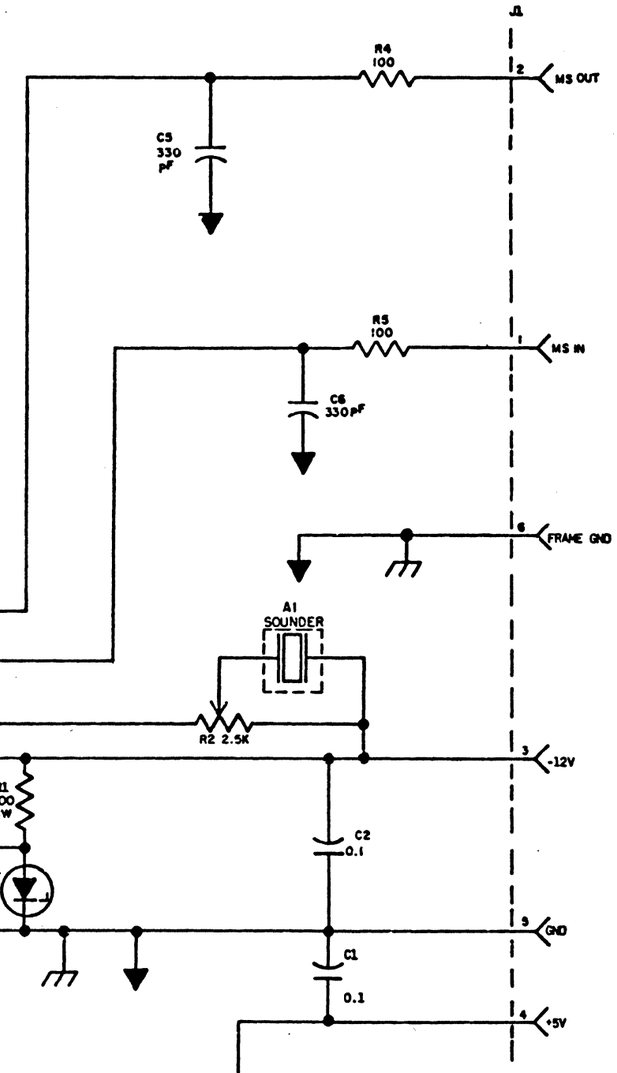
TC654-0579

FS-1 KEYSWITCH AND INTERFACE LOGIC

ISSUE
1
2
3
4

ML KEYSWITCH POSITION NOS. (SEE FIGURE BELOW)										
SENSE	DRIVE									
	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
S1	92	76	56	37	13	2	26	45	65	102
S2	91	75	55	36	12	3	27	46	66	84
S3	90	74	54	35	11	4	28	47	67	103
S4	89	73	53	34	10	5	29	48	68	85
S5	104	72	52	33	9	6	30	49	69	86
S6	88	71	51	32	8	7	31	50	70	87
S7	93	77	57	38	14	24	44	64	83	105
S8	94	78	58	39	20	19	43	63	82	101
S9	95	79	59	40	15	1	25		100	106
S10	96	80	60	41	16	18	23			107
S11	97	81	61	42	21					108
S12	98		62	22	17					109
S13	99									110





THESE KEY POSITIONS ARE FUNCTIONAL ON THE 410967 CARD ASSEMBLY ONLY

KEYSWITCH POSITIONS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
18	19													20	21	22
23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73
74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107
108	109	110														

SCHEMATIC DIAGRAM FOR THE 410896, 410967 CIRCUIT CARD ASSEMBLY

TELETYPE CORPORATION

4896SD-B1

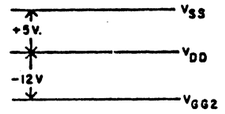
TC640-0878

ISSUE
1
2

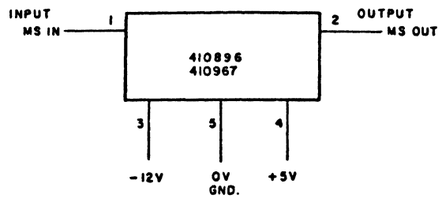
CIRCUIT NOTES

101. SUPPLY VOLTAGES:

THE FOLLOWING VOLTAGES ARE MEASURED WITH RESPECT TO V_{DD}

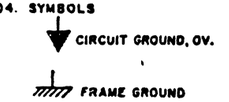


102. SIGNAL VOLTAGES:



INFORMATION NOTES

301. ALL RESISTANCE VALUES ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
302. ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SHOWN.
303. ALL CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
304. SYMBOLS

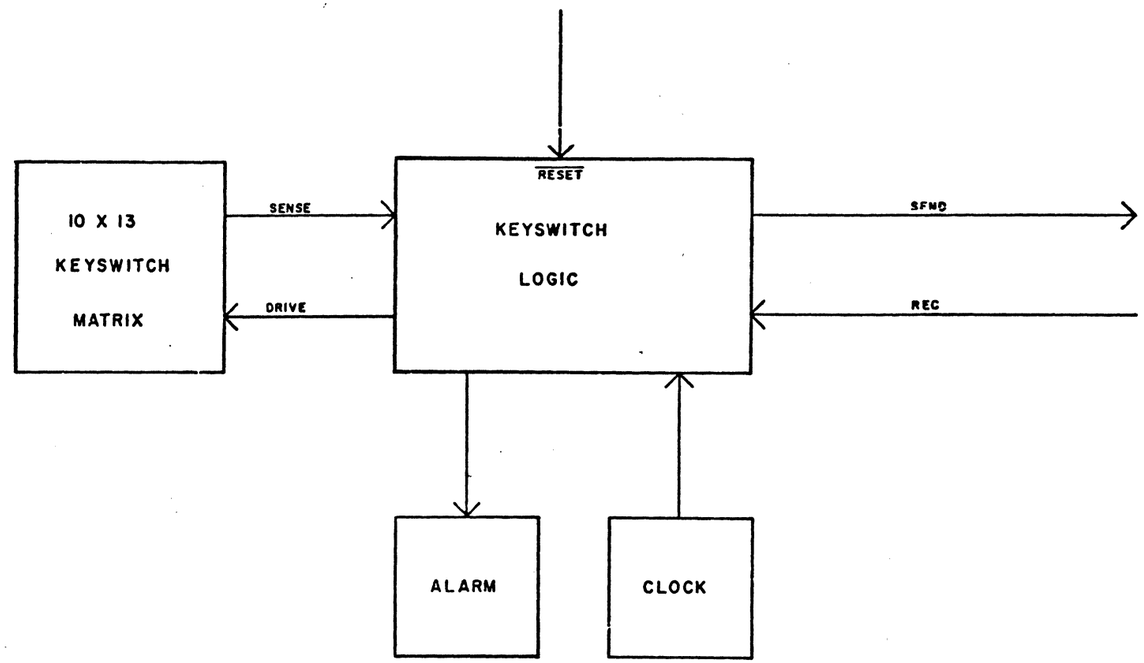


SCHEMATIC DIAGRAM FOR THE 410896, 410967 CIRCUIT CARD ASSEMBLY	TELETYPE CORPORATION SKOKIE, ILLINOIS
	4896SD-DI

TC640-0781

ISSUE
1
2

BD-1 BLOCK DIAGRAM



SCHEMATIC DIAGRAM FOR THE 410896, 410967 CIRCUIT CARD ASSEMBLY	TELETYPE CORPORATION SKOKIE, ILLINOIS
	4896SD-HI

TC640-0781