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checked: C. Thacker	authors: Norm Cohler	approval date	revision date
checked: Gordon Bell	Norman R. Cohler	classification: Specification	
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ABSTRACT and CONTENTS

This document specifies the phase 1.5 CPU multiplier.

Introduction

The multiplier operates in two modes: integer and floating point. Integer multiply (MUL) will take two 24-bit positive number from the X bus and return a 48-bit positive product on the Y bus, according to the scratchpad addresses described below. Floating multiply (FMP) will take two 24-bit words and two 12-bit words from the X bus and return a 72-bit product on the Y bus, according to the scratchpad addresses below. This 72-bit product will be right shifted 1 bit from the correct answer and a Ø inserted into the sign bit.

Integer Multiply Description (MUL)

The A register will be placed on the X bus directly ($\emptyset\ A_{23} \rightarrow \emptyset\ X_{23}$) and scratchpad address 40_8 will load X into the multiplier register ($_{\emptyset}NE_{23}$) and preset the multiply counter to 24 decimal. Then (1ØØ nsec later) the B register will be placed on the X bus directly ($_{\emptyset}B_{23} \rightarrow {}_{\emptyset}X_{23}$) and scratchpad address 43_8 will load X into the multiplicand register ($_{\emptyset}IC_{23}$) and set the AUGO flip flop. Once AUGO is set, any attempts by the EU to read from or write into any multiply register will cause the EU clock to stop until AUGO is reset automatically at the conclusion of the operation. The result will appear in the correct bit position (i.e., $(2B7)^2 = 4B14$) in the product register ($_{\emptyset}N_{35}$) and top third of the multiplier register ($_{\emptyset}NE_{11}$), and is obtainable on

the Y bus by giving two successive scratchpad addresses: 44_8 ($\emptyset^{N}{}_{23} \rightarrow \emptyset^{Y}{}_{23}$) and 45_8 ($_{24}N_{35}$, $\emptyset^{NE}{}_{11} \rightarrow \emptyset^{Y}{}_{23}$). The actual time for the multiplication is 24 200 nsec cycles. Each 24-bit load or read takes 100 nsec.

Floating Multiply Description (FMP)

The magnitude of the accumulator mantissa will be placed on the X bus ($_1A_{23}$, $B_\emptyset \rightarrow \emptyset^{X}{}_{23}$) and loaded into the multiplier register ($\emptyset^{NE}{}_{23}$), upon setting the scratchpad address to $4\emptyset_8$. The remaining portion of the accumulator mantissa will be placed on the X bus ($_1B_{12} \rightarrow \emptyset^{X}{}_{11}$) and loaded into the multiplier register ($_{24}NE_{35}$), upon setting the scratchpad address to 41_8. Scratchpad address 41_8 will preset the multiply counter to 37 decimal. Next the bottom part of the operand mantissa will be placed on the X bus ($_1\beta_{12} \rightarrow \emptyset^{X}{}_{11}$) and loaded into the multiplicand register ($_{24}IC_{35}$), upon setting the scratchpad address to 42_8. Finally, the top portion of the magnitude of the operand mantissa will be placed on the X bus ($_1\alpha_{23}$, $\beta_\emptyset \rightarrow \emptyset^{X}{}_{23}$) and loaded into the multiplicand register ($\emptyset^{IC}{}_{23}$), upon setting the scratchpad address to 43_8. Scratchpad address 43_8 also sets the AUGO flip flop, as in MUL, and will cause the stopping of the EU clock if the EU tries to load or read any multiply register before the operation is complete. The 72-bit product will be automatically right shifted one bit (before resetting AUGO) in order to provide the proper placement of bits for the EU

floating point format. For example, $|4B11|^2 = +1B23$. A zero will be inserted into the topmost bit of the product, so that only 71 bits of valid product are held in $\emptyset^{N}_{35}$ and $\emptyset^{NE}_{35}$ at the conclusion of FMP. The results are read into the EU by setting the scratchpad addresses as follows:

44_8 ($\emptyset^{N}_{23} \rightarrow \emptyset^{Y}_{23}$), 45_8 ($_{24}N_{35}$, $\emptyset^{NE}_{11} \rightarrow \emptyset^{Y}_{23}$),

46_8 ($_{12}NE_{35} \rightarrow \emptyset^{Y}_{23}$).

The actual time for the multiplication is 37 200 nsec cycles. Each 24-bit load or read takes 100 nsec.

Summary

SSP Address (octal)		Effect
	4Ø	$\emptyset^{X}_{23} \rightarrow \emptyset^{NE}_{23}$, 24 → MPCT
Needed only in FMP	41	$\emptyset^{X}_{11} \rightarrow {}_{24}NE_{35}$, 37 → MPCT
	42	$\emptyset^{X}_{11} \rightarrow {}_{24}IC_{35}$
	43	$\emptyset^{X}_{23} \rightarrow \emptyset^{IC}_{23}$, Set AUGO
	44	$\emptyset^{N}_{23} \rightarrow \emptyset^{Y}_{23}$
	45	$_{24}N_{35}$, $\emptyset^{NE}_{11} \rightarrow \emptyset^{Y}_{23}$
	46	$_{12}NE_{35} \rightarrow \emptyset^{Y}_{23}$

Any address 4Ø-47 will stop EU clock if AUGO is set.