BCG-800

Assembly/Test Manual

Biotech Electronics
P.O. Box 485
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First Edition
First Printing

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SECTION 1

Introduction and General Information

1.0 INTRODUCTION AND GENERAL INFORMATION

1.1 Introduction

This manual was created for BCG-800 owners and contains all the necessary information to assemble, test, trouble-shoot and modify your color graphics board. In order to obtain the best picture possible and isolate any potential faults, test/diagnostic programs have been included to be used after assembly. Be sure to read the manual completely before beginning assembly.

1.2 General Information

1.2.1 BCG-800 General Description

The BCG-800 is a low cost, high density color graphics board. It can operate in any S-100 microcomputer. The BCG-800 is capable of generating 8 colors or 2 sets of 4 colors. It has 11 different software selectable modes: 1 alphanumeric mode - 32x16 characters in a 2 color display, 2 semi-graphic modes with display densities ranging from 64x32 to 64x48 in 8 and 4 color sets, and 8 full graphic modes with display densities ranging from 64x64 to 256x192 in 2 and 4 colors. Special features included are 6K bytes of on-board screen refresh RAM, bank select, board protect and composite video.

1.2.2 Receiving Information

Biotech Electronics insures all product leaving its door. As soon as you receive your BCG-800, inspect the package and its contents for damage during shipment. If damage has occurred, contact us immediately and we will take the necessary steps.

1.2.3 Warranty Information

All components sold in kit form are warranted for 90 days following date of purchase. All units assembled by Biotech Electronics are warranted for 180 days following date of purchase. Refer to Appendix I for detailed warranty information.

1.2.4 Factory Service

Factory repair service is provided for out-of-warranty products upon request. Call the factory for a cost estimate and return authorization number, then ship prepaid to Biotech Electronics, 780 Pine Crest Drive, Boulder Creek, California, 95006. Include a detailed description of the problem and be sure to provide static protection during shipment. Upon repair, the product will be shipped back prepaid.

SECTION 2

Assembly Procedure

2.0 ASSEMBLY PROCEDURE

2.1 Construction

2.1.1 Tools

While assembling your color graphics board, a clean, well-lighted work area is a must. Tools which you will need are:

- Soldering Iron
- Solder
- Needle nosed pliers
- Small diagonal cutters

2.1.2 Soldering

When assembling electronic components or equipment, it is essential to exercise the "art" of soldering. If all of the connections are properly soldered, the product should work properly the first time power is applied. A hasty and/or poor job of soldering can mean endless hours trying to locate a short circuit or intermittent connection.

2.1.2.1 Soldering Procedure (Figure 1)

- Touch tip of soldering iron to joint until heated.
- Touch end of soldering roll onto heated joint. Allow only 1/8" of solder to melt onto joint.
- The melted solder appears wet and shiny and will flow evenly and completely around the joint to be soldered.
- Remove the soldering iron as soon as both surfaces have been wetted.
- Wipe tip of soldering iron clean with a wet sponge.

- The whole soldering procedure should only take 2-3 seconds to complete.

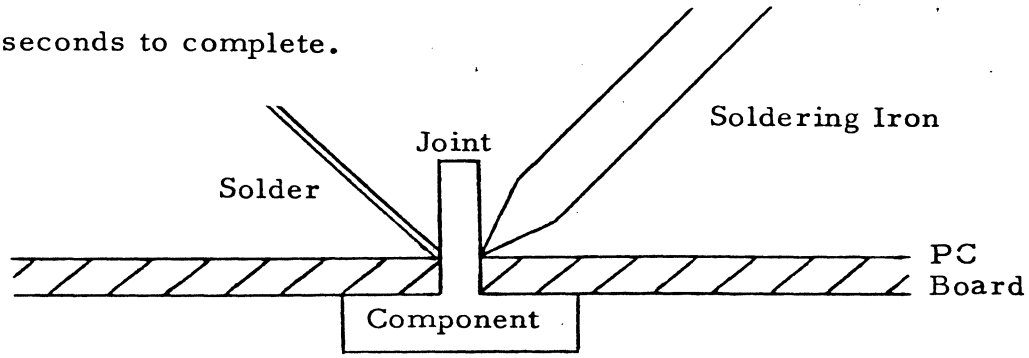


Figure 1 - Soldering Procedure

2.1.2.2 Soldering Tips

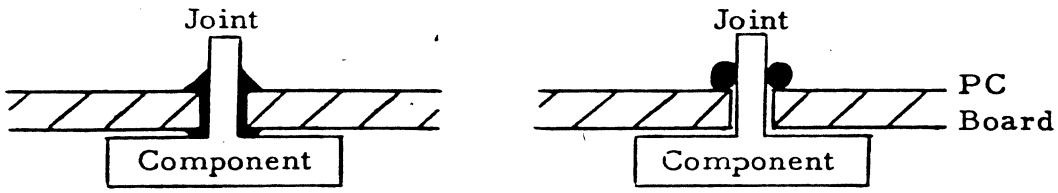
- Use low wattage soldering iron (25 watts maximum) with a small, chisel-shaped tip. Avoid the use of soldering guns.
- Use 60/40 tin/lead solder only (supplied with kit).
- Solder neat and rapidly.
- Don't press soldering iron onto the traces and pads. This may cause traces and pads to lift from the board.
- Use a minimum amount of solder. Too much solder will short circuit the bottom of the board, or flow through the holes and short circuit the top of the board.
- Always inspect the board when completed.

2.1.2.3 Soldering Precautions/Problems

- Excess Solder - Too much solder can cause short circuits on the bottom of the board, or flow through the holes and short circuit the top of the board.
- Excess Heat - Too much heat can cause traces or pads to

lift from the board and/or the board base material will begin to turn brown.

- Cold Solder Joint - This is caused when not enough heat is applied from the soldering iron causing bad solder connections. Cold solder joints are characterized by a dull, lumpy or balled appearance (Figure 2).



Good Solder Joint Cold Solder Joint

Figure 2 - Good vs. Bad Solder Joint

- Solder Bridges - This is caused from excess solder bridging two or more traces together. Solder bridges are caused by too much solder, soldering too quickly, or too big a soldering iron.

2.1.2.4 Soldering/Assembly Aids

To aid in assembly, the printed circuit board has a solder mask. A component placement layout is also silk screened onto the component side of the printed circuit board.

2.2 Assembly Precautions

- Do not insert or remove your BCG-800 from the computer while the power is turned on.
- Do not insert or remove IC's from the board while the power is turned on.

- Be sure the +5V regulator is generating a +5V output voltage before installing any IC's.
- Be careful to insert all IC's in correct positions and with the correct orientation (Figure 3).

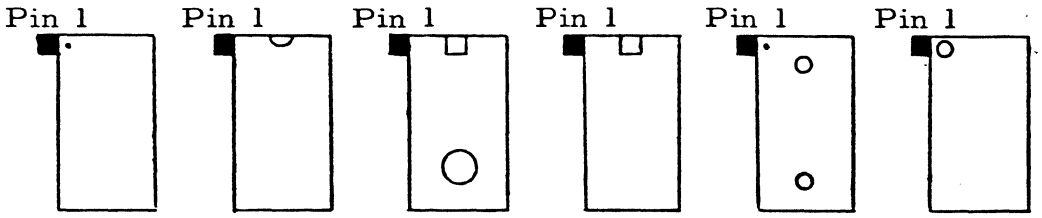


Figure 3 - IC Pin 1 Orientation

- Be careful to insert the electrolytic and tantalum capacitors correctly. Due to polarity, capacitors must be inserted with positive end oriented correctly (Refer to silk screen legend on PC board and/or the Assembly Drawing in Appendix E.).

2.3 Assembly Procedure

2.3.1 Inspection

- Check the printed circuit board carefully for flaws. Inspect closely for any shorts between traces. Shorts between traces are nearly impossible to locate after the PC board is assembled, especially if they fall underneath a socket and/or IC.
- Check the parts supplied against the complete parts list located in Appendix C. If any parts are missing, contact us immediately for prompt replacement parts.

2.3.2 Board Orientation

Throughout the Assembly Procedure section, the board will be referred to assuming the reader is facing the component side of the board so that the integrated circuit numbers (U numbers) are readable. The regulator and heat sink section are on the left hand edge of the board with the 100-pin edge connector running along the bottom.

2.3.3 Component Insertion

2.3.3.1 Sockets

2.3.3.1.1 Soldering Procedure for Sockets

There are several ways to insert and solder sockets, but Biotech Electronics uses the following procedure:

- Insert each socket, one at a time, in the designated position.
- After each socket is inserted into the PC board, turn the PC board over and bend two leads of the socket against the PC board so that the socket will stay in the proper position (i.e. on 16 pin socket, bend pins 8 and 16).
- Solder two bent leads only.
- Turn the PC board over and check to see if the socket is flush against the PC board. If not, re-heat both leads and push the socket flush against the PC board.
- Solder the remaining leads.

2.3.3.1.2 Socket Insertion

Install and solder the thirty-five sockets following the silk

screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

( ) • Install and solder the twelve 14 pin sockets at the following locations: U16, U17, U19, U23, U24, U25, U26, U28, U29, U32, U37, U38.

( ) • Install and solder the eight 16 pin sockets at the following locations: U20, U21, U22, U31, U33, U34, U35, U36.

( ) • Install and solder the thirteen 18 pin sockets at the following locations: U2, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15.

( ) • Install and solder the one 24 pin socket at the following location: U30.

( ) • Install and solder the one 40 pin socket at the following locations: U3.

2.3.3.2 Resistors

Install and solder the twenty-one resistors following the silk screen legend and/or the Assembly Drawing located in Appendix E. Be sure to wear eye protection when cutting the resistor leads. Proceed as follows:

Check	Resistor Value	R/Z Number	Color Code
( )	220 ohms	R17, R18	Red/Red/Brown
( )	1K ohms	R1, R3, R4, R10	Brown/Black/Red
( )	2.2K ohms	R16, R19	Red/Red/Red

Check	Resistor Value	R/Z Number	Color Code
( )	2.7K ohms	R5, R6	Red/Violet/Red
( )	3.9K ohms	R11	Orange/White/Red
( )	5.1K ohms	R2, R14	Green/Brown/Red
( )	10K ohms	R12, R13	Brown/Black/Orange
( )	24K ohms	R9	Red/Yellow/Orange
( )	47K ohms	R7, R8	Yellow/Violet/Orange
( )	1K ohms trimpot 10 turn	R15	---
( )	2.2K ohms (16 pin resistor pack)	Z1, Z2	---

2.3.3.3 Capacitors

Install and solder the thirty capacitors following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check	Capacitor Value	C Number
( )	.01mfd (paper) 25V	C15, C16, C19
( )	.1mfd (paper) 25V	C1, C3, C5, C7, C9, C11, C14, C21, C22, C23, C25, C26, C27, C28, C29, C30
( )	*22mfd (tantalum) 15V	C2, C4, C6, C8, C12, C20
( )	*22mfd (tantalum) 25V	C10
( )	43pf (mica 5%)	C17
( )	56pf (mica 5%)	C18
( )	82pf (mica 5%)	C24

Check	Capacitor Value	C Number
( )	9-35pf (ceramic trimmer capacitor	C13

*Insert with positive end oriented correctly (Refer to silk screen legend and/or the Assembly Drawing located in Appendix E.).

2.3.3.4 Regulators/Heat Sinks

Install the regulators and heat sinks following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

( ) • Bend down the three leads of the two 5V regulators (U18 and U27/LM340-5) 90° so that the leads fit into the correct holes while the bolt holes line up. Do not solder yet.

• Install the 5V regulator and heat sink so that the following sequence of hardware results from bottom to top: 6-32 small pan hex nut, PC board, heat sink, 5V regulator, 6-32 small pattern lock washer, 6-32x1/4" pan head screw. Tighten the bolt (do not over-tighten), then solder the regulator leads.

( ) • Bend down the three leads of the 12V regulator (U1/LM340-12) 90° so that the leads fit into the correct holes while the bolt holes line up. Do not solder yet.

• Install the 12V regulator so that the following sequence of hardware results from bottom to top: 6-32 small pan hex nut, PC board, 12V regulator, 6-32 small pattern lock

washer, 6-32x1/4" pan head screw. Tighten the bolt (do not over-tighten), then solder the regulator leads.

2.3.3.5 Semiconductors

Check

( ) • LED's (D1 and D2) - Insert and solder D1 with flattened side of LED facing left side of the board; then insert and solder D2 with flattened side of LED facing right side of the board (as indicated by dots on the silk screen legend).

( ) • 2N2222 Transistor (Q1) - Insert and solder the transistor with the tab pointing to the upper left hand corner of the PC board (as indicated by the tab on the silk screen legend).

( ) • 3.579545 Color Burst Crystal (Y1) - Bend top two leads 90° so that the leads fit into the correct holes. Insert and solder into the PC board. In addition to the two leads, the bottom of the crystal case should be soldered to the PC board by soldering a piece of clipped resistor lead between the crystal case and the ground plane.

2.3.3.6 Miscellaneous Components

Install and solder the four remaining components following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check

( ) • Insert and solder the 5 pin male molex connector (J1) with the connector pointing toward the top of the board.

Check

( ) • Insert and solder the three dip switches (SW1, SW2, SW3) as follows (Figures 4, 5 and 6):

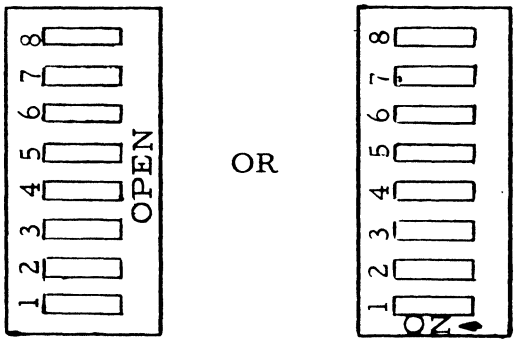


Figure 4 - SW1 Orientation

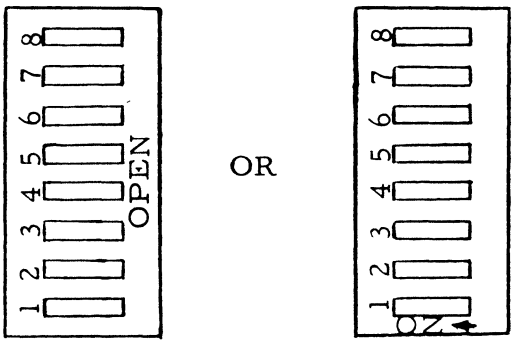


Figure 5 - SW2 Orientation

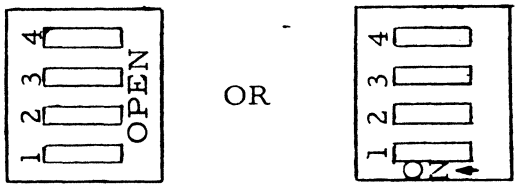


Figure 6 - SW3 Orientation

2.3.4 Voltage Check

- Plug the PC board into the computer.
- Apply power to the PC board. Keep hands and face away from the component side of the PC board.
- Check for +5VDC ± 10% at the positive terminals of ~~C2~~ C4 and ~~C6~~ C8.

- Check for +12VDC ± 10% at the positive terminal of C12.

2.3.5 Integrated Circuits

2.3.5.1 Integrated Circuit Insertion Tips

- Do not insert IC's with the power on.
- Be sure all IC's are in the correct position and with the correct orientation (Figure 3). Pin 1 is designated by a white dot adjacent to the upper left hand corner of each IC location.
- Be sure all leads are straight and parallel. If not, gently straighten and align the pins with a pair of needle nosed pliers.
- If the IC leads are wider than the IC socket holes making insertion difficult, close the rows of pins slightly until they are aligned with the IC socket holes. Close the row of pins uniformly by placing the IC on it's side on a flat surface, so that one row of pins is flat against the surface (Figure 7).

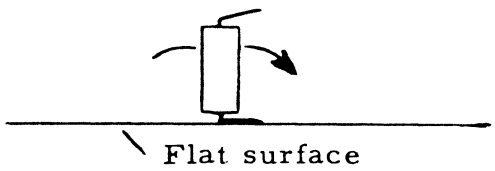


Figure 7 - IC Pin Alignment

Push the row of pins against the flat surface until the pins are vertical to the IC package. Repeat the process to the second row of pins.

- Be sure to handle static sensitive IC's carefully (S68047 and 2114 RAMs/U3 through U15 inclusive). Do not handle unnecessarily. When installing static sensitive IC's, make sure the IC's, the PC board and your body are grounded.
- If an IC must be removed from the socket, do so carefully so that the pins will not be bent during removal. Remove by gently prying, with a screwdriver, a little bit at a time at each end.

2.3.5.2 Integrated Circuit Insertion

Insert the thirteen static sensitive IC's following the silk screen legend and/or the Assembly Drawing located in Appendix E. Follow the static sensitive insertion tips above. Proceed as follows:

Check	U Number	IC
( )	U3	S68047
( )	U4	2114
( )	U5	2114
( )	U6	2114
( )	U7	2114
( )	U8	2114
( )	U9	2114
( )	U10	2114
( )	U11	2114
( )	U12	2114
( )	U13	2114

Check	U Number	IC
( )	U14	2114
( )	U15	2114

Insert the remaining twenty-two IC's following the silk screen legend and/or the Assembly Drawing located in Appendix E. Proceed as follows:

Check	U Number	IC
( )	U2	LM1889
( )	U16	LS136
( )	U17	LS136
( )	U19	LS00
( )	U20	LS42
( )	U21	LS367
( )	U22	LS367
( )	U23	LS136
( )	U24	LS136
( )	U25	LS136
( )	U26	LS10
( )	U28	LS136
( )	U29	LS136
( )	U30	8212
( )	U31	LS112
( )	U32	LS00
( )	U33	LS367

Check	U Number	IC
( )	U34	LS367
( )	U35	LS367
( )	U36	LS367
( )	U37	LS32
( )	U38	LS00

SECTION 3

Testing

3.0 TESTING

3.1 Visual Inspection

The first thing that should be done after stuffing all the components in the PC board is to give the board a thorough visual inspection. The first step is to clean the board. Use a stiff brush to remove small conductive particles. Next, examine the board for solder bridges, components not in correct orientation, anything that looks incorrect. On the component side, examine each IC for pins that are turned under. They are not easy to spot, but bent pins can cause considerable loss of time, money and energy. Look at each pin very closely. On the solder side, look for joints which are not shiny (cold solder joints). If you find any, re-solder them.

3.2 Getting a Good Display

To interface the BCG-800 to a commercial color T.V., a modulator is required if the T.V. does not have a direct video input. There are many excellent modulators commercially available. We suggest using a modulator with a carrier frequency in the UHF band that can be battery operated to eliminate switching noises from your computer.

When you apply power, the display should be random alphanumeric characters in green. Two possibilities exist if the display is not in color. Either the T.V. is not tuned in properly, or the trimmer capacitor (C13) is not adjusted properly. If the character field extends beyond the screen or if the characters are smeared,

then the 1K ohm variable resistor (R15) needs to be adjusted for the proper display width.

The board needs no further adjustments. Adjusting the tint, brightness and contrast on your T. V. will produce a brilliant color display.

The following diagnostic program will aid in the adjustment of the colors. The program will generate the eight bands of colors which the board is capable of producing. The program is written in Basic. The variable "S" is the screen address in decimal, for example S = 49152 for the screen refresh memory addressed at C000 Hex. The variable "M" is the mode port address (See Section 3.3 for the proper switch settings.). The example shows the mode port address at 01 Hex. With some versions of Basic, the FILL command must be replaced with POKE.

Basic Program:

```
  5 REM COLOR GRAPHICS - FOR SEMIGRAPHICS 4
 10 K = 49152
 20 OUT 01, 160
 30 FOR L = 0 TO 15
 40 FOR N = 0 TO 7
 50 FOR I = 0 TO 3
 60 FILL K + I + (N*4) + (L*32), (N*16) + 15
 70 NEXT I
 80 NEXT N
 90 NEXT L
100 END
```

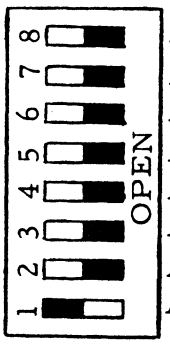
The colors generated will be: green, yellow, cyan, red, blue, cyan/blue, magenta and orange.

3.3 Mode Control Port

The mode control port is an eight bit register which selects one of eleven different modes, as well as the selection of the border color. The mode control port has the following bit assignments:

Bit 7 - Board Protect
Bit 6 - $\overline{\text{INT}}$/EXT
Bit 5 - $\overline{\text{A}}$/S
Bit 4 - $\overline{\text{A}}$/G
Bit 3 - CSS
Bit 2 - GM4
Bit 1 - GM2
Bit 0 - GM1

The mode control port can be assigned to one of two hundred fifty six possible output port addresses. SW2 selects the mode port address as follows (Figure 8):



SW2	A7	0	Open
	A6	0	Open
	A5	0	Open
	A4	0	Open
	A3	0	Open
	A2	0	Open
	A1	0	Open
	A0	0	Closed

Example: Mode Port Address = 01 Hex

Figure 8 - Mode Port Address Selection

NOTE: Bit 7 of the mode port is the board enable. If the Protect Jumper (W2) is installed, bit 7 must be set to 1 for the board to be enabled.

The following diagnostic program, written in Basic, will test the mode port and the different modes of the S68047. The program will ask for the color (1 = blue, 2 = green) and the mode number (1-11) which can be determined by the following table (Table 1):

Mode Number	Mode	Mode Port Data			
		Hex CSS		Dec CSS	
		0	1	0	1
1	Alphanumerics	00	08	00	08
2	Semigraphics-4	20	28	32	40
3	Semigraphics-6	60	68	96	104
4	Graphics 0	10	18	16	24
5	Graphics 1	11	19	17	25
6	Graphics 2	12	1A ~~20~~	18	26
7	Graphics 3	13	1B ~~21~~	19	27
8	Graphics 4	14	1C ~~22~~	20	28
9	Graphics 5	15	1D ~~23~~	21	29
10	Graphics 6	16	1E ~~24~~	22	30
11	Graphics 7	17	1F ~~25~~	23	31

Table 1 - S68047 Mode Selection

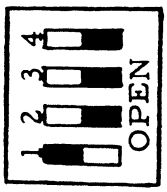
Line 80 of the Mode Test Program has the mode address at 01 Hex. This should be changed for other configurations.

Mode Test Program:

```
 5 REM MODE TEST
10 INPUT "ENTER COLOR (1 = BLUE, 2 = GREEN):", X
20 INPUT "ENTER NODE:", M
30 IF M = 1 THEN N = 0
40 IF M = 2 THEN N = 32
50 IF M = 3 THEN N = 96
60 IF M > 3 THEN N : 16 + (M-4)
70 IF X = 1 THEN C = 8 ELSE C = 0
80 OUT 01, N + C
90 GOTO 10
```

3.4 Refresh Memory

The screen refresh memory consists of 6,144 bytes of 450ns static RAM. The memory can be addressed on any 8K byte boundary. SW3 selects the board address as follows (Figure 9 and Table 2):



A15
A14
A13
Bank Select Disable

Figure 9 - SW3 Address Selection

Address Range Hex	High Order Bits			Dip Switch Setting		
	A15	A14	A13	A15	A14	A13
8K 0000 - 1FFF	0	0	0	Open	Open	Open
16K 2000 - 3FFF	0	0	1	Open	Open	Closed
24K 4000 - 5FFF	0	1	0	Open	Closed	Open
32K 6000 - 7FFF	0	1	1	Open	Closed	Closed
40K 8000 - 9FFF	1	0	0	Closed	Open	Open
48K A000 - BFFF	1	0	1	Closed	Open	Closed
56K C000 - DFFF	1	1	0	Closed	Closed	Open
64K E000 - FFFF	1	1	1	Closed	Closed	Closed

Table 2 - SW3 Address Selection

With the Wait Jumper (W1) installed, one wait state will be added to the memory cycle. The LED (D2) will turn on when the board is addressed and enabled.

The following diagnostic program, written in Basic, will test the 6,144 bytes in the screen refresh memory and report any errors.

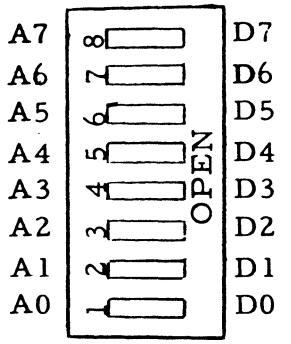
Memory Test:

```
 10 REM MEMORY TEST
 20 K = 49152
 30 OUT 00, 159
 40 D = 1
 50 FOR I = 0 TO 6143
 60 FILL K+I, D
 70 T = EXAM (K+ I)
 80 IF T< > D THEN 160
 90 IF D = 128 THEN 120
100 D = D*2
110 GOTO 130
120 D = 1
130 NEXT I
140 PRINT "PASSED"
150 GOTO 50
160 PRINT "ERROR AT LOC:",I," WRITTEN AS:,D,
    " READ AS:",T
170 GOTO 90
```

The program takes about 3 1/2 minutes to run. The FILL and EXAM functions may need to be changed to POKE and PEEK for some versions of Basic.

3.5 Bank Select

The bank port address is fixed at Hex 40, as in the Cromemco system. The bank byte select is determined by SW1. The bank enabled signal is activated if any high data bit (DØ-D7) has its corresponding switch closed (SW1-Ø - SW1-7). A few combinations are shown below (Figure 10):



Data Bit	A7	A6	A5	A4	A3	A2	A1	A0
0 only	0	0	0	0	0	0	0	1
1 only	0	0	0	0	0	0	1	0
2 or 3	0	0	0	0	1	1	0	0
4, 6 or 7	1	1	0	1	0	0	0	0

Closed = 1, Open = 0

Figure 10 - SW1 Bank Select

The LED (D2) will be lit when the bank is enabled. Power-on-clear ($\overline{POC}$) will always reset the bank select latch. Either the $\overline{EXTCLR}$ (W3) or $\overline{PRESET}$ (W4) may be jumpered in as the clear signal.

The Bank Select feature can be disabled by closing SW3-1.

SECTION 4

Theory of Operation

4.0 THEORY OF OPERATION (Figure 11)

4.1 Color Video Display Generator (VDG)

The heart of the BCG-800 is the AMI S68047 Video Display Generator or VDG (U3). The VDG generates the address (AØ-A12) to access the screen refresh memory, then reads the eight bits of data from the refresh memory, serializes the data and interprets it into video and color information which appears on three output pins: Y(Video), R-Y and B-Y (Color components). All timing and control is done within the VDG chip. The LM1889 modulator chip (U2) generates a 3.58MHz color frequency clock which the VDG uses to generate timing for the horizontal sync, horizontal blank, field sync and vertical blank. The video clock is generated by a 1K ohm trimpot resistor (R15) and an 86pf capacitor (C24). Adjusting the trimpot resistor will vary the display width.

The address and data lines are tri-stated when the $\overline{MS}$ (memory select) pin goes low so that the VDG does not interfere with the CPU operation. The $\overline{FS}$ (field sync) and $\overline{RP}$ (row preset) signals are used to determine when the VDG display is inactive so the CPU can directly change the data in the refresh memory during that time with no interuption to displayed data. NOTE: Using $\overline{RP}$ to indicate an inactive display increases the data transfer rate from the CPU to the refresh memory, but also creates small glitches on the display border. By cutting the trace to pin 13 of U19 (74LS00), only $\overline{FS}$ will indicate an inactive display and the display will be totally glitch

free, but slower.

4.2 Color Encoding and Oscillators

The four outputs from the VDG (Y, R-Y, B-Y and Bias) drive the LM1889 modulator chip (U2). The LM1889 is not used to generate an RF signal, but rather to combine Y, R-Y and B-Y to provide a composite video signal. The LM1889 generates a 3.579545MHz color sub-carrier for the VDG. By adjusting the variable trimmer capacitor (C13), the sub-carrier frequency is changed causing the color to change slightly. The trimmer capacitor should be adjusted so on power-up the display is in color.

The base of the 2N2222 transistor (Q1) is a summing junction for the color sub-carrier (pin 13 of the LM1889) with Y(Video) (pin 9 of the VDG).

4.3 Screen Refresh Memory

The BCG-800 has 6,144 bytes of screen refresh memory. The memory is shared between the VDG and the S-100 bus. The processor can read or write a location in memory just as it would with any main memory. The address is placed on the address bus (16 bits) while signaling a read or write by the state of the control bus. The three most significant address bits (A13-A15) are then compared to the switch settings of SW3. If these bits match with the VDG signaling an inactive display ($\overline{FS}$ or $\overline{RP}$ going low), then the remaining thirteen address bits (AØ-A12) are gated through three hex bus drivers (U21, U22 and U33) to select the memory location.

At this time, the appropriate bus drivers are enabled to read from or write into memory, according to the control bus signals (SMEMR or MWRT).

An IN or OUT instruction will not affect the screen refresh memory. If the processor is trying to access the screen refresh memory while the VDG is using the memory for the display, the processor will enter a wait state until the VDG is done with that frame. Approximately 4ms is available for screen updating.

It is important to note that when the Protect Bit jumper is installed, the processor will not be able to access the screen refresh memory unless bit 7 is set in the mode control port.

4.4 Mode Control Port

The mode control port is an eight bit latch (U30) which allows the user the ability to software select the various graphic modes.

The port address is placed on the lower order address lines (AØ-A7) while signaling an SOUT on the control bus. If the address bits AØ-A7 compare with the switch settings of SW2, then the data on the data bus (DØ-D7) are latched into the mode port. $\overline{A}$/G (bit 4 of the mode control port) determines whether the display will be in alphanumerics or graphics. With $\overline{A}$/G high, GM1, GM2 and GM4 (bits Ø, 1 and 2 respectively) determine the graphics mode (graphics Ø - grahics 7) (Refer to the AMI Data Sheet in Appendix G). $\overline{A}$/G (bit 4) and $\overline{A}$/S (bit 5) are used to select alphanumerics,

semigraphics-4 or semigraphics-6. If $\overline{A}$/G and $\overline{A}$/S are both low, alphanumerics will be selected. With $\overline{A}$/S high, semigraphics-4 is selected by $\overline{INT}$/EXT (bit 6) being low, and semigraphics-6 is selected with $\overline{INT}$/EXT being high.

The Board Protect (bit 7 of the mode control port) must be set high if the protect bit jumper is installed to ensure the refresh memory can be accessed by the processor. CSS (bit 3) allows the user to select the border color for the two-color and four-color graphics (Bit 3 = 0 produces a green border, bit 3 = 1 produces a cyan/blue border). When the VDG is in the semigraphics mode (CSS - bit 3), select one of the two color sets available (Refer to the AMI Data Sheet in Appendix G).

4.5 Bank Select

The bank selection of the BCG-800 is compatible with the Cromemco bank select systems, as well as other currently available memory boards. NOTE: This is not compatible with the IMSAI address select system.

The bank port address (U23 and U24) is fixed at port 40 Hex. The bank byte comparitor (U28 and U29) is connected to the data out lines (DOØ-DO1). If the data out bus compares with the switch settings of SW2, then the common collector outputs remain high and the flip-flop (U31) is set enabling the board and turning on the bank selected LED.

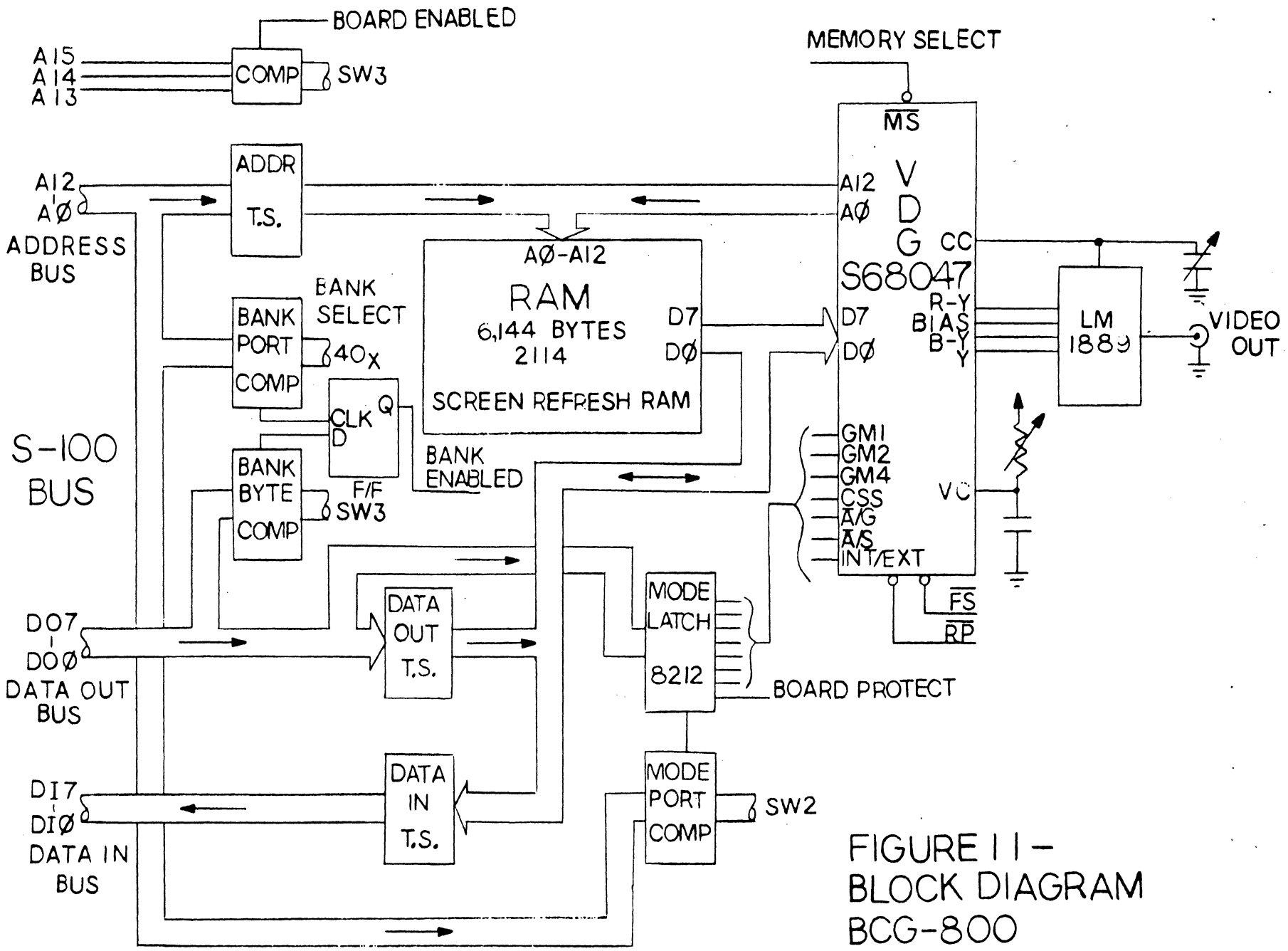


FIGURE 11 – BLOCK DIAGRAM BCG-800

APPENDIX A

Troubleshooting

APPENDIX A

Troubleshooting

The first step to fixing your BCG-800 is to check the obvious. Proceed as follows:

(a) Check for the proper settings of the dip switches.

(b) Verify that all the IC's are in the correct sockets.

(c) Visually inspect to see that all IC leads are in the sockets, not bent under.

(d) Verify the output voltages are correct.

(e) Inspect the solder side of the PC board for solder bridges. Run a sharp knife between traces that look suspicious. A magnifying glass is a must.

Having done all of the above and the board still does not work, then there is most likely a bad device. Proceed as follows:

(a) If you have a problem with the addressing:

1) Check U17 (LS136) for board address.

2) Check U21, U22 and U33 (LS367), address buffer, for shorts as well as proper operation.

(b) If you have a problem with the data input or output (consistent missing bits):

1) Check U35 and U36 (LS367) for data input.

2) Check U33 and U34 (LS367) for data output.

(c) If the modes do not change:

1) Check U30 (8212) for the appropriate bits to be set.

2) Check U16 and U25 (LS136) for address compare.

3) Check the output of U32 (LS00), pin 8, for the $\overline{\text{SOT}}$ strobe.

d) If the memory cannot be read or written into:

1) Verify that bit 7 of the mode port is high if the Protect Bit jumper is installed.

2) Verify that $\overline{\text{FIELD SYNC}}$ or $\overline{\text{ROW PRESET}}$ are low.

3) Verify that U17 (LS136), board address, is working.

4) Verify that U31 (LS112), pin 5, is high (Bank Selected).

5) Verify that U37 (LS32), pin 8 ($\overline{\text{MEMORY SELECT}}$) goes low.

e) If only half of the memory can be accessed:

1) Verify that U31 (LS112) and U34 (LS367) are operating correctly.

2) Verify that U3 (S68047), pin 31, is clocking U31 (LS112).

f) If there is no picture:

1) Check Q1 (2N2222 transistor) for proper operation.

2) Check U3 (S68047), pin 2, for color clock (frequency = 3.579545MHz).

APPENDIX B

Software Driver Routines

APPENDIX B

Software Driver Routines

The software supplied with the BCG-800 is written in 8080 assembly language, and allows the user the ability to change the mode, clear the screen to any color, plot a point, move a point and draw a line. The software is designed for easy interfacing with Basic or assembly language programs.

The plot point, move point and draw line subroutines only in full graphic modes. All input parameters are passed to the sub-routines through an input parameter array located anywhere in system RAM.

The user must personalize the software driver by changing bytes in the program to initialize the input parameter array starting location, the board address and the mode port address.

The input parameter array is ten bytes which must be located in RAM.

Input Parameter Array:

Byte	Label	Description
1	X_{Start}	X Coordinate (Start)
2	Y_{Start}	Y Coordinate (Start)
3	Z_{Start}	Z Intensity/Color (Start)
4	X_{End}	X Coordinate (Destination)
5	Y_{End}	Y Coordinate (Destination)
6	Z_{End}	Z Intensity/Color (Destination)

Byte	Label	Description
7	NOL	Number of Lines
8	BPL	Number of Bytes per Line
9	MODE	Mode Value
10	SUBR	Subroutine Number

To call a subroutine, the subroutine number must be placed in the tenth byte of the input parameter array and the program must CALL the starting location of the software driver.

Subroutine Numbers:

01	CHANGE MODE
02	CLEAR SCREEN
03	PLOT POINT
04	MOVE POINT
05	DRAW LINE
06	FUTURE USE
07	FUTURE USE
08	FUTURE USE

For example, if you wanted to clear the screen and you had the input parameter array located at 1000 (decimal) and the software drivers started at location 0000, the program in Basic would be:

```
10 POKE 1010, 02
20 X = CALL (0000)
```

NOTE: X is a dummy variable.

Change Mode

To change modes, three bytes in the input parameter array must be specified:

Byte 7 - Number of Lines
Byte 8 - Bytes per Line
Byte 9 - Mode

These values can be determined by Table 3. The mode can be changed at any time by specifying the three bytes and calling the change mode subroutine (01). The mode can also be changed by calling any of the other subroutines.

Clear Screen

The clear screen subroutine requires only one input parameter, Z_{Start} or byte 3 in the input parameter array. Z_{Start} will determine the color or intensity the screen will be cleared to depending on the mode:

For 4-Color Graphics:

Z	CSS = 0	CSS = 1
00	Green	Blue
01	Yellow	Cyan/Blue
10	Cyan	Magenta
11	Red	Orange

For 2-Color Graphics:

Z	CSS = 0	CSS = 1
0	Black	Black
1	Green	Cyan/Blue

Plot Point, Move Point and Draw Line

The plot point, move point and draw line subroutines use an X, Y and Z cartesian coordinate system where Z is the intensity or color of the display element.

The screen is configured such that the origin is located at the bottom left hand corner (Figure 12).

The plot point subroutine requires three bytes in the input parameter array: X_{Start}, Y_{Start} and the Z intensity or color.

TABLE 3 - Mode Selection

Mode #	Mode	Hex CSS		Dec CSS		Decimal	
		0 Green	1 Blue	0 Green	1 Blue	Rows (# of Lines) NOL	Columns (Bytes/Line) BPL
1	Alphanumerics	00	08	00	08	---	---
2	Semigraphics-4	20	28	32	40	---	---
3	Semigraphics-6	60	68	96	104	---	---
4	Graphics 0	10	18	16	24	63	16
5	Graphics 1	11	19	17	25	63	16
6	Graphics 2	12	20	18	26	63	32
7	Graphics 3	13	21	19	27	95	16
8	Graphics 4	14	22	20	28	95	32
9	Graphics 5	15	23	21	29	95	32
10	Graphics 6	16	24	22	30	191	32
11	Graphics 7	17	25	23	31	191	32

NOTE: Subroutines only work with full graphics mode.
To change from one color to another add 8.

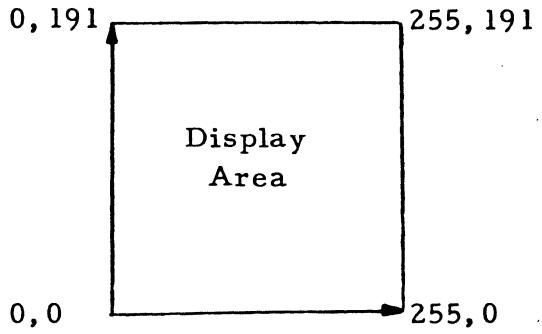


Figure 12 - Screen Coordinate Systems for Graphics 7

The move point subroutine requires six bytes: X_{Start}, Y_{Start}, Z_{Start}, X_{End}, Y_{End} and Z_{End}. The point specified by X_{Start}, Y_{Start} is moved to X_{End}, Y_{End}. The point X_{Start}, Y_{Start} may be either left on or off by specifying Z_{Start}.

The draw line subroutine is very similar to the move point except a line is generated between points. When Z_{Start} and Z_{End} are "on", then a line will be generated. When Z_{Start} and Z_{End} are "zero" the line will be erased.

Software Configuration

The software listing is assembled at location 0000H. This should be considered as a relative address and relocation can be done by changing the two bytes following the JMP and CALL instructions.

The driver routine is set up for the input parameter array at location ~~0100H~~ 1000H. This can be modified by changing the two bytes following an LDA or STA instruction.

The mode port address can be changed by modifying the addresses 06H and ~~36H~~ 38H. The listing uses mode port address at 07H.

Graphics Driver Subroutine

```
0000                    0010 ; BCG-800 COLOR GRAPHICS DRIVER
0000                    0020 ; SYS EQUATES
0000                    0030 ;
0000                    0040 XS      EQU   1000H          ;X START
0000                    0050 YS      EQU   1001H          ;Y START
0000                    0060 ZS      EQU   1002H          ;Z START
0000                    0070 XE      EQU   1003H          ;X END
0000                    0080 YE      EQU   1004H          ;Y END
0000                    0090 ZE      EQU   1005H          ;Z END
0000                    0100 NOL     EQU   1006H          ;NO. OF LINES
0000                    0110 BPL     EQU   1007H          ;BYTES PER LINE
0000                    0120 MODE    EQU   1008H          ;MODE NUMBER
0000                    0130 SUBR    EQU   1009H          ;SUBROUTINE
0000                    0140 ;
0000                    0150 SCADR   EQU   0C000H
0000                    0160 MDPT    EQU   00H
0000                    0170 ;
0000 3A 08 10           0180 START   LDA   MODE           ;GET MODE
0003 F6 80              0190         ORI   80H
0005 D3 00              0200         OUT   A,MDPT         ;UNPROTECT BOARD
0007 3A 09 10           0210         LDA   SUBR           ;GET SUBR NO.
000A FE 01              0220         CPI   01H
000C CA 32 00           0230         JZ    END            ;SET MODE
000F FE 02              0240         CPI   02H
0011 CA 3A 00           0250         JZ    CLEAR          ;CLEAR SCREEN
0014 FE 03              0260         CPI   03H
0016 CA 75 00           0270         JZ    PLOT           ;PLOT POINT
0019 FE 04              0280         CPI   04H
001B CA 02 01           0290         JZ    MOVE           ;MOVE POINT
001E FE 05              0300         CPI   05H
0020 CA 1F 01           0310         JZ    DRAW           ;DRAW LINE
0023 FE 06              0320         CPI   06H
0025 CA 32 00           0330         JZ    END            ;FUTURE SUBROUTINE
0028 FE 07              0340         CPI   07H
002A CA 32 00           0350         JZ    END            ;FUTURE SUBROUTINE
002D FE 08              0360         CPI   08H
002F CA 32 00           0370         JZ    END            ;FUTURE SUBROUTINE
0032 3A 08 10           0380 END     LDA   MODE
0035 E6 7F              0390         ANI   7FH
0037 D3 00              0400         OUT   A,MDPT
0039 C9                 0410         RET                  ;RETURN TO USER PGM
003A                    0420 ;
003A                    0430 ;       CLEAR SCREEN
003A                    0440 ;
003A 21 00 C0           0450 CLEAR   LXI   H,SCADR        ;SCREEN ADDRESS
003D 3A 08 10           0460         LDA   MODE           ;GET MODE
0040 0F                 0470         RRC                  ;TEST FOR 2 OR 4
0041 DA 62 00           0480         JC    CMODE          ;COLOR MODE
0044 3A 02 10           0490         LDA   ZS             ;GET COLOR
0047 47                 0500         MOV   B,A
0048 07                 0510         RLC
0049 07                 0520         RLC
```

```
004A B0          0530         ORA   B
004B 47          0540         MOV   B,A
004C 07          0550         RLC
004D 07          0560         RLC
004E 07          0570         RLC
004F 07          0580         RLC
0050 B0          0590         ORA   B
0051 57          0600         MOV   D,A
0052 72          0610 LOOP    MOV   M,D          ;WRITE TO
0053 3A 3C 00    0620         LDA   003CH        ;HIGH SCREEN
0056 47          0630         MOV   B,A
0057 7C          0640         MOV   A,H          ;GET HIGH SCREEN ADDR
0058 90          0650         SUB   B
0059 FE 18       0660         CPI   18H
005B CA 74 00    0670         JZ    FIN
005E 23          0680         INX   H,L          ;OF SCREEN MEMORY
005F C3 52 00    0690         JMP   LOOP         ;AND RETURN
0062 3A 02 10    0700 OMODE   LDA   ZS
0065 FE 01       0710         CPI   01H          ;WRITE NEXT BYTE
0067 CA 6F 00    0720         JZ    ZSET
006A 16 00       0730         MVI   D,00
006C C3 52 00    0740         JMP   LOOP         ;IF Z=1
006F 16 FF       0750 ZSET    MVI   D,0FFH       ;WRITE 00'S
0071 C3 52 00    0760         JMP   LOOP
0074 C9          0770 FIN     RET
0075             0780 ;
0075             0790 ;       PLOT POINT
0075             0800 ;
0075 3A 01 10    0810 PLOT    LDA   YS           ;FETCH Y COORDINATE
0078 47          0820         MOV   B,A
0079 3A 06 10    0830         LDA   NOL          ;FETCH NUMBER OF LINE
007C 90          0840         SUB   B            ;(NOL-YS)
007D 21 00 00    0850         LXI   H,0000       ;INITIALIZE H,L
0080 16 00       0860         MVI   D,00H        ;INITIALIZE D
0082 5F          0870         MOV   E,A
0083 3A 07 10    0880         LDA   BPL          ;FETCH BYTES PER LINE
0086 19          0890 MTPLY   DAD   D
0087 3D          0900         DCR   A            ;MULTIPLY BY BPL
0088 FE 07  0300 0910         CPI   A,000H
008A C2 86 00    0920         JNZ   MTPLY        ;(H,L)=(NOL-Y)*32
008D 3A 08 10    0930         LDA   MODE
0090 0F          0940         RRC                ;TEST FOR 2 OR 4
0091 D2 C9 00    0950         JNC   EMODE        ;COLOR MODE
0094 3A 00 10    0960         LDA   XS           ;FETCH X COORDINATE
0097 E6 F8       0970         ANI   0F8H         ;MASK LOWER 3 BITS
0099 0F          0980         RRC
009A 0F          0990         RRC                ;DIVIDE BY 8
009B 0F          1000         RRC
009C 16 00       1010         MVI   D,00H
009E 5F          1020         MOV   E,A          ;(D,E)=X/8
009F 19          1030         DAD   D  SCADR     ;(H,L)=(NOL-Y)*32 +X/
00A0 11 00 C0    1040         LXI   D,~~0C000H~~ ;LOAD SCREEN ADDRESS
00A3 19          1050         DAD   D            ;H,L=SA+(NOL-Y)*BPL+X
00A4 3A 00 10    1060         LDA   XS           ;GET X COORDINATE
```

```
00A7 E6 07        1070          ANI   07H           ;MASK UPPER 5 BITS
00A9 47           1080          MOV   B,A
00AA 3E 07        1090          MVI   A,07H         ;INVERT LOW ORDER
00AC 90           1100          SUB   B             ;3 BITS TO SWAP BYTE
00AD 47           1110          MOV   B,A
00AE 03           1120          INX   B
00AF 3E 01        1130          MVI   A,01H         ;CONVERT NUMBER 3
00B1 07           1140 SHIFT    RLC                 ;INTO A '1' IN BIT
00B2 05           1150          DCR   B             ;POSITION 3
00B3 C2 B1 00     1160          JNZ   SHIFT
00B6 47           1170          MOV   B,A
00B7 3A 02 10     1180          LDA   ZS            ;GET INTENSITY
00BA 0F           1190          RRC
00BB DA C5 00     1200          JC    ZEQ1          ;IF Z=1 TURN PIXEL ON
00BE 78           1210          MOV   A,B
00BF 2F           1220          CMA                 ;MASK ALL BUT BIT
00C0 47           1230          MOV   B,A           ;POSITION
00C1 7E           1240          MOV   A,M
00C2 A0           1250          ANA   B             ;CHANGE BYTE
00C3 77           1260          MOV   M,A
00C4 C9           1270          RET                 ;RETURN TO USER PGM
00C5 7E           1280 ZEQ1     MOV   A,M           ;Z=1
00C6 B0           1290          ORA   B             ;CHANGE BYTE
00C7 77           1300          MOV   M,A
00C8 C9           1310          RET                 ;RETURN TO USER PGM
00C9 3A 00 10     1320 EMODE    LDA   XS            ;4 COLOR MODE
00CC E6 FC        1330          ANI   0FCH          ;MASK LOW 2 BITS
00CE 0F           1340          RRC
00CF 0F           1350          RRC                 ;DIVIDE BY 4
00D0 16 00        1360          MVI   D,00H
00D2 5F           1370          MOV   E,A           ;(H,L)=(NOL-Y)*BPL+X/4
00D3 19           1380          DAD   D
00D4 11 00 C0     1390          LXI   D,SCADR       ;SCREEN ADDRESS
00D7 19           1400          DAD   D             ;H,L=SA+(NOL-Y)*BPL+X/4
00D8 3A 00 10     1410          LDA   XS            ;GET X COORDINATE
00DB E6 03        1420          ANI   03H           ;MASK UPPER 6 BITS
00DD 47           1430          MOV   B,A
00DE 3E 03        1440          MVI   A,03H
00E0 90           1450          SUB   B             ;INVERT BYTE POSITION
00E1 3C           1460          INR   A
00E2 4F           1470          MOV   C,A
00E3 47           1480          MOV   B,A
00E4 3A 02 10     1490          LDA   ZS            ;LOAD COLOR (0-3)
00E7 05           1500 LOOP1    DCR   B
00E8 CA F0 00     1510          JZ    DONE1         ;SHIFT COLOR
00EB 07           1520          RLC                 ;TO PROPER BIT
00EC 07           1530          RLC                 ;POSITION
00ED C3 E7 00     1540          JMP   LOOP1
00F0 5F           1550 DONE1    MOV   E,A
00F1 3E FC        1560          MVI   A,0FCH        ;GENERATE MASK
00F3 0D           1570 LOOP2    DCR   C
00F4 CA FC 00     1580          JZ    DONE2         ;CREATE MASK SO
00F7 07           1590          RLC                 ;NOT TO CHANGE
00F8 07           1600          RLC                 ;OTHER DATE
```

```
00F9 C3 F3 00      1610          JMP   LOOP2
00FC 47            1620 DONE2    MOV   B,A
00FD 7E            1630          MOV   A,M
00FE A0            1640          ANA   B              ;MASK BITS
00FF B3            1650          ORA   E              ;ADD COLOR
0100 77            1660          MOV   M,A            ;STORE PIXEL
0101 C9            1670          RET                  ;RETURN TO USER PGM
0102               1680 ;
0102               1690 ;        MOVE POINT
0102               1700 ;
0102 3E 00         1710 MOVE     MVI   A,00H
0104 32 02 10      1720          STA   ZS
0107 CD 75 00      1730          CALL  PLOT
010A 3A 03 10      1740          LDA   XE
010D 32 00 10      1750          STA   XS
0110 3A 04 10      1760          LDA   YE
0113 32 01 10      1770          STA   YS
0116 3E 01         1780          MVI   A,01H
0118 32 02 10      1790          STA   ZS
011B CD 75 00      1800          CALL  PLOT
011E C9            1810          RET
011F               1820 ;
011F               1830 ;        DRAW LINE
011F               1840 ;
011F 3A 00 10      1850 DRAW     LDA   XS             ;H=XS
0122 67            1860          MOV   H,A
0123 3A 01 10      1870          LDA   YS             ;L=YS
0126 6F            1880          MOV   L,A
0127 3A 03 10      1890          LDA   XE             ;D=XE
012A 57            1900          MOV   D,A
012B 3A 04 10      1910          LDA   YE             ;E=YE
012E 5F            1920          MOV   E,A
012F 7A            1930 DRAW1    MOV   A,D            ;XE
0130 94            1940          SUB   H              ;XE-XS
0131 D2 38 01      1950          JNC   VTST
0134 EB            1960          XCHG
0135 C3 2F 01      1970          JMP   DRAW1
0138 CA 5A 01      1980 VTST     JZ    VERT
013B 47            1990 Q14      MOV   B,A
013C 7B            2000          MOV   A,E
013D 95            2010          SUB   L
013E DA 4F 01      2020          JC    Q4
0141 CA 87 01      2030          JZ    HORZ
0144 4F            2040 Q1       MOV   C,A
0145 90            2050          SUB   B
0146 DA AF 01      2060          JC    OCT1
0149 CA AF 01      2070          JZ    OCT1
014C C3 D6 01      2080          JMP   OCT2
014F 4F            2090 Q4       MOV   C,A
0150 80            2100          ADD   B
0151 D2 FD 01      2110          JNC   OCT7
0154 CA 28 02      2120          JZ    OCT8
0157 C3 28 02      2130          JMP   OCT8
015A 7B            2140 VERT     MOV   A,E            ;YE
```

```
015B 95
015C DA, 73 01
015F 7C
0160 32 00 10
0163 7D
0164 32 01 10
0167 CD 9C 01
016A 7B
016B 95
016C CA 9B 01
016F 2C
0170 C3 63 01
0173 7C
0174 32 00 10
0177 7D
0178 32 01 10
017B CD 9C 01
017E 7B
017F 95
0180 CA 9B 01
0183 2D
0184 C3 77 01
0187 7D
0188 32 01 10
018B 7C
018C 32 00 10
018F CD 9C 01
0192 7A
0193 94
0194 CA 9B 01
0197 24
0198 C3 8B 01
019B C9
019C F5
019D C5
019E D5
019F E5
01A0 3E 0F
01A2 3D
01A3 C2 A2 01
01A6 00
01A7 CD 75 00
01AA E1
01AB D1
01AC C1
01AD F1
01AE C9
01AF 58
01B0 50
01B1 14
01B2 7D
01B3 32 01 10
01B6 7C
01B7 32 00 10

2150            SUB   L             ;YE-YS
2160            JC    DOWNV
2170 UPV        MOV   A,H           ;XS
2180            STA   XS
2190 YSETV      MOV   A,L           ;YS
2200            STA   YS
2210            CALL  POUT
2220            MOV   A,E
2230            SUB   L             ;YE-YS
2240            JZ    DONE          ;YE=YS
2250            INR   L             ;XS<>1
2260            JMP   YSETV
2270 DOWNV      MOV   A,H
2280            STA   XS
2290 XSETV      MOV   A,L
2300            STA   YS
2310            CALL  POUT
2320            MOV   A,E
2330            SUB   L
2340            JZ    DONE
2350            DCR   L
2360            JMP   XSETV
2370 HORZ       MOV   A,L
2380            STA   YS
2390 YSV2       MOV   A,H
2400            STA   XS
2410            CALL  POUT
2420            MOV   A,D
2430            SUB   H
2440            JZ    DONE
2450            INR   H
2460            JMP   YSV2
2470 DONE       RET
2480 POUT       PUSH  PSW
2490            PUSH  B
2500            PUSH  D
2510            PUSH  H
2520            MVI   A,0FH
2530 DLAY       DCR   A
2540            JNZ   DLAY
2550            NOP
2560            CALL  PLOT
2570            POP   H
2580            POP   D
2590            POP   B
2600            POP   PSW
2610            RET
2620 OCT1       MOV   E,B
2660            MOV   D,B
2670            INR   D
2680 YSET       MOV   A,L
2690            STA   YS
2700 XSET       MOV   A,H
2710            STA   XS
```

```
01BA CD 9C 01       2720 PLOT1  CALL  POUT
01BD 7B             2730        MOV   A,E
01BE 91             2740        SUB   C
01BF D2 CD 01       2750        JNC   RIGHT
01C2 80             2760 DIAG   ADD   B
01C3 5F             2770        MOV   E,A
01C4 2C             2780        INR   L
01C5 15             2790        DCR   D
01C6 CA 9B 01       2800        JZ    DONE
01C9 24             2810        INR   H
01CA C3 B2 01       2820        JMP   YSET
01CD 15             2830 RIGHT  DCR   D
01CE CA 9B 01       2840        JZ    DONE
01D1 24             2850        INR   H
01D2 5F             2860        MOV   E,A
01D3 C3 B6 01       2870        JMP   XSET
01D6 59             2880 OCT2   MOV   E,C
01D7 51             2920        MOV   D,C
01D8 81             2930 DIAG2  ADD   C
01D9 7C             2940 XSET2  MOV   A,H
01DA 32 00 10       2950        STA   XS
01DD 7D             2960 YSET2  MOV   A,L
01DE 32 01 10       2970        STA   YS
01E1 CD 9C 01       2980        CALL  POUT
01E4 7B             2990        MOV   A,E
01E5 90             3000        SUB   B
01E6 D2 F4 01       3010        JNC   UP
01E9 81             3020 DIAC2  ADD   C
01EA 5F             3030        MOV   E,A
01EB 2C             3040        INR   L
01EC 15             3050        DCR   D
01ED CA 9B 01       3060        JZ    DONE
01F0 24             3070        INR   H
01F1 C3 D9 01       3080        JMP   XSET2
01F4 15             3090 UP     DCR   D
01F5 CA 9B 01       3100        JZ    DONE
01F8 2C             3110        INR   L
01F9 5F             3120        MOV   E,A
01FA C3 DD 01       3130        JMP   YSET2
01FD 79             3140 OCT7   MOV   A,C
01FE 2F             3180        CMA
01FF 3C             3190        INR   A
0200 4F             3200        MOV   C,A
0201 59             3210        MOV   E,C
0202 51             3220        MOV   D,C
0203 14             3230        INR   D
0204 7C             3240 XSET7  MOV   A,H
0205 32 00 10       3250        STA   XS
0208 7D             3260 YSET7  MOV   A,L
0209 32 01 10       3270        STA   YS
020C CD 9C 01       3280        CALL  POUT
020F 7B             3290        MOV   A,E
0210 90             3300        SUB   B
0211 D2 1F 02       3310        JNC   DOWN7
```

```
0214 81          3320 DIAG7  ADD   C
0215 5F          3330        MOV   E,A
0216 2D          3340        DCR   L
0217 15          3350        DCR   D
0218 CA 9B 01    3360        JZ    DONE
021B 24          3370        INR   H
021C C3 04 02    3380        JMP   XSET7
021F 15          3390 DOWN7  DCR   D
0220 CA 9B 01    3400        JZ    DONE
0223 2D          3410        DCR   L
0224 5F          3420        MOV   E,A
0225 C3 08 02    3430        JMP   YSET7
0228 58          3440 OCT8   MOV   E,B
0229 50          3480        MOV   D,B
022A 14          3490        INR   D
022B 79          3500        MOV   A,C
022C 2F          3510        CMA
022D 3C          3520        INR   A
022E 4F          3530        MOV   C,A
022F 7D          3540 YSET8  MOV   A,L
0230 32 01 10    3550        STA   YS
0233 15          3560        DCR   D
0234 7C          3570 XSET8  MOV   A,H
0235 32 00 10    3580        STA   XS
0238 CD 9C 01    3590        CALL  POUT
023B 7B          3600        MOV   A,E
023C 91          3610        SUB   C
023D D2 4A 02    3620        JNC   RT8
0240 80          3630 DIAG8  ADD   B
0241 5F          3640        MOV   E,A
0242 2D          3650        DCR   L
0243 CA 9B 01    3660        JZ    DONE
0246 24          3670        INR   H
0247 C3 2F 02    3680        JMP   YSET8
024A 15          3690 RT8    DCR   D
024B CA 9B 01    3700        JZ    DONE
024E 24          3710        INR   H
024F 5F          3720        MOV   E,A
0250 C3 34 02    3730        JMP   XSET8
```

Symbol Table

SYMBOL TABLE

```
BPL    1007   CLEAR  003A   DIAC2  01E9   DIAG   01C2   DIAG2  01D8   DIAG7  0214
DIAG8  0240   DLAY   01A2   DONE   019B   DONE1  00F0   DONE2  00FC   DOWN7  021F
DOWNV  0173   DRAW   011F   DRAW1  011F   EMODE  00C9   END    0032   FIN    0074
HORZ   0187   LOOP   0052   LOOP1  00E7   LOOP2  00F3   MDPT   0000   MODE   1008
MOVE   0102   MTPLY  0086   NOL    1006   OCT1   01AF   OCT2   01D6   OCT7   01FD
OCT8   0228   OMODE  0062   PLOT   0075   PLOT1  01BA   POUT   019C   Q1     0144
```

```
Q14    013B    Q4     014F    RIGHT  01CD    RT8    024A    SCADR  C000    SHIFT  00B1
START  0000    SUBR   1009    UP     01F4    UPV    015F    VERT   015A    VTST   0138
XE     1003    XS     1000    XSET   01B6    XSET2  01D9    XSET7  0204    XSET8  0234
XSETV  0177    YE     1004    YS     1001    YSET   01B2    YSET2  01DD    YSET7  0208
YSET8  022F    YSETV  0163    YSV2   018B    ZE     1005    ZE01   00C5    ZS     1002
ZSET   006F
```

Object Code

```
DUMP 0000 0252
0000 3A 08 10 F6 80 D3 00 3A 09 10 FE 01 CA 32 00 FE
0010 02 CA 3A 00 FE 03 CA 75 00 FE 04 CA 02 01 FE 05
0020 CA 1F 01 FE 06 CA 32 00 FE 07 CA 32 00 FE 08 CA
0030 32 00 3A 08 10 E6 7F D3 00 C9 21 00 C0 3A 08 10
0040 0F DA 62 00 3A 02 10 47 07 07 B0 47 07 07 07 07
0050 B0 57 72 3A 3C 00 47 7C 90 FE 18 CA 74 00 23 C3
0060 52 00 3A 02 10 FE 01 CA 6F 00 16 00 C3 52 00 16
0070 FF C3 52 00 C9 3A 01 10 47 3A 06 10 90 21 00 00
0080 16 00 5F 3A 07 10 19 3D FE 00 C2 86 00 3A 08 10
0090 0F D2 C9 00 3A 00 10 E6 F8 0F 0F 0F 16 00 5F 19
00A0 11 00 C0 19 3A 00 10 E6 07 47 3E 07 90 47 03 3E
00B0 01 07 05 C2 B1 00 47 3A 02 10 0F DA C5 00 78 2F
00C0 47 7E A0 77 C9 7E B0 77 C9 3A 00 10 E6 FC 0F 0F
00D0 16 00 5F 19 11 00 C0 19 3A 00 10 E6 03 47 3E 03
00E0 90 3C 4F 47 3A 02 10 05 CA F0 00 07 07 C3 E7 00
00F0 5F 3E FC 0D CA FC 00 07 07 C3 F3 00 47 7E A0 B3
0100 77 C9 3E 00 32 02 10 CD 75 00 3A 03 10 32 00 10
0110 3A 04 10 32 01 10 3E 01 32 02 10 CD 75 00 C9 3A
0120 00 10 67 3A 01 10 6F 3A 03 10 57 3A 04 10 5F 7A
0130 94 D2 38 01 EB C3 2F 01 CA 5A 01 47 7B 95 DA 4F
0140 01 CA 87 01 4F 90 DA AF 01 CA AF 01 C3 D6 01 4F
0150 80 D2 FD 01 CA 28 02 C3 28 02 7B 95 DA 73 01 7C
0160 32 00 10 7D 32 01 10 CD 9C 01 7B 95 CA 9B 01 2C
0170 C3 63 01 7C 32 00 10 7D 32 01 10 CD 9C 01 7B 95
0180 CA 9B 01 2D C3 77 01 7D 32 01 10 7C 32 00 10 CD
0190 9C 01 7A 94 CA 9B 01 24 C3 8B 01 C9 F5 C5 D5 E5
01A0 3E 0F 3D C2 A2 01 00 CD 75 00 E1 D1 C1 F1 C9 58
01B0 50 14 7D 32 01 10 7C 32 00 10 CD 9C 01 7B 91 D2
01C0 CD 01 80 5F 2C 15 CA 9B 01 24 C3 B2 01 15 CA 9B
01D0 01 24 5F C3 B6 01 59 51 81 7C 32 00 10 7D 32 01
01E0 10 CD 9C 01 7B 90 D2 F4 01 81 5F 2C 15 CA 9B 01
01F0 24 C3 D9 01 15 CA 9B 01 2C 5F C3 DD 01 79 2F 3C
0200 4F 59 51 14 7C 32 00 10 7D 32 01 10 CD 9C 01 7B
0210 90 D2 1F 02 81 5F 2D 15 CA 9B 01 24 C3 04 02 15
0220 CA 9B 01 2D 5F C3 08 02 58 50 14 79 2F 3C 4F 7D
0230 32 01 10 15 7C 32 00 10 CD 9C 01 7B 91 D2 4A 02
0240 80 5F 2D CA 9B 01 24 C3 2F 02 15 CA 9B 01 24 5F
0250 C3 34 02
```

APPENDIX C

Parts List

APPENDIX C

Parts List

Resistors

R/Z Number	Resistor Value	Color Code
R1	1K ohms *	Brown/Black/Red
R2	5.1K ohms *	Green/Brown/Red
R3	1K ohms *	Brown/Black/Red
R4	1K ohms *	Brown/Black/Red
R5	2.7K ohms *	Red/Violet/Red
R6	2.7K ohms *	Red/Violet/Red
R7	47K ohms *	Yellow/Violet/Orange
R8	47K ohms *	Yellow/Violet/Orange
R9	24K ohms *	Red/Yellow/Orange
R10	1K ohms *	Brown/Black/Red
R11	3.9K ohms *	Orange/White/Red
R12	10K ohms *	Brown/Black/Orange
R13	10K ohms *	Brown/Black/Orange
R14	5.1K ohms *	Green/Brown/Red
R15	1K ohms trimpot 10 turn	---
R16	2.2K ohms *	Red/Red/Red
R17	220 ohms *	Red/Red/Brown
R18	220 ohms *	Red/Red/Brown
R19	2.2K ohms *	Red/Red/Red
Z1	2.2K ohms 16 pin resistor pack	---
Z2	2.2K ohms 16 pin resistor pack	---

*1/4 watt 5%

Capacitors

C Number	Capacitor Value	Capacitor Type
C1	.1mfd 25V	Paper
C2	22mfd 15V	Tantalum
C3	.1mfd 25V	Paper
C4	22mfd 15V	Tantalum
C5	.1mfd 25V	Paper
C6	22mfd 15V	Tantalum
C7	.1mfd 25V	Paper
C8	22mfd 15V	Tantalum
C9	.1mfd 25V	Paper

Parts List (Con't.)

C Number	Capacitor Value	Capacitor Type
C10	22mfd 25V	Tantalum
C11	.1mfd 25V	Paper
C12	22mfd 15V	Tantalum
C13	9-35pf	Ceramic trimmer capacitor
C14	.1mfd 25V	Paper
C15	.01mfd 25V	Paper
C16	.01mfd 25V	Paper
C17	43pf	Mica 5%
C18	56pf	Mica 5%
C19	.01mfd 25V	Paper
C20	22mfd 15V	Tantalum
C21	.1mfd 15V	Paper
C22	.1mfd 15V	Paper
C23	.1mfd 15V	Paper
C24	82pf	Mica 5%
C25	.1mfd 15V	Paper
C26	.1mfd 15V	Paper
C27	.1mfd 15V	Paper
C28	.1mfd 15V	Paper
C29	.1mfd 15V	Paper
C30	.1mfd 15V	Paper

Semiconductors

Semi Number	Semi Type	Semi Description
D1	LED	Red 2V 20MA
D2	LED	Red 2V 20MA
Q1	Transistor	2N2222 GP NPN
Y1	Crystal	3.579545 Color Burst Crystal

Integrated Circuits

IC Number	IC Type	IC Description
U1	LM340-12	12V Regulator
U2	LM1889	Modulator
U3	S68047	Video Display Generator
U4	2114	1KX4 Static RAM
U5	2114	1KX4 Static RAM
U6	2114	1KX4 Static RAM
U7	2114	1KX4 Static RAM

Parts List (Con't.)

IC Number	IC Type	IC Description
U8	2114	1KX4 Static RAM
U9	2114	1KX4 Static RAM
U10	2114	1KX4 Static RAM
U11	2114	1KX4 Static RAM
U12	2114	1KX4 Static RAM
U13	2114	1KX4 Static RAM
U14	2114	1KX4 Static RAM
U15	2114	1KX4 Static RAM
U16	LS136	Quad Exclusive Or-Gate
U17	LS136	Quad Exclusive Or-Gate
U18	LM340-5	5V Regulator
U19	LS00	Quad 2-Input Positive-Nand Gate
U20	LS42	4 Line-to-10-Line Decoder
U21	LS367	Hex Bus Driver
U22	LS367	Hex Bus Driver
U23	LS136	Quad Exclusive Or-Gate
U24	LS136	Quad Exclusive Or-Gate
U25	LS136	Quad Exclusive Or-Gate
U26	LS10	Triple 3-Input Positive-Nand Gate
U27	LM340-5	5V Regulator
U28	LS136	Quad Exclusive Or-Gate
U29	LS136	Quad Exclusive Or-Gate
U30	8212	8 Wide I/O Port
U31	LS112	Dual J-K Negative-Edge-Triggered Flip-Flop
U32	LS00	Quad 2-Input Positive-Nand Gate
U33	LS367	Hex Bus Driver
U34	LS367	Hex Bus Driver
U35	LS367	Hex Bus Driver
U36	LS367	Hex Bus Driver
U37	LS32	2-Input Positive-Or Gate
U38	LS00	Quad 2-Input Positive-Nand Gate

Miscellaneous

Number	Description
J1	5 Pin Male Molex Connector
SW1	8 Position Dip Switch

Parts List (Con't.)

Number	Description
SW2	8 Position Dip Switch
SW3	4 Position Dip Switch

Quantity	Description
12	14 Pin Low Profile Socket (Solder Tail)
8	16 Pin Low Profile Socket (Solder Tail)
13	18 Pin Low Profile Socket (Solder Tail)
1	24 Pin Low Profile Socket (Solder Tail)
1	40 Pin Low Profile Socket (Solder Tail)
3	6-32x1/4" Pan Head Screw
3	6-32 Small Pan Hex Nut
3	6-32 Small Pattern Lock Washer
2	Heat Sink TO-220 Package
1	PC Board
1	Assembly Manual and Software
1	Solder

APPENDIX D

Parts List Summary

APPENDIX D

Parts List Summary

Resistors

2	220 ohms	*
4	1K ohms	*
2	2.2K ohms	*
2	2.7K ohms	*
1	3.9K ohms	*
2	5.1K ohms	*
2	10K ohms	*
1	24K ohms	*
2	47K ohms	*
1	1K ohms trimpot 10 turn	
2	2.2K ohms 16 pin resistor pack	

*1/4 watt 5%

Capacitors

3	.01mfd (paper) 25V
16	.1mfd (paper) 25V
6	22mfd (tantalum) 15V
1	22mfd (tantalum) 25V
1	43pf (mica 5%)
1	56pf (mica 5%)
1	82pf (mica 5%)
1	9-35pf (ceramic trimmer capacitor)

Semiconductors

2	LED Red 2V 20MA
1	2N2222 GP Transistor NPN
1	3.579545 Color Burst Crystal

Integrated Circuits

3	LS00	Quad 2-Input Positive-Nand Gate
1	LS10	Triple 3-Input Positive-Nand Gate
1	LS32	Quad 2-Input Positive-Or Gate
1	LS42	4 Line-to-10-Line Decoder
1	LS112	Dual J-K Negative-Edge-Triggered Flip-Flop
7	LS136	Quad Exclusive-Or Gate
5	LS367	Hex Bus Driver
1	LM1889	Modulator

Parts List Summary (Con't.)

Integrated Circuits (Con't.)

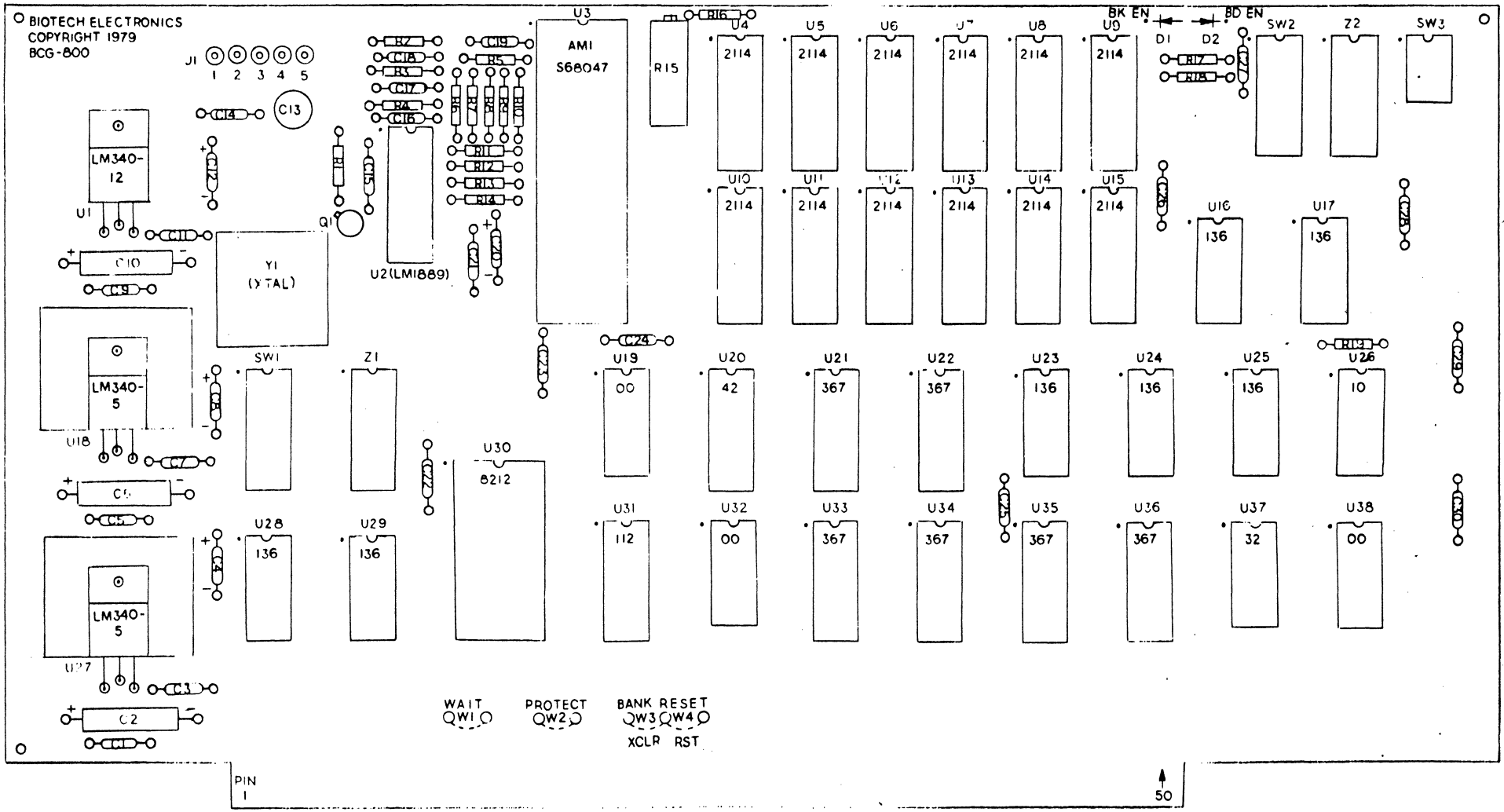
2	LM340-5	5V Regulator
1	LM340-12	12V Regulator
12	2114	1KX4 Static RAM
1	8212	8 Wide I/O Port
1	S68047	Video Display Generator

Miscellaneous

1	5 Pin Male Molex Connector
2	8 Position Dip Switch
1	4 Position Dip Switch
12	14 Pin Low Profile Socket (Solder Tail)
8	16 Pin Low Profile Socket (Solder Tail)
13	18 Pin Low Profile Socket (Solder Tail)
1	24 Pin Low Profile Socket (Solder Tail)
1	40 Pin Low Profile Socket (Solder Tail)
3	6-32x1/4" Pan Head Screw
3	6-32 Small Pan Hex Nut
3	6-32 Small Pattern Lock Washer
2	Heat Sink TO-220 Package
1	PC Board
1	Assembly Manual and Software
1	Solder

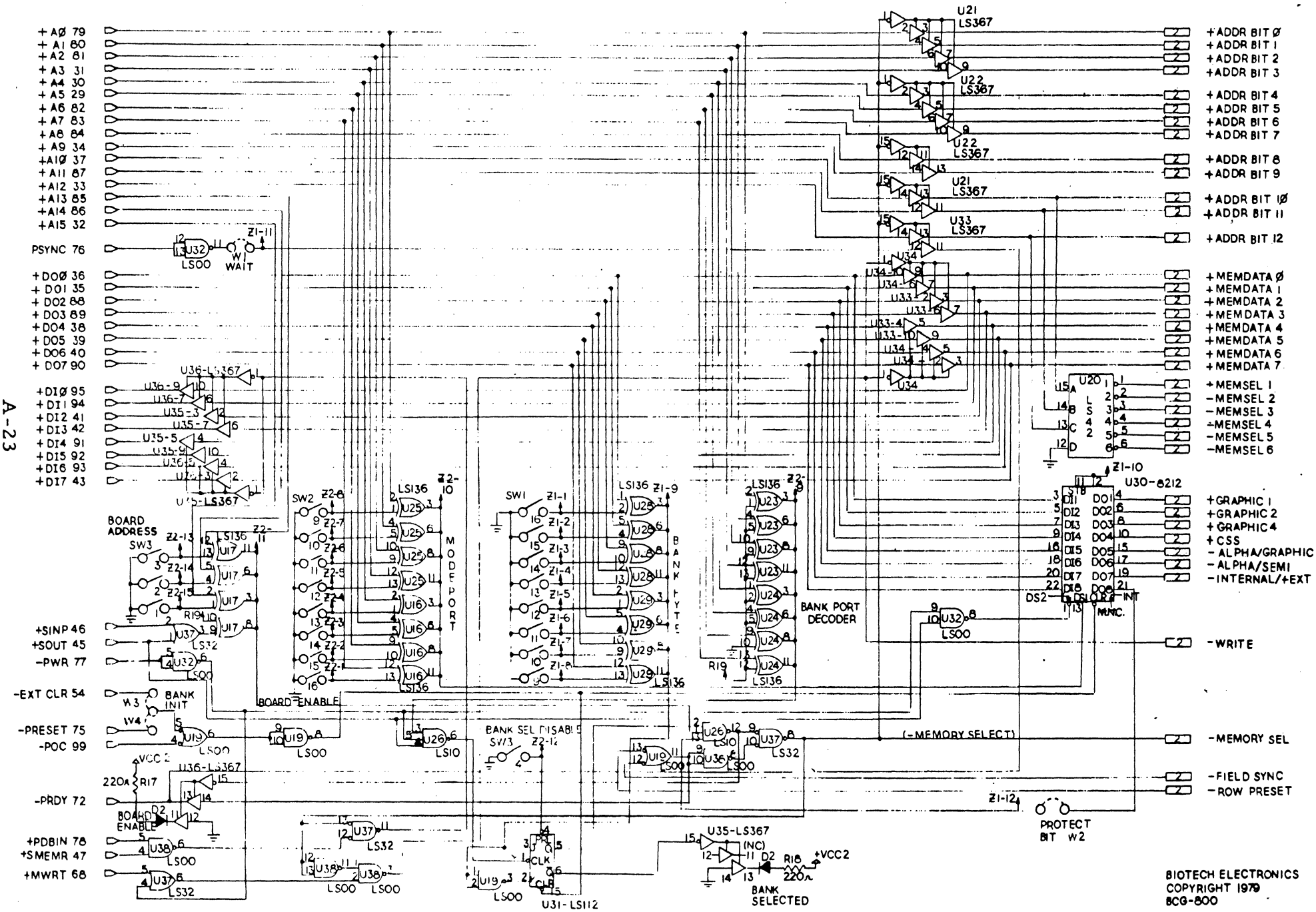
APPENDIX E

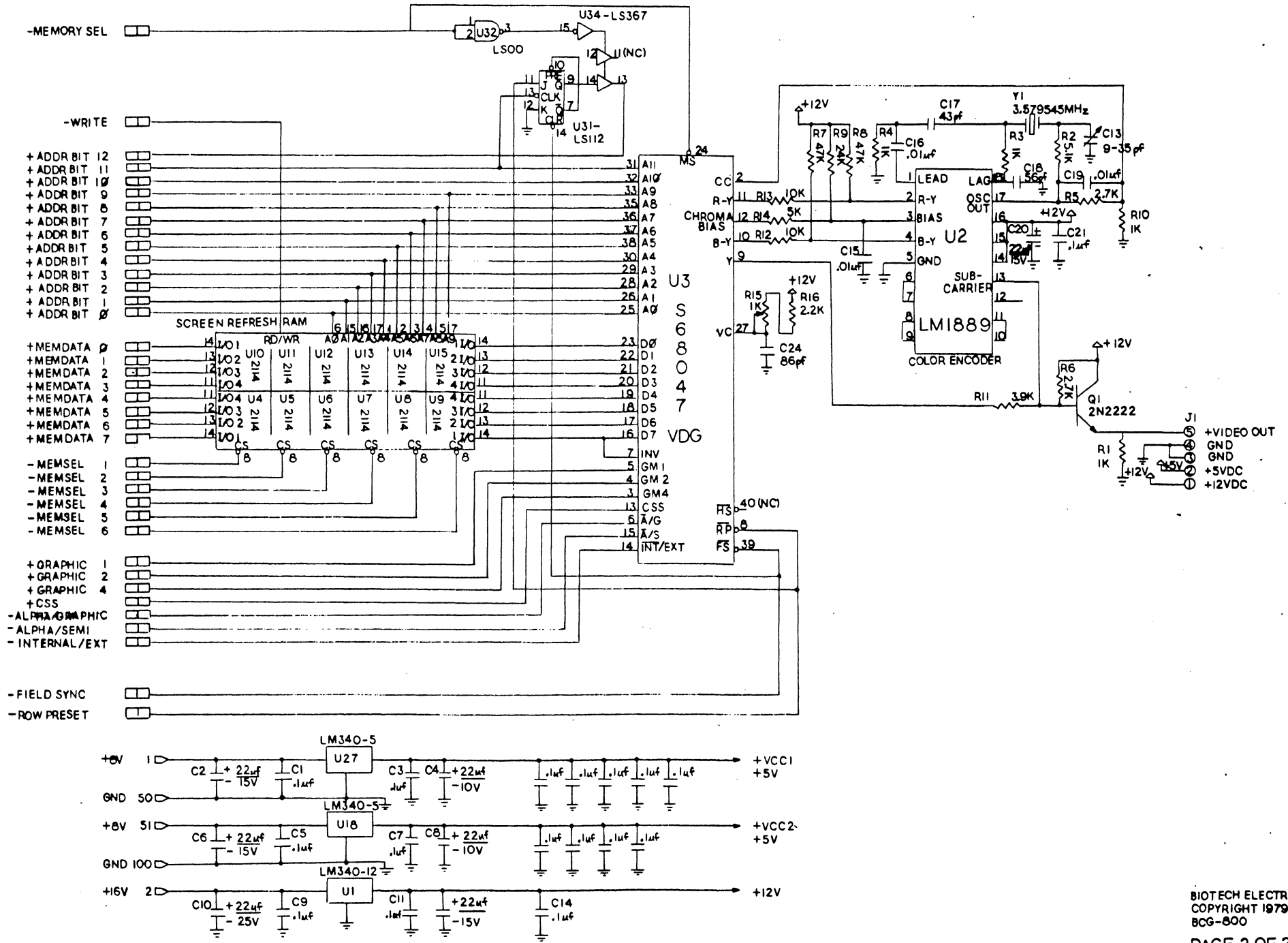
Assembly Drawing


BIOTECH ELECTRONICS
COPYRIGHT 1979
BCG-800
J1
1 2 3 4 5
C13
C14
C12
LM340-12
U1
C11
C10
C9
Y1
(XTAL)
Q1
R8
C15
U2(LM1889)
R7
C18
R6
C17
R4
C16
C19
R5
R9
R8
R3
R10
R11
R12
R13
R14
C21
C20
U3
AMI
S68047
R15
R16
C24
C23
U4
2114
U5
2114
U6
2114
U7
2114
U8
2114
U9
2114
BK EN
BD EN
D1
D2
R17
R18
C27
SW2
Z2
SW3
U10
2114
U11
2114
U12
2114
U13
2114
U14
2114
U15
2114
C26
U16
136
U17
136
C28
R19
C29
SW1
Z1
U18
LM340-5
C8
C7
C6
C5
U19
00
U20
42
U21
367
U22
367
U23
136
U24
136
U25
136
U26
10
C22
U30
8212
U28
136
U29
136
U27
LM340-5
C4
C3
C2
C1
U31
112
U32
00
U33
367
U34
367
U35
367
U36
367
U37
32
U38
00
C25
C30
WAIT
W1
PROTECT
W2
BANK RESET
W3
W4
XCLR
RST
PIN
1
50

APPENDIX F

Schematic


+A0 79
+A1 80
+A2 81
+A3 31
+A4 30
+A5 29
+A6 82
+A7 83
+A8 84
+A9 34
+A10 37
+A11 87
+A12 33
+A13 85
+A14 86
+A15 32
PSYNC 76
+D00 36
+D01 35
+D02 88
+D03 89
+D04 38
+D05 39
+D06 40
+D07 90
+DI0 95
+DI1 94
+DI2 41
+DI3 42
+DI4 91
+DI5 92
+DI6 93
+DI7 43
+SINP 46
+SOUT 45
-PWR 77
-EXT CLR 54
-PRESET 75
-POC 99
-PRDY 72
+PDBIN 78
+SMEMR 47
+MWRT 68
U21 LS367
U22 LS367
U22 LS367
U21 LS367
U33 LS367
U34
+ADDR BIT 0
+ADDR BIT 1
+ADDR BIT 2
+ADDR BIT 3
+ADDR BIT 4
+ADDR BIT 5
+ADDR BIT 6
+ADDR BIT 7
+ADDR BIT 8
+ADDR BIT 9
+ADDR BIT 10
+ADDR BIT 11
+ADDR BIT 12
+MEMDATA 0
+MEMDATA 1
+MEMDATA 2
+MEMDATA 3
+MEMDATA 4
+MEMDATA 5
+MEMDATA 6
+MEMDATA 7
U20
+MEMSEL 1
-MEMSEL 2
-MEMSEL 3
-MEMSEL 4
-MEMSEL 5
-MEMSEL 6
U30-8212
+GRAPHIC 1
+GRAPHIC 2
+GRAPHIC 4
+CSS
-ALPHA/GRAPHIC
-ALPHA/SEMI
-INTERNAL/+EXT
DS2
MISC.
-WRITE
-MEMORY SEL
-FIELD SYNC
-ROW PRESET
PROTECT BIT W2
BOARD ADDRESS SW3
BOARD ENABLE
BANK INIT W3
W4
SW2
SW1
MODE PORT
BANK BYTE
BANK PORT DECODER
BANK SEL DISABLE SW13
(-MEMORY SELECT)
U35-LS367 (NC)
BANK SELECTED
U31-LS112
R17 220Ω
R18 220Ω
+VCC2
BIOTECH ELECTRONICS
COPYRIGHT 1979
BCG-800
PAGE 1 OF 2



APPENDIX G

AMI S68047 Data Sheet

AMI

AMERICAN MICROSYSTEMS, INC.

S68047

VIDEO DISPLAY GENERATOR

January 1979

Features

- 32 x 16 (512 total) Alphanumeric Two Color Display on Black Background with Internal or External Character Generator ROM.
- Two Semigraphics Modes with Display Densities Ranging from 64 x 32 to 64 x 48 in 8 and 4 Color Sets Respectively, plus Black.
- Full Graphics Modes with Display Densities Ranging from 64 x 64 to 256 x 192 in 2 and 4 Colors.
- Full NTSC Compatible Composite Video with Choice of Interlaced and Non-interlaced Display Versions.
- Provides Microprocessor Compatible Interface Signals.
- Generates Display Refresh RAM Addresses.
- NMOS Device, Single 5V Supply, TTL Compatible Logic Levels.
- Color Set Select Pin Can Give 8 Color Displays in Full Graphics Mode.

General Description

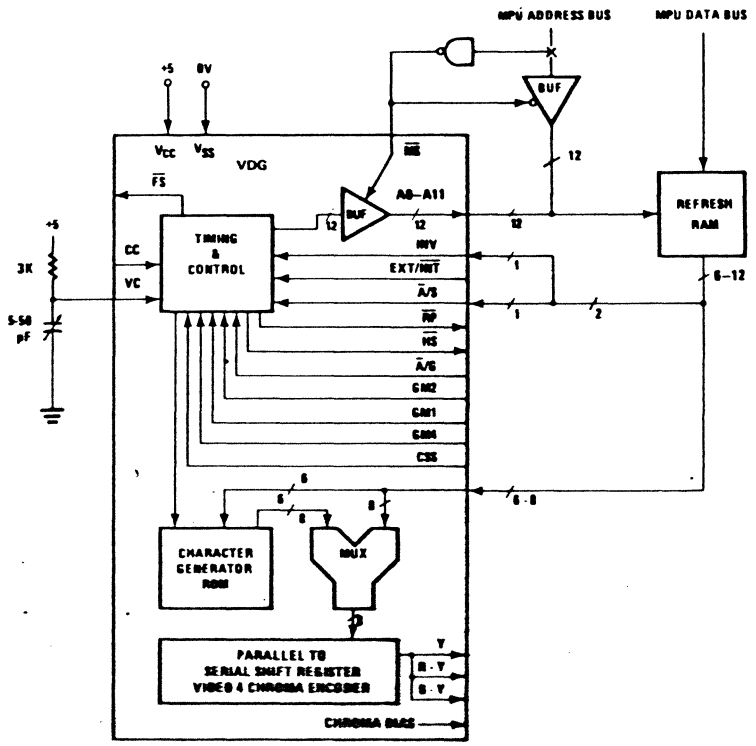
The S68047 Video Display Generator (VDG) is designed to produce composite video suitable for display on a standard American NTSC compatible black/white television or color televison or monitor.

There are three major types of display which the S68047 can generate. These include an alphanumerics mode of which there are two types, each with normal or inverted video; a semigraphics mode of which there are also two types; and full graphics mode of which there are eight types.

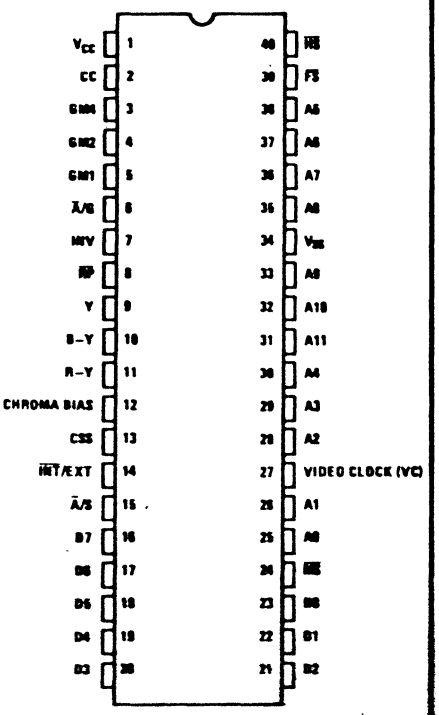
Alphanumeric Modes

The alphanumeric modes, internal and external, enable the S68047 to display a matrix of 32 x 16 (512 total) characters. The internal mode utilizes an on-chip 64 ASCII character ROM to display each character in a 5 x 7 dot matrix font. In the external alphanumeric

Block Diagram



Pin Configuration



General Description (Continued)

mode, an external memory is required, either ROM or RAM, which is used to display the 32 x 16 character matrix with each character located within an 8 x 12 dot matrix of customized font. Switching between internal and external alphanumerics modes and normal and inverted video can be accomplished on a character by character basis.

Semigraphic Modes

The two semigraphic modes, semigraphic 4 (SG4) and semigraphic 6 (SG6), subdivide each of the 512 (32 x 16) character blocks of 8 x 12 dots each into 2 x 2 and 2 x 3 smaller blocks respectively. In SG4 each block is created from 4 x 6 dots and in SG6 each block consists of 4 x 4 dots. In addition the SG4 and SG6 modes can each be displayed in 8 and 4 colors plus black.

Display switching from alphanumerics to semigraphics modes or vice versa during a raster display is called minor mode switching and can take place on a character basis.

Graphics Modes

The eight full graphics modes are divided into two major groups, 4 color and 2 color. The 4 color graphics provide 4 display densities ranging from 64 x 64 for Graphics 0 through to 128 x 192 elements for Graphics 6. The 2 color graphics also provide 4 display densities ranging from 128 x 64 for Graphics 1 through to 256 x 192 elements for Graphics 7. The latter display has the highest density of the eight graphics modes. The amount of display memory increases proportionately with increasing density of display to a maximum of 6K bytes for Graphics 7. Switching between either the alphanumeric modes or semigraphics modes and any of the full graphics modes is called major mode switching. Major mode switching can only occur at the end of every twelfth raster line scan.

Applications

Anywhere data can be more usefully presented graphically on a CRT and for a minimum cost, the VDG in conjunction with a microprocessor based controller can utilize a standard American NTSC compatible TV or monitor for such a purpose. Applications are extremely broad ranging from educational systems, video games, small low cost business/home computers to process control monitors and medical diagnostic displays.

The different modes of operation permit various cost/display presentation tradeoffs. The alphanumerics modes allow use of the TV screen as a video teletype at the most limited level of operation. Only 512 bytes, one for each character, need to be stored, each byte being a minimum of six bits wide per the ASCII code. If video inversion switching or alpha to semigraphics switching is required per character then two extra bits are required in the display RAM as shown in Fig. 5. The semigraphics modes each offer an intermediate range of graphics densities with tradeoffs in density versus color. Typical semigraphics display capabilities are bar graphs, charts, mini displays, etc. which with minor mode switching to alphanumerics modes allow annotation or captioning of the resultant display. The various graphics modes provide greater density displays with greater freedom of display presentations. The tradeoffs in increasing density are with increasing display memory size and color versus density. A minimum Graphics 0 provides a display density of 64 x 64 (4096) elements, each element being composed of a matrix of 12 (4 x 3) dots with a selection of four colors per element. Since each of the even numbered 4 color graphics modes map two bits of the data word to one picture element, each data word of memory provides four picture elements. Thus Graphics 0 requires 4096/4 = 1024 bytes of display RAM, Graphics 2 requires 8192/4 = 2048 and so on. Graphics 1, like all the odd numbered 2 color graphics modes, maps one bit of data word to one picture element. Each data word therefore maps eight elements. Graphics 1 density of 128 x 8 (8192) elements therefore requires 8192/8 = 1024 bytes of display RAM and Graphics 7, the densest display, requires 49, 152/8 = 6144 bytes of RAM. At the higher density graphics displays, the rate of change of elements approaches the maximum dot frequency of 6MHz. This video rate taxes the capabilities of most commercially available television sets and thus the quality of the display system (television or monitor) should be commensurate with the highest video rate to be used.

Electrical Specifications

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

DC (Static) Characteristics (V_{CC} = 5.0V ± 5% ; T_A = 25°C, unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input Voltage High	2.0		V_{CC}	V	
V_{IH}	Input Voltage High (Color Clock only)	4.0		V_{CC}	V	
V_{IL}	Input Voltage Low	-0.3		+0.6	V	
I_{IN}	Input Leakage Current (all inputs)		1.0	2.5	μA	V_{IN} = 0 - 5.25V; V_{CC} = 0V
$I_{L(TS)}$	Tri-State Output Leakage Current (A0 — A11)			10	μA	V_{CC} = 5.25V; $\overline{MS}$ = 0V; V_{IN} = 0.4 -2.4V
I_{LO}	Output Leakage Current ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			10	μA	V_{IN} = 2.4V; V_{CC} = 0V
V_{OH}	Output Voltage High (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)	2.4			V	I_{OH} = -100μA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0μA (A_0 - A_{11}); CL = 30pF
V_{OL}	Output Voltage Low (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			0.4	V	I_{OL} = 1.6mA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0mA (A_0 - A_{11}); CL = 30pF
I_{CC}	V_{CC} Supply Current		45		mA	V_{CC} = 5V; T_A = 25°C
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz

AC Electrical Characteristics (V_{CC} = 5.0V ± 5%; T_A = 0 - 70°C except where noted).

Alpha Internal Mode (Figure 1)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{vc}	Video Clock Frequency	5.6	6.0	6.4	MHz	
t_{ch}	Character Time	1.43	1.33	1.25	μs	
t_{ACC}	Access-Time of External Refresh RAM			0.7	μs	
t_{dot}	Dot Time	178	166	156	ns	

Alpha External Mode (Figure 1)

NOTE: All parameters are the same as in Alpha Internal Mode except t_{ACC}

t_{ACC}	Access-time of Refresh RAM + Access-time of External ROM			0.7	μs	

Semigraphics Mode (Figure 1)

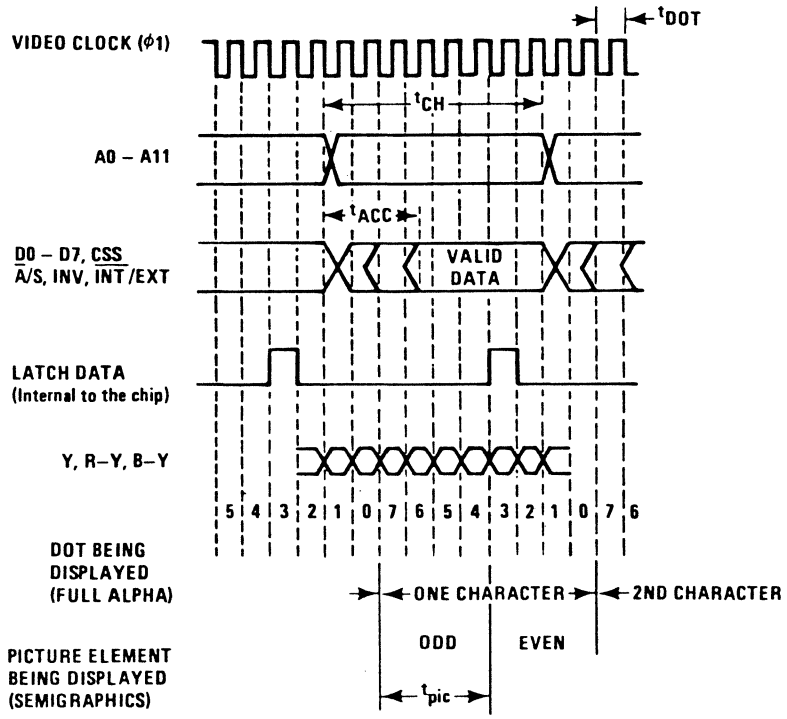
t_{pic}	Picture Element Duration	712	664	624	ns	

NOTE: All other parameters are the same as in Alpha Internal Mode.

Color Sub-carrier Input

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CC}	Frequency		3.579545 ±10 Hz		MHz	
t_r	Rise Time			10	ns	
t_f	Fall Time			10	ns	
PW_{CC}	Pulse Width		140		ns	
V_{IL}	Zero Level			0.6	V	
V_{IH}	One Level	4.0			V	
DR	Duty Ratio	40%	50%	60%		

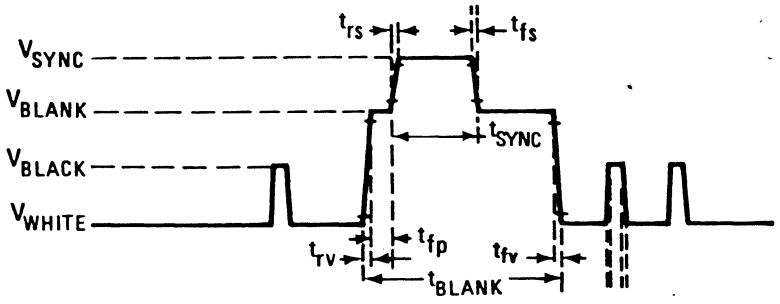
Figure 1. Refresh RAM Interface Timing



Composite Video Timing (Figure 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{SYNC}	Sync duration		4.888889		μs	
t_{fp}	Front Porch duration		1.536508		μs	
t_{BLANK}	Horizontal Blank Duration			11.44	μs	
t_{rs}, t_{fs}	Rise time and Fall time of Horizontal Sync			250	ns	
t_{rv}, t_{fv}	Rise time and Fall time of Horizontal Blank			340	ns	

Figure 2. Composite Video Timing on Y Pin



Chroma R and Chroma B Output Timing; C_L = 10pF; 1K Load (Figure 3.)

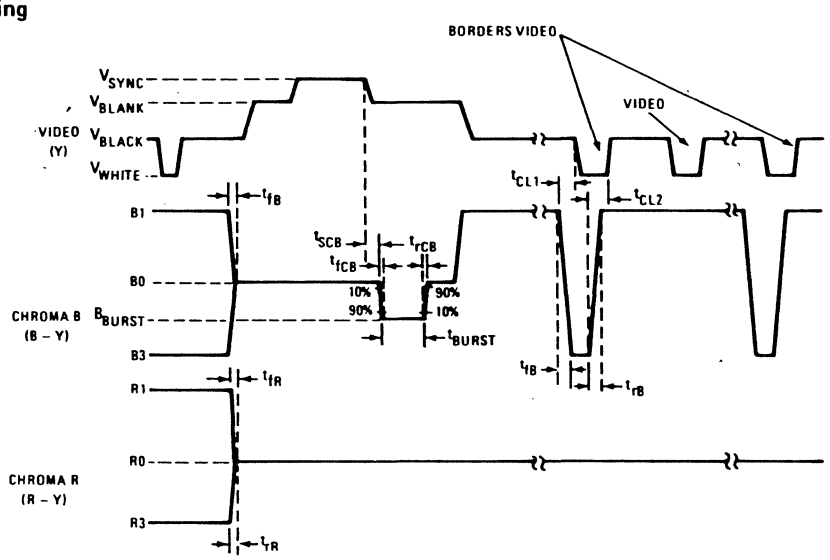
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{rB}, t_{fB} t_{rR}, t_{fR}	Color Signals rise and fall time		50		ns	Load = R-Y, B-Y input of LM1889
t_{scB}	Color Burst to Sync lag		410		ns	
t_{BURST}	Color Burst Duration		2.45		μs	
t_{fcB}, t_{rcB}	Color Burst rise and fall times		175		ns	
t_{cL1}, t_{cL2}	Video to color signals lag		75		ns	

Voltage Levels

Video (Y) and Chroma (R—Y, B—Y) Output Levels (Figure 3.) C_L = 10pF; Video Clock = 5.6MHz; T_A = 25°C; V_{CC} = 5V ± 5%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SYNC}	Sync Voltage	0	0.1	0.5	V	
V_{BLANK}	Blanking Level		1.5		V	
V_{BLACK}	Black Level		1.7		V	
V_{WHITE}	White level	2.4	4.0	V_{CC}	V	
V_{B1}, V_{R1}		2.4	4.0	V_{CC}	V	
V_{B0}, V_{R0}			2.0		V	
V_{B3}, V_{R3}		0	0.1	0.5	V	
V_{BURST}			0.4		V	
$V_{CHROMA\ BIAS}$			2.0		V	

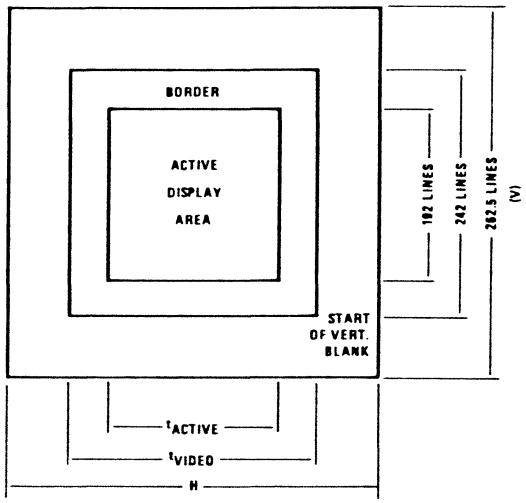
Figure 3. Chroma Timing



Video Display Format Timing (Figure 4.)

Symbol	Parameter	Typ.	Units	Conditions
H	Horizontal Scan Time	63.55557	μs	
V	Field Time	16.683337	ms	
F	Frame Time	33.366674	ms	
I/V	Field Rate	59.94004	sec^{-1}	
t_{ACTIVE}	Active Display Duration	41	μs	
t_{VIDEO}	Active Display + Border Duration	52.8	μs	
t_{RP}	Row Preset Period (12 Horizontal Scans)	762.66684	μs	

Figure 4. Video Display Format



Pin Description (Figure 2.)

V_{CC}	+5V
V_{SS}	0V
CC	(Color Burst Clock 3.579545 MHz)
VC	(Video Clock Oscillator ≅ 6MHz)
A0 — A11	(Address Lines to Display Memory; high-impedance during $\overline{MS}$ low)
D0 — D5	(Data from Display Memory RAM or ROM; D4 — D6 — Color Data in Semigraphics)
D6, D7	(Data from Display Memory in GRAPHIC Mode; Data also in ALPHANUMERIC Mode; Color Data in ALPHA SEMIGRAPHIC — 6)
R — Y, B — Y, Y	(Color and Composite Video)
CHB	(Chroma Bias; References R — Y and B — Y Levels)
$\overline{RP}$	(Row Preset in any ALPHA Mode; goes low in all modes every 12 lines)
$\overline{HS}$	(Horizontal Sync)
INV	(Inverts Video in all FULL ALPHA Modes; no effect in Semigraphics or Graphics Mode)
EXT/$\overline{INT}$	(Switches to External ROM in ALPHA Mode; between SEMIG — 4 and SEMIG — 6 in Semigraphics; no effect in all Graphics Modes)
$\overline{A}$/S	(Alpha/Semigraphics: Selects between FULL ALPHA and SEMIGRAPHICS in ALPHA Modes; no effect in all Graphics Modes)
$\overline{MS}$	(Memory Select; forces VDG Address Buffers to high-impedance state; also used as a strobe in TEST and RESET functions). The TV screen is forced black when $\overline{MS}$ = low
$\overline{A}$/G	(Switches between ALPHA and GRAPHIC Modes)
$\overline{FS}$	(Field Synchronization; LOW during vertical blanking time)
CSS	(Color Set Select: Selects between two ALPHA Display Colors; between two Color Sets in SEMIGRAPHICS — 6 and FULL GRAPHICS: selects Border Color in 8 Graphic Modes)
GM1, GM2 GM4	(Graphics Mode Select; select one of eight Graphic Modes; no affect in Alpha and Semigraphic Modes; GM1, GM2 select TEST and RESET mode when $\overline{A}$/G = 0 and $\overline{MS}$ pin is strobed low)

Internal Description

Internally the VDG is the combination of four integrated subsystems (timing and control, MUX, address buffers and shift registers to form the VDG function. A block diagram of the VDG is shown on Page 1. Each subsystem is described below.

Timing and Control

The timing and control subsystem of the VDG uses the 3.58MHz color frequency to generate timing information. It accepts the color clock (generated off-chip) (CC) input and generates timing for the horizontal sync, horizontal blank, field sync, vertical blank and row preset signal ($\overline{RP}$) for external character generator ROM. The video clock is generated on-chip by external RC and generates addresses A0 — A11 to address the external refresh RAM.

The color-set-select (CSS) input to the Timing and Control subsystem of the VDG is used to determine the color-set of the display.

The EXT/$\overline{INT}$ input has two functions. In the full alphanumeric mode, it is used to select either internal ROM or external ROM. It is also used to select between semigraphic 4 and semigraphic 6 mode in semigraphic modes ($\overline{A}$/S = 1).

The INV input is utilized by the timing and control subsystem to invert the display while in full alpha mode.

Internal Description (Continued)

$\overline{A}$/G, $\overline{A}$/S, GM1, GM2, GM4 inputs to the timing and control subsystem determine which of the fourteen VDG modes is to be used (Table 1).

MUX

The MUX provides the function of selecting the data source to be displayed. The source can be either internal ROM or external ROM or RAM. For the internal alphanumeric mode, the data source is the internal ROM. For all other modes (semigraphic and graphics) the data source is external ROM/RAM.

Address Buffers

The address buffers provide the buffering required for external drive (ROM/RAM). The buffers are tri-stated when the $\overline{MS}$ pin goes low and tri-states the buffers so that VDG does not interfere with the MPU operation. The $\overline{FS}$ pin (output) from the VDG signals to the MPU that the TV is in the vertical retrace mode and the MPU can directly change the data in the display memory during that time with no interruption to displayed data.

Shift Registers

The two shift registers serialize bytes coming from internal/external ROM/RAM for conversion to data on the TV screen. The shift registers output also goes to the chroma encoder circuitry to determine the color of each individual dot. Each shift register has 4-bits.

VDG

The VDG has fourteen modes, grouped in three sets. They are:

4 Alphanumerics Modes
- ☐ Normal internal alpha
- ☐ Inverted internal alpha
- ☐ Normal external alpha
- ☐ Inverted external alpha

2 Semigraphics Modes
- ☐ Semigraphics 4
- ☐ Semigraphics 6

8 Full-graphics Modes
- ☐ 4 Graphics four-color modes
- ☐ 4 Graphics two-color modes

The six alphanumeric modes can be switched among themselves on a character-by-character basis. Switching within the six alphanumeric modes is referred to as minor-mode switching. All other mode switching is referred to as major-mode switching.

The display can be major-mode switched on after any multiple of twelve rows have been completed. This is signalled to the MPU by $\overline{RP}$ output going low. Switching among the full-graphics modes is permitted at the end of every twelfth row just as in major-mode switching.

Table 1 tabulates the modes of the VDG. The data structures for each mode are listed in Table 7. Table 2 and Table 3 show the Alpha Select Mode and Graphic Select Mode configurations respectively. Table 4 gives the Two-color Graphics and Full-alpha Color Specification. Table 5 shows the semigraphics and Four-color Graphics Color Specification.

Table 1. VDG Modes

	Mode	Description	Memory
I.	ALPHA INTERNAL	32 x 16 BOXES: 5 x 7 CHARACTER	512 x 7 – 8
II.	ALPHA INTERNAL INVERTED	IN 8 x 12 BOX	
III.	ALPHA EXTERNAL	32 x 16 BOXES: 5 x 7 OR 7 x 9 CHARACTERS	512 x 7 – 8
IV.	ALPHA EXTERNAL INVERTED	IN 8 x 12 BOX OR FULL 8 x 12 LIMITED GRAPHICS	
V.	ALPHA SEMIGRAPHICS 4	32 x 16 BOXES: 2 x 2 ELEMENTS PER BOX; EIGHT COLORS PLUS BLACK	512 x 4 – 7
VI.	ALPHA SEMIGRAPHICS 6	32 x 16 BOXES 2 x 3 ELEMENTS PER BOX; FOUR COLORS PLUS BLACK	512 x 6 – 8
VII.	GRAPHICS 0	64 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	1K x 8
VIII.	GRAPHICS 1	128 x 64 ELEMENTS: TWO COLORS PER ELEMENT	1K x 8
IX.	GRAPHICS 2	128 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	2K x 8
X.	GRAPHICS 3	128 x 96 ELEMENTS: TWO COLORS PER ELEMENT	1.5K x 8
XI.	GRAPHICS 4	128 x 96 ELEMENTS: FOUR COLORS PER ELEMENT	3K x 8
XII.	GRAPHICS 5	256 x 96 ELEMENTS: TWO COLORS PER ELEMENT	3K x 8
XIII.	GRAPHICS 6	128 x 192 ELEMENTS: FOUR COLORS PER ELEMENT	6K x 8
XIV.	GRAPHICS 7	256 x 192 ELEMENTS: TWO COLORS PER ELEMENT	6K x 8

Table 7. Detailed Description of VDG Model

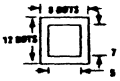
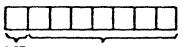
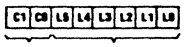
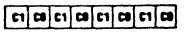
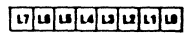
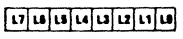
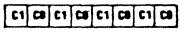
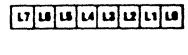
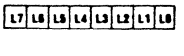
VDG PINS								COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
A/G	A/S	INT/EXT	GM2	GM1	GM0	CSS	INV	CHARACTER COLOR	BACK-GROUND	BORDER	DISPLAY MODE	DETAIL		
0	0	0	X	0	0	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows			ALPHANUMERIC INTERNAL mode uses internal character generator with on-chip 64 ASCII character ROM to display each character in 5x7 dot matrix font.
							1	Black	Green					
						1	0	Blue	Black	Black				
							1	Black	Blue					
0	0	1	X	0	0	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows			ALPHANUMERIC EXTERNAL mode uses external ROM or RAM to display 512 characters in custom fonts each in 8x12 dot matrix.
							1	Black	Green					
						1	0	Green	Black	Black				
							1	Black	Green					
0	1	0	X	0	0	X	X	L_x C_2 C_1 C_0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Cyan 1 0 1 1 Red 1 1 0 0 Blue 1 1 0 1 Cyan/ Blue 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 32 Display elements in rows			SEMIGRAPHICS 4 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into four equal parts. The dominance of each block is determined by the corresponding bit (L0-L3) on the VDG data bus. Color of each block is determined by 3 bits (C0-C3).
0	1	1	X	0	0	0	X	L_x C_1 C_0 0 0 0 Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Cyan 1 1 1 Red 1 0 0 Blue 1 0 1 Cyan/ Blue 1 1 0 Magenta 1 1 1 Orange		Black	64 Display elements in columns 48 Display elements in rows			SEMIGRAPHICS 6 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into six equal parts. The luminance of each part is determined by the corresponding bits (L0-L5) on the VDG bus. Color of each block is determined by 2 bits (C0, C1).
						1	X							
1	X	X	0	0	0	0	X	C_1 C_0 0 0 Green 0 1 Yellow 1 0 Cyan 1 1 Red 0 0 Blue 0 1 Cyan/ Blue 1 0 Magenta 1 1 Orange		Green	64 Display elements in columns 64 Display elements in rows			GRAPHICS 0 mode uses a maximum of 1024 bytes of display RAM in which one pair of bits (C0, C1) specifies on picture element. (Ex.).
						1				Cyan/ Blue				
1	X	X	0	0	1	0	X	L_x Color 0 Black 1 Green		Green	128 Display elements in columns 64 Display			GRAPHICS 1 mode uses a maximum of 1024 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1		0 Black 1 Cyan/ Blue		Cyan/ Blue				
1	X	X	0	1	0	0	X	Same color as Graphics 0		Green	128 Display elements in columns 64 Display elements in rows			GRAPHICS 2 mode uses a maximum of 2048 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
						1				Cyan/ Blue				
1	X	X	0	1	1	0	X	Same color as Graphics 1		Green	128 Display elements in columns 96 Display elements in rows			GRAPHICS 3 mode uses a maximum of 1536 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1				Cyan/ Blue				
1	X	X	0	1	0	0	X	Same color as Graphics 0		Green	128 Display elements in columns 96 Display elements in rows			GRAPHICS 4 mode uses a maximum of 3072 bytes of display RAM in which one pair of bits (C0, C1 specifies one picture element (Ex.)
						1				Cyan/ Blue				
1	X	X	1	0	1	0	X	Same color as Graphics 1		Green	256 Display elements in columns 96 Display elements in rows			GRAPHICS 5 mode uses a maximum of 3072 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1				Cyan/ Blue				
1	X	X	1	1	0	0	X	Same color as Graphics 0		Green	128 Display elements in columns 192 Display elements in rows			GRAPHICS 6 mode uses a maximum of 6144 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
						1				Cyan/ Blue				
1	X	X	1	1	1	0	X	Same color as Graphics 1		Green	256 Display elements in columns 192 Display elements in rows			GRAPHICS 7 mode uses a maximum of 6144 bytes of display RAM in which one bit (Lx) specifies one picture element.
						1				Cyan/ Blue				

Table 2. Alpha Mode Select

GM2	GM1	$\overline{A}$/G	$\overline{A}$/S	$\overline{INT}$/EXT	INV	$\overline{MS}$	MODE
X	0	0	0	0	0		INTERNAL ALPHANUMERICS
X	0	0	0	0	1		INTERNAL INV. ALPHA
X	0	0	0	1	0		EXTERNAL ALPHA
X	0	0	0	1	1		EXTERNAL INV. ALPHA
X	0	0	1	0	X		SEMIGRAPHICS – 4
X	0	0	1	1	X		SEMIGRAPHICS – 6
0	1	0	X	X	X	STROBED LOW	TEST ROM
1	1	0	X	X	X	STROBED LOW	RESET

NOTES: 1) GM4 pin has no effect when $\overline{A}$/G = 0.

2) Invert pin has no effect except in Internal Alpha or External Alpha.

3) Under normal operation, care should be taken not to take GM1 pin HIGH, when $\overline{A}$/G pin is LOW. If this happens, any of the following conditions will occur depending on the status of $\overline{MS}$ and GM2 pin:

   a) The VDG might go to TEST mode.

   b) The VDG might be reset.

   The VDG will not return to normal operation unless $\overline{A}$/G and GM1 pins are returned to LOW level and $\overline{MS}$ pin is strobed.

4) X = Don't care.

Table 3. Graphic Mode Select

	$\overline{A}$/G	GM4	GM2	GM1	MODE
GRAPHICS 0	1	0	0	0	64 x 64 4 – COLOR
GRAPHICS 1	1	0	0	1	128 x 64 2 – COLOR
GRAPHICS 2	1	0	1	0	128 x 64 4 – COLOR
GRAPHICS 3	1	0	1	1	128 x 96 2 – COLOR
GRAPHICS 4	1	1	0	0	128 x 96 4 – COLOR
GRAPHICS 5	1	1	0	1	256 x 96 2 – COLOR
GRAPHICS 6	1	1	1	0	128 x 192 4 – COLOR
GRAPHICS 7	1	1	1	1	256 x 192 2 – COLOR

NOTE: $\overline{A}$/S, $\overline{INT}$/EXT, INV pins have no effect when $\overline{A}$/G = 1.

Table 4. Two-Color Graphics and Full-Alpha Color Specification

CSS PIN	COLOR OF 'ON' DOTS
0	GREEN
1	CYAN-BLUE

Table 5. Semigraphics and Four-Color Graphics Color Specification

4-COLOR GRAPHICS	SEMI-GRAPHICS – 6	SEMI-GRAPHICS – 4
EVEN BIT	D6	D4
ODD BIT	D7	D5
CSS	CSS	D6

COLOR SET 1	0 0 0	GREEN
	0 0 1	YELLOW
	0 1 0	CYAN
	0 1 1	RED
COLOR SET 2	1 0 0	BLUE
	1 0 1	CYAN/BLUE
	1 1 0	MAGENTA
	1 1 1	ORANGE

NOTE: In Semigraphics – 6, if any bit D0 – D5 is '0', then picture element corresponding to that bit would be black. In Semigraphics – 4, if any bit D0 – D3 is zero, then the picture element corresponding to that dot will be black.

Table 6. Two-Color Graphics and Four-Color Graphics Border Color Specification

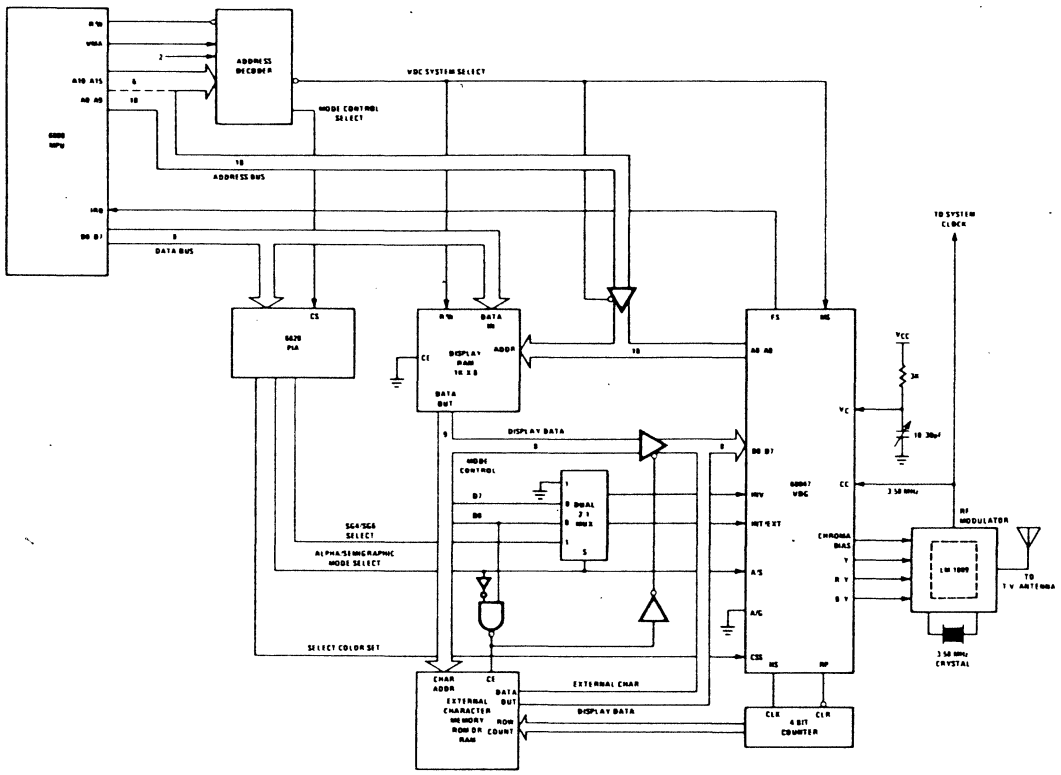
CSS PIN	BORDER COLOR
0	GREEN
1	CYAN-BLUE

Typical System: A typical S6800 microprocessor based S68047 system is shown on Figure 5. This system has the capability of displaying internally and externally generated characters, semigraphics 4 and 6 modes with mode switching control from the microcomputer input/output ports. A full graphics system configuration would be similar in complexity with possibly additional display RAM for the denser graphics modes. The National Semiconductor LM1889 RF modulator shown, has an on chip 3.58 MHz oscillator which can provide the microcomputer system clock as well as the color burst reference for the S68047. Other RF modulators are available through various commercial channels. Only 512 bytes are needed to display the 512 character blocks on a TV screen. However, because of current static RAM configurations (ie. 1Kx1 & 1Kx4) the extra 512 bytes available in the 1Kx9 RAM shown can be used as scratchpad by the host microcomputer system.

Ordering Information

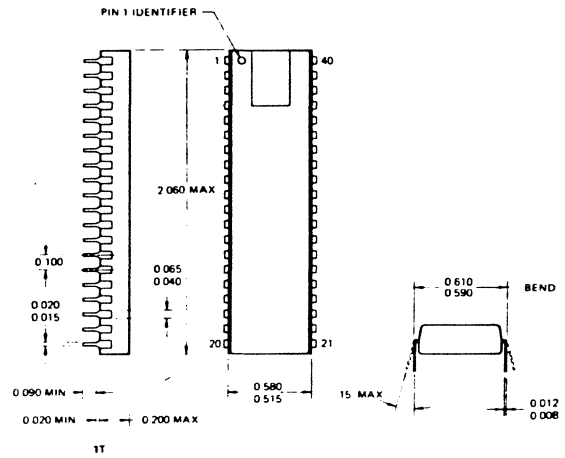
Ordering No.	No. Pins	Package	Temp. Range	Description
S68047	40	Ceramic	0-70°C	VDG non-interlaced
S68047P	40	Plastic	0-70°C	VDG non-interlaced
S68047Y	40	Ceramic	0-70°C	VDG interlaced
S68047YP	40	Plastic	0-70°C	VDG interlaced

Figure 5. Typical System (Alphanumeric Internal/External & Semigraphics 4 and 6 Modes.)

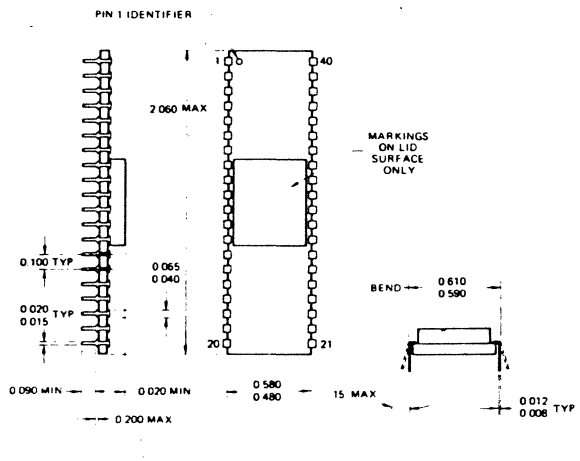


Physical Dimensions

40-Pin Plastic



40-Pin SLAM



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APPENDIX H

IC Pin Outs

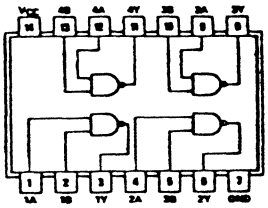
APPENDIX H

IC Pin Outs

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$

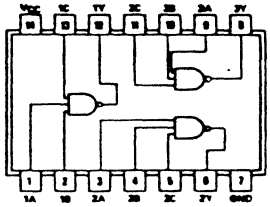


74LS00

TRIPLE 3-INPUT
POSITIVE-NAND GATES

10

positive logic:
$Y = \overline{ABC}$

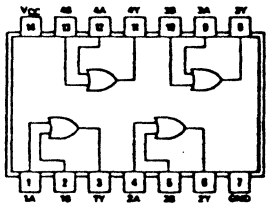


74LS136

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

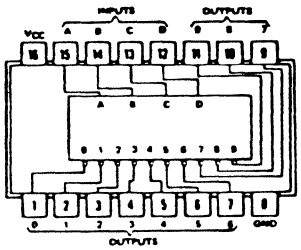
positive logic:
Y = A+B



74LS32

4 LINE-TO-10-LINE DECODERS

42 BCD-TO-DECIMAL



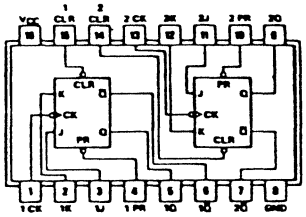
74LS42

IC Pin Outs (Con't.)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH
112 PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

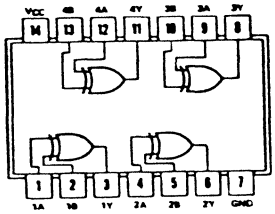


74LS112

QUAD EXCLUSIVE-OR GATES

136

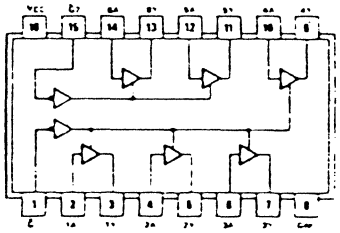
positive logic: $Y = A \oplus B = A\bar{B} + \bar{A}B$



74LS136

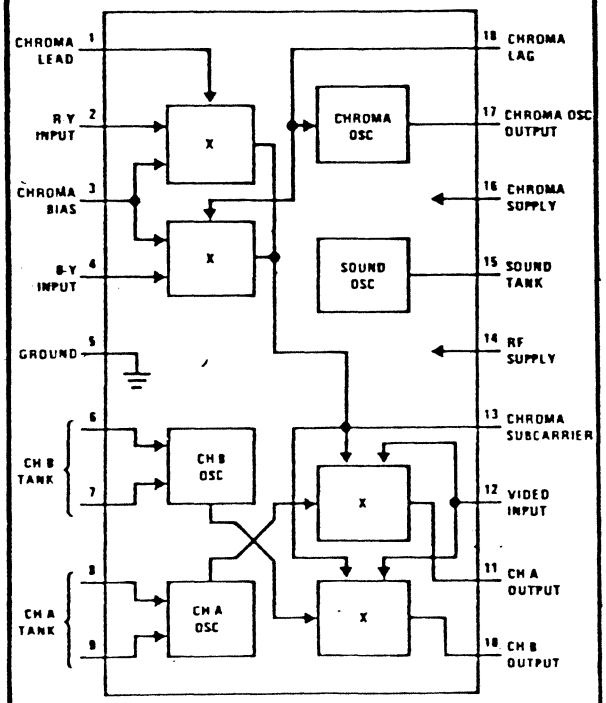
HEX BUS DRIVERS

367 NONINVERTED DATA OUTPUTS
4-LINE AND 2-LINE ENABLE INPUTS
3-STATE OUTPUTS



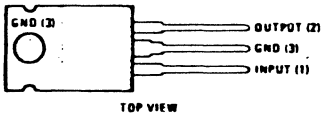
74LS367

Dual-In-Line Package



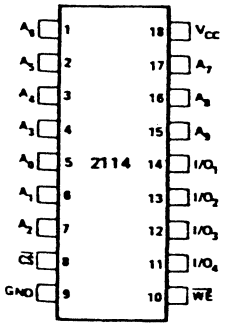
LM1889

IC Pin Outs (Con't.)

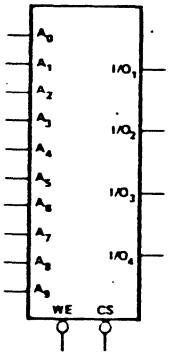


LM340-5
LM340-12

PIN CONFIGURATION



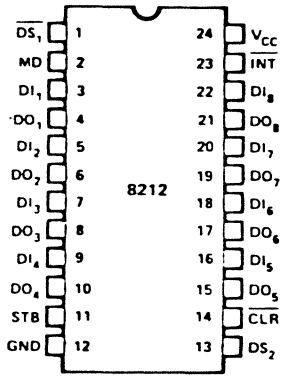
LOGIC SYMBOL



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

2114

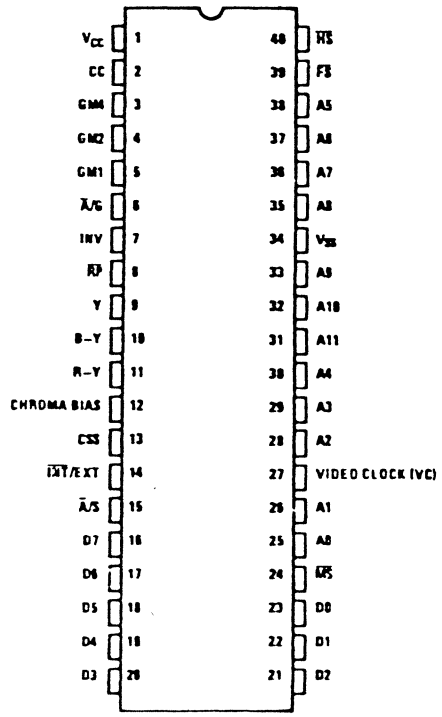


PIN NAMES

DI_1–DI_8	DATA IN
DO_1–DO_8	DATA OUT
$\overline{DS_1}$, DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

8212

Pin Configuration



AMI S68047

APPENDIX I

Warranty

APPENDIX I

Limited Warranty

Biotech Electronics warrants the electrical and mechanical parts and workmanship of this product to be free of defects for a period of:

a) 90 days from the date of purchase, if purchased in kit form, or,

b) 180 days from the date of purchase, if purchased assembled and tested.

If such defects occur, Biotech Electronics will repair the defect at no cost to the purchaser. This warranty does not extend to bare board (BCG-800B) purchases. This warranty does not extend to defects resulting from improper use or assembly by purchaser, nor does it cover transportation to the factory. Also, the warranty is invalid if all instructions included in the accompanying documentation are not carefully followed. Should a unit returned for warranty repair be deemed by Biotech Electronics to be defective due to purchaser's action, then a repair charge not to exceed $20.00 without purchaser's consent will be assessed. This warranty is made in lieu of all other warranties, express or implied, and is limited to the repair or replacement of the product described in this manual.

APPENDIX J

Resistor Color Code

APPENDIX J

Resistor Color Code

Color	Significant Figure	Decimal Multiplier	Tolerance (%)
Black	0	1.00	
Brown	1	10.00	
Red	2	100.00	
Orange	3	1,000.00	
Yellow	4	10,000.00	
Green	5	100,000.00	
Blue	6	1,000,000.00	
Violet	7	10,000,000.00	
Gray	8	100,000,000.00	
White	9	1,000,000,000.00	
Gold	---	0.10	5
Silver	---	0.01	10
No Color	---	---	20

May 1979

ERRATA SHEET

Page	Section	Description
2-10	Voltage Check	The capacitors referred to when checking for +5VDC should read C4 and C8 instead of C2 and C6, respectively.
2-11	Voltage Check	The capacitor referred to when checking for +12VDC should read C12 instead of C10.
3-4	Mode Control Port	Referring to Table 1 (S68047 Mode Selection), column 1 of Hex CSS reads 08, 28, 68, 18, 19, 20, 21, 22, 23, 24, and 25. This should read 08, 28, 68, 18, 19, 1A, 1B, 1C, 1D, 1E, and 1F, respectively.
3-4	Mode Control Port	In paragraph 1, line 90 referred to should read line 80.
3-4	Mode Control Port	In the Mode Test Program, line 80 reads: 80 OUT 00, N+C. This should read: 80 OUT 01, N+C.
A-7	Software Configuration	In paragraph 2, 0100H referred to should read 1000H.
A-7	Software Configuration	In paragraph 3, 36H referred to should read 38H.
A-8	Graphics Driver Subroutine	Line 200 reads as follows: 0005 D3 07 0200 OUT A,MDPT This should read: 0005 D3 00 0200 OUT A,MDPT
A-8	Graphics Driver Subroutine	Line 400 reads as follows: 0037 D3 07 0400 OUT A,MDPT This should read: 0037 D3 00 0400 OUT A,MDPT
A-9	Graphics Driver Subroutine	Line 910 reads as follows: 0088 FE 07 0910 CPI A,000H This should read: 0088 D3 00 0400 OUT A,000H
A-9	Graphics Driver Subroutine	Line 1040 reads as follows: 00A0 11 00 C0 1040 LXI D,0C000H This should read: 00A0 11 00 C0 1040 LXI SCADR

Page	Section	Description
A-10	Graphics Driver Subroutine	Line 1390 reads as follows: 00D4 11 00 C0 1390 LXI D,0C000H This should read: 00D4 11 00 C0 1390 LXI SCADR
A-15	Object Code	The following addresses should be changed in the object code to read as follows:

Location:	Now Reads:	Change to:
0006	07	00
0038	07	00
0089	07	00