

SINGLE STAGE
(FLYBACK-DISCONTINUOUS)

POWER SUPPLY

MAINTENANCE MANUAL

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NOTE: The descriptions and component designations in this manual refer to the OL25-1001. However, all flybackdiscontinuous supplies have analogous circuits which operate in a manner similar to the OL25-1001.

Figure 1
single stage (flyealk-discontinuous) power supply SMPLIFIED SCHEMATIC


GENERAL THEORY OF OPERATION

The flyback converter-discontinuous mode derives its name from the fact that during each cycle a point is reached where current ceases to flow in either the primary or secondary windings. Thus, the flux in the transformer virtually "ceases" at some point in the cycle.

The converter design is extremely simple. This class of converter operates as a blocking oscillator under the following control law: The output is linearly proportional to the current flowing in the power switch when it turns off, i.e., the output voltage is proportional to the amount of energy loaded into the core in the form of a magnetic field. The greater the field, the higher the output voltage.

The feedback loop regulates output voltages by adjusting the turn-off point of the power switch. Switching frequency is around 25 kHz at full power, and operating frequency is inversely proportional to the output power. The duty cycle remains relatively constant for a constant line voltage.

Input Circuit


Figure 2
INPUT CIRCUIT
a. RFI Filter. Consists of $\mathrm{L} 1, \mathrm{Cl}, \mathrm{C} 2$ and C 3 . The purpose of this circuit is to filter out 20 kHz and above switching noise, preventing it from being transmitted back out the input line.
b. Fuse. F1 is included to protect the PC board traces and to reduce fire and personal hazard in the event of catastrophic supply failure. Boschert strongly recommends the use of an additional external line fuse for further protection. A Littlefuse $3 A G$ series or equivalent rated at 1-1/2 $A$ is sufficient.
c. Voltage Doúbler Circuit is a method of allowing the supply to operate from either a 115 VAC or 220 VAC source. In the 115 VAC mode (strap in) capacitors C4 and C5 charge on alternate line half cycles. The voltage which appears across each capacitor is approximately the peak input voltage (about 150 V ). The total voltage to the switching regulator is about 300 V .

In the 220 VAC mode (strap out) the input rectifiers act as a full wave bridge rectifier, charging C4 and C5 to approximately the peak input voltage (about 300 V ). Resistors R14 and R15 force C4 and C5 to charge equally, and discharge the capacitors when the power is turned off.
d. Inrush Limiting is accomplished with thermistor RI. When cool, its resistance is high. When the supply is initially turned on, it prevents a huge surge current from flowing into C4 and C5, which are initially discharged. In operation, the normal input current quickly heats R1 decreasing its resistance by a factor of about 10. Since C4 and C5 are fully charged by this time, there is no further need for surge limiting. When the supply is turned off, R1 cools and C4 and C5 discharge. The circuit is designed so that the discharge time constant and cooling time constant are roughly equal. Thus, if the supply is turned back on before R1 has fully cooled, the inrush current is limited by a combination of the charge remaining on C4 and C5, and the resistance of R1.
e. Energy Storage in capacitors C4 and C5 insure that the supply will continue to operate within regulation limits for a minimum of 16 mS after the input line has fallen below limits or failed. This allows time for information in a volatile memory to be stored permanently before system failure following line interruption or line brownout.


Figure 3
POWER SWITCH CIRCUIT

In the first half of the power cycle, switch Ql will turn on and load energy into the transformer in the form of a magnetic field. Switch Q1 will then turn off.

The second half of the power cycle is described in the Output Circuit description.

When power ( +300 ) is applied, a small trickle current through R3 begins to bias Q1 on. As the full supply voltage +Vcc begins to appear across winding one ( W 1 ), transformer action induces about 6 V across winding two (W2). CR2 is forward biased, and regenerative feedback current from W2 quickly forces Q1 into saturation.

Now the current in Wl begins to ramp up linearly. A voltage ramp also appears across $R 5$ due to the current ramp.

Meanwhile, W2 is also charging C9 to about +6 V via R9 and CR3. When this voltage rises high enough, Q3 is biased on. This also turns on current buffer Q2. Q1 begins to turn off because Q2 and Q3 are conducting base drive away from Q1. The current ramp in W1 stops rising because $Q 1$ is beta limited and is coming out of saturation. The rate of current change ( $\mathrm{di} / \mathrm{dt}$ ) has become negative, therefore the voltage polarity on the windings must change. W2 has now reversed voltage (the dotted end is now positive) and it helps turn off Q1 by completely backbiasing the base emitter junction via R5, R4 and C8. When Q1 is off, and the voltage across all transformer windings has reversed, C10 is charged via CR4 and R9.
(The second half of the cycle is continued in the Output Circuit Section.)

Output Circuit


Figure 4
OUTPUT CIRCUIT

This section describes the second half of the power cycle. The first half was described in the Power Switch Circuit description.

In the first half of the power cycle, switch Q1 turned on and loaded energy into the transformer in the form of a magnetic field. Q1 then turned off, and the collapsing magnetic field is now driving positive the dotted ends of all transformer windings, looking for a discharge path.

As the voltage rises on the dotted ends of all the windings, it will eventually forward bias diodes CR5 through CR8. The magnetic field in the transformer rapidly collapses by discharging energy into the outputs. The C-L-C PI filters in the output store and filter this energy.

When the magnetic field has sufficiently collapsed, diodes CR5 through CR8 stop conducting. There is enough energy left in the core to allow it to "ring back." That is, the current in the secondary suddenly reduces its rate of discharge when the diodes stop conducting. di/dt changes, and the dotted end of all windings becomes negative. Q1 begins to conduct again. This is the start of the next cycle.


Figure 5
MODULATOR CIRCUIT

The modulator varies the point at which Q1 turns off thereby regulating the output voltages.

In the absence of any feedback loop, Q1 would continue loading energy into the core until a fixed point was reached. This fixed amount of energy would be subsequently discharged into the load. If the load changed, the output voltage would change because Q1 was still loading a fixed amount of energy into the transformer. To compensate for load changes, the feedback loop varies the point at which Q1 turns off, thereby varying the amount of energy loaded in the core. The greater the load, the more energy is loaded into the core. This accomplishes regulation.

During normal operation, C9 and C10 are each charged to about 6 V , or about 12 V total. Since the junction of C 9 and C 10 is referenced essentially to ground via R5, the base-emitter junction of Q3 must be back
biased due to the base voltage determined by dividers R8 and R9. When Q1 turns on, the voltage across R5 ramps up. This makes the entire modulator circuit voltage rise relative to ground. Eventually a point is reached where Q3 is biased on, which turns off Q1, terminating the first half of the cycle.

The point at which Q3 turns on can be varied by changing the ratio of R8 to R9. The opto-isolator transistor, $Q A 3$, acts as a variable resistor to change this ratio. If the +5 V output tended to fall due to an increase in load, for example, the opto-isolator transistor would turn off, making the base voltage on Q3 more negative. It would take longer for the voltage ramp on $R 5$ to reach a point where Q3 was biased on. More energy would be loaded into the transformer, which would be discharged into the load, raising the output voltage.


Figure 6
MAIN FEEDBACK LOOP

This circuit maintains the +5 V output at a constant voltage. The loop compares a voltage divided down from the +5 V output via R 13 to a 2.75 V reference within the 430 integrated circuit. A proportional current is sunk by the 430 , driving the opto-isolator diode via R12. RIl provides bias current for the 430. Cl3 frequency compensates the loop.

The auxiliary (other than +5 V ) outputs are "semi-regulated." That is, because of the tight magnetic coupling of all the outputs, an increased load on an auxiliary output lowers the volts per turn of the transformer, which is reflected in the +5 V output (which begins to go down). The feedback loop works to restore the 55 V output, and in so doing partially compensates for the load change on the auxiliary output. Boschert calls this "semi-regulation."

## Overvoltage Protection



Figure 7
OVP CIRCUIT

The purpose of overvoltage protection is to protect the user's load from an overvoltage condition caused by supply failure. All standard Boschert supplies incorporate this feature. Also, Boschert supplies require OVP on only one output. If all outputs have simple passive filtering, and if one output should rise due to supply failure, they all would rise. Thus, protection is needed on only one output.

If the +5 V output exceeds $6.25 \mathrm{~V} \pm 0.75 \mathrm{~V}$, the SCR pulls the +12 V supply down (to about 1.5 V ) and activates the short circuit protection. The +12 V supply is used to insure clean foldback. Pulling the +5 V down to 1.5 V might not exceed the foldback point, and might simply deliver a lot of power to the SCR, destroying it.

This circuit can be cleared by cycling line power.

## Spike Catcher Circuit



Figure 8
SPIKE CATCHER CIRCUIT

The purpose of the spike catcher circuit is to prevent high voltage turn off transients on the collector of Q1 from destroying it.

C4 and C5 are the input capacitors, charged to about 300 V . When Q1 has finished loading energy into the transformer core and turns off, WI begins to look like a current source. Its dotted end becomes positive and the voltage rises. Although the discharge path is ultimately through the output, there is enough leakage inductance in W1 to allow the voltage to rise to a destructive value. However, as the dotted end of $W 1$ reaches 300 V , so does the dotted end of W 3 . (They both have the same number of turns.) As the voltage tries to rise further, CR1 conducts and clamps the collector voltage to 600 V . This prevents the destruction of Q1.

## TROUBLESHOOTING INSTRUCTIONS

## EQUIPMENT NEEDED:

150 MHz oscilloscope with isolated ground
1 DVM or VTVM with isolated ground
1 Isolation transformer
$i$ IA Variac ( $0-130 \mathrm{Vac}$ )
2 Adjustable lab supplies, $0-20 \mathrm{VDC}$ @ 500 mA , with adjustable current limit. A.good supply of resistors and clip leads.

1 AC voltmeter (0-130Vac)

CAUTION: Lethal voltages are present in this supply. Only authorized service technicians should perform these tests. Use AC isolated equipment in all tests.

NOTE: It is desirable to use an AC isolation transformer in performing all tests to minimize shock hazard. The kVA rating of this transformer should be three times the maximum supply power to avoid AC line waveform distortion.

NOTE: Steps 1 thru 9 are intended as passive tests to be performed with the supply completely disconnected from line power. To prevent any oscillations, connect jumper wire from the anode of CR5 to the cathode of CR8.


Figure 9

1. Use DVM to check the continuity of the input fuse (FI), thermistor (TRI)
bridge rectifier ( $B R-1$ ), diodes CR1
thru CR8 for proper continuity.
Replace as necessary.
2. Connect a lab supply ( 15 V with current limit at 500 mA ) across the $A C$ input terminals. After an initial surge, no current should flow. Reverse the leads and repeat. If any current flows, check the input section for shorts.


Figure 10
3. Check the operation of Q1. Set the lab supply for 15 V with the current limit set for 500 mA . Connect a 220 ohm resistor in series with the positive output and connect this to the 115 V input terminals as shown. With the DVM across the collector-emitter terminals of Q1, momentarily parallel R3 (220K) with a 100 ohm $1 / 4 \mathrm{~W}$ resistor. Is
 voltage drop across Q1 as follows?

Vce (Q1)
R3 not paralleled $13.5 \mathrm{~V} \pm 1 \mathrm{~V}$ R3 paralleled $\quad 1.5 \mathrm{~V} \pm 1 \mathrm{~V}$

Yes - Go to Step 4
No - Replace Q1 and repeat Step 3

Figure 11


Figure 12
4. Check the operation of Q2 and Q3. Use a DVM or a lab supply with the output set at +5 V , current limit at 10 mA . Check the continuity of Q2 and Q3 for opens or shorts. Replace as necessary. Then go to Step 5.
5. Check overvoltage protection operation. Set both supplies to +5.0 V with the current limit set to 100 mA . Connect the first supply across the +5 V output and return. Connect the second supply across the +12 V output and return. (The +12 V output should be the one which the anode of the SCR is connected to. If not, the supply should be connected to the output which is connected to the SCR anode. Now slowly ramp up the voltage on the first supply. At $6.25 \mathrm{~V} \pm 0.75 \mathrm{~V}$ on the first


Figure 13 supply, does the second supply suddenly go into current limit?

$$
\begin{aligned}
& \text { Yes - Go to Step } 7 \\
& \text { No - Go to Step } 6
\end{aligned}
$$

6. Check CR9. Set lab supply current limit to 100 mA and the voltage to 0 . Connect the positive terminal to the +5 V output and the negative terminal to the return. Put a DVM across CR9. Turn the voltage slowly up to 10V, or to the point where the supply limits. Does the DVM voltage ramp up to $5.6 \mathrm{~V} \pm 0.25 \mathrm{~V}$ and stop?

$$
\text { Yes - Replace CR4, and Repeat Step } 5
$$

No - Replace SCR-1 and Repeat Step 5


Figure 14
7. Check A2. Set lab supply to +5.OV (Ilim $=300 \mathrm{~mA}$ ) across +5 V output. Read voltage across R11 with DVM while adjusting pot R13. Are the voltages as follows?

RI3 fully clockwise $\quad 3.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ R13 fully counterclockwise $0.2 \mathrm{~V} \pm 0.2 \mathrm{~V}$

Yes - Go to Step 8
No - Replace A2 and repeat Step 7
8. Check A3 and modulator. Hook up first supply ( +5 V , $17 \mathrm{l}=3=300 \mathrm{~mA}$ ) across the +5 V output. Hook up second supply ( +5 V , Ilim $=300 \mathrm{~mA}$ ) across the modulator. Watch the voltage across R8 with the DVM while adjusting R13. Are the voltages as follows?

$$
\text { R13 fully clockwise } \quad 3.0 \mathrm{~V} \pm 0.5 \mathrm{~V}
$$

RT3 fully counterclockwise $0.3 \mathrm{~V} \pm 0.2 \mathrm{~V}$

Yes - Go to Step 9
No - Replace A3, repeat Step 8

NOTE: This concludes all the passive tests. Disconnect all supplies, DVM, and jumper
from CR5 to CR8 before proceeding.
9. Disconnect all connections made for the passive tests. Plug the supply into the Variac and turn the voltage up to 115 Vac . Is the voltage across the input capacitor(s) within the following limits?

Supply designed for 115 Vac only $150 \mathrm{~V} \pm 10 \mathrm{~V}$

Supply designed for 220Vac only


Figure 17
$300 \mathrm{~V} \pm 20 \mathrm{~V}$

Supply 115/220 strappable
$300 \mathrm{~V} \pm 20 \mathrm{~V}$

Yes - Go to Step 10

No - Look for faulty component in input circuit. Repeat Step 9.
10. Use an oscilloscope to check the voltage waveform on the collector of Q1 with respect to emitter.


Figure 18

With proper waveform, notice that duty cycle is roughly $50 \%$.


Figure 19
Proper Waveform
Horizontal - $5 \mu \mathrm{~s} / \mathrm{Div}$.
Vertical - 50V/Div.

With no output load, the supply "burps" every 120 ms or so. This is known as the burp mode. (The supply waits about 120 ms , tries to turn on, the SCR fires because there is no +5 V load to keep it from overshooting, and it folds back and waits 120 ms again.)


Figure 20
No load waveform
Horzontal - $5 \mu \mathrm{~s} /$ Div.
Vertical - 50V/Div.

In an overload condition, all output voltages and currents are very low. Notice the very short duty cyle (about 12\%) which typifies the overload condition. Under a heavy overload, the supply "burps" every 500 ms or so.


Figure 21
Overload Waveform
Horizontal 5 $\mathrm{s} /$ /Div.
Vertical 50V/Div.


Figure 22
Output Short Waveform Horizontal 5 $\mu \mathrm{s} /$ Div.
Vertical 50V/Div.
11. Use the oscilloscope on each or any output to determine if any faults are occurring.


Figure 23


Figure 24
Proper Output Waveform
Horizontal - 50ms/Div.
Vertical - 2V/Div.


Figure 25
No Load on Outputs
Horizontal - 50ms/Div.
Vertical - 2V/Div.

The much longer fall time of an output indicates a short on some other output than the one measured.

No rise or fall indicates the short is on this output.


Figure 26
Short on some other output
Horizontal - 50ms/Div.
Vertical - 2V/Div.


Figure 27
Short on this output Horizontal - 50ms/Div. Vertical - 2V/Div.

| APPLICATION |  | REVISION |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NEXT ASSY | USED ON | Rev | eco | DESCRIPTION | DATE | APPROVED |
| 40006 |  | 1 | 1284 | PRE RELEASED FOR PRLD |  |  |
|  |  | A | 2259 | RELEASED FOR PROD. | 9-13-78 | $\sqrt{117}$ |
|  |  | B | 2385 | $\begin{aligned} & \text { CORRECTED CURRENT } \\ & \text { CALL-OUTS ADDED } \\ & \text { PARA. } 3 \text { ON PG. } 3 \\ & \hline \end{aligned}$ | 12-18-78 | $\begin{aligned} & 2 x \\ & w h \end{aligned}$ |
|  |  | c | 5355 | CORAECTED NDTE BC. $5 H T 30 F 3 .$ | 11-2.79 | RKS (H0N0 |
|  |  | D | 4072 | INCORPORATED | 4.23-80 | go |

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 BOSCNETY HCORPQRATEG.


VISUAL INSPECTIONS
TURN ON AND TURN OFF
SWITCH WAVEFORM
CURRENT MAX. LIMIT RANGE
CURRENT MIN. LIMIT RANGE
INVERTER WAVE FORMS SAME
INVERTER PERIOD RANGE
INVERTER PEAK-PEAK VOLTAGE

## SEE PAGE 3 FOR LIMITS

$\square$

OUTPUT VOLTAGE-CURRENT TEST POINTS:

| OUTPUT |  |
| :---: | :---: |
| 1 | $\frac{+5}{\text { VOLTAGE }}$ |
| 2 | $\frac{+12}{-12}$ |
| 3 | $V$ |
| 4 | -5 |
| 5 | $V$ |
| 0 | $V$ |


[SET VOLTAGE HERE]



OVA | 5994 B | (IN752) |
| :--- | :--- |
|  | 5993 B |$($ IN751)

| $\frac{\text { Minimum }}{5.7}$ |
| :--- |


| MAXIMUM |
| ---: |
| 6.8 |

】 110 VAC
SNAP -ON
AlIBLE NOISE
FACTORY SELECT PROCEDURE FOR RH, SEE PAGE 3. BURN IN NO. OUI
$\square$ STRAPABLE test cable no. os


FACTORY SELECT PROCEDURE FOR RU

1. a. SET LOAD AT: 3A, +5V

$$
\begin{aligned}
& .5 A,+12 V \\
& .5 A,-12 V \\
& .5 A,-5 V
\end{aligned}
$$

b. SET LINE VOLTAGE AT gOVAc
c. SELECT RA FOR +5V OUTPUT TO EE

$$
4.95 \mathrm{~V} \leq+5 \mathrm{~V} \text { OUTPUT } \leq 5.05 \mathrm{~V}
$$

2. a. SET LINE VOLTAGE TO lloVAC
b. SET ALL LOADS TO O AMB
C. LOAD LV SLOWLY. IV OUTPUT
VOLTAGE MUST REGULATE TO $5 V \pm 0.05 O V A T+5 V$ OUTPUT CURRENT OF $\leqslant 0.8$ AMP.

CURRENT MAX LIMIT TEST
a. SET LINE VOLTAGE TO $I I V V A C$
b. SET LOAD TO: +5V 3A

$$
\begin{array}{ll} 
\pm 12 V & 0.5 A \\
-5 V & 0.5 A
\end{array}
$$

c. INCREASE OUTPUT CURRENT OF +5V AND NOTE MAXIMUM CURRENT. MAXIMUM CURRENT, I MAX, MUST BE: 6.5A $\leq$ I MAX $\leq 8.0 A$. IF CURRENT LIMIT IS NDT IN SPEC, CHANGE RI 4 TO ANDTHER VALUE BETWEEN 470 AND OK (NOMINAL VALUE INSTALLED is 1.2 K ). LOWER THE RESISTOR VALUE TO BRING THE CURRENT LIMIT DOWN or raise the value to increase the current LIMIT,


| APPLICATION |  | REVISION |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NEXT ASSY | USED ON | LTR | DESCRIPTION | DATE | APPROVED |  |
|  |  | 1 | 1986 | PRE RELEASED FOR PROD |  |  |
|  | A | ZХ59 RELEASED FOR PROD. | $9-13.78$ | ROM |  |  |


| PIN \# FUNCTION |  |
| :---: | :---: |
| 1 | FSV |
| 2 | RETUFN |
| 3 | RETURN |
| 4 | $+12 V$ |
| 5 | $-12 V$ |
| 6 | -5 |
| 7 | $A C I N$ |
| 8 | $A C I N$ |

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 when pernission of an officer of ERT ENCORPORATEO.



D ESHOP GRAFHICS/ACCUPRESS

8. FACTORY SELECT R4 GR14.
7. FOR QA SPEC SEE DWG NO. 20270
6. FOR PINOUT CHART SEE DWG NO 20267
5. FOR OUTLINE INSTALLATION SEE DWG NO. 20168
4.
3. FOR TEST SPEC SEE DWG NO. 20269
2.

1. FOR SCHEMATIC SEE 20139

Notes:







| APPLICATION |  | REVISION |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Next Assy | USED ON | Rev | ECO | description |  |  | DATE | APPROVED |
| 45-10157-01 | XL25-1001 | $!$ | - | PR | REL | FOR PROD | U6:\% | Le Sx. |
| $\left[\begin{array}{l}5-10152-01 \\ 5-10152-02\end{array}\right.$ | XL25-3001 XL25-4001 | A |  | REL | FOR | PROD. |  |  |

## PIN ORIENTATION



NOTE 1 - For 110 V as shown; For 220 V strap JP1 to E2 (applicable to the XL25-3001/4001 only).

| PIN |  | voltage |  |
| :---: | :---: | :---: | :---: |
| 2 | INPUT | A.C. NEUT/HOT |  |
| 3 | INFUT | A.C. HOT |  |
| 1 | CHAS GND |  | MODEL NO. XL-25 |
| 4 | OUTPUT | -5V |  |
| 5 | OUTPUT | -12V | MFG. ASSEMBLY NO. |
| 7 | OUTPUT | $+5 \mathrm{~V}$ |  |
| 8 | OUTPUT | +12V |  |
|  | OUTPUT |  | mating |
|  | OUTPUT |  | CONNECTOR |
|  | OLIPLT |  |  |
|  | OUTPUT |  |  |
| 6 | RETURN |  | AUTOMATIC SHORT CIRCUIT RECOVERY $\square$ |
|  | NOTUSED |  | AUTOMATIC SHORT CIRCUIT SHUT DOWN $\square$ |
|  |  |  | DWG. NO. 97-10147 REV A |







table a
ASSYNO MODEL NO VOLT RATING
10. UNLESS OTHERWISE SPECIFIED: RESISTORS ARE $1 / 4 \mathrm{w}$ : DIODES ARE $\operatorname{IN} 4004$; CAPACITANCE is in uf

9 APPLY A THIN COAT OF HEATSINK COMPOUND (PIN 74-7765) BEFORE ASSY.
[8] Core must be 15 above ejafo.
7) apply labels in approx position shown not covering the component identification.
[5 R2 \& RIB MUST BE MOUMITEL OFF EIARD.
4. ALL heAtsinks must be mounted . 10 IN. off the boaro
3. ALL RESIStors two (2) watts and above must be mounted in in off the h'ald uilejs thel.wile specified.
2. FOR REFERENCE DWG SEE LIST OF MATERIAL

T mark assy ioent no current rev level in approx location shown per table a
NOTES:


