B 1700

CENTRAL SYSTEM

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Burroughs

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SECTION

I

INTRODUCTION
AND
OPERATION

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INTRODUCTION

The B1700 System is a small scale data processing system used for general purpose data processing. The B1700 System contains an S-Memory Processor and a low speed I/O system. The S-Memory Processor, Memory and power supplies are described within this manual. The S-Memory Processor is a micro-programmed processor. Figure I-1 illustrates the B1700 System.

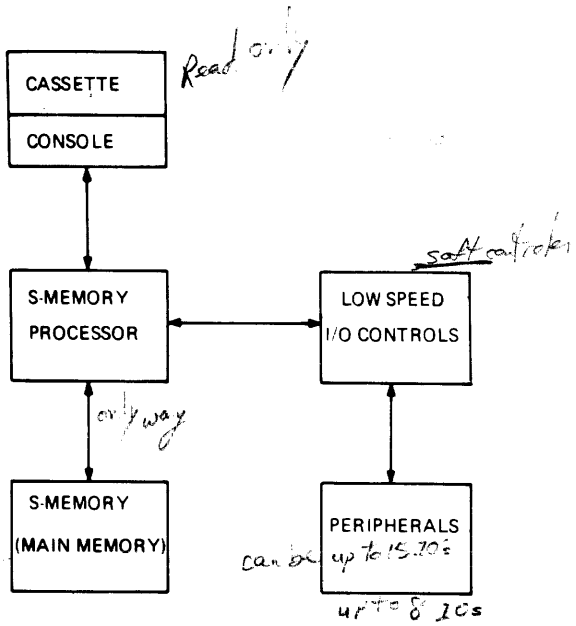

Fig. I-1 B1700 SYSTEM FUNCTIONAL BLOCK DIAGRAM

MICRO INSTRUCTION

The B1700 Central System performs its operations by executing a set of low level (micro) instructions which are fetched and executed from the Main Memory of the system. There are approximately 25 of these micro instructions along with the associated logic sections, arithmetic sections, registers and pseudo registers required for performing a specific operation such as an add, data movement, I/O operations, etc. A micro instruction is hereby defined as the least amount of work an instruction could possibly perform within this system.

MACRO INSTRUCTION

A "macro" instruction is the maximum amount of work which can be done by one instruction. In the B1700 these macro instructions are "built" by the programmer by using a series of micro instructions. An example of this would be an Add where a macro performs a complete add with storage of the sum and the detection of carries automatically. In the micro instruction set there is not an add instruction. The machine however, thru a series of micro instructions can perform an add operation and hence the add is "built" by the programmer.

MICRO PROGRAMMING

The micro programming of the B1700 or S-Memory Processor has several definite advantages. One advantage which is most obvious being ease in modification of the macro. That is, a macro can be changed through software rather than requiring a modification of the logic. The second obvious advantage is that micro programming allows the hardware to be "tailored" to the idiosyncrosies of a particular language such as COBOL, FORTRAN, etc.

B1700 CENTRAL SYSTEM

The B1700 Central System as previously discussed is a low level micro programmed processor and has been provided the necessary logic to perform the operations of a normal central processing unit. A basic block of the central system is shown in Figure I-2.

The B1700 System may be divided into the following functional areas:

Processor
Memory
I/O Sub-System
Power

Each of these areas are described generally within Section I of this manual. A detailed description is contained in Section II with the exception of the I/O Sub-System which is described in the B1700 System I/O Sub-System Technical Manual.

PROCESSOR

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The S-Memory Processor, consisting of 9 logic cards, console and cassette loader contains the necessary logic to perform the arithmetic, logical and data movement/storage functions of a data processor. It also controls all I/O operations. The following is a list of the areas within the Processor and the Console with Cassette loader.

1. Cassette Tape Loader
2. Console
3. Main Exchange
4. Local Memory
5. 24-Bit Arithmetic and Combinatorial Unit
6. 4-Bit Arithmetic and Combinatorial Unit
7. Processor Registers

Figure I-2 is a basic block diagram of the processor and the following descriptions contain the basic functions of each of the seven portions of the processor listed.

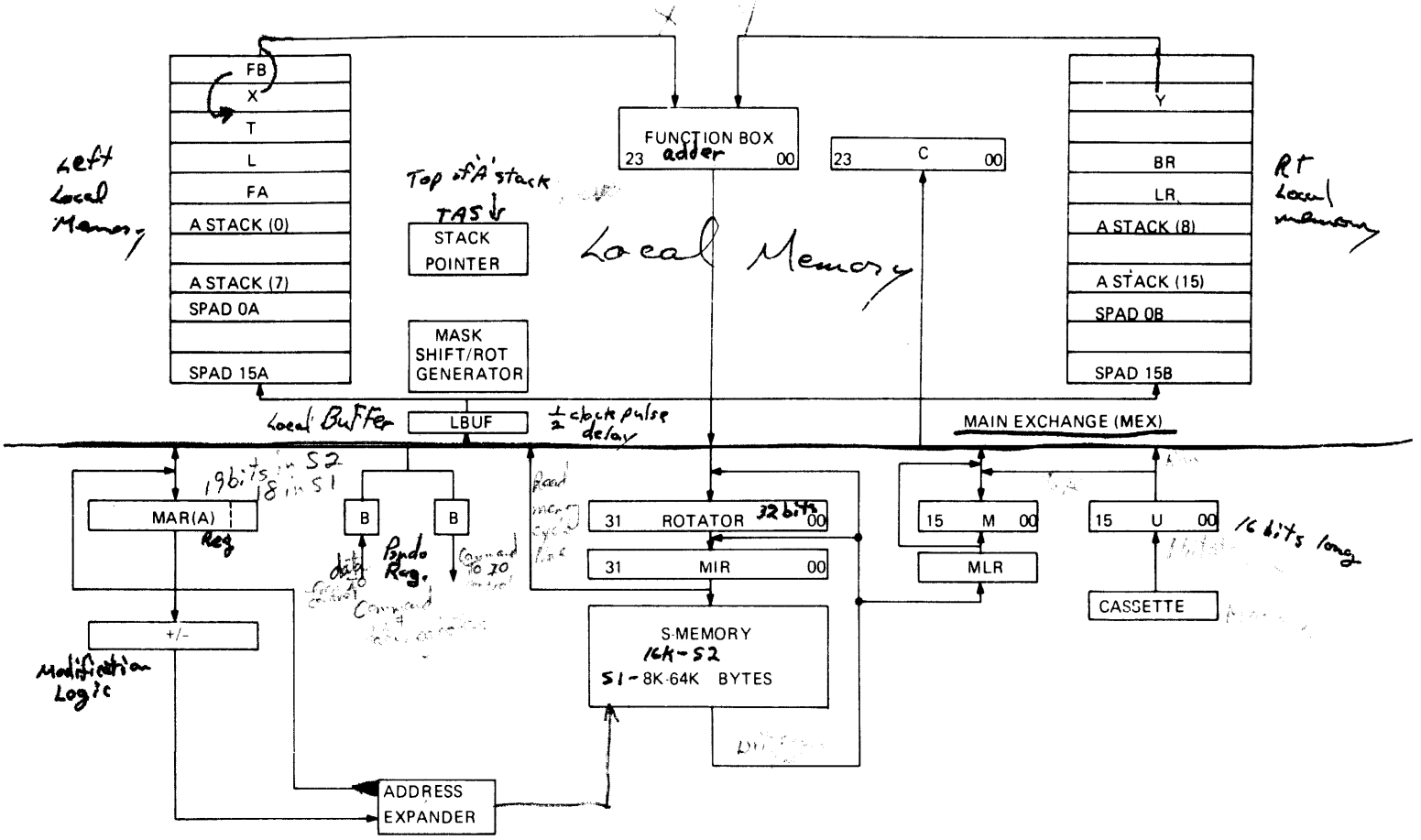


Fig. I-2 BASIC BLOCK DIAGRAM

CASSETTE TAPE

The C assette is physically located on the Console of the B1700 as shown in Figure I-3. The Cassette on the Console is a "read only" device, used for program loading and for storage of MTR/Diagnostic Routines which may be executed directly from the Cassette or entered in the Main Memory prior to execution. The physical characteristics of the Cassette are as follows:

Speed-10 ips (Inches per second)
Density-800 BPI (Bits per inch)
Tape Length-300 ft.
Data Format-Bit Serial/8 bits per character

For a detailed description of the Cassette and format used on entering micros via the Cassette refer to Section II.

CONSOLE

The Console of the B1700 is used for displaying/entering data of various registers within the S-Memory Processor. Data also may be loaded into memory from the console. The console may also be used to display memory data. The Console contains a mode switch to place the machine in the RUN/STEP/TAPE mode of operation. As previously described, the Cassette is a part of the Console and therefore, the Console contains the necessary switches/lamps for operation of the Cassette. Refer to Figure I-4.

Fig. I-3

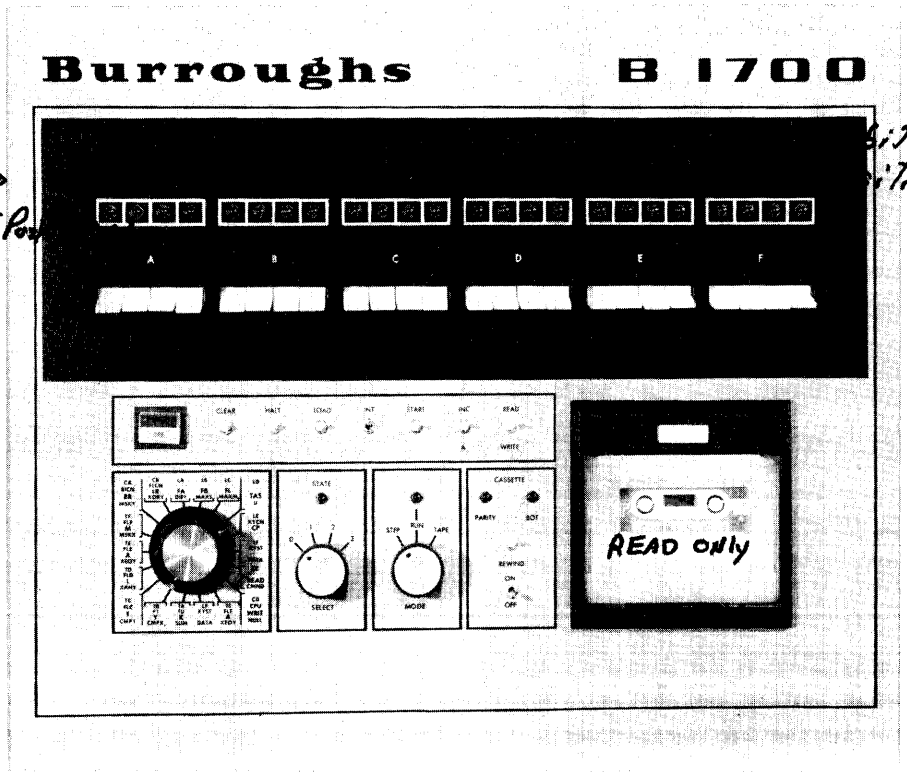


Fig. I-4

MAIN EXCHANGE (MEX)

The Main Exchange is the main bus within the processor. It is used for movement of data within the processor and is 24 bits wide. It is also used to transfer 4 bit data from source to destination in addition to the normal 24 bit word.

The Main Exchange, when the machine is halted, receives data from the register selected by the console switches and this data is automatically displayed on the console lamps. If the load button is depressed when the processor is halted, the contents of the console switches will be placed on the Main Exchange and subsequently loaded into the register which has been previously selected.

LOCAL MEMORY

The Local Memory is that part of the machine where the majority of the registers reside. Several registers such as the C Register and MAR (A) have been made discreet because they must always be present for operations whereas if they were located in the Local Memory they would not be available for the controlling functions which they must provide. Each of these registers and micros which affect these registers are described in Section I.

Local Memory is divided into three main sections of logic; LBUF, Left (A) Half, and Right (B) half. The following is a brief description of each section and its contents:

A. LBUF

LBUF is the input to the Local Memory and receives its input from the Main Exchange. LBUF is 24 bits in width and is used to hold the data to be written into local memory for an additional half clock period to allow the local memory write logic to complete the write operation.

B. Left (A) Half

Left Half of the local memory or sometimes referred to as "A" Half contains the following 4, 16, and 24-bit registers:

Registers – FB
X
L
T
FA

(Note that FA, FB, L, and T may be divided into other registers)
In addition to the above mentioned register, Left Half of Local Memory contains words zero through seven of "A" Stack and words zero through fifteen of Left Scratchpad.

C. Right (B) Half
The Right Half sometimes referred to as "B" Half of Local Memory contains only 24 bit registers in addition to words eight through fifteen of "A" Stack and words zero through fifteen of Right Scratchpad. The following are the 24 bit registers located in Right Half of Local Memory:
Registers – Y
TEMPB
BR
LR

TEMPB (Temporary Buffer)
TEMPB is a temporary buffer in the right half of local memory. TEMPB is not addressable as a source or sink and is therefore not available to the programmer. The function of TEMPB is strictly hardware and its use is for the 7C Read/Write Memory micro or the 8D Scratchpad Relate FA micro. When used for either of these micros it is a temporary holding register. TEMPB is described in detail within Section II of this manual.

24 BIT ARITHMETIC AND COMBINATORIAL UNIT (24 BIT FUNCTION BOX)
The 24 Bit Function Box is used to produce the normal arithmetic or logic functions between two 24 bit operands.

Input
Operand inputs to the function box are the X and Y registers and control inputs are CYF, CPU, and CPL which will be discussed as a portion of the C Register.

Outputs
Outputs of the Function Box include SUM, DIFFERENCE, AND, OR, EXCLUSIVE-OR, CARRY OUT, BORROW, EQUAL TO, GREATER THAN and LESS THAN functions. Also it has as outputs the complement of the X and Y Registers and the masked outputs of X and Y.

Arithmetic
The arithmetic section of the function box is controlled by CPU, CPL, CYF and the operand inputs X and Y. The arithmetic operations consist of either an add or subtract with the operands being binary data or four Bit BCD data designated by CPU as follows:

CPU =00 Binary
01 Four Bit BCD
10 UNDEFINED
11 UNDEFINED

The operand length is defined by the value contained in CPL with a maximum value of 24 bits. If, for example, CPU = 01 and CPL = 24 then the operand input from X and Y is considered to be six 4-bit BCD characters. Either the SUM or DIFFERENCE is obtained by addressing the SUM or DIFFERENCE pseudo registers (SUM OR DIFF) via a Register Move type micro operator. In the case of the DIFFERENCE, the value in Y is subtracted from the value in X. The input CYF for a SUM is a carry in and for a DIFFERENCE is a borrow.

Logic Functions – And/Or/Exclusive Or
The logical functions which may be obtained are addressed as pseudo source registers. The AND/OR/EXCLUSIVE OR functions are merely the ANDing, ORing or exclusive ORing of the contents of the X or Y. Those pseudo registers associated with these functions are XANY, XORY, and XEOY Registers. If the value in CPL is less than 24, then the most significant bits are filled with zeros.

One's Complement
The one's complement of the X and Y Register may be obtained by using a Register Move type micro which addresses either the pseudo CMPX or CMPY Register.

Mask of X or Y

Normally by addressing the X or Y Register as a source, 24 bits are obtained. If less than 24 bits are desired the Mask of X or Mask of Y (MSKX or MSKY) pseudo registers may be addressed. Depending upon the value in CPL, from one to 24 bits of X or Y may be obtained as source data with zero bits in the most significant bit positions.

Conditions/States

In addition to the logical and arithmetic functions, the 24 Bit Function Box can produce various conditions/states which are addressable as source registers only. These conditions/states are referred to as the three pseudo registers-BICN (Binary Conditions), XYCN (X-Y Conditions) and XYST (X-Y States). All of the above pseudo registers are four bit registers and their functions with bits shown in Table I-1.

BIT	XYCN	BICN	XYST
0	X > Y	CYL	X ≠ 0
1	X < Y	CYD	Y ≠ 0
2	X = Y	CYF	INT
3	MSBX	LSUY	LSUX

TABLE I-1
Condition States

The XYCN Register produces the relational conditions of X is greater than, less than or equal to Y. The MSBX bit is true if the Most Significant Bit of the X Register as designated by CPL is true.

The BICN Register produces CYL which is a Carry Out Level, CYD a Borrow Out Level, status of CYF and LSUY. Least significant unit of Y (LSUY) is true if the least significant bit of Y is ONE and CPU = 00, or if CPU ≠ 00 and the least significant four bits of Y is equal to nine (1001).

The four bit pseudo XYST Register checks and generates the X≠0, Y ≠ 0, INT or LSUX conditions. INT is an Interrupt and is true if one of the following interrupt is true:

Timer Interrupt
BUS I/O Interrupt
Console Interrupt
Memory Parity Error Interrupt

The LSUX (Least Significant Unit of X) bit is true if the least significant bit of X is ONE and CPU = 00, or if the least significant four bits of X equal nine (1001) and CPU ≠ 00.

FOUR BIT ARITHMETIC AND COMBINATORIAL SECTION (FOUR BIT FUNCTION BOX)

The Four Bit Arithmetic and Combinatorial Section otherwise referred to as the Four Bit Function Box is used to produce the normal arithmetic or logic functions between two 4-bit operands.

The Four Bit Function Box is also used to test various conditions of four bit registers and branch or skip on the results. The following is a description of the Four Bit Function Box.

Inputs

Inputs to the Four Bit Function Box are any of the four bit registers that are listed in Table I-2 with a second input being obtained from the micro instruction itself.

FOUR BIT FUNCTION BOX INPUTS

TA	TB	TC	TD	TE	TF
LA	LB	LC	LD	LE	LF
FU	FT	FLC	FLD	FLE	FLF
CA	CB	CC	CD		
BICN	XYCN	FLCN			

TABLE I-2

Logic Functions

In addition to the development of the various logical/arithmetic functions such as SET, AND, OR, EXCLUSIVE-OR, BINARY SUM MODULO SIXTEEN and BINARY DIFFERENCE MODULO SIXTEEN, the Four Bit Function Box through specific micros can test one bit or combinations of bits in various four bit registers. The micros which perform some of the above functions are as follows: 1C Register Move, 2C Scratchpad Move, 3C Four Bit Manipulate, 4C Bit Test Relative Branch False, 5C Bit Test Relative Branch True and 6C Skip When. For a description of these micros as to function refer to the appropriate pages in Section I of this manual.

REGISTERS

REGISTER SELECTION

The various registers of the B1700 system are addressed within the micro operator or from the front console by a series of coordinates.

The first coordinate is to select one of 16 groups of registers, the second coordinate then selects one of four registers from that group. Table I-3 illustrates the selecting of the register according to REGISTER GROUP and REGISTER SELECT. This chart must be used when generating or observing micro code in order to determine the designated register.

EXAMPLE: FB Register is register Group 9 and Register Select 2.

REGISTER GROUP	REGISTER SELECT 0	1	2	3
0	TA	FU	X	SUM
1	TB	FT	Y	CMPX
2	TC	FLC	T	CMPY
3	TD	FLD	L	XANY
4	TE	FLE	MAR(A)	XEOY
5	TF	FLF	M	MSKX
6	CA	BICN	BR	MSKY
7	CB	FLCN	LR	XORY
8	LA	RES .	FA	DIFF
9	LB	RES .	FB	MAXS
10	LC	RES .	FL	MAXM
11	LD	RES .	TAS	U
12	LE	XYCN	CP	RES .
13	LF	XYST	RES .	DATA
14	CC	RES .	READ	CMND
15	CD	CPU	WRIT	NULL

TABLE I-3
REGISTER TABLE

M REGISTER (MICRO REGISTER) AND INPUTS

The M register is a 16 bit register (discrete) which is used to hold the active micro-operator that was previously obtained from S-Memory, or from the Tape Cassette in Tape Mode. The contents of this register is decoded in various areas of the processor to enable the micro to perform its designated function. The M register is addressable both as a source, and as a sink. When it is used as a sink, the incoming data is bit ORed with the next incoming micro, thus modifying the new micro being placed in M for execution.

The M register has two sources from which it can receive micros:

A. S-Memory via Memory latches (ML)
B. U Register (to facilitate micro execution in Tape Mode)

MAR (A) REGISTER (MEMORY ADDRESS/ADDRESS REGISTER)

The MAR (A) Register is a 19 bit micro-program address register. The MAR (A) Register has two basic functions and in actuality is a shared register for addressing memory at two specific times. As a program address register it is referred to as the A Register, and addresses 16 bit micro operators in main memory by assuming them to be located at bit boundary addresses exactly divisable by 16. When used in this manner the lower order four bits are ignored and the micro is fetched and stored in the M Register. In the case of the micro fetch ("M" FETCH), the memory rotator is by-passed.

The MAR (A) Register is capable of having binary increments from 0 through 4095 (multiplied by 16) added to or subtracted from it with a high speed adder to facilitate program branching. The MAR (A) Register is automatically incremented by binary 16 during the run mode. Wrap-around of MAR (A) can occur and is permitted.

The MAR (A) Register also serves as a Memory Address Register (thus the name MAR) for the Read/Write Memory micro operator. In this case the full 19 bits of MAR (A) are used and the address is a bit address. The data read/written is passed through the rotator to insure the data is placed in the proper memory locations due to variable field length, variable field direction and the bit addressability of the memory. When used as a Memory Address Register, the address of the next micro (A Register function) is temporarily stored in a holding register, referred to as Temporary Buffer (TEMPB).

The MAR (A) Register is addressable as a source and as a sink. When addressed as a source, all bits are produced onto the Main Exchange. When used as a sink, the rightmost four bits of the source are moved to the rightmost four bits of the MAR (A) Register although they are not significant. Moves into the MAR (A) Register cause the instruction address to change and are therefore regarded as branches.

TAS REGISTER (TOP OF A STACK REGISTER)

The TAS Register is a 24 bit register which is the top of the A Stack. The top of the A Stack is addressed by a stack pointer that can be changed by moves into the A Stack or by moves from the A Stack. Because the pointer addresses different A Stack locations, the TOP of the A Stack is a relative position within the A Stack. Moves into TAS cause the A Stack Pointer to first be upcounted, and then, the source data is stored in the location addressed by the pointer. Moves from TAS cause the data in the A Stack location which is addressed by the Stack Pointer to be read and placed in the destination register. After the read occurs the Stack Pointer is decremented and a new A Stack location is addressed which becomes the new TAS.

A STACK

The A Stack is a 16 words deep, 24 bit wide memory. Generally the A Stack is used for normal Call/Return programming where subroutines may be obtained and upon completion of the subroutine, control is returned to the program. The Call/Return is obtained by CALLING a subroutine (branching) and storing the address where the program exited in the A Stack. Return from the subroutine is then done by moving the contents of the A Stack to MAR(A) which acts as a BRANCH back into the normal program.

The A Stack operates as a push down stack with a last in, first out structure. The A Stack is addressed by a Stack Pointer and wrap around of the pointer is provided. Sixteen consecutive writes (pushes) into the A Stack or sixteen consecutive reads (pop) from the A Stack will cause the pointer to address the same location as it did at the beginning of the write or read operations. Although the A Stack is not intended to be used as an operand stack (data storage), it has been purposely made 24 bits wide to allow for limited operand storage. (Scratchpad usually provides for data storage.)

The only micro which has a specific affect on the A Stack other than the Register Move type micros is the 145C Call. Refer to the 145C Call micro for the specific function of the A Stack with this micro.

MAXS REGISTER (MAXIMUM S-MEMORY REGISTER)

The MAXS Register is a 24 bit register which is set by the field engineer to indicate the maximum size of the installed memory. The MAXS Register is not a discreet register but is wired constant and thus addressable as a source register only.

BR AND LR REGISTER (BASE AND LIMIT REGISTER)

The Base and Limit Registers are both 24 bit registers which can be addressed as either a source or destination. These registers are used for protection of memory and base relative addressing. Memory Addressing within the Base and Limit registers is generally allowed. If the address does not fall within the Base and Limit then it is a software function to determine whether the cycle is to be allowed.

MAXM REGISTER (MAXIMUM M-MEMORY REGISTER)

M-Memory is not available as an option in the S-Memory Processor and by addressing this register as a source all zeros will be obtained. All zeros indicates that M-String is not present.

X REGISTER

The X Register is a 24 bit general purpose register and used primarily for the storage of an operand for the 24 Bit Function Box. The register may be addressed as either a source or destination. In addition to its input to the 24 Bit Function Box, it is one of four registers (X, Y, T and L) which may be used as a source or destination for data on a memory operation. The X Register is also capable of being shifted or rotated by the 4D, 5D or 3F micro operators.

On an add operation the X Register will contain the addend and on a subtract operation the X Register contains the minuend.

Y REGISTER

The Y Register is a 24 bit general purpose register and used primarily for storage of an operand for input to the 24 Bit Function Box. (See X Register) The Y Register may be addressed as either a source or destination. In addition to its input to the 24 Bit Fuction Box it is one of four registers (X, Y, T, and L) which may be used as a source or destination for data on a memory operation. The Y Register is also capable of being shifted or rotated by the 4D or 5D micros. On an add operation the Y Register will contain the augend and on a subtract, it contains the subtrahend.

L REGISTER (LOGICAL REGISTER)

The L Register is a 24 Bit general purpose register and is also addressable in four bit groups denoted as LA, LB, LC, LD, LE, and LF. The L Register may be used as a 24 bit source or destination or can be addressed in the above mentioned four bit groups as a source or destination. Since the L Register is addressable in four bit groups, its contents are available for analysis and alteration via the four Bit Function Box. The L Register is one of the four registers (X, Y, L, and T) which may be used as a source or destination for data on a memory operation.

T REGISTER (TRANSFORM REGISTER)

The T Register is a 24 bit general purpose register used as either a source or destination. The T Register is addressable in four bit groups denoted TA, TB, TC, TD, TE, and TF. Since the T Register is addressable in four bit groups, it is available for analysis and alteration via the Four Bit Function Box.

The T Register is one of the four registers (X, Y, L and T) which may be used as a source or destination for data on memory operations. The T Register is capable of Shift/Rotate operations (10C micro), and data may be extracted from the T Register (11C micro).

FA REGISTER (FIELD ADDRESS REGISTER)

The FA Register is a 24 bit register used to hold an absolute bit address for Main Memory. It has the capability of directly addressing any bit in the memory starting at any location. The FA Register is addressable as both a source and destination and can be loaded, stored or swapped with the contents of a word in the Scratchpad. FA is upcounted or downcounted by a literal value in the 7C Read/Write memory micro or by the value in CPL if that literal is equal to zero. A separate micro 6D Count FA/FL may be used to count FA up or down depending upon the variants of the micro.

On memory operations the FA Register is transferred to MAR(A) which will be used to address the memory location. In this case the upper five bits of FA are truncated but this is not significant as FA has the capability of addressing more memory than will be available in the machine.

FB REGISTER

The FB Register is a 24 bit register which can be functionally divided into three portions; a Four Bit FU (Field Unit) Register, a Four Bit FT (Field Type) Register, and a 16 Bit FL (Field Length) Register.

NOTE: Field Type is not specifically defined by the hardware and therefore has only specific meaning to the software.

The FB Register as well as each four bit portion of FB, denoted as FU, FT, FLC, FLD, FLE and FLF is addressable as a source and destination. In addition, the 16 bit portion denoted as FL is addressable as a source and destination.

The FU Register holds the length of the unit which makes up a field of data in memory such as binary and four bit BCD. FL holds the total length of the field with FL having the capability of describing fields up to 65,536 bits. FL may be adjusted up or down by a literal in the 7C Read/Write Memory micro, by the value in CPL or specifically by a 6D Count FA/FL micro.

FB has the ability of being loaded, stored or swapped along with FA into a Scratchpad memory word. FU and FL along with corresponding portions of the first cell or Right Scratchpad are used to set the various conditions of FLCN (Field Length Conditions) and the various conditions of the CP Register (See Bias micro 3E.)

SCRATCHPAD MEMORY

Scratchpad Memory consists of sixteen 48 bit words (16 x 48), or could be regarded as consisting of thirty-two 24 bit words (32 x 24). Scratchpad from a hardware standpoint is regarded as general purpose storage but its typical use is for storage of S-Language (See software concept) stack pointers or processor registers which are under constant manipulation.

The first cell of right scratchpad is referred to as SFL and SFU, which correspond to FL and FU in the FB portion of the F Register. SFL is used for comparison to FL for the FLCN (Field Length Conditions) and SFU is used if selected by the appropriate variants in conjunction with the 3E Bias micro.

C REGISTER (CONTROL REGISTER)

The C Register is a 24 bit register which is NOT addressable as such. The C Register may be addressed by four bit groups referred to as CA, CB, CC and CD. The least significant eight bits may be addressed as CP. CP may further be divided into three sections: CPL equal to five bits, CPU equal to two bits and CYF being one bit. Figure I-5 illustrates the addressing portions of the C Register.

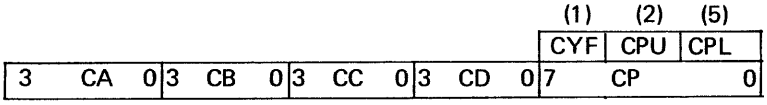


Fig. I-5 C REGISTER

The CA and CB portions of the C Register do not have any specific hardware use and are, therefore, described as general purpose four bit storage registers.

The CC portion is used for storage of various processor interrupt conditions or the processor state. The bits of CC are defined as follows:

CC(0) Console Interrupt derived from the console interrupt button.

CC(1) Bus Interrupt derived from the various I/O Controls attached to the B1700 I/O Bus. This bit is set as a result of a service request by one or more of the controls which may be attached to the I/O Bus.

CC(2) Timer Interrupt is developed from the primary power frequency. The Interrupt occurs every 100 milliseconds to set CC(2).

NOTE: Adjustable by the Field Engineer for either 50 Hz or 60 Hz.

CC(3) Console State Lamp. The setting of CC(3) by software causes the Console State Lamp to illuminate. Use of the State Lamp is defined by software.

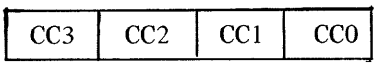


Figure I-6
CC REGISTER

The CD portion of the C Register is also used for storage of interrupt conditions. CD(3) will be set if a parity error occurred on a memory read operation that was initiated by the processor. CD(2) thru CD(0) is reserved.

The CPL portion (Control Parallelism Length) is used to define the data length of the 24 Bit Function Box or used to define length at various times, such as if the literal in the 7C Read/Write Memory micro is equal to zero, then the value in CPL is used. CPL is a five bit register and defines lengths of one to twenty-four bits.

CPU is the Control Parallelism Unit of the CP portion of the C Register. The CPU Register is two bits and defines the unit of data as either binary or Four Bit BCD.

CPU=00 Binary Data
CPU=01 Four Bit BCD Data
CPU=10 Reserved
CPU=11 Reserved

CYF is the Carry Flip-Flop and used to store overflows from the 24 Bit Function Box as a result of an add or subtract operation but must be set by sampling the appropriate level from the function box. (See 6E micro, Carry Flip-Flop Manipulate.)

All four bit portions of the C Register are addressable as both a source and destination. Their contents are available for analysis and alteration via the Four Bit Function Box.

U REGISTER

The U Register is a 16 bit register used primarily to accumulate the bit serial input from the console cassette tape loader. The U Register is addressable only as a 16 bit source and NOT a destination. Only the micro 1C Register move can access the U Register. If the data is not yet available in the register, the micro 1C finish is delayed until the U Register is full.

In the Tape Mode the contents of the U Register are directly transferred to the M Register in order to cause the execution of micros from the tape. If the micro Read is a 9C move 24 bit literal then Execution is delayed until the remaining 16 bits of the literal have been accumulated in the U Register.

FLCN REGISTER (FIELD LENGTH CONDITIONS)

The FLCN Register is a four bit pseudo register which indicates comparison conditions. FLCN is a static comparison between the FL portion of the FB Register and the corresponding portion of the first word of right scratchpad referred to as SFL. FLCN carries the conditions listed in Table I-4.

BIT	CONDITION
0	FL $\neq$ 0
1	FL $<$ SFL
2	FL $>$ SFL
3	FL = SFL

TABLE I-4
FIELD LENGTH CONDITIONS

CMND REGISTER (COMMAND REGISTER)

The CMND Register is a 24 bit pseudo register which can act only as a destination. A Register Move type of operation with CMND as the destination will cause a command to be transferred on the I/O BUS and the Command Active signal (CA) is generated. This operation is used to transfer a Command to an I/O Control on the I/O Bus.

DATA REGISTER

The Data Register like the Command Register is a 24 bit pseudo register but it can act as both a source and destination. The Data Register is used to transfer data to and from the I/O Controls attached to the I/O Bus. When used as a source, the processor generates the Response Complete (RC) signal and accepts the 24 bits of data from the I/O Bus. When used as a destination, the processor generates the RC signal to the I/O interface and places the data from a source register on the I/O bus.

NULL REGISTER

NULL is a pseudo register with a length of 24 bits. NULL is used primarily on a load or display of a designated register from the Front Panel (Console). In the Halt Mode the hardware will generate moves from NULL in order to cause the contents of the console switches to be loaded in the designated destination register. This is accomplished by depressing the LOAD button on the Console. If the Load Button is not depressed the hardware in the Halt Mode generates a Register

move to NULL which will cause the designated register to be displayed on the console lamps.

In the Run Mode or Tape Mode, the NULL Register may be moved to a register for the purpose of clearing that register. (NULL is equal to all zeros.)

MEMORY REGISTER AND ASSOCIATED LOGIC

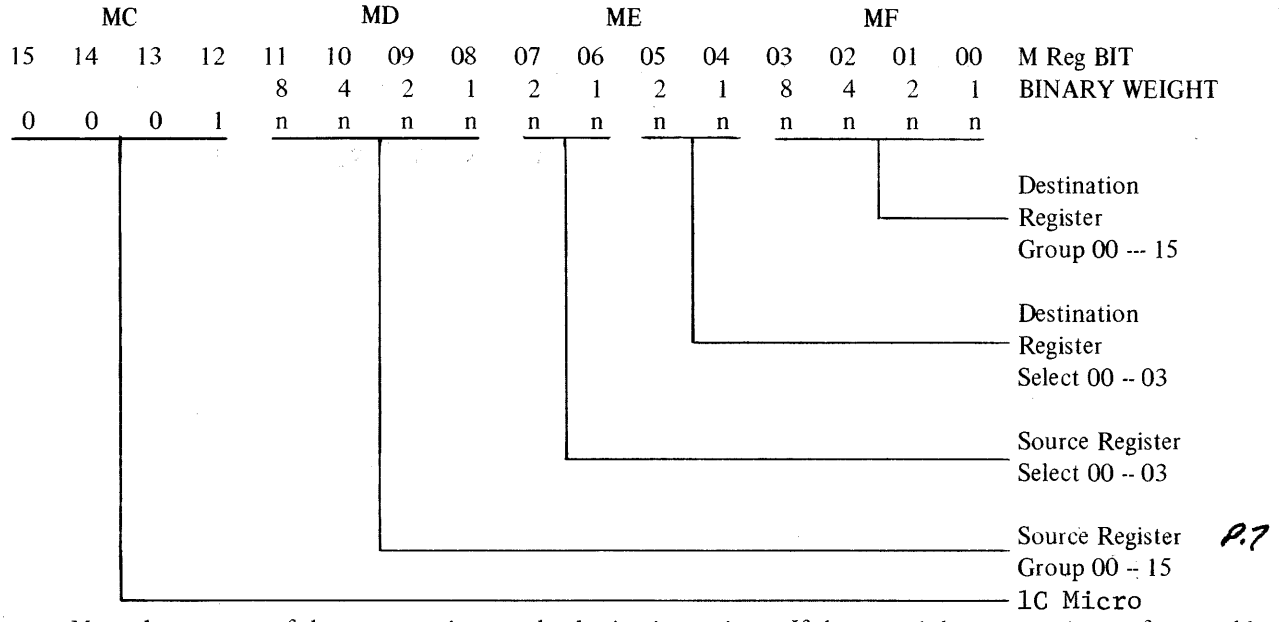
The registers associated directly with memory such as MIR (Memory Information Register) and MLR (Memory Latch Register) along with associated memory logic such as the rotator are generally described in the S-Memory portion of Section I of this manual (refer to index).

MICRO OPERATORS

INTRODUCTION

The B1700 Micro Processor has the capability of producing approximately 60 different micro instructions. It was necessary to develop only 24 of the possible 60 combinations and Table I-5 lists those 24 micros which have been implemented. The micros are referred to by name and by binary weight within the specific portion of the M Register. The 1C Register Move for example has a binary weight of 1 in the MC Register. The other bits of the 1C Register Move are used for selection of source and sink registers according to Table I-3. The variants for various micros are listed in Table I-5 but for a more detailed explanation of the micro and variants refer to the individual micro operator descriptions.

1C REGISTER MOVE



Move the contents of the source register to the destination register. If the move is between registers of unequal lengths, the data is right justified with left (most significant) zero bits supplied or with data truncated from the left whichever is appropriate.

The contents of the source register are unchanged unless it is also the destination register.

The basic execute time is two clocks to which is added one additional clock if the source is BCD, and two additional clocks if the destination is the MAR (A) register. If the U-Register is the source, the time takes many clocks.

Exceptions:

1. CPU and CMND are excluded as source registers.
2. When M is used as a destination register, the operation is changed to a bit OR which modifies the next micro-operation. It does not modify the instruction as stored in the memory.
3. BICN, FLCN, XYCN and XYST are excluded as destination registers.
4. All registers and pseudo registers in column select=3 are excluded as destination registers except CMND and DATA.
5. When DATA is designated as a source, CMND and DATA are prohibited as destinations.
6. U is excluded as a source register in STEP and TAPE mode. It is permitted as source in RUN mode. However, when U is used as a source the TAS, A and M registers are excluded as destination registers.

	MICRO NAME	MC 15	14	13	12	MD 11	10	9	8	ME 7	6	5	4	MF 3	2	1	0
1C	REGISTER MOVE	0	0	0	1	REG 1 GROUP SOURCE REGISTER				REG 1 SELECT		REG 2 SELECT		REG 2 GROUP SINK REGISTER			
2C	SCRATCHPAD MOVE	0	0	1	0	REGISTER GROUP SOURCE OR SINK				REG SELECT		MOV DIR	DPW 1/2	DOUBLE PAD WORD ADDRESS			
3C	4 BIT MANIPULATE	0	0	1	1	REGISTER GROUP, 4 BIT SOR & SNK				REG SEL	MANIPULATE VARIANTS			4 BIT MANIP LITERAL			
4C	BIT TEST REL BRANCH FALSE	0	1	0	0	REGISTER GROUP, 4 BIT SOURCE				REG SEL	TESTBIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG.			
5C	BIT TEST REL BRANCH TRUE	0	1	0	1	REGISTER GROUP 4 BIT SOURCE				REG SEL	TESTBIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG.			
6C	SKIP WHEN	0	1	1	0	REGISTER GROUP 4 BIT SOR & SNK				REG SEL	SKIP TEST VARIANTS			4 BIT TEST MASK			
7C	READ/WRITE MEMORY	0	1	1	1	R/W VAR	COUNT FA/FL VARIANTS			DATAREG CODE			TW SGN	DATA TRANSFER WIDTH MAGNITUDE			
8C	MOVE 8 BIT LITERAL	1	0	0	0	REGISTER GROUP; REG SEL IS 2.				ENTIRE 8 BITS OF 8 BIT LITERAL							
9C	MOVE 24 BIT LITERAL	1	0	0	1	REGISTER GROUP; REL SEL IS 2.				8 MOST SIGNIFICANT BITS OF FULL 24 BIT LITERAL							
10C	SHIFT/ROTATE T REG	1	0	1	0	SINK REGISTER GROUP				SNK REG SELECT		S/R VAR		LEFT SHIFT/ROTATE COUNT			
11C	EXTRACT FROM T REG	1	0	1	1	RIGHT BIT POINTER FOR EXTRACTION FLD				SNK REG CODE				EXTRACTION FIELD WIDTH			
123C	BRANCH RELATIVE	1	1	0	DSP SGN	RELATIVE DISPLACEMENT MAGNITUDE											
145C	CALL RELATIVE	1	1	1	DSP SGN	RELATIVE CALLED ADDRESS MAGNITUDE											
4D	SHIFT/ROTATE X OR Y	0	0	0	0	0	1	0	0	S/R DIR VARIANT		X/Y VAR		LEFT OR RIGHT, XOR Y SHIFT/ROTATE COUNT			
5D	SHIFT/ROTATE X AND Y	0	0	0	0	0	1	0	1	S/R DIR VARIANT				LEFT OR RIGHT X AND Y SHIFT/ROTATE COUNT			
6D	COUNT FA/FL	0	0	0	0	0	1	1	0	COUNT FA/FL VARIANTS				COUNT SCALAR MAGNITUDE			
7D	EXCHANGE DPW	0	0	0	0	0	1	1	1	SINK DPW ADDRESS				SOURCE DPW ADDRESS			
8D	SCRATCHPAD RELATE FA	0	0	0	0	1	0	0	0				DSP SGN	LEFT HALF PAD WORD ADDRESS			
9D	MONITOR	0	0	0	0	1	0	0	1	LITERAL OCCURRENCE IDENTIFIER							
2E	CASSETTE CONTROL	0	0	0	0	0	0	0	0	0	0	1	0	CASSETTE MANIP VARIANTS			
3E	BIAS	0	0	0	0	0	0	0	0	0	0	1	1	BIAS VARIANTS			TST FLG
6E	CARRY FF MANIPULATE	0	0	0	0	0	0	0	0	0	1	1	0	CYF ⇒ CYD	CYF ⇐ CYL	CYF ← 1	CYF → 0
1F	HALT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
3F	NORMALIZE X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
ZERO	NO OPERATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REVISIONS

VARIANTS	0 000	1 001	010	011	100	101	110	111
MOV DIR: 1/2 DPW:	P←R LEFT	R←P RIGHT						
MANIP VARIANTS:	SET	AND	OR	EOR	INC	INC TEST	DEC	DEC TEST
DSP SIGN:	+	−						
DSP SIGN:	+	−						
SKIP TEST VARIANTS:	ANY CLR/	ALL CLR/	EQL CLR/	ALL CLR	ANY/ CLR/	ALL / CLR /	EQL / CLR /	ALL / CLR
R/W VAR	READ	WRT						
CNT VAR	NØP	FA↑		FA↑	FA↓	FA↑		FA↓
REG SEL:	X	Y	FL↑	FL↓	FL↑		FL↓	FL↓
TW SIGN:	+	−	T	L				
S/R VAR:	SHFT	ROT						
SINK REG CODE:	X	Y	T	L				
DSP SIGN:	+	−						
DSP SIGN:	+	−						
X/Y VAR:	X	Y						
S/R, DIR:	SFT←	SFT→	ROT←	ROT→				
S/R, DIR VARIANTS:	SFT← 1BIT	SFT→ 1BIT	RES.	RES.				
COUNT FA/ FL VAR:	NØP	FA↑	FL↓	FA↑ FL↓	FA↓ FL↑	FA↑	FL↓	FA↓ FL↑
DSP SIGN:	+	−						
CASSETTE MANIP:	START TAPE	STOP@ GAP	STOP ON X≠Y	UNDEF	UNDEF	UNDEF	UNDEF	UNDEF
TEST FLG: BIAS VAR:	TST/ UNIT	TEST F	S	FS	NØP	FCP	NØP	UNDEF

REGISTER SELECT

REGISTER GROUP	0	1	2	3
0	TA	FU	X	SUM
1	TB	FT	Y	CMPX
2	TC	FLC	T	CMPY
3	TD	FLD	L	XANY
4	TE	FLE	MAR(A)	XEQY
5	TF	FLF	M	MSKX
6	CA	BICN	BR	MSKY
7	CB	FLCN	LR	XORY
8	LA	RES	FA	DIFF
9	LB	....	FB	MAXS
10	LC	....	FL	MAXM
11	LD	....	TAS	SJ
12	LE	XYCN	CP	RES
13	LF	XYST	RES	DATA
14	CC	RES	READ	CMND
15	CD	CPU	WRIT	NULL

INDIVIDUAL BITS OF SOME 4-BIT REGISTERS HAVE SPECIAL MEANINGS AS NOTED BELOW:

NOTE:
BITS ARE NUMBERED HERE ACCORDING TO THE HARDWARE CONVENTION:

LA	LB	LC	LD	LE	LF
3 0,3	0,3	0,3	0,3	0,3	0
MSB 2,3		L			LSB 0,0

BIT #	BICN	XYCN	XYST	FLCN
0	CYL	X>Y	X≠0	FL≠0
1	CYD	X<Y	Y≠0	FL<SFL
2	CYF	X=Y	INT OR	FL>SFL
3	LSUY	MSBX	LSUX	FL=SFL

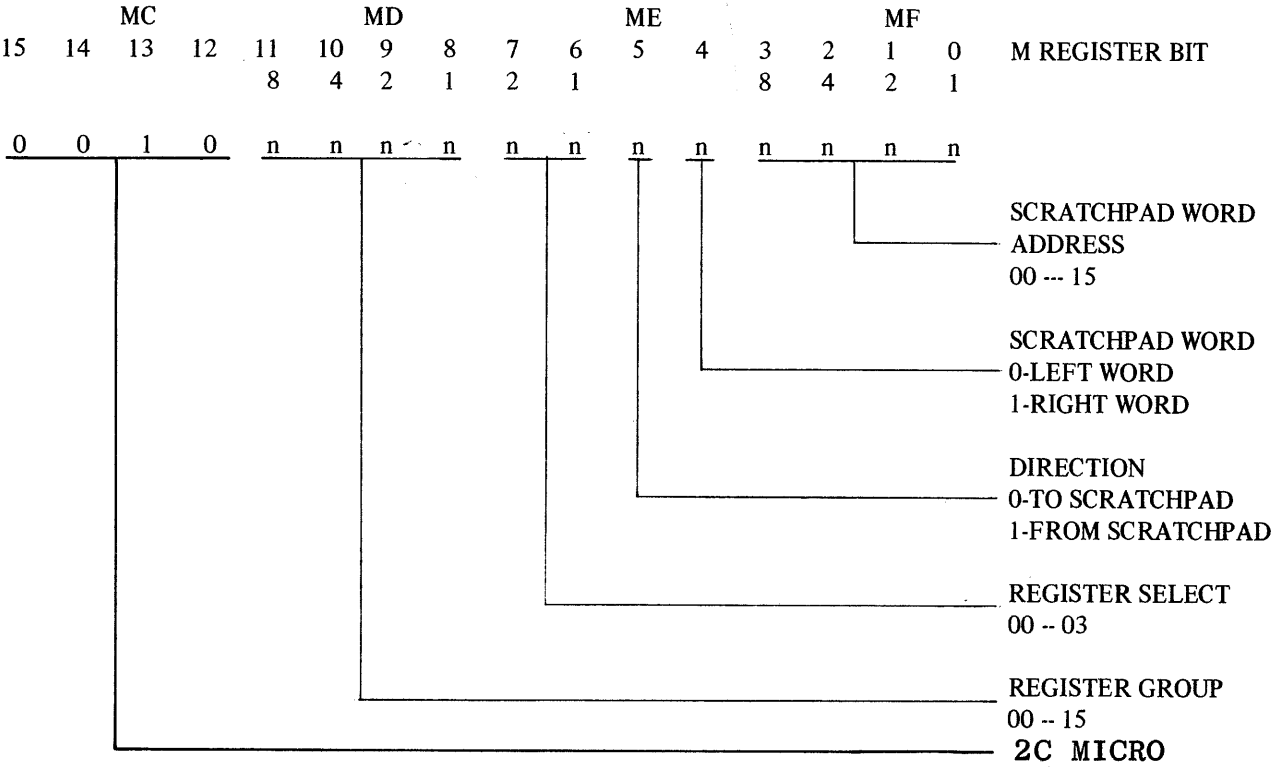
INT OR = ANY 1 OR MORE OF: CC0 CC1 CC2 CD3

CC & CD
- CC0 CONSOLE SOFT HALT INTERRUPT
- CC1 I/O BUS SERVICE REQUEST INTERPT.
- CC2 REAL TIME CLOCK (100 MS) INTERPT
- CC3 STATE PARITY ERROR (DISPLAYED ON CONSOLE)
- CD0 RESERVED
- CD1 RESERVED
- CD2 RESERVED
- CD3 MEMORY READ DATA PARITY ERROR INTERRUPT

TABLE I-5

7. When CMND or DATA is designated as a destination, SUM and DIFF are prohibited as sources.
8. When A, M, CP or DATA are designated as a source, all 4-bit registers are prohibited as destinations

2C SCRATCHPAD MOVE



Move the contents of the register (scratchpad) to the scratchpad (register). If the move is between registers of unequal lengths, the data is right justified with left (most significant) zero bits supplied or with data truncated from the left whichever is appropriate.

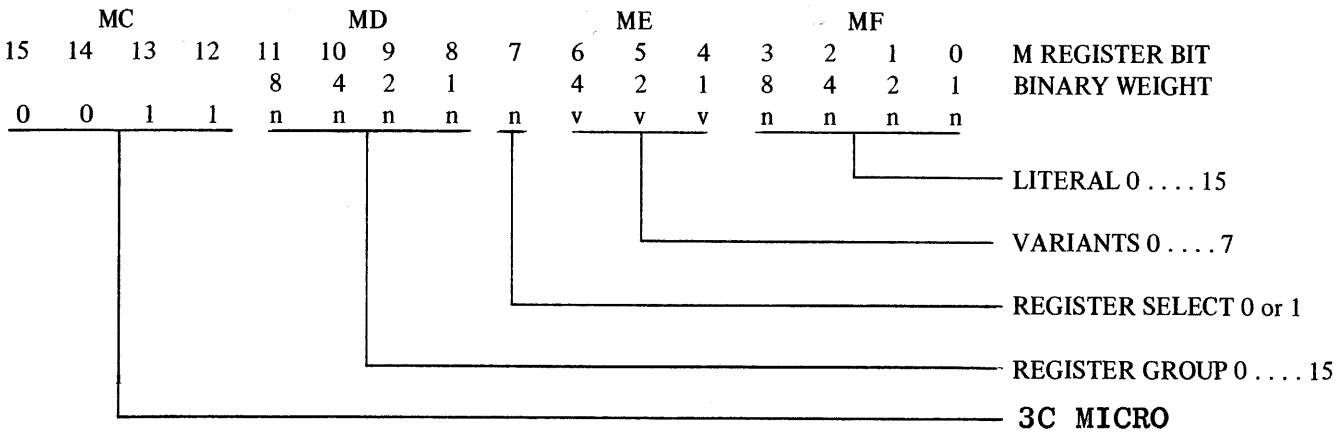
The contents of the source register are unchanged.

The basic execute time is two clocks to which is added one additional clock if the source is BCD and two additional clocks if the destination is the MAR(A) register.

Exceptions:

1. U, CPU and CMND are excluded as source registers.
2. When M is used as a destination register, the operation is changed to a bit OR which modifies the next micro-operation. It does not modify the instruction as stored in the memory.
3. BICN, FLCN, XYCN, and XYST are excluded as destination registers.
4. All register and pseudo registers in column select=3 are excluded as destination registers except CMND and DATA.
5. M as a source would result in a transfer of 24 zeroes.

3C 4 BIT MANIPULATE



Perform the Manipulate operation as specified by the variants on the addressed 4 Bit Register.

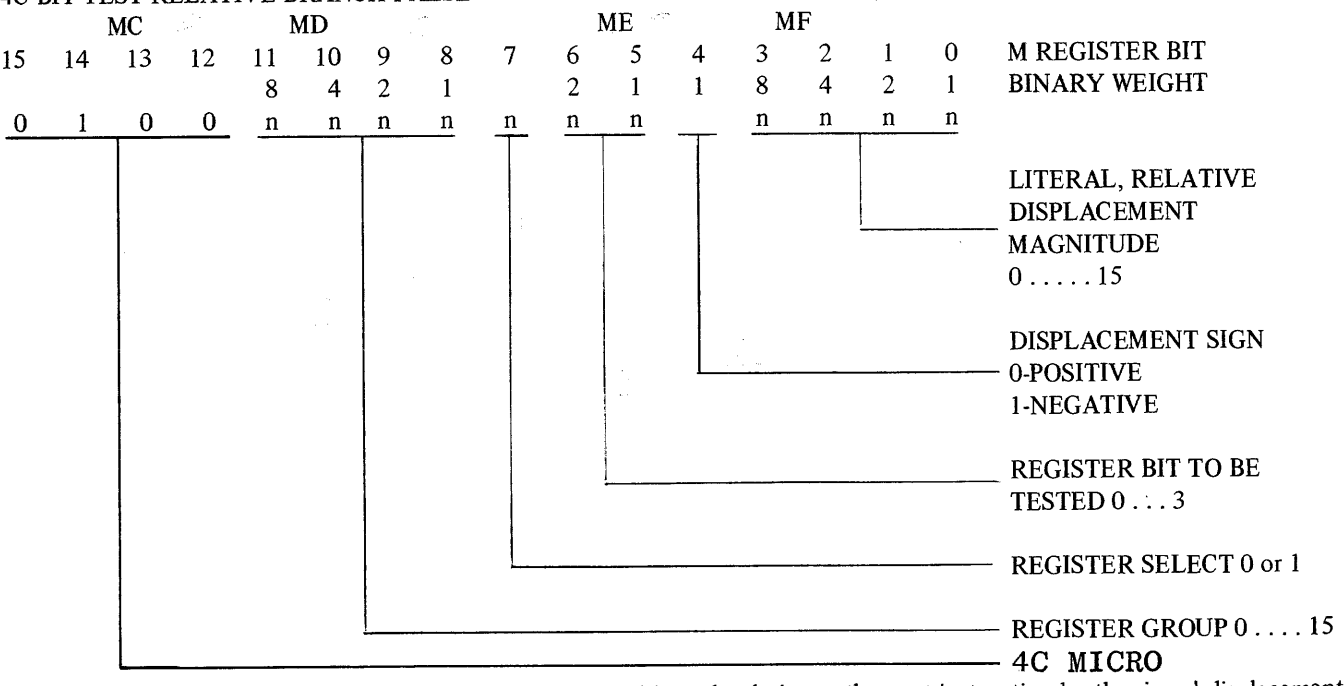
VARIANT	=	NAME	ACTION
000=0		SET	REG:=LIT
001=1		AND	REG:=REG*LIT
010=2		OR	REG:=REG+LIT
011=3		EOR	REG:=REG+LIT
100=4		INC	REG:=REG plus LIT (Disregard Overflow)
101=5		INC T	REG:=REG plus LIT (SKIP ON OVERFLOW) T=TEST
110=6		DEC	REG:=REG-LIT (Disregard Underflow)
111=7		DEC T	REG:=REG-LIT (SKIP ON UNDERFLOW) T=TEST

V=0 Set the Register to the value of the literal
1 Set the Register to the Logical and of the Register and Literal.
2 Set the Register to the Logical OR of the Register and Literal.
3 Set the Register to the Logical EXCLUSIVE OR of the Register and Literal.
4 Set the Register to the Binary SUM MODULO 16 of the Register and Literal
6 Set the Register to the Binary DIFFERENCE MODULO 16 of the Register and Literal.
5 Set the Register to the BINARY SUM MODULO 16 of the Register and Literal and Skip the next M-Instruction if a carry is produced.
7 Set the Register to the BINARY DIFFERENCE MODULO 16 of the Register and Literal and Skip the next M-Instruction if a borrow is produced.

The basic execute time is two clocks to which is added two additional clocks if the branch is taken.

Exceptions:
1. BICN, FLCN, XYCN, XYST, and CPU are excluded as source/destination registers.

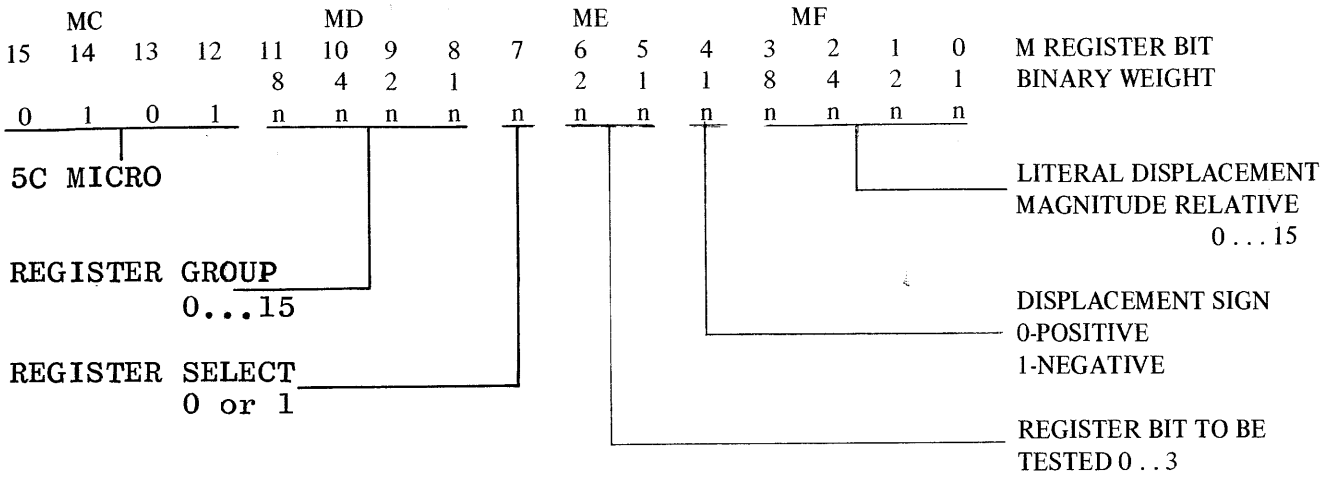
4C BIT TEST RELATIVE BRANCH FALSE



Test the designated bit within the specified register and branch relative to the next instruction by the signed displacement value if the bit is zero. If the bit is one, a displacement value of zero is assumed and control passes to the next in-line M-instruction. A displacement value indicates the number of 16 bit words from the next in-line instruction.

The basic execute time is two clocks to which is added one additional clock if the source is BCD (BICN with CPU=01) and two additional clocks if the branch is taken.

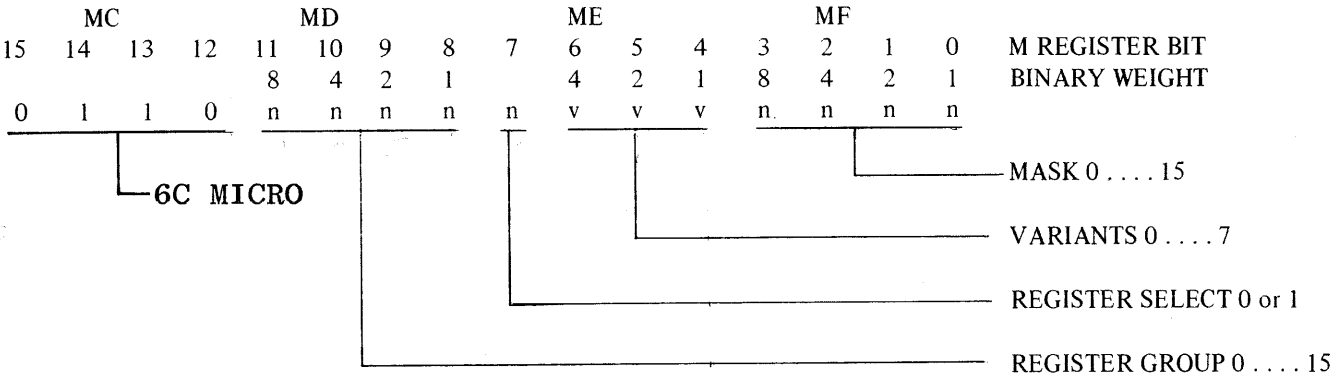
5C BIT TEST RELATIVE BRANCH TRUE



Test the designated bit within the specified register and branch relative to the next instruction by the signed displacement value if the bit is one. If the bit is zero, a displacement value of zero is assumed and control passes to the next in-line M-instruction. A displacement value indicates the number of 16 bit words from the next in-line instruction.

The basic execute time is two clocks to which is added one additional clock if the source is BCD (BICN with CPU=01) and two additional clocks if the branch is taken.

6C SKIP WHEN



Test only the bits in the register that are referenced by the "1" bits in the mask ignoring all others and then perform the action as specified below.

Exception: If V=2 or V=6, compare all bits for an equal condition.

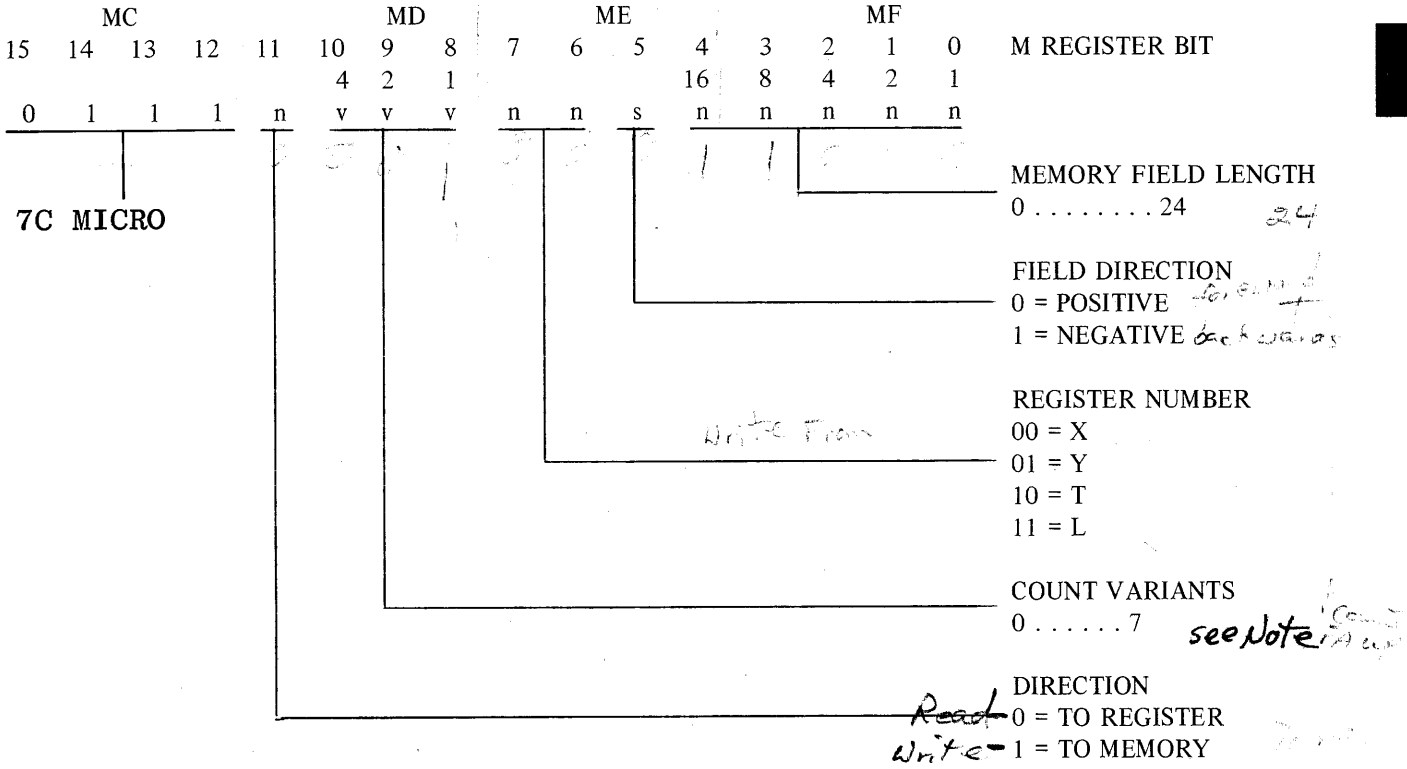
V=0 If any of the referenced bits is a "1", skip the next M-instruction.
V=1 If all of the referenced bits are "1", skip the next M-instruction.
V=2 If the register is equal to the mask, skip the next M-instruction.
V=3 Same as V=1, but also clear the referenced bits to zero without affecting the non-referenced bits.
V=4 If any of the referenced bits is a "1", do not skip the next M-instruction.
V=5 If all of the referenced bits are "1", do not skip the next M-instruction.
V=6 If the register is equal to the mask, do not skip the next instruction.
V=7 Same as V=4 but also clear the referenced bits to zero without affecting the non-referenced bits.

The basic execute time is two clocks to which is added one additional clock if the source is BCD (BICN with CPU=01) and two additional clocks if the branch is taken.

NOTE: If the mask equals 0000 the ANY result is false. The skip is not made for V=0 and is made for V=4. If the mask equals 0000, the ALL result is true. The skip is made for V=1 and V=3 and is not made for V=5 and V=7.

Ex Exceptions: BICN, FLCN, XYCN, and XYST are excluded as operand registers when V=3 or when V=7.

7C READ/WRITE MEMORY



Move the register's (memory's) contents to the memory (register). If the value of the memory field length is less than 24, the data from memory is right justified with left (most significant) zero bits supplied, while the data from the register is truncated from the left.

The contents of the source is unchanged.

Register FA contains the bit address of the memory field while the memory field direction sign and memory field length is given in the instruction.

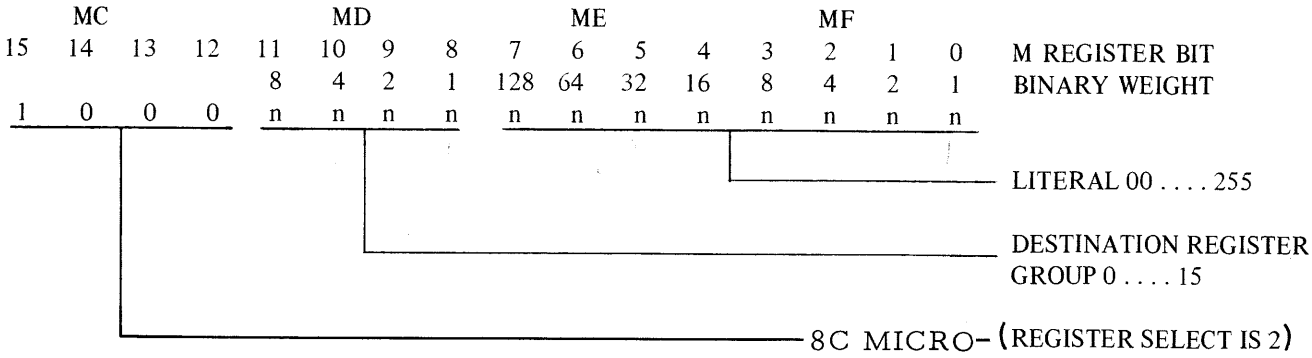
If the value of the memory field length as given in the instruction is zero, the value in CPL is used.

Count variants are as follows:

V = 000 No Count
001 Count FA Up
010 Count FL Up
011 Count FA Up and FL Down
100 Count FA Down and FL Up
101 Count FA Down
110 Count FL Down
111 Count FA Down and FL Down

Time equals eight clocks.

8C MOVE 8 BIT LITERAL

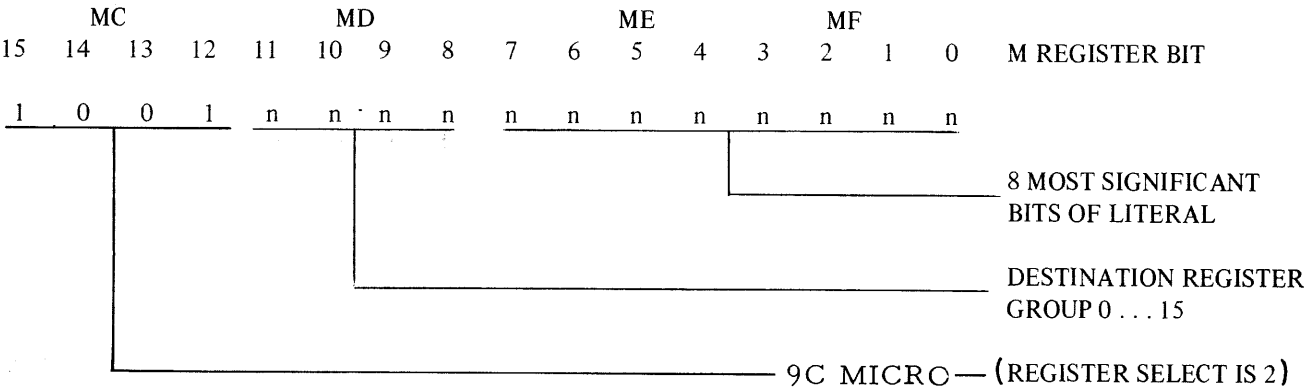


Move the 8 bit register literal even in the instruction to the destination register. If the move is to a register that is greater than 8 bits in length, the data is right justified with left (most significant) zero bits supplied.

Only registers X, Y, T, L, MAR (A), BR, LR, FA, FB, FL, TAS and CP can be specified. The register select is assumed to be 2.

The basic execute time is two clocks to which is added two additional clocks if the destination is the MAR(A) register.

9C MOVE 24 BIT LITERAL

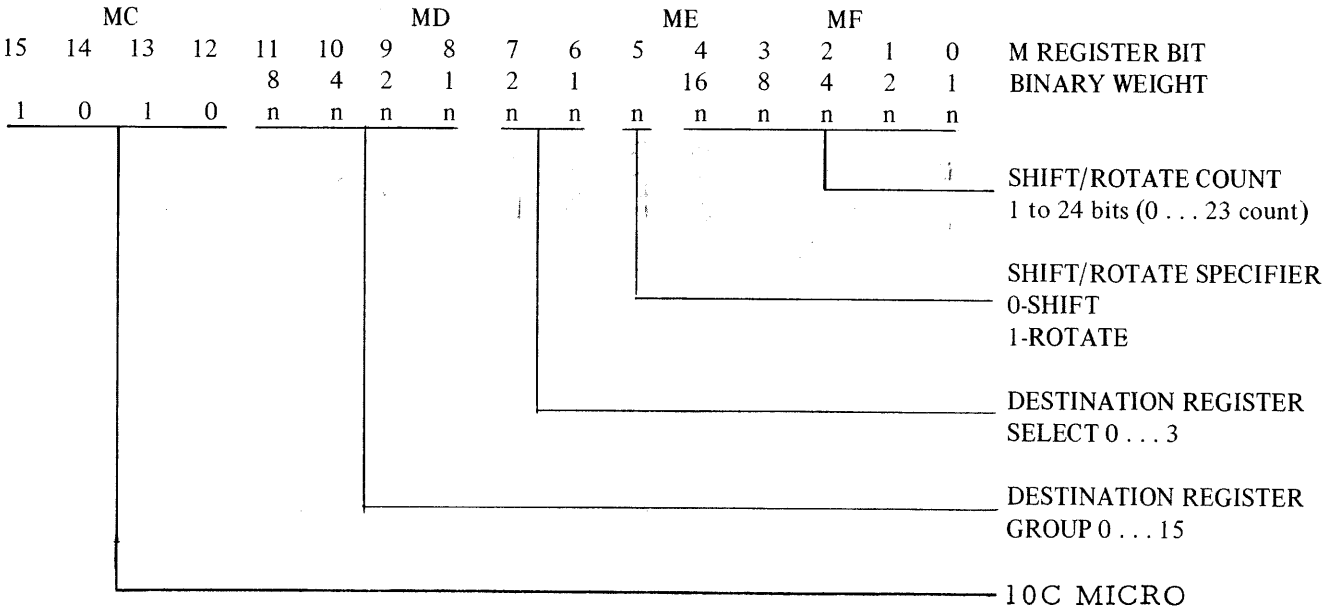


Move the 24-bit literal given in the instruction to the destination register. If the move is between registers of unequal lengths, the literal is truncated from the left.

Only registers X, Y, T, L, MAR (A), BR, LR, FA, FB, FL and TAS can be specified. The register select number is assumed to be 2.

Time equals six clocks.

10C SHIFT/ROTATE T REGISTER LEFT



Shift (Rotate) register T left by the number of bits specified and then move the 24 bit result to the destination register. If the move is between registers of unequal lengths, the data is right justified with data truncated from the left.

The contents of the source register is unchanged unless it is also the destination register.

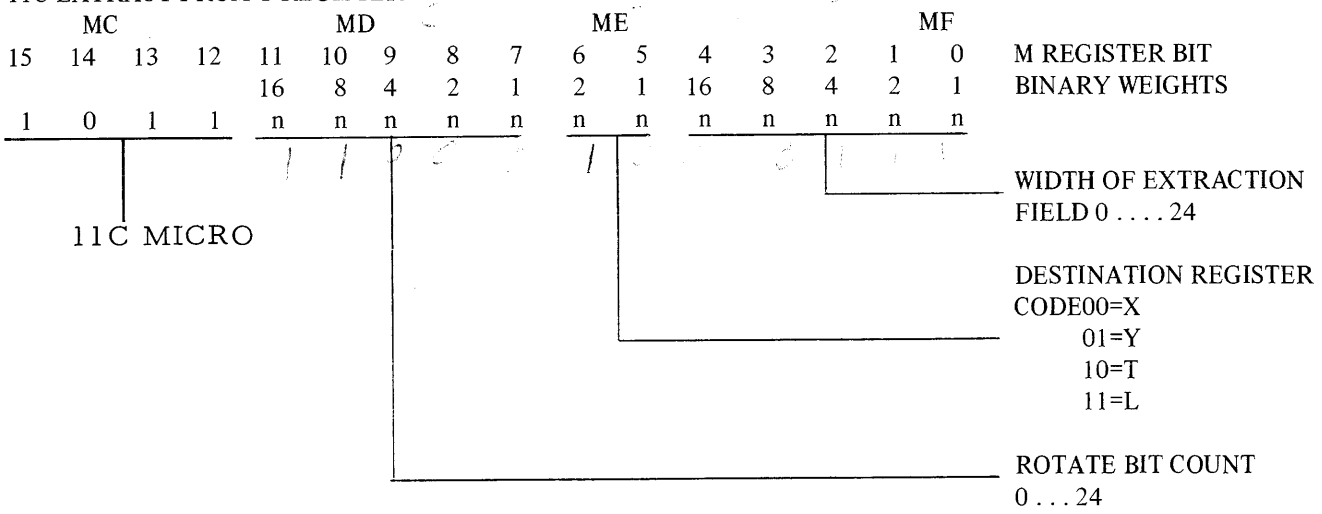
Zero fill on the right and truncation on the left occurs for the shift operation.

If the value of the shift/rotate count as given in the instruction is zero, the value given in CPL is used.

The basic execute time is three clocks to which is added two additional clocks if the destination is MAR(A).

Exceptions:
1. When M is used as a destination register, the operation is changed to a bit OR which modifies the next micro-operation. It does not modify the instruction as stored in the memory.
2. BICN, FLCN, XYCN, and XYST are excluded as destination registers.

11C EXTRACT FROM T REGISTER



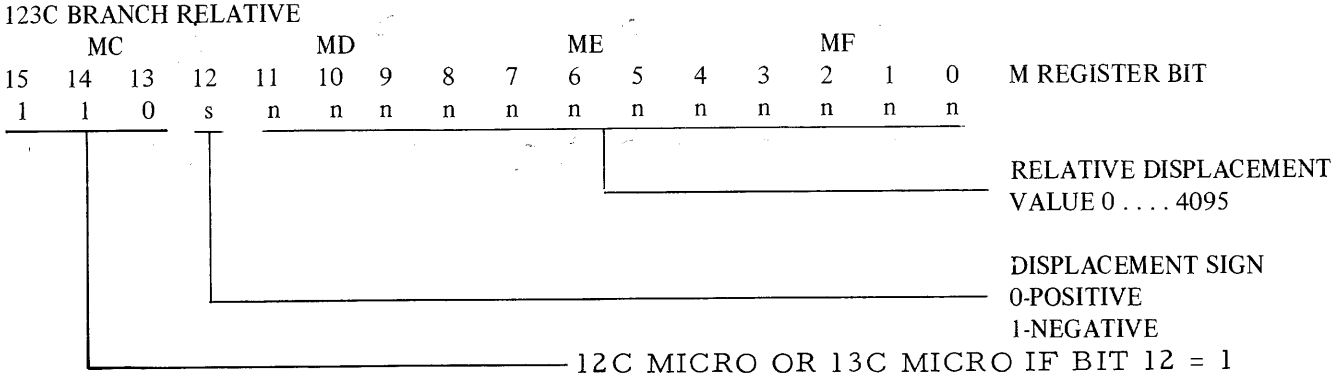
Rotate register T left by the number of bits specified and then extract the number of bits specified. Move the result to the destination register. If the extract bit count is less than 24, the data is right justified with left (most significant) zero bits supplied.

The contents of the source register is unchanged unless it is also the destination register.

A rotate value of 24 is equivalent to 0.

Time equals three clocks.

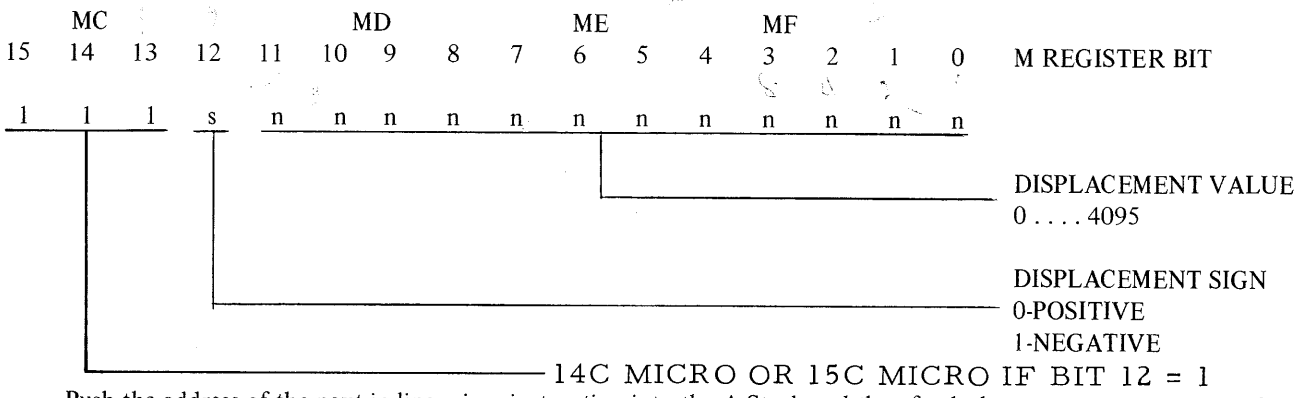
123C BRANCH RELATIVE



Fetch the next micro-instruction from the location obtained by adding the signal displacement value given in the instruction to the word address of the next in-line micro-instruction. A displacement value indicates the numbers of 16-bit words.

Time equals four clocks.

145C CALL

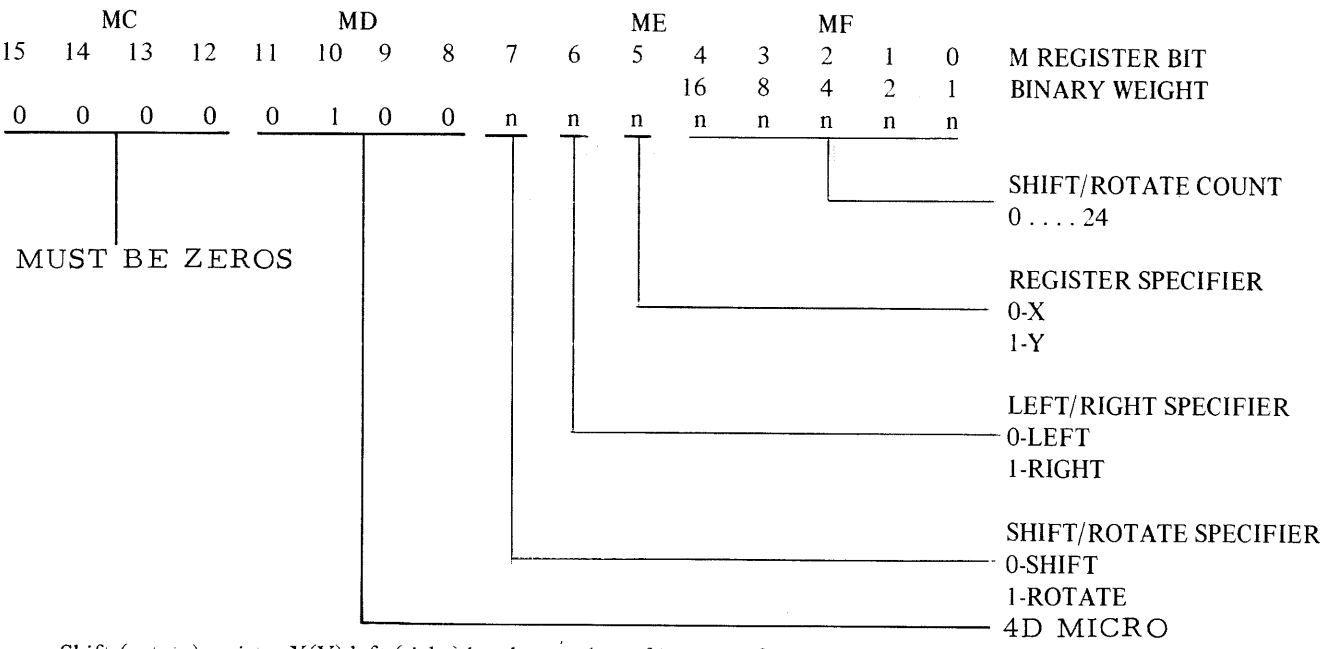


Push the address of the next in-line micro-instruction into the A Stack and then fetch the next micro-instruction from the location obtained by adding the signed displacement value given in the instruction to the word address of the next in-line micro-instruction. The displacement value indicates the number of 16 bit words.

NOTE: Exit is accomplished by employing the Move Register Instruction with the TAS as the source register and MAR(A) as the destination register.

Time equals five clocks. This time includes the time to fetch the next micro-instruction.

4D SHIFT/ROTATE X OR Y



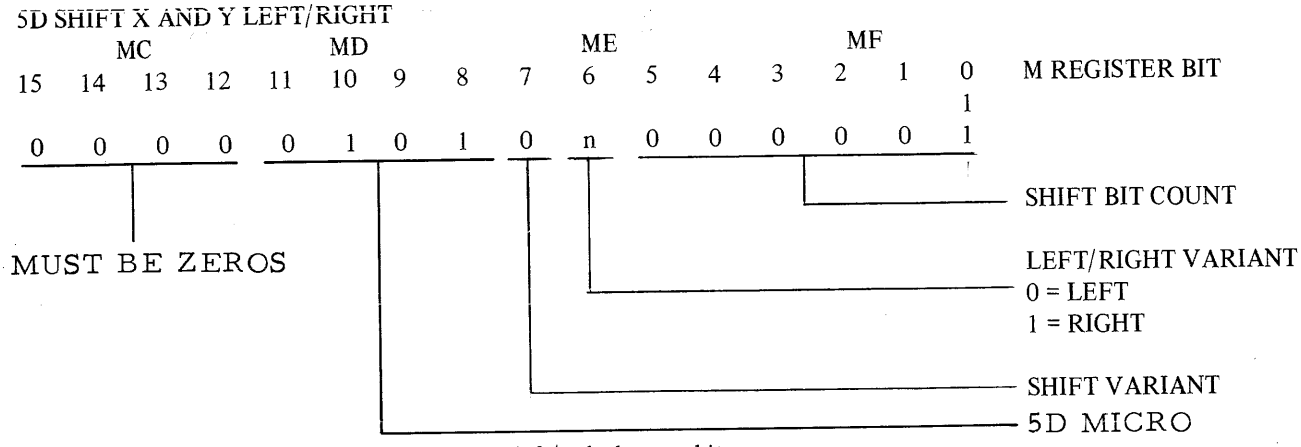
Shift (rotate) register X(Y) left (right) by the number of bits specified.

Zero fill on the right and truncation on the left occurs for the left shift. Zero fill on the left and truncation on the right occurs for the right shift.

If the value of the shift/rotate count as given in the instruction is zero, the amount the operand is shifted (rotated) is zero.

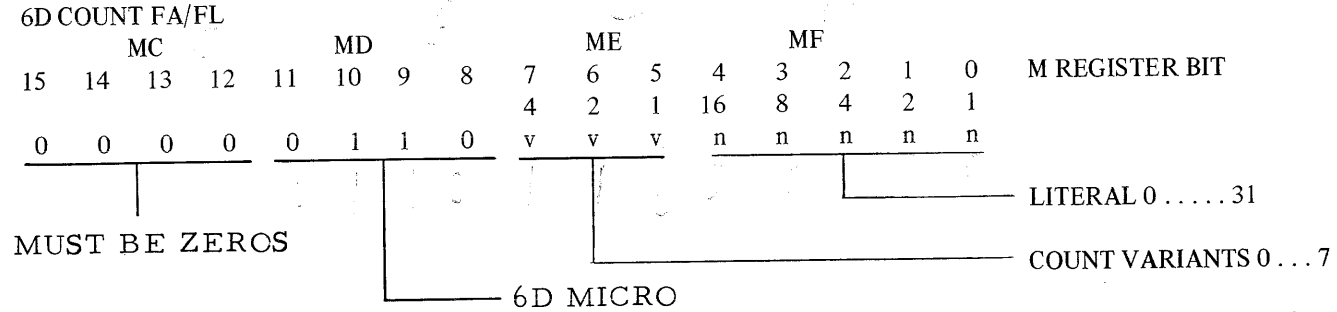
Time is three clocks. It is the same for all counts.

5D SHIFT X AND Y LEFT/RIGHT



Shift the concatenated X and Y registers left/right by one bit.
The X register is the leftmost (most significant) half of the concatenated 48 bit XY register.
Zero fill on the right and truncation on the left occurs for the left shift.
Zero fill on the left and truncation on the right occurs for the right shift.
If the value of the shift count as given in the instruction is not one, an undefined result will occur.
Time equals six clocks.

6D COUNT FA/FL



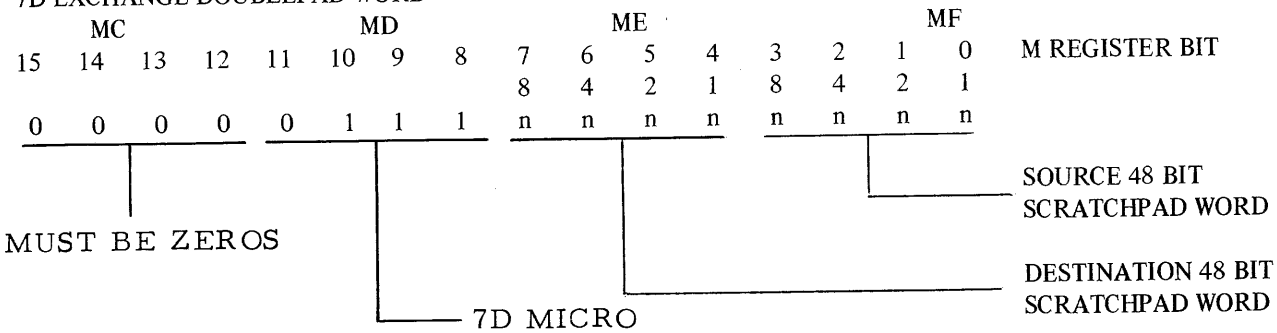
Increment (decrement) binarily the designated register(s) by the value of the literal contained in the instruction or by the value of CPL if the value of the literal is zero.

Neither overflow nor underflow of FA is detected. The value of FA may go through its maximum value or its minimum value and wrap around. Overflow of FL is also not detected. The value of FL may go through its maximum value and wrap around. Underflow of FL is detected and will not wrap around. The value of zero is left in FL.

Count variants are as follows:

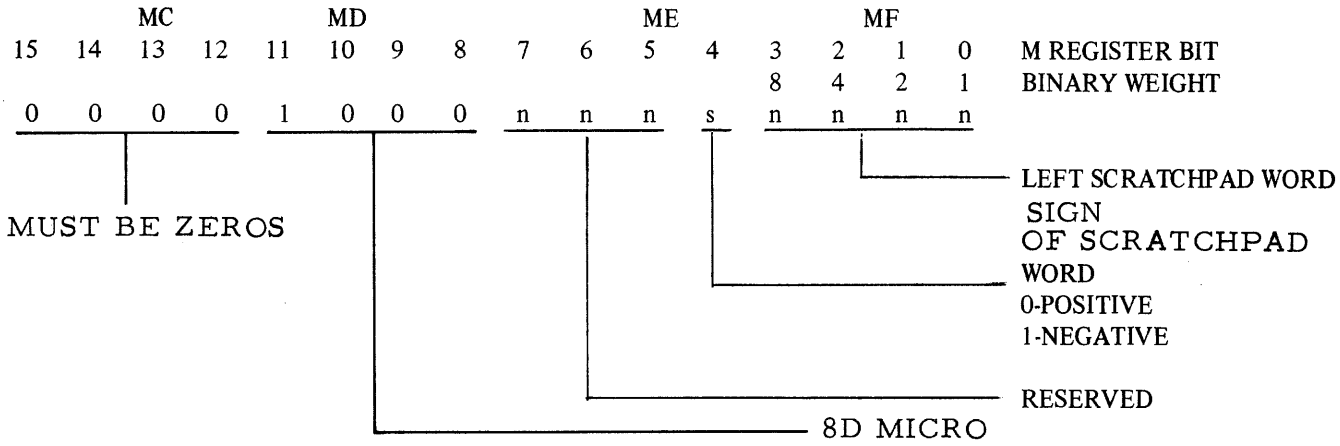
V = 000 No Count
001 Count FA Up
010 Count FL Up
011 Count FA Up and FL Down
100 Count FA Down and FL Up
101 Count FA Down
110 Count FL Down
111 Count FA Down and FL Down
Time equals four clocks.

7D EXCHANGE DOUBLEPAD WORD



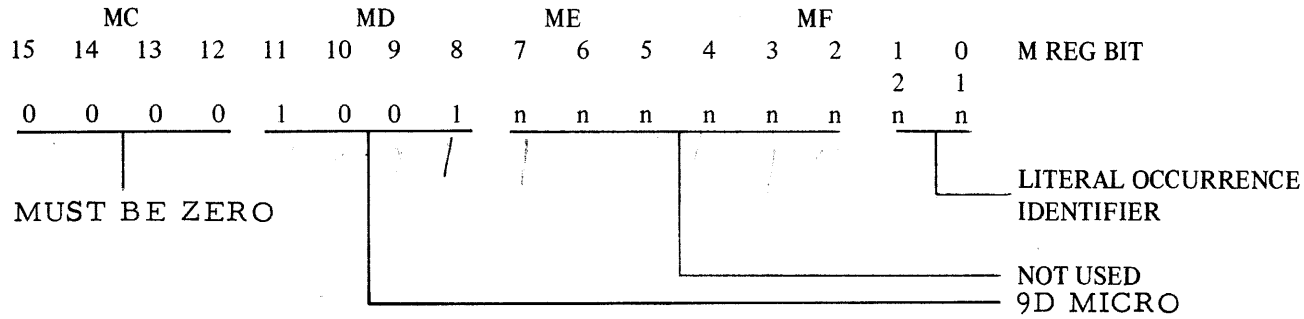
Move the contents of the FA and FB registers to a holding register. Holding register is MIR.
Move the contents of the left and right source scratchpad word to the FA and FB registers respectively. Move the contents of the holding register to the left and right word of the destination scratchpad word.

8D SCRATCHPAD RELATE FA



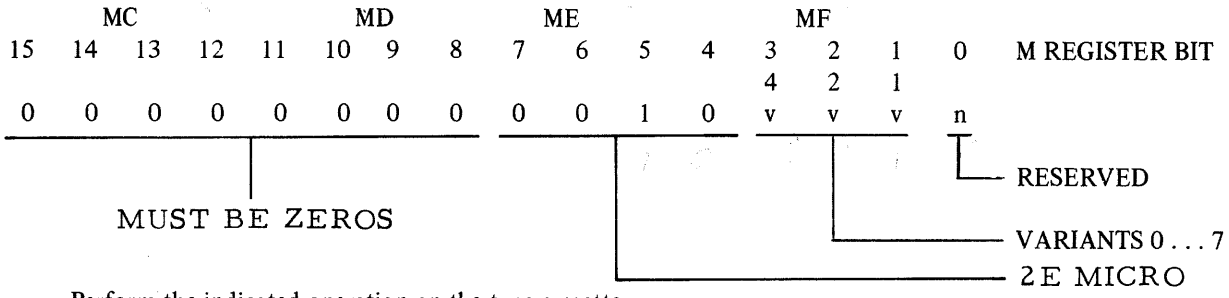
Replace the contents of the FA register by the sum of the FA register and the specified scratchpad register.
Time equals four clocks.

9D MONITOR



The Monitor has no function programmatically and is treated as a NO-OP.

2E CASSETTE CONTROL

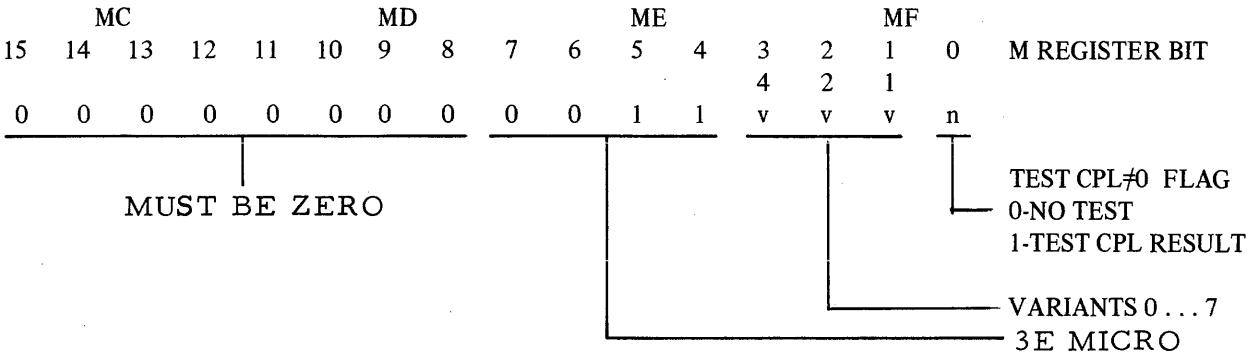


Perform the indicated operation on the tape cassette.

V=0 Start Tape
1. Stop Tape (The Processor also halts in TAPE mode.)
2. Stop Tape if X≠Y
3-7 UNDEFINED

All tape stops variants cause the tape to halt in the next available gap.
Time equals two clocks.

3E BIAS



Set CPU to the value 1 if the value of FU is 4 and to 0 otherwise.

Exception: For V=2, the value set into CPU is determined by SFU in lieu of FU.

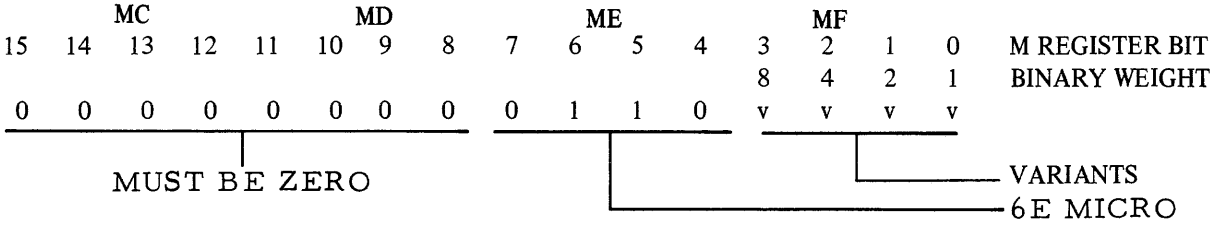
Set the value of CPL to the value denoted or to the smallest of the values denoted in the following table.

V	VALUES
0	FU
1	24 OR FL
2	24 OR SFL
3	24 OR FL OR SFL
4	CPL
5	24 OR CPL OR FL
6	CPL
7	NOT DEFINED

If test flag equals 1 and final value of CPL is not zero, the next 16 bit micro-instruction is skipped.

Time equals two clocks.

6E CARRY FF MANIPULATE



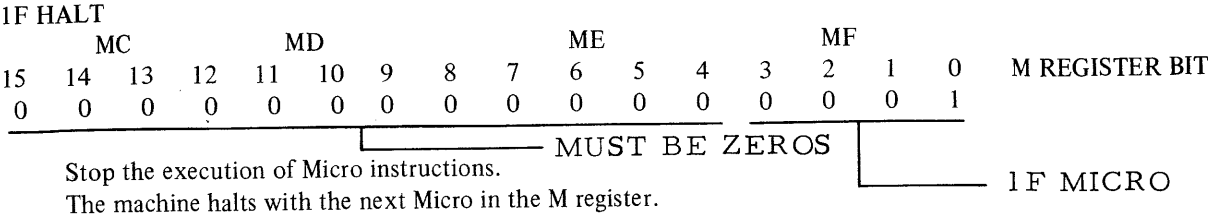
Set the carry flip-flop as specified by the variants

V = 1 SET CYF TO 0
2 SET CYF TO 1
4 SET CYF TO CYL
8 SET CYF TO CYD

NOTE: (X < Y) + (X = Y) * CYF = CYD

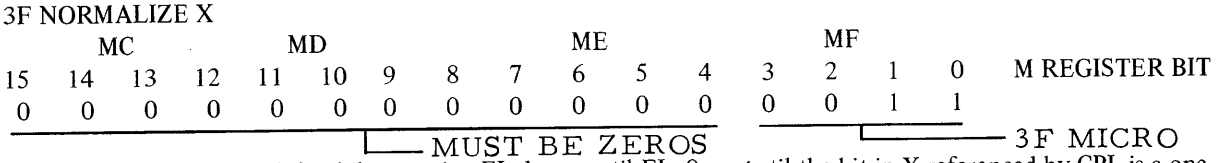
Time equals two clocks.

1F HALT



Stop the execution of Micro instructions.
The machine halts with the next Micro in the M register.
Time equals two clocks.

3F NORMALIZE X

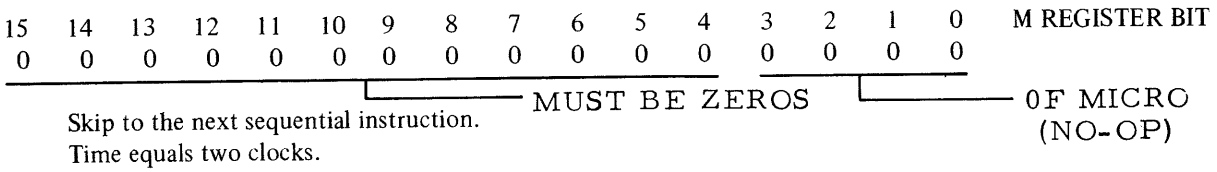


Shift the X register left while counting FL down until FL=0, or until the bit in X referenced by CPL is a one. Zeroes are shifted into the rightmost end of X.

CPL = 1 references the rightmost bit of X while CPL = 24 references the leftmost bit of X.

Time equals six clocks per bit shifted plus two additional clocks if FL=0 or plus four additional clocks if MSBX=1.

ZERO NO OPERATION



Skip to the next sequential instruction.
Time equals two clocks.

BASIC SOFTWARE OVERVIEW

The B1700 System has previously been described as one that executes its programs under control of MICRO instructions. It is impractical, however, for the programmers to write micro programs and, therefore, various higher level languages have been developed for use on the system. It is not the intent of this section to describe these higher level languages but to describe the relationship that exists between the micro program and the higher level language.

S LANGUAGE

The programmer writes a program in one of the standard high level languages such as COBOL (Common Business Oriented Language), FORTRAN (Formula Translating) or a new Burrough's language referred to as SDL (Software Development Language). After the program has been written it is compiled and from the compiler an S-Language program is generated. The S-Language is similar in nature to instructions of past processors such as data moves, arithmetic instructions, etc. The S-Language program is then stored in Main Memory and will be fetched and executed from Main Memory. It must be remembered that the S-Language instruction will not directly cause the hardware to perform a function.

INTERPRETER

In addition to the S-Language program (customer program) another program which is referred to as an interpreter is stored. An interpreter has been developed for each of the high level S-Languages; COBOL, FORTRAN and SDL. It is the function of the interpreter to fetch the S-Language instruction from Main Memory, interpret the instruction and then call a series of micro instructions which will cause the hardware to perform the function specified by the S-Language instruction. Upon completion of execution of the series of micro instructions, the interpreter will fetch the next S-Language instruction and the operation continues in this manner.

PROGRAM STORAGE

The micro instructions and series of micro instructions to perform the S-Language instruction are stored in Main Memory or may be called from disk.

The S-Language programs and required interpreters are located and loaded from disk under control of the Master Control Program (MCP). Upon completion of the load the MCP then passes control to the S-Language program. The MCP has been written in SDL and, therefore, the SDL interpreter is always present in the system. If the users program is also written in SDL, the MCP need not call an interpreter when the user's program is loaded from disk.

The B1700 user may design his own S-Language and interpreters, but in doing so they may not operate under MCP control. In this case the user must also develop his own bootstrap loader and I/O routines.

Figure I-7 illustrates the Interpreter/S-Language instruction relation and Figure I-8 shows the flow of how an S-Language Add instruction could be executed through use of an interpreter sub-routine.

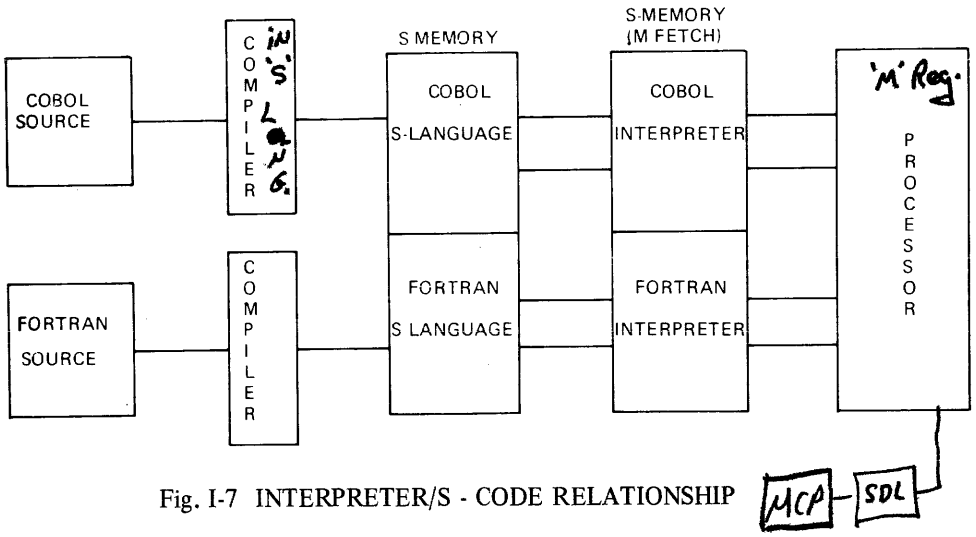


Fig. I-7 INTERPRETER/S - CODE RELATIONSHIP

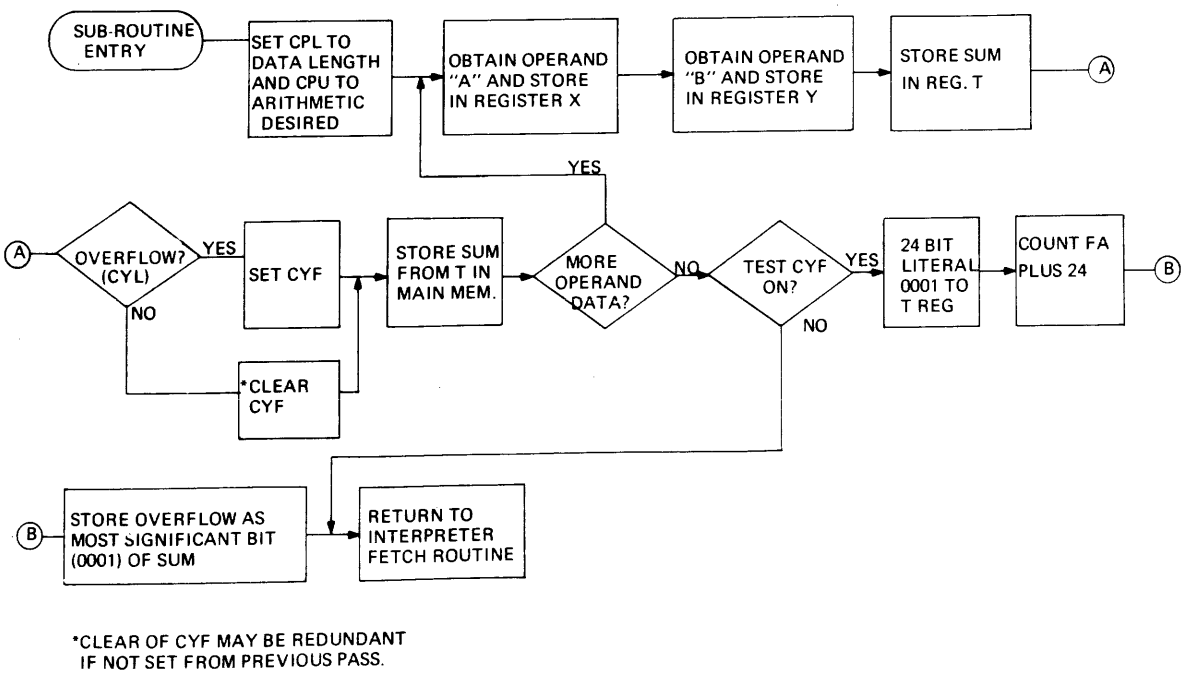


Fig. I-8 SUB-ROUTINE FLOW FOR 4BIT BED SUM (RESULTED FROM S-LANGUAGE) (SUM INSTRUCTION)

SYSTEM INTERRUPT

The B1700 Interrupt System is described as a SOFT interrupt system. That is, any interrupt which occurs does NOT cause any specific hardware function. The interrupt is not recognized by the system until it is recognized by the software of the system. In terms of hardware, there are not any specific rules for handling an interrupt and, therefore, the handling is strictly up to the discretion of the programmer/MCP.

INTERRUPT CONDITIONS

The various interrupts which occur are listed in Table I-6.

1) Timer Interrupt
2) I/O Bus Service Request Interrupt
3) Console Interrupt
4) Memory Parity Error Interrupt

TABLE I-6 INTERRUPT CONDITIONS

Each of the above listed conditions generate their own specific interrupt bit and are recognized by examination of the appropriate bits in the CC or CD Registers. (Refer to description of C Register.) In addition to the individual interrupt bits developed, the XYST (S-Y State) Register has a bit referred to as INT OR (Interrupt Or) which will indicate that one or more of the interrupt conditions are true. The software may then first test that bit of XYST [XYST(2)] and if it finds that bit true, then may examine CC and CD to determine specifically what caused the interrupt(s). If, on the other hand, the software finds the INT OR bit false, no further checking is required.

S-MEMORY (SYSTEM MEMORY)

S-Memory is the Main Memory of the B1700 System. S-Memory is used for storage of data, micro program and S Language object code. The S-Memory is available in increments of 8K bytes with the storage capacity ranging from 8K bytes to 64K bytes (8, 192 to 65,536 bytes). Parity generation and checking is provided on a byte basis with the parity bit causing the total number of bits stored to be odd.

The memory write operation is a read/write cycle and requires 750 nanoseconds to complete the cycle. The write operation can write from 1 to 24 bits of information from a source register starting at a bit address specified by the address register. A read before write occurs only for the purpose of MERGING and generating correct parity on the total data written.

NOTE: Even though a write of less than 24 bits may be specified, the actual write cycle writes 32 bit of data for parity correction which is required due to the bit addressability of the machine. Writing may be in a forward or reverse direction from the address specified. In either case the least significant bit of the source register will ALWAYS be stored in the most significant address position of the memory.

The memory read operation is strictly a read operation with 32 bits being obtained from memory. Only 24 of the 32 bits contain GOOD data or as little as one of the twenty-four bits may be considered GOOD as the length of the data is variable from 1 to 24 bits as on the write operation. The read cycle is 500 nanoseconds with data being available some time before the completion of the cycle.

Memory consists of two to eight cards located in the processor backplane with each card having an 8K byte storage capacity. Figure I-9 illustrates the layout of the memory and also the bit addressability.

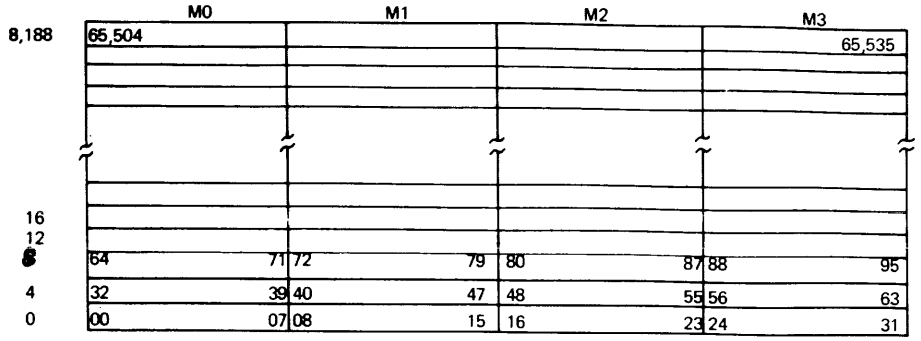


Fig. I-9 "S" MEMORY LAYOUT

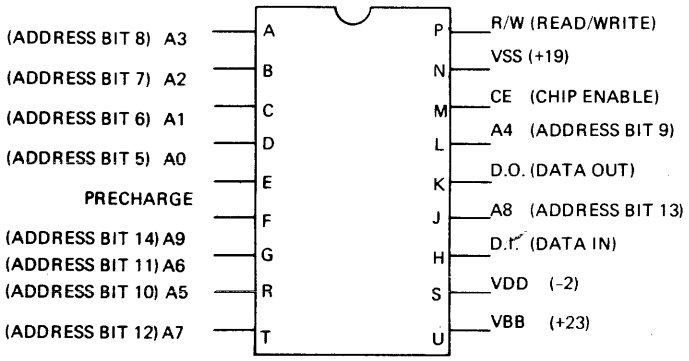


Fig. I-10 DYNAMIC STORAGE CHIP

MEMORY CHIPS (RAM)

These memory chips are contained within an eighteen (18) pin DIP package. Each memory chip contains 1024 (1k) bits and can decode binary addresses within the chip. See Figure I-10.

STORAGE BOARD

These boards are standard size B1700 boards. They are divided in half (x and y). Each half is called a module. Each module contains 4096 (4K) bytes (9 bits including parity). One board can contain 8192 (8K) bytes of memory storage.

Each module is subdivided into four (4) rows that contain nine (9) I.C. memory chips. Each row is equal to 1024 (1K) bytes of memory storage. See Figure I-11.

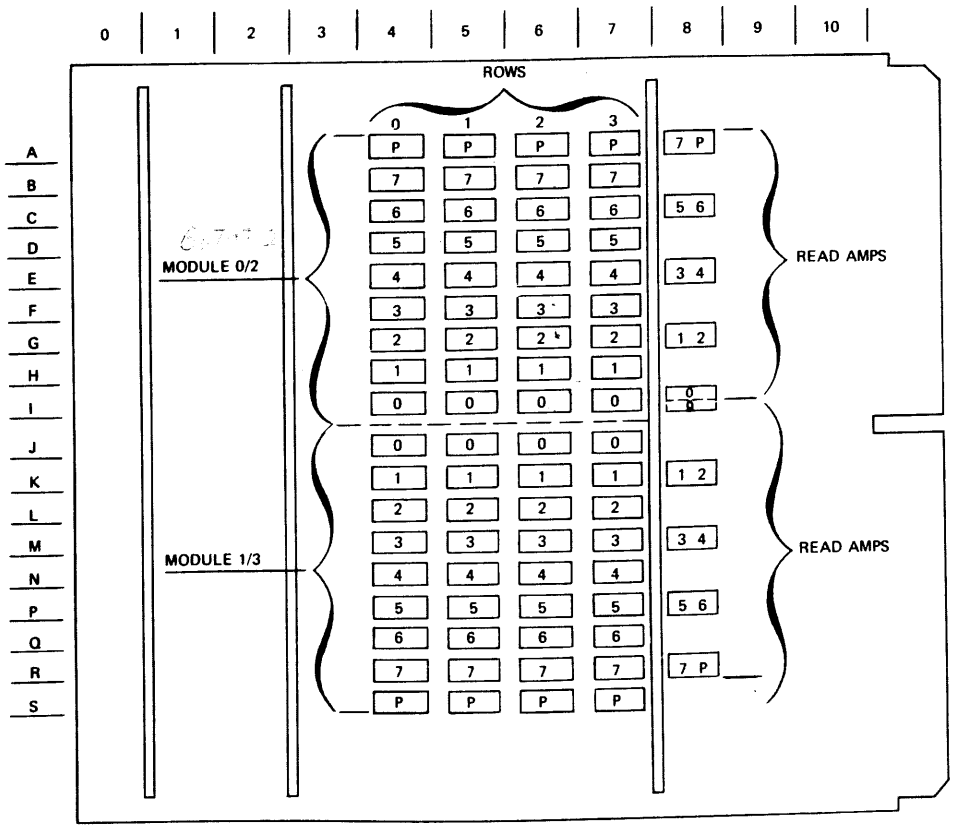
MEMORY GROUPING

The memory boards are always grouped in pairs. At no time will there be an odd number of memory boards in the B1700. With this arrangement, Modules 0 and 1 (Bytes 0 and 1) will be contained on one board and Modules 2 and 3 (Bytes 2 and 3) will be contained on the second board. See Figure I-13.

MEMORY SIZE

Memory size can vary from 8K bytes to 64K bytes in increments of 8K bytes. A minimum memory configuration will consist of two (2) boards that contain a total of 8K bytes of memory. A maximum memory configuration will consist of eight (8) boards that contain a total of 64K bytes of memory.

The capacity of a memory storage board is determined by its population of memory chips. With two (2) boards making up an 8K memory, each board must contain 4K of memory or one-half (½) of a full 8K complement. This is considered to be a half population board and may be repeatedly referred to in this manner throughout this and other manuals. See Figure I-12.



S-1 Mem Fig. I-11 "S" MEMORY STORAGE CARD

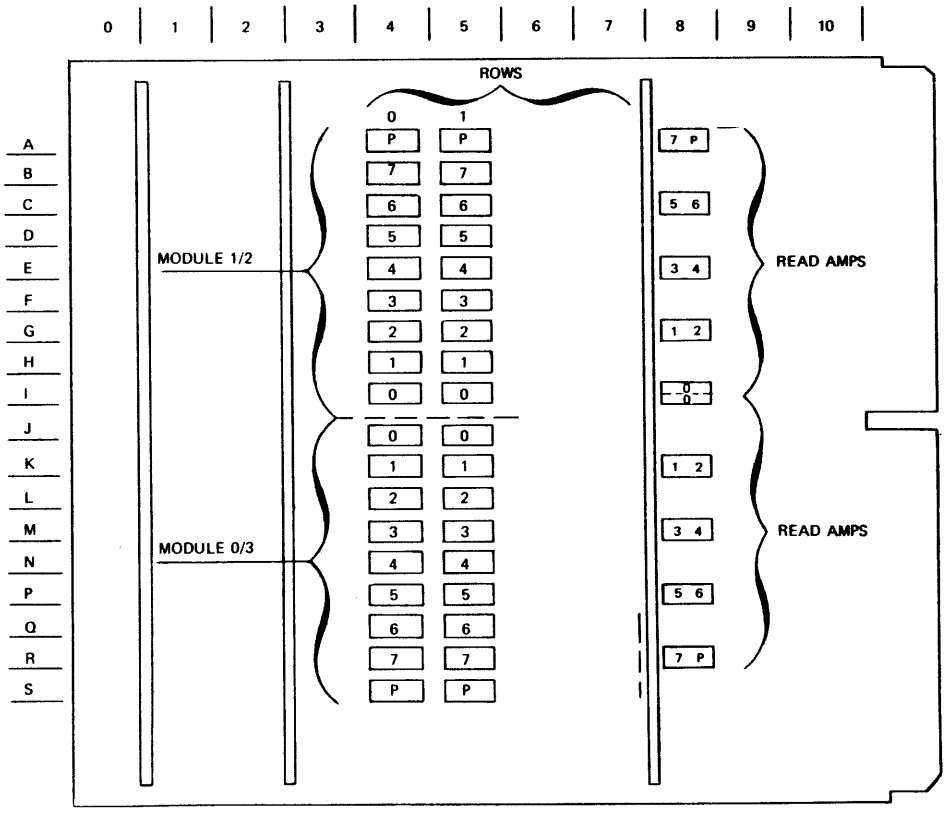


Fig. I-12 1/2 POPULATED STORAGE CARD

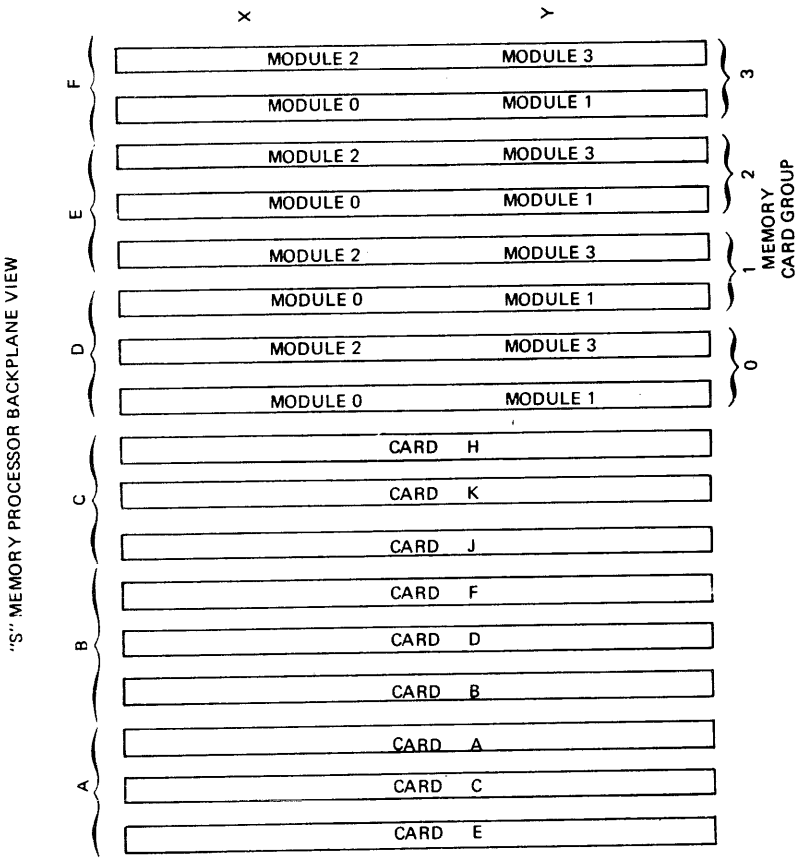


Fig. I-13

A maximum memory (64K bytes) will contain four (4) memory board groups. Each group will contain two (2) fully populated boards (16K). See Figure I-13.

Memory size has limits in that there will never be a fully populated board and a half populated board within the same group. There will either be two (2) fully populated boards or two (2) half populated boards in each group. See Section VI for further information on memory size.

REFRESH

Memory refresh is necessary because of the characteristics of the dynamic type memory. Since this type memory has a tendency to discharge through associated circuitry or leakage, it becomes necessary to restore the information. This is known as refresh.

Every refresh cycle will refresh 1/32 of the memory at a time. This means that it takes thirty-two (32) refresh cycles to refresh the complete memory. Also, the complete memory must be refreshed every two milliseconds (2 msecs).

MEMORY ADDRESS LOGIC

This area consists of the Memory Address Register, and the Address Distribution Logic. The Memory Address Register (MAR) is also called the Address Register (A), depending on whether it is addressing a micro location in memory or a data location. It is normally referred to as the MAR (A) Register. More information on the MAR (A) Register is contained under registers elsewhere in this manual.

ADDRESS DISTRIBUTION LOGIC

This area controls the incrementation of the address for micro fetching, which is a value of 16. It is also responsible for address production during the memory refresh cycles, which are required every two milliseconds for all of S-Memory.

The two higher order address bits (A17 and A18) with their complements are wired on the backplane to select a particular card location. Address bit A15 and A16 select one of the four rows of chips. Address bits A05 and A14 select a cell within each of the chips in the row selected by bits 15 and 16. See Figure I-14.

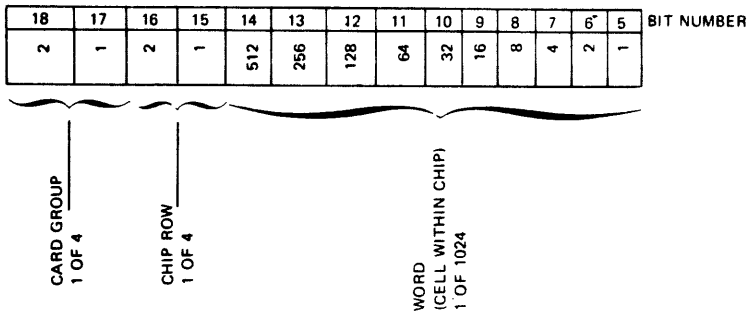


Fig. I-14 MEMORY ADDRESS BITS

MEMORY INFORMATION LOGIC AND ROTATOR

The memory information area consists of:

- Memory Information Register
- Rotator
- Parity Generator and Check
- ML Register (For Micro Fetch)

The Rotator is also involved in memory information retrieval and alignment.

The three Parity areas are responsible for the generation of ODD Parity by byte, for checking of this parity on a READ, and for indication, if an error exists on a read, and for reinsertion of the error.

MEMORY INFORMATION REGISTER (MIR)

This is a 32 bit register (0-31) used primarily for handling of S-Memory data. It also works in conjunction with the Rotator for register to register data modification (shifting or rotation).

The register is laid out in the reverse of MEX. (MEX 24-0, MIR 0-31).

Bit 31 of MIR is applied to bit 0 of MEX. When used with the Rotator for data shift/rotation, the most significant 24 bits of MIR are used as outputs to MEX.

The operation of MIR with S-Memory is slightly different since all memory cycles are 32 bit operations. On a write cycle, during the read portion, the portion of the 32 bits that will not be affected by the WRITE are applied directly to MIR. The WRITE data is applied to MIR via the Rotator, and all 32 bits are then written.

This operation is similar for a read, only the desired data (not all 32 bits) will appear in the MIR, according to the data length indicated by the instruction. The READ data length is aligned by the Rotator. At the finish, the micro is moved into the M register and an M-Fetch is started for the next micro.

ROTATOR

This unit is used to shift/rotate data from MEX, Or from S-Memory. The two inputs consists of 24 and 32 bits respectively.

The Rotator itself is made up of two stages, providing a maximum shift/rotation of 32 bit positions.

The Rotator, in conjunction with MIR, is used to shift/rotate register to register data (MEX → ROT → MIR → MEX), as in the 10C and 4D micros.

As mentioned previously, the Rotator is also used for data alignment during S-Memory READ, and WRITE operations.

PARITY

There is a parity bit for each byte (8 bits). With every read cycle, 36 bits (4 bytes + 4 parity bits) of data are read from memory. Also, when writing into memory, thirty-six (36) bits (4 bytes + parity) are written during a write cycle.

Any one of the four (4) parity bits can cause a parity error during the read cycle. This parity error will be FLAGGED by the hardware and handled by the software (program). If a parity error occurs during a micro fetch operation, then the hardware will detect the parity error and halt the processor.

MEMORY LATCHES (MLR)

The memory latches act as an intermediate storage register for micro operators read from memory on a micro fetch (M-Fetch), at the start of the previous micro execution. That is to say, that at the start of each micro execution, a memory cycle is done to obtain the next micro. This micro is held in the ML until the finish of the micro presently in the M register.

ASSOCIATED MEMORY REGISTERS

These registers are used to control the addressing, size, and type of Memory. The explanation of their functions are described elsewhere in this section. (Refer to Index) The associate memory registers are:

1. MAXS Register (Maximum S-Memory Register)
2. BR and LR Register (Base and Limit Register)
3. MAR (A) Register (Memory/Address Register)
4. FA Register (Field Address Register)
5. FB Register

I/O SUBSYSTEM

The B1700 I/O Subsystem is comprised of I/O device controls, each connected to one (or more) peripheral device, with all controls also connected to the I/O bus. The controls are located close to the processor to minimize the length of the I/O bus, which minimizes propagation time.

I/O BUS

The Input/Output Bus is a 24 bit wide bi-directional bus which is used to carry either data or commands to/from the I/O Sub-System/Processor. This bus is shared by all I/O Controls attached to the S-Memory Processor. In conjunction with the 24 bit bus are control lines which define the operation as to phase either A or B and also as to either data on the bus or a command. Refer to the detailed description of the I/O Subsystem contained in Section II of this manual for details.

I/O BASE

The controls are installed in modules called I/O bases and I/O base extensions, which are packaged similarly to the processor. (See Figure I-15.) Each control is constructed on one or more cards, and one to five of these controls are installed in each I/O base or base extension. One I/O Base can have a maximum of five I/O controls. A maximum of eight controls total is permitted when both an I/O base and I/O base extension are used.

Each base contains a distribution card which interfaces the base to the main I/O bus. The primary function of the distribution card is buffering; i.e., line receivers and line drivers, to minimize loading and reflection on the main I/O bus. The base distribution card provides the following additional functions: (a) processes and distributes the system clock to the I/O base extensions, and (b) generates and distributes the slow clocks to the I/O base extensions.

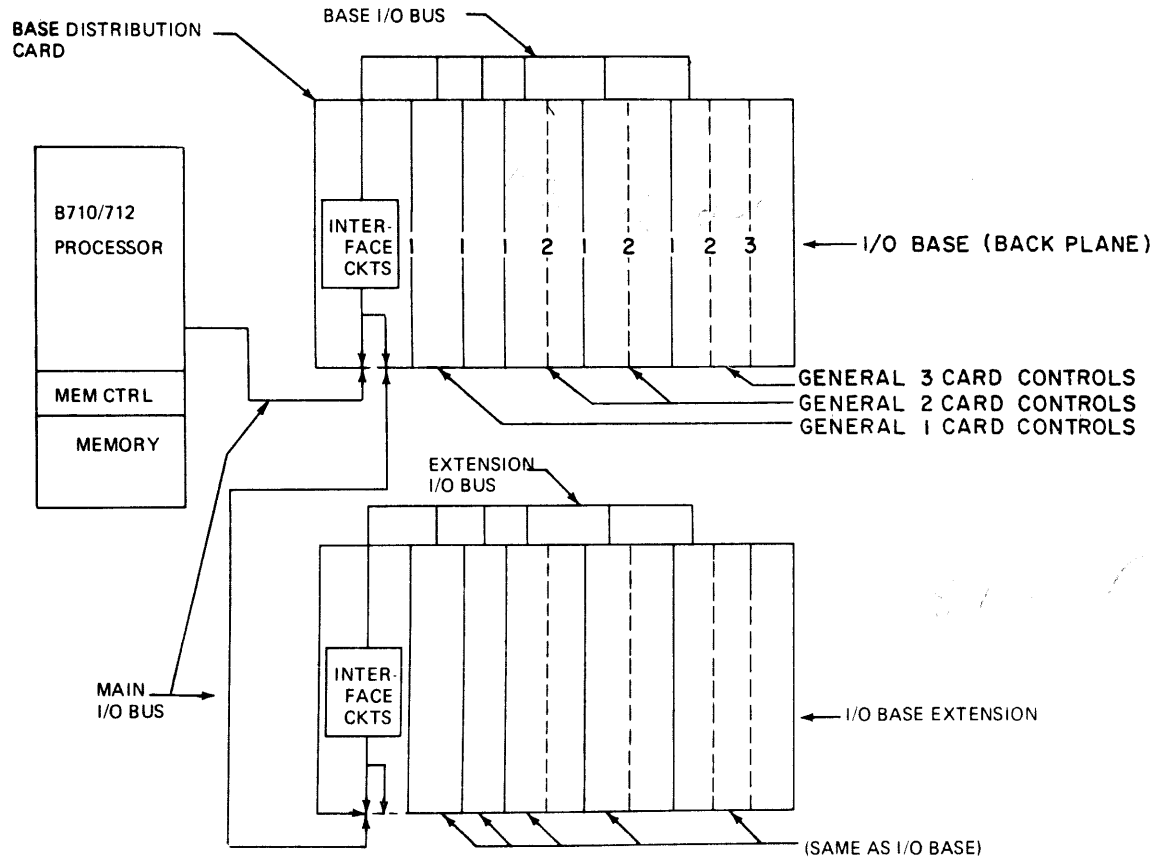
The I/O bus connects from the processor to the base distribution card by strip cable. Another strip cable connects from the base distribution card in the following base, continuing the I/O bus. Succeeding modules are similarly connected. These strip cables are connected on each distribution card by printed circuit conductors. The I/O base is explained in detail in the I/O BASE TECHNICAL MANUAL.

I/O CONTROLS

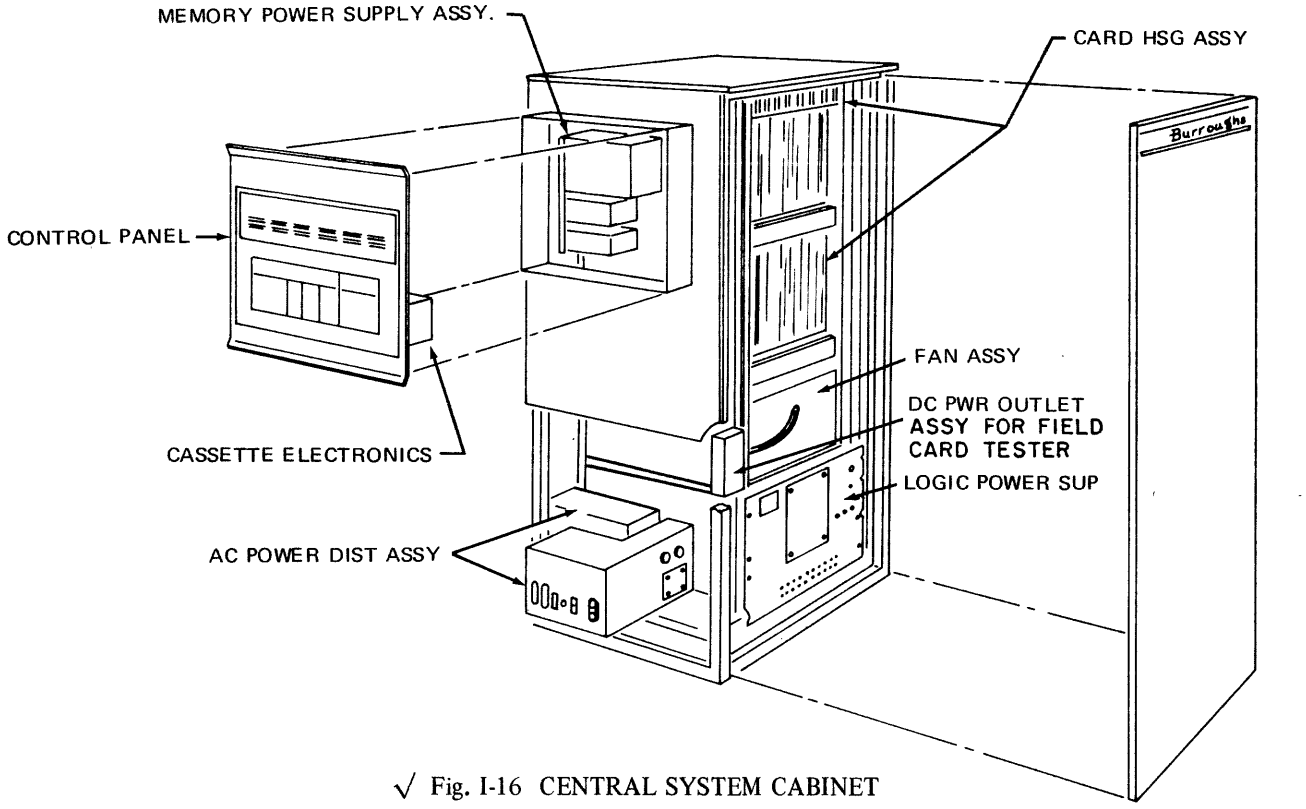
The I/O Controls used on the B1700 System are special purpose controls. Each control is unique. Several controls which have been developed are for the handling of an 80 column card reader, 96 column card equipment, disk pack, Supervisory Printer (SPO) and a Single Line Control for Data Communications. In most cases a single control handles a single device. The description of each control and operation is discussed in various I/O TECHNICAL MANUALS.

POWER

Power for the B1700 Central System is supplied by four Power Supplies within the framework of the B1700 Central System cabinet. One Logic Supply and three Memory Supplies provide all necessary power. Figure I-16 illustrates the physical location of the supplies within the Central System cabinet as well as the AC Power Distribution Assembly, DC Power Outlet Assembly, Fan Assembly and other basic assemblies of the Central System.



√ Fig. I-15 I/O SUBSYSTEM



√ Fig. I-16 CENTRAL SYSTEM CABINET

POWER DISTRIBUTION

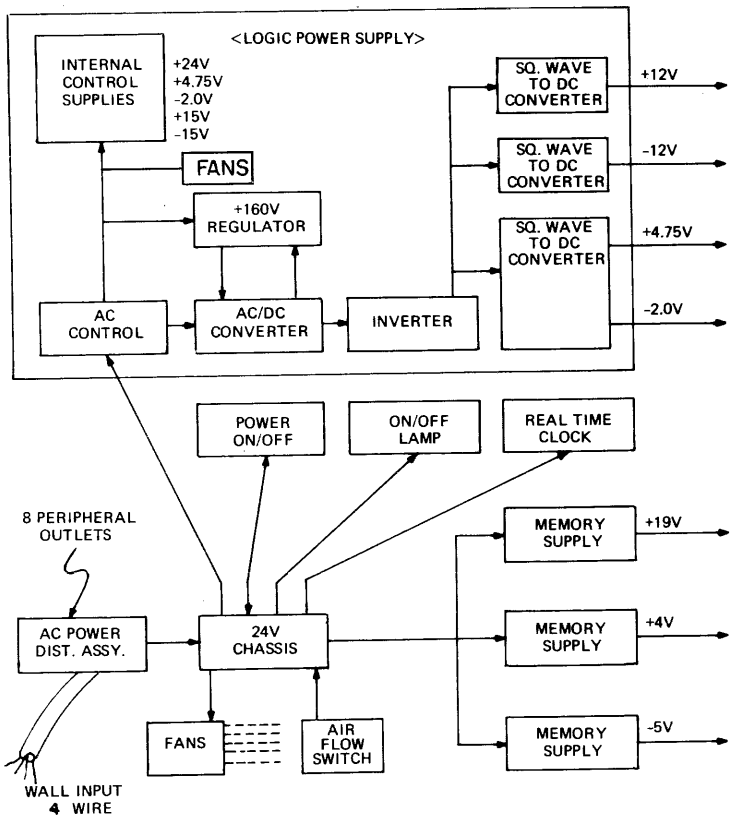
The basic distribution of power within the B1700 Central System cabinet is illustrated in Figure I-17. The Wall Input required is single phase, 188-253 VAC RMS, 47-63 Hz and is connected to the AC Power Distribution Assembly as shown. Contained within the AC Power Distribution Assembly is a main 35 amp circuit breaker which supplies the input voltages for the Logic Power Supplies, Memory Power Supplies and Fan Assemblies via the 24V Chassis. Also contained within this AC Power Distribution Assembly is a 20 amp circuit breaker which supplies voltages for the Peripheral or Convenience Outlets. A .5 amp fuse is also provided to protect the low voltage circuit of the ON/OFF Switch, ON/OFF Lamp, and associated relays contained in the 24V Chassis.

The 24V Chassis contains five Relays which are used to sequence the distribution of the input voltages to the Fan Assembly, Logic and Memory Power Supplies. All outputs of the 24V Chassis are dependant on the Power ON/OFF Switch, with the exception of the 24VAC used for the Real Time Clock circuitry. A transformer within the 24V Chassis provides a 24VAC supply which is used to pick the five relays which control the sequencing of distributing the input voltages to the Fan Assembly, Logic and Memory Power Supplies.

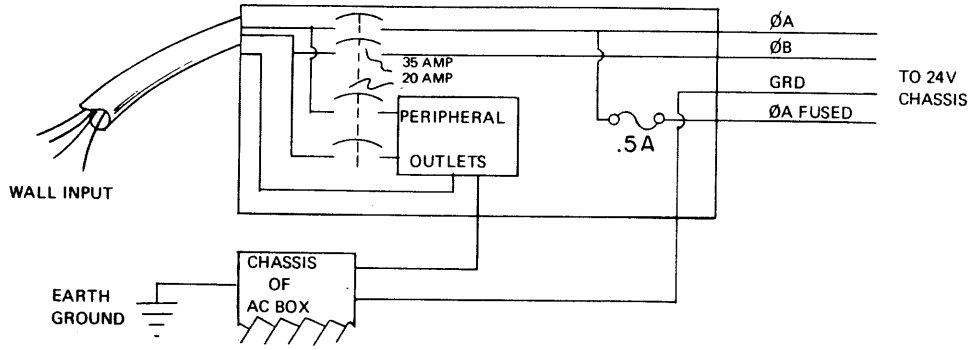
POWER OPERATION (Refer to Figures I-17 thru I-19)

AC POWER DISTRIBUTION ASSEMBLY (Refer to Figure I-17 and Figure 18)

The 35 amp circuit breaker when ON supplies the input voltages (188-253 VAC) to the 24V Chassis. The 20 amp circuit breaker when ON supplies voltages (110 VAC) to the Peripheral or Convenience outlets. Neither circuit breaker is dependant on the other for operation.



√ Fig. I-17 BASIC POWER DISTRIBUTION CENTRAL SYSTEM



√ Fig. I-18 AC POWER DISTRIBUTION ASSEMBLY BLOCK DIAGRAM

24V CHASSIS (Refer to Figure I-17 and Figure I-19)

With the 35 amp circuit breaker ON in the AC Power Distribution Assembly the input voltages (188-253 VAC) is present at the inputs of the 24V Chassis. The ØA (fused) input which is approximately 110 VAC is applied to the primary of transformer T1 which supplies 24VAC which is used internally throughout the 24V Chassis to lite lamps, pick Relays, etc.. In addition 24VAC is available for the Real Time Clock circuitry. The Block Diagram of the 24V Chassis illustrated in Figure I-19 is shown in the POWER OFF state. The sequence which occurs when the Power ON Switch is set to the ON or OFF position is as follows: (Assume the 35 amp circuit breaker is ON)

1. 24VAC available. (OFF Lite is ON)
2. Depress Power ON.
3. K3 Left is picked, K3 Right is released. (ON Lite is ON and OFF Lite is OFF)
4. K1 picked. (Fans ON) K5 Picked (30 sec time delay)
5. When Air Flow Switch closes, Pick K4 which picks K2 (Logic & Memory Power Supplies)
6. If Fans FLICKER for more than 1 sec., K4 is released thus K2 is released (Power is removed from Logic and Memory Supplies).
7. With K5 picked and K4 released, K3 right is picked (LFF Lite is ON) and the ON Lite is OFF).

1. Assume Power ON has been depressed and all supplies are up.
2. Depress Power OFF
3. Pick K3 right (OFF Lite ON and ON Lite OFF).
4. Release K3 left (Releases K1 and K5)
5. With K1 released the Fan, Logic and Memory Supplies power is removed.
6. With K5 released, K3 right is held picked by the OFF Switch.
7. When the Air Flow Switch opens, K4 is released thus K2 is released and the initial state of the Relays is established.

LOGIC POWER SUPPLY (Refer to Figure I-17)

The Logic Supply converts the 188-253 VAC RMS wall input voltage to four output voltages used throughout the Central System for the CTL Logic and Drivers and Receivers. The four output voltages are defined as follows:

1. +4.75V Used as the Vcc of CTL logic with 200 amp. nominal output current.
2. -2.0V Used as the Vee of CTL logic with 200 amp. nominal output current.
3. +12.0V Used mainly as a supply voltage to Line Drivers with a 10 amp. nominal output current.
4. -12.0V Used mainly as a supply voltage to Line Drivers and Line Receivers with a 10 amp. nominal output current.

The Logic Power Supply is a compact unit which is mounted in a standard 19 inch RETMA rack. It is physically mounted on rails which provides the facility to pull the supply out of the B1700 Central System cabinet. When pulled from the cabinet, the supply can also be rotated 90 degrees. The top is rotated 90 degrees to a vertical position. With the top removed, the heat sink may be pivoted out.

AC Control (Refer to Figure I-17)

The AC Control portion of the Logic Power Supply provides a 20 amp circuit breaker which is controlled by an overvoltage detection which will open the circuit breaker when an over voltage in either the +4.75V Logic Supply is detected. In addition, the AC Control portion provides RFI filtering, over heat detection and distribution of the 188-253 VAC input to the AC/DC Converter, the Internal Control Voltage Supplies and the 160V DC Regulator.

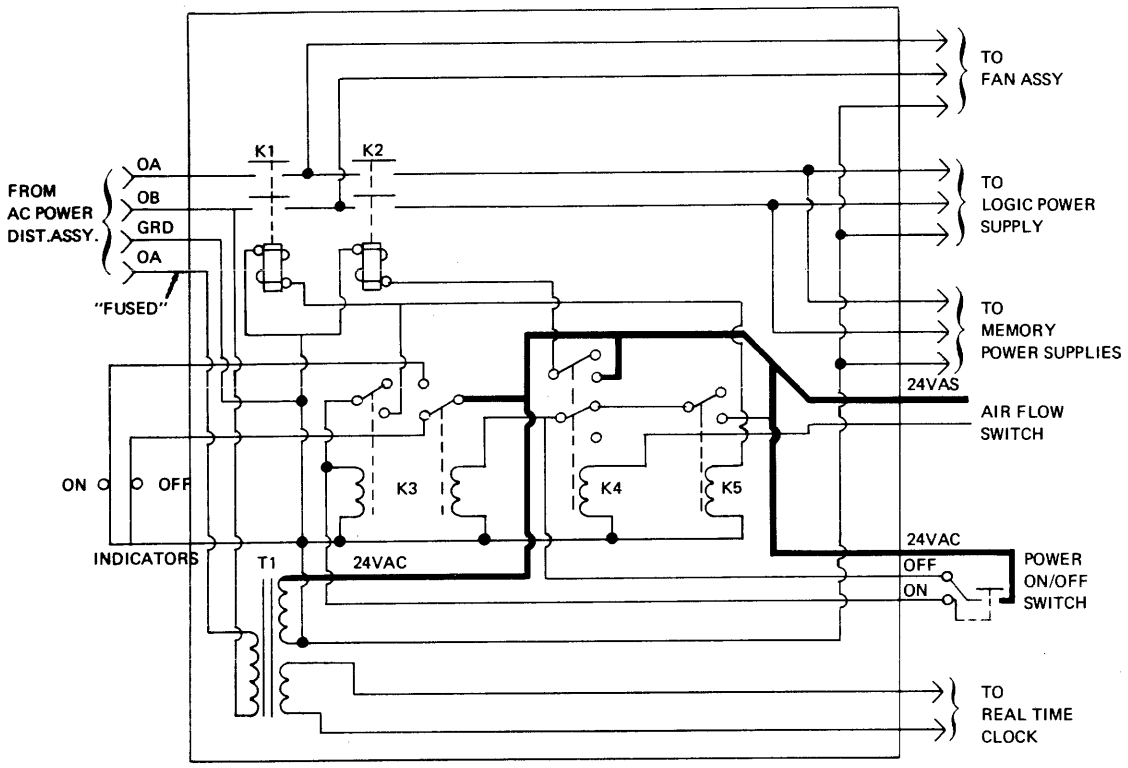


Fig. I-19 24V CHASSIS BLOCK DIAGRAM

AC/DC Converter (Refer to Figure I-17)

The AC/DC Converter converts the RAW 188-253 VAC input voltage to 160V DC. The output of the Converter is sensed by the +160V Regulator which in turn regulates the output of the Converter. The 160V DC output of the Converter is used to develop the four output voltages of the Logic Power Supply.

+160V Regulator (Refer to Figure I-17)

The 160V Regulator samples the output of the AC/DC Converter and regulates the same by controlling the firing time of two SCRs in the bridge rectifier portion of the AC/DC Converter. The 160V Regulator also converts the output of the AC Control portion of the Logic Power Supply to voltages used internally in the Regulator.

Inverter (Refer to Figure I-17)

The Inverter converts the 160VDC output of the AC/DC Converter to a 320V peak to peak approximate square wave with a frequency of 5 KHz. The periodic wave form output is applied to the primary winding of a transformer where the voltage is stepped down, rectified, and filtered to provide the four output voltages of the Logic Power Supply. The Inverter is controlled primarily by a Comparator/VCO/Logic Timing/ and Gate Driver circuit which samples the amount of output current present on the +4.75V output of the Logic Supply.

Square Wave to DC Converters (Refer to Figure I-17)

The 320V peak to peak approximate square wave output of the Inverter is applied to a step down transformer with three secondary windings. Two of the three secondary windings are rectified and used in two identical power supplies to develop the +12V and -12V Supplies. The grounding scheme determines whether a + or - supply is developed.

Each supply provides current limiting, and OV/UV detection. The OV circuit provides an initial power up clear and the OV detection provides triggering an SCR which in turn causes a fuse to blow when OV is sensed. Both supplies (+ 12V) are regulated. The third secondary winding of the step down transformer is rectified and filtered to develop the +4.75V and -2.0V Logic Supply.

Internal Control Supplies (Refer to Figure I-17)

The AC input from AC Control is applied to a transformer, stepped down, and rectified by one bridge rectifier and one center tapped bridge rectifier which in turn are used to develop five internally used control voltages. The +15V and -15V supplies are regulated separately and in addition the positive regulator tracks the negative regulator. The +24V, +4.75V and -2.0V supplies are also regulated and provide current limiting.

Logic Power Supply Characteristics

In addition to the foregoing circuits of the Logic Power Supply, OV/UV detection is provided for the +4.75V and -2.0V Logic Power Supplies. Although UV detection is available the only function of the circuitry is to provide an initial power up clear. The OV detection circuitry provides opening the 20 amp. circuit breaker in the AC Control portion of the Logic Power Supply and shorting the output of the +4.75V and -2.0V Logic Power Supply when a OV condition is sensed in either the +4.75V or -2.0V Logic Power Supply.

A -2V Shunt Regulator is provided to control the output current of the -2.0V Logic Supply (200 amps).

Logic Power Supply Component Location

There are seven KEYED etched circuit boards within the Logic Power Supply which contain most of the Power Supply's components. These seven cards contain the following BASIC units:

Card # 1. Comparator, VCO, Logic Timing, and Current Limiter (+4.75V).
Card # 2. Gate Drivers (6).
Card # 3. 160V Regulator.
Card # 4. Control Supplies (+24V, +4.75V, -2.0V, +15V and -15V).
Card # 5. -2V Shunt Regulator, OV/UV Detection for +4.75V and -2.0V Logic Power Supplies.
Card # 6. +12V or -12V Supply (dependant on grounding scheme).
Card # 7. +12V or -12V Supply (dependant on grounding scheme).

MEMORY POWER SUPPLIES (Refer to Figure I-17)

Three Memory Power Supplies are provided which convert the raw 188-253 VAC RMS wall input voltages (via the 24V Chassis) to voltages required for the 1024-Bit MOS MEMORY Chips and Dual Sense Amplifiers. One supply develops +19V DC, another +4V DC, and another -5V DC. Distribution of the three output voltages is as follows:

1. The 1024-Bit Mos Memory Chip requires +19V, +23V and -2V for operation. The +19V is supplied by the +19V DC output of one Memory Supply. The +23V is supplied by connecting the +19V and +4V outputs of the Memory Supplies in Series. The -2V is supplied by the -2V Logic Power Supply.
2. The Dual Sense Amplifiers require -5V and +4.75V for operation. The -5V is supplied by the -5V output of the Memory Supply and the +4.75V is supplied by the +4.75V Logic Power Supply.

All three supplies provide converting the raw input AC voltage to rectified DC via a step down transformer, full wave rectifier and capacitive filters. All supplies provide voltage regulation and current limiting circuitry. Over heat detection is also present which will cause a fuse to blow thus disabling the supply.

GLOSSARY OF TERMS-B1700 CENTRAL PROCESSOR

ADATnnAO	"A" DATA from Card A backplane which is the output of local memory. nn=00 through 11.
ADATnnBO	"A" DATA from Card B backplane which is the output of local memory. nn=12 through 23.
ADA/nnB1	"A" DATA which is the direct output of local memory on Card B. nn=12 through 23.
ADDMARF.	ADD to MEMORY ADDRESS REGISTER which is true for a branch forward in order to cause the literal (branching displacement magnitude) to be added to the contents of MAR.
AEB . . . A.	"A" EQUAL "B" is true if the "A" DATA equals "B" DATA at a given time.
AGB . . . AO	"A" GREATER THAN "B" is true if "A" DATA is greater than "B" DATA at a given time.
AINC . . F.	"A" REGISTER INCREMENT is true if the micro being executed will require a branch operation and also that MAR Register is selected as a sink.
ALB . . . AO	"A" LESS THAN "B" is true if the A DATA is less than the B DATA is greater than "B" DATA at a given time.
ANYAL . C.	AN/ALL is true if the Any or All variant condition of the 6C micro is true in the Four Bit Function Box.
APADEND .	"A" PAD ENABLE is true to enable the address of a register contained within a micro to be sent to Local Memory.
APADnnA.	"A" PAD DATA which is wire-or'd with data from output of local memory; Card A.
APADnnB.	"A" PAD DATA which is wire-or'd with data from output of local memory; Card B.
ARITH . D.	ARITHMETIC is true if the source register is SUM, DIFF or BICN.
ASNK . . F.	"A" SINK is true to cause the Main Exchange bits 00 through 18 to be gated to the Memory Address Register.
AO-23 . A.	"A" DATA ZERO THRU TWENTY THREE is true if any of the A DATA bits is true.
Ann . . . K1	Output of Rotation Control Logic on Card K. nn=01, 02, 04, 08, 16.
A+B . nnA.	A DATA OR B DATA OR BOTH where nn=00 through 23 are the inputs to the multiplexor elements in the 24 Bit Function Box which feed the Main Exchange.
A+B/nnA.	A DATA OR B DATA inverted is used to obtain the CMPX or CMPY from the 24 Bit Function Box.
A/B/ . . D.	True if either the Complement of "X" or the Complement of "Y" is selected in order to cause proper addressing of multiplexor elements located in the 24 Bit Function Box.
BBAnn . K.	BIT BOUNDARY ADDRESS is the least significant five bits of the MAR(A) Register. nn=01, 02, 04, 08, 16. Located on Card K.
BCARnnA.	BINARY CARRY is the carry output of the dual full adder/subtractor elements located on both cards A and B within the 24 Bit Function Box.
BDATnnB.	B DATA is the direct output of local memory elements contained on Card B where nn=12 through 23.
BDATnnTO	B DATA is the backplane wired-or of BDATA from local memory on Card A and Card B.
BDA/nnB1	B DATA is one of the outputs of Local Memory which produces the term BDATnnB. on Card B.
BGENnnA.	BINARY GENERATE is the "generate" output of the dual full adder/subtractor elements located within the 24 Bit Function Box located on cards A and B.
BGRPnnA.	"B" GROUP is an output of Local Memory on Card A.
BGRPnnB.	"B" GROUP is an output of Local Memory on Card B.
BINARYA.	BINARY is true if the value in the CPU Register indicates binary mode.
BINARYD.	BINARY is true on Card D if the micro is one which will cause a count of either FA or FL register.
BITEn.E.	BYTE "N" counts the bytes received from the cassette. n=0 through 3.
BPADnnB.	"B" PAD is an output from Local Memory on Card B.
BPRGnnA.	BINARY PROPAGATE is the propagate out of the adder in the 24 Bit Function Box located on cards A and B.
BRNCH . F.	BRANCH is an output term in the 4 Bit Function Box used in conjunction with the branch function of the 4C and 5C micros.
BRNCHF.	BRANCH is true if the 123C Branch Relative Micro is decoded in the M Register.
BSUMnnA.	BINARY SUM is the sum/difference output of the adder/subtractor located on Cards A and B for the 24 Bit Function Box.
BS0+2 . E.	BYTE ZERO or BYTE 2 is true for the first and third bytes received from cassette.
BS1+3 . E.	BYTE ONE or BYTE 3 is true for the second and fourth bytes received from the cassette.
BTQ1 . . E.	BYTE COUNT ONE is the output of the cassette logic byte counter flip-flops.

BT2 . . . E.	BYTE COUNT TWO is an output of the cassette logic byte counter flip-flops.
BUSnnIE1	BUS "N" IN is the input to the processor from the I/O Bus on Processor Card E. nn=00 through 23.
BWD . . . E.	BACKWARD DRIVE is sent to the cassette to cause a rewind operation.
CALL . . D.	CALL micro 145C as decoded on Processor Card D.
CALL . . F.	CALL micro 145C as decoded on Processor Card F.
CCn . . . F.	CONTROL REGISTER "CC" portion where n=0 through 3.
CC-MEXD1	CC REGISTER replaced by MAIN EXCHANGE.
CDn . . . F.	CONTROL REGISTER "CD" portion where n=0 through 3.
CENABLKO	CHIP ENABLE is sent to the memory storage element to allow a read or write operation.
CLEAR . C.	CLEAR is the output of the flip-flop which produces a General Processor Clear as a result of the clear button on the console having been depressed.
CLKENDE.	CLOCK ENABLE is true in the cassette logic if a bit is not received in order to produce a pseudo tape clock pulse to be used within the cassette logic.
CLK4 . . KO	CLOCK 4 is the 4 MHZ output of the clock generator on Processor Card K.
CLK4/ . KO	CLOCK 4 NOT is the inverted 4 MHZ output of the clock generator on Processor Card K.
CLK8 . . KO	CLOCK 8 is the 8 MHZ output of the clock generator on Processor Card K.
CLR . ENC.	CLEAR ENABLE is true to allow a clear from the console to occur with the condition being that a refresh cycle for memory has not been granted.
CLR . . . J.	CLEAR is true to the memory latches on Card J.
CLRM . . DO	CLEAR "M" is true to cause a clear of the M Register.
CLRRGIK .	CLEAR REAL TIME CLOCK GENERATOR is true for 16.667 milli-seconds and allows the clearing of the Real Time Clock counter on Card K.
CNTDN . F1	COUNT DOWN is true to cause the Stack Pointer for A STACK to be decremented.
CNTUD . F1	COUNT UP is true to cause the STACK Pointer for the A STACK to be incremented.
CNTn . . K.	COUNT "N" is the output of the Real Time Clock Counter on Card K.
CPSINKC.	CP SINK is true if the CP portion of the C Register is designated as a destination.
CREGnnCO	CONTROL REGISTER BITS where nn=00 through 07 which corresponds to the CP portion of the C Register.
CSAGPa DO	CHIP SELECT GROUP "A" is addressing levels for local memory A DATA to select four bit registers. "a" = A,B,C,D,E or F.
CSAPADDO	CHIP SELECT "A" PAD is false for the register selection and A STACK words 0 through 7. It is true for Left Scratchpad words 0 through 15.
CSBGRPTO	CHIP SELECT B GROUP is true to select registers and A STACK words 8 through 15 of B DATA and false for Right Scratchpad words 0 through 15.
CSBPADDO	CHIP SELECT B PAD is true for Right Scratchpad words zero through fifteen and false for registers and A STACK words eight through fifteen of B DATA.
CSSINKF1	CHIP SELECT SINK is a result of micro decoding and timing which when true indicates a register, A STACK word or Scratchpad word has been selected as a sink. Generates Local Memory Write Enable.
CSTPG . D1	CASSETTE STOP AT GAP is true as a result of Cassette micro which indicates stop.
CSTRT . D0	CASSETTE START is true as a result of a Cassette micro indicating start cassette.
CSWnn . T1	CONSOLE SWITCHES is the input from the twenty-four console switches and are the inputs to multi-plexors which gate the console switches to the Main Exchange. nn=00 through 23.
CYD . . . A.	CARRY DECREMENT is the borrow output of the adder/subtractor most significant stage as determined by the value in CPL Register.
CYL . . . TO	CARRY LEVEL OUT is either the carry or borrow output of the adder/subtractor and is the wired-or from Cards A and B which produce the terms CYL . . . BO, CYL . 1 . AO and CYL . 2 . AO which feed CYL . . . TO.
C/S/C . T1	True when the Clear Button on the Console is depressed.
C/S/C/T1	False when the Clear Button on the Console is depressed.
C/S/G . T1	True when the READ/Write button on the Console is depressed.
C/S/G/T1	False when the READ/WRITE button on the Console is depressed.
C/S/H . T1	True when the HALT button on the Console is depressed.
C/S/H/T1	False when the HALT button on the Console is depressed.
C/S/L . T1	True when the LOAD button on the Console is depressed.
C/S/L/T1	False when the LOAD button on the Console is depressed.

C/S/S . T1	True when the START button on the Console is depressed.
C/S/S/T1	False when the START button on the Console is depressed.
DATASTCO	DATA STROBE on Card C is true to strobe read data from memory into the Memory Information Register.
DATASTKO	DATA STROBE on Card K is true for a 7C Read/Write Memory micro to allow the parity error detection logic to be enabled.
DATA=0E.	DATA EQUAL ZERO is true if the bit received from Cassette is a "0" bit.
DEC . . . D.	DECIMAL is true if the value in CPU indicates a decimal operation.
DELAY8F.	DELAY 8 MHZ is a delayed 8 MHZ clock which is used to produce a Local Memory Write Enable pulse.
DFL25 . K.	DATA FIELD LENGTH 25 is true to force good parity to be written.
DFL26/K.	DATA FIELD LENGTH 26 NOT is false to force bad parity to be written in a memory location.
DISCYF.	DISABLE CARRY FLIP-FLOP is true to disable the Carry Flip-Flop input to the adder/subtractor of the twenty-four bit function box.
DISPL . C.	DISPLAY LEVEL is true if the register selected is to be displayed.
DIVBY5K.	DIVIDE BY 5 is true if the system has 50 CPS input power and is used in the Real Time Clock logic.
DIVBY6K.	DIVIDE BY 6 is true if the system has 60 CPS input power and is used in the Real Time Clock logic.
DRFSETJ.	DEMAND REFRESH SET is true to cause the Demand Refresh Flip-Flop to set.
DRF . . . JO	DEMAND REFRESH FLIP-FLOP sets approximately every 62 milli-seconds for a memory refresh.
DSCP1 . K.	DELAYED SYSTEM CLOCK is produced from a 4 MHZ clock and delayed by a buffer element.
DSETC . C.	D SET C REGISTER is true when the CP Register is selected as a sink.
DSETMLJ .	D SET MEMORY LATCHES is true to place the memory latches in a D Set mode.
DSUMnnA .	DECIMAL SUM is the BCD corrected output of the adder in the 24 Bit Function Box.
ENBCYFC .	ENABLE CARRY FLIP-FLOP is true to enable the Carry Flip-Flop to be gated as an input to the 24 Bit Function Box.
ENSn . . D.	ENABLE SEQUENCE n is true to enable a finish term to be produced. ENSn . . D. is a result of micro decoding where n=1 through 4.
EQUAL . B.	EQUAL is true if the 6C micro is being executed and the mask is equal to the register selected.
EXCKENKO	EXTERNAL CLOCK ENABLE is not wired and may be forced true if an external clock generator is desired.
FBPAG . H1	FORCE BAD PARITY is true if the address is out of bounds to force a parity error indication.
FGPAE . H1	FORCE GOOD PARITY if the address is at the upper limit of memory but still within bounds. Forces good parity for Module 0,1 or 2 depending upon address.
FGP0nHH1	FORCE GOOD PARITY "N" where N= 0,1,2 or 3 to force good parity for an out of bounds module although the Key Byte Address is still in bounds.
FINISHC.	FINISH is true when a micro is finished and occurs with a 4 MHZ clock. Input to console logic flip-flops on CARD C.
FINISHDO	FINISH is true as a result of micro decoding and micro timing when a micro is done or finished.
FINOK . F.	FINISH OK is true if finish occurs and a refresh has not been granted in order to allow upcounting of MAR+1.
FLCOMPDO	FIELD LENGTH COMPARE is true to allow a comparison for the 3E Bias micro or if the FLCN Register is selected as source.
FLDN6DD.	FL REGISTER DOWN is true if the micro is a 6D with the Count FL down variant.
FLDN7CD.	FL REGISTER DOWN is true if the micro is a 7C with the Count F1 down variant.
FLDOWNDO	FL DOWN is true if the operation is a count FL down.
FL . L . CB.	FL LESS THAN ZERO is ture if the operation is a count FL down and the operation is a count FL down and the operation is trying to count FL below a count of zero.
FWD . . . E.	FORWARD DRIVE is a level sent to the cassette to cause forward tape motion.
GAP . . . E .	GAP is true if a cassette tape gap is present.
GAPI . . E.	GAP I is true if tape pulses have been absent for 500 usec.
GOTOCOJ.	GO TO is true to reset the Refresh Control Flip-Flop when the 62 us multi has timed out and Granted Refresh is false.

GPCLRBCO	GENERAL PROCESSOR CLEAR BUS which is true as a result of Clear being depressed on the Console or power up clear.
GRF . . . CO	GRANTED REFRESH FLIP-FLOP is set if the refresh cycle is granted.
GRINHIC.	GRANTED INHIBIT CONTROL is true if a Console clear operation is not occurring therefore a refresh is allowed to occur.
GRPSNKD.	GROUP SINK is true if either Y,BR or LR is a sink for the 2C, 8C, 9C or 10C micros.
HALLTRF.	Halt is true when the HALT . . CO Flip-Flop is set which indicates the Processor is to be halted. HALLTRF. enables resetting the RUNS . . FO Flip-Flop when the Micro currently executing is "finished".
HALT . . CO	Halt is a 2 clock period true pulse which occurs when the Halt Button on the Console has been depressed. HALT . . CO causes the HALT . . CO flip-flop to set thus remembering the fact that a halt of the Processor is to occur.
HALTP8F.	Halt Processor is the OR-ed result of all conditions which can cause the RUNS . . FO flip-flop to be reset; thus halting the Processor. The conditions are depressing the Halt Push Button, the execution of the Halt Micro, and MFETCH parity error, a Cassette Tape parity error, the Stop at the Gap or Stop on X≠Y Micro and MTR Mode true or when the Processor is in the Step mode and Finish occurs.
HALTS . C.	Halt Switches is true when the Processor is in the Halt state. HALTS . C. is used to enable generating a two clock period Load Timing pulse (L/DTIMCO) which is used to initiate a Read or Write of S-Memory from the Console.
HALTS . F.	Halt State is true when the RUNS . . FO flip-flop is reset. When true the Processor is in the Halt state.
HLDRFRF.	Hold Demand Refresh is normally true and enables a refresh of S-Memory to occur via setting GRF . . . C. and generating RFG . . . CO. When false because of either the M-Register has been designated as sink, a jump condition exists or the Processor is to be halted, a refresh S-Memory cycle is delayed until the specific operation in progress is finished.
HOLD . . F.	Hold is the set output of the HOLD . . F. flip-flop. When set it indicates the U-Register is being sourced either in the Run or MTR Mode. NO OPs are forced while the current Micro executing is "held" in the M-Register. This causes FINISHDO to occur at a frequent interval thus allowing a refresh of S-Memory to occur.
HOLD./FO	Hold Not is the reset output of the HOLD . . F. flip-flop. HOLD ./FO is normally true except when the U-Register is sourced and is used primarily when true to "expose" the Micro held in the M-Register to the Micro Distribution Bus for decoding and execution.
HU/FINF.	Hold Not, UFULL Not and Finish is true when HOLD ./FO, UFUL ./.F, and FINISHDO are true. When true it enables generating a S-Memory cycle to fetch the next Micro to be executed from S-Memory.
IDATA . E.	Incoming Data is the CTL converted serial data bit received in the Processor (Card E) from the Cassette Tape.
IDATASE .	Incoming Data Stored is the set output of a flip-flop in the Cassette control logic of the Processor (Card E) which indicates a serial data bit from tape was received during the time a tape clock pulse was received from the Cassette. IDATASE. remains true until the tape clock pulse goes false which effectively holds the presense of a serial data bit for a considerable length of time.
IDATI . E.	Incoming Data In is true when IDATASE. is true and TO time occurs providing the assembling of serial data from the tape is not to be disabled. IDATI . E. is the input to the U-Register (Lower) which assembles the serial data bits from tape.
IDTESTDO	Increment Decrement Test is the result of decoding the 3C Micro with the manipulate variants set to either Increment & Test or Decrement & Test. When true it enables generating 3CSKIPDO which causes the next upcoming Micro to be skipped in the event either over flow or under flow is detected on the functions which occurred.
IHMPARH1	
INCA . . CO	Increment A is a two clock period pulse which occurs when the Increment A pushbutton is depressed. When true it increments the value of MAR(A) by 16 bits which points to the address of the next Micro.
INCA . . T1	Increment A (T1) is the true when the Increment A push button is depressed. When in the halt state it generates the two clock period INCA . . CO.
INCA/ .T1	Increment A Not (T1) is true when the Increment A push button is not depressed. When true it effectively resets two flip-flops used to generate the two clock period INCA . . CO pulse.

INHCLRC .	Inhibit Clear prevents generating a General Processor Clear (GPCLRBCO) when granted refresh (GRF . . . C.) is true.
INTERPF.	Interrupt "OR" is the "OR-ed" output of sensing any of the four Interrupt conditions. When true the level is gated to the Auxiliary 4-bit Bus (bit 2) when XYST is sourced.
INV60HK.	Inverter 60 Hz is true during each negative half cycle of the 60 Hz input used for the generation of the Real Time Clock pulses.
IORCO . F.	I/O Receive is true when either the 1C or 2C Micro is executed and DATA is source. IORCO . F. enables gating the contents of the I/O Bus to the Main 24-bit Exchange.
I/OCL . K.	I/O Clock is the clock pulses sent to the I/O Controls. The frequency is that of the System Clock and it occurs approximately 30 nsec after the inverter system.
JUMP/ .F.	Jump Not is true when a Micro is executing which does not require that MAR(A) be incremented or decremented or replaced by a value other than the normal increment of "plus 1", (MAR+1). It's used to enable halting the Processor when a halt condition exists.
KBAnn . H.	Key Byte Address (nn = 03 thru 18) are the outputs of the MAR(A) Register bits 03 thru 18.
KBA04 . Hl	Key Byte Address 04 has special significance as the incrementation of MAR(A) by MAR+1 . FO will effectively toggle Key Byte Address 04. This output bit position of MAR(A) thus points to one of two 16-bit Micros in the ML-Register.
LBUFCKA .	L Buff Clock (Card A) is the clock used to set the data on the Main 24-bit Exchange into LBUF (bits 00 thru 11) on Card A. The clock occurs when the inverted System Clock occurs.
LBUFCKB .	L Buff Clock (Card B) is the clock used to set the data on the Main 24-bit Exchange into LBUF (bits 12 thru 23) on Card B. The clock occurs when the inverted System Clock occurs.
LBUFnnA1	L Buff (nn = 00 thru 11) are the outputs of LBUF (bits 00 thru 11) on Card A. LBUF is the input holding register to all storage elements within Local Memory.
LBUFnnB1	L Buff (nn = 12 thru 23) are the outputs of LBUF (bits 12 thru 23) on Card B. LBUF is the input holding Register to all storage elements within Local Memory.
LDBSROE.	Leading Byte SRO is true when the leading one bit from Cassette Tape is sensed in the U-Register (Lower) and the byte is either the first or second and parity is good. It's used to generate U-Register Full (UFULL . EO).
LENMKnCO	Length Mask (n = 0 thru 4) is used to generate a mask of 1 to 24 bits for operations which require the use of the Rotation logic.
LIFTMKFO	Lift Mask is used to generate a mask of 24-bits in order to allow a complete 24-bit register to be gated onto the Main 24-bit Exchange.
LINKBTC .	Link Bit is the set output of the Link Flip-Flop. The flip-flop is used to temporarily store the truncated data bit during left or right shift operations which involve 48-bits of information.
LITn . . . C	Literal (n = 0 thru 4) are used to generate the length of the mask (LEMKnCO) by using the literal value of the Micro or the value of CPL depending on the particular operation.
LMADDnB1	Local Memory Address (n = 0 thru 3) B1 are the address line inputs to each of twelve 64-bit Memory Chips used to store the 12 MSB of all 24-bit storage areas of Local Memory. Located on Card B.
LMADDnA1	Local Memory Address (n = 0 thru 3) A1 are the address line inputs to each of twelve 64-bit Memory Chips used to store the 12 LSB of all 24-bit storage areas of Local Memory. Located on Card A.
LMADDnBTO	Local Memory Address (n = 0 thru 3) BTO are the four address lines which address all twenty-four 64 bit Memory Chips of Local Memory. The levels become either LMADDnA1 or B1 on cards A & B respectively.
LMWE . . FO	Local Memory Write Enable is true when a storage area within Local Memory is designated as sink. The level is the write enable to the twenty four 64 bit Memory Chips of all of Local Memory.
LOAD . . CO	Load is a two clock period pulse generated when the Load Push Button is depressed on the Conole. It can only be generated in the halt state of the Processor and will cause a selected register to be loaded with the contents of the Console Switches.
LOAD/ . C.	Load Not is true when LOAD . . CO is false and is used in the halt state of the Processor to force the 1C pseudo micro (move the register selected by the console switches to NULL). This displays the register selected on the Console lamps.
LSUY . . A.	Least Significant Unit of Y is true when the LSB of the Y-Register is equal to 1, when CPU=00, When CPU≠00, then the level is true if the four LSB of the Y-Register equals 1001 (decimal 9).
L/DTIMCO	Load Timing is a two clock period pulses which occurs when the Read/Write Pushbutton on the Console has been depressed providing the Processor is in the halt state. The pulses will cause either a read or write of S-Memory to occur depending on the position of the Register Group rotary switch.

MARCDnH1	MEMORY ADDRESS REGISTER CONTROL D is true to place MAR in the "D" set mode.
MARCDOH.	MEMORY ADDRESS REGISTER CONTROL is true to place MAR in the Subtract Mode.
MARCD2H	MEMORY ADDRESS CONTROL is true to place the MAR Register in the Add Mode. True with MARCDOH. to place MAR in subtract mode.
MAR+1 . FO	MEMORY ADDRESS REGISTER PLUS ONE is true to upcount the micro address.
MAR-MXFO	MEMORY ADDRESS REGISTER REPLACED BY MAIN EXCHANGE.
MASKnnA.	MASK is generated to allow data according to proper length to the Main Exchange.
MASKnnK.	MASKnn is the output of the reset side of the Memory Information Register.
MASKSTCO	MASK STROBE CONTROL is true to clock the mask into MIR for rotation operations and also inhibits the lift mask term from allowing all 24 bits of data to the Main Exchange.
MAXSSEF.	MAXIMUM "S" REGISTER SOURCE is true for a 1C or 2C micro with MAXS designated as source.
MAXSnnE.	MAXIMUM "S" REGISTER is the output of a wired chip indicating maximum S-Memory installed where nn=15 thru 19.
MBUSEBFO	M BUS ENABLE is true to bits 16 through 23 of MAXS, CONSOLE SWITCHES and I/O Buf to the Main Exchange.
MBUSENFO	M BUS ENABLE is true to allow bits 00 through 11 of the M Register to the Main Exchange bits 04 through 15. Generally provides enable for multiplexor elements on Card E to gate data to Main Exchange bits 00 through 15.
MBUSEnE.	M BUS ENABLE where n=1 or 2 is true to multiplexor elements on Card E to gate data to Main Exhange.
MBUSnnFO	M BUS "N" is the addressing levels to the multiplexor elements on Card E to select which data is to be gated to the Main Exchange. NN=00, 01 or 12.
MCAR15B.	MODULO CARRY 15 is true if when decrementing the FL Register a subtraction would cause FL from going below zero. FL will be forced to a value of zero in place of the negative value that would occur as a normal result of the subtraction.
MCONENDO	MULTIPLEXOR CONTROL is a term which controls the multiplexor outputs on Cards A and B upper 20 bits to the Main Exchange.
MCONMnDO	MULTIPLEXOR CONTROL where n=0, 1 or 2 are the addressing terms to the multiplexor elements on Cards A and B.
MDATnnA.	MULTIPLEXOR DATA where nn=00 through 23 are the direct outputs of the multiplexors on Card A and B prior to gating to the Main Exchange.
MEM/ .C.	MEMORY NOT is true if the operation is not a 7C Read/Write memory micro or a read or write from the console.
MEXCENDO	MULTIPLEXOR EXCHANGE ENABLE is a term which controls the multiplexor outputs on Card A least significant four bits to the Main Exchange.
MEXnnBaO	MAIN EXCHANGE BITS ZERO THRU TWENTY-THREE on Cards A, K, B, and E which are wire-or'd at the backplane to produce MEXnnBTO.
MFETCHFO	MICRO FETCH is true if the memory read operation is to fetch a micro.
MGENnnA.	MASK GENERATE is produced on Cards A and B to produce a mask to gate data to the Main Exchange or produce a mask for shift/rotate operations.
MIC . 1FF.	MICRO 1F; HALT
MIC . 3FF.	MICRO 3F; NORMALIZE X.
MIC . 4DC.	MICRO 4D; Shift/Rotate X or Y as decoded on Card C.
MIC . 4DF .	MICRO 4D; Shift/Rotate X or Y as decoded on Card F.
MIC . 5DC.	MICRO 5D; Shift X and Y as decoded on Card C.
MIC . 6DC.	MICRO 6D; Count FA/F1 as decoded on Card C.
MIC . 6DD.	MICRO 6D; Count FA/FL as decoded on Card D.
MIC . 7DF.	MICRO 7D; Exchange Doublepad Word as decoded on Card F.
MIC . 8DD.	MICRO 8D; Scratchpad Relate FA as decoded on Card D.
MLCONTHO	MEMORY LATCH CONTROL is true to allow memory data to be read from memory latches 16 through 31.
MLCON/J.	MEMORY LATCH CONTROL NOT is false at the time MLCONTHO is true to prevent memory latches 00 through 15 from being read.
MLENBLFO	MEMORY LATCH ENABLE is true to allow memory latches 00 through 15 to be read.
MLnn . . JO	MEMORY LATCH OUTPUT where nn=00 through 31.
MODnn . H1	MODIFIED ADDRESS is the output of the memory address modification logic which adds/subtracts one from the address in MAR.

MOPnnBEO	MICRO OPERATOR BUS is the output of the M Register where nn=00 through 15.
MOPnnBTO	MICRO OPERATOR BUS is the wired-or of the M Register output at the backplane.
MOP05/C.	MICRO OPERATOR BIT FIVE FALSE.
MOVE8/E.	MOVE EIGHT BIT LITERAL NOT is true if the micro in the M REGISTER is not an 8 bit literal.
MPDOn . KO	MEMORY PARITY BIT TO MODULE "N" where n=0 through 3 is the output of the parity generator.
MRDnn . J1	MEMORY READ DATA input to the Memory Information Register.
MRDnn . MO	MEMORY READ DATA from the memory storage cards.
MREGnnE.	M REGISTER BITS where nn=00 through 15.
MSBX . . BO	MOST SIGNIFICANT BIT OF X as designated by CPL from CARD B.
MSBX . nAO	MOST SIGNIFICANT BIT OF X as designated by CPL from CARD A.
MSINK . E.	M REGISTER SINK is true to gate the Main Exchange Data to the M Register if designated as a destination for a register move type micro.
MSINKFO	M REGISTER SINK produced logically on CARD F to enable Main Exchange to M Register. (MSINK . E.)
MSKST2K.	MASK STROBE TWO is true when the data is to be written into the Memory Information Register.
MSOR . . F.	M SOURCE is true if the M Register is the source register for a 1C, 2C or 8C micro (literal).
MSTARTK.	MEMORY START is a flip-flop which is set for 250 nsec to start the memory logic timing for a memory cycle.
MSTARTFO	MEMORY START is true to set the Memory Start Flip-Flop and is produced as a result of micro decoding and timing.
MTR . . . F.	MAINTENANCE TEST is true if the mode switch on the console is in the Tape Mode.
MTR . . /F.	MAINTENANCE TEST NOT is true if the mode switch on the console is either in the Run or Step Mode.
MTRFINF.	MAINTENANCE TEST FINISH insures that the M Register cannot be designated as a sink in the MTR MODE or actually the mode is TAPE.
MX-MIRFO	MAIN EXHCHANGE REPLACED BY MEMORY INFORMATION.
M3MOD1H1	MODULE 3 MODIFIED ADDRESS is true to gate the modified address to module 3.
M4M5/.D.	MICRO OPERATOR BIT FOUR OR FIVE is false.
M-MLMXF.	M REGISTER REPLACED BY MEMORY LATCH DATA.
M-ML+UFO	M REGISTER REPLACED BY MEMORY LATCHES OR U REGISTER DATA.
M-SWI . F.	M REGISTER REPLACED BY SWITCHES with the load button depressed in the Halt Mode and M Register selected.
M-U . . . F.	M REGISTER REPLACED BY U REGISTER DATA IN THE MTR/TAPE MODE.
NOOP1 . F.	NO-OPERATION is true if the micro is not a skip or branch micro.
NORMALD.	NORMAL is a gating term developed for the producing of Source and Sink enable terms for register move type micros.
PADDn . D.	PAD ADDRESS where n=0 through 3 is a part of the addressing for Local Memory, Scratchpad portion.
PAREDETKO	PARITY ERROR DETECT is true if a parity error occurs for a memory read operation. PARDETKO is used to set the parity error indicator, CD3.
PC0n . . J1	PARITY CHECK "N" is true for the memory modules 0 through 3, that have good parity (odd).
PELAMPF.	PARITY ERROR LAMP as a result of a micro fetch parity error is sent to the halt logic to cause the machine to halt on a parity error.
PEMFETF.	PARITY ERROR "M" FETCH at SO time of the sequencer to true to cause the processor to halt on a parity error during an M FETCH.
PEMFETKO	PARITY ERROR M FETCH is true if a parity error occurs for an M FETCH.
PE1 . . . E.	PARITY ERROR ONE is set if a parity error is detected on the 10 bits assembled in U Register Lower during a Cassette read operation.
PE2 . . . E.	PARITY ERROR TWO is set if a parity error is detected on bytes 0 or 2 read from the cassette.
PE3 . . . E.	PARITY ERROR THREE is true if a parity error is detected on either bytes 0 and 1 or bytes 2 and 3 which means the parity error is non-recoverable.
PMOnA . K.	PARITY MANIPULATE "N" is true if good parity was detected during the read data portion of a memory cycle or if a data field length of twenty-five is indicated. n=0 thru 3.
PRECH . KO	PRECHARGE is one of the three basic signals sent to memory for memory read/write operations and is produced by the memory timing logic on card K.

PWRON . SO	POWER ON FROM SUPPLY is a level from the power supplies which is used to generate a processor clear on power up.
P4.75V . 0	POWER 4.75 VOLTS
RCLEBLCO	ROTATION CONTROL ENABLE is true as a result of gating for micros which require use of the rotator.
RCLTnnK.	ROTATION CONTROL where nn=01, 02, 04, 08 and 16 are a result of the data field length for the particular operation and are derived from the terms LITn . . . C.
RD+WR . FO	READ OR WRITE is true for a memory read/write operation from the console.
RD/WT . KO	READ/WRITE is the level sent to memory and will be false for a read and true for write enable.
READ . . F.	READ is true if the memory operation from the console is a read.
REGCLKK.	REAL TIME GENERATE CLOCK is true for 250 nsec of each input cycle and used for the generation of the Real Time Clock.
REPEATF1	REPEAT FLIP-FLOP is set for generally long micros and prevents the new micro from being placed in the M REGISTER even though a finish pulse may occur.
REWINDE.	REWIND is true if the rewind button is depressed for a cassette rewind and provided forward drive has been removed.
RFACLRH.	REFRESH ADDRESS CLEAR is true when the five bit Refresh Address Counter has reached a maximum count and another refresh is granted.
RFACRYH.	REFRESH ADDRESS CARRY is the carry out from the lower stage of the Refresh Address Counter to the upper stage.
RFAD . nH.	REFRESH ADDRESS where n=5 thru 9 to correspond with the address lines send to memory. RFAD . nH. is the output of the Refresh Address Counter on Card H.
RFG . . . CO	REFRESH GRANTED is true if a refresh of memory is to occur and is used to set the Granted Refresh Flip-Flop and also used to cause the Address Distribution Logic to send the Refresh Address to the memory modules.
RFMV1 . J1	REFRESH MULTIBRATOR is used to request a refresh cycle approximately every 62 micro seconds.
RGRPn . T1	REGISTER GROUP "N" (n=1,2,4,8) is used as a co-ordinate for selection of the registers.
RSELn.T1	REGISTER SELECT "N" (n=1 or 2) is used as a second co-ordinate for selection of registers.
RSFETCF.	RESET FETCH FLIP-FLOP is used to reset MFETCHFO for micros which require more than two clock periods.
RTCLOCKO	REAL TIME CLOCK is the output of the Real Time Clock Generator and is true for 250 nano seconds at a frequency of once per 100 milli-seconds.
RUNHLDF.	RUN/HOLD is true if the processor is running and the HOLD ./FO is true as a result of the U Register being full. RUNHLDF. is used to reset the HOLD ./FO flip-flop when finish occurs in the MTR (TAPE) Mode.
RUNS . . FO	RUN FLIP-FLOP is set if the Start Button on the console is depressed.
RUN . . . F1	RUN is true if the mode switch on the console is positioned in the RUN MODE.
RUNMODCO	RUN MODE is true if the mode switch on the console is positioned in the RUN MODE.
RWD . . . T1	REWIND is sent to the cassette in order to cause a rewind to BOT (Beginning of Tape).
RWnn . . J1	READ/WRITE "nn" are the thirty-two outputs of the rotator where nn=00 through 31. Rotator located on Card J.
SCPMY/F.	SYSTEM CLOCK PULSE NOT is an inverted 4MHZ clock.
SCPM4 . C.	SYSTEM CLOCK is a 4MHZ clock.
SCPM8 . F.	SYSTEM CLOCK PULSE 8 is an 8MHZ clock.
SCPM . . E.	SYSTEM CLOCK PULSE CARD E is a 4 MHZ clock.
SECONDF.	SECOND is true for long micros and is true to cause the sequencer to make a second count to obtain counts S4 thru S7.
SECSEQF.	SECOND SEQUENCE is generated at S3 time of the sequencer to produce SECONDF.
SETHLTF.	SET HALT FLIP-FLOP is a gated term which reset the RUNS . . FO Flip-Flop to halt the processor.
SETRUNF.	SET RUN FLIP-FLOP is a gated term as a result of the Start Button being depressed to set RUNS . . FO.
SETUF2E.	SET "U" FULL TWO is true for the second sixteen bits accumulated in the U Register and will cause the term UFULL to be generated.
SEQRSTF1	SEQUENCER RESET is true to reset the sequencer as a result of a finished micro.
SICOLnD.	SINK COLUMN "N" where n=0 or 1 is true if the micro being executed is selecting column 0 or 1 as the sink register. (4 bit registers)

SIMIC . F.	SEQUENCER ONE MICROS is true at S1 time of the sequencer if the micro is not a 3F or 7D. SIMIC . F. is used to produce a finish pulse.
SINKEND1	SINK ENABLE is true to allow the logic to gate data to local memory.
SITASnD.	SINK TAS "N" is true to produce local memory addressing to write into the TAS Register of local memory. n=1 or 2.
SKADn . D.	SINK ADDRESS where n=0 through 3 is a portion of local memory addressing for sinking data into the TAS Register in local memory.
SKIP . . CO	SKIP is true to cause the next micro to be skipped if the 6C or 3E micro skip conditions are met.
SKIP . . F.	SKIP is true if a micro is to be skipped and its function is to prevent transferring the next micro into the M Register and this forcing a NO-Operation micro in place of the next micro which would be normally executed.
SNGMODCO	SINGLE MODE is true if the MODE Switch on the console is in the STEP position.
SNKTASD.	SINK TOP OF A STACK is true if TAS is designated as a source or destination for a register move type micro.
SOCOLnD.	SOURCE COLUMN is true if the register address for the source register corresponds to the column number where n=1 or 2.
SORENBD.	SOURCE ENABLE is true to allow selection of a register as source for a register move type micro.
SOTAS . D.	SOURCE TOP OF A STACK is true if the A Stack is selected as a source.
SOTAS . F.	SOURCE TOP OF A STACK is true to decrement the Stack Pointer if the A STACK is selected as a source.
SRO . . . E.	SENSE REG. OUT is true each time the leading one bit of the 10 bit character from cassette is detected assembled in U Register Lower.
SRPE-OE.	SHIFT REGISTER/PARITY ERROR REPLACED BY ZERO is true to clear U Register Lower and PE1 prior to a character being assembled from the Cassette.
SRO*T3E.	SHIFT REGISTER OUT AND TIME 3 is true for each character which is assembled in U LOWER and is used to count the Byte Counter.
START . CO	START is produced as a result of the Start button on the console being depressed.
STFETCF.	SET FETCH is true to cause the M Fetch Flip-Flop (MFETCHFO) to set.
STKADOFn	STACK ADDRESS is the output of the Stack Pointer for addressing the A Stack words located within Local Memory, n=0 through 3.
STPAGPE.	STOP AT GAP is true to cause the cassette to stop at the next gap as a result of a 3E Cassette Control micro.
STP/ . . E.	STOP NOT is true to allow serial data from the tape to be accumulated (Cassette).
STRTO . E.	START TAPE RESET is true for a general processor clear or when tape is initially started to clear miscellaneous cassette logic and produce STP/ . . E. to allow cassette data to be accumulated.
STRTRWE.	START REWIND is true to hold the rewind button output for a cassette rewind operation.
STRT . . E.	START is true as a part of the sequence to apply forward drive for a cassette operation.
STRUN.F.	SET RUN is true when the start button is depressed and its function is to set the M Fetch Flip-Flop to fetch the first micro from memory.
SUBTR . F.	SUBTRACT is true to place MAR(A) in the subtract mode for branching relative in a negative direction.
SUB . . . DO	SUBTRACT is true to place the Arithmetic Unit of the 24 Bit Function Box in the subtract mode.
SWISELF.	SWITCH SET LOAD is true if the Load Button is depressed or if the Rotary Switch is in the Write position and the Read/Write Button is depressed.
SWRITEFO	SET WRITE is true if the memory operation is a write. SWRITEFO is used to extend the duration of Chip Enable and also to send the write level to memory.
SY5CL1K.	SYSTEM CLOCK is the output of the Video Amplifier from the 8 MHZ crystal which produces the system basic clock.
Sn . . . . D.	SEQUENCER OUT on Card D where n=1 through 7.
Sn . . . . F.	SEQUENCER OUT on Card F where n=1 through 5.
S14BENDO	SOURCE BIT ENABLE is true to allow data on Card A to be gated to the 4 bit bus (4BTBOnAO).
S14BMnDO	SOURCE BIT MODE where n=0-2 is the addressing for the multiplexor to gate data to the 4 bit bus on Card A.
S24BENDO	SOURCE BIT ENABLE is true to allow ADATA on CARD B to be gated to the 4 bit bus (4BTOnBO).
S24BMnDO	SOURCE BIT MODE where n=0-2 is the addressing for the multiplexor to gate data to the 4 bit bus on Card B.

TASNK . D1	Tas Sink is true when the Micro decoding logic has determined that tas has been designated as the sink register.
TA F1	Time "A" is the first sequencial output of the sequencer used to control when FINISHDO occurs.
TB F0	Time "B" is the second sequencial output of the sequencer used to control when FINISHDO occurs.
TC F1	Time "C" is the third sequencial output of the sequencer used to control when FINISHDO occurs.
TC/ . . . F1	Time C Not is used to set TA . . . . F1 when TD/ . . . F1 is also true.
TD F0	Time "D" is the fourth sequencial output of the sequencer used to control when FINISHDO occurs.
TD/ . . . F1	Time D Not is used to set TA . . . F1 when TC/ . . . F1 is also true.
TPCLKIE.	Tape Closk In is true for one to many clock periods depending on whether or not a serial data bit is received from the Cassette Tape during the time the Tape Clock Pulse from the Cassette is true. It is used to trigger the sequencing of shifting the serial data from the Cassette's Tape into the U-Register (Lower).
TPCLK . E.	Tape Clock is the CTL converted tape clock pulse received from the Cassette Tape. It is true for approximately 106 usec and false for 19 usec, occurring at a frequency of 8 KHz for the length of a record previously written on tape.
TPRDY . E.	Tape Ready when true indicates the Cassette Tape unit is ready. It's used to enable sending Forward Drive level to the Cassette.
TRIL/ . . 1	Tape Read Information Level is the DTL serial data bit received in the Processor (Card E) from the Cassette's logic. It is true for approximately .5us when a serial data bit is transferred.
TRUE01A.	True is the output of an inverter assumed to be a constant CTL true voltage level. Card A. (Input open)
TRUE . . K.	True is the output of an inverter assumed to be a constant CTL true voltage level. Card K. (Input open)
TRUE01D.	True is the output of an inverter assumed to be a constant CTL true voltage level. Card D. (Input open)
TRUE1 . E.	True is the output of an inverter with an open input, assumed to be a constant CTL true level. Card E.
TRUE4 . J.	True is the output of an inverter with an open input, assumed to be a constant true CTL voltage level. Card J.
TRUE03A.	True is the output of an inverter with an open input assumed to be a constant true CTL voltage level. Card A.
TRU60HK.	True 60 Hz is true during the positive half cycle of the 60 Hz input used for the Real Time Clock circuitry.
TRWP/ . E1	Tape Rewind Pulse is the DTL converted level sent to the Cassette to initiate a rewind of tape.
TWS . . . H1	Transfer Width Sign when true indicates the field direction is negative. When false, a positive field direction is indicated.
TO . . . . E.	Time O is true for one clock period immediately after Tape Clock In (TPCLKIE.) is true. It's used to sequence the assembly of serial data from the Cassette.
T0-7 . . F1	Time 0 thru 7 indicates the time the Sequencer is effectively in the "first sequence". It is true for the entire execution of those Micros which require 4 or fewer clock periods to Finish. Certain Micros requiring more than 4 clock periods to finish may also find the level true for the entire time.
T0T1T2D.	Time "0", Time "1", Time "2", is true when the Sequencer is in its first three clock periods (8MHz clock). Card D.
T0T1T2F.	Same as above except the decoding is on Card F.
T1 . . . . E.	Time 1 is true for one clock period immediately following T0 . . . . E.. It's used to sequence the assembly of serial data from the Cassette.
T11 . . . F.	Time "11" is true when the Sequencer is at its 12th clock period (8 MHz clock). This is also the 4th clock period of the second sequence which is entered for the execution of "longer" Micros. Card F.
T12T14F.	Time "12 thru 14" is true when the Sequencer is in its 13th thru 15th clock periods (8MHz clock). This is also the 5th thru 7th clock periods of the second sequence which is entered for the execution of "longer" Micros. Card F.
T13 . . . F.	Time "13" is true when the Sequencer is at its 14th clock period (8 MHz clock). This is also the 6th clock period of the second sequence which is entered for the execution of "longer" Micros. Card F.
T15 . . . F.	Time "15" is true when the Sequencer is at its 16th clock period, (8 MHz clock). This is also the 8th clock period of the second sequence used for longer Micros. T15 . . . F. is the maximum "count" to which the Sequencer can be incremented. The next clock will cause T0 . . . . n. to be true. Card F.
T2 . . . . E.	Time "2" is true for one clock period during the assembling of each serial data bit from Cassette Tape. When it occurs it is dependent on the time duration of the Tape Clock Pulse. Card E.
T3 . . . . E.	Time "3" is true for one clock period immediately following T2 . . . . E. . It's used to sequence the serial data assembly in the U-Register of the data from the Cassette. Card E.

T3 . . . . D.	Time 3 is true when the Sequencer is in its 4th clock period (8 MHz clock). It is only true during the first sequence of the Sequencer. Card D.
T3 . . . . F.	Time 3 is the same as T3 . . . . D. except the level is decoded on Card F.
T4T5T6F.	Time 4, Time 5, Time 6 is true when the Sequencer is in either its 5th, 6th, or 7th clock period (8 MHz clock). It is true only during the first sequence providing the Sequencer is not reset after (T3) time. Card F.
T4T5T6D.	Time 4, 5, & 6 is the same as T4T5T6F. except that the decoding is done on Card D.
T7 . . . . D.	Time 7 is true when the Sequencer is in its 8th clock period (8 MHz clock). Time 7 is the highest "time" possible for the first sequence. The next time will be either Time 0 of the first sequence or Time 8 which is effectively the 1st clock period of the second sequence. The decoding is on Card D.
T7 . . . . F.	Time 7 is the same as T7 . . . . D. except that the decoding is done on Card F.
T8-15 . F0	Time 8 thru 15 when true indicates the Sequencer is in the second sequence which is entered for the execution of some of the longer Micros. When T8-15.F0 is true, levels T8 thru 15. . . . a. or combinations of the same will be true. Card F.
T8910 . F1	Time 8, 9 & 10 is true when the Sequencer is in either its 9th, 10th, or 11th clock period (8 MHz clock). This time is defined as the first three clock periods of the second sequence. Card F.
T9 . . . . D.	Time 9 is true when the Sequencer is in its 10th clock period (8 MHz clock). This is also the 2nd clock period of the second sequence at which time T8-15 . F0 is true. The level is decoded on Card D.
T9 . . . . F.	Time 9 is the same as T9 . . . . D. except that the decoding is done on Card F.
UDSET . E.	U REGISTER "D" SET is true to allow the transfer of U LOWER to U UPPER.
UFULL . E.	U REGISTER FULL is true if both U Register Upper and Lower are full.
UFULL1E.	U REGISTER FULL ONE is true with UFULL.E. true and a clock.
UFULL . E0	U REGISTER FULL is true for 250 nano seconds as a result of UFULL1E. setting.
ULSET . E.	U LOWER SET is true to transfer the contents of U Lower to U Upper.
UMSB-OE.	U REGISTER TO M REGISTER SET BUS is true to allow readout of U Upper and to transfer the entire U Register to the input of the M Register.
URDnn . F.	U REGISTER DATA is the output of the U Register where nn=00 thru 15.
USOR . . F.	U REGISTER SOURCE is true if the U Register is selected as a source for a Register Move micro.
WAIT . . F.	WAIT indicates a 24 Bit Literal has been read from the cassette in the Tape Mode therefore another 16 bits from tape must be accumulated before the micro can be executed.
WAIT . FF.	WAIT indicates a micro has been read from the cassette and executed.
WRITE . F.	WRITE is true if a memory write from the console is being performed.
Wnn . . . K0	DATA OUTPUT of the Memory Information Register where nn=00 thru 07. (8 of 32 bits).
WnnXnnK0	DATA OUTPUT of the Memory Information Register (24 of 32 bits). The first nn=08 thru 31 to correspond with the Read/Write Data Levels. The second nn=23 thru 0 to correspond with the Main Exchange data positions. Ex. W08X23K0.
XANY . . D.	X AND Y is the logical "and" of the X and Y Registers produced by the 24 Bit Function Box.
XEOY . . D.	X EXCLUSIVE OR Y is the logical exclusive or of the X and Y Registers.
XY . AB . D.	X REGISTER DATA/Y REGISTER DATA/A DATA/B DATA is the data to the multiplexors which feed the Main Exchange and data is dependent upon the Local Memory data which has been addressed by the operation.
01C . . . D.	1C Micro decoded on Card D.
01C . . . F.	1C Micro decoded on Card F.
02C . . . D.	2C Micro decoded on Card D.
02F . . . D.	The MF portion of a Micro (MOP bits 3 thru 0) are set to 2 (0010). Card D.
03D . . . F1	The MD portion of a Micro (MOP bits 11 thru 8) are set to 3 (0011). Card F.
04C . . . F.	4C Micro decoded on Card F.
04D . . . F1	The MD portion of a Micro (MOP bits 11 thru 8) are set to 4 (0100). Card F.
05C . . . F.	5C Micro decoded on Card F.
05D . . . F1	The MD portion of a Micro (MOP bits 11 thru 8) are set to 5 (0101). Card F.

05F . . . D1	The MF portion of a Micro (MOP bits 3 thru 0) are set to 5 (0101). Card D.
07C . . . C.	7C Micro decoded on Card C.
07C . . . D.	7C Micro decoded on Card D.
07C . . 1F.	7C Micro decoded on Card F.
07C . . . F.	7C Micro decoded on Card F.
08C . . . D0	8C Micro decoded on Card D.
08C . . . F.	8C Micro decoded on Card F.
08D . . . F1	The MD portion of a Micro (MOP bits 11 thru 8) are set to 8 (1000). Card F.
09C . . . D.	9C Micro decoded on Card D.
09C . . . F.	9C Micro decoded on Card F.
09C/ . . F.	The 9C Micro has not been decoded. Card F inversion of 09C . . . F.
1CCLO . D.	1C Micro and the Sink Register Select is 0. Card D.
1EA . . . F1	MOP bit 5 is true and MOP bit 4 is false. Card F.
1+3ETIE.	1 or 3 Error Tape is true when a non recoverable tape parity error has been detected on the serial data read from Cassette Tape. When the level is true, further assembling of serial data from tape is disabled and the Processor is halted when the next FINISHDO occurs providing JUMP/.F. and REPEA/F. are true.
10C . . . C.	10C Micro decoded on Card C.
10C . . . D.	10C Micro decoded on Card D.
10C . . . F.	10C Micro decoded on Card F.
11C . . . F.	11C Micro decoded on Card F.
11D . . . F1	The MD portion of Micro (MOP bits 11 thru 08) are set to 11 (1011). Card F.
11F . . . D.	The MF portion of a Micro (MOP bits 03 thru 00) are set to 11 (1011). Card F.
12BTBRF.	12 Bit Branch is true when either the 123C or 145C Micro has been decoded on Card F.
1236C . D.	3C or 6C Micro decoded or the 1C or 2C Micro and the U-Register is not the source. Card D.
15D . . . C.	The MD portion of a Micro (MOP bits 11 thru 08) are set to 15 (1111). Card C.
16BSNKD.	16 Bit Sink is true when either the 1C, 8C, or 9C Micro has been decoded with the FL-Register selected as sink.
2EA . . . D.	MOP bit 5 is true and MOP bit 4 is false. Card D.
2EA . . . F.	MOP bit 5 is true and MOP bit 4 is false. Card F.
2EB . . . D.	MOP bit 07 is true and MOP bit 06 is false. Card D.
2SNK . . D1	8C or 9C Micro decoded on Card D. 2C or 10C Micro decoded on Card D with Register replaced by Pad if the 2C and the sink register selected is 2 for either the 2C or 10C Micro, also Card D.
2EB . . 2F.	MOP bit 07 is true and MOP bit 06 is false.
210C . . D.	2C Micro (Register replaced by Pad) and register selected is 2 decoded on Card D, or the 10C Micro and the register selected is 2 also decoded on Card D.
21CM5/F.	1C Micro or the 2C Micro (Pad replaced by Register) decoded on Card F.
24BSNKD.	24 Bit Sink is true when the 1C, 8C, or 9C Micro has been decoded with either the X, T, L, FA, or FB Register selected as sink. Card D.
24LMTRF.	24 Bit Literal "MTR" is true when either the 1C or 2C Micro has been decoded and the U-Register is source and TAPEFWF. is Ture, or the 9C Micro has been decoded and the U-Register is Full (UFULL . E0). Card D.
24LRUNF.	24 Bit Literal "RUN" is true when the 9C Micro has been decoded and either Run or Step Mode is true.
24 . 4 . . D.	Register Move with a 24 bit source register being move to a 4 bit destination.
24X24 . F0	True if the rotation is a processor operation for the 10C, 11C, 4D, 5D and 3F micros.
24X32 . F0	True for a memory write operation.
3CAND . D.	3C micro with the "AND" variant decoded.
3CDECTD.	3C micro with the Decrement and Test variant decoded.
3CDEC . D.	3C micro with the Decrement variant decoded.
3CEOR.D.	3C micro with the Exclusive Or variant decoded.
3CINCTD.	3C micro with the Increment and Test variant decoded.
3CINC . D.	3C micro with the Increment variant decoded.

3COR . . D.	3C micro with the OR variant decoded.
3CSET . D.	3C with the SET variant decoded.
3CSKIPBO	3C SKIP is true if the micro is a 3C with a test and the test condition is met to cause a skip of the next micro.
3EA . . . F1	True if the M Register bits 4 and 5 are set.
3EB . . . D1	True if the M Register bits 6 and 7 are set.
32X24 . FO	True for a memory read operation.
4BCAR3B.	4 Bit Binary Carry is the output of the most significant stage of the adder/subtracter in the 4 Bit Function Box which is used for the 3C Increment or Decrement function.
4BCNENDO	4 BIT CONTROL ENABLE is true to enable the multiplexors on Card B to gate data from the 3C micro, MIR data and 4 bit register data to the 4 bit bus (4BITnnBO).
4BCNMnDO	4 BIT CONTROL MODE "N" is the addressing for the multiplexors on Card B where n=0 thru 2.
4BSUMnB.	4 BIT BINARY SUM is the output of the 4 bit adder subtractor of the 4 Bit Function Box.
4BITBRF.	4 BIT BRANCH is true for a 4C or 5C micro.
4BITOnBO	4 BIT BUS is the output of the 4 Bit Function Box where n=0 through 3.
4BITn . D.	4 BIT is used for multiplexor addressing enable for register move operations where a 4 bit register is either source or sink. n=1 or 2.
4BTBOnaO	4 BIT AUXILIARY BUS is the input to the 4 Bit Function Box where n=0 through 3 and a=Card A, Card B, Card F or backplane "or'. 4BTBOnTO.
4BTSUBDO	4 BIT SUBTRACT is true to place the adder/subtractor in the 4 Bit Function Box in the subtract mode.
4C5CBRF.	4C or 5C BRANCH is true for a 4C or 5C micro and the branch condition is met.
5CBRCHF.	5C BRANCH is true if the micro is a 5C and the branching condition is true.
6CSKIPC.	6C SKIP is true if the micro is a 6C Skip When and the skipping condition is true.
60HRETKO	60 HERTZ RETURN is an input to the Real Time Clock Logic from the basic 60HZ input.
60HZINKO	60 HERTZ IN is an input to the Real Time Clock Logic from the basic 60 HZ input.
7CREADF.	7C READ is true if the micro is a 7C with the Read variant set.
7CWRITF.	7C WRITE is true if the micro is a 7C with the Write variant set.
9C . . . . F.	9C micro decoded in the M Register.
nCMP . . C.	"N" COMPLEMENT where n=1 thru 4 are used to produce the twenty-four's complement of the literal for generation of Mask and Rotation Control for the 10C Shift T left, 5D SHIFT X*Y Left or 4D Shift X or Y.

B 1700

CENTRAL SYSTEM

SECTION

II

FUNCTIONAL
DETAIL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Printed in U.S. America 11-20-72

For Form 1053360.

INTRODUCTION

This section describes the B 1700 S-Memory Processor Console, including Cassette, System Clock, Real Time Clock, Sequencer, Control Logic, Micro Operators, Micro Operator Timing, 24 Bit Function Box, 4 Bit Function Box, Rotator and Mask Generator, Local Memory, Modes of Operation, and Data and Control Signals Transfer Paths.

CONSOLE SWITCHES–INDICATORS AND THEIR FUNCTIONS/OPERATION

The B 1700 Console contains the necessary controls and indicators for operation of the B 1700 System. The Console provides for Power On/Off, Mode Select, Register Load/Display and Cassette Controls. See Figure II-1. The actual Cassette is considered a portion of the Console and therefore the Cassette is described generally within this manual. For detailed operation and maintenance procedures for the Cassette refer to the Cassette Technical Manual.

Fig. II-1 B1700 CONSOLE

24 CONSOLE LAMPS

The 24 Console Lamps are used to display the contents of the 24 Bit Main Exchange. In the Halt Mode this display will be either the contents of a selected register or the contents of MIR. The Register Display is enabled by forcing a 1C Register Move in the Halt Mode using the register selected as the source and NULL as the destination. In the Run and Tape Mode the lamp display is dependent upon the micros being executed and the data. Data at this time is probably not discernable.

24 CONSOLE SWITCHES

The 24 Console Switches are used in the Halt Mode to enter data in a selected register or into an addressed memory

location. The data entry into a register occurs by forcing a 1C Register Move using NULL as the source (Console Switches) and the selected register as the destination during the time the Load Button is depressed. The data entry into memory occurs by forcing a 7C write using Null (console switches) as the source by depressing the Read/Write push-button with write selected on the register select switch.

REGISTER SELECT AND REGISTER GROUP SWITCHES

The Register Group Switch is the large rotary switch at the lower left corner of the console. The Register Group selects a co-ordinate to select four registers. The Register Select switch then selects one of the four and is located to the immediate right of the Register Group Switch.

MODE SWITCH

The Mode Switch places the processor in one of three modes either Step, Run or Tape. With the processor "halted" and the Mode Switch in the Step position, one micro will be executed by depressing Start and the machine returns to the halted state with the next micro to be executed in the M Register. If the Mode Switch is in the Run Mode, the processor will upon depression of the start button continuously execute micros until either the Halt Button has been depressed or the Halt Micro has been decoded in the M Register. In the Tape Mode, the processor will upon depression of the start button, start tape movement and execute micros on the tape. The machine is returned to the halted state by depression of Halt, detection of a Halt Micro, Tape Error or Cassette Stop Micro having been decoded. In all cases the Tape will not stop until the next gap is detected.

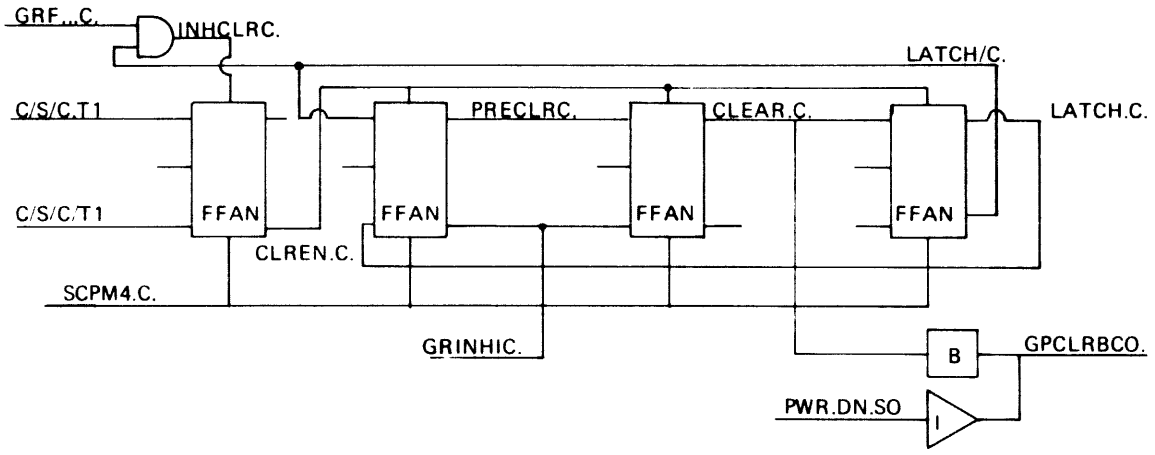


Fig. II-2 GENERAL PROCESSOR CLEAR

CLEAR PUSHBUTTON

The Clear Button generates the general clear (GPCLRBCO) which resets the system and clears the following registers in the processor: M, C, U, ML, MAR(A), MIR and the Stack Pointer. If a S-Memory refresh cycle has been granted then the clear operation is inhibited until the refresh cycle is complete. Figure II-2 is the logic on Card C for generation of the General Processor Clear.

Figure II-3 is a timing diagram showing the development of the CLEAR . C. term through depression of the Clear Button. Note that in this example a refresh cycle has been granted, therefore the clear operation is delayed until the refresh cycle is complete.

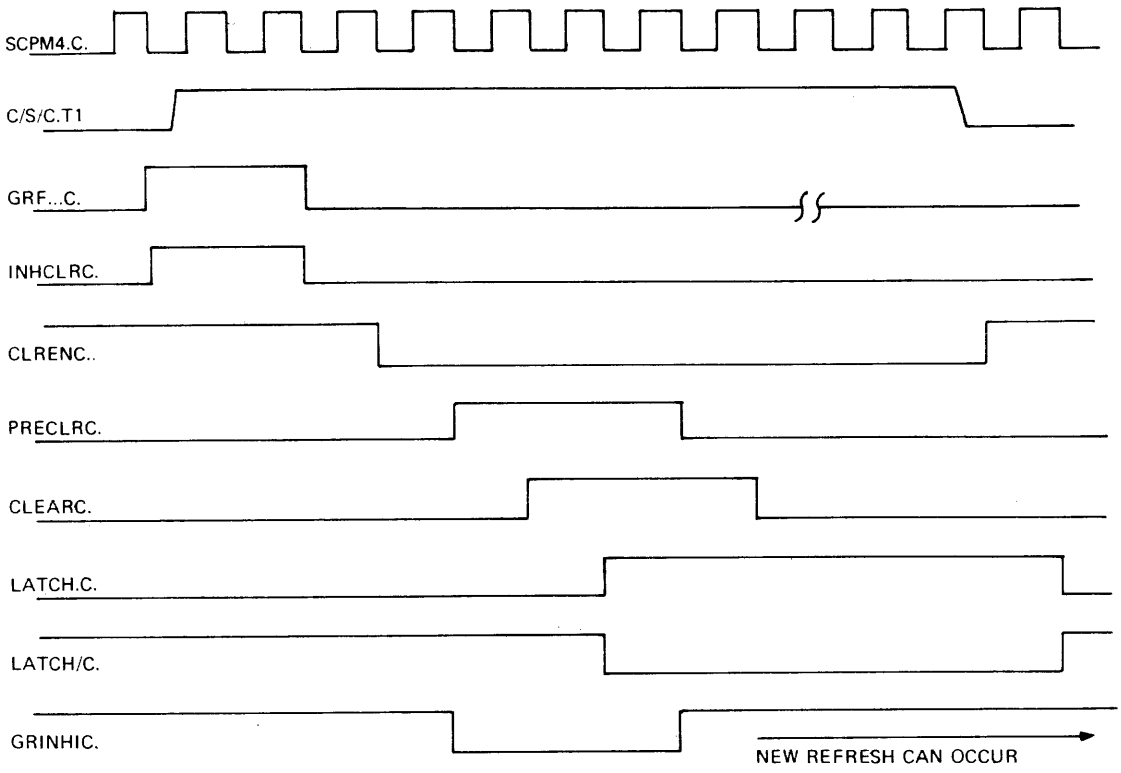


Fig. II-3 CLEAR TIMING (CARD C)

After the clear occurs, the Granted Refresh Inhibit (GRINHIC.) goes false and will allow a new refresh cycle to occur. During the period that C/S/C . T1 remains true, the LATCH . C. Flip-flop is set to prevent another clear from being produced thus only one clear pulse occurs for each depression of the button.

HALT PUSHBUTTON

The depression of the Halt Button will cause the Processor to halt at the completion of executing the micro following the current micro in the M Register. Before the halt occurs the next micro (micro following the last micro executed) will be fetched into M and the address will be upcounted to point at the next micro. Figure II-4 is the logic for generation of the halt term (HALT . . CO).

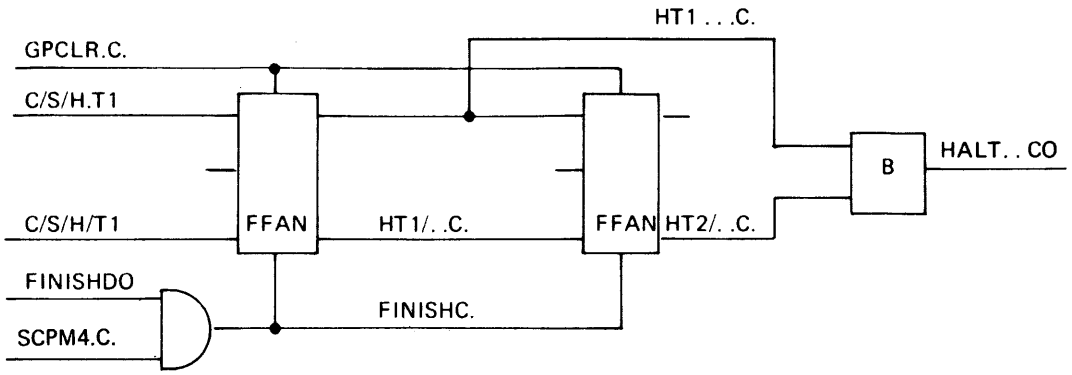


Fig. II-4 HALT LOGIC

Figure II-5 is the timing diagram for development of the HALT . . CO term. It should be noted that the machine halt is dependent upon FINISHDO which varies according to the micro being executed. For sake of simplicity assume that all micros being executed are two clock micros.

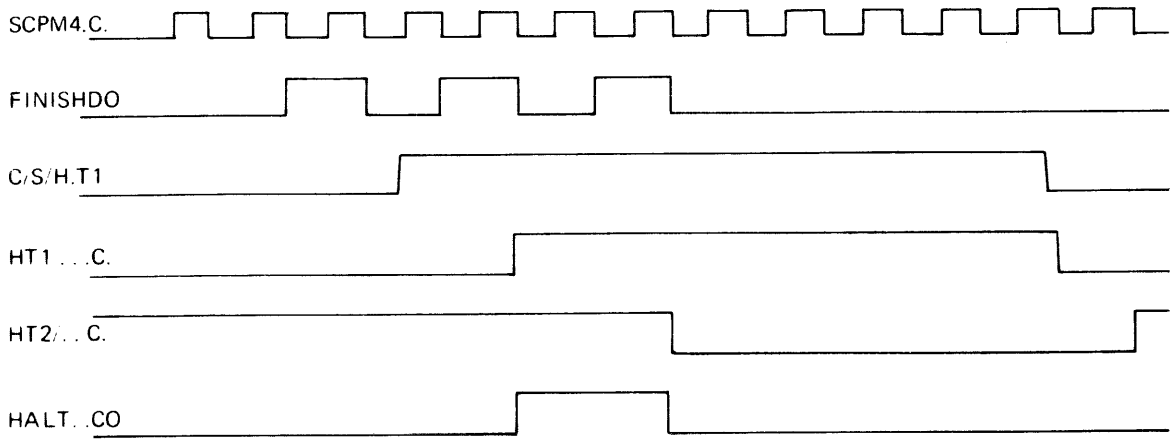


Fig. II-5 HALT TIMING

INT. SW. Then Disk Pwr. Then cons. Pwr. of

INTERRUPT SWITCH

The Interrupt Switch will cause the HALTI . CO flip-flop to set on Card C. The output term HALTI . CO is sent to the CC Register bit zero position and cause CC(0) to set. The HALTI . CO flip-flop is reset when the Interrupt Switch is returned to the off position.

INCREMENT A PUSHBUTTON

Depression of the Increment A Pushbutton will cause the address in MAR(A) to be upcounted by 16 bits or one micro word. This switch is generally used in conjunction with ready or writing S-Memory from the console. Figure II-6 shows the logic generation of the increment A term (INCA . . CO).

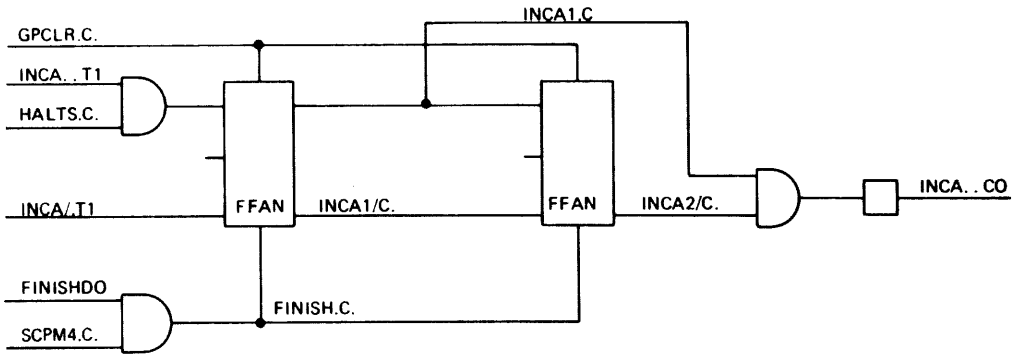


Fig. II-6 INCREMENT A LOGIC

As can be seen from Figure II-6 the machine must be in the halted state for operation of the Increment A Button. Note that the clock is FINISHC. which will normally occur every other 4MHZ clock period in the Halted State. The resultant output term INCA . . CO will be true for two-4MHZ clock periods (500 nsec).

START PUSHBUTTON

The Start Button is depressed normally to cause the machine to be placed in the Run State and thus cause an execution of a series of micro instructions. If the Mode Switch is in the Run Mode then the micros will be obtained from S-Memory or Cassette. If the Mode Switch is in Tape Mode then the micros will be obtained from the Cassette.

If the Mode switch is in the Step Mode then depression of Start will cause the execution of one micro and the machine will return to the Halt State. As can be seen from the logic for development of the start pulse (START . CO) (Figure II-7) the clocking term is FINISHC. and therefore the duration of START . CO will be for two-4MHZ clock periods (500 NSec).

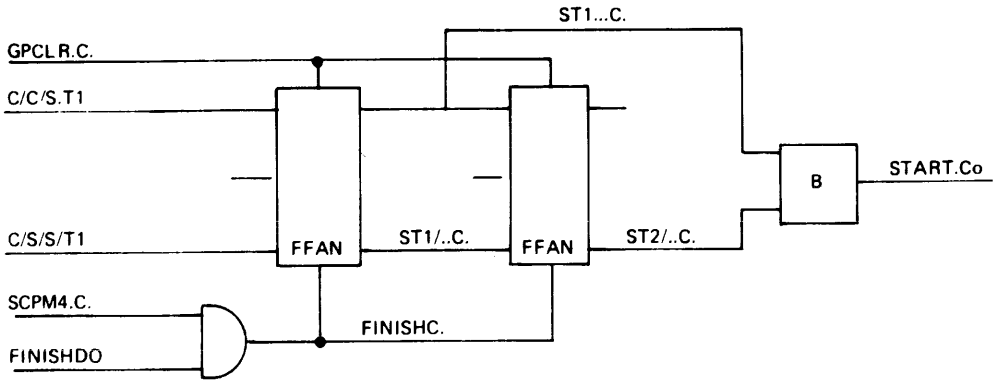


Fig. II-7 START PULSE LOGIC

READ-WRITE PUSHBUTTON

The Read-Write Pushbutton will produce a pulse to cause either a read or write of S-Memory depending upon the position of the Register Group Rotary Switch. If the switch is in the READ position then depression of Read/Write will cause a read of the location specified by the address previously load in MAR(A). The read data (24 bits) will be displayed in the Console Lamps. If the switch is in the WRITE position then the contents of the Console Switches will be written into the location specified by MAR(A). The machine must be in the halted state for these operations to occur. Figure II-8 shows development of the L/DTIMCO pulse (Load Timing); true for two-4MHZ clock periods.

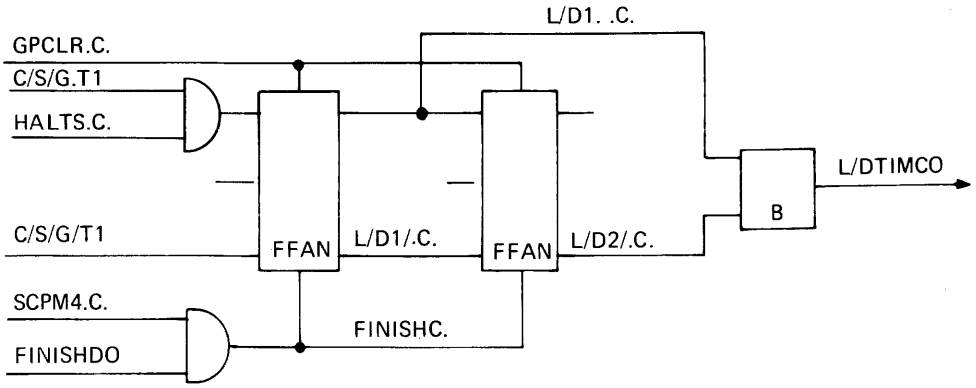


Fig. II-8 READ-WRITE INITIATION LOGIC

LOAD PUSHBUTTON

The Load Button is used for loading data in various registers from the Console Switches. The register to be loaded is placed in the Console Switches and by depressing the LOAD pushbutton, a 1C Move from NULL to the selected register is generated by the logic. Before depression of the Load Button, logic is generated to cause a 1C Move from the register to NULL which allows the contents of that register to be displayed. The LOAD . . CO pulse will be a pulse having a width of 500 nsec (Two-4MHZ Clocks). Figure II-9 is the logic generation of the LOAD . . CO pulse and Figure II-10 illustrates the timing for the execution of a 1C LOAD or display operation. The generation of the 1C Register Move micro logic for either a Display or Load of a selected register is shown in Figure II-11.

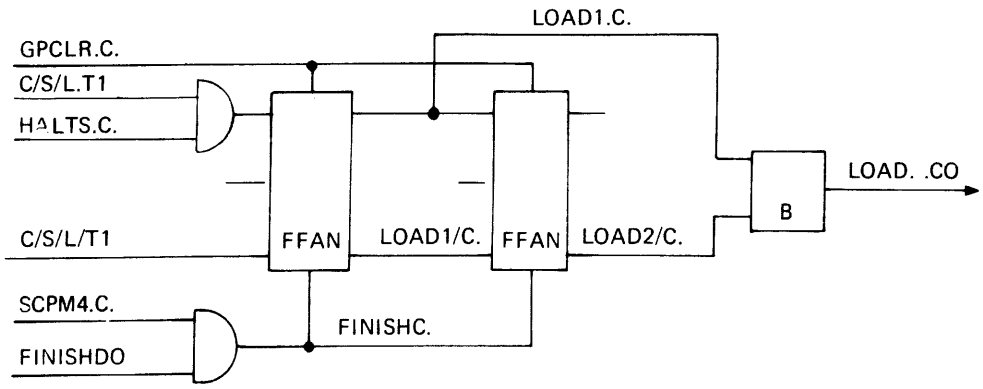
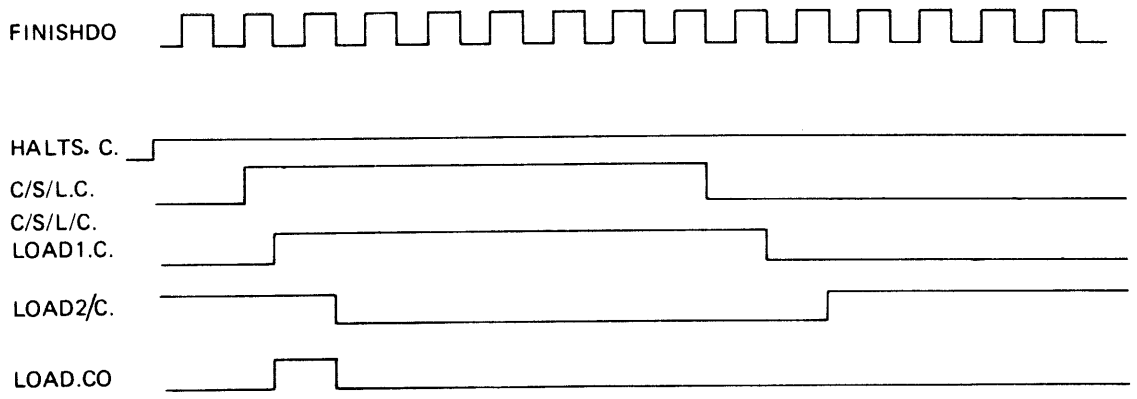
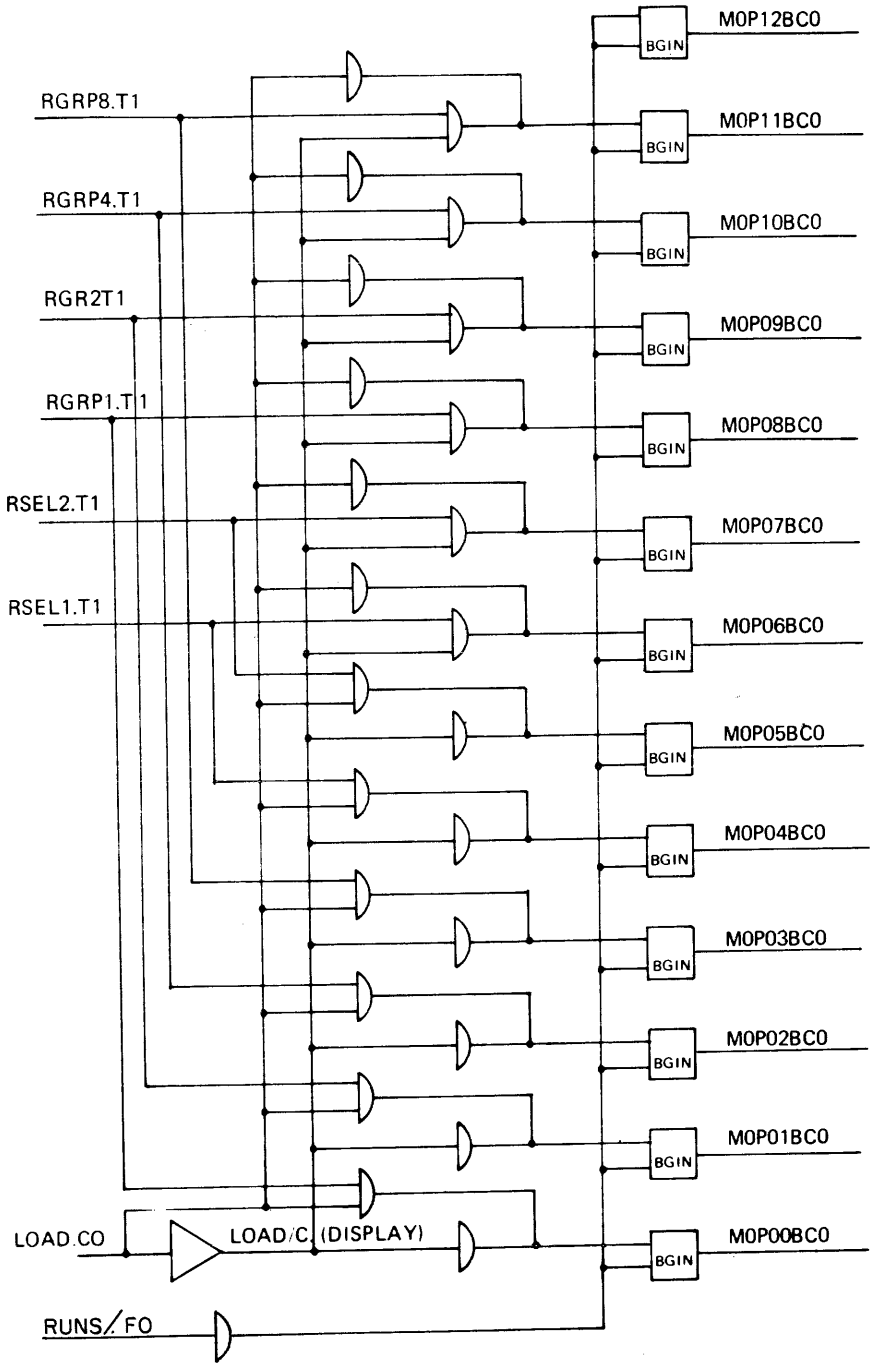


Fig. II-9 LOAD LOGIC



√ Fig. II-10



√ Fig. II-11 LOGIC TO LOAD OR DISPLAY REGISTERS

POWER ON/OFF SWITCH

Power ON/Off Switch is the switch for system power on or power off.

RUN INDICATOR

The Run Indicator when lit, indicates the machine is in the Run State and either executing micros from the Cassette Loader or from S-Memory.

CASSETTE ON/OFF

Cassette ON/Off is the power on/off for the Cassette Loader.

BOT INDICATOR

The Beginning of Tape Indicator is lit when tape in the Cassette Loader is at the beginning as detected by the Cassette. The BOT Level is sent from the Cassette Loader to the Cassette Control Logic on Card E of the processor.

REWIND SWITCH

The Rewind Switch when depressed will cause the tape in the Cassette Loader to return to the Beginning of Tape via a highspeed rewind and cause the BOT Indicator to illuminate.

TAPE PARITY INDICATOR

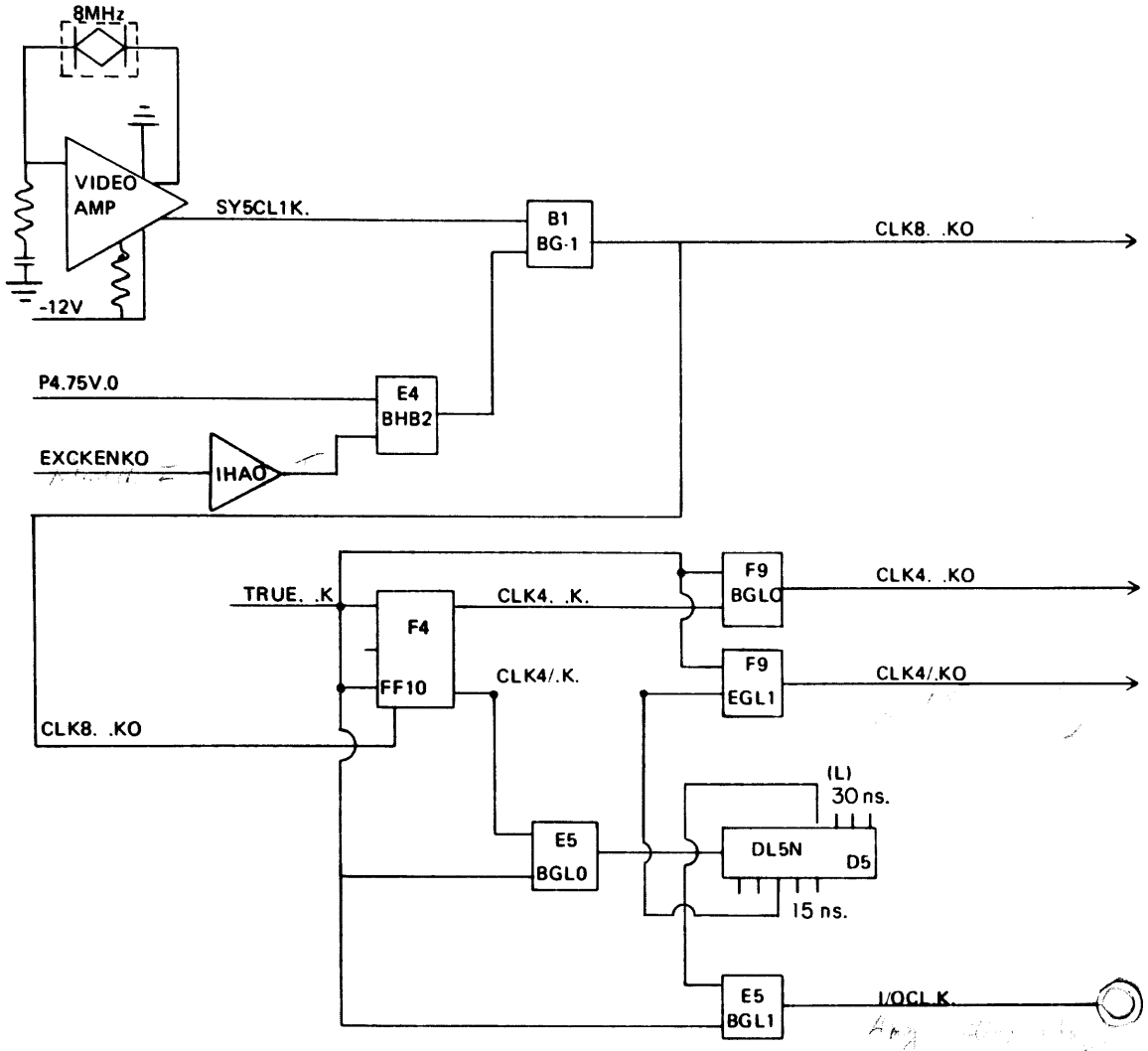
The Tape Parity Indicator illuminates when the parity detection logic on Card E detects a parity error of data on the Cassette Tape. Refer to Figure D-11 for details.

SYSTEM CLOCK

The B 1700 System Clock consists primarily of an 8 MHZ Crystal Controlled Oscillator, a video amplifier, associated gates, buffers, inverters, flip-flops, and delay lines. Refer to Section III for circuit details of the 8 HMZ Oscillator and Video Amplifier.

LOGIC OUTPUTS

The clock logic develops four clock outputs shown in Figure II-12. CLK8 . . KO, 8MHz; CLK4 . . KO, 4MHz; CLK4/ . KO, 4MHz inversion of CLK4 . . KO. The System Clock logic is located on Processor Card K (4-4).

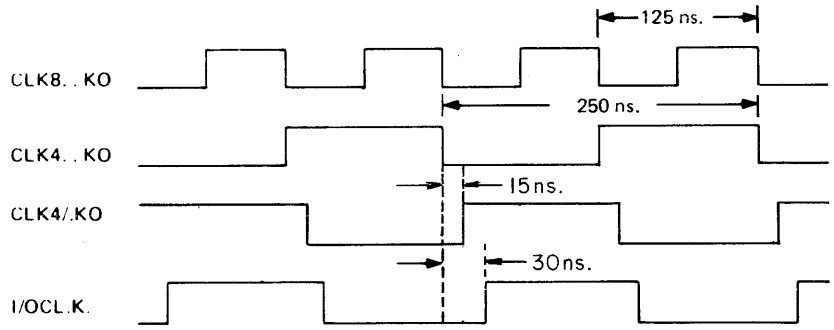


√ Fig. II-12 SYSTEM CLOCK

FUNCTIONAL DETAIL

During normal operation, buffer BHB2, located at E4, outputs a constant true. Buffer BG-1, located at B1, outputs a 8MHz pulse. EXCKENKO, normally false, provides the circuit with an external means of disabling the 8MHz output of buffer BG-1. ENCKENKO is used with the card tester. An external pulse generator may be applied to the backplane output of CLK8 . . KO when desired.

Assuming CLK8 . . KO is occuring at 8MHz, Figure II-13 illustrates the timing relationship of the four outputs developed by the system clock circuitry. The flip-flop (FF10), located at F4, will toggle with each CLK8 . . KO input applied thus generating outputs CLK4 . . KO and CLK4/.KO as shown. The I/OCL . K. output occurs 30 nsec after CLK4/.KO occurs. This delay is developed by the 50 nsec delay chip (DL5N) located at D5. Pin L (30 nsec tap) is used as shown.



√ Fig. II-13 SYSTEM CLOCK TIMING

DISTRIBUTION

CLK8 . . KO, CLK4 . . KO, and CLK4/.KO output Processor Card K via the backplane and are distributed to the various cards within the Processor as shown in Table II-1 (shown below). The I/O Clock, I/OCL . K., outputs card K via coaxial cable and is an input to the Distribution Card.

Card	A	B	C	D	E	F	H	J	K	Dist. Card
CLK8 . . KO	0	0	0	0	0	1	0	0	X	0
CLK4 . . KO	0	0	1	0	1	1	1	1	X	0
CLK4/ . KO	1	1	0	0	0	0	0	0	X	0
I/OCL . K.	0	0	0	0	0	0	0	0	X	1 Coax

Note: 1 indicates the clock is an input to the card
0 indicates the clock is not an input to the card.
X indicates card "K" (clock card).

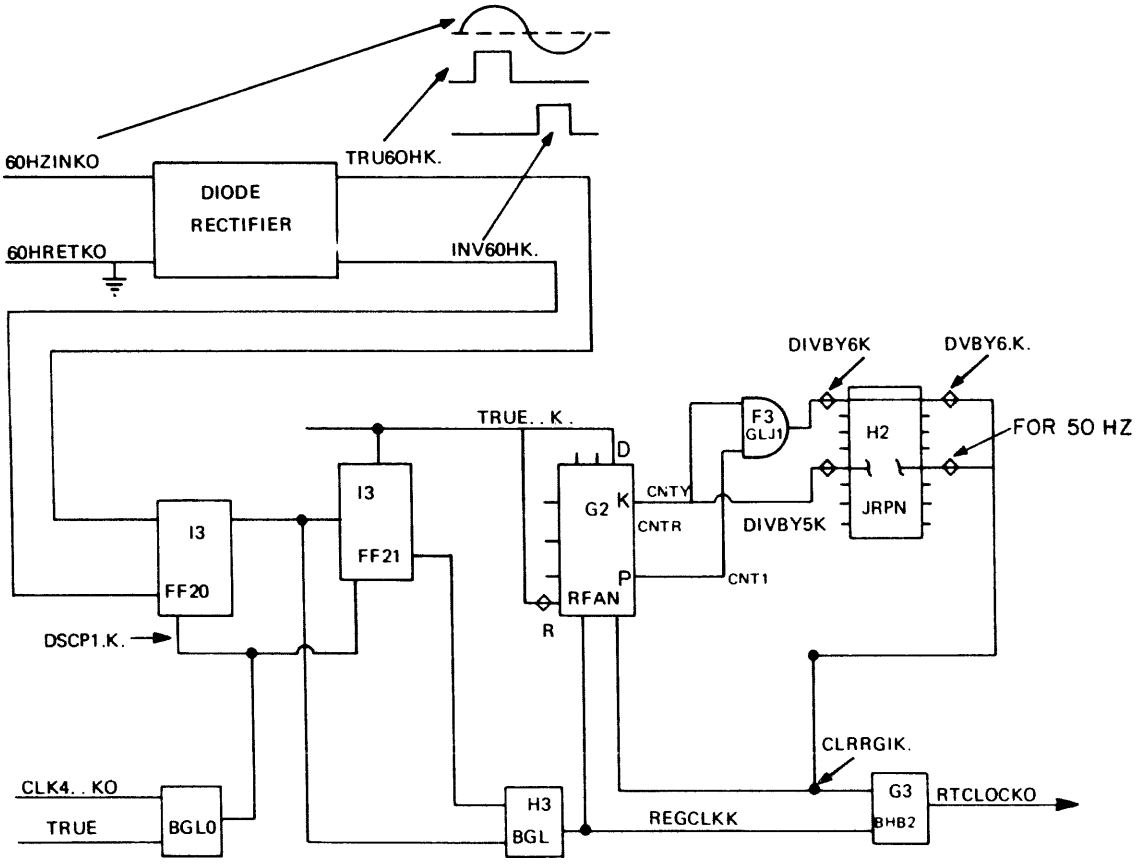
TABLE II-1
SYSTEM CLOCK DISTRIBUTION

REAL TIME CLOCK

The Real Time Clock Circuit is illustrated in Figure II-14. The circuit provides the system with a Real Time Clock pulse which occurs once every 100 msec. The function of the Real Time Clock pulse (RTCLOCKO) is to set the timer interrupt (CC-Register 2-bit position) every 100 msec. The Real Time Clock circuitry is located on Processor Card K (4-4). The CC Register 2 Bit Position (CC2 . . . F.) is located on Processor Card F(5-5).

FUNCTIONAL DETAIL (Refer to Figure II-14)

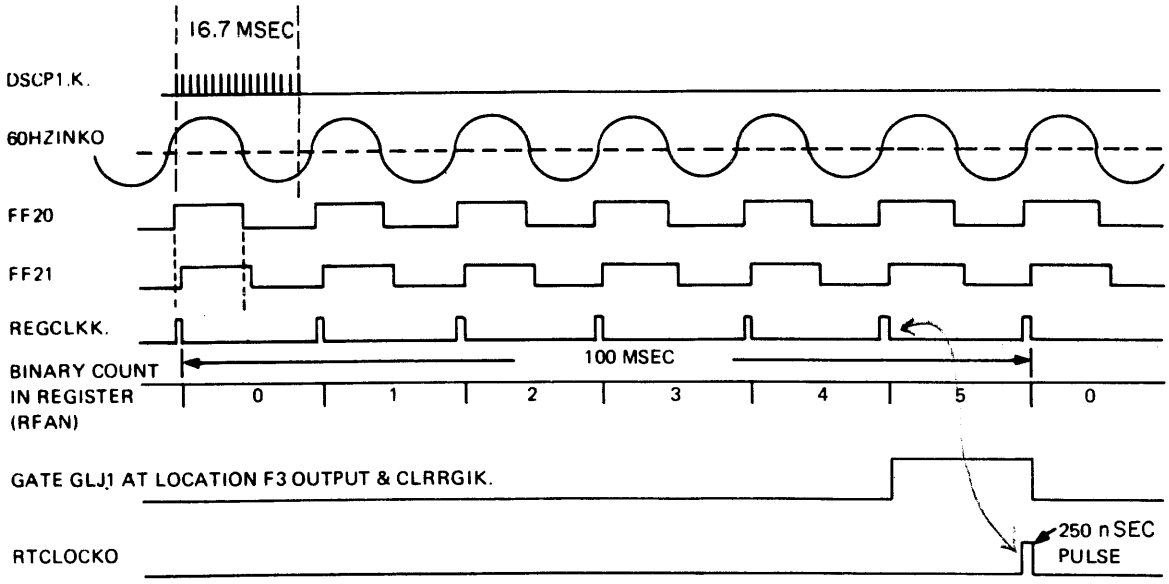
The circuit uses the primary power frequency of 60 Hz as the input to a diode rectifier circuit. The 60 Hz input is the 24VAC output of transformer T1 (secondary winding, Pins 8 & 9) located on the 24V chassis. (Refer to AC Power Distribution).



√ Fig. II-14 REAL TIME CLOCK

The diode rectifier circuit has two outputs TRU60HK and INVO60HK. During each input cycle to the diode rectifier, INV60HK.and TRU60HK. will output once as shown in Figure II-14.

TRU60HK. and INV60HK. are used to set and reset flip-flop (FF20) located at I3. The 4MHz clock (CLK4 . . KO) is used as the clock input to FF20 and FF22. When F/F FF20 is set, flip-flop FF21 will set with the next DSCP pulse trailing edge. During the time FF20 is set and FF21 is reset, REGCLKK. is true. REFGLKK. is true for 250 nsec. of each input cycle and is used as the Clock input to a 3-bit register (RFAN) located at G2, with a constant true applied to the carry input of this Register (pin R) and also to the Add mode input (Pin D). The 3 bit register is incremented by 1 with the trailing edge of each REGCLKK. to occur. When the Register contains a binary value of 101, (5) pins K & P are true; thus the output of Gate GLJ1 at F3 (DIVBY6K) is true. With DIVBY6K true, DVBY6.K is true through the jumper chip JRPN at H2 and CLRRGIK is also true. The next REGCLKK which occurs will cause RTCLOCKO to be true for 250 nsec and will reset the 3 Bit Register (RFAN) to a binary value of 000 (zero). Figure II-15 illustrates the timing generation of one Real Time Clock pulse (RTCLOCKO).



√ Fig. II-15 REAL TIME CLOCK TIMING

RTCLOCKO is the "J" input to the CC Register 2 Bit Position Processor Card F (5-5). The next CLK4 . . KO pulse will cause CC2 . . . F. to set as shown in Figure II-16.

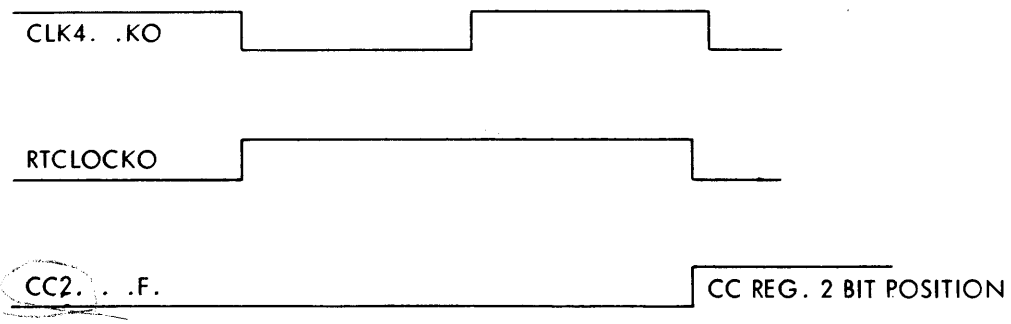


Fig. II-16

BASIC MACHINE STATES

The B 1700 S-Memory Processor can be in either of two basic machine states, Halt or Run. Refer to Figure II-17.

HALT STATE

Within the Halt State there are effectively four substates: Display, Load, Read and Write.

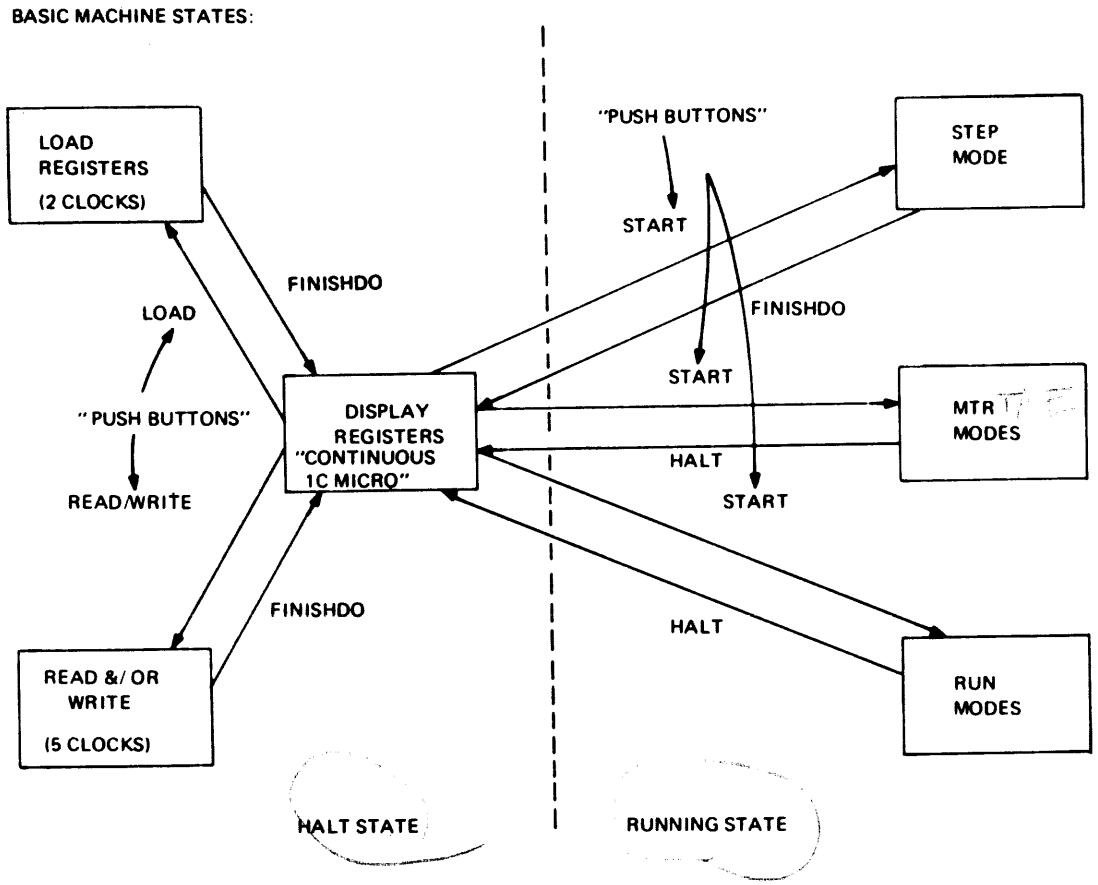


Fig. II-17 BASIC MACHINE STATE BLOCK DIAGRAM

DISPLAY SUB-STATE

When the Processor is in the Halt State, the quiescent sub-state is the Display Registers Sub-state at which time a 2 clock 1C Micro is continuously executed. Hard logic within the Processor (Card C) will cause the 1C Micro (Move Register designated by the Register Select & Group Switches on the Console to NULL). NULL is a 24 bit pseudo register which indicates "nowhere"; however, executing the 1C Micro moves the register selected to the Main 24-bit Exchange and the Console lamps reflect the contents of the main exchange.

LOAD SUB-STATE

Setting the Register Group and Select Switches to a particular register and depressing the LOAD Push Button will cause the Load Register Sub-state to be entered for 2 clock periods. FINISHDO occurs during the second clock period. During the Load Register operation, the contents of the Console Switches are gated to the Main 24-bit Exchange and set in the Sink Register selected by the Register Group and Select Switches. The 1C Micro (hard wired) is also executed when in the Load Register state. The format of the Micro is change however to Move NULL to Register selected by the Register Group and Select Switches.

READ WRITE SUB-STATE

Setting the Register Group and Select Switches to either READ or WRITE will, when the READ/WRITE Push Button is depressed, cause either memory read data to be displayed on the console lamps or the contents of the console switches to be written into S-Memory. In either case, the Memory Address Register (MAR(A)) will determine the address of the information to be read from or written into S-Memory. The READ or WRITE state is true for 5 clock periods, FINISHDO occurs during the 5th clock period. The 1C Micro is also executed in the READ or WRITE state and the formate will be either Move READ to NULL or WRITE from NULL. Depressing the READ/WRITE Pushbutton triggers the memory cycle.

RUN STATE

Within the Run State there are three sub-states: Step, Tape and RUN. Depressing the Start Button will cause the Run State to be entered depending upon the position of the Run/Tape/Step switch.

STEP SUB-STATE

When the switch is set to the STEP position and the Start Button is depressed, the Micro currently in the M-Register is executed. When the Micro is finished, the Processor returns to the HALT state. If the Micro executed in the Step Mode is one which results in a branch or skip to a Micro other than the up coming Micro from S-Memory, the Processor does not return to the HALT state when FINISHDO occurs. Instead, a two clock NO OP is executed during which time the Micro located at the branch or skip address is fetched from S-Memory. When the two clock NO OP is finished, the Processor then returns to the HALT state.

TAPE SUB-STATE

When the switch is set to Tape and the Start Button is depressed, forward drive level is sent to the Cassette's drive logic (providing the Cassette is Ready). Data is read serially from tape, assembled in the U-Register and executed in the M-Register. The operation continues until one of the following occurs:

1. Tape parity error is detected;
2. The 2E Micro (Stop on X≠Y)([redacted]);
3. The stop at the gap variant is executed;
4. The General Processor Clear Button is depressed;
5. The Halt Push Button is depressed

When any of these conditions are met, the Processor returns to the HALT state. FINISHDO must again be true to enter the HALT state. This insures the Micro currently executed is allowed to finish.

RUN SUB-STATE

When the switch is set to RUN and the Start Button is depressed, the Micro currently in the M-Register is executed. Micros are fetched from S-Memory during concurrent MFETCH operations which occur during the execution of each Micro. The execution of Micros from S-Memory will continue until a condition is present which will cause the Processor to return to the Halt state. The conditions which will cause the Processor to return to the HALT state are:

1. The Halt Button is depressed.
2. The General Processor Clear Button is depressed.
3. Executing the 1F (Halt) Micro.
4. The Cassette is initiated via the execution of the 2E (Cassette Control) Micro, and a tape parity error is detected.
5. A Memory parity error during an "M" Fetch.

RUN/HALT FLIP-FLOP

The RUN/HALT Flip-Flop determines whether the Processor is in the Halt State or the Running State. Both outputs of the Flip-flop (RUNS . . FO & HALTS . F.) are used to control functions which occur through the System. Certain functions are allowed only when one or the other of the outputs are true. Other functions throughout the system can occur regardless of the state of the Processor. The functions the two outputs of the RUN/HALT flip-flop control are too numerous to detail; however, the conditions that will set the flip-flop to one of the two states is considered.

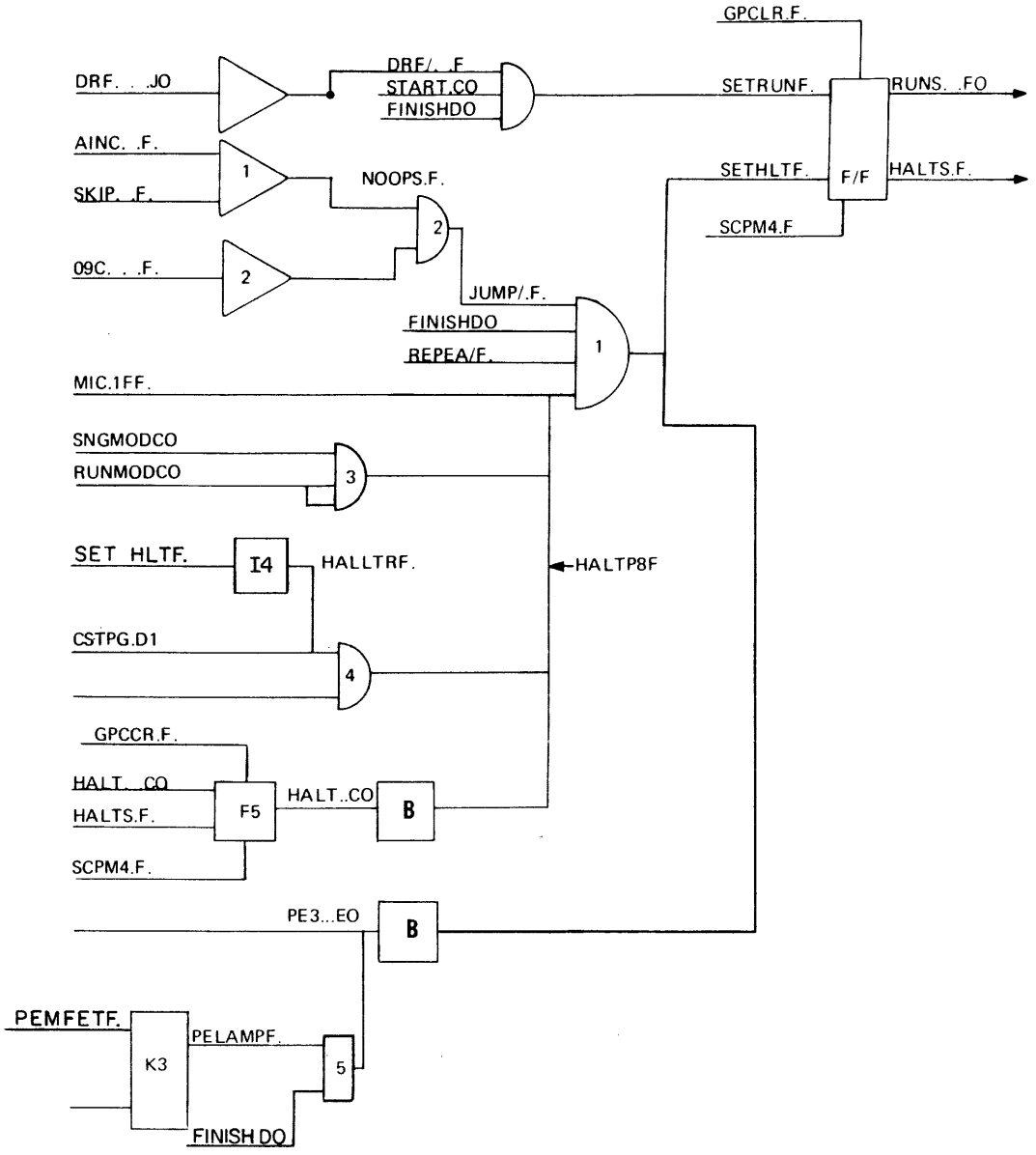
RUN/HALT LOGIC

The Run/Halt State logic is illustrated in Figure II-18. Assuming the General Processor Clear Button on the Console has been depressed, the HALTS . F. state of the Processor is true. Only the functions which can occur when the Processor is halted can occur at this time. To enter the RUN state, the Start Button on the Console must be depressed which will generate START . CO. START . CO is a 2 clock period pulse. Providing the Demand Refresh Flip-flop (DRF . . . JO) is not set, when the next FINISHDO occurs the RUNS . . FO flip-flop will set. Depending on the Mode Switch (RUN/MTR/STEP) the Processor will execute the Micros gated to the M-Register until a halt condition is true.

SYSTEM HALT LOGIC

Five conditions provide a means to cause the Processor to return to the Halt state: depressing General Processor Clear or enabling gate 1 shown in Figure II-18 which provides four conditions to halt the Processor. To enable gate 1, the three levels shown as inputs to inverters 1 & 2 must all be false. The five enable conditions for Gate #1 are:

1. AINC . . F. indicates basically when true that a Micro is currently executing which requires a branch to an address location of S-Memory other than the address location of the next up coming Micro. It may also indicate that the Memory Address Register (MAR(A)) is selected as the sink register in which case a Micro other than the next up coming Micro from S-Memory is to be the next Micro executed. Regardless of the condition present which generated AINC . . F., the Processor is not returned to the Halt state until the next Micro to be executed is fetched.



√ Fig. II-18 RUN/HALT STATE LOGIC

When a branch address is to be established, a NO-OP is executed during which time the fetch of the next Micro (at the Branch Address) occurs. At the completion of the NO-OP, the Processor will be allowed to return to the Halt State.

2. SKIP . . F. when true indicates the skip of the next up coming Micro to occur. The Processor is again delayed from returning to the Halt state until the next Micro to be executed has been fetched.

3. 09C . . . F. true indicates the 9C Micro (Move 24 bit Literal) is currently executing. As the 16 LSB of the Literal must be sourced before the Micro is completed, the Processor is prevented from returning to the Halt state when the 9C Micro is in the M-Register and executing. This has significance in the RUN or STEP Mode only. When TAPE Mode is true, the Repeat flip-flop is set when the 9C Micro is executed. REPEA/F. false will disable gate 1.
   Example: After the 9C Micro has finished (RUN or STEP Mode) a 2 clock NO OP is executed during which time the next Micro to be executed is fetched. Assuming the inputs to inverters 1 & 2 (Figure II-18) are false, gate 2 is enable and therefore the upper input to gate 1 is true. FINISHDO must be true to return to the Halt state. FINISHDO is explained separately. Refer to FINISHED LOGIC.
4. Basically FINISHDO indicates the Micro currently executing is finished. FINISHDO can occur as early as the second clock period on many clock periods after the initial start of the execution of a Micro. The particular type of Micro executing and the Mode of operation will determine when FINISHDO occurs.
5. REPEA/F. is normally true. The REPEATF1 flip-flop is explained in detail under General Control Logic. Basically REPEATF 1 is set only when either executing the 7D Micro (Exchange Double Pad Work), or when the U-Register is sourced in the RUN Mode, or when the 9C Micro is executed in the TAPE Mode.
   The significance of REPEA/F as an input to gate 1 is when the U-Register is sourced in the RUN Mode. When a Micro is executed which designates the U-Register as source, NO OP's are executed during the time the U-Register is assembling the serial read data from tape. Each of the NO OP's executed at this time produce FINISHDO, therefore with the REPEATF1 flip-flop set, RPEA/F. will be false thus disabling the Processor from returning to the Halt state until source information (U-Register data) is available and the Micro is finished. For an example of this particular case refer to the cassette logic.
   The lower input to gate 1, Figure II-18 (HALTP8F.) is effectively the "cause" for returning to the Halt state. The upper three inputs previously explained are used for "control". The six conditions which cause HALTP8F. to be true are defined as follows:
   (1) MIC . 1FF. – If Micro (Halt) executed.
   (2) SNGMODCO & RUNMODCO (STEP MODE)
   SNGMODCO & RUNMODCO indicate the Mode of operation is STEP. Mode of Operation is illustrated in Figure II-19. When FINISHDO occurs providing the Micro executed is not of the branch or skip type of the 9C Micro the Processor is returned to the Halt state. Note that the U-Register is not permitted as source in the STEP or TAPE Mode; therefore REPEA/F. has no significance as the flip-flop will be reset when FINISHDO occurs when executing the 7D Micro in STEP Mode.
   (3) CSTPG . D1 and MTR . . . F.
   CSTPG . D1 and MTR . . . F. indicate the 2E Micro (Cassette Control) is executed and the variant bits indicate either Stop at Gap or Stop when X≠Y. If the variants are set to Stop when X≠Y and X≠Y, CSTPG . D1 will be true. CSTPG . D1 has significance only in the MTR Mode.
   (4) HALT . . CO and MTR . . . F.
   HALT . . CO and MTR . . . F. Indicate the Halt Push Button has been depressed and the Processor is in the MTR MODE.
   (5) HALT . . CO
   HALT . . CO is true for two clock periods when the Halt Button is depressed. Presence of HALT . . CO is remembered in the HALT . . CO flip-flop F5 and will remain true until HALTS . F. is true. This effectively indicates the Processor is Halted.
   (6) PE3 . . . EO
   PE3 . . . EO is true when a non recoverable Cassette parity error is detected. PE3 . . . EO remains true until GPCLR . E or CSTRT . DO is true. PE3 . . . EO will also be true if a memory parity error is detected on an MFETCH operation via gate 5. An MFETCH operation is the concurrent S-Memory fetch of the next Micro to be executed in the M-Register. This has significance only in the RUN Mode. Parity error lamp PELAMPF will be true if this occurs.

MODE OF OPERATION

The Mode of Operation (RUN/STEP/TAPE) is determined by the RUN/STEP/TAPE selector switch on the Console. Positioning the switch in one of three positions will select the Mode of Operation in which the Processor will run. Although the selector switch will always indicate one of the three Modes of Operation, the Mode selected has significance only when the Processor is in the Running State. Refer to Console Logic for an explanation of the selector switch positions. Figure II-19

illustrates the logic on Card F (Processor) which decodes the output of the selector switch. RUN . . . F. is true when the switch is in the RUN position. MTR . . . F. is true when the selector switch is in the TAPE position. When the selector switch is in the STEP position, neither RUN . . . F1 nor MTR . . . F. is true; however, both SNGMODCO and RUNMODCO are true thus providing a return to the Halt state upon completion of executing one Micro. Operations which can be performed when the Processor is in the halt State do not require a specified mode to be true.

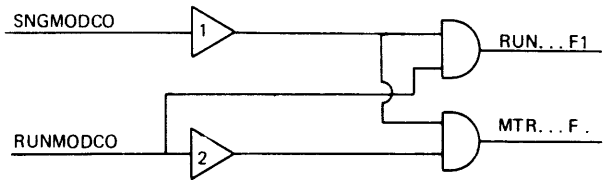


Fig. II-19 MODE OF OPERATION

SEQUENCER (Refer to Figure II-20)

A Sequencer consisting primarily of five flip-flops, is provided to control the execution of the Micro Operators. The Sequencer is located on Processor Card F (1-5). Each Micro, when executed, requires at least two clock periods (4 MHz clock) and up to and including as many as ten clock periods (4 MHz clock) for the 7D Micro, and an infinitive number of clock periods for the execution of the 3F Micro depending on its use. An infinite number of clock periods also occurs when assembling the U-Register from Cassette.

The five flip-flops are shown in Figure II-22 which illustrates the Sequencer and Finish Logic. As the individual Micros when executed require different number of clock periods to "FINISH", the pattern of the states that the five flip-flops will be set to is dependent therefore on the particular Micro being executed. The pattern of "states" the flip-flops will enter when the Processor is halted is illustrated in Figure II-20.

HALT STATE

Assuming all five flip-flops of the Sequencer are initially reset, the flip-flops will produce the pattern of states as illustrated when the Processor is halted. With reference to Figure II-22 with TC/ . . . F1 * TD/ . . . F1 true, the trailing edge of the first SCPM8 . F. clock pulse (8 MHx) sets the TA . . . . F1 flip-flop. The trailing edge of the next clock pulse sets TB . . . . FO and the trailing edge of the next clock pulse sets TC . . . . F1. During the two SCPM8 . F. clock periods prior to when TB . . . . FO is set, the 1/8 Decoder (DFAN) at J6 zero bit output (SO . . . F.) is true. This establishes the SO time.

When TB . . . . FO is set, the DFAN's ones output at L7 and J6 (S1 . . . . D. and S1 . . . . F. respectively are true. This establishes the S1 time. The S1 . . . . D. output is an input to one leg of an AND gate located at K4. Assuming neither MIC . 3FFO nor MIC . 7DD is true, SIMIC . F. will be true at S1 time. This true is applied to the zeroes input bit position of the MFAN located at K5. The Priority Encoder (EFAN) at J4 is used to establish an address for the 8 Input Multiplexor (MFAN). When the Processor is halted, the EFAN's outputs will be false, therefore addressing the zero input to the MFAN. With a true at the zero input to the MFAN, the output FINISHDO is true when S1 time occurs.

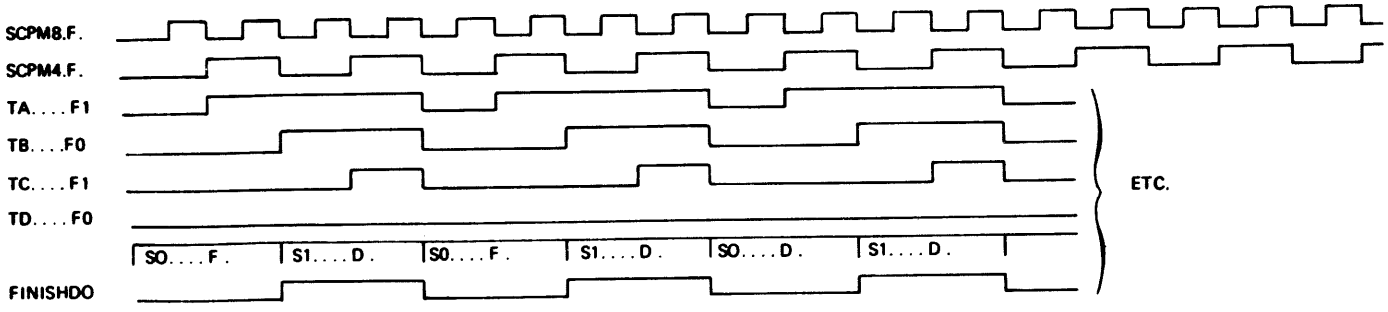


Fig. II-20 SEQUENCEER "HALT STATE"

FINISHDO * SCPM4 . F. are the AND-ed inputs to buffer BHA2 at I5 which produces Sequence Reset (SEQRSTF). The trailing edge of the next SCPM8 . F. clock pulse that finds SEQRSTF true, will cause the TA, TB, TC and TD . . . . Fn

Flip-flops to reset. SEQRSTF is the D-set mode input to these four flip-flops. Therefore, in the Halt mode, the Sequencer will produce S0 . . . S1 . . . S0 . . . S1 pattern.

The pattern of "states" the flip-flops might reach assuming a free running type of operation are illustrated in Figure II-21.

MAXIMUM COUNT

The maximum count of the Sequencer shown in Figure II-21 illustrates the maximum number of discrete states in which the Sequencer can be set to. It should be noted that this timing diagram does not indicate the states of any particular Micro, but only the total or maximum count possible if the sequencer were allowed to "Free Run." The particular sequence which is followed for each of the Micros is given in the explanation of the execution of the individual Micros.

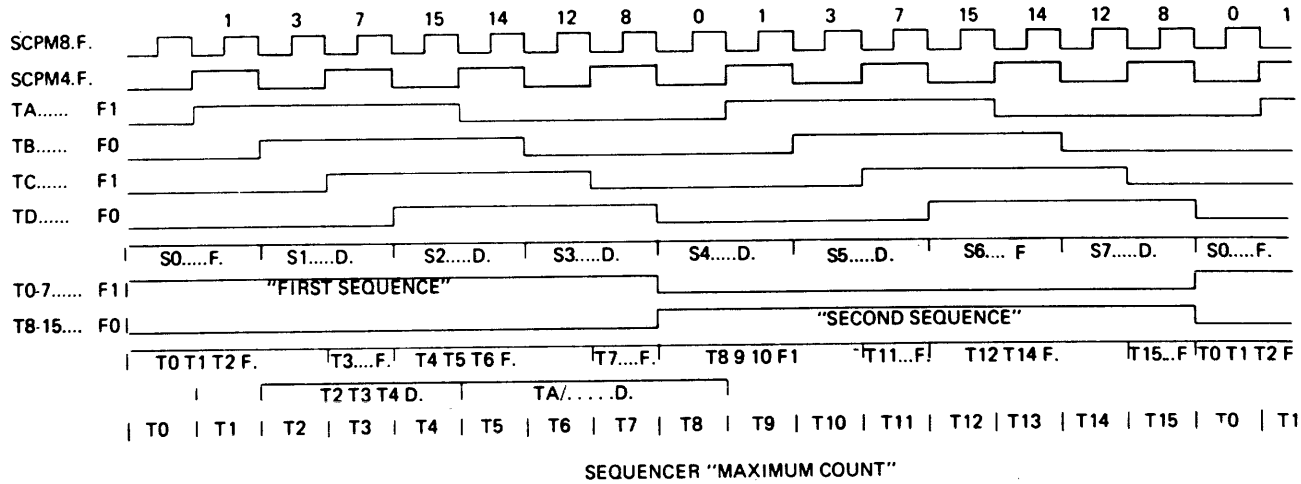


Fig. II-21 SEQUENCER "MAXIMUM COUNT"

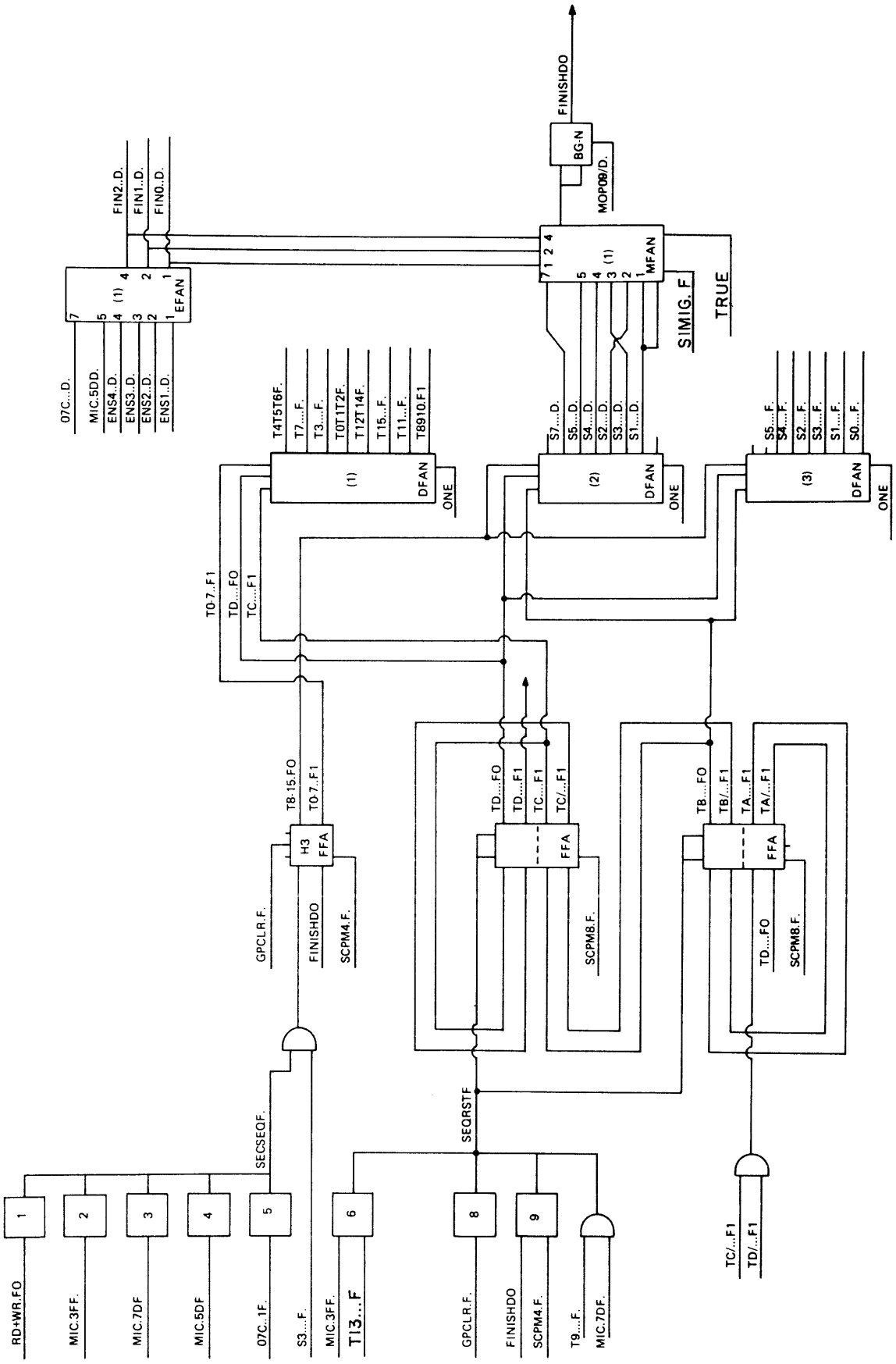
SEQUENCER LOGIC

Sequencer logic is illustrated in Figure II-22. The state of the flip-flop (FFAO) located at H3, determines whether the Sequencer is in the "first sequence" or the "second sequence". Those Micros requiring up to a maximum of 4 clock periods (4MHz) to execute, will cause the Sequencer to sequence only in the "first sequence" (S0, S1, S2 & S3). Longer Micros will cause the Sequencer to enter the "second sequence" (S4S7), and some of the longer Micros will cause the sequence to repeat before the Micro is finished. Each of the eight 4MHz clock periods (S0 thru S7) is divided into two 8MHz clock periods (T0 thru T15). The logic also produces terms such as T4T5T6F. which indicates the time from the beginning of T4 to the termination of T6. The "S" and "T" outputs of the Sequencer and its associated logic are used to control and perform the individual functions to occur when a Micro is executed.

FINISHDO

Each Micro when executed, and upon completion of its execution, will produce the term FINISHDO. The function of FINISHDO is to basically indicate the current Micro executing is finished, thereby allowing the next Micro to be executed to be gated to the M-Register for execution.

An exception to this general rule of FINISHDO is when the U-Register is sourced either in the RUN or MTR mode. During this time, although the Micro executing will require an infinitive number of clock periods to "finish", a HOLD . . F. Flip-flop is provided to force "Machine or pseudo NO-OPs" which in turn allows FINISHDO to occur. FINISHDO is required to occur often so a refresh of S-Memory can occur when necessary. In reference to Figure II-22, Sequencer & Finish Logic, when FINISHDO is true, and a SCPM4.F. pulse is present, buffer #9 will output a true which in turn resets the Sequencer to effectively the SO & TO states in preparation of sequencing the next Micro.



√ Fig. II-22 SEQUENCER FINISH LOGIC

FINISH LOGIC

Logic that develops FINISHDO is shown in Figure II-22. A Priority Encoder (EFAN) located at J4 is used to establish an address which then points to a particular input of an 8 Input Multiplexor (MFAN) at K5. When the input (SM . . . . J.) to the MFAN is true which is currently pointed to the address generated in the EFAN (J4) then FINISHDO is true. If for example the 5 bit position input to the Encoder (MIC . 5DD.) is true, then FIN2 . . D. * FIN0 . . D. will be true and FIN1 . . D. will be false. If at this time the 5 bit position input to the MFAN (S5 . . . . D.) is true, the output FINISHDO will be true. The conditions which cause the six inputs to the Priority Encoder (EFAN) at J4 to be true are stated on the following pages. When none of the inputs to the Priority Encoder are true, the three outputs (FIN2 thru O . . D.) will be false. This effectively addresses the zero input to the MFAN, which will be true when SIMIC . F. is true. During the execution of a two clock period Micro, address zero will be pointed at which will then cause FINISHDO to come true during the second clock period (S1 time).

SEQUENCER-FINISHDO

In summary, the Sequencer will continually change from states S0 - S1 - S0 - S1 . . . . . etc., indicating FINISHDO is occurring at every S1 time unless a Micro is currently executing which, through the decoding illustrated in Figure II-22, prevent FINISHDO from occurring. When this occurs, the Sequencer will then be incremented beyond S0 & S1 times to S2 time etc. until the Micro is to "finish".

SEQUENCER INPUT TERMS AND DEFINITIONS

The following terms are the result of decoding logic and will when true allow the T and S Counter to change states. They are defined as follows:

MIC . 3FF .	3F Micro
MIC . 7DF.	7D Micro
MIC . 5DF.	5D Micro
07C . . 1F.	7C Micro
S3 . . . . F.	7C Micro
S3 . . . . F.	TB . . . . F0 * TD . . . . F0 * T8-15 . F0/
T9 . . . . F.	TA . . . . F1 * T8-15. F0 * TD . . . . F0/ * TB F0/
RD+WR . F0	Console switches set to READ or WRITE and Read/Write Depressed
T13 . . . F.	S6 . . . . F. * TA/ . . . F1

FINISHDO INPUT TERMS AND DEFINITIONS

The following six input levels to the EFAN at J4 will when true produce an address used to determine when FINISHDO is to occur. The basic conditions which must be true to generate these terms is stated to the right of each term as follows:

07C . . . D.	7C Micro exposed to the Micro Distribution Bus.
MIC . 5DD.	5D Micro exposed to the Micro Distribution Bus.
ENS4 . . D.	Processor in Halt Mode, Register Group & Select Switches are set to 15 & 2 respectively (Write from Console) and the Read/Write Button is depressed (one clock period).
	+Processor in Halt Mode, Register Group & Select Switches are set to 14 & 2 respectively (Read to Console) and the Read/Write Button is depressed (one clock period).
	+7D Micro exposed to the Micro Distribution Bus and the Repeat Flip-Flop is reset.
ENS3 . . D.	6D Micro exposed to the Micro Distribution Bus.
	+8D Micro exposed to the Micro Distribution Bus.
	+9C Micro exposed to the Micro Distribution Bus and MTR/.
	+3F Micro exposed to the Micro Distribution Bus and MSBX. T0 is true.

ENS2 . . D. 3,4,5 or 6C Micro and Register is BICN and CREG05BC (BCD)'
+1 or 2C (P R) and Source is SUM or DIFF and CREG05BC (BCD)
+1C or 2C (P R) and Register is BICN and CREG05BC (BCD)
+10C
+11C
+4D
+5D
+145C
ENS1 . . D. UFULL . E) (Indicates +3F Micro and FL=0)

HOLD FLIP-FLOP

The function of the Hold Flip-Flip is to cause certain functions to occur depending on the particular operations taking place.

RESET-HOLD ./FO (TRUE)

The specific functions of the level HOLD./FO are as follows:

1. Enables setting the MFETCHFO Flip-Flop. The MFETCHFO level is used basically to cause the S-Memory Distribution Logic to send a MAR(A) address to the four Memory Modules. Modification of the address is disabled; therefore, during MFETCH operations, Bytes 0, 1, 2, and 3 of one word address are read from S-Memory. Run Mode only.
2. MFETCHFO also causes the ML-Register to be in the D-set Mode providing Granted Refresh (GRF . . . CO) is not true. With the ML-Register in the D-Set mode the next Micro to be executed in the M-Reg which is fetched during a concurrent MFETCH operation, is allowed to be set in the ML-Register. This has significance in the RUN & STEP Mode only.
3. Enables incrementing the MAR(A) address by 1 (MAR+1.F0). MAR+1.F0 effectively increments the MAR(A) address by a bit address of 16. This points to the next Micro to be read from S-Memory during a MFETCH operation. (Run & Step Mode only)
4. Enables gating the contents of the ML-Register to the M-Register in the RUN Mode. (M←ML+UFO)
5. Enables gating the contents of the M-Register to the Micro operator Bus. RUN or TAPE Mode.

Although HOLD./F0 enables the five preceding functions to occur, these functions are also dependent on other Control levels. Figure II-23 illustrates the logic used to set and/or reset the HOLD . . F. Flip-flop. Assuming the General Processor Clear Button has been depressed, the HOLD . . F. Flip-flop is reset and HOLD./F0 is true. The five basic functions listed of HOLD./F0 will occur without interruption, thus Micros are fetched from S-Memory during MFETCH operations, the Memory Address Register (MAR(A)) is incremented by 1 for each Micro fetched, the Micro fetched and temporaraily stored in the Micro Latch Register (MLR) is gated to the M-Register for execution and the Micro in the M-Register is exposed to the Micro Distribution Bus for decoding and execution. Certain operations however require that the normal sequence stated above be disabled temporarily. These operations are those which pertain to the U-Register as a source of either 16 bits of data or Micros.

SET – HOLD. . F. (TRUE)

The function of the HOLD . . F. Flip-flop is to allow a refresh of S-Memory to occur when operations within the system are occurring which do not follow the normal principles of operation. The "normal" operation referred to is that each micro executed will finish within a limited number of clock periods thus allowing a refresh of S-Memory to occur. When the U-Register is sourced either in the RUN or TAPE mode, considerable time is required to assemble 16 bits of information in the U-Register. So as not to disable "FINSHDO" from occurring until the U-Register is full (completely assembled) the HOLD . . F. flip-flop provides a means whereby the current Micro executing is held in the M-Register and Machine or pseudo NO-OPs are forced each being two clock periods in length and each generating a FINISHDO pulse. This insures a refresh of S-Memory can occur when necessary.

The specific functions of HOLD . . F. is as follows:

1. HOLD . . F. when true will cause the MFETCHF0 Flip-flop to be reset at S1 time. This disables the S-Memory Distribution logic from sending a MAR(A) address to the four memory modules, RUN mode only.

2. In addition when the MFETCHF0 flip-flop is reset the ML-Register is no longer in the D-set Mode but rather in the No-Action Mode. Therefore, the contents of the ML-Register will remain unchanged unless a General Processor clear should occur. With the contents of the ML-Register "locked in" the next Micro to be executed which was fetched from S-Memory, is held in the ML-Register. RUN Mode only.

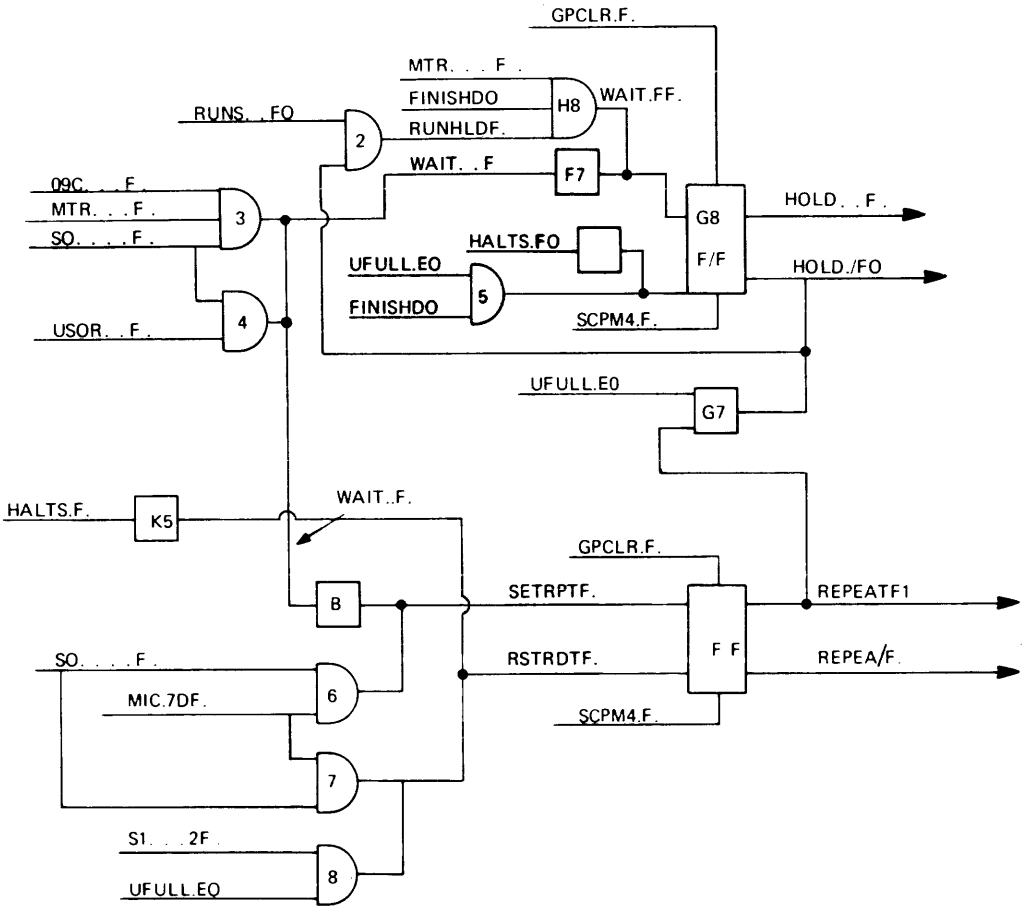


Fig. II-23 HOLD./FO & REPEATF1 CONTROL LOGIC

REPEAT FLIP/FLOP

The Repeat Flip-Flop (REPEATF1) is used during the execution of a 7D Micro or a 1C or 2C Micro with the U Register designated as the source. The Repeat Flip-flop is also used during the MTR mode at S0 time when the 9C Micro is executing. A detailed explanation follows. The Repeat Flip-Flop logic is illustrated in Figure II-23.

1. When the 7D Micro (Exchange Double Pad Word) is executed, as the 7D Micro requires 10 clock periods to complete, REPEATF1 is set at the trailing edge of the first "S0" time will disable FINISHDO from occurring until "S4" time and of the second sequence. Note the sequence will set to S0, S1, S2, S3, S4, S0, S1, S2, S3 and S4 during the execution of the 7D Micro FINISHDO will not occur until the second S4 time occurs. REPEATF1 is reset at the trailing edge of the second "S0" time.

2. When MTR Mode is true, the 9C Micro is currently executing at "S0" time. WAIT . . F. provides for setting REPEATF1 at this time. With REPEATF1 set, when the 16 LSB of the literal are assembled in the U-Register (Indicated by UFULL .F0) HOLD ./F0 is forced true thus "exposing" the 9C Micro for execution. As both REPEATF1 and HOLD . . F. are set, at the trailing edge of "S0" time, FINISHDO which will occur at S1 time will not find the 9C Micro currently executing but rather a Machine or pseudo NO-OP due to HOLD ./F0 being false.

3. When in the RUN Mode and either the 1C or 2C Micro is executed with the U-Register designated as source (USOR . . F.), WAIT . . F. is also true which causes the REPEATF1 flip-flop to be set at the trailing edge of "S0" time. The source data of either the 1C or 2C Micro being the U-Registers contents is not immediately available. With the REPEATF1 flip-flop set, when the U-Register data is available (UFULL .E0) HOLD ./F0 is forced true, thus "exposing" either the 1C or 2C Micro for execution. Note that as "S0" time is used to set REPEATF1 and HOLD . . F., FINISHDO which would occur during S1 time will not find the 1C or 2C Micro currently executing but rather a Machine or pseudo NO-OP due to HOLD ./F0 being false.

REPEAT AND HOLD F/F INPUT TERMS & DEFINITIONS

The input levels to the HOLD . F. and REPEATF1 flip-flops are defined as follows:

WAIT . FF.

1. MTR . . . F. indicates that the Processor is in the MTR mode.
2. FINISHDO indicates a Micro read from tape and assembled in the U-Register has been transferred to the M-Register and has completed its execution.
3. RUNHLDF indicates that the Processor is Running and HOLD ./F0 is true.
4. During a Cassette operation, HOLD ./F0 will be true when the U-Register is completely assembled. (UFULL .EO* FINISHDO).

FINISHDO is generated as the result of the Machine or Pseudo No-OPs which are forced during the assembling of data in the U-Register from Cassette.

In summary a Micro from tape has been executed and because MTR Mode is ture, the HOLD . . F. flip-flop must be set which causes HOLD ./F0 to be false thus forcing NO-OPs, until the next Micro is read and assembled from tape.

WAIT . . F

WAIT . . F. when true indicates the 9C Micro, Move 24 Bit Literal has been read from tape (TAPE Mode) and gated to the M-Register for execution. S0 . . . . F. indicates the first clock period of the execution of this 9C Micro. The 16 LSB's of the literal are the next 16 Bits of information to be read from tape; therefore, the HOLD . . F. flip-flop is set thus disabling HOLD . /F0 from exposing the 9C Micro to the Micro Distribution Bus for execution. This forces a Machine or Pseudo NO-OP to Finish at S1 time followed by many 2 clock pseudo NO-OPs during the assembling of the 16 LSB of the literal. The REPEATF1 flip-flop is also set with WAIT . . F. When UFULL . E0 occurs with REPEATF1 true, this indicates that the U-Register has 16 bits of information completely assembled. HOLD ./F0 is forced true via Buffer G7 to insure that the 9C Micro "held in the M-Register" is exposed immediately and executed. Gate 4 will effectively cause the same actions to occur as did gate 3. Gate 4 is used in the RUN mode when the U-Register is sourced. In this case the Micro executed which caused USOR . . F. to be true must be held in the M-Register while Machine or Pseudo No-OPs are forced, during the assembling of the U-Register Information.

UFULL . E0	indicates the U-Register is full. "16 Bits of information."
FINISHDO	refer to FINISHDO explanation
MTR . . . F .	MTR Mode. When the Prcoessor is running, Micros are read from tape, assembled in the U-Register and executed in the M-Register.
USOR . . F .	The Processor is in the Run Mode and either the 1C or 2C Micro is executing in the M-Register with the U-Register designated as source.
RUNS . . F0	The processor is running (The Start Pushbutton has been depressed).
09C . . . . F.	The 9C Micro is in the M-Register and is currently executing.
S0 . . . . F .	"S0" time of the Sequencer
MIC . 7DF .	The 7D Micro (Exchange Double Pad Word) is in the M-Register and is currently executing.
S1 . . . 2F .	"S1" time of the Sequencer
HALTS . F .	The processor is halted.

ML ENBLFO (MEMORY LATCH ENABLE)

The function of MLENBLFO is to enable "reading" the contents of the ML-Register. The contents of the ML-Register read is normally a 16-Bit Micro which is to be set into the M-Register. During the execution of the 9C Micro (RUN or STEP Mode) the information read will be the 16 LSB of the 24-bit literal. In addition to MLENBLFO, the status of MLCONTHO will determine which 16 bits of the 32-bit ML-Register is read. Refer to ML-Register explanation for details.

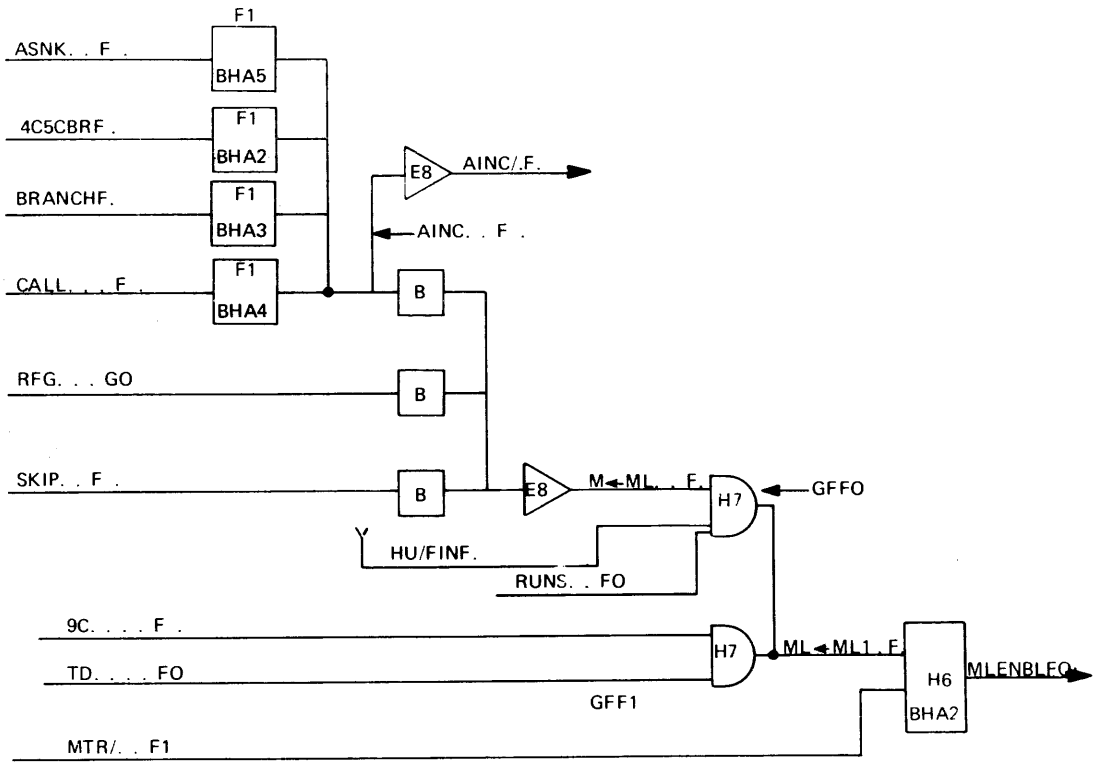
FUNCTIONAL DETAIL

The logic that develops MLENBLFO is illustrated in Figure II-24. MTR/ . . F1 insures a read of the ML-Register can occur only in the RUN or STEP Mode. Gate GFF1 at location H7 enables reading the 16 LSB of the lietral during the execution of the 9C Micro. These 16 LSB are gated to the 16 LSB of the Main Exchange at TD . . . . F0 time (S2 and S3 time). Note a Machine NO-OP is forced upon completion of the 4 clock 9C micro as the M-Register is cleared. A MFETCH operation occurs during the NO-OP to fetch the next Micro for execution.

Gate GFFO at location H7 enables reading the ML-Register as follows:

A. RUNS . . F0 indicates the Processor is Running "the Start Button has been Depressed."

B. HU/FINF . indicates HOLD . /FO * UFUL . / . F * FINISHDO are true. Refer to the MSTARTFO explanation Figure II-25, Gate 2.



√ Fig. II-24 "MLR" CONTROL LOGIC

C. M←ML . . F . indicates none of the OR-ed inputs to the Inverter at F8 are true. The "OR-ed" inputs when all false indicate the Micro currently executing is not one which requires a Branch or Skip to a "new" MAR(A) address but rather one which allows the execution of the next in line MICRO fetch from S-Memory during a MFETCH operation. This next in line MICRO is in the ML-Register when FINISHDO occurs. A Refresh S-Memory operation will also disable M←ML1 . F . and therefore disable reading teh ML-Register contents. This effectively gates zeros to the M-Register causing a 2 clock NO-OP to be executed during the refresh cycle. Note that RFG . . . C0 is the result of Demand Refresh and FINISHDO. An exception to this is during the execution of the 3F Micro when a Refresh is required before the 3F Micro is finished. Although M←ML . . F . is still disabled, thus causing "zeros" to be at the output of the ML-Register, the M-Register will not receive the zeros but will rather "hold" the 3F Micro until finished. "M←ML+UFO will not be true until FINISHDO occurs." Refer to the 3F Micro Timing for details.

MSTARTFO

The function of Memory Start (MSTARTFO) is to initiate an S-Memory Read or Write cycle. The MSTARTFO logic is located on Processor Card F (4-5). MSTARTFO is an output to Processor Card K (4-4) and triggers an S-Memory cycle. Refer to Memory Base Timing.

The following condition will cause an S-Memory cycle to be initiated via MSTARTFO (Refer to Figure II-25)

1. A Memory Refresh Cycle granted will generate a memory cycle via RFG . . . CO (gate 6 Figure II-25). Refer to memory refresh explanation for generation of RFG . . CO.
2. SETRUNF . (Gate 5) is true when the Start Button has been depressed (START . CO), FINISHDO is true, and a refresh cycle is not in progress (DRF/ . . F .). SETRUNF . is also the set input to the RUN/HALT flip-flop which indicates whether the Processor is in the RUN or HALT State. When the Processor enters the RUN state, the contents of the M-Register is executed. By generating MSTARTFO with SETRUNF . a MFETCH operation is initiated at the same time the Processor enters the Running State. This MFETCH operation is concurrent with the execution of the Micro in the M-Register which is executed when Start is depressed. The MFETCH operation which occurs has significance only in the RUN or STEP Mode as MTR mode true will disable reading the ML-Register contents to the M-Register (MLENBLFO is held false when in the MTR Mode). Note that the Memory read data, present as the result of the MFETCH operation is latched into the ML-Register prior to being gated to the M-Register. When the Processor is in the MTR Mode, because the contents of the M-Register is initially executed, it is essential that the M-Register be cleared prior to depressing Start.

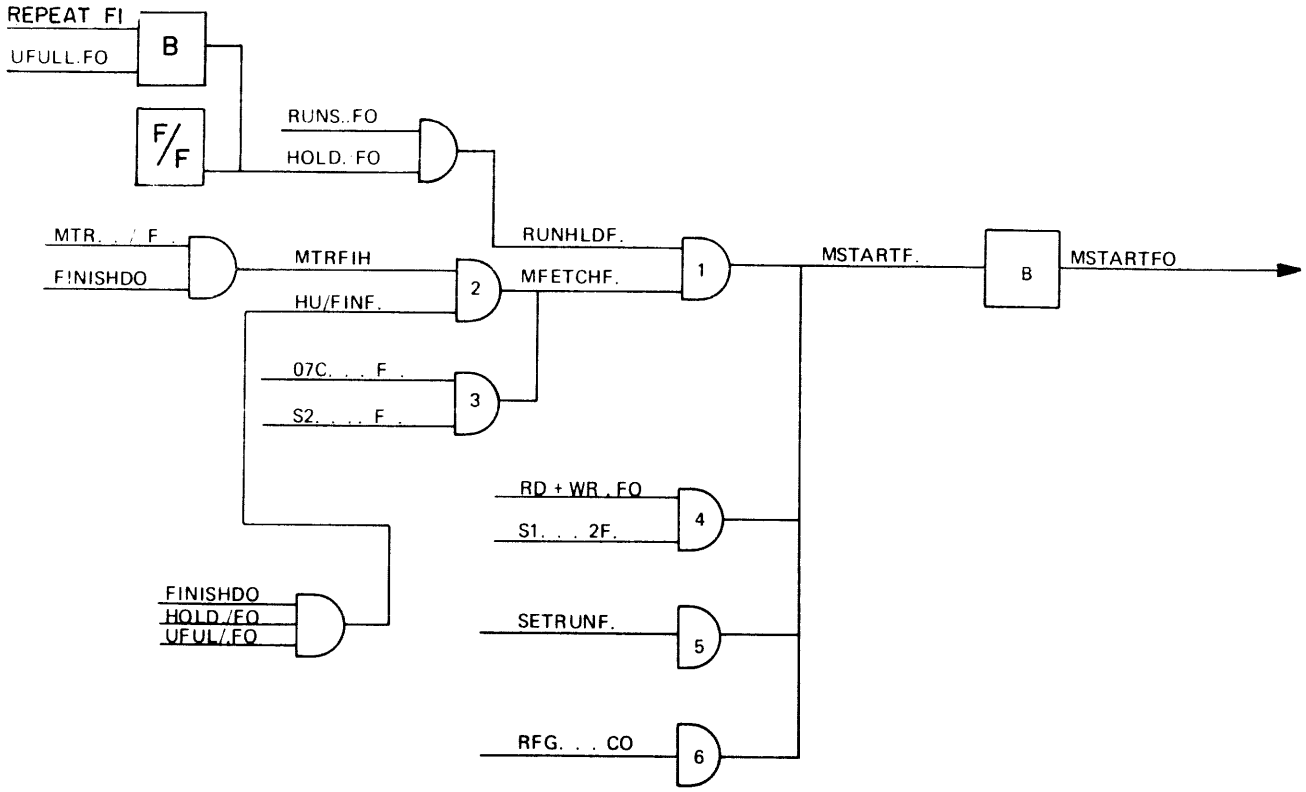


Fig. II-25 "M" START

3. Executing a Read or Write Memory operation via the console will enable Gate 4 at S1 time.
4. Gate 1 Figure II-25 is used to generate MFETCH and READ/WRITE Memory Cycles operations when the Processor is in the RUN & STEP Mode only. RUNHLDF . true indicates the Processor is running (RUNS . . F0) and that the Micro executing is not one that is held in the M-Register (HOLD ./F0) while Machine NO-OP's are forced. The exception to this is if REPEATF 1 and UFULL. E0 are true which forces HOLD ./F0 true. At this time the U-Register is being sourced via the 1C or 2C Micro, U-Register is FULL (completely assembled).

The significance of UFULL .EO * REPEATF1 causing HOLD . /FO to be true is to expose the Micro in the M-Register for execution only. Gate 2 via HU/FINF . being false at this time prevents a MFETCH operation from being initiated as the next Micro to be executed has been fetched from S-Memory and is "latched" in the ML-Register.

Gate 2 indicates FINISHDO is true and MTR Mode is false (MTRFINF .) and HOLD ./FO, UFUL/ .EO, & FINISHDO are true (HU/FINF .). This logic causes a MFETCH operation to be initiated at the same time the Micro in the ML Register is transferred to the M-Register for execution. The MFETCH operation is initiated at SO time. In the case where the U-Register is sourced via the execution of either the 1C or 2C Micro (RUN Mode), REPEATF1* UFULL . EO force the rest output of the HOLD . . FO Flip/flop (HOLD ./FO) true, a machine or pseudo NO-OP is forced at the completion of the execution of the 1C or 2C Micro as the M-Register is cleared and the next Micro to be executed (in the ML-Register) is not gated to the M-Register. When execution of the 2 clock pseudo NO-OP is complete, an MFETCH operation will be initiated which is at the same time as the micro held in the ML register is transferred to the M register for execution.

Gate 3 indicates the 7C Micro (Read or Write Memory) is executing. The MFETCH operation to Fetch the next Micro occurs during S0 and S1 time via Gate 2 and 1. The memory read or write cycle generated via gate 3 at "S2" time is the S-Memory read or write "data" cycle.

MFETCH . F0 F/F

The function of the MFETCHF0 flip/flop when set is to enable the ML-Register in the D-Set Mode. With the ML-Register in the D-Set Mode, the Memory Read Data gated to the input of the ML-Register as the result of a MFETCH operation will be "latched" into the ML-Register. MFETCHF0 when true also causes the S-Memory Distribution logic to send a MAR(A) address to the four Memory Modules. Address Modification is disabled during MFETCH operations, Bytes 0, 1, 2, and 3 of one word address are read from S-Memory.

THEORY OF OPERATION

In order for the above functions to occur MFETCHF0 must be true. Many of the Micros executed are 2 clock periods in duration which indicates FINISHDO will occur at S1 time. When a string of 2 clock Micros is executed the MFETCHF0 flip/flop will remain set thereby allowing concurrent MFETCH operations during the execution of each of these 2 clock Micros. The input logic to set and reset the MFETCHF0 F/F has significance when a Micro is executed which requires more than 2 clock periods. Assuming the Processor is either in the RUN or STEP Mode, and MFETCH operation will occur during the first two clock periods (S0 and S1 time) of all Micros executed. When a Micro is executed requiring more than two clock periods, the MFETCHF0 F/F will be reset, thus disabling the functions of the flip-flops which have been stated above for the remaining clock periods of the longer Micro. When the longer Micro does FINISH, the MFETCH Flip-flop is again set.

When it is necessary to do a Memory Refresh the S-Memory Distribution logic uses the level MFETCHF0 to disable address modification and to send a refresh address to all four Memory Modules – refer to S-Memory section for details.

FUNCTIONAL DETAIL

The logic that develops MFETCHF0 is shown in Figure II-26. A detailed explanation follows.

SETRUNF . (F7) occurs during S1 time when the Start Button has been depressed. Setting the MFETCHF0 F/F at this time insures the fore-going functions of MFETCHF0 will occur. Note that setting the MFETCHF0 F/F via SETRUNF . has significance only in the STEP or RUN Mode. In the MTR Mode, although the functions stated occur, the contents of the ML-Register is not gated to the M-Register for execution.

HU/FINF The output of Gate GFJO at F8 (HU/ . FINF) provides for setting the MFETCHFO F/F at the completion of each Micro when FINISHDO is true with the following exception. In the case of Cassette operations whereby the U-Register is sourced via execution of the 1C or 2C Micro, the status of the level UFUL . / . F is sensed. When the U-Register is full, UFULL . EO is true and UFUL . / . F will be false. During the 2 clock periods when UFUL . / . F is false the 1C or 2C Micro is exposed for execution as HOLD . /F0 will be true. A MFETCH operation is not desired at this time as the next Micro to be executed has already been fetched from S-Memory and is latched in the ML-Register. When the 1C or 2C Micro finishes, a 2 clock machine or pseudo NO-OP is forced which clears the M-Register. When the 2 clock NO OP finishes, gate GFJO at F8 will be enabled and the MFETCHFO F/F will be set thus enabling gating the MFETCH read data to the ML-Register.

SETFETCF . During 2 clock Micros, Gate 2 will output a true at S1 time thus gate 1 is disabled and MFETCHFO remains true. When Finish does not occur at S1 time, gate 2 outputs a false thus gate 1's output is true and the MFETCHFO F/F is reset.

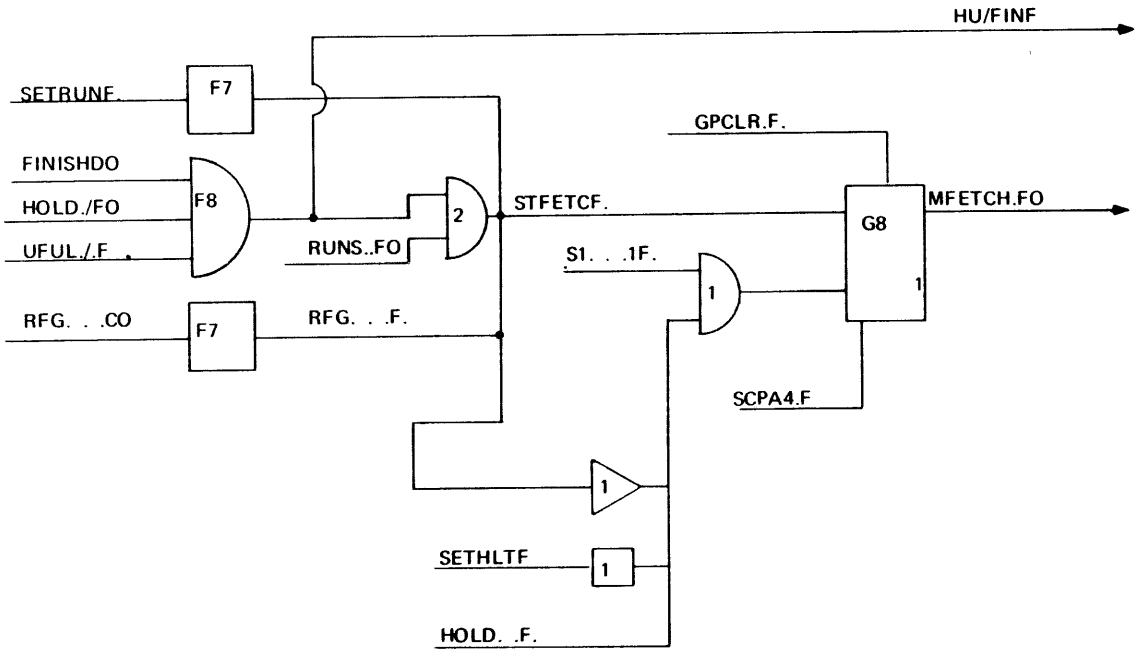
SETHLTF . SETHLTF . is true when FINISHDO occurs and any condition is true that will cause the Processor to be halted. SETHLTF . has major significance when a 2 clock Micro is executed as longer Micros will cause MFETCHFO to be reset at S1 time via Inverter 1's output being true. When a halt of the Processor is indicated the next Micro to be executed when the Processor is again started is in the M-Register and depressing the start button will cause the next MFETCH operation to occur at that time.

HOLD . . F . The HOLD . . F . input to gate 1 is redundant as the HOLD . /F0 intput to gate GFJO at F8 serves all its functions.

RFG . . . C0 RFG . . . C0 true indicates a refresh of S-Memory is to occur. MFETCHFO is set at this time to disable Address Modification and enable the S-Memory Distribution logic to send a refresh address to the four Memory Modules.

GPCLR . F . GPCLR . F . (General Processor Clear) is the D-Mode enable to the MFETCHFO F/F. When true, the trailing edge of the next system clock (SCPM4 . F .) will reset MFETCHFO as the D-Mode Input is not used (always false).

RSFETCF . When a Micro is executed which requires more than 2 clock periods to finish the MFETCHFO F/F will be reset via Gate 1 by using "S1" time as one input. As the basic principle of operation is that only one MFETCH operation occurs during the execution of one Micro, resetting MFETCHFO at S1 time insures that only one MFETCH operation will occur.



√ Fig. II-26 MFETCHFO LOGIC

MSINK . F0

The function of MSINK . F0 is to enable gating the MAIN 24-Bit Exchange (Bits 00 through 15 only) to the inputs of the M-Register. This gating is on Processor Card E (5-5). Note that when the M-Register is the Destination Register the next upcoming Micro to be executed in the M-Register is OR-ed with the source Data. The logic for MSINK . F0 is on Processor Card F (2-5). The M-Register is on Processor Card E (5-5).

FUNCTIONAL DETAIL

The Micros which when executed allow the MEX to be gated to the M-Register are as follows: Refer to Figure II-27.

1C Micro and the M-Register is designated as Sink (gate GFJ0 at Location F2).

2C or 10C Micro and the M-Register is designated as SINK (Gate GFJ1 at Location F2). Note that the input 05D . . . . F1 indicates MOP Bits 8 and 10 (M-Register) and 2 SNK . . D1 indicates the 2C Micro (R←P) or the 10C Micro. 2 SNK . . D1 is also true when the 8C or 9C Micro is executed; however, this has significance when TAS or MAR(A) is designated as the Destination register. The M-Register is not permitted as sink during the execution of the 8C or 9C Micro by software rule.

In the HALT State, when the Selector Switch is set to the M-Register MSINK . F0 is true when MTRFINF . is true (gate GFJ0 at Loc. F2) if the Load Button is depressed. Depressing Load will gate the value of the console switches, via the Main 24-Bit Exchange (16LSB) to the M-Register. This is effectively the result of decoding the 1C Micro which is executed in the HALT Mode. Depressing the Load Button causes the 1C Move NULL (Switches) to M to be executed. This will generate MSINK . F0. Also M←ML+UF0 will be true when MSINK . F0 * LOAD . . C0 are true, which puts the M-Register in the D-set Mode.

ASNK . . F .

The function of ASNK . . F . is to enable gating the contents of the Main 24-Bit Exchange (Bits 18-00) to the input of the MAR(A) Register (Bits 18-00 respectively). ASNK . . F . causes the MAR(A) register to be in the D-set Mode. The logic that develops ASNK . . F . is shown in Figure II-27. Note that both the above functions occur when FINISHDO is true.

The logic to develop ASNK . . F . is on Processor Card F (2-5) and the MAR(A) control decoding is on Card F (5-5). The MAR(A) Register and further control decoding is on Processor Card H.

ASNK . . F . disables MLENBLF0 and MAR+1.F0 from coming true at Finish time. MLENBLF0 false disables "reading" the ML-Register to the M-Register. This is necessary to disable gating the next upcoming Micro to the M-Register. Note that MAR(A) designated as "Sink" indicates the next Micro to be executed is located at another address in S-Memory. MAR+1.F0 false disables upcounting the MAR(A) address by a bit value of 16.

The MICROS which when executed generates ASNK . . F . are as follows:

1C Micro and MAR(A) is

1C Micro and MAR(A) is sink (gate GFJ0 at location D0)

2C (R←P), 10C, 8C or 9C Micro and MAR(A) is sink (gate GFJ1 at Location D0 via 2SNK . . D1)

Note that 04D . . . F1 indicates Register Group 4, MAR(A).

In the HALT State when the Load Button is depressed, ASNK . . F . is true via gate GFJ0 at D0 if the selector switch is set to MAR(A).

SNKTASD .

The function of SNKTASD . is to enable using the value contained in the Stack Pointer (TAS) to address the A-Stack during either Read or Write A-Stack operations.

FUNCTIONAL DETAIL

The generation logic of SNKTASD . is on Processor Card D (4-6), see Figure II-27, as well as the gating of the Pointers value to generate the Local Memory Address and Chip Select Levels. The Stack Pointer is on Card F (2-5).

The micros which when executed generate SNKTASD . with the A-Stack as the source or Sink are:

SINK ONLY

The 1C Micro and TAS is sink (gate GFJ0 at Location D2) and the 8C, 9C, 2C, or 10C Micro and TAS is sink (Gate GFJ1 at Loc H3). Note the five foregoing Micros are ANDed with RUNS . . F0 at gate 1 which therefore indicates TAS cannot be a Sink Register during any console operations in the HALT State. The output of Gate 1 (TASNK . D .) is also ANDed with SINKEND1 (Gate GFF1 at Loc. E4). SINKEND1 has basically a timing function to insure a write into TAS occurs at the correct time. Refer to the explanation of either the individual Micro timing or SINKEND1 for details. 145C Micro (Call Relative either Positive or Negative) generates CALL . . D . (gate GFF0 at Loc. E4). T3 . . . . D . has a timing function. SINKEND . is also generated at T3 time, refer to the explanation of either SINKEND . or Micro timing for more details.

SOURCE ONLY

1C or 2C (P←R) Micro and TAS is source generates SOTAS . D. (gate GFJ2 at Loc. E1). SORENBD . has basically a timing function to insure TAS is sourced at the proper time. Refer to Individual Micro Timing or SORENBD . for details.

MTRFINF . Refer to Figure II-27.

The function of MTRFINF . is to indicate FINISHDO is true and in addition the mode of operation is not MTR. (Either RUN or STEP Mode will produce MTRFINF . when FINISHDO is true.

FUNCTIONAL DETAIL

In Figure II-27 MTRFINF . insures the M-Register cannot be the SINK Register when the Mode Switch is set to MTR. Note this will disable a load M-Register operation in the HALT State, although the Mode of Operation has no primary function at this time.

In addition MTRFINF . is used to generate a read of S-Memory during MFETCH operations (Refer to MSTARTF0) and it places the M-Register in the D-set Mode ready to receive the next Micro for execution (Refer to M←ML+UF0).

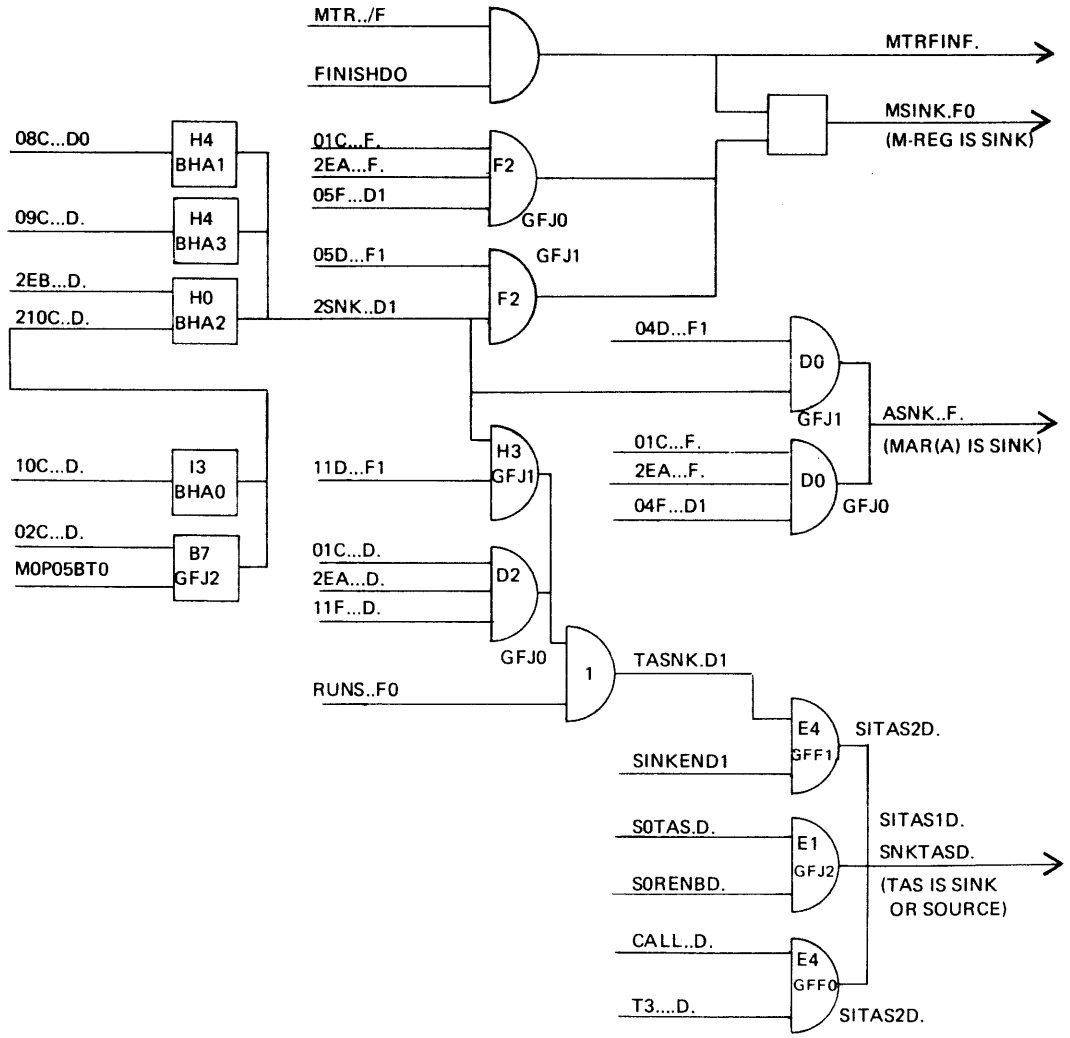


Fig. II-27 M – A – TAS SINK LOGIC

MAR+1 . F0

The function of MAR+1 . F0 is to cause MAR(A) to be incremented by a binary value of 16 which is an increment of the 4th bit position of MAR(A). The output at the 4th bit position of MAR(A) is KBA04 . H. An increment of MAR(A) by "1" at the 4th bit position points the MAR(A) address to the location of the next Micro or in the case of executing the 9C Micro the 16 LSB of the 24-Bit Literal.

FUNCTIONAL DETAIL

The logic which causes MAR+1 . F0 to occur is illustrated in Figure II-28. MAR+1 . F developed by the inputs to Gate F4 provides the means to increment MAR(A) in the HALT State by depressing the Increment A pushbutton.

INCA . . C0

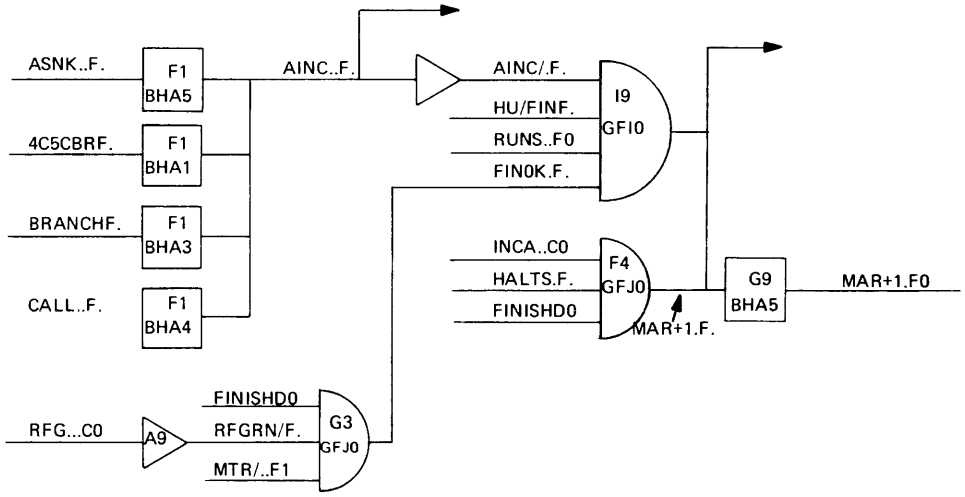
Gate GFI0 at location 19 provides the means to increment MAR(A) in either the STEP or RUN mode. A refresh S-Memory cycle disables MAR+1 . F0 from occurring.

AINC/ . F .

AINC/ . F . true indicates the Micro executing is not one which will result in a Branch to a new Micro at an address other than that of the next upcoming Micro from S-Memory.

HU/FINF .

HU/FINF . is normally true (RUN or STEP Mode) when FINISHDO occurs. The significance of HU/FINF . is when the U Register is sourced when executing either the 1C or 2C Micro (RUN Mode). When the U-Register is assembled, the Micro held in the M-Register is exposed and executed. (HOLD/ . F0 is forced true) At this time the MAR(A) is not incremented as the ML-Register already has the next Micro available for execution. Following the 1C or 2C Micro U as source a Machine or pseudo NO-OP is forced. This NO-OP will cause FINISHDO, and with HU/FINF . true will then allow the MAR(A) address to be incremented. Refer to the Cassette Logic Timing "RUN" Mode and 1C Micro (U-Register Source) for timing details.



√ Fig. II-28 MAR+1.FO LOGIC

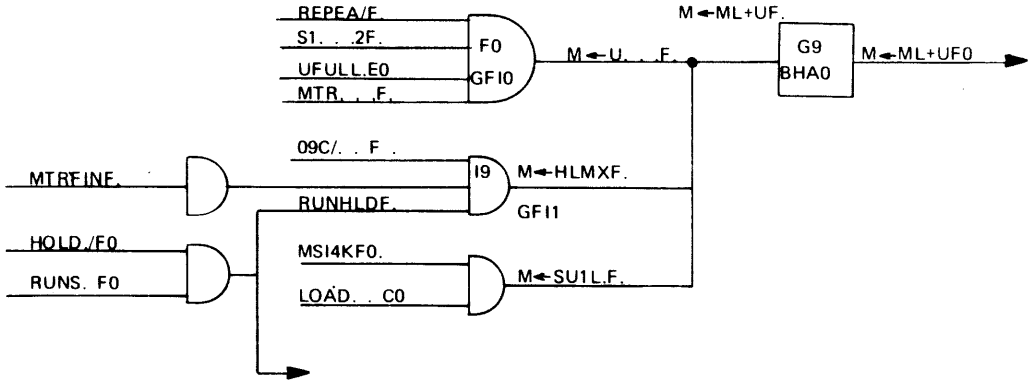
M←ML+UF0

The function of M←ML+UF0 is to cause the M-Register to be in the D-set Mode. When the M-Register is in the D-set Mode, the Micro gated to the inputs of the M-Register will be set in the M-Register with the trailing edge of the next system clock pulse (CLK4 . . K0). When M←ML+UF0 is false, the M-Register is in the Bit set Mode.

FUNCTIONAL DETAIL

The logic which generates M←ML+UF0 is shown in Figure II-29 and is defined as follows:

Three sources of Micros for inputs to the M-Register are available; therefore three control levels are shown: M←U . . . F ., M←MLMXF ., and M←SWI . F . Each when true will cause M←ML+UF0 to be true.



√ Fig. II-29 M←ML+UFO GENERATION LOGIC

M←U . . . F . is true when the contents of the U-Register is to be gated to the M-Register. Note this is done only in the MTR Mode. Refer to Cassette Logic timing for details.

M←MLMXF . is true when the ML-Register or the ML-Register and Main 24-Bit Exchange is to be gated to the M-Register. Note that when the 9C Micro is executed, M←ML+UF0 will not be true when FINISHDO occurs as the contents of the ML-Register at this time is the 16LSB of the 24-bit literal. The 9C Micro is followed by a Machine or pseudo NO-OP as the M-Register is cleared. During the NO-OP the next Micro to be executed is fetched during a MFETCH operation.

M←SWI . F . is true when the M-Register is selected on the Console Register Select Switch and the load timing button is depressed. This allows gating the bit configuration selected by the console switches via the Main 24-Bit Exchange to the M-Register.

CNTUD . F . and CNTDN . F1

The function of CNTUD . F . and CNTDN . F1 is to either put the A-Stack Pointer in the ADD or Subtract Mode.

CNTUD . F1

CNTUD . F1 true causes both 3-bit registers of the A-Stack Pointer to be in the ADD Mode.

CNTUD . F1 and CNTDN . F1

CNTUD . F1 and CNTDN . F1 true causes both 3-bit registers of the A-Stack Pointer to be in the Subtract Mode.

THEORY OF OPERATION

CNTUD . F1 and CNTDN . F1 . logic is shown in Figure II-30. When the top of the A-Stack (TAS) is sourced, source TAS (SOTAS . F .) is true. Either the 1C or 2C Micro (21CM5 /F .) will cause a decrement of the Stack Pointer to occur when FINISHDO is true. This is effectively a decrement after Read.

When the top of the A-Stack (TAS) is designated as Sink then TAS Sink (TASNK . D1) is true and at S0 time the Stack Pointer is incremented. This therefore causes an increment before write to occur.

When the 145 C Micro (Call Relative) either positive 14C or negative 15C is executed, in addition to branching to a new MAR(A) address the address of the next in line Micro is Stored in TAS. As this is a write TAS operation the write occurs after the Increment at S0 time.

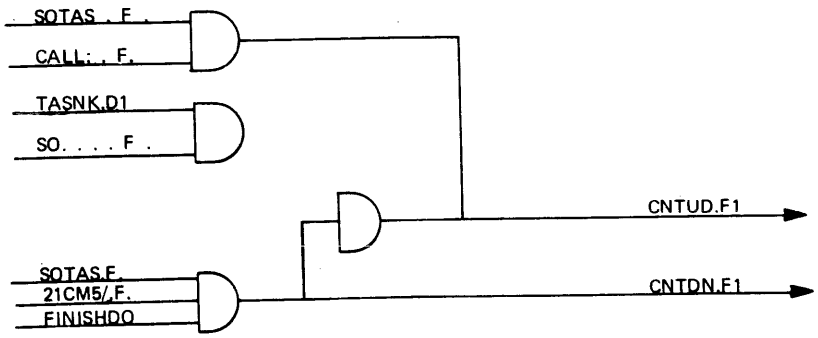


Fig. II-30 CNTUD.F1 & CNTDN.F1

LOCAL MEMORY SOURCE AND SINK ENABLE

The function of the Source and Sink Enable levels (SORENBD . and SINKEND . or SINKEND1 respectively) is to enable the Micro decoding logic to generate the source and/or Sink addresses and chip select levels for storage areas within Local Memory.

The source enable (SORENBD .) is normally true as any move operation would require a source before sink. It is therefore the function of logic to cause SORENBD . to go false and SINKEND . and SINKEND1 to go true at the proper time. Note that all inputs in Figure II-31 are controlled by "T" times.

LOCAL MEMORY SOURCE AND SINK ENABLE INPUT TERMS

The following list of terms control the Source and Sink Enable levels generated which are used to address Local Memory. Each is defined as follows:

TASNK . D1	1C, 2C, 8C, 9C, or 10C Micro and TAS is sink register
01C . . . D	
1EA . . . F1	1C Micro and sink register is Register select 1.
24BSNKD .	1C, 8C or 9C Micro and either X, T, L, FA or FB is sink.
16BSNKD .	1C, 8C or 9C Micro and FL is sink.
GRPSNKD .	2C, 8C, 9C, or 10C and either Y, BR or LR is sink.
	1C Micro and either Y, BR or LR is sink.
SICOLOD .	2C, 3C, 6C, or 10C Micro and sink register is Register Select 0.
S1COL1D .	2C, 3C, 6C, or 10C Micro and Sink Register is Register Select 1.
1CCL0 . D .	1C Micro and sink register select is 0.
09C . . . D .	9C Micro.
10C . . . D .	10C Micro.
1236C . D .	3C or 6C Micro.
	1C or 2C Micro and the U-Register is not the source register.
ARITH . D .	1C or 2C (P←R) and source is SUM or DIFF
	1C or 2C (P←R) and register is BICN.
	3C, 4C, 5C, or 6C and Register is BICN.
CREG05C0	BCD is indicated.
UFULL . E0	Indicates the U-Register is full. Goes false on the trailing edge of the FINISHDO which occurs when UFULL . E0 is ture.
MIC . 7DD .	7D Micro (Exchange DPW)
CALL1 . D .	145C Micro (Call Relative)
CSSINKF1	Refer to Separate explanation at Local Memory Write Timing.

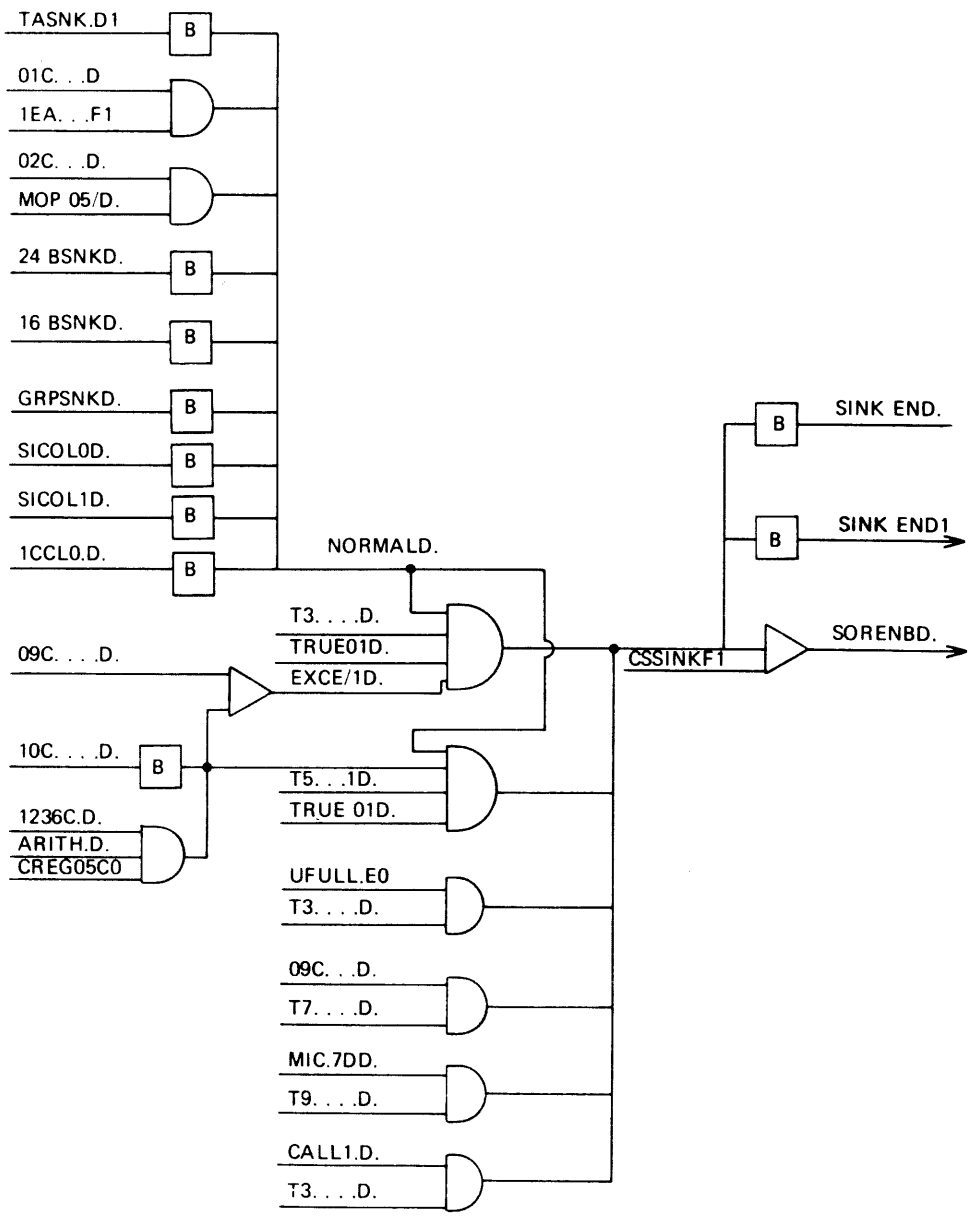


Fig. II-31 SOURCE AND SINK ENABLE

LOCAL MEMORY

Local Memory consists of twenty-four 64 Bit Memory Chips (RFCN's) and six 4 Bit Registers (RFBN's). The twenty-four 64 Bit Memory Chips provide the system with a storage area for 1,536 bits of information. The six 4-bit registers are used as a 24-bit input holding register for all information to be written (stored) in either the A or B-DATA portion of Local Memory. This 24-bit Register is referred to as LBUF (Local Memory Input Buffer).

A DATA AND B DATA

Local Memory is divided into two sections; A-DATA and B-DATA. The A & B-DATA portions of Local Memory each consist of storage areas capable of storing 768 bits of information. The A-DATA and B-DATA portions of Local Memory consist of the following:

A-DATA:
- (5) Registers: FB, X, T, L and FA, each 24 bits in length.
- (3) Reserved Registers each 24-bits in length.
- (8) A-Stack Words (00 thru 07) each 24-bits in length.
- (16) Left Scratch Pad Words (00 thru 15) each 24-bits in length.

The above represents 32 discrete storage areas for Registers, A-Stack, and Scratch Pad words, each being 24-bits in length. Therefore, 32 x 24 = 768 bits of storage is available.

B-DATA:
- (1) Y-Register 24-bits in length
- (1) TEMP-B 24-bits in length
- (1) Base-Register (BR) 24-bits in length
- (1) Limit Register (LR) 24-bits in length
- (4) Reserved Registers each 24-bits in length
- (8) A-Stack Words (08 thru 15) each 24-bits in length
- (16) Right Scratch Pad Words (00 thru 15) each 24-bits in length.

The B-DATA also consists of 32 discrete storage areas each 24-bits in length for a total of 768 bits of storage.

A Block Diagram of Local Memory, illustrated in Figure II-32 shows the A & B-DATA portions of Local Memory. The A-DATA is to the left and the B-DATA is to the right. The LBUF-Register is shown as the input "holding register" to each of the 32 discrete 24-bit storage areas of the A-DATA portion as well as the B-DATA portion.

The input to the LBUF-Register is the Main 24 Bit Exchange (MEX 23-00BT0). All information to be written (stored) in either the A or B-DATA portion of Local Memory must first be gated and stored in LBUF from the Main 24-bit Exchange. The contents of LBUF can then be written (stored) into any of the 32 discrete 24-bit storage areas of either the A or B-DATA portion of Local Memory. Each particular 24-bit storage area has it's own address as well as its own chip select levels. Note that it is the combination of 4 address levels and 9 chip select levels which reference a particular storage area. One write enable level is used for all of Local Memory to control either reading out of or writing into Local Memory.

The address and chip select levels as well as the write enable term are generated through the decoding of the Micro Operators. When the information stored in Local Memory is to be read, the outputs of each of the 32 discrete storage areas are OR-ed so that the 32 storage areas of the A-DATA portion become ADAT (Bits 00 thru 23) and the 32 storage areas of the B-DATA portion become BDAT (Bits 00 thru 23). The ADAT and BDAT outputs (Bits 00 thru 23) of the A & B-DATA portions of Local Memory respectively are inputs to the 24-Bit Function Box (which contains a 24-bit adder), the 4-bit Function Logic, A-DATA only or the outputs can be gated directly to the Main 24-bit Exchange. It should be noted that as LBUF is the input "holding register" for both the A & B-DATA portions of Local Memory, only one 24-bit, storage location in all of Local Memory will be addressed at any particular time when a write into Local Memory is to occur. The exception to this is when either a 4-bit or 16-bit (in the case of FL) Register is selected as the sink register. In this case, only the four or sixteen bits of the particular register selected will be written into Local Memory. When the information stored in any of the 24-bit storage locations of all Local Memory is to be gated to the Main 24-bit Exchange, only one 24-bit storage location will be addressed at a particular time. When a 4-bit or 6-bit source register is selected, all 24 bits are read.

The execution of certain Micros will gate the contents of both a 24-bit storage location within the A & B-DATA portions to the 24-Bit Function Box.

An example of this type of operation is when the 1C Micro is executed. In this case, the contents of the X and Y-Registers are gated to the ADDER within the 24-bit Function Box. The SUM is then gated to the Main 24-bit Exchange and set in the Sink Register selected.

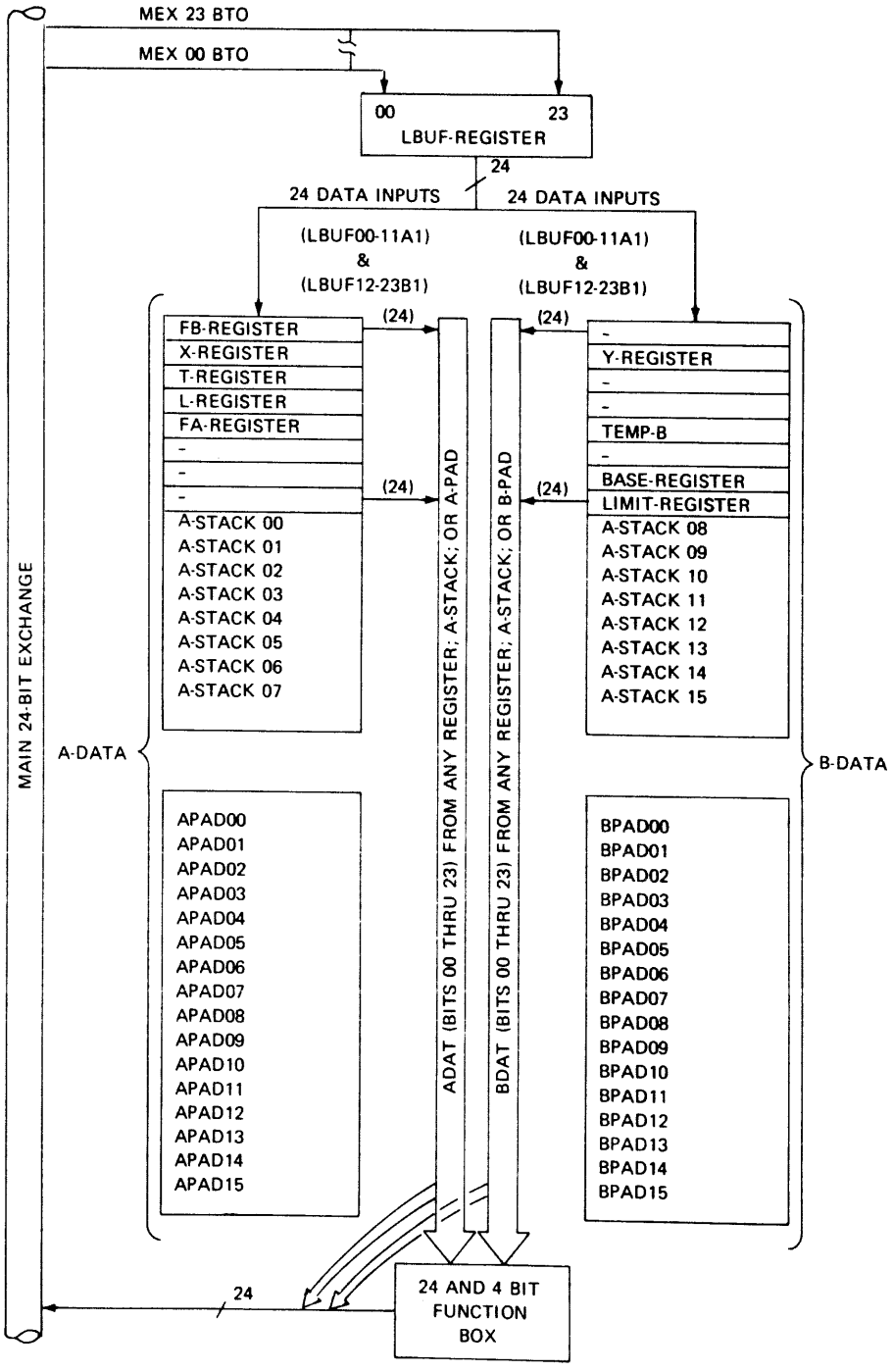


Fig. II-32 BLOCK DIAGRAM/LOCAL MEMORY

LBUF

LBUF consists of six 4-bit Registers (RFBN's) as illustrated in Figure II-33. The Main 24-bit Exchange (MEX 23-00 BT0) is the only input to LBUF. The output of LBUF (LBUF 23-12 B1, and LBUF 11-00 A1) is the only input to Local Memory. Therefore, all data to be written (stored) in Local Memory, either A or B-DATA, must first be written to in LBUF.

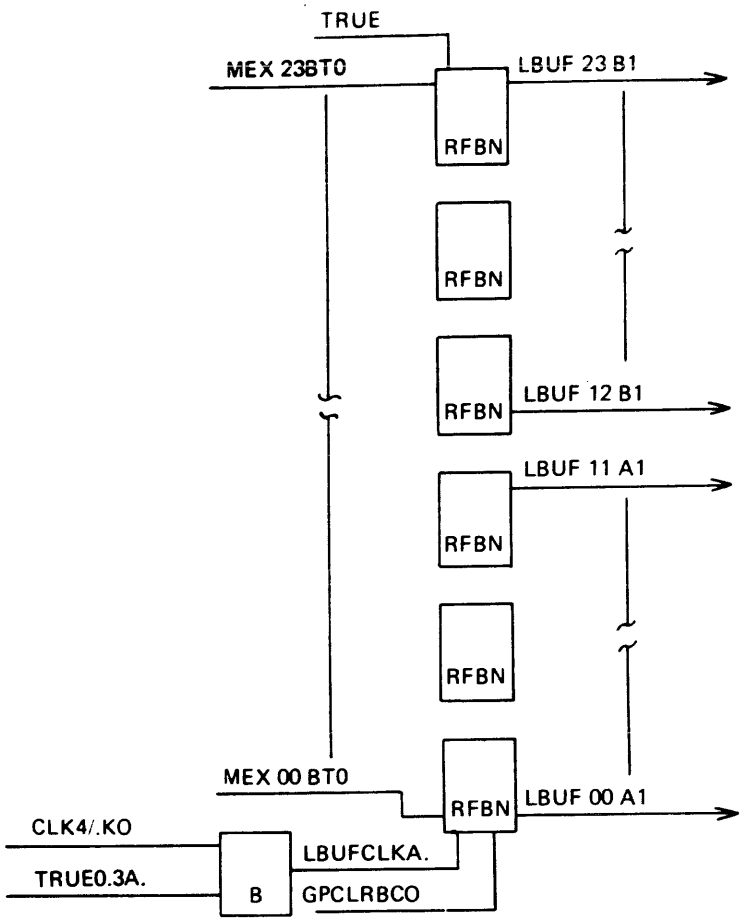
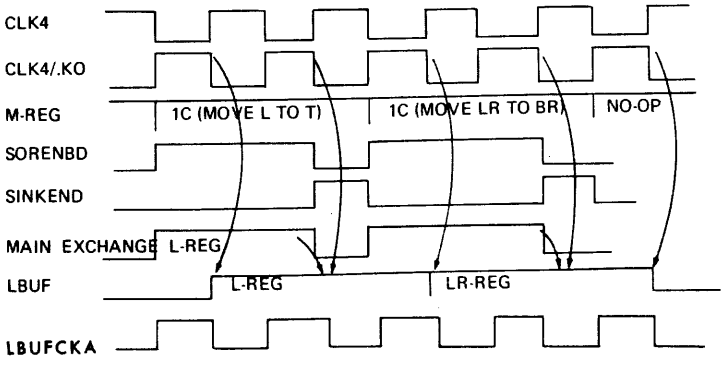


Fig. II-33

LBUF THEORY OF OPERATION

The Mode Control input to the six 4-bit registers designated as LBUF, which causes the registers to be in the "D" set mode, is tied to a true. The trailing edge of the clock pulse used for LBUF (LBUFCKA.) sets the contents of the Main 24-Bit Exchange into the LBUF-Register. Therefore, LBUF will receive the contents of the Main 24-Bit exchange as illustrated in the Timing Diagram, Figure II-34.



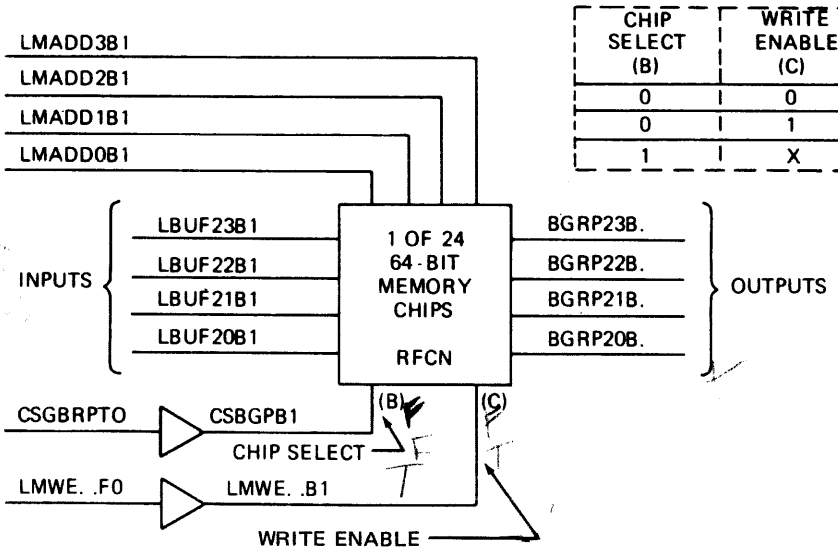
√ Fig. II-34 LBUF INPUT TIMING

Each individual output (e.g., LBUF23B1) is "OR-ed" as an input to four of the twenty-four 64-bit Memory Chips of Local Memory. This provides that each output line from LBUF is an input to each of the thirty-two 24-bit storage locations of A-DATA as well as the thirty-two 24-bit storage locations of B-DATA.

LOCAL MEMORY ADDRESSING

Each of the twenty-four 64 Bit Memory Chips has four address line inputs. These four address lines are LMADD3B1, LMADD2B1, LMADD1B1, and LMADD0B1. As illustrated in Figure II-35, each 64 Bit Memory Chip provides storage for four bits of information for each of the 16 addresses possible using the 16 binary combinations (0000 thru 1111) of the address line inputs. Thus 4 Bits of information for each of 16 24-Bit storage areas is contained in one chip.

If, for example, all the address line inputs are true, then the 15th storage location within the chip would be addressed. Providing the Chip Select input (CSGBRPTO) is true, the four outputs (BGRP23-20B.) will contain the four bits of information stored at this address.



CHIP SELECT (B)	WRITE ENABLE (C)	FUNCTION
0	0	WRITE
0	1	READ
1	X	NO ACTION

Fig. II-35 "ONE" 64-BIT MEMORY CHIP

√ " Fig. II-36 Deleted"

ADDRESSING AND CHIP SELECT

The four chips used to store the four most significant bits (23 thru 20) of each of the thirty-two 24-bit storage locations for the A-DATA as well as the thirty-two 24-bit storage locations for the B-DATA is illustrated in Figure II-37. The address line inputs (LMADD3 thru 0B1) are used to address the four chips illustrated as well as the remaining twenty chips of Local Memory. All twenty four chips are the same write enable (LMWE. .F0). Chips H1 and H0 contain the four MSB of all B-DATA; Chips I1 and I0 contains the four MSB's of all A-DATA. Chip H1 contains specifically the four MSB's of the B-DATA's Registers and A-Stack (Words 8 thru 15). To read out of or write into Chip H1, the chip select level (CSGBRPTO) must be true.

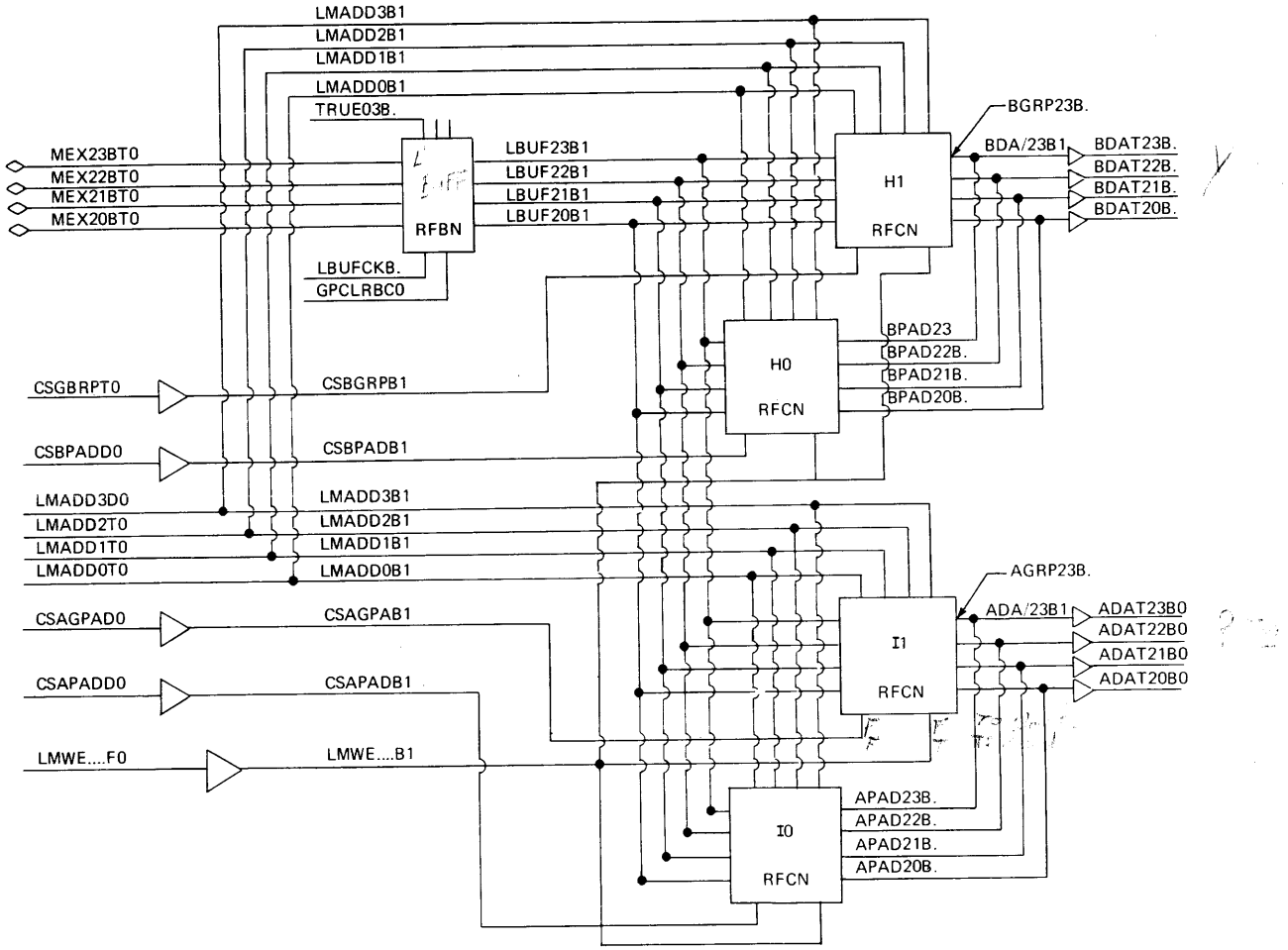


Fig. II-37 LOCAL MEMORY (BITS 23 THRU 20)

When the chip select level is true then the particular location, whether a register or A-Stack Word, is determined by the address lines. Chip H0 contains the four MSB of Right Scratch Pad of B-PAD. When chip H0's select (CSBPADDO) is true, a read out of or write into can occur. The particular Word of Right Scratch Pad addressed is determined by the four address lines. Chips I1 contains the MSB's of the A-DATA's Register and A-Stack (Words 0 thru 7) information. Chip I1's chip select (CSAGPADO) must be true to either read out of or write into the chip. When the chip select is true, the four

address lines determine the Register or A-Stack Word addressed. Chip I0 contains the MSB's of the A-DATA's Left Scratch Pad or A-Pad (Words 00 thru 15). The chip select CSAPADDO must be true to either read out of or write into the chip. The Left Scratch Pad word selected is determined by the four address lines.

Note that the outputs of the H1 and H0 chips are OR-ed, and through an inverter they become BDAT 23 through 20B. . . For this reason, only one of the thirty two 24-bit storage locations is addressed at one time. The same is true for the remaining LSB of the B-DATA as well as all the bits of the A-DATA.

ADDRESSING/CHIP SELECT B-DATA

The Block Diagram, B-DATA Address/Chip Select, Figure II-38, illustrates the twelve 64-bit memory Chips used for the storage of B-DATA. The four address lines (LMADD3-0 B1) shown as inputs to two of the chips are also inputs to the remaining chips. The six chips to the right (D1 thru H1) are used to store bits 23 through 00 of B-DATA Registers and A-Stack words 8 thru 15. The chip select CSBGRPTO will enable all six chips when true. The address lines will therefore determine the register or A-Stack word addressed when the chip select level is true. The six chips to the left (D0 thru H0) are used to store the B-DATA's Right Scratch Pad or B-Pad words 00 through 15. Chip select CSBPADDO when true will enable all six chips. The address lines will again determine the particular word of Right Scratch Pad addressed. Only one chip select level is used to address 24-bits of any registers, A-Stack words, and Right Scratch Pad words within the B-DATA portion of Local Memory. B-DATA is addressable only in 24-bit lengths.

ADDRESSING/CHIP SELECT A-DATA

The Block Diagram A-DATA Address/Chip Select, Figure II-39, illustrates the twelve 64-bit Memory Chips used for the storage of A-DATA. Again the same four address lines (LMADD 3-0 B1) are used to address all twelve chips. The six chips to the right (E1 thru 11) are used to store bits 23 thru 00 of A-DATA Registers and A-Stack words 0 thru 7. As it is permissable to address a 4 bit sink register (e.g., FU-Register) or a sixteen bit sink register (e.G., FL-Register), each 64-bit Memory Chip which contains the A-DATA's Register and A-Stack information has it's own chip select leve. These six chip select levels are CSAGP A thru F DO. When all 24 bits of a register or A-Stack word are addressed either as source or sink, the six chip select levels will be true.

When a 4 or 16 bit source is selected, the six chip select levels will also be ture, thus addressing the 24 bit register in which the 4 or 16 bit register is contained (e.g., FL is the 16LSB of the FB-Register). The six chips to the left (E1 thru I0) are used to store the A-DATA's Left Scratch Pad or A-Pad words 00 thru 15, each 24 bits in length (bits 23 thru 00). Chip select CSASPADDO, when true, will enable all six chips. The address lines will determine which word of Left Scratch Pad is addressed, because only one chip select level is used to address 24 bits of information, the Left Scratch Pad words within the A-DATA are addressable only in 24 bit lengths.

WE Local Memory Write Enable (LMWE. A1 & B1), both are developed from the term LMWE. .F0

ADDRESS AND CHIP SELECTION A & B DATA

The address lines and chip select levels which must be true to select a particular 24, 16, or 4 bit register (sink only), a word of A-Stack (sink or source), and a word of Scratch Pad Left or Right (sink or source) as shown in Fig. II-40. The four address lines are shown to the left. Their binary weight (00 through 15) will address a particular register (either 24 bits or a portion thereof) of either A or B-DATA. They are also used to address either a word of A-Stack (A or B-DATA0 and words of Left or Right Scratch Pad (A or B-DATA). In addition to the address lines, a chip select level or levels must also be true to further "decode" or select a particular register, A-Stack or Scratch Pad word.

Although the address lines are used for both A and B-DATA, the seven chip select levels within the A-DATA columns select only those registers (sink only). A-Stack or Scratch Pads words (sink or source) listed under A-DATA. The two chip select levels under the B-DATA columns select only B-DATA registers (sink or sink), A-Stack or Scratch Pad words (sink or source) listed under B-DATA. To address for example the four bit LC register as sink, the following address lines and chip select levels must be true. All others will be false.

1. LMADD1T0 2. LMADDOT0 3. CSAGPCD0

To address the four bit LC register as source, the chip select levels for the entire L-Register must be true. When Local Memory is address as source, 8 Input Multiplexor's (MFAN's) are used external to Local Memory to select the four or sixteen bit portion of a register if the entire 24 bits is not selected as source. The physical location of some of the registers within Local Memory as far as "like" addresses are concerned is due to the functional operation of the System.

The X and Y Registers are inputs to the ADDER, therefore sharing the same address (Address line LMADDOTO only). The contents of both registers can be read out of Local Memory at the same time. To read out the contents of the X-Register, the six chip select levels (CSAGP A through F DO) must be true. To read out the contents of the Y-Register, chip select level CSBGRPTO must be true. During the execution of the 1C Micro (move SUM to X), the above address line and chip select levels will be true; therefore, both the A-DATA (X-Register) and B-DATA (Y-Register)'s contents will be read out of Local Memory simultaneously. The X & Y-Register's contents are then gated to the inputs of the ADDER within the 24-bit Function Box. The SUM output is then gated on to the Main 24-Bit Exchange and to the Sink Register Selected.

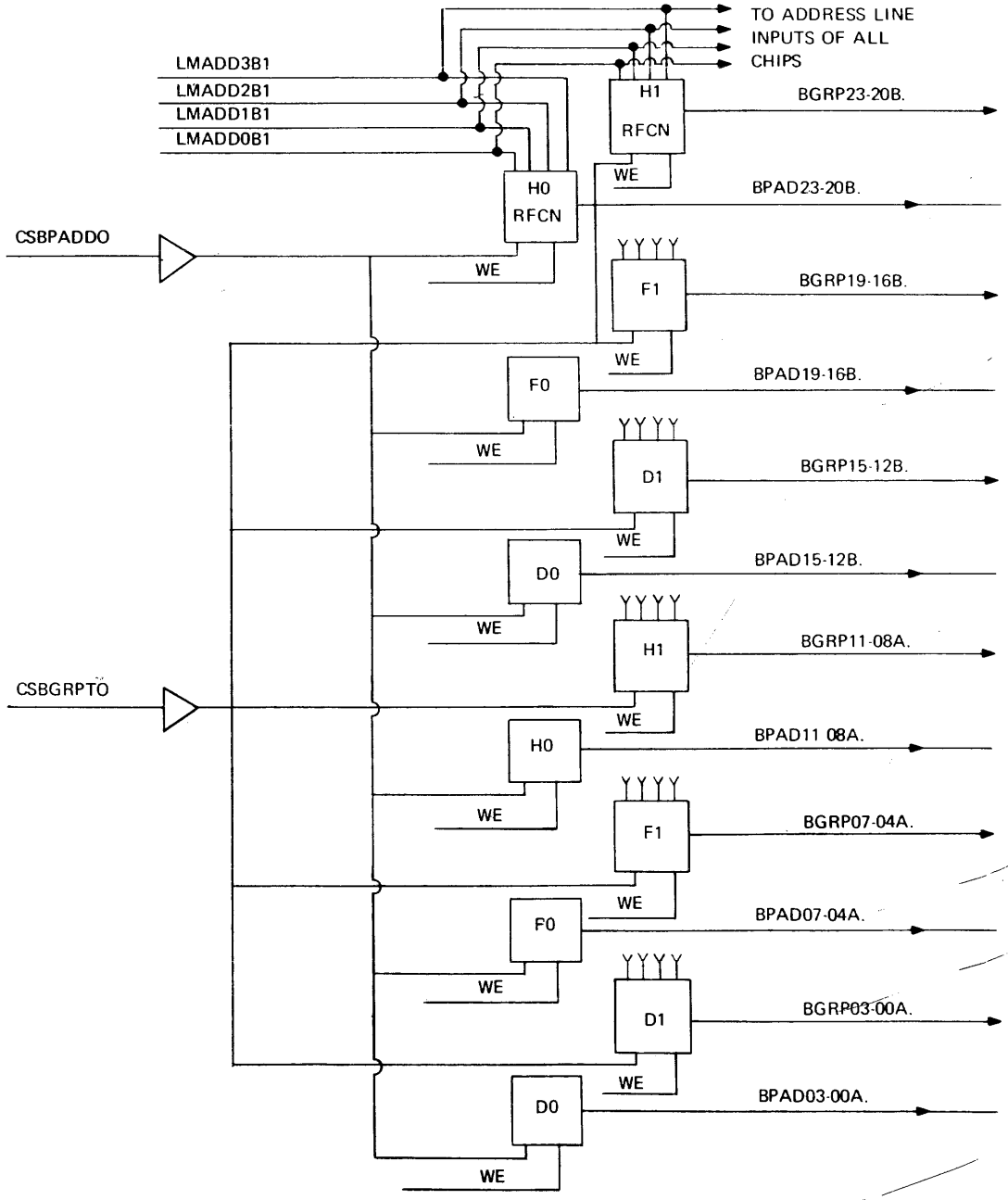


Fig. II-38 B-DATA ADDRESS/CHIP SELECT BLOCK DIAGRAM

The physical location of the FA-Register and TEMP-B also has special significance. During the execution of the 8D Micro (Scratch Pad Relate FA) TEMP-B is used as the holding register for the contents of the Scratch Pad Left word selected. The FA-Register and TEMP-B Register's contents are then gated through the ADDER within the 24-Bit Function Box, to the Main 24-Bit Exchange and back to the FA-Register. Note that the same address (0 1 0 0) will address both the FA-Register and TEMP-B.

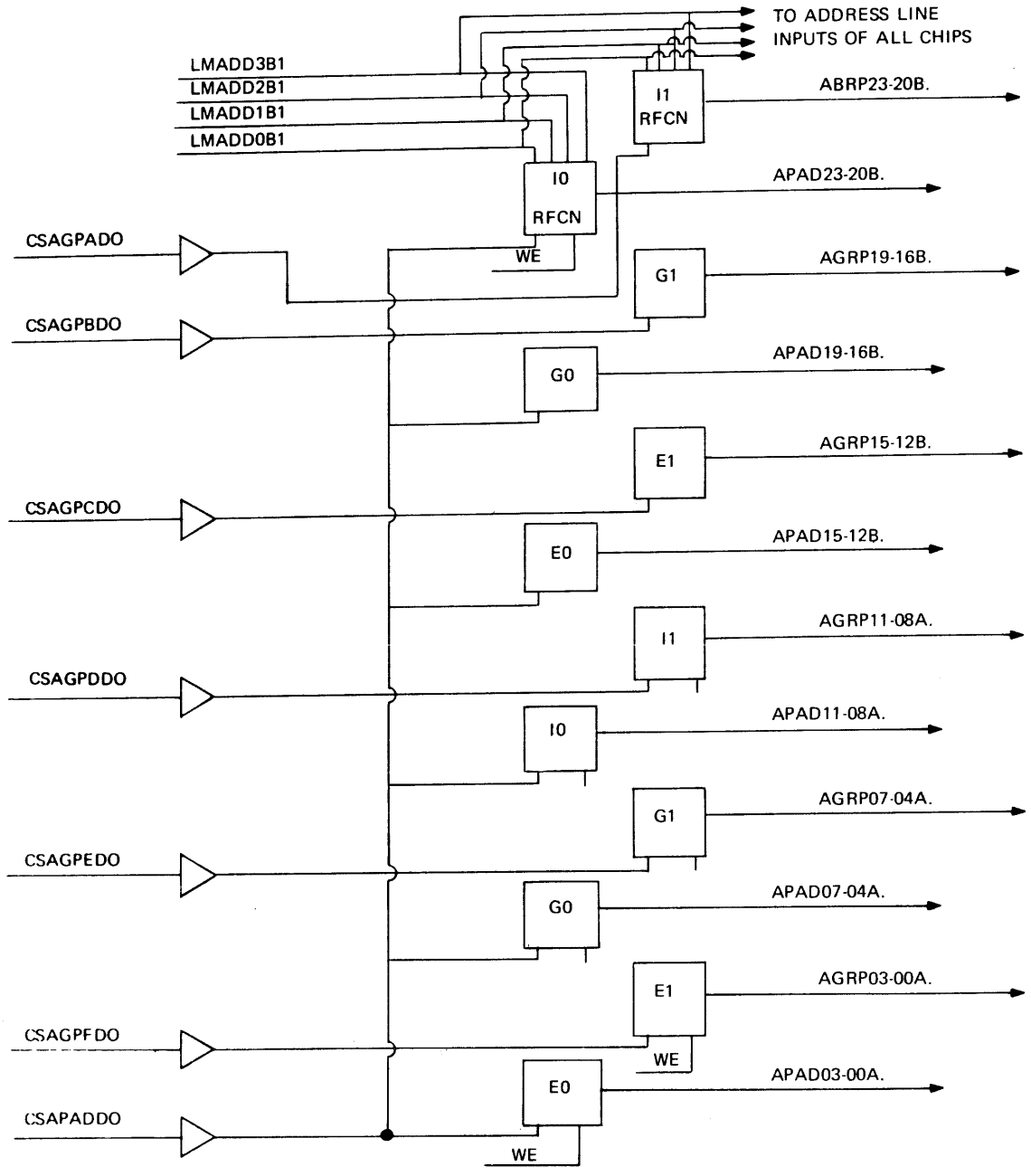


Fig. II-39 A-DATA ADDRESS/CHIP SELECT BLOCK DIAGRAM

Functional Detail

ADDRESS LINES				"A-DATA"								"B-DATA"			
LMADD3TO	LMADD2TO	LMADD1TO	LMADD0TO	CSAPADDO	CSAGPADO	CSAGPBDO	CSAGPCDO	CSAGPDDO	CSAGPEDO	CSAGPFDO	Register Selected	CSBPADDO	CSBGRPTO	Register Selected
0	0	0	0	0	1	1	1	1	1	1	FB	0	1	Reserved
0	0	0	0	0	0	0	1	1	1	1	FL			
0	0	0	0	0	1	0	0	0	0	0	FU			
0	0	0	0	0	0	1	0	0	0	0	FT			
0	0	0	0	0	0	0	1	0	0	0	FLC			
0	0	0	0	0	0	0	0	1	0	0	FLD			
0	0	0	0	0	0	0	0	0	1	0	FLE			
0	0	0	0	0	0	0	0	0	0	1	FLF			
0	0	0	1	0	1	1	1	1	1	1	X	0	1	Y
0	0	1	0	0	1	1	1	1	1	1	T	0	1	Reserved
0	0	1	0	0	1	0	0	0	0	0	TA			
0	0	1	0	0	0	1	0	0	0	0	TB			
0	0	1	0	0	0	0	1	0	0	0	TC			
0	0	1	0	0	0	0	0	1	0	0	TD			
0	0	1	0	0	0	0	0	0	1	0	TE			
0	0	1	0	0	0	0	0	0	0	1	TF			
0	0	1	1	0	1	1	1	1	1	1	L	0	1	Reserved
0	0	1	1	0	1	0	0	0	0	0	LA			
0	0	1	1	0	0	1	0	0	0	0	LB			
0	0	1	1	0	0	0	1	0	0	0	LC			
0	0	1	1	0	0	0	0	1	0	0	LD			
0	0	1	1	0	0	0	0	0	1	0	LE			
0	0	1	1	0	0	0	0	0	0	1	LF			
0	1	0	0	0	1	1	1	1	1	1	FA	0	1	TEMP-B (Reserved)
0	1	0	1	0	(Any or All)						Reserved	0	1	Reserved
0	1	1	0	0	(Any or All)						Reserved	0	1	BR
0	1	1	1	0	(Any or All)						Reserved	0	1	LR
											A-Stack Word #			A-Stack Word #
1	0	0	0	0	1	1	1	1	1	1	0	0	1	8
1	0	0	1	0	1	1	1	1	1	1	1	0	1	9
1	0	1	0	0	1	1	1	1	1	1	2	0	1	10
1	0	1	1	0	1	1	1	1	1	1	3	0	1	11
1	1	0	0	0	1	1	1	1	1	1	4	0	1	12
1	1	0	1	0	1	1	1	1	1	1	5	0	1	13
1	1	1	0	0	1	1	1	1	1	1	6	0	1	14
1	1	1	1	0	1	1	1	1	1	1	7	0	1	15
											Left Pad Word #			Right Pad Word #
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0	0	0	0	1	1	0	1
0	0	1	0	1	0	0	0	0	0	0	2	1	0	2
0	0	1	1	1	0	0	0	0	0	0	3	1	0	3
0	1	0	0	1	0	0	0	0	0	0	4	1	0	4
0	1	0	1	1	0	0	0	0	0	0	5	1	0	5
0	1	1	0	1	0	0	0	0	0	0	6	1	0	6
0	1	1	1	1	0	0	0	0	0	0	7	1	0	7
1	0	0	0	1	0	0	0	0	0	0	8	1	0	8
1	0	0	1	1	0	0	0	0	0	0	9	1	0	9
1	0	1	0	1	0	0	0	0	0	0	10	1	0	10
1	0	1	1	1	0	0	0	0	0	0	11	1	0	11
1	1	0	0	1	0	0	0	0	0	0	12	1	0	12
1	1	0	1	1	0	0	0	0	0	0	13	1	0	13
1	1	1	0	1	0	0	0	0	0	0	14	1	0	14
1	1	1	1	1	0	0	0	0	0	0	15	1	0	15

√ NOTE: A-DATA CSAGP (A–F)DO ash shown indicates only the Chip Select Levels for 4, 16, or 24 Bit Sink. 4 or 16 bit sources will produce the Chip Select Levels for the 24 Bit Register in which the 4 or 16 Bit Register is located.

√ Fig. II-40 LOCAL MEMORY ADDRESS LINES AND CHIP SELECT

ADDRESS AND CHIP SELECTION GENERATION

The generation of the four Address Lines and nine Chip Select Levels is the result primarily of Micro Operator Decoding Logic. The generation of these lines and levels when A-Stack "TAS" is designated as either the source or sink is controlled by the current value of the A-Stack Pointer. For this reason, the generation of these lines and levels is explained separately.

REGISTER AND/OR SCRATCH PAD ADDRESS/CHIP SELECT GENERATION

The Address/Chip Select Generation Block Diagram, Figure II-41, illustrates the basic decoding which occurs when either a Register within Local Memory (A or B-DATA0 or a word of Scratch Pad (A or B-DATA) is designated as either a source or sink. The micro currently executing is held in the M-Register and exposed to the Micro Operator Distribution Bus Lines (MOPnnBTO). The Micro Operator Distribution Bus distributes the Micro (bits 15 through 00) throughout the system to micro decoding logic. As the result of the micro decoding logic, levels are generated which indicate a particular micro-operator (e.g., 1C, 2C, etc. .,.) is currently executing. When the micro currently executing is one that requires addressing one of the Registers or word of Scratch Pad contained within Local Memory, the micro decoding logic will generate levels which designate the Source Group, Source Select, and/or Sink Group, and Sink Select. These levels together with the "Micro-OP" under control of timing logic, and within some cases the Mop lines generate the Source and Sink Addresses at the proper time. Effectively the Chip Select levels are decoded in the same manner.

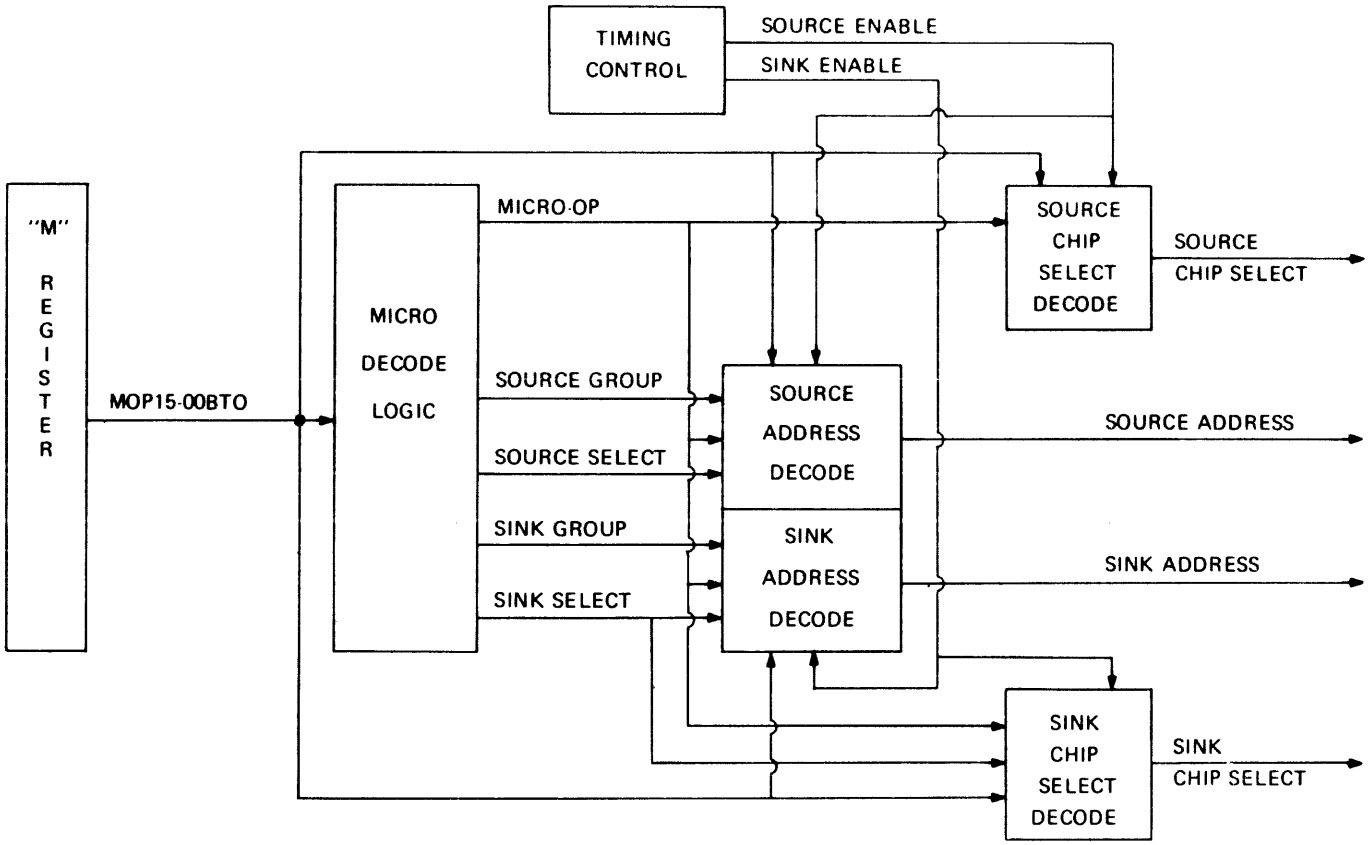


Fig. II-41 LOCAL MEMORY .....ADDRESS/CHIP SELECT GENERATION BLOCK DIAGRAM

THEORY OF OPERATION

Address & Chip Select Generation, Figure II-42, illustrates the detailed decoding of the 1C Micro, the Source Address and Chip Select and the Sink Address and Chip Select decoding. The format of the micro used which generates the logic shown in Figure II-42 is as follows:

0 0 0 1 0 0 1 1 1 0 1 0 0 0 1 0

- Sink Register Group 2, Sink Register Select 2 } T-Register
- Source Register Select 2, Source Register Group 3 } L-Register
- Micro-Op . . . . . 1C, Move L to T.

Note that Fig. II-42 illustrates only the logic that pertains to the above micro format. If another Register were selected as either source or sink, similar logic will be generated.

Assuming the 1C Micro with the above format is in the M-Register and Exposed to the Micro Operator Distribution Bus Lines (MOP15-00BT0) with RUNS. .F0 and HOLD/ .F0 true, the Mop lines are inputs to four DFAN's and one Buffer with output levels designated as 01C. . .D., 03D. . .F1, 2EB. . .D., 02F. . .D., and 2EA. . .D. . As DFAN's require no clock, the outputs are established approximately 12ns after the inputs are present. These five outputs have the following definitions:

01C. . .D.	Indicates a 1C Micro.
03D. . .F1	Indicates the Register Group (Source) is 3.
2EB. . .D.	Indicates the Register Select (Source) is 2.
02F. . .D.	Indicates the Register Group (Sink) is 2.
2EA. . .D.	Indicates the Register Select (Sink) is 2.

These five levels therefore indicate a 1C Micro, Move L (Source) to T (Sink). With the source and sink Registers established, the address and chip select levels required to address these registers is now under control of the timing logic which generates sink enable (SINKEND.) and source enable (SORENBD.) These enable terms (SORENBD. & SINKEND.), are defined separately in this manual as well as during the explanation of Execution of the individual Micros with respect to when they occur and how they are developed.

FUNCTIONAL DETAIL

Assuming the source enable term is true (SORENBD.), the output of gate A (CSAF3.D.) is true. Refer to Figure II-42. With CSAF3.D. true, CSAAFOD. is true, Buffer 2's output is true; therefore, chip select CSAGPFDO is true. With CSAAFOD. true, the five lower outputs of the Micro Operator chip (MOPN) are also true; therefore, chip select levels CSAGP E through A DO are also true. These six chip select levels must be true when selecting the L-Register as source, refer to Figure II-40. SORENBD. true, also generates the source address via EFAN (1). LMADD1FO and LMADDOFO are the address lines required to address the L-Register.

When the sink enable term (SINKEND.) is true, gate B is enabled thus generating chip select levels CSAGP F through A DO for the T-Register. SINKEND. true also causes EFAN (2) to be enabled, thus generating the address line LMADD1FO required to address the T-Register.

A-STACK "TAS" ADDRESS/CHIP SELECT GENERATION

The block diagram of Address and Chip Select Generation, Figure II-43, illustrates the basic decoding which occurs when the A-Stack "TAS" is designated as either source or sink. A-Stack words 0 through 7 indicate A-DATA, and words 8 through 15 indicate B-DATA. Both A and B-DATA can be addressed by the Pointer.

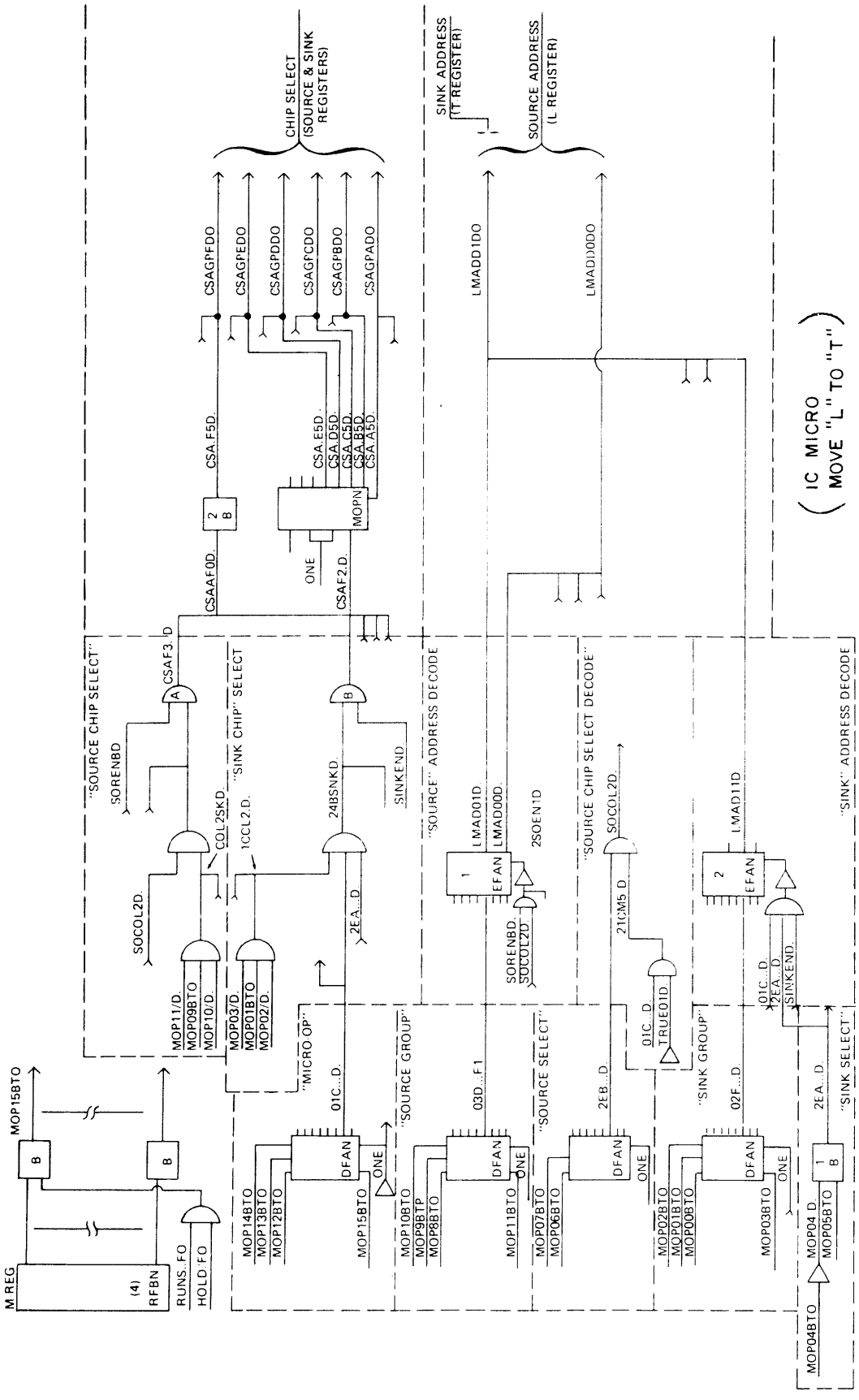


Fig. II-42 ADDRESS AND CHIP SELECT GENERATION

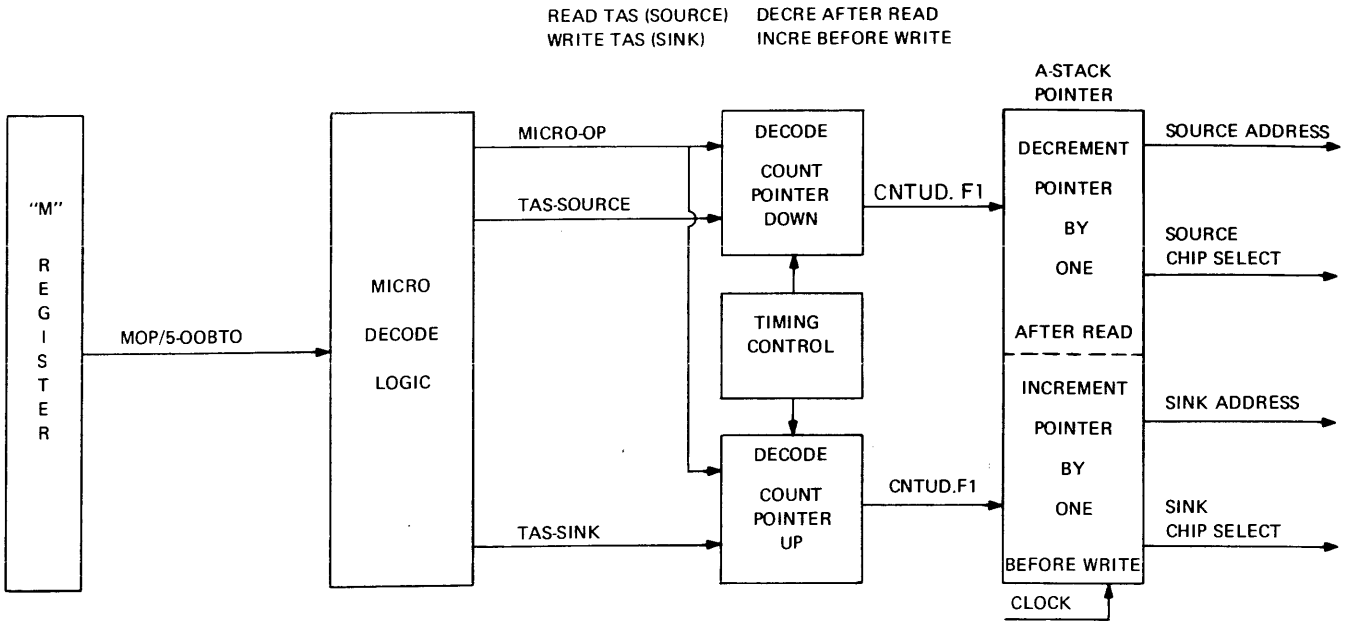
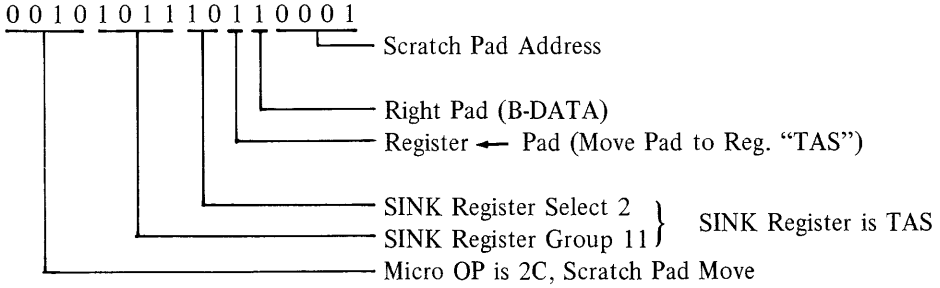


Fig. II-43 LOCAL MEMORY ..... ADDRESS/CHIP SELECT GENERATION BLOCK DIAGRAM

√ THEORY OF OPERATION

The micro currently executing is held in the M-Register and exposed to the Micro Operator Distribution Bus Lines (MOP 15-OOBTO). The Micro on the distribution bus lines is decoded throughout the system. When as a result of this decoding, the A-Stack is designated as either the source or sink, logic is generated which either down counts or up counts the A-Stack Pointer by one. When the A-Stack is designated as the source, the pointer is decremented by one after the read occurs. When the A-Stack is designated as the sink, the the Pointer is incremented by one before the write occurs.

When Top of the A-Stack "TAS" is designated as the source, the level CNTDN.F1 is generated which causes the value of the Pointer to be decremented by one after the read occurs. Therefore, the current value of the pointer which is referred to as TAS, before the decrement occurs, generates the source address and chip select levels. When TAS is designated as the sink, the level CNTUD.F1 is generated which causes the Pointer to be incremented before the write occurs. Therefore, the value of the pointer, after the increment occurs, will generate the sink address and chip select levels. Figure II-44, A-Stack Pointer/Source & Sink Generation, illustrates the detailed decoding of the 2C Micro, Source Address and Chip Select and Sink Address and Chip Select. The format of the 2C Micro used which generates the logic shown in Figure II-44 is as follows:



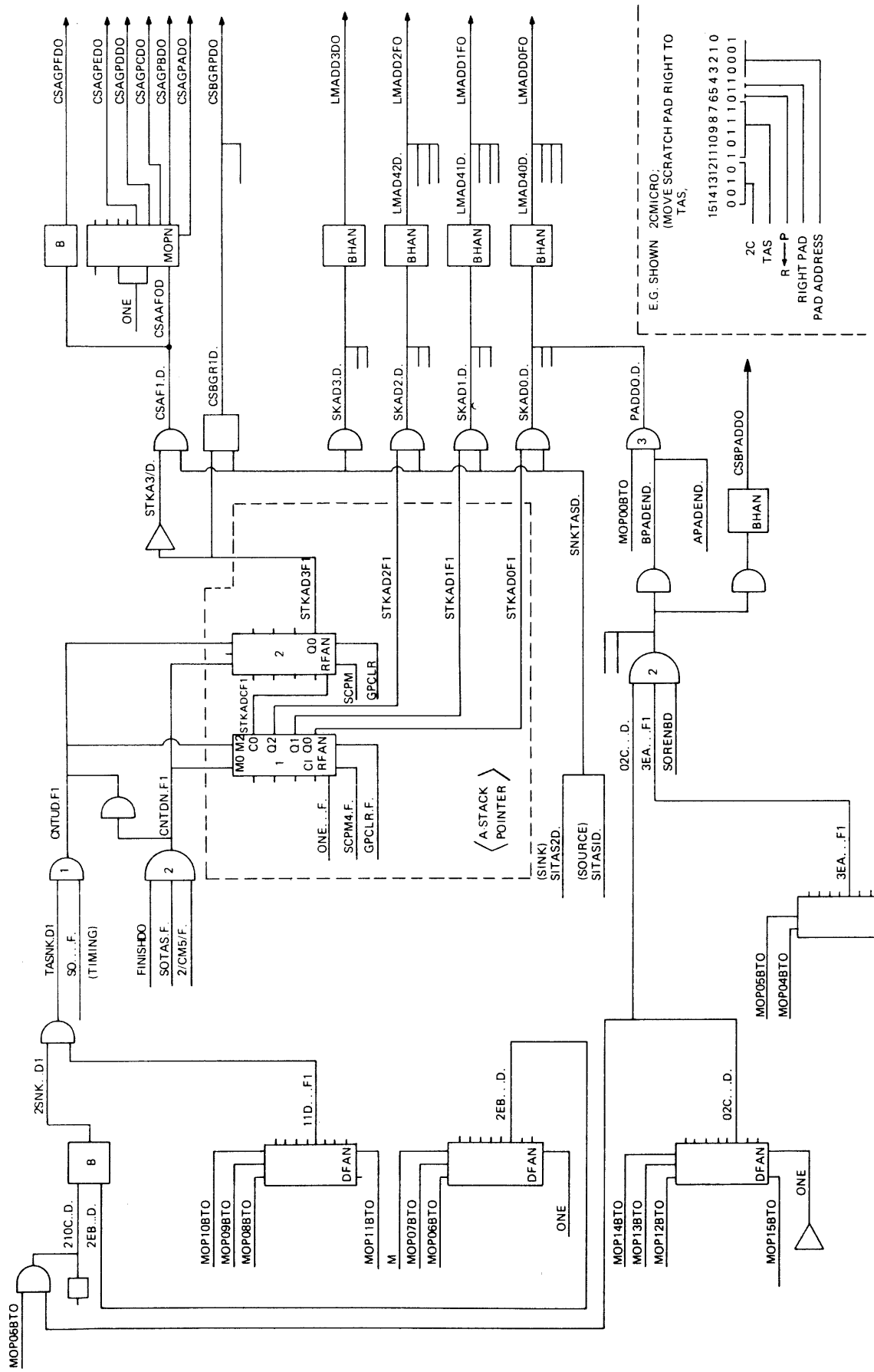


Fig. II-44 A-STACK POINTER SOURCE AND SINK GENERATION

Note that Figure II-44 illustrates only the logic that pertains to the above format. The Pointers inputs and outputs are shown in detail. If another word of Scratch Pad Right were designated as sink, then similar logic would be generated. Example: Assuming the 2C Micro with the above format is in the M-Register and exposed to the Micro Operator Distribution Bus Lines (MOP 15 through OO BTO), these Mop lines are inputs to decoding logic throughout the system. Four terms are generated as the result of this decoding; 2EB. . D., 11D. . .F1, 02C. . .D., and 3EA. . .F1. As a clock is not required for the operation of a DFAN, the four outputs are generated in approximately 12ns after the inputs are present. The four outputs have the following definitions.

11D. . .F1 Indicates the Register Group (Sink) is 11
2EB. . .D. Indicates the Register Select (Sink) is 2
} Sink Register is "TAS"

02C. . .D. Indicates the 2C Micro

3EA. . F1 Indicates Register ← Pad (Right Scratch Pad).

These four levels indicate the 2C Micro, Move Right Pad to TAS. With the Sink and Source (TAS and Pad Right respectively) now established, further decoding to generate the addresses and chip select levels is under control of Micro timing.

FUNCTIONAL DETAIL

When the control timing logic develops the level S0 . . . . F., gate No. 1 is enabled which causes the level CNTUD . F1 to be true. When true and the trailing edge of the next SCPM4.F. occurs, the current value of the Pointer is incremented by one. The Pointer consists of RFAN's (1) & (2). As the Pointer is incremented before the write occurs, by incrementing the Pointer at SO time, it will be pointing to the incremented address when sink enable (SNKTASD) is ture. The four outputs of the Pointer (STKAD 3 through 00 F1) will therefore generate the sink address and sink chip select levels for a word of A-Stack pointed at after the incrementation of the pointer occurs. This word of A-Stack is referred to as the Top of the A-Stack (TAS).

When STKAD3F1 is false, CSAGPF through A DO will be true. With the chips select levels true, a word of A-Stack (0 through 7) is addressed as per the value of STKAD 2 through 0 F1. when SNKTASD. is true. Assuming a General Processor Clear initially reset the Pointer to zero, then after the increment occurs the STKADOF1 output of the Pointer will be true. This will cause LMADDOFO to be true at SNKTASD. time. Word No. 1 of A-Stack will be addressed. When TAS is designated as ink, then SITAS2D. will be true at sink time. STKAD3F1 true indicates Words 8-15 of A-Stack are to be addressed as per the value of STKAD 2 through 00 F1.

When TAS is designated as the Source, SITAS1D. will be true, causing SNKTASD. to be true. The Pointer is decremented, after the source address and chip select levels are used with CNTDN.F2. The operation of the Pointer is explained separately during A-Stack Pointer which follows. Figure II-44 also illustrates the generation of the source address and chip select levels generated as the result of executing the 2C Micro with the format given previously. When the source enable term (SORENBD.) is true, gate 2 outputs a ture. As the format used indicated Mop bit 0 thru, gate 3 is enabled thus generating the term PADDO.D. which becomes LMADDOFO. Gate 2 true also causes the term CSBPADDO to be true. With CSBPADDO and LMADDOFO true, word No. 1 of Right Scratch Pad (B-DATA) is addressed as the source Scratch Pad word. Note that the source occurs before the sink.

A-STACK POINTER

The A-Stack Pointer consists of two 3-bit Registers (RFAN's) which are shown on Figure II-44, A-Stack Pointer. Associated with the Pointer are two Mode Control inputs (CNTDN.F1 & CNTUD.F1). CNTUD.F1 when true, causes both 3-bit registers to be in the add mode (M2 input true). CNTDN.F1 when true, causes both 3-bit registers to be in the subtract mode (M0 and M2 inputs true). The carry input to Register No. 1, (ONE. . .F.) is a constant true level. With this constant true to the carry input (C1), the carry out (C0) output of Register No. 1, (STKADCF1) is true when the following conditions are true.

1. When in the ADD Mode (CNTUD.F1 true) and outputs Q2 (STKAD2F1), Q1 (STKAD1F1), and Q0 (STKAD0F1) are true. This allows a carry input to Register No. 2 to be sensed immediately.
2. When in the SUBTRACT Mode (CNTDN.F1 true) and the Q2, Q1, and Q0 outputs of Register No. 1 are false. This allows a borrow out to be sensed immediately at the carry input to Register No. 2.

The four outputs of the Pointer (STKAD 3 through 0 F1) determine the address lines and chip select levels of the current word No. of A-Stack 0 through 7 (A-DATA0 and 8 through 15 (B-DATA). This current address of the A-Stack is referred to as TAS (Top of the A-Stack). The Q2, Q1, and Q0 outputs of both registers change state on the trailing edge of the clock pulse (SCPM4.F). The carry out or borrow out level of Register No. 1 does not require a clock pulse to be true, but only the conditions listed previously.

FUNCTIONAL DETAIL–WRITE TAS

For the purpose of explanation, assume a General Processor Clear pulse (GPCLR.F.) has occurred which sets both registers to a value of zero (Q2, A1, A0 and carry out (C0) levels false). When a micro is then executed which designates TAS as sink, the term CNTUD.F1 will become true which causes both registers to be in the ADD Mode. The trailing edge of the next clock pulse will set Register No. 1 to a value of one. The Q0 output (STKAD0F1) is now true. If another Micro is executed designating TAS as sink, the register is again incremented by one which causes the Q1 output to go true and the Q0 output to go false. Successive operations when TAS is designated as sink will cause the Pointer to increment by one with each trailing edge of the clock pulse when the mode control inputs indicate ADD.

The pattern of the output levels which will occur when successive increment operations occur is illustrated in the Timing Diagram, Figure II-45, A-Stack Pointer Increment. Note that when STKAD 0, 1, and 2 F1 are true, and the ADD mode input is true, the carry out (CO) level STKADCF1 is also true. This carry out level is then true to the carry input of Register No. 2 causing the Q0 output (STKAD3F1) to go true with the trailing edge of the next clock pulse. The STKAD3F1 output of the Pointer therefore determines whether word No's. 0 through 7 or No's. 8 through 15 are to be addressed. When the Pointer "points" to word No. 15, the next write operation (Sink TAS), will cause the Pointer to again point to word No. 0. The pointer therefore wraps around, pointing to the same word of A-Stack that was pointed at after the General Processor Clear Occurred. It should be noted that the term CNTUD.F1 on Figure II-46 is shown continually true, only for explanation purposes, to indicate the count of the Pointer, the word number addressed, and the rap around occur (Sink TAS).

During normal operation, when successive write operations occur, the term CNTUD.F1 will be true for one clock period only, which allows the Pointer to be incremented by one only once during the execution of each Micro designating TAS as sink. The Control Logic will cause the increment to occur before the write occurs. Timing of the Control Logic is explained during the explanation CNTUD.F1 and during the explanation of the individual execution of Micros.

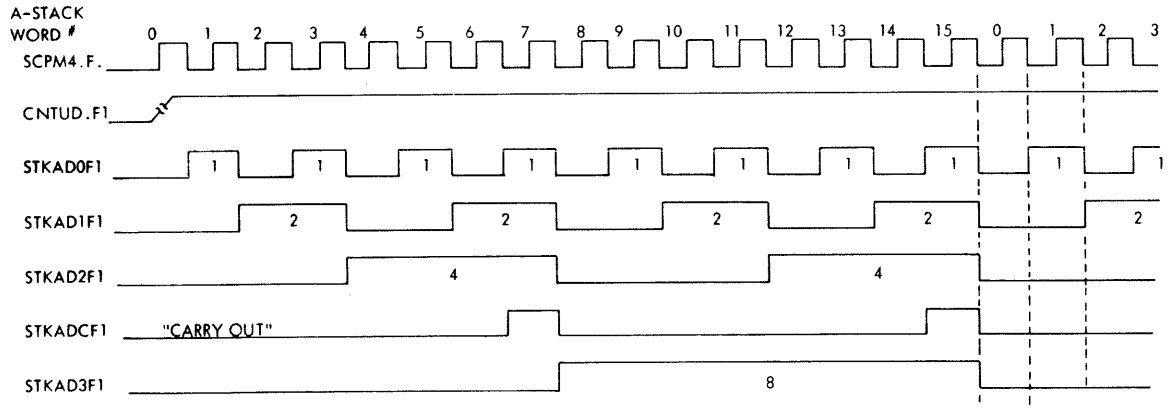


Fig. II-45 A-STACK POINTER INCREMENT (WRITE)

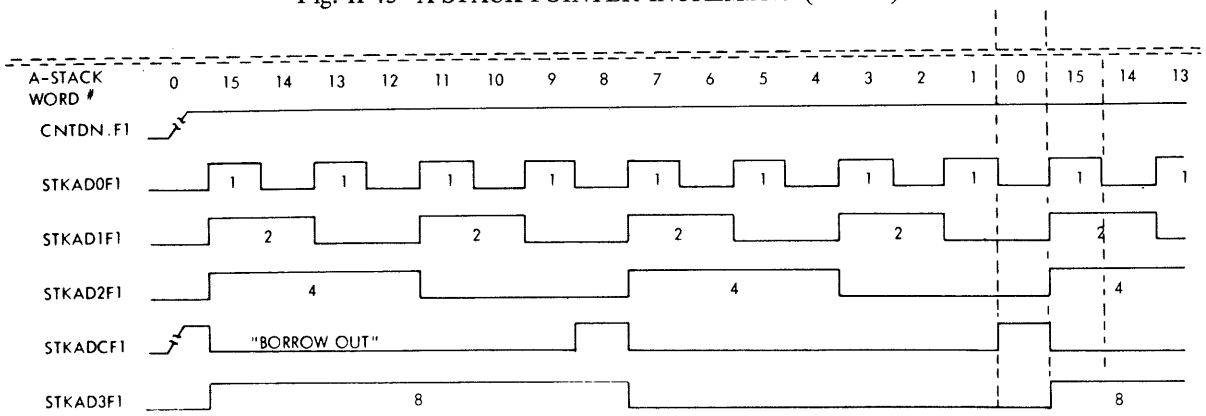


Fig. II-46 A-STACK POINTER DECREMENT (READ)

FUNCTIONAL DETAILS–READ TAS

When successive read operations are executed (Source TAS), the Pointer is decrement by one to the values illustrated in Figure II-46. Note that if initially set to zero, the first decrement to occur will cause the outputs (STKAD 3 through 0 F1) to go true. This addresses word No. 15 which is B-DATA. During read operations, the pointer is decremented after the read occurs. Timing is explained during the explanation of CHTUD.F1 and CNTDN.F1 as well as during the explanation of the execution of micros. CNTDN.F1 is shown continually true for explanation purposes only as was CNTUD.F1. Successive read operations also cause the wrap around procedure to occur.

LOCAL MEMORY WRITE TIMING

The Local Memory Write Enable pulse (LMWE. .F0) occurs when SCPM8.F. (8 MHz clock pulse) and Chip Select SINK (CSSINKF1) are true. Refer to Figure II-47. The decoding logic which generates CSSINKF1 is primarily concerned with the type of MICRO and the timing; therefore additional logic is provided to decode the actual Chip select levels necessary to select a particular storage area within Local Memory. Refer to CSSINKF1 explanation for the conditions which generate the same.

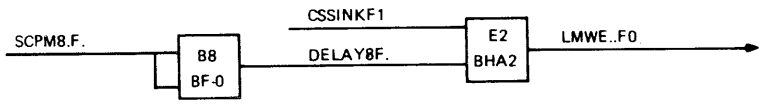


Fig. II-47 LOCAL MEMORY WRITE ENABLE

Local Memory Write Timing is shown in Figure II-48 and illustrates the occurrence of LMWE. .F0 during T1 time when the 7C Micro is executed. LBUF receives the contents of the Main 24-Bit Exchange at the trailing edge of CLK4/ as shown. The MAR(A) address is stored in TEMB during SO time of the 7C Micro.

READ TIMING

Local Memory Read time occurs any time the address and Chip Select levels are present. (LMWE. .F0 is quiescently false.)

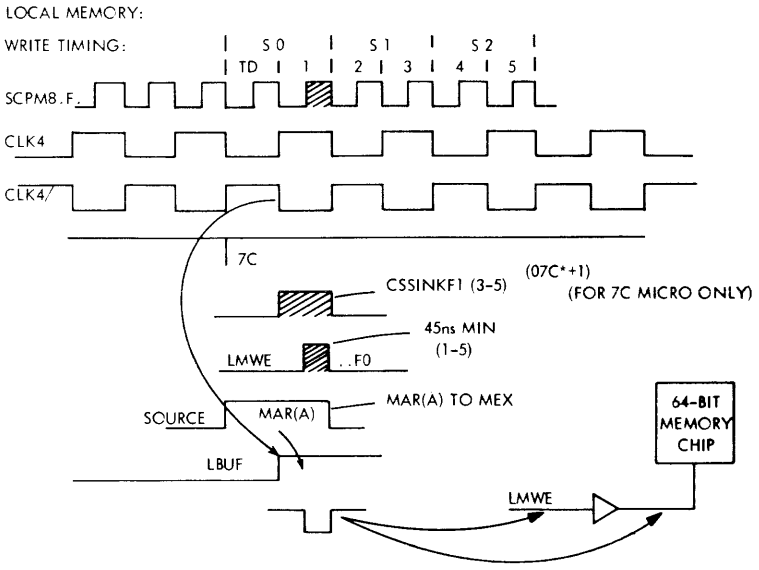


Fig. II-48 LOCAL MEMORY WRITE TIMING

CSSINKF1

Figure II-49 illustrates the basic conditions which, when true, generate CSSINKF1.

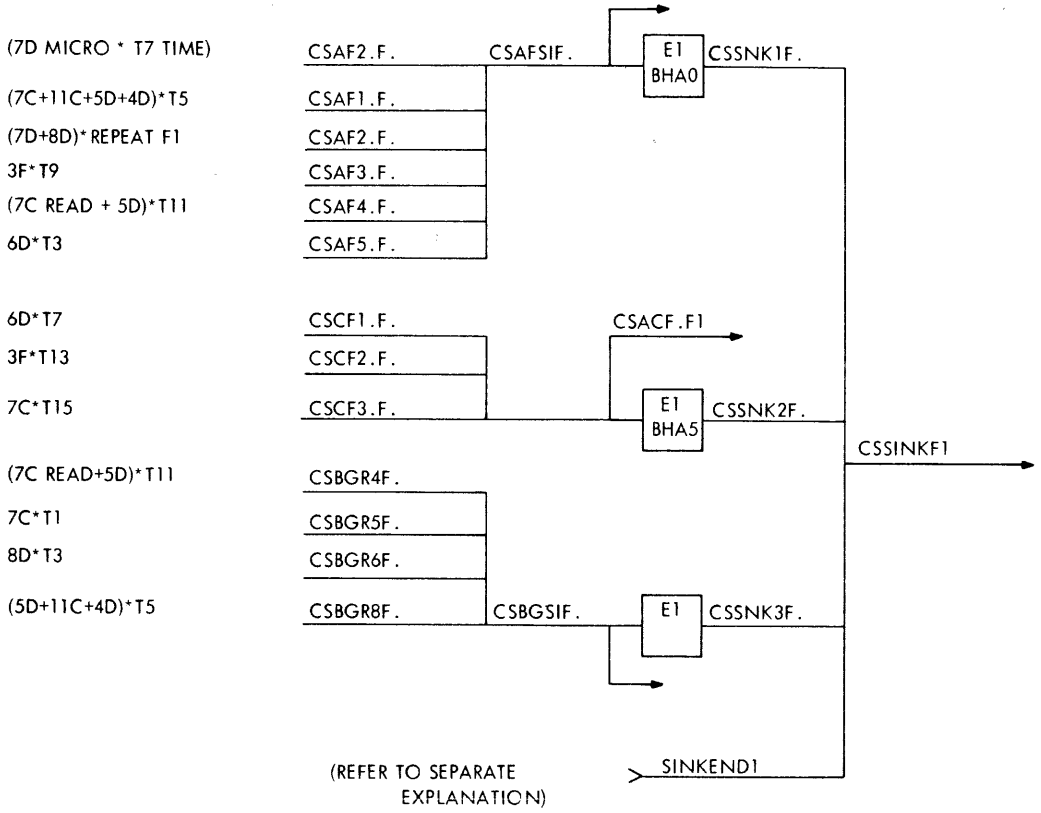


Fig. II-49 CSSINKFO DECODING

24 BIT FUNCTION BOX INTRODUCTION

The 24 Bit Function Box, located on Processor Cards A and B, is normally used to perform the common functions between two operands. These functions include a SUM, DIFFERENCE, AND, OR, EXCLUSIVE OR, COMPLEMENT and MASK of the operand data.

DATA STORAGE

The operand data is stored in the X and/or Y Registers dependent upon the desired operation. A typical example would be a SUM operation where the Addend and Auguend are placed in the X and Y Registers respectively. If the SUM output is designated then a Binary or 4 Bit BCD add operation will occur with the output being placed on the Main Exchange and sinked into a destination register. If data is to be complemented or masked it may be placed in either the X or Y Register and by designating either the Complement of X or the Complement of Y, the desired output may be obtained. In the example of the Complement, only one of the two registers contained operand data.

OUTPUTS

The following is a list of outputs from the Function Box which are considered 24 Bit Functions:

SUM	X plus Y
DIFF	X minus Y
CMPX	Complement of the X Register
CMPY	Complement of the Y Register
XANY	Logical "AND" of the X and Y Register

XORY Logic "OR" of the X and Y Register
XEOY Logical "EXCLUSIVE OR" of the X and Y Register
MSKX Mask of X Register Data (Controlled by CPL)
MSKY Mask of the Y Register Data (Controlled by CPL)

The above operations are all under direct control of the CP Register. The CP Register controls either length or mode of the operation or both length and mode. Mode is defined as being either Binary or 4 Bit Binary Coded Decimal (BCD).

4 BIT RESULTS

The 24 Bit Function Box also produces various 4 bit results which are referred to as pseudo registers. These pseudo registers are XYST (X-Y States), XYCN (X-Y Conditions) and BICN (Binary Conditions). The pseudo registers are available as outputs only and may be inputs to the 4 Bit Function Box where the contents of the pseudo registers can be examined by the 4C or 5C Bit Test micros.

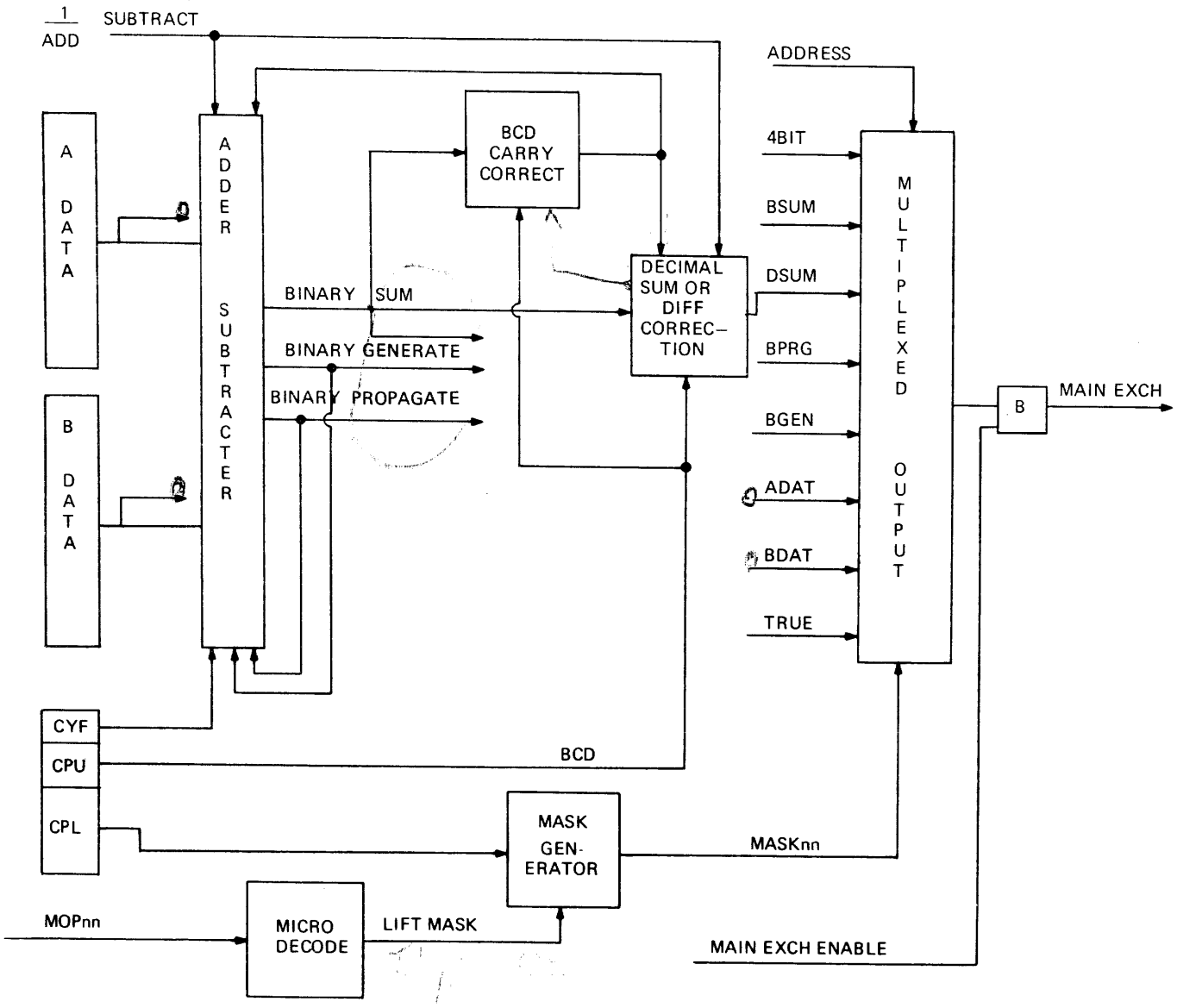


Fig. II-50 BLOCK DIAGRAM 24 BIT FUNCTION BOX

INCREMENT/DECREMENT

In addition to the normal 24 Bit Functions, the 24 Bit Function Box is used by various micros which require increment and decrement functions. The adder/subtracter of the Function Box is therefore shared with these micros. The micros which require use of the adder/subtractor are 7C Read/Write Memory for counting of FA and/or FL, 6D Count FA/FL, 8D Scratchpad Relate FA and 3F Formalize X.

DATA PATH

Due to the structure of the machine, the Function Box also receives all data from the Local Memory and passes it to the Main Exchange. In this case the 24 Bit Function Box will not alter the data but become a transparent path to the Main Exchange.

BLOCK DIAGRAM

The Block Diagram in figure II-50 illustrates the 24 Bit Function Box and the outputs to the Main Exchange. Also illustrated in figure II-50 is the output of Local Memory to the Main Exchange (ADAT and BDAT). Now shown in this figure are the four bit results obtained by the Function Box. These four bit results will be discussed individually.

24 BIT FUNCTION BOX CONTROL

Control of the 24 Bit Function Box encompasses a large area due to the fact that the Function Box is shared by various micro operations. The Control Logic described will discuss the control of the add/subtract mode, binary BCD mode, carry control, input control and output control. The first of these to be discussed will be the add/subtract mode control. Figure II-51 illustrates the inputs for control of the add/subtract mode. If the SUB. . . .DO term is true then B DATA will be subtracted from the A DATA and conversely if SUB. . . .DO is false the A DATA and B DATA will be added.

SUBTRACT

The gates shown in Figure II-51 if enabled will place the Arithmetic Unit in the Subtract Mode. Each of the gates are enabled depending upon the current micro in the M Register, variants of that micro and controlled for timing by the Sequencer outputs. The gates have been assigned an alphabetic designation and are discussed accordingly.

GATE A — Gate A is enabled for the 7C Read/Write Memory micro during the first half of the micro execution time. This is done provided that M0P10BTO is true indicating that FA is to be downcounted.

GATE B — Gate B is enabled anytime a Register Move type micro uses the Difference Register as the source. DIFF is indicated by SOCOL3D (Source Column 3) and 08D. . .F1 indicating Register Group Eight.

GATE C — Gate C is enabled for the 8D Scratchpad Relate FA if MOPO4BTO is true indicating the value in Scratchpad is a negative value and therefore a subtract must occur.

GATE D — Gate D is enabled for the 6D Count FA/FL if the FA Register is to be downcounted.

GATE E — Gate E is enabled for the 3F Normalize X micro in order to downcount the FL Register.

GATE F — Gate F is enabled for the 6D Count FA/FL if the FL Register is to be downcounted.

GATE G — Gate G is enabled for the 7C Read/Write Memory if the variant specified that the FL register is to be downcounted.

The result of the various subtract operations is placed on the Main Exchange under control of the output selection control logic.

BINARY/BCD

The Binary/BCD Mode of the Arithmetic Unit within the processor is handled by basically two controlling factors. The first of these factors is the current micro in the M Register. If the micro is a 7C Read/Write Memory, 6D Count FA/FL, 8D Scratchpad relate FA or 3F Normalize X then the Adder/Subtractor is always in the Binary Mode of operation. If, however, the SUM, DIFF or BICN Registers are selected as a source for a Register Move "type" micro then the mode is controlled by bits five and six of the CP Register which are referred to as CPU. With CPU equal to 00 the mode is Binary and if CPU is equal to a 01 then the mode is BCD. Any other bit configuration of the CPU Register is undefinied. With the BCD mode specified, a correction must be done to the initial result of the Add or Subtract and this is done by either adding or subtracting a value of six (0 1 1 0) from each of the modulo sixteen stages. In addition to that, the various carriers must be corrected if the operation is an add. The BCD correction is discussed in detail with the description of the SUM and DIFFERENCE operations.

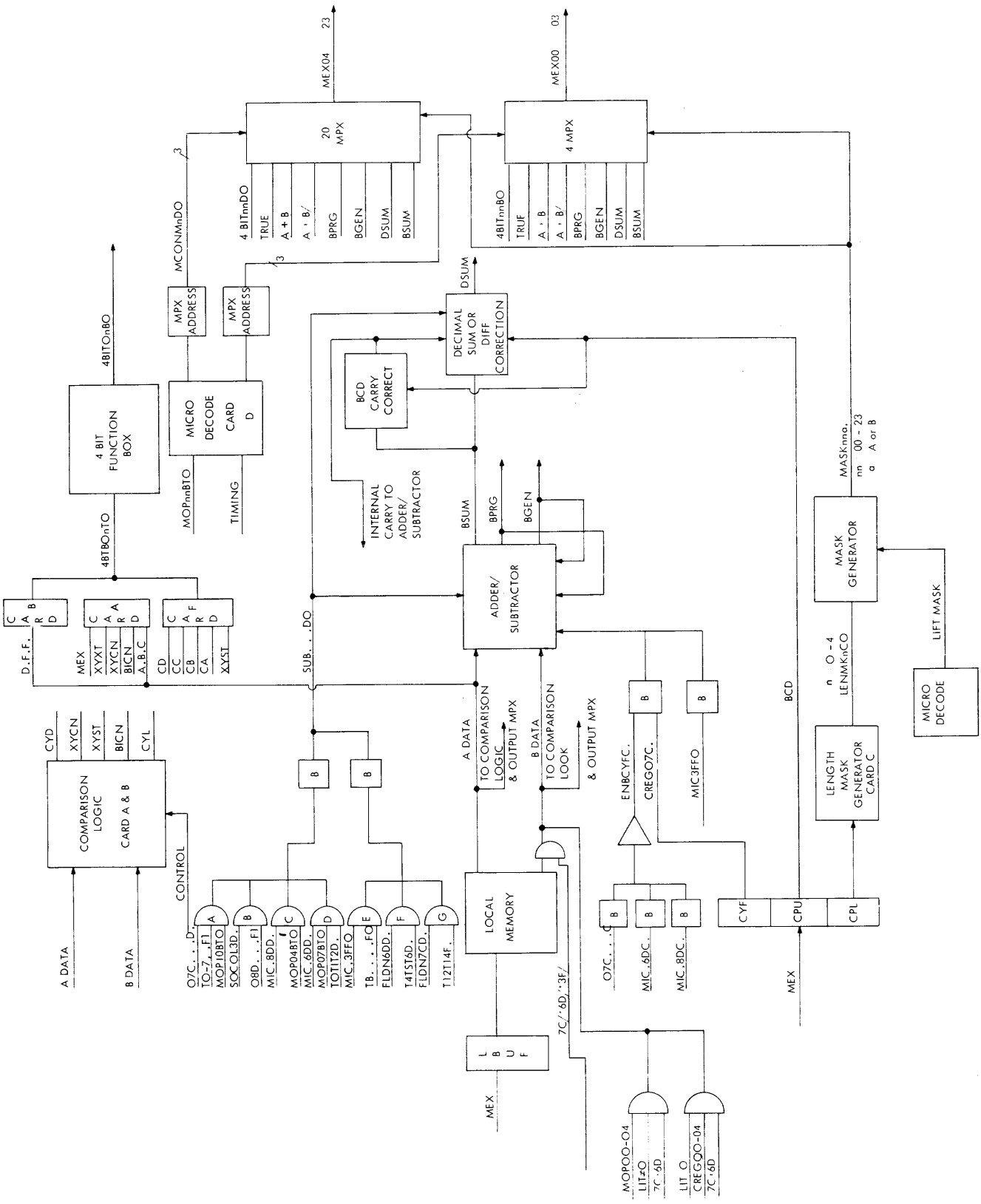


Fig. II-51 THRU Fig. II-54

CARRY F/F INPUT

The Carry Flip-flop input control is performed on Card C. The various operations can either inhibit CYF into the Arithmetic Unit, force CYF to the Arithmetic Unit or allow the current state of CYF to the Arithmetic Unit. During Add operations, CYF is a carry into the adder and on subtract operations, CYF is a borrow from the subtractor. Those operations which explicitly inhibit the CYF input to the Arithmetic Unit are the 7C Read/Write Memory, 6D Count FA/FL and 8D Scratchpad Relate FA. The 3F Normalize micro on the other hand forces CYF true as a borrow out from the Subtractor which will allow the value "one" to be subtracted from FL during the Normalize X operation. During any other time, the state of CYF will be enabled to the Arithmetic Unit and its use will be a function of the operation being performed. For example, if a SUM is sourced then CYF will act as a carry into the Arithmetic Unit and if DIFF is sourced then CYF will act as a borrow from the Arithmetic Unit. Figure II-52 shows the control of CYF (CREG07) to the Arithmetic Unit.

INPUTS AND SELECTION

Inputs to the 24 Bit Function Box are "A" DATA and "B" DATA, disregarding the Control inputs such as CP and other controls. "A" DATA will be the Augend for an add operation and the Minuend for a subtract operation. "A" DATA is obtained by reading the contents of Local Memory with the register read being output onto the "A" DATA lines. Those registers which are used for A DATA are the X Register for arithmetic operations, FA Register for the 7C or 6D micro and FL for either the 3F, 6D or 7C micros. It is not the function of this discussion to provide the information for addressing and timing functions of these micros but only to discuss the data in relation to the Arithmetic Unit of the 24 bit Function Box. If information is needed as to the reading of Local Memory or the timing, refer to the appropriate section of this manual.

The B DATA is obtained in a slightly more complex manner as it is the variable in the operations which can be performed. First consider the normal arithmetic operation where the SUM or DIFF is referenced as the source. The micro which is specifying either of these registers as a source will cause a read of both the X and Y Register from Local Memory. The X Register becomes A DATA and the Y Register becomes B DATA. The input having been obtained, either a subtract or add will occur with the result being sent to the sink register. This is the simplest of the B DART operations. Using the 7C micro, B DATA is obtained on Card C from either the Literal within the micro, or the value in CPL if the literal is equal to zero. The 6D micro like the 7C, obtains B DATA either from the Literal within the micro or from CPL. The 8D Scratchpad Relate FA is the most complex of the micros discussed. B DATA for the 8D Scratchpad Relate FA is the contents of one of the locations of Left Scratchpad. However, in reviewing the Local Memory section it can be seen that Left Scratchpad Data is normally obtained on the A DATA output. The 8D micro, therefore, must initially read the contents of Left Scratchpad onto the A DATA output and then write the contents into TEMP B which is in the B DATA portion of Local Memory.

When the actual increment/decrement occurs, the FA Register is read from Local Memory as ADATA and TEMPB is read from Local Memory as BDATA. Both outputs of Local memory are then sent to the Arithmetic Unit of the 24 Bit Function Box and the Add/Subtract operation is performed according to the sign of the data in scratchpad. The remaining operation which requires a decrement is the 3F Normalize X. The contents of FL are input as A DATA and BDATA inputs are supressed. The decrement is done by forcing CREG07 (CYF) true which in the subtract mode is a borrow out level and will therefore cause the contents of FL to be downcounted by one. Figure II-53 illustrates the selection of the BDATA input to the Arithmetic Unit.

OUTPUT SELECTION CONTROL (Refer to Figure II-50)

The output of the 24 Bit Function Box is controlled by a series of multiplexor elements on Cards A and B with the least significant twelve bits on Card A and most significant twelve on Card B. The enable input to each of the multiplexors is a mask bit from the Mask Generator located on Cards A and B. The Mask Generator will be discussed as a separate item. A specific multiplexor having been enabled by the mask, it is the function of the address lines to select the appropriate output to the Main Exchange. It should be noted that the output of the multiplexors do not immediately gate to the Main Exchange but are sent through a buffer which must be enabled before the output to the Main Exchange is allowed.

MULTIPLEXOR INPUTS

Figure II-50 shows one of these multiplexor elements with the associated inputs and addressing.

The following is a description of the various inputs to the Multiplexor and their use.

4BITOnBO — This input is from the output of the 4 Bit Function Box. The multiplexor's (4) on Card A allow for this output to be placed on the Main Exchange least significant four positions if the operation is a 4 to 24. If the operation is a 4 to 4 or 24 to 4 then the multiplexors (24) on Card A and B are enabled to place six copies of this data on the Main Exchange.

TRUEO1A. — This input is a constant true level and is gated into the Main Exchange where it is sent to the Rotator for those micros which require a shift or rotate operation.

A+B.nnA. — This input will contain either ADATA, BDATA or both. The both function is for obtaining an "or" function to produce the XORY Register output. ADATA in this case is the X Register and BDATA is the Y Register. For normal Register Move type operations or operations where a register's contents must be placed on the Main Exchange, the Register is read from Local Memory and placed on ADATA or BDATA and gated to the Main Exchange accordingly. An example of this would be if a 1C Register Move indicated "move" T Register to nn Register. The T Register contents would be read from Local Memory, be output on the ADATA lines and sent to the multiplexor elements. The multiplexor elements would then gate the ADATA to the Main Exchange and from there to the destination.

A+B/nnA. — This input is either inverted ADATA or inverted BDATA. This input is selected for either CMPX or CMPY.

BPRGnnA. — Binary Propagate is the output of the Arithmetic Unit of the 24 Bit Function Box. This is an input to the multiplexor to produce the XEOY function.

BGENnnA. — Binary Generate is the output of the Arithmetic Unit and is used to produce the XANY function.

BSUMnnA. — Binary Sum is the output of the Arithmetic Unit and will contain either the SUM of DIFF depending upon the register which has been selected as a source.

DSUMnnA. — Decimal Sum is the output of the Arithmetic Unit decimal correction section and will contain either the decimal SUM or DIFF depending upon the register which has been designated as a source.

MULTIPLEXOR ADDRESSING

Each of these inputs are addressed by either a MEXCMnDO term or a MCONMnDO term. The least significant four bits are addressed by MEXCMnDO and the most significant four bits are addressed by MEXCMnDO. This split of the multiplexor's is due to the various combinations of register move type micros. Those combinations being 24X24, 24X4, 4X24 and 4X4. Figure II-55 illustrates how the MEXCMnDO and MCONnDO terms are produced and as can be seen from the diagram the only difference is the 4BITn.DO term on the uppermost input to the EFAN's.

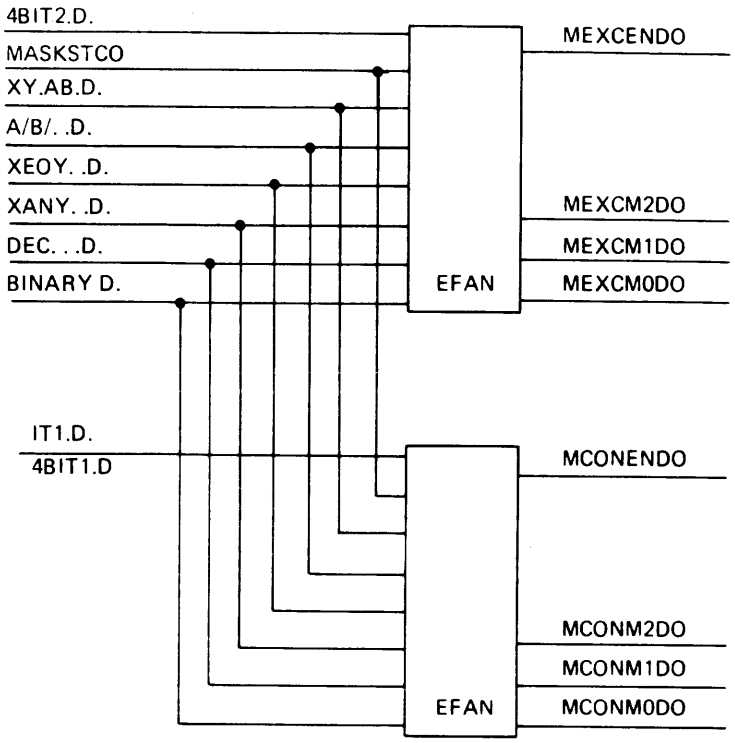


Fig. II-55 MULTIPLEXOR ADDRESSING (CARD D)

ADDRESSING EXAMPLE

Using an example to explain the addressing, assume that the X and Y (XANY) function has been designated as a source. The term XANY. .D. will cause the top EFAN to produce MEXCENDO and MEXCM1DO. The same term to the bottom EFAN produces corresponding outputs; MCONENDO and MCONM1DO. All four of these terms are sent to Card A and Card B where they will address the BGENnnA. input to the multiplexors to the MDATnnA. output (refer to Figure II-54). The terms MEXCENDO AND MCONENDO are used to enable the buffers to allow the MDATnnA. output onto the Main Exchange. Note that the Mask which enables the multiplexors have not as of yet been taken into consideration therefore assume that the number of bits placed onto the Main Exchange is the number designated by CPL.

4 BIT SOURCE OR ~~SINK~~ destination

If either a four bit souce or sink is designated then the 4BITn.D. terms will have an effect upon the operation.

4X24 Operation

If a four bit result or four bit source register is required and the sink is a twenty-four bit register then the term 4BIT2.D. is true and only the least significant four multiplexor elements will be addressed. Subsequently only the least significant four bits are placed on the Main Exchange. The source data (refer to Figure II-56) is obtained from the 4 Bit Function Box, the mnemonic being **4BIT0nBO.**

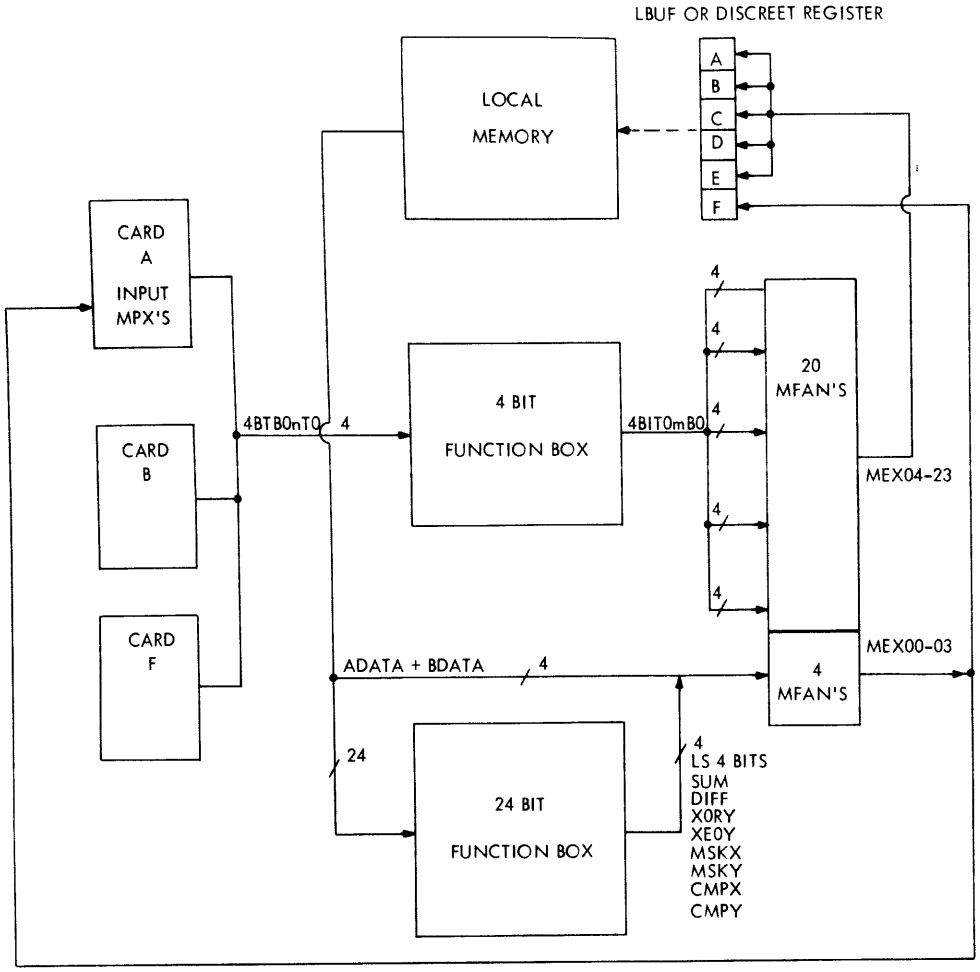


Fig. II-56

4X4 Operation

If a four bit source is designated and is to be sinked to a four bit register then both 4BIT2.D. and 4BIT1.D are true. The four bit source data is obtained from the 4 Bit Function Box and six copies of the source data is sent to the multiplexor elements. All multiplexor elements are enabled and six copies of the source data are placed on the Main Exchange. This allows the source data to be gated to any position of a destination register. Example: TA, TB, TC, TD, TE, TF. In these examples only the desired four bit portion of the sink would be addressed in Local Memory and only that four bit sink would be written at Sink Enable Time.

24X4 Operation

If a 24 bit register was used as a source and a four bit register as a sink, the term 4BIT1.D. would be true. The term 4BIT1.D. will allow the output of the 4 Bit Function Box to be gated to the upper twenty bits of the main Exchange (5 copies of the data). The original data is obtained by enabling only the least significant four bits of the source data is then sent to the 4 Bit Function Box and the 5 copies of the original data are placed on the MAIN EXCHANGE. Refer to Figure II-56. Note that the lower 4 and upper 20 multiplexors have a different address.

In Figure II-56 24X4, the sink data is either sent to a discrete register such as CA, CB, CC, CD or may be written into one of the 4 bit registers in Local Memory. If the data is written into Local Memory, it is first stored in LBUF and then written into the 4 bit addressed location. If the 24 Bit source is a result of the 24 Bit Function Box, the X and Y Registers must first be read and sent to the Function Box. On the output of the Function Box, only the least significant four bits are sent through the 4 Bit Function Box where five copies are produced and distributed to the upper 20 bits of the Main Exchange. It should be emphasized that Figure II-57 represents only a 24 to 4 type of operation.

OUTPUTS TO AUXILLIARY 4 BIT BUS

In addition to the outputs to the Main 24 Bit Exchange, the 24 Bit Function Box provides an output to the 4 Bit Auxilliary Bus. The outputs to the 4 Bit Auxilliary Bus provided for on Card A are for the BICN, XYCN, XYST and FLCN result registers. Card A also provides an output to the 4 Bit Auxilliary Bus for ADATA. The significance of the ADATA to the Auxilliary Bus is if a 4 Bit Register is addressed as a source. The A DATA portion of Local Memory is that portion which may be addressed as four bit registers. Card A provides the path for the least significant 12 bits of ADATA to the 4 Bit Bus. (Only 4 of the 12 may be selected at any one time). Card B provides the path for the most significant 12 bits of ADATA to the 4 Bit Bus. (nly 4 of the 12 may be selected at any one time and of the total 24 only 4 can be selected by properly addressing the multiplexor elements). The Figure II-57 shows the sets of multiplexor elements on Card A and B to the 4 Bit Auxililliary Bus. Card F also provides a path to the Bus but is not within the scope of this discussion.

4 BIT AUXILLIARY BUS OUTPUT SELECTION

As can be seen from Figure II-57 the various 4 bit results such as XYST, XYCN, BICN and FLCN are selected on Card A by a series of multiplexor elements. In addition to the four bit results, the ADATA output of Local Memory or the contents of the Main Exchange least significant four bits may be placed on the Auxilliary Bus. The multiplexors are addressed and enabled by decoding logic which is developed on Card D. The following discussion will describe the input to the multiplexors according to the address and function.

1. ADDRESS 7 MAIN EXCHANGE TO 4 BIT AUXILLIARY BUS
   The data on the Main Exchange least significant four bits may be placed on the Auxilliary Bus as na input to the 4 Bit Function Box when a 24 bit source register has been designated to be placed in a 4 bit sink register. This operation has been previously described in the 24 Bit Output Section of the 24 Bit Function Box. To review however, it is the function of this operation to place the least significant four bits of the source data into the 4 Bit Function in order to produce five copies to be placed on the Main Exchange in addition to the original.
2. ADDRESS 6 X-Y STATES TO 4 BIT AUXILLIARY BUS
   With an Address of 6, the XYST result register is gated to the 4 Bit Auxilliary Bus. The input to bit 3 is LSUX. .A. which indicates the least significant bit of the X Register is true if the mode is binary or if the mode is BCD then LSUX indicates the least significant four bits of X are equal to nine (1 0 0 1). Bit 2 input is not obtained from Card A for the XYST but instead produced on Card F. Bit 2 is the Interrupt "or" which is an or of CC0, CC1, CC2 and CD3. The input for bit 1 is B0-23.A. which indicates that one of the BDATA bits (Y Register) is on true therefore the BDATA (Y Register) is not equal to zero (Y≠0). The final bit, bit zero, for the XYST is X≠0 and the input term is A0-23.A. indicating an ADATA bit is on true (X Register Bit) and therefore X≠0 is true.

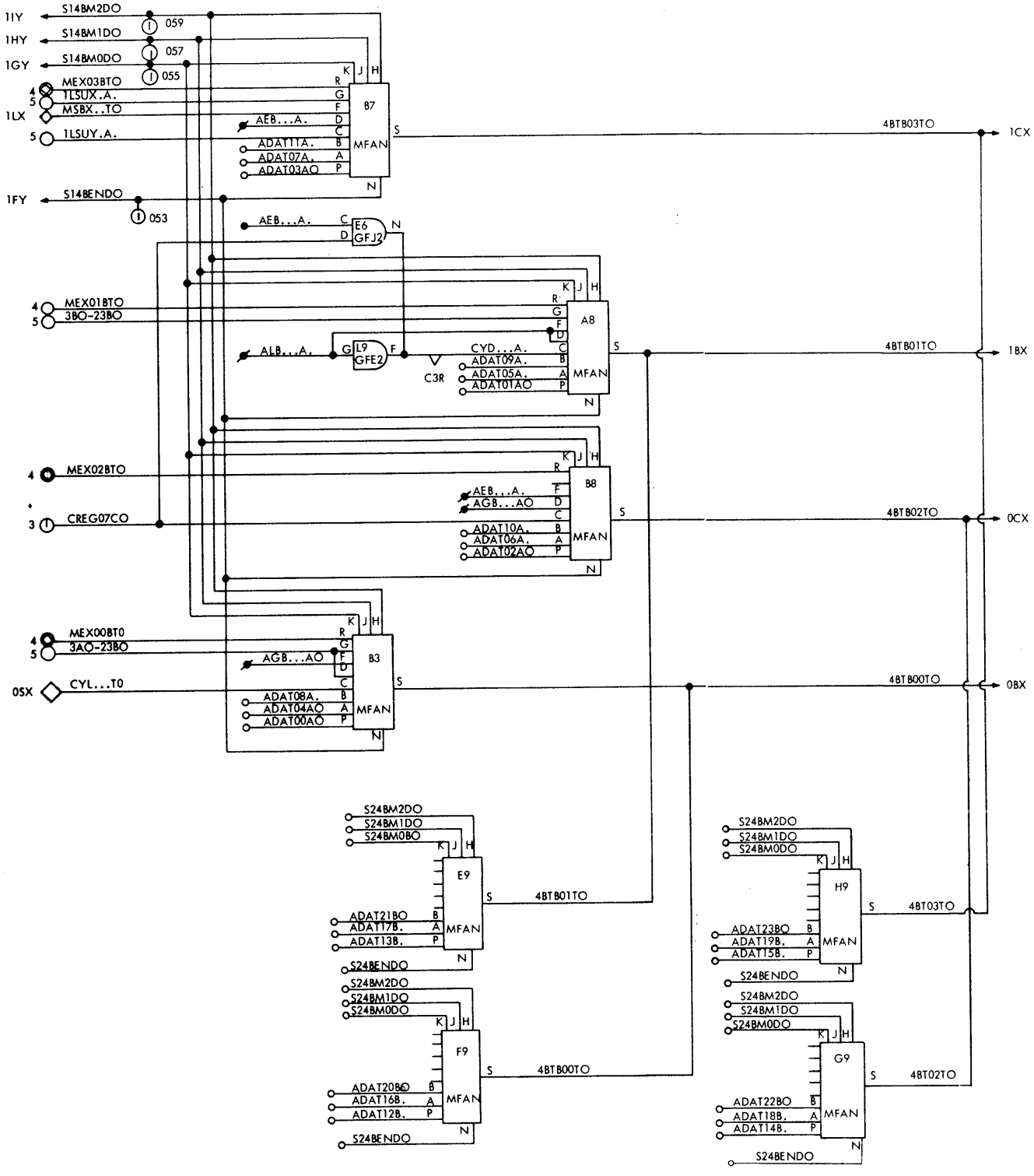


Fig. II-57 24 BIT FUNCTION BOX OUTPUT TO 4 BIT AUXILIARY BUS

3. ADDRESS 5 X-Y CONDITIONS TO 4 BIT AUXILLIARY BUS
   The Address of five will allow the XYCN result register to be gated to the 4 Bit Auxilliary Bus. Bit 3 input to MSBX. .TO which indicates the most significant bit (determined by CPL) of the X Register is equal to a "1". Bit 2 input is AEB. . .A. which indicates ADATA is equal to BDATA, ADATA being the X Register and BDATA being the Y Register. Thus the term or bit X=Y is true for the XYCN. Bit 1 input term is ALB. . .A., A Less Than B, which indicates ADATA is less than BDATA and therefore X is less than Y. Bit 0 input isis AGB. . .A0 indicating ADATA is greater than BDATA and therefore X is greater than Y.
4. ADDRESS 4 FIELD LENGTH CONDITIONS TO 4 BIT AUXILLIARY BUS
   The Field Length Conditions (FLCN) are a comparison between the Field Length Register (FL) and SFL Register which is a portion of word zero Right Scratchpad. In order for the comparison to occur, the data must be read with FL being placed on the A DATA output of Local Memory and SFL placed on the B DATA output of Local Memory. Bit 3 term is AEB. . .A. indicating that FL is equal to SFL (FL=SFL). Bit 2 term is AGB. .A. indicating that FL is greater than FL. Bit 1 term is ALB. . .A. indicating that FL is less than FL. Bit zero term is AO-23.A. indicating that FL is not equal to zero (FL≠0).
5. ADDRESS 3 BINARY CONDITIONS TO 4 BIT AUXILLIARY BUS
   The Binary Conditions result register is a check of the various Carry/Borrow terms associated with the Arithmetic Unit and also the Least Significant Unit of the Y Register (LSUY). Bit 3 input is the Least Significant Unit of Y and is true in the Binary Mode if the Least Significant bit of the Y Register if "1" or is true if in the BCD Mode, the least significant four bits of the Y Register are equal to nine (1 0 0 1). Bit 2 is the CREG07C0 input which is the Carry Flip-Flop from the CP Register (CYF). Bit 1 is the CYD. . .A. input which is a borrow level from the most significant stage of the subtractor. Bit 0 input is CYL. . TO which is the Carry Level from the most sifnificant stage of the adder as determined by CPL.
6. ADDRESS 2, ADDRESS 1, ADDRESS 0
   These three addresses are enabled to allow a four bit portion of a 24 bit register to be input into the 4 Bit Function Box. This operation is done to select one of the six portions of the total 24 bits to act as source data. When a 4 Bit Register is to be used as a source and that 4 bit register is located in Local Memory then a read of all 24 bits from Local Memory occurs. It is at this point then that only those 4 bits which are to be used are selected.

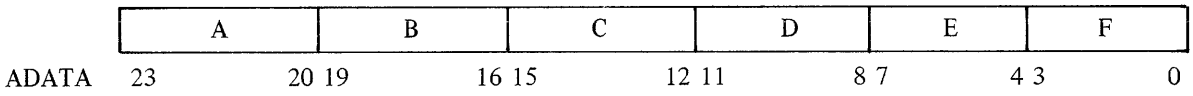


Fig. II-58 "A" DATA

As can be seen by referring to Figure II-58 and Figure II-57, Address 2 addresses bits 8 through 11, Address 1 addresses bits 4 through 7 and Address 0 addresses bits 0 through 3 as the source data. The multiplexors on Card B address the remaining portions of the A Data in a similar manner. The four bit data is placed on the Main Exchange after it has been sent through the 4 Bit Function Box and six copies are placed on the Main Exchange if the destination is a 4 Bit Register or only one copy if the destination is a twenty-four bit register. (Upper 20 bits would be filled with zeroes).

MASK GENERATOR

The Mask Generator which is located on Processor Cards A and B is also discussed for its function in generating a mask for the S-Memory Processor Rotator Logic. In the rotation logic, the Mask Generator produces the length of the mask which is to be sent to the Rotator and set into MIR. The multiplexor elements on Cards A and B receive an address of six which is connected to a true voltage and the Mask Generator enables "X" number of multiplexors to produce a mask onto the Main Exchange. Because the logic for the Mask Generator is the same the Mask Generator itself will not be discussed in detail. For further information refer to Mask Generator Rotation Logic. It should be noted that the length of the mask which is generated disregarding the Shift/Rotate functions is either under control of CPL or a Lift Mask term is true to allow a full mask to be generated. If, for example, the X, Y, T, L. FA, FB, Scratchpad or A Stack were selected as a source then the Lift Mask term would cause a mask of twenty-four bits to be generated as the registers mentioned are all twenty-four bit register. On the other hand, if certain result registers such as SUM, DIFF, MSKX, MSKY, XORY, XEOY, XANY, CMPX or CMPY are selected then the length of the mask is solely dependent upon the value in CPL. The actual selection logic which selects CPL as the value which determines the mask is on Card C. The logic in Figure II-59 illustrates the logic for the generation of the mask or Bits 00 thru 11.

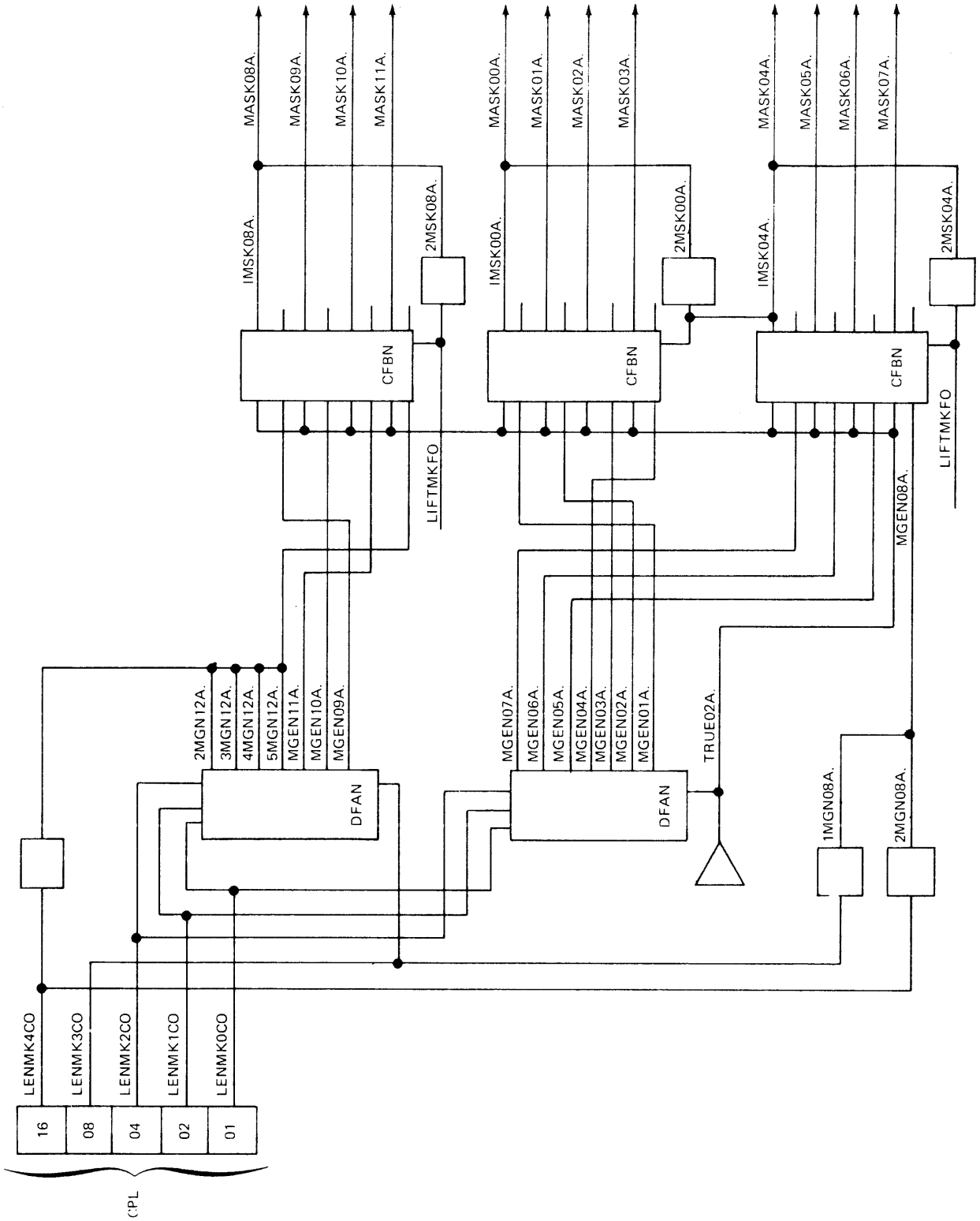


Fig. II-59 MASK GENERATION (BITS 00-11)

OUTPUT BUFFER CONTROL

The output of the various multiplexors are not sent directly to the Main Exchange but instead are sent to a series of 24 buffer elements which must be enabled. Like the multiplexors, the buffers are also divided into two groups with the upper twenty bits in one group and the lower four bits in the other. In most cases all 24 buffers are enabled or all 24 are disabled. The one case where this does not hold true is if a four bit register is designated as a source and a 24 bit register as the sink. In this example, only the least significant four buffers are enabled to gate the data to the Main Exchange. The top twenty buffers are disabled and therefore zeros are placed on the upper twenty bits of the Main Exchange to allow zeros to be placed in the most significant twenty bits of the sink register.

Shown in Figure II-60 is the enable logic for the 24 buffers. The basic enable terms are MCONENDO and MEXCENDO which are produced if any of the corresponding multiplexors are addressed (See Figure II-55) and if the operation is not for the downcounting of the FL Register. If the operation is an FL down (FLDOWNDO) and MCAR15B. is true indicating that a subtraction will result in FL going below zero then the output of the buffers are inhibited which results in FL being forced to zero at sink time of the downcount FL operation.

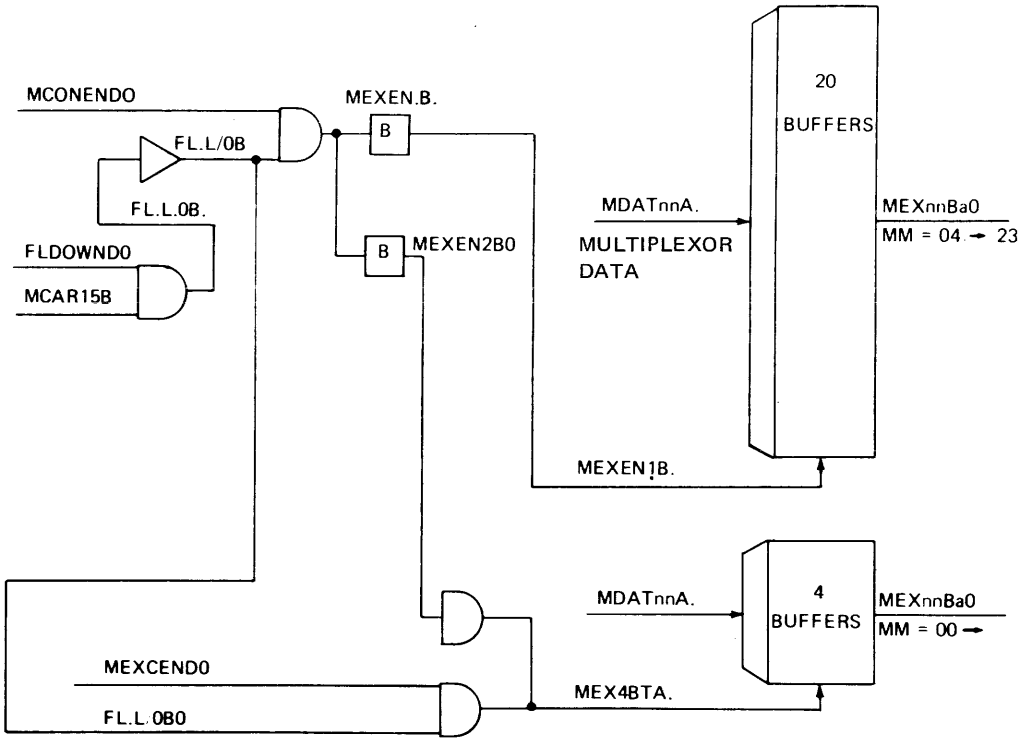


Fig. II-60 24 BIT FUNCTION TO MEX ENABLE

GENERAL OPERATION BINARY SUM

The 24 Bit Function Box has been provided the logic to generate a binary sum of the "A" and "B" data. The various inputs to the "A" and "B" data have been previously discussed therefore this discussion only concerns itself with generating a binary sum of those inputs. The sum operation is directly under control of the M Register contents and/or the CP Register. For this discussion assume and the micro in the MRegister is one that requires a SUM operation that is designated for by a register move type micro with SUM as source. In reviewing the effect of CP, CPL controls the length from 1 to 24, CPU controls the mode either binary or BCD and CYF is the carry into the adder provided it is set (TRUE).

The Binary Sum described for an example will therefore add the contents of X+Y+CYF and place the result at the input of the 24 output multiplexor elements. (Refer to Figure II-54 for inputs to the multiplexor).

ADDER (Detailed Description)

The adder as can be seen in Figure II-61 is a 24 bit adder which consists of six modulo 16 adders along with the associated carry logic. The adder elements are the Dual Full Adder/Subtracter elements referred to as AFANS and the carry elements are the High Speed Carry element CFBN. Figure II-62 shows a detailed diagram of one modulo sixteen adder with binary weights assigned to the various inputs and outputs. The following formulas can be applied to each individual stage for the development of the sum output represented by Si, the generate output represented by Gi and the propagate output represented by Pi. Note that the propagate and generate formulas given at this time are for an add operation only where the Si formula applies to both a sum and difference operation.

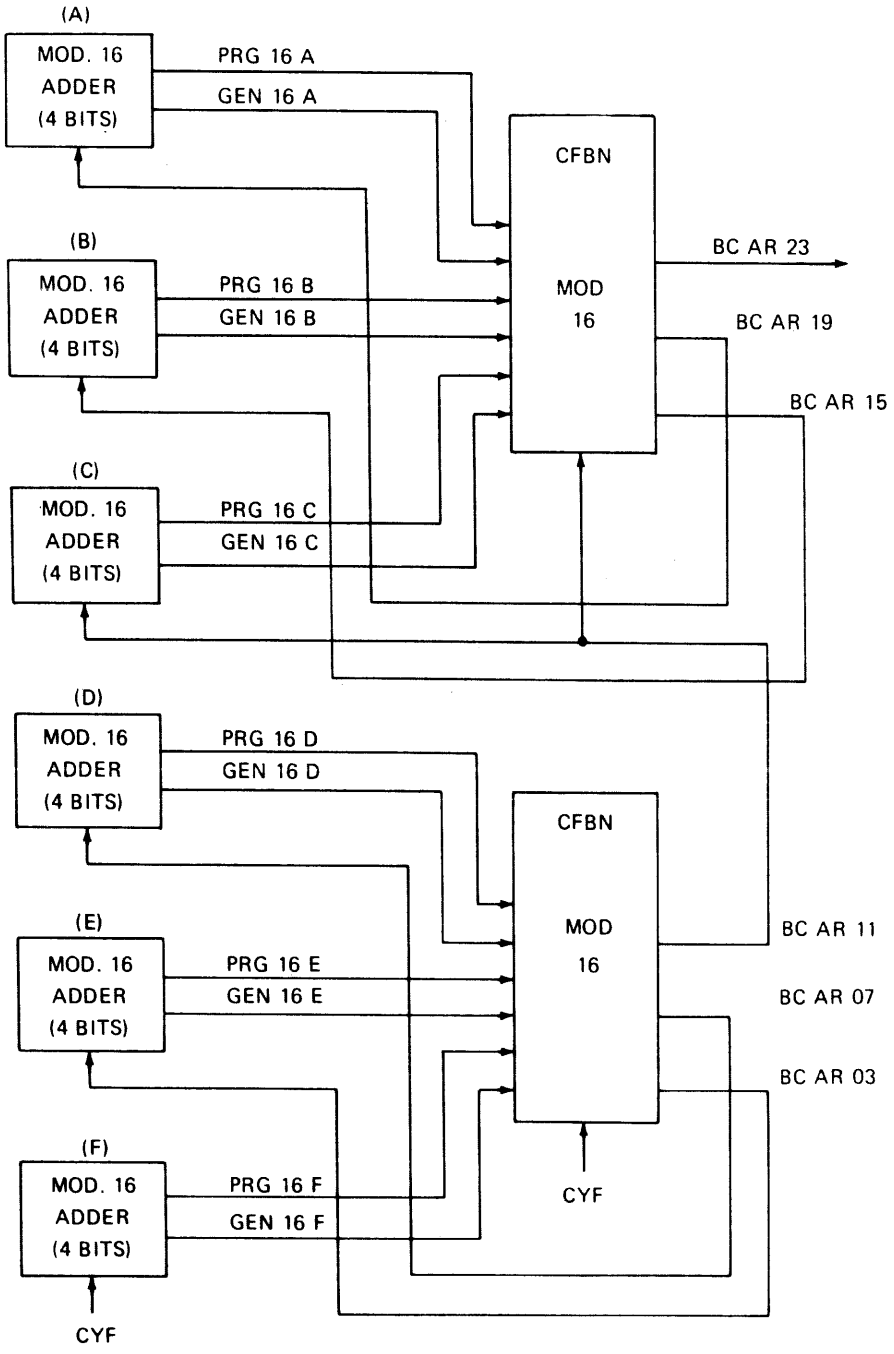


Fig. II-61 24 BIT BINARY ADDER

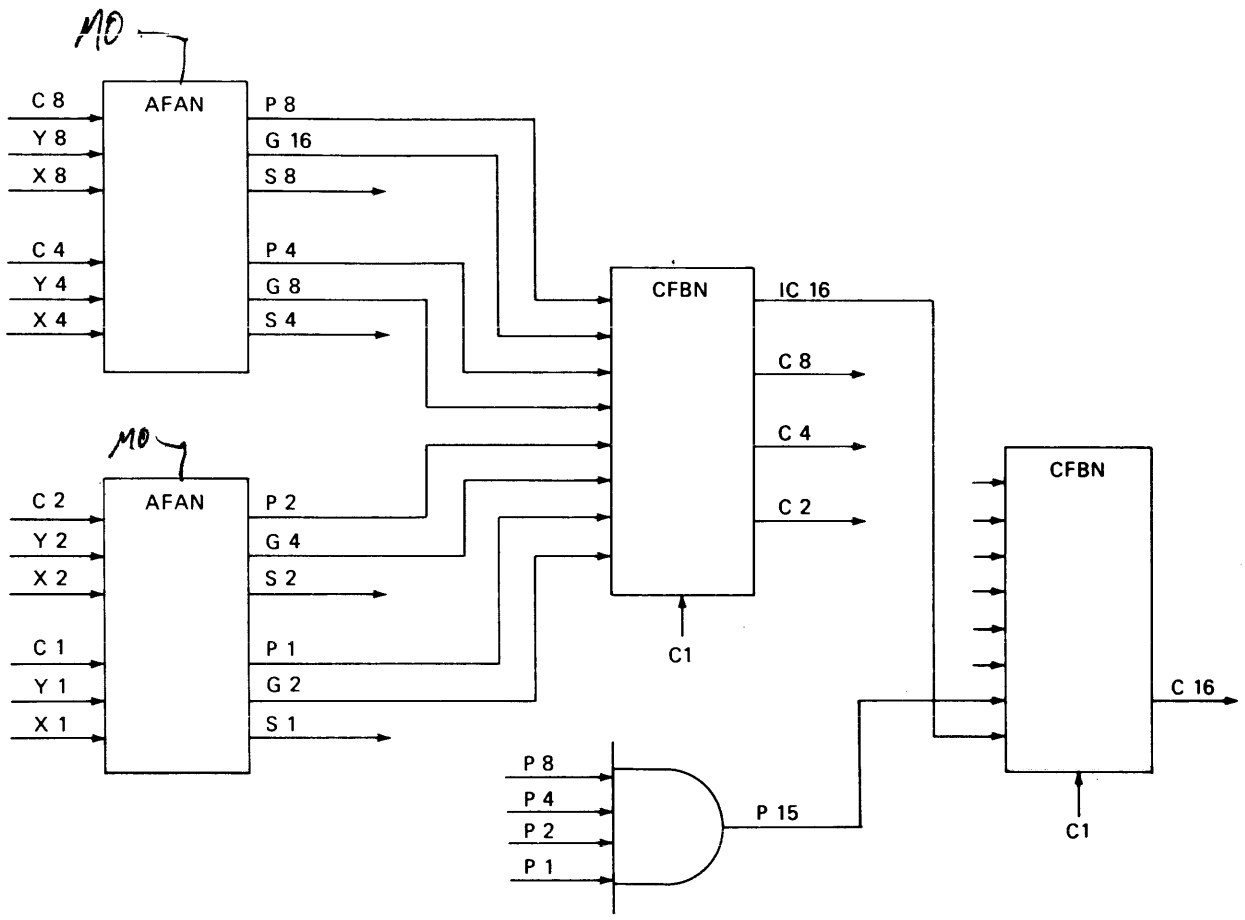


Fig. II-62 MOD. 16 ADDER SHOWING WEIGHTED FACTORS

Si = $CI*(\overline{ADATA}*\overline{BDATA}+ADATA*BDATA)+\overline{CI}*(\overline{ADATA}*BDATA+ADATA*\overline{BDATA})$

ADATA = X Register, FA Register, FL Register
BDATA = Y Register, Literal of Micro or CPL, left scratchpad (8D Micro) Refer to Figure II-53

Gi = ADATA*BDATA

Pi = $(\overline{ADATA}*BDATA)+(ADATA*\overline{BDATA})$

GENERATE AND PROPAGATE TERMS

The generate and propagate terms are sent to a carry element (CFBN) which will examine the Propagate and Generate terms in parallel. By examining the propagate and generate terms in parallel the appropriate carry terms can be produced almost "instantaneously". Before continuing the discussion it is probably in order to define the propagate and generate terminology.

Propagate — Propagate is produced if an individual section of the adder to the next stage of the adder. The propagate is produced regardless of that carry input from the previous stage therefore it may be stated that the propagate "anticipates" that carry occurring. As can be seen from the Pi formula that propagate is true if one or the other of the two inputs to a stage is true. If this condition exists and a carry into that stage is true than that stage will simple "pass" that carry onto the next stage or in our terminology, propagate the carry.

Generate — Generate is produced if an individual stage or section of the adder will produce a carry. A carry is produced by that stage only if the inputs are a "1" and a "1" as shown in the Gi formula.

The production of these levels as previously mentioned allow the carry elements to produce the appropriate carriers in order to facilitate the speed of the add operation.

ADD EXAMPLE

In order to describe the logic, take into consideration one modulo sixteen stage and assume the ADATA input (X Register) is 1000 and the BDATA input (Y Register) is 1001. The desired result will be in binary 10001 or seventeen. The logic in actuality will produce 0001 from the stage being discussed with a carry out of that stage to the next modulo sixteen stage. If CPL has designated a length of four then the carry would not be sent to the next stage but instead be sent out of the Function Box as CYL. It would be a software function to detect the carry out or overflow and act accordingly realizing the result is not 0001 but instead 10001. Note that the carry is not automatically stored but must be detected and stored by setting CYF if desired. Figure II-63 shows the add of the 1000 and 1001 with the sum, generate and propagate levels which are produced.

16	8	4	2	1
	1	0	0	1
	1	0	0	0
1	0	0	0	1
	Si = 0	Si = 0	Si = 0	Si = 1
	Pi = 0	Pi = 0	Pi = 0	Pi = 1
	Gi = 1	Gi = 0	Gi = 0	Gi = 0

Fig. II-63 ADDER EXAMPLE

Figure II-63 in addition to showing the binary weighted inputs to the actual adder elements also shows the binary values of the carry levels which are generated.

Carry Term Definition

The following equations and descriptions of equations are intended to explain the production of the carry terms and the significance of the propagate, generate and carry terms in the equation. All terms are referenced to the binary weight as shown in Figure II-63.

C2=(G2)+(P1*C1)

Carry Out of the first stage will result from the X and Y inputs being both equal to one (1+1=0 with a carry out) or with either X or Y equal to one (1+0 or 0+1) and a carry in to that stage (1+0+C1=0 and carry out.

C4=(G4)+(P2*G2)+(P1*P2*C1)

G4 indicates a carry which was generated by the inputs to this stage of the AFAN (1+1=0 with a carry out). P2*G2 indicate a generation of a carry in the previous stage and one of the inputs to this stage is true (either X or Y). P1*P2*C1 indicate a carry from the previous stage (P1*C1) along with one input to this stage.

C8=(G8)+(P4*G4)+(P4*P2*G2)+(P4*P2*P1*CI)

In a similar manner, C8 recognizes a generation of a carry in this stage (G8) or propagates and generates developed in previous stages which will cause a carry out of this stage.

C16=(IC16)+P8*P4*P2*P1*CI)

C16 is produced as a result of an internal carry 16 which actually is a result of G16 or combinations of the propagate and generate terms from the previous stages. The following is the formula for the IC16: (G16)+(P8*G8)+ P8*P4*G4)+(P8*P4*G8*G2). The second term in the C16 equation is underlined because it is not internal to the CFBN elements but must instead be built with an external gate.

EXAMPLES FOR C16

C16=(G16+P8G8+P8P4G4+P8P4P2G2) + P8P4P2P1C1

1. G16

```
    8421
X   1000
Y   1000
   10000
```

2. P8G8

```
    8421
X   1100
Y   0100
   10000
```

3. P8P4G4

```
    8421
X   0110
Y   1010
   10000
```

4. P8P4P2G2

```
    8421
C1     0
X   0101
Y   1011
   10000
```

5. P8P4P2P1C1

```
    8421
C1     1
XX  1010
Y   C101
   10000
```

Four Bit BCD (Binary Coded Decimal) Sum

In order for the Arithmetic Unit to perform a four Bit BCD sum, the value 01 must be placed in CPU and the value in CPL must be an even multiple of four; 4, 8, 12, 16, 20, or 24.

Four Bit BCD Sum Example E

In order to illustrate a four Bit BCD Sum, consider several examples:

```
EXAMPLE 1          EXAMPLE 2          CORRECTION
  0111 = 7           0111 =  7                    1111 = 15  (Binary Result)
  0001 = 1           1000 =  8            1       0110 =  6
  1000 = 8           1111 = 15            ↓       0101 =  5
                                       CARRY
                                       OUT
```

In example one, the BCD value of 7 is added to 1 with the result being 8. Because the sum is less than 10, no correction is necessary. The second example adds seven plus eight to obtain a value of 15. The value 15 as shown initially in Example 2 is not BCD but instead a binary 15. Therefore, it must be corrected by adding a value of six to the initial binary sum.

BCD SUM CORRECTION

In any add operation if the sum is greater than nine then it must be decimally corrected by adding a value of six to the sum with the carry being sent to the next stage. Figure II-64 illustrates the logic and add/subtract six for BCD. Notice upon correction, the BCD value is now five with a carry to the next stage.

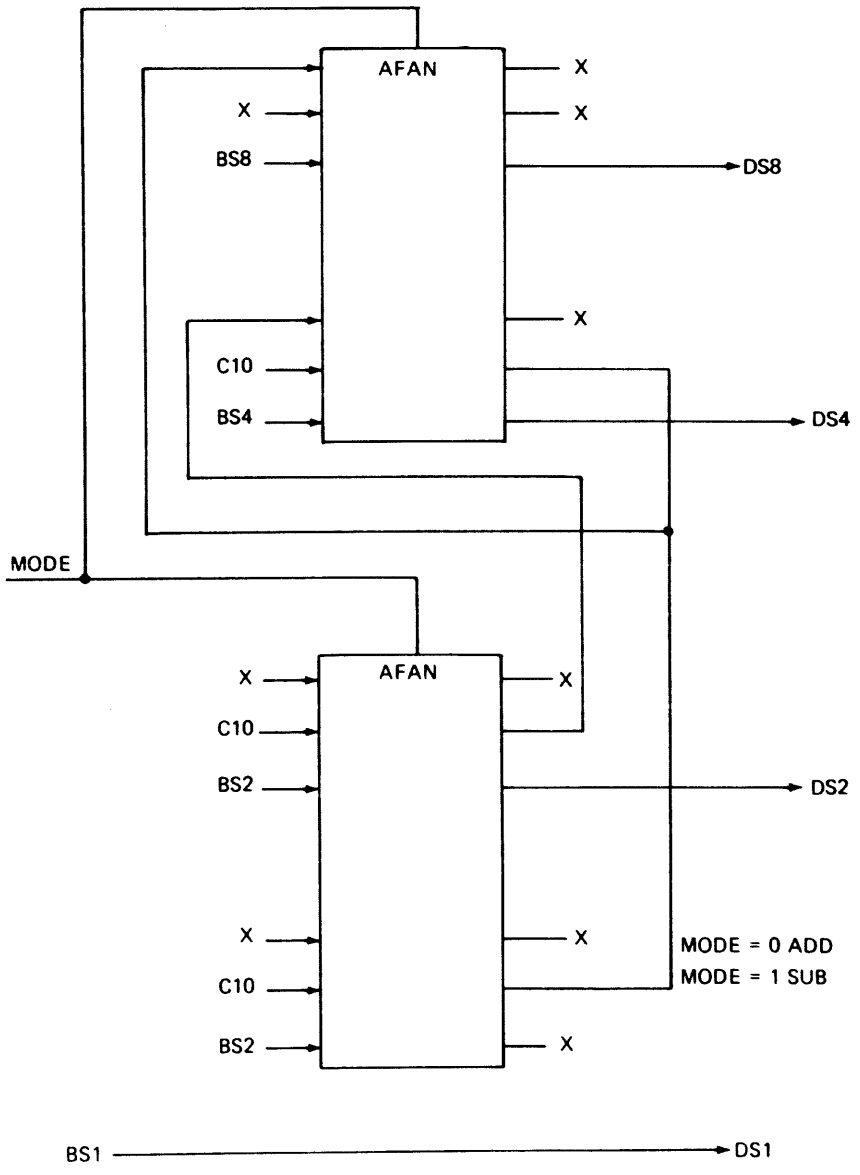


Fig. II-64 LOGIC FOR ADD/SUB 6 FOR BCD

The carry would enter the next stage and be added to the two 4 Bit BCD operands of that stage or if CPL=4 then the carry would be output to CYL and would have to be recognized by software in the same manner as discussed in the Binary Sum section. It is significant at this time to note that the Carry Out is not actually obtained from the BCD Correction Logic but must be generated from the actual binary adder. From the example of 8+7, it can be seen that the binary adder will not produce a carry to the next stage. Logic has therefore, been specifically implemented for the BCD add in order to generate or force a carry to the next stage if the result of the add is equal to or greater then ten. Figure II-65 shows the generation of C16 for the BCD ADD.

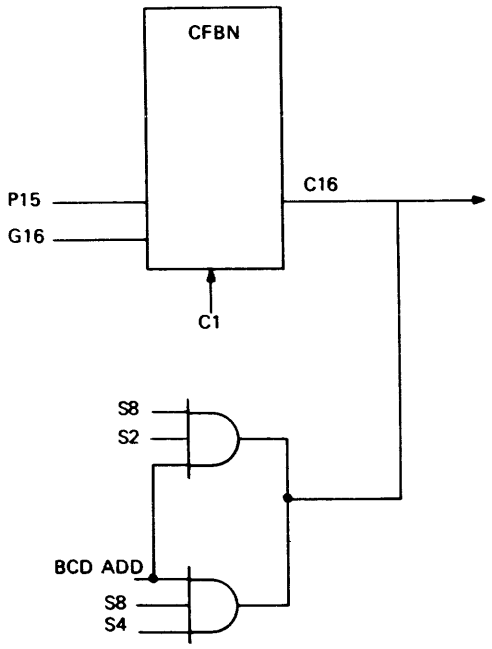


Fig. II-65 BCD CARRY CORRECTION

BINARY AND BCD DIFFERENCE

The difference operations like the Sum operations are under control of the CP Register. In other words, CPL controls the length and CPU the mode where CPU=00 for binary and CPU-01 for BCD. The same arithmetic unit which was used to perform the SUM will be used to obtain the difference of X-Y-CYF. The Arithmetic Unit is placed in the subtract mode by the term SUB. . .DO which is generated on Card D as shown in Figure II-51 (24 Bit Function Box Control).

BCD ADDER

The conversion form Binary to BCD is handled in two steps.

1) Carry correction
2) Binary sum correction

1. CARRY CORRECTION

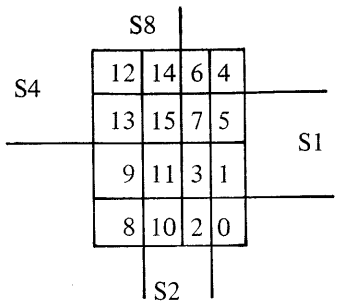
The carry for MOD 16 was:

C16 = G16 + P15C1

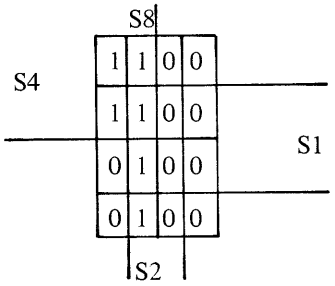
For BCD we want

C10 = C16 + Sum (10 + More)

C10 = G16 + P15C1 + S8S2 + S8S4



S10 MAP



S10 = S8S2 + S8S4

Fig. II-66 S10 MAP

BCD DIFFERENCE CORRECTION

Unlike the SUM operation there is no correction of the carry/borrow for the BCD DIFFERENCE. Like the SUM operation however if a borrow is present from one of the modulo sixteen stages then the DIFFERENCE result must be corrected. Figure II-64 illustrates the logic for add/subtract 6 for BDC. The BCD correction for the DIFFERENCE is accomplished by subtracting six from the result of the binary subtraction.

4BIT BCD DIFFERENCE EXAMPLE

Consider the two examples; in the first example no correction is required and in the second example a correction is required.

EXAMPLE 1	EXAMPLE 2	CORRECTION
1001 = 9	0001 0111 = 23 (BINARY)	1110 = 14
0111 = 7	0000 1001 9	0110 = 6
0010 = 2	1110 14	1000 = 8

In Example 1 a borrow from the first stage did not exist therefore a BCD correction was not requred. In the second example the Binary Adder assumed the subtraction was 23-9 to give a result of 14, but in actuality the number into the adder in BCD is 17-9 to give a result of 8. Because the mode is BCD and a borrow is present from the first stage to the second, a subtraction of six is performed to five the desired BCD output which is eight. Propagates are performed if the bits into a stage are equal (X=1 and Y=1 or X=0 and Y=1) for that stage. If the value of the entire binary or BCD number in the X Register is less than the value in the Y Register then a borrow out will exist which is referred to as CYD. Like the ADd operation, it is the function of the software to check for this level from the Arithmetic Unit.

CYF FLIP-FLOP (SUBTRACT)

The last item which must be discussed for the subtract is the CYF flip-flop. In the case of the subtract, CYF is a borrow from the Arithmetic Unit. It was previously mentioned that is CYD were true that the software must recognize it and it may be the function of the software to set CYF upon detection of the borrow. Two more operands may then be placed in X and Y with CYF acting as a borrow from the two previous operands.

COMPLEMENT X (CMPX)

The Complement of X is the one's complement of the X Register. The length of X is designated by CPL with the complement of the bits of the X Register gated to the Main Exchange and the most significant bits will be leading zeros provided the value of CPL is less than 24. The complement of X is obtained by placing thecontents of X through an inverter to the multiplexed output of the 24 Bit Function Box. Refer to Figure II-54.

COMPLEMENT Y (CMPY)

The Complement of Y is the one's complement of the Y Register. The length of Y is determined by CPL, with the complement of the least significant bits of the Y Register gated to the Main Exchange and the most significant bits will be leading zeros. The complement of Y is obtained by placing the contents of Y through an inverter to the multiplexed output of the 24 Bit Function Box. Refer to Figure II-54.

X AND Y

X and Y is the logical AND of the X and Y Registers with the length of the "And" being determined by CPL. Leading zeros are gated to the left of the significant data. The "And" function is obtained by placing the X and Y Registers into the Adder and then by using the Generate term out of each stage or each bit position of the adder, and the logical "And" is obtained. In reviewing the adder the formula for the generate term was; $Gi=A*B*\overline{MO}$. The significance of the mode line being false is that the arithmetic unit must be in the Add mode which will be true if the operation is X and Y as bit eleven of the M Register will be off. From Figure II-54 it can be seen the Generate term is the input to the multiplexor for the "And" function.

EXCLUSIVE OR, X AND Y

The Exclusive Or of X and Y is the logical function "exclusive or". The function can be defined by the following equations:

$\overline{X}+\overline{Y}=0$
$X+\overline{Y}=1$
$\overline{X}+Y=1$
$X+Y=0$

The length of the exclusive or is defined as in previous operations by CPL; left zeros are placed on the Main Exchange if the length is less than twenty four. The Exclusive Or is obtained by placing the Arithmetic Section in the Add Mode and then gating the inputs of X and Y to the Arithmetic Unit. The Exclusive Or is obtained from the Arithmetic Section by using the Propagate and sending it through the multiplexed output to the Main Exchange. The formula for the Propagate is as follows: $Pi=\overline{MO}*(\overline{X}*Y+X*\overline{Y})$. (See Figure II-54).

X OR Y (XORY)

X or Y is the logical function of an "OR" of either the X or Y Register to the Main Exchange. As in previous operatons the length of X or Y is defined by CPL and if CPL is less than twenty four the data is right justified on the exchange with left leading zeroes. The "OR" is obtained at the input to the multiplexor by enabling both X and Y onto the same input leg and then selecting that input to the Main Exchange. (See Figure II-54).

MASK OF X (MSKX)

The Mask of the X Register provides for the gating of a portion of the X Register to the Main Exchange and subsequently a sink register. The length of the Mask is controlled by CPL. For Example; assume CPL=8. With a length of bits designated and the Mask of X requested, the least significant 8 bits of X will be gated to the Main Exchange with the most sifnificant bits on the Main Exchange filled with zeros.

The generation of the bits for the mask to allow only a portion of the data onto the Main Exchange is shown on figure II-59, and is the same for all other operatons where the length is less than twenty four.

MASK OF Y (MSKY)

The Mask of the Y Register is identical to the Mask of X with the exception the Y Register bits are gated to the Main Exchange. Again the length of the mask is controlled by CPL.

24 BIT FUNCTION BOX 4 BIT RESULTS

As stated earlier, three pseudo registers contain various 4 bit results produced by the 24 Bit Function Box. A detailed explanation follows.

BINARY CONDITIONS (BICN)

The Binary Conditions of the 24 Bit Function Box are considered as a source register only. The four conditions to be discussed are:

LSUY	Least Significant Unit of the Y Register
CYF	Carry Flip/Flop which is a part of the CP Register
CYD	Borrow Out Level as a result of the Y Register greater than the X Register on a DIFFERENCE operation.
CYL	Carry Out Level as a result of an X register plus Y Register SUM operation where CYL out of the most sifnificant bit is controlled by CPL.

LSUY is true if the least significant unit of the Y Register is equal to "1" and CPU=00 which is designating the binary mode. LSUY in this case is defined as the least significant "bit" of the Y Register. If CPU≠00 meaning that the mode is not binary but BCD then LSUY is true if the least significant unit (least significant four bits) of the Y Register is equal to 1 0 0 1 or decimally speaking 9. Figure II-67 is of the logic on Card A which produces LSUY.

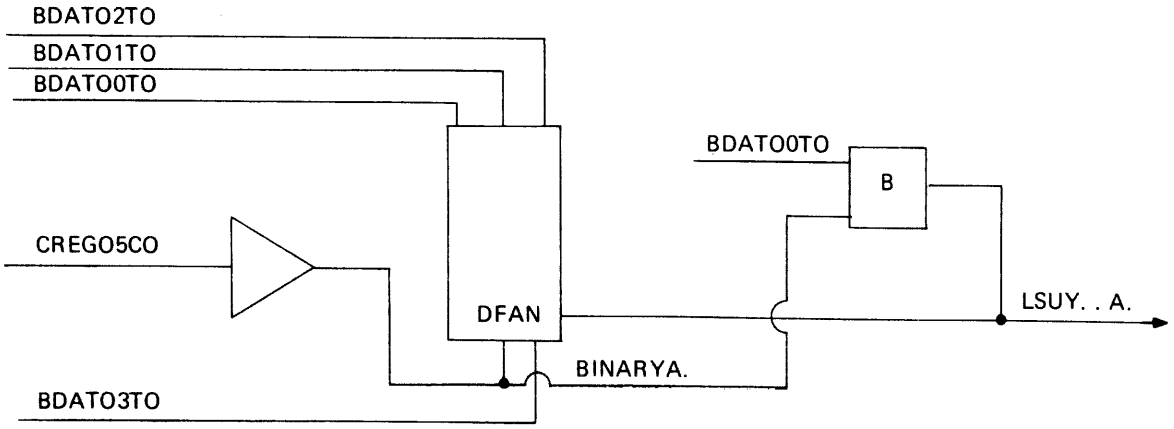


Fig. II-67 LSUY A LOGIC

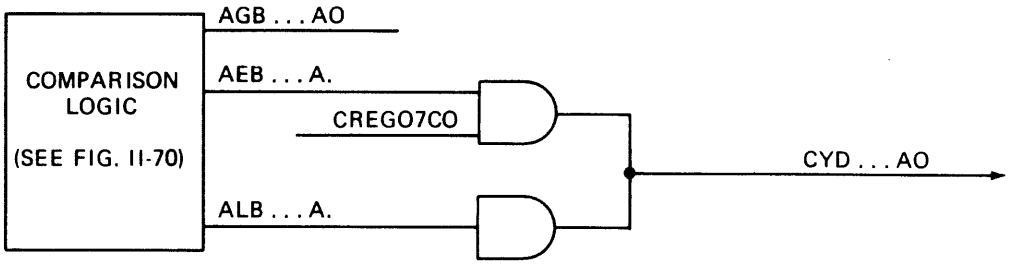


Fig. II-68 Y>X CARRY OUT LOGIC

[redacted] of the Binary Conditions is the most sifnificant bit of the CP Register. When the Binary Conditions are selected by a micro instruction the Carry Flip-Flop is gated to the multiplexor element which in turn gates CYF onto the 4 Bit Auxilliary Bus. CYF is manipulated by a 6E micro, Carry Flip-Flop Manipulate, and would be used to store a carry or borrow as a result of an add or subtract operation.

[redacted] is produced thru gating on Card A and is produced if X is greater than Y or if X equals Y and CYF is set which indicates a borrow exists immediately. CYD is independent of CPL. Figure II-68 shows the generation of CYD.

[redacted] is produced as a result of a carry from the most significant stage of the adder as designated by CPL. If CPL is equal to zero then CYL will reflect the state of CYF. The mnemonic for CYL is CYL. . .TO which is produced by the logic illustrated in Figure II-69.

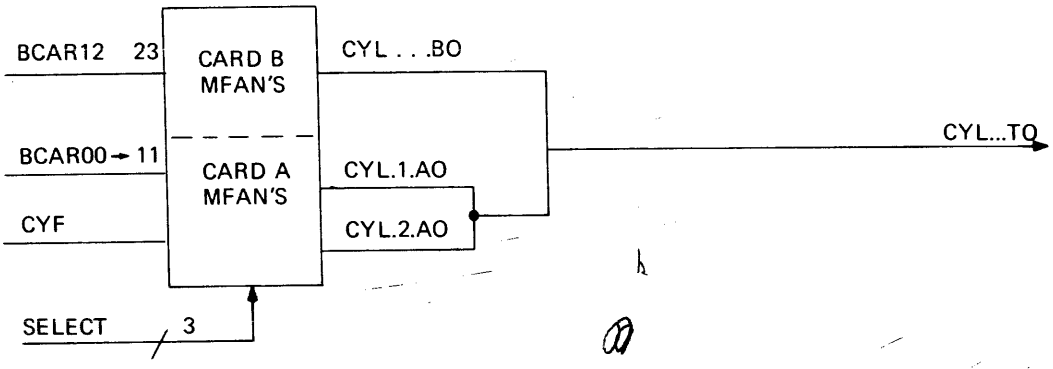


Fig. II-69 SUM CARRY OUT LOGIC

X-Y Conditions are a comparison between the X and Y Register data. This comparison occurs on both Cards A and B as shown in Figure II-70. Card B tests the upper twelve bits and sends the result of that comparison to Card A which uses those inputs plus the lower twelve bits in order to determine if a comparison exists or the relationship of X and Y. In the figure it can be seen that the input to the logic is A Data and B Data, A Data being the X Register and B Data the Y Register. The three resultant terms AEB. . .A. (A EQUAL B), AGB. . .AO (A GREATER THAN B) and ALB. . .AO (A LESS THAN B) are sent to the 4 Bit Output Section of the 24 Bit Function Box which is shown in Figure II-71. The other bit of the XYCN is not a comparison between the X and Y Register but instead is a test of the most significant bit (MSBX) of the X Register as indicated by the value in CPL. If the bit designated is true then the term MSBX. .TO will be true. The MSBX. .TO term is made up of either MSBX. .BO, MSBX.1AO or MSBX.2AO which are produced in a similar manner as CYL. .TO as shown in Figure II-69.

X-Y STATES (XYST)

The X-Y States are relational conditions which are considered as a 4 bit group and are addressable as a source only. The four conditions produced by the logic are: Least Significant Unit of X (LSUX), Interrupt (INT), Y is unequal to zero (Y≠0) and X is unequal to zero (X≠0).

Both the X≠0 and Y≠0 functions are produced in similar fashions and are both based on the binary value of 24 bits of X or Y. Each of the 2 cards (A and B) have the logic for comparison of 12 bits and if any bit is on then the appropriate level (X≠0 or Y≠0) is produced and a backplane "or" (〈come〉) exists to combine the appropriate term into the mutiplexor element which preceeds gating onto the Auxilliary Bus.

The Least Significant Unit of X is similar to the Least Significant Unit of Y which has been discussed in the Binary Conditions. If CPU of the CP Register is equal to zero and the least significant bit in the X Register is on then LSUX will be true. If CPU of the CP Register is unequal to zero indicating a BCD mode then the least significant four bits of the X Register are examined and if equal to nine (1001) then LSUX is true.

The last conditions of the X-Y States is the Interrupt "or" which is not relevant to any X/Y state or condition. The Interrupt will be true if any of the following conditions as reflected in CC or CD are true:

1. Console Soft Halt Interrupt (CC0)
2. I/O Bus Service Request Interrupt (CC1)
3. Real Time Clock Interrupt (CC2)
4. Memory Read Data Parity Error Interrupt (CD3)

The development of the Interrupt "Or" bit for the XYST is shown in Figure II-71.

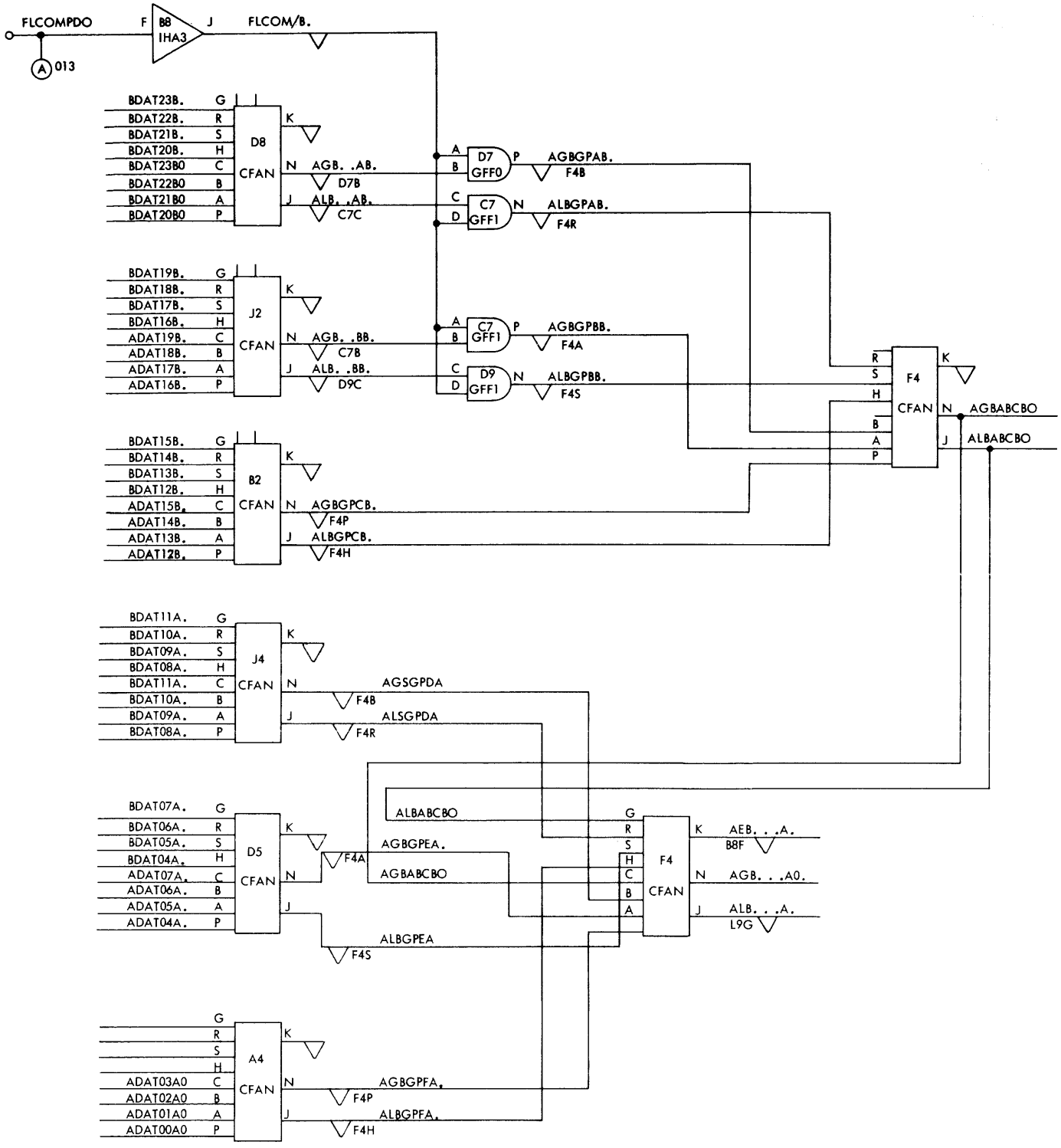


Fig. II-70 X–Y CONDITIONS LOGIC

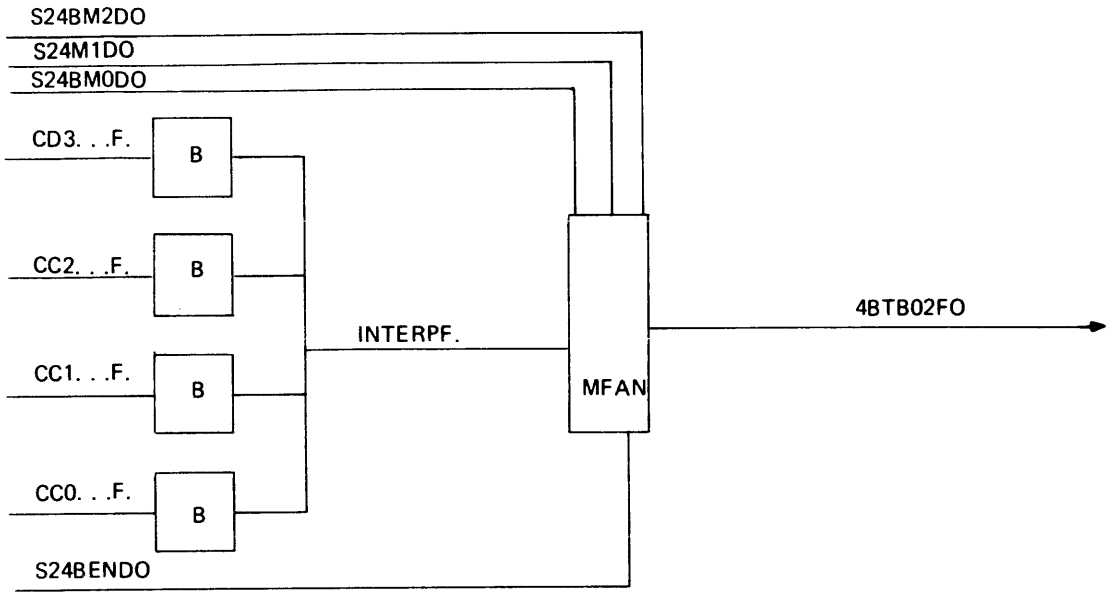


Fig. II-71 INTERRUPT "OR" BIT

It should be noted that while bits 0, 1 and 3 are gated to the 4 Bit Auxilliary Bus on Card A that the INT OR is produced and gated to the Bus on Card F.

FOUR BIT ARITHMETIC AND COMBINATORIAL SECTION

The Four Bit Arithmetic and Combinatorial Section, otherwise referred to as the Four Bit Function Box, contains the logic to produce the output results most commonly used between two operands. A simplified block diagram of the 4 Bit Function Box is illustrated in Fig. II-72. Figure II-73 is a more detailed version.

INPUTS

Input to the Function Box is any of the four bit registers and pseudo registers listed in Table II-II. A second input is obtained from the M-Instruction itself. The actual inputs to the multiplexor chips are shown in Figure II-73.

INPUTS

TA	TB	TC	TD	TE	TF
LA	LB	LC	LD	LE	LF
FU	FT	FLC	FLD	FLE	FLF
CA	CB	CC	CD		
BICN	XYCN	XYST	FLCN		

TABLE II–II

OUTPUTS

Outputs of the Function Box include generation of set, and, or, exclusive, or binary modulo sixteen SUM, and binary modulo sixteen DIFFERENCE. The actual output logic is illustrated in Figure II-73. The output which is obtained is sinked to the same register which acted as the source. The exceptions to this are the pseudo registers which are listed on the last line of the Chart II-11 and these cannot act as a destination. The logical and binary results which are obtained are done so by using the source register as one of the operands and the least significant four bits of the micro (four bit

manipulate literal) as the other. Other functions which are performed in addition to setting the register with the logical function are to test various bits of a register and depending upon the result and instruction branch or skip to a new instruction. The four bit function box will be described in the following sections according to micro operator.

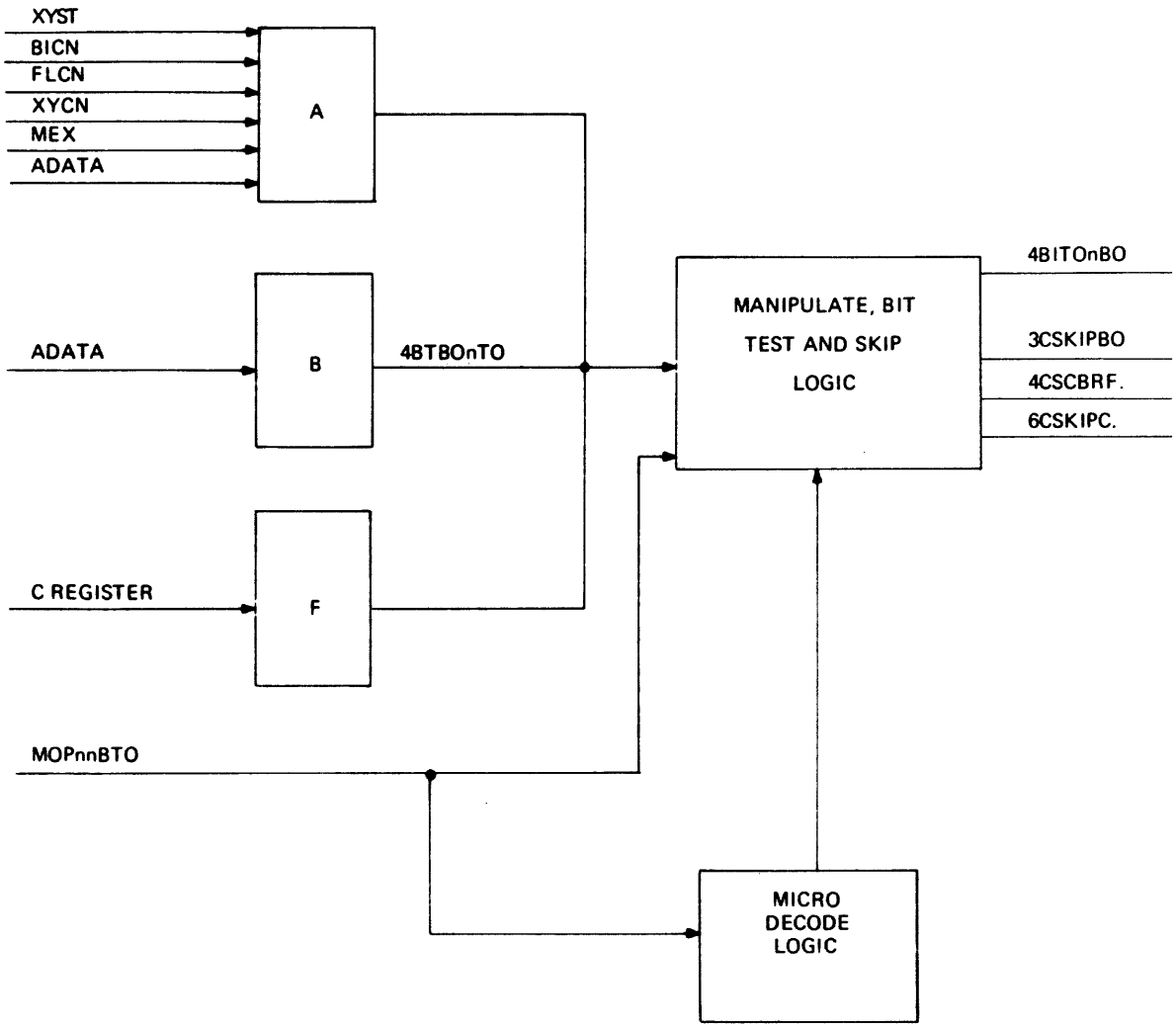


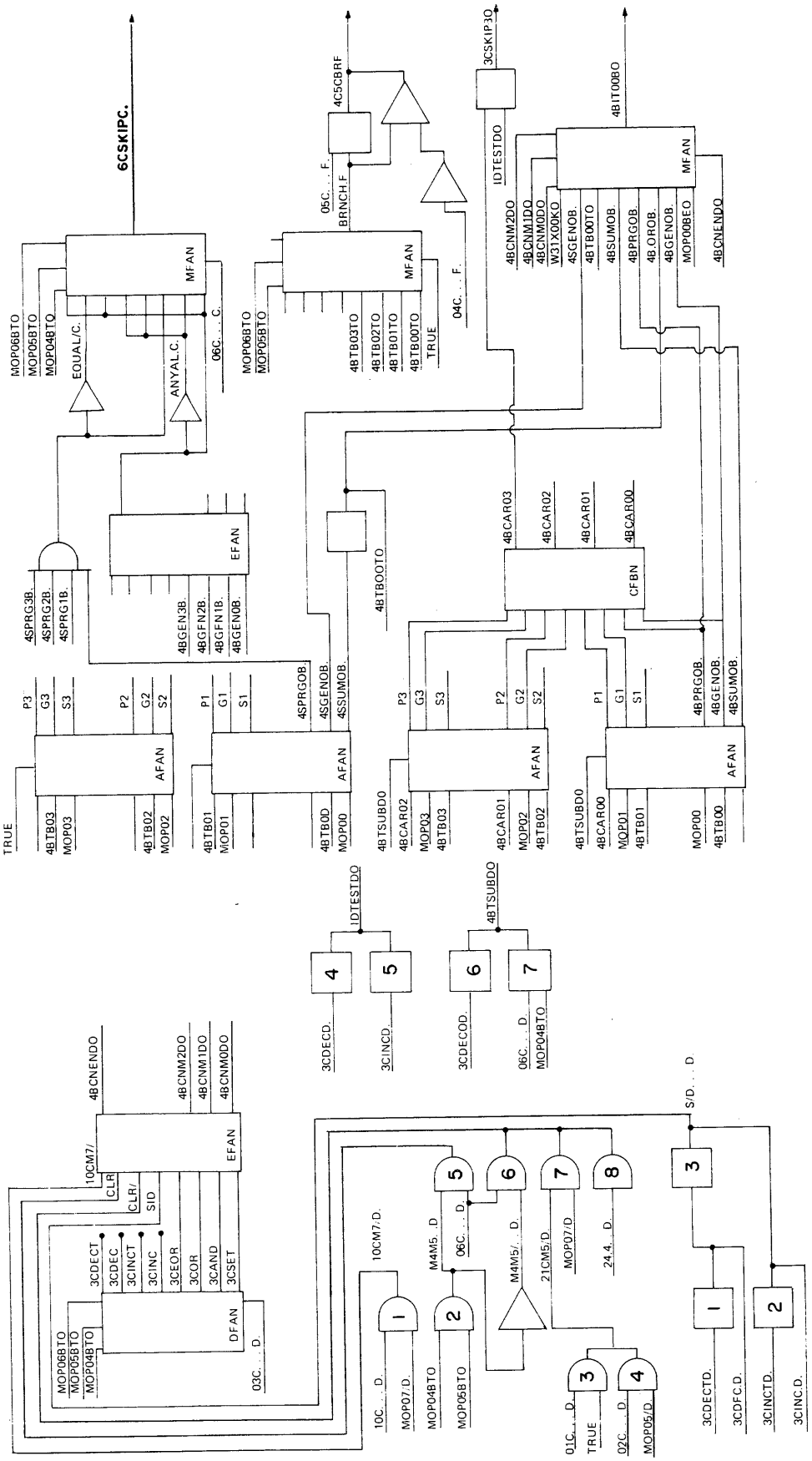
Fig. II-72 4 BIT FUNCTION BOX BLOCK DIAGRAM

MICROS

Those micros which affect the function box are: 1C Register move, 2C Scratchpad move, 3C 4 bit manipulate, 4C Bit test relative branch false, 5C bit test relative branch true and 6C Skip when 10C shift/rotate T.

1C REGISTER MOVE

The 4 Bit Function Box becomes a part of the 1C Register Move micro when a 4 bit register is designated as either a source or sink. When the register sourced is a 4 bit register, the micro decoding will allow the source data to be gated through the 4 Bit Function Box and to the 24 bit Main Exchange. If the 4 bit register which has been sourced is to be sent to another 4 bit register then six copies of the source information will be placed on the Main Exchange and if the destination register is a 24 bit register then only the least significant 4 bits of the Main Exchange will contain data and the most significant 20 bits will contain zeros. If a 24 bits register has been designated as the source with a four bit register as destination then the 4 least significant bits of the source register will be enabled through the 4 Bit Function Box and six copies of the data will be gated to the Main Exchange.



√ Fig. II-73 4 BIT FUNCTION BOX

2C SCRATCHPAD MOVE

The 4 Bit Function Box becomes a part of the 2C Scratchpad Move when a move from a 4 bit register to scratchpad is selected or if the contents of scratchpad is to be sent to a four bit register. The data flow for the 2C Scratchpad Move is identical as the data flow for the 1C Register Move.

10C SHIFT/ROTATE T

The 4 Bit Function Box becomes a part of the 10C Shift/Rotate T micro when a 4 bit register is designated as sink. The data is read from the T Register and the Shift/Rotate result is obtained in the Memory Information Register (MIR). With the sink register being a four bit register, the 4 LSB of MIR are gated thru the 4 Bit Function Box to the Main Exchange in 6 copies (A, B, C, D, E, F). The requirement, in addition to a decode of the 10C micro is that the micro operator bit seven (M0P07) is false which indicates either register select zero or one is true to select a 4 bit register.

3C 4 BIT MANIPULATE

The logic within the 4 Bit Function Box provides the generation of the logical and arithmetic functions of the 3C 4 Bit Manipulate Micro Instruction. These logical and arithmetic functions are generated as a result of the manipulate variants within the micro which provide for: 1 set function, 3 logical functions and two arithmetic functions with a test capability for overflow on the sum and underflow on the difference. The Functions which are produced are: Set, And, Or, Exclusive Or, Increment, Decrement, Increment and Test and Decrement and Test. The manipulate variants are bits four, five and six (M0P04, M0P05 and M0P06) of the 3C micro. Figure II-73 illustrates the decoding of the 3C micro according to the function. The terms from the decoding elements will select the appropriate outputs from the Four Bit Function Box. In addition to the data out, if a test is indicated and the test condition is met, then the term 3CSKIPBO is sent to the Control Logic to allow the next micro to be skipped. Each of the functions will be discussed in the following description of the eight variants.

SET: The Set function of the 3C micro instruction is not a logically produced function. The Set function allows the literal contained in the micro to be sent to the destination register by gating the literal from the Micro Operator Bus through the 4 bit Function Box and to the destination. In this operation the term 4BCNENDO will be true (4 Bit Control Enable) and allow the output section multiplexors to gate the literal to the 4 Bit Bus ($BITOnBO) and subsequently to the Main Exchange where it will be sent to the destination. Figure II-74 indicates the 4 Bit Mode Control lines which are enabled for each of the eight functions of the 3C micro. The logic development of these terms and their functions are shown in Figure II-73.

AND: The "AND" function of the 3C micro instruction is logically obtained by anding the source register with the literal contained with the micro. The elements used to obtain the "and" are two Dual Full Adder/Subtracters (AFAN) placed in the add mode. These elements are the bottom two AFAN's shown in Figure II-73 with the 4 Bit Auxiliary Bus (4BTOnTO) and Micro Operator Bus (MOPOnBTO) as inputs. The output of the Dual Full Adder/Subtractor which is used for the "And" function is the generate output. The equation for the generate for the Dual Full Adder/Subtractor is as follows:

$$Gi = A_O * B_O = 4BTnnTO*MOPnnBEO$$

As can be seen from the above equation that the Dual Full Adder/Subtractor will produce a logical "and" which is used for the 3C micro.

OR: The "OR" function of the 3C micro instruction is obtained from a set of dual full adder/subtracter elements as shown in Figure II-73. The two elements used are the top two AFAN's in Figure II-73. In the case of the "OR" function, the elements are placed in the subtract mode by a constant true level to the mode control lines. The sum output is then used to obtain the "OR". The following equations illustrate how the OR functions are obtained:

$$Si = (A * \bar{B}) + (\bar{A} * B) = (MOPOOBEO + 4BTOOBTO) + (\overline{MPOPPBEO} + 4BTOOBTO)$$

If either the "A" or "B" input is true the output will be true. In the case where both "A" and "B" are true the or is obtained by separately sending the literal bit to the output multiplexor element as can be seen in Figure II-73.

EXCLUSIVE OR:

The "Exclusive Or" is obtained by using the propagate output of the bottom two Dual Full Adder/Subtractor elements shown in Figure II-73. The Exclusive Or function will allow the elements to be placed in the add mode and if either the literal bit or the source register bit is true then the output (propagate output) will be true. If both inputs are true then the propagate out is false which is the characteristic of the AFAN. The output which is used and sent to the output multiplexor elements are mnemonically referred to as 4BPRGnB. (4 Bit Binary Propagate).

INCREMENT: The increment function of the 3C micro instruction is a binary add of the source register to the 4 bit manipulate literal with any carry out resulting is ignored. The adder elements are shown in Figure II-73 and are the bottom two AFAN's which are shown. The Dual Full Adder/Subtractor elements are in the add mode as the term 4BTSUBDO (4 Bit Subtract) is false. The sum output (4BSUMnB.) is sent to the multiplexor where it is gated onto the 4 Bit Bus and sent to the destination register via the 24 bit Main Exchange.

DECREMENT: The decrement is obtained from the same two Dual Full Adder/Subtractor elements which were used for the Increment Function of the 3C Micro. In the case of the Decrement, the term 3CDECOB. (3C Decrement) will be true and cause 4BTSUBDO to be true to place the AFAN's in the subtract mode. In the case of the decrement, the literal is subtracted from the source register with the result (4BSUMnB.) being gated through the output multiplexor and subsequently to the destination register via the Main Exchange.

INCREMENT/DECREMENT TEST: The last two functions of the 3C micro to be discussed are the Increment or Decrement and "TEST". The increment/decrement functions are identical as those previously discussed. The difference occurs in that either an overflow for the increment or underflow for the decrement can be tested. If the test is to occur, the term IDTESTDO will be true to indicate that the result is to be tested. If an overflow or underflow occurs the carry/borrow output of the adder (4BCARO3) will be true and cause 3CSKIPBO to be true. 3CSKIPBO is sent to the Control Logic and will allow the next micro in the string to be skipped.

ADDRESS				CONDITIONS	
4BCNENDO	4BCNM2DO	4BCNM1DO	4BCNM0DO		
0	0	0	0	DISABLE	
1	0	0	0	3C SET	0
1	0	0	1	3C AND	1
1	0	1	0	3C OR	2
1	0	1	1	3C EXCLUSIVE OR	3
1	1	0	0	3C INCREMENT OR INCREMENT TEST, 3C DECMREMENT OR DECREMENT TEST	4
1	1	0	1	24 to 4, 6C*CLR/, IC*4 BIT SOURCE, 2C*4 BIT SOURCE	5
1	1	1	0	6C*CLR	6
1	1	1	1	10C*4 BIT SINK	7

Fig. II-74 4 BIT FUNCTION OUTPUT CONTROL ADDRESSING

4C BIT TEST RELATIVE BRANCH FALSE

The 4C Bit Test Relative Branch if the result is false will examine one of four bits in a designated register and if the bit selected is zero (false), then a branch relative will result. If the bit tested is true then the next micro in the sequence will be executed. The bit under test is designated by Micro Operator Bus bits five and six (MOPO5BTO and MOPO6BTO). The logic for the 4C micro is shown in Figure II-73. As can be seen the term 04C. . .F. will be true and be sent through an inverter where it is "anded" with BRNCH.F. If both inputs to the nand is false then the term 4C5CBRF. will be true

and allow the Control Logic to perform the Branch Relative according to the value in the micro. The term 4C5CBRF. will allow for the adding/subtracting of the relative displacement value to/from the value in the MAR(A) Register. It also prevents the normal MAR+1 upcount at that time.

5BIT TEST RELATIVE BRANCH TRUE

The Bit Test Relative Branch if the result is true will examine one of four bits in a designated register and if the bit selected is a one (true) than a branch relative will result.The next instruction in the sequence will be executed if the selected bit is false. This instruction is similar to the 4C which has been previously discussed and performs in an identical manner with the exception of how the branch enable term (4C5CBRF.) is produced. In the case of the 5C, if BRNCH.F. is true then the branch will occur as opposed to the 4C where BRNCH.F. had to be false to allow the branch. The logic is shown in Figure II-73. The multiplexor which produces the term BRNCH.F. examines the bit under test and will produce an output if the selected bit is true.

6C SKIP WHEN

The Skip When Micro tests a selected register for various conditions which exist between the source information and a 4 bit mask contained within the Skip When Micro. The logic test to be performed is selected by three variant bits which can designate eight different conditions. These conditions are as follows:

V=0 If any of the referenced bits is a "1", skip the next M-Instruction
V=1 If all of the reference bits are "1", skip the next M-Instruction
V=2 If the register is equal to the mask, skip the next M-Instruction
V=3 If all the referenced bits are "1", clear the referenced bits to zero without affecting the non-reference bits and skip the next M-Instruction
V=4 If any of the referenced bits are "1", Do Not skip the next M-Instruction
V=5 If all of the referenced bits are"1", Do Not skip the next M-Instruction
V=6 If the register is equal to the mask, Do Not skip the next M-Instruction
V=7 If any of the referenced bits is a "1", Do Not skip the next M-Instruction and clear the references bits to zero without affecting the non-referenced bits.

The 6C Skip When Micro will produce the Skip function of the term 6CSKIPC. is true. The term is produced as shown in Figure II-73. The ANY, ANY/, ALL and ALL/ functions originate from the EFAN shown which in turn receives its inputs from the bottom set of Dual Full Adder-Subtractors. For the ALL functions, the elements are placed in the subtract mode and for the ANY functions the add mode. The equal functions of the 6C are produced from the top set of Dual Full Adder/Subtractor elements shown in Figure II-73. The top set of elements are always in the subtract mode and the propagate output will be true if the inputs (literal or mask and source register) are equal then the term EQUAL.B. will be true and if the mask does not equal the source then EQUAL.B. will be false. According to which function has been selected by the variant, a skip may occur.

S-MEMORY PROCESSOR ROTATION LOGIC

The S-Memory Processor Rotation Logic is a shared rotator that is used for the rotation of data during the execution of the following Micros:

1. 7C Read/Write Memory Micro
2. 10C ROTATE/SHIFT T LEFT Micro
3. 11C EXTRACT T Micro
4. 4D SHIFT/ROTATE X or Y LEFT or RIGHT Micro
5. 5D SHIFT X AND Y LEFT or RIGHT Micro or the
6. 7D EXCHANGE DOUBLEPAD WORD Micro.

All of the above Micros use either a shift or rotate function with the exception of the 7D Micro, Exchange Doublepad Word, which uses the Rotation Logic as general storage to perform the exchange of the Doublepad Word with the contents of FA and FB. The Rotation Logic that is discussed in this section includes the Mask Generator, Rotation Control Logic, Rotator and the Memory Information Register which stores the Mask and the data that has been rotated.

BASIC FUNCTIONS

Since the Rotation Logic is shared, the functions of each portion will be discussed in a general format. The timing of each Micro for the generation of the mask, rotation and sinking is discussed in the individual description of the Micros

in Section II of this Manual. Generally speaking, the logic functions in the following manner:

Mask Generated
Mask Rotated (Various Micros do not rotate the mask)
Mask Stored in MIR (Mmeory Information Register)
Source Data Rotated
Output of Rotator (Source Data) Stored in MIR
Contents of MIR stored in sink register/memory

Figure II-75 shows all the Micros which use the rotation logic. In addition, it shows the number of bits placed in the mask, the amount that the mask must be rotated and the amount of rotation for the data.

In the column showing the number of bits in the mask, the terms labeled LIT refer to either the Literal value in the Micro or if the value within the Micro is zero then CPL (CREG00 thru CREG04) is selected. In the case where the number of bits in the mask is specified as 24-LIT, the 24's complement of the literal value (either Literal or CPL) is selected. In some cases neither of the three inputs are used but instead a constant value of either 23 or 24 is forced. In the cases where the value in the mask is the 24's complement (24-LIT) of the Literal, a subtraction must be done prior to sending the appropriate value to the Length Mask Generator. This is also done on Card C and may be used on the 10C and 4D Micros. Note that both of these Micros require a "left" shift. It should be noted at this time that the Rotator is a "right" oriented rotator. Therefore, if a shift left, for example, of eight bits is specified, then the rotator will actually rotate the data sixteen positions to the right which in effect is identical to a shift left of eight. Prior to the data being rotated, the mask will be rotated in a similar manner to give the appropriate truncation of the bits.

MASK GENERATOR

The Mask Generator is contained on S-Memory Processor cards A and B. Card A contains the least significant 12 bits of the Mask Generator and Card B contains the most significant 12 bits.

MASK GENERATOR INPUTS

Inputs to the Mask Generator are from Card C and Card F. The inputs from Card C are the five Length Enable terms (LENMK0CO thru LENMK4CO) and the input from Card F is a lift mask (LIFTMKFO) which will if true cause a mask of all bits (24 bits) to be generated. The lift mask term is normally true except when inhibited which is the case

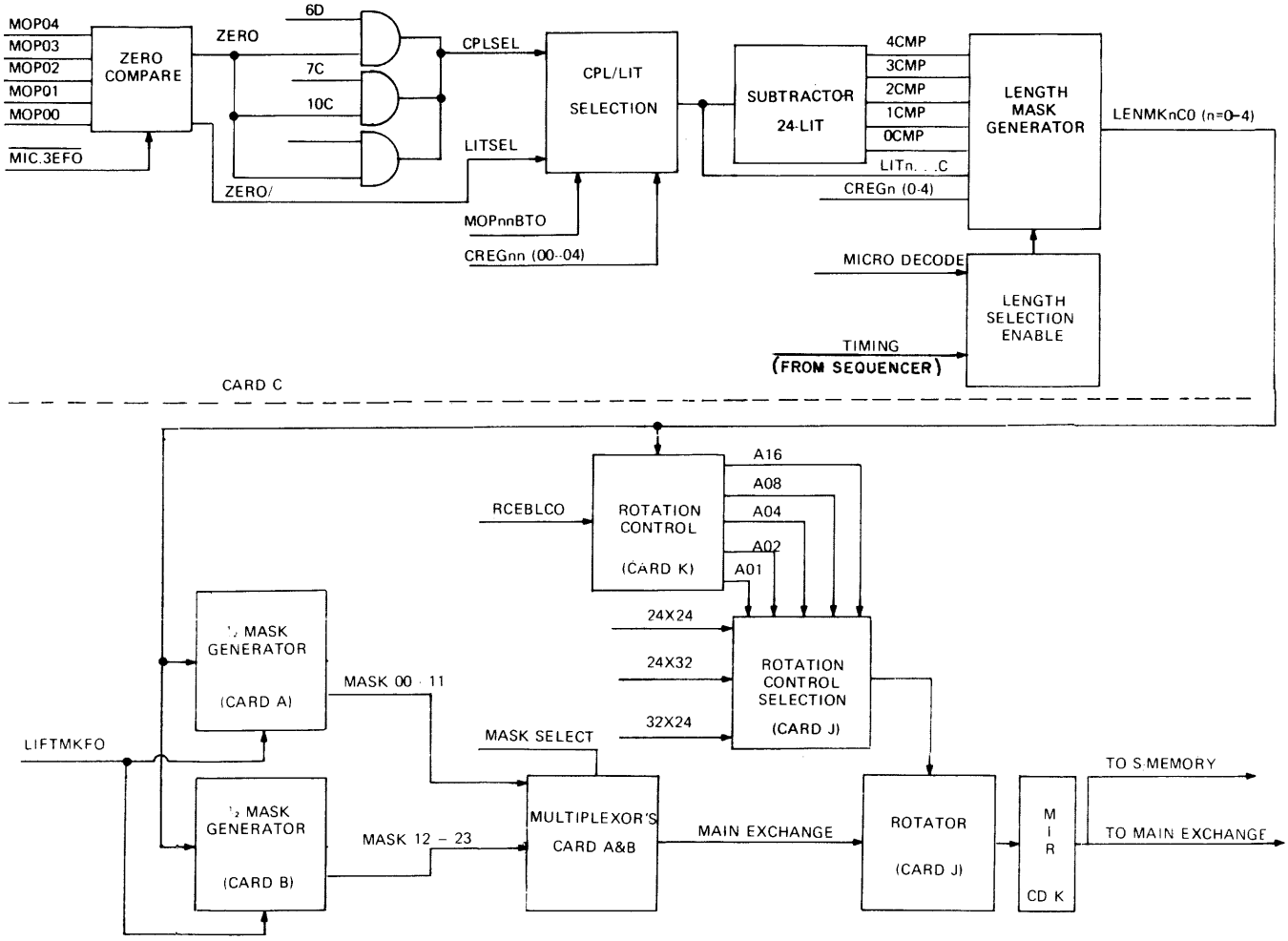
MICRO	NUMBER OF BITS IN MASK	AMOUNT OF MASK ROTATION	AMOUNT OF DATA ROTATION
11C EXTRACT T	LITERAL IN 11C	NO ROTATION	DETERMINED BY M11 ← M7
3F NORMALIZE X	23	23	23
5D SHIFT X&Y LEFT	23	24-1=(23)	24-1=(23)
5D SHIFT X&Y RIGHT	23	NO ROTATION	1
10C SHIFT T LEFT	24-LIT	24-LIT	24-LIT
10C ROTATE T LEFT	24	NO ROTATION	24-LIT
7C READ TWS-	LIT	NO ROTATION	32—VALUE
7C READ TWS+	LIT	NO ROTATION	32—LIT+BBA (LS 5 BITS)
7C READ TWS+ (CONSOLE)	24	NO ROTATION	32—24+BBA (LS 5 BITS)
7C WRITE TWS-	LIT	5 LSB BBA	5 LSB BBA
7C WRITE TWS+	LIT	LIT+5 LSB BBA	LIT+5 LSB BBA
7C WRITE TWS+ (CONSOLE)	24	24+5 LSB BBA	24+5 LSB BBA
4D SHIFT X OR Y LEFT	24-LIT	24-LIT	24-LIT
4D SHIFT X OR Y RIGHT	24-LIT	NO ROTATION	LIT
4D ROTATE X OR Y LEFT	24	NO ROTATION	24-LIT
4D ROTATE X OR Y RIGHT	24	NO ROTATION	LIT
7D EXCHANGE DPW	24	NO ROTATION	NO ROTATION

Note 1 TWS here means a negative field direction
TWS+ means positive field direction
Note 2 Subtraction from 32 is an inherent characteristic of the Rotator for the Memory Read operation
Note 3 When adding the 5 least significant bits (BBA) to the literal, any carry beyond the fifth bit is discarded.

Fig. II-75 ROTATION CONTROL AND MASK VALUES

when a mask is to be generated by the Length Enable Mask terms (LENMK0CO thru LENMK4CO). The five Length Enable Mask terms give a binary weight of the mask which is to be generated.

The Length Enable Mask terms are generated on Card C. Figure II-76 is a block diagram of the Rotation Logic with the portion shown for Card C concerning the generation of the LENMKnCO terms. As can be seen from the diagram, the Length Mask Generator has as its inputs five complement terms (nCMP), five literal terms (LITn. . .C) and five bits from the CP Register (CPREGn). The Length Selection Enable Logic will select as the output one of the three combinations according to the Micro which has been decoded and at the appropriate time within the Micro as generally controlled by the Sequencer on Card F.



√ Fig. II-76 MASK GENERATOR LOGIC

Having generated the Length Mask, the appropriate terms are sent to Cards A and B to generate the mask. In addition to the Length Mask terms, another term, MASKSTCO, is generated in order to inhibit the Lift Mask (LIFTMKFO). If a mask is not generated by the LENMKnCO terms then LIFTMKFO may be true to cause a mask of all 24 bits to be generated. The generation of the least significant 12 mask bits on Card A are shown in Figure II-77. The inputs to the Mask Generator (LEMNKnCO) have binary values from one thorugh 16. If, for example, the length of the mask were six bits, then LENMK1CO and LENMK2CO would be true and cause the mask output bits MASK00 through MASK05 to be true and MASK06 through MASK11 to be false on Card A. On Card B the Mask terms MASK12 through MASK23 all would be false. With the mask being generated from the Length Mask Enable Logic, the term MASKSTCO would be true causing the lift mask term, LIFTMKFO, to be false. The output of the Mask Generator is sent to a series of MFAN's where the Mask is "gated" onto the Main Exchange and subsequently sent to the Rotator. The Mask is enabled onto the Main Exchange by a series of decoding for the Micro and the timing as controlled by the Sequencer.

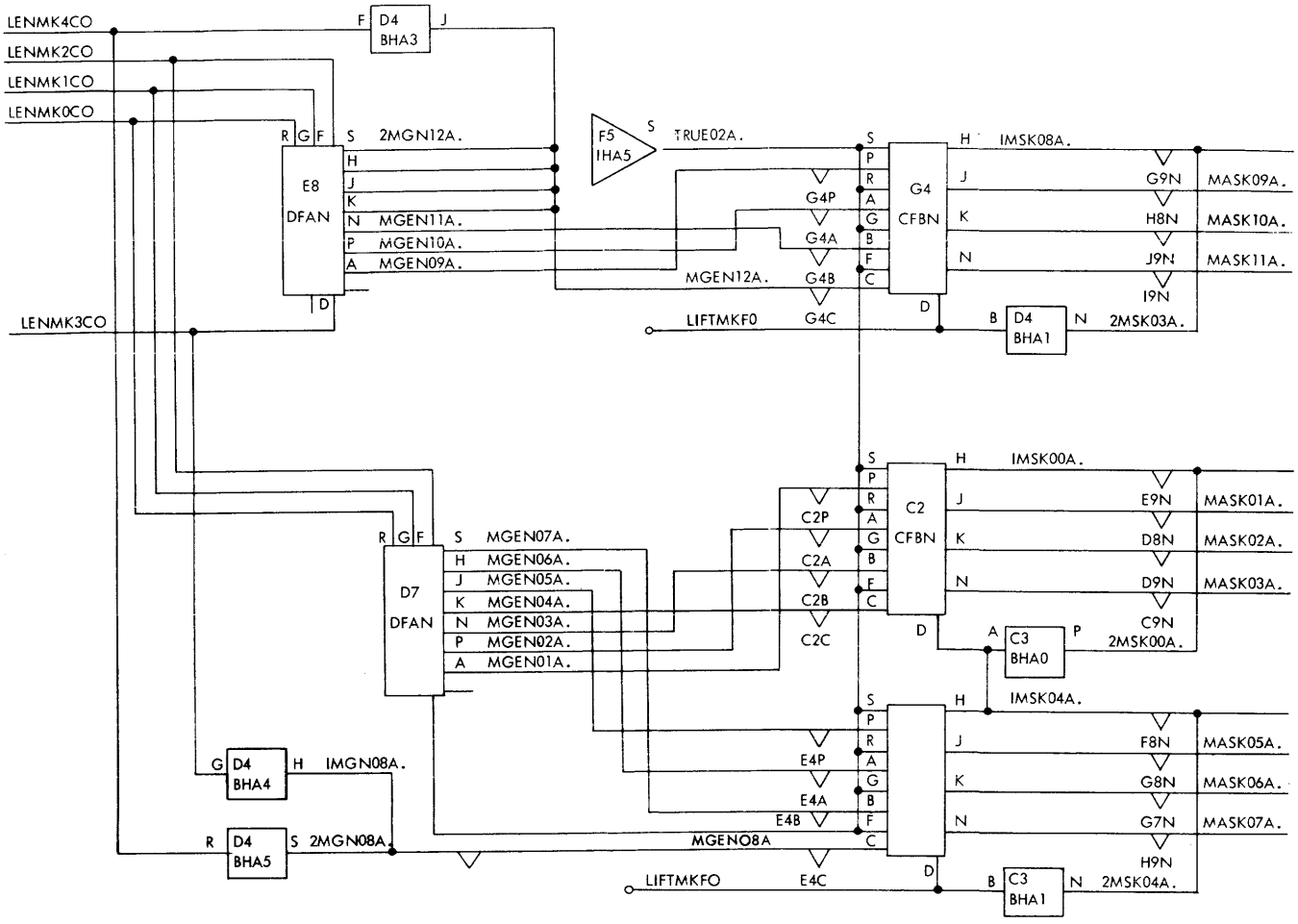


Fig. II-77 MASK GENERATOR BITS 00 THRU 11 (CARD A)

ROTATION CONTROL AND CONTROL SELECTION

The Mask having been generated and placed on the Main Exchange, it is now sent to the Rotator which will either send it directly to the Memory Information Register or rotate the mask depending upon the Micro that is being executed. The Rotation Control is located on Card K. See Figure II-78.

INPUTS AND OUTPUTS

The basic inputs to the Rotation Control are:

1. The Length Enable Mask terms
2. Bit Boundary Address for Memory operations
3. The Rotation Control Enable term (RCLEBLCO).

The outputs of the Rotation Control are:

1. A01. . .K.
2. A02. . .K1
3. A04. . .K1.
4. A08. . .K.
5. A16. . .K.

These levels are binarily weighted and dependent upon the input terms.

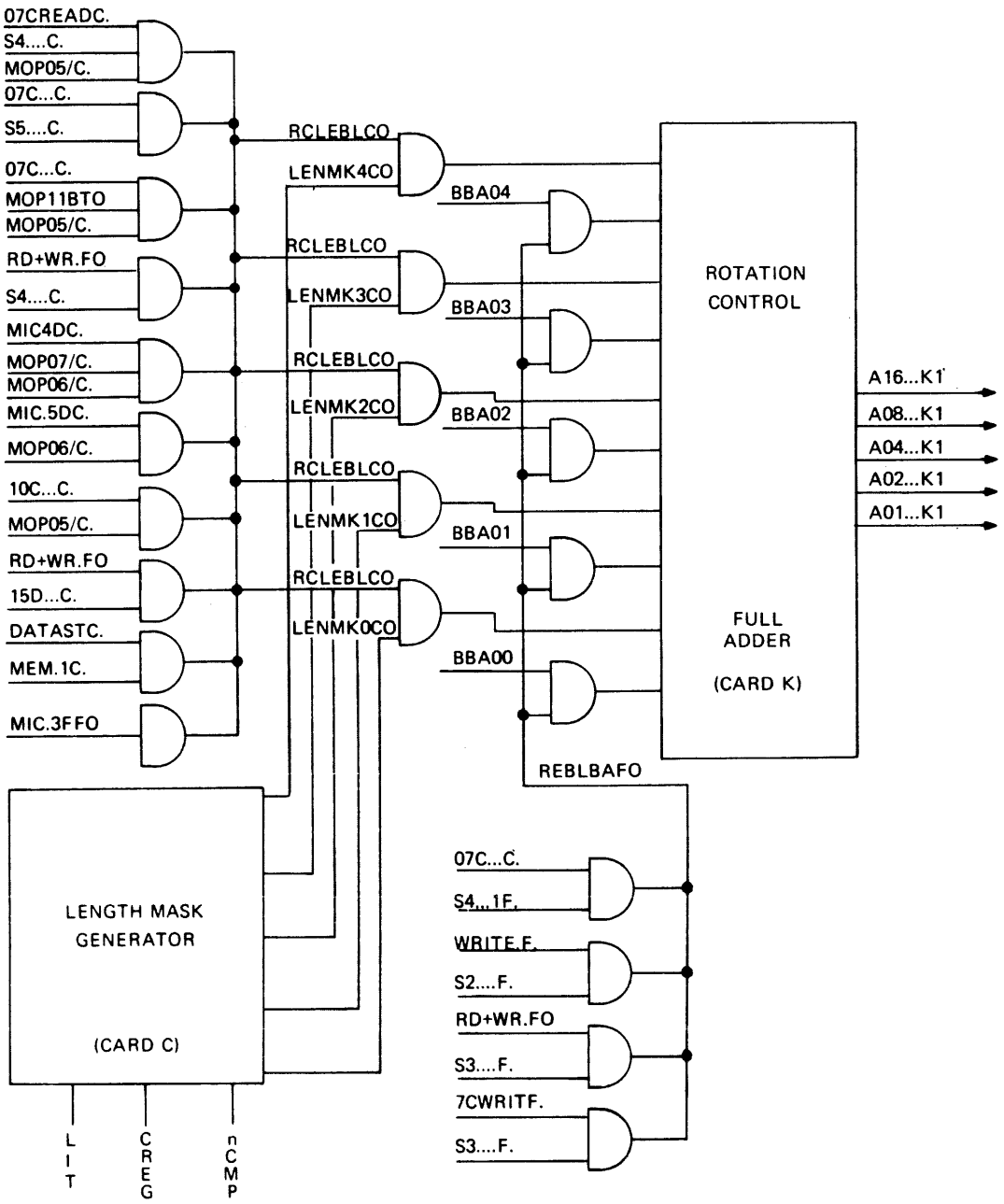


Fig. II-78 ROTATION CONTROL

FUNCTIONAL DETAIL

The chart in Figure II-67 gives the necessary binary weights from the Rotation Control for the various Micros and for either the mask or data rotation. Where no rotation is required, the inputs LENMKnCO and BBAnn.K. are inhibited into the logic and, therefore, the output levels will all be false. In the cases where a literal value is specified the term RCLEBLCO will be true to allow the Length Mask terms to be reflected at the output.

Example – Refer to Figure II-78. To illustrate, if LENMKOCO is true then AO1. . .K1 is true and each of the Length Mask terms correspond to an output Ann. . .K1 term. If the chart requires a rotation of LIT+ 5LSB BBA then both inputs are enabled to the Rotation Control and an add of the Literal and five least significant bits of the bit boundary address (BBA1nn.K.) occurs with the sum being placed on the Ann. . .K1 lines. In the case of the add if a carry out of the most significant stage occurs, it is ignored. The final condition for rotation could be that the rotation is directly under control of the least significant five bits of the Bit Boundary Address. In this case the five least significant

Functional Detail

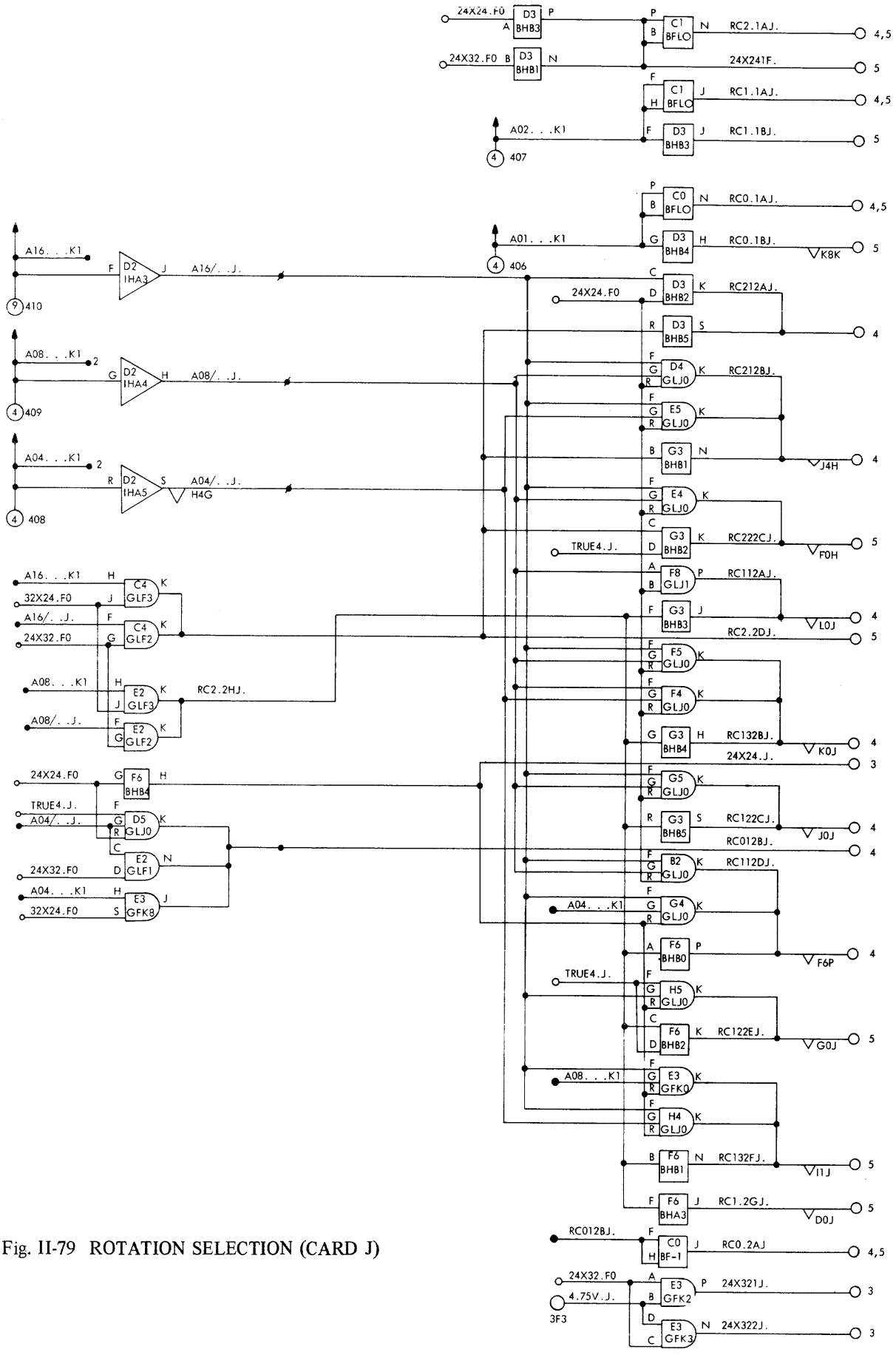


Fig. II-79 ROTATION SELECTION (CARD J)

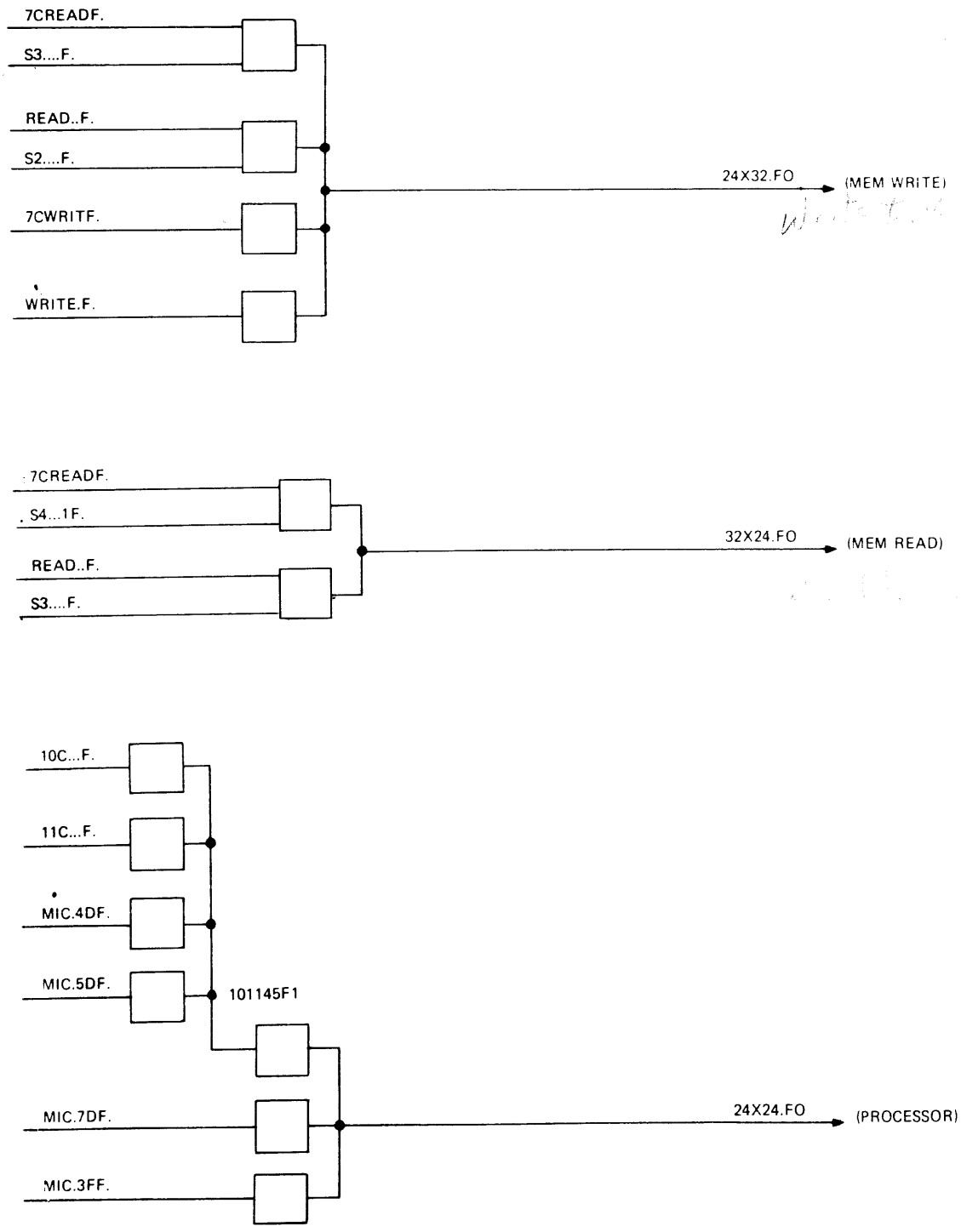


Fig. II-80 ROTATION SELECTION TERMS

bits are reflected directly from MAR(A) into the Ann. . .K1 lines.

The five Ann. . .K1 terms are sent to Card J where the Rotation Control Distribution and Selection will supply the appropriate Rotation Control terms to the Rotator.

The Rotation Control Distribution and Selection is shown in Figure II-79 and as can be seen, its inputs are the Ann. . .K. terms and three other terms referred to as 24X24.FO, 24X32.FO and 32X24.FO.

These three terms originate on Processor Card F and their development is shown in Figure II-80. The development of these terms are from the micro decoding and will allow rotation for either:

1. Memory Read – A Memory Read rotation is specified by the 32X24.FO term.
2. Memory Write – A Memory Write is specified by the 24X32.F0 term.
3. Processor Rotate–The Processor Rotate is signified by the 24X24.FO term and is developed as a result of the following:
   a. 10C SHIFT/ROTATE T
   b. 11C EXTRACT T
   c. 4D SHIFT/ROTATE X or Y
   d. 5D SHIFT X AND Y LEFT
   e. 7D EXCHANGE DOUBLEPAD WORD
   f. 3F NORMALIZE X.

One of these three levels will be true to the Rotation Control Distribution and Selection Logic to allow the production of the appropriate rotation control terms.

ROTATOR

The Rotator, located on Card J, consists of 64 Multiplexor elements arranged in two stages of 32 elements per stage. It is the function of the Rotator to rotate the input data on any given bit such that the bit can be placed on any one of the 32 output lines.

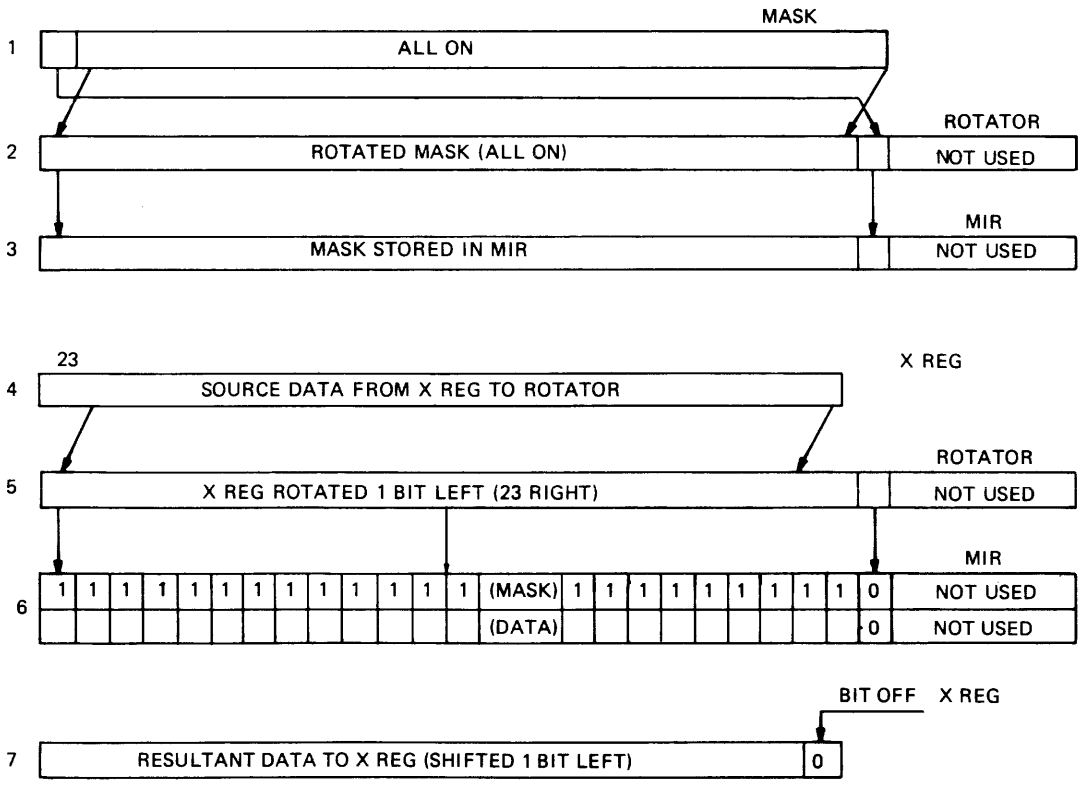


Fig. II-81 ROTATOR EXAMPLE

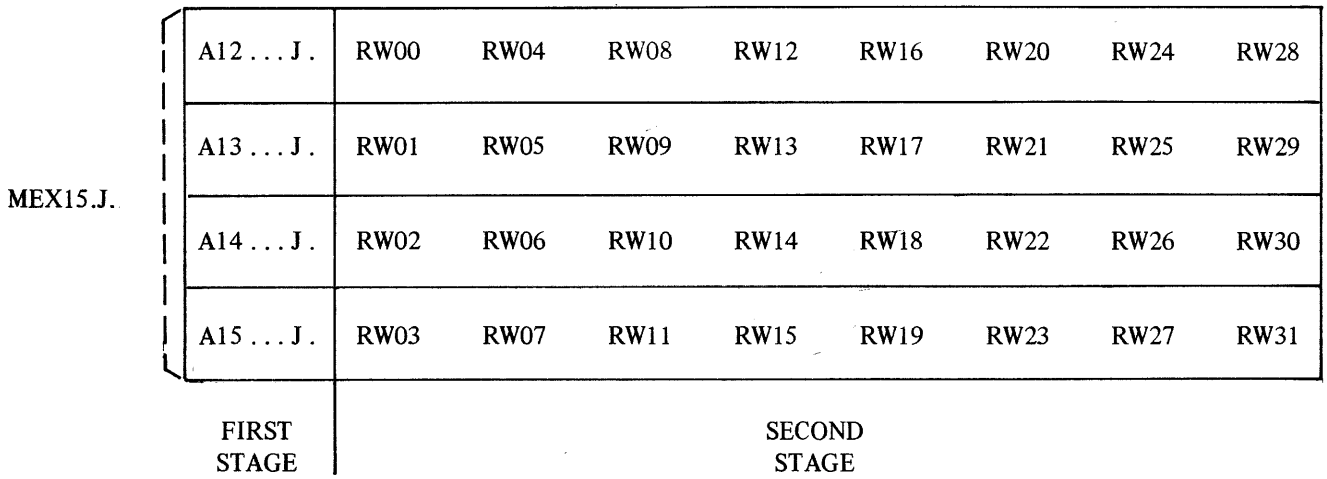
FUNCTIONAL DETAIL

On Processor operations (24X24.FO), the Rotator's function is to rotate the mask such that the mask will correspond to the appropriate bit positions in the Memory Information Register where an output is desired.

Example: Assume the micro is a 3F Normalize X. The Mask Generator will generate a Mask of 23 bits and send the 23 bits to the Rotator. It is then the function of the Rotator to rotate the mask 1 bit to the left (23 bits to the right) such that when data is rotated in a like manner (1 bit to the left or 23 to the right), 23 bits will be placed in the MIR and where the mask bit was off a zero bit will automatically be obtained from the Memory Information Register to the sink (X Register). The operation for the generation of the mask, rotation of the mask and rotation and storage of the data for the 3F Normalize X is as follows:

1 Mask is generated with the least significant 23 bits on and most significant bit off.
2 Mask is shifted (rotated) 1 bit to the left.
3 Mask is stored in the Memory Information Register.
4 Source data is obtained from the X Register to be rotated.
5 X Register rotated (shifted) 1 bit to the left (23 to right).
6 Rotated Data is sent to MIR and input where a mask bit had been previously set. (Truncates LS Bit to fill right zeros)
7 Result Data shifted 1 bit to left sinked to X Register.

The Rotator is arranged such that any one input to the first stage may be selected to any one of four outputs. An example of this would be to use the Main Exchange bit fifteen as an input. (See Figure II-82). By selecting the appropriate Rotation Control Levels, MEX15.J may appear at A12. . J., A13. . J., A14. . .J. or A15. . .J. Any one of these outputs of the first stage is then sent to the second stage of the rotator and appears at the input to eight multiplexors. Again having the appropriate control levels enabled will allow selection of one of the four Ann. . .J. levels to the final output of the Rotator. Using this arrangement any one bit which is input to the rotator may be selected to any one of the 32 output lines referred to as RWnn. .J1.



√ Fig. II-82

The output of the Rotator, which is either the rotated mask or rotated data, is sent to the Memory Information Register. In some of the cases shown in Figure II-75 no rotation is desired. In those cases, the information is still passed through the rotator before being sent to the Memory Information Register.

MEMORY INFORMATION REGISTER

The Memory Information Register is a multi-function register within the S-Memory Processor. On a Memory Read operation for data (as opposed to MFETCH), it will store the data which has been read and rotated and consequently place the rotated data on the Main Exchange. On a Memory Write operation, it stores the data that is to be written into a specific memory location. Before the write can occur, however, the MIR must first store a mask which will allow the data read from memory and the data to be written into memory to be "merged". If the mask bit is on, then the data to be written will be obtained from the source register which has been rotated. If a mask bit is off then data will be obtained from the bit read from memory. In addition to the basic function of a Memory Information Register, MIR serves as a

storage register for various processor shift/rotate functions. It is also used as a general purpose storage for the 7D Exchange Doublepad Word micro. Because of the multiple independent functions, MIR is discussed according to its function for the various operations.

READ FUNCTION

The first function of MIR to be discussed is for a Memory Read operation. Operation is as follows:

1. Mask Generated for number of bits to be read.
2. Mask is sent to the Rotator and NOT rotated.
3. Output of Rotator causes the MIR bit to set as MSKST2K. is false to place the MIR in the J/K mode. Where a "1" is obtained from the Rotator, the corresponding MIR bit sets and where a "0" is obtained from the Rotator the MIR bit remains reset.
4. Data is read from Memory and sent to the Rotator which will rotate the data such that the data bit in the most significant address location read will be placed in MIR bit W31XOOKO.

For an example assume the Bit Boundary Address is zero and a read of 24 bits is specified. See Figure II-83.

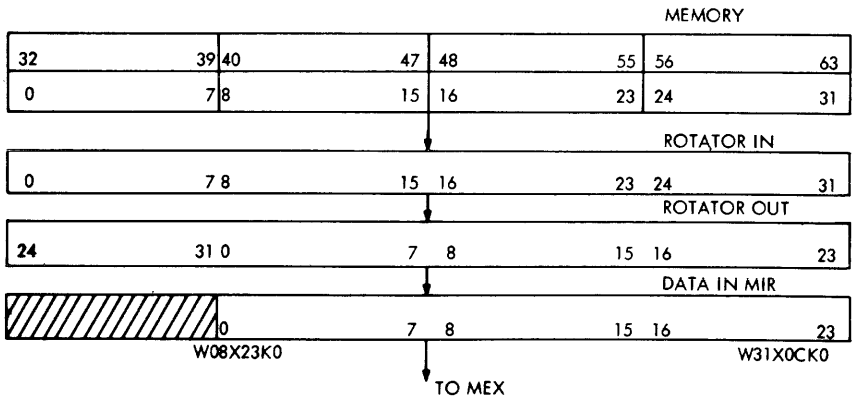


Fig. II-83

In example shown in Fig. II-83, a total of 32 bits were read from memory and rotated to the right by eight positions. Because the operation was described as a read of 24 bits, a mask had previously been generated and set into MIR bit W08X23KO thru W31X00KO.

been set, a rotator output can be set into MIR. Where a mask bit is off, the MIR will not receive information from the Rotator. In examining the mnemonic names of the MIR bits, the first number is the position of the rotator input and the second number is the bit number to the Main Exchange. An example of this is the W08X23IO term. The 08 signifies the input was from the Rotator eight bit (RW08. .K1) position and the 23 indicates the output of that position will go to the Main Exchange bit twenty-three (MEX23BKO). Figure II-84 is a diagram of one bit from the Memory Information Register.

When the Mask is to be placed in the MIR, the term Mask Set (MASKSTCO) is true which causes the output of the inverter (MSKST2K.) to be false. MSKST2K. false will disable the AND gate and allow the FFAN to be placed in the J/K mode of operation. If the Mask Bit is true from the Rotator, the RWnn. .J1 term will be true and when the clock trailing edge occurs the flip-flop will set. Note that the clock is CLK4. .KO*MASKSTCO for the setting of the Mask into MIR.

The Memory Read Data is then read and rotated with the output of the Rotator being sent to the MIR on the RWnn. .J1 lines. Notice these 32 lines are inputs to the J-K side of the FFAN. If a Mask Bit had been previously set into the MIR, the term MASKnnK. will be false thus placing the FFAN in the J-K mode and allow information from the Rotator to be set into MIR. If the data bit is a "0" then the FFAN resets with the trailing edge of the clock. Note that in this case the clock is DATASTCO (Data Set) and CLK4..KO. If a Mask Bit had not been set into the MIR then the MASKnnK. true and MSKST2K. true, the FFAN is placed in the "D" mode of operation. The "D" input to the FFAN is the Memory Read Data ANDed with 24X321J which is false for the Memory Read Operation. When the clock occurs, the FFAN remains reset.

WRITE FUNCTION

The Memory Write operation is similar to the Read with the exceptions being that the Mask generated is first rotated and then placed in MIR. The Mask bits which are "on", correspond to the new data (source register data) and the mask bits

"off", will correspond to old data, or in other words, data which has been read from memory and is to be written back. In the case of a write, the MIR acts as a "merger". When the Memory Read Data MRDnn.MO is present it is ANDed with the 24X321J term which is also true for a write. The result being that those MIR bits with the Mask "on" will be in the J/K mode and receive their information from the Rotator. In contrast those bits with the Mask bit "off" will be in the "D" mode and receive data from memory. Refer to Figure II-85.

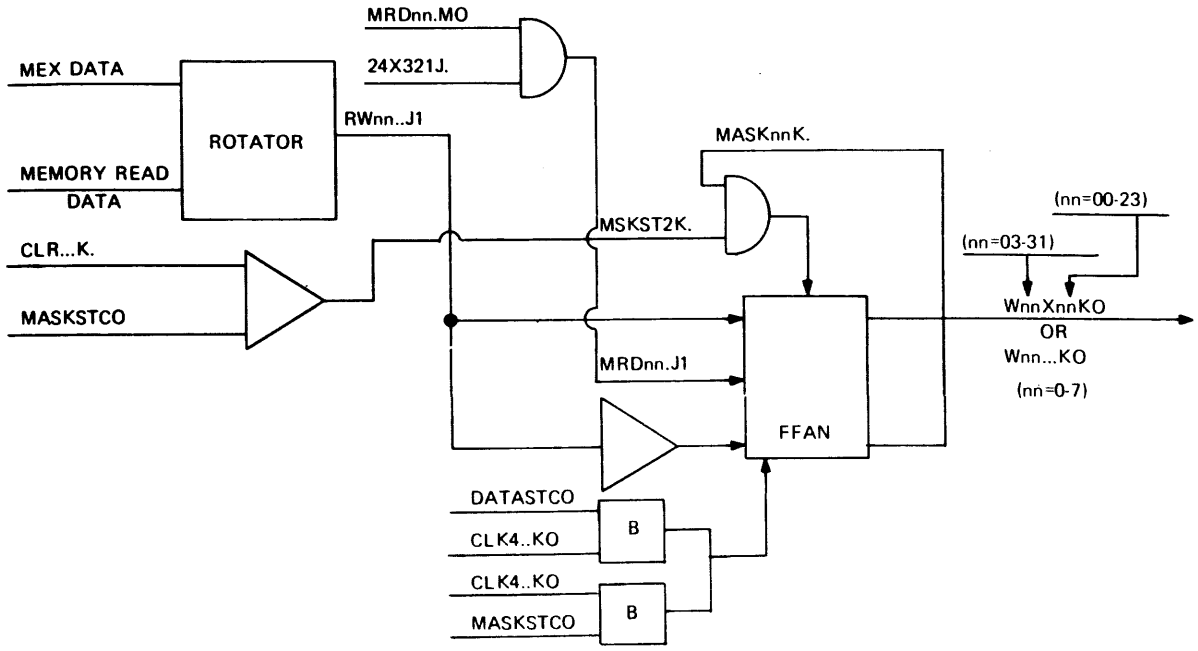


Fig. II-84 MEMORY INFORMATION REGISTER (CARD K)

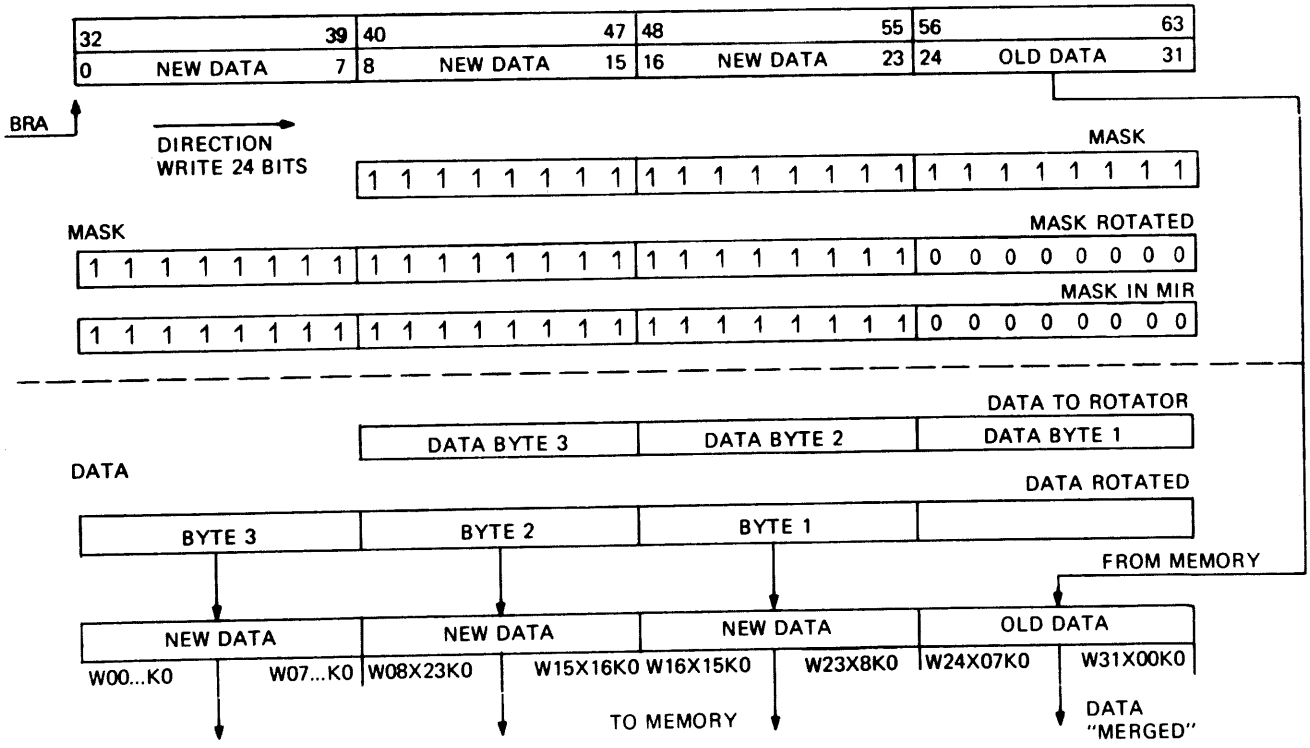


Fig. II-85 MEMORY WRITE OPERATION OF MIR

The output of the Memory Information Register is 32 bits which are sent to Memory via backplane wiring and written in the appropriate location as determined by the address in MAR(A). In examining the mnemonic names of the MIR output it can be seen that the first two numbers in the mnemonic correspond to the bit position of the data to be written. Bits for Module Zero are referred to as WOO. . .KO through WO7. . .KO, bits for Module One are referred to as WO8X23KO through W15X16KO, for Module Two they are referred to as W16X15KO through W23X08KO and for Module Three as W24X07KO through W31X00KO. In the write operation the last two numbers have no specific significance in the mnemonic name.

PROCESSOR FUNCTION

The Memory Information Register when used for Processor operations functions identically to the Memory Read operation. The only difference in the two operations is that on the Processor operation the source data is obtained from a register within the processor rather than memory. In either case the data is rotated and set into the MIR where a mask bit is "1". The data out of MIR is then placed on the Main Exchange at the appropriate time according to the individual micro timing.

MAIN 24-BIT EXCHANGE

The Main 24-Bit Exchange consists of 24 Bi-directional Bus lines used to transfer information through the Processor. The contents of the MAIN Exchange is dependent on the State of the Processor (RUN or HALT), the Mode of Operation (RUN, STEP, or MTR) and the particular Micro currently executing. Figure II-86 illustrates a Block Diagram of the Main Exchange. The connections to/from various registers and functional logic is shown as well as the number of lines connecting these registers and logic to the Main Exchange. Each particular area or Register within the Processor which causes information to be gated to or from the Main Exchange is explained separately in this manual. Reference should be made to those areas of concern for details.

√ MAIN 24-BIT EXCHANGE GATING

Typical gating used throughout the system to gate information on to the Main 24-Bit exchange is shown in Figure II-87. Card E (3 of 4 and 4 of 4) contains 24 Multiplexor Chips (MFANs) which are used to gate the M-Register, ML-Register, U-Register, I/O Bus, MAXS, and the Console Switches to the Main Exchange.

The EFAN at Location J9 provides generating an "Address" which is applied to all 24 MFANs. Eight (8) "addresses" are possible, as the three levels MBUS02FO, MBUS01FO, and MBUS00FO will represent a binary value from 0 to 7 which is applied to each of 24 MFANs.

The inputs to the EFAN are defined as follows:

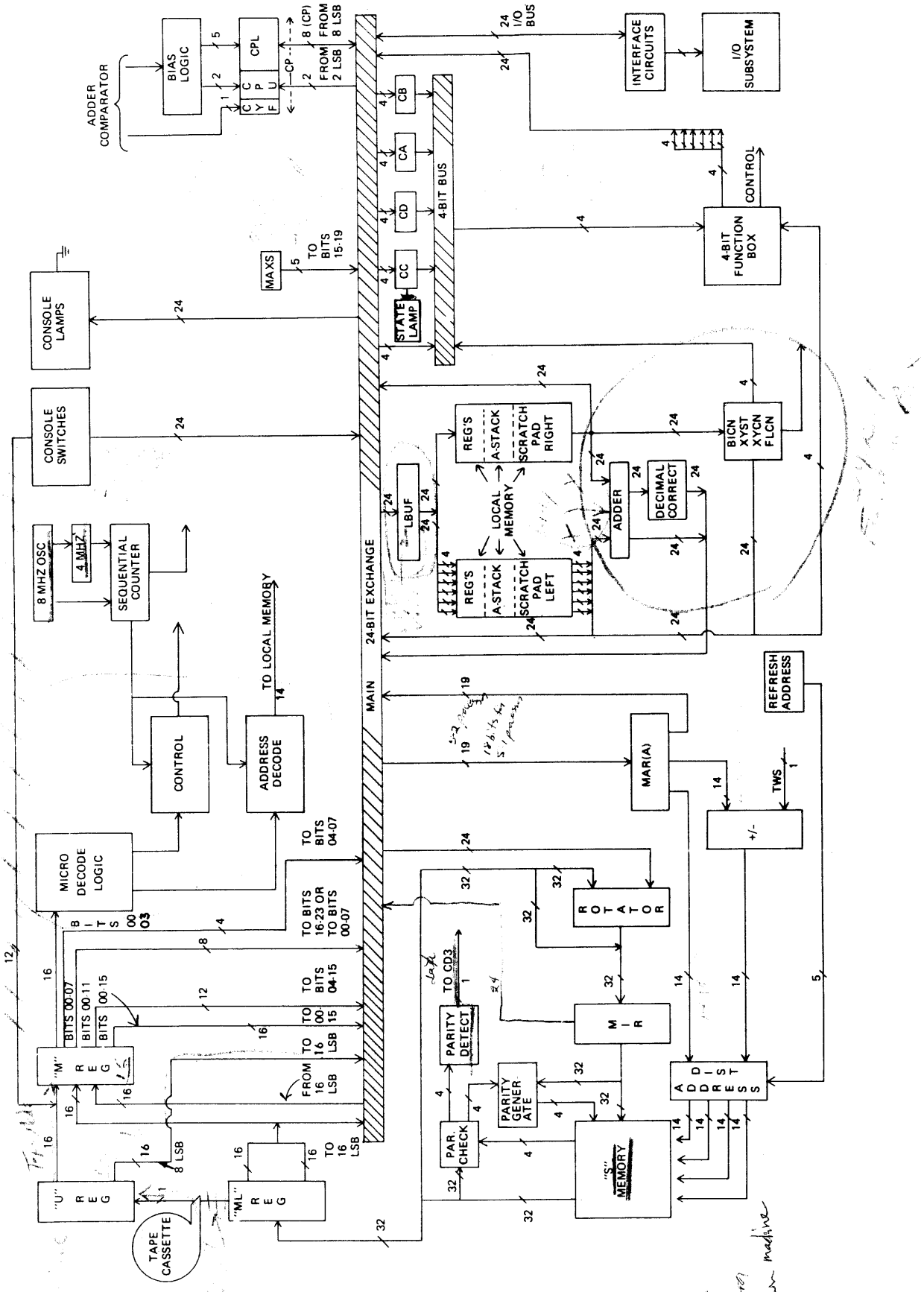
1ORCO.F. 1C and 2C Micro and DATA is Sink
SWISELF. Load Button Depressed
+ Console Switches set to Write and Load
Timing Depressed
MAXSSEF. 1C or 2C Micro and MAXS is source
24LMTRF. 1C or 2C and U-Register is Source (Run Mode only)
+ 9C Micro * UFULL.EO
2YLRUNF. 9C Micro * RUN or STEP Mode
12BTBRF. 123C or 145C Micro
4BITBRF. 4C or 5C Micro
MSOR.F. 1C or 2C * M is Source (Halt state)
+ 8C Micro

Once an "address" is established the value of the corresponding bit position input to each of the 24 MFANs is gated to the Main 24-Bit Exchange.

If, for example, MBUSOOFO is true and MBUSO1FO and MBUSO1FO are false, the contents of the M-Register Bits 03-00 will be gated to the Main 24 Bit Exchange Bits 07-04 respectively.

The enable input of each MFAN is either MBUSE1E., MBUSE2E. or MFUSEBFO as shown. When the U-Register is Sourced (Run Mode) MBUSEBFO is false thus gating to the Main Exchange Bits 16-23 is Disabled.

When the 8C Micro is executed, MBUSE2E. is false, thus gating to the Main Exchange Bits 08-15 is disabled. Only the 8 LSB (Literal) are gated to the Main Exchange Bits 00-07.



√ Fig. II-86 BLOCK DIAGRAM MAIN 24 BIT EXCHANGE

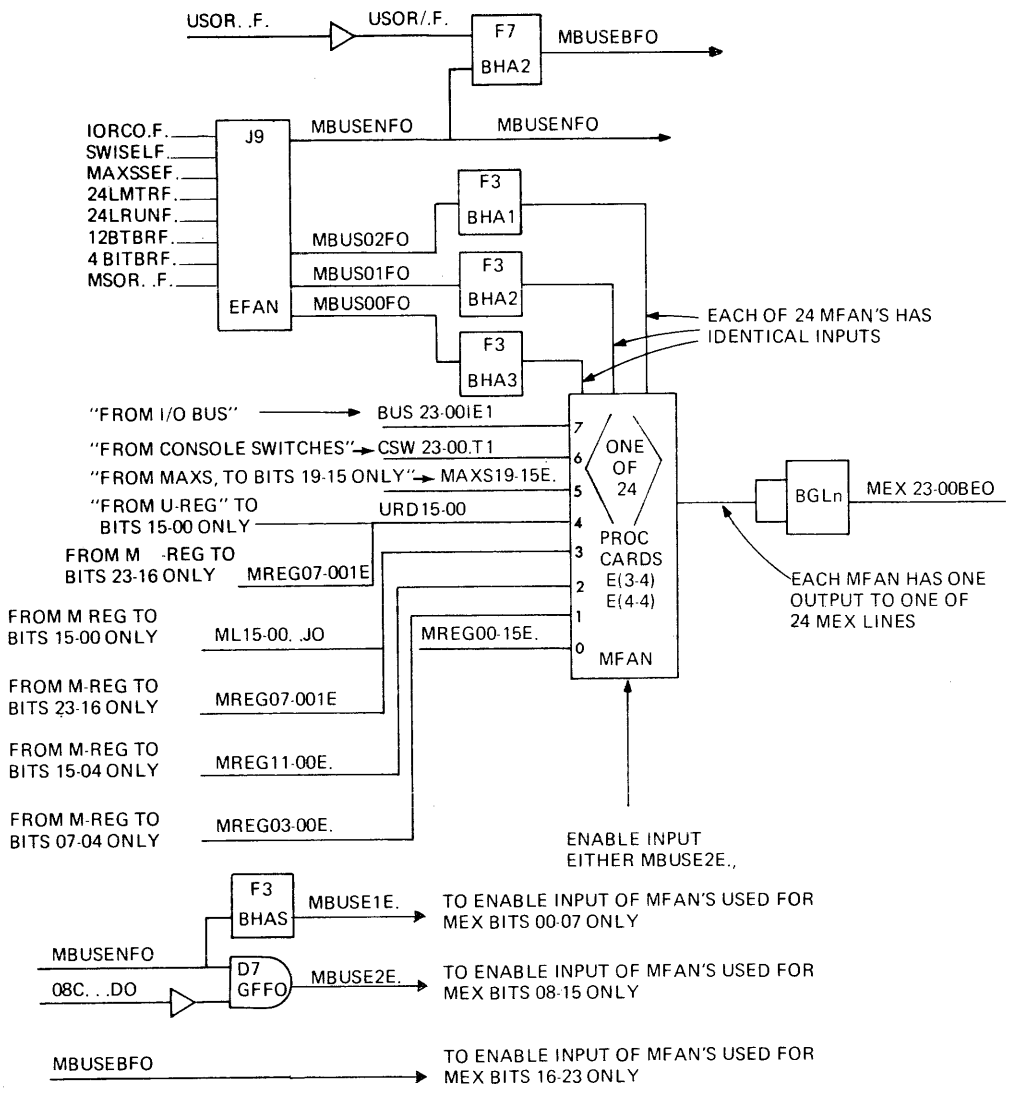


Fig. II-87 MAIN 24-BIT EXCHANGE GATING PROCESSOR CARD E

√ M AND ML REGISTERS

The Micro Register (M-Register) and Micro Latch Register (ML-Register) are used primarily for the execution of Micros. In certain cases, however, the registers will contain data other than Micros. The M & ML Registers Block Diagram, Figure II-88, illustrates the data transfer paths to and from each of the registers. The Mode of Operation (RUN, TAPE, or STEP) must also be considered when determining the particular type of data (whether Micros or data) that might be transferred to and from the registers. In addition to the mode of operation, the Micro currently executing must also be considered.

One source of information is shown in Figure II-88 for the ML-Register. This source is 32 bits of Memory Read Data from S-Memory. Only 16 bits of the 32 bits read will be used at a given time. The ML-Register's information can be gated either to the M-Register or to the Main 24 bit Exchange. the 16 bits of information used can be from either "half" of the ML-Register; the portion used is determined by the value of the Memory Address Register (MAR(A)). The M-Register has three sources of information. The U-Register, the ML-Register (either "half") or the Main 24 bit Exchange. The M-Register's information (Micro's) can be gated either to the Micro Distribution Bus or to the Main 24 bit Exhcnage. When gating is to the Main 24 bit Exchange the Micro in the M-Register is also gated to the Micro Distribution Bus. The "basic" conditions and data transferred to and from the registers is shown in Figure II-88.

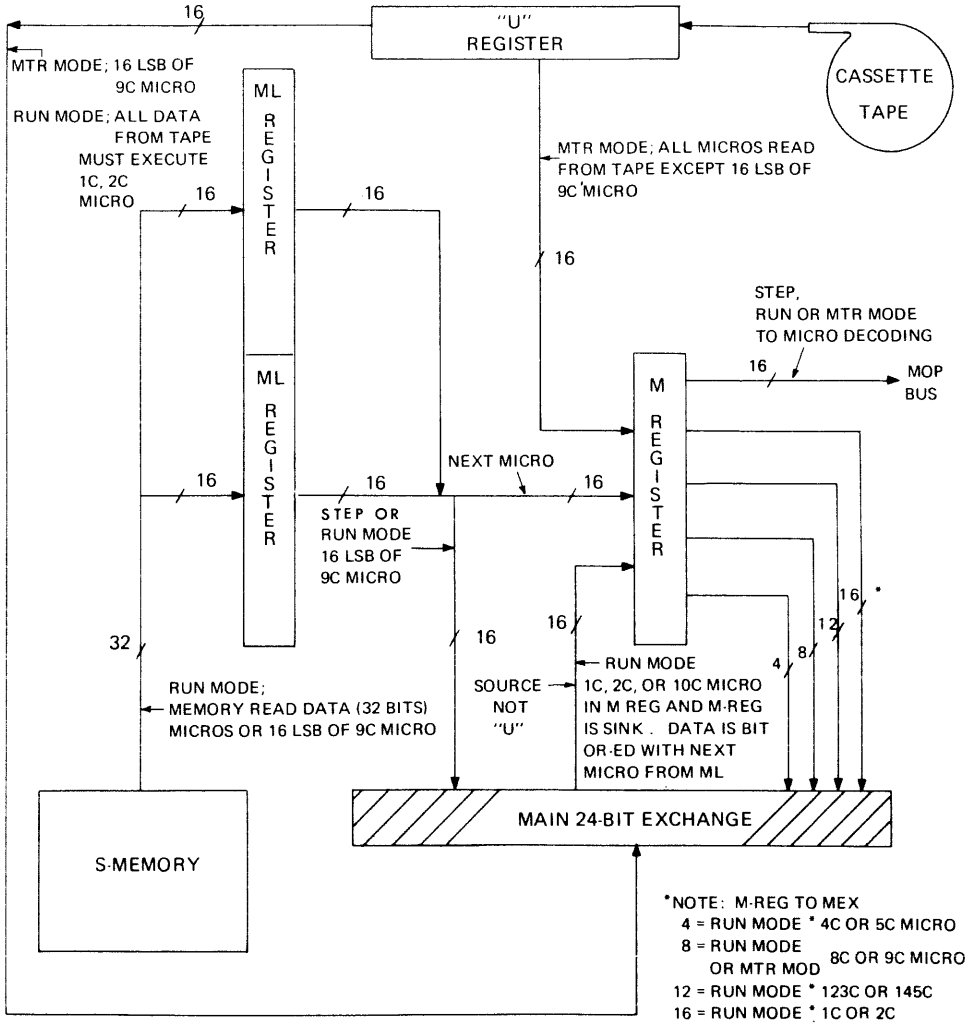


Fig. II-88 M AND ML REGISTERS BLOCK DIAGRAM

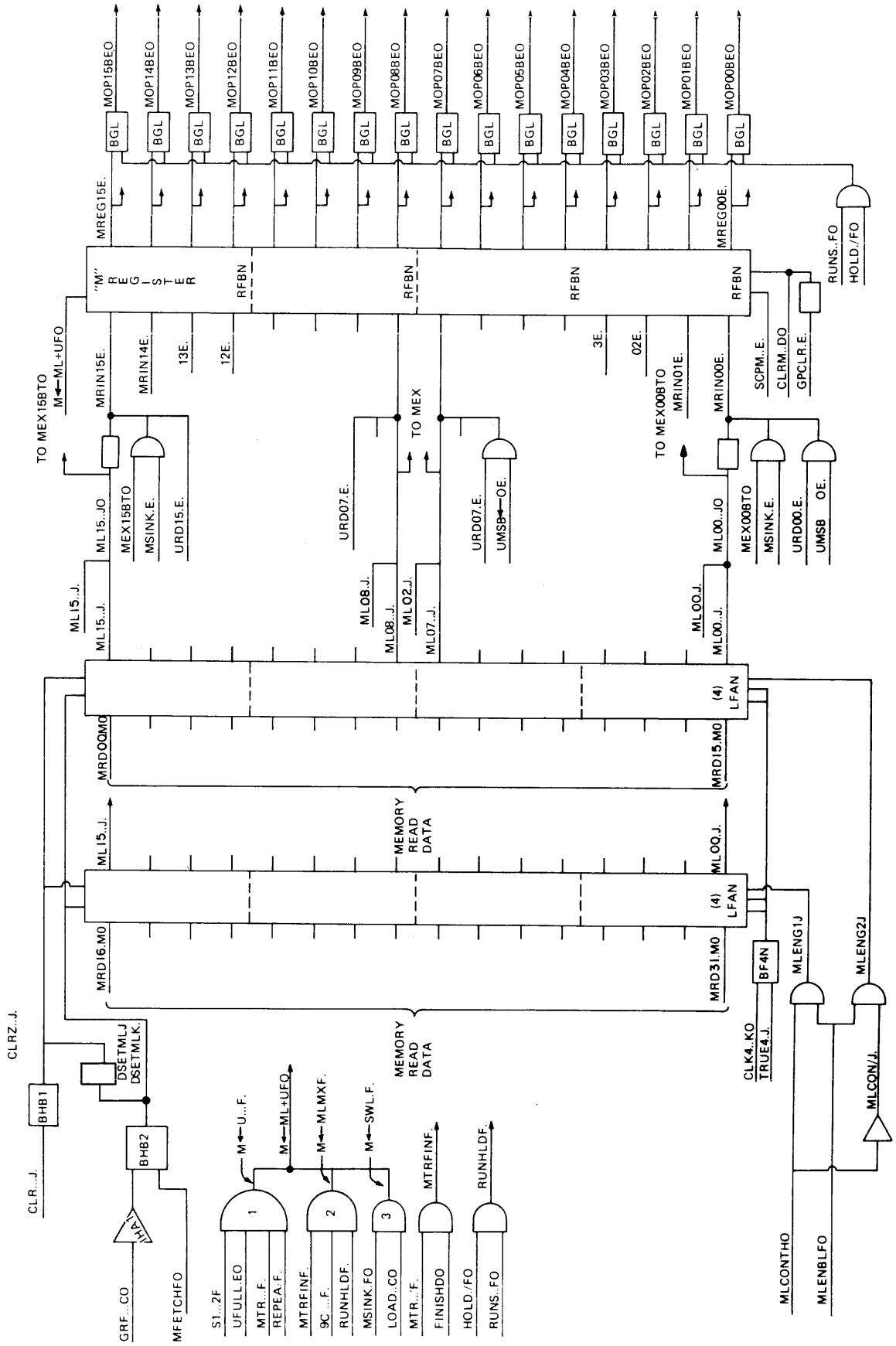
√ M-REGISTER

The M-Register (Micro Register) is a 16-bit register consisting of four 4-bit registers (RFBN's). The register is used to hold the current active Micro. The Logical Diagram of the ML & M-Registers, Figure II-88, illustrates the M-Register, the 16 inputs and outputs to and from the Register, and the clock, clear, and mode control levels to the register. The clock input (SCPM. .E.) is the 4MHz clock (CLK4. .KO) through one buffer. The clear input (CLRM. .DO) is true when either General Processor Clear (GPCLR.E.) is true or when the term CLRM. .DO is true. CLRM. .DO is true when 09C. . .D. and FINISHDO are true which occurs during the execution of the 9C Micro (Move 24-bit Literal) in either the RUN, STEP or TAPE mode. USOR. .D. and FINISHDO also produces CLRM. .DO and is true when the U-Register is sourced in either the RUN or MTR Mode. The mode enable input (M ML+UFO) connected to the MO input causes the four registers to be the the D-Set mode when true. When M ML+UFO is false, the register is in the Bit Set mode. The output reflects the contents of the register at all times.

M-REGISTER OUTPUTS

The sixteen outputs of the M-Register (MREG 15 thru 00 E.) are AND-ed through sixteen buffers with RUNS. .FO and HOLD./FO. The output of these sixteen buffers are the sixteen lines of the Micro Distribution Bus (MOP 15 thru 00 BEO). Refer to Figure II-89. These sixteen MOP lines (15 thru 00) are distributed throughout the System to the Micro decoding logic. The conditions necessary to cause RUNS. .FO and HOLD./FO. to be true are explained separately in this Manual.

Functional Detail



√ Fig. II-89 "ML AND M" REGISTERS

In addition, the output of the M-Register can also be gated to the Main 24-bit Exchange. 8 Micros when executed are capable of gating either all or part of the contents of the M-Register to the Main 24-bit Exchange. The Micros which have this capability are listed below with the bit positions of the M-Register affected as source as well as the sink position to which they are gated to the Main 24-bit Exchange.

1 & 2. 1C or 2C Micro and the M-Register selected source; M-Register bits 00 thru 15 to the Main 24-bit Exchange bits 00 thru 15.

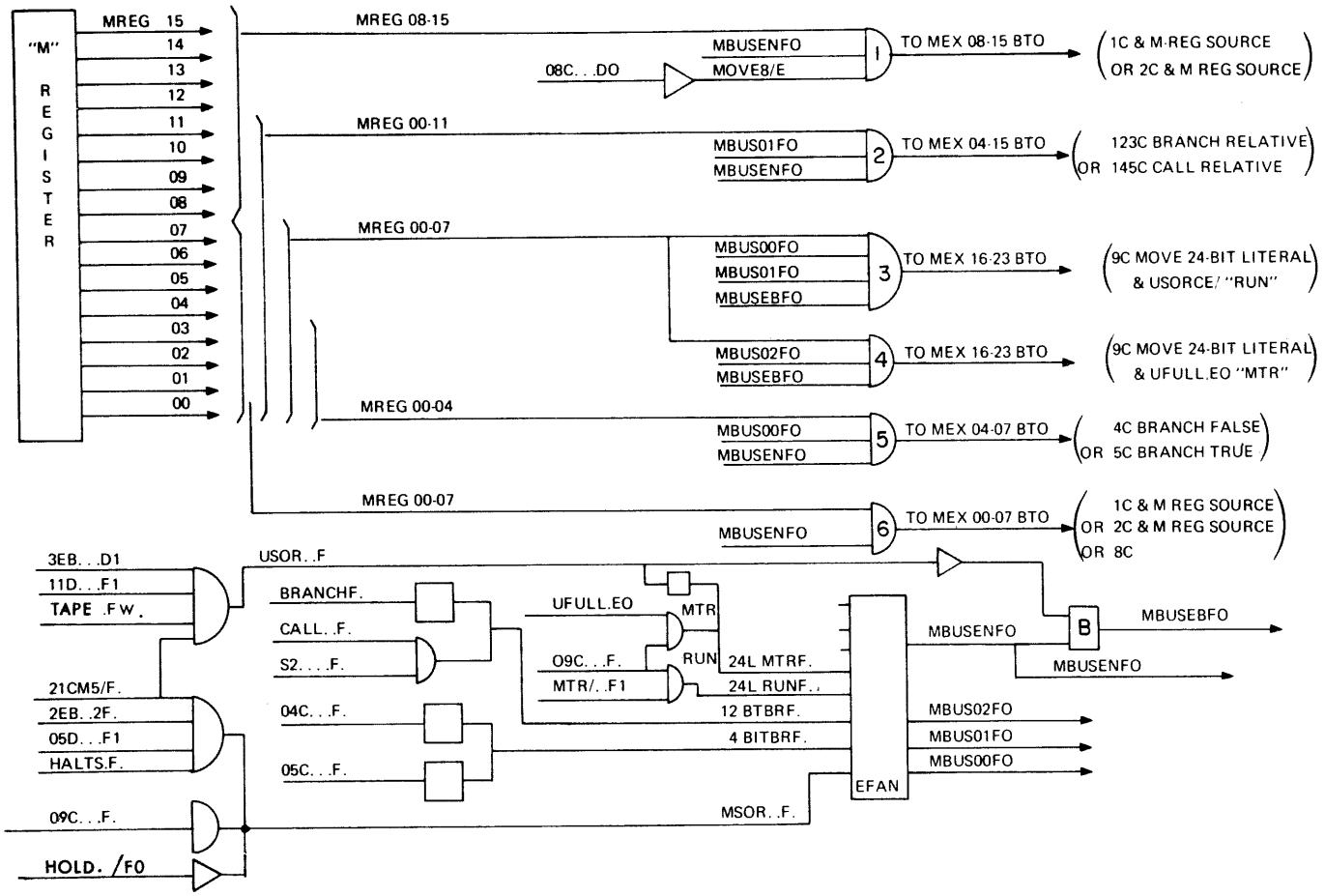
3 & 4. 4C or 5C Micro (when the Branch is to be executed); M-Register bits 00 thru 04 to the Main 24-bit Exchange bits 04 thru 07.

5 & 6. 123C (Branch Relative) or 145C (Call Relative) Micro; M-Register bits 00 thru 11 to the Main 24-bit Exchange bits 04 thru 05.

7. 8C Micro; M-Register bits 00 thru 07 to the Main 24-bit Exchange bits 00 thru 07.

8. 9C Micro (TAPE Mode & UFULL.EO or RUN Mode); M-Register bits 00 thru 07 to the Main 24-bit Exchange bits 16 thru 23.

The enable levels and the generation of the same which gate the various bits of the M-Register to the Main 24-bit Exchange are shown in Figure II-90. The Micros which cause a branch to occur (123C, 145C, 4C, and 5C) cause the M-Register's value to be shifted four places higher on the Main 24-bit Exchange. This is due to the fact that Micros are located in S-Memory at either a Key Byte address of 0 or 2. The 9C Micro moves the LSB of the 9C Micro the 8 MSB of the Main 24-bit Exchange. The 16 LSB of the Literal are either the next 16 bits of information read during a concurrent MFETCH operation when in the RUN Mode, or the 16 bits of the U-Register when in the TAPE Mode.



√ Fig. II-90 M-REGISTER GATING TO MEX

M-REGISTER INPUTS

The sixteen inputs to the M-Register (MRIN 15 thru 00 E.) are each the output of a three wire OR gate as illustrated in Figure II-89. The source of these sixteen inputs is either from the ML-Register (MLR), the Main 24-bit Exchange (MEX), or the U-Register (URD). The source of these sixteen inputs to the M-Register is determined by control logic which gates one or two of these sources to the inputs of the M-Register.

The U-Register data is gated to the inputs to the M-Register with UMSB OE., the Main 24-bit Exchange (bits 00 thru 15 ONLY) are gated with MSINK.E., and the ML-Register is gated with either MLENG1J. or MLENG2J. It is also possible, when the M-Register is designated as the sink register, to gate the ML-Register and the MEX 15 thru 00 to the inputs of the M-Register. When this occurs, the ML-Register is bit "OR"-ed with the MEX. It should be noted that the sixteen inputs to the M-Register will effectively contain one 16-bit Micro. In the case of the M-Register being designated as the sink register, the bit OR which occurs will "alter" the up-coming Micro from the ML-Register. Each of the three sources of Micros; ML, URD, and MEX are explained separately: Each requires M←ML+UFO true to D-Set Mode the M-Register.

ML-REGISTER (MLR)

The ML-Register (Micro Latch Register) consists of eight Quad Latches (LFAN) which together make up one 32-bit register. The 32-bit ML-Register is functionally divided into two portions as illustrated in Figure II-89. The function of the ML-Register is to temporarily store the next Micro, read from S-Memory, which is to be gated to and executed in the M-Register. When an MFETCH occurs (fetch the next Micro from S-Memory), only the Word address in the Memory Address Register MAR(A) is sent to S-Memory. (MAR address is not modified on MFETCH). Two Micros will be read from S-Memory when each MFETCH occurs as an S-Memory read cycle will read 32-bits of information.

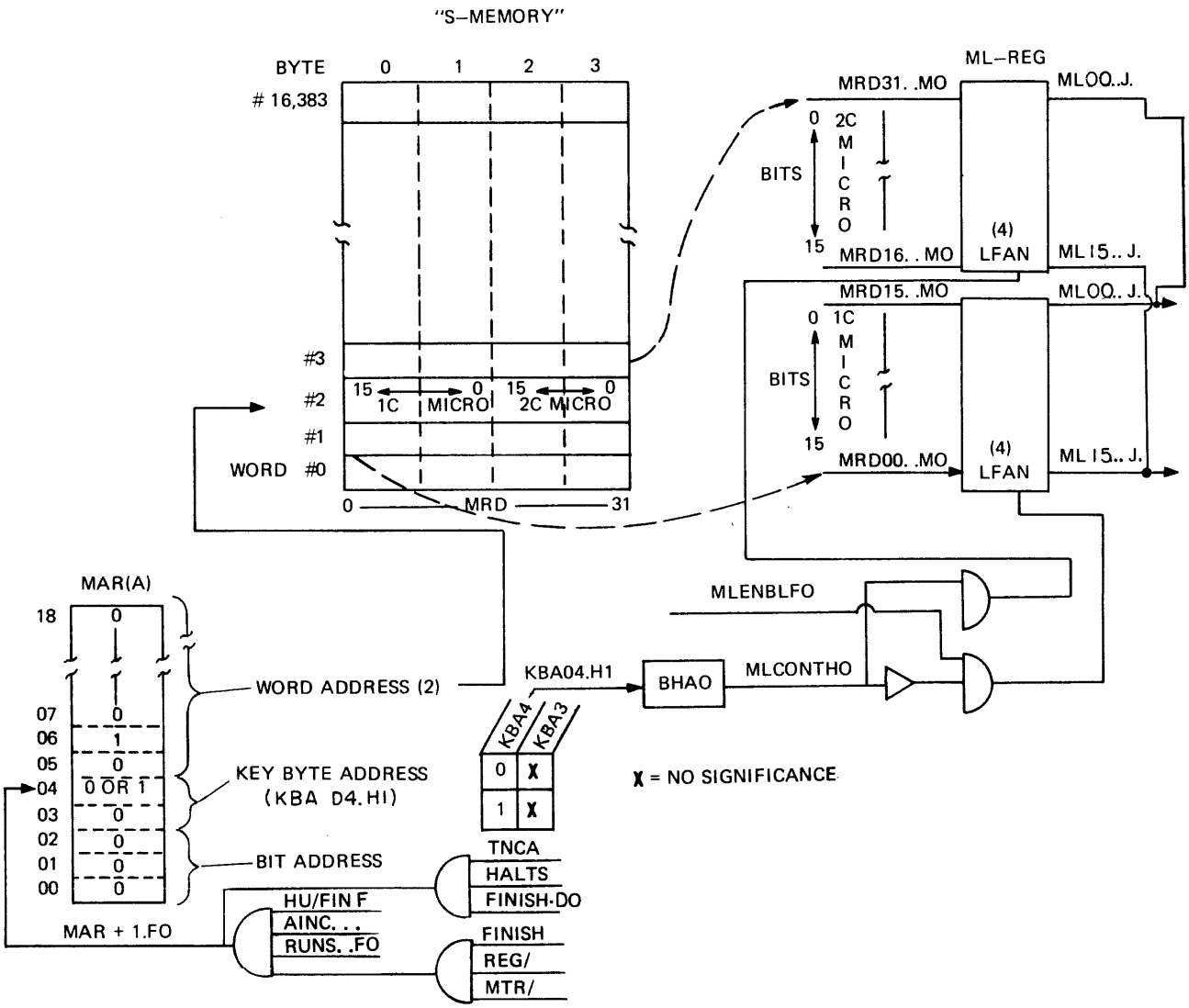
The Control Logic which produces either MLENG2J. or MLENG1J. will determine which of the two Micros read from S-Memory, and stored in the ML-Register will be gated to the M-Register to be executed. Figure II-91, illustrates an example of reading two Micros from S-Memory during a MFETCH operation. Note that the contents of the ML-Register is not changed when a Refresh Memory Cycle occurs.

During a MFETCH operation to fetch two Micros, the MAR(A) register is incremented by a binary value of 16 with a true to the carry in input to the 4-bit position of the MAR(A) register. This input is MAR+1.FO. KBA04.H1, the output of the 4-bit position of the MAR(A) register, will therefore toggle with each MFETCH operation to occur. When KBA04.H1 is false, bytes 0 and 1 which contain the 1C Micro as illustrated in Figure II-91, will be gated from the ML-Register (bits 15 thru 00) to the M-Register (Bits 00 thru 15 respectively) when MLENBLFO is true. Note the MSB of the Micro is at the ML-Register output ML00. .J. . When KBA04.H1 is true, bytes 2 and 3 which contain the 2C Micro as illustrated and will be gated from the ML-Register (bits 31 thru 16) to the M-Register (Bits 16 thru 31 respectively) when MLENBLFO is true. Again the MSB of the Micro is at the ML-Register output ML16. .J. .

The source of the information to be gated into the ML-Register is S-Memory read data (32-bits of information). This information consists "Usually" of two 16-bit Micros, one of which will be executed in the M-Register when the transfer occurs. In the case of executing the 9C Micro (move 24-bit Literal), when the 9C Micro is executed, the MFETCH operation which occurs during the time the 9C Micro is executing will fetch the 16 LSB of the 24-bit Literal. These 16 bits are fetched from S-Memory at the next memory address (byte 0 & 1 or 2 & 3 of a particular word) where the next Micro usually is located. These 16 bits of information are then gated to the Main 24-bit Exchange directly from the ML-Register. The 8 MSB of the 24-bit Literal are gated to the Main 24-bit Exchange (8MSB) from the 8 LSB of the M-Register. A 2 clock period NO OP is forced upon completion of the execution of the 9C Micro at which time an MFETCH operation occurs to fetch the next executable Micro. CLRM. .DO will force the NO OP to occur. The logic required to gate the ML-Register to the Main 24-bit Exhcnage is illustrated in Figure II-92.

U–REGISTER DATA

U-Register data is available for gating into the M-Register in the TAPE Mode only. When in the TAPE Mode and the U-Register is full, UMSB←OE. is generated for one clock period at S1 time. Refer to Cassette Logic for details. UMSB←OE. true will enable gating the LSB of the U-Register to the corresponding inputs of the M-Register. UMSB←OE. when true will also enable reading the 8 MSB of the U-Register (LFAN's). The M-Register must be in the D-Set Mode in order to set the U-Registers contents into the register. M←ML+OUO is the D-Set Mode enable for the M-Register. The logic required is illustrated in Figure II-89. Note that the Repeat Flip-Flop (REPEATF1) must be reset to general M←ML+UFO. The Repeat Flip-Flop is set when the Micro read from tape and executed in the M-Register is the 9C Micro. This disables gating the 16 LSB of the 24-Bit Literal, which is the next 16 bits read from tape, to the M-Register for execution. Instead, the 16 LSB of the Literal from the U-Register is gated to the Main 24-bit Exchange (16 LSB).



√ Fig. II-91 MFETCH "TWO MICROS"

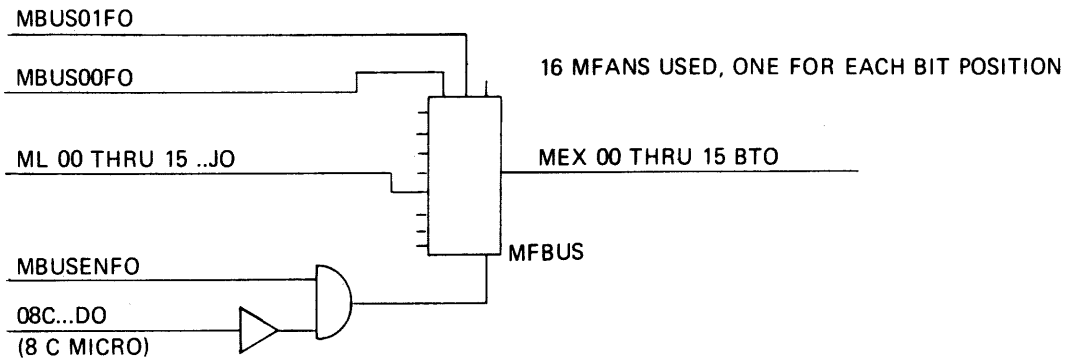


Fig. II-92 ML-REGISTER TO MEX

MAIN 24-BIT EXCHANGE DATA

The contents of the Main 24-bit Exchange is available for gating to the M-Register when MSINK.E. & M ML+UFO are true. Three Micros when executed can gate the contents of the Main 24-bit Exchange to the M-Register. The three Micros are: 2C, 1C & 10C providing the M-Register is selected as sink. Presence of any of the three Micros on the Micro Distribution Bus will when FINISHDO occurs and not in the TAPE Mode generate MSINK.FO. Gate No. 2, Figure II-89, will also be enabled at the same time thus generating M←ML+UFO. When executing any of the above three Micros, when FINISHDO occurs, MLENBLFO will also be true. With both the ML-Register's data and the data on the Main 24-bit Exchange gated to the inputs of the M-Register, the two sources of information is bit "OR-ed" into the M-Register at clock time. This effectively alters the upcoming Micro read from S-Memory and stored in the ML-Register.

CASSETTE TAPE

Don't Believe Tech Manual C.K. Handout

The Cassette is physically located on the front Console of the B 1700 Central System Cabinet. The Cassette is a read only device and is used for program loading and for storage of MTR/Diagnostic Routines which may be either executed when read from Cassette or written into S-Memory prior to execution. The physical characteristics of the Cassette are as follows:

Speed - 10 ips (Inches per second)
Density - 800 BPI (bits per inch)
Tape Length - 300 feet
Data Format - Bit Serial

TAPE FORMAT

All Micros are defined as 16 bits in length, however one complete Micro on Cassette tape consists of 40 serial bits of information.

Example: 1C Micro (Move the contents of the X-Register to the Y-Register). This Micro will appear in S-Memory or the M-Register as shown in Figure II-80.

Bit Number	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bit "format" ...	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1
Micro in "HEX"			1				0				A				1	

Fig. II-93 1C MICRO (MOVE X TO Y)

On tape, a 16-bit Micro is divided into two 8-bit characters, each 8-bit character being duplicated. Each of the four 8-bit characters is then preceded by a leading one bit and followed by an even parity bit. This makes a total of 40 bits as illustrated in Figure II-94. The exception is the 9C Micro which occupies 80 bits.

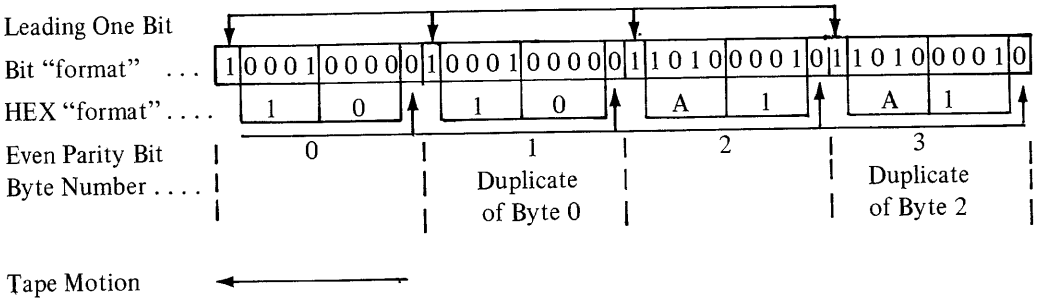


Fig. II-94 1C MICRO (MOVE X TO Y ON CASSETTE TAPE)

Each 8-bit portion of the Micro is duplicated due to parity checking logic which allows a second attempt to assemble each "half" of a Micro in the event a parity error is detected on the first attempt. This operation is explained in detail under the titles Data Transfer, Cassette to U-Register, and Parity Checking.

When data rather than a Micro is assembled on tape, the same format is used. Each 16-bits of data being divided into two 8-bit characters each of which is duplicated and each of the four 8-bit characters preceded by a leading one bit and followed by an even parity bit. Each 40 bits of serial information is assembled in the U-Register in 10-bit bytes, thus BYTE 0, 1, 2, and 3 indicate to the Cassette logic within the Processor which particular byte of information is currently being assembled. Each byte has a leading one bit, eight data bits (which may be either 8-bits of a Micro or data bits), and an even parity bit. With reference to Figure II-94, presence of a bit is indicated by a (1) and the absence of a bit is indicated by a (0) in the line across from Bit "format".

As parity for each byte (10-bits of information) is even, the parity bit can be either a (1) or (0) depending on whether the sum of the leading one bit and 8 data bits is odd or even respectively.

Each consecutive four bytes (0 thru 3) when assembled in the U-Register will equal either one 16-bit Micro or 16-bits of data. Although the leading one bit and parity bit for each byte is assembled and used in the U-Register "lower", they are not gated to any of the sink registers. Only the 16 data bits are used to represent a 16-bit Micro or 16-bits of data.

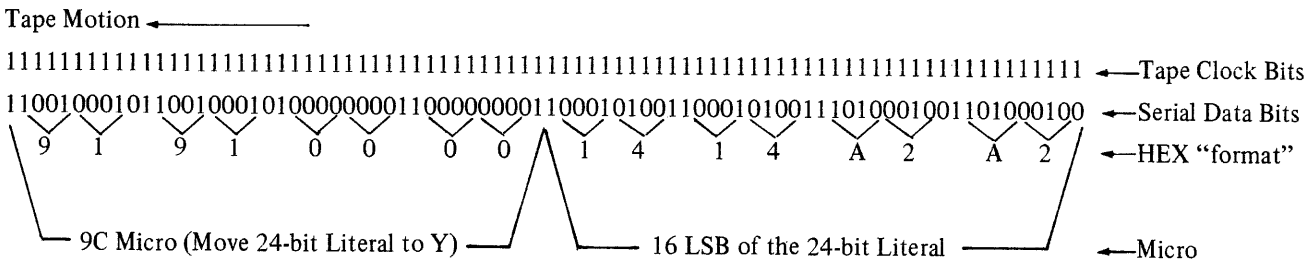


Fig. II-95 9C MICRO (MOVE 24-BIT LITERAL TO Y)

Figure II-95 illustrates the serial bit configuration of the 9C Micro on tape which effectively occupies 80 bits. The 9C Micro including the 8 MSB of the 24-bit Literal form the first 40 bits of information while the 16 LSB of the 24-bit Literal form the second 40 bits of information. In the illustration shown, the 16 LSB of the Literal is the 1C Micro (Move A-Register to T-Register). Assuming the Processor is in the TAPE Mode, the Literal portion of the 9C Micro (24 bits) will be written into the Y-Register when the Cassette tape is read. Shown also in Figure II-95 in a Tape Clock bit which is written on tape in parallel with each serial data bit position whether or not the serial data bit is a (1) or (0).

√ MODES OF OPERATION

Two modes of operation are available for Cassette Operations, each is defined as follows:

TAPE MODE

When the Micro Programed Processor is in the TAPE Mode, the basic function of the Tape Cassette is to provide a means whereby a "string" of Micros previously assemble (written) on the Cassettes Tape will be read serially from tape, assembled in the U-Register, and transferred to the M-Register for execution. Depending on the particular Micros which have been previously written on the Cassette's Tape, two basic concepts in the use of the Cassette is available. It should first be understood that the concept of operation is that every Micro which is read from tape and assembled in the U-Register is then gated to the M-Register for execution. An exception to this applies when the Micro read from tape, assembled in the U-Register and set in the M-Register for execution is the 9C Micro.

When the 9C Micro is executed, a 24-bit Literal must be available. The 16 LSB of the 24-bit Literal are in this case obtained from tape; thus the 16-bits (40 serial bits on tape) which immediately follows the 9C Micro on tape will be the 16 LSB of the 24-bit Literal. These 16-bits are not set in the M-Register and executed but are rather gated to the sink register selected in the 9C Micro. Example programs are shown which illustrate the execution of every Micro from tape (Figure II-96) and the execution of the 9C Micro from tape (Figure II-97) where the Micro following the 9C Micro on tape will be set in the sink register selected and not executed in the M-Register.

14A2	(Move A to T)	1st Micro on tape; executed.
2503	(Move TF to Pad Left)	2nd Micro on tape; executed.
13A3	(Move L to T)	3rd Micro on tape; executed.

Fig. II-96 EXAMPLE PROGRAM (EXECUTED EVERY MICRO)

Figure II-96 illustrates an example program of three Micros (shown in HEX) which then read from tape in the TAPE Mode will each be executed in the M-Register. There is no storage of any of these Micros available.

9100	(Move 24-bit Literal to Y)	1st Micro; executed.
14A2	(Move A to T)	2nd Micro; stored in Y.
7950	(Write 16-bits from Y, Count FA up 16)	3rd Micro; executed.
9100	(Move 24-bit Literal to Y)	4th Micro; executed.
2503	(Move TF to Pad Left)	5th Micro; stored in Y.
7950	(Write 16-bits from Y, Count FA up 16)	6th Micro; executed.
9100	(Move 24-bit Literal to Y)	7th Micro; executed.
13A2	(Move L to T)	8th Micro; stored in Y.
7950	(Write 16-bits from Y, Count FA up 16)	9th Micro; executed.

√ Fig. II-97 EXAMPLE PROGRAM (USING THE 9C MICRO)

Figure II-97 illustrates an example program which when read from tape and executed in the M-Register will store the same three Micros illustrated in Figure II-96 in S-Memory. The 16 LSB of the 24-bit Literal of the 9C Micro is the next Micro read from tape. These 16 bits together with the 8 MSB of the Literal which is part of the 9C Micro are set in the Y-Register. Executing the 7C Micro provides writing the contents of the Y-Register (3 Micros shown in Figure II-96) into ascending S-Memory locations for execution when the Processor is in either the Run or Step Mode. To execute the "string" of Micros which are stored in S-Memory when the program illustrated in Figure II-97 is executed the following must be true: 1. Either Run or Step Mode true. 2. The address of the 1st Micro stored in S-Memory must be in the MAR(A) Register. 3. The Start Button is depressed.

RUN MODE

When the Micro Programmed Processor is in the Run mode, Micros are "fetched" from S-Memory, temporarily stored in the ML-Register, and executed in the M-Register. When the Micro currently executing from the M-Register is the 1C Micro (Move Register to M-Register) the next upcoming Micro from S-Memory to be executed is bit OR-ed with the source registers contents thus modifying the next Micro to be executed. When the "string" of Micros executing out of S-Memory contains the 2E (Cassette Control) Micro with the variant bits set indicating "start tape", additional Micros or Data can be read from tape. Assuming the Cassette's tape has been started, executing the 1C Micro (Move U-Register to sink register) will transfer the contents of the U-Register to the sink register selected.

As a considerable length of time is required to asssemble the serial data from tape in the U-Register, the 1C Micro (Move U to Sink) is delayed from finishing until the U-Register is completely assembled (full). TAS, A, and the M-Registers are not permitted as sink registers when the U-Register is the source; thus bit OR-ed conditions explained above will not exist.

Using the U-Register as source in the Run mode therefore provides a supplement to the "string" of Micros executing out of S-Memory or it can provide a means of inputing data if so desired. An example program is shown in Figure II-98 which when executed from S-Memory will initiate the Cassette Tape (apply forward drive), and read in either Micros or data from tape, and store the same in S-Memory for latter use.

```
0000    NO OP
0020    2E Micro (Casette Control, Start Tape)
1BE0    1C Micro (Move U-Register to X-Register)
7910    7C Micro (Write 16 bits from the X-Register in S-Memory)
1BE0    1C Micro (Move U-Register to X-Register)
7910    7C Micro (Write 16 bits from the X-Register in S-Memory)
0022    2E Micro (Cassette Control, Stop at the Gap)
```

Fig. II-98 EXAMPLE PROGRAM (START AND READ CASSETTE)

Figure II-98 illustrates an example program which when executed will send forward drive to the Cassette thus causing tape to be read. It will also store the contents of the U-Register in the X-Register and write the contents of the X-Register into S-Memory. The example program will read from tape and store in S-Memory only two 16-bit Micros or two 16-bit groups of data. Executing the Cassette Control Micro (Stop at the Gap) disables the assembly of any more serial data from tape in the U-Register. Although the original "record" on tape might be considerably longer, the tape continues to move in a forward direction until the gap is sensed. The Processor will continue to "run" executing the Micro from S-Memory which follows the 2E Micro (Stop at the Gap).

√ CASSETTE DATA TRANSFER

As previously stated, serial data is read from tape and assembled in the U-Register. To completely assemble the U-Register with either a 16-bit Micro or with 16-bits of data, 40 serial data bits must be read from tape. Each serial data bit whether true or false is accompanied with a tape clock bit (always true). Each "group" of 40-bits of data is assembled in the U-Register (Lower) in four 10-bit bytes. These bytes are referred to as BITES 0 thru 3 with BITE 0 being the first 10-bit byte received and assembled in the U-Register (Lower). A particular "string" of Micros or data previously written on tape is done so in a contiguous manner such that once forward drive is applied to the Cassette and the data and tape clock bits are received within the logic of the Processor, the serial data and tape clock bits are received approximately every 125 usec.

The explanation which follows concerning Cassette Data Transfer details the operations which occur in order that serial data from the Cassette be assembled in the U-Register into one 16-bit Micro or one 16-bit byte of data. The transfer of serial data from the Cassette to the U-Register within the Processor is the same whether the mode of operation is RUN, or TAPE. It is also the same regardless of the particular bit configuration of the data which is read from tape e.g., The 1C Micro is assembled in the U-Register identically to the 9C Micro or any other Micro.

INTERFACE

Two levels interface the Cassette logic within the Processor (Card E) and the Cassette logic within the Cassette Unit. These two levels are TRIL/. . 1 and TRCP/. . 1, both are DTL and both pertain to data transfers from the Cassette to the Processor. Both levels are converted to CTL within the Processors logic on Card E as shown in Figure II-99.

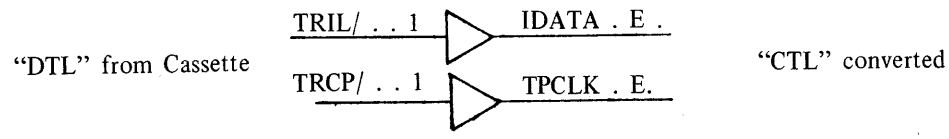


Fig. II-99 "DTL" TO "CTL" CONVERSION

Figure II-99 illustrates the CTL to DTL conversion of a serial data bit from tape (TRIL/. . 1 & IDATA. E.) and the CTL to DTL conversion of a tape clock bit from tape (TRCP/. . 1 & TPCLK. E.). Each mnemonic is defined as follows:

TRIL/. . 1 Tape Read Information Level (- volts indicates a data bit is present)
TRCP/. . 1 Tape Read Clock Pulse (- volts indicates a tape clock pulse is present)
IDATA. E. Incoming Date (+ CTL voltage indicates a data bit is present) IDATA. E. is true when either the leading one bit, a data bit present, or a parity bit present is received.
TPCLK. E. Tape Clock (+ CTL voltage indicates a tape clock pulse is present). TPCLK. E. is true for approximately 106 usec every 125 usec for the length of the serial data written on tape.

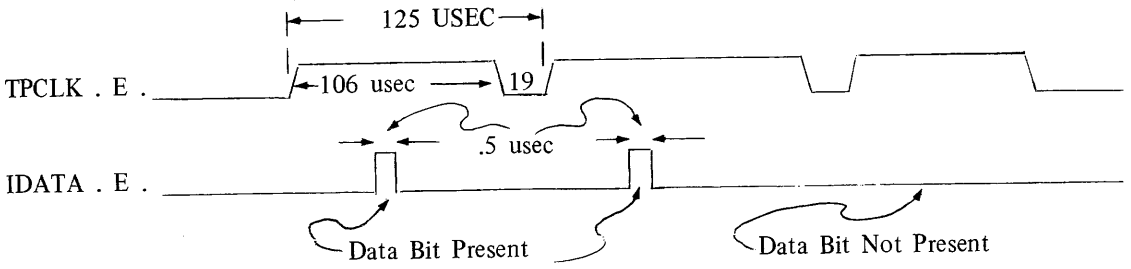


Fig. II-100 SERIAL DATA AND TAPE CLOCK TIMING

Figure II-100 illustrates the contiguous tape clock pulses (TPCLK. E.) which are received in the Processor (Card E) when forward drive is applied to the Cassette Tape, assuming that tape clock bits have previously been written on tape. The serial data bits (IDATA. E.) when true, occur approximately midway between the leading edge and trailing edge of the tape clock pulses. The tape clock pulses occur at a frequency of approximately 8KHz (once every 125 usec) and are true for approximately 106 usec. The serial data bits when present are true for approximately .5 usec.

DATA SENSING

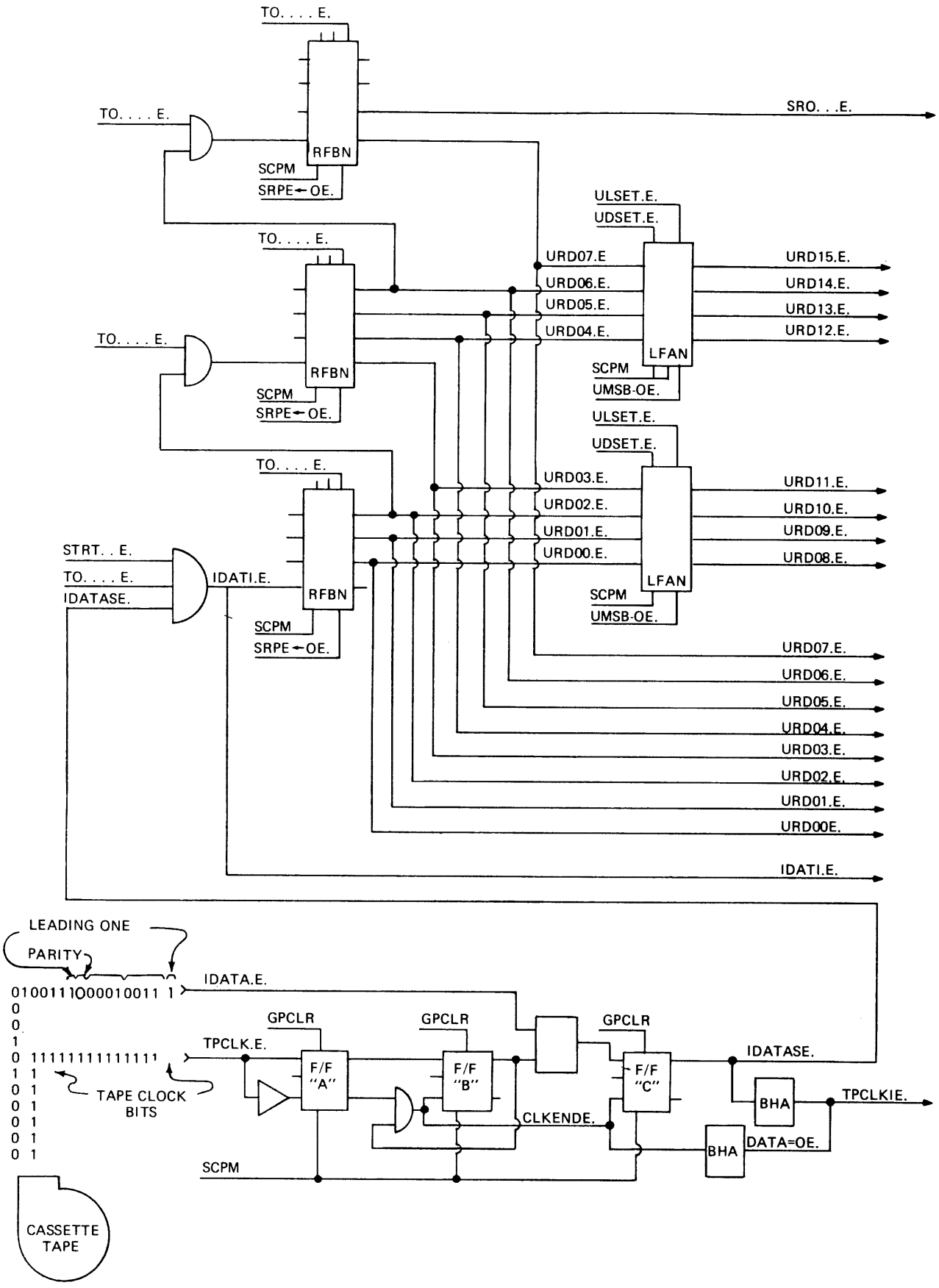
The Cassette Control logic within the Processor (Card E) provides sensing the presense of only one serial data bit (IDATA. E.) from tape during the time the tape clock (TPCLK. E.) is true. This prohibits any "noise" in addition to a serial data bit from being accepted as an additional serial data bit.

CASSETTE SERIAL DATA ASSEMBLY

Figure II-101 illustrates the logic within the Processor, Card E, which synchronizes the Tape Clock pulses received from the CAssette with the serial data bits whether present or not present. In addition the figure shows the U-Register (Lower to the left and Upper to the right) and the serial data input to the register. The three Flip-Flops (A, B, & C) function somewhat differently when a serial data bit is present than when a serial data bit is not present. For this reason a Timing Diagram illustrating each case is provided along with an explanation of the same. Regardless of whether a serial data bit is present, the output level Tape Clock IN (TPCLKIE.) is always generated for each Tape Clock pulse received from the Cassette. TPCLKIE. is used to trigger a "counter" which is used to sequence the assembly of serial data.

When a serial data bit is present, Flip-Flop C will be set thus generating both Incoming Data Stored (IDATASE.) and Tape Clock In (TPCLKIE.). When a serial data bit is not received, then only Tape Clock In (TPCLKIE.) will be true via the level DATA=OE. . The "counter" which is triggered by TPCLKIE. will generate the levels T0. . . . E., T1. . . E., T2. . . . E., and T3. . . . E. . At T0. . . . E. time, when a serial data bit is present (IDATASE. true), the serial data bit is set into the lowest bit position of the U-Register (lower) via Incoming Data In (IDATI. E.). If the serial data bit is not present (IDATASE. false) then a zero is set into the lowest bit position of U-Register (Lower). When T0. . . . E. is true, the U-Register (Lower) is the shift up mode, therefore the contents of the register before the trailing edge of the System Clock Pulse (SCPM. . E.) is shifted up one bit position when the trailing edge of the clock occurs. Assuming the first serial data bit received from the Cassette's Tape is the leading one bit, after 10 serial data bits have been received, set into, and shifted up in U-Register (Lower) with each T0. . . . B. time, the leading one bit will be at the output bit position of U-Register (Lower) called Sense Register Output (SR0. . .E.).

The serial data bits will be at the outputs of U-Register (Lower) called U-Register Data (URD 07 thru 00 .E.). The Parity Bit will be at the output bit position of U-Register (Lower) directly opposite the IDATI. E. input. With SR0. . . E. true, a byte counter's output is enabled which determined which of four bytes of information is assembled in U-Register (lower). At T1. . . . E. time, depending on the results of the Parity Checking logic which is explained separately, and the particular byte of data assembled in U-Register (Lower), a transfer of the contents of U-Register (Lower) to U-Register (Upper) can occur. At T2. . . . E. time, the Parity Checking logic is enabled, and at T3. . . . E. time, U-Register (Lower) is cleared in preparation of assembling the next 10-bits of serial data from the Cassette Tape. Due to the control of the Parity Checking logic, the count of the byte counter, and the Tn. . . .E. times which occur, the destination of the contents of U-Register (Lower) is explained under the titles; U LOWER FULL, U LOWER & UPPER FULL, and PARITY CHECK.



√ Fig. II-101 DATA TRANSFER CASSETTE TAPE TO U-REGISTER

DATA BIT PRESENT

When a serial data bit is received from the Cassette Tape, the three Flip-Flops (A, B, & C) shown in Figure II-101 function as illustrated in the Timing Diagram; Figure II-102. Assume for explanation purposes that a Tape Clock pulse (TPCLK. E.) is received from the Cassette Tape. Also received from the Cassette Tape and midway between the leading and trailing edge of the Tape Clock pulse is the leading one bit which is represented by Incoming Data (IDATA. E.). The logic shown function as follows:

1. F/F A is set with the trailing edge of the first SCPM pulse which occurs that finds TPCLK. E. true. (SCPM. . E. @ 4 MHz).
2. F/F B is set with the trailing edge of the first SCPM pulse which finds F/F A set.
3. When the serial data bit is received, IDATA. E. will be true thus causing F/F C to set with the trailing edge of the first SCPM pulse to occur. (IDATASE. and TPCLKIE. are true when F/F C is set.
4. As IDATA. E. is .5 usec in duration, the set input to F/F C is disabled when IDATA. E. goes false.
5. When the Tape Clock pulse (TPCLK. E.) goes false after 106 usec., F/F A will reset with the trailing edge of the next SCPM pulse.
6. F/F's B & C are reset with the trailing edge of the next SCPM pulse which finds F/F A reset and F/F A reset and F/F B set.

DATA BIT NOT PRESENT

When a serial data bit is not received from the Cassette Tape, the three Flip-Flops (A, B, & C) shown in Figure II-101 function as illustrated in the Timing Diagram; Figure II-103. Assume for explanation purposes that a Tape Clock pulse (TPCLK . E .) is received from Cassette Tape, and during the 106 usec. duration of the tape clock pulse no serial data bit is sensed (IDATA. E. remains false). This would indicate any of the (0) bits of IDATA. E. shown in Figure II-101. The logic shown will function as follows:

1. F/F A is set with the trailing edge of the first SCPM pulse which occurs that finds TPCLK. E. true. (SCPM. . E. @ 4 MHz.).
2. F/F B is set with the trailing edge of the first SCPM pulse which finds F/F A set.
3. As a serial data bit equal to (1) does not occur, F/F C will remain reset.
4. When the Tape Clock pulse (TPCLK. E.) goes false after 106 usec., F/F A will reset with the trailing edge of the next SCPM pulse.
5. During the time (one clock period) that F/F A is reset and F/F B is set, Data Equals Zero (DATA=0E.) is true thus TPCLKIE. is true.
6. F/F B is reset with the next SCPM pulse to occur that finds F/F A reset and F/F B set. F/F C remains reset.

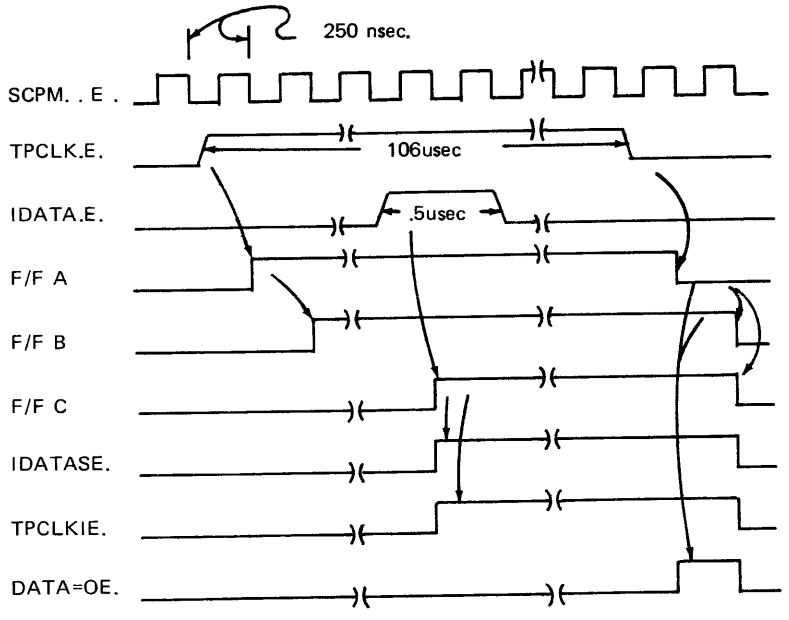


Fig. II-102 TIMING DIAGRAM SERIAL DATA BIT = (1)

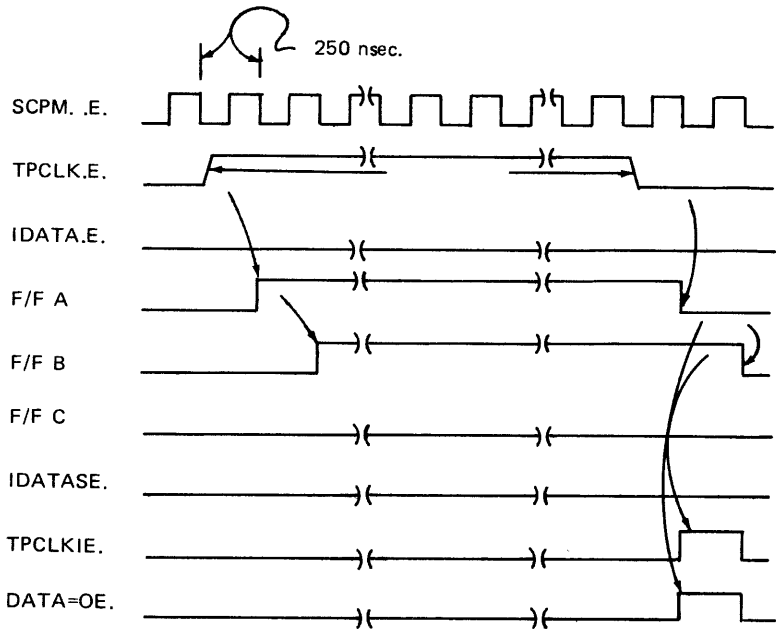


Fig. II-103 TIMING DIAGRAM SERIAL DATA BIT = (0)

CASSETTE COUNTERS

The Cassette's logic within the Processor (Card E) provides two counters which are used as follows. A "timing" counter (Tn. . . . E.) sequences the operations which occur during the synchronization of each Tape Clock pulses with the serial data bits (0 or 1), and a "byte" counter (BITEn. E.) establishes which of four 10-bit bytes of information from tape is assembled in the U-Register (Lower). Each is defined separately as follows:

Tn. . . . E. COUNTER Refer to Figure II-104

A 3-bit Register (RFAN) and a 1/8 Decoder (DFAN) are used to sequence the assembly of each serial data bit transferred from the Cassette Tape to the U-Register (Lower). The "timing" counter (Tn. . . . E.) is initially triggered with Tape Clock In (TPCLKIE.), which is either true for many clock periods (when IDATA . E. is true) or true for only one clock period (when IDATA.E . is false). Because of these two cases, two Timing Diagrams (Figure II-105 and Figure II-106) illustrate the difference when a serial data bit is either a 1 or 0 (present or not present).

The RFAN is in the D-Set Mode when the (TRUE) enable only is true. When both TRUE and X3Q. ./E. are true, the RFAN is in the Bit Set Mode. TRUE is a constant CTL true voltage level.

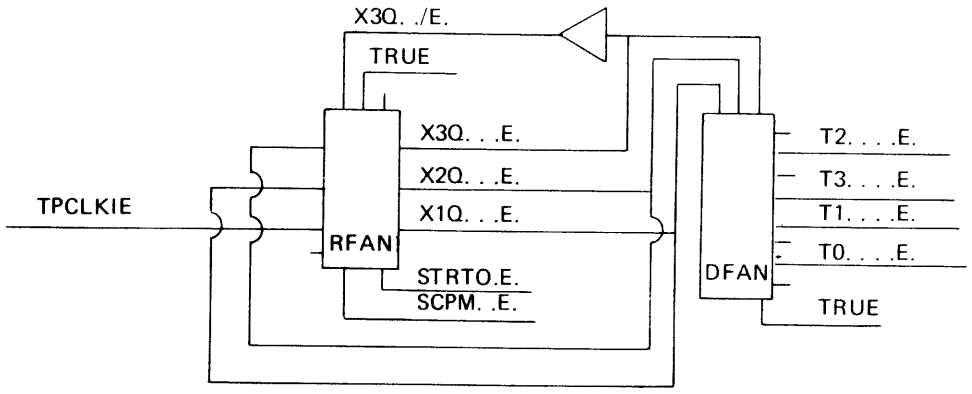


Fig. II-104 TN . . . . E . COUNTER

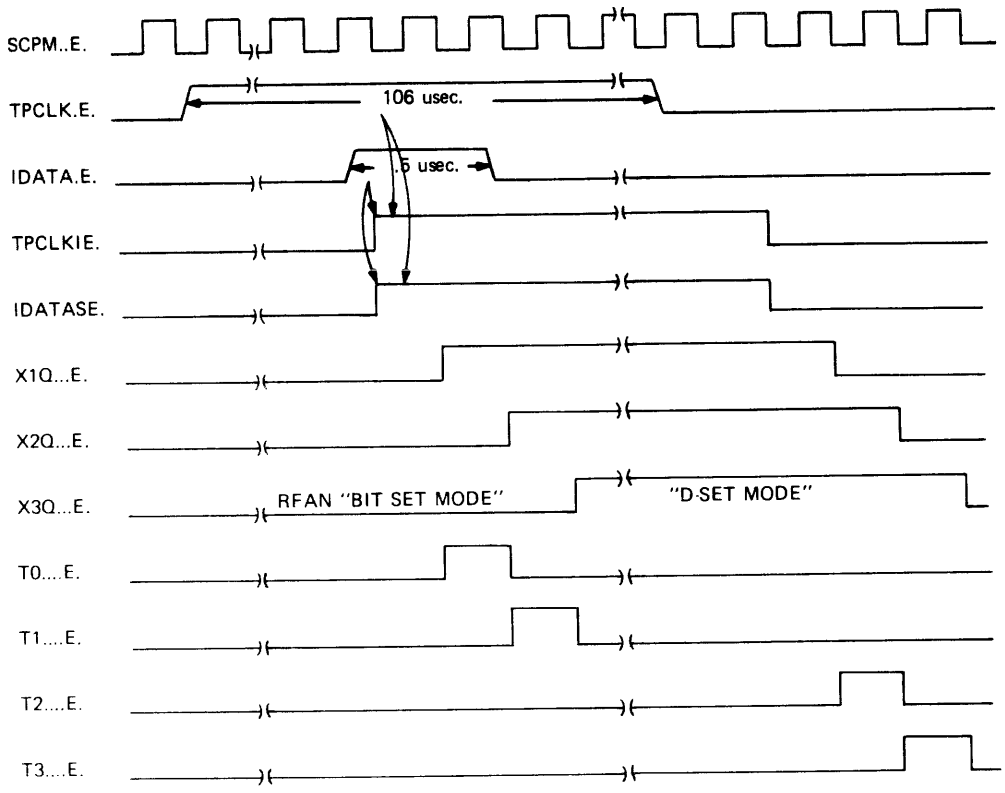


Fig. II-105 DATA BIT PRESENT TIMING DIAGRAM

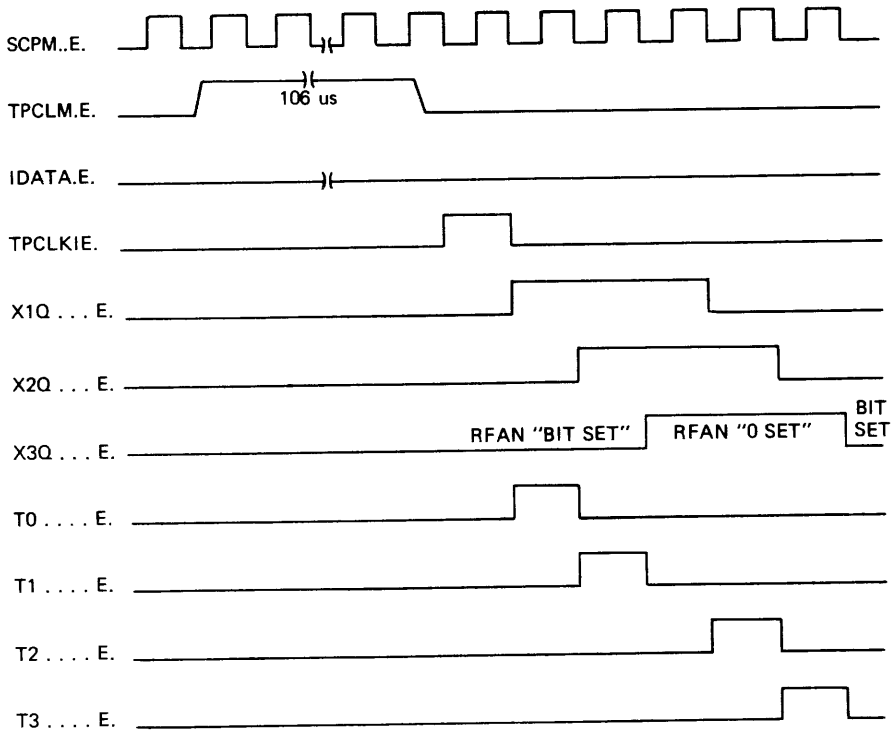


Fig. II-106 DATA BIT NOT PRESENT TIMING DIAGRAM

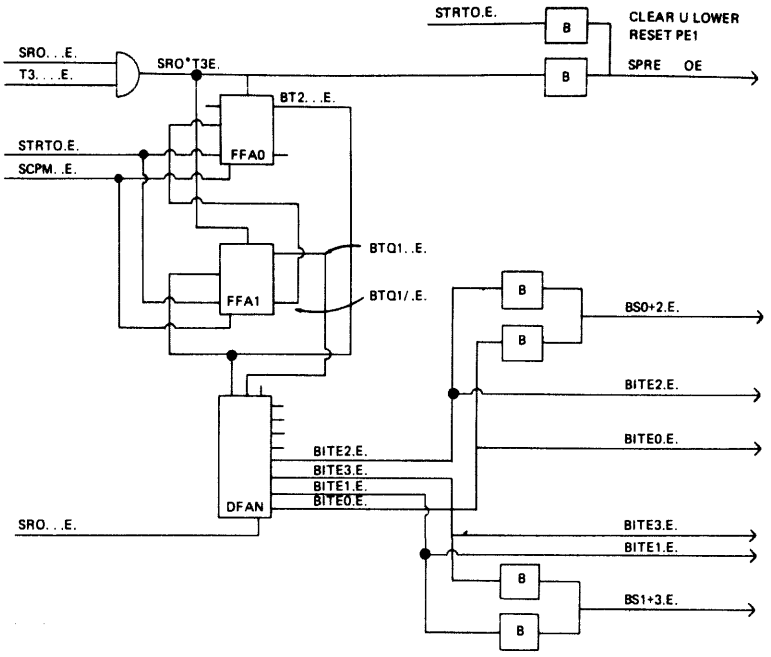
BITEn. E. COUNTER Refer to Figure II-107

Two Flip-Flops and one 1/8 Decoder (DFAN) are used to determine which of four 10-bit bytes of serial data is assembled in the U-Register (Lower). When the leading one bit of 10 serial data bits (one byte) is set in the MSB position of the U-Register (Lower) the level Sense Register Output (SRO . . . E.) is true. SRO . . . E. becomes true with the trailing edge of the SCPM pulse which finds TO time (TO . . . . E.) true, assuming 10 serial data bits from tape have been received. With SRO . . . E. true, the DFAN is enabled which reflects the status of the "byte counters" flip-flops. For explanation purposes assume forward drive has been sent to the Cassette Tape and the two flip-flops are initially reset with Start Tape Reset (STRTO .E.). With both flip-flops reset, when SRO . . . E. is true the BITEO .E. output of the DFAN will be true. BITEO .E. true indicates the first 10-bits of forty serial data bits from tape are assembled in the U-Register (Lower). During T1 time, BITEO .E. true is used to enable gating the contents of U-Register (Lower) to U-Register (Upper).

During T2 time, BS0+2.E. true is used to enable Parity Checking logic. When T3 time (T3 . . . . E.) occurs, SRO*T3E. is true which causes both flip-flops to be in the D-Set Mode. The trailing edge of the next SCPM pulse will set the BT2 . . . E. flip-flop. The same SCPM pulse will reset U-Register (Lower) with SPRE-0E. also true, therefore SRO . . . E. is no longer true and the DFAN is disabled (BITEn. E. false). The next 10-bits of serial data from tape is assembled in the U-Register (Lower) and again SRO . . . E. will be true when the leading one bit is sensed. The DFAN is again enabled, this time causing BITE1 .E. to be true.

BITE1 . E. true indicates the second 10-bits of forty serial data bits from tape are assembled in the U-Register (Lower). During T1 time, BITE1 . E. true is used to enable gating the contents of U-Register (Lower) to U-Register (Upper) if a parity error was detected on the first 10-bits assembled in the U-Register and there are no errors on these 10-bits. If the first 10-bits assembled had good parity, then the second 10-bits are not used. During T2 time, BS1+3 . E. true is used to enable Parity Checking logic. When T3 time occurs, the two flip-flops are again in the D-Set Mode.

The trailing edge of the next SCPM pulse will set the BTQ1 . . E. flip-flop. BTQ2 . . E. remains set. The same SCPM pulse will reset U-Register (Lower) with SPRE-0E. also true, therefore SRO . . . E. is no longer true and the DFAN is disabled (BITE1 . E. false). This pattern repeats for the third and fourth 10-bit bytes of serial data assembled in the U-Register (Lower). BS0+2 . E. and BS1 . 3 . E. are used to determine whether the 10-bits of serial data assembled in U-Register contains the first or duplicate 8-bits of data which is written on tape. This information is used in the Parity Checking logic explained separately. The BITEn . E . Counter Timing shown in Figure II-108 illustrates the assembly of 40 serial data bits from tape. Note that the outputs of the DFAN (BITEn . . E.) are true only during T1 thru T3 time when the leading one bit is sensed in the U-Register (Lower), indicated when SRO . . . E. is ture.



√ Fig. II-107 BITEn . E . COUNTER

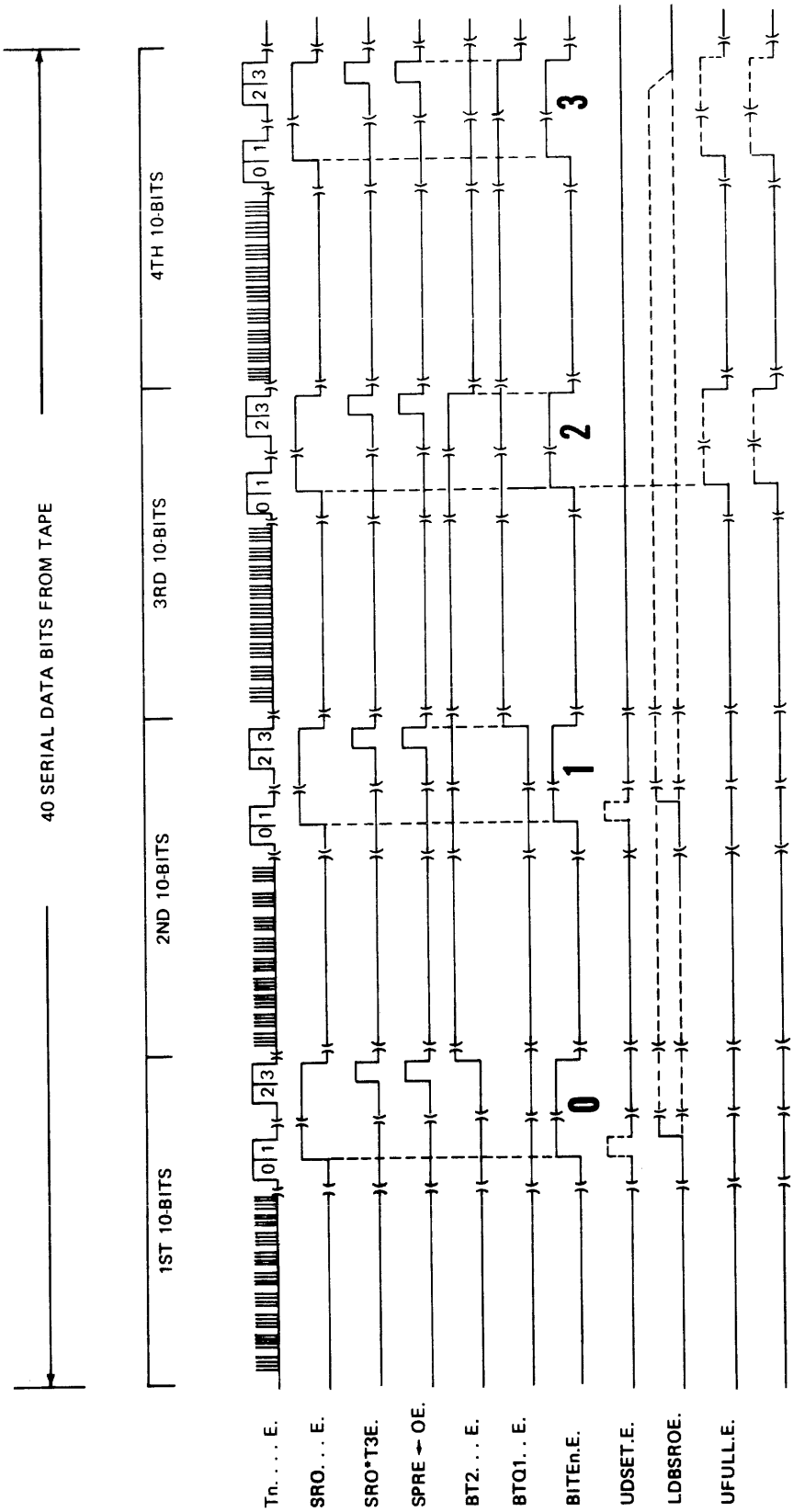


Fig. II-108 BITEn . E . COUNTER TIMING

CASSETTE DATA AVAILABLE Refer to Figure II-109

Serial data from the Cassette Tape is available as source when UMSB ← 0E. and UFULL .E0 are true. The logic shown in Figure II-109 is used to determine when the U-Register is "FULL". The logic uses the BITEn . E. Counter, Tn . . . E. Counter, Parity Checking logic (PEn . . . E. levels), FINISHDO, and various other Cassette logic levels to determine when the U-Register is assembled with 16-bits of information (either data or a micro). The U-Register is referred to as U-Lower (bits 00 thru 07) and U-Upper (bits 08 thru 15). The serial data from tape is first assembled in U-Lower. The data assembled in U-Lower will consists of 10-bits of information from tape. The 10-bits consisting of (1) leading one bit, (8) data bits, and (1) parity bit. Depending on which of four 10-bit bytes of information from tape is assembled in U-Lower and the results of the parity checking logic, the (8) data bits are either gated to the U-Upper portion of the U-Register, cleared in U-Lower and not used, or are made available for gating to either the M-Register or the Main 24-bit Exchange.

U-LOWER FULL Refer to Figure II-109

Assume for explanation purposes, that a Cassette operation has been initiated. The level STRTO . E. will be true until the tape clock pulses are received from the Cassette Tape. STRTO . E. true provides initially resetting flip-flop "A" shown in Figure II-109. In addition the level provides resetting the BITEn . E. Counter, Tn . . . E. Counter, Parity Checking logic, and the U-Register (Upper and Lower). When the 1st leading one bit of 10 serial data bits from tape is sensed at the SRO . . . E. output position of U-Lower, flip-flop "A" will have a true to the D1 input.

With reference to Figure II-108 which illustrates the BITEn . E. Counter Timing, when SRO . . . E. is true, BITEO . E. is also true. At T1 . . . . E. time, providing no parity error is detected on the 10 serial data bits received (PE1/ . . . E. true), gate No. 1 Figure II-109 will output a true thus generating UDSET . E. during T1 time. With UDSET . E. true, flip-flop "A" is in the D-Set Mode and will set with the trailing edge of the next SCPM . . E. pulse. The set output of flip-flop "A" (LDBSROE .) when true indicates the leading byte of serial data from tape (either BITEO . E. or BITE1 . E.) has been assembled without parity error in U-Lower and transferred in parallel to U-Upper. Note that UDSET . E. true also develops ULSET . E. and together they cause the U-Upper portion of the U-Register to be in the D-Set Mode (Refer to Figure II-101).

If a parity error is detected on the first 10 serial data bits from tape assembled in U-Lower then gate No. 1, Figure II-109 will not output a true at T1 time. When the second 10 serial data bits from tape are assembled in U-Lower BITE1 . E. and SR0 . . . E. will be true. Gate No. 2 will output a true at T1 . . . . E. time providing an error was detected on the first 10 serial data bits (PE2 . . . E. true) and an error is not detected on the second 10 serial data bits (PE1/ . . E. true). Gates No. 1 and 2 therefore control setting flip-flop "A" which develops LDBSROE. when either the first or second 10-bit byte of serial data is assembled and transferred to U-Upper without parity error.

If neither byte is assembled without parity error, U-Lower is not transferred to U-Upper and further assembly of data in U-Lower is disabled via the parity checking logic explained separately. Note that regardless of whether U-Lower is transferred to U-Upper or not used, the U-Lower portion is cleared before the next byte is assembled. Clearing occurs at T3 time and transfers to U-Upper occur at T1 time.

U-LOWER & U-UPPER FULL Refer to Figure II-109

Assume for explanation purposes that the first and second 10-bit bytes of serial data from tape have been assembled in U-Lower and that one of the two bytes was assembled without parity error. Assume also that one of these two bytes (8-bit data portion) was transferred in parallel to U-Upper with UDSET . E. true. The set output of flip-flop "A" (LDBSROE.) is true and STP/ . . . E. is true. STP/ . . E. becomes true when a Cassette operation is first initiated and remains true until a stop at the gap condition exists. When the third 10-bit byte of serial data is assembled in U-Lower and the leading one bit is sensed at the SRO . . . E. output position of U-Lower, BITE2 . E. will be true. Providing this byte of serial data from tape is assembled in U-Lower without parity error (PE1/ . . E. true), gates No. 4 & 5 will output a true. The level UFULL . E. will be true thus enabling setting flip-flop "B" when the next FINISHDO occurs. If a parity error is detected on the third 10-bit byte of serial data assembled in U-Lower then gates No. 4 & 5 will not output trues thus flip-flop "B" will not be set when the next FINISHDO occurs. In this case when the fourth 10-bite byte of serial data is assembled in U-Lower, BITE3 . E. will be true. Providing this byte is assembled without error (PE/ . . E. true), gate No. 4 & 6 will output trues thus generating UFULL . E. which will enable setting flip-flop "B" when the next FINISHDO occurs. Note that PE2 . . . E. will be true if a parity error is detected on the third 10-bit byte of serial data from tape. Gates 5 & 6 therefore control setting flip-flop "B" when either the third or fourth 10-bit byte of serial data from tape is assembled in U-Lower without parity error. Figure II-108 illustrates the BITEn . E. Counter Timing and the occurence of UFULL . E. when either BITE2 . E. or BITE3 . E. is true.

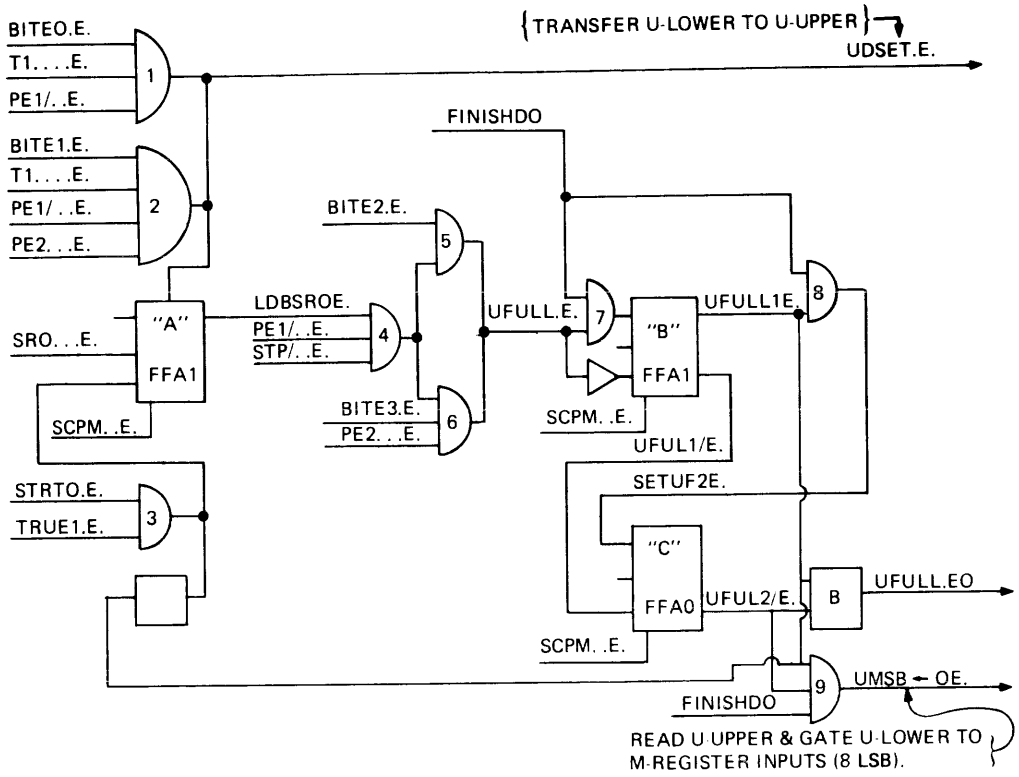


Fig. II-109 U-REGISTER "FULL" LOGIC

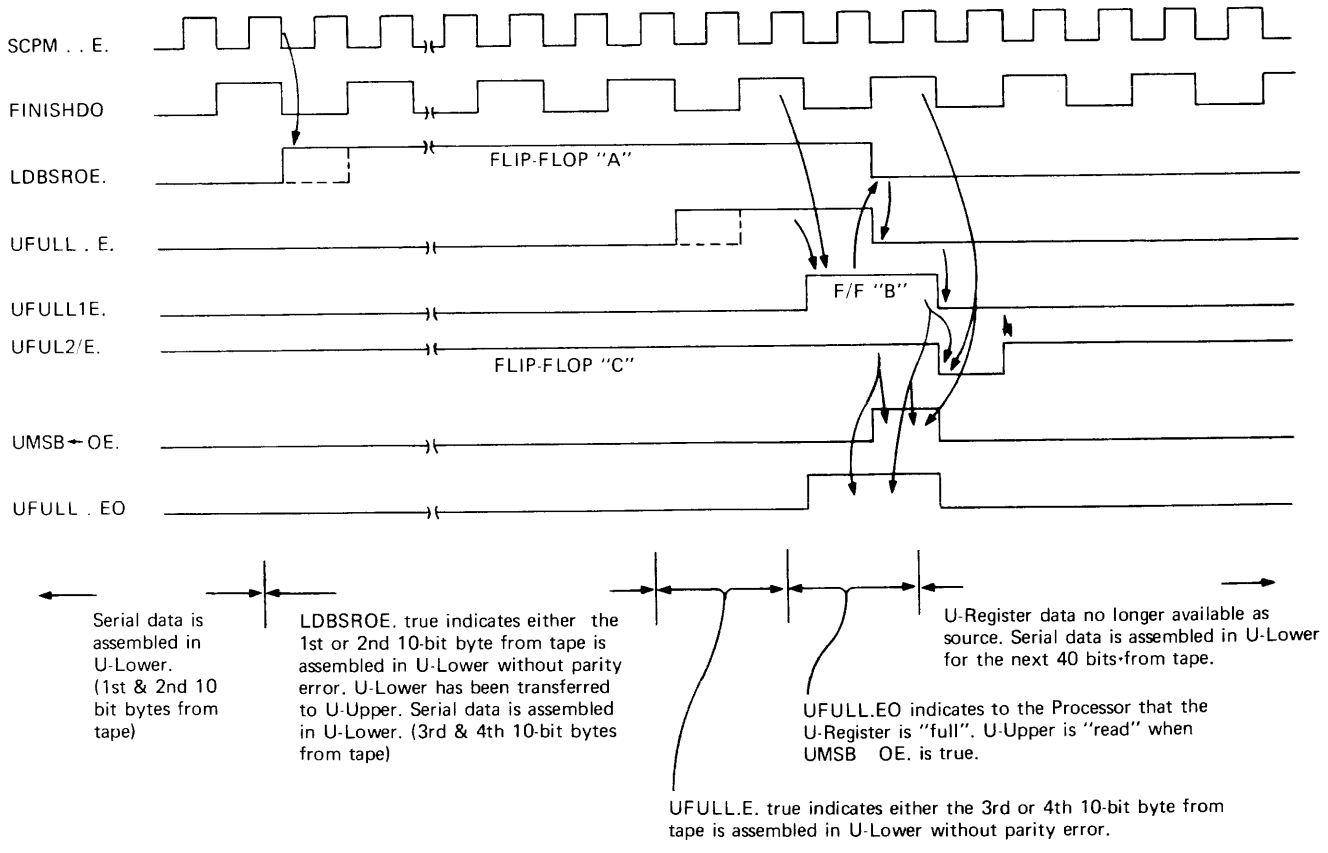


Fig. II-110 UFULL . EO TIMING AND Fig. II-111

UFULL . E0 TIMING Refer to Figures II-109 & II-110

Figure II-109 illustrates the logic used to synchronize the gating of the contents of the U-Register to either the M-Register or the Main 24-bit Exchange with the FINISHDO level. This is necessary as the assembly of the serial data from tape is not synchronous with the execution of Micros in the M-Register. Figure II-110, UFULL . E0 TIMING, illustrates the two clock period generation of UFULL . E0 and the one clock period generation of UMSB-0E. Both LDBSROE. and UFULL . E. are shown with "dotted lines" which is to indicate that they occur during the trailing edge of SCPM . . E. and not with any relationship to FINISHDO.

PARITY CHECK

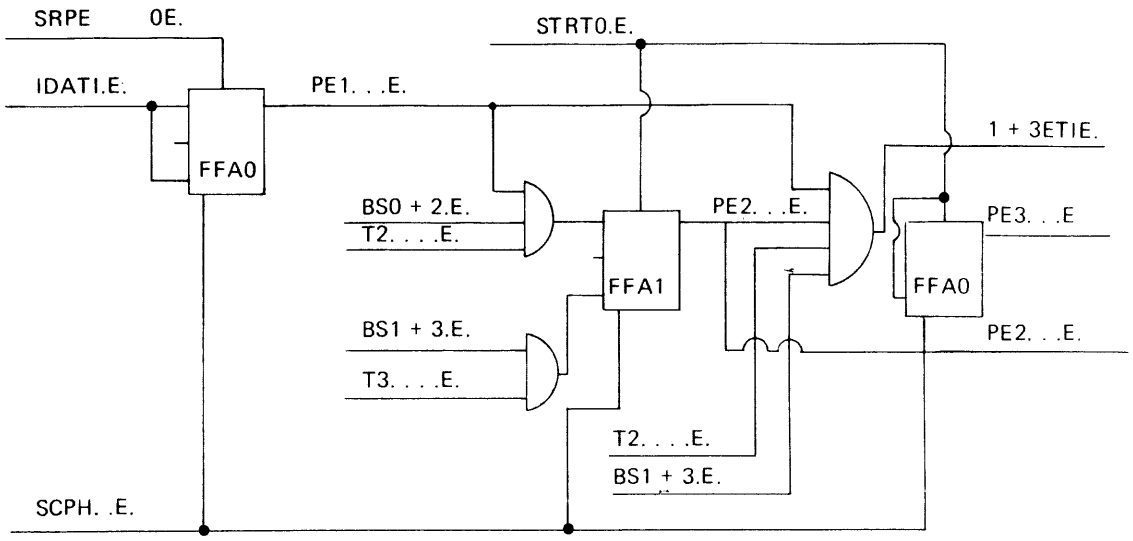
Each half (eight bits of sixteen bits) of either a Micro or data previously written on Cassette Tape is duplicated for the purpose of providing a second attempt to read eight bits with correct parity in the event a parity error is detected on the first eight bits of the Micro or data read from tape.

FUNCTIONAL DETAIL

Three Parity Checking Flip-Flops are used to determine if a correct read of eight bits of either a Micro or data has occurred. The three flip-flops are shown in Figure II-112, Parity Check Logic. Assuming the three flip-flops are initially reset they function as follows:

Each of the 10-bits of each byte of information read from tape which is true will cause the PE1 . . . E. flip-flop to toggle. IDATI . E. is true when a "data bit", either a leading one, a data bit, or the parity bit is true. As even parity is used, the PE1 . . . E. flip-flop is reset after 10 bits of information has been read from tape and assembled in U Lower providing there is not a parity error on the 10 bits assembled in U Lower. Assuming the first 10 of 40 bits is assembled in U Lower with no errors, PE1 . . . E. will be false.

At T1 time with BITE0 . E . true, USET . E. is true and a transfer in paralle to U Upper of the first eight data bits occurs. If an error is detected on the first 10 bits assembled in U-Lower than PE1 . . . E. is set. At T2 time and BSO+2 . E. true the PE2 . . . E. flip-flop is set to "remember" a parity error did occur on the first 10-bits of information read from tape. (Byte 0). The second 10 bits of information (Byte 1) is read from tape and again at T2 time the PE1 . . . E. flip-flop is checked to determine if an error has occured on the second 10 bits of information only when PE2 . . .E. is set. If PE2 . . . E. is reset, the second 10 bits (Byte 1) of information read from tape is cleared from U Lower and not used. If PE2 . . . E. is set then the PE1 . . . E. flip-flop is checked at T2 time when BS1+3 . E. will be true. If an error has occurred on Byte 1 as well as on Byte), then PE3 . . . E0 is set. The same clock pulse that set PE3 . . . E0 will also set the Stop Flip-Flop causing STP/11E. to be false. With STP/ . . E. false, all further data inputs to U Lower from tape are disabled, refer to Figure II-112. With PE3 . . .E0 true, when the next FINISHDO occurs and providing certain control terms (JUMP/ . F. & REPEA/F .) are true, the Processor's RUN Flip-Flop (RUNS . . F0) is reset causing HALTS . . F . to be true. Effectively the Processor is halted. If an error is not detected on the second 10 bits (Byte 1) then UDSET . E. will be true, and the



√ Fig. II-112 PARITY CHECK LOGIC

second 10 bits of information is transferred in parallel to U Upper. Providing either Byte 0 or 1 is read correctly Bytes 2 and 3 will be read and checked for correct parity as were Bytes 0 and 1. Note that either Byte 0 or 1 is gated to U Upper and that either Byte 2 or 3 is used as the eight LSB of either the Micro or data read from tape. The particular mode of operation (RUN or MTR) and the particular Micro in the M-Register (if any) will determine where teh 16 bits (either a Micro or data) in the 16 bits of the U-Register will be gated.

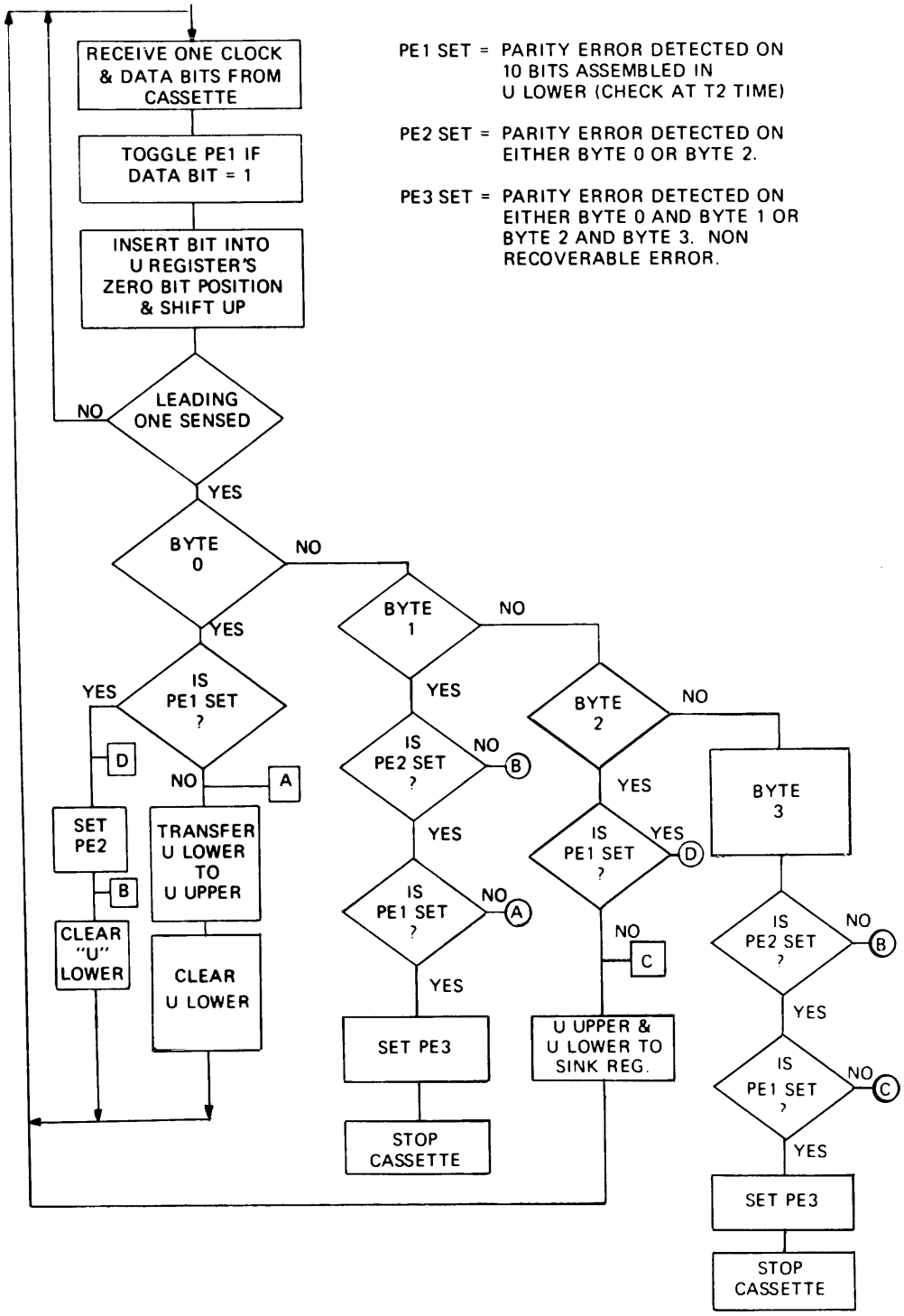


Fig. II-113 PARITY CHECK FLOW

PARITY CHECK FLOW

The sequence of events that takes place during a tape read operation are shown in Figure II-113.

DATA TRANSFER (U-REGISTER TO M-REGISTER, U-REGISTER TO MEX)

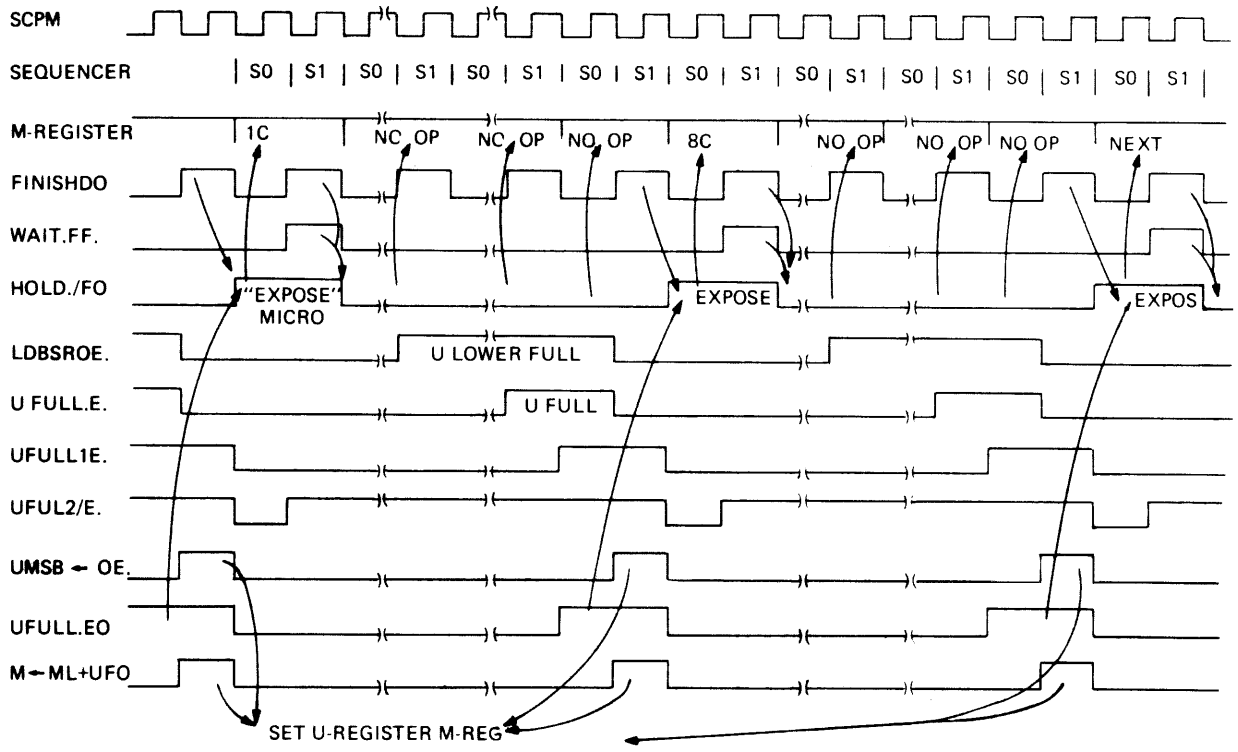
Depending on the running mode of the Processor (RUN or TAPE) and depending on the particular Micro current executing (if any other than a NO OP), a transfer of the contents of the U-Register (16-bits) to the M-Register (16 bits) can occur.

MTR MODE

Assuming a Tape Cassette is present and ready, depressing the Start Button on the console will cause forward drive to be applied to the cassette. The "string" of Micros previously written on tape are read serially from tape, assembled in the U-Register and gated then to the M-Register for execution. Upon completion of executing each Micro read from tape the logic provides the "wait" capability for the U-Register to again assemble the next Micro read from tape. During this wait period the NO OP Micro will be executed many times as the M-Registers contents will not be gated to the Micro Distribution Bus for decoding and execution.

When in the TAPE mode, all Micros executed are effectively those from tape, Micros that provide Skip or Branch features are not permitted. Note that Micros with this feature may alter the Memory Address Register (MAR(A)) which does not pertain to the operation of the Processor when in the TAPE Mode, except when the 7C Micro is read from tape and executed. This use of the MAR(A) register doesn't relate to the alteration of MAR(A) which might be the result of a Skip or Branch type Micro and is therefore not considered.

When the Micro read from tape is the 9C Micro (Move 24-bit Literal) the 16 LSB of the literal will be the next Micro read from tape and assembled in the U-Register. In this particular case, the U-Registers contents is not gated to the M-Register and executed but is gated to the Main 24-Bit Exchange and to the Sink Register selected. When the U-Register is "Full" (16-bits assembled) two significant terms are developed. UFULL . E0 will be true for two clock periods (4 MHz) and UMSB←0E. will be true for one clock period. The generation of these levels is shown in Figure II-108 UFULL Logic. UFULL . E0 and the 9C Micro in the M-Register and exposed to the Distribution Bus provides for gating the U-Register to the Main 24-bit Exchange. UMSB←0E. gates the U-Register data (bits 00 through 07) to the inputs of the M-Register. UMSB 0E. also enables reading the U-Register bits 15 through 08 which are contained in Quad Latches (LFAN's). Data Transfer, Cassette to U-Register Upper's enable (UMSB←0E.). See Figure II-89



√ Fig. II-114 TAPE MODE AND EXECUTE EACH MICRO

The ML & M-Register explanation illustrates the enabling of gating U-Register bits 07 through 00 to the M-Register. Note that although UMSB←0E. will gate the contents of the U-Register to the input of the M-Register, a control level (M←ML+UFO) must be true to cause the M-Register to be in the D-Set Mode. The logic required to cause M←ML+UFO to be true is shown in Figure II-89, ML & M-Registers. The level REPEA/F. into gate 1 Figure II-89, is a control level used to enable gate 1 when in the TAPE Mode. The level is "normally" true, however, when in the TAPE Mode and the 9C Micro is in the M-Register and exposed when REPEA/F. if false which provides disabling the gating of the LSB (U-Register) of the 24-bit Literal to the M-Register.

FUNCTIONAL DETAIL, 1C and 8C MICRO

The Timing Diagram, Figure II-114, 1C and 8C Micro, illustrates the sequence of events which occur when the Processor is in the TAPE Mode. Shown is the execution of two Micros from tape (LC & 8C Micro). Two control flip-flops (HOLD ./F0 & REPEATF1) are used to control TAPE Mode operations. Assuming the 1C Micro was previously read from tape, assembled in the U-Register and gated to the M-Register for execution, the operation is as follows: With HOLD ./F0 true, the 1C Micro assumed to be in the M-Register is exposed to the Micro Distribution Bus, decoded and executed. Assuming a 2 clock period 1C Micro (Move Register to Register . . . not BCD), when FINISHDO occurs the execution of the 1C Micro is complete. When FINISHDO occurs, the control logic generates the level WAIT . FF . which will set the HOLD . /F0 flip-flop (HOLD . /F0 is the reset output). With HOLD . /F0 false, the contents of the M-Register is not "exposed" to the Micro Distribution Bus; therefore a NO OP is executed until HOLD . /F0 goes true. When UFULL . E0 is true and FINISHDO is true, the HOLD . /F0 flip-flop is reset causing HOLD . /F0 to be true. The same clock pulse that resets the flip-flop also sets the contents of the U-Register into the M-Register as both UMSB←0E. & M←ML+OF0 are true. Assuming the 8C Micro is the next Micro from tape, it is now executed in the M-Register. The operation repeats for the assembling of the next Micro which follows the 8C Micro.

FUNCTIONAL DETAIL, 7C AND 9C MICROS

The Timing Diagram, Figure II-115 illustrates the sequence of events which occur in the TAPE Mode when the 9C Micro is read from tape. As previously mentioned, the 9C & 7C Micro's provide a menas of storing Micro's read from tape into S-Memory for execution in the RUN Mode. Assuming the 9C Micro is read from tape, assembled in the U-Register and gated to the M-Register and executed, the operation is as follows:

The 9C Micro, exposed and executed generates at S0 time the level WAIT . . F. which sets the REPEATF1 & HOLD . /F0 flip-flops. The 9C Micro is therefore exposed initially for only one clock period; however, the 9C Micro will remain in the M-Register until the next 16-bits of information from tape is assembled in the U-Register. When UFULL . E0 occurs and with the REPEATF1 flip-flop set, the reset output of the HOLD . /F0 flip-flop (HOLD . /F0) is held true; thus exposing the 9C Micro to the Micro distribution Bus again. The 16LSB of the Literal are now in the U-Register and are gated to the 16 LSB of the Main 24-bit Exchange. The 8 MSB of the literal are the 8 LSB of the 9C Micro in the M-Register; they too are also gated to the 8 MSB of the Main 24-bit Exchange. The 24-bit Literal on the Main 24-bit Exchange is then set into the sink register selected. CLRM . . D0 is true when the 9C Micro is exposed and FINISHDO is true; therefore, the 9C Micro is cleared from the M-Reg, effectively executing a NO OP until the U-Register is again full and transferred to the M-Register for execution. Assuming the next Micro read from tape is the 7C Micro, the 16 LSB of the 24-bit Literal previously stored in a sink register during the execution of the 9C Micro can then be written into S-Memory. The Sequencer will generate S0 through S7 times for the execution of the 7C Micro. Refer to the explanation of the 7C Micro for details. Upon completion of the execution of the 7C Micro, NO OP's will be executed until the U-Register is again full.

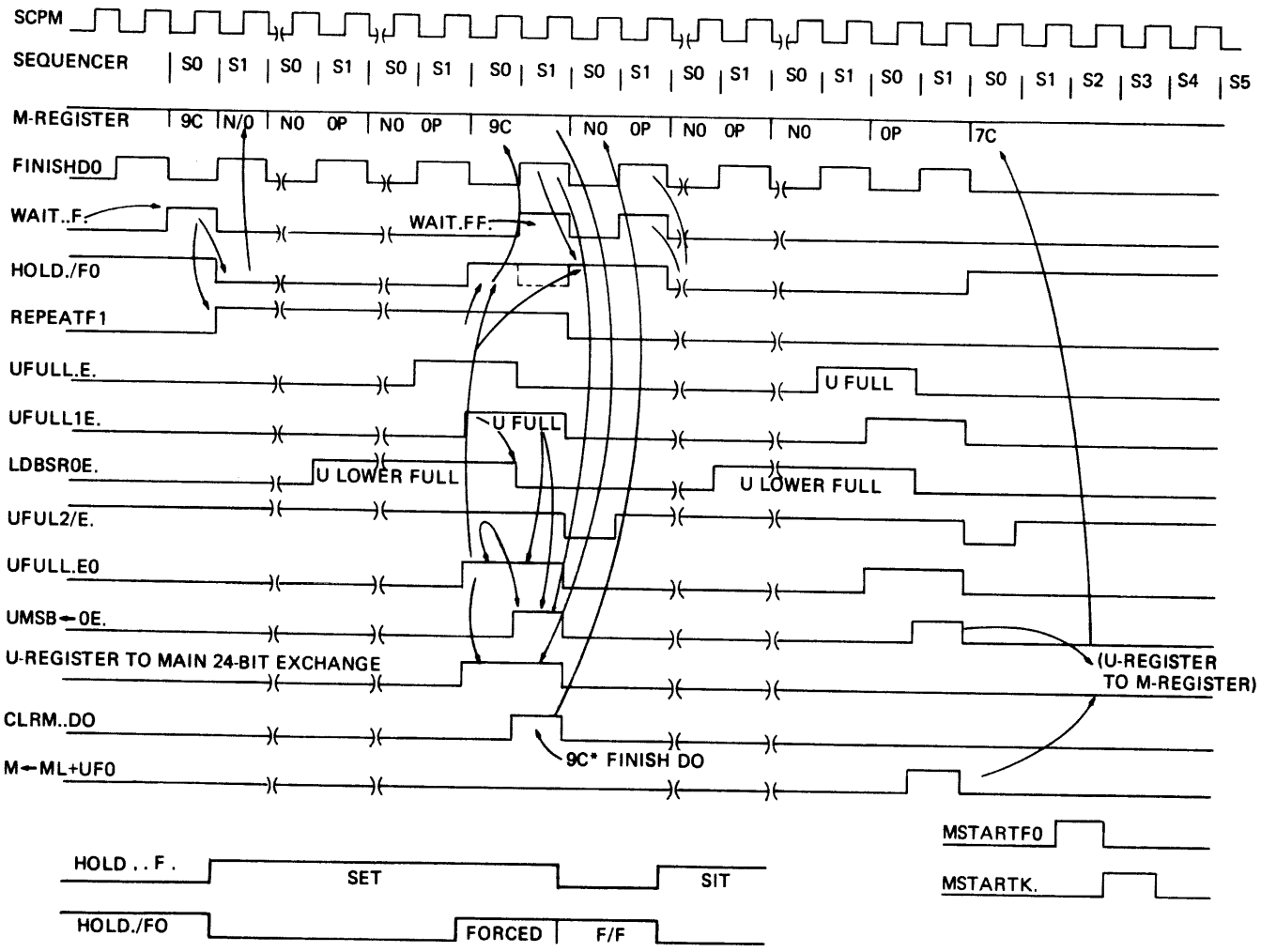
RUN MODE

When the Processor is in the RUN Mode, Micros are executed in the M-Register which are "fetched" from S-Memory during concurrent MFETCH operations which is explained separately.

Three Micros are available for execution (from the S-Memory string of Micro's currently executing) which have significance with Cassette operations. These three Micros are: 2E Cassette Control, 1C (Move U to Sink), and the 2C (Move U to Scratch Pad) Micro's. When in the RUN Mode, the M-Register is not permissable as a sink register when the U-Register is source; therefore, bit "ORE" functions with the U-Register's information is not allowed.

All data transfers from the serial data read from tape, assembled in the U-Register are via the Main 24-bit Exchange to the sink register selected. This illustrates the sequence of events which occur when in the RUN Mode and the Cassette is initiated with the execution of the 2E Micro (Cassette Control . . . Start Tape).

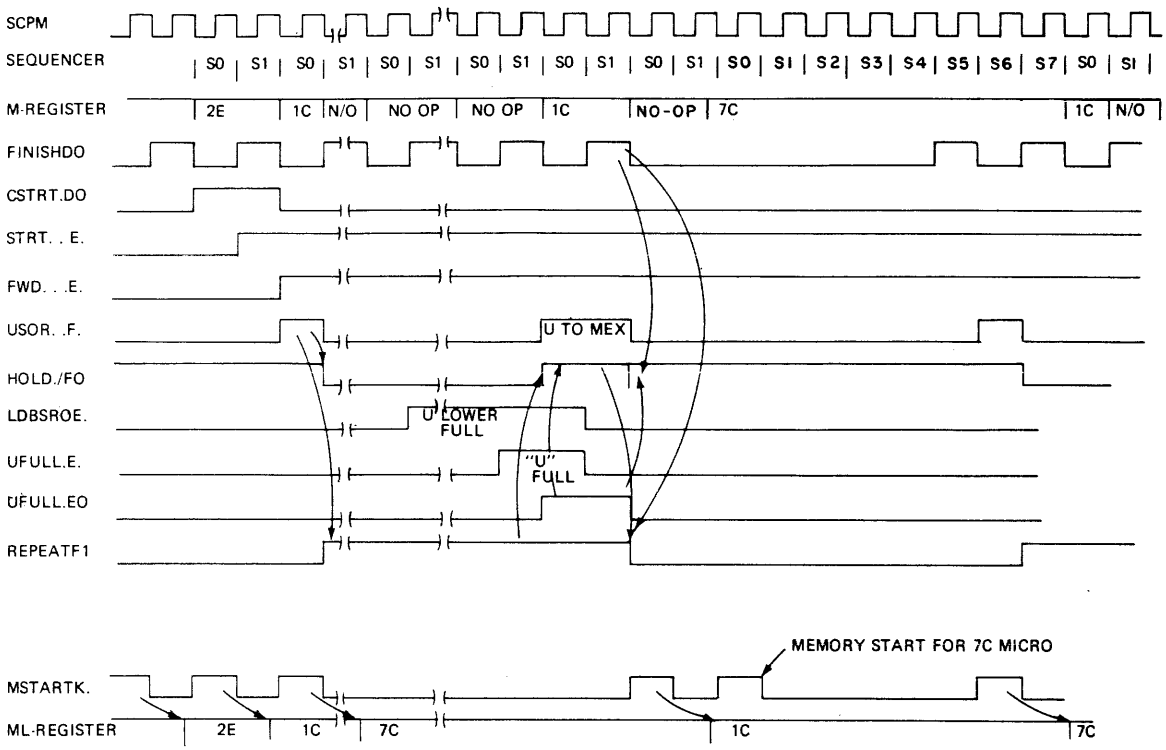
Note that each Micro executed in the M-Register has been fetched from S-Memory and not from tape. Assuming the 2E Micro (Cassette Control . . . Start Tape) is executed, forward drive will be applied to the Cassette and the Micros or



√ Fig. II-115 TAPE MODE AND STORE IN S-MEMORY

data previously written on tape are read and assembled in the U-Register. The next Micro fetched from S-Memory during the concurrent MFETCH operation which occcurs during the execution of the 2E Micro to be the 1C Micro (Move U to a Sink Register) as illustrated in Figure II-116. When the 1C Micro is exposed to the Micro Distribution Bus and decoded, the level USOR . . F is generated. USOR . . F. and S0 time will cause the HOLD . /F0 flip-flop to be set with the next clock pulse thus causing HOLD . /F0 to be false. With HOLD . /F0 false, the 1C Micro is exposed for one clock period and followed by a one clock period NO-OP. USOR . . F. true also causes the REPEATF1 flip-flop to be set. Serial data is received from tape and assembled in the U-Reg. When UFULL . E0 occurs and the REPEATF1 flip-flop is set, the output of the HOLD . /F0 flip-flop is held true, thus HOLD./F0 is true. With HOLD . /F0 true, the 1C Micro is again exposed to the Micro Distribution Bus and executed. The contents of the U-Register is then gated to the Main 24-bit Exchange and set in the Sink Register selected. UFULL . E0 & FINISHDO cause the HOLD . /F0 flip-flop to be reset, thus HOLD./ F0 remains true until USOR . . F . occurs. Assuming the next Micro to be executed is the 7C Micro, the data read from tape can be written into S-Memory.

Upon completion of the execution of the 7C Micro, executing another 1C Micro (Move U to Sink) will again cause the same to occur. NO OP's will be executed until the U-Register is full. The concurrent MFETCH operations are shown when MSTARTK. is true. MSTARTK. initiates a memory cycle which read the next Micro to be executed from S-Memory. The Micro "fetched" is stored in the ML-Register until FINISHDO and HOLD ./F0 are true. With these two levels true, M ← ML+UF0 is true which enables the M-Register in the D-Set Mode.



√ Fig. II-116 RUN MODE AND 1C MICRO (U-REGISTER SOURCE)

CASSETTE POSITIONING

The position of the Cassette in respect to the beginning of Tape (BOT) should be considered prior to initiating a Cassette Start. The first time the cartridge is inserted and locked in position, an automatic rewind will cause Tape to position in the clear leader area (BOT). If the Tape has previously been read, a rewind of Tape by either:

1. Depressing the Rewind button on the Console or
2. By "unlocking" the Tape cartridge from the latched position and then relocking it again will cause Tape to position in the clear leader area (BOT).

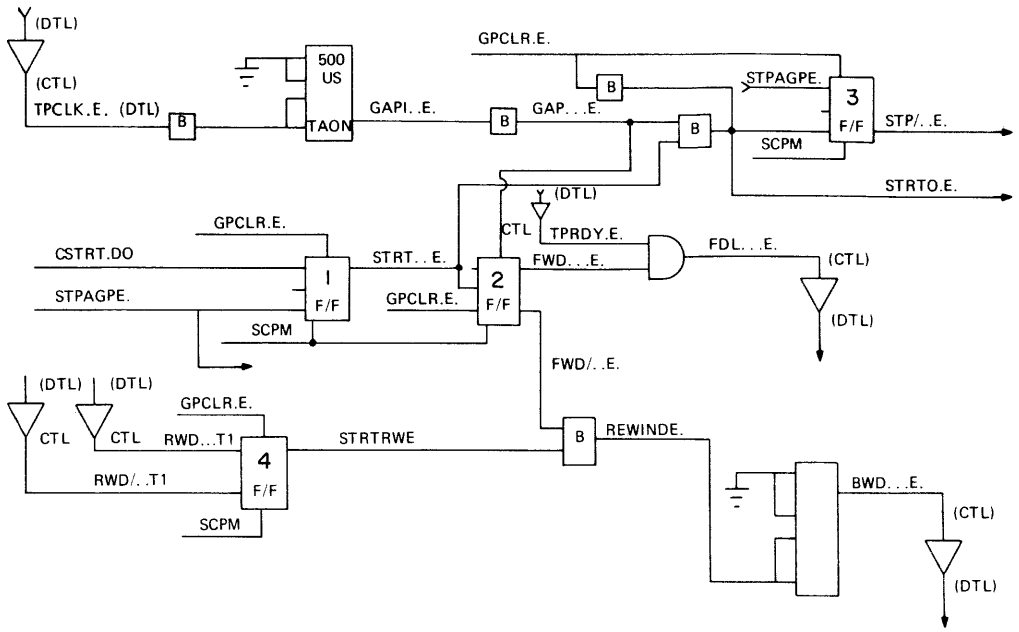
√ CASSETTE START LOGIC

The Cassette's control logic within the Processor provides the facility to start tape by applying forward drive to the Cassette. Forward Drive can be sent to the Cassette's drive logic in either the RUN or TAPE Mode. In order to send the forward drive level to the Cassette's drive logic, the level CSTRT . D0 must be true. CSTRT . D0 is true for when either of the two following conditions are true.

TAPE MODE:
1. Power ON (Processor & Cassette)
2. Mode Switch set to MTR
3. Start Button Depressed

RUN Mode:
1. Power ON (Processor & Cassette)
2. Mode Switch set to RUN
3. 2E Micro (Cassette Control) is executed with the variants of the Micro indicating Start Tape.

With either of the above two conditions true and the tape Cassette Ready, Forward Drive will be sent to the Cassette's Drive Logic. Serial data will be read from the tape, transmitted to the Processor's control logic and assembled in the U-Register. The Start Logic within the Processor is illustrated in Figure II-117 and the Start Logic Timing is shown in Figure II-118.



√ Fig. II-117 START/STOP LOGIC

START SEQUENCE

1. Cassette Start CSTRT . D0 is true at J input of the Start FF when a Forward Drive condition is sensed.
   TAPE Mode * Start button depressed
   +RUN Mode * 2E Micro (with Start Cassette variant) CSTRT . D0
2. At the trailing edge of the clock(s) the Start FF is set and STRT . . E . comes true.
3. During this time the tape is not in motion, therefore, clock pulses are not received from the tape. Consequently, the Gap Multivibrator stays at the reset state and the level GAPI . . E . is true and through a buffer (GAP . . . E .) enables the set mode at the forward F . F.
4. At the trailing edge of clock(s) the Forward FF sets and FWD . . . DE comes true.
5. If the tape is ready to receive the command the Forward Drive level is sent through the Interface and forward tape motion begins.
6. The Start operation is now complete and the tape will continue forward until Forward Drive is removed by the Stop Logic.
   With STRT . . E . * GAP . . . E .
   A) The Stop FF is reset and STP/ . . E . is true, this enables gating the data bits to U-Register and the U-Full logic.
   B) The level STRTO . E . true is sent to clear Parity Checking, Timing FF and U-Register. (In data transfer logic)

When the tape clock appears the Gap Timer triggers and the GAP . . E . level goes false. This removes the level STRTO . E . at the data transfer logic.

The delay of the Gap Multivibrator is longer than the tape clock tape period. This keeps the level GAP . . . E . false except during gap time.

CASSETTE STOP LOGIC

To Stop tape motion, the Forward Drive level must be removed. The Forward Drive level (FDL . . . E .) will be false when any of the following conditions are true.

1. Tape Drive goes Not Ready
2. Forward Drive Flip-Flop is reset

The Forward Drive Flip-Flop is reset when any of the following are true.

1. Tape clock pulses are being received and the General Processor Clear Button (CPCLR . E.) is depressed.
2. The Start Flip-Flop is reset and tape clock pulses are not received causing the level GAP . . . E . to be true.

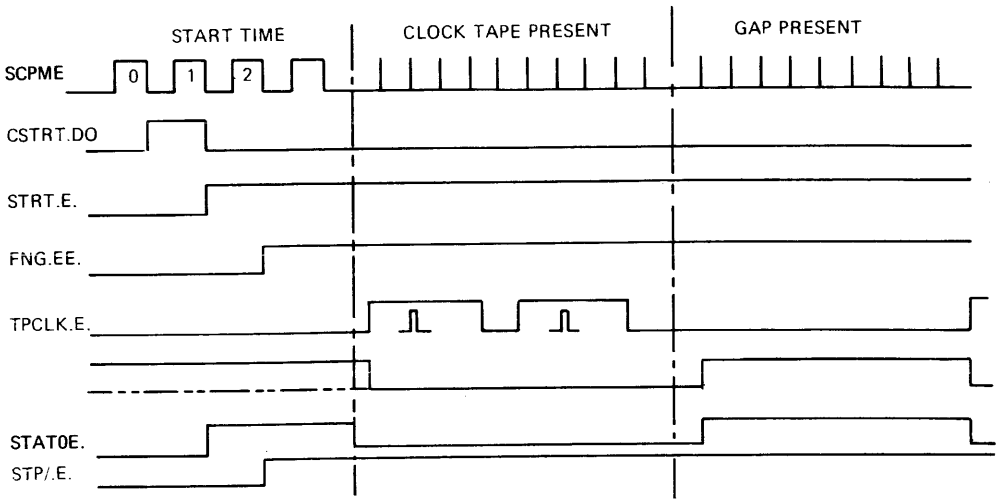


Fig. II-118

The Start Flip-Flop is reset when either the General Processor clear Button is depressed or when the level Stop at the Gap (STPAGPE.) is true. STPAGPE. is true when either a non-recoverable tape parity error is true (1+3ETIE.), or when CSTPG . D0 and FINISHDO are true. Refer to Figure II-119.

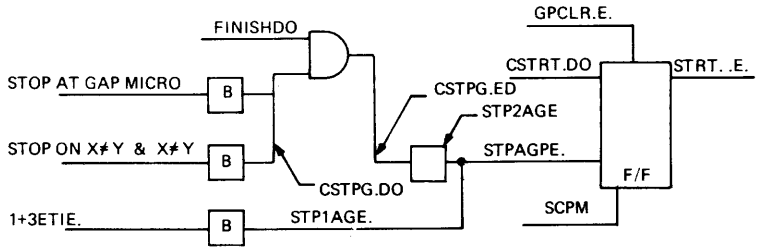


Fig. II-119 STOP LOGIC

Figures II-119 and II-120 illustrate the logic affected and the timing of the same when STPAGPE. is true. Note that GAPI . . E. must be true in order to stop at the Gap. GAPI . . E. true, indicates the absence of tape clock pulses for 500 us.

STOP AT GAP STOP SEQUENCE

1. STPAGE. is true and resets start FF at trailing edge of clock (1)
2. STRT . . E. is now false.
3. When the tape clock is no longer present, indicating end of record gap, the Gap Multivibrator will time out causing GAP . . . E. true. This enables the D-Mode to the forward FF which turns off with clock (n) forward FF reset removes Forward Drive from Cassette and stops the tape.

CASSETTE REWIND LOGIC

Prior to initiating a rewind of tape, forward drive level must be removed. When forward drive is removed, depressing the Rewind Button on the Console will cause a rewind drive level to be sent to the Cassette. Figure II-121 illustrates the Processor's logic which develops the backward drive level (BWD . . . E.) when the rewind button is depressed. Releasing the rewind button will reset the Start Rewind (STRTRWE .) Flip-Flop; however the control logic within the Cassette will continue to cause tape to be rewound until the Beginning of Tape (BOT) mark is sensed. The timing associated with Figure II-121, is illustrated in Figure II-122.

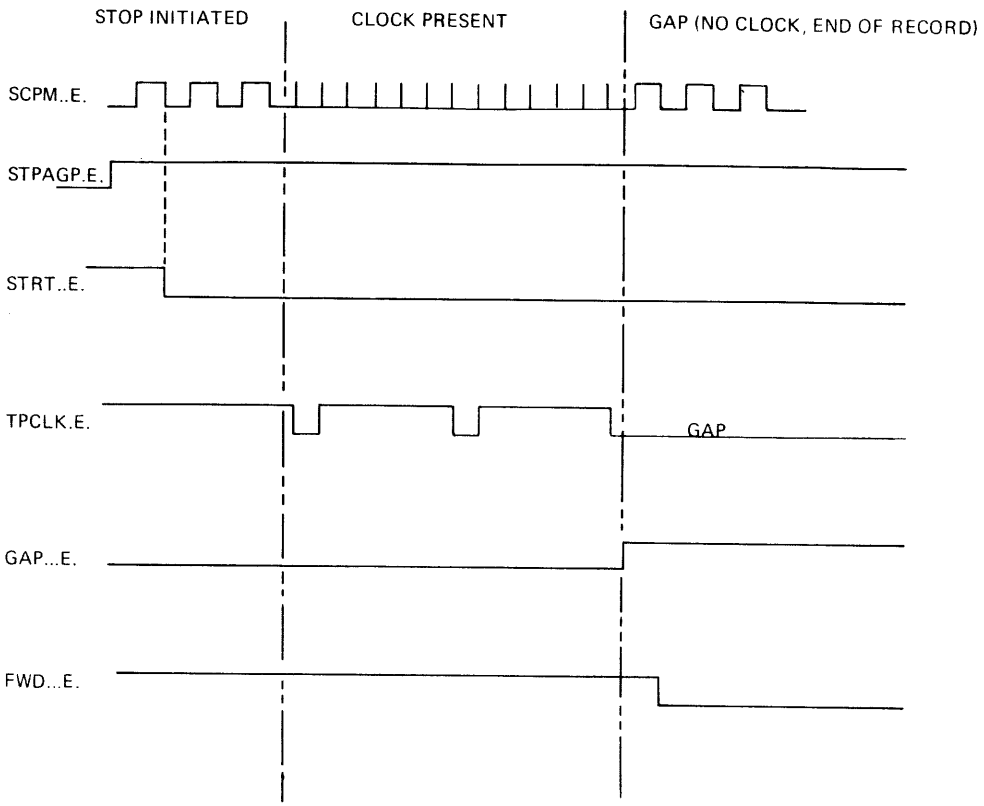


Fig. II-120

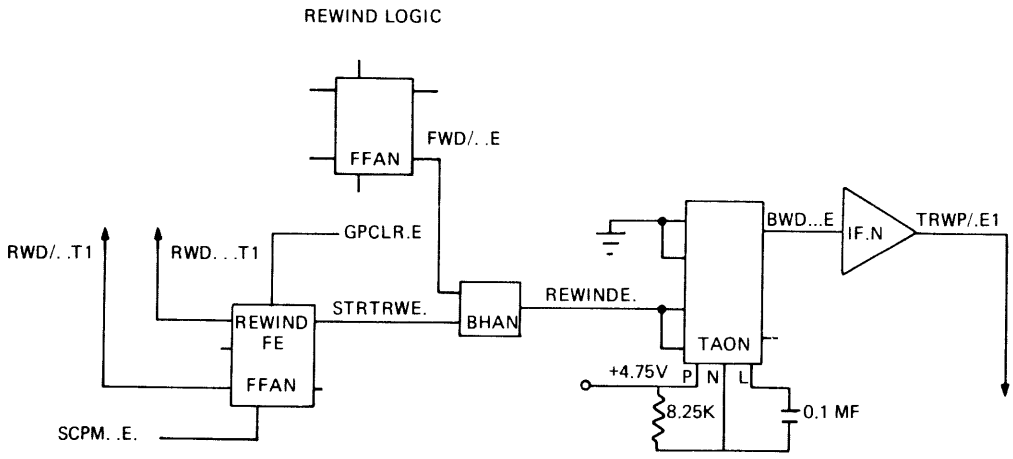


Fig. II-121 REWIND LOGIC

EXECUTION OF MICROS

Each of the twenty-four Micros when executed will cause a definite sequence of events to occur which is applicable to the individual Micro currently executing. In addition to the basic functions which occur when a particular Micro is executed, most of the Micros have available various bit configurations which permits the individual Micros to perform more than one particular function.

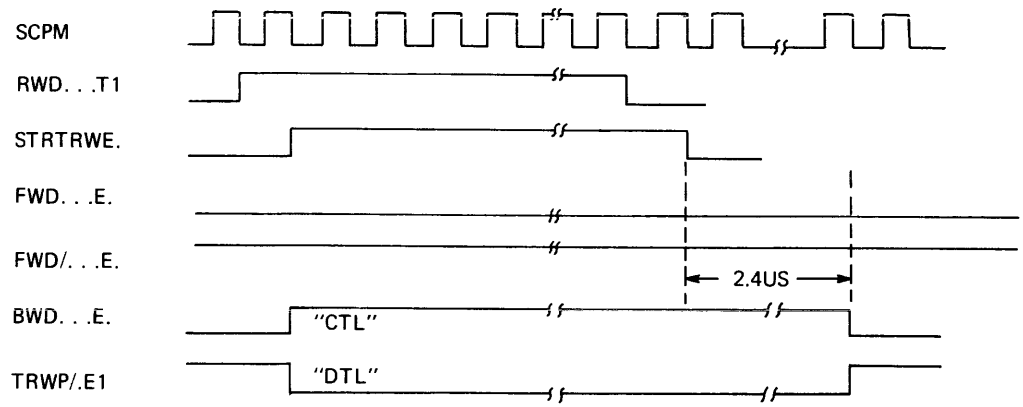


Fig. II-122 REWIND CASSETTE TIMING

Example: An example of the various functions a particular Micro when executed can perform is the execution of the 1C Micro. The 1C Micro permits one of a number of source registers to be selected as well as one of a number of sink registers. The source and/or sink registers can be 24-bits in length, 16-bits in length (in the case of the FL-Register) or 4-bits in length. In addition to the selection of particular registers as source and sink, a move to the M-Register will perform a bit OR-ing of the source registers information with the up coming Micro from the ML-Register.

In summary, most of the Micros when executed will perform a function which is specifically designated by the bit configuration of the particular Micro executed. An example execution of each of the Micros is shown on the following pages. The Micros which in addition to the basic functions they perform also provide unique functions within as designated by their particular bit configurations will be shown in more than one example. Each Micro when executed is held in the M-Register for the duration of the execution of the Micro. It is necessary to expose the current Micro in the M-Register to the Micro Distribution Bus lines (MOP 15 through BTO) where it is distributed throughout the System and executed. Two terms (RUNS . . FO & HOLD . /F0) must be true to expose the Micro in the M-Register to the Micro Distribution Bus. When either of these two levels is false, the contents of the M-Register is not gated to the Micro Distribution Bus. When the Processor is in the Halt mode, another source is available to the Micro Distribution Bus via hard wired logic which executes a 1C Micro. This operation is explained during Console Operations.

1C MICRO

The function of the 1C Micro is to move a source registers data to a sink register. The registers not permissable as source or sink are stated in Section 1 of this manual. The basic execution time of the 1C Micro is 2 clock periods (4 MHz). The exceptions are as follows:

1. When the source is BCD, 3 clocks
2. When the sink is MAR(A), 4 clocks
3. When the sink is MAR(A) and source is BCD, 5 clocks (3 for BCD and 2 extra clocks for MAR(A) as sink)
4. When the U-Register is source, "many" clocks

Each of the above five cases is explained separately. The 1C Micro which is executed when the Processor is halted is explained during the explanation of Console Operations.

2 CLOCK EXECUTION

The basic functions which occur when the 1C Micro is executed that requires 2 clock periods is illustrated in Figure II-123. The example shown moves the L-Register (24 bits) to the T-Register (24 bits). Assuming a 2 clock Micro has been executed prior to the execution of the 1C Micro, MFETCHFO will be true during the first S1 time. A previous MFETCH operation which occurred during the execution of the previous 2 clock Micro will generate a S-Memory read cycle which will cause memory read data to be on the memory read data inputs to the ML-Register. With MFETCHFO true at this time, the read data (32-bits of information from a word address of S-Memory) will be "latched" into the ML-Register as shown. Note that the ML-Register at this time actually contains two Micros, although only one will be used at this time. Either the 1C Micro and the previous Micro or the 1C Micro and the Next Micro. The value of the MAR(A)'s 4-bit position will determine which of the two Micros is gated to the M-Register. For this explanation, assume the 1C Micro is set into the M-Register at this time. The trailing edge of the 4 MHz clock which finds FINISHDO true, will set the 1C Micro, from the ML-Register, into the M-Register. Functionally, two operations will occur during the execution of the 1C Micro:

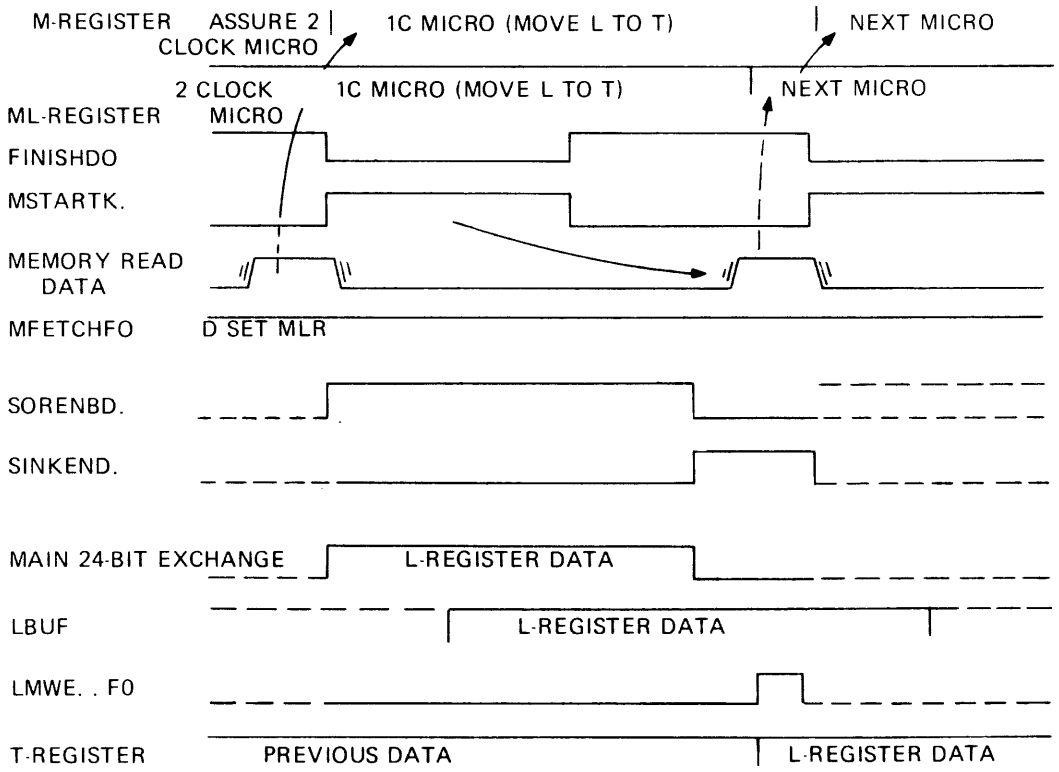


Fig. II-123 1C MICRO TIMING 2 CLOCK EXECUTION

√ 1. A MFETCH operation will occur which will generate a S-Memory read cycle to read the next Micro to be executed when the 1C Micro is finished. This is done regardless of whether or not the next Micro is at this time in the ML-Register. The trailing edge of the 4MHz clock which finds FINISHDO true sets the Memory Start Flip-Flop (MSTARTK .). Read Data is available approximately 434 ns after the trailing edge of the 4 MHz clock pulse which set the 1C Micro into the M-Register. The read data remains present until approximatey 511 ns from the trailing edge of the same clock pulse. With MFETCHFO true, this read data (the next micro to be executed) is set into the ML-Register. The trailing edge of the 4 MHz clock which finds FINISHDO true during the S1 time of the execution of the 1C Micro will set the next Micro to be executed into the M-Register. Note that if a Memory Refresh Cycle has been requested during the execution of the 1C Micro, the next Micro to be executed will remain in the ML-Register but will not be gated to the M-Register as shown. A N0-OP will be executed for two clock periods during the refresh cycle. When the refresh cycle finishes, the next Micro will then be gated from the ML-Register to the M-Register.

2. Presence of the 1C Micro in the M-Register and exposed to the Micro Distribution Bus will cause the Micro to be decoded. The decoding logic will generate the Source Enable (SORENBD .) level during T0, T1, and T2 times. A Local Memory address and Chip Select levels will also be generated at this time which will allow the L-Registers data in Local Memory to be read and gated to the Main 24-bit Exchange. The L-Register data on the Main Exchange is set into LBUF with the trailing edge of the inverted 4 MHz clock (CLK4/ .K0). When T3 time occurs, the decoding logic develops the Sink Enable level (SINKEND .) which also develops the Local Memory Write Enable pulse (LMWE . . F0). The address lines and chip select levels for the T-Register will also be true during the time SINKEND . is true. The L-Register data in LBUF is then written into the T-Register within Local Memory. In summary, the execution of the 1C Micro has moved the contents of the L-Register to the T-Register (both within Local Memory) and has executed a MFETCH operation to read the next Micro to be executed from S-Memory.

3 CLOCK EXECUTION

The basic functions which occur when the 1C Micro is executed that requires 3 clock periods is shown in Figure II-124. The example shown moves the SUM of the X and Y Registers (both 24-bits in length) to the FA-Register. Note that

the BCD Sum (decimal corrected sum) of the X and Y-Registers is developed due to assumption that the CPU-Register is set to 1. The generation of a decimal corrected sum requires an additional clock period due to the additional functions which occur within the 24-bit Function Box when the decimal sum is designated. If the SUM were Binary, only two clock periods would be required. The execution of the 3 clock 1C Micro is similar to that of the 2 clock period 1C Micro in that a MFETCH will occur and a move of a source register to a sink register also occurs.

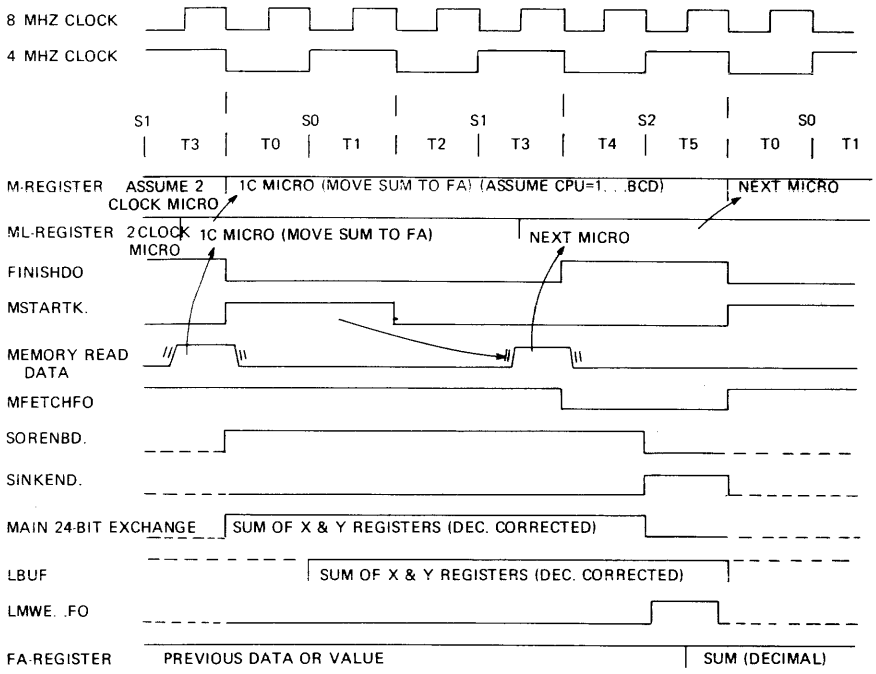


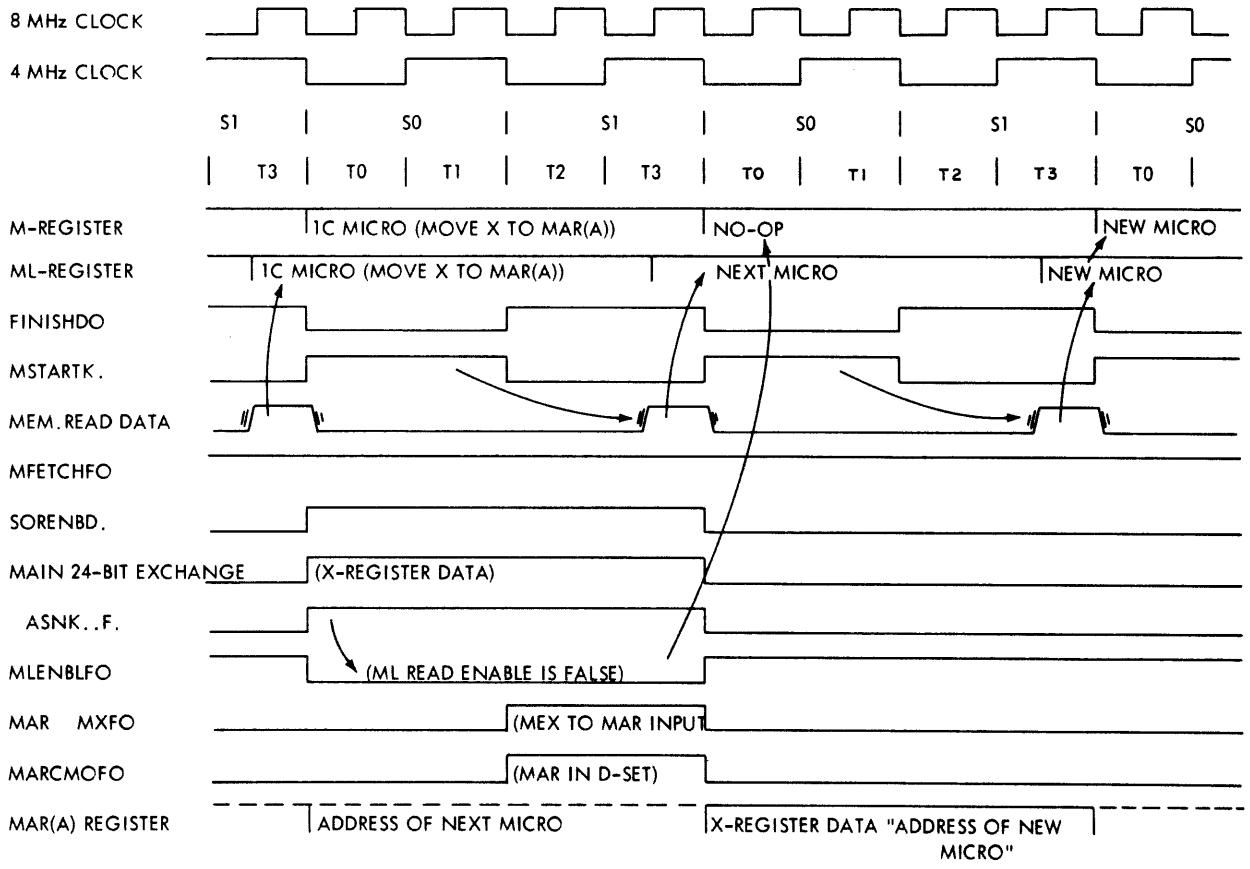
Fig. II-124 1C MICRO TIMING 3 CLOCK EXECUTION

During the execution of the 3 clock 1C Micro, FINISHDO is delayed until S2 time which allows time for the addition of X & Y to occur and the decimal correction of the same to occur. The MFETCH operation is initiated at the beginning of S0 time with the read data (next Micro) available during T3 time. The next micro is then stored in the ML-Register and will be set in the M-Register with the trailing edge of the 4 MHz clock pulse which finds FINISHDO true. The source enable (SORENBD.) is extended until T5 time when sink enable (SINKEND.) is true.

During source enable time (T0 through T4), both the X-Registers data (A-DATA) and the Y-Registers data (B-DATA) is read from Local Memory simultaneously and gated to the 24-bit Function Box. The output of the 24-bit Function Box is gated onto the Main 24-Bit Exchange. The trailing edge of the inverted 4 MHz clock sets the Main Exchange data into LBUF. Local Memory Write Enable (LMWE . . F0) is true during T5 time which allows the contents of LBUF (Decimal corrected SUM) to be written into the FA-Register within Local Memory. During sink enable time, the address lines and chip select levels are true which designate the FA-Register as Sink.

4 CLOCK EXECUTION

The basic functions which occur when the 1C Micro is executed that requires 4 clock periods is shown in Figue II-125. The example shown moves the X-Register (19 Least Significant Bits) to the Memory Address Register (MAR(A)). During S0 & S1 time, the basic function which occurs is the gating of the X-Register data in Local Memory, to the Main 24-bit Exchange and into the MAR(A) Register. A MFETCH operation occurs at this time in the usual manner, and the read data is latched in the ML-Register. The operation differs however from the "normal" 2 clock operation in that when FINISHDO is true, the next Micro in the ML-Register is not set into the M-Register. When the 1C Micro is executed with MAR(A) designated as the sink, the decoding logic develops the term ASNK . . F. which causes the ML-Register's read enable (MLENBLFO) to be false. With MLENBLFO false, the next Micro which normally would be set in the M-Register with the trailing edge of the 4 MHz clock is not read from the ML-Register. This effectively causes a NO-OP to be set in the M-Register. During S0 & S1 time, the decoding logic develops the address lines and chip select levels to address the



1C MICRO TIMING: (MOVE X TO MAR(A))

FORMAT: 0001 0000 1010 0100

√ Fig. II-125 1C MICRO TIMING 4 CLOCK EXECUTION

X Register in Local Memory. With source enable (SORENBD .) true, the X-Register data (24-bits) is gated to the Main 24-bit Exchange. ASNK . . F. and FINISHDO cause MAR MXFO and MARCMOFO to be true.

The MAR(A) register is a 19-bit register: therefore, only the 19 LSBs of the Main 24-bit Exchange (MEX 18 through 00 BTO) are set in the MAR(A) Register with the trailing edge of the 4 MHz clock. The X-Register data which is in the MAR(A) register during S0 & S1 time is the S-Memory address of the New Micro to be executed. The MFETCH operation which is initiated with MSTARTK. during S0 time causes a read memory cycle to occur which reads this New Micro from S-Memory. With MFETCHFO true, this New Micro is "latched" into the ML-Register and gated into the M-Register to be executed at the next S0 time. Note that MLENBLFO is now true, which allows reading the New Micro in the ML-Register.

5 CLOCK EXECUTION

The basic functions which occur when the 1C Micro is executed which requires 5 clocks to finish is illustrated in Figure II-126. Due to the similarity of the 3 clock example (BCD SUM of X & Y to the FA-Register as sink) and the 4 clock example (MAR(A)) as the sink Register) the details of the 5 clock execution are not shown. Reference the 3 & 4 clock execution examples for details. During S0, S1, & S2 time, the decimal corrected SUM of the X & Y-Registers data is developed, gated to the Main 24-bit Exchange, and set in the MAR(A) Register with the trailing edge of the 4MHz clock which occurs during S2 time. Although a MFETCH occurs during this time period, the Next Micro read from S-Memory and "latched" in ML is not set in the M-Register. A NO-OP is forced during S3 & S4 time at which time another MFETCH operation occurs to read the New Micro from S-Memory at the address specified by the SUM of X & Y now in the MAR(A) Register.

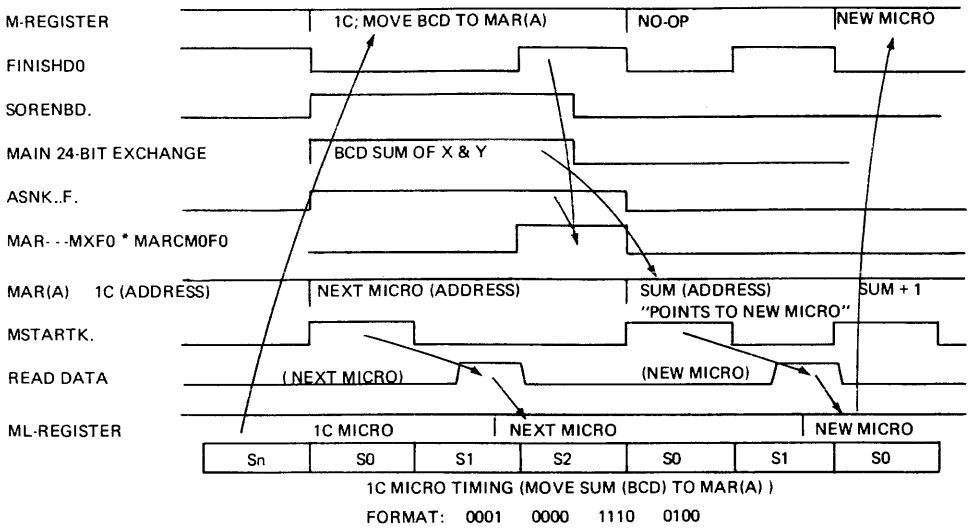


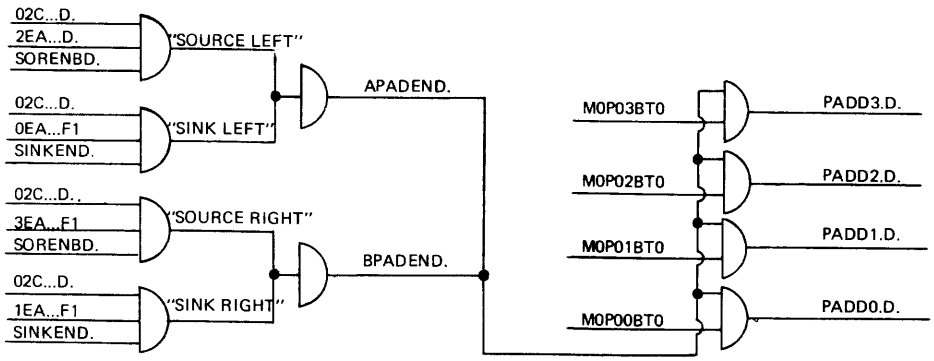
Fig. II-126 1C MICRO TIMING 5 CLOCK EXECUTION

2C MICRO

The function of the 2C Micro is either to move a source register to a word of Scratch Pad or move a source Scratch Pad word to a sink register. Any word of either Scratch Pad right or left is permissable as either a source or a sink. The registers not permissable as source or sink are stated in Section 1 of this manual. The basic execution time of the 2C Micro is 2 clock periods (4 MHz). The exceptions are as follows:

1. When the source is BCD (SUM or DIFF), 3 clocks;
2. When the sink is MAR(A), 4 clocks.

The execution of the 2C Micro (2, 3, or 4 clock period duration) is identical to that of the execution of the 1C Micro (2, 3, or 4 clock duration). The exception being the decoding of Mop Bits 5 & 4 to determine the move direction and whether right or left Scratch Pad is designated as source or sink. Figure II-42, of the Local Memory explanation illustrates a typical example of decoding Mop Bits 5 & 4 to determine the particular word of Scratch Pad addressed and whether the word is the source or sink. Four gates are used to select either a word of APAD (A-DATA) or BPAD (B-DATA) as either source or sink as illustrated in Figure II-127



√ Fig. II-127 SOURCE/SINK . . . R/L SCRATCH PAD ADDRESSING

2, 3 AND 4 CLOCK EXECUTION

An example of the timing of the execution of the 2, 3, & 4 clock 2C Micro is illustrated in Figures II-128, II-129, & II-130 respectively. As the execution is similar to that of the 1C Micro, reference the examples given for the 1C Micro for details.

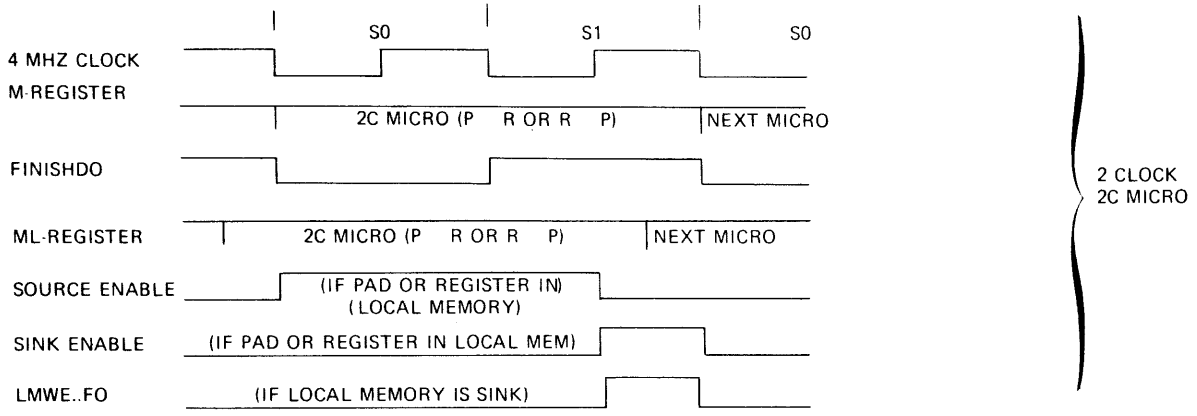


Fig. II-128 2 CLOCK 2C MICRO

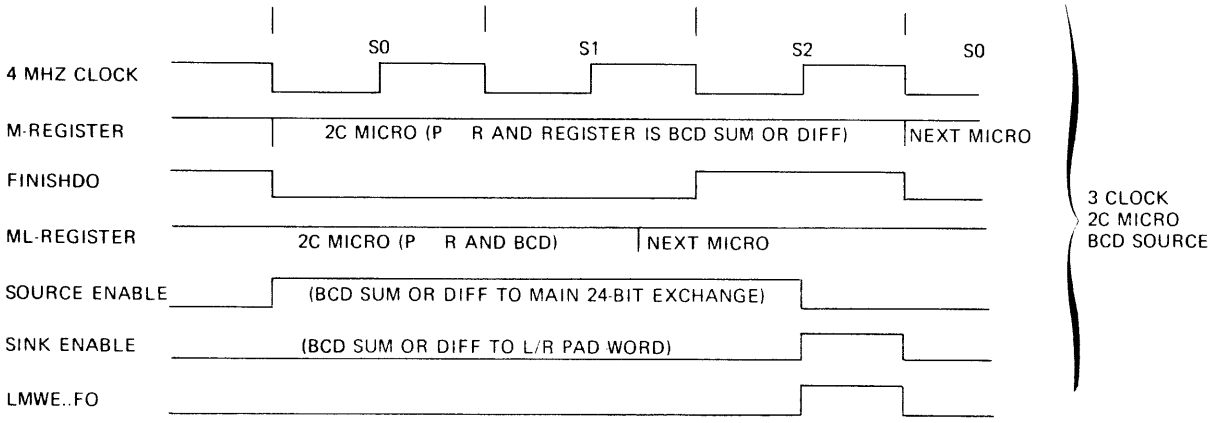


Fig. II-129 3 CLOCK 2C MICRO BCD SOURCE

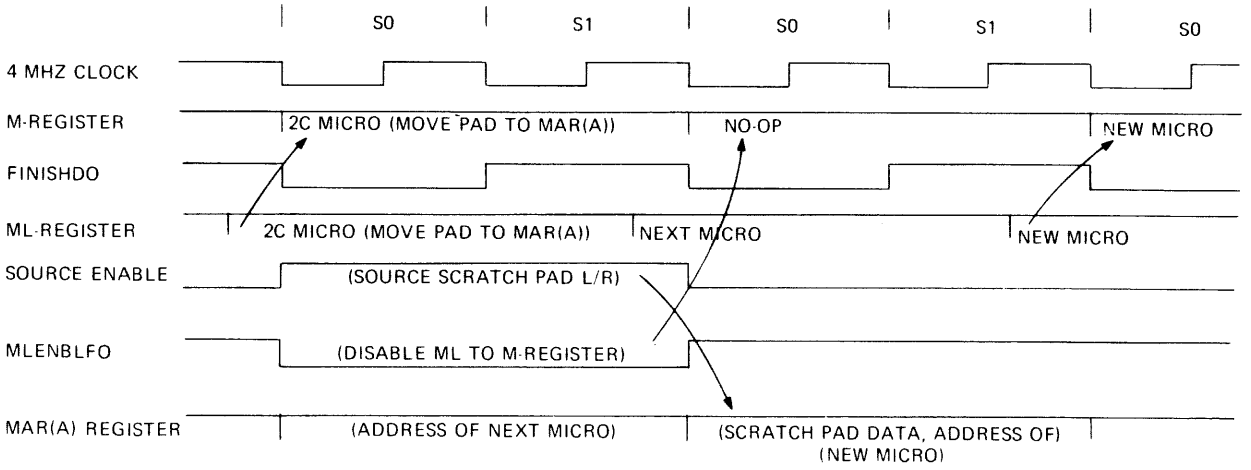


Fig. II-130 4 CLOCK 2C MICRO MOVE PAD TO MAR(A)

3C MICRO

The function of the 3C Micro is to perform a particular operation as selected by the variants on the designated Source/Sink Register. The Source and Sink register is the same; therefore, the source register is usually changed when the execution of the Micro is completed. The registers permitted as source and sink are stated in Section 1 of this Manual. The execution time of the 3C Micro is 2 clock periods except for the following condition:

When either the Increment and TEST or Decrement and TEST is performed, and the operation results in the generation of a carry, (Incre & TEST) or a borrow (Decre & TEST), at which time the execution time is 4 clock periods.

The 4-bit Registers permissable as source and sink may be either located within Local Memory or they may be one of the four 4-bit Discrete Registers (CA, CB, CC or CD).

2 CLOCK EXECUTION (4 BIT REGISTER WITHIN LOCAL MEMORY)

Figure II-131, illustrates the basic data flow of the 3C Micro when a 4-bit Register located within Local Memory is designated as Source and Sink. The 4-bit addressable registers within Local Memory permissable as source and sink when executing the 3C Micro are all within the A-DATA portion; therefore, B-DATA is not referenced during the execution of the 3C Micro. The 4-bit register selected is gated to the 4-Bit Function Box where the operation selected by the variant bits of the Micro is performed. The output of the 4-Bit Function Box is then gated to the Main 24-Bit Exchange such that each consecutive 4-bits of the Main 24-Bit Exchange will contain the result of the 4-bit function performed. This "New" value of the 4-bit register is then "latched" into LBUF and set into the same register within Local Memory. During Sink Enable time, only the address and chip select levels to the particular 4-bit register will be selected.

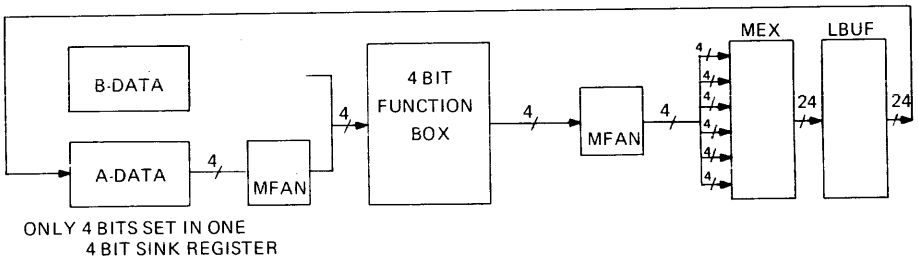


Fig. II-131 3C MICRO DATA FLOW

Figure II-132 illustrates the basic functions which occur when the 3C Micro is executed and a register within Local Memory is Source/Sink. It is also assumed that the function performed does not result in a skip of the next Micro. Note the skip of the next Micro occurs when the function is either Increment and TEST and a carry is generated or Decrement and TEST and a borrow is generated.

A MFETCH operation occurs concurrent with the operation performed on the 4-bit register in the 4-bit Function Box. As the function performed on the register does not generate a skip, the next Micro read from S-Memory during the concurrent MFETCH operation is gated from the ML-Register to the M-Register and executed when the 3C Micro is finished.

2 CLOCK EXECUTION (CA, CB, CC, or CD REGISTER)

Figure II-133 illustrates the basic data flow of the 3C Micro when either the CA, CB, CC, or CD Register is selected as source and sink. The contents of the particular register selected is gated to the 4-Bit Function Box where the function selected by the variant bits of the Micro is performed. The output of the 4-Bit Function Box is again gated to the Main 24-bit Exchange such that each consecutive four bits of the Main Exchange will contain the result of the function performed. Only the four LSB of the Main 24-bit Exchange are inputs to each of the four 4-bit Registers. The timing logic will cause the four bit register selected as source and sink to be in the D-Set mode at which time the trailing edge of the 4 MHz clock will set the "New" value in the register selected.

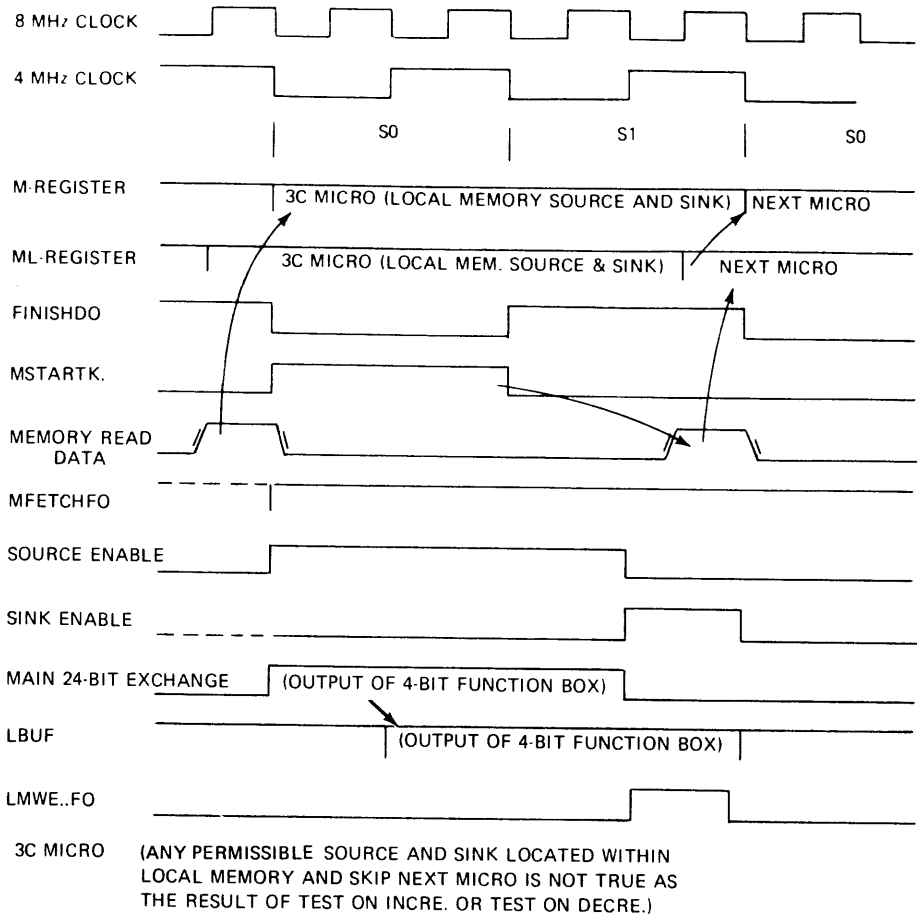


Fig. II-132 3C MICRO LOCAL MEMORY IS SOURCE/SINK

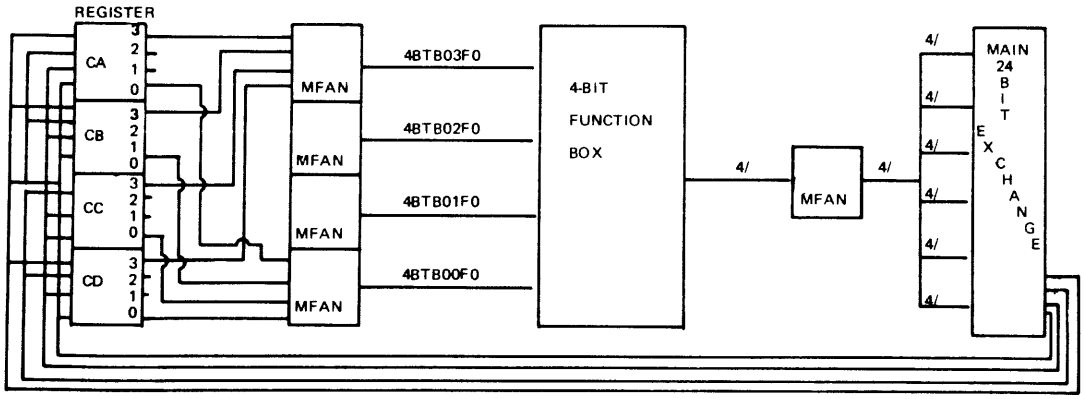


Fig. II-133 3C MICRO: DATA FLOW DISCRETE REGISTER AS SOURCE/SINK

Figure II-134 illustrates the basic functions which occur when executing the 3C Micro and the function is performed on a discrete register not located within Local Memory. It is also assumed a skip of the next Micro is not generated as the result of an Increment and TEST and a carry is generated or a Decrement and TEST and a borrow is generated. The execution of the 3C Micro when a discrete register is selected rather than one in Local Memory varies slightly in that the source enable is true for two clock periods. The function is performed in the 4-Bit Function Box and immediately gated to the Main 24-bit Exchange. The results of the function performed are set in the 4-bit register when the D-Set Mode enable to the register is true and the trailing edge of the 4 MHz clock occurs.

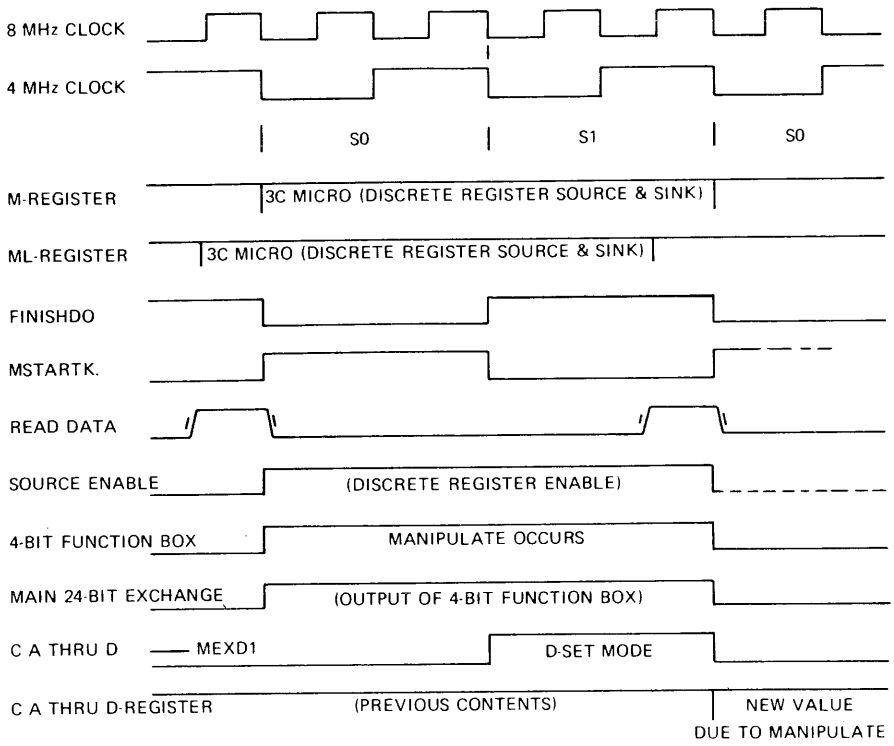


Fig. II-134 3C MICRO CA, CB, CC, CD REGISTER IS SOURCE OR SINK

4 CLOCK EXECUTION

When either the Increment and TEST or the Decrement and TEST is performed and the function results in a carry or borrow respectively, a skip of the next Micro "usually executed" occurs. This requires an additional 2 clocks to fetch the New Micro to be executed. This is true regardless of whether the register is discrete or within Local Memory. Figure II-135, illustrates the basic "Skip" functions which occur with either a discrete register or a Local Memory register selected as source/sink. The function selected occurs during S0 & S1 times with the result being stored in the sink register in the usual manner. During the second S0 & S1 times, a NO-OP is forced in the M-Register by gating all zeros to the input of the M-Register. SKIP . . F. is set with the trailing edge of the inverted 4 MHz clock. When set, SKIP . . F. prevents MLENBLFO from being true when FINISHDO is true, therefore, the next Micro in ML is not read but rather zeros are gated to the M-Register.

4C & 5C MICRO

The basic functional operation of the 4C and 5C Micro is similar in that the execution of either Micro "tests" a selected bit in a specific 4-bit register. If the test is a success, then a branch will occur which causes a "New" Micro to be executed, after a 2 clock NO-OP, located at a S-Memory address equal to either the sum of the Relative Branch Displacement value (Mop bits 03 thru 00) and the next in-line Micros address or the difference of the next in-line Micros address and the Relative Branch Displacement value (Mop bits 03 thru 00). The sum or difference is determined by the Displacement Sign (Mop bit 04).

Note that when either the 4C or 5C Micro is set in the M-Register for execution, the MAR(A) register is also incremented by one which points to the next in-line Micro to be executed. It is to this address in MAR(A) that the Relative Branch Displacement value is either added to or subtracted from. When the branch is to occur, the Relative Branch Displacement value (M-Register bits 03 thru 00) are either added to or subtracted from bits 07 thru 04 of the next in-line Micros address in the MAR(A)-Register. The gating is via the Main 24-bit Exchange and is illustrated in Figure II-137. Because the Relative Branch Displacement value effects bit positions 07 thru 04 of the MAR(A)-Register, a "branch forward" of up to fifteen 16-bit Micro Instructions from the next in-line Micro is possible when the Displacement Sign is positive. When the Displacement Sign is negative, a "branch backward" of up to fifteen 16-bit Micro Instructions from the next in-line Micro is also possible.

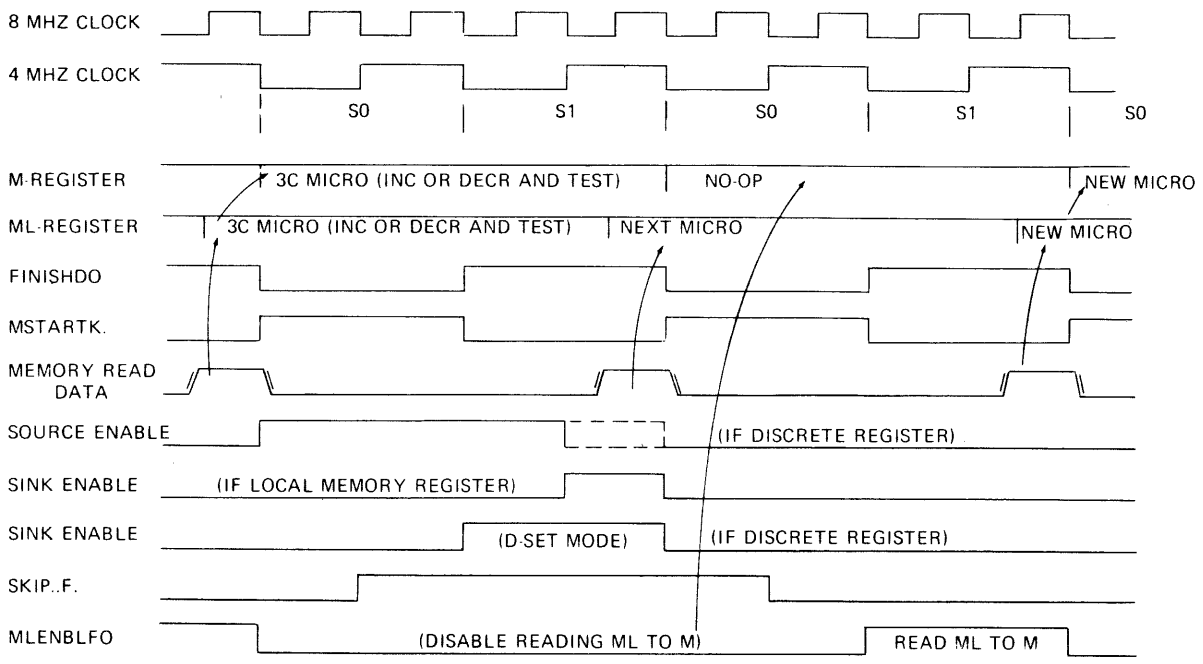


Fig. II-135 MICRO SKIP FUNCTIONS

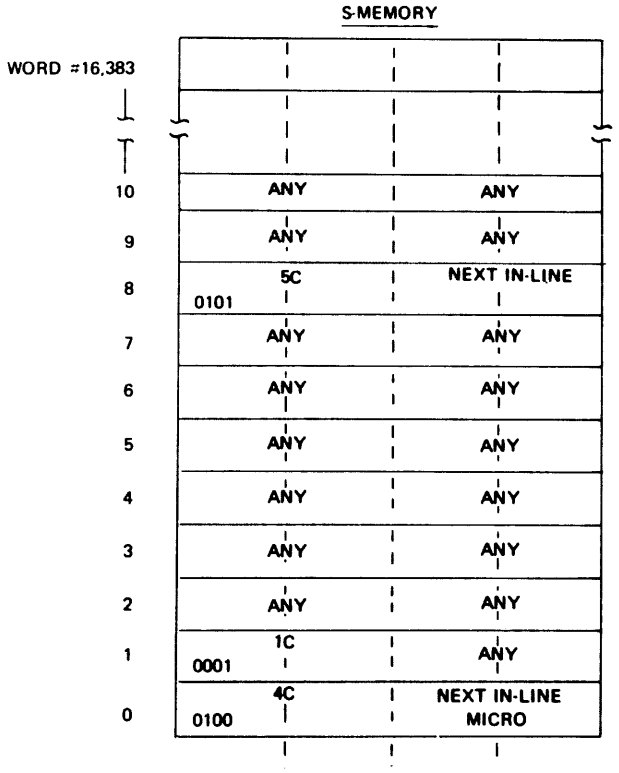


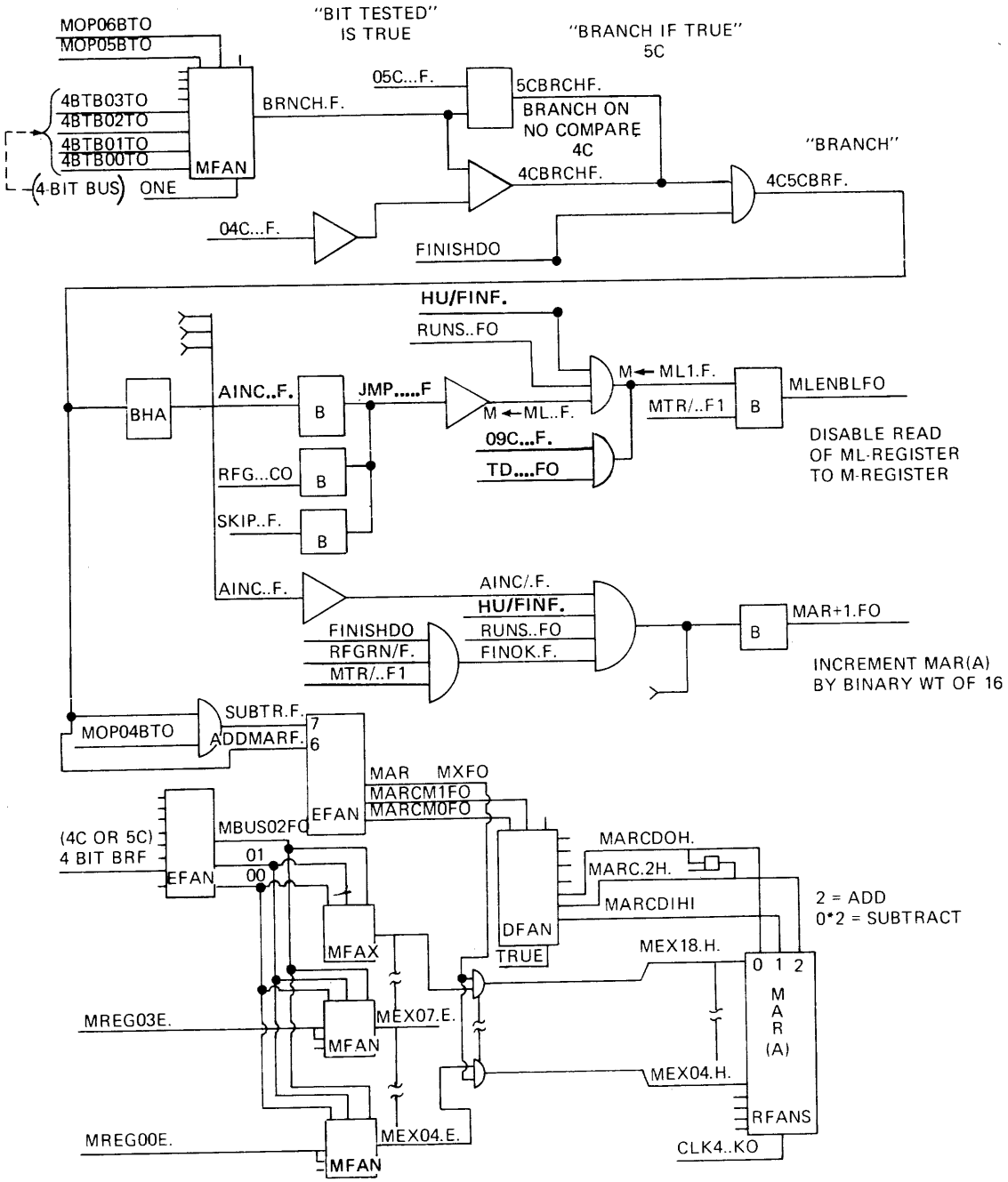
Fig. II-136 MAXIMUM BRANCH OF 4C AND 5C MICRO

Figure II-136 illustrates the "physical" maximum number of 16-bit Micro Instructions in S-Memory which can be branched over in either direction. If executing the 4C Micro and a branch is indicated, depending on the Branch Relative Displacement value either the Next in-line, 1C or any Micro up to and including the 5C Micro at Word No. 8 can be the next Micro executed after a 2 clock NO-OP. Note that this is assuming a branch in a positive direction.

When executing the 5C Micro and a branch negative is indicated, a branch backward to the 5C itself, or any Micro back to and including the 1C Micro can occur depending on the value of the Branch Relative Displacement. Again the Micro branched to will be executed after a 2 clock Micro is executed.

FUNCTIONAL DETAIL

The primary difference between the 4C & 5C Micro is that the 4C Micro will cause the branch to occur if the bit tested in the 4-bit register selected is false and the 5C Micro will cause the branch to occur if the bit tested is true. The logic which checks the particular bit being tested is shown in Figure II-137. BRANCH . F. will be true if the bit under test is true · when either the 4C or 5C Micro is executed.



√ Fig. II-137 4C AND 5C MICRO BRANCH BIT TEST LOGIC

The contents of the 4-bit Register selected is gated to the 4-bit Auxilliary-Bus (4BTB 03 thru 00 TO). These four lines are the 3 thru 0 inputs of an 8 Input Multiplexer (MFAN). The particular bit under test is designated by Mop bits 6 & 5. When the bit tested is true, BRNCH . F. is true. 5CBRCHF. is true when the bit tested is true and the 5C Micro is executed, 5CBRCHF. indicates a branch will occur. 4CBRCHF. is true when the bit tested is false and the 4C Micro is executed, it also indicates the branch will occur. When FINISHDO occurs, usually the ML-Registers read enable (MLENBLFO) is true, however when the branch is to occur, 4C5CBRF. will prevent MLENBLFO from being true, which forces a NO-OP to the M-Register for execution. During the time the NO-OP is executed (2 clocks) a MFETCH occurs to read the "branch" Micro at the incremented or decremented MAR(A) address. The new MAR(A) address is established at effectively the same time the NO-OP is gated to the M-Register. Note when 4C5CBRF. is true, MAR+1 .F0 is false which prevents the MAR(A) Register from being incremented by the normal binary weight of 16 which would point to the next in-line Micro to be executed. If the Branch Relative Displacement value is zero, then the normal next in-line Micro to be executed (already in the ML-Register when the NO-OP is executed) is again read from S-Memory during the MFETCH operation which occurs during the time the NO-OP is executed. 4C5CBRF. is also AND-ed with MOPO4BTO to cause a subtract to occur in the MAR(A) register. When MOPO4BTO is false, then an ADD will occur.

A 2 clock and 4 clock execution of the 4C Micro, when the source is not BCD (BICN with CPU = 01) is shown in Figures II-138 and II-139. The 2 clock example illustrates the test of the bit results in BRNCHF. true. As the 4C Micro will branch only when the bit tested is false, the branch will not occur. MAR(A) is incremented by 1 with MAR+1.F0 and the next inline Micro to be executed is gated to the M-Register when FINISHDO is true and the trailing edge of the 4 MHz clock occurs.

The 4 clock example illustrates the test of the bit results in BRNCHF. being false. The 4C Micro will branch on a false result of the bit test, therefore 4CBRCHF. will be true indicating a branch.

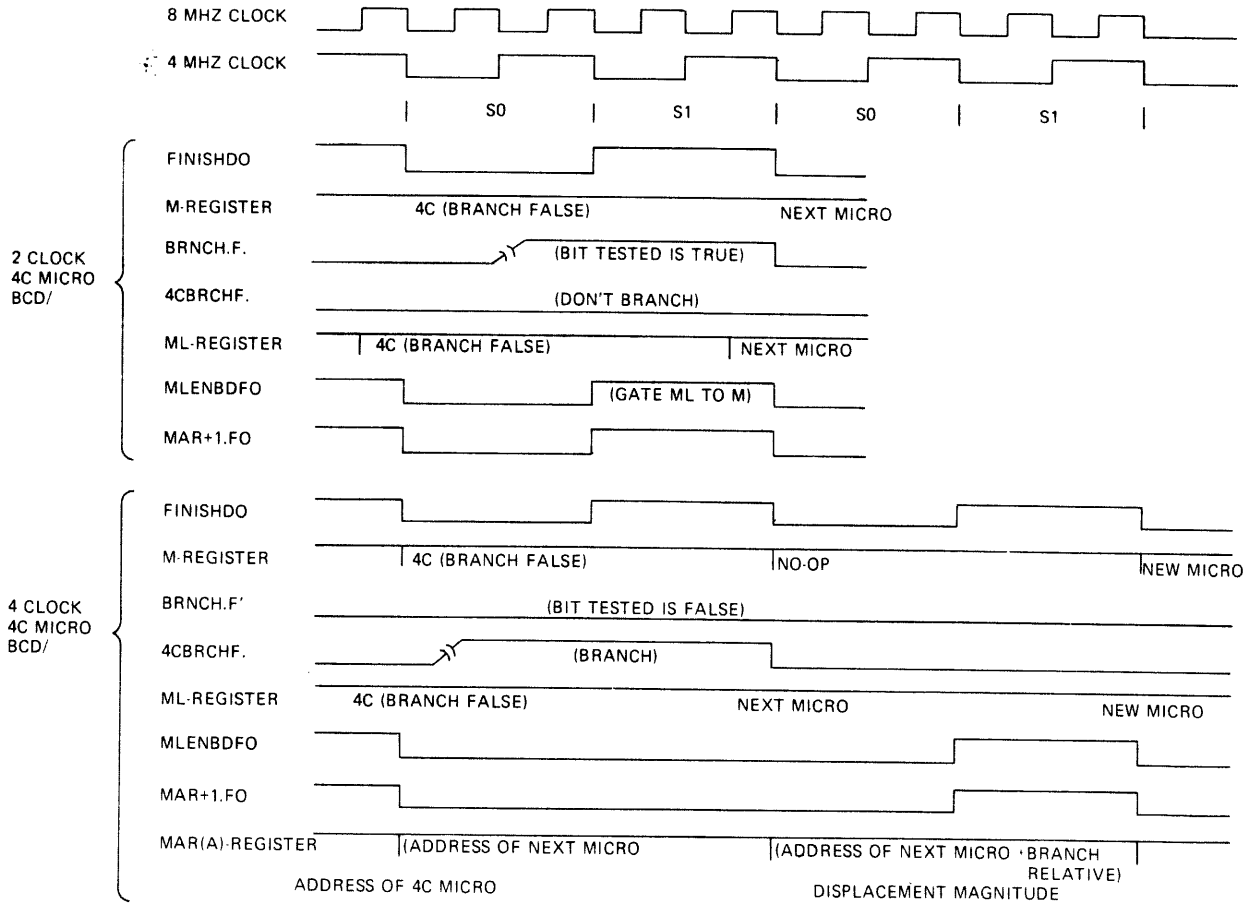


Fig. II-138 4C MICRO (2 AND 4 CLOCK EXECUTION) SOURCE NOT BCD

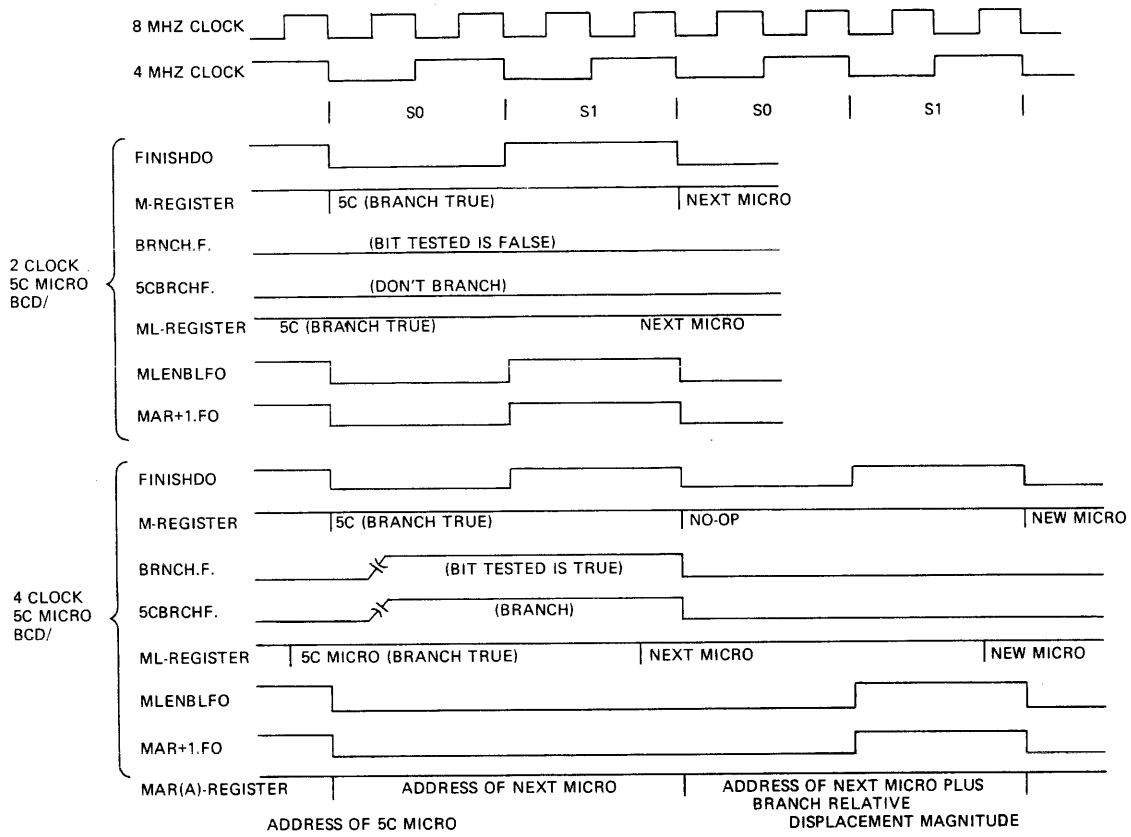


Fig. II-139 5C MICRO (2 AND 4 CLOCK EXECUTION) SOURCE IS NOT BCD

When FINISHDO occurs, MLENBLFO and MAR+1 . F0 will remain false, refer to Figure II-139. The trailing edge of the 4 MHz clock which occurs during S1 time when the 4C Micro is in the M-Register will set the Branch Micros address into the MAR(A) register as shown. An MFETCH will occur at this address during S0 & S1 times when the NO-OP is forced into the M-Register. When FINISHDO is true during S1 time of the NO-OP and the trailing edge of the 4 MHz clock occurs, the Branch Micro is then set into the M-Register from the ML-Register. Note that each Micro read from S-Memory during a MFETCH operation is temporarily stored in the ML-Register.

The 2 clock and 4 clock execution of the 5C Micro when the bit tested is false is shown in Figure II-139. A 2 clock execution occurs as the 5C Micro will only branch when the bit tested is true. Functionally, the 4C & 5C Micros are identical except for the condition which must be true to cause the branch. Figure II-140 assumes the source is not BCD (BICN and CPU = 01).

When the source is BCD (BICN and CPU = 01), then the execution time of the 4 or 5C Micro is either 3 clocks (No Branch) or 5 clocks (Branch is true). The additional clock is required to allow time for the decimal correction of the source register. Figure II-140, illustrates the basic timing of either the 4C or 5C Micro with a BCD source and Branch or No Branch. When BCD correction is designated, FINISHDO does not come true until S2 time, therefore an extra clock period is allowed for the decimal correction to occur. All other functions occur essentially the same as they occur during a 4 clock execution.

6C MICRO

The function of the 6C Micro is to skip the next up coming Micro when the "test" of a particular 4-bit Register indicates the skip is to be executed. Refer to Section 1 of this Manual for the Skip Test Variants used. Note that depending on the particular variant selected, the skip may or may not be executed when the "test" is either a success or fail. The basic execution time of the 6C Micro is as follows:

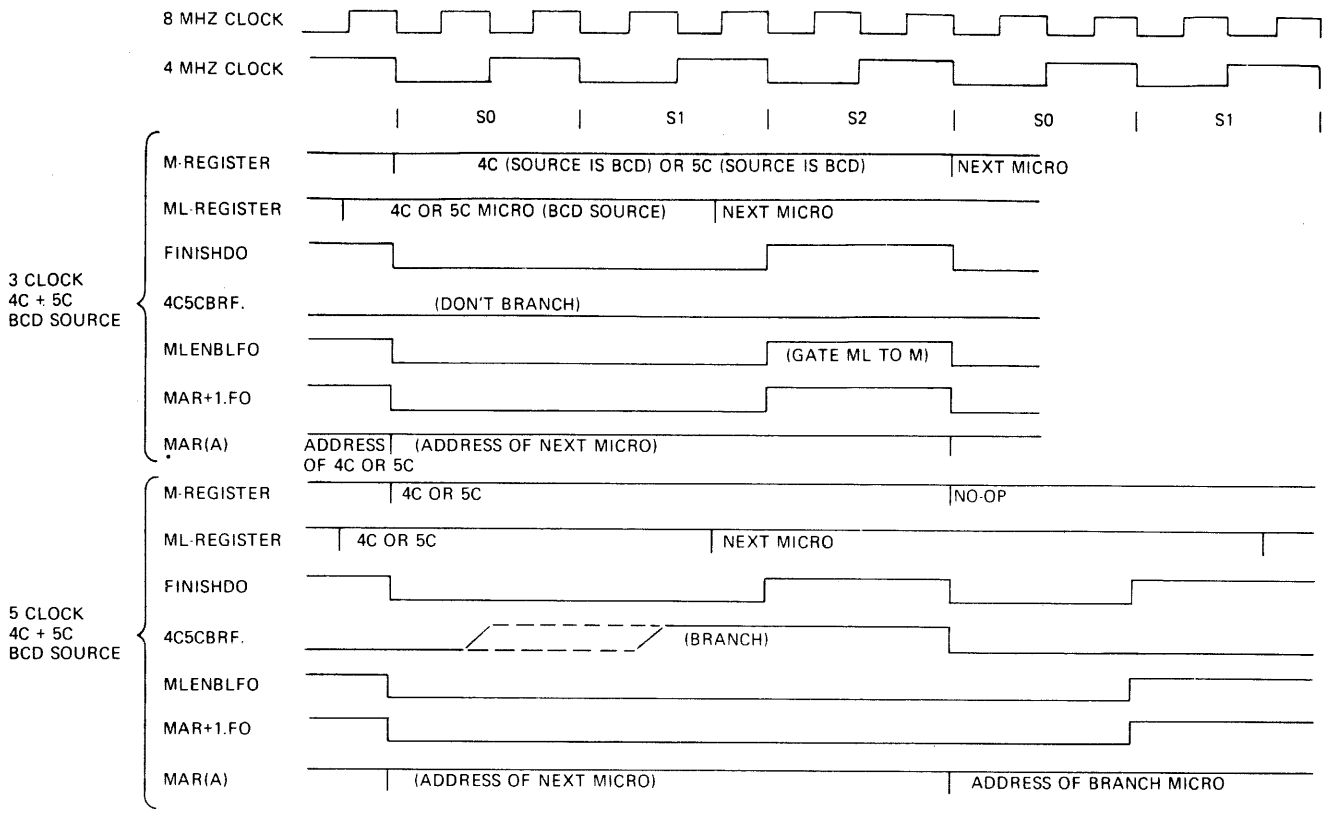


Fig. II-140 4C AND 5C MICRO TIMING: BCD SOURCE (BICN AND CPU = 01)

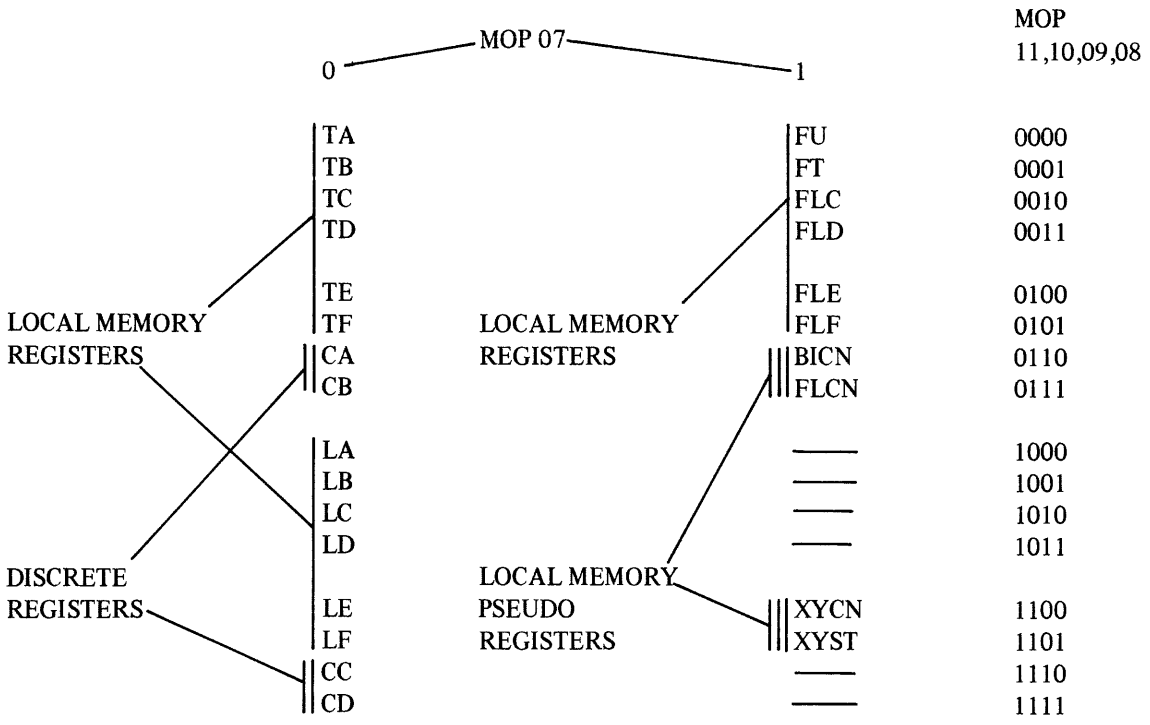


Fig. II-141 6C MICRO 4 BIT REGISTER SELECTION

1. Two (2) or three (3) clock periods if the skip is not taken.
2. Four clock. Two (2) clock periods followed by a second 2 clock period NO-OP if the skip is to be executed.
3. When the source is BCD (BICN with CPU = 01) then the execution time is 3 clocks followed by a 2 clock NO-OP if the skip is executed.

The forced 2 clock period NO-OP is required to fetch the next Micro to be executed.

- The 4-bit register selected as source is gated to the 4-bit Function Box to be compared with the Mask (Mop Bits 00 thru 03) which is also gated to the 4-bit Function Box. The 4-bit register selected may be either from Local Memory or a discrete Register or Pseudo Register as illustrated in Figure II-141

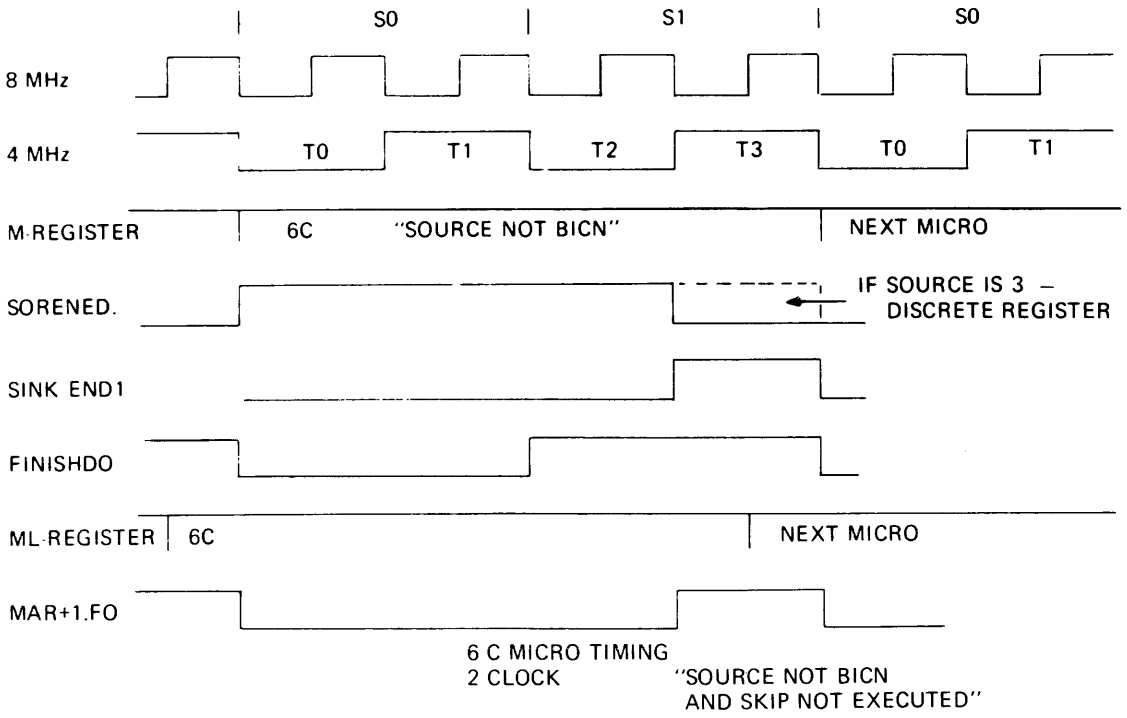


Fig. II-142 6C MICRO TIMING 2 CLOCK "SOURCE NOT BICN AND SKIP NOT EXECUTED"

2 CLOCK EXECUTION

Timing for a 2 clock execution is shown in Figure II-142. The trailing edge of FINISHDO sets the 6C Micro in the M-Register. At this same time a MFETCH operation is initiated to fetch the next Micro to be executed from S-Memory. This next Micro is latched in the ML-Register when the "read data" is available from S-Memory at approximately T3 time. The MFETCHFO F/F is set during S0 & S1 time allowing the Read data to set in the ML-Register. Note the ML-Register consists of LFANS and data is set in the latches with the leading edge of CLK4 (4 MHz). FINISHDO will occur at S1 time as BICN is not indicated. MAR+1. F0 is true when FINISHDO is true to increment the MAR(A) address by a bit value of 16. The first MAR+1 . F0 shown points the MAR(A) to the address of the Next Micro to be executed following the execution of the 6C Micro.

Note the source register source enable is extended during T3 time if the source register is not within Local Memory.

3 CLOCK EXECUTION

When the source register is BICN and CPU = 01 (CREG05CO true) an additional clock period is necessary to allow time for the Decimal Correction in the Adder portion of the Function Box to occur. Refer to Figure II-143. BICN is a pseudo register, however it is addressed by addressing the X & Y Register within Local Memory. For this reason SORENBD & SINKEND1 will be generated to source the X & Y Registers. A concurrent MFETCH operation occurs during S0 & S1 time and the memory read data is latched in the ML-Register at approximately T3 time. As FINISHDO does not occur until S2 time, the MFETCHFO F/F is reset at S1 time to disable the ML-Register from latching in zeros during the time the 4 MHz clock is true at T5 time. Note that Memory read data will be gone at this time.

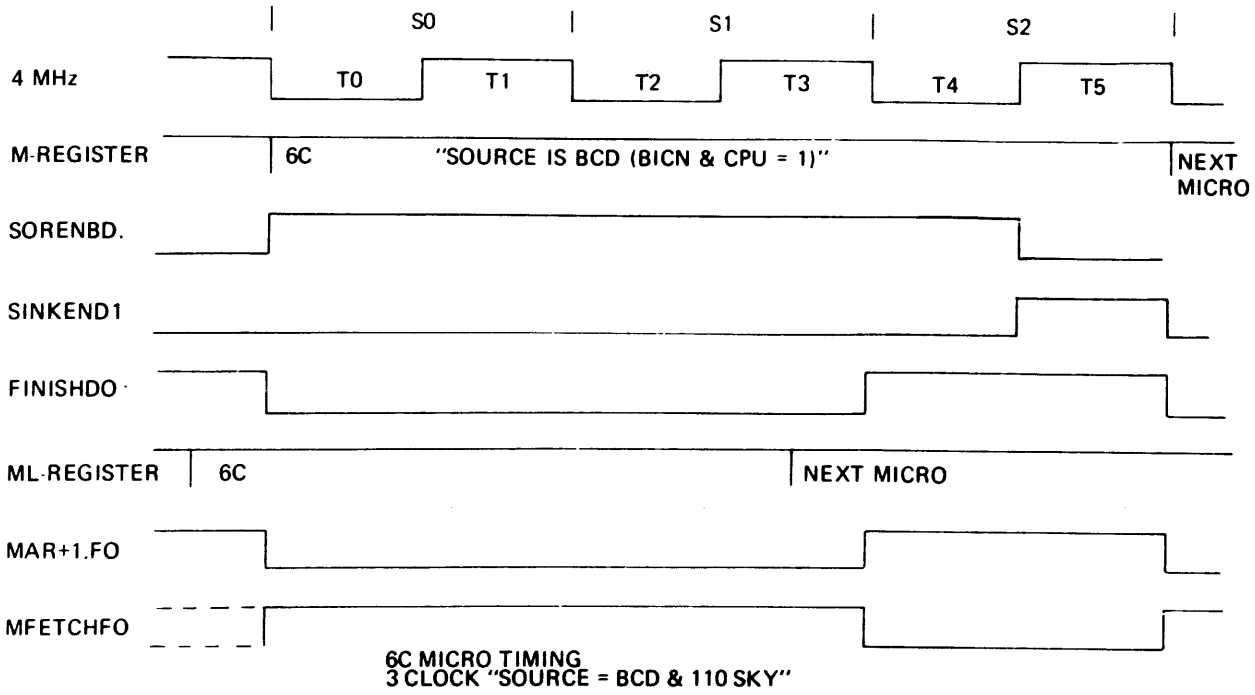


Fig. II-143 6C MICRO TIMING 3 CLOCK "SOURCE = BCD AND NO SKIP"

4 CLOCK EXECUTION

A 4 clock execution is shown in Figure II-144. When the Skip of the next upcoming Micro is executed, the SKIP . . F. F/F is set thus disabling the contents of the ML-Register from being set in the M-Register. The 4-Bit Function Box on Card B (6-6) compares the 4-Bit Source Register with the 4-Bit Mask (MOP Bits 03 thru 00). The results of this compare is again compared with the Skip test Variant Bit compare indicates a Skip, the level SKIP . . C0 is true (Card C (4-4)). SKIP . . C0 will cause the SKIP . . F. F/F to set with the trailing edge of the inverted 4 MHz clock (SCPMY/F.). SKIP . . F. disables MLENBLFO from occuring when FINISHDO is true, thus zeros are gated to the M-Register for execution. Note that MLENBLFO is the read enable fro the ML-Register. MAR+1 . F0 occurs without interruption as well as concurrent MFETCH operations. The Micro executed after the Machine or pseudo NO-OP is the Next in-line Micro which follows the Next Micro. For example, if the string of Micros in S-Memory were the 6C, 1C, 3C, & 7C, the Micro executed would be the 6C, a 2 clock Machine NO-OP in place of the 1C, and then the 3C, 7C etc.

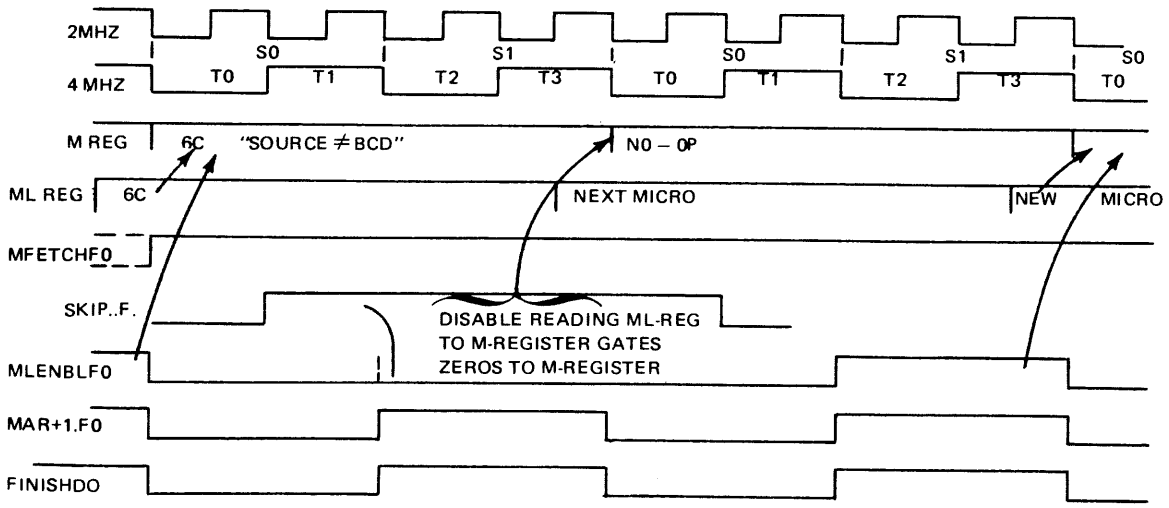


Fig. II-144 6C MICRO TIMING 4 CLOCKS (SOURCE AND BCD AND SKIP)

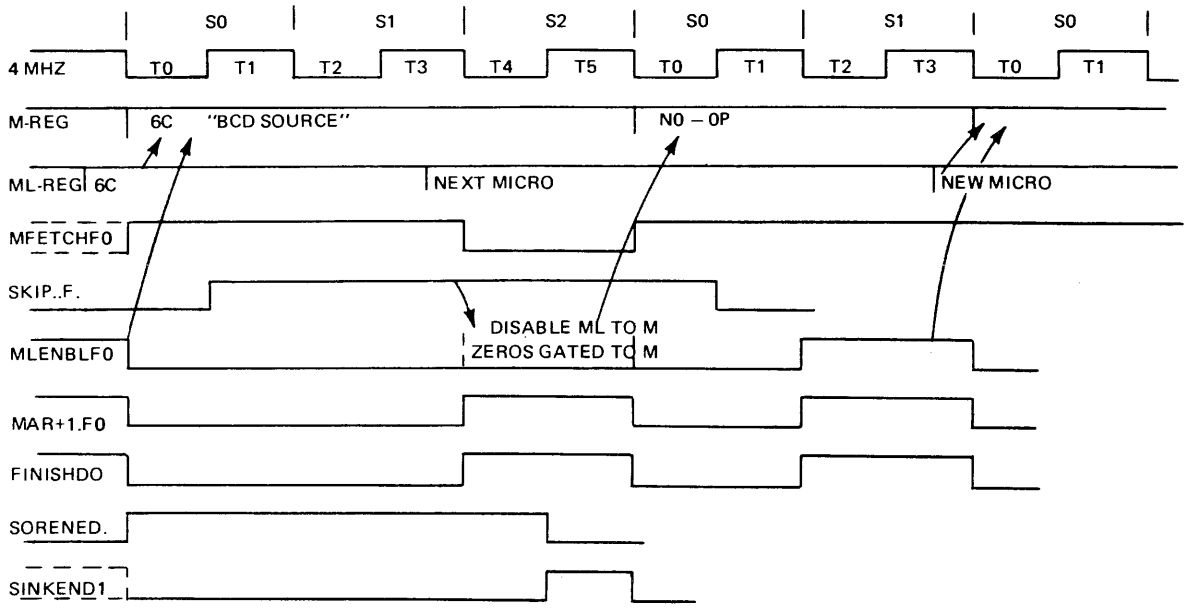


Fig. II-145 6C MICRO TIMING 5 CLOCKS (SOURCE = BCD AND SKIP)

5 CLOCK EXECUTION

When BCD is source and extra clock is required (see Figure II-145) refer to 3 clock execution for details. The SKIP . . R. F/F set indicates the next upcoming Micro is not to be executed. SKIP . . F. is set and reset with the inversion of the 4 MHz clock (SCPM4/F .). A 2 clock NO-OP is forced as SKIP . . F. true disables MLENBLFO thus disabling the "reading" of the ML-Register during FINISHDO time. Zeros are set in the M-Register. An MFETCH operation occurs during the 2 clock NO-OP at which time the next Micro is fetched and latched in to the ML-Register.

7C MICRO

The function of the 7C Micro is to read out of or write into S-Memory. The execution of the 7C Micro also provides incrementing and/or decrementing the FA and/or FL Register. One of 4 registers is permissable as data source (when writing into S-Memory) or as sink register (when reading S-Memory). These registers are the X, Y, T or L Registers. Up to 24 Bits of Data can be effectively read from or written into S-Memory. Note that a 32-Bit Read and/or Write will always occur; however, only up to 24 bits of this data will actually be affected by the 7C MIcro. Refer to S-Memory Explanation for details. Mop Bit 5 provides designating the transfer width sign. If = to zero, then Memory is accessed in a positive direction from the Bit address. If = to one, then access is in a negative direction.

The execution time of the 7C Micro is 8 clock periods. Refer to S-Memory Explanation for details pertaining to the actual Memory cycle.

READ MEMORY FUNCTIONAL DETAIL

As 8 clock periods are required to execute the 7C Micro, Figures II-146 throu II-152 illustrate the Basic functions which occur during S0 through S7 times. They are defined as follows:

S0 TIME

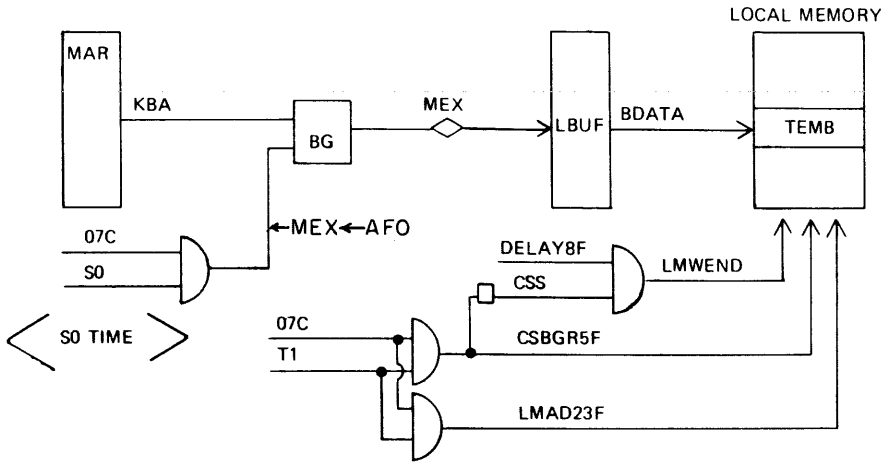
The MAR(A) address is pointing to the address of the next upcoming Micro from S-Memory which will be executed in the M-Register when the 7C Micro finishes. During S0 and S1 time a concurrent MFETCH operation will occur which will cause this next Micro to be executed to be latched in the ML-Register. As the function of the 7C Micro is to read S-Memory, the MAR(A) register will be used to address the location in S-Memory where the read will occur. Therefore the current MAR(A) address is stored in TEMB during the read S-Memory cycle. Figure II-146 illustrates the data flow path for storing the MAR(A) address in TEMB. During S0 time MAR(A) is gated to the MEX and set in LBUF at the trailing edge of the inverted 4MHz clock (CLK4/.K0) at T1 time when the 8 MHz clock pulse (DELAY8F.) is true, the contents of LBUF is written into TEMB.

S1 AND S2 TIME

Refer to Figure II-146 and II-147. The address in S-Memory where the Read will occur is in FA. The address is gated through the Function Box to MAR(A) as well as S4 time. The FA address is gated to the Function Box as well as the Lit or C Reg Valve at T2 and T3 and T4 time. The Binary Sum is gated to the Main Exchange and set in LBUF. LMWE . . F0 will occur at T5 time when CSSINKF1 is true. This stores the incremented or decremented value of FA back in FA.

S3 TIME

A Mask is generated which is determined by the Literal or C Register Bits 00-04 if the Lit is equal to zero. MASKSTC0 is true at S3 time thus causing the MIR Register to be in the J-K Mode. If a Mask Bit is true, the Bit is set in MIR at S3 time.



√ Fig. II-146

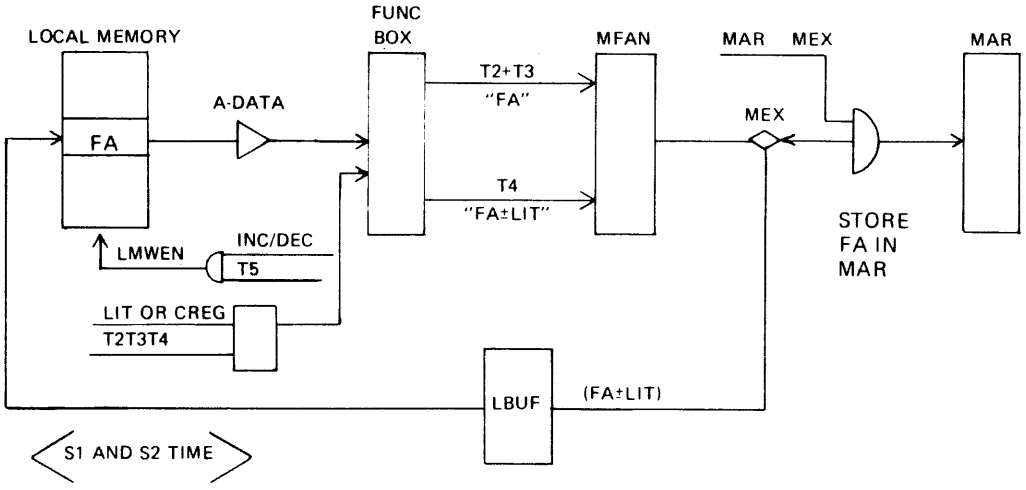


Fig. II-147 S1 AND S2

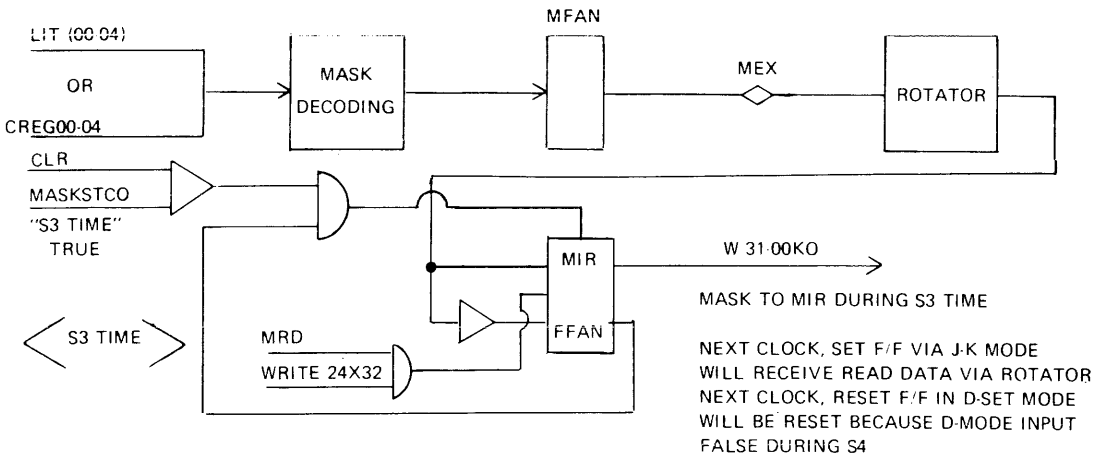


Fig. II-148 7C MICRO (READ) S3 TIME

S4 TIME

Read Data is available at S4 time and a bit will be set in MIR if the corresponding MASK Bit during S3 time was a one. TEMB is sourced and gated to the Main Exchange at S4 time. As the Memory Read operation is complete, the address of the next Micro to be executed which was stored in TEMB at S0 time is gated back to MAR(A).

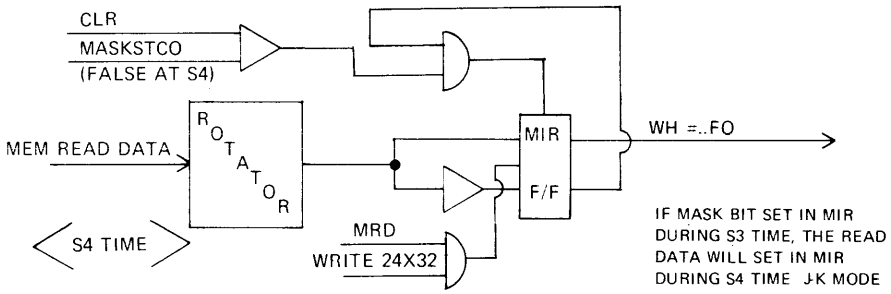


Fig. II-149 MASK BIT S4 TIME

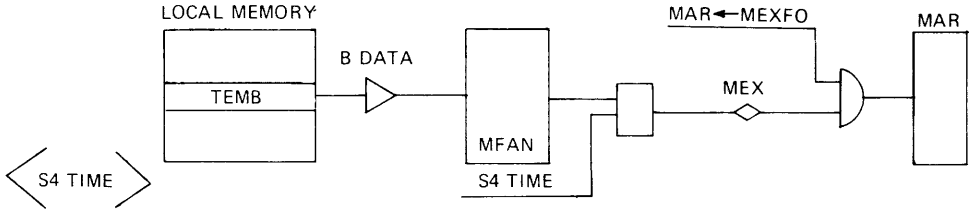


Fig. II-150 7C MICRO (READ) S4 TIME

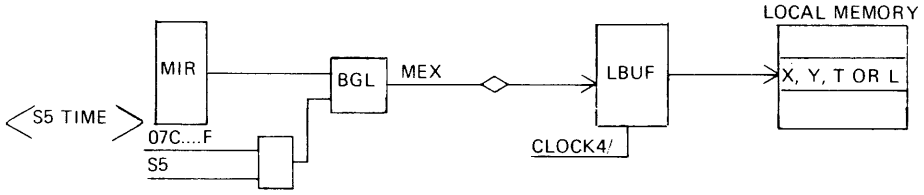


Fig. II-151 7C MICRO (READ) S5 TIME

S5 TIME

The read data in MIR is sourced and gated to LBUF prior to being set in the sink register selected (enter X, Y, T or L). The write into Local Memory occurs at T11 time.

S6 AND S7 TIME

The value of FB is gated through the Function Box with the Lit or C-Register valve at T12-T14 time. The sum or difference is set back in FB via the MEX to LBUF.

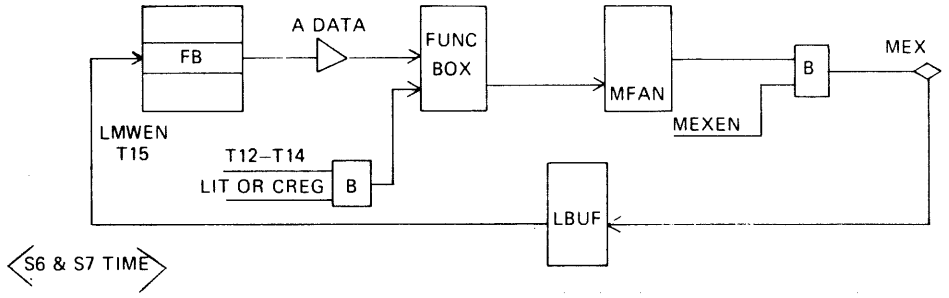
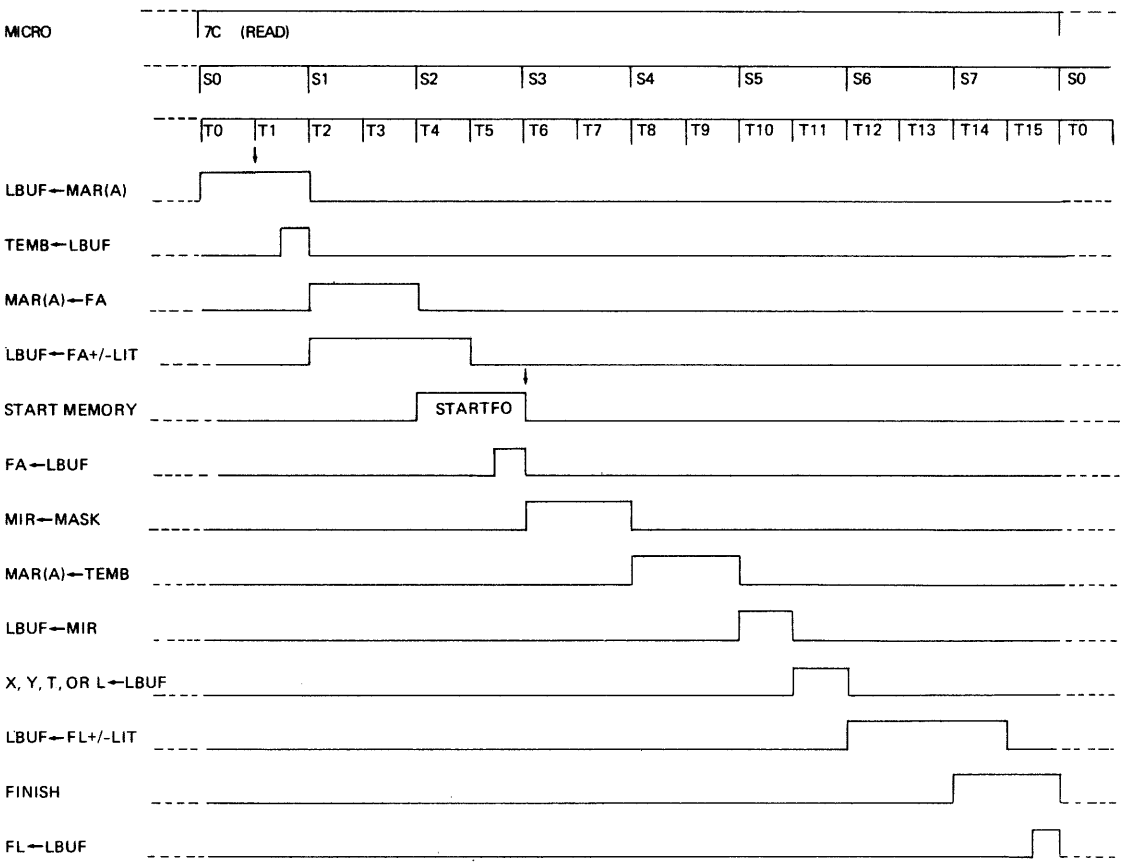


Fig. II-152 7C MICRO (READ) S6 AND S7 TIME

READ TIMING "BASIC FUNCTION"

Figure II-153 illustrates the primary functions which occur at the various S & T times. Note the S-Memory cycle is started at the beginning of S3 time, and the read data is available at approximately T9 time.



√ Fig. II-153 READ TIMING BASIC FUNCTION

Functional Detail

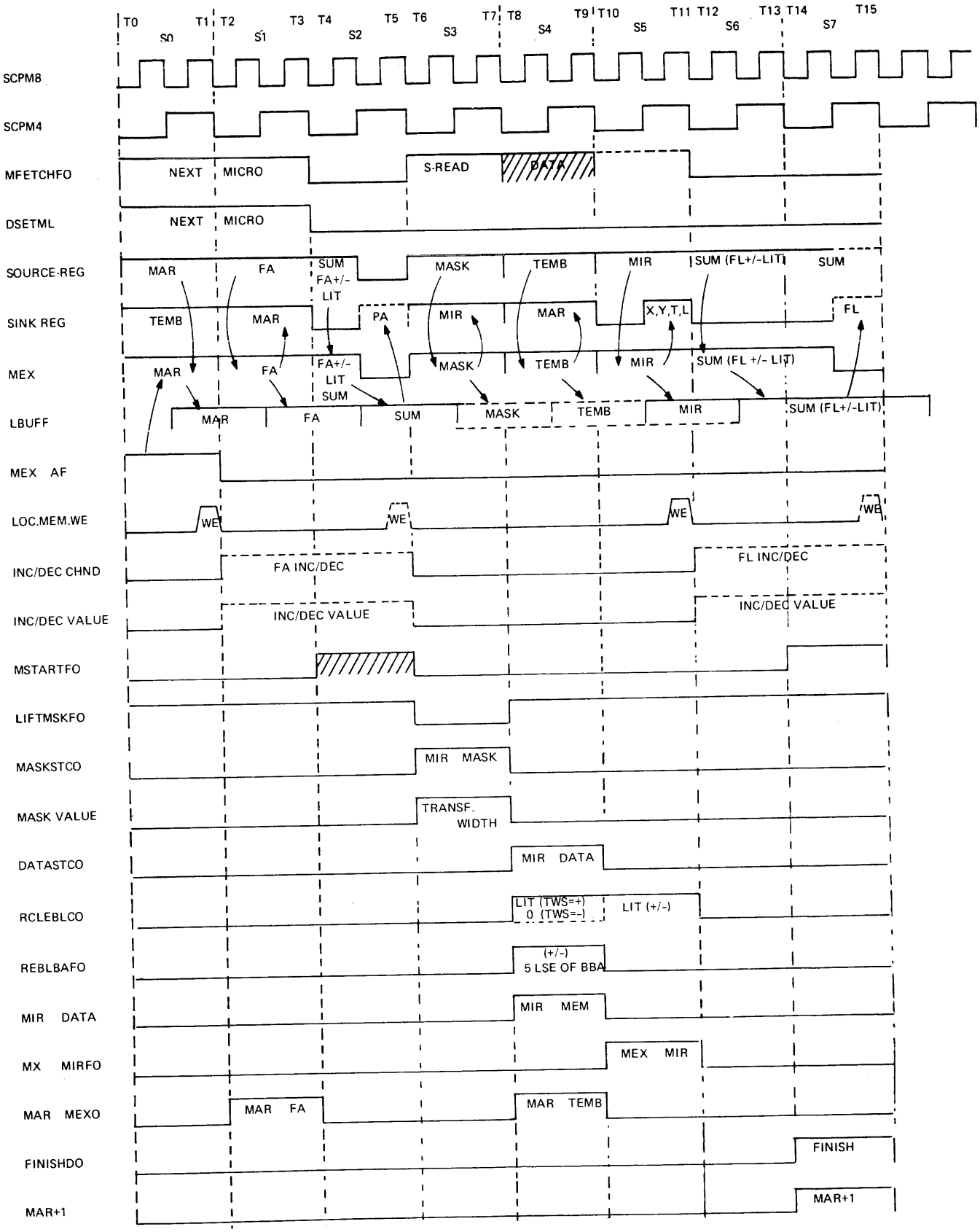


Fig. II-154 7C MICRO READ (OCTAIL TIMING)

READ TIMING "DETAILED"

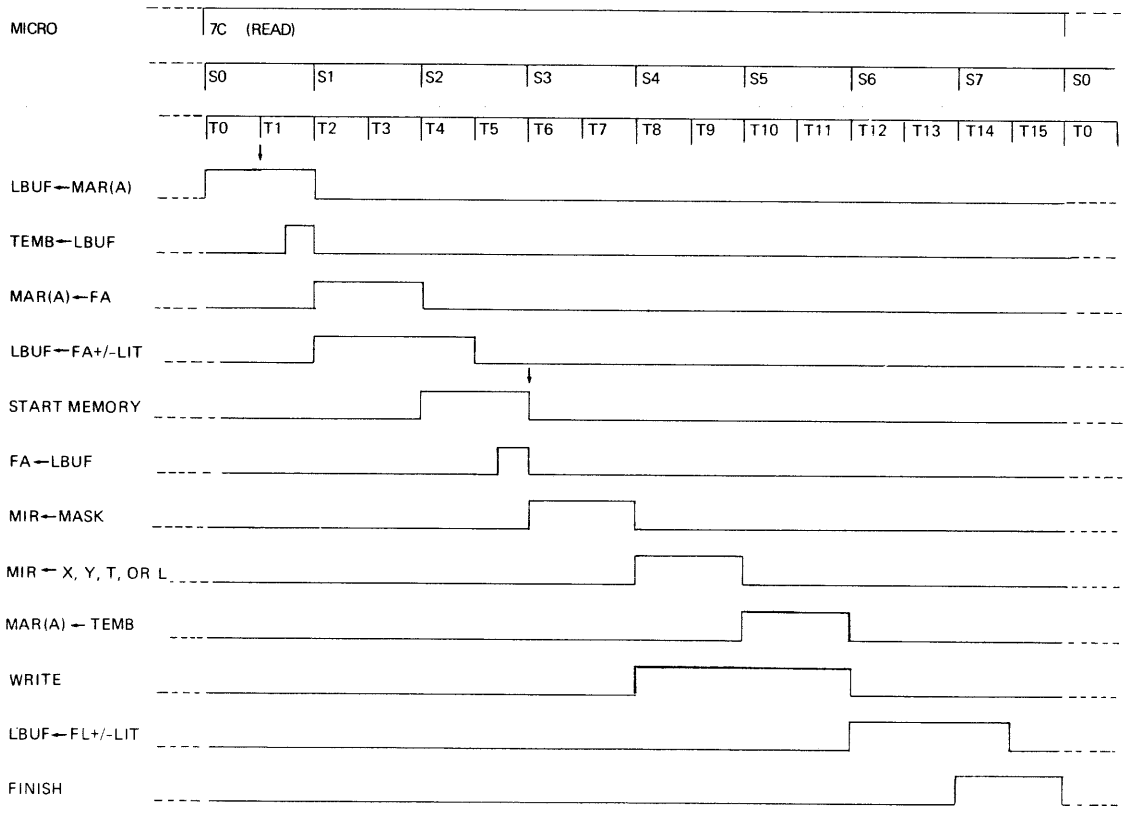
Figure II-154 illustrates the contents of the various Registers at each T & S time as well as some of the control levels which control the actual S Memory Read cycle at S3 and S4 times. The arrows indicate data movements.

7C MICRO WRITE TIMING

The overall timing of the write memory operation is similar to a read memory operation with the following exceptions:

Figure II-155 illustrates the Basic data plan of the 7C Write Memory operation. During S4 time the write data in either S, Y, T or L is sourced and gated to MIR. As during a read cycle, a Mask is set in MIR at S3 time. If a bit in the Mask is set, the corresponding bit of write data from the rotator will be set in MIR. If the bit in the Mask was not set, then the memory read data is set in MIR. Note that 32 bits will be read and 32 bits will be written.

The MAR(A) address of the next Micro to be executed that is stored in TEMB during S0 time is gated back to MAR(A) at S5 time.



√ Fig. II-155

Functional Detail

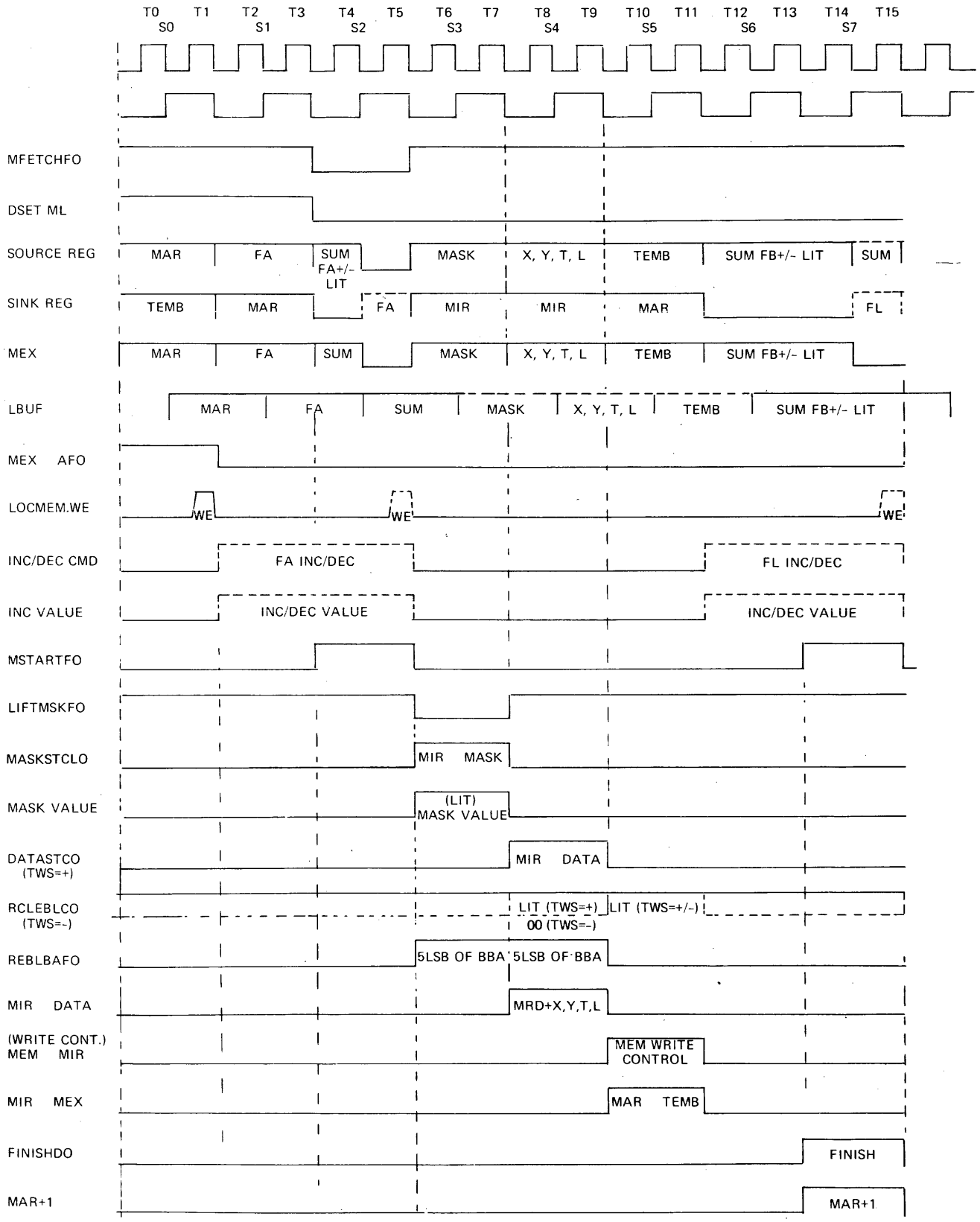


Fig. II-156

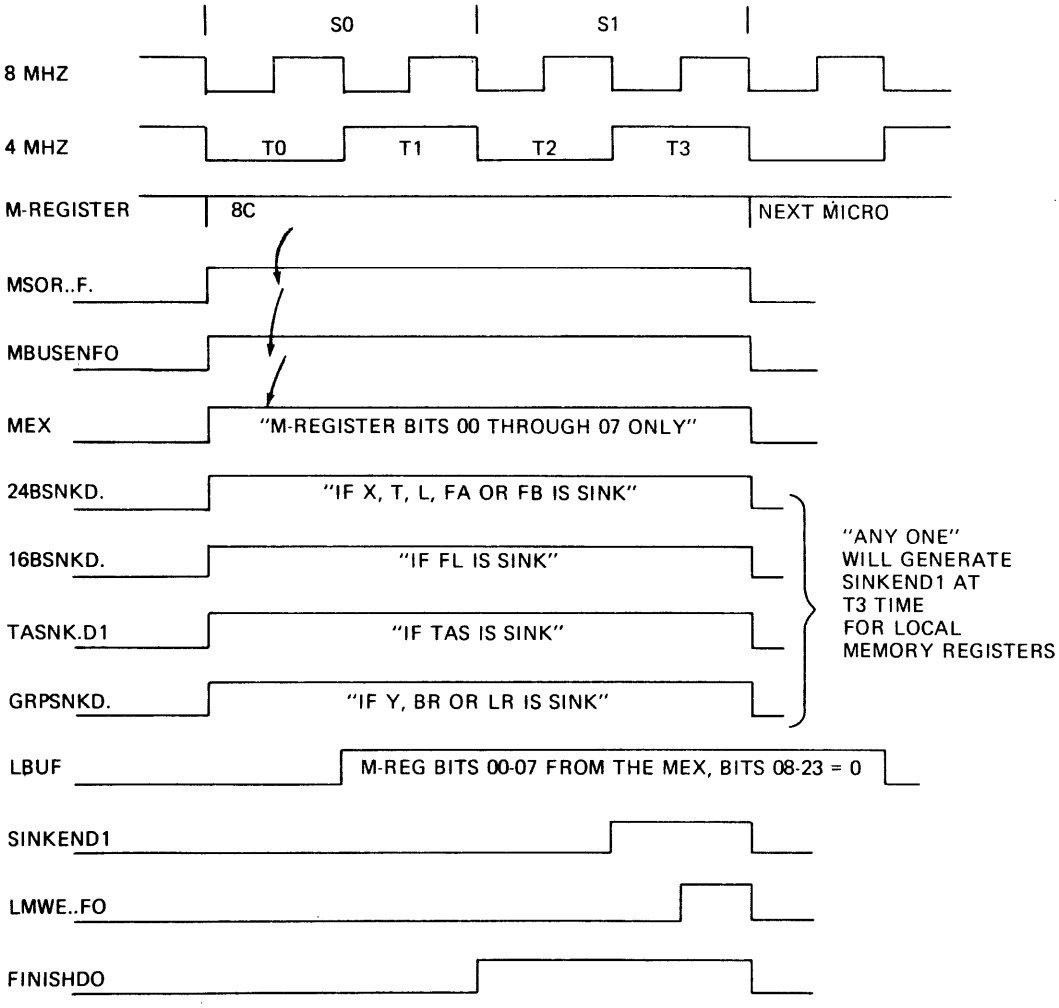
Figure II-156 illustrates the contents of the various registers at the various S and T times. With the exception of the actual Memory cycle the timing is similar to that of a read cycle.

8C MICRO

The function of the 8C Micro is to move the 8LSB of the Micro (8-Bit Literal) to a sink register. Regardless of the Sink Register selected the Literal transfer is from the M-Register Bits 00-07 to the Main 24-Bit Exchanges in Bits 00-07 to the Sink Register. When a register in Local Memory is selected, the MEX is gated to LBUF prior to being written in the Register in Local Memory. The MSB of the MEX will contain zeroes. The 8C Micro requires 2 clock periods for execution with the additional 2 clocks if MAR(A) is sink.

2 CLOCK EXECUTION

The 8C Micro when in the M-Register and exposed for execution will generate MSOR . . F. and MBUSENFO. Refer to Figure II-157 which will allow gating the M-Register Bits 00-07 to the Main Exchange Bits 00-07 respectively. Depending on the Sink Register selected either 24BSNKD. 16BSNKD., TASNK .D4, GRPSNKD. or CPSINKC. will be true. The first 4 levels cause SINKEND1 to be true at T3 time and designate a register with in Local Memory is selected as sink. CPSINKC. will cause the C-Register Bits 00-07 to be enabled thus allowing the contents of the MEX to be set in the C-Register with the trailing edge of the 4MHz clock.



√ Fig. II-157 8C MICRO 2 CLOCK EXECUTION

4 CLOCK EXECUTION - Refer to Figure II-158

The 8C Micro when executed will cause the 8 Bit Literal (M-Register Bits 00-07) to be gated to the Main Exchange (Bits 00-07) to be gated to the Main Exchange (Bits 00-07 respectively). With MAR(A) selected as sink ASINK. . F. is true thus disabling MLENBFLO and MAR+1. FO from occurring when FINISHDO is true. With MLENBLFO false when FINISHDO occurs a machine or pseudo NO-OP is set in the M-Register for execution. ASINK. . F. and FINISHDO true, MAR(A) is in the D-Set Mode and will receive the contents of the Main 24-Bit Exchange at the trailing edge of T3 time. An MFETCH operation is initiated at T0 time of the NO-OP to fetch the new Micro gated at the MAR(A) address specified by the Literal value of the 8C Micro. This Micro when fetched is latched in the ML-Register and gated to the M-Register for execution when the pseudo NO-OP finishes.

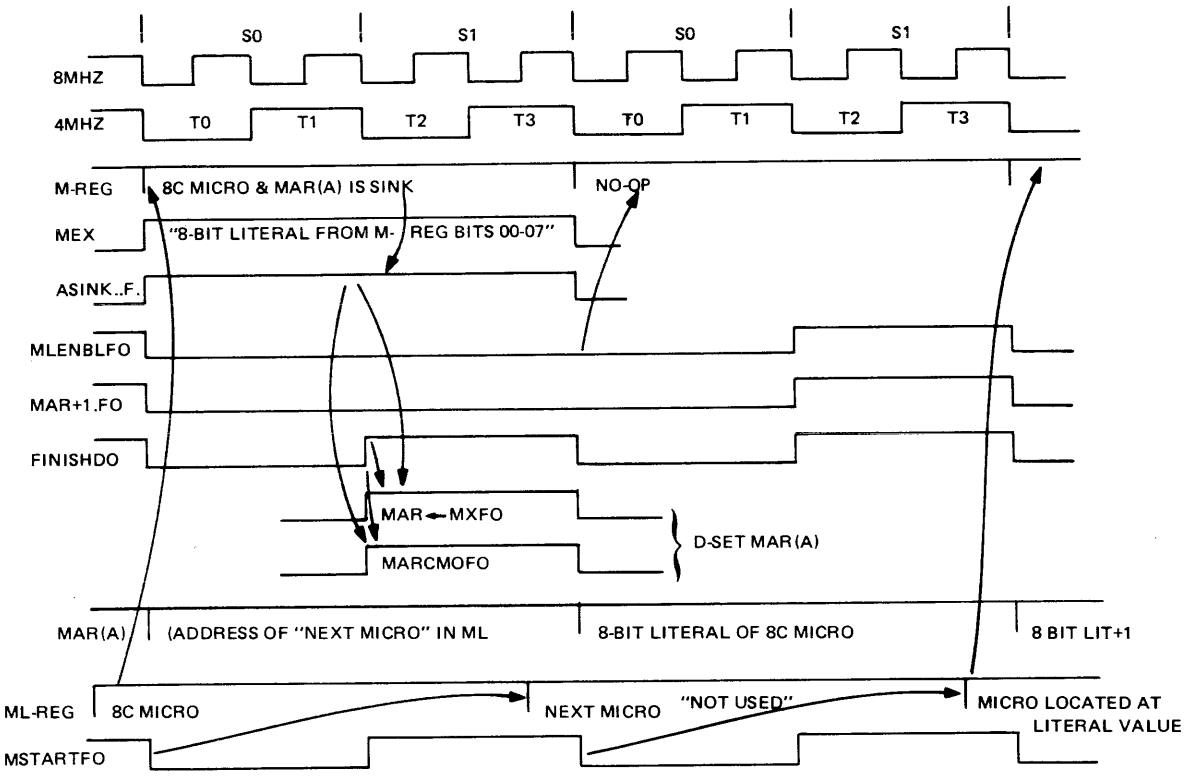


Fig. II-158 8C MICRO & SINK IS MAR(A)

9C MICRO

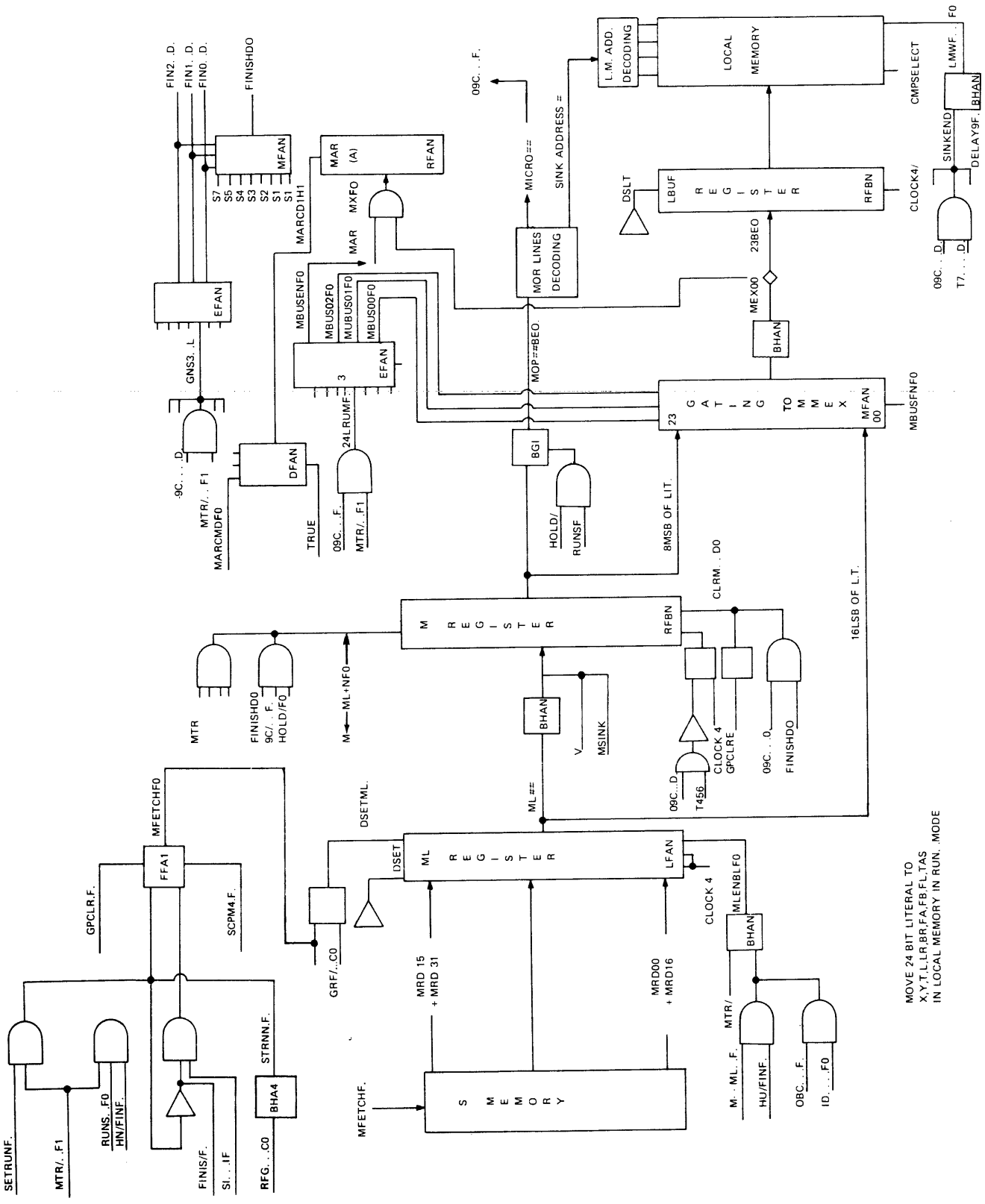
The function of the 9C Micro is to Move a 24-Bit Literal to a Sink Register. Only the RUN or Step Mode is considered at this time. Refer to Cassette Logic timing for the execution of the 9C in MTR Mode.

The 24-bit literal consist of the 8-Bit literal portion of the 9C Micro (MOP Bits 07-00) as the MSB of the 24-Bit literal and the next upcoming 16 bits from S-Memory as the 16 LSB of the 24-Bit Literal. The execution time is 6 clock periods regardless of sink selected.

FUNCTIONAL DETAIL

The 9C Micro is read from S-Memory during a MFETCH operation latched in the ML-Register and set in the M-Register. Refer to Figure II-159. When the 9C is set in the M-Register another MFETCH operation is initiated to read the 16 LSB of the literal from S-Memory. the 16 LSB of the literal are latched in the ML-Register but are not set in the M-Register. When the 24-Bit Literal is assembled in the M and ML-Register, the literal is gated to the Main 24-Bit Exchange.

Functional Detail



√ Fig. II-159 9C MICRO EXECUTION PATH

LOCAL MEMORY IS SINK

When the sink register is located in Local Memory, the literal on the MEX is gated to LBUF prior to being written in Local Memory. When MAR(A) is the sink Register, the MEX is gated directly to MAR(A). See Figure II-160.

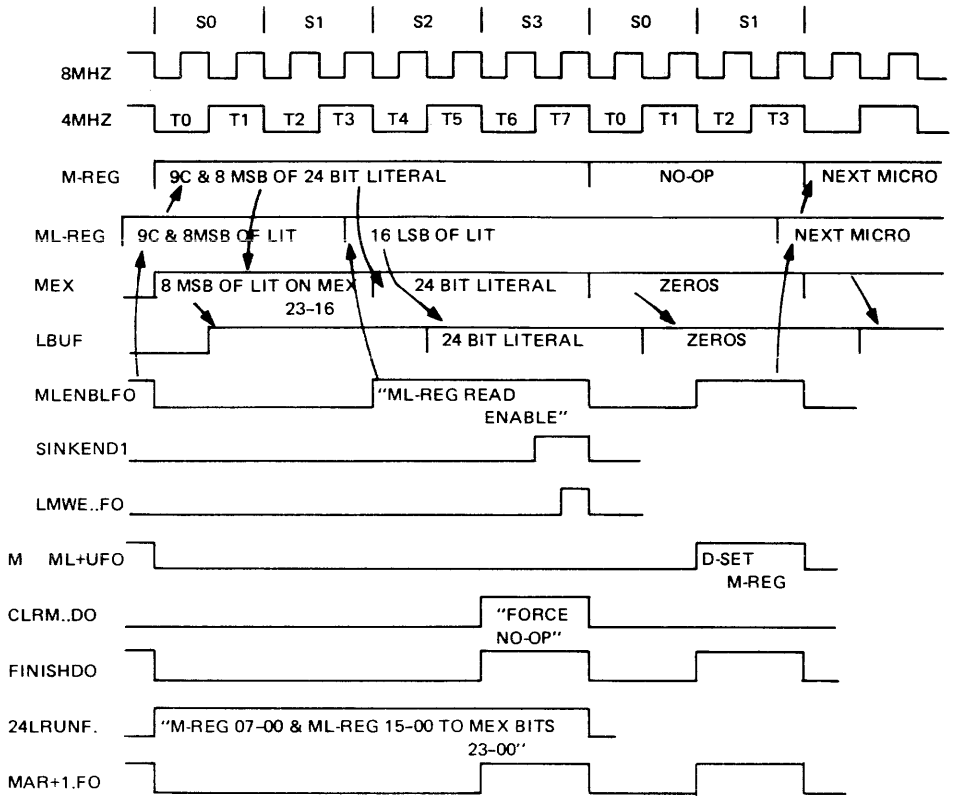


Fig. II-160 9C MICRO TIMING LOCAL MEMORY IS SINK

LOCAL MEMORY REG IS SINK

During S0 through S3 time, the 9C Micro including the 8MSB of the literal is held in the M-Register. 24LRUNF. is true during this time and gates the M-Register (Bits 07-00) to the MEX 9 Bits 23-16) and the ML-Register (Bits 15-00) to the MEX (Bits 15-00). A MFETCH operation is initiated at T0 time to fetch the 16 LSB of the Literal are latched in the ML-Register. MLENBLFO is true at TD time and provides reading the contents of the ML-Register Thus at T4 through T7 time the 24-Bit literal is on the MEX. SINKEND1 occurs at T7; thus the local Memory Register is addressed and a write will occur when LMWE. . FOR is true. CLRM. . DO occurs when FINISHDO is true; thus the M-Register is cleared and a machine NO-OP is forced. During the time the NO-OP is executed a MFETCH occurs to fetch the next Micro to be executed.

MAR(A) IS SINK

When MAR(A) is sink, generally speaking the same functions occur as when a Local Memory Register is Sink with the exception that MAR+1. F0 is disabled when the 9C Micro finishes and MAR(A) is put in the D-Set mode at Finish time; thus the new address (24-Bit Literal) is set in MAR(A). See Figure II-161.

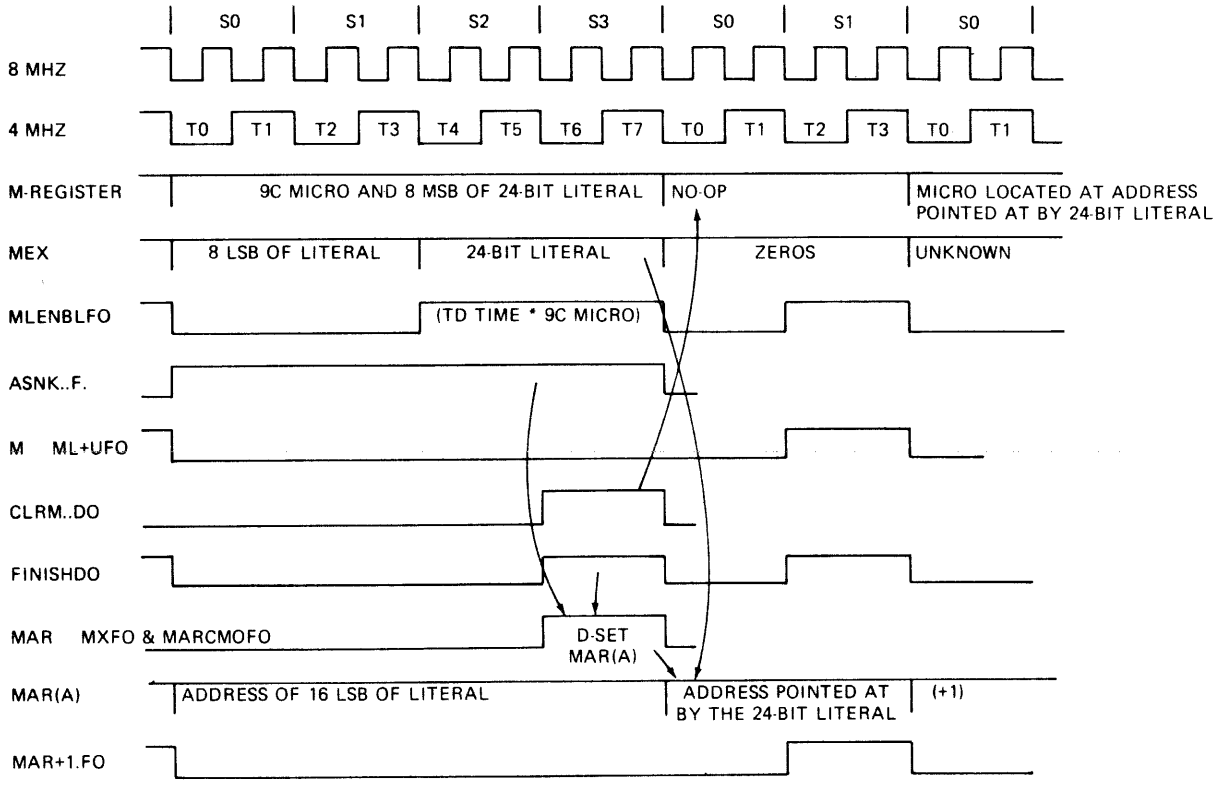


Fig. II-161 9C MICRO TIMING MAR(A) IS SING

10C MICRO

The function of the 10C Micro is to either Shift or Rotate the T-Register left by the number of bits specified by the Shift/Rotate Count (MOP Bits 00 thru 04). The contents of the T-Register is not changed unless it is designated as the Sink Register. Data is right justified and truncated from the left of the sink register is less than the source register The Shift operation causes zeros to fill on the right and data to be truncated on the left.

The basic execution time is 3 clocks. If MAR(A) is sink the execution time is 5 clocks.

3 CLOCK EXECUTION – ROTATE

A Mask of 24 Bits is generated when the 10C Micro is executed and Rotate T is designated. Refer to Figure II-162. The Mask is gated to the MEX, thru the Rotator (No Rotation) and to MIR at S0 time. The T-Register is then sourced in Local Memory and gated to the MEX. The MEX is then gated to the Rotator where the T-Register is Rotated by the 24s compliment of the Literal value of the Micro if ≠ zero. If the Literal = zero, then the rotation amount is the 24s compliment of the value of CPL. The Rotated value of the T-Register is set in MIR (Bits 08 thru 31) at S1 time. Note the Mask is set to 24, therefore the 24 rotated Bits of T is set in MIR. At S2 time MIR is sourced and the contents is gated to the MEX. Depending on the Sink Register selected the MEX is then gated to either a discrete register or to a register within Local Memory.

If the M-Register is sink then the rotated data is Bit OR-ed with the next Micro from the ML-Register.

3 CLOCK EXECUTION – SHIFT

The Shift operation will cause essentially the same data flow to occur as a rotate operation with the following exceptions. Refer to Figure II-162.

1. The Mask Length is determined by the complement of the Literal (MOP Bits 00 thru 64) if ≠ zero or the CPL value if the Literal = zero.
2. The Mask is rotated and the amount of rotation is determined by the complement of the Literal if ≠ 0 or the value of CPL if the Literal = 0.

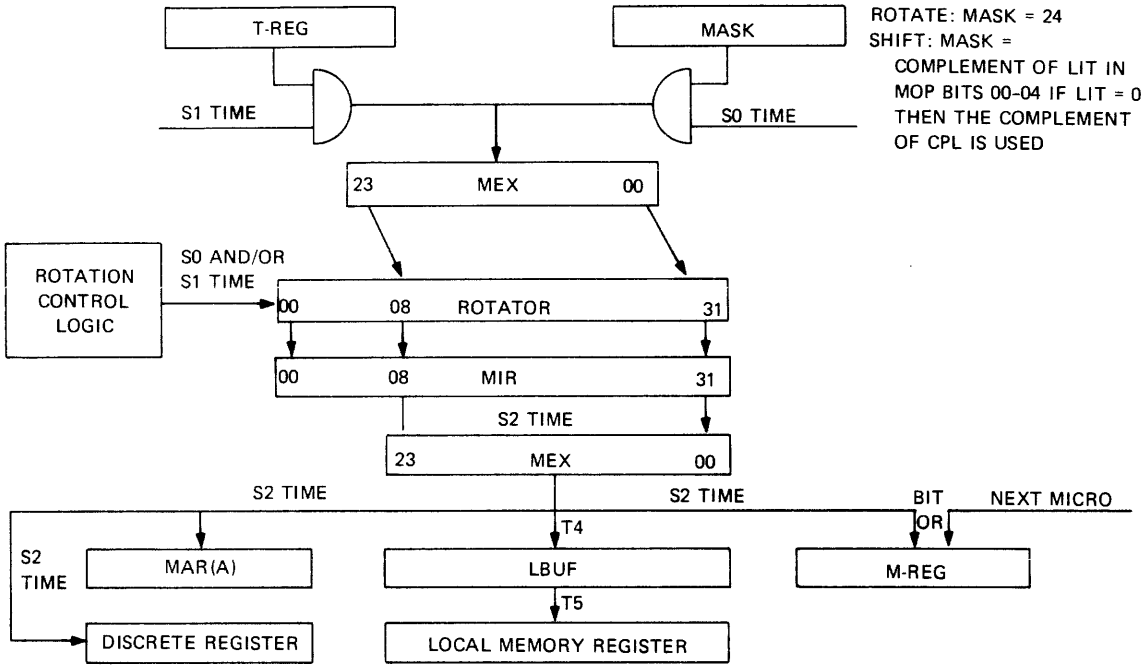


Fig. II-162 10C MICRO DATA FLOW

3 CLOCK EXECUTION – SINK REGISTER IS NOT MAR(A)

When the Sink Register is not MAR(A), the sequence for the execution of the 10C Micro is as follows: (Refer to Figure II-163.

S0 Time

MASKSTCO is true as a result of decoding the 11C Micro. At S0 time, it enables generating the Mask and allows the Mask to be set in MIR. Note the Mask is generated in the Mask generation and gated to the MEX. The MEX is then gated to the Rotator and the Rotator to MIR.

S1 Time

DATASTCO is true which allows the T-Register Data to be set in MIR. The T-Register Data is gated first to the MEX as the address and chip select levels (LAMDD1F0 and CSAGP. F1) which point to the T-Register are true at S1 time. CSAGP. F1 generates CSAGP A-F D0 thur all 24 Bits of T are sourced. The MEX is gated to the Rotator where the T-Register Data is Rotated by the 24x complement of the Lit if $\neq 0$ or the complement of CPL if the Lit = 0.

S2 Time

MIR is sourced and gated to the MEX. If the Sink Register is in Local Memory, SINKEND. will be true at T5 time, therefore generating a write into the Local Memory selected as sink when LMWE. . F0 is true. MSINK. F0 is true if the M-Register is sink. CC MEXD1 is true if the four Bit CC-Register is sink. Similar levels will be true at S2 time if another discrete register is selected as sink. FINISHDO occurs at S2 time thus the next Micro is set in the M-Register at the trailing edge of T5 time.

MFETCHF0 is reset during S2 time to disable the D-Set Mode of the ML-Register

5 CLOCK EXECUTION (SIN IS MAR(A))

With respect to the function of the 10C Micro, the 5 clock exeuction when MAR(A) is sink is identical to that of the 3 clock execution when any other register selected is sink with the following exceptions. See Figure II-164.

MAR(A) designated as sink generates the level ASNK. . F. which prevents MLENBLFO from occuring when FINISHDO is true. MLENBLFO when true, allows reading the next up-coming Micro (stored in the ML-Register) to the M-REgister with MLENBLFO false a Machine or pseudo NO-OP is forced. During the execution of the NO-OP, the new Micro located at the address specified by the Shift-Rotate T-Register Data is fetched from S-Memory.

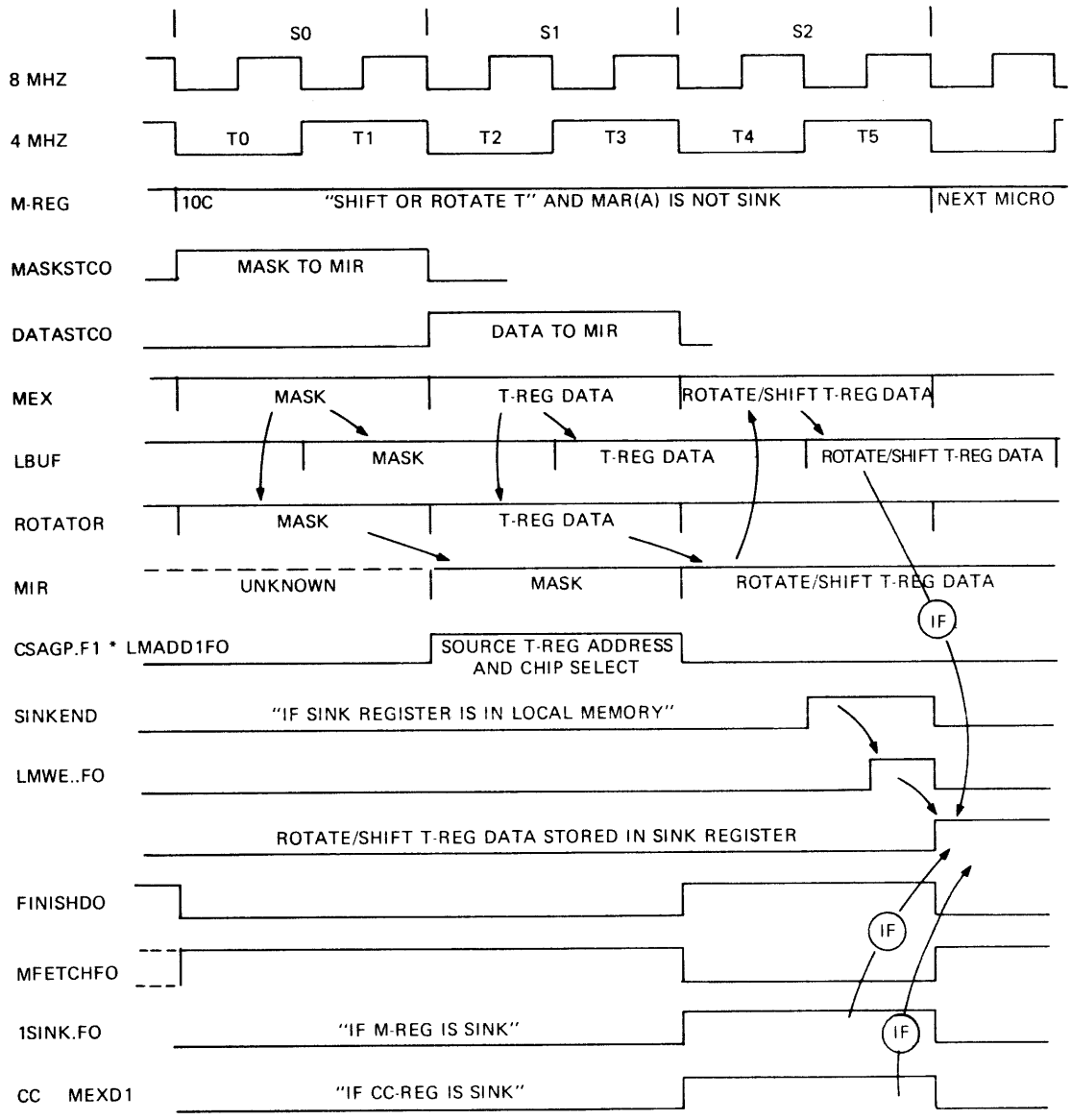


Fig. II-163 10C MICRO TIMING 3 CLOCK EXECUTION

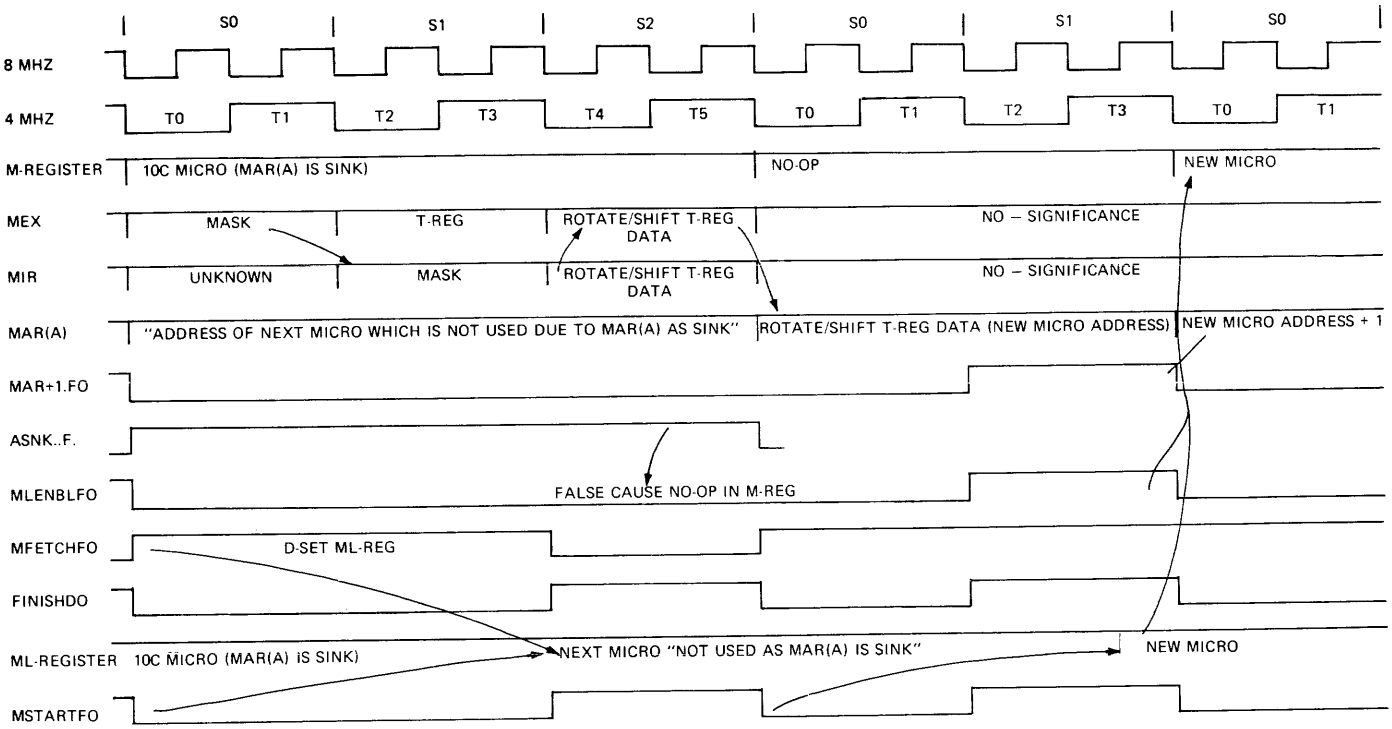


Fig. II-164 10C MICRO 5 CLOCK EXECUTION

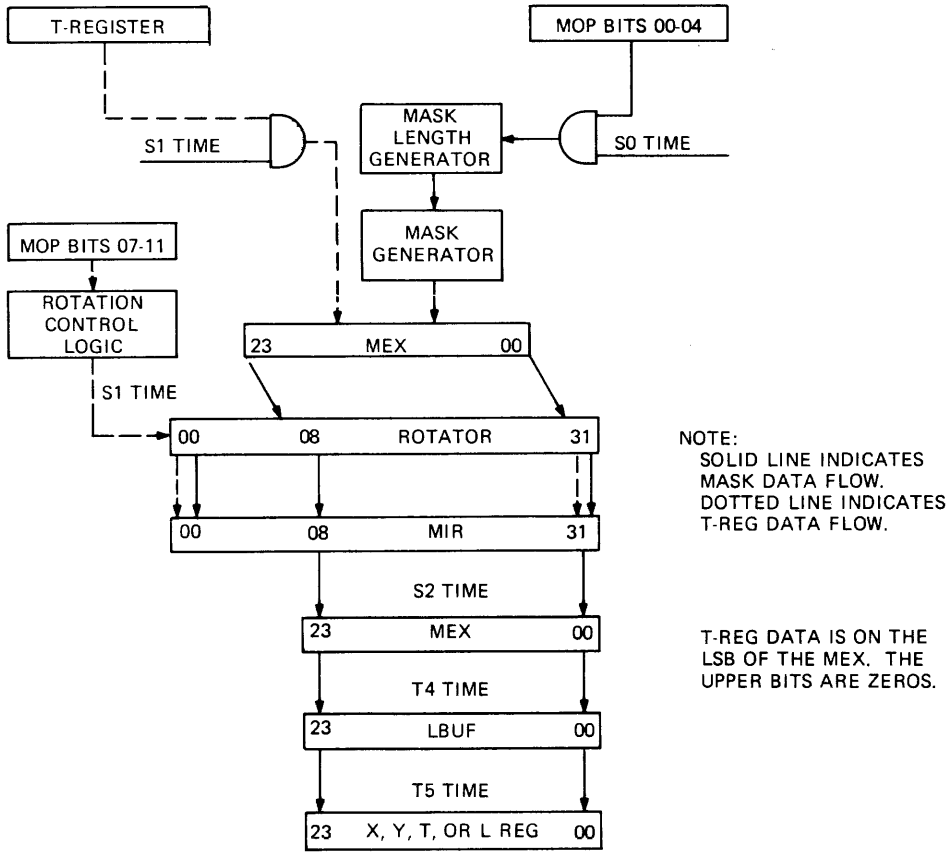


Fig. II-165 11C MICRO DATA FLOW 3 CLOCK EXECUTION

11C MICRO

The function of the 11C Micro is to rotate the T-Register left by the number of bits specified by the Right Bit Pointer (MOP Bits 07 thru 11) and extract the number of bits specified by the Extraction Field Length (MOP Bits 04 thru 00). The value of the T-Register is not changed unless it is also the sink register. The execution time is 3 clock periods.

FUNCTION DETAIL

The Block Diagram in Figure II-165 illustrates the data flow for the 11C Micro. MOP Bits 00 thru 04 provide the extraction field length which is applied to the Length Mask Generator. The output of the Mask Length generated enable the Mask Generator to produce a Mask Bit for each Bit to be extracted. 24 MFANS are used to gate the Mask Bits to the Main Exchange. Each Mask Bit on the Main Exchange represents the data field length of the amount of the T-Register to be extracted. If the Mask is less than 24 bits, the Mask Bits will be right justified with zeros filling the upper Bits of the MEX (Bits 23, 22 - etc.). The MEX Bits 23 thru 00 are then gated to the Rotator Bits 08 thru 31 respectively and set in MIR (Bits 08 thru 31).

The T-Register is then sourced and gated to the MEX. The MEX is then gated to the Rotator. The T-Register's contents is rotated so that the Bit of the T-Register pointed at by the Right Bit Pointer (MOP Bits 07 thru 11) is at the output Bit position of the Rotator indicated as the 31st Bit. The output of the Rotator is then set into MIR. Note that only the Bit positions of MIR that were set by Mask Bits will be set to the value of the T-Register. In summary, MIR will contain only the Number Bits of the T-Register designated by the extraction field length and pointed at by the Right Bit Pointer. MIR is then gated to the MEX with the LSB of the MEX containing the T-Register data extracted. The MEX is then set into LBUF and written in the Local Memory register selected as sink.

3 CLOCK EXECUTION

S0 Time

The 11C Micro when executed in the M-Register, will generate MASK STCO. Refer to Figure II-166. MASK STCO true will allow the "Mask", which is generated by decoding MOP Bits 00 thru 04, to be gated to the MEX. MASK STCO also causes MIR to be in the J-K Mode thus able to receive the Mask from the MEX via the Rotator. MASKSTCO is also anded with CLK4. . CO as the clock to the MIR Flip-Flops. MIR receives the MASK at the trailing edge of S0 time.

S1 Time

SORENBD. is normally true thus enabling sourcing the T-Register in Local Memory when the T-Register address (LMADD1TO) and Chip Select Levels (CASGP A-FDO) are true. The contents of the T-Register is gated to the MEX and to the Rotator. At the trailing edge of S1 time, the rotated T-Register data is set in MIR.

S2 Time

MIR is sourced and gated to the MEX. The trailing edge of the inverted 4 MHz clock (CLK4/.D0), which is true at T4 time, sets the MEX data in LBUF. CSSINKF1 is true at T5 which causes LMWE. . F0 causes the data in LBUF to be written into the sink register selected.

123C MICRO

The function of the 123C Micro is to either subtract from or add to the address of the Next Micro in MAR(A) the value of the 12 LSBs of the Micro held in the M-Register. MOP Bit 12 determines whether an add or subtract will occur. The 12 LSBs of the Micro held in the M-Register represent the Relative Displacement Magnitude. The Execution time is 4 clock periods: (a) 2 clocks for the 123C Micro and (b) 2 clocks for a Machine or pseudo NO-OP.

During the execution of the pseudo NO-OP, the Micro located at the "Branch" address is fetched.

THEORY OF OPERATION

The Block Diagram in Figure II-167 shows the data paths for the 123 Micro. The 12 LSB of the Micro (MOP bits 00-11) are gated to the MEX (bits 04-15 respectively) via 12 Multiplexor chips. The MEX (bits 04-18) are gated to the Inputs of the MAR(A) register (bits 04-18 respectively). At S1 time either ADDMARF. or SUBTR. F. will be true and the trailing edge of the next clock will increment or decrement MAR(A) by the value of MOP Bits 00-11 which are at the inputs of the MAR(A) register (bits 04-15).

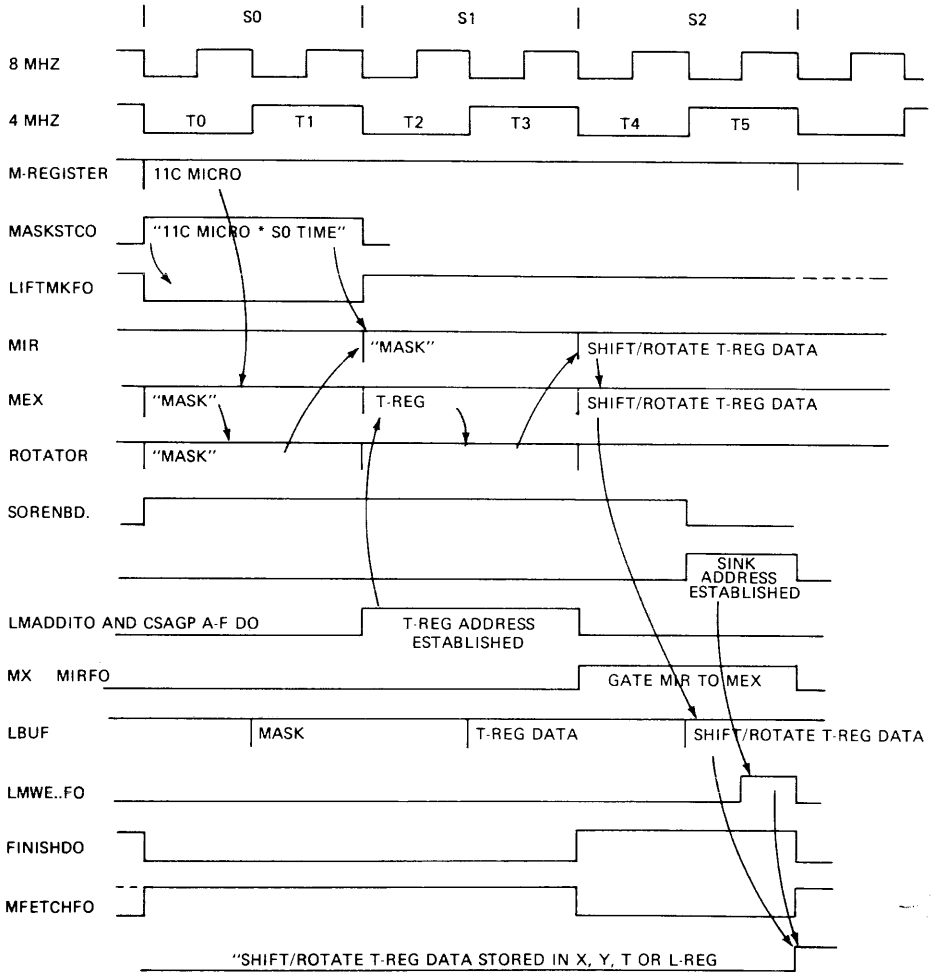


Fig. II-166 11C TIMING 3 CLOCK EXECUTION

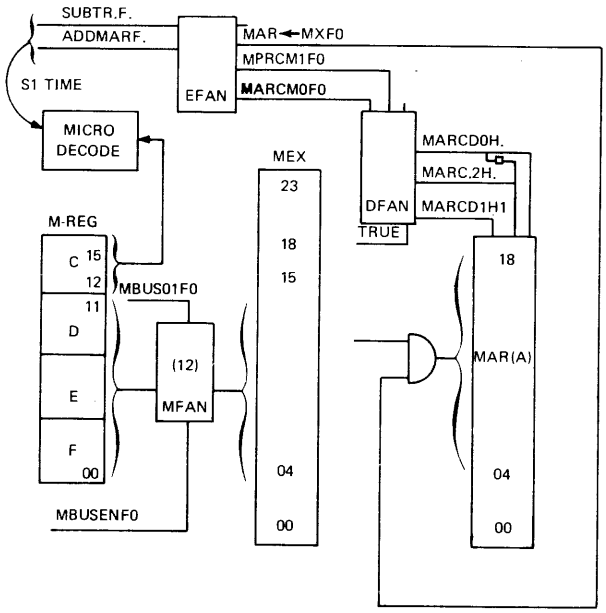


Fig. II-167 123C MICRO DATA FLOW BLOCK DIAGRAM

4 CLOCK EXECUTION

With the 123C Micro in the M-Register and exposed to the MOP lines for execution BRANCHF. is true. Refer to Figure II-168. BRANCHF. true causes MBUSENFO*MBUSO1F0 to be true thus gating MOP lines 00-11 to the MEX lines 04-15 respectively. BRANCHF. true also disables MLENBLFO*MAR+1. F0 from occurring when FINISHDO is true. At S1 time, BRANCHF. generates either MAR←MXFO*MARCM/F0 (MAR(A) in add mode) or MAR←MXFO*MARCM/FO*MARCMOFO. (MAR(A) in Subtract mode). MOP bit 12 will determine which is true. When FINISHDO occurs and because MLENBLFO is false, a Machine or pseudo NO-OP is forced to the M-Register for execution. During the execution of the pseudo 2 clock NO-OP a concurrent M-Fetch operation occurs which fetches the Micro located at the incremented or decremented MAR(A) address. This "new Micro" is then latched in the ML-Register. The ML-Register is set in the M-Register when FINISHDO is true and the trailing edge of the 4MHz clock occurs.

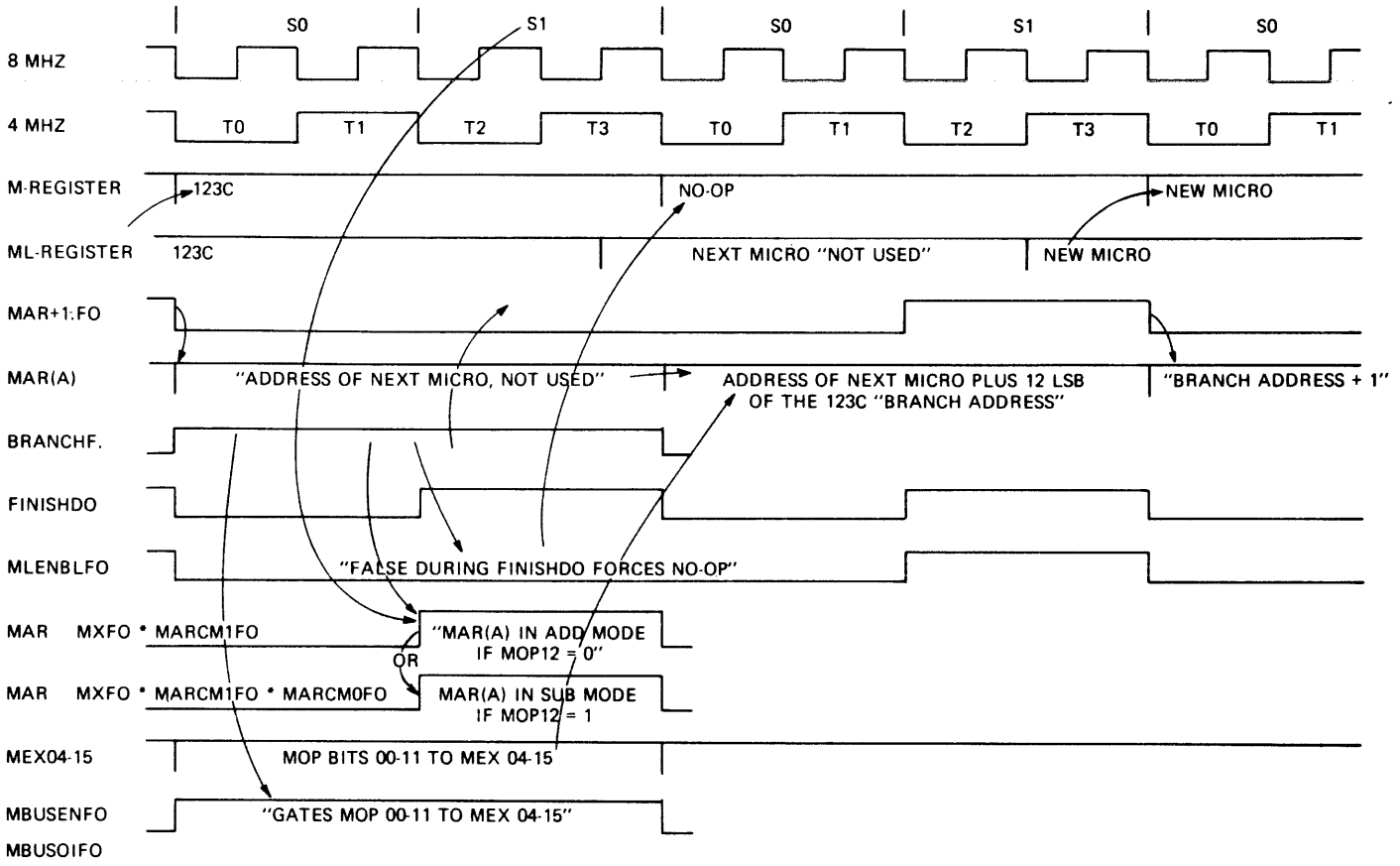


Fig. II-168 123C MICRO TIMING

145C MICRO

The function of the 145C Micro is to increment or decrement the address of the next in line Micro in MAR(A) by the value of the 12 LSB of the Micro (Relative called address Magnitude). In addition, the address in MAR(A) of the next in line Micro to be executed is written into the A-Stack (TAS). The execution time is 5 clocks and includes a 2 clock Machine or pseudo NO-OP to fetch the next executable Micro. With the exception of storing MAR(A) in TAS and incrementing and decrementing MAR(A) at S2 time rather than S1 time, the 145 C Micro is identical to the 123C Micro.

THEORY OF OPERATION

The Block Diagram in Figure II-169 illustrates the basic data flow for the 145C Micro.

S0 Time

A-Stack pointer is increment by one in preparation of a Sink TAS operation.

Functional Detail

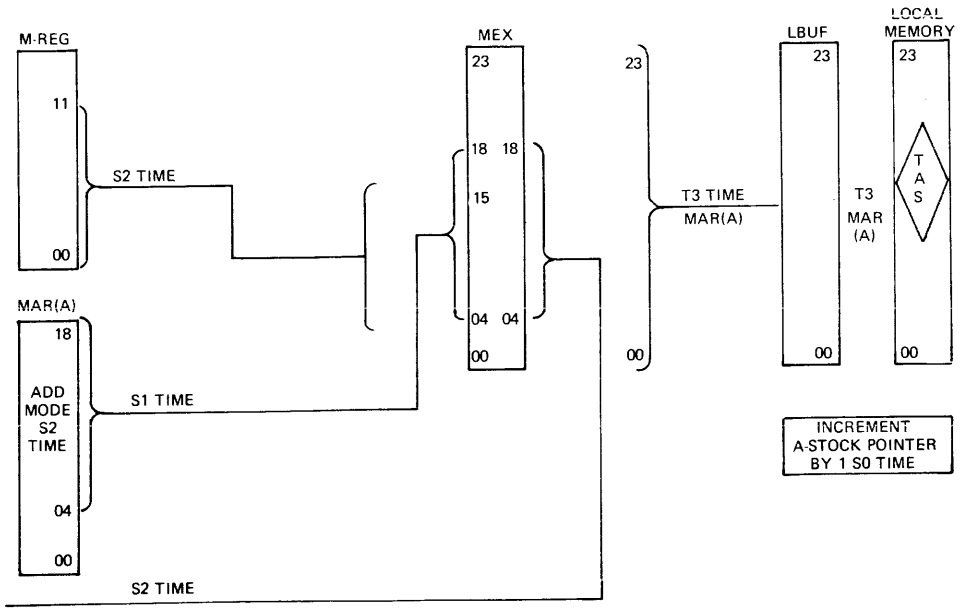


Fig. II-169 145C MICRO BASIC DATA FLOW BLOCK DIAGRAM

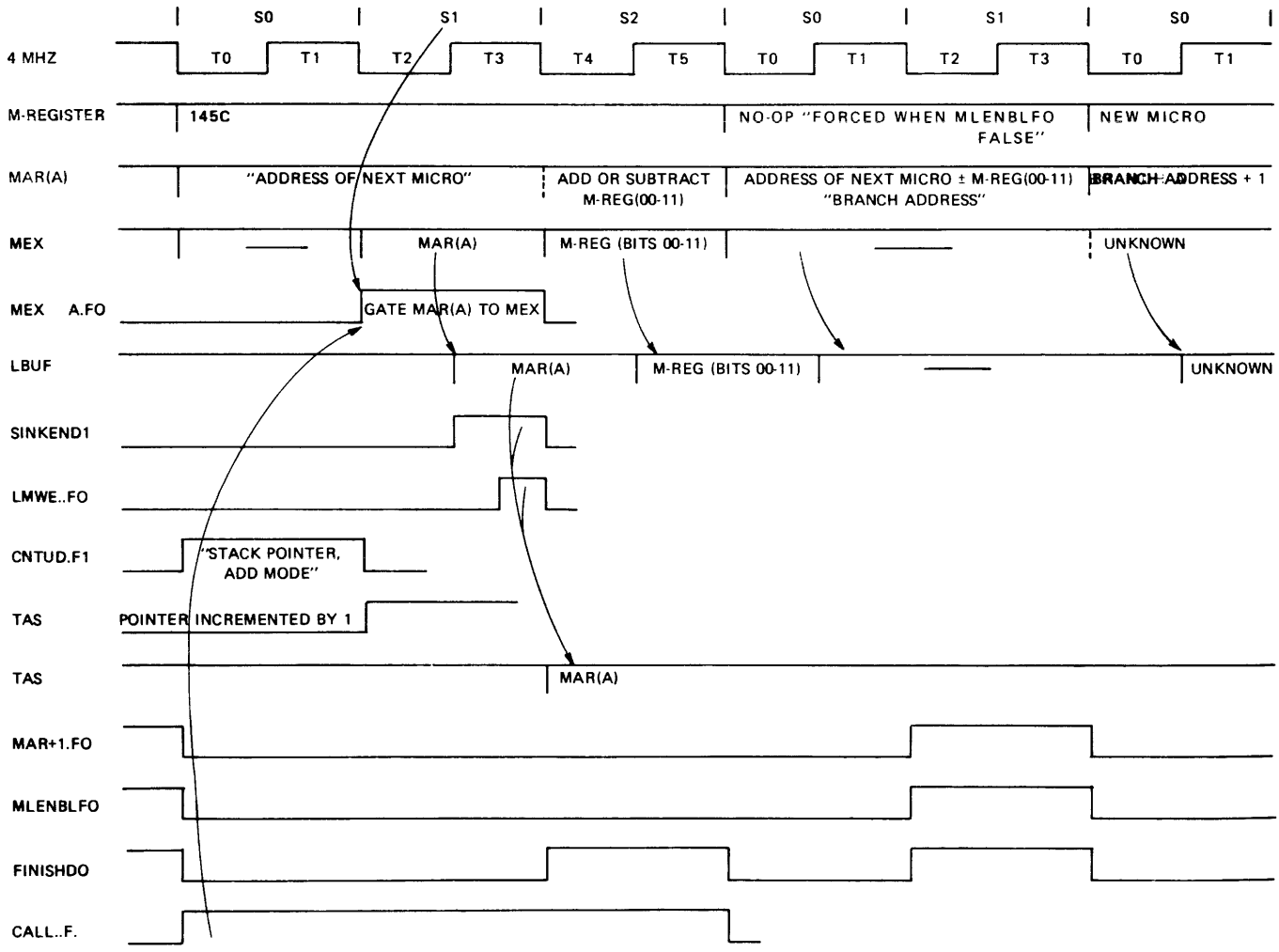


Fig. II-170 145C MICRO TIMING

S1 Time

The address in MAR(A) bits 04 through 18 are gated to the MEX bits 04-18. The 24 bits of the MEX are set in LBUF and written in TAS when local Memory Write Enable (LMWE. . FO) is true.

S2 Time

M-Register (Bits 00-11) are gated to the MEX (bits 15-04) shifting the bits "up four" points to a Micro address. The contents of the MEX (bits 04-18) are added to or subtracted from the address in MAR(A).

5 CLOCK EXECUTION

The 145C Micro when executed generates CNTUD. F1 at S0 time. Refer to Figure II-170.

CONTUD. F1 will cause the A-Stack Point to be incremented by 1 with the trailing edge of the next clock (4MHz).

CALL. . F. is true when the 145C Micro is held in the M-Register and decoded. When CALL. . F. * S1 are true.

√ MEX A. FO is true.

MEX A. FO true gate the contents of MAR(A) bits 94-18 to the MEX (bits 04-18).

SINKEND1 is true at T3 time and therefore the address of TAS is established.

LMWE. . FO causes the contents of LBUF to be written into TAS.

CALL. . F. at S2 time will cause MAR(A) to either be in the Add or Subtract Mode depending on whether MOP bit 12 equals a zero or one. Similar decoding to that of the 123C Micro applies as CALL. . F. *S2 time cause the same to occur as does BRANCHF. *S1 time.

During the 2 clock pseudo NO-OP which is forced because MLENBLFO is held false when FINISHDO occurs, a MFETCH operation occurs. This will fetch the next Micro to be executed from S-Memory at an address specified by the Incr/Decr MAR(A). This new address is referred to as the Branch Address.

4D MICRO

The function of the 4D Micro is to either Shift or Rotate the X or Y Register either Left or Right by the number of bits specified. When Rotate is specified, all 24 bits are rotated.

What a Left Shift is specified zeros are filled on the right and data is truncated on the left. When a Right Shift is specified the reverse will occur.

THEORY OF OPERATION

The basic data flow for the 4D Micro is shown in Figure II-171.

S0 Time

At S0 time a Mask which is generated by decoding MOP bits 00-04 and MOP bit 07 is gated to the MEX, through the rotator and set in MIR. The Mask is rotated in the Rotator only when a Shift Left is specified. The amount of rotation when Shift Left is specified is the complement of the Shift Rotate Count (MOP Bits 00-04).

S1 Time

At S1 time the data from either the X or Y Register is gated to the MEX, through the rotator and set into the MIR bit positions which have the MASK bit set. Data is rotated by the value of the Shift/Rotate count (MOP bits 00-04), when either Shift/Rotate Right is specified. Data is rotated by the complement of the Shift/Rotate Count when either Shift/Rotate Left is specified.

S2 Time

At S2 time and MIR (Bits 08-31) register is sourced and gated to the MEX (Bits 23-00 respectfully). At T5 time the MEX data is set in LBUF and written into the original source data register (X or Y) when LMWE. . FO is true.

3 CLOCK EXECUTION

S0 Time

MASKSTCO is true during S0 time. MASKSTCO enables gating the Mask Bits generated by the Mask Generator to the MEX, the Rotator and into MIR.

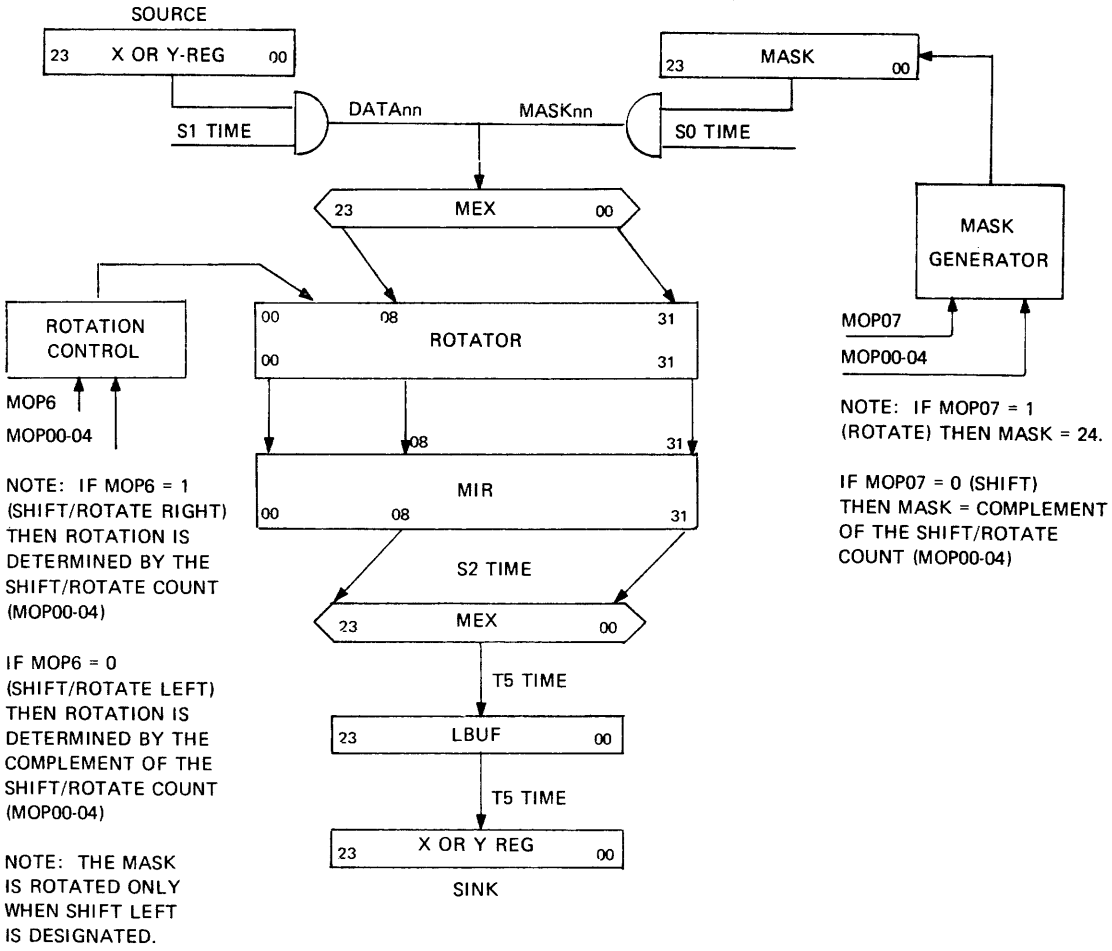


Fig. II-171 4D MICRO DATA FLOW BLOCK DIAGRAM

S1 Time

DATASTCO enables gating the X or Y Register Data to the MEX, the Rotator and into MIR.

S2 Time

MX←MIRFO gates the contents of MIR to the MEX. The MEX data is then set into LBUF with the trailing edge of the inverter 4 MHz clock which is true during +4 time. CSSINKF1 is true during +5 time and the address of the sink register is also established at this time. LMWE. . FO occurs when CSSINKF1 and the 8 MHz clock is true. The Shift/Rotate is set in the Sink Register (Same or Source register) with the trailing edge of the 4MHz clock at T5 time.

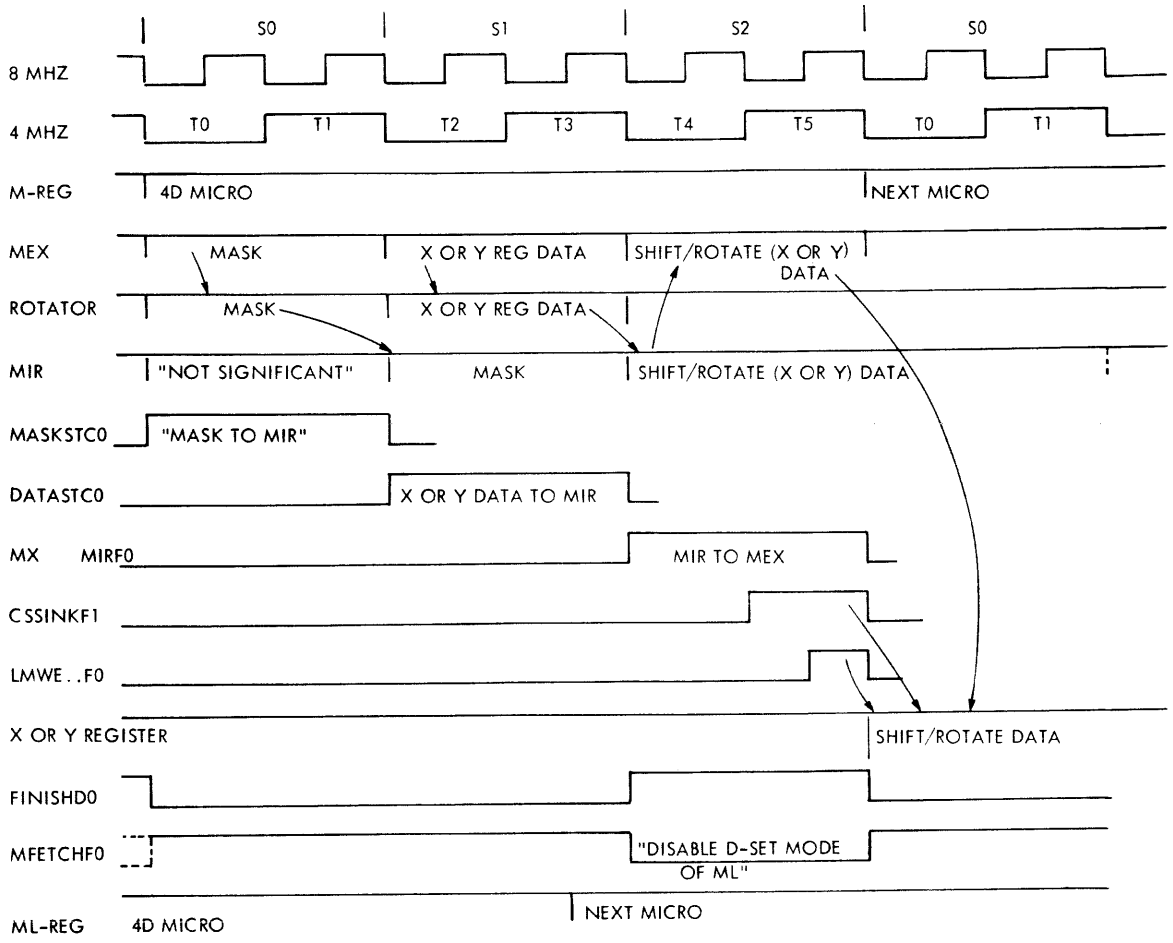


Fig. II-172 4D MICRO TIMING

The MFETCHFO F/F is reset at S2 time to disable the D-Mode of the ML-Register. The next Micro is set in the ML-Reg. When the read data from S-Memory is available during T3 time. MFETCHFO false therefore insures the next Micro remains in ML until it is set into the M-Reg for execution.

5D MICRO

The function of the 5D Micro is to Shift the concatenated X & Y Registers left or right by one bit.

When executing the 5D Micro, the X & Y registers are considered as one 48 Bit Register with the X register the leftmost (MSB) half of the concatenated 48 bit register.

When a shift left is specified, a zero bit is filled on the right and the data bit is truncated on the left. When a shift right is specified the reverse occurs. The execution time is 6 clock periods.

THEORY OF OPERATION – SHIFT RIGHT

The basic data flow for a shift right is shown in Figure II-173.

S0 Time

Execution of the 5D Micro requires a Mask of 23 to be true; therefore, the Shift/Rotate Count (Mop Bits 04-00) must = 00001. With the Shift/Rotate Count = to 00001, mask will equal 23 (24s complement of 00001). The Mask of 23 is gated to the MEX (bits 00-22) through the rotator (not rotated) and set in MIR (bits 31-09).

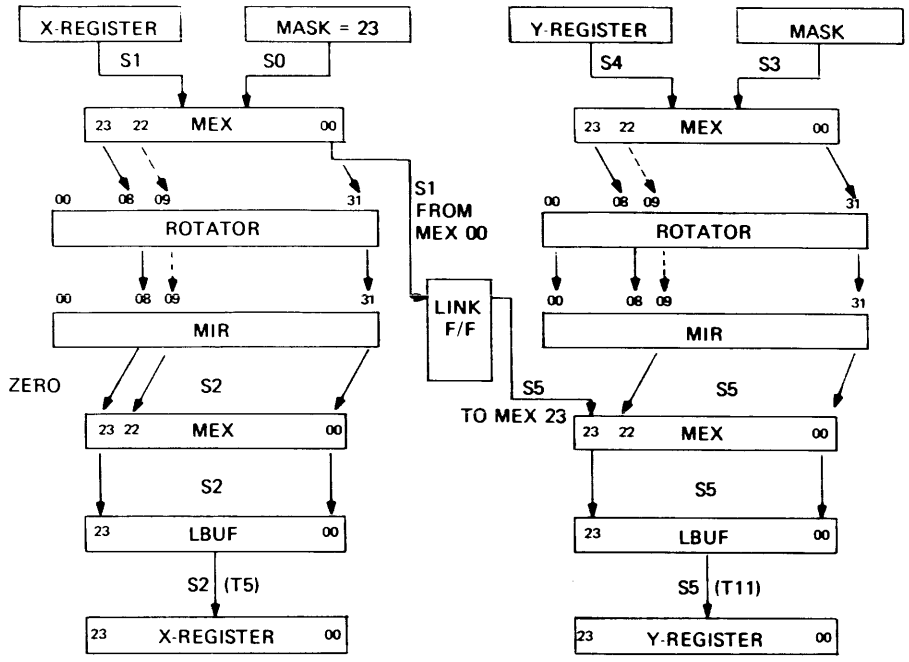


Fig. II-173 5D MICRO & RIGHT SHIFT DATA FLOW

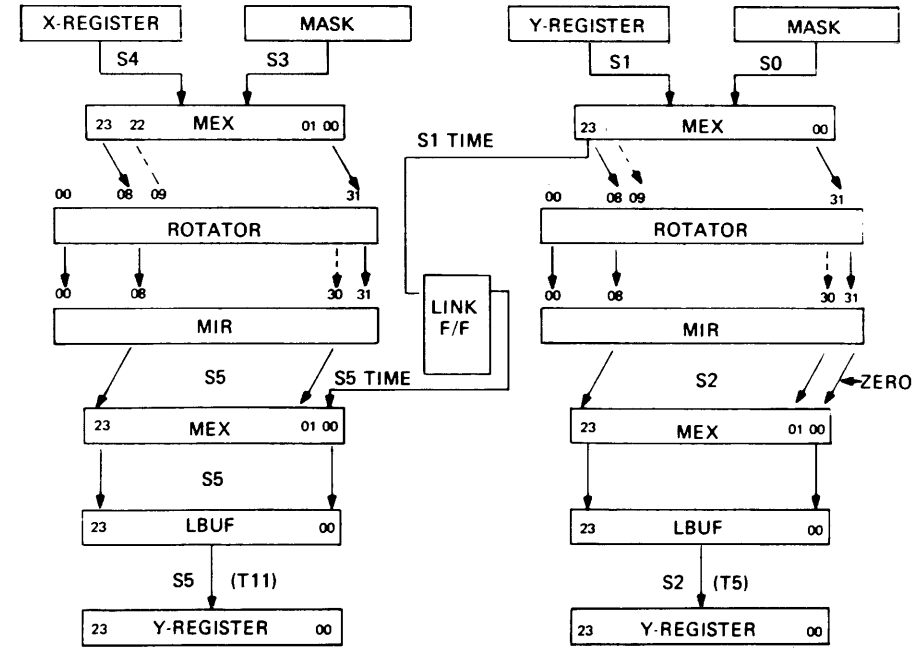


Fig. II-174 5D MICRO & LEFT SHIFT DATA FLOW

S1 Time

The X Register data is gated to the MEX through the rotator to MIR. The LSB of the MEX 9 Bit 00) is set in the LInk F/F. The data is shifted right one bit position with zero filled on the MSB and the LSB of data truncated on the right. Note the LSB is set in the Link F/F.

S2 Time

MIR IS sourced and the shifted X-Register is set back in the X-Register.

S3 Time

A Mask of 23 is gated to the MEX, through the Rotator and set in MIR.

S4 Time

The Y-Register Data is gated to the MEX, through the Rotator to MIR. The Data is shifted right one bit with the LSB of the Y-Register truncated with a zero filled on the MSB.

S5 Time

MIR and the Link F/F are sourced and gated to the MEX. Only MIR bits 09 through 31 contain Y-Register data Bits and are gated to the MEX Bits 22-00. The Link F/F is gated to the MEX bit 23. The contents of the MEX is then set in LBUF and set in the Y register a S5 (T11) time.

THEORY OF OPERATION – SHIFT LEFT

The overall function of the Shift left operation is similar to the shift right operation with the following exceptions. Refer to Figure II-174.

S0 Time

The 23 Bit Mask is gated to the MEX (Bits 00-22). The Mask is shifted one bit to the left and set in MIR.

S1 Time

The Y-Register data is gated to the MEX through the Rotator to MIR. The data is shifted one bit to the left (Right shift of 23). The MSB of the MEX 9 bit 23) is set in the LInk F/F.

S2 Time

The shifted Y-Reg. data is set back in the Y-Register.

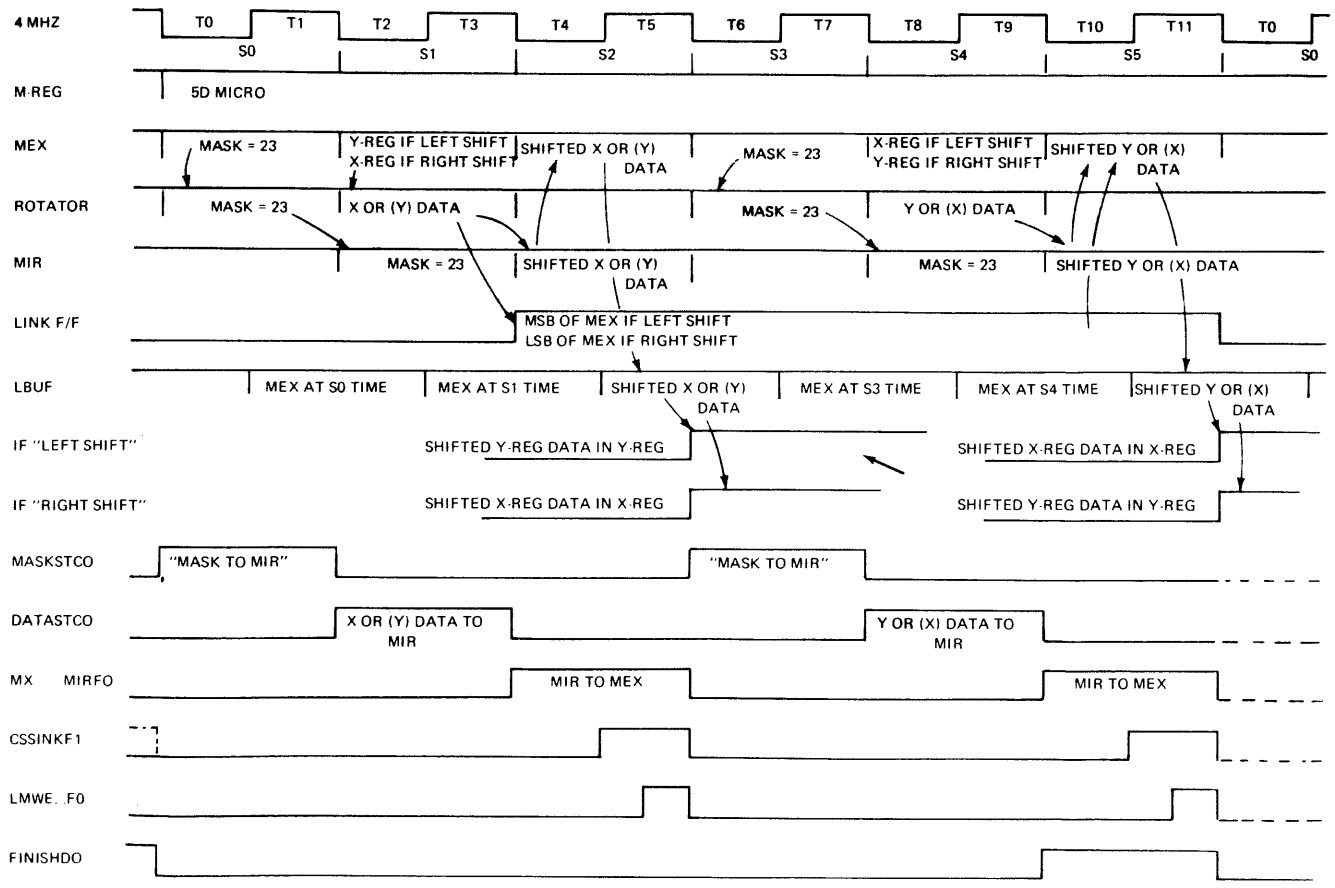


Fig. II-175 5D MICRO TIMING

S3 Time

A 23 Bit Mask is gated to the MEX (Bits 00-22). The Mask is shifted one bit to the left and set in MIR.

S4 Time

The X-Register Data is gated to the MEX, through the Rotator to MIR the Data is shifted left one bit in the rotator. (Right shift of 23)

S5 Time

The Shifted X-Register data in MIR (Bits 09-30) is gated to the MEX 9 Bits 23 through 01). The MSB of the Y Register Data which was stored in the Link F/F is gated to the LSB of the MEX. The contents of the 24-Bit MEX is set LBUF and written into the Y-Register.

6 CLOCK EXECUTION

The 5D Micro when executed generates MASKSTCO at S0 and S3 time. MASKSTCO true enables gating a Mask of 23 Bits to the MEX, through the rotator to MIR. Refer to Figure II-175 DATASTCO is true at S1 and S4 time which allows gating the X or Y Data to the MEX through the rotator to the MIR. MX←MIRFO is true at S2 and S5 time and allows gating the MIR register to the MEX. The contents of the MEX is always set in LBUF with the trailing edge of the inverted 4MHz clock. At T5 and T1 time the sink registers address and chip select levels are true which generate CSSINKF1. When LMWE. . F0 occurs, the contents of LBUF is written into the selected sink Register.

The Link F/F will store the MSB of the MEX (left Shift) on the LSB of the MEX (Right Shift) with the trailing edge of the 4 MHz clock which is true during T5 time. The bit stored in the Link F/F is gated to the LSB of the MEX (left Shift) or the MSB of the MEX (Right Shift) during S5 time. FINISHDO resets the Link F/F.

LINK FLIP FLOP

The function of the Link F/F is to temporarily store the truncated data bit in either a left or right shift operation. The bit stored in the Link F/F is then gated to either the LSB of the MEX (Left Shift) or the MSB of the MEX (Right shift). Refer to 5D Micro Data Flow, Figures II-173 and II-174. Figure II-176 illustrates the Link F/F.

At S1 time, if MOP 06 = 1 (Shift Right) the LSB of the MEX 9 Bit 00) is set in the Link F/F (LINKBTC.). If MOP 06 = 0 (Shift Left) the MSB of the MEX (Bit 23) is set in the Link F/F. At S5 time if MOP 06 = 1 (Shift Right) the link bit is gated to the MSB or the MEX (Bit 23). If MOP 06 = 0 (Shift Left) the link bit is gated to the LSB of the MEX (Bit 00). FINISHDO will reset the Link F/F at S5 time if a 1 bit is set in the F/F during S1 time. Note that if at S1 time the F/F is not set and if at S5 time the MEX bit into gate A5 or K5 is true and the corresponding gate C5 or G7 respectfully outputs a true, the Link F/F will set (The F/F will toggle). The next FINISHDO will then reset the F/F. In certain cases executing 2 consecutive 5D Micros will not function properly.

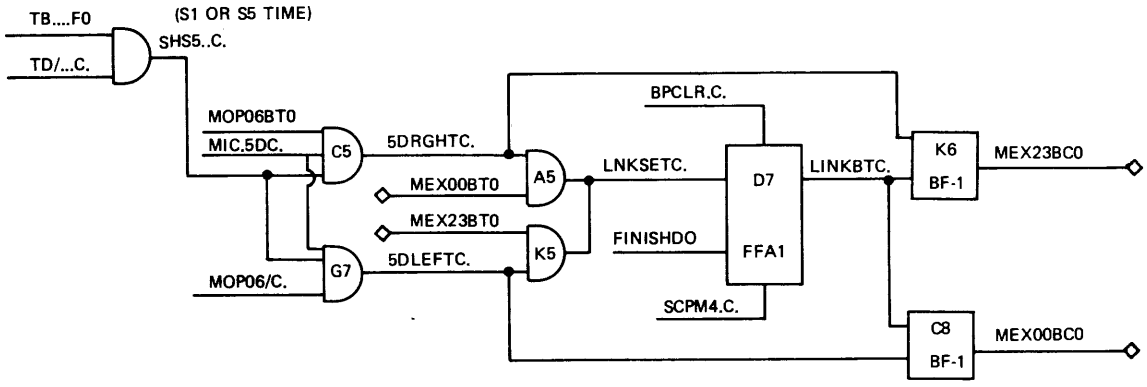


Fig. II-176 LINK FLIP-FLOP

6D MICRO

The function of the 6D Micro is to Increment and/or Decrement the FA and/or FL-Register by the Count Magnitude (MOP Bits 00-04). If MOP bits 00-04 equal zero then the value of CPL (C-Reg 00-04) is used as the Increment and/or decrement value. MOP bits 00-07 determine which register(s) is selected and whether increment or decrement of each is to be performed.

The execution time is 4 clock periods.

THEORY OF OPERATION

The execution of the 6D Micro is completed in two phases. See Figure II-177. During the first phase, the FA register is incremented or decremented by the value of MOP bits 00-04 if ≠ zero or the value of CPL bits 00-04 if MOP bits 00-04 = zero. Although the increment or decrement will always occur in the 24-Bit Function Box, the results is written back into FA only when a Incr/Decr of FA is specified. During the second phase the same occurs only the FS-Register if affected.

4 CLOCK EXECUTION

The timing for the 6D Micro is shown in Figure II-178 during T0T1T2 time, the FA-Register is sourced. The value of FA and the Count Value is applied to the inputs of the 24 Bit Function Box as ADATA and BDATA respectfully. The Binary Sum ouput of the 24-Bit Function Box is gated to the MEX. LBUF will contain the Binary Sum of FA and the Count Value at the trailing edge of the inverted 4MHz clock which is true during T2 time. If Count FA Down is specified, SUB. . . DO will be true which causes a subtract to occur within the Function Box. Normally the 24-Bit Function Box will perform a add operation. At T3 time the address and Chip Select levels for the FA-Register in Local Memory will be true only when the FA register is either to be incremented or decremented. CSSINKF1 is the result of the FA-address being generated and enables a write into Local Memory to occur via LMWE. . F0.

At T4T5T6 time the FL-Register is sourced and the Binary Sum of the FL-Register and the Count Value is gated to the MEX (Bits 00-15) from the output of the 24-Bit Function Box. SUB. . . D) is true only if FL is to be decremented. CSSINKF1 and LMWE. . FO are true during T7 time only when the FL register is to be either incremented or decremented.

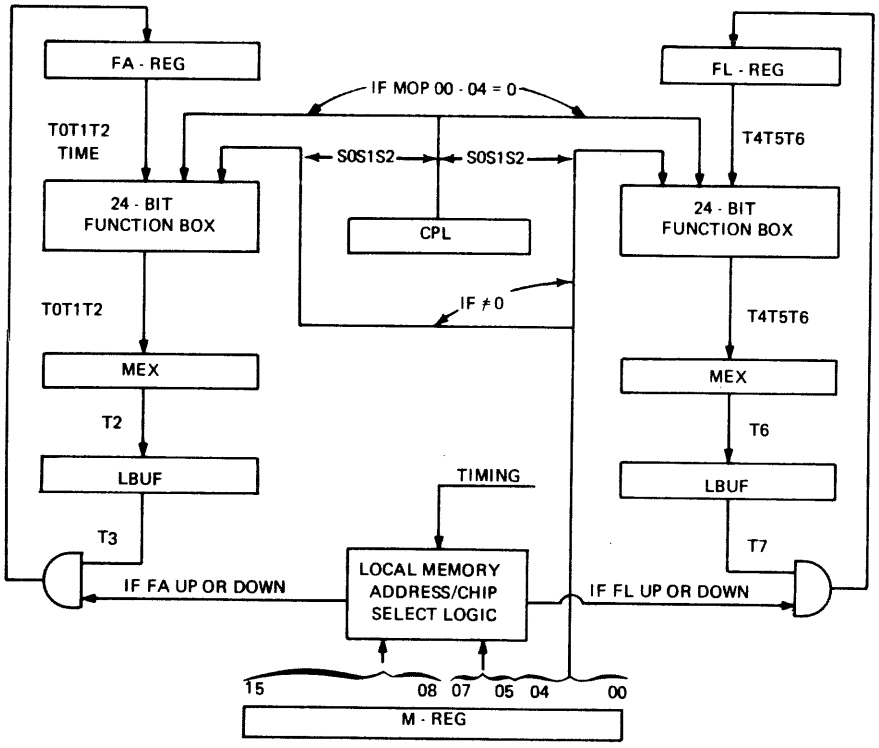


Fig. II-177 6D MICRO DATA FLOW

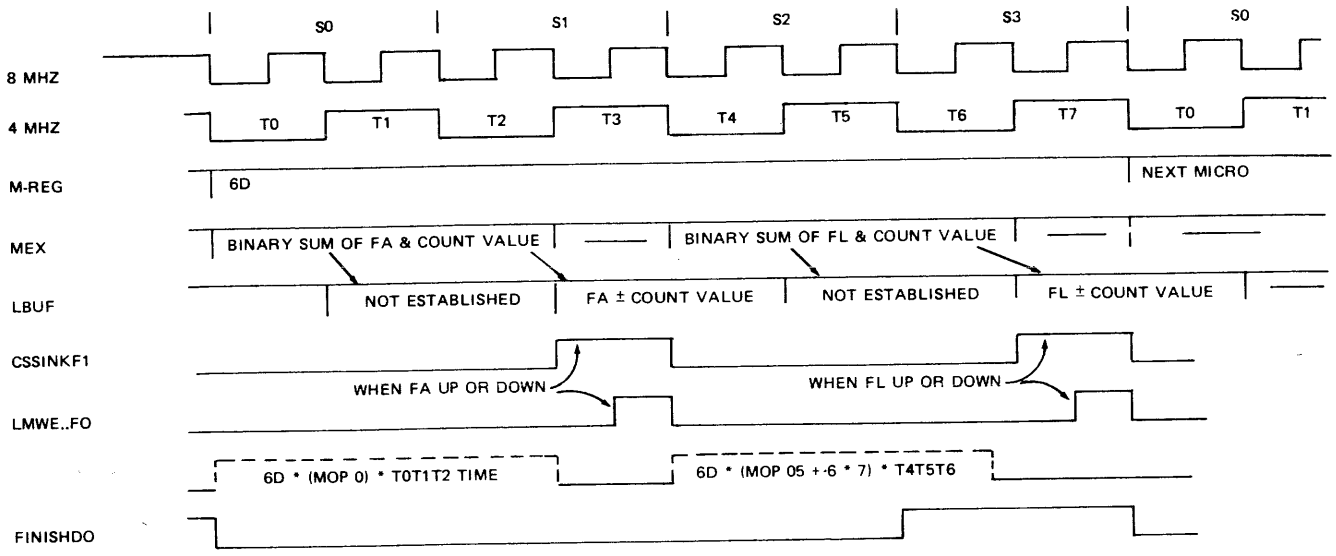


Fig. II-178 6D MICRO TIMING

7D MICRO

The function of the 7D Micro is to move the contents of the FA and FB Registers to MIR and from MIR to a destination word of Left and Right Scratch Pad respectfully. In addition the contents of a word of Left and Right Scratch Pad is also moved to the FA and FB Registers respectfully.

The basic sequence of operations is as follows:

1. FA to MIR
2. Scratch Pad Left (source) to FA
3. MIR to Scratch Pad Left (Sink)
4. FB to MIR
5. Scratch Pad Right (source) to FB
6. MIR to Scratch Pad Right (Sink)

The execution time is 10 clock periods.

THEORY OF OPERATION

Because the execution of the 7D Micro requires 10 clock periods to complete and the Sequencer provides only eight discrete 4 MHz clock periods (S0 through S7), the REPEATF1 flip flop is used to establish 10 clock periods. The Sequencer will sequence from S0 through S4 twice with the REPEATF1 flip flop set during the first S1 through S4 time and during S0 time of the second sequence.

All functions which involve the FA-Register and Left Scratch Pad occur during the first sequence (S0 through S4 time). Those functions which involve the FB-Register and Right Scratch Pad occur during the second Sequence (S0 through S4 time).

First Sequence - Refer to Figure II-179

S0 Time

A 24-Bit Mask is gated to the MEX through the Rotator to MIR.

S1 Time

The FA-Register is sourced, gated to the MEX, through the Rotator to MIR.

NOTE: With the MASK = 24 all 24 Bits of FA are gated to MIR.

S2 Time

When T4T5T6 time is true, the source word of Left Scratch Pad is addressed, gated to the MEX and latched into LBUF.

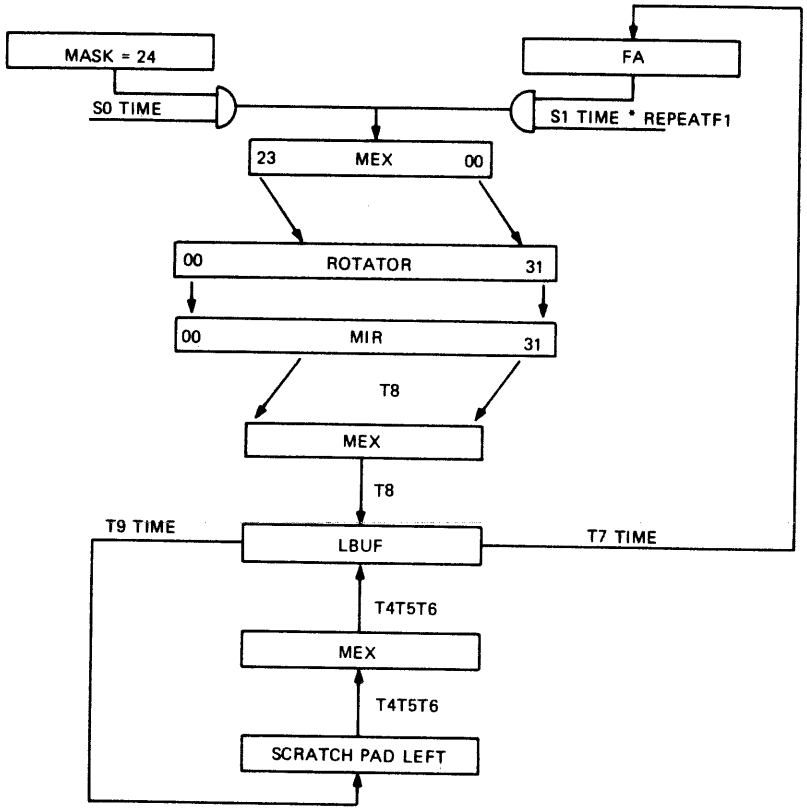


Fig. II-179 7D MICRO DATA FLOW; FIRST SEQUENCE

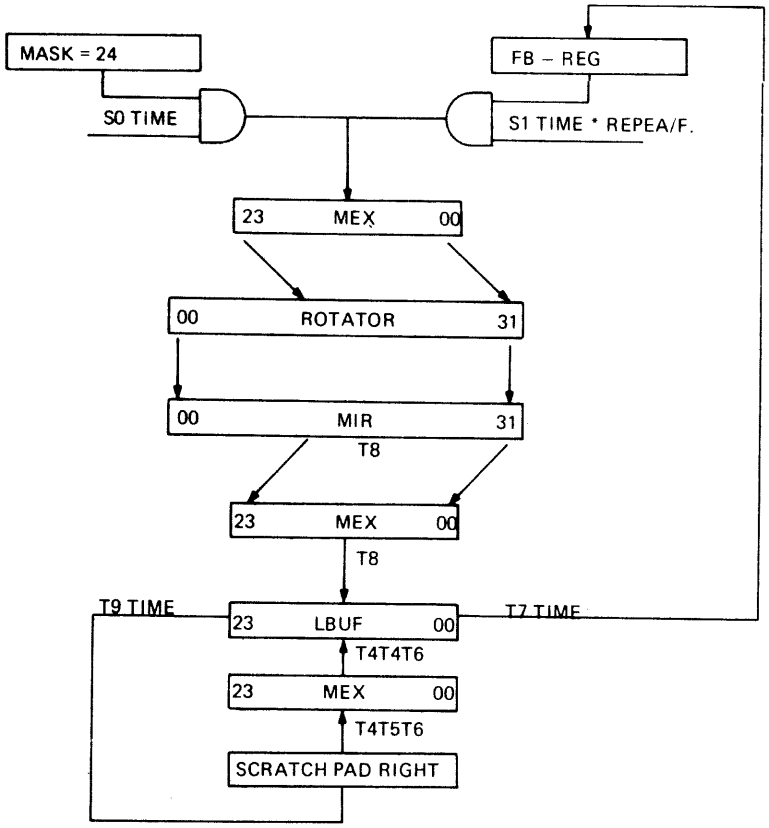


Fig. II-180 7D MICRO DATA FLOW; SECOND SEQUENCE

S3 Time

When T7 is true, the contents of LBUF is set into the FA-Register.

S4 Time

When T8 time is true, MIR is sourced, gated to the MEX and set in LBUF. When T9 time is true, the contents of LBUF is written into the Sink Word of Left Scratch Pad.

Note that the source and sink Left Scratch Pad words may be either the same or different words.

Second Sequence - Refer to Figure II-180

The second sequence is identical to the first sequence except the FB-Register and the Source and Sink Scratch Pad Right words are affected.

10 CLOCK EXECUTION

The 7D Micro is held in the M-Register for 10 clock periods. See Figure II-181. The sequencer will be cleared when T9 time is true. The REPEATF1 F/F is set at the trailing edge of S0 time and reset at the trailing edge of the next S0 time to occur. When set it basically provides functions to occur which pertain to the FA-Register and Left Scratch Pad. The MIR register is used as a "Holding Register" when moving the contents of FA and FB to words of Scratch Pad Left and Right respectfully. A "Holding Register" is necessary as the 7D Micro allows the source and sink word of Scratch Pad to be the same. Although the contents of the FA and FB-Registers are gated through the Rotator, no Rotation occurs. A MASK of 24 bits is used to enable MIR to receive the true 24-bit contents of the FA and FB-Registers. Four Local Memory writes occur as well as four sources. The arrows indicate data movement with the exception of the arrows from LMWE. . FO which indicate the particular data written into the four sinks.

8D MICRO

The function of the 8D Micro is to either add to or subtract from the value of the FA-Register the value of word of Left Scratch Pad. The execution time is 4 clock periods.

THEORY OF OPERATION

Due to the fact that both the FA-Register and Left Scratch Pad is addressed as A-Data within Local Memory, it is necessary to move the word of Left Scratch Pad to TEMB. which is located in the B-Data portion of Local Memory, it is is done so both the FA-Register and Left Scratch Pad Word (stored in TEMP) can be gated simultaneously through the 24 bit adder portion of the 24-Bit Function Box. See Figure II-182.

4 CLOCK EXECUTION

The timing for the 8D Micro is shown in Figure II-183.

During S0 & S1 time Scratch Pad Left is gated to the MEX, set in LBUF and written into TEMB. During S2 and S3 time both FA and TEMB are sourced (same address except for Chip Select) and gated to the 24-Bit Function Box where either a add or subtract will occur. MOP bit 04 if true indicates Subtract the Left Pad word from FA. the level SUB. . . DO will be true. The Binary "Sum" output of the Function Box is gated to the MEX set in LBUF and written back in FA. Refer to Figure II-182.

During T0T1T2 time the address of the word of Left Scratch Pad designated is true. The word of Left Scratch Pad is gated to the MEX which in turn is set in LBUF with the trailing edge of the inverted 4MHz clock pulse. At T3 time the sink address of TEMB is true and the contents of LBUF is written into TEMB with LMWE. . FO. At T4T5T6 time both the FA and TEMP registers are sourced and gated to the Function Box. The Binary Sum output (Sum of Diff) is gated to the MEX and set in LBUF. At T7 time, the sink address (FA-Register) is true and the results of the add or subtract operation now in LBUF is written into the FA-Register.

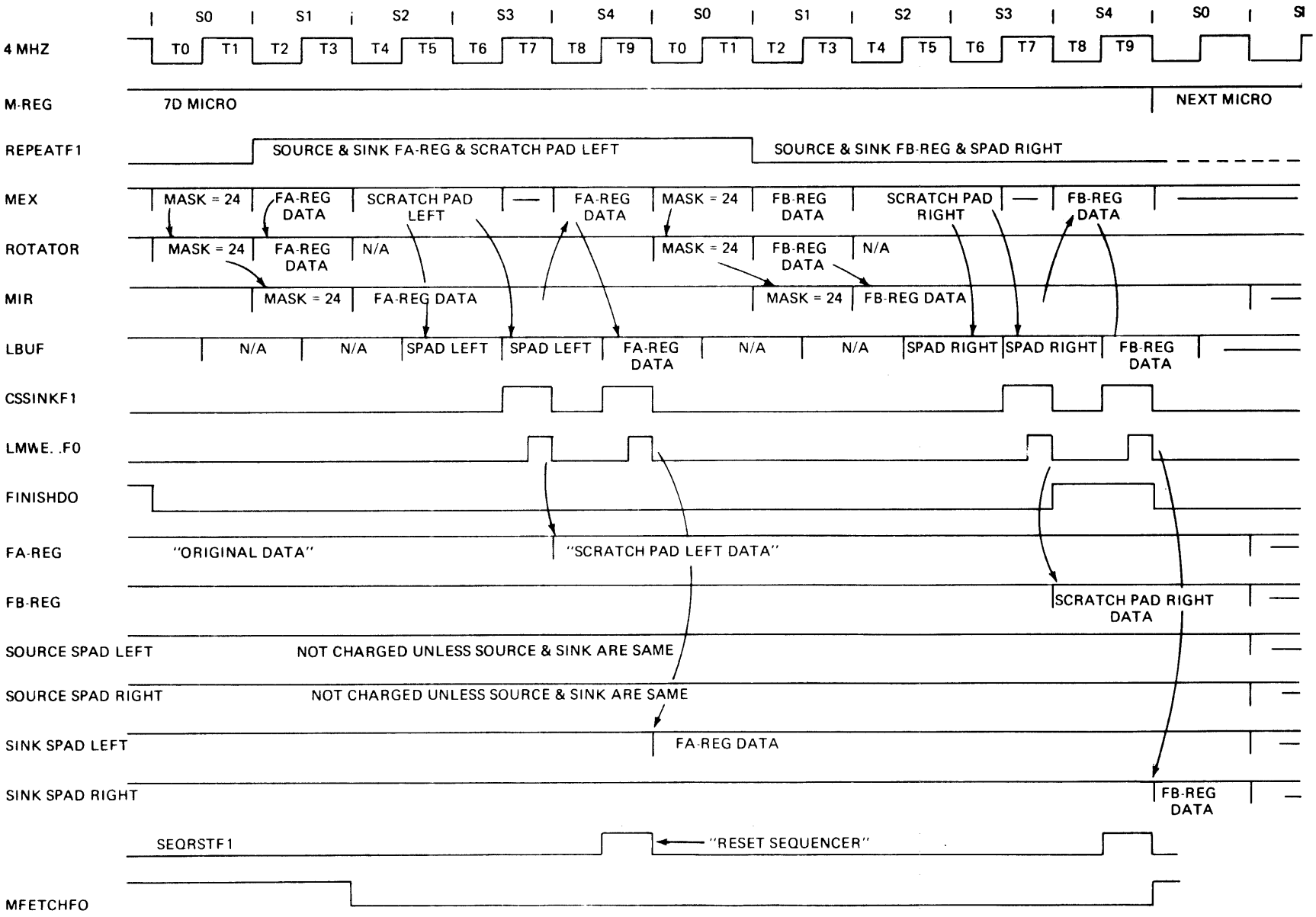


Fig. II-181 7D MICRO 10 CLOCK EXECUTION

Functional Detail

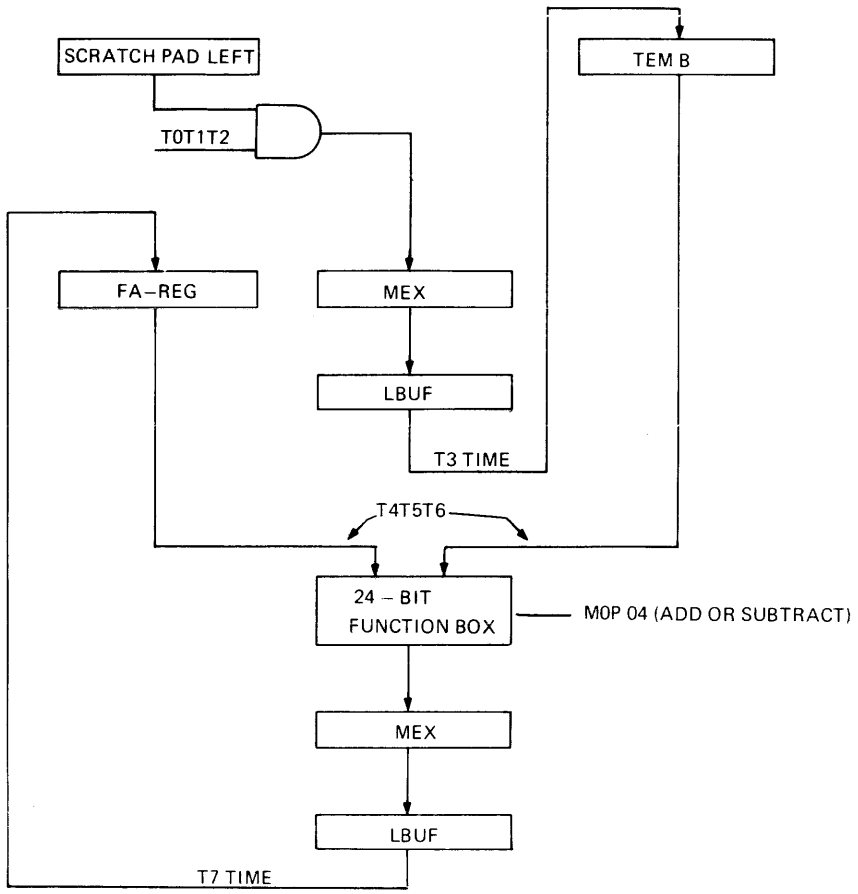


Fig. II-182 8D MICRO DATA FLOW

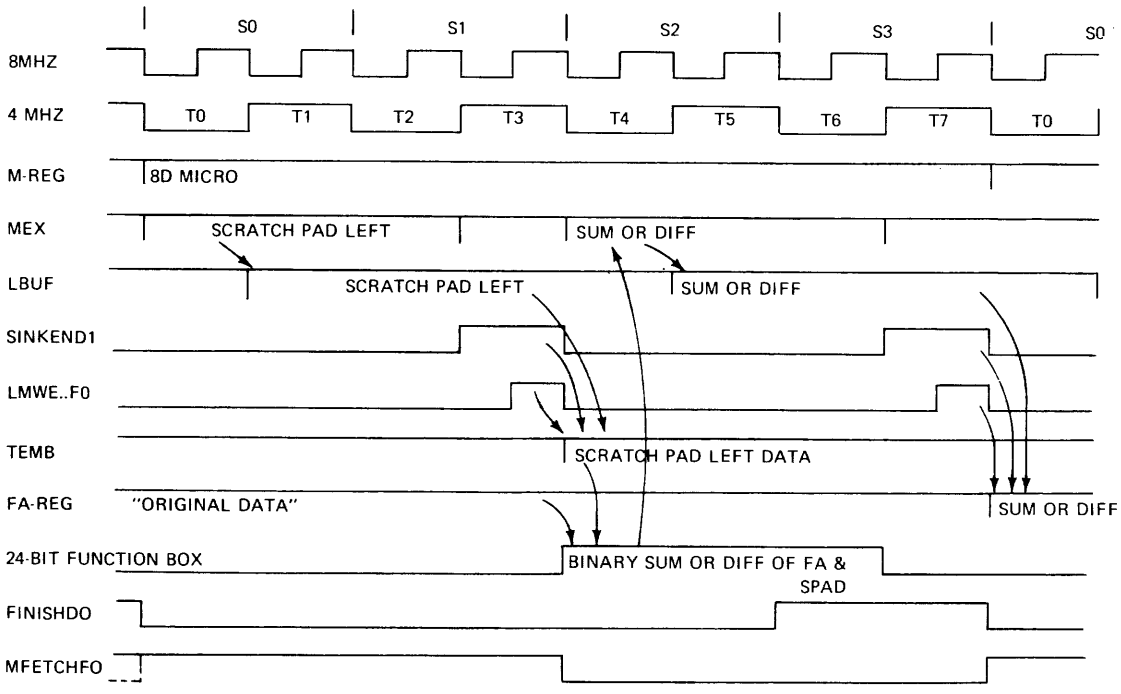


Fig. II-183 8D MICRO TIMING

2E MICRO

The function of the 2E Micro is to control starting or stopping the Cassette.

The 2 E Micro (regardless of the variant bit values) cause a read of the Z & Y registers values to occur. A comparison of the value of the register also occurs to determine if X ≠ Y. The effect of generating either Cassette Stop at the Gap (CSTPG.DO) or Cassette Start (SCTRT.DO) is explained during the explanation of the Cassette. Refer to Section II, Cassette Logic for details. Execution time is 2 clock periods.

2 CLOCK EXECUTION

The X & Y Register are sourced during S0 and S1 time and the value of the Registers is gated to the 26-bit Function Box for a compare. Refer to Figure II-184. If X ≠ Y, then the level AEB/. . AO is true at approximately T1T2T3 time. CS+PS. DO is true when AEB/. . AO is true and the Cassette Control variants = 010 (Mop Bits 3, 2 & 1). If Mop Bits 3, 2 & 1 = 001 then CSTPG. DO is true at approximately T0 time, as shown. If MOP Bits 3, 2, & 1 = 000, then CRTRT. DO is true as shown. If the Mode of Operation is MTR, then CSTPG. . DO will also cause the RUNS. . FO to reset, thus halting the Processor.

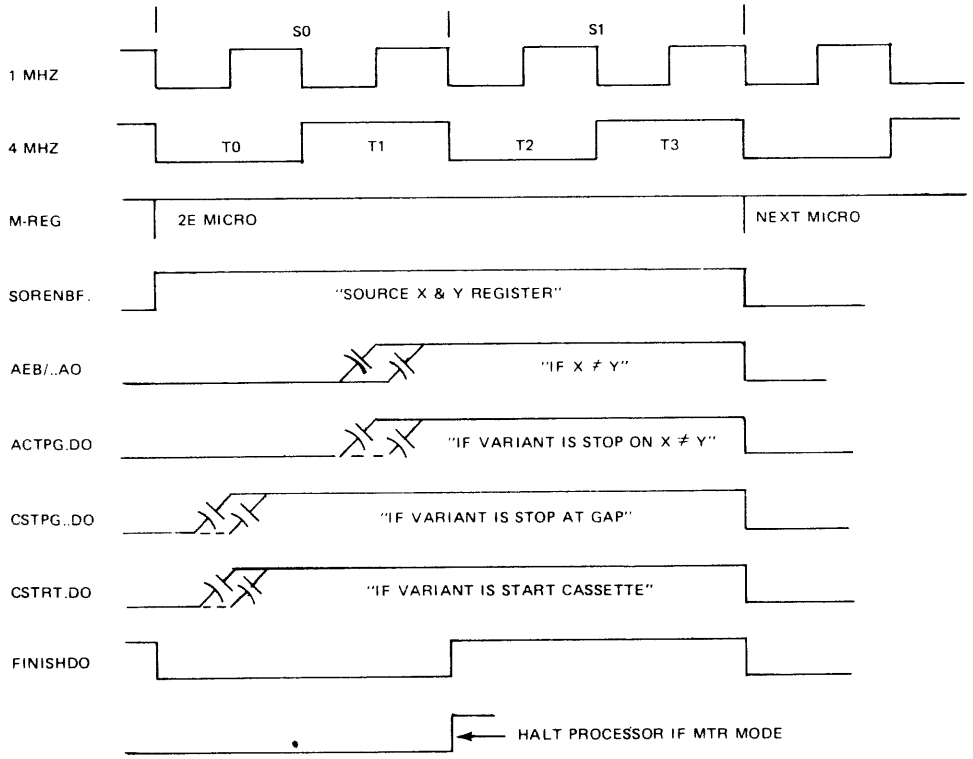


Fig. II-184 2E MICRO 2 CLOCK EXECUTION

6E MICRO

The function of the 6E Micro is to set the Carry F/F by the value specified by the Varient Bits (MOP Bits B-O). A read of the X & Y register will occur regardless of Variant Bit Set and the sum of the two registers will be available. The summing of the two registers will produce many results, two of which have significance during the execution of the 6E Micro. The Carry Level (CYL) is a direct result of the addition and CYD which is a result of a Static comparison. CYD = (X<Y) + (X = Y) * CYF.

DATA TRANSFER

The results of the comparison of X and Y (CYD*CYL) are gated with MOP Bits 03 and 02 respectively. See Figure II-185. If the MOP Bit is set and the appropriate output level of the Function Box is true, the CYF is set. When MOP bit 01 is true the CYF F/F is set regardless of the compare mode on the value of the X & Y Register. When MOP bit 00 is true, CYF is reset.

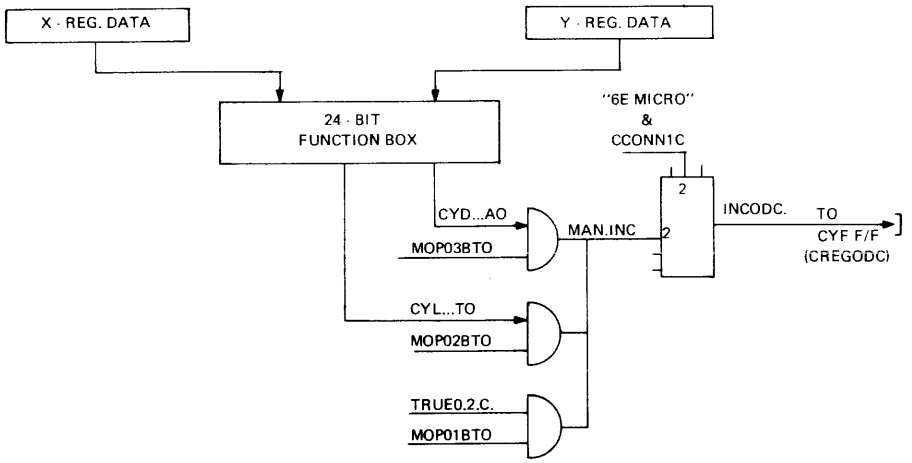


Fig. II-185 6E MICRO DATA FLOW

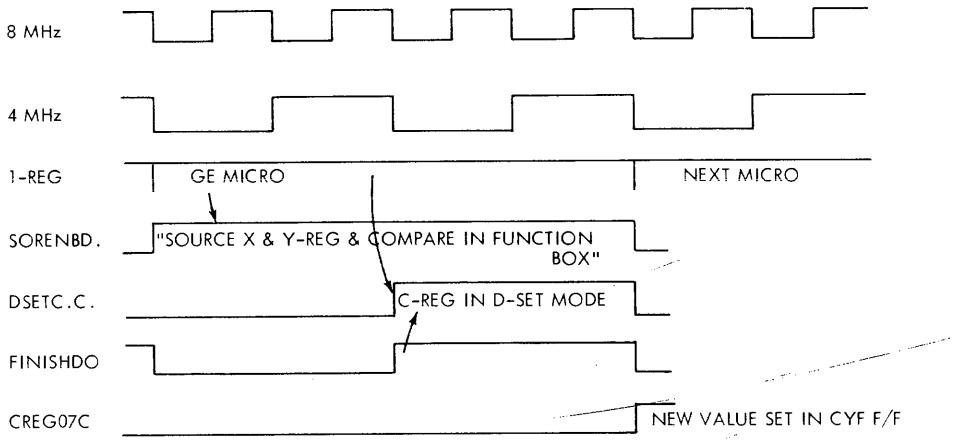


Fig. II-186 6E MICRO TIMING

TIMING

Timing for the 6E Micro is shown in Figure II-186. The X & Y registers are sourced during S0 and S1 time. Both registers are gated to the 24-Bit Function Box, where a comparison of X & Y is made to determine CYD and the sum if generated to produce CYL. DSETC. C. is true when FINISHDO is true and the 6E Micro is executed. DSETC. C. enables the D-Mode of the C-Register 07 Bit Position (CYF F/F).

1F MICRO

The function of the 1F Micro is to halt the processor thereby stopping the execution of Micros. Executing the 1F Micro will cause the RUNS. . FO F/F to be reset, thus the "halt state" of the Processor is true.

TIMING

The 1F Micro timing is shown in Figure II-187. The 1F Micro causes the RUNS. . FO F/F to reset when FINISHDO is true. JUMP/. F. and REPAA/F. will be true as the Halt Micro (1F) does not cause these levels to go false. When the Processor is halted pseudo or machine NO-OPs are executed to display the Register selected on the console switches on the console lamps.

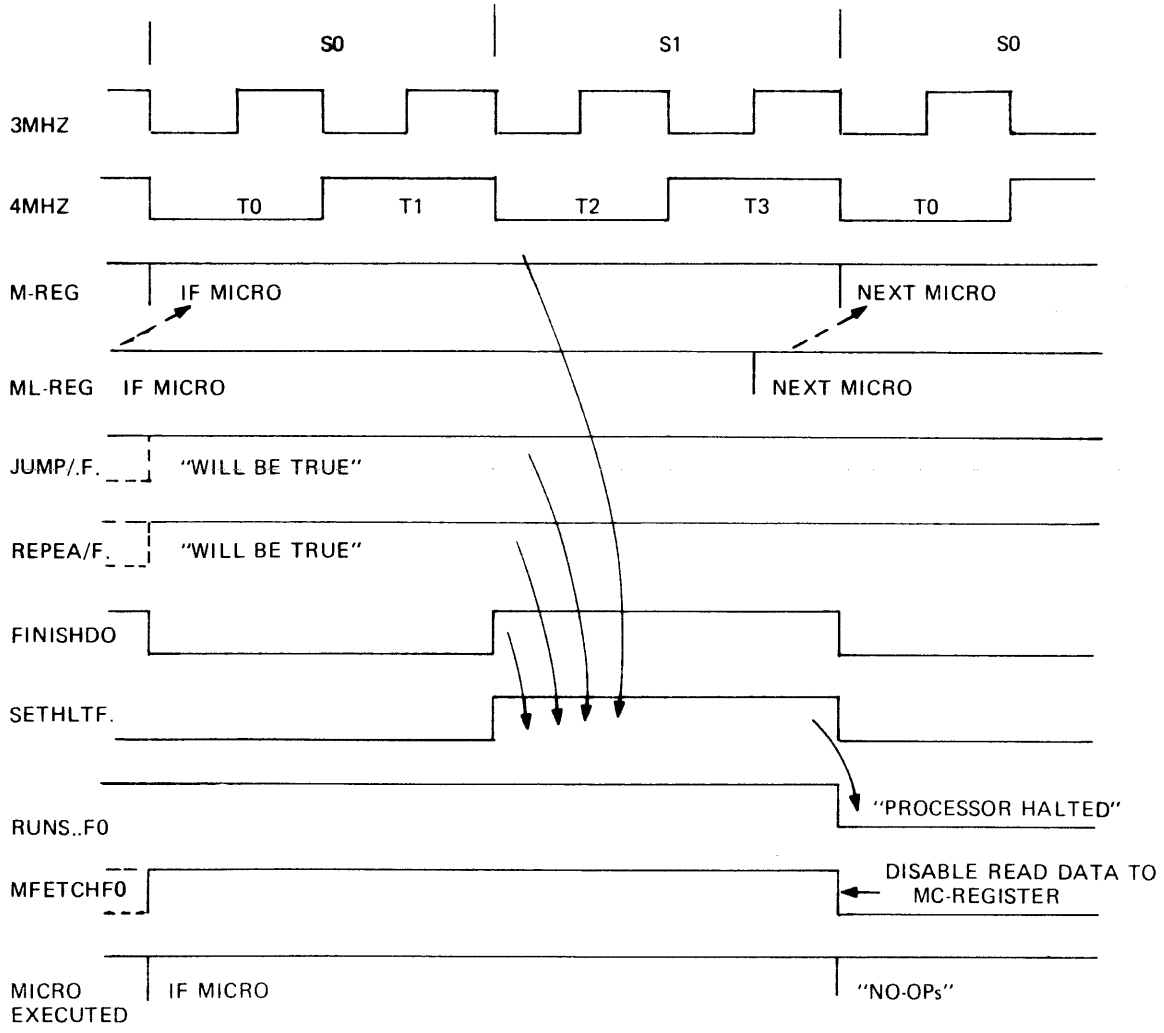


Fig. II-187 1F MICRO TIMING

3F MICRO

The function of the 3F Micro is to shift the contents of the X Register left while counting FL down by 1 after each shift occurs. The operation continues until either FL equals zero or the bit reference by CPL is a one. The execution time is 6 clock periods per bit shifted. The Micro will finish after 2 clocks if FL = 0 or after 4 clocks if MSBX = 1. A Refresh memory cycle is permitted during the execution of the 3F Micro when required. The refresh cycle does not alter the execution of 3F Micro.

DATA FLOW (Refer to Figure II-188)

During S0 and S2 time the FL Register is sourced in Local Memory. The 16 Bits of the FL Register are checked to determine if FL $\neq$ 0. If FL is not = to zero then FINISHDO is disabled at S1 time. At S1 time, regardless of the value of FL, a mask of 23 Bits is gated to the MEX, through the rotator to the MIR register. The Mask is rotated 23 Bits (left 1), thus a mask bit is not set in MIR bit 31. This provides a zero fill on the right. At S2 & S3 time the contents of the X Register is sourced in Local Memory. The MSB of the X Register (MSBX) is checked to determine if the MSBX = 1. If MXBX = 1 is true then finish occurs at S3 time. At S2 time, the X-Register is also gated to the MEX, through the Rotator, shifted 23 (left 1) and set in MIR. Note that the check of MSBX = 1 is not done on the rotated X Register in MIR but on the source data from the X Register at S3 time. MIR is sourced, gated to the MEX and latched in LBUF at T9 time. The shifted data is set back in the X Register during T9 time when LMWE. F) is true. During T10T11T12 time the FL Register is again sourced and the value of the FL is decremented by 1. The results of FL-1 is gated to the MEX latched in LBUF at T13 time and written back in the FL Register when LMEW. . FO is true. Assuming neither FL = 0 is true at S1 time and MSBX = 1 is true at S3 time, the sequencer is reset to zero at S6 time and the foregoing will repeat.

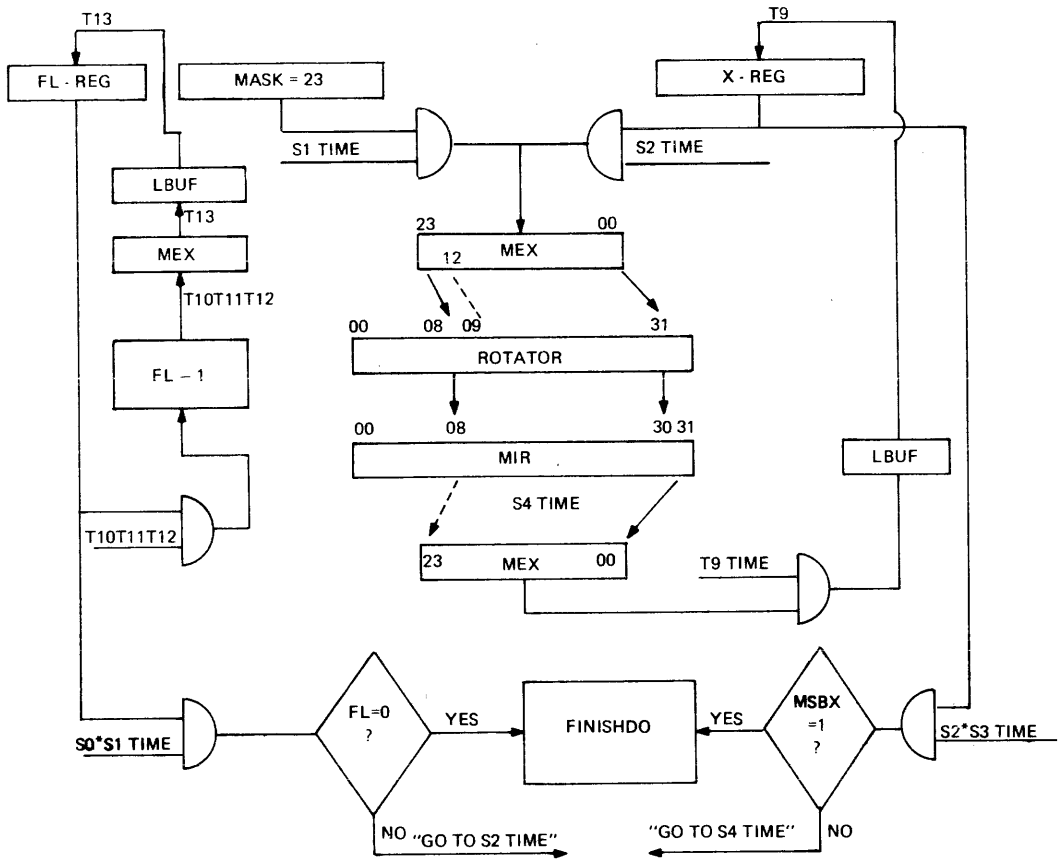


Fig. II-188 3F MICRO DATA FLOW & DECISION FLOW

TIMING (Refer to Figure II-189)

The 3F Micro will cause the sequencer to sequence from S0 to S6 time (7 clock periods) and will continue to repeat this sequence until either FL = 0 or MSBX = 1. FL = 0 is tested at S1 time, therefore if true during S1 time, FINISHDO will occur and the next Micro will be set in the M Register and executed at which is illustrated in Figure II-183 as S3 time. MSBX = 1 is tested at S3 time, and if true will generate FINISHDO at S3 time. In this case the next Micro would be set in the M Register at S4 time as illustrated in Figure II-183. Note that when the next Micro is set in the M Register the sequencer will be reset to zero therefore S2 or S4 time would be S0 time. Regardless of the number of "repeats" of S0 to S6 time required to execute the 3F Micro, only one MFETCH operation will occur during the first S0 and S1 time. The next Micro to be executed is latched in the ML Register and held until FINISHDO occurs at which time it is set in the M Register and executed. A refresh memory cycle can occur during S5 and S6 times as shown, without interruption to the execution of the 3F Micro.

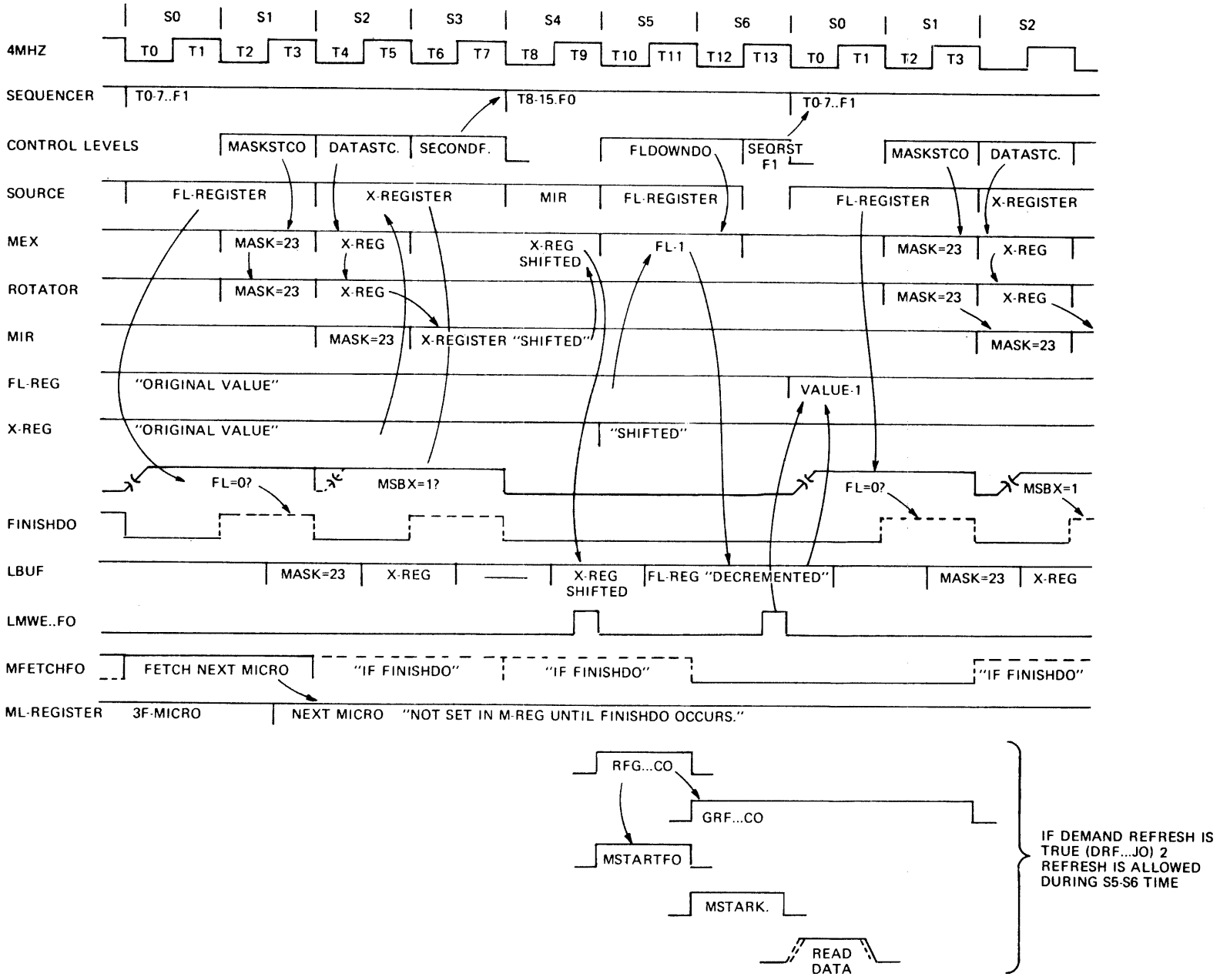

S0 S1 S2 S3 S4 S5 S6 S0 S1 S2
4MHZ
T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T0 T1 T2 T3
SEQUENCER
T0-7..F1
T8-15.F0
T0-7..F1
CONTROL LEVELS
MASKSTCO
DATASTC.
SECONDF.
FLDOWNDO
SEQRST F1
MASKSTCO
DATASTC.
SOURCE
FL-REGISTER
X-REGISTER
MIR
FL-REGISTER
FL-REGISTER
X-REGISTER
MEX
MASK=23
X-REG
X-REG SHIFTED
FL-1
MASK=23
X-REG
ROTATOR
MASK=23
X-REG
MASK=23
X-REG
MIR
MASK=23
X-REGISTER "SHIFTED"
MASK=23
FL-REG
"ORIGINAL VALUE"
VALUE-1
X-REG
"ORIGINAL VALUE"
"SHIFTED"
FL=0?
MSBX=1?
FL=0?
MSBX=1
FINISHDO
LBUF
MASK=23
X-REG
X-REG SHIFTED
FL-REG "DECREMENTED"
MASK=23
X-REG
LMWE..FO
MFETCHFO
FETCH NEXT MICRO
"IF FINISHDO"
"IF FINISHDO"
"IF FINISHDO"
ML-REGISTER
3F-MICRO
NEXT MICRO
"NOT SET IN M-REG UNTIL FINISHDO OCCURS."
RFG...CO
GRF...CO
MSTARTFO
MSTARK.
READ DATA
IF DEMAND REFRESH IS TRUE (DRF...JO) 2 REFRESH IS ALLOWED DURING S5-S6 TIME

Fig. II-189

OF MICRO (NO-OP)

The function of the NO-OP is to effectively do nothing for 2 clock periods and then execute the next sequential MICRO. A concurrent MFETCH operation will occur which fetches the next Micro to be executed from S-Memory. In a "String" of Micros written into S-Memory, the NO-OP can be used as a "black Micro" which could be substituted by other Micros without changing the context of the string. e.g., the Halt Micro could be manually loaded at the same address as a previously written NO-OP, the function of the string when executed would not change and a halt could be forced at a particular point of execution.

TIMING (Refer to Figure II-190)

A concurrent MFETCH operation occurs and with MFETCHFO true, the next sequential Micro is latched in ML and set in the M Register for execution when FINISHDO occurs.

9D MONITOR MICRO

If used, the 9D will function identical to the OF Micro (NO-OP). The intended use is to determine (via software) the time it takes to execute various routines. Logic at this time has not been implemented to perform this function.

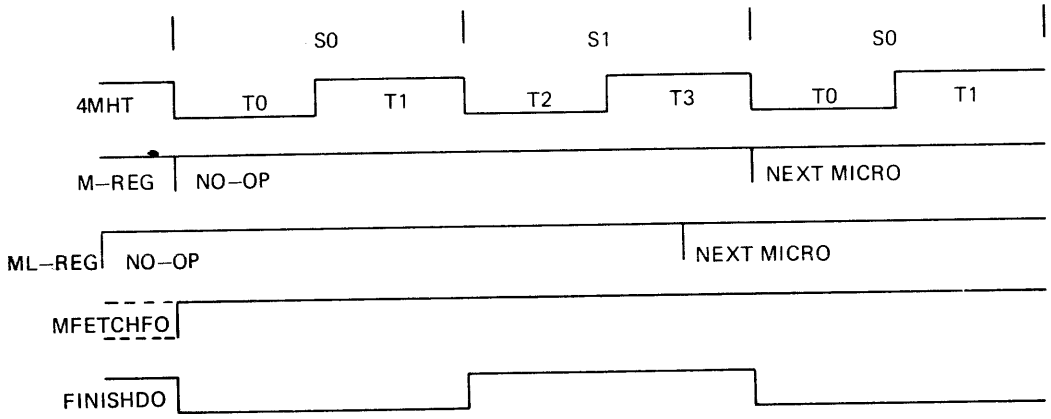


Fig. II-190 NO-OP TIMING

MEMORY

This section describes the memory base, addressing, read and/or write operations, refresh, physical characteristics, and memory data rotation.

STORAGE MEDIA

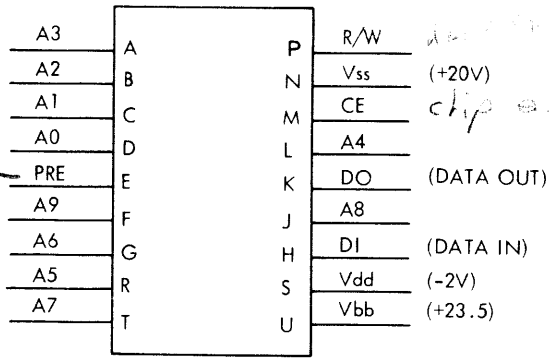
The storage media of the S-Memory is a 1024 x 1 dynamic random access MOS (Metal Oxide Semiconductor) integrated memory array.

Dynamic referring to the fact that the memory must be refreshed every 2 milliseconds or the contents of memory would be lost. Refresh is accomplished by simply reading memory and this is done by the hardware of the S-Memory Processor. This will be covered under Refresh.

The following are the eight listed characteristics of the storage element:

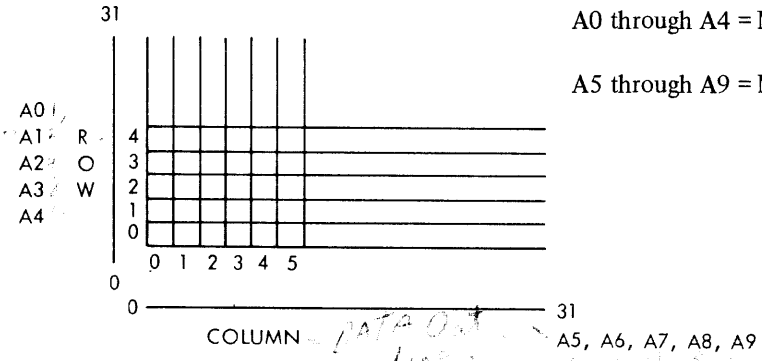
1. 1024 x 1 random access element packaged in 18 pin dip. (See figure II-191).
2. Inputs are 10 address lines A0 thru A9, Precharge Input (PRE), Chip enable (CE), Read/Write (R/W) and Data Input (DI).
3. The memory requires periodic data refreshing which is accomplished by cycling through read cycle A0 thru A4 inputs. This operation must be performed at least every 2 milliseconds.
4. Cell readout is NONDESTRUCTIVE.
5. Data Written in the memory element is inverted at the output.
6. For interfacing with the CTuL logic, drivers are used at the input, and sense amplifiers at the output.
7. The memory outputs offer the possibility of wire-or connection, and this characteristic is used on the storage cards.
8. Maximum read access time measured from the address, or negative going edge of the precharge, is 300 NS.

Figure II-191 shows the 18 pin dip storage element:



√ Fig. II-191 DYNAMIC MOS MEMORY CHIP

While the storage chip is used as a 1 x 1024 bit, the actual storage within the chip is arranged in a 32 x 32 configuration, with A0 thru A4 addressing the Row, and A5 thru A9 addressing the column. Figure II-192 illustrates the arrangement of the internal element.



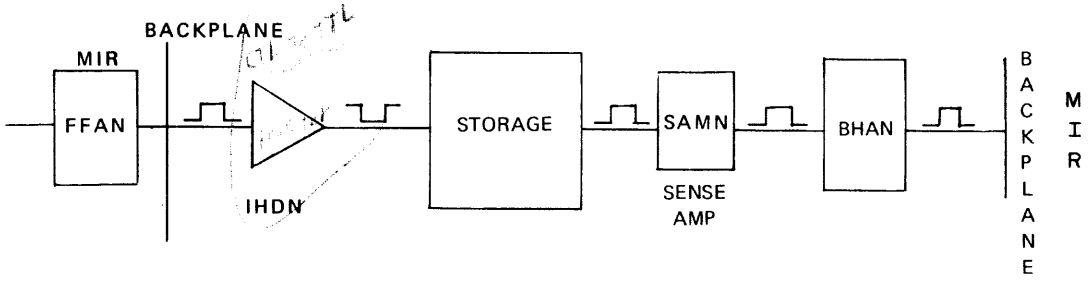
A0 through A4 = MAR 5 through 9 (ROW)

A5 through A9 = MAR 10 through 14 (COLUMN)

Fig. II-192 CHIP INTERNAL STORAGE

STORAGE CARD

The B1700 Memory Storage Card is the standard size circuit card, 11-3/4 inches by 14-1/4 inches, used within the B1700 system. The card is non-standard in the component layout as the storage card requires 125 integrated components. This is in contrast to the standard 120 components per card layout. Each card is divided into two distinct sections or otherwise referred to as modules. The storage capacity of each module being 4,096 bytes of information. The module consists of 36 storage elements arranged in a 9 x 4 array. See Figure II-162. In addition to the 36 storage elements a module consists of the necessary drivers and sense amplifiers required for interfacing the CTuL of the system to the MOS storage element. Figure II-161 is a diagram of that interface for the portion which is concerned with data only. The other inputs such as address, precharge, chip-enable and read/write are through similar circuits.



√ Fig. II-193 INTEL STORAGE CIRCUIT

Each of the 9 x 4 arrays are arranged in four rows which is a significant factor in analyzing an address to determine a malfunctioning storage element. See figure II-162.

As can be seen from Figure II-162, Module 0 and Module 1 are located on one card and Module 2 and Module 3 on another. With two cards installed the total memory is 16K Bytes and the diagram implies therefore that 16K is the

Functional Detail

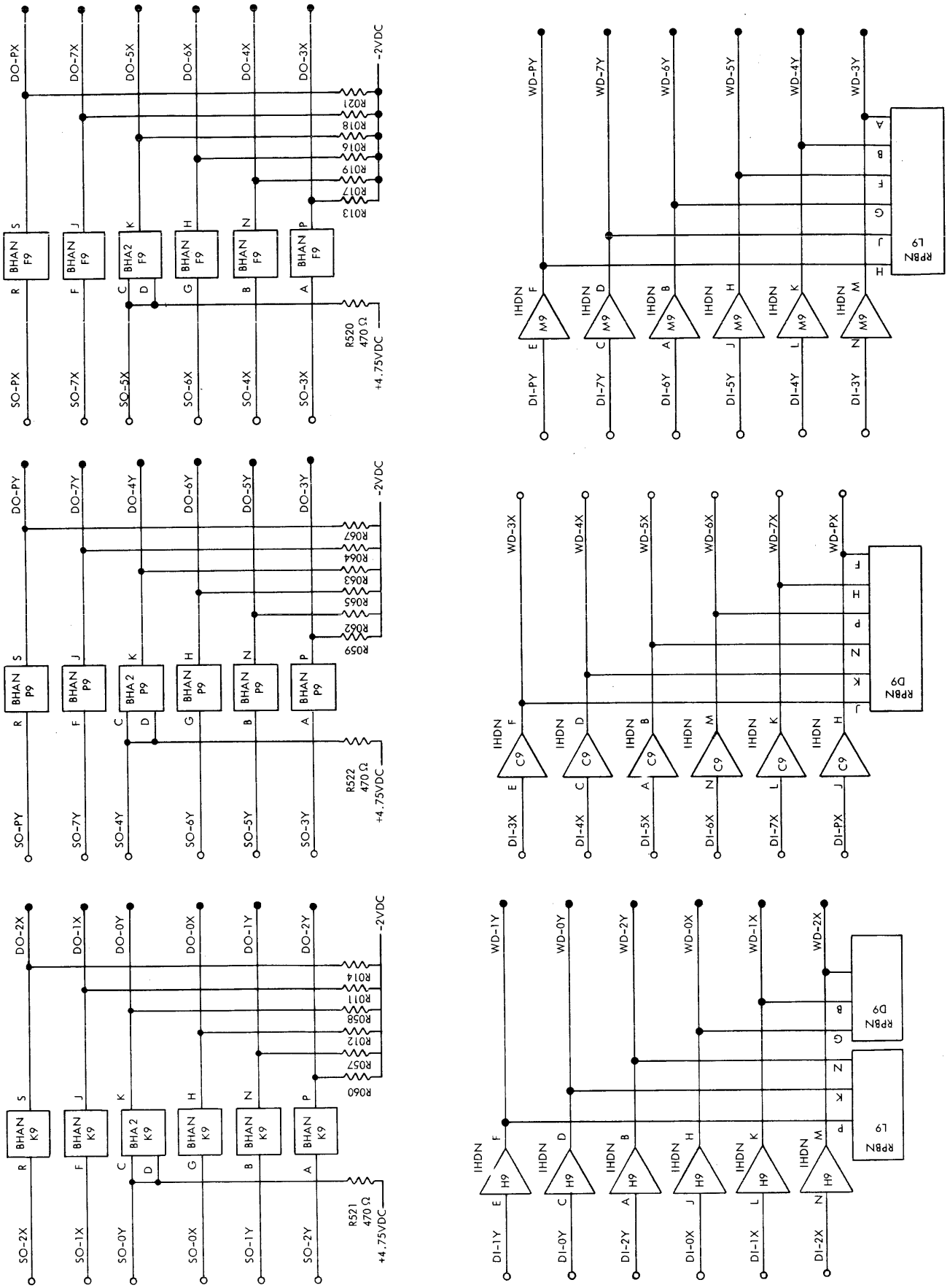


Fig. II-193A

minimum memory due to the module concept. This, however, is not true as a card may be half-populated to allow for incrementation of memory by 8K bytes. In the case of a half-populated card, each card that makes up a complete module set (Module 0, 1, 2 and 3) would contain only 4K bytes. Another point illustrated then is that when memory is expanded, it is done by adding two cards at a time. If two fully populated cards are added then memory has been incremented by 16K or if two half-populated cards are added then memory has been incremented by 16K or if two half-populated cards are added then memory is incremented by 8K bytes. Figure II-194 shows a block diagram of a storage card.

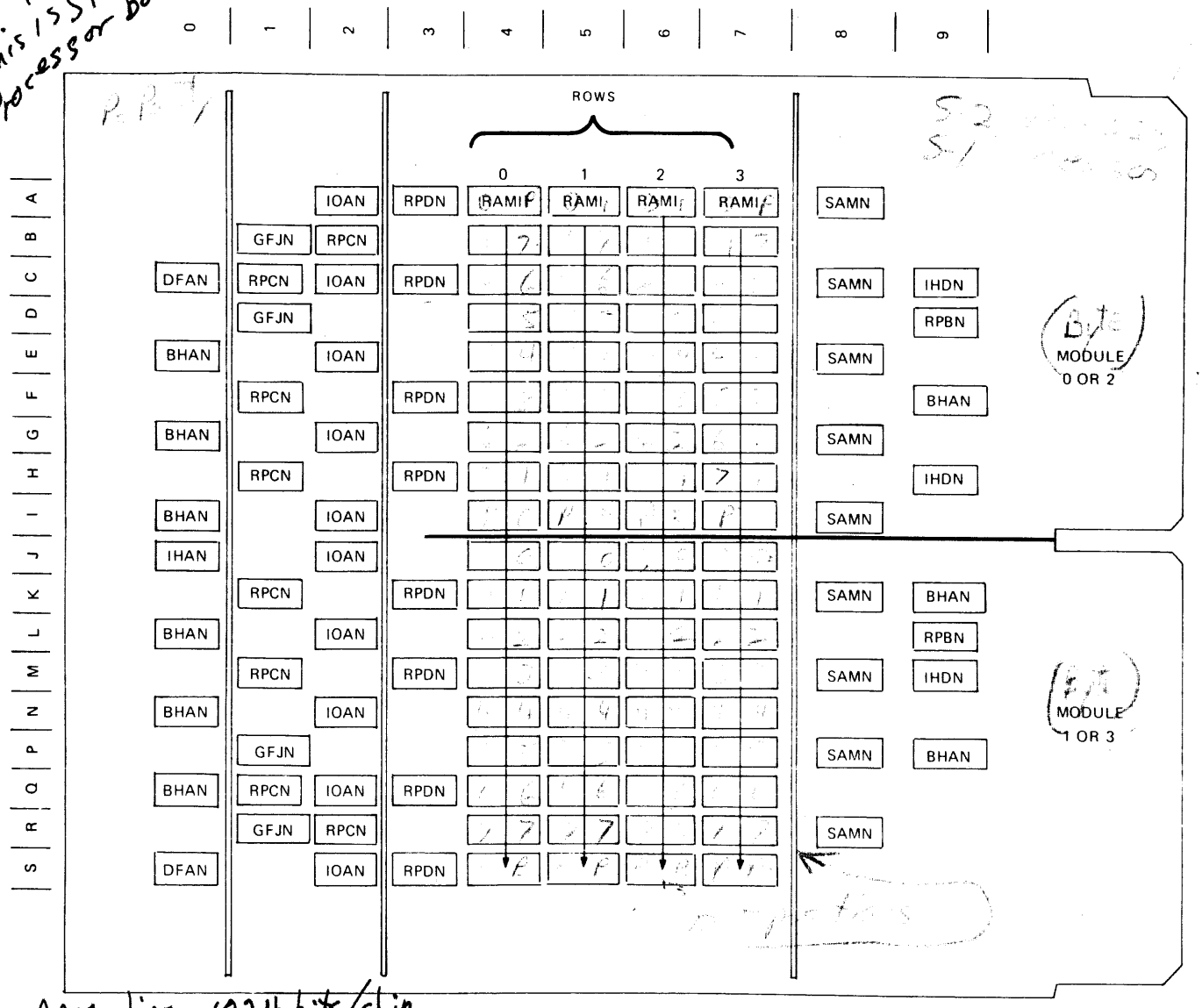


Fig. II-194 MEMORY STORAGE BOARD

MEMORY GROUP

Storage cards will alwys be installed in pairs. Due to the Module concept, Module 0 and 1 will be on one card and Module 2 and 3 will be on the second card.

MEMORY UNIT

The B1700 "S" Memory Unit of up to four card groups (eight storage cards). The minimum memory unit consists of one card group (2 cards), each card being half populated. The maximum unit will consist of four card groups of 2 cards each, with each card containing 2 Modules, each Module will contain 4096 Bytes. (4K)

Functional Detail

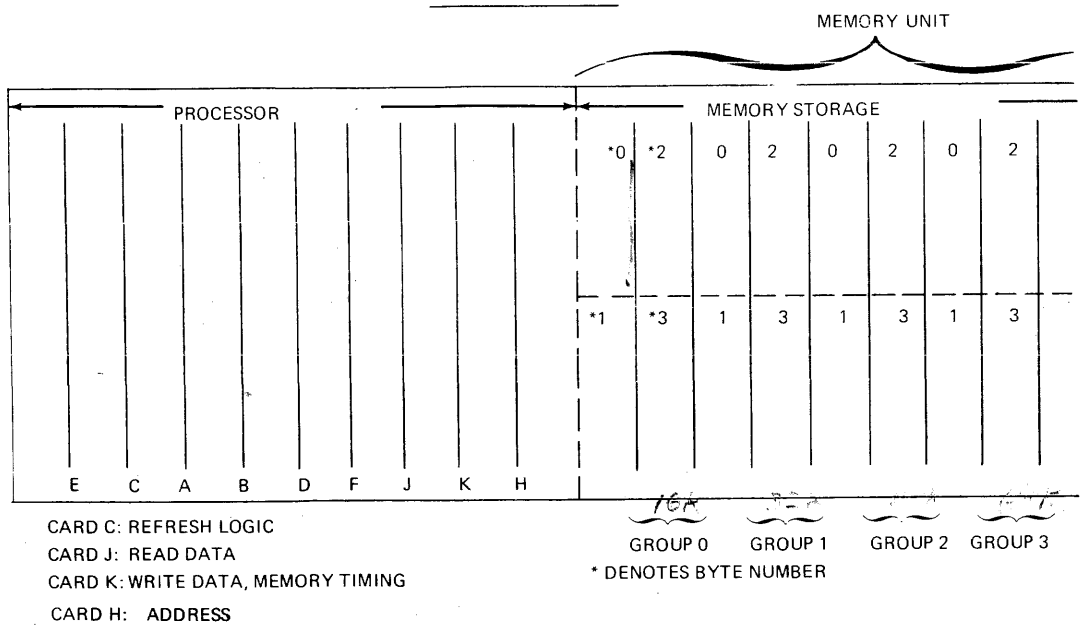


Fig. II-195 B1700 18C AND BACKPLANE LOADING

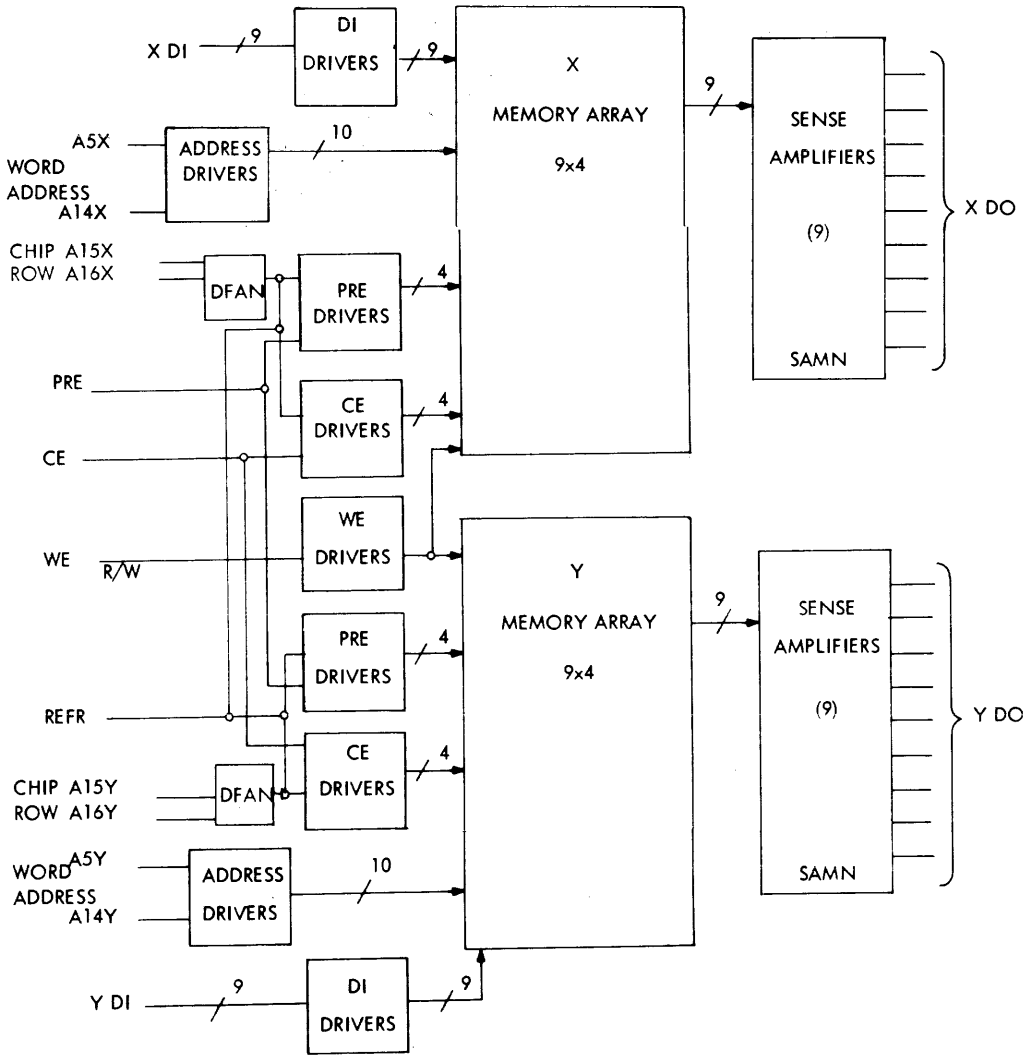


Fig. II-196 STORAGE CARD FUNCTION BLOCK DIAGRAM

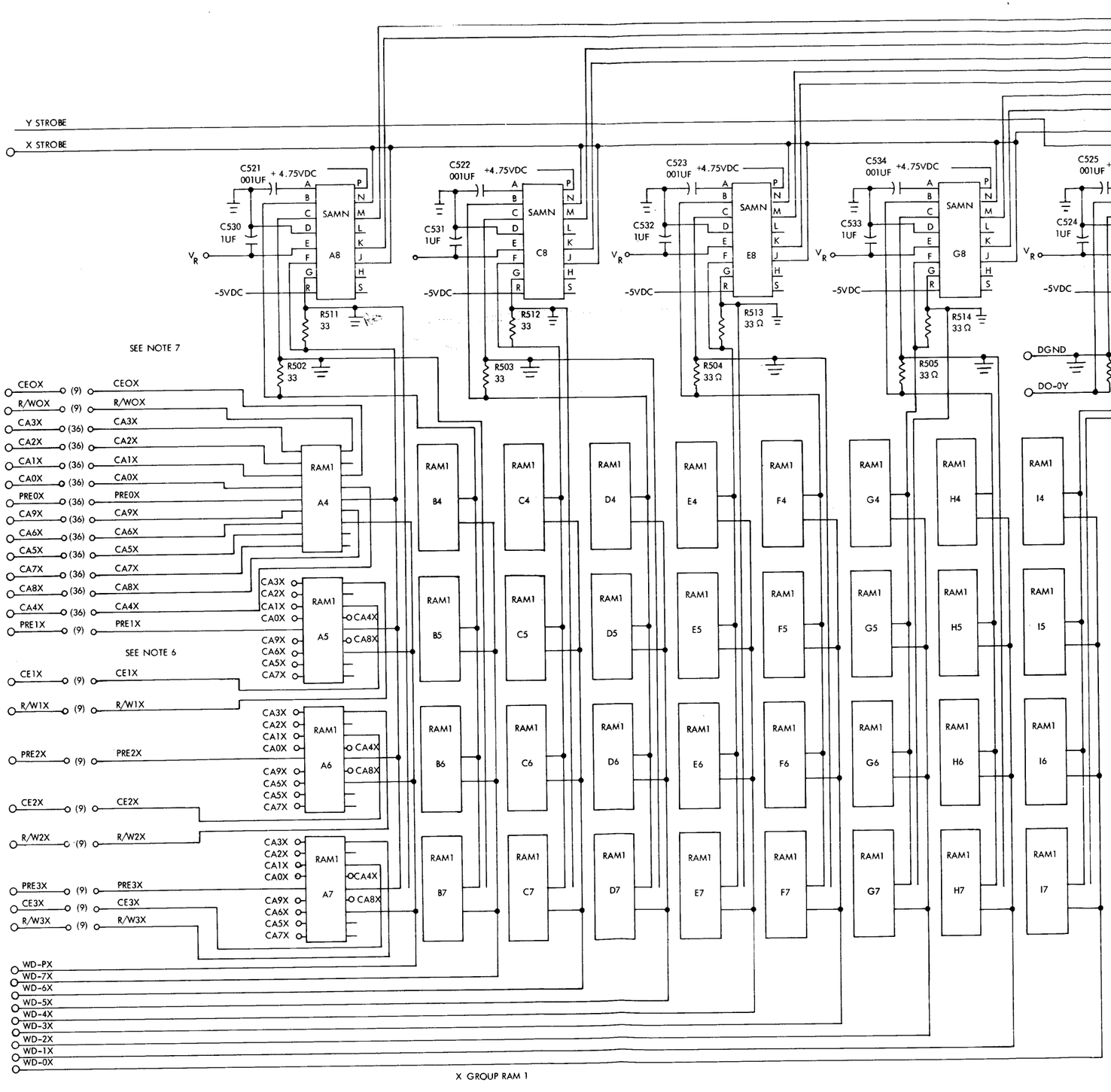

SO-7X
SO-PX
SO-5X
SO-6X
SO-3X
SO-4X
SO-1X
SO-2X
Y STROBE
X STROBE
Y STROBE
SO-0Y
SO-0X
C521 001UF
C522 001UF
C523 001UF
C534 001UF
C525 001UF
+4.75VDC
C530 1UF
C531 1UF
C532 1UF
C533 1UF
C524 1UF
SAMN
A8
C8
E8
G8
I8
V_R
-5VDC
R511 33
R512 33
R513 33 Ω
R514 33 Ω
R515 33
R502 33
R503 33
R504 33 Ω
R505 33 Ω
R506 33 Ω
DGND
DO-0Y
SEE NOTE 7
SEE NOTE 6
CEOX (9)
R/WOX (9)
CA3X (36)
CA2X (36)
CA1X (36)
CA0X (36)
PREOX (36)
CA9X (36)
CA6X (36)
CA5X (36)
CA7X (36)
CA8X (36)
CA4X (36)
PRE1X (9)
CE1X (9)
R/W1X (9)
PRE2X (9)
CE2X (9)
R/W2X (9)
PRE3X (9)
CE3X (9)
R/W3X (9)
RAM1
A4
A5
A6
A7
B4
B5
B6
B7
C4
C5
C6
C7
D4
D5
D6
D7
E4
E5
E6
E7
F4
F5
F6
F7
G4
G5
G6
G7
H4
H5
H6
H7
I4
I5
I6
I7
WD-PX
WD-7X
WD-6X
WD-5X
WD-4X
WD-3X
WD-2X
WD-1X
WD-0X
X GROUP RAM 1

Fig. II-196A

MEMORY ADDRESSING

The B1700 Memory is addressed by a Memory Address Register in the S-Memory Processor which consists of 19 bits of address. Of the 19 address bits, only the significant 14 are sent to memory. The address contained in MAR(A) is either an address for data, or an address from which a micro is to be obtained. Another address which may be generated and will be discussed separately is the Refresh Address, which is not stored in the MAR(A) Register. Using the above information, it can be seen that memory is addressed for one of three reasons which are listed as follows:

1. Address for read/write data
2. Address for M Fetch (Obtain micro)
3. Address for memory refresh every 2 milliseconds

The major difference between the data address and the M Fetch address is that the data address uses the least significant three bits of the total 19 which are sent to the data rotation circuitry. On the other hand, the M Fetch completely ignores those least significant three bits as rotation of the micro is not required. Rotation is not required on the M Fetch, as the address is on byte boundaries. A M Fetch will always start at module 0 and include module 1, 2, and 3 in that order. The following discussion concerns itself only with the memory addressing and not with the data.

As can be seen in Figure II-197, the B1700 or S-Memory Processor addressing logic consists of the MAR(A) Register, Address Modification Logic, Address Distribution Logic and Address Distribution Control Logic. The functions and operation of each of these sections are described individually.

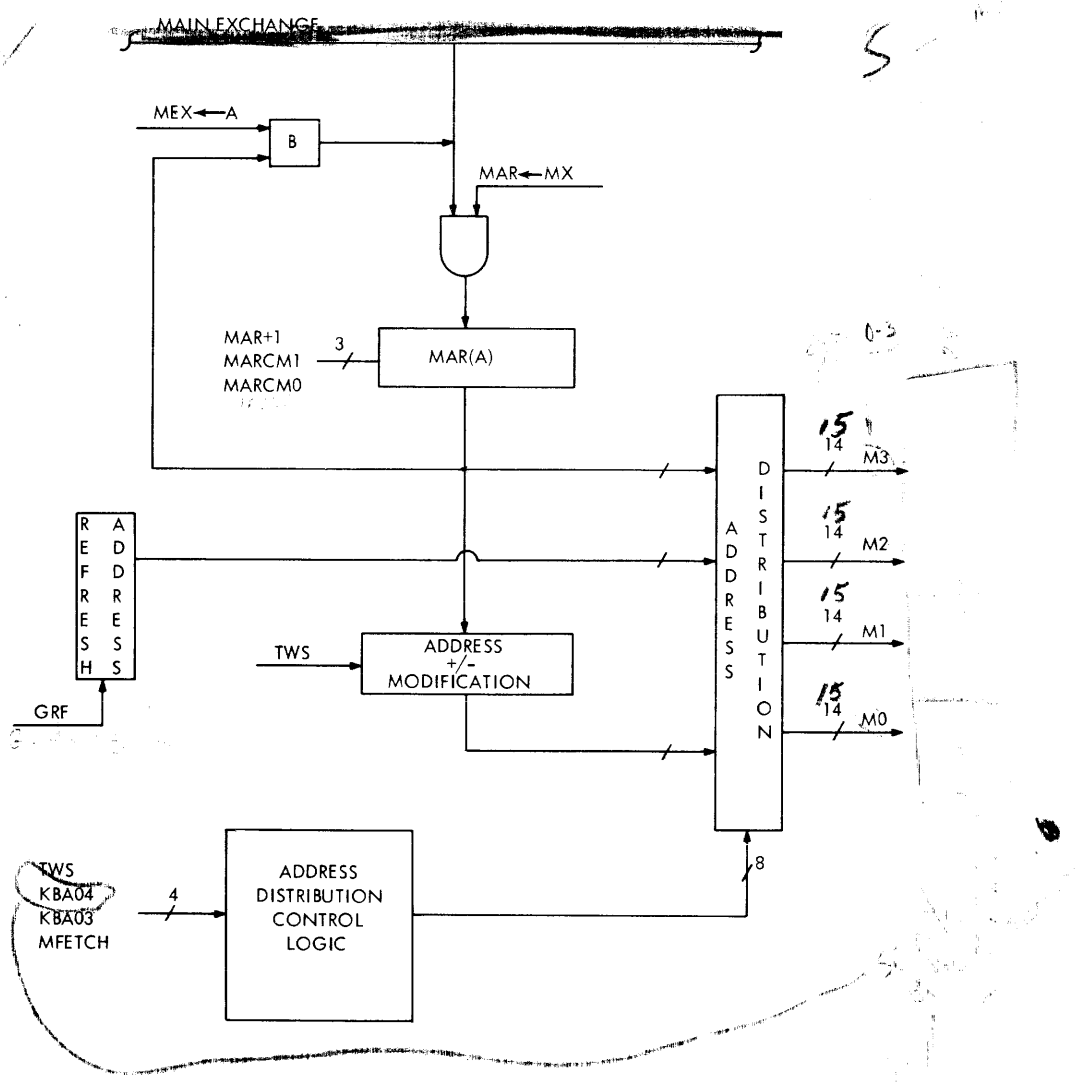


Fig. II-197 S-MEMORY ADDRESSING

MEMORY ADDRESS REGISTER

The Memory Address Register is a 19 bit register which is shared by two functions within the S-Memory Processor. In one instance, it is used as an address register which points or addresses micros in S-Memory, and in the other case it is used as a storage register to contain the address data in memory which is to be read/written with the 7C Read/Write memory micro instruction. When used with the 7C micro to address data, the contents of the FA (Field Address Register) Register are transferred to MAR(A) and the contents of MAR(A) are stored in a temporary buffer (TEMP B) within the local memory. Upon completion of the 7C micro, the address stored in TEMP B is returned to MAR(A) which is then the address of the next micro. It can, therefore, be seen that the MAR(A) normally contains a micro instruction address, and when a read/write memory is commanded then the contents of MAR(A) is replaced with the memory data address (FA Register).

MAR(A)'s most significant 16 bits, which are the key byte address, are located on S-Memory Processor Card H, and the least significant three bits are located on Card K. The least significant three bits are not sent to memory, but are used within the Rotation Logic to rotate the data so that on a memory write, the data will be rotated in a manner such that the least significant bit of the data register will be written into the most significant address location. On a read, it will rotate the data so that the bit in the most significant address location will be stored in the least significant bit location of the data register. The operation of the Rotator is discussed in the data flow portion of the S-Memory Description.

Figure II-198 diagram shows the bits of the MAR(A) Register and their significance, in order to determine the actual location of a component on a storage card.

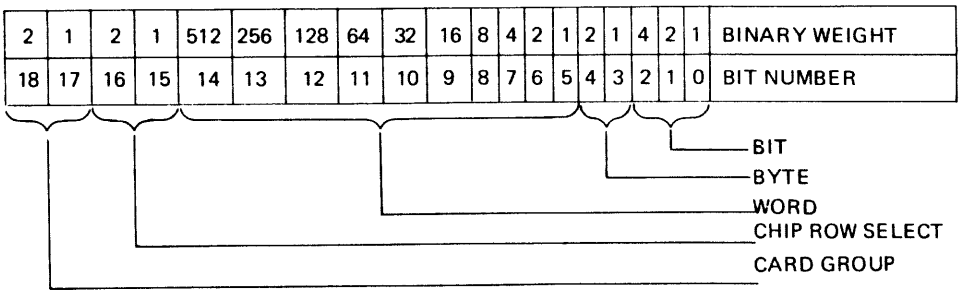


Fig. II-198 MAR-REGISTER BIT SIGNIFICANCE

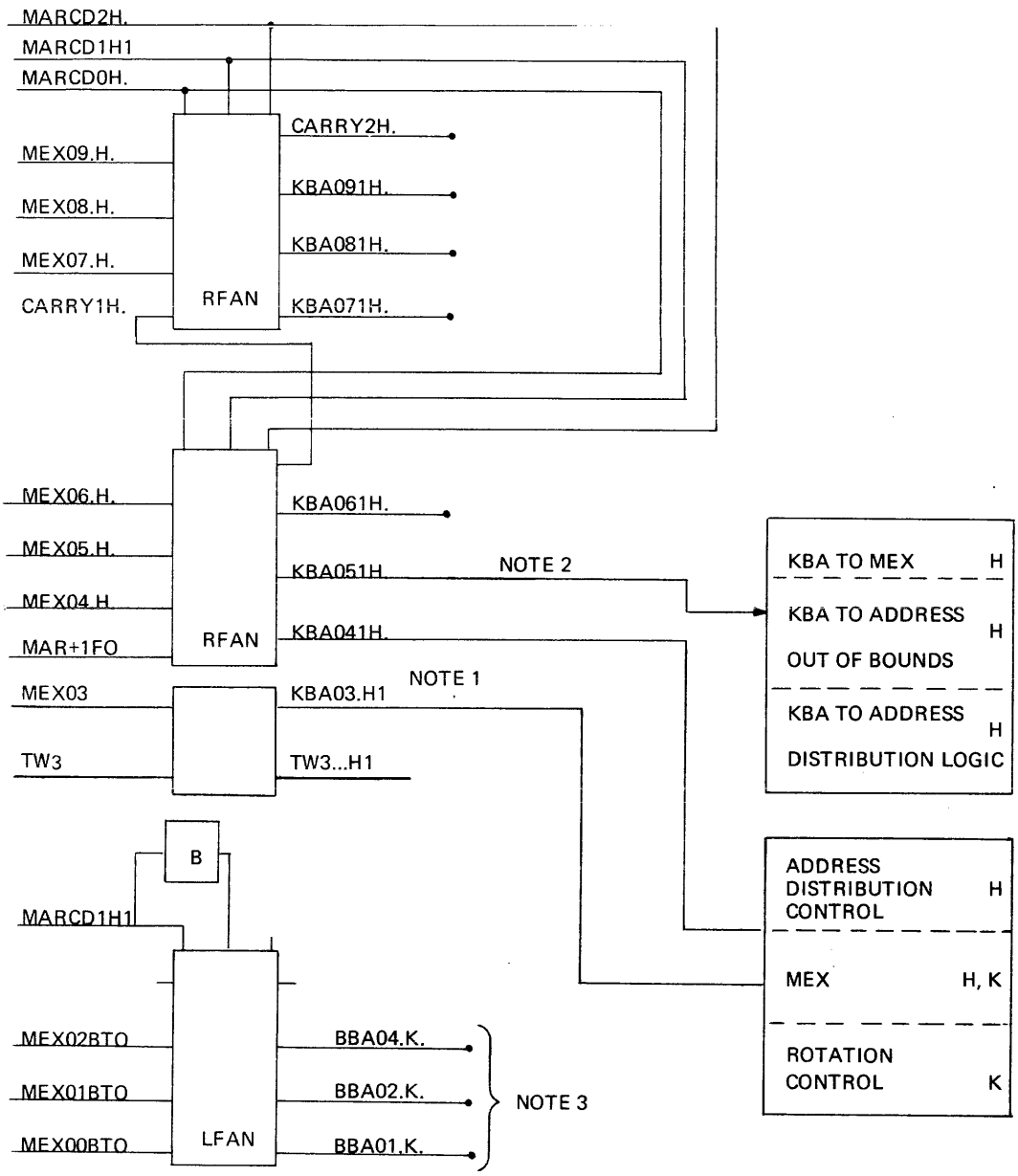
The Memory Address Register as shown in Figure II-200 has outputs to the Main Exchange Address Modification Logic and to the address distribution Logic. The MAR(A) Register itself is controlled by the three mode lines which cause the MAR(A) Register to be placed in the Add Mode, Subtract Mode, D Set Mode or NO-OP Mode. The Add Mode is used for normal incrementation of MAR(A) when used as a micro address register or may be used when a Branch Relative in a forward direction is called for by a micro instruction. The Subtract Mode of the MAR(A) is used when a Branch Relative in a negative direction is decoded. In this case a value will be subtracted from the contents of MAR(A). The D-Set Mode is enabled when the MAR(A) is designated as a destination for a Register Move type micro and will cause the contents of the MAR(A) to be replaced with the value on the Main Exchange. Figure II-199 lists the mode lines and the action they will cause for the MAR(A) Register:

ISOLATH	MARCD1H1	MARCDOH	ACTION
0	0	0	NO OPERATION
0	1	0	D-SET
1	0	0	ADD
1	0	1	SUBTRACT

√ Fig. II-199 MAR(A) REGISTER MODE CONTROL LINES

NOTE: The least significant three bits of the MAR(A) are located on Card K and only receive the MARCD1H1 term. Therefore, the least significant three bits may only be D-Set as there is not any need to ADD or SUBTRACT to these bits.

Functional Detail



NOTE 1 KBA03 BECOMES BBA08 ON CARD K
NOTE 2 KBA05 THRU KBA18 INPUT TO FUNCTIONS SHOWN
NOTE 3 BBA0M.K. USED IN ROTATION CONTROL ON OUTPUT TO MEX ON CARD K

Fig. II-200 MEMORY ADDRESS REGISTER

The MAR+1 logic is developed from the S-Memory Processor Control Logic and is generated as a result of a micro finishing. The MAR+1 term (MAR+1. FO) is sent to KBA04 of the MAR(A) in order to upcount the MAR(A) by 16 bits or in other terminology by one micro instruction word. This is ONLY done when MAR(A) is used as a micro address register.

ADDRESS MODIFICATION LOGIC

The function of the Address Modification Logic, located on S-Memory Processor Card H, is to either add or subtract one word from the Key Btye Address that is contained in the MAR(A) Register. If the Transfer Width Sign (TWS) indicates a positive or forward direction then an add of the word address in MAR(A) plus one occurs or conversely if the TWS indicates a negative or reverse field direction then a subtract of one from the contents of MAR(A) occurs.

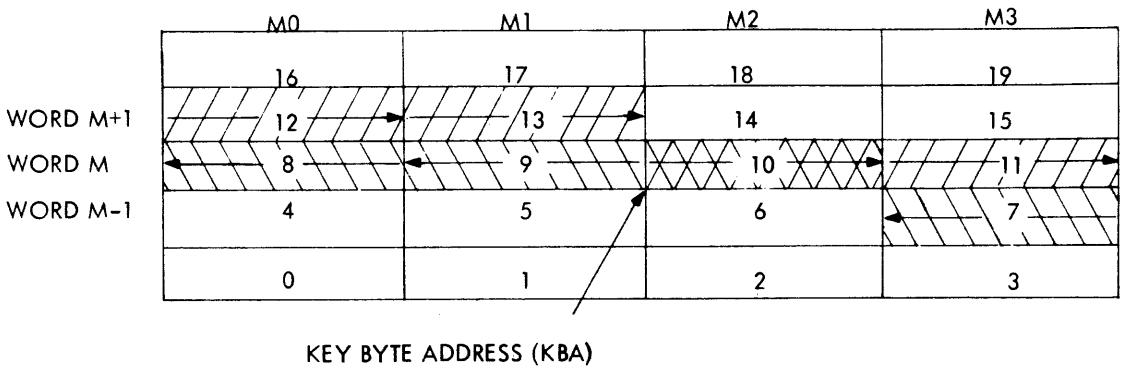


Fig. II-201 KEY BYTE ADDRESS (KBA)

In Figure II-201 the Key Byte Address is byte ten.

If the field direction is positive then the Address Modification adds one to the KBA. It is then the function of the Address Distribution Logic to send the KBA address (Word n) to Modules two and three (10 and 11) and the KBA plus one word address (Word + n) to Modules zero and one (12 and 13). Conversely speaking, if the KBA is at the same address and a negative field direction is indicated then the logic will generate a KBA Address at Word n for Modules Zero, One and Two (10, 9 and 8) and with a subtraction by the logic, distributes the address (Word - n) to Module Three (7). It should be noted at this time that the addition or subtraction always occurs and it is the function of the Address Distribution Control to determine whether the modified or the unmodified address is to be used. Figure II-202 shows actual logic of the address modification adder-subtractor.

Functional Detail

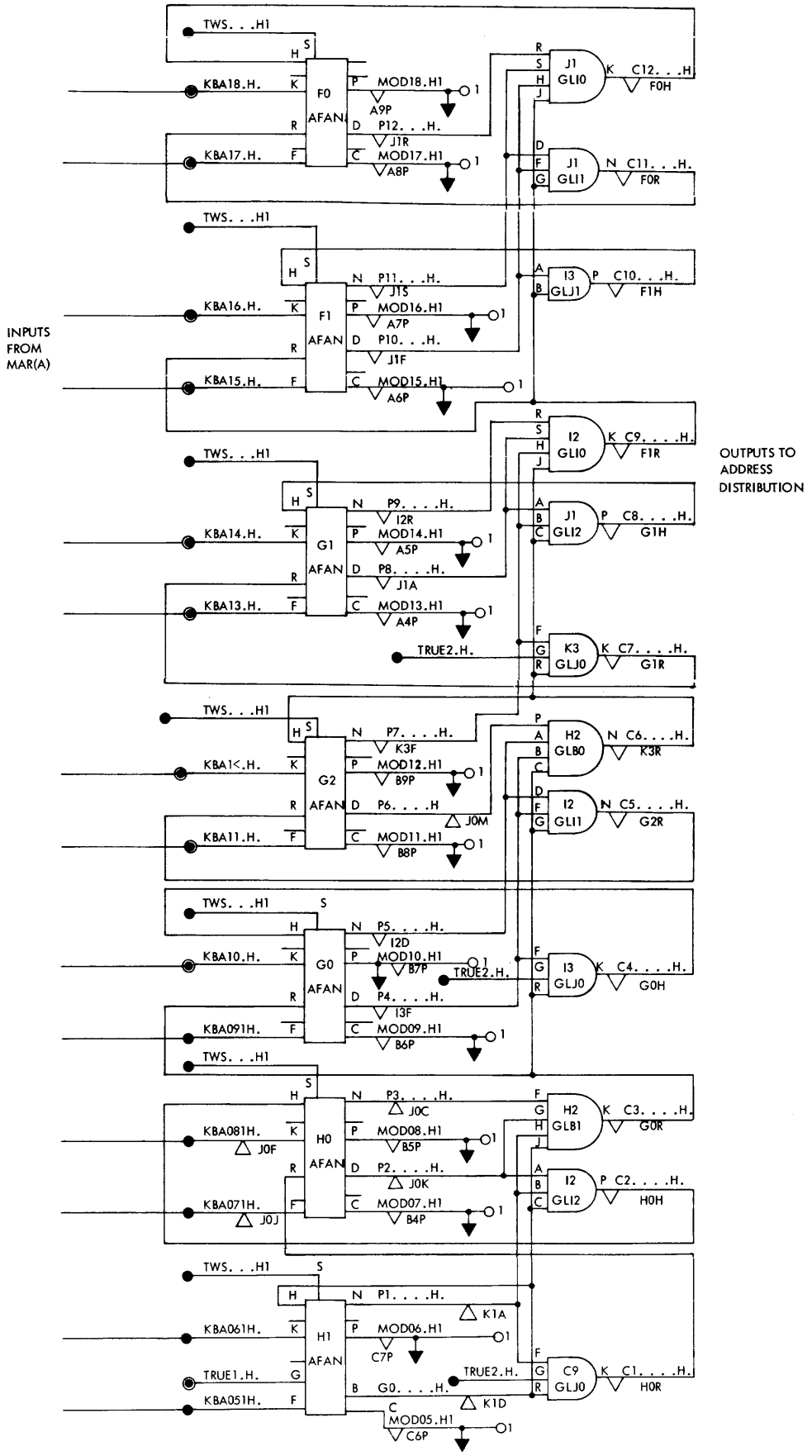


Fig. II-202 ADDRESS MODIFICATION ADDER-SUBTRACTOR

TWS	KBA04	KBA03	MODULE 0	MODULE 1	MODULE 2	MODULE 3	
0	0	0	WORD n	WORD n	WORD n	WORD n	POSITIVE FIELD DIRECTION
0	0	1	WORD n+1	WORD n	WORD n	WORD n	
0	1	0	WORD n+1	WORD n+1	WORD n	WORD n	
0	1	1	WORD n+1	WORD n+1	WORD n+1	WORD n	
1	0	0	WORD n	WORD n-1	WORD n-1	WORD n-1	NEGATIVE FIELD DIRECTION
1	0	1	WORD n	WORD n	WORD n-1	WORD n-1	
1	1	0	WORD n	WORD n	WORD n	WORD n-1	
1	1	1	WORD n	WORD n	WORD n	WORD n	

Fig. II-203 ADDRESS MODIFICATION CHART

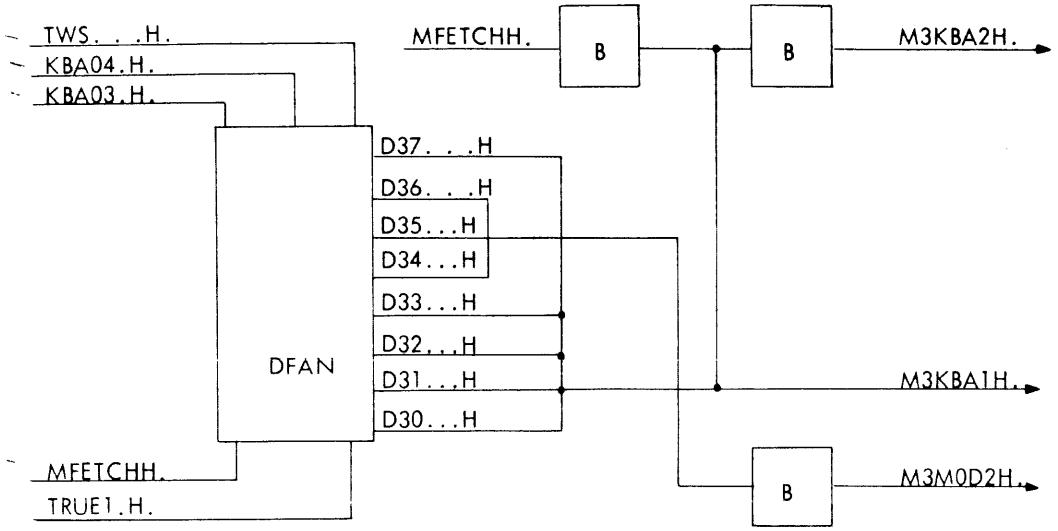


Fig. II-204 ADDRESS DISTRIBUTION CONTROL

ADDRESS DISTRIBUTION CONTROL

It is the function of the Address Distribution Control to determine what address each of the four memory modules are to receive. The four inputs to the Address Distribution Control are the Transfer Width Sign, the M Fetch term and the Memory Address Register bits KBA03 and KBA04. From these inputs the logic can determine which address is to be sent to the various modules. The module may receive the Key Byte Address as contained in MAR(A) or may receive the modified Key Byte Address. If the memory operation is an M Fetch then the operation will automatically cause the Key Byte Address (KBA05 to KBA18) which is in MAR(A) to be sent to Memory.

Figure II-203 defines the address that is sent to each of the four modules if the operation is not an M Fetch.

The diagram shown in Figure II-204 is a typical example of the logic which determines the address to be sent to a specific module. The example shown is for Module Three. If the address is to be sent without modification, then the term M3KBA1H1 and M3KBA2H1 are true. If the address is to be modified then the term M3MOD2H. is generated which will cause the output of the Address Modification Logic to be selected in place of the MAR(A) contents. Note that if the memory operation is an M Fetch then the term MFETCHH. will be true which disables the DFAN and through buffers causes the terms M3KBA1H1 and M3KBA2H. to be generated to select the address in MAR(A) to all modules.

ADDRESS DISTRIBUTION

The Address Distribution Logic sends fourteen address lines to each of the four memory modules (KBA05 - KBA18). The Address Distribution Logic is controlled by the Address Distribution Control Logic which will enable either the address in MAR(A) or the Modified Address to be sent to memory. Another function of the Address Distribution is to distribute a Refresh Address to the four memory modules if a refresh cycle is granted. In this case the refresh address is sent in place of the address in MAR(A) or a modified address. Figure II-205 shows the Address Distribution Logic for one of the fourteen address lines.

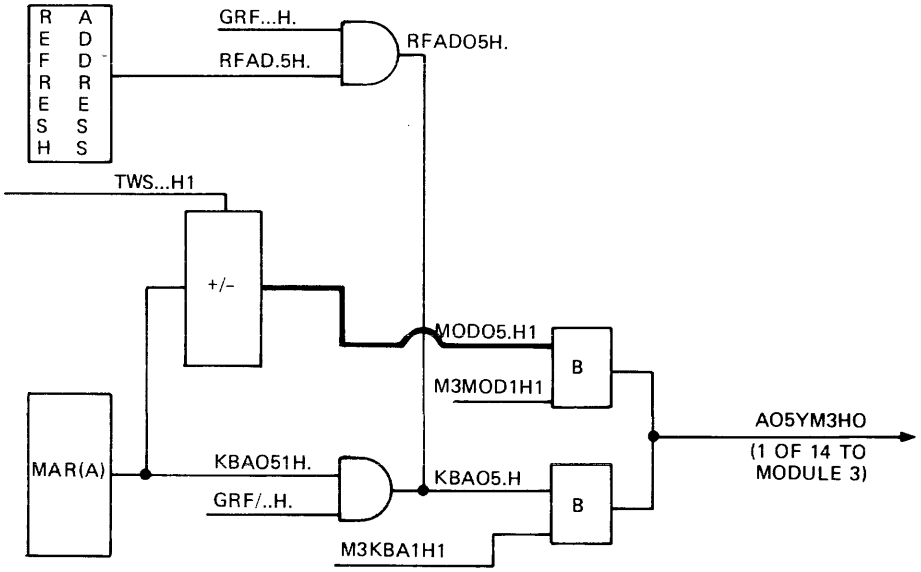


Fig. II-205 ADDRESS DISTRIBUTION

MEMORY REFRESH

A Memory Refresh must be accomplished because of the dynamic storage element. The refresh is accomplished by simply doing a read of the memory. The read is done by cycling a refresh address which only addresses the column portion of the storage element (see Figure II-192). The column is addressed by lines AO0 thru AO4. By using AO0 thru AO4 there are five bits which give a total of 32 unique address combinations. Memory is, therefore, refreshed by doing 1/32 portions of memory of each refresh cycle. Because each of the 1/32 portions must be refreshed every two milliseconds a refresh is demanded approximately every 62 usec at which time 1/32 of memory is refreshed. A refresh cycle would occur for that same 1/32 portion of memory approximately 1.984 milliseconds (32 x 45 usec = 1.984 milliseconds) later which falls within the 2 millisecond requirement. The repetition rate of the refresh is controlled by two free-running multivibrators which will produce a 2 usec pulse every 62 usec. When the pulse occurs a refresh cycle is DEMANDED. Figure II-206 shows the two free-running multivibrators and the setting of the Demand Refresh Flip-Flop.

The following is a description of the set for the Demand Refresh Flip-Flop.

1. Every 62 micro seconds, the term RFMV1.J. will come true from the TAON and the not side, RFMV1/J. will go false. These outputs remain in their respective states for two micro seconds.
2. With the term RFMV1/J. going false and the flip-flop which has the output term RFC1. . J. being reset, the input to set the Demand Refresh Flip-Flop is true. The input being Demand Refresh Set (DRFSETJ.).
3. The first DSCP which finds DRFSETJ. true, will set the Demand Refresh Flip-Flop. Demand Refresh is then sent to the memory request logic where it will generate the necessary terms to initiate a memory cycle and generate Granted Refresh (GRF. . . CO).
4. Demand Refresh is reset when the Granted Refresh is set and upon reception of the clock which finds GRF true. The RFC1. . J. flip-flop is reset when GRF is false and the multi has timed out with RFMV1. J. going false and RFMV1/J. going true.

The timing of Demand Refresh Flip-Flop is shown in Figure II-207.

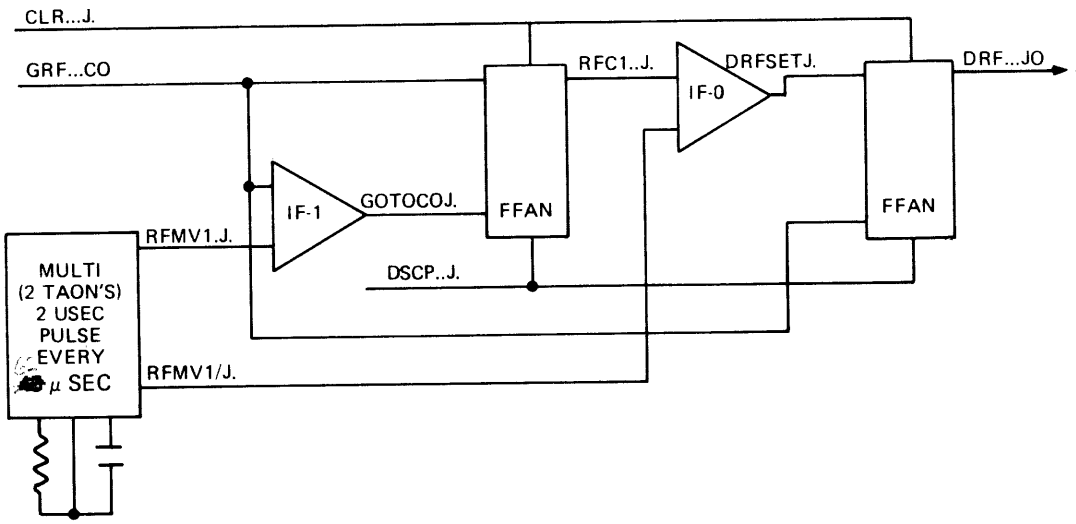
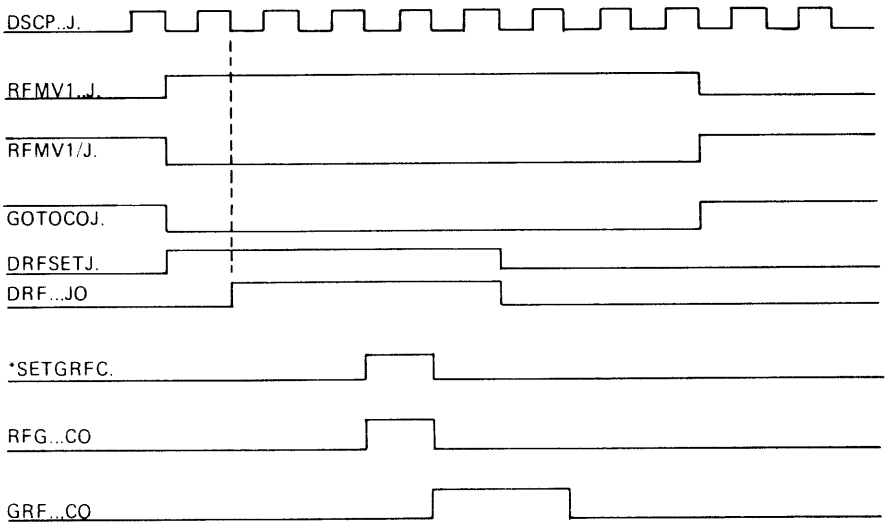


Fig. II-206 DEMAND REFRESH



*REFER TO FOLLOWING DISCUSSION FOR GENERATION OF THE SET GRANTED REFRESH LEVEL (SETGRFC.)

Fig. II-207 DEMAND REFRESH TIMING

Upon having set the Demand Refresh Flip-Flop, the output DRF. . JO is sent to the request refresh logic on Card C of the processor. Demand Refresh is gated with two terms, the first (GRINHIC) indicating the Console clear is not taking place and the second term (C/S/G/T1) indicating the Console Read/Write has not been depressed. If the gate with these three terms (See Figure II-208) is enabled then the term Demand Refresh Enable (DRFENBC.) is true and sent to two gates. The refresh at that time will be granted under one of two possible conditions. The first condition is that if DRFENBC. is true along with HLDRFRFO and at finish time (FINISHDO) for a micro then the term SET GRANTED REFRESH (SETGRFC.) will be true to cause GRF. . . CO to set. The term HLDRFRFO (Hold Refresh) would be false to prevent a refresh under three conditions. The first condition is that if the micro being executed is a move to the M Register and refresh is not allowed as the micro in the ML Register must be bit "or"-ed with the source register data. If the refresh were allowed at this time the term MLENBLFO would be false and the bit "or" would not occur. The second condition is that the micro must not be a jump. If the micro were a jump and a refresh were allowed, the jump would occur for one address past the desired address as both the refresh and jump forced NO-OP cause a MAR+1. The final condition is if the machine is to halt for any reason a refresh is not allowed as the next micro must be placed in the M Register before halting. If the refresh were allowed, the machine would not halt with the next micro in M but rather a

NO-OP in M. The second condition for setting the Granted Refresh Flip-Flop is that if the micro is a 3F NORMALIZE X, then FINISHDO may not occur for a long period of time. It is therefore necessary to provide for a refresh in the "middle" of the 3F micro. This is done by gating the Demand Refresh with a term indicating the Normalize micro (MIC.3FFO) and at a particular state of the Sequencer, S5. . . . C. time. Figure II-208 illustrates the logic required for the Granted Refresh.

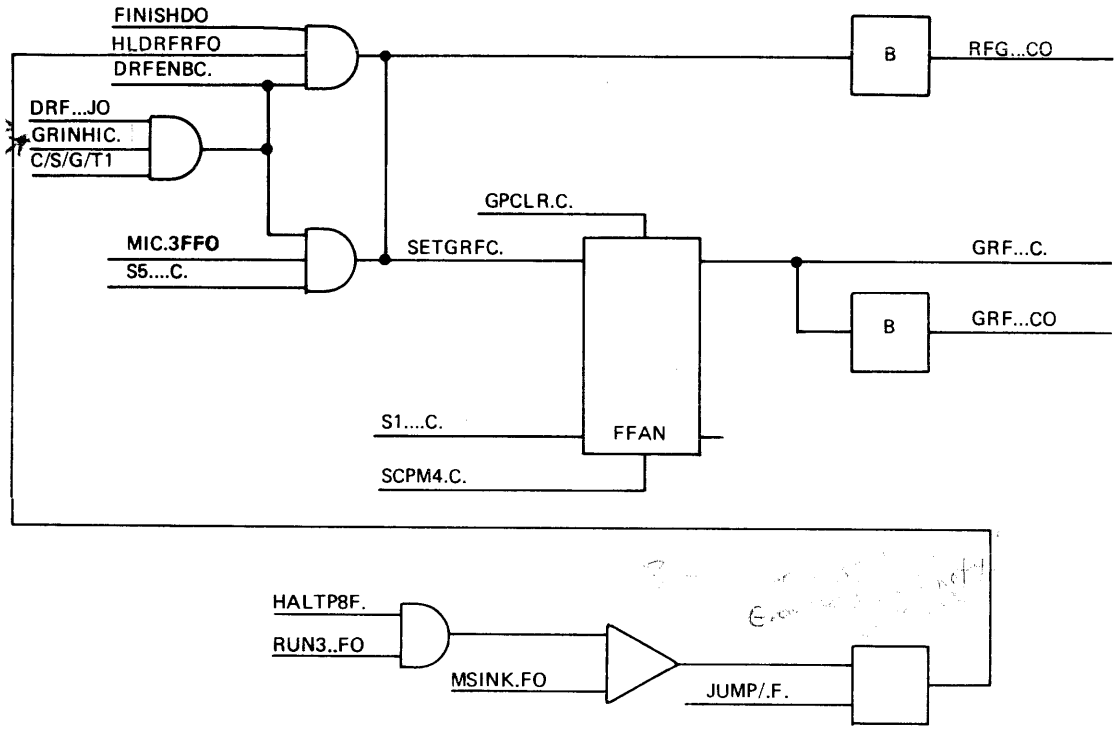


Fig. II-208 GRANTED REFRESH FLIP-FLOP

Figure II-209 in addition to showing the timing involved with the Granted Refresh shows that a NO-OP (no operation) micro is forced in place of the micro in the MLR and that the first Finish that occurs to allow the refresh will not upcount the MAR(A) Register. The operation can easily be understood by simply defining the various terms. The first term to consider the Refresh Granted (RGF. . . CO) terms. RFG. . . CO is sent to Card F where it produces MSTARTFO (Memory Start), Refresh Granted Not (FRGN/F.) false, sets the M Fetch Flip-Flop (MFETCHFO) and prevents the transfer of the MLR to the M Register. The first term mentioned, MSTARTFO, initiates the memory cycle, RFGRN/F. being false inhibits the upcount of MAR(A) and the setting of MFETCHFO allows the Refresh Address to be gated through the Memory Address Distribution Logic to the various memory modules without any modification. The actual refresh occurs during the forced NO-OP period and when the NO-OP is finished, the refresh cycle is complete and, therefore, the finish developed by the NOP can produce the normal MAR+1 and bring the micro which has been waiting in MLR into the M Register for execution

Another important term to discuss is the GRF. . . CO term which gates the Refresh Address to the Address Distribution Logic in place of MAR(A) and the trailing edge of GRF. . . CO serves as a clock to upcount the Refresh Address Generator for the next cycle which will occur.

The following timing diagram illustrates the setting and resetting of the Granted Refresh Flip-Flop (GRF. . . C.)

The final term of major importance if the CRF. . . C. term which is sent to the Console Clear logic and is used to prevent a clear while a Refresh is in progress.

The final portion of the Refresh Cycle to discuss is the actual generation of the Refresh Address which can be described by Figure II-210 of the Refresh Address Generator and an associated timing diagram. (Fig. II-211). It is important to remember that it is the trailing edge of the clock (Clock is GRF. . . CO) that upcounts the Address Generator.

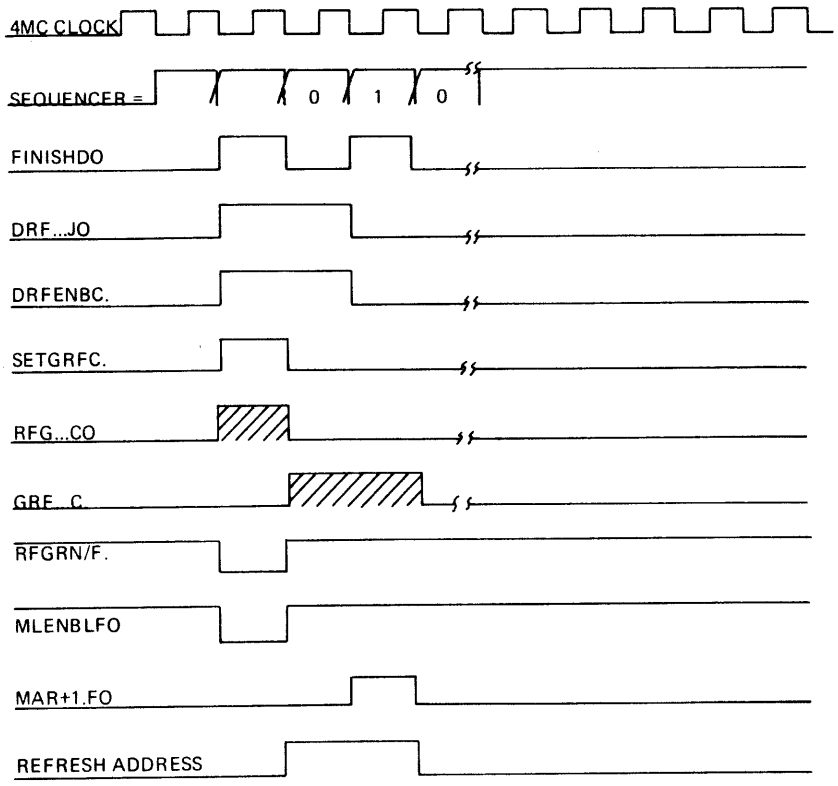


Fig. II-209 GRANTED REFRESH TIMING

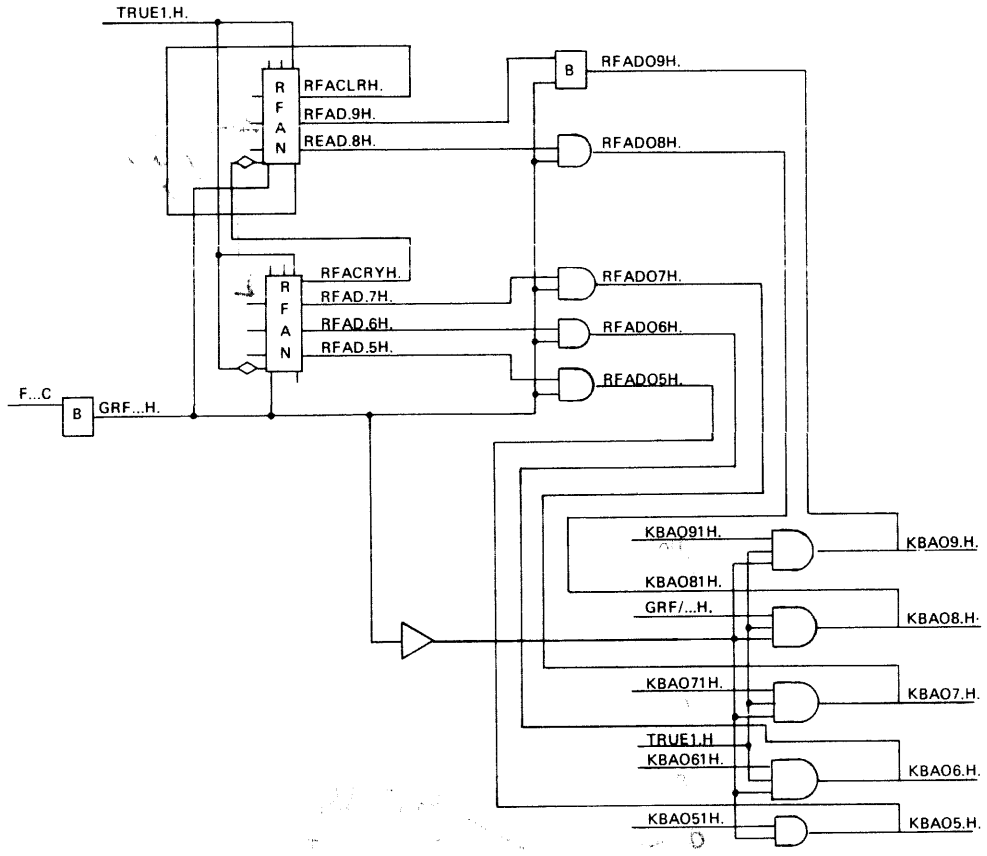


Fig. II-210 REFRESH ADDRESS GENERATOR

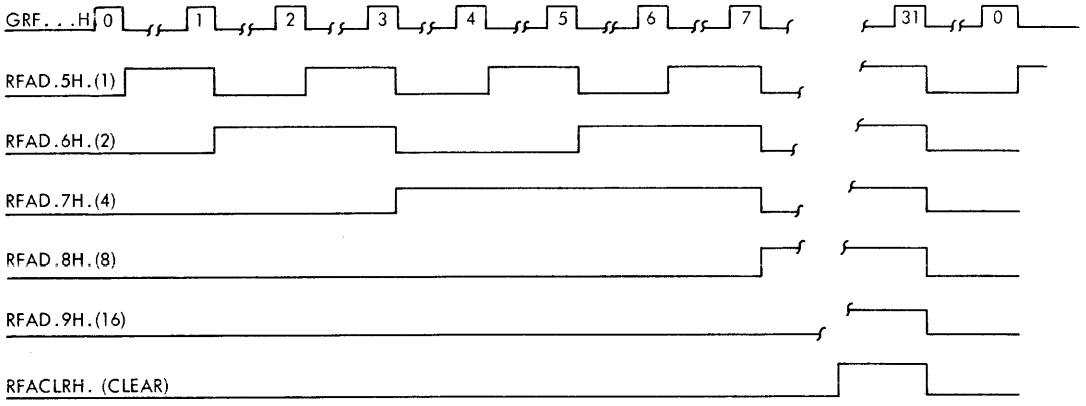


Fig. II-211 REFRESH ADDRESS TIMING

MEMORY BASE TIMING

Timing for the B 1700 S-Memory is provided for by the Memory Base Timing logic card K of the S-Memory Processor. It is the function of the Memory Base timing upon reception of the Memory Start Pulse, MSTARTFO, to supply the necessary terms to the various memory modules. The three levels that Memory Base Timing supplies are Precharge (PRECH. KO), Chip Enable (CENABLKO) and the Read/Write (RD/WT. KO). Figure II-212 illustrates the Memory Base Timing Logic.

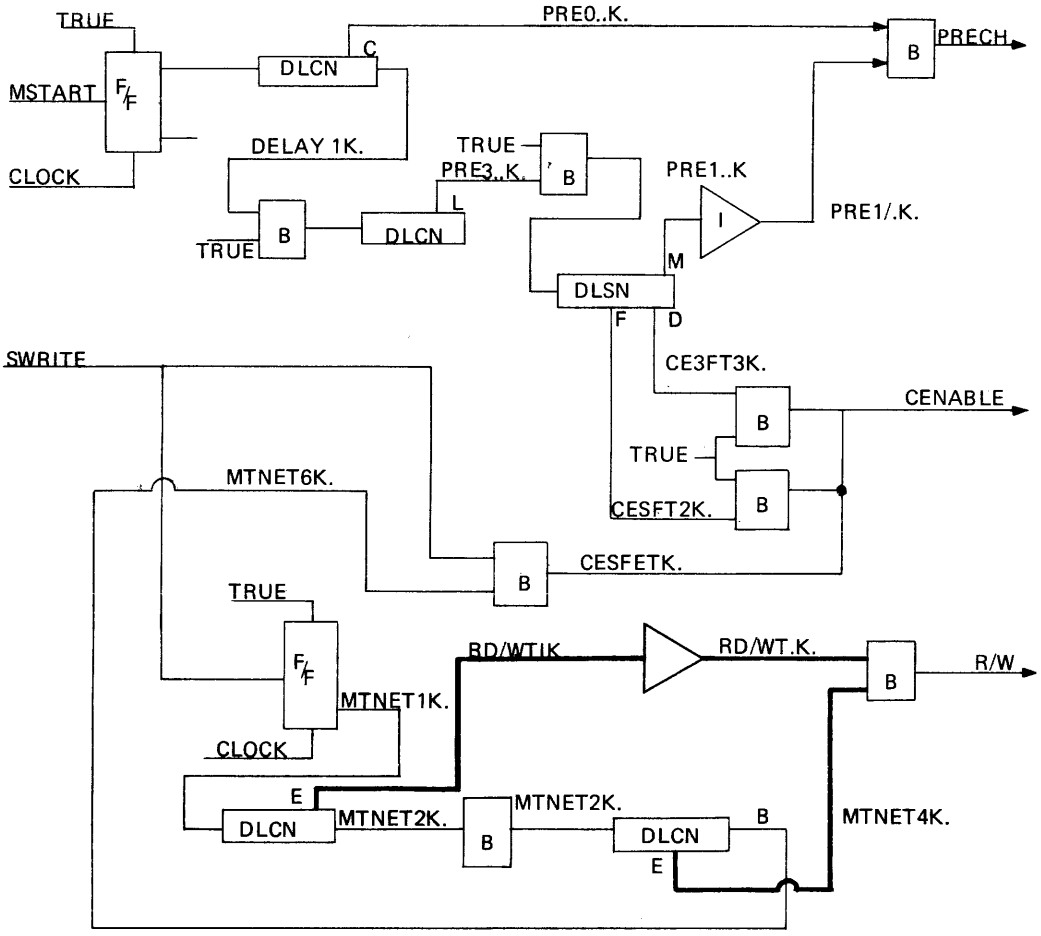


Fig. II-212 MEMORY TIMING

As can be seen from Figure II-212, all memory base timing is initiated by a Memory Start Pulse (MSTARTFO) from the S-Memory Processor Control Logic. Timing is controlled by a series of delay lines which will, at appropriate times, allow the generation of the Precharge, Chip Select and, if appropriate write enable. Fig. II-213 illustrates the Memory Base timing. The major difference between a Read and Write Cycle, as can be seen, is the Read/Write signal (RD/WT. KO) which is generated as a result of SWRITEFO from the Control Logic. If the memory operation is a read, then SWRITEFO will remain low, which will allow the memory operation to terminate at T500. Note that if the operation terminates at T500 (Read), then the Chip Enable term (CENABLKO) goes false prior to T500. However, if the operation is a Write, then the Control logic supplies the SWRITEFO signal true at T250, which extends the memory operation to T750. Because SWRITEFO is true, the timing logic produces a write level (RD/WT. KO) to the memory.

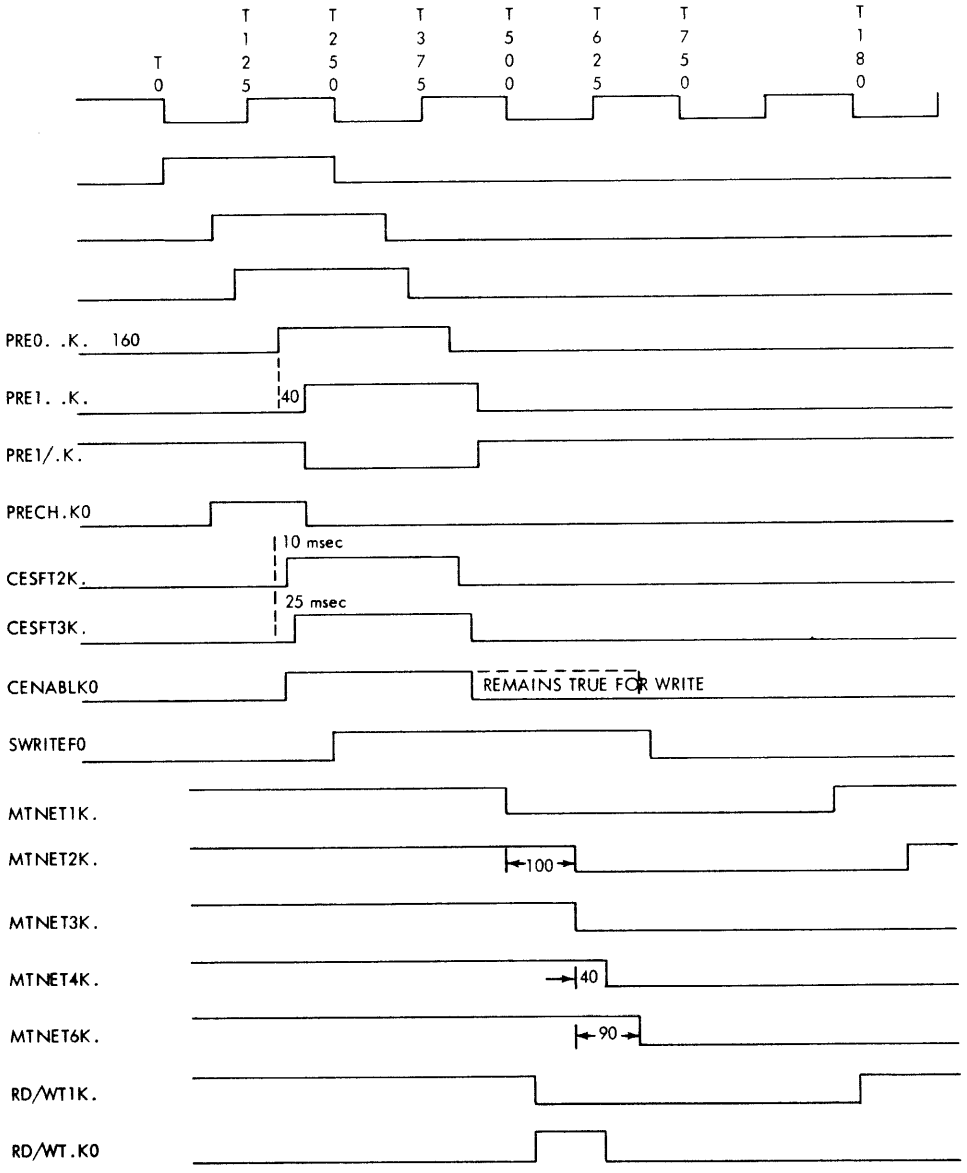


Fig. II-213

In addition, SWRITEFO and MTNET6K. will hold Chip Enable true past T500, and cause the term to go false prior to T750. For general timing on the Read refer to Figure II-214 and for Write, refer to Figure II-215. These two figures show generally when the major signals are present to memory, and also show the data times.

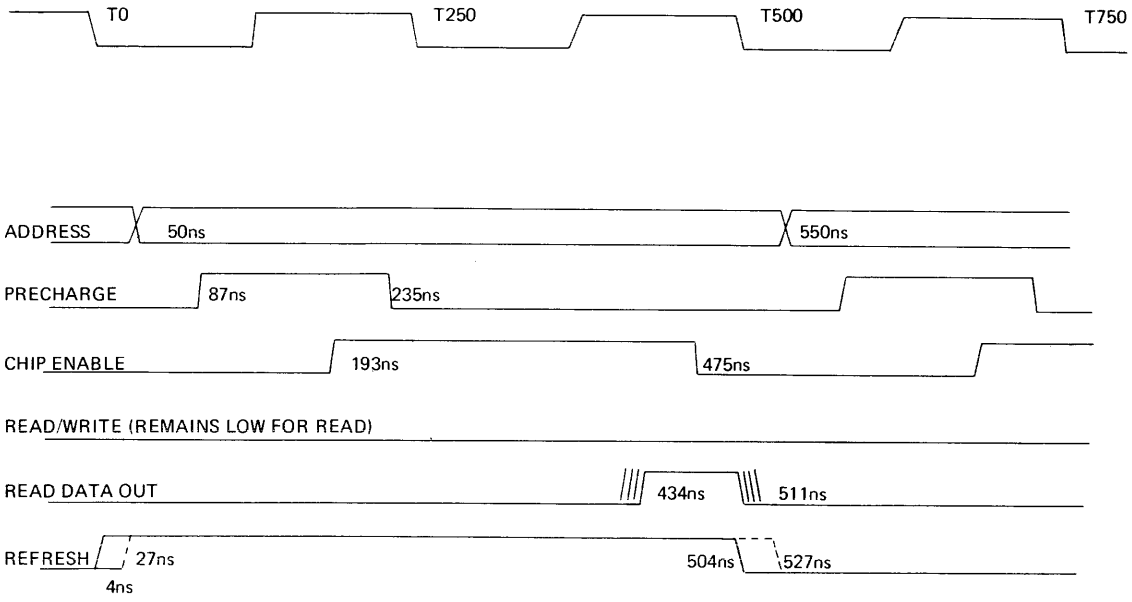


Fig. II-214 BASIC MEMORY READ TIMING

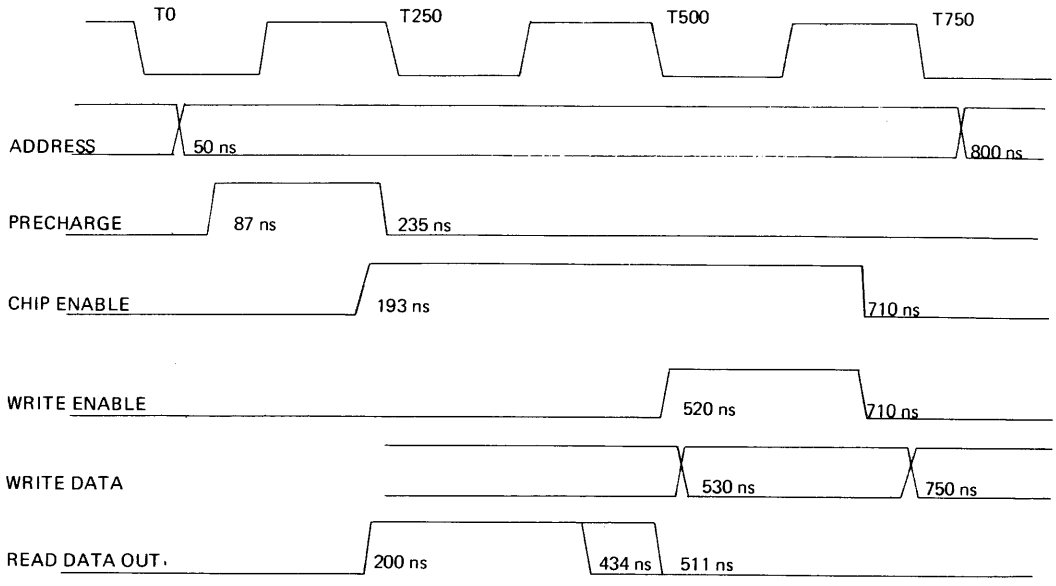
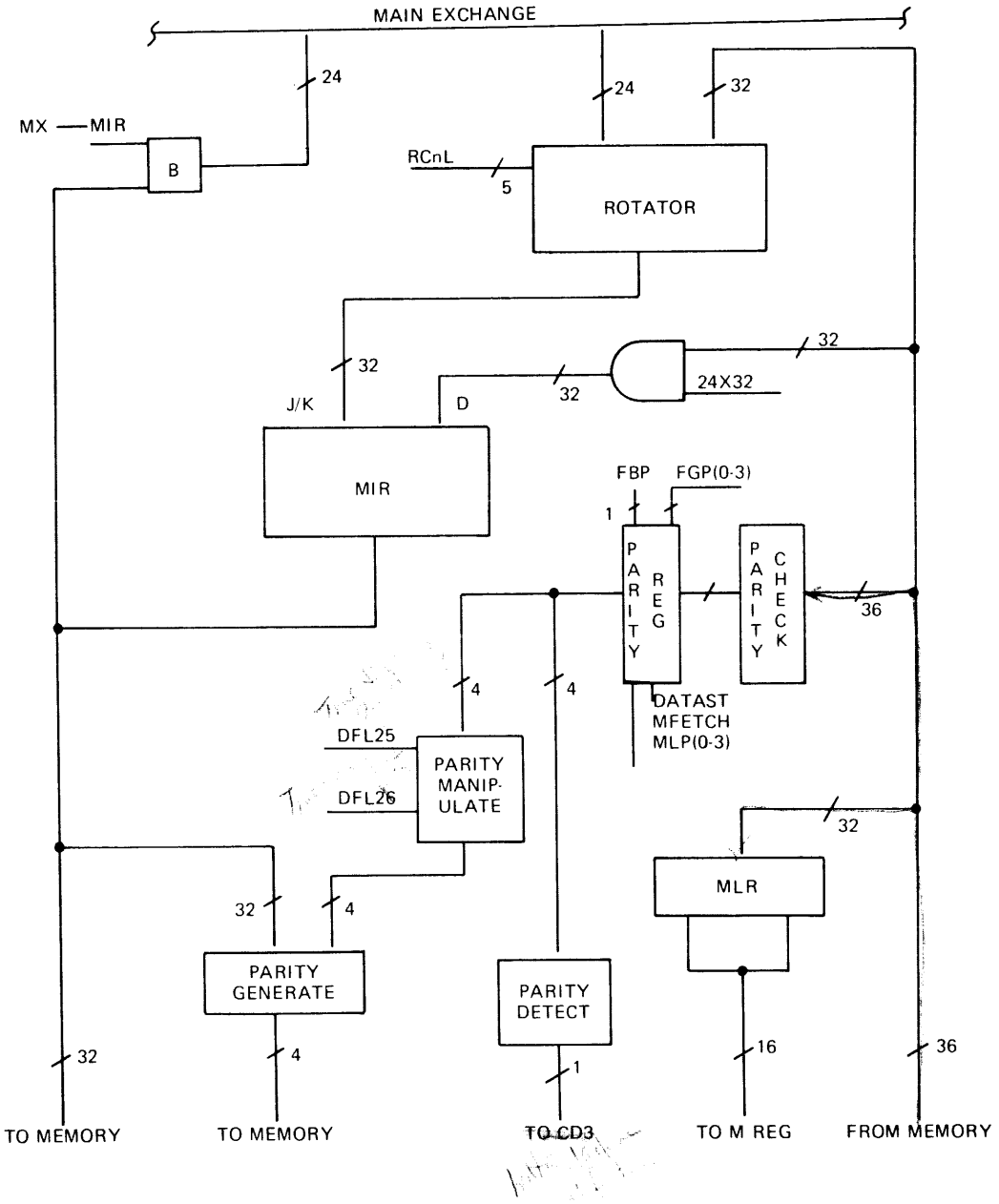


Fig. II-215 BASIC MEMORY WRITE (READ MODIFY WRITE) TIMING

MEMORY DATA FLOW (READ)

The Memory Read Data from the B 1700 S-Memory basically has two separate paths which can be taken. The two paths are dependent upon the reason for which the memory operation is being performed. If the memory operation is for a M Fetch (Fetch of a micro) then the path is simply from Memory to the MLR and from MLR to the M Register. Only 16 bits of MLR are sent to the M Register and this is determined by a bit in MAR(A), KBA04. If KBA04 is off, then data is taken from MLR bits 00 thru 15 to the M Register and if KBA04 is on, then data is taken from MLR bits 16 thru 31 to the M Register. If a M Fetch is being performed, the memory is addressed strictly by word and, therefore, no rotation of the data is required.

The second path for data, which is under control of the 7C Read/Write Memory micro, is that the data read will be sent to a rotator, from the rotator to the Memory Information Register (MIR) and from MIR to the register that is to receive the data (X, Y, L or T). A detailed description of the Rotator is described in the appropriate section of this manual. A path is also provided for the read data to the parity checking logic which will check to insure the data read is good. If a parity error exists, an appropriate bit (CD3) will be set to flag the error.



Figs. II-216 & 217 MEMORY DATA PATHS

MEMORY DATA FLOW (WRITE)

Memory Data on a write operation is obtained from one of five sources. The five sources are as follows: X Register, Y Register, T Register, L Register or from the Console Switches. Regardless of the source for the write data, the information is taken from the Main Exchange, rotated by the Rotator and set into the MIR. The data placed in the MIR is merged with data read during the read portion of the write cycle for the purpose of obtaining 32 bits of information to write. From the Memory Information Register, the data is sent to Memory and to the Parity Generation Logic where parity is generated for the merged data. The operation of the rotation is explained in a separate description of the Rotator. Figure II-216 illustrates the data paths for both a read and write operation.

MEMORY INFORMATION REGISTER

The Memory Information Register in the S-Memory Processor is a shared register. In addition to the normal memory functions, the MIR is used in the 10C, 11C, 4D, 5D, 7D, and 3F micros. These seven micros share MIR for the purpose of logic reduction within the S-Memory Processor. Through use of the MIR and it's associated rotation logic and mask functions, the need for several rotators within the processor has been eliminated. The 7D does not use the rotate function, but merely uses MIR as an additional intermediate storage register for the swapping of a Double Pad Word.

On the memory operations, a mask may be set into MIR and data is read, rotated and stored in MIR. On a memory write, a mask is set into MIR and data to be written into memory is placed in MIR either from the Rotator or from memory. Where a bit of the mask is on the data into MIR is selected from the Rotator and with a mask bit of data is selected from memory read data lines.

MEMORY PARITY GENERATION LOGIC

It is the function of the Memory Parity Generation Logic within the S-Memory Processor to generate a parity bit for each memory section (one parity bit for each group of eight bits). The parity bit generated will cause the total number of bits for each group to be an odd number of bits. For example:

P	7	6	5	4	3	2	1	0
1	0	1	0	0	1	0	0	0
0	0	0	1	1	0	1	0	0

NUMBER OF DATA BITS EVEN-PARITY BIT ON

NUMBER OF DATA BITS ODD-PARITY BIT OFF

Parity is generated only on a Memory Write operation.

Because of the bit addressability of the memory, the input to the parity generation logic is the output of the MIR which is the combined read and write data to be written.

There are several peculiarities contained within the logic. If, for example, on the memory read portion of a write operation, a parity error is detected, then at write cycle time BAD parity will be written back into that memory location. This is done because of bit addressability as the parity error may or may not be in the portion of the byte that is to be written.

Special logic is provided to correct parity errors, however, and this would be done by writing the memory location in error using a Data Field Length of 25. With a DFL of 25, the parity error control term is disregarded and correct parity can be generated. Each time a system is powered on, memory may or may not contain parity errors and one of the routines on initialization would be to write all of memory using a DFL of 25 to insure all parity errors are cleared. Another circuit contained allows for generation of BAD parity. If, for example, a test routine desires to check the parity error detection logic, it can write into a memory location and using a Data Field Length of 26, BAD parity is generated. The routine could then read the information at that location and determine whether the error detection logic found the error.

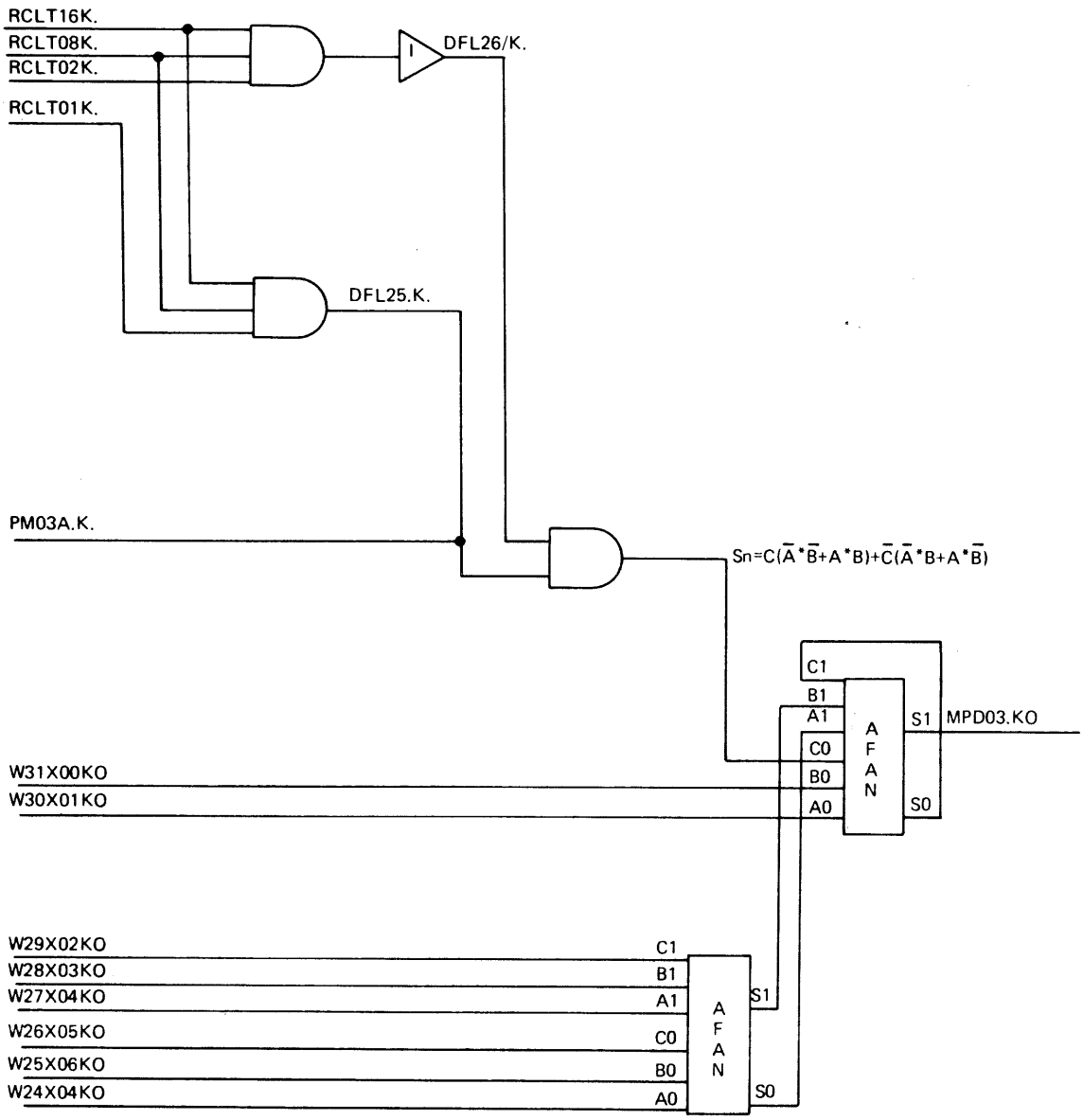


Fig. II-218 1 OF 4 PARITY GENERATE (MODULE 3)

The Parity Generation Logic consists of four unique sections; one for each section of memory or one for each "module". Figure II-218 shows the parity generation logic for the data to be written into module three. The write levels (WnnXnnK0) are from the Memory Information Register after the read and write data have been "merged". The output MPD03 . K0, is sent as the parity bit to Module 3. Parity is generated if the Parity Manipulate term (PM03A . K .) is true.

In order for PM03A . K. to be true, good parity must have been detected on the read data during the read portion of the cycle. PM03A . K. is "ANDED" with a Data Field Length that is not equal to 26 (DFL26/K) in order to generate correct parity. If a data field length of 25 (DFL25 . K.) is specified then the PM03A .K . term is forced true in order to cause correct parity to be generated regardless of the fact that a parity error may have been detected on the read cycle. If a data field length of 26 is specified, the DFL26/K. term is false causing the logic to force incorrect parity for that module (byte).

PARITY LOGIC

Parity Check and Detection Logic is provided within the Processor Card J and H respectively to insure that no parity error exists when data is read from memory owning a Micro M Fetch Operation or the execution of the 7C read/write memory micro.

PARITY CHECK

The Parity Check Logic is divided into four independent circuits, one for each module. Each circuit is made up of two dual full adder/subtraction chips (AFAN's). Inputs to the AFANS is the memory read data from each Byte to its respective circuit. Figure II-219A illustrates the Parity Check Logic for Byte 0. In order for the Parity Check Term (PCMM) to be true, an odd number of bits must be read.

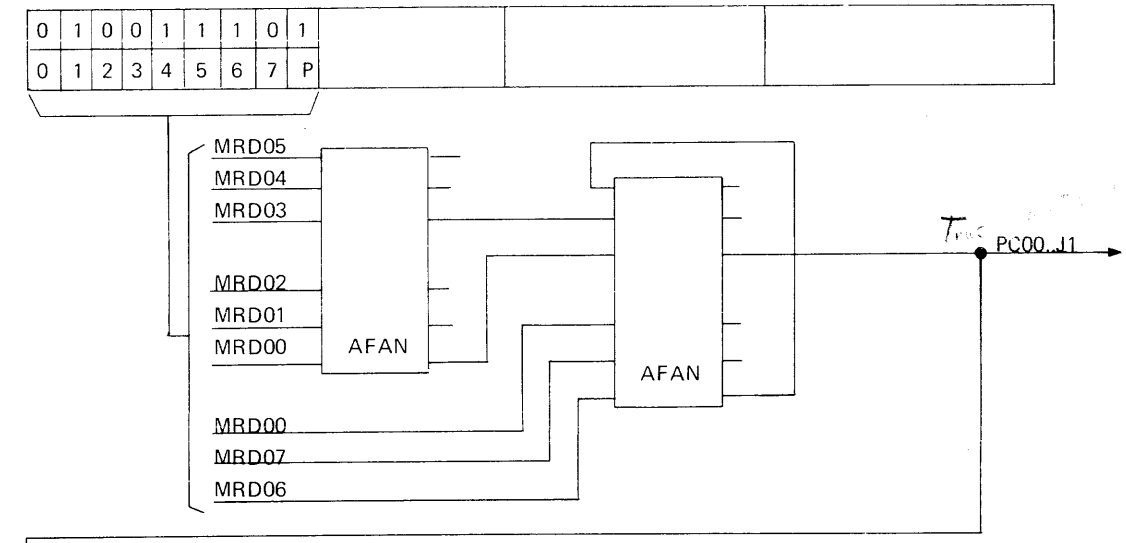


Fig. II-219A PARITY CHECK LOGIC

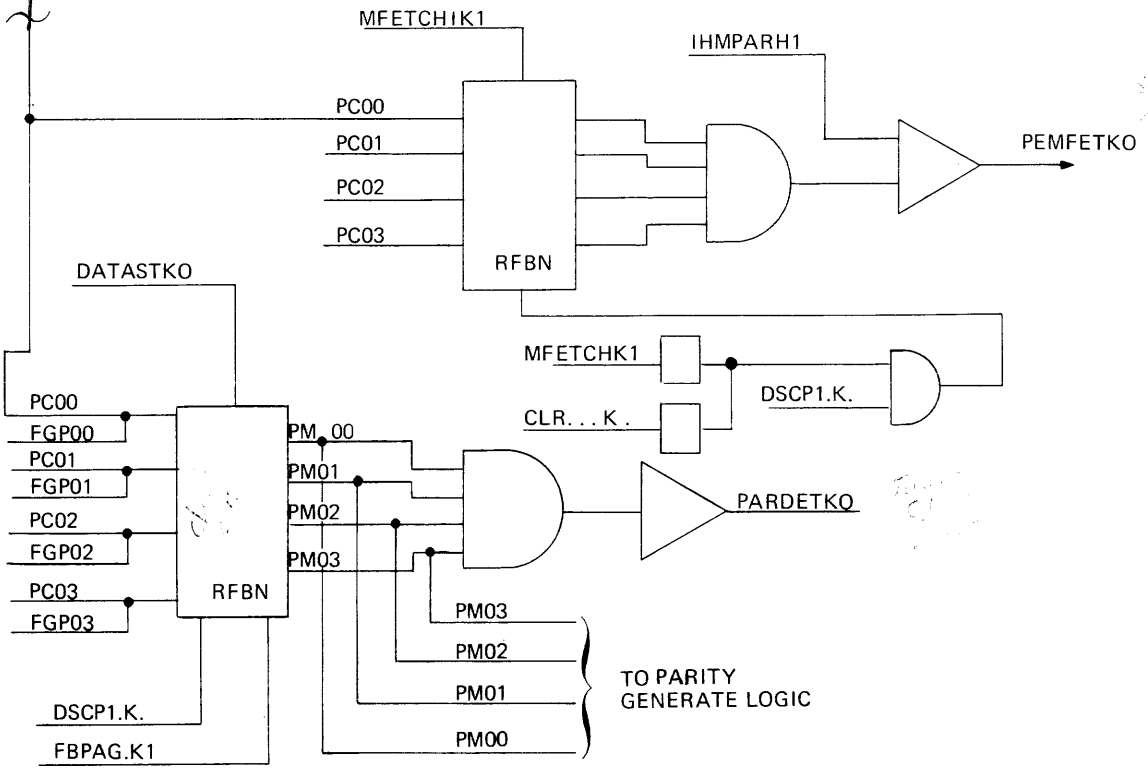


Fig. 219-B PARITY DETECT LOGIC

PARITY ERROR DETECT 7C MICRO

The Parity Error Detect Logic is shown in Figure II-219B. During the execution of a 7C Micro, the four parity check terms (PCnn. . J1) are set into the four bit register, which is enabled by DATASTKO. DATASTKO indicates that a 7C Read/ Write Memory Micro is being executed. If parity is good on all four bytes of data, then the Parity Error Detect Term (PARDETKO) will be false and prevent the setting of CD3. If an error occurs, the appropriate parity manipulate term (PMnn) will be false causing PARDETKO to be true thus setting CD3 to flag the error.

The four bit register inputs also has terms which are ORed with the Parity Check terms. These terms (FGP0n) are used to force good parity when the address is pointing to a boundary where part of the information is to be read from a non-existent memory module. If the address is pointing to a non-existing memory location, then a term (FBPAG. K1) Force Bad Parity is true, which will cause the four bit register to clear thus causing a parity error to be detected. The conditions for forcing good and bad parity are described in the Address Out of Bounds Logic description.

PARITY ERROR DETECT M FETCH

When a Micro is read from memory, additional gating is used to cause a Processor halt, if a parity error was detected.

During M Fetch, the Parity Manipulate (PMnn) are set into a second four bit register located at C3. This four bit Register is enabled by MFETCHK1. with no parity error present. All output will be true causing PEMFETKO to go false. PEMFETKO false means that no parity error was detected during the M Fetch.

ADDRESS OUT OF BOUNDS LOGIC

The Address Out of Bounds Logic, located on Card H, will check the address in MAR(A) and compare it to a wired constant. The constant is wired according to the amount of memory installed. The function of the logic is to force good parity if the location addressed is in bounds but is at a lower boundary address with a negative field direction or if the boundary address is at an upper boundary with a positive field direction. Figure II-220 is an example of both cases where good parity would be forced.

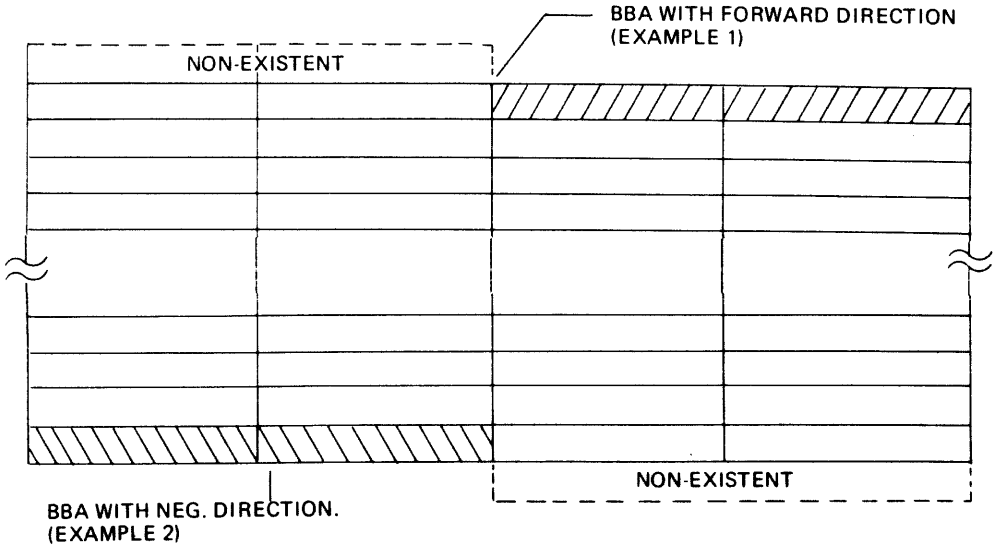


Fig. II-220 ADDRESS OUT OF BOUNDS

In Figure II-220, Example 1, a Bit Boundary Address is pointing between Modules 1 and 2 and a forward field direction is specified. In this example, the most significant two bytes of memory are to be read and the Address Modification Logic will generate an address to read two bytes from Module 0 and Module 1 which are non-existent. It is, therefore, the function of the Address Out of Bounds Logic to force good parity for Modules 0 and 1. In Example 2, a Bit Boundary Address is pointing between Modules 0 and 1 at the lower end of memory and a negative field direction is specified. When the read occurs, the least two significant bytes of memory are read and good parity must be forced for Modules 2 and 3 as the Address Modification Logic generates an address for these non-existent modules. If the Address is out of bounds completely on the upper limit, then BAD parity is forced for all four modules. Figure II-221 illustrates the Address Boundary Checking Logic in a block diagram.

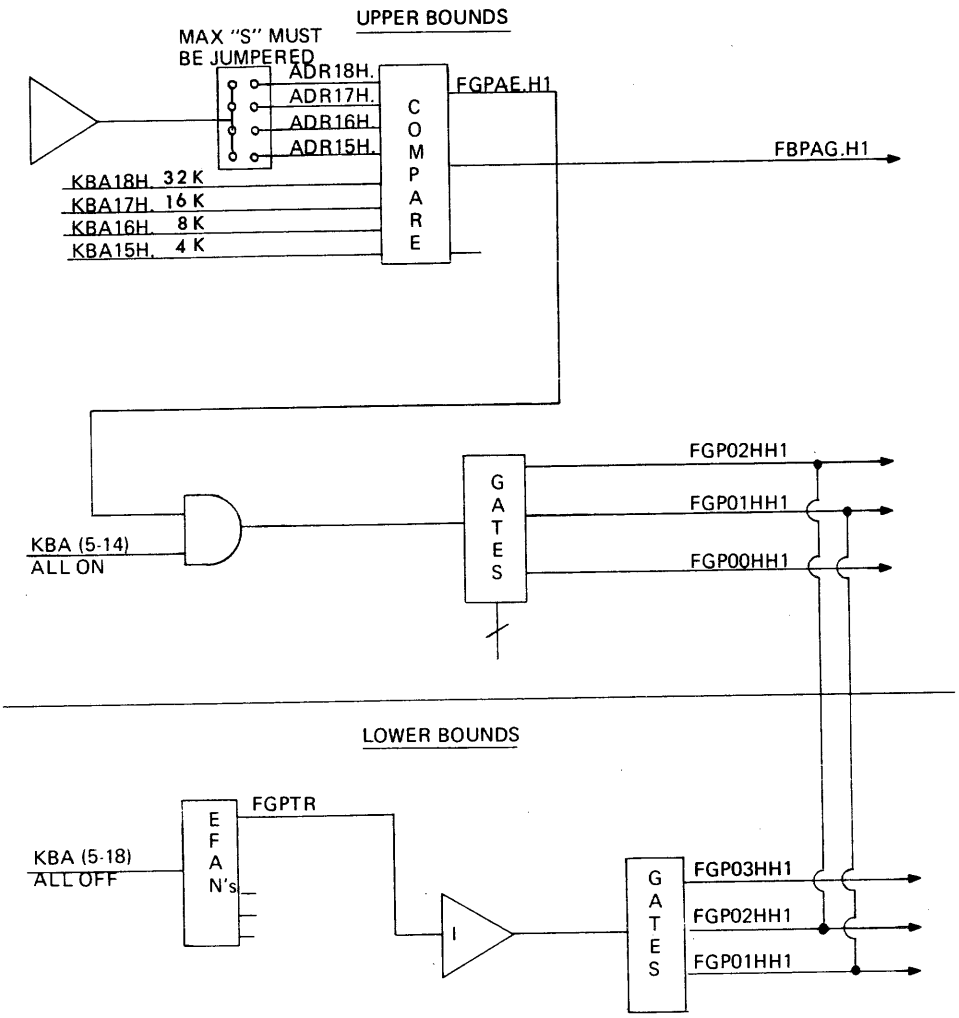


Fig. II-221 ADDRESS OUT OF BOUNDS LOGIC (CARD H)

PROCESSOR – I/O LOGIC INTERFACE

SOFTWARE CONCEPT (BASIC)

All data transfers between the Processor and the I/O Subsystem are controlled by a soft I/O routine referred to as the I/O Driver Routine. Very basically, when an I/O operation is to occur, the I/O Driver Routine is entered, which effectively executes a string of Micros, which in turn will control the transfer of all data to/from the I/O Subsystem. Prior to entering the I/O Driver Routine, the L-Register will contain a 24-bit Reference Address and the T-Register will contain the Channel Number of the Control designated to do an I/O operation. At the time of entering the I/O Driver Routine, via previous software operations, the Reference Address in the L-Register will point to a location in S-Memory where all pertinent information relating to the I/O operation to be executed is stored. Once the I/O Driver Routine is entered, although all available Micros to the concept of the System might be executed, only two have significance directly with the transfer of data to/from the I/O Subsystem. These two Micros are the 1C and 2C Micros. The final decoding of these two Micros which effect I/O operations is illustrated in Figure II-222 and is explained under the title 1C & 2C Micro Decoding.

I/O BUS

The I/O Bus consists of 24 bi-directional lines between the Processor (Card E) and the Distribution Card which is located in the I/O Base. The 24-bits of the I/O Bus are designated as BUS 00 IE1 thru BUS 23 IE1. All data (including OP-Codes, Result Descriptors, Input/Output Data, Reference Addresses, File Addresses, Status Counts, etc.) which is transferred to/from an I/O Control will be transmitted on the I/O Bus.

I/O BUS DATA TRANSFER

The 24-bit I/O Bus is bi-directional and therefore requires logic to gate information to and from the bus lines. Figure II-222 illustrates the logic used to gate information to/from the I/O Bus in the Processor (Card E). The gating to/from the Bus on the Distribution Card is illustrated and explained in the I/O Base Technical Manual. Refer to Section II Page 2 of the I/O Base Technical Manual for details. With reference to Figure II-222, 24 buffers are used to send data to an I/O Control via the I/O Bus. The 24 buffers are enabled with the level IOENB1E. 24 MFANs are used to receive data on the I/O Bus from an I/O Control. The 24 MFANs are enabled when MBUSENFO, MBUS02FO, MBUS01FO, and MBUS00FO are true. MBUS 02 thru 00 FO when true cause the 17 input to twenty-four MFANs (8 input Multiplexers) to be addressed.

Each of the 24-bits of the I/O Bus is an input to the 17 input of an MFAN whose output corresponds. (e.g., BUS23EI1 is an input to the 17 input of the MFAN whose output is MEX23BEO). All gating either to or from the I/O Bus of data within the Processor is via the Main 24-bit Exchange (MEX 23-00BTO or MEX 23-00BEO). The logic which develops the enable levels for either the 24-buffers or the 24 MFANs is explained under the title "1C & 2C Micro Decoding".

1C & 2C MICRO DECODING

The function of the final decoding logic of the 1C and 2C Micro which is illustrated in Figure II-222 is to enable gating the contents of the Main Exchange to the I/O Bus or visa versa. When CMND or DATA is designated as "sink" the Main 24-bit Exchange is gated to the I/O Bus. When DATA is designated as "source" the I/O Bus is gated to the Main 24-bit Exchange. The decoding (by gate number) is given below:

Gate #1.	2C Micro	(Move Pad to Register and CMND is the Register selected). When S1 time occurs (Sequencial Counter), Command Active (CA) is true and IOENABCO is true. The contents of the word of Scratch Pad addressed is gated to the I/O Bus via the Main 24-bit Exchange.
Gate #2.	1C Micro	(Move Register to CMND). This gate effectively functions as did gate #1 except that when gate #2 is enabled, it indicates a Register is sourced rather than a word of Scratch Pad.
Gate #3.	2C Micro	(Move Pad to Register and DATA is the register selected). When S1 time occurs, Response Complete (RC) is true and IOENABCO is true. The contents of the word of Scratch Pad addressed is gated to the I/O Bus via the Main 24-bit Exchange. Gate #3 is designed to be used during the OB portion of a Transfer Out B command which is currently not used by the Processor or the I/O Controls.
Gate #4.	1C Micro	(Move Register to DATA). This gate effectively functions as did gate #3 except that when gate #4 is enabled, it indicates a Register is sourced rather than a word of Scratch Pad. Gate #4 is currently not used for the same reason as Gate #3.
Gate #5.	1C Micro	(Move DATA to Register).
	+2C Micro	(Move DATA to Scratch Pad).
		When S1 time occurs RC is true. When Gate #5 is enabled, it indicates the OB portion of any command except Transfer Out B. The I/O Control sensing that the OB portion of a two part cycle is true, must generate I/O Send (IOS) which will enable gating data from the I/O Control to the I/O Bus within the Distribution Card. Gate #7 is also enabled when gate #5 is enabled thus gating the I/O Bus to the Main 24-bit Exchange with MBUSENFO and MBUS 02-00 FO.
Gate #6.	2C Micro	(Move Register to Pad) Note that the Register is not specified, refer to Gate #7.
Gate #7.	1C Micro	(Move DATA to Register).
	+2C Micro	(Move DATA to Pad)
		The four outputs of the EFAN shown are true, thus the contents of the I/O Bus is gated to the Main 24-bit Exchange. Gate #5 is also true when Gate #7 is enabled.
Gate #8.		When enabled indicates the Command Active (CA) time of any of the seven command types listed in Figure II-6 of the I/O Base Technical Manual.
Gate #9.		When enabled indicates the Response Complete (RC) time of a Transfer Out B type command. This command is not used at present by either the Processor (software) or the I/O Controls.
Gate #10.		When enabled indicates the Response Complete (RC) time of all-commands listed in Figure II-6 of the I/O Base Technical Manual except the Transfer Out B command.

NOTE: The current Driver Routine executes only the 1C (Move Register to CMND) Micro and the 1C (Move DATA to Register) Micro. It can therefore be assumed that only gates 2, 8, 5, 10, and 7 will be used.

Functional Detail

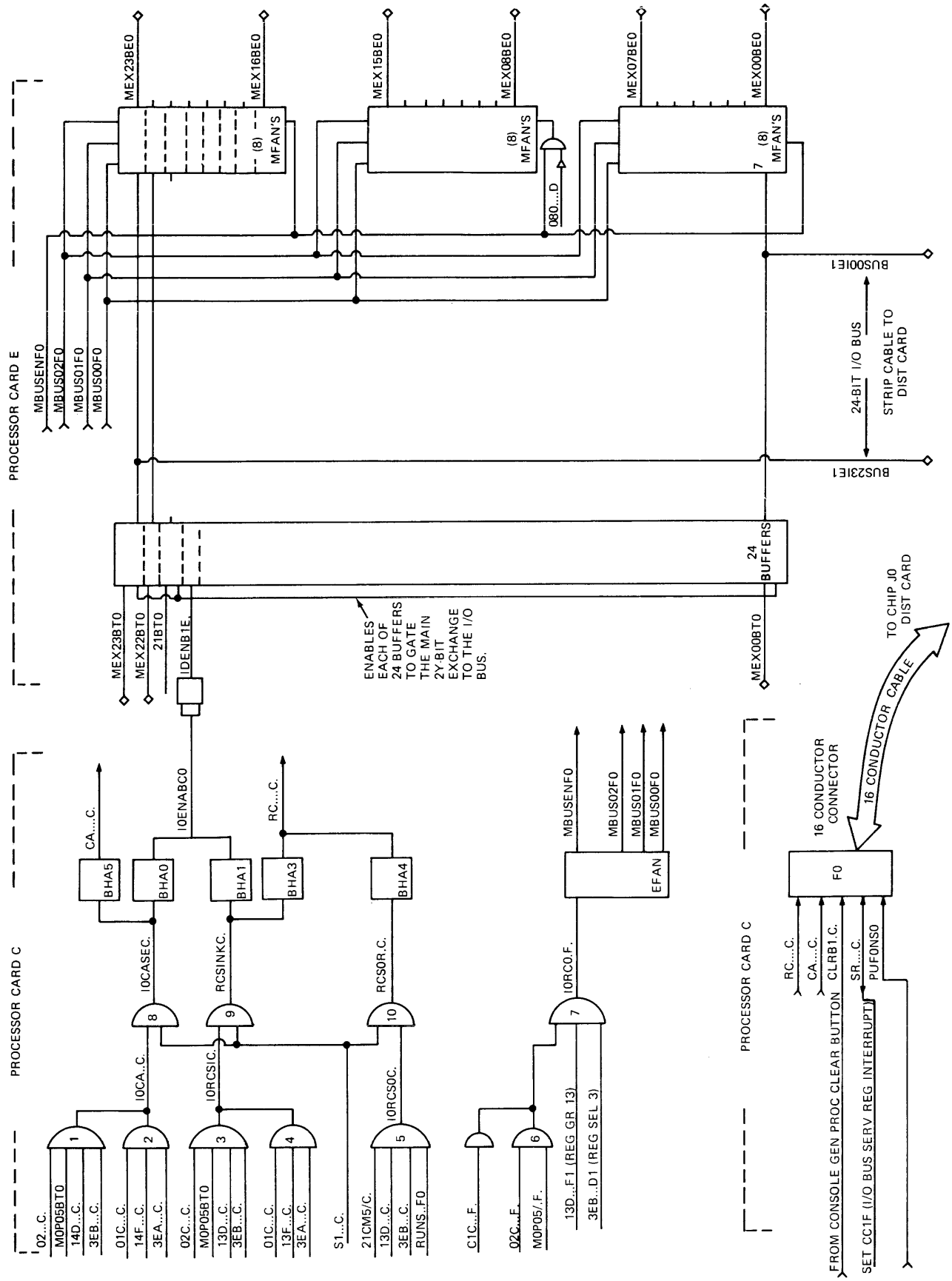


Fig. II-222 PROCESSOR I/O INTERFACE LOGIC

CONTROL SIGNALS

In addition to the 24-bit I/O Bus, five control signals interface the Processor and the I/O Sub System. Four of these levels are generated within the Processor and one is generated within the I/O Controls. A 16 connector cable is used to transmit the signals to/from the Processor and the Distribution Card in the I/O Base. Each of the signals is defined as follows:

1. RC — Response Complete is true during S1 time when either gate #9 or gate #10 is enabled (refer to 1C & 2C Micro Decoding for details). RC indicates to an I/O Control that the OB portion of a two part I/O cycle is complete.
2. CA — Command Active is true during S1 time when gate #8 is enabled (refer to 1C & 2C Micro Decoding for details. CA indicates to an I/O Control that a command is being transmitted to either one or all I/O Controls. The Control(s) designated must receive the command at this time. CA indicates OA time is complete.
3. CLRB — Clear Bus is true when the General Processor Clear Button has been depressed. Most logic within the Controls will be reset.
4. SR — Service Request is sent to the Processor from an I/O Control when the Control is at a point in its operation where it requires intervention by the Processor. SR true will set the CC-Registers 1 bit (CC1F) which indicates an I/O Bus Service Request Interrupt. The MCP will check for CC1F true and initiate appropriate action to service the Control(s) which need servicing.
5. PWRON — Power On is normally true. During a Power Up of the Processors Logic Power Supply, PWRON is false for a period of time which causes a Power Up Clear to occur.

LOGIC POWER SUPPLY

GENERAL

This section describes the functions and detailed operation of the B 1700 Logic Power Supply which converts the raw 188-253 VAC RMS single phase 47-63 Hz wall input voltages to four (4) output voltages which are used throughout the B 1700 Central System. As explained in Section I, the raw wall input is first connected to the AC Power Distribution Assembly and then to the 24V Chassis. The output of the 24V Chassis is the input to the Logic Power Supply. The four output voltages of the supply are as follows:

1. +4.85V 200 amp output used primarily for CTuL logic.
2. -2.0V 200 amp output used primarily for CTuL logic.
3. +12V 10 amp output used for Line Drivers.
4. -12V 10 amp output used for Line Drivers and Receivers.

All four outputs are DC voltages with voltage regulation and current limiting provided. In addition the Logic Supply develops Control Voltages which are used exclusively within the Logic Power Supply. Shut down capabilities are provided when either an over voltage is detected or an over current drain occurs.

OVERVIEW

Figure II-223, Block Diagram of the Logic Power Supply, illustrates the overall functional operation of the Logic Supply. It should be noted that although Figure II-223 illustrates some of the circuitry of the Logic Power Supply in a certain amount of detail all circuits are condensed and are therefore not complete. The heavy lines illustrate either the grounding of various components or the main "flow" of the Power Supply with respect to input and output. Assuming the main 35 amp circuit breaker in the AC Power Distribution Assembly is closed and Power ON has been depressed, the OA and OB inputs will supply the input with 188-253 VAC RMS, single phase, at 47-63 Hz. This input voltage is applied to the primary of Transformer T1 and to the input of the AC/DC Converter. The secondary windings of Transformer T1 provide AC step down which is then rectified by both the Control Supplies and the 160V Regulator circuits. The Control Supplies provide the Logic Power Supply with internal voltages used throughout as bias voltages, reference voltages, source voltages to trigger SCRs, and general miscellaneous uses.

The 160V Regulator uses the stepped down secondary AC voltage of Transformer T1 which is rectified within the Regulator as it's source voltage. The input AC applied to the AC/DC Converter is rectified and filtered to 160V DC. The 160V output of the Converter is regulated at +160V DC by the 160V Regulator which controls the firing time of two SCRs in the rectifier portion of the AC/DC Converter. The +160V DC output of the AC/DC Converter is converted to a 320V peak to peak approximate square wave by the Inverter circuit. The output of the Inverter is applied to a step down Transformer (T2) whose secondary windings are rectified and filtered to the four output voltages of the Logic Power Supply +4.85 -2.0V, +12V, and -12V DC). The output of the Inverter is effectively controlled primarily by the Comparator, VC0, Logic Timer, and Gate Driver circuits.

The output voltage of the 4.85V Logic Supply is monitored at the input of the Comparator. The Comparator in turn regulates the output frequency of the Voltage Comparator Oscillator (VCO) which produces a pulse train at approximately 10 KHz when the output of the Logic Power Supply is at approximately 4.75V. The 10 KHz output of the VCO circuit provides an input to the Logic Timing circuitry which in turn will pulse the gate drivers at the proper time.

The Gate Drivers effectively control the ON/OFF time of the four power SCRs and two Control SCRs in the Inverter. The output current of the +4.85V Logic Supply is also monitored by a current limiting circuit which drains the input of the VCO circuit when the Logic Supply is over loaded. The Current Limiting circuit also provides draining the output of the VCO circuit when the input to the Inverter is less than 130V DC. Either condition will cause the frequency of the pulses to the SCRs in the Inverter to be reduced.

A -2V Shunt Regulator is provided to maintain a 200 amp output current of the -2.0V Logic Supply. Over voltage and Under voltage detection is provided which senses the +4.85V and -2.0V Logic Supply. A UV detection has no effect other than to produce an initial clear pulse when power is first brought up. A OV detection in either supply will short the output of the +4.85V and -2.0V supply and remove the AC input to the Supply. OV/UV detection is also present within the $\pm$12V Supplies with an OV condition sensed causing a fuse to blow at the input to the particular $\pm$12V supply.

AC CONTROL

The AC Control consists of discrete components as shown in Figure II-224. The functions of the AC Control are as follows:

1. Provide an AC source voltage for the AC/DC Converter.
2. Provide an AC source voltage to the primary of the main transformer.
3. Provide excessive heat and current detection to the primary of the main transformer.
4. Provide detection of an excessive input current and provides for removing the input voltage when a OV condition is present in either the +4.85V or -2.0V Logic Supply.
5. Provides Radio Frequency detection in both directions.

When the main circuit breaker on the breaker panel is closed and the on/off switch is in the ON position, 208/240 volts AC is applied at the input terminals (OA and OB) of the internal 20 amp. circuit breaker of the Logic Power Supply. Note that specifications for the System require an input voltage at 188-253 VAC RMS, 47-63 Hz, Single Phase. The 20 amp. circuit breaker is normally closed which allows this input to be applied to the Radio Frequency Interference Filter (RFI Filter). The function of the RFI Filter is to filter out the undesireable frequencies from both directions. The 20 amp. breaker (normally closed), is controlled by a series trip coil and a relay trip coil. The series trip coil is activated when the input current is in excess of 20 amps, thereby causing the breaker to open. The relay trip coil is activated when an overvoltage is detected in either the +4.85V or -2.0v CTL Logic Supply.

The AC "filtered" output of the RFI Filter is applied directly to the Rectifier Bridge of the AC/DC Converter. The AC "filtered" output of the RFI Filter is also applied to the primary of transformer T1 through a power diode thermostat and a 2 amp. fuse. The Power Diode Thermostat will open when the temperature of the heat sink reaches 120 C. The 2 amp. fuse will blow when the primary current exceeds 2 amp. Either condition will remove the input to the primary of transformer T1.

AC/DC CONVERTER (Refer to Figure II-225)

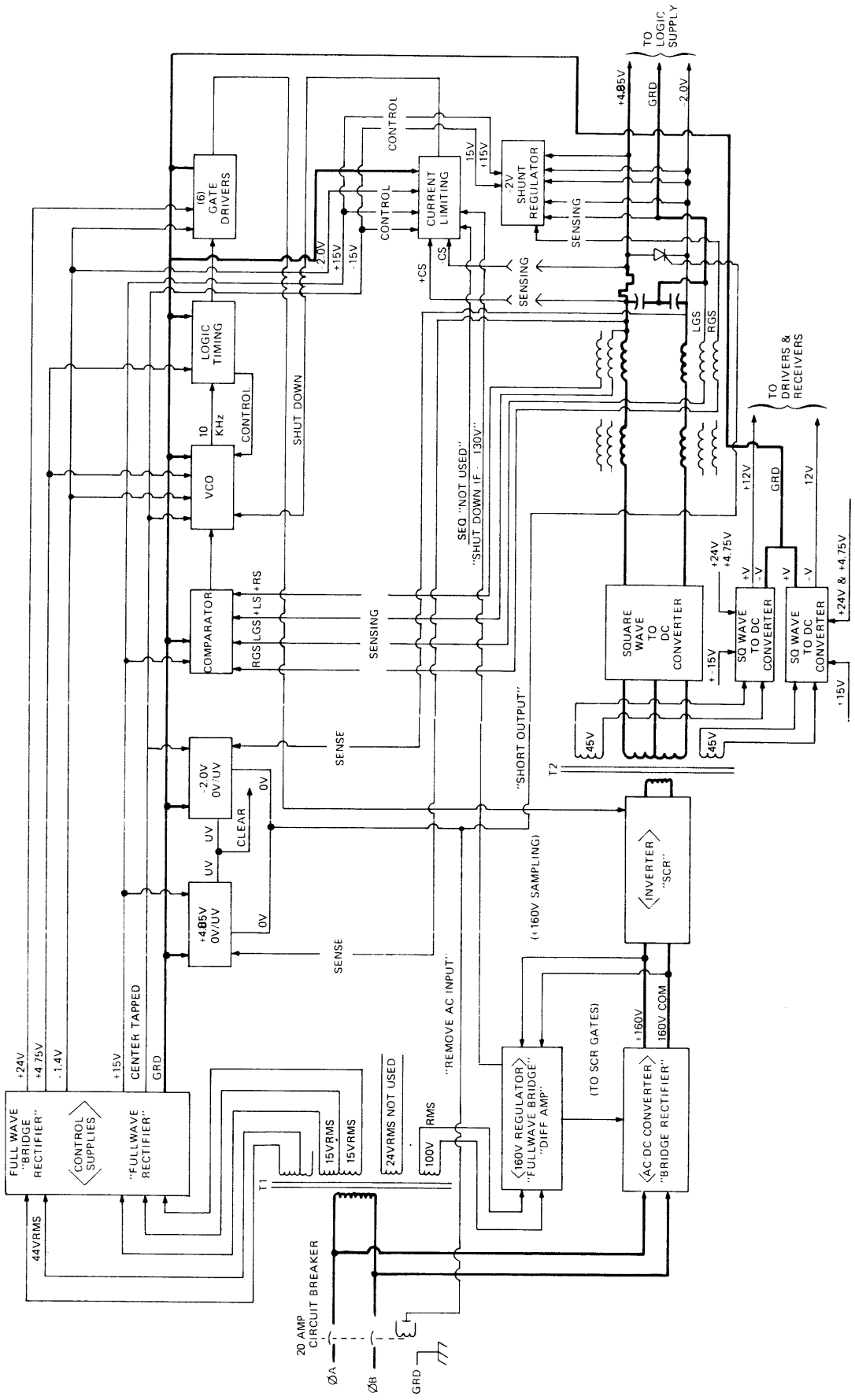
The function of this converter is to convert the AC input to a +160 DC voltage. The +160V DC output of the AC/DC Converter is used in the Inverter Circuit which in turn develops the +4.85V and -2.0V CTL supplies. The +160V DC output is controlled by the +160V Regulator. The AC/DC Converter consists of a bridge rectifier, a gate trigger circuit, and an inductive filter. Each is explained separately as follows:

Bridge Rectifier:

The Bridge Rectifier consists of three rectifier diodes and two SCR's. Assuming the "upper" AC input to the bridge rectifier is positive, the following occurs. A-12 is controlled by the gate triggering circuit which receives a pulse from the pulse transformer in the +160V Regulator. When this pulse is received, A-12 is turned ON. Current flow is then through A-12 and diode (CR10) in the bridge rectifier. When the "lower" AC input to the bridge rectifier is positive, then the reverse is true. The amount of current flowing through the bridge rectifier is therefore controlled by the gate triggering signals to each of the SCR's.

A Commutating Diode (CR15) is provided to link the positive terminal of the output to the common terminal. When both SCR's are OFF, the commutating diode provides a path for the output current to flow in a complete loop. This is needed as the input choke (L1) continues to pump current when the SCR's are turned OFF.

Functional Detail



√ Fig. II-223 LOGIC POWER SUPPLY BLOCK DIAGRAM

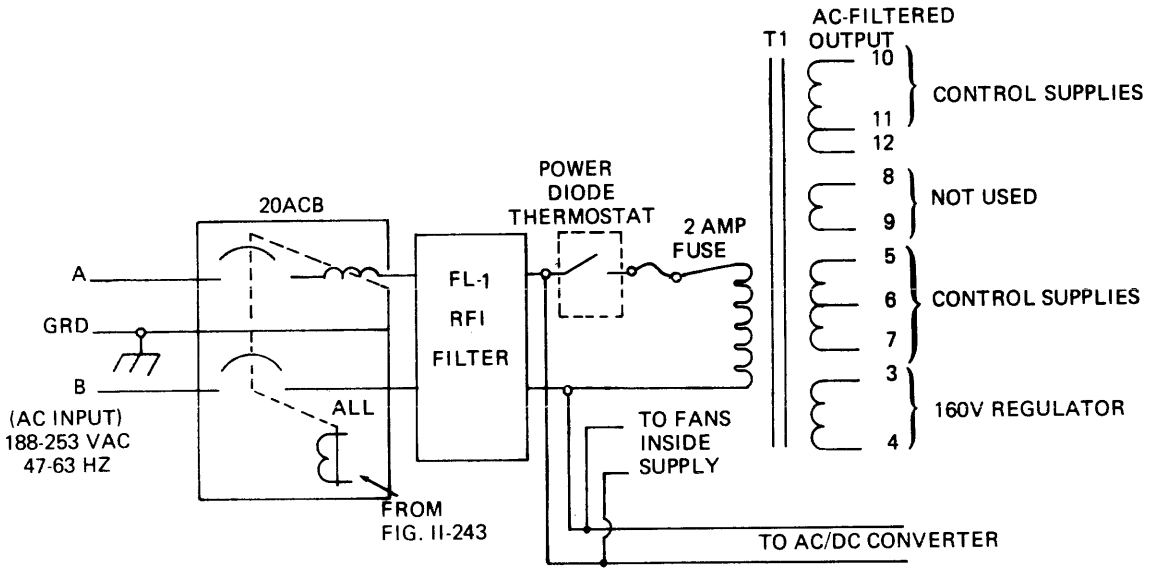
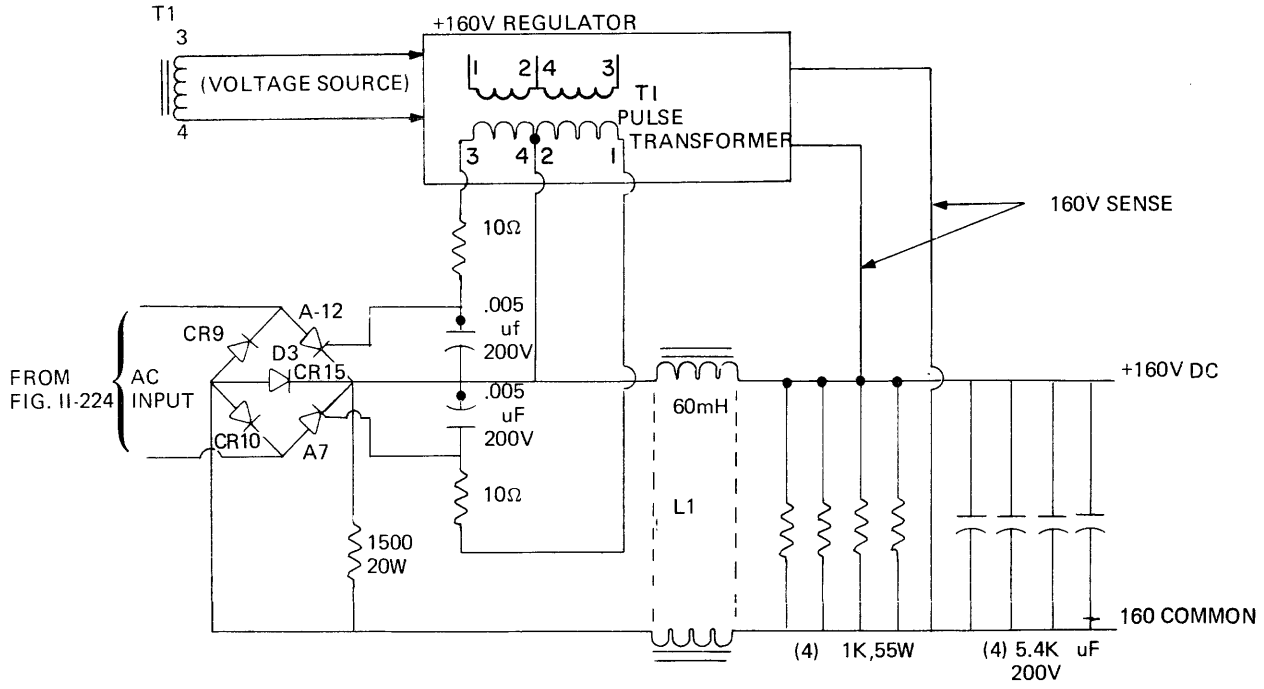


Fig. II-224 AC CONTROL



√ Fig. II-225 AC/DC CONVERTER

Gate Triggering Circuit:

The triggering signals from the pulse transformer in the +160V Regulator pass through the low-pass filters to the gates of the SCR's. The low-pass filters have a small time constant sufficient to suppress any noise in the Gate & Pulse Transformer Circuit. The 10 ohm resistors provide impedance to the gates. The 1500 ohm bleeder resistor provides a path for the SCR holding current.

Filter:

The choke input filter consists of a 60mh choke (L1), four 1K ohm bleeder resistors, and four 5.4K uF shunt capacitors. The choke is divided into two equal portions as shown connected to both the output terminals of the bridge rectifier. This is done to insure the output is stable since the output is not grounded. When the input to the AC/DC

Converter is first applied, the four capacitors present essentially a short circuit to the rectifier, therefore, to prevent component damage it is necessary to begin the charging of the filter capacitors by only using part of AC cycle input to the bridge rectifier. This is accomplished via the Slow Start Circuit in the +160V Regulator.

+160 REGULATOR: (Refer to Figure II-226)

The basic function of this circuitry is to activate, control, and regulate the AC/DC Converter whose output is +160V DC. The +160V Regulator consists of a full wave bridge rectifier, a UJT oscillator triggering circuit, a slow start circuit, a feedback control, and a pulse transformer. Each of these particular portions of the regulator is explained separately as follows:

Bridge Rectifier:

The Full Wave Bridge Rectifier is used as the source voltage throughout the +160V Regulator. Each positive half cycle output of the rectifier is used basically to fire one of the UJTs which in turn through a pulse transformer will fire one of the SCRs in the Bridge Rectifier of the AC/DC Converter. Two 180 degree out of phase sinewaves from the secondary of transformer T1 (pins 3 & 4) are also used in the regulator circuitry to alternately fire the UJTs. The voltage at the secondary of this transformer is 100 Vrms when the input voltage at the transformers primary is 188 Vrms. The phase relationship of the outputs of the bridge rectifier are illustrated.

UJT Oscillator:

The UJT's Oscillator Circuit is primarily used to cause alternate current flow through a pulse transformer which in turn will alternately fire the two SCRs in the Bridge Rectifier of the AC/DC Converter. By controlling the "time" the UJTs are fired, the amount of current flow through the SCRs in the Bridge Rectifier of the AC/DC Converter can also be controlled. This control is the function of both the Slow Start Circuit and the Feedback Control Circuit.

The principle of operation of the UJT Oscillator is the use of synchronized waveforms to create different potentials at each Base 2 of the UJTs so that the trigger signal will fire the UJTs, one at a time. The 20V zener (CR11) clamps the bridge output at 20V DC. This voltage is applied to Base 2 of each UJT. The 100 Vrms AC voltage of the secondary is applied to the two 27V zener diodes (CR6 & CR9) alternately. Assuming the "upper" AC input line is high and the "lower" AC input line is low, the voltage at Base 2 of UJT (Q1) is clamped at 20V since the zener diode (CR6) cannot reach 27V. During this same time, when the "upper" AC input is high, the voltage at Base 2 of the UJT Q2 will reach 27V. Since both UJTs are identical, the UJT with the lowest Base 2 voltage will fire first providing the trigger signal is present; thus UJT Q1 will be fired during the time the "upper" AC input line is high. When the "lower" AC input line is high, the reverse is true which will cause UJT Q2 to be fired. The trigger applied to the emitter of the UJTs to cause the same to fire is present when the timing capacitor, (C2) is charged sufficiently. This timing capacitor is located in the Slow Start Circuit. The charge and discharge time of this capacitor is explained under the headings: Slow Start Circuit & Feedback Control Circuit. The type 7 diodes CR5, CR7, CR8, and CR10 are used to prevent backward current flow.

UJT

The basic operation of the Unijunction Transistor is as follows: When the timing capacitor (C2) is charged sufficiently to cause the voltage at the emitter of the UJT to be more positive than the voltage at Base 1, the UJT conducts and the capacitor will discharge through the emitter and Base 1, causing the output signal at Base 1 to rise. This output will cause current flow in the pulse transformer which in turn fires one of the SCRs in the Bridge Rectifier of the AC/DC Converter. As the timing capacitor is discharging, the emitter voltage to the UJT will drop. When this emitter voltage is approximately equal to that of Base 2, the UJT is turned OFF, causing the output at Base 1 to return to normal. With this basic operation in mind, when the Base 2 voltage is at 27V, the UJT is effectively turned OFF, thus the UJT with the lowest Base 2 voltage will fire first.

SLOW START CIRCUIT

The basic function of the Slow Start Circuitry is to provide the trigger signal for the UJTs. When the input is first applied, the Slow Start Circuit will cause the UJTs to be fired "late" in each half cycle which will in turn cause the two SCRs in the AC/DC Converter to be fired late. The Slow Start Circuit will also cause the UJTs to gradually be fired earlier in each half cycle until the desired firing time is reached. The purpose of this slow start procedure is to prevent a sudden current surge to the capacitor bank at the output of the +160V AC/DC Converter.

The 27V zener diode (CR21) clamps the input voltage to 27V DC. Transistor Q1 is momentarily turned ON when the input is first applied during the charge time of the 0.1 uF capacitor C5 at its base. Turning Q7 ON insures there is no

current flowing to the base of transistor Q6 when the input is first applied. When capacitor C5 is charged, the base potential of Q7 will reach its steady value causing Q7 to turn off. When Q7 is off, diode CR19 at the emitter is reserved biased which will cause the base potential of transistor Q6 to rise due to the charging of the 100 uF capacitor C3. This capacitor and the parallel resistors (R16 and R17) determine the slow start rate. When the input is first applied the voltage drop across R16 and R17 will cause transistor Q5 to conduct, and start to change the .082 uF timing capacitor (C2). The amount of conduction of transistor Q5 is determined by the amount of current flow through transistor Q6. As transistor Q6 will gradually conduct more, as the 100 uF capacitor (C3) is charged, the collector current of Q6 will be sufficient to cause the 4.7V zener (CR17) to reach its voltage. When this occurs, transistor Q5 will conduct at its maximum thus current is supplied to charge the 0.082 uF timing capacitor (C2) at the normal operating rate.

When the input is first applied, the timing capacitor is therefore charged at a slower rate. This will cause the UJTs to be fired "late" in each half cycle. As the 100 uF capacitor (C3) is charged, the 0.082 uF capacitor (C2) will gradually charge earlier thus firing the UJTs earlier. The circuit will reach its normal operating rate in approximately 2 seconds. When the input is removed, the 0.1 uF capacitor (C5) will discharge through the 100K resistor. This will cause transistor Q7 to turn ON which will cause the 100 uF capacitor (C3) to discharge through the 215 ohm resistor, type 7 diode, and transistor Q7. Effectively this is the "prime" function of the 0.1 uF capacitor. It should be noted that if a cycle is missed which would cause the 0.1 uF capacitor to discharge; the 100 uF capacitor will also be discharged thus insuring a "Slow Start!" The 100 uF capacitor (C4) is used as a filter.

FEEDBACK CONTROL CIRCUIT

The function of the Feedback Control Circuit is to "sample" the +160V output of the AC/DC Converter and provide a change in the firing time of the UJTs when the +160V output increases or decreased. The principle of operation is as follows: When the +260V output of the AC/DC Converter is at +160V, a constant current is drawn from the emitters of transistors Q3 and Q4. When the +160V output of the AC/DC Converter increases the bias voltage to transistor Q4 of the differential amplifier is increased by an equal amount. This is due to the clamping action of the 4.7V zener (CR15) at the base of Q4. The bias voltage to transistor Q3 is increased by about 96% of the change in the input voltage.

This will cause more current to be drawn through transistor Q4 which in turn decreases the charging current to the timing capacitor (C2) located in the Slow Start Circuit. By decreasing the charge current to the timing capacitor (larger phase angle) the UJTs will fire later thus reducing the average input voltage to the AC/DC Converter. When the +160V output of the AC/DC Converter decreases, the reverse is true which will cause the charge current to the timing capacitor to increase. This will therefore cause the UJTs to fire earlier which will allow more current through the two SCRs in the Bridge Rectifier of the AC/DC Converter. The 0.68 uF capacitor (C1) in the bias circuit of transistor Q3 creates a leading edge to the input lagging ripples which minimizes oscillation. The 130V zener (CR27) is used to allow the photo-couple-pair to send a control signal to the Current Limiting Circuit when the +160V output of the AC/DC Converter is greater than +130V.

PULSE TRANSFORMER

The function of the pulse transformer is to couple the pulsed output voltage at Base 1 of each UJT to the gate of the corresponding SCR in the Bridge Rectifier of the AC/DC Converter.

±15V COMPLEMENTARY TRACKING POWER SUPPLIES (Refer to Figure II-227)

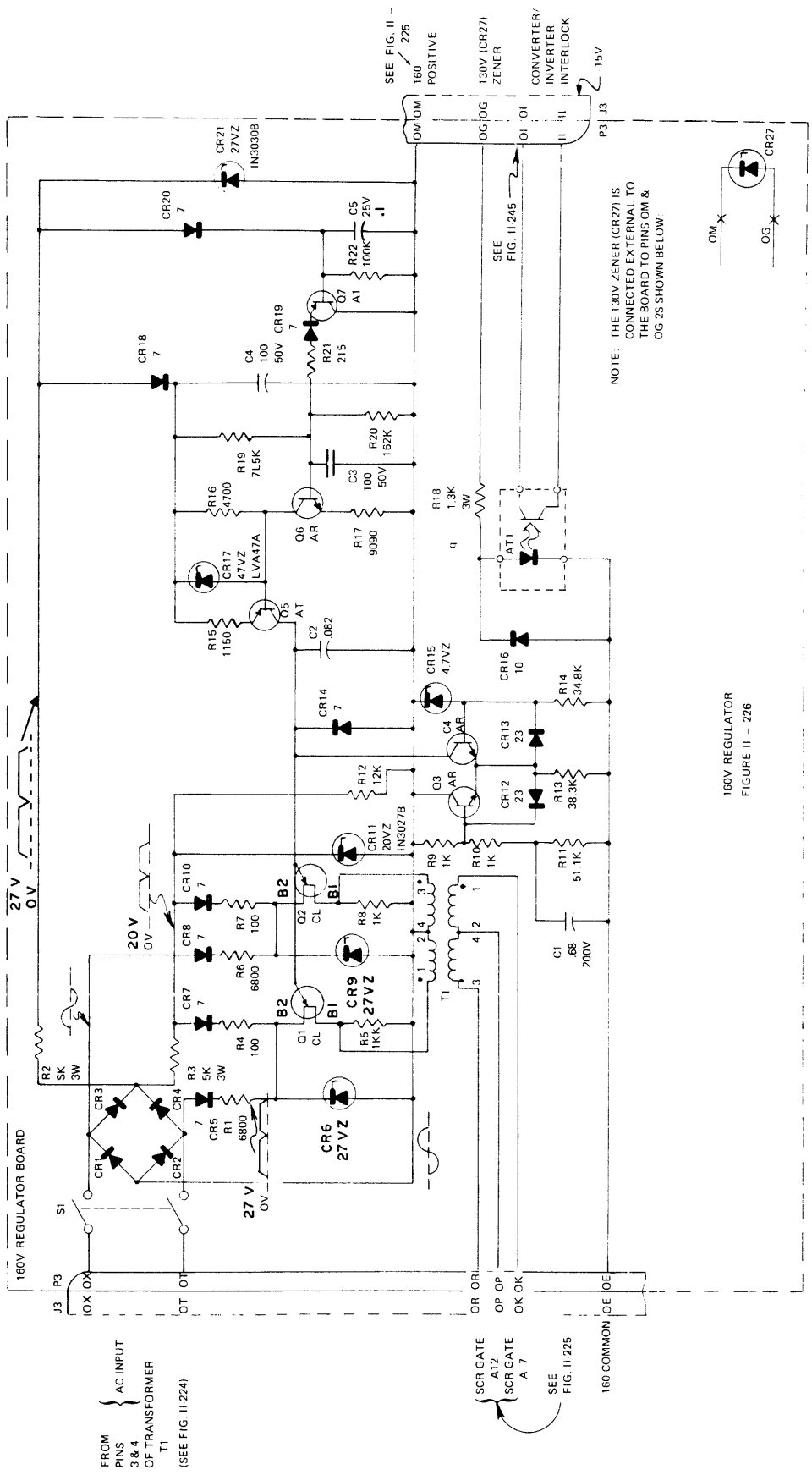
The function of the ±15V Complementary Tracking Power Supply is to convert the AC input to +15V and -15V DC. The +15V and -15V output of the power supply is used throughout the Logic Power Supply as control voltages. The supply consists of mainly a full wave center-taped bridge rectifier, two identical capacitor-input filters, a pair of complementary positive and negative voltage regulators (MC1469 and MC1463 respectively), plus circuitries of pass transistors, current limiting and voltage tracking. Each of these particular portions of the power supply is explained separately as follows:

BRIDGE RECTIFIER & INPUT FILTER

The Full Wave center-taped Bridge Rectifier converts the AC input to +24.4V and -24.4V DC. The input Filters provide a minimum amount of ripple. The +24.4V and -24.4V DC is used as the input voltages to the positive and negative power-supply voltage regulators.

The voltage across the transformer (T1) secondary terminals 5 and 6, or 6 and 7 is 15.5Vrms when the input voltage at the primary of the same transformer is 188Vrms. When the voltage at the secondary is positive, rectifier diodes

Functional Detail



√ Fig. II-226 160V REGULATOR

CR3 and CR4 conduct while CR2 and CR1 do not. Current flows through both 1K resistors thus causing the voltage at the input (pin 3) of the positive power supply regulator (MC1469) to be at +24.4V. When the voltage at the secondary is negative, rectifier diodes CR2 and CR1 conduct while CR3 and CR4 do not. Current flows again in the same direction through the two 1K resistors causing the input (Pin 3) of the positive power supply regulator to be +14.4V. The junction of the two 1K resistors is at zero volts, and the input (Pin 4) of the negative power supply regulator is at -24.4V.

The 0.3 ohm 3W series resistors prevent excessive starting surge currents. The 44K uf 30V filter capacitors will discharge sufficient current as required to maintain a ripple factor of no more than 5%.

POSITIVE & NEGATIVE POWER SUPPLY VOLTAGE REGULATORS

The basic function of these voltage regulators is to convert the +24.4V and -24.4V input supplied by the full wave center-taped bridge rectifier to a regulated +15V and -15V output. Internally each regulator consists of four basic sections: Control, Bias, DC Level Shift, and Output Regulator. In reference to Figure II-227, these four basic sections are illustrated by the A, B, C, and D division markings on the top heavy black line of each regulator. The heavy line represents the physical boundaries of each regulator. The Control portion is illustrated basically as that position of the regulator designated by "A", Bias by "B", DC Level Shift by "C" and Output Regulator by "D". The purpose of this manual is not to explain in detail the internal circuitry of these regulators, however particular portions are referenced in the explanation of the voltage regulation and the external circuitry used. The basic functions of these four sections are as follows:

A. Control — The Control Section provides two functions: Start Up and Shut Down. The shut down function is not used in either the positive or negative regulator as input pins 2 & C are tied together. The Start Up function is used to establish an internal reference voltage.

B. Bias — The Bias section maintains the reference voltage initially achieved via the Start Up function of the Control section. The positive regulator will have a reference voltage of +3.5V and the negative regulator will have a reference voltage of -3.5V. Each is illustrated in Figure II-227.

C. DC Level Shift — The function of the DC Level Shift is to basically amplify the reference voltage established internally to a level which can be used as the final or output reference voltage of the output regulator. The positive regulator does not use the internal reference voltage of +3.5V to establish an output reference voltage for the output regulator. The output reference voltage used in the positive regulator is effectively zero volts which inputs to the positive regulator on Pin 6. The negative regulator does use the internal reference voltage of -3.5V to establish a final or output reference voltage of -15V. The -15V is illustrated at input Pin 9 and also at the base of transistor T5 in the Output Regulator portion.

D. Output Regulator — The function of the Output Regulators is to regulate the +15V and -15V supplies. The positive regulator using the zero volts at Pin 6 as the output reference will detect an output voltage change at Pin 5 (output sense) and regulate the output voltage at Pin 1. The negative regulator using the internal -15V output reference at Pin 9 will detect an output voltage change at Pin 8 (output sense) and regulate the output voltage at Pin 6.

POSITIVE VOLTAGE REGULATOR:

The non-inverting input (Pin 6, Output Reference) of the Output Regulator is tied to ground (zero volts). The inverting input (Pin 5, Output Sense) of the Output Regulator will sense the voltage developed at the junction of the two 316 ohm resistors. When the output voltages of the two regulators is at +15 and -15V, the junction of the two 316 ohm resistors will be at zero volts. When either the +15V or -15V output goes more positive, the junction of these two resistors will also go positive. This will cause transistor (T4) in the Output Regulator to conduct more. With T4 conducting more, T1 and T2 will conduct less, therefore the output at Pin 1 will decrease. When either the +15V or -15V output goes more negative, the junction of the two 316 ohm resistors will also go negative. This will cause transistor T4 to conduct less and T1 and T2 to conduct more; therefore, the output voltage at Pin 1 will increase.

NEGATIVE VOLTAGE REGULATOR

The internal -3.5V reference voltage is used as the input to a Darlington differential amplifier which may also be considered an operational amplifier. Pin 1 will be at -3.5V and via negative feedback obtained from the two external resistors (R11 and R15) Pin 9 is at -15V. The adjustable resistor provides an adjustment of the -15V output reference voltage at Pin 9. The Output Regulator operates essentially like that of the positive regulator. The output sense at Pin 8 detects a change in the -15V output. When the output at Pin 8 goes more positive, transistor T6 will conduct more which causes T7 and T8 to conduct more therefore the output at Pin 6 will go more negative. The reverse occurs when the output sensed at Pin 8 goes more negative.

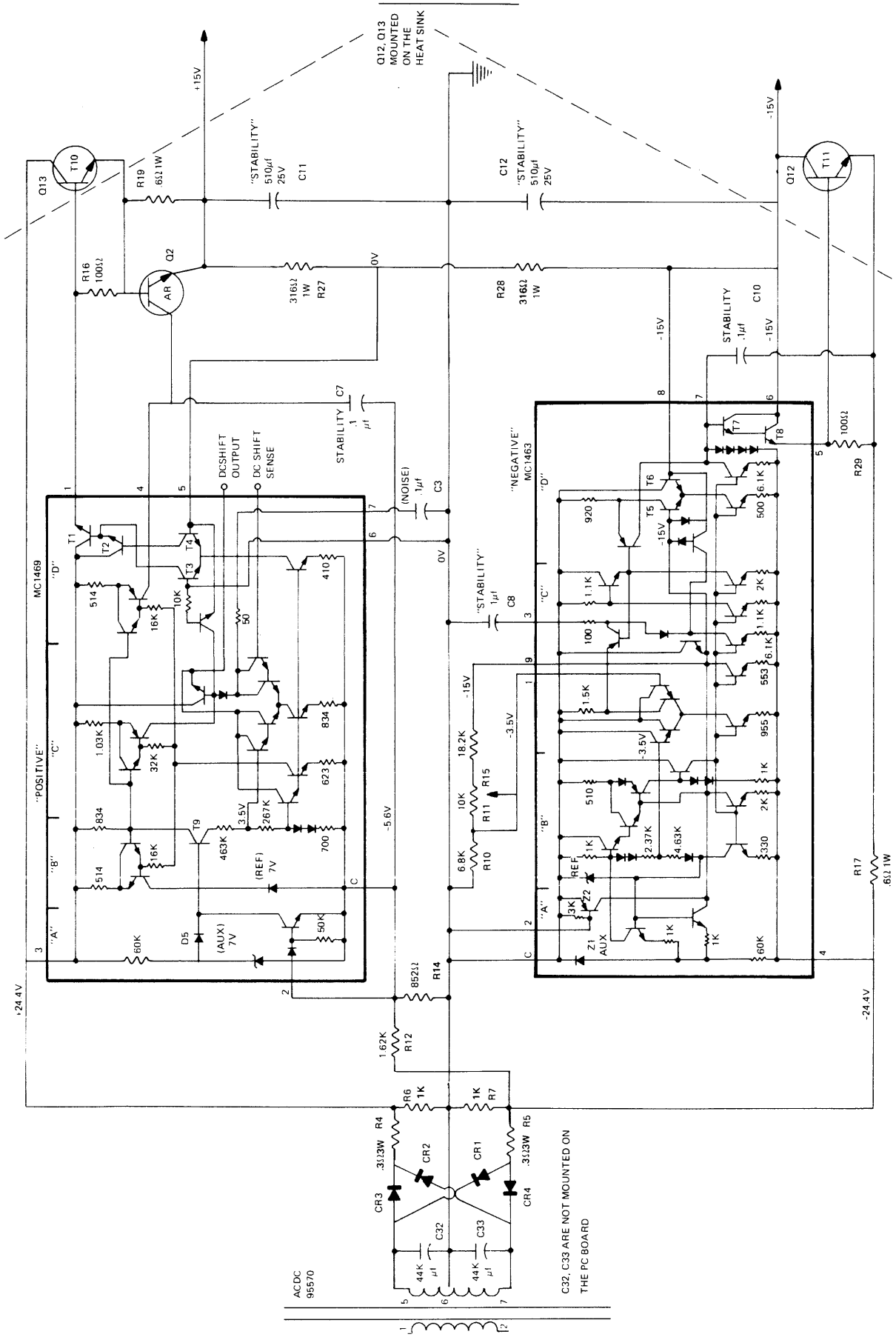


Fig. II-227 ±15V COMPLEMENTARY TRACKING POWER SUPPLY

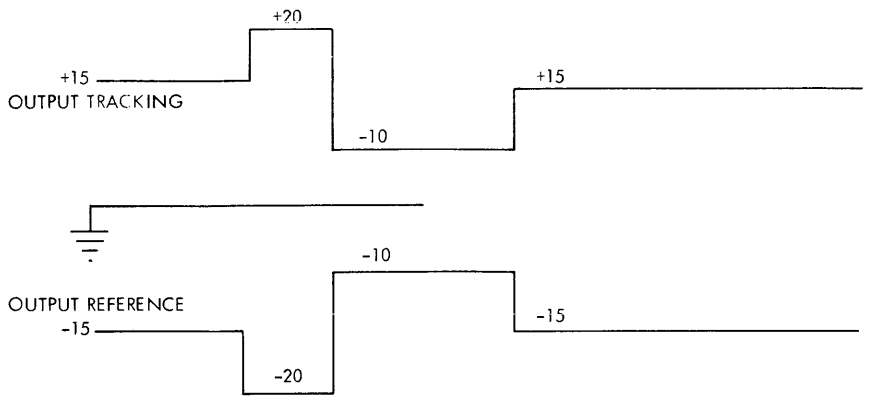


Fig. II-227A

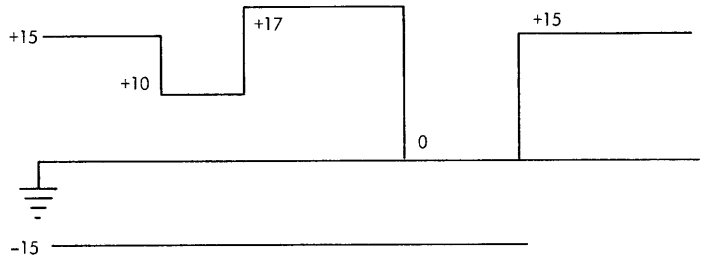


Fig. II-227B

CURRENT LIMITING AND VOLTAGE TRACKING

The external switching NPN transistor (Q2) is used to limit the output current of the positive regulator. When the load current flowing through the .6 ohm 1W bias resistor (R19) is 1 ampere, transistor Q2 is turned ON which drains the base current to transistor T2 in the output regulator. The external series pass transistor (Q13) is under control of the differential amplifier (T3 and T4) in the output regulator. A change in the voltage at Pin 5 will cause the voltage at Pin 1 to change, thus transistor (Q13) will also conduct more or less. The positive regulator tracks the output of the negative regulator, e.g., if the negative regulators output voltage at Pin 6 goes to -14V, then the voltage at the junction of the two 316 ohm resistors will be at approximately +.5V. This will cause Pin 5 (output sense) of the positive regulator to be also at +.5V.

Transistor T4 will conduct more, which causes T2 and T1 to conduct less. Therefore the +15V output will go to +14V. The output voltages arrive at the same levels almost simultaneously. The negative regulator DOES NOT track the positive regulator. If for example the positive output is at +14V, the negative output will remain at -15V. This is due to the output sense (Pin 8) of the negative regulator being connected to the -15V output. The external connected power transistor (Q12) is used to handle the load current of the negative regulator. The four internal diodes are provided to accommodate the use of this transistor to boost the output current. An external current limiting resistor (R17) is connected to this transistor to sample the full load current.

±15 VOLT REGULATOR (Refer to Figure II-227A)

In this circuit the -15 volt regulator establishes a reference voltage. The +15 volt regulator uses this reference voltage to extablish its own output voltage and is said to be operating in a slave regulator. The +15 volt regulator tracks this reference voltage.

The positive and negative regulators also correct for voltage variation within their own circuits. However, the output of the slave (+) regulator will not in any way effect the output of the master (-) regulator.

+24V, +4.75V, -2.0V CONTROL SUPPLIES (Refer to Figure II-228)

The basic function of these three supplies is to provide control voltages for the ± 12V Supply and the -2V Shunt Regulator.

The supplies consist of one full wave bridge rectifier, a capacitor input filter, a pre-regulator, three positive power supply voltage regulators (MC1469) and external voltage regulating and current limiting circuitries. Each of the preceding is explained as follows:

BRIDGE RECTIFIER (FULL WAVE), FILTER AND PRE-REGULATOR

The Full Wave Bridge Rectifier converts the AC input to DC. The out voltage (after filter and pre-regulation) is 28.4V DC. This voltage is used to develop each of the three supply voltages (+24V, +4.75V, & -1.9V). The voltage across transformer (T1) secondary terminals 10 and 11 is 44Vrms when the input voltage at the primary is 188Vrms. The molded assembly bridge rectifier (CR-5) will provide full wave rectification when connected as illustrated. Capacitors C16 and C18 are used to discharge current as required to maintain a ripple factor of no more than 5%. The 50 ohm 5W resistor (R17), the 30V 50W zener (CR20), and the pass transistor (Q1) form the Pre-Regulator with an output voltage equal to 28.4V. The 25 uf 50V capacitor (C17) reduces input ripple to the Pre-Regulator.

+24V, 2 AMPERE SUPPLY

The +24V regulated output of this supply is used for control in the following sections of the Logic Supply:

The positive power supply voltage regulator (MC1469) is the same as the positive regulator illustrated in Figure II-227 (±15V COMPLEMENTARY TRACKING POWER SUPPLY). For this reason, the internal logic of this regulator is not shown or explained. The +24V positive regulator (MC1469) has connected to Pins 9, 6 & 8, three resistors valued at 34.8K, 10K (adjustable) and 6.8K. Internally, the voltage devloped at Pin 8 is 3.3V; Pins 6 and 9 will be at +24V. This +24V is the internal reference voltage of the differential amplifier in the output regulator portion of the MC1469 regulator. Pin 3 is at 28V and is the input voltage to the regulator. Pins 2 and C tied together disable the Shut Down function of the Control portion of the Regulator. Pin 7 connected to a .1 uf capacitor (C1) is used to suppress noise. Pin 1 is the output of the voltage regulator and is at +25V. This output controls the series pass transistor (Q3) which will then maintain an output of +24V at Pin OW. The +24V output is controlled by the output voltage sense at Pin 5 which is at +24V. The .3 ohm 3W resistor tied to the base of the Current Limiting transistor (Q1) is used limit the amount of output current. When the current through the resistor is at 2 amperes, the AR transistor is turned ON, thus draining the base current at Pin 4 to the internal Darlington connected transistors at Pin 1. An output voltage change sensed at Pin 5 will internally change the voltage at Pin 1, therefore controlling the base voltage of the pass transistor (Q3). The MC1469 is essentially the same regulator as that used in the ±15V Complementary Tracking Supply with two basic differences: for higher voltage, the resistance between Pins 8 and 9 is set proportionally higher, and for higher current, the bias resistance (0.3 ohm resistor to the base of transistor Q1) is proportionally reduced.

Effectively this supply is the same in operational theory as that of the +24V Control Supply, with one important exception. A 7.5 ohm 55 W series resistor is used to dissipate excessive power when the current is high. This helps the power handling of the pass transistor Q5.

-1.9V CONTROL SUPPLY

Since the minimum regulated output voltage of the MC1469 positive power supply regulator is +2.5V, when connected in the conventional manner, a special level sensing circuit is necessary for the -1.9V Control (Sinking) Supply.

1. Voltage Regulating:
   The potential at Pin 8 is established internally at +3.3V above Case potential (ground). With +3.35V at Pin 8, the potential at Pin 5 is +4.73V; at pin 9, 9.6V; at Pin 6, 4.7V. The +4.7V at Pin 6 is the output sense voltage used internally as the reference voltage of the differencial amplifier of the output regulator portion of the MC1469 regulator. As this voltage is regulated, the output voltage of -1.9V is also regulated by the 10K and 14K resistors. Under normal operational conditions, Diode 7 is reversed based and Pin 4 is a few volts above Pin 6. During worst case conditions (diode 7 is forward biased) the potential at Pin 4 is approximately 7.9V since the voltage at the anode of diode 7 is set to 8.4V.
2. Current Limiting:
   The current is limited primarily by the 82.5 ohm resistor (RYO). With a full load (4 amps) the base current of transistor Q5 is approximately 3mA so that the voltage across the 82.5 ohm reistor (R40) is 0.5V. With the Darlington (Q8 & Q5) base-emitter drop of approximately 1.4V, the total voltage across the output is about 1.9V. The output voltage is therefore set to be regulated at -1.9V. When the load current goes higher than 4 amps, the voltage across the 82.5 ohm resistor R40 will be higher than 0.5V which in turn will cause the output voltage of the supply to increase (more negative). This however is not permitted due to the voltage regulation. Transistor Q4 does not limit the output sink current but limits the regulator (MC1969) load current to about 15mA.

The normal operating voltages at each pin is illustrated in Figure II-228. Pin 2 and C tied disable the Shut Down function of the Control portion of the regulator. The .1 uf capacitor at Pin 7 is used to suppress noise.

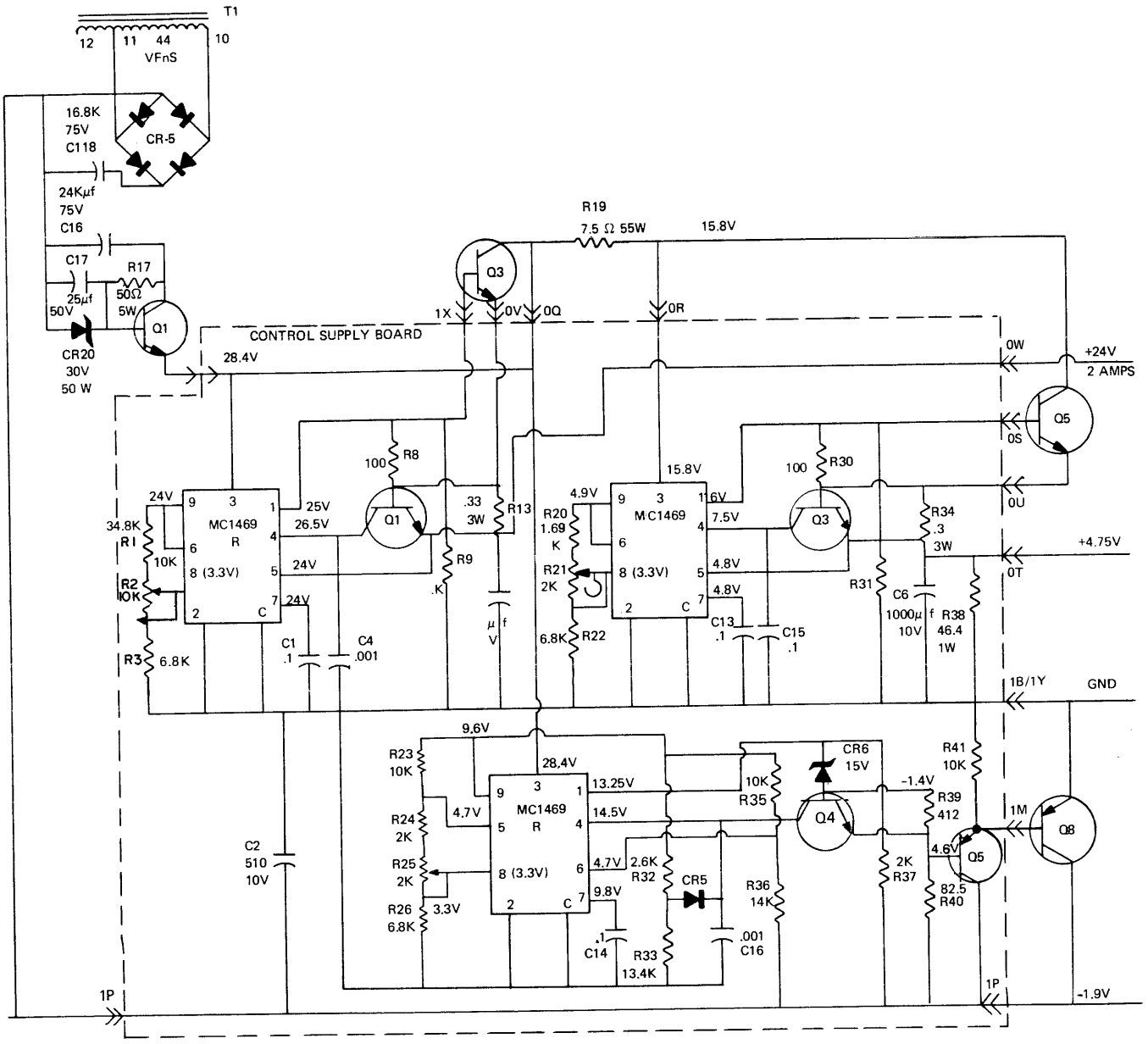


Fig. II-228 CONTROL SUPPLIES

INVERTER (Refer to Figures II-229 thru II-234)

The function of the Inverter is to convert the +160V DC developed by the AC/DC Converter to a 320V peak-to-peak approximate square wave. The approximate square wave developed by the Inverter has a frequency of 5KHZ, which is applied to the primary of transformer T2. The secondary of transformer T2 has three windings which are used to develop the high current +4.75V and -2.00V CTL logic supply and the +12V and -12V supplies used as supply voltages for the Line Drivers and Receivers throughout the System. The operation of the Inverter is described in three steps: the "Basic" operation of a switch inverter, the operation of the SCR Inverter, and the Improved SCR Inverter. The improved SCR Inverter is present in the Logic Power Supply.

A. Basic Switch Inverter:

Illustrated in Figure II-229 is the simplest form of an inverter which consists of four switches, and a load (T1). When switches 1 & 2 are closed simultaneously, current flows through switch 1, through the load, and through switch 2 as indicated by the solid line. The potential difference created across load is positive (+) on the left and negative (-) on the right. When switches 1 & 2 are opened and switches 3 & 4 are closed, current flows in the oppo-

site direction as indicated by the broken line thus causing the difference of potential across the load to be negative (-) and positive (+) on the right. Repeating this action will cause an output waveform as shown in Figure II-230. The voltage output waveform is the difference of potential across the load (T1).

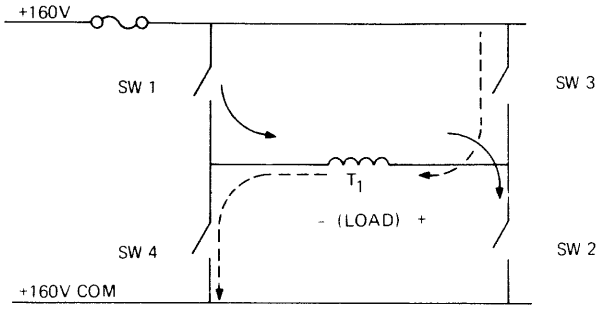


Fig. II-229 BASIC SWITCH INVERTER

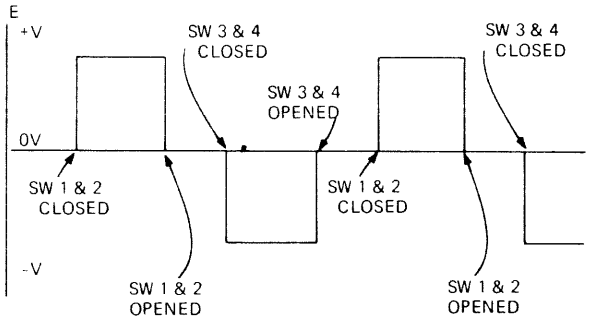


Fig. II-230 VOLTAGE OUTPUT WAVEFORM

B. Basic SCR Inverter:

Illustrated in Figure II-231, is the basic SCR Inverter used in the B1700 Logic Power Supply. When SCR's A1 and A2 are triggered simultaneously, current flows through A1, the load (T1), and through A2 as indicated by the solid line. The difference of potential created across the load is positive (+) to negative (-), left to right. Assuming SCR's A1 and A2 at Shut OFF, when SCR's A3 and A4 are triggered simultaneously, then current flows in the opposite direction through A3, the load, and through A4 as indicated by the broken line thus creating a difference of potential across the load (T1) of negative (-) to positive (+) left to right. This operation is essentially the same as that of the switch Inverter with an exception that the Power SCR's (A1, A2, & A3, A4) require a reverse bias voltage to shut them OFF after they have been triggered. The trigger signals applied to the gates of the SCR's (A1 thru A6) are developed in the Inverter Timing circuitry. Figure II-232, illustrates the relationship of six gate drive outputs of the Inverter Timing Logic, and ON/OFF time of the SIX SCR's, and the output of the Inverter (difference of potential across the load, T1).

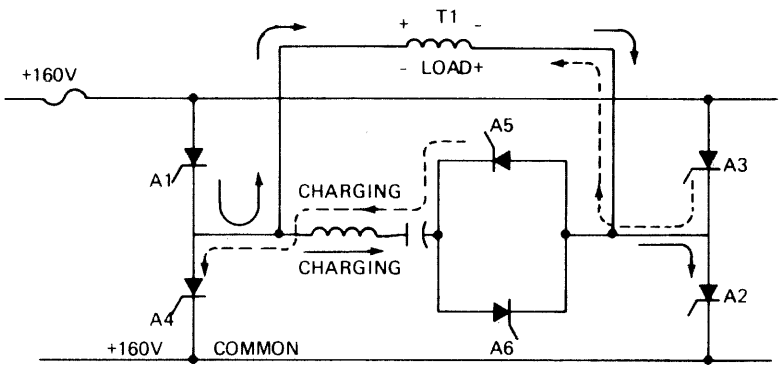


Fig. II-231 BASIC SCR INVERTER

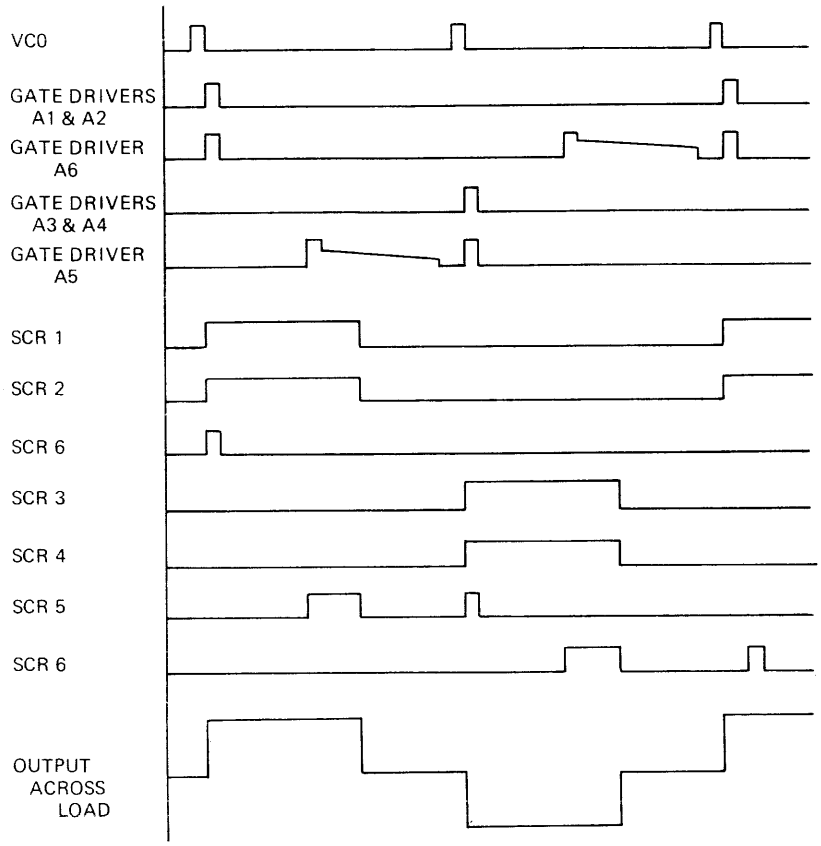


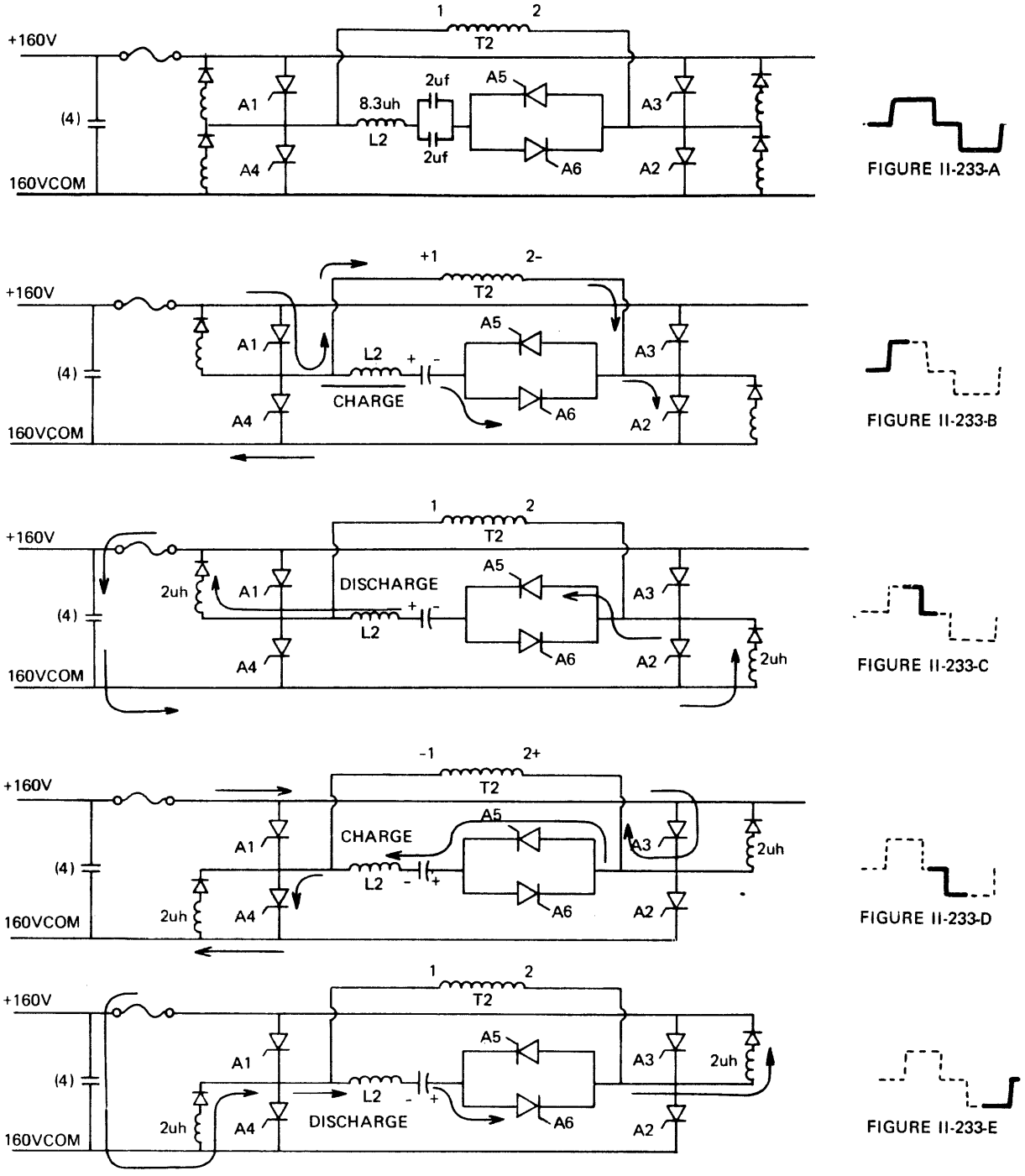
Fig. II-232 INVERTER RELATIONSHIP

When the gate signals are applied to the SCR's as illustrated in Figure II-233 the SCR's will conduct as shown and the output across the load will be a 320V peak to peak approximate square wave as shown. Assuming all SCR's are turned OFF initially, the 320V peak to peak square wave output of the Inverter is developed as follows: When Gate Drivers A1, A2, and A6 output a 5 us pulse signal to the gates of the corresponding SCR's, the SCR's are triggered and will therefore conduct, assuming the +160V DC input is present. This is illustrated in Figure II-233B. A voltage is created across the primary of transformer T2, terminals 1 & 2. This voltage is +160V with terminal 1 positive with respect to terminal 2. The commutating LC circuit (8.3uh inductor and the two 2uf capacitors) start to oscillate thus generating a sinusoidal waveform with periods equal to 36.2 Msec. After the gate signals are removed, SCR A6 will be ON for a maximum of 52 Msec and is turned OFF by the negative going half of the sinewave generated. At this time the two 2uf capacitors are charged up to 160V (positive on the left and negative on the right). This charge will be used to create a reverse bias voltage sufficient to cause SCR's A1 & A2 to turn OFF. To provide the discharge path, SCR A5 is turned ON with the signal applied to its gate from Gate Driver A5. This discharge path is illustrated in Figure 233-C. The discharge voltage is shared by the three inductors in the discharge path. The voltage across each of the 2uh inductors is approximately 20V, which is sufficient to reverse bias SCR's A1 and A2, during this "circuit commutating turn OFF time". After the gate signal to SCR A5 is removed, SCR A5 will turn OFF by the reverse biased half sinwave (positive going). At this time the commutating circuit stops oscillating, and the voltage across the primary of transformer T2 returns to zero volts.

When SCR's A3, A4, & A5 are triggered with the signals applied to there gates from the corresponding Gate Drivers, the negative going output of the 320V peak to peak approximate square wave is developed as illustrated in Figure II-233-D. When the gate signals are removed from the SCR's, SCR A5 will be turned OFF by the reverse half sinewave created by the oscillation of the commutating LC circuit. At this time the two 2uf capacitors are charged up

Improved SCR Inverter

Figure II-234 illustrates the Improved SCR Inverter used in the B1700 Logic Power Supply. Each of the power SCR's (A1, A2, A3 and A4) are shunted with RC suppression circuits (snubbers) which consists of a 10 ohm 40W resistor, a 0.1 uf capacitor, and an "A114A" diode. When the power SCR's (A1 thru A4) are turned OFF, the A114A diode shunts the 10 ohm resistor is parallel with each SCR.



√ Fig. II-233 BASIC INVERTER

to 160V (positive on the right and negative on the left). This charge will be used to create a reverse bias voltage sufficient to cause SCR's A3 and A4 to turn OFF. To provide this discharge path, SCR A6 is turned ON with a signal applied to its gate from Gate Driver A6. This discharge path is illustrated in Figure II-233-E. The discharge voltage is shared by the three inductors in the discharge path. The voltage across each of the 2uh inductors is approximately 20V, which is sufficient to reverse bias SCR's A3 and A4 during this "commutating turn OFF time". After the gate signal to SCR A6 is removed, SCR A6 will turn OFF by the reverse biased half sinewave (negative going). At this time the commutating circuit stops oscillating and the voltage across the primary of transformer T2 returns to zero volts. The cycle repeats when signal is applied to the gates of SCR's A1, A2, and A6.

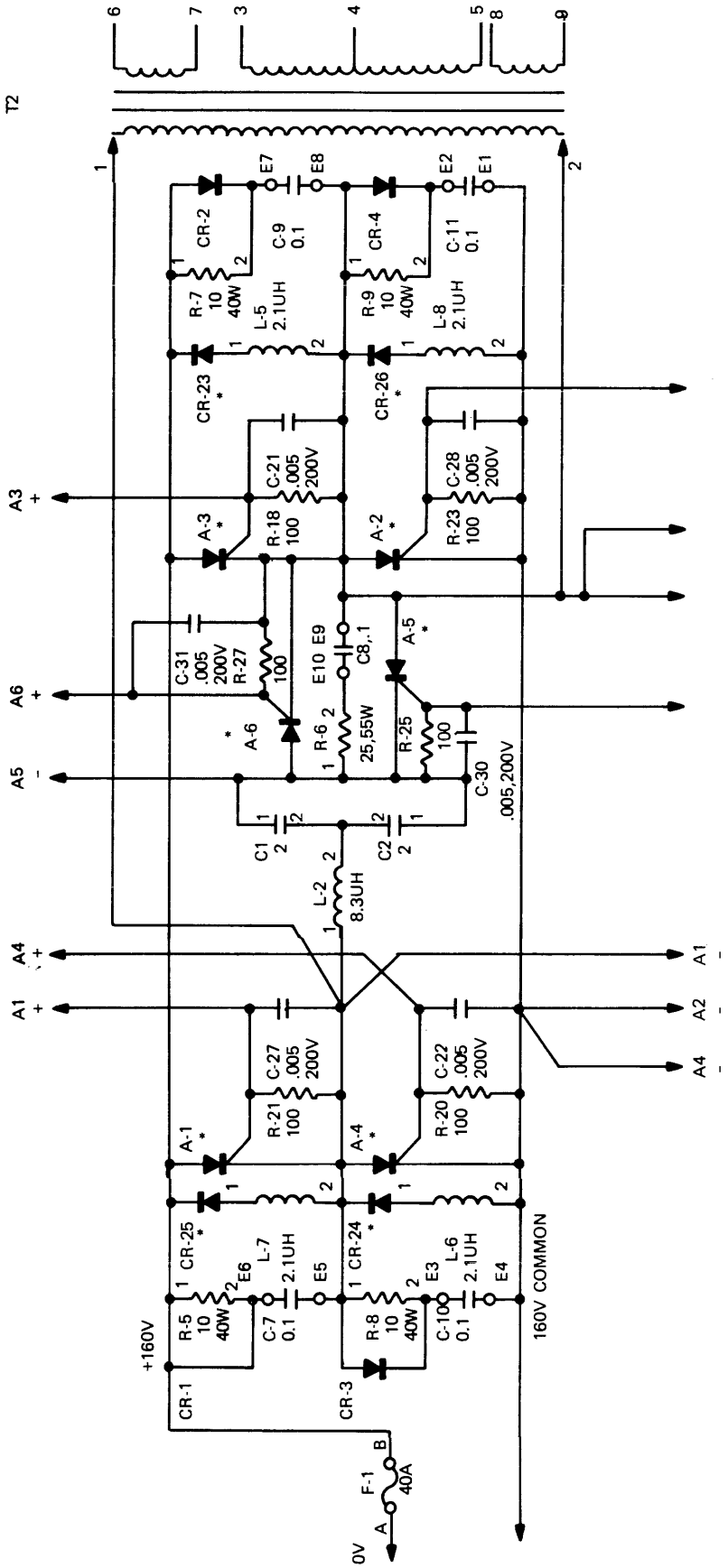


Fig. II-234 IMPROVED SCR INVERTER

INVERTER TIMING

The function of the Inverter Timing circuit is to generate the gate driver pulses used to enable and disable the six SCR's in the Inverter. Figure II-235 illustrates the basic Block Diagram summary of the Inverter Timing Circuit. Each of these blocks of the Block Diagram is explained separately.

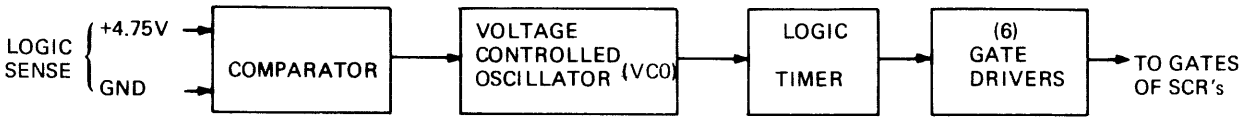


Fig. II-235 INVERTER TIMING BLOCK DIAGRAM

COMPARATOR (Refer to Figure II-236)

The Comparator is a differencial amplifier consisting of an operational amplifier and a voltage reference. The reference voltage is provided by the voltage divider (R4, R5, R6, R7, R8, & R9) and the 7.5V zener diode (CR1). The reference voltage is fixed at +4.85V and is connected to the positive (+) input of the operational amplifier (1/2 747). The .01 uf capacitor (C1) is used to filter noise from the +15V supply connected to the 511 ohm resistor (R4). Both the Remote Ground Sense (RGS) and the Local Ground Sense (LGS) are used as the base of the reference voltage. The voltage at the negative (-) input of the operational amplifier (1/2 747) is the Remote Sense (+RS) and the Local Sense (+LS) of the +4.85V supply output. When the output of the operational amplifier is 5 volts. This effectively means when the negative (-) and positive (+) inputs to the operational amplifier are equal, the output will be 5 volts.

If the output of the +4.85V supply (+RS & +LS) is greater than +4.85V Reference Voltage the output voltage of the operational amplifier will be approximately -0.6V which has the same effect on the VCO circuit as does an output of zero volts. If the output of the +4.85V supply is less then +4.85V the output voltage of the operational amplifier is increased (more positive). This difference is amplified by the 1K ohm input resistor and the 100K ohm feedback resistor, hence the lower the output voltage of the +4.85V supply, the larger the difference and the larger the output voltage of the operational amplifier. This increase in the output voltage of the operational amplifier and the effect of the same is explained during the explanation of the Voltage Controlled Oscillator (VC).

VOLTAGE CONTROLLED OSCILLATOR (VCO) (Refer to Figure II-236)

The function of the VCO is to supply a pulse train at a frequency proportional to the input voltage which is the output voltage of the operational amplifier in the Comparator circuit previously explained. The output frequency will be 10 KHZ output is used as the input to the Logic Timer whose function is to basically generate four output pulses. These four output pulses will be used to activate the six gate driver circuits used to trigger the SCR's in the Inverter. The VCO four output pules will be used to activate the six gate driver circuits used to trigger the SCR's in the Inverter. The VCO circuit consists of an input limiting circuit, a diode bridge, an integrator (operational amplifier, 1/2 747), an AND gate, and a NOR gate. The basic function of each is as follows:

1. Input Limiting Circuit: The 6.2V zener diode (CR2) clamps the input voltage to a maximum of 6.2V. The 10K ohm series input resistor (R16) limits the input current to approximately 0.3 mA's maximum. The 68.1 ohm resistor (R21) and the 47 uf capacitor (C8) provide a series RC network used to suppress noise at the input. Capacitor C8 also provides noise filtering.
2. Diode Bridge: The diode bridge provides directional charging and discharging paths for the 6800 pf feedback capacitor (C12) of the integrator (operational amplifier 1/2 747).
3. Integrator: The integrator is the main part of the VCO circuit and together with the feedback capacitor provides the oscillating output of the VCO.
4. AND & NOR Gates: The AND & NOR gates at the output modify and control the oscillator output according to other control signals generated outside the VCO circuit. The basic function of the AND gate is to buffer signals. The basic function of the NOR gate is to invert the output and to provide control from outside the VCO circuit. The operation of the VCO circuit is as follows:

When the +4.85V (+RS & +LS) supply to the negative (-) input of the operational amplifier of the Comparator circuit is greater than +4.75V, the output of the same and input to the VCO circuit is less positive or approaching zero volts or -0.6V. With a more positive voltage present at the input the following will occur. A small amount of current will flow

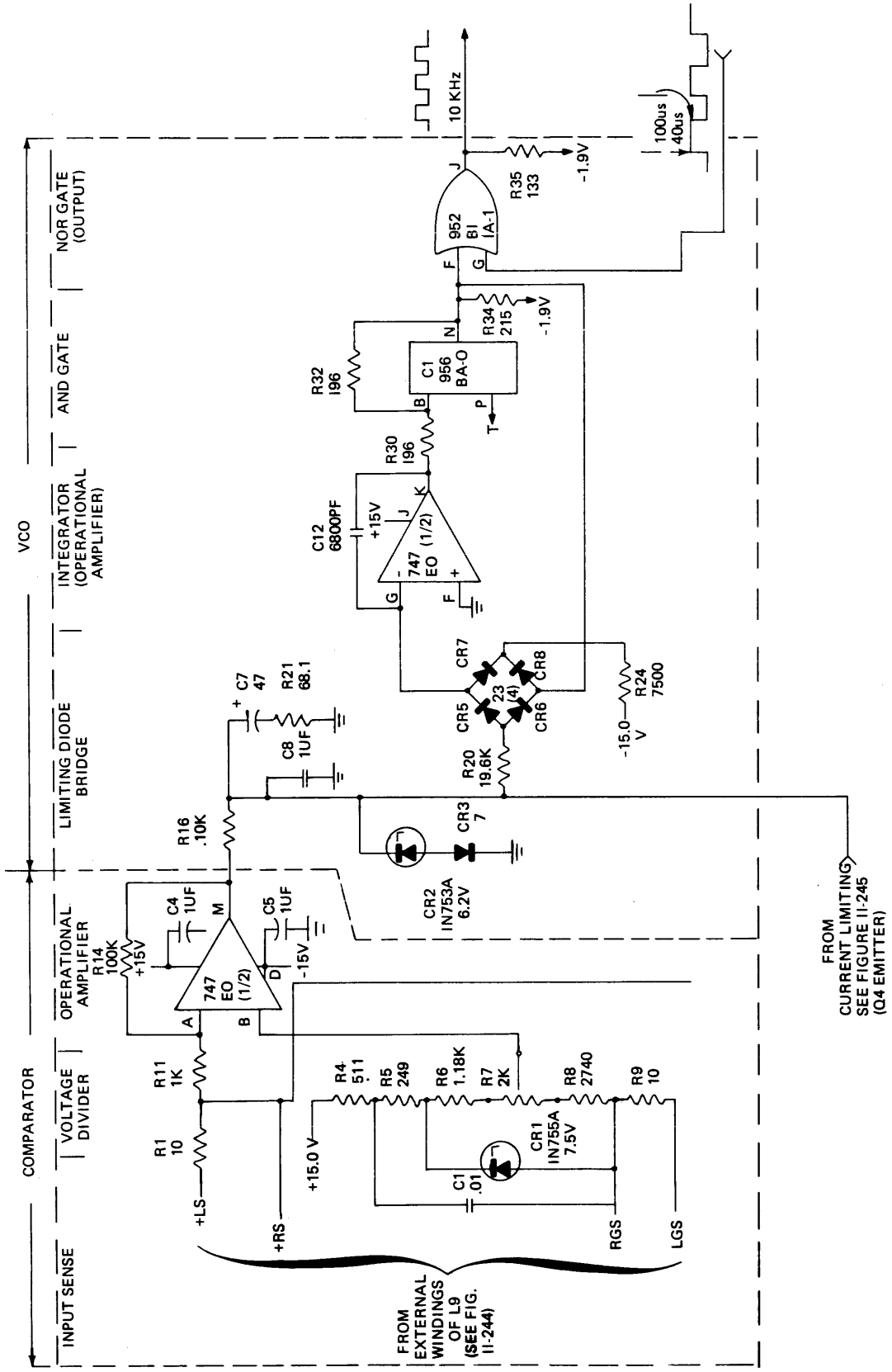


Fig. II-236 COMPARATOR & VCO TIMING

into the diode bridge from the -15V supply, through diodes CR7 and CR5 and through the 19.6K ohm resistor (R20) to the input. The small amount of current is not sufficient to charge the 6800 pf feedback capacitor (C12) high enough to make the negative (-) input to the second operational amplifier above the reference or positive (+) input which is ground potential. Hence, the output of the second integrator (operational amplifier 1/2 747) is high, the output of the AND gate (buffer 956 at location C1) is high, and the output of the NOR gate (inverter 952 at location B1) is low. With the output of the NOR gate held low, there is no oscillation. Therefore, the VCO produces no pulse when the input is either zero volts or -0.6V. When the output of the AND gate is high, the feedback to the junction of diodes CR8 & CR6 in the diode bridge causes diode CR6 to be reverse biased, and diode CR8 to be forward biased.

When the +4.85V (+RS & +LS) supply to the negative (-) input of the operational amplifier of the Comparator circuit is equal to or less than +4.85V, the output of the same, and the input to the VCO circuit is 5 volts or greater than 5 volts due to the amplification of the differential amplifier in the Comparator circuit.

This positive (+) voltage to the input of the VCO circuit will cause the 6800 pf feedback capacitor (C12) to charge up to a few hundred millivolts which is sufficient to cause the negative (-) input to the integrator to be above ground which causes the output of the integrator to drop below zero volts. When the output of the integrator (operational amplifier 1/2 747) is low, the output of the AND gate is low, causing the output of the NOR gate to go high. During the charge time of the feedback capacitor (C12), diode CR6 in the diode bridge is reverse biased and diode CR8 is forward biased. When the feedback capacitor charges sufficiently to cause the output of the integrator to go low, the output of the AND gate is also low. Diodes CR6 and CR8 in the diode bridge are then forward biased thus causing the input current to flow through diodes CR6 and CR8. This provides the time when the 6800 pf feedback capacitor (C12) will discharge through diode CR7 of the diode bridge. When the negative (-) input to the integrator drops below ground potential, the cycle repeats, thus oscillation at the output of the integrator occurs. This oscillation also occurs at the output of the NOR gate which is the input to the Logic Timing circuits. The lower input to the AND gate is a constant true as it's tied to +4.75V. The lower input to the NOR gate provides the external control to the output of the VCO circuit. Its function is explained during the Logic Timing explanation which follows. The -1.9V tied to the input of the AND gate through the 196 and 215 ohm resistors (R32 & R34), and to the output of the NOR gate through the 133 ohm resistor (R35) is used as a pull up and pull down resistor function to increase switching speed.

To summarize the VCO circuit, the higher the input voltage, the faster the feedback capacitor is charged, hence the faster the VCO oscillates. In general, for each increment of 1V input, the VCO oscillates 2 KHZ faster, e.g., 1V input = KHZ output, 2V input = 4 KHZ output; 6V input = 12 KHZ output.

LOGIC TIMER

The function of the Logic Timer is to provide four pulsing outputs in such an order as to trigger the SCR's in the Inverter so that an ON-OFF order can be obtained. Assume for explanation purposes that the input to the Logic Timer circuit is oscillating at 10 KHZ (100 us from leading edge to leading edge). This input is the oscillating output of the VCO circuit. The Logic Timer is described both from the functional standpoint as shown in Figure II-237, and from a detailed standpoint as shown in Figure II-238.

The timing within the Timer Logic may be analyzed in the following steps:

1. In reference to both Figures II-238 & 239, assume the "J" input to the Flip-Flop is initially high (point J) and the "K" input to the Flip-Flop is initially low (point K) when the first output pulse from the VCO circuit is received. The trailing edge of the first VCO output will then cause the "1" output of the Flip-Flop to go high (point B) and the "0" output of the Flip-Flop to go low (point C).
2. Immediately after point B is high, the 5 us Pulse Shaper whose input is point B will output a 5 us pulse. This will cause point L to output a 5 us pulse which causes Gate Drivers A2 and A1 to output, and it causes point N to output a 5 us pulse through gate 1 which causes Gate Driver A6 to also output. The additional delay of gate 1 is negligible at this point.
3. The first output pulse from the VCO circuit received is also applied to the 40 us delay. The output of the 40 us delay Pin 6 (D) will remain low for 40 us and then high for 60 us. The 40 us delay is triggered on the trailing edge of VCO. Immediately after the output of the 40 us delay goes high (point D) the 50 us Pulse Shaper will output a 50 us pulse (point E).
4. The 50 us output pulse at point E is ANDed with the levels from points B & C at gates 3 & 2 respectively. Since point B is high at this time, a 50 us pulse is produced at points G and P. Gate Driver A5 therefore receives a pulse when point P is high for 50 us.

5. When the 50 us pulse appears at point C, there is no signal at point F. Therefore, the RS Flip-Flop is reset. The 10 us Delays at the outputs of the RS Flip-Flop will cause the "J" input to the J-K Flip-Flop to go low immediately and the "K" input to the J-K Flip-Flop to go high after a 10 us delay.

In summary of the previous five steps, Gate Drivers A2, A1, and A6 each received a 5 us pulse immediately following the trailing edge of the first VCO output. The power SCR's A1 and A2 in the Inverter have been triggered, and the comutate SCR A6 has also been triggered. After the 40 us delay Gate Driver A5 received a 50 us pulse therefore causing SCR A5 in the Inverter circuit to be triggered. The output of the Inverter to this point is a positive square wave of +160V for a 60 us duration. It should be noted that Gate Drivers A1, A2, and A6 initially cause the Inverter to output the +160V. Gate Driver A5 receiving a pulse causes the +160V output of the Inverter to return to OV.

6. When the next (second) output pulse from the VCO circuit is received, the trailing edge of this pulse resets the J-K Flip-Flop. Point B goes low and point C goes high.
7. Immediately after the J-K Flip-Flop is reset, a 5 us pulse appears at points M and P, thus causing Gate Drivers A3, A4, and A5 to output.
8. The second output pulse from the VCO circuit is also applied to the input of the 40 us delay. The output of the 40 us delay Pin 6 (D) will remain low for 40 us and then high for 60 us. Immediately after the output of the 40 usec delay goes high (point D), the 50 usec Pulse Shaper will output a pulse at point E.
9. The 50 usec output pulse at point E is again ANDed with the levels from points B & C at gates 3 & 2 respectively. Since the J-K Flip-Flop is at this time reset, point C high, a 50 usec pulse is produced at points F & N. Gate Driver A6 therefore receives a pulse for 50 usec.
10. When the 50 usec pulse appears at point F, there is no signal at point G. Therefore, the RS Flip-Flop is set. The 10 usec delays at the output of the RS Flip-Flop will cause the "K" input to the J-K Flip-Flop to low immediately and the "J" input to the J-K Flip-Flop to go high after a 10 us delay.

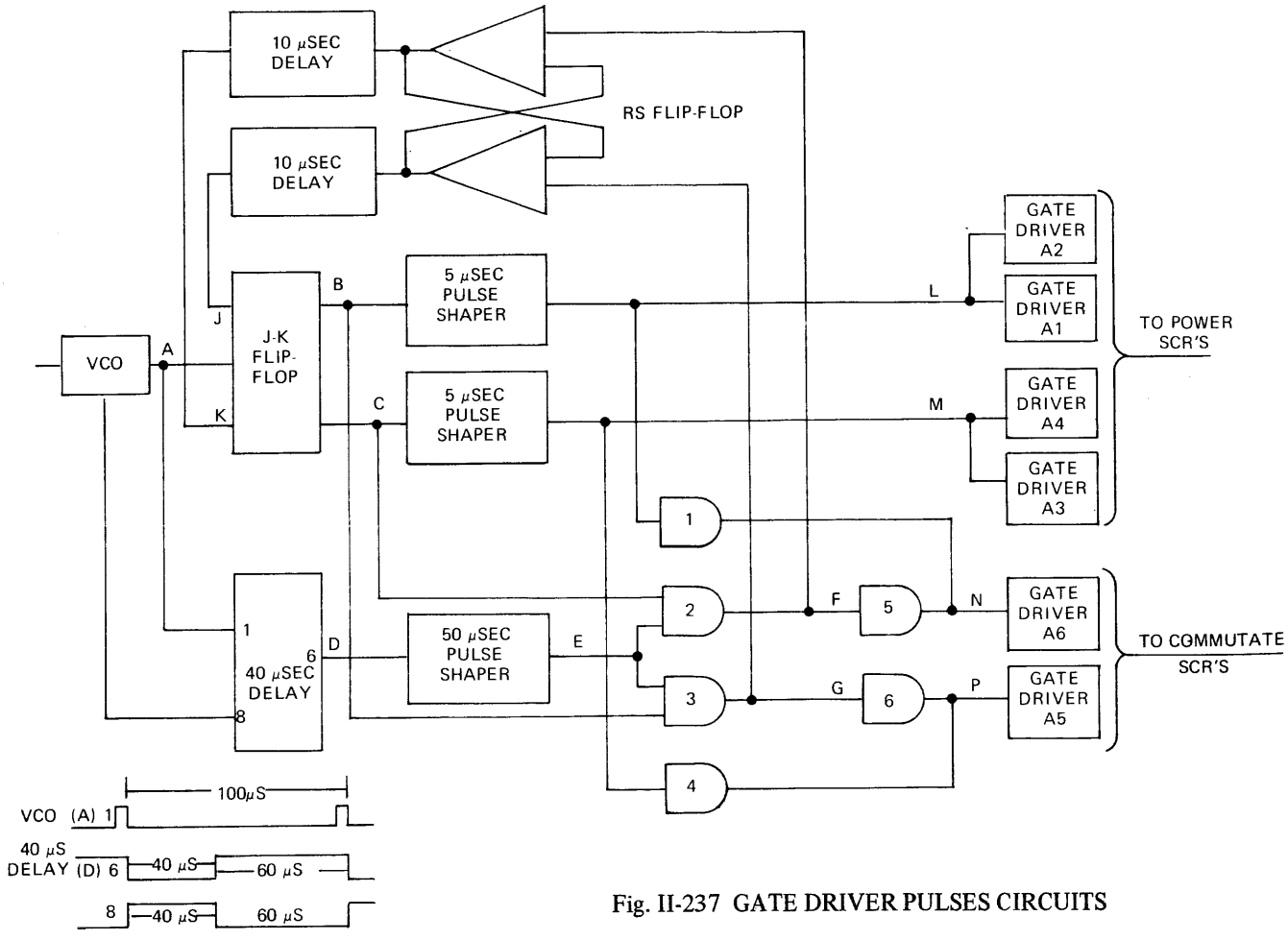


Fig. II-237 GATE DRIVER PULSES CIRCUITS

Functional Detail

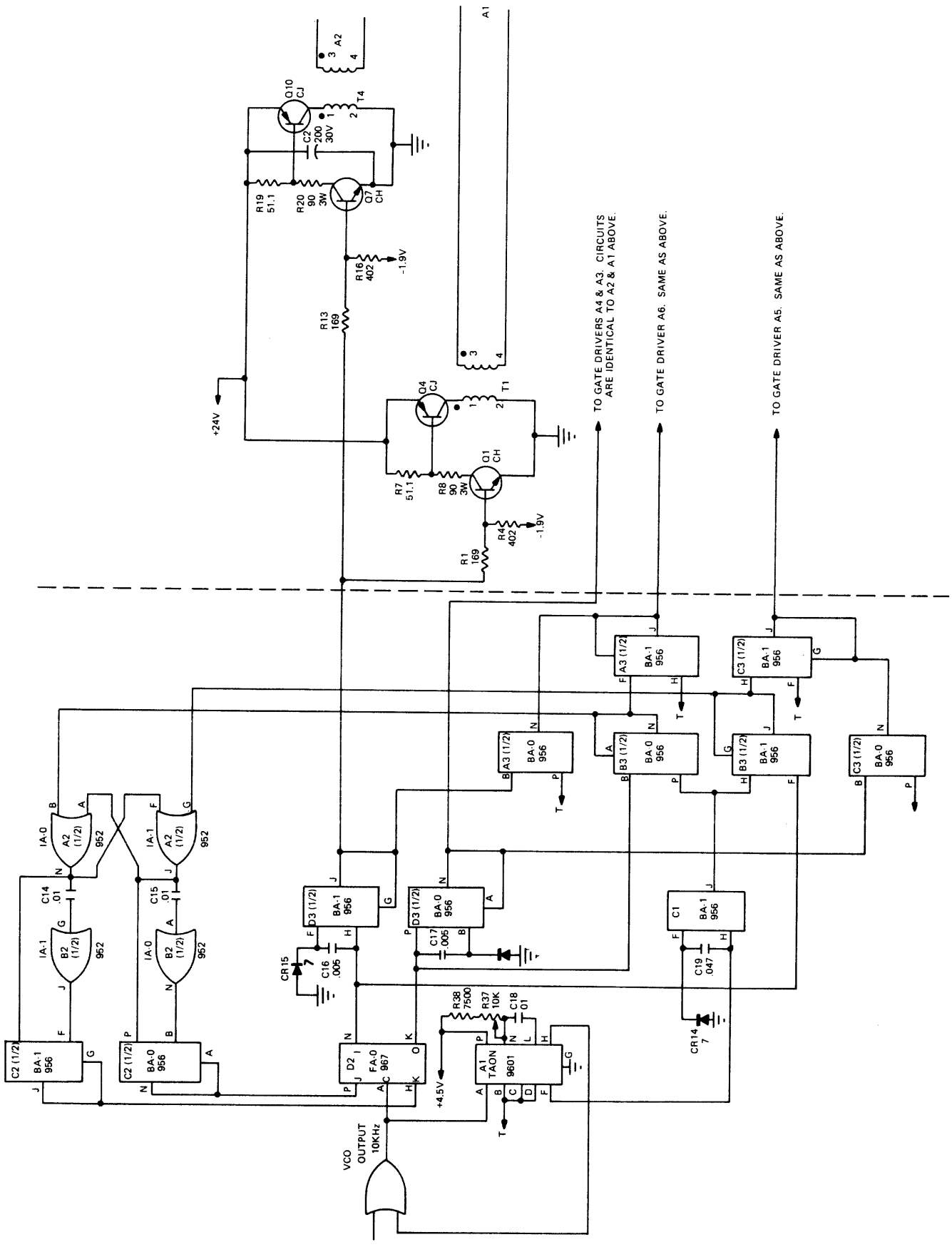
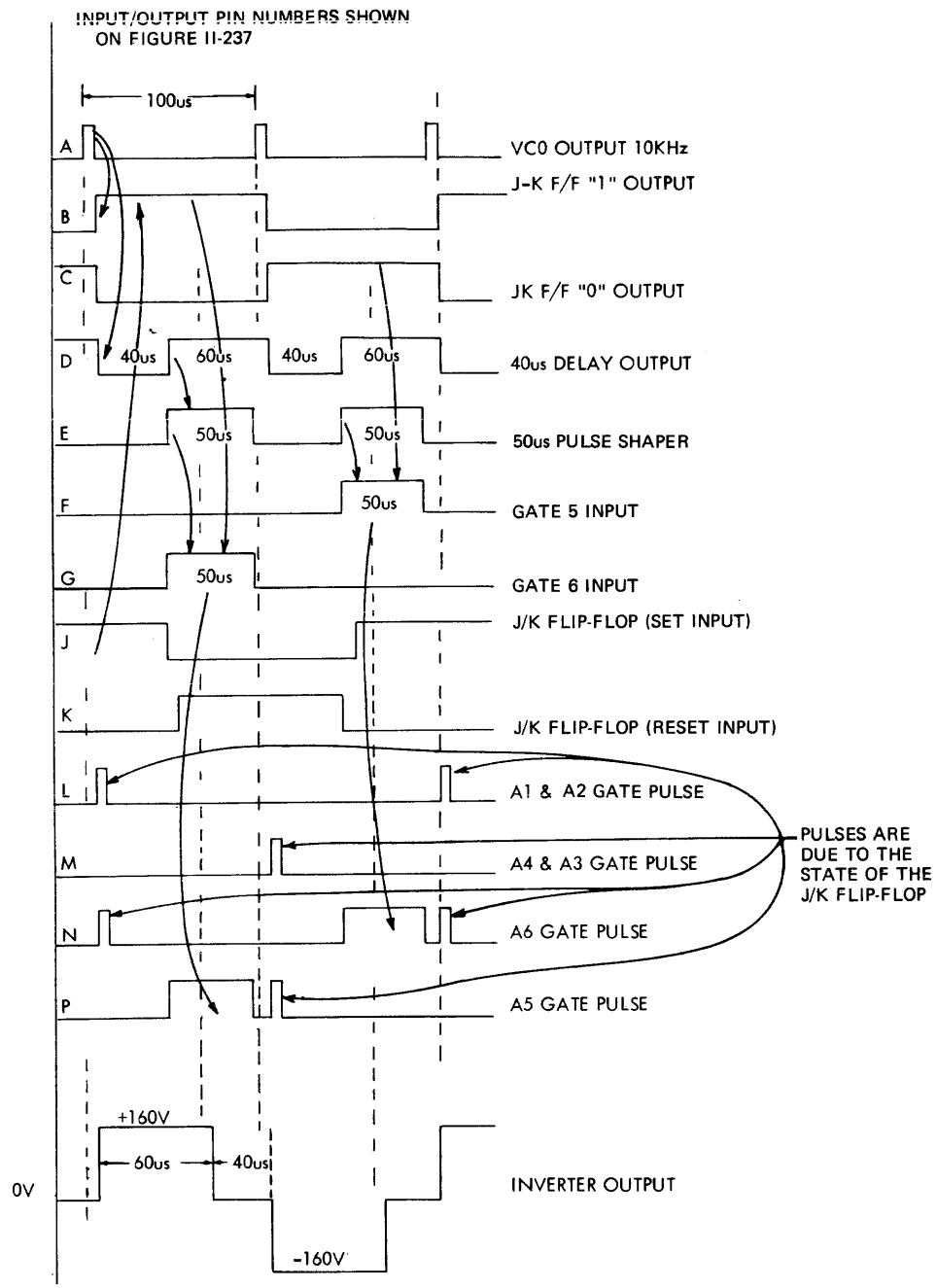


Fig. II-238 "LOGIC" TIMING BOARD GATE DRIVER BOARD

Functional Detail



√ Fig. II-239 GATE DRIVER PULSES

In summary of steps 6 thru 10, Gate Drivers A3, A4, and A5 each received a 5 usec pulse immediately following the trailing edge of the second VCO output pulse. The power SCR's A3 & A4 in the Inverter have been triggered, and the comutate SCR A5 has also been triggered. After the 40 usec delay Gate Driver A6 received a 40 usec pulse therefore causing SCR A6 in the Inverter circuit to be triggered. When SCR's A3, A4 & A5 in the Inverter are triggered, the Inverter outputs a negative square wave of -160V for a 60 usec duration. When SCR A6 is triggered, the output of the Inverter returns to zero volts.

The cycle repeats when the third output pulse from the VCO is received at point A.

NOTE that an inter-lock signal is provided from the feedback of the 40 usec delay (Pin 8) to the NOR gate in the VCO circuit. The signal is high during the time the pulse at point A is being delayed through the 40 usec delay. As the signal is an input to the NOR gate in the VCO circuit, this prevents the VCO circuit from sending any output pules to the Logic Timer until the output Pin 6 (D) of the 40 usec delay is high. The 10 usec delays at the outputs of the RS Flip-Flop provide sufficient time for SCR's A1 and A2 to turn OFF before SCR's A3 and A4 are triggered ON. . . or vice-versa.

±12V DC SUPPLY

Two identical power supplies are provided in the system which produce the -12V DC and +12V DC required for the line drivers and receivers throughout the system. One supply is connected to provide the +12V DC and the other supply is connected to provide -12V DC. When ground is connected to the ±12V COM output the supply is positive. When ground is connected to the ±12V POS output the supply is negative. Note that this is the only difference. The supply is described in five sections as follows:

SECTION A. – INPUT (Refer to Figure II-240)

Secondary windings of Transformer T2 (terminals 6 & 7 or 8 & 9) provide the source voltage for the two supplies. Note the input to Transformer T2 (terminals 1 & 2) is the 320V peak to peak square wave output of the Inverter which is described separately in this manual. The square wave input is rectified by the diode bridge (CR11) consisting of the four diodes as illustrated and filtered by the choke input filter (L-3). The "crowbar" SCR A-8) will short the output, if the output of the supply is over voltage. Pin 1W is connected to the Positive Input and Pin 1V is connected to the Negative Input or ±12V COM.

SECTION B. – VOLTAGE REGULATOR & CURRENT LIMITER (Refer to Figure II-241)

The Positive Monolithic Voltage Regulator (MC1469) provides the heart of either a +12V or -12V regulator. The external switching transistor (Q4) and resistors R22, R27, R28 and R31 provide the heart of the current limiting. The input is applied to Pin 3 of the MC1469 regulator and to the collectors of the two series pass transistors (Q4 & Q14) shown in parallel. The voltage at the Positive Input (Pin 3) is at approximately 20V when operating under minimum load and up to 40V with maximum load. Assuming a voltage of 20.19V at Pin 3, a DC Shift Output voltage is established at Pin 9 of 12.9V. Pin's 9 and 6 are connected, therefore the Output Reference voltage at Pin 6 is established at 12.29V. The voltage divider (R3, R4 and R5) provide a voltage drop such that Pin 8 (DC Shift Sense) is 3.35V. The + Remote Sense tied to Pin 5 is 12.27V when Pin 3 is 20.19V. A change in voltage sensed at Pin 5 (Output Sense) will cause the MC1469 Regulator to function internally in such a way that Pin 1 (Output) will reflect the change inversely.

If the voltage sensed at Pin 5 increases, the voltage at Pin 1 will decrease. Likewise if the voltage at Pin 5 decreases, the voltage at Pin 1 will increase. Pin 2 provides the regulator with Shut Down capabilities when high. The Sequence Input is not used. The Current Limiting circuitry employs the "foldback" current limiting technique which causes the output current to be decreased when the output voltage is decreased due to either an overload or short. Externally connected to the 12V Supply circuit board is a .16 ohm 36 watt resistor (R31-1). Assuming a load of 5 amps passes through the .16 ohm resistor R31-1), a drop of approximately 0.8V is developed across the resistor. The potential at point "A" is therefore 12.8V above the ±12V COM. This voltage at point "A" is shared by the 1K potentiometer (R28), the 100 ohm resistor (R27) and the 12.7K resistor (R22) so that the VBE of transistor Q4 is approximately 0.5V which is insufficient to turn transistor Q4 ON. If the output voltage drops to for example 6 volts due to overload, point "A" is then at 6.8 volts (assuming a full load of 5 amps). Because the potentiometer (R28) is set to a previous setting, the VBE of transistor Q4 is increased to approximately 0.64 volts which is sufficient to turn transistor Q4 ON. With transistor Q4 ON, Pin 4 is drained which therefore reduces the output current.

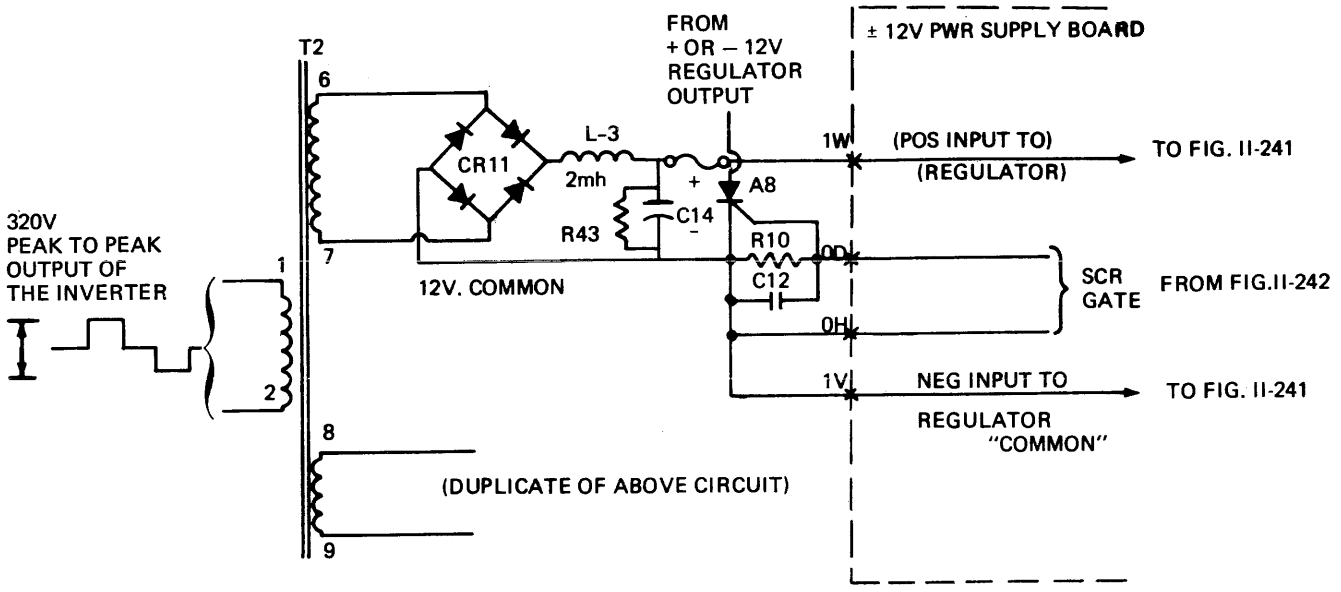
SECTION C. – SEQUENCE CONTROL & VOLTAGE SOURCE (Refer to Figure II-242)

The ±12V Supply is monitored to accept sequence control. In addition the supply will produce Undervoltage, Overvoltage, and "Clear" signals. As the supply output may be either positive or negative, the voltage detecting circuitry requires a voltage source to set a reference. The sequence Control consists of a Switching Transistor (BA) and a current source (AT). These transistors are illustrated as Q1 and Q2 respectively. When the Sequence Input is Low, transistors Q1 and Q2 are OFF, therefore current is not allowed to flow to Pin 2 of the voltage regulator (MC1469). When the Sequence input is high, both transistors are ON and sufficient current will flow to Pin 2 of the regulator (MC1469) to cause the regulator to Shut OFF. The voltage source consists of two zener diodes, (CR1 & CR2), Transistor AT, and two current limiting resistors (R13 & R18).

The voltage source is ON when the +15 volt source boltage is applied. The voltage output (collector of transistor Q3) is clamped at 6.8V above the ±12V COM. Note that at present, the sequence input is not used.

SECTION D. – UNDER VOLTAGE & ONE SHOT (Refer to Figure II-242)

The negative (-) input to the Operational Amplifier (1/2 747) is set to 2.4 volts above ±12V COM and the positive (+) input is at 3 volts when the supply is operating normally. Initially when power is first applied, the high input to the



√ Fig. II-240 ±12V REGULATOR INPUT

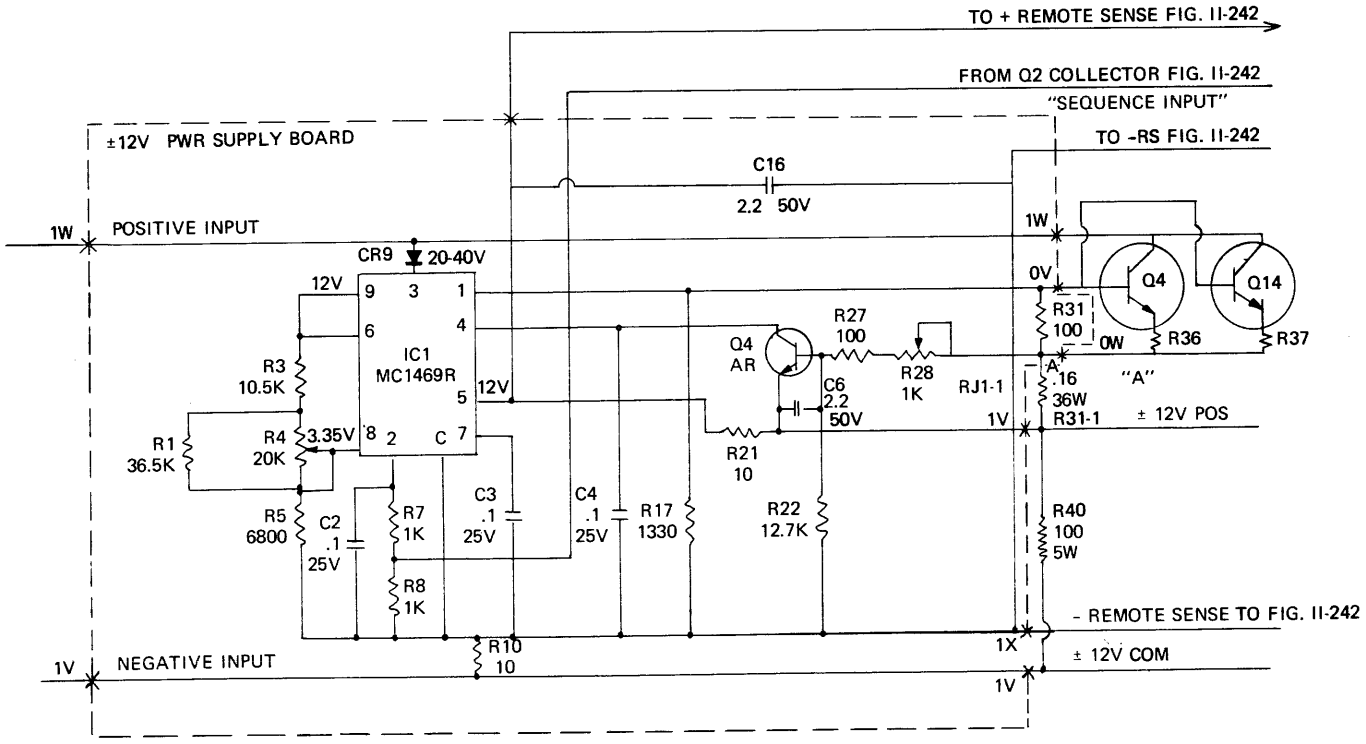


Fig. II-241 VOLTAGE REGULATOR/CURRENT LIMITER

TAON (pins C & D) will cause the output of the TAON (pin F) to output a false for the delay time of the RC external circuitry. This false is inverted in the Processor to produce a General Processor Clear. After the delay times out, the F output of the TAON will go true and remain true as long as the supply is operating normally. An Under Voltage signal is generated (output of the Operational Amplifier low) when the supply drops to approximately 9.6 volts. With the output of the supply at 9.6 volts, the positive (+) input to the Operational Amplifier will approach 2.4 volts which is sufficient to cause the output of the Operational Amplifier to go to zero volts. The Undervoltage condition is not sensed at present; therefore not used.

SECTION E. – OVER VOLTAGE, ONE SHOT, & SCR GATE (Refer to Figure II-242)

The negative input to the Over Voltage Operational Amplifier is set to 3.65 volts above ±12V COM by the voltage divider R14 and R15. The positive (+) input is at 3.0 volts during normal operation. The output of the Operational Amplifier at this time is low and the T output of the TAON is false. If the supply output raises to or above 14.6 volts, the positive input to the Operational Amplifier will increase to approximately 3.6 volts at which time the output of the Operational Amplifier will go high. With the T output high, transistors Q5 and Q6 will turn ON. With Q6 ON, the 30V capacitor (C15) will discharge through Q6 and the primary winding of transformer T1 thus producing a pulse to the gate of the "crowbar" SCR at the input of this supply. The fuse blows and the supply is OFF. Note that the output of the TAON in either the UV or OV circuit is a ONE Shot and the output pulse width is determined by the external RC network. The pulse to the gate of the SCR will be approximately 50 usec. The OV output of the circuit is not used at present to indicate the same however the pulse to the SCR will cause the supply to Power OFF.

+4.85V & -2.0V OUTPUT MONITOR (Refer to Figure II-243)

The function of the Output Monitor circuit is to sense the output voltages of the Logic Supply and produce signals if the outputs are under-voltaged, over-voltaged, or "clear". The circuit also activates the input circuit breaker and trips and turns on the "crowbar" SCR which in turn shorts out the output of the supply when an overvoltage occurs. The circuit consists of four Operational Amplifiers, one Monostable Multi-(TAON), five AND gates, a gate driver and a "coil" or CKT Breaker driver. The upper two Operational Amplifiers monitor the +4.85V output and the lower two Operational Amplifiers monitor the -2.0V output. The upper most Operational Amplifier that monitors the +4.85V senses the Under voltage and the lower Operational Amplifier which monitors the +4.85V senses for Over Voltage. The lower two Operational Amplifiers sense for Undervoltage and Overvoltage in the same manner. As an Under voltage condition of either the +4.85V or -2.0V supply will cause different functions to occur than when an Over Voltage in either supply is sensed, each is described separately as follows:

Under Voltage

The (+) input to the upper most Operational Amplifier which senses uv is approximately +4.48V when the supply is operating normally. The (-) input to this Operational Amplifier is the reference voltage and is set to approximately +3.84V. The output of this Operational Amplifier at this time is high. The third from the top Operational Amplifier which senses for Under Voltage in the -2.0V supply has approximately -2.0V at the (-) input, -1.6V at the (+) input and a high at the output during normal operating conditions. When the +4.85V supply drops below the reference voltage of +3.84V, the output of the top Operational Amplifier will go low which is the UV signal. Likewise if the -2.0V supply drops below the reference voltage of -1.60V (more positive), the output of the 3rd from top Operational Amplifier goes low which is the UV signal for an under voltage in the -2.0V supply. The UV Operation Amplifiers of both the +4.85V and -2.0V supplies provide an initial CLEAR pulse produced when power is first applied. The high outputs of these two Operational Amplifiers are AND-ed at pins F & H of the dual AND gate chip. The output triggers the TAON which will output a false (one-shot) for a preset 5 sec time duration which is determined by the 38.3 resistor and 47uF capacitor. When the output of the TAON (pin F) goes high and with the outputs of both the UV Operational Amplifiers high, the B & P input pins to the dual AND gate chip are true, thus the K1 Relay is picked and the clean signal is removed.

Over Voltage

The 2nd from the top Operational Amplifier senses for an Over voltage in +4.85V supply and the bottom Operational Amplifier senses for over voltage in the -2.0V supply. The +4.85V over voltage Operational Amplifier has approximately +4.85V at the (+) input, +6.54V reference voltage at the (-) input, and a low at the output during normal operating conditions. When the +4.85V supply rises above the +6.45V reference voltage, the output of the Operational Amplifier goes high which is an OV signal. The -2.0V over voltage Operational Amplifier has approximately -2.0V at the (-) input, -2.45V at the (+) input and a low at the output during normal operating conditions. When the -2.0V supply rises above the -2.45V reference voltage (more negative) an over voltage is sensed and the output of the Operational Amplifier goes high. This is the OV signal for an overvoltage condition in the 2.0V supply. When either the +4.85V or -2.0V supply is over voltage, the output of one of the Operational Amplifiers will go high. Each of these outputs is applied to a separate AND gate whose other input is always high. The high output of this AND gate is the input to another dual AND gate chip, pins H, F, P & B. When the output at pin N is high, Q3 and Q4 conduct for 1 Msec which applies +24V to the gate of the "crowbar" SCR in the output of the +4.85V -2V logic supply. This shorts the output voltage. When the output at pin J is high, Q6 & Q5 conduct thus tripping the main circuit breaker at the AC input to the logic supply. On OV condition in either the +4.85V or the - 20 OV supply will cause both the crowbar and the relay trip coil to be activated.

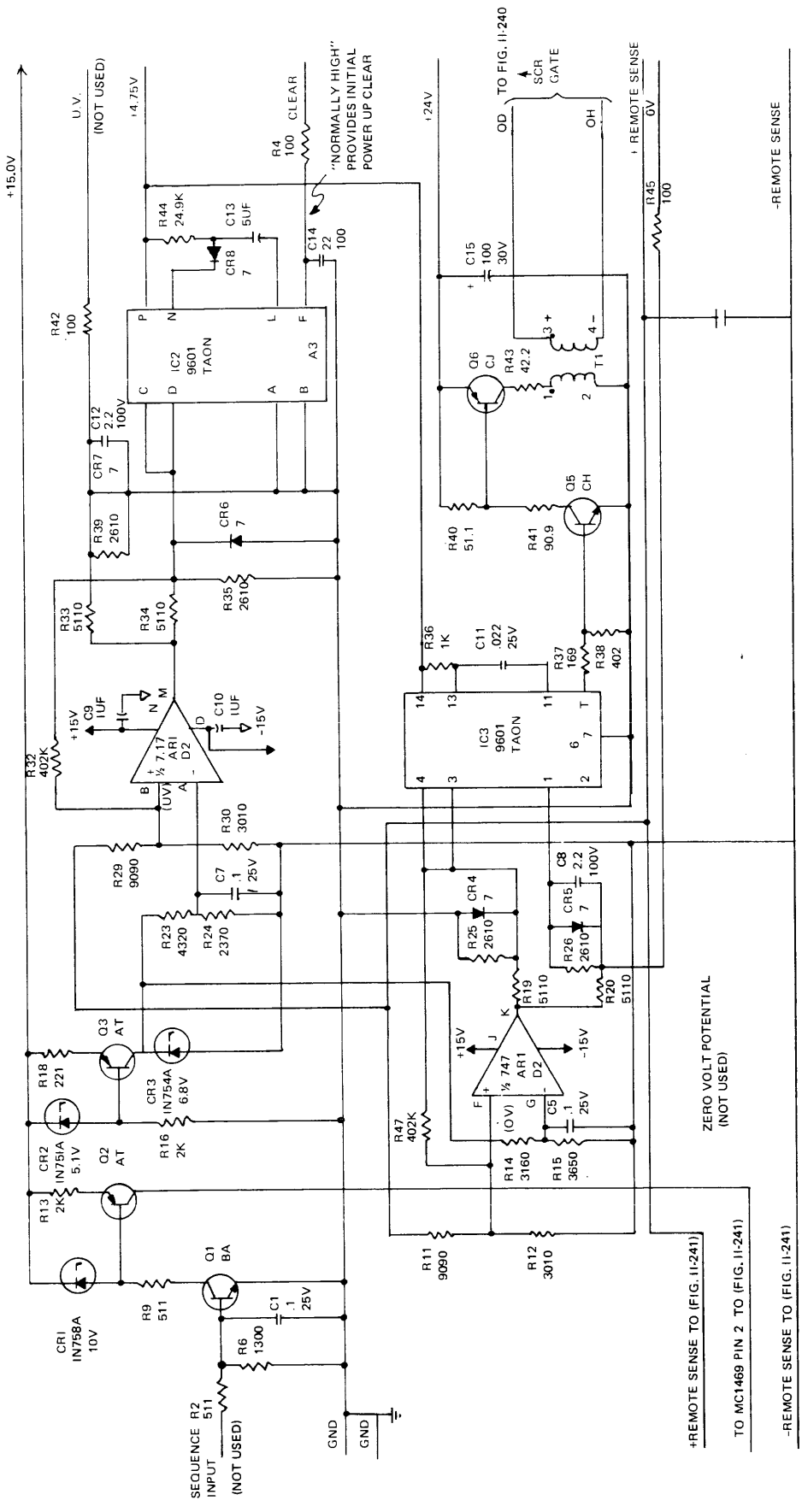


Fig. II-242 ±12V SEQUENCE CONTROL, VOLTAGE SOURCE, AND UV/0V DETECTION

Functional Detail

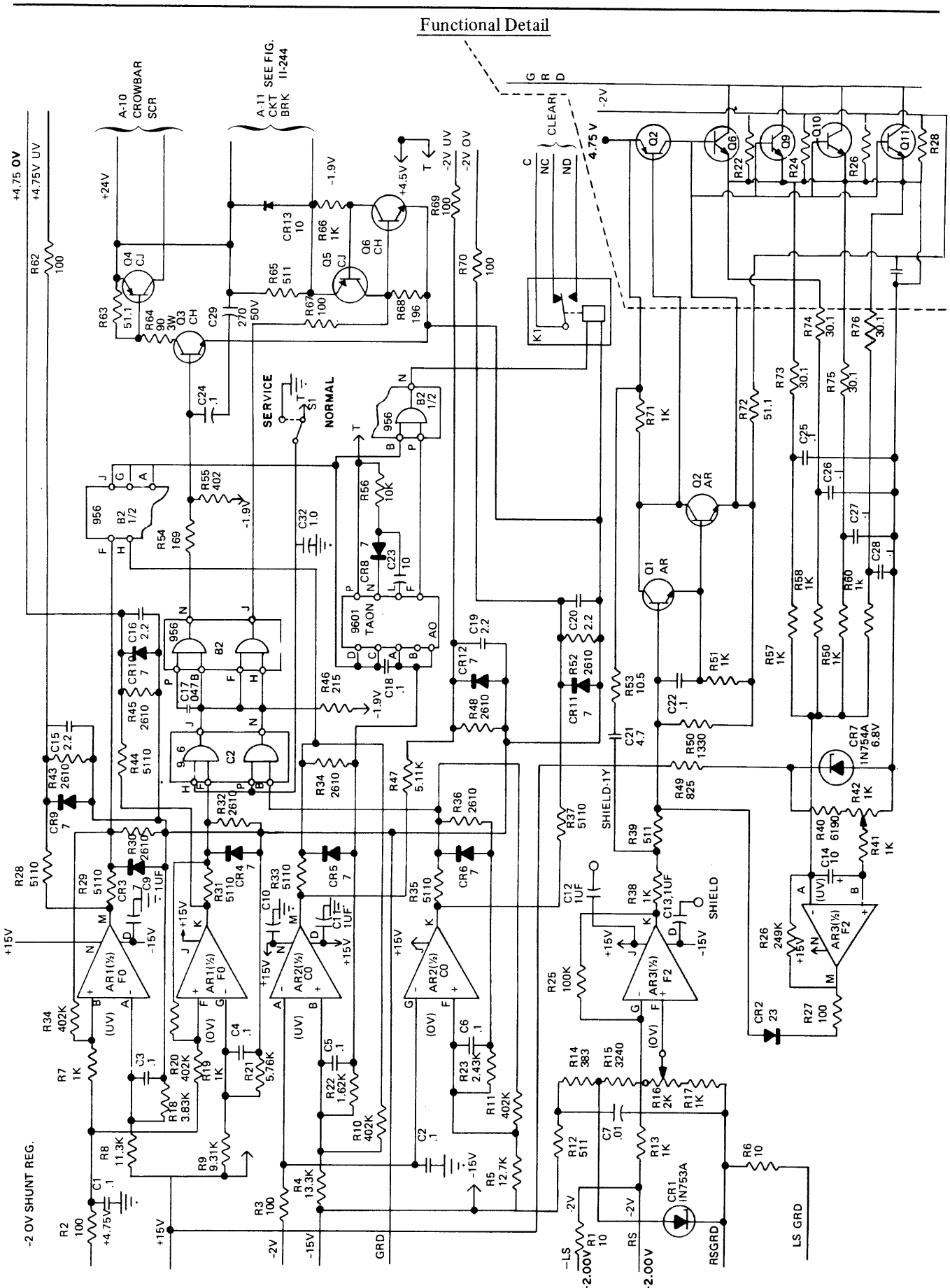


Fig. II-243 -2V SHUNT REGULATOR & LOGIC SUPPLY 0V/UV DETECTION

-2V SHUNT REGULATOR (Refer to Figure II-243)

The purpose of the -2V Shunt Regulator is to control the output current of the -2 volt Logic Supply. The circuit regulates the output current such that a 200 amp output is maintained. The operation of the Regulator is as follows: The -2.0V Remote and Local sensing are connected to the negative (-) input of the first Operational Amplifier through a 1K ohm limiting resistor (R13). Assuming normal operating conditions the voltage at the (-) input is -1.98 volts. A reference level is established by the 6.2 volt Zener (CR1) which is reversed biased by the Remote Sense Ground and Local Sense Ground (RS GRD & LS GRD). The 383 ohm Resistor (R14) limits current flowing through the Zener. The 511 ohm Resistor (R12) also limits the current flow and combines with the 0.01 capacitor (C7) to form a noise suppressor.

The 2K Potentiometer (R16) is adjusted to provide a reference voltage slightly higher than the -1.98 volts which is the (-) input to the Operational Amplifier. The reference voltage therefore (slightly higher) is felt at the (+) input of the Operational Amplifier. This difference is amplified 100 times by the 100K ohm feedback resistor which under normal operating conditions causes the output of the Operational Amplifier to be approximately +1.42 volts. The positive output of the Operational Amplifier causes the Darlington Pair (Transistors Q1 & Q2) to conduct. The RC network (C22 & R51) at the base of the Darlington Pair is used to suppress noise at this point as any noise at this point is amplified 10 to 100 thousand times at the Logic Supply output. The Darlington Pair drives a PNP Power Transistor which in turn drives four NPN high power transistors in parallel. Each of the four high power transistors will carry approximately 25 amps during normal operation (full load).

The 0.02 ohm emitter series resistors (R22, 24, 26 & 28) will have approximately 0.5 volts across each resistor. The series resistors stabilize and balance the current sharing of the four high power transistors (Q6, 9, 10 & 11). The voltage across each 0.02 ohm resistor is sensed and input currents are "summed" by the second Operational Amplifier through the four 1K ohm input resistors. This current sum is compared with the (+) input signal obtained from the 6.8V Zener (CR7) reference diode.

If the sum of the voltages across the 0.02 ohm resistors is more than approximately 2.0 volts, the (-) input of the Second Operational Amplifier will be higher than the (+) input which causes the output of the Operational Amplifier to be less positive or negative. A negative output of the second Operational Amplifier will drain the current from the base of the Darlington Pair thus reducing the output current of the supply. The diode (CR2) at the output of the Operational Amplifier prevents current flow to the base of the Darlington Pair when the output of the Operational Amplifier is high. During normal operating conditions the (+) input to the Operational Amplifier is approximately -1.44V, the (-) input approximately -1.73 volts and the output approximately +14.33 volts. When the sum of the voltages across the 0.02 ohm resistors is more than approximately 2 volts, the voltage to the right of R73, 74, 75 & 76 will go more positive (from approximately -1.5V to -1.0V). This causes the voltage at the (-) input to the Operational Amplifier to also go more positive (from -1.73V to approximately -1.44V). At this time the output goes negative thus draining the current from the base of the Darlington Pair. If the circuit "current limits" although the current is reduced, the output voltage increases therefore causing an Overvoltage condition.

SQUARE WAVE TO DC CONVERTER (Refer to Figure II-244)

Section A. – Transformer and Rectifier Circuit.

The function of the square wave to DC converter is to convert the 320V peak to peak square wave output of the Inverter to DC values as inputs to three power supplies. Secondary windings (terminals 6 & 7 and 8 & 9) are used as inputs to the ±12V DC supplies and are described separately in this manual. Secondary windings 3, 4, & 5 are used as inputs for the +4.85V & -2.0V DC Logic Supply described in this section as follows: The input applied to Transformer T-2 is the 320 volt peak to peak square wave output of the Inverter. The frequency of this input is 5KHz. Secondary terminal 4 provides a center tap and terminals 3 & 5 are connected to rectifier diodes to form a full wave rectifier circuit with an output of 14V across terminals 1 & 4 of the 40 MH choke. When terminal 1 of the primary is positive with respect to terminal 2, terminal 3 of the secondary is positive with respect to terminal 4. During this time rectifier diode CR-21 conducts. When terminal 2 of the primary is positive with respect to terminal 1, terminal 5 of the secondary is positive with respect to terminal 4. During this time, rectifier diode CR-22 conducts, the output across terminal 1 & 4 of the choke is approximately 14V. A Thermostat is connected across rectifier diode CR-21 to sense the heat sink temperature. When the heat sink temperature reaches 120 degrees Centigrade, the contacts open. With the contacts open, the AC input to Transformer T-1 is removed thus disabling the input voltage to the Control Supplies and the +160V Regulator. An immediate Power Down will occur.

Functional Detail

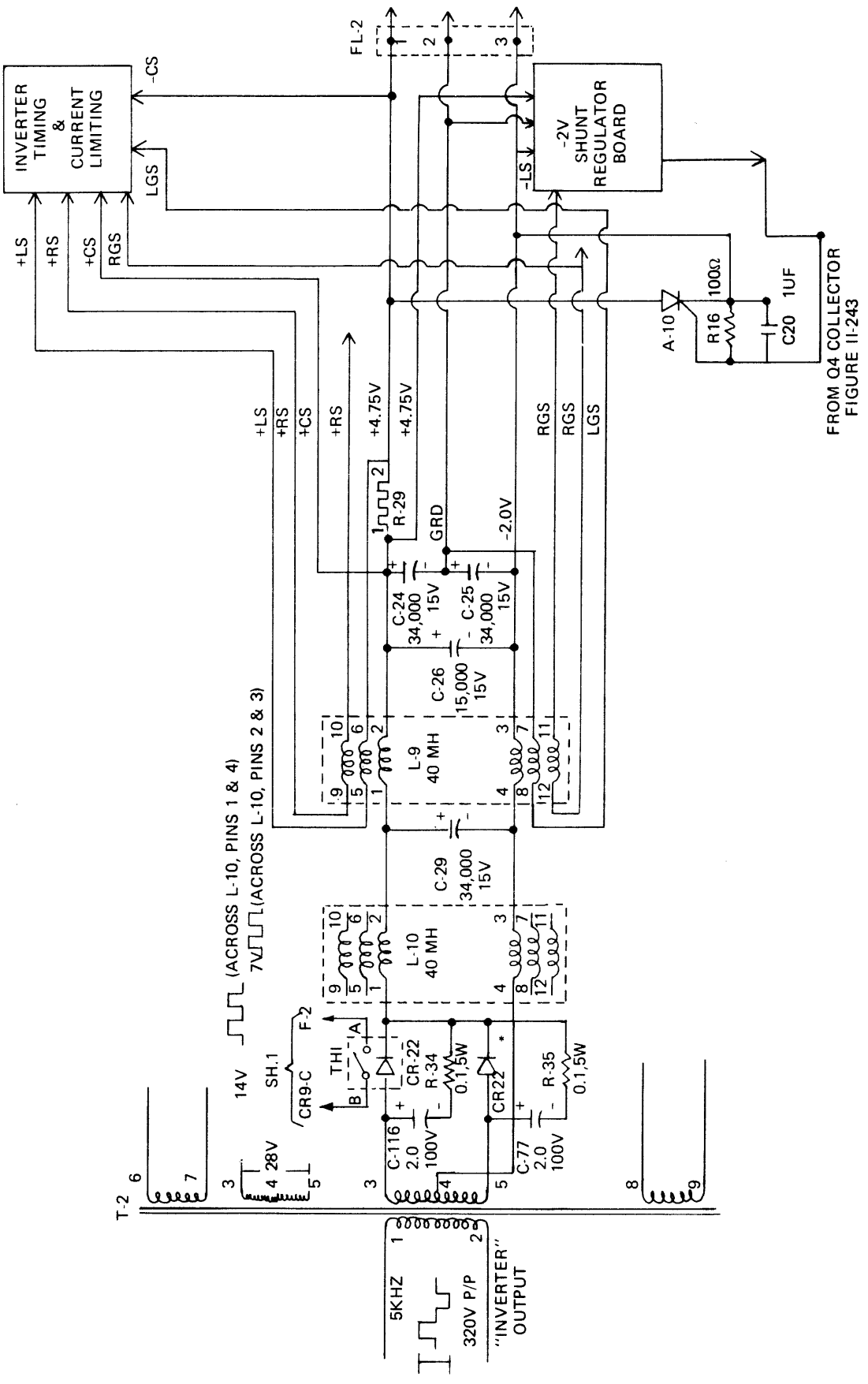


Fig. II-244 LOGIC VOLTAGE OUTPUT CIRCUIT

Section B. – Filter

The filter consists of two LC sections of equal values. Using two LC sections provides better filtering. Two additional windings are added to each half of each of the two LC sections, however only the second LC section has the additional windings connected. The additional windings provide for better stability and also provide a path for voltage level sensing.

The capacitor combination in the second section has approximately the same capacitance as the first section (34KuF). This arrangement establishes the ground. A precision current measuring device (R-29) is used to measure the amount of current flowing. With a 200 amp output the difference of potential across terminals 1 & 2 (+CS & -CS respectively) is approximately 100 m volts. The +CS & -CS output is used in the Current limiting circuit described separately in this manual. The SCR (A-10) is used to short the converter output if the output voltage is too high. The -2V Shunt Regulator provides sensing the load current so that the supply can be shut off if over loaded. The RFI Filter (FL-2) filters any radio frequency interference signals generated inside the +4.85V and -2.0V power supplies.

Current Limiting (Refer to Figure II-245)

The function of this circuit is to monitor the output current of the logic power supply and monitor the input voltage to the inverter. If either the output of the logic supply is overloaded or the input voltage to the Inverter drops, the current is drained from the input of the VCO in the Inverter timing circuit so that the frequency of gate trigger signals to the SCR's in the Inverter is reduced.

CURRENT LIMITING

The function of this circuit is to monitor the output current of the logic power supply and monitor the input voltage to the Inverter. If either the output of the logic supply is over loaded or the input voltage to the Inverter drops, the current is drained from the input of the VCO in the Inverter Timing Circuit so that the frequency of the trigger signals to the SCR's in the Inverter are reduced.

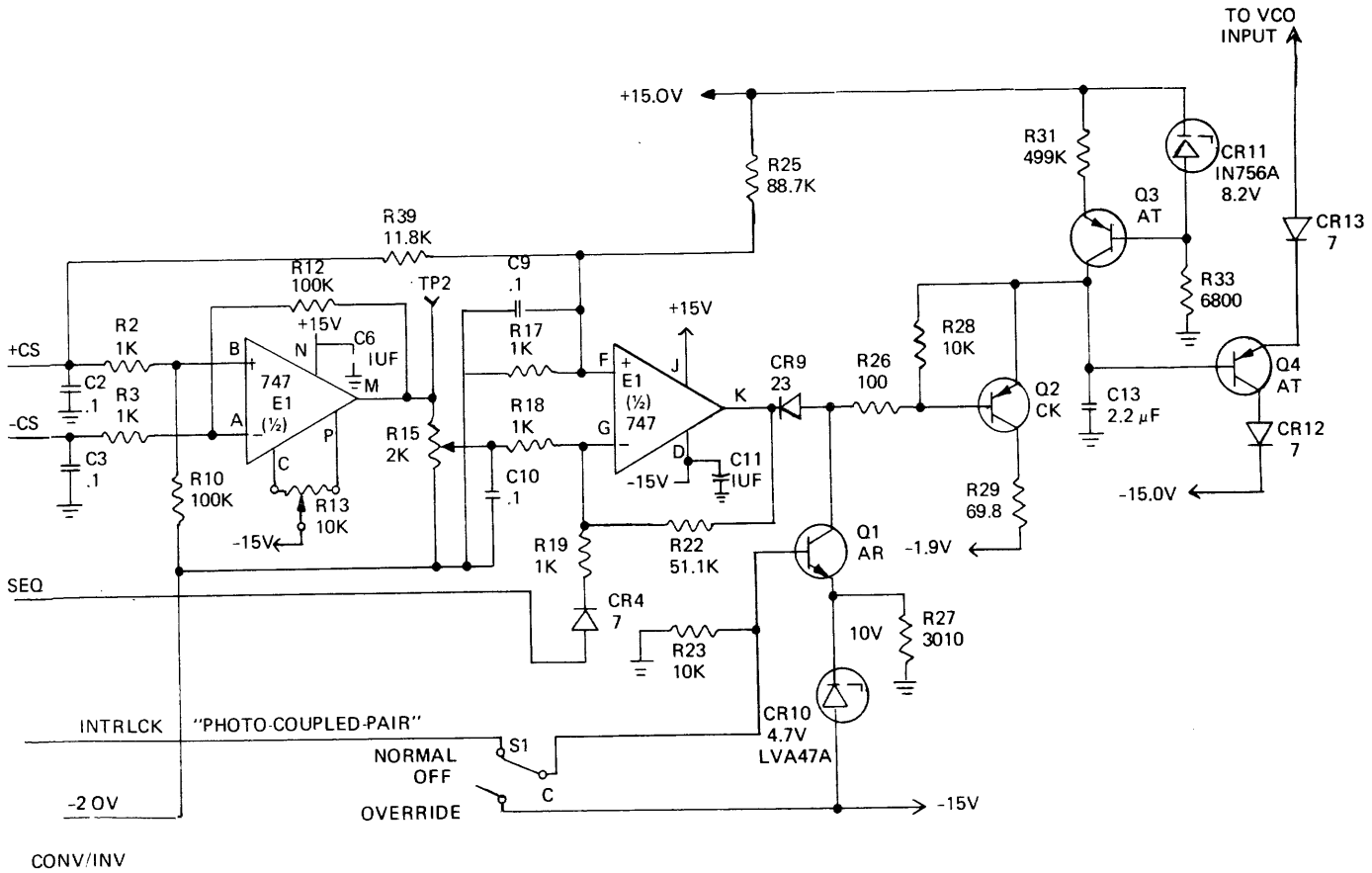


Fig. II-245 VCO TIMING SHUT DOWN

SECTION A. – OP AMP CIRCUIT

Inputs to the first Operational Amplifier are from the current shunt (+CS & -CS) outputs of the current measuring device (R-29). Refer to Section B. Filter of the Square Wave to DC Converter explanation and Figure II-244. Under normal conditions (200 amp load) the difference of potential at the +CS and -CS inputs is approximately 100 volts with the +CS input slightly more positive. With this condition at the input to the first Operational Amplifier, the negative input (-) to the second Operational Amplifier is set close to 0.7 volts. The voltage divider R25 & R39 from the +15 volt & +CS source provides a fixed voltage close to 0.7V to the positive (+) input to the second Operational Amplifier. With the inputs to the second Operational Amplifier approximately equal (– input slightly less than the + input) the output of the second Operational Amplifier is positive. Once the current is exceeded, the shunt immediately provides a difference of potential at the inputs to the first Operational Amplifier greater than 100 mv. The +CS input more positive than the -CS input. The output of the first Operational Amplifier becomes more positive and the output of the second Operational Amplifier becomes more negative. This activates the rest of the circuit to drain current from the input of the VCO circuit. Note that an additional input is provide to the - input of the second Operational Amplifier from Sequence Input (SEQ). Although the Sequence input is not used at present, a high on this input will cause the same effect as would a high output from the first Operational Amplifier.

SECTION B. – SWITCHING TRANSISTORS & CURRENT SOURCE (Refer to Figure II-245)

When the output of the second Operational Amplifier is negative, current is drained from the base of the CK Transistor (Q2) which is turned ON. With Q2 on, current is drained from the current source Transistor AT (Q3) and the 2.2uf capacitor (C13). This forces the base of the second AT Transistor (Q4) to drop to ground potential which therefore causes Q4 to turn ON. With Transistor Q4 on, current is drained from the input of the VCO circuit through diode CR13. This is effectively the means of reducing the frequency of the Inverter when the output of the logic supply is overloaded.

When the input voltage to the Inverter drops below +130V, the AR Transistor (Q1) is turned ON which causes the same actions to occur as when the output of the second Operational Amplifier goes negative. When the +160V DC is above +130V, a Photo-Couple-Pair in the Feedback Circuit of the +160V DC Regulator is ON. This causes -15V to be felt at the base of Transistor Q1, thus Q1 is OFF. Switch S1 is normally in the Normal position at which time the condition of the Photo-Couple-Pair is sensed. When in the OFF position, Q1 is always ON and when in the OVERRIDE position, Q1 is always OFF.

B 1700

CENTRAL SYSTEM

SECTION

III

CIRCUIT
DETAIL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Printed in U. S. America 11-20-72

For Form 1053360

INTRODUCTION

The B1700 Central System utilizes the latest integrated circuit technology. A large variety of I/C chips are employed throughout the logical areas of the system. Some of these are:

1. Multiplexor chips –MFAN
2. Decoders –DFAN
3. Dual Adder/Subtractors –AFAN
4. Three and Four Bit Registers –RFAN, RFBN
5. Etc.

Due to variety and complexity of the internal circuit functions of many of these elements, a logic element rules book has been established. This book illustrates all of the elements utilized within the B1700 Central System.

CRYSTAL OSCILLATOR

The B1700 Central System clocks are developed from the 8 MHZ crystal oscillator shown in Figure III-1. The 2200 8460 video amplifier is the feedback element that maintains oscillations of the crystal. Features of this video amplifier are:

1. Internal input biasing
2. Open collector current source output
3. Output limits, either a positive or negative input overdrive.

FUNCTIONAL DETAIL

The oscillator is connected as shown in Figure III-1. At the start of operation any noise generated by the video amplifier produces a voltage in R_1. A component of this noise is at the series resonance where the crystal looks pure resistive. This is feedback to the input at R_2, since this is positive feedback the amplitude quickly builds up to an equilibrium point where the video amplifier current source is either on or off.

The crystal at series resonance looks like a resistor and forms a divider network with R_2 such that a loop gain of about plus five is formed. At overtone or spurious modes the crystal series resistance is specified to be much higher so the resultant divider network with R_2 lowers the loop gain so much oscillations cannot be maintained in these modes and therefore the oscillator always oscillates at the fundamental frequency.

The other video amplifier output is the same as the output that drives R_1 except that it is out of phase with it. This inverted output drives the divider network of R_3 and the buffer internal pull down resistor. The video amplifier output looks like a current switch of about 6.5 Ma nominal to –12 volts or zero Ma. If R_3 is selected such that the average video amplifier current produces a voltage at the buffer that is its threshold voltage a symmetrical CTL waveform will result.

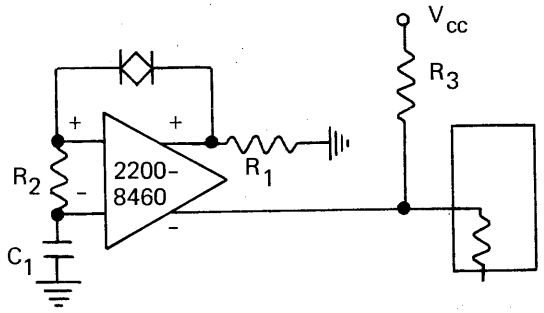


Figure III-1 CLOCK AMPLIFIER CIRCUIT

B 1700

CENTRAL SYSTEM

SECTION

IV

Burroughs

ADJUSTMENTS

FIELD ENGINEERING

TECHNICAL MANUAL

Printed in U. S. America 11-20-72

For Form 1053360

Adjustments

INTRODUCTION

This section covers the following:

1. *Clock Circuit
2. Memory Timing
3. Memory Voltages
4. Logic Voltages

*NOTE: Refer to Section IV (Adjustments in the I/O Base for additional adjustments on the clock.

CENTRAL SYSTEM CLOCK

The Central System Clock Distribution is shown in Figure IV-1. It consists of a 8 MHz oscillator driving a buffer, which is used as a clock driver. The 8 MHz signal from the buffer is passed on to the central system backplane. From the backplane it is distributed to all using cards. In addition, the 8 MHz output from the buffer is used internally on the source card to drive a Divide-By-Two Flip-flop. This produces two phases of 4 MHz (4 MHZ and 4 MHz/). The 4 MHz signal is the basic clock for the system. Both signals are buffered on to the backplane through clock drivers. These signals are distributed on the backplane to all using cards. Figure IV-2 shows the complete schematic of the clock generation on Card K of the processor. For a detailed circuit explanation refer to Section II of the B1700 S-Memory Processor Technical Manual.

TERMINATION

For all these lines, the receiver which is the farthest away from the source is terminated by a resistor on the backplane of the card. The value of the resistor is selected to load the driver to approximately 20 CT, ul loads.

CLOCK OUTPUT TO THE I/O BASE

The 4 MHz signal also passes through a buffer into a delay line of (50 nanoseconds). This in turn is routed through a buffer to a standard 95.3 ohm coaxial cable to the I/O distribution card. The output is I/O CLK. This buffer has its output connected through a pull down resistor, 178 ohm, 1/2 watt to -2 volts.

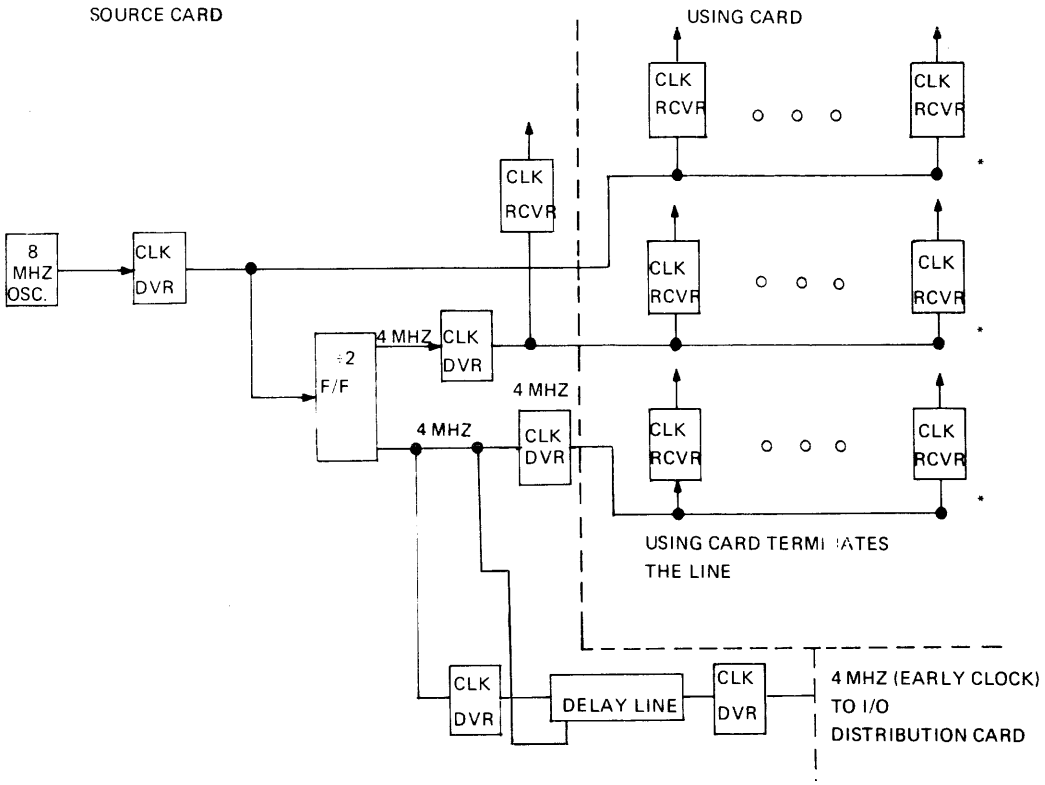


Fig. IV-1 CENTRAL SYSTEM CLOCK DISTRIBUTION

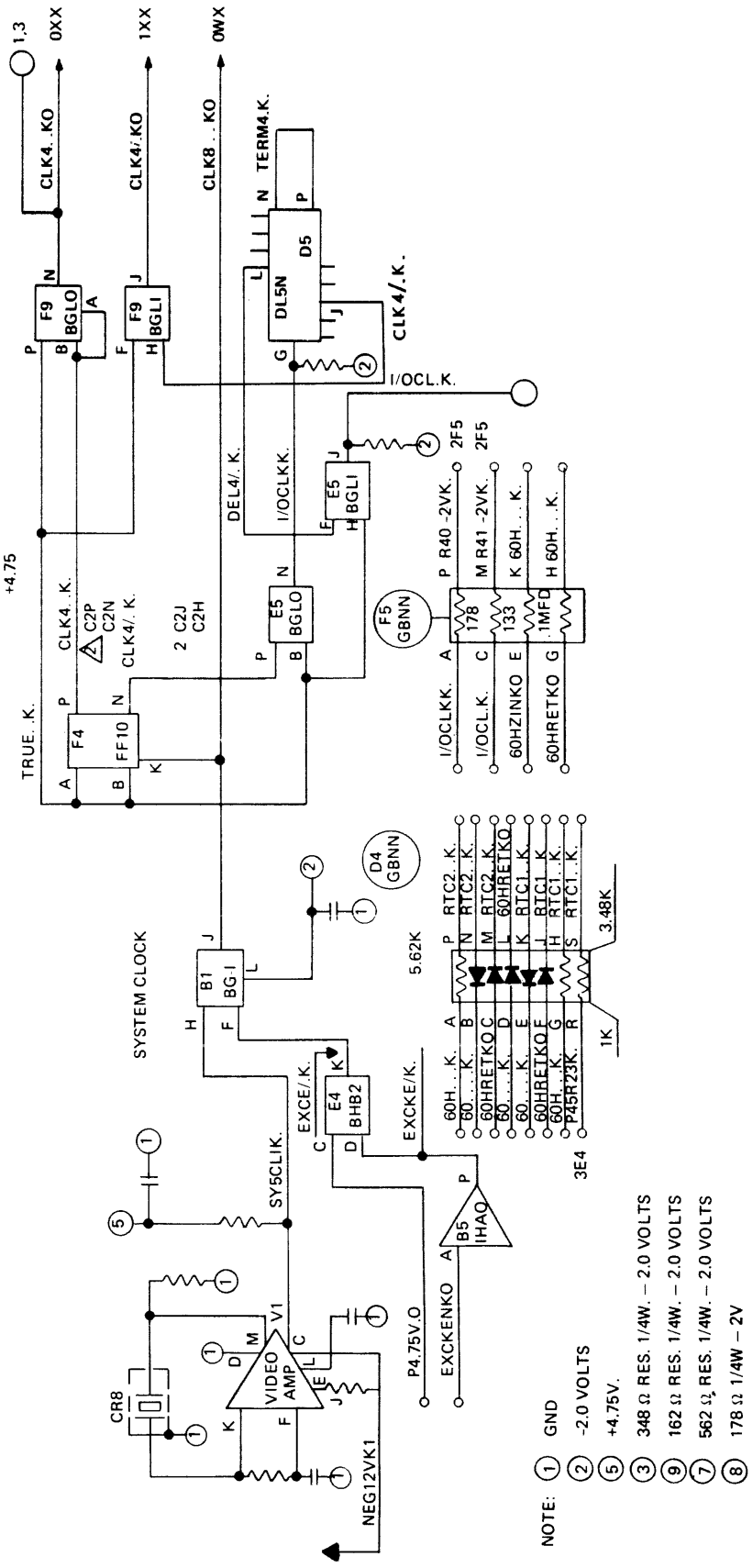


Fig. IV-2 SYSTEM CLOCK

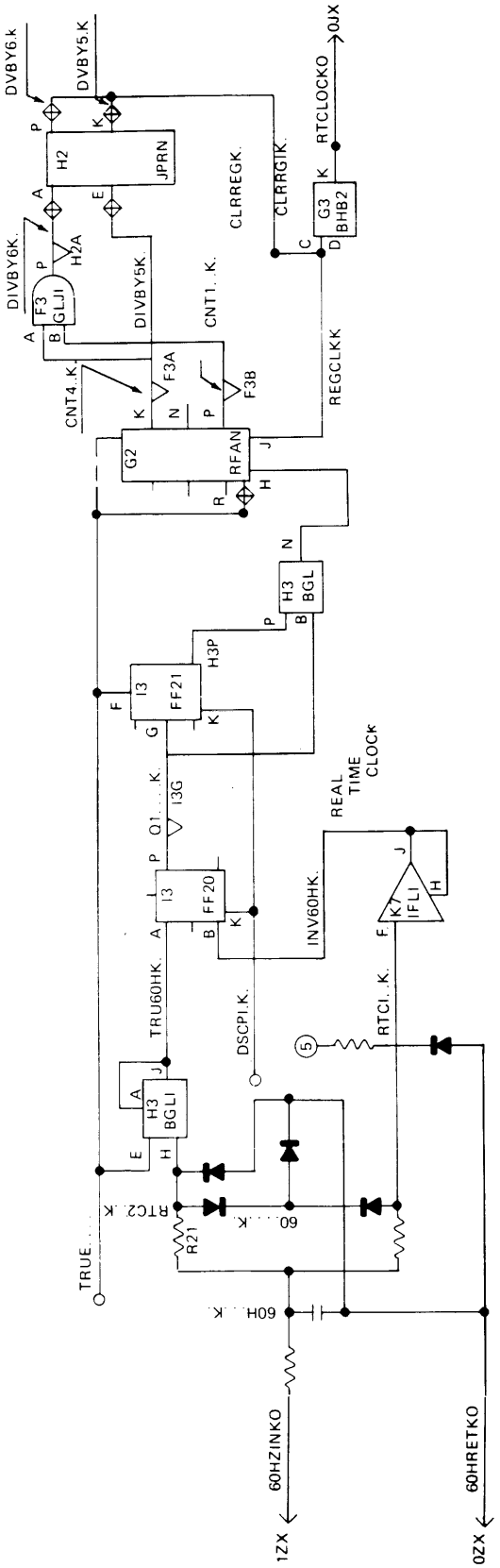


Fig. IV-3 REAL TIME CLOCK

REAL TIME CLOCK (RTCLOCKO)

Figure IV-3 shows the circuitry for the generation of real time clock on Card K of the processor. The levels 60HZINKO and 60HRETKO are outputs from the secondary of a transformer in the 240 distribution box. For a detailed circuit explanation, refer to Section II of the B1700 S-Memory Processor Technical Manual.

CLOCK DISTRIBUTION

The clocks developed on Processor Card K are:

1. CLK8 . . KO
2. CLK4 . . KO
3. CLK4/ . KO
4. I/OCL . K
5. RTCLOCKO

These five clocks are distributed to cards and pages listed in Figure IV-4

Card	Backplane Pin	Page	Source Clock Level	Internal Card Signal Generated
A	OWY	1	CLK4/KO	LBUFCKA
B	OWX	1	CLK4/KO	LBUFCKB
C	OWX	6	CLK4 . . KO	SCPM4 . . C
E	OWX	2	CLK4 . . KO	SCPM . . E.
F	OXX	1	CLK4 . . KO	SCPM4 . F.
F	OWX	1	CLK8 . . KO	SCPM8 . F.
F	OJX	5	RTCLOCKO	CC2 . . . F.
H	OWX	1	CLK4 . . KO	DSCP . . H.
J	OWX	1	CLK4 . . KO	DSCP4 . J.
K	OXX	1	CLK4 . . KO	DSCP4 . K.
K	OXX	3	CLK4 . . KO	DSCP1 . K.
K	IXX	5	CLK4/ . KO	I/OCL . K.

Fig. IV-4 CLOCK BACKPLANE PINS

SYSTEM CLOCK CHECKS

All illustrated wave shapes were taken using Tektronix 453 scope with 10 to 1 probes.
Purpose: To verify that the correct relationship between the system clock exists.

I. Processor
   A. Procedure
      1. Plug in all processor cards.
      2. Power up system
      3. System in halted state
      4. Verify that wave shapes displayed on the scope coincide with the appropriate illustration.
      5. Amplitude – Verify that the true level of both clocks are greater than the + 2.4 volts and the false level is more negative than - 0.4 volts.
      6. Verify that the fall time measured from ground to the 2 volt level is less than 15NS on both clocks (8MC and 4MC).

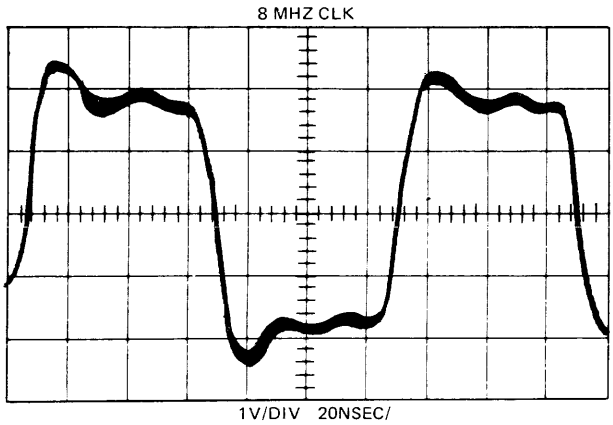


Fig. IV-5 8 MHZ CLOCK

B. 8 MHz Clock (Figure IV-5)
   1. Scope Settings
   2. Sync – internal positive
   3. Sweep Mode – Normal
   4. Horiz. Display – A
   5. Mag on = x10
   6. Time Base = .2/usec } = 20 nanoseconds per division
   7. Probe A = Card K Pin OXW
   8. Adjustment - None

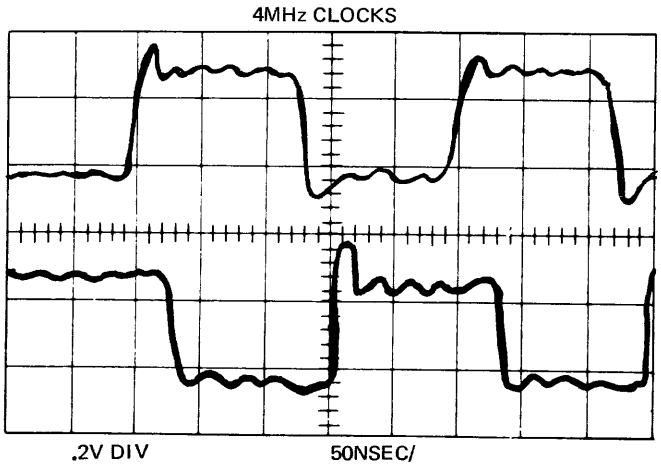


Fig. IV-6 4 MHZ CLOCK

C. 4 MHz Clock (Figure IV-6)

1. Scope Settings
2. Sync – External Positive
3. Volts Div – .2
4. Sweep Mode – Normal
5. Horiz. Display – A
6. Mag on – x10
7. Time Gase – .5 usec } = 50 nanoseconds per division
8. Mode – Alternate
9. Probe A – Card K Pin OXX
10. Probe B – Card K Pin 1XX
11. External Sync. – Card K Pin 0XW
12. Adjustment – None

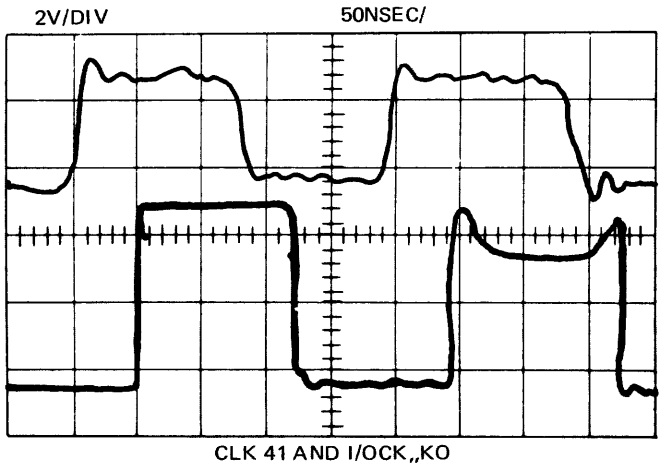


Fig. IV-7 I/O CLOCK – 250 NANOSECONDS

I/O CLOCK – 250 nsec (Figure IV-7)

D.

1. Sync. – Internval Positive, Channel 1
2. Volts Div – .2
3. Sweep Mode – Normal
4. Horiz. Display – A
5. Mag on – X10
6. Time Base – .5 usec } 50 ns/Div.
7. Mode – Alternate
8. Channel 1 – Card K Pin 1XX
9. Channel 2 – Card K Coax Connector Output
10. Adjustment: Card K – Page 5 – Chip D5 pin L is the normal position.

E. Real Time Clock (Figure IV-9)

1. Sync – Internal Positive
2. Volts Division – .1
3. Sweep Mode – Normal
4. Horiz. Display – A
5. Time Base
6. Probe A – Card K Pin OJX
7. Adjustments:

Card K – Page 5 – Chip H2
Jumper Chip
60 Hz Input Power – Pins A to P
50 Hz Input Power – Pins E to K

8. A Constant Voltage Transformer located in the 24 Volt Relay Box (mounted behind the A.C. Distribution Box), is used to generate Real Time Clock. The wiring to Terminal Board One should be checked to ensure that this transformer is correctly connected to the system as shown in Figure IV–8.

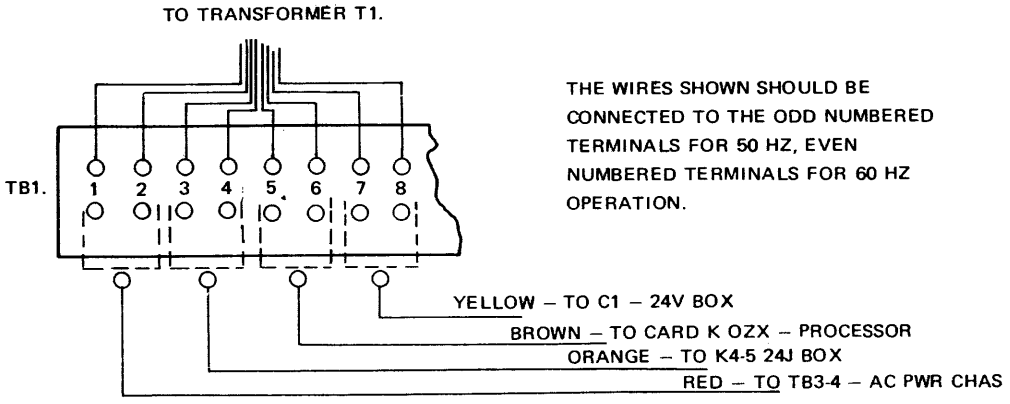


Fig. IV-8 REAL TIME CLOCK CONNECTIONS 50/60 Hz

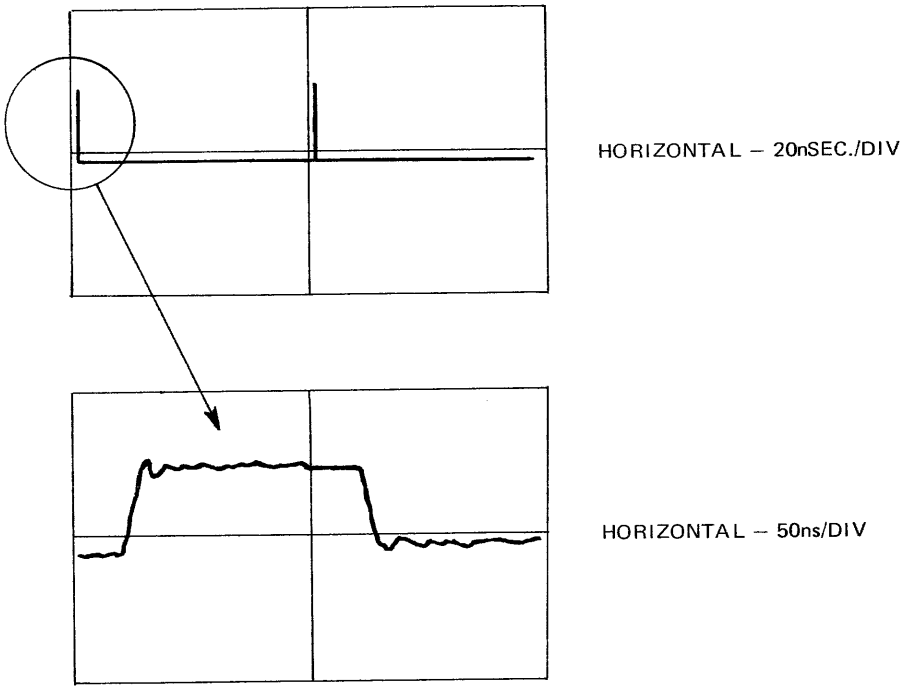


Fig. IV-9

MEMORY TIMING ADJUSTMENTS

All adjustments for memory timing are factory selected and installed. All adjustments are accomplished through a network of delay lines and are considered to be permanent for the particular style and size of memory. No memory timing adjustments should need to be made unless more memory is added or any components that affect timing are replaced. The instructions below are to be done in sequence; if they are not, bear in mind what other adjustment might be affected.

Two memory timing adjustment procedures are provided:

1. K2 Adapter Card (2 MHz)
2. K1 Adapter Card (4 MHz)

ADJUSTMENTS K2 Adapter Card (2 MHz)

Initial Set-up

For starting alignment of a new K2 card or for a reference point, the jumper chips should be wired as shown in Figure IV-10.

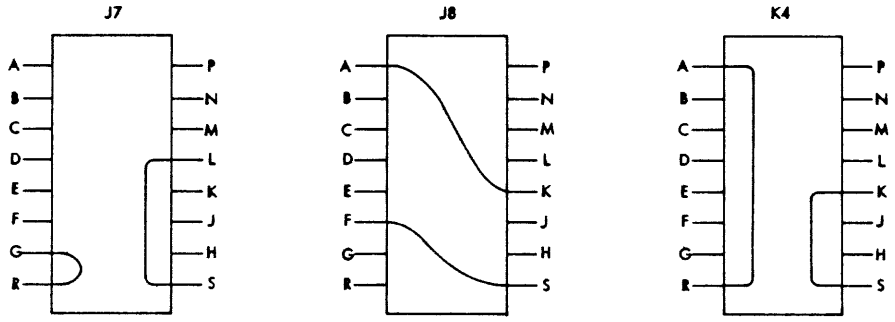


Fig. IV-10. JUMPER CHIP SET-UP

Procedure

Measurements should be made using a CALIBRATED Tektronix 453A or equivalent oscilloscope with EQUAL length x 10 probes. Probes must be grounded at processor backplane. Check probes for proper calibration. ALL measurements will be made at the 1 volt level. Adjustments should be made in sequence listed. Refer to Figure IV-11.

STEP 1 – CHIP ENABLE (CE) LEADING EDGE

A. Set up scope as follows:
   Vertical – .1v/cm (x10 probe = 1 volt)
   Mode – Alternate
   Horizontal – .1us (200 ns)/cm
   External trigger – MSTARTFO (CARD K, Pin 1YY)
   Channel 1 – CLK2 . . KO (Card K, Pin OXX)
   Channel 2 – CENABLKO (Card K, Pin ORY)
   Machine is in idle state.

B. Obtain wave form shown in Figure IV-12.

C. Change scope time base setting to .2us/cm and center CE leading edge with horizontal control. Turn on the X10 magnifier. By adjusting the horizontal control, set the leading edge of CE and the trailing edge of the last clock as shown in Figure IV-13. Time base is set to 20 ns/cm (.2us x10).

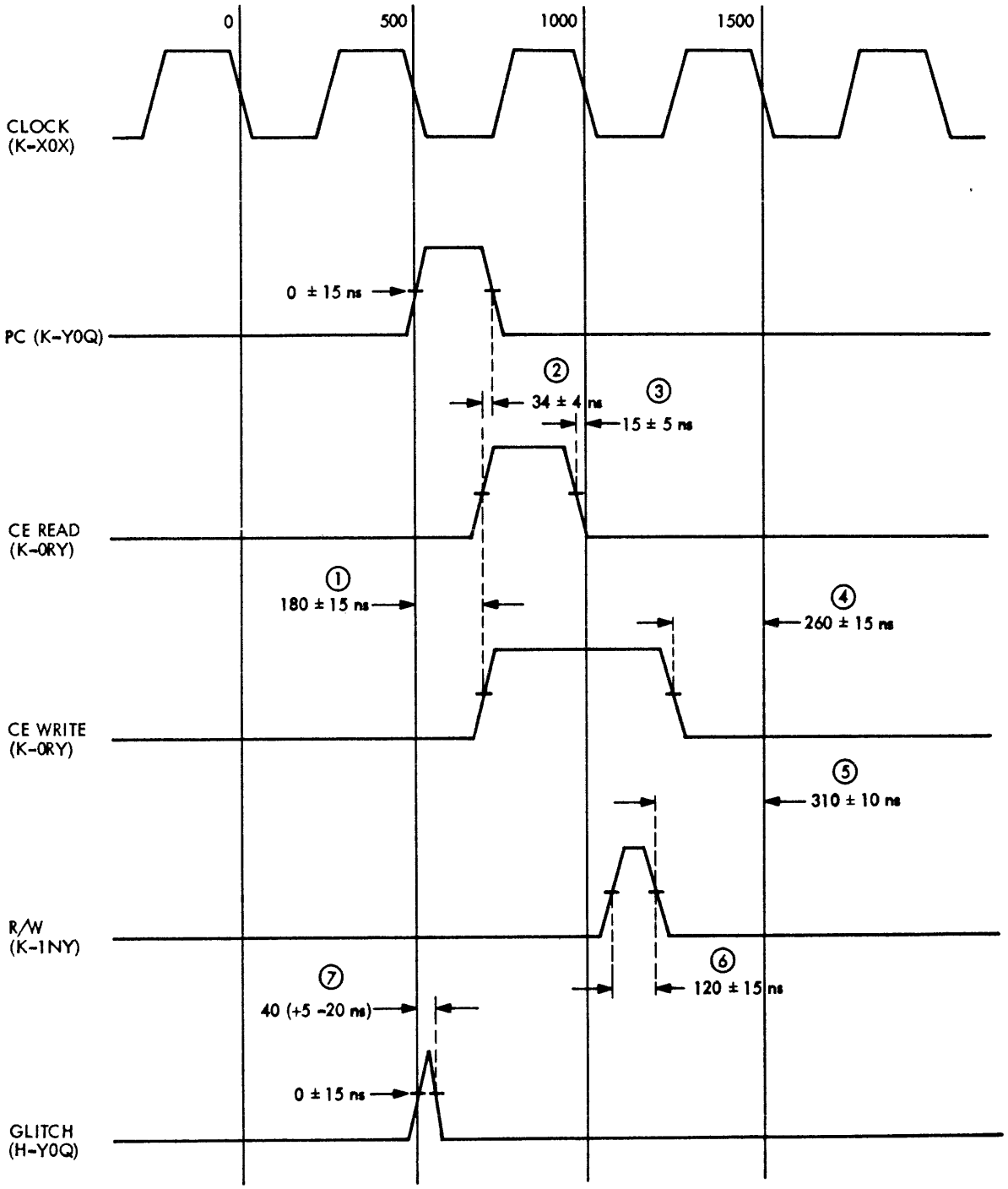


Fig. IV-11. K2 ADAPTER MEMORY TIMING

NOTE
For steps 1, 2 and 3 sync on
MSTARTFO (Card K, Pin 1YY).

For steps 4, 5, 6 and 7 sync on
SWRITEFO (Card K, Pin ONY).

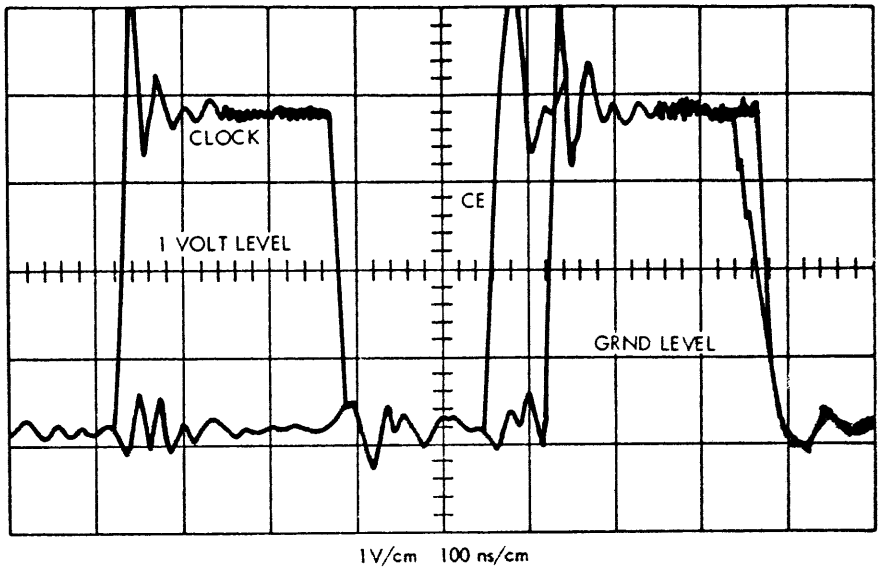


Fig. IV-12. CE LEADING EDGE

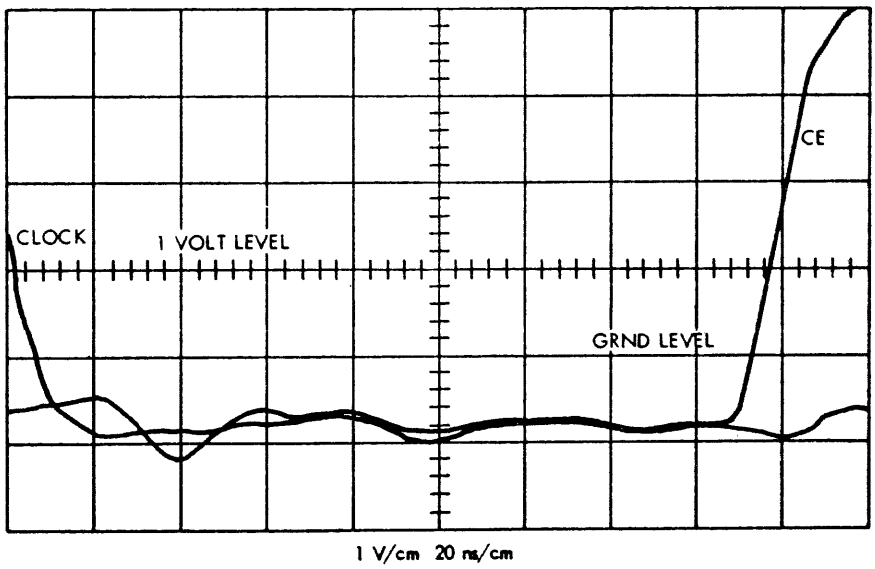


Fig. IV-13. CE LEADING EDGE AND CLOCK

D. The trailing edge of clock to leading edge of CE should be 180 ns. If this adjustment is off greater than 10 ns, a coarse adjustment is necessary. For less than 10 ns a fine adjustment is necessary.

Coarse Adjustment

Delay line K7 is controlled by jumpers wired at jumper J7. Pin R is the output of the jumper and will be wired to pin D, E, F, or G.

Fine Adjustment

Delay line K8 provides fine adjustment. This delay is controlled by jumper chip J8. Pin S is the jumper chip output and will be wires to pin F, H or J.

Step 2 – PRECHARGE (PC) TRAILING EDGE

A. Set up scope as follows:
   Vertical – .1v/cm
   Mode – Alternate
   Horizontal – .lus (100NS)/cm
   Est. Trigger – MSTARTFO (Card K, Pin 1YY)
   Channel 1 – ENABLKO (Card K, Pin ORY
   Channel 2 – ENABLKO (Card K, Pin ORY)
   Machine is in idle state.

B. Obtain wave form shown in Figure IV-14.

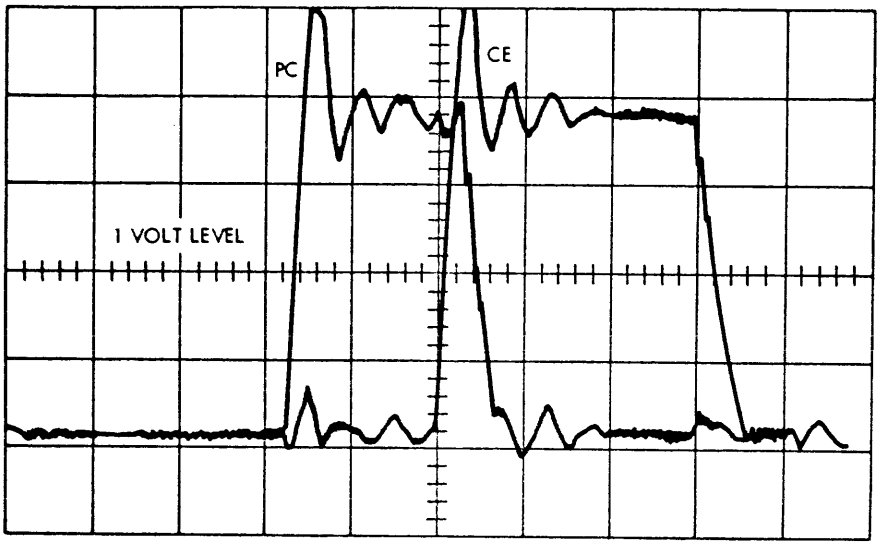


Fig. IV-14. PC TRAILING EDGE

C. Turn on X10 magnifier. Manipulate horizontal control to obtain the waveform shown in Figure IV-15. Time base is set to 10 ns/cm.

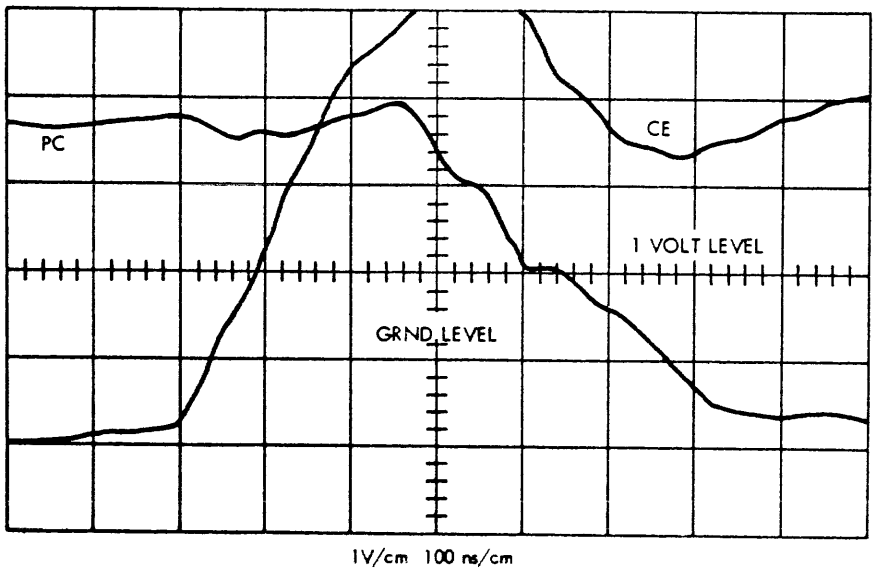


Fig. IV-15. PC AND CE

Adjustments

D. The trailing edge of PE should be 34 ns from the leading edge of CE.

Adjustment

Delay line K8 provides adjustment. This delay is controlled by jumper chip J8. Pin A is the PC output of the jumper chip and will be wired to Pin H, F, J, E, K, L. C. M. B. or N.

STEP 3 – CHIP ENABLE TRAILING EDGE

Read Cycle

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Alternafe
Horizontal – .1us (100ns)
External Trigger – MSTARTFO (Card K, Pin 1YY)
Channel 1 – CLK . . KO (Card K, Pin OXX)
Channel 2 – CENABLKO (Card K, Pin ORY)
Machine is in idle state.

B. Obtain wave form shown in Figure IV-16.

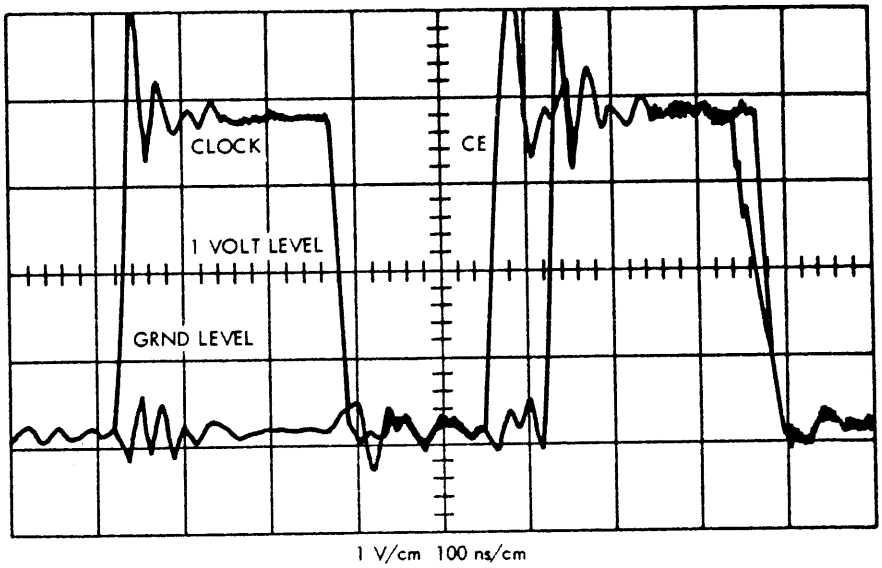


Fig. IV-16. CE TRAILING EDGE

C. Manipulate CE trailing edge to the center of screen with the horizontal control. Turn X10 magnifier on. Obtain wave form shown in Figure IV-17.

D. Trailing edge of CE should be 15 ns $\pm$ 5 nx before trailing of clock. CE trailing edge is controlled by delay line J6. Jumper chip J7 provides for adjustment. Pin S is the output of the jumper chip and will be wires to Pin A, B, K, L. M. N, or P.

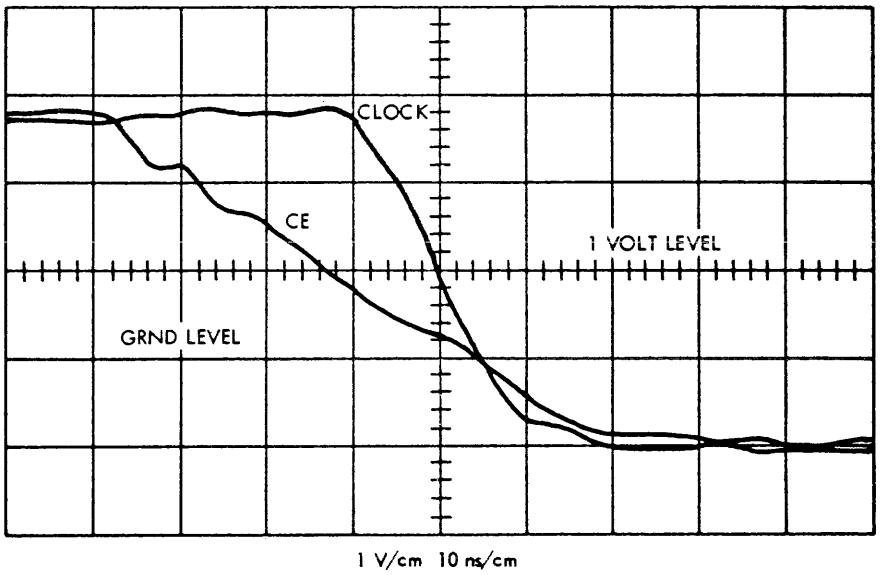


Fig. IV-17. CE AND CLOCK

STEP 4 – CHIP ENABLE TRAILING EDGE

Write Cycle

A. Set up scope as follows:
   Vertical – .1v/cm
   Mode – Alternate
   Horizontal – .5us (500ns)
   External Trigger – SWRITEFO (Card K, Pin ONY)
   Channel 1 – CLK . . KO (Card K, Pin OXX)
   Channel 2 – CENABLKO (Card K, Pin ORY)
   Machine must be performing writes.

B. The following program can be loaded to produce write cycle.

A Reg	Write
000000	7818F0
000010	F00200

   Load FA to 000040

C. In the event that memory is not functioning do the following:
   1. Load M register to 007818
   2. Install a jumper on the backplane from Pin OBX on card D to +4.75. (Pin OAX). This holds the micro in M Register.
   3. Pressing Run should loop the machine in a write cycle.
   4. If Mfetch parity is causing machine to halt install a jumper from the backplane from 1BX on Card H to +4.75 (Pin OAX). This inhibits the parity halt.

D. Obtain wave form shown in Figure IV-18. Disable channel 1 preamp by placing mode switch (Grnd, AC, DC) to ground.

E. Wide pulse in Figure IV-18 is CE during write cycle. Center trailing edge of this pulse on scope screen. Enable channel 4 preamp (switch to DC). Turn on X10 magnifier by manipulating the horizontal control; position the trailing edge of CE and the trailing edge of clock as shown in Figure IV-19.

F. Trailing edge of CE (write) to trailing edge of clock should measure 260 $\pm$ 15 ns. If this adjustment is wrong it will be necessary to move the tap on delay line J4. The wire going to K5D is the controlling wire. This wire should be moved to the needed delay.

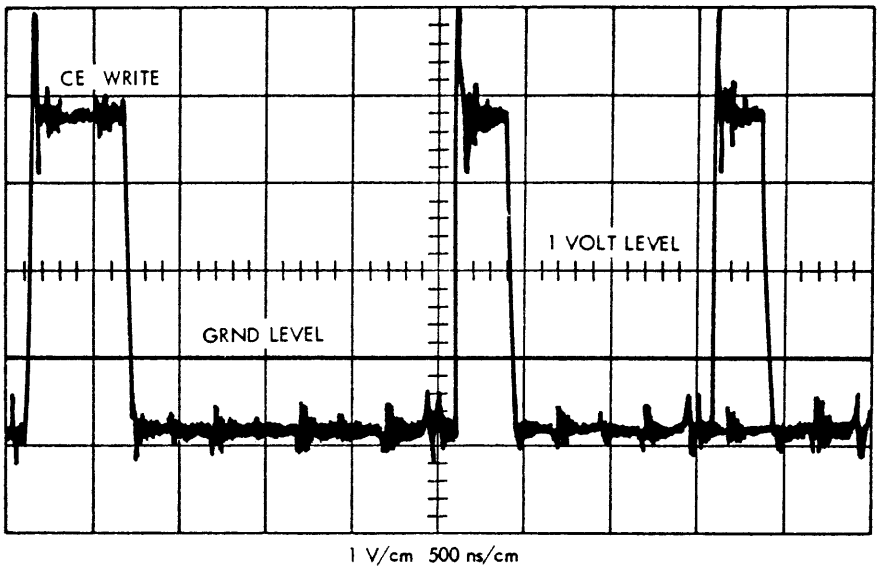


Fig. IV-18. CE TRAILING EDGE (WRITE)

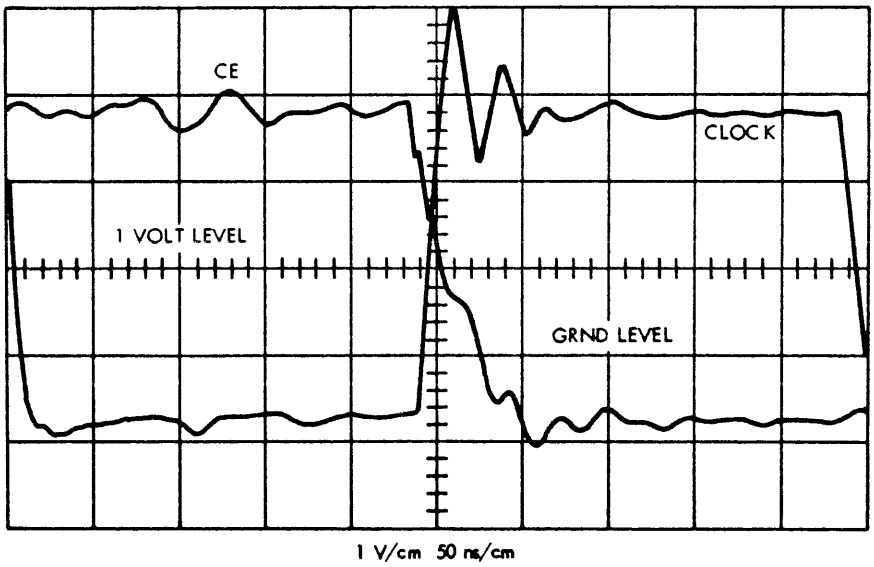


Fig. IV-19. CE (WRITE) AND CLOCK

STEP 5 – READ WRITE (RW) TRAILING EDGE

A. Set up scope as follows:

Vertical – .1v/cm
Mode – Alternate
Horizontal – .5us (500ns)
External trigger – SWRITEFO (Card K, Pin ORY)
Channel 1 – CLK . . KO (Card K, Pin OXX)
Channel 2 – RD/WDKO (Card K, Pin 1NY)

Machine must be performing writes Refer to Step 4 for guidance in setting of machine.

B. Obtain wave form shown in Figure IV-20.
C. Center RW on Screen with horizontal control. Turn on X10 magnifier (50 ns/cm). Obtain wave from shown in Figure IV-21.
D. RW trailing edge should be 310 ± 10ns to the trailing edge of the clock. Delay line J4 controls the trailing edge of RW. Jumper chip K4 is used to change delay times. Pin S is the output of the jumper chip and will be wired to pins H, J, K, L, or M.
E. Leave scope set for Step 6.

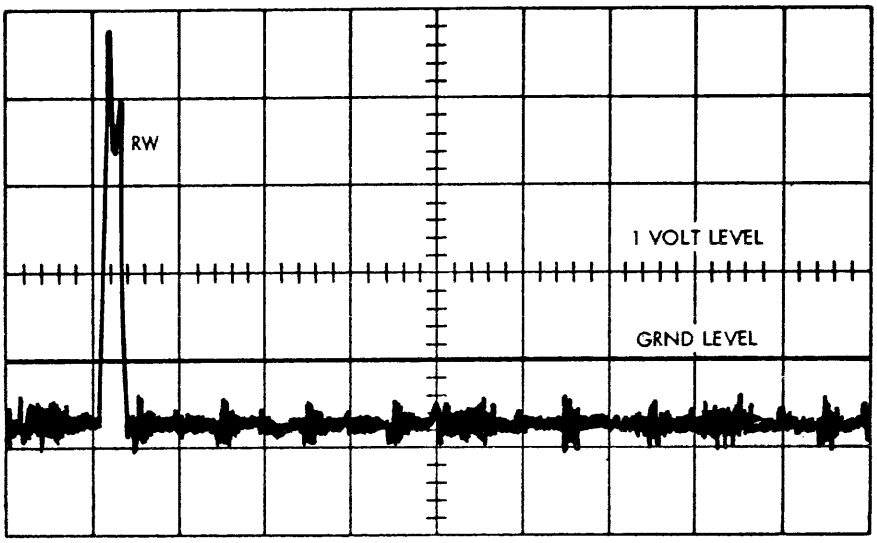


Fig. IV-20. RW TRAILING EDGE

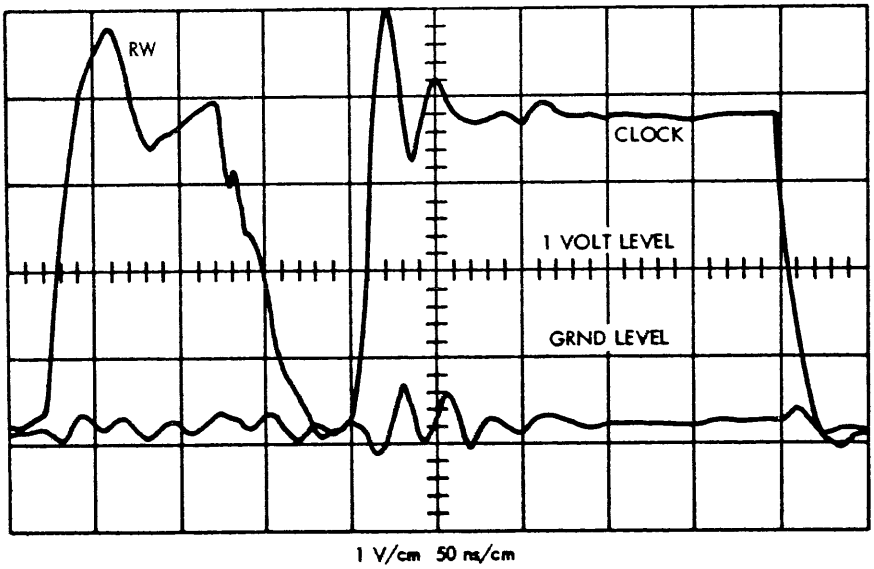


Fig. IV-21. RW AND CLOCK

STEP 6 – READ WRITE (RW) LEADING EDGE

A. Set up scope as follows:
Vertical – .1v/cm
Horizontal – .2us /cm (200ns)
External Trigger – SWRITEFO (Card K, Pin ONY)
Channel 1 – CLK . . KO (Card K, Pin OXX)
Channel 2 – RD/WDKO (Card K, Pin 1NY)
Machine must be performing write. Refer to Step 4 for guidance in setting up machine.

Disable Channel 1, preamp be placing mode Su (AC, DC, Grnd) to ground.

B. Obtain wave form shown in Figure IV-22.

C. Center RW on screen with horizontal control. Turn on X10 magnifier. Obtain wave forms as shown in Figure IV-23.

D. Pulse width of RW should measure 120 ns. If not, the leading edge will be moved to obtain it. Delay line K3 controls the leading edge. Jumper chip K4 is used to change delay times. Pin R is the leading edge output of the jumper chip and will be wired to Pin A, B, C, P, or N.

E. Enable Scope channel 1. GO TO 0.5 us time base and use the X10 magnifier. Obtain the following wave form. Check that both the pulse width and the trailing edge of RW are in SPEC. Refer to Fig.IV-24.

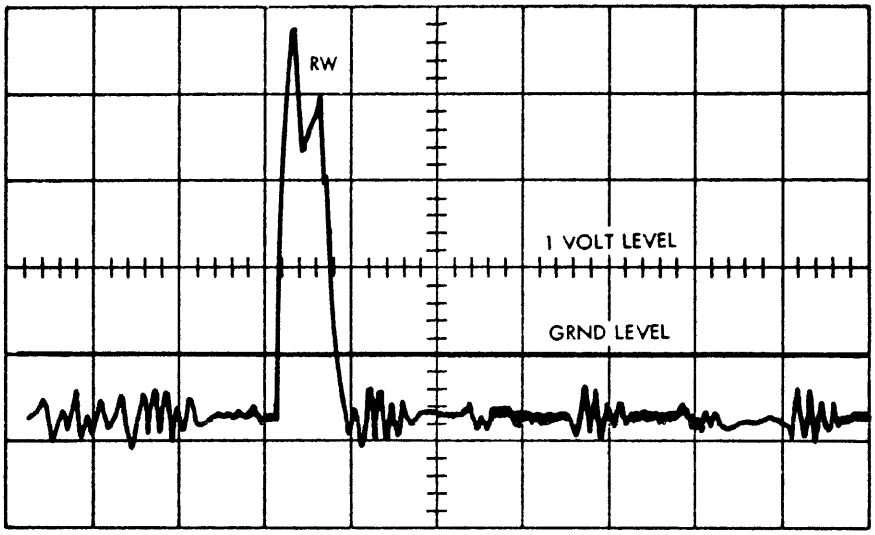


Fig. IV-22. RW

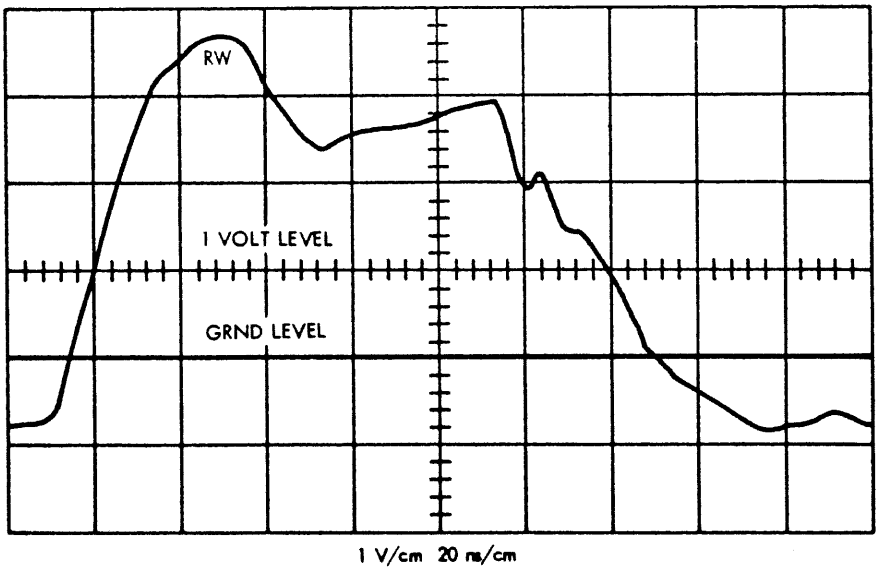


Fig. IV-23. RW PULSE WIDTH

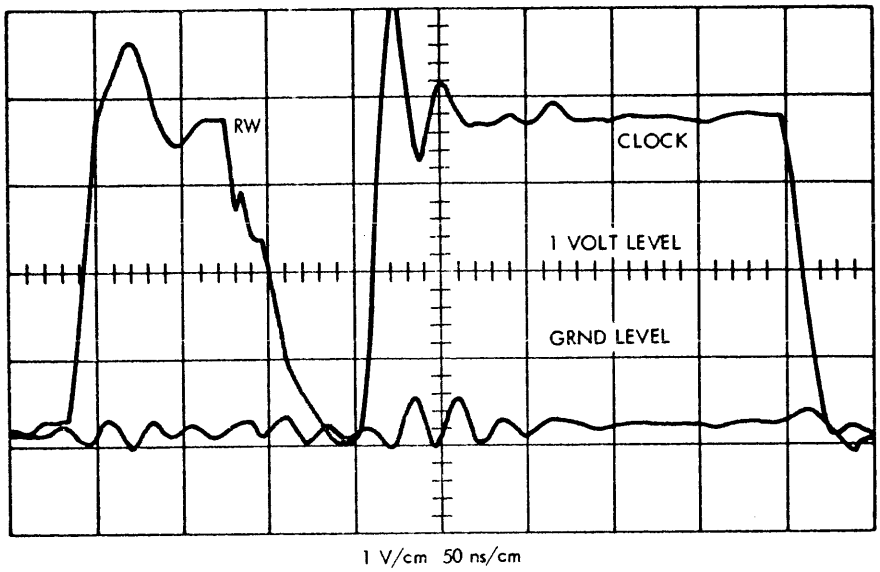


Fig. IV-24. RW AND CLOCK

STEP 7 – GLITCH TRAILING EDGE

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Alternate
Horizontal – .1us (100ns) cm
External trigger – SWRITEFO (Card K, Pin ONY)
Channel 1 – CLK4 . . KO (Card K, Pin OXX)
Channel 2 – GRF . . . HO (Card H, Pin OQY)
Machine is cycled in write state
For write information refer to Step 4. Glitch appears on the Granted Refresh Line.

B. Obtain wave form shown in Figure IV-25. Disable Channel 1 preamp by switching mode switch (DC, AC, Gnd) to ground.

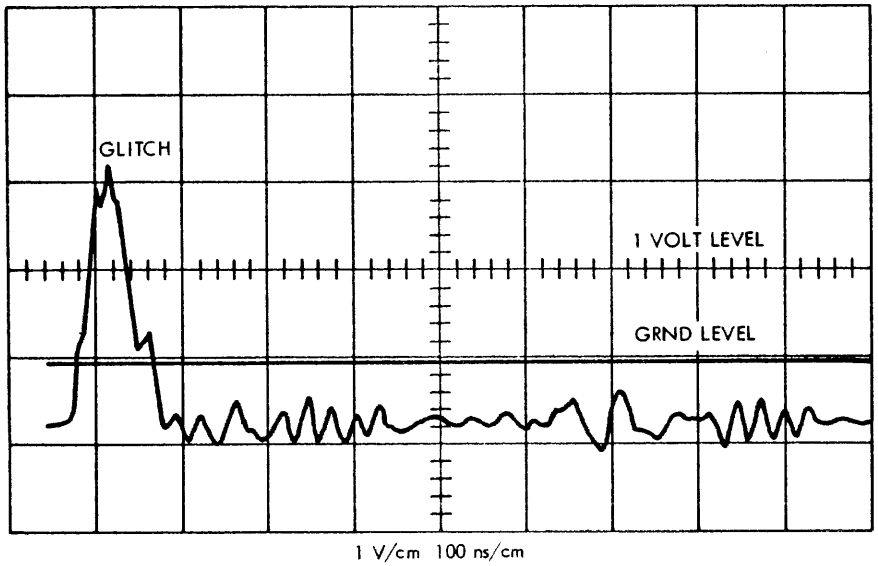


Fig. IV-25. GLITCH

C. There is no adjustment for the leading edge of glitch. The trailing edge is adjusted to vary the pulse width. Turn on X10 magnifier (10 ns/cm). By manipulating the horizontal control position obtain wave form as shown in Figure IV-26. Enable Channel 1.

D. The glitch adjustment is not critical. In general the narrowest pulse reaching 1.5 v of amplitude (measured at 1 v level) should be used. The pulse should be narrower than 45 ns. In practice pin F of delay line J3 is normally wires to GOR, if an adjustment is needed. This tap can be moved to either pin G or H of the delay line J3.

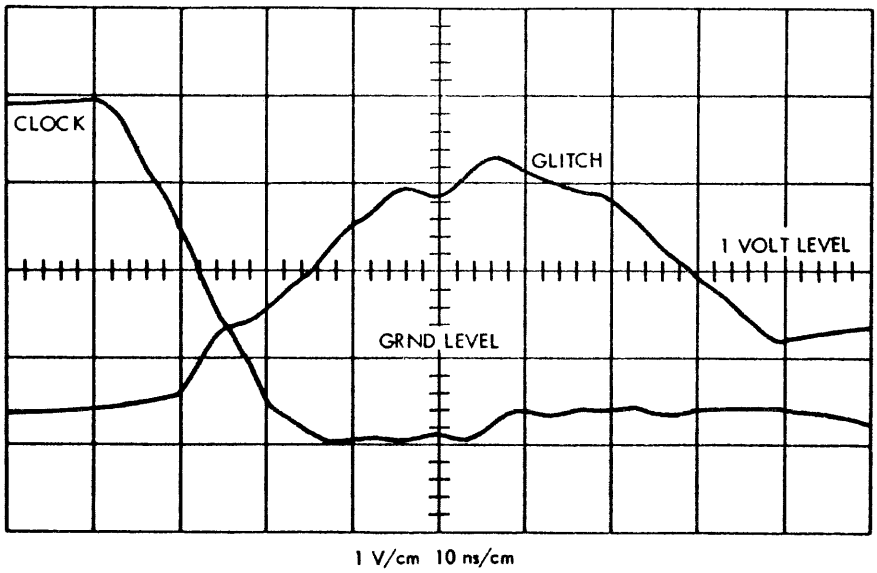


Fig. IV-26. GLITCH AND CLOCK

ADJUSTMENTS K1 Adapter Card (4MHz)
Reference: (Figure IV-43 and Five IV-44)

Procedure

Measurements should be made using a CALIBRATED Tektronix 453A or equivalent oscilloscope with EQUAL length x 10 probes. Probes must be grounded at processor backplane. Check probes for proper calibration. All measurements will be made at the 1 volt level. Adjustments should be made in sequence listed. Refer to Figure IV-43.

STEP 1 – CHIP ENABLE (CE) LEADING EDGE

A. Set up scope as follows:
Vertical – .1v/cm (x10 probe = 1 volt)
Mode – Alternate
Horizontal – .1us (100ns)/cm
External trigger – MSTARTFO (CARD K, Pin 1YY)
Channel 1 – CLK4 . . KO (Card K, Pin OXX)
Channel 2 – CENABLKO (Card K, Pin ORY)
Machine is in idle state.

B. Obtain wave form shown in Figure IV-27.

C. Center CE leading edge with horizontal control. Turn on the X10 magnifier. By adjusting the horizontal control, set the leading edge of CE and the trailing edge of the last clock as shown in Figure IV-28. Time base is set to 10 ns/cm (.1 us x 10).

D. CE Leading Edge Coarse Adjustment
If the time between trailing edge of clock and the leading edge of CE differs more than 10ns from the specified 40ns, adjust the 100 ns delay line (K6). (Wire connecting delay line K6 to J5B.) See Figure IV-28.

E. CE Leading Edge Fine Adjustment
Fine adjustment is now obtained by the tap on the 50ns delay line J6. Adjust to 40 $\pm$ 5ns. (Wire connecting delay line J6 to J9P.) See Figure IV-28.

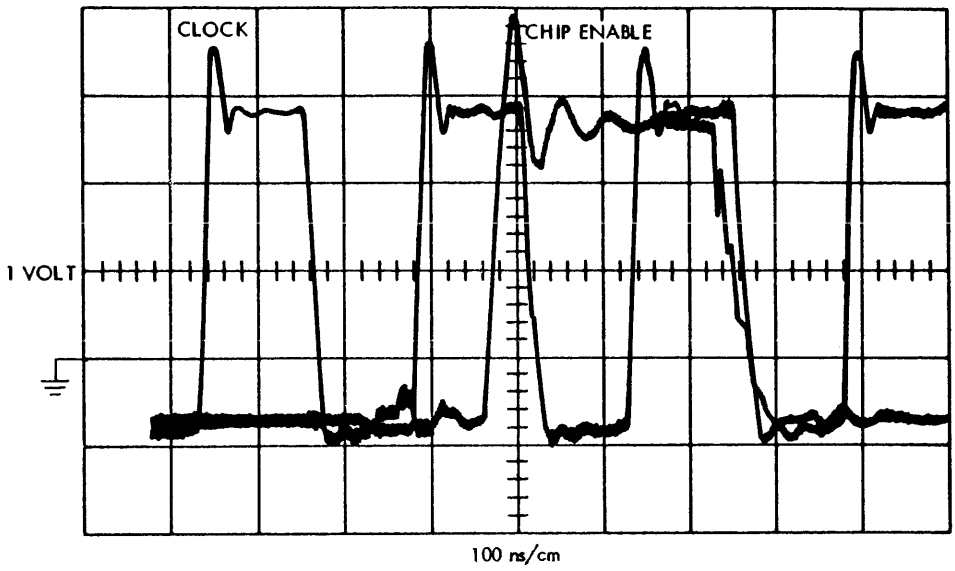


Fig. IV-27. CE LEADING EDGE AND CLOCK 100 ns/cm

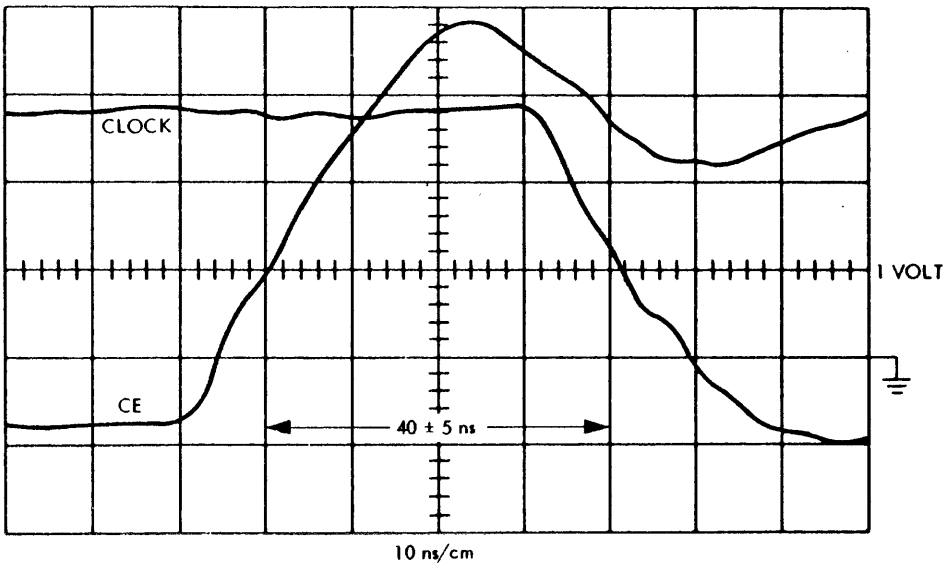


Fig. IV-28. CE LEADING EDGE AND CLOCK 10 ns/cm

STEP 2 – PRECHARGE (PC) LEADING EDGE

A. Set up scope as follows:
   Vertical – .1v/cm
   Mode – Alternate
   Horizontal – .1us (100ns)/cm
   External trigger – MSTARTFO (Card K, Pin 1YY)
   Channel 1 – Precharge (Card K, Pin OQY)
   Channel 2 – CLK4 . . KO (Card K, Pin OXX)
   Machine is in idle state

B. Obtain wave form shown in Figure IV-29.

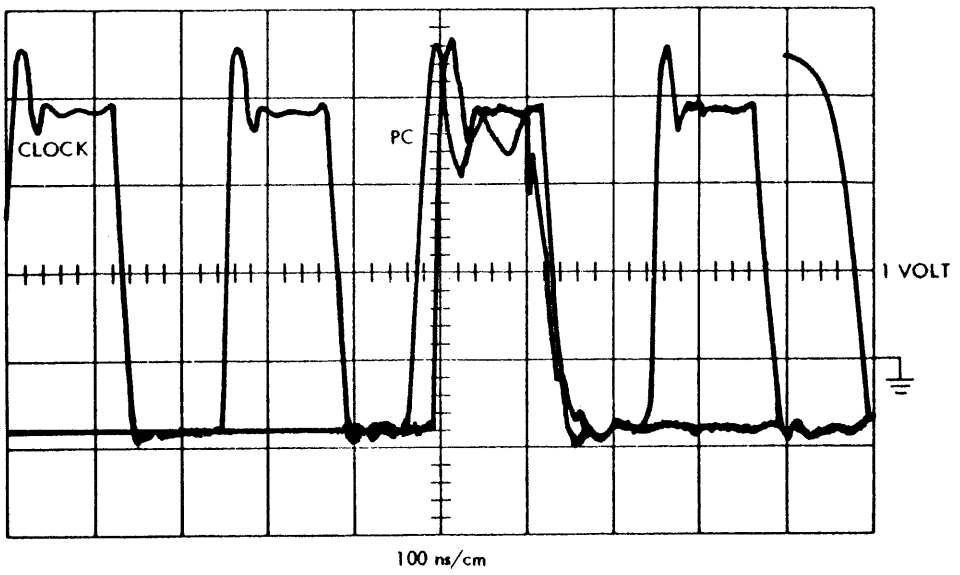


Fig. IV-29. PC LEADING EDGE 100 ns/cm

C. Change time base to .2us/cm. Turn on the X10 magnifier. Manipulate horizontal control to obatin the wave form shown in Figure IV-30. Time base is now set to 20 ns/cm.

D. To adjust the leading edge of precharge (PC) to the specified 155 + 7ns from the trailing edge of clock, move the tap on the 100 ns delay line J4. NOTE: There are two wires on this pin. Both wires are to be moved to the same pin. (Wire connecting delay line J4 to K9P and FOP.) See Figure IV-30.

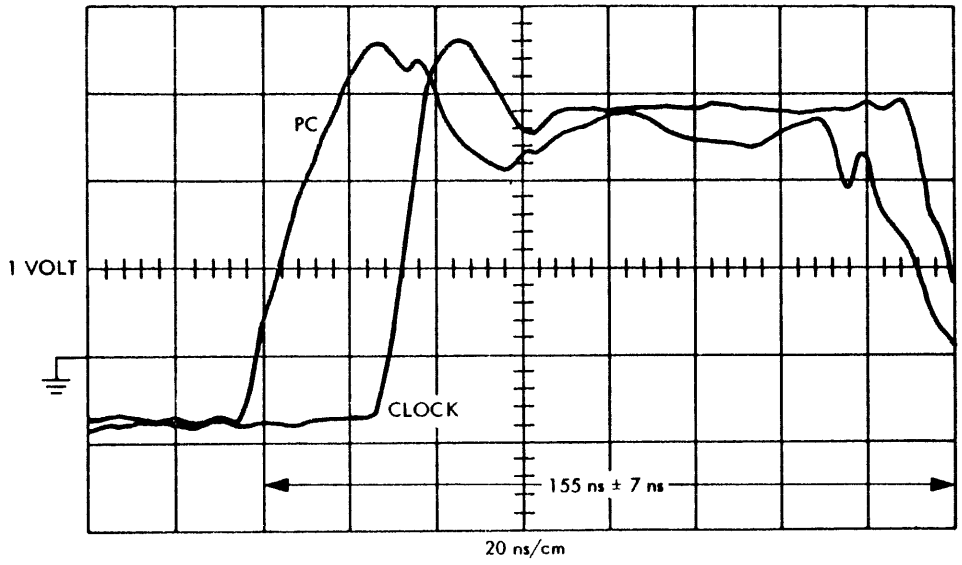


Fig. IV-30. PC LEADING EDGE 20 ns/cm

STEP 3 – PRECHARGE (PC) TRAILING EDGE

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Alternate
Horizontal – .1us (100ns)/cm

Ext. Trigger – MSTARTFO (Card K, Pin 1YY)
Channel 1 – Precharge (Card K, Pin OQY)
Channel 2 – CENABLKO (Card K, Pin ORY)
Machine is in idle state.

B. Obtain wave form shown in Figure IV-31.

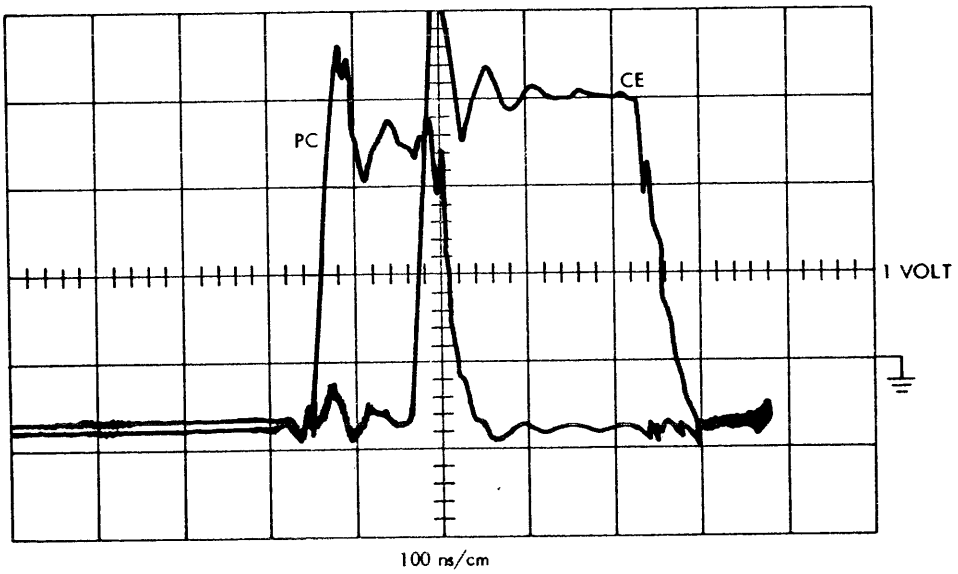


Fig. IV-31. PC LEADING EDGE 100 ns/cm

C. Turn on X10 magnifier. Manipulate horizontal control to obtain the wave form shown in Figure IV-32. Time base is now set to 10 ns/cm.

D. To adjust the trailing edge of precharge (PC) to the specified 34 ± 4 ns from the leading edge of chip enable, move the tap on the 50 ns delay line J6. (Wire from delay line J6 to K7A.) See Figure IV-32.

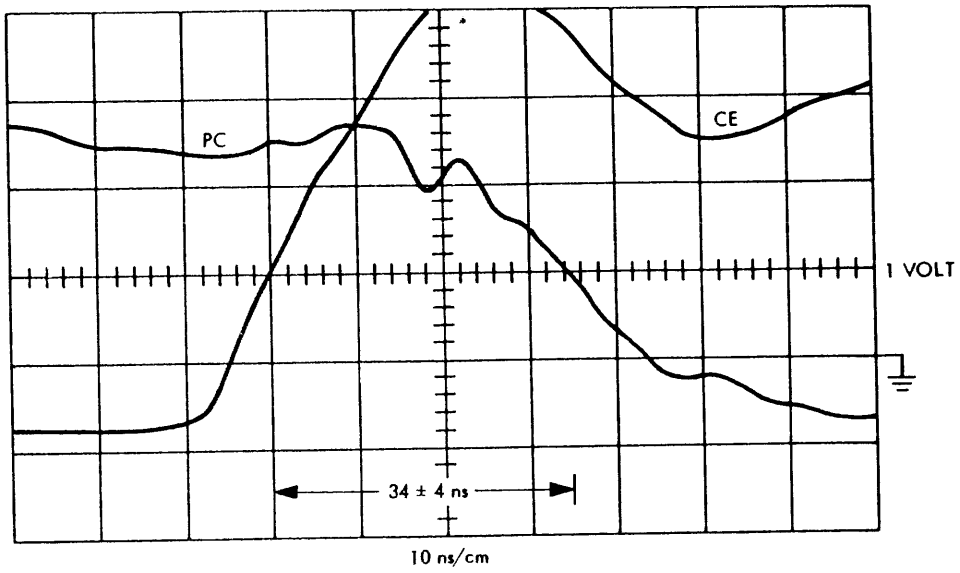


Fig. IV-32. PC AND CE 10ns/cm

STEP 4 – CHIP ENABLE TRAILING EDGE

Read Cycle

A. Set up scope as follows:
   Vertical – .1v/cm
   Mode – Alternate
   Horizontal – .1us (100ns)
   External Trigger – MSTARTFO (Card K, Pin 1YY)
   Channel 1 – CLK4.KO (Card K, Pin OXX)
   Channel 2 – CENABLKO (Card K, Pin ORY)
   Machine is in idle state.

B. Obtain wave form shown in Figure IV-33.

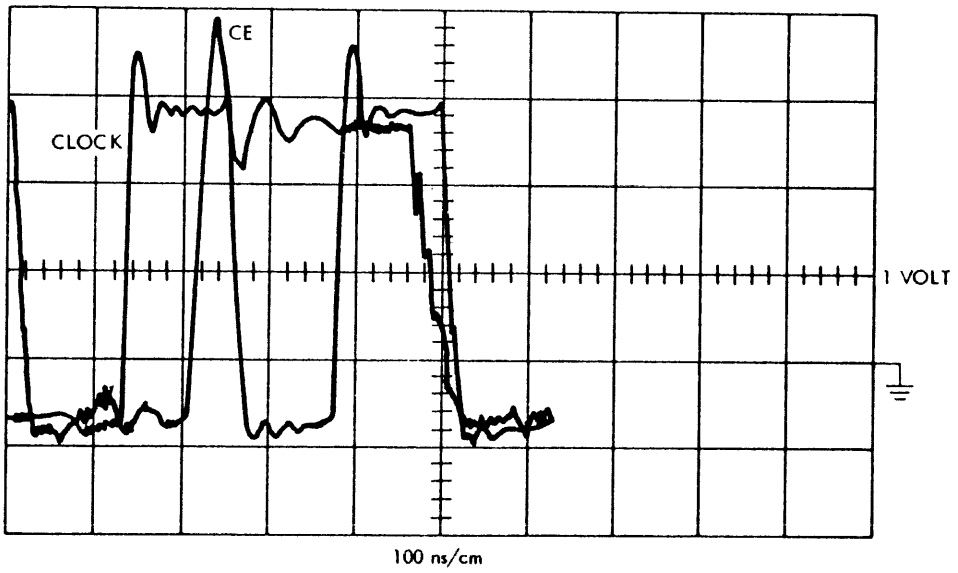


Fig. IV-33. CE TRAILING EDGE 100 ns/cm

C. Manipulate CE trailing edge to the center of screen with the horizontal control. Turn X10 magnifier in. Obtain wave form in Figure IV-34.

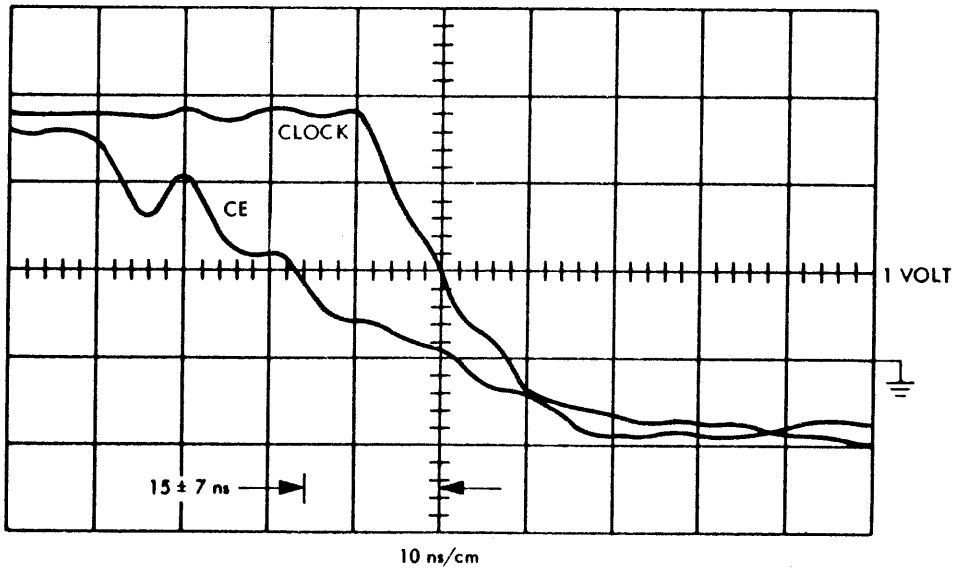


Fig. IV-34. CE TRAILING EDGE 10 ns/cm

D. To adjust chip enable trailing edge (for read cycles) to the specified 15 ± 5 ns from the trailing edge of dock change the tap on the 50 ns delay line J6. (Wire from delay line J6 to J9F.) See Figure IV-34.

STEP 5 – CHIP ENABLE TRAILING EDGE

Write Cycle

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Alternate
Horizontal – .1us (100ns)/cm
External trigger – SWRITEFO (Card K. Pin ONY)
Channel 1 – CLK . . KO (Card K, Pin OXX)
Channel 2 – CENABLKO (Card K, Pin ORY)
Machine must be performing writes.

B. The following program can be loaded to produce write cycle.

A Reg	Write
000000	7818FO
000010	F00200

Load FA to 000040

C. In the event that memory is not functioning, do the following:

1. Load M register to 007818.
2. Install a jumper on the backplane from Pin OBX on Card D to +4.75 (Pin OAX). This hold the micro in M Register.
3. Pressing Run should loop the machine in a write cycle.
4. If Mfetch parity is causing machine to halt, install a jumper on the backplane from IBX on Card H to +4.75 (Pin OAX). This inhibits the parity halt.

D. Obtain wave form shown in Figure IV-35.

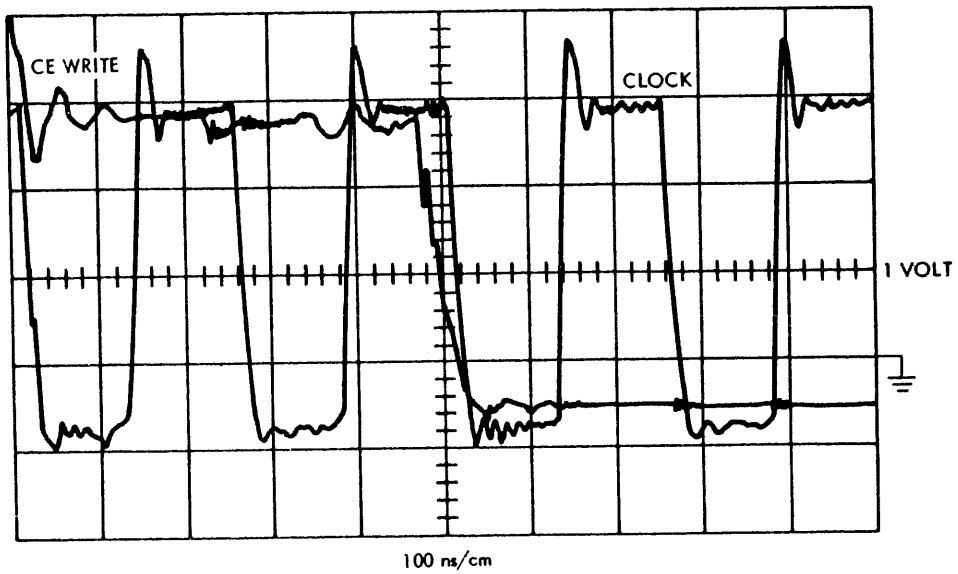


Fig. IV-35. CE TRAILING EDGE (WRITE) 100 ns/cm

E. Wide pulse in Figure IV-35 is CE during write cycle. Center tailing edge of this pulse on scope screen. Turn on X10 magnifier. By manipulating the horizontal control; position the trailing edge of CE and the trailing edge of clock as shown in Figure IV-36.

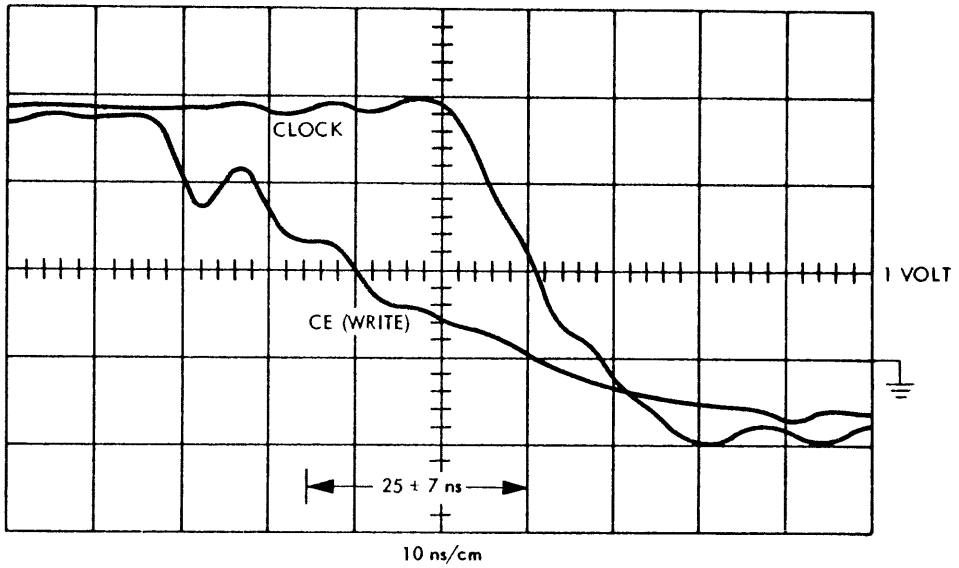


Figure IV-36. CE TRAILING EDGE (WRITE) 10 ns/cm

F. To adjust chip enable trailing edge (for Write cycles) to the specified 25 ± 7 ns from the trailing edges of clock, change the tap on the 100 ns delay line K8. (Wire from the delay line K8 to K9F.) See Figure IV-36.

STEP 6 – READ WRITE (RW) TRAILING EDGE

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Alternate
Horizontal – .1us (100 ns)
External trigger – SWRITEFO (Card K, Pin ORY)
Channel 1 – CLK . . KO (Card K, Pin OXX)
Changel 2 – RD/WDKO (Card K, Pin 1NY)
Machine must be performing writes. Refer to Step 4 fuidance in setting of machine.

B. Obtain wave forms shown in Figure IV-37.

C. Center RW on Schreen with horizontal control. Turn on X10 magnifier (10 ns/cm). Obtain wave form shown in Figure IV-38.

D. Adjust the trailing edge of RW to the specified 60 ± 7 ns from the trailing edge of clock by changing the tap of the 100 ns delay line K8. (Wire from the delay line K8 to J7P.) See Figure IV-38.

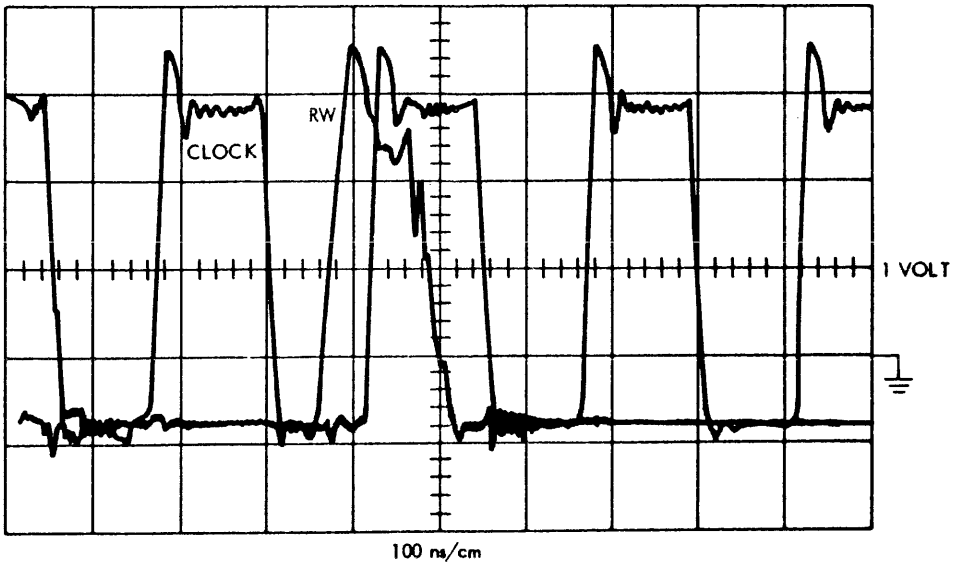


Fig. IV-37. RW TRAILING EDGE 100 ns/cm

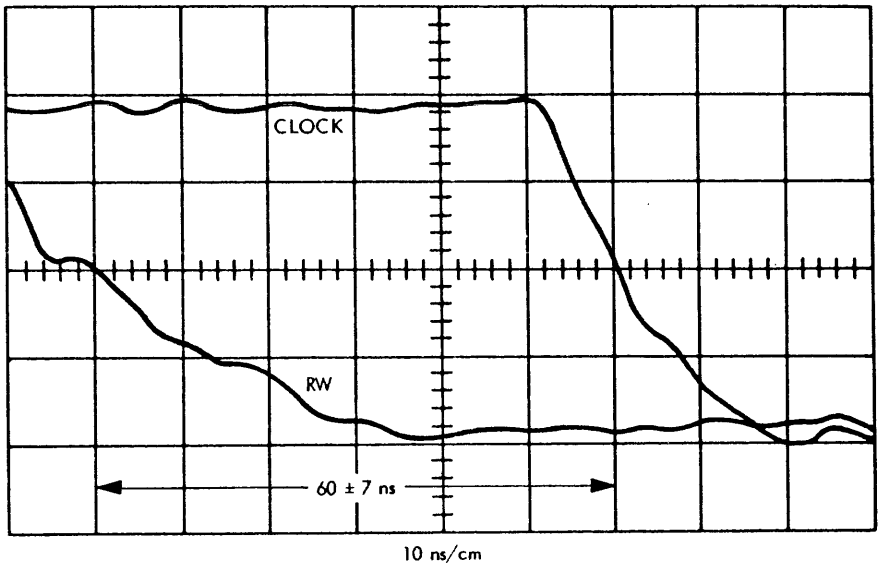


Fig. IV-38. RW TRAILING EDGE 10 ns/cm

STEP 7 – READ WRITE (RW) LEADING EDGE

A. Set up scope as follows:
   Vertical – .1v/cm
   Horizontal – .2us/cm (200 ns)
   External Trigger – SWRITEFO (Card K, Pin ONY)
   Channel 1 – CLK . . KO (Card K, Pin OXX)
   Channel 2 – RD/WDKO (Card K, Pin 2NY)
   Machine must be performing write. Refer to Step 4 for guidance in setting up machine.
   Disable channel 2, preamp by placing mode switch (AC – DC – ground) to ground.

B. Obtain wave form shown in Figure IV-39.

C. Center RW on screen with horizontal control. Turn on X10 magnifier. Obtain wave forms as shown in Figure IV-40.

D. Adjust Read/Write (RW) leading edge to the specified 110 ns ± 7 ns pulse width with the 100 ns delay line K3. (Wire from the delay line K3 to L3R.) See Figure IV-40.

E. After the leading edge adjustment above, go back and recheck the trailing edge adjustment (Step 6). There is a possibility that adjusting the leading edge will slightly affect the point where the trailing edge crosses the 1 volt reference line.

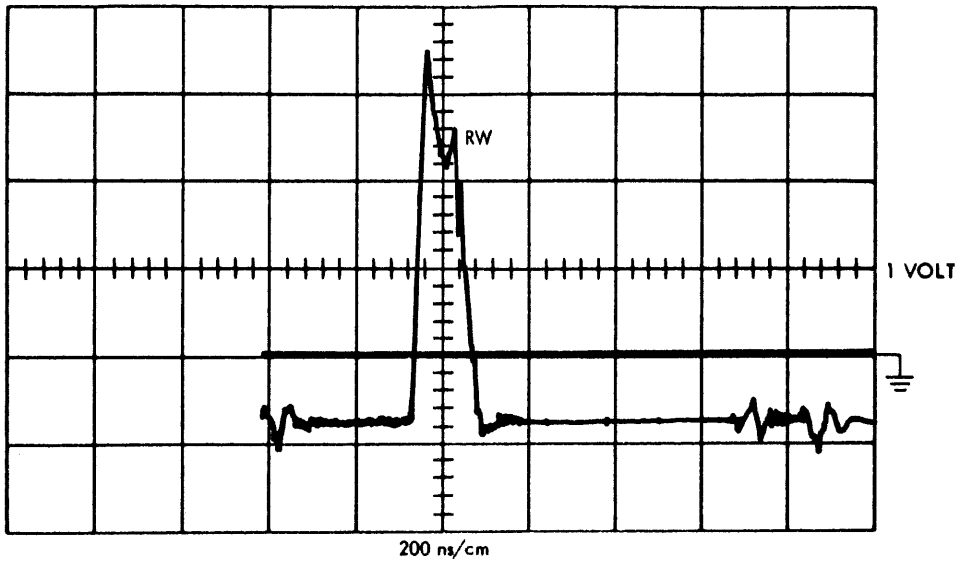


Fig. IV-39. RW 200 ns/cm

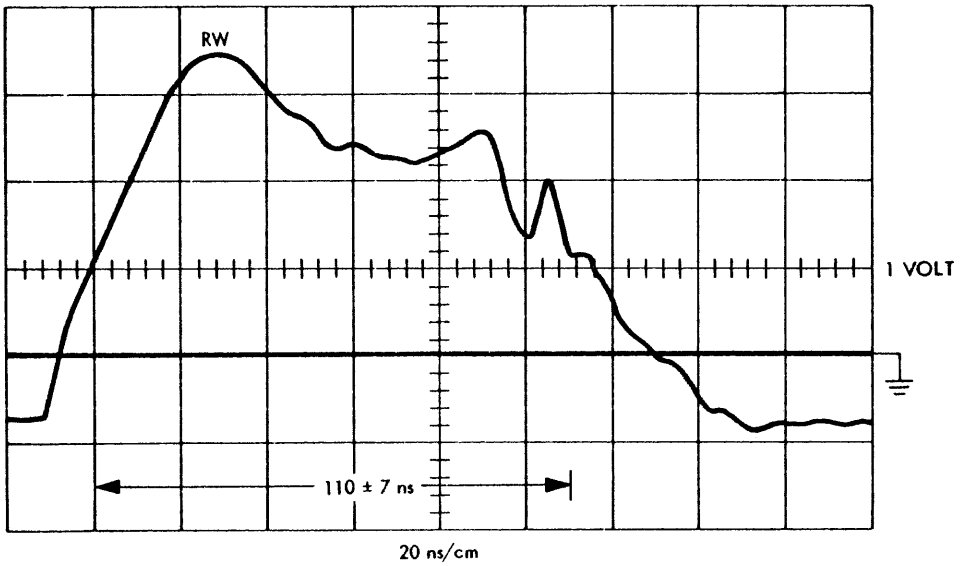


Fig. IV-40. RW PULSE WIDTH 20 ns/cm

STEP 8 – GLITCH TRAILING EDGE

A. Set up scope as follows:
Vertical – .1v/cm
Mode – Channel 1
Horizontal – .1us/cm
External trigger – SWRITEFO (Card K, Pin ONY)
Channel 1 – GRF . . . HO (Card H, Pin OGY)
Machine is cycle in a write cycle.
For write information, refer to Step 5.
Glitch appears on the Granted Refresh Line.

B. Obtain wave form shown in Figure IV-41.

C. Turn on the X10 magnifier by manipulating the horizontal control position wave form as shown in Figure IV-42.

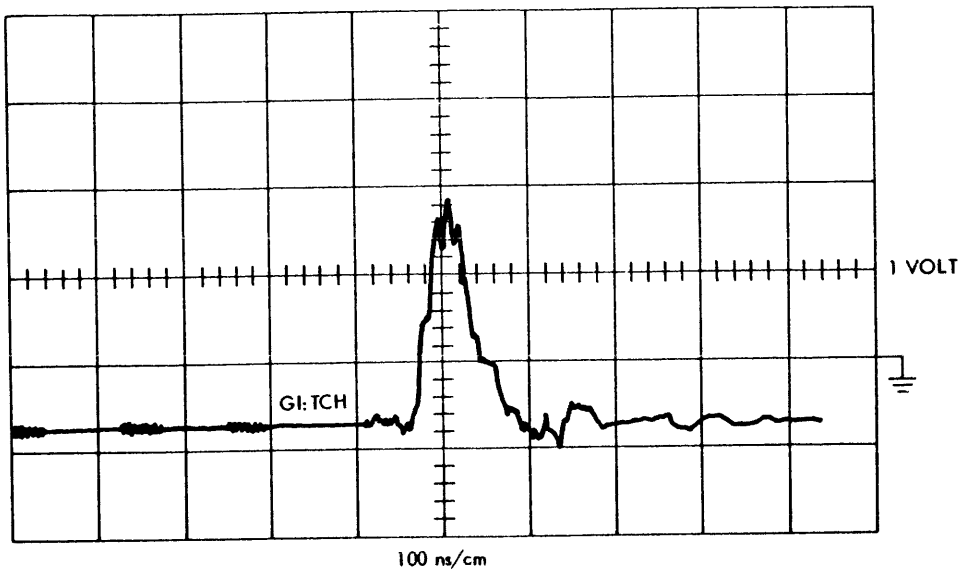


Fig. IV-41. GLITCH 100 ns/cm

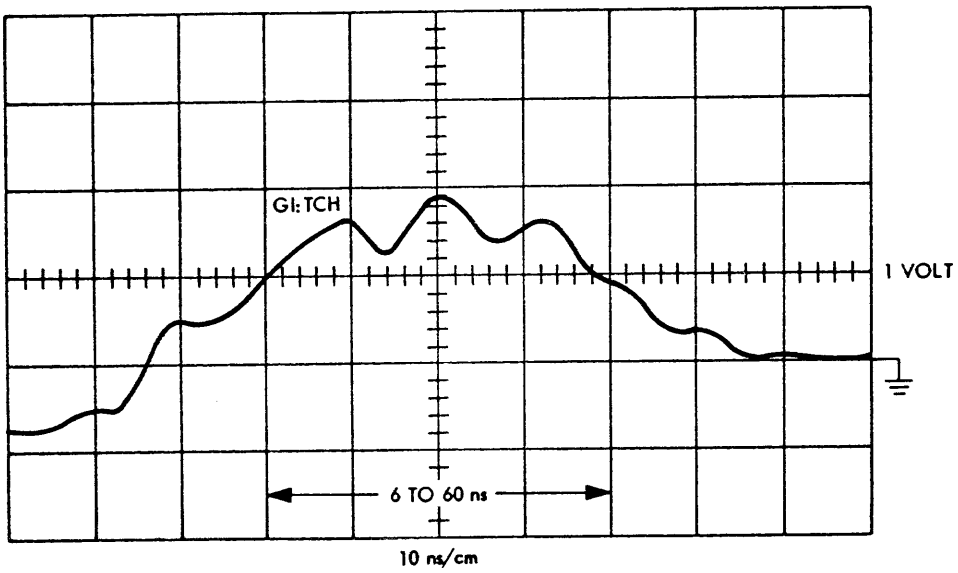


Fig. IV-42. GLITCH 10 ns/cm

D. The glitch adjustment is not critical. In general, the narrowest pulse reaching 1.5v of amplitude (measured at 1v level) should be used. The pulse should be narrower than 60 ns.
The adjustment does not affect the leading edge.
To adjust glitch trailing edge, the wire going to GOR from delay line J4 should be moved. J4 is a 100 ns delay line.

Table IV-1. DELAY LINE TAPS

Pin	DLCN	DL5N	Pin	DLCN	DL5N
G	Input	Input	L	60 ns	30 ns
H	10 ns	5 ns	C	70 ns	35 ns
F	20 ns	10 ns	M	80 ns	40 ns
J	30 ns	15 ns	B	90 ns	45 ns
E	90 ns	20 ns	N	100 ns	50 ns
D,K	50 ns	25 ns			

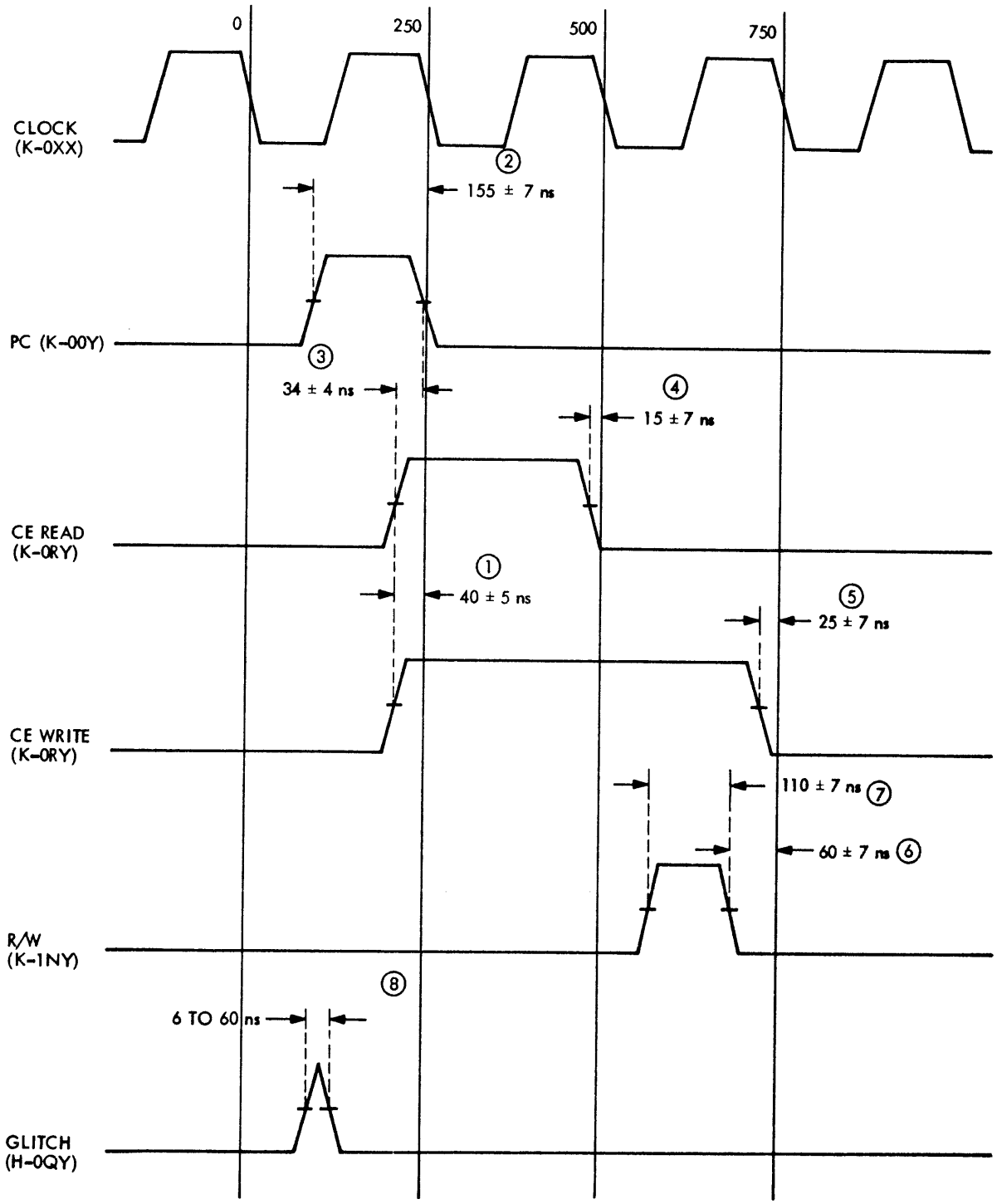


Fig. IV-43. K1 Adapter Memory Timing Wave Forms

For steps 1, 2, 3 and 4 Sync on MSTARTFO
(Card K Pin 1YY)
For steps 5, 6, 7 and 8 Sync on SWRITEFO
(Card K Pin ONY)

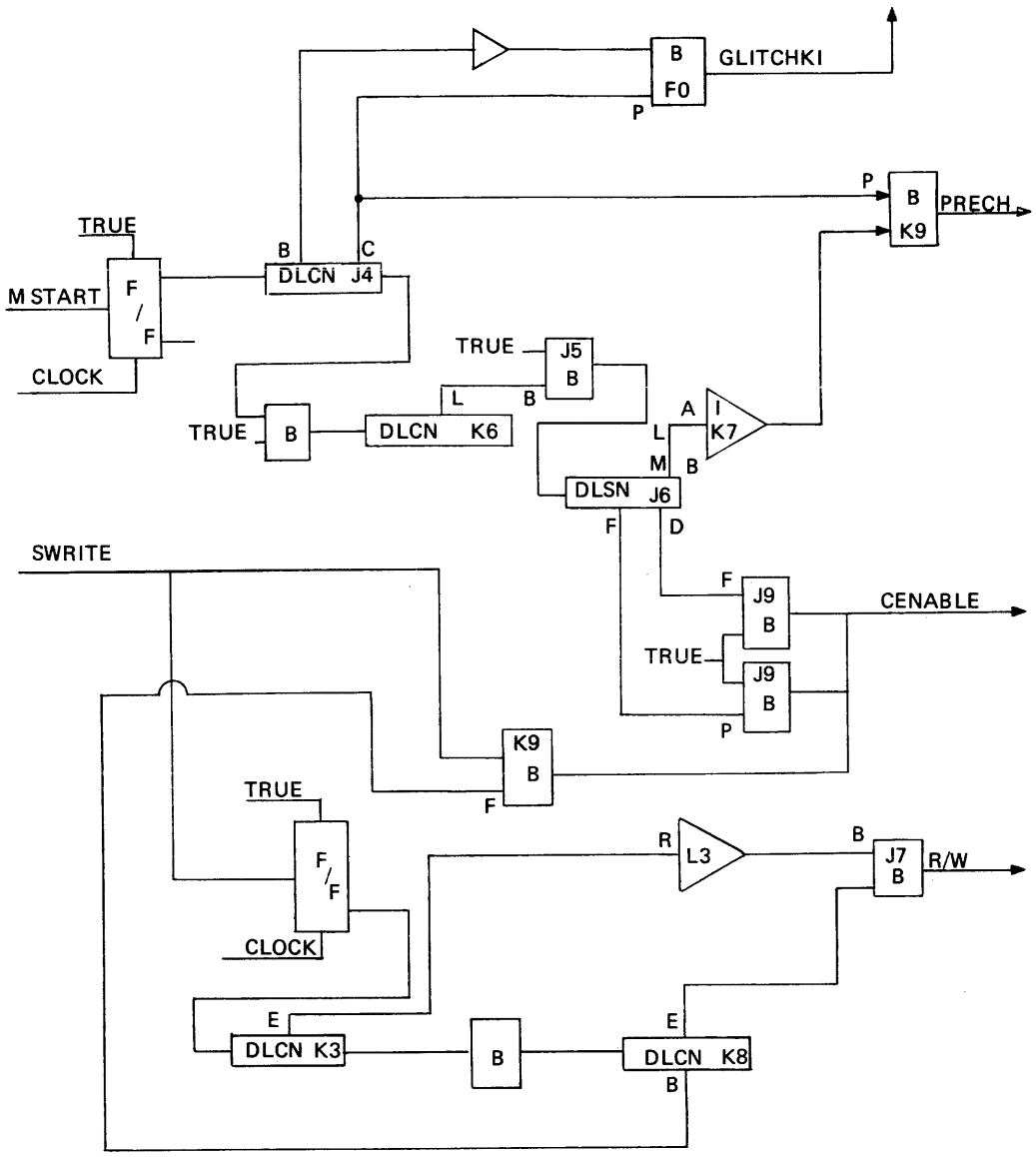


Fig. IV-44. MEMORY TIMING LOGIC K1 CARD

MEMORY POWER OVERVOLTAGE ADJUSTMENTS

The overvoltage adjustment of the memory power supplies should be made prior to any final adjustment for any of the memory voltages. This will insure that any misadjustment over the allowable upper limit will cause the power supply to drop its output power and not damage the memory.

All of the memory voltage adjustments should be made with a digital voltmeter (DVM) and are referenced to logic ground on the backplane of any memory or storage board. Below is the recommended procedure for the overvoltage adjustment for the memory power supplies. See Figure IV-45 for potentiometer location.

A. Turn the power off.
B. Remove all of the storage boards from the S-Memory Processor Chassis
C. Turn the power on.
D. Turn the overvoltage adjustment pots three (3) turns CCW on each power supply.
E. Using a DVM with Logic ground as a reference, adjust the following voltages to the settings listed. See Figure IV-45 for potentiometer location

	Voltage	Location	Card
1	+20V ± .IV	YOA	Any Memory Card
2	*+5V	Y1A	Any Memory Card
3	-6.0 ± .IV	X0D	Any Memory Card
4	Logic Ground	Y1D	Any Memory Card

When adjusting the memory voltage and overvoltage, this +4V power supply will be considered and should be noted that it is riding at a +19V level or on the +19V supply. All measurements for this voltage must be performed utilizing the +19 volt output as reference (Y1A Any Memory Card).

F. Slowly turn the overvoltage adjustment pot CW until the power supply being adjusted drops its output. Do this to all three (3) supplies.

G. Turn the power off.

H. Back the memory supply voltages off of their previous settings by turning their pots 1/4 turn CCW.
At this time, it is necessary to adjust the memory voltages. Refer to the section on Memory Voltage Adjustments.

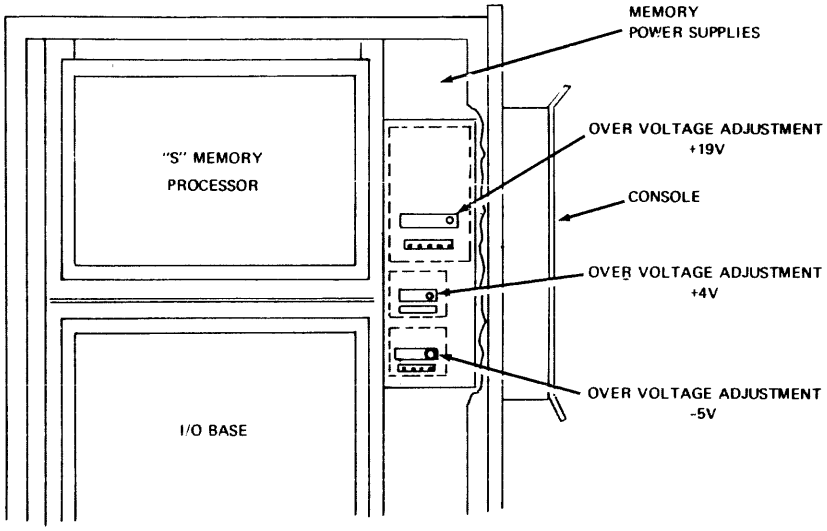


Fig. IV-45. MEMORY OVERVOLTAGE ADJUSTMENTS

MEMORY VOLTAGE ADJUSTMENTS

After the overvoltage adjustments have been made, it is necessary to make the final adjustments on the memory power supplies. It must be made clear that the +19V adjustment must be made first because of the series configuration between the +19V supply and the +4V supply. After these adjustments have been made, the memory storage cards can be installed and a recheck and final adjustment (if any) of the memory voltages should be made.

All voltage measurements and adjustments should be made with a digital voltmeter (DVM) and are referenced to logic ground on the backplane of any memory or storage board. Below is the recommended procedure for the adjustment of the memory power supplies. See Figure IV-46.

A. Make sure that the overvoltage circuits are adjusted correctly. See Overvoltage Adjustment.

B. Remove the memory storage cards from the S-Memory Processor Chassis.

C. Turn on the power and verify AC input is 208-10% to 240+5%.

D. Using a DVM with logic ground as a reference, adjust the following voltages to the settings listed. Be sure to adjust the +19V supply before making the +23V adjustment.

Adjustments

	Voltage	Card	Location
1	+19.0 ± .1V	All Memory Cards	Y0A
2	*+4V ± .1V	All Memory Cards	Y1A
3	-5.0 ± .25V	All Memory Cards	Y0Z
4	Logic Ground	All Memory Cards	Y1D

*All measurements for these voltages must be performed utilizing the +19 volt output as references (Y1A AKY Memory Card)

E. Turn off the power
F. Install storage boards into the S-Memory Processor Chassis.
G. Turn on the power.
H. Recheck voltages, if the voltages are now incorrect check for current limit or problems on the storage boards.

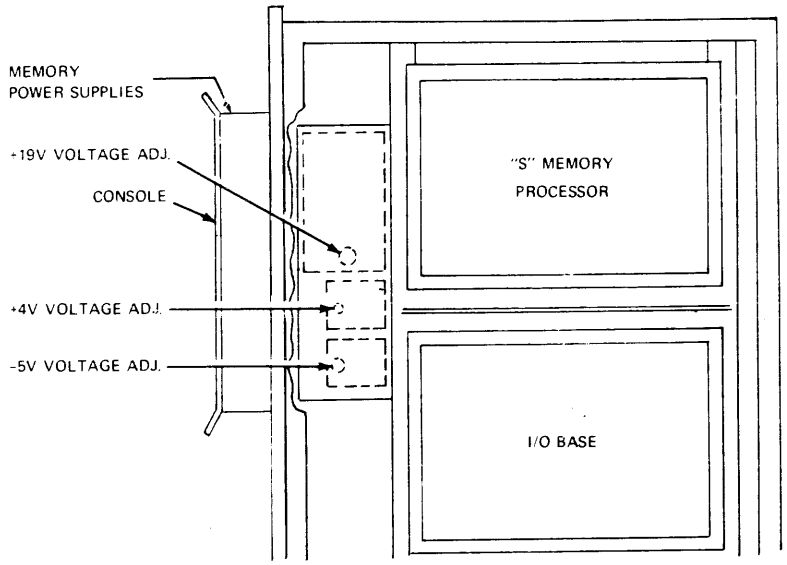


Fig. IV-46. MEMORY VOLTAGE ADJUSTMENTS

+19 VOLT, CURRENT LIMIT CALIBRATION

This adjustment is necessary only at the factory or upon replacement of the +20 volt supply in the field. The supply must be removed from the system, and the cover must be removed from the supply. For this adjustment only, the +S terminal must be bussed to the +V terminal and the -S terminal must be bussed to the -V terminal. When the adjustment is completed, remove the +S to +V and the -S to -V busses.

Connect power to the supply (208 volts AC single phase). Turn the current limit adjustment, R12-500Ω,FCCW. Verify the output voltage is adjusted to 19.00 ± .01 volts. Place a 1.9 ± .01 ohm, 200 watt, resistive load on the power supply or connect an ammeter in series with a variable resistor (200 watt) as a 10 Amp load on the power supply. Adjust the current limit adjustment CW until the voltage just starts to decrease.

ADJUSTMENTS LOGIC POWER SUPPLY

CAUTION

Do not use metal adjusting tools

GENERAL

All Power Supply voltages are set at the factory and should not need adjusting unless a component is damaged and/or replaced. If it becomes necessary to adjust or reset any of the voltages the following procedure should be used for the logic supply.

MEASUREMENT TECHNIQUES

The Power Supply must be disconnected from the data processing system; connections J12A, J12B, JLG and the high current terminals must be disconnected.

All voltages measurements should be made with a digital voltmeter (DVM). However a Triplett 630 or equivalent may be used if a DVM is not available. All necessary wave forms should be checked with a Tektronix 453A oscilloscope or equivalent.

CAUTION: All test equipment must be isolated from power ground. Test equipment chassis must never come in contact with the Power Supply chassis.

Refer to Figure IV-47 for test jack identification and the correct location of the various adjusting potentiometers.

PRE-CALIBRATION PROCEDURE

1. Power down the system.
2. Extend the power supply. For disassembly refer to Section V.
3. Connect a one hundred ampere (100 amp) dummy load between the +4.75 output and ground.
4. Remove all the power supply logic cards.
5. Remove the 40 amp fuse F1.

160 VOLT REGULATOR ADJUSTMENT

1. Insert the 160V Regulator Card into J3.
2. Turn card switch ON.
3. Turn supply breaker ON and depress the power on pushbutton.
4. Insert meter probes into 160V test jacks on front of the supply.
5. Adjust 160 Adj pot, R10, until meter reads 160 ± 5 VDC.
6. Turn card switch OFF.
7. Turn supply breaker OFF.

CONTROL CARD ADJUSTMENT

1. Insert the control card into J4.
2. Turn the supply breaker ON.
3. Insert the meter probes in the proper test jacks.
4. Adjust the corresponding control card potentiometer for the correct setting.

Test Jacks	Pot	Meter Readings
Grd + 24	R2	+22 to + 24 volts
Grd +4.5	R21	+4.75 ± .1 volts
Grd −1.9	R25	−2.00 ± .1 volts
Grd − 15	R11	−15.00 ± .1 volts
Grd + 15		+15.00 ± .1 volts

1 Adjustment Tracking Supplies

Turn supply breaker OFF.

TIMING CARD ADJUSTMENT

1. Insert the Extender Card in J1, then insert the timing card in the extender.

NULL ADJUSTMENT

1. Short Timing Card pins 1W and 0Q together.
2. Connect the meter between chip F2 Pin M Timing Card pin OR.

3. Turn supply breaker ON.
4. Adjust NULL pot R13 until meter indicates a null, 0.000 ± 0.020 volts.
5. Turn the supply breaker OFF.
6. Remove the short between pins 1W and 0Q.

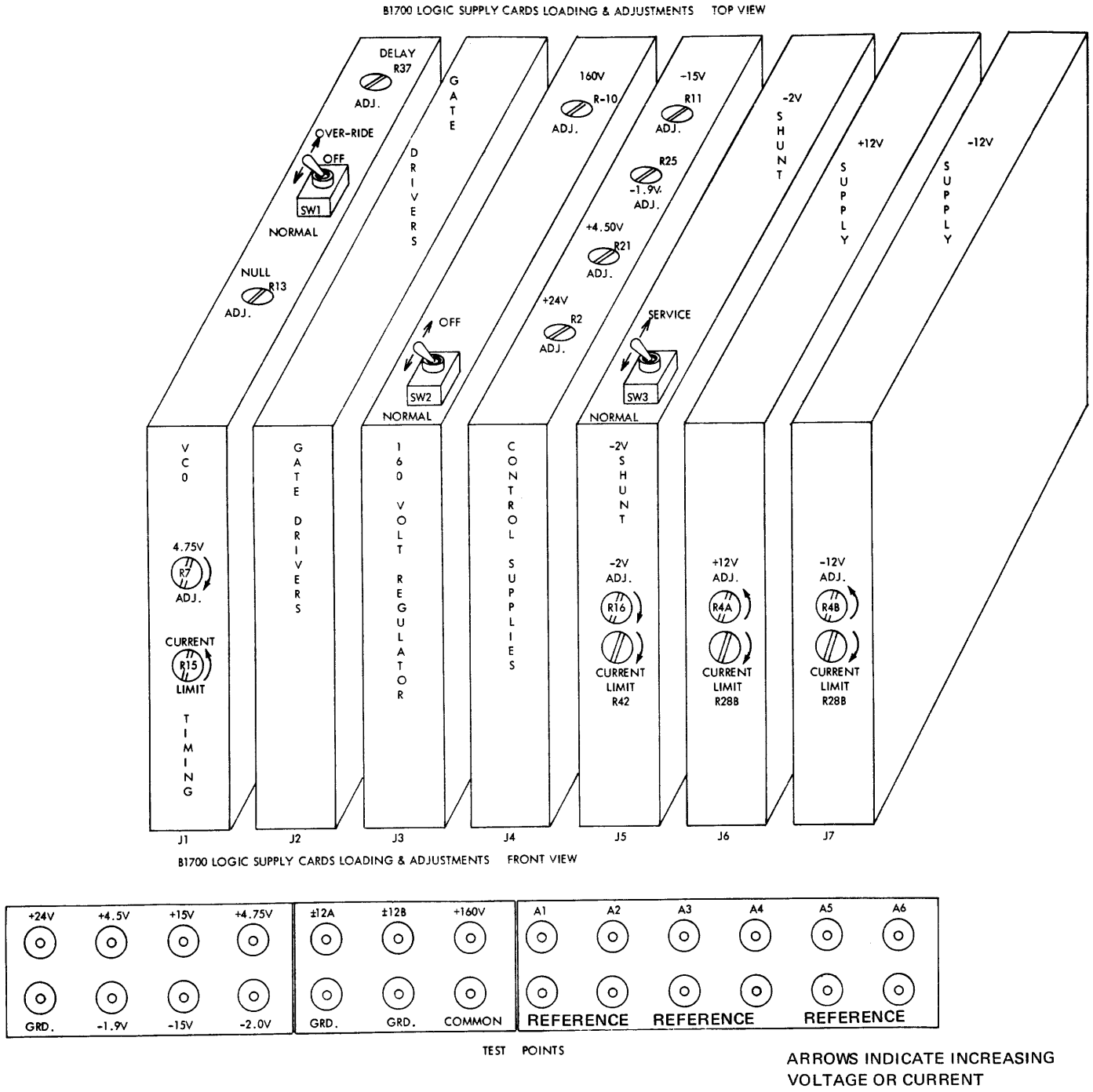


Fig. IV-47.

DELAY ADJUSTMENT

1. Connect the scope from Timing Card ground to Chip C1 Pin H.
2. Turn the Timing Card switch to the Over Ride position.
3. Turn the supply breaker ON.
4. Adjust the Delay pot, R37 for a 40 ± 2 usec False Level.
5. Turn the supply breaker OFF.

GATE DRIVER VERIFICATION

1. Insert the Gate Driver card into J2.
2. Turn the supply breaker ON.
3. Verify at the test points, the following waveforms: A1, A2, A3, A4 shown in Figure IV-48, A5 and A6 shown in Figure IV-49.

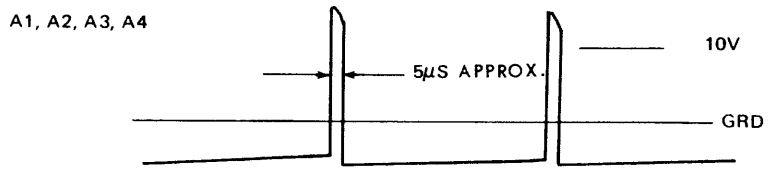


Fig. IV-48

4. Turn the Timing Card switch to OFF.
5. Turn the switch to Normal.
6. Verify no pulses on the scope.
7. Turn the breaker OFF.

–2 VOLT ADJUSTMENT

1. Install the 40 Amp fuse.
2. Turn the 160V Regulator Card switch ON.
3. Insert the –2V Shunt Regulator card into J5.
4. Turn the –2V card switch to Service.
5. Turn the supply breaker ON.
6. Adjust the –2.00V output by adjusting R16.
7. Output test points are available on the front panel.
8. Set the output to –2.00 ± 0.01V.

+4.75 VOLT ADJUSTMENT

1. Adjust the +4.75V output by adjusting R7 on the timing card. Output test points are available on the front panel.
2. Set the output to +4.75 ± 0.01V.
3. Turn the supply breaker OFF.

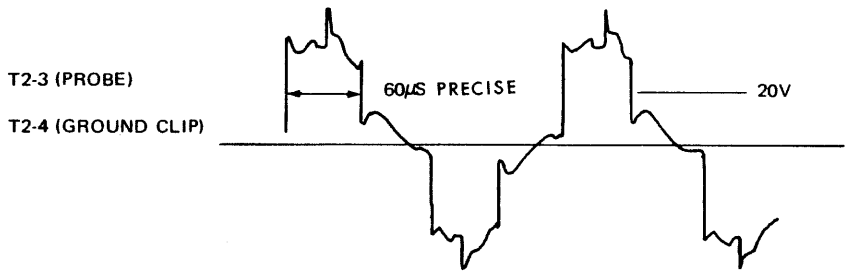


Fig. IV-49.

INVERTER ADJUSTMENT

1. Verify the oscilloscope is isolated from power ground.
2. Connect the scope from transformer T2 Pin 3 (probe) to Pin 4 (ground clip).
3. Turn the supply breaker ON.
4. Adjust the Timing Card Delay pot, R37, to obtain a 60 ± 2 usec pulse width on the scope (this adjustment must be done when the +4.75V to Ground output is loaded with the dummy load, 90 ± 5 Amps.). See Figure IV-23.
5. Turn the supply breaker OFF.

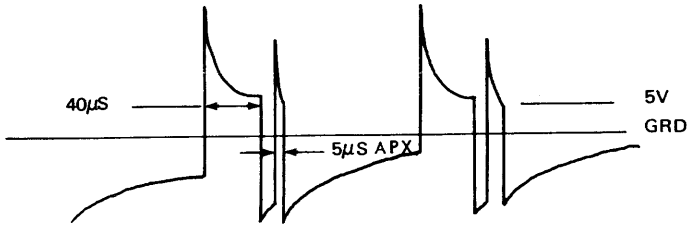


Fig. IV-50.

NULL VERIFICATION

1. Short Timing Card pins 1W and 0Q together.
2. Connect the meter between chip F2 Pin M Card pin OR.
3. Turn the supply breaker ON.
4. Adjust the NULL pot R13-10K until meter indicates a null, 0.000 ± 0.020 volts.
5. Turn the supply breaker OFF.
6. Remove the short between pins 1W and 0Q.
7. Remove the card extender and insert the Timing Card directly into J1.

NORMAL SWITCH SETTINGS

1. Turn the –2V card switch to Normal.
2. Verify the 160V card switch is ON.
3. Verify the Timing Card switch is Normal.

± 12 VOLT ADJUSTMENT

1. Insert the ± 12A Card into J6.
2. Turn the supply breaker ON.
3. Adjust R4 to adjust the 12 volt output. Output test points are available on the front panel.
4. Turn the supply breaker OFF.
5. Insert the ± 12B card. Repeat 2, 3 and 4.

ADJUSTING THE LOGIC SUPPLY IN A B1700

1. Place the supply into a B1700.
2. Connect buss bars, JLG, J12A, and J12B.
3. Turn the supply ON and then turn the system ON.

+4.85V Backplane Adjustment

1. Connect the meter probes (GRD) to the +4.75 volt Buss Bar at the backplane.
2. Adjust the Logic Supply +4.85 V Adj. (R7) to +4.85 ± 0.01.
3. Adjust the Logic Supply +4.85 I Adj. (R15) until the +4.85 begins to current limit (+4.85 VDC reading begins to decrease). Then back-off the current limit adjustment 2 turns.

−2.00V Backplane Adjustment

1. Connect the DVM from (GRD) to the −2 Volt Buss Bar at the backplane.
2. Adjust the Logic Supply −2.00 V Adj. (R16) to −2.00 V Adj. (R16) to −2.00 ± 0.01 VDC.
3. Adjust the Logic Supply −2.00 I Adj. (R42) until the −2.00 begins to current limit (−2.00 VDC reading begins to increase). Then back-off the current limit adjustment 2 turns.

+12.00V Backplane Adjustment

1. Connect the DVM from (GRD) to the bottom of the +12V Buss (furtherest from the backplane).
2. Adjust the Logic Supply ±12A V Adj. to +12.00 ± 0.01 VDC.
3. Adjust the Logic Supply ±12A I Adj. (R28A) until the +12.00 begins to current limit (+12.00 VDC reading begins to decrease). Then back-off the current limit adjustment 2 turns.

−12.00V Backplane Adjustment

1. Connect the DVM from (GRD) to the bottom of the -12V Buss (nearest the backplane).
2. Adjust the Logic Supply +12B V Adj. to −12.00±0.01 VDC.
3. Adjust the Logic Supply ± 12B I Adj. (R28B) until the −12.00 begins to current limit (−12.00 VDC reading begins to decrease). Then back-off the current limit adjustment 2 turns.

ADJUSTMENT COMPLETED.

B 1700

CENTRAL SYSTEM

SECTION

V

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

MAINTENANCE
PROCEDURES

Printed in U. S. America 11-20-72

For Form 1053360

INTRODUCTION

This section contains maintenance and troubleshooting procedures for the B1700 Central System. In general the manual will be separated by the three major areas: Processor, Memory and Power Supplies. The I/O subsystem is contained in separate manuals.

PROCESSOR MAINTENANCE PROCEDURES

The following items will be covered for the processor:

1. Maintenance aids
2. Preventive maintenance
3. Test points
4. Troubleshooting procedures
5. Removal and/or replacement

MAINTENANCE AIDS

Maintenance aids consist of all hardware and software devices that are used to keep the B1700 processor operational. They include the following:

1. Test equipment
2. Test programs
3. Logic diagrams and associated documentation

TEST EQUIPMENT

The test equipment used to properly maintain the B1700 processor is listed below. In addition to the equipment listed, many field engineers may find it helpful to construct and use the single clock generator as shown in Figure V-1.

1. Tektronix 453A oscilloscope
2. Triplett 630 multimeter or equivalent
3. Burroughs digital voltmeter (DVM)
4. B1700 Card Tester
5. Card Extender

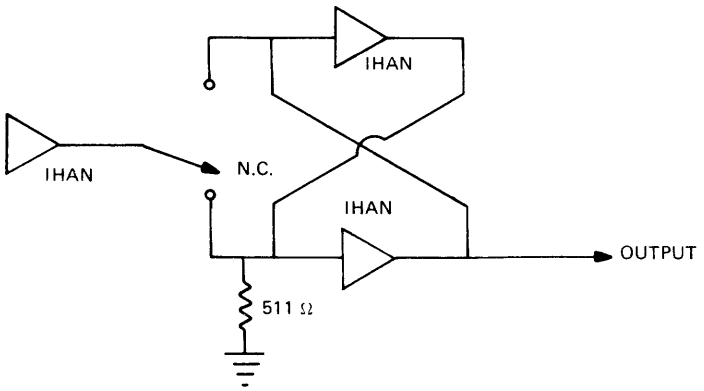


Fig. V-1 SINGLE CLOCK PULSE SWITCH

TEST PROGRAMS

The test programs exercise the processor with sequences of micro operators. The results of these sequences are compared against proper responses. Since some test programs use the console display lamps and other programs may use the SPO, a correct result or incorrect result is not readily apparent to the field engineer. For this reason, the field engineer should use the appropriate procedure that accompanies every test program.

A list of the test programs that are used to properly maintain the B1700 processor are listed below. Refer to the troubleshooting section for further information about using test programs.

1. Maintenance Test Routines (MTR) – These tests are loaded and executed directly from the cassette tape.
2. Dynamic Tests – These tests are loaded from the cassette tape into the S-Memory. They are then executed from S-Memory.

LOGIC DIAGRAMS

All logic diagrams and associated documentation should accurately reflect the system of which they are part. These documents should be maintained because they are an integral part of any maintenance concept. The following list indicates the documentation that is used to maintain the B1700 processor.

1. Card schematics (logic diagrams)
2. Element Representation Book
3. Name ordered circuit list

B1700 LOGIC CARDS

Logic for the B1700 is located on pluggable cards that are 14½" long by 12½" high. There is etching on both sides of the cards. See Figures V-4 and V-5.

The card sides are designated either even or odd with the components being mounted on the even (0) side. The soldered side is referred to as the odd (1) side. The cards have 50 backplane connections on each side. These are divided into sections X and Y, with X being the upper and Y being lower. The contacts of the cards are lettered A through Z, with the letter O being omitted. Therefore, it is possible to have 100 connections to the backplane wiring. See Figure V-2.

A card may also contain from 1 to 4 frontplane cable connectors. Each cable connector consists of 25 pins, and are labeled by the following method:

1. $X
2. #X
3. $Y
4. #Y

The contacts for each connector are labeled A to Z with the letter O being omitted. See Figure V-3.

Each card can contain up to 120 chips. The card consists of 12 rows with 10 columns in each row. Rows are oriented from top to bottom and are identified alphabetically by the letters A through L. Columns are identified numerically. They are numbered 0 through 9 left to right, with 9 being nearest to the backplane connector. See Figure V-4.

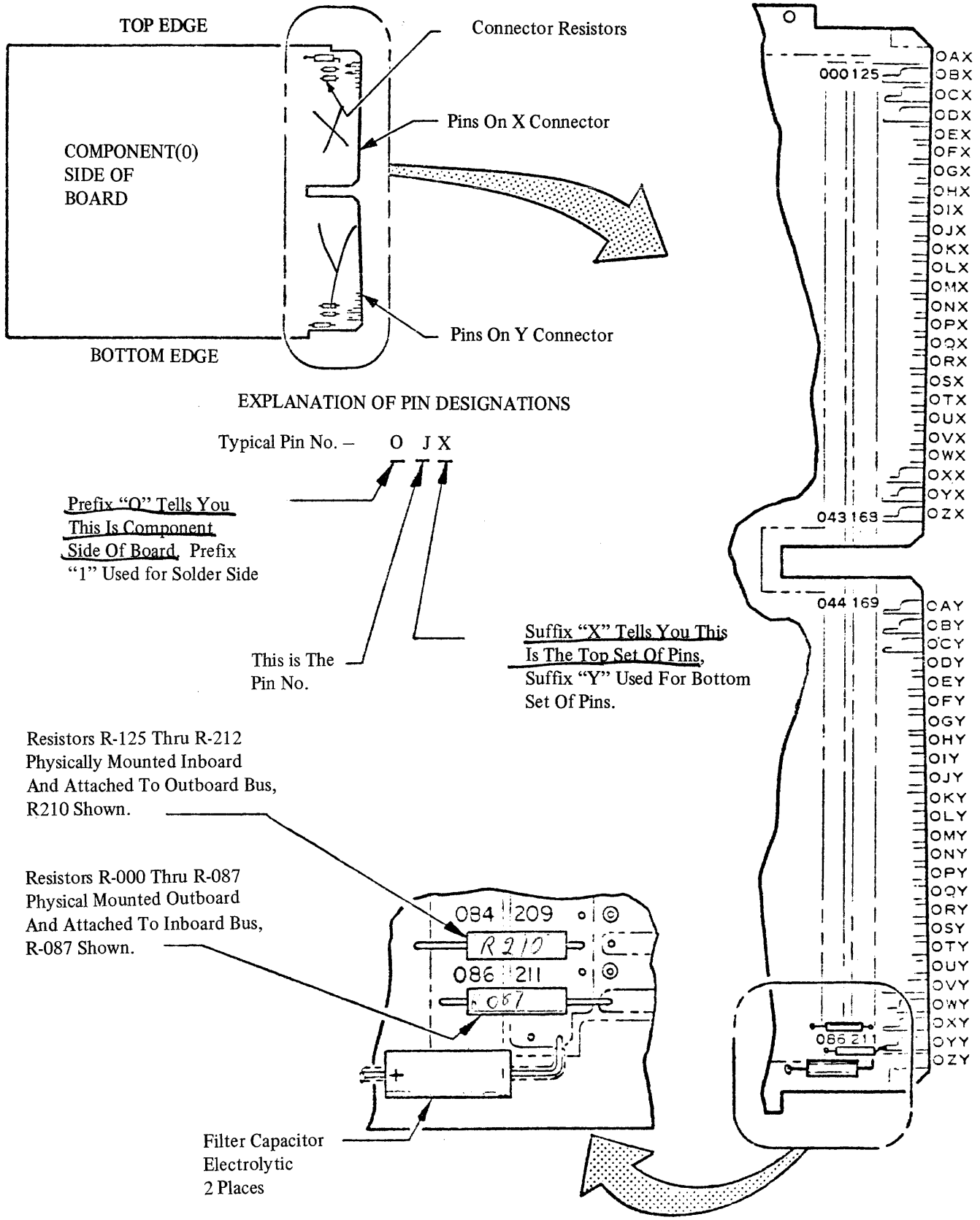


Fig. V-2 DESIGNATION SCHEME FOR PINS AND RESISTORS ON BACK PLANE CONNECTORS

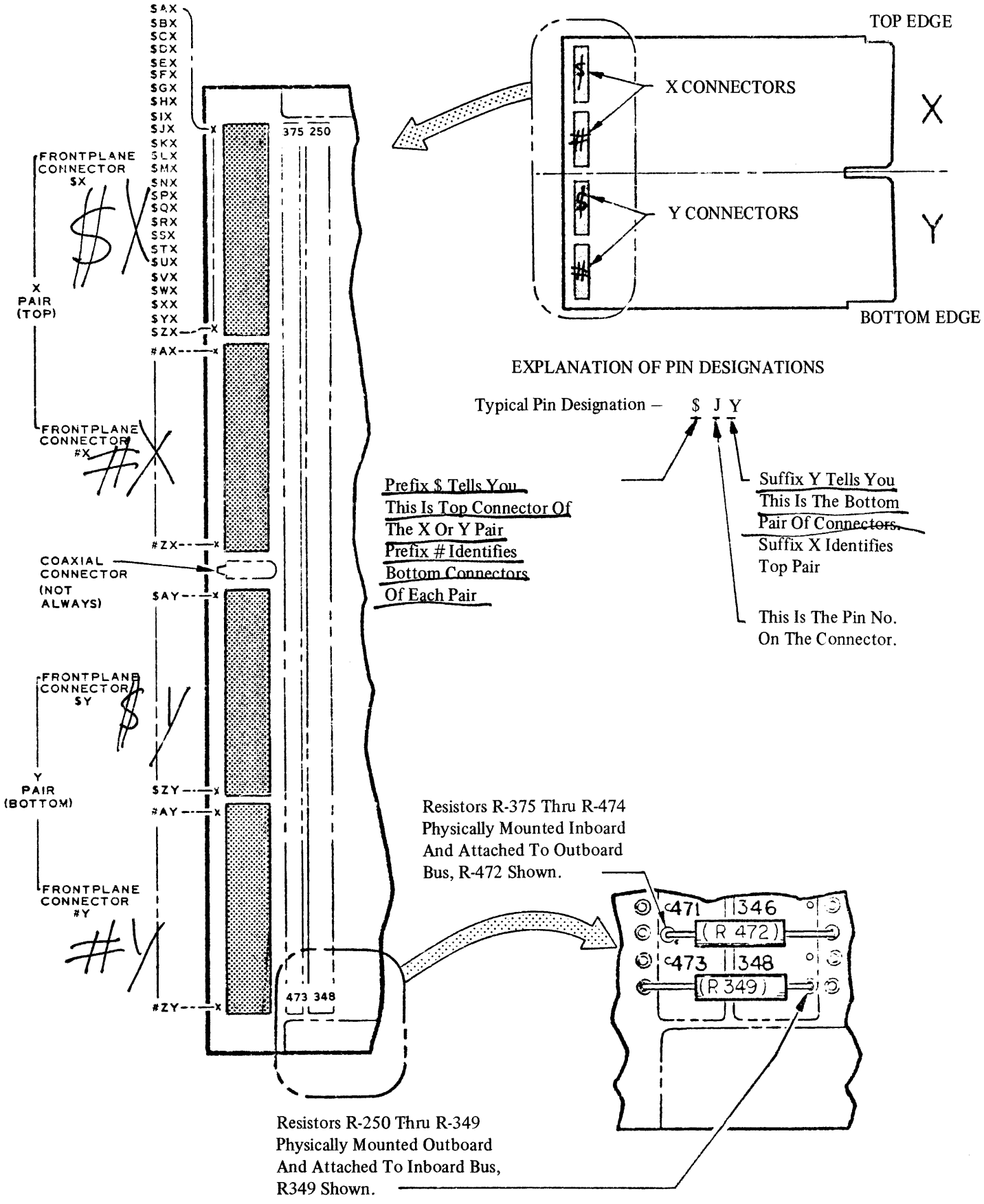
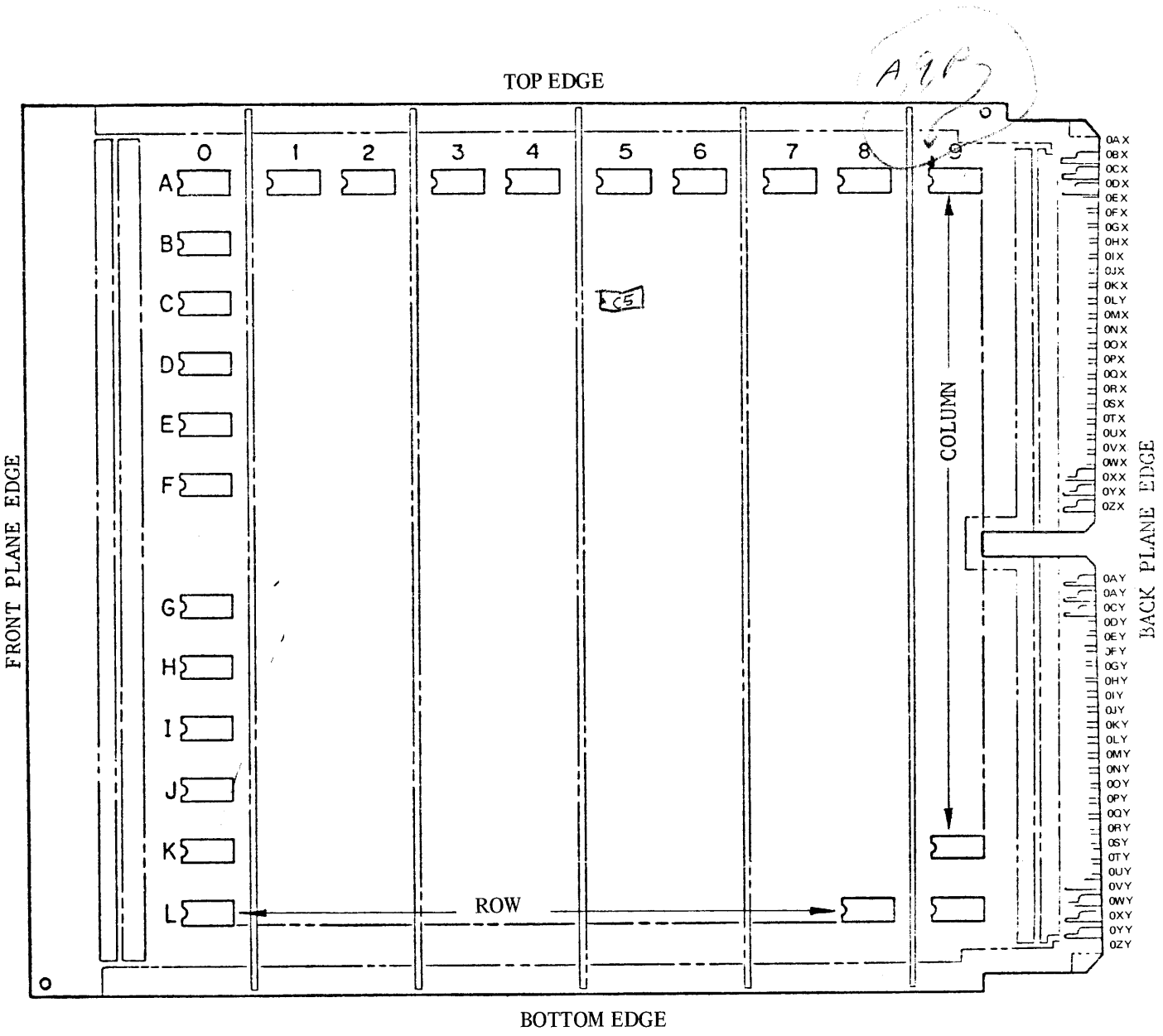


Fig. V-3 DESIGNATION SCHEME FOR CONNECTOR PINS AND RESISTORS ON FRONTPLANE EDGE OF CARD



NOTE:
The Row, Column Coordinate Location Of A Chip Is Used As It's Reference Designation On The Card Logic Diagram; EG. A Chip Located In Row C, Column 5 Has the Ref. Designation C5.

Fig. V-4 COORDINATES FOR CHIP LOCATIONS ON COMPONENT SIDE OF BOARD

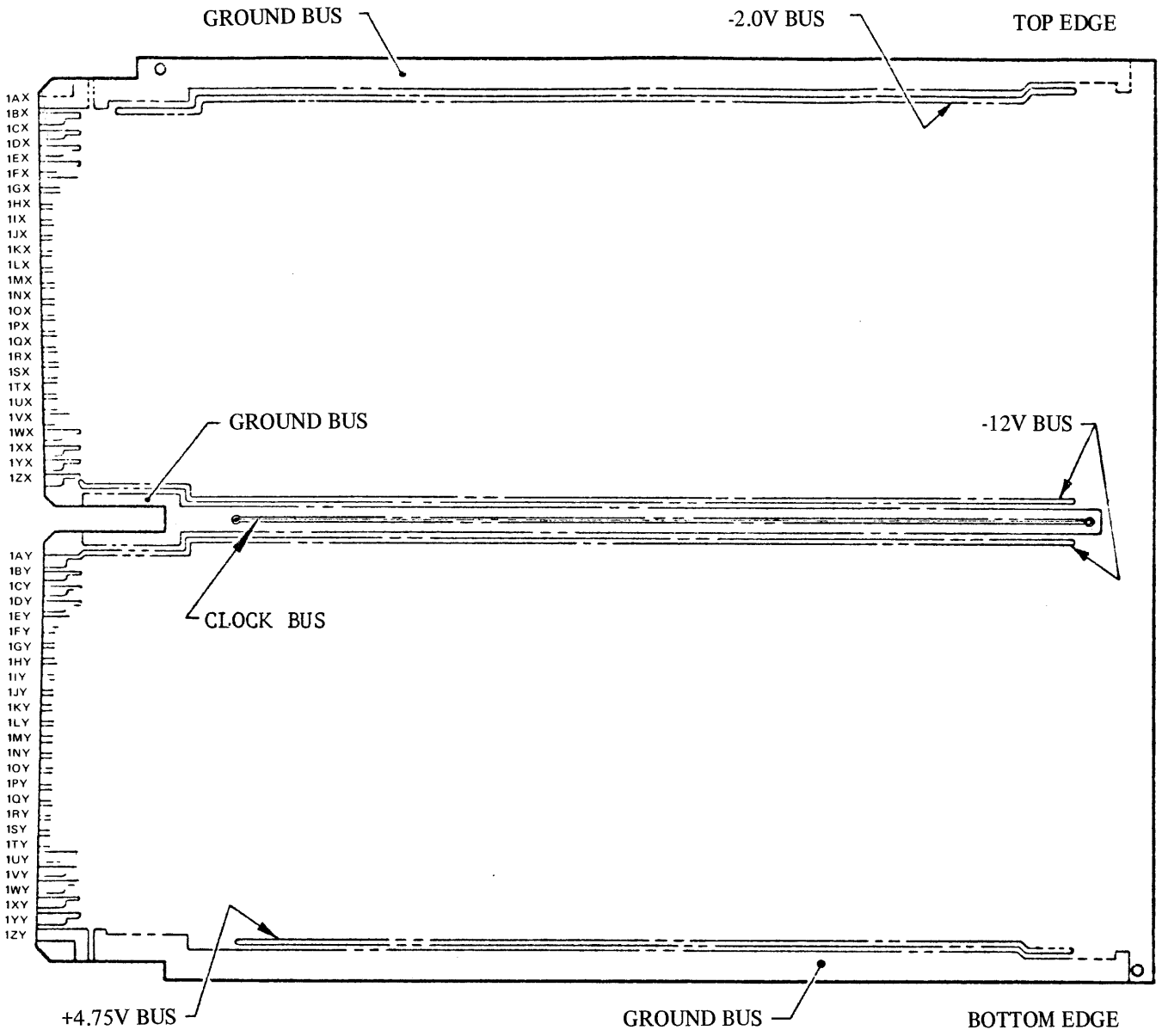


Fig. V-5 ARRANGEMENT OF BUSSES ON SOLDER SIDE OF CARD

B1700 MEMORY STORAGE CARDS

Memory for the B1700 is located on pluggable cards that are 14½ inches long by 12½ inches high. There is etching on both sides of cards.

The card sides are designated either even or odd with the components being mounted on the even (0) side. The soldered side is referred to as the odd (1) side. The cards have 50 backplane connections on each side. These are divided into sections X and Y, with X being the upper and Y being lower. The contacts of the cards are lettered A through Z, with the letter O being omitted. Therefore, it is possible to have 100 connections to the backplane wiring.

In theory each card could contain up to 198 chips. They however contain only 128. The card consists of 18 rows with 11 columns in each row. Rows are oriented from top to bottom and are identified alphabetically by the letters A through S, with the letter O omitted. Columns are identified numerically. They are numbered 0 through 10 left to right, with 10 being nearest to the backplane connector. See Figure V-6.

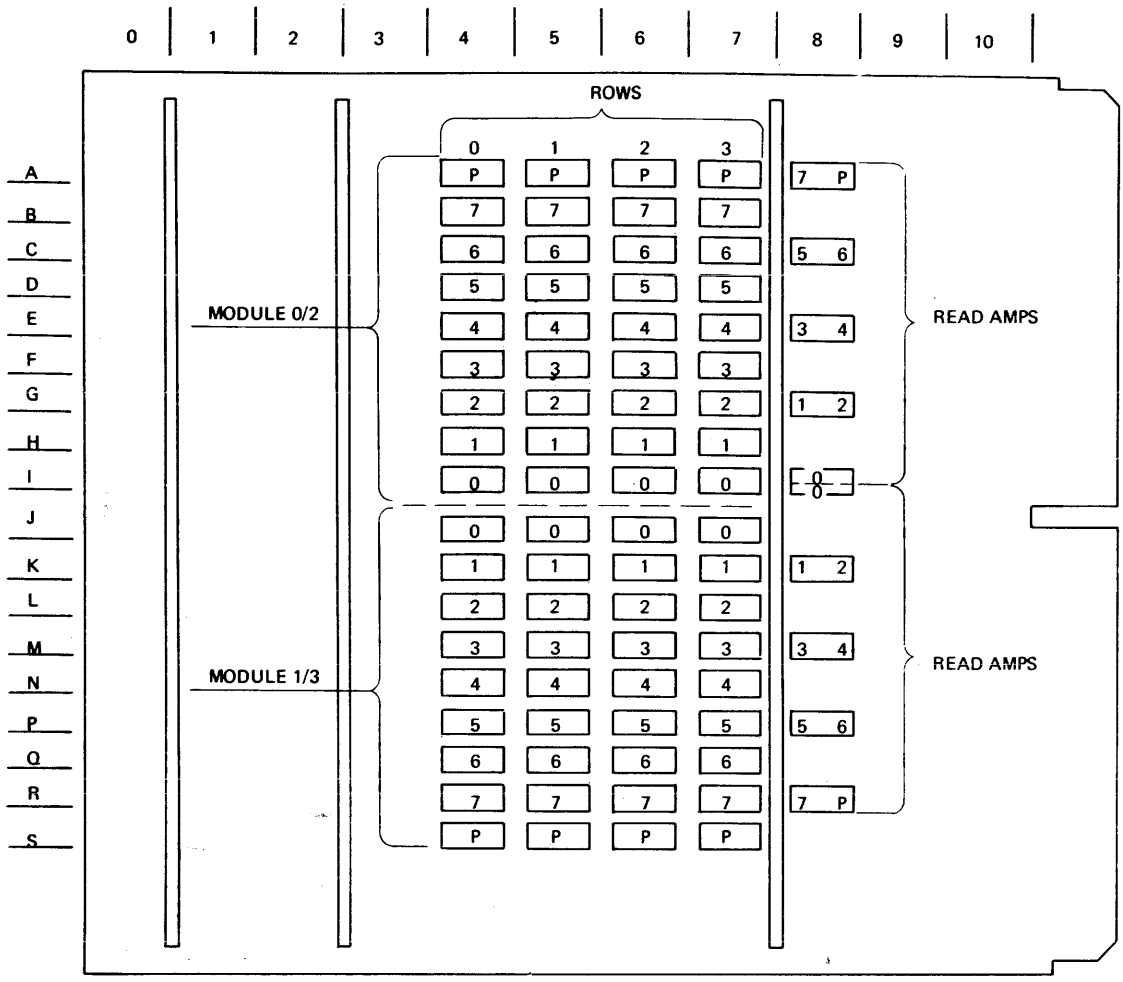


Fig. V-6 MEMORY STORAGE CARD

INTEGRATED CHIPS

Each chip contains external pins which serve as connections to and from the integrated circuits within the chip to the etched card. See Figure V-7 thru Figure V-9.

14 Pin Chip

Seven pins on each side of the chip. One side is lettered A through G, the other side is lettered H through P with the letters I and O being omitted.

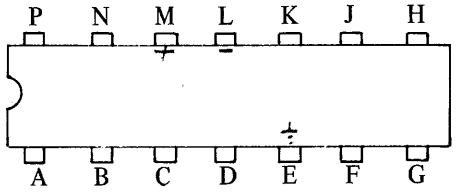


Fig. V-7 14 PIN CHIP

16 Pin Chip

The 16 Pin chip is similar to the 14 Pin chip except for the additions of Pin R and Pin S.

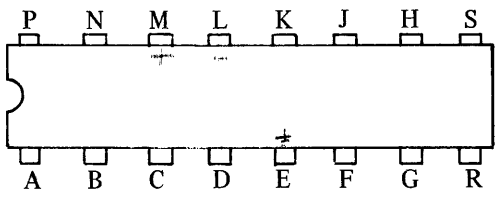


Fig. V-8 16 PIN CHIP

Dedicated Chip Pins are:

Pin E	Ground
Pin M	+4.75
Pin L	-2V

18 Pin Chip

The 18 pin chip is similar to the 16 pin chip except for the addition of Pin T and Pin U.

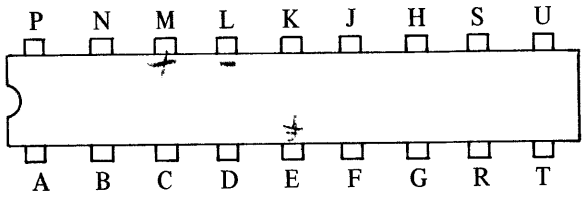
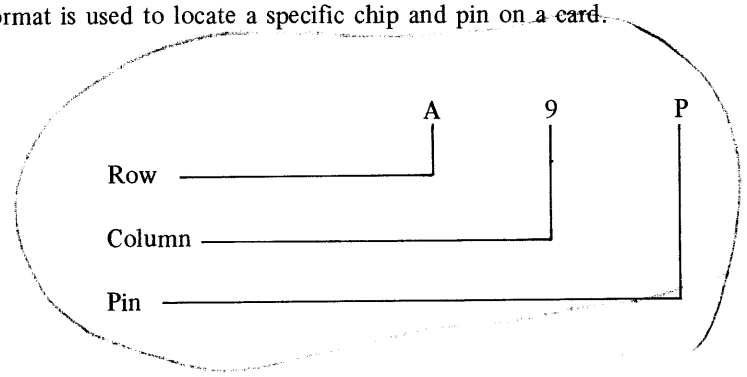


Fig. V-9 18 PIN CHIP

The following format is used to locate a specific chip and pin on a card.



Therefore:

For location A9P, the chip would be located in the upper right-hand corner of the card near to the backplane connector etching.

1. A B1700 logic card consists of two sections:
   A. Upper or X section
   B. Lower or Y section
2. These sections are physically separated by the spacing of chip rows F and G.

	Upper X	Lower Y
Backplane Pins	OAX -> OZX 1AX -> 1ZX	OAY -> OZY 1AY -> 1ZY
Frontplane Pins	$AX -> $ZX #AX -> #ZX	$AY -> $ZY #AY -> #ZY
Chip Locations	A0 -> A9 B0 -> B9 C0 -> C9 D9 -> D9 E0 -> E9 F0 -> F9	G0 -> G9 H0 -> H9 I0 -> I9 J0 -> J9 K0 -> K9 L0 -> L9
Backplane Resistors	000 -> 043 125 -> 168	044 -> 087 169 -> 212
Frontplane Resistors	250 -> 299 375 -> 424	300 -> 349 425 -> 474

Fig. V-10

0AX		1AX	+4.75V		
1DX		1JX	1QX	1WX	Ground
1DY		1JY	1QY	1WY	
0ZY	1ZY	-2. VOLTS			
XOW	--	CLOCK			

√ Fig. V-11 DEDICATED BACKPLANE PINS

Cards that are designated for major clock distribution will have a coax connector located near the frontplane between chip locations FO and GO.

DISCRETE COMPONENTS

Resistors or capacitors that are external to a chip are referred to as discrete components. These components may be installed in the following manner on a card.

Capacitors

1. Physically located in a chip position.
2. Physically mounted on top of a chip.

Resistors

1. Physically located in a chip position.
2. Installed adjacent to frontplane or backplane connector etching. See Figures V-2 and V-3.
3. 150 ohm to ground mounted on the solder side.

VOLTAGE DISTRIBUTION

Operating voltages enter a card through backplane pins. See Figure V-12.

Voltages	Backplane Pins
+4.75v	0AX 1AX
-2v	0ZY 1ZY
-12v (when required by a card)	1AY 1ZX
+12v (when required)	1 LY

√ Fig. V-12 LOGIC VOLTAGE PINS

The main distribution busses for +4.75 and -2v are located on the component (0) side, across the top and bottom of the card respectively. Coinciding busses on the soldered (1) side of a card are for ground distribution. Additional voltage distribution is provided by five (5) insulated buss bars installed vertically on the card.

****WARNING: NEVER PERMIT A HOT SOLDERING IRON TO COME IN CONTACT WITH THE INSULATED BARS.**

CHIP REPLACEMENT

To replace a chip that is soldered to a card use the following procedure.

1. Use a CLEAN low heat soldering iron. Do not force the iron into etching. Let the heat do the work.
2. Heat each leg on the solder side and use desolder pump tool #1622 2887 to remove solder from each leg.
3. Using a solder aid or small screwdriver press each leg toward chip body (on component side). This should break any leg loose that might still be sticking.
4. Lift out chip with chip removal tool #1622 4206. Do not pry with screwdriver or other instrument for this can break etching.

*****CAUTION: DO NOT OVERHEAT AS EXCESSIVE HEAT WILL DAMAGE THE ETCHING.**

CARD INSTALLATION

When installing a B1700 logic card in the backplane, the component (0) side should be to the right and the soldered (1) side to the left. As a further aid and protective measure, the cards are keywayed: That is to say that the notches that are cut at the top and bottom of the card are of different lengths and coincide with the card receivers that are mounted in the backplane. These keyways help prevent the card from being incorrectly installed in the backplane.

B1700 CARD SCHEMATICS

B1700 card schematics may contain the logic, all associated interconnections, all mnemonic signal names and their distribution for up to 120 chips.

Rules

1. Schematics for a single card will consist of one (1) or more pages.
2. Logic flow is from left to right.
3. A signal can be either:
   A. Uni-Directional – signal moves in one direction only.
   B. Bi-Directional – signal may move in either direction.
4. Uni-Directional input signals from frontplane connectors will enter a card schematic at the top of the page. Uni-Directional output signals will leave from the bottom of the page.
5. Bi-Directional signals from frontplane connectors may appear at the top or bottom of the page.
6. Backplane and inter-page output signals will exit to the right.

Rules for Signal Names

Logical names, whether input or output names, are eight characters in length and are composed of letter special symbols, digits and/or spacers. The first character must be a letter or a digit and unused positions must be filled with spacers. The permissable characters are:

Letters: A through Z excluding Ø

Special Symbols: $\neq$, $\geq$, $\leq$, +, –, *, $\leftarrow$, /, =, $\rightarrow$

Digits: 0 through 9

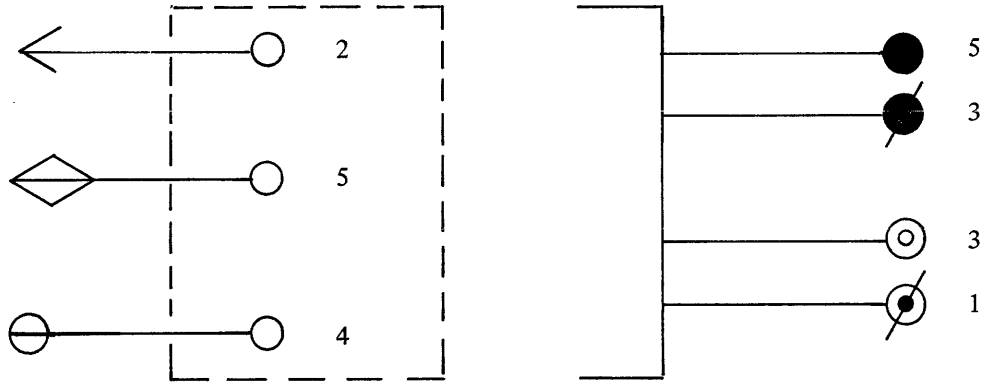
Spacer: Period (.)

PSEUDO CONNECTION SYMBOLS AND PRINCIPLE

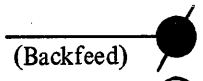
A B1700 logic card contains up to 120 chips. In order to provide high quality legible prints it is not possible to draw a complete card schematic on one page. In addition, due to the complexity of many circuits it was not feasible to completely illustrate all interconnections between chips. To circumvent this problem and alleviate congestion on the system drawings pseudo connection symbols were created. The placement of these symbols in conjunction with a numerical value designates the actual number of places that the logic signal is used as a source or a sink. The following explanation describes the symbols employed on B1700 Documentation. All of these symbols implement the pseudo connection principle.

Internal Page Symbols

The numeral directly to the right of these symbols designates the number of places that the signal goes to on a particular page.

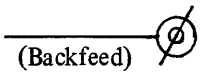



Logic that is generated and used on this page only.



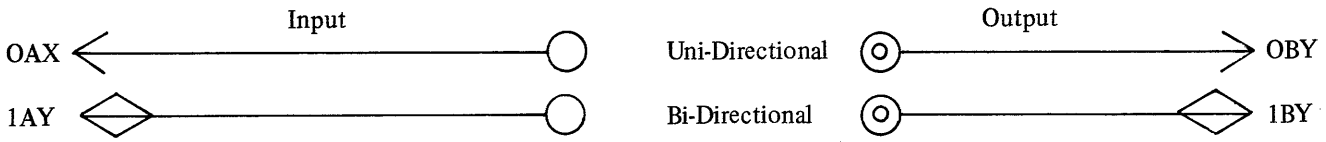
Logic generated and used on this page only. At least one sink is located to the left of the source.


Logic that is generated and used on this page. This signal is an output from this page.



Logic that is generated and used on this page. Sink that is located to the left of this source. Signal that is an output from this page.

BACKPLANE PINS SYMBOLS



Backplane pins are labeled A through Z with the letter O being omitted. Backplane pin designation is shown in Table V-1 where a is equal to a letter A through Z. Backplane pins are listed to the left of an input signal, and to the right of an output signal.

0aX
1aX
0aY
1aY

TABLE V-1

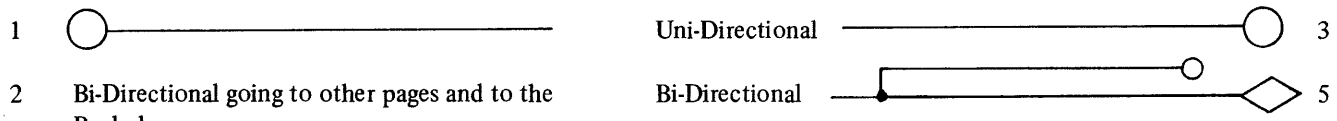
FRONTPLANE PIN SYMBOLS

Frontplane pins are labeled A through Z with O being omitted. Frontplane pin designation is shown in Table V-2 where a is equal to a letter A through Z.

$aX
#aX
$aY
#aY

TABLE V-2

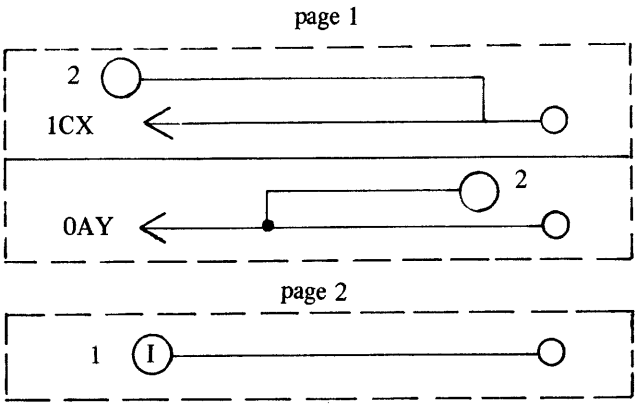
INTER-PAGE CONNECTIONS SYMBOLS



ORX

The number to the left of an input signal designates the page where the signal originated.

The number to the right of an output signal references the page or pages where that signal is used.



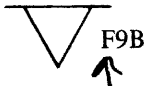
Logic generated on page 2 is OR-ed with backplane inputs on page 1.

An input from the backplane on page 1 where the logic is used. It is also used on page 2 where the input signal will contain an (I).

This symbol signifies that the input is a backplane pin input to page 1.

SPECIAL SYMBOLS

A triangle placed perpendicular to an output signal line designates that a pull down or load resistor is connected to this circuit. The accompanying alpha numeric combination tells the chip location and pin where this resistor is located.



An inverted triangle placed on an output line designates a 150 ohm load resistor to ground on the solder side of the board. The alpha numeric combination next to the triangle indicates the pin location the resistor is tied to.

PREVENTATIVE MAINTENANCE

Preventative maintenance procedures consist of inspection and cleaning. They are invaluable in keeping the central system operational and functioning accurately.

When operating schedules permit, perform these checks listed below.

1. Check for proper installation of all cards and cables.
2. Check power supply voltages (Logic and Memory). Refer to Section VI for adjustments, if needed.
3. Check the cleanliness at the Central System. Look for foreign particles or corrosion.
4. Ensure that all fans rotate freely.
5. Ensure that those fans that do not have airflow switches are operational.
   NOTE: Never remove or install any item to the system while power is on during preventative maintenance.
6. Periodically check the air flow filter. Replace if necessary.

Preventative maintenance procedures for the I/O controls are described in Section V of the B1700 I/O Base Technical Manual. Preventative maintenance for all peripherals are described in their respective technical manuals.

TROUBLESHOOTING PROCEDURES

The following troubleshooting procedures describe general techniques applicable to all operations. They shall be divided into two (2) distinct groups. One is a general troubleshooting technique that localizes a problem and solves it in broad terms. The other is specific troubleshooting as it applies to the B1700 Processor.

GENERAL TROUBLESHOOTING TECHNIQUES

The general steps for troubleshooting a problem are illustrated in Figure V-13. These general steps are described below.

1. Define the Problem. Take time to thoroughly define the problem. For example, if the 1C Micro (Move Sum to T) does not produce the correct results, is the fault the function of the registers the adder, the carry, or some other element? Are the operational registers being properly loaded? Use the displays, backplane, and integrated circuit terminations to gather the necessary data.
2. Look for Obvious Solutions. Make sure that a malfunction has actually occurred. Relate problems to recent events such as cleaning or servicing. Look for improperly set controls or test equipment and accidental disconnections of cables, etc. Consider miscellaneous temporary failures, such as mechanical jamming of peripheral equipment.
3. Locate the Trouble Area. Isolate the fault to a functional area of the system. Isolating the malfunctioning area is generally a process of eliminating the functional areas that are operating properly.
4. Analyze the Isolated Area. When the fault has been isolated to a functional area, the rest of the system can be temporarily ignored. Use the logic schematics and associated documentation to isolate the problem to an individual card or element.
5. Correct the Fault. Repair the faulty card or replace the faulty element. Attempt to analyze the cause of the failure (before restoring power) to prevent recurrence of the failure.
6. Restore the System to Operation. When the system appears to be operating correctly, make sure it is returned to normal operating conditions. If cards or cables have been removed, be sure that they are properly reseated. Correctly set all controls. Finally, verify proper operation by running the test programs.

PROCESSOR TROUBLESHOOTING

The specific troubleshooting procedures outlined in the following paragraphs are used when it has been determined that the processor is not operating properly. This is usually determined by the use of test programs. A failure in the processor generally produces failures in more than one test. Some test programs may not exercise a failing function within the processor, so all test programs should be used. Also, use should be made of the console to determine where a failure may be present. Knowledge of the console and how to access memory and processor registers will lend much assistance in troubleshooting the memory or processor.

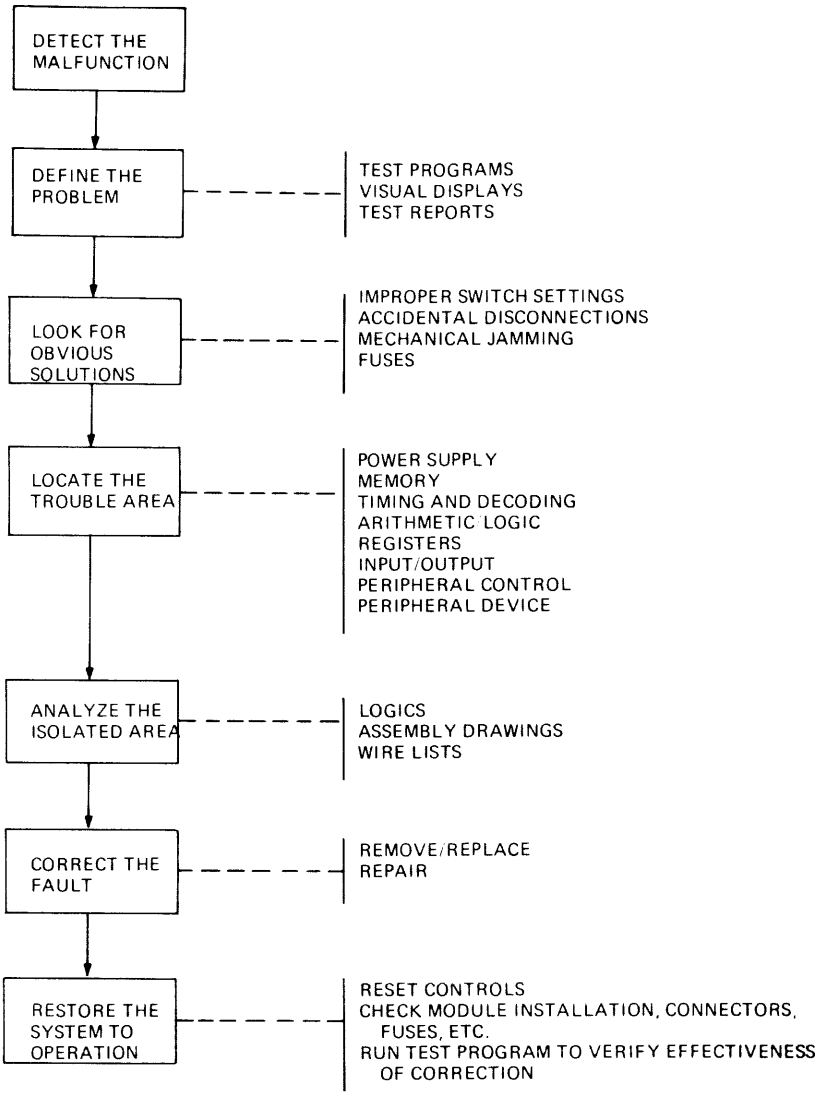


Fig. V-13 TROUBLE SHOOTING FLOW

B1700 CONSOLE

The Console provides for:

1. Power On/Off
2. Mode Select
3. Register Load and Display
4. Memory Load and Display
5. Cassette Operation

Console Controls and Their Function

24 Console Lamps

The 24 Console Lamps are used to display the contents of the 24 Bit Main Exchange. In the Halt Mode this display will be either the contents of a selected register or the contents of a memory location.

24 Console Switches

The 24 Console Switches are used in the Halt Mode to enter data in a selected register or into an addressed memory location.

Register Select and Register Group Switches

The Register Group Switch is the large rotary switch at the lower left corner of the console. The Register Group selects a co-ordinate to select four registers. The Register Select switch then selects one of the four and is located to the immediate right of the Register Group Switch.

MODE SWITCH

The Mode Switch places the processor in one of three modes, Step, Run or Tape. With the processor HALTED and the Mode Switch in the Step position, one micro will be executed by depressing START and the machine returns to the halted state with the next micro to be executed in the Register. If the Mode Switch is in the Run Mode, the processor will upon depression of the start button continuously execute micros until either the Halt Button has been depressed or the Halt Micro has been decoded in the M Register. In the Tape Mode, the processor will upon depression of the start button, start tape movement and execute the micros on the tape. The machine is returned to the halted state by depression of Halt Button, detection of a Halt Micro, Tape Error or Cassette Stop Micro having been decoded. In all cases the Tape will not stop until the next gap is detected.

CLEAR PUSHBUTTON

The Clear Button generates the general clear (GPCLRBCO) which resets the system and clears the following registers in the processor: M, C, U, ML, MAR(A), MIR and the Stack Pointer.

HALT PUSHBUTTON

The depression of the Halt Button will cause the processor to halt at the completion of the current micro in the M Register. Before the halt occurs the next micro will be fetched into M and the address will be upcounted to point at the next micro.

INTERRUPT SWITCH

The Interrupt Switch will cause the HALT1. C0 flip-flop to set on card C. The output term HALT1. C0 is sent to the CC Register bit zero position and causes CC(0) to set. This interrupt bit is software controlled. It is reset by depressing the clear button.

INCREMENT A PUSHBUTTON

Depression of the Increment A Pushbutton will cause the address in MAR(A) to be upcounted by 16 bits or one micro word. This switch is generally used in conjunction with reading or writing S-Memory from the console. The machine must be in the halted state for operation of the Increment A Button.

START PUSHBUTTON

The Start Button is depressed normally to cause the machine to be placed in the Run State and thus cause an execution of a series of micro instructions. If the Mode Switch is in the Run Mode then the micros will be obtained from S-Memory, or if the Mode Switch is in Tape Mode then the micros will be obtained from the Cassette Loader on the Console. If the Mode Switch is in the Step Mode then depression of Start will cause the execution of one micro and the machine will return to the Halt State.

READ-WRITE PUSHBUTTON

The Read-Write Pushbutton will produce a pulse to cause either a read or write of S-Memory depending upon the position of the Register Group Rotary Swtich. If the switch is in the READ position then depression of Read/Write will cause a read of the location specified by the address previously loaded in MAR(A). The read data (24 bits) will be displayed in the Console Lamps. If the switch is in the WRITE position then the contents of the Console Switches will be written into the location specified by MAR(A). The machine must be in the halted state for these operations to occur.

LOAD PUSHBUTTON

The Load Button is used for loading data in various registers from the Console Switches. The register to be loaded is selected by the Register Group and Register Select Rotary Switches. Data to be loaded is placed in the Console Switches and by depression of the load button the selected register is loaded with this data.

POWER ON/OFF SWITCH

Power On/Off Switch is the switch for system power ON or power OFF.

RUN INDICATOR

The Run Indicator when lit indicates the machine is in the Run State and either executing micros from the Cassette Loader or from S-Memory.

CASSETTE ON/OFF

Cassette On/Off is the power on/off for the Cassette Loader.

BOT INDICATOR

The Beginning of Tape Indicator is lit when tape in the Cassette Loader is at the beginning of tape as detected by the Cassette.

REWIND SWITCH

The Rewind Switch when depressed will cause the tape in the Cassette Loader to return to the Beginning of Tape.

TAPE PARITY INDICATOR

The Tape Parity Indicator illuminates when the parity detection logic detects a parity error of data on the Cassette Tape.

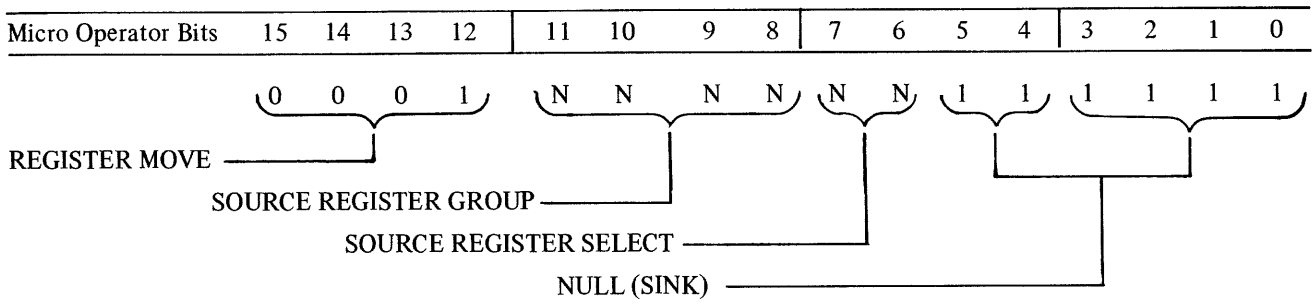
BASIC CONSOLE TROUBLESHOOTING

Philosophy: When the processor is not running the 24 console lights display the contents of a register selected by the console control switches. At this time certain signals are present on the backplane that are useful for troubleshooting basic console Load/Display operations.

Basic Console Theory: In a halted state a hardware forced micro-operator is generated and continuously executed by the processor to permit the loading and displaying of registers from the console. This micro is a 2 clock 1C Register Move Microperator. Processor card C contains the logic which generates this micro and also develops control signals used by some of the registers during their load/display cycles.

Display Cycle: When displaying, we move the register to be displayed to no-where or NULL. This places the contents of the register on the Main 24 Bit Exchange. The console indicator lamps are coupled to the main 24 bit exchange. Therefore the pattern displayed in the console lamps is a visual representation of the contents of the register selected.

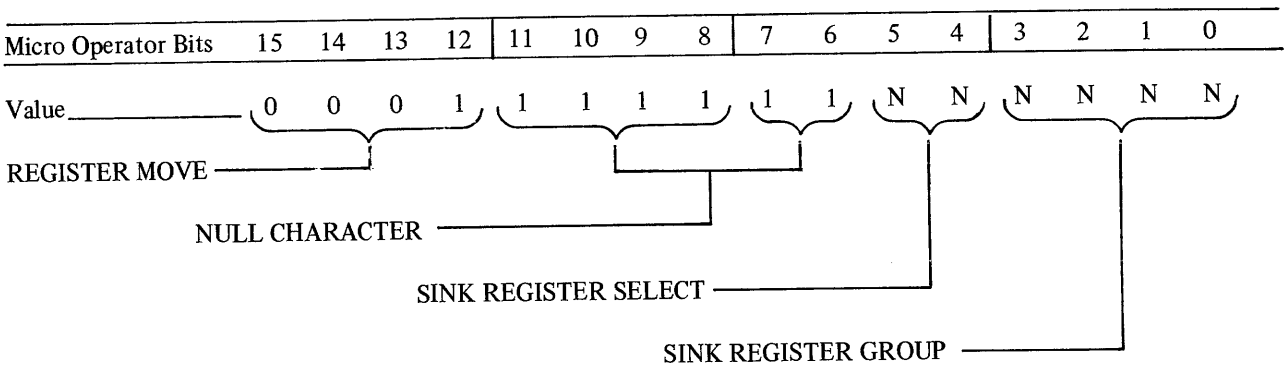
1C Register Move DISPLAY



N = Variable Dependent upon which register is selected.

Load Cycle: During a load cycle the status of the 24 console switches are gated on to the main exchange and transferred into the desired register. The load pushbutton located on the front console generates a pulse exactly two clock periods in duration every time it is depressed.

1C Register Move LOAD



N = Variable dependent upon which register is selected.

Signals and Their Backplane Pin Assignments

Micro – Op Bit	PIN
15	1KY
14	0KY
13	1GY
12	0GY
11	1ZX
10	0ZX
09	1VX
08	0VX
07	1SX
06	0SX
05	1NX
04	0NX
03	1KX
02	0KX
01	1GX
00	0GX
LOAD . . C0	0WY

B1700 PROCESSOR CARDS

Processor Card A

1. Local Memory Buffer Bits 00-11
2. Local Memory B Data Bits 00-11
3. Part of Local Memory Interface
4. Local Memory A Data Bits 00-11
5. Part of Local Memory Interface
6. Binary Adder 00-11
7. Decimal Carry Correction
8. Decimal Sum Correction
9. Multiplex Data to Main Exchange 00-11
10. Mask Generator 00-11
11. LSUX-LSUY
12. Part of CYL Logic
13. Part of MSBX Logic
14. Part of A & B Data OR's
15. Source of one of 4 Bit Multiplex Data
16. Part of 24 Bit Comparator

Processor Card B

1. Local Memory Buffer 12-23
2. Local Memory B Data 12-23
3. Part of Local Memory Interface
4. Local Memory A Data 12-23
5. Part of Local Memory Interface
6. Binary Adder 12-23
7. Decimal Carry Correction
8. Decimal Sum Correction
9. Multiplex Data to Main Exchange 12-23
10. Mask Generation 12-23
11. Part of CYL Logic
12. Part of MSBX Logic
13. Source Two 4 Bit Multiplex Data
14. Part of A & B Data OR's
15. 4 Bit Function Box
16. Part of Data Comparator

Processor Card C

1. Logic Function: CP Logic
2. Logic Function: Control Panel Interface
3. Logic Function: Part of Control Logic
4. Logic Function: Part of Control Logic

Processor Card D

1. 125 and 250ns timing source
2. Local Memory "write enable", chip select and address logic.
3. Micro Finish logic
4. Function Box Multiplexor controls (4-bit and 24-bit fields).
5. Arithmetic Control (subtract, FL compare, FL down, BCD add, INC/DEC test)
6. M register decode logic.

Processor Card E

1. Part of Cassette Logic
2. Multiplex Data to Main Exchange and to I/O Buss Bits 0-11
3. Multiplex Data to Main Exchange and to I/O Buss Bits 12-23
4. Input Logic to M. Register 0 = 16 Buffers to Mop Lines

Processor Card F

1. Sequencer Timing Pulse Generator Micro-operator Decodes for 01C-145C
2. "A" Stack Pointer, Mult Clock, Address & Chip Select Micro-operator Decode
3. Multiple Clock, Chip Select, Address Logic.
4. State Mach Cont. "M" Reg Cont, "S" Memory Write Cont. Lift Mask Logic
5. Misc. Controls Incl. Memory, Rotator, MIR. 4 Bit Branch, Skip, MD Decode, Upper "C" Register

Processor Card H

1. Mar (A)
2. FA Manipulate
3. Mar to Mex.
4. FA Distribution Logic – Bytes 0 & 1
5. FA Distribution Logic – Bytes 2 & 3
6. Mar(A) Control
7. Parity Manipulate
8. Refresh Address

Processor Card J

1. ML Register
2. Parity Check
3. Rotation Control Translation
4. Refresh Timing
5. Demand Refresh F/F
6. Read Data to MIR
7. Mex to Rotator
8. Rotator

Processor Card K

1. MIR (0-15)
2. MIR (15-31)
3. Parity Generate
4. Parity Manipulate Detect
5. MIR → MEX
6. Memory Base Timing
7. ½ Rotation Control
8. Real Time Clock
9. System Clock

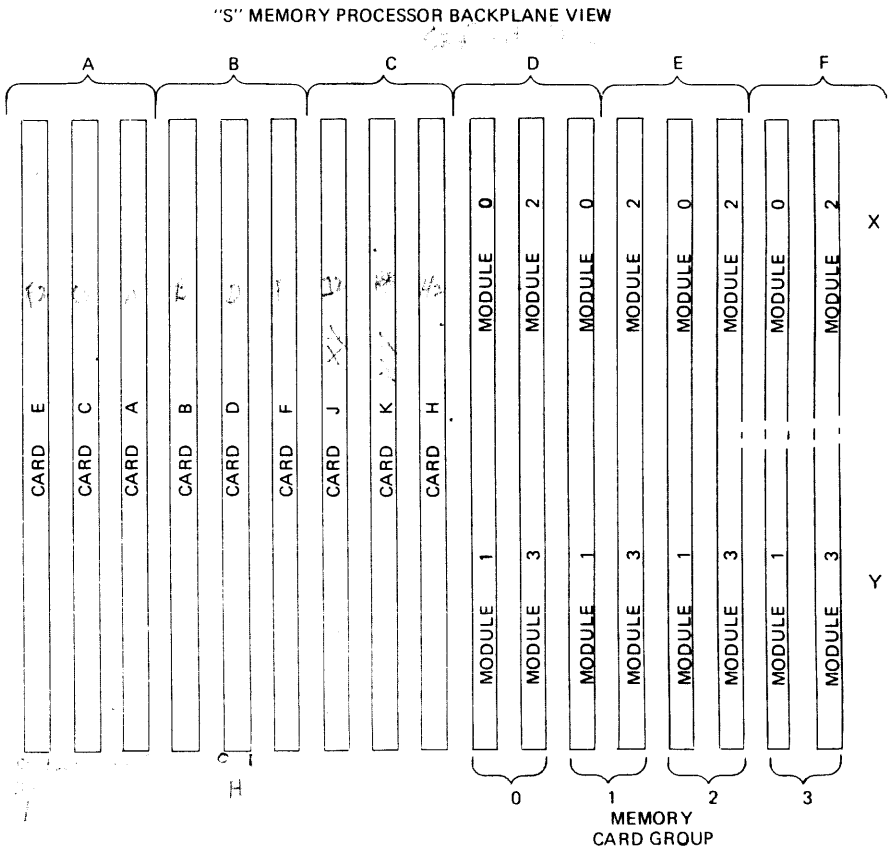


Fig. V-14 "S" MEMORY PROCESSOR BACKPLANE VIEW

REGISTER SUMMARY

MICRO-INSTRUCTION CONTROL REGISTERS

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
A (MAR)	19	ADDRESS REG.	SOURCE/DEST.	
M	16	MICRO-INST.	SOURCE/DEST.	
TAS	24	TOP OF STACK	SOURCE/DEST.	PSEUDO

MAIN MEMORY CONTROL REGISTERS

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
BR	24	BASE REG.	SOURCE	
LR	24	LIMIT REG.	SOURCE	
FA	24	FIELD ADR.	SOURCE/DEST.	
FL	16	FIELD LGTH.	SOURCE/DEST.	FLC/D/E/F
CP	8	ARITH. CTL.	SOURCE/DEST.	CYF, CPU, CPL
CYF	1	CARRY FLAG	SOURCE/DEST.	
CPU	2	ARITH. UNIT	DEST.	00 = BINARY 01 = 4-BIT
CPL	5	DATA LENGTH	SOURCE/DEST.	MAX. VAL. 24
MAXS	24	MAIN MEM. SIZE	SOURCE	
MAXM	24	CONTROL MEM. SIZE	SOURCE	
FLCN	4	FLD. LGTH. COND.	SOURCE/DEST.	

INTERRUPT CONTROL REGISTERS

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
CC	4	INTR. COND.	SOURCE/DEST.	0 = CONSOLE INTR. 1 = I/O SER. RQ. 2 = CLOCK INTR. 3 = STATE FLAG

GENERAL PURPOSE REGISTERS

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
X	24		SOURCE/DEST.	INP. TO FUNCT. BOX
Y	24		SOURCE/DEST.	INP. TO FUNCT. BOX
T	24		SOURCE/DEST.	
L	24		SOURCE/DEST.	
CA	4		SOURCE/DEST.	
CB	4		SOURCE/DEST.	

INPUTS TO 24-BIT FUNCTION BOX

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
X	24	INPUT	SOURCE/DEST.	
Y	24	INPUT	SOURCE/DEST.	
CYF	1	CARRY FLAG	SOURCE/DEST.	
CPU	2	ARITH. UNIT	DEST.	
CPL	5	DATA LENGTH	SOURCE/DEST.	

OUTPUTS FROM 24-BIT FUNCTION BOX

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
BICN	4	BINARY COND.	SOURCE	
XYCN	4	X AND Y COND.	SOURCE	
XYST	4	X AND Y STATES	SOURCE	
CYL	1	CARRY OUT LEVEL	SOURCE	
CYD	1	BORROW OUT LEVEL	SOURCE	

AVAILABLE FROM 24-BIT FUNCTION BOX

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
SUM	24	X + Y	SOURCE	AND CYF
DIFF	24	X - Y	SOURCE	AND CYD
XORY	24	X OR Y	SOURCE	
XEOY	24	X EXOR Y	SOURCE	
XANY	24	X AND Y	SOURCE	
CMPX	24	COMPL. X	SOURCE	AND CPL
CMPY	24	COMPL. Y	SOURCE	AND CPL
MSKX	24	MASK X	SOURCE	AND CPL
MSKY	24	MASK Y	SOURCE	AND CPL

MISCELLANEOUS REGISTERS

MNEMONIC	WIDTH	FUNCTION	USAGE	REMARKS
U	16	CASSETTE INPUT	SOURCE	
NULL	24		SOURCE	CONTAINS ZEROS
DATA	24	I/O DATA	SOURCE/DEST.	
CMND	24	I/O COMMAND	DEST.	

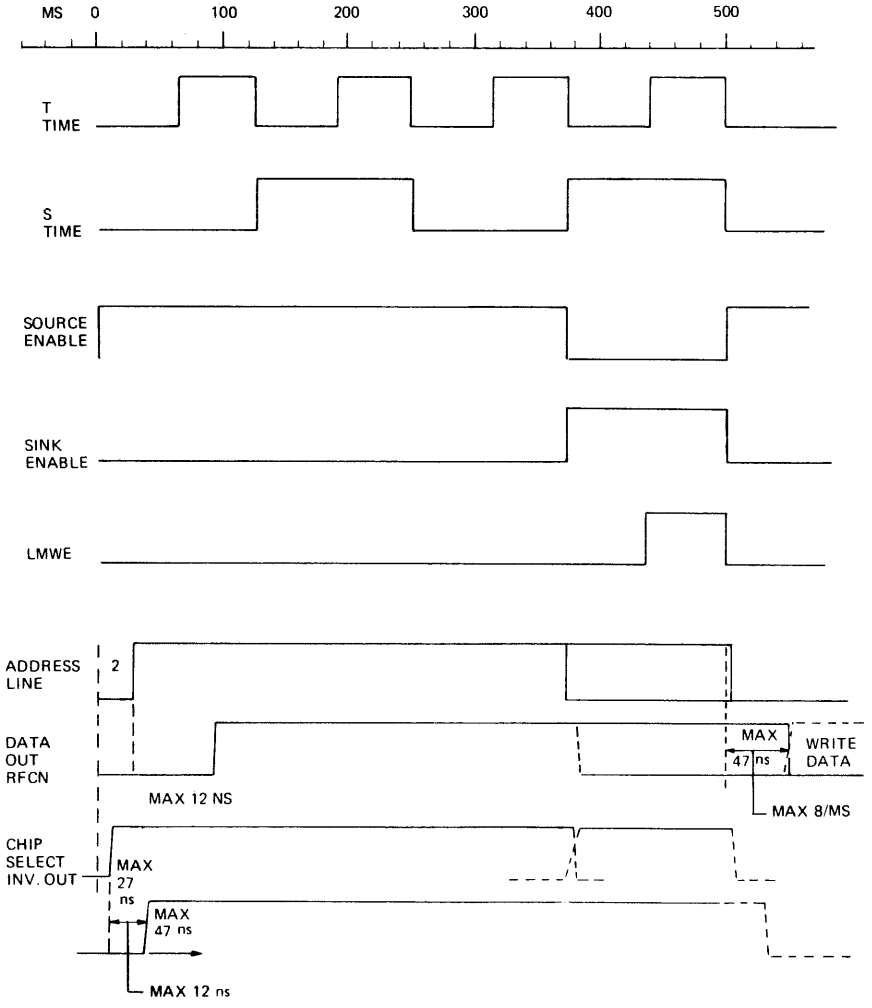


Fig. V-15 TIMING LOCAL MEMORY

LOCAL MEMORY ADDRESS LINE

ADDRESS LINE	SIGNAL NAMES	INPUT OF CARD A	INPUT OF CARD B	SOURCE CARD D
0	LMADD0T0	1KY	1KY	0 L Y
1	LMADD1T0	1LY	1LY	1 L Y
2	LMADD2T0	1NY	1NY	1 N Y
3	LMADD3D0	1RY	1RY	1 R Y

CHIP SELECT
A GROUP

A	CSAGPAD0		0 T X	0 T X
B	CSAGPBD0		0 U X	0 U X
C	CSAGPCD0		0 V X	1 U X
D	CSAGPDD0	0 B Y		0 B Y
E	CSAGPED0	0 D Y		0 D Y
F	CSAGPFD0	0 E Y		0 E Y

CHIP SELECT A PAD	CSAPADD0	0 A Y	0 S X	0 A Y
CHIP SELECT B GROUP	CSBGRPT0	0 G Y	0 Y X	0 Y X
CHIP SELECT B PAD	CSBPADD0	0 F Y	0 X X	0 X X

ADDRESS LINES				"A-DATA"								"B-DATA"			
LMADD3A1	LMADD2A1	LMADD1A1	LMADD0A1	CSAPADD0	CSAGPAD0	CSAGPBD0	CSAGPCD0	CSAGPDD0	CSAGPED0	CSAGPFD0	Register Selected	CSBPADD0	CSBGRPT0	Register Selected
0	0	0	0	0	1	1	1	1	1	1	FB	0	1	Reserved
0	0	0	0	0	0	0	1	1	1	1	FB			
0	0	0	0	0	1	0	0	0	0	0	FU			
0	0	0	0	0	0	1	0	0	0	0	FT			
0	0	0	0	0	0	0	1	0	0	0	FLC			
0	0	0	0	0	0	0	0	1	0	0	FLD			
0	0	0	0	0	0	0	0	0	1	0	FLE			
0	0	0	0	0	0	0	0	0	0	1	FLF			
0	0	0	1	0	1	1	1	1	1	1	X	0	1	Y
0	0	1	0	0	1	1	1	1	1	1	T	0	1	Reserved
0	0	1	0	0	1	0	0	0	0	0	TA			
0	0	1	0	0	0	1	0	0	0	0	TB			
0	0	1	0	0	0	0	1	0	0	0	TC			
0	0	1	0	0	0	0	0	1	0	0	TD			
0	0	1	0	0	0	0	0	0	1	0	TE			
0	0	1	0	0	0	0	0	0	0	1	TF			
0	0	1	1	0	1	1	1	1	1	1	L	0	1	Reserved
0	0	1	1	0	1	0	0	0	0	0	LA			
0	0	1	1	0	0	1	0	0	0	0	LB			
0	0	1	1	0	0	0	1	0	0	0	LC			
0	0	1	1	0	0	0	0	1	0	0	LD			
0	0	1	1	0	0	0	0	0	1	0	LE			
0	0	1	1	0	0	0	0	0	0	1	LF			
0	1	0	0	0	1	1	1	1	1	1	FA	0	1	TEMP-B (Reserved)
0	1	0	1	0	(Any or All)						Reserved	0	1	Reserved
0	1	1	0	0	(Any or All)						Reserved	0	1	BR
0	1	1	1	0	(Any or All)						Reserved	0	1	LR
											A-Stack Word #			A-Stack Word #
1	0	0	0	0	1	1	1	1	1	1	0	0	1	8
1	0	0	1	0	1	1	1	1	1	1	1	0	1	9
1	0	1	0	0	1	1	1	1	1	1	2	0	1	10
1	0	1	1	0	1	1	1	1	1	1	3	0	1	11
1	1	0	0	0	1	1	1	1	1	1	4	0	1	12
1	1	0	1	0	1	1	1	1	1	1	5	0	1	13
1	1	1	0	0	1	1	1	1	1	1	6	0	1	14
1	1	1	1	0	1	1	1	1	1	1	7	0	1	15
											Left Pad Word #			Right Pad Word #
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0	0	0	0	1	1	0	1
0	0	1	0	1	0	0	0	0	0	0	2	1	0	2
0	0	1	1	1	0	0	0	0	0	0	3	1	0	3
0	1	0	0	1	0	0	0	0	0	0	4	1	0	4
0	1	0	1	1	0	0	0	0	0	0	5	1	0	5
0	1	1	0	1	0	0	0	0	0	0	6	1	0	6
0	1	1	1	1	0	0	0	0	0	0	7	1	0	7
1	0	0	0	1	0	0	0	0	0	0	8	1	0	8
1	0	0	1	1	0	0	0	0	0	0	9	1	0	9
1	0	1	0	1	0	0	0	0	0	0	10	1	0	10
1	0	1	1	1	0	0	0	0	0	0	11	1	0	11
1	1	0	0	1	0	0	0	0	0	0	12	1	0	12
1	1	0	1	1	0	0	0	0	0	0	13	1	0	13
1	1	1	0	1	0	0	0	0	0	0	14	1	0	14

Fig. V-16 LOCAL MEMORY ADDRESS LINES & CHIP SELECT

MICRO	NUMBER OF BITS IN MASK	AMOUNT OF MASK ROTATION	AMOUNT OF DATA ROTATION
11C EXTRACT T	LITERAL IN 11C	NO ROTATION	DETERMINED BY M11 ← M7
3F NORMALIZE X	23	23	23
5D SHIFT X&Y LEFT	23	24-1=(23)	24-1=(23)
5D SHIFT X&Y RIGHT	23	NO ROTATION	1
10C SHIFT T LEFT	24-LIT	24-LIT	24-LIT
10C ROTATE T LEFT	24	NO ROTATION	24-LIT
7C READ TWS-	LIT	NO ROTATION	VALUE OF BBA
7C READ TWS+	LIT	NO ROTATION	LIT+BBA (LS 5 BITS)
7C READ TWS+ (CONSOLE)	24	NO ROTATION	24+BBA (LS 5 BITS)
7C WRITE TWS-	LIT	5 LSB BBA	5 LSB BBA
7C WRITE TWS+	LIT	LIT+5 LSB BBA	LIT3
7C WRITE TWS+(CONSOLE)	24	24+5 LSB BBA	24+ 5 LSB BBA
4D SHIFT X OR Y LEFT	24-LIT	24-LIT	24-LIT
4D SHIFT X OR Y RIGHT	24-LIT	NO ROTATION	LIT
4D ROTATE X OR Y LEFT	24	NO ROTATION	24-LIT
4D ROTATE X OR Y RIGHT	24	NO ROTATION	LIT
7D EXCHANGED	24	NO ROTATION	NO ROTATION

Fig. V-17 ROTATION CONTROL AND MASK VALUES

REMOVAL AND REPLACEMENT

Due to electrical or mechanical failures in the processor chassis, it may become necessary to remove sub assemblies within the processor for repair or replacement. This will necessitate the utilization of certain procedures to accomplish these tasks for each sub assembly that has to be removed. The procedures for the removal and replacement of all sub assemblies are listed in the following paragraphs.

S MEMORY PROCESSOR CONSOLE

The console contains all of the necessary hardware (switches, lamps, buttons, etc., for processor operation. It also includes the Tape Cassette for MTR operation. The console is mounted to the processor chassis by hinges attached to the right hand side and is held closed by magnetic latches mounted on the left hand side of the console.

The console will open very easily by exerting a slight forward pressure to the back left side of the console. The console will swing open in a left to right arc and present easy access to any cable, switch or indicator L.E.D that needs to be removed.

CONSOLE INDICATOR L.E.Ds

The indicator lamps are mounted on a separate printed-circuit board. If any lamp is defective and needs to be replaced, it is necessary to remove this printed circuit board from the console so that the necessary replacement can be made.

Each L.E.D is slightly larger than the hole into which it is mounted and presents enough pressure to insure an adequate bonding to the console without the use of screws. Consequently, only a slight amount of pressure need be applied to the printed circuit board at various locations to remove the printed circuit board from contact with the console.

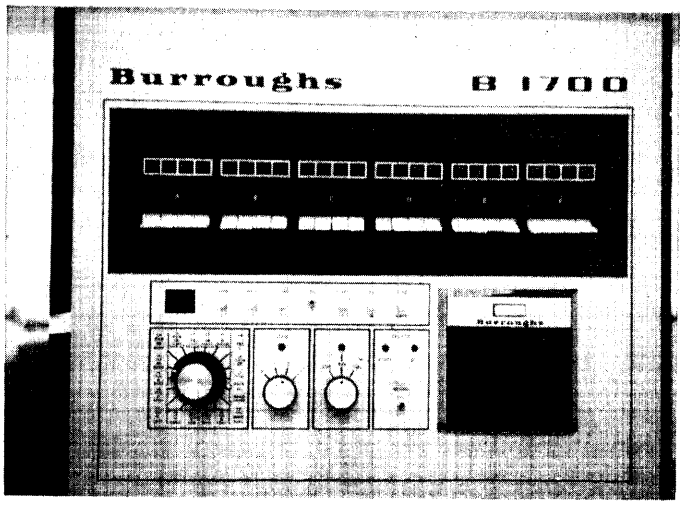


Fig. V-18 B1700 CONSOLE

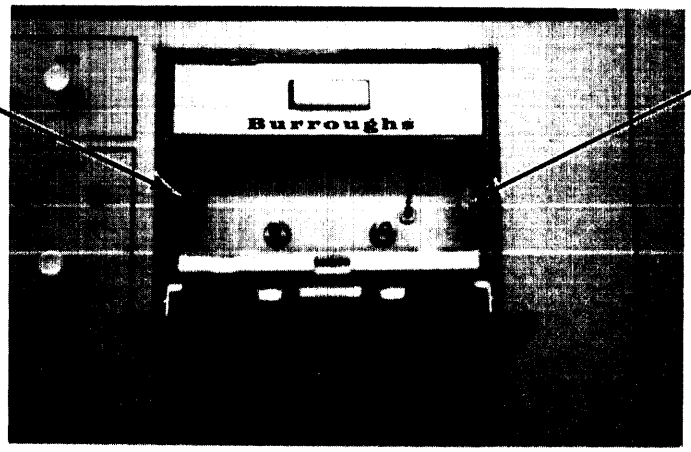


Fig. V-19 B1700 CASSETTE

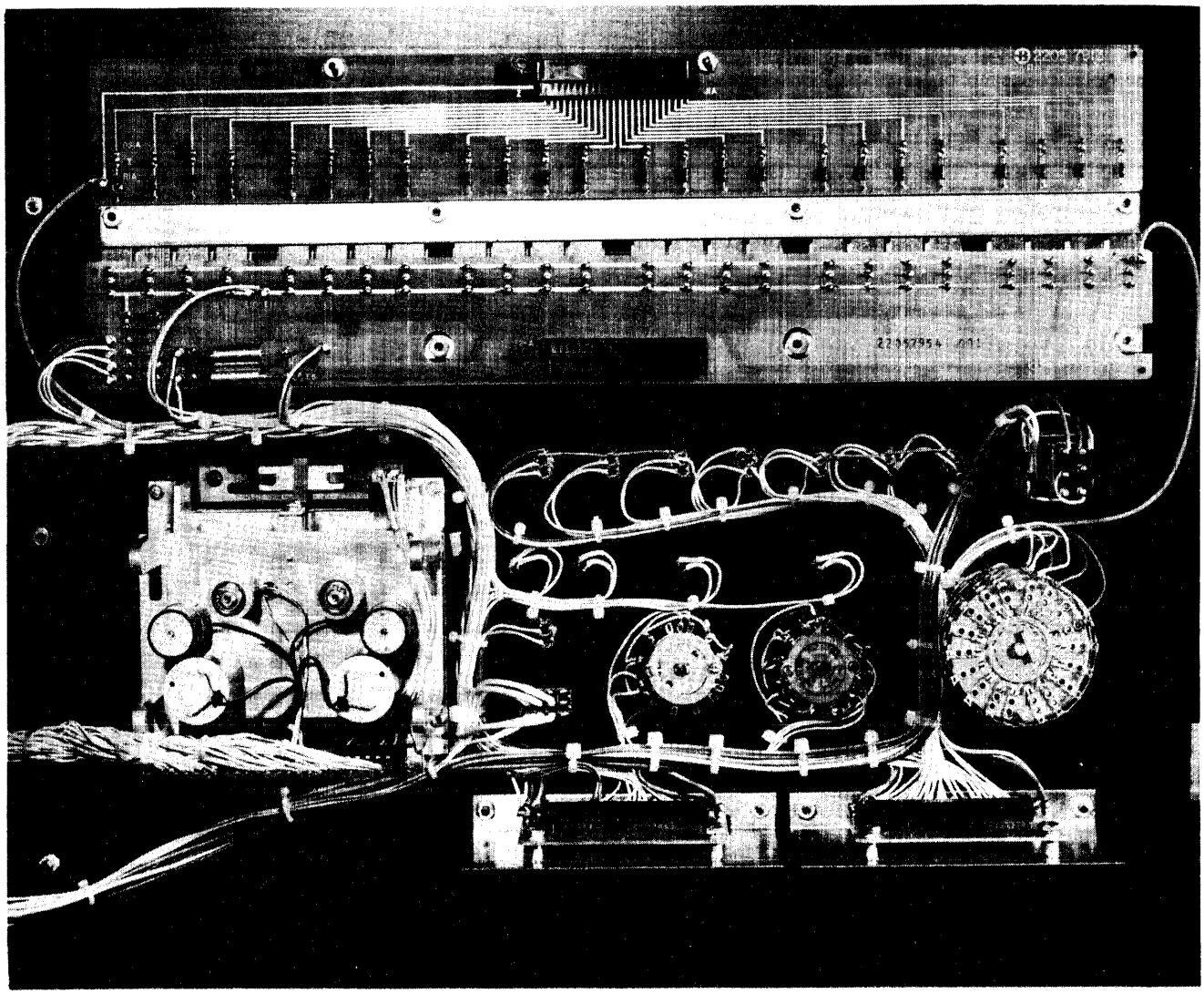


Fig. V-20 CONSOLE WIRING

The recommended procedure for removal and replacement of a LED is as follows:

1. Open the processor console
2. Remove the indicator LED Cable
3. Remove the printed circuit board that contains the twenty-four (24) LEDs.
4. Unsolder the defective LED.
5. Observing the polarity of the LED, install the new LED and reassemble the console by reversing the order of the first three (3) instructions.

NOTE: The polarity of the LED can be determined by looking at its case. The flat side denotes the cathode element whose lead is soldered to the etching that connects to the resistor in the circuit. See Figure V-22 for the circuit board schematic.

CONSOLE SWITCHES

The twenty-four (24) console switches that correspond to the twenty-four (24) Indicator LEDs are mounted on a separate printed circuit board. If any switch is defective and needs to be replaced, it is necessary to remove this printed circuit board from the console so that the necessary replacement can be made. The recommend procedure for removal and replacement of a console switch is as follows:

1. Open the processor console.
2. Remove the indicator LED cable.
3. Remove the twenty-four (24) console switch cable.
4. Remove the eight (8) retaining nuts (use a 1/4" nut driver of socket) that mount the printed circuit board to the console.
5. Remove the metal retaining bars.
6. Remove the printed circuit board.
7. Unsolder the defective switch.
8. Install a new console switch by reversing the order of the previous seven (7) instructions. See Figure V-22 for the console switch schematic.

S-MEMORY PROCESSOR BACKPLANE. REPLACEMENT PROCEDURE

1. Disconnect all cables from the logic cards in the processor chassis.
2. Remove all logic and memory cards from the processor chassis and carefully store them aside to prevent them from being damaged.
3. Unsolder the Special Backplane Power Wiring that routes along the center of the processor backplane. Label each wire for easy identification when the backplane is either replaced or reinstalled.
4. Remove the thirty-six (36) screws at the top and bottom of the backplane. The backplane is now ready to be removed from the processor chassis.
5. Replacement or reinstallation of the processor backplane is accomplished by reversing the order of the previous four (4) steps. Refer to Steps 1-6 for the wire list location for the Special Backplane Power wiring.

Special Backplane Power Wiring

Step 1. +23 Volts use No. 20 gauge wire. Red recommended.

TB2-1	to	YD0A	1
YD0A	to	YD3A	2
TB2-2	to	YD6A	1
YD6A	to	YE0A	2
TB2-3	to	YE3A	1
YE3A	to	YE6A	2
TB2-4	to	YF0A	1
YF0A	to	YF3A	2

Step 2. +19 Volts use No. 20 gauge wire. Black recommended.

TB1-1	to	YD1A	1
YD1A	to	YD4A	2
TB1-2	to	YD7A	1
YD7A	to	YE1A	2
TB1-3	to	YE4A	1
YE4A	to	YE7A	2
TB1-4	to	YF1A	1
YF1A	to	YF4A	2

Step 3. -5 Volts use No. 20 gauge wire. Brown recommended.

TB4-1	to	XD0Z	1
ZD0Z	to	XD3Z	2
TB4-2	to	XD6Z	1
XD6Z	to	XE0Z	2
TB4-3	to	XE3Z	1
XE3Z	to	XE6Z	2
TB4-4	to	XF0Z	1
XF0Z	to	XF3Z	2

Step 4. +4.75 Volts use No. 26 gauge wire.

YA4P to XA4A 1

Step 5. -12 Volts (NEG12VS0) use No. 26 gauge wire

XC6Z to -12 Volt Bus.

Step 6. Real Time Clock - Use No. 20 gauge wire. Brown recommended.

The two wires are to be twisted together.

(60HRETK0)	XC3Z	to	T1-9	(24 Volt Chassis)
(60HZINK0)	XC4Z	to	TB1-8	(24 Volt Chassis)

CASSETTE REMOVAL AND REPLACEMENT

In order to remove the Tape Cassette from the processor console, the following procedure is recommended.

1. Remove power from the Cassette by placing the Cassette on/off switch in the OFF position.
2. Push the white access button the the Tape Cassette chassis to extend the tape cassette for removal. (Use enough pressure on the white button to allow for full extension of the tape.)
3. Remove the right skin (as you face the console) of the processor cabinet.
4. Disconnect the power cable that is connected at the top rear sector of the cassette chassis. See Figure V-20.
5. Locate the two (2) mounting latches that hold the cassette chassis in place. They are at either side of the chassis as you face the console and have slots for access by a medium size screwdriver. See Figure V-19.
6. Using the correct screwdriver, rotate the mounting latches (at least a 1/4 turn) until the cassette chassis free. The cassette can now be removed from the processor console.
7. Remove the cassette by pulling the cassette chassis forward from the processor console.
8. Replacement or reinstallation of the Tape Cassette is accomplished by reversing the order of the previous seven (7) instructions.

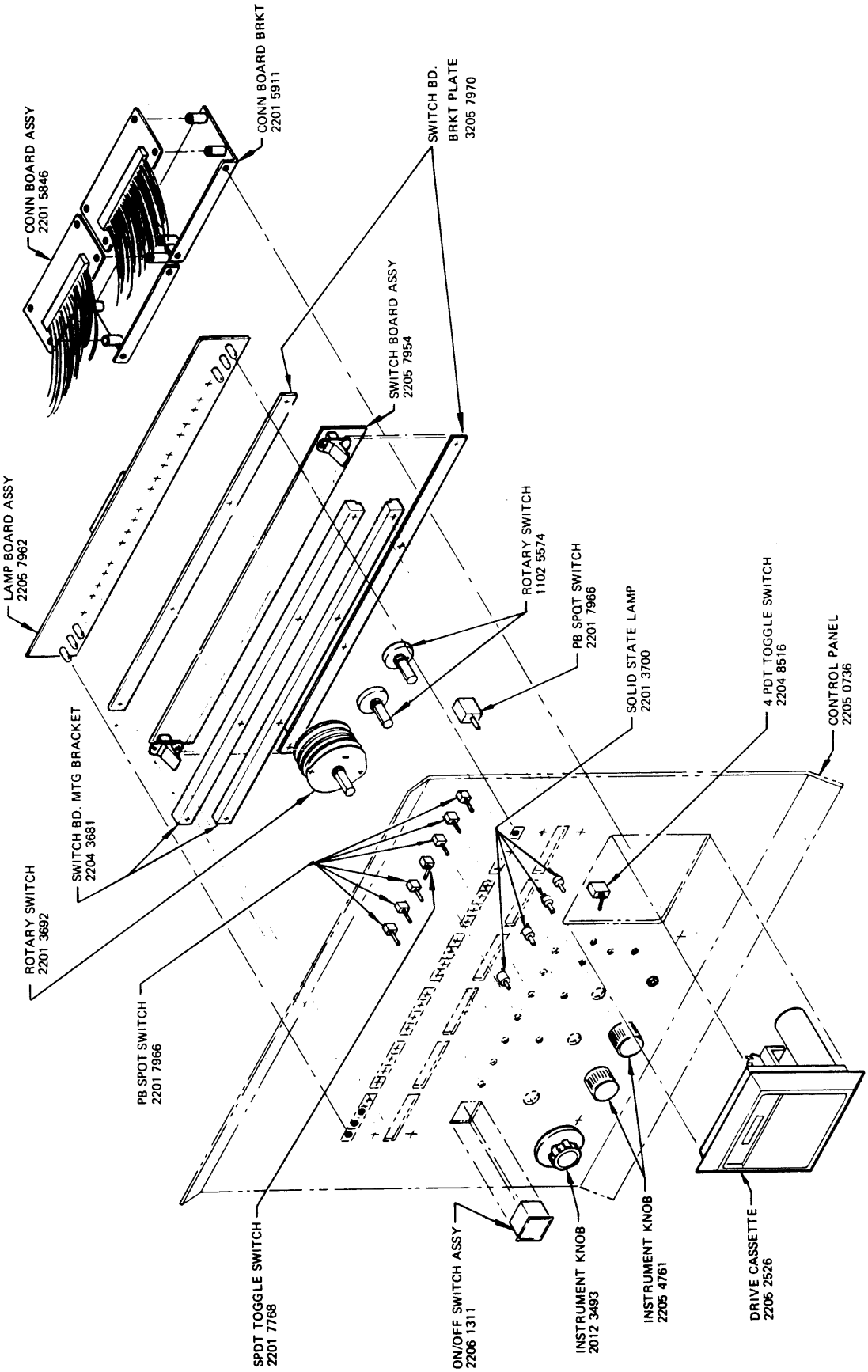
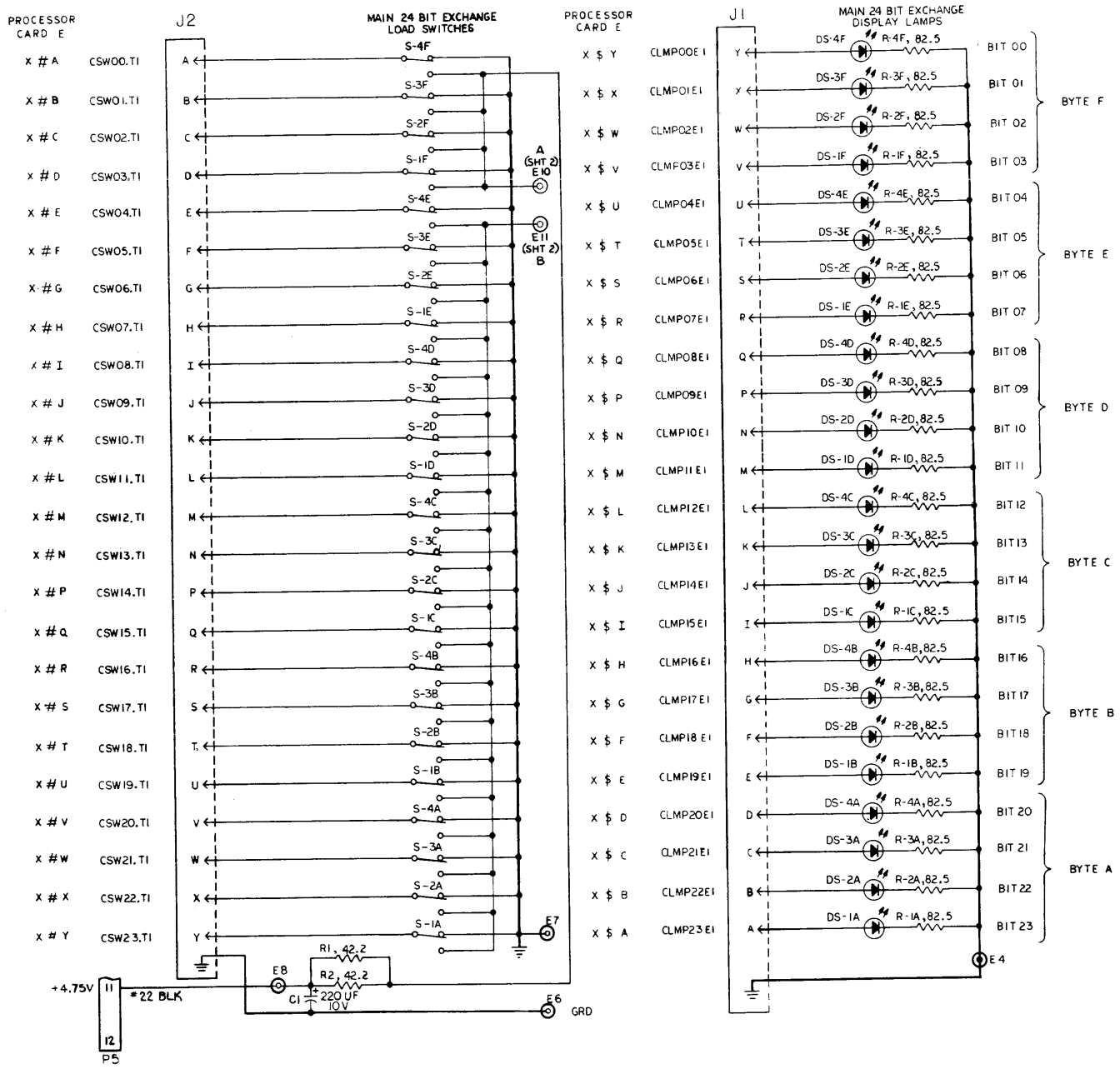


Fig. V-21 CONTROL PANEL ASSEMBLY



3. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE 1/4W ±2%. RESISTOR VALUES ARE IN OHMS.
2. CAPACITOR VALUES ARE IN MICROFARADS.
1. UNLESS OTHERWISE SPECIFIED, ALL WIRES ARE #22 WHITE, EXCEPT FOR CONNECTIONS ON THE SAME SWITCH WHICH ARE #22 BUS WIRE.

NOTES:

Fig. V-22 SCHEM-PNL CONTROL

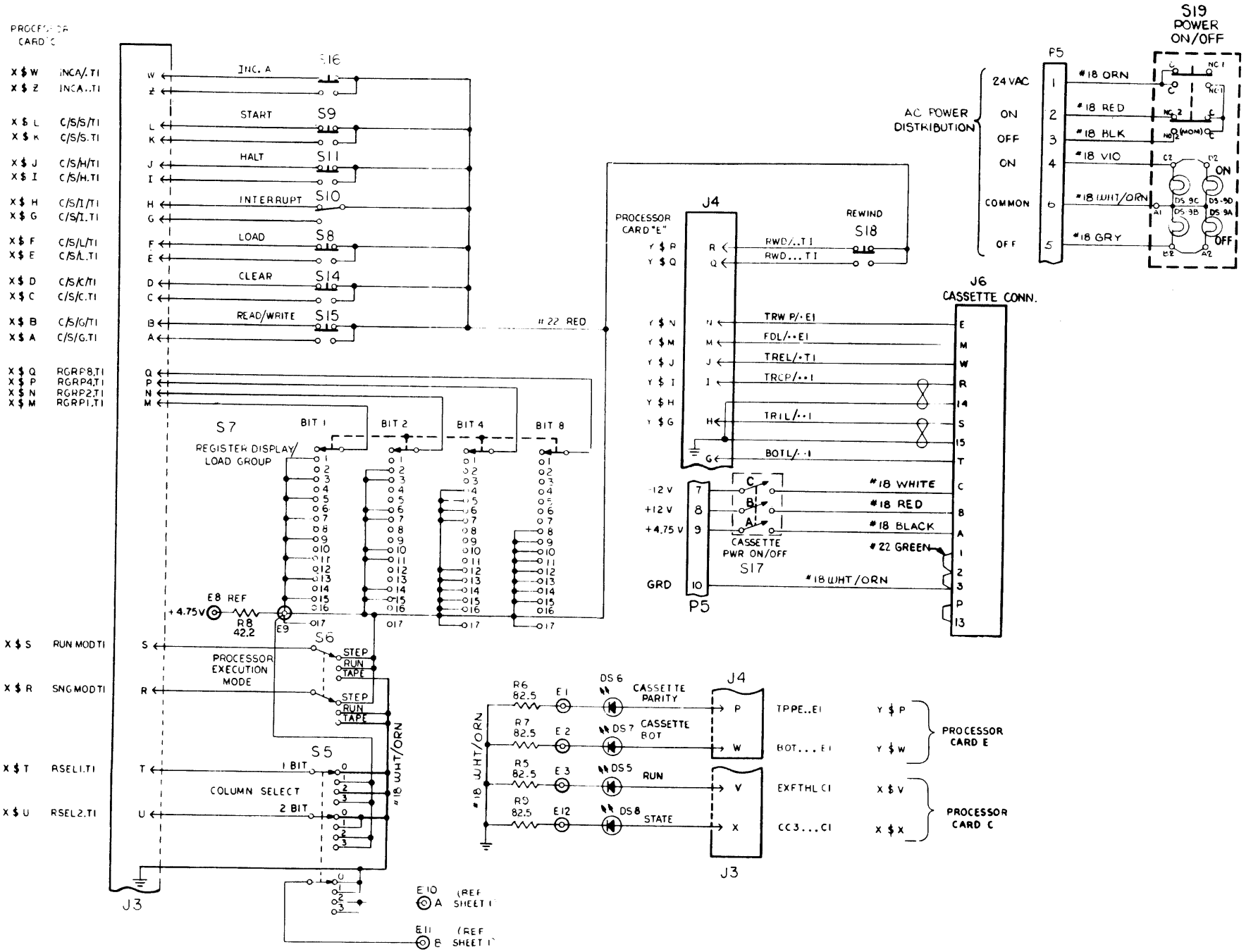


Fig. V-23 SCHEM-PNL CONTROL

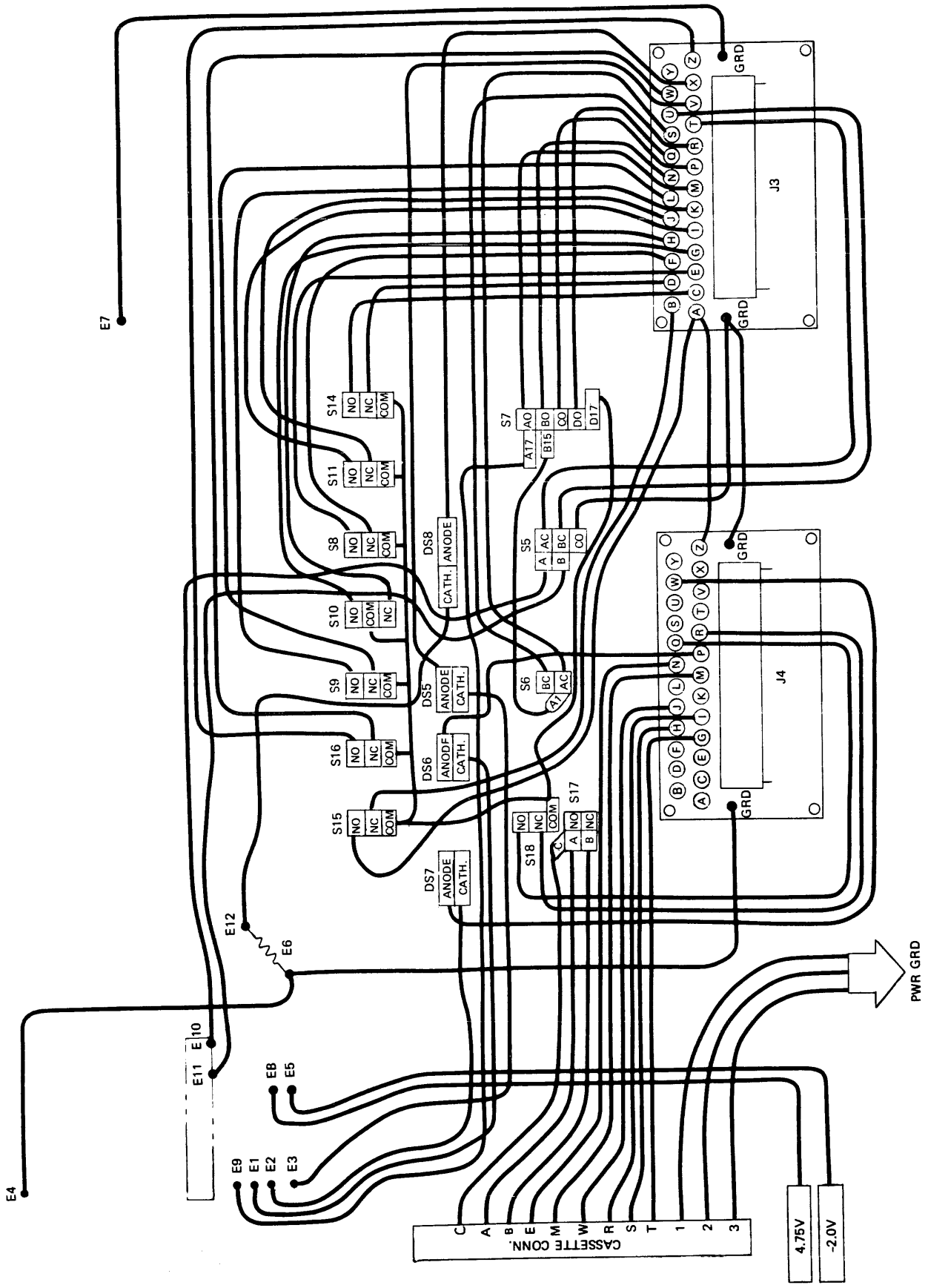

E7
E4
E12
E6
E10
E11
E8
E5
E9
E1
E2
E3
J3
J4
GRD
S14
S11
S8
S10
S9
S16
S15
S7
S5
S6
S17
S18
DS8
DS5
DS6
DS7
ANODE
CATH.
CASSETTE CONN.
4.75V
-2.0V
PWR GRD

Fig. V-24

MEMORY

The following items will be covered for memory:

1. Preventive Maintenance
2. Card Location
3. Test Points
4. Memory Timing
5. Troubleshooting Procedures
6. Memory Wave Shapes
7. Interface Signals

PREVENTIVE MAINTENANCE

The memory has no preventive maintenance other than memory voltage. These should be verified every six months. See Section IV for actual voltage settings and adjustment procedures if needed.

CARD LOCATION

The memory storage cards are located within the S-Memory Processor Card Housing. Since some of the processor cards contain the control logic for certain memory functions, the complete card location for the S-Memory Processor Card Housing is shown in Figure V-25.

The memory control logic is contained on the following cards.

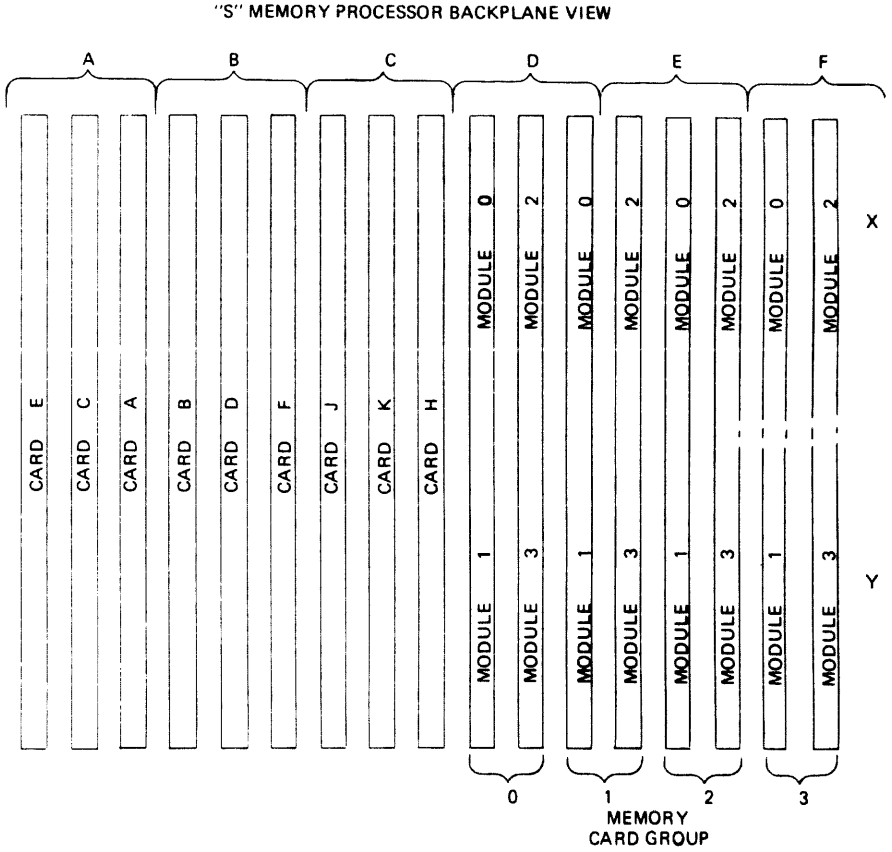


Fig. V-25 "S" MEMORY PROCESSOR BACKPLANE VIEW

A. Card C – Memory Refresh Logic
B. Card H – Memory Addressing
C. Card J – Data Read Logic
D. Card K – Data Write and Memory Timing Logic

These four cards contain the control logic that more directly affect the memory operation. Other cards may contain logic that generate useful information that these four cards combine into signals that are used in the memory timing cycles.

TEST POINTS

Frontplane Test Points on Card H

Name	Pin
FGPAE.HI	$XY
FGPALTHI	$ZY
M2KBAIHI	$SY
M2MODIHI	$TY
M3KBAIHI	$QY
M3MODIHI	$RY
MIKBAIHI	$UY
MIMODIHI	$VY
MOKBAIHI	$WY
MOMODIHI	$XY
MOD18.HI	$BY
MOD17.HI	$CY
16	$DY
15	$EY
14	$FY
13	$GY
12	$HY
11	$IY
10	$JY
09	$KY
08	$LY
07	$MY
06	$NY
MOD05.HI	$PY
TWS. . .H1	$AY

Memory Card – Backplane

	0		1	
+4.85	Vcc	AX	Vcc	+4.85
	D10X	BX	D11X	
	D12X	CX	DI3X	
		DX	Vdd Gnd	
	D14X	EX	D15X	
	D16X	FX	D17X	
	PIX	GX		
	D00X	HX	D01X	
	D02X	IX	D03X	
		JX	Vdd Gnd	
	D04X	KX	D05X	
	D06X	LX	D07X	
	POX	MX	A17X	
	A18X1	NX	A17X	
	A18X	PX		
		QX	Vdd Gnd	
		RX		
	A15X	SX	A16X	
	A13X	TX	A14X	
	A11X	UX	A12X	
	A9X	VX	A10X	
		WX	Vdd Gnd	
	A7X	XX	A8X	
	A5X	YX	A6X	
-5V		ZX		
	0		1	
+23	Vbb	AY	Vss + 19V	
	D10Y	BY	D11Y	
	D12Y	CY	D13Y	
		DY	Vdd Gnd	
	D14Y	EY	D15Y	
	D16Y	FY	D17Y	
	PIY	GY		
	D00Y	HY	D01Y	
	D02Y	IY	D03Y	
	*Ref 2	JY	Vdd Gnd	
	D04Y	KY	D05Y	
	D06Y	LY	D07Y	
	POY	MY	A17Y	
	A18Y	NY	A17Y	
	A18Y	PY	WE	
	PRE	OY	Vdd Gnd	
	CE	RY	REF	
	A15Y	SY	A16Y	
	A13Y	TY	A14Y	
	A11Y	UY	A12Y	
	A9Y	VY	A10Y	
		WY	Vdd Gnd	
	A7Y	XY	A8Y	
	A5Y	YY	A6Y	
-2V	Vee	ZY	Vee	-2

*Refresh 2: This is the backplane pin used for refreshing the memory.

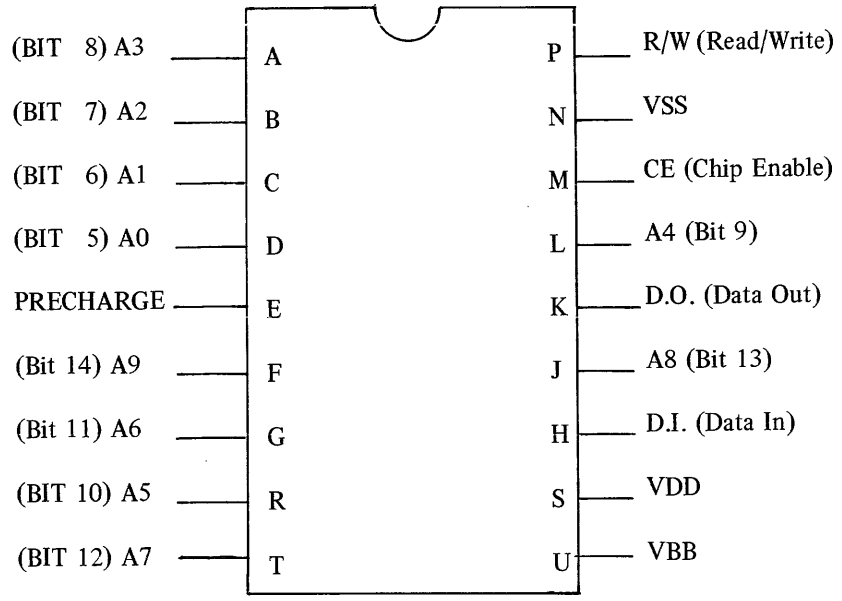


Fig. V-26 DYNAMIC STORAGE CHIP

MEMORY TIMING

Memory timing is developed by the OCCURRENCE of one of four events. They are:

1. Memory Refresh
2. M Fetch (the fetch of a micro)
3. 7C Micro (Read/Write Memory)
4. Console Read/Write

These four events will cause the generation of signal MSTARTFO. A write 7C micro and console write also causes the generation of signal SWRITEFO which is used only during a write operation.

MSTARTFO, through a network of delay lines, generates the signal PRECH.KO which precharges the memory chips prior to enabling them. MSTARTFO also generates CENABLKO which is delayed longer than PRECH.KO but must come true before PRECH.KO goes false. See Figure V-27.

SWRITEFO generates RD/WT.KO which when true indicates that a write operation is taking place and when false, a read operation is taking plce. SWRITEFO also extends CENABLKO to keep the memory chips enabled until the write operation is complete. This is because a write operation involves a read operation prior to writing data and, therefore, no writing into memory occurs until the latter part of a 7C micro.

COMPONENTS THAT EFFECT TIMING

Certain components on processor card K directly affect the memory timing. Whenever any of these parts are found defective and replaced, the timing of the memory must be checked. If adjustment is necessary see Section IV. The components that have direct effect on the memory clocks timing are the following:

Location	Description
K5	Dual J-K Flip Flop
J5	Dual Buffer
J7	Dual Buffer
J9	Dual Buffer
K9	Dual Buffer
K7	Dual Inverter
L3	Dual Inverter
J4	100 ns Delay Line
J6	50 ns Delay Line
K3	100 ns Delay Line
K6	100 ns Delay Line
K8	100 ns Delay Line

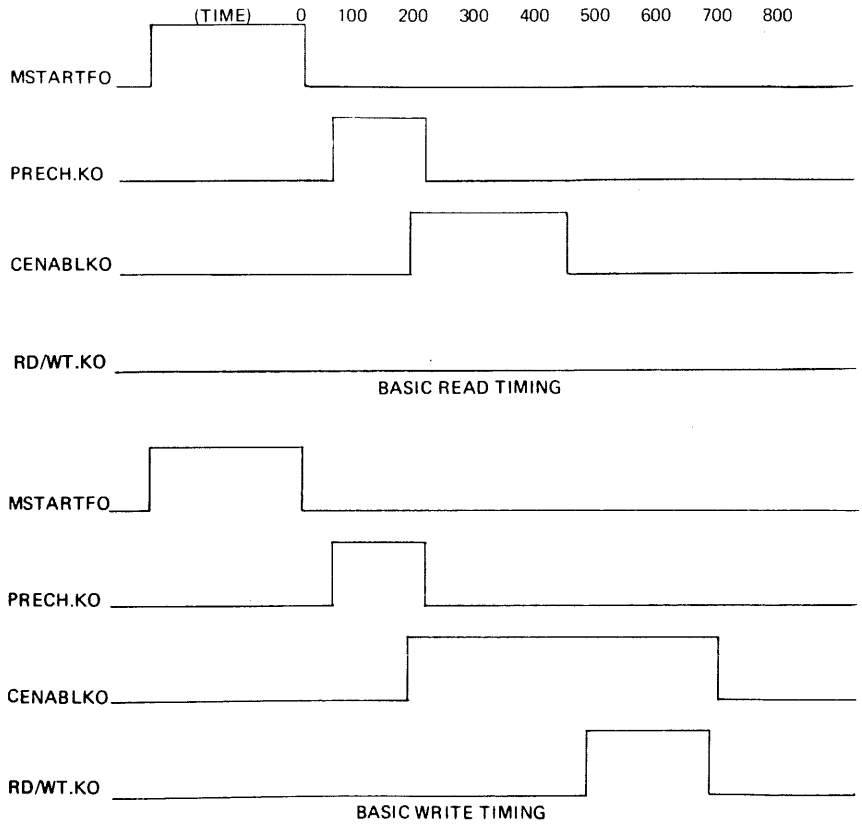


Fig. V-27 SIMPLIFIED BASE MEMORY TIMING

TROUBLESHOOTING PROCEDURES

Prior to troubleshooting any section of the system, certain precautions should be observed. These precautions could save time and needless effort in pursuing any problem. Take the time and look for the items that are frequently overlooked when starting to troubleshoot any problem. The basic ones are as follows:

1. All cables should be secure.
2. The jumper chips on cards H and E are correct (see Section VI).
3. Logic voltages are correct.
4. Memory voltages are correct.
5. Memory timing is correct.

If any of these items are in error, correct the problem and then retry the program that indicated a fault and determine if it is functioning correctly.

If all of these items are correct, run the processor tests to see if it is functioning correctly.

MEMORY FAILURES

After it has been determined that there is a failure in the Memory, the problem should present itself in one of two forms. They are:

1. Solid failure.
2. Random or intermittent failure.

SOLID FAILURE

A failure that constantly exhibits itself in one or more locations in memory. Some of the more common indications are:

1. Unable to write data correctly.
2. Unable to read data correctly.

Memory Test 2207 1823 will isolate the failing address(s) and data pattern(s).

RANDOM FAILURE

Failures of this type do not lend themselves to exact explanation. They are intermittent and can take the form of a solid failure only to disappear and reappear in random fashion.

Since it is very hard to isolate a failure of this type, the following procedure is recommended to determine what the cause may be.

1. Check the Refresh Logic and Refresh addressing.
2. Exchange storage boards to determine if the problem can be isolated to one board.
3. Check Memory timing. See Section IV.

If the problem cannot be isolated to a board, then the problem will more than likely be of a control or voltage nature. DO NOT overlook the fact that the memory can be correct but the Interface lines to the processor could be faulty.

CONSOLE TROUBLESHOOTING

A failure may be isolated by using the console. All console read or writes will be 14 bits in length starting at the bit address selected by MAR(A). If any bit pattern selected is changed after performing a write, then the suspected bit address should be investigated.

Example: Write 24 zeroes into memory starting at any bit address.

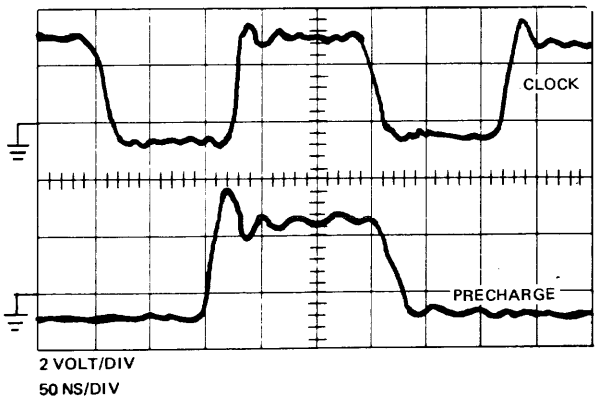
1. Set the Bit address on the Console switches and load it into MAR(A) via the load button.
2. Select Write and write into memory via Read/Write button.
3. Select Read and read from memory via Read/Write button.
4. The twenty-four (24) bits displayed should be zeroes (0). If any bit is a one (1), then add sequentially from right to left with the selected bit address as the reference. This will indicate the failing bit address.

There are other methods of console troubleshooting but they are usually developed through experience. The foregoing example is one of these methods.

MEMORY WAVE SHAPES

Memory wave shapes can be instrumental in maintaining and trouble shooting the memory. These waveshapes show a dynamic relationship between the memory timing signals. For actual timing and adjustment of memory see Section IV. Figure V-27 shows an overall timing diagram while Figure V-28 through Figure V-33 show actual dynamic wave shapes.

Figure V-28 shows the relationship between the timing signals CLK4. . KO and PRECH. KO. The oscilloscope settings are such as to obtain 2 volts/cm of vertical deflection and 50 nanoseconds/cm of horizontal timing. The oscilloscope uses MSTARTFO as its trigger.

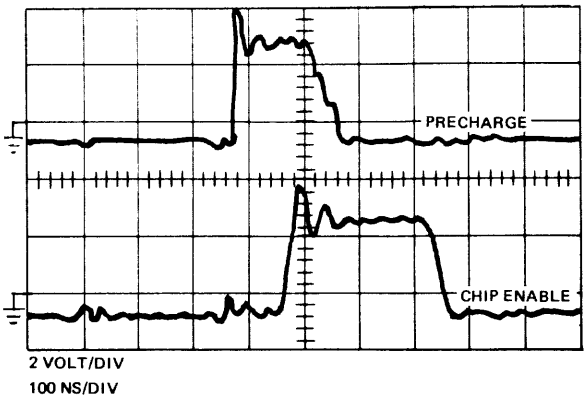


Vertical
2 Volts/Division
Horizontal
50nsec/division

Channel 1
Card K OXX

Channel 2
Card K OQY

Fig. V-28 PRECHARGE/CLOCK



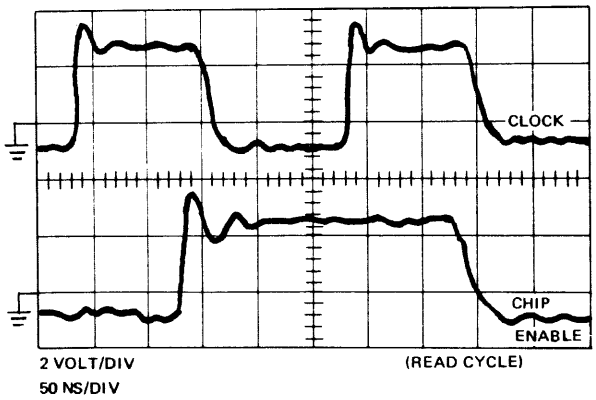
Vertical
2 Volts/Division
Horizontal
100nsec/division

Channel 1
Card K OQY

Channel 2
Card K ORY

Fig. V-29 PRECHARGE/CHIP ENABLE

Figure V-29 shows the relationship between the memory timing signals PRECH. KO and CENABLKO. The oscilloscope settings are such as to obtain 2 volts/cm of vertical deflection and 100 nanoseconds/cm of horizontal timing. The oscilloscope uses MSTARTFO as its trigger.



Vertical
2 Volts/Division

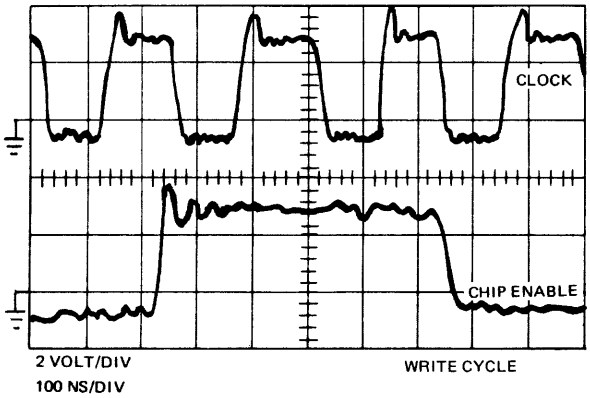
Horizontal
50nsec/Division

Channel 1
Card K OXX

Channel 2
Card K ORY

Fig. V-30 CHIP ENABLE (READ CYCLE)

Figure V-30 shows the relationship between the timing signals CLK4. . KO and CENABLKO during a Read cycle. The oscilloscope settings are such as to obtain 2 volts/cm of vertical deflection and 50 nanoseconds/cm of horizontal timing. The oscilloscope uses MSTARTFO as its trigger.



Vertical
2 Volts/Division

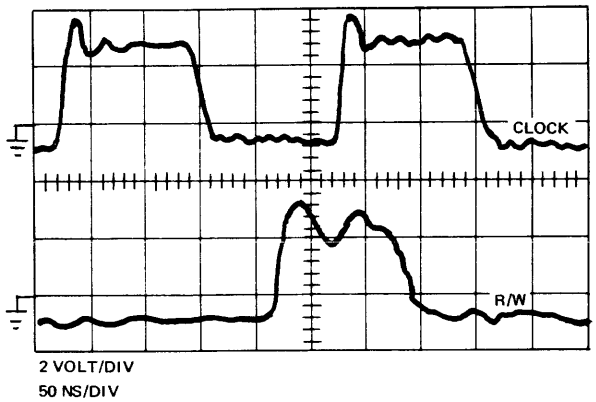
Horizontal
100 nsec/Division

Channel 1
Card K OXX

Channel 2
Card K ORY

Fig. V-31 CHIP ENABLE (WRITE CYCLE)

Figure V-31 shows the relationship between the timing signals CLK4. . KO and CENABLKO during a write 7C Micro. The oscilloscope setting are such as to obtain 2 volts/cm of vertical deflection and 100 nonoseconds/cm of horizontal timing. The oscilloscopes uses SWRITEFO as its trigger.



Vertical
2 Volts/Division

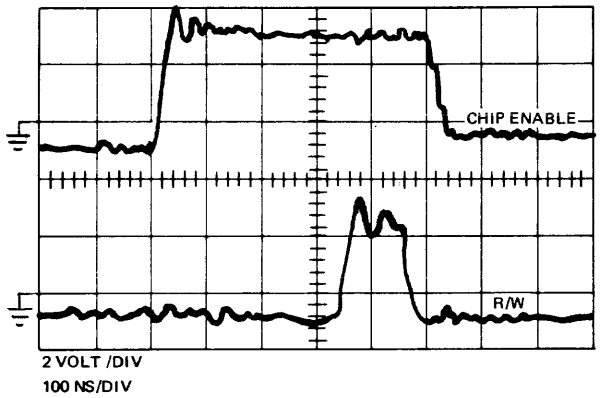
Horizontal
50nsec/Division

Channel 1
Card K OXX

Channel 2
Card K 1NY

Fig. V-32 READ/WRITE (WRITE CYCLE)

Figure V-32 shows the relationship between the timing signals CLK4. . KO and RD/WT. KO during a 7C Write micro. The oscilloscope settings are such as to obtain 2 volts/cm of vertical deflection and 50 nanoseconds/cm of horizontal timing. The oscilloscope uses SWRITEFO as its trigger.



Vertical
2 volts/Division

Horizontal
100nsec/Division

Channel 1
Card K ORY

Channel 2
Card K 1NY

Fig. V-33 CHIP ENABLE – READ/WRITE (WRITE CYCLE)

Figure V-33 shows the relationship between the timing signals CENABLKO and RD/WT. KO during a 7C Write micro. The oscilloscope settings are such as to obtain 2 volts/cm of vertical deflection and 100 nonoseconds/cm of horizontal timing. The oscilloscope uses SWRITEFO as its trigger.

INTERFACE SIGNALS

Table V-3 shows the interface signals between the processor and memory.

Signal	Quantity	Direction Proc:Mem
Precharge	1	→
Cenable	1	→
Read/Write	1	→
Address	32	→
Write Data	36	→
Read Data	36	←
Refresh	1	→

INTERFACE SIGNALS
Table V-3

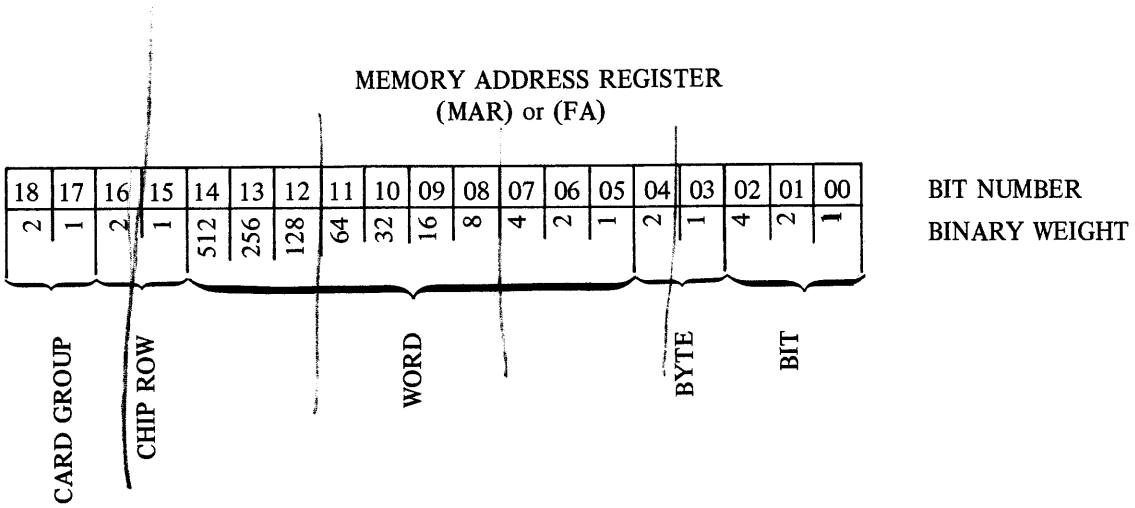


Fig. V-34 MEMORY ADDRESS REGISTER (MAR) OR (FA)

BINARY WEIGHT

Card Group	Chip Row	Word	Byte	Bit	Mar
2	8	8192	32768	262144	18
1	4	4096	16384	131072	17
0	2	2048	8192	65536	16
0	1	1024	4096	32768	15
0	0	512	2048	16384	14
0	0	256	1024	8192	13
0	0	128	512	4096	12
0	0	64	256	2048	11
0	0	32	128	1024	10
0	0	16	64	512	9
0	0	8	32	256	8
0	0	4	16	128	7
0	0	2	8	64	6
0	0	1	4	32	5
0	0	0	2	16	4
0	0	0	1	8	3
0	0	0	0	4	2
0	0	0	0	2	1
0	0	0	0	1	0

Fig. V-35 MEMORY ADDRESSING

POWER SUPPLY

ASSEMBLY AND DISASSEMBLY

It may be necessary at times to remove th logic power supply from the B1700 cabinet and extend it to troubleshoot a problem. When it does occur, there are certain procedures and cautions to follow for quick access and to eliminate hazards. The logic supply is shown extended in Figure V-36.

The following procedures is recommended for extension of the logic power supply.

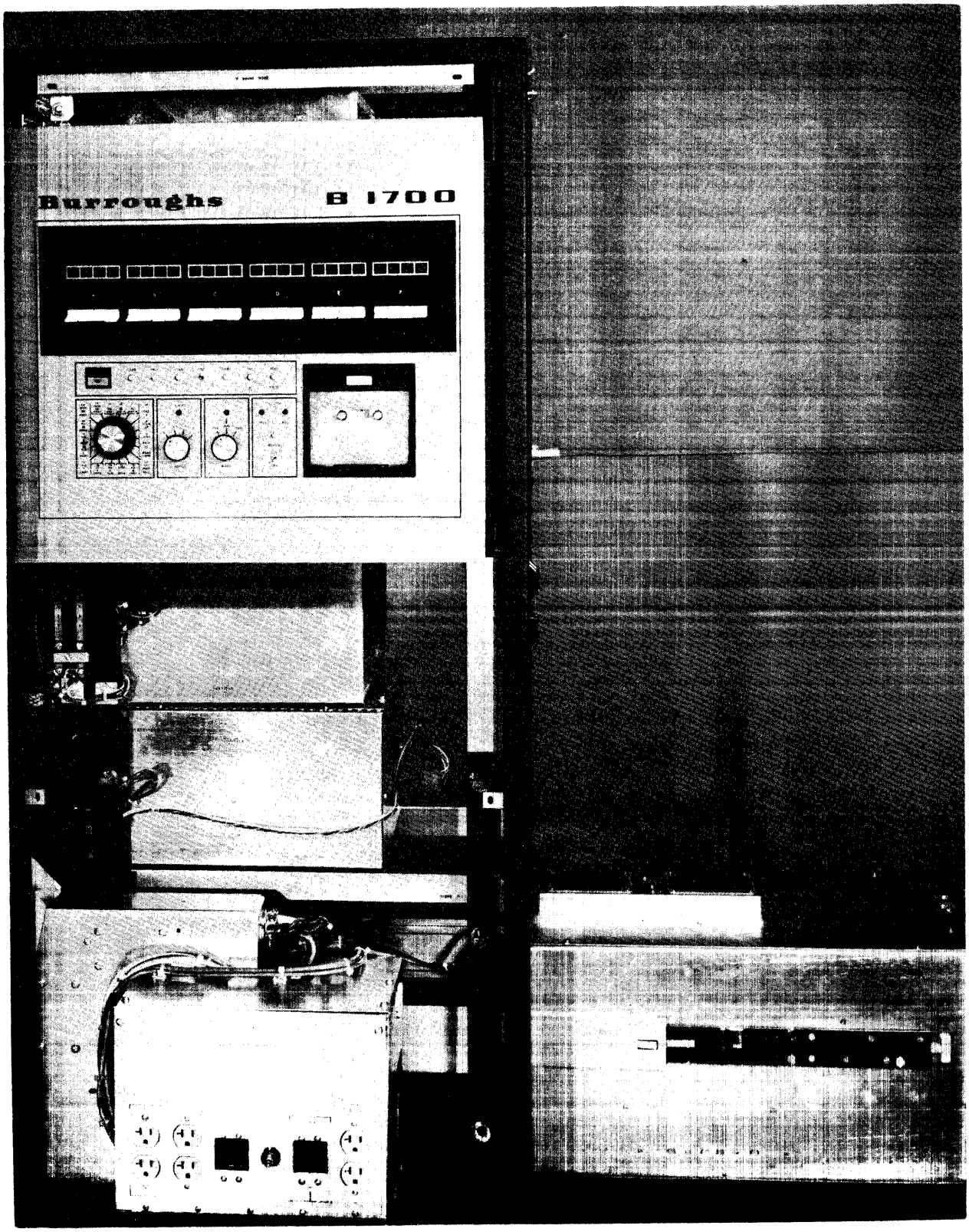


Fig. V-36 POWER SUPPLY (FRONT)

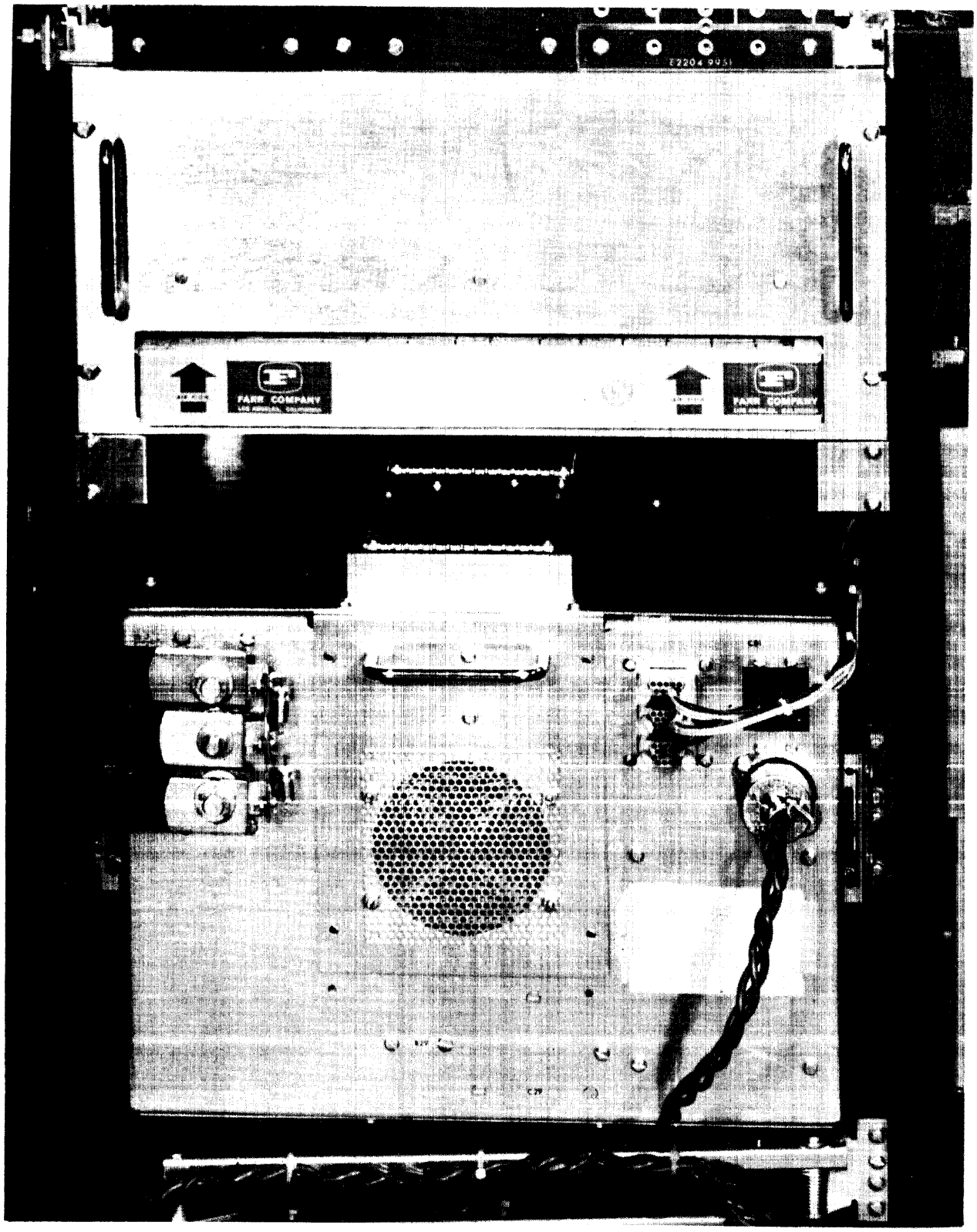


Fig. V-37 POWER SUPPLY (REAR)

CAUTION: The supply is very heavy. Putting any extra weight on it when it is extended may cause it to tip the cabinet over.

1. Remove both the right and left panels from the B1700 cabinet.
2. At the left side of the cabinet (rear of the supply), remove the bus bars (4.75V, Gnd, and -2.0V) from the power supply chassis. See Figure V-37.
3. Disconnect the J12A, J12B, and JLG connectors from the power supply chassis.
4. At the right side of the cabinet (front of the power supply), remove the eight (four on a side) screws that secure the power supply to the cabinet frame.
5. The supply can now be extended out the right side of the B1700 cabinet. Use caution when extending to insure that the weight of the supply (200 lbs.) isn't shifted too quickly on the side rails.
6. The supply can be reinstalled by reversing to order of the previous five (5) instructions.

INSTALLING THE DUMMY LOAD

After extending the logic power supply for troubleshooting, it is necessary to install a dummy load to the outputs of the supply. The dummy load is shipped with the power supply. The dummy load will allow the power supply to furnish 100 amperes through its resistance. It gets very hot and caution must be observed when it is connected and power applied. A shorting bar is normally connected between the -2.0V output and ground. The dummy load is then connected to the +4.75V output and ground. This arrangement will allow for the loading required for the -2.0V supply as well as the +4.75V supply.

The following procedure is recommended for installing the dummy load.

CAUTION: The connectors for J12A, J12B and JLG must be disconnected while using the dummy load.

1. Connect a shorting bar between the -2.0V terminal and the ground terminal on the rear of the power supply chassis.
2. Connect the dummy load between the +4.75V terminal and ground terminal on the rear of the power supply chassis.

Figure V-38 shows a top view of the power supply when its extended and the cover is removed. A view of the erectable heat sink is shown in Figure V-39.

MAINTENANCE AIDS

Figure V-40 is a block diagram of the B1700 power supply.

CAUTION: Any trouble shooting of the supply shall be done off line.

With the system running (1/2 hour or more), feel the bus bars and assure that there are no warm or hot spots especially at or near the bolted connections. If these do occur, it indicates poor electrical connection and conduction and therefore should be cleaned and retightened.

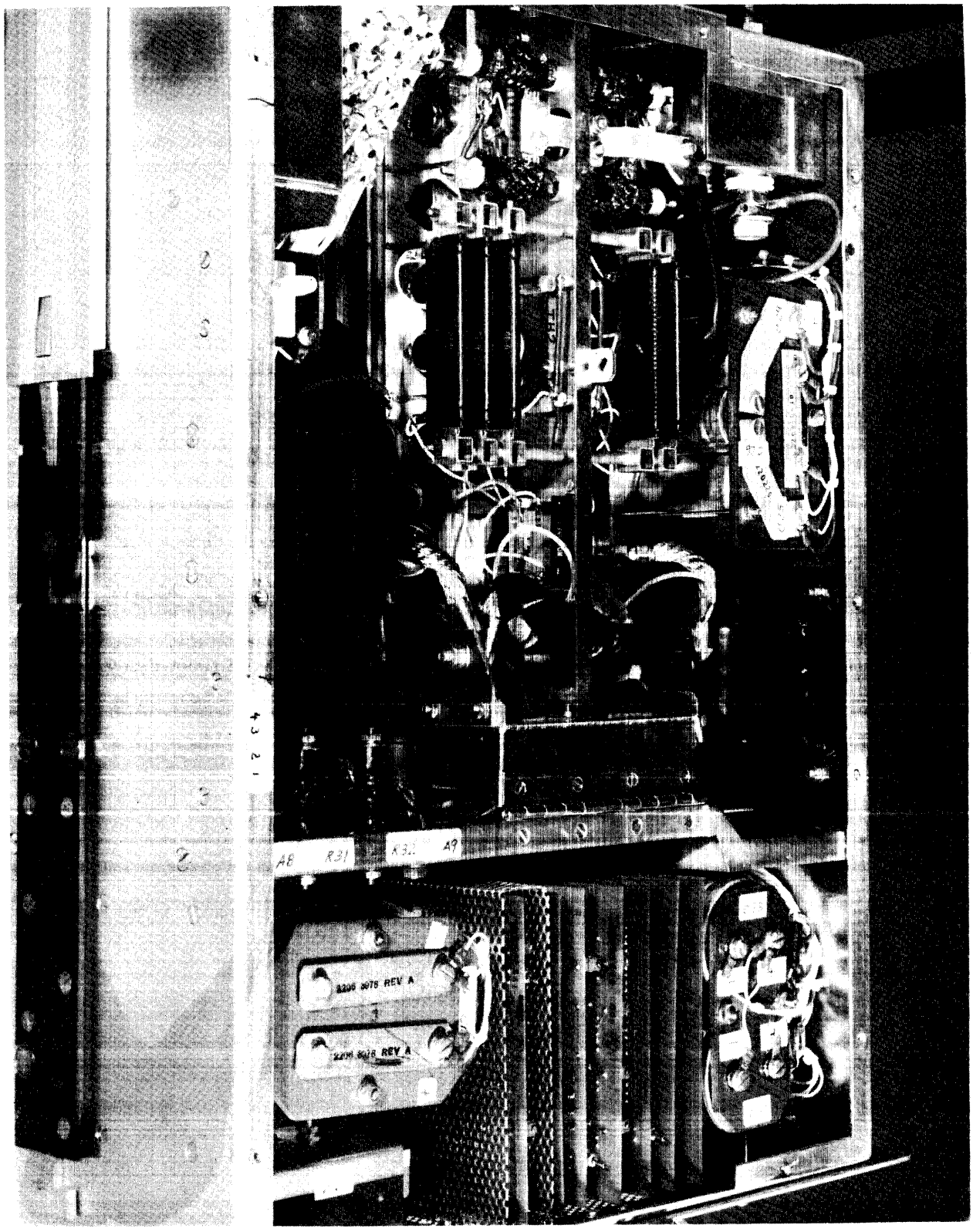


Fig. V-38

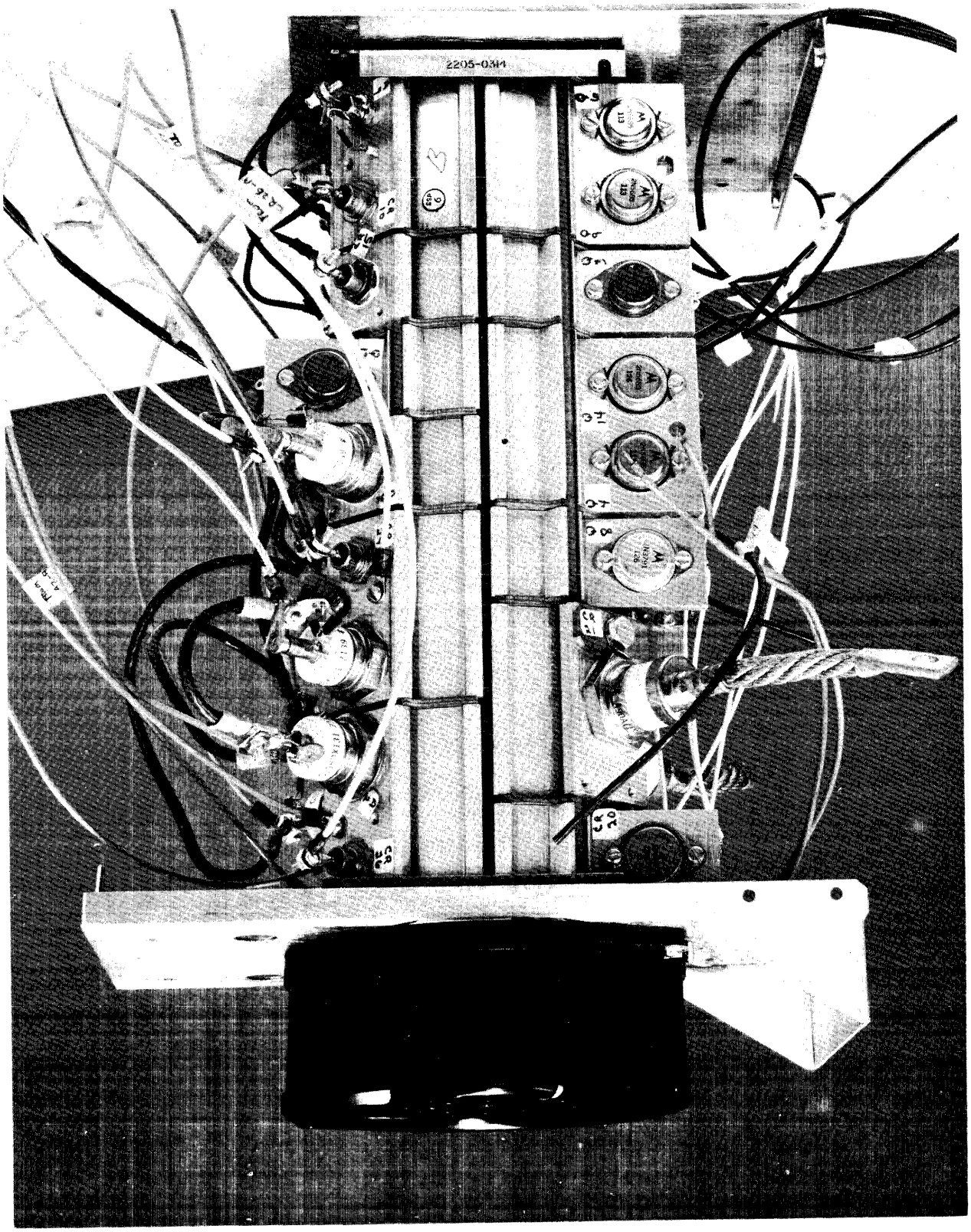


Fig. V-39

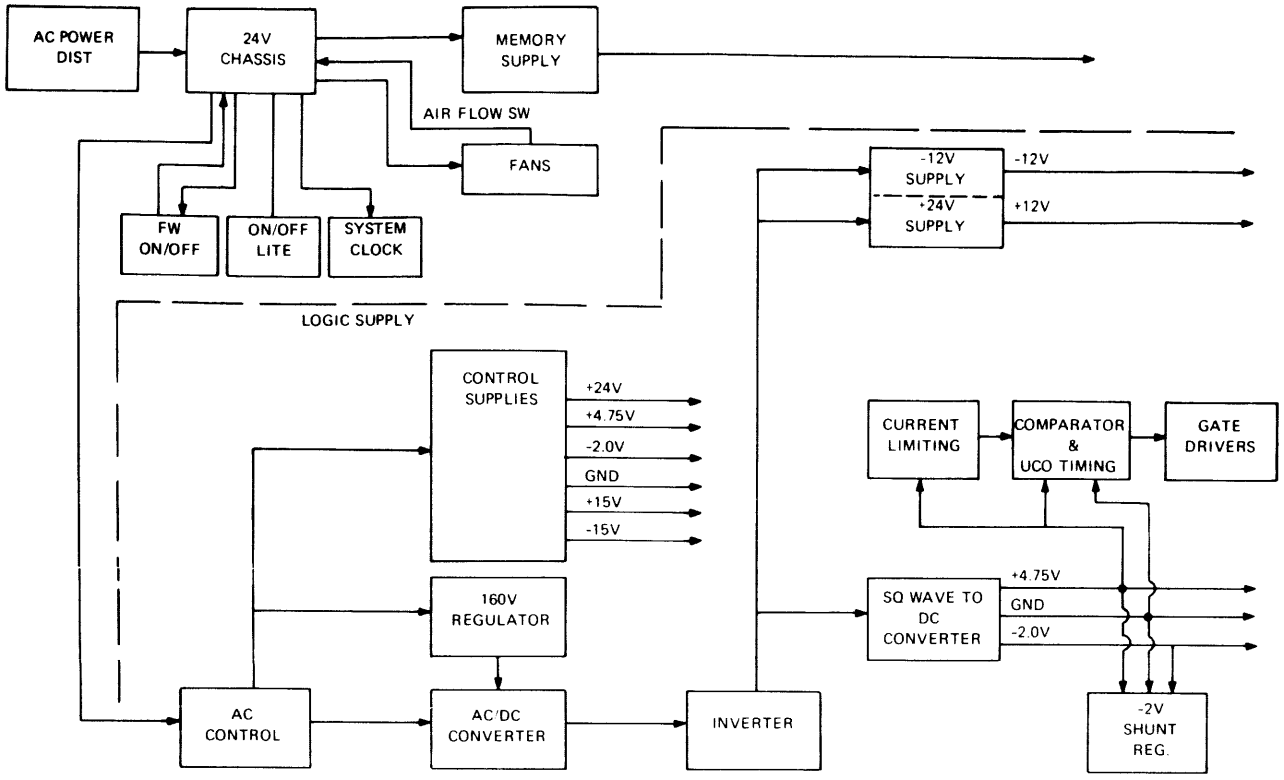


Fig. V-40 POWER SUPPLY BLOCK DIAGRAM

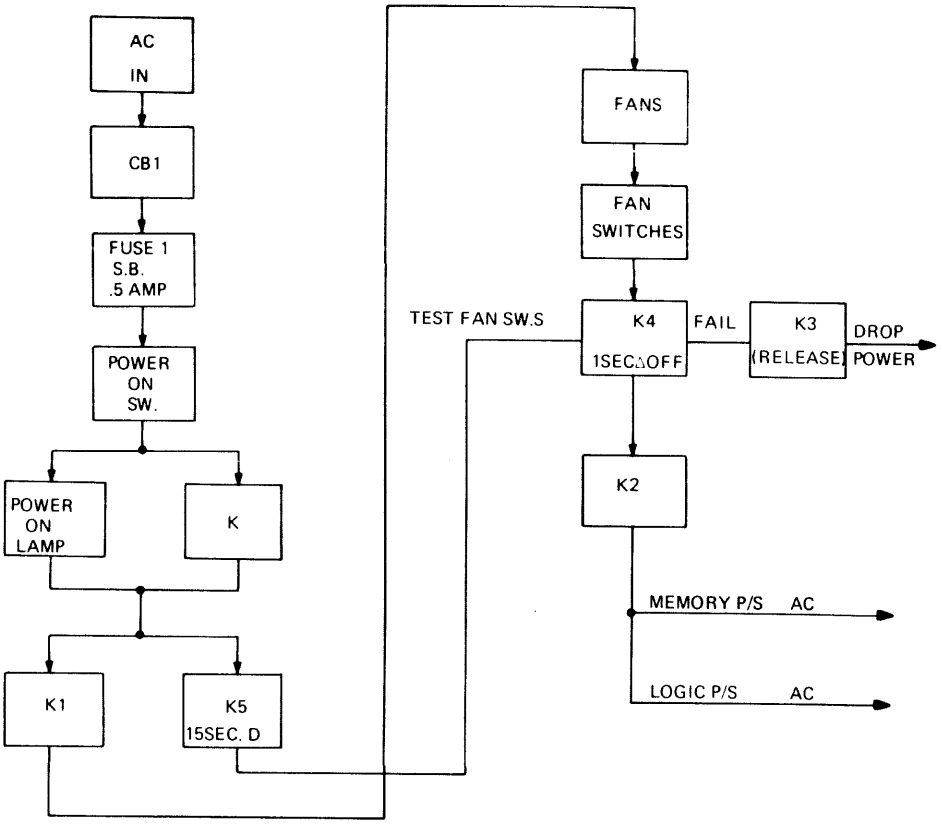


Fig. V-41 AC DISTRIBUTION FLOW

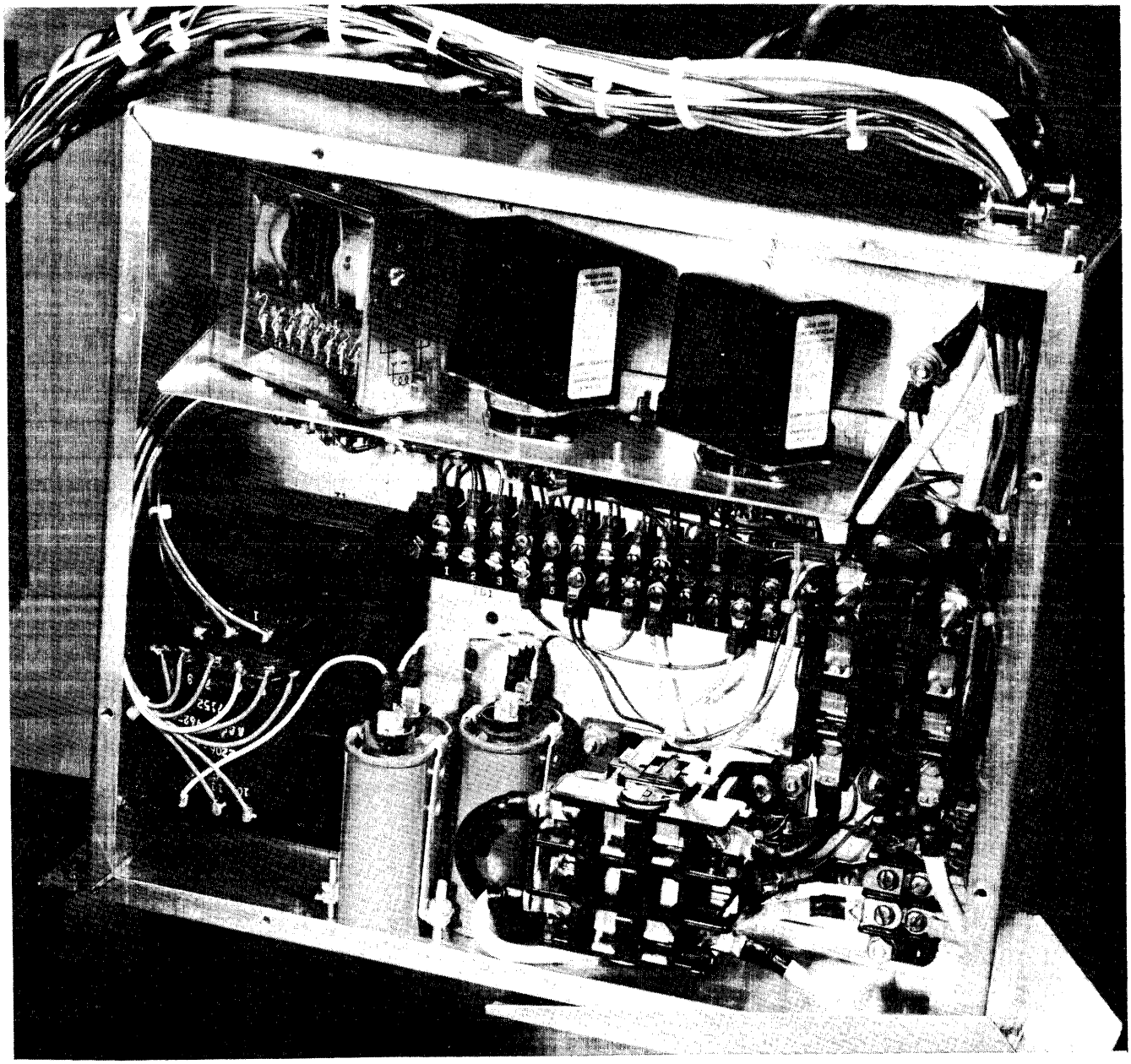


Fig. V-42 24 VOLT CHASSIS

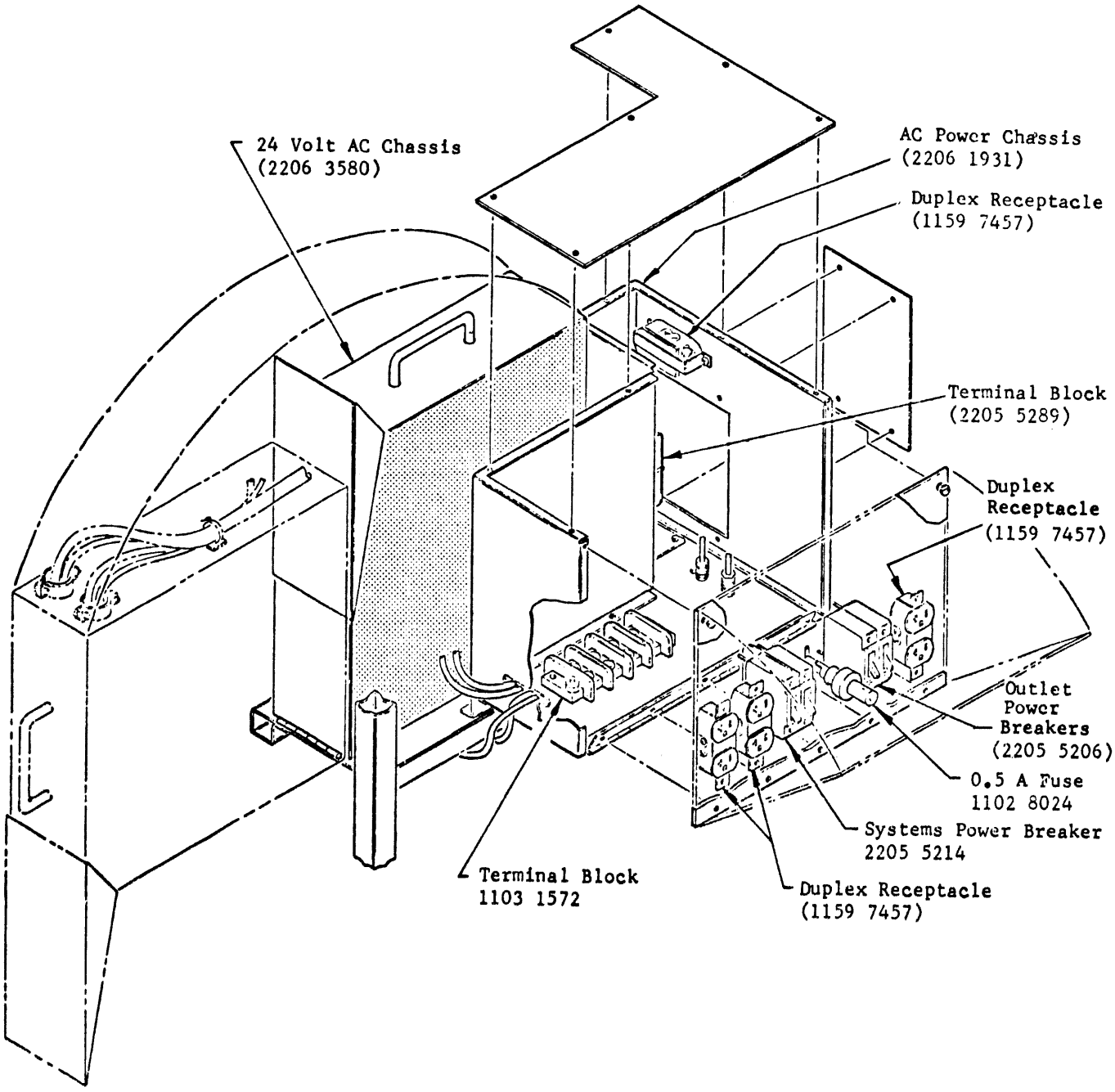


Fig. V-43 AC DISTRIBUTION BOX

POWER UP

With the CB2 and CB3 closed, 110 VAC is applied to J1 through J4. With CB1 closed, 208 VAC is applied to terminals 1 and 2 of TB3 in the AC power distribution box and also to terminals 3 and 5 of normally open K1 and to pins 2 and 3 of transformer T1 in the AC control. T1 is a step down transformer, and from terminals 5 and 6 the 24 VAC supply is developed.

When the 24 VAC is developed and the Power ON/OFF switch is in the OFF position, 24 VAC is applied to the OFF indicator through contacts 19 and 16 of K3B illuminating it. When the Power On switch is depressed 24 VAC is applied to the coil of K3A which picks it. This releases the pick of K3B and applies 24 VAC through contacts 13 and 19 to the ON indicator and illuminates it. Pin 7 is now making with Pin 4 of K3A which applies 24 VAC to the coil of K1 and K5. When K1 picks, 208 VAC through pins 5 and 6 and 3 and 4 is applied to the fans. K5 being a 30 sec. time delay relay adjusted to 15 sec. by R, is coming up to pick, but during this 15 sec delay the fans are coming up to speed. When the fans are up to speed the air flow switch closes the 14 VAC is applied to the coil of K4. K4 picks and opens contacts 12 and 9 and closes contacts 1 and 3. By this time K5 has picked and 24 VAC is applied to pin 11 of K5 and to pin 9 of K4. When K4 picked and contacts 1 and 3 made, 24 VAC was applied to the coil of K2 and it picks. When K2 picks, 208 VAC is applied to the logic power supply and the memory power supply.

POWER DOWN

If the fans fail causing the air flow switches to flutter for 1 second or more K4, 1 second time release relay, will drop causing K2 to drop. K2 dropped removes 208 VAC from the logic supply and memory supply. K4 dropped with K5 picked, reapplies 24 VAC to contact 22 of K3B restoring it its normal state and OFF lite is on.

POWER OFF

Depressing the power off switch will pick K3B and release K3A, K3B picked, turns the OFF lite on. K3B picked drops K5 and K1. K1 dropped removes 208 VAC from fans and after K4 drops K2 drops and power is off.

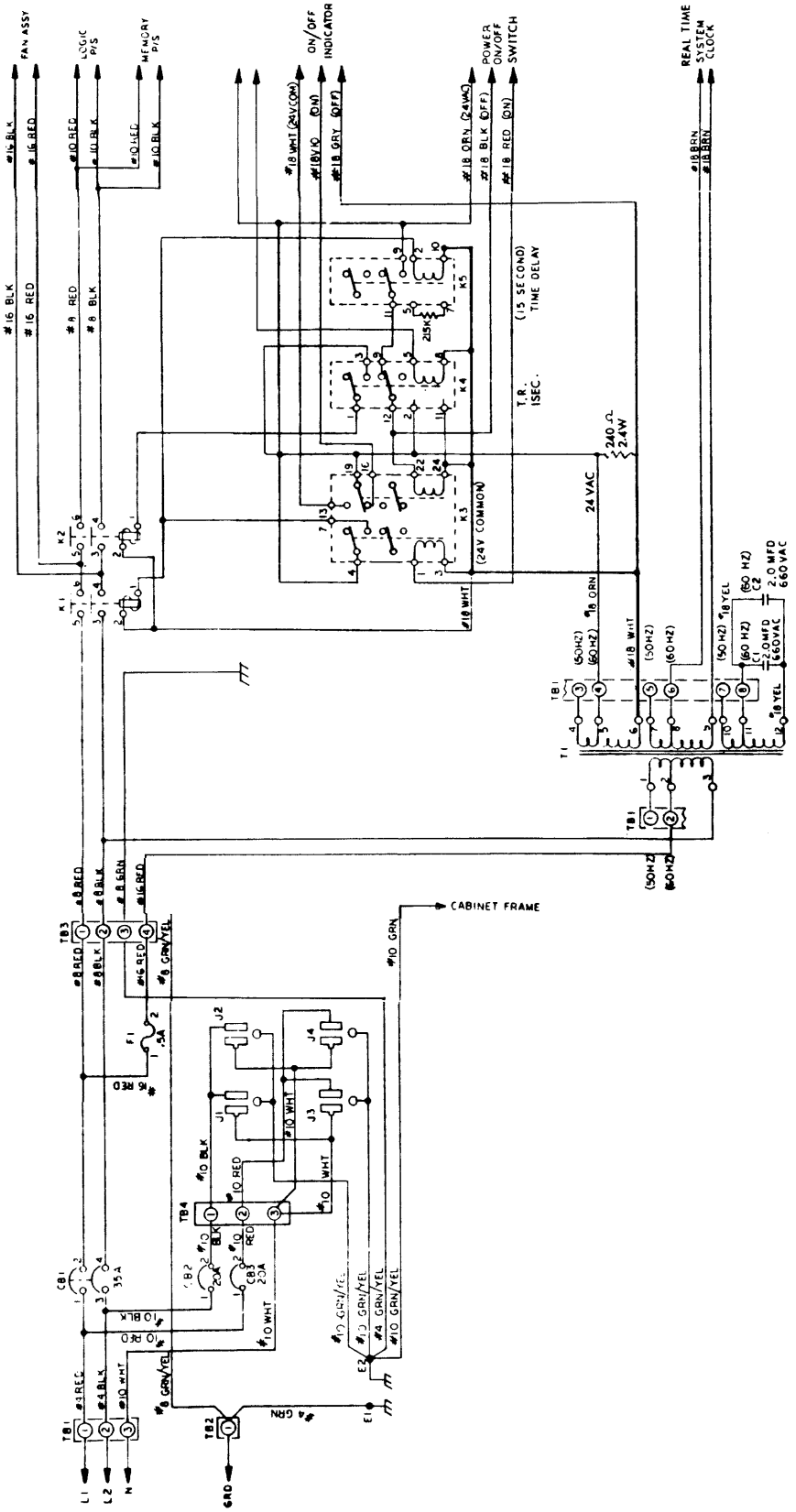


Fig. V-44 AC DISTRIBUTION

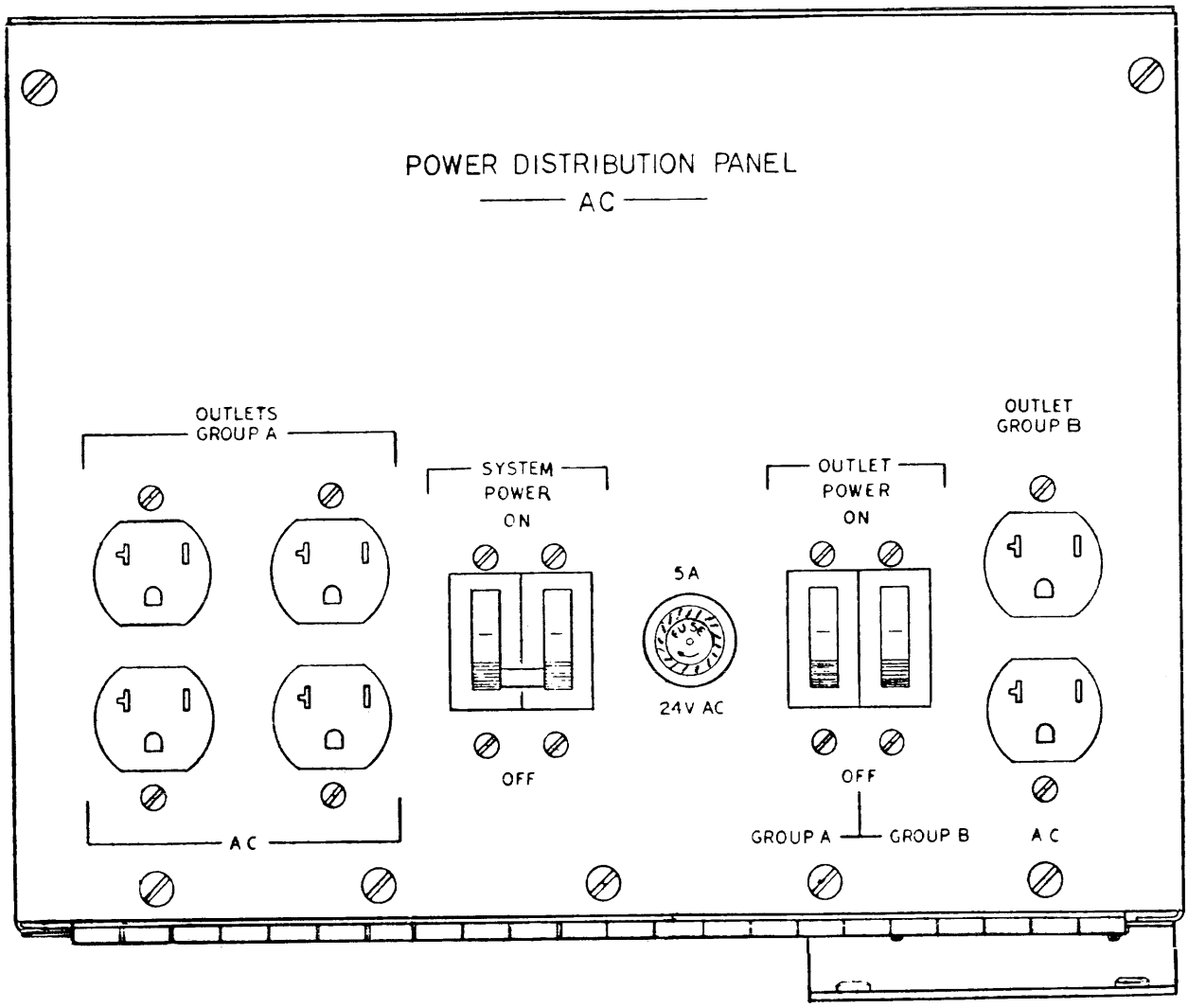
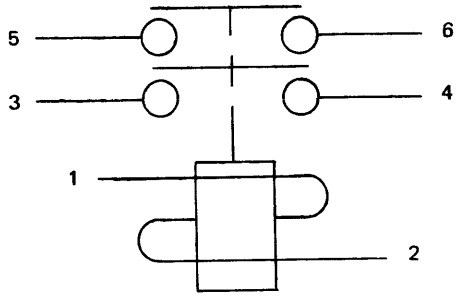


Fig. V-45 AC POWER DISTRIBUTION PANEL

RELAYS

K1 and K2 are contactors 2 Pole N.O. contacts. 10. 30 A. 24VAC. Operating characteristics are pull in voltage 20V maximum, drop out voltage approximately 15V.



K1 and K2 are contractors 2 Pole N.O. contacts. 1Ø. 30 A. 24VAC. Operating characteristics are pull in voltage 20V maximum, drop out voltage approximately 15V.

Fig. V-46 K1 AND K2

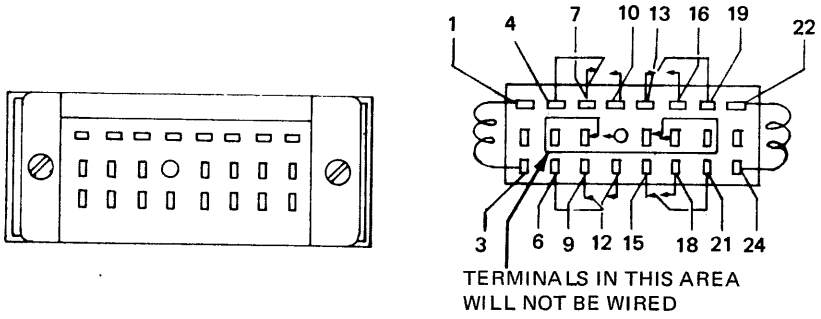
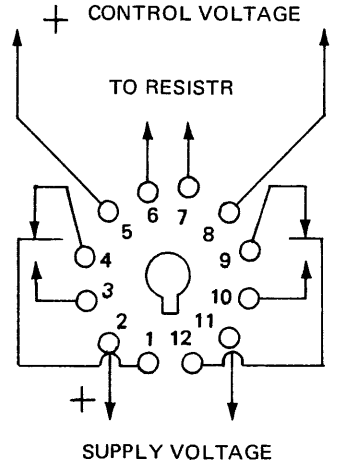
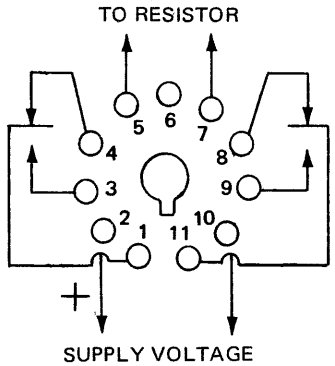


Fig. V-47 K3 RELAY, LATCHING AND RESET, 24VAC. 4 PDT



TYPE: DELAY ON RELEASE, INTERNAL RELAY
SUPPLY VOLTAGE: 24 V AC
DELAY: 1 SECOND, FIXED
RELAY SWITCH: DPDT

Fig. V-48 K4 RELAY, TIME DELAY SOLID STATE, 24 VAC, 1 SECOND DELAY



RESISTOR TO DECREASE DELAY
(215K DECREASES TO 15 SEC)

TYPE: DELAY ON OPERATE, INTERNAL RELAY
SUPPLY VOLTAGE: 24 V AC
DELAY: 30 SECONDS, FIXED
RELAY SWITCH: DPDT
CONTACTS: 10 AMPS AT 115 V AC, 32 V DC

Fig. V-49 K5 RELAY, TIME DELAY SOLID STATE, 24 VAC 30 SECOND DELAY

LOGIC POWER SUPPLY

The logic power supply consists of a main chassis assembly. Within this main assembly there are two additional subassemblies. These subassemblies are a logic card housing and a tubular heat sink. The main chassis assembly houses the logic and control voltage transformers, capacitors, filter chokes, associated circuits and the two subassemblies. The tubular heat sink has a fan mounted at one end to cool the high power components mounted on it. There are two temperature sensing thermostats on the heat sink which will remove the AC input to the transformer when the heat sink temperature reaches 120°C.

The logic card housing is composed of seven cards:

1. VCO timing card
2. Gate driver card
3. 160 volt regulator card
4. Control supply voltage card
5. -2 Volt shunt card
6. +12 volt card
7. -12 Volt card

These cards are mounted on the inside of the cabinet and have backplane wiring which can be used for troubleshooting. These logic cards can also be placed on a card extender to test locations not available at the backplane. Detailed circuit descriptions are contained in Section II. Additional troubleshooting aids includes overvoltage sensing for ±12V, 4.75V and -2 volts. These output voltages also have overcurrent protection.

TROUBLE SHOOTING

When trouble shooting the logic power supply, the following rules must be observed:

1. All trouble shooting must be performed with the dummy load connected to the system.
2. The oscilloscope must be floating. (Not connected to power ground).
3. The oscilloscope and the main chassis assembly must not come in contact.
4. Only one probe can be used when checking gate driver pulses.
5. Dummy load must be correctly installed.
6. Extra care and caution must be observed. Remember 208 volts is present throughout the supply when power is applied.

The logic cards can be tested individually with the exception of the gate driver card and the -2 volt shunt card. These cards must be tested with the VCO timing card and the control supply card inserted. Power can be applied to the system with the -2 volt shunt card removed only if the -2 volt output is shorted to ground, with the shorting bar supplied with the dummy load. The +12 volt and -12 volt cards are identical and may be interchanged for trouble shooting purposes.

There are three service switches available to the Field Engineers when trouble shooting the logic power supply. The following is a description of the function of each of the switches:

Switch No.	Card	Position	Function
1	VCO Timig	Normal	Normal operation
		Off	No VCO timing pulses to the gate drivers.
		Override	Simulates the presence of the 160 converter. Used to check the gate driver circuits.
2	160 volt Regulator	On	Normal Operation
		Off	The +160 volts is removed by opening the secondary winding to the +160 volt regulator.
3	-2 volt Shunt	On	Normal operation
		Override	When the supply fails due to an overvoltage this switch will keep the supply running.

Switch No.	Position	Result
1	Off	The inverter, VCO timing and gate drivers are disabled.
2	On	The 160 volt converter is active.
3	Normal or Service	

Switch No.	Position	Result
1	Override	The VCO timing and gate driver circuitrs are operational.
2	Off	The 160 volt converter and inverter are disabled.
3	Normal or Service	

Switch No.	Position	Result
1	Normal	The overvoltage shutoff circuits are disabled. The output voltages may be checked to locate the incorrect voltage.
2	Normal	
3	Service	

The 40 amp fuse (F1) may be removed to isolate the +160 volts when trouble shooting the inverter circuit.

PRELIMINARY INSPECTION

1. Check that input and output terminals are properly connected.
2. Measure the AC input. Make sure that the incoming AC voltages is between 190-250 volts.
3. Check for an overload condition at the power supply output terminals.
   A. Using a ohm meter measure:
      (1) -2V to ground reading should not be less than 10 mega ohms.
      (2) +4.75V to ground reading should not be less than 24 mega ohms to ground.
   B. Measure $\pm$12 volt supply. Reading should not be less than 1.2 ohms to ground.

TROUBLESHOOTING STEP I – PREPARATION

1. Open circuit breaker (C.B.).
2. Disconnect all power supply loads.
3. Pull power supply chassis out of cabinet.
4. Remove upper panel.
5. Check and replace if necessary the 40-Amp fuse and/or the MDL-1 1-Amp fuse.
6. Power up system.
7. If a system does not come up, refer to Main Trouble Shooting Flow.

TROUBLE SHOOTING STEP III – OVERHEATING

The thermostat switch automatically opens when the heatsink temperature reaches 120^{o}C or above and closes when it drops below 120^{o}C. If thermostat opens after the Logic Supply has been turned on, eliminate any cooling obstruction or any cause of over-heating. Replace thermostat if necessary.

Figures V-51 through V-56 are board layouts showing component location on each card. These should be used in conjunction with their counter part electrical schematic.

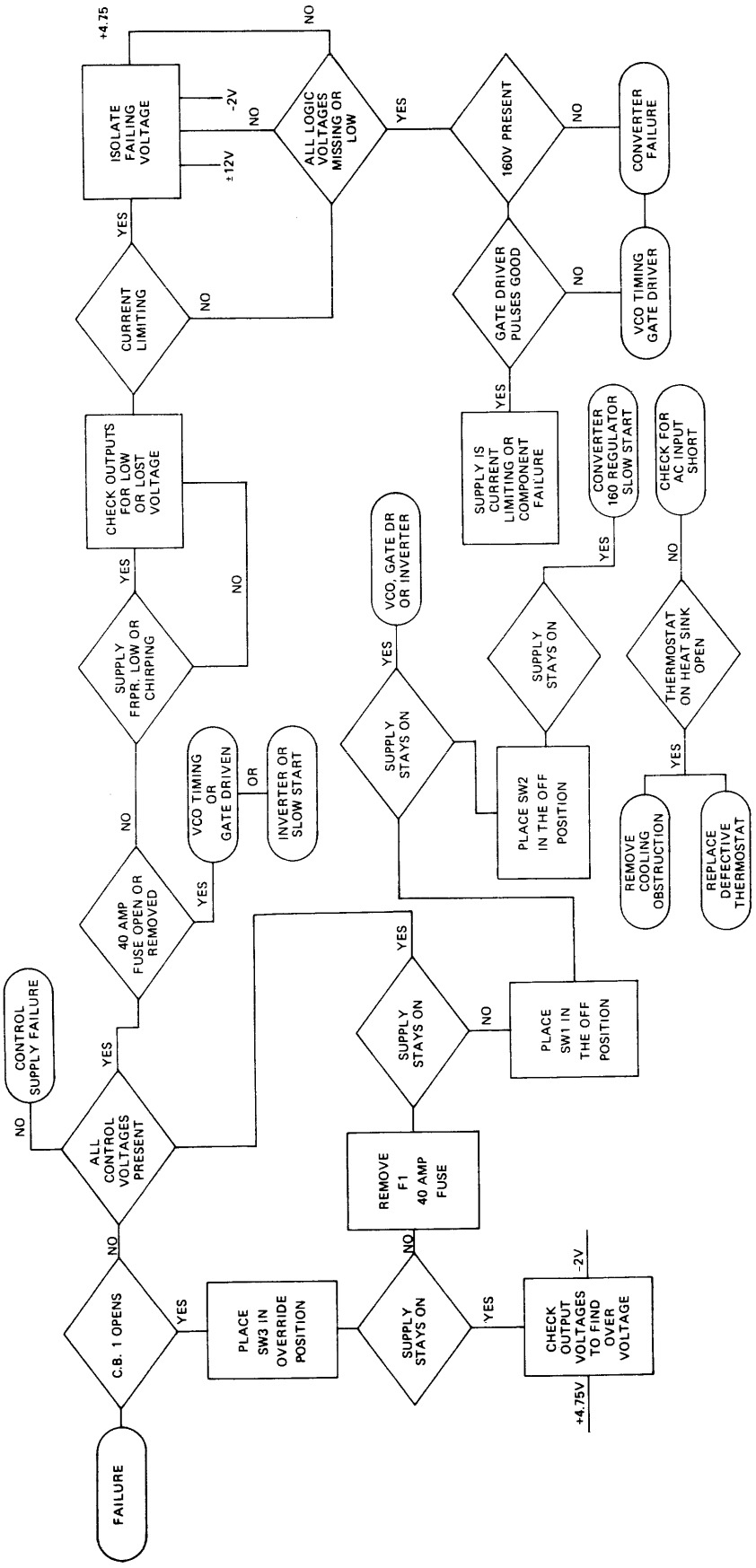


Fig. V-50 B1700 LOGIC SUPPLY MAIN TROUBLE SHOOTING FLOW

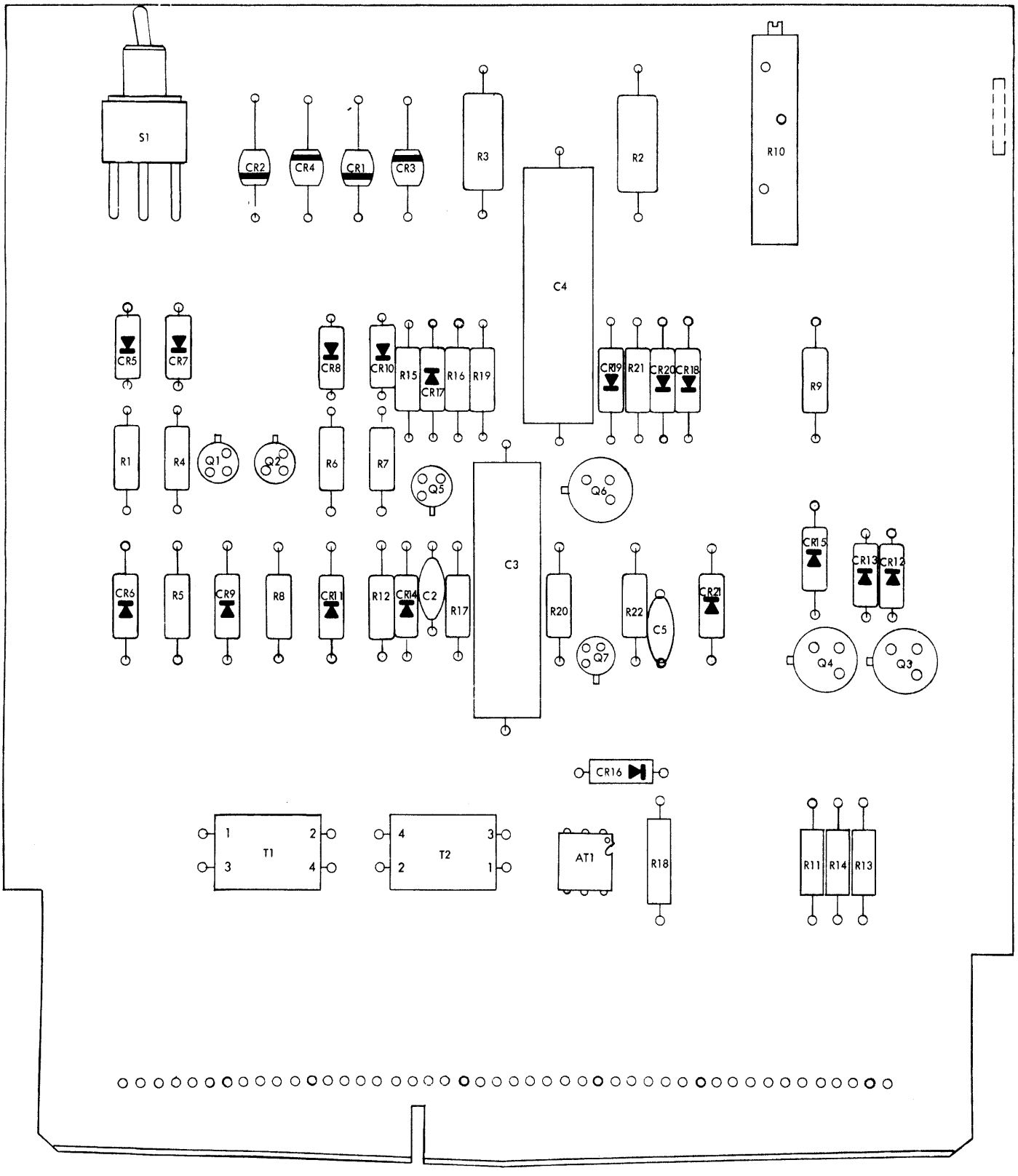


Fig. V-51 -160 VOLT REGULATOR

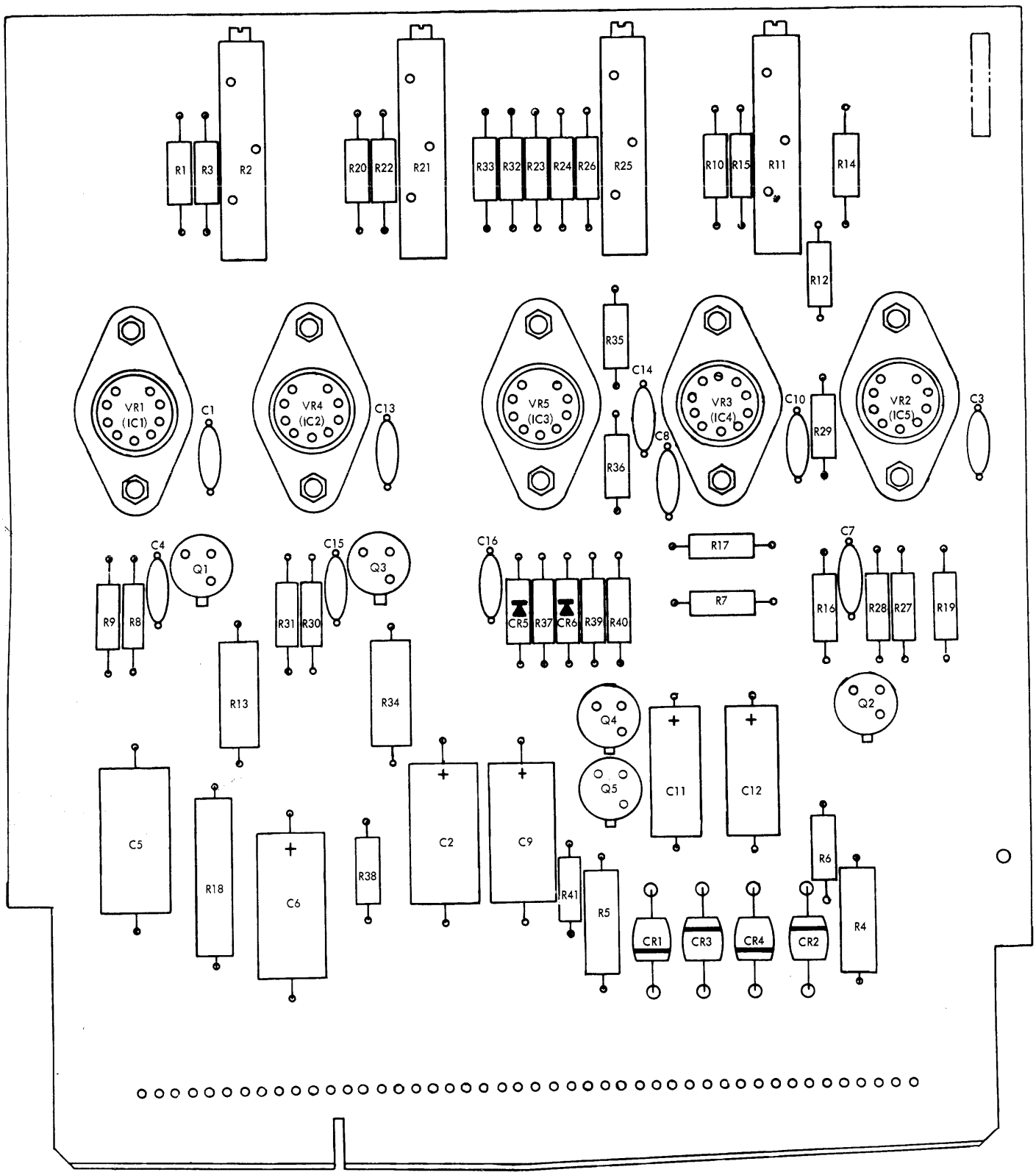


Fig. V-52 CONTROL SUPPLY

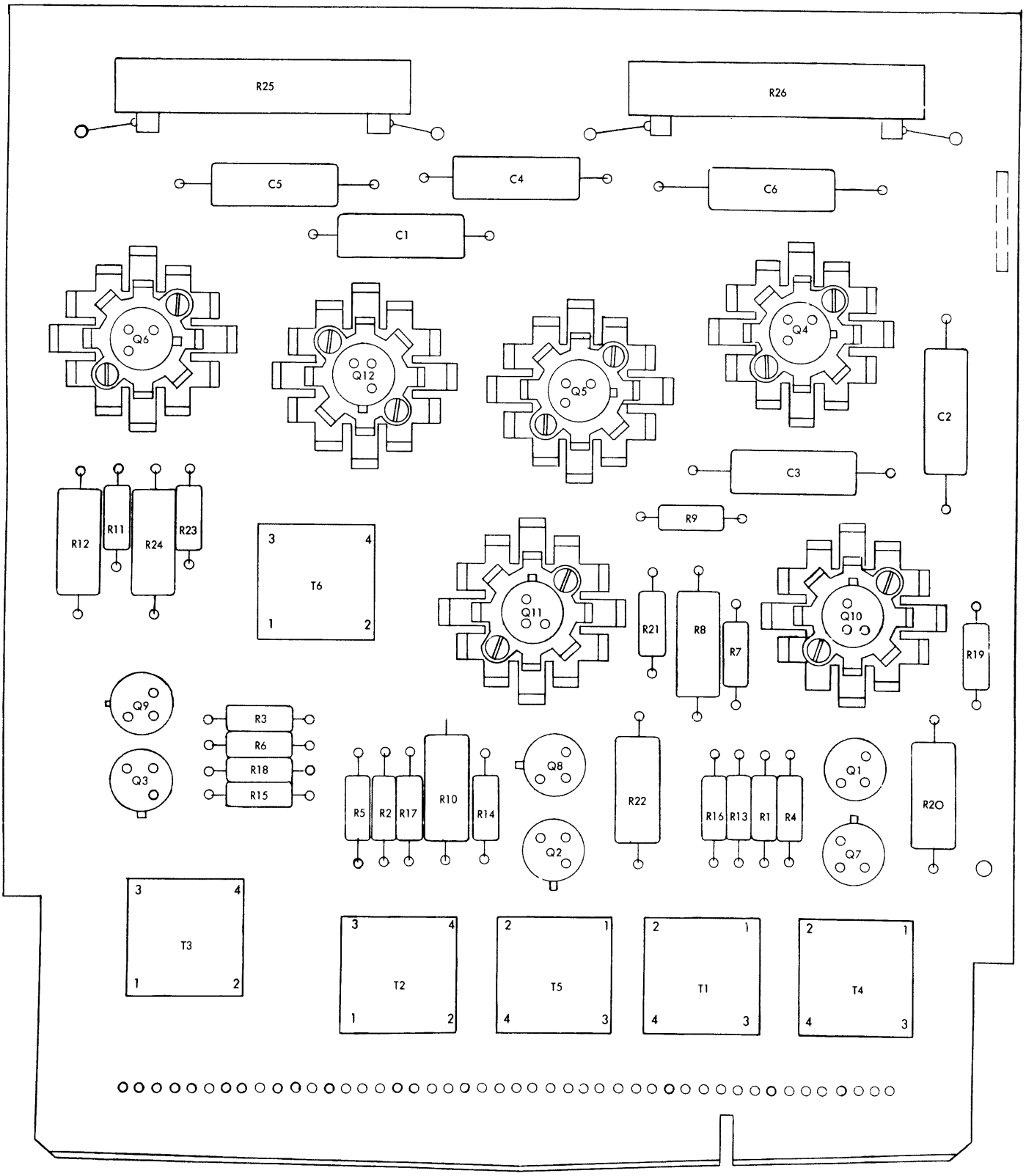


Fig. V-53 GATE DRIVER

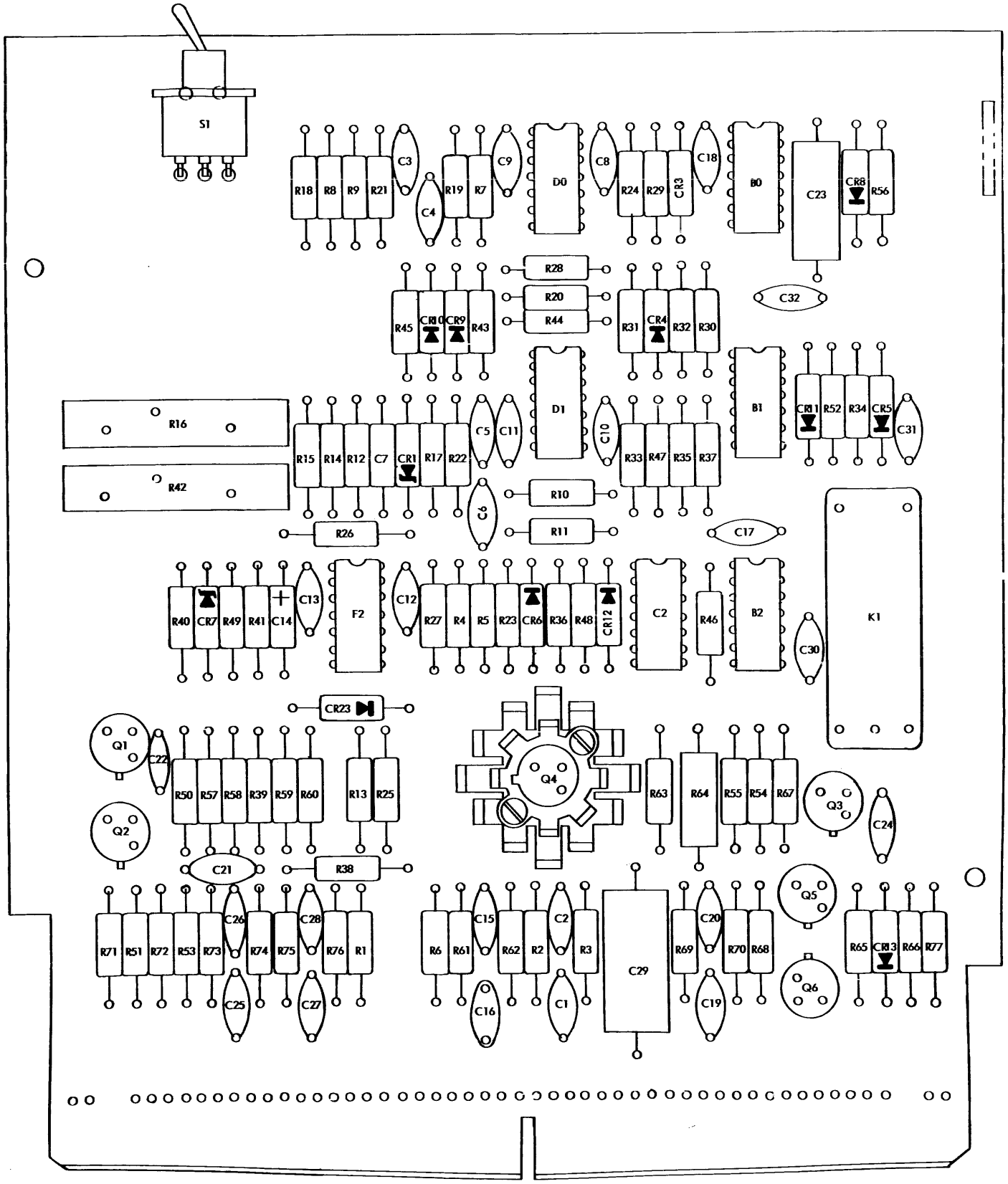


Fig. V-54 -2 VOLT SHUNT REGULATOR

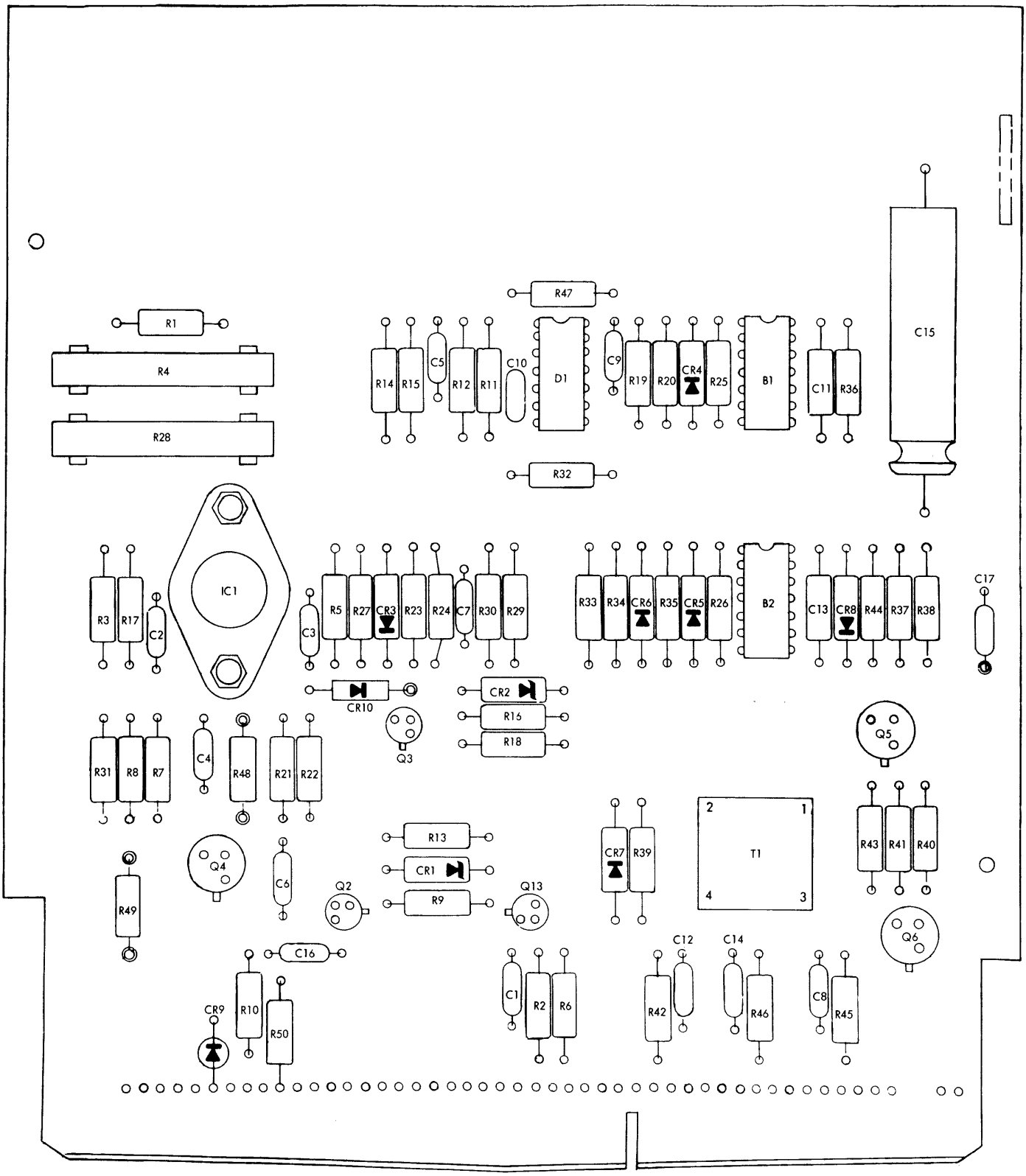


Fig. V-55 12 VOLT POWER SUPPLY

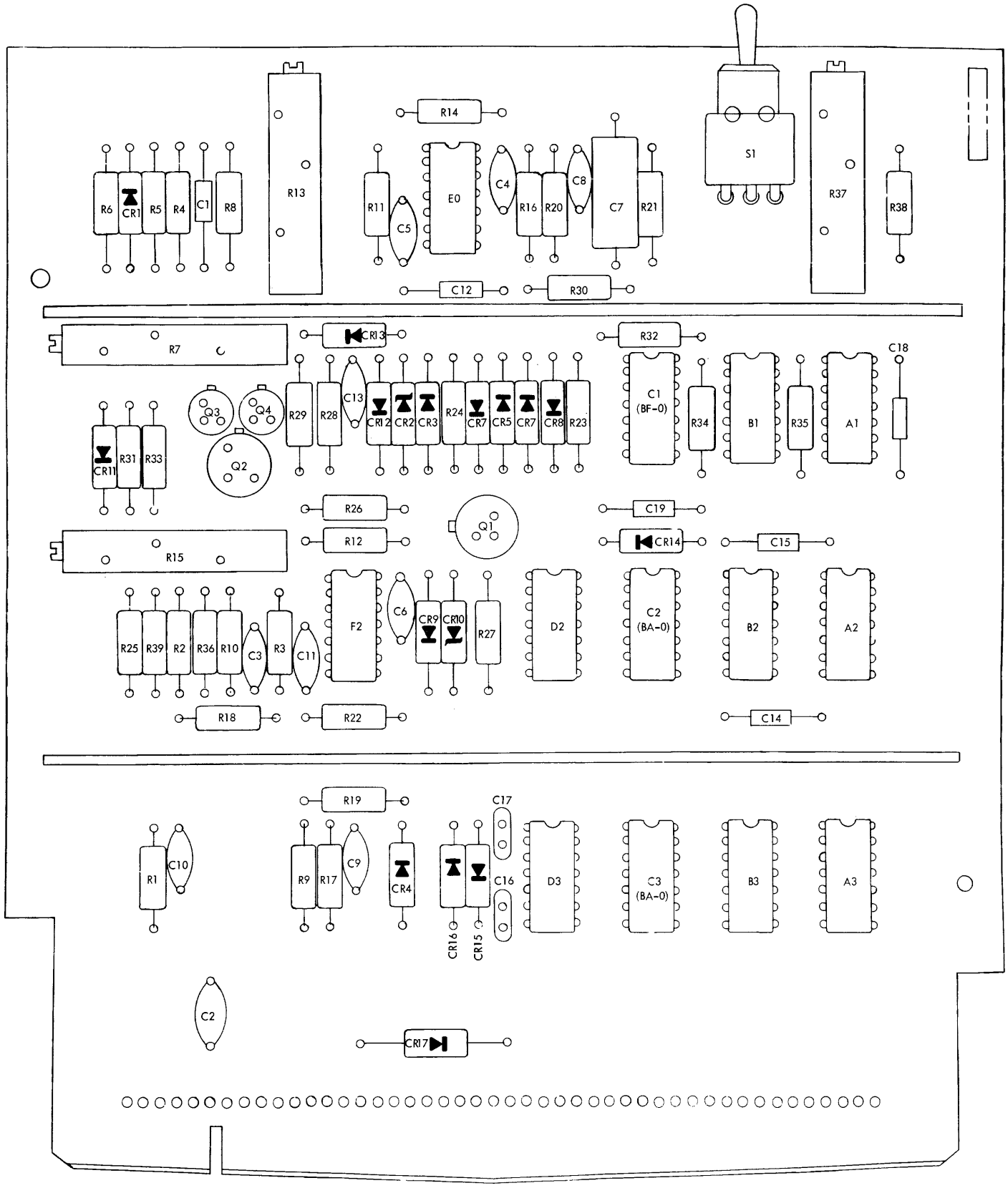


Fig. V-56 TIMING CARD

TYPICAL WAVEFORMS

The wave forms shown in Figure V-57 through V-78 represent the different test points important to the operation of the power supply. All measurements were made with the supply driving 100 AMP dummy load.

Figure V-57 shows the wave forms from the Cathodes of CR14, CR6 and CR9 to 160 volt positive.

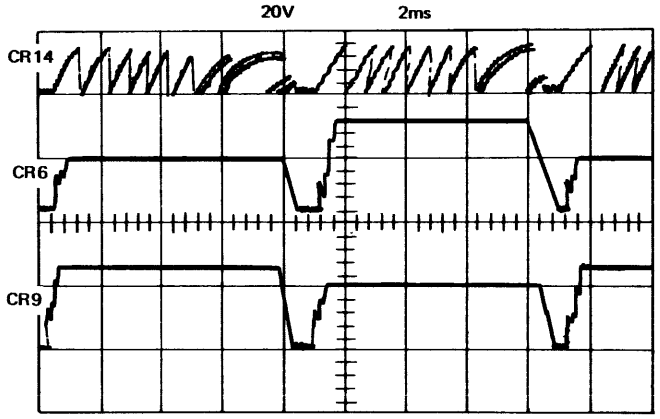


Fig. V-57 +160V REGULATOR CARD

Figure V-58 shows the wave forms of the SCR Gate at J3 pins OR to OP and OP to OK.

Figures V-59, V-60 and V-61 show the wave forms of the comparator timing to be observed from D2N, D2K, D2H, D2A, D2P, D2H, F0G, E0K.

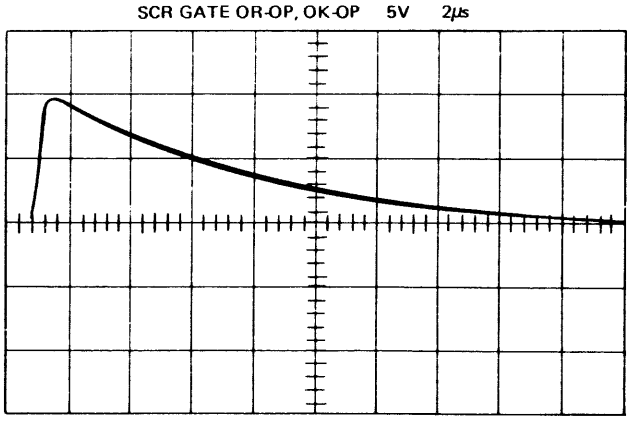


Fig. V-58 +160V REGULATOR CARD SCR GATE

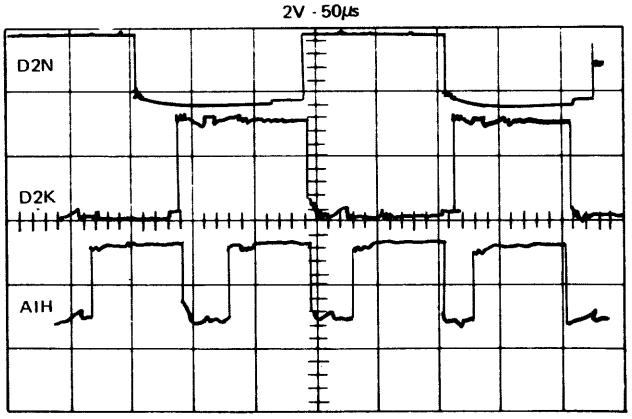


Fig. V-59 COMPARATOR – VCO-TIMING CARD (TIMING)

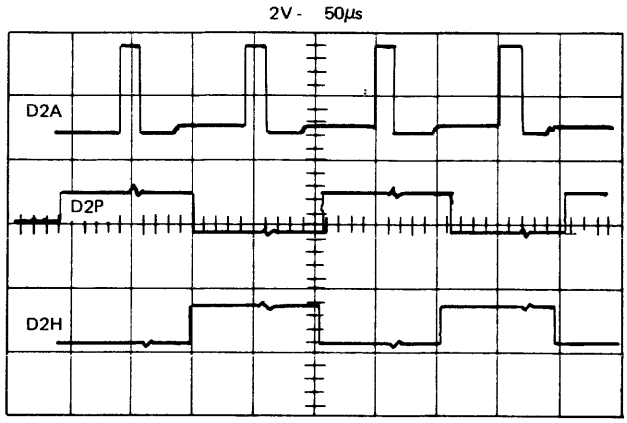


Fig. V-60 COMPARATOR – VCO-TIMING CARD (TIMING)

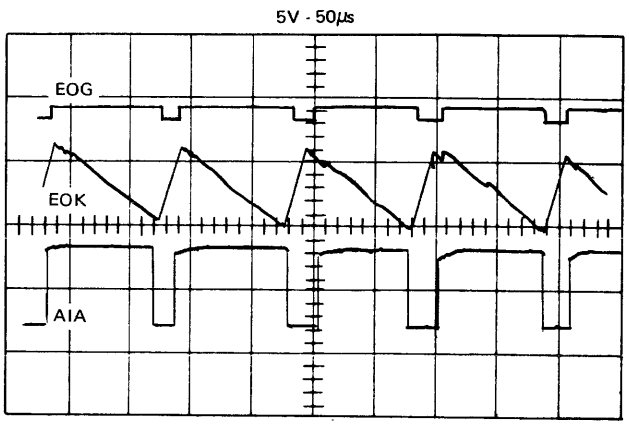


Fig. V-61 COMPARATOR – VCO-TIMING CARD (VCO)

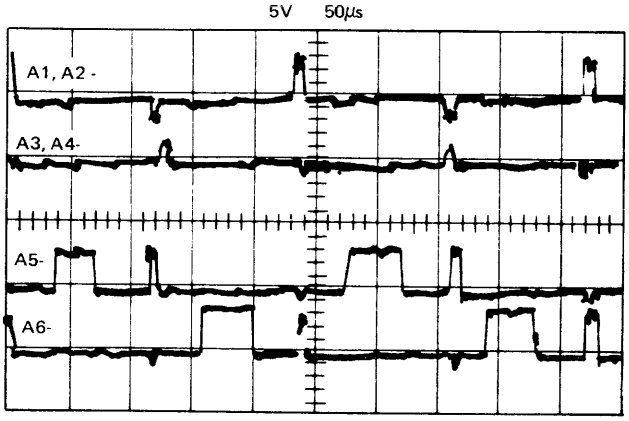


Fig. V-62 GATE DRIVER INPUTS

Figure V-62 shows the wave forms to be observed between A1, A2, A3, A4, A5, A6 and ground on the Timing Card.

Figures V-62 thru V-64 shows the wave forms to be observed at A1, A2, A3, A4, A5 and A6. Be sure to float the scope when making these measurements.

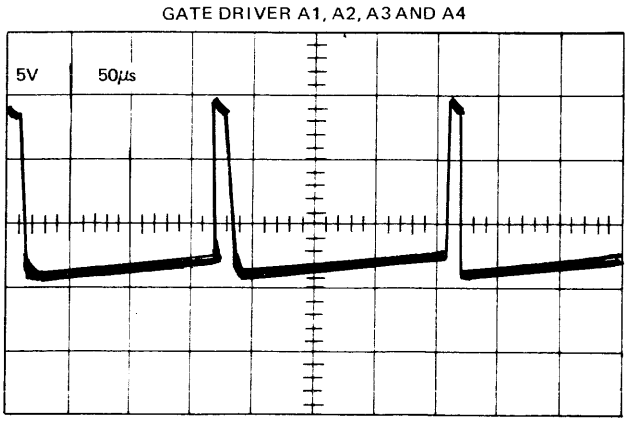


Fig. V-63 GATE DRIVER OUTPUTS

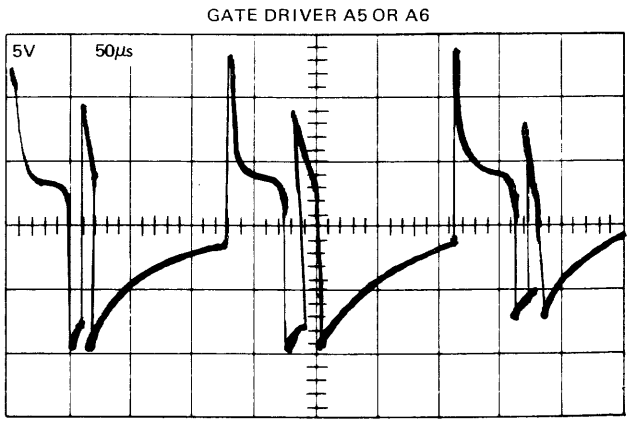


Fig. V-64 GATE DRIVER OUTPUTS

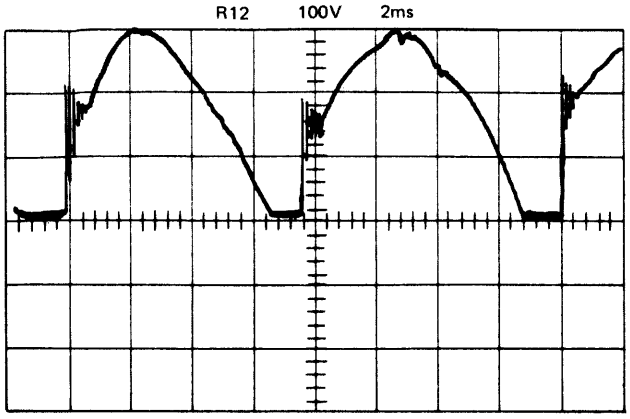


Fig. V-65 AC/DC CONVERTER TERMINAL 2 & 3

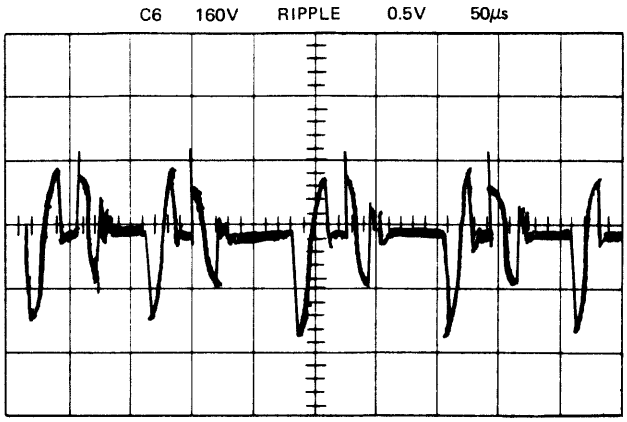


Fig. V-66 RIPPLE ON 160V OUTPUT

Figure V-65 shows the wave form to be observed at terminals 2 and 3 of L1 in the converter.
Figure V-66 shows the wave form to be observed across C6 in the converter.

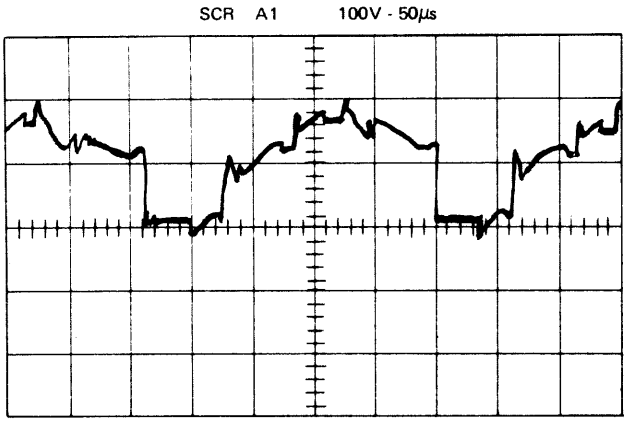


Fig. V-67 INVERTER SCR A1

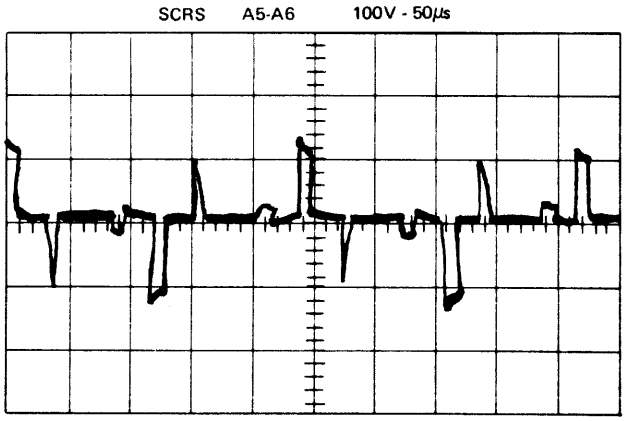


FIG Fig. V-68 INVERTER SCR A5 & A6

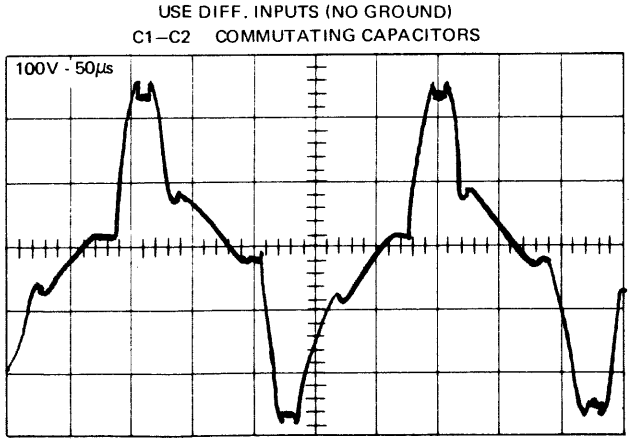


Fig. V-69 COMMUTATING CAPACITORS

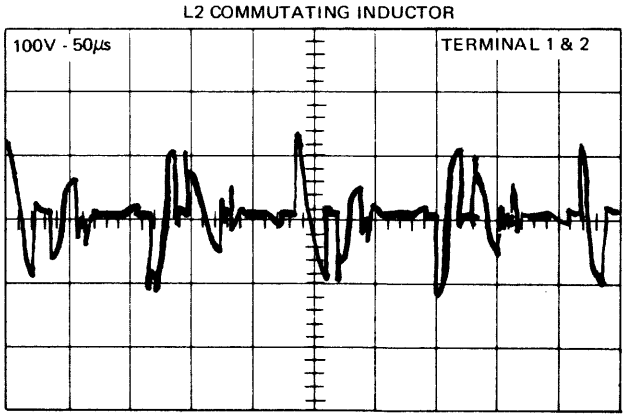


Fig. V-70 COMMUTATING INDUCTOR

Figure V-67 through V-71 shows the waveforms to be observed across components in the inverter. On Power Supply schematic 1 of 8.

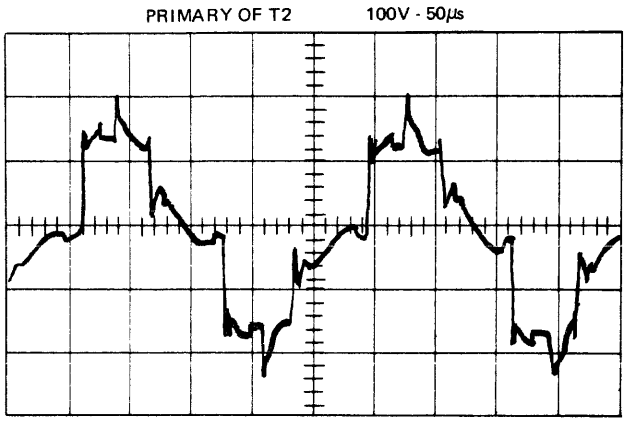


Fig. V-71 T2 OUTPUT

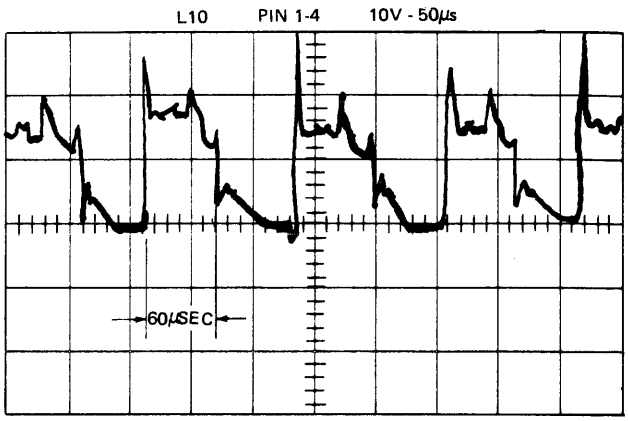


Fig. V-72 AC/DC CONVERTER TIMING

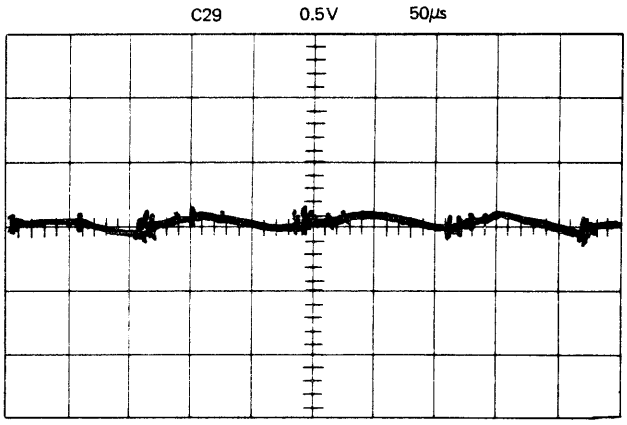


Fig. V-73 C29 RIPPLE

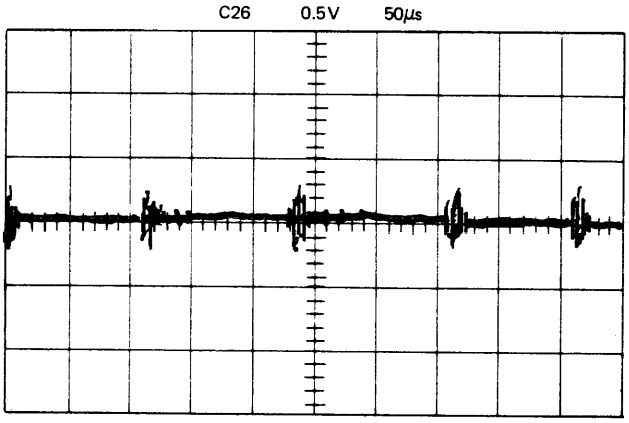


Fig. V-74 C26 RIPPLE

Figure V-72 through V-74 shows the wave forms to be observed across components in the AC/DC converter on power supply schematic 2 of 8.

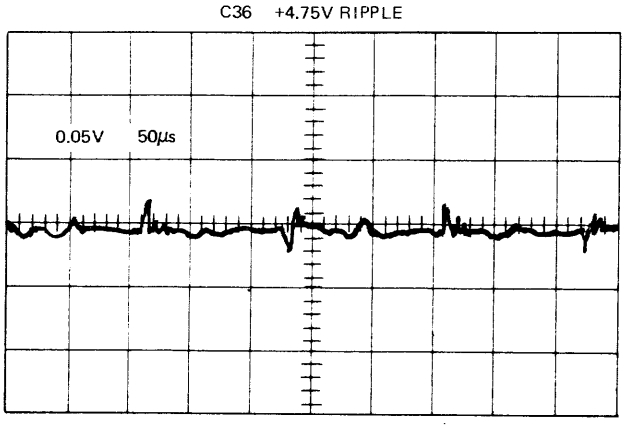


Fig. V-75 +4.75V OUTPUT

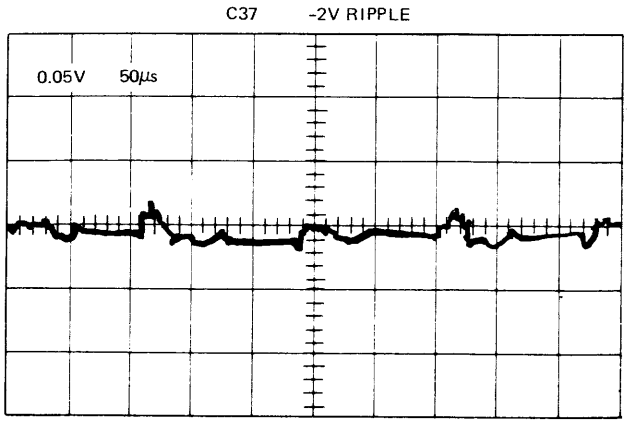


Fig. V-76 -2.0 VOLT RIPPLE

Figure V-75 shows the wave form to be observed across C36 on Power Supply schematic 2 of 8.
Figure V-76 shows the wave form to be observed across C37 on Power Supply schematic 2 of 8.

MEMORY POWER SUPPLIES

Figure V-77 is a general flow approach to troubleshoot the memory supplies. For detailed troubleshooting, maintenance and adjustment procedures, refer to the North Electric Manuals N10000 and N14000 supplied as part of T & F documents.

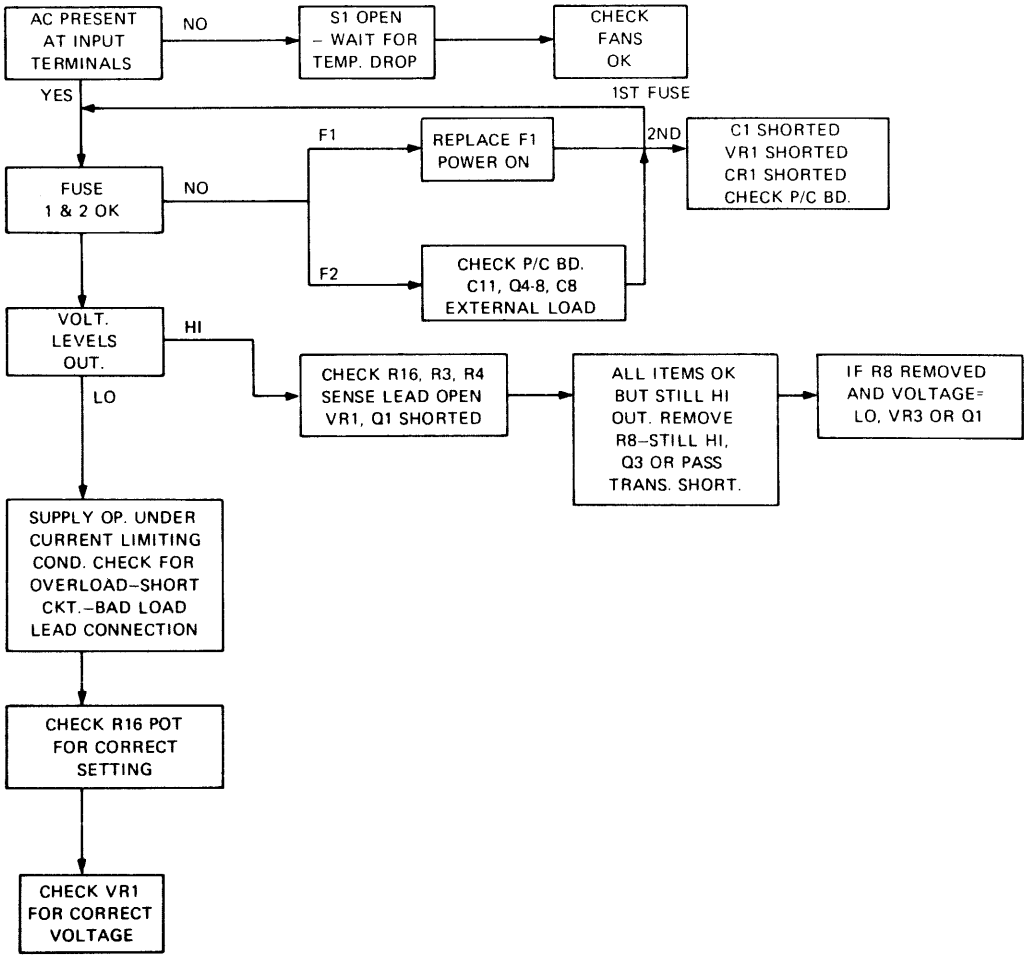


Fig. V-77 MEMORY POWER SUPPLY TROUBLE SHOOTING FLOW

WIRE WRAP TOOL

There is a specific hand wire wrap tool for each gauge (26 or 30) solid wire. To wrap a wire to a pin, proceed as follows:

1. Remove the insulation from the end of the wire. Approximately one and one quarter inches of wire is required for a six-turn connection of wire.

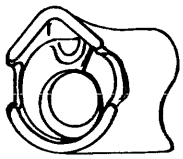


Fig. V-78
BIT AND SLEEVE

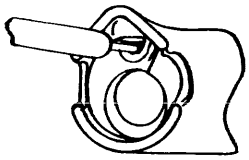


Fig. V-79
WIRE INSERTION

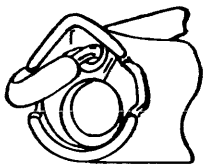


Fig. V-80
WIRE ANCHORING

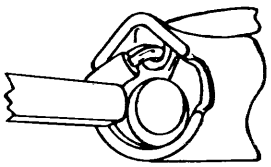


Fig. V-81
TERMINAL INSERTION

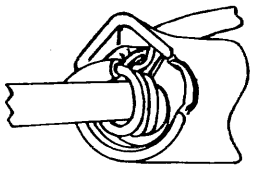


Fig. V-82
WRAPPING

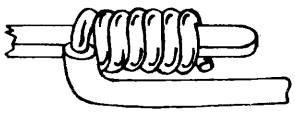


Fig. V-83
FINISHED CONNECTION

2. Select the wire wrap tool applicable for the specific gauge wire used.
3. Place the tool over the wire as shown in Figure V-79.
4. Anchor the wire as shown in Figure V-80 and insert the tool over the pin as shown in Figure V-81.
5. Rotate the tool in a clockwise direction. The wire will wrap around the pin as shown in Figures V-32 and V-83. Too much pressure will cause the wire to bunch.

The following should be used as a guide when installing RINs or when making wiring changes in the field.

1. Number of Turns – The minimum number of turns (per connection) of bare wire is FIVE, and maximum number is SEVEN. The maximum number of turns of insulation preceding the bare wire is THREE for any connection.
2. Insufficient Insulation – Wire insulation shall be no greater than 1/32" from wire wrapped connections.
3. Wire and Terminal Contact – The bare wire and terminal must make contact on all corners following the point at which the origin of the number of turns are counted.
4. Separation of Turns – Turns may have a maximum separation of ½ the thickness of wire being used to make the wrapped connection.
5. Excessive Tail Wire – The wire tail shall be construed as being "that end of bare wire which follows the last wrap". The wire tail shall be parallel to the terminal surface within 1/32 of an inch.
6. Overlapping of Turns – This condition is caused when succeeding wraps overlap the ones previously made. If this condition exists, it will be necessary to make a new connection.
7. Clearance – There shall be at least 1/32 of an inch clearance between grid pattern connections, terminals, bare wire or components.
8. Height – The maximum clearance between the connector block and the first turn of the first connection shall be 1/16 of an inch.
9. Height for Single Wrap – The maximum height for a single wrap shall be 1/4 of an inch.
10. Height for Two Wraps – The maximum height for two wrapped connections shall be ½ of an inch.
11. Unwrapping – The connection shall be capable of being unwrapped from the wire wrapped terminal without breaking. The unwrapping operation shall be done with a standard unwrapping tool only, so as to insure the life of the wire wrapped terminal.
12. Wire-Re-Use – IF A WIRE WAS PREVIOUSLY WRAPPED, THE PORTION OF THE WIRE WHICH WAS WRAPPED CANNOT BE USED AGAIN. If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. Soldering a wrapped connection directly at the terminal is not recommended.
13. Terminal Re-Use – Prior to re-wrapping, the terminal should be inspected for damage. When there is plating loss, corrosion or other damage which would cause a poor connection, the terminal must be replaced.

B 1700

CENTRAL SYSTEM

SECTION

VI

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

INSTALLATION
PROCEDURES

Printed in U.S. America 11-20-72

For Form 1053360

INTRODUCTION

This section contains information for the installation of the Central System. The installation of the Central System is unique to itself and the I/O Base will be covered in the B1700 I/O Base Technical Manual. Also, refer to the B1700 Installation Manual for complete system installation.

GENERAL

The Central System installation is normally in three (3) parts. They are as follows:

A. Mechanical assembly of the Central System components.
B. Electrical interconnection by cable installation.
C. Initial checkout to verify correct installation and operation.

All packing containers should be checked for damage when the system arrives. Also, after the equipment has been unpacked, verify that all items have been received. Then, install and interconnect the system as outlined in the following paragraphs.

MECHANICAL ASSEMBLY

The Central System, except for the table, is shipped in an assembled condition. The table is connected to the main chassis via four (4) bolts. Refer to the B1700 Installation Manual for the correct procedure.

All of the I/O control and peripheral assembly is discussed in the B1700 I/O Base Technical Manual.

Description	Cab	Cd. Pos.
Processor Card A	A	A6/7
Processor Card B	A	B0/1
Processor Card C	A	A3/4
Processor Card D	A	B3/4
Processor Card E	A	A0/1
Processor Card F	A	B6/7
Processor Card H	A	C6/7
Processor Card J	A	C0/1
Processor Card K	A	C3/4

TABLE VI-1

Description	Cab	Cd Pos	Conn	Cab	Zone	Cd Pos	Conn
Processor Card A	A	A6/7					
Processor Card B	A	B0/1					
Processor Card C	A	A3/4	X$		J3	Console	
Processor Card D	A	B3/4	X#			B6/7	X#
Processor Card D	A	B3/4	Y$			B6/7	Y$
Processor Card E	A	A0/1	X$		J1	Console Lights	
Processor Card E	A	A0/1	X#		J2	Console Switches	
Processor Card E	A	A0/1	Y$		J4	Console Cassette	
Processor Card E	A	A0/1	Y#	I/0	Bus	A0/1	X#
Processor Card F	A	B6/7	X#			B3/4	X#
Processor Card F	A	B6/7	Y$			B3/4	Y$
Processor Card H	A	C6/7	X$			C3/4	X$
Processor Card J	A	C0/1	X#			C3/4	X#
Processor Card J	A	CO/1	Y$			C3/4	Y$
Processor Card J	A	C0/1	Y#			C3/4	Y#
Processor Card K	A	C3/4	X$			C6/7	X$
Processor Card K	A	C3/4	X#			C0/1	X#
Processor Card K	A	C3/4	Y$			C0/1	Y$
Processor Card K	A	C3/4	Y#			C0/1	Y#

TABLE VI-2

ELECTRICAL INTERCONNECTION

The Central System is shipped with all cables (except power) connected. Card locations and cable connections between cards are listed in Tables VI-1 and VI-2.

The system power is connected to the AC Power Distribution Module. Refer to the B1700 Installation Manual for the correct procedure.

INITIAL CHECKOUT

The Central System has been thoroughly checked out at the factory and should be received trouble free. To insure that the Central System will perform correctly, certain precautions should be observed before applying power and before the system is given to the customer. These precautions will be explained in the following phases of the checkout procedure.

A. Static tests (Power off)
B. Static tests (Power on)
C. Dynamic Tests

After satisfactory completion of the checkout procedure, refer to the I/O Base Technical Manual for the proper installation and checkout of the B1700 peripheral devices.

STATIC TESTS (POWER OFF)

These tests will insure that the Central System will not fail due to short or open circuits. The following procedure is recommended for this series of tests.

A. Check to see that both the system and wall circuit breakers are in the off position.
B. Using a recommended multimeter, insure that some measure of resistance is present between the +4.75V, -2.0V, +12.0V, and -12.0V when referenced to ground. See Section VI for testpoints.
C. Insure that some measure of resistance is present between each of the supply voltages mentioned above.
D. Check for continuity between the logic power supply outputs on the processor backplane pins listed in Table VI–3.

Voltage	Backplane Testpoint	Comments
+4.75V	0AX	All Cards
	1AX	
-2.0V	0ZY	All Cards
	1ZY	
-12.0V	0ZX	Card H

TABLE VI-3 LOGIC VOLTAGE PINS

E. Check the memory voltage supplies to insure that some measure of resistance is present between logic ground and the voltages listed in Table VI–3.

	Voltage	Backplane Testpoint	Comments
1.	+19.0V	0AY	All memory cards
2.	+23.0V	1AY	All memory cards
3.	-5.0V	0ZX	All memory cards

TABLE VI-4 MEMORY VOLTAGE PINS

F. Check for continuity between the memory power supplies and the points listed in Table VI–4.

STATIC TESTS (POWER ON)

These tests are performed to insure that the basic system requirements for proper operation are present and set to the proper values. These tests involve four (4) integral areas within the system:

1. Power supplies
2. Clock circuits
3. Console
4. Basic control logic

With the satisfactory completion of these tests, a building block will have been established for more thorough testing of the Central System.

POWER UP

To power up the system: A) place both the wall and the system circuit breakers in the ON position; B) depress the Power On button.

Power Supplies–Check the outputs of the logic and memory power supplies. Insure that all the voltages are within tolerance. Refer to Section IV (Adjustments) of this Manual, if any voltage requires adjustment.

Clock Circuits–Perform the checkout procedure outlined in Section IV (Adjustments) of this Manual.

Console–The ability to load and display registers or memory location from the console insures that basic control logic and circuit function are operating correctly. The basic testing of this logic is discussed within this section.

The following procedures load the value selected by the 24 console switches (0's or 1's) into a designated sink register. In addition the new contents of this register are displayed by the 24 console lamps.

Execution Procedure:

A. Depress the clear pushbutton.
B. Place the register select rotary switch to the designated position.
C. Place the register group rotary switch to the designated position.
D. Set the 24 toggle switches to the required value.
E. Depress the load pushbutton.
F. Special instructions will be specified for each test.

Test 1 and Test 2 verify the ability to load, change and read the contents of all Registers Select 2 Sink location.

TEST 1

1. Register select rotary switch = 2
2. Register group rotary switch = X
3. Toggle switches = FFFFFF (All up)

Special Instructions:

After each depression of the load pushbutton rotate the register group rotary switch in a clockwise direction one position, until one revolution is completed.

The test results are shown in Table VI-5.

REGISTER GROUP		INDICATOR LIGHTS
	X	FFFFFF
	Y	FFFFFF
	T	FFFFFF
	L	FFFFFF
MAR	A	-7FFF-
	M	--FFFF
	BR	FFFFFF
	LR	FFFFFF
	FA	FFFFFF
	FB	FFFFFF
	FL	--FFFF
	TAS	NO CHANGE (SOURCE ONLY)
	CP	----FF

TABLE VI-5 TEST RESULTS

TEST 2

1. Register select rotary switch = 2
2. Register group rotary switch = X
3. Toggle switches = 000000 (all down)

Special Instructions:

After each depression of the load pushbutton, rotate the register group rotary switch one position in a clockwise direction until one revolution is completed.

The test results are shown in Figure VI-6.

REGISTER GROUP		INDICATOR LIGHTS
	X	000000
	Y	000000
	T	000000
	L	000000
MAR	A	-0000-
	M	--0000
	BR	000000
	LR	000000
	FA	000000
	FB	000000
	FL	--0000
	TAS	NO CHANGE (SOURCE ONLY)
	CP	----00

TABLE VI-6 TEST 2 RESULTS

TEST 3

This test checks the ability to address the T and L registers in 4 bit increments.

1. Register select rotary switch = 2
2. Register group rotary switch = T
3. Toggle switches = ABCDEF (10, 11, 12, 13, 14, 15) values
4. Depress load pushbutton
5. Register group rotary switch = L
6. Depress load pushbutton.

Special Instructions:

A. Register select rotary switch = 0
B. Register group rotary switch = TA thru LF

The test results are shown in Table VI-7.

REGISTER GROUP	INDICATOR LIGHTS
TA	00000A
TB	00000B
TC	00000C
TD	00000D
TE	00000E
TF	00000F
LA	00000A
LB	00000B
LC	00000C
LD	00000D
LE	00000E
LF	00000F

TABLE VI-7 TEST 3 RESULTS

TEST 4

This test checks for the ability to address registers CA, CB, CC and CD as either a four (4) bit sink or source.

1. Register select rotary switch = 0
2. Register group rotary switch = CA
3. Toggle switches = 00000F
4. Depress the load pushbutton

Special Instructions:

A. After each depression of the load pushbutton, rotate the register group rotary switch one position in a clockwise direction until the switch is set to the TE Register.
B. Return the register group rotary switch to the CA position.
C. Place all of the toggle switches in the OFF position (down). Repeat the above steps.

The test results are shown in Table VI-8.

Toggle switches = 00000F	Toggle switches = 000000
CA = 00000F	CA = 000000
CB = 00000F	CB = 000000
CC = 00000F	CC = 000004 (Real Time Clock
CD = 000008	CD = 000000 Intp. sets ccb:T2)

TABLE VI-8 TEST 4 RESULTS

TEST 5

This test check for the ability to address the FB register in four (4) bit increments.

1. Register select rotary switch = 2
2. Register group rotary switch = FB
3. Toggle switches = ABCDEF
4. Depress the load pushbutton

Special Instructions:

A. Register select rotary switch = 1
B. Register group rotary switch = rotate 1 position at a time from FU to FLF.

The test results are shown in Table VI-9.

REGISTER GROUP	INDICATOR LIGHTS
FU	A
FT	B
FLC	C
FLD	D
FLE	E
FLF	F

TABLE VI-9 TEST 5 RESULTS

In tests six (6) through eleven (11) the X and Y conditions are checked. In doing these tests it verifies that the basic logic of the 24 bit arithmetic unit is functioning properly.

TEST 6

X = Y when X and Y are set to 0.

1. Set X and Y registers to zero.
2. Register select rotary switch = 1
3. Register group rotary switch = XYCN (X and Y condition)
4. Results = 000004 (X = Y)

TEST 7

X > Y The contents of the X register is greater than the Y register.

1. Set Y register to zero
2. Register select rotary switch = 2
3. Register group rotary group = x
4. Toggle switches = 000001
5. Depress the load pushbutton
6. Register select rotary switch = 1
7. Register group rotary switch = XYCN
8. Results = 000001 (X > Y)

TEST 8

X < Y The contents of the X register is less than the Y register.

1. Set X register to zero
2. Register select rotary switch = 2
3. Register group rotary switch = Y
4. Toggle switches = 000001
5. Depress the load pushbutton
6. Register select rotary switch = 1
7. Register group rotary switch = XYCN
8. Results = 000002 (X < Y)

TEST 9

MSBX Detect the most significant bit of X

1. Register select rotary switch = 2
2. Register group rotary switch = X
3. Toggle switches = 800000
4. Depress the load pushbutton
5. Register group rotary switch = CP
6. Toggle switches = 000018
7. Depress the load pushbutton
8. Register select rotary switch = 1
9. Register group rotary switch = XYCN
10. Results = 000009 (MSBX and INTOR)

TEST 10

X ≠ 0 and LSUX The X register is not equal to zero (0) and the least sifnificant unit is detected in the X register.

1. Register select rotary switch = 2
2. Register group rotary switch = X
3. Toggle switches = 000001
4. Depress the load pushbutton
5. Resistor group rotary switch = Y
6. Toggle switches = 000000
7. Depress the load pushbutton
8. Register select rotary switch = 1
9. Register group rotary switch = XYST
10. Results = 00000D (X ≠ 0, LSUX and INTOR)

TEST 11

Y ≠ 0 The register is not equal to zero (0)

1. Register select rotary switch = 2
2. Register group rotary switch = Y
3. Toggle switches = 000001
4. Depress the load pushbutton
5. Register select rotary switch = 1
6. Register group rotary switch = XYST
7. Results = 000006 (Y ≠ 0 and INTOR)

TEST 12

This test checks the ability to address the CPN register as a sink.

1. Push clear (Zeros CP)
2. Register select rotary switch = 1
3. Register group rotary switch = CPU
4. Toggle switches = 000003
5. Depress the load pushbutton
6. Register select rotary switch = 2
7. Register group rotary switch = CP
8. Results = 000060

Tests 13, 14 and 15 check the ability to read and write into memory from the console.

TEST 13

INCA. Increment the A register when the INC "A" pushbutton is depressed.

1. Depress clear pushbutton
2. Register select rotary switch = 2
3. Register group rotary switch = A
4. Depress the INCA pushbutton seven (7) times
5. Results = 000070

TEST 14

Write Memory Store 24 is starting at S-Memory Address Zero (0).

1. Register select rotary switch = 2
2. Register group rotary switch = MAR(A)
3. Toggle switches = 000000 (Address)
4. Depress the load pushbutton. (This action selected address zero)
5. Register group rotary switch = write
6. Toggle switches = FFFFFF (Write Data)
7. Depress Read/Write pushbutton
8. Results = FFFF00

TEST 15

Read the 24 bits that has been written in memory starting at memory address zero.

1. Register select rotary switch = 2
2. Register group rotary switch = READ
3. Toggle switches = 000000
4. Depress Read/Write Pushbutton
5. Results = FFFFFF

NOTE: Tests 14 and 15 may be done using any available memory location by setting the desired starting address with the console switches. This is done in Step 3 in Test 14. Different data configurations may be written by setting the 24 console switches to the desired patterns in Step 6 of Test 14.

DYNAMIC TESTS

The dynamic tests consist of software subroutines that exercise the processor with sequences of instructions. The results of these sequences are checked against proper responses. Any negative response to these sequences is an error condition. A positive response will indicate that no errors exist and the central system is operational.

There are three (3) tests for the Central System. Two tests are for the processor and the other test is for the nory. S-Memory. They are loaded in the Maintenance Test Routine (MTR) Mode and executed in the S-Memory.

When running these dynamic tests, refer to the associated documentation that accompanies them for the correct operational procedures. If any error occurs during the performance of these tests, refer to Section V for the maintenance procedure of the failing section.

MEMORY ARRANGEMENT

The memory storage card backplane is part of the processor backplane (See Figure VI-1). This backplane is pre-wired to handle from minimum to maximum memory size. Memory size will be from 16,384 bytes to 56,536 bytes in increments of 8,192 bytes. Each fully loaded or populated storage card will contain 8,192 bytes of storage. The storage cards must be installed in pairs. From this it is seen that with 2 fully populated storage cards the memory size would be 16,384 bytes or 2 fully populated cards containing 8,192 bytes. In order to obtain only 8,192 bytes of storage it is necessary to install 2 half populated cards. These will contain rows "0" and I. Rows 2 and 3 will be omitted (See Figure VI-2).

MEMORY POWER

Memory power is supplied by the main power supply (+4.75 and -2V) and 3 small power supplies (-5V, 20V and 23.5V). The three power supplies are mounted behind the console front panel. These will handle the current requirements of a minimum to maximum memory without any adjustments.

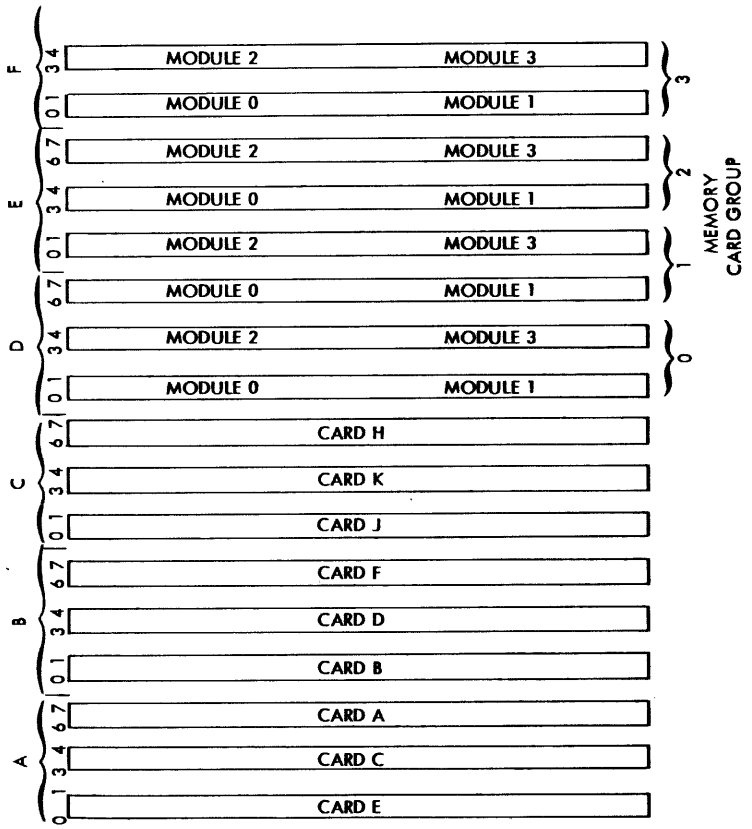


Fig. VI-1 "S" MEMORY PROCESSOR BACKPLANE VIEW

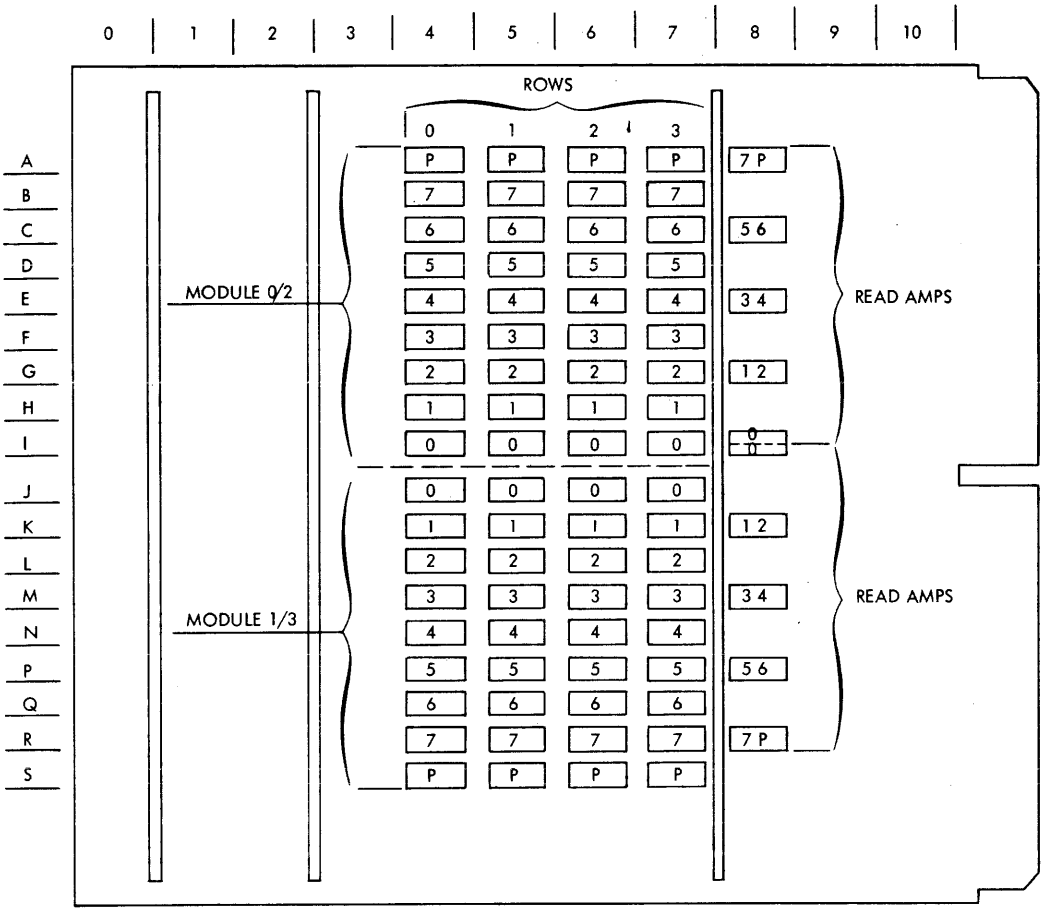


Fig. VI-2 MEMORY "A" STORAGE CARD

EXPANSION KITS

There are three means of expansion. They are as follows:

"S" Memory Adapter	What it consists of
1675 0879	Contains 2 fully populated storage boards and media packages (schematics board layout, etc.)
1675 0887	Contains 2 half populated storage boards and media package
Kit Number	
1675 0895	Contains seventy-two 18 pin MOS memory chips and media package

See Memory Expansion for installation of any of the kits.

MEMORY EXPANSION

The memory can be expanded in increments of 8K bytes up to a total of 64K bytes. If it ever becomes necessary to expand the memory, the following procedure is recommended.

A. Run memory test 2207 1823. (Refer to confidence routines.) This should verify that the present memory is functioning properly. The reason this is advisable is your present program might not be exercising all of memory. This should prove any untested or unused areas within memory.

B. Power the system down.
C Refer to Figure VI-3 to determine the expansion kits needed.

Adapter #1675 0879 = 2 fully populated cards
Kit #1675 0895 = Enough chips to fully populate 2, 1/2 populated cards
Adapter #1675 0887 = 2 half populated cards

Present Memory Size	Boards and Population		Expanded Memory Size	Boards and Population		√ Adapter or Expansion Kit Needed to Expand		
	Half	Full		Half	Full	1675 0895	1675 0887	1675 0879
8K	2	0	16K	0	2	1		
			24K	2	2			1
			32K	0	4	1		1
			40K	2	4			2
			48K	0	6	1		2
			56K	2	6			3
			64K	0	8	1		3
16K	0	2	24K	2	2		1	
			32K	0	4			1
			40K	2	4		1	1
			48K	0	6			2
			56K	2	6		1	2
			64K	0	8			3
24K	2	2	32K	0	4	1		
			40K	2	4			1
			48K	0	6	1		1
			56K	2	6			2
			64K	0	8	1		2
32K	0	4	40K	2	4		1	
			48K	0	6			1
			56K	2	6		1	1
			64K	0	8			2
40K	2	4	48K	0	6	1		
			56K	2	6			1
			64K	0	8	1		1
48K	0	6	56K	2	6		1	
			64K	0	8			1
56K	2	6	64K	0	8	1		
64K	0	8	The system is not configured for further expansion.					

Fig. VI-3 MEMORY EXPANSION

D. Do this step if your present memory has any one-half populated storage cards which need to be expanded to fully populated storage cards.
   1. Increased memory capacity is accomplished by simply inserting 36 semiconductor memory chips (Part Number 1674 5150) into the 36 sockets defined by the following index locations: A6, A7, B6, B7, C6, C7, D6, D7, E6, E7, F6, F7, G6, G7, H6, H7, I6, I7, J6, J7, K6, K7, L6, L7, M6, M7, N6, N7, P6, P7, Q6, Q7, R6, R7, S6, S7.
   2. Remove the stick-on label for the depopulated assembly (1673 5086). This will expose the part number for the fully populated assembly (1675 1562).
   3. Since the memory storage board was factory tested as a fully populated version, and since the memory chips (1674 5150) were factory tested, an operational assembly should result from the mating of these parts.

E. Refer to Figure VI–4 to determine where storage boards go.

F. Insert the storage boards into their proper locations.
   NOTE: If there are any one-half populated cards, they will be to the left of all others as viewed from the frontplane side.

G. Add jumpers to jumper chip location D2 of processor Card H and chip location I6 of Processor Card E as follows:

Memory Size	Card H Chip D2 Jumper				Card E Chip 16 Jumper		
8K	R-S				G-H		
16K	R-S	G-H			F-J		
24K	F-J	R-S			G-H	F-J	
32K	F-J	G-H	R-S		E-K		
40K	E-K	R-S			G-H	E-K	
48K	E-K	G-H	R-S		F-J	E-K	
56K	E-K	F-J	R-S		G-H	F-J	E-K
64K	E-K	F-J	G-H	R-S	D-L		

H. Turn Power on.

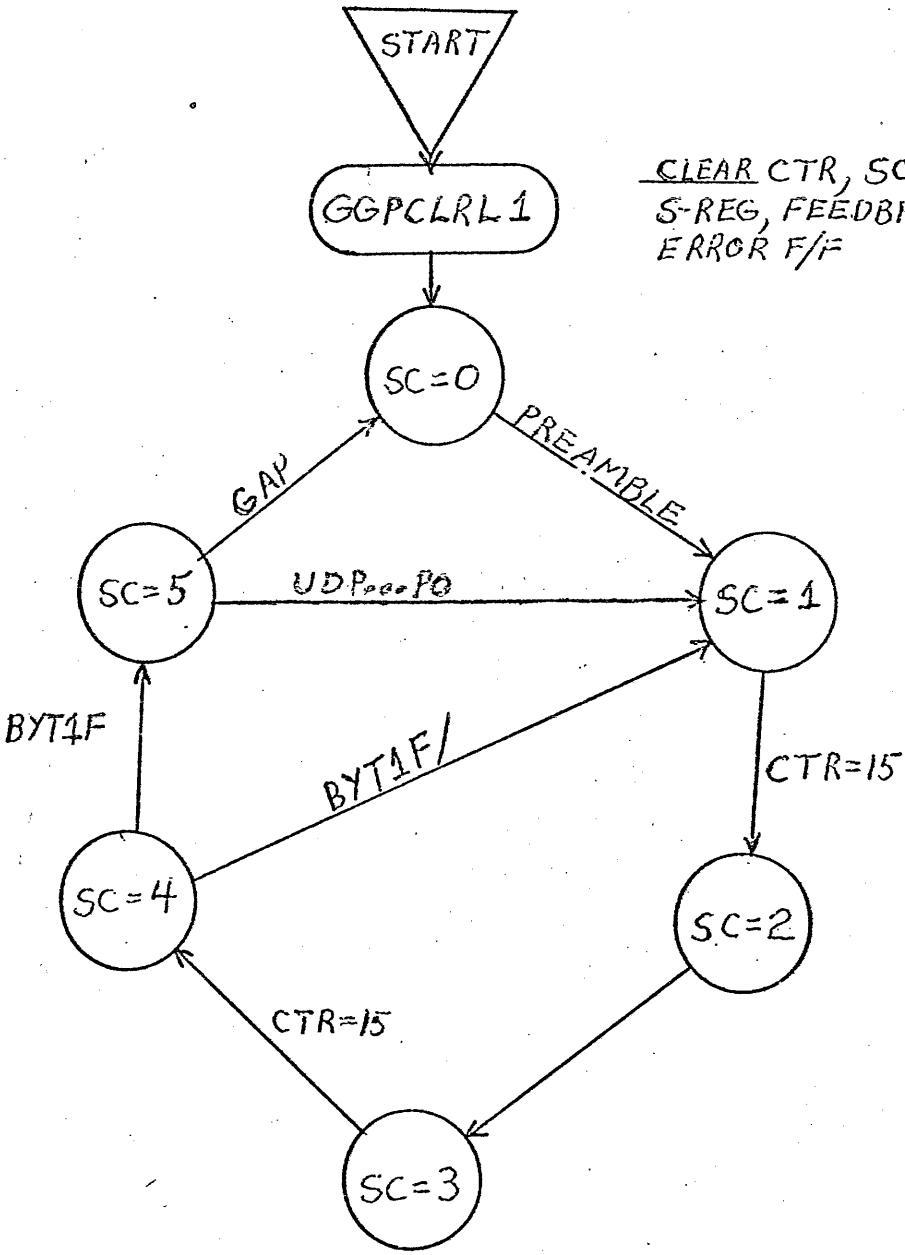
I. Verify memory backplane voltages as follows:
   YD0A = +23V
   YD1A = +19V
   XD0Z = -5V
   XD0A = +4.85V
   YD0Z = -2.05V

J. Check memory timing as outlined in Section IV and adjust if necessary.

K. Run memory test. For any failures refer to Section V of this manual.

Memory Size	Number of Cards	Number of Fully Populated Cards	Card Locations See Table VI-1	Number of Half Populated Cards	Card Locations See Table VI-1
8K	2	0		2	D0/1 D3/4
16K	2	2	D0/1 D3/4	0	
24K	4	2	D0/1 D3/4	2	D6/7 E0/1
32K	4	4	D0/1 D3/4 D6/7 E0/1	0	
40K	6	4	D0/1 D3/4 D6/7 E0/1	2	E3/4 E6/7
48K	6	6	D0/1 D3/4 D6/7 E0/1 E3/4 E6/7	0	
56K	8	6	D0/1 D3/4 D6/7 E0/1 E3/4 E6/7	2	F0/1 F3/4
64K	8	8	D0/1 D3/4 D6/7 E0/1 E3/4 E6/7 F0/1 F3/4	0	

Fig. VI-4 MEMORY SIZE


START
GGPCLRL1
CLEAR CTR, SC, U-REG, S-REG, FEEDBK F/F, BYT1F F/F, ERROR F/F
SC=0
PREAMBLE
GAP
SC=5
UDP...PO
SC=1
BYT1F
BYT1F/
CTR=15
SC=4
SC=2
CTR=15
SC=3

CASSETTE LOGIC

Cassette Logic Data

Forward drive to the cassette is initiated by executing a 2E Cassette Control Micro with a Start variant. Forward drive continues provided TPREDYL (Tape Ready) remains true until a 2E Micro with a stop variant is executed or an inter-record gap on the tape is reached. Execution of the Cassette Start Micro sets START.L F/F. With Gap and TPREDYL both true, forward drive is applied to the cassette. Gap and START.L give GGPCLRL1 (Gap or General Clear). The leading edge of the first TPCLK.L1 (Tape Clock) will force Gap false.

Cassette Sequence Counts

SC=0 Input data from tape is shifted into the S-Register with TPCLK1 and the Counter is incremented with each bit shifted in. When the Preamble is decoded, the Sequence Counter is incremented, CTR is reset and FEEDBACK F/F is set. If the Counter equals 15 before PREAMBLE is decoded, then the ERROR F/F is set.

SC=1 The Data Byte is shifted into the U-Reg and the S-Reg with TPCLK1 and then FECC is shifted into the S-Reg. CTR is counted with each TPCLK1. When CTR=15 then SC is incremented with the next TPCLK1.

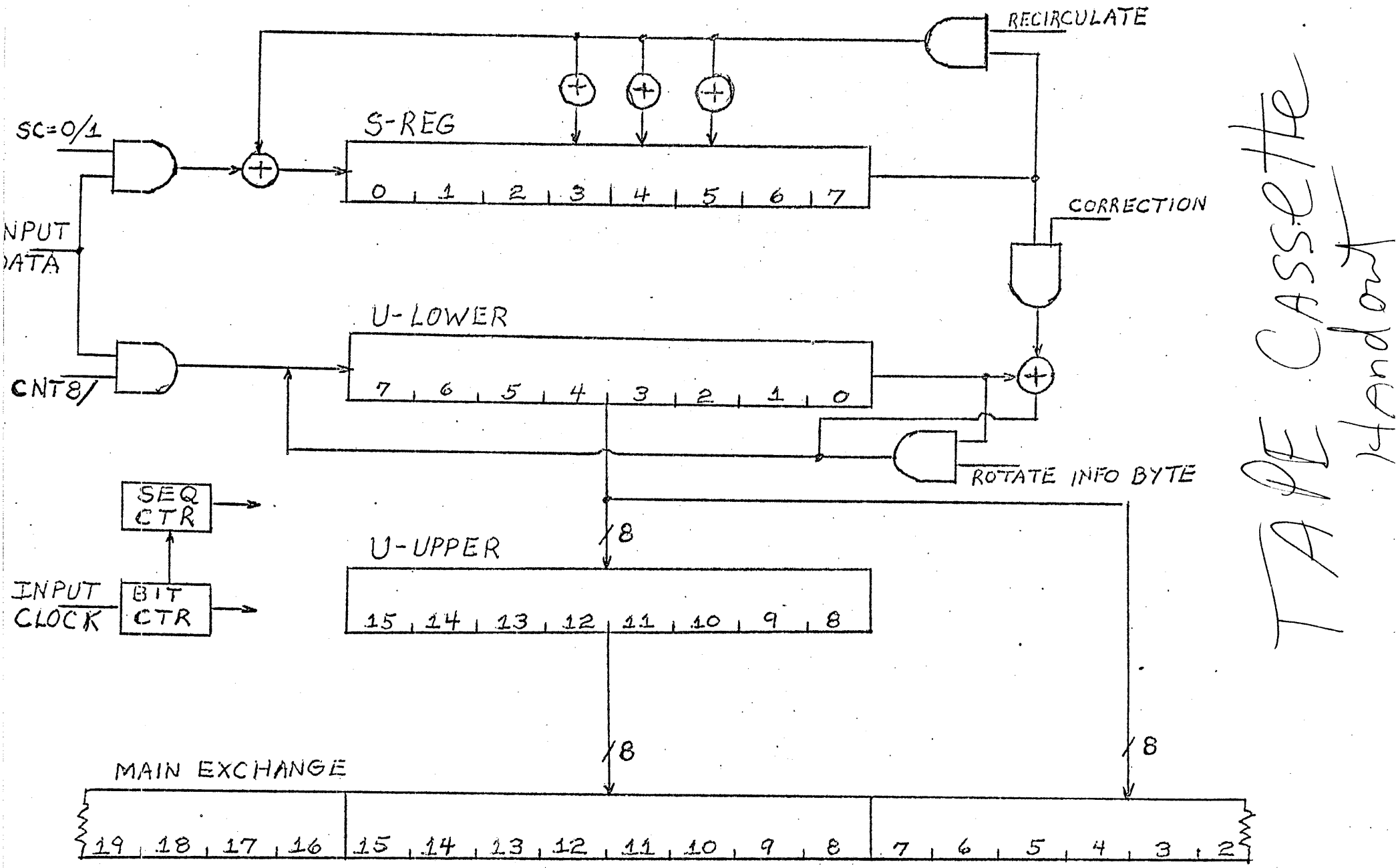
SC=2 True for one system clock pulse. The S-Reg is shifted one position and the FEEDBACK F/F is reset if S-Reg indicates an ERROR FREE condition.

SC=3 U-Reg lower is rotated eight positions (one complete rotation), S-Reg is shifted eight positions and the CTR is incremented by successive DSCPM's. When the S-Reg indicates it is ERROR FREE (the low 5 bits,SR0,1,2,3,4 are equal to zero) then FEEDBACK F/F is reset. The U-Reg is again rotated and the S-Reg shifted. The input to the U-Reg is corrected by exclusively-Oring with S-Reg data as rotation takes place. At CTR=15 the SC is incremented.

SC=4 If this is the first byte of the micro instruction to be read (BYT1F/ is true) then the U-Reg lower is D-Set into the U-Reg upper, BYT1F is set and the SC is set to SC=1.

If this is the second byte to be read (BYT1F is true) then SC is incremented.

SC=5 UDP...P0 (U-DATA Present) is set to indicate to the Processor that a Micro has been assembled in U-Reg and BYT1F is reset. If Gap is encountered, SC are set to "0"; if not,then SC are set to "1".



TAPE Cassette Handpunch

THE CASSETTE

CASSETTE

In addition to the storage of incoming data from the cassette, the cassette logic contains special circuitry to enable correction of data bytes containing errors in a burst of up to 3 consecutive bits.

The format of the tape is as shown on Fig. 1. The first byte read is the PREAMBLE byte which must be recognized by the logic before loading of data will take place. The PREAMBLE byte is hexadecimal AA with the Least Significant Bit (L.S.B.) leading. Following is the first Data Byte with the L.S. Bit of the Least Significant Digit of the byte leading. Following the Data Byte is a unique Forward Error Correction Character (FECC) associated with the Data Byte just read. An error in the Data Byte up to a maximum of a 3 bit burst can be corrected by the FECC and any error in the FECC up to 3 consecutive bits will not effect the data. Any error which can not be corrected, such as bits lost in the Data Byte and FECC, are flagged as a parity error. At the end of Data is a CRC character of 16 bits (Cyclic Redundancy Check) and a POSTAMBLE of HEX AA. The logic does not utilize the CRC or POSTAMBLE.

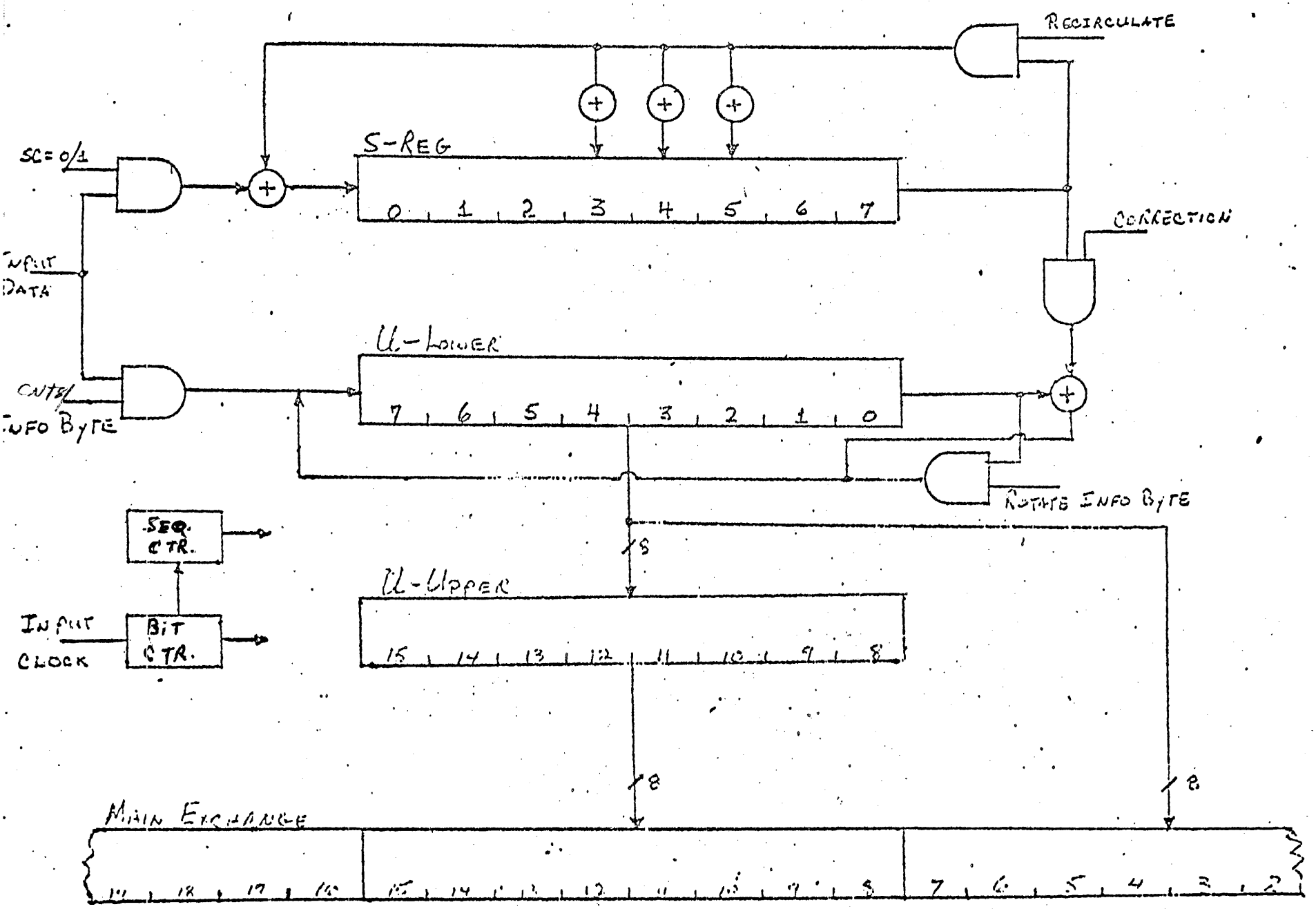
The cassette logic is located on Card L, Pages 5, 6, 7 and consists of the following major components:

U-REGISTER: A 16 bit register used to store one micro instruction read from tape. The U-Reg consists of two halves. The lower half, Bits 0 to 7, are RFBn'S operating in the D-Set mode. Input data from tape enters at URD07 (U REG BIT 7) and is shifted down to URD00. U Reg lower may also be rotated and the data modified as rotation takes place. When the first data byte is error free it is gated into two LFAn'S operating in D-Set Mode which makes up the upper half of U Reg Bits 08 to 15.

S-REGISTER: An 8 bit register comprising two RFBn'S operating in D-Set mode. Input data from tape enters at SR0 and is shifted up to SR7. As the S-Reg. is shifted the contents may be modified by using two AFAN's to EXCLUSIVE OR THE INPUT, SR2, SR3, SR4 as these levels are shifted up into positions SR0, SR3, SR4, SR5. The outputs of the S-Register are also used to decode the PREAMBLE byte and an ERROR FREE condition.

SEQUENCE COUNTER (SC): A counter used to count from 0 to 5 to sequence the operation of the cassette logic.

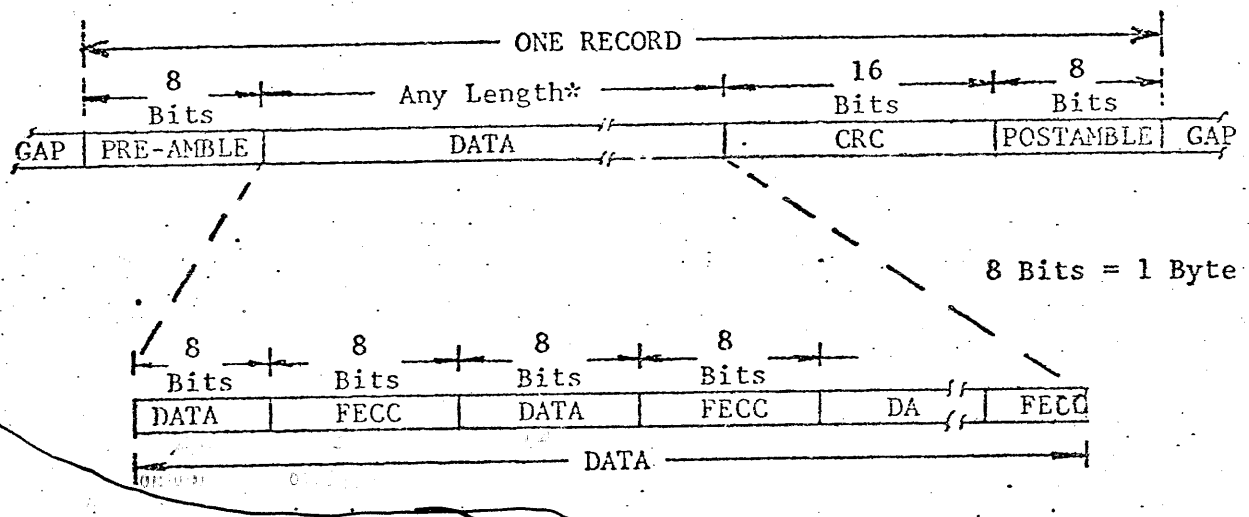
COUNTER (CTR): Counts from 0 to 15 and indicates to the logic the bit being shifted.


RECIRCULATE
S-REG
0 1 2 3 4 5 6 7
SC = 0/1
CORRECTION
INPUT DATA
U-LOWER
7 6 5 4 3 2 1 0
CNTS/ INFO BYTE
ROTATE INFO BYTE
SEQ. CTR.
8
U-UPPER
15 14 13 12 11 10 9 8
INPUT CLOCK
BIT CTR.
8
8
MAIN EXCHANGE

C. THE CASSETTE

The cassette used in the B1726 is the same type of tape-drive as used on the B1712/14 systems. It is also mounted on the console panel and includes the drive logics and the read amplifiers. The data-handling logic is located on the processor card L and is connected to the cassette via a front plane ribbon cable.

The tape format is shown below:



*Data length (which includes FECCs) must be modulo four bytes, i.e. 400 data bytes plus 400 FECC bytes is good, 97 data bytes plus 97 FECC bytes is not allowed.

A data-byte is always followed by a FORWARD ERROR CORRECTION CHARACTER (FECC), whose configuration depends on the preceeding data byte. The number of data bytes followed by their respective FECC's is only limited by the length of the tape. Using this FECC, the data handling logic is capable of recovering from a loss of one to three consecutive bits during the read of a data byte. Any other read error would result in a parity error.

Cyclic redundancy check and postamble bits are not required by the logic and are discarded. For further information refer to cassette detailed description.

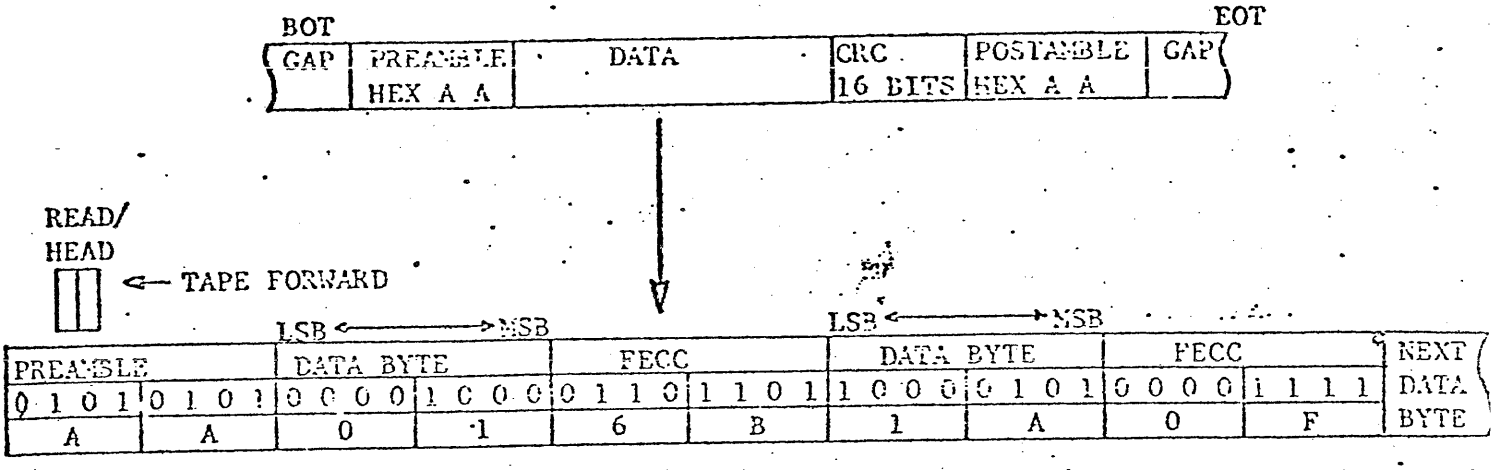


FIG.1 CASSETTE TAPE FORMAT SHOWING A 1C MOVE X to Y MICRO INSTRUCTION (10A1) as it would appear on Tape.

FEEDBKL. FLIP FLOP: When set allows modification of S-Register to determine if the Data Byte is ERROR FREE. When an ERROR FREE condition is determined the flip flop is reset and allows correction, if necessary, of the U-Register to take place.

BYTIF.L. FLIP FLOP: When set indicates that the second byte of the micro instruction is being read and the first byte is all ready loaded in U-Register.

CASSETTE LOGIC DATA AND CLOCK TIMING (Fig. 2)

Forward drive to the cassette is initiated by executing a 2E Cassette Control micro instruction with a Start variant. Forward drive continues provided TPREDYL. (Tape Ready) remains true until a 2E micro with a Stop variant is executed or an inter-record gap on the tape is reached. Execution of the Cassette Start micro sets START.L. flip flop. With GAP and TPREDYL. both true forward drive is applied to the cassette. GAP and START.L. give GGPCLRL1 (Gap or General Processor Clear). This pulse resets the COUNTER, SEQUENCE COUNTER, S-REG., U-REG., FEEDBKL. flip flop, BYTIF.L. flip flop, ERROFL. and PE3 flip flop. The leading edge of the first TPCLK.L1 (Tape clock) will force GAP false. GAP is the reset output of a TAON with a 650 μSEC delay. Each successive TPCLK.L1 will retrigger the TAON until 650 μSECS after the leading edge of the last TPCLK.L1, GAP will again go true. TPCLK.L1 sets SYNCLKL. flip flop which sets CLKTRUL. flip flop (Tape Clock True). A data pulse from the cassette on the TRIL line is inverted and, with CLKTRUL. true, will be stored in the IDATASL1 flip flop (Input Data Stored). After approximately 1 06 μSECS TPCLK.L1 goes false and SYNCLKL. flip flop is reset. With SYNCLK1 true and CLKTRU true then TPCLKIL1 (Tape Clock Isolated) is true. The next DSCPM will reset CLKTRUL. flip flop and TPCLKI will go false. TPCLKI is the clock used to sample and control the cassette logic. It is one system clock wide and occurs at the end of every Tape Clock.

Dependant on the Sequence Count at which the logic is, TPCLKI true enables SRSHFTL. (S-REG Shift Control) SRCLK (S-REGISTER Clock) URSHFTL. (U-REG. Shift) LOUCLK (Lower U-REGISTER Clock) and increments the COUNTER as indicated in the timing chart, Fig. 2.

SEQUENCE COUNTER (Fig. 3)

The Sequence Counter cycles through six sequences 0 to 5 and during each of these sequences a specific function is performed on the data read from tape.

SC = 0: Input data from tape is shifted into the S-Register with TPCLKI and the COUNTER is incremented with each bit shifted in. When the PREAMBLE is decoded the Sequence Counter is incremented, CTR is reset and FEEDBKLF.F. is set. If the COUNTER equals 15 before PREAMBLE is decoded then ERROR flip flop is set.

SC = 1: The Data Byte is shifted into the U-Reg and S-Reg with TPCLKI and then FEC character is shifted into the S-Reg. CTR is counted with each TPCLKI. When CTR = 15 then SC is incremented with the next TPCLKI.

SC = 2: True for one system clock pulse. The S-Reg is shifted one position and the FEEDBACK F.F. is reset if S-Reg indicates an ERROR FREE CONDITION.

SC = 3: U-Register lower is rotated eight positions (one complete rotation), S-Register is shifted eight positions and the CTR is incremented by successive DSCPM's. When the S-Register indicates it is ERROR FREE (the Low 5 bits, SR0, 1, 2, 3, 4 are equal to zero) then FEEDBACK F.F. is reset. The U-Reg is again rotated and the S-Reg shifted. The input to the U-Reg is corrected by EXCLUSIVELY ORing with S-Reg data as rotation takes place. At CTR = 15 the SC is incremented.

SC = 4: If this is the first byte of the micro instruction to be read (BYT1F/ is true) then U Reg lower is D-set into U-Reg upper, BYT1F flip flop is set and the SC is set to SC = 1.

If this is the second byte to be read (BYT1F/F.F. is true) then SC is incremented.

SC = 5: UDP (U Data Present F.F.) is set to indicate to the processor that a micro has been assembled in U-Reg and BYT1F is reset.

DETAILED OPERATION (References are to Fig. 4 unless stated otherwise)

As covered in the section CASSETTE LOGIC and DATA TIMING the Sequence Counter is initially reset to zero and with the tape moving FORWARD the logic is waiting for the first TRCP/ (Tape Clock Pulse). The first TRCP/ is inverted to TPCLK.L1 which sets GAP/ true and allows TRIL/ (Tape Read Information Level Not) pulses to be stored in the IDATASL1 (Input Data Stored) flip flop. At the trailing edge of TPCLK.L1 a pulse TPCLKIL1 is produced, which is one system clock wide.

SC = 0	Initial Conditions	FEEDBKL F.F.	Reset
		CTR = 00	True
		S-Reg.	Cleared
		U-Reg.	Cleared
		ERROR F.F.	Reset
		BYT1F	Reset

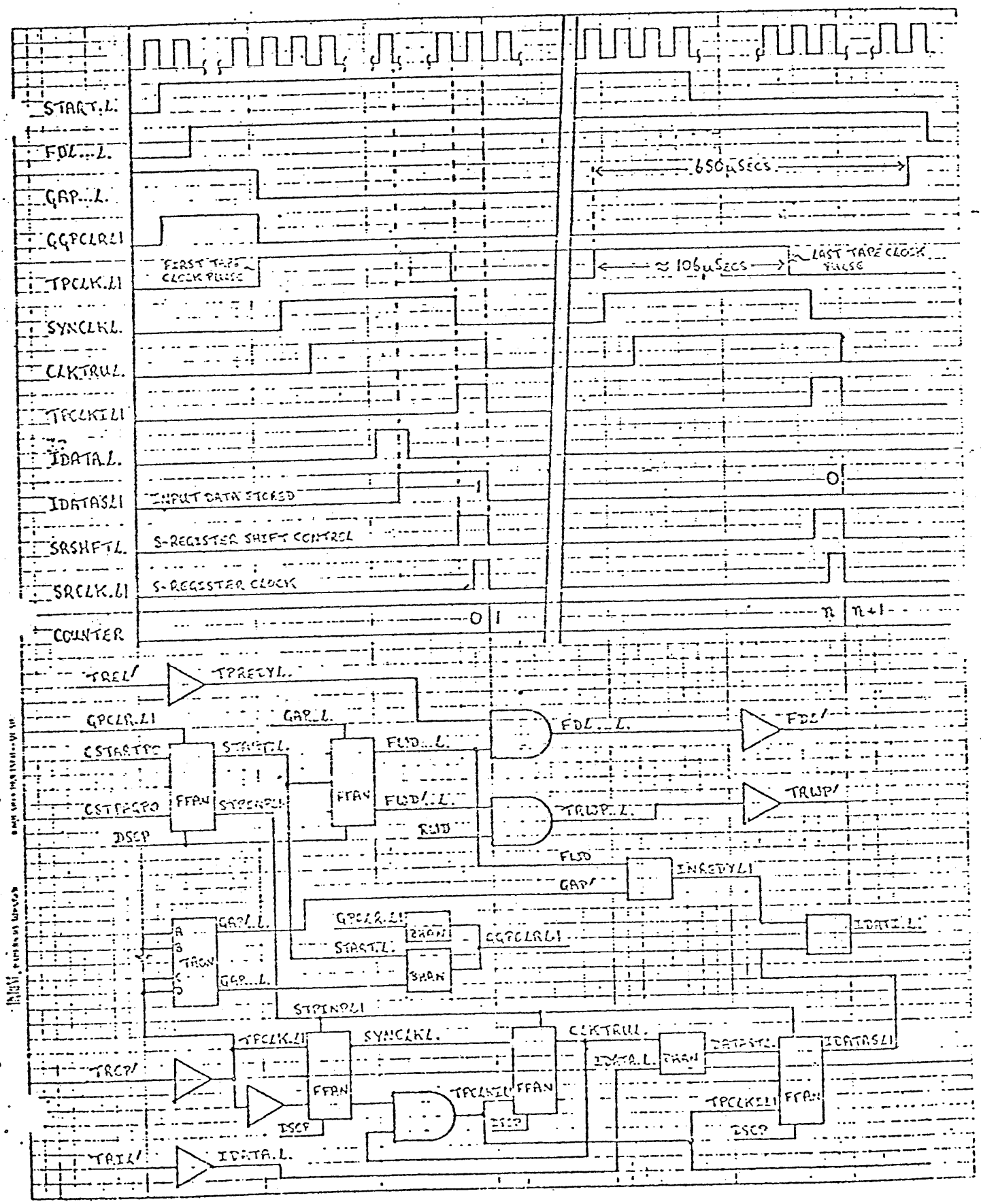


FIG. 2 CASSETTE CONTROL / CLOCK AND INPUT DATA TIMING

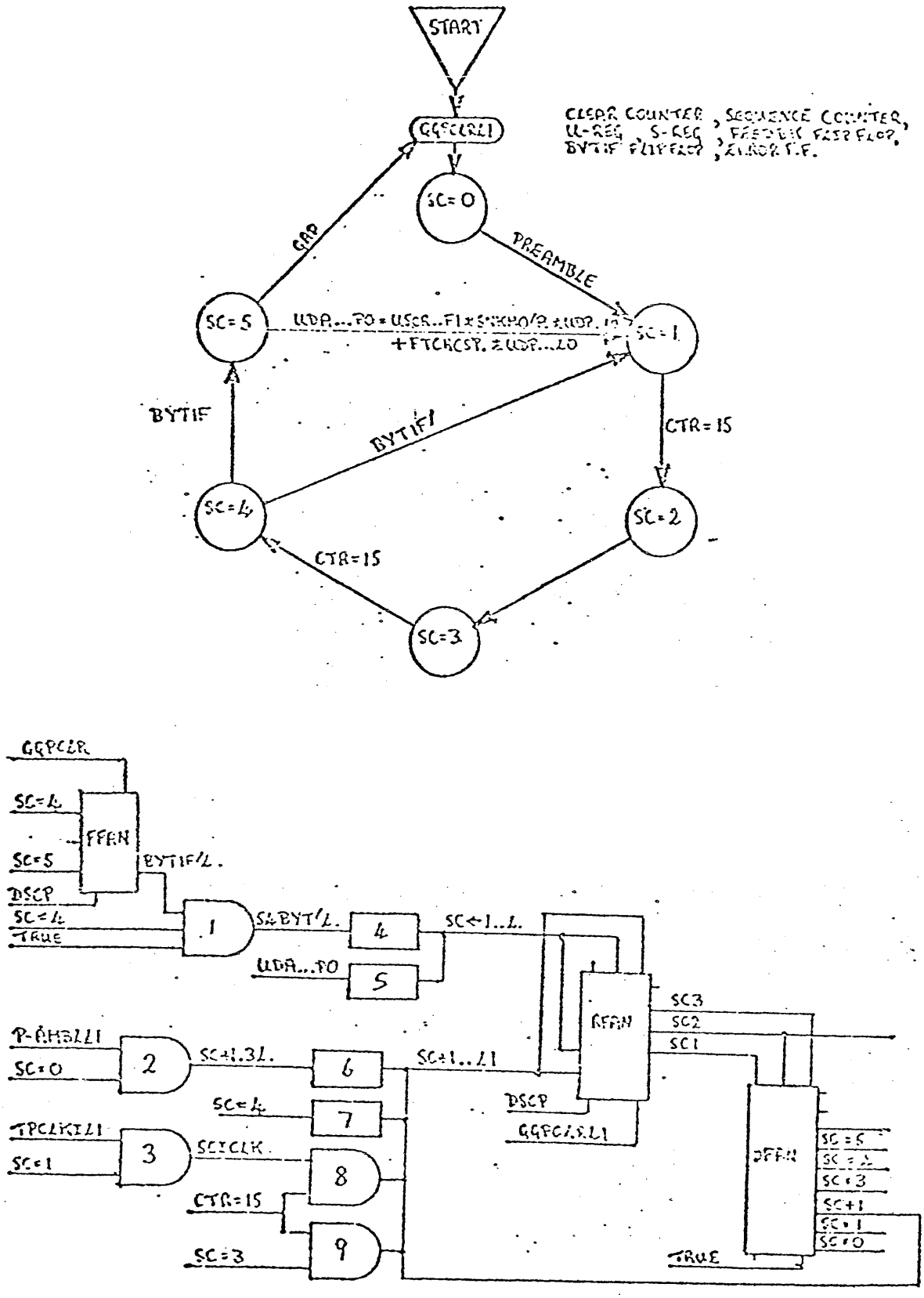


FIG. 3 SEQUENCE COUNTER

TPCLKIL1 enables SRSHFTL. (S-Reg Shift Control) at Gate 7. With the next SCPM a pulse SRCLKL1 (S-Reg Clock) is generated through Gate 18. The trailing (-vz going) edge of SRCLKL1 shifts up the S-Register and sets the Input Data through Gates 1 and 5 into SRO.

SRSHFTL also puts the BIT COUNTER RFAN (32) into ADD mode and one is added to the Counter on the trailing edge of DSCP. The U-Register is not shifted at this time as LOUCLKL. (Lower U-Reg. Clock) is held false. Successive TRCP/ pulses from the Cassette generate TPCLKIL1 pulses and Input Data is shifted up the S-Register and the Counter is incremented.

After eight bits of data have been shifted into the S-Register (CTR=8), Gate 17, which comprises three AND gates, an INVERTER and a DFAN, should decode the PREAMBLE BYTE (01010101 - Hex AA). If the Preamble is not decoded then Input Data will continue to be shifted up the S-Register until CTR=15. At CTR = 15, Gate 38 will give SETERFL. true (Set Error F.F.) and the ERROR F.F. will set on the next DSCP.

When P-AMBLL. is decoded from Gate 17 before CTR = 15 then Gate 2 and 6 (Fig. 3) will add one to the Sequence Counter on the trailing edge of the next DSCP.

SC+1.3L. = P-AMBLL1*SC=0

SC+1..L1 = SC+1.3L.

SC+1.3L. true also gives USCLR.L. true (U-Reg. and S-Reg. - Clear) at Gate 21 which puts a true on the CLEAR inputs of U-Reg. and S-Reg. RFBN's and allows the next SCPM to clear the two registers through Gates 25, 26, 18 and 23. Additionally SC+1.3L. true sets the FEEDBKL flip flop 27, and SC+1..L. true gives CLRCTRL. true (Gate 34) and the BIT COUNTER is cleared.

SC = 1 Initial Condtions		
	FEEDBKL F.F.	Set
	S-REG.	Clear
	U-REG.	Clear
	CTR=00	True
	CTR8/	True
	BYT1F	Reset

IDATASL1 during SC = 1 is gated through Gate 1 and 6 to the input of SRO and through Gates 1, 6, 2 and 12 to the input IUR07 (Input U-Reg. Bit 07) of the U-Register. TPCLKIL1 through Gate 4 produces SC1CLKL. (Sequence Counter 1 Clock). SC1CLKL. enables SRSHFTL. at Gate 8 and URSHFTL (U-Reg. Shift Control) at Gate 10. The next SCPM will shift the

S-Register with SRCLKL1 at Gate 18 and the U-Register with LOUCLKL. (Lower U-Reg. Clock) at Gate 23, and 1 will be added to the BIT COUNTER with DSCP. With CTR = 00 true when the first data bit is being shifted SC1CLKL. will also force a "1" bit into SR' through Gate 16. The logic now waits approximately 125 micro seconds for the next TPCLKIL1 to be generated. Input Data will continue to be shifted in the S and U Registers and the BIT COUNTER incremented until the seventh bit has been shifted and the Counter is at 7. At this time the "1" bit that was forced into SR1 at CTR = 00 has been shifted up to SR7. SR7 is true and as FEEBKL. flip flop was set at the beginning of Sequence 1 then Gate 30 is enabled which gives RECIRCL. true. This applies a "1" bit to the EXCLUSIVE OR gates associated with the S-Register. When the next shift takes place INPUT.L1, SR2, SR3 and SR4 will be EXCLUSIVE ORed with "1" bits as they are shifted into SR0, SR3, SR4, SR5.

The next shift takes place with the next TPCLKIL1 pulse. S-Register is shifted up and the data modified, the U-Register is shifted down and the counter is incremented, to CTR8 true. The eight bits of the Data-Byte have now been shifted into S-Register and U-Register. Shifting of U-Register is now disabled at Gate 10 with CTR8/ being false. Tape Input Data continues to be shifted into the S-Register as each TPCLKIL1 pulse is generated and anytime SR7 is true then INPUT.L1, SR2, SR3 and SR4 will be EXCLUSIVELY ORed as it is shifted up. The counter continues to increment until CTR = 15. At this time 15 bits have been shifted through the S-Register since the Preamble. The next TPCLKIL1 pulse shifts in the 16th bit which is the last bit of the FECC, one is added to the Sequence Counter (Gate 3 and 8, Fig. 3) and the Counter is cleared (Gate 34).

SC+1..L1 = TPCLKIL1*SC=1*CTR=15

SEQUENCE COUNT 2	Initial Conditions	SC2	True
		FEEBKLF.F.	Set
		CTR = 00	True

SC2 is true for one system clock as the SEQUENCE CTR is incremented on the trailing edge of the next DSCP.

SC+1 = SC2*SC3/*SC1/ (Fig. 3)

Gate 9 gives SRSHFTL. true and S-Reg. is shifted one position with SCPH through Gate 18.

With SC2 true a test is made to see if the Data Byte read from tape is ERROR FREE. After the Data Byte and FECC have been shifted through and manipulated in S-Register during SC=1, the lower five bits of S-Reg, SR0, SR1, SR2, SR3 and SR4 should be zero. If the lower 5 bits are 0 then the

signal LO5=0 from Gate 17 will be true. ENDIVL. (END) from Gate 24 will be true. This will put a false in Gate 29 making FDBACKL. false and disabling Gate 30. S-Register will be shifted without modifying the contents regardless of whether SR7 is TRUE or FALSE, and FEEDBKL. flip flop will be reset. If the lower five bits are not all zero then an error condition exists. In this case S-Register contents will be modified if SR7 is TRUE when the shift take place. INPUT.L1 is now held false because neither SC=0 or SC=1 are true at Gates 5 and 6.

SC + 1 being true holds the counter reset when the shift takes place (Gate 34).

SC = 3 Initial Conditions

SC = 3	True
SC2	True
CTR = 00	True

SC2 being true enables SRSHFTL. at Gate 9 and the S-Reg is shifted by successive SCPM's through Gate 18. INPUT.L1 to S-Reg. is held false.

SC = 3 true enables URSHFTL at Gate 11 and U-Reg. is rotated by successive SCPM's. The rotation path of the data is through GATES 3 and 12. With each shift of the S-Reg SRSHFTL true enables one to be added to the counter with each DSCP.

If the data in S-Register was ERROR FREE in Sequence Count 2 then in SC = 3 "0" bits will shift into S-Register and there will be no modification of the contents.

If it was determined that an error existed in SC = 2 by LO5 = 0 being false then S-Reg.contents are modified at each shift if SR7 is true. After each shift S-Reg. is tested to see if it is now ERROR FREE. If it is LO5 = 0 will be true, no further modification of S-Reg. will take place as it is shifted and FEEDBKL. flip flop will be reset.

Shifting and rotation continues until CTR3 is true. At this time U-Register has undergone one complete rotation with the data unchanged. Shifting and rotation continue with the next SCPM but now the rotation path of U-Reg. data is through Gates 41 and 7. Gate 41 is an EXCLUSIVE OR of the signal CORREC.L and the output of BIT 00 of the U-Register.

If during SEQU. COUNT 2 or the first eight shifts of SC=3 the data was determined to be ERROR FREE then L05=0 will be true giving ENDIVL. true at Gate 24. This will enable CORRECL. (Correction Recirculate) to reflect the TRUE or FALSE condition of SR7. During the next eight shifts after CTR8 is true, the input to the U-Reg. is the EXCLUSIVE OR of SR7 and URD00. If L05=0 was TRUE at SC=2 then the S-Reg. will contain all zeros and there will be no change to U-Reg. data as it is rotated. This is the ideal condition indicating that the Data Byte and FECC have been read correctly from tape. If L05=0 came true during the first eight shifts of SC=3 then some correction of U-Reg. data will take place during the next eight shifts. If L05=0 has not yet come true during SC=2 or SC=3 then modification of S-Reg. will take place as it is shifted when SR7 is true, and U-Reg. will rotate with the data unchanged. When L05=0 comes true Gate 31 is enabled and URD00 is EXCLUSIVELY ORed with SR7 and shifted into the U-Reg. with the next SCPM. FEEBKL. flip flop will be reset. When the CTR=15 is true the next System Clock will rotate, and correct if necessary, the U-Reg., shift the S-Reg., increment the Sequ. Ctr. to SC=4 (Gate 9, Fig. 3) and clear the counter.

SC=4

SC=4 is true for one system clock.

SC + 1..L. = SC=4 (Gate 7, Fig. 3).

If FEEDBKL flip flop was not reset in SC=2 or SC=3 then the data in U-Reg. lower was not read correctly from tape and was not able to be corrected by the FECC. FDBACKL. will be true and the ERROR F.F. will be set through Gate 37.

If FEEDBKL. is reset then the data is ERROR FREE.

If this is the first Data Byte (Byte 0) read from tape then BYT1F/ (BYTE 1 flip flop not) will be true. S4BYT/L (Sequ Count 4 Byte (1) not) will be true at Gate 1, Fig 3. SC←1..L. and SC + 1..L. are true, Gate 4 and 7, Fig. 3. This will put the Sequ Counter RFAN. in SHIFT UP mode and the next DSCP will set SC = 1.

S4BYT/L. true will also place the U-Reg. Upper LFAN's in D-Set Mode (Gate 15) and DSCP will set the U-Reg. lower data into U-Reg Upper.

BYT1F F.F. will be set (Fig. 3).

The logic returns to SC=1 and waits for the next Tape Clock Pulse.

If BYT1F F.F. is set when entering SC=4 then no further action takes place and the Sequ Ctr is incremented to SC=5 (Gate 7, Fig. 3).

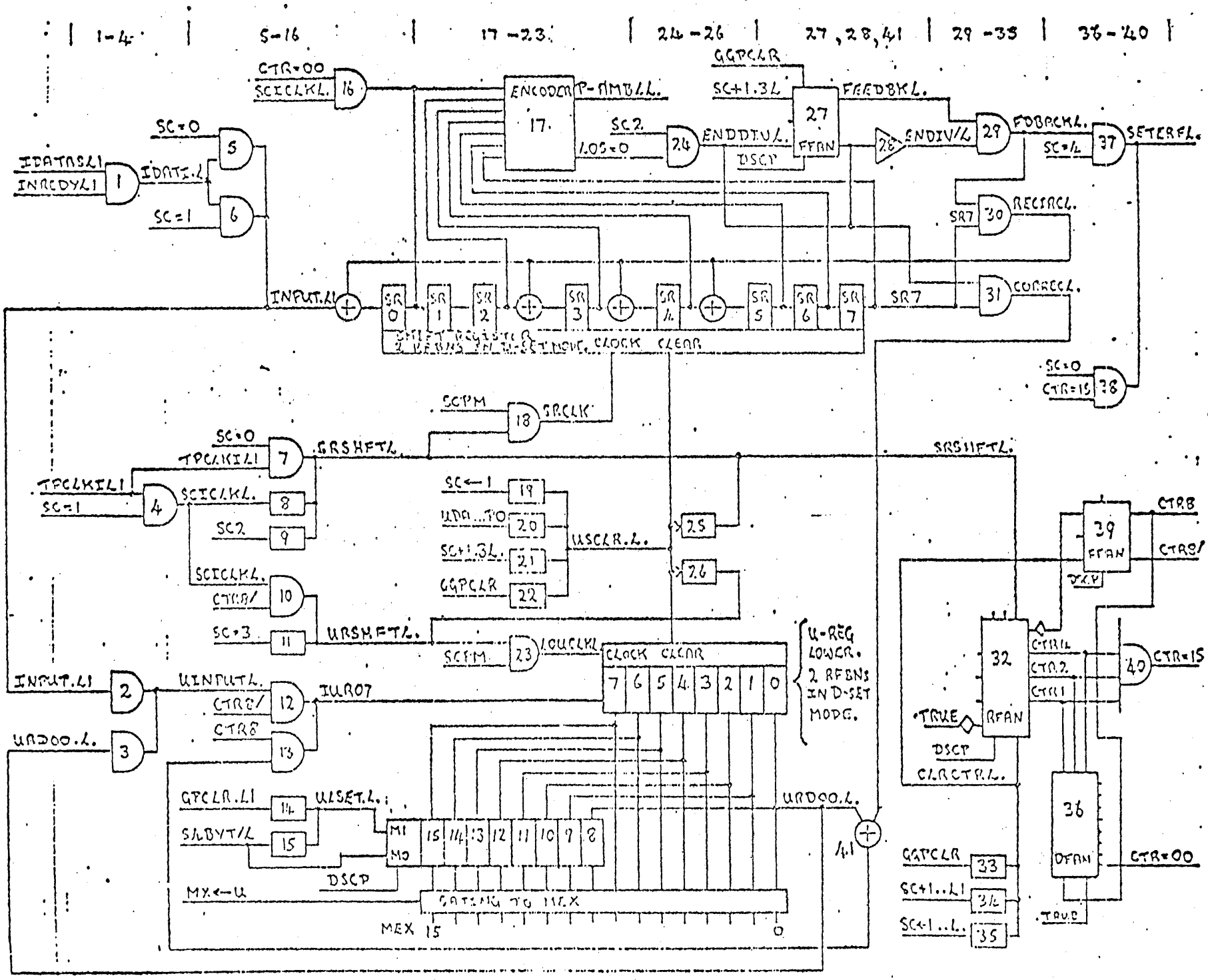


FIG. 4 DATA CONTROL

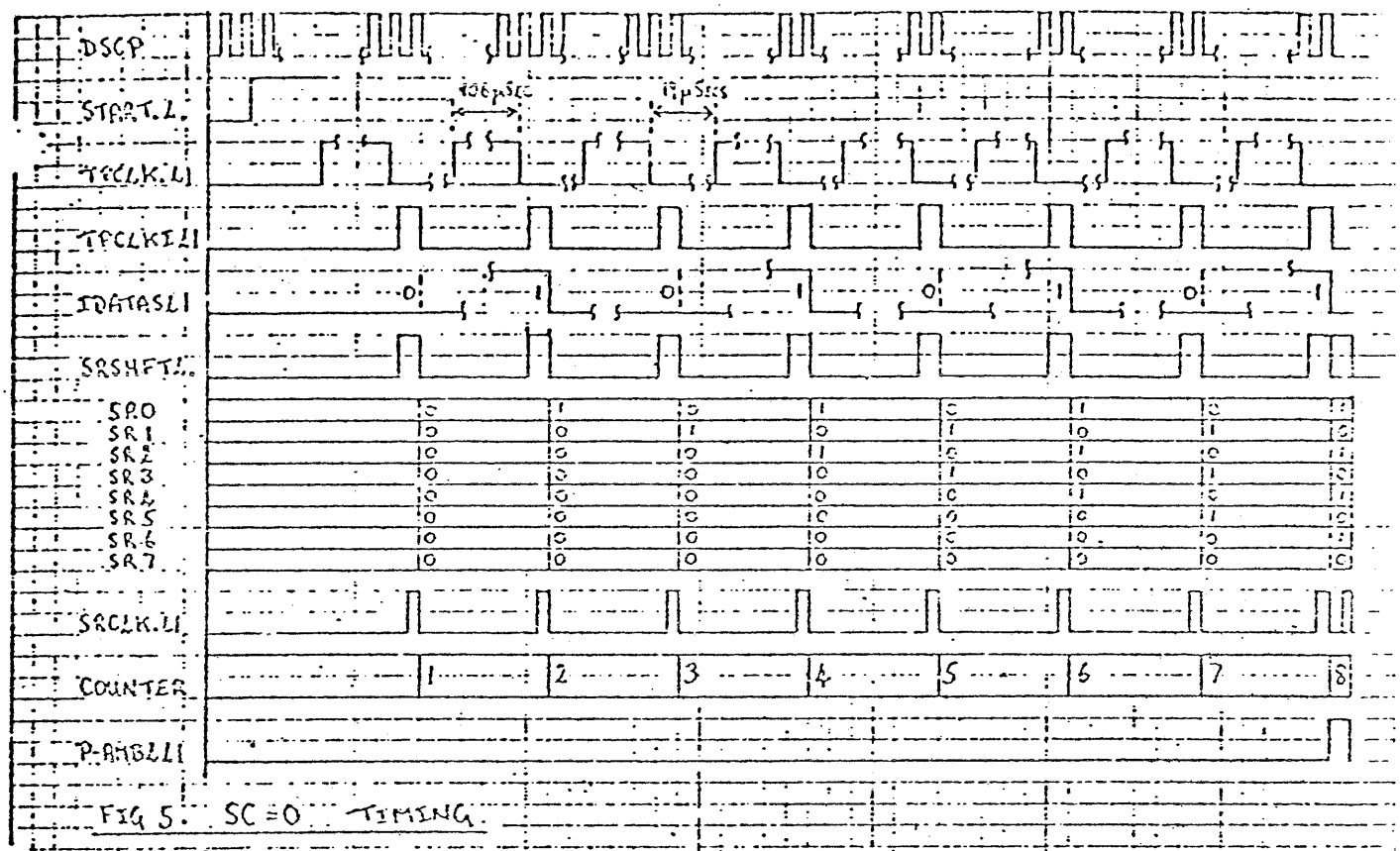


FIG 5. SC=0 TIMING

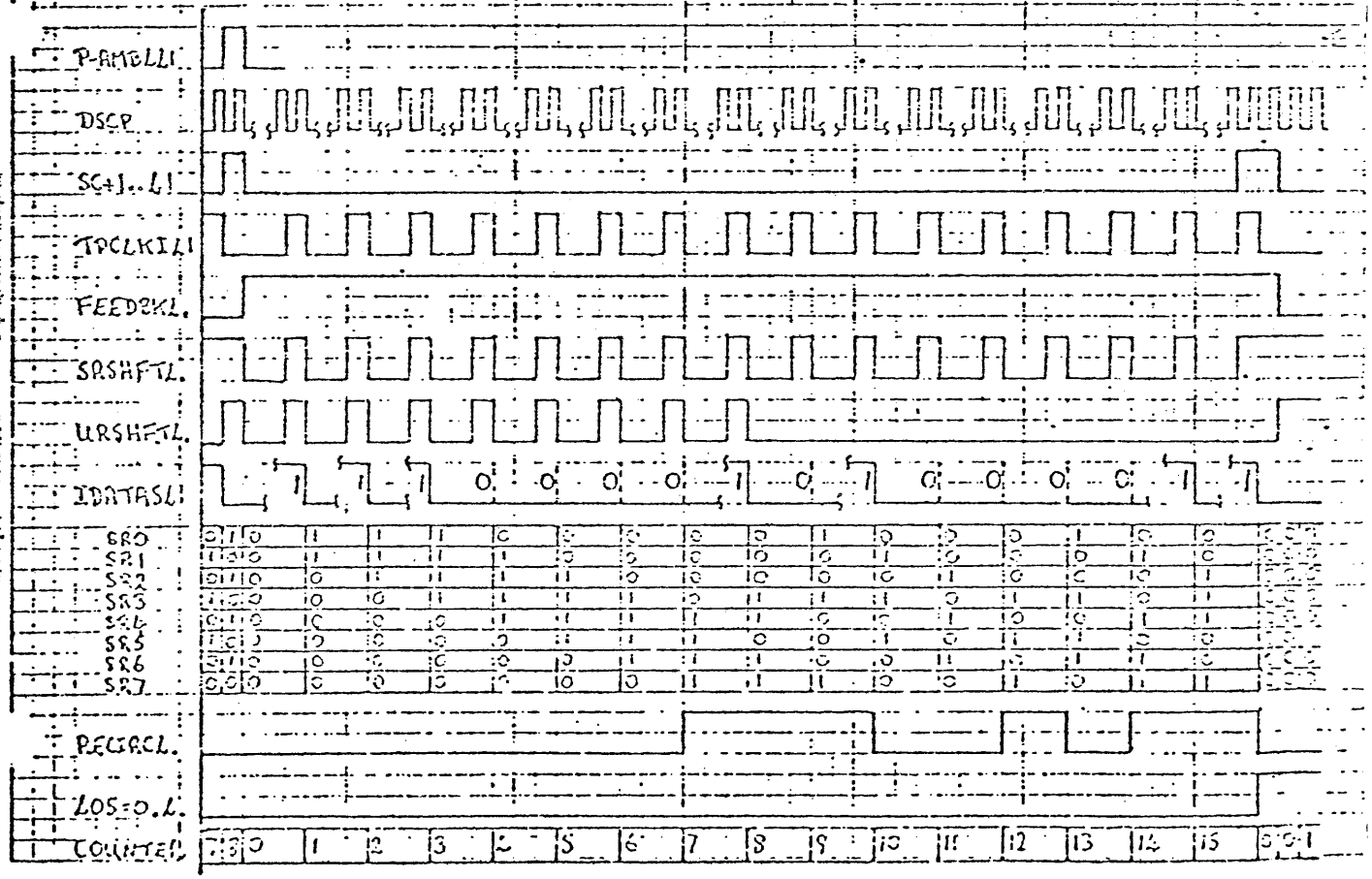


FIG. 6 SC=1 TIMING

SC=5

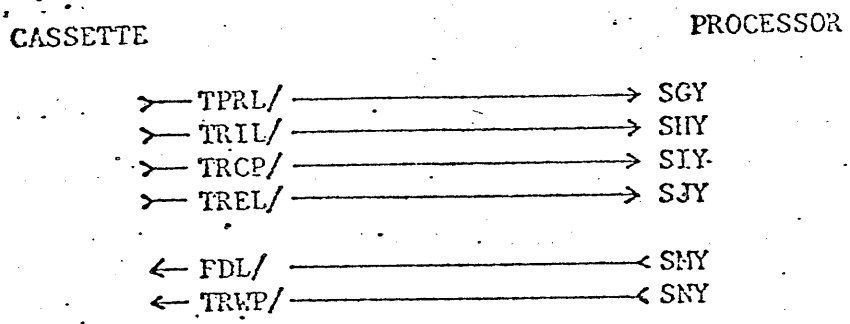
UDP (U Data Present) flip flop is set to indicate to the Processor that there is a micro instruction in the U-Reg.

BYTIF.F. is reset in anticipation of reading the first Date Byte of the next micro instruction.

The logic remains in SC=5 until the processor sources the U-Reg. data. This will give UDA...PO true (U Data Accessed) and SC←1..L. true through Gate 5, Fig. 3. The Sequence Counter RFAN will be in the D-Set Mode and the next DSCP will set it to SC=1.

CASSETTE/PROCESSOR INTERFACE:

As installed in the B1726 the cassette is an input device only. The following signals comprise the interface between the cassette drive module and processor card L.



TPRL/ - Tape position ready level. When false (low) the tape is in position to start reading.

TRIL/ - Tape Read Information Level. A -ve going pulse of 0-5 uSEC duration indicating a "1" bit has been read from tape.

TRCP/ - Tape Read Clock Pulse. A -ve going pulse of 100 μSEC duration. During this period a -ve pulse on the TRIL/ line is read as a "1" bit. The absence of a -ve pulse on the TRIL/ is read as an "0" data bit.

TREL/ - Tape Ready Level. When low indicates a cartridge is installed and the cassette drive is ready to receive a tape command.

FDL/ - Forward Drive Level. When low causes the tape to be driven forward.

TRWP/ - Tape Rewind Pulse. The leading edge of this -ve pulse will initiate a rewind cycle.

GLOSSARY OF TERMS - CASSETTE LOGIC:

BOT...L1	Beginning of tape.
CLKTRUL.	"Tape Clock True". Output of CLKTRUL F.F.
CLRCTRL	Clear counter.
CORRECL	Correction recirculate. Part of error detection and correction in cassette.
CTRCO.L.	Counter carry out.
CTR8..L.	Counter equals 8.
CTR=00L.	Counter equal to zero.
CTR=15L.	Counter equal to 15.
CTR#..L1	Counter # F.F.; # = 1, 2 & 4. Output of 3 bit counter register.
CUB000L	CU Binary.
DATASTL.	Data start. Tape input data.
ENDDIVL.	End. Turns off feedback F.F.
ENDIV/L.	End.
FDBACKL.	Feedback. Part of cassette error det. & corr.
FDL...L.	Forward drive level.
FDL1..L1	
FEEDBKL.	Feedback. Turns on feedback gates.
FWD...L.	Forward drive. Output of forward drive flip flop.
GAP...L1	GAP. Indicates presence of a gap on tape being read.
GAPTMEL.	GAP TIMER. Gives gap duration of 650 uSECS.
GAP/..L.	GAP NOT. When true there is no gap but a record.
GGPCLRL1	Gap or Gen. Proc Clear. Start and tap or gen. proc. clear.
IDATASL1	Input Data Stored. Stored tape data.
IDATA.L.	Input Data. Data input from cassette.
IDATI.L.	Input Data Isolted. Controlled data input from cassette.
INPUT.L1	Input (To Shift Reg.).
INREDYL1	Input Ready. Allows to start sampling data from the cassette.

CASSETTE

ISR#..L.	Input Shift Reg. Bit #; # = 0, 3, 4, 5. Corrected shift reg. input.
IUR07.L.	Input at U-Reg. (Bit) 07.
LM4 = 0.L.	Low Micro Operator 4 Bits Non Zero.
LOUCLKL1	Lower U-Reg. Cloc. Non-continuous clock.
L04 = 0.L.	Low (Shift Reg.) 4 Bit value is Zero.
L05 = 0.L.	Low (Shift Reg.) 5 Bit value is Zero.
MX - U..L.	Main Exchange Set Equal to U-Reg.
PE3...L1	(Total) Parity Error.
P-AMBLL1	Preamble.
RECIRCL.	Recirculate. Part of Cassette error det. and correction.
RWD...T1	Rewind. Output of rewind switch on console.
SB0101L.	Shift Reg. Bin. Value Equals 0111.
SB0101L.	Shift Reg. Bin. Value Equals 1111.
SCICLKL.	Sequence Count Clock.
SC + 1..L.	Sequence Count Incremented by One.
SC + 1.3L.	Sequence Count Plus One.
SC 1..L.	Sequence Count Set Equal to One.
SC = #..L.	Sequence Count Equals #; # = 0, 1, 3, 4, 5. Decoded outputs of Sequ. Count Reg.
SC # ...L.	Sequence Count #; # = 1 = 3. Output of 3 bit Sequ. Count Reg.
SETERFL.	Set Error Flip Flop.
SRCLK.L1	Shift Reg. Clock, Non Continuous Clock.
SRSHFTL.	Shift Reg. Control.
SR4 = 0.L.	Shift Reg. Bit 4 = 0.
SR # ...L.	Shift Reg. Output #; # = 0 = 7.
START.L.	Start Cassette Drive. Turns on cassette fwd drive F.F.
STPINPL1	Stop Input (Data) Pulse (Sampling).
SYNCLKL.	Synchronized (Tape) Clock.
SYCLK/L1	Synchronized (Tape) Clock (Flip Flop) Not.
S4BYT/L.	Sequence Count 4 Byte (1) Not.

TPCLK.L1	Tape Clock. Tape clock from cassette unit.
TPCLKIL1	Tape Clock Isolated. This is the clock used to sample and control the cassette logic. It is one system clock wide and occurs at the end of every tape clock.
TPCLK/L.	Tape Clock Inverted.
TPREDYL.	Tape Ready. Protects Forward Drive Level from being turned on when the tape is not ready.
TRWP..L.	Tape Rewind Pulse. Rewinds the tape.
UCOLM3L.	Upper Column 3. Registers of column 3.
UDP...LO	U-Reg. Data Present.
UINPUTL.	U-Reg. Input.
ULSET.L.	U-Reg. Lower (D) Set. D-Set mode for the lower 8 bits of the U-Reg. (8-15).
URSHFTL.	U-Reg. Shift.
USCLR.L.	U-Shift Reg. Clear.
VLIDPEL.	Valid Parity Error.

EXAMPLE:- READ FROM TAPE

1001	0101	1011	0100
9	A	B	2

CTR	IN=01234567	IN=01234567	IN=01234567	
0	100000000	100000000	100000000	
1	011000000	011000000	011000000	SC=1. Data byte and FECC are shifted through S-Register. Data byte is shifted into U-Register.
2	001100000	001100000	001100000	
3	100110000	100110000	XOR 00110000	
4	010011000	010011000	000011000	
5	101001100	101001100	XOR 00001100	
6	010100110	010100110	000000110	
7	101010011	XOR 01010011	100000011	
8	100110101	110110101	100011101	
9	100000110	101000110	100010010	
10	010000011	010100011	010001001	
11	111011101	111001101	111011000	
12	001110010	001111010	011101100	
13	100111001	100111101	101110110	
14	000000000	000000010	010111011	
15	000000000	000000001	011000001	
0	000000000	010011100	011111100	SC2
0		001001110	001111110	
1		000100111	000111111	SC=3
2	Data is	010001111	010000011	
3	error free,	011011011	011011101	
4	correction	011110001	011110000	
5	is not	011100100	001111000	
6	necessary.	001110010	000111100	
7		000111001	000011110	
8		010000000	000001111	
9		001000000	010011010	
10		000100000	001001101	
11		000010000	010111010	
12		000001000	001011101	
13	LOS=0 TRUE:→	000000100	010110010	
14		000000010	001011001	
15		000000001	010110000	
			001011000	SC=4

Two non-adjacent "1" bits have been lost and the error is not correctable.

U-Register: 00000001
10010100 ⊖
Corrected U-Reg: 10010101
9 A

A "1" bit was dropped from data and corrected.

(A) (B) (C)

CASSETTE TAPE DATA READ:- (A) ERROR FREE.
(B) CORRECTABLE ERROR.
(C) NON-CORRECTABLE ERROR.

ENCODED FORWARD ERROR CORRECTING CODE (DC) PER DATA BYTE (BA), HEXADECIMAL

A \ DC	B 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	39	B6	1E	91	77	F8	50	DF	A5	2A	82	0D	EB	64	CC	43
1	4B	C4	6C	E3	05	8A	22	AD	D7	58	F0	7F	99	16	BE	31
2	DD	52	FA	75	93	1C	B4	3B	41	CE	66	E9	0F	80	28	A7
3	AF	20	88	07	E1	6E	C6	49	33	BC	14	9B	7D	F2	5A	D5
4	C8	47	EF	60	86	09	A1	2E	54	DB	73	FC	1A	95	3D	B2
5	BA	35	9D	12	F4	7B	D3	5C	26	A9	01	8E	68	E7	4F	C0
6	2C	A3	0B	84	62	ED	45	CA	B0	3F	97	18	FE	71	D9	56
7	5E	D1	79	F6	10	9F	37	B8	C2	4D	E5	6A	8C	03	AB	24
8	E2	6D	C5	4A	AC	23	8B	04	7E	F1	59	D6	30	BF	17	98
9	90	1F	B7	38	DE	51	F9	76	0C	83	2B	A4	42	CD	65	EA
A	06	89	21	AE	48	C7	6F	E0	9A	15	BD	32	D4	5B	F3	7C
B	74	FB	53	DC	3A	B5	1D	92	E8	67	CF	40	A6	29	81	0E
C	13	9C	34	BB	5D	D2	7A	F5	8F	00	A8	27	C1	4E	E6	69
D	61	EE	46	C9	2F	A0	08	87	FD	72	DA	55	B3	3C	94	1B
E	F7	78	D0	5F	B9	36	9E	11	6B	E4	4C	C3	25	AA	02	8D
F	85	0A	A2	2D	CB	44	EC	63	19	96	3E	B1	57	D8	70	FF

Note: Data appears on cassette tape in this order: D C B A.
Digit A is read first, D last.