

## TECHNICAL MANUAL

1

## INTRODUCTION AND <br> OPERATION

2
FUNCTIONAL DETAIL

3
CIRCUIT
DETAIL

4
ÁDJUSTMENTS

5
MAINTENANCE PROCEDURES

6
installation
PROCEDURES

## Burroughs



## FIELD ENGINEERING

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Correspondence regarding this document should be addressed directly to Burroughs Corporation, P.O. Box 4040, El Monte, California 91734, Attn: Publications Department, TIO-West.

## LIST OF EFFECTIVE PAGES



## TABLE OF CONTENTS

Page Section ..... Page
PREFACE ..... xv
1 INTRODUCTION AND OPERATION
General ..... 1-1
Logic Power Supply ..... 1-1
Logic Power Supply - 2 ..... 1-2
Logic Power Supply-2 Sections ..... 1-4
Malfunction Protection Circuits ..... 1-4
Sequencing Circuits ..... 1-4
+300 Volt Supply and Inrush Control ..... 1-4
$\pm 15$ Volt Auxiliary Supply ..... 1-4
Master Oscillator, Clock, and Ramp Circuitry ..... $1-4$
Regulators ..... 1-4
Inverters ..... $1-6$
Operation ..... 1-6
General Operating Cónsiderations ..... $1-6$
Specialized Operational Modes ..... 1-6
Physical and Operating Specifications ..... 1-6
Logic Power Supply-1, -3, and -4 ..... 1-7
Logic Power Supply Sections ..... 1-7
Power Supply AC Control ..... 1-7
+160 Volt Supply and Regulator ..... 1-7
Inverter ..... 1-7
High Current Supply ..... 1-9
$\pm 12$ Volt Supplies ..... 1-9
Control Supply ..... 1-9
Operation (Logic Power Supply-1, -3, and -4) ..... 1-9
General Operating Considerations ..... 1-9
Specialized Operational Modes ..... $1-10$
Physical and Operating Specifications (Logic Power Supply -1, -3, and -4) ..... 1-10
Memory Power Supply ..... $1-10$
Memory Power Supply Sections ..... $1-12$
-5 Volt Supply ..... 1-12
+19 Volt Supply ..... 1-12
+4 Volt Supply ..... 1-12
Operations ..... 1-12
Physical and Operating Specifications ..... 1-12
+20 Volt Paper Tape Power Supply ..... 1-12
Operation ..... 1-13
Physical and Operating Specifications ..... 1-14
System AC Control ..... 1-14
System AC Control Operation ..... 1-14
Glossary of Terms ..... 1-16FUNCTIONAL DETAILGeneral2-1
Logic Power Supply -2 ..... 2-1
Malfunction Protection Circuits ..... 2-1
Sequencing Circuitry ..... 2-4
+300 Volt Supply and Inrush Control ..... 2-5
$\pm 15$ Volt Auxiliary Supply ..... 2-5

TABLE OF CONTENTS (Cont)
Section Page
2 FUNCTIONAL DETAIL (Cont)
Master Oscillator, Clock, and Ramp Circuitry ..... 2.6
Regulators ..... 2-7
Inverters ..... 2-7
Logic Power Supply-1, -3 , and -4 ..... 2.9
Malfunction Protection Circuits ..... 2-9
Main AC Circuit Breaker ..... 2-9
Overvoltage Detectors ..... 2-12
Undervoltage Detectors ..... 2-12
+160 Volt Supply and Regulator ..... 2-13
Inverter ..... 2-14
High Current Supply ..... 2-14
$\pm 12$ Volt Supplies ..... 2-14
Control Supply ..... 2-14
Memory Power Supply Functional Detail ..... 2-17
+20 Volt Paper Tape Power Supply Functional Detail ..... 2.19
System AC Control Functional Detail ..... 2-19
CIRCUIT DETAIL
General ..... 3-1
Logic Power Supply-2 ..... 3-1
AC Input ..... 3-1
+300 Volt Supply and Inrush Control ..... 3-1
+300 Volt Supply ..... 3-2
Inrush Control ..... 3-3
Inrush Control Sequence of Operation ..... 3-3
$\pm 15$ Volt Auxiliary Supply ..... 3-7
Conventional Supply and Regulators ..... 3-7
Auxiliary Override Circuit ..... 3-8
Master Oscillator, Clock Signal Generator and Ramp Generator ..... 3-8
Master Oscillator ..... 3-8
Clock ..... 3-8
Ramp ..... 3-9
Malfunction Protection Circuits, Clear Detector, and +10 Volt Reference Supply ..... 3-9
Main Malfunction Protection Circuit (Including Main Crowbar) ..... 3-9
+4.75 Volt Overvoltage Detector ..... 3-10
-2.0 Volt Overvoltage Detector ..... 3-11
+12 Volt Overvoltage Detector and Crowbar Circuit ..... 3-12
-12 Volt Overvoltage Detector and Crowbar Circuit ..... 3-12
+4.75 Volt Undervoltage Detector ..... 3-13
-2.0 Volt Undervoltage Detector ..... 3-13
Clear Detector ..... 3-14
+10 Volt Reference Supply ..... 3-15
Sequencing Circuitry ..... 3-15
+4.75/2.00 Volt Hold-Off Circuit ..... 3-15
12-Volt Hold-Off Circuit ..... 3-16
+12 Volt Inverter Channel (Example) ..... 3-16
+12 Volt Sense Amplifier ..... 3-16
+12 Volt Current Limiter ..... 3-17
+12 Volt Disable Circuit ..... 3-18
+12 Volt Inverter Driver ..... 3-20

## TABLE OF CONTENTS (Cont)

Section ..... Page
3 CIRCUIT DETAIL (Cont)
+12 Volt Inverter Output ..... 3.21
Functional Detail of Individual Inverter Channels ..... 3-22
+4.75 Volt Inverter Channel ..... 3-22
+4.75 Volt Sense Amplifier ..... 3-23
+4.75 Volt Current Limiter Circuit ..... 3-23
+4.75 Volt Disable Circuit ..... $3-23$
+4.75 Volt Inverter Driver ..... 3-25
+4.75 Volt Inverter Output ..... 3-25
-2.0 Volt Inverter Channel ..... 3-27
-2.0 Volt Sense Amplifier ..... 3-28
-2.0 Volt Current Limiter Circuit ..... 3-28
-2.0 Volt Disable Circuit ..... 3-28
-2.0 Volt Inverter Driver ..... 3.29
-2.0 Volt Inverter Output ..... 3-30
-12 Volt Inverter ..... 3-30
-12 Volt Sense Amplifier ..... 3-30
-12 Volt Current Limiter ..... 3.33
-12 Volt Disable Circuit ..... 3-33

- 12 Volt Inverter Driver ..... 3-34
- 12 Volt Inverter Output ..... 3-34
Logic Power Supply -1, -3, and -4 ..... 3-34
Logic Supply AC Control ..... 3-35
+4.75 Volt and -2.0 Volt Output Monitor ..... 3-36
Overvoltage Detectors ..... 3-36
Undervoltage Detectors ..... 3-40
+160 Volt Supply and Regulator ..... 3-40
+160 Volt Bridge Rectifier ..... 3-40
+160 Volt Regulator ..... $3-42$
Regulator Bridge Rectifier ..... 3-42
Feedback Control Circuit ..... 3-42
Slow Start Circuit ..... 3-45
Gate Driver Circuit ..... 3-45
Inverter ..... 3-46
Basic SCR Inverter ..... 3-46
Improved SCR Inverter ..... 3-47
Inverter Timing Circuit ..... 3-47
Comparator (Logic Power Supply-1 and -3) ..... 3-51
Comparator (Logic Power Supply-4) ..... 3-51
Voltage Controlled Oscillator ..... 3-51
Logic Timer and Gate Driver Circuit ..... 3-54
High Current Supply ..... 3.59
+4.75 Volt Current Limiter (Logic Power Supply-1 and -3) ..... 3-59
+4.75 Volt Master/Slave Control Circuits (Logic Power Supply-4) ..... 3-62
+4.75V Current Limiter and Sequencing/Interlock Circuit (Logic Power Supply-4) ..... 3-63
-2.0 Volt Shunt REgulator (Logic Power Supply-1 and -3) ..... 3-65
-2.0 Volt Shunt REgulator and Master/Slave Control Circuits (Logic Power Supply-4) ..... 3-65
$\pm 12$ Volt Supplies ..... 3-65
Rectifier and Filter ..... 3-69
Voltage Regulator and Current Limiter ..... 3-69
Overvoltage Detector ..... 3-69


## TABLE OF CONTENTS (Cont)

Section
Page
3 CIRCUIT DETAIL (Cont)
Undervoltage Detector ..... 3-71
Control Supply ..... 3-71
Positive and Negative Integrated Circuit Regulators ..... 3-71
+15 Volt Complementary Tracking Supply ..... 3-73
Negative Voltage Regulator (-15V) ..... 3-73
Positive Voltage Regulator ( +15 V ) ..... 3-73
$+24 \mathrm{~V},+4.5 \mathrm{~V}$, and -1.9 V Supply ..... 3-77
Bridge Rectifier and Preregulator ..... 3-77
+24 Volt Supply ..... $3-78$
+4.5 Volt Supply ..... $3-78$
-1.9 Volt Supply ..... 3-78
Memory Power Supply Circuit Detail ..... 3-80
AC Input ..... 3-80
+19 Volt Supply ..... 3-80
+4 Volt Supply ..... 3-83
-5 Volt Supply ..... 3-87
+20 Volt Paper Tape Power Supply Circuit Detail ..... 3-87
Auxiliary Half Wave Rectifier and Filter ..... 3-87
Bridge Rectifier and Filter ..... 3-87
Integrated Circuit Regulator ..... 3-87
System AC Control ..... 3-90
Power Switching Circuit ..... 3-90
Overtemperature Protection Circuit ..... 3-90
ADJUSTMENTS
General ..... $4-1$
Logic Power Supply Adjustments ..... 4-1
Test Equipment ..... 4-1
Single Supply Adjustments (Logic Power Supply-2) ..... 4-1
Preparations for Calibration ..... 4-1
Detailed Alignment ..... 4-5
Auxiliary Supply Adjustment ..... 4-5
+10 Volt Reference Voltage Adjustment ..... $4-5$
Output Voltage Adjustment ..... $4-6$
Overvoltage Trip Point Check and Adjustment ..... 4-6
Balance Adjustment and Current Limit Check (+4.75 and -2.00 Volt) ..... 4-7
Adjustments Under System Load (Single Logic Supply) ..... 4-8
Preparatory Steps ..... $4-8$
+4.75 and -2.0 Volt Packplane Adjustments ..... 48
+12.0 Volt Backplane Adjustment ..... $4-9$
-12.0 Volt Backplane Adjustment ..... 4-10
Parallel Supply Adjustments (Logic Power Supply-2) ..... 4-10
Master/Slave Setup ..... 4-10
Master Supply ..... 4-10
Slave Supply ..... 4-11
Balance Adjustments ..... 4-11
Preparatory Steps ..... 4-11
+4.75 Volt Balance Adjustment ..... 4-11
-2.00 Volt Balance Adjustment ..... 4-13
Adjustments Under System Load (Parallel Operation) ..... 4-13

## TABLE OF CONTENTS(Cont)

Section ..... Page
4 ADJUSTMENTS (Cont)
Parallel Current-Limiting Adjustment ..... 4-13
Final Balance Adjustment ..... 4-14
+4.75 Volt Backplane Adjustment ..... 4-14
-2.0 Volt Backplane Adjustment ..... 4-14
+12.0 Volt Backplane Adjustment ..... 4-14
-12.0 Volt Backplane Adjustment ..... 4-15
Single Supply Adjustments (Logic Power Supply-1, -3 and -4) ..... 4-15
Preparations for Calibration ..... 4-15
Detailed Alignment ..... 4-16
+160 Volt Regulator Adjustment ..... 4-17
Control Card Adjustment ..... 4-18
VCO Card Adjustment (Logic Power Supply-1 and -3) ..... 4-18
VCO Card Adjustment (Logic Power Supply-4) ..... 4-19
Delay Adjustment ..... 4-19
Gate Driver Pulse Check ..... 4-20
-2.00 Volt Adjustment ..... 4-21
+4.75 Volt Adjustment ..... 4-21
Inverter Adjustment ..... 4-21
Null Verification (Logic Power Supply-1 and -3) ..... 4-23
Null Verification (Logic Power Supply-4) ..... 4-23
$\pm 12$ Volt Adjustment ..... 4-24
Adjustments Under System Load (Single Logic Supply) ..... 4-25
Preparatory Steps ..... 4-25
+4.75 Volt Backplane Adjustment ..... 4-25
-2.0 Volt Backplane Adjustment ..... 4-25
+12.0 Volt Backplane Adjustment ..... 4-25
-12.0 Volt Backplane Adjustment ..... 4-26
Parallel Supply Adjustments (Logic Power Supply-4) ..... 4-26
Master/Slave Setup ..... 4-26
Master Supply ..... 4-26
Slave Supply ..... 4-26
Balance Adjustment ..... 4-27
+12.0 Volt Backplane Adjustment ..... 4-27
-12.0 Volt Backplane Adjustment ..... 4-27
Memory Power Supply Adjustments ..... 4-28
Test Equipment ..... 4-28
Detailed Alignment ..... 4-28
Overvoltage Adjustments ..... 4-28
Voltage Adjustments ..... 4-29
Current Limit Adjustments ..... 4-31
+20 Volt Paper Tape Power Supply Adjustments ..... 4-33
Test Equipment ..... 4.33
Detailed Alignment ..... 4-33
Overvoltage Protector Adjustment ..... 4-33
Output Voltage Adjustment ..... 4-33
MAINTENANCE PROCEDURES
General ..... 5-1
Preventive Maintenance ..... 5-1
Corrective Maintenance (Logic Power Supply-2) ..... 5-1

## TABLE OF CONTENTS (Cont)

Section Page
5 MAINTENANCE PROCEDURES (Cont) Troubleshooting Flow5-2
Placing the Supply in the Diagnostic Configuration ..... 5-2
Placing the Supply in the Simulated Operation Configuration ..... 5-8
Verification of Repairs ..... 5-9
Maintenance References ..... 5-9
Test Point Locations ..... 5-13
Standard Test Conditions ..... $5-13$
Voltage and Waveform References ..... 5-17
Replacement of Power Transistors ..... 5-49
Testing and Replacement of Inverter Protective Diodes ..... 5-49
Corrective Maintenance (Logic Power Supply-1, -3 and -4) ..... 5-50
Troubleshooting Flow ..... 5-50
Maintenance References ..... 5-50
Component Locations ..... 5-50
Maintenance Features ..... 5-81
Waveform References ..... 5-81
Corrective Maintenance (Memory Power Supply) ..... 5-81
Troubleshooting Flow ..... 5-81
Maintenance References ..... 5-81
Corrective Maintenance (+20 Volt Paper Tape Power Supply) ..... 5-85
Troubleshooting ..... 5-85
Maintenance References ..... 5-85
Corrective Maintenance (System AC Control) ..... 5-87
6 INSTALLATION PROCEDURES
General ..... 6-1
Logic Power Supply Installation ..... 6-1
Logic Power Supply Replacement ..... 6-1
Logic Power Supply Substitution ( -2 Version for $-1,-3$ or -4 Version) ..... 6-3
Logic Power Supply Substitution (-1, -3 or -4 Version for -2 Version) ..... 6-6
Memory Power Supply Installation ..... 6-8
Replacement ..... 6-8
Installing an Additional Supply ..... 6-8
+20 Volt Paper Tape Power Supply Installation ..... 6-13
LIST OF ILLUSTRATIONS
Figure ..... Page
1-1 Logic Power Supply -2 ..... 1-2
1-2 Logic Power Supply-2 Installed in B 1726 System (Two Each) ..... $1-3$
1-3 Logic Power Supply-2 Sections ..... 1-5
1-4 Logic Power Supply -1, -3 or -4 ..... $1-8$
1-5 Memory Power Supply ..... 1-11
1-6 +20 Volt Paper Tape Power Supply ..... 1-13
1-7 System AC Control ..... 1-15
2-1 Logic Power Supply-2 Basic Block Diagram ..... 2-2
2-2 Overvoltage Protective Circuit Block Diagram ..... 2-3
2-3 Clear Detector Block Diagram ..... 2-4

## LIST OF ILLUSTRATIONS (Cont)

Figure Page+300 Volt Supply Block Diagram2-5
2.5 $\pm 15$ Volt Auxiliary Supply Block Diagram ..... 2-6
2-6 Master Oscillator, Clock, and Ramp Block Diagram ..... 2-6
2-7 Regulator Block Diagram (One Channel Only is Shown) ..... 2-7
2-8 Disable Pulse Generation ..... 2-8
2-9 Inverter Block Diagram (One Channel Only is Shown) ..... 2-8
2-10 Inverter Timing ..... 2-10
2-11 Logic Power Supply-1, -3, and -4 Block Diagram ..... 2-11
2-12 Overvoltage Protection Circuit ( +4.75 V and -2.0 V Outputs Only) ..... 2-12
2-13 Undervoltage Detectors and Clear Signal Generator ..... 2-13
2-14 +160 Volt Supply and Regulator ..... 2-13
2-15 Inverter Block Diagram ..... 2-15
2-16 High Current Supply Block Diagram ..... 2-16
2-17 $\quad 12$ Volt Power Supply Block Diagram ..... 2-16
2-18 $\pm 15$ Volt Section of Control Supply ..... 2-17
$2-19+24 \mathrm{~V},+4.5 \mathrm{~V}$ and -1.9 V Section of Control Supply ..... 2-17
2-20 Memory Power Supply Block Diagram ..... 2-18
2-21 +20 Volt Paper Tape Power Supply Block Diagram ..... 2-19
2-22 System AC Control Block Diagram ..... 2-20
3-1
AC Input and +300 Volt Supply (Less Inrush Control) ..... 3-2
3-2 Inrush Control ..... 3-5
3-3 $\pm 15$ Volt Auxiliary Supply ..... 3-7
3-4 Master Oscillator, Clock and Ramp Generator ..... 3-8
3-5 Main Malfunction Protection Circuit ..... 3-10
3-6 $\quad$ 4.75 Volt and -2.0 Volt Overvoltage Detectors ..... 3-11
3-7 $\quad+12$ Volt Overvoltage Detector and Crowbar ..... 3-12
3-8 -12 Volt Overvoltage Detector and Crowbar ..... 3-13
3-9 +4.75 Volt and -2.00 Volt Undervoltage Detectors and Clear Detector ..... 3-14
3-10 $\quad+10.0$ Volt Reference Supply ..... 3-15
3-11 +4.75/-2.0 Volt Hold-Off Circuit ..... 3-16
3-12 12-Volt Hold-Off Circuit ..... 3-17
3-13 +12 Volt Sense Amplifier ..... 3-18
3-14 +12 Volt Current Limiter ..... 3-19
3-15 $\quad+12$ Volt Disable Circuit ..... 3-19
3-16 +12 Volt Driver ..... 3-21
3-17 +12 Volt Inverter Output Stage ..... 3-22
3-18 $\quad$ +4.75 Volt Sense Amplifier ..... 3-23
3-19 +4.75 Volt Current Limiter ..... 3-24
3-20 +4.75 Volt Disable Circuit ..... 3-24
3-21
+4.75 Volt Inverter Driver ..... 3-25
3-22 $\quad+4.75$ Volt Inverter Output (Less Rectifiers and Filter) ..... 3-26
3-23 +4.75 Volt Rectifier and Filter ..... 3-27
3-24 -2.00 Volt Sense Amplifier ..... 3-28
3-25 -2.00 Volt Current Limiter ..... 3-29
3-26 -2.00 Volt Disable Circuit ..... 3-29
3-27 -2.00 Volt Inverter Driver ..... 3-30
3-28 -2.00 Volt Inverter Output (Less Rectifier and Filter) ..... 3-31
3-29 -2.00 Volt Rectifier and Filter ..... 3-32
3-30 -12 Volt Sense Amplifier ..... 3-32
3-31 -12 Volt Current Limiter ..... 3-33
3-32 -12 Volt Disable Circuit ..... 3-33

## LIST OF ILLUSTRATIONS (Cont)

Figure Page
3-33 -12 Volt Inverter Driver ..... 3-34
3-34 -12 Volt Inverter Output ..... 3-35
3-35 Logic Supply AC Control ..... 3-36
3-36 $\quad$ +4.75 Volt and -2.0 Volt Output Monitor ..... 3-37
3-37 Overvoltage Detectors, Crowbar Trip Circuit and Breaker Trip Circuit ..... 3-39
3-38 Undervoltage Detectors and Clear Circuit ..... 3-41
3-39 +160 Volt Supply ..... 3-42
3-40 +160 Volt Regulator ..... 3-43
3-41 Bridge Inverter Operation ..... 3-46
3-42 Basic SCR Inverter ..... 3-47
3-43 SCR Inverter Operation ..... 3-48
3-44 Improved SCR Inverter ..... 3-49
3-45 Inverter Timing Circuit Block Diagram ..... 3-51
3-46 Comparator and VCO Circuits ..... 3-52
3-47 +2.75V Comparator (Master/Slave Supplies) ..... 3-53
3-48 Inverter Timing Circuit Block Diagram ..... 3-54
3-49 Inverter Timing ..... 3-56
3-50 Timing Logic and Gate Driver Circuits ..... 3-57
3-51 High Current Supply ..... 3-60
3-52 $\quad$ +4.75 Volt Current Limiter (Stand Alone Supply) ..... 3-61
3-53 +4.75 Volt Slave Control Circuit ..... 3.62
3-54 $\quad$ +4.75 Volt Current Limiter (Master/Slave Supplies) ..... 3-63
3-55 Sequencing/Interlock Circuit (Master/Slave Supplies) ..... 3-64
3-56 -2.0 Volt Shunt Regulator (Stand Alone Supplies) ..... 3-67
3-57 -2.0 Volt Shunt Regulator (Master/Slave Version) ..... 3-61
3-58 12 Volt Rectifier and Filter ..... 3-69
3-59 12 Volt Regulator and Current Limiter ..... 3-70
3-60 12 Volt Output Monitor ..... 3-72
3-61 +15 Volt Complementary Tracking Supply ..... 3-75
3-62 $\pm 15$ Volt Supply Tracking ..... $3-77$
3-63 Bridge Rectifier and Pre-Regulator ..... 3.77
3-64 +24 Volt Supply ..... 3-78
3-65 +4.75V Supply ..... 3-79
3-66 -1.9 Volt Supply ..... 3-79
3-67 +19 Volt Supply ..... 3-81
3-68
IC Regulator Block Diagram (Showing Relationship to External Supply Sections) ..... 3-83
3-69 +4 Volt Supply ..... 3-85
3-70 -5 Volt Supply ..... 3-88
3-71 +20 Volt Paper Tape Power Supply Schematic Diagram ..... $3-89$
3-72 Integrated Circuit Regulator Block Diagram ..... 3-90
3-73 AC Control (B 1710 Series AC Control Shown) ..... 3-91
4-1 Supply in Test Configuration ..... 4-2
4-2 Regulator Board Control and Test Point Locations ..... 4-3
4-3 Power Board Controls ..... 4-4
4-4 B 1712/B 1714 Backplane Voltage Sense Points ..... 4-9
4-5 B 1720-Series Current Shunt and Voltage Sense Locations ..... 4-12
4-6 Logic Supply Card and Control 1Ocations (Logic Power Supply-2 and -3) ..... 4-16
4-7 Logic Supply Card and Control Locations (Logic Power Supply-4 Only) ..... 4-17
4-8 Logic Power Supply Test Jacks ..... 4-18
4-9 Power SCR Gate Driver Pulses ..... 4-20
4-10 Commutating SCR Gate Driver Pulses ..... 4-20

## LIST OF ILLUSTRATIONS (Cont)

Figure Page
4-11 Transformer T2 Test Connections (Inverter Adjustment) ..... 4-22
4-12 Inverter Pulses ..... 4-23
4-13 Memory Power Supply Controls (Current Version, P/Ns 22111942 and 2210 9052) ..... 4-30
4-14 Memory Power Supply Controls (Earlier Version, P/N 2201 4229( ..... 4-31
4-15 Memory Supply Dummy Load Connections ..... 4-32
4-16 $\quad+20$ Volt Paper Tape Power Supply Controls ..... 4-34
5-1 Logic Power Supply Main Troubleshooting Flow ..... 5-3
5-2 Maintenance Features ..... 5-7
5-3 Regulator Board Test Location ..... 5-8
5-4 RUN/TEST Mode Selection ..... 5-9
5-5 Logic Power Supply Main Schematic ..... 5-11
5-6 Test Point Locations on Regulator Board (Component Side) ..... 5-14
5-7 Test Point Location on Inrush Control Board (Component Side) ..... 5-15
5-8 Test Point Location on Main Power Board (Underside) ..... 5-16
5-9 Regulator Board Voltage and Waveform References ..... 5-17
5-10 Power Board Voltage and Waveform References ..... 5-34
5-11 Inrush Control Board Voltage and Waveform Refrences ..... 5-47
5-12 Logic Power Supply -1 Troubleshooting Flow ..... 5-51
5-13 Logic Power Supply-1 \&-3 Main Schematic ..... 5-52
5-14 Logic Power Supply-1 \&-3 VCO Card Schematic ..... 5-56-2
5-15 Logic Power Supply-1 \& -3, -2.0 Volt Shunt Regulator Card Schematic ..... 5-58
5-16 Logic Power Supply-4 Main Schematic ..... 5-60
5-17 Logic Power Supply -4 VCO Card Schematic ..... 5.64
5-18 Logic Power Supply-4, -2.0 Volt Shunt Regulator Card Schematic ..... 5-66
5-19 Logic Power Supply-1, $-3 \&-4,+160$ Volt Regulator Card Shcematic ..... 5-68
5-20 Logic Power Supply-1, -3, \& - 4 Gate Driver Card Schematic ..... 5-68-2
5-21 Logic Power Supply-1, -3, \& $-4,12$ Volt Regulator Card Schematic ..... 5-70
5-22 +160 Volt Regulator Card Component Locations ..... 5-71
5-23 Control Supply Card Component Locations ..... 5-72
5-24 Gate Driver Card Component Locations ..... 5-73
5-25 -2 Volt Shunt Regulator Card Component Locations (Logic Power Supply -1 \& -3) ..... 5-74
5-26 -2 Volt Shunt Regulator Component Locations (Logic Power Supply -4) ..... 5-75
5-27 VCO Card Component Locations (Logic Power Supply -1 \& -3) ..... 5-76
5-28 VCO Card Component Locations (Logic Power Supply 4) ..... 5.77
5-29 12 Volt Supply Card Component Locations ..... 5.78
5-30 Logic Power Supply Card Extension ..... 5-79
5-31 Logic Power Supply Heat Sink Extension . ..... 5-80
5-32 160 Volt Regulator Card Internal Waveforms (Measured from Cathodes of CR6, CR9 \& CR14 to +160 V ) ..... 5-82
5-33 +160 Volt Regulator Gate Driver Pulse (Measured at Pins OP/OR and OP/OK of Connector U3) ..... 5-82
5-34 VCO Comparator Waveforms (Measured at Comparator E0 and B1 on VCO Card) ..... 5-82
5-35 VCO Internal Waveforms (Measured at Inputs of Flip-Flop D2 on VCO Card) ..... 5-82
5-36 VCO Output Waveforms (Measured at Outputs of Flip-Flop D2 and Multivibrator A1 on VCO Card) ..... 5-82
5-37 VCO Card Output Waveforms (Measured from Pins OK, OH, OD and OG to Ground on VCO Card) ..... 5-82
5-38
Gate Driver Outputs A1-A4 (Measured Across Secondary of Pulse Transformers T1, T2, T4 and T5 on Gate Driver Card) ..... 5-83
5-39
Gate Driver Outputs A5 \& A6 (Measured Across Secondary of Pulse Transformers T3 and T6 on Gate Driver Card) ..... 5-83
5-40 Diode/SCR Bridge Rectifier Output (Measured Between Pins 2 and 3 of Choke L1) ..... 5-83
5-41 Ripple On +160 Volt Output (Measured Across C6 at Output of +160 Volt Supply) ..... 5-83
5-42 Inverter SCR A1 Output (Measured at A1 Test Jacks on Supply Front Panel) ..... 5-83

## LIST OF ILLUSTRATIONS (Cont)

Figure ..... Page
5-43 Inverter SCR's A5 \& A6 Output (Measured at A5 \& A6 Test Jacks on Supply Front Panel) ..... 5-83
5-44 Waveform at Commutating Capacitors (Measured Across Capacitors C1 \& C2 in Inverter) ..... 5-84
5-45 Waveform at Commutating Inductor (Measured Across Inductor L2 in Inverter) ..... 5-84
5-46 Waveform at Primary of Transformer T2 (Measured Across T2 Primary) ..... 5-84
5-47 High Current Rectifier Output (Measured Across Pins $1 \& 4$ of Choke L10) ..... 5-84
5-48 High Current Supply Ripple (Measured Across Capacitor C29) ..... 5-84
5-49 High Current Supply Ripple (Measured Across Capacitor C26) ..... 5-84
5-50 Ripple on +4.75 Volt Output (Measured from +4.75 Volt Terminal to Ground) ..... 5-85
5-51 Ripple On -2.0 Volt Output (Measured From -2 Volt Terminal to Ground) ..... $5-85$
5-52 Memory Power Supply Troubleshooting Flow ..... 5-86
6-1 Logic Power Supply Removal and Replacement ..... 6-2
6-2 Installation of Logic Power Supply -2 Slides in B 1700 Frame ..... 6-4
6-3 Installation of Slide Chassis Sections (Logic Power Supply -2) ..... 6-5
6-4 Supply Movement Range (Logic Power Supply -2) ..... 6-5
6-5 Regulator Board Bracket Installation ..... 6-6
6-6 Installation of Logic Power Supply -1 Slides in B 1700 Frame ..... 6.7
6-7 Installation of Chassis Sections (Logic Power Supply -1) ..... 6.7
6-8 Supply Movement Range (Logic Power Supply -1) ..... 6-8
6-9 Memory Power Supply Mounting (B 1710 Series Systems) ..... 6-9
6-10 Memory Power Supply Mounting (B 1720 Series Systems) ..... 6-10
6-11 Memory Supply Locations in B 1720 Series Systems ..... 6-11
6-12 Memory Supply AC Connections ..... 6-11
6-13 Memory Supply Cabling ..... 6-12
6-14 Memory Supply Output Connections ..... 6-13
6-15 +20 Volt Power Supply Wiring ..... 6-14
6-16 $\quad+20$ Volt Power Supply Installation ..... 6-15
6-17 +20 Volt Power Supply AC Wiring ..... 6-16
6-18 +20 Volt Power Supply AC Cable Routing (B 1710 Series Systems) ..... 6-16
6-19 +20 Volt Power Supply AC Cable Routing (B 1720 Series Systems) ..... 6-17
LIST OF TABLES
Table ..... Page
1-1 Logic Power Supply Variants ..... 1-1
2-1 Malfunction Results ..... 2-3
4-1 Control Preset Conditions ..... 4-4
4-2 Switch Preset Conditions ..... 4-4
4-3 Output Voltage Adjustments ..... 4-6
4-4 Overvoltage Crowbar Trip Points ..... 4-7
4-5 Master Supply Setup ..... 4-10
4-6 Slave Supply Setup ..... 4-11
5-1 Test Condition Applicability (By Supply Section) ..... 5-13
5-2 Standard Test Conditions ..... 5-13
5-3 +20 Volt Paper Tape Power Supply Troubleshooting ..... 5-86

## PREFACE

This Field Engineering Technical Manual (FETM) contains a complete information package on each power control and supply device used in the B 1700 Series Central Systems. Included are the Logic Power Supplies, Memory Power Supplies, the Central System AC Control, and the 20V Paper Tape Power Supply.

This FETM is divided into eight sections.
Section 1 - INTRODUCTION AND OPERATION. This section contains the general characteristics of each of the power control and supply devices and describes their operation.

Section 2 - FUNCTIONAL DETAIL. This section contains the functional descriptions of the power device circuits.
Section 3 - CIRCUIT DETAIL. This section provides detailed information on the individual circuits and circuit elements within the power devices.

Section 4 - ADJUSTMENTS. This section contains the complete adjustment procedures required to place power supplies into operation.

Section 5 - MAINTENANCE PROCEDURES. This section contains troubleshooting aids and information on the maintenance features incorporated into the design of the power devices.

Section 6 - INSTALLATION PROCEDURES. This section describes the physical installation of each type of power supply in a B 1700 system.

Section 7 - OPTIONAL FEATURES
Appendix A - GLOSSARY OF TERMS
Appendix B-LINS
Appendix C - RINS

## SECTION 1

## INTRODUCTION AND OPERATION

## GENERAL

This section discusses the purpose and basic functions of each power subsystem device of the B 1700. Included are all the devices relating to the control of, or production of, operating voltages for use within the central system cabinet, and those devices that are physically located within the central system cabinet.

## LOGIC POWER SUPPLY

The Logic Power Supply serves as the main source of operating power for the B 1700 Central System Logic, exclusive of memory power. The supply operates from 188 through 253 volts ac, rms $50 / 60 \mathrm{~Hz}$, single phase primary input power, and produces four dc output voltages:
a. $\quad+4.75$ volts. Used as the Vcc (collector voltage) of the system CTL logic, with a maximum continuous output current of 200 amperes.
b. $\quad-2.0$ volts. Used as the Vee (emitter voltage) of the system CTL logic, with a maximum continuous output current of 200 amperes.
c. $\quad+12.0$ volts. Used as the positive operating voltage for discrete circuit elements, with a maximum continuous output current of up to 10 amperes (depending on the supply model concerned).
d. -12.0 volts. Used as the negative operating voltage for discrete circuit elements, with a maximum continuous output current of up to 18 amperes (depending on the supply model concerned).

The Logic Power Supply is designed for use both as an individual unit, and in combination with other units of its type. In systems where one supply is insufficient to meet the load requirements (specifically the B 1720 Series), additional supplies are added as needed. In B 1700 systems of maximum configuration, three such supplies are used. Because the demand for current in the front bay of B 1720 series systems can exceed 200 amperes, the first and second supplies in B 1720 systems are connected in parallel (Master/Slave). In the master/slave mode, the regulation círcuits of the second supply are controlled by those in the first to provide equal output voltages and current sharing. The third supply, when present, always stands alone. .

Logic power supplies are produced in four versions, and are identified by the suffix $-1,-2,-3$, or -4 . The differences between the various logic supplies and their applications are explained in table 1-1.

Table 1-1. Logic Power Supply Variants

| Designation | Part <br> Number | Applications | Comments |
| :---: | :---: | :--- | :--- |
| Logic Power Supply-1 (LPS-1) | 22050975 | B 1710 Systems | Non-UL Approved, Not Master/Slave <br> Capable |
| Logic Power Supply-2 (LPS-2) | 22082739 | All B 1700 Systems | Current Production <br> Logic Power Supply-3 (LPS-3) |
| 22082937 | B 1710 Systems | UL Approved Version of LPS-1 <br> UL Approved \& Master/Slave Cap- <br> able Version of LPS-1 |  |

There are four designated versions of the logic supply, but only two main designs. Logic Power Supplies $-1,-3$, and -4 are basically the same design. Logic Power Supply-2 is radically different in design from -1, -3 , and -4 . (LPS-2 will eventually supersede all other Logic Power Supplies in B 1700 systems.) Despite the design differences, all Logic Power Supplies are essentially interchangeable electrically and physically. Therefore, it is possible to substitute one version for another in a given system, provided that master/slave operation is not involved. Where master/slave operation is employed, both logic supplies involved must be of the same type (two each of LPS-2 or two each of LPS-4).

Since the circuit design, manner of operation, adjustments, and troubleshooting procedures for the two supply designs are unrelated to each other, these topics are discussed separately in each section of the manual. The Logic Power Supply- 2 is discussed first in each case.

## LOGIC POWER SUPPLY-2

The Logic Power Supply - 2 is the inverter-rectifier type (figure 1-1) with separate transistor inverters for each of the four output voltages it produces. Each of the inverter-rectifiers (channels) incorporates provisions for independent regulation of its output voltage, output current limiting, and protective deactivation in the event of a malfunction. The inverters are controlled by sensing circuits which vary the length of fixed-frequency driving pulses. Internal operating voltages for the inverters are provided by a controlled bridge rectifier operating directly from the ac line. Low-level circuitry throughout the logic supply is powered by an ac operated auxiliary supply. Figure 1-2 shows the LSP-2 installed.


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Figure 1-1. Logic Power Supply -2


GIII 80

Figure 1-2. Logic Power Supply-2 Installed in B 1726 System (Two Each)

## B 1700 Power Subsystem

## Logic Power Supply-2 Sections

The Logic Power Supply-2 consists of a number of individual sections. The operational makeup is described in the following paragraphs. Physical divisions of the supply are illustrated in figure 1-3.

## Malfunction Protection Circuits

Protection against malfunctions within the supply includes overcurrent, overvoltage, and overtermperature detection. These potential hazards are monitored as follows:
a. Input (ac) overcurrent protection is provided by a circuit breaker in the primary supply line.
b. Overtemperature protection is provided by thermal switches which monitor the inverter heat sink temperature. This feature serves mainly to guard against ventilation failure.
c. Overvoltage protection is provided by operational amplifier detectors which monitor the output of each inverter channel.

## Sequencing Circuits

Sequencing of the inverter outputs allows the control circuits within the supply to achieve full operation before actual regulation action is required. Sequencing is accomplished by applying "hold-off" voltages to the regulators to prevent the inverters from operating. The application of these hold-off voltages is a time-controlled event that occurs each time the supply is cycled on. An associated portion of the sequencing circuitry is the clear detector. This detector informs the processor that the supply is operational.

## +300 Volt Supply and Inrush Control

The +300 volt supply provides the internal operating voltages for the output stages of the inverters. This supply does not use a transformer, but rather a controlled bridge rectifier operating directly from the ac line. The inrush control is a timecontrolled circuit that provides a "slow start" of the +300 volt supply, preventing excessive current flow each time the supply is cycled on.

## $\pm 15$ Volt Auxiliary Supply

The $\pm 15$ volt auxiliary supply provides the internal operating voltages for low-level circuits within the Logic Power Supply -2 . This supply employs dual operating modes. During initial start-up, the $\pm 15$ volt auxiliary supply operates from the ac line. After inverter operation has started, source power for the supply is derived from the +4.75 volt channel by an auxiliary override circuit. This circuit isolates the auxiliary supply from power line fluctuations by forcing it to operate from a regulated internal source.

## Master Oscillator, Clock, and Ramp Circuitry

The switching rate of all four inverters within the supply is derived from a free-running master oscillator that operates at a frequency of approximately 18.8 kilohertz. The sine wave output from the oscillator is coupled to two following stages, producing square wave CLK and CLK/ signals and a sawtooth wave ramp signal. The CLK and CLK/ signals are used to toggle the inverters. The ramp signal is used in the regulation circuitry.

## Regulators

Each of the four inverter channels is controlled by a regulator circuit which disables the inverter driver stage for a portion of each pulse of the CLK and CLK/ steering signals. This disabling action varies the driving signal pulse width, accomplishing the desired regulation by varying the percentage of time during which current is allowed to flow to the load. The voltage regulation drive signal is supplied to the regulator by a detector circuit. This circuit monitors the voltage at the output of the inverter channel.


In addition to supplying voltage regulation control, the regulator circuits incorporate provisions for current limiting. Current limiting is also controlled by varying the inverter pulse length. The current-limiting drive signal is derived by monitoring the current flowing in the inverter output. In practice, both the voltage regulation drive signal and current-limiting drive signal are applied simultaneously to the regulator, where they tend to oppose each other. This opposition is normal, since a voltage regulator tends to increase supply output in response to an increase in load, whereas a current limiter tends to reduce supply output. An operational balancing adjustment renders the current-limiting influence negligible, in the absence of excessive supply output loading.

## Inverters

Each of the four inverters is a two-stage device consisting of driver and output sections. The driver is toggled by the modified CLK and CLK/ steering pulses. The driver output, in turn, toggles the output stage. This action results in the switching of high-level dc current in the primary of the output transformers. The secondaries of the output transformers feed a full-wave rectifier system. Filtering is accomplished by a choke input LC network, and crowbar-type protection circuitry is connected across the dc output.

## Operation

Supply operation is divided into two categories: (1) general operating considerations, and (2) specialized operational modes.

## General Operating Considerations

The Logic Power Supply - 2 is an integral part of the B 1700 System and requires no attention from the operator. Upon application of primary ac power, the supply sequences itself in an orderly manner. Until the +4.75 and -2.0 volt supplies rise to their operating levels, a CLEAR signal is sent to the processor. This causes the processor to perform its normal clearing function, initializing the system for operation.

The supply is self-compensating for differences in ac line voltage, and requires no adjustment or modification for input voltages over the range of 188 through 253 volts ac. In addition, the supply is designed to accommodate temporary severe undervoltage (brownout) conditions on the ac line. Once started at 180 volts ac minimum, the supply continues producing full output down to 130 volts ac input.

## Specialized Operational Modes

There are three specialized operational modes in which the Logic Power Supply -2 can be used: normal, slave, and test. In the normal mode, all portions of the supply are active, and all controlling and regulating functions are accomplished internally. In the slave mode, regulation control of both the +4.75 and -2.0 volt channels is transferred to the "master" supply. The +12 and -12 volt channels are unaffected. The slave mode is used only in the second supply of a pair connected in parallel for increased current output. The test mode is a special variation in which the +300 volt supply (which powers the inverter output stages) is operated at a reduced input voltage to allow non-destructive troubleshooting. In the test mode, the +300 volt supply input is connected to the secondary of the auxiliary supply transformer. This transformer has a secondary voltage of 30 volts ac, resulting in an approximate 10 -to -1 reduction of voltage applied to the inverters. The test mode is used only for bench testing when the supply is disconnected from the data processing system.

## Physical and Operating Specifications

The physical and operating specifications of the Logic Power Supply -2 are as follows:


## B 1700 Power Subsystem

## LOGIC POWER SUPPLY-1, -3 , and -4

Logic Power Supplies-1, -3 , and 4 (figure 14) are of the inverter-rectifier type, with a single SCR inverter being used to produce all the supply output voltages. The inverter is controlled by a sensing circuit to vary the frequency of fixed-length driving pulses in response to load requirements on the +4.75 volt output. The -2.0 volt output is controlled by a shunt regulator, while the +12 volt and -12 volt outputs have individual series regulators. Internal operating voltage for the inverter is provided by a controlled bridge rectifier operating directly from the ac line, while low level circuitry throughout the unit is powered by the outputs of an additional ac operated control supply.

## Logic Power Supply Sections

The individual sections which make up the Logic Power Supply-1, -3 and -4 are described in the following paragraphs.

## Power Supply AC Control

The power supply ac control feeds ac power to the various portions of the power supply that require ac power. The AC control performs the following functions:
a. Manual switching of the input ac power.

## NOTE

This switching is normally done externally.
b. Input overcurrent sensing and shutdown by circuit breaker action.
c. Additional shutdown capability when a +4.75 V or -2.0 V output overvoltage is sensed, using an auxiliary trip coil on the circuit breaker. Note that the crowbar is also tripped when an overvoltage condition occurs.
d. Main heat sink overtemperature sensing, with shutdown of the internal control supplies (thus removing the outputs) when this condition occurs.
e. Suppression of unwanted radio frequency signals, preventing both externally generated signals from entering the supply, and internally generated signals from being coupled to the power line.

## +160 Volt Supply and Regulator

The +160 volt supply provides the internal operating voltage used by the inverter section of the Logic Power Supply-1, -3 , or 4. The +160 volt supply consists of a diode/SCR bridge rectifier operating directly from the power line, plus a control circuit to provide regulation by varying the firing time (in each ac half cycle) of the SCR's in the bridge. The +160 volt regulator also has a built-in line-operated supply to provide internal operating voltages.

## Inverter

A single high-power inverter is used to produce all four logic supply output voltages. The inverter consists of a four-leg (bridge) SCR circuit to switch dc current in the primary of a transformer. From the transformer secondaries square wave ac is rectified to produre the de output voltages. The operation of the inverter is controlled by varying the frequency of its SCR triggering pulses. Since the inverter pulses are fixed length (as determined by circuit constants), regulation is accomplished by changing the percentage of time in which current is allowed to flow to the load. The SCR triggering is controlled by a Comparator/VCO/Gate Driver circuit which monitors the +4.75 volt output (only). The regulation for the other three outputs is accomplished independently by conventional dc regulation circuits.



Figure 1-4. Logic Power Supply -1, 3 or -4

## High Current Supply

The high current supply, which provides both the +4.75 volt and -2.0 volt outputs, consists of a full-wave, center-tapped rectifier that produces a nominal output of 6.75 volts under load. The rectifier output is floating, with the positive terminal being used as the +4.75 volt supply output, and the negative terminal as the -2.0 volt output. The supply ground terminal is established artificially by a -2.0 volt shunt regulator circuit to provide a constant drop between "ground" and the -2.0 volt terminal. As mentioned previously, regulation control for the +4.75 volt output is accomplished by varying the inverter pulse frequency. A crowbar circuit is also provided to short out the high current outputs when an overvoltage condition is detected.

## $\pm 12$ Volt Supplies

The +12 volt and -12 volt supplies are nearly identical, differing only by the output terminal that is grounded. Rather than being independent units, the 12 volt supplies derive their operating power from the output of the main logic supply inverter. As such, each supply consists of a bridge rectifier (connected to a secondary winding of the inverter output transformer) and a series regulator circuit. The regulator incorporates current limiting plus overvoltage sensing and automatic shutdown through a crowbar circuit. Since the main inverter output varies in response to loading of the +4.75 V supply line, this factor as well as variations in their own loads must be compensated for by the 12 volt regulators.

## Control Supply

The control supply (actually two supplies in one) provides the internal operating voltages for low level circuitry within the logic supply, producing regulated outputs of $+24 \mathrm{~V},+4.5 \mathrm{~V}$, and -1.9 V from one section and $\pm 15 \mathrm{~V}$ from the other. The supply is ac line operated, sharing an input step-down transformer with the +160 volt regulator.

The $\pm 15$ volt supply consists of a single bridge rectifier followed by a pair of series regulators. The transformer center tap is used as ground, with the plus and minus terminals of the bridge feeding the plus and minus 15 volt regulators respectively. The regulators are the self-contained integrated circuit type, each driving an external pass transistor, and incorporating current limiting.

The multi-output control supply section consists of one bridge rectifier and pre-regulator, plus a secondary regulator for each of its three output voltages. The secondary regulators for the +24 V and +4.5 V outputs are the series type, and in each case consist of an integrated circuit driving an external pass transistor.

The -1.9 volt output utilizes a shunt regulator (also an integrated circuit with external pass transistor). The ground reference of the multi-output section is floating, being established by the -1.9 volt shunt regulator.

## Operation (Logic Power Supply-1, -3, and -4)

Supply operation is divided into two categories: general operating considerations and specialized operating modes.

## General Operating Considerations

The Logic Power Supplies-1, -3, or -4 (an integral part of B 1700 Systems) require no attention by the operator. Upon application of primary power, the supply initiates operations in an orderly manner. A CLEAR signal is sent to the processor for a predetermined time each time power is applied. This function causes the processor to perform its normal "clearing" function, thereby initializing the system for operation.

## NOTE

The supply is self-compensating for differences in line voltage, and requires no adjustment or modification for input voltage from the range of 188 through 253 volts ac.

## Specialized Operational Modes

There are three specialized operational modes in which the B 1700 Logic Power Supplies $-1,-3$, and -4 can be used: normal, slave, and test. In the normal mode, all portions of the supply are active, and all controlling and regulating functions are accomplished internally. In the slave mode (LPS-4 only), regulation control of the +4.75 volt and -2.0 volt outputs is transferred to a master supply. The +12 and -12 volt outputs are unaffected. The slave mode is used only in the second supply of a pair connected in parallel for increased current output. The test mode is used for troubleshooting and repair work, and involves operating the supply with a dummy load connected to the output. In the test mode, a number of options regarding operation of the supply's internal circuits can be exercised to assist in fault location.

## Physical and Operating Specifications (Logic Power Supply -1, -3, and -4)



## MEMORY POWER SUPPLY

The memory power supply (figure 1-5) provides the operating voltages for the dynamic RAM (Random Access Memory) S-memory used in the B 1700 central system. The supply operates from 188 through 253 volts ac, RMS, $50 / 60 \mathrm{~Hz}$, single phase primary input power, and produces three dc output voltages as follows:
a. $\quad-5.0$ Volts. Used as the negative supply voltage for dual sense amplifiers within the memory, with a nominal output current of 2.5 Amperes.
b. $\quad+19.0$ Volts. Used as the Vss (source voltage) by the RAM memory chips, with a maximum continuous output current of 10 Amperes.
c. $\quad+23.0$ Volts. (Actually +4 Volts referenced to the +19.0 Volt output.) Used as the Vbb (substrate voltage) by the RAM memory chips, with a maximum continuous output current of 1.5 amperes.

The memory power supply provides the power necessary to operate one 64 -kilobyte memory unit. Where memory sizes exceed this figure, additional memory supplies are used as appropriate.

There are several versions of memory power supplies. The various models, along with appropriate comments, are as follows:

| Burroughs Part Number | Vendor Part Number | Comments |
| :---: | :---: | :--- |
|  |  | Original Design |
| 22014229 | PEC 3604 | Redesign |
| 22111942 | PEC 3604A | Modification of 3604A for use |
| 22109052 | PEC 3604B | with Logic Power Supply-2 |

The memory power supply is the rectifier - series regulator type, and operates from the ac line. The unit is three supplies in one, all of which operate from secondary windings of a single input transformer and are similar in circuit design. Each of the supply sections incorporates series regulation and current limiting (controlled by an integrated circuit regulator), plus output overvoltage sensing and protective deactivation by a crowbar circuit.


Figure 1-5. Memory Power Supply

## MEMORY POWER SUPPLY SECTIONS

The three individual supplies within the memory power supply are described in the following paragraphs.

## -5 Volt Supply

The -5 volt supply consists of a full-wave, center-tapped rectifier, filters, an integrated circuit regulator, and a crowbar circuit. The supply operates from a winding in the secondary of T 1 , the main memory supply transformer. The -5 volt supply positive output is connected to the common (ground), with the negative lead being the -5 volt output. A separate sense lead is provided for sensing the output voltage at the point of use.

## +19 Volt Supply

The +19 volt supply is similar to the -5 volt circuit, except for the utilization of the positive and negative outputs (the negative is grounded) and uses heavier components due to the higher output current.

## +4 Volt Supply

The +4 volt supply (also similar to the -5 volt circuit), has its negative lead connected to the +19 volt supply's positive output. This causes the +4 volt positive lead to become +23 volts with respect to ground. An additional feature incorporated in the +4 volt supply consists of a tracking circuit to prevent the +23 volt output from falling below the +19 volt level under any circumstances. Also included are a half-wave rectifier and filter to provide operating power for the integrated circuit regulators of the +4 volt and +19 volt supplies.

## OPERATION

Application of ac power to the memory supply is controlled by the ac control circuit in the central system. The memory supply operates continuously whenever the system power is ON . There are no operator controls.

## PHYSICAL AND OPERATING SPECIFICATIONS

The physical and operating specificatons of the memory power supply are as follows:


## +20 VOLT PAPER TAPE POWER SUPPLY

The +20 volt paper tape power supply (figure 1-6) serves as an auxiliary power source for operation of a peripheral paper tape reader or paper tape punch. As such, the supply's operation is independent of the B 1700 Central System, although it is located within the system cabinet. The supply operates from 188 through 253 volts ac, RMS, $50 / 60 \mathrm{~Hz}$, single phase primary input power and produces a single dc output voltage of +20.0 volts at a nominal output current of 1.0 ampere.

The +20 volt paper tape power supply is of the rectifier-series regulator type, and incorporates current limitng and external overvoltage protection. The voltage regulation and current limiting features are controlled by an internal integrated circuit regulator, while the overvoltage protection is provided by an independent external circuit.


Figure 1-6. +20 Volt Paper Tape Power Supply

## OPERATION

AC power is applied to the +20 volt paper tape power supply whenever the system power is ON. There are no operator controls.

## PHYSICAL AND OPERATING SPECIFICATIONS

| Dimensions | . | . | . | . | Width: $3-3 / 16$ inches |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |
|  |  | Depth: <br> Height: $6-1 / 2$ inches |  |  |  |  |
| Weight . . . . . . . . . . . . . | 6 pounds |  |  |  |  |  |

## SYSTEM AC CONTROL

The system ac control (figure 1-7) is that portion of the central system through which ac power is applied to the various devices that use the control. The system ac control serves four distinct purposes as follows:
a. To provide distribution of ac power to the central system and several additional peripheral devices.
b. To control the application of ac power to the central system itself.
c. To protect the central system from damage due to ventilation failure.
d. To supply a power-line derived ac signal to the system real-time clock circuit.

The central system ac control consists of relays, circuit breakers, fuses and switches. The control is located in its own subchassis within the central system cabinet.

## SYSTEM AC CONTROL OPERATION

Since the system ac control serves to implement the on/off functions selected by the console ON/OFF switch, its operation directly follows the states chosen by the ON/OFF switch. Four states can exist within the control and are described as follows:

OFF: ac power is available for the use by the central system, but is switched OFF. This state is indicated by illumination of the console OFF lamp.

ON: ac power is applied to the central system. This state is indicated by illumination of the console ON lamp.
OVER TEMPERATURE: ac power has been removed from the central system due to failure of one or more ventilating fans. This state is indicated by illumination of the console TEMP lamp, and can be reset only by returning to the OFF state.

POWER UNAVAILABLE: ac power is not available at the system inputs due to tripping of the main circuit breaker, disconnection, or other cause external to the system. This state is indicated by all three indicator lamps (OFF, ON and TEMP) being extinguished.


Figure 1-7. System AC Control

## GLOSSARY OF TERMS

$$
\text { Name }
$$

Autotransformer Action
Circulating Current
Comparator
Complementary Transistor Logic (CTL)

Crowbar

## DVM

Floating Ground

## Foldback

Gate Driver

Inrush Control

Latching Relay

LED

Master Mode

Multivibrator

## Description

Transfer of energy between sections of an electrically continuous winding due to mutual coupling. One section of the winding must be excited externally for this action to occur.

Undesirable flow of current within a circuit, or between circuits, resulting from imbalances or misadjustments.

A circuit or device which compares two signals (or voltages), and produces an output proportional to the difference between them.

A digital logic circuit configuration making use of complementary transistor, emitter-coupled AND/OR gates.

A protective device (usually an SCR circuit) which, when triggered, applies a direct short circuit across the output of a power supply. Crowbars usually are employed where a positive, quick acting means of protecting external circuits from excessive voltages is needed.

Digital Voltmeter.

A circuit design which uses some level other than earth or chassis ground as the power source reference.

Overcompensation for a paraineter which is beyond acceptable limits.
A circuit which produces triggering pulses to devices capable of being gated (such as silicon controlled rectifiers).

Control of ac input current. In the logic power supply, this is accomplished by controlling the firing time of SCR legs in an input bridge rectifier. Inrush control action is a one-time event occurring each time the supply is powered up.

A relay with contacts that lock in either the energized or deenergized position (or both). The latching action may be accomplished electrically or mechanically.

Light Emitting Diode. A semiconductor device capable of producing light.

An operational mode in which power supply regulation is controlled entirely from within the supply. The voltage comparator output for both the +4.75 and -2.0 volt regulators in a "master" supply is used to drive these same regulators in a second, parallel-connected supply operating in the slave mode.

A relaxation oscillator in which the in-phase feedback voltage is obtained from two active devices. The frequency of oscillation is determined by resistive-capacitive elements which couple the output of each active device to the input of its counterpart.

Name
Offset Voltage Level
Operational Amplifier (Opamp)

Resistance-Capacitance (RC) circuit

Secondary Regulator

Series Regulator

Shunt Regulator

Slave Mode

Speedup Inductor

Steering Signals

Description
This level is the difference in operating potentials (with respect to ground) detected between the left and right legs of inverter output stages.

Any of several types of dc amplifiers having single or differential inputs and/or outputs. Operational amplifiers are generally used for circuit control. See "Comparator."

A time-determining network of resistors and capacitors. The time constant is defined as resistance times capacitance ( $\mathrm{R} \times \mathrm{C}$ ).

A voltage regulator which services a voltage source that has already been regulated by another device. Used where extreme precision in setting voltage levels is required.

A voltage regulator which operates by creating a dynamic resistance between a power source and its load. This resistance is inversely proportional to the load, and serves to maintain the total voltage drop at a constant level.

A voltage regulator which operates by creating a dynamic resistance in parallel with the actual load on a power source. This resistance is directly proportional to the load, and serves to maintain the voltage drop across the supply output at a constant level.
$\dot{A}$ operational mode in which power supply regulation is externally controlled. Contrast with Master Mode.

An inductor used to assist in causing a silicon controlled rectifier to cease conducting.

Control signals for circuit elements that are repeatedly switched on and off.

## SECTION 2

## FUNCTIONAL DETAIL

## GENERAL

This section describes the manner of operation and the major divisions of internal circuits of the various power devices employed in the B 1700 power subsystem.

## LOGIC POWER SUPPLY-2

The following discussion provides a functional description of the individual circuits of the Logic Power Supply-2. The power supply (figure 2-1) accepts single-phase ac input power and converts the power to several internal dc working voltages. The +15 and .15 volt supplies are used for operating low level circuits within the supply. The +300 and +150 volt outputs are used by the four inverter channels to produce the supply outputs. By alternately switching on and off their left and right legs, the inverters produce pulsating dc in the opposing halves of an output transformer primary. These pulses appear as ac on the transformer secondary, and are rectified and filtered. The four resulting pure dc voltages are the supply outputs that, in addition to supplying the load, are monitored by voltage and current-sensing circuits. These sensing circuits drive the regulators which, in turn, control the operation of each channel by varying the width of the inverter pulses. The remaining circuits shown in figure 2-1 perform specialized functions within the supply such as serving to guard against the potential hazards of output overvoltage and input current surges.

## MALFUNCTION PROTECTION CIRCUITS

The malfunction protection devices consist of active detectors that sense each of the output voltages, thermal switches mounted on the inverter heat sinks, and a circuit breaker with an auxiliary trip coil. These circuit elements are interconnected as shown in figure 2-2. Refer to table 2-1 for specific malfunction results.

The main circuit breaker can be tripped in several ways, as indicated in table 2-1. This circuit breaker is sensitive to a current surge and/or a sustained fractional overload. These two conditions are internal functions, and are affected only by the ac current flowing through the breaker. Also provided for protection is a dc trip coil, used for supply cutoff when excess heat sink temperature occurs (as sensed by thermal switches), or when the main crowbar trips due to an overvoltage on the +4.75 volt or -2.00 volt channel.

Control of the crowbar circuits is provided by differential operational amplifier detectors that monitor the output voltage of each channel. These detectors are separate and distinct from the sense amplifiers which control the regulation. The detectors, in each case, feed a trip signal generator circuit which produces the required crowbar pulse. Since the main crowbar is common to both the +4.75 and -2.00 volt channels, the detector circuitry is arranged so that an overvoltage condition on either channel can cause it to trip. Refer to figure 2-3.

An overvoltage condition on either the +4.75 or -2.00 volt supply output trips the circuit breaker (by its auxiliary trip coil) and the main crowbar. The circuit breaker can be tripped by the above overvoltage condition, by closing the thermal switches (which also energize the circuit breaker auxiliary trip coil), or by excessive current on the input line.

Tripping either the +12 or -12 volt crowbar does not affect the remainder of the supply, but renders the logic circuitry which uses that voltage inoperative. Resetting the 12 volt crowbars can be accomplished only by cycling the supply off, then on again.


Figure 2-1. Logic Power Supply-2 Basic Block Diagram


Figure 2-2. Overvoltage Protective Circuit Block Diagram
Table 2-1. Malfunction Results

\left.| Malfunction | Result |
| :--- | :--- |
| Excess primary current | Main circuit breaker trips. |
| Excess heat sink temp. | Main circuit breaker trips. |
| Overvoltage of +4.75 or -2.0 volts | Main circuit breaker and main crowbar trip. |
| Overvoltage of +12 volts | +12 volt crowbar trips. |
| Overvoltage of -12 volts | -12 volt crowbar trips. |\(\right\left.\} \begin{array}{l}Remainder of <br>

supply continues <br>

operating.\end{array}\right]\)



Figure 2-3. Clear Detector Block Diagram
Current-limiting on the dc outputs is not a malfunction and does not interrupt supply operation. The affected output voltage, however, is lowered by the limiting action. If a voltage reduction on either the +4.75 or -2.0 volt supply output is severe enough to allow the clear detector relay to drop out (see sequencing circuitry), the processor halts.

## SEQUENCING CIRCUITRY

Application of ac power is not controlled within the power supply, except for initial current-limiting in the +300 volt rectifier by the inrush control. Sequencing is accomplished by disabling the inverter circuits with a "hold-off" voltage. For the +4.75 and -2.00 volt channels, removing this voltage is a function of the +15 volt auxiliary supply level, and takes approximately 50 milliseconds after power is first applied. The purpose of sequencing is to ensure that the regulators are operating before the inverters begin producing output voltage. The +12 and -12 volt channels have a similar holdoff voltage controlled by the +4.75 volt output. This hold-off voltage is removed when the +4.75 voltage reaches its operating level.

Included also is a clear detector circuit which signals the processor that the supply is operational. This circuit is similar to the crowbar controls, except that the clear circuit output is derived by sensing an undervoltage condition on both the +4.75 and -2.00 volt channels. The CLEAR signal is removed when the output voltages of both supplies have reached their operating levels. Refer to figure 2-3.

Upon application of ac power, the sequence of events is as follows:
a. The +300 volt and $\pm 15$ volt (auxiliary) supplies begin operation. Inrush control prevents full functioning of the +300 volt supply until output filter capacitors have charged.
b. Low-level circuitry becomes active. Hold-off voltages are applied to all inverters.
c. The +4.75 and -2.0 volt hold-off voltage is disabled. The +4.75 and -2.0 volt inverters then begin operation.
d. The +4.75 volt output reaches operating level, disabling the +12 and -12 volt hold-off voltage. The +12 and -12 volt inverters begin operation. The auxiliary override function also takes place at this time.

## B 1700 Power Subsystem

e. The -2.0 volt output reaches its operating level and, in conjunction with the +4.75 volt supply output, terminates the CLEAR signal (which is sent to the processor).

## +300 VOLT SUPPLY AND INRUSH CONTROL

The +300 volt supply (figure 2-4) consists of a full-wave bridge rectifier operating directly from the ac power line and filtered by output capacitors. A voltage divider produces an additional output of +150 volts. Two legs of the bridge are comprised of silicon-controlled rectifiers for which the firing time is determined by an inrush control circuit. This circuit is designed to provide a "slow start" by enabling the bridge rectifier for progressively longer portions of each ac cycle until full operation is reached. The rate of operation of the inrush control circuit is determined by a resistor/capacitor (RC) time constant network, and is fixed. The inrush control circuit incorporates a reset feature that ensures a siow start will occur again in the event of a power interruption. An interlock is provided that closes a bleeder circuit across the +300 volt output when the top cover of the Logic Power Supply is removed. The supply can be operated when this cover is removed.

## $\pm 15$ VOLT AUXILIARY SUPPLY

The $\pm 15$ volt auxiliary supply consists of a step-down transformer and bridge recitifer (with center tap common), connected in parallel with a full-wave, center-tapped rectifier and associated current-driven, half-wave rectifier operating from the +4.75 volt inverter output. This latter is known as the auxiliary override circuit. The overall purpose of the auxiliary override circuit is to provide additional protection against line voltage fluctuations. Because the regulator circuit has considerable dynamic range, deriving the $\pm 15$ volt auxiliary voltages from the inverter output allows the supply to continue delivering full output voltage despite a severe undervoltage condition on the ac line. Both the full-wave and bridge rectifiers feed a common regulator circuit, as shown in figure 2-5. The +15 volt output is adjustable by a zener-controlled series regulator. Regulation of the -15 volt output is by zener diode only, and is non-adjustable.


Figure 2-4. +300 Volt Supply Block Diagram


Figure 2-5. $\pm 15$ Volt Auxiliary Supply Block Diagram
Power for the $\pm 15$ volt auxiliary supply is derived from the transformer and bridge rectifier only when ac power is first applied. When the +4.75 volt inverter begins operating, the auxiliary override circuit becomes active and assumes control of the supply. This action occurs because the voltage output of the auxiliary override rectifiers is somewhat higher than that of the transformer/bridge. This higher voltage effectively blocks the diodes in the bridge rectifier by applying reverse bias.

## MASTER OSCILLATOR, CLOCK, AND RAMP CIRCUITRY

The master oscillator produces an 18 -kilohertz sine wave signal, driving both the clock and ramp generators (see figure 2-6). This signal is not used for any other purpose within the circuit, and is fixed in frequency. Because they are derived from a common source, the CLK, CLK/, and ramp signals are synchronized. This relationship is significant since the ramp signal, which is a sawtooth waveform at twice the oscillator frequency, is used to generate disable pulses. These pulses shorten the inverter-switching pulses produced by CLK and CLK/. The operating levels of the master oscillator, clock, and ramp stages are all set by circuit constants, and are non-adjustable. The charging voltage for the ramp generator is taken from the unregulated output of the auxiliary override rectifier. This voltage is directly proportional to the ac line voltage, and therefore controls the level (slope) of the ramp. This provides a coarse method of compensating for fluctuations in the line voltage.


Figure 2-6. Master Oscillator, Clock, and Ramp Block Diagram

## REGULATORS

The regulator circuits produce disable pulses which limit the amount of time during which current flows in the inverters. In normal operation, the inverter pulses are always shorter than the CLK and CLK/ steering pulses which toggle them. This shortening action affects only the ratio of on-to-off time; the frequency does not change. Disable pulses are present during all supply operations except at initial start-up when the hold-off voltage is high. The hold-off voltage overrides all regulation control and forces a constant high disable level that prevents the inverters from operating.

The disable pulses are created by the combined action of the ramp signal and a dc control voltage. These pulses are applied to a comparator circuit which, in turn, controls a disable pulse generator. (See figure 2-7.) The ramp signal and the dc control voltage act in opposition, with the control voltage tending to inhibit the triggering action of the ramp. The control voltage sets a triggering threshold which the ramp (a sawtooth waveform) must overcome to activate the pulse generator. The length of the disable pulse is determined by the portion of the ramp pulse which exceeds the triggering threshold of the comparator. The relationship between the ramp, control voltage level, and disable pulse length is illustrated in figure 2-8. The disable pulse length is inversely proportional to the load.

The dc control voltage, on which regulation action depends, is derived from the output of a sense amplifier, that is, a differential operational amplifier circuit. This circuit has an adjustable reference voltage input, plus direct and remote sense inputs to which the dc output voltage of the channel is applied. Tied to the comparator, in parallel with the output of the sense amplifier, is the output of a current-limiter circuit. This circuit also generates a control voltage, and is responsive to the current flowing in the inverter output. The operation of the current limiter is such that when normal levels of current are flowing, the output is idle, allowing the sense amplifier to drive the comparator. When an excessive current flows, the current limiter becomes active, and its output overrides the influence of the sense amplifier.

## INVERTERS

The inverter consists of driver and output stages, rectifiers and filters, and crowbar protection circuits, as illustrated in figure 2-9. The driver and output stages of each inverter function together to produce the required output. The difference between these stages is their condition in the "resting" state. The resting state defined is that time when power is applied, but no output is present.

In the driver stage, "resting" is characterized by simultaneous conduction of both the left and right switching legs. This condition in the driver stage prevents operation of the output stage, causing both switching legs to be turned off. Conversely, switching one of the driver legs off triggers the corresponding leg in the output stage, generating an output pulse. Since the output stage cannot conduct when the driver is in the resting state, returning the driver to that condition terminates the output pulse.


Figure 2-7. Regulator Block Diagram (One Channel Only is Shown)


Figure 2-8. Disable Pulse Generation


Figure 2-9. Inverter Block Diagram (One Channel Only is Shown)

The inverter driver stages are toggled by the square-wave CLK and CLK/ steering signals, each of which controls one switching leg. Toggling the driver stage results in a similar but inverse action in the output stage; each switching leg conducts only for the length of time that the corresponding driver leg remains off. The inverter output (before rectification) reproduces nearly exact inverted versions of the steering pulses, except that the inverter output pulses are shorter than the steering pulses, due to the action of the disable pulses. Inverter timing is illustrated in figure 2-10.

All inverter driver stages are basically alike except for the following: the +4.75 volt inverter driver has parallel left and right switching legs. In addition, the +4.75 volt inverter output stage employs four legs, each with three switching transistors connected in a modified bridge configuration.

The +12 and -12 volt inverters have a single switching transistor in the left and right output legs, and the -2.0 volt inverter employs four paralleled switching transistors in each output leg. Where paralleled transistors are employed, special transformers are included to force simultaneous turn-on and equalized current-sharing among each associated group. As an additional modification to produce the higher output current required from the +4.75 and -2.0 volt inverters, each has a transformer-coupled feedback circuit within the output stage to provide additional base drive.

The crowbar circuit uses SCR's that, when activated, complete the circuit for a low-resistance bleeder. When the crowbar is activated, the output of the driver stage is clamped, effectively blocking the inverters. With the inverter thus deactivated, the crowbar SCR itself serves only to discharge the output filter capacitors, and can therefore be much smaller than if it were of the conventional type.

## LOGIC POWER SUPPLY-1, -3 , and -4

The following discussion provides a functional description of the individual circuits comprising the Logic Power Supply-1, -3 , and -4 . The supply, as shown in figure 2-11 accepts single-phase ac input power and converts it to several internal dc working voltages. Of these,+160 volts is used to operate the high power inverter from which all supply outputs are derived. The remaining $+24,-1.9,+15$, and -15 voltages are used for the operation of low level circuits.

The inverter functions by alternately switching on and off a dc current in the left and right halves of a transformer primary. These pulses appear as ac on the transformer secondaries, which is rectified and filtered to produce the various supply outputs. The inverter transformer has three secondary windings, and these are used for the +12 volt, -12 volt and combined $+4.75 /-2.0$ volt outputs respectively. Control of the inverter is maintained by a circuit which monitors the voltage on the +4.75 volt output (only), and varies accordingly the frequency of SCR triggering pulses fed to the inverter. Since the inverter pulses are of fixed length (as set by circuit constants), regulation is accomplished through control of their repetition frequency. The -2 volt (shunt) regulator functions independently, as do the +12 and -12 volt regulators. An overall block diagram of the supply is shown in figure 2-11.

## MALFUNCTION PROTECTION CIRCUITS

The protection of the power supply and the data processing system against supply malfunctions is provided by malfunction protection circuits that include a main ac circuit breaker, overvoltage detectors, and undervoltage detectors. These circuits function as described in the following paragraphs.

## Main AC Circuit Breaker

The main ac breaker removes input power to the supply when tripped. Tripping of the breaker is done two ways: internal action, and by activation of an auxiliary trip coil. Internal tripping of the breaker is a self-actuated function, and occurs when excessive current flows through the breaker. The auxiliary trip coil allows the breaker to be tripped when some external malfunction occurs which in this case is an overvoltage condition on the supply outputs. Overvoltage tripping is controlled by the +4.75 volt and -2.0 volt overvoltage detectors which are described in the following paragraphs.


NOTE: CLK AFFECTS LEFT DRIVER AND OUTPUT LEGS ONLY. CLK/ AFFECTS RIGHT DRIVER AND OUTPUT LEGS ONLY. DISABLE PULSES AFFECT BOTH.

Figure 2-10. Inverter Timing


## Overvoltage Detectors

A separate overvoltage detector circuit is provided for each of the supply outputs $(+4.75 \mathrm{v},-2.0 \mathrm{v},+12 \mathrm{v}$ and $-12 \mathrm{v})$. These detectors are operational amplifier comparators which are arranged to compare the actual output voltages of the supply with special reference voltages from the internal control supply. The overvoltage detectors are separate and distinct from the voltage regulation circuits, and their outputs are used exclusively to deactivate the supply section concerned when an overvoltage occurs.

The +4.75 volt and -2.0 volt overvoltage detectors (figure $2-12$ ) are connected so as to deactivate the entire supply when an overvoltage occurs on either output. When such a condition occurs, the detector concerned causes the main ac breaker to trip (by its auxiliary trip coil), and the main crowbar to fire. The main crowbar is a silicon controlled rectifier (SCR) which when fired, shorts together the +4.75 volt and -2.0 volt outputs. The +12 volt and -12 volt overvoltage detectors deactivate only the supply section they are associated with. When an overvoltage condition occurs on the +12 volt or -12 volt output, the corresponding detector causes a crowbar SCR in the section concerned to fire. Firing the +12 volt or -12 volt crowbar shorts the affected output to ground, causing that section's regulator to go into a current limiting condition. The remainder of the logic supply continues operating normally when crowbar firing occurs. To restore the affected section to proper operation, the entire supply must be cycled off, then on again.


Figure 2-12. Overvoltage Protection Circuit ( +4.75 V and -2.0 V Outputs Only)

## Undervoltage Detectors

Operational amplifier undervoltage detectors (figure 2-13) are also provided for the +4.75 volt and -2.0 volt outputs. As with the overvoltage circuits, these detectors are arranged to compare the supply outputs with reference voltages. The outputs of both detectors are ANDed, then fed to a one-shot multivibrator. The multivibrator provides a pulse of 5 seconds duration which controls a relay. The net operation of the circuit is to hold the relay in the de-energized state (thus generating a clear signal) for five seconds either following the first application of power or a dip in output voltage below acceptable levels. Generation of the clear signal during such periods prevents the processor from operating until the supply outputs have stabilized.

## NOTE

An excessive load on any of the supply outputs is not considered a malfunction. Such a condition simply causes the current limiting circuit of the affected output to act. Current limiting is usually manifested by a reduction in output voltage, while the current remains at the maximum allowable level. When such a condition occurs on the +4.75 volt or -2.0 volt output, generation of the clear signal results, even though no actual malfunction (within the supply) has occurred.


Figure 2-13. Undervoltage Detectors and Clear Signal Generator

## +160 VOLT SUPPLY AND REGULATOR

The +160 volt supply (figure $2-14$ ) provides the internal operating voltage for the inverter portion of the logic supply. The +160 volt supply is transformerless, having a controlled bridge rectifier operating directly from the ac line. The output of the +160 volt supply is regulated, and this feature is accomplished by controlling the conduction time (during each ac half cycle) of the SCR legs in the bridge rectifier itself. The +160 volt regulator therefore serves only to supply firing pulses for the SCRs in the bridge. Incorporated into the regulator are provisions for causing a "slow start" each time the logic supply is cycled on. The slow start feature prevents excessive current flow, which would otherwise occur due to charging of the +160 volt supply filter capacitors.


Figure 2-14. +160 Volt Supply and Regulator

## INVERTER

The single inverter (figure 2-15) within the logic supply consists of four SCRs in a bridge configuration. These SCRs alternately switch off and on high level dc currents in the left and right halves of a transformer primary winding (thus simulating the application of ac). The transformer secondary windings feed three separate rectifiers, from which the four dc outputs of the logic supply are derived.

Operation of the inverter is controlled by a timing circuit that provides firing pulses for the SCRs. The firing pulse frequency is determined by the +4.75 volt regulator, and serves to control the inverter output by varying its ratio of on-to-off time (conduction vs nonconduction of the SCR legs). Control of the output in this manner is possible because the inverter pulse length is fixed by circuit constants. Both voltage control and current limiting for the +4.75 volt supply output are accomplished through control of the inverter pulse frequency. Although the -2.0 volt, +12 volt and -12 volt logic supply outputs are also derived from the inverter, regulation control for each is accomplished separately by conventional (series or shunt regulation) methods.

## HIGH CURRENT SUPPLY

The high current supply (figure 2-16) consists of one secondary winding of the inverter transformer, a full-wave, center-tapped rectifier circuit, filters, and the -2.0 volt shunt regulator. The supply is essentially a single output unit from which both positive and negative outputs are derived. This feature is accomplished by creation of an artificial ground floating between the two output terminals. The floating ground is provided by the -2.0 volt shunt regulator, which maintains a constant drop between the negative output terminal and ground. The action of this regulator provides a constant 200 ampere drain on the negative output regardless of the actual load present.

As previously mentioned, regulation for the +4.75 volt output is accomplished through control of the inverter itself. Current limiting for the -2.0 volt output is inherent; that is to say that since the output is created by an artificial voltage drop, an attempted overload causes the voltage thereby developed to be proportionately reduced.

## $\pm 12$ VOLT SUPPLIES

The +12 volt and -12 volt supplies are identical except for connections to their output terminals. Therefore, the following description applies to both. Each 12 volt supply (figure 2-17) consists of a bridge rectifier followed by filters and a series regulator circuit. Included in the regulator are an integrated circuit comparator driving an external pass transistor, an overvoltage detector and crowbar firing circuit, and a sequencing circuit. The regulator functions conventionally, and includes provisions for current limiting. An overvoltage condition causes the 12 volt crowbar to fire, disabling that output (only).

## CONTROL SUPPLY

The control supply, which provides internal operating and reference voltages for the logic supply circuitry, is actually two supplies in one. Both sections are ac line operated, being fed from secondary windings of the +160 volt regulator input transformer. Each section consists of a bridge rectifier followed by regulators, and produces at least two outputs.



Figure 2-16. High Current Supply Block Diagram


Figure 2-17. 12 Volt Power Supply Block Diagram

## B 1700 Power Subsystem

The first section (figure 2-18) produces +15 and -15 volts, having individual series regulators on the positive and negative outputs of the bridge rectifier. In this arrangement, the transformer center tap is used as the common output (ground). The second section (figure 2-19) produces three outputs ( $+24,+4.5$ and -1.9 volts), doing so by a two-stage regulation process. The basic supply has a bridge rectifier and series regulator, and this is followed by secondary regulators for the +24 volt and +4.5 volt outputs. The -1.9 volt output is created in the same way as the -2.0 volt output of the logic supply, this being accomplished by a shunt regulator which maintains a 1.9 volt drop between the negative terminal of the bridge rectifier and the floating ground.

## MEMORY POWER SUPPLY FUNCTIONAL DETAIL

The memory power supply, (figure 2-20) converts the ac input to three reduced working voltages, then rectifies, filters and regulates each. Each regulator incorporates both voltage regulation and current limiting, and consists of an IC regulator driving one or more external pass transistors. Additional overcurrent/short circuit protection is provided for each supply section by a separate detector which activates a crowbar SCR. Tripping the crowbar shorts the supply output. Input protection is provided by a fuse in the primary of the main transformer.


Figure 2-18. $\pm 15$ Volt Section of Control Supply


Figure 2-19. $+24 \mathrm{~V},+4.5 \mathrm{~V}$ and -1.9 V Section of Control Supply


Figure 2-20. Memory Power Supply Block Diagram

## +20 VOLT PAPER TAPE POWER SUPPLY FUNCTIONAL DETAIL

The +20 volt paper tape power supply, (figure 2-21) consists of a step down transformer, a bridge rectifier and filter, an auxiliary half wave rectifier and filter, an IC regulator with two driver stages and a pass transistor, and an external overvoltage protection circuit.

## SYSTEM AC CONTROL FUNCTIONAL DETAIL

The basic functions of the system ac control (figure 2-22) are to remotely control the application of power to the central system, and to indicate the system power status. The circuit operates by using the contacts of a latching type ON/OFF switch to control a power relay in the ac line going to the central system. In the absence of a malfunction, pressing the console ON/OFF switch once causes power to be applied to the central system (including the logic and memory power supplies, the ventilating fans, and the real time clock circuit). Pressing the ON/OFF switch again removes the power. The control lines between ON/OFF switch and the power relay pass through the contacts of a latching relay. These latching relay contacts are normally closed.

To protect against damage to the system logic due to a ventilation system failure, airflow switches are built into the fan assemblies. The airflow switches are connected to a time delay relay such that if one of them closes for the delay period (indicating a lack of airflow), the time delay relay closes. The closing of the time delay relay contacts picks the latching relay, which in turn, breaks the circuit activating the power relay. This action causes the power relay to drop out, removing ac power from the central system. Picking the latching relay also illuminates the TEMP lamp and extinguishes the ON lamp within the ON/OFF switch. The over-temperature condition (latching relay picked) is reset by pressing the ON/OFF switch.


Figure 2-21. +20 Volt Paper Tape Power Supply Block Diagram


Figure 2-22. System AC Control Block Diagram

## B 1700 Power Subsystem

## SECTION 3

## CIRCUIT DETAIL

## GENERAL

This section describes in detail the functioning of the individual circuits within the various power supply and control devices employed in the B 1700 system.

## LOGIC POWER SUPPLY-2

The following circuits within the Logic Power Supply-2 are described in this section:
a. AC inputs.
b. +300 volt supply.
c. Inrush control.
d. $\pm 15$ volt auxiliary supply.
e. Master oscillator, clock, and ramp.
f. Overvoltage and undervoltage detector and crowbar control.
g. Sequencing circuitry.
h. Inverter channels.

## AC INPUT

The unregulated 188 through 235 volt ac power (figure 3-1) enters the supply through circuit breaker CB1 and through the RF1 filter to the +300 volt bridge rectifier (CR101 through CR104). Also connected across the ac line are fans B1, B2, and B3, plus transformer T5, which feeds the $\pm 15$ volt Auxiliary Supply. The fans are all 115 -volt types, with B1 and B2 connected in parallel, and this combination connected in series with B3. The common line between B1, B2, and B3 is extended to the center tap of T5, to help equalize the voltage drop across the fans.
+300 VOLT SUPPLY AND INRUSH CONTROL

The +300 volt supply consists of diode rectifiers CR101 and CR102, and silicon-controlled rectifiers (SCR) CR103 and CR104, which are connected in a bridge configuration. The rectifying action of the bridge is controlled by the firing time of the SCR legs. This firing time is determined by the inrush control circuit. The inrush control provides a "slow start" when the supply is first turned on by delaying SCR firing until late in the voltage cycle. This delay is progressively shortened according to a predetermined time constant until 66 percent full-time operation is reached. The overall purpose of the inrush control is to prevent excessive surge currents from flowing while the supply filter capacitors are charging.


Figure 3-1. AC Input and +300 Volt Supply (Less Inrush Control)

## +300 Volt Supply

The remainder of the +300 volt supply, exclusive of the inrush control, consists of main filter capacitors C102, 103, 104 and 105. These are followed by a voltage divider comprised of capacitors C122 and C123, and resistors R125 and R127. This voltage divider produces an additional output of +150 volts. A bleeder resistor (R176) is provided to discharge the main filter capacitors when interlock switch S101 is closed (when the supply cover is removed). The interlock reduces the shock hazard when the supply is opened for service or maintenance.

The +150 volt output is significant only in that it establishes a reference point about which the voltages appearing across the inverter output legs are centered. The voltage divider serves to provide an artificial center tap which maintains a constant drop of 150 volts across all switching legs not conducting. This consideration is necessary for transistor protection. Note that the voltage divider does not form a current path for the inverter-switching pulses.

## B 1700 Power Subsystem

## Lheush Contī̀l

The inrush control (figure 3-2) operates directly from the ac line, deriving its operating power from a bridge rectifier composed of diodes CR501, CR502, CR506, and CR507. The power SCR firing pulses (the output of the inrush control) are generated by pilot SCRs CR511 and CR514. These SCRs are alternately triggered by pulses from the ac line through resistors R511 and R516. In the absence of further influence from the remainder of the inrush control circuit, the portions just described would allow early triggering of the pilot SCRs, and therefore almost full-time functioning of the +300 volt bridge rectifier.

Triggering of the pilot SCRs is controlled by transistors Q504 and Q505. When these transistors conduct, the ac iine pulses are prevented from acting upon the SCRs. Transistors Q504 and Q505 are both controlled by Q503 which, in turn, follows Q502, from which overall control of the circuit emanates. Conduction of Q502 is dependent on the time constant of the RC circuit comprised of $\mathrm{R} 504, \mathrm{R} 505$, and C 502 . Because the operating voltage of the inrush control is unfiltered, pulsating dc at twice the ac line frequency, C 502 charges once each half-cycle, causing Q502 to conduct when its bias threshold is reached. The time constant of $\mathbf{C} 502$ is a function of the charging voltage; it is this controlled parameter that provides the "slow start."

A second RC circuit, composed of R501, R504, and C501 is used to control the charging voltage of C502. This circuit has a much longer time constant, and serves to hold the voltage at the junction of R505 and R504 at a reduced value for the slow-start period. Also incorporated in the inrush control is a reset feature to provide a repetition of the slow start procedure if the ac input power is interrupted. This is provided by Q501, which discharges C501 when the supply voltage is lost. Transistor Q501 conducts because its base bias (as determined by R501 and R502) drops to 0 when power goes off. The time constant of this circuit is such that resetting will occur if power is lost for more than 3 or 4 cycles of the ac line.

An additional feature of the inrush control is the network made up of CR517, CR518, C507, and R522. This network provides suppression of RFI noise generated by the firing of pilot SCRs CR511 and CR514. Diode CR516 and resistor R520 provide a return path for the power SCR firing pulses.

## Inrush Control Sequence of Operation

When power is first applied, the voltage at the junction of R504 and R505 is held at a very low level, due to the initial charging of C501. Consequently, it takes almost the full half-cycle for C502 to charge to the bias threshold of Q502. At this point Q502 conducts, which, in turn, causes Q503 to conduct. The conduction of Q503 causes Q504 and Q505 to be cut off, allowing the ac line pulse to fire either pilot SCR CR511 or CR514.

The pilot SCRs fire alternately, in response to the changing direction of current flow in the ac line. Firing one of the pilot SCRs in turn fires the corresponding power SCR, activating one side of the +300 volt bridge rectifier.

Because of the reduced rate at which C502 is allowed to charge, firing of the SCRs is delayed until near the end of the first half-cycle. On subsequent cycles, the voltage at the junction of R504 and R505 rises as C501 continues to charge. As this voltage continues to rise, C502 charges in progressively shorter periods of time, causing the SCRs to be fired earlier in the cycle. This continues until a preset equilibrium point is reached which limits the delay to approximately 60 of the 180 degrees of the half-cycle. The voltage on C 501 reaches a level of approximately +30 volts, beyond which it cannot go. This level is established by diodes CR508 and CR510, which form a clamping circuit with the collectors of Q504 and Q505.

The 60 -degree delay point is the normal operating condition of the supply. This is the area at which the supply develops full output voltage. Operation continues in this manner until the supply voltage is interrupted. At that point Q501 conducts, discharging C501 through R503, and resetting the inrush control.


## B 1700 Power Subsystem

## $\pm 15$ VOLT AUXILIARY SUPPLY

The $\pm 15$ volt auxiliary supply (figure 3-3) is a dual-input supply. During initial start-up it functions as a conventional ac line-operated supply that employs a step-down transformer and bridge rectifier. When the +4.75 volt inverter channel begins operation, the auxiliary override circuit becomes active, allowing the $\pm 15$ volt supply to function from the windings in the secondaries of the +4.75 volt output transformers. This supply produces output voltages similar to, but higher than, the voltages from the bridge. The override voltages disable the bridge by back-biasing the bridge diodes.

Since the auxiliary override circuit pertains directly to the $\pm 15$ voltage auxiliary supply, it is discussed in this section, rather than with the +4.75 volt inverter, of which it is a part.

## Conventional Supply and Regulators

The conventional supply is composed of transformer T5 and rectifier diodes CR105, CR106, CR107, and CR108. The center tap of the transformer is used as a common line, with the front and back terminals of the bridge used to supply positive and negative levels of approximately 15 volts each. Once filtered by capacitors C107 and C108, these voltages are passed to the regulators.

The +15 volt regulator is a zener-referenced series-type, and is adjustable. Zener diode CR109 provides a reference voltage of


Figure 3-3. $\pm 15$ Volt Auxiliary Supply

## B 1700 Power Subsystem

Potentiometer R108 (+15V ADJUST) maintains proper current flow through Q103 by adjustment of the base bias of Q103. Transistor Q103 controls Q102 and, subsequently, controls the Darlington-coupled pair (Q101), comprising the series regulator. The -15 volt supply is zener-regulated only, and is fixed. Zener diode CR110 provides the -15 volt regulation.

## Auxiliary Override Circuit

The auxiliary override rectifiers operate from windings in the secondaries of T101 and T102, the +4.75 volt inverter output transformers. The +15 volt auxiliary override voltage is produced by a full-wave, center-tapped rectifier composed of CR138 and CR139. Current transformer T114 is connected in series with the output of the +15 volt rectifier, and its secondary is used to produce the -15 volt auxiliary override voltage through CR140. The center tap line from transformers T101 and T 102 is used as common for both supplies. An additional peak detector circuit, composed of CR137 and R124, is connected to the output of the +15 volt rectifier. The output from this circuit is used to supply a portion of the ramp generator circuit. The $\pm 15$ volt auxiliary supply override voltages, plus the common are fed to the +15 volt auxiliary supply at TP1, TP6, and TP4, respectively.

## MASTER OSCILLATOR, CLOCK SIGNAL GENERATOR AND RAMP GENERATOR

The master oscillator generates the clock and ramp signals to provide overall system timing.

## Master Oscillator

The clock frequency of the system is generated by the Master Oscillator circuit (figure 34) consisting of Q217, R282, R283, C217, C218, C219, R284, R285, and the primary of transformer T201. The oscillator operates in the range of 18.0 kilohertz to 19.6 kilohertz ( 18.8 kilohertz nominal).

## Clock

The sine wave clock signal is coupled through T201 to square-wave generators Q218 and Q219. One side of the secondary winding of T201 is connected to the base of Q218, and the other to Q219, so that they are toggled alternately, producing the CLK and CLK/ signals. Operating voltage for the square-wave generator stages is provided through R441, R286, R289 and R442. Resistors R287 and R288 supply base bias for Q218 and Q219 respectively.


Figure 3-4. Master Oscillator, Clock and Ramp Generator

## Ramp

The secondary of T201 also connects, through CR224, CR225, R290 and C225, to the base of Q220. Transistor Q220, in conjunction with Q221 and associated components R291, R292, R423 and C220, generates the ramp signal. The ramp is a sawtooth waveform, twice the oscillator frequency. It is non-adjustable, but the level does vary in response to changes in the ac line voltage.

This change in the ramp signal level has a direct effect on the regulator circuitry, and such adjustment is used to provide a form of coarse regulation to compensate for changes in the line voltage. This is accomplished by Q220, which derives its power from the peak detector in the auxiliary override circuit. An increase in the ac line voltage results in a proportional increase in the peak detector voltage, and thereby the level of the ramp. The higher ramp voltage increases the action of the regulators, reducing the inverter output. This ramp circuit is necessary since, in addition to changes in load, the inverter output stages are responsive to changes in the level of their operating voltages, which come from the unregulated +300 volt supply.

## MALFUNCTION PROTECTION CIRCUITS, CLEAR DETECTOR, AND +10 VOLT REFERENCE SUPPLY

Overvoltage and undervoltage detection for control of the crowbar circuits and generation of the CLEAR signal is a separate function, as distinguished from the sense amplifiers which control the regulation of the supply. Differential operational amplifier detectors are, provided for overvoltage sensing in all four of the inverter outputs. Similar undervoltage detectors are provided for the +4.75 and -2.0 volt outputs. Provisions have been made within the circuit for inclusion of this function for both 12 -volt outputs as well. This is an option that is not utilized in the present version of the supply; therefore, etching for the $\pm 12$ volt undervoltage detectors is present on the circuit board, but the necessary components are omitted.

Functionally, the overvoltage detectors are used to activate the crowbar circuits. Since the main crowbar circuit is common to both the +4.75 and -2.0 volt outputs, the corresponding overvoltage detectors are arranged so that either may cause crowbar activation. Conversely, the 12 -volt crowbar circuits function independently.

The undervoltage detectors are used for generation of the CLEAR signal, which goes to the processor. The absence of an undervoltage condition on both the +4.75 volt and -2.0 volt channels is required for deactivation of the CLEAR signal.

The differential operational amplifier (op amp) detectors use voltage dividers for input sensing. These dividers are fed from both the supply outputs and a reference voltage. Since the Logic Power Supply-2 design requirements specify provisions for a common-point system ground, return lines for the individual voltage outputs are floating with respect to the chassis and auxiliary common. Therefore, sensing is provided on the return lines. The network of voltage dividers employed within the circuitry permits each detector to sense only the voltage between the corresponding supply output and return lines while utilizing the same reference voltage as the other detectors in the supply.

The reference voltage ( +10.0 volts) is provided by a special reference supply operating from the +15 volt auxiliary voltage. The reference supply serves as a secondary regulator, providing a highly regulated source for the voltage dividers used in the sensing circuits.

## Main Malfunction Protection Circuit (Including Main Crowbar)

The main malfunction protection circuit consists of a crowbar SCR connected between the +4.75 and -2.0 volt output terminals, an auxiliary trip coil on the ac circuit breaker, and additional circuit elements for activating both. Only one crowbar is needed, since the high current outputs are of the opposite polarity and share a common ground terminal. Basically, the main crowbar circuit is actuated whenever the overvoltage trip signal is received from either the +4.75 or -2.0 volt overvoltage detectors. Activating the main crowbar circuit also trips the breaker, shutting down the entire supply. It is also possible to trip the ac breaker without firing the crowbar circuit. This occurs whenever an ac input overload is present (an internal function of the breaker itself), or one of the heat sink thermal switches closes.

Functionally, the overvoltage trip signal fires pilot SCR CR112, opening a path from the +15 volt auxiliary supply line to common through the auxiliary trip coil of CB1 and T133 (see figure 3-5). The rush of current trips the breaker and, by way of a pulse induced in the secondary of T133, fires crowbar SCR CR156. The firing of CR112 also opens a discharge path (through CR113, CR116 and CR141) for the voltage supply lines from which the +4.75 volt and -2.0 volt inverter driver stages operate. This action disables both inverter channels. SCR CR156 and R125 serve only as a triggerable bleeder, whose

## B 1700 Power Subsystem

function is to discharge the output filter capacitors. Tripping CB1 may also be accomplished by closing any of the three heat sink thermal switches (S102, S103 or S104). These switches are connected in parallel with the pilot SCR (CR112)-T133 combination, and therefore trip the breaker. This action does not fire the crowbar.


Figure 3-5. Main Malfunction Protection Circuit

## +4.75 Volt Overvoltage Detector

The +4.75 volt overvoltage detector (figure 3-6) consists of operational amplifier Z 207 and two voltage dividers composed of R221, R222, R223 and R224, R225, R226, R227. Both voltage dividers are shared with Z208. Also included is feedback resistor R254. This detector is the only one of the circuit that is adjustable. Its output feeds Q213 which, when conducting, produces the main crowbar trip signal. Note that Q212, which is driven by the -2.0 volt overvoltage detector, can also produce this trip signal.

Functionally, the inverting input of Z 207 is driven by the +4.75 volt supply output, and the non-inverting input is driven by the common return. Either a relative increase in potential at the +4.75 volt output or a decrease at the common return drives the operational amplifier output in a negative direction. The voltage level at the inverting input is set by potentiometer R226 (4.75V O.V. ADJUST), governing overall operation of the stage. When the output voltage of Z 207 is reduced to +11 volts (from its normal of +15 volts), Q213 conducts, activating the crowbar circuit, clamping the +4.75 and -2.0 volt inverter inputs, and tripping the main circuit breaker. To prevent undesired overvoltage sensing during testing and adjustment work, an OVERVOLTAGE DISABLE switch (S201) is provided which disconnects the trip line running from Q212 and 213.

In addition to the sensing circuitry, the +4.75 volt overvoltage detector includes an overvoltage pulse generator consisting of CR213, CR214, R256, R257, C211, and Q207. See figure 5-5. The components of this circuit are omitted from the Logic Power Supply used in the B 1700 systems because present designs do not require an external +4.75 volt overvoltage pulse.


Figure 3-6. +4.75 Volt and -2.0 Volt Overvoltage Detectors

## -2.0 Volt Overvoltage Detector

The -2.0 volt overvoltage detector (figure 3-6) is similar to the +4.75 volt overvoltage detector except that its trip point is fixed. In addition, the connections to the inverting and non-inverting inputs of the operational amplifier are transposed. This is due to the overvoltage condition on the -2.0 volt output being in reverse (with respect to polarity) to that of the +4.75 volt output.

This overvoltage detector consists of operational amplifier Z205, and two voltage dividers composed of R214, R215, R216 and R217, R218, R219, R229. Both voltage dividers are also shared with Z206 (see figure 2-5). Also included is feedback resistor R246. The output of Z205 drives Q212, which, when conducting, activates the main crowbar circuit and breaker (CB1), and clamps the +4.75 and -2.0 volt inverters.

Device Z205 also drives a - 2.0 volt overvoltage pulse generator that is composed of CR209, CR210, R247, R249, C208, and Q205. The components of the 2.0 volt overvoltage pulse generator are omitted since these pulses are not required. See figure 5-5.

## +12 Volt Overvoltage Detector and Crowbar Circuit

The +12 volt overvoltage detector (figure 3-7) consists of operational amplifier Z203 plus two voltage dividers, one composed of R208, R209, R210 and one composed of R211, R212, R213. Also included is feedback resistor R238. The output of Z203 drives Q211, which, when conducting, produces the +12 volt overvoltage trip signal. Functionally, this circuit is similar to the +4.75 volt overvoltage detector, with the inverting input of $Z 203$ being fed by the +12 volt supply output, and the non-inverting input fed by the +12 volt return line. The inverting and non-inverting inputs are referenced by means of the voltage dividers to the auxiliary common and +10 volt reference voltage, respectively. As with the other detectors, an increase in potential between the inverting and non-inverting inputs drives the output of Z203 in a negative direction, causing Q211 to conduct when the output of the operational amplifier reaches approximately +11 volts.

The +12 volt crowbar circuit consists of an SCR (CR171) in series with a low value resistor (R144) connected directly across the +12 volt supply output. This main SCR is fired by a pilot SCR (CR169), which in turn is activated by the +12 volt overvoltage detector. The crowbar circuit itself serves only as a triggerable bleeder to discharge the supply filter capacitors. When the pilot SCR fires, a current pulse is generated through T134, firing the main SCR. In addition, the pilot SCR opens a direct path to the auxiliary common (by way of CR159) for the supply voltage from which the inverter driver stage operates, disabling the inverter. Firing the +12 volt crowbar circuit does not affect the other inverter channels.

## -12 Volt Overvoltage Detector and Crowbar Circuit

The -12 volt overvoltage detector (figure 3-8) consists of operational amplifier Z201, plus two voltage dividers, one composed of R201, R202, R203 and the other composed of R204, R205, R206, R207. Also included is feedback resistor R230. The output of Z201 drives Q210, which, when conducting, produces the -12 volt crowbar trip signal. This circuit functions in a manner similar to that of the +12 volt overvoltage detector, except that the inverting and non-inverting inputs of the operational amplifier are transposed because the supply output is negative. As in the other detectors, Q210 conducts when the operational amplifier output reaches approximately +11 volts.


Figure 3-7. +12 Volt Overvoltage Detector and Crowbar


Figure 3-8. -12 Volt Overvoltage Detector and Crowbar
The -12 volt crowbar circuit is identical to the +12 volt crowbar circuit, and functions in the same manner. It is composed of pilot SCR CR182, crowbar SCR CR184, and associated components. Refer to the +12 volt crowbar description for details.

## +4.75 Volt Undervoltage Detector

The +4.75 volt undervoltage detector circuit consists of operational amplifier Z208, plus two voltage dividers composed of R221, R222, R223 and of R224, R225, R226, R227. Operational amplifier Z208 shares these dividers with Z207. Also included are feedback resistors R258 and diode CR280 (figure 3-9). The +4.75 volt undervoltage detector is connected in reverse with respect to the +4.75 volt overvoltage detector; that is, the non-inverting input follows the +4.75 volt output and the inverting input follows the common return. The operational amplifier output is driven positive when the supply voltage increases. The output of this stage feeds the clear detector.

## -2.0 Volt Undervoltage Detector

The -2.0 volt undervoltage detector (figure 3-9) consists of operational amplifier Z206, feedback resistor R250, and diode CR279, plus two voltage dividers composed of R214, R215, R216 and R217, R218, R219, R220. Operational amplifier Z206 shares these dividers with Z205. As in the case of the 4.75 volt undervoltage detector, the inverting input follows the lower potential ( -2.0 volt) supply output, and the non-inverting input follows the higher (return) output. Thus, the operational amplifier output is driven positive when the supply voltage goes more negative. The output drives the clear detector by means of CR219.


Figure 3-9. +4.75 Volt and $-2,00$ Volt Undervoltage Detectors and Clear Detector

## Clear Detector

The clear detector (figure 3-9) is composed of Q214, Q215 and relay K201, with associated components CR219, CR220, CR221, CR276, R275, R274, R275, R276 and C216. Functionally, Z206 and Z207, by way of CR219 and CR220, form a discharge path for the base of Q214, holding it in conduction as long as the output voltage of either the +4.75 or -2.0 volt undervoltage detector is low. With transistor Q214 conducting, Q215 is cutoff. During this time, the K201 relay is inactivated. Diodes CR219 and CR220 form an AND gate, requiring that the discharge paths through both Z206 and Z208 be eliminated for Q214 to become cutoff. This action is accomplished by the outputs of Z206 and Z207 being driven positive, back-biasing diodes CR219 and CR220. Cutoff of Q214 causes Q215 to conduct, picking the relay and deactivating the CLEAR signal. An output of approximately +10 volts from the undervoltage detectors is required to back-bias CR219 or CR220. This represents a supply voltage of $90 \pm 5 \%$ of its nominal operating level.

## B 1700 Power Subsystem

The network composed of CR276, R273 and C216 provides a delay in activating the clear detector circuit. This network ensures that the CLEAR signal is generated, even though the undervoltage condition may only be momentary. Diode CR221 provides fast drop out of the relay once the energizing voltage is removed. This serves as further insurance of CLEAR signal generation on momentary undervoltage conditions.

## +10 Volt Reference Supply

The +10 volt reference supply (figure 3-10) is a secondary regulator operating from the +15 volt auxiliary supply. This reference supply is composed of operational amplifier Z209 and series regulator transistor Q209. A fixed reference is provided by CR217 to the non-inverting input of Z209. The supply output is fed back to the inverting input by means of a voltage divider composed of R264, R265, R266, and is adjustable by means of R265 (REF. VOLTAGE ADJUST). Functionally, an increase in voltage at the emitter of Q209 also raises the voltage at the inverting input of Z209. This drives the output of Z209 negative, reducing the conduction of Q209 and thereby causing a series voltage drop in the +10 volt supply line.


Figure 3-10. +10.0 Volt Reference Supply

## SEQUENCING CIRCUITRY

Power-up sequencing within the Logic Power Supply is provided by a hold-off circuit that disables the +4.75 and -2.0 volt inverters. In turn, the +12 and -12 volt inverters are controlled by the +4.75 volt output, and are allowed to begin operation when this voltage reaches its operating level. The hold-off circuit operates as a function of an RC time constant (approximately 50 milliseconds).

## +4.75/-2.00 Volt Hold-Off Circuit

The hold-off circuit consists of Q216, R280, R281 and C262 (refer to figure 3-11). Functionally, Q216 conducts as soon as output from the +15 volt auxiliary supply appears. This hold-off circuit applies a positive bias to the +4.75 and -2.0 volt inverter disable circuits by means of CR237 and CR249. In so doing, Q232 and Q241 are clamped on, preventing the inverter drivers from operating. Transistor Q216 conducts because its base is held at a low potential while C267 is charging. Capacitor C262 is charged from the +15 volt auxiliary supply at a rate determined by R280 and R281. When the charge on C262 reaches approximately +5 volts, the base-emitter junction of Q216 becomes back-biased, causing it to become cutoff. This action removes the bias to Q232 and Q241.


Figure 3-11. +4.75/-2.0 Volt Hold-Off Circuit

## 12-Volt Hold-Off Circuit

The 12 -volt hold-off circuit (figure 3-12) consists of Q252, R380, R386 and R387. This stage operates in an opposite manner to that of the $+4.75 /-2.0$ volt hold-off circuit. When the +15 volt auxiliary voltage comes up, a positive bias is applied to both 12 -volt inverter disable circuits by means of R380, CR261 and CR273. This bias clamps Q244 and Q258 on, preventing the 12 -volt inverters from operating. When the +4.75 volt output comes up to its operating level, Q252 conducts, shorting the bias voltage to ground. A 12 V ENABLE switch (S203) is provided to accomplish this function manually for test purposes.

## +12 VOLT INVERTER CHANNEL (EXAMPLE)

The following paragraphs describe a typical inverter channel. Since the mode of operation is the same for all channels, only the +12 volt supply is described in detail. The following discussion should be used for reference purposes whenever inverter operation is in question. Refer to the subsequent sections for specific details regarding the $+4.75,-2.0$, and -12 volt channels.

## +12 Volt Sense Amplifier

The +12 volt sense amplifier is a differential operational amplifier similar in function to the overvoltage and undervoltage detectors. Its operating level is governed by a reference voltage, and it is connected to produce an output voltage proportional to the dc potential across the corresponding inverter output. Using the +12 volt sense amplifier as an example, it may be seen that the +12 volt remote sense and +12 volt return remote sense lines are connected through isolating resistors R 388 , R389, R390 and R391 to the non-inverting and inverting inputs, respectively, of Z212. (Refer to figure 3-13). These lines, in turn, are connected to the +12 volt bus bar and +12 volt return bus bar at the backplane of the B 1700 processor. This connection is made to ensure that the voltage is correct at the point of use, and serves to compensate for voltage drops due to lead resistance. In addition to the remote sense leads, the direct supply output is connected to the sense amplifier by

## B 1700 Power Subsystem

means of R392 and R393, serving as a redundant sensing connection to prevent runaway in the event one of the remote sense leads is broken. A voltage reference for Z212 is provided by the network composed of R381, R382, and R383. This network operates from the main supply reference voltage provided by CR222. Potentiometer R382 ( +12 V VOLTAGE ADJUST) is used to set the operating level Z212, thereby controlling the inverter output voltage.


Figure 3-12. 12-Volt Hold-Off Circuit

Since the higher potential supply output feeds the non-inverting terminal, the operational amplifier output follows the level of this voltage. As with the overvoltage and undervoltage detectors, the return output may drive the operational amplifier as well, because a single-point system ground is utilized. The operational amplifier output driver, Q 251 , is the main component of the pulse width modulation regulation circuit. Under normal conditions, the operational amplifier output voltage is approximately -8 volts, and becomes less negative in response to an increase in supply output voltage.

## +12 Volt Current Limiter

Current limiting within the +12 volt inverter channel is provided by a circuit that senses current flowing in the inverter output stage. The signal derived is used to apply a secondary controlling influence to the disable pulse generator. (Primary control is exerted by the +12 volt sense amplifier.) The current limiter is a "fast attack" circuit which remains inactive at current levels below a pre-set amount. When the maximum allowable current level is reached, the limiter circuit produces sufficient output (actually a current drain) to override the disable pulse generator used to control the +12 volt sense amplifier. This action is accomplished by forcing the generation of longer disable pulses.


Functionally, the current-limiter circuit operates from a current transformer in the inverter output stage. In the +12 volt inverter, this transformer is T125. The output of T125 powers a bridge rectifier composed of CR256, CR257,CR258, and CR259. (See figure 3-14.) The output of this bridge is used to charge C234, and thereby set the bias on Q265. Transistor Q265 acts similar to a shunt regulator on the positive supply voltage (+AUX) for Q250. Under stable conditions Q256 conducts, holding the voltage at the junction of R433 and R439 at a low level. An increase in supply output current is reflected in increased output from the bridge, with a resultant higher charge on C234. This causes Q265 to become cutoff: as the current drain through Q265 decreases, the voltage supplied to the emitter of Q250 rises. The effective bias level of Q250 is changed, moving it toward the point where it conducts. When Q250 conducts, the average emitter voltage on Q251 increases, lowering the pulse generator triggering threshold (see figure 3-15). The current level at which conduction of Q250 occurs is determined by its preset bias, which is adjustable by means of R378 ( +12 V CURRENT).

An additional feature of the current limiter circuit is the section composed of Q262, R370 and R371, which provides a "part-time artificial load" for the current transformer. The design of this transformer requires that a low impedance be provided at the secondary when current is flowing in the primary. This reduction in impedance is accomplished by Q262, which, when conducting, presents a load of approximately 120 ohms (as set by R372) across the bridge output. Transistor Q262 conducts only for the duration of each current pulse from the bridge, since the absence of a (higher) charging voltage would allow C234 to discharge through it. CR248 prevents the voltage on C234 from holding Q262 on.

## +12 Volt Disable Circuit

The disable circuit is, in effect, a square-wave generator that incorporates pulse width modulation capabilities. Its output pulses are merged with the CLK and CLK/ steering pulses (which toggle the inverter), modifying them with respect to the ratio of on-to-off time. This modification provides a form of primary regulation, in that the power level at which the inverter is permitted to operate is adjusted to meet the load requirements.

B 1700 Power Subsystem


Figure 3-14. +12 Volt Current Limiter not control


Figure 3-15. +12 Volt Disable Circuit

## B 1700 Power Subsystem

The disable circuit functions through manipulation of a single comparator transistor. In the +12 volt channel, this transistor is Q251 (see figure 3-15). The state of the comparator, in turn, controls Q249, which, when conducting, causes Q248 to conduct. Conduction of Q248 applies a positive potential to the bases of Q245 and Q247 in the inverter driver stage, causing both to conduct. This same method, whether momentary (disable pulse) or continuous (hold-off), is used to control the operation of each inverter channel. In the latter case, an external bias is applied to the circuit by means of CR261.

Several factors have a bearing on the operating conditions of the comparator transistor and combine to determine the width of the disable pulse. In normal operation (load on supply output stable and within acceptable limits), Q251 is biased to conduct at a fixed current. This operating current is set by the output voltage of the +12 volt sense amplifier (Z212). This output is applied to the emitter of Q251 through R273.

## NOTE

The voltage on the emitter of Q251 can also be controlled by the output of the current limiter.

With Q251 conducting, the voltage at the base of Q249 is dropped to a low level, biasing it to cutoff. This steady-state condition is i terrupted by the ramp signal, which applies a steadily increasing voltage to Q251 through R375. During the ramp voltage excursion, Q251 serves as a current source, tending to minimize the voltage drop across R375, and at the same time continuing to hold the base of Q249 at a low potential. The ability of Q251 to perform this function is limited by the current available from Z212. This current varies in accordance with the output of Z212. When the voltage drop across R375 becomes less than the ramp voltage, the collector voltage of Q251 begins to rise. This causes Q249 to conduct, generating the disable pulse. The point at which conduction of Q249 occurs is known as the triggering threshold, and is dependent upon both the slope of the ramp and the emitter voltage of Q25 1.

The emitter voltage of Q251 (which is the output of the regulation circuitry) is the primary means of controlling the operation of the +12 volt inverter channel. The ramp voltage (and therefore the slope, since the frequency is fixed) is a function of the ac line voltage. This voltage is derived from the peak detector circuit in the output of the +4.75 volt inverter channel. Changes in the ramp voltage affect the operation of all four inverter channels.

## +12 Volt Inverter Driver

The inverter driver consists of two identical legs of transistor switches which control the flow of current in the primary winding of an interstage coupling transformer. The opposing legs are alternately toggled by the CLK and CLK/ signals, and, in so doing, drive the inverter output stage that follows.

In the +12 volt inverter channel, the inverter driver stage is composed of Q244, Q245, Q246, and Q247, plus associated components (see figure 3-16). Each leg consists of a Darlington-connected transistor pair, with protective diodes across the output.

In order to trigger the following inverter stage, the legs of the transistors are switched off rather than on. This triggering method involves the regeneration feature incorporated in the output stage, causing legs of the output stage (once triggered) to continue conducting (within limits) until cut off by external action. Therefore, to cause the output to be triggered, only a short trigger pulse is required, such as that created by the flux change in the interstage transformer primary when one of the driver legs is switched off.

Cutoff of the output stage occurs when the non-conducting driver leg is again activated. Conduction of both driver legs causes a very low impedance to appear across the interstage transformer primary, allowing it to "steal" power back from the secondary. This condition effectively quenches the regenerative base drive which caused sustained conduction in the output stage. Cutoff is accomplished by a disable pulse which returns the inactive driver leg to conduction; this event occurs before the appearance of the next clock pulse. As discussed in the +12 Volt Disable Circuit description, presented previously in this section, it is through control of this "off" period that supply regulation is accomplished. The system of using driver switchoff for output stage triggering offers better noise immunity than does conventional circuitry.

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B 1700 Power Subsystem


The functions of the diodes across each driver leg are as follows. The zener diodes (CR252 and CR254) serve to protect the switching transistors from inductive kicks produced by abrupt changes in current flow. The common diodes (CR253 and CR255) provide a reverse current path across each transistor in order to accomplish the quenching action described above. This action is required since the driver-switching transistors are polarized oppositely with respect to the transformer primary winding. This opposition of switching transistors prevents the driver stage from appearing as a complete dc circuit to the power reflected back from the transformer secondary.

## +12 Volt Inverter Output

The inverter output stage is composed of single-transistor left and right switching legs (used to control the current flow in the primary of the output transformer), a full-wave, center-tapped rectifier, and appropriate filtering. In the +12 volt inverter, these areas consist of transistors Q125 and Q126, output transformer T123, rectifiers CR166 and CR167, and associated components (refer to figure 3-17).

As mentioned previously, this stage incorporates regeneration; that is, once a switching leg has been turned on, it continues conducting (within limits) until disrupted by an external influence. The regeneration is accomplished by using the secondaries of the input transformer (T124) as autotransformers.

Since the turn-on pulse is generated by switching off the corresponding leg in the driver stage, it is of very short duration. Turn-off of the inverter leg occurs when the corresponding driver is switched back on by the disable pulse, as previously discussed. The disable pulse restores the driver to its resting condition; i.e., both legs are in conduction. This method applies an effective ac short across the primary of T124. This ac short is reflected to the secondary, where it effectively quenches the regenerative base drive to the conducting inverter leg.


Figure 3-17. +12 Volt Inverter Output Stage
The remaining details of the inverter circuit operation are straightforward. Note that the opposing legs both operate with a potential of 150 volts across the transistor, but these voltages differ with respect to each other. Transistor Q125 operates with +300 volts on the collector and +150 volts on the emitter, and Q126 operates between +150 volts and ground. This system is used since both voltages are necessary in the +4.75 volt inverter circuit. They are used in this manner in the remaining inverters merely to balance the load. The inverter circuit also incorporates noise suppression circuitry, composed of C132 and R136, C133 and R137, and R138 and C134. Components CR160, CR161, CR163, and CR164 provide transient protection for the transistors, while reverse transient protection is provided by CR162 and CR165. Transformer T125 is the current-sensing pickup for the current-limiter circuit. The rectifier system is a conventional full-wave, center-tapped type, with choke input. Resistor R180 serves as a bleeder circuit. The crowbar circuit was described previously in this section.

## FUNCTIONAL DETAIL OF INDIVIDUAL INVERTER CHANNELS

The following paragraphs outline the differences between the +12 volt channel (used in the +12 inverter channel example) and the remaining channels.

## +4.75 Volt Inverter Channel

The +4.75 volt channel operates in the same manner as the +12 volt channel in the +12 volt inverter channel example. The significant difference is the modifications that are needed to produce the higher current required.
+4.75 Volt Sense Amplifier
The +4.75 volt sense amplifier consists of operational amplifier Z 210 and associated components. Refer to figure 3-18. An increase in potential across the sensing terminals drives the output in a positive direction (less negative than its normal output of -8 volts). Note that the output passes through S202 (master/slave) to the disable circuit. Switch S202, when in the SLAVE position, replaces the output of Z210 with the output from the master supply.

## +4.75 Volt Current Limiter Circuit

The +4.75 volt current-limiter circuit consists of Q231, Q263, Q233, and associated components (see figure 3-19). This circuit differs from that described in the +12 volt inverter channel example only in the inclusion of R 310 from the base of Q263 to the collector of Q235. This resistor provides positive feedback, causing the current to be limited more sharply than in the lower current channels. There is no foldback of voltage.

## +4.75 Volt Disable Circuit

The +4.75 volt disable circuit consists of Q230, Q232, and Q234. (See figure 3-20.) The operation of this circuit is similar to that discussed in the +1.2 volt inverter example.

1726-2pwr. supplies


Figure 3-18. +4.75 Volt Sense Amplifier


Figure 3-19. +4.75 Volt Current Limiter


Figure 3-20. +4.75 Volt Disable Circuit

## +4.75 Volt Inverter Driver

The +4.75 volt inverter driver is similar to the +12 volt inverter example, except that the left and right legs each consist of two parallel-connected equivalent switching circuits. These circuits are composed of Darlington-coupled pairs Q222, Q223 and Q228, Q229 for the left leg, and Q224, Q225 and Q226, Q227 for the right leg (see figure 3-21). Note that although individual transient protection diodes (CR228, CR229, CR230, and CR231) are associated with each transistor pair, only one zener diode is required for both pairs. Two transistor pairs comprise the left and right switching legs. These zeners are CR226 and CR227, for the left and right legs, respectively. The parallel driver configuration is utilized to meet the increased drive requirements of the +4.75 volt channel.

## +4.75 Volt Inverter Output

This circuit differs significantly from that discussed in the +12 inverter channel example, in that it consists of four transistor switching legs connected in a parallel configuration, i.e., two sets of left and right legs which supply a common load. See figures 3-22 and 3-23. To meet the current requirements, each individual leg is made up of three transistors operating in parallel. In addition to these considerations, a +300 volt $/+150$ volt offset supply method is used to operate the paralleled switching legs. This method consists of connecting the corresponding left and right legs of the parallel channels in series for dc to force equal current flow. In so doing, circulating currents and other unwanted effects are avoided. The rectifier system is conventional, consisting of a full-wave center tap coupled to a choke input filter.


Figure 3-21. +4.75 Volt Inverter Driver


Figure 3-22. +4.75 Volt Inverter Output (Less Rectifiers and Filter)


Figure 3-23. +4.75 Volt Rectifier and Filter
Special transformer-type devices are used within the output stage to force positive turn-on and equalized current sharing of the switching transistors. Networks T105 through T108 contribute to both functions, and work in conjunction with transformer T111, which serves a dual purpose. Being a saturable reactor, T111 delays full current flow through the output circuit for a fraction of each half cycle. This delay (used for magnetizing T111) allows the equalizing networks, T105 through T108, to "condition" the active legs for full conduction. In addition, T111 supplies, by means of its secondary, sustaining feedback to the primaries of T103 and T104. This feedback is used to hold the active legs in conduction until the regenerative feedback (resulting from autotransformer action in the secondaries of T103 and T104) is built up.

## -2.0 Volt Inverter Channel

The -2.00 volt channel, like the 4.75 volt channel, is adapted for high-current output. Otherwise, its operation is similar to that discussed in the example.

## -2.0 Volt Sense Amplifier

The -2.0 volt sense amplifier consists of operational amplifier Z211 and associated components. See figure 3-24. This circuit functions in the same manner as the +4.75 volt sense amplifier. Note that the higher potential output $(+4.75$ volt $/-2.0$ volt return) is connected to the non-inverting input, and the lower potential output ( -2.0 volts) to the inverting input.


Figure 3-24. -2.00 Volt Sense Amplifier

## -2.0 Volt Current Limiter Circuit

The - 2.0 volt current limiter circuit is composed of Q240, Q264, Q242, and associated components. See figure 3-25. This circuit functions in the same manner as that discussed in the +12 example. Additional feedback is incorporated with resistor R392.

## -2.0 Volt Disable Circuit

The -2.0 volt disable circuit consists of Q239, Q241, and Q243. See figure 3-26. The functions of this circuit are the same as those described in the example.


Figure 3-25. -2.00 Volt Current Limiter


Figure 3-26. -2.00 Volt Disable Circuit

## -2.0 Volt Inverter Driver

The - 2.0 volt inverter driver consists of Q235, Q236, Q237, and Q238 plus associated components. See figure 3-27. The functions of this circuit are the same as that described in the example. Note that the output transistors are the same type as those used in the +4.75 volt inverter driver.


Figure 3-27. -2.00 Volt Inverter Driver

## -2.0 Volt Inverter Output

As in the +4.75 volt channel, this circuit utilizes multiple transistors in each leg (four each in this circuit). See figures 3-28 and 3-29. The circuit functions in the same manner as the +4.75 volt channel, and employs the same method for providing coordinated turn-on and additional base drive. The left and right legs are operated at the offset voltage levels. The left leg consists of Q117, Q118, Q119, and Q120, and operates between +300 and +150 volts. The right leg consists of Q121, Q122, Q123, and Q124, and operates between 150 volts and common.

## -12 Volt Inverter

The -12 volt inverter is basically the same as that described in the +12 volt inverter channel example. The differences include the type of transistors and output transformer used in the inverter output stages. In the following paragraphs, the significant differences in the -12 volt channel (from the +12 volt channel) are discussed.

## -12 Volt Sense Amplifier

The -12 volt sense amplifier consists of an operational amplifier, Z213, and associated components. See figure 3-30. The inputs to the sense amplifiers appear to be reversed (as in the -2.0 volt channel) in respect to the positive output channels. Functionally, the higher (absolute) potential output ( -12 volt return) is connected to the non-inverting input. The lower potential output ( -12 volts) is connected to the inverting input. These connections are the same for all channels.


B 1700 Power Subsystem


Figure 3-29. -2.00 Volt Rectifier and Filter


Figure 3-30. -12 Volt Sense Amplifier
-12 Volt Current Limiter

The -12 volt current limiter consists of Q259, Q266, Q260, and associated circuitry. See figure 3-31. This circuit operates the same as that described in the example.


Figure 3-31.-12 Volt Current Limiter
-12 Volt Disable Circuit
The -12 volt disable circuit consists of Q257, Q258, Q261, and associated circuitry. See figure 3-32. This circuit operates the same as that described in the example.


Figure 3-32. -12 Volt Disable Circuit

## -12 Volt Inverter Driver

The -12 volt inverter driver consists of Q253, Q254, Q255, Q256, and associated circuitry. See figure 3-33. This circuit operates the same as that described in the example.


Figure 3-33.-12 Volt Inverter Driver

## - 12 Volt Inverter Output

The -12 volt inverter output consists of Q127, Q128, and associated circuitry. See figure 3-34. The transistor types and output transformer differ from that in the +12 volt inverter channel example, since this supply has increased current output requirements. In addition, rectifier diodes are paralleled to handle this increased current requirement. The remainder of this circuit operates the same as that described in the example.

## LOGIC POWER SUPPLY -1, -3, AND -4

The following circuits within the logic power supply $-1,-3$, and -4 are described in this section:
a. Logic supply ac control.
b. $\quad+4.75$ volt and -2.0 volt output monitor.
c. Overvoltage detectors.
d. Undervoltage detectors.
e. $\quad+160$ volt supply and regulator.
f. Inverter and +4.75 volt regulator.
g. High current supply.
h. $\quad-2.0$ volt shunt regulator.


Figure 3-34. -12 Volt Inverter Output
i. $\pm 12$ volt supplies.
j. Control supply.

## LOGIC SUPPLY AC CONTROL

Figure $3-35$ contains a configuration diagram of the logic supply ac control. The 20 amp circuit breaker is normally in the ON position since the application of ac power is controlled external to the logic supply. Therefore, when power is applied to the input terminals it is allowed to pass, by the breaker and the RFI filter, to the internal circuits. Beyond the breaker the ac is unswitched except for the thermostat in series with transformer T1. This thermostat monitors the power diode heat sink temperature, opening when $120^{\circ} \mathrm{C}$ is exceeded. There is also a 2 amp fuse in series with the primary of T 1 , which serves to protect against excess current. When either the thermostat or fuse opens, power is removed from the control supply and +160 volt regulator. Without power the inverter SCR gate drivers cannot operate, and the supply output collapses. Note that since the thermostat is self resetting, it is possible for the supply to cycle on and off repeatedly under certain conditions (such as a blower failure).


Figure 3-35. Logic Supply AC Control
The main circuit breaker is constructed to trip from either excessive current flow by its series trip coil, or by external action by its auxiliary relay trip coil. The series trip coil is activated whenever the input current exceeds 20 amps . The auxiliary trip coil is activated when an overvoltage is detected on either the +4.75 volt or -2.0 volt supply output.

## +4.75 VOLT AND -2.0 VOLT OUTPUT MONITOR

Figure 3-36 contains the output monitor that consists of four operational amplifier detectors. Two of the detectors are connected to sense overvoltage conditions, one each for the +4.75 volt and -2.0 volt outputs. These detectors drive an AND gate network (connected to effectively OR the outputs), which in turn drives a crowbar trip circuit and a breaker trip circuit. The remaining two detectors sense undervoltage conditions on the same outputs. The undervoltage detector outputs are ANDed (only), then feed a 5 second delay circuit which is followed by a relay.

Since operation of the overvoltage and undervoltage detectors serve different purposes, they are discussed separately.

## Overvoltage Detectors

The overvoltage detectors are arranged to sense the supply output voltages (figure 3-37). Detector $\mathbf{A}$ in the illustration monitors the +4.75 volt supply output, having this voltage connected to its non-inverting input and a +6.54 volt reference voltage connected to its inverting input. Under normal conditions the opamp output is low (negative) resulting in a false level to the AND gate which follows it. When the +4.75 V supply voltage rises above the +6.54 volt reference voltage, the opamp output goes high, supplying a true level to the AND gate.

The -2.0 volt overvoltage detector (B) operates in a similar manner to that described previously, with the exception that the -2.0 volt supply output is connected to the opamp inverting input and a -2.45 volt reference voltage is connected to the non-inverting input. This arrangement produces a condition similar to that existing in the +4.75 volt circuit, with the output of the opamp being low. When the -2.0 volt supply output rises above (goes more negative than) the -2.45 volt reference voltage, the opamp output goes high, supplying a true level to the AND gate which follows it. The second inputs of both AND gates following the overvoltage detectors are always true (except when the NORMAL/SERVICE switch is in the SERVICE position).



## B 1700 Power Subsystem

Therefore a true output from either opamp produces a true at the AND gate outputs, which are tied together. The twin AND gates drive an additional AND gate pair, and these in turn drive a crowbar trip circuit, and a circuit breaker tripper.

When either the +4.75 volt or -2.0 volt overvoltage detector output goes high, the output of the AND gate which follows it is also driven high. This event results in the outputs of both secondary AND gates going high also, activating the trip circuits. Transistors Q3 and Q4 in the crowbar trip circuit both conduct when the AND gate outputs go high, applying +24 volts to the gate of the crowbar SCR across the supply output. Firing the crowbar shorts the output voltages. Transistors Q5 and Q6 in the breaker trip circuit also conduct when the AND gate outputs go high, energizing the auxiliary trip coil in the main breaker.

## Undervoltage Detectors

The undervoltage detectors (figure 3-38) are similar to the overvoltage detectors, differing only with respect to the reference voltages used. The +4.75 volt undervoltage detector (A) has the +4.75 volt supply output applied to its non-inverting input and a reference voltage of +3.84 volts to its inverting input. Therefore, under normal supply operating conditions the +4.75 volt undervoltage detector output is high.

The -2.0 volt undervoltage detector (B) is similar, having the -2.0 volt supply output applied to its inverting input and -1.60 volts to its non-inverting input. Should either supply output voltage drop below the corresponding reference voltage, the monitoring detector's output goes low. Each detector's output feeds one leg of an AND gate, with a true output from both required for a true out of the gate. Following the AND gate is a TAON delay line chip and another AND gate, with the latter driving a relay coil directly. The TAON-AND gate circuit is connected to provide a 5 second delay in energizing the relay coil whenever a true output is received from the preceding AND gate. Generation of the Clear signal (which goes to the processor) occurs whenever the relay is in the deenergized state. Therefore, when power is initially applied, the clear level remains true until both the +4.75 volt and -2.0 volt outputs have risen above the undervoltage reference levels; then the 5 second delay provided by the TAON has expired. Since picking the relay is a logical AND of the outputs of both undervoltage detectors, the effect of either output voltage dropping below its reference voltage is to force the clear level true. Clear remains true until the undervoltage condition has passed and the 5 second delay period thereafter has passed.

## +160 VOLT SUPPLY AND REGULATOR

The +160 volt supply serves to provide the internal dc operating power for the main inverter portion of the logic power supply. The +160 volt supply consists of a controlled bridge rectifier operating directly from the ac line, and a regulator circuit. These are discussed separately in the following subsections.

## +160 Volt Bridge Rectifier

The bridge rectifier (figure 3-39) consists of two SCR legs, two diode legs, and a commutating diode. The bridge operates (as does any other bridge rectifier) with one SCR leg and one diode leg conducting during each half cycle of the ac. For example, CR9 and A7 in figure 3-5 conduct simultaneously during one half of each ac cycle, with CR 10 and A12 conducting for the other half. Since the dc current path passes through both conducting legs, effective control can be maintained with the use of only one switchable device (an SCR) on each side of the bridge. In practice, this means is used to regulate the +160 volt output. The task is accomplished by varying the percentage of time (within each half cycle) that current is allowed to flow to the load.

The commutating diode (CR15) serves to provide a dc current path from the negative to the positive terminal of the rectifier when both SCRs are off. The current path is needed to allow the current produced by the collapsing field in filter choke L1 to discharge through the load. Triggering signals for the SCR rectifier legs are provided by the +160 volt regulator, and are coupled to the SCRs by way of a pulse transformer. The portions of the triggering circuit located within the +160 volt supply are a low pass filter (C18, C19, and R15) and a bleeder resistor (R12).



Figure 3-39. +160 Volt Supply

## +160 Volt Regulator

The +160 volt regulator (figure $3-40$ ) controls the operation of the +160 volt supply by controlling the application of firing pulses to the SCRs in the bridge rectifier. Incorporated in the +160 volt regulator are provisions for both regulation of the supply output voltage, and a "slow start" on initial power up. The latter feature is necessary to prevent overloading of the rectifier since the supply filter capacitors present an effective "dead short" when in the discharged state. The +160 volt regulator consists of a regulator bridge rectifier, a feedback control circuit, a slow start circuit, and a gate driver circuit. Each of these is explained in the following subsections.

## Regulator Bridge Rectifier

The regulator Bridge Rectifier provides the internal operating voltage for the +160 volt regulator circuit. The bridge is conventional in design, and operates from the secondary of an ac step-down transformer. The bridge output is unfiltered, pulsating dc of approximately 100 volts RMS. Half-wave ac pulses from the transformer secondary are used within the circuit to provide firing impulses for the SCR gate drivers.

## Feedback Control Circuit

The feedback control circuit provides the source of regulation control for the +160 volt supply. This control is implemented by varying the charging voltage available to the timing capacitor (C2) in the Slow Start Circuit. In function, the feedback control acts as a shunt regulator on the output of transistor Q 5 , and is the source of the timing capacitor charging voltage (Q5 is actually part of the Slow Start Circuit). The feedback control consists of transistors Q3 and Q4, diodes CR12, CR13, and CR15, and associated components.


## B 1700 Power Subsystem

In nperation, transistors Q3 and Q4 of the feedback control comprise a differential amplifier. When the output of the +160 wit supply is at its proper level, a constant current is drawn from the emitters of both transistors. If the +160 volt output ses, the base bias of transistor Q4 will also rise by an equal amount, due to the clamping action of zener diode CR15.
 capacitor (C2).
he circuit composed of 130 volt zener diode CR27, diode CR16, and the LED/phototransistor AT1 generate a control signal the +160 volt supply is greater than 130 volts.

## Slow Start Circuit

The basic function of the slow start circuit is to provide the charging potential for timing capacitor C 2 . The circuit is arranged to gradually increase this charging potential from zero to the normal operating level when power is first applied to the supply. Once normal operation is achieved, control of the charging potential is assumed by the feedback control circuit. Since the relationship of the slow start circuit and the feedback control circuit to the timing capacitor charging potential are that of source and drain respectively, both affect the absolute level of this voltage.
The operation of the slow start circuit is a time sequenced event dependent on the circuit constants involved. Transistor Q7 is momentarily turned on when voltage is first applied to the circuit. With Q7 conducting, the base of transistor Q6 is held t low potential, holding Q6 off. Q6 determines the amount of current flow through transistor Q5. Q5 is. therefore, also eld off when Q 7 is conductino. This initial condition allows no charging current to flow to capacitor C 2 . The base po ential of Q 7 rises above the cutoff point and Q 7 ceases to conduct when capacitor C 5 has charged. With Q 7 off, diode CR19 is reverse biased, allowing the base potential of Q6 to rise (due to the charging of capacitor C3). As C 3 charges, Q 6 conducts in proportionately greater amounts, and causes the conduction of Q 5 to increase. Greater conduction of Q5 allow more rapid charging of capacitor C2. The overall slow start rate is determined by the time constant set by resistors R16 and 19 in series with C3. The slow start circuit reaches the "full conduction of Q5" state approximately 2 seconds after the first application of power.

When input power is removed (even momentarily), capacitor C5 discharges immediately through R22, turning Q7 on again. Conduction of Q7 discharges C , returning the slow start circuit to the inactive state by a reversal of the process described above.

Gate Driver Circuit
The gate driver circuit generates the necessary firing pulses for the SCRs in the +160 volt bridge rectifier. Producing the fring pulses are a pair of unijunction transistors (UJT), each of which services one SCR. The UJTs themselves are caused o conduct alternately, in synchronization with the ac line current reversals, but subject to a variable delay factor. The delay is determined by the level to which timing capacitor C2 is charged, reflecting the combined effects of the feedback ontrol and slow start circuits.

In circuit terms the charge on capacitor C 2 serves as the emitter voltage for the UJTs. The base 2 of each UJT is supplied with the output of the regulator bridge rectifier (clamped to +20 volts by zener diode CR11) and the rectified positive half㲘 R7 (for Q2). Thefore the 2 foch UIT rest +20 volts, and rises to +27 volts for half of each (cycle. Since CR7 (for Q2). Therefore the base 2 of each UST rests at +20 volts, and rises to +27 volts for half of each

Because the base 2 voltages of the UJTs are unequal during each half ac cycle, the one with the lowest base 2 voltage (and therefore the lowest base 1 voltage as well) conducts first when the timing capacitor charges sufficiently. This conduction occurs when the emitter voltage (from C2) is more positive than the lowest base 1 voltage. Conduction of the UJT dis charges the timing capacitor through one half of pulse transformer T1. This current pulse is reflected in the secondary of , causing the corresponding SCR in the +160 volt bridge rectifier to fire. The UJT which has fired continues to conduct until its emitter volt

## NVERTER

The inverter converts the +160 volt dc internal operating voltage to a 320 volt peak-to-peak approximate square wave. This square wave is developed in the primary of a transformer, and rectified at the secondaries of same to produce the dc supply outputs ( +4.75 volts, -2.0 volts, +12 volts, and -12.0 volts). The inverter is of the bridge type using SCR switches, and, in basic form, approximates the circuit shown in figure $3-4$. In this circuit switching action is used to provide reversals of dc current through a transformer primary, simulating the application of ac. For example, current flows from the positive epl negative on the right. When switches 1 and 2 are opened 3 and 4 are closed. The current flows in the opposite di-
 rection through the primary, causing the difference in potential to be positive on the right and negative on the left. Repititions of this action produce an output waveform similar to that shown in figure 3-41(B).

## Basic SCR Inverter

The inverter used in the logic power supply is similar to the circuit shown in figure $3-41$, except that it incorporates an additional feature (a commutating circuit) necessary when using SCRs as switching devices. Since the basic characteristics of SCRs is to conduct in the forward direction (once triggered) until shut off by a reverse bias, an artificial means of generating a negative shut-off pulse is needed in an inverter. This requirement is satisfied by a "commutating circuit which stores a charge during each inverter pulse, and later uses this charge to generate the necessary shut-off pulse. The basic SCR inverter circuit (illustrated in figure 3-42) consists of power SCR's A1, A2, A3 and A4, commutating SCR's A5 and A 6 , and commutating circuit L 2 and $\mathrm{C} 1 / \mathrm{C} 2$. Note that the commutating circuit is connected in parallel with the load (primary of T2). Also included in the inverter circuit are "speedup" inductors (L5, L6, L7 and L8) across which the SCR shutoff pulses are developed. A series diode (CR23, CR24, CR25, and CR26) is provided with each speed-up inductor to avoid shorting the +160 volt supply line to the common.


OUTPUT WAVEFORM LAT SECONDAR
Figure 3-41. Bridge Inverter Operation

B 1700 Power Subsystem


## Figure 3-42. Basic SCR Inverte

The functions of the basic SCR inverter are as follows. Assuming that all SCR's are OFF initially, the circuit waits for triggering pulses from the gate drivers. For a given half inverter cycle, SCR's A1, A2, and A6 are fired simultaneously by entical 5 striggering pulses. Conduction of A1 and A2 allows current to flow through T2 in the direction shown in igure $3-43(\mathrm{~A})$, initiating the first inverter pulse. Simultaneously the conduction of A6 initiates operation of the commutating C circuit which begins to oscillate at its natural resonant frequency ( $36.2 \mathrm{msec} / \mathrm{cycle}$ ). Conduction of commutating diode 6 continues for less than one oscillation cycle, since the negative-going half sine wave reverse-biases A6, cutting it off At A6 continues for less than one oscillation cycle, since the negative-going half sine wave reverse-biases A6, cutting it off. At this time the capacitor elements of the commutating circuit are charged up to 160 volts and used to generate the shutoff
pulses for SCR's A1 and A2. SCR A5 is turned on at the appropriate time by a trigger pulse from the gate driver circuit, to provide the discharge path for this stored charge. Conduction of A5 allows the stored charge in $\mathrm{C} 1 / \mathrm{C} 2$ to flow throug the discharge path illustrated in figure 3-43. Approximately 20 volts are developed across "speedup" inductors L7 and L8, which is sufficient to reverse-bias SCR's A1 and A2

SCR A5 is turned off by the reverse-bias generated during discharge oscillation (positive-going half sine wave) of the commutating circuit. When A5 turns off, the commutating circuit stops oscillating, and the voltage across the primary of T2 returns to zero volts.

In the second half of the inverter cycle the same functions described above are repeated, except that current flow through the load (T2) is reversed. In this case SCR's A3, A4 and A5 are simultaneously triggered by the gate drivers. This action initiates the negative going inverter pulse and starts oscillation of the commutating circuit. A 5 is shut off by the negative going sine wave of the oscillation; A 6 is triggered by its gate driver; then the discharge of $\mathrm{C} 1 / \mathrm{C} 2$ shuts off A 3 and A 4 by developing 20 volts reverse bias across speed-up inductors L5 and L6. The cycle repeats when triggering signals are again applied to the gates of SCR's A1, A2 , and A6

## Improved SCR Inverter

The inverter circuit used in the Logic Power Supply is shown in figure 3-44. The "improved SCR inverter" differs from the "Basic SCR Inverter" example only by the addition of R-C suppression circuits (snubbers) which shunt the power SCR's

## Inverter Timing Circui

The inverter timing circuit, which provides regulation control for the +4.75 volt supply output, generates the gate drive pulses used to trigger the six SCR's in the inverter. The timing circuit consists of a comparator, voltage controlled oscillator (VCO), logic timing and gate driver sections as shown in figure 3-45. This circuit's overall manner of operation is to sense the level of the +4.75 volt supply output, and to generate a pulse train which is inversely proportional in frequency. The pulse train is used for triggering the gate drivers, which in turn fire the SCR's in the inverter. Incorporated in the logic timer section are delay line elements which are used to fix the interval between the power SCR firing pulses and those for he commutating circuit SCR's. This fixed delay determines the length of the inverter pulses. With fixed length pulses control of the inverter output may be affected by varying the frequency, and thereby the interval between pulses. In practice, both output voltage regulation and current limiting are accomplished through control of the VCO frequency. To further describe the operation of the inverter timing circuit, the various sections are discussed separately. Note that the comparator circuits in the Logic Power Supply-1 and -3 are different from those in the -4 version




Figure 3-45. Inverter Timing Circuit Block Diagram

## Comparator (Logic Power Supply-1 and -3)

The comparator is a differential operational amplifier which compares the +4.75 volt supply output to a reference voltage, and produces an error voltage used to control the VCO. Referring to figure 3-46, the reference voltage is provided by a voltage divider composed of $\mathrm{R} 4, \mathrm{R} 5, \mathrm{R} 6, \mathrm{R} 7, \mathrm{R} 8$ and R 9 , plus a 6.2 volt zener diode (CR1). The reference voltage is fixed at +4.85 volts, and is connected to the noninverting input of the operational amplifier. Since a B 1700 system design requirement specifies a common point, ground capability, local and remote ground sensing inputs are provided as part of the voltage divider string. The +4.75 volt supply output is applied to the opamp inverting input. For this purpose the +4.75 volts come from both local and remote sense points. (Local sensing is done at the supply output, whereas remote sensing comes from the distribution bus at the system backplane.)

Operationally, the opamp is set up to produce a nominal output of +5.0 volts when its inverting and noninverting inputs are equal. If the +4.75 volt supply output increases, it causes the opamp output to swing in a negative direction. The reverse occurs for a decrease in supply output, and the resulting error voltage is used to control the VCO stage which follows. Zener diode CR2 prevents the control voltage from rising above 6.8 volts.

## Comparator (Logic Power Supply-4)

The comparator in supplies equipped for master/slave operation is similar to its equivalent in the "stand alone" supply, but employs a different output circuit. (Refer to figure 3-47.)

In the master mode (S1 up) the comparator provides a control voltage to the VCO as previously described. The network consisting of R36, C14, CR21 and CR22 serves to prevent output voltage overshoot when the supply is turned on, and also in the event of transients. Zener diode CR4 prevents the comparator output from rising above approximately 7 volts, thus providing protection against excessive supply output voltage in the event that the regulator monitor circuits fail to act.

In the slave mode the VCO control voltage is provided by the slave control circuit, with the regular +4.75 volt comparator output disconnected ( $\mathrm{S}-1$ down). Excessive output voltage protection is provided by zener diode CR4 in this mode as well, with CR3 serving to isolate this function from the +4.75 volt comparator output.

## Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) consists of an operational amplifier similar to the one used as a comparator, but connected to operate as an oscillator. Following the opamp are an AND gate and a NOR gate, which form the oscillator output into square waves, and control the passage of the resulting signal to the logic timer circuit.

The net operation of the VCO circuit is to generate a square wave pulse train of a frequency determined by the output voltage of the comparator. This square wave signal has an approximate frequency of 10 kHz under stable supply output conditions, and varies at a rate of 2 kHz change for each 1 volt change in comparator output.


Figure 3-46. Comparator and VCO Circuits


Figure 3-47. +2.75V Comparator (Master/Slave Supplies)
Operation of the voltage controlled oscillator is dependent on the state of charge on feedback capacitor C12 in figure 3-46. Assuming an output of 5 volts or more from the comparator, the following occurs: sufficient current flows through the diode bridge to charge the feedback capacitor ( C 12 ) to a few hundred millivolts. This voltage causes the inverting input of the VCO opamp to rise above ground potential, which in turn drives the opamp output negative. With a negative opamp output, the output of the following AND gate is also low, driving the subsequent output of the NOR gate high. During the initial charge time of C12, diode CR6 in the diode bridge (consisting of CR5, CR6, CR7 and CR8) is reverse biased and diode CR8 is forward biased. When the AND gate output goes low, the bias conditions in the diode bridge are changed, causing CR6 to be forward biased (CR8 remains forward biased). With CR6 forward biased, the feedback capacitor discharges through diode CR7, continuing until the opamp inverting input potential drops below zero. The latter event drives the opamp output positive, resulting in the AND gate going high, and the NOR gate going low. This cycle repeats in the manner described above, with the rate of oscillation being determined by the speed at which C12 charges. The charging time (of C 12 ) is inversely proportional to the applied voltage from the comparator output. The comparator output is prevented from rising above 6.2 volts by zener diode CR2.

When the input to the comparator circuit is greater than +4.85 volts, the comparator output is driven in the negative direction. With a comparator output level approaching zero volts (or to -0.6 volts maximum swing), there is not sufficient potential available to charge the feedback capacitor (C12). In this condition the VCO opamp inverting input never rises above ground potential, and oscillation does not occur. With no oscillation there is no output signal, and firing of the inverter SCR's is prevented. When the supply output voltage drops (because the output power has been dissipated through the load), the comparator output swings positive again and operation resumes.

Logic Timer and Gate Driver Circuit
The logic timer and gate driver circuit serves to properly sequence the firing of the power and commutating SCR's in the inverter, effectively determining the inverter pulse length. The circuitry to perform this function consists of several flipflops, delay lines, and pulse shapers as shown in figure 3-48.

This circuit functions as follows. (Also see figures 3-49 and 3-50.)


Figure 3-48. Inverter Timing Circuit Block Diagram

## B 1700 Power Subsystem

a. Assuming that the " $J$ " innut to the $\mathrm{I}-\mathrm{K}$ flin-flop in figure $3-48$ is innitially high and the "K" input is low, the trailing edge of the next VCO output pulse causes the set output (B) of the flip-flop to go high and the reset output (C) to go low.
b. When the J-K flip-flop set output goes high, the $5 \mu \mathrm{~s}$ pulse shaper connected to it generates a $5 \mu \mathrm{~s}$ pulse. This pulse triggers gate drivers A1 and A2 directly, and gate driver A6 by way of AND gate 1. The gate drivers in turn fire the corresponding power and commutating SCR's in the inverter, initiating an inverter output pulse.
c. In addition to causing the J-K flip-flop to change state, the VCO output pulse is applied to a monostable multivibrator circuit. The multivibrator is programmed to provide an output which remains low for $40 \mu \mathrm{~s}$ after triggering (delay period), then goes high for $60 \mu \mathrm{~s}$. The multivibrator output feeds a $50 \mu \mathrm{~s}$ pulse shaper which serves to limit the pulse generated to that length.
d. The $40 \mu \mathrm{~s}$ delayed pulse from the shaper is ANDed with the Set and Reset outputs of the J-K flip-flop at gates 3 and 2 respectively. Since the flip-flop set output (B) is still high at this time, the delayed pulse is passed to gate driver A5. The driver triggers commutating SCR A5, discharging the commutating tank circut, and thereby terminating the inverter output pulse by reverse biasing the two conducting power SCR's.
e. The appearance of the delayed pulse at the output of AND gate 3 serves an additional function: to trigger the R-S flip-flop, causing it to change state. The R-S flip-flop outputs determine the conditions at the J and K inputs of the J-K flip-flop, with the net effect being to provide alternate triggering of the left and right halves of the inverter. In series with each output of the R-S flip-flop is a $10 \mu \mathrm{~s}$ delay circuit which serves to prevent both sides from changing state at once. (The side going from high to low does so instantaneously; the reciprocal change of the other side from low to high is delayed by $10 \mu \mathrm{~s}$.) This protective device prevents the opposite inverter legs from conducting at the same time.

In summary of the first five events (a. through e.), gate drivers A1, A2 and A6 each received a $5 \mu \mathrm{~s}$ triggering pulse immediately following the VCO output pulse. The gate drivers in turn fired power SCR's A1 and A2, plus commutating SCR A6 in the inverter. The firing of these SCR's initiated one inverter pulse and charged the commutating circuit. When the $40 \mu \mathrm{~s}$ delay provided by the monostable multivibrator had elapsed, this circuit generated a $50 \mu \mathrm{~s}$ output pulse which triggered gate driver A5 and reset the RS flip-flop. Gate driver A5 in turn fired commutating SCR A5, terminating the inverter output pulse. The R-S flip-flops change of state preset the gate driver circuit to fire the opposite half of the inverter at the next VCO pulse.
f. When the next (second) output pulse is received from the VCO, the J-K flip-flop changes state, with the set output going low and the reset output going high.
g. The J-K flip-flop reset output going low causes the $5 \mu \mathrm{~s}$ pulse shaper following it to generate a $5 \mu \mathrm{~s}$ pulse. This pulse triggers gate drivers A3 and A4 directly, and gate driver A5 by way of AND gate 4. These gate drivers in turn fire the power SCR's in the opposing half of the bridge inverter and initiate the commutator circuit charging cycle.
h. The VCO output pulse also triggers the monostable multivibrator. As in paragraph c., this circuit provides a $60 \mu \mathrm{~s}$ pulse which is delayed for $40 \mu \mathrm{~s}$ after triggering. The $60 \mu \mathrm{~s}$ pulse is limited to $50 \mu \mathrm{~s}$ by the following pulse shaper, and serves to trigger gate driver A6 by way of AND gate 2. (The reset output of the J-K flipflop is still high at this time).
i. Firing SCR A6 terminates the conduction of power SCR's A3 and A4 by commutating circuit action. In addition, the pulse appearing at the output of AND gate 2 resets the R-S flip-flop, preparing the circuit for the next cycle.

An interlock signal from the monostable multivibrator is used to control gating of the VCO output. This signal is the complement of the normal $40 \mu \mathrm{~s}$ delay output, and serves to prevent the entrance of a VCO pulse until the delay period has expired.

B 1700 Power Subsystem


Figure 3-49. Inverter Timing


## B 1700 Power Subsystem

## HIGH CURRENT SUPPLY

The high current supply produces both the +4.75 volt and -2.0 volt outputs. The supply (figure $3-51$ ) consists of a full wave center tapped rectifier, filters, a crowbar circuit for overvoltage protection, and a -2.0 volt shunt regulator circuit. In operation the high current rectifier is conventional, except that two output voltages are derived from it by use of the -2.0 volt shunt regulator. To provide the dual outputs, the negative or center tap output from the rectifier is used (directly) as the -2.0 volt output. The "ground" level between the +4.75 V and -2.0 V outputs is established artificially by providing a constant voltage drop between it and the negative reference.

In addition to diode rectifiers (CR21 and CR22), the high current supply employs two filter chokes (C9 and C10), and filter capacitors C24, C25, C26, and C29. Shunt resistor R29 is used for current sensing as part of the current limiting circuit. The crowbar SCR (A10) is fired by the +4.75 volt and -2.0 volt output monitor when an overvoltage occurs on either of these outputs. Firing the crowbar effectively shorts the high current rectifier positive and negative terminals together, "killing" the supply output. Supply operation can also be terminated by excessive heat sink temperature, this being detected by thermostat TH1. TH1 opens when the heat sink temperature reaches 120 degrees centigrade, removing the ac input to transformer T 1 (which supplies the +160 volt regulator and control supply).

## +4.75 Volt Current Limiter (Logic Power Supply-1 and -3)

The current limiter is a circuit similar to the comparator (which provides VCO control voltage in the inverter), and is in fact connected in parallel with the comparator at the input to the VCO diode bridge. In operation the limiter acts in opposition to the comparator, providing a drain on the VCO control voltage. This drain tends to reduce the frequency of VCO oscillation, and thereby the supply high current output. In practice the current limiter is adjusted to have little effect until a selected current level is exceeded (usually 200 amps ). At the maximum allowable current the limiter increases the control voltage drain, reducing the supply output. If the load continues to increase, the output current is held at a maximum allowable value by reduction of the output voltage.

The current limiter circuit consists of two cascaded operational amplifiers driving a network of switching transistors (as shown in figure 3-52). Inputs to the first opamp are the current sense lines ( + CS and -CS) from a shunt in the +4.75 volt output circuit. These sense lines go to the opamp noninverting and inverting inputs respectively. Under normal operating conditions ( 200 amp load) approximately 100 millivolts is developed across the shunt, with the +CS input slightly more positive. This condition causes the output of the first operational amplifier to be positive, resulting in a voltage of approximately +0.7 volts at the inverting input to the second opamp. The noninverting input to the second opamp is also set to approximately +0.7 volts, this being determined by voltage divider R25-R39. With nearly the same conditions as in the first opamp existing at its inputs, the second opamp output is also positive. Following the second opamp is transistor Q2, which controls the voltage at the base of drain transistor Q4. With the output of opamp 2 high, Q2 is turned OFF, thereby causing no drain on the output of current source transistor Q3.

Actual current limiting action occurs whenever the voltage across supply the output shunt rises above 100 mV . This event drives the output of the first opamp further positive, which in turn causes the second opamp output to swing negative. A negative output (actually a current drain) at the base of Q2 turns it ON, providing a current drain from current source transistor Q3. This condition causes the base of transistor Q4 to drop to ground potential, turning it ON and opening the current drain path from the VCO control input. The added drain causes the VCO timing capacitor to charge at a slower rate, and therefore reduces the frequency of oscillation. The operating point, or current level at which current limiting occurs, is adjustable by way of R15. Current limiting can be set to any level desired.

In addition to the "excessive current" situation, action of the current limiter circuit can also be initiated by the converter/ inverter interlock. This circuit is located in the +160 volt regulator, and serves to monitor the output of the +160 volt supply. Whenever the input voltage to the inverter drops below +130 volts, transistor Q1 in the current limiter is turned ON. This event causes the same actions as when the output of the second opamp swings negative. To control Q1, the level from the photo-coupled pair is high whenever the inverter supply voltage is above the +130 volt level. Q1 may be forced OFF by moving S1 to the OVERRIDE position.


Figure 3-51. High Current Supply


Figure 3-52. +4.75 Volt Current Limiter (Stand Alone Supply)

## B 1700 Power Subsystem

## +4.75 Volt Master/Slave Control Circuits (Logic Power Supply-4)

Supplies equipped for master/slave operation are provided with additional control circuits which permit paralleling their +4.75 volt and -2.0 volt outputs for increased current. To accomplish this method of operation, additional operational amplifier circuits are included to make the high current regulators in the "slave" supply track those in the "master". In the +4.75 volt regulator, the additional circuits consist of three comparators which provide an alternate source of control voltage for the VCO.

The overall scheme of master/slave operation is to allow the supply designated as "master" to operate normally, and to develop a control voltage proportional to the output of the master current for driving the regulator in the "slave". Changing a given supply from one mode to the other is accomplished by way of a single switch (S1).

The +4.75 volt slave control circuit functions as follows (refer to figure 3-53). Assuming that the slave mode has been selected ( S 1 down in figure 3-53), operational amplifier A senses the current flowing in the slave supply's own +4.75 volt output. For sensing purposes opamp A shares the primary current sensing shunt with the current limiter circuit.

NOTE

The current limiter is inactive in the slave mode.


Figure 3-53. +4.75 Volt Slave Control Circuit
Opamp A is connected so that an increase in (slave) supply output current drives its output in a negative direction. The output signal of opamp A feeds the noninverting input of opamp B. Concurrent with the above, the output current of the master supply is sensed by opamp $C$, the output of which drives the inverting input of opamp $B$. Master current sensing is accomplished by way of a secondary shunt in the +4.75 volt output circuit of that supply, and the signal derived therefrom is designated "master regulation" (M.R.) in the master supply and "slave control" (S.C.) in the slave.

## B 1700 Power Subsystem

As with opamp $A$, the output of opamp $C$ is negative-going with an increase in sensed current. The action of opamp $C$ tends to counterbalance the effect of $\mathbf{A}$ (as regards their effect on the output of opamp $\overline{\mathbf{B}}$ ). Ïn the slave mode, opamp $\overline{\mathbf{B}}$ drives the VCO directly, with a more positive output causing an increase in oscillation frequency and, therefore, greater +4.75 V supply output. Adjustment of the negative feedback from opamp A is by way of R26 ( +4.75 V BALANCE), and this means is used to set the output level of the slave supply (with respect to the master).

## +4.75V Current Limiter and Sequencing/Interlock Circuit (Logic Power Supply-4)

In the master/slave-capable logic supply the current limiter and sequencing/interlock circuits are separated, with the former being active only in the master mode. (The current limiter output is connected to the master side of S 1 , in parallel with the voltage comparator.) The current limiter functions in the same manner as described for the stand-alone logic supply, except that the transistor stages following the second opamp are omitted, and the opamp sinks the VCO diode bridge directly. Refer to figure 3-54. Note that the omitted stages are still present in the supply, but are part of the sequencing/interlock circuit.


Figure 3-54. +4.75 Volt Current Limiter (Master/Slave Supplies)
The sequencing/interlock circuit is connected to the VCO diode bridge full time, and serves the named functions as well as providing the supply with a "slow start" capability.

The circuit (figure 3-55) performs three distinct functions; each is described separately.
a. The interlock function serves to prevent VCO oscillation until the internal +160 volt supply output has risen to +130 volts minimum. This is accomplished through control of transistor Q7. In its quiescent state, the base of Q7 is a ground potential, causing Q7, and in turn Q5 and Q6, to conduct. The conduction of Q6 provides an artificial drain on the charging voltage applied to the VCO diode bridge, thus preventing oscillation. When the photo-coupled pair in the +160 volt regulator conducts, -15 volts is applied to the base of Q7, biasing it off. This condition in turn halts the conduction of Q5 and Q6, removing the artificial drain from the VCO diode bridge input. Note that the ON state (Q6 cutoff) can be forced by moving the NORMAL/OVERRIDE switch (S2) to the OVERRIDE position. This feature is used for troubleshooting.


Figure 3-55. Sequencing/Interlock Circuit (Master/Slave Supplies)
b. The slow-start function also prevents VCO oscillation for a predetermined time when the supply is cycled on. As with the interlock function, the slow start is provided by controlling the conduction of transistor Q6. In this case, the conduction of Q6 depends on the state of charge on capacitor C17. When power is first applied, Q6 conducts because its base is at ground potential. Once the interlock circuit is activated the drain provided by Q 5 is removed. At this time C17 begins to charge (by way of transistor Q3), increasing the base bias of Q6. When sufficient charge is reached, Q6 cuts off, allowing the VCO to begin operating.
c. The sequencing function permits control of logic supply operation by an external device. Sequencing is accomplished in the same manner as the slow start and interlock functions, but uses a separate means of control. To activate the supply by external means, a positive voltage is applied to the SEQ input. This voltage turns on transistor Q1, which in turn causes transistors Q2 and Q4 to conduct. Transistor Q4 duplicates the function of Q7, this being to turn on Q5, which turns off Q6. Note that the sequencing function is not used in present versions of the supply. (Q1 is omitted from the circuit.)

## -2.0 Volt Shunt Regulator (Logic Power Supply-1 and -3)

The -2.0 volt shunt regulator provides the -2.0 volt output from the logic supply, doing so by artificially creating a "ground" level which floats between the positive $(+4.75 \mathrm{~V})$ and negative $(-2.0 \mathrm{~V})$ terminals of the high current rectifier. The regulator's means of creating this level is to provide a constant voltage drop between the -2.0 V terminal and ground, so that the actual -2.0 V load current plus the current passed by the regulator is always equal to 200 amperes.

The -2.0 volt shunt regulator (figure 3-56) consists of an operational amplifier voltage sensing comparator which drives, through several stages of amplification, four paralleled high current shunt transistors. Also included is a second comparator which senses current flow through the shunt transistors, providing current limiting action within the regulator. In operation, opamp A in figure 3-56 senses the voltage on the -2.0 volt output, comparing it with the level established by zener diode CR1 and the setting of potentiometer R16. Under normal conditions (200 amp output) the voltage at the inverting input of opamp A (as determined by the -2.0 volt remote sense and -2.0 V local sense lines) is -1.98 volts. This voltage is compared to the reference established by the 6.2 volt zener CR1. The reference voltage is set by way of R16 to a level slightly more positive than -1.98 volts. With the reference (noninverting) input more positive, the output of opamp $A$ is positive, causing Darlington coupled transistors Q1 and Q2 to conduct. These in turn cause conduction of driver transistor Q2 (on the heat sink) and thereby power shunt transistors Q6, Q9, Q10 and Q11.

Current sensing for the regulator is provided by opamp B in figure 3-56. In the sensing circuit the current flowing through the four shunt transistors is summed and applied to the opamp inverting input. This level is compared with a reference voltage set by zener diode CR7 and R42, which is applied to the noninverting input. During normal operation the opamp inputs are approximately -1.73 volts and -1.44 volts respectively, resulting in a positive output from the opamp.

An increase in current flow through the shunt transistor emitter series resistors ( $\mathrm{R} 22, \mathrm{R} 24, \mathrm{R} 26$ and R 28 ) proportionately raises the "sum" voltage at the opamp inverting input. The voltage increase results in a corresponding reduction, or swing toward negative at the opamp output. When the output of opamp B does go negative, it forms a current drain from the base of Q1, reducing this transistor's drive to the shunt circuit, and thereby reducing the shunt current. Note that artificially reducing the shunt current in a shunt-regulated supply causes the output voltage to rise. In the -2.0 volt supply, current limiting results in an overvoltage condition. The excessive voltage is detected by the overvoltage monitor circuit, and deactivation of the entire logic supply results.

## -2.0 Volt Shunt Regulator and Master/Slave Control Circuits (Logic Power Supply-4)

As in the +4.75 volt circuit, slave control of the -2.0 volt output is accomplished by forcing the slave supply to track the master. To provide a tracking control signal a second "summing" opamp and buffer opamp ( C and D respectively in figure 3-57) are used in the master. The Master Regulation signal (pins 0 Q and 1 Y of P 5 ) is sent to the slave supply. In the slave this signal is known as Slave Control and is applied to opamp E by way of pins 0 R and 1 R of P 5 . Opamp E in turn drives Opamp F, which drives the shunt regulator circuit directly when S1 is in the SLAVE position.

Since the summing resistors are connected to the inverting input of opamp $C$, an increase in current through the shunt regulator transistors in the master supply causes the output of C to swing in a negative direction. This change is repeated by opamp D, which serves as a buffer, and also by E (in the slave supply), which amplifies the change. Opamp F (in the slave) serves as a comparator, with the negative-going Slave Control signal tending to drive the output of $\mathbf{F}$ positive, and the Balance level derived from its own summing opamp tending to drive its output negative. Since the output of opamp $F$ drives the slave shunt regulator directly, a servo loop is formed in which a tendency to increase conduction of the regulator is offset by a more negative output (Balance) from opamp C. The servo loop is operational in the slave supply only, since the setting of S1 prevents opamp $F$ from affecting regulation in the Master.

## $\pm 12$ VOLT SUPPLIES

The +12 volt and -12 volt supplies (which are identical) operate as conventional diode rectifier/series regulated circuits. The two supplies are unusual only in that their input power is taken from additional secondary windings in the main inverter transformer rather than the ac line. To produce both positive and negative 12 volt outputs, the positive output terminal of one supply and the negative output terminal of the other are grounded. (This is the only difference between the two supplies.) They are described as a single unit. The 12 volt supplies each employ a bridge rectifier, a series regulator with current limiting, a sequence control, over and under-voltage detection, and a crowbar type output protection circuit. The +12 volt supply is used as an example in the following description.



## Rectifier and Filter

Secondary windings of T2 provide the source power for both 12 volt supplies. The input to T2 is the 320 volt peak-to-peak square wave generated by the inverter. At the secondary the stepped-down approximate 5 kHz voltage is rectified by a diode bridge (CR11 in figure 3-58), and filtered by an L-C network (C3 and C14). This dc voltage can vary between +20 and +40 volts, depending on loading of the high current supplies. The output of the rectifier is fused ( 15 amps ), and is bridged by a crowbar SCR. The crowbar is a protective device which shorts the supply output whien activated.

## Voltage Regulator and Current Limiter

Supply regulation is provided by an integrated circuit regulator which drives two external series pass transistors (IC1, Q4 and Q5 respectively in figure 3-59). Action of the regulator is determined by the setting of R4 (VOLTAGE) and is applied by controlling the conduction of Q4 and Q5. Current limiting is provided by the action of transistor Q4, which when conducting causes a sharp decrease in the conduction of the pass transistors. Q4 senses the supply output current by way of shunt resistor R31, with the limiting point being set by R28 (CURRENT).

## Overvoltage Detector

An operational amplifier comparator is used to detect overvoltage conditions at the output of the supply. This circuit is followed by a one-shot pulse generator and driver circuit which fires the crowbar SCR whenever such a condition occurs.


Figure 3-58. 12 Volt Rectifier and Filter


Figure 3-59. 12 Volt Regulator and Current Limiter

## B 1700 Power Subsystem

The comparator (figure 3-60) is connected with the inverting input set to a reference voltage of +3.65 volts. This level is determined by voltage divider $\mathrm{R} 14 / \mathrm{R} 15$, which is connected to a +6.8 V voltage reference composed of $\mathrm{Q} 3, \mathrm{CR} 2, \mathrm{CR} 3, \mathrm{R} 16$, and R18. The comparator noninverting input bias is determined by the supply output voltage, and is set to approximately 3.0 volts by voltage divider R11/R12 during normal operation. With the inverting input at a higher potential, the comparator output is low and the crowbar trip circuit which follows is inactive.

When the supply output voltage rises to 14.6 volts or above, the noninverting input voltage exceeds the +3.65 volt reference at the inverting input, driving the comparator output positive. This event in turn activates the TAON one-shot monostable multivibrator, generating a single output pulse. The multivibrator output going true switches on transistors Q5 and Q6, the latter of which opens a discharge path for capacitor C15.

C15 discharges through the primary of pulse transformer T1, providing a pulse to the gate of the crowbar SCR. This pulse is of approximately $50 \mu$ s duration, and causes the SCR to fire, shorting the rectifier output. Firing the crowbar causes the supply to go into extreme current limiting. This event does not affect operation of the remainder of the logic supply.

## Undervoltage Detector

The undervoltage detector, like the overvoltage circuit, consists of an operational amplifier comparator followed by a one-shot multivibrator. The circuit serves to generate a pulse which indicates that supply output voltage has risen to an acceptable level.

## NOTE

## This capability is not utilized at present.

The undervoltage comparator is provided with a reference voltage of approximately +2.4 volts at the inverting input, this voltage being supplied by voltage source Q3 and the voltage divider composed of R23/R24 (refer to figure 3-60). In normal operation the comparator noninverting input has +3 volts applied (as determined by the supply output voltage, and voltage divider R29/R30), resulting in a positive output from the stage. This condition is significant only when power is first applied, since it is the opamp swing from negative to positive as the voltage comes up that triggers the following multivibrator stage. Upon receiving the positive input, the TAON generates a false output pulse, the duration of which is determined by external RC circuitry. When the pulse delay time has expired the TAON output goes true, and remains true as long as the supply is operating normally. Were it used, the TAON output pulse would be inverted, and applied as a clearing signal.

## CONTROL SUPPLY

The control supply is actually two supplies in one, and delivers a number of different output voltages. These voltages are used for reference levels and operating power by low level circuits throughout the logic supply. The two supply sections are both $A C$ line operated, and employ conventional series and shunt-regulation techniques. Also common to both sections is regulation control by way of integrated circuit regulator chips. The sections are known by the outputs they produce, being identified as the $\pm 15$ volt complementary Tracking Supply, and the $+24 \mathrm{~V},+4.5 \mathrm{~V}$ and -1.9 V supply. Each is discussed separately below.

## Positive and Negative Integrated Circuit Regulators

Regulation within the control supply is provided by integrated circuit (IC) regulators which incorporate many functions (usually performed by discrete circuitry) into one package. In each supply section, a single IC regulator is used to drive an external pass transistor which performs the active power dissipation function. Internally, each IC regulator consists of Control, Bias, DC Level Shift and Output Regulator sections. The basic functions of these four sections are as follows:
a. Control The control section provides start up and shut down functions. The start up function serves to establish an internal reference voltage. The shut down function is not used in either the positive or negative regulator, as this input is grounded in both circuits.
b. Bias The Bias section maintains the reference voltage initially established by the start up circuit. The positive regulator has a reference voltage of +3.5 V and the negative regulator a reference of -3.5 V .


Figure 3-60. 12 Volt Output Monitor

## B 1700 Power Subsystem

c. DC Level Shift
d. Output Regulator

The DC Level Shift circuit amplifies the reference voltage generated by the bias circuit to a level which can be used as the final or output reference voltage for the output regulator.

The Output Regulator provides the actual regulation action. This can be used directly at low current levels, or as drive for an external pass transistor where higher current levels are needed.

## NOTE

Circuit divisions within the positive and negative regulators are indicated by $\mathrm{A}, \mathrm{B}, \mathrm{C}$, and D in the $\pm 15 \mathrm{~V}$ supply illustration (figure 3-61).

## $\pm 15$ Volt Complementary Tracking Supply

The $\pm 15$ volt complementary tracking supply employs a single transformer/bridge rectifier. Dual (opposite) voltages are produced from the supply by using both the positive and negative terminals of the rectifier as active outputs. In this circuit the intermediate (ground) reference is supplied by the transformer center tap, and the positive and negative outputs are regulated separately. The regulators are tracking; this meaning that their output voltages are jointly controlled so as to cause the positive output voltage to follow fluctuations of the negative (although opposite in polarity). This means is used to ensure proper functioning of the numerous operational amplifiers elsewhere in the logic supply which use both voltages. In the tracking regulation system the negative regulator acts as master and the positive regulator as slave. Therefore, a fluctuation in the negative output is reflected at the positive output, but the reverse is not true. These two cases are illustrated in figure 3-62 (A) and 3-62 (B) respectively.

## Negative Voltage Regulator (-15V)

The negative regulator is configured to operate utilizing an internal reference, this being accomplished by applying the dc shift output (pin 9) of the IC to the voltage divider composed of R10, R11, and R15. The divider determines the level supplied to the dc shift sense input (pin 1) of the output regulator. A second input to the regulator is the output sense (pin 8 ), which is connected directly to the -15 volt output line. In operation, the two regulator inputs tend to counterbalance each other, maintaining a stable output. The level at the dc shift sense input is determined by the setting of potentiometer R11, which effectively controls the regulated voltage output. Regulation action results from changes in output level detected at pin 8 . When the output at pin 8 goes less negative, this causes increased conduction of transistor T6 inside the regulator chip. When T6 conducts more, this causes (indirectly) increased conduction of transistors T7 and T8, which in turn drive Q12 (external) to increased conduction, raising the supply output voltage. The reverse occurs when the output sensed at pin 8 goes more negative.

## Positive Voltage Regulator ( +15 V )

The positive regulator operates as a slave to the negative regulator, such that its actions represent a mirror image of events occurring in the latter circuit. This control is accomplished by tying the positive regulator's Output Reference input (pin 6) to ground, and driving its Output Sense input (pin 5) from a summing network connected to the outputs of both regulators. The dc Shift Output and dc Shift Sense Input of the positive regulator chip are not used.

The summing network consists of two equal value resistors (R27 and R28), the junction of which is at zero volts when the positive and negative supply output voltages are equal. When the +15 V output goes more positive or the -15 V output goes less negative, the summing point goes more positive also. This event causes transistor T 4 in the positive IC output regulator to conduct more. With T 4 conducting more, T 1 and T 2 in the positive output regulator conduct less, reducing the conduction of pass transistor Q13. When the summing point voltage goes negative (in response to a negative swing of either the +15 V or -15 V output) the reverse occurs. Since the summing point voltage effectively controls the positive regulator, the regulator responds both to variations in its own load, and the output voltage of the negative regulator. Because the summing point voltage has no effect on the negative regulator, the positive regulator must track the former's output but not vice versa.



Figure 3-61. +15 Volt Complementary Tracking Supply


NOTE: THE NEGATIVE SUPPLY OUTPUT IS CHANGING DUE TO VARIATIONS IN ITS LOAD. THESE OUTPUT FLUCTUATIONS ARE TRACKED BY THE POSITIVE SUPPLY (EQUAL BUT OPPOSITE POLARITY).


## NOTE: THE POSITIVE SUPPLY OUTPUT IS CHANGING DUE TO VARIATIONS IN ITS LOAD. THE NEGATIVE SUPPLY IS UNAFFECTED.

Figure 3-62. $\pm 15$ Volt Supply Tracking
$+24 \mathrm{~V},+4.5 \mathrm{~V}$ and -1.9 V SUPPLY
The three-output supply produces its outputs by a two-stage regulation process. This method involves the use of a bridge rectifier and preregulator which produce an internal working voltage of approximately +30 volts. Following the preregulation are three individual secondary regulators which drop the working voltage to the desired output levels.

## Bridge Rectifier and Preregulator

Input to the supply is by way of a secondary winding of transformer T1 (figure 3-63). The bridge rectifier (CR5) is a onepiece molded assembly, and is followed by filter capacitors C16 and C118. The supply working voltage output is maintained by a zener-referenced series regulator composed of CR20, Q1 and associated components.

T1


Figure 3-63. Bridge Rectifier and Pre-Regulator

## +24 Volt Supply

The +24 volt output is produced by an integrated circuit regulator with external series pass and current limiting transistors. These components are IC1, Q3 and Q1 respectively in figure 3-64. The regulator features an internal zener reference, and is controlled by the setting of potentiometer R2 in voltage divider string R1-R2-R3. The output current of the regulator is sensed by shunt resistor R13. When the current level exceeds 2 amperes, Q1 is turned ON, serving to drain base current from the pass transistor drive circuit inside the regulator chip. Regulator chip pin functions are the same as the +15 volt regulator in figure 3-61.

## +4.5 Volt Supply

This circuit is similar to the +24 volt regulator, except for component value changes. IC2, Q5 and Q3 (in figure 3-65) perform the regulating, series pass, and current limit functions respectively. Note that the input voltage to this regulator is reduced to +15.8 volts by series dropping resistor R19.

## -1.9 Volt Supply

The -1.9 volt output, like its +24 volt and +4.5 volt counterparts, is produced by an integrated circuit regulator and several external active devices. However, due to the low voltage involved, this circuit employs a system of shunt regulation similar to that of the -2.0 volt high-current output of the logic supply itself. This method involves utilizing the negative lead of the bridge rectifier as the output, and creating the ground level (to which the +24 V and +4.5 V outputs are referenced) by action of the shunt regulator. In the shunt function the regulator serves to maintain a constant voltage drop between the negative terminal and "ground".

Since the minimum regulated output voltage of the IC regulator is +2.5 volts, a special level-sensing circuit is necessary. This arrangement involves reversing several of the usual sensing connections, and operating the IC itself with an artificial reference (figure 3-66). Output voltage sensing is taken from the junction between R35 and R36 (which comprise a voltage divider), while the internal reference for the regulator is determined by the setting of potentiometer R 25 , which is a member of the voltage divider string made up of R23, R24, R25 and R26. Actual regulation is done by controlling the conduction of transistors Q5 and Q6, which are a Darlington coupled pair. Transistor Q4 serves to limit the IC regulator load current to about 15 milliamperes.


Figure 3-64. +24 Volt Supply

B 1700 Power Subsystem


Figure 3-65. +4.5V Supply


Figure 3-66. -1.9 Volt Supply

## MEMORY POWER SUPPLY CIRCUIT DETAIL

This subsection describes in detail the functioning of the following circuits within the memory power supply.
a. AC input.
b. $\quad-5$ volt supply.
c. +19 volt supply.
d. +4 volt supply.

Since the three supplies function in a similar manner, the +19 volt supply is used as an example. Following this, the difference between the other two supplies and the example are pointed out.

## NOTE

The circuits described are those of the current model supply. Those of earlier models are similar, but differ with respect to minor details.

## AC INPUT

The ac input section consists simply of the primary of transformer T1, plus a slow-blow fuse and a 2 ohm current limiting resistor. The application of ac power is controlled externally.

## +19 VOLT SUPPLY

The +19 volt supply operates from a full-wave, center-tapped rectifier composed of diodes CR1 and CR2 (figure 3-67). Capacitors C1 and C2 are dc filters and resistors R14 and R15 are bleeders. The junction of R14 and R15 is used to provide the supply voltage for the regulator chip in the -5 volt supply.

Regulation for the supply is controlled by an integrated circuit regulator (Fairchild $\mu \mathrm{A} 723$ ). The regulator serves to sense a difference between a reference voltage and the supply output voltage (as sensed at the memory backplane), and to provide an error voltage which controls the conduction of an external pass transistor. The IC Regulator consists of a voltage reference amplifier, an error amplifier and a current limiting transistor, the equivalent circuit of which is shown in figure 3-68.

In the regulator circuit the internal voltage reference output (pin 6 ) is connected to the error amplifier noninverting input (pin 5, by way of resistor R115), thus serving as a reference for the regulation action. The error amplifier inverting input (pin 4) is fed from the tap of potentiometer R117, which with R116 and R118 comprises a voltage divider for the sensed supply output. If the sensed voltage drops, the voltage at pin 4 will also drop, and since this is the inverting input, the error amplifier output voltage (at pin 10) will rise. An increased error amplifier output voltage causes the driver transistor (Q103) and the pass transistors (Q2 through Q13) to increase conduction, thus raising the supply output voltage. If the sense voltage were to increase, the output of the regulator chip would decrease, and the pass transistors would conduct less. Therefore, the regulation action maintains a constant voltage at the sense point, and the equilibrium level at which this condition is reached is determined by the setting of potentiometer R117 (VOLTAGE ADJ).

Current limiting is provided by an internal (to the regulator chip) current limit transistor. This transistor is connected (by way of pins 2 and 3) to sense the current flowing in the driver and pass transistor stages. If the current exceeds a certain value (determined by circuit constants), the resulting voltage drop causes the current limit transistor to conduct, draining the output of the error amplifier. The drop in output from the error amplifier in turn reduces conduction of the driver and pass transistors, reducing the supply output. The current level at which the limiting action occurs is determined by the setting of potentiometer R112. Since the limiting action directly affects the supply output voltage, the usual indication of this condition is a reduction in voltage, with the current remaining at the maximum allowable level. (A point of equilibrium is reached in the limiting condition just as in normal regulation.) Undervoltage detection is not provided, so a current limiting condition in the system environment would manifest itself as bad performance of the memory unit (parity errors).

Overvoltage protection is provided by transistor Q203, which serves as an independent sensor of supply output voltage. When Q203 conducts, the change in potential at its collector fires crowbar SCR CR204, shorting the output of the supply. The base bias of Q203 (and hence the overvoltage trip point) is determined by the setting of potentiometer R212.



Figure 3-68. IC Regulator Block Diagram (Showing Relationship to External Supply Sections)

## +4 VOLT SUPPLY

The +4 volt supply is basically similar to the +19 volt supply except for minor details . (Refer to figure 3-69.) Significant differences include the following:
a. The negative output terminal is connected to the positive terminal of the +19 volt supply, resulting in an effective supply output of +23 volts with respect to ground. (Nominal supply output is +4 volts.)
b. The variable input to the IC regulator error amplifier is referenced to the supply negative output. This connection causes the +23 volt supply to track the +19 volt supply.
c. Only one pass transistor is employed, due to the lower output current level.
d. An auxiliary half wave supply composed of CR102 and C102 is included to provide operating power for the IC regulator chip. The IC regulator in the +19 volt supply also operates from this source.
e. A thermistor (RT201) is included in the overvoltage protection circuit to balance the circuit, and keep the firing voltage for the SCR constant.


## -5 VOLT SUPPLY

The -5 volt supply (figure $3-70$ ) is nearly identical to the +4 volt supply, except for the following:
a. The supply positive output terminal is connected to the memory supply common. This allows the negative terminal to be used as a -5 volt output.
b. Dual pass transistors are employed.
c. No half-wave auxiliary supply exists in this circuit. Instead, the IC regulator chip derives its operating power from a voltage divider in the +19 volt supply.

## +20 VOLT PAPER TAPE POWER SUPPLY CIRCUIT DETAIL

This subsection describes in detail the functioning of the various circuits within the +20 volt supply. (Refer to figure 3-71.)

## AUXILIARY HALF WAVE RECTIFIER AND FILTER

The auxiliary half wave rectifier consists of rectifier CR1 and capacitors C16 and C1 (figure 3-71). This circuit provides an operating voltage of approximately 21 volts dc for the integrated circuit regulator (IC1).

## BRIDGE RECTIFIER AND FILTER

The bridge rectifier and filter consists of rectifiers CR2, CR3, CR4 and CR5, plus capacitor C6. This circuit provides an output voltage of approximately 30 volts dc, which after regulation becomes the output of the supply.

## INTEGRATED CIRCUIT REGULATOR

The integrated circuit regulator IC1 is a self-contained package which includes a preregulator, a voltage reference, a voltage comparator, a current comparator, an OR gate, and an amplifier. These circuits are related to one another as shown in figure 3-72.

Operating power for the IC regulator circuits comes from the auxiliary half wave rectifier, the output of which is fed through the internal preregulator before distribution. Operation of the main regulator circuit itself is determined by the inputs to its voltage and current comparators. Both comparators have inputs derived from internal and external sources. In the voltage comparator these are a reference voltage developed from the preregulator output, and a sense voltage from the output of the +20 volt supply itself. The current comparator similarly has a reference input from a constant current network (which operates from the preregulator output), and a sense input from a current sensing network in the +20 volt supply output circuit. Each comparator produces an error voltage output, and these are ORed together, then amplified to develop a regulation drive signal. The regulation drive signal is further amplified by two external driver stages, and then serves to control the conduction of a pass transistor which performs the actual regulation function.

In operation the supply voltage output level is determined by the setting of potentiometer R 8 (figure 3-71), which determines the level of the output sense voltage returned to the voltage comparator. An increase in the sensed output voltage level drives the voltage comparator output negative, causing a reduction in the regulation drive signal. A lower-level regulation drive signal in turn reduces conduction of Darlington-coupled driver transistors Q1 and Q3, and pass transistor Q2. Reducing the conduction of transistor Q2 increases its effective resistance and therefore the voltage drop across it, with the net effect being a reduction in supply output voltage.

The output current level at which current limiting action occurs is determined by the values of resistors R6, R9, R21, R22, and R23, and is not adjustable. The output current level is sensed as a voltage drop developed across resistor R22, and this voltage is used as one input to the current comparator. An increase in supply output current develops a greater voltage drop across R22, and this condition affects the regulator in a manner similar to that of an increase in sensed voltage output. When current limiting does occur, this is reflected by a drop in the supply output voltage, while the output current remains at the predetermined limit value.




Figure 3-72. Integrated Circuit Regulator Block Diagram

## SYSTEM AC CONTROL

This subsection describes in detail the functioning of the system ac control. The discussion applies equally to the B 1710 and B 1720 series central systems, which differ only in that the power input to the B 1720 is three phase, requiring a three pole contactor (the B 1710 is single phase and has a two pole contactor). Also, since the B 1720 has two ventilating fan assemblies, the airflow switches in both are connected in parallel so that either may activate the over temperature function. Otherwise, the ac controls in all B 1700 systems function identically.

## POWER SWITCHING CIRCUIT

The ac control (figure 3-73) operates in response to activation of the console ON/OFF switch, remotely carrying out the actions of the operator to turn the system power on or off. The ON/OFF switch is of the double-pole, double-throw latching type, which when pressed once, latches in the ON position. Switching the power on applies 24 volts ac from the secondary of transformer T1 to contactor K1 and the console ON lamp. The lamp and contactor circuit is completed by way of normally closed contacts (terminals 1 and 7) in relay K2. Note that unswitched ac is applied to the primary of transformer T1 at all times. Picking contactor K1 applies ac power to the central systems user devices, and also completes the circuit from an additional winding of transformer T 1 . This winding supplies an ac voltage to the real time clock circuit.

Switching the ON/OFF switech on also applies 24 volts ac to the heater of time delay relay K3, the contacts of which are normally open. The heater circuit of the relay is returned to the 24 volt common by way of the airflow switch(es) in the system fan assembly. The airflow switch is of the normally closed type, and opens when airflow is present. Therefore, as long as airflow continues. the time delay relay circuit is not completed, and its contacts remain open.

## OVERTEMPERATURE PROTECTMON CIRCUIT

When the airflow ceases or drops sufficiently to close the airflow switch, the heater of time delay relay K 3 is energized. If the condition continues for the delay period (about 30 seconds), the contacts of K3 close. The closing of K3 applies 24 volts ac to the coil of latching rekay K2, picking it and illuminating the TEMP lamp. Picking K2 also breaks the 24 volt suply the to contactor K1, causing it toudrop out and thus remove power from the system. The ON lamp is also extinguist ad at it: time. The latching action $O$ ? is provided by a set of normally open contacts which connect the relay coil directly to the 24 volt ac line (from the $F$ sitch) when it is picked. Therefore, when latched. K2 is independent of the time delay relay, and can only be reset by towning the ON/OFF switch off. Note that when in the off pusition, section B of the ON OfF switch applies 24 volts ac to the OFFlamp.


## SECTION 4

## ADJUSTMENTS

## GENERAL

This section contains those procedures required to place fully functioning logic power supplies, memory power supplies, and +20 volt paper tape power supplies into operation within a B 1700 system. No adjustments are necessary for the System ac Control.

## LOGIC POWER SUPPLY ADJUSTMENTS

Separate adjustment procedures are provided for power supplies $-1,-2,-3$, and -4 . Determine the type of supply to be adjusted before beginning and follow the applicable procedure.

The following instructions pertain to supplies that have been installed in the system. If the installation has not been performed, refer to Section 6.

Included in the following are instructions for both single (stand alone) and parallel (Master/Slave) logic supply adjustments. Note that where parallel operation is involved, both logic supplies must be calibrated individually. as described in the Single Supply Adjustments, before the Parallel Adjustments are performed. Both procedures (for both logic supply designs) are described in this section.

## TEST EQUIPMENT

The following equipment is required to perform the adjustment procedure:
a. Digital Voltmeter (DVM) - Burroughs Model 3300, or equivalent (one required).
b. B 1700 Logic Power Supply Dummy Load, part number 22070999 (one required).
c. Tektronix model 453A Oscilloscope with equal length 10:1 probes or equivalent (one required; needed for Logic Power Supply-1, -3 and -4 calibration only).

## SINGLE SUPPLY ADJUSTMENTS (Logic Power Supply-2)

Use the following procedure to calibrate individual Logic Power Supplies. In systems employing more than one supply, perform the adjustments separately for each.


## Preparations for Calibration

To perform the calibration, first disconnect the supply from the data processing system. This includes disconnecting connectors J12A, J12B, JLG and the high-current terminals. Do not remove the ac power cable.

## B 1700 Power Subsystem

## CAUTION

Make sure the system power is off before disturbing any connections.

When the supply has been disconnected, perform the following steps in order:
a. Extend the supply from the system and remove the top and bottom covers.
b. Remove the regulator board from the supply and mount on the left-hand processor frame rail, using the regulator board mounting bracket located on the rail. The regulator board is installed in the compartment at the rear of the supply, and is equipped with extension cables. The component side of the board should face the power supply. Refer to figure 4-1.
c. Preset the potentiometers as indicated in table 4-1. All are located on the regulator board. Refer to figure 4-2.
d. Verify that the switches shown in table 4-2 are in the indicated position.
e. Check the fanning strip located on the fan side of the main power board. This strip should be connected in the RUN position. The fanning strip is in the RUN position when its lugs are connected to terminals 1 through 9 of the associated terminal strip. Refer to figure 4-3.


Figure 4-1. Supply in Test Configuration


Figure 4-2. Regulator Board Control and Test Point Locations

Table 4-1. Control Preset Conditions

| Control Name | Designation/Value | Setting |
| :---: | :---: | :--- |
| +4.75 V VOLTAGE | R321 (5K) | FCCW (Fully counterclockwise) |
| +4.75 V CURRENT | R317 (5K) | FCCW (Fully counterclockwise) |
| -2.0 V VOLTAGE | R353 (5K) | FCCW (Fully counterclockwise) |
| -2.0 V CURRENT | R350 (5K) | FCCW (Fully counterclockwise) |
| +12.0 V VOLTAGE | R382 (5K) | FCCW (Fully counterclockwise) |
| +12.0 V CURRENT | R378 (5K) | FCCW (Fully counterclockwise) |
| -12.0 V VOLTAGE | R413 (5K) | FCCW (Fully counterclockwise) |
| -12.0 V CURRENT | R410 (5K) | FCCW (Fully counterclockwise) |
| -4.75 V BALANCE | R312 (25K) | Mid-range |
| -2.0 V BALANCE | R344 (25K) | Mid-range |

Table 4-2. Switch Preset Conditions

| Switch Name | Designation | Location | Position |
| :---: | :---: | :---: | :---: |
| O. V. DISABLE/RUN | S201 | Regulator Board <br> (top left) | DISABLE <br> (away from <br> board) |
| MASTER/SLAVE | S202 | S203 ENABLE/RUN | S105 |
| TEST/OPERATE |  | Regulator Board <br> (top center) <br> Regulator board <br> (top right) <br> (away from <br> board) | RUN <br> (toward <br> board) |
| Main power board |  |  |  |
| (fan side, center) | OPERATE <br> (away from <br> heat sink) |  |  |



Figure 4-3. Power Board Controls

## Detailed Alignment

The following procedures are separated into sections which basically follow the main divisions of circuitry within the supply. Each procedure should be performed in the order listed.

## Auxiliary Supply Adjustment

This adjustment sets the regulation circuit operating voltage to the proper value.
a. Connect the dummy load between the +4.75 volt output stud and the GND stud.

b. Connect the DVM from the +4.75 volt stud to the GND stud.
c. Turn the supply breaker ON.

## NOTE

System power must also be ON.
d. Adjust the +4.75 V CURRENT control (R317) to mid-range.
e. Adjust the +4.75 V VOLTAGE control $(\mathrm{R} 321)$ for a reading of $4.00 \pm 0.1$ volts on the DVM.
f. Connect the DVM between J203 (+) and the common on the regulator board.
g. Adjust the + AUX ADJUST control (R108) for a DVM reading of $+15 \pm 0.1$ volts.

## NOTE

R108 is located on the power board.
h. Move the positive DVM lead from J203 ( + ) to $\mathbf{J} 203(-)$ and verify that the voltage at this point is $-15 \pm 0.75$ volts. (There is no adjustment.)
i. Turn the supply breaker OFF.

## + 10 Volt Reference Voltage Adjustment

This adjustment sets the OV/UV detector reference voltage to its proper value.

1. a. Connect the DVM from TP1 ( + ) to common ( - ) on the regulator board.
2. b. Turn the supply breaker ON .
3. c. Adjust the O.V./U.V. REFERENCE control (R265) for a reading of $10.0 \mathrm{~V} \pm 0.01$ volts on the DVM.
4. d. Move the (+) DVM lead from TP1 to the wiper of R226(+4.75V O.V. ADJUST).

5. e. Adjust R226 for a reading of $3.06 \pm 0.01$ volts on the DVM.
6. f. Turn the supply breaker OFF and disconnect the DVM.

## Output Voltage Adjustment

This adjustment presets the supply output voltages to their approximate working levels.
H. a. Turn the supply breaker ON.

万. b. Perform the adjustments listed in table 4-3.

Table 4-3. Output Voltage Adjustments

| DVM Connection | Control | Adjust To |
| :---: | :---: | :---: |
| $\begin{aligned} & +4.75 \text { V Stud }(+) \text { to Ground }(-) \\ & -2.0 \text { V Stud }(-) \text { to Ground }(+) \\ & -2.0 \text { V Stud }(-) \text { to Ground }(+) \\ & \text { J12A-A }(+) \text { to J12A-B }(-) \\ & \text { J12A-A }(+) \text { to J12A-B }(-) \\ & \text { J12B-A }(+) \text { to J12B-B }(+) \\ & \text { J12B-A }(+) \text { to J12B-B }(+) \end{aligned}$ | $\begin{aligned} & +4.75 \text { V VOLTAGE (R321) } \\ & -2.0 \text { V CURRENT (R350) } \\ & -2.0 \text { V VOLTAGE (R353) } \\ & +12.00 \text { V CURRENT (R378) } \\ & +12.00 \text { V VOLTAGE (R382) } \\ & +12.00 \text { V CURRENT (R410) } \\ & \text { - 12.00 V VOLTAGE (R413) } \end{aligned}$ | $4.85 \mathrm{~V} \pm 0.01 \mathrm{Vdc}$ <br> Mid-range $\begin{aligned} & -2.08 \mathrm{~V} \pm 0.01 \mathrm{Vdc} * \\ & \text { Mid-range } \\ & +12.00 \mathrm{~V} \pm 0.01 \mathrm{Vdc} \end{aligned}$ <br> Mid-range $-12.00 \mathrm{~V} \pm 0.01 \mathrm{Vdc}$ |

* Adjust to $-2.05+0.01 \mathrm{Vdc}$ in B 1720-series systems


## Overvoltage Trip Point Check and Adjustment

This procedure calibrates the $\pm 4.75$ and -2.0 volt crowbar firing circuitry.
a. Ensure that the O.V. DISABLE/RUN switch (S201) is in the RUN position (toward the board).
b. Connect the DVM between the +4.75 volt stud and the ground (GND) stud.
c. Turn the supply breaker ON .
d. Slowly adjust the +4.75 V VOLTAGE control (R321) clockwise until the supply circuit breaker trips OFF. Note the voltage at which the breaker trips. This voltage should be between +5.60 and +5.80 volts. Reduce the control setting and reapply power to the supply, if necessary, to repeat the test for an accurate measurement. The overvoltage protective circuit has about a 1 -second time delay. Therefore, the +4.75 V VOLTAGE control should be adjusted yery slowly when making this test.
e. If the trip voltage is out of tolerance, readjust the + 4.75 V OVERVOLTAGE ADJUST control (R226) and repeat the test. Continue the test until a reading is obtained that is within tolerance.
f. Reset the +4.75 V VOLTAGE control (R321) to $+4.85 \pm 0.01$ volts.
g. Use table $4-4$ to verify the trip points for other voltages. There is no adjustment for these readings. If the voltages are out of tolerance, repairs must be made.

NOTE
The -2.0 volt output must be reset to its nominal operating level before testing the $\pm 12$ volt outputs. It is necessary to cycle the main circuit breaker OFF/ON to reset the 12 volt crowbars.

Table 4-4. Overvoltage Crowbar Trip Points

| DVM Connection | Control/Location | DVM Indicated Trip Point |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { - 2.0 V Stud (-) to GND } \\ & \text { Stud }(+) \end{aligned}$ | - 2.0 V VOLTAGE (R353) | $-2.30 \text { to }-2.50 \mathrm{Vdc}$ <br> (Circuit breaker trips) |
| J12A-A (+) to J12A-B (-) | + 12 V VOLTAGE (R382) | $+12.5 \text { to }+14.40 \mathrm{Vdc}$ <br> (Voltage collapses) |
| J12B-A (+) to J12B-B (-) | - 12 V VOLTAGE (R413) | $\begin{aligned} & -12.5 \text { to }-14.40 \mathrm{Vdc} \\ & \text { (Voltage collapses) } \end{aligned}$ |

## NOTE

The +10 volt reference supply can be adjusted slightly to bring a marginal overvoltage trip level into specifications. Refer to the +10 Volt Reference Voltage Adjustment in this section.
h. Reset all voltages as indicated in table 4-3.

## Balance Adjustment and Current Limit Check (+ 4.75 and - 2.00 Volt)

This procedure performs operational testing and provides adjustments for the +4.75 and -2.00 volt current limit circuits.
a. Turn the supply breaker OFF and connect the dummy load from the +4.75 volt stud to the -2.00 volt stud.
b. Connect the DVM from the +4.75 volt stud $(+)$ to the GND stud ( - ).
c. Turn the supply breaker ON.
d. Turn the +4.75 V CURRENT control (R317) fully clockwise. The DVM should indicate $+4.85 \pm 0.01$ volts. If not, readjust the +4.75 V VOLTAGE control (R321).
e. Turn the supply breaker OFF.
f. Connect the DVM to TP15 (+) and common (-) on the regulator board.
g. Turn the supply breaker ON.
h. Adjust the +4.75 V BALANCE control (R312) until the DVM indicates $-7.30 \pm 0.1$ volts.
i. Move the DVM leads to the +4.75 volt stud ( + ) and GND stud ( - ).
j. Turn the +4.75 V CURRENT control (R317) counterclockwise slowly. The DVM indication should decrease smoothly, though quickly, to zero or near zero. This should occur during approximately the last 90 degrees of the rotation of R317.
k. Turn the +4.75 V CURRENT control (R317) clockwise until the DVM again indicates $+4.85 \pm 0.01$ volts.

1. Move the (+) DVM lead to the -2.00 volt stud. (The negative lead should remain connected to the GND stud.)
m. Turn the -2.00 V CURRENT control (R350) fully clockwise. The DVM should indicate $-2.0 \pm 0.01$ volts. If not, readjust the -2.00 V VOLTAGE control (R353).
n. Turn the supply breaker OFF.
o. Connect the DVM to TP25 (+) and common (-) on the regulator board.
p. Turn the supply breaker ON.
q. Adjust the -2.00 V BALANCE control (R344) tantil the DVM indicates $-6.90 \pm 0.01$ volts.
r. Move the DVM leads to the GND stud (+) and -2.00 volt stud ( - ).
s. Turn the - 2.00 V CURRENT control (R350) Slowly counterclockwise. The DVM indication should decrease, smoothly, though quickly, to zero or near zero. This should occur during approximately the last 45 degrees of the rotation of R350.
t. Turn the -2.00 V CURRENT control (R350) clockwise again until the DVM indicates $-2.0^{\boxed{6}} \pm 0.01$ volts. This should occur during the last 45 degrees of the rotation of R350, but at the opposite end.
u. Turn the supply breaker OFF.
v. Disconnect the dummy load. Do not replace the high-current terminal hardware at this time.
w. Re-install the regulator board in the rear compartment of the power supply. Make sure the fiber insulating card is mounted on the standoffs between the board and chassis.
x. Replace the top and bottom supply covers.

## Adjustments Under System Load (Single Logic Supply)

The following procedure is the final step in installing a Logic Power Supply and applies only to systems employing a single Logic Power Supply. Refer to the heading entitled PARALLEL SUPPLY ADJUSTMENTS (in this section) when working on systems employing multiple supplies.

## Preparatory Steps

This procedure connects the supply to the system load.
a. Place a $3 / 8^{\prime \prime}$ plain washer on the GND terminal; then slide the supply into the B 1700 cabinet and secure with the front panel screws.
b. Connect the bus bars to the +4.75 volt, GND, and -2.0 volt terminals. Use a $1 / 2-20$ nut, a $1 / 2 "$ plain washer and a $1 / 2^{\prime \prime}$ lock washer for the +4.75 volt and -2.0 volt terminals. Use a $3 / 8-24$ nut, a $3 / 8^{\prime \prime}$ lock washer, and a $3 / 8^{\prime \prime}$ plain washer for the GND terminal.
c. Connect the cables which mate with JLG, J12A, and J12B.

## +4.75 and - 2.0 Volt Backplane Adjustments

This procedure sets the +4.75 and -2.0 voltages to their final operating levels. Refer to figure $4-4$ in conjunction with the following steps.
a. Turn the supply breaker ON , then turn the system ON .
b. Connect the DVM to the +4.75 volt bus $(+)$ and GND bus $(-)$ at the right side of the processor backplane. This is the most distant point from the Logic Power Supply.
c. Adjust the -4.75 V VOLTAGE control until a reading of $+4.85 \pm 0.01$ volts is obtained. Access to this and the other controls may be gained through the marked chassis holes. Use a non-metallic adjusting tool.
d. Adjust the +4.75 V CURRENT control counterclockwise until the +4.75 volt supply begins to current limit ( +4.85 volt reading begins to decrease), then turn the control back $d_{f}$ division clockwise. The divisions are marked on the chassis around the access hole.

## B 1700 Power Subsystem

e. Move the DVM (+) lead to the -2.0 volt bus at the right side of the processor backplane. The (-) lead should remain connected to the GND bus.
f. Adjust the -2.00 V VOLTAGE control until a reading of $-2.08 \pm 0.01$ volts is obtained.
g. Adjust the -2.00 V CURRENT control counterclockwise until the -2.00 volt supply begins to current limit ( -2.00 volts reading decreases). Turn the control of division clockwise.


Figure 4-4. B 1712/B 1714 Backplane Voltage Sense Points

## + 12.0 Volt Backplane Adjustment

This procedure sets the +12 voltage to its final operating level.
a. Connect the DVM from the bottom of the +12 volt bus $(+)$ to the GND bus ( - ). The +12 volt bus is the one farthest from the backplane. Refer to figure 4-4.
b. Adjust the +12 V VOLTAGE control until a reading of $+12.00 \pm 0.1$ volts is obtained.
c. Adjust the +12 V CURRENT control counterclockwise until the +12.00 volt supply begins to current limit $(+12.00$ volts reading begins to decrease). Turn the control de division clockwise.

## - 12.0 Volt Backplane Adjustment

This procedure sets the -12 voltage to its final operating level.
a. Connect the DVM from the bottom of the -12 volt bus $(+)$ to the GND bus $(-)$. The -12 volt bus is the one nearest the backplane. Refer to figure 4-4.
b. Adjust the -12 V VOLTAGE control until a reading of $-12.00 \pm 0.1$ volts is obtained.
c. Adjust the -12 V CURRENT control counterclockwise until the -12.00 volt supply begins to current limit ( -12.00 volt reading begins to decrease). Then turn the control d/e division clockwise.

This completes the Single Supply adjustments.

## PARALLEL SUPPLY ADJUSTMENTS (LOGIC POWER SUPPLY-2 9172

The following adjustments provide alignment of a pair of Logic Power Supplies whose outputs are connected in parallel. These adjustments are necessary to avoid circulating currents and other undesirable effects.

Both Logic Power Supplies are identical, and therefore either may be used as a master supply or a slave supply. By definition, the supply nearest the front console of a system is operated as the master supply, and the supply at the rear is operated as the slave.

To properly calibrate the supplies, each supply must first be adjusted individually as described previously in this section under SINGLE SUPPLY ADJUSTMENTS. Since adjustments under system load are different, the instructions provided below must be followed. Note that the master/slave setup (below) must be done before the supply covers are replaced at the end of the Single Supply Adjustments procedure.

## Master/Slave Setup

This procedure prepares the two supplies for parallel operation.

## Master Supply

Set the regulator board switches, as indicated in table 4-5, for the master supply (mounted in the front of the cabinet).
Table 4-5. Master Supply Setup

| Switch | Location <br> on Regulator Board | Position |
| :--- | :--- | :--- |
| O.V. DISABLE/RUN (S201) | Top left | RUN (toward board) |
| MASTER/SLAVE (S202) | Top center | MASTER (away from board) |
| 12 V ENABLE/RUN (S203) | Top right | RUN (toward board) |

Replace the top and bottom supply covers. Slide the supply back into the frame and connect cables JLG, J12A, and J12B. Also connect the high-current terminals.

## B 1700 Power Subsystem

## Slàve Süpply

Set the regulator board switches, as indicated in table 4-6, for the slave supply (mounted in the rear of the cabinet).
Table 4-6. Slave Supply Setup

| Switch | Location <br> on Regulator Board | Position |
| :--- | :--- | :--- |
| O.V. DISABLE/RUN (S201) | Top left | RUN (toward board) |
| MASTER/SLAVE (S202) | Top center | SLAVE (toward board) |
| 12 V ENABLE/RUN (S203) | Top right | RUN (toward board) |

Replace the top and bottom supply covers. Slide the supply back into the frame and connect cables JLG, J12A, and J12B. Also connect the high-current terminals. Proceed with the Balance Adjustments.

## Balance Adjustments

These procedures preset the +4.75 and -2.0 voltages to their approximate operating levels with supplies connected in parallel, but under artificial load.

## Preparatory Steps

The following are physical preparations for the balance adjustment.
a. Ensure that both supplies are secured in place, and that the connections to JLG, J12A, J12B, and the high-current terminals are properly made.
b. Remove all four (4) shunt shorting bars. These are located on the bus bars immediately adjacent to the highcurrent terminals. Refer to figure 4-5.

## NOTE

The upper set of shorting bars is for measuring +4.75 volt current. The lower set is for measuring -2.0 volt current.
c. Disengage all logic cards and memory cards in the system. They need not be removed, but must be pulled out of the backplane connectors.
d. Connect the dummy load between the +4.75 volt and GND bus bars, both of which go up the center of the mainframe backplane.
e. Turn ON the circuit breakers of both supplies.
f. Turn system power ON.

## +4.75 Volt Balance Adjustment

This adjustment sets the +4.75 volt outputs of both supplies to exactly the same level.
a. Measure the voltage across the master and then the slave +4.75 volt (upper) shunts with the DVM.
b. Adjust the +4.75 V BALANCE control on the slave supply only until the voltage across both shunts is equal ( $\pm 0.003$ volt).


Figure 4-5. B 1720-Series Current Shunt and Voltage Sense Locations

## B 1700 Power Subsystem

c. Turn off the circuit breakers of both supplies.
d. Turn system power OFF and disconnect the dummy load from the GND volt bus bar (the +4.75 V connection should be left intact).

## - 2.00 Volt Balance Adjustment

This adjustment sets the -2.0 volt outputs of both supplies to exactly the same level.
a. Connect the dummy load between the -2.00 volt and +4.75 volt bus bars, both of which go up the center of the mainframe.
b. Turn ON the circuit breakers of both supplies.
c. Turn system power ON.
d. Measure the -2.0 volt shunt (lower) first across the master supply, and then the slave supply with the DVM.
e. Adjust the -2.00 V BALANCE control on the slave supply only until the voltage across both shunts is equal ( $\pm 0.003$ volt).
f. Turn OFF the circuit breakers of both supplies.
g. Turn system power OFF and disconnect the dummy load.

## Adjustments Under System Load (Parallel Operation)

These procedures repeat the adjustments previously performed, this time with system load connected.

## Parallel Current-Limiting Adjustment

This adjustment sets the +4.75 volt and -2.0 volt current limiter circuits to their final calibration points.
a. Reinstall all logic and memory boards in the system.
b. Turn ON the circuit breakers of both supplies.
c. Turn system power ON.
d. Connect the DVM across the +4.75 volt (upper) shunt on the master supply.
e. Turn the +4.75 V CURRENT control on the master supply slowly clockwise until the DVM reading just stops increasing or until the DVM reads 100 millivolts ( 200 amperes). Do not adjust the control to a reading greater than 100 millivolts.
f. Connect the DVM across the +4.75 volt (upper) shunt on the slave supply.
g. Turn the +4.75 V CURRENT control on the slave slowly clockwise until the reading on the DVM stops increasing or reaches 100 millivolts.
h. Reconnect the DVM across the +4.75 volt shunt on the master supply.
i. Turn the +4.75 V CURRENT control on the master supply slowly counterclockwise until the DVM reading just begins to decrease.
j. Turn the +4.75 V CURRENT controls on both the master and slave supplies one division clockwise (as marked on the access hole). This operation completes the balance adjustment for the +4.75 volt supply outputs.

## B 1700 Power Subsystem

k. Connect the DVM across the -2.00 volt (lower) shunt on the master supply.

1. Turn the -2.00 V CURRENT control on the master supply slowly clockwise until the DVM reading just stops increasing or until it reads 100 millivolts (200 amperes). Do not adjust the control to a reading greater than 100 millivolts.
m. Move the DVM leads to the -2.00 volt (lower) shunt on the slave supply.
n. Turn the -2.00 V CURRENT control on the slave supply slowly clockwise until the DVM reading stops increasing or reaches 100 millivolts.
o. Reconnect the DVM across the -2.00 volt shunt on the master supply.
p. Turn the -2.00 V CURRENT control on the master supply slowly counterclockwise until the DVM reading just begins to decrease.
q. Turn the -2.00 V CURRENT controls on both the master and slave supplies one division clockwise (as marked in the access hole).

## Final Balance Adjustment

This procedure ensures that the +4.75 and -2.0 volt outputs of both supplies track under system load.
a. Repeat the +4.75 V BALANCE adjustment procedure, this time with system load.
b. Repeat the -2.00 V BALANCE adjustment procedure, this time with system load.
c. Turn OFF the circuit breakers of both supplies.
d. Turn system OFF.
e. Replace the shorting bars on all four (4) shunts.

## +4.75 Volt Backplane Adjustment

This adjustment sets the +4.75 volt output to its final operating level.
a. Connect the DVM from the +4.75 V sense point to the GND sense point on the backplane. Refer to figure $4-5$.
b. Turn ON the circuit breakers of both supplies.
c. Turn system power ON.
d. Adjust the master supply +4.75 V VOLTAGE control until a reading of $+4.85 \pm 0.01$ volts is obtained.

## - 2.00 Volt Backplane Adjustment

This adjustment sets the -2.0 volt output to its final operating level.
a. Connect the DVM from the GND sense point to the -2.00 volt sense point on the backplane.
b. Adjust the master supply -2.00 V VOLTAGE control until a reading of $-2.05 \pm 0.01$ volts is obtained.

## +12.0 Volt Backplane Adjustment

This adjustment sets the +12 volt output to its final operating level.

## B 1700 Power Subsystem

a. Connect the DVM from the GND sense point to the bottom of +12 volt bus nearest the console. Refer to figure 4-5.
b. Adjust the +12 V VOLTAGE control on the master supply until a reading of $+12.00 \pm 0.1$ volts is obtained.
c. Turn the +12 V CURRENT control on the master supply counterclockwise until the +12.00 volt channel begins to current limit ( +12.00 volts reading begins to decrease). Turn the +12 V CURRENT control one division clockwise.
d. Repeat steps a through c (above) for the slave supply. Connect to the +12.00 volt bus farthest from the console.

## - 12.0 Volt Backplane Adjustment

This adjustment sets the -12 volt output to its final operating level.
a. Connect the DVM from the GND sense point to the bottom of the -12 volt bus nearest the console.
b. Adjust the -12 V VOLTAGE control on the master supply until a reading of $-12.00 \pm 0.1$ volts is obtained.
c. Turn the -12 V CURRENT control on the master supply counterclockwise until the -12.00 volt channel begins to current limit ( -12.00 volts reading begins to decrease). Turn the -12 V CURRENT control clockwise one division.
d. Repeat steps a through c (above) for the slave supply. Connect the DVM to the -12.00 volt bus farthest from the console.

## SINGLE SUPPLY ADJUSTMENTS (LOGIC POWER SUPPLY-1, -3 AND -4)

Use the following procedure to calibrate individual logic power supplies. In systems employing more than one supply, perform the following adjustments separately for each before proceeding to the Parallel Adjustments.

## CAUTION

All test equipment must be isolated from power ground, and the test equipment chassis must never touch the logic power supply chassis. Otherwise, extensive damage to the equipment will result.

## WARNING

Lethal voltages are present within the logic supply. Use extreme caution when working with the top cover removed.

## Preparations for Calibration

To perform the calibration, first disconnect the supply from the data processing system. This includes disconnecting connectors J12A, J12B, JLG and the high-current terminals. Do not remove the ac power cable.

## CAUTION

Make sure the system power is off before disturbing any connections.
When the supply has been disconnected, perform the following steps in order.
a. Extend the supply from the system and remove the top cover.
b. Connect the logic supply dummy load between the +4.75 V output terminal and ground.
c. Remove all the power supply circuit cards.
d. Remove the 40 Amp. fuse (F1).

## Detailed Alignment

The following procedures are separated into sections which basically follow the main divisions of circuitry within the supply. Each procedure should be performed in the order listed. Refer to figure 4-6 (Logic Power Supply-1 and -3) or figure 4-7 (Logic Power Supply-4) as appropriate for the following procedures.


Figure 4-6. Logic Supply Card and Control Locations
(Logic Power Supply-1 and -3)


Figure 4-7. Logic Supply Card and Control Locations
(Logic Power Supply-4 Only)
+160 Volt Regulator Adjustment
This adjustment sets the +160 voltage to its proper operating level.
a. Insert the 160 Volt Regulator Card into J3 (see figure 4-6).
b. Make sure the NORMAL/OFF switch on the 160 V regulator card is in the NORMAL position.
c. Turn the logic supply breaker and the system POWER switch ON.
d. Insert the DVM probes into the +160 V and COMMON test jacks on the front of the supply. Refer to figure 4-8.
e. Adjust the 160 ADJ . control (R10 on the top edge of the card) for a meter reading of $+160, \pm 5$ volts.
f. Turn the NORMAL/OFF switch OFF.
g. Turn the supply breaker OFF.


Figure 4-8. Logic Power Supply Test Jacks

## Control Card Adjustment

This adjustment sets the control voltages to their proper working level.
a. Insert the control card into J4.
b. Turn the supply breaker ON .
c. Connect the DVM to the +24 V and GRD test jacks. Adjust control R2(+24V ADJ.) for a reading of +24.0 , $+0,-2.0$ volts.
d. Connect the DVM to the +4.5 V and GRD test jacks. Adjust control R21 (+4.75V ADJ.) for a reading of $+4.75 \pm 0.1$ volts.
e. Connect the DVM to the -1.9 V and GRD test jacks. Adjust control R25 (-1.9V ADJ.) for a reading of -2.0 $\pm 0.3$ volts.
f. Connect the DVM to the -15 V and GRD test jacks. Adjust control R11 (-15V ADJ.) for a reading of -15.0 $\pm 0.1$ volts.
g. Connect the DVM to the +15 V and GRD test jacks. The meter reading should be $+15.0 \pm 0.1$ volts. Since the +15 V supply tracks the -15 volt supply, there is no adjustment.
h. Turn the supply breaker OFF.

## VCO Card Adjustment (Logic Power Supply-1 and -3)

This adjustment balances the +4.75 volt current limiter circuit.
a. Insert a card extender in J 1 , then insert the VCO card in the extender.
b. Short VCO card backplane pins 1 W and 0 Q together. This may be done by spot soldering a short piece of wire to the etching adjacent to each of the two pins.
c. Connect the DVM between pin M of chip F2 and pin OR on the VCO card backplane. Note that figures 5-29 and 5-30 (section 5) show the component layout of this card.
d. Turn the supply breaker ON .

## B 1700 Power Subsystem

e. Adjust the NULL control (R13) until a reading of $0.000 \pm 0.020$ volts is obtained.
f. Turn the supply breaker OFF.
g. Remove the short between pins 1 W and 0Q.

## NOTE

Do not remove the shorting wire entirely, as it will be used again later.

## VCO Card Adjustment (Logic Power Supply-4)

This adjustment balances the +4.75 volt current limiter circuit.
a. Insert a card extender in J1. Then insert the VCO card in the extender.
b. Short VCO card backplane pins 1 W and OQ together. This may be done by spot soldering a short piece of wire to the etching adjacent to each of the two pins.
c. Connect the DVM between pin M of chip F2 and pin OR on the VCO card backplane. Note that figures 5-27 and 5-28 (section 5) show the component layout of this card.
d. Turn the supply breaker ON.

e. Adjust the NULL 1 control (R20) until a reading of $0.000 \pm 0.020$ volt is obtained.
f. Connect the DVM between chip GO pin K and VCO card ground.
g. Adjust the NULL 2 control (R22) until a reading of $0.000 \pm 0.020$ volt is obtained.
h. Turn the supply breaker OFF.
i. Remove the short between pins 1 W and 0 Q .
j. Short VCO card pins 0 E and 1 E together.
k. Connect the DVM between chip A1 pin K and VCO card ground.

1. Turn the supply breaker ON.
m. Adjust the NULL 3 control (R24) until a reading of $0.000 \pm 0.020$ volt is obtained.
n. Turn the supply breaker OFF.
o. Remove the short between pins 0 E and 1 E .

## NOTE

Do not remove the shorting wire entirely, as it will be used again later.

## Delay Adjustment

This adjustment sets the VCO output pulse length.
a. Move the NORMAL/OVERRIDE switch on the VCO card to the OVERRIDE position.
b. Connect the oscilloscope channel 1 probe to pin H of chip A1 (F3 on master/slave capable supply) on the VCO card.

## NOTE

Component layouts for the circuit cards are shown in section 5.
c. Turn the supply breaker ON .
d. Measure the negative-going output pulse from this chip. The pulse should be $40 \pm 2$ usec in length. Adjust the DELAY control (R37; R61 in master/slave capable supplies) for proper pulse length if necessary.
e. Turn the supply breaker OFF.

## Gate Driver Pulse Check

This check verifies that the Inverter SCR drive pulses are being generated properly.
a. Insert the Gate Drive card into J2.
b. Turn the supply breaker ON .
c. Verify that the gate driver waveforms of Power SCR's A1, A2, A3 and A4 appear as shown in figure 4-9. These may be checked by connecting the scope probe to test jacks A1 $\rightarrow$ A4 in sequence. Use the corresponding REFERENCE jack for probe ground in each case.
d. Verify that the gate driver waveforms of commutating SCR's A5 and A6 appear as shown in figure 4-10. Use test jacks A5 and A6, along with the corresponding REFERENCE jacks.
e. Move the NORMAL/OVERRIDE switch back to the NORMAL position.
f. Recheck test points A1 $\rightarrow$ A6. No pulses should be present in the NORMAL mode.
g. Turn the supply breaker OFF.

A1, A2, A3, A4


Figure 4-9. Power SCR Gate Driver Pulses


Figure 4-10. Commutating SCR Gate Driver Pulses

- 2.00 Volt Adjustment

This adjustment sets the -2.0 volt output to its approximate working level.
a. Install the 40 amp fuse.
b. Move the NORMAL/OFF switch on the +160 Volt Regulator card to the NORMAL position.
c. Insert the - 2.0 Volt Regulator card into J5.
d. Move the NORMAL/SERVICE switch on the -2.0 Volt Regulator Card to the SERVICE position.
e. Connect the logic supply dummy load between the +4.75 V high current terminal (stud) and the Ground Terminal.

## NOTE

Do not short the -2.0 volt terminal to ground.
f. Connect the DVM between the -2.00 volt high current terminal (stud) and the Ground terminal.
g. Turn the supply breaker ON.
h. Adjust the -2.00 volt output to $-2.00 \pm 0.01$ volts, using control R16 ( -2 V ADJ) on the -2.0 Volt Regulator Card.

## + 4.75 Volt Adjustment

This adjustment presets the +4.75 volt output to its approximate working level.
a. Connect the DVM between the +4.75 volt high current output terminal (stud) and ground.
b. Adjust the output voltage to $+4.75 \pm 0.01$ volts by way of control R7 [R12 in Logic Power Supply-4] ( +4.75 V ADJ) on the VCO card.
c. Turn the supply breaker OFF.

## Inverter Adjustment

This adjustment sets the length of the inverter pulses to the proper value.
a. Verify that the oscilloscope chassis is isolated from power ground (ground pin of 3-prong ac plug must be removed or disconnected).
b. Connect the oscilloscope from transformer T2 pin 3 (probe) to pin 4 (ground clip). Refer to figure 4-11.
c. Turn the supply breaker ON .
d. Adjust the VCO card DELAY control (R37; R61 on master/slave capable supplies) to obtain an inverter pulse length of $60 \pm 2$ usec. Refer to figure 4-12.
e. Turn the supply breaker OFF.


Figure 4-11. Transformer T2 Test Connections
(Inverter Adjustment)


Figure 4-12. Inverter Pulses

## Null Verification (Logic Power Supply-1 and -3)

This adjustment verifies that the +4.75 volt current limiter comparator is balanced.
a. Short together VCO card backplane pins 1 W and 0 Q .

## NOTE

Card should still be in extender.
b. Connect the DVM between pin M of chip F2 and backplane pin OR (on the VCO card).
c. Turn the supply breaker ON .
d. Adjust the NULL control (R13) for a reading of $0.000 \pm 0.020$ volt.
e. Turn the supply breaker OFF.
f. Remove the short between pins 1 W and 0 Q .

## NOTE

Remove the shorting wire entirely.
g. Remove the card extender and insert the VCO card directly into J 1.

At this time, the following switch settings should be made or verified:
a. Move the NORMAL/SERVICE switch on the -2.0 Volt Regulator Card to NORMAL.
b. Verify that the NORMAL/OFF switch on the +160 Volt Regulator Card is in the NORMAL position.
c. Verify that the NORMAL/OVERRIDE switch on the VCO card is in the NORMAL position.

## Null Verification (Logic Power Supply-4)

This adjustment verifies that the +4.75 volt current limiter comparator is balanced.
a. Short together VCO card backplane pins 1 W and 0 Q .

## NOTE

Card should still be in extender.
b. Connect the DVM between pin M of chip F2 and backplane pin OR (on the VCO card).
c. Turn the supply breaker ON.

## B 1700 Power Subsystem

d. Adjust the NULL 1 control (R13; R20 on master/slave capable supplies) for a reading of $0.000 \pm 0.020$ volt.
e. Turn the supply breaker OFF.
f. Connect the DVM between pin K of chip GO and VCO card ground.
g. Turn the supply breaker ON .
h. Adjust the NULL 2 Control (R22) until a reading of $0.000 \pm 0.020$ volt is obtained.
i. Turn the supply breaker OFF.
j. Remove the short between pins 1 W and 0 Q .
k. Short together VCO card backplane pins 0 E and 1 E .

1. Connect the DVM between pin K of chip A1 and VCO card ground.
m . Turn the supply breaker ON.
n. Adjust the NULL 3 control until a reading of $0.000 \pm 0.020$ volt is obtained.
o. Turn the supply breaker OFF.
p. Remove the short between pins 0 E and 1 E .

## NOTE

Remove the shorting wire entirely.
q. Remove the card extender and insert the VCO card directly into J1.

At this time, the following switch settings should be made or verified:
a. Move the NORMAL/SERVICE switch on the -2.0 Volt Regulator Card to NORMAL.
b. Verify that the NORMAL/OFF switch on the +160 Volt Regulator Card is in the NORMAL position.
c. Verify that the NORMAL/OVERRIDE switch on the VCO card is in the NORMAL position.

## $\pm 12$ Volt Adjustment

This procedure sets the $\pm 12$ volt outputs to their approximate working levels.
a. Insert one 12 Volt Supply Card into J6 and the other 12 Volt Supply Card into J7.

## NOTE

The cards are interchangeable.
b. Turn the supply breaker ON.
c. Connect the DVM between the +12 A test jack and the GRD jack just below.
d. Adjust R4 (+12V ADJ) on the +12 Volt Supply card (in J6) for a reading of $+12.0 \pm 0.1$ volts.
e. Connect the DVM between the -12 B test jack and the GRD jack just below.
f. Adjust R4 (-12V ADJ) on the $\mathbf{- 1 2}$ Volt Supply card (in J7) for a reading of $\mathbf{- 1 2 . 0} \pm 0.1$ volts.
g. Turn the supply breaker and the system power OFF. Disconnect the dummy load.

These portions of the logic supply adjustments which are conducted with no load or under artificial load are now completed. For systems employing a single logic supply, continue with the Adjustments Under System Load (below). For systems employing two logic supplies, proceed to the Parallel Supply Adjustments in this section.

## Adjustments Under System Load (Single Logic Supply)

The following procedure is the final step in calibrating a logic power supply, and applies only to systems employing a single supply.

## Preparatory Steps

This procedure connects the supply to the system load.
a. Place a $3 / 8^{\prime \prime}$ plain washer on the GND terminal, then slide the supply into the B 1700 cabinet and secure with the front panel screws.
b. Connect the bus bars to the +4.75 volt, GND, and -2.0 volt terminals.
c. Connect the cables which mate with JLG, J12A, and J12B.

## +4.75 Volt Backplane Adjustment

This procedure sets the +4.75 voltage to its final operating level.
a. Turn the supply breaker ON , then turn the system power ON .
b. Connect the DVM between the +4.75 volt and GND bus bars at the backplane. Refer to figure 4-4.
c. Adjust the +4.75 V ADJ. control (R7) for a reading of $+4.85 \pm 0.01$ volts.
d. Adjust the +4.75 V CURRENT LIMIT control (R15) until the +4.85 V reading just begins to decrease. (This is the current limiting point.) Then turn the current limit control four turns in the opposite direction.

## - 2.0 Volt Backplane Adjustment

This procedure sets the -2.0 voltage to its final operating level.
a. Connect the DVM between the -2.0 volt and GND bus bars at the backplane. Refer to figure 4-4.
b. Adjust the -2 V ADJ control (R16) for a reading of $-2.05 \pm 0.01$ volts.
c. Adjust the -2 V CURRENT LIMIT control (R42) until the -2.05 V reading just starts to decrease, then turn the current limit control four turns in the opposite direction.

## +12.0 Volt Backplane Adjustment

This procedure sets the +12 voltage to its final operating level.
a. Connect the DVM between the end of the +12 V bus and the GND bus. See figure 4-4.
b. Adjust the +12 V ADJ control ( R 4 of 12 V card in J 6 ) for a reading of $+12.0 \pm 0.1$ volts.
c. Adjust the +12 V CURRENT LIMIT control (R28 of 12 V card in J 6 ) until the +12 V reading just starts to decrease. Then turn the control two turns in the opposite direction.

## - 12.0 Volt Backplane Adjustment

This adjustment sets the -12.0 voltage to its final operating level.
a. Connect the DVM between the bottom of the -12 V bus and the GND bus. See figure 4-4.
b. Adjust the -12 V ADJ. control ( R 4 of 12 V card in J 7 ) for a reading of $-12.0 \pm 0.1$ volts.
c. Adjust the -12 V CURRENT LIMIT control ( R 28 of 12 V card in J 7 ) until the -12 V reading just starts to decrease. Then turn the control two turns in the opposite direction.

This completes the single supply adjustments.

## PARALLEL SUPPLY ADJUSTMENTS (LOGIC POWER SUPPLY-4)

The following adjustments provide alignment of a pair of logic power supplies whose outputs are connected in parallel. These adjustments are necessary to balance the outputs of the two supplies, thus minimizing circulating currents and other undesirable effects.

Both logic power supplies are identical. Either can be used as the master supply or the slave supply. By convention, the supply nearest the front console of a system is operated as the master supply; the supply directly behind it is operated as the slave. A third supply, if used (in an extension cabinet), operates independently.

To properly calibrate the supplies, each supply must first be adjusted individually as described previously in this section under SINGLE SUPPLY ADJUSTMENTS (excluding the ADJUSTMENTS UNDER SYSTEM LOAD, which do not apply). Once this has been done, proceed with the PARALLEL ADJUSTMENTS described below. Note that the master/slave setup must be done before the top covers of the supplies are replaced.

## Master/Slave Setup

This procedure prepares the two supplies for parallel operation.

## Master Supply

a. Verify that the MASTER/SLAVE switches on the VCO card and the -2 Volt Shunt Regulator card are both in the MASTER position.
b. Replace the top supply cover, then slide the supply back into the frame and secure with the eight (8) front panel screws.
c. Connect the bus bars to the +4.75 volt, GND and -2.0 volt terminals. Also connect the cables which mate with JLG, J12A and J12B.

## Slave Supply

a. Move the MASTER/SLAVE switches on the VCO card and the -2.0 Volt Shunt Regulator card both to the SLAVE position.
b. Replace the top supply cover, then slide the supply back into the frame and secure with the eight front panel screws.
c. Connect the bus bars to the +4.75 volt, GND, and -2.0 volt terminals. Also connect the cables which mate with JLG, J12A and J12B.

## CAUTION

Do not apply power to the system with both supplies in the same mode.

## Balance Adjustment

This procedure balances the +4.75 volt and -2.0 volt outputs of the master and slave logic power supplies.
a. Verify that all logic cards normally used in the system are inserted in the backplane. This condition is necessary for proper adjustment.
b. Make sure that the system power is OFF. Then remove the shorting bars across the 4 shunts, and re-tighten the bolts. Refer to figure 4-5.
c. Turn the system power ON .
d. Measure the voltage across the +4.75 V shunt nearest the master supply and record the measurement.
e. Measure the voltage across the +4.75 V shunt nearest the slave supply and record the measurement.
f. Determine the voltage which is mid-way between the two readings and adjust the +4.75 Volt CURRENT BALANCE control in the slave until the value is obtained.

## NOTE

DVM still connected across slave +4.75 shunt.
g. Reconnect the DVM across the +4.75 V master shunt and compare this reading with that across the slave shunt. Repeat steps $d, e$, and $f$ until less than 1 millivolt difference is obtained.
h. Perform the same procedure for the -2 volt outputs, measuring across the -2 volt shunts and adjusting the -2 volt CURRENT BALANCE control (in the slave supply).
i. Turn the system power OFF.
j. Reinstall the four shorting bars, tightening the connections securely.

## +12.0 Volt Backplane Adjustment

This procedure sets the +12 voltage to its final operating level. Note that the 12 volt adjustments are the same as in Single Logic Supply operation, and must be performed separately for each supply.
a. Turn the system power ON.
b. Connect the DVM between the end of the +12 V bus and the GND bus nearest the front of the system. Refer to figure 4-5.
c. Adjust the +12 V ADJ control of the front logic supply ( R 4 of 12 V card in J 6 ) for a reading of $+12.0 \pm 0.1$ volts.
d. Adjust the +12 V CURRENT LIMIT control of the front logic supply (R28 on 12 V card in J6) until the +12.0 V reading just starts to decrease. Then turn the control two turns in the opposite direction.
e. Repeat $b$ thru $d$ (above), measuring at the +12 V bus nearest the rear of the system, and adjusting the +12 V controls in the rear logic supply.

## - 12.0 Volt Backplane Adjustment

This procedure sets the -12.0 voltage to its final operating level. As with the +12 V adjustment, the -12 V adjustment must be done separately for each logic supply.

## B 1700 Power Subsystem

a. Connect the DVM between the lower end of the -12 V bus and the GND bus nearest the front of the system. Refer to figure 4-5.
b. Adjust the -12 V ADJ control of the front logic supply ( R 4 of 12 V card in J 7 ) for a reading of $-12.0 \pm 0.1$ volts.
c. Adjust the - 12V CURRENT LIMIT control of the front logic supply ( R 28 on 12 V card in J 7 ) until the -12.0 volt reading just starts to decrease. Then turn the control two turns in the opposite direction.
d. Repeat a thru c, measuring at the -12 volt bus nearest the rear of the system and adjusting the -12 V controls in the rear logic supply.

This completes the parallel supply adjustments.

## MEMORY POWER SUPPLY ADJUSTMENTS

The memory power supply adjustments are divided into three parts: Overvoltage Adjustments, Voltage Adjustments, and Current Limit Adjustments. These adjustments are performed separately for each of the three supply sections, and are to be made under the following conditions:
a. Overvoltage Adjustments. These adjustments must be made prior to the final settings of any of the memory voltages. The overvoltage adjustments serve to ensure that damage to the memory will be prevented in the event that the allowable upper voltage limits are exceeded either through misadjustment or malfunction.
b. Voltage Adjustments. These adjustments set the three memory supply output voltages to their proper operating levels. They are made in two stages, first with the storage cards removed, and then again with the cards in place.
c. Current Limit Adjustments. These adjustments are made prior to installation, and need to be checked and reset only when a memory supply is changed in the field or when components which could affect them have been replaced.

## TEST EQUIPMENT

For the general adjustment procedures, a digital voltmeter (DVM) is required. A Burroughs model 3300 (or equivalent) is suitable. For the current limit adjustments (only), the following load resistors are required:
a. One $1.9 \Omega \pm .01 \% 200$ Watt (for +19 V supply).
b. One $2.6 \Omega \pm 5 \% 10$ Watt (for +4 V supply).
c. One $2.0 \Omega \pm 5 \% 15$ Watt (for -5 V supply).

## NOTE

For the $2.6 \Omega$ resistance, two each $\mathrm{P} / \mathrm{N} 11002938$ may be used.
For the $2.0 \Omega$ resistance, use one $\mathrm{P} / \mathrm{N} 11112190$.

## DETAILED ALIGNMENT

The complete alignment procedure for memory power supplies include Overvoltage adjustments, Voltage adjustments, and Current Limit adjustments. These three procedures are to be performed in the sequence listed.

## Overvoltage Adjustments

The following adjustments set the overvoltage trip points for each of the memory supply sections. Perform the following steps in order:
a. Turn the system power OFF.

## B 1700 Power Subsystem

b. Remove all memory storage cards from the backplane (within the memory unit being serviced). Note that the B 1710 Series Central Systems have only one memory unit; the B 1720 Series Systems can have up to four.
c. Turn the system power ON.
d. Turn each of the three CWBR (Crowbar) controls three turns counterclockwise. Refer to figures 4-13 and 4-14. The locations and reference numbers for these controls differ somewhat in the older and newer versions of the supply. Use whichever of the two illustrations is appropriate.
e. Using the DVM, adjust the supply output voltage levels as follows:

| Control | Adjust To | Referenced To | Measure At |
| :---: | :--- | :--- | :--- |
| +19 V Voltage | $+20 \mathrm{~V} \pm 0.1 \mathrm{~V}$ | Ground | 1 AY |
| +23 V Voltage | +5.0 V | +19 V Output | 0 AY |
| -5 V Voltage | -6.0 V | Ground | 0 ZY |

NOTE
Measurement locations are backplane pin numbers. (Any storage card position may be used.) Use backplane pin YB1J of the same position as the logic ground reference.
f. Connect the DVM to each of the measurement points used above. At each one, turn the associated crowbar (CWBR) control clockwise slowly until the supply section being adjusted drops its output voltage.
g. Turn the system power OFF.
h. Turn each of the CWBR controls $1 / 4$ turn counterclockwise, then proceed to the Voltage Adjustments.

## Voltage Adjustments

The following adjustments set the supply output voltages to their operating levels. Perform the following steps in the order listed:
a. Turn the system power ON (storage cards still removed).
b. Verify that the ac input voltage is between 188 and 253 volts.
c. Using the DVM with logic ground (backplane pin YB1J of any storage card location) as a reference, adjust the supply output voltages as follows:

| Adjustment | Measure at (Backplane locations) | Adjust to |
| :--- | :--- | :---: |
| +19 V Voltage | Any Storage Card, Pin 1AY | $+18.75 \pm 0.05 \mathrm{~V}$ |
| +23 V Voltage | Any Storage Card, Pin 0AY | $+3.60 \pm 0.02 \mathrm{~V} *$ |
| -5 V Voltage | Any Storage Card, Pin 0ZY | $-5.00 \pm 0.05 \mathrm{~V}$ |
| * Reference to +19 V (Pin 1AY of any storage card). |  |  |

d. Turn the system power OFF.
e. Install all storage cards in the memory unit.
f. Turn the system power ON. Recheck all voltages. Adjust if necessary.


Figure 4-13. Memory Power Supply Controls (Current Version, P/Ns 22111942 and 2210 9052)


Figure 4-14. Memory Power Supply Controls
(Earlier Version, P/N 2201 4229)

## Current Limit Adjustments

The following adjustments set the current limiting circuits to their proper operating settings. Note that the output voltages must be within specifications before proceeding with the current limit adjustments.

Perform the following steps in the order listed:
a. Turn the system power OFF.
b. Disconnect the memory power supply input and output cables. Remove it from the system frame. Move to a suitable work area where $188-253 \mathrm{VAC}, 50 / 60 \mathrm{~Hz}$ power is available.
c. Turn each of the Current Limit Controls (+19V C.L., + 23V C.L. and - 5V C.L.) three turns counterclockwise.
d. Install load resistors on the supply outputs (refer to figure 4-15) as follows:

B 1700 Power Subsystem

| Resistor | From $\leftarrow$ Connect $\rightarrow$ | To |
| :---: | :---: | :--- |
| $1.9 \Omega$ | 200 W | +19 V Terminal |
| $2.6 \Omega$ | 10 W | +23 V Terminal |
| $2.0 \Omega$ | 15 W | $-5 V$ Terminal |



Figure 4-15. Memory Supply Dummy Load Connections
e. Apply ac power to the supply.
f. Connect the DVM across each load resistor in turn, and turn the corresponding Current Limit control clockwise until the reading just starts to decrease.
g. Remove the ac power, then disconnect the load resistors and reinstall the supply in the system.
h. Recheck the memory supply output voltages under system load (storage cards installed). Repeat the adjustments if necessary.

This completes the memory power supply adjustments.

## +20 VOLT PAPER TAPE POWER SUPPLY ADJUSTMENTS

Two adjustments are necessary for proper functioning of the +20 Volt Paper Tape Power Supply: the Overvoltage Protector Adjustment and the Output Voltage Adjustment.

## TEST EQUIPMENT

A digital voltmeter (DVM) is required for the +20 volt supply adjustments. A Burroughs model 3300 (or equivalent) is suitable.

## DETAILED ALIGNMENT

Perform the Overvoltage Protector Adjustment and the Output Voltage Adjustment in the order listed.

## Overvoltage Protector Adjustment

This adjustment sets the overvoltage trip level. Proceed as follows:
a. Turn the system power OFF. Then remove the load from the +20 volt power supply by disconnecting (at the I/O distribution panel) the cable going to the paper tape punch or paper tape reader.
b. Turn the Overvoltage Protector Adjust (OVP) control fully clockwise, and the +20 Volt Adjust control fully counterclockwise. Refer to figure 4-16.
c. Connect the DVM to TP1 $(+20 \mathrm{~V})$ and TP2 (Common). Then turn the system power ON.
d. Turn the +20 Volt Adjust control clockwise until a reading of $+22.0 \pm 0.01$ volts is obtained.
e. Slowly turn the Overvoltage Protector Adjust (OVP) control counterclockwise until the protector circuit trips, causing the supply output voltage to fall abruptly to 2 volts or less.
f. Turn the system power OFF.
g. Turn the +20 Volt Adjust control two turns counterclockwise.
h. Turn the system power ON .
i. Slowly turn the +20 Volt Adjust control clockwise and note the point at which the output drops to 2 volts or less. If the trip point is $22 \pm 0.1$ volts, proceed to the Output Voltage Adjustment. If the trip point is not within this specification, repeat steps $b$ through $i$.

## Output Voltage Adjustment

This adjustment sets the supply output voltage to its final operating level. Proceed as follows:
a. Turn the system power OFF.
b. Turn the +20 Volt Adjust control two turns counterclockwise.
c. Turn the system power ON.
d. Slowly turn the +20 Volt Adjust control clockwise until a reading of $20.0 \pm 0.01$ volts dc is obtained.
e. Turn the system power OFF and disconnect the DVM.
f. Reconnect the Paper Tape Punch or Paper Tape Reader cable at the I/O distribution panel.

This completes the +20 Volt Paper Tape Supply adjustments.


Figure 4-16. +20 Volt Paper Tape Power Supply Controls

## B 1700 Power Subsystem

## SECTION 5

## MAINTENANCE PROCEDURES

## GENERAL

This section contains procedures and information to assist in troubleshooting and repair of B 1700 Central System power devices. Included are discussions of preventive maintenance, corrective maintenance, and maintenance references. Note that the preventive maintenance discussion is general, and applies to all the power devices. Separate discussions of corrective maintenance, plus maintenance references (where applicable) are provided for each device.

## PREVENTIVE MAINTENANCE

Periodic attention is not required, other than keeping the supply physically clean and electrical connections tight. It is recommended, however, that the system operating voltages be checked (at the backplane) whenever maintenance work is performed on the processor itself. As part of these checks, it is advisable to physically touch the bus bars to assure that there are no warm-or spots especially at or near the boltedconnections. This "touch" test should be performed when the system has been operating for one half hour or more

## CAUTION

Avoid contacting the bus bars with tools or other metal objects when the system is operating. Always the system OFF when attempting to correct a "hot spot" condition.

Clean and retighten bolted connections which show evidence of poor electrical contact.

## CORRECTIVE MAINTENANCE (LOGIC POWER SUPPLY-2)

To help alleviate servicing problems, a fault location procedure has been devised. This procedure is known as the troubleshooting flow, and constitutes the primary diagnostic tool available for solving power supply problems. Use of the flow enables isolation of a malfunction to individual components or sections within the supply, and should result in considerable savings of time if initiated at the beginning of repair work.

Corrective action should include the following items in the sequence listed:
a. Execute the troubleshooting flow, performing the various tests and observations as directed. When so directed in the flow, change the supply troubleshooting configuration in accordance with the separate instructions provided for this purpose.
b. Repair any faults isolated in the course of troubleshooting. This generally involves replacement of defective components. If the problem appears to be one of misadjustment, calibrate the supply as directed in section 4 (Adjustments) of this manual.
c. Perform the Vexification of Repairs procedure after making the nccessary repairs. This procedure entails checking voltages and waveforms throughout the supply circuit while operating it in the TEST mode. Operation in the TEST mode prevents repeat failures due to remaining unlocated faults.
d. Perform the appropriate adjustment procedures listed in section 4 (Adjustments) of this manual.

## TROUBLESHOOTING FLOW

The troubleshooting flow is presented in diagram form (figure 5-1). The flow consists of a series of tests and observations which lead, by a process of elimination, to isolation and identification of faults existing in the Logic Power Supply. Instructions and conditions applying to the use of the flow are as follows:
a. To use the flow, start at the upper-left corner (Malfunction), and follow the route determined by the outcome of each succeeding test. Each test has two (or more) possible results which either indicates a fault or directs a subsequent test to be performed.
b. When directed to monitor the voltage or waveform appearing at a test point, refer first to the corresponding illusration or listing in the voltage and waveform references. Accompanying each voltage and waveform reference entry are equipment settings and other data needed to perform the test. To conserve space and avoid repetition, those test parameters which are frequently used have been designated standard test conditions and are listed later in this section. The standard test conditions are identified by letters A through I.

## NOTE

In some cases, deviation from the standard conditions is necessary. If so, the additional data required to perform the test is noted in the reference entry.
c. There are four distinct Logic Power Supply Test Configurations in which troubleshooting can be performed. They are:

Configuration 1 (Normal). The power supply is installed in the normal system environment (with system load connected). The supply has normally been operating in this configuration when the failure occurred. Normal is used within the flow only to confirm that a malfunction condition exists.

Configuration 2 (Diagnostic). The power supply is prepared for internal testing. These tests are made while the supply is operating at full power (RUN mode), but with the system load removed and a dummy load attached. The diagnostic configuration is used for the majority of tests in the flow, and follows the normal configuration in sequence.

Configuration 3 (Simulated Operation). The power supply is operated in the TEST mode with all output loads disconnected. This configuration is used for troubleshooting when diagnostic operation is not possible. and to verify that repairs have been effective in restoring the supply to operating condition. Simulated operation is to be employed only when so directed.

Configuration 4 (Static Testing). The power supply is disconnected from input power and output loads. Individual components are tested for shorts, opens, changes in value, for example. Both the RUN/TEST switch ( $\mathrm{S}-105$ ) and the movable fanning strip must be in their respective RUN positions for Static testing. This configuration is used when so directed in the flow, and when the use of other configurations is not possible, such as when physical damage to the supply is evident.

## Placing the Supply in the Diagnostic Configuration

Preparations for internal tests and measurements involve disconnecting the supply from the system and configuring it for ease of access to all test points. The maintenance features which may be utilized when servicing the supply are shown in figure 5-2. To prepare the supply for testing, proceed as follows:
a. Turn system power OFF.
b. Disconnect the +4.75 volt, GND, and -2.0 volt high-current terminals from the system bus bars and disconnect J12A, J12B, and JLG. Extend the supply fully on the slides.
c. Remove the top and bottom supply covers.
$5-q-d, e, F$



Figure 5-1. Logic Power Supply Main Troubleshooting Flow (Sheet 2 of 4)


Figure 5-1. Logic Power Supply Main Troubleshooting Flow (Sheet 3 of 4)

flou chart symbols
(Legend)


TEST POINT
decision
(perform a test or obser--
VATION, AND PROCEED AS
DETERMINE D BY THE RESULTS)
auxilitary operation
(intermediate step to pre-
pare for the next test)
mote: all test points shown on this flow are located ON THE REGULATOR Board EXCEPT (8) (9) $1+300$ volts
terminal
(IDENTIF HCATION OF
problem)

Figure 5-1. Logic Power Supply Main Troubleshooting Flow (Shect 4 of 4)


## B 1700 Power Subsystem

d. Detach the regulator board and inrush control board from their mountings inside the supply and place in the test locations. These locations are shown in figures 5-2 (inrush control board) and 5-3 (regulator board). The latter is installed on a special bracket reserved for this purpose (located on the processor frame).


Figure 5-3. Regulator Board Test Location
e. Inspect each of the circuit boards for evidence of physical damage, burned components, etc. If such damage is apparent, use of the troubleshooting flow should not be attempted. Proceed with static testing in Configuration 4. When all defective components have been located and replaced, perform the Verification of Repairs procedure, presented in this section.

## CAUTION

The following step directs connection of the dummy load. DO NOT, under any circumstances, short the -2.0 volt and GND output terminals together when connecting the load.
f. Connect the dummy load between the -2.0 volt and +4.75 volt output terminals. Ensure that the leads do not contact any nearby objects or surfaces.

## Placing the Supply in the Simulated Operation Configuration

The Simulated Operation Configuration involves operating the supply in the TEST mode, with all loads disconnected. To prepare the supply for simulated operation, perform the following steps:
a. Disconnect all cables and leads from the supply, except for the ac input cable. This includes the dummy load, if attached.
b. Move the RUN/TEST switch (S-105) to the TEST position. Refer to figure 5-4.
c. Transfer the movable fanning strip to the TEST position. This will involve loosening all screws holding the strip in place, and moving the lugs, as a group, one position to the right. Retighten the screws. Refer to figure 5-4.


Figure 5-4. RUN/TEST Mode Selection

## VERIFICATION OF REPAIRS

When repairs have been effected, it is desirable to test the supply for proper operation without exposing it to the danger of repeat failures. Such failures can occur because of unlocated faults and the tendency of solid state circuits to experience "chain reaction" failures, destroying numerous components. This hazard may be minimized by testing the supply in Configuration 4 (Simulated Operation) before attempting to operate it at full power.

To verify that the supply has been restored to operating condition, perform the following steps:
a. Place the supply in the Simulated Operation Configuration.
b. Apply ac power and observe the supply to ensure that operation is begun in a satisfactory manner.
c. Using the voltage and waveform references, monitor the condition at each test point within the supply. Observe the standard test conditions shown with each listing or illustration to prepare the equipment for making the measurement.
d. If an unsatisfactory condition is observed, trace it to the source, using the main schematic (figure 5-5) to locate the various test points with respect to the supply sections. When the failing section or stage has been isolated, remove the ac power and locate the defective components through static testing. Replace components as necessary.
e. When satisfactory voltages/waveforms are obtained at all test points, remove ac power and return the supply to the RUN mode. This may be accomplished by moving the RUN/TEST switch ( $\mathrm{S}-105$ ) and the movable fanning strip back to their respective RUN positions.
f. Proceed to section 4 (Adjustments) and calibrate the supply as described therein.

## MAINTENANCE REFERENCES

The following references are provided to assist in troubleshooting and repair work. Included are test point locations, standard test conditions, and voltage and waveform references.



## B 1700 Power Subsystem

## Test Point Locations

Figures 5-6 (regulator board), 5-7 (inrush control board), and 5-8 (power board) show the locations of the various test points used in test and repair work. In most cases, these are vertical pin lugs, and are best engaged with a spring-loaded hook-style probe. Note that there are two groups of test points with similar identifying numbers. In all cases, those test points appearing on sheet 1 of the main schematic (figure 5-5) are located on the power board (TP1 thru TP34) or on the inrush control board (TP51 thru TP59). Test points appearing on sheet 2 of the main schematic (figure 5-5) are located on the regulator board. All test points on the power board are on the underside.

## Standard Test Conditions

Several standard test conditions have been adopted for making measurements and interpretation of waveforms. These conditions are designated by a letter from A to I, and describe the equipment settings and reference points appropriate to the test point being monitored. A standard test condition entry accompanies each test point listing in the voltage and waveform references. The standard test conditions are divided into groups corresponding to the main circuit divisions within the supply itself, as shown in table 5-1.

Table 5-1. Test Condition Applicability (by Supply Section)
$\underline{\text { Standard Test Condition }} \underline{\text { Section }}$

| A-D | Regulator Board |
| :--- | :--- |
| E-H | Power Board |
| I | Inrush Control Board |

The standard test conditions are listed in table 5-2. Unless otherwise stated, the equipment settings indicated refer to the use of an oscilloscone. Test I utilizes ac line triggering. Any 'ditional equipment settings which apply are noted with the corresponding voltage/waveform reference

Table 5-2. Standard Test Conditions

| Test | Equipment Setting | Reference Point |
| :---: | :---: | :---: |
| A | DC-coupled | Common Test Terminal. for scope |
| B | DC-coupled | Auxiliary Common (TP49) for scope |
| C | AC-coupled | Common Test Terminal unless otherwise noted. |
| D | Voltmeter readings | Common Test Terminal. |
| E | Voltmeter readings | Auxiliary Common (TP49). |
| F | AC-coupled | TP9 or as noted. |
| WARNING |  |  |
| The primary circuit has high voltage present. |  |  |
| G | Voltmeter readings | TP9 |
| WARNING |  |  |
| The primary circuit has high voltage present. |  |  |
| H | AC-coupled | GND output terminal or as noted. |
| I | DC-coupled | TP51 |
| WARNING |  |  |

The primary circuit has high voltage present.


Figure 5-6. Test Point Locations on Regulator Board (Component Side)


Figure 5-7. Test Point Location on Inrush Control Board (Component Side)
5.16


Figure 5-8. Test Point Location on Main Power Board (Underside)

## B 1700 Power Subsystem

## Voltage and Waveform References

The following illustrations and listings indicate the normal voltages and waveforms that should be obtained when monitoring the various test points within the supply. An entry is included for each test point in both the RUN and TEST supply operating modes. When using the voltage and waveform references, always note the "TEST COND." first. This refers to the standard test condition (from table 5-2) which applies to the test point in question. Configure the test equipment as directed in this reference before making the measurement. Note that these voltage and waveform references are a guide only. The voltages and waveforms differ somewhat from one supply to another, and therefore may not appear exactly as illustrated. As a general rule, a monitored voltage or waveform which is reasonably close to the listing or illustration should be considered acceptable.

The voltage and waveform references are divided into three groups of test points: the regulator board (figure 5-9), power board (figure 5-10), and inrush control board (figure 5-11).
(regulator board)

| TP1 +10.000 | TP1 |  |
| :--- | :--- | :--- | :--- |

(A) TEST COND. D
TP1 (RUN)
(B) TEST COND. D
TP1 (TEST) G11073

RÉULATOR BOARD

| TP2 | +6.216 | TP2 | +6.206 |
| :---: | :---: | :---: | :---: |
| (C) TEST COND. D | TP2 (RUN) | (D) TEST COND. D | TP2 (TEST) |

REGULATOR BOARD

| TP3 +14.829 | TP3 |
| :--- | :--- | :--- |
| (E) TEST COND.D |  |

### 611.075

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 1 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 2 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 3 of 17)

(A) TEST COND. B

TP11 (RUN)
(B) TEST COND. B'

TP11(TEST)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 4 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 5 of 17)

| TP18 | +14.248 | TP18 |  |
| :---: | :---: | :---: | :---: |
| (E) TEST COND. $D$ | TP18 (RUN) | (F) TEST COND. D' |  |

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 6 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 7 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 8 of 17)

| TP28 +14.255 | TP28 | -11.1 |
| :--- | :---: | :--- | :--- |
| (E) TEST COND. D TP28 (RUN) | (F) TEST COND. D' | TP28 (TEST) |

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 9 of 17)

(C) TEST COND. B TP32 (RUN)
(D) TEST COND. B'

TP32 (TEST) *


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 10 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 11 of 17)


| TP37 $-0.00^{*}$ | TP37 $+0.00^{*}$ |  |
| :--- | :--- | :--- |
| (C) TEST COND. D | TP37 (RUN) | (D) TEST COND. D' |

* COMPONENTS FOR THIS CIRCUIT OMITTED IN CURRENT VERSIONS OF THE SUPPLY.

| TP38 +14.236 | TP38 |
| :--- | :--- | :--- |
| (E) TEST COND. D TP38 (RUN) |  |

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 12 of 17)



(E) TEST COND. B TP43 (RUN)
(F) TEST COND. BI TP43 (TEST) *

* 12 V ENABLE SWITCH MUST bE IN THE ENABLE POSITION

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 13 of 17)


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 14 of 17)

## B 1700 Power Subsystem



| TP47 $-0.00^{*}$ | TP47 $+0.00^{*}$ |  |
| :--- | :--- | :--- |
| (C) TEST COND. D | TP47 (RUN) | (D) TEST COND. D' $\quad$ TP47 (TEST) |

(C) TEST COND. D

TP47 (RUN)
(D) TEST COND. D'

TP47 (TEST)

* COMPONENTS FOR THIS CIRCUIT OMITTED IN CURRENT VERSIONS OF THE SUPPLY.

| TP48 +14.275 | TP48 |  |  |
| :--- | :--- | :--- | :--- |
| (E) TEST COND. D | TP48 (RUN) | (F) TEST COND. D' | TP48 (TEST) |

Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 15 of 17)


| J203-1 | -15.530 | J203-1 | -13.108 |
| :--- | :--- | :--- | :---: |



Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 16 of 17)

B 1700 Power Subsystem

| C24 |  |  |
| :--- | :--- | :--- | :--- |
| -12.008 | C24 |  |

* 12 V ENABLE SWITCH MUST BE IN THE ENABLE POSITION.


Figure 5-9. Regulator Board Voltage and Waveform References (Sheet 17 of 17)

## B 1700 Power Subsystem



Figure 5-10. Power Board Voltage and Waveform References (Sheet 1 of 13)




Figure 5-10. Power Board Voltage and Waveform References (Sheet 2 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 3 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 4 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 5 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 6 of 13)

(A) TEST COND. F

TP25 (RUN) REF.TP27
(B) TEST COND. F' TP25 (TEST) REF. TP27*

(C) TEST COND. F

TP26 (RUN) REF. TP28
(D) TEST COND. F'

TP26 (TEST) REF. TP28 *


* 12 V ENABLE SWITCH MUST BE IN THE ENABLE POSITION.


Figure 5-10. Power Board Voltage and Waveform References (Sheet 8 of 13)

(A) TEST COND. F

TP31 (RUN) REF. TP29
(B) TEST COND. F'

TP31 (TEST) REF. TP29 *

(E) TEST COND. F TP33 (RUN) REF. TP 32
(F) TEST COND. F' TP33 (TEST) REF.TP32 *

* 12 V ENABLE SWITCH MUST BE IN THE ENABLE POSITION.

Figure 5-10. Power Board Voltage and Waveform References (Sheet 9 of 13)

B 1700 Power Supply



Figure 5-10. Power Board Voltage and Waveform References (Sheet 10 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 11 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 12 of 13)


Figure 5-10. Power Board Voltage and Waveform References (Sheet 13 of 13)

(A) TEST COND. I

(C) TEST COND. I

TP53 (RUN) REF. TP5 1
(D) TEST COND. I'

TP53 (TEST) REF. TP51


Figure 5-11. Inrush Control Board Voltage and Waveform References (Sheet 1 of 3 )
Nush contro (Board


Figure 5-11. Inrush Control Board Voltage and Waveform References (Sheet 2 of 3)


Figure 5-11. Inrush Control Board Voltage and Waveform References (Sheet 3 of 3)

## $\underline{\text { Replacement of Power Transistors }}$

It may be noted that the inverter output stages of the $+4.75 \mathrm{~V},-2.0 \mathrm{~V}$ and +12.0 V channels use the same type transistor. However, the actual transistors used in these channels are notinterchangeable, because they are individually graded by fall time, and assigned different part numbers accordingly. The highest grade units are used in the +4.75 V inverter, with the middle and lowest going to the -2.0 V and +12 V channels, respectively. The part numbers are as follows:

| Channel | Vendor $\mathrm{P} / \mathrm{N}$ | $\underline{\text { Burroughs } \mathrm{P} / \mathrm{N}}$ |
| :--- | :--- | :--- |
| +4.75 V | 500042.2 | 22083562 |
| -2.0 V | 500042.1 | 22083554 |
| +12.0 V | 500042.0 | 22083398 |
| -12.0 V | 500111 | 22083406 Donotsubstitute upi |

In emergency cases, higher grade transistors may be substituted for lower grade units. However, under no circumstances, may different grades be mixed within a given channel (all transistors in the channel must be upgraded for the substitution to work). Because of the grading requirement, no attempt should be made to replace the inverter output transistors with locally purchased parts.

Field replacement with higher graded transistors should be a temporary substitution only, and the correct parts should be fitted as soon as possible.

## Testing and Replacement of Inverter Protective Diodes

Protective diodes are connected in series with the high power switching transistors in each of the inverter output stages. The purpose of these diodes is to protect the transistors against transients resulting from the switching action. These protective diodes are of the press-fit type in the +4.75 volt and -2.0 volt inverters, and are mounted in pairs on small heat sinks. To allow series connection while sharing a common heat sink, one diode of each pair has reversed (internally) anode and cathode terminals. In addition, to satisfy packaging requirements, the diode heat sinks are themselves joined together in pairs (the two halves of which are electrically insulated from one another). The complete 4 -diode assembly is then plugged into the circuit board.

## CAUTION

Since the heat sink assemblies are symmetrical, it is possible to reverse them upon installation. Doing so results in malfunctioning of the inverter of which they are a part. Therefore, when reinstalling the +4.75 volt and -2.0 volt protective diodes use caution to ensure that correct orientation of the heat sink assembly is obtained.

The affected diodes are identified as follows:

Normal polarity (type DRS185): CR118, CR121, CR124. CR127, CR143 and CR146.
Reverse polarity (type DRS1851R): CR117, CR120, CR123, CR126, CR142 and CR145.

## CORRECTIVE MAINTENANCE (LOGIC POWER SUPPLY - 1, - 3 AND - 4)

A troubleshooting flow has been provided to simplify the fault location process. This flow is a series of tests and observations leading to the isolation of a malfunction to individual components or sections within the supply. Use of the flow may result in considerable savings of time if employed at the beginning of repair work. Any corrective action should include the following items in the sequence listed.
a. Perform the various tests and observations as directed by the Troubleshooting Flow (figure 5-12).
b. Repair any faults isolated in the course of troubleshooting. This repair work generally involves replacement of defective components. (Since the Troubleshooting Flow indicates only the general nature of a fault, identification of defective components is usually accomplished by way of static testing, i.e., ohmmeter checks.)
c. Perform the appropriate adjustment procedure listed in section 4 of this manual.

## NOTE

Adjustment alone may be sufficient if misadjustment was the original cause of the problem.

## TROUBLESHOOTING FLOW

The Troubleshooting Flow, presented in diagram form in figure 5-12. consists of a series of tests and observations which lead by a process of elimination to isolation and identification of faults existing in the Logic Power Supply.

The flow starts at the upper left corner (START). The route thereafter is determined by the outcome of the succeeding tests. Each test has two or more possible results, with the outcome indicating either a fault or directing that a subsequent test be performed.

## MAINTENANCE REFERENCES

The following references are provided to assist in troubleshooting and repair work. Included is information on component locations, maintenance features, and waveform references. The supply main schematic is illustrated in figures $5-13$ through 5-21.

## Component Locations

Figures 5-22 through 5-29 illustrate component locations on the various circuit cards used in the supply. The component numbers shown also appear on the main schematic. The locations of other significant components external to the circuit cards are shown in the B 1700 Systems Field Engineering Parts Catalog, Form No. 1057692.



Figure 5-13 Logic Power Supply - $1 \& 3$ Main Schematic
(Sheet 1 of 4)


Figure 5-13 Logic Power Supply - $1 \& 3$ Main Schematic (Sheet 1 of 4 continued)


Figure 5-13 Logic Power Supply - 1 \& 3 Main Schematic
(Sheet 2 of 4 continued)









Figure 5-15 Logic Power Supply - 1 \& 3, -2.0 Volt Shunt Regulator Card Schematic
(Sheet 1 of 2 continued)

B 1700 Power Subsystem


Figure 5-15 Logic Power Supply - 1 \& 3, -2.0 Volt Shunt Regulator Card Schematic
CONTINUED ON NEXT PAGE


(Sheet 1 of 4 continued)

B1700 Power Subsystem









Figure 5-17 Logic Power Supply -4 VCO Card Schematic
(Sheet 1 of 2 continued)




B1700 Power Subsystem


B 1700 Power Subsystem





Figure 5-19. Logic Power Supply-1,-3\&-4,+160 Volt
Regulator Card Schematic
5-68



Figure 5-21. Logic Power Supply-1, -3, \& -4, 12 Volt


Figure 5-22. +160 Vclt Regulator Card Component Locations


Figure 5-23. Control Supply Card Component Locations


Figure 5-24. Gate Driver Card Component Locations


Figure 5-25. -2 Volt Shunt Regulator Card Component Locations (Logic Power Supply -1 \& -3)


Figure 5-26. -2 Volt Shunt Regulator Component Locations (Logic Power Supply -4)


Figure 5-27. VCO Card Component Locations
(Logic Power Supply -1 \& -3)


Figure 5-28. VCO Card Component Locations
(Logic Power Supply 4)


Figure 5-29. 12 Volt Supply Card Component I oncatinne


Figure 5-30. Logic Power Supply Card Extension


Figure 5-31. Logic Power Supply Heat Sink Extension

## B 1700 Power Subsystem

## Maintenance Features

A number of special features have been included in the logic supply to facilitate troubleshooting and repair. These features include the following:
a. Most low-level circuits are located on pluggable circuit cards which can be extended (with the use of a card extender, P/N 2207 0254) for ease of access. Refer to figure 5-30.
b. The supply is mounted on slides which permit extension from the system cabinet and rotation for access to the underside.
c. All internal voltages are available at test jacks on the supply front panel. Also available are the inverter gate driver outputs.
d. All high-power semiconducter devices are located on a multi-section heat sink which swings out of the supply for ease of access. Refer to figure 5-31.

## NOTE

A number of wires must be disconnected before the heat sink can be moved.
e. Internal mode switches are provided to defeat certain protective circuits for test purposes.

## Waveform References

The waveforms shown in figures 5-32 through 5-51 represent signals typically found at the various test points in the logic supply. All measurements were made with the supply driving a 100 ampere load (Logic Supply Dummy Load).

## CORRECTIVE MAINTENANCE (MEMORY POWER SUPPLY)

A troubleshooting flow has been provided to aid in the repairing of a Memory Power Supply which has malfunctioned. This flow is a series of tests and observations which lead by a process of elimination to the location of the failing supply section or component. Corrective action should include the following items in the sequence listed:
a. Perform the various tests and observations as directed by the Troubleshooting Flow (Figure 5-52).
b. Repair any faults that are isolated in the course of troubleshooting. The identification of defective components usually requires static testing in addition to the general checks listed in the Troubleshooting Flow. Refer to the Maintenance References.
c. Perform the appropriate adjustment procedures listed in section 4.

## TROUBLESHOOTING FLOW

The Troubleshooting Flow (figure 5-52) begins in the upper left corner (START). Follow the route determined by the outcome of each test. Each test has two or more possible results, and indicates either a fault, or directs that a subsequent test be performed.

## MAINTENANCE REFERENCES

Component locations within the memory power supply are shown in the B 1700 Systems Field Engineering Parts Catalog, Form No. 1057692. Refer to section 3, figures 3-67 through 3-70 for schematic diagrams of the various circuit divisions within the supply.


Figure 5-32. 160 Volt Regulator Card Internal Waveforms (Measured From Cathodes of CR6, CR9 \& CR14 to +160 V )


Figure 5-34. VCO Comparator Waveforms (Measured at Comparator E0 and B1 on VCO Card)

Figure 5-36. VCO Output Waveforms (Measured at Outputs of Flip-Flop D2 and Multivibrator A1 on VCO Card)



VERTICAL $=5 \mathrm{~V} / \mathrm{CM}$
HORIZONTAL $=2 \mu \mathrm{~S} / \mathrm{CM}$
Figure 5-33. +160 Volt Regulator Gate Driver Pulse (Measured at Pins OP/OR and OP/OK of Connector U3)


Figure 5-35. VCO Internal Waveforms (Measured at Inputs of Flip-Flop D2 on VCO Card)


VERTICAL $=5 \mathrm{~V} / \mathrm{CM}$

HORIZONTAL $=50 \mu \mathrm{~S} / \mathrm{CM}$

Figure 5-37. VCO Card Output Waveforms
(Measured from Pins OK, OH, OD and OG to Ground on VCO Card)


Figure 5-38. Gate Driver Outputs A1-A4
(Measured Across Secondary of Pulse Transformers T1, T2, 44 and T5 on Gate Driver Card)


Figure 5-40. Diode/SCR Bridge Rectifier Output (Measured Between Pins 2 and 3 of Choke L1)


VERTICAL $=100 \mathrm{~V} / \mathrm{CM}$

Figure 5-42. Inverter SCR A1 Output (Measured at A1 Test Jacks on Supply Front Panel)

Figure 5-39. Gate Driver Outputs A5 \& A6 (Measured Across Secondary of Pulse Transformers T3 and T6 on Gate Driver Card)


Figure 5-41. Ripple On +160 Volt Output (Measured Across C6 at Output of +160 Volt Supply)


VERTICAL $=100 \mathrm{~V} / \mathrm{CM}$
HORIZONTAL $=50 \mu \mathrm{~S} / \mathrm{CM}$
Figure 5-43. Inverter SCR's A5 \& A6 Output (Measured at A5 \& A6 Test Jacks on Supply Front Panel)

NOTE: Outputs of A2, A3 and A4 should be similar


VERTICAL $=100 \mathrm{~V} / \mathrm{CM}$
HORIZONTAL $=50 \mu \mathrm{~S} / \mathrm{CM}$

Figure 5-44. Waveform at Commutating Capacitors (Measured Across Capacitors C1 \& C2 in Inverter)

NOTE: Use differential inputs (No Ground)


Figure 5-46. Waveform at Primary of Transformer T2 (Measured Across T2 Primary)


Figure 5-48. High Current Supply Ripple (Measured Across Capacitor C29)


Figure 545. Waveform at Commutating Inductor (Measured Across Inductor L2 in Inverter)


VERTICAL $=10 \mathrm{~V} / \mathrm{CM}$
HORIZONTAL $=50 \mu \mathrm{~S} / \mathrm{CM}$

Figure 5-47. High Current Rectifier Output (Measured Across Pins $1 \& 4$ of Choke L10)


Figure 5-49. High Current Supply Ripple (Measured Across Capacitor C26)

## B 1700 Power Subsystem



VERTICAL $=0.05 \mathrm{~V} / \mathrm{CM}$

Figure 5-50. Ripple on +4.75 Volt Output (Measured From +4.75 Volt Terminal to Ground)


VERTICAL $=0.05 \mathrm{~V} / \mathrm{CM} \quad$ HORIZONTAL $=50 \mu \mathrm{~S} / \mathrm{CM}$ (Measured From -2 Volt Terminal to Ground)

## CORRECTIVE MAINTENANCE (+20 VOLT PAPER TAPE POWER SUPPLY)

To repair a +20 Volt Paper Tape Power Supply which has malfunctioned, proceed as follows:
a. Locate the fault(s) with the aid of the Troubleshooting Chart (table 5-3).
b. Repair any faults isolated on the course of troubleshooting.
c. Upon completion of repairs, perform the appropriate adjustment procedures listed in section 4.

## TROUBLESHOOTING

The troubleshooting procedure for the +20 volt power supply is summarized in table $5-3$. To use the table, examine the supply for evidence of one or more of the symptoms listed. To identify these symptoms use a dc meter or oscilloscope as appropriate. When a symptom has been found, isolate the cause of the fault as directed in table 5-3 under the probable cause and remedy column entries.

## MAINTENANCE REFERENCES

Refer to section 3, figure 3-71, for an overall schematic diagram of the +20 Volt Paper Tape Power Supply Circuit.


* CHECK EACH OUTPUT SEPARATELY

Figure 5-52. Memory Power Supply Troubleshooting Flow
Table 5-3.
+20 Volt Paper Tape Power Supply Troubleshooting

| Symptom <br> Number | Symptom <br> Description | Probable Cause(s) | Remedy |
| :---: | :---: | :--- | :--- |
| 1 | Zero volts dc output. | OUTPUT VOLTAGE control <br> turned fully CCW. | Check OUTPUT VOLTAGE control <br> for proper setting and correct as <br> necessary. |
|  |  | Short circuit across output of <br> supply. <br> Check load, and load connections; <br> correct as necessary. |  |
| F1 open. | Replace F1; if it blows immediately, <br> check shorted diode CR7, Trans- <br> istors Q1, Q2 and, as applicable, Q3 <br> and capacitors C7, C15. Replace as <br> necessary. |  |  |

Table 5－3．
+20 Volt Paper Tape Power Supply Troubleshooting（Cont）

| Symptom <br> Number | Symptom <br> Description | Probable Cause（s） | Remedy |
| :---: | :---: | :---: | :---: |
| 1 （cont） |  | Open CR6 or，as applicable，CR15． | Check CR6 or CR15 for open；re－ place as necessary． |
|  |  | Current sensing resistor open． | Check R22 for open；R6 for short． |
|  |  | Auxiliary rectifier CR1 open． | Check CR1 for open；replace as necessary． |
|  |  | Open CR8，CR9（as applicable） or R1． | Check and replace as necessary． |
| 2 | Unable to adjust output voltage． | Damaged OUTPUT VOLTAGE control． | Check R8 for short and／or open， replace as necessary． |
| 3 | High ripple at line frequency or twice line frequency and unregulated dc out－ put． | Series regulator transistors shorted． | Check and replace as necessary； Q1，Q2 and，as applicable，Q3． |
|  |  | Defective main rectifier causes ripple at twice line frequency． | Check for open and／or short CR2， CR3，CR4 and CR5． |
| 4 | Same as 3 ，except intermittent． | Foreign matter fallen into unit． | Check for loose bench hardware and wire clippings that may have fallen through cover． |
| 5 | High ripple at fre－ quency other than line or twice line frequency． | Oscillation due to defective com－ ponent in filter network． | Check for open C7，C2 and check for open and／or short in C11 and R2．Replace defective component． |
| 6 | Large spikes at out－ put． | Capacitor C5，or as applicable， C4 and C14，open． | Replace C5（or C4 and C14）． |

## CORRECTIVE MAINTENANCE（SYSTEM AC CONTROL）

Repairing an AC Control which has malfunctioned should be accomplished by isolating the failing component and replacing it．Troubleshooting can be performed by way of voltage checks and visual inspection

## WARNING

Lethal voltages are present in the AC Control when the system is connected to the ac power line．Use extreme caution while troubleshooting．Remove the ac power at the source（breaker at service panel of building）prior to replacing defective components．

## B 1700 Power Subsystem

## SECTION 6

## INSTALLATION PROCEDURES

## GENERAL

This section contains installation procedures for the various power supplies used in the B 1700 Central System. Included are procedures for installing Logic Power Supplies, Memory Power Supplies, and Paper Tape Power Supplies. No installation procedure is provided for the AC Control, since field replacement of this unit is normally not required.

## LOGIC POWER SUPPLY INSTALLATION

The procedure for installing a logic power supply depends on the previous type of supply and the replacement type. The Logic Power Supply - 1, - 3 and - 4 and Logic Power Supply - 2 versions are interchangeable electrically, but use different mechanical mounting devices,. Therefore, when switching from one type to another, the mounting hardware must be changed.

## CAUTION

Although the two logic power supply versions can be substituted for one another individually, they are not compatible for master/ slave operation. Therefore, both logic supplies in the main cabinet of B 1720 Series Central Systems must be of the same type.

Three different procedures for logic power supply replacement are provided below. Included are direct replacement of both supply versions with another of the same type, and substitution of the opposite version for each. Use the procedure which is appropriate.

## LOGIC POWER SUPPLY REPLACEMENT

Replacing one Logic Power Supply (any version) with another of the same type involves simply disconnecting all cables and bus bars, removing the old supply from the system cabinet, and installing the new supply in its place. Proceed as follows:
a. Turn the system power OFF.
b. Disconnect the logic supply ac input cable, the output bus bars and connectors $\mathrm{J} 12 \mathrm{~A}, \mathrm{~J} 12 \mathrm{~B}$ and JLG.
c. Remove the front panel retaining screws and extend the supply from the cabinet.

## WARNING

Due to the weight of the power supply, it is recommended that two people perform the following steps. Otherwise, personal injury could result.
d. Release the extension locks on the supply sides, and lift the supply from the cabinet. Refer to figure 6-1.
e. Install the new supply in reverse order of steps $c$ and d above. Note that it is necessary to transfer the chassis sections of the extender slides from the old supply to the new.
f. Perform the appropriate adjustments as described in Section 4 (Adjustments) of this manual before connecting the supply outputs to the system load.


Figure 6-1. Logic Power Supply Removal and Replacement

## B 1700 Power Subsystem

## LOGIC POWER SUPPLY SUBSTITUTION (-2 VERSION FOR - 1, - 3 OR - 4 VERSION)

When substituting the newer version logic power supply ( -2 ) for the older one ( $-1,-3$, or -4 ) requires changing the supply mounting hardware.

## CAUTION

The Logic Power Supply - 2 may only be installed in systems employing compatible memory power supplies. Those supplies can be identified as follows:
a. Modified North Electric supplies bearing a suffix B on the part number, for example, PEC 3604B. These supplies have Burroughs part number 22120067.
b. Burroughs-produced supplies bearing part number 22112049.

This compatibility requirement exists due to a difference in cabinet ventilation patterns produced by the different Power Supply versions.

## NOTE 1

A longer ac power cable is required for use of the Logic Power Supply - 2. The cables concerned carry the same part numbers as previous versions, but are covered by revised specifications. The part numbers for these cables are as follows:

22095244 AC cable for B 1710 systems or B 1720 systems master (front) logic supply.
$22095251 \quad$ AC cable for B 1720 systems slave (rear) logic supply.

## NOTE 2

The master/slave interconnect cable used with the Logic Power Supply - 2 is different from the earlier version. The new cable may be ordered under part number 22104425.

Proceed as follows for the substitution procedure:
a. Remove the existing logic supply as described in the Logic Power Supply Replacement procedure.
b. Remove the remaining portions of the logic supply extender slides from the system cabinet.
c. Install the Logic Power Supply - 2 extender slides in the B 1700 frame as shown in figure 6-2. The slides must be installed on the backplane side of the frame rails, and with the lower mounting screw of each bracket at the hole located $7-5 / 16^{\prime \prime}$ from the base of the frame. Use two \# 10-32 x $5 / 8$ " screws, two \# 10 lock washers and one spacer bar at each bracket location. Note that the wider (offset) side of the spacer bars should be toward the slide.
d. Install the slide chassis sections on the new power supply as shown in figure 6-3. Use a $5 / 16-24$ pivot screw and 5/16" flat washer at the center, and a \# 12-24 tilt stop screw and \# 12 flat washer at the forward end of each chassis section. Ensure that the front (cutaway) end of each chassis section is below its tilt stop screw.


Figure 6-2. Installation of Logic Power Supply - 2 Slides in B 1700 Frame

## WARNING

Due to the weight of the power supply, use two people for the following procedure. Otherwise, personal injury could result.
e. Place the supply in the slides by lifting from both siaes and inserting the chassis slide sections into their tracks in the intermediate sections. Push inwards until the extension locks engage, then check to ensure that the supply may be freely rotated upwards for access to the underside. Check also for freedom of travel into and out of the frame. Refer to figure 6-4.
f. Replace the existing ac power cable(s) with the longer versions. This step is necessary to allow full rotation of the supply when extended.
g. Replace the existing master/slave interconnect cable (B 1720 systems only) with the new version.
h. Install the regulator board bracket on the left rail of the B 1700 frame, as viewed from the frontplane side of the cabinet. Use two \# $10-32 \times 3 / 8$ " screws and two \# 10 lock washers. Place the bracket with the lower mounting screw located 19-5/16" from the base of the rail. Refer to figure 6-5.
i. Perform the appropriate adjustments as described in Section 4 (Adjustments) of this manual before connecting the supply outputs to the system load.


Figure 6-3. Installation of Slide Chassis Sections
(Logic Power Supply - 2)


Figure 6-4. Supply Movement Range (Logic Power Supply - 2)


Figure 6-5. Regulator Board Bracket Installation

## LOGIC POWER SUPPLY SUBSTITUTION ( $-1,-3$ OR - 4 VERSION FOR - 2 VERSION)

Substituting an older version supply ( $-1,-3$, and -4 ) for a newer supply ( -2 ) requires mounting hardware changes.

## NOTE

Substitution of Logic Power Supply - 4 versions for the -2 versions in B 1720 series systems requires that the master/slave interconnect cable be replaced with a cable compatible with these earlier model supplies. The proper cable may be ordered under part number 22095384.

Proceed as follows:
a. Remove the existing logic supply as described in the Logic Power Supply Replacement procedure.
b. Remove the remaining portions of the logic supply extender slides from the system cabinet.
c. Install the Logic Power Supply - 1 extender slides in the B 1700 frame as shown in figure 6-6. The slide brackets must be installed on the backplane side of the frame rails, and with the lower mounting screw of each bracket at the hole located 9-1/4" from the base of the frame. Use four each \# 10 lock washers at each bracket location.
d. Install the slide chassis sections on the logic supply -1 as shown in figure 6-7. Use six each \# 10-32 x 5/8" flat head screws, \# 10 lock washers and \# 10-32 nuts for each.


Figure 6-6. Installation of Logic Power Supply - 1 Slides in B 1700 Frame


Figure 6-7. Installation of Chassis Sections
(Logic Power Supply - 1)

## B 1700 Power Subsystem

## WARNING

Due to the weight of the power supply, use two people for the following procedure. Otherwise, personal injury could result.
e. Place the supply in the slides by lifting from both sides and inserting the chassis sections into their tracks in the intermediate sections. Push inwards until the extension locks engage, then check to ensure that the supply may be freely rotated upwards for access to the underside. Note that the rotation locks on each side must be released to lift the supply. Check also for freedom of travel into and out of the frame. Refer to figure 6-8.
f. Perform the appropriate adjustments as described in Section 4 before connecting the supply outputs to the system load.


Figure 6-8. Supply Movement Range
(Logic Power Supply - 1)

## MEMORY POWER SUPPLY INSTALLATION

Installing a memory power supply can become necessary for one of two reasons: replacement of an existing supply which has failed, or adding a new supply as part of an increase in the size of S-memory. Each is discussed separately.

## REPLACEMENT

Replacing a memory power supply involves simply disconnecting the input and output cables from the old supply, and removing it from its mounting brackets. The new supply is then put in place and connected in reverse order from the removal procedure. Memory power supply mounting in B 1710 Series systems is shown in figure 6-9. For B 1720 Series systems, refer to figure 6-10.

## INSTALLING AN ADDITIONAL SUPPLY

In B 1720 Series systems, the allowable S-memory size can range from the minimum practical size of about 48 K bytes up to a maximum of 256 K bytes. The S -memory is modular, and can easily be expanded in the field. Since one memory supply can support a maximum of 64 K bytes, the maximum configuration $(256 \mathrm{~K})$ would require four such supplies.

B 1700 Power Subsystem


Figure 6-9. Memory Power Supply Mounting (B 1710 Series Systems)


Figure 6-10. Memory Power Supply Mounting (B 1720 Series Systems)

To install an additional memory power supply (as part of a memory expansion) proceed as follows:
a. Determine the number of memory power supplies presently installed in the system. Additional supplies are to be positioned in accordance with the memory unit number they are associated with. Figure $6-11$ shows the proper locations of the four possible memory power supplies.


CONSOLE

Figure 6-11. Memory Supply Locations in B 1720 Series Systems
b. Install the new memory supply in the appropriate location at the rear of the system cabinet. Refer to the supply or supplies already in place for mounting details. Note that the second and fourth supplies (where used) are to be installed upside down with respect to the first and third.
c. Connect the ac power cable from the new supply to the ac distribution box (figure 6-12). The cable to be used for this purpose consists of two parts which are to be joined together, end-to-end, then connected to the ac source. Route the ac cable as shown in figure 6-13.


Figure 6-12. Memory Supply AC Connections
d. Connect the memory voltage distribution cable from the newly-installed memory base backplane to the memory voltage cable from the supply (the two have mating connections). Refer to figure $6-14$. Route the cable as shown in figure 6-13.
e. This completes the supply installation. Verify that the supply is properly adjusted (as described in Section 4 of this manual) before placing it in service.


3 OR 4 MEMORY POWER SUPPLY SYSTEM

LEGEND:

| BACKPLANE WIRING |
| :--- |
| CABLE 22097679 (1 EACH IN CABLE KIT \#1, 2 EACH IN KITS 2, 3, AND 4) |
| CABLE 22095228 (1 EACH IN CABLE KIT \#3, 2 EACH IN KIT \# 4) |
| CABLE 22111686 (1 EACH IN CABLE KIT \#3, 2 EACH IN KIT \#4) |

Figure 6-13. Memory Supply Cabling


Figure 6-14. Memory Supply Output Connections

## +20 VOLT PAPER TAPE POWER SUPPLY INSTALLATION

Installing a +20 Volt Paper Tape Power Supply involves attaching the unit, along with its mounting bracket, to an otherwise unused area on the system frame, and connecting the input and output cabling. Proceed as follows:
a. Turn the system power OFF.
b. Connect the +20 Volt cable (red/green) from the I/O distribution panel to the +20 Volt supply, as shown in figure 6-15. This cable is a "loose end" of the multipair flat cable which runs between the Paper Tape Reader/ Punch I/O Control and the I/O distribution panel. (P/N 18623868 for Paper Tape Reader or 18617191 for Paper Tape Punch.)
c. Install the +20 Volt power supply assembly in the system frame as shown in figure $6-16$. The assembly is to be attached to the frame rails above the logic power supply, with the lower mounting screws in the rail holes 19-3/8" from the bottom. Use a \# $\# 0-32 \times 5 / 8^{\prime \prime}$ screw, a $\# 10$ flat washer and a $\# 10$ lock washer at each mounting hole.

## NOTE

Install the supply in the rear bay of B 1720 series systems.
d. Connect the ac cable ( $\mathrm{P} / \mathrm{N} 22133755$ ) to the ac input terminals of the memory power supply (memory supply \# 1 in B 1720 series systems) as shown in figure 6-17. Route the cable as shown in figure $6-18$ (B 1710 series systems) or figure 6-19 (B 1720 series systems), securing it with cable ties to the system frame or existing wire harnesses at six-inch intervals.
e. Perform the appropriate adjustment procedures as directed in Section 4 (Adjustments) of this manual before attempting operation.

This completes the +20 Volt supply installation.


NOTE: THE OVERVOLTAGE PROTECTOR IS AN INTEGRAL PART OF THE SUPPLY ASSEMBLY.

Figure 6-15. +20 Volt Power Supply Wiring


Figure 6-16. +20 Volt Power Supply Installation


Figure 6-17. +20 Volt Power Supply AC Wiring


Figure 6-18. +20 Volt Power Supply AC Cable Routing (B 1710 Series Systems)


Figure 6-19. +20 Volt Power Supply AC Cable Routing (B 1720 Series Systems)

