B/1965 B/1995

PROCESSOR 9-9S

VOLUME 1 OF 2

CONTAINS

HISTORY SHEET

A 2233 8123 AA BACKPLANE M-PROC 9S
A 2233 8115 AB BACKPLANE M-PROC 9
A 2233 7596 AA CD A9
A 2233 7604 AA CD B9
A 2233 7612 AB CD C9
A 2233 7620 AB CD D9
A 2233 7638 AA CD E9
A 2233 7646 AB CD F9
A 2233 7653 AA CD G9
A 2233 7661 AG CD H9

INSTRUCTIONS JUMPER A 1990 1974 A

CLOCK ALIGNMENT A 2233 3686 D

MAINTENANCE GUIDE

SYSTEM A 2233 5715 AE

UNIT 2228 7700

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	CKT LIST			Remarks or related B/P & Card changes	rev.
	2229	2228				
	1595	7783				

EI 92874		AB+BI			COORDINATE WITH CHANGE TC CD 39 & C9	AA
DC 48055		AC			INCORP. EI 9287A	AA

Unit NO	card name	Document number	rev
2228 7783	8-CARD BACKPLANE	A - 2233 8123	AA

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number 2229 2502	CKT LIST 2229 2510			Remarks or related B/P & Card changes	rev.
EI 9299		AB+EI			CONNECTED -12V TO I/O SLOTS OPX & OVY	AA
EI 9287		AB+EI			COORDINATE WITH CHANGE TO CD B9 & C9	AA
DC46290		AC			INCORP.EI 9299 AND EI 9287	AA
QC46778		AC+ECN			MODIFICATION TO ALLOW USE OF DCP4	AA
QC48247		AC+ECN			CORRECT QC ECN 46778	AA
DC48066		AD			INCORP.QC ECN 46778 AND QC ECN 48247	AA
20002A		AD			ADD IN HIST SHEET REF. ECN 48247	AB

Unit NO	card name	Document number	rev
2228 7700	18 CD B/P M/MEM PROC-9	A - 2233 8115	AB

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46319	2230 2640	2230 2657	2230 2665		INITIAL RELEASE	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST.SHEET	AA

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD A9 M/MEM.PROC.9-9S	A - 2233 7596	AA

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46321	2230 2905	2230 2913	2230 2921		INITIAL RELEASE	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST.SHEET	AA

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD B9 M/MEM.PROC.9-9S	A - 2233 7604	AA

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46462	2229 8483	2229 8491	2229 8509		INITIAL RELEASE	AA
46407	1988 5862	-	-		FIX 9D MONITOR MICRO	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST SHEET.	AA
48241	-	1990 2121	-		DOC.UPDATE. INCORP ECN	AB

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD C9 M/MEM.PROC. 9-9S	A - 2233 7612	AB

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46372	2230 1600	2230 1618	2230 1626		INITIAL RELEASE	AA
46406	1988 5854	-	-		MODIFY RECYCLED AW TO WORK IN TAPE MODE	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST.SHEET.	AA
48241	-	1990 2147	-		DOC.UPDATE. INCORP.ECNS	AB

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD D9 M/MEM.PROC. 9-9S	A - 2233 7620	AB

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46330	2230 1089	2230 1097	2230 1105		INITIAL RELEASE	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST.SHEET	AA

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD E9 M/MEM.PROC. 9-9S	A - 2233 7638	AA

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46391	2229 8228	2229 8236	2229 8244		INITIAL RELEASE	AA
46405	1988 5847	-	-		TO CORRECT ERRORS GENERATED WHEN CD WAS RECYC	AA
47950	1988 7660	-	-		IC P/N CHANGE	AA
48112	-	-	-		RELEASE JUMP. INSTR. AND HIST. SHEET	AA
48241	-	1990 2162	-		DOC UPDATE. INCORP. ECNS	AB

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD F9 M/MEM. PROC. 9-9S	A - 2233 7646	AB

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
46331	2230 2129	2230 2137	2230 2145		INITIAL RELEASE	AA
48112	-	-	-		RELEASE JUMP.INSTR. AND HIST SHEET	AA

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CD G9 M/MEM.PROC. 9-9S	A - 2233 7653	AA

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

" 1987 1110 1

ECN NO	ASSY number	SCHEMA NO	BOARD NO		Remarks or related B/P & Card changes	Doc. issue
46459	1986 0105	1986 0113	1986 0121		INITIAL RELEASE	
46509	1988 6027				RES.CHANGE	
46656	1988 6605				RES.CHANGE	
46658	1988 6613				CORR.SHORT ON CD.	
46727	1988 6944				CORR.SCHEMA.	
46776	1988 7264				P/N CHANGE	
47784	1988 7298				PERFORMANCE IMPR.	
47865	1988 7561				FILTER + 12Vcc	
48015	1988 7637				PROM CHANGE	
47939	1988 7678				IC P/N CHANGE	
48112	1988 7678				RELEASE JMPR INSTR. RELEASE HIST SHEET	AA
48261	1990 2246				PROM CHANGE	AA
48260	1990 2246	1990 2220			DOC.UPDATE INCORP.ECN'S	AB

Unit NO	card name	Document number	rev
2228 7700 2228 7783 1987 1110	CARD H9 FINE/LINE	A - 2233 7661	AG

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
20001A	3158 1754	3158 1846			TO SOLVE CPU CONTROL ERROR	AC
20043A	3158 1986	3158 1994			TO SOLVE INTERMITTENT SELF TEST ERROR	AD
20047A	3158 2141	3158 2166			TO SOLVE INTERMITTENT SELF TEST ERROR	AE
20104A	3158 6449	3158 6464			AVOID ENABLE OF B2CN OF SUBDISTRIB.CARD	AF
20113 A	3158 7397	3158 7405			TO SOLVE A CASSETTE LOADING PROBLEM	AG

Unit NO	card name	Document number	rev
2228 7700 2228 7783	CARD H9 FINE / LINE	A - 2233 7661	AG

Burroughs Corporation Liege plant

L O G I C C A R D H I S T O R Y S H E E T.

ECN number	ASSY number	SCHEMA number rev.	BOARD number rev.		Remarks or related B/P & Card changes	rev.
20001A	3158 1754	3158 1846			TO SOLVE CPU CONTROL ERROR	AC
20043A	3158 1986	3158 1994			TO SOLVE INTERMITTENT SELF TEST ERROR	AD
20047A	3158 2141	3158 2166			TO SOLVE INTERMITTENT SELF TEST ERROR	AE
20104A	3158 6449	3158 6464			AVOID ENABLE OF B2CN OF SUBDISTRIB.CARD	AF
20113 A	3158 7397	3158 7405			TO SOLVE A CASSETTE LOADING PROBLEM	AG

Unit NO	card name	Document number	rev
2228 7700 2228 7783	CARD H9 FINE / LINE	A - 2233 7661	AG

CHANGE SHEET

Burroughs Corporation

COMPUTER SYSTEMS GROUP
PASADENA, CALIFORNIA 91109

PASADENA PLANT
U.S. AMERICA

PAGE	DWG. SIZE	DOC. NO.	REV./ISS.	DSGN. CONT PLT. NO.
1 OF 14	A-	1990 1974	A	011

DOC. TYPE	TITLE	CLASS CODE
-	INSTR-JMPR, M/PROC 9	40205

REV. OR ISSUE	CONTROL DOC. & NUMBER	PREP.	CHKD.	APPD. & DATE	PAGE	LINE OR PARA.	REVISION DESCRIPTION
A	ECN 48112	B.P.	G.P.	S.C. 3/17/83			*****RELEASED*****

TYPED DRAWING

Burroughs Corporation	PAGE 2	DWG. SIZE A-	DWG. NO. 1990 1974	REV. A	DSGN CON PLT NO 01
COMPUTER SYSTEMS GROUP PASADENA, CALIF. 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9		CLASS CODE 40205	
GENERAL QUALITY SPECIFICATION 1183 5543 APPLIES	PREP B.PORTZEL	CHKD G. PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

JUMPER CONFIGURATIONS FOR CARD A9

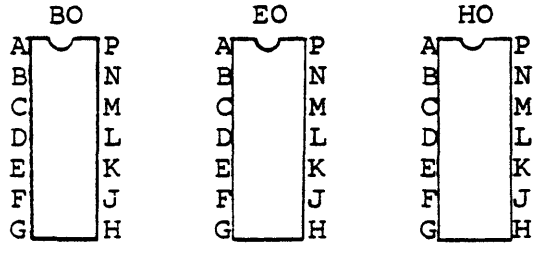
A. S-MEMORY INTERFACE TERMINATION:

NOTE: TERMINATING RESISTORS SHOULD BE INSTALLED ON CARD ASSEMBLIES AT EACH END OF THE S-MEMORY RIBBON CABLES AND REMOVED FROM ALL OTHER ASSEMBLIES CONNECTED TO THE S-BUSES.

THE TERMINATING RESISTORS ARE DIP TYPE RR11,P/N 2228 6777 HAVING A VALUE OF 330/470 OHMS.

FOR THE A9 CARD INSTALL OR REMOVE THE TERMINATIONS AT B0,E0,AND H0 DEPENDING ON THE S-MEMORY DATA CABLE CONNECTOR POSITION:

-INSTALL RESISTOR PACKAGES IF THE A9 CARD IS AT THE END OF THE CABLE.
-REMOVE RESISTOR PACKAGES IF THE A9 CARD IS NOT AT THE END OF THE CABLE.



B. INSTALL THE CONNECTIONS ON THE JUMPER CHIP AT LOCATION K8 ACCORDING TO THE S-MEMORY SIZE.THE MEMORY SIZES AND THE REQUIRED JUMPER CONNECTIONS ARE DEFINED ON PAGE 2.

C. ADJUST THE SYSTEM CLOCK ACCORDING TO THE APPLICABLE SYSTEM TIMING SPECIFICATION.

D. FIXED JUMPER LOCATIONS J8,I0,D9,AND E3 FORMERLY FOR FIELD CARD TEST ARE DEFINED ON PAGE 4.

TYPED DRAWING

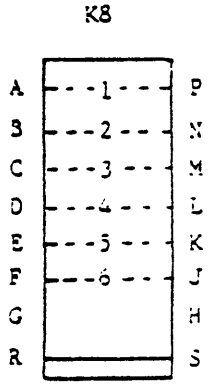
Burroughs Corporation	PAGE 3	DWG. SIZE A-	DWG. NO. 1990 1974	REV. A	DESIGN CONT PL 011
COMPUTER SYSTEMS GROUP PASADENA, CALIF. 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9		CLASS CODE 40205	
GENERAL QUALITY SPECIFICATION 1183 5543 APPLIES	DSGN B. PORTZEL	CHKD. G. PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

JUMPER CONFIGURATIONS FOR CARD A9

THE TOP SIX JUMPERS AT LOCATION K8 MUST BE CONFIGURED ACCORDING TO S-MEMORY SIZE(MAKS). THE TABLE BELOW INDICATES THE JPRN CONNECTIONS REQUIRED FOR EACH AVAILABLE S-MEM. SIZE. FOR A GIVEN S-MEMORY SIZE, THE "1'S" IN THE TABLE INDICATE WHICH PINS TO CONNECT AND THE "0'S" INDICATE WHICH PINS NOT TO.

THE BOTTOM 2 JUMPER POSITIONS ARE NOT RELATED TO MAX-S. THE JUMPER FROM G TO H IS NEVER CONNECTED. THE JUMPER FROM R TO S MUST ALWAYS BE CONNECTED.

MEM. SIZE IN KBYTES	1 A-P	2 B-N	3 C-M	4 D-L	5 E-K	6 F-J
64	1	1	1	1	0	1
128	1	1	1	0	1	1
192	1	1	1	0	0	1
256	1	1	0	1	1	1
320	1	1	0	1	0	1
384	1	1	0	0	1	1
448	1	1	0	0	0	1
512	1	0	1	1	1	1
576	1	0	1	1	0	1
640	1	0	1	0	1	1
704	1	0	1	0	0	1
768	1	0	0	1	1	1
832	1	0	0	1	0	1
896	1	0	0	0	1	1
960	1	0	0	0	0	1
1024	0	1	1	1	1	1
1088	0	1	1	1	0	1
1152	0	1	1	0	1	1
1216	0	1	1	0	0	1
1280	0	1	0	1	1	1
1344	0	1	0	1	0	1
1408	0	1	0	0	1	1
1472	0	1	0	0	0	1
1536	0	0	1	1	1	1
1600	0	0	1	1	0	1
1664	0	0	1	0	1	1
1728	0	0	1	0	0	1
1792	0	0	0	1	1	1
1856	0	0	0	1	0	1
1920	0	0	0	0	1	1
1984	0	0	0	0	0	1
2048	1	1	1	1	1	1

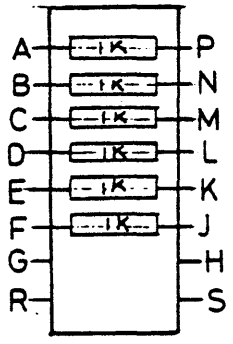


TYPED DRAWING

Burroughs Corporation	PAGE 4	OWG. SIZE A-	DWG. NO. 1990 1974	REV A	DSGN CONT PLT NO 011
COMPUTER SYSTEMS GROUP PASADENA, CALIF 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9		CLASS CODE 40205	
GENERAL QUALITY SPECIFICATION 1183 5543 APPLIES	PREP B.PORTZEL	CHKD G PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

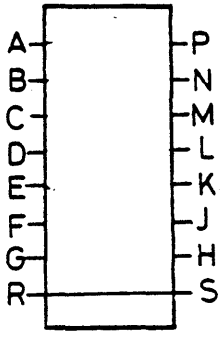
JUMPER CONFIGURATIONS FOR CARD A9

GBNN
J8



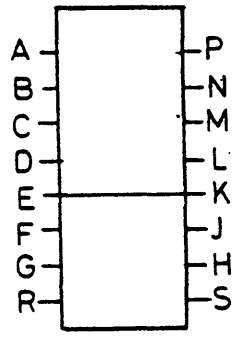
6-1K 1/4W RES
P/N 1111 8734

JPRN
K8

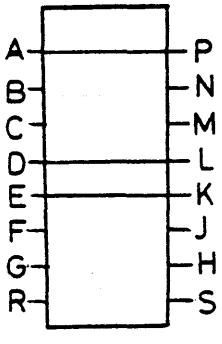


NOTE: JPRN K8 ALSO SHOWN ON PG.3

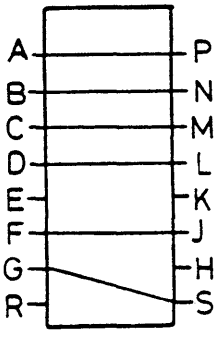
JPRN
D9



JPRN
E3



JPRN
I0

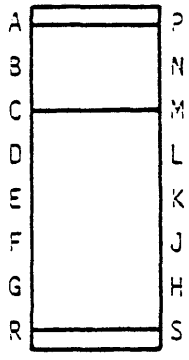


TYPED DRAWING

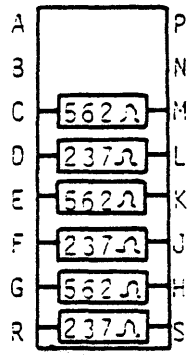
Burroughs Corporation	PAGE 5	DWG. SIZE A-	DWG. NO. 1990 1974	REV A	DSGN CONT PLT NO 011
COMPUTER SYSTEMS GROUP PASADENA, CALIF. 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9		CLASS CODE 40205	
GENERAL QUALITY SPECIFICATION 1183 5343 APPLIES	PREP B.PORTZEL	CHKD. G PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

JUMPER CONFIGURATIONS FOR CARD B9

JPRN
D9



GBNN
K1



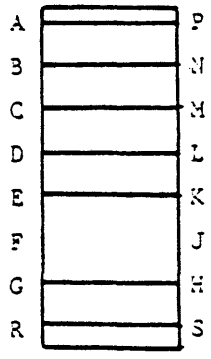
(3) 562 OHM 1/4W RES
P/N 1111 8676
(3) 237 OHM 1/4W RES
P/N 1111 8585

TYPED DRAWING

Burroughs Corporation COMPUTER SYSTEMS GROUP PASADENA, CALIF. 91109 — PASADENA PLANT U.S. AMERICA	PAGE 6	DWG. SIZE A-	DWG. NO. 1990 1974	REV. A	DSGN CONT FLT NO 011
	DOC. TYPE	TITLE: INSTR-JMPR, M/PROC 9		CLASS CODE: 40205	
GENERAL QUALITY SPECIFICATION 1133 5543 APPLIES	PREP. B. PORTZEL	CHKD. G. PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

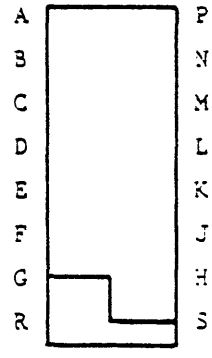
JUMPER CONFIGURATIONS FOR CARD C9

D9



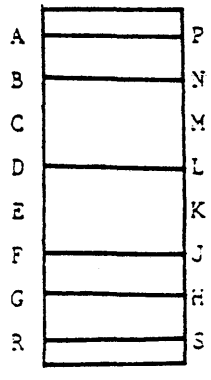
JPRN

E9



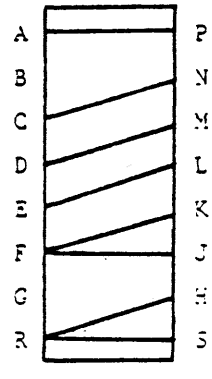
JPRN

J8



JPRN

L2



JPRN

JUMPER CONFIGURATIONS FOR CARD D9

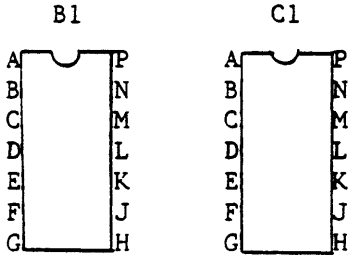
A. S-MEMORY INTERFACE TERMINATION:

NOTE: TERMINATING RESISTORS SHOULD BE INSTALLED ON CARD ASSEMBLIES AT EACH END OF THE S-MEMORY RIBBON CABLES AND REMOVED FROM ALL OTHER ASSEMBLIES CONNECTED TO THE S-BUSES.

THE TERMINATING RESISTORS ARE DIP TYPE RR11, P/N 2228 6777 HAVING A VALUE OF 330/470 OHMS.

FOR THE D9 CARD INSTALL OR REMOVE THE TERMINATIONS AT B1 AND C1 DEPENDING ON THE S-MEMORY CONTROL CABLE CONNECTOR POSITION:

-INSTALL RESISTOR PACKAGES IF THE D9 CARD IS AT END OF CABLE.
-REMOVE RESISTOR PACKAGES IF THE D9 CARD IS NOT AT END OF CABLE.



B. THE PORT NUMBER OF THE PROCESSOR IS AUTOMATICALLY FIGURED OUT BY THE D9 CARD. THERE IS NO NEED TO CHANGE ANY JUMPER ON THE D9 CARD FOR THE PROCESSOR PORT NUMBER.

C. ADJUST THE SYSTEM CLOCK ACCORDING TO THE APPLICABLE SYSTEM TIMING SPECIFICATION.

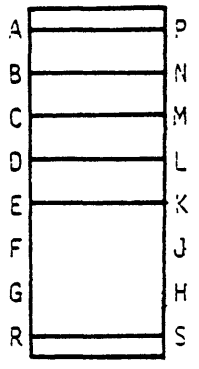
D. FIXED JUMER LOCATIONS A3, D9, AND H4 FORMERLY FOR FIELD CARD TEST, ARE DEFINED ON PAGE *8*.

TYPED DRAWING

Burroughs Corporation	PAGE 8	DWG. SIZE A-	DWG. NO 1990 1974	REV A	DSGN PLT ING CONT 011
COMPUTER SYSTEMS GROUP PASADENA, CALIF. 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9			CLASS CODE 40205
GENERAL QUALITY SPECIFICATION 1183 5543 APPLIES	DRFR B.PORTZEL	CHKD G PAQUET	ENGR.		APPD
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE		DATE

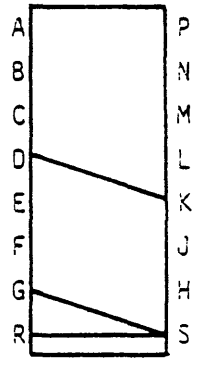
JUMPER CONFIGURATIONS FOR CARD D9

A3 (A6E1)



JPRN

D9 (C4L0)



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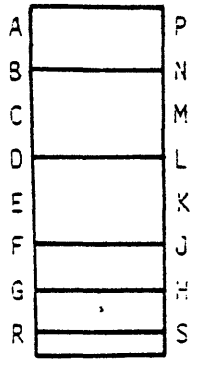

JPRN

TYPED DRAWING

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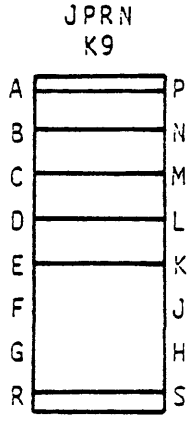
GENERAL QUALITY SPECIFICATION 1183 3543 APPLIES	PREP. B.PORTZEL	CHKD. G PAQUET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

JUMPER CONFIGURATIONS FOR CARD E9



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GENERAL QUALITY SPECIFICATION 1183 5543 APPLIES	PREP. B. PORTZEL	CHKD G. PAQUET	ENGR.	APPD	
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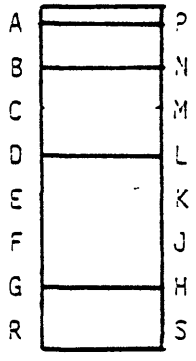
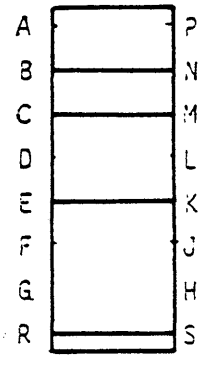
JUMPER CONFIGURATIONS FOR CARD F9

A4



JPRN

F4



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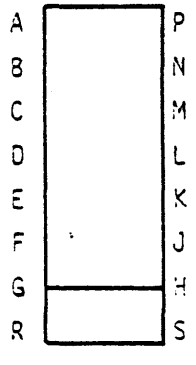

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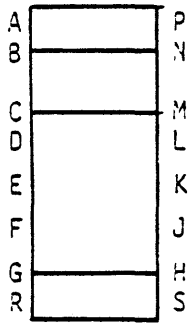
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

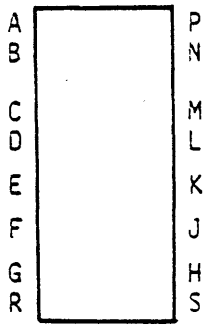
JUMPER CONFIGURATIONS FOR CARD G9

AB



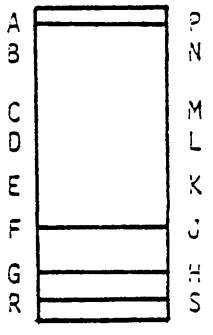
JPRN

F8



JPRN

I7



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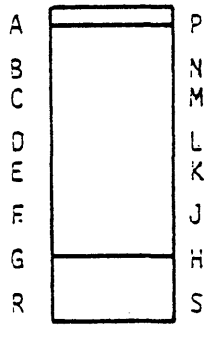
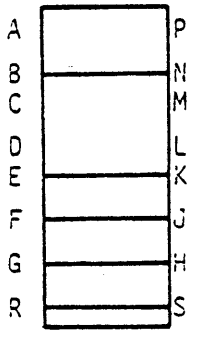
J2



JPRN

K5



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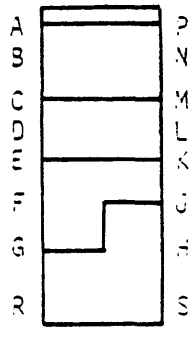
L5



JPRN

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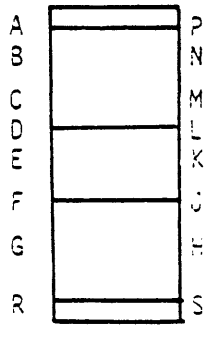

JPRN

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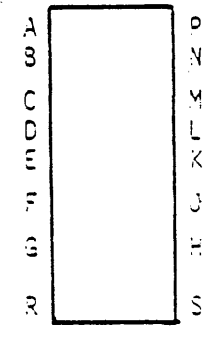


JPRN

JUMPER CONFIGURATIONS FOR CARD H9

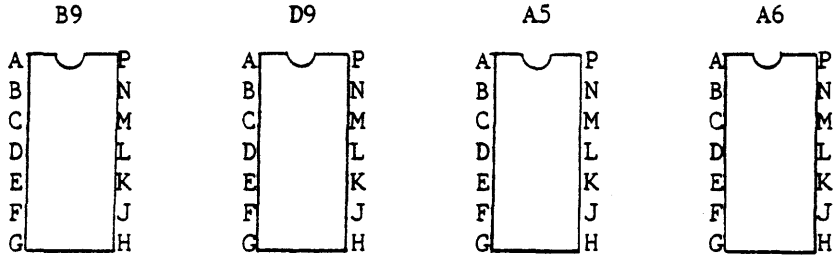
A. I/O BUS TERMINATION:

NOTE: TERMINATING RESISTORS SHOULD BE INSTALLED ON CARD ASSEMBLIES AT EACH END OF THE I/O BUS RIBBON CABLE AND REMOVED FROM ALL OTHER ASSEMBLIES CONNECTED TO THE I/O BUS.

THE TERMINATING RESISTORS ARE DIP TYPE RR12, P/N 2228 6785 HAVING A VALUE OF 240/1.2k OHMS.

FOR THE H9 CARD INSTALL OR REMOVE THE TERMINATIONS AT B9 AND D9 DEPENDING ON THE I/O BUS CABLE CONNECTOR POSITION:

-IF THE H9 CARD IS AT THE END OF THE CABLE, TAKE THE RESISTOR PACKAGES FROM LOCATIONS A5 & A6 AND INSTALL THEM AT B9 & D9.
-IF THE H9 CARD IS NOT AT THE END OF THE CABLE, TAKE THE RESISTOR PACKAGES FROM LOCATIONS B9 & D9 AND INSTALL THEM AT A5 & A6.



B. ADJUST THE SYSTEM CLOCK ACCORDING TO THE APPLICABLE SYSTEM TIMING SPECIFICATION.

C. IF THE H9 CARD IS INSTALLED IN AN A PROCESSOR, THE FIXED CONFIGURATION JUMPERS AT LOCATIONS A2, B0, F7, L2A, J1 AND K3 ARE DEFINED ON PAGE 13. IF THE H9 CARD IS INSTALLED IN THE B PROCESSOR, THE FIXED CONFIGURATION JUMPERS AT THE SAME LOCATIONS ARE DEFINED ON PAGE 14.

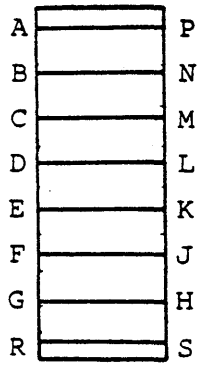
TYPED DRAWING

Burroughs Corporation	PAGE 13	DWG SIZE A-	DWG NO 1990 1974	REV A	DSGN CONT PLT NO 011
COMPUTER SYSTEMS GROUP PASADENA, CALIF 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE INSTR-JMPR,M/PROC 9		CLASS CODE 40205	
GENERAL QUALITY SPECIFICATION 1132 5543 APPLIES	PREP B.PORTZEL	CHKD G PAIVET	ENGR.	APPD	
PROPRIETARY TO BURROUGHS CORPORATION. NOT TO BE REPRODUCED OR USED FOR MANUFACTURING PURPOSES, EXCEPT ON BURROUGHS ORDER OR PRIOR WRITTEN CONSENT.	DATE 2/24/83	DATE 3/07/83	DATE	DATE	

JUMPER CONFIGURATIONS FOR CARD H9

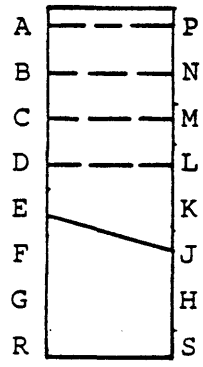
FIXED CONFIGURATION JUMPER CHIPS SHOULD BE INSTALLED AT THE FOLLOWING LOCATIONS ON CARD H9 OF THE A PROCESSOR:

A2



JPRN

80*



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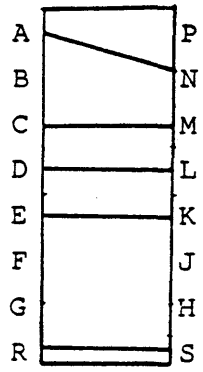
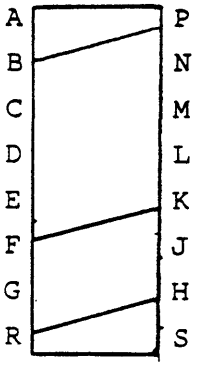


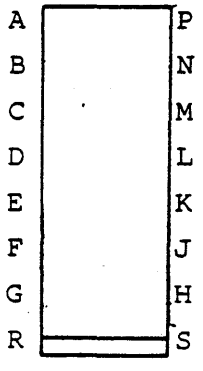
JPRN

J1



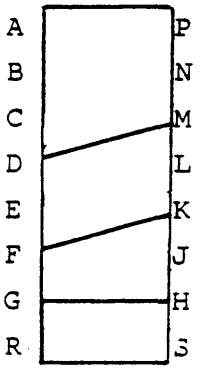
JPRN

K3



JPRN

L2A



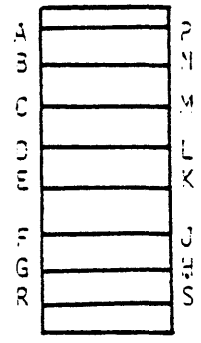
JPRN

*DASHED LINE CONNECTIONS ARE INSTALLED WHEN THIS CARD IS AT THE END OF THE I/O CABLE DAISY CHAIN

JUMPER CONFIGURATIONS FOR CARD H9

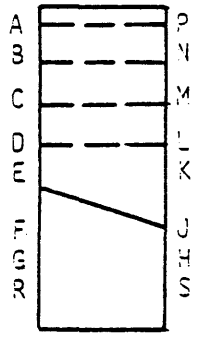
FIXED CONFIGURATION JUMPER CHIPS SHOULD BE INSTALLED AT THE FOLLOWING LOCATIONS ON CARD H9 OF THE B PROCESSOR:

A2



JPRN

B0 *



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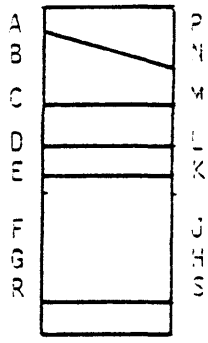
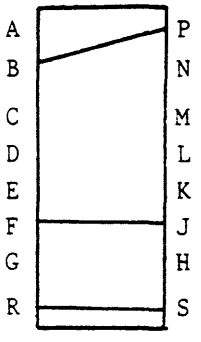


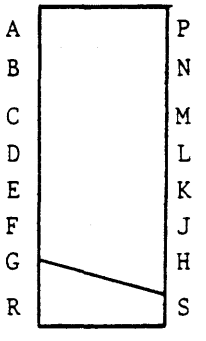
JPRN

J1



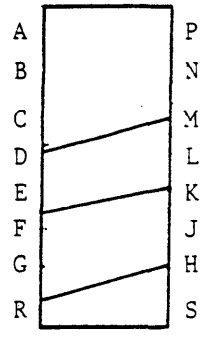
JPRN

K3



JPRN

L2A



JPRN

* DASHED LINE CONNECTIONS ARE INSTALLED WHEN THIS CARD IS AT THE END OF THE I/O CABLE DAISY CHAIN.

COVER SHEET TO BE ADDED TO CLOCK ALIGNMENT 2233 3686 REV. D.
****

Pages 11, 15, 25 of this document have changed by RIN 7651-009. All other pages are unchanged: they are the same as rev. E.

Clock alignment document is now rev. E.

Printed in U.S. America

CHANGE SHEET

Burroughs Corporation	PAGE 1 OF 26	DWG. SIZE A-	DOC. NO. 2233 3686	REV./ISS. D	DSGN. CONT PLT. NO. 011
COMPUTER SYSTEMS GROUP PASADENA, CALIFORNIA 91109 — PASADENA PLANT U.S. AMERICA	DOC. TYPE	TITLE M-PROCESSOR-9 CLOCK ALIGNMENT		CLASS CODE	

REV. OR ISSUE	CONTROL DOC. & NUMBER	PREP.	CHKD.	APPD. & DATE	PAGE	LINE OR PARA.	REVISION DESCRIPTION
A	ECN 46283						Initial Issue
B	ECN 48204	LS LS 4/5/83	SC SC 4/8/83	RH RH ME 4/15/83			Updated Sections 3 through 7 per REE 91203 and REE 90053. Sections 5, 5.1, 5.3 through 5.7, 6.2 and 6.3 were updated per REE 91313.
C	ECN 20007A						TO INCORPORE EDA 90780: CHANGE XC7R WAS XB7R CHANGE XC4Z WAS XL4W TO INPROVE QUALITY OF DRAWING
D	ECN 20038A						UPDATED SECTIONS 5-6 AND 5-7 PER REE 93464 CORRECT PIN LOCATION ERROR REE 24052

PAS 1668 REV 12-74

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3	Processor Adjustment Theory	PAGE	6
4	Preliminary Set-Up.	PAGE	7
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5.1	I/O Clock Delay Adjustment Processor (Backplane).	PAGE	9
5.2	I/O Clock Width Adjustment Processor (Backplane).	PAGE	10
5.3	Pad/Cache/Stack Clock Delay Adjustment.	PAGE	11
5.4	Memory Clock Alignment.	PAGE	12
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5.6	Sub-Distribution Delay Adjustment	PAGE	14
5.7	Sub-Distribution Clock Width Adjustment	PAGE	17
5.8	Disk Subsystem Clock Adjustment	PAGE	18
6	Dual Processor Clock Generation	PAGE	20
6.1	'B' Processor System Clock Width Adjustment	PAGE	22
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6.3	'B' Processor Pad, Stack And Cache Clock Adjustment	PAGE	25
7	Nominal Settings.	PAGE	26

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1 INTRODUCTION

The GEM processor's clock distribution system has been designed to minimize the requirements for clock width and delay adjustment. The B1905/B1955 clock generation system employed single clock lines for each destination card, and separate delay adjustments for each of these lines. GEM employs a shared clock signal among several cards. This technique allows for a major reduction in adjustment requirements, while maintaining the same timing margins.

Nominal configuration for the GEM is one Multiline-4, one MBU-9, and one MP-9, and one DSC-2. The Multiline and MBU clocks are available via coaxial connectors located on the frontplane, and adjustment is accomplished on the respective control. The processor requires width adjustment of its system clock, delay adjustment of the scratchpad/cache clock, and delay and width adjustment of the backplane clock. Thus in nominal configuration, there are a total of six adjustments required.

Dual processor configurations require additional adjustments. In addition to the adjustments required for the nominal configuration, there are several adjustments required to synchronize the 'A' and 'B' processors. The 'A' processor supplies two early clocks to the 'B' processor. These are an early processor, and an early scratchpad/cache clock. A delay adjustment for the early processor clock is available in the 'A' processor. In the 'B' processor, the processor clock width and delay must be adjusted, as well as the delay of the scratchpad/cache clock delay to coincide with the active edge of the 'A' processor.

The I/O sub-distribution base, Multiline, and Memory Base units all receive their clocks via coaxial connections. Memory and the Multiline employ a 50% duty cycle clock at 6 MHz, the I/O sub-distribution system uses a 41 ns pulse width clock at 6 MHz. The relationship between the active edge of the processor clock and the respective base is adjustable on the base card.

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2 CLOCK SYSTEM SCHEMATICS

Figure 1 illustrates a schematic representation of the GEM clock generation logic.

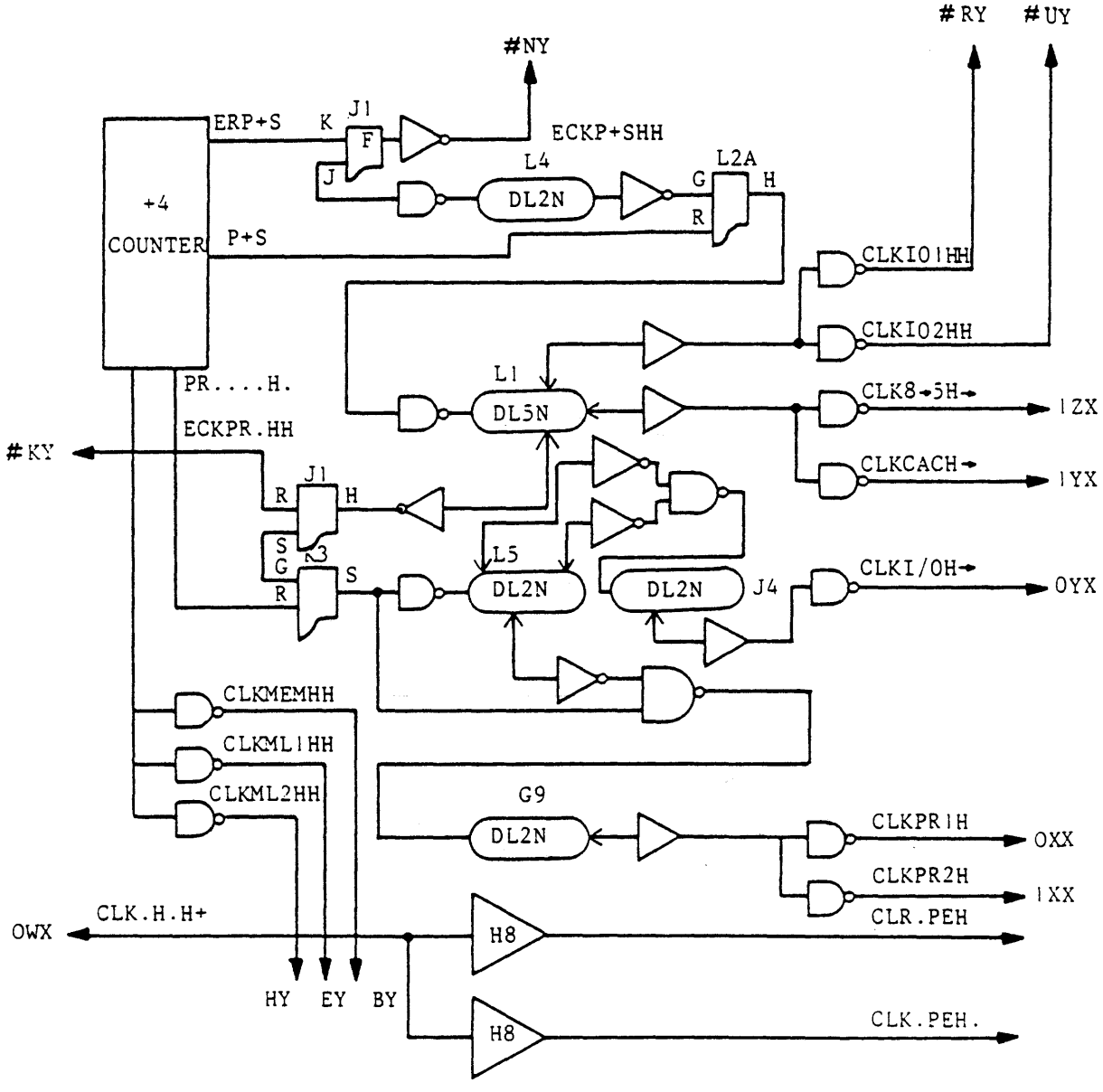

FIGURE 1

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H9 CARD COAX-CABLE CONNECTION

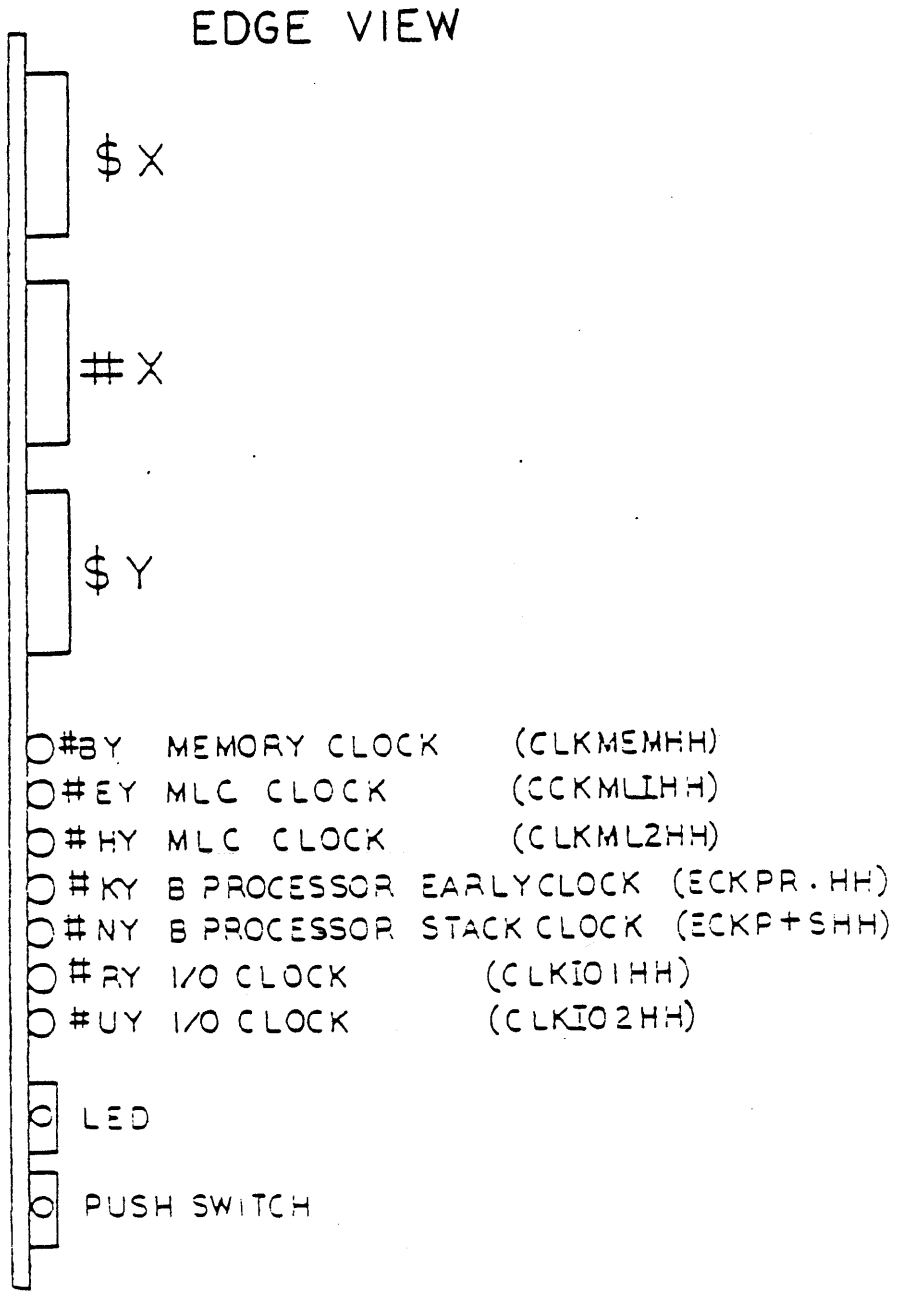

FIGURE 2

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3 PROCESSOR ADJUSTMENT THEORY

The 24 MHz is divided down by 4 to yield a 6 MHz clock with a 41 ns pulse width. This signal is available in four phases, three of which are used. The second count phase of the divide-by-four counter is used to generate the early pad/stack/cache clock (ERP+S.H.). Counter phase 3 is used for two sets of signals, the early processor clock and the normal pad/stack/cache clock. The fourth phase of the clock is used for generation of the I/O clock and processor clock. The processor clock has a width control adjustment which allows it to be narrowed to a nominal 20 ns pulse width. All of the backplane clocks are delay-adjustable.

The pad/stack/cache clock is set so that it occurs before the system clock. These clocks are used as gated write pulses to the cache, A-stack and scratchpad memory devices. Adjustment of the delay on one clock will adjust both signals.

The I/O clocks may be divided into the clocks available on the frontplane via coaxial connectors, and the I/O clock which is sent to the I/O controls resident in the 18 card processor backplane. The I/O clock present on the backplane is the only one of these clocks which is adjustable on the H9 card. The other two clocks must be adjusted on the respective sub-distribution cards. All of the I/O clocks must be adjusted to be coincident with the processor clock. The backplane I/O clock, CLKI/OH+, is generated by the same phase of the clock as the processor clock. Frontplane I/O clocks are generated in the same phase as the pad/stack/cache clock signal, and are essentially early clocks. This is done to account for variable length coaxial cables, and varying delays on the respective sub-distribution cards.

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4 PRELIMINARY SET-UP

1. Verify that all system voltages are set to nominal.

2. Use a calibrated scope which is able to display five nanoseconds per centimeter.

3. Use two identical probes (type and length) with short ground leads connected to DC ground on a backplane pin near the clock pin.

4. Verify the probes and scope preamp by attaching the probes to the same backplane pin (e.g., use Backplane Pin XC4X on card H9). Channel A & B signals should be within 1 ns and show no significant difference in waveform shape or amplitude.

   Notes: a. Make all measurements at the +1.5 volt level.

   b. Unless otherwise specified, the system should be in halt state.

   c. As a point of reference, the nominal delays are shown.

   d. Diagrams are not drawn to scale.

   e. Trigger on channel 1.

   f. Set scope for 'AUTO' mode.

   g. Logic cards should not be extended.

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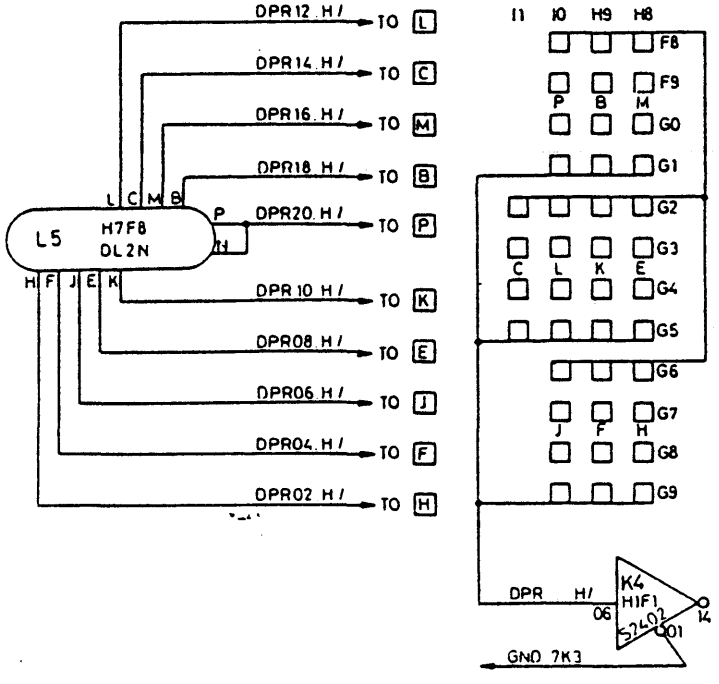
5 SYSTEM CLOCK WIDTH ADJUSTMENT

With H9 card inserted, place channel 1 probe on CLK.H.H+ (Backplane Pin XC3W) of card H9. The nominal width of this signal measured at 1.5 volts should be 20 ns +/- 2.5 ns. (See figure below.)

Width of signal CLK.H.H+

This adjustment can be made by moving delay line taps as shown below. If the delay is increased, the pulse width gets shorter. If the delay is decreased, the pulse gets wider.

Example: Assume initial setting at tap 'K' and pulse is measured as being 25 ns. This implies that the delay must be increased to decrease the pulse width. Either adding 4 ns, or 6 ns will place the width within the allowed margin. Therefore, the tap may be moved to 'C' or 'M' to accomplish the required adjustment.



Adjustment located on H9 card. Connect appropriate delay line across to taps available in rows G1, G5 or G9.

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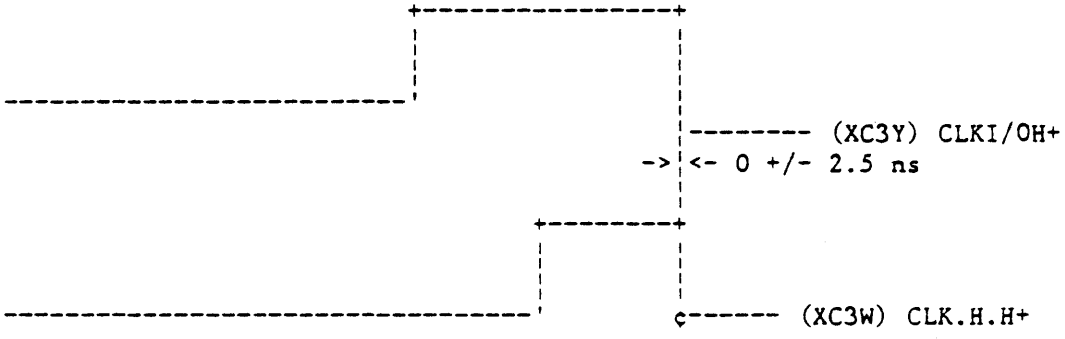
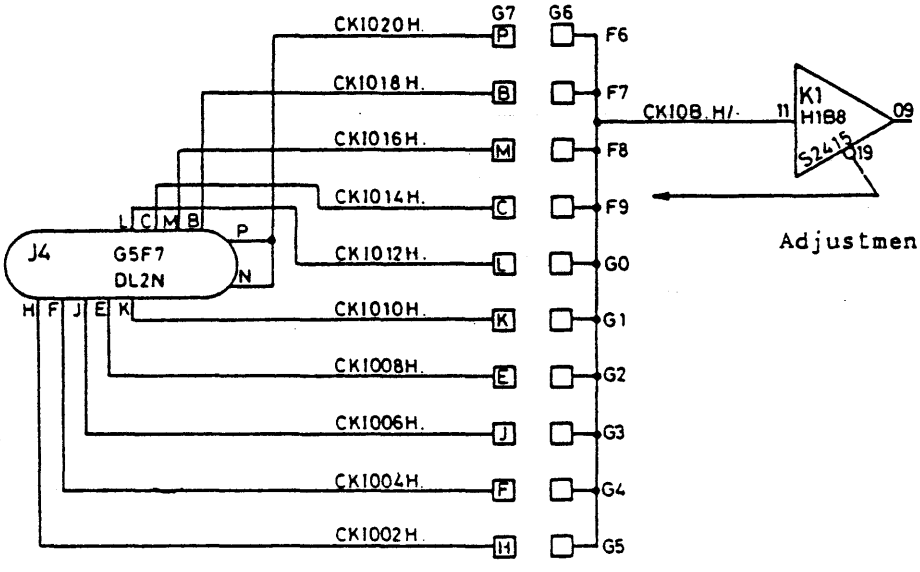
5.1 I/O CLOCK DELAY ADJUSTMENT PROCESSOR (BACKPLANE)

With H9 card inserted, place channel 1 probe on the processor clock CLK.H.H+ at XC3W and place channel 2 probe on the backplane I/O clock CLKI/OH+ at XC3Y. Adjust the delay to within 2.5 ns of the falling edge of the processor clock. (See figure below.)



Example: Assume that the delay line tap is on 'L' and the I/O clock edge occurs 6 ns after the processor clock. For a nominal adjustment 6 ns should be removed from the delay path. This is accomplished by moving the tap from 'L' to 'J'. The possible delay positions are shown below.



Adjustment on H9 card.

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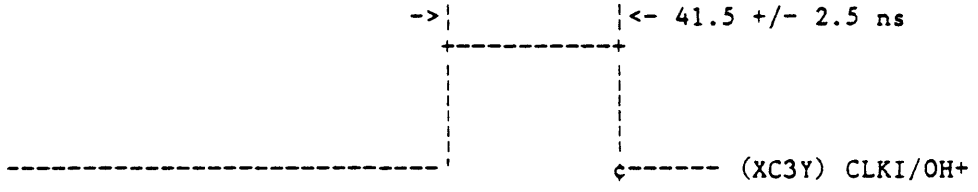
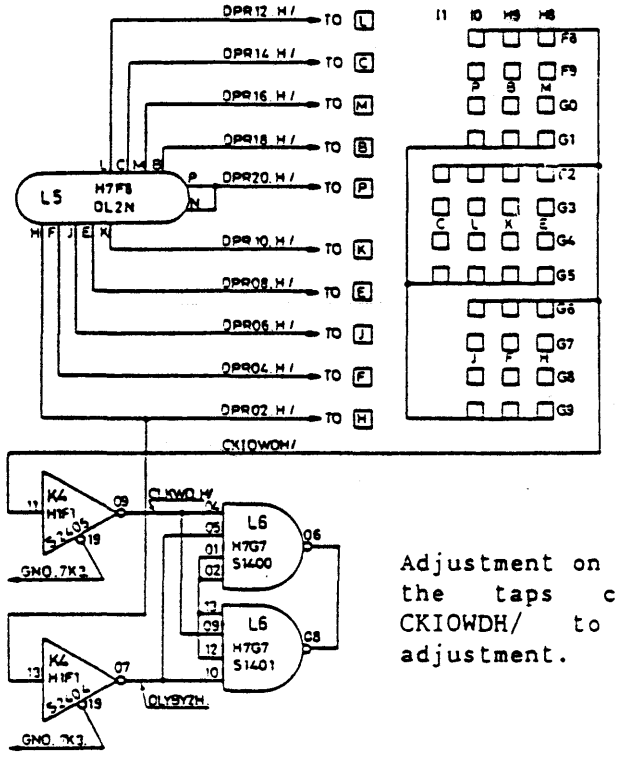
5.2 I/O CLOCK WIDTH ADJUSTMENT PROCESSOR (BACKPLANE)

With the H9 card inserted, place channel 2 probe on the backplane clock CLKI/OH+ at XC3Y. Adjust the width of this signal to 41.5 ns +/- 2.5 ns. (See figure below.)



Example: Assume that the width is 47 ns, and the tap is on pin 'H'. A 6 ns change is required, and this may be accomplished by changing the tap from 'H' to 'E'. To decrease the width, the delay is increased.



Adjustment on H9 card. Use the taps connected to CKIOWDH/ to make the adjustment.

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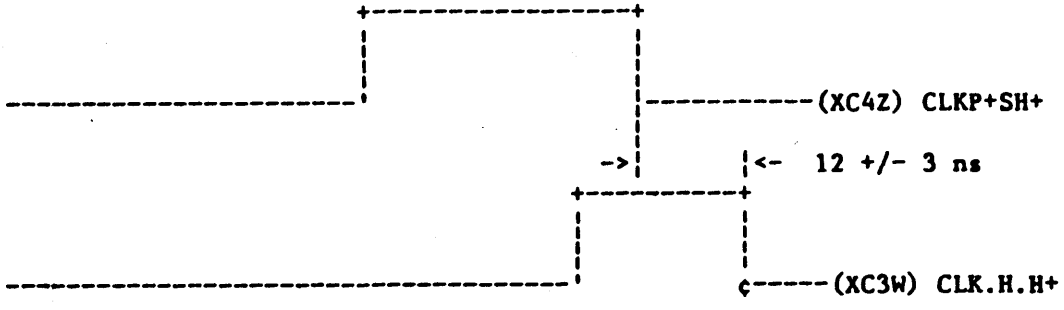
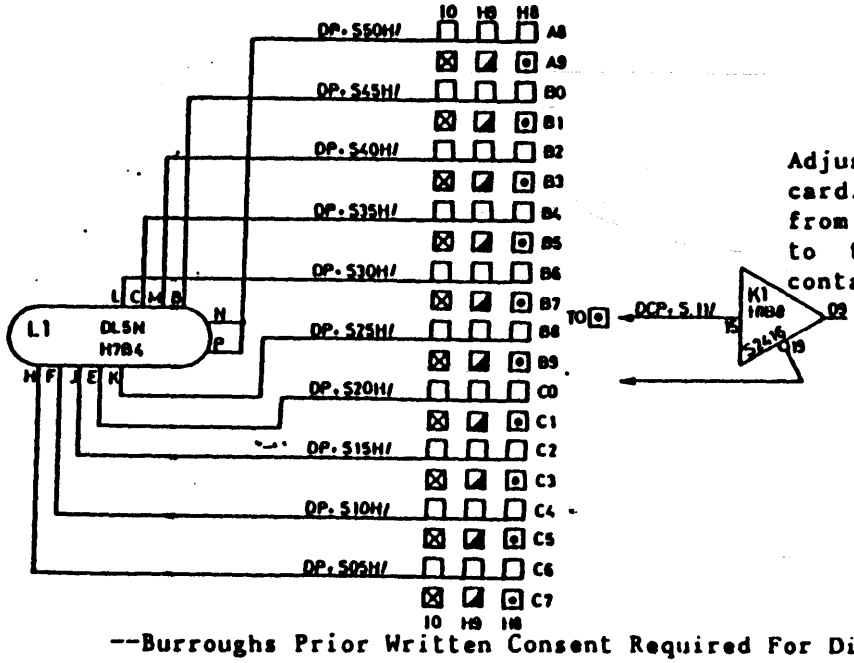
5.3 PAD/CACHE/STACK CLOCK DELAY ADJUSTMENT

With the H9 card inserted, place channel 1 probe on XC3W for signal CLK.H.H+, and channel 2 probe on XC4Z for signal CLKP+SH+. Adjust the falling edge of CLKP+SH+ to be 12 ns +/- 3 ns before falling edge of CLK.H.H+. This relation is shown below.



Example: Assume that the tap is on 'K' and CLKP+SH+ is 20 ns ahead of CLK.H.H+. 8 ns of delay should be removed for a nominal setting, but only 5 ns increments are available. If 10 ns of delay is removed, CLKP+SH+ would be 10 ns ahead of CLK.H.H+. This is within tolerance, thus the tap should be moved from 'K' to 'C'.



Adjustment located on H9 card. Use column H8 taps from delay line to connect to taps indicated by dot contained within box.

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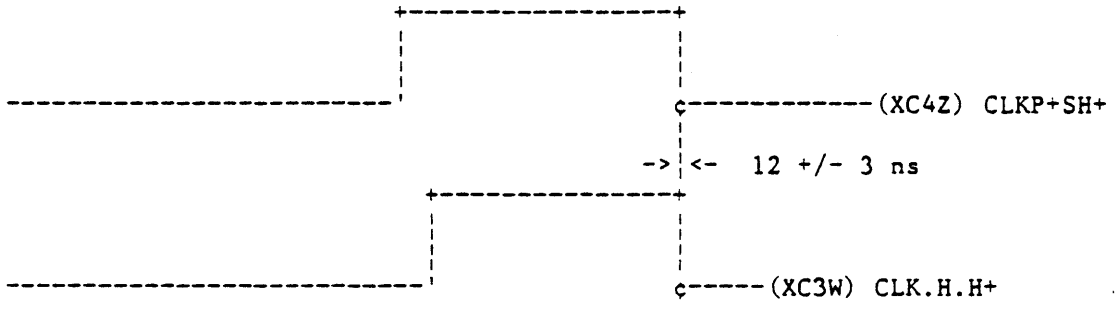
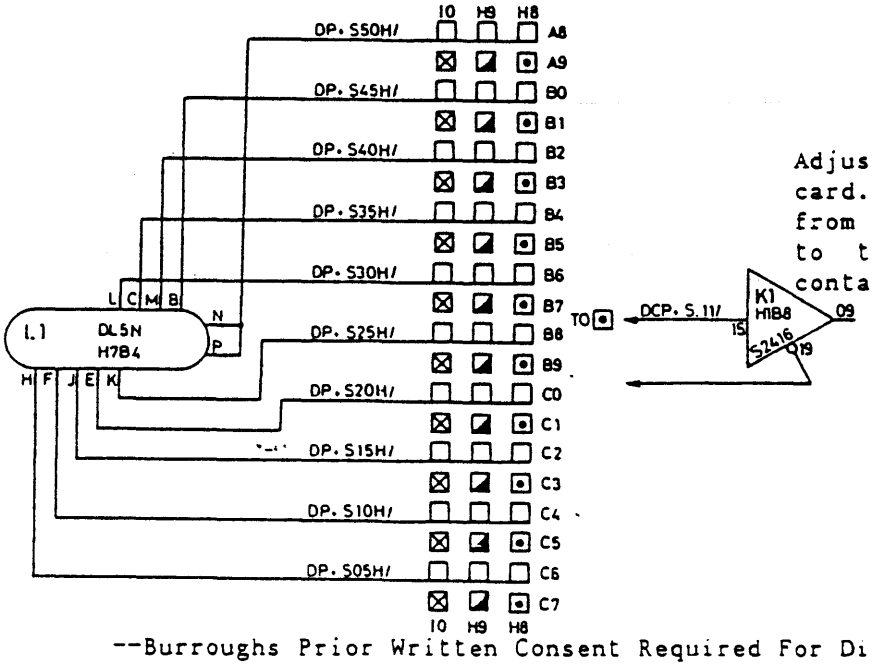
5.3 PAD/CACHE/STACK CLOCK DELAY ADJUSTMENT

With the H9 card inserted, place channel 1 probe on XC3W for signal CLK.H.H+, and channel 2 probe on XC4Z for signal CLKP+SH+. Adjust the falling edge of CLKP+SH+ to be 12 ns +/- 3 ns before falling edge of CLKPR2H+. This relation is shown below.



Example: Assume that the tap is on 'K' and CLKP+SH+ is 20 ns ahead of CLKPR2H+. 8 ns of delay should be removed for a nominal setting, but only 5 ns increments are available. If 10 ns of delay is removed, CLKP+SH+ would be 10 ns ahead of CLKPR2H+. This is within tolerance, thus the tap should be moved from 'K' to 'C'.



Adjustment located on H9 card. Use column H8 taps from delay line to connect to taps indicated by dot contained within box.

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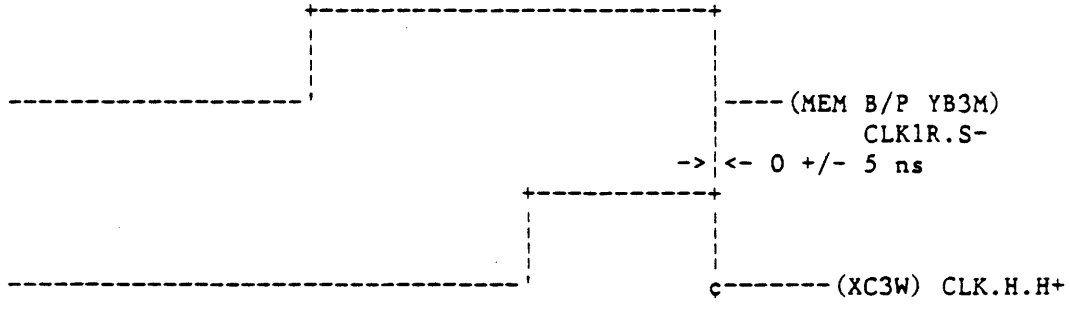
5.4 MEMORY CLOCK ALIGNMENT

With all cards inserted, and S9 card coax cable plugged in, place channel 1 probe on the processor clock CLK.H.H+ at XC3W of card H9. Place the channel 2 probe on the MBU backplane clock CLK1R.S- at YB3M of card S9. Adjust the delay of the MBU clock to within 5 ns of the falling edge of the processor clock. EARLYC must always have 20 ns less delay than ICLK1. (See figure below.)



Example: Assume that the JPRN at K7 on the S9 card is configured nominally. (See figure below.) If the MBU clock occurs 13 ns after the processor clock, decrease the amount of delay to both clocks by 10 ns. ICLK1 should be connected to DLY50 and EARLYC should be connected to DLY30.

Location K7

DLY60	A	P	
DLY70	B	N	
DLY80	C	M	ICLK1
DLY90	D	L	
DLY100	E	K	DLY10
DLY50	F	J	DLY20
DLY40	G	H	DLY30
DLY00	R	S	EARLYC

Nominal Setting for Memory Base

(Adjustment on card S9)

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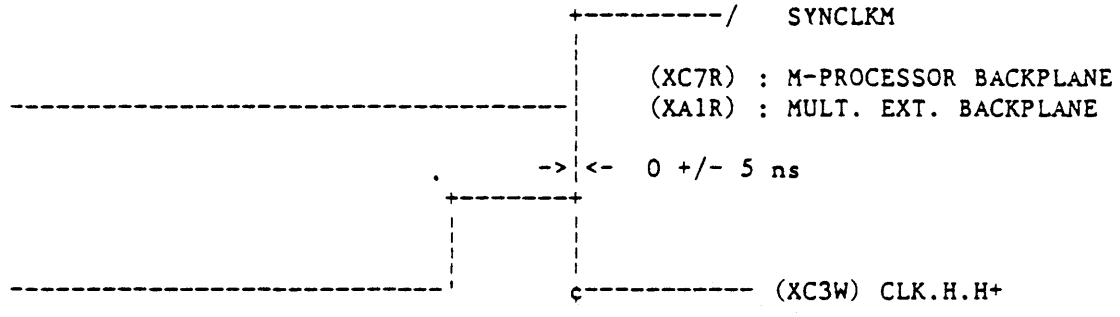
5.5 MULTILINE CLOCK ALIGNMENT

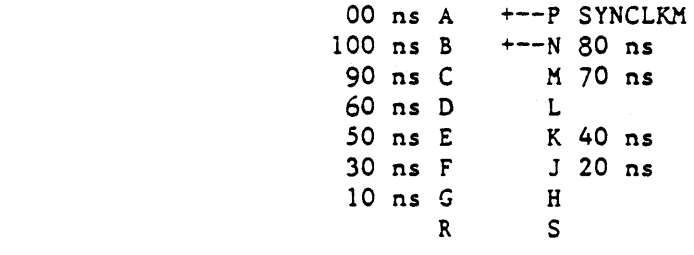
With all cards inserted, place channel 1 probe on the processor clock CLK.H.H+ at XC3W of card H9. Place the channel 2 probe on MLC backplane clock SYNCLKM- at XC7R of the MLC-4 control. Set the MLC clock to within 5 ns of the falling edge of the processor clock. 'Use the rising edge of the MLC clock.' (See figure below.)

Note: This alignment is applicable for both MLC in main cabinet and in expansion cabinets.



Example: Assume that the MLC is at a nominal setting as shown in figure below with a tap at the 80 ns delay position. The rising edge of SYNCLKM- is observed to be 13 ns ahead of the falling edge of CLK.H.H+. 10 ns of delay must be added. Move the tap from 'N' (80 ns delay) tap 'C' (90 ns delay). (See following figures.)

Location L0



MLC-4 Nominal Setting

(Adjustment on MLC card)

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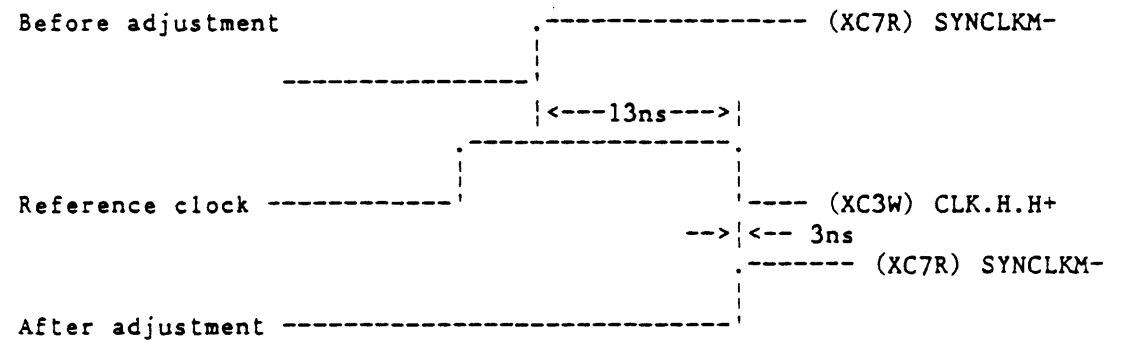
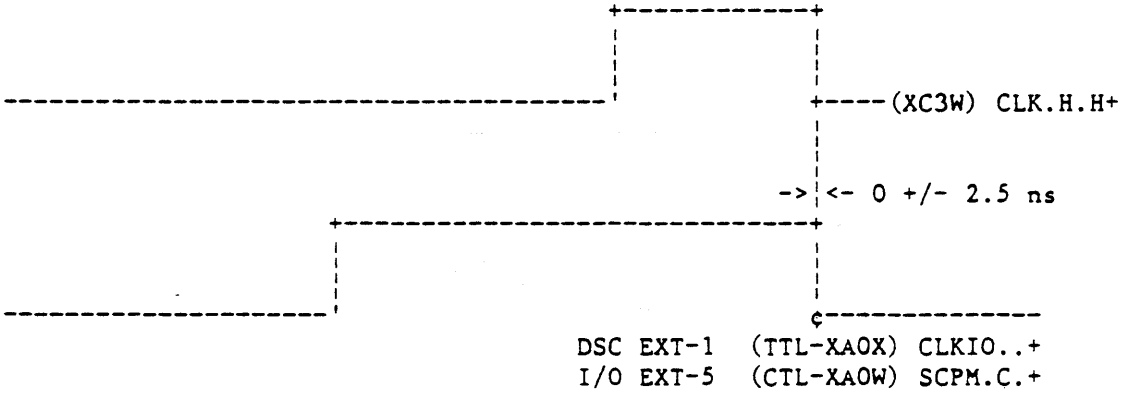
5.5 MULTILINE CLOCK ALIGNMENT (Continued)



5.6 SUB-DISTRIBUTION DELAY ADJUSTMENT

With the card inserted, place channel 1 probe on the processor clock CLK.H.H+ on XC3W of the A Processor H9 card. Place channel 2 probe on the backplane of the I/O sub-distribution card at clock CLKIO..+ on pin XA0X for DSC extension or at clock SCPM.C+ on pin XA0W for CTL controls. Adjust the delay to within 0 ns +/- 2.5 ns. Move wire on F5R for delay adjustment. (See figure below.)



Example: Assume the F5R tap is on 'F' and CLKIO..+ is 4 ns later than CLK.H.H+. 4 ns of delay must be removed for a proper delay adjustment. To accomplish this, the delay F5R tap must be moved from 'E' to 'F' to remove 4 ns of delay and put this adjustment within tolerances.

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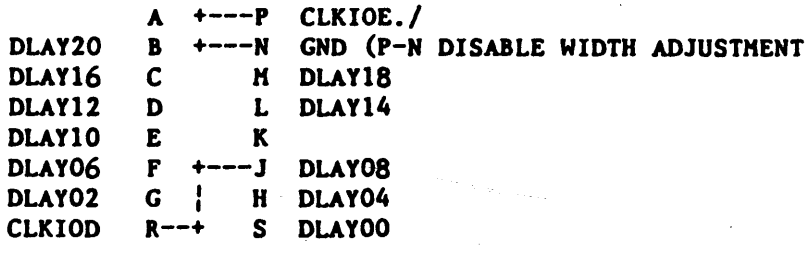
5.6 SUB-DISTRIBUTION DELAY ADJUSTMENT (Continued)

Note: (1) If the delay adjustment cannot be made, the delay adjustment for CLKIOnHH on the H9 should be changed. To make adjustment for CLKIOnHH, use column H9, and connect to the appropriate delay line tap (see diagram next page).

(2) The F5P tap must always be connected to F5N.

LOCATION F5



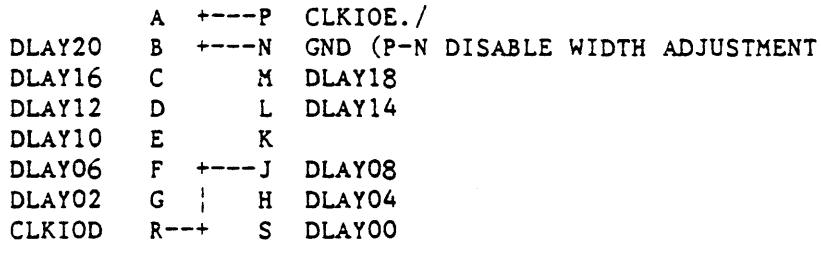
(Adjustment on Sub-Distribution Card)

5.6 SUB-DISTRIBUTION DELAY ADJUSTMENT (Continued)

Note: (1) If the delay adjustment cannot be made, the delay adjustment for CLKIOnHH on the H9 should be changed. To make adjustment for CLKIOnHH, use column H9, and connect to the appropriate delay line tap (see diagram next page).

(2) The F5P tap must always be connected to F5R.

LOCATION F5



(Adjustment on Sub-Distribution Card)

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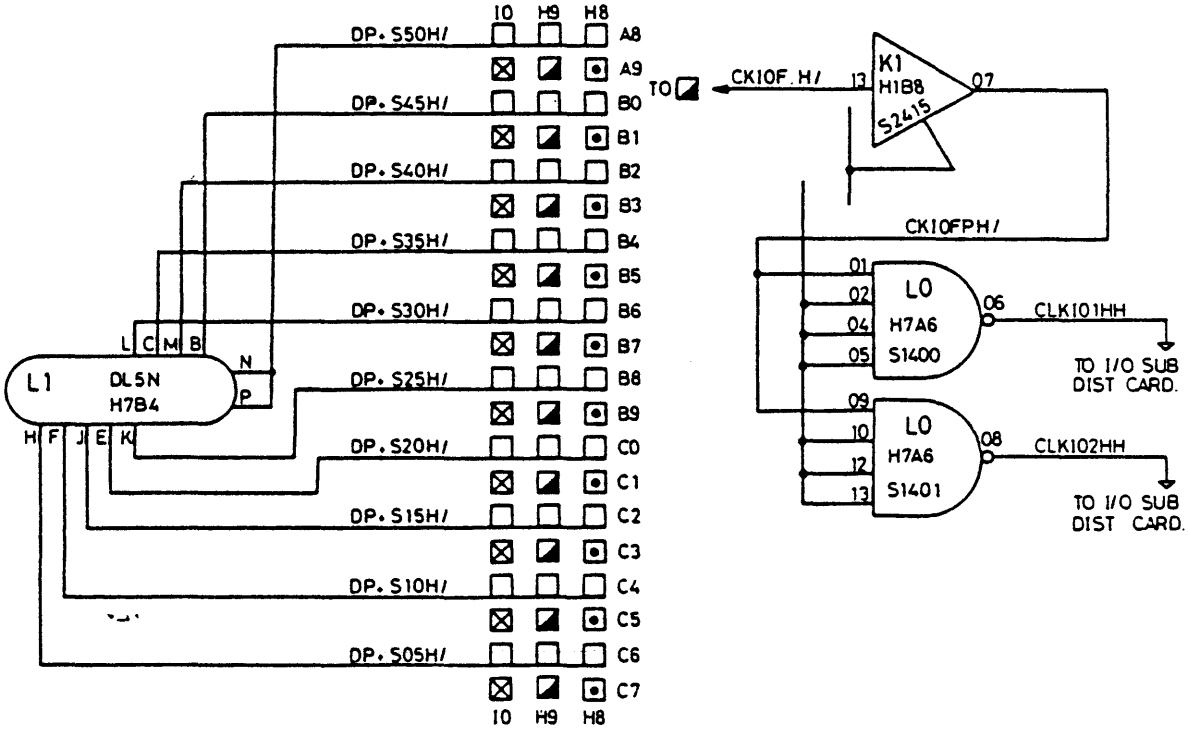

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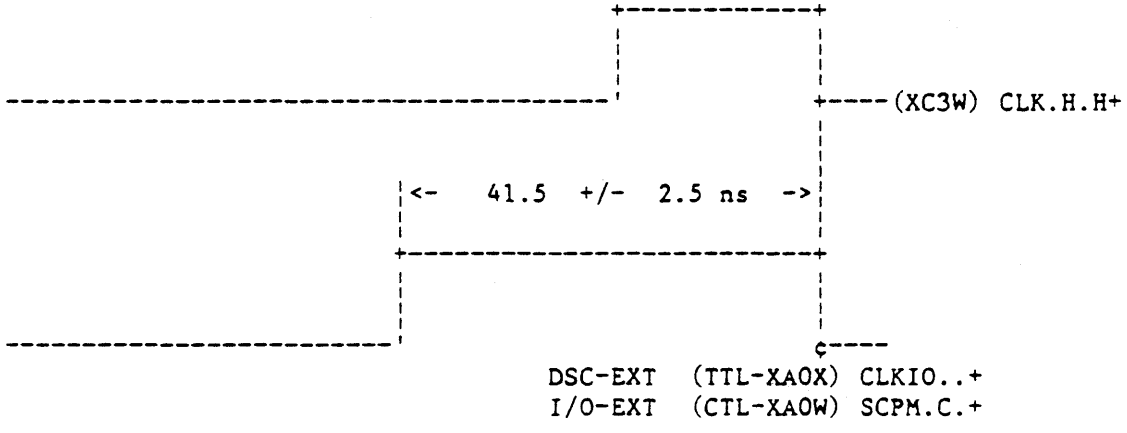
5.7 SUB-DISTRIBUTION CLOCK WIDTH CONTROL

With the card inserted, place channel 1 probe on the processor clock CLK.H.H+ on XC3W of the H9 card. Place channel 2 probe on the backplane of the I/O sub-distribution card at clock CLKIO..+ on pin XA0X for DSC EXT or at clock SCPM.C.+ on pin XA0W for CTL controls. Control the pulse width of the clock to be 41.5 +/- 2.5 ns.



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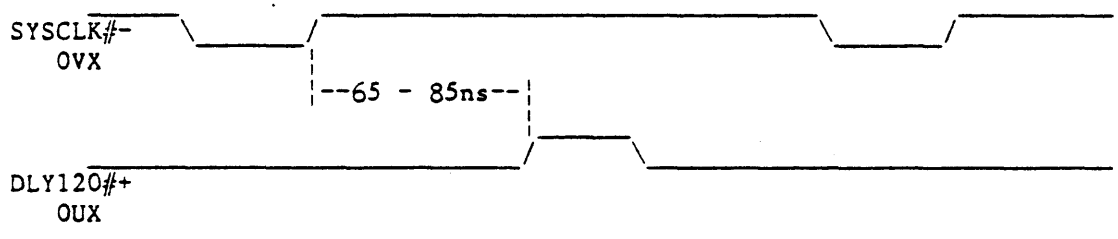
5.8 DISK SUBSYSTEM CLOCK ADJUSTMENT

The delay line at location E8 (DLCN) and the eight surrounding sets of push-on jumpers are used to adjust the delay of the write enable pulse for the RAMS on Card 1.

Adjustment is achieved by monitoring pins XE3V (XA3V for DSC extension) (SYSCLK#-) and XE3U (XA3U for DSC extension) (DLY120#+) on the backplane. With an oscilloscope connected to these two points, the observed waveform should be similar to that shown below. The objective is to make the positive edge of DLY120#+ trail the positive edge of SYSCLK#- by 65 to 85 ns.



If the required delay is not observed, determine in multiples of 10 ns how much it is off and consult the picture below. The eight different taps are shown as they reside on the card. The delay of each one is noted. These values should not be confused with the actual delay of the DLY120#+ signal, they are only for reference. Move the jumper to the appropriate delay tap. As an example, assume that you observe a delay of 95 ns. You need to decrease the delay by 20 ns to conform to the timing specification. If the tap currently selected is 'C', then you would move the pushpin to the 'K' tap.

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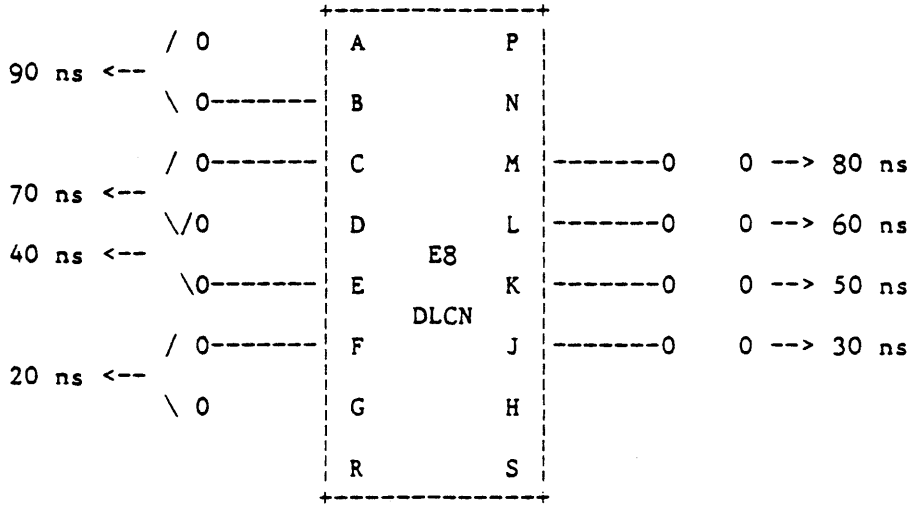
5.8 DISK SUBSYSTEM CLOCK ADJUSTMENT (Continued)



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6 DUAL PROCESSOR CLOCK GENERATION

The 'A' and 'B' processors are slaved together via two early clocks called ECKP+SHH and ECKPRHH. The ECKP+SHH signal is delayed to become the pad, stack, and cache clocks on the 'B' processor. The ECKPR.HH signal is delayed to become the 'B' processor system clocks CLKPR1H+ and CLKPR2H+. The ECKPRHH signal has delay adjustments available on the 'B' processor. Clock ECKPR.HH may be delayed by up to 50 ns on the 'A' processor, and 20 ns on the 'B' processor.

To align a dual processor, the procedures for the 'A' processor is identical to those already presented with the exception of the change of jumper chips necessary to present early clocks at the frontplane coax connectors. This jumper connection is shown on the next page. Note that the nominal delay of the signal ECKPR.HH should be such that it will not be necessary to adjust delay on the 'A' processor, but this delay is available.

Adjustment of the 'B' processor begins with alignment of the processor pulse width. The next adjustment is the processor delay to coincide with the 'A' processor's system clock. Aligning the cache, pad, and stack clocks should be done with respect to the 'B' processor's system clock which necessitates the movement of the scope probes. This final adjustment is done in the same manner as the 'A' processor. Any external subsystem alignment should be done before this last adjustment. These external subsystems are all aligned with respect to the 'A' processor system clock.

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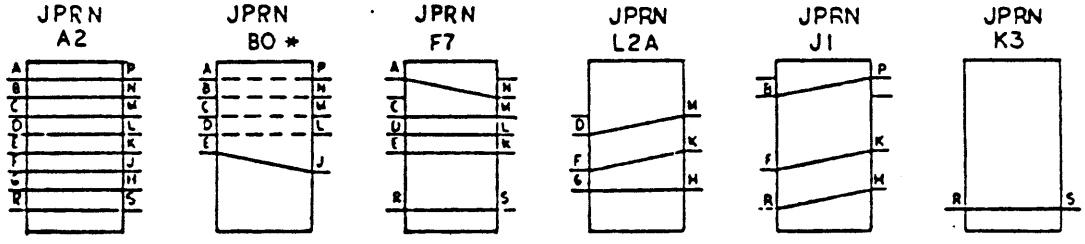
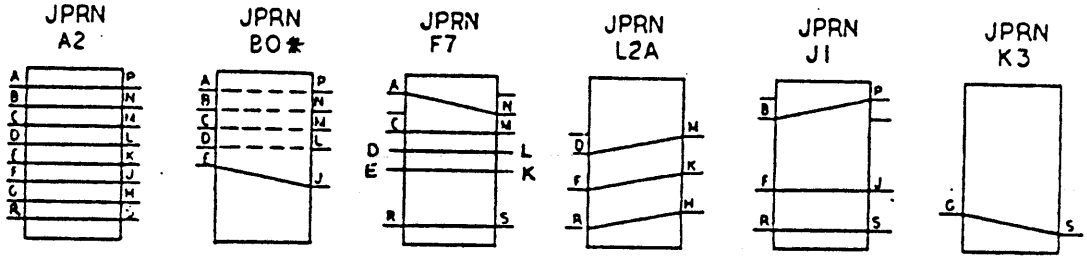


A PROCESSOR



B PROCESSOR

* Connection should be made for the dash lines if the H9 card is at the end of the I/O bus.

JUMPER CONFIGURATIONS FOR DUAL PROCESSORS

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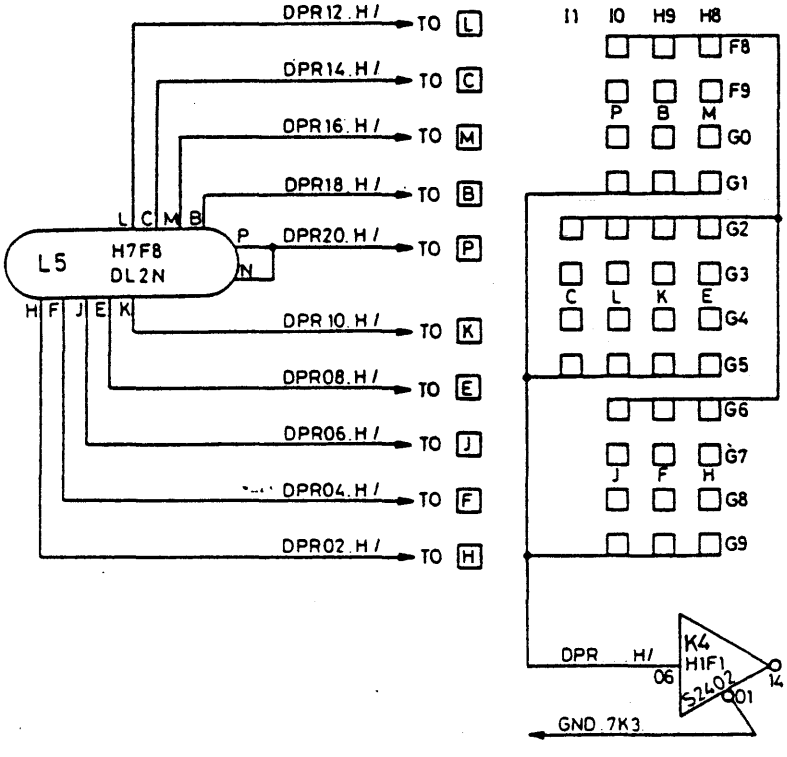
6.1 'B' PROCESSOR SYSTEM CLOCK WIDTH ADJUSTMENT

With card inserted, place channel 1 probe on pin XC3W of 'B' processor card H9. The nominal width of this signal is 20 +/- 2.5 ns. (See figure below.)

This adjustment can be made by moving delay line taps as shown below. If the delay is increased, the pulse width gets shorter. If the delay is decreased, the pulse will get longer.

Example: Assume initial setting at tap 'K' and the pulse is measured as being 25 ns. This implies that the delay must be increased to decrease the pulse width. Either adding 4 ns or 6 ns will place the width within the allowed margin. Therefore, the tap may be moved to the 'C' or 'M' taps to accomplish the required adjustment.



Adjustment located on H9 card. Connect the appropriate delay line tap across to taps located in rows G1, G5 or G9.

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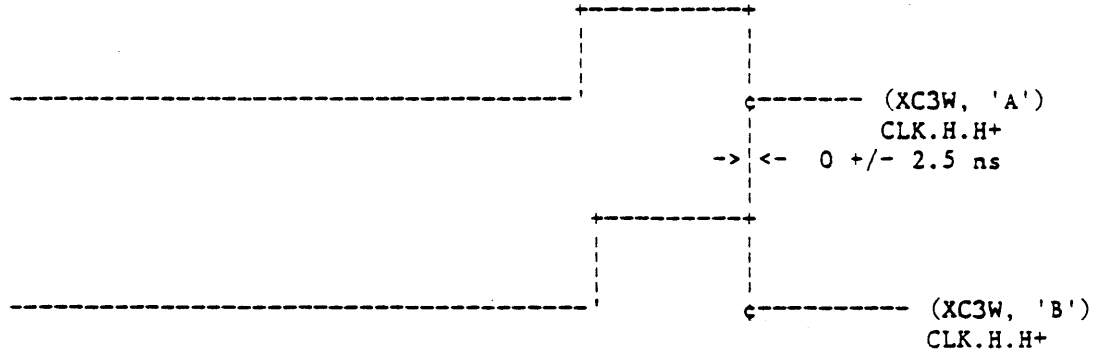
6.2 'B' PROCESSOR SYSTEM CLOCK DELAY ADJUSTMENT

With the H9 cards inserted, place channel 1 probe on XC3W of card H9 in processor 'A'. Place the channel 2 probe on pin XC3W of card H9 in the 'B' processor. The delay of the 'B' processor's system clock must be adjusted to cause the falling edge to be within 0 +/- 2.5 ns of the falling edge of the 'A' processor system clock. This relationship is illustrated below.



Example: Assume 'B' processor clock is measured to be 33 ns ahead of the 'A' processor system clock. Assume further that the signal ECKPR.H/ is connected to tap 'J' of delay line at L1 on the 'A' processor, and signal DCPR..H/ is connected to tap 'K' of the delay line located at G9 on the 'B' processor. There are several solutions to this problem, one will be presented. A rough adjustment can be made on the 'A' processor by adding 30 ns of delay. This is accomplished by moving the tap from 'J' to 'B' for signal ECKPR.H/. The card should be re-inserted, and the clocks should be again compared since there is an inherent error margin within delay lines. Assume that only 27 ns of delay was added such that the 'B' processor system clock is still 6 ns ahead of the 'A' processor system clock. Add 6 ns of delay by moving the DPR...H/ tap from 'K' to 'M' on delay line L5 on the 'B' processor. Re-insert the 'B' processor H9 card and verify that the adjustment brought the system within specification.

See next page for adjustment locations.

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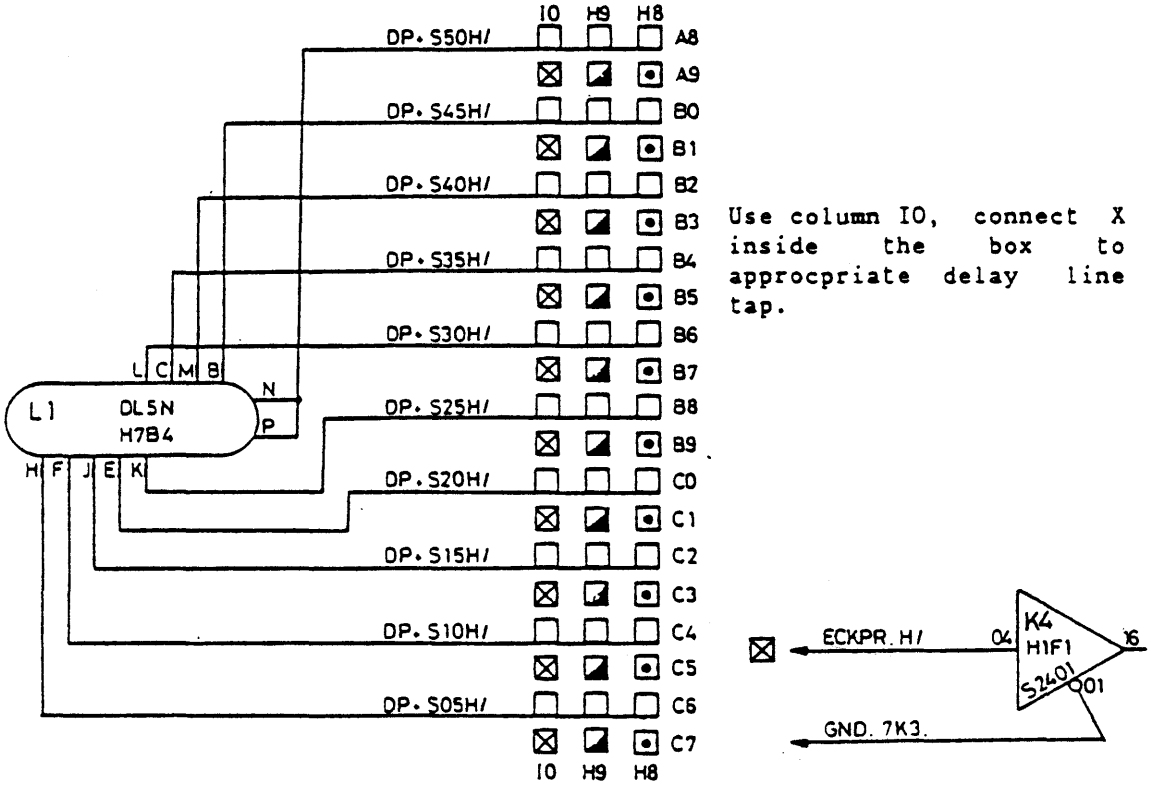
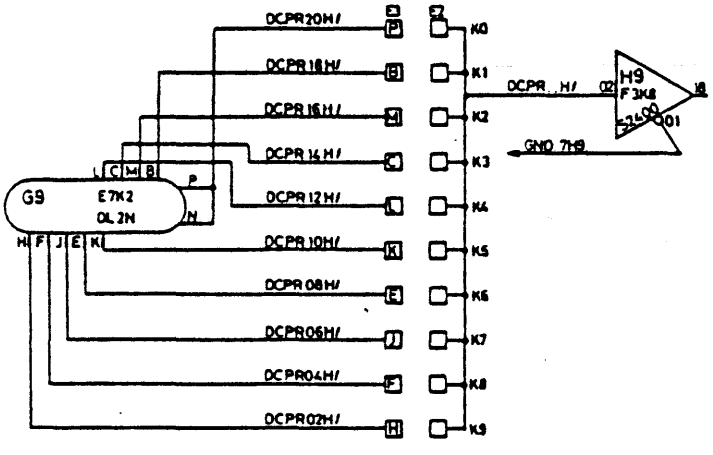


Use column IO, connect X inside the box to approcpriate delay line tap.

Adjustment on A processor H9 card



Connect appropriate delay line tap of column E3 to column E2.

Adjustment on B processor H9 card

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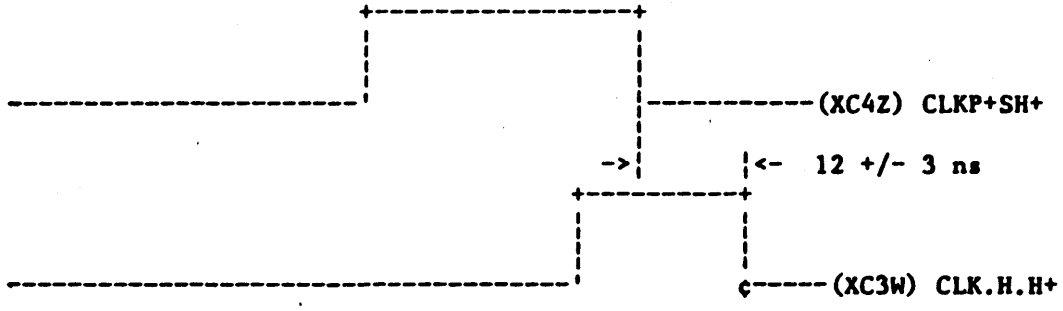
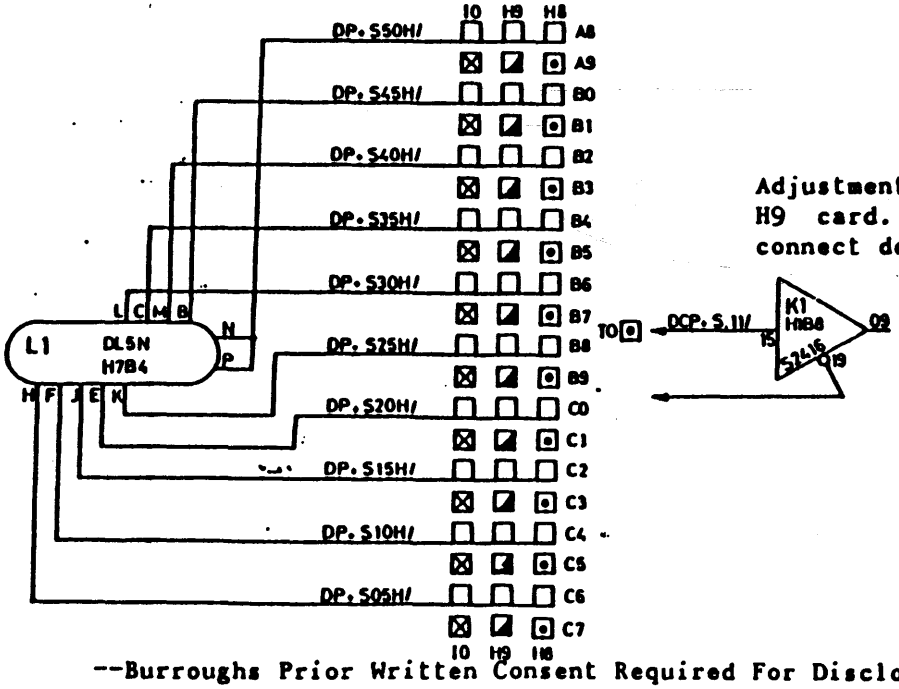
6.3 'B' PROCESSOR PAD, STACK AND CACHE CLOCK ADJUSTMENT

With the cards inserted, place channel 1 probe on XC3W for signal CLK.H.H+ on card H9 of processor 'B'. Place channel 2 probe on pin XC4Z of card H9 of processor 'B' for signal CLKP+SH+ to be 12 +/- 3 ns before the falling edge of CLK.H.H+. This relation is shown below.



Example: Assume that the tap is on 'K' and CLKP+SH+ is 20 ns ahead of CLK.H.H+. 8 ns of delay should be removed for a nominal setting, but only 5 ns increments are available. If 10 ns of delay is removed, CLKP+SH+ would be 10 ns ahead of CLK.H.H+. This is within tolerance, thus the tap should be moved from 'K' to 'J'.



Adjustment on 'B' processor H9 card. Use column H8, connect dots to dots.

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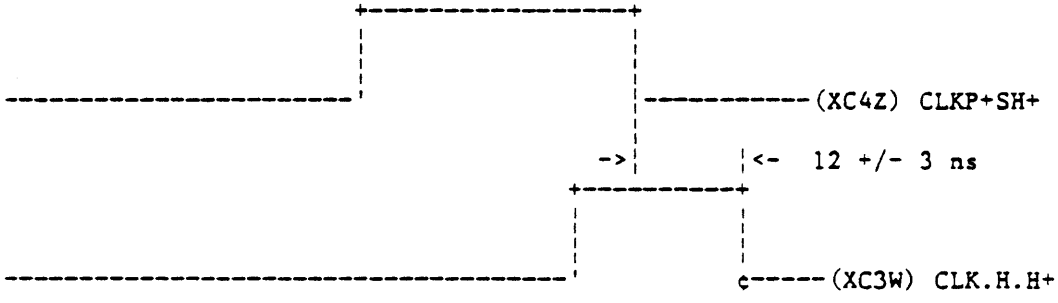
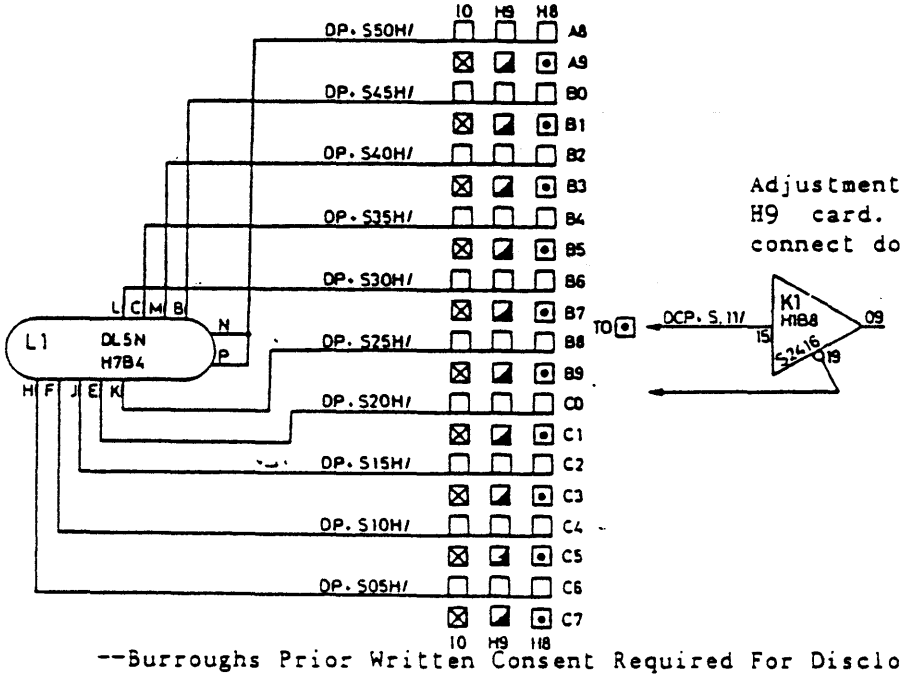
6.3 'B' PROCESSOR PAD, STACK AND CACHE CLOCK ADJUSTMENT

With the cards inserted, place channel 1 probe on XC3W for signal CLK.H.H+ on card H9 of processor 'B'. Place channel 2 probe on pin XC4Z of card H9 of processor 'B' for signal CLKP+SH+ to be 12 +/- 3 ns before the falling edge of CLK.H.H+. This relation is shown below.



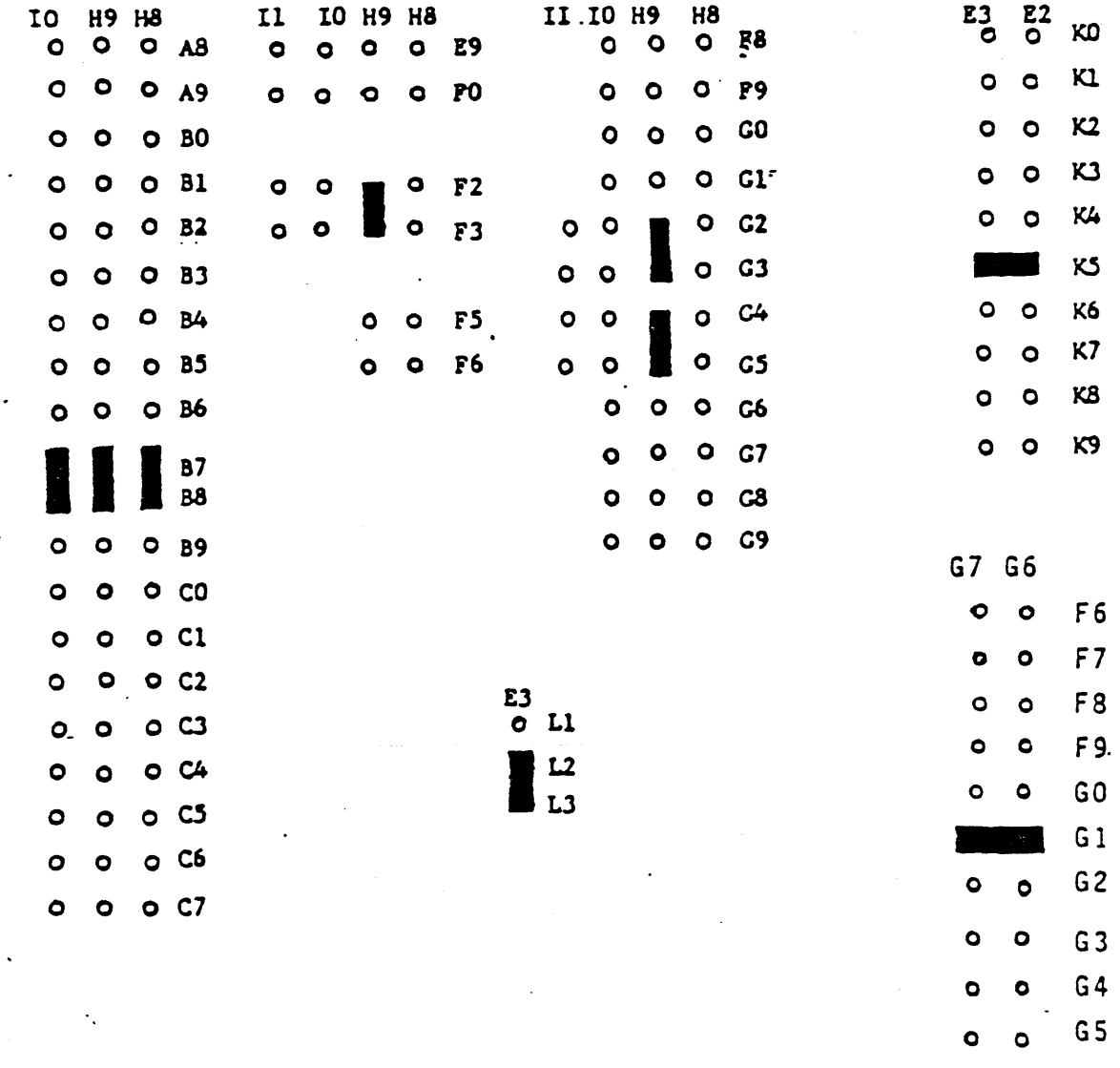
Example: Assume that the tap is on 'K' and CLKP+SH+ is 20 ns ahead of CLKPR2H+. 8 ns of delay should be removed for a nominal setting, but only 5 ns increments are available. If 10 ns of delay is removed, CLKP+SH+ would be 10 ns ahead of CLKPR2H+. This is within tolerance, thus the tap should be moved from 'K' to 'J'.



Adjustment on 'B' processor H9 card. Use column H8, connect dots to dots.

--Burroughs Prior Written Consent Required For Disclosure Of This Data--

7 NOMINAL SETTINGS



INSTALL 2 PIN JUMPER, SHORTING PIN P/N 2228 7478 (9 REQ) ONTO

TEST POINT PAIRS ON CARD H9 AT LOCATIONS SHOWN ABOVE

--Burroughs Prior Written Consent Required For Disclosure Of This Data--

```
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
BBBBBBBBBBBBBB                BBBBBBBBBB
BBBBBBBBBBBBBB                 BBBBBBBBB
BBBBBBBBBBBBBBBB    BBBBBB      BBBBBBBB
BBBBBBBBBBBBBBBB    BBBBBBB      BBBBBBB
BBBBBBBBBBBBBBBB    BBBBBBB      BBBBBBB
BBBBBBBBBBBBBBBB    BBBBBB      BBBBBBBB
BBBBBBB                        BBBBBBBBB
BBBBBBB   Burroughs.          BBBBBBBBBB
BBBBBBB                        BBBBBBBBB
BBBBBBBBBBBBBBBB    BBBBBB      BBBBBBBB
BBBBBBBBBBBBBBBB    BBBBBBB      BBBBBBB
BBBBBBBBBBBBBBBB    BBBBBBB      BBBBBBB
BBBBBBBBBBBBBBBB    BBBBBB      BBBBBBBB
BBBBBBBBBBBBBB                 BBBBBBBBB
BBBBBBBBBBBBBB                BBBBBBBBBB
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
```

```
BBBBBBBBB       11      9999999       66666    555555555
BBBBBBBBBB     111     999999999     6666666   555555555
 BBB   BBB    1111     999   999    666 666    555
 BBB   BBB   11111     999 · 999   666         555
 BBBBBBBB      111     999999999   66666666    55555555
 BBBBBBBBB     111      99999999   666666666   555555555
 BBB    BBB    111          999   666   666         555
 BBB    BBB    111     999  999    666   666   555   555
BBBBBBBBBBB  1111111   9999999     666666666   555555555
BBBBBBBBBB   1111111    99999       6666666     5555555
```

```
                //     9999999    555555555
               //     999999999   555555555
              //      999   999   555
             //       999   999   555
            //        999999999   55555555
           //          99999999   555555555
          //                999         555
         //           999  999    555   555
        //            9999999     555555555
       //              99999       5555555
```

```
 SSSSSSSS   YYY      YYY   SSSSSSSS   TTTTTTTTT  EEEEEEEEE  MM        MM
SSSSSSSSSS   YYY    YYY   SSSSSSSSSS  TTTTTTTTT  EEEEEEEEE  MMM      MMM
SSS    SSS    YYY YYY     SSS    SSS     TTT     EEE        MMMM    MMMM
SSSS           YYYYY      SSSS           TTT     EEE        MMMMM  MMMMM
 SSSSSSS        YYY        SSSSSSS       TTT     EEEEEE     MMMMMMMMMMMM
  SSSSSSS       YYY         SSSSSSS      TTT     EEEEEE     MMM MMM MMM
      SSSS      YYY             SSSS     TTT     EEE        MMM  M  MMM
SSS    SSS      YYY       SSS    SSS     TTT     EEE        MMM     MMM
SSSSSSSSSS      YYY       SSSSSSSSSS     TTT     EEEEEEEEE  MMM     MMM
 SSSSSSSS       YYY        SSSSSSSS      TTT     EEEEEEEEE  MMM     MMM
```

B1965/B1995 SYSTEM TEST

02/04/83

PROPRIETARY PROGRAM MATERIAL

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CASSETTE TAPE PART NUMBER	CT 2231 3233	REVISION AE
LISTING PART NUMBER	T 2231 3225	REVISION AE

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PROGRAM REVISION INFORMATION

Revision AC is the initial release for the B1965/95 system.

Revision AD includes the following changes :

1. Change to section 12 to use the DCP on the lowest channel.

2. Change to section 9 to suppress DCP tests while running on the slave processor.

Revision AE includes modifications in order to be able to use Memorex drives (677-33 & 659).

OPERATING PROCEDURE

1) Place the SYSTEM TEST cassette in the system cassette reader.

2)

HALT the processor. If SLAVE present, put ON-LINE.

3) Type "RD MTR GO" on the ODT and XMT.

4) The entire program should load from cassette without stopping, then begin execution and run to completion without stopping. However, if during SECTION 12 both "MCPII" and "CMS" environments are present in the system, then an OPERATOR INTERVENTION HALT will occur (see halt @12FFFF@).
The test will halt after executing all test sections without error, with LR = CCCCCC and a message displayed in the text area through the "RD" command. If LR does not equal CCCCCC when the test halts, consult the HALT CODE LISTING, starting on PAGE 15 of this document.

5) Part number and revision level information will be displayed in the X, Y, T, and L registers, as shown below, during the program load (LR will contain @AAAAAA@), and, at the ENTER OPTIONS HALT, LR=EEEEEE, which is obtained by depressing the INTERRUPT switch while the test is running , and holding it until the test halts. The cassette must have finished loading before the INTERRUPT switch is pressed.

    X = @003233@ : Cassette part number in HEX.
    Y = @003225@ : Listing part number in HEX.
    T = @00C1C5@ : Cassette revision (EBCDIC for "AE").
    L = @00C1C5@ : Listing revision (EBCDIC for "AE").

NOTE: the LR = @AAAAAA@ display will not occur until the basic processor test cases have been completed, which is approximately 60 seconds after the load begins.

6) The program takes about 2 1/2 minutes to load from cassette, and then less than 2 minutes to run to completion.

REMOTE OPERATION

This test can be executed in "remote" mode by following normal remote operation procedures. All displays that appear on the local ODT screen will also be displayed remotely, with the exception of the "TEST,TEST" and "I/O STATUS" screens outputed during SECTION 12. These displays are part of the MLC test process, and displaying them remotely would assume that the MLC (Line 3) was operational, and is thus illogical at this time. During remote operation the System Test uses only the MAC to communicate with the remote site, the MLC is never used for this purpose.

CONSOLE DISPLAY DURING DEFAULT EXECUTION

During the DEFAULT load and execution of the test, the program will halt/restart several times, causing the console display to be automatically updated. By observing the contents of the LR register, and in some cases various other indicators, the progress of the test can be followed.

The following table lists, in chronological order, the displays that should occur:

LR REGISTER	OTHER OBSERVATIONS
@_____@	Console display is invalid for first 60 seconds of load process.
@AAAAAA@	For final 90 seconds of load process. X, Y, T, L contain test revision data.
@010903@	CNS HALT/RESTART function test
@A1111A@	Indicates 'BEGINNING OF TEST' (Memory resident portion)
@B1111B@	Indicates beginning of 'CASE 1' test group.
@_____@	"TEST TEST TEST ...." ETC. Online test of ODT function
@_____@	Online I/O status display
@810050@	CNS HALT/RESTART function test
@810130@	"ERROR" will be displayed briefly
@B2222B@	Beginning of 'CASE 2' test group
@B3333B@	Beginning of 'CASE 3' test group
@B4444B@	Beginning of 'CASE 4' test group
@CCCCCC@	Test Completed Halt

Note that after a "restart" (see next page) the "ERROR" display may not be seen during the LR = 810130 display (this is dependent on the status of the SLAVE).

RESTART PROCEDURES

There are three RESTART PROCEDURES. Each one is applicable in specific circumstances :

A. At the LR=CCCCCC halt, enter "GO" to run program again.

B. If the test is running, depress and hold the INTERRUPT switch until the LR = EEEEEE halt occurs. (At the LR = CCCCCC halt, enter "GO" and hold the INTERRUPT switch until the LR = EEEEEE halt occurs). The program scratchpads may be modified at this at this time. Enter "GO" to restart program execution.

C. For a HARD RESTART; HALT the processor, enter "SW24 0 0, 0 CLR A 80 GO" .

LOOPING PROCEDURE

1) Hold console INTERRUPT switch down until LR=EEEEEE halt.

2) Set S06A equal to the number of times the entire program should be repeated. Default = 1, FFFFFF = Loop Forever.

3) Enter "GO". The program will run until done (LR=CCCCCC), or, until an error is detected, or, until console INTERRUPT switch is depressed again (LR=EEEEEE).

POSSIBLE RESTARTS FROM ERROR HALT

1) To repeat the failing section: enter "S01A 0 GO".

2) To continue with next section: enter "S01A 4 GO".

SCRATCHPAD OPTIONS

These PADS should only be changed while at the ENTER OPTIONS HALT (LR=EEEEEE) , obtained by depressing the INTERRUPT switch and holding until halted. The definitions given for scratchpad contents ONLY APPLY IF THE SYSTEM IS HALTED WITH LR = EEEEEE.

A-pads contain control information for the MASTER processor.

B-pads contain control information for the SLAVE processor.

S01A PROGRAM OPTIONS

S02A MASTER PROCESSOR TEST SECTIONS

Each bit position selects one section. DEFAULT = 1FF800 = SECTIONS 3 thru 12.

S03A MASTER PROCESSOR SECTION CURRENTLY EXECUTING.

S06A PROGRAM PASS LIMIT.

REPEAT LIMIT, indicates the number of times the entire program will be repeated. DEFAULT = 1.

S07A PROGRAM PASS COUNTER

Counts number of program passes.

S12A MASTER PROCESSOR PORTS.

Contains 6 port numbers. The A, B, C & D fields contain MLC port numbers. The E-field contains the MASTER processor port number and the F-field contains the SLAVE processor port number. If any field is not used, then will be @F@.

S02B SLAVE PROCESSOR TEST SECTIONS

Each bit position selects one section. DEFAULT = 1FC000 = SECTIONS 3 thru 9.

S03B SLAVE PROCESSOR SECTION CURRENTLY EXECUTING

S12B SLAVE PROCESSOR PORTS.

Contains 6 port numbers. The A, B, C & D fields contain MLC port numbers. The E-field contains the SLAVE processor port number and the F-field contains the MASTER processor port number.

PROGRAM OPTIONS [S01A!

BIT MAP:

```
0 0 0 0   0 0 0 0   0 0 1 1   1 1 1 1   1 1 1 1   2 2 2 2
0 1 2 3   4 5 6 7   8 9 0 1   2 3 4 5   6 7 8 9   0 1 2 3
```

BIT	MEANING
12	There is no SLAVE processor on the system.
16	CLEAR. When turned on at an LR=EEEEEE (ENTER OPTIONS HALT), causes program options and pads to be reinitialized and then program is started. Performs the same function as typing "CLEAR A 80 GO".
17	START. When turned on at an LR=EEEEEE (ENTER OPTIONS HALT), restores program options and pads from a memory save area and then restarts program.
18	HALT AT START OF PROGRAM. This bit is checked just after program starts. The bit causes an LR=AAAAAA halt. DEFAULT = OFF
19	HALT AT START OF SECTION. This bit is checked after section is loaded and before starting section. The bit causes an LR=SSAAAA halt. SS=section number. DEFAULT = OFF
21	IGNORE ERRORS. This bit is checked following an error halt. If ON, then the failing section is NOT REPEATED. If OFF, the failing section is REPEATED. DEFAULT = ON.

SECTION SELECTION

Usually, SECTION SELECTION bits should not be changed. The complete test should always be run to assure the maximum chance of the program detecting any errors.

Each test section is represented by a bit in SCRATCHPAD S02. MASTER section numbers are listed in S02A, SLAVE section numbers are listed in S02B. Both processors use the same sections. MASTER processor uses sections 3 thru 12, SLAVE uses 3 thru 9. Sections 1 and 2 are run by both processors but are not selectable. S02A should only be changed while at the ENTER OPTIONS HALT .

S02A bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16-23
MASTER sections	3	4 5 6 7	8 9 10 11	12	

S02B bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16-23
SLAVE sections	3	4 5 6 7	8 9		

PROGRAM INFORMATION

The objective of the three central system DIAGNOSTIC programs for the B1965/95 is to direct the Field Engineer systematically towards a failure. The three CENTRAL SYSTEM DIAGNOSTICS are:

SYSTEM TEST
PROCESSOR TEST
S-MEMORY TEST

The SYSTEM TEST is designed to be the first central system test to be run and should be helpful in isolating failures to the MASTER or SLAVE PROCESSOR, MEMORY, MULTILINE-CONTROL, or DSC. Then the appropriate DIAGNOSTIC test can be run for isolation. The system test will load and run in less than 5 minutes.

If a problem is suspected in the DSC or MLC then that diagnostic program should be run first. If these programs will not load, give invalid results, or detect no errors, then the SYSTEM test should be run. Likewise if a processor or memory problem is indicated, that program should be run first, then the SYSTEM test.

The minimum system for this program consists of one processor, S-memory, MLC4 or DCP with ODT, DSC with at least one unit READY. The Disk Unit that is made READY is normally the one used for Clear Start, but must contain at least the following software:

MCPII : "SYSTEM/MLFIRMWARE"
or, CMS : "SYSTEST-FWAD".

If not, then errors will be indicated. The maximum system tested is two processors, 2 megabytes S-memory, MLC with ODT, DSC with one unit READY. Other I/O devices present will be utilized only to test the I/O bus interface.

PROGRAM OPERATION

SECTION 1 is executed in MTR (TAPE) mode. If an error is detected then the cassette stops on the error, with a HALT CODE in LR. The ERROR DIRECTORY begins on PAGE 15.

PROGRAM LOADER is written into S-memory after SECTION 1 has completed, and started. A check is made of the 7C micro and if an error is found then the documentation points to either the memory or the processor as the source. The rest of the program is now written from cassette into S-memory.

SECTION 2 is executed in NORMAL MODE to verify that the subset of micros used in the main program EXECUTIVE is operational. If not, then documentation refers to the PROCESSOR TEST for isolation.

EXECUTIVE controls program execution for MASTER processor, and SLAVE processor if present. The rest of the sections in the program are executed in NORMAL MODE in the following manner:

CASE 1: MASTER processor runs sections 3 thru 12. Sections 3 thru 6 test processor functions, section 7 tests memory and memory micros, sections 8 and 9 test dispatch logic and the multiline-control interface logic. Section 10 tests the soft I/O interface. Section 11 performs a read check on DSC. Section 12 reads from disk & writes to ODT If error then documentation points to the suspected subsystem in error.

CASE 2: SLAVE processor, if present, runs sections 3 thru 9 of the set of sections described above. If error, then documentation refers to the appropriate subsystem.

CASE 3: The SLAVE processor is started running sections 3 thru 9, then the MASTER processor starts running sections 3-9 at the same time.

CASE 4: Section 9 (MLC OPs) is run by MASTER processor at the same time as section 9 (MLC OPs) is run by the SLAVE.

SECTION DESCRIPTIONS

SECTION 1 - MTR MODE TESTS

These MICROS are tested to ensure that they are operational when used later by the program loader. Errors will come to a cassette stop error halt and the specific micro failing will be described. For additional isolation, the PROCESSOR TEST should be run.

9C to X,Y,LR and 2E cassette control
1C to X,Y,FA,BR,LR,TAS,A,PERM,PERP,CD
CP=24, CD=4
X,Y SUM & DIFF
8C to X,Y
9C to FA,BR,TAS,A
X LSS Y
6F INC A
12C 13C 14C 15C, A-reg, TAS
6D COUNT FA by 16, FL by 1
7C
TAS, 8 levels of STACK
3C on MSSW
10C S/R T to A,MSSW,TAS,CP
2C with X,Y,S0A,S15B,other pads,A,B,TAS,CP,MSSW
CACHE KEY STORE
CACHE-ONLY execution
S-MEMORY-ONLY exection
NORMAL-MODE execution

SECTION 2

Specific MICRO VARIANTS are tested in NORMAL MODE to ensure they are operational when used later by the main program.

3C OR/AND to T & CC
3C INC FLF BY 1 TEST & DEC FLF BY 1 TEST
4C/5C on XYCN and CC(0,1)
6C on T and LF=F
8C to TAS, 8C to FL
10C SHIFT T LEFT BY 0-24 bits
6D COUNT FL DOWN BY CPL-24
FLF OR-with-M
1C FB to TAS, FL to CP
2C A & B pads.

SECTION DESCRIPTIONS (CONT.)

SECTION 3

Verifies more processor MICROS. If failure then processor is suspect. Run PROCESSOR TEST for isolation.

4D 5D SHIFT ROTATE X Y
3F NORMALIZE X
24-bit FUNCTION BOX
6E CARRY manipulate

A CHECKSUM is accumulated on all registers as each test is performed, and compared with a precalculated checksum.

SECTION 4

Verifies more MICROS. If failure then processor is suspect. Run PROCESSOR TEST for isolation.

3C/6C 4-bit manipulate and SKIP WHEN
4C/5C BIT TEST BRANCH
10C/11C SHIFT ROTATE T

A CHECKSUM is accumulated on all registers as each test is performed, and compared with a precalculated checksum.

SECTION 5

Verifies more MICROS. If failure then processor is suspect. Run PROCESSOR TEST for isolation.

3D CLEAR
6D COUNT FA/FL
3E BIAS
4E/5E LOAD STORE
7D EXCHANGE
8D RELATE

A CHECKSUM is accumulated on all registers as each test is performed, and compared with a precalculated checksum.

SECTION 6

PIPELINE FLOW, WAIT LOGIC, and CONFLICTS tests. If failure then run PROCESSOR test for isolation.

SECTION DESCRIPTIONS (CONT.)

SECTION 7

Verifies all MICROS that function with S-MEMORY. If failure then PROCESSOR or MBU is called out as suspect.

SECTION 8

Processor DISPATCH LOGIC is tested using own port number and invalid port numbers. If failure then either PROCESSOR, MBU, or MLC is suspect.

SECTION 9

PROCESSOR TO MULTILINE CONTROL testing. If failure, then the MULTILINE CONTROL is suspect. If NO MLC found than error indicated.

SECTION 10

SOFT IO CHANNELS are tested. If failure, then the I/O device on that channel is suspect. Run that particular test for isolation. Or if no response from any channel, then the processor is suspect.

SECTION 11

The DSC is tested with a disk pack mounted. If none found then error is indicated. If error detected then run the DSC diagnostic.

Assuming a 205, 206 or 207 pack. For the lowest channnel DSC found, UNIT 0 (SYSTEM disk), execute READS ONLY from SECTORS 0 through @020000@. This test will effectively test the I/O bus to the DSC and that the DSC can transfer data from the disk.

SECTION 12

All disks present are searched until a "SYSTEM/MLFIRMWARE" file (on MCPII systems), or a "SYSTEST-FWAD" file (on CMS systems) is found. The FIRMWARE file is read to memory then downloaded to the MLC on PORT 1 (or DCP 0). FIRMWARE is STARTED and ODT CONFIGURATION FILE loaded (for MLC). A full screen of I/O status information is written then read back and compared. RESULT STATUS and DATA COMPARE ERRORS are reported.

HALT CODE FORMATS

When a HALT CONDITION occurs, LR register will contain the HALT CODE.

FORMAT	MEANING
SSONNN	ERROR HALT. SS = test SECTION where error occurred. If the halt was due to a SLAVE processor error, then the most significant bit of LR is also on. NNN = error number.
AAAAAA	BEGIN PROGRAM HALT. "BEGIN PROGRAM HALT" option bit is selected and program is ready to begin.
SSAAAA	BEGIN SECTION HALT. SS = test SECTION. "BEGIN SECTION HALT" option bit is selected and section is ready to begin.
BXXXXB	HALT CODE displayed while CASE XXXX is running. If halted then have unexpected error. CASE XXXX = 1111, 2222, 3333, or 4444
BBBBBB	UNEXPECTED HALT IN EXECUTIVE.
SSBBBB	UNEXPECTED HALT IN A TEST SECTION.
CCCCCC	PROGRAM COMPLETE. All selected loops and passes of the test have completed. (See PAGE 60 for extra information).
EEEEEE	ENTER OPTIONS HALT. Occurs when "INTERRUPT" pushbutton is depressed while program is running. Any scratchpad option can be changed here. The following information is displayed: X = cassette part number in HEX. Y = listing part number in HEX. T = cassette revision in EBCDIC. L = listing revision in EBCDIC.

ERROR DIRECTORY

SECTION 1 - MTR MODE TESTS

These MICROS are tested to ensure that they are operational when used later by the PROGRAM LOADER. Errors will come to a cassette stop error halt and either the PROCESSOR TEST or MBU TEST specified to be run for isolation.

Unless specified otherwise all halts in this section are PROCESSOR errors; PROCESSOR TEST should be run for isolation.

9C to X,Y,LR and 2E CASSETTE CONTROL
1C to X,Y,FA,BR,LR,TAS,A,PERM,PERP,CD
CP=24, CD=4
X,Y SUM & DIFF
8C to X,Y
9C to FA,BR,TAS,A
X LSS Y
6F INC A
12C 13C 14C 15C, A-reg, TAS
6D COUNT FA BY 16, FL BY 1
7C
TAS, 8 levels of STACK
3C on MSSW
10C S/R T to A,MSSW,TAS,CP
2C with X,Y,S0A,S15B,other pads,A,B,TAS,CP,MSSW
CACHE KEY STORE
CACHE-ONLY execution
S-MEMORY-ONLY exection
NORMAL-MODE execution

HALT CODE	DESCRIPTION
010010	@90000000@ or @91000000@ failed. These are the first and second micros off the cassette (MOVE 24 bit LITERAL).
010100	@90000001@ executed as a HALT micro, or @91000022@ executed as a CASSETTE STOP micro.
010110	MOVE @FFFFFF@ TO X or MOVE @FFFFFF@ TO Y failed.
010112	MOVE @AAAAAA@ TO X failed.
010114	MOVE @AAAAAA@ TO Y failed.
010116	MOVE @555555@ TO X failed.

010117 MOVE @555555@ TO Y failed.

010120 MOVE X TO FA or MOVE FA TO Y failed. X = 0

010121 MOVE FA TO X failed. X = 0

010122 MOVE X TO FA or MOVE FA TO Y failed. X = FFFFFF

010123 MOVE FA TO X failed. X = FFFFFF

010125 MOVE X TO BR or MOVE BR TO Y failed. X = 0

010126 MOVE BR TO X failed. X = 0

010127 MOVE X TO BR or MOVE BR TO Y failed. X = FFFFFF

010128 MOVE BR TO X failed. X = FFFFFF

010130 MOVE X TO TAS or MOVE TAS TO Y failed. X = 0

010131 MOVE TAS TO X failed. X = 0

010132 MOVE X TO TAS or MOVE TAS TO Y failed. X = FFFFFF

010133 MOVE TAS TO X failed. X = FFFFFF

010135 MOVE X TO A or MOVE A TO Y failed. X = 0

010136 MOVE A TO X failed. X = 0

010137 MOVE X TO A or MOVE A TO Y failed. X = FFFFFF

010138 MOVE A TO X failed. X = FFFFFF

010140 MOVE X TO PERM or MOVE PERM TO Y failed. X = 0

010141 MOVE PERM TO X failed. X = 0

010142 MOVE X TO PERM or MOVE PERM TO Y failed. X = F

010143 MOVE PERM TO X failed. X = F

010145 CD not equal 8 after previous test.

010146 MOVE X TO PERP or MOVE PERP TO Y failed. X = 0

010147 MOVE PERP TO X failed. X = 0

010148 MOVE X TO PERP or MOVE PERP TO Y failed. X = 7

010149 MOVE PERP TO X failed. X = 7

010150 CD not equal 8 after previous test.

010151 MOVE X TO CD or MOVE CD TO Y failed. X = 0

010152 MOVE CD TO X failed. X = 0

010153 MOVE X TO CD or MOVE CD TO Y failed. X = F

010154 MOVE CD TO X failed. X = F

010160 MOVE NULL TO CP or MOVE CP TO X failed. X = 0

010162 MOVE 24 TO CP failed.

010170 SUM or DIFF is incorrect.

010171 SUM or DIFF is incorrect.

010175 SUM or DIFF is incorrect.

010176 SUM or DIFF is incorrect.

010180 SUM or DIFF is incorrect.

010181 SUM or DIFF is incorrect.

010185 SUM or DIFF is incorrect.

010186 SUM or DIFF is incorrect.

010200 MOVE @00@ TO Y failed.

010210 MOVE @00@ TO X failed.

010220 MOVE @FF@ TO X failed.

010230 MOVE @55@ TO Y failed.

010240 MOVE @AA@ TO X failed.

010250 MOVE @AA@ TO Y failed.

010260 MOVE @FF@ TO X failed.

010270 MOVE @FF@ TO Y failed.

010300 MOVE @FFFFFF@ TO FA failed.

010310 MOVE @000000@ TO FA failed.

010320 MOVE @FFFFFF@ TO BR failed.

010330 MOVE @000000@ TO BR failed.

010360 MOVE @FFFFFF@ TO TAS failed.

010370 MOVE @000000@ TO TAS failed.

010372 XYCN is incorrect.

010374 XYCN is incorrect.

010376 XYCN is incorrect.

010378 XYCN is incorrect.

010380 MOVE @000000@ TO A failed.

010390 MOVE @0FFFF0@ TO A failed.

010400 INCREMENT A failed. A should equal 000010.

010410 INCREMENT A failed. A should equal 555560.

010420 INCREMENT A failed. A should equal 0AAAB0.

010430 INCREMENT A failed. A should equal 000000.

010450 MICRO C000 failed. A should equal 0.

010451 MICRO CFFF failed. A should equal 00FFF0.

010452 MICRO C000 failed. A should equal 0efff0.

010453 MICRO CFFF failed. A should equal 0FFFE0.

010455 MICRO D000 failed. A should equal 0.

010456 MICRO DFFF failed. A should equal 0E0010.

010460 MICRO E000 failed. A should equal 0.

010461 MOVE TAS TO X failed. X should equal 0.

010462 MOVE TAS to A failed. A should equal 0.

010463 MICRO EFFF failed. A should equal 0FFFE0.

010464 MOVE TAS TO X failed. X should equal 0EFFF0.

010465 MOVE TAS TO A failed. A should equal 0EFFF0.

010466 MICRO F000 failed. A should equal 0.

010467 MOVE TAS TO X failed. X should equal 0.

010468 MOVE TAS TO A failed. A should equal 0.

010510 COUNT FA UP BY 16 failed. FA should equal 000010.

010520 COUNT FA UP BY 16 failed. FA should equal 00000F.

010530 COUNT FL DOWN BY 1 failed. FL should equal 0000.

010540 COUNT FL DOWN BY 1 failed. FL should equal FFFE.

010600 WRITE (25) BITS FROM X INC FA failed to INC FA to 000018.

010602 PERM NEQ 0 after above WRITE.

010604 WRITE 16 BITS FROM Y changed FA. FA should equal 000018.

010606 PERM NEQ 0 after above write.

010608 READ 24 BITS TO Y INC FA failed to return correct data. Y should equal 0. FA = 0. Run PROC.test first, then MBU.

010610 INC FA in above micro failed. FA should equal 000018.

010612 PERM after above micro NEQ 0.

010614 READ 16 BITS TO X failed to return correct data. FA = 000018. X should equal 0. Proc. test first, then MBU.

010616 PERM after above micro NEQ 0.

010618 WRITE (25) BITS FROM X INC FA AND DEC FL failed. FA should equal 00124C.

010620 PERM NEQ 0 after above micro.

010621 FL NEQ 00D8 after above micro.

010622 WRITE 16 BITS FROM X changed FA from 00124C.

010624 PERM NEQ 0 after above micro.

010626 READ 24 BITS TO X INC FA failed to return correct data. X should equal FFFFFF. FA = 001234. Run PROC. test first, then MBU.

010628 INC FA failed on above micro. FA should equal 00124C.

010630 PERM NEQ 0 after above micro.

010632 READ 16 BITS TO Y failed to return correct data. Y should equal 00D8. FA = 00124C. Run PROC. test first, then MBU.

010634 PERM NEQ 0 after above micro.

010720 Nine pushes of A-STACK were done, with 000000, 111111, 222222, 333333, 444444, 555555, 666666, 777777, 888888. Followed by a MOVE TAS TO Y which failed to return the correct value. X equals the correct value.

010730 MOVE MSSW TO X failed. X should equal 3.

010732 AND MSSW WITH 3 failed.

010734 OR MSSW WITH 2 failed.

010736 EOR MSSW WITH 0 failed.

010750 SHIFT T LEFT BY 1 BIT TO A failed; A should = 000020.

010752 ROTATE T LEFT BY 1 BIT TO MSSW failed; MSSW should = 3.

010754 SHIFT T LEFT BY 1 BIT TO TAS failed; TAS should = 2.

010756 SHIFT T LEFT BY 1 BIT TO CP failed; CP should equal 2.

010758 MOVE X TO S0A,S15B,S3B,S1A,S2B or MOVE S01, S15B, S3B, S1A, S2B TO Y failed; X equal FF00FF.

010760 MOVE S0A TO A or MOVE A TO S15B failed; all = 056780.

010762 MOVE S0A TO M followed by MICRO 0000 failed; S0A = 0621.

010764 MOVE S0A TO TAS or MOVE TAS TO S15B failed; all = FFFFFF.

010766 MOVE S0A TO CP or MOVE CP TO S15B failed; all = 0000FF.

010771 FL = 0; A = FFF0; MICRO 5791 failed; A should = 10000.

010772 FL NEQ 0; A = FFF0; MICRO 5791 failed; A should = FFF0.

010773 FL = 0; A = FFF0; MICRO 5792 failed; A should = 10000.

010774 FL NEQ 0; A = FFF0; MICRO 5792 failed; A should = FFE0.

010775 FL = 0; A = FFF0; MICRO 5794 failed; A should = 10000.

010776 FL NEQ 0; A = FFF0; MICRO 5794 failed; A should = FFC0.

010777 FL = 0; A = FFF0; MICRO 5798 failed; A should = 10000.

010778 FL NEQ 0; A = FFF0; MICRO 5798 failed; A should = FF80.

010780 FA = 0; X = 01FFFF; WRITE CACHE FROM X Y T L followed by READ CACHE KEY.DATA TO Y failed to return Y = 500001.

010781 See above. READ CACHE TO Y failed to return Y = 01FFFF.

010782 See above. PERP NEQ 0.

010785 FA = FF0000. X = 0. WRITE CACHE FROM X Y T L followed by READ CACHE KEY.DATA TO Y failed to return Y = 5001FF.

010786 See above. READ CACHE TO Y failed to return Y = 0.

010787 See above. PERP NEQ 0.

NOTE >>> For 010788 - 010804 the following is tested: Transition from MTR mode to CACHE-ONLY mode. Then execution in CACHE-ONLY from every CACHE location. Then transition from CACHE-ONLY mode to MTR mode.

010788 The CACHE routine has been loaded incorrectly.

010794 WRITE (25) BITS FROM X INC FA hung up.

010796 Switching from CACHE-ONLY to MTR doesn't work.

010800 Switching from MTR to CACHE-ONLY doesn't work.

010802 PERP found UNEQUAL to 0 following CACHE execution.

010804 The routine in CACHE failed to execute properly.

010805 In CACHE-ONLY mode, S-MEMORY failed to return correct data. Try MBU test.

010806 Same as 805.

010807 Same as 805.

010808 Same as 805.

NOTE >>> For 010810 - 010844 the following is tested: Transition from MTR mode to S-ONLY mode. Execution in S-ONLY from FFF0 addresses. Transition from S-ONLY mode to MTR mode. Transition from MTR mode to NORMAL mode. Execution in NORMAL from FFF0 addresses. Transition from NORMAL mode to MTR mode.

010810 MBU. The S-MEMORY routine has been loaded incorrectly.

010812 MBU. WRITE (25) BITS FROM X INC FA hung up.

010818 PROC. Switching from S-ONLY or NORMAL to MTR mode not ok.

010820 PROC. Switching from MTR to S-ONLY doesn't work.

010824 PROC. PERM found UNEQUAL to 0 following above execution.

010825 The routine in S-ONLY failed to execute properly. Run MBU test. Also suspect can be the MLC which can interfere with S-MEMORY operations. Try disconnecting the MLC and running this test again.

010840 Switching from MTR mode to NORMAL doesn't work correctly.

010842 PERM NEQ 0 after above NORMAL mode routine.

010844 The routine in NORMAL failed to execute properly.

NOTE: THE REST OF THE TESTS IN SECTION 1 WILL BE IN NORMAL MODE.

010850 MAC card H is suspect. CNS.ENABLE (000081) moved to CNS. MAC failed to respond with CNS=000081.

010860 MAC card H is suspect. CNS.GET.STATUS.VECTOR (000002) moved to CNS. MAC failed to respond with non zero in CNS.

010870 MAC card H is suspect. CNS.HALT.SLAVE (000003) moved to CNS. MAC failed to respond with CNS=000000.

010880 MAC card H is suspect. CNS.HALT.RESTART (000040) moved to CNS. MAC failed to respond with CNS=000040.

010890 MAC card H is suspect. CNS.DISABLE (000083) moved to CNS. MAC failed to respond with CNS=000083.

010900 In NORMAL mode, JUMP PROCESSOR.TYPE (micro 0009) failed to skip.

010901 MASTER processor port number found unequal to 0.

010902 READ.PORT.NUMBER (8F) MICRO failed to return MASTER processor port number into TF. Run PROCESSOR test.

010903 MAC card H9 is suspect. The following CNS sequence failed. MOVE @81@ TO CNS, MOVE @03@ TO CNS, MOVE @40@ TO CNS, HALT MICRO. Halt occurred but MAC should have prevented it.

010904 The SLAVE processor has branched erroneously into code meant only for MASTER. Suspect SLAVE processor MICRO error in a BRANCH. Run PROCESSOR TEST on SLAVE processor.

010909 Switch from MTR to NORMAL failed.

010910 PERM NEQ 0 following WRITE 16 BITS FROM X INC FA. See FA.

010911 Memory from end of program to MAXS-16 was written with zeros. Then READ 16 BITS TO T INC FA failed to return 0. Run MBU test.

010912 See above. PERM NEQ 0.

010950 The main program is being loaded to memory. PERM NEQ 0. See FA. Run MBU test.

010955 PERP NEQ 0 after program load.

010960 MICRO 0A01 ECHO S-MEMORY CABLE failed. Run MBU test.

010962 MICRO 0B01/0B09 ECHO WRITE DATA failed. Run MBU test.

010964 MICRO 0B0A/0B2A ECHO ADDRESS failed. Run MBU test.

010966 MICRO 0B04/0B0C/0B00 WRITE/READ DIRECT failed. Run MBU test.

010970 READ ELOG MICRO failed. Run MBU test.

010971 READ ELOG MICRO failed. Run MBU test.

010972 7C timed out. Run MBU test.

010974 7C MICRO failed. Run PROCESSOR test.

SECTION 2

Specific MICRO VARIANTS are tested in NORMAL mode to ensure they are operational when used later by the main program.

HALT CODE	DESCRIPTION
020010	Processor error, run PROCESSOR test. OR with M failed.
020020	Processor error, run PROCESSOR test. 3C MICRO failed.
020030	Processor error, run PROCESSOR test. 4C or 5C MICRO failed.
020040	Processor error, run PROCESSOR test. 6C MICRO failed.
020050	Processor error, run PROCESSOR test. 6D MICRO failed.
020060	Processor error, run PROCESSOR test. 10C MICRO failed.

SECTION 3

Processor MICROs. If failure in any of these halts, run PROCESSOR test for isolation.

HALT CODE	DESCRIPTION
030010	SHIFT X RIGHT failed.
030020	Same as 010.
030030	SHIFT X LEFT failed.
030040	Same as 030 except a single bit is being shifted.
030050	SHIFT Y RIGHT failed.

(continued next page)

030060 Same as 050 except a single bit was shifted.

030070 SHIFT Y LEFT failed.

030080 Same as 070 except a single bit was shifted.

030090 ROTATE X LEFT failed.

030100 Same as 090 except a single bit was rotated.

030110 ROTATE X RIGHT failed.

030120 Same as 110 except a single bit was rotated.

030130 ROTATE Y LEFT failed.

030140 Same as 130 except ROTATE Y RIGHT failed.

030150 SHIFT X AND Y RIGHT BY 1 BIT failed. The X half is incorrect.

030160 Same SHIFT as 150 except the Y half failed.

030170 SHIFT X AND Y RIGHT BY 47 BITS failed.

030180 Same SHIFT as 170 except Y half is incorrect,

030190 SHIFT X AND Y LEFT BY 21 BITS failed.

030200 Same as 190 but Y is incorrect.

030210 SHIFT X AND Y LEFT BY 24 BITS failed. Y half is incorrect. It should be zero.

030220 Same as 210 except the X half is incorrect.

030230 ROTATE X AND Y RIGHT BY 36 BITS failed. X half is incorrect.

030240 Same as 230 but Y is wrong.

030250 ROTATE X AND Y RIGHT BY 25 BITS failed. X half is incorrect and should be zero.

030260 Same as 250 but Y half failed.

030270 ROTATE X AND Y RIGHT BY 0 bits. X should not have changed but did.

030280 Continued from 270. Y should not have changed either but did.

030290 ROTATE X AND Y LEFT BY 0 BITS. X should not have changed but did.

030300 Continued from 290. Y should not have changed either but did.

030310 ROTATE X AND Y LEFT BY 1 BIT failed. X half is incorrect.

030320 Same as 310 but Y half failed.

030330 ROTATE X AND Y LEFT BY 24 failed. X half is incorrect.

030340 Same as 330 but Y failed.

030350 ROTATE X AND Y LEFT BY 36 BITS failed. X half is incorrect.

030360 Same as 350 but Y failed.

030370 NORMALIZE MICRO failed. CP set to 24, FL set less than 24 and a 1 bit was set in X that should NORMALIZE to @800000@ while FL should count down to 1. X did not NORMALIZE to @800000@.

030372 Same NORMALIZE MICRO as above but FL was not @0001@ after NORMALIZE.

030374 X set to 0 and FL set to @5555@. A NORMALIZE MICRO was executed but FL was not found equal to zero.

030376 3F failed. With CP varied from 24 to 1, X is set to 1 and FL set to NORMALIZE to @0001@. FL did not count down to @0001@ correctly.

030378 Same NORMALIZE MICRO as above but X did not shift correct number of times.

030400 The CARRY MANIPULATE micro (6E) was used to set CYF, but CYF was not found to be true.

030402 The CARRY MANIPULATE micro (6E) was used to reset CYF, but CYF was not found to be false.

030404 With CYF set to 1, X= FFFFFF and Y= FFFFFF, CYL should by set but was found to be false.

030406 Same conditions as 220 except the SUM had the wrong result.

030408 @FFFFFF@ was moved to X and Y, and CYL was not found on. CP is counted down by 1 for each check of CYL.

030410 With @FFFFFF@ in X and Y, a MOVE SUM TO Y had wrong results. CP is counted down by 1 for each check of SUM.

030412 Same as 250 except X and Y are equal to @AAAAAA@. CYL was found false and should be on.

030414 Same as 250 except CYL was true, expected false.

030416 With the same conditions as 250 and CYL true, a CARRY SUM micro (0064) was executed after which CYF was found false.

030418 With the same conditions as 250 and CYL false, a CARRY SUM micro (0064) was executed after which CYF was found true.

030420 Same as 260 except using @AAAAAA@ in X and Y.

030422 Same as 270 except using @555555@ in X and Y.

030424 Same as 280 except using @555555@ in X and Y.

030426 Same as 310 except using @555555@ in X and Y.

030428 With @AAAAAA@ in X and @555555@ in Y, CYL was found true when it should be false.

030430 With @AAAAAA@ in X and @555555@ in Y, a MOVE SUM TO Y yielded a bad result . CP is counted down by 1 for each check of SUM.

030432 Same as 350 except X= @555555@ and Y= @AAAAAA@.

030434 Same as 360 except X= @555555@ and Y= @AAAAAA@.

030436 LSUX was found on with X= 0.

030438 LSUY was found on with Y= 0.

030440 LSUX was found false with X= 1.

030442 LSUY was found false with Y= 1.

030444 The BINARY ADDER and 4 BIT REGISTERS are used to generate 4 bit BCD results to test each 4 bit group of the 24 BIT ADDER. CYL was found false but should be true.

030446 Same as 430 but CYL is true, should be false.

030450 Same as 430 except the BCD SUM is incorrect.

030460 Same as 430 with CYF true.

030470 Same as 440 with CYF true.

030480 Same as 450 with CYF true.

030490 LSUX was found on with CPU= 01, and the bottom 4 bits of X not equal to 9.

030500 LSUY was found on with CPU= 01, and the bottom 4 bits of Y not equal to 9.

030510 LSUX was found false with X=9.

030520 LSUY was found false with Y= 9.

030530 CYL was found false in BCD (decimal) mode. X and Y are loaded to allow a sum of 9 in all 4 bit groups according to CPL. With CARRY on, a carry should propagate through all lower 4 bit groups and a CYL should have resulted.

030540 With X and Y equal to @FFFFFF@ and CYF false, CYD was found true when it should not be.

030550 Same conditions as 540 except a CARRY DIFFERENCE micro (0068) was executed and CYF was found true.

030560 With X and Y equal to @FFFFFF@ and CYL false, a move of DIFFERENCE TO X did not result in zero.

030570 With X and Y equal to @FFFFFF@ and CYF true, CYD was found false.

030580 Same conditions as 570 except a MOVE DIFF TO X had incorrect results.

030590 Same as 570 but X= @555555@, Y= @AAAAAA@.

030600 Same as 580 except X= @555555@, Y= @AAAAAA@.

030610 Same as 570 except X= @AAAAAA@, Y= @555555@.

030620 Same as 580 except X= @AAAAAA@, Y= @555555@.

030630 DECIMAL DIFFERENCE (BCD) failed. BINARY DIFF and 4 bit registers are used to test the BCD DIFF. CYD was found to be false.

030640 Same as 630 except CYD was true but should be false.

030650 Same as 630 except a CARRY DIFFERENCE micro (0068) was executed with CYD true and CYF was found false.

030660 Same as 630 except a CARRY DIFFERENCE micro (0068) was executed with CYD false and CYF was found true.

030670 Same as 630 except BCD DIFF result was incorrect

030680 X and Y are setup to create a CARRY DIFF for all CPL values in increments of 4 bits. CYD was found false when it should be true.

030900 While the above tests were executing, a sum was being accumulated on registers: X Y T L FA FB BICN FLCN PERM PERP XYCN SUM DIFF CMPX CMPY XANY XEOY MSKX MSKY XORY XYST CA CB CC CD CP INCN. At the end of the section, a pre-calculated sum was compared with the actual sum accumulated and found to be unequal. One of the following MICROs failed: Run PROCESSOR test for isolation.

1C source/sink all regs to X & Y
2C source/sink all pads to X & Y
10C SHIFT/ROTATE T TO X & Y
11C EXTRACT T TO X & Y
2D SWAP MEMORY with X & Y
3D CLEAR X & Y
4D/5D SHIFT/ROTATE X & Y
3F NORMALIZE X
24-BIT FUNCTION BOX

03AAAA Start of section halt.

03BBBB Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 4

Processor MICROs. If failure then run PROCESSOR TEST.

HALT CODE	DESCRIPTION
040210	3C INC AND TEST failed to skip properly.
040220	3C DEC AND TEST failed to skip properly.
040230	6C VAR=0 failed to skip properly.
040240	Same as above.
040250	6C VAR=1 failed to skip properly.
040260	Same as above.
040270	6C VAR=2 failed to skip properly.
040280	Same as above.
040290	6C VAR=3 failed to skip properly.
040300	Same as above.
040310	6C failed to skip properly.
040410	SHIFT T TO Y failed. SHIFT X is used to test SHIFT T and each time the shift amount is decreased from 23 to 0. Shift pattern is 000000.
040420	Same as 410 except SHIFT T TO L failed.
040430	Same as 410 except SHIFT T TO X failed.
040440	Same as 410 except SHIFT T TO T failed.
040450	Same as 410 using a pattern of FFFFFF.
040460	Same as 420 using a pattern of FFFFFF.
040470	Same as 430 using a pattern of FFFFFF.
040480	Same as 440 using a pattern of FFFFFF.
040490	Same as 410 using a pattern of 555555.

040500 Same as 420 using a pattern of 555555.

040510 Same as 430 using a pattern of 555555

040520 Same as 440 using a pattern of 555555.

040530 Same as 410 using a pattern of AAAAAA.

040540 Same as 420 using a pattern of AAAAAA.

040550 Same as 430 using a pattern of AAAAAA.

040560 Same as 440 using a pattern of AAAAAA.

040570 ROTATE T TO Y failed. ROTATE X is used to test ROTATE T and each time the rotate amount is decreased from 23 to 0. Shift pattern is @000000@. Y should be 0.

040580 Same as 570 except ROTATE T TO L failed.

040590 Same as 570 except ROTATE T TO X.

040600 Same as 570 except ROTATE T TO T failed.

040610 Same as 570 using a pattern of @FFFFFF@.

040620 Same as 580 using a pattern of @FFFFFF@.

040630 Same as 590 using a pattern of @FFFFFF@.

040640 Same as 600 using a pattern of @FFFFFF@.

040650 Same as 570 using a single bit.

040660 Same as 580 using a single bit.

040670 Same as 590 using a single bit.

040680 Same as 600 using a single bit.

040690 Same as 570 using a pattern of @FFFFFE@.

040700 Same as 580 using a pattern of @FFFFFE@.

040710 Same as 590 using a pattern of @FFFFFE@.

040720 Same as 600 using a pattern of @FFFFFE@.

040730 SHIFT T BY CPL failed. SHIFT X is used TO check SHIFT T BY CPL and each time the shift amount is decreased from 24 TO 0.

040740 Same as 730 except ROTATE T is tested.

040750 Sink decode - ROTATE T LEFT BY 23 BITS TO TA

040751 Sink decode - ROTATE T LEFT BY 23 BITS TO TB

040752 Sink decode - ROTATE T LEFT BY 23 BITS TO TC

040753 Sink decode - ROTATE T LEFT BY 23 BITS TO TD

040754 Sink decode - ROTATE T LEFT BY 23 BITS TO TE

040755 Sink decode - ROTATE T LEFT BY 23 BITS TO TF

040756 Sink decode - ROTATE T LEFT BY 23 BITS TO LA

040757 Sink decode - ROTATE T LEFT BY 23 BITS TO LB

040758 Sink decode - ROTATE T LEFT BY 23 BITS TO LC

040759 Sink decode - ROTATE T LEFT BY 23 BITS TO LD

040760 Sink decode - ROTATE T LEFT BY 23 BITS TO LE

040761 Sink decode - ROTATE T LEFT BY 23 BITS TO LF

040762 Sink decode - ROTATE T LEFT BY 23 BITS TO CA

040763 Sink decode - ROTATE T LEFT BY 23 BITS TO CB

040764 Sink decode - ROTATE T LEFT BY 23 BITS TO CC

040765 Sink decode - ROTATE T LEFT BY 23 BITS TO CD

040770 SHIFT T BY 1 BIT TO FU failed. T= @FFFFFF@ and FB was not found equal TO @E00000@.

040771 SHIFT T BY 2 BITS TO FT failed. T= @000001@. FT should be @4@.

040772 ROTATE T BY 4 TO FLC failed. T=@A00000@. FLC should be @A@.

040773 ROTATE T BY 8 BITS TO FLD failed. T=@050000@. FLD should be @5@.

040774 ROTATE T BY 4 TO FLE failed. T=@A00000@. FLE should be @A@.

040775 ROTATE T BY 8 BITS TO FLF failed. T=@050000@. FLF should be @5@.

040780 Sink decode - ROTATE T LEFT BY 23 BITS TO FA.

040790 Sink decode - ROTATE T LEFT BY 23 BITS TO FB.

040800 Sink decode - ROTATE T LEFT BY 23 BITS TO BR.

040810 Sink decode - ROTATE T LEFT BY 23 BITS TO LR.

040820 Sink decode - ROTATE T LEFT BY 23 BITS TO TAS.

040830 Sink decode - ROTATE T LEFT BY 23 BITS TO FL.

040840 Sink decode - ROTATE T LEFT BY 23 BITS TO M.

040850 EXTRACT FROM T TO X with T= zero failed. The EXTRACT micro in FL was OR-ed to a NOP in M for execution. The EXTRACTION FIELD POINTER (hdwr bits 11-7 of the EXTRACT micro) is counted down from 24 TO 0. The EXTRACTION FIELD WIDTH (hdwr bits 4-0) is counted down from 24 TO 0.

040860 Same as 450 using a pattern of @FFFFFF@. MSKY is used to check EXTRACT T.

040870 Same as 450 using a pattern of @AAAAAA@. ROTATE Y and MSKY are used to check EXTRACT T.

040880 Same as 850 using a pattern of @555555@. ROTATE Y and MSKY are used to check EXTRACT T.

040890 Same as 850 except EXTRACT T TO Y failed using a pattern of @5A5A5@.

040892 Same as 850 except EXTRACT T TO L failed using a pattern of @123456@.

040894 Same as 850 except EXTRACT T TO T failed using a pattern of @9ABCDE@.

040900 While the above tests were executing, a sum was being accumulated on registers: CA CB CC CD TA TB TC TD TE TF LA LB LC LD LE LF FU FT FLC FLD FLE FLF BICN FLCN PERM PERP XYCN XYST. At the end of the section, a pre-calculated sum was compared with the actual sum accumulated and found to be unequal. One of the following micros failed: Run PROCESSOR TEST for isolation.

3C all variants
6C all variants
4C/5C branches

04AAAA Start of section halt.

04BBBB Unexpected halt. Type "CLEAR A 80 GO" TO restart.

SECTION 5

Processor MICROs. Run PROCESSOR TEST for isolation if failure.

HALT CODE	DESCRIPTION
050001	3D CLEAR failed to clear FA
050002	3D CLEAR failed to clear FL
050003	3D CLEAR failed to clear FU
050004	3D CLEAR failed to clear CP
050010	6D micro, COUNT FL is tested using the 4 bit function box. FL is counted from 1 to 15 and compared after each count.
050011	Same as 010 except COUNT FL UP BY 16 thru 24.
050012	Same as 010 except COUNT FL DOWN is tested.
050013	Same as 012 except COUNT FL DOWN is tested.
050014	FL NEQ 0 failed. FL was set to 0, and FL NEQ 0 was found to be true.

050015 FL NEQ 0 failed. With FL= FFFF, FL NEQ 0 was found false.

050016 FL NEQ 0 failed. A single true bit was moved to FL. FL NEQ 0 was not found true.

050017 With FL= 0 a 6D, COUNT FL DOWN (amount in L) caused FL to change. FL should remain = 0.

050020 COUNT FA UP failed.

050025 Same as 010 except the upper 16 bits of FA are tested and FL is not used.

050030 With FA= @FFFFFF@ A COUNT FA UP BY 1 did not cause FA to reset to zero.

050040 COUNT FA DOWN failed.

050050 Same as 040 except the upper 16 bits of FA are tested and FL is not used.

050055 COUNT FL UP BY values 25 thru 31 (in FA) failed to count FL only by 24 (from @FFE8@ to @0000@).

050060 COUNT FA UP BY CPL failed.

050070 Same as 060 except COUNT FL UP failed.

050080 COUNT FA DOWN BY CPL failed

050090 COUNT FL DOWN BY CPL failed.

050100 COUNT FA UP AND FL DOWN BY CPL failed. The FA portion is incorrect.

050110 Same count micro as 100 but FL part is wrong.

050120 COUNT FA DOWN AND FL UP BY CPL failed. The FA portion is incorrect.

050130 Same count micro as 120 but FL part is wrong.

050140 COUNT FA AND FL DOWN BY CPL failed. The FA portion is incorrect.

050150 Same count micro as 140 but FL part is wrong.

050170 The next micro following the "BIAS BY UNIT TEST", with FU equal to zero, was not executed. It should have been.

050180 CP was not found equal to zero after a "BIAS BY UNIT TEST" with FU equal to zero.

050190 CP was not found equal to zero after a "BIAS BY UNIT" with FU equal to zero.

050195 A "BIAS BY UNIT TEST" failed to skip when CPL was not equal to 0.

050200 CPU was not found equal to zero after a "BIAS BY UNIT" when FU was not equal to 4 or 8.

050210 CPU was not found equal to 1 after a "BIAS BY UNIT" with FU equal to 4 or 8.

050220 CPL was not found set to the proper value after A "BIAS BY UNIT".

050230 The micro after a "BIAS BY F TEST", with FL = a non-zero value, was not skipped.

050240 With FU= 0, CPU was not found equal to zero after a "BIAS BY F".

050250 Same as 220 except a "BIAS BY F" was executed.

050255 a "BIAS BY F TEST" failed to skip when CPL NEQ 0.

050260 Same as 200 except a "BIAS BY F" was executed.

050270 Same as 210 except a "BIAS BY F" was executed.

050280 Same as 220 except a "BIAS BY F" was executed.

050290 The micro following a "BIAS BY S TEST", with SFL = a non-zero value, was not skipped.

050300 CPU was not found equal to zero after a "BIAS BY S". SFU is saved in FU.

050310 CPL NEQ the proper value after a "BIAS BY S".

050315 "BIAS BY S TEST" failed to skip when CPL NEQ 0.

050320 CPU was not found equal to zero after a "BIAS BY S" when SFU was not 4 or 8. SFU is saved in FU.

050330 CPU was not found equal to a 1 after a "BIAS BY S" with SFU equal to 4 or 8. SFU is saved in FU.

050340 Same as 220 but "BIAS BY S" used. SFL in FL.

050350 The next micro following a "BIAS BY F AND S TEST" with SFL= 0, FL= a non-zero value was not skipped.

050360 CP NEQ 0 after a "BIAS BY F AND S TEST" with SFL equal to zero and FL not equal to zero.

050370 The MICRO following "BIAS BY F AND S TEST", with SFL and FL NEQ 0, was executed but should not have.

050380 Same as 240 but "BIAS BY F AND S" was executed.

050390 Same as 220 but "BIAS BY F AND S" was executed.

050395 "BIAS BY F AND S TEST" did not skip for CPL NEQ 0.

050400 Same as 200 but a "BIAS BY F AND S" was executed.

050410 Same as 210 but a "BIAS BY F AND S" was executed.

050420 Same as 220 but a "BIAS BY F AND S" was executed.

050425 "BIAS BY F AND S TEST" did not skip for CPL NEQ 0.

050430 Same as 200 but a "BIAS BY F AND S" was executed.

050435 Same as 210 but a "BIAS BY F AND S" was executed.

050440 Same as 220 but a "BIAS BY F AND S" was executed.

050450 The micro following "BIAS BY F AND CP TEST", with CPL = 0, FL NEQ 0 was skipped. It should not have.

050460 CP NEQ 0 after a "BIAS BY F AND CP TEST" when CPL was 0 and FL not equal 0.

050470 The micro following a "BIAS BY F AND CP TEST", with FL and CPL NEQ 0 was not skipped.

050480 Same as 240 but "BIAS BY F AND CP" was executed.

050490 Same as 220 but "BIAS BY F AND CP" was executed.

050495 "BIAS BY F AND CP TEST" did not skip for CPL NEQ 0.

050500 Same as 200 but "BIAS BY F AND CP" was executed.

050510 Same as 210 but "BIAS BY F AND CP" was executed.

050520 Same as 220 but "BIAS BY F AND CP" was executed.

050525 "BIAS BY F AND CP TEST" did not skip for CPL NEQ 0.

050530 Same as 200 but "BIAS BY F AND CP" was executed.

050540 Same as 210 but "BIAS BY F AND CP" was executed.

050550 Same as 220 but "BIAS BY F AND CP" was executed.

050560 A BIAS micro with variant 4 TEST (@0039@) caused a skip when it should not have.

050570 Same BIAS micro as 560 but result in CPL was incorrect.

050580 A BIAS micro with variant 6 TEST (@003D@) caused a skip when it should not have.

050590 Same BIAS micro as 580 but the result in CPL was incorrect.

050600 A BIAS micro with variant 7 TEST (@003F@) caused a skip but should not have.

050610 Same BIAS micro as 600 but the result in CPL was incorrect.

050700 5E LOAD failed.

050800 4E STORE failed.

050820 7D EXCHANGE failed.

050840 8D RELATE ADD failed.

050860 8D RELATE SUBTRACT failed.

050900 While the above tests were executing, a sum was being accumulated on registers: FA FB CP SOA SOB FLCN BICN. At the end of the section, a pre-calculated sum was compared with the actual sum accumulated and found to be unequal. One of the following micros failed: Run PROCESSOR TEST for isolation.

3D CLEAR
6D COUNT FA/FL
2C, 7D, 8D, 5E, 4E scratchpad micros

05AAAA Start of section halt.

05BBBB Unexpected halt. Type "CLEAR a 80 GO" to restart.

SECTION 6

PIPELINE FLOW, WAIT LOGIC, and CONFLICTS TESTS. If failure then run the PROCESSOR TEST for isolation.

HALT CODE	DESCRIPTION
NOTE >>>	200-250 are SCRATCHPAD back to back conflict cases.
060200	MOVE BR TO S10A & MOVE S10A TO LR failed.
060210	MOVE FA TO S11B & MOVE S11B TO BR failed.
060220	MOVE FB TO S10A & MOVE S10A to FL failed.
060230	MOVE TAS TO S11B & MOVE S11B TO Y failed.
060250	MOVE NULL-A TO S11B & MOVE S11B TO Y failed.
060300	A slow source MOVE TO SCRATCHPAD failed.
060350	MOVE 4-BIT REGS OF T & L TO/FROM SCRATCHPAD failed.
060360	MOVE 4-BIT REGS OF FB TO/FROM SCRATCHPAD failed.
060370	MOVE SUM TO SCRATCHPAD failed.
060380	MOVE DIFF TO SCRATCHPAD failed.

NOTE >>> 400-490 test for correct operation of the I/O SPREADER and ENDIO logic for CA+RC, RC+CA, RC+RC.

060400 CA+RC took too many clocks.

060410 CA+RC took too few clocks.

060420 RC+CA took too many clocks.

060430 RC+CA took too few clocks.

060440 RC+RC took too many clocks.

060450 RC+RC took too few clocks.

060460 CA+RC using 2C MOVEs took too many clocks.

060470 CA+RC using 2C MOVEs took too few clocks.

060480 CA+RC using 10C MICROs took too many clocks.

060490 CA+RC using 10C MICROs took too few clocks.

060500 MOVE X TO S15B & MOVE S15B TO Y failed.

060550 MOVE FL TO SFL & 5C on FLCN slow source failed.

060560 FLCN slow source above returned bad data.

060600 MOVE A TO TAS & MOVE TAS TO Y push-pop conflict case failed to return correct data.

060700 6C SKIP into a slow source failed:

```
MICRO 3008
MICRO 6028
MICRO 1641
MICRO 56E2
ERROR HALT
ERROR HALT
```

060710 3C SKIP into a slow source failed:

```
MICRO 3000
MICRO 3071
MICRO 6CC6
MICRO 4CE2
ERROR HALT
ERROR HALT
```

060720 4C SKIP into a slow source failed:

ERROR HALT
MICRO 3071
MICRO 1641
MICRO 4CF5
MICRO C012

060730 5C SKIP into a slow source failed:

ERROR HALT
MICRO 6028
MICRO 1641
MICRO 56F5
MICRO C005

06AAAA Start of section halt.

06BBBB Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 7 - S-MEMORY TESTS

Verify all micros that function with S-memory. If failure then either PROCESSOR or MBU is suspect. Unless specified otherwise run the MBU TEST first for isolation, then the PROCESSOR TEST.

HALT CODE	DESCRIPTION
070005	MBU. The port number READ via MICRO @0008@ doesn't match the port number returned in ELOG following a forced MEMORY ERROR. Either MBU or PROCESSOR is faulty.
NOTE >>>	For halts 010 thru 090, MBU is suspect. Run MBU test.
070010	7C MICRO failed. @FFFFFF@ written from X, but data read to Y at the same address was wrong.
070020	Same as 010 but a parity error occurred. Data OK.
070030	7C MICRO failed. @000000@ written from Y but data read TO X from the same address was incorrect.
070040	Same as 030 but a parity error occurred. Data OK.

070050 7C MICRO failed. @AAAAAA@ written from T but data read to L is wrong.

070060 Same as 050 but a parity error occurred. Data OK.

070070 7C MICRO failed. @555555@ written from L but data read to T was wrong.

070080 Same as 070 but a parity error occurred. Data OK.

070090 Data FIELD LENGTH driven from MOP lines failed. @FFFFFF@ was written into memory. As the field length is counted down from 24 to 1, the number of bits read to Y should decrease by 1 but the wrong result was found.

NOTE >>> For halts 100 - 200, run PROCESSOR TEST.

070100 Data FIELD LENGTH BY CPL failed. @FFFFFF@ written to memory. CPL is counted from 24 to 1. The number of bits read to Y should decrease by 1 but the wrong result was found.

070110 A READ AND INC FA MICRO failed.

070120 Same as 110 except a READ AND DEC FA failed.

070130 A READ AND INC FL MICRO failed.

070140 Same as 130 except a READ AND DEC FL failed.

070150 READ AND INC FA AND DEC FL MICRO failed. FA is incorrect.

070160 Same as 150 but DEC FL is wrong.

070170 READ AND DEC FA AND INC FL MICRO failed. FA is incorrect.

070180 Same as 170 but INC FL is wrong.

070190 READ AND DEC FA AND DEC FL failed. DEC FA is wrong.

070200 Same as 190 but DEC FL is wrong.

070210 MBU. A 24 BIT WRITE REVERSE FROM X failed.

070220 MBU. A 24 BIT READ REVERSE TO X failed.

070230 MBU. A 24 BIT READ REVERSE TO X from address 000040 failed.

070240 MBU. At FA= 000000, @123456@ was written. At 000018, @789AB@ was written. Thus each byte can be identified. With the above data in memory a read at FA= 000000 returned incorrect data.

070250 Same data in memory as in 240.

070260 Same as 250.

070270 Same as 250.

070280 MBU. 24 bits were written from X. A read at the same address yielded incorrect data.

070290 Same as 280.

070300 Same as 280.

070310 Same as 280.

070320 MBU. 24 BIT SWAP WITH Y failed. Memory data read to Y is incorrect.

070330 MBU. Same SWAP as 320 but the write of Y to memory is incorrect.

070340 MBU. Same SWAP as 320 but a parity error occurred.

070350 PROC. 24 BIT SWAP WITH X failed. Read to X portion is incorrect.

070360 Same SWAP as 350 except in this case the write from X to memory portion is incorrect.

070370 Same SWAP as 350 but a parity error occurred.

070380 Proc. 24 BIT SWAP WITH T failed. The read to T part is wrong.

070390 Same SWAP as 380 but write from T part failed.

070400 Same SWAP as 380 but a parity error occurred.

070410 Proc. 24 BIT SWAP WITH L failed. The read to L part is wrong.

070420 Same SWAP micro as 410 but write from X is wrong.

070430 Same SWAP as 410 but a parity error occurred.

070440 Proc. 24 BIT REVERSE SWAP WITH Y failed. Read to Y part is incorrect.

070450 Same SWAP as 440 but write from Y part is wrong.

070460 Same SWAP as 440 but a parity error occurred.

070470 PROC. A SWAP WITH X was executed. Each time the FIELD LENGTH is decreased by 1. The read to X part is wrong.

070480 Same as 470 but write from X part is wrong.

070490 Same micro as 470 but parity error occurred.

070500 PROC. 24 bits of data were SWAPPED with X. The data swapped from memory to X is wrong.

070510 Same as 500 but data swapped from X to memory is incorrect.

070900 While the above tests were executing, a sum was being accumulated on registers: X Y T L FA FB BR LR PERM PERP CD INCN CP. At the end of the section, a pre-calculated sum was compared with the actual sum accumulated and found to be unequal. One of the following micros failed. Run PROCESSOR TEST.

1E DISPATCH
7C/2D
8F READ PORT NUMBER
FA/BR/LR COMPARES
10D, 11D DIAGNOSTIC MICROs

07AAAA Start of section halt.

07BBBB Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 8

Processor DISPATCH LOGIC is tested using own port number and invalid port numbers. If failure then either PROCESSOR is suspect, MBU DISPATCH LOGIC is suspect, or the MLC is becoming active when the processor port is being used.

Run PROCESSOR TEST first, then MBU TEST, then MLC TEST. If processor test fails to find indicated problem, then disconnect the MLC and run SYSTEM TEST again. If it runs then MLC is suspect.

HALT CODE	DESCRIPTION
NOTE >>>	For all halts in this section, see description above.
080110	DISPATCH READ AND CLEAR failed to clear INCN.
080120	PERM found unequal to zero following above test.
080130	DISPATCH LOCK SKIP WHEN LOCKED skipped on INCN=0
080140	INCN unequal 1 following above test.
080150	PROC. or MLC failure. Try disconnecting MLC and run again. A STOP-OP descriptor with INTERRUPT REQUEST set was DISPATCHED to the processor's port number. After a delay of 100 ms., INCN was found to be reset, indicating that some other device (MLC) erroneously accepted descriptor.
080152	See 150. INCN NEQ 3 following a DISPATCH WRITE to own port
080154	See 150. PERM unequal 0 following above DISPATCH WRITE.
080160	See 150. A DISPATCH READ failed to return L = REFERENCE ADDRESS sent. Suspect MLC.
080162	See 160. Source port # returned in T not equal to port # DISPATCHED. Suspect MLC.
080164	See 160. INCN found not = 3 following DISPATCH READ.
080166	See 160. PERM found unequal 0 following DISPATCH READ.
080170	INCN found unequal 0 following DISPATCH READ AND CLEAR
080172	PERM unequal 0 following DISPATCH READ AND CLEAR.
080174	DISPATCH WRITE failed to write correct address at location 000000 in S-memory.
080176	PERM unequal 0 following 7C READ of address 0.

080230	DISPATCH WRITE HIGH failed to set INCN equal 7.
080240	PERM unequal 0 following DISPATCH WRITE HIGH.
080250	DISPATCH READ AND CLEAR failed to return correct data into L. L should = FFFFFF.
080260	INCN found unequal to 0 following above.
080270	DISPATCH READ AND CLEAR failed to return correct data into L.
080280	DISPATCH READ AND CLEAR failed to return correct data into L.
080290	DISPATCH LOCK SKIP WHEN LOCKED skipped erroneously.
080300	DISPATCH LOCK SKIP WHEN LOCKED failed to skip.
080310	DISPATCH LOCK SKIP WHEN UNLOCKED skipped erroneously.
080320	DISPATCH LOCK SKIP WHEN UNLOCKED failed to skip.
080410	DISPATCH WRITE to own port number followed by a 7C READ from address 000018 failed to return correct data.
080420	7C READ from address 000000 failed to return correct data.
080510	DISPATCH WRITE to port = 6 failed to set INCN equal 9.
080900	While the above tests were executing, a sum was being accumulated on registers: X Y T L FA FB BR LR PERM PERP CD INCN CP. At the end of the section, a pre-calculated sum was compared with the actual sum accumulated and found to be unequal. See description of tests being performed above.
08AAAA	Start of section halt.
08BBBB	Unexpected halt. Type "CLEAR a 80 GO" to restart.

SECTION 9

PROCESSOR TO MULTILINE CONTROL TESTING. By this section, processor DISPATCH functions have been verified so if failure then MLC or MBU is likely suspect. Run MLC TEST first, then MBU TEST.

HALT CODE	DESCRIPTION
NOTE >>>	For halt codes 090100, 090105 & 090106 ports 1 and 3 are examined for multilines. If failure in these three tests then examine memory area for the saved responses from each port. Also, for tests 090106 and beyond, S09A contains the port number being tested and S12A contains all active ports found on system. At these halts the FA register contains the address of the memory area used for saves. Display this area with console READ memory. Type "SR24 <CONTENTS OF FA>", then "NEXT" to get to HARD IO area. For each port numbered 0 thru 4, 12 24-bit words are displayed on this page, reading left to right, each column is one port. Information not stored for processor ports or unused ports. Format of information displayed: Word 1: Contents of T before DISPATCH WRITE of TEST-OP Word 2: Contents of L before DISPATCH WRITE of TEST-OP Word 3: Contents of T after INTERRUPT & DISPATCH READ Word 4: Contents of L after INTERRUPT & DISPATCH READ Word 5: RS field of the TEST-OP descriptor DISPATCHED Word 6: INCN after INTERRUPT & DISPATCH READ Word 7-12: Not used will be 000000
090100	NO MLC FOUND on any port, nor was DCP found on any channel. See memory save area for stored responses on all ports.
090105	DISPATCH WRITE to an inactive port number failed to set INCN equal 9. All valid port numbers are contained in pad S12A. Current port # in S09A. Run MLC test.
090106	After a DISPATCH WRITE to a port, the LOCK bit failed to be reset, indicating that NO DEVICE WAS PRESENT, but PORT ABSENT INCN(0) was not set, indicating that the MLC is present but not responding to the DISPATCH. Current port # in S09A. Run MLC test. See memory save area
090107	See above test. After LOCK was reset by the MLC, an INTERRUPT failed to come back within 150 milliseconds from the MLC to indicate that the TEST-OP was completed. Current port # in S09A.
NOTE >>>	For the following tests pad S12A contains the ports found present. The first (left) four 4-bit fields contain port numbers where a MLC was found or equal @F@ if none found. The rightmost two 4-bit fields contain MASTER and SLAVE processor port numbers, respectively.

090110	PROC. DISPATCH READ AND CLEAR failed to clear INCN.
090120	MLC. After DISPATCH WRITE to MLC, the MLC failed to reset LOCK bit within 150 milliseconds.
090130	See 120. The MLC failed to turn the LOCK bit on again within 150 milliseconds. The OP sent is a TEST-OP.
090140	PROC. INCN failed to clear after a DISPATCH READ AND CLEAR
090150	See 120. Port number returned by DISPATCH READ & CLEAR is not the port number being used.
090160	See 150. Interrupt address returned is not correct.
090170	See 120. The RS field does not have OP COMPLETE bit on.
090180	MLC. INCN found unequal 0 after 250 milliseconds.
090190	MLC. INCN failed to clear by DISPATCH READ AND CLEAR.
NOTE >>>	MLC. For halt codes 200, 210 & 220 the following test is performed: 512 TEST-OPs are DISPATCHED to the MLC, with the REFERENCE ADDRESS being incremented by 8 each time. Then INTERRUPT ADDRESS is checked.
090200	MLC failed to INTERRUPT after the DISPATCH WRITE.
090210	MLC. IINTERUPT ADDRESS returned is incorrect.
090220	MLC. Source port number returned is incorrect.
090410	MLC. DISPATCH LOCK SKIP WHEN LOCKED failed.
090440	The MLC failed to correctly access memory. Run the MLC DIAGNOSTIC TEST for fault isolation.
09050X	The DCP on channel X does not pass the SELF TEST. Run the DCP DIAGNOSTIC TEST for fault isolation.
09AAAA	Start of section halt.
09BBBB	Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 10

MASTER PROCESSOR TO SOFT I/O TESTING

PROCEDURE: Send a TEST STATUS then a TEST-OP to every ID present, then save CA, RC and RS result word in memory area. After all channels tested, then examine responses for errors. The user must make decision based on whether one device or more than one device shows failure. If only one device failure then run that device diagnostic for isolation. If more than one device shows failure then suspect processor cards D or H.

DISPLAY: The FA register contains the address of the memory area used for saves. Display this area with console type "SR24 <contents of FA>". For each channel, 4 24-bit words are displayed, reading down on the screen. Format of information displayed:

Word 1: TEST STATUS CA: 0001 CCCC 0000 0000 0000 0001
Word 2: TEST STATUS RC: XxxS SSSS xxxx xxxx xIII IIII
Word 3: TEST OP RESULT: 1000 0000 0000 0000 1III IIII
Word 4: READ OP RESULT if DSC channel, used by SECT 11.
CCCC = channel
S SSSS = status count
III IIII = device ID

100080 An RC cycle failed to reset the bus. Following "MOVE @1C0001@ TO CMND" then "MOVE DATA TO T", another "MOVE DATA TO X" found X unequal 0. Suspect cards H, D. See "DISPLAY" above.

100100 No devices found on any channel. Suspect H card CLOCKS, cards H,D CA/RC CONTROL, or else no devices are attached See "DISPLAY" above.

100200 STATUS COUNT found unequal to 1 on one or more channels. If one device failed, suspect that device. If more than one device failed suspect D or H cards. See "DISPLAY" above.

NOTE >>> HALT CODE 100300 will only occur when program is first loaded. After having occurred once, it will not occur again unless program is restarted with "CLEAR A 80 GO".

100300 A TEST-OP was dispatched to every channel with a device shown present by a TEST STATUS. Then OP COMPLETE bits and ID FIELD compared to the ID returned on TEST STATUS. Display the saved IO responses. See above "DISPLAY".

100400 See 100300. The TABDRIVER returned with an ERROR CODE for channel 0. Run DIAGNOSTIC TEST for this device.

100401	See 100400, channel 1 device indicated an error.
100402	See 100400, channel 2 device indicated an error.
100403	See 100400, channel 3 device indicated an error.
100404	See 100400, channel 4 device indicated an error.
100405	See 100400, channel 5 device indicated an error.
100406	See 100400, channel 6 device indicated an error.
100407	See 100400, channel 7 device indicated an error.
100408	See 100400, channel 8 device indicated an error.
100409	See 100400, channel 9 device indicated an error.
10040A	See 100400, channel A device indicated an error.
10040B	See 100400, channel B device indicated an error.
10040C	See 100400, channel C device indicated an error.
10040D	See 100400, channel D device indicated an error.
10040E	See 100400, channel E device indicated an error.
10AAAA	Start of section halt.
10BBBB	Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 11

THE DSC IS TESTED WITH A DISK PACK MOUNTED. If none found then halts with LR = 110100. If other errors detected then the DSC test should be run. This section assumes a 205, 206 or 207 pack. For the lowest channel DSC found, unit 0 (SYSTEM disk), ID = 01 is tested as follows:

1) TEST STATUS to find the DSC. If NO DSC PRESENT then halt.

2) EXECUTE the following routine:

```
  INITIALIZE SECTOR B ADR = 1
.L READ SECTOR 0, 1 SECTOR, 180 BYTES TO BFR1.
  READ SECTOR B, 1 SECTOR, 180 BYTES TO BFR2
  READ SECTOR 0, 1 SECTOR, 180 BYTES TO BFR3
  COMPARE BFR1 TO BFR3
  SHIFT SECTOR B ADR LEFT BY 1
  GO TO -L 18 TIMES (UNTIL SECTOR ADR = @020000@)
```

This test will effectively test the I/O bus to the DSC and that the DSC can transfer data from the disk.

DISPLAY: The FA register contains the address of the memory area used for saves. Display this area with console type "SR24 <contents of FA>". For each channel, 4 24-bit Words are displayed, reading down on the screen. Format of information displayed:

```
Word 1:  TEST STATUS CA:  0001 CCCC 0000 0000 0000 0001
Word 2:  TEST STATUS RC:  XxxS SSSS xxxx xxxx xIII IIII
Word 3:  TEST OP result:  1000 0000 0000 0000 1Iii iiii
Word 4:  READ OP result if DSC channel, used by SECT 11.
         CCCC = channel
         S SSSS = status count
         III IIII = device ID
```

HALT CODE	DESCRIPTION
NOTE >>>	All halts in SECTION 11 will only occur once. If a disk problem is found and any halt is reported, then when program is started again, no SECTION 11 halt will be reported. Program must be reloaded or "CLEAR A 80 GO" restart performed to cause section halts to occur again
110100	NO DSC ID=01 found using TEST STATUS commands. If a DSC is known to be present, then DSC is not responding correctly. Run DSC DIAGNOSTIC. Type "GO" to skip section if no DSC present.
110200	NO UNIT found READY on any DSC channel. If units are known to be READY then have error. READY unit and type "S01A 0 GO" to retry this section. Note that ONLY READS ARE DISPATCHED TO THE DISK PACK.
11030X	DSC on channel X. TEST-OP failed to respond with OP COMPLETE bits.
11040X	DSC on channel X. A READ OP descriptor for sector 0 was sent. Driver returned with an error. Run DSC DIAG-NOSTIC.
11050X	DSC on channel X. A READ OP descriptor for a sector other than 0 was sent. Driver returned with an error. Sectors read starting at 1 and ending at 20000 HEX. Run DSC DIAGNOSTIC.

11060X DSC on channel X. A READ OP descriptor for sector 0 was sent. Driver returned with an error. Run DSC DIAGNOSTIC.

11070X DSC on channel X. DSC sector 0 was read, then another sector (starting at 000001 and progressing each pass up to 020000) was read, then sector 0 was read again. The data read in the first sector 0 read does not match the data read in the second sector 0 read. Run DSC DIAGNOSTIC test.

110900 After all the tests are completed, a checksum was accumulated on the memory data areas used in the these tests. This checksum does not compare with a previously generated sum, indicating that the DSC wrote into memory areas incorrectly. Run the DSC DIAGNOSTIC test.

11AAAA Start of section halt.

11BBBB Unexpected halt. Type "CLEAR A 80 GO" to restart.

SECTION 12

This section is divided into two subsections, one for "MCPII" environment, and a second for "CMS" enviroment. Basically these two subsections are similar and executed as follow :

- All I/O controls are scanned until a "DSC" with READY unit is found. This unit will be considered as the unit generally used for CLEAR/START operation.

- VERIFICATION OF THE PACK LABEL.

- Scan DISK DIRECTORY for DATACOM FIRMWARE:

  MCPII : "SYSTEM"/"MLFIRMWARE".
  CMS : "SYSTEST-FWAD".

- The FIRMWARE file is loaded to memory then DOWNLOADED to the DATACOM CONTROLLER (MLC PORT 1, DCP0). FIRMWARE is STARTED and, for MLC, the ODT CONFIGURATION is LOADED. A full screen of I/O status information is written then read back and compared. RESULT STATUS and DATA COMPARE ERRORS are reported.

DISPLAY: The FA register contains the address of the memory area used for saves. Display this area with console type "SR24 <contents of FA>". For each channel, 4 24-bit Words are displayed, reading down on the screen. Format of information displayed:

```
Word 1:  TEST STATUS CA:  0001 CCCC 0000 0000 0000 0001
Word 2:  TEST STATUS RC:  XxxS SSSS xxxx xxxx xIII IIII
Word 3:  TEST OP result:  1000 0000 0000 0000 1III IIII
Word 4:  READ OP result if DSC channel, used by SECT 11.
         CCCC = channel
         S SSSS = status count
         III IIII = device ID
```

HALT CODE	DESCRIPTION
NOTE >>>	Unless otherwise specified, halts in this section will only occur once. If disk problem is found any halt is reported, then when program is started again, no SECTION 12 halt will be reported. Program must be reloaded or "CLEAR A 80 GO" restart performed to cause section halts to occur again.
120010	No DSC found with a READY unit.
120020	DSC result descriptor error
120030	DSC first READY unit reported WRITE LOCKOUT. If WRITE LOCKOUT is not set then run DSC test else hit START to continue this section with WRITE LOCKOUT.
120100	INVALID DISK PACK LABEL. Valid pack must be "MCPII" or "CMS" pack. Mount valid pack then hit START, or run DSC TEST
120110	DSC pack is not an "MCPII" SYSTEM pack. Mount "MCPII" SYSTEM pack and hit START or run DSC TEST.
120120	DSC pack is not a "CMS" pack. Mount "CMS" pack and hit START, or run DSC test.
120130	MCPII error : "SYSTEM"/"MLFIRMWARE" not on disk.
120140	CMS error : "MCP" not on disk.
120150	CMS error : "SYSTEST-FWAD" file not found.

120160 MCPII error : INVALID SELF ADDRESS in directory or DISK FILE HEADER sector.

120200 Missing SERVICE REQUEST while reading disk. Run DISK DIAGNOSTIC.

120210 Invalid STC count reached while reading disk. Run DISK DIAGNOSTIC.

120220 Invalid STC count reached while reading disk. Run DISK DIAGNOSTIC.

120300 DISPATCH to MLC on port 1 failed to respond within 150 milliseconds.

120310 DISPATCH to MLC on port 1 with a LOAD-OP 600000 failed twice to return a result without an EXCEPTION BIT on. A LOAD of FIRMWARE was attempted.

120320 DISPATCH to MLC on port 1 failed to respond within 150 milliseconds. START FIRMWARE OP 610000 attempted.

120330 DISPATCH to MLC on port 1 with a START-OP 610000 failed to return without EXCEPTION BIT on.

120340 DISPATCH to MLC on port 1 failed to respond within 150 milliseconds. LOAD CONFIGURATION OP 620000 failed

120350 DISPATCH to MLC on port 1 with an OP of 620000 failed to return without EXCEPTION BIT on.

120400 TIMEOUT on FAST SELECT message to terminal $$ ODT.

120410 TIMEOUT on SEND ACK message to terminal $$ ODT.

120420 TIMEOUT on FAST SELECT message to terminal $$ ODT.

120430 TIMEOUT on SEND ACK message to terminal $$ ODT.

120440 TIMEOUT on POLL message to terminal $$ ODT.

120450 TIMEOUT on SEND ACK message to terminal $$ ODT.

120460 No EOT back after sending XMIT PAGE character to terminal, and expecting to read full page.

120470 Data sent to ODT failed to be returned correctly.

120500 DCP halt : Protocol error. Run DCP 3/4 test.

12BBBB Unexpected halt. Type "CLEAR A 80 GO" to restart.

12FFFF Operating system configuration halt.

This halt does not report a failure but only occurs when both "MCPII" and "CMS" operating system hardware environment are present in the system. Type "RD" to display the configuration instructions on the screen.

SLAVE PROCESSOR ERRORS.

If failure occurs then switch processors and either run this test again or the PROCESSOR TEST.

810010 With SLAVE running and on-line, the MAC command, GET.STATUS.VECTOR (MOVE 000002 TO CNS), was executed and CNS loaded into T-register. T(16) was found equal to 0, indicating SLAVE is off-line. Either the SLAVE is actually off-line, in which case put the SLAVE on-line and "GO", or the MAC card H9 is suspect, or the MAC command GET.STATUS.VEXTOR is not working correctly. If SLAVE is offline or not present, INCN will set = 9. If SLAVE is online, then INCN will set = 3 on DISPATCH.

810020 Continued from above. T(20) found equal to 1, indicating that SLAVE processor is not running. The MAC card H9 is suspect, GET.STATUS.VECTOR is not working correctly.

810030 MAC card H9 is suspect. The following sequence resulted in a halt, but should not have: ENABLE (MOVE @81@ TO CNS), HALT.RESTART (MOVE @40@ TO CNS), HALT.SLAVE (MOVE @03@ TO CNS), HALT micro.

810040 SLAVE was halted with CNS.HALT.SLAVE, then STATUS.VECTOR was read to T. T(20), SLAVE running bit, was found to be on. Suspect MAC card H9.

810050 See 810030. Same sequence was executed and halt occurred erroneously. Suspect MAC H9 card.

810060 SLAVE port number found to be same as MASTER port number. Either SLAVE READ.PORT.NUMBER 8F MICRO failed or else SLAVE port number is incorrectly jumpered on D-card.

810070 SLAVE DISPATCH WRITE to the MASTER failed, or SLAVE processor hung up with error. Switch processors and run either this test again or PROCESSOR TEST.

810080 CNS.GET.STATUS.VECTOR failed to report that SLAVE is not present. If SLAVE is actually present, then SLAVE processor is hanging up somewhere in lower memory. Suggest that PROCESSOR TEST be run on SLAVE processor. Otherwise suspect MAC card (H9).

810090 SLAVE processor READ.PORT.NUMBER 8F MICRO failed.

810100 Responding to the MASTER's first DISPATCH to SLAVE, the SLAVE failed to correctly ECHO L-address. Suspect SLAVE DISPATCH micro failed. Run SYSTEM TEST with SLAVE equal MASTER.

810110 SLAVE processor micros failure. Run PROCESSOR TEST on SLAVE processor.

810120 The SLAVE is halted with CNS.HALT.SLAVE (MOVE @03@ TO CNS) then DISPATCH WRITE to the SLAVE. PORT ABSENT bit should have been turned on in MASTER INCN but wasn't.

810130 See above test. Following that test, CNS.HALT.RESTART (MOVE @40@ TO CNS) and a HALT micro failed to restart the SLAVE. Suspect MAC H9 card.

810140 LOCK bit found on following DISPATCH READ AND CLEAR. Suspect SLAVE processor. Run this test with SLAVE = MASTER

810142 SLAVE failed to respond to MASTER DISPATCH WRITE. Run SYSTEM TEST again with SLAVE as MASTER.

810144 SLAVE failed to correctly ECHO L-address sent by MASTER with DISPATCH WRITE. L SENT = 000000, L = DATA RECEIVED.

810150 LOCK bit found on following DISPATCH READ AND CLEAR. Suspect SLAVE processor. Run this test with SLAVE = MASTER

810152 SLAVE failed to respond to MASTER DISPATCH WRITE. Run SYSTEM TEST again with SLAVE as MASTER.

810154 SLAVE failed to correctly ECHO L-address sent by MASTER with DISPATCH WRITE. L sent = FFFFFF, L = DATA RECEIVED.

810160 LOCK bit found on following DISPATCH READ AND CLEAR. Suspect SLAVE processor. Run this test with SLAVE = MASTER

810162 SLAVE failed to respond to MASTER DISPATCH WRITE. Run SYSTEM TEST again with SLAVE as MASTER.

810164 SLAVE failed to correctly ECHO L-address sent by MASTER with DISPATCH WRITE. L sent = AAAAAA, L = DATA RECEIVED.

810170 LOCK bit found on following DISPATCH READ AND CLEAR. Suspect SLAVE processor. Run this test with SLAVE = MASTER

810172 SLAVE failed to respond to MASTER DISPATCH WRITE. Run SYSTEM TEST again with SLAVE as MASTER.

810174 SLAVE failed to correctly ECHO L-address sent by MASTER with DISPATCH WRITE. L sent = 555555, L = data received.

810180 SLAVE processor READ.PORT.NUMBER 8F MICRO failed.

810190 SLAVE processor 8F MICRO returned a port number in TF that doesn't match the port number obtained by forcing a memory error and then extracting the port number from the ELOG into Y-register. Run PROCESSOR TEST on SLAVE.

810200 SLAVE was found with INCN(3) on. Run PROCESSOR TEST.

810210 SLAVE didn't interrupt within 10 seconds. If SLAVE is OFFLINE, put it ONLINE and enter GO. If SLAVE is ONLINE, run test again with SLAVE as MASTER.

810300 Processor problem, run PROC. TEST with SLAVE processor as MASTER. 8C MICRO failed.

810310 Processor problem, run PROC. TEST with SLAVE processor as MASTER. 9C MICRO failed.

810320 Processor problem, run PROC. TEST with SLAVE processor as MASTER. 1C MICRO failed.

810330 Processor problem, run PROC. TEST with SLAVE processor as MASTER. X, Y, or TAS registers failed.

810335 Processor problem, run PROC. TEST with SLAVE processor as MASTER. 2C MICRO or pads failure.

810340 Processor problem, run PROC. TEST with SLAVE processor as MASTER. Memory MICROs failed.

810350	Processor problem, run PROC. TEST with SLAVE processor as MASTER. 8F MICRO failed to return correct port number.
810360	Processor problem, run PROC. TEST with SLAVE processor as MASTER. 1E DISPATCH MICRO operations failed. If no failure found, then run MBU TEST. If no failure found, disconnect the MLC and run tests again.
820010	Processor error, run PROCESSOR TEST on SLAVE. OR-with-M failed.
820020	Processor error, run PROCESSOR TEST on SLAVE. 3C MICRO failed.
820030	Processor error, run PROCESSOR TEST on SLAVE. 4C or 5C MICRO failed.
820040	Processor error, run PROCESSOR TEST on SLAVE. 6C MICRO failed.
820050	Processor error, run PROCESSOR TEST on SLAVE. 6D MICRO failed.
820060	Processor error, run PROCESSOR TEST on SLAVE. 10C MICRO failed.
830010 thru 83BBBB	SLAVE executing SECTION 3. See SECTION 3 halt codes 030210 thru 03BBBB for error description.
840210 thru 84BBBB	SLAVE executing SECTION 4. See SECTION 4 halt codes 040210 thru 04BBBB for error description.
850170 thru 85BBBB	SLAVE executing SECTION 5. See SECTION 5 halt codes 050170 thru 05BBBB for error description.
860200 thru 86BBBB	SLAVE executing SECTION 6. See SECTION 6 halt codes 060200 thru 06BBBB for error description.
870010 thru 87BBBB	SLAVE executing SECTION 7. See SECTION 7 halt codes 070010 thru 07BBBB for error description.
880110 thru 88BBBB	SLAVE executing SECTION 8. See SECTION 8 halt codes 080110 thru 08BBBB for error description.

890105 thru 89BBBB	SLAVE executing SECTION 9. See SECTION 9 halt codes 090105 thru 09BBBB for error description.

MISCELLANEOUS HALT CODES

A1111A	START OF PROGRAM PASS HALT.
B1111B	UNEXPECTED HALT IN CASE 1
B2222B	UNEXPECTED HALT IN CASE 2
B3333B	UNEXPECTED HALT IN CASE 3
B4444B	UNEXPECTED HALT IN CASE 4
BBBBBB	UNEXPECTED PROGRAM HALT. Type "CLEAR A 80 GO" for HARD RESTART.
CCCCCC	END OF PROGRAM HALT. Type "GO" to run again. To run with different options, hold down console INTERRUPT and press START.

NOTE >>> A record of I/O devices present and results of a TEST STATUS command CA/RC cycle and a TEST-OP descriptor is available in memory for display. The FA register contains the address of the memory area used for saves. Display this area with console type "SR24 <contents of FA>". For each channel, 4 24-bit Words are displayed, reading down on the screen. Format of information displayed:

```
Word 1:  TEST STATUS CA: 0001 CCCC 0000 0000 0000 0001
Word 2:  TEST STATUS RC: XxxS SSSS xxxx xxxx xIII IIII
Word 3:  TEST OP result: 1000 0000 0000 0000 1III IIII
Word 4:  READ OP result if DSC channel, else = 0
         CCCC = channel
         S SSSS = status count
         III IIII = device ID
```

(continued next page)

Next in memory is the HARD I/O saved responses area. To display this area type "NEXT". For each port numbered 0 thru 4, 12 24-bit Words are displayed. Processor port(s) information is not stored. Format of information displayed:

Word 1: Contents of T before DISPATCH WRITE
Word 2: Contents of L before DISPATCH WRITE
Word 3: Contents of T after DISPATCH WRITE & READ
Word 4: Contents of L after DISPATCH WRITE & READ
Word 5: RS field results of the TEST-OP descriptor
Word 6: INCN after DISPATCH READ
Word 7-12: Not used will be 000000

If no I/O device responses are listed and I/O devices are known to be attached, then suspect cards D & H.

EEEEEE CONSOLE INTERRUPT is on. ENTER OPTIONS HALT. Program scratchpads and program options in S01A may be changed. Type "GO" to continue.

NOTES

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