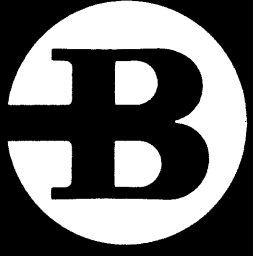
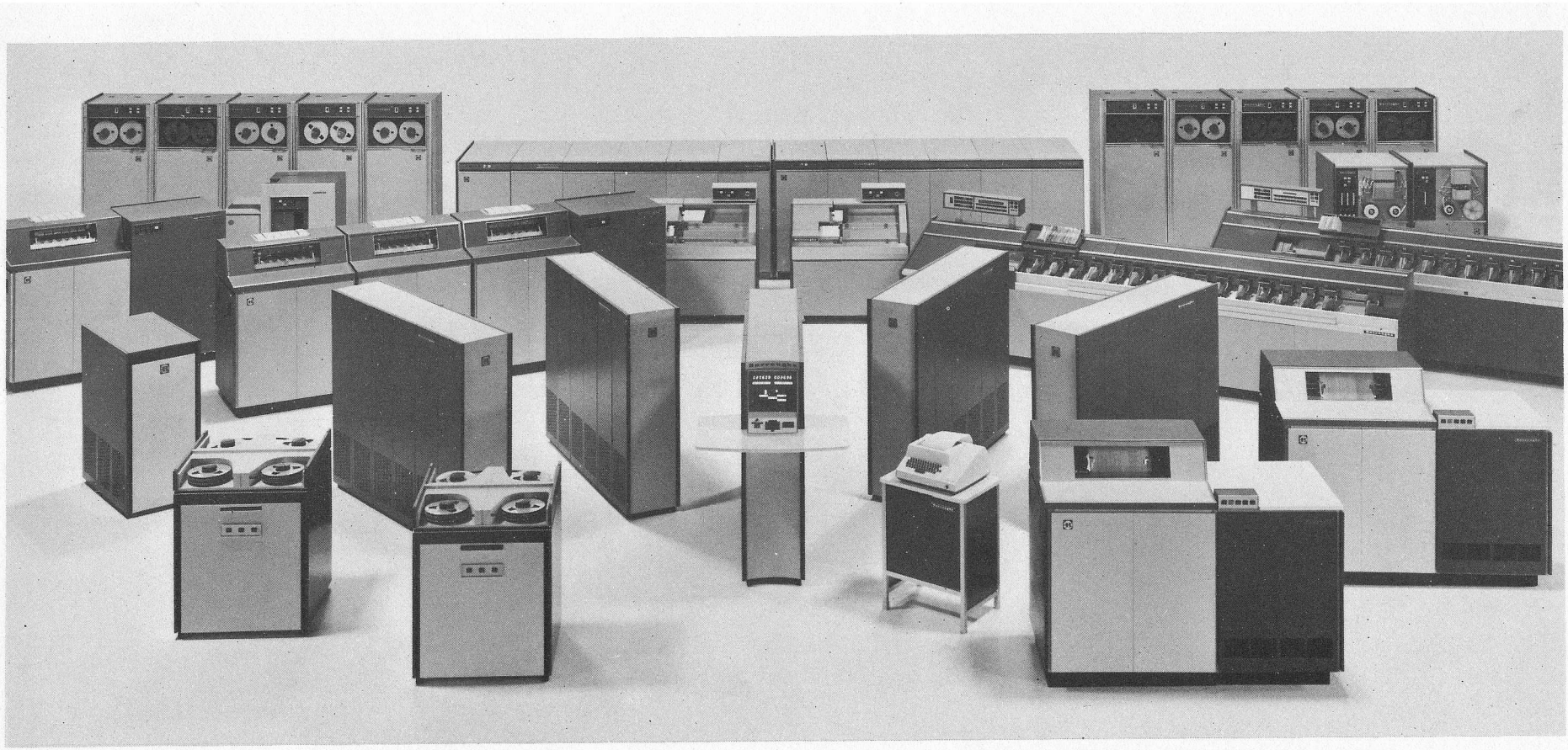
Burroughs

B 2500 and B 3500 SYSTEMS

REFERENCE MANUAL





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B 2500 and B 3500 SYSTEMS REFERENCE MANUAL

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INTRODUCTION

The Burroughs B 2500/B 3500 Systems offer a totally integrated hardware/software design that incorporates monolithic, solid-state circuitry and high-speed disk capabilities, along with years of experience in the art of machine/man interface to create an unparalleled system for the dollar investment involved. The B 2500 and B 3500 Systems are completely compatible in either direction, with the basic differences in the two systems being internal speed, maximum peripheral component capacity, and maximum memory capacity. Because of these slight differences, the statements contained within this manual apply to both systems unless otherwise noted.

The B 2500 and B 3500 Systems are character-oriented toward business and data communications applications. They consist of highly efficient modular hardware/software, plus a wide range of exceptional peripheral devices that fulfill the sophisticated requirements involved to solve the data gathering and immediate response requirements that confront data processing installations today and in the near future.

This new level of computer responsiveness to business, as well as scientific problems, is available to even the smallest organization with a requirement for electronic data processing. Speed and flexibility are the key words which describe these systems. To support this statement, Burroughs offers:

a. Extremely fast hardware speeds, some measured in billionths of a second.

b. The ability to do many unrelated jobs at the same time in a truly multiprocessing mode and to continue doing them without interruption, even if a rush job is dropped in on the spur of the moment. Multiple compilations of COBOL symbolic programs, along with multiple compilations of FORTRAN, or any other mix, can be accomplished in the same run with operational programs.

c. An unprecedented degree of self-regulation in low cost computer systems.

d. Programing so simple that it can be started by one programmer and finished by another, or divided up between programmers and then integrated by the Operating System.

e. Higher-level programing languages which save time and money as well as improved communication by removing the machine language curtain between those who understand the in-house problem and those who understand the computer.

f. A special suitability to real time, data communications, and time sharing problems.

g. The ability to accommodate the fastest random access disk file on the market in a simple and direct manner.

h. From 4 to 20 input/output channels, all of which may be active simultaneously and still leave ample time free for computation.

It is the purpose of this manual to acquaint the reader with the hardware and associated components offered by Burroughs Corporation which are applicable to the B 2500 and B 3500 Systems.

For detailed information pertaining to programing, the reader should refer to the appropriate B 2500/B 3500 software manuals.

SECTION 1
GENERAL DESCRIPTION

GENERAL

This section contains an overall description of the B 2500 and B 3500 Data Processing Systems, without explaining the specifics of the internal machine logic. The systems are designed for modularity, utilizing silicon solid-state, monolithic circuitry. Integrated with the hardware is a modular software system, making the B 2500 or B 3500 an effective and flexible data processing system. Incorporated in the hardware are features such as positive memory protection, an automatic interrupt system, variable length instructions and data fields, decimal addressing and arithmetic, and many other features that will be discussed in this manual. The hardware has been designed to facilitate the integration of the software system, a necessity for today's data processing system. This concept has created a more efficient and effective hardware/software data processing system than any other system, within its price range, on the market today.

SYSTEM CONFIGURATION

The B 2500 and B 3500 Systems consist of the processor, central control, core memory, power control and supplies, input/output channels, and input/output controls. The equipment is modular and can utilize any desired peripheral units within the scope of the input/output channel and control. The minimum to maximum central system configurations of the B 2500 and B 3500 are shown in tables 1-1 and 1-2 respectively.

Table 1-1
B 2500/B 3500 2-Cabinet System Configuration Chart

Description	Minimum	Maximum	Remarks
Processor	1	1	Includes Display and Control Panel, and AC Power Supply
Central Control and Memory Base	1	1	10K to 60K bytes and can accommodate up to 3 large and 3 small I/O controls
Address Memory	24 words	24 words	24 words are included within the processor and are sufficient for the 6 I/O controls
Input/Output Channel	4	6	
Input/Output Controls	1	6	Dependent on peripheral devices on system

Table 1-2
B 2500/B 3500 3-Cabinet System Configuration Chart

Description	Minimum	Maximum	Remarks
Processor	1	1	Includes Display and Control Panel
Central Control B	1	2	Each control can accommodate 10 I/O controls

Table 1-2 (cont)
B 2500/B 3500 3-Cabinet System Configuration Chart

Description	Minimum	Maximum	Remarks
Memory Module Base B	.1	4	10K to 500K bytes; a maximum of 3 cabinets; a maximum of 150K for first 2 cabinets and 200K for third cabinet
Auxiliary Cabinet	0	2	Contains exchanges and multiline extensions
Address Memory	24 words	120 words	8 extensions each containing 12 words; the multiline control with all of the multiline extensions requires 6 Address Memory Extensions
AC Power Supply	1	2	Modular depending on number of cabinets; 4-6 cabinets require 1; 7-9 cabinets require 2
DC Power Supply			Modular depending on system demands; installed in Memory Base B if exchanges or multiline extensions are in Memory Base B; not required in Auxiliary Cabinet
Input/Output Channel	6	20	
Input/Output Controls and Exchanges		20 controls; multiline control reduces maximum to 19	Dependent on peripheral and I/O channel configuration and needs of user

The maximum number and types of peripheral units that can be used on a system is a function of the number of input/output channels and the number of input/output controls and/or exchanges that comprise the central system.

CENTRAL SYSTEM CABINETS

Modular cabinets are used to contain all central system modules. One or more cabinets can be used, as required, for housing the modules in a given configuration. Cabinet dimensions are approximately:

a. 17.3 inches wide.

b. 60.5 inches high.

c. 77.5 inches long.

There are five cabinets in the central system which are:

a. Processor.

b. Central control and memory base.

c. Central Control B.

d. Memory Base B.

e. Auxiliary.

A B 2500 System consists of one processor cabinet, and one central control and memory base cabi-

net. The maximum length of the coaxial cable between these two cabinets is 35 feet (25 feet is standard).

A B 3500 System consists of one processor cabinet, at least one and at most two Central Control B cabinets, and at least one and at most four Memory Base B cabinets. The maximum length of the coaxial cables between any two of these cabinets is 35 feet (25 feet is standard). Up to two auxiliary cabinets may be added, as required. The upper limit of coaxial cable length to the auxiliary cabinet depends on the cabinet, as follows:

a. Multiline extension (35 feet is maximum – 25 feet is standard).
b. Disk file exchange, 2 x 10 or 4 x 10 (50 feet maximum).
c. Terminal unit exchange, 1 x 9 (50 feet maximum).
d. Magnetic tape exchange No. 1. (50 feet maximum).

Processor Cabinet

The processor cabinet includes:

a. The processor.
b. An operator console.

The processor cabinet also houses the following adapters:

a. Floating point adapter or floating point jumper. Processor models 1 and 2A require the floating point jumper adapter if no floating point adapter is present.
b. Address memory extension adapters.
c. One B 2500 or B 3500 adapter (required).
d. One multiline (ML) control processor adapter is required if a ML control is attached to the system.
e. One multiline extension (MLE) address memory driver adapter for each ML extension (as required).
f. Terminate-driver adapters 2 and 3 and channel read adapter (as required).

Central Control and Memory Base Cabinet

This cabinet includes:

a. Central Control A.
b. Memory Base A.
c. Three large control channels (numbered 0, 1, and 2).
d. Two left-hand control channels (numbered 3 and 4).
e. One right-hand control channel (numbered 5).

In addition, the central control and memory base cabinet may house the following modules or adapters:

a. One BCL/EBCDIC translator or BCL/EBCDIC jumper adapter. The system requires a choice of one.
b. Up to six input/output (I/O) controls and associated adapters listed in table 1-3, three of which are selectable from Large Controls or Left-Hand Controls, one of which is selectable from Right-Hand Controls, and two of which are selectable from Left-Hand Controls.

NOTE

When a selection is made from Left-Hand Controls for use in a large control channel, a central control and memory base extender are required.

c. Up to two memory modules.
d. One magnetic tape, disk file, or terminal unit exchange (in lieu of second memory module).
e. One power compatibility kit, if required.

Table 1-3
Selectable Input/Output Controls

Large Controls	Right-Hand Controls	Left-Hand Controls
Magnetic tape	Card reader	Card reader
Disk File	Card punch control no. 1	Paper tape reader
Single line	Paper tape reader	Buffered printer
Multiline	Paper tape punch	Console printer
(counts as two controls)	Buffered printer	Reader Sorter

Table 1-3 (cont)
Selectable Input/Output Controls

Large Controls	Right-Hand Controls	Left-Hand Controls
	Console printer Lister Reader Sorter Terminal unit Unbuffered printer Card punch control no. 2	Unbuffered printer Card punch control no. 1 Card punch control no. 2

Central Control B Cabinet

This cabinet includes:

a. Central Control B.

b. Five large control channels (numbered 0 through 4 or 10 through 14).

c. Five small control channels (numbered 5 through 9 or 15 through 19).

In addition, the Central Control B cabinet may house the following modules:

a. Up to ten I/O controls and associated adapters listed in table 1-3, five of which are selectable from Large Controls or Left-Hand Controls, and five of which are selectable from Right-Hand Controls.

NOTE

When controls are selected from Left-Hand Controls, each selection requires a Central Control B extender.

b. One AC module, if required.

c. One BCL/EBCDIC translator or BCL/EBCDIC jumper adapter.

d. One power compatibility kit, if required.

Memory Base B Cabinet

This cabinet includes Memory Base B and may house the following modules in various combinations:

a. One to five memory modules. A memory extension adapter is required when more than two memory modules are installed.

b. 2 x 10 disk file exchange. A 2 x 10 disk file exchange occupies either the fourth or fifth position and precludes the use of the fifth position by a memory module.

c. One magnetic tape or terminal unit exchange. A magnetic tape or terminal unit exchange occupies the fifth position.

d. One to four multiline extensions. A multiline extension can occupy any position and precludes the use of higher positions by memory modules.

e. 4 x 10 disk file exchange. A 4 x 10 disk file exchange occupies either the fourth or fifth position. If it is the fourth position, it precludes use of the fifth position by a memory module.

f. One power module (either AC or DC), if required. A DC power module is required if b, c, or d exists and excludes the AC power module. If the AC power module is required, it must be contained in Central Control B.

g. One power compatibility kit, if required.

Auxiliary Cabinet

This cabinet may house the following modules (permitted combinations depend upon the number of cables associated with the cabinet):

a. Terminal unit exchange.

b. Disk file exchange, 2 x 10.

c. Disk file exchange, 4 x 10.

d. Magnetic tape exchange.

e. Multiline extensions.

f. Lockout memory.

g. Disk file exchange, 4 x 20.

h. AC power module, if required.

i. Power compatibility kit, if required.

WEIGHTS OF SYSTEM COMPONENTS

For planning purposes, the following estimates of system component weights may be used:

a. Any cabinet fully loaded – processor, Central Control B, or central control and memory base (600 to 700 pounds).

b. Tape cluster – four stations (600 to 700 pounds).

c. Line printer (1530 pounds).

d. System memory (325 pounds).

e. Console printer (SPO) – without stand (40 pounds).

DATA REPRESENTATION

The decimal addressing technique used in core memory allows data to be addressed in variable-length fields of 16-bit words, 8-bit (byte) or 4-bit (digit) units. Even though memory is addressable to a digit position, memory is accessed by means of a 2-byte word, plus a parity bit. Internally, the processor is capable of operating with any 8-bit code, two of which are programmatically selectable (EBCDIC and USASCII).

EBCDIC Internal Code

One of the codes of the B 2500 and B 3500 is the 8-bit Extended Binary Coded Decimal Interchange Code (EBCDIC). This is the standard internal code and is programmatically selectable (see appendix D).

USASCII Internal Code

The other programmatically selectable code which the processor uses is the United States of America Standard Code for Information Interchange (USASCII). This code is an 8-bit extension of the standard 7-bit ASCII code (refer to appendix D).

BCL Input/Output Code

The present Burroughs Common Language code (BCL) is optionally provided as an input/output code. A translator located in central control will automatically translate BCL to EBCDIC on input operations, and EBCDIC to BCL during output operations when required. Refer to appendix D for a list of BCL codes.

Digits

More efficient utilization of memory can be made if numeric data is compressed into 4-bit fields, which is allowed on B 2500 and B 3500 Systems. One byte position in memory may contain two binary coded decimal (BCD) digits. The commands of the B 2500 and B 3500 allow a programmer to generate numeric digit fields from EBCDIC or USASCII information, perform calculations, and generate an EBCDIC or USASCII coded result. If a 4-bit field is moved to an 8-bit EBCDIC or USASCII field, the four most significant bits of each 8-bit character will be automatically set to values required by the numeric subset of the internal code selected by the programmer.

Floating Point Representation

In addition to fixed point arithmetic, the B 2500 and B 3500 Processors are capable of performing floating point arithmetic. If floating point arithmetic is used, the numeric data must be in the specific format shown in figure 1-1.

The first digit (D1) of the field is the sign of the exponent and specifies whether the exponent is positive or negative. The actual value of the exponent is contained in the second and third digit (D2 and D3) positions of the field. The first three digits allow the exponent value to range from -99 to +99, a very large range. The fourth digit (D4) always indicates the sign of the mantissa. The mantissa is variable in length from 1 to 100 and is contained in positions D5 through Dn, as required. The mantissa is always a whole number with the decimal point assumed to the right of the last digit. Several examples of floating point data are shown in table 1-4.

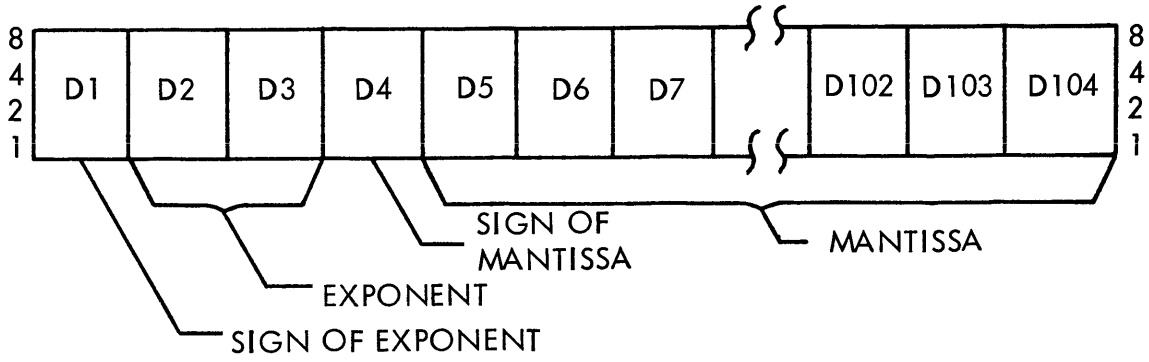

Figure 1-1. Floating Point Data Format

Table 1-4
Floating Point Representation

Value	Floating Point Data
+123	+00+123
-1.23	-02-123
+0.0057	-04+57
-9.786×10^{-6}	-09-9786
$+3.75 \times 10^{6}$	+04+375

FUNCTIONS OF MAJOR UNITS

Core Memory

The memory consists of a highly modular group of components to provide a variety of memory sizes for both the B 2500 and B 3500 Systems. Each B 2500 System may have memory sizes ranging from 10,000 bytes to 60,000 bytes in increments of 10,000 bytes. Each B 3500 System may have memory sizes of from 10,000 bytes to 500,000 bytes in variable increments. The increments of the B 3500 core memory are as follows:

From	To	Byte Increment(s)
10,000	90,000	10,000
90,000	240,000	30,000
240,000	360,000	60,000
360,000	450,000	90,000
450,000	500,000	50,000

Decimal addressing allows for addressing any single digit within core memory. Even though a digit position can be addressed, the memory access is made on the word in which the digit is located. A B 2500 or B 3500 word consists of two bytes and a parity bit (16 bits plus parity). Whenever a byte is addressed, the decimal address must be an even address. Whenever a word is addressed, the decimal address must be divisible by four. The memory cycle time for one word is one microsecond on the B 3500. The B 2500 has a word cycle time of two microseconds.

Address Memory

Address memory is a modular array of storage registers. Each register within the array consists of a 6-digit word capable of containing an address. Each B 2500 or B 3500 System includes 24 words of address memory. Six words are used by the processor to store the three addresses and other logical requirements of an instruction. Two words contain the real-time clock and the control time interval used by the software. The remaining 16 words are used in pairs by the input/output channels for I/O operations. A total of eight address memory extensions, each consisting of 12 words, can be added to a B 3500 System. Therefore, address memory is modular from 24 to 120 words in increments of 12 words. The addition of input/output channels may require the addition of the address memory extensions.

Central Control

The central control essentially provides:

a. Priority resolution between controls within central control.

b. Result descriptor address generation for the controls.

c. For lines from the processor which are used when a control is initiated (control has not requested memory access).

d. A common buss which is shared by all of the controls.

e. An interface to Address Memory in the processor for the purpose of manipulating addresses.

f. A standard interface to each control attached.

g. Provision for a BCL/EBCDIC translator.

Control priority within a central control cabinet is changeable. Central control requests access from the highest to the lowest priority, one at a time.

Priority between central control cabinets is determined in the central processor. There are equal levels of priority between central control cabinets. Access is granted to the central control which was not granted the last access by the logic in the processor.

Access is granted to the processor if, and only if, no requests are made by a central control.

TRANSLATOR

A plug-in translator is provided optionally as a part of central control. The translator can provide BCL to EBCDIC translation of data as it is transferred from an input unit to main memory. The translation of EBCDIC to BCL can also be made on information being transferred from main memory to an output device. For each transfer through central control, a signal from the requesting I/O control indicates whether the data is to pass through or bypass the translator. Since the translation is accomplished by the hardware, there is no slowdown in the transfer process. All EBCDIC codes outside the graphic set are translated to the BCL code for a question mark. A substitution is made when there is no conflict, i.e., the BCL graphic is not contained in the EBCDIC graphic set, and vice-versa.

Processor

The processor contains the necessary logic and circuitry to execute all instructions. It can operate in any one of four states:

a. Control state, zero base – the interrupt flip-flop can be set, but the interrupt branch is not executed until the return to normal state. Privileged instructions are allowed.

b. Control state, non-zero base – the interrupt flip-flop can be set, but the interrupt branch is not executed until the return to normal state. Privileged instructions are disallowed.

c. Normal state, zero base – the interrupt branch is allowed to be executed, and privileged instructions are allowed.

d. Normal state, non-zero base – the interrupt branch is allowed to be executed, and privileged instructions are disallowed.

NOTE

Some error conditions which result in a processor result descriptor being stored will not set the interrupt flip-flop, but the interrupt branch is executed directly.

Object programs, assemblers, compilers, generators, etc., are executed in the normal state, non-zero base, whereas most of the Master Control Program is executed in the control state, zero base. A small set of privileged instructions (used exclusively by the Master Control Program) can only be executed in zero base. This set includes such commands as Initiate Input/Output and Read Timer.

Automatic interrupt detection is an integral part of the processor whenever the processor is operating in a normal state. When a result descriptor is generated and stored, an interrupt occurs after the current instruction is completed.

The processor is changed to operate in control state, zero base and an automatic branch is executed to the interrupt handling routine of the software after storing the return point and logical registers for program reentry. Result descriptors contain the information necessary to determine the type of interrupt that occurred.

LOGICAL UNITS

Included in the processor are logical units that are used or changed by instructions. All instruction addresses, and the data field addresses within the instructions, are relative to a base register. The base register is added to all instruction addresses to create the absolute memory address of an instruction or data field. The base register value is set by the Master Control Program. There are also three index registers available to every pro ram being operated. Thus, the absolute memory address can consist of the algebraic sum of the base register, the relative address, and one of the three index registers. To ensure memory protection, a program also has a limit address register that is set by the software. All memory addresses are checked automatically to determine if the address is within the bounds of the base and limit address registers.

Other logical units utilized are the overflow flip-flop, the comparison flip-flops, the normal/control state flip-flop, the mode flip-flop, and the interrupt flip-flop.

PROCESSOR INTERRUPTS

Whenever the processor is operating in the non-zero base, any of the following conditions will generate a result descriptor and cause the interrupt branch to take place.

a. A memory parity error during a memory access by the processor.

b. Detection of a memory address error.

c. Execution time of an instruction exceeds a preset adjustable limit.

d. Attempt to execute an invalid instruction such as:

1) Non-assigned Op Codes.

2) Non-present options.

3) Invalid halts.

4) Invalid communicate address (non-decimal digits).

5) Invalid communicate address (first digit at NNNN must be 1111).

6) Privileged instruction.

An interrupt generated by the real time clock sets the interrupt flip-flop.

The processor result descriptor contains the information necessary to define the type of interrupt that occurred. This enables the interrupt handling routine of the software to take the necessary steps for the specific interrupt. If conditions a, b, c, or d1, d2, d3 above occur when operating in zero base, the processor clock is turned off and processing stops. Conditions d4 and d5 cause interrupt branching and do not set the interrupt flip-flop. Condition d6 is valid. An additional interrupt that only occurs in zero base is the execution of an invalid input/output operation. This interrupt and the clock interrupt generate a result descriptor and set the interrupt flip-flop. Automatic branching does not occur while operating in the control state.

INSTRUCTION FORMAT

The two instruction formats used by B 2500 and B 3500 Processors are format A, which is variable in length from one to four syllables, or format B, which is a fixed length of eight digits. Most instructions consist of one to four syllables, depending on the particular instruction. An instruction syllable consists of six digits. The syllable instruction format is shown in figure 1-2.

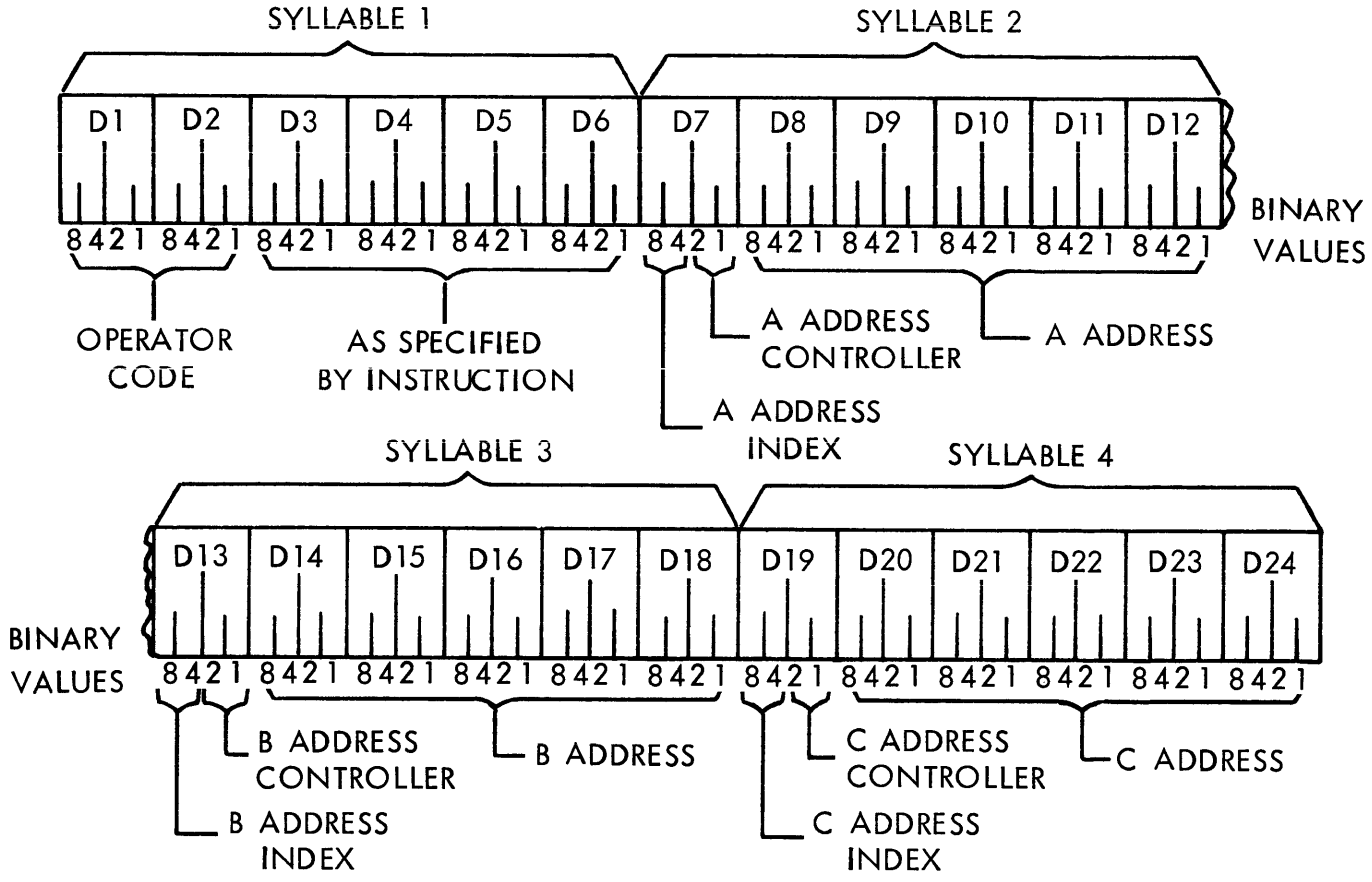

Figure 1-2. Syllable Instruction Format

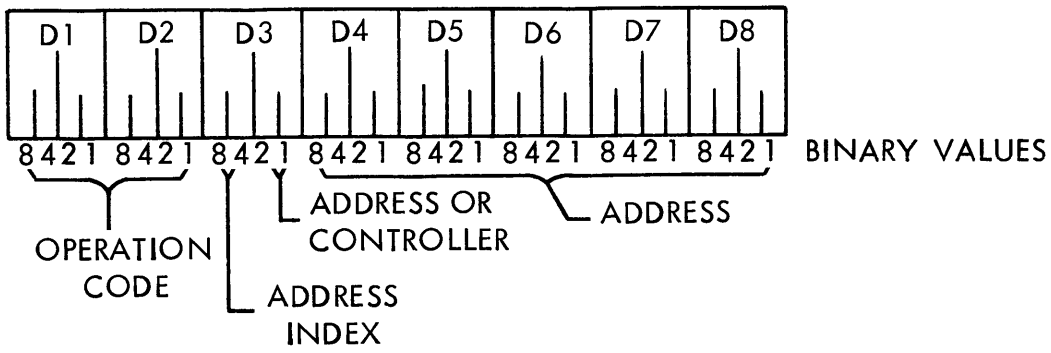

Figure 1-3. Eight-Digit Instruction Format

The first syllable of every instruction contains the operation code in digits D1 and D2. Digit positions D3 through D6 have various functions as specified by each instruction. Generally, D3 and D4 specify the length of the A field, whereas D5 and D6 specify the length of the B field. Several instructions consist of a single syllable. In multiple syllable instructions, the second, third, and fourth syllables are the A field, B field, and C field addresses, respectively. The addresses always address the most significant digit of the field. Digits D7, D13, and D19 specify various control functions with respect to the A, B, and C field addresses, respectively. The two address-index bits determine which index register, if specified, to use in generating the absolute address. The two address-controller bits specify whether signed or unsigned 4-bit or 8-bit formatted information is in the data field. The address controller bits may also specify indirect addressing. Digits D3 and D4 of the first syllable can specify that the second syllable (D7 through D12) is a literal value and not an address. The format of the literal is given in digits D3 and D4.

The 8-digit format is used only when an operation code and address are necessary, such as in a Branch instruction. The 8-digit instruction format is shown in figure 1-3.

READ-ONLY MEMORY

The read-only memory of the processor is a resistive type of storage. It contains a set of microprograms that controls most of the actions taken by the processor. The microprograms are initiated by the operation codes of program instructions after they are fetched from memory. The microprograms utilize the addresses stored in address memory during the execution of the instruction. During the fetch cycle of an instruction, the absolute addresses are assembled and stored in address memory. The use of read-only memory and address memory reduces the number of "hard registers" within B 2500 and B 3500 Systems.

Input/Output System

The input/output system of the B 2500 or B 3500 consists of the input/output channels and the input/output or peripheral controls/exchanges. All of the input/output operations are initiated, but are not executed by the processor. The execution of any specified input/output operation is accomplished by an I/O control unit. The I/O operation may be executed simultaneously with a processor operation and other previously initiated I/O operations on other I/O channels. The type of input/output operation is determined by an I/O descriptor that is transferred to the input/output control by an initiate I/O operation of the processor. At the conclusion of an I/O operation, a result descriptor is generated and stored, and the interrupt flip-flop is set ON. The result descriptor will specify any exception that may have occurred during the execution of the input/output operation, as well as other pertinent information.

I/O DESCRIPTORS

The input/output descriptors consist of a variable number of 6-digit syllables. Most of the input/output descriptors contain one, two, or three syllables, depending on the specific I/O operation requirements. Disk file I/O descriptors contain four syllables. The format of the I/O descriptors is shown in figure 1-4.

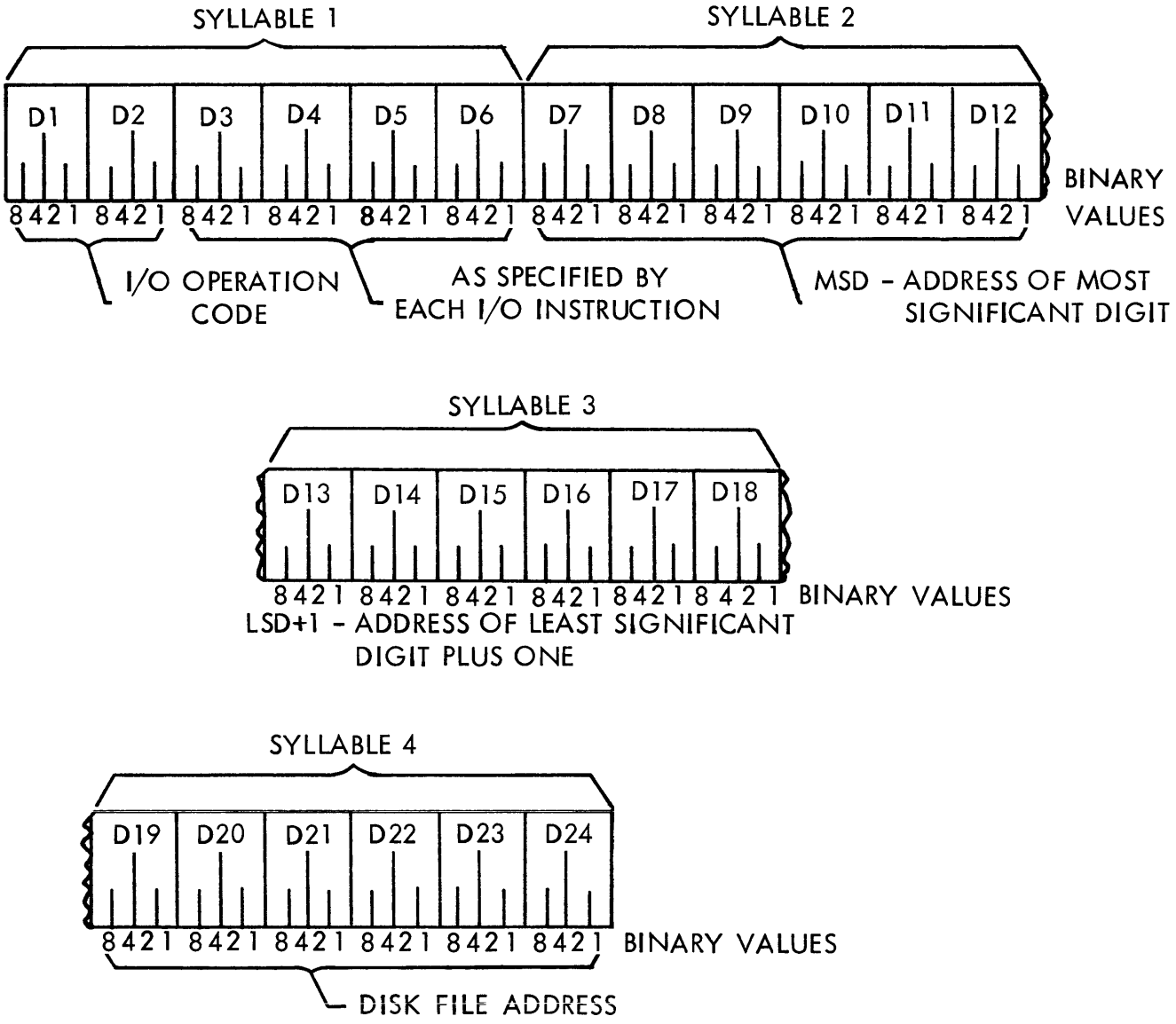

Figure 1-4. I/O Descriptor Syllable Format

Digits D1 and D2 always specify the type of I/O operation to be performed. Digits D3 through D6 specify which of the various options the specific I/O operation may incorporate. The second syllable will contain the address of the most significant digit of the input or output core memory buffer area. This is also called the beginning address and must be synchronized modulo-4 – it must begin at a word boundary. The third syllable contains the address of the least significant digit plus one. This address is called the ending address and is actually the address of the first digit in the field immediately following the input/output buffer area. Magnetic tape, disk file, sorter-reader, and lister descriptors require the ending address to be synchronized modulo-4. This address must be modulo-2 (even) for all other I/O descriptors.

Disk file descriptors require four syllables. The last syllable contains the disk file address. All beginning and ending addresses used in I/O descriptors are always absolute 6-digit addresses. Any I/O operation that attempts to access memory beyond the ending address will inhibit a memory transfer. Each type of I/O operation will generate a result descriptor. The result descriptor contains information pertinent to the type of I/O operation, indicating normal or non-normal execution.

RESULT DESCRIPTORS

The I/O result descriptor is generated by the I/O control at the completion of each I/O operation. It is stored in a fixed location of reserved memory that is dependent on the I/O channel that is being used (refer to table 2-1). The format of the result descriptor is shown in table 1-5, where bit 1 is the most significant bit of the 16-bit descriptor.

Table 1-5
Result Descriptor Format

Bit	Function
1	This bit is ON when an I/O complete has occurred on the I/O channel for the reserved result descriptor.
2	This bit is ON when an exception condition occurred during the I/O operation.
3 thru 16	These bits indicate specific exception conditions for the I/O controls.

The privileged instruction, Scan Result Descriptor, is used by the Operating System to test for a result descriptor with bit 1 ON, indicating an I/O complete has taken place on the specific channel. In addition, a test is made of the status of bit 2 to determine if an exception condition occurred on the initiated I/O operation. The specific exception conditions are detailed in section 6 under each type of I/O control unit.

Console

The console is an integral part of the processor and consists of a display panel, a control panel, and a working surface at table or stand-up height.

The display panel contains two 6-digit display registers made up of NIXIE® tubes for displaying instructions, addresses, or information. The panel also contains back-lighted, fixed messages for the major logical units of the processor and I/O channel indicators.

The control panel consists of a 16-digit keyboard and various control switches for use by the systems operator. With the control panel the operator can:

a. Start, stop, or single-step a program.

b. Initiate a load operation.

c. Examine instructions, addresses, or data contained in core memory.

d. Enter instructions, addresses, or data into core memory, or alter information presently in core memory.

e. Activate the emergency power-off cycle.

LOAD

Two types of load operations are available to the operator: normal and universal.

The normal load is executed by pressing the CL (Clear) key and then the LD (Load) key on the control panel. This causes the processor to initiate a Read operation from a particular peripheral unit previously established. The input operation reads 100 bytes into a fixed area of memory, compresses the data by stripping off the zone digits, and then branches to the first instruction contained in the data.

The universal load feature allows the operator to enter the desired peripheral unit via the keyboard into absolute address zero. A Load instruction, entered through the keyboard and then executed, initiates the input operation on the unit entered by the operator. Once initiated, the load operation is the same as the normal load previously described.

Console Printer

For operation with the Master Control Program, a console printer (SPO) is required for communication between the system and the systems operator. The console printer peripheral control contains a single-character buffer since data transmission to and from the console printer is serial-by-bit, whereas it is serial-by-character to main memory.

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GENERAL SYSTEM LAYOUT

The general layout of B 3500 Systems is shown in figure 1-5. The number of I/O channels that can be accommodated is a function of the type(s) of central control(s) used on the system. The flow of information between the peripheral units and core memory is accomplished in such a manner that the processor is not directly involved. Central control handles the requests for memory accesses for all I/O control units. Simultaneous requests are handled on a priority basis. The processor and central control both use address memory to obtain the address of data fields within core memory.

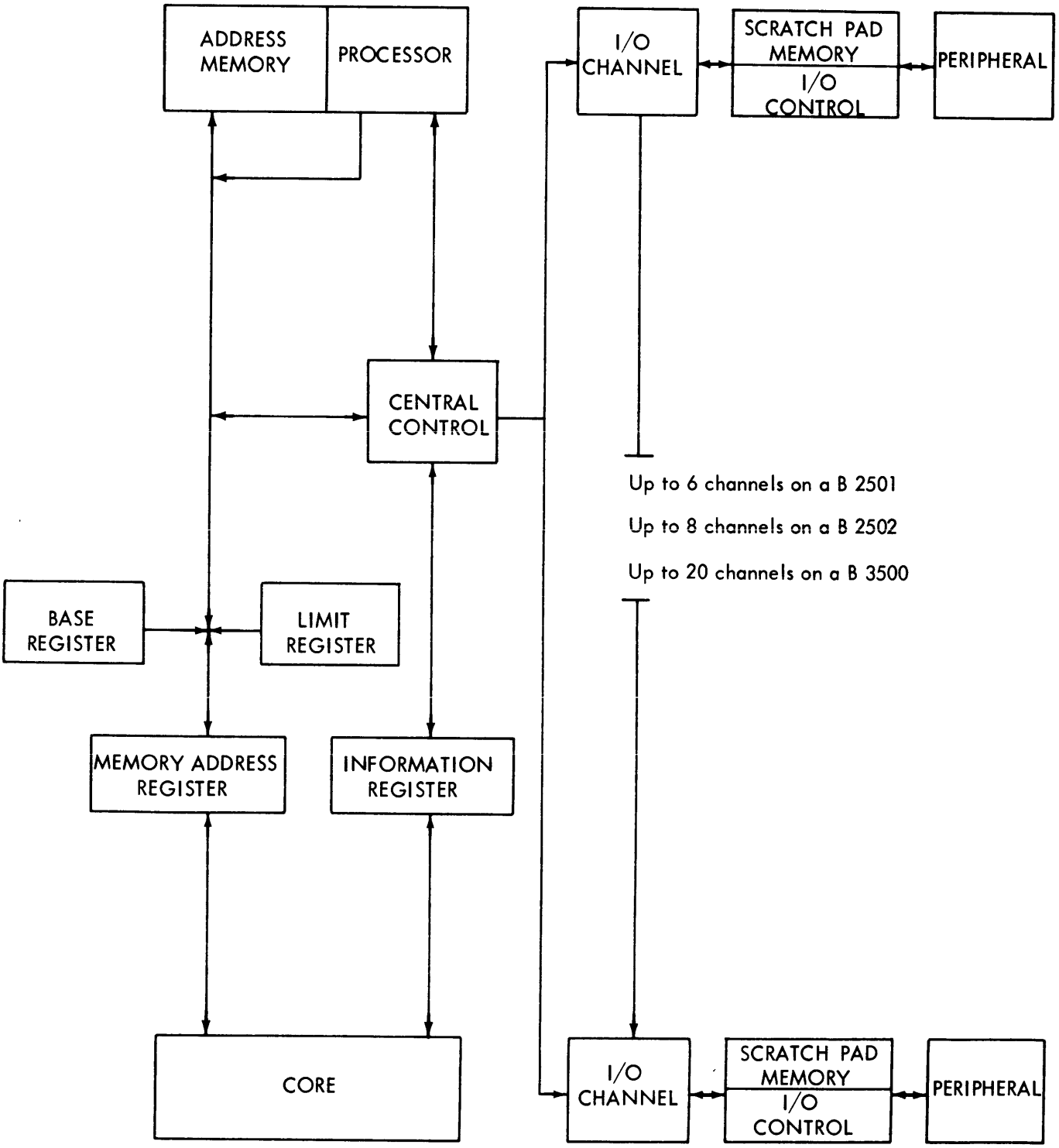

Figure 1-5. General System Layout for B 3500 Systems

GENERAL SYSTEM OPERATION

Central control functions as the interface between the I/O channel and the processor or memory during system operation. It determines the priority of memory accesses, should more than one channel need access, and translates data coming to the I/O channel from memory or from the channel to memory. It correlates various functions of the channels. The sequence of events is initiated by the processor when an I/O channel is needed.

When the program being performed has need of a peripheral unit, the processor executes the Initiate I/O instruction. This instruction reads the I/O descriptor from memory and sends the necessary information to the I/O channel through central control. This information contains the type of operation (Op Code) and variant information. The remaining portion of the I/O descriptor, beginning and ending addresses, is stored in address memory in the processor. The channel is selected by the channel designate level (CDL) from the processor. Once all the information is available, the I/O channel is released by the start channel buss (STCB) to operate independently. When the I/O channel has been released, it operates as another processor sharing memory with the processor or other channels. (See figure 1-6.)

If the operation being performed is with an input unit, the data are received by the I/O control and stored in a buffer within the I/O control. The channel then requests access to memory via central control. This request is processed by the priority logic which controls the request at the same time. Once access to memory has been granted, the information is transferred to memory. The information may or may not be translated, depending upon the I/O descriptor. This information is then written into memory at the location specified by the beginning and ending addresses in address memory. The type of operation determines which address is used. The address is then modified to point to the location when the next data will be written and returned to address memory. (See figure 1-7.)

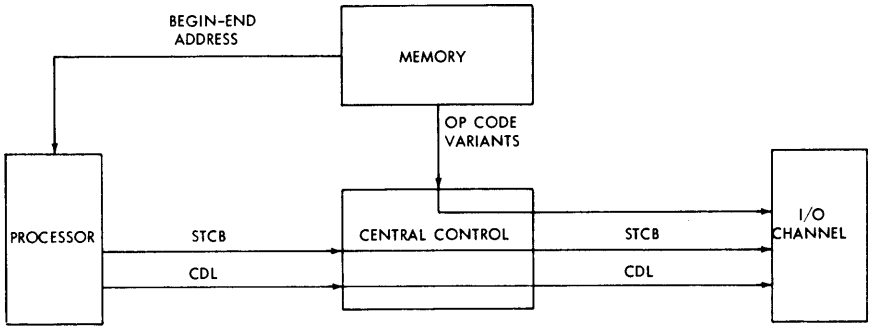

Figure 1-6. Initiate Information Flow

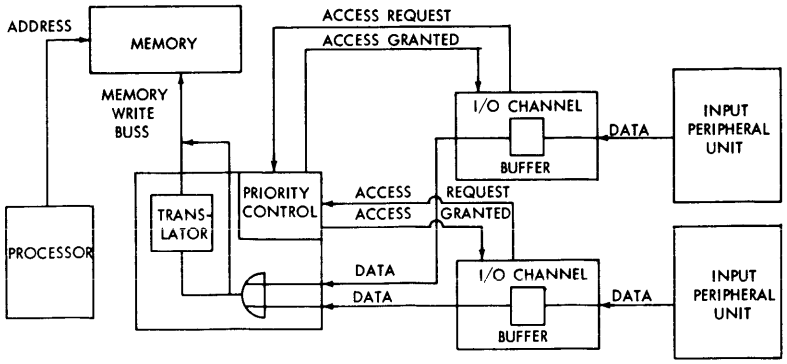

Figure 1-7. Input Media Data Flow

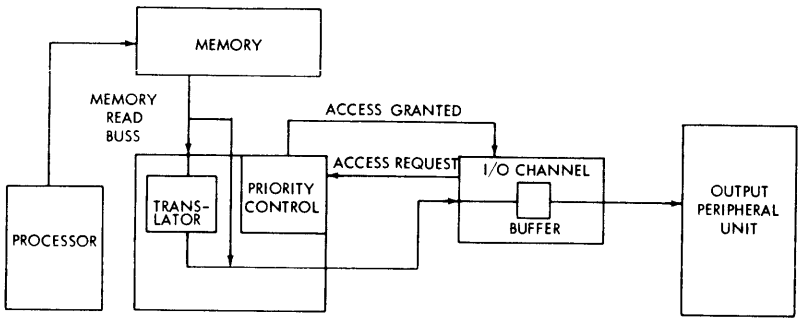

Figure 1-8. Output Media Data Flow

If an output operation is being performed, a similar sequence of events occurs, except data go from memory to the I/O channel. When the peripheral unit needs data, a memory access request is made to central control by the I/O channel. When priority is granted to the channel, the data are read from memory from the address specified by the beginning address in address memory. These data are transferred to the I/O buffer through, or bypassing, the translator, depending upon the I/O descriptor. From the buffer, data enter the peripheral unit. (See figure 1-8.)

SECTION 2
CORE MEMORY

GENERAL

This section describes the main memory of the B 2500/B 3500 Systems in detail. The physical arrangement of memory, memory addressing, reading into memory, reading from memory, the memory cycle and access time, and system operation using memory are discussed.

MAIN MEMORY

The main memory for the B 2500/B 3500 Systems is a coincident current core memory with a minimum cycle time of one microsecond, housed in a central control and memory base cabinet or in multiple Memory Base B cabinets. Figure 2-1 shows the Memory Base B cabinet or the central control and memory base cabinet. Both have the same physical appearance. Main memory can vary from 10,000 to a maximum of 500,000 8-bit characters (bytes) when used with Memory Base B cabinets and from 10,000 to a maximum of 60,000 when used in a central control and memory base cabinet.

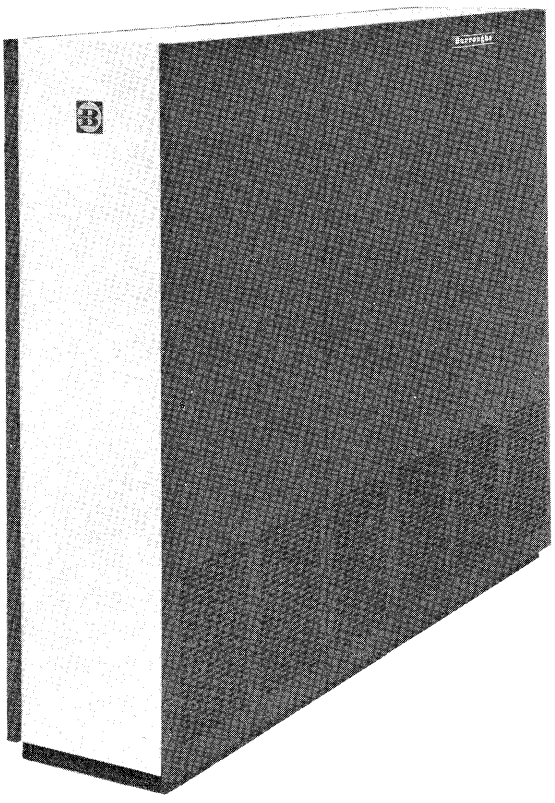

Figure 2-1. Memory Base B Cabinet or Central Control and Memory Base Cabinet

MEMORY BASE

A memory base is contained in the central control and memory base cabinet and in all Memory Base B cabinets. The memory base contains the memory information register (MIR), the memory address register (MAR), certain memory timing circuits, parity checking circuits, some address decoding, a memory information buss, and memory modules.

Memory Modules

Individual modules are available in 10,000, 20,000 and 30,000 byte sizes. Each module is essentially independent, containing all drivers, sense amplifiers, and core necessary for operation. Each core module is 17 planes deep and is addressable internally by word only. A word (two bytes) uses one bit from each plane, including parity. Externally any digit of any module is addressable. The three modules are described as follows:

a. Module A (10,000 bytes).

   1) Memory word size – 16 bits and 1 parity bit.

   2) Capacity.

      a) 5,000 16-bit words.

      b) 10,000 8-bit characters (bytes).

      c) 20,000 4-bit digits.

b. Module B (20,000 bytes).

   1) Memory word size – 16 bits and 1 parity bit.

   2) Capacity.

      a) 10,000 16-bit words.

      b) 20,000 8-bit characters (bytes).

      c) 40,000 4-bit digits.

c. Module C (30,000 bytes).

   1) Memory word size – 16 bits and 1 parity bit.

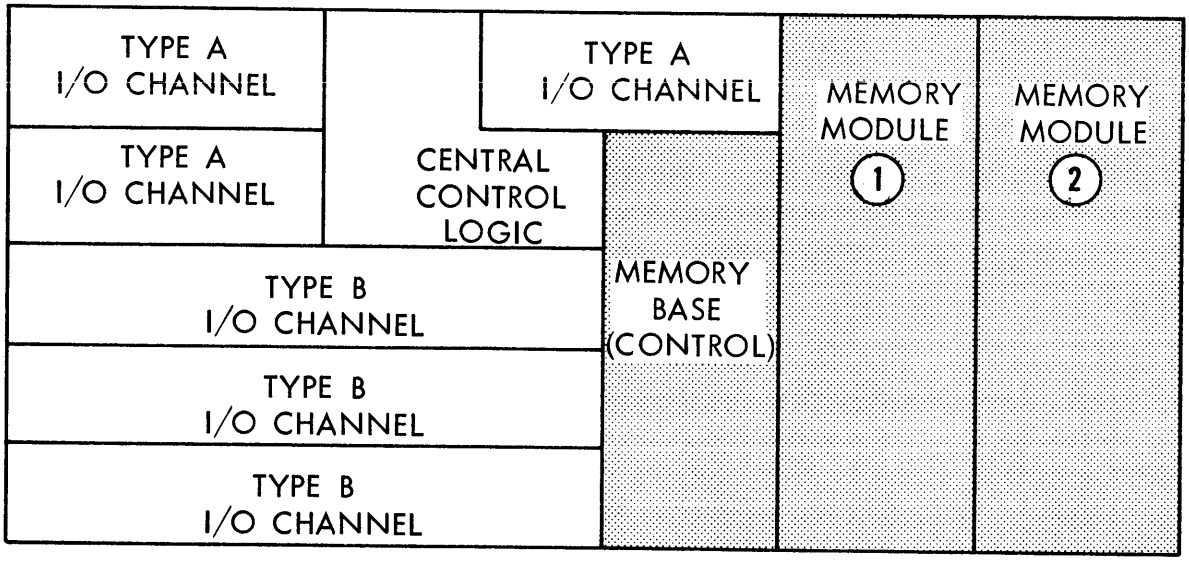

Figure 2-2. Memory Arrangement in Central Control and Memory Base Cabinet

2) Capacity.

a) 15,000 16-bit words.

b) 30,000 8-bit characters (bytes).

c) 60,000 4-bit digits.

Modularity

Either one central control and memory base cabinet or up to four Memory Base B cabinets may be used with a system. They cannot be intermixed.

Memory Base (2-Cabinet Configuration)

The B 2500 or the B 3500 System can be a two-cabinet system, consisting of a processor cabinet, and a central control and memory base cabinet. There are two locations in the central control and memory base cabinet for memory modules (see figure 2-2). Since the largest stack is 30,000 bytes (15,000 words), this limits the size of memory to 60,000 bytes.

If the number of modules in memory is increased beyond one, it is necessary that location 1 in figure 2-2 contain a 30,000-byte module. A second module must be placed in location 2. Since there are three different size modules, increasing the amount of core in location 1 will necessitate the removal of the smaller stack and the installation of the larger one. To increase memory from 10,000 to 20,000 bytes, the 10,000-byte module must be replaced by a 20,000-byte module, rather than adding another 10,000-byte module in location 2.

MEMORY MODULE CONFIGURATIONS

One or two core-memory modules may be accommodated by a central control and memory base cabinet in the following configuration only:

Digits of Memory	Bytes of Memory	Core Position 1	Core Position 2
20,000	10,000	A	
40,000	20,000	B	
60,000	30,000	C	
80,000	40,000	C	A
100,000	50,000	C	B
120,000	60,000	C	C

Memory Base B

Memory Base B is contained within its own memory cabinet (figure 2-1). There are a maximum of four Memory Base B cabinets for a system containing maximum memory. Each cabinet has room for five modules, providing a total of 150,000 bytes per cabinet, for a maximum memory of

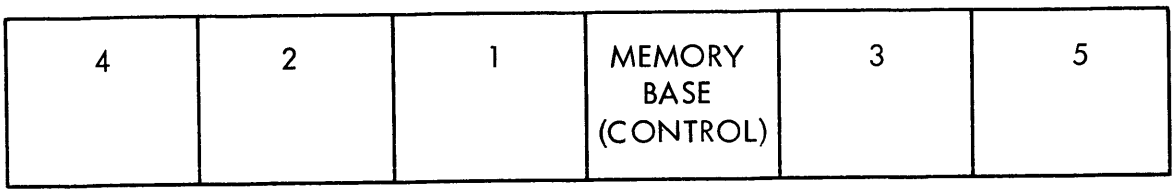

Figure 2-3. Memory Arrangement in Memory Base B Cabinet

500,000 bytes per system. The modules are placed into specific locations in the cabinet as the size of memory is increased (figure 2-3). Each consecutive location must contain 30,000 bytes before the next location is used.

Each of the first three installed Memory Base B cabinets must contain 300,000 digits of core memory before another Memory Base B cabinet is added. The fourth Memory Base B cabinet may contain up to two core-memory modules in the following configuration only:

Digits of Memory	Bytes of Memory	Core Position 1	Core Position 2
20,000	10,000	A	
40,000	20,000	B	
60,000	30,000	C	
80,000	40,000	C	A
100,000	50,000	C	B

MEMORY MODULE CONFIGURATIONS

Up to five core-memory modules may be accommodated by one Memory Base B cabinet in the following configurations only:

Digits of Memory	Bytes of Memory	Core Position 1 2 3 4 5
20,000	10,000	A
40,000	20,000	B
60,000	30,000	C
80,000	40,000	C A
100,000	50,000	C B
120,000	60,000	C C
140,000	70,000	C C A
160,000	80,000	C C B
180,000	90,000	C C C
200,000	100,000	C C C A
220,000	110,000	C C C B
240,000	120,000	C C C C
260,000	130,000	C C C C A
280,000	140,000	C C C C B
300,000	150,000	C C C C C

Core positions are numbered 4, 2, 1, 3, and 5 from left to right (looking at the pin side), with the memory control between positions 1 and 3.

RESERVED CORE MEMORY

A portion of the lower end of core memory is reserved for specific uses. These locations are used automatically by some of the processor instructions, the I/O control units, and the interrupt system. Table 2-1 lists the reserved locations and their specific purposes. Many of these locations are used constantly by the software system.

In addition to the reserved absolute addresses listed in table 2-1, each object program has base relative locations reserved for specific purposes. These base relative addresses which are reserved are shown in the B 2500 and B 3500 Assembler Reference Manual (1034949).

Table 2-1
System Reserved Memory Assignment

Absolute Address		Purpose	
Begin	End		
000000	000007	Load Usage	These may also be used for indirect field length storage.
08	15	Index Register 1	
16	23	Index Register 2	
24	31	Index Register 3	
32	39	Unassigned	

Table 2-1 (cont)
System Reserved Memory Assignment

Absolute Address		Purpose
Begin	End	
40	45	Enter-Exit Instruction Usage
46	47	Breakpoint Bit Pattern
48	53	Reserved
54	59	Pointer to MCP Variables
60		Trace Digit
61	63	Reserved
64	69	Interrupt and Reinstate Program Address Storage
70	72	Interrupt and Reinstate Base Register Storage
73	75	Interrupt and Reinstate Limit Register Storage
76		Interrupt and Reinstate E-A Mode, Overflow, Comparison Flip-Flops Storage
77		Breakpoint Execution Digit
78	79	Unassigned
80	87	Processor Result Descriptor and Link Area
88	93	Processor Usage
94	99	Interrupt Branch Address
100	107	Channel 00 Result Descriptor and Link Area
108	119	MCP Usage
120	127	Channel 01
128	139	MCP Usage
140	147	Channel 02 Result Descriptor and Link Area
148	159	MCP Usage
.	.	The format for channels 03
.	.	through 18 is the same as the
.	.	format for channel 02.
480	487	Channel 19 Result Descriptor and Link Area
488	499	MCP Usage
500	507	Multiline Adapter 01 Result Descriptor and Link Area
508	519	MCP Usage
.	.	The format for adapters 02
.	.	through 35 is the same as the
.	.	format for adapter 01.
1200	1207	Multiline Adapter 36 Result Descriptor and Link Area
1208	1219	MCP Usage

MEMORY CYCLE AND ACCESS TIME

The memory cycle time is one microsecond. Cycle time is defined as the time from the initiation of one memory operation to the initiation of the successive waiting memory operation on the memory system.

The read access time is less than 350 nanoseconds. Read access time is defined as the time from the initiation of the memory cycle to the time when data is stored in the memory information register. It does not include the time of transfer of an address from an external unit to memory, or transfer of the information from memory to an external unit.

MEMORY ADDRESSING

A memory cycle begins when either a processor or an I/O channel request is granted access to memory. This is determined by the priority control

logic in the processor as well as the central control section(s) of the I/O cabinet(s). When an access is granted, a memory cabinet is selected by decoding the most significant digit position of the address register (ADR). One of four possible memory start levels will be generated from this decoding to select one of four memory cabinets. If the address is less than 300,000, cabinet one is selected. If the address is between 300,000 and 600,000, cabinet two is selected, etc.

Once the cabinet has been selected, the remainder of the decoded address is gated to the selected cabinet's memory address register (MAR). MAR will express the address relative to the 000,000 position in that cabinet (see figure 2-4).

MEMORY READ/WRITE OPERATIONS

Once the memory cycle has been started, the type of operation in the processor (Read or Write) is determined by the memory control flip-flops (MCF). The outputs of the MCF's gate two self-latching circuits in memory control (MCL). These latches indicate the following:

a. MCL–0 (Read – word only).

b. MCL–1 (Write digit).

c. MCL–2 (Write Character).

d. MCL–3 (Write word).

MEMORY BASE SELECT

Address in ADR	Memory Start Level	Address Sent to MAR
000,000-299,999	1	000,000-299,999
300,000-599,999	2	000,000-299,999
600,000-899,999	3	000,000-299,999
900,000-999,999	4	000,000-099,999

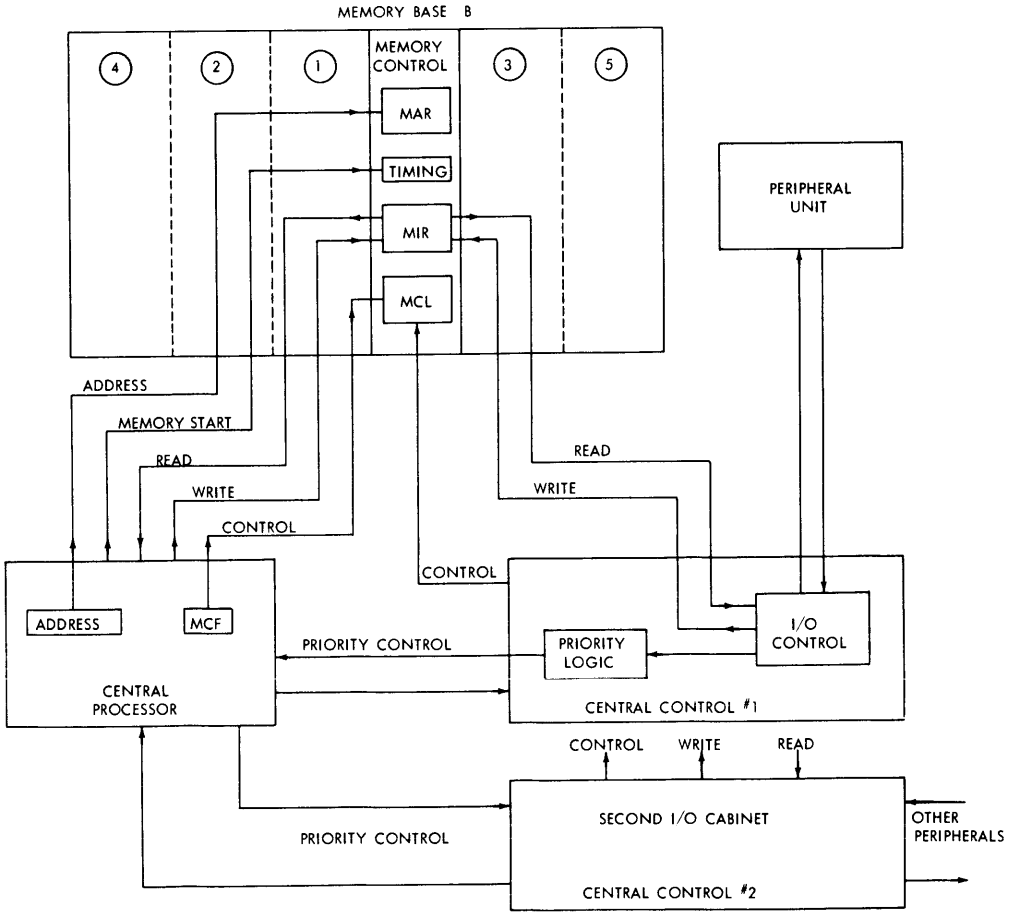

Figure 2-4. Memory Addressing

When a Read operation is requested, MCL is set to 0. The information is read from the location in core addressed by MAR and placed in the memory information register (MIR). From MIR, the information is sent to the processor or requesting unit via the memory read buss.

During a Write operation, the information is sent from the unit which has been granted access to the memory write buss. The amount of information (digit, byte, or word) is determined by the setting of MCL. This information is placed in MIR and written into a memory location specified by MAR.

SECTION 3
ADDRESS MEMORY

GENERAL

Address memory is a modular array of storage registers sharing a common memory address register and is located in the processor cabinet. It is addressed directly by the processor or central control for every memory request that is made by either unit.

MODULARITY

Included in all B 2500 and B 3500 Systems is a basic address memory that contains 24 words. Eight words are used by the processor and the remaining 16 words are available for use by I/O channels. Each I/O channel utilizes two consecutive words. Each word consists of six digits, large enough to contain any absolute address within core memory configurations. Address memory extensions can be added to this basic module, each extension containing an additional 12 words. A total of eight extensions can be added to the basic module, allowing address memory to contain a maximum of 120 words.

MEMORY ASSIGNMENT

The assignment of address memory is shown in figure 3-1. Each word in address memory consists of six 4-bit digits as shown by word 5 in figure 3-1. Digit D1 is the most significant digit of the word. The information contained in the first three word

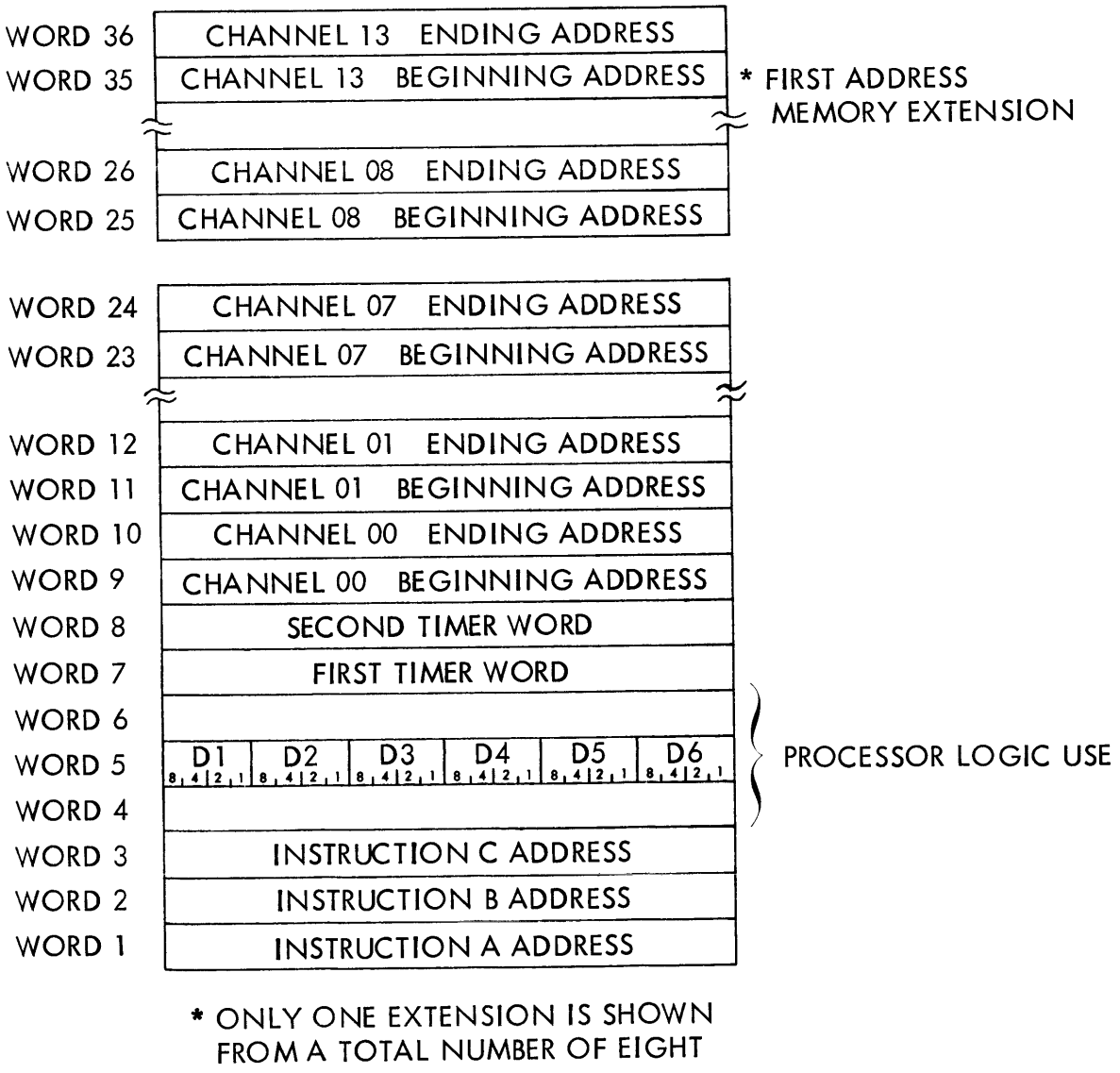

Figure 3-1. Address Memory Assignment

locations is reserved for the A, B, and C addresses of the processor instructions. These addresses are the absolute addresses that were generated during the fetch cycle of the instruction. The instruction determines whether there is a valid address in the three reserved locations. Words 4, 5, and 6 are used by the processor and do not necessarily contain an address. Word 7 is the first timer word which is counted up at a 1 KC rate; therefore, it is capable of containing a value of up to 999.999 seconds. This timer word can be read from address memory and may also be simultaneously cleared by a privileged instruction. The eighth word in address memory is the second timer word. This word is set by the Operating System and is constantly compared with the first word. When the two words become equal, a timer interrupt is generated. The timer will continue to count until reset by the Master Control Program. The remainder of address memory is reserved for input/output operations as pairs of words for each I/O channel. The two words will contain the beginning and ending addresses obtained from the I/O descriptor initiated on the specific I/O channel. Only one address memory extension is shown. Additional extensions in groups of twelve words build word locations up to word 120.

LIMITATIONS

Limitations on the assignment of groups of address memory words are as follows.

The system provides for a maximum of 120 positions of address memory. Of the standard 24 words provided in the processor, twelve of these words must be assigned to positions 1 through 12. The second twelve and all twelve-word extensions are assigned to other positions equal to 1 through 12, modulo 12 (i.e., positions 13-24, 25-36, 37-48, etc.).

When Central Control B cabinets are used, positions 9 through 12 are assigned to the lower two large controls in the first Central Control B cabinet, positions 13-24 are assigned to the upper three large controls and the lower three small controls in the first Central Control B cabinet, positions 25-36 are assigned to the upper two small controls in the first Central Control B cabinet and to the lower four large controls in the second Central Control B cabinet, and positions 36-48 are assigned to the upper large control and to the five small controls in the second Central Control B cabinet. Positions 49-120 are assigned to the multiline adapters.

When the central control and memory base cabinet is used, the initial 24 words must be assigned to positions 1-24. Positions 9 through 12 are assigned to the lower two large controls and positions 13-20 are assigned to the remaining large control and the three small controls.

SECTION 4
CENTRAL CONTROL

GENERAL

As stated previously, there are two types of central control units: Central Control A in the central control and memory base cabinet and Central Control B in the Central Control B cabinet. The central control and memory base cabinet and the Central Control B cabinet have the same appearance as the Memory Base B cabinet shown in figure 2-1. Central Control A can accommodate up to six I/O channels and Central Control B can accommodate up to ten I/O channels. Only one Central Control A may be used in a system and up to two Central Control B units may be used in a system. Central Control A and Central Control B may not be intermixed in a system.

There are two different physical sizes of I/O channels: type A and type B. The type A channel provides space for one row of 36 printed circuit card positions. The type B channel provides space for one row of 85 printed circuit cards.

In the central control and memory base cabinet there is one type A channel located to the right, and two located to the left of the central control logic (see figure 2-2). In the Central Control B cabinet, type A channels are located to the right, and type B channels are located to the left of the central control logic.

Any channel position located to the right of the central control logic requires a right-hand control; any position located to the left of the central control logic requires a left-hand control (refer to table 1-3).

All 1 x 85 controls (one row containing 85 card positions) are left-hand controls that require type B I/O channel positions. A 1 x 36 control may occupy either a type A or type B channel position and may, therefore, be either a left-hand or a right-hand control. A left-hand control is required in type B.

LOGIC FLOW

Figure 4-1 shows the logic which connects the I/O channels with the processor and memory through central control. Logic levels are generated in each I/O channel and combined by central control before being sent to the processor and memory. Other logic levels are generated with processor memory and distributed by central control to each I/O channel. There are also logic levels which pass through central control, with central control performing as the connecting block between the processor and the I/O channels. Priority logic determines which of the I/O channels will be allowed access to memory, should more than one channel need access at the same time. Translator logic is described in the following paragraph.

TRANSLATOR

Included as an optional part of central control is a plug-in translator. This translator is modular and is capable of translating BCL data to/from EBCDIC to/from core memory.

The I/O control unit requests central control to use the translator or to bypass it. The translation takes place as data is transferred between the I/O control unit and main memory. Additional time is not required for an input/output operation when translation is necessary.

The translator logic translates incoming BCL data to EBCDIC data, or outgoing EBCDIC data to BCL. EBCDIC codes not assigned a BCL code will generate the code for a BCL question mark.

NOTE

All graphics are assigned to a BCL code.

MEMORY REQUEST CONTROL

Central control provides interface from the I/O channels, the processor, and core memory. Control information from the processor is sent to central control where it is distributed to each I/O channel. Central control handles all of the core memory requests made by the I/O control units. Data from each I/O channel which are to be written into core memory are placed on the memory write buss by central control, and data which are to be read from core memory are placed on the core memory read buss and distributed to each I/O channel.

When a request is made by an I/O control, central control will obtain the core memory address from the address memory location reserved for the specific I/O channel. The address is used to access main memory and the memory cycle is initiated. The memory cycle could be either a read or write, depending on the specific input/output operation. When the processor requests a memory access, the

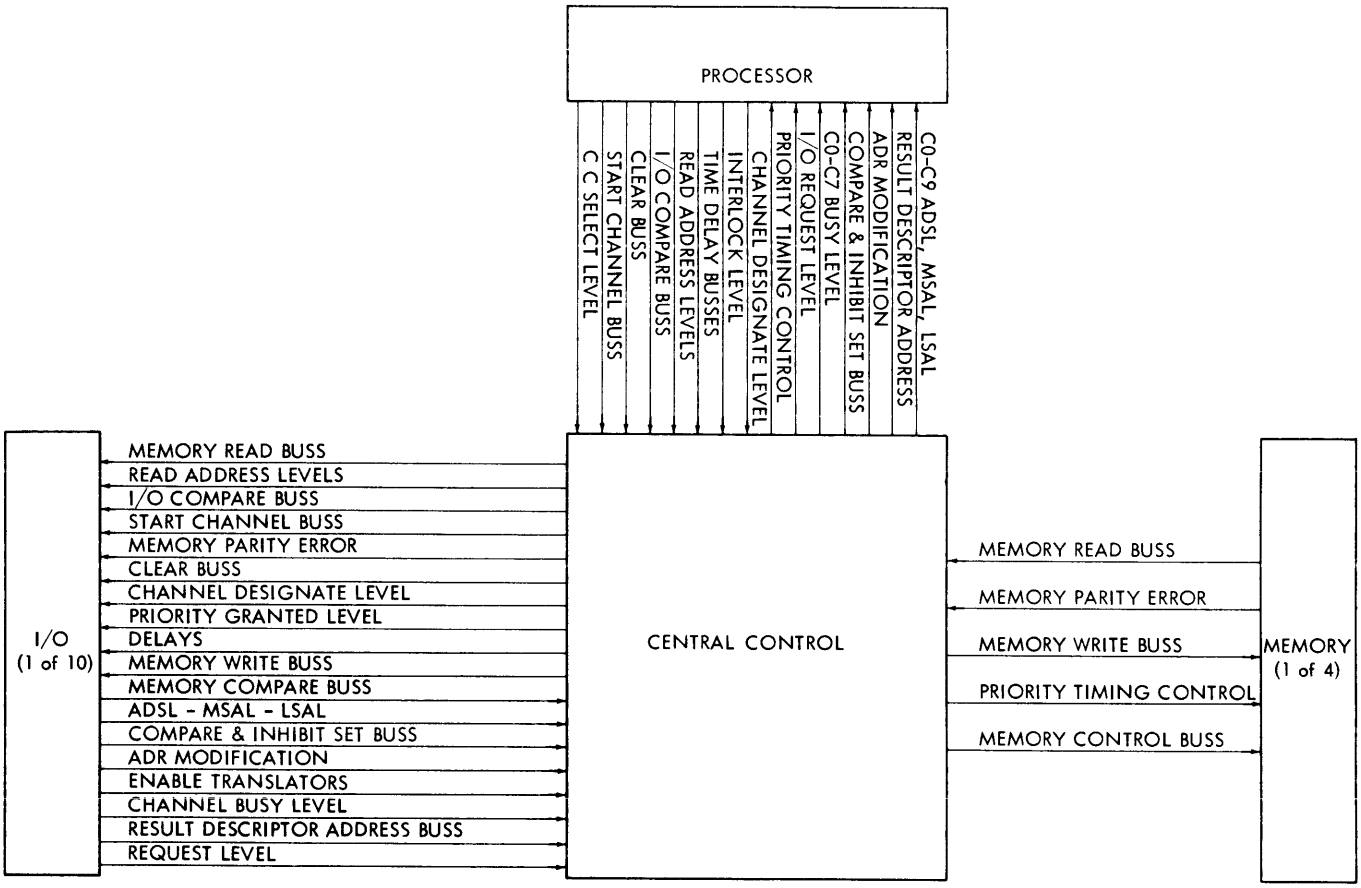

Figure 4-1. Logic Flow through Central Control

address is also obtained from an address memory location reserved for the processor. This address is used to access main memory and the memory cycle, either a read or write, is initiated.

Since only a single memory access can be made, multiple memory requests must be handled individually. This handling is accomplished automatically by central control. As previously mentioned, each central control contains priority logic which is established or changed by a field engineering adjustment. As I/O channels are added to a central control, they are added to the priority network. The processor has lower priority than a central control. The highest priority request is granted first and, as soon as it is completed, the next highest request is automatically granted. This process is repeated until all of the multiple requests are handled. Requests are alternately granted to each central control, depending on which control was last granted a request. If a central control does not want the access, then it is granted to the processor.

SECTION 5
CENTRAL PROCESSOR

GENERAL

This section describes the B 2501, B 2502 and B 3501 Central Processors used with the B 2500/B 3500 Systems (see figure 5-1). The instruction format, interrupts, descriptors, logical units, stack, adder, and read-only memory are discussed.

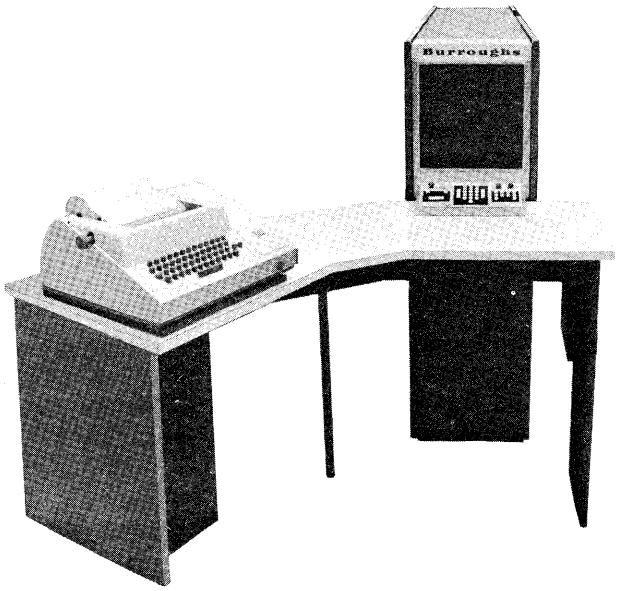

Figure 5-1. B 2500/B 3500 Central Processor

The processor contains the circuitry and logic to perform the instruction set of the B 2500 and B 3500 Systems. The B 3501 Processor operates with a cycle time of one microsecond and the B 2501 and B 2502 operate with a cycle time of two microseconds. The instructions are capable of performing operations on digit-, byte-, or word-formatted data fields. The internal 8-bit code may be either EBCDIC or USASCII code and is programmatically selectable. In addition to executing the instruction set, the processor has an automatic interrupt system.

NOTE

The only difference between the B 2501 and B 2502 is that the B 2502 may optionally have two more Type B channels for a total number of eight channels maximum, whereas the B 2501 has a maximum of six channels.

DATA MODES

Two modes are used in the B 2500 and B 3500 Systems to represent internal data. They are:

a. 4-bit mode.

b. 8-bit mode.

4-Bit Mode

In a 4-bit mode, data are interpreted in units of four bits. Where a sign is expected, it is interpreted as a separate and leading 4-bit unit. The internal code in 4-bit mode is interpreted by the arithmetic unit in the processor as follows:

Binary Code	Sign Code	Decimal Equivalent		
0000	+	0		
0001	+	1		
0010	+	2		
0011	+	3		
0100	+	4		
0101	+	5		
0110	+	6		
0111	+	7		
1000	+	8		
1001	+	9		
1010	+	Ø	(undigit 0)	Accepted by the arithmetic unit, but will give unspecified results.
1011	+	1	(undigit 1)	
1100	+	2	(undigit 2)	
1101	-	3	(undigit 3)	
1110	+	4	(undigit 4)	
1111	+	5	(undigit 5)	

When a signed 4-bit format is specified in the receiving field for any operation, the sign digit is set as follows:

USASCII Code	EBCDIC Code
+ = 1011	+ = 1100
- = 1101	- = 1101

A plus sign compares higher than a minus sign in the system's collating sequence for signed fields.

8-Bit Mode

In an 8-bit mode, data are interpreted in units of eight bits (byte) unless otherwise specified. Conversion between 4-bit mode and 8-bit mode is accomplished automatically during the execution of instructions with no timing costs to the program being operated.

For code sensitive instructions involving the manipulation of 4-bit numeric data, the most significant four bits of a 2-byte defined receiving

field are automatically set to the code indicating the numeric subset of the selected 8-bit code. Those four bits are 1111 (undigit 5) in EBCDIC code and 0101 (binary 5) in USASCII code.

8-bit data are considered unsigned except in the cases of the Move Alphanumeric, Move Numeric, and Edit instructions. Additional details are given in the B 2500 and B 3500 Assembler Reference Manual (1034949).

Alphanumeric comparisons are performed in binary. The collating sequence for EBCDIC code is special characters, alphabetical characters, and digits; the collating sequence for USASCII code is special characters, digits, and alphabetic characters.

PROCESSOR OPERATING MODES

The central processors of the B 2500 and B 3500 Systems operate in one of four states. They are:

a. Control state, zero base – the interrupt flip-flop can be set, but the interrupt branch is not executed until the return to normal state. Privileged instructions are allowed.

b. Control state, non-zero base – the interrupt flip-flop can be set, but the interrupt branch is not executed until the return to normal state. Privileged instructions are disallowed.

c. Normal state, zero base – the interrupt branch is allowed to be executed, and privileged instructions are allowed.

d. Normal state, non-zero base – the interrupt branch is allowed to be executed, and privileged instructions are disallowed.

NOTE

Some error conditions which result in a processor result descriptor being stored will not set the interrupt flip-flop, but the interrupt branch is executed directly.

INSTRUCTION FORMAT

The basic format of the instruction set is discussed in section 1. An instruction may consist of from one to four 6-digit syllables, or a single 8-digit syllable.

Operator Code

The first two digits of the first syllable represent the operator code. This operator code is a decimal value ranging from 00 through 99, but all values are not used. All unassigned codes are reserved for expansion. If the processor receives any operator code that has not been assigned, an invalid instruction interrupt is generated. The operator code itself determines the number of syllables that must be fetched. Appendix A lists the instruction set of the B 2500 and B 3500 Systems. For detailed information on a particular instruction which is not covered in this manual, refer to the B 2500 and B 3500 Assembler Reference Manual (1034949).

Field Length

For a majority of the instructions, the third, fourth, fifth, and sixth digits (D3 through D6) of the first syllable control the field lengths of the data fields (see figure 5-2). Digits D3 and D4 determine the A field length (AF), whereas digits D5 and D6 determine the B field length (BF).

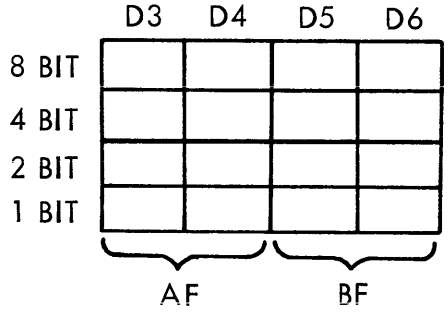

Figure 5-2. Field Length Digits

The field length values can range between 00 and 99, inclusively. If a field length of 00 is specified, the field length is 100. The digits D3 and D5 may also specify an indirect field length. This is accomplished by making the D3/D5 8-bit and 4-bit (figure 5-2) both equal to a 1. The base relative indirect address of the field length is obtained from the two low-order bits of D3/D5 and the even values of the D4/D6 digit. Thus, the indirect field-length base relative address can be any even value from 00 through 38 – a total of 20 base relative addresses. The reserved memory format shown in table 2-1 shows the reserved core memory locations that correspond to the indirect field-length addresses.

Address Index

The two most significant bits (8 and 4) of the first digit in the address field is the address index control (see figures 1-2 and 1-3). The bit configuration of the address index signifies which of three index registers is to be used while generating an absolute address. The 8-bit, 4-bit configuration is as follows:

a. 00 – no indexing.

b. 01 – index register 1 (IX1).

c. 10 – index register 2 (IX2).

d. 11 – index register 3 (IX3).

There is an address index controller for the A, B, and C address fields, and also for the address field of the 8-digit instruction. If indexing is specified, the designated index register value contained in reserved locations within an object program is added algebraically to the address field and base register during the fetch cycle, prior to storage in its reserved address memory location.

Address Controller

The two low-order bits (2 and 1) of the first digit in the address field specify the data field format (see figures 1-2 and 1-3). The address controller bits and address index bits comprise the entire first-digit position of the address field. Four different 2-bit and 1-bit combinations can be specified by the two address controller bits as follows:

a. 00 – unsigned 4-bit format.
b. 01 – signed 4-bit format.
c. 10 – unsigned 8-bit format.

(Most significant address digit for the branch instructions)

d. 11 – indirect address.

Any combination may be used except where prohibited by a specific instruction. The unsigned 4-bit format means that the data field consists of digits of information without a sign digit. The signed 4-bit format specifies a digit data field with a sign digit preceding the most significant digit of the field. The field length does not include the sign digit position when a signed data field is specified. A bit configuration of 1101 is always treated as a minus sign (-), whereas any other bit configuration is considered as a plus sign (+). The unsigned 8-bit (character/byte) format specifies that the data field is in an internal 8-bit alphanumeric code. The indirect address bit configuration specifies that the data field address is located at the specified base relative location. During the fetch cycle, another access must be made to obtain the specified field address.

An indirect address must be even and is checked after indexing, if any. An odd indirect address is considered to be a non-synchronized address contained in an instruction and causes a processor interrupt.

Address Digits

Since the first digit of the address field comprises the address index and controller bits, five digits remain for use as the data field address; however, addresses may generate beyond this seemingly maximum address of 99,999 by utilizing the address controller bits at binary values up to a 2, thus creating an actual maximum address range per program of 000000 to 299,999. Programs exceeding the address of 99,999 cannot contain referenced data areas in excess of the 99,999 address. This address is always base relative and is added to the base register value during the fetch cycle. The absolute address stored in address memory is comprised of the value in the address field added to the base register. It can also be indexed by an index register when specified. The address digits are limited to the decimal digits zero through nine, thus creating a completely decimal addressing scheme for a beneficial system/programmer/operator interface.

LITERAL SPECIFICATION

Some of the instructions allow the A field length digits to specify that the A address syllable contains a literal value and not the address of a data field. Figure 5-3 shows the bit configuration for the various literals that the A address syllable can contain.

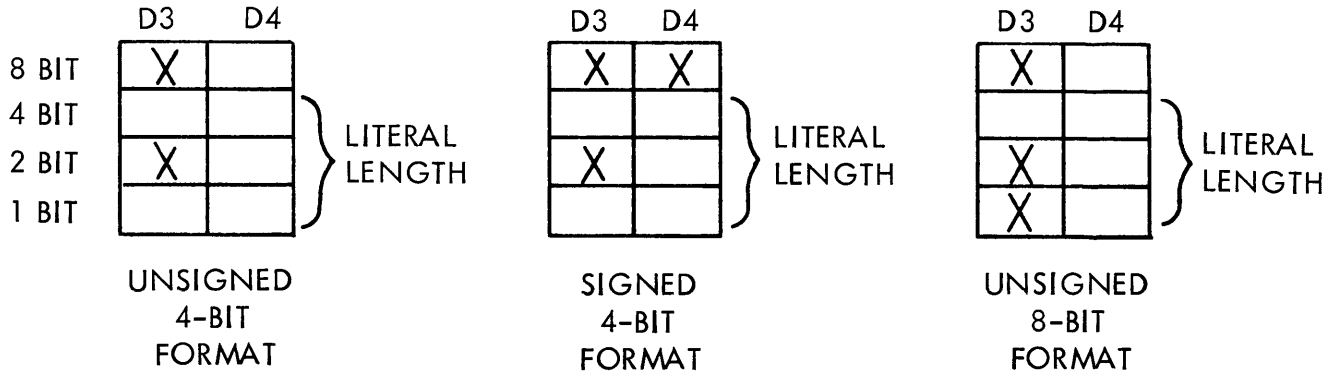

Figure 5-3. Literal Specification Control

When D3 has the 8-bit and 2-bit ON with the 4-bit OFF, the A address is a literal. The D3 1-bit and D4 8-bit specify the format of the literal as shown in figure 5-3. When the literal specification is an unsigned 4-bit format, the literal length can be one through six – the total number of digits in the address field. When the signed 4-bit format is specified, the literal length can be one through five since the most significant digit is the sign digit.

When the 8-bit format is specified, the literal length can have a value of one through three. If the literal length is less than the maximum length for the specified format, the literal is always assumed to be left-justified.

NORMAL STATE INTERRUPTS

When certain operational conditions occur within the processor while executing instructions in the normal state, the following logic occurs:

a. If either an operator interrupt, a timer interrupt, or an I/O interrupt occurs, the interrupt will generate a result descriptor and store the descriptor in the reserved memory location specified in table 2-1.

b. The interrupt will turn the interrupt ON (set) and store the program return point and logical register settings.

c. An automatic branch is taken to the address specified by the contents or reserved memory location 000094 (refer to table 2-1). The processor operational mode is changed from normal state to control state, zero base.

The branch to the control state is a branch to the Operating System – the Master Control Program. It is the function of the Operating System to determine the type of interrupt and the course of action that is to be followed. The interrupt system, as explained, is automatic and is an integral part of the processor hardware system.

Memory Parity

When a memory parity error is sensed during a processor access from main memory, an interrupt occurs. (The instruction is continued until completion if the error did not occur during fetch.) The instruction being executed is completed before allowing the automatic interrupt system to become operative.

Address Error

A memory address error can occur under any of the following conditions:

a. Base or limit address error.

b. Non-synchronized addresses of instructions.

c. Non-synchronized addresses contained in instructions.

d. Non-decimal digits contained in addresses.

Detection of address errors is made on those addresses developed after the addition of the base and index register, if applicable, and on all developed addresses which are advanced during the execution of the instruction. Note that when the base or index register is added to an address con-

taining a non-decimal digit, the resultant address may be changed to an undefined address which no longer contains a non-decimal digit and, therefore, will not be detected. Detection of non-synchronized addresses contained in instructions is limited only to addresses which are used to write into memory.

If any of the above four error conditions occurs, the instruction is completed, but all memory write cycles are inhibited. A memory read cycle is inhibited only when an address contains a non-decimal digit. However, when addresses are advanced during the execution of an instruction, non-decimal digits may be changed to decimal digits, allowing a memory read or write cycle to be performed.

When one of the above error conditions occurs and an instruction is completed, an interrupt is generated and the automatic interrupt system takes over control. A base or limit address error occurs whenever a memory address is out of bounds of the base and limit register settings. This feature provides for memory protection when operating in a multiprograming mode.

Non-synchronized addresses of instructions is an error when a branch occurs to an address that is not an even value (Mod 2). An error that results from non-synchronized addresses contained in an instruction is caused when an address is not Mod 2 or Mod 4 when required by the format control bits or the instruction code. A non-decimal digit in an address is a digit that has a binary value of 10 through 15 and is referred to as an undigit.

Instruction Time Out

When an instruction is fetched, an adjustable timer of approximately 250 milliseconds is triggered. If execution of the instruction is not completed during the preset time, an interrupt is generated immediately. This does not include actual I/O operations since the processor only initiates them, whereas the I/O control unit executes them.

NOTE

The contents of the reserved location for the next instruction address may or may not have meaning.

Invalid Instructions

An invalid instruction is defined as follows:

a. All non-assigned operator codes.

b. Operator codes requiring options which are not present.

c. Invalid Branch Communicate instruction.

d. Invalid halts.

e. Privileged instructions during non-zero base state operation.

If any of these conditions occur, the absolute address of the invalid instruction is stored in the memory location reserved for the program address. Execution of the instruction and all memory write cycles are inhibited.

Privileged Instructions

There is a set of instructions that can only be executed in zero-base state. If one of these privileged instruction codes is detected while operating in non-zero-base state, an interrupt is generated. Memory write cycles are inhibited, no instruction is executed, and the memory location reserved for the program address contains the absolute address of the privileged instruction.

Clock Interrupt

Two words that comprise the timer and its control value are contained within address memory. The first timer word is counted at a one millisecond rate. The second timer word can contain any six-decimal digit value. When the real timer word is counted to the value of the control, the clock interrupt is generated. The real timer value will continue to count and requires the MCP to read and clear this value from the address memory location. The maximum value that the real timer word can achieve is 999,999 milliseconds. In any event, the current instruction is completed before automatic interrupt handling takes place.

CONTROL STATE INTERRUPTS

When the processor is operating in control state, there are interrupt conditions generated, but no automatic interrupt handling takes place at the

completion of an instruction. Rather, at the time that the MCP attempts to return to normal state, automatic branching to control location 000094 will occur so that these interrupts will be handled by the MCP.

If the processor is operating in the zero-base state, the following processor conditions will cause the processor clock to be turned off, leaving all conditions static:

a. Memory parity error interrupt.

b. Address error interrupt.

c. Instruction time out interrupt.

d. All non-assigned operator codes.

e. Operator codes requiring options which are not present.

f. Invalid halts.

Since the processor is in the zero-base state, any of the above interrupts indicates that a hardware or an Operating System error exists. A privileged instruction interrupt cannot occur because all of the instructions are executable in the zero-base state. The clock interrupt condition occurs in the same manner as in normal state, but no automatic branching occurs in control state.

Invalid I/O Operation

Since the zero-base state must be entered to execute an initiate I/O operation, it is possible to have an invalid I/O descriptor which will set the interrupt flip-flop ON and store a result descriptor. Automatic interrupt branching occurs in normal state, but not in control state. An invalid I/O operation interrupt can occur under any of the following conditions:

a. The specified I/O channel is not attached to the system.

b. The I/O descriptor for the specified channel is an invalid operation.

c. An attempt is made to initiate an I/O operation on a channel that is busy with a previously initiated operation.

d. The addresses within the I/O descriptor are not valid (not synchronized, non-decimal digits, or the ending address is not greater than the beginning address).

PROCESSOR RESULT DESCRIPTOR

All processor interrupts that do not turn off the processor clock generate a result descriptor. The interrupt flip-flop is not necessarily turned ON. The format of the result descriptor is shown in figure 5-4.

The result descriptor is a complete memory word of 16 bits, with bit 1 being the most significant. The function of each bit is shown in table 5-1.

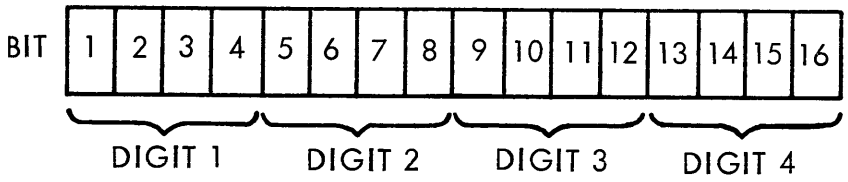

Figure 5-4. Processor Result Descriptor

Table 5-1
Bit Functions of Processor Result Descriptor

Bit	Function
1	This bit is ON whenever a result descriptor is stored.
2	This bit is ON whenever an exceptional condition occurs (always ON whenever a result descriptor is stored).

Table 5-1 (cont)
Bit Functions of Processor Result Descriptor

Bit	Function
3	This bit is reserved.
4	This bit is ON if the interrupt was generated by the execution of an invalid I/O operation.
5	This bit is ON if the interrupt was generated by the execution of an invalid instruction.
6	This bit is ON if the interrupt was caused by a memory parity error.
7	This bit is ON if the interrupt was caused by a memory address error.
8	This bit is ON if the interrupt was caused by an instruction time out.
9	This bit is ON if the interrupt was caused by the clock interrupt.
10	This bit is ON if the interrupt was caused by an operator.
11-16	These bits are reserved.

If a processor interrupt is generated, reserved memory will contain a word with bit 1, bit 2, and one or more of the other specified bits ON. When the result descriptor is handled, the first two bits must be turned OFF by the Operating System. The privileged instruction (Scan Result Descriptor) is used by the Operating System to sense the presence of a result descriptor in reserved memory.

LOGICAL UNITS

There are a number of logical units within the processor which affect its operation. These logical units are set or changed by instructions, or control the execution of specific instructions.

Overflow Flip-Flops

The overflow flip-flop is a hardware logical unit that indicates the data field of a move or arithmetic instruction is exceeded. If an overflow condition is detected, the command is executed but the data is not affected. The overflow flip-flop is not cleared at the beginning of an arithmetic operation but is preserved; therefore, it indicates overflow that has occurred any time before or during a series of arithmetic operations or other interjected non-arithmetic operations. Instructions that can create an overflow condition are:

a. Arithmetic instructions except Multiply.

b. Floating point arithmetic instructions.

c. Move Numeric.

d. Move Alphanumeric.

Overflow cannot occur during a Multiply instruction since the receiving field is always large enough to contain the product. In all cases except the floating point instructions, overflow results when the receiving field cannot contain the sending field. With floating point instructions, the overflow can also be caused by an out-of-range exponent. For specific information on the instructions, refer to the B 2500 and B 3500 Assembler Reference Manual (1034949). The overflow flip-flop is turned OFF by the Branch On Overflow instruction. Once cleared, it can be turned ON if the conditions arise while executing those instructions that may turn it ON. There are two ways by which the present setting of the overflow flip-flop may be stored in the 4-bit of reserved location 000076 (see table 2-1), and then clearing the flip-flop. These are:

a. Branch Communicate.

b. Automatic interrupt feature.

The overflow flip-flop is restored from the reserved memory location by the Branch Reinstate instruction. In addition, the object program may branch to some subroutine and the overflow flip-flop set-

ting must be retained and restored at the conclusion of the subroutine execution, prior to continuing in the object program. The Enter instruction will store the flip-flop setting into the four bits of the reserved character location in the memory stack, and then clear the overflow flip-flop. The Exit instruction will restore the overflow flip-flop setting from this reserved location.

Comparison Flip-Flops

Two hardware flip-flops make up the comparison logical unit. These two flip-flops have the following four combinations (0 = OFF, 1 = ON):

a. 00 – cleared.

b. 01 – greater or high comparison result.

c. 10 – less or low comparison result.

d. 11 – zero or equal comparison result.

These four states represent the result of executing an instruction that affects these logical units. The cleared state actually indicates that there is no comparison result existing. The instructions that set a result into the comparison flip-flops and are reflected on the appropriate console indicators are:

a. All arithmetic instructions.

b. All floating point instructions.

c. Compare instructions.

d. Move Numeric instruction.

e. Move Alphanumeric instruction.

f. The bit test instruction.

g. The logical instructions.

h. The scan instructions.

i. The Edit instruction.

j. The Scan Result Descriptor instruction.

k. Search instruction.

Any branching that is done on the basis of the comparison flip-flops does not change their status. Only another instruction that affects them can change their status. When entering control state by means of the Branch Communicate instruction or the automatic interrupt system, the status of the comparison flip-flops is stored. The 2-bit and 1-bit of the same character that stores the overflow flip-flop status will contain the status of the comparison flip-flops. The flip-flops are then cleared before branching to control state. When return is made to the normal state, the Branch Reinstate instruction will restore the comparison flip-flops from the character in reserved memory. Similarly, when entering a subroutine, the Enter instruction stores the comparison flip-flops in the 2-bit and 1-bit of the specified character in the memory stack. This same character contains the overflow flip-flops status. When leaving the subroutine with the Exit instruction, the comparison flip-flops are restored from this character in the stack.

EBCDIC/USASCII Mode Flip-Flop

This flip-flop determines whether the processor is operating on EBCDIC or USASCII internally coded data. The OFF state of the flip-flop indicates that the processor is using the EBCDIC code. The flip-flop can be programmatically set ON to indicate that the processor is to use USASCII code. The Set Mode instruction sets or resets this flip-flop, as desired by the programmer. The following instructions are sensitive to the setting of the EBCDIC/USASCII mode flip-flop:

a. All Arithmetic instructions.

b. All Floating Point instructions.

c. Move Numeric instruction.

d. Move Alphanumeric instruction.

e. Move Repeat instruction.

f. Translate instruction.

g. Scan Delimiter Equal instruction.

h. Scan Delimiter Unequal instruction.

i. Edit instruction.

When branching to the control state, the setting of the EBCDIC/USASCII mode flip-flop is also stored in the 8-bit of the same character containing the settings of the overflow and comparison flip-flops. It is then cleared prior to entering the control state. This is done by either of the following:

a. Branch Communicate instruction.

b. Automatic interrupt branch.

When returning to normal state, the Branch Reinstate instruction will restore the EBCDIC/USASCII mode flip-flop from the character in reserved memory. When entering a subroutine, the Enter instruction will store the status of the mode flip-flop in the 8-bit of the specific character in the stack which also contains the overflow and comparison flip-flop settings. The Exit instruction will restore the EBCDIC/USASCII mode flip-flop from the character in the stack when leaving the subroutine. This is necessary in the event that the flip-flop is changed by the subroutine. The special character in reserved memory or the stack contains the setting of the EBCDIC/USASCII mode flip-flop in the 8-bit, the setting of the overflow flip-flop in the 4-bit, and the settings of the comparison flip-flops in the 2-bit and 1-bit.

Interrupt Flip-Flop

The interrupt flip-flop is a hardware logical unit that indicates the presence of an interrupt. This flip-flop controls the automatic interrupt circuitry when the processor is operating in normal state. If the flip-flop is OFF (no interrupt condition), execution continues in sequence from instruction to instruction. If an interrupt occurs, the flip-flop is turned ON. If the flip-flop is ON at the completion of an instruction execution cycle, the automatic interrupt branch to control state, base zero occurs. The flip-flop is turned ON by the detection of any I/O complete interrupt. The Scan Result Descriptor instruction will turn the interrupt flip-flop OFF while executing the interrupt handling routine.

Normal/Control State Flip-Flop

The setting of this flip-flop dictates the state of operation of the processor. When it is ON, the processor is operating in normal state and allows the execution of the automatic interrupt branching. This flip-flop can only be turned ON by the Branch Reinstate instruction which is executed by the Operating System. It is turned OFF by either the Branch Communicate instruction or the automatic interrupt branch. When it is OFF, the processor is operating in control state which inhibits the automatic interrupt circuitry.

Timer

The timer, as previously described, consists of two words in address memory (see figure 3-1). The first timer word is counted at a 1 KC rate. This word is compared with the value of the second word which is placed there by the Operating System. When the first word is equal to or greater than the second word, a clock interrupt occurs. The timer will continue to count after the interrupt and requires the Operating System to read and clear the first word of the timer. The value read from the timer word is used by the Operating System for logging functions and updating the real-time clock.

Base Register

The base register in the processor is a three-digit register. These three digits are always added to the two high-order digits of the 5-digit program and instruction address to form a six-digit absolute address. This makes the base register modulo 1000, that is, a base register value of 137 is actually 137,000. This base register value is always added to the base relative addresses contained in the instructions. This computation takes place during the fetch cycle, prior to storing the absolute address generated into address memory. For any program, the base register value is created by the Operating System and stored in reserved memory location 000070 (table 2-1) prior to initiating the program. When the Branch Reinstate instruction is executed, the base register is set to the value contained in reserved memory establishing the base register of the normal state program. If a Branch Communicate instruction or an automatic interrupt branch is executed, the base register value is stored in the reserved memory location prior to entering control state and the base register is also cleared to zero.

Limit Register

The limit register within the processor is a three-digit register. The purpose of the limit register is to provide memory protection. Memory protection is

accomplished by comparing the high-order three digits of the absolute address generated for instructions with the base and limit registers. The base register provides the lower limit and the limit register provides the upper limit. The value of the limit register is provided by the Operating System and stored in reserved memory location 000073. The Branch Reinstate instruction sets the limit register to the value contained in reserved memory. When the Branch Communicate instruction or automatic interrupt branch is executed, the limit register value is stored in reserved memory prior to entering control state and the limit register is set to the system memory size. This allows the Operating System to access all memory.

Index Registers

The index registers used in a B 2500 or B 3500 System are not hardware registers like the base and limit registers. Three index registers are contained in reserved locations of an object program and are always assigned the same base relative address. The format of the index register is shown in figure 5-5.

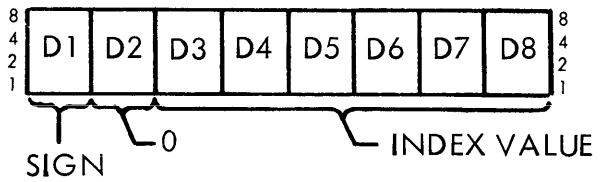

Figure 5-5. Index Register Format

Each index register consists of eight digit positions. The most significant digit (D1) is the sign of the index value. The second digit position is not used when indexing. The value of the index is the decimal value contained in the remaining six digit positions (D3 through D8). If an instruction address specifies indexing, the value of the specified index register is added algebraically to the base register, plus the base relative address prior to storing the generated address in address memory. The index register value can be changed by any instruction that addresses memory. In addition, the Enter and Exit instructions use and alter the setting of Index Register 3 (IX3); however, the settings are saved and restored. In the zero-base state, the Scan Result Descriptor instruction and the Search instruction use IX1 in its execution. Refer to the B 2500 and B 3500 Assembler Reference Manual (1034949) for further details on specific instructions.

STACK

The memory stack was previously mentioned with respect to storing the mode, overflow, and comparison flip-flop status prior to entering a subroutine. The stack is an area of memory that has been reserved by the programmer in which to store subroutine linkage words. The beginning address of the stack is stored in the base relative reserved memory location 000040. When an Enter instruction is executed, the address of the stack is obtained from base relative location 000040 and into this stack is automatically stored:

a. The six-digit address of the next instruction.

b. The eight-digit contents of Index Register 3.

c. One character containing the status of the mode, overflow, and comparison flip-flops.

d. The parameters as specified by the Enter instruction.

Index Register 3 is set to the address of the beginning of the stack, and reserved memory location 000040 is set to the address following the parameters (beginning of the next stack) in the event that another subroutine is entered from the one that is being executed. As additional nested subroutines are entered, the same storage process of linkage words into the stack takes place. As the subroutines are exited, return to the preceding level occurs by restoring the values of registers from the stack linkage words. These exits occur until the object program is reached at which time IX3, the address in 000040, and the logical flip-flops are restored to the conditions existing at the time of the first Enter instruction execution. This stack concept greatly simplifies the ability to call on subroutines and to make nested calls on other subroutines.

ADDER

The processor uses an adder that accumulates two fields from the most significant to the least significant digit positions. Reverse addition, as incorporated in B 2500 and B 3500 Systems, has the advantage of detecting an overflow condition prior to altering the receiving field for the result. The principle used in this type of adder is illustrated by the flow chart in figure 5-6 and the five examples in figure 5-7. If the data fields are signed, sign manipulation takes place prior to the addition since they are the most significant digits.

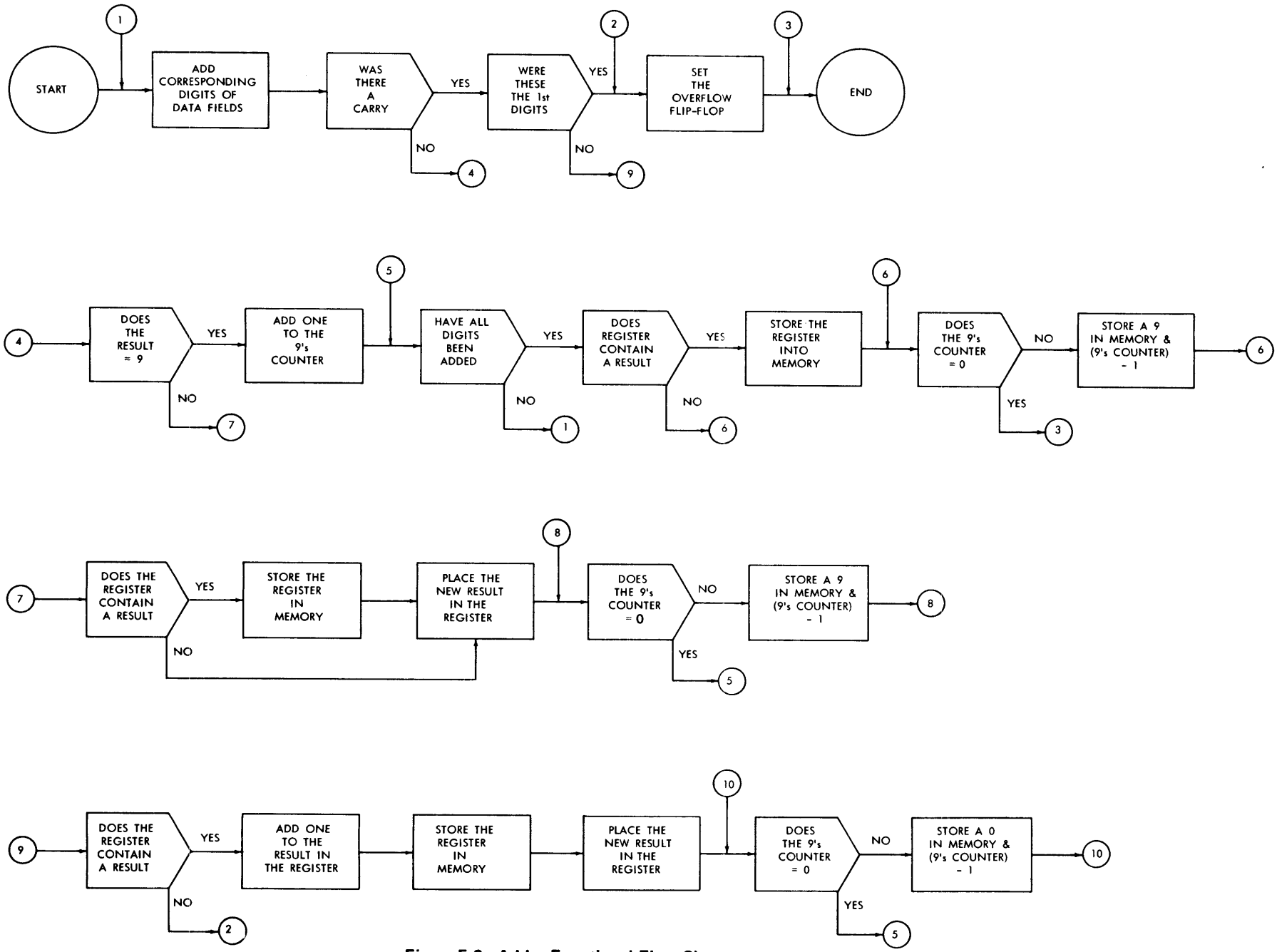

Figure 5-6. Adder Functional Flow Chart

EXAMPLE 1:

```
          12343
          12343
RESULT    24686
```

EXAMPLE 2:

```
          12345
          92345
RESULT 1: 0 + CARRY
FINAL RESULT: OVERFLOW FLIP-FLOP SET
```

EXAMPLE 3:

```
          876543229
          123455779
RESULT 1: 999998998 + CARRY
FINAL RESULT: 999999008
```

EXAMPLE 4:

```
          0876543
          0123457
RESULT 1: 0999990 + CARRY
FINAL RESULT: 1000000
```

EXAMPLE 5:

```
          876543
          123457
RESULT 1: 999990 + CARRY
FINAL RESULT: OVERFLOW FLIP-FLOP SET
```

Figure 5-7. Adder Examples

In figure 5-7, there is no manipulation of signs shown. The addition of two data fields is only shown to present the technique of a left-to-right adder.

In example 1, as each set of digits is added, no carry is generated and no nines are produced. As each new result is generated by the adder, the previous result is stored in the result field in core memory. In example 2, an overflow condition is immediately detected because of a carry on the first digit addition. In example 3, the first five nines are not stored until the result equal to eight is generated. The eight is retained until the carry is generated when adding the last digits, at which time the eight is made into a nine and stored. The following nines are then stored as zeros in the receiving field, and then the final digit (8) is stored. Nothing is stored in example 4 until the final digits are added. The receiving field in example 5 remains unchanged even though an overflow condition is not detected until the final digits are added. This is due to the result being contained in the nine's counter of the adder.

CONSOLE

The operator's console (figure 5-8) consists of two panels: a display panel and a control panel. The display panel is the vertical upper panel; the control panel is the curved lower panel that is placed on a slope with the display panel.

Display Panel

The display panel contains a NIXIE® tube display and back-lighted fixed message displays. The display panel can be divided into three areas as follows:

a. A NIXIE tube display consisting of two groups of tubes representing six contiguous digits of memory data or address information. Each group is appropriately identified by one of three legends which are illuminated directly below the tube display when the system is operating in that particular mode. Each tube position is capable of displaying all 16 digits of the extended binary set. Undigits will be displayed as their decimal value, less ten, with a slash through the digit. A halt, either programed or manual, displays the legend OP AF BF and INSTRUCTION ADDRESS. An 8-digit instruction (Address Branch, Exit, Halt Branch) displays its Op Code on the left side of the display panel and the instruction address on the right side.

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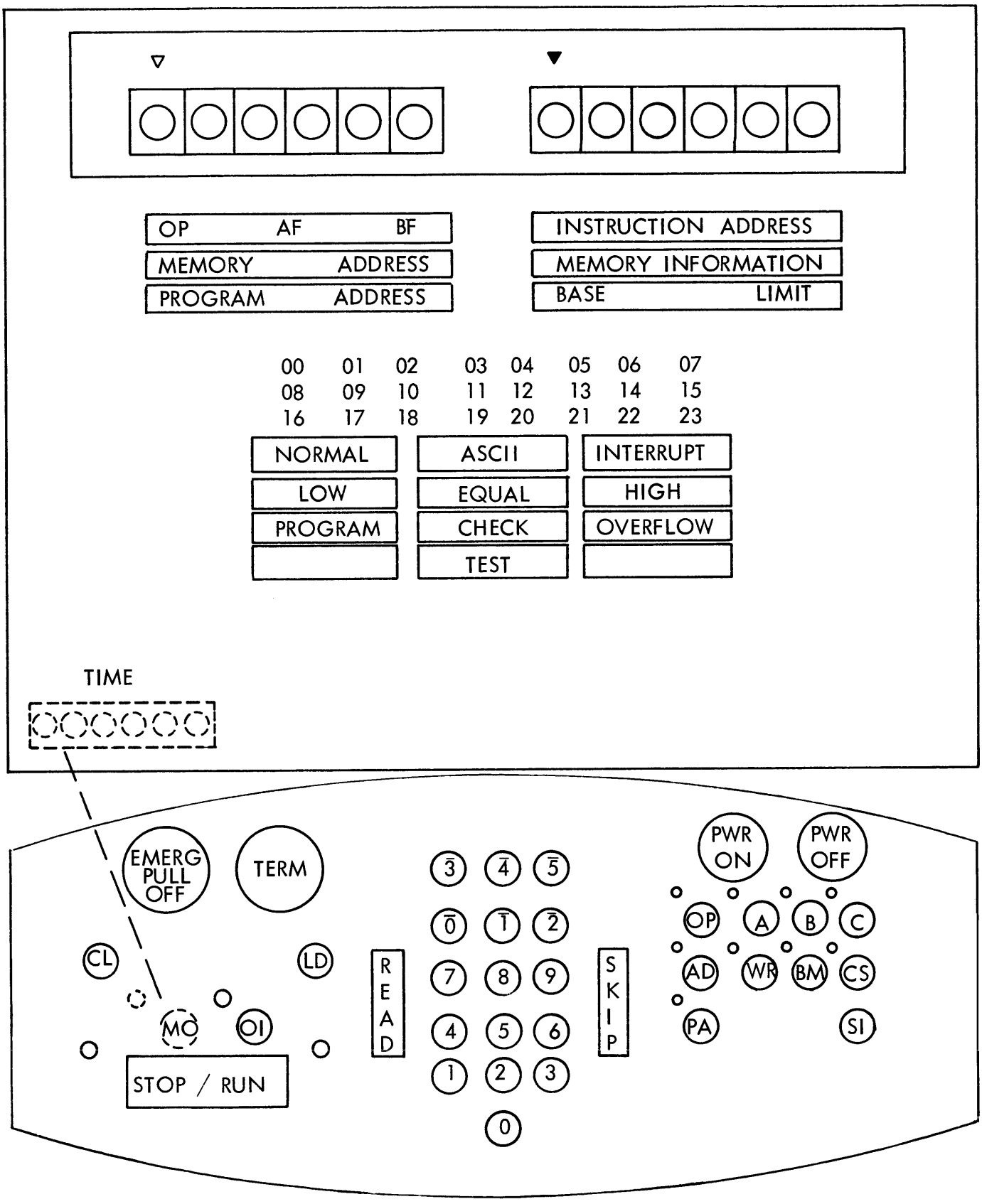


Figure 5-8. Operator's Console

When indirect field length is specified in the AF or BF fields, the display in the AF or BF positions is the resultant field length and not the bit combination specifying indirect field and its address. When a literal is specified in the AF field, the bit combination specifying the literal operand and the bit combination specifying the controller are cleared to zero before display. Subsequent use of the A key on the control panel displays the address of the operand and not the literal. The left group of six NIXIE tubes on the display panel reflects:

1) OP AF BF (first interruption syllable).

2) MEMORY ADDRESS.

3) PROGRAM ADDRESS.

The right group of six NIXIE tubes reflects:

1) INSTRUCTION ADDRESS.

2) MEMORY INFORMATION.

3) BASE and LIMIT (registers).

b. Twenty back-lighted channel indicators (00-19) that illuminate when an appropriate channel is busy, and are used for testing purposes. Indicators 20-23 are used by the Maintenance Test Routine (MTR).

c. Back-lighted, fixed-message indicators which reflect the state of the logical flip-flops. Control state operation is indicated by the NORMAL indicator not being lit. The PROGRAM indicator lights when an invalid operation or an invalid address is encountered. The PROGRAM and CHECK indicators light when an instruction time out occurs. The CHECK indicator lights if a parity interrupt occurs. The INTERRUPT indicator lights if a logical interrupt is not completed. A complete list of the indicators is as follows:

1) NORMAL.

2) LOW.

3) PROGRAM.

4) ASCII.

5) EQUAL.

6) CHECK.

7) TEST.

8) INTERRUPT.

9) HIGH.

10) OVERFLOW.

An optional feature is provided with the B 2500/B 3500 operator console to time certain operations or program runs as desired by the operator. This feature is a time indicator consisting of six NIXIE tubes located on the display panel and a time indicator control switch located on the control panel.

Control Panel

The control panel consists of keys which allow the operator to enter information into registers or memory, keys to control the display of information, a key to start and stop the processor, one key for emergency power off, one key for terminating operation, and keys for power on and off. The uses of these keys are as follows:

CL (CLEAR) KEY

When this key is pressed, all of the flip-flops in the processor, I/O controls, central control, and memory control are reset to the cleared state and the limit register is set to the system memory size. This key is only active when all I/O operations are completed and the processor is halted.

LD (LOAD) KEY

After the system has been cleared by the CL key, pressing this key initiates the normal load operation. Loading of the Operating System is performed on the I/O channel that has been predesignated (normally the systems memory or a disk unit) by the field engineer.

STOP/RUN KEY

The STOP/RUN key serves two functions. If the processor is running, pressing the key causes the processor to stop. If the processor is stopped, pressing the key causes the processor to continue

execution of the stopped program. A stop will only occur at the end of the instruction being executed; the keyboard is inactive until all of the I/O operations are completed. The status of processor operations is indicated by the stop or run indicators located near the STOP/RUN key.

SI (SINGLE INSTRUCTION) KEY

This is a single step key which is active when the processor is in a stopped status. Pressing this key causes the current instruction displayed in the NIXIE tube display to be executed and the next instruction to be fetched and displayed in the NIXIE tube display. If the current instruction is a Halt instruction, only a fetch and display of the next instruction occurs.

OI (OPERATOR INTERRUPT) KEY

The system may be interrupted temporarily by the operator pressing this switch.

MO (TIME METER OFF) KEY

When the time indicator option is provided with the B 2500 or B 3500 System, this switch turns the time indicator located on the display panel off if the processor is in the Halt state. The RUN key turns the time indicator back on.

OP KEY

This key is active in the stopped status only. Pressing this key causes the OP AF BF and address of the current instruction tube displayed in the left and right groups of NIXIE tubes, respectively. Digits can then be entered, right to left, into the OP AF BF register from the keyboard. The entry of the first digit blanks the left-most NIXIE tubes and the first digit will be displayed. The remaining digits will be displayed as they are entered from the keyboard.

A, B, AND C (FIELD ADDRESS) KEYS

These three keys all essentially perform the same function as the OP key and are only active when the processor is in a stopped status. Pressing any one of the three keys causes the OP AF BF of the current instruction to be displayed in the left group of NIXIE tubes. The right group of NIXIE tubes will contain the A, B, or C field address of the instruction, depending on whether the A, B, or C key was pressed.

PA (PROGRAM ADDRESS) KEY

This key is only active in the stopped status. Pressing the key causes the program address of the next instruction to be displayed in the left group of NIXIE tubes. The three-digit base register and three-digit limit register values will be displayed in the right group of NIXIE tubes. The program address can be changed by entering digits from the keyboard. Entry of the first digit blanks the display and the first digit of the new program address will be displayed. A limit of six digits can be entered, at which time the keyboard becomes inactive.

AD (ADDRESS) KEY

This key is only active in the stopped status. When the key is pressed, the memory address register is displayed in the left group of NIXIE tubes and the information contained at that address is displayed in the right group of NIXIE tubes. A limit of six digits can be entered from the keyboard to change the memory address. Entry of the first address digit blanks the remaining display and will move from right to left. The entered digits are shifted with newly entered digits following, until the register is full.

WR (WRITE) KEY

This key can only be used after pressing the AD key and is used to write new information into core memory, a digit at a time, via the keyboard. The memory address register advances one digit position for each entry. The digit currently contained at the memory address appears left-justified in the right group of NIXIE tubes, and the keyboard entry digit is right-justified. If it is not necessary to change a digit, it can be bypassed by means of the SKIP key. Once the WR key is pressed, the write function is active until one of the other keys is pressed (other than a digit or SKIP key).

SKIP KEY

This key is only active after the WR key has placed the keyboard into a write function status. Pressing this key causes the memory address register to increase by one digit position. It is used to skip over

digit positions that are not to be changed in core memory.

READ KEY

This key is active only after the AD key has been pressed. When displaying information from core memory, this key causes the next digit (or groups of digits) to be read from memory and displayed in the right group of NIXIE tubes. The memory address is increased by one if the address is not modulo-4. Once the address is modulo-4, words will be read out and the address will increment by four.

BM (BASE MEMORY) KEY

When this key is pressed and used in conjunction with other appropriate keys, the memory address, program address, or instruction address is displayed base relative instead of its absolute systems address.

CS (CONTROL STATE) KEY

This key is used in conjunction with the SI (single instruction) key. In normal state, the SI key causes execution of a single instruction. If the execution of that single instruction causes a return to control state when this key is active, all control state instructions are executed continuously and the processor halts only when normal state is reinstated. Thus, the execution of a Branch Communicate instruction consists of the execution of all control state instructions associated with the Branch Communicate.

TERM (TERMINATE) KEY

This key performs the same function as the CL (clear) key except that this key is always active and provides an absolute means of halting the processor which otherwise may not be able to be halted because of undefined hardware or software difficulties. The halt is immediate and all displays are blank.

DIGIT KEYS

A total of sixteen digit keys on the keyboard are available for manually entering information into the system. The ten keys, labeled 0 through 9, represent the 4-bit binary values of decimal digits 0 through 9, whereas the other six keys, labeled $\overline{0}$ through $\overline{5}$, represent the 4-bit binary values of 10 through 15 for entering the upper 4-bit stack of 8-bit character combinations. The transfer of this information is controlled by the previous pressing of an appropriate control key. The keyboard is active in the stop state and inactive in the run state.

EMERG PULL OFF (EMERGENCY POWER) KEY

This switch provides a signal to an external device that causes power to be removed from all of the units. This signal is not distributed to the system and no system unit has the capability to respond to this signal. It is provided for emergency conditions only and must not be used for normal power shutdown operations.

PWR ON KEY

This key is used to apply power to the system.

PWR OFF KEY

This key is used to remove power from the system.

Load Function

Two types of Load commands are available for the B 2500/B 3500 Systems. The first type, called Universal Load, permits the operator's selection of the input media; the second type, called Normal Load, restricts the selection of the input media to that of a particular peripheral unit (normally systems memory or disk). The two types of Load commands are discussed in the following paragraphs.

NORMAL LOAD

The Normal Load operation is initiated by clearing the computer by pressing the CL (clear) key and the LD (load) key. Pressing the LD key writes a 2-digit channel number and the first syllable of an I/O descriptor into reserved memory starting at address 000000. The channel number and I/O descriptor is predesignated by the user and is a field engineering modification. To retrieve a new copy of the MCP by the quickest means available requires that the LD key be wired to call on the appropriate disk channel on which the resident MCP is stored. After writing the channel number and I/O descriptor into core memory, the proces-

sor will initiate an I/O operation using the information in address 000000. The hardware automatically sets the beginning address to 001000 and the ending address to 001400. If the I/O unit is systems memory or a disk file, the segment address is set to zero. The processor idles until the interrupt flip-flop is set by the I/O control unit at the completion of the I/O operation. The processor then automatically branches to absolute address 001000 and begins executing the program that was just loaded. If an exception condition occurs, the Load operation must be repeated by the systems operator. It must be noted that if the I/O unit is designated as systems memory or disk, a previously cold-started MCP or MCP loader operation must have been accomplished after a power-off condition.

UNIVERSAL LOAD

The Universal Load operation is initiated by the operator in the following manner:

a. Press the STOP/RUN key to stop the system.

b. Press the CL (clear) key to clear the system.

c. Press the AD key and then the WR key.

d. Starting at absolute address 000000, enter the two digits for the channel number and the six digits (first syllable) of the I/O descriptor. This allows the operator to select any channel and the input peripheral unit which contains the cold-start or MCP loader deck (or images).

e. Press the OP key and enter Op Code 66 into the OP register by typing 660000 on the keyboard.

f. Press the STOP/RUN key to start the system.

When the STOP/RUN key is pressed at this point, the processor executes a Load operation that selects the control program from a "SYSTEM" magnetic tape and loads it. The processor will now go into a pseudo initiate I/O cycle in which the channel number and the first syllable of an I/O descriptor are obtained from core memory starting at address 000000.

The beginning and ending addresses for the I/O descriptor are set to 001000 and 001400 respectively and the segment number, when systems memory or a disk file is used, is set to zero. Having completed the initiate I/O cycle, the processor idles until the interrupt flip-flop is set, signifying completion of the I/O operation. When the interrupt flip-flop is set, the processor transfers the absolute address of the pertinent result descriptor to IX1 and clears the result descriptor area to zero after transferring the two most significant bits of the result descriptor to the comparison flip-flops. If the comparison is high (operation complete and no exceptions), the processor executes a Move Alphanumeric instruction with a field length of 100 for both the A and B fields. The address controllers for the A and B fields are 8-bit format and unsigned 4-bit format respectively. The A and B addresses are both 001000. This move strips off the zone bits (most significant digit of a character) and compresses the field to 100 4-bit digits. A branch is then taken to location 001000.

If the comparison is equal, indicating that the peripheral control returned an exception bit, operation contained in the above paragraph is automatically retried.

An invalid descriptor causes the processor to halt and, the comparison LOW indicator is set.

SECTION 6
INPUT/OUTPUT SYSTEM

GENERAL

The input/output system of the B 2500 or B 3500 Systems consists of the input/output channels and the input/output or peripheral controls/exchanges. All of the input/output operations are initiated, but are not executed by the processor. The execution of any specified input/output operation is accomplished by an I/O control unit. The I/O operation may be executed simultaneously with a processor operation and other previously initiated I/O operations on other I/O channels. The type of input/output operation is determined by an I/O descriptor that is transferred to the input/output control by an initiate I/O operation of the processor. At the conclusion of an I/O operation, a result descriptor specifies any exception condition requiring program operation, as well as other pertinent information.

I/O descriptors differ from processor instructions in that the addresses do not specify address controllers or index registers. The I/O descriptor addresses are machine absolute and not base relative. This permits I/O operations to be processor independent and also to be independent of the base and limit registers.

The number of addresses in the various descriptors varies. Where no memory accesses are involved, such as in Magnetic Tape Backspace, no address syllables are required. If the data area required is of fixed length, such as punch or print operations, only the MSD address is required. Also, in certain special cases, extra parameters are required which use one additional syllable. An example is in the case of disk file descriptors which require disk file segment addresses in addition to memory addresses.

Other than above, the most significant digit address and the least significant digit-plus-one address represent the maximum memory bounds of the record being transmitted. A record may or may not reach its maximum memory bound, but an attempt to exceed this limit will cause transmission of data to that area to be terminated. For instance, cards may be read into an area greater than 80 characters, i.e., with the MSD and LSD+1 more than 80 characters apart, or they may be read into an area of less than eighty characters. For example, the record area defined in an object program reflects 40 characters in a card reader record. Columns 1 through 40 will be stored in the record area of memory and the card reader will continue to read columns 41 through 80, but will transmit no data into memory for those columns. This prevents other record areas, or storage, from being clobbered by the extra data and allows for conservation of memory allocations. The format of the I/O descriptor is given in section 1.

I/O CHANNEL

The input/output channel of a B 2500 or B 3500 System is essentially a transparent exchange between the attached I/O control unit and main memory. The total number of I/O channels that may be included on the system is dependent on the central control units used. If the central control and memory base cabinet are used (indicating a B 2500 System), the total number of I/O channels that can be used is six. Two Central Control B cabinets can be used on a B 3500 System, each capable of accommodating ten I/O channels. The I/O channels are numbered 00 through 19 and each channel has two reserved words in address memory (see figure 3-1). In addition, each I/O channel has four digits of reserved memory which will contain the result descriptor. A linkage address, used by the MCP, follows the result descriptor. Two Types of I/O channels may be used on a B 2500 or B 3500 System: a type A and a type B channel. Only half of the total maximum I/O channels can be type B channels. Thus, a maximum I/O channel configuration would have ten type B and ten type A channels.

I/O CONTROLS

An I/O control unit controls the operation of the peripheral unit(s) attached to that control. Each type of peripheral unit requires a different I/O control unit, e.g., a card reader I/O control cannot accommodate a magnetic tape unit, etc.

When an input/output operation is initiated by the processor, the I/O control on the specified channel receives the I/O descriptor and stores it. The specific I/O control then executes the input/output operation as specified by the self-stored I/O descriptor. The format of the I/O descriptor is explained in section 1 and a list of I/O descriptors appears in appendix B. At the completion of the input/output operation, a result descriptor (refer to section 1 and appendix C) is stored in the reserved memory location for the specific channel that was used for the operation, and the interrupt flip-flop is set.

All digits and bits of descriptors not defined are reserved for expansion and must be zero. Where use of the EBCDIC/BCL translator is required during memory accesses, its use is specified by a signal from the I/O control at the descriptor command and is accomplished automatically by the hardware.

If channel priority, or conflicts in requests for memory, causes a delay sufficiently long to cause loss of data, the condition is detected by the affected I/O control and reported in its result descriptor as a memory access error at the completion of the operation.

In all cases of input operation where an attempt is made to increment the beginning address beyond the ending address, transfers into memory are terminated.

The first two digits of each I/O descriptor are checked by the I/O control. If they are not valid for the type of control being used, no I/O operation takes place, the processor interrupt flip-flop is set ON, the invalid I/O bit of the processor result descriptor is set, and the result descriptor is stored.

All beginning addresses must be synchronized modulo-4 and all ending addresses must be even. If any core memory address is not so synchronized, no I/O operation takes place and a processor interrupt is initiated with the invalid I/O descriptor bit of the processor result descriptor set ON. Ending addresses refer to the first digit of the next field in memory, i.e., the least significant digit of the field, plus 1.

All I/O controls include the capability to respond to a Read Address instruction from the processor by allowing the transfer of the contents of either word of associated address memory to the processor.

The following paragraphs describe the different I/O control units used on the B 2500 and B 3500 Systems. All descriptor digits, or bits, which are not defined are reserved for future expansion and must contain zeros.

Card Reader Control (B 2110/B 3110)

The card reader I/O control executes the card reader I/O descriptors as initiated by the Operating System for any Burroughs card reader. Reading is terminated by reaching the ending address, or when 80 columns of information have been transferred to main memory. The control supplies blanks in the case of short cards, which are then stored in memory unless terminated by the ending address. This I/O control signals central control to automatically translate BCL to EBCDIC when reading BCL cards. One BCL character per card column is received from the card reader and one 8-bit EBCDIC character is stored in memory. A validity or read check error does not cause the card reader to go Not Ready, but bits are set in the result descriptor. The VALIDITY CHECK indicator or the READ CHECK indicator remains on until it is reset by the next Card Read command or by the systems operator. When a validity error occurs when reading BCL or EBCDIC, the I/O control will store the EBCDIC code 0110 1111, representing the ? character. When reading EBCDIC, 256 card-hole combinations are valid, including the combination for the EBCDIC ? character; when reading BCL, 63 card-hole combinations are valid, excluding the hole combination for the ? character.

CARD READER I/O DESCRIPTORS

The card reader I/O descriptors are shown in table 6-1.

Table 6-1
Card Reader I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Card Read BCL	20	RRRR	Begin	End
Card Read Binary	21	RRRR	Begin	End
Card Read EBCDIC	22	RRRR	Begin	End
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

R indicates reserved for future expansion.

Card Read BCL. A card is read into ascending memory locations beginning with the location specified by the A address (digits 7-12) and continuing to but not including the terminal location specified by the B address (digits 13-18). The contents of each card column occupies one alphanumeric character position in memory.

Card Read Binary. A binary card image is stored in ascending memory locations beginning with the location specified by the A address and continuing to but not including the location specified by the B address. The contents of each card column are divided into two 6-bit characters. The upper 6 bits are stored in the memory location specified by the A address; the lower 6 bits are stored in the memory location specified by the A address plus 2, and so forth for each column. The unsigned high-order bits of each 8-bit character are cleared during this operation.

Card Read EBCDIC. A card is read into ascending memory locations beginning with the location specified by the A address and continuing to but not including the terminal location specified by the B address. The contents of each card column occupies one alphanumeric 8-bit character position in memory.

Input Request Enable. When the card reader I/O control is able to receive an input, the control will return a result descriptor indicating that an operation has been completed, the card reader is Ready, and the START button on the reader has been pressed.

Input Request Disable. This descriptor makes the control insensitive to any condition the reader may present.

Test. This descriptor returns a result descriptor, indicating that the Test operation has been completed and the card reader is Ready (operation complete), or the reader is Not Ready (Op Not complete or exception), as appropriate.

RESULT DESCRIPTOR

The result descriptor exception bits for card reader operations are:

a. Bit 3 – card reader Not Ready.

b. Bit 4 – memory access error.

c. Bits 4 and 6 – validity error.

d. Bits 7-12 – reserved.

e. Bits 13-16 – unit number (0).

NOTE

A memory access error on any I/O operation reflects that a memory request was not handled before the next memory request occurred and information was lost during the I/O operaton.

Card Punch Control

The card punch I/O control executes card punch I/O descriptors and contains an EBCDIC/EBCDIC card-code translator. This control can signal the central control to perform EBCDIC to BCL translation of data when transferring from core memory to the I/O control. The control may contain one and only one of the following code translators in addition to the EBCDIC/EBCDIC card-code translator:

a. BCL/ICT card code.

b. BCL/BULL card code.

c. BCL/BCL card code.

Information is transferred to the punch as bit-serial for each punch position, with twelve separate 80-bit serial transfers to the punch being required to punch a card. Transfer of a given row to punch-2 consists of 40 bit-pairs. The punch control is sensitive to the EBCDIC code 1100 1111 (CF) in the data stream for cards being punched in BCL; is sensitive to the code 1xxxxxx (x represents any value) for cards being punched in binary, and will cause punching to be terminated from that column to the end of the card. Bit information to complete the terminated 80-column row is supplied by the control. The control is capable of punching binary information when required to do so by the object program.

CARD PUNCH CONTROL 1

This control is used with the B 9210 and B 9211 Card Punches. When a punch check, access, or memory error is detected during the punching of a card, the punching of that card is completed and the next card is punched. Both cards are sent to

Table 6-2
Card Punch I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12
Card Punch BCL	23	SRRR	Begin
Card Punch Binary	24	SRRR	Begin
Card Punch EBCDIC	25	SRRR	Begin
Input Request Enable	35	RRRR	
Input Request Disable	97	RRRR	
Test	99	RRRR	

R indicates reserved for future expansion.

the error stacker and the card punch remains in the Ready condition. The control will set the punch check bit in the second card result descriptor and turn off the PUNCH CHECK indicator on the punch.

CARD PUNCH CONTROL (B 2212 or B 3212)

This control is used with the B 9212 and B 9213 Card Punches. When a punch check, access, or memory error is detected by the control during the punching of a card, the punching of that card is completed and the card is sent to the error stacker. The punch check bit in the result descriptor is set for that card and the card punch remains ready.

CARD PUNCH I/O DESCRIPTORS

The card punch I/O descriptors are shown in table 6-2. Programmatic stacker selection is accomplished by the value of S in position D3. The stacker selected depends on the type of punch attached. The B 9210 has one stacker to which all cards are routed regardless of the value of S or whether a punch-detected error exists. The error stacker of the B 9211, B 9212 and B 9213 receives cards only as a result of a punch-detected error. S-values of 0 or 2 cause cards to be routed to the normal stacker; S=1, routes cards to the auxiliary stacker.

Digit 3 (S) may be:

a. 0 – normal stacker for all card punches.

b. 1 – normal stacker for B 9210, or auxiliary stacker for B 9211, B 9212, and B 9213.

c. 2 – normal stacker for B 9210 and B 9211, or error stacker for B 9212 and B 9213.

NOTE

The error stacker is also selected by the control when an error is detected.

Card Punch BCL. A card is punched from ascending memory locations beginning with the location specified by the A address. Punching is terminated by the EBCDIC code 1100 1111 (CF) or the punching of 80 columns. During punching, the EBCDIC/BCL translator is enabled and one of the three optional card-code translators is required to complete the data transfer.

Card Punch Binary. A card is punched from ascending memory locations beginning with the location specified by the A address. Punching is terminated by the code 1xxx xxxx (x represents any value) or the punching of 80 columns. The contents of each card column are divided into two 6-bit characters. The upper six bits are accessed from the memory location specified by the A address; the lower six bits are accessed from the location specified by the A address plus 2, and so forth for each column. The two high-order bits of each 8-bit character are not used except as a delimiter and must otherwise be zero.

NOTE

A total of 160 memory characters are required to punch 80 columns. Two 1xxx xxxx codes are required when punching less than 80 columns.

Card Punch EBCDIC. A card is punched from ascending memory locations beginning with the location specified by the A address. One column is punched for each EBCDIC memory character and 80 columns are always punched (blanks are required in memory if less than 80 columns are to be punched).

Input Request Enable. When the control is input-request-enabled, the control returns a result descriptor, indicating that an operation has been completed if, and when, the punch is ready.

Input Request Disable. The control is made insensitive to any condition the card punch may present.

Test. A result descriptor is returned, indicating a completed operation (Ready and no punch check), a Not Ready condition, or a punch check, as appropriate.

RESULT DESCRIPTOR

The result descriptor exception bits for the card punch operations are:

a. Bit 3 – card punch Not Ready.
b. Bit 4 – punch check or parity error.
c. Bits 4 and 6 – memory parity error.
d. Bit 5 – reserved.
e. Bit 7 – punch identification (test OP only).
f. Bits 8-12 – reserved.
g. Bits 13-16 – unit number (0).

NOTE

Bit 7 is set as part of the Test Command only if punches B 9211, B 9212, and B 9213 are being tested.

Paper Tape Controls

PAPER TAPE READER CONTROL (B 2120/B 3120)

This control is used with the B 9120 Paper Tape Reader. All paper tape controls can store or fetch one character per memory access. If the number of characters specified is not read, spaced, or backspaced due to termination by the reader, bit 7 is set in the result descriptor. If the termination was caused by the end-of-tape or beginning-of-tape reflective strip, bit 5 in also set.

If a tape parity or memory access error is encountered, the control continues the operation. The appropriate bits (4 and 6 or 4) are set in the result descriptor.

NOTE

The position of the tape after an access error(s) is indeterminate when the operation is terminated by the ending address.

PAPER TAPE READER I/O DESCRIPTORS

The paper tape reader I/O descriptors are shown in table 6-3.

Paper Tape Read. A record is read from the paper tape reader into ascending memory locations beginning at the location specified by the A address and continuing to, but not into the terminal location specified by the B address.

If the V variant contains a zero, only the least significant seven bits of the eight bits received from the reader, together with a high-order zero bit, are stored in memory. The parity error line from the reader is monitored.

If the V variant contains a 1, the eight bits received from the reader are transferred to memory via the BCL/EBCDIC translator; however, the translator will ignore the two most significant bits. The parity error line from the reader is monitored and the BCL paper tape code/BCL code in the reader is enabled.

If the V variant contains a 2, the eight bits received from the reader are transferred to memory. The parity error line from the reader is ignored.

Table 6-3
Paper Tape Reader I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Paper Tape Read	40	RRVR	Begin	End
Paper Tape Space	41	RRRR	Begin	End
Paper Tape Backspace	43	RRRR	Begin	End
Paper Tape Rewind	47	RRRR		
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

R indicates reserved for future expansion and V indicates a variant of the Op Code.

Paper Tape Space. The tape is spaced forward the number of characters specified unless stopped by an end-of-tape condition. The number of characters specified is the same as the number of characters read for the same A and B addresses. This I/O descriptor requires no memory space.

Paper Tape Backspace. The tape is spaced backward the number of characters specified unless stopped by a beginning-of-tape condition. The number of characters specified is the same as the number of characters read for the same A and B addresses. This I/O descriptor requires no memory space.

Paper Tape Rewind. The tape is rewound to the beginning-of-tape.

Input Request Enable. When the control is input-request-enabled, the control will return a result descriptor, indicating that an operation has been completed if and when the unit is ready.

Input Request Disable. The control is made insensitive to any condition the unit may present.

Test. The status of the designated unit is tested and a result descriptor is returned.

RESULT DESCRIPTOR

The result descriptor exception bits for paper tape reader operations are:

a. Bit 3 – paper tape reader Not Ready.

b. Bit 4 – memory parity error.

c. Bit 5 – end-of-tape or beginning-of-tape.

d. Bits 4 and 6 – tape parity error.

e. Bits 8-12 – reserved.

f. Bits 13-18 – unit number (0).

NOTE

An incomplete record means that an end-of-tape or beginning-of-tape was encountered prior to the completion of a Read or Space I/O operation, or the peripheral stopped because certain control code buttons on the paper tape reader were pressed.

PAPER TAPE PUNCH CONTROL
(B 2220/B 3220)

This control is used with the B 9220 Paper Tape Punch. All paper tape punch controls can fetch one character per memory access. When the number of characters specified is not written due to termination by the peripheral unit, the incomplete record bit is set in the result descriptor. Punching is not terminated by a low-paper condition. Bit 5 is set in the result descriptor after the punching operation is completed. During a Write operation, if a memory parity error is encountered, the punching will terminate immediately and the erroneous character is not punched. Bit 4 is set in the result descriptor.

If the number of characters specified is not punched due to termination by the punch, bit 7 is set in the result descriptor.

PAPER TAPE PUNCH I/O DESCRIPTORS

The paper tape punch I/O descriptors are shown in table 6-4.

Paper Tape Write. A record is punched on the paper tape punch from ascending memory locations beginning at the location specified by the A address and continuing to, but not from the terminal location specified by the B address.

Table 6-4
Paper Tape Punch I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Paper Tape Write	48	RRVR	Begin	End
Paper Tape Punch Leader	49	RRRR	Begin	End
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

R indicates reserved for future expansion and V indicates a variant of the Op Code.

If the variant contains a 0 (zero), the eighth bit received from memory is ignored and an even parity bit is sent on the eighth line.

If the variant contains a 1, the EBCDIC/BCL translator is enabled. The control will terminate the operation when the delimiter (1000 0000) is detected; the delimiter is not sent to the punch. The seventh bit received from memory is ignored, a zero bit is forced on the seventh line, and an even parity bit is sent on the eighth line. The BCL/BCL paper tape code translator in the paper tape punch is enabled to complete the data transfer.

If the variant contains a 2, the control sends all eight bits received from memory to the paper tape punch. Parity is neither generated nor sent.

Paper Tape Punch Leader. A record consisting of all holes is punched on the paper tape punch. The number of characters punched is given by the A and B addresses.

Input Request Enable. When the control is input-request-enabled, the control will return a result descriptor, indicating that an operation has been completed if and when the unit is ready.

Input Request Disable. The control is made insensitive to any condition the unit may present.

Test. The status of the designated unit is tested and a result descriptor is returned.

RESULT DESCRIPTOR

The result descriptor exception bits for paper tape punch operations are:

a. Bit 3 – paper tape punch Not Ready.

b. Bit 4 – memory parity error.

c. Bit 5 – low-paper condition.

d. Bit 7 – incomplete record.

e. Bits 8-12 – reserved.

f. Bits 13-18 – unit number (0).

NOTE

An incomplete record means that the peripheral stopped because certain control code buttons on the paper tape punch were pressed.

Line Printer Controls

A line printer control executes I/O operations on the buffered and unbuffered line printers.

BUFFERED LINE PRINTER CONTROL

This control is used with the B 9240 and B 9241 Buffered Line Printers. It signals central control to perform automatic EBCDIC to BCL translation on the data as it is transferred from core memory to the I/O control. The EBCDIC code 1100 1111 (CF) in the data stream is translated by the EBCDIC/BCL translator to 1000 0000 (80). When the I/O control detects the 1 in bit position 8, memory accesses are terminated and the remaining positions of the printer buffer are filled with blanks.

The I/O control contains a one-character buffer which receives information from core memory serially-by-character and transfers information to the printer serially-by-character. Transfer of paper-motion information takes place after the printer buffer is filled. The I/O control is capable of loading the printer buffer while paper motion is occurring in response to a previous descriptor. After the paper motion of the previous command is completed, format information is received for the information in the buffer, which can now be printed. The print-check error bits refer to the line associated with the previous descriptors, and the current descriptor is executed. The memory parity error bits refer to the current line, and the current descriptor is executed. The end-of-page signal from the printer carriage control tape sets the end-of-tape bit in the result descriptor; if the current descriptor specifies no skipping, the current descriptor is executed. The EBCDIC to BCL translator is enabled by the control for printing operation. The control can be used with one printer, or with two if one of the pair includes the dual printer adapter. If the dual printer switch is set at the BOTH position, the same information is printed by both printers simultaneously.

UNBUFFERED LINE PRINTER CONTROL
(B 2240/B 3240, B 2242/B 3242)

This control is used with the B 9242 and B 9243 Unbuffered Line Printers. It signals central control to perform EBCDIC to BCL translation on the data as it is transferred from core memory to the I/O control. The EBCDIC code 1100 1111 (CF) in the

data stream is translated as in the buffered control. When the control detects the digit 1 in bit position eight, this indicates the end of the line.

This I/O control contains a two-character buffer which receives information from core memory via the translator, two characters at a time, for comparison with the six bits (plus parity code) corresponding to the upcoming graphic on the printer. The control will also check the six bits (plus parity code) presented by the printer for odd parity.

The control transfers bit-serial information to the printer column buffer for each comparison. A 1 bit indicates a true comparison and a 0 bit indicates a false comparison. The printer must receive bit information for all columns, two bits per transfer.

A counter, to keep count of the number of graphics left to be printed, is contained in the control. The initial count is a function of the number of print positions in the printer; the length of the line is determined by the EBCDIC code 1100 1111 (CF) in the data stream, and the number of blanks is determined by the EBCDIC code 0100 0000 (40) in the printer line.

The printer control includes a quick release feature which terminates scanning and enables start of paper motion as soon as all non-blank characters have been printed, thus gaining absolute speed over short lines of print. Printing speed with this feature is unpredictable; however, line rate is greater than 815 LPM and less than 1400 LPM (the hardware upper limit).

The error bits (memory parity, bit transfer, code parity) of the result descriptor refer to the line associated with the current descriptor, and the current descriptor is executed. If a memory access is missed, the control waits until the same graphic is presented to the control the second time and then continues, providing automatic recovery.

Overprinting shall not occur and, replicated sets of graphics are not acceptable. The control requires that 64 unique codes be received from the printer during each drum revolution. Note that this permits a character set of 64 graphics.

LINE PRINTER I/O DESCRIPTORS

The line printer I/O descriptors are shown in table 6-5.

The following designations are used for digits 3-6:

a. R – reserved for future expansion.
b. S – spacing requirement.
c. U – unit number.
d. N – skip-to-channel number in carriage-control tape.

Printer Write. A line of data is printed from ascending memory locations beginning with the location specified by the A address. The length of the line is determined by the EBCDIC code 1100 1111 (CF) in the data stream or by the number of printer columns (120, 132), whichever is encountered first. Spacing or skipping as specified by digits D3, D5, and D6 takes place after printing. Skipping takes precedence over spacing. Print characters which are not assigned a 6-bit code are translated by central control as the EBCDIC ? character. Coding for digits D3, D4, D5, and D6 is as follows:

a. D3 – 0 (no space).
b. D3 – 1 (single space).
c. D3 – 2 (double space).
d. D4 – 0 (printer number one).
e. D4 – 1 (printer number two).
f. D5 and D6 – 00 (no skip).
g. D5 and D6 – 01 through 11 (skip-to-channel nn).

Printer Skip. The number of lines as specified by digits D3, D5, and D6 are spaced. Skipping takes precedence over spacing. Coding is the same as for Printer Write.

Input Request Enable. When the control is input-request-enabled, the control will return a result

Table 6-5
Line Printer I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12
Printer Write	10	SUNN	Begin
Printer Skip	11	SUNN	
Input Request Enable	35	RURR	
Input Request Disable	97	RRRR	
Test	99	RURR	

descriptor, indicating that an operation has been completed if and when the printer is Ready.

Input Request Disable. The control is made insensitive to any condition the printer may present.

Test. A result descriptor is returned, indicating operation complete (Ready) or the printer is Not Ready, as appropriate.

RESULT DESCRIPTOR

The result descriptor exception bits for line printer operations are:

a. Bit 3 – printer Not Ready.
b. Bits 4 and 5 – bit transfer error.
c. Bits 4 and 6 – memory parity error.
d. Bits 4 and 7 – print check error and code parity error.
e. Bit 8 – reserved.
f. Bit 9 – end of page (hole in channel 12 of the carriage-control tape).
g. Bits 10-12 – reserved.
h. Bits 13-16 – unit number (0 or 1).

Magnetic Tape Controls

The magnetic tape control executes I/O operations for magnetic tape as specified by the specific I/O descriptor. If desired, the control can signal central control to perform automatic BCL to EBCDIC (input data) or EBCDIC to BCL (output data) translation, depending on whether an input or output 7-channel magnetic tape operation is being performed. In addition, the control can perform nonstop ("shoot the gap") forward operation if a second I/O operation is initiated in the prescribed minimum time.

An access error during a Read operation causes:

a. Characters between the first character which missed storage and the longitudinal parity check (LPC) character to be read, but not stored.
b. The LPC to be recognized by the control which causes the tape to stop in front of the record, or block, that is causing the read error.
c. The memory access error bit to be set ON in the result descriptor.

Read retries are not automatic in the control, but they are programed in the MCP.

An access error during a Write operation causes:

a. An indeterminate character to be written on tape in place of the missed character.
b. The indeterminate character to be sequentially written until the first character is read (if the first written character of the record has not yet been read). Thus, a record of valid size is created.
c. The tape to be stopped in front of the record, or block, that is causing the write error.
d. The access error bit to be set ON in the result descriptor.

Write retries are not automatic in the control, but they are programed in the MCP. Transfers into memory are terminated in all cases where input operations attempt to increment the beginning address beyond the ending address.

In all cases if an operation calls for the use of a non-present option, the control does not perform the operation and returns a result descriptor.

All magnetic tape controls can store or fetch two 8-bit characters per memory access. The number of memory cycles required is: ½ times the number of 8-bit characters per record, plus 1. The time between memory cycles is: 2 divided by the product of the speed and density (transfer rate).

The magnetic tape control with a cluster adapter senses a signal from the active tape station which indicates the type of head (7 or 9 track) on that station. It transmits data to or from the station only if the number of data channels matches the number of tracks. If an attempt is made to use a mismatched station, the Not Ready bit in the result descriptor is set.

NOTE

This precaution is required because a cluster with a 2X adapter permits any of its stations to be addressed, regardless of the type of head. Furthermore, station designation can be changed by the operator. Seven and nine track vertical self-standing transports are not permitted on the same exchange; therefore, the magnetic tape unit is not designed to recognize a head-type signal, even if present.

Magnetic tape I/O controls and magnetic tape I/O exchanges are described in the following paragraphs after a distinction is made between the two. The primary differences between an I/O control and an I/O exchange are:

a. The I/O control is associated with the I/O channel, and controls variables such as transfer rate, code sensitivity, etc., as related to a specific type of I/O unit.

b. The I/O exchange allows two I/O channels with their associated I/O controls to "float" on as an available basis between the same group of tape units, this allowing simultaneous Read/Write capabilities.

7-TRACK FREE-STANDING MAGNETIC TAPE CONTROL (B 2391 or B 3391)

This control is used with all 7-track free-standing transports. A maximum of six free-standing transports can be used on the control without an exchange, and a maximum of ten free-standing transports can be used with a 2 x 10 exchange. This control has the capability of operating at 200, 556, and 800 BPI densities. The ability to perform nonstop forward operations is also included.

9-TRACK FREE-STANDING MAGNETIC TAPE CONTROL (B 2393 or B 3393)

This control is used with all 9-track free-standing transports. A maximum of six free-standing transports can be used on the control without an exchange, and a maximum of ten transports can be used with a 2 x 10 exchange. This control has the capability of operating at 200, 800, and 1600 BPI densities; however, for 200 BPI density, a 200 BPI adapter is required.

9-TRACK CLUSTER MAGNETIC TAPE CONTROL (B 2381 or B 3381)

This magnetic tape control is used with the B 9381 and B 9382 Magnetic Tape Clusters (9-Track versions). Used in conjunction with a B 2680 or B 3680 Control Adapter and a B 9989 7-Channel Station Adapter, it provides for 7-Track cluster operation. This control has the capability of operating at 200, 800, and 1600-BPI densities, and can handle up to a maximum of eight cluster stations. However, for 200-BPI density, a B 2681 adapter is required.

2 x 8 CLUSTER EXCHANGE (B 2480, B 2481, B 3480, and B 3481)

The B 2480 or B 3480 (7-Track) and the B 2481 or B 3481 (9-Track) 2 x 8 exchanges provide for concurrent and independent reading and/or writing to any two different tape stations.

2 x 10 FREE-STANDING EXCHANGE (B 2490, B 2491, B 3490 and B 3491)

The B 2490 or B 3490 (7- or 9-Track) 2 x 10 exchanges are used with the B 9390, B 9391, B 9392, and B 9394 free-standing tape units. The B 2491 or B 3491 (9-Track) 2 x 10 exchanges are used with the B 9393 free-standing tape unit. These exchanges provide for concurrent and independent reading and/or writing to any two different tape stations.

MAGNETIC TAPE I/O DESCRIPTORS

The magnetic tape I/O descriptors are shown in table 6-6.

Table 6-6
Magnetic Tape I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Magnetic Tape Read Forward	02	FUVT	Begin	End
Magnetic Tape Read Backward	03	FUVT	Begin	End
Magnetic Tape Write	06	FUVR	Begin	End
Magnetic Tape Erase	04	FURR	Begin	End
Magnetic Tape Rewind	01	RURR		
Magnetic Tape Space Forward	08	FUNN		
Magnetic Tape Space Backward	09	FUNN		
Test	99	RURR		

The symbols for digits 3-6 represent the following:

a. F – density.

b. U – unit number.

c. V – variant of the Op Code.

d. T – track.

e. R – reserved for future expansion.

f. N – amount of spacing requested.

Variant coding for digits 3-6 are as follows:

a. D3 – 0 (800 BPI, even parity, not standard on 9 track).

b. D3 – 1 (800 BPI, odd parity).

c. D3 – 2 (555 BPI, even parity, 7 track only).

d. D3 – 3 (555 BPI, odd parity, 7 track only).

e. D3 – 4 (200 BPI, even parity, not standard on 9 track).

f. D3 – 5 (200 BPI, odd parity).

g. D3 – 7 (1600 BPI, odd parity, 9 track only).

h. D3 – 8 (density as selected by the tape unit, even parity).

i. D3 – 9 (density as selected by the tape unit, odd parity).

j. D4 – any digit 0 through 9 (unit number).

k. D5 – 1-3 (maintenance variant on read).

l. D5 – 2 (write a tape mark record – write).

m. D5 – 4 (EBCDIC/BCL translator enabled – 7 track only; meaningless on 9 track).

n. D6 – for a 9-track Read operation if the most significant bit is 1, the remaining three bits indicate the track which is to be corrected via the cyclic-redundancy-check correction adapter. If the most significant bit is 0, no correction is attempted and the remaining three bits are meaningless. For a 7-track Read operation, digit D6 is meaningless.

NOTE

The cyclic-redundancy-check character is a hardware means of generating another check character during Write operations and provides error correcting capabilities. During a Read, the generated cyclic-redundancy-check character must agree with the one that was written. This is a feature that is used to ensure a more reliable magnetic tape operation.

For a 7-track Read operation when the record length is less than the memory area defined by the beginning and ending addresses, the EBCDIC code 1100 1111 (CF) is stored after the last character that is read. This character is the least significant character for a Read Forward operation and the most significant character for a Read Backward operation. When a vertical parity error is detected, the EBCDIC code 1100 1100 (CC) is stored in memory in place of the character in error.

For a 7-track Write operation, the EBCDIC code 1100 1111 (CF) in the data stream terminates the Write operation. This code is not transferred to tape.

For a 7-track Read or Write operation in which the EBCDIC/BCL translator is not enabled, information is stored in or obtained from the lower-order six bits of a character. The two higher-order bits are cleared to zero for a Write operation.

An end-of-tape condition does not terminate an operation; the end-of-tape bit is set in the result descriptor. The incomplete-record bit is set ON in the result descriptor when a record which has been read is shorter than the read area defined by the beginning and ending addresses. Spacing or reading over six feet of blank tape automatically terminates the operation and returns a result descriptor with bit 12 set ON.

Magnetic Tape Read Forward. A record is read from the designated unit into ascending memory locations beginning with the location specified by the A address and continuing to, but not into the ending location specified by the B address. Reading is terminated by the detection of an interrecord gap.

Magnetic Tape Read Backward. A record is read from the designated unit into descending memory locations, beginning with the location specified by the B address minus 4 and continuing to, but not beyond the ending location specified by the A address, while the tape is moving in the reverse direction. A record occupies the identical memory cells when reading forward or backward only if the record length is equal to the memory area defined by the beginning and ending addresses. Reading is terminated by detecting an interrecord gap.

NOTE

The decremented B address is contained in the lower numbered address memory location and can be read via the Read Address instruction with a zero variant.

Magnetic Tape Write. A record is written in a forward direction on the designated unit from ascending memory locations beginning with the location specified by the A address and continuing to, but not into the terminal location specified by the B address.

Magnetic Tape Erase. Magnetic tape is erased in the forward direction on the designated unit. The number of characters erased is the same as the number of characters which would be written for the same A and B addresses. No memory space is used, but memory cycle time is used.

Magnetic Tape Rewind. Magnetic tape will be rewound on the designated unit to the beginning-of-tape. After the operation is initiated, a result descriptor is returned and the interrupt flip-flop is set ON. The result descriptor will contain the rewinding bit which is set ON. If the tape is already at the beginning-of-tape when the rewind is initiated, the rewinding bit will be set ON and the beginning-of-tape bit will reflect OFF status.

Magnetic Tape Space Forward. Magnetic tape is spaced forward the number of records specified by digits D5 and D6 (00 = 100 records) unless the tape is stopped by the detection of an end-of-file record.

Test. The status of the designated unit is tested and a result descriptor is returned. All bits except 4, 9, 10, and 12 are possible.

RESULT DESCRIPTOR

The result descriptor exception bits for magnetic tape operations are:

a. Bit 3 – tape unit Not Ready.

b. Bit 4 – memory access error (read, write, or erase).

c. Bits 4 and 6 – memory parity error (write or erase).

d. Bits 4, 7, and 8 – tape parity error (read, write, or space).

e. Bit 5 – end-of-tape or beginning-of-tape.

f. Bit 6 – write lockout (write or test) or end-of-file (read or space).

g. Bit 7 – incomplete record (read).

h. Bit 8 – attempt to exceed maximum address (read only).

i. Bits 7 and 8 – density switch (00 = 800, 01 = 555, 10 = 200, 11 = 1600).

j. Bit 9 – cyclic-redundancy-check correction possible (read).

k. Bit 10 – non-present option required or track in error (if bit 9 is set ON).

l. Bit 11 – rewinding or track in error (if bit 9 is set ON).

m. Bit 12 – spacing six feet of blank tape or track in error (if bit 9 is set ON).

n. Bits 13-16 – unit number.

Console Printer (SPO) Control (B 2340/B 3340)

The console printer (supervisory printer) control is used to control the supervisory printer I/O device, B 9340, Model 33 or Model 35 Keyboard Send-Receive Teletypewriter. The control contains a bidirectional translator which translates from EBCDIC to USASCII code. (Refer to appendix D.) All USASCII codes received from the typewriter which have no equivalent EBCDIC code become the null code (0000 0000). All EBCDIC codes sent to the typewriter which have no equivalent USASCII code become the USASCII code 1011

1111 (BF), which represents the USASCII question mark. Information between the console printer and the control is transferred serially by bit, whereas it is transferred serially by character between the control and main memory.

The control can be input-request-enabled, at which time the control is sensitive only to the USASCII ENQ code 1000 0101 (85) from the keyboard. When the control receives this code, a result descriptor with only bit 1 ON is generated and the interrupt flip-flop is set ON. The ENQ is not stored in memory.

Upon receipt of a Read descriptor, the control automatically generates a signal to light an indicator on the console printer and to await an input message from the systems operator. The control is sensitive to the USASCII ETX code 1000 0011 (83) in an input message which is translated to EBCDIC and transferred to core memory. The control is sensitive to the USASCII NAK code 1001 0101 (95) in an input message which is translated and stored in memory as 0001 0101 (15). The NAK code sets the interrupt flip-flop and stores a result descriptor with bits 1, 2, and 7 set ON. The control is then insensitive to inputs until an Input Request Enable descriptor or a Read descriptor is initiated. If the input message exceeds the buffer area defined by the beginning and ending addresses, the operation is terminated with the result descriptor bits 1, 2, and 8 set ON. If a carriage return and line feed are part of an output message, the message must be followed by a non-spacing, non-printing code. The control is sensitive after translation to the USASCII ETX code 1000 0011 (83) in an output message; the end-of-text code sets the interrupt flip-flop ON and stores a result descriptor with bit 1 set ON. If a maximum address is reached without ETX in an output message, the operation is terminated with the result descriptor bit 1 set ON. If the console printer is operating off-line, the Not Ready bit is set ON in the result descriptor of a Read, a Write, or a Test descriptor.

CONSOLE PRINTER I/O DESCRIPTORS

The console printer I/O descriptors are shown in table 6-7.

Read. The message being typed on the typewriter keyboard is read into ascending memory locations beginning with the location specified by the A address and continuing until an end-of-text code is detected, but not into the terminal location specified by the B address.

Write. A message is typed on the console printer from ascending memory locations beginning with the location specified by the A address and continuing until an end-of-text code is detected, but not from the terminal location specified by the B address.

Input Request Enable. With this descriptor the control is sensitive to only the inquiry code input from the keyboard ENQ key. This descriptor is valid only if the control is idle.

Input Request Disable. With this descriptor the control is made insensitive to any input from the keyboard, i.e., the control is placed in an idle condition. The descriptor is valid only if the control is input-request-enabled.

Test. A result descriptor is returned, indicating that an operation has been completed.

Table 6-7
Console Printer I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Read	32	RRRR	Begin	End
Write	34	RRRR	Begin	End
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

R indicates reserved for future expansion.

RESULT DESCRIPTOR

The result descriptor exception bits for the console printer are:

a. Bit 3 – console printer Not Ready.

b. Bit 4 – memory parity error (write).

c. Bits 5 and 6 – reserved.

d. Bit 7 – error (NAK key).

e. Bit 8 – attempted to exceed maximum address (read only).

f. Bits 9-12 – reserved.

g. Bits 13-16 – unit number.

Reader Sorter Control (B 2130/B 3130)

The reader sorter control is used to execute I/O operations on reader sorters. One result descriptor is returned for each I/O Initiate operation. In demand mode this occurs after the completion of each Read descriptor and after each Pocket Select descriptor. In flow mode this occurs immediately after the completion of the first Read operation and thereafter after the receipt of each Pocket Select descriptor, but not before the completion of a valid Read operation.

If a memory access is not granted, bit 4 and, if appropriate, bits 10 and/or 11 are set ON in the result descriptor. If an unencoded document is encountered, the control stores blanks and sets bits 4, 7, and, if appropriate, bits 10 and 11 ON. If a cannot-read signal is received by the control, bits 4, 7, and, if appropriate, bits 10 and/or 11 are set ON in the result descriptor. A batch ticket will cause a Stop Flow condition and bits 5 and 7 are set ON in the result descriptor on the completion of the reading of a batch ticket. The item must then be pocket selected.

For underspaced and overlength documents, the fault item(s) is rejected without reading, and flow continues. The result descriptor indication is given for the rejected item(s).

Bits 3 and 5 are set ON in the result descriptor when:

a. The reader sorter is Not Ready.

b. There is an empty hopper.

c. A jam or mis-sort occurs.

d. One of the pockets is full.

e. The sorter STOP button has been pressed.

The result descriptor for conditions b, d, or e is returned after all items in motion are processed.

When a jam occurs, the sorter stops the feeder, and the control causes all documents in the feed line which have not been read to be sent to the reject pocket. The result descriptor is returned after the last item has been rejected.

If a jam occurs in area 2 or a mis-sort occurs, the reader sorter control sets bits 3 and 5 ON in the result descriptor. If an Input Request Enable descriptor is then received, bit 7 in the result descriptor is set ON, provided no interjected Read descriptors have been received. The Master Control Program normally issues the Input Request Enable descriptor after a Not Ready condition. When bit 7 is returned, the MCP will return the program to the EOF label (jam label).

The Not Ready condition can be cleared by making the sorter Ready and then pressing the sorter START button.

The reader sorter control translates the 4-bit MICR code received from the sorter into EBCDIC code as shown in table 6-8. (The BCL/EBCDIC translator is not used.)

Table 6-8
Translation of 4-Bit MICR Code into EBCDIC Code

Sorter Symbol	Sorter Code	Internal EBCDIC Code	Internal Graphic Code	Lister Graphic
0	0000	1111 0000	0 (F0)	0
1	0001	1111 0001	1 (F1)	1
2	0010	1111 0010	2 (F2)	2
3	0011	1111 0011	3 (F3)	3

Table 6-8 (cont)
Translation of 4-Bit MICR Code into EBCDIC Code

Sorter Symbol	Sorter Code	Internal EBCDIC Code	Internal Graphic Code	Lister Graphic
4	0100	1111 0100	4 (F4)	4
5	0101	1111 0101	5 (F5)	5
6	0110	1111 0110	6 (F6)	6
7	0111	1111 0111	7 (F7)	7
8	1000	1111 1000	8 (F8)	8
9	1001	1111 1001	9 (F9)	9
Amount	1010	0111 1011	# (7B)	.
Transit	1011	0111 1100	@ (7C)	X
On-Us	1100	0111 1010	: (7A)	,
Hyphen	1101	0110 0000	- (60)	-
Cannot read	1111	0101 1100	* (5C)	*
S5	1110	0111 1101	Apostrophe (7D)	*
		0100 0000	Blank (40)	Blank

The reader sorter control can store one character per memory access. The time between memory accesses is approximately 420 microseconds for an MICR Read. One hundred memory accesses are required per item per read head.

The control employs either alternating or non-alternating buffer operation as determined by the variants in the Read descriptor.

A Pocket Select descriptor for an item must be received before another item is allowed to be read into the same memory area or the first item reaches the pocket area, whichever occurs first. The control stops the feeder if the descriptor is not received in time. If a Pocket Select descriptor is received in time for pocket selection but too late to allow reading into the same buffer area, the item is correctly pocketed and bits 4, 5, and 6 are set ON in the result descriptor after all remaining items following the first item are rejected.

If a Pocket Select descriptor is received after the first item reaches the pocket area, the first item and all remaining items are rejected. Bit 6 in the result descriptor is immediately set ON; if flow has stopped, bit 5 is also set ON. If flow has not stopped, an additional Pocket Select descriptor must be received by the control and is held until flow stops; bit 5 is then reported.

READER SORTER I/O DESCRIPTORS

The reader sorter I/O descriptors are shown in table 6-9.

The symbols for digits 3-6 represent the following:

a. R – reserved for future expansion.

b. V – variant of the Op Code.

c. N – number of pocket to be selected or pocket light to be lit.

d. C – formatting and validity checking.

Flow Read and Demand Read (Non-Alternating Buffer). Data are read into descending memory locations starting with the location specified by the B address minus two and the A address minus two. The A address defines the storage area for the data from the second read station and the B address defines the storage area for the data from the first read station. Blanks (0100 0000) are stored following the last data character read until a total of 100 characters is stored in both areas.

The variants for the Demand Read descriptor are:

a. V – 0 (read first station only).

b. V – 2 (read second station only).

c. V – 4 (read both stations).

The variants for the Flow Read descriptor are:

a. V – 0 (read first station only).

b. V – 2 (read second station only).

Table 6-9
Reader Sorter I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Flow Read	62	RVRC	A address	B address
Demand Read	63	RVRC	A address	B address
Pocket Select	60	NNRV		
Batch Count	66	RRRR		
Pocket Light	64	NNRR		
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

The Flow Read descriptor establishes flow mode. The appropriate A or B address given in the descriptor is reestablished by the control for each item to be read. Only the Pocket Select descriptor is valid when in flow mode.

The Demand Read descriptor establishes demand mode. One item per descriptor is read.

Variants for validity checking and formatting of MICR read information for the first read station are as follows:

a. C – 0 (end reading at 7¾ inches or at the end of the document, whichever comes first, do not format the information, and report all read errors).

b. C – 1 (same as a; except do not report cannot-read errors after the second S2).

c. C – 2 (same as a; except end reading and data transfer after the second S2 symbol).

d. C – 4 (same as a; except format the information and report any errors in the amount field and the A.B.A transit field uniquely).

e. C – 5 (same as d; except do not report cannot-read errors after the second S2 symbol).

f. C – 6 (same as d; except end reading and data transfer after the second S2 symbol).

Formatting is accomplished by storing data continuously into descending memory locations until the first S2 symbol is received. Blanks are then stored until the fortieth character location is reached at which point the S2 symbol and the remaining data are stored. Blanks are stored following the last information character read until a total of 100 characters is stored.

Validity checking of the amount field includes checking:

a. The first and twelfth characters stored for amount symbols.

b. The intervening ten characters for decimal digits.

Validity checking of the transit field includes checking:

a. The fortieth and fiftieth characters stored for transit symbols.

b. The intervening nine characters for four decimal digits followed by a hyphen followed by four digits. (Canadian checks are reported as a transit error.)

Flow Read (Alternating Buffer). Data from the odd items (first, third, etc.) are read from the first read station into descending memory locations starting with the location specified by the B address minus two, and from the second read station into descending memory locations starting with the location specified by the A address minus two. Blanks (0100 0000) are stored following the last information character read until a total of 100 characters is stored in each area.

The above two Read operations are repeated to read information from the even items (second, fourth, etc.) starting with memory locations B-address-minus-202 and A-address-minus-202, respectively.

Variants for the type of Read operation are as follows:

a. V – 1 (read first station only).

b. V – 3 (read second station only).

c. V – 5 (read both stations).

Variants for validity checking and formatting of MICR Read information are the same as for the Flow Read and Demand Read (non-alternating buffer) descriptors.

Pocket Select. The last item read is pocket selected. The Read operation(s) are continued if the sorter is in flow mode. Pocket selection is determined by digits 3 and 4 (NN) of the Pocket Select descriptor. The V variant has the following meaning:

a. V – 0 (continue flow).

b. V – 1 (stop flow).

Batch Count. The batch counter in the sorter is advanced by one. Flow must be stopped and all items must be pocket selected.

Pocket Light. The pocket light specified by digits 3 and 4 is lighted. Flow must be stopped and all items must be pocket selected. This descriptor sets the control to a Not Ready condition which must be cleared by pressing the START button on the sorter.

Input Request Enable. An input request is recognized by setting bit 1 ON in the result descriptor, or a jam/mis-sort condition is recognized by setting bits 1, 2, and 7 ON in the result descriptor.

Input Request Disable. This descriptor removes the Input Request Enable descriptor and any request or jam/mis-sort condition is ignored. A result descriptor is immediately returned.

Test. The sorter is tested and a result descriptor is immediately returned to indicate whether the sorter is Ready or Not Ready.

RESULT DESCRIPTOR

The result descriptor exception bits for sorter-reader operations are as follows:

a. Bit 3 – Not Ready.

b. Bit 4 – Memory Access error.

c. Bit 5 – Flow stopped.

d. Bit 6 – too late to Pocket Select.

e. Bit 7 – Jam in area 2 or Mis-sort condition.

f. Bits 3 and 5 – a Stop has occurred because of a Jam, or a sorter is Not Ready.

g. Bits 4 and 7 – cannot Read or an Unencoded Document.

h. Bits 4 and 8 – Double Document.

i. Bits 4 and 10 – Amount Field error (if the C variant is 4, 5, or 6). Amount and/or Transit Field errors are reported in addition to other Read errors.

j. Bits 4 and 11 – Transit Field error (if the C variant is 4, 5, or 6). Amount and/or Transit Field errors are reported in addition to other Read errors.

k. Bits 5 and 6 – too late to Pocket Select and Flow has stopped.

l. Bits 5 and 7 – Batch Ticket (new sorter on Read; old sorter on Pocket Select).

m. Bits 4, 5, and 6 – too late to Read (new sorter).

n. Bits 4, 5, and 7 – Batch Ticket error (cannot Read, Unencoded, or Memory Access error – new sorter on Read; old sorter on Pocket Select).

o. Bits 4, 7, and 8 – cannot Read and Double Document (old sorter).

p. Bits 5, 6, and 7 – too late to Pocket Select Batch Ticket (new sorter on Read; old sorter on Pocket Select).

q. Bits 4, 5, 6, and 7 – too late to Read Batch Ticket (new sorter on Read; old sorter on Pocket Select).

r. Bit 12 – buffer number (0 or 1 – exception bit is not set ON).

s. Bits 13-16 – unit number (0).

Table 6-10
Lister I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Lister Print	70	UTUT	Begin	End
Lister Space	71	UTUT		
Lister Skip	72	UTUT		
Lister Slew	73	UVUT		
Input Request Enable	35	RRRR		
Input Request Disable	97	RRRR		
Test	99	RRRR		

Lister Control (B 2244/B 3244)

This control is used to execute I/O operations on the multiple tape listers. The control enables the EBCDIC/BCL translator in central control to translate data while transferring it from core memory to the control. During any operation when the paper is near the end, the operation takes place and the end-of-paper bit is set ON in the result descriptor.

The control contains a one-character buffer and data is transferred to the lister buffer serially by character. The control is capable of loading the lister buffer while paper motion is occurring in response to a previous Space or Print descriptor. The result descriptor for Skip and for Slew is reported after paper motion has finished.

The print-check-error bits refer to the line associated with the previous descriptor; the current descriptor is executed. The memory-parity-error bits refer to the line associated with the current descriptor; the current descriptor is executed.

LISTER I/O DESCRIPTORS

The lister I/O descriptors are shown in table 6-10.

The symbols for digits 3-6 represent the following:

a. V – variant.

b. U – unit number.

c. T – tape number.

d. R – reserved for future expansion.

NOTE

A lister descriptor with an invalid (unspecified) unit number or invalid tape numbers can cause the control to appear to be constantly busy. Pressing the STOP button on the lister control panel causes the lister Not Ready condition and releases the lister to the I/O control channel.

Lister Print. Data is printed from ascending memory locations beginning at the location specified by the A address continuing to, but not from, the ending location specified by the B address. The A and B addresses must define a 44-character buffer.

For the master/slave/slave combinations, the first 22 characters are printed on both the master tape of unit 1 and the tape designated by digits D3 and D4. If D3 is zero, then printing on both the master tape on unit 1 and the tapes D3 and D4, is suppressed. Printing on the master tape can be suppressed while the tape specified by D3 and D4 prints by manual selection of the printers (Manual Selector Switch in N position). When D4 is set to zero, the master tape prints, but no second tape prints from buffer positions 1-22. Thus, printing can be suppressed on any one or two tapes.

For the 6-tape/6-tape combination, D4 must be zero and the first 22 characters are printed on the master tape of the unit designated by D3. If D3 is zero, then printing of the master tape is suppressed.

The second 22 characters are printed on the tape designated by digits D5 and D6. Single spacing always occurs after printing.

The coding for U and T in digits D3 through D6 is as follows:

a. U – 1-3 (unit number).

b. U – 0 (suppress print).

c. T – 1-6 (tape number).

NOTE

The printing of the tape designated by digits D3 and D4 is possible only with the B 9249-1 Tape Lister.

Lister Space and Lister Skip. A skip of 2½ inches occurs or the lister tapes are spaced as designated. For the master/slave/slave combination, a Skip/Space operation is performed on both the master tape of unit 1 and the tape designated by digits D3 and D4. If D3 is zero, skipping/spacing on both the master tape on unit 1 and the tape designated by D4 is suppressed. For the 6-tape/6-tape combination, D4 must be zero and skipping/spacing of the master tape on the unit designated by D3 is performed. If D3 is zero, then skipping/spacing of the master tape is suppressed. An additional tape may be skipped/spaced as designated by D5 and D6.

The coding for U and T in digits D3 through D6 is as follows:

a. U – 1-3 (unit number).

b. U – 0 (suppress skip or space).

c. T – 1-6 (tape numbers).

Lister Slew. Lister tapes are slewed 10 inches as designated by digits D3 through D6. The coding for U and V in digits D3 and D4 is as follows:

a. V – 0 (allow slew of master tape).

b. V – 1 (inhibit slew of master tape).

c. U – 1 (slew all tapes on unit 1).

d. U – 2 (slew all tapes on unit 2).

e. U – 3 (slew all tapes on units 1 and 2).

f. U – 5 (slew all tapes on units 1 and 3).

g. U – 6 (slew all tapes on units 2 and 3).

h. U – 7 (slew all tapes on units 1, 2, and 3).

NOTE

For the 6-tape/6-tape combination, only D3 equal to 3 can be designated.

The coding for T and U in digits D5 and D6 to suppress slew of designated tapes is as follows:

a. U – 0 (do not suppress slew).

b. U – 1-3 (unit number).

c. T – 1-6 (tape number).

NOTE

Digits D5 and D6 are used only on the 18-tape lister and must otherwise be zero.

If the use of unspecified variants in lister commands causes a continuous Busy condition, depression of the lister STOP control (which causes a lister Not-Ready condition) releases the lister to a I/O unit channel.

Input Request Enable. When the control is input-request-enabled, the control returns a result descriptor, indicating that an operation is completed if and when the lister is ready.

Input Request Disable. The control is made insensitive to any condition the lister can present.

Test. A result descriptor is returned, indicating a completed operation, a Not Ready condition, or an end-of-paper condition, as appropriate.

RESULT DESCRIPTOR

The result descriptor exception bits for the multiple tape lister are:

a. Bit 3 – lister Not Ready.

b. Bits 4 and 6 – memory parity error.

c. Bits 4 and 7 – print check.

d. Bit 5 – end of paper.

e. Bits 8-12 – reserved.

f. Bits 13-16 – unit number (0).

Disk File Controls and Exchanges (B 2371, 3 & 5/B 3371, 3 & 5)

A disk file control unit is used to execute disk file and system memory I/O operations. Up to four disk file control units and up to ten disk file electronics units or system memory units may be used with the B 2500/B 3500 Systems. An exchange is required if more than one control is used.

A disk file control unit can store or fetch two 8-bit characters (one word) per memory access. The number of memory cycles required is one-half times the number of characters per record plus one.

When information is read onto any disk file, a longitudinal parity character is generated automatically by the control unit for each segment. During a Read or a Check operation, a comparison is made against the parity character to determine whether an error occurred during the Read or Check. If an error has occurred, the read-error bit of the result descriptor is set ON and the operation is terminated at the end of the segment in error. When a memory access is missed during a Read, Check, or a Write operation, accesses to memory are terminated immediately and a result descriptor is stored when the unfinished segment is completed.

If a memory parity error is detected during a Write operation, accesses from memory are terminated immediately, the segment is completed with null characters, and a result descriptor is stored. If the maximum address of a unit is executed or if a missing storage unit is addressed during an initial Read, Check, or Write operation, operations are not performed and bit 3 of the result descriptor is set ON.

The control contains an adjustable timer which causes time-out if the addressed unit does not send the correct segment address for at least one disk revolution; a result descriptor is stored with bit 12 set ON.

There are presently three disk file controls available on the B 2500/B 3500 Systems; disk file control B 2373 or B 3373, systems memory control B 2371 or B 3371, and combination control B 2375 or B 3375. The combination control provides for both disk and systems memory. The B 2373 or B 3373 disk file control is used with the B 9371 modular random storage device and B 9375 data memory bank. The B 2371 or B 3371 systems memory control is used with the B 9370 systems memory unit. The characteristics for the disk file control are contained in the paragraphs that follow.

DISK FILE AND SYSTEMS MEMORY CONTROL

Reading and writing may be continuous across consecutive modules, but not across electronics units or system memory units. Changing modules can result in a time loss equivalent to one disk revolution.

The system memory or electronics unit is given in digit D3 of the I/O descriptor and the module number is included in the file address.

When a busy electronics unit or system memory is addressed by disk file control, the control does not wait but sets bit 5 ON in the result descriptor.

Disk file control does not request memory accesses more often than every other memory cycle; it includes three characters of buffering for reading, and none for writing. When writing at the highest transfer rate, disk file control must receive an access after a maximum of two intervening memory cycles for system memory and three intervening memory cycles for a disk file module.

DISK FILE/SYSTEMS MEMORY CONTROL I/O DESCRIPTORS

I/O descriptors used with all disk file and systems memory control units are shown in table 6-11.

Table 6-11
Disk File/System Memory Control I/O Descriptors

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18	Digits 24-30
Disk File Write	50	UFVV	Begin	End	File address
Disk File Read	51	UFVV	Begin	End	File address
Disk File Check	52	UFVV	Begin	End	File address
Test	99	URRR			

The symbols for digits 3-6 represent the following:

a. U – unit number.

b. F – density.

c. V – variant of the Op Code.

d. R – reserved for future expansion.

Disk File Write. Data are written onto the disk file from ascending memory locations beginning with the location specified by the A address and continuing to, but not from the ending location specified by the B address. When the V variant is 8, this indicates a maintenance segment write.

NOTE

Null characters are written to complete each segment.

Disk File Read. Data are read from the disk file into ascending memory locations beginning with the location specified by the A address and continuing to, but not into the terminal location specified by the B address. The result descriptor read-error bit is set ON in the event of a read error.

Disk File Check. A Check operation is the same as a Read operation with one exception. It does not store or change any data in memory.

Test. The status of the designated unit is tested and a result descriptor is returned.

DISK FILE/SYSTEMS MEMORY CONTROL RESULT DESCRIPTOR

The result descriptor exception bits for disk file and systems memory control are:

a. Bit 3 – disk file Not Ready.

b. Bit 4 – memory access error.

c. Bits 4 and 6 – memory parity error (write) or read error (read and check).

d. Bit 5 – electronics unit busy.

e. Bit 6 – write lockout (write).

f. Bits 7-11 – reserved.

g. Bit 12 – time out.

h. Bits 13-16 – unit number.

DISK FILE EXCHANGE 1 x 2 (B 2473/B 3473)

This exchange provides the capability of addressing up to two system memory units or disk file electronics units using one control. The exchange is a plug-in part of the disk file control.

DISK FILE EXCHANGE 2 x 10 (B 2474/B 3474)

This modular exchange provides the capability of interfacing up to ten system memory units or disk file electronics units to either one or two disk file control units. One disk file exchange 2 x 10 adapter is required for each attached peripheral unit (disk file electronics unit or system memory).

DISK FILE EXCHANGE 4 x 10

This exchange provides the capability of interfacing up to ten system memory units or disk file electronics units to any one of four controls. Priority is first come, first served. Asynchronous requests from the controls are permitted and are serviced at least every ten microseconds.

DISK FILE EXCHANGE 4 x 20 EXTENSION

This modular exchange extension provides the capability of interfacing an additional 10 system memory or disk file exchange units to any one of four controls connected to the 4 x 20 exchange.

The use of disk file exchange n x 2 and 2 x 2 adapters are required in the extension as well as in the exchange. The modularity of the adapters in the extension is the same as stated for the exchange.

SECTION 7
PERIPHERAL UNITS

GENERAL

The peripheral units are those units that provide the input and output facilities for B 2500 or B 3500 Systems. They operate independently of the processor, but always under control of the Master Control Program through the I/O control unit. This section describes the peripheral units that may be used on the B 2500 and B 3500 Systems.

CARD READERS

All card readers are capable of reading binary, BCL, or EBCDIC card codes. The EBCDIC code is considered as the standard mode and data recorded in other modes are passed through an appropriate automatic translator. Refer to the B 2500 and B 3500 Master Control Programs Information Manual (1031218) for information pertaining to the input of card data.

B 9110 Card Reader

The B 9110 Card Reader (figure 7-1) is designed for use as a compact, general purpose card reader capable of reading 80-column punched cards at a maximum rate of 200 cards per minute (CPM) under control of the I/O control unit. Buffered operation, through the I/O control unit, permits computations to proceed while the card data is being read. The card reader can handle cards that are notched during verification.

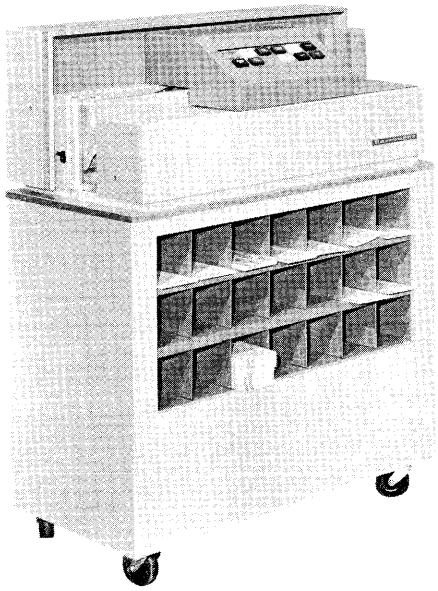


Figure 7-1. B 9110 Card Reader

FUNCTIONAL CHARACTERISTICS

A single path mechanism transports cards from the picking mechanism, through the read station, and into the stacker. A failure to feed, or feed jams, causes a Not Ready signal to be relayed to the associated I/O control unit. A jam will halt the card read operation with no more than two cards in a jammed condition. Information punched in the card is read and transferred into the one-word input buffer, parallel by bit, serially by column. By use of the switch on the control panel, the validity of each character in the card can be checked. For proper MCP operation, the VALIDITY switch must be turned on. A demand-type card picking mechanism permits the complete reading of an 80 column card in a total time of 350 ms or less after a start feed signal is received. The card hopper has a capacity of 450 cards. Cards may be placed into the hopper while the unit is operating as long as approximately 150 cards are still in the hopper. During loading, the cards already in the hopper remain in proper position for the continuous feeding without manual support from the operator. A single, one-column data reading station reads the cards column-by-column serially for the entire 80 columns. The card data may be in tabulating card code or binary code and is transferred to the input buffer of the associated I/O control unit in 6-bit code. The cards are stacked in the stacker in the same sequence as they are fed and cannot be removed from the stacker while the unit is operating.

CONTROL PANEL

A B 9110 Card Reader control panel (figure 7-2) contains the switches and indicators for operation of the unit and indicates error conditions. The function of each of these elements is provided in table 7-1.

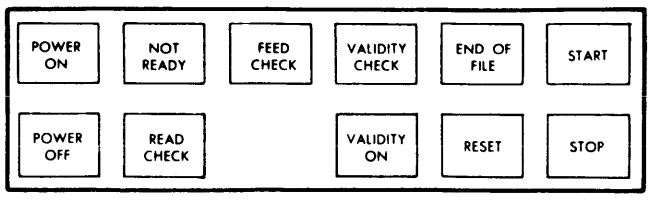


Figure 7-2. B 9110 Card Reader Control Panel

Table 7-1
B 9110 Card Reader Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This is a combination switch-indicator that applies power to the card reader and lights when pressed.
NOT READY	This indicator lights when any of the following conditions exist: card jam, stacker full, cover not in place, empty hopper, or STOP switch pressed. The condition causing the NOT READY indicator to light must be corrected before reading can be resumed.
FEED CHECK	This indicator lights as a result of a card jam or a failure to feed or stack a card properly.
VALIDITY CHECK	This indicator lights when an invalid character is read by the card reader, and the MCP is notified of this by flagging the I/O result descriptor. The VALIDITY CHECK indicator and its associated circuitry are only operative when the VALIDITY ON switch-indicator is lit.
END OF FILE	This switch-indicator is not used for B 2500 or B 3500 operations. An end-of-file is accomplished with control cards.
START	This switch will ready the card reader (turn the NOT READY indicator off) to allow the card reader to read cards under control of the B 2500 or B 3500.
STOP	This switch is used to stop the card reader from feeding cards. When the switch is pressed, the card reader will go Not Ready.
RESET	This switch clears all error indicators on the card reader. However, the NOT READY indicator is not turned off by pressing this switch.
VALIDITY ON	This switch-indicator provides the means of performing a validity check by the card reader. Validity checking is performed when the switch is pressed and the indicator lights. Validity checking is disabled when the switch is pressed and the indicator goes out.
READ CHECK	This indicator lights when the read check circuitry detects an operational failure.
POWER OFF	This switch removes power from the unit.

B 9111 Card Reader

The B 9111 Card Reader (figure 7-3) is used to process punched cards of 51, 60, 66, or 80 columns of either standard or post card thickness, under control of an I/O control unit, at the rate of 800 CPM. An immediate-access clutch provides demand feeding. Read data is transferred to the one-word buffer of the I/O control unit and then to memory. Cards cut on any corner and cards that have been verified (notched on the right edge) may be used. However, the card stock thickness and the length must be consistent during any one run.

FUNCTIONAL CHARACTERISTICS

A single, one-column reading station reads the cards column by column. Column 1 is read first. A demand-type card picking mechanism picks the cards from the card hopper; and, if an initial pick

Figure 7-3. B 9111 Card Reader

fails, a second pick would be attempted automatically. The card hopper has a capacity of 2400 cards and can be loaded by the operator while the unit is operating. The operator does not have to hold the cards already in the hopper in position while loading additional cards. Cards are conveyed from the hopper to the card stacker by means of a card transport mechanism. The cards are then stacked into the card stacker in the same sequence and manner in which they were fed. The stacker will also hold a maximum of 2400 cards. Cards may be removed from the stacker during operation. Failure to feed a card will cause a missing card condition, and the card reader will be placed in a Not Ready state. A card jam will not cause mechanical damage, but the unit will stop operating when two cards are jammed.

CONTROL PANEL

The B 9111 Card Reader contains a control panel (figure 7-4) for communication with the I/O control unit and to indicate error conditions. The function of each switch and indicator on the control panel is given in table 7-2.

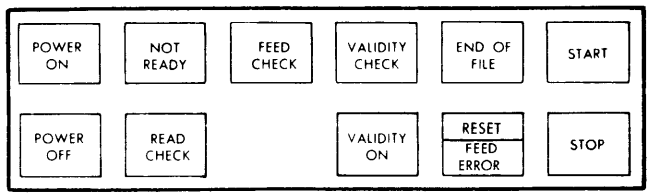


Figure 7-4. B 9111 Card Reader Control Panel

Table 7-2
B 9111 Card Reader Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This is a combination switch-indicator that applies power to the card reader and lights when pressed.
NOT READY	This indicator lights when any one of the following conditions exists: card jam, stacker full, cardline mechanism not locked, empty hopper, or STOP switch pressed. The condition causing the NOT READY indicator to light must be corrected before reading can be resumed.
FEED CHECK	This indicator will light as a result of a card jam or a failure to feed or stack a card properly.
VALIDITY CHECK	This indicator lights when an invalid character is read by the card reader. The MCP is notified of this condition by flagging the I/O result descriptor. The VALIDITY CHECK indicator and its associated circuitry are only operative when the VALIDITY ON switch-indicator is lit.
END OF FILE	This switch-indicator is not used for B 2500 or B 3500 operations. An end-of-file is accomplished with control cards.
START	This switch will ready the card reader (turn the NOT READY indicator off) to allow the card reader to read cards under control of the B 2500 or B 3500.

Table 7-2 (cont)
B 9111 Card Reader Control Panel Switches and Indicators

Switch/Indicator	Function
STOP	This switch is used to stop the card reader from feeding cards. When the switch is pressed, the card reader will go Not Ready.
RESET/FEED ERROR	The RESET switch clears all error indicators on the card reader. However, the NOT READY indicator is not turned off by pressing this switch. The FEED ERROR indicator lights when a double document is detected.
VALIDITY ON	This switch-indicator provides the means of performing a validity check by the card reader. Validity checking is performed when the switch is pressed and the indicator lights. Validity checking is disabled when the switch is pressed and the indicator goes out.
READ CHECK	This indicator lights when the read check circuitry detects an operational failure.
POWER OFF	This switch removes power from the unit.

On those card readers with a B 9919 Treasury Check Option, there is an additional switch-indicator located on the control panel. This switch (labeled 1-40) provides the ability to read only columns 1 through 40 and ignore any punched to the right of column 40. It can be used with 50-, 60-, and 80-column cards. Successive depressions of the switch cause the 1-40 column read mode to alternate with the normal 1-80 column read mode. The indicator is lit during the 1-40 mode. Validity checking can be performed when in the 1-40 mode, but only on the first 40 columns.

On card readers equipped with a B 9918 Postal Money Order option, there is an additional switch-indicator located on the control panel. This switch-indicator is labeled POSTAL M.O. and provides the ability to read the round holes in money orders. Successive depressions of the switch cause the money order mode to alternate with the normal 1-80 column read mode. The indicator is lit during the money order mode. Validity checking is performed in either mode.

B 9112 Card Reader

This high speed input unit provides buffered reading of 1400 cards per minute. Appearance and physical characteristics are the same as the B 9111. An empty hopper condition causes the transport to shut off. When cards are placed in the empty hopper, the transport restarts without additional operator action.

B 9120 PAPER TAPE READER

The B 9120 Paper Tape Reader (figure 7-5) is capable of reading punched paper tape at speeds of 1000 or 500 characters per second (CPS). If metalized Mylar or fanfold tape is to be read, the speed must be 500 CPS. The B 9120 can accommodate 5-, 6-, 7-, or 8-channel tape, as selected by the operator. Optional code translation facilities are available if required. Tape guides provide positive detent action to handle 11/16-, 7/8-, and 1-inch tape interchangeably. Beginning and end of tape are sensed via adhesive opaque strips. Tape reels can be either 5.5 or 7 inches in diameter. The paper tape reader is buffered through the I/O control unit. The B 9120 is also capable of checking tape for parity errors as an off-line operation. In the off-line mode, the B 9120 will stop upon detection of a parity error.

Functional Characteristics

Start time for the paper tape reader is 5 ms or less. Start time (when using 10-character-per-inch tape) is defined as the duration from the moment a start signal is received until the next character is read. Stop time for the B 9120 is one ms or less (non-oiled tape). The paper tape reader requires a 20 ms stop stabilization time prior to executing another instruction. When reading paper tape or Mylar tape punched 10 characters per inch at speeds up to 1000 CPS, the B 9120 will stop in position to read the next character. A minimum of four feet of tape leader is required with reeling. For strip reading, a

one-foot tape leader is required. If a broken tape condition occurs, the tape reel motors are shut off automatically. Rewind can be initiated by the B 2500 or B 3500.

Channel Select Plugboard

A channel select plugboard is provided for interchanging channels. This action changes the bit configuration from paper tape to an interchanged bit configuration in memory. Paper tape with even parity can be accommodated by inverting the desired channel. All unused channels must be connected to the corresponding C channel. Figure 7-6 illustrates the channel select plugboard BCL and teletype wiring configuration.

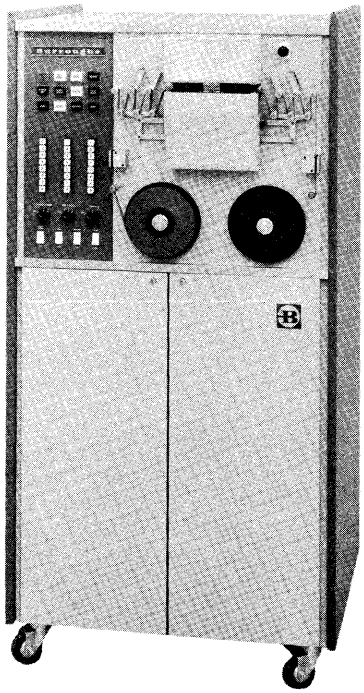


Figure 7-5. B 9120 Paper Tape Reader

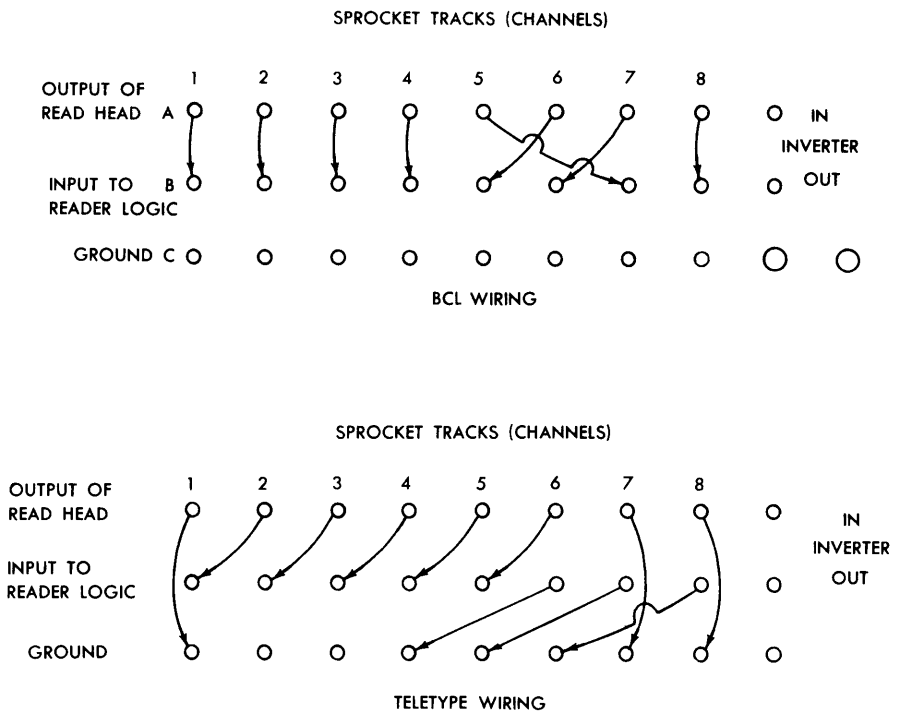


Figure 7-6. B 9120 Channel Select Plugboard

B 9926 Code Translator

The B 9926 Input Code Translator, which is an optional feature, permits translation of 5-, 6-, 7-, or 8-level codes. Up to 64 information levels can be translated by the code translator which is located in the paper tape reader cabinet. The following describes the plugboard layout (figure 7-7).

a. Exits: The exit hubs represent data as received from the paper tape channel select plugboard and consists of 256 possible con-

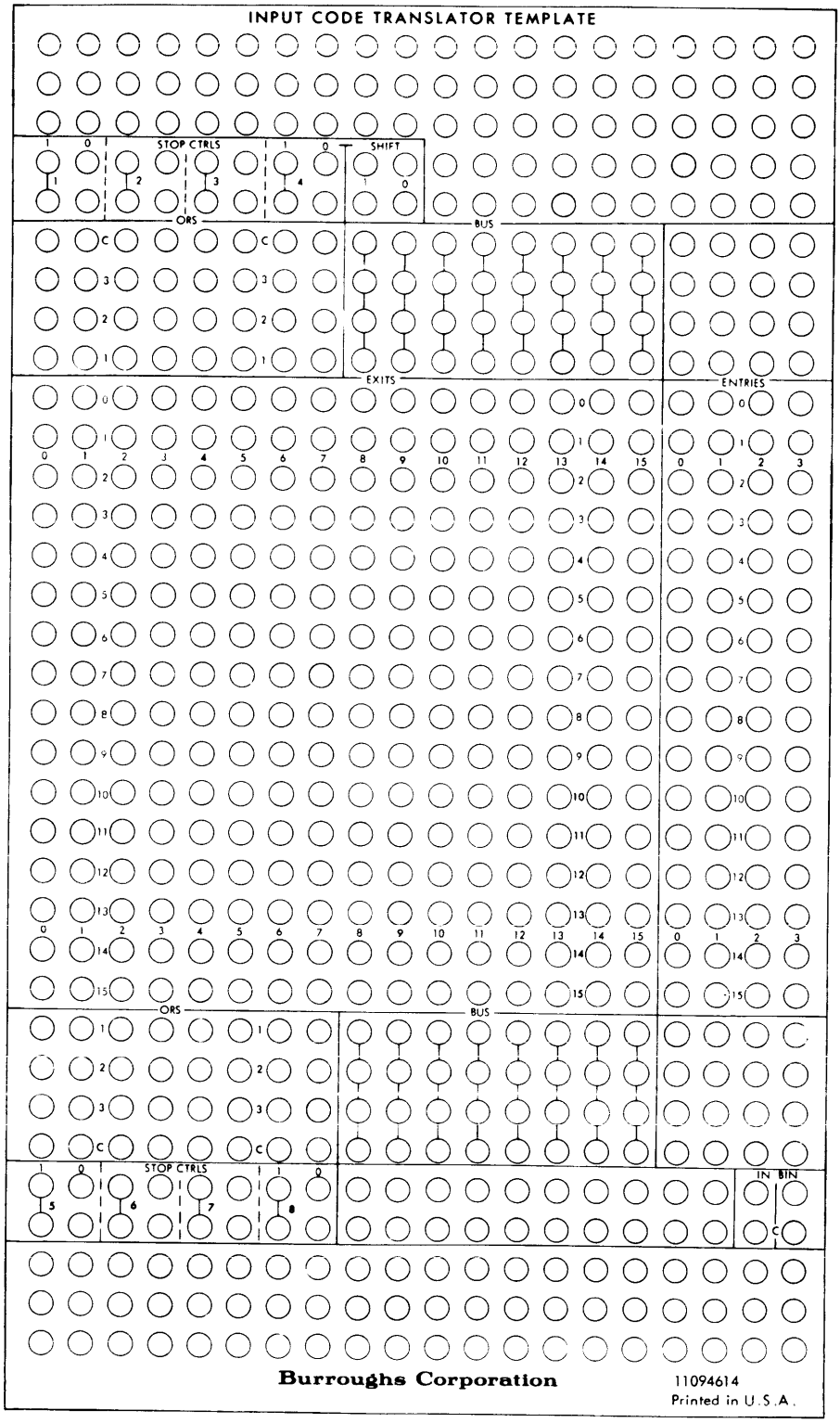


Figure 7-7. B 9926 Plugboard Layout

figurations that can be generated by 8-level code. Column numbers are the decimal equivalents of the binary numbers represented by the "input to reader logic" (B) hubs 1 to 4 of the channel select plugboard. For example:

Binary Equivalent	(1)	(2)	(4)	(8)	
Channel B	1	2	3	4	
	0	1	0	1	goes to column 10

Row numbers are the decimal equivalents of the binary numbers represented by the "input to reader logic" (B) hubs 5 to 8 of the channel select plugboard. For example:

Binary Equivalent	(1)	(2)	(4)	(8)	
Channel	5	6	7	8	
B	0	1	1	1	goes to row 14

b. Entries: The entry hubs represent data sent to the I/O control unit consisting of the 64 possible BCL combinations. Column numbers are the decimal equivalents of the binary numbers represented by the B and A bits of the BCL code (BA = 0, 1, 2, and 3). Row numbers are the decimal equivalents of the binary numbers represented by the 8, 4, 2, 1 bits of the BCL code. For example, if row 7 of column 3 is connected, the bit configuration is represented as B A 8 4 2 1 or the BCL character G.

c. Stop Controls: There are eight sets of stop control hubs. To designate a stop code, an exit hub is wired to the input of a stop control. Only one exit can be wired directly to a single stop control input. If the stop code is to be stored, the output of a stop control is wired to an entry hub. Any exit code not wired is deleted and is not transferred to the I/O control unit.

d. Shift Codes: The shift code is designated by wiring an exit to the upper shift code input. An un-shift code is designated by wiring an exit hub to the lower shift code input. The shift code is made functional by connecting two shift output hubs together. When in the shift case, channel 8 (channel selector plugboard) is set to 1. When in the up-shift case, channel 8 is set to zero.

NOTE

Teletype code can be converted to a single case code via the teletype switch.

e. BCL/Binary Input: To enable the translator, the two enable hubs must be connected together. If they are not connected, the translator is bypassed and normal BCL paper tape code to BCL code conversion takes place. To obtain an output which is the direct image of the channel select plugboard (six channels only), the binary hubs must be connected together. The I/O control unit will perform a BCL-to-internal code translation on this input.

f. OR Hubs and BUS Hubs: The following three input OR hub and BUS hub usage is permitted:

1) Up to nine exits can be connected to a single entry by using three OR elements and a BUS.

2) Up to nine exits can be connected to a single stop control by using three OR elements and a BUS.

3) Up to six exits can be connected to a single stop control by using two OR elements (no BUS required).

Control Panel

The B 9120 Paper Tape Reader control panel (figure 7-8), contains switches and indicators for operation of the unit and for the detection of errors. The function of each of these elements is contained in table 7-3.

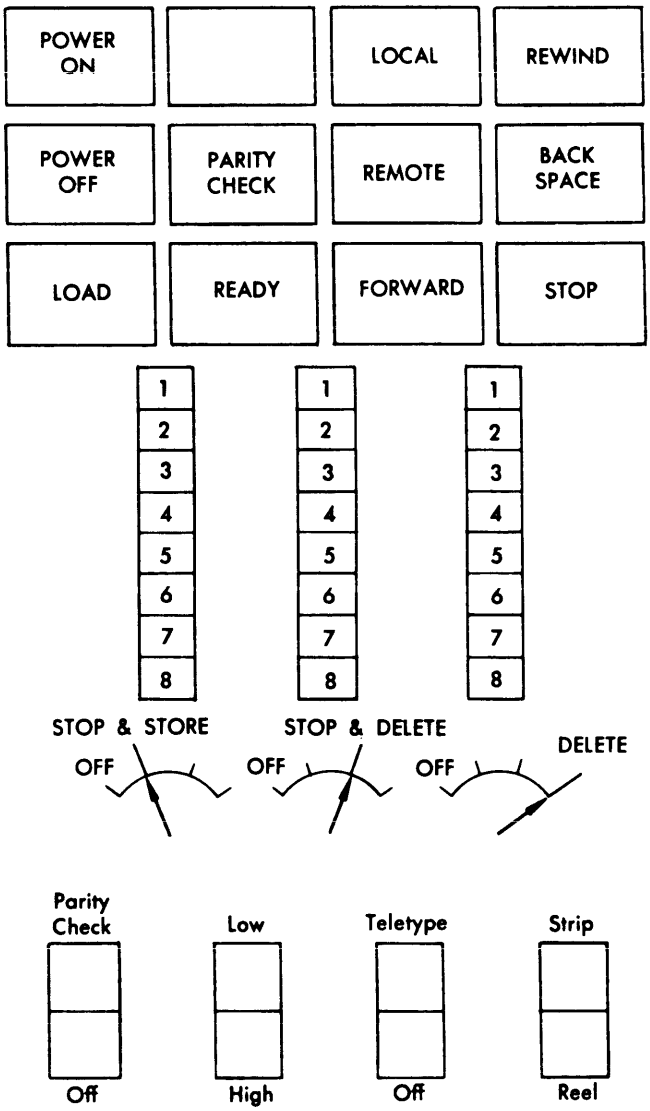


Figure 7-8. B 9120 Paper Tape Reader Control Panel

Table 7-3
B 9120 Paper Tape Reader Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This switch-indicator lights when pressed, indicating that power is applied to the unit.
NOT READY	This indicator lights when a Not Ready condition exists.
LOCAL	This switch places the B 9120 in a local condition, and makes the unit unavailable to the B 2500 or B 3500 System. The LOCAL indicator will also light.
REWIND	When this switch is pressed, the paper tape moves in the reverse direction until a beginning-of-tape condition is detected. The tape will then stop. This switch is active only when the unit is in a Local state and the STRIP/REEL switch is in the REEL position.

Table 7-3 (cont)

B 9120 Paper Tape Reader Control Panel Switches and Indicators

Switch/Indicator	Function
POWER OFF	When pressed, this switch removes power from the unit.
PARITY CHECK	This indicator lights when a parity error is detected. This is activated only when the PARITY switch is ON.
REMOTE	This switch/indicator lights when pressed, indicating that the unit is under control of the B 2500 or B 3500 System.
BACK SPACE	This switch moves the tape in a reverse direction to the immediate previous control code, or beginning-of-tape. This switch is active only when the unit is in a Local condition. The switch may also be used to check parity, off line, while rewinding tape.
LOAD	This switch releases the brakes, allowing loading of the paper tape. This switch is active only when the unit is in the Local condition.
READY	When pressed, this switch sets the brakes and starts the capstan rollers. The servos are also activated when the STRIP/REEL is in the REEL position and the tape is properly positioned in the storage arms.
FORWARD	This switch moves the tape forward to the next control code or to the end-of-tape. This is only active when the paper tape reader is in a local status.
STOP	The operation of the B 9120 will stop when this switch is pressed. This is only active when the paper tape reader is in a Local status.
CONTROL CODE	This is a set of three switches that provides manual selection of three different control codes. Any combination of control codes may be used concurrently. The control code characters may be stored or deleted, as selected. A four-position switch for each code set determines the action taken when the control code is detected. The CONTROL CODE switches are active in either the Local or Remote condition. The four positions of the switch are: OFF, STOP AND STORE, STOP AND DELETE, and DELETE.
PARITY ON-OFF	When this switch is in the ON position, parity checking is enabled. The parity error level is reset when in the OFF position.
HIGH-LOW	In the HIGH position, high-speed operation is selected (1000 CPS); in the LOW position, low-speed operation is selected (500 CPS).
TELETYPE ON-OFF	When in the ON position, five levels of teletype are converted to a 6-level, single-case code.
STRIP-REEL	In the STRIP position, the reel motors are deactivated and the NO TAPE switch is bypassed. In the REEL position, the reel motors are activated and the NO TAPE switch is activated.
NO TAPE	This switch is activated when the STRIP REEL switch is in the REEL position and there is no tape loaded or the tape breaks. Activation of this switch deactivates the reel motors.
GUIDE SELECTION SWITCH	This switch is located to the right of the read mechanism. The switch adjusts the paper guide to the width of the tape being used.

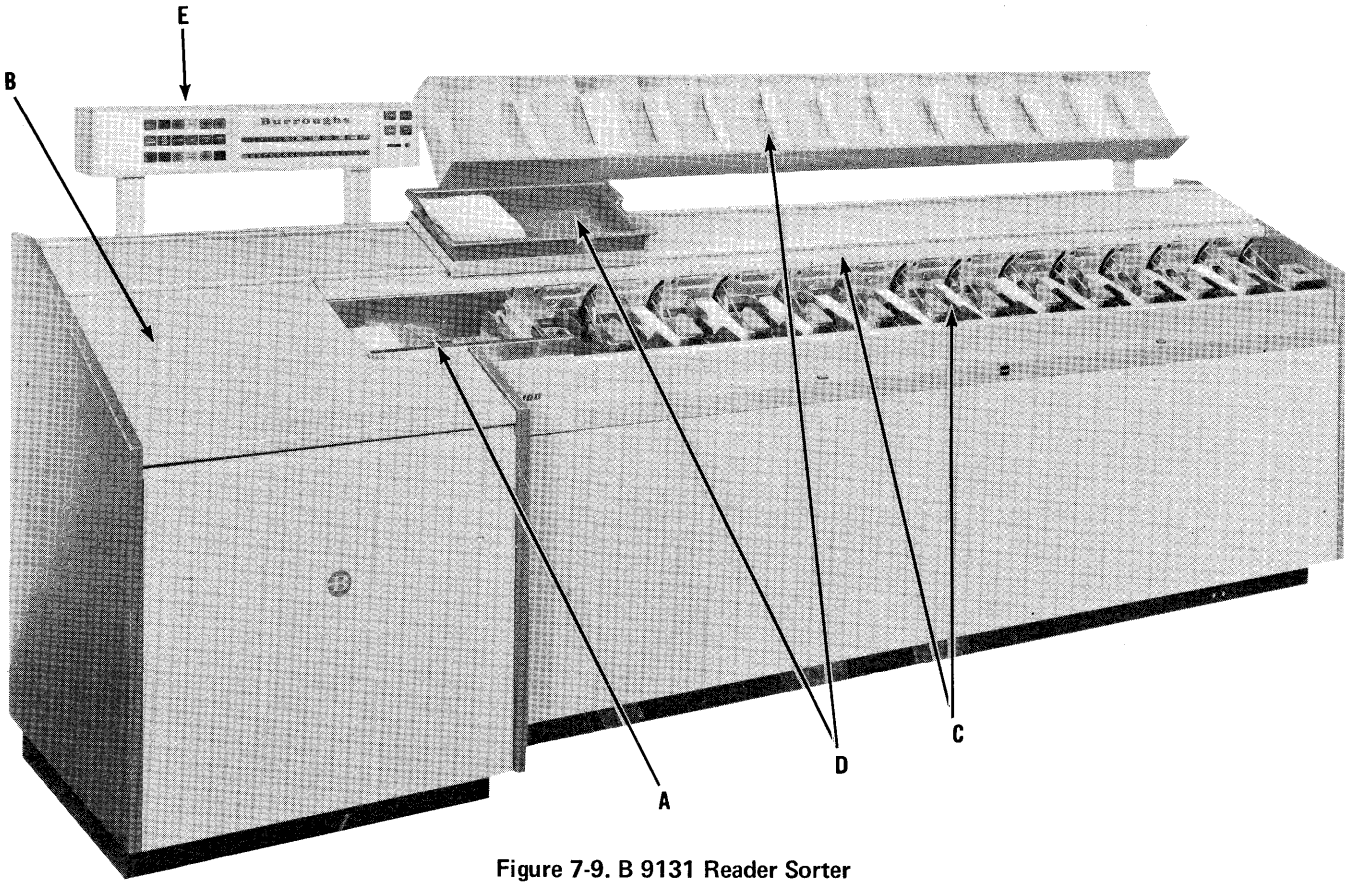


Figure 7-9. B 9131 Reader Sorter

B 9131 AND B 9132 READER SORTER

The reader sorter (figure 7-9) is capable of reading and sorting documents encoded with magnetic ink at speeds up to 1565 items per minute. Information encoded on the documents is converted to Burroughs Common Language (BCL) representation and transferred to core storage in the central processor as EBCDIC. When used with a magnetic tape system, information can be transferred to the central processor for editing and then to magnetic tape. When under program control, the reader sorter can operate in two modes: Demand and Flow. In Demand mode, documents are fed one at a time, as required by the program, at a maximum rate of 400 items per minute. In Flow mode, documents are read and sorted at the free flow rate of the reader sorter, which is up to 1565 items per minute, depending upon document size.

The reader sorter is comprised of five distinct areas (illustrated in figure 7-9 and identified by the letters A through E):

a. Document feeding area (A).

b. Transport and read area (B).

c. Transport and pocket area (C).

d. Temporary storage area and mobile carrier (D).

e. Control panel (E).

Document Feeding Area

This area encompasses the document hopper, the feeder belt, the hold back belt, and the acceleration drum.

The document hopper (figure 7-10) is 15 inches long, 9½ inches wide, and can hold approximately 3000 documents. The documents are placed in the hopper with the front of the document facing to the left. A follow-block provides the necessary pressure to move the documents into the feeder belt and moves smoothly along a guide rail which extends the length of the hopper. The follow-block can be easily tilted out of the hopper when desired.

To load documents while sorting, the new documents are placed to the right of the follow block; the follow block is then raised from its position between the two groups of documents and repositioned directly behind the last document in the hopper.

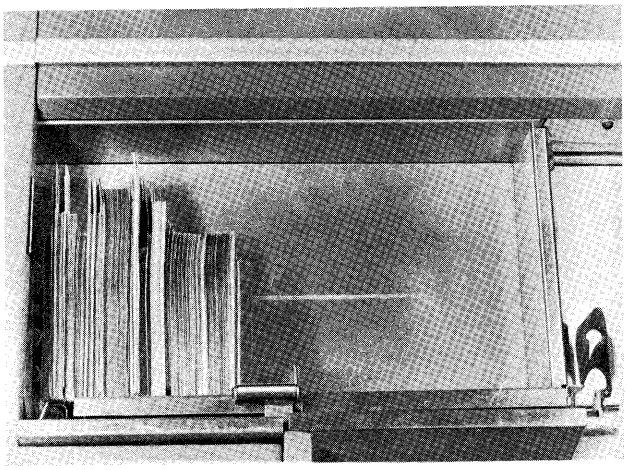


Figure 7-10. B 9131 Document Hopper

The hold back belt, in combination with the feeder belt, restricts feeding to one document at a time. The function of the hold back belt is to separate the documents, thus permitting only one document at a time to be transported to the read station. Figure 7-11 illustrates the two belts in relation to their position in the document feeding mechanism.

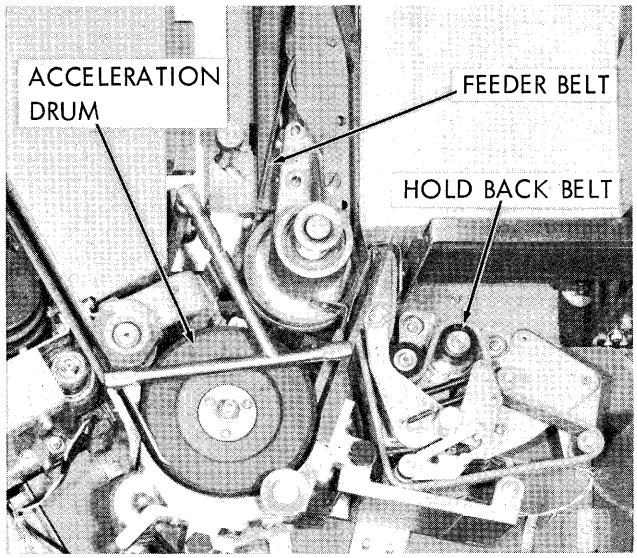


Figure 7-11. B 9131 Document Feeding Area

Documents are selected from the hopper by the feeder belt at the rate of 150 inches per second and accelerated to 400 inches per second by the acceleration drum. Proper spacing between documents is important to ensure the reading and sorting of each document. Improper spacing between documents is detected by strategically located beams of light, which cause such documents to be sorted into a reject pocket. Document feeding is stopped for 300 milliseconds to permit the reject and then automatically continues. Such rejects also occur when a document fails to meet minimum or maximum size specifications.

The document feeding area also includes a device called the batch detector. This is an optical sensing device located between the hopper and the acceleration drum to provide the means of stopping the feeding of documents upon the detection of a black band on the front of the batch ticket. By stopping the flow of items, all items in one batch can be completely processed before continuing with the next batch.

Transport and Read Area

This area is made up of four functional control points which are located between the document feeding area and the pocket area. The four functional points illustrated in figure 7-12 are as follows:

a. The aligning mechanism.

b. The read station.

c. Endorser unit (optional).

d. The chute blade selector.

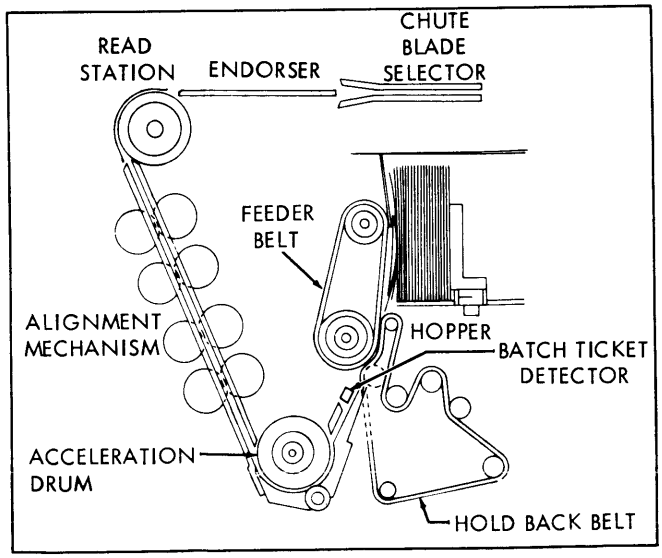


Figure 7-12. B 9131 Transport and Read Area

After the documents pass the acceleration drum, they enter the alignment mechanism which posi-

tions the documents by the application of a firm, but gentle, downward pressure by a series of eight alignment rollers, four of which are located on each side of the document transport belt. By the time the document reaches the end of the alignment mechanism, its lower edge is in the correct position for entry into the read station.

To assure that the characters to be read have been properly magnetized before the document passes the read head, it is passed over a permanent magnet. This permanent magnet is mounted in the stationary hub of the read drum assembly. A nonmagnetic metallic strap is used to guide the document through the read station and to maintain a constant pressure between the magnetized characters and the read head. After passing the permanent magnet, the characters on the document are read by the read head; and the resultant impulses are routed to the central processor memory.

The third control point in the B 9131/B 9132 Reader Sorter is an optional B 9932 endorser unit. This high-speed endorser provides the ability to endorse all items as they pass through the sorter-reader. The endorsement is printed on the backs of all documents as they move from the read station to the chute blades. While using the endorser, the Demand mode may not be used.

The fourth control point consists of the chute blade selector and magnetic assemblies which are used to control the path of the documents to the pockets and are under control of the central processor. There are 12 movable chute blades in the standard reader sorter. In actuality, the chute blades are in two sections (upper and lower) and so positioned that they cover the lower and upper portions of the document as it is routed to its pocket. The blades extend the entire length of the transport mechanism ending at the entrance to the document pocket. This assures that once an item enters the chute blades, it will only be routed to the selected pocket.

Transport and Pocket Area

The transport area is located above and behind the pocket area and carries documents from the chute blades to the pocket determined by the chute blade opening. Once the proper chute selection is made, the document cannot be delivered to any other pocket. Figure 7-13 shows the reader sorter with the cover raised and a document in the transport area.

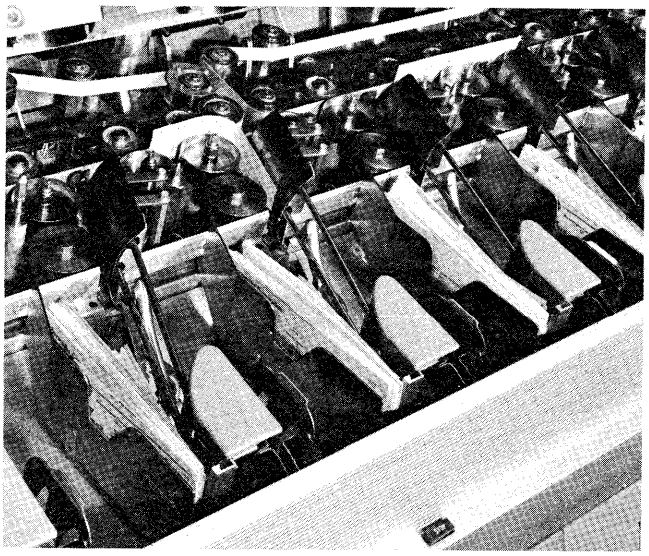


Figure 7-13. B 9131 Transport and Pocket Area

The standard reader sorter has 13 pockets positioned left to right from the document hopper and designated in the following order: reject, 0 through 9, X, and Y. Each pocket is 4 inches wide and has the capacity for approximately 800 documents. Items are sorted to any of the 13 pockets, based upon the program instructions in core storage. All checking functions are also under control of the central processor.

NOTE

The B 9132 Reader Sorter incorporates 16 distribution pockets. The sixteenth pocket (Y-pocket) has a 2000 item capacity as compared with 800 items for the other pockets. When operating in the off-line Sort mode, the additional three pockets serve as overflow capacity for the X-pocket.

There are two plastic worm gears in the bottom of each pocket which guide the lower edges of the document toward a sliding pocket wall (figure 7-14). These worm gears are friction driven so that light finger pressure will immediately stop their operation, thus protecting the operator.

As the documents enter the pocket, their leading edges are caught by the pull-in wheels. These wheels serve two purposes – they pull the items to the front of the pocket and keep the items from rebounding after hitting the front of the pocket.

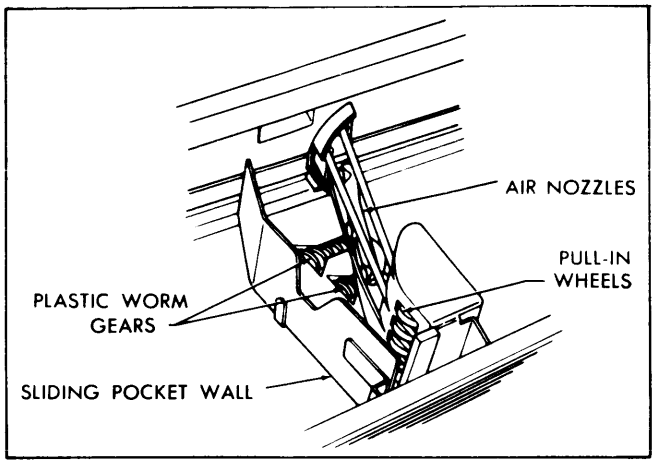


Figure 7-14. B 9131 Pocket Mechanism

While the bottom edge of the document is being guided by the plastic worm gears, a continuous jet of air from three air nozzles is directed against the top rear of the documents from the instant they enter the pocket. This helps position the documents and produces a more orderly pack of stacked items.

The right side of the pocket is engineered to guide the documents along smooth guide rails into their proper position in the pocket. The sliding pocket wall permits the pocket size to vary according to the number of items in the pocket. As documents enter the pocket, the sliding pocket wall moves to the left. When the pocket is filled to ¾ of its capacity (approximately 600 items), a pocket warning light, located immediately above the pocket, is turned on automatically. When the capacity of the pocket is reached, the document feeder automatically stops and a FULL POCKET indicator on the control panel illuminates.

Each pocket can be unloaded while the sorter-reader continues its normal sorting pattern by the use of a divider block which is similar in construction to the follow block in the document feeder. By inserting the divider block into the pack of documents in the pocket, the items to the left of the divider block can be easily removed while documents are entering the pocket during this operation. When the items have been removed, the sliding pocket wall, which provides the expansion pressure required to hold the items in place, returns to its normal position; and the divider block can be returned to the left side of the pocket.

Figure 7-15 shows the divider block in its normal position to the left of the sliding pocket wall, whereas figure 7-16 shows the divider block inserted in the pack of documents in the pocket prior to document removal.

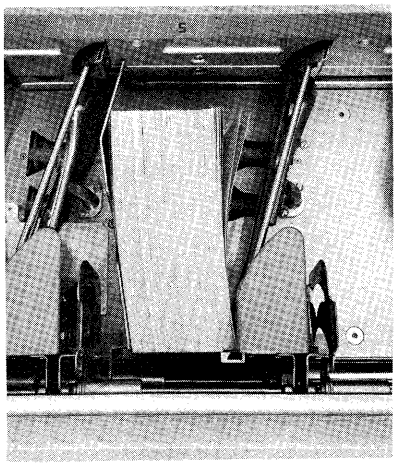


Figure 7-15. B 9131 Divider Block Normal

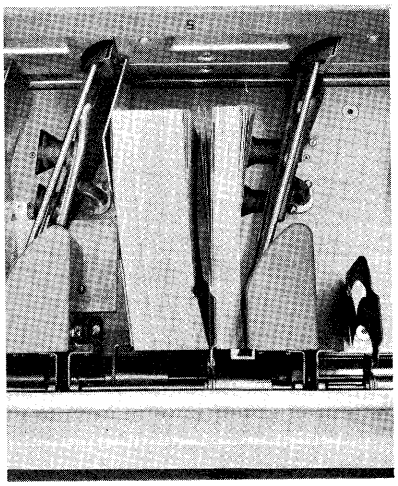


Figure 7-16. B 9131 Divider Block Inserted

Temporary Storage Area and Mobile Carrier

The temporary storage area and mobile carrier assist in the removal and storage of sorted documents efficiently while sorting operations continue.

Documents removed from the pockets during sorting can be placed in the corresponding compartments of the temporary storage area located above the transport area. Up to 4000 documents can be loaded in the removable item tray which moves in either direction with the mobile carrier. Figure 7-17 illustrates the two features.

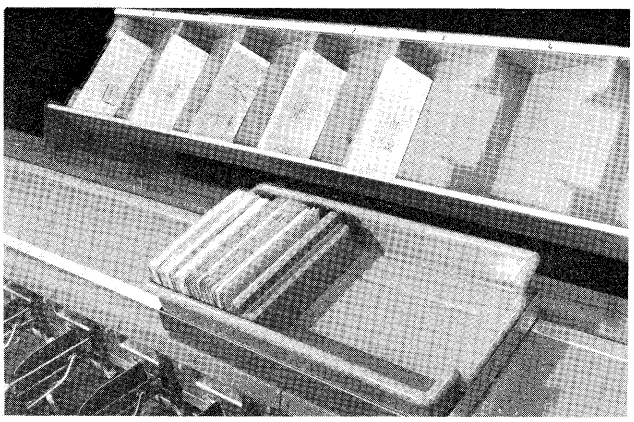


Figure 7-17. B 9131 Temporary Storage Area and Mobile Carrier

The reader sorter can also be used independently of the system. When used off-line, sorting is controlled by a patchboard housed in the rear of the control panel. A detailed explanation of the use of the reader sorter off-line is available in the Sorter-Reader Operator's Manual (1018678).

B 9131 and B 9132 Reader Sorter Control Panels

The reader sorter control panel contains a number of switches, indicators, and selection keys that provide a communication link between the operator and the reader sorter. There are four major elements of the control panel:

a. Operating switches.

b. Communication indicators.

c. Field selection keys.

d. Digit selection keys.

Figure 7-18 illustrates the control panels of the B 9131 and B 9132 Reader Sorter. The function of these switches and indicators is provided in tables 7-4 and 7-5.

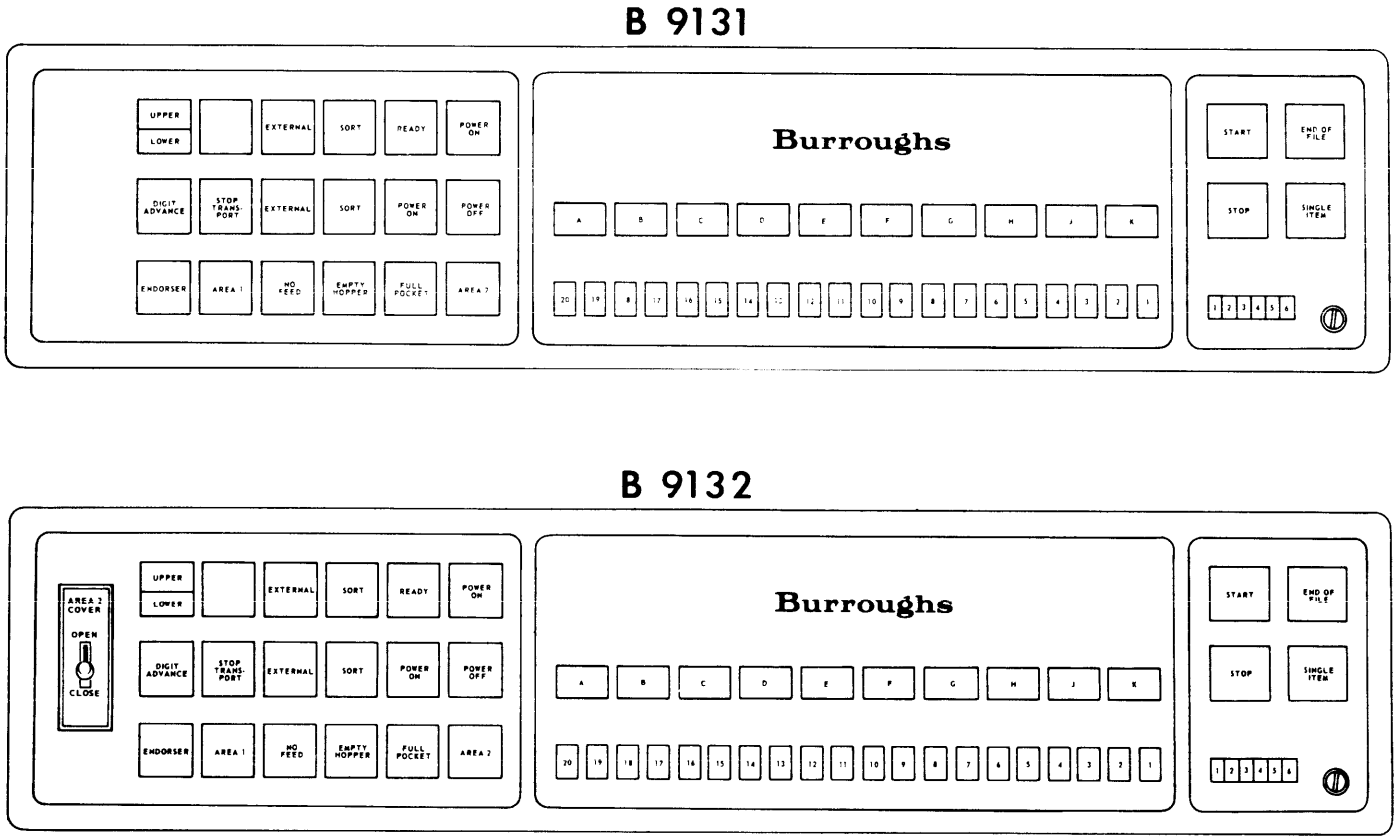


Figure 7-18. B 9131 and B 9132 Control Panels

Table 7-4
B 9131 and B 9132 Reader Sorter Control Panel Operating Switches

Switch	Function
(Left Side of Control Panel)	
DIGIT ADVANCE	This switch is used off-line to advance the three-digit batch number in the endorser unit by one. It is inactive if the document feeder is running. It has no function during on-line operation since the batch number is advanced by the external unit under program control.
STOP TRANSPORT	This switch is used to stop the transport system. The NO FEED indicator will turn on. To return the reader sorter to the Ready state, it is necessary to use the SINGLE ITEM switch.
EXTERNAL	When power is turned on, the reader sorter is automatically put in Sort mode. This switch is used to transfer control to the central processor when the reader sorter is used for input purposes. This switch can be used before the reader sorter is in a Ready state.
SORT	This switch has no function when the reader sorter is used on-line.
POWER ON	This switch applies power to the reader sorter. The POWER ON indicator will light.
POWER OFF	This switch removes power from the equipment. An auxiliary POWER OFF switch is located immediately to the right of the Y-pocket (figure 7-19). It serves the same function as the one on the control panel.

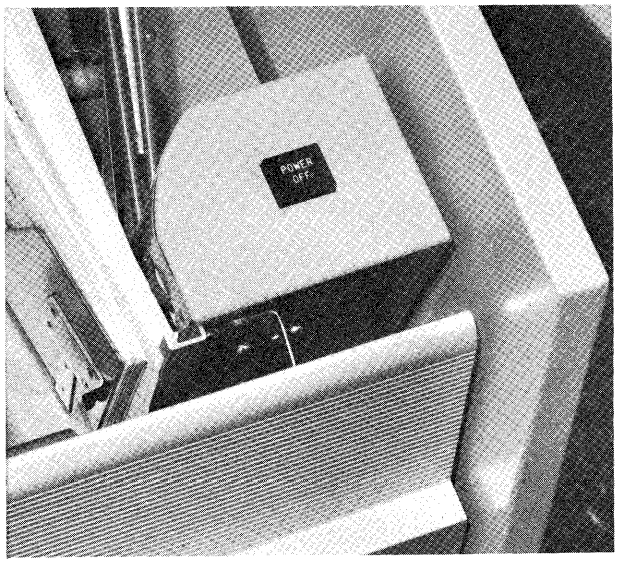


Figure 7-19. Auxiliary POWER OFF Switch

Table 7-4 (cont)
B 9131 and B 9132 Reader Sorter Control Panel Operating Switches

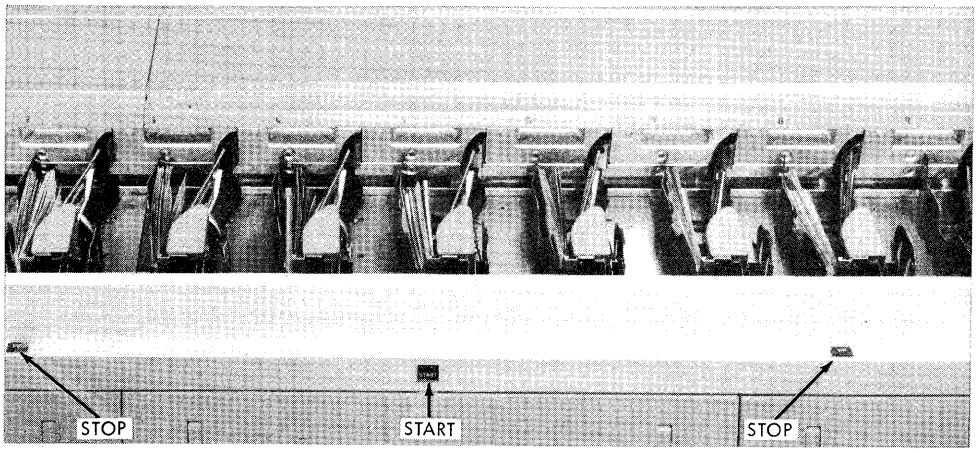
Switch	Function
(Right Side of Control Panel)	
START	This switch sends a signal to the central processor. Document feeding starts on command from the I/O control. Specifically, if the program has stopped because of an empty hopper, the program will restart automatically upon loading the hopper and using the START switch. In other instances, it is used simply to turn off the EMPTY HOPPER indicator.
END OF FILE	This switch is used to set the EOF bit in the result descriptor. The EMPTY HOPPER indicator will light to signal this requirement.
STOP	This switch is used to stop the feeding of documents. An interlock prevents the covers from being raised. The reader sorter remains in a Ready state when this switch is used. Item flow is resumed by using the START switch. Two other STOP switches are located in front of document pockets 2 and 8 for the operator's convenience (figure 7-20).
	
	Figure 7-20. Auxiliary START/STOP Switches
	NOTE The B 9132 Reader Sorter incorporates a start/stop bar that extends the length of the 16 pockets. This bar alternately activates or stops the system when pressed.
SINGLE ITEM	This switch must be used to put the reader sorter in a Ready state after a No Feed or Area 1 or Area 2 stop condition has occurred. A document is not fed in this instance. This switch should not be used to feed a single document when the reader sorter is used on-line.

Table 7-5

B 9131 and B 9132 Reader Sorter Control Panel Indicators

Indicator	Function
(Left Side of Control Panel, Top Row)	
UPPER/LOWER	This is a two-part indicator that operates only during the endorsing operation. The lower half is labeled LOWER and is green; the upper half is labeled UPPER and is amber. The lights indicate which of the two endorsing bands is active. When the endorser is active, one of the indicators will be lit.
EXTERNAL	This indicator indicates that the reader sorter is being operated on-line and under control of the I/O control. Sorting is determined by the program being executed.
SORT	This indicator is only operative when the reader sorter is used off-line.
READY	This indicator signals that the reader sorter is ready for use after power is turned on or a stop condition has been corrected.
POWER ON	This indicator lights when power is applied to the reader sorter.
(Left Side of Control Panel, Bottom Row)	
ENDORSER	This is a combination switch/indicator for control of the endorser device. When the endorser is off, pressing this switch will activate the device and the indicator will light. When the endorser is active, pressing this switch will turn the device off and the indicator will go out.
AREA 1	This indicator signals a document jam or a potential jam condition in the area between the acceleration drum and the chute blades. The indicator is turned off by pressing the SINGLE ITEM switch after Area 1 is checked and/or cleared and the Area 1 cover is closed.
NO FEED	This indicator lights when an item is not fed from the document hopper within 150 milliseconds after the preceding item or when a document jam occurs in the document feeding area. The indicator is turned off by use of the SINGLE ITEM switch provided a stop condition is corrected and the Area 1 cover is closed.
EMPTY HOPPER	This indicator lights when reader sorter instruction cannot be executed because a document is not present at the read station due to an empty hopper condition. The system will halt when this occurs. To continue processing, the hopper must be refilled and the START switch pressed to turn off the indicator. If the processing run has been completed, the END OF FILE switch is used to set the EOF bit in the result descriptor.
FULL POCKET	This indicator lights when a pocket reaches full capacity. Document feeding stops, and all documents in the transport system are directed to their respective pockets. At this point the system halts. The documents should be removed from the pocket and the START switch pressed to resume processing.

Table 7-5 (cont)
B 9131 and B 9132 Reader Sorter Control Panel Indicators

Indicator	Function
AREA 2	This indicator signals a document jam or a potential jam in the area encompassing the chute blades and the individual pockets. The indicator is turned off by use of the SINGLE ITEM switch.
AREA 2 COVER	On the B 9132 Reader Sorter, a two-position switch is provided on the control panel for raising and lowering the Area 2 cover. When the cover is raised, lights are lit to provide good visibility to the operator for clearing the jam and also to provide an additional warning that the cover is in the raised position. When the Area 2 cover switch is set to the down position, there is a slight delay before the cover actually begins to lower. During this delay, the lights under the cover begin to flash as a warning that the cover is going to lower. These lights continue to flash until the cover has lowered into proper position. When two people are operating the sorter, the person at the control panel should take great caution to warn the pocket operator when the cover is going to be lowered.

NOTE

On the right side of the control panel is a 6-digit, resettable item counter which counts the number of documents that pass through the reader sorter. The switch to the right of the counter is used to reset the counter to 000000. A B 9939 non-resettable counter can be obtained as a special option in place of the resettable one. The field and digit select switches located in the center of the control panel pertain only to the operation of the reader sorter while in the off-line mode. These are described in the Sorter - Reader Operator's Manual (1018678).

B 9134-1 READER SORTER

This reader sorter is capable of processing MICR encoded documents at a rate of 1625 documents per minute (DPM). The 1625 DPM rate is obtained with standard minimum length documents of six inches. Documents of greater length will result in a reduction of the DPM rate.

This unit reads E-13B MICR font. CMC7 MICR font is available and replaces the standard E-13B capability. Also available as options are capability to read OCR-A, size A and OCR-B, size 1, fonts.

The B 9134-1 is separated into five distinct areas (shown in figure 7-21 and depicted by A-E) and discussed in the paragraphs that follow. These five areas are as follows:

A. Basic unit.

B. Document feeding area.

C. Read area.

D. Control panel.

E. 4-pocket modules.

Standard Unit

The standard unit consists of four selectable pockets for stacking documents at a rate of 1625 DPM. This unit operates on-line, under control of an external device. Off-line sorting capability is available as an optional feature. The basic unit can be expanded by adding optional four pocket modules. This provides for configurations of 8, 12, 16, 20, 28, and a maximum of 32 pockets.

Document Feeding Area

The input hopper has the capacity to hold a 17½ inch stack of documents. The hopper may be loaded while the feeder is operating.

NOTE

Documents which are more than ½ inch above the hopper floor, at any point along the bottom edge of the documents, possibly will not be aligned properly for reading and consequently will be sent to the "Reject" pocket.

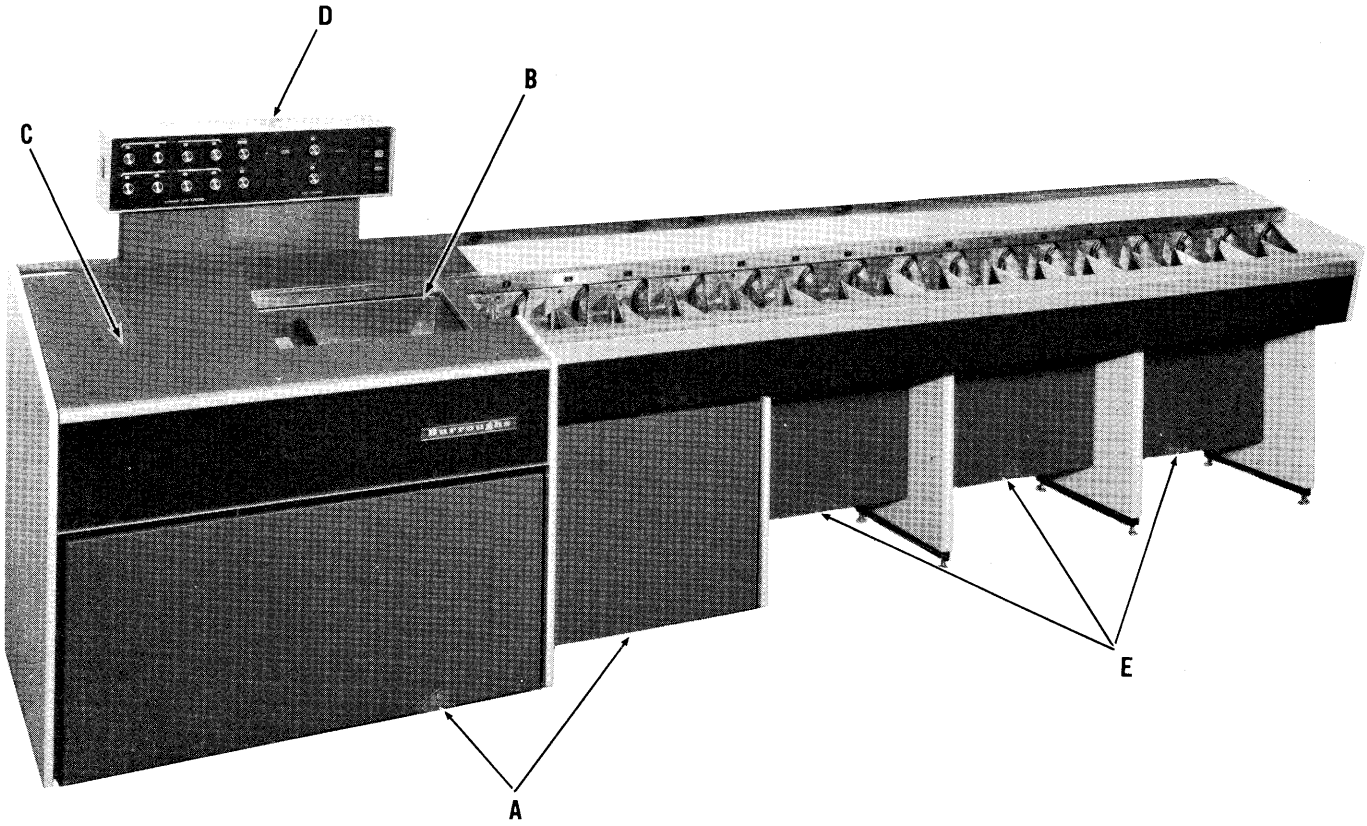


Figure 7-21. B 9134-1 Reader Sorter

The feeder is able to maintain a maximum document rate of 1625 DPM. This rate is obtained with documents which are six inches in length. Longer documents will result in the following rates:

a. 7 inches – 1392 DPM.

b. 8 inches – 1218 DPM.

c. 9½ inches – 1026 DPM.

The feeder is capable of handling documents which are of intermixed length, height, and thickness but, will cause a lower DPM rate.

Read Area

The standard read station consists of one read head which reads E-13B MICR characters located along the bottom edge of the document. This is accomplished via a multi-track character recognition system in accordance with ASA Standard X3.3–1963.

Dual read capability (optional) can be obtained by incorporating a second read head into the unit. Either one MICR and one OCR, or two OCR systems can be intermixed, used singly or together. When operating singly, the DPM rate is 1625 for 6 inch documents, unless otherwise specified. When both read heads are operating simultaneously, a rate of 1625 DPM with six inch documents should be maintained; however, if necessary, the rate may be reduced to a minimum of 1000 DPM with six inch documents.

NOTE

Only one character recognition system shall be active when operating in the optional off-line mode.

B 9134-1 Reader Sorter Control Panel

The reader sorter control panel contains a number of switches, indicators, and selectors that provide a communication link between the operator and the reader sorter. Figure 7-22 illustrates the B 9134-1 basic control panel. The function of these controls is provided in table 7-6. Figure 7-23 illustrates the full control panel with optional controls added to the basic panel. The function of these added controls is provided in table 7-7.

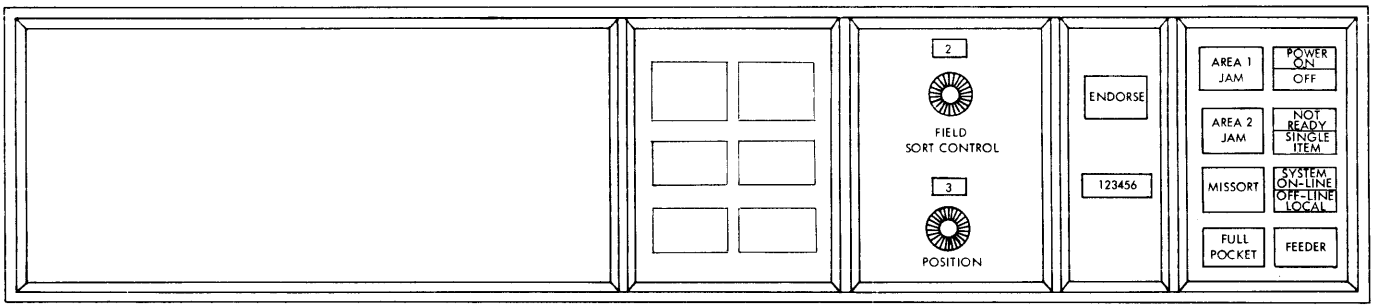


Figure 7-22. B 9134-1 Basic Control Panel

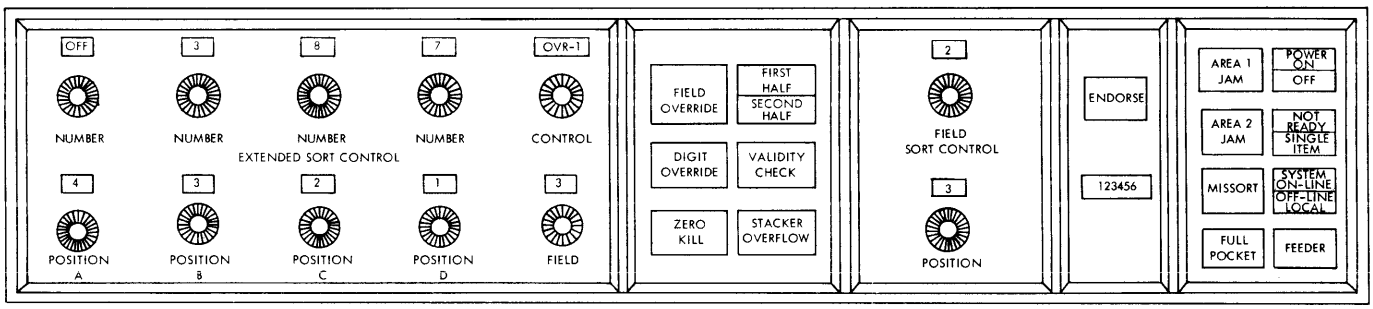


Figure 7-23. B 9134-1 Control Panel

Table 7-6
B 9134-1 Reader Sorter Control Panel Operating Switches

Switch	Function
POWER ON/OFF	An indicating switch which controls both power on and power off functions of the unit. This switch button has a upper and a lower area. The upper area is designated POWER ON and is illuminated when power is turned on. Color is green. The lower area is designated OFF, and is illuminated if any of the power controls for the transport motors or logic power are off. Color is red.
ON LINE/OFF LINE	An indicating switch which selects either the on-line (system) or the optional off-line (local) mode of the unit. This switch button has an upper and a lower area. The upper area is designated ON-LINE and is illuminated when the on-line mode is selected. Color is green. The lower area of the switch button is designated OFF-LINE, and is illuminated when the optional off-line mode is selected. Color is yellow. This switch must be in the OFF-LINE position whenever the maintenance mode is utilized on any unit.
NOT READY/SINGLE ITEM	An indicating switch which has an upper and lower area. The upper area is designated NOT READY and is illuminated when the unit is in a not ready state. The lower area is designated SINGLE ITEM and is non-illuminating. The switch controls the feeder and enables a single document to be fed each time it is depressed. The entire indicator is colored white.

Table 7-6 (cont)
B 9134-1 Reader Sorter Control Panel Operating Switches

Switch	Function
FEEDER	An indicator which is illuminated when the input hopper becomes empty or if the feeder fails to feed a document for a period of approximately 180 ms. Color is red.
AREA 1 JAM	An indicator which is illuminated if a jam occurs between the feeder and the endorser, inclusively. Color is red.
AREA 2 JAM	An indicator which is illuminated if a jam occurs in any location beyond the area for the endorser. Color is red.
MISSORT	An indicator which is illuminated if a document has gone into other than its designated pocket. The color is red. The pocket light of the pocket containing the missorted document will blink.
FULL POCKET	An indicator which is illuminated if a pocket is filled to capacity. Color is red.

Table 7-7
B 9134-1 Reader Sorter Control Panel Optional Operating Switches

Switch	Function
ENDORSE	An indicating switch located on the control panel and is illuminated when the endorser is active. Color is green. The endorser is activated by operator-accessible platen and cover-plate switches located on the endorser mechanism. The batch number will advance by one digit each time the ENDORSE indicating switch is depressed, but only when the unit is in the optional off-line or maintenance mode.
VALIDITY CHECK	An indicating switch which activates the validity character check feature. This feature when activated, checks the readability of each MICR OR OCR character and symbol in the field which is being sorted. If any character cannot be recognized, the document is sorted to the "REJECT" pocket. When this feature is activated, the VALIDITY CHECK indicating switch is illuminated. Color is green.
STACKER OVERFLOW	An indicating switch which activates the overflow feature. This feature enables the documents which are intended for the last off-line pocket (maximum of 16 pockets) to be routed to available adjacent overflow pockets, when the last off-line pocket is filled to capacity. The pocket directly adjacent to the last off-line pocket will be the first to receive the overflow and when filled, this process will be repeated sequentially with each available overflow pocket. When this feature is active the switch is illuminated. Color is green.
FIRST HALF/SECOND HALF	A two position indicating switch that provides for fine sorting, at any given digit position, on a 8-pocket unit. This fine sorting is accomplished in two sort passes. Depression of this switch will alternately select one of two modes; either First Half or Second Half. The upper area of this switch is designated FIRST HALF, and is illuminated when characters 0 through 4 are to be sorted. Color is green. The lower area of this switch is designated SECOND HALF, and is illuminated when characters 5 through 9 are to be sorted. Color is yellow. This feature can only be used on 8-pocket units.

Table 7-7 (cont)
B 9134-1 Reader Sorter Control Panel Optional Operating Switches

Switch	Function
ZERO KILL or NO FIELD-NO DIGIT	An illuminating switch adjacent to the STACKER OVERFLOW switch, which is designated either ZERO KILL or NO FIELD-NO DIGIT, depending on which option is desired. If labeled ZERO KILL, this feature will sort documents which contain a zero at a specific location to a designated zero kill pocket, providing the sort field contains only zeros to the left of the sort digit. If the digit in the sort position is not a zero, or if any of the positions to the left contain other than zeros, the document is sorted to the pocket which corresponds to the digit in the sort position. This feature is activated by the ZERO KILL switch. Color is green. If designated NO FIELD-NO DIGIT, this feature will outsort any documents which do not have a sort field at a specified location to a designated pocket. It can also outsort documents which do not have a sort digit in the normal sort position to another designated pocket. All other documents will be sorted to the regular pockets. This feature is activated by the NO FIELD-NO DIGIT switch which is illuminated when the feature is activated. Color is green.
DIGIT OVERRIDE or DIGIT EDIT	An illuminating switch adjacent to the VALIDITY CHECK switch, which is designated either DIGIT OVERRIDE or DIGIT EDIT, depending on which option is desired. If labeled DIGIT OVERRIDE, this feature will sort documents which contain a specific digit or digits at a specific location to either one or two designated override pockets. All other documents will be sorted to the regular pockets. This feature can be applied to digits 0 through 9. A maximum of five pairs of digits can be programmed on a unit, but only one selection may be active. Some units are restricted to single override digits and one override pocket. This feature is activated by the DIGIT OVERRIDE switch which is illuminated upon activation. Color is green.
FIELD OVERRIDE or FIELD EDIT	An illuminating switch adjacent to the FIRST HALF/SECOND HALF switch, which is designated either FIELD OVERRIDE or FIELD EDIT, depending on which option is desired. If labed FIELD OVERRIDE, this feature will sort documents which contain a specified eight digit consecutive code to a designated override pocket. All other documents will be sorted to the regular pockets. This feature is activated by the FIELD OVERRIDE switch which is illuminated upon activation. Color is green. If labeled FIELD EDIT, this feature will sort documents which contain a specific eight digit consecutive code to the regular sort pockets. All documents which do not correspond to the specific code will be sorted to a designated collection pocket. This feature is activated by the FIELD EDIT switch which is illuminated upon activation. Color is green.
FIELD SORT CONTROL/POSITION	Two separate dialable Sort Control selector switches provide for sorting in the off-line mode. The two switches labeled FIELD SORT CONTROL and POSITION, are controlled by a "field Card" which must be programmed by the field engineer to enable proper sorting off-line.
EXTENDED SORT CONTROL	The extended sort control option provides additional override capability for fields installed with the basic and extended off-line sort features.

A START/STOP bar (located along the front, and running the length of the modular unit(s)) controls the starting and stopping of the feeder by the operator. This bar is also the "RESET" control. A separate bar is provided for each 4-pocket section of a unit. One depression of the START/STOP bar will cause the feeder to stop. One depression of the START/STOP bar will cause the feeder to start after the correction of an empty hopper or full stacker pocket condition or after a previous feeder stop via the START/STOP bar. Two depressions of the START/STOP bar will be required to start the unit after the occurrence of either of the following conditions:

a. Stopped transport (other than two minute shut-down).

b. Open interlock.

c. Feed failure.

d. Jam.

e. Missort.

The first depression will reset the "not ready" condition and the second depression will cause the feeder to start. Three depressions of the START/STOP bar will be required to start the unit after a combination jam/missort condition occurs. The first depression will reset the missort condition, the second depression will reset the jam condition, and the third depression will cause the feeder to start.

4-POCKET MODULE (see figure 7-24)

The 4-pocket optional module provides the capability of increasing the number of stacker pockets, in groups of four, to a maximum of 32 pockets. Therefore, the basic 4-pocket DRS can be expanded to either 8, 12, 16, 20, 24, 28, or 32 pockets. All stacker pockets are of equal capacity and shall be numerically designated.

The stacker of each 4-pocket module contains four stacker pockets which receive documents which have been read or rejected. These pockets are designated as "R" [reject], "O", "1", and "2". Each pocket has the capacity to hold a 3½ inch stack documents. The stacker pockets may be unloaded while the unit is operating. Each stacker pocket has a red warning light which will indicate full pocket, missort, and jam condition for their respective pockets.

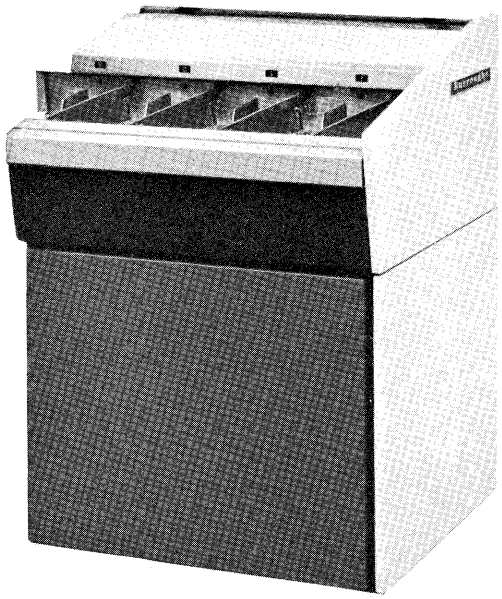


Figure 7-24. 4-pocket Module

NOTE

When operating in the off-line mode on units larger than 16 pockets, only the first 16 pockets are active.

DOCUMENT STORAGE RACKS AND MOBILE CARRIER

The Reader Sorter is designed to support document storage racks which are mounted on the top of each 4-pocket module. Each rack is capable of holding four document trays. The document storage racks and trays are not furnished by Burroughs and must be obtained by the customer from another vendor.

The mobile carrier is designed to hold one document storage tray. This carrier enables a storage tray to be moved along the DRS transport area. The storage tray is not furnished by Burroughs and must be obtained by the customer from another vendor.

B 9210 CARD PUNCH

The B 9210 Card Punch (figure 7-25) feeds, punches, checks, and stacks 80-column cards in both standard and post card thickness at the maximum rate of 100 CPM. The cards may be cut on any corner and may also be scribed for either tearing or folding. However, certain types of scribed cards may generate error signals if used with the PUNCH CHECK switch on (table 7-8) In the B 9210 Card Punch all formatting is under control of the object program. The B 9210 operation is completely buffered through the I/O control unit, thus allowing processing to continue during the card punch operation.

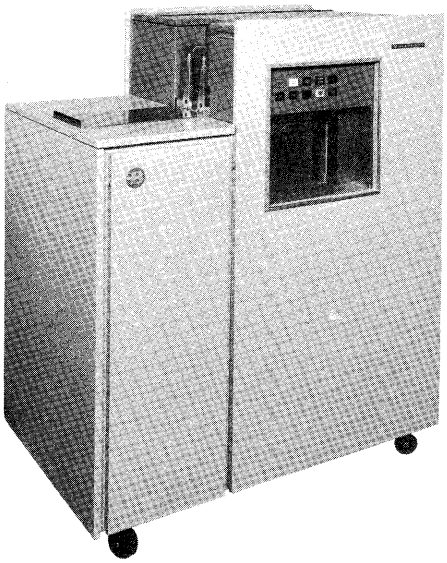


Figure 7-25. B 9210 Card Punch

Functional Characteristics

Cards that are to be punched are placed in the hopper, face down, 12-edge first. Card stock thickness must be consistent during any one run, and cards can be loaded into the hopper while the unit is operating without disturbing the cards that are already loaded into the hopper. Entry of cards into the feed rollers is accomplished by feed knives which select cards sequentially when activated by a feed signal. Cards are under positive control of pairs of feed rollers during their travel from hopper to stacker (figure 7-26). The B 9210 punch unit is capable of punching up to 80 columns simultaneously in any one row of a standard card without overloading. Up to 60 columns can be punched in post card stock cards. Card jams will not cause any damage to the punch mechanism. The stacker holds 800 cards and can be unloaded while the unit is punching. The B 9210 is capable of idling with cards in the feed mechanism. Card movement is controlled by the I/O control unit.

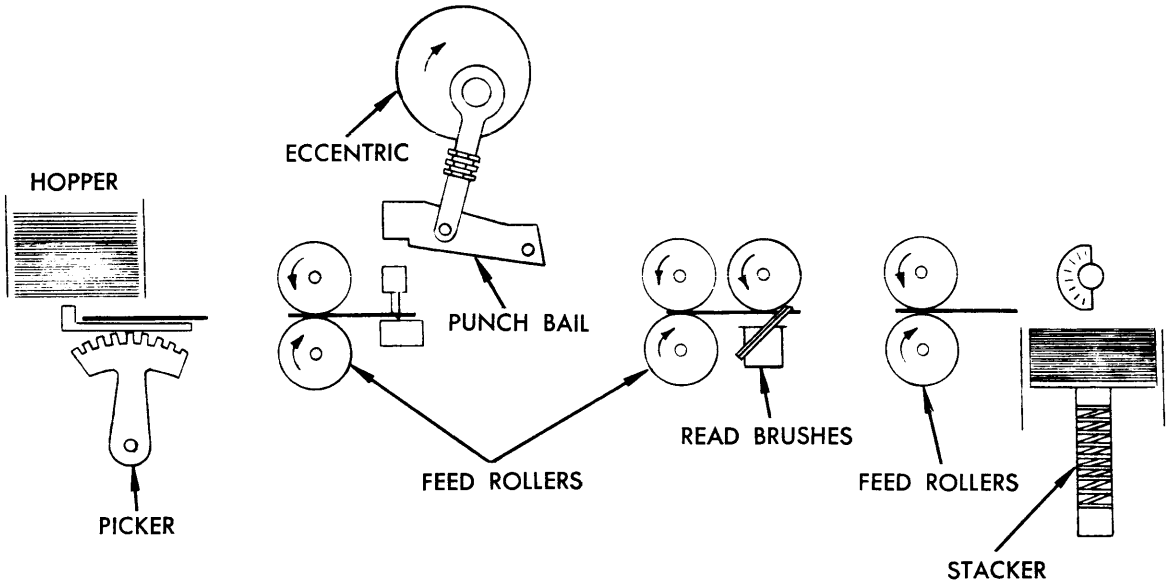


Figure 7-26. B 9210 Card Punch Feed Mechanism

Control Panel

The B 9210 Card Punch control panel (figure 7-27) contains switches and indicators for operation of the unit and indication of error conditions. The function of each of these elements is described in table 7-8.

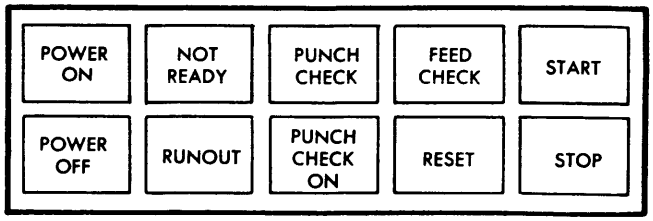


Figure 7-27. B 9210 Card Punch Control Panel

Table 7-8

B 9210 Card Punch Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This is a combination switch-indicator that applies power to the unit when pressed. The indicator lights when power is on.
NOT READY	This indicator lights when any one of the following conditions exists: STOP switch is pressed, empty hopper, improperly registered card, punch die not in place, card line mechanism not locked, stacker full, chip box not in place, and punching error. The condition causing the Not Ready state must be corrected, and the START switch pressed, before operation can be resumed.
PUNCH CHECK	This indicator lights if fewer than 80 data bits are received for each row, or if more or fewer than 12 row cycles are counted (punch station check). It will also light if the number of punched holes does not agree with the number of bits in the original data received from the I/O control unit (post-punch read station check).
FEED CHECK	This indicator lights when either a failure to feed or a jammed condition exists.
START	Pressing this switch causes one card to move from the hopper to the ready station, provided that all Not Ready conditions listed above have been corrected. Pressing this switch does not clear Punch Check or Feed Check conditions.
STOP	Pressing this switch will stop card feeding, light the NOT READY indicator, and set the unit to a Not Ready state. When the switch is pressed, cards that are in motion will be processed completely through the duration of the cycle.

Table 7-8 (cont)

B 9210 Card Punch Control Panel Switches and Indicators

Switch/Indicator	Function
RESET	Pressing this switch clears the Feed Check and Punch Check conditions.
PUNCH CHECK ON	This is a switch-indicator that selects either full punch checking or partial punch checking. The switch includes a mechanical toggle which reverses its choice each time it is pressed. When the switch is pressed and the indicator lights, a check is made of both punch station error conditions and post-punch read station error conditions. When the indicator is not lit, a check is only made on punch station error conditions. This feature allows the use of pre-punched and certain prescribed cards.
RUNOUT	As long as this switch is pressed, cards will pass through the unit without being punched. The switch is only effective when the unit is in a Not Ready state. Error conditions, if any, are not cleared.
POWER OFF	Pressing this switch removes power from the unit.

B 9211 CARD PUNCH

The B 9211 Card Punch (figure 7-28) has a maximum card punching capacity of 300 cards per minute (CPM). The format of the output cards is under object program control. Buffering through the I/O control unit allows processing to continue during the card punch operation. Cards can remain in the punch station for as long as five minutes while awaiting a punch command without any damage to the card. After five minutes, the card is released to the error stacker. Cards can remain in the punch station for as long as eight hours, with the unit turned off, without damage to the card. Cards can be cut on any corner or scribed for ease of tearing or folding. Certain types of scribing may generate error signals if used with the PUNCH CHECK switch on (table 7-9). Cards of varying thickness cannot be used during any one run.

Figure 7-28. B 9211 Card Punch

Functional Characteristics

The B 9211 card hopper holds approximately 1000 80-column cards of either standard or post card thickness. The cards must be placed in the hopper, face down, 12-edge first (figure 7-29). A removable ramp can be placed on the hopper to increase its capacity by an additional 2000 cards. The ramp automatically feeds cards into the hopper as they are required. Cards are automatically joggled as they are being fed from the ramp into the hopper. Cards can be loaded into the ramp while the unit is operating without holding the previous cards in

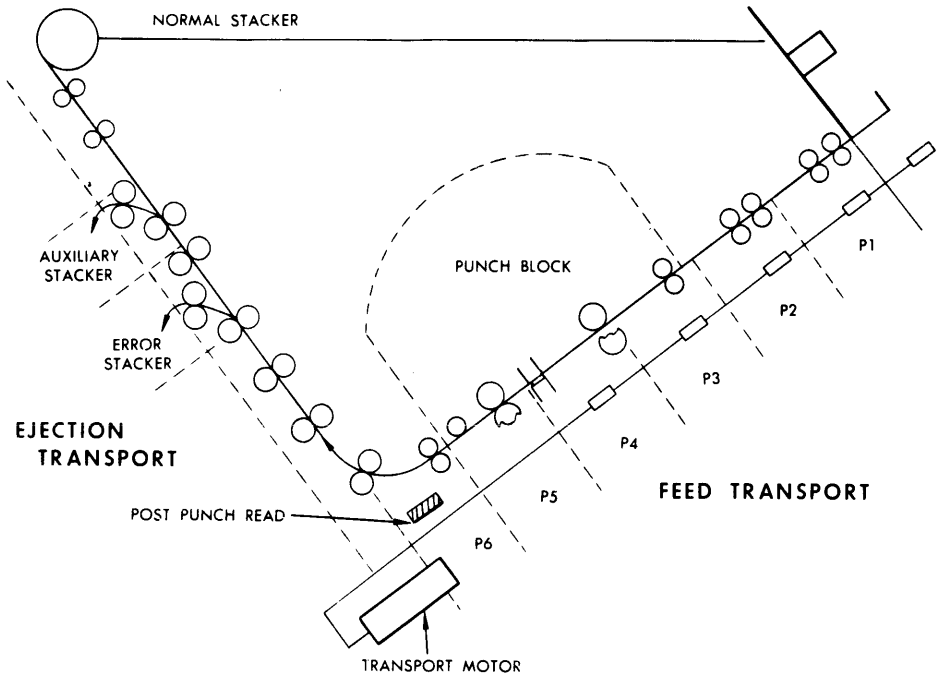


Figure 7-29. B 9211 Transport System

position. When there are no cards in the ramp, or if the ramp is not used, a follow block is required for proper feeding from the hopper. Cards are punched one row at a time by a single row of 80 punch dies. A punch station holds the card until it is punched. The same or random alphanumeric characters can be punched in all 80 columns of every card.

Punching all 960 holes in several successive cards due to punch or system malfunction does not result in equipment damage. A post-punch read station is used for punch checking. The reading is done by a row of 80 brushes. The B 9211 includes three card stackers: primary, error, and auxiliary. The three stackers each have a capacity of not less than 1000 cards. The primary stacker is a ramp type with a follow block that keeps the cards stacked neatly. Cards can be unloaded from the primary stacker while punching takes place. A full primary stacker causes a Not Ready condition. Error cards, ejected cards, and runout cards are stacked in the error stacker. A full error stacker causes a Not Ready condition. The stacker selection for each card is controlled by a signal from the central processor.

Control Panel

The B 9211 Card Punch control panel (figure 7-30) is located to the right of the card hopper and contains the switches and indicators for operation of the unit and for error indication. The functions of these elements are contained in table 7-9.

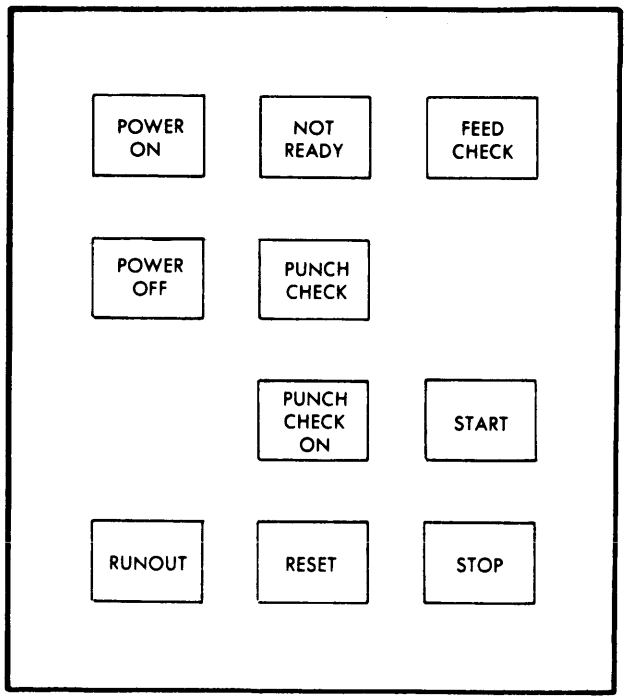


Figure 7-30. B 9211 Card Punch Control Panel

Table 7-9

B 9211 Card Punch Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This is a switch-indicator that applies power to the unit, and lights when pressed.
NOT READY	This indicator lights when one of the following conditions exists: no card at the punch station, feed check condition, card transport mechanism open, punch die not in place, covers not in place, punch error, and primary, auxiliary, or error stacker full. The error conditions must be cleared before processing can begin.
FEED CHECK	This indicator lights when there is no card present at the punch station because of either a failure to feed or a card jam (except when automatically ejected because of delayed punching).
PUNCH CHECK	This indicator will light if fewer than 80 bits of data are received for each row, or if more or less than 12 row cycles are counted (punch station check). It will also light if the number of punched holes does not agree with the number of bits in the original data received from the card punch control (post-punch read station check).
POWER OFF	This switch removes power from the unit.
START	This switch readies the punch for operation under control of the B 2500 or B 3500. The switch does not reset Feed Check or Punch Check error conditions.
PUNCH CHECK ON	This is a switch-indicator that selects between full punch checking and partial punch checking. The switch includes a mechanical toggle that reverses each time it is pressed. When the switch is pressed and the indicator lights, a check is made of both punch station error conditions and post-punch read station error conditions. When the indicator is not lit, a check is only made on punch station error conditions. This feature allows the use of pre-punched and certain pre-scribed cards.
RUNOUT	This switch causes cards in the feed line to pass through the machine without being punched. No additional cards are fed from the hopper. The switch is only effective when the unit is in the Not Ready state. Runout cards are directed to the error stacker. Error conditions, if any, are not reset.
RESET	This switch clears the Feed Check and Punch Check error conditions.
STOP	This switch causes the punch operation to stop after completing the punching of the card in the dies and then places the unit in the Not Ready state.

B 9212 CARD PUNCH

The B 9212 Card Punch is identical in appearance and operating characteristics as the B 9213 with one exception, the punching speed of the B 9212 is 150 CPM whereas the speed of the B 9213 is 300 CPM.

B 9213 CARD PUNCH

The B 9213 Card Punch (figure 7-31) has a maximum card punching capacity of 300 cards per minute. The card hopper has a capacity of at least 1200 cards of .007 inch, nominal, thickness. Cards in the hopper face the entry to the card transport area face down and enter it 12-edge first. A weight is provided and must be used to assure proper feeding if the amount of cards in the hopper falls to less than one inch. Cards can readily be added to the hopper when the unit is idling; or, if the supply

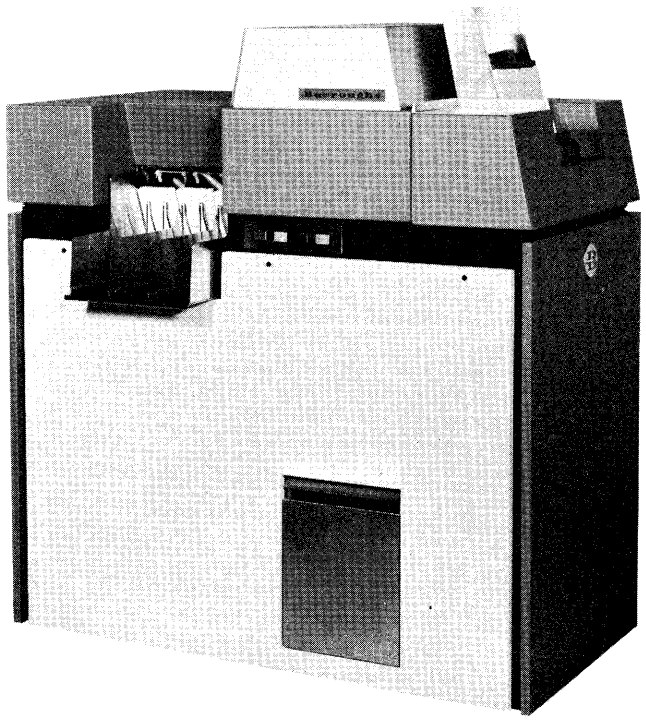


Figure 7-31. B 9213 Card Punch

of cards has not fallen below one inch, cards can readily be added during punching. A hopper extension may optionally be added, giving a total hopper capacity of at least 2200 cards of .007 inch, nominal thickness.

The B 9213 Card Punch includes three card stackers: primary, auxiliary, and error. Each of the three stackers has a capacity of not less than 1400 cards. A stacker is selected for each card by a control signal coming into the card punch from a card punch control. Cards are stacked in the correct order of reentry; they may be readily removed from the stacker during operation and during idling.

The feed mechanism feeds cards to the ready stop so that a 300 CPM rate can be maintained. Failure to feed a card causes the card punch to stop at the end of a card cycle.

The punching mechanism of the card punch is capable of punching rectangular holes in standard 80-column tab cards. Cards are punched one row at a time, face down, starting at row 12 and proceeding to row 9. The punch is capable of punching any combination of holes in any number of cards.

The B 9213 Card Punch is capable of idling indefinitely between commands, with a card at the punch station, without causing damage to the card. Parts which are subject to significant mechanical wear are permitted to stop if no request for operation is received for a period of 30 seconds. However, the punch remains in a Ready condition and responds to the next command after a start-up delay of approximately two seconds.

The punch provides a signal indicating readiness to start a card punch operation to an external device.

The punch also provides signals indicating readiness to accept serial-bit information for each row, one row at a time, 80 bits of information, two at a time, must be received by the punch for each row. All formatting is affected by the external device.

The punch detects no punch errors. However, it transmits to an external device serial-bit information indicating the movement of each punch for each row, one row at a time. 80 bits of information, two at a time, must be transmitted by the punch for each row. One additional dummy row cycle must be performed to obtain the punch movement information for the last row of a card.

A Not Ready condition occurs, which is indicated by the STOP switch illuminating, whenever any one of the following conditions exists:

a. Empty hopper.

b. Full stacker.

c. Failure to feed.

d. Pressing the STOP switch.

e. Jam.

f. Covers not in place.

If conditions a through d occur during the punching of a card, the card operation in process is completed. The motor in the card punch remains on for conditions a and b, and stops for conditions c through f.

Control Panel

The B 9213 Card Punch control panel (figure 7-32) contains the switches and indicators for operation of the card punch and for error indication. The functions of these elements are contained in table 7-10.

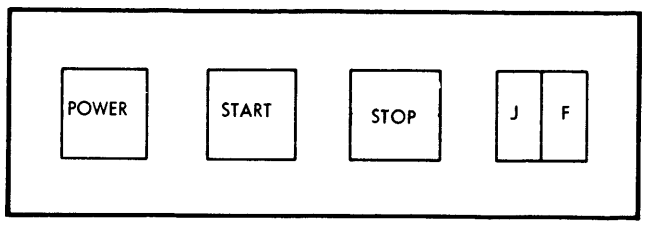


Figure 7-32. B 9213 Card Punch Control Panel

Table 7-10
B 9213 Card Punch Control Panel Switches and Indicators

Switch/Indicator	Function
POWER	Pressing this switch, when power is off, turns on the DC power supplies and fans in the punch; it does not turn the motor on. Pressing this switch, when power is on, turns off the DC power supplies, motor, and fan. When power is on, the switch is illuminated.
START	Pressing this switch when the punch is Ready causes the motor, if off, to be turned on and the switch to be illuminated. If the hopper is empty and the motor is running, a card is ejected from the punch station to the error stacker. If there are cards in the hopper, if the stacker is not full, if there is no stacker jam, and if all interlocks are closed, a Not Ready condition is eliminated, and the motor is turned on. This switch is non-illuminating.
STOP	Pressing this switch turns off the motor, if on, and causes a Not Ready condition. If a card is being processed when the STOP switch is pressed, the stop is delayed until the card is fully punched. The STOP portion of this switch is also illuminated for a Not Ready condition. When the Not Ready condition is eliminated, pressing this switch turns on the motor.
J/F	The J portion of this indicator and the STOP indicator are illuminated when a jam condition exists. The F portion of this indicator and the STOP indicator are illuminated when a misfeed condition exists.

B 9220 PAPER TAPE PUNCH

The B 9220 Paper Tape Punch (figure 7-33) is basically a teletype paper tape punch which is capable of punching standard paper tape format. The B 9220 will punch 5-, 6-, 7-, or 8-level tape at a minimum rate of 100 CPS, ten characters per inch. Standard tape widths of 11/16, 7/8, and 1-inch may be punched, as selected by the operator. Either oiled paper tape, laminated fiber, dry paper tape, metalized or laminated Mylar paper tape may be punched on the B 9220. The maximum size supply reel that can be placed on the B 9220 is eight inches in diameter. The reel hub measures two inches in diameter. The punched tape is wound onto a 5½- or 7-inch diameter take-up reel. It is not necessary to use the take-up reel when punching tape. The end-of-tape is indicated by the LOW TAPE indicator when approximately 35 feet of tape remain on the supply reel. The B 9220 is buffered through the I/O control unit. This allows processing to continue while punching paper tape.

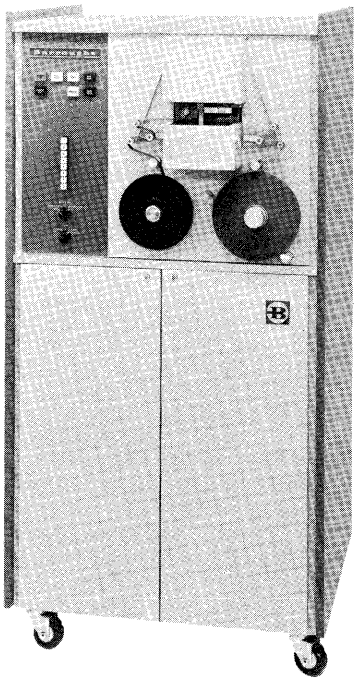


Figure 7-33. B 9220 Paper Tape Punch

Functional Characteristics

A method is provided for the operator, through the channel select plugboard wiring, to interchange any of the five, six, seven, or eight channels that might be desired. Undesignated channels in the channel select plugboard are not punched or sensed as controls for the B 9220. When the B 9220 receives a Paper Tape Write instruction from the I/O control unit, paper tape will be punched in a forward direction. The output record length is determined by a specific word count in the I/O descriptor or a control code in the data stream which is manually designated by a switch setting on the B 9220 control panel or translator. The code is punched or suppressed as indicated by the control code switch or translator plugboard wiring. BCL codes are transferred from the I/O control unit, one character at a time, to the paper tape punch. The code translator permits the translation of BCL to a single frame code by means of a removable plugboard. Also, teletype codes can be translated. Teletype is a double-case code (figures/letters shift) with several special requirements. To accommodate the shift used by teletype code, each of the allowable characters is designated as a figures or a letters code. Whenever a character is of a different case (figure/letter) than its predecessor, the appropriate shift code must be punched prior to the character. The two shift codes used for teletype tape can be designated by code translator plugboard wiring. The special requirements used for teletype codes are:

a. Automatic generation of codes for the figures shift after Space, Tab, Line Feed, and Carriage Return.

b. Automatic generation of codes for the carriage return, and line feed only must be generated immediately following all end-of-line codes.

Channel Select Plugboard

This plugboard is provided mainly for purposes not requiring a translator. It is possible for the operator to select any of the six internal code levels and interchange them to any of the eight possible paper tape channels. Paper tape with even parity can be punched by inverting the desired channel. All unused channels must be connected to the corresponding C channel. Figure 7-30 illustrates the channel select plugboard BCL and Teletype wiring configuration.

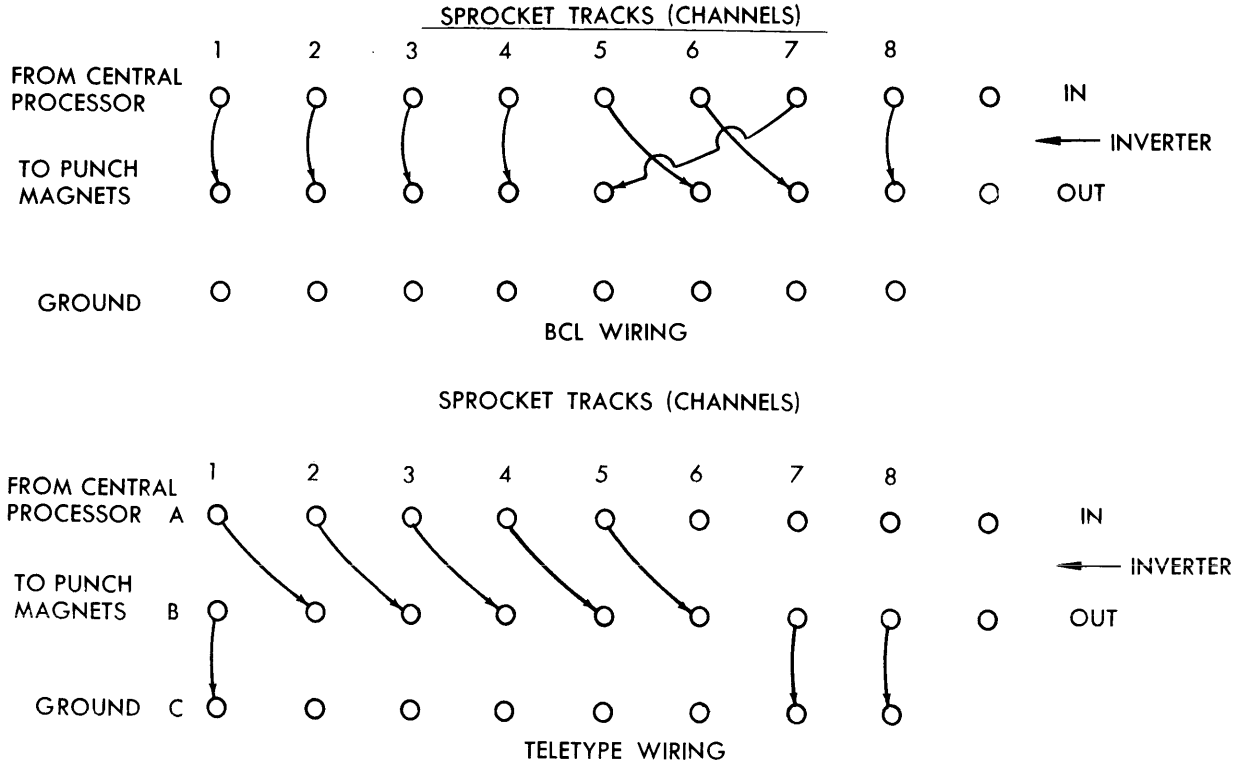


Figure 7-34. Channel Select Plugboard

B 9928 Code Translator

The B 9928 Output Code Translator, which is an optional feature, permits translation of BCL code to any 5-, 6-, 7-, or 8-channel code. The code translator is located in the paper tape punch cabinet. Character (code) flow is from the I/O control unit to the channel select plugboard to the translator to the paper tape punch. The following describes the plugboard layout (figure 7-35):

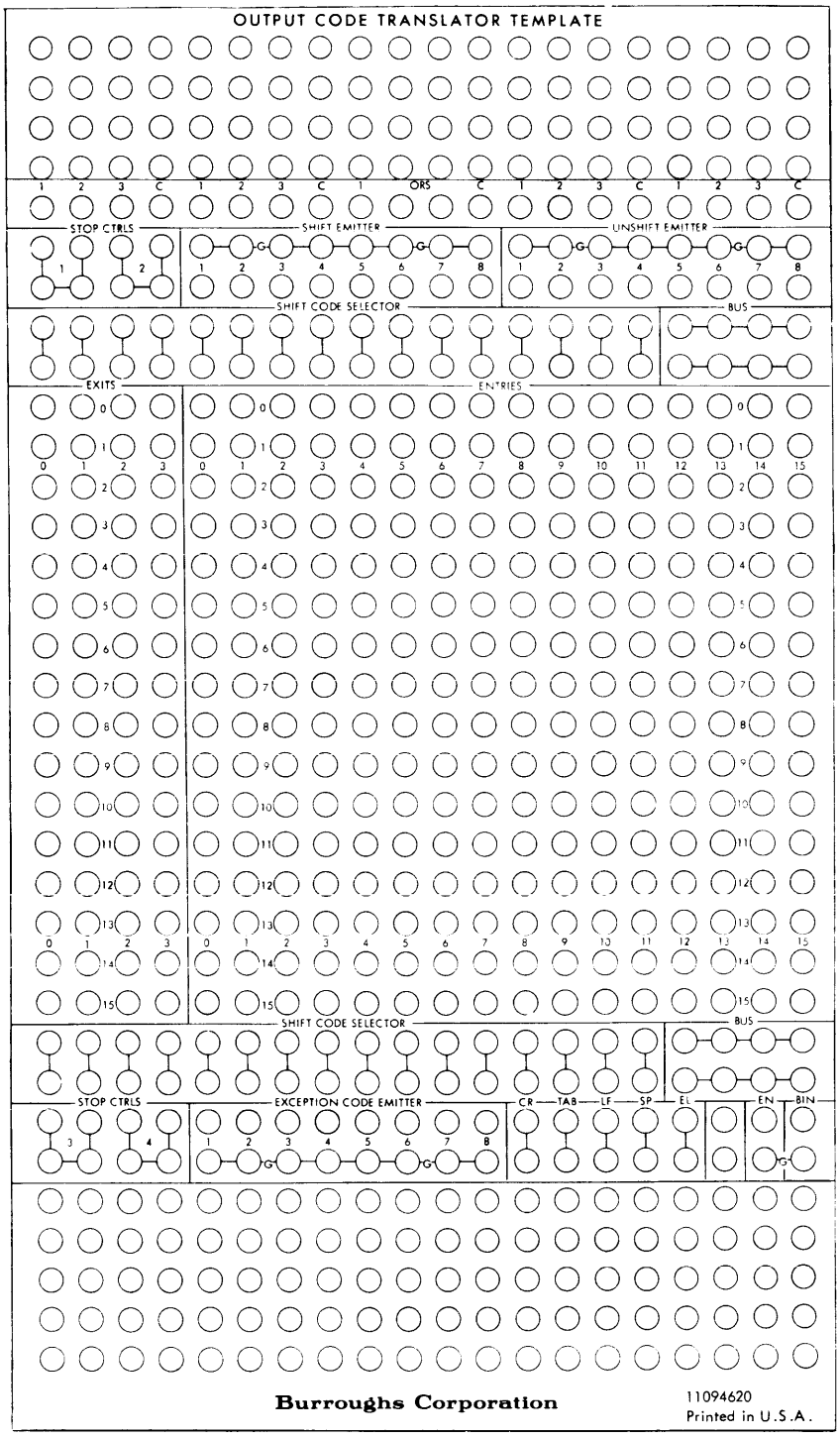


Figure 7-35. B 9928 Plugboard Layout

a. Exits: The exit hubs represent data sent from the I/O control unit via the channel select plugboard. Assume the following bit configuration.

	1	2	4	8	A	B	P
		.	.		.	.	.
Corresponding channel hubs (B) on channel select plugboard	1	2	3	4	5	6	7

Input to punch logic (B) hubs 1 to 4 of the channel select plugboard identify the translator row (binary value).

Binary Equivalent	(1)	(2)	(4)	(8)	
(B) Channel hubs	1	2	3	4	
(bits from 1 to 4)		.	.		or row 6

Therefore, the assumed bit configuration identifies column 3, and row 6 of the exit hubs.

b. Entries: The entry hubs, when impulsed, generate the selected 5-, 6-, 7-, or 8-channel output character to be punched. There are 256 possible combinations using eight level code. The code punched is determined by column and row. The decimal value of the column and row are converted to a binary value as follows:

The binary value of the column identifies which channels, 1 to 4, are to be punched. Example: column 10 would punch

Binary Equivalent	(1)	(2)	(4)	(8)
Channel	1	2	3	4
Punches		.		.

The binary value of the row identifies which channels, 5 to 8, are to be punched. Example: row 7 would punch

Binary Equivalent	(1)	(2)	(4)	(8)
Channel	5	6	7	8
Punches	.	.	.	

Therefore, if column 10 of row 7 were impulsed, the following code would be punched in paper tape.

Channel	1	2	3	4	5	6	7	8
Punches		.		.	.	.	.	

c. Stop Controls: There are four sets of stop control hubs. To designate a stop code, an exit hub is wired to a stop control hub. If the stop code is to be stored, a stop control hub, impulsed by a connected exit hub, is connected to the desired entry hub. If an entry hub is not connected to the stop control hub, the stop code will not be punched.

d. Shift Codes: These hubs are required when the output data requires shift and unshift codes. These hubs are connected to exit hubs to determine which codes require a shift code (maximum 32). Any codes not connected to these hubs are considered as requiring an unshift code. The associated hub is connected to an entry hub for the required code translation. Whenever a change is required from an unshift code to a shift code or vice versa, as selected on these hubs, the appropriate shift or unshift code is punched.

e. Shift Emitter: Any 8-bit code can be selected as the shift code by connecting the channel requiring a bit to the hub located directly above the designated channel. All channels unconnected will be considered as a zero (no bit). This code will be punched when required as designated by the shift code selection.

Unshift Emitter: Any 8-bit code can be selected as the unshift code by selecting the channel requiring a bit to the hub located directly above the designated channel. All channels unconnected will be considered as a zero (no bit). This code will be punched when required as designated by the unselected codes, that is, those not connected to the shift code selector hubs.

OR Hubs: The OR hubs permit up to three different codes, designated by the exit hubs, to initiate one common code or action.

f. Exception Codes: These hubs are provided to handle special Teletype code set problems. These codes are CR, TAB, LF, SP, and EL. These codes are connected from the exit hubs and to the selected entry hubs. Since these codes will not be selected as shift codes, they will be considered as unshift codes. The EL (end-of-line) code will initiate the punching of the exception code before the actual code is punched. The exception codes are set up in the exception code emitter.

g. Exception Code Emitter: Any 8-bit code can be selected as this code by connecting the channel requiring a bit to the hub located directly above the designated channel. All channels unconnected will be considered as a zero (no bit). This code will be punched when required by the designated EL code.

h. Bus Hubs: There are two sets of bus hubs. Each set permits multiple connections to a single hub.

i. Enable Hubs: These hubs must be connected to activate the translator. If unconnected, the normal translation of BCL internal code to BCL paper tape code will take place.

Control Panel

The B 9220 Paper Tape Punch control panel (figure 7-36) contains the switches and indicators for operation and error indication. The function of each element is described in table 7-11.

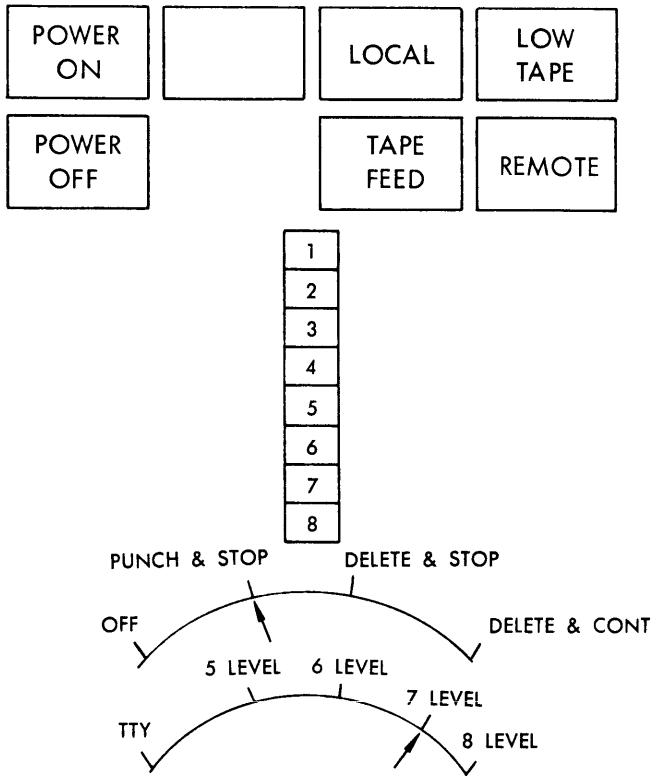


Figure 7-36. B 9220 Paper Tape Punch Control Panel

Table 7-11

B 9220 Paper Tape Punch Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This switch-indicator lights when pressed, indicating that power is applied to the unit.
NOT READY	This indicator will light when a Not Ready condition exists.
LOCAL	This switch-indicator places the B 9220 in a Local condition, making the unit unavailable to B 2500 or B 3500 Systems.
LOW TAPE	This indicator will light when 35 feet of tape, or less, remains on the supply reel.
POWER OFF	This switch removes power from the unit.
TAPE FEED	This switch feeds tape with all holes punched. The switch is active when the LOCAL switch is activated. The tape feed rate is 100 characters per second.

Table 7-11 (cont)

B 9220 Paper Punch Control Panel Switches and Indicators

Switch/Indicator	Function
REMOTE	This switch-indicator lights when pressed, indicating that the unit is under control of the B 2500 or B 3500 System.
CONTROL CODE	This switch allows the operator to designate a control code. The code may or may not be punched. The switch is active in REMOTE or LOCAL and has four positions, which determine the action taken when a control code is detected. The four positions of the switch are: OFF, PUNCH AND STOP, DELETE AND STOP, and DELETE AND CONTINUE.
LEVEL DESIGNATION	This switch is used to select the number of channels and type of paper tape to be used.

LINE PRINTERS

The Burroughs Line Printers provide high-quality, high-speed, alphanumeric printout. Line printers, varying in operating speeds from 315 LPM to a maximum of 1040 LPM, and available with either 120 or 132 print positions, are provided for use on B 2500 and B 3500 Systems.

For all practical purposes, the operational characteristics of the line printers are similar; therefore, the description that follows applies to all printers except where specifically noted.

Functional Description

EBCDIC or BCL codes for characters to be printed are compared with codes of upcoming graphics in the printer. Where there is coincidence, the graphics are printed. Scanning and printing are continued until all characters of the line are printed.

The buffer and scan functions for buffered printers (B 9240, B 9241, and B 9245-1) are in the printers. The buffer and scan functions for unbuffered printers (B 9242 and B 9243) are in the unbuffered printer control.

Continuous forms are used in the printer, and skipping and spacing operations are controlled by the program through the use of the I/O control unit. Vertical spacing may be from zero to 99 spaces before or after printing a line. Each line consists of 120 or 132 print positions, 10 positions per line. Vertical spacing is six or eight lines per inch. Formatting and editing are under object program control.

There are 63 alphanumeric and special characters, plus a blank for each print position. The 64 characters contained in each print position consist of 26 alphabetic, 10 numeric, and 28 special characters (refer to appendix D). Printing is done on continuous paper forms which may be from 5 to 20 inches in width, including marginal punch strips. Length can be 22 inches (at 6 lines per inch) or 16½ inches (at 8 lines per inch). The forms are loaded in the cabinet below the printing mechanism and forms are transported through the unit, by means of pin-fed tractors, to the stacker. As many as five carbons plus the original may be printed. In general, the printer can process legible copy forms up to 0.02 inch in overall thickness. The thinnest form that can be processed is 0.0025 inch. The optimum number of copies can be legibly printed by using premium paper and carbon. A clearance adjustment, required when changing from one form thickness to another, is available to the operator and can be accomplished within 30 seconds without the aid of tools.

TAPE CONTROLLED CARRIAGE

The line printer does not directly control the feeding and spacing of the forms. This is performed by the tape controlled carriage of the printer in conjunction with instructions from the I/O control unit.

CONTROL TAPE

The carriage control tape (figure 7-37) has column positions (1-12) called channels. Horizontal lines can be skipped (up to 132 lines) for control of a form. For ease in preparation, the tape is somewhat longer than required. Pre-punched holes located in the center of the tape are used by a pin feed mechanism to move the tape past the sensing device. Movement of the carriage control tape is synchronized with the movement of the form

through the carriage. Skipping the form to any predetermined position is accomplished by addressing any one of 11 holes in the carriage control tape. A twelfth channel in the control tape is used to signal the last print line on the form. When a hole in this position is sensed, the printer sends a signal to the I/O control unit, flagging the result descriptor for the MCP. The twelve carriage control tape channels are usually punched to control the following functions:

a. Channel 1 will normally be used to identify the first print line (heading) of a form.

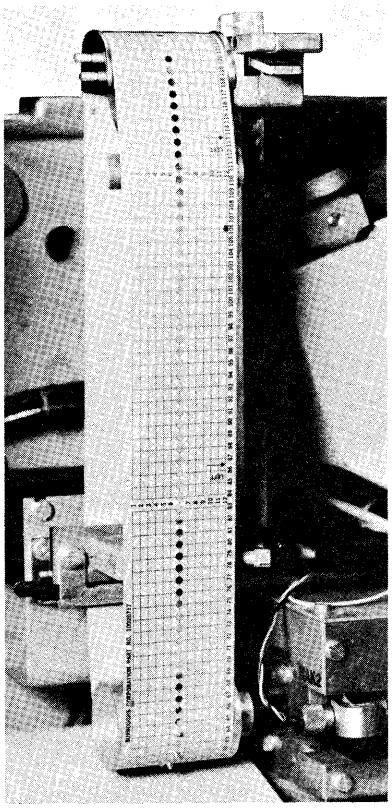


Figure 7-37. Carriage Control Tape

b. Channel 2 will usually be used to indicate the first body line of a form on which detail information appears. In an invoicing operation, where the first printing line and first body line are not the same, channel 1 would be used to indicate the heading on the form, in this case a name and address. Channel 2 would correspond to the first printed line of detail information.

c. Channels 3-11 will normally be used to identify any one of 9 user determined print positions. These channels may be used in any desired sequence.

d. Channel 12 is reserved for punching the hole indicative of the last printing line in the body of a form.

The nominal skip speed is 25 inches per second with an optional high-speed skip of 75 inches per second.

CONTROL PANEL

A typical line printer control panel (figure 7-38) contains switches and indicators for operation of the equipment and for error indications. The control panel is located at the front of the unit, to the right of the print section. The function of the switches and indicators is described in table 7-12.

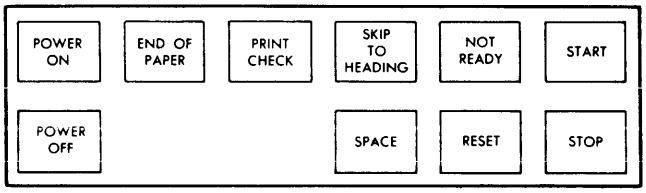


Figure 7-38. Line Printer Control Panel

Table 7-12.
Line Printer Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This is a switch-indicator that applies power to the unit and lights when pressed.
END OF PAPER	This switch-indicator signals nearing an out-of-paper condition. Pressing this switch removes the end-of-paper condition and extinguishes the light. One line can then be printed; thereafter, the unit returns to the end-of-paper condition. Successive depressions of this switch enable printing successive lines to complete the last line on a form.

Table 7-12 (cont)

Line Printer Control Panel Switches and Indicators

Switch/Indicator	Function
PRINT CHECK	This indicator lights when a print check error has been sensed, or when the print drum is not properly synchronized.
SKIP TO HEADING	Pressing this switch causes the carriage to skip to the first punch in channel 1 of the carriage control tape.
NOT READY	This indicator will light when any one of the following conditions exists: the END OF PAPER indicator is lit, the 6/8-lines-per-inch switch is in position N, the unit slews paper for more than one second, or the START switch has not been pressed.
START	This switch is used to signal the B 2500 or B 3500 System that the printer is ready for use. It is also used to restart printer operations stopped by a line printer Not Ready condition.
STOP	Pressing this switch will stop the line printer prior to the execution of the next Print instruction. The print buffer will not be loaded after the switch has been pressed, and the printer will go Not Ready.
RESET	Pressing this switch resets the PRINT CHECK indicator. (This function is combined with START in 815-LPM printers.)
SPACE	Pressing this switch causes the forms to be single spaced.
POWER OFF	This switch removes power from the unit.

In addition to the above mentioned indicators and switches on the control panel, duplicate controls and indicators are provided at the rear of the printer for increased operator efficiency. These duplicate switches and indicators include START, STOP, RESET, SPACE, NOT READY, and SKIP TO HEADING. They perform the same function as their counterpart on the control panel.

B 9240 LINE PRINTER

The buffered B 9240 Line Printer (figure 7-39) operates at a speed of 700 LPM and contains 120 print positions. An additional 12 print positions are available through the use of a B 9941 option.

B 9241 LINE PRINTER

The buffered B 9241 Line Printer operates at 1040 LPM and contains 120 print positions. Twelve additional print positions are available through use of the B 9941 option. This printer features a "quick cancel" memory and a rearranged character set to permit high-speed printing. The 37 most-used characters are arranged in consecutive locations on the print drum. At the instant a character is printed, its buffer position is set to blank. When all characters in the buffer are blank, the printer is released for spacing. This allows paper to be advanced while unused character locations on the drum are passed. This printer is similar in appearance to the B 9240.

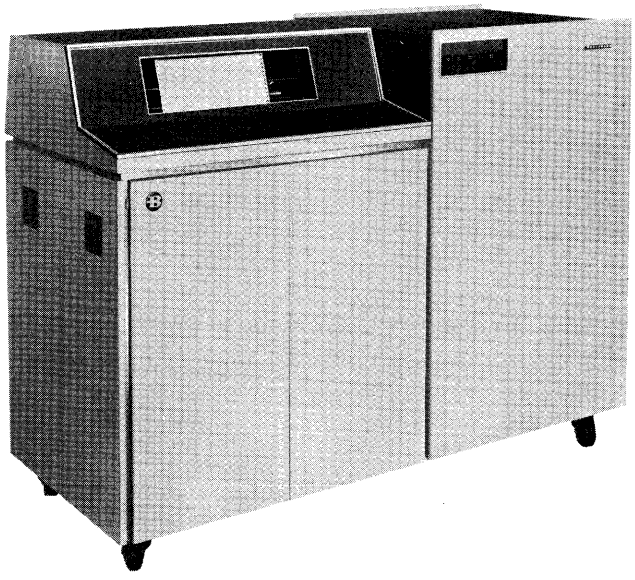


Figure 7-39. B 9240 Line Printer

B 9242 LINE PRINTER

The unbuffered B 9242 Line Printer (figure 7-40) when controlled by a suitable external device has an inherent print rate (using a 63 or 64-graphic character set) of 815 single-spaced LPM. Higher rates of print are attainable when certain subsets of fewer than the available 64 characters are printed.

NOTE

This increase is obtained with the normal drum, which contains no replicated subsets of graphics.

Figure 7-40. B 9242 Line Printer

The blank code is a member of all subsets. If the B 9240 is buffered (optional), the blank code can be assigned to more than one row of the drum if an optional character set is to include fewer than 63 unique characters. Of the 64 characters on the drum, 63 or fewer can be printed by the buffered printer.

The B 9242 Line Printer contains 120 print positions (132 with B 9941 option) of the same graphic, which form one printer row. There are 64 such rows and each row is assigned a 6-bit code.

Functional Description

Each of the 64 rows on the drum of the B 9242 Line Printer contains the graphic corresponding to one code only, in all print positions (columns). As each row of graphics comes into position under the print hammers, the printer generates a code corresponding to the upcoming row. This code is made available to the printer control. This code is generated by a modular, replaceable code unit.

The printer contains a bit register with a position corresponding to each of the printer columns. The bit controls the print hammer for its corresponding column.

The printer control transmits bit information to indicate in which columns the upcoming graphic is to be printed. A 1 is sent to indicate print, or an 0 is sent to indicate non-print, for each of the 120 or 132 columns in sequence, starting with the bit-pair for columns one and two. The unbuffered printer can print the graphic row opposite the encoders blank code, if so signaled by the printer control. The drum is not to contain any replicated rows of the same character(s).

The printer provides to the printer control, a signal indicating that the final bit-pair of column storage is being addressed.

The printer prints the upcoming graphic in the columns indicated, and provides the code for the next upcoming graphic. This process continues until terminated by a signal from the printer control.

The buffered B 9242 Line Printer accepts information for the buffer parallel by bit and serial by character, least significant character or digit (LSD) first. It then receives format information, releases the control, and begins printing.

NOTE

An optional feature which allows information to be received MSD first is available.

The code of each up-coming row of graphics on the drum is compared to the codes of the characters in the buffer and printed in those positions in which coincidence occurred. Compare-and-print is continued until all characters of the line are printed. When this occurs, the paper motion prescribed by the format information is performed. During this paper motion, the buffer can be reloaded by the printer control, for the next line. The format for

the next line can be received by the printer as soon as paper motion stops. At this time, the just-loaded line is printed, etc.

B 9242-1 LINE PRINTER

The unbuffered B 9242-1 is similar in appearance to the B 9242 which it replaces. The operating characteristics are the same except for printing speed. The speed of the B 9242-1 is 860 LPM, whereas the B 9242 is 815 LPM.

B 9243 LINE PRINTER

The unbuffered B 9243 Line Printer is similar in appearance to the B 9242, but its print speed is 1040 LPM due to the arrangement of the 46 most-used characters on the print drum. The printer contains 120 print positions with 12 additional available with the B 9941 option. The B 9940 optional slew rate is also available with this printer.

B 9243-1 LINE PRINTER

The unbuffered B 9243-1 Line Printer is similar in appearance to the B 9242. The B 9243-1 replaces the B 9243 and, has the same operating characteristics with the exception of printing speed. The speed of the B 9243-1 is 1100 LPM whereas the speed of the B 9243 is 1040 LPM.

B 9245 LINE PRINTER

The buffered B 9245 Line Printer (figure 7-41) operates at a speed of 315 lines per minute, contains a 64-character set, and is available with either 120 print positions (B 9245-2 Line Printer) or 132 print positions (B 9245-3 Line Printer).

B 9943 PRINTER MEMORY

The B 9943 Printer Memory is an optional feature available on the B 9242-1 and B 9243-1 Line Printers. Printer Memory is an external buffer containing 120 or 132 character positions, and it is physically located in the printer. Printer Memory gives a line printer the externally buffered characteristics of the B 9240 and B 9241 Line Printers. This option is a Factory Installed option and, cannot be field installed.

Printer Memory gives the B 9242-1 and B 9243-1 Line Printers the ability to be used with the B 9947 Dual Printer Control option to enable two line printers on one I/O Channel and control.

Figure 7-41. B 9245 Line Printer

B 9244-1 TAPE LISTER

The B 9244-1 Tape Lister (figure 7-42) is an electromechanical, buffered, drum-type printer with six separate print units. The normal operating speed of this lister is 1565 LPM. The B 9244-1 can operate as a separate unit with a B 2500 or B 3500 System, or it can have either one or two B 9244-2 six-tape slave units attached.

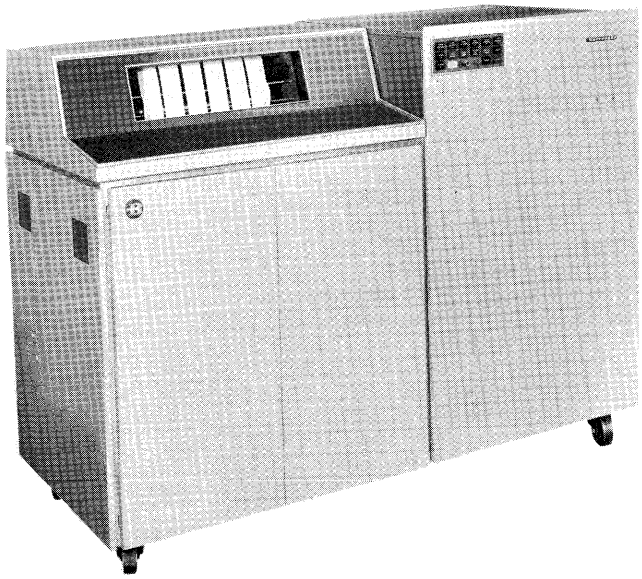


Figure 7-42. B 9244-1 Tape Lister

Functional Description

The B 9244-1 Tape Lister accepts binary coded decimal, alphanumeric information in parallel-by-bit, serial-by-character mode and stores the data in a 44-position buffer. Upon the completion of buffer loading and paper movement, the characters in the buffer are printed. When invalid characters are received, the scan cycle will continue for a complete drum revolution. The numeric print rate will be reduced to the rated alphanumeric speed of 800 LPM for the print line with the invalid character. Also, the invalid character will cause a blank in the particular column.

Character spacing is 10 to the inch; line spacing is 6 to the inch. All forms are adding machine type without margin-hole strips. The forms may be single part or two part with carbon-backed or plastic-backed first sheet. If single-part forms are used, the form can be exited from the machine through either the top tear strip opening or the rear exit opening, as required by the operator. Forms exited from the rear opening can be torn off or fan folded. Single part forms that exit from the top tear strip opening cannot be fan-folded or re-stacked. Restacking of forms in the fan-fold condition can only be accomplished with forms that are exited through the rear opening. If two-part forms are used, both can be exited from the machine as a non-decollated unit through either the top tear strip opening or the rear exit. The carbon copy from the rear exit can be restacked in fan-folds. The stacker has a capacity of 1000 feet (minimum) of single-part, fan-folded forms.

To maintain a printing rate of 1565 lines-per-minute, only 16 characters may be used. They are:

0-9

, (Comma)

. (Decimal)

x (Pocket X)

y (Pocket Y)

R (Reject)

* (Asterisk)

To process the full alpha-character set, a printing rate of 600 lines-per-minute is established. There are a total of 40 printable characters. They are:

0-9

, (Comma)

. (Decimal)

A thru Z

- (Hyphen)

* (Asterisk)

When the B 9244-1 is connected to either one or two B 9244-2 slave units, it can operate in either of two modes: normal (two-tape mode) or multiprocessing (three-tape mode). In the normal mode, two tapes maximum can be simultaneously printed by one command from the central processor. When in the multiprocessing mode, the lister simultaneously prints three tapes: the master, the detail tape, and the multiprocessing tape.

The master and detail tapes print identical information from buffer positions 1 through 22. The multiprocessing tape prints information from buffer positions 23 through 44.

A master-tape-selector switch with seven positions, N and 1 through 6, is used to select the tape, 1 through 6, on which the master information in buffer positions 1-22 is printed. The N position suppresses print of master information. The master information is printed on the master unit only of an 18-tape lister configuration. The central processor designates the detail tape which may be any of the 18 tapes not otherwise assigned. If the central processor supplies a detailed designation of N=2-6, which equals the master-tape-selector switch setting, detailed action is diverted to tape 1. This diversion always occurs whether or not a master unit designation was supplied by the external control.

Control Panel

The tape lister control panel (figure 7-43) contains operating switches and indicators. The control panel is located on the front of the unit, to the right of the print section. In addition, several switches are provided at the rear of the unit (figure 7-44) for operator convenience. The function of the switches and indicators is provided in table 7-13

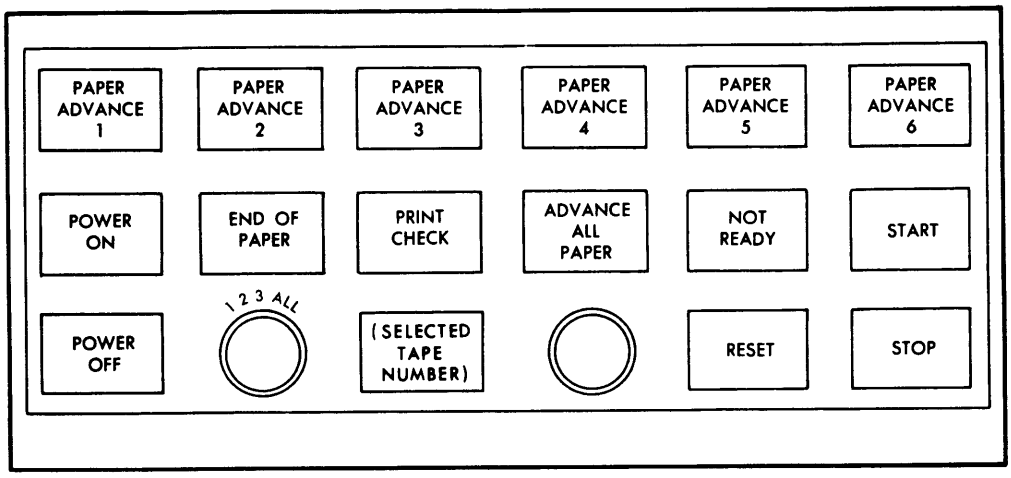


Figure 7-43. B 9244-1 Tape Lister Control Panel

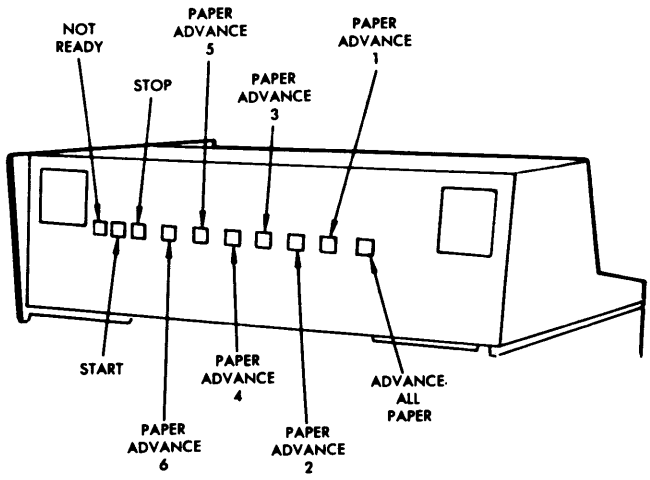


Figure 7-44. B 9244-1 Rear Control Panel

Table 7-13

B 9244-1 Tape Lister Control Panel Switches and Indicators

Switch/Indicator	Function
PAPER ADVANCE 1 through PAPER ADVANCE 6	Pressing these switches will cause the corresponding tape to be advanced, until the switch is released, when in the Not Ready condition. Duplicate switches are located at the rear of the unit.
POWER ON	Pressing this switch applies power to the unit.
END OF PAPER	This indicator will light when one of the subunits is almost out of forms or if a feeding problem exists. If this condition is sensed during a Skip or Print instruction, the result descriptor will have the end-of-paper bit set. The condition causing the indicator to light must be corrected and the RESET and START switches pressed.

Table 7-13 (cont)

B 9244-1 Tape Lister Control Panel Switches and Indicators

Switch/Indicator	Function
PRINT CHECK	This indicator will light when a print check error is sensed in any print position or if the drum is not synchronized with the drum position counter. A signal is sent to the I/O control and the appropriate bit is set in the result descriptor.
ADVANCE ALL PAPER	When in a Not Ready condition, pressing this switch causes all paper to be advanced until the switch is released. A duplicate switch is located at the rear of the unit.
NOT READY	This indicator will light if one of the following conditions exists: START switch not pressed, paper slews for more than one second, end-of-paper condition exists, or paper tears within the unit. A duplicate indicator is located at the rear of the unit.
START	Pressing this switch conditions the lister to accept instructions from the I/O control. A duplicate switch is located at the rear of the unit.
STOP	Pressing this switch places the unit in the Not Ready state. If a lister instruction is being executed when the switch is pressed, the instruction will be completed before the unit halts. Upon encountering the next instruction, the I/O control will return a result descriptor with the Not Ready bit set ON. This switch also appears at the rear of the unit.
RESET	Pressing this switch with the unit in the Ready state resets the print check circuitry and extinguishes the PRINT CHECK indicator. With the lister in the Not Ready state, pressing the switch clears all error circuitry except NOT READY. The START switch must be pressed to clear this indicator.
POWER OFF	Pressing this switch removes power from the unit.
(MASTER SELECTION SWITCH)	This is a seven-position rotary switch, which is located to the left of the RESET switch, and is used for the selection of one of the six subunits as the master tape. The switch positions (1 through 6 and N) are designated by use of a sphericular tube to the left of the switch. When in the N position, the switch is disabled.
(SELECTED TAPE NUMBER)	This indicator designates which of the six tapes is selected as the master tape by the MASTER SELECTION switch.
(LISTER DESIGNATE)	This four-position switch, which is located between the selected-tape-number indicator and the POWER OFF switch, is used to select the master unit (1 position), slave 1 (2 position), slave 2 (3 position), or the master and two slaves (ALL position), for which the PAPER ADVANCE switches on the control panel are to be effective. This switch has no effect on the PAPER ADVANCE switches on the rear of the units.

MAGNETIC TAPE UNITS

Magnetic tape units that are used with B 2500 and B 3500 Systems are capable of reading, writing, erasing, backward and forward spacing, and rewinding magnetic tape under control of a magnetic tape peripheral control. Two basic types of tape units are available: free-standing units and clustered tape units.

Clustered tape units share various electronic and electromechanical components, such as power supplies and vacuum motors, whereas free-standing tape units do not. All tape units are available with

either 7- or 9-track capability (i.e., they can accommodate magnetic tape which has seven or nine tracks across the width of standard ½-inch magnetic tape).

In addition to the flexibility of handling both 7- and 9-track tapes, certain B 2500 and B 3500 tape units can also handle either NRZI- (Non-Return to Zero, flux change on one) or phase-coded tapes. NRZI-encoded tapes have, at most, one flux change per bit position, whereas phase-encoded tapes have up to two flux changes per bit position. Phase-encoded tapes have the resultant advantage of being assured of at least one flux change per bit position. This certainty permits considerably higher packing densities and reduces the possibility of incurring failures as a result of skew, drop-outs, and low read-signal amplitude.

Types of Tape Units

B 2500 and B 3500 tape units are available in a wide variety of packing densities, speeds, and transfer rates. Direct-recorded tapes include packing densities of up to 800 BPI; phase-encoded tapes are specified at 1600 BPI. Provision has been made for accommodating both 800 and 1600 BPI on some tape units in order to facilitate the transition from the older, direct-recorded tapes to the new phase-encoded tapes. The available capabilities are shown in table 7-14.

Functional Characteristics

Table 7-14, lists the various combinations of packing densities and speeds that are available on B 2500 and B 3500 tape units.

Both free-standing and clustered tape units are capable of reading tape in the backward direction. This ability increases the efficiency of magnetic tape sorting, as well as offering increased efficiency of user programs which use magnetic tape. The various tape units can accept either 7-channel or 9-channel tapes (as a field modification), thereby facilitating the modernization of existing 7-channel tape libraries. Similarly, the various cluster tape units can accept either direct or phase-encoded tapes, thereby providing the flexibility of operating in any operational environment.

If a descriptor is not sent to the I/O soon enough, the tape unit will stop with the read/write head centered in the interrecord gap, ready to read or write the next record or block.

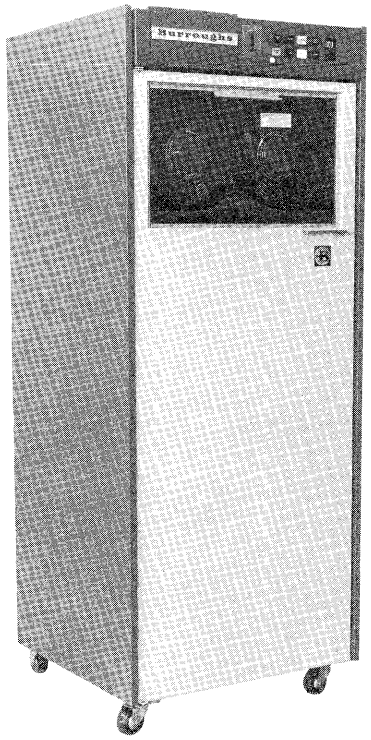


Figure 7-45. Free-Standing Magnetic Tape Unit

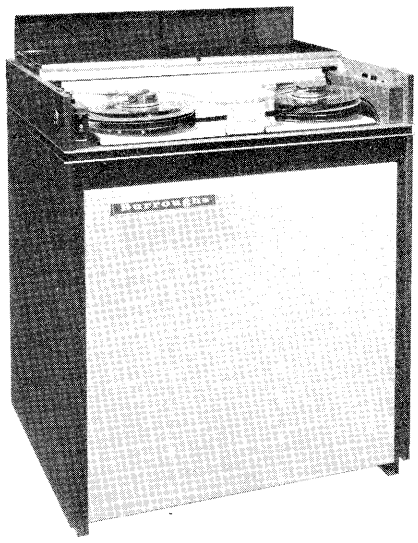


Figure 7-46. Clustered Tape Unit

Tape reels on both types of tape units have a groove on the rear face which accommodates a write ring to enable writing on the tape. Lack of a write ring prevents any writing or erasing operations on the tape reel. The presence of a write ring is indicated by the WRITE RING indicator on the control panel.

Table 7-14

Magnetic Tape Control Characteristics

Type	Channels	Speed (IPS)	Density (BPI)	Transfer Rate (KC)
Clustered				
B 9381	7	45	200/556/800	9/25/36
B 9381	9	45	200/800	9/36
B 9382	7	45	200/556/800	9/25/36
B 9382	9	45	1600	72
B 9382	9	45	200/1600	9/72
B 9382	9	45	800/1600	36/72
Free-Standing				
B 9390	7	90	200/556	18/50
B 9391	7	90	200/556/800	18/50/72
B 9392	9	90	200/800	18/72
B 9393-1	9	90	1600	144
B 9393-2	9	90	1600	192
B 9393-3	9	90	1600	240
B 9394-1	7	120	200/556/800	24/66/96
B 9394-2	9	120	800	96

Physical Characteristics of Free-Standing Tape Units

Free-standing tape units contain the components necessary to spool tape off of a supply reel of tape onto a take-up reel while writing data on the tape or reading data that has been previously recorded. Provisions also exist for rewinding the tape onto the supply reel at high speeds. Normal drive speed is 90 inches per second; rewind speed is an average of 300 inches per second. Figure 7-47 provides an illustration of a free-standing tape unit transport. The take-up reel is on the left side of the unit and the supply reel is on the right. In response to a forward-drive operation, tape is driven from the supply reel to the take-up reel. In response to a reverse-drive operation, the opposite is true.

Tape drive is accomplished through the combined action of constantly rotating capstan rollers and pinch rollers (see figure 7-48). On command, a pinch roller engages tape against a capstan to produce the drive action. One capstan roller is used for forward drive; the other for backward drive. Vacuum columns are used to buffer or separate the heavy reels and reel drive system from the low-inertia tape and tape drive system, thus permitting fast acceleration. During rewind, tape drive is accomplished by use of the reel motors rather than the capstan rollers that are used during the normal drive.

Free-Standing Tape Unit Control Panel

The local switches and indicators for the free-standing magnetic tape units are located on a control panel at the front top of the unit (see figure 7-49). The functions of these switches and indicators are provided in table 7-15.

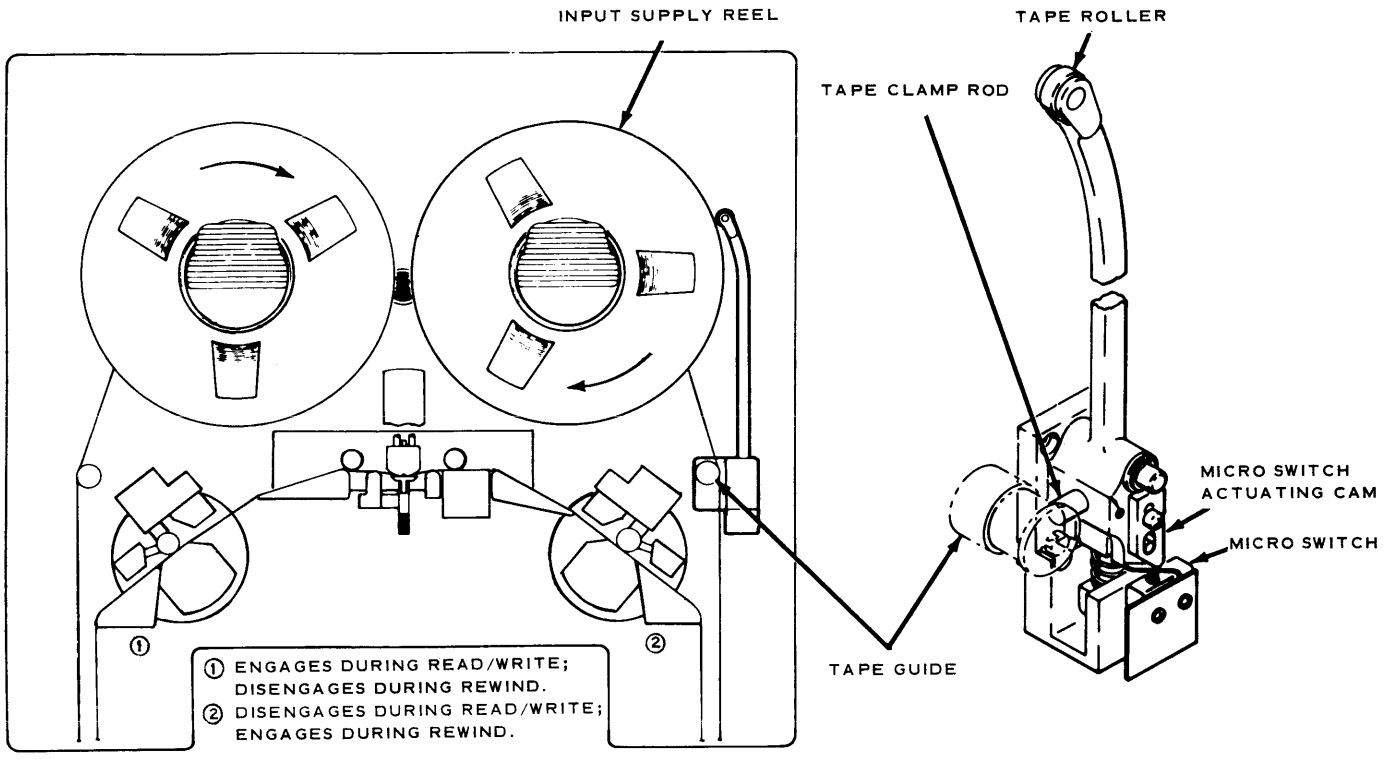


Figure 7-47. Free-Standing Magnetic Tape Unit Transport

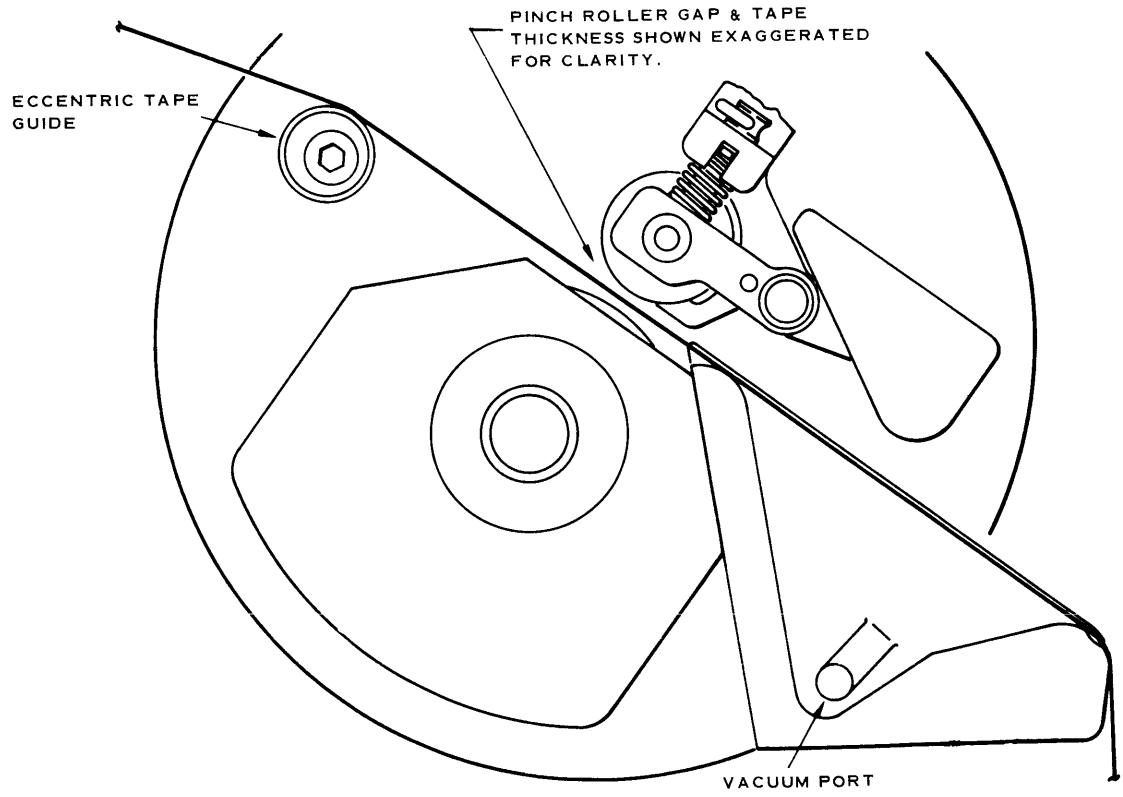


Figure 7-48. Expanded View of Right-Hand Tape Guide Drive Module

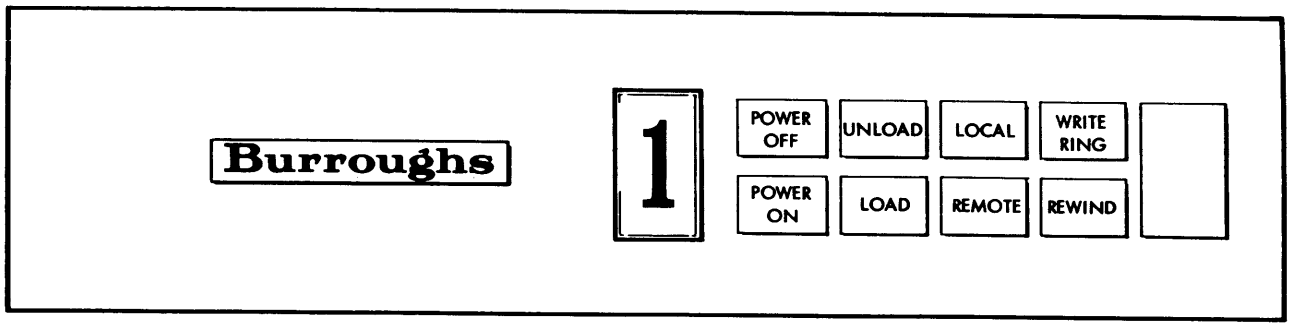


Figure 7-49. Free-Standing Magnetic Tape Unit Control Panel

Table 7-15
Free-Standing Magnetic Tape Unit Switches and Indicators

Switch/Indicator	Function
POWER OFF	Removes power from the tape unit.
UNLOAD	Positions tape to the point where the latch leader is on the supply reel side of the tape latch, thereby permitting the operator to unload the tape. This is only active in the Local mode.
LOCAL	Removes the tape unit from control of the B 2500 or B 3500 System. The switch lights when pressed.
WRITE RING	Signals that the supply reel has a write ring installed and that writing can be performed on the tape.
REWIND	Rewinds the tape to the beginning-of-tape mark. Rewind speed is approximately 300 inches per second. The switch is only active when the unit is in the Local mode.
REMOTE	Places the tape unit under control of the B 2500 or B 3500 System. The switch lights when pressed and the LOCAL indicator goes out.
LOAD	Causes tape to be drawn into the vacuum columns and moves the tape so that the beginning-of-tape is at the read/write head. This switch is only active in the Local mode.
POWER ON	Applies power to the unit. The switch lights when pressed.
(UNIT DESIGNATOR)	This switch-indicator permits operator selection of unit designation from 0 to 9; it is located to the left of the POWER ON and POWER OFF switches.
(DENSITY SELECTOR)	This switch allows the operator to select the desired density: 200, 556, or 800 BPI; it is located to the right of the WRITE RING and REWIND switches.

Free-Standing Tape Unit Operating Instructions

Procedures for loading and unloading tapes on free-standing magnetic tape units are described in the following paragraphs.

LOAD PROCEDURE

Proceed as follows:

a. Press the POWER ON switch (if power is not on).

b. Open the tape compartment window, thus placing the tape unit in a Standby condition. The take-up reel leader is held by the tape clamp when there is no supply reel present on the tape unit.

c. If a supply reel is present, push the tape clamp arm to the right to clamp the take-up reel leader to preclude its dropping into the vacuum column.

d. Place the input tape supply reel on the right-hand reel hub. This is accomplished by pulling out on the reel hub latch and placing the reel on the reel hub.

e. Lock the reel on the reel hub by pushing in on the reel hub latch.

f. Attach the permanent female leader latch of the take-up reel to the male latch leader of the supply reel.

g. Release the tape clamp by moving the tape clamp arm to the left.

h. Close the tape compartment window.

i. Press the LOAD button and wait for the tape to stop moving.

j. Press the REMOTE button, thus allowing the Master Control Program to direct further tape unit action.

UNLOAD PROCEDURE

Proceed as follows:

a. Press the LOCAL switch.

b. Press the UNLOAD switch and wait for the tape to stop at the unload point.

c. Open the tape compartment window.

d. Move the tape clamp arm to the right.

e. Separate the male and female latch leaders.

f. Remove the tape reel from the reel hub by pulling out on the reel hub latch.

TAPE LEADERS

The tape reels are placed on the right hand reel hub so that the tape will unwind when rotated in a clockwise direction. There must be a male latch leader on the physical beginning of each input tape or scratch tape. The take-up reel is mounted on the left reel hub and must have a female latch leader receiver at the physical beginning of tape. The take-up receiving leader is wound around the take-up reel and threaded through the tape unit as shown in figures 7-47 and 7-48.

Physical Characteristics of Clustered Units

A clustered unit can contain the components necessary to perform any two magnetic tape operations simultaneously on any two of the four available tapes. It is then possible to read and write on any two tapes concurrently. All four stations may rewind tape at the same time. Normal drive speed is 45 inches per second. The take-up reels are located below the feed reels in each station. Latch receivers protrude from slots on the left side of each station (as accessed). As on the free-standing units, tape drive is accomplished via the combined action of a capstan roller and a pinch roller. Each station has its own drive mechanism, but the stations share read/write electronics, power, drive source, and information paths. The clustered tape unit incorporates a minimum number of switches and indicators. An indicator (one for each tape station) on one of the tape stations lights when that station is operative (tape away from the rewound point).

A magnetic tape cluster may be either a master unit which is connected directly to an external control unit, or a slave unit which is connected to a master cluster unit. When only a master cluster is used, up to four tape stations can be active; use of the master-slave combination permits up to six tape stations. A station-designate switch is optionally provided on master-slave combinations with up to eight active stations.

Operating times for the magnetic tape cluster are as follows:

a. Start time – 5 milliseconds.

b. Stop time – 3.5 milliseconds.

c. Tape reversal time – 3.2 milliseconds.

d. Full reel rewind time – 4.5 minutes.

e. Start distance – 0.3 inch.

f. Stop distance – 0.1 inch.

In order to determine start-time-to-rewind or stop-time-to-center-of-an-interrecord-gap, assume 0.6-inch gaps for 9-channel tape and 0.75-inch gaps for 7-channel tape.

Magnetic Tape Cluster Control Panel

The switches and indicators for the magnetic tape cluster units are located on a control panel at each tape station (see figure 7-50). Figure 7-51 shows an enlarged view of one tape station. The power ON and OFF switches are located on the front of the unit at the left-front tape station; the STATION (optional), DENSITY, and REWIND switches, and the indicator (tape station is being utilized when lit) are located at each station. The functions of these switches and indicators are provided in table 7-16

Table 7-16

Tape Cluster Switches and Indicators

Switch/Indicator	Function
STATION (optional)	This switch, if included, is used to designate the tape station associated with the switch. If the switch is not included, station designations are automatically made by the internal wiring.
DENSITY	This three-position switch is provided at each tape station and is used to select tape densities of either 200, 556, or 800 BPI for 7-track or 9-track; 200, 800, or 1600 BPI for NRZI (nonreturn to zero)/PE (phase encoded); or 200, 800, or 800 for NRZI only. All clusters attached to one control must have the same maximum density capability.
REWIND	This button is located under each individual station access door. Tape rewind occurs when the access door is closed after the REWIND button is pressed.
(TAPE-SELECTED INDICATOR)	This indicator is located at each tape station, to the left of the REWIND switch, and lights when the tape reels at that station are being utilized. The indicator lights during the first forward operation which moves the beginning-of-tape marker past the read heads. The indicator goes out if a backward operation, such as Rewind, moves the tape to a position such that the beginning-of-tape marker is sensed.
ON	This switch applies power to all active stations on the cluster and is located at the left-front tape station.
OFF	This switch removes power from all stations on the cluster and is located under the ON switch.
UNLOAD	When this switch is moved in the direction that the arrow is pointing, the tape automatically rewinds from the load point to the point at which the male and female leader latches are accessible; the UNLOAD switch then causes the tape clamp to clamp the tape. When moved in the direction opposite to that which the arrow is pointing, the tape clamp is released, allowing free tape movement.

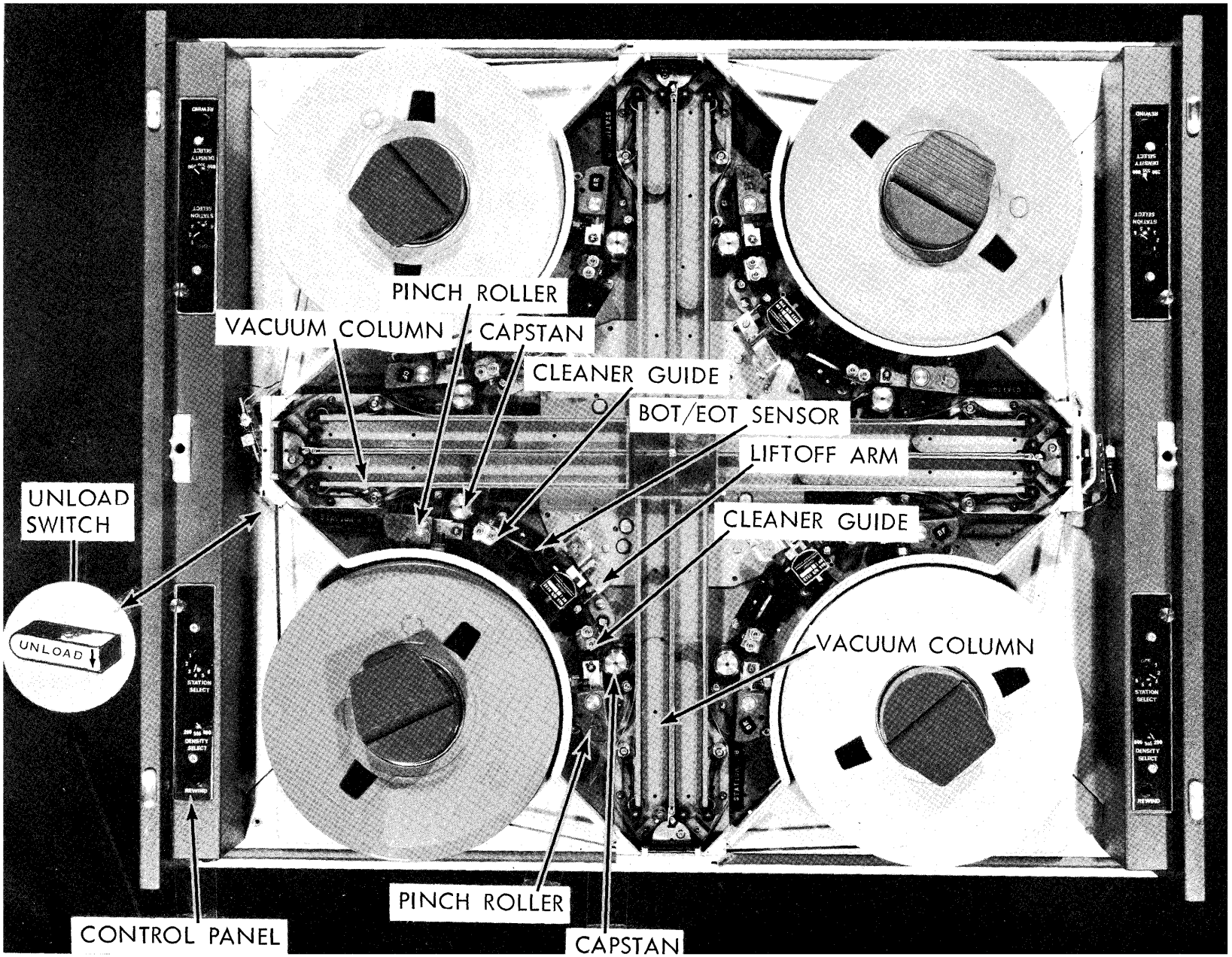


Figure 7-50. Magnetic Tape Cluster Control Panel

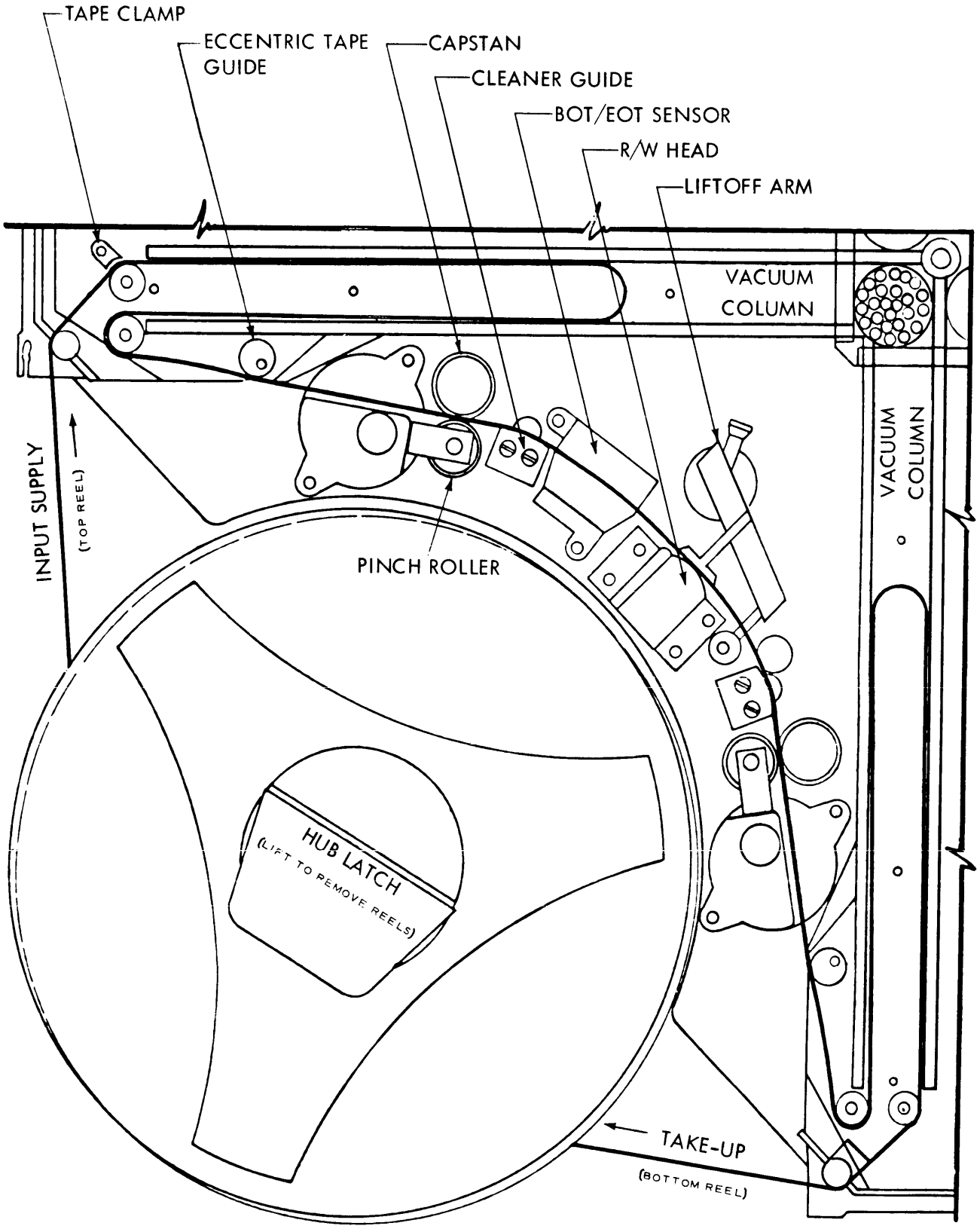


Figure 7-51. Magnetic Tape Cluster Tape Station, Left-Front View

Clustered Tape Unit Operating Instructions

Procedures for loading and unloading tapes on clustered magnetic tape units are described in the following paragraphs (see figures 7-50 and 7-51).

CAUTION

Do not press the REWIND switch unless absolutely sure that the tape is not already physically rewound. If adherence to this caution is ignored, possible servo damage might occur or the servo fuse might be blown.

LOAD PROCEDURE

Proceed as follows:

a. Lift the operator access cover. The tape transport station associated with the same cover is automatically set into a Not Ready condition. Operations of other stations having the covers closed are not affected.

NOTE

Do not lift the inner cover.

b. Mount the input supply tape on the reel hub by lifting the reel hub latch.

c. Push down on the reel hub latch to lock the tape reel to the reel hub.

d. Connect the tape latch leader (male) to the permanent take-up leader (female).

e. Move the UNLOAD switch in the direction opposite to that which the arrow is pointing.

f. Close the operator access cover, thus allowing the Master Control Program to direct further tape unit action.

The take-up reel can be considered an integral part of the hardware system and does not have to be accessible to the operator when the access door is opened. An operator can very simply gain access to the take-up reel if it becomes necessary to change the female latch leader, or to remove and replace unserviceable tapes.

UNLOAD PROCEDURE

Proceed as follows:

a. Lift the operator access cover.

NOTE

Do not lift the inner cover.

b. Move the UNLOAD switch in the direction that the arrow is pointing. This causes the tape to automatically rewind from the load point to the point at which the male and female leader latches are accessible, and then causes the tape clamp to stop tape movement. Allow the tape to come to a complete stop before proceeding.

c. Disconnect the tape from the take-up latch leader.

d. Lift the reel hub lock.

e. Remove the tape reel.

f. Push down on the reel hub lock.

g. Close the cover.

TAPE LEADERS

The female latch leaders should have the opening toward the center of the tape cluster rather than towards the outside. This will prevent the leaders from unlatching when they travel around the rollers in the vacuum columns.

Latch leaders should be checked weekly so that damaged or torn leaders can be replaced before they cause problems. Also, operators should be notified to check male leaders on tape reels for fold-over or tears. A torn, folded, or damaged latch leader will hang up, or separate, when used in the magnetic tape cluster.

Folded, creased, or torn tape leaders on the take-up reel should be replaced immediately. To produce a clear strip on the leader of standard magnetic tape, use Burroughs Platen Restorer on the oxide side of the tape. This will remove the oxide and binder, leaving the clear mylar. Be sure that the tape is dry before reinstalling it in the tape station.

The clear strip on the tape should be a minimum of 13 inches, starting approximately 11 inches from the end of the female latch leader.

Magnetic Tape

The magnetic tape used with B 2500 and B 3500 Systems is the standard 0.5-inch wide, polyester-based magnetic tape that has gained the computer industry's acceptance since 1955. It is available in 1200- or 2400-foot lengths on 8.5-inch reels. Tape used on direct-recorded tape units cannot be used on phase-encoded units and must be purchased expressly for phase-encoding operation. Both types of tape units include a latch receiver on the take-up reel. When the latch leader is connected to the latch receiver, the systems operator can initiate a load cycle on a free-standing unit which will automatically feed some of the tape from the supply reel onto the take-up reel. This leaves the tape in position for the execution of a Read or Write operation. The clustered tape unit does not include an automatic load cycle as on the free-standing unit. The first Read or Write command drives the tape to the proper operating point prior to execution of the operation.

Tape Format

The format of the data written on magnetic tape varies with the number of tracks on the tape and the type of recording used (direct or phase). Seven-track tape can only store frames consisting of six bits plus parity (64-character set); the minimum record length for 7-track tape is seven characters. Nine-track tape can store frames consisting of eight bits plus parity (256-character set); the minimum record length for 9-track tape is 18 characters. In addition, 9-track tape can also store two decimal digits per frame in cases where it is desirable to store only numeric data.

Nine-track tape can accommodate standard USASCII and EBCDIC formatted data. USASCII (United States of America Standard Code for Information Interchange) data conform to standards established by the American Standards Association in liaison with manufacturers and users of data processing equipment. EBCDIC (Extended Binary Coded Decimal Interchange Code) data conform to de facto standards established through past practice and precedent.

Write Rings

All magnetic tape reels for free-standing and clustered magnetic tape units have a groove on the rear face which accommodates a write ring to enable writing on the tape. Lack of a write ring will prevent Write or Erase operations on a reel of tape. On free-standing tape units, the presence of a write ring is indicated by the WRITE RING indicator being illuminated.

DISK FILE UNITS

Disk file units include two types of files (system memory and disk file) which are quite different in capacity, access time, and transfer rate. The disk files are completely compatible in addressing structure and segment size so that the Master Control Program is able to use either type of unit for memory and file storage.

The range of random storage is a minimum of one million bytes on system memory and a maximum of one billion bytes on a full disk file subsystem. The technique of a read/write head on each track provides an average access time of 17 milliseconds on system memory and from 20 to 40 milliseconds on the disk file system.

B 9370 System Memory

System memory (figure 7-52) is a single disk con-

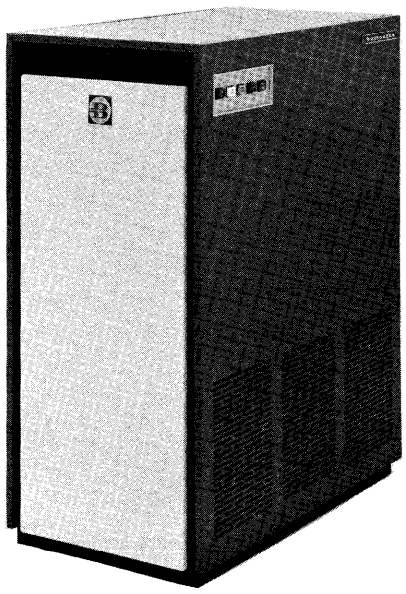


Figure 7-52. B 9370 System Memory

tained in a cabinet and connected to the system by a disk file control unit and a type B I/O channel. A second system memory can be attached to the system memory control through a 1 x 2 system memory exchange (B 2473 or B 3473) to provide system memory capacity of three or four million bytes of storage. An electronics unit is incorporated into the system memory module.

Characters are recorded in 8-bit form. For example, a 4-million byte file can also be used to contain 8-million, 4-bit digits.

System memory provides backup storage for the software system, but any area not used by the software may be used for general storage by the customer.

The system memory disk is capable of storing either one million or two million bytes of information (two million or four million digits, respectively). If the one-million byte capacity system memory disk is attached to the system, it can be increased to the two million byte capacity in the field. Data are stored serially by bit on a given segment on a given track and are transferred serially by byte. The specifications for the system memory disk are provided in table 7-17.

Table 7-17

System Memory Specifications

Description	Domestic Power 60 AC
Segment Length – Bytes	100
Segment Length – Digits	200
Tracks per Disk Face	100
Disk per System Memory	1
Segments per Disk Face	10,000
Bytes per Disk Face	1,000,000
Digits per Disk Face	2,000,000
Rotation Rate	1745 RPM
Access Time, Maximum	34 MS
Access Time, Average	17 MS
Data Transfer Rate, Maximum	303 KC

In addition to the 100 information bytes in each segment, an additional longitudinal parity byte is also written. The information on the disk is retained without regeneration during normal start-up and shut-down operations. If the disks are shut down completely, they must be turned on and rotated for a prescribed time prior to use. If an accidental loss of power occurs during a system memory Read operation, information on the disk is still retained. Disk information is considered destroyed if the power loss occurs during a system memory Write operation.

Assuming the dust-tight covers have not been removed, the unit is capable of performing all of its functions, including the reading of previously written data with no warm-up delay after a power turn-off condition if the turn-off time is less than 30 minutes. Where the power-off condition exceeds 30 minutes, the warm-up time required does not exceed the power-off time and in no case exceeds 1½ hours.

CONTROLS AND INDICATORS

For simplicity, there are very few controls and indicators on the system memory unit. They are:

a. Power ON – OFF.

b. LOCAL – REMOTE – MAINTENANCE Control.

The LOCAL-REMOTE-MAINTENANCE control is in a remote status unless the field engineering personnel are performing maintenance on the unit. System memory is in a Not Ready status when any of the following conditions exist:

a. Power is off.

b. The disk is not rotating at its prescribed speeds.

c. The air pressure used by the unit is below the minimum value specified.

d. A one-million character system memory is addressed beyond one million.

The causes of the Not Ready condition must be corrected before the unit can be used by the system.

CLOCK TRACKS

One spare clock track is provided. Clock tracks may not be copied or written in the field.

B 9371 Disk File Electronics Unit

This unit (figure 7-53) incorporates all of the electronics for attaching a maximum of 50 million bytes or 100 million digits in addressable segments of 100 bytes or 200 4-bit digits. Up to ten electronics units can be connected via an exchange to a single disk file control for a maximum capacity of 500 million bytes. The electronics unit contains the main air pressure system, starting controls, basic head switching logic, and read/write amplifiers for the five storage modules that can be connected to it.

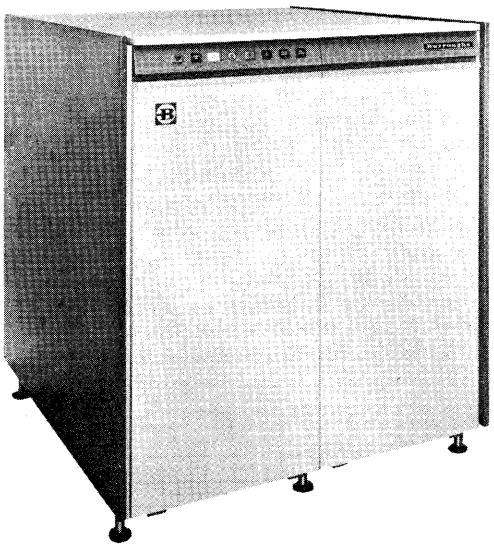


Figure 7-53. B 9371 Disk File Electronics Unit with One B 9372 Disk File Module Attached

A lockout switch is provided on the control panel to optionally prevent writing on any of the modules connected to the electronics unit. It is possible to read from the unit whenever it is placed in the Write Lockout state.

The switches and indicators for the B 9371 Disk File Electronics Unit are located on a control panel on the front of the unit, near the top. The functions of these switches and indicators are provided in table 7-18.

B 9372 Disk File Module

This unit (figure 7-53) contains four disks and has a capacity of 10 million bytes or 20 million 4-bit digits. From one to five of these units can be connected to a single B 9371 Disk File Electronics Unit. The disks have a read/write head for each track, providing an average access time of 20 milliseconds.

The specifications for the disk file modules are as follows:

a. Segment length – 100 bytes or 200 4-bit digits.

b. Segments per track – zone 1 (70), zone 2 (90), zone 3 (90).

c. Disks per unit – 4.

d. Rotation rate – 1500 RPM.

e. Maximum access time – 40 milliseconds.

f. Average access time – 20 milliseconds.

g. Maximum data transfer rate – 240 kilobytes/second.

h. Average data transfer rate – 200 kilobytes/second.

Disk File Exchanges

An exchange is a device (housed in memory cabinet backplane area or auxiliary cabinet) that allows a set, or sets, of electronics units and modules to be connected with from one to four disk file controls. The disk file exchanges included for the system are the 1 x 2 or 2 x N for the B 2500, and 1 x 2 or N_1 x N_2 up to 4 x 20 for the B 3500. An exchange is used on a system when more than one electronics unit and/or more than one disk file

Table 7-18
Disk File Control Panel Switches and Indicators

Switch/Indicator	Function
POWER ON	This switch supplies AC power to the electronics unit and to the module connected to it.
POWER OFF	This switch removes AC power from the electronics unit and from the module.
NOT READY	This indicator lights when one of the following conditions exists: AC power off, DC power off, all disks in the storage module are not up to speed, or air pressure is low.
DISK LOCKOUT	This indicator lights when one or more disk lockout switches (located under the hinged cover – one for each pair of disks) or the master lockout switch (under the hinged cover) is pressed.

control is attached to a system. For efficient allocation and use of random storage, an MCP-operated system uses an exchange after the first electronics unit regardless of the number controls used.

The first number of the exchange designation applies to the number of controls, and the second number refers to the number of electronics units. For example, a 4 x 10 exchange is for a maximum of four disk file controls and ten electronics units. In effect, the exchange provides the subsystem with floating I/O channels. For example, with a 4 x 10 exchange, it is possible to read or write the same segment or record from any one of four controls.

Disk file exchanges are described in more detail in section 6.

Disk File Control

The disk file control is the connecting link from the disk file system to the processor. The control is housed in the I/O cabinet and utilizes a type B I/O channel. Each control contains a small buffer to hold two bytes of data until it can be transferred to core memory on a Read command or to the module on a Write command. The control has other circuitry so that the disk file operation can be carried on without interfering with processor or other I/O operations, except for the memory cycle to transfer two bytes.

Disk file controls are discussed in more detail in section 6.

SECTION 8
DATA COMMUNICATIONS

GENERAL

This section describes the data communications network used with the B 2500/B 3500 Systems.

DATA COMMUNICATIONS CONTROL UNITS

The following data communications controls may be used on B 2500/B 3500 Systems:

a. Single-Line Control.

b. Multiline Control.

c. Terminal Unit Control.

These controls are described in the following paragraphs.

The single-line control and the multiline control are functionally equivalent, except that the single-line control services one communications line, whereas the multiline control services a number of communications lines on a time-shared basis.

The single-line control and the multiline control can be adapted to accommodate a variety of data sets and remote terminals. The following are representative of the remote terminals that may be used:

a. Touch-Tone* instrument on dialed lines (multiline only).

b. Another B 2500/B 3500 via dialed or leased lines.

c. B 9350 Typewriter on dialed, leased, or directly connected line.

d. A.T. & T. 8A1 Selective Calling Station (Model 35) on leased lines.

e. A.T. & T. 83B3 Selective Calling Station (Model 28) on leased lines.

f. Teletypewriter Model 33 or 35 on TWX network.

g. IBM 1050 on TWX, dialed, or leased lines.

h. IBM 1030 on leased or directly connected lines.

i. Univac DCT-2000 on dialed or leased lines.

j. Burroughs Input Display System on dialed, leased, or directly connected lines.

k. TC 500 or TC 700 on dial, leased, or directly connected.

l. B 300/B 500/B 5500 on dial or leased lines.

No translation is provided for any code by the controls. However, the Audio Line Adapter translates BCM code to an 8-bit EBCDIC code. Code translation is performed by tables stored in the MCP.

All controls include the capability to respond to a Read Address instruction from the processor by allowing the transfer of the contents of either word of its associated address memory to the processor. The invalid I/O descriptor bit of the processor is set ON in the event that the instruction is received by a busy channel. (A multiline channel is not considered busy after returning a channel result descriptor.)

Single-Line Control

A single-line control is an input/output control which provides a connection between a single I/O channel of the B 2500 or B 3500 and a single communications line. A line adapter is required to equip the single-line control for use with a particular type of remote I/O device. The adapter determines code sensitivity, transmission rate, and character length in bits. The single-line control uses one Type B I/O channel. The control communicates with the attached adapter serially by bit and with the B 2500 or B 3500 serially by character. All line adapters are field installable and field interchangeable. The types of adapters available are described later in this section. The single-line control occupies one large I/O channel position in a cabinet and has associated with it two words of processor address memory and the reserved memory area for one result descriptor. The control unit includes one character of data storage.

MODULARITY

One code adapter, one station parameter adapter, and one line adapter are required with the single-line control; one automatic calling unit adapter is optional. The Automatic Calling Unit (ACU) adapter, in conjunction with all switched line adapters, provides an automatic calling feature. ACU

*Registered Trade Mark of AT&T.

Adapter A is utilized with telephone systems which are capable of accepting dial digits immediately upon presentation of the tone signal to the ACU adapter (e.g., BELL). ACU Adapter B is used with telephone systems which require at most a one second delay (e.g., General Telephone).

Multiline Control

The multiline control is an input/output control which allows a number of communications lines to time share one I/O channel. A line adapter is required for each communications line. One multiline control with 36 subchannels can be connected to a B 3500 System. The multiline control physically occupies two contiguous large I/O channel positions in a cabinet but utilizes only the lower numbered channel which has associated with it two words of processor address memory and the reserved memory area for one result descriptor. In addition, each of the line adapters connected to the multiline control require two words of the address memory and a result descriptor area separate from those assigned to the multiline control. The result descriptor memory address for each line adapter is 000480 + 20N, where N = 1 . . . 36. The multiline control provides the following features:

a. A standard I/O control interface.

b. A basic capacity to accept up to four line adapters and associated automatic calling unit adapters and the facility to control up to a maximum of 36 communications line adapters. An Audio line adapter is permitted only on the multiline extension and may not be one of the basic four line adapters in the control. A maximum of 32 such adapters may be accumulated. Only three model 28 (83B3) adapters may be housed in a basic multiline control.

c. Time sharing of the control by all line adapters.

d. A basic 12-word scratch pad memory capable of being extended to 36 words. The scratch pad memory is used for holding control information and data associated with an attached line adapter.

e. A scanner for rapidly scanning line adapters to detect those requiring attention.

f. Capacity to accept up to eight code adapters.

g. Capacity to accept up to three station parameter adapters.

The control provides for the collection and distribution of characters, checking for code sensitivity and other control functions, according to the requirements of the specific Op Code stored in the scratch pad memory for the associated line adapter. The multiline control uses a standard 8-bit parallel data transfer to and from memory. When fewer than 8 data bits are received, the control sets the most significant bits to zero (except for shift codes) before storing in memory. When an adapter is performing a Read operation with time-out inhibited and data has not yet been received, the control appears Not Busy to the processor console.

MODULARITY

The basic multiline control accommodates from one to four adapters of any type, or mixture of types (except Audio line adapters and model 28 (83B3) as indicated. Up to four multiline extensions may be added to the system. Each extension has a capacity for eight additional line adapters of any type, or mixture of types (including Audio line adapters); however, the maximum number of line adapters is 36. The multiline extensions are located in a cabinet separate from the cabinet in which the multiline control is located.

The multiline control includes a scratch pad memory, consisting of 12 48-bit words. Up to two 12-word scratch pad extensions may be added, providing modular expandability to a maximum of 36 words. One word of scratch pad memory is required for each line adapter.

Two words of address memory are required for each line adapter. Address memory is assigned for multiline control use in increments of full 12-word address memory extensions. Use of an address memory extension cannot be shared between a multiline control and other I/O controls.

Station parameter adapters are provided in the multiline control on a plug-in basis; only one of a given type is required. Space is provided for up to three different types, providing the capability of handling 31 different types of line adapters.

Code adapters are also provided in the multiline control on a plug-in basis; only one of a given type is required. Remote devices utilizing the same control codes and functions may share the same code adapter. Space is provided for up to eight code adapters, each being capable of containing up to 10 control characters.

Automatic calling unit adapters may be used in conjunction with all switched line adapters to provide an automatic calling feature. The space provided for the line adapters includes room for an ACU adapter. ACU Adapter A is utilized with telephone systems which are capable of accepting dial digits immediately upon presentation of the first tone signal to the ACU adapter (e.g., BELL). ACU Adapter B is used with telephone systems which require at most a one second delay (e.g., General Telephone).

Up to four voice response extension adapters are provided in each multiline extension on a plug-in basis. One voice response extension adapter is required for each pair of voice (audio) line adapters desiring voice response.

All adapters, multiline extensions, and scratch pad extensions are field installable. Switched-leased line adapters can be field modified for either switched or leased line applications.

Line Adapters for Single-Line and Multiline Controls

The adapters are input/output devices that provide the terminal connections between a telephone or telegraph facility and an I/O channel via the single-line or multiline controls. The adapters operate in the half-duplex mode.

During input, all adapters receive data from the line serially by bit and serially by character. When a bit has been stored, the adapter signals the control to accept the bit. During output, all adapters receive data from the control serially by bit and serially by character. As each bit is transmitted, the adapter requests the next bit from the control.

The adapter provides information to the single-line or multiline control which defines the type of remote equipment attached. Such characteristics as character length, number of stop and start bits, type of transmission, synchronous or asynchronous, type of line control, type of error control, and control code sensitivity are supplied.

A time-out feature is provided in the control for each adapter to detect hardware and line malfunctions that could not otherwise be recognized. For switched lines only, a 5-second timer is started upon receipt of the descriptor. When data flow starts, the normal time-out associated with the adapter is employed. For all adapters, the normal timer commences upon receipt of the first bit of the first character for a read descriptor and immediately after switching to the read portion of a write-then-read descriptor. The timer is reset with the receipt of the first bit of each subsequent character. In the event of a time-out by an adapter, a result descriptor which signifies this condition is stored. The timer is stopped by the end of the operation or by a cancel descriptor. The inhibit time-out variant inhibits all time-outs.

Adapters (Burroughs model numbers in parentheses) to accommodate the following devices are available with the B 2500 and B 3500 Systems:

a. B 9350 Typewriter locally (B 2651 or B 3651).

b. TWX station or B 9350 Typewriter remotely (B 2652-1 or B 3652-1).

c. TWX station or B 9350 Typewriter remotely with automatic dial out (B 2652-2 or B 3652-2).

d. Another B 2500 or B 3500 (B 2653-1 or B 3653-1).

e. Another B 2500 or B 3500 with automatic dial out (B 2653-2 or B 3653-2).

f. IBM 1050 (B 2655-1 or B 3655-1).

g. IBM 1050 with automatic dial out (B 2655-2 or B 3655-2).

h. Western Electric (WE) Model 35 Teletypewriter on 8A1 Selective Calling Station (B 2657 or B 3657).

i. Burroughs Input and Display System (B 9351):

   1) Direct connect (B 2659 or B 3659-1).

   2) Data set asynchronous (B 2659-2 or B 3659-2).

   3) Data set synchronous (B 2659-3 or B 3659-3).

   4) Data set asynchronous with automatic dial out (B 2659-4 or B 3659-4).

   5) Data set synchronous with automatic dial out (B 2659-5 or B 3659-5).

j. Univac DCT-2000 (B 2654-1 or B 3654-1).

k. IBM 1030 (B 2656-1 or B 3656-1).

l. 83B3 Model 28 Teletypewriter (B 2662 or B 3662).

m. Audio response (B 2663 or B 3663).

n. TC 500/TC 700:

1) Direct connect (B 2664-1 or B 3664-1).

2) Data set asynchronous (B 2664-2 or B 3664-2).

o. B 300/B 500/B 5500:

1) Data set synchronous (B 2653-3 or B 3663-3).

2) Data set synchronous with automatic dial out (B 2653-4 or B 3653-4).

p. Burroughs Input and Display System (B 9352):

1) Direct connect (B 2659-8 or B 3659-8).

2) Data set asynchronous (B 2659-9 or B 3659-9).

3) Data set synchronous (B 2659-10 or B 3659-10).

4) Data set asynchronous with automatic dial out (B 2659-11 or B 3659-11).

5) Data set synchronous with automatic dial out (B 2659-12 or B 3659-12).

These adapters are described in the following paragraphs. It should be noted that some line adapters come in more than one of the following versions:

a. Switched line.

b. Leased line.

c. Direct.

LOCAL B 9350 TYPEWRITER ADAPTER (B 2651 or B 3651)

This adapter provides connection to a B 9350 typewriter station locally. The station must be located within one mile of the B 2500 or B 3500 if it is connected directly. The B 2651 or B 3651 has the following specifications:

a. Character length – 8 bits.

b. Stop bit – 2 bits.

c. Start bit – 1 bit.

d. Signaling speed – 110 BPS.

e. Data set – none on direct connection.

f. Code – ASCII X3.4-1963.

g. Clock – asynchronous.

h. Time-out – 20 seconds.

i. Bit sequence – least significant bit first.

j. Longitudinal parity – none.

REMOTE TWX STATION/B 9350 TYPEWRITER ADAPTERS (B 2652-1 or B 3652-1)

These adapters provide connections to Model 33 or 35 Teletypewriters on the teletypewriter exchange (TWX) network via the WE 811B Data Set with regeneration, or the B 9350 on dial lines via WE 103A Data Set. When the B 9350 is used on dial lines with a WE 103A, Teletype Coupler No. 198420 is required. The break (input and output) and automatic dial-out features may also be incorporated. The adapter has the following specifications:

a. Character length – 8 bits.

b. Stop bit – 2 bits.

c. Start bit – 1 bit.

d. Signaling speed – 110 BPS.

e. Data set – WE 811B with data unit 6B1 or WE 103A on dial lines (DDD).

f. Code – USASCII-1963A.

g. Station parameter adapter-A – asynchronous.

h. Time-out – 20 seconds.

i. Bit sequence – least significant bit first.

j. Longitudinal parity – none.

REMOTE TWX STATION/B 9350 TYPEWRITER ADAPTER WITH AUTOMATIC DIAL OUT (B 2652-2 or B 3652-2).

This adapter has the same characteristics as the B 2652-1 or the B 3652-1, except that an auxiliary data set (801A) is used in conjunction with the 103A data set.

ANOTHER B 2500 OR B 3500 ADAPTER (B 2653-1 OR B 3653-1)

This switched-leased line adapter provides for interconnection of B 2500 or B 3500 computers over dialed lines or leased lines. The B 2500/B 3500 to B 2500/B 3500 adapter has the following specifications:

a. Character length – 8 bits plus 1 parity.

b. Signaling speed – 2000 BPS on dial lines; 2400 BPS on leased lines.

c. Data set – WE 201A3 on dial lines (DDD); WE 201B1 on leased lines.

d. Code – EBCDIC 8-bit.

e. Time-out – 1 second.

f. Clock – synchronous (provided by data set).

g. Bit sequence – least significant bit first.

h. Longitudinal parity – even on 8 bits (odd vertical Parity on LPC).

B 2500/B 3500 ADAPTER WITH AUTOMATIC DIAL OUT (B 2652-2 or B 3652-2).

This adapter has the same characteristics as the B 2652-1 or the B 3652-1, except that an auxiliary data set (801A) is used in conjunction with the 201A data set.

IBM 1050 ADAPTER (B 2655-1 OR B 3655-1)

The switch-leased line adapter provides connection to an IBM 1050 on a TWX network or dial lines, on leased lines, or direct lines. The IBM 1050 System is a group of slow-speed devices which can transmit data to, or receive data from, another 1050 System or a computer. Data are transmitted at 14.8 characters per second in a half-duplex mode. The 1050 System permits transmission of data, back and forth, using punched cards, punched paper tape, printer and keyboard. A 1050 System at one location consists of a 1051 Control Unit and one or more of the following:

a. 1052 Printer Keyboard.

b. 1053 Printer.

c. 1054 Paper Tape Reader.

d. 1055 Paper Tape Punch.

e. 1056 Card Reader.

f. 1057 card punch (similar to an 024).

g. 1058 printing card punch (similar to an 026).

h. 1092 programed keyboard.

i. 1093 programed keyboard.

The adapter for the IBM 1050 system has the following specifications:

a. Character length – 6 bits plus 1 parity.

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signaling speed – 133.2 BPS.

e. Data set – WE 103A on TWX or dial; WE 103F on scheduled 4 leased lines.

f. Code – IBM perforated tape and transmission code for 6 bits (PTTC-6).

g. Time-out – 20 seconds.

h. Bit sequence – most significant bit first.

i. Clock – asynchronous.

j. Longitudinal parity – even on all 7 bits.

IBM 1050 ADAPTER WITH AUTOMATIC DIAL OUT (B 2655-2 or B 3655-2)

This adapter has the same characteristics as the B 2655-1 or B 3655-1, except that an auxiliary data set (801A) is used in conjunction with the 103 data set.

WESTERN ELECTRIC (WE) MODEL 35 TELETYPEWRITER ON 8A1 SELECTIVE CALLING STATION ADAPTER (B 2657 or B 3657)

This leased-line provides connection to WE Model 35 Teletypewriter equipped for selective calling on leased lines. The 8A1 system is a multi-station, leased line, narrow band, polling system which allows up to 400 stations. In practice, it would be unusual to have 400 stations on a single net because it could possibly create long message traffic overloads. However, the large number of calling codes for 400 stations becomes quite useful. For instance, if 50 calling stations were on a net, each of these stations could utilize several different calling codes. According to its calling code, a station is or is not included in a party line call. The 8A1 Selective Calling System adapter has the following specifications:

a. Character length – 7 bits plus 1 parity.

b. Stop bit – 2 bits.

c. Start bit – 1 bit.

d. Signaling speed – 110 BPS.

e. Data auxiliary set – WE 816A on schedule 3A leased lines.

f. Code – ASCII X3.4-1963.

g. Time-out – 5 seconds for paper tape; 25 seconds for keyboard. Selection determined by control code.

h. Clock – asynchronous.

i. Bit sequence – least significant bit first.

j. Longitudinal parity – none.

BURROUGHS INPUT DISPLAY SYSTEM (B 9351) DIRECT ADAPTER (B 2659-1 OR B 3659-1)

This adapter provides connection between the B 2500 and B 3500 Systems and the Burroughs Input Display System. The Burroughs Input Display System-direct adapter has the following specifications:

a. Character length – 7 bits plus 1 parity (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signaling speed – 1200 or 2400 BPS.

e. Data set – none.

f. Line connection – 2-wire direct (max. length 1000 feet).

g. Code – USASCII X3.4-1967.

h. Clock – asynchronous.

i. Bit sequence – least significant bit first.

j. Time-out – 1 second.

k. Longitudinal parity – even.

BURROUGHS INPUT DISPLAY SYSTEM (B 9351) ASYNCHRONOUS ADAPTER (B 2659-2 OR B 3659-2)

The specifications for this adapter are as follows:

a. Character length – 7 bits plus 1 parity (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signaling speed – 1200 BPS.

e. Break feature – input and output on dial or 4-wire

f. Data set – WE 202C on dial lines; WE 202D on scheduled 4A lines.

g. Code – USASCII – X3.4-1967.

h. Clock – asynchronous.

i. Time-out – 1 second.

j. Bit sequence – least significant bit first.

k. Longitudinal parity – even on 7 bits (even vertical parity on LPC).

The longitudinal parity character is generated over all characters following the STX or SOH characters and follows the ETX character in the transmission.

BURROUGHS INPUT DISPLAY SYSTEM-SYNCHRONOUS ADAPTER (B 2659-3/3659-3)

The specifications for this adapter are as follows:

a. Character length – 7 data plus 1 parity (odd).

b. Signaling speed – 2000 BPS on dial lines; 2400 BPS on leased lines.

c. Break feature – input and output on dial or 4-wire lease.

d. Data set – WE 201A3 on dial lines; WE 201B1 on schedule 4C leased lines.

e. Code – USASCII-1967D.

f. Clock - synchronous (provided by data set).

g. Time-out – 1 second.

h. Bit sequence – least significant bit first.

i. Longitudinal parity – even on 7 bits (odd vertical parity on LPC).

The longitudinal parity character is generated over all characters following the STX or SOH characters and follows the ETX character in the transmission.

BURROUGHS INPUT AND DISPLAY SYSTEM (B 9352) DIRECT ADAPTER (B 2659-8 OR B 3659-8).

a. Character length – 7 bits plus 1 parity (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signal speed – 2400 or 1200 BPS.

e. Line connection – 2 wire direct (max. length of 1000 feet).

f. Code – USASCII X3.4-1967.

g. Clock – asynchronous.

h. Bit sequence – least significant bit first.

i. Time-out – 1 second.

j. Longitudinal parity – even.

BURROUGHS INPUT AND DISPLAY SYSTEM (B 9352) ASYNCHRONOUS ADAPTER (B 2659-9 OR B 3659-9)

The specifications for this adapter are as follows:

a. Character length – 7 data bits plus 1 parity (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signal speed – 1200 BPS.

e. Break feature – input and output on dial or 4 wire leased lines.

f. Data set – WE 202C on dial lines; WE 202D on schedule 4A lines.

g. Code – USASCII X3.4-1967.

h. Clock – asynchronous.

i. Time-out – 1 second.

j. Bit sequence – least significant bit first.

k. Longitudinal parity – even on 7 bits (even vertical parity on LPC).

The longitudinal parity character (LPC) is generated over all characters following the STX or SOLT characters and follows the ETX character in the transmission.

BURROUGHS INPUT AND DISPLAY SYSTEM (B 9352) SYNCHRONOUS ADAPTER (B 2659-10 OR B 3659-10).

The specifications for this adapter are as follows:

a. Character length - 7 data bits plus 1 parity bit (odd).

b. Signal speed – 2000 BPS on dial lines; 2400 on leased lines.

c. Break feature – input and output on dial or 4 wire lines.

d. Data set - WE 201A3 on dial lines; WE 201B1 on schedule 4C leased lines

e. Code – USASCII X3.4-1967.

f. Clock – synchronous (provided by data set).

g. Time-out – 1 second.

h. Bit sequence – least significant bit first.

i. Longitudinal parity – add on 7 bits (odd vertical parity on LPC).

The longitudinal parity character (LPC) is generated over all characters following SOLT or STX characters and follows the ETX character in the transmission.

BURROUGHS INPUT AND DISPLAY SYSTEM (B 9352) ASYNCHRONOUS WITH AUTOMATIC DIAL OUT (B 2659-11 OR B 3659-11)

This adapter has the same characteristics as the B 2659-9 or the B 3659-9, except that an auxiliary data set (801A) is used in conjunction with the 202C data set.

BURROUGHS INPUT AND DISPLAY SYSTEM (B 9352 SYNCHRONOUS WITH AUTOMATIC DIAL OUT (B 2659-12 OR B 3659-12)

This adapter has the same characteristics as the B 2659-10 or the B 3659-10, except that an auxiliary data set (801A) is used in conjunction with the 201A data set.

TC 500 TERMINAL COMPUTER DIRECT ADAPTER (B 2664-1 OR B 3664-1)

This adapter has the following characteristics:

a. Character length – 7 bits plus 1 parity bit (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signal speed – 1200 BPS.

e. Line connection – 2 wire direct (maximum of 1000 feet in length).

f. Code – USASCII X3.4-1967.

g. Clock – asynchronous.

h. Bit sequence – least significant bit first.

i. Time-out – 1 second.

j. Longitudinal parity – even.

TC 500 TERMINAL COMPUTER ASYNCHRONOUS ADAPTER (B 2664-2 OR B 3664-2)

This adapter has the following characteristics:

a. Character length – 7 bits plus 1 parity (even).

b. Stop bit – 1 bit.

c. Start bit – 1 bit.

d. Signal speed – 1200 BPS.

e. Data set – WE 202C on dial lines; WE 202D on schedule 4A lines.

f. Code – USASCII X3.4-1967.

g. Clock – asynchronous.

h. Time-out – 1 second.

i. Bit sequence – least significant bit first.

j. Longitudinal parity – even on 7 bits (even vertical parity on LPC).

The longitudinal parity check (LPC) is generated over all characters following the SOH or STX character and follows the ETX character in the transmission.

B 300/B 500/B 5500 ADAPTER
(B 2653-3 OR B 3653-3)

This adapter has the following characteristics:

a. Character length – 7 bits plus 1 parity (odd).

b. Signal speed – 2000 BPS on dial lines and 2400 BPS on leased lines.

c. Data set – WE 201A3 on dial lines; WE 201B1 on schedule 4C leased lines.

d. Code – ASCII X3.4-1967 for B 300/B 500/ B 5500 or 7 bit BCL for B 300/B 5500.

e. Time-out – 1 second.

f. Clock – synchronous (provided by data set).

g. Bit sequence – least significant bit first.

h. Longitudinal parity – odd on 7 bits (odd vertical parity on (LPC).

The longitudinal parity character (LPC) is generated over all characters following the STX and follows the ETX character in the transmission.

UNIVAC DCT-2000 ADAPTER
(B 2654-1 or B 3654-1)

The specifications for this switch-leased line adapter are as follows:

a. Character length – 7 data plus 1 parity.

b. Signaling speed – 2000 BPS on dial lines; 2400 BPS on leased lines.

c. Data set – WE 201A3 on dial lines; WE 201B1 on schedule 4C leased lines.

d. Code – USASCII X3.4-1967.

e. Time-out – 1 second.

f. Clock – synchronous (provided by data set).

g. Bit sequence – least significant bit first.

h. Longitudinal parity - odd on 7 bits (odd vertical parity on LPC).

The longitudinal parity character is generated over all characters following the SOH or STX characters and follows the ETX character in the transmission.

UNIVAC DCT-2000 ADAPTER WITH
AUTOMATIC DIAL OUT (B 2654-2 OR
B 3654-2)

This adapter has the same characteristics as the B 2654-1 or the B 3654-1, except that an auxiliary data set (801A) is used in conjunction with a 201A data set.

IBM 1030 ADAPTER (B 2656-1 OR B 3656-1)

The specifications for this leased adapter are as follows:

a. Character length – 6 bits plus 1 parity.

b. Stop bit – 2 bits.

c. Start bit – 1 bit.

d. Signaling speed – 600 BPS.

e. Data set – WE 202D on schedule 4 leased lines.

f. Code – PTTC-6.

g. Time-out – 20 seconds.

h. Clock – asynchronous.

i. Bit sequence – most significant bit first.

j. Longitudinal parity – even on all 7 bits.

The longitudinal parity character is generated over all characters following the EOA character and follows the EOB character in the transmission.

There is also a direct-line adapter for the IBM 1030.

83B3 MODEL 28 TELETYPEWRITER ADAPTER (B 2662 OR B 3662)

The specifications for this adapter are as follows:

a. Character length – 5 bits.

b. Start bit – 1 bit.

c. Stop bit – 2 bits.

d. Signaling speed – 74.6 BPS.

e. Code – Baudot A.

f. Clock – asynchronous.

g. Time-out – 20 seconds.

h. Bit sequence – least significant bit first.

i. Longitudinal parity – none.

j. Computer's CDC = BB.

k. Only 3 of these adapters may be used with a basic MLC.

The loss-of-carrier bit is set in the result descriptor if an open circuit exists for three seconds.

The adapter detects upper and lower case shift characters. The characters following an upper case shift character are stored in memory with the high-order bits of the eight bits set to 0-0-0. On each I/O operation, lower case is assumed initially until receipt of a shift character. Control codes are also flagged as upper and lower case. Shift characters are deleted from an input.

AUDIO ADAPTER (B 2663 OR B 3663)

The specifications for this adapter are as follows:

a. Character length – 8 bits.

b. Signaling speed – 10 characters per second.

c. Data set – WE 403E3 or -D5 on dial lines or schedule 4 leased lines.

d. Data code as stored in core memory – EBCDIC.

e. Time-out – 5 seconds.

f. Longitudinal parity – none.

The Touch-Tone translator adapter provides the translation from a BCM (binary coded mode) code to an 8-bit EBCDIC code as follows:

Key	BCM Code	EBCDIC	Graphic
0	0001	1111 0000 (F0)	0
1	1010	1111 0001 (F1)	1
2	1001	1111 0010 (F2)	2
3	1011	1111 0011 (F3)	3
4	0110	1111 0100 (F4)	4
5	0101	1111 0101 (F5)	5
6	0111	1111 0110 (F6)	6
7	1110	1111 0111 (F7)	7
8	1101	1111 1000 (F8)	8
9	1111	1111 1001 (F9)	9
*	0010	0000 0011 (03)	ETX
#	0011	0000 0101 (05)	ENQ

I/O Descriptors for Single-Line and Multiline Controls

The I/O descriptors for the single-line and multiline controls are listed in table 8-1 and are described in the following paragraphs.

UU denotes the linc adapter number and may be from 01 to 36, VV denotes variants to the Op Code, and RR denotes reserved for future expansion.

Sync codes, if required, must be received before the control is sensitive to any other code; leading sync codes are not stored in memory. After the receipt of the last leading sync code, the control stores in memory all codes except those assigned to the sync function, the upper-case-shift function, and the lower-case-shift function. One exception is that the read-transparent descriptor stores all codes following the last leading sync code. Codes following a shift code are appropriately identified with a flag bit.

Table 8-1
I/O Descriptors for Single-Line and Multiline Controls

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Read to Control	32	UUVV	Begin	End
Write to Control	34	UUVV	Begin	End
Write Transparent Read to Control	33	UUVV	Begin	End
Buffer Empty	31	UURR		
Input Request Enable	35	UURR		
Unconditional Cancel	39	UUVV		
Conditional Cancel	37	UURR		
Test	99	UURR		
Prepare to Read Address	38	UURR		

A control which denotes the response function, the negative-response function, or the end-of-transmission function terminates the appropriate portion of the operation if, and only if, they are not preceded by a code which denotes the start of text. One exception is that if a flip variant is used, a control code which denotes the EOT function will not cause a disconnect on the write portion. If a code denoting the start of text is received or sent before any other codes, only a code denoting the end of text terminates the appropriate portion of the operation, and other control codes are considered a part of the text.

If the 1 bit of the V variant is 1, a dial number is accessed from memory, starting at the location given by the A address. The dial number must be in 4-bit format and the dial field must be terminated by the control code 1100 (C). The total number of digits must be even and a filler digit must be inserted after the code 1100 (C), if necessary. Information to be written or received starts in the field following the control code or filler digit, as the case may be.

If the V variants indicate stream, a Read to Control, a Write to Control, and both portions of a Write to Control – Read to Control descriptor operate in a continuous stream mode. Stream is not permitted for Write to Control – Read Transparent descriptor. Operation is as follows:

a. The B address defines two buffer areas. Buffer area 1 is from memory location B minus 200 to, but not including, memory location B. Buffer area 2 is from memory location B to, but not including, memory location B plus 200.

b. For a Write to Control or a Read to Control descriptor, the information to be written or read starts either in the location specified by the A address or if V = 1, indicating dial, information starts in the location following the dial control code or dial filler digit.

c. For a Write to Control – Read to Control descriptor, the information to be written starts in the location as described above and the information to be read starts in the location following the control code which terminates the writing.

d. The initial transmittal and/or storage of data continues to, but not from/into, the location specified by the B plus 200 address. Subsequent transmittal and/or storage of data is from and/or to the memory locations defined by buffer areas 1 and 2.

e. The control sets the interrupt flip-flop ON and stores a result descriptor with the 1 bit and 2 bit set ON every time the B address and the B plus 200 address is reached.

f. The control must receive a Buffer Empty descriptor between each interrupt (during the second and each subsequent 100-character transmittal and/or storage time) to enable writing and/or reading from/to the next 100-character buffer area. If this descriptor is not received in time, the attempt-to-exceed-maximum-address bit is set ON in the result descriptor.

g. For a Read or a Write descriptor, a control code denoting the end of text terminates the operation. For a Write/Read descriptor, the control code denoting ETX in the Write portion terminates only the Write, and the control code denoting ETX in the Read portion terminates the Read operation.

h. During writing, a parity error or data loss terminates the operation immediately. During reading, the appropriate result descriptor bits are set ON when a result descriptor is stored, and operation continues.

If bit 6 of the V variant is 1, the control code denoting the end of text is not transmitted, the EOT function is ignored, and LRC is not generated or sent.

If bit 5 of the V variant is 1, the first code received or sent is considered text and is used in generating the LRC. The start of text function is preset.

If bit 7 of the V variant is 1, the time-out feature is inhibited.

If bit 8 of the V variant is 1 and bits 2 and 4 are 0 (zero), then characters received from memory are sent to the voice responder; these characters are used as voice track addresses.

If bits 4 and 8 of the V variant are 1 and bit 2 is 0 (zero), then each character received from memory is used to select a particular tone for a period of approximately 200 to 400 milliseconds. The EBCDIC character A (1100 0001) selects a tone of 1017 cycles per second; an EBCDIC character B (1100 0010), 2025 cycles per second. The EBCDIC character C (1100 0011) selects no tone and allows a pause of approximately 200 to 400 milliseconds.

If the V variant indicates ignore-ENQ, a Read operation ignores the ENQ response code.

READ TO CONTROL

Data are read from the remote device into ascending memory locations, beginning with the location specified by the A address. Reading is continued until a control code, denoting the end of text, is detected. In no case are the data stored in the ending location specified by the B address. The complete message read must be terminated by the receipt of the control code. Variants for dial, stream mode, preset STX, ignore ENQ, and inhibit time-out apply for this descriptor.

WRITE TO CONTROL

Data are written to the remote device from ascending memory locations, beginning with the location specified by the A address and continuing until a control code, which denotes the end of text, is detected.

In no case are data transmitted from the ending location specified by the B address. The complete message written must be terminated by the receipt of the control code. Variant bits are used independently and in combination as follows:

a. Bit 1 – dial.

b. Bit 5 – preset STX.

c. Bit 6 – delete ETX.

d. Bit 7 – inhibit time out.

e. Bits 8, 4, 3, and 2 as follows:

1) 0000 – Write to Control.

2) 0001 – Write to Control (stream mode).

3) 0010 – Write to Control/Read to Control.

4) 0011 – Write to Control – Stream/Read to Control – Stream.

5) 0100 – Write to Control/Read Transparent.

6) 0101 – invalid and undefined.

7) 0110 – Write to Control/Read to Control/Write to Control/Read to Control (polling).

8) 0111 – Write to Control/Read to Control – Stream/Write to Control/Read to Control – Stream (polling).

9) 1000 – Write to Control (voice response).

10) 1001 – invalid and undefined.

11) 1010 – Write to Control – Voice Response/Read to Control.

12) 1011 – Write to Control/Read to Control – Ignore ENQ.

13) 1100 – Write to Control – tone response.

14) 1101 – invalid and undefined.

15) 1110 – Write to Control – tone response/Read to Control.

16) 1111 – Write to Control/Read to Control – Ignore ENQ/Write to Control/Read to Control – Ignore ENQ (polling).

If the V variants indicate flip to Read to Control, data is written to the remote device from ascending memory locations, beginning with the location specified by the A address. Writing is continued until a control code which denotes the end of text is detected. Data is then read from the remote device into ascending memory locations, beginning with the location following the control code which terminated the writing. Reading continues until a control code which denotes the end of text is detected – up to, but not into, the ending location specified by the B address. Each portion of the message written and read must be terminated by a control code.

If the V variants indicate flip to Read Transparent, data is written to the remote device from ascending memory locations, beginning with the location specified by the A address. Writing continues until a control code which denotes the end of text is detected. Data is then read from the remote device into ascending memory locations, beginning at the location following the control code which terminated the writing. Reading continues until the ending location specified by the B address is reached; data is read up to, but not into, the B address. Reaching the ending address, when caused by the read portion of the descriptor, does not set the attempt-to-exceed-maximum-address error condition (bit 8) in the result descriptor.

If the V variants indicate polling, each poll address contained in memory must be delimited by a control code denoting ETX or by a control code denoting response (when not preceded by an STX function code). Detection of the code delimiting the poll address terminates the Write to Control operation and flips to a Read to Control operation for the response. A negative response code is not stored in memory, but terminates the Read to Control and flips back to the Write to Control operation for continuation of the polling.

A positive response is stored in memory following the code which terminated the Write to Control operation. The Read to Control operation is then terminated in the normal manner. The exhaustion of the poll list is determined by an ETX code immediately following the code delimiting the last

poll address. Note that polling information may not start with an ETX code.

WRITE TO TRANSPARENT –
READ TO CONTROL

Data is written to the remote device from ascending memory locations, beginning with the location specified by the A address. Writing continues until the ending location specified by the B address is reached; data is written up to, but not from, the B address. Data is then read into ascending memory locations, starting at the B address and continuing until a control code which denotes the end of text is detected. Data is read up to, but not into, the location specified by the B address plus 200. The variants for dial (bit 1) and inhibit time-out (bit 7) apply for this descriptor.

BUFFER EMPTY

A 100-character buffer area between the limits of the B - 200 and the B address, or between the limits of the B address and the B + 200 address, is made available to the control during the stream input/output mode.

INPUT REQUEST ENABLE

On dial lines, the phone line is disconnected; on dial and leased lines, input requests from the remote device, specified by adapter UU, are recognized.

UNCONDITIONAL CANCEL

The prior descriptor for adapter UU is unconditionally canceled. If bit 7 of the V variant is 1, a break is transmitted to the remote station. The break is applicable only to full duplex data sets. If bit 1 of the V variant is 1, the phone line is disconnected. Input requests are then ignored.

CONDITIONAL CANCEL

A prior descriptor is canceled if, and only if, an operation is not in process. Input requests from the remote device specified by adapter UU are ignored.

TEST

Line adapter UU is tested for a Ready or Busy condition and a channel result descriptor is returned which indicates the adapter identification number in bits 8-12. A busy single-line control does not store a channel result descriptor, but causes the invalid descriptor to be set ON in the processor result descriptor.

PREPARE TO READ ADDRESS

The contents of the two address memory words associated with adapter UU are transferred to the two address memory words associated with the control.

NOTE

This descriptor is valid only for the multiline control.

Single-Line and Multiline Result Descriptors

There are three result descriptors used with single-line and multiline controls which are:

a. Channel Result descriptor (test Op).

1) Bit 1 – operation complete.

2) Bit 2 – exception condition (set only if bit 3 or bit 5 is set).

3) Bit 3 – not ready (local).

4) Bit 4 – reserved.

5) Bit 5 – busy adapter multiline only; single-line causes processor result descriptor bit to be set).

6) Bits 6 and 7 – reserved.

7) Bits 8-12 – adapter identification number.

8) Bits 13-16 – unit number.

b. Multiline Channel result descriptor.

1) Bit 1 – operation complete.

2) Bit 2 – exception condition.

3) Bit 3 – not ready (local).

4) Bit 4 – invalid descriptor.

5) Bits 5-12 – reserved.

6) Bits 13-16 – unit number.

c. Adapter result descriptor.

1) Bit 1 – operation complete.

2) Bit 2 – exception condition.

3) Bit 3 – not ready (local – single-line; multiline if during operation).

4) Bit 4 – data error.

5) Bit 5 – abandon call and retry (ACR).

6) Bit 6 – cancel complete.

7) Bit 7 – end of transmission (EOT).

8) Bit 8 – attempted to exceed maximum address.

9) Bit 9 – time-out.

10) Bit 10 – memory parity error.

11) Bit 11 – write error.

12) Bit 12 – carrier loss.

13) Bits 13-16 – unit number.

14) Bits 4 and 5 – data loss.

15) Bits 6 and 7 – break detected.

If an invalid descriptor is sent to a single-line control, bit 4 in the processor result descriptor is set ON. An invalid descriptor sent to a multiline control sets bit 4 ON in the channel result descriptor.

For a Not Ready (local) condition, the operation is terminated immediately and bit 3 in the appropriate result descriptor is set ON. For the multiline control, the bit is set ON in the Channel result descriptor unless it occurs during an operation, in which case it is set ON in the Adapter result descriptor.

When a data error (message or character parity) occurs, bit 4 is set ON; bit 12 is set ON for a carrier loss; and for data loss (missed memory access or missed MLC cycle), bit 4 and bit 5 are set ON. In all cases, a reading operation continues until terminated in the normal manner; the phone line is not disconnected in any case. (An attempt to exceed maximum addresses, time-out, or an end of transmission can also occur.) When a data loss occurs during a writing operation, the writing is terminated immediately and bits 4, 5, and 11 are set ON.

During an abandon-call-and-retry condition, bit 5 is set ON and the phone line is disconnected.

For cancel-complete, bit 6 is set ON if the cancel takes place. If a cancel is sent to any idle control or if an operation is in process upon receipt of a conditional cancel, the single-line control sets bit 4 ON in the Processor result descriptor and the multiline control sets bit 4 ON in the Multiline Channel result descriptor.

When the end of transmission occurs, bit 7 is set ON and the phone line is disconnected.

When an attempt to exceed a maximum address occurs, the operation is terminated immediately; if the attempt occurs during a reading operation, bit 8 is set ON and if the attempt occurs during a writing operation, bits 5 and 11 are set ON. The phone line is not disconnected in any case.

When a time-out condition occurs, bit 9 is set ON and the phone line is not disconnected.

For memory parity error, bits 10 and 11 are set ON immediately; the phone line is not disconnected. Memory parity is reported only during a writing operation.

When a break is detected, a writing operation stores bits 6 and 7. The phone line is not disconnected.

Terminal Unit Control

The B 2350-1 or B 3350-1 Terminal Unit Controls are provided to accomplish on-line banking operations. The terminal unit control is housed in the I/O cabinet and uses a Type A I/O channel. Only one B 2350-2 Central Terminal Unit can be connected to a terminal unit control on a B 2500 System, but up to nine additional central terminal units can be connected to a terminal unit control via an exchange on a B 3500 System. One B 3650 Line Adapter permits one B 3350-2 Central Terminal Unit to be attached to the exchange.

The terminal unit controls can be intermixed on a system with single-line and multiline controls or other terminal unit controls up to the number of I/O channels available.

The terminal unit control gives priority for requests in a unidirectional ascending sequence to central terminal units, starting with the central terminal unit number specified in the descriptor. Output requests are given priority over input requests.

The terminal unit control uses a standard 8-bit parallel data transfer to memory and a 6-bit parallel data transfer to the attached terminal unit.

The code relationship is as follows:

Bits transferred to memory –	8 7 6 5 4 3 2 1
Bits transferred to attached terminal unit –	6 5 4 3 2 1

Bits 7 and 8 are deleted from outgoing data and are set to 00 for incoming data. The control is sensitive to the code 01 1111 as the end-of-message. The Input Request Disable descriptor puts the terminal unit control into an idle state in which all lines from the terminal units are ignored.

If a Read or Write descriptor is sent to a terminal unit which is unable to perform the operation, the appropriate bits of the result descriptor are set ON. Thus, if a Write descriptor is sent to a terminal unit that is Input Ready, bits 1, 2, and 6 are set ON. If a Read descriptor is sent to a terminal unit that is Output Ready, bits 1, 2, and 7 are set ON. The terminal unit number is also returned in the result descriptor.

If the control is input-request-enabled, an input request sets bits 1, 2, and 6; an output request sets bits 1, 2, and 7. The terminal unit number is also returned in the result descriptor.

If a reading operation is terminated because of reaching an ending address, bits 1, 2, 7, and 8 are set ON. In response to a Read descriptor, Test descriptor, or a Write descriptor, an idle terminal unit sets bits 1, 2, 6, and 7 ON. The terminal unit numbers (0-9) are selected at the time of terminal unit installation. The time required for the scanner to examine adjacent channels for Ready states is a maximum of one microsecond; a complete scan takes 10 microseconds. (The terminal unit control must receive an Enable descriptor every 11 seconds or less.)

MODULARITY

One terminal unit connects directly to the terminal unit control and subsequent terminal units connect to the terminal unit exchange. From one to nine terminal unit exchange adapters can be added to the terminal unit exchange; one adapter must be used for each terminal unit connected to the exchange. From one to three terminal unit exchange extension adapters can be added to the terminal unit exchange. One adapter must be used for each group of three terminal units connected to the exchange.

I/O Descriptors for Terminal Unit Controls

The I/O descriptors which are used for terminal unit controls are listed in table 8-2.

U denotes terminal unit designators and R denotes reserved for future expansion.

Each of these descriptors is described in the following paragraphs.

READ

Data is read from the terminal unit into ascending memory locations, beginning with the location specified by the A address and continuing until a

Table 8-2
I/O Descriptors for Terminal Unit Controls

Name	Op Code	Digits 3-6	Digits 7-12	Digits 13-18
Read	32	RURR	Begin	End
Write	34	RURR	Begin	End
Input Request Enable	35	RURR		
Input Request Disable	97	RRRR		
Test	99	RURR		

control code indicating end-of-message is detected. Data is read into memory up to, but not into, the ending location specified by the B address. In all cases, the complete message read must be terminated by the receipt of the control code. The control code is transferred to memory.

WRITE

Data is loaded into the terminal unit buffer from ascending memory locations, beginning with the location specified by the A address and continuing until either the control code which indicates end-of-message is detected, the terminal unit buffer is filled, or the ending location specified by the B address is reached. In all cases, except for the final buffer load which is terminated by the control code, the buffer must be filled.

INPUT REQUEST ENABLE

All input and output requests from all terminal units are ignored.

TEST

Terminal unit U is tested and a result descriptor is returned which reflects the conditions of that terminal unit.

Terminal Unit Result Descriptor

The terminal unit is defined as follows:

a. Bit 1 – operation complete.

b. Bit 2 – exception condition.

c. Bit 3 – not ready.

d. Bit 4 – parity error.

e. Bit 5 – busy.

f. Bit 6 – input ready.

g. Bit 7 – output ready.

h. Bits 6 and 7 – terminal unit is idle.

i. Bit 8 – exceed maximum address.

j. Bits 9-12 – reserved.

k. Bits 13-16 – unit number (0-9).

CENTRAL TERMINAL UNIT

The B 2350-2 and B 3350-2 Central Terminal Units (figure 8-1) provide temporary storage for messages between the teller consoles and the B 2500 or B 3500 System. There are six identical channels to the central terminal unit (CTU), with up to 16 teller consoles serviced by each channel. The six channels can accumulate messages simultaneously because of the time sharing technique.

Figure 8-1. Central Terminal Unit

The CTU polls each teller console (TC) of a buffer pair sequence. This poll takes place between 20 and 60 milliseconds per TC. The poll code is sent to all teller consoles of a buffer pair. Only the addressed TC responds with a Ready-to-Send response to the CTU when a TC which has an input is polled and the remote terminal unit to which it is connected is free. A transmit code is sent to the remote terminal unit from the CTU. In the event of the absence of a Ready-to-Send response, polling continues.

Three words stored in the TC by the teller are transmitted to the CTU and stored in one of the buffer pairs assigned to the channel. Upon receipt

of an error-free completed message, the CTU sets a flag indicating to the terminal unit control that the CTU is ready for system attention. The system periodically interrogates the terminal unit control to check if it has located any CTU's that are ready for system attention. If the terminal unit indicates that a CTU is System Ready, a Read order will be initiated to transfer the input message to the processor. After processing the input message, the system transmits the output message to the CTU buffer. The CTU polls the appropriate TC to determine if it is Output Ready. The message is then transmitted to the TC a segment at a time. The message transmission continues until a group mark indicates end-of-message.

REMOTE TERMINAL UNIT

The remote terminal unit (figure 8-2) is used to connect up to eight teller consoles to the B 2500 or B 3500 System through the use of full duplex private telephone lines. It should be noted that the remote terminal unit (RTU) is not a full duplex unit and will not be able to send and receive information simultaneously.

Figure 8-2. Remote Terminal Unit

The RTU always knows the input/output status of the teller console, provides temporary storage of information received for and from the teller console, maintains constant contact with the processing center through control messages and replies, initiates message and reply transmission, and checks the accuracy of information received from the teller console and processing center, as well as adding checking data to all messages it transmits. The RTU may be located up to 50 feet from the teller console and Data Set 202D.

TELLER CONSOLE

The teller console (figure 8-3) is the communication link between the teller and the processing center; each console serves two tellers. The console operates similarly to the style F 6214 two-teller Sensimatic machine, but has been modified to provide read-in and read-out capabilities in the system as well as certain other features essential to an on-line savings and mortgage application. It accepts teller-indexed transaction messages for transmission to the processing center and prints processed replies (received from the processing center) on customer passbooks, transaction tickets, and the transaction journal.

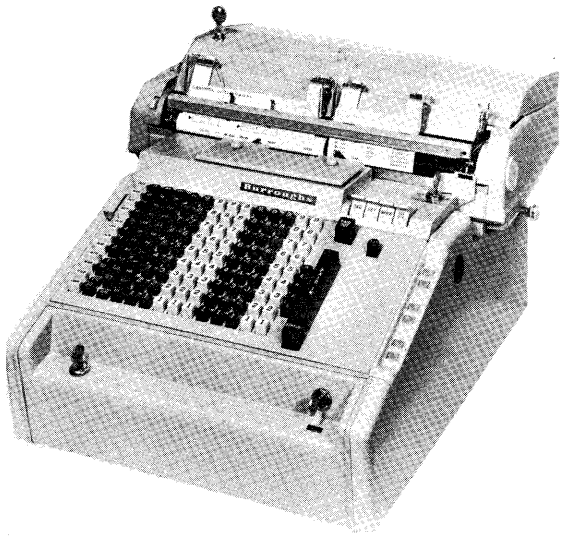


Figure 8-3. Teller Console

Through the teller console, tellers can perform the following:

a. Post payments and disbursements to savings or mortgage accounts.

b. Inquire into the status of such accounts.

c. Handle other types of window transactions and inquiries encountered in a financial institution.

Through the computer, and also independently of the computer, the teller console controls teller cash increases and decreases as affected by the various transactions.

The teller console can be programed to fit existing passbooks and to meet operating and auditing requirements of individual institutions, including complete control of the entry, removal, and override of account holds. Excellent communication between the computer and the teller is provided by status lights, an audible signal, and alphanumeric account status print-outs. A detailed audit trail is provided in the form of validated transaction tickets and an easily read transaction journal on which each transaction occupies one line with each entry of the transaction in separate columns.

Automatic features protect against incorrect posting on the passbook. These features are:

a. Non-operation of the teller console if the transaction requires posting on a passbook and the book is not inserted.

b. Spacing over the stitching at the centerfold.

c. Non-operation when the passbook has printed on the last line.

d. Protection against posting on the wrong line of the book which avoids over-printing of current transactions on previous lines of posting.

Proved teller-oriented design provides maximum ease and efficiency of operation through a simplified keyboard, exclusive single entry-key operation, and buffering which permits the teller to enter the entire transaction without delay even when other teller consoles are transmitting or receiving data.

B 9350 TYPEWRITER INQUIRY STATION

The B 9350 Typewriter Inquiry Station utilizes a Send/Receive Page Printer set. The alphanumeric keyboard is provided with contacts suitable for keying of alphanumeric input data. The B 9350 communicates with the single-line or multiline control via a single multiple conductor cable. This B 9350 may be up to one mile from the B 2500 or B 3500 System. The station set operates at a standard rate of 10 characters per second by selectively pressing the keys and space bar of the keyboard in the same manner as typing.

COMMON CARRIER AND DATA SET COMPATIBILITY

The data communications network provides the capability to operate over the following available common carrier services and data sets. Data sets equivalent to those listed may also be used.

a. Telephone company private lines.

   1) Schedule 3 channel; less than or equal to 75 BPS; Relay.

   2) Schedule 3A channel; less than or equal to 150 BPS; WE 816A.

   3) Schedule 4 channel; less than or equal to 1000 BPS; WE 202D, 103E, 403E3, 403D5.

   4) Schedule 4A channel; less than or equal to 1200 BPS; same data sets as schedule 4.

   5) Schedule 4B channel; less than or equal to 1800 BPS; WE 202D.

   6) Schedule 4C channel; less than or equal to 2400 BPS; WE 201B1.

b. Telephone company switched lines.

   1) TWX; WE 103A, 811B.

   2) Dataphone (normal DDD network); WE 103A, 103E, 202C, 201A3, 403E3, 403D5.

   3) WATS (normal DDD network); WE103A, 103E, 202C, 201A3, 403E3, 403D5.

c. Western Union private lines.

   1) Class D channel; less than or equal to 180 BPS; WE 103F.

   2) Class E channel; less than or equal to 2400 BPS; WE 202D, 201A3, 201B1.

   3) Class F channel (two point only); less than or equal to 2400 BPS; WE 202D, 201A3, 201B1.

d. Western Union switched lines (none).

e. International leased lines.

1) Telephonic; less than or equal to 1200 BPS; WE 202D.

2) Telephonic; 600 BPS; B.P.O. DATEL 1C5, S.E.L. type GH-2011 model 5.

3) Telephonic; 1200 BPS; B.P.D. DATEL 1C5, S.E.L. type GH-2011 model 5.

f. International switched lines.

1) Telephonic; less than or equal to 1200 BPS; WE 202C.

CONTROL CODES

Appendixes E and F provide various transmission codes and control codes used with the data communications network. Appendix E provides Baudot/EBCDIC translation and PTTC/6 to EBCDIC translation.

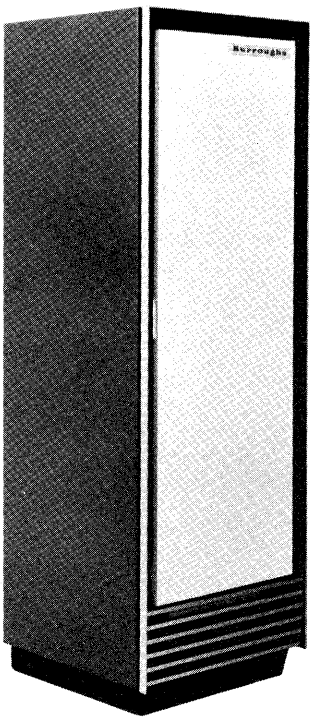


Figure 8-4. Audio Response Unit

AUDIO RESPONSE UNIT

This unit allows the B 2500/B 3500 Systems to construct an audio message by digitally addressing words or phrases that have been pre-recorded on a photographic film drum. The output message is then transmitted over a telephone line to a telephone handset at the remote end. The audio response unit accommodates up to 128 telephone lines beginning with two lines and increasing in increments of two lines. Any recorded track on the drum can be read onto any telephone line at any point in time. That is, track 1 may produce output to all 128 telephone lines simultaneously, or all 64 tracks may produce output to telephone lines simultaneously. The audio response unit is shown in figure 8-4.

An essential part of the audio response unit is the audio response generator (figure 8-5). The generator consists of a photographic sound film, a light source, detector cells, and circuitry to transmit the sound waves detected.

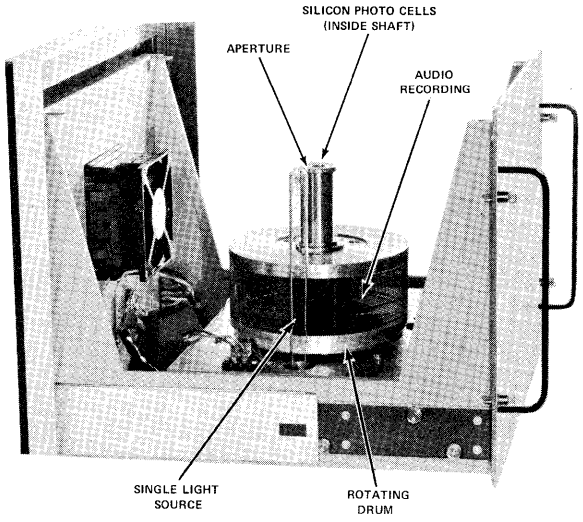


Figure 8-5. Audio Response Generator

An audio response unit consists of the following units and modules:

a. Cabinet.

1) Ten-line module.

2) Two-line module.

b. Auxiliary cabinet 1.

c. Auxiliary cabinet 2.

d. Film drum.

The various units are described in the following paragraphs.

Main Cabinet

This unit consists of a cabinet, power supply, single-light audio response unit, and can accept up to three ten-line modules.

Auxiliary Cabinet 1

This unit consists of a cabinet and can accept up to eight ten-line modules.

Auxiliary Cabinet 2

This unit consists of a cabinet and a power supply, and can accept up to five two-line modules.

Ten-Line Module

This unit consists of the necessary electronic components to accept up to five two-line modules.

Two-Line Module

This unit consists of plug-in cards which are installed in a ten-line module. A two-line module is required for each two phone lines to be serviced.

Audio Response System Requirements

The number and types of cabinets required depends on the number of lines as listed in table 8-3.

Recording Medium

The recording medium for the audio information consists of a transparent drum with film wrapped around its surface. This film stores spoken words or phrases on photographic sound tracks. The drum completes a revolution in 1.6 seconds; it is read via a light source and photo cells (one photo cell per track per light source). A user may have his own unique vocabulary film. A film can be changed in approximately one hour by a Burroughs Corporation representative.

The cylindrical film drum is 7-3/8 inches in diameter and 5½ inches high. The design of the film drum for a particular customer may be accomplished in one of two ways. A large library of words and phrases will be made available to the customer from which to choose his own library. If the library does not contain particular words and/or phrases that a customer desires, a special recording session may be set up to create that customer's vocabulary.

Storage Unit

This unit has 64 tracks of which 63 are audio information tracks. One track contains a timing pulse with no audio information. There is no sound on the timing pulse track and it is addressed when pause or silence is desired on the output. The vocabulary may consist of words and/or phrases. A phrase utilizes the whole track with no repetition, whereas a word is recorded three times around on a track as shown in figure 8-6.

A phrase may consist of several words. The duration of a phrase is approximately 1½ seconds and the duration of a word is approximately ½ second. Different words may be recorded in the three different word locations although undesired pauses may then be present in the audio response. If an answer consists of a phrase following a word, the program must supply "silence" words to ensure that the phrase always begins at the phrase time.

Table 8-3
Audio Response System Requirements

Number of Lines	Cabinet	Auxiliary Cabinet 1	Auxiliary Cabinet 2
1-30	1	0	0
31-64	1	1*	0
65-80	1	0	1
81-128	1	1	1

* Auxiliary cabinet 2 may be substituted if future expansion is anticipated.

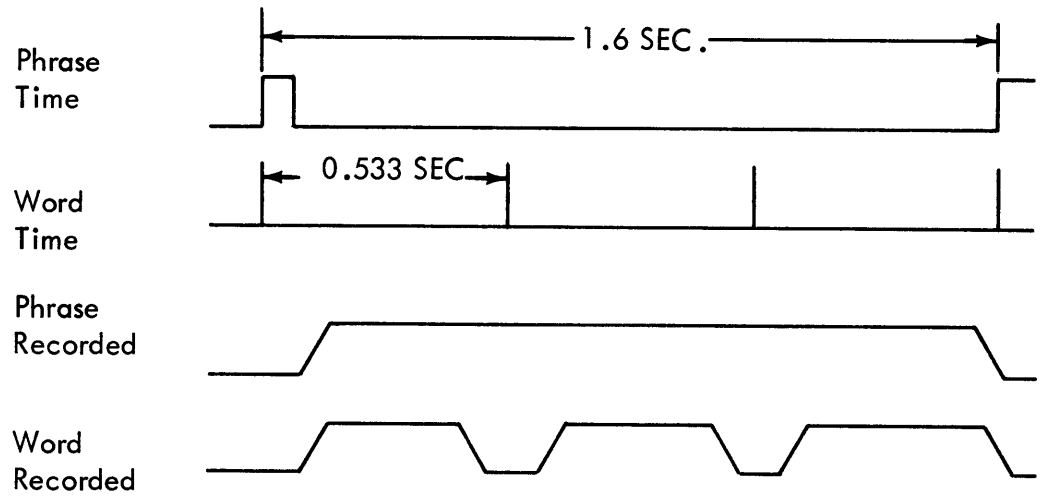


Figure 8-6. Word/Phrase Timing Relationship on Audio Response Unit Track

ADDRESSING

A 6-bit code is used to address the desired track (1-64). One of the tracks is used for timing purposes and, therefore, contains no audio information. It may be addressed to create a pause or whenever the no-output state is desired.

All 64 tracks may be read simultaneously, with the information being passed on to the telephone lines. Addressing to read an output begins at the defined starting point on the drum. From that point on, a new track address is required every one-third revolution of the drum to allow each word to be separately addressed. The message is then constructed by selecting, in a desired sequence, the appropriate words or phrases which make up the reply.

ADDRESSING EXAMPLES

Following are two examples which show the method of representing words and phrases in the audio response unit.

Example 1

1.5 Second Phrase

"Your present balance is

0.5 Second Words

three hundred sixty dollars twenty cents"

This message requires 4.5 seconds to transmit and nine data characters for addressing. The address for the sentence might be:

AAA3QBPTU

where:

a. AAA – Your present balance is
b. 3 – three
c. Q – hundred
d. B – sixty
e. P – dollars
f. T – twenty
g. U – cents

Example 2

1.5 Second Phrase

"The amount is

0.5 Second Words

two three three one four"

This message requires four seconds to transmit and requires eight data characters for addressing. The address for the sentence might be:

BBB23314

where:

a. BBB – The amount is
b. 2 – 2
c. 3 – 3
d. 3 – 3
e. 1 – 1
f. 4 – 4

ABDFPG5T9U

where:

a. A – Your

b. B – account

c. D – is

d. F – overdrawn

e. P – by

f. G – six

g. 5 – five

h. T – dollars

i. 9 – nine

j. U – cents

TC 500 Terminal Computer

The TC 500 Terminal Computer (figure 8-7) is a desk type unit, operator controlled, electronic digital computer with integrated circuity. It can function as an independent computer or as a remote terminal in a data communication network to a central computer data center. It contains two processors to provide independent data communication and main memory control.

A magnetic disk provides the memory for the system and serves both the data communication processor and the main memory processor. Programs are stored internally in main memory. The main memory processor permits a variable and flexible instruction list. The data communication processor implements a flexible communication control procedure and provides for message buffering.

The TC 500 includes keyboards for operator entry of numeric and alphabetic data, and a serial printer for output. These represent the basic means of input and output. Optional features include punched paper tape and edge-punched card input and output, or 80-column punched card input and output.

Figure 8-7. TC 500 Terminal Computer

The memory of the TC 500 consists of a magnetic disk of ceramic composition, which revolves at a speed of 6,000 RPM, or 10ms per revolution. The disk contains 1,280 words of 64 bits each, and is organized into 5 blocks of 8 tracks each, or a total of 40 tracks. Each track has its own read-write head. Only one side of the disk is utilized.

Each word in memory may be utilized in any of the following formats: It may consist of 15 digits plus sign; it may contain 8 alphanumeric characters; or it may contain four instructions of 4 digits each (in machine language coding). This flexibility permits memory to be used to store program instructions, numeric factors and constants, alpha characters and messages, printing formats to control printing and punching, and other information for control of the system such as flags and registers for indexing and forms control.

For purposes of explaining key functions and keyboard instructions, the console is considered as having three separate keyboards: Typewriter, Numeric, and Program Selectors. From a design standpoint however, it has only a keyboard since there is no mechanical linkage between it and other sections of the computer.

The console can contain up to 16 program select keys, 4 operational control keys (located on both the numeric and alphanumeric keyboards), standard alphanumeric communications typewriter keyboard, and a 10-key numeric keyboard. Up to 29 operator communication lights are provided.

The serial printer for output is a 64-character removable ball which prints serially 10 characters per inch at a rate of 20 characters a second. It is mounted on a carrier mechanism called a servo device. Printer positioning and printing are controlled by the program. The print line is 150 character positions. The print cycle executes an escape before it prints.

The standard 64-character set includes the 26 letters. A thru Z, numerals 0 thru 9, fractions 1/4, 1/2, and 3/4, and 25 symbols.

The printer ribbon with two-color control (black and red) is contained in a removable cartridge which is attached to the printer carrier. An automatic reversing mechanism is provided to reverse the direction of ribbon travel.

The Forms Transport of the TC 500 is designed to permit rear feeding of individual cut forms or continuous forms of various lengths and widths, and provides programmatic alignment to the first printing line with either type of form. It includes a stationary 15.5 inch platen. The length of the print line is 150 characters, at 10 characters per inch.

Split and normal platens are provided to facilitate forms handling flexibility. The standard split location is 11.5 inches from the left end of the printing line, however, a number of split positions are available. The location of the split is in relation to the print position in that the split is located between print positions immediately to the left and immediately to the right of a split without impairment of any printed character.

The power requirements for the TC 500 are 115 volts at 60 cycles, and the environmental requirements are:

a. Temperature – 105 degrees F max. and 50 degrees F min.

b. Relative humidity – 5% to 95%.

The physical characteristics are as follows:

a. Height – 29-7/8 inches.

b. Width – 48 inches.

c. Depth – 41 inches.

d. Weight – 398 pounds.

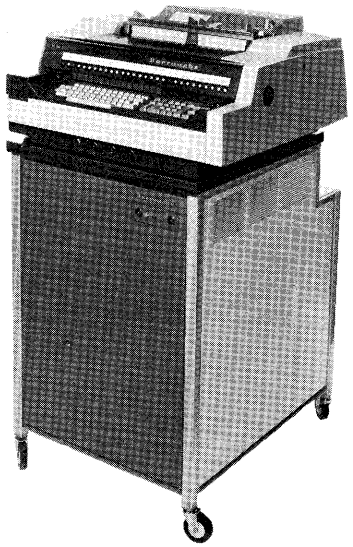


Figure 8-8. TC 700 Terminal Computer

TC 700 Terminal Computer

The TC 700 has all the functional capabilities of the TC 500 (with the exception of the 80-column punched card I/O), and in addition handles passbooks, unit documents, and transaction journals.

The physical characteristics for the TC 700 are as follows:

a. Keyboard Printer Section height – 13 inches.

b. Keyboard Printer Section width – 30 inches.

c. Keyboard Printer Section depth – 26 inches.

d. Logic and Memory Section height – 37 inches.

e. Logic and Memory Section width – 25 inches.

f. Logic and Memory Section depth – 30 inches.

The sections are cable connected and can be separated up to 50 feet.

B 3351 Input and Display System

The B 9351 Input and Display System is a general purpose, alphanumeric input/output system for use with all Burroughs computer systems. The system can be connected to the computer locally using cable or remotely using telephone lines.

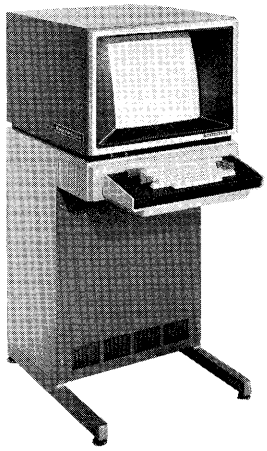


Figure 8-9. B 9351 Input and Display System

The B 9351 System has the following features:

a. The system may consist of a control unit, monitor and keyboard, or a shared control unit accommodating one to four monitors and one to four keyboards (one keyboard per monitor).

b. Each control unit contains 1,024 character positions of high speed core memory of which a maximum of 1,018 are available for display data. When a control unit is shared among two to four display monitors, memory is available in combinations of 762, 506, or 250 character positions per monitor.

c. The information stored in memory has no special relationship to the information displayed on the screen. The contents of memory can be displayed in any of the 2,000 positions on the screen.

d. Total or partial contents of the screen may be transmitted.

e. The monitor has a 9 x 12 inch distortionless viewing area.

f. The image is flicker-free and non-floating.

g. Minimum brightness is 50 foot-lamberts.

h. Monitor includes a single function brightness control.

i. Screen capacity is 2000 character positions.

j. Display area consists of 25, 80-character lines.

k. Line spacing is 3.33 lines per inch.

l. A total of 67 characters may be displayed. These consist of all alphanumeric characters and 30 special characters plus the cursor.

m. Character spacing is seven characters per inch.

n. Characters are formed using up to 12 straight line strokes.

o. The keyboard includes the conventional typewriter arrangement plus special character and control keys.

p. The keys are electrically interlocked to prevent results from more than one key action at a time.

q. Ten fixed tabulator positions are provided.

r. A non-destructive cursor simplifies operation.

s. A separate on-off switch is provided for the monitor.

t. Modular construction allows monitor, keyboard, and control to be separated where such an arrangement is more convenient.

Optional features which are available on this system are as follows:

a. A stand to hold the monitor and keyboard when it is not mounted on the control unit.

b. Insert/delete option which allows a character or a full or partial line to be inserted or deleted.

c. Input and display system printer which provides a hard-copy reproduction of displayed messages.

d. Controlled format option which prevents accidental alteration of computer supplied forms and enables transmission of operator-entered data only.

e. A programmatic cursor control option simplifies cursor positioning under computer control.

The physical characteristics of the control unit are:

a. Width – 19-1/4 inches.

b. Depth – 14 inches.

c. Height – 25 inches.

d. Weight – 85 pounds.

e. Power requirements – 105 to 125 volts a.c., 50/60 cycle, single phase.

f. Power consumption – 400 watts.

g. Operating environment – 59 to 100 degrees F temperature and 10 to 90 percent humidity.

The physical characteristics for the monitor are:

a. Width – 19-1/4 inches.

b. Depth – 22 inches.

c. Height – 18 inches.

d. Weight – 70 pounds.

e. Power requirements – 105 to 125 volts, a.c., 50/60 cycle, single phase.

f. Power consumption – 300 watts

g. Operating environment – 59 to 100 degrees F temperature and 10 to 90 percent humidity.

The physical characteristics for the keyboard are:

a. Width – 17-1/2 inches.

b. Depth – 6-5/8 inches.

c. Height – 3-1/2 inches.

d. Weight – 5 pounds.

e. Power source – Control Unit.

f. Operating environment – 59 to 100 degrees F temperature and 10 to 100 percent humidity.

Auxiliary components for use with this system are as follows:

a. Modem Expander – This unit may be used when multiple terminals are required at one location. It accommodates up to four terminal units and may be used on a single-point or multi-point communications circuit. An extension is available to accommodate four additional terminal units. Up to three extensions may be handled by each expander. This provides a total capacity of 16 terminal units per expander unit.

b. Data Set Adapter – This provides compatibility with Bell System DATA-PHONE data set series 201, 202, or equivalent modems and operates from 1200 to 2400 BPS.

c. Up to nine terminals may be directly connected to the computer on one cable.

B 939 B 9352 Input and Display Terminal

The B 9352 is a general purpose, alphanumeric input/output terminal for use with all Burroughs computer systems. The terminal can be connected to the computer locally using cable, or remotely using common carrier lines.

The terminal is a free-standing, self-contained unit which includes a monitor screen, keyboard, character generator, control logic, and memory. The

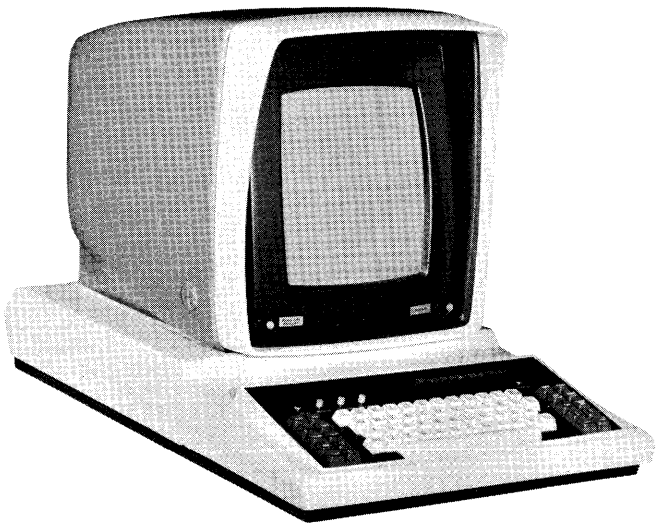


Figure 8-10. B 9352 Input and Display Terminal

operating characteristics for this unit are as follows:

a. The terminal contains 960 characters of magnetostrictive delay line memory.

b. Information contained in memory is specially related to the data displayed on the screen.

c. Screen capacity is 960 characters.

d. Two screen formats are available: A vertical format with 24 lines of 40 characters each or a horizontal format with 12 lines of 80 characters each.

e. The vertical format viewing area is 7-1/2 by 8-1/2 inches.

f. The horizontal viewing area is 11 by 7-1/2 inches.

g. Line spacing is 3.33 lines per inch.

h. A total of 70 different characters may be displayed. These consist of all alphanumeric characters, 31 special characters, cursor, blank, and a full raster.

i. Characters are formed using the dot matrix technique.

j. The minimum brightness is 50 foot-lamberts.

k. The image is flicker-free and non-floating.

l. Total or partial contents of the screen may be transmitted.

m. The monitor controls consist of a combination on-off and brightness control and a focus control.

n. The keyboard consists of the conventional character and control keys.

o. The keys are electrically interlocked to prevent results from more than one key action at a time.

p. A non-destructive cursor simplifies operation.

q. The line erase key allows a line to be deleted between the cursor and the end of the line.

r. The erase lock key protects against accidental erasures.

s. Tabs may be set at any or all character positions on the horizontal line.

t. An audible alarm sounds for incoming messages.

u. An audible alarm at a different frequency acts as an end of line indicator.

The following are optional features which may be provided with this unit:

a. Input and display printer to provide hard-copy reproduction of displayed messages.

b. Controlled format option prevents accidental alteration of formats supplied by the computer. Only operator-entered data is transmitted.

c. The polling and select option is required when more than one terminal is used. A "broadcast" capability is included with this option.

The physical characteristics for the vertical format version of this unit (B 9352-1) are as follows:

a. Width – 17-1/2 inches.

b. Depth – 30-1/8

c. Height – 19-3/8 inches.

The physical characteristics for the horizontal format version of this unit (B 9352-2) are as follows:

a. Width – 17-1/2 inches.

b. Depth – 30-1/8 inches.

c. Height – 17-7/8 inches.

The weight of these units is 100 pounds.

Auxiliary components for use with this system are as follows:

a. Modem Expander – This unit may be used when multiple terminals are required at one location. It accommodates up to four terminal units and may be used on a single-point or multi-point communications circuit. An extension is available to accommodate four additional terminal units. Up to three extensions may be handled by each expander. This provides a total capacity of 16 terminal units per expander unit.

b. Data Set Adapter – This provides compatibility with Bell System DATA-PHONE data set series 201, 202, or equivalent modems and operates from 1200 to 2400 BPS.

c. Up to nine terminals may be directly connected to the computer on one cable.

APPENDIX A
B 2500/B 3500 HARDWARE INSTRUCTION LIST

This appendix presents lists of mnemonic operation codes used by the B 2500/B 3500 Systems hardware. The operation codes are grouped by general classification, and most three-character operation codes (representing actual systems operation codes) produce a single instruction. These instructions, together with pseudo and macro instructions peculiar to the Assembler, are described in detail in the B 2500 and B 3500 Assembler Reference Manual (1034949).

Mnemonic	Function	No. of Addresses
Data Movement		
MVA	Move Alphanumeric	2
MVN	Move Numeric	2
MVR	Move Repeat	2
MVW	Move Word	2
MVC	Move and Clear Word	2
MVL	Move Links	3
Arithmetic		
INC	Add – Two Address	2
ADD	Add – Three Address	3
DEC	Subtract – Two Address	2
SUB	Subtract – Three Address	3
MPY	Multiply	3
DIV	Divide	3
Floating Point Arithmetic		
FAD	Floating Point Add	3
FSU	Floating Point Subtract	3
FMP	Floating Point Multiply	3
FDV	Floating Point Divide	3
Logical		
TRN	Translate	3
SDE	Scan to Delimiter – Equal	2
SDU	Scan to Delimiter – Unequal	2
SZE	Scan to Delimiter – Zone Equal	2
SZU	Scan to Delimiter – Zone Unequal	2
BZT	Bit Zero Test	1
BOT	Bit One Test	1
AND	AND	3
ORR	OR	3
NOT	NOT	3
SEA	Search	3
CPA	Compare Alphanumeric	2
CPN	Compare Numeric	2
EDT	Edit	3
Address Branching		
NOP	No Operation	1*
LSS	Branch on Less Than	1*
EQL	Branch on Equal	1*

* Length is one character and one address. There is no AF or BF.

Mnemonic	Function	No. of Addresses
LEQ	Branch on Equal or Less Than Equal	1*
GTR	Branch on Greater	1*
NEQ	Branch on Not Equal	1*
GEQ	Branch on Greater Than or Equal	1*
BUN	Branch Unconditionally	1*
OFL	Branch on Overflow	1*
NTR	Enter	1
Branching		
EXT	Exit	1
BCT	Branch Communicate	0
Privileged		
BRE	Branch Reinstate	0
IIO	Initiate I/O	1
RAD	Read Address	1
RCT	Read and Clear Timer	1
RDT	Read Timer	1
SRD	Scan Result Descriptor	0
STT	Set Timer	1
Miscellaneous		
SMF	Set Mode Flip-Flop	0
HBR	Halt, Branch	1*
HBK	Halt, Breakpoint	0

* Length is one character and one address. There is no AF or BF.

APPENDIX B
B 2500/B 3500 I/O DESCRIPTORS

Op Code	Function	No. of Addresses
Magnetic Tape		
01	Magnetic Tape Rewind	0
02	Magnetic Tape Read Forward	2
03	Magnetic Tape Read Backward	2
04	Magnetic Tape Erase	2
06	Magnetic Tape Write	2
08	Magnetic Tape Space Forward	0
09	Magnetic Tape Space Backward	0
Line Printer		
10	Printer Write	1
11	Printer Skip	0
Card Reader		
20	Card Read BCL	2
21	Card Read Binary	2
22	Card Read EBCDIC	2
Card Punch		
23	Card Punch BCL	1
24	Card Punch Binary	1
25	Card Punch EBCDIC	1
Data Communications		
31	Buffer Empty	0
32	Read to Control	2
33	Write Transparent – Read to Control	2
34	Write to Control	2
37	Conditional Cancel	0
38	Prepare to Read Address	0
39	Unconditional Cancel	0
Paper Tape		
40	Paper Tape Read	2
41	Paper Tape Space	2
43	Paper Tape Backspace	2
47	Paper Tape Rewind	0
48	Paper Tape Write	2
Disk File		
50	Disk File Write	3
51	Disk File Read	3
52	Disk File Check	3
Sorter-Reader		
62	Flow Read	2
63	Demand Read	2
60	Pocket Select	0
66	Batch Count	0
64	Pocket Light	0
35	Input Request Enable	0

Op Code	Function	No. of Addresses
97	Input Request Disable	0
99	Test	0
Lister		
70	Lister Print	2
71	Lister Space	0
72	Lister Skip	0
73	Lister Slew	0
Used With More Than One Control		
35	Input Request Enable	2
97	Input Request Disable	2
99	Test	2

APPENDIX C
B 2500/B 3500 RESULT DESCRIPTORS

APPENDIX D
EBCDIC, ASCII, AND BCL REFERENCE TABLES

The charts reflected in this appendix define the EBCDIC, ASCII, and BCL code specifications as implemented by the Burroughs Corporation for the B 2500/B 3500 systems.

Table D-1 and table D-2 show the USASCII X3.4 - 1963 and USASCII X3.4 - 1967 code sets respectively. The major differences in the code sets are in columns 0 and 1 (control characters) and columns 6 and 7 (lower case characters).

Table D-3 is an explanation of all characters and their functions or meanings for both the 1963 and 1967 versions of the USASCII character set. In this presentation, the first entry is the column/row notation in respect to tables D-1 and D-2. The second item is the character as it appears in the two tables, the 1963 version appearing at the top and the 1967 version on the bottom. Following the characters is the name and function of the character, if in fact it is not evident.

When reading table D-1 and D-2, and using columns and rows; the standard 7-bit character representation, with B 7 the high-order bit and b the low-order bit, is shown below:

EXAMPLE:

The bit representation for the character K positioned in column 4, row 11 is:

$b_7\ b_6 b_5 b_4 b_3 b_2 b_1$
1 0 0 1 0 1 1

The decimal equivalent of the binary number formed by bits b_7, b_6, and b_5, collectively, forms the column number, and the decimal equivalent of the binary number formed by bits b_4, b_3, b_2, and b_1, collectively, forms the row number.

Table D-4 reflects the Extended Binary Coded Decimal Interchange Code (EBCDIC) and is read exactly as tables D-1 and D-2.

Table D-1

USASCII X3.4-1963

Bits b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1 Row \ Column	0	1	2	3	4	5	6	7
0 0 0 0 0	NULL	DC_0	b	0	@	P	↑	↑
0 0 0 1 1	SOM	DC_1	!	1	A	Q		
0 0 1 0 2	EOA	DC_2	"	2	B	R		
0 0 1 1 3	EOM	DC_3	#	3	C	S	UNASSIGNED	UNASSIGNED
0 1 0 0 4	EOT	DC_4	$	4	D	T		
0 1 0 1 5	WRU	ERR	%	5	E	U		
0 1 1 0 6	RU	SYNC	&	6	F	V		
0 1 1 1 7	BELL	LEM	´ (APOS)	7	G	W		
1 0 0 0 8	FE_0	S0	(	8	H	X		
1 0 0 1 9	HT/SK	S1	)	9	I	Y		
1 0 1 0 10	LF	S2	*	:	J	Z		
1 0 1 1 11	VT	S3	+	;	K	[		↓
1 1 0 0 12	FF	S4	, (COMMA)	<	L	\		ACK
1 1 0 0 13	CR	S5	-	=	M	]		①
1 1 1 0 14	SO	S6	.	>	N	↑		ESC
1 1 1 1 15	SI	S7	/	?	O	←	↓	DEL

① Unassigned Control

Table D-2

USASCII X3.4-1967

Bits b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1 Row \ Column	0	1	2	3	4	5	6	7
0 0 0 0 0	NUL	DLE	SP	0	@	P	`	p
0 0 0 1 1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0 2	STX	DC2	"	2	B	R	b	r
0 0 1 1 3	ETX	DC3	#	3	C	S	c	s
0 1 0 0 4	EOT	DC4	$	4	D	T	d	t
0 1 0 1 5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0 6	ACK	SYN	&	6	F	V	f	v
0 1 1 1 7	BEL	ETB	´	7	G	W	g	w
1 0 0 0 8	BS	CAN	(	8	H	X	h	x
1 0 0 1 9	HT	EM	)	9	I	Y	i	y
1 0 1 0 10	LF	SUB	*	:	J	Z	j	z
1 0 1 1 11	VT	ESC	+	;	K	[	k	{
1 1 0 0 12	FF	FS	,	<	L	\	l	|
1 1 0 1 13	CR	GS	-	=	M	]	m	}
1 1 1 0 14	SO	RS	.	>	N	^	n	~
1 1 1 1 15	SI	US	/	?	O	_	o	DEL

Table D-3

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 / USASCII X3.4 – 1967	NAME/FUNCTION
0/0	NULL / NUL	Null: The all zeros character which may serve to accomplish time fill and media fill.
0/1	SOM	Start of Message: It is used in conjunction with EOA, EOM, and EOT for messages on tapes where the message is to be sent automatically.
	SOH	Start of Heading: A communication control character used at the beginning of a sequence of characters which constitute a machine-sensible address or routing information. Such a sequence is referred to as the "Heading." An STX character has the effect of terminating a heading.
0/2	EOA	End of Address: This character, together with SOM, will be used to define the section of perforated tape in which the call-directing codes of the addressee are contained.
	STX	Start of Text: A communication control character which precedes a sequence of characters that are to be treated as an entity and entirely transmitted through to the ultimate destination. Such a sequence is referred to as "text." STX may be used to terminate a sequence of characters started by SOH.
0/3	EOM	End of Message: It may be used to separate individual messages which are sent in sequence on a single transmission between two stations (see SOM).
	ETX	End of Text: A communication control character used to terminate a sequence of characters started with STX and transmitted as an entity.
0/4	EOT / EOT	End of Transmission: A communication control character used to indicate the conclusion of a transmission which may have contained one or more texts and any associated headings.
0/5	WRU / ENQ	Enquiry: A communication control character used in data communication systems as a request for a response from a remote station. It may be used as a "Who Are You" (WRU) to obtain indentification, or may be used to obtain station status, or both.
0/6	RU	Are You: Use of this character for confirmation type of answer back has been discontinued until a more suitable arrangement can be devised.
	ACK	Acknowledge: A communication control character transmitted by a receiver as an affirmative response to a sender.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
0/7	BELL BELL	Bell: A character for use when there is a need to call for human attention. It may control alarm or attention devices.
0/8	FE BS	Backspace: A format effector that controls the movement of the printing mechanism one print position backward on the same print line.
0/9	HT/SK HT	Horizontal Tabulation: A format effector that controls the movement of the printing mechanism to the next in a series of predetermined positions along the print line. (Applicable also to the skip function on punched cards.)
0/10	LF LF	Line Feed: A format effector that controls the movement of the paper one line at a time.
0/11	VT VT	Vertical Tabulation: A format effector that controls the movement of paper to the next in a series of predetermined print lines.
0/12	FF FF	Form Feed: A format effector that controls the movement of the printing position to the first predetermined printing line on the next form or page.
0/13	CR CR	Carriage Return: A format effector that controls the movement of the print mechanism to the first print position on the same print line.
0/14	SO SO	Shift Out: A control character indicating that the code combinations that follow shall be interpreted as outside of the character set of the standard code table until a Shift In character is reached.
0/15	SI SI	Shift In: A control character indicating that the code combinations that follow shall be interpreted according to the standard code table.
1/0	DC_0 DLE	Data Link Escape: A communication control character that will change the meaning of a limited number of contiguously following characters. It is used exclusively to provide supplementary controls in data communication networks.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 / USASCII X3.4 – 1967	NAME/FUNCTION
1/1 1/2 1/3 1/4	DC_1 DC_2 DC_3 DC_4	Device Controls: DC_1 (X-ON) turns the tape reader ON and DC_3 (X-OFF) turns the tape reader OFF in Models 33 and 35. DC_2 and DC_4 can be used as PUNCH–ON and PUNCH–OFF controls.
	DC_1 DC_2 DC_3 DC_4	Device Controls: Characters for the control of ancillary devices associated with data processing or telecommunication systems, more especially switching devices ON or OFF. (If a single "stop" control is required to interrupt or turn off ancillary devices, DC is the preferred assignment.
1/5	ERR / NAK	Negative Acknowledge: A communication control character transmitted by a receiver as a negative response to the sender.
1/6	SYN / SYN	Synchronous Idle: A communication control character used by a sychronous transmission system in the absence of any other character to provide a signal from which synchronism may be achieved or retained.
1/7	LEM	Logical End of Media: Used to indicate the end of usable information, as in "End-of-Card".
	ETB	End of Transmission Block: A communication control character used to indicate the end of a block of data for communication purposes. ETB is used for blocking data where the block structure is not necessarily related to the processing format.
1/8	SO	Information Separators.
	CAN	Cancel: A control character used to indicate that the data with which it is sent is in error or is to be disregarded.
1/9	S1	Information Separators.
	EM	End of Medium: A control character associated with the sent data which may be used to identify the physical end of the medium, or the end of the used, or wanted, portion of information recorded on a medium. (The position of this character does not necessarily correspond to the physical end of the medium).
1/10	S2	Information Separator.
	SUB	Substitute: A character that may be substituted for a character which is determined to be invalid or in error.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 –1963 USASCII X3.4 – 1967	NAME/FUNCTION
1/11	S3 ESC	Information Separator. Escape: A control character intended to provide code extension (supplementary characters) in general information interchange. The Escape character itself is a prefix affecting the interpretation of a limited number of contiguously following characters.
1/12 1/13 1/14 1/15	S4 S5 S6 S7 FS GS RS US	Information Separators. File Separator, Group Separator, Record Separator, and Unit Separator: These information separators may be used within data in optional fashion, except that their hierarchical relationship shall be: FS is the most inclusive, then GS, then RS, and US is least inclusive. (The content and length of a File, Group, Record or Unit are not specified.)
2/0	SP SP	Space: A normally non-printing graphic character used to separate words. It is also a format effector which controls the movement of the printing position, one printing position forward.
2/1	! !	Exclamation Point.
2/2	” ”	Quotation Marks (Diaeresis).
2/3	# #	Number Sign.
2/4	$ $	Dollar Sign.
2/5	% %	Percent.
2/6	& &	Ampersand.
2/7	’ ’	Apostrophe (Closing Single Quotation Mark; Acute Accent).

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 - 1963 USASCII X3.4 – 1967	NAME/FUNCTION
2/8	((	Opening Parenthesis.
2/9	))	Closing Parenthesis
2/10	* *	Asterisk
2/11	+ +	Plus.
2/12	, ,	Comma (Cedilla).
2/13	- -	Hyphen (Minus).
2/14	. .	Period (Decimal Point).
2/15	/ /	Slant (Slash).
3/0	0 0	Figure Zero.
3/1	1 1	Figure One.
3/2	2 2	Figure Two.
3/3	3 3	Figure Three.
3/4	4 4	Figure Four.
3/5	5 5	Figure Five.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
3/6	6 6	Figure Six.
3/7	7 7	Figure Seven.
3/8	8 8	Figure Eight.
3/9	9 9	Figure Nine.
3/10	: :	Colon.
3/11	; ;	Semicolon.
3/12	< <	Less Than.
3/13	= =	Equals.
3/14	> >	Greater Than.
3/15	? ?	Question Mark.
4/0	@ @	Commercial At.
4/1	A A	Upper Case Letter A.
4/2	B B	Upper Case Letter B.
4/3	C C	Upper Case Letter C.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
4/4	D D	Upper Case Letter D.
4/5	E E	Upper Case Letter E.
4/6	F F	Upper Case Letter F.
4/7	G G	Upper Case Letter G.
4/8	H H	Upper Case Letter H.
4/9	I I	Upper Case Letter I.
4/10	J J	Upper Case Letter J.
4/11	K K	Upper Case Letter K.
4/12	L L	Upper Case Letter L.
4/13	M M	Upper Case Letter M.
4/14	N N	Upper Case Letter N.
4/15	O O	Upper Case Letter O.
5/0	P P	Upper Case Letter P.
5/1	Q Q	Upper Case Letter Q.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
5/2	R R	Upper Case Letter R.
5/3	S S	Upper Case Letter S.
5/4	T T	Upper Case Letter T.
5/5	U U	Upper Case Letter U.
5/6	V V	Upper Case Letter V.
5/7	W W	Upper Case Letter W.
5/8	X X	Upper Case Letter X.
5/9	Y Y	Upper Case Letter Y.
5/10	Z Z	Upper Case Letter Z.
5/11	[[	Opening Bracket.
5/12	\ \	Reverse Slant,
5/13	]]	Closing Bracket.
5/14	↑ ^	Exponentiation or Up Arrow. Circumflex.
5/15	← –	Replace by or Left Arrow. Underline.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
6/0		Unassigned.
	`	Grave Accent (Opening Single Quotation Mark).
6/1		Unassigned.
	a	Lower Case Letter a.
6/2		Unassigned.
	b	Lower Case Letter b.
6/3		Unassigned.
	c	Lower Case Letter c.
6/4		Unassigned.
	d	Lower Case Letter d.
6/5		Unassigned.
	e	Lower Case Letter e.
6/6		Unassigned.
	f	Lower Case Letter f.
6/7		Unassigned.
	g	Lower Case Letter g.
6/8		Unassigned.
	h	Lower Case Letter h.
6/9		Unassigned.
	i	Lower Case Letter i.
6/10		Unassigned.
	j	Lower Case Letter j.
6/11		Unassigned.
	k	Lower Case Letter k.
6/12		Unassigned.
	l	Lower Case Letter l.
6/13		Unassigned.
	m	Lower Case Letter m.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 USASCII X3.4 – 1967	NAME/FUNCTION
6/14		Unassigned.
	n	Lower Case Letter n.
6/15		Unassigned.
	o	Lower Case Letter o.
7/0		Unassigned.
	p	Lower Case Letter p.
7/1		Unassigned.
	q	Lower Case Letter q.
7/2		Unassigned.
	r	Lower Case Letter r.
7/3		Unassigned.
	s	Lower Case Letter s.
7/4		Unassigned.
	t	Lower Case Letter t.
7/5		Unassigned.
	u	Lower Case Letter u.
7/6		Unassigned.
	v	Lower Case Letter v.
7/7		Unassigned.
	w	Lower Case Letter w.
7/8		Unassigned.
	x	Lower Case Letter x.
7/9		Unassigned.
	y	Lower Case Letter y.
7/10		Unassigned.
	z	Lower Case Letter z.
7/11		Unassigned.
	{	Opening Brace.

Table D-3 (cont)

1963, 1967 USASCII Characters

COLUMN / ROW	CHARACTER	
	USASCII X3.4 – 1963 / USASCII X3.4 – 1967	NAME/FUNCTION
7/12	ACK	Acknowledge: A communication control character transmitted by a receiver as an affirmative response to a sender.
	|	Vertical Line.
7/13		Unassigned Control.
	}	Closing Brace.
7/14	ESC	Mode shift character used to indicate a departure from the standard set of basic characters; e.g., used to shift from upper to lower case letters.
		Overline (Tilde; General Accent)
7/15	DEL / DEL	Delete: This character is used primarily to "erase" or "obliterate" erroneous or unwanted characters in perforated tape. (In the strict sense, DEL is not a control character.)

TABLE D-4

B 2500/B 3500
EXTENDED BINARY CODED DECIMAL INTERCHANGE CODES (EBCDIC)

CARD, 9-TRACK MAGNETIC TAPE, DISK AND MEMORY* FORMATS

BITS b8 b7 b6 b5 →	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
b4 b3 b2 b1 ROW ↓ COL →	0	1	2	3	4	5	6	7	8	9	10 (A)	11 (B)	12 (C)	13 (D)	14 (E)	15 (F)
0 0 0 0 0	NUL 12-0-9-8-1	DLE 12-11-9-8-1			SP BLANK	& 12	- 11						PZ (+) 12-0	MZ (!) 11-0		0 0
0 0 0 1 1	SOH 12-9-1	DC1 11-9-1					/ 0-1		a 12-0-1	j 12-11-1			A 12-1	J 11-1		1 1
0 0 1 0 2	STX 12-9-2	DC2 11-9-2		SYN 9-2					b 12-0-2	k 12-11-2	s 11-0-2		B 12-2	K 11-2	S 0-2	2 2
0 0 1 1 3	ETX 12-9-3	DC3 11-9-3							c 12-0-3	l 12-11-3	t 11-0-3		C 12-3	L 11-3	T 0-3	3 3
0 1 0 0 4									d 12-0-4	m 12-11-4	u 11-0-4		D 12-4	M 11-4	U 0-4	4 4
0 1 0 1 5	HT 12-9-5	NL 11-9-5	LF 0-9-5						e 12-0-5	n 12-11-5	v 11-0-5		E 12-5	N 11-5	V 0-5	5 5
0 1 1 0 6		BS 11-9-6	ETB 0-9-6						f 12-0-6	o 12-11-6	w 11-0-6		F 12-6	O 11-6	W 0-6	6 6
0 1 1 1 7	DEL 12-9-7		ESC 0-9-7	EOT 9-7					g 12-0-7	p 12-11-7	x 11-0-7		G 12-7	P 11-7	X 0-7	7 7
1 0 0 0 8		CAN 11-9-8							h 12-0-8	q 12-11-8	y 11-0-8		H 12-8	Q 11-8	Y 0-8	8 8
1 0 0 1 9		EM 11-9-8-1							i 12-0-9	r 12-11-9	z 11-0-9		I 12-9	R 11-9	Z 0-9	9 9
1 0 1 0 10 (A)					[12-8-2	] 11-8-2	12-11	: 8-2								
1 0 1 1 11 (B)	VT 12-9-8-3				. 12-8-3	$ 11-8-3	, 0-8-3	# 8-3								
1 1 0 0 12 (C)	FF 12-9-8-4	FS 11-9-8-4		DC4 9-8-4	< 12-8-4	* 11-8-4	% 0-8-4	@ 8-4								
1 1 0 1 13 (D)	CR 12-9-8-5	GS 11-9-8-5	ENQ 0-9-8-5	NAK 9-8-5	(12-8-5	) 11-8-5	(US) 0-8-5	8-5								
1 1 1 0 14 (E)	SO 12-9-8-6	RS 11-9-8-6	ACK 0-9-8-6	9-8-6	+ 12-8-6	; 11-8-6	> 0-8-6	= 8-6								
1 1 1 1 15 (F)	SI 12-9-8-7	US 11-9-8-7	BEL 0-9-8-7	SUB 9-8-7	| 12-8-7	¬ 11-8-7	? 0-8-7	" 8-7					DELIMETER 12-0-9-8-7			

$b_8\ b_7\ b_6\ b_5 / b_4\ b_3\ b_2\ b_1$

*INTERNAL COLLATING SEQUENCE = 0 0 0 0 / 0 0 0 0 TO 1 1 1 1 / 1 1 1 1

TABLE D-4 (cont'd)

CONTROL AND SPECIAL CODES

NUL — NULL - The all-zeros character which may serve to accomplish time fill and media fill.

SOH — START OF HEADING - A communication control character used at the beginning of a sequence of characters which constitutes a machine-sensible address or routing information. Such a sequence is referred to as the "heading." An STX character has the effect of terminating a heading.

STX — START OF TEXT - A communication control character which precedes a sequence of characters that is to be treated as an entity and entirely transmitted through to the ultimate destination. Such a sequence is referred to as "TEXT." STX may be used to terminate a sequence of characters started by SOH.

ETX — END OF TEXT - A communication control character used to terminate a sequence of characters started with STX and transmitted as an entity.

HT — HORIZONTAL TABULATION - A format effector which controls the movement of the printing position to the next in a series of predetermined positions along the printing line. (Applicable also to display devices and the SKIP function on punched cards.)

DEL — DELETE - This character is used primarily to "ERASE" or "OBLITERATE" erroneous or unwanted characters in perforated tape. (In the strict sense, DEL is not a control character.)

VT — VERTICAL TABULATION - A format effector which controls the movement of the printing position to the next in a series of predetermined printing lines. (Applicable also to display devices.)

FF — FORM FEED - A format effector which controls the movement of the printing position to the first predetermined printing line on the next form or page. (Applicable also to display devices.)

CR — CARRIAGE RETURN - A format effector which controls the movement of the printing position to the first printing position on the same printing line. (Applicable also to display devices.)

SO — SHIFT OUT - A control character indicating that the code combinations which follow shall be interpreted as outside of the character set of the Standard Code Table until a shift in character is reached.

SI — SHIFT IN - A control character indicating that the code combinations which follow shall be interpreted according to the Standard Code Table.

DLE — DATA LINK ESCAPE - A communication control character which will change the meaning of a limited number of contiguously following characters. It is used exclusively to provide supplementary controls in data communication networks.

DC1, DC2, DC3, DC4 — DEVICE CONTROLS - Characters for the control of ancillary devices associated with Data Processing or Telecommunication Systems, more especially switching devices "ON" or "OFF." (If a single "STOP" control is required to interrupt or turn off ancillary devices, DC4 is the preferred assignment.)

NL — NEW LINE - A format effector which causes both Carriage Return and Line Feed.

BS — BACKSPACE - A format effector which controls the movement of the printing position one printing space backward on the same printing line. (Applicable also to display devices.)

CAN — CANCEL - A control character used to indicate that the data with which it is sent is in error or is to be disregarded.

EM — END OF MEDIUM - A control character associated with the sent data which may be used to identify the physical end of the medium, or the end of the used, or wanted, portion of information recorded on a medium. (The position of this character does not necessarily correspond to the physical end of the medium.)

FS — FILE SEPARATOR
GS — GROUP SEPARATOR
RS — RECORD SEPARATOR
US — UNIT SEPARATOR

These information separators may be used within data in optional fashion, except that their hierarchical relationship shall be: FS is the most inclusive, then GS, then RS, and US is least inclusive. (The content and length of a File, Group, Record, or Unit are not specified.)

LF — LINE FEED - A format effector which controls the movement of the printing position to the next printing line. (Applicable also to display devices.)

ETB — END OF TRANSMISSION BLOCK - A communication control character used to indicate the end of a block of data for communication purposes. ETB is used for blocking data where the block structure is not necessarily related to the processing format.

ESC — ESCAPE - A control character intended to provide code extension (supplementary characters) in General Information Interchange. The escape character itself is a prefix affecting the interpretation of a limited number of contiguously following characters.

ENQ — ENQUIRY - A communication control character used in Data Communication Systems as a request for a response from a Remote Station. It may be used as a "WHO YOU ARE" (WRU) to obtain identification, or may be used to obtain Station Status, or both.

ACK — ACKNOWLEDGE - A communication control character transmitted by a receiver as an affirmative response to a sender.

BEL — BELL - A character for use when there is a need to call for human attention. It may control alarm or attention devices.

SYN — SYNCHRONOUS IDLE - A communication control character used by a synchronous transmission system in the absence of any other character to provide a signal from which synchronism may be achieved or retained.

EOT — END OF TRANSMISSION - A communication control character used to indicate the conclusion of a transmission, which may have contained one or more texts and any associated headings.

NAK — NEGATIVE ACKNOWLEDGE - A communication control character transmitted by a receiver as a negative response to the sender.

SUB — SUBSTITUTE - A character that may be substituted for a character which is determined to be invalid or in error.

SP — SPACE - A normally non-printing graphic character used to separate words. It is also a format effector which controls the movement of the printing position, one printing position forward. (Applicable also to display devices.)

OTHER CODES

PZ — PLUS ZERO
MZ — MINUS ZERO

Code 0110 1110, is never obtained from a BCL plus sign; plus zero (PZ) code 1100 0000 prints as a plus sign. Minus zero (MZ) prints as an }. Choice of graphic for PZ and MZ may vary from system to system. The choice of styling (} or }) for graphic code 0100 1111 may also vary from system to system.

APPENDIX E
DATA COMMUNICATIONS TRANSLATION TABLES

This appendix provides tables for translating Baudot code to EBCDIC code, and PTTC/6 code to EBCDIC code.

BAUDOT TO EBCDIC TRANSLATION TABLE

Baudot		EBCDIC	
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic
00	BLK	00	NULL
01	E	C5	E
02	LF	0A	LF
03	A	C1	A
04	SPACE	40	SPACE
05	S	E2	S
06	I	C9	I
07	U	F4	U
08	CR	0D	CR
09	D	C4	D
0A	R	D9	R
0B	J	D1	J
0C	N	D5	N
0D	F	C6	F
0E	C	C3	C
0F	K	D2	K
10	T	E3	T
11	Z	F9	7
12	L	D3	L
13	W	E6	W
14	H	C8	H
15	Y	E8	Y
16	P	D7	P
17	Q	D8	Q
18	0	D6	0
19	B	C2	B
1A	G	C7	G
1B	FIGS	02	STX
1C	M	D4	M
1D	X	E7	X
1E	V	E5	V
1F	LTRS	7C	@
20	BLK	00	NULL
21	3	F3	3
22	LF	0A	LF
23	-	60	-
24	SPACE	40	SPACE
25	BELL	07	BELL
26	8	F8	8
27	7	F7	7
28	CR	0D	CR
29	$	5B	$
2A	4	F4	4
2B	,	6B	,
2C	7/8	5E	:

BAUDOT TO EBCDIC TRANSLATION TABLE (cont)

Baudot		EBCDIC	
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic
2D	1/4	7D	[
2E	1/8	4F	+
2F	1/2	5C	*
30	5	F5	5
31	”	7F	”
32	3/4	5D	)
33	2	F2	2
34	DIMOND	6F	6
35	6	F6	6
36	0	F0	0
37	1	F1	1
38	9	F9	9
39	5/8	4D	(
3A	&	50	&
3B	FIGS	02	STX
3C	.	4B	.
3D	/	61	/
3E	3/8	6C	%
3F	LTRS	7C	@

PTTC/6 TO EBCDIC TRANSLATION TABLE

PTTC/6		EBCDIC		1050 Standard Card Code
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic	
Lower Case				
00	SPACE	40	SPACE	
01	1	F1	1	1
02	2	F2	2	2
03	3	F3	3	3
04	4	F4	4	4
05	5	F5	5	5
06	6	F6	6	6
07	7	F7	7	7
08	8	F8	8	8
09	9	F9	9	9
0A	0	F0	0	0
0B	= or #	7B	#	8-3
0C	PN	11	DC1	9-4
0D	Rs	14	DC4	9-5
0E	UC	36		9-6
0F	EOT	04	EOT	9-7
10	@	7C	@	8-4
11	/	61	/	0-1
12	S	A2	S	0-2
13	T	A3	T	0-3

PTTC/6 TO EBCDIC TRANSLATION TABLE (cont)

PTTC/6		EBCDIC		1050 Standard Card Code
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic	
14	U	A4	U	0-4
15	V	A5	V	0-5
16	W	A6	W	0-6
17	X	A7	X	0-7
18	Y	A8	Y	0-8
19	Z	A9	Z	0-9
1A	≠	6D	USCOR≠	0-8-2
1B	,	6D	,	0-8-3
1C	BY	24		0-9-4
1D	LF	0A	LF	0-9-5
1E	EOR	17	FTR	0-9-6
1F	PRE	01	SOH	0-9-7
20	-	60	-	11
21	J	91	J	11-1
22	K	92	K	11-2
23	L	93	K	11-3
24	M	94	M	11-4
25	N	95	N	11-5
26	O	96	)	11-6
27	P	97	P	11-7
28	Q	98	Q	11-8
29	R	99	R	11-9
2A	M7	7D	APOS≥	11-0
2B	$	5B	$	11-8-3
2C	RFS	0C	FF	11-9-4
2D	NL	0D	CR	11-9-5
2E	BS	08	BS	11-9-6
2F	IL	00	NULL	11-9-7
30	+ or &	4E	+	12
31	A	81	A	12-1
32	B	82	B	12-2
33	C	83	C	12-3
34	D	84	D	12-4
35	E	85	E	12-5
36	F	86	F	12-6
37	G	87	G	12-7
38	H	88	H	12-8
39	I	89	I	12-9
3A	PZ	50	&	12-0
3B	.	4B	.	12-8-3
3C	PF	12	DC2	12-9-4
3D	HT	09	HT	12-9-5
3E	LC	1A	SS	12-9-6
3F	DEL	FF	DEL	12-9-7
Upper Case				
40	SPACE	40	SPACE	

PTTC/6 TO EBCDIC TRANSLATION TABLE (cont)

PTTC/6		EBCDIC		1050 Standard Card Code
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic	
41	>	6E	>	1
42	)	5D	)	2
43	;	5E	;	3
44	SBLANK	4A	CENT	4
45	(	4D	(	5
46	:	7A	:	6
47	”	7F	”	7
48	*	50	*	8
49	[	70	[	9
4A	]	6A	]	0
4B	SEGMRK	7E	=	8-3
4C	PN	11	DC1	9-4
4D	RS	14	DC4	9-5
4E	UC	36		9-6
4F	EOT	04	EOT	9-7
50	DELTA	5F	NOT<	8-4
51	QUES	6F	QUES	0-1
52	S	E2	S	0-2
53	T	E3	T	0-3
54	U	E4	U	0-4
55	V	E5	V	0-5
56	W	E6	W	0-6
57	X	E7	X	0-7
58	Y	68	Y	0-8
59	Z	E9	Z	0-9
5A	GRPMRK	6D	USCOR≠	0-8-2
5B	,	6B	,	0-8-3
5C	BY	24		0-9-4
5D	LF	0A	LF	0-9-5
5E	EOB	17	ETB	0-9-6
5F	PRF	01	SOH	0-9-7
60	BACK/	60	-	11
61	J	D1	J	11-1
62	K	D2	K	11-2
63	L	D3	L	11-3
64	M	D4	M	11-4
65	N	D5	N	11-5
66	O	D6	O	11-6
67	P	D7	P	11-7
68	Q	D8	Q	11-8
69	R	D9	R	11-9
6A	GAMMA	7D	APOS>	11-0
6B	V.BAR	4F	V.BAR←	11-8-3
6C	RES	0C	FF	11-9-4
6D	NL	0D	CR	11-9-5
6E	BS	08	RS	11-9-6
6F	IL	00	NULL	11-9-7

PTTC/6 TO EBCDIC TRANSLATION TABLE (cont)

PTTC/6		EBCDIC		1050 Standard Card Code
Decimal Equivalent	Graphic	Decimal Equivalent	Graphic	
70	<	40	<	12
71	A	C1	A	12-1
72	B	C2	B	12-2
73	C	C3	C	12-3
74	D	C4	D	12-4
75	E	C5	E	12-5
76	F	C6	F	12-6
77	G	C7	G	12-7
78	H	C8	H	12-8
79	I	C9	I	12-9
7A	SQ.RT	6C	%	12-0
7B	.	4B	.	12-8-3
7C	PF	12	DC2	12-9-4
7D	HT	09	HT	12-9-5
7E	LC	1A	SS	12-9-6
7F	DEL	FF	DEL	12-9-7

APPENDIX F
DATA COMMUNICATIONS CONTROL CODES

The tables in this appendix identify the codes that are used with remote terminals for information interchange with the B 2500/B 3500 data communications network. Line control procedures and codes vary for each of these terminals. Also listed in the tables are the functions performed by the control and the applicable control code(s) used to generate that particular function.

USASCII X3.4-1967 TRANSMISSION CONTROL CODES

Graphic	Function	Code 7654321
SOH	Start of heading	0000001
STX	Start of text	0000010
ETX	End of text	0000011
EOT	End of transmission	0000100
ENQ	Enquiry	0000101
ACK	Acknowledge	0000110
DLE	Data link escape	0010000
DC1	Device control	0010001
DC2	Device control	0010010
NAK	Negative acknowledge	0010101
SYN	Synchronous idle	0010100
ETB	End of transmission block	0010111
NUL	Null	0000000

ASCII X3.4-1963 TRANSMISSION CONTROL CODES

Graphic	Function	Code 7654321
SOM	Start of message	0000001
EOA	End of address	0000010
EOM	End of message	0000011
EOT	End of transmission	0000100
WRU	Who are you	0000101
RU	Are you	0000110
SYNC	Synchronous idle	0010110
ERR	Error	0010101
ACK	Acknowledge	1111100
DC1	(XON)	0010001
\	Reverse slash	1011100
*	Asterisk	0101010

ASCII A CONTROL CODE FUNCTIONS

Function	Code
Start of text	Any code
End of text	ETX (EOM), DC1 (XON), ENQ (WRU), or EOT (EOT)
End of transmission	EOT (EOT)
Enquiry	ENQ (WRU)

NOTE — Codes in parentheses are 1963 codes.

ASCII B CONTROL CODE FUNCTIONS

Function	Code
Start of text	Any code except * or \
End of text	ETX (EOM) or EOT (EOT)
Response	NONE (ACK)
Negative response	NONE (ACK)
Timing select	SOH (SOM)
	NOTE When SOM is used as start-of-text, the time-out is changed from 5 to 25 seconds.

NOTE

Codes in parentheses are 1963 codes.

ASCII C CONTROL CODE FUNCTIONS

Function	Code
Start of text	SOH (SOM) or STX (EOA)
End of text	ETX (EOM) or ETB (LEM)
Response	ACK (RU), NAK (ERR), EOT (EOT), or ENQ (WRU)
Enquiry	ENQ (WRU)
Syn	SYN (SYNC)

ASCII D CONTROL CODE FUNCTIONS

Function	Code
Start of text	SOH (SOM) or STX (EOA)
End of text	ETX (EOM) or ETB (LEM)
Response	ACK (RU), NAK (ERR), EOT, DC1 or DC2
Enquiry	ENQ (WRU)
Syn	SYN (SYNC)

IBM PTTC/6 TRANSMISSION CONTROL CODES

Function	Code BA8421
EOT (end of transmission)	001111
EOA (end of address – #)	001011
EOB (end of block)	011110
Positive response-polling (#)	001011
Positive response-addressing (.)	111011
Positive response-inquiry (#)	001011
Negative response-polling (-)	100000
Negative response-addressing (-)	100000
Positive ACK-error control (.)	111011
Negative ACK-error control (-)	100000
Upper case	001110
Lower case	111110

PTTC/6 CONTROL CODE FUNCTIONS

Function	Code
Start of text	EOA
End of text	EOB
End of transmission	EOT
Response	. (period) or - (hyphen)
Negative response	- (hyphen)
Upper case shift	U.C.
Lower case shift	L.C.

BAUDOT TRANSMISSION CONTROL CODES

Graphic	Code 54321
M	11100
V	11110
H	10100
S	00101
Figures	11011
Letters	11111

BAUDOT A CONTROL CODE FUNCTIONS

Function	Code
Start of text	Any code but B
End of text (read)	H
End of text (write)	H with a flag bit
Response	V or letters

BAUDOT A CONTROL CODE FUNCTIONS (cont)

Function	Code
Negative response	V
Upper case shift	Figures
Lower case shift	Letters
Enquiry	Letters

NOTE

In addition to the control code sensitivity defined for each adapter, the switched line adapters are sensitive to a 4-bit end-of-number code (1100) when dialing. The EON code is not transferred to the 801A1 ACU.

APPENDIX G
TAPE MARKS

9-CHANNEL TAPE MARKS

The following is an explanation of Burroughs 9-channel tape marks and is applicable to both 9-channel clustered and free-standing tape units.

200-BPI Tape Mark

This tape mark is a one-character record consisting of a 1-bit in tracks 2, 3, and 8 being ON. Three character spaces follow the tape mark and then a longitudinal parity character is written.

800-BPI Tape Mark

The tape mark for 1600-BPI is a special control mark, but followed by seven character spaces, and then a longitudinal parity character is written. There is no CRC (Cyclic Redundancy Check) character.

200-BPI and 800-BPI

The one-character configuration for both of the above densities is the EBCDIC DC3 character (0001 0011).

1600-BPI Tape Mark

The tape mark for 1600 BPI is a special control block consisting of from 64 to 256 flux reversals (3200 flux changes per inch – FCI) in tracks 2, 5, and 8. Tracks 1, 4, and 7, in any combination, may be DC erased or recorded in the manner stated for tracks 2, 5, and 8. All combinations shall be treated as an EBCDIC DC3 character.

7-CHANNEL TAPE MARKS

End-of-Record Mark

This mark is the last character in a record and is coded as 001111 (0F). This character is included in the longitudinal check character.

End-of-File Mark

This mark is written after the record-gap following the last record on tape. The mark is two characters long and is coded as 001111 111111 (0F3F), followed by a longitudinal check character.

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