Burroughs

FIELD ENGINEERING TRAINING

Course No. BMG 387555
INT'L 274308

B 9489
INDUSTRY COMPATIBLE MINI-DISK (ICMD)

TRAINING COURSE

WORKBOOK

June 1979 Form 2101333

Printed in U. S. America

B 9489 ICMD FIELD ENGINEERING TRAINING PROGRAM

COURSE REQUIREMENTS

TRAINING PREREQUISITES :

Ability to operate MTR routines on the available host system

and

Principles of Micro-Based Computer Systems

or

Business Machine Fundamentals: Course Number 300002, part of introduction to Field Engineering Form No. 1075602 (BMG)

COURSE DURATION:

The course is self-paced. Students should normally complete the course within 15 hours. A guide to the approximate time required to complete each lecture is given in the Student Introduction.

AUDIO-VISUAL REQUIREMENTS:

35mm Slide Projector	Preferably with remote control
Cassette Tape Player	Preferably with tape "pause" control and a tape position counter.
Screen	

In addition to this package, the following materials are required to complete the B 9468 ICMD Training Program.

B 9489 ICMD FIELD ENGINEERING TRAINING PROGRAM

TECHNICAL LITERATURE:

Field Engineering Technical Manual:

Volume 1	Form 1084308
Volume 2 (Parts Catalogue)	Form 1101771

Field Test and Reference Documentation Package.

Current RIN's/LIN's and ATI's.

Host system documentation and MTR.

HARDWARE AND TOOLS:

Host System	Any available unit with controller/ adaptor.
B 9489-5 ICMD Unit	The unit may be mounted in a host system or be part of B 9489-15, -16, -17 or -18 free-standing unit connected to host system.
Alignment Diskette	2029 1852
Standard Tool Roll	
BMD 1250 or Equivalent	
Oscilloscope	Tektronix 453 or Equivalent

MACHINE SUPPLIES:

Diskette	43-0010-081

COURSE SUPERVISOR INTRODUCTION

The B 9489 ICMD Field Engineering Training Program is a self-study course requiring a minimum of supervision in either a Branch or Training Center environment. The course divides into three lectures, each using a variety of instructional methods to give the student the required skills and knowledge. The course should be supervised by a Training Instructor, Branch FE Manager or assigned representative. The Course Supervisor responsibilities are outlined as follows:

TRAINING SITE:

Select an area which is free from distraction and provides a sufficiently large area for the student to work comfortably. To view the slides, it is necessary to reduce the level of light in the work area.

COURSE MATERIALS:

The student must be provided with all the materials listed in the Course Requirements section of this manual.

Any available style of host system can be used to drive the ICMD unit during this course. However, the student requires the ability to operate the ICMD MTR routines on the available host system and may require assistance to achieve this.

DOCUMENTATION:

The blue course binder contains a master copy of the workbook and lecture material. Order one copy of the document per student. The student should answer the review tests on the question pages provided in the ordered copy. Do not use the master. The student is allowed to retain the copy (without the question pages) for future reference.

REVIEW TESTS:

Both Lecture 1 and Lecture 2 contain review tests which the Course Supervisor is required to grade. Although questions are numbered sequentially for the complete test, the tests are divided into several parts. Each part must be graded immediately on completion to identify any part of the preceding Lecture which the student should review.

THE ANSWER SHEETS FOR THE REVIEW TEST FOLLOW THIS INTRODUCTION AND MUST BE REMOVED BEFORE THE PACKAGE IS GIVEN TO THE STUDENT. THESE SHEETS ARE ONLY INCLUDED IN THE MASTER COPIES OF THE WORKBOOK.

After reviewing the test with the student, the Question/Answer pages must be retained by the course supervisor or destroyed.

PRACTICAL WORK:

The course contains a number of practical exercises requiring the student to disassemble, reassemble and adjust the unit. On completion of the course, a qualified Field Engineer must check the unit to ensure that it is correctly adjusted and operating to specification. Any deficiencies should be brought to the attention of the student for correction.

QUESTIONS:

The students are encouraged to determine the answers to any questions for themselves. If a question is asked which you are unable to answer, refer the question to a Training Center or other technical support facility for resolution.

COURSE CONTENT AND PRESENTATION:

Due to the variety of different controllers used by different host systems, this course does not include host system controllers or the optional medium/large system adaptor. These should be included in the host system training course.

The workbook contains copies of each of the Lecture scripts with black and white copies of each slide. This document is provided for personal reference by the student and cannot be used as a subsitute for the cassette and slide presentations.

COURSE RECORDS:

INTERNATIONAL -- Complete a Field Engineering Training Report (Form INT 1591) for each student. Distribute copies per instructions on form. Send additional copy to Subisidiary FE Training Manager when applicable.

BMG -- Upon completion of the course, a "Training Report" (Form 1902202) must be initiated for each student. These reports should be forwarded to:

BMG FE TRAINING ADMINISTRATION
WHQ-DETROIT, ROOM 2D22

Refer to F.M.M. 10.3.10 for further references. When these reports are received and processed, a "Certificate of Accomplishment" will be sent to each student.

REVIEW TEST ANSWERS

THE FOLLOWING REVIEW TEST ANSWER PAGES MUST BE REMOVED FROM THIS PACKAGE BEFORE IT IS GIVEN TO THE STUDENT.

REVIEW TEST ANSWERS — LECTURE 1

1. (b) One disk drive housed in the 44 inch cabinet.
2. (c) Reference the beginning of each track.
3. (a) True
4. (b) False
5. (e) 77
6. (e) 26
7. (d) Write the sector address on the diskette.
8. (e) A positive or negative going peak between clocks.
9. (a) 242,944 data bytes.

REVIEW TEST ANSWERS — LECTURE 2

1. (b) Allow for head load settle time.

2. (b) Indicates that the read/write head is at track 00.

3. (d) 43

4. False

5. (c) A false or logic 0 is indicated by a 5v signal level.

6. Write Enable (Any Order)
   Differential Amplification
   Phase Shift and Amplification
   Analogue to Digital Conversion

7. (e) Differential video amplifier

8. True

9. True

10. (d) Q2, Q3, U1, U2, U20

11. (b) Write Data

12. False

13. (Any Order)
    A write enable is issued when the head is not loaded
    Write data are sent at the wrong clock rate
    A write is issued and data not received within 450uS

14. (e) Q18

15. IC U16 Pin 4

16. (a) 3

(Continued on following page)

REVIEW TEST ANSWERS

LECTURE 2 CONTINUED

17. (e) 15 degrees

18. a. Track 00 Detector Output (Any Order)
    b. Phase "A" Active

19. a. Reset the stepper motor phase counter (Any Order)
    b. Reset the write fault latch

20. U3 (Any Order)
    Q5
    Q6
    CR3

21. True

22. (e) 170mS

23. U25 (Any Order)
    U27
    SW1

B 9489 ICMD FIELD ENGINEERING TRAINING PROGRAM

STUDENT INTRODUCTION

The B 9489 ICMD Field Engineering Training Program is an objective oriented course designed for self-study with minimum supervision.

COURSE GOAL:

On completion of this course, you will be able to install, maintain and repair to the component level, any configuration of B 9489 ICMD unit including the power supply incorporated in the free standing styles.

LECTURE OBJECTIVES:

Each Lecture is preceded by one or more Lecture Objectives. These objectives broadly define the knowledge and skills you will acquire during the following Lecture. Read each Lecture Objective carefully before proceding to the first Practice Objective.

PRACTICE OBJECTIVES:

Each Lecture is divided into sections. The activities within a section are designed to enable you to achieve each of the associated Practice Objectives. Read each Practice Objective carefully before proceding to the Practice.

PRACTICE:

The Practice lists the various tasks you are required to complete. A typical sequence will ask you to view part of the Lecture and then complete an exercise. This exercise may be a review test or a practical exercise. Complete each exercise in sequence.

REVIEW TESTS:

Complete each Review Test on the question sheets contained in the workbook. On completion of each Review Test, give your completed answers to the Course Supervisor for grading. Lecture 3 does not include a Review Test. There is no time limit for completion of the Review Tests. You may refer to any available documentation or equipment when completing your answers.

TIME ALLOCATION:

The course is self-paced. Dependent on your previous knowledge and local circumstances, the course will normally require less than 15 hours to complete.

QUESTIONS:

Should you have a question which you are unable to answer for yourself, make a note of the question and proceed with the Lecture -- you may find the answer in a later section. If, after completing the Lecture, you are still unable to find the answer, refer your question to the Course Supervisor.

START:

Check that you have all the equipment required to complete the course and proceed to Lecture 1 in the Study Guide.

LECTURE 1

READ THE STUDENT INTRODUCTION BEFORE STARTING

LECTURE INTRODUCTION:

The first Lecture divides into two sections:

i) The first section introduces the various B 9489 ICMD unit styles and options, examines the physical characteristics of the media giving attention to the need for correct handling and storage before describing operation of the unit.

ii) The second section describes the Industry Compatable diskette format and encoding method, concluding with a summary of the B 9489 ICMD units capacities and performance characteristics.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Identify the style and hardware options for any B 9489 ICMD Unit.

2. Identify the physical characteristics of the media.

3. Operate the B 9489 ICMD Unit observing proper media handling and storage procedures.

PRACTICE:

1. Listen to the cassette for Lecture 1 and view slides 1 to 34.

2. Remove a diskette from the protective envelope and locate the following: (DO NOT touch the recording surface)
   a) The index hole.
   b) The reinforced spindle hole.
   c) The read head slot.

3. Observing proper handling precautions, insert a diskette into a drive and determine that the unit is ready.

4. Complete the following Review Test.

REVIEW TEST LECTURE 1

1. The B 9489-15 unit consists of:

   a) Two disk drives housed in the 33 inch cabinet.
   b) One disk drive housed in the 44 inch cabinet.
   c) One disk drive housed in the 44 inch cabinet with an adaptor card.
   d) One disk drive housed in the 33 inch cabinet.
   e) One disk drive for housing in the host system cabinet.

2. The Index hole is used to:

   a) Register the diskette.
   b) Locate the diskette.
   c) Reference the beginning of each track.
   d) Enable the read/write head.
   e) Access the recording surface.

3. The write protect hole feature is not used by the Burroughs B 9489 ICMD Units.

   a) True
   b) False

4. Contaminated diskettes can be removed from the jacket and cleaned.

   a) True
   b) False

Give your answers to the Course Supervisor for grading. If any answer is incorrect, review the relevant part of the Lecture before continuing.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Identify the diskette media format and encoding method which determine that the media is Industry Compatable.

2. Relate the Industry Compatable media format and capacities to the performance characteristics of the B 9489 ICMD Unit.

PRACTICE:

1. Continue listening to the cassette for Lecture 1 and view slides 35 to 53.

2. Complete the following Review Test.

REVIEW TEST LECTURE 1

5. How many tracks are there on an ICMD diskette in total?

a) 26
b) 73
c) 64
d) 128
e) 77

6. How many sectors are there on each track?

a) 4
b) 16
c) 12
d) 8
e) 26

7. The primary function of the diskette initialization is to:

a) Align the read/write head with track 00.
b) Register and align the diskette in the drive unit.
c) Read the diskette error directory.
d) Write the sector addresses on the diskette.
e) Trim the inter track spaces.

(Continued on next page)

8. In the double frequency encoding method used, a data one bit is indicated in the read head output signal by:

   a) A positive going peak between clocks.
   b) A negative going peak between clocks.
   c) A positive or negative going peak between clocks.
   d) A positive level between clocks.
   e) A negative level between clocks.

9. The data capacity of the ICMD diskette is:

   a) 242,944 data bytes
   b) 401,016 data bytes
   c) 65,536 data bytes
   d) 129,072 data bytes
   e) 258,144 data bytes

LECTURE 2

LECTURE INTRODUCTION:

The second Lecture divides into two sections:

i) The first section identifies the physical locations and functions of the major components and sub-assemblies in the unit.

ii) The second section describes the theory of operation for the unit using block diagrams to relate the function of each area of logic to the schematic drawings.

READ THE FOLLOWING LECTURE OBJECTIVES

LECTURE OBJECTIVES

1. Interpret the unit schematics to determine the function and mode of operation of any part of the unit logic.

2. Given any unit logic failure, use your knowledge of the unit logic to supplement the unit MTR's.

3. Make measurements of the unit logic signals to determine correct or incorrect operation of any given circuit.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Locate and correctly identify the function of each major sub-assembly within the basic B 9489-5 unit.

2. Locate any given test point on the logic PCB.

3. Determine the number of head load and power on hours for any unit.

PRACTICE:

1. Listen to the cassette for Lecture 2 and view slides 1 to 10.

2. Locate the following sub-assemblies:

   Disk Load Arm
   Head Load Solenoid
   Read/Write Head
   Index Hole Detector

3. Observe the mechanical operation of the unit with the unit powered off by performing the following:

   - Open and close the door to observe the action of the Registration Cone.

   - Rotate the stepper motor screw shaft to observe the action of the Read/Write Head carriage assembly.

   - Press and release the Head Load Solenoid Clapper to observe the action of the Head Load Bail assembly.

PRACTICE (CONTINUED)

4. With the unit powered on and a diskette inserted, locate the test point on the logic PCB for the Index Pulse. (Refer to FETM Volume 1 Page 4-13.) Use a BDM 1250, or equivalent, to measure the frequency of the Index Pulse.

   Note: This test point is the output of the Index phototransistor which is not a TTL logic level. The peak voltage is approximately 4 volts.

5. On the unit with which you are working, determine:

   i) The number of head load hours to date.
   ii) The number of power on hours to date.

READ THE FOLLOWING PRACTICE OBJECTIVES

PRACTICE OBJECTIVES:

1. Identify and determine the correct function of any interface signal.

2. Determine the unit drive number for any ICMD unit.

PRACTICE:

1. Continue listening to the cassette for Lecture 2 and view slides 11 to 20.

2. Use the unit logic schematic to determine the unit drive number for your unit by observing the position of the dual in line package switches on the logic PCB.

3. Complete the following Review Test.

REVIEW TEST LECTURE 2

1. The Head Load command must be initiated 60 milliseconds before a read or write operation to:

   a) Register the diskette on the spindle.
   b) Allow for head load settling time.
   c) Ensure the Write Fault latch is reset.
   d) Give the head time to step to the required track.
   e) Provide time for the unit to sense the Index hole.

2. The Track 00 signal:

   a) Steps the read/write head to track 00.
   b) Indicates that the read/write head is at track 00.
   c) Reads data from track 00.
   d) Inhibits a write to track 00.
   e) Allows time for the read/write head to reach track 00.

3. The Low Current signal from the controller reduces the write current when a write operation is taking place on a track above:

   a) 24
   b) 34
   c) 36
   d) 43
   e) 47

(Continued on next page)

REVIEW TEST (CONTINUED)

4. Data written to the diskette is checked during a write operation by the Write fault logic.

   True/False

5. A convention used on the signal interface is:

   a) A false or logic 1 is indicated by a 5v signal level.
   b) A true or logic 1 is indicated by a 5v signal level.
   c) A false or logic 0 is indicated by a 5v signal level.
   d) A true or logic 0 is indicated by a 5v signal level.

Give your answers to the Course Supervisor for grading. If any answer is incorrect, review the relevant section of the lecture before continuing.

READ THE FOLLOWING PRACTICE OBJECTIVES

PRACTICE OBJECTIVES:

1. Determine the function and mode of operation of any part of the Read Logic.

2. Given any Read Logic failure, use your knowledge of the Read Logic to determine the cause of the failure.

PRACTICE:

1. Continue listening to the cassette for Lecture 2 and view slides 21 to 34.

2. Complete the following Review Test.

REVIEW TEST LECTURE 2

6. State the four main functional blocks of the Read Logic:

   1.

   2.

   3.

   4.

7. Component U4 is a:

   a) Differential voltage comparator.
   b) One shot multivibrator.
   c) Multi stage circuit.
   d) Analogue to digital converter.
   e) Differential video amplifier.

8. The Read Data signal output to the controller represents individual clock and one data bits by a pulse of nominally 250 nano-seconds.

   True/False

9. The value of certain resistors is Test Selected during manufacture. When an associated component is replaced, it may be necessary to change the value of some Test Selected components.

   True/False

(Continued on next page)

REVIEW TEST (CONTINUED)

10. Refer to the Logic Schematic for the ICMD unit and consider the following failure condition:

    A read operation is attempted, the head loads but checking Read Data Composite at TP12 shows no data. A further check between TP2 and TP3 shows data. Which major components would you suspect?

    a) Q15, Q16, U4, Q1, Q2
    b) Q1, Q2, Q3, U1, U20
    c) U4, Q1, Q2, U1, Q4
    d) Q2, Q3, U1, U2, U20
    e) U20, U29, U1, U2, Q3

Give your answers to the Course Supervisor for grading. If any answer is incorrect, review the relevant section of the Lecture before continuing.

READ THE FOLLOWING PRACTICE OBJECTIVES

PRACTICE OBJECTIVES:

1. Determine the function and mode of operation of any part of the Write Logic.

2. Given any Write Logic failure, use your knowledge of the Write Logic to determine the cause of the failure.

PRACTICE:

1. Continue listening to the cassette for Lecture 2 and view slides 35 to 51.

2. Use a BDM 1250 or equivalent to measure the Write Enable leading edge delay between U30-6 and U9-6 and the trailing edge delay between U30-6 and U9-6. Compare these values with the theoretical value of 450uS.

3. Complete the following Review Test.

REVIEW TEST LECTURE 2

11. The clock input to the Write Toggle flip flop U21 when the unit is selected is the signal:

    a) Write Clock
    b) Write Data
    c) Write Enable
    d) Data Write Clock
    e) Write Enable Delayed

12. During a write operation below track 43, Q14 and Q17 conduct simultaneously to provide the necessary current.

    True/False

13. List the three conditions which determine a Write Fault.

    1.

    2.

    3.

14. Which component is the Erase Driver?

    a) Q7
    b) CR22
    c) Q9
    d) U9
    e) Q18

(Continued in next page)

REVIEW TEST (CONTINUED)

15. Refer to the drawing of the Write Fault logic given on the next page and consider the following failure condition:

    The failing unit is one of two drives connected to the same host system controller. The other drive functions normally. The failing unit indicates a continuous Write Fault.

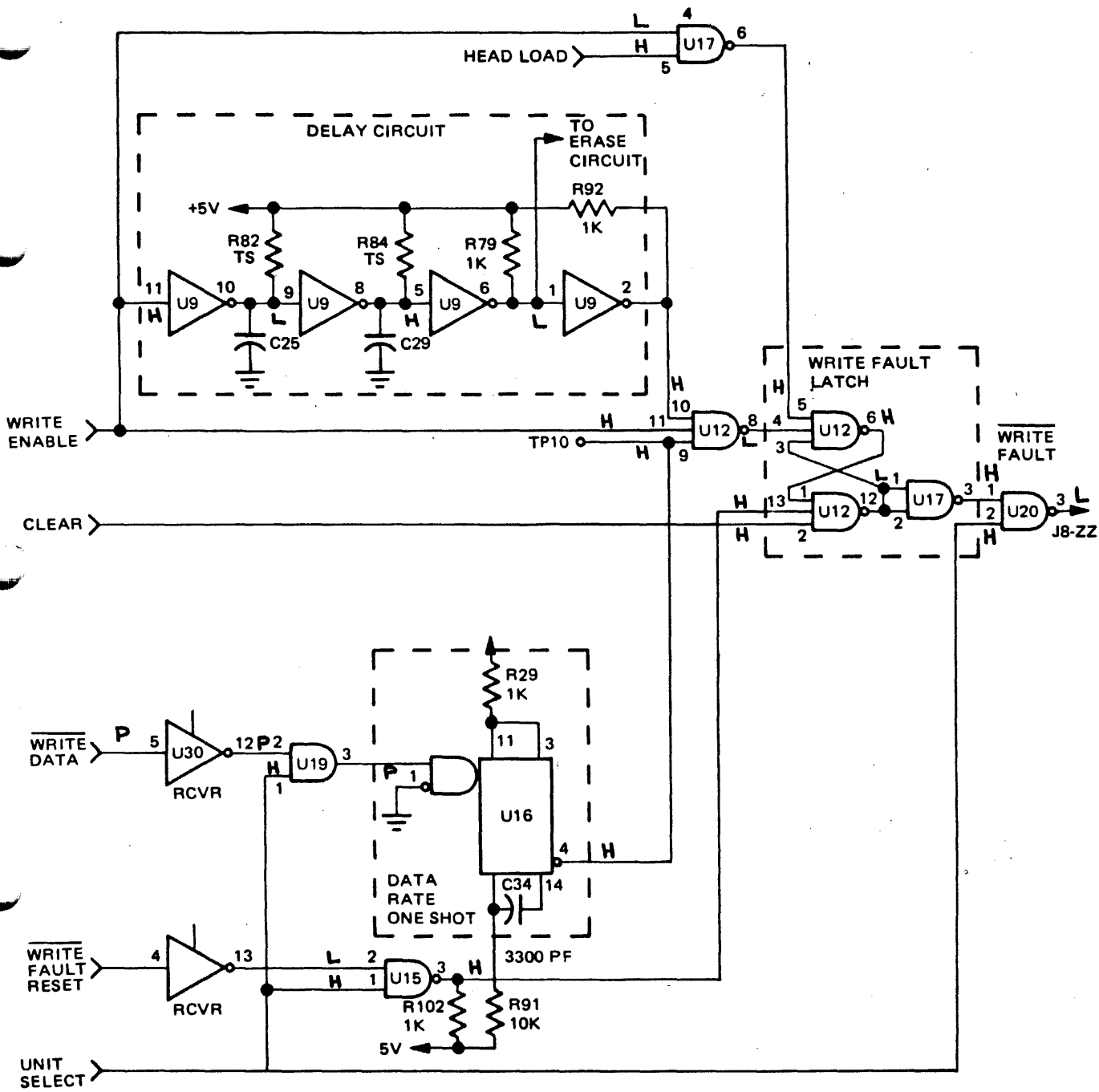
    The drawing gives the condition of the various signals associated with the Write Fault latch measured during a continuous write operation.

    Determine the source of the erroneous signal from the information on the drawing.

    IC PIN

REVIEW TEST LECTURE 2

QUESTION 15



KEY

H = High
L = Low
P = Pulsing

READ THE FOLLOWING PRACTICE OBJECTIVES

PRACTICE OBJECTIVES:

1. Determine the function and mode of operation of any part of the Control Logic.

2. Given any Control Logic failure, use your knowledge of the Control Logic to determine the cause of the failure.

PRACTICE:

1. This section of the Lecture assumes that you are familiar with the operation of a stepper motor. Review the section covering the theory of operation of a stepper motor in the FE Technical Manual, Volume 1 pages 6-5 to 6-6.

2. Continue listening to the cassette for Lecture 2 and view slides 52 to 65.

3. Using a BDM 1250, measure the time period that the signal Clear/ (U11-1) remains low after the +5 volt level is true.

4. Complete the following Review Test.

(Note: This Practice continues after the Review Test.)

REVIEW TEST LECTURE 2

16. How many phases does the stepper motor have?

a) 3
b) 6
c) 8
d) 12
e) 15

17. Each step rotates the stepper motor rotor and lead screw by:

a) 30 degrees
b) 120 degrees
c) 60 degrees
d) 12 degrees
e) 15 degrees

18. State the two conditions required by the logic to determine that the read/write head is at track 00.

1.

2.

19. State the two functions performed by the clear signal.

1.

2.

(Continued on next page)

REVIEW TEST (CONTINUED)

20. Refer to the Logic Schematic for the ICMD unit and consider the following failure condition:

    The stepper motor is excessively hot. Checking the output of U7 pin 4 with a BDM 1250 indicates a 16 millisecond negative going pulse after each single step command.

    List the four components most likely to account for the overheating motor.

    1.

    2.

    3.

    4.

Give your answers to the Course Supervisor for grading. If any answer is incorrect, review the relevant section of the Lecture before continuing.

PRACTICE (CONTINUED)

5. Continue listening to the cassette for Lecture 2 and view slides 66 to 70.

6. Determine whether the unit you are working with is equipped with the Head Load Time Out Option, by visual inspection.

7. Complete the following Review Test.

REVIEW TEST LECTURE 2

21. The Ready flip flop is set when the diskette is rotating within ±15% of the normal operating speed of 360 rpm.

    True/False

22. At the nominal speed of 360 rpm, one diskette revolution takes approximately:

    a) 10mS
    b) 25mS
    c) 80mS
    d) 128mS
    e) 170mS

23. Refer to the Logic Schematic for the ICMD unit and consider the following failure condition:

    The failing unit is one of two mounted in the same cabinet. The other unit works correctly. On the failing unit, a diskette is inserted and the Ready Indicator illuminates. However, when the host system attempts to use the failing unit, it reports that the unit is not Ready. Excluding the Interface cable and components, list the three most likely suspect components.

    1.

    2.

    3.

Give your answers to the Course Supervisor for grading. If any answer is incorrect, review the relevant section of the Lecture before continuing.

READ THE FOLLOWING PRACTICE OBJECTIVES

PRACTICE OBJECTIVES:

1. Configure the unit power supply for operation at the correct line voltage and frequency.

2. Determine the purpose and function of each circuit within the power supply.

3. Determine the conditions which cause the power supply protection circuitry to operate.

4. Check power supply voltage levels and make any necessary adjustment to correct for variations in component tolerances.

PRACTICE:

1. Continue listening to the cassette for Lecture 2 and view slides 71 to 77.

2. Check the transformer tapping for the unit you are working with against the appropriate table for the line voltage used.

3. Identify a suitable location to measure each voltage produced by the power supply. Measure each voltage. Locate the two adjustment potentiometers. Note that these adjustments are made during manufacture and should not require attention unless associated components are replaced.

This concludes Lecture 2.

LECTURE 3

LECTURE INTRODUCTION:

The third lecture divides into three sections:

i) The first section describes unit installation for all styles of B 9489 ICMD units.

ii) The second section details all ICMD unit adjustments describing their purpose and where necessary, the correct sequence. Also included are practice instructions for removal and replacement of each major component.

iii) The third section covers unit maintenance which includes both fault finding using the MTR procedures and preventative maintenance requirements.

READ THE FOLLOWING LECTURE OBJECTIVES

LECTURE OBJECTIVES:

1. Install any style of B 9489 ICMD unit.

2. Determine the need for and be able to correctly apply all unit adjustments in the correct sequence.

3. Remove and replace any component or sub-assembly of the ICMD unit applying all necessary adjustments.

4. Use the MTR and knowledge of the unit to detect any given failure and to correct the failure by adjustment or component replacement.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Correctly configure any style ICMD unit for operation with the local power supply voltage and frequency.

2. Install resistor chip terminators as necessary.

3. Set the unit designate number for each unit.

4. Correctly configure the Unit Select and Unit Ready designations.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 1 to 11.

2. Check the drive belt alignment adjustment on the unit you are working with.

3. If you are working with a free standing unit, use the transformer tapping table in the Technical Manual, Volume 1, Section 2 to determine the voltage and frequency for which the unit is configured.

4. Review all currently released RIN, LIN and ATI information, determine whether all updates have been applied and apply any which are found to be outstanding.

5. Locate and determine the settings of the Unit Select and Unit Ready switches.

6. If you are working with a free standing unit, locate and determine the setting of the Subsystem Designate Switch.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Determine for each of the following adjustments that the adjustment is correct and the effect of incorrect adjustment. Correctly perform each adjustment;

   a. Registration cone and spindle alignment.
   b. Push rod travel and door interlock switch.
   c. Head load bail.

2. Remove and replace any assembly or component associated with the registration cone and spindle, push rod, door interlock and head load bail assemblies.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 12 to 17.

2. Remove and replace the chassis support assembly referring to the Technical Manual, Volume 1, Page 4-8 for the correct procedure and adjustment sequence.

3. Check and if necessary, perform the head load bail adjustment.

READ THE FOLLOWING PRACTICE OBJECTIVE AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVE:

1. Ensure compatability of units by obtaining the correct carriage assembly (track) alignment.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 18 to 23.

2. Referring to the Technical Manual, Volume 1, Page 5-5, check the cateyes alignment pattern using an alignment diskette or oscilloscope. DO NOT adjust the alignment at this time. This adjustment is performed in a later practice.

READ THE FOLLOWING PRACTICE OBJECTIVE AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVE:

1. Determine the need for and correctly adjust the optical track 00 sensor using the appropriate adjustment procedure, either referenced to track 38 or to the outer carriage stop.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 23 to 28.

2. Referring to the Technical Manual, Volume 1, Page 5-7 through Page 5-9, verify that the adjustment of the track 00 optical sensor is correct using the two procedures described.

   NOTE: These adjustments have been revised to ensure that the sensor output switches between tracks 01 and 02, i.e. J3 pin 2 should be high at tracks 00 and 01 but low at track 02. Refer to ATI 54403. DO NOT adjust the optical track 00 sensor at this time. This adjustment is performed in a later practice.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Determine the need for and correctly adjust the carriage stops.

2. Remove and replace any assembly or component associated with the head carriage assembly and stepper motor assembly, ensuring that following replacement, the unit is correctly adjusted for proper unit function and media compatability with other drive units.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 29 and 30.

2. Referring to the Technical Manual, Volume 1, Page 4-7 remove and replace the head carriage assembly, performing the carriage assembly (track) alignment, optical track 00 sensor and carriage stop adjustment.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Ensure correct adjustment of the Index Hole sensor.

2. Given the need to replace specific electronic components, associate any related TS (test selected) resistors and determine the need to change the value of any test selected component.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 31 to 36.

2. Referring to the Technical Manual, Volume 1, Page 5-11, check the optical Index sensor adjustment. Adjust if necessary.

3. Using the Test Selected Resistor table in the Technical Manual, Volume 1, Page 4-12, verify by measurement that the values of each test selected resistor in the unit is within tolerance.

B 9489 ICMD FIELD ENGINEERING TRAINING PROGRAM

READ THE FOLLOWING PRACTICE OBJECTIVES
AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVES:

1. Identify the Maintenance Philosophy for the ICMD unit.

2. Use the MTR, any available host system test procedures and your knowledge of the unit logic to determine that a unit is failure free or to detect and define any failure to the failed component.

PRACTICE:

1. Listen to the cassette for Lecture 3 and view slides 37 to 45.

2. Run any available host system test program and the unit MTR failure investigation path to determine that a unit is failure free. Correct any failures or performance defects.

READ THE FOLLOWING PRACTICE OBJECTIVES AND COMPLETE THE PRACTICE

PRACTICE OBJECTIVE:

1. Complete the preventative maintenance schedule at the prescribed interval.

2. Ensure that the unit is correctly adjusted and operates to specification.

PRACTICE:

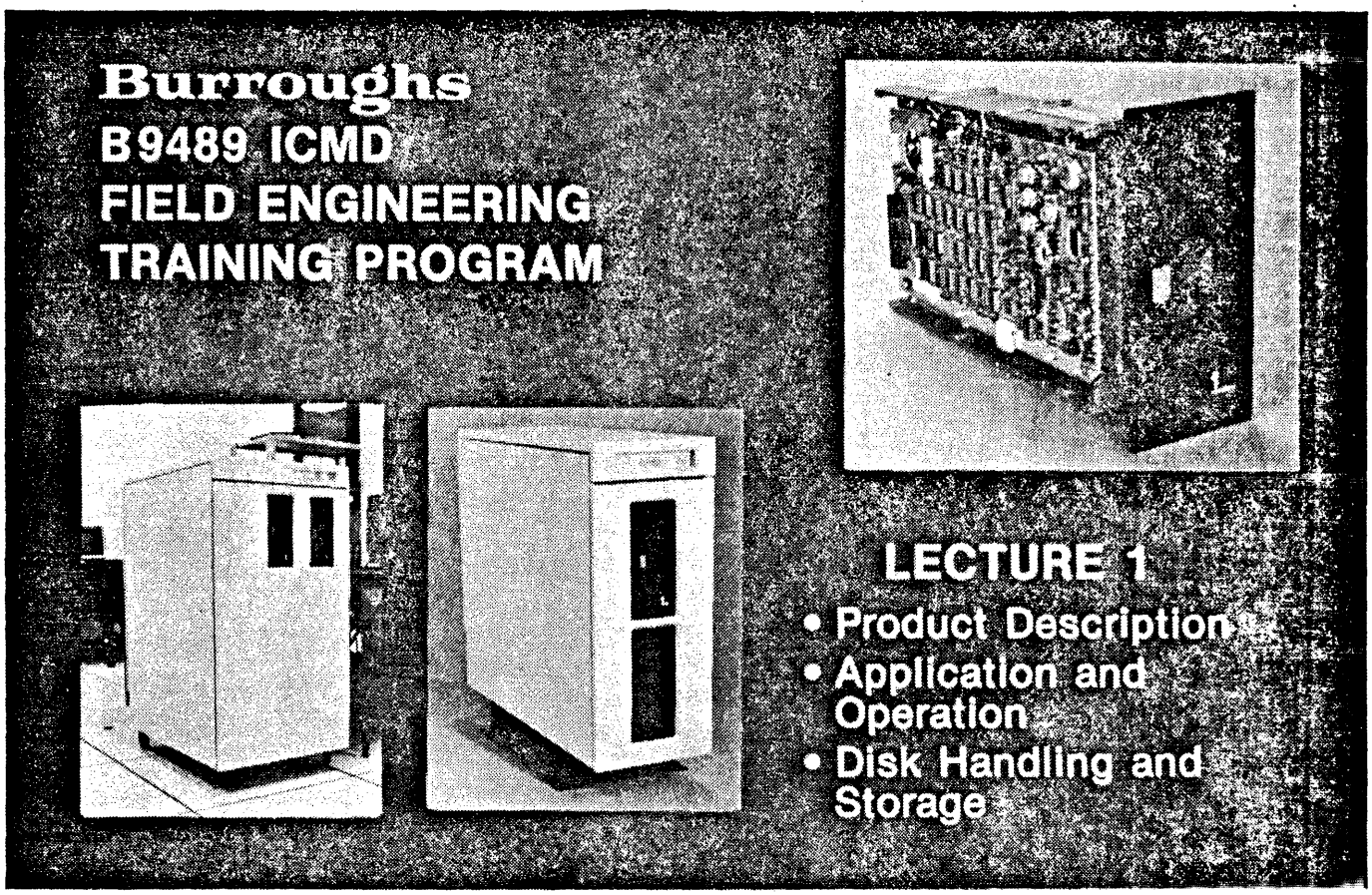
1. Refer to the Technical Manual, Volume 1, Page 4-1 through 4-3. Read the section headed "Preventative Maintenance Procedures."

2. Check all adjustments and test the unit. Correct as necessary. Ask course supervisor to check the unit.

This concludes the B 9489 ICMD Field Engineering Training Program.

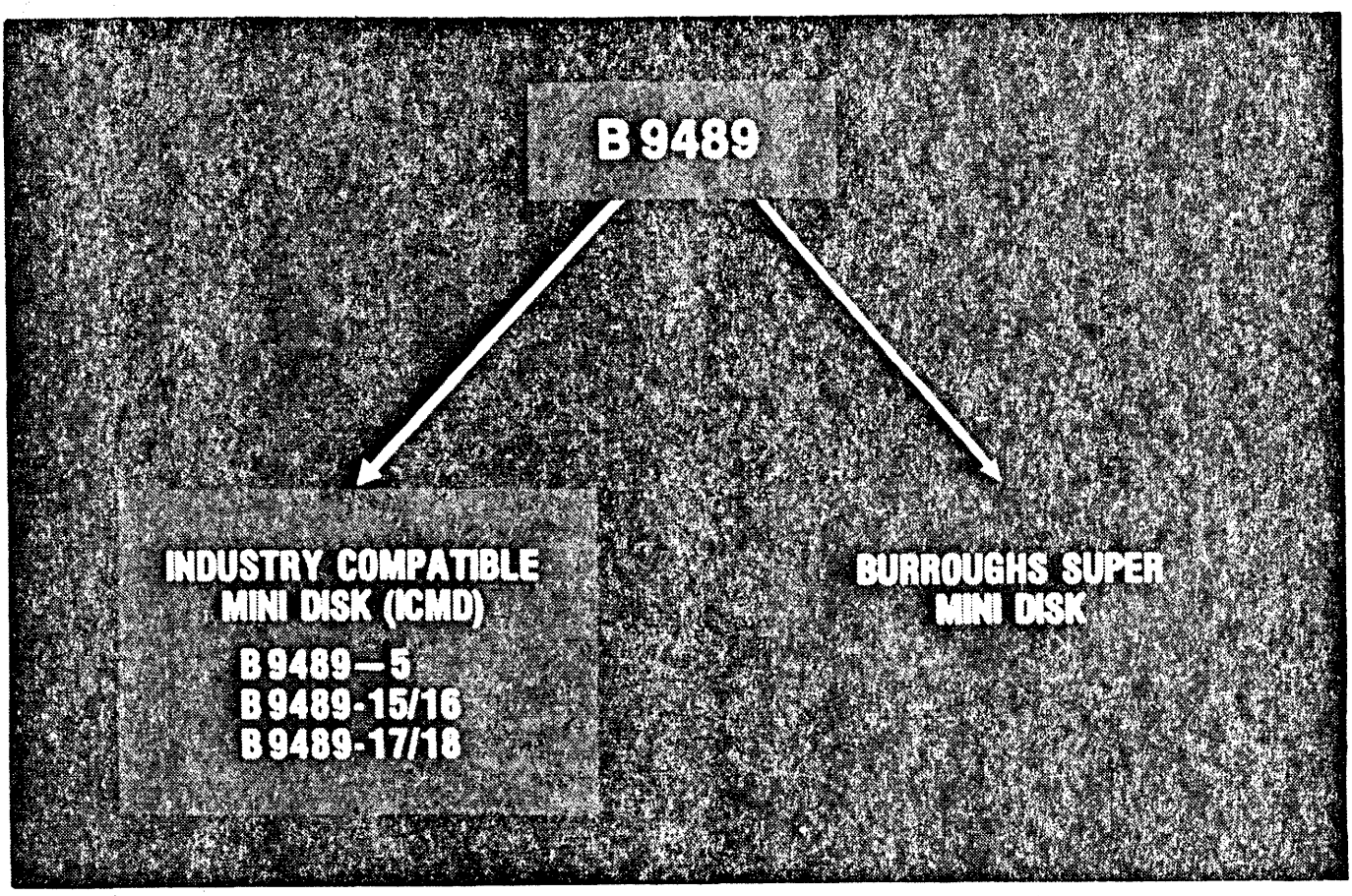
Review any objective which you feel that you have not fully achieved and refer any outstanding questions or problems to your Course Supervisor.

Ensure that the unit is correctly adjusted and performing to specification before asking your Course Supervisor to finally check the unit.



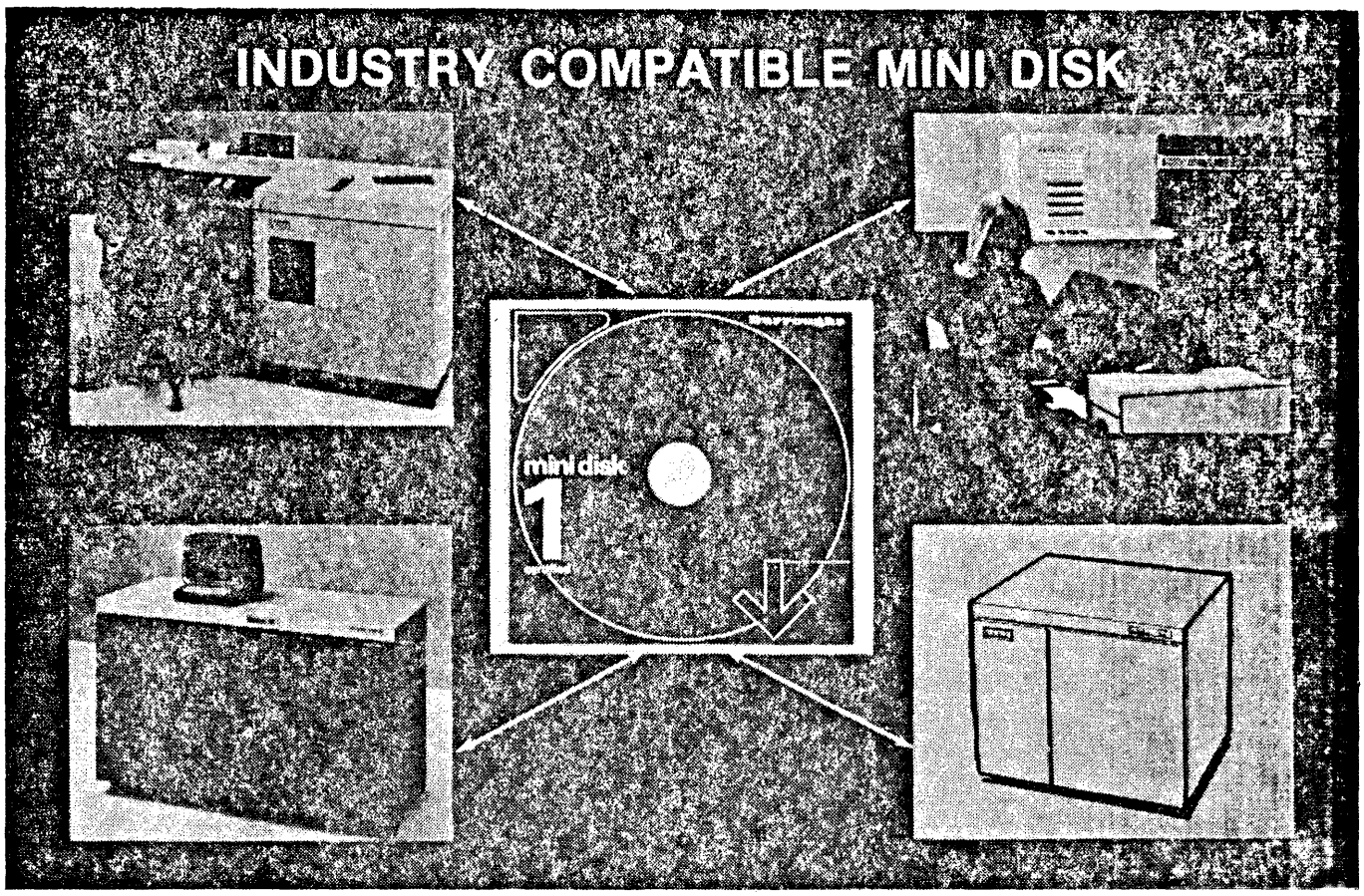
THIS IS THE FIRST LECTURE IN THE BURROUGHS B 9489 INDUSTRY COMPATIBLE MINI DISK (ICMD) TRAINING PROGRAM. THIS FIRST LECTURE GIVES A PRODUCT DESCRIPTION, DESCRIBING BOTH THE TYPE OF APPLICATION AND OPERATIONAL CHARACTERISTICS OF THE ICMD DRIVE AND INCLUDES THE BASIC RULES FOR DISK HANDLING AND STORAGE.

2



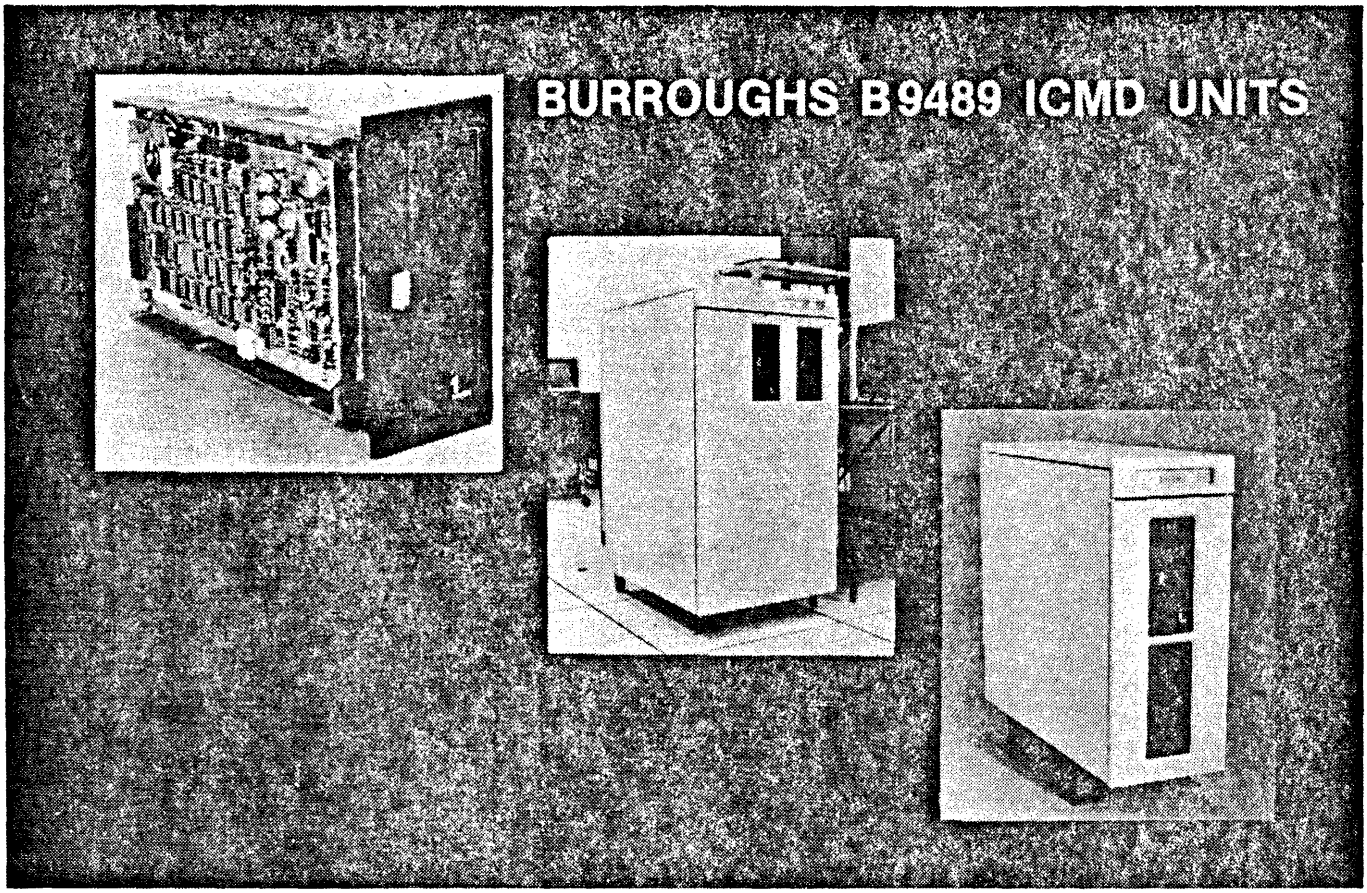
THERE ARE TWO DISTINCT GROUPS OF DISK DRIVES WITHIN THE B 9489 FAMILY WHICH SHOULD NOT BE CONFUSED. FIRST, THERE IS THE INDUSTRY COMPATIBLE MINI DISK GROUP WHICH IS THE SUBJECT OF THIS TRAINING PROGRAM. SECOND, THERE IS THE BURROUGHS SUPER MINI DISK GROUP WHICH IS DIFFERENT, BOTH IN THE HARDWARE OPERATION OF THE DRIVE AND THE FORMAT IN WHICH DATA IS RECORDED. FUTURE DEVELOPMENTS COULD ADD ADDITIONAL GROUPS TO THE FAMILY.

3



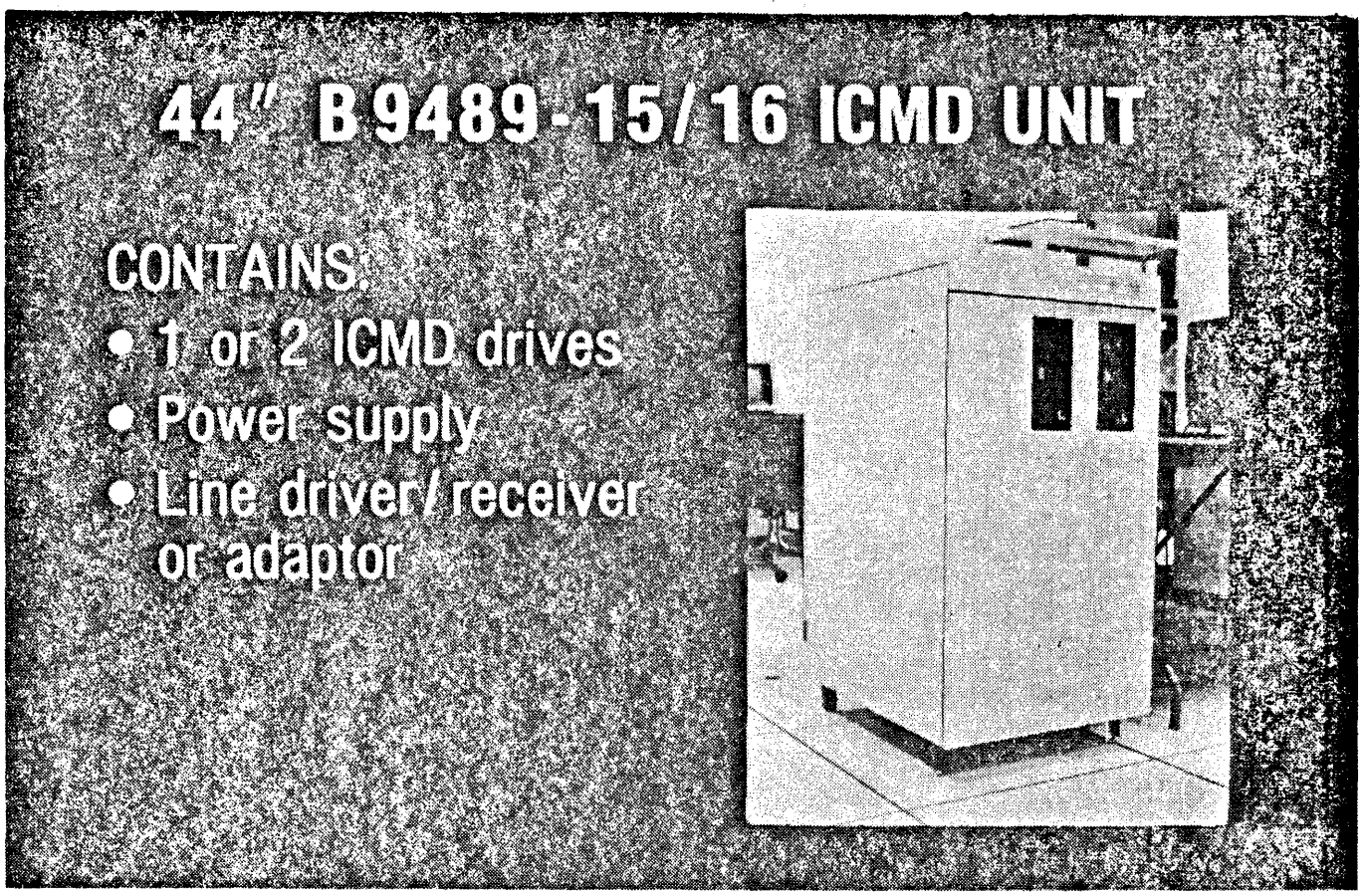
THE ICMD FLEXIBLE DISK DRIVE SUBSYSTEMS ARE PERIPHERAL DEVICES USED IN DATA ENTRY AND STORAGE APPLICATIONS. AN INDUSTRY COMPATIBLE REMOVABLE MEDIA CALLED A DISKETTE OR FLEXIBLE DISK IS USED. DATA IS STORED ON THE DISKETTES USING MAGNETIC TECHNIQUES IN AN INDUSTRY COMPATIBLE FORMAT, ALLOWING MEDIA INTERCHANGE BETWEEN ANY COMPUTER SYSTEM WITH EQUIVALENT FLEXIBLE DISK DRIVE SUBSYSTEMS, REGARDLESS OF THE MANUFACTURER AND VENDOR.

4



THREE BASIC CONFIGURATIONS OF THE BURROUGHS FDD SUBSYSTEM ARE AVAILABLE FOR USE WITH THE VARIOUS BURROUGHS HOST SYSTEMS. EACH CONFIGURATION USES THE SAME BASIC DISK DRIVE. THIS DISK DRIVE MAY BE BUILT INTO THE HOST SYSTEM OR BE FREESTANDING IN EITHER A 30 OR 44 INCH HIGH CABINET. WE WILL LOOK AT EACH CONFIGURATION IN TURN.

5



THE B 9489-15 AND -16 SUBSYSTEMS HOUSE ONE AND TWO DISK DRIVES RESPECTIVELY IN THE 44 INCH HIGH CABINET. THE UNIT ILLUSTRATED IS THE -16 HOUSING TWO DISK DRIVES. THESE SUBSYSTEMS FUNCTION AS STAND ALONE PERIPHERAL UNITS THAT CONTAIN ALL NECESSARY POWER SUPPLIES, INTERNAL CABLING AND EITHER A LINE DRIVER/RECEIVER CARD OR AN ADAPTOR CARD TO INTERFACE TO THE BURROUGHS HOST SYSTEM.

6

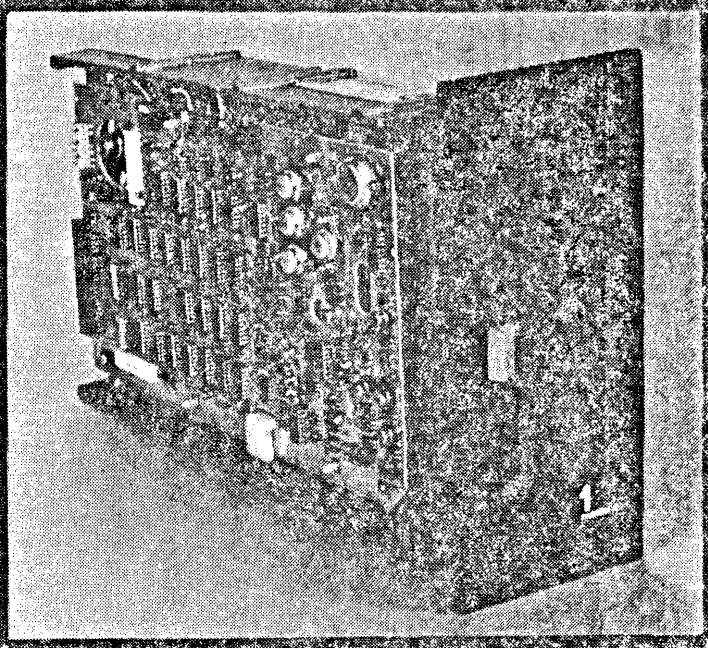
THE B 9489-17 AND -18 SUBSYSTEMS AGAIN HOUSE ONE AND TWO DISK DRIVES RESPECTIVELY, BUT IN THE 30 INCH HEIGHT CABINET. THE UNIT ILLUSTRATED IS THE -17 HOUSING ONE DISK DRIVE. LIKE THE -15 AND -16 VERSIONS, THESE SUB-SYSTEMS CONTAIN THE POWER SUPPLY AND INTERNAL CABLING. HOWEVER, THE UNIT DOES NOT HAVE THE OPTION OF AN ADAPTOR CARD AND DEPENDING ON THE REQUIREMENTS OF THE HOST SYSTEM THE DRIVER/RECEIVER CARD IS OPTIONAL.

7

B9489-5 ICMD UNIT

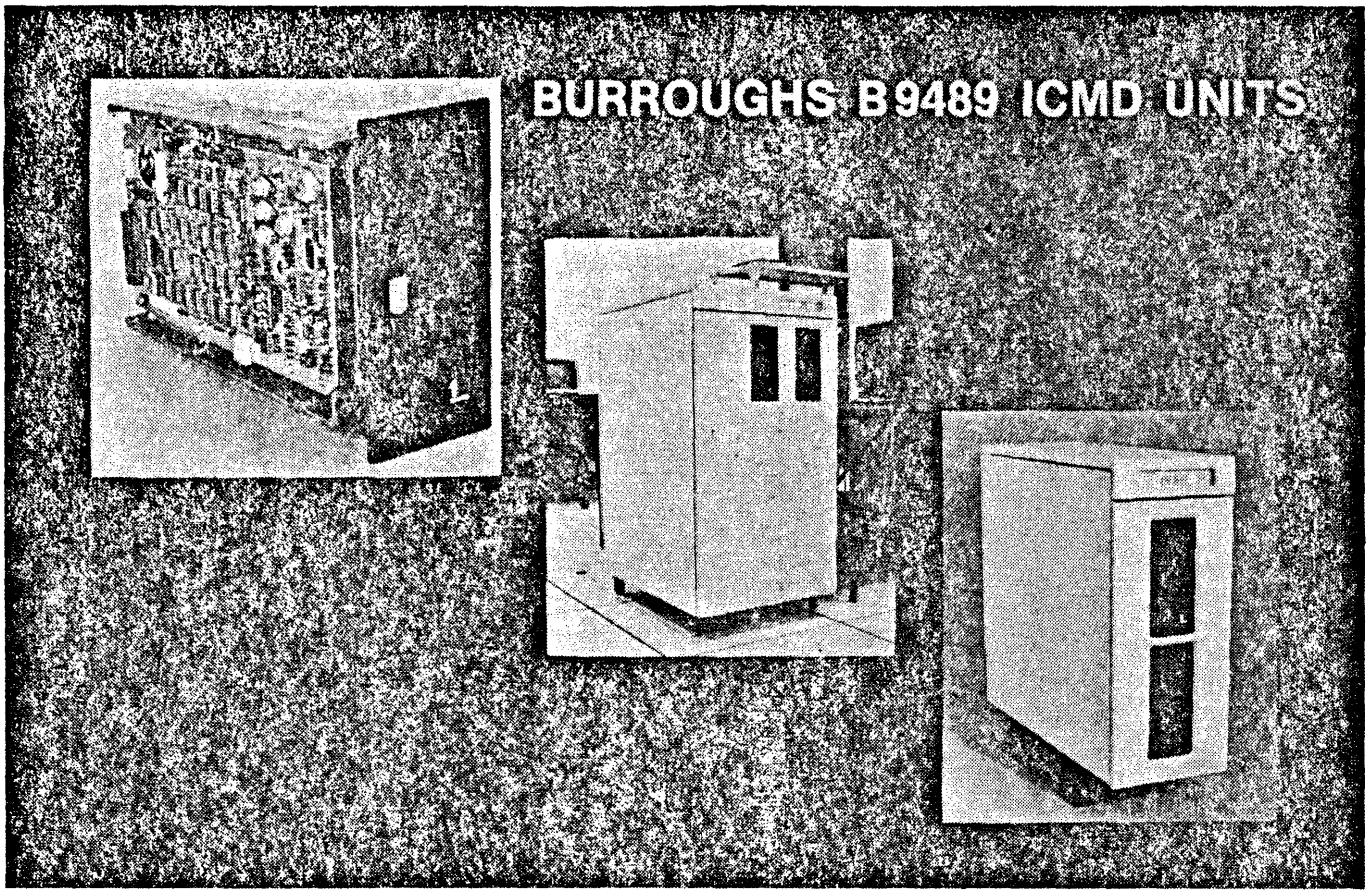
HOST SYSTEM MOUNTING

- External power



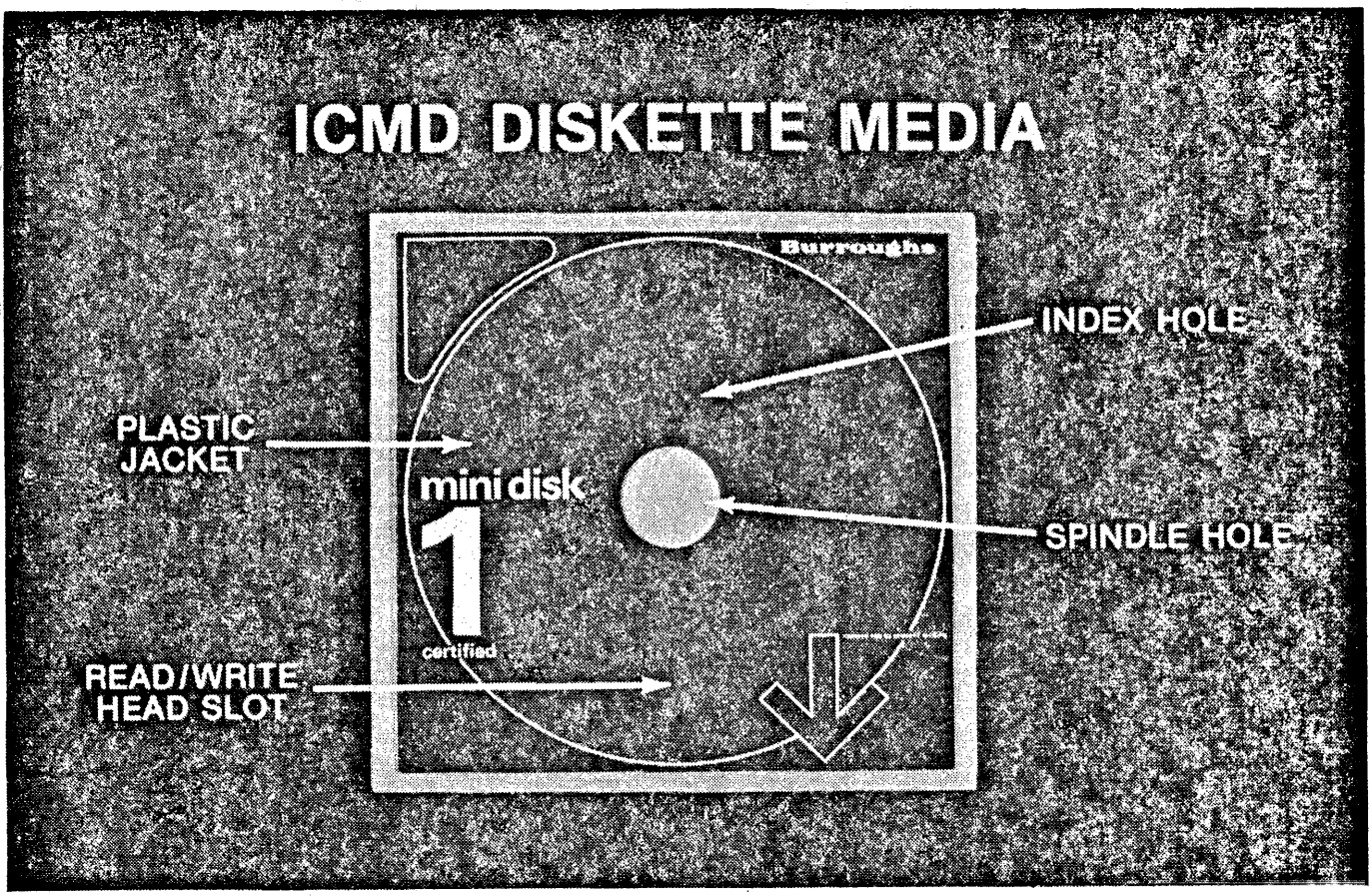
THE B 9489-5 UNIT IS THE SAME BASIC FLEXIBLE DISK DRIVE AS USED IN BOTH THE FREESTANDING CABINET SUBSYSTEMS, BUT WITHOUT THE POWER SUPPLY AND CABLING. THIS UNIT IS DESIGNED FOR MOUNTING IN THE HOST SYSTEM CABINETRY AND POWER MUST BE PROVIDED BY THE HOST SYSTEM.

8



THESE THREE BASIC CONFIGURATIONS OF THE BURROUGHS FDD SUBSYSTEM ALLOW THE INDUSTRY COMPATIBLE MINI DISK TO BE USED WITH A WIDE RANGE OF BURROUGHS PRODUCTS FROM SMALL SYSTEMS SUCH AS THE B 80 THROUGH TO VERY LARGE SYSTEMS SUCH AS THE B 7700.

9



LET US LOOK AT THE MINI DISK OR DISKETTE MEDIA ITSELF IN MORE DETAIL AND CONSIDER SOME OF THE HANDLING AND STORAGE PROCEDURES WHICH SHOULD BE FOLLOWED TO MINIMIZE THE RISK OF MEDIA DAMAGE.

THE DISKETTE IS CONTAINED IN A FLEXIBLE PLASTIC JACKET FROM WHICH IT IS NEVER REMOVED. THE DISK IS COATED ON ONE SIDE WITH A MAGNETIC OXIDE SIMILAR TO THAT USED ON AUDIO RECORDING TAPE.

THE CENTRAL SPINDLE HOLE IS USED TO BOTH REGISTER -- THAT IS CORRECTLY ALIGN -- AND ROTATE THE DISK.

A SMALL HOLE, CALLED THE INDEX HOLE, IS LOCATED CLOSE TO THE SPINDLE

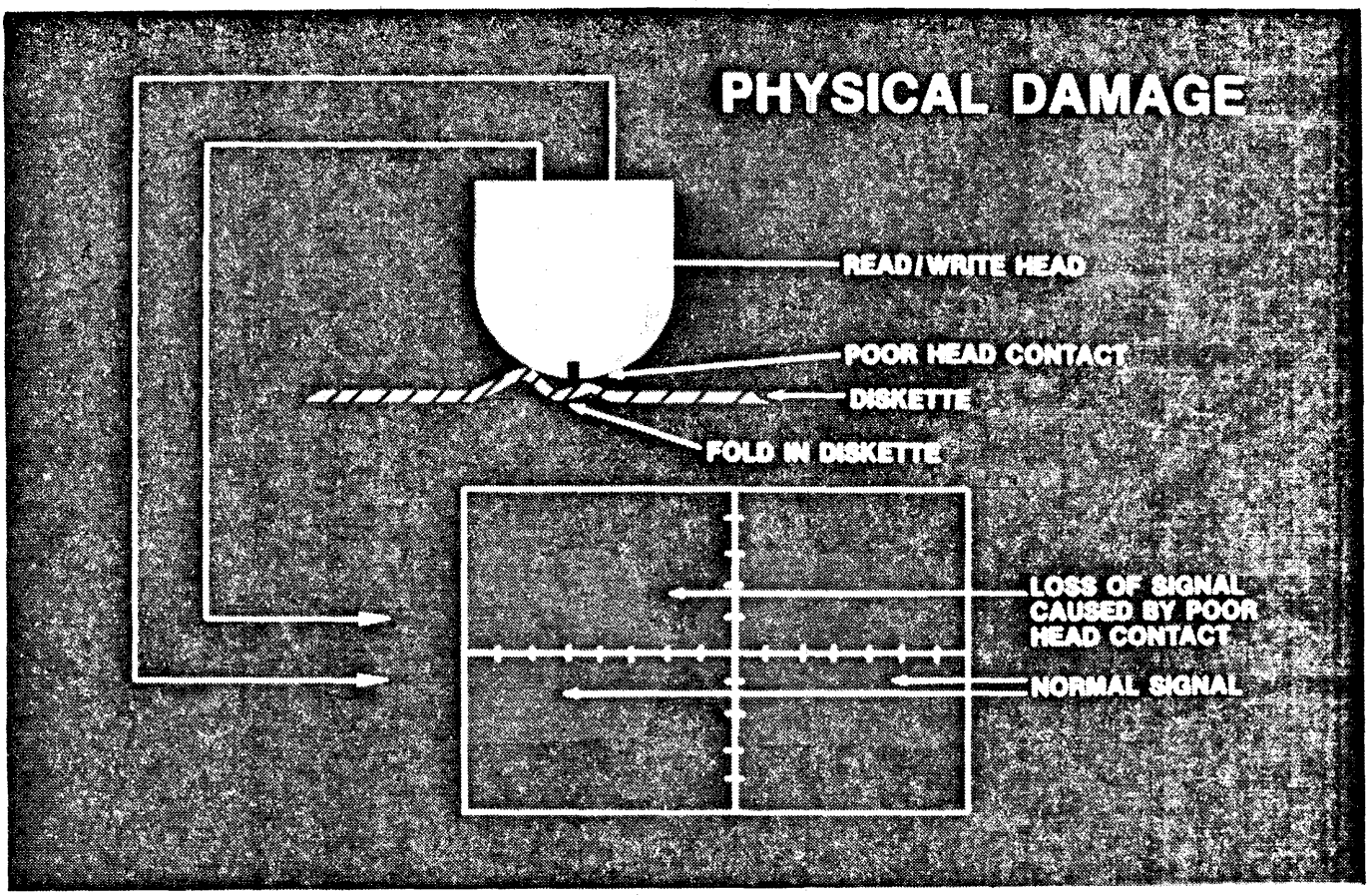
HOLE. THE INDEX HOLE IS SENSED AS IT PASSES AN OPTICAL SENSOR IN THE FDD TO GENERATE A TIMING PULSE CALLED "INDEX" WHICH OCCURS ONCE PER DISKETTE REVOLUTION.

DURING A READ OR WRITE OPERATION, THE FDD READ/WRITE HEAD CONTACTS THE DISKETTE SURFACE THROUGH AN OPEN SLOT IN THE PLASTIC JACKET.

10

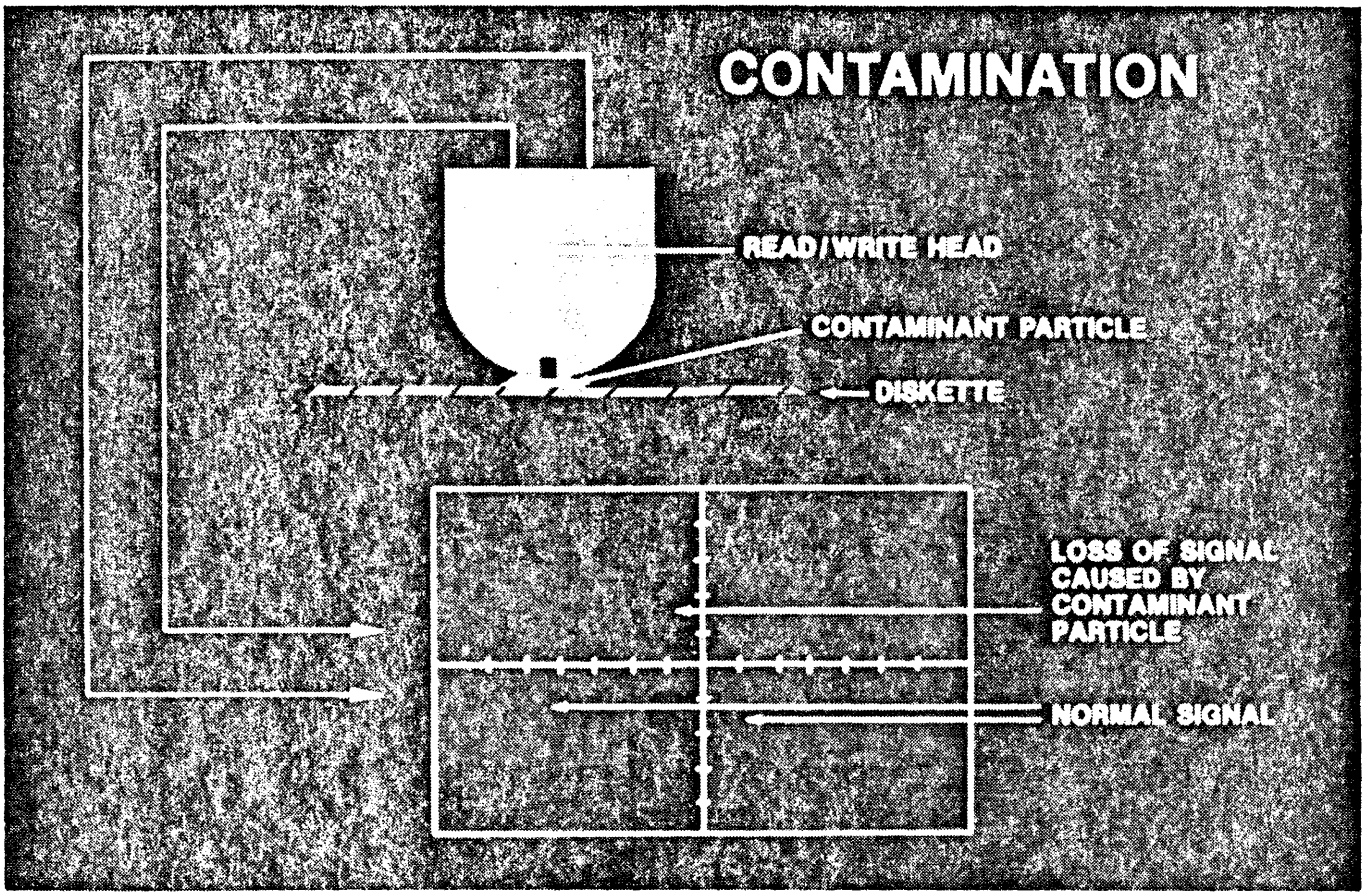
PROPER CARE AND HANDLING OF THE DISKETTE IS ESSENTIAL TO ENSURE LONG DISKETTE LIFE AND TO MINIMIZE THE POSSIBILITY OF MEDIA ERRORS. IMPROPER CARE AND HANDLING CAN RESULT IN THREE MAIN TYPES OF DAMAGE. THESE ARE PHYSICAL DAMAGE, CONTAMINATION AND LOSS OF RECORDED DATA.

11



THE FIRST TYPE OF DAMAGE, PHYSICAL DAMAGE SUCH AS FOLDS, SCRATCHES OR DISTORTION OF THE DISK, CAUSES ERRORS BECAUSE THE READ/WRITE HEAD IS UNABLE TO MAINTAIN CLOSE CONTACT WITH THE MAGNETIC OXIDE RECORDING SURFACE OF THE DISK RESULTING IN A LOSS OF SIGNAL DURING A READ OPERATION OR BADLY RECORDED DATA DURING A WRITE OPERATION. IN SERIOUS CASES, DAMAGE TO THE READ/WRITE HEAD ITSELF MAY OCCUR.

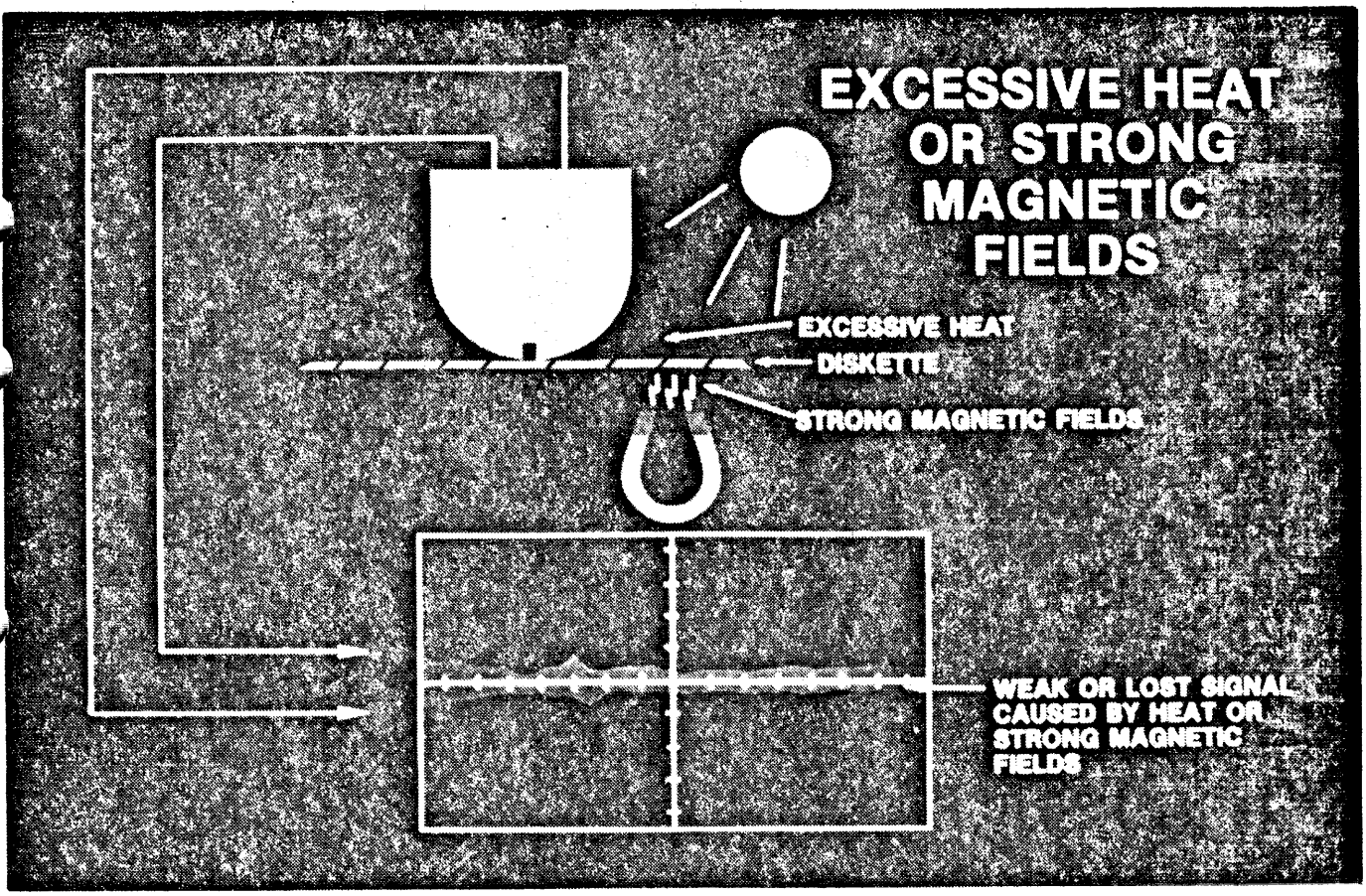
12



THE SECOND TYPE OF DAMAGE, CONTAMINATION, IS CAUSED BY PARTICLES OF DIRT ON THE MAGNETIC OXIDE SURFACE OF THE DISKETTE. AS WITH PHYSICAL DAMAGE, CONTAMINATION CAN CAUSE THE READ/WRITE HEAD TO LOOSE CLOSE CONTACT WITH THE MAGNETIC OXIDE RECORDING SURFACE OF THE DISK RESULTING IN A LOSS OF SIGNAL DURING A READ OPERATION OR, BADLY RECORDED DATA DURING A WRITE OPERATION.

TYPICAL CONTAMINANTS ARE DUST, FOOD PARTICLES AND CIGARETTE ASH. CONTAMINANTS CAN CAUSE SCRATCHES IN BOTH THE DISKETTE SURFACE AND READ/WRITE HEAD AND CAN BUILD UP ON THE READ/WRITE HEAD TO BE TRANSFERRED FROM DISKETTE TO DISKETTE.

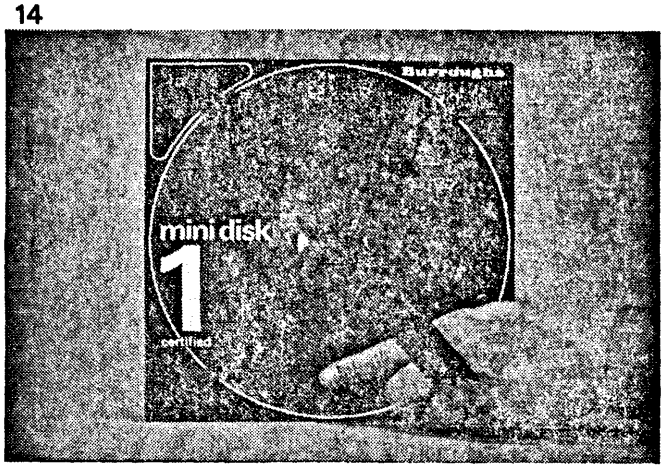
13



THE THIRD TYPE OF DAMAGE IS LOSS OF DATA RECORDED ON THE MAGNETIC OXIDE CAUSED BY EXPOSURE TO STRONG MAGNETIC FIELDS OR EXCESSIVE HEAT. STRONG MAGNETIC FIELDS CAN ERASE THE MAGNETICALLY RECORDED DATA ON THE DISKETTE CAUSING LOSS OF SIGNAL DURING A READ OPERATION. EXCESSIVE HEAT CAN BOTH ERASE MAGNETICALLY RECORDED DATA AND CAUSE PHYSICAL DISTORTION OF THE DISK.

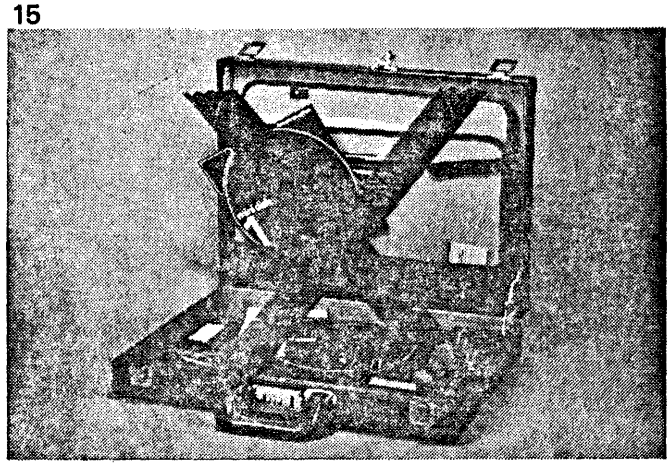
TO AVOID SUCH HAZARDS, REMEMBER THE FOLLOWING RULES WHEN HANDLING DISKETTES.

14



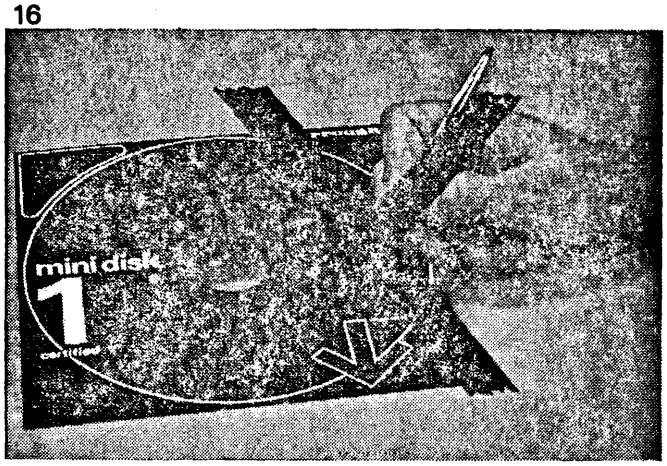
DO NOT TOUCH THE DISKETTE SURFACE EXPOSED BY THE JACKET SLOT.

15



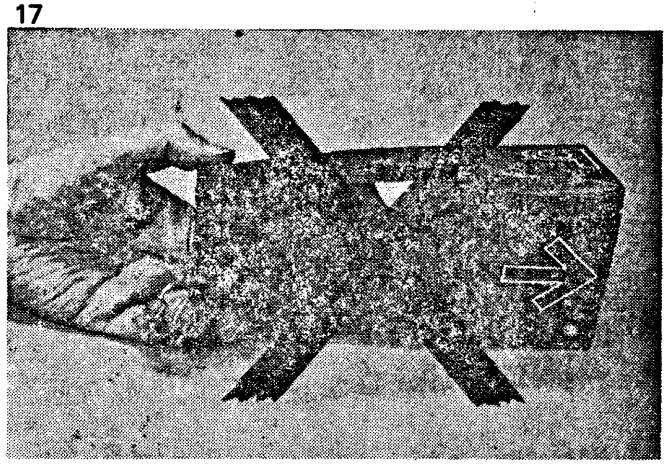
DO NOT LEAVE DISKETTE WITHOUT PROTECTIVE ENVELOPE WHEN NOT IN USE.

16



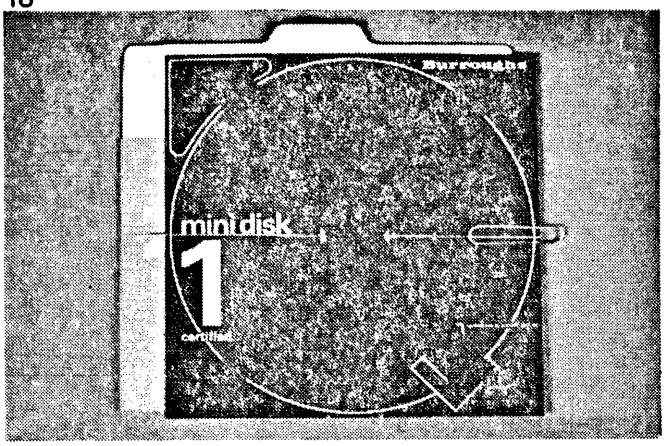
DO NOT WRITE ON THE JACKET LABEL WITH A LEAD PENCIL OR BALL POINT PEN SURFACE DAMAGE OR CONTAMINATION CAN RESULT. A FELT TIP PEN IS RECOMMENDED.

17



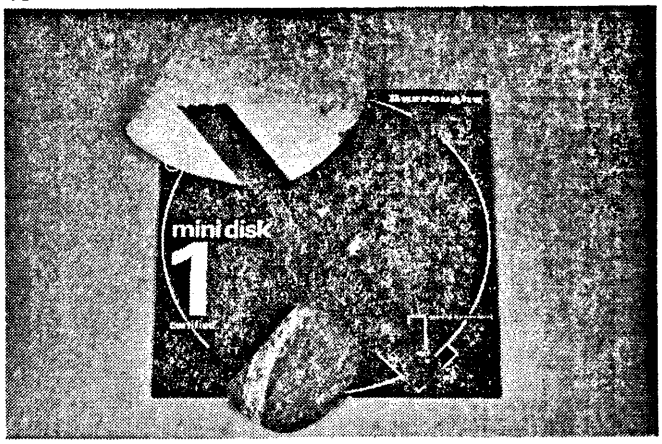
DO NOT FOLD OR BEND THE DISKETTE.

18



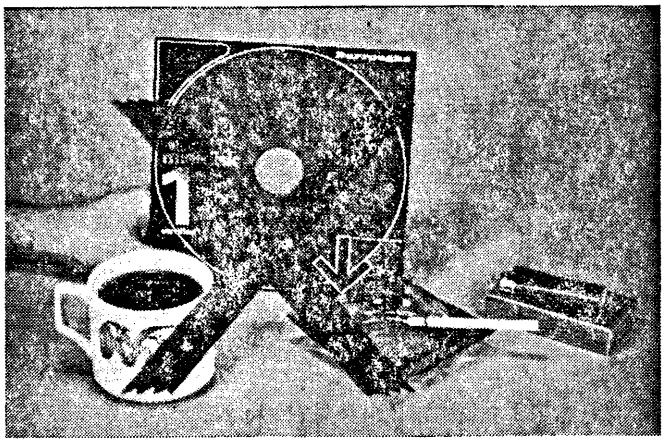
DO NOT USE RUBBER BANDS OR PAPER CLIPS ON DISKETTES.

19



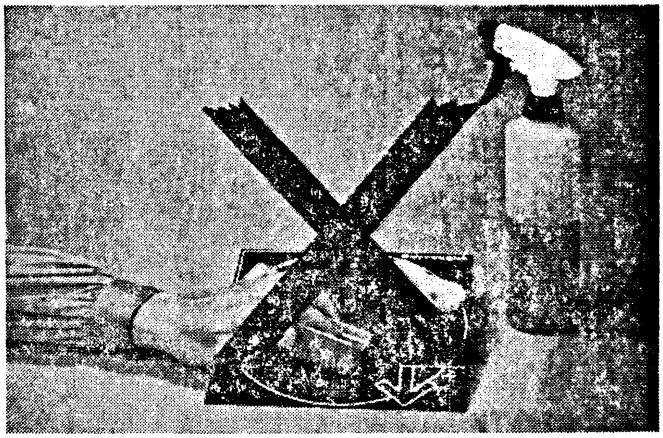
DO NOT PLACE HEAVY OBJECTS ON DISKETTES.

20

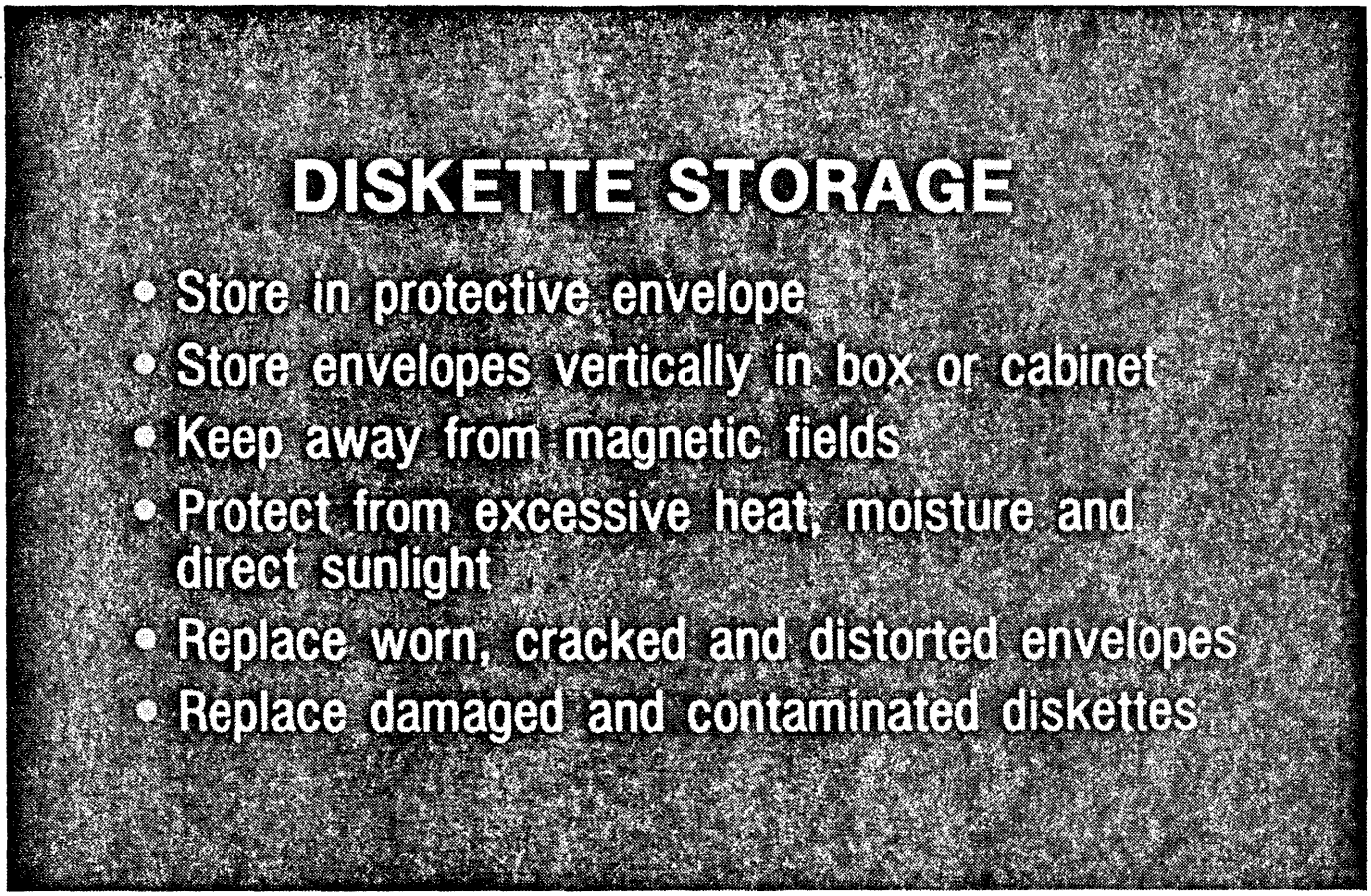


DO NOT SMOKE, EAT OR DRINK WHILE HANDLING DISKETTES.

21



DO NOT ATTEMPT TO CLEAN THE MAGNETIC OXIDE SURFACE. SUBSTANCES SPILLED ON THE DISKETTE JACKET CAN BE REMOVED AND DATA RECOVERED ONLY IF THE CONTAMINANT DOES NOT REACH THE RECORDING SURFACE.



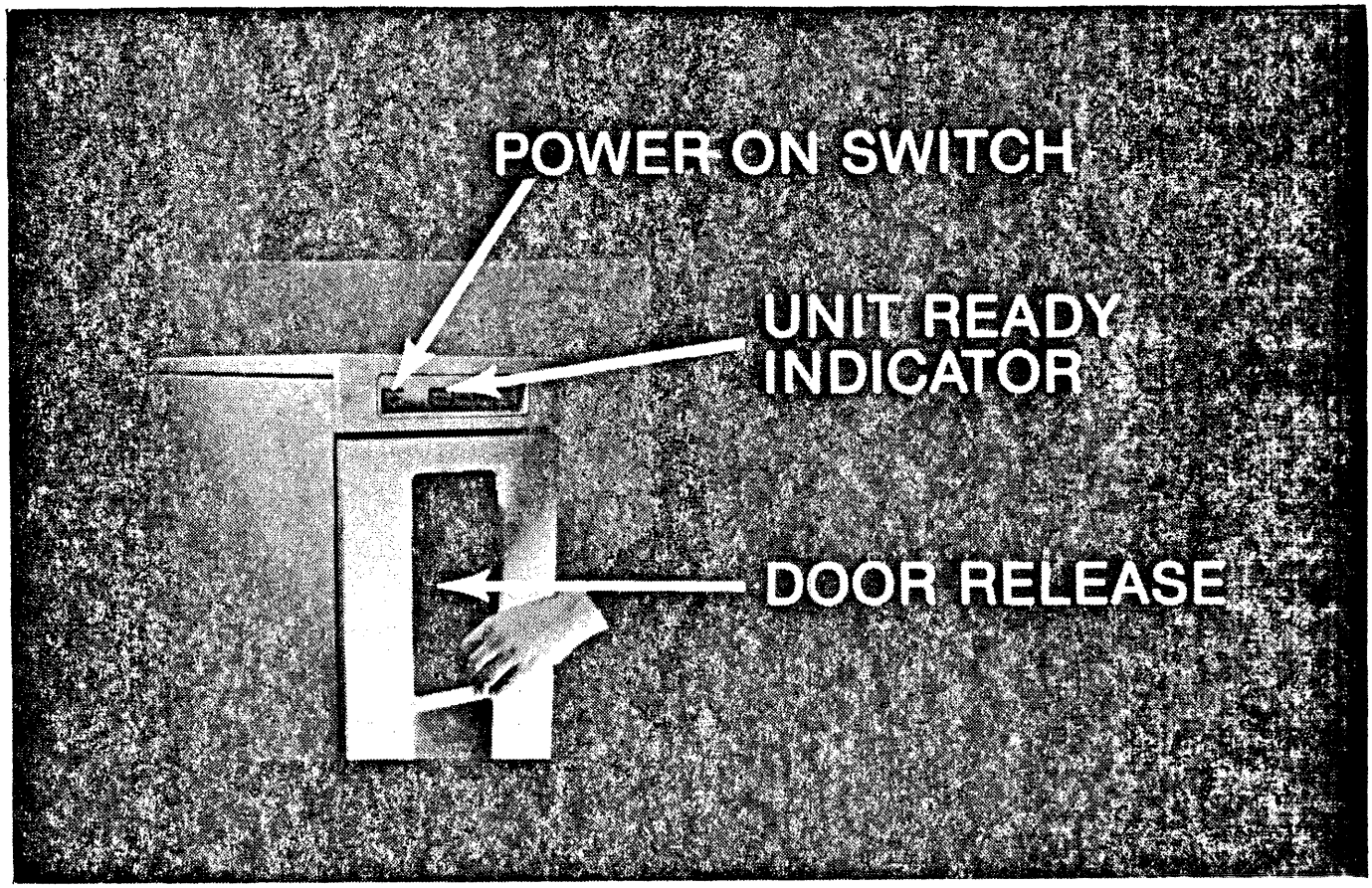
AS WITH DISKETTE HANDLING, CERTAIN RULES SHOULD BE APPLIED TO DISKETTE STORAGE:

- ALWAYS STORE THE DISKETTE IN THE PROTECTIVE ENVELOPE WHEN NOT IN USE.
- STORE THE PROTECTED DISKETTE IN THE BOX OR A CABINET IN A VERTICAL POSITION.
- KEEP THE DISKETTE AWAY FROM MAGNETIC FIELDS OR MATERIALS WHICH MAY BE MAGNETIZED.
- PROTECT THE DISKETTE FROM EXCESSIVE HEAT, MOISTURE AND DIRECT SUNLIGHT. ENVIRONMENTAL LIMITS ARE SPECIFIED IN THE TECHNICAL MANUAL.
- REPLACE STORAGE ENVELOPES THAT HAVE BECOME WORN, CRACKED OR

DISTORTED.

- REPLACE DAMAGED OR CONTAMINATED DISKETTES AND REMEMBER, A DAMAGED OR CONTAMINATED DISKETTE CAN CAUSE DAMAGE TO THE DISK DRIVE ITSELF AND SUBSEQUENTLY TO OTHER DISKETTES.

23

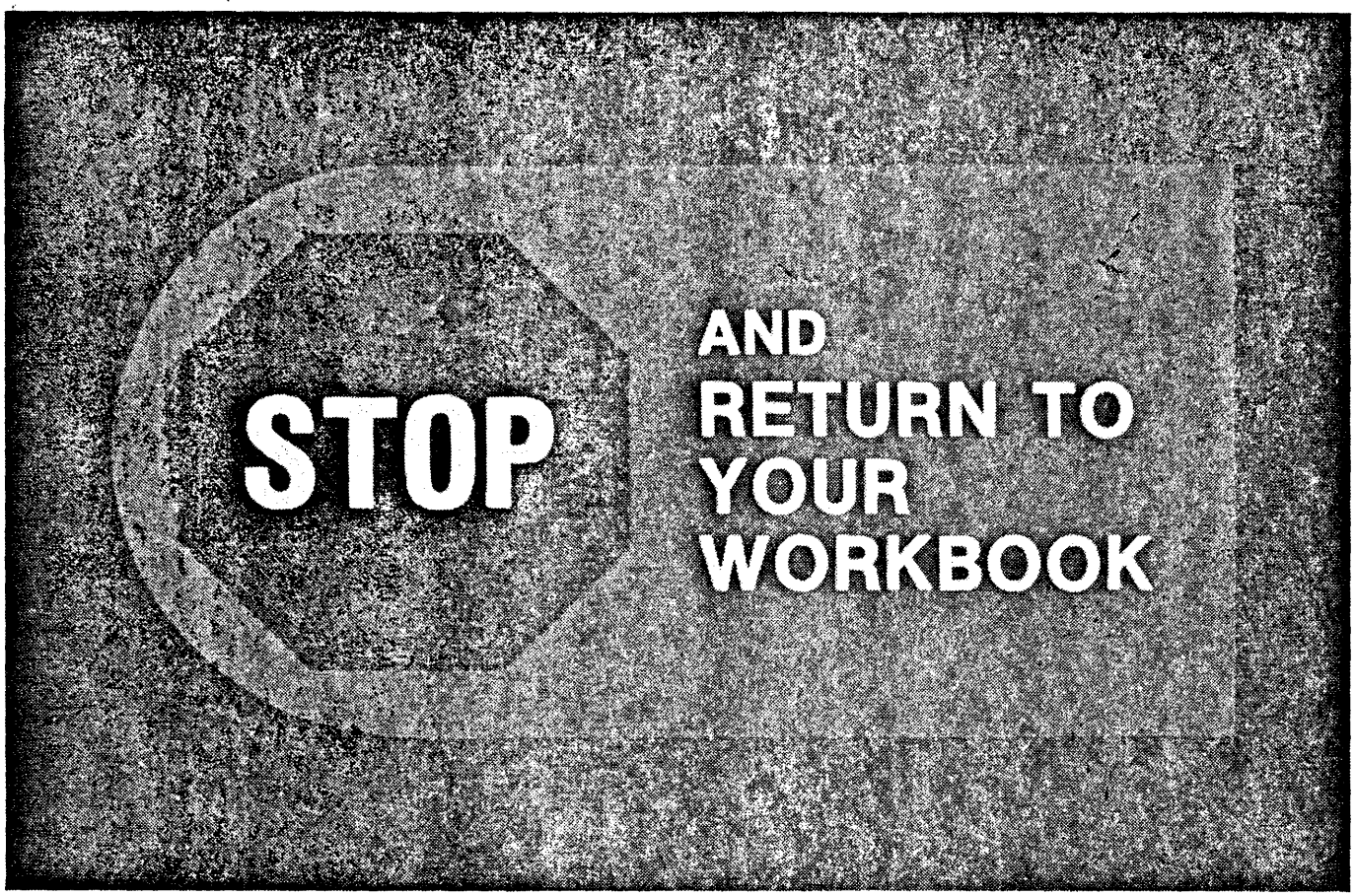


TO OPERATE THE B 9489 ICMD DRIVE, THE OPERATOR IS REQUIRED TO OPEN THE SPRING LOADED DOOR, INSERT THE DISKETTE FULLY INTO THE DRIVE MECHANISM AND CLOSE THE DOOR. ALL SUBSEQUENT OPERATIONS ARE CONTROLLED BY THE HOST SYSTEM.

A UNIT READY INDICATOR IS PROVIDED ON BOTH THE FREESTANDING CABINET AND HOST SYSTEM MOUNTED VERSIONS. THE UNIT READY INDICATOR INDICATES THAT THE DISKETTE IS INSERTED CORRECTLY, THE DOOR IS CLOSED AND THE DISKETTE IS ROTATING AT THE CORRECT SPEED.

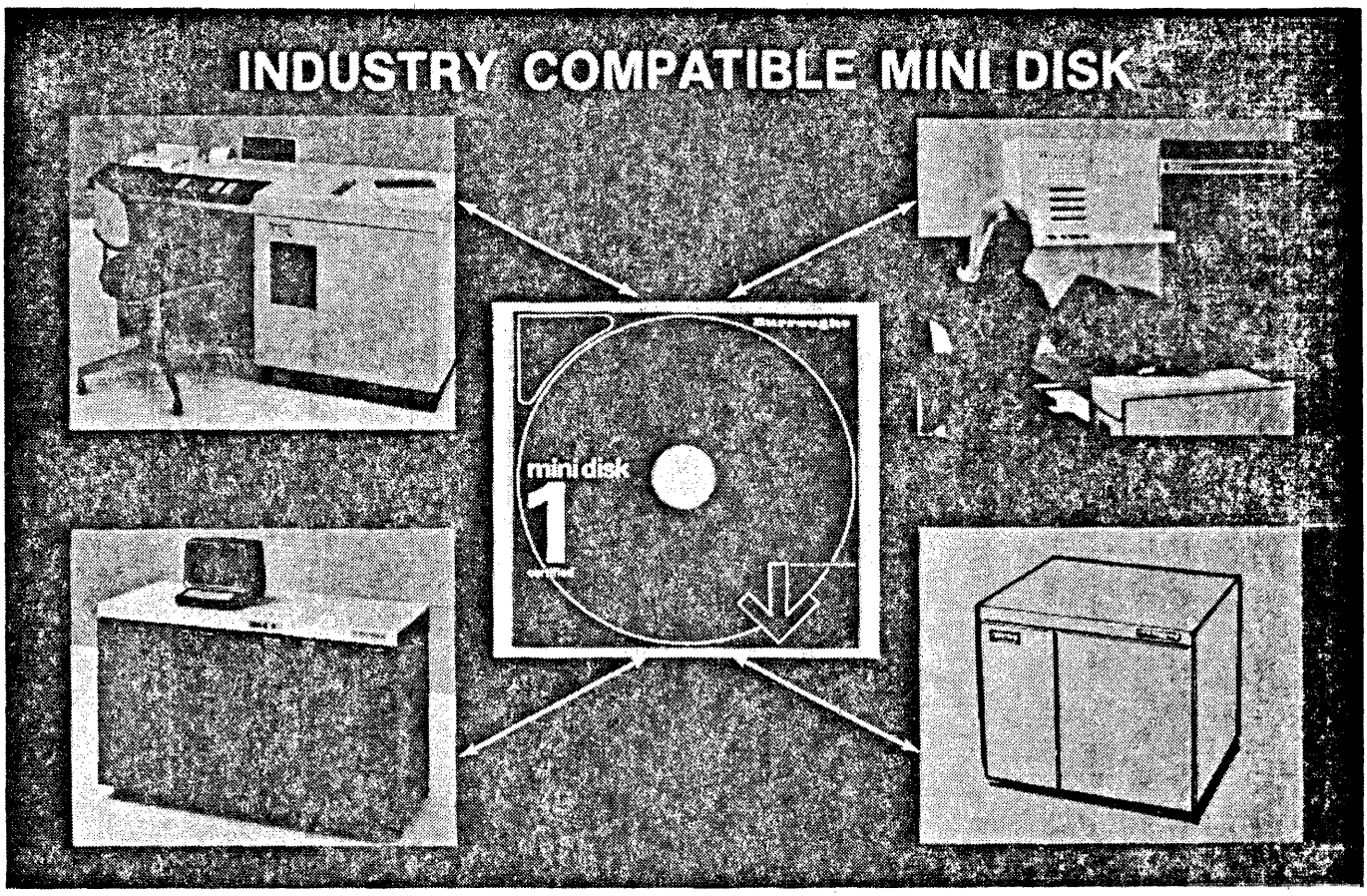
A POWER ON SWITCH IS PROVIDED ON FREE STANDING UNITS WHICH CONTAIN AN INTERNAL POWER SUPPLY, INDEPENDENT OF THE HOST SYSTEM.

24



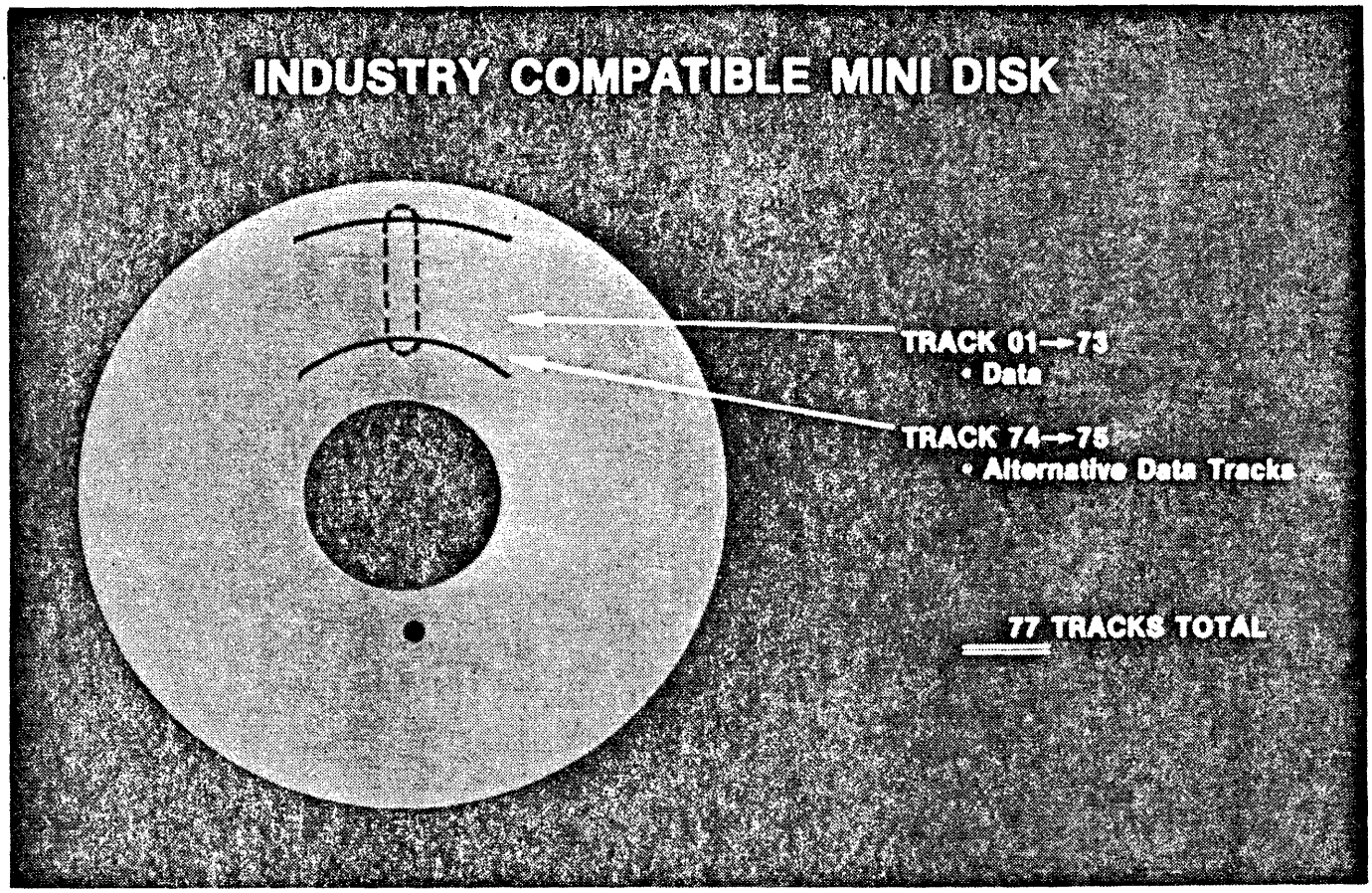
STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

25



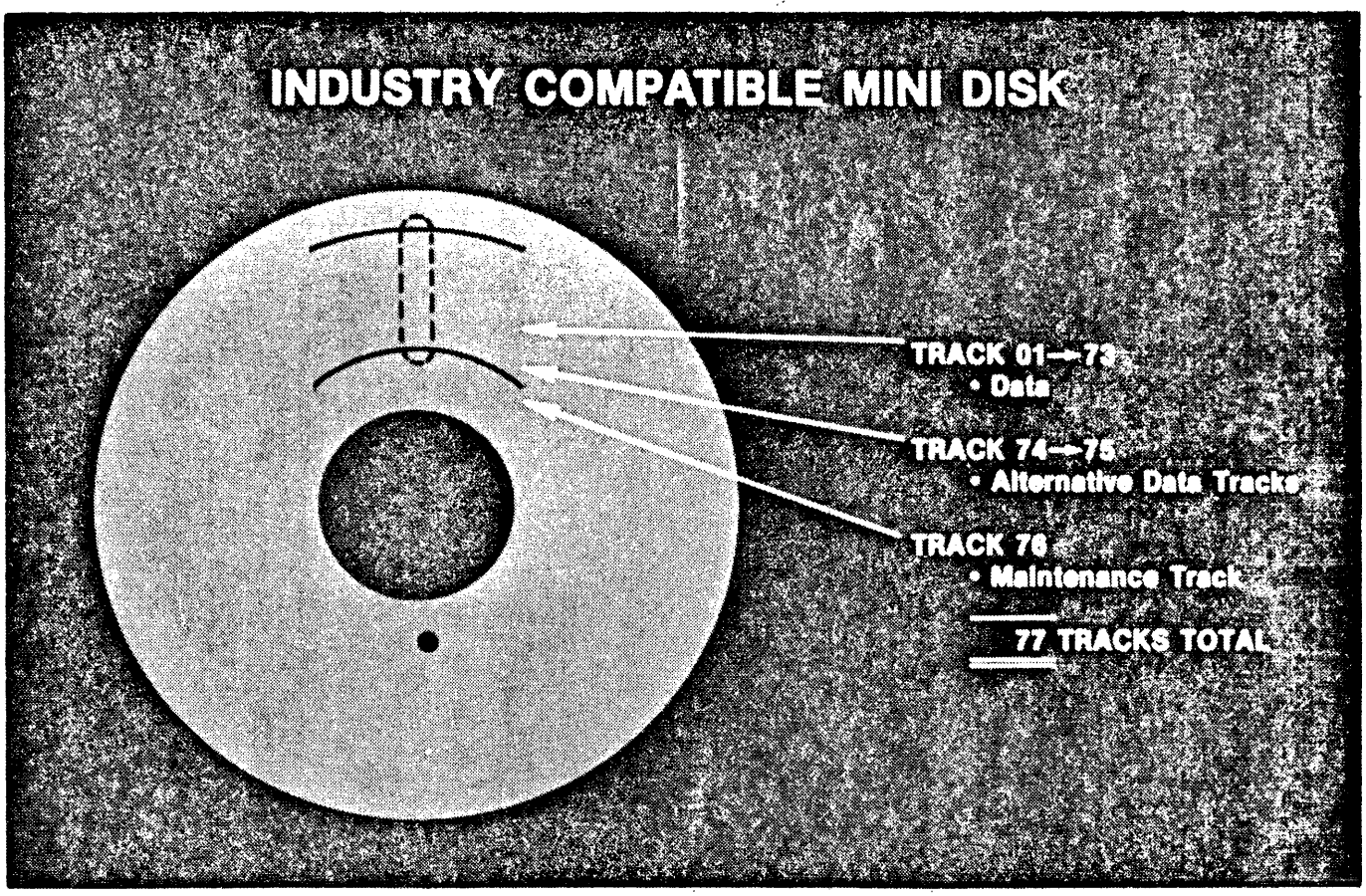
CONTINUING WITH THIS FIRST LECTURE, YOU WILL REMEMBER THAT WE SAID THE MEDIA IS INDUSTRY COMPATIBLE, MEANING THAT THE DATA FORMATS AND ENCODING METHODS USED ON THE DISKETTE ARE THE SAME AS THOSE USED BY OTHER MANUFACTURERS TO ALLOW MEDIA INTERCHANGE BETWEEN DIFFERENT MANUFACTURERS COMPUTER SYSTEMS.

LET US LOOK FIRST AT THE DISKETTE FORMAT AND SECOND, AT THE ENCODING METHOD. BOTH ARE USED TO MAKE THIS MEDIA INTERCHANGE POSSIBLE.



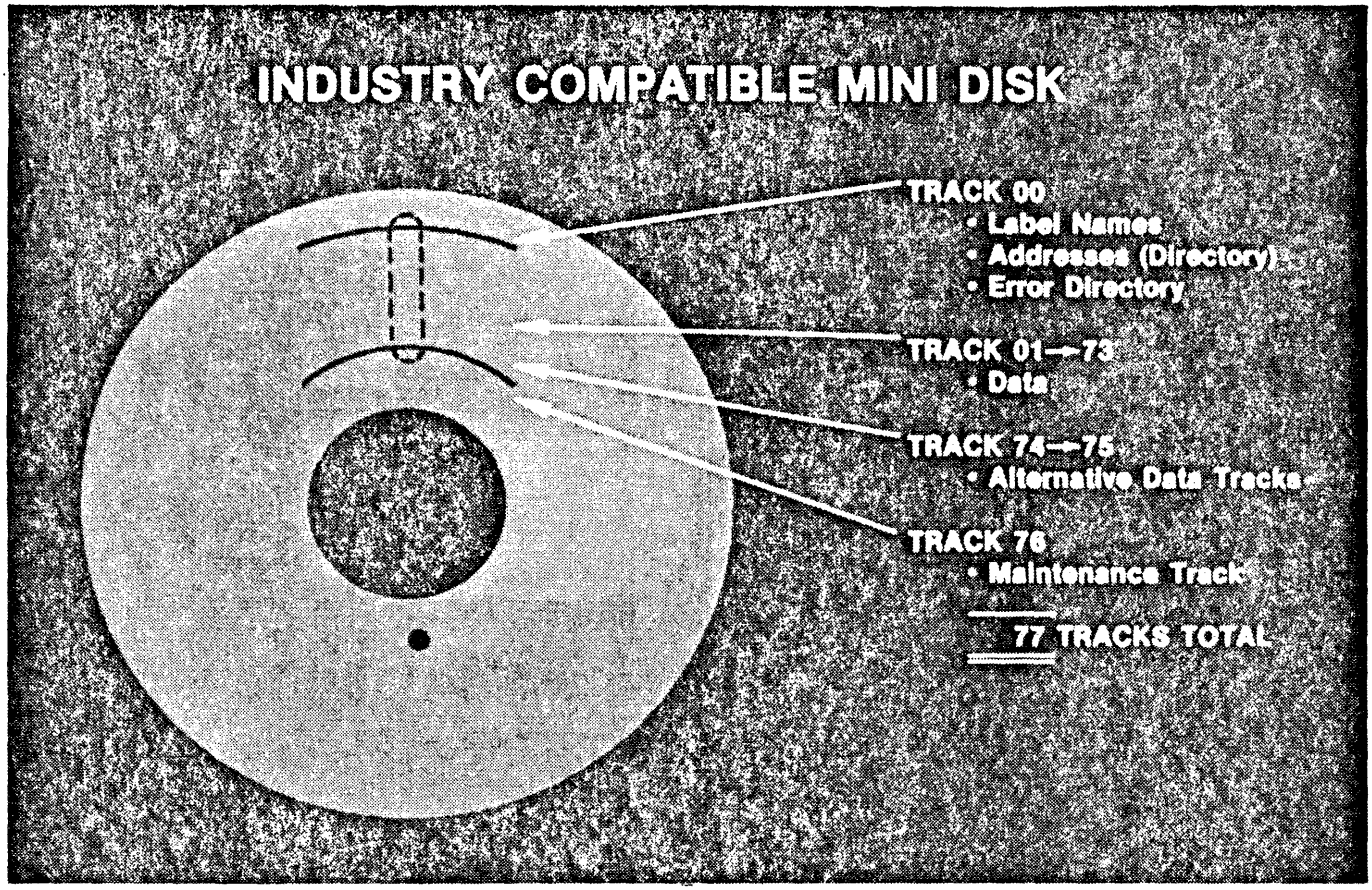
THE DISKETTE HAS A TOTAL OF 77 TRACKS. 73 OF THESE TRACKS ARE USED TO STORE DATA. TWO OF THE REMAINING FOUR TRACKS ARE RESERVED FOR USE AS ALTERNATIVE DATA TRACKS IF ANY OF THE NORMAL 73 TRACKS ARE FOUND TO CONTAIN MEDIA FLAWS AND CONSEQUENTLY CANNOT BE USED.

27



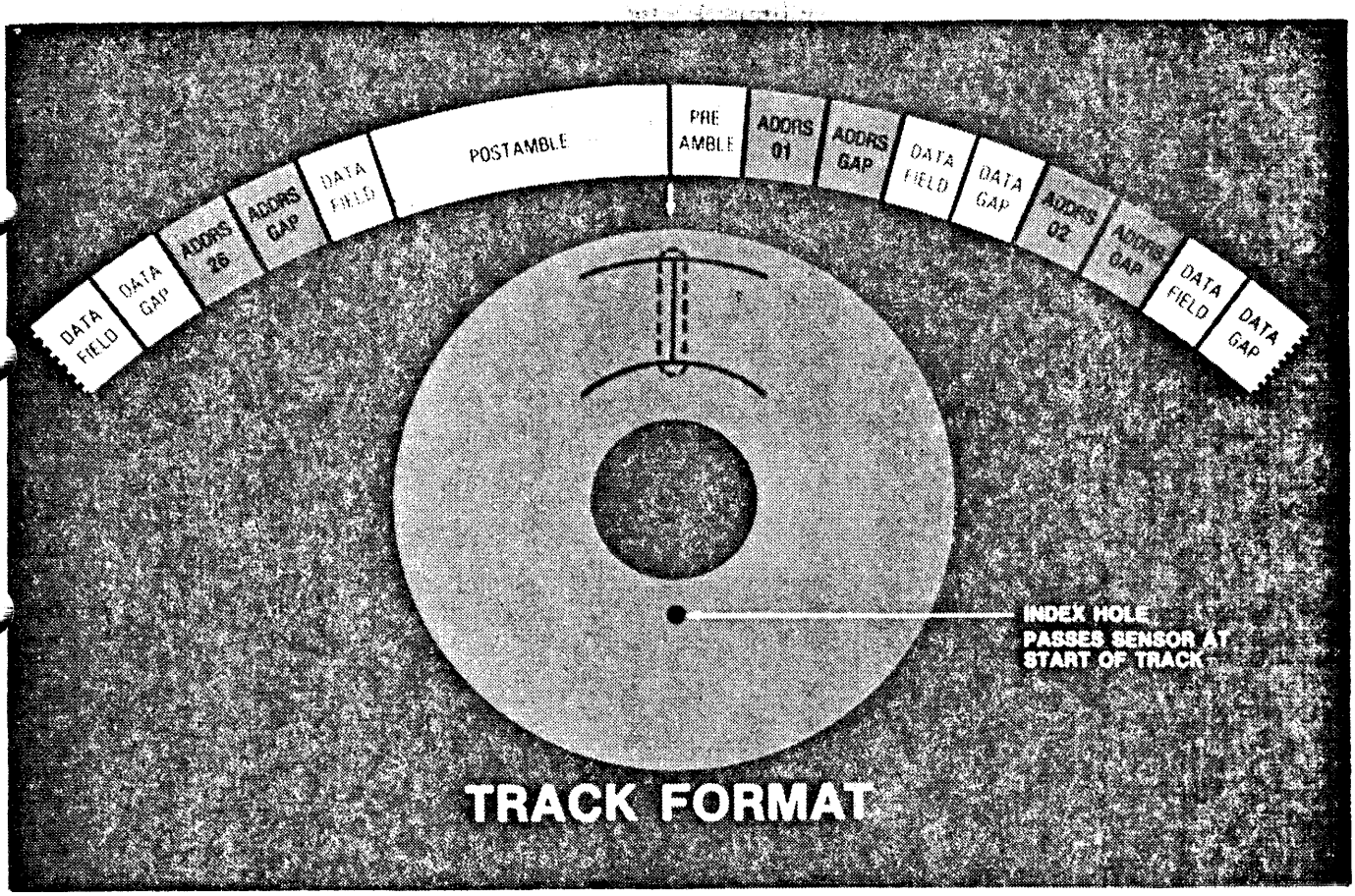
ONE OF THE REMAINING TWO TRACKS IS RESERVED FOR MAINTENANCE PURPOSES AND IS NOT NORMALLY USED BY BURROUGHS.

28



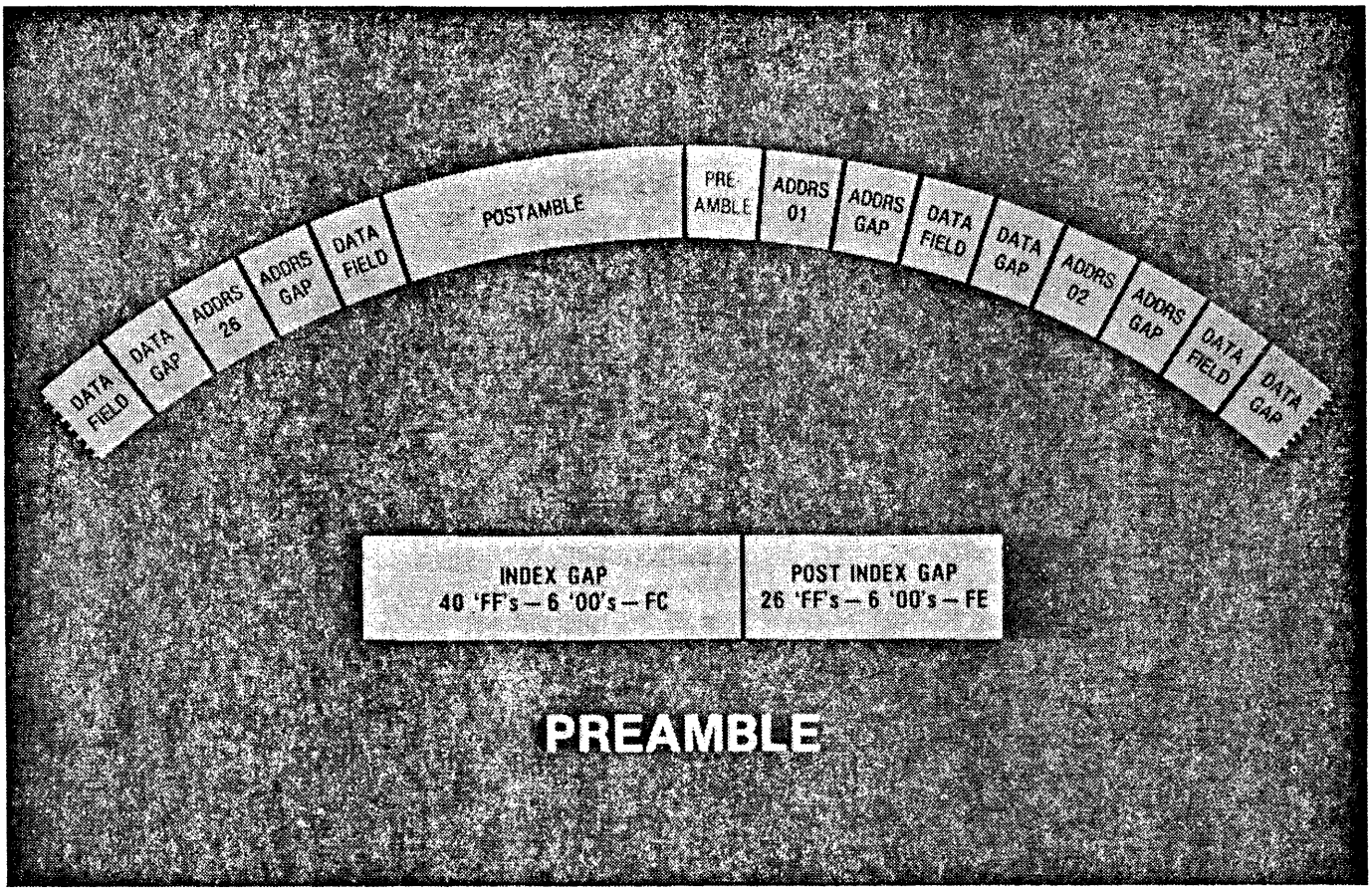
THE REMAINING TRACK IS THE FIRST PHYSICAL TRACK ON THE DISK, TRACK 00, WHICH CONTAINS DESCRIPTIVE INFORMATION ABOUT THE DATA RECORDED ON THE DISKETTE. THIS INFORMATION INCLUDES THE LABEL NAMES OF FILES WRITTEN ON THE DISKETTE, THE DISKETTE ADDRESSES TO INDICATE WHERE THE FILES ARE LOCATED, THE ERROR DIRECTORY, ETC. YOU CAN FIND A DETAILED DESCRIPTION OF THE CONTENT OF THE INDEX TRACK IN SECTION 1 OF THE FIELD ENGINEERING TECHNICAL MANUAL.

29



THE START OF A TRACK IS INDICATED TO THE MINI DISK CONTROLLER IN THE HOST SYSTEM BY THE SIGNAL "INDEX" AS THE INDEX HOLE PASSES THE OPTICAL SENSOR, WHICH IS 180 DEGREES FROM THE READ/WRITE HEAD.

STARTING OPPOSITE THE INDEX HOLE, AT THE START OF A TRACK, THE TRACK CONSISTS OF A SINGLE PREAMBLE FIELD FOLLOWED BY AN ADDRESS FIELD AND AN ADDRESS GAP FIELD. THE ADDRESS GAP FIELD IS FOLLOWED BY A DATA FIELD, SOMETIMES CALLED A SECTOR, AND A DATA GAP FIELD. WITH THE EXCEPTION OF THE PREAMBLE FIELD, THIS SEQUENCE IS REPEATED 26 TIMES WITH THE 26TH DATA FIELD FOLLOWED BY A POSTAMBLE FIELD SIGNIFYING THE END OF THE TRACK.



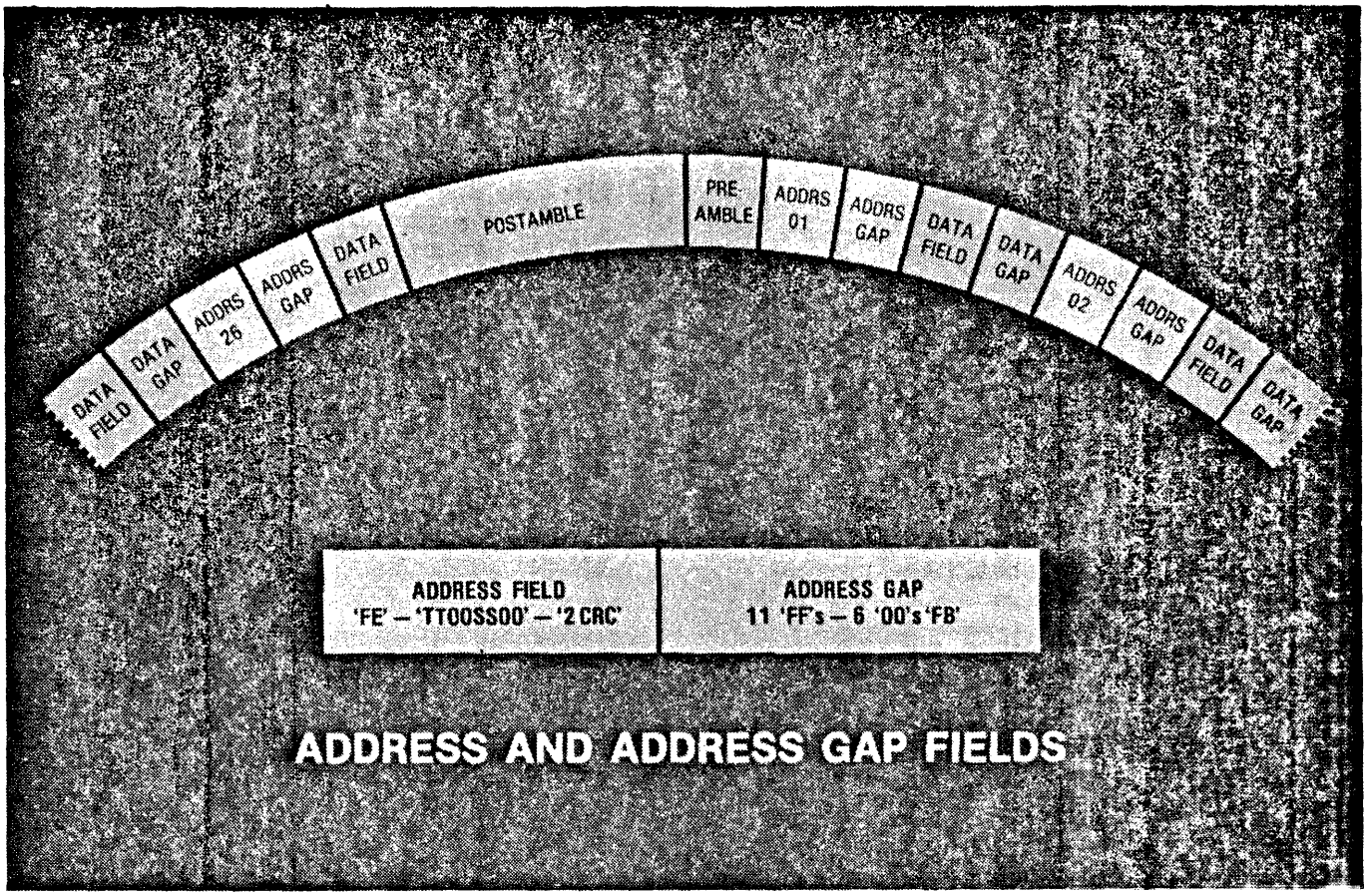
TAKING EACH FIELD IN TURN, THE PREAMBLE FIELD DIVIDES INTO TWO PARTS, THE INDEX GAP AND THE POST INDEX GAP.

THE INDEX GAP CONTAINS 40 "FF" CHARACTERS FOLLOWED BY SIX "00" CHARACTERS. THESE ARE FOLLOWED BY THE HEXADECIMAL CHARACTERS "FC" WHICH ARE THE INDEX SYNC MARK BYTE.

SYNC MARK BYTES ARE USED TO IDENTIFY THE BEGINNING OF FIELDS AND TO SYNCHRONIZE THE READ LOGIC IN THE CONTROLLER.

THE POST INDEX GAP FOLLOWS IMMEDIATELY CONTAINING 26 "FF" CHARACTERS FOLLOWED BY SIX "00" CHARACTERS AND THE ADDRESS SYNC MARK BYTE. THE ADDRESS SYNC MARK BYTE IS THE HEXADECIMAL CHARACTER "FE" TO IDENTIFY THE FOLLOWING FIELD AS AN ADDRESS FIELD.

31



ADDRESS AND ADDRESS GAP FIELDS

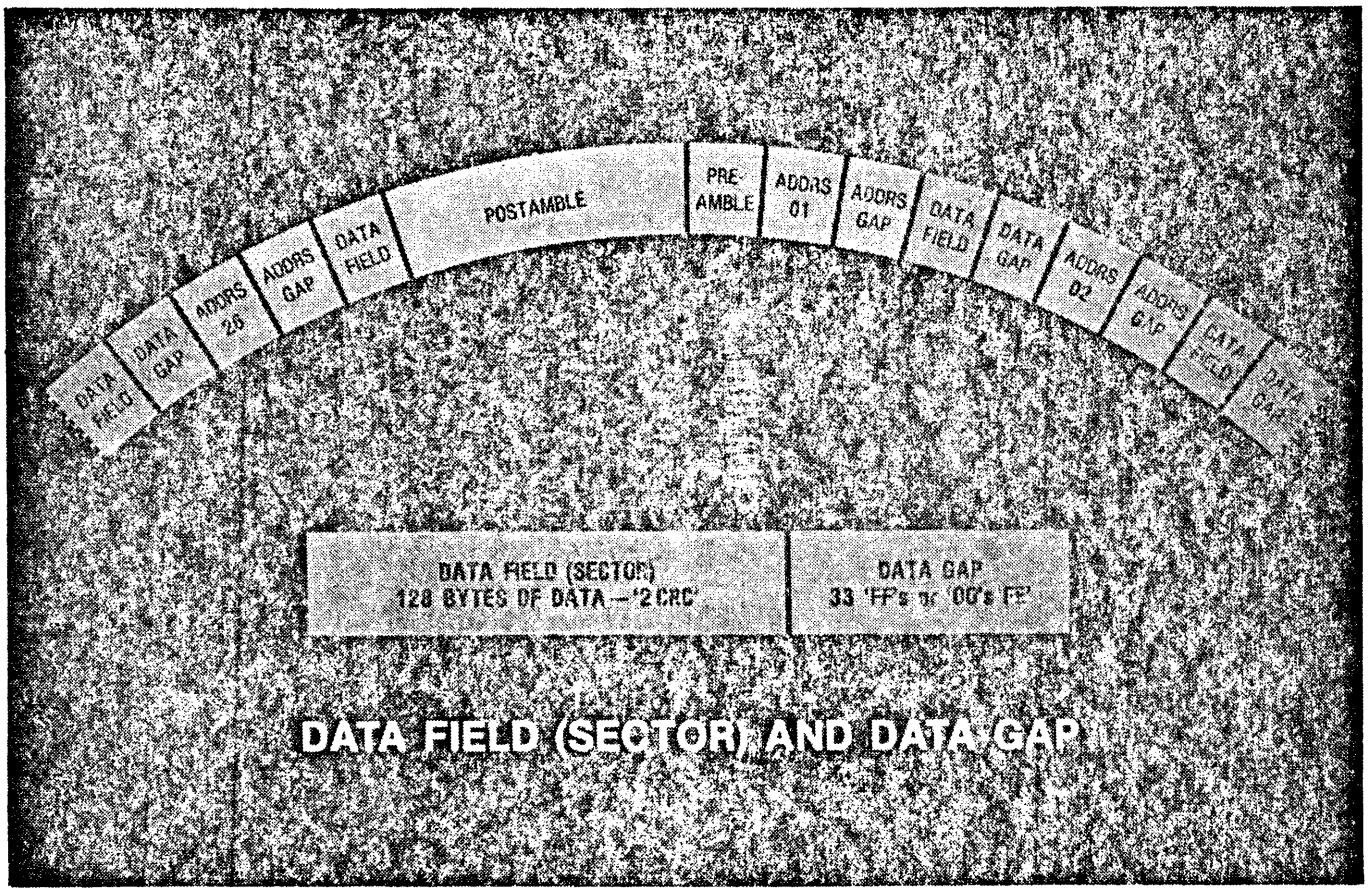
THE FIRST ADDRESS FIELD FOLLOWS THE PREAMBLE AND CONTAINS THE ADDRESS OF THE FIRST DATA FIELD. IN THE FORMAT SHOWN IN THE DIAGRAM, "TT" REPRESENTS THE TRACK ADDRESS IN THE RANGE 00 THROUGH 76, "00" IS A SEPARATOR "SS" REPRESENTS THE SECTOR, THAT IS DATA FIELD ADDRESS, "00" IS ANOTHER SEPARATOR FOLLOWED BY TWO CYCLIC REDUNDANCY CHECK (CRC) CHARACTERS.

TWO CRC CHARACTERS ARE USED AT THE END OF THE ADDRESS FIELD TO ENSURE THAT DATA IS READ BACK CORRECTLY FROM THE DISKETTE.

AN ADDRESS GAP FIELD FOLLOWS EACH ADDRESS FIELD. THIS FIELD CONTAINS NO DATA AND IS USED TO ALLOW TIME FOR THE WRITE LOGIC TO TURN ON, DURING A

WRITE OPERATION, AFTER THE ADDRESS HAS BEEN READ. THE ADDRESS GAP FIELD CONTAINS 11 "FF" CHARACTERS FOLLOWED BY SIX "00" CHARACTERS AND THE DATA SYNCH MARK CHARACTER "FB". NOTE THAT ALTHOUGH THE FIRST 11 CHARACTERS ARE PREFERABLY "FF"S, "00" CHARACTERS ARE PERMISSIBLE AND MAY BE USED BY SOME SYSTEMS.

32

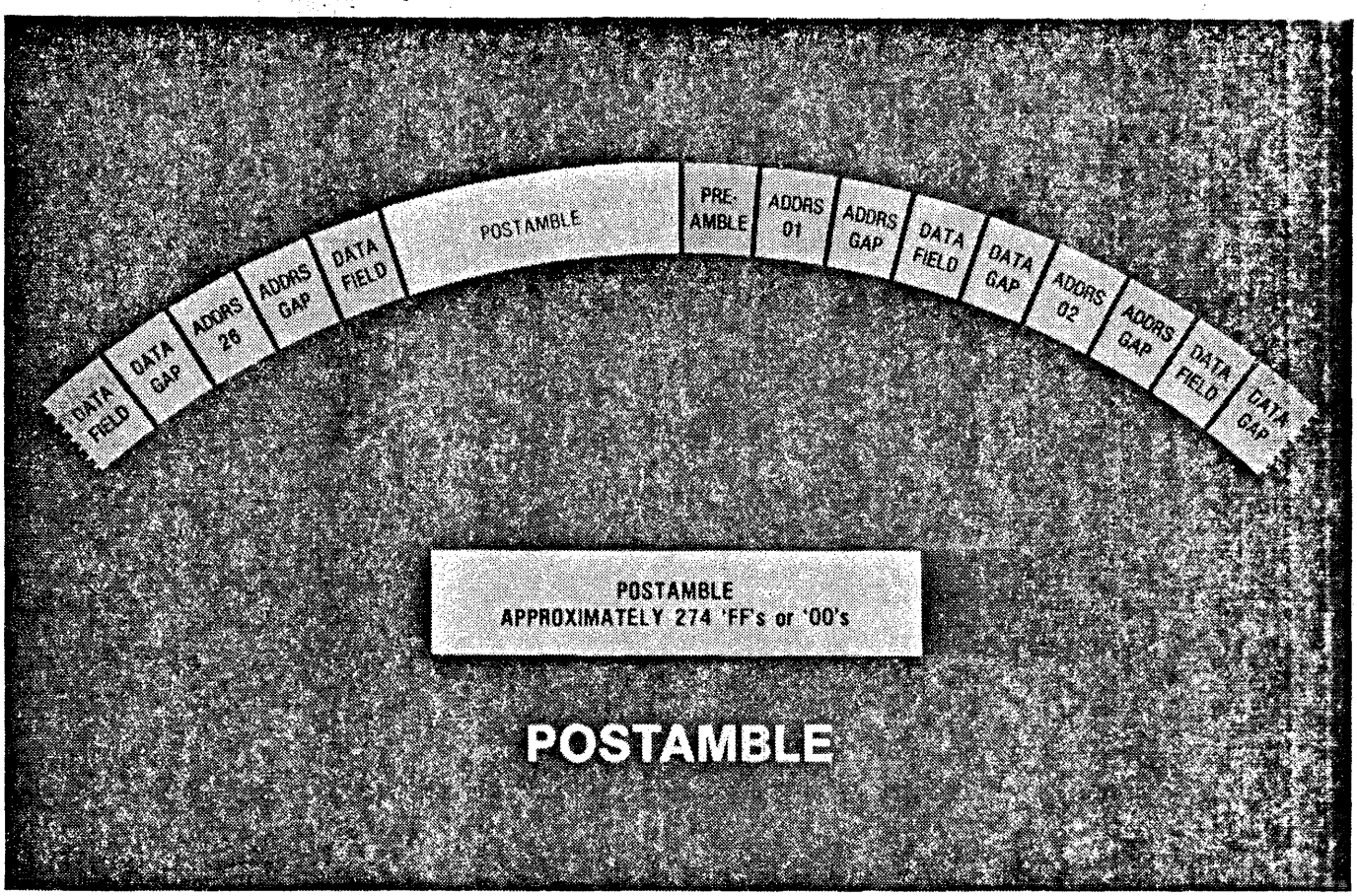


AFTER THE DATA SYNCH MARK CHARACTER "FB" IN THE ADDRESS GAP FIELD COMES THE DATA FIELD OR SECTOR. THIS CONSISTS OF 128 BYTES OF DATA FOLLOWED BY TWO CRC CHARACTERS TO CHECK THAT DATA READ BACK FROM THE DATA FIELD IS CORRECT.

THE DATA FIELD IS FOLLOWED BY A DATA GAP FIELD WHICH LIKE THE ADDRESS FIELD GAP CONTAINS NO DATA. THE DATA GAP FIELD CONTAINS 33 "FF" OR "00"

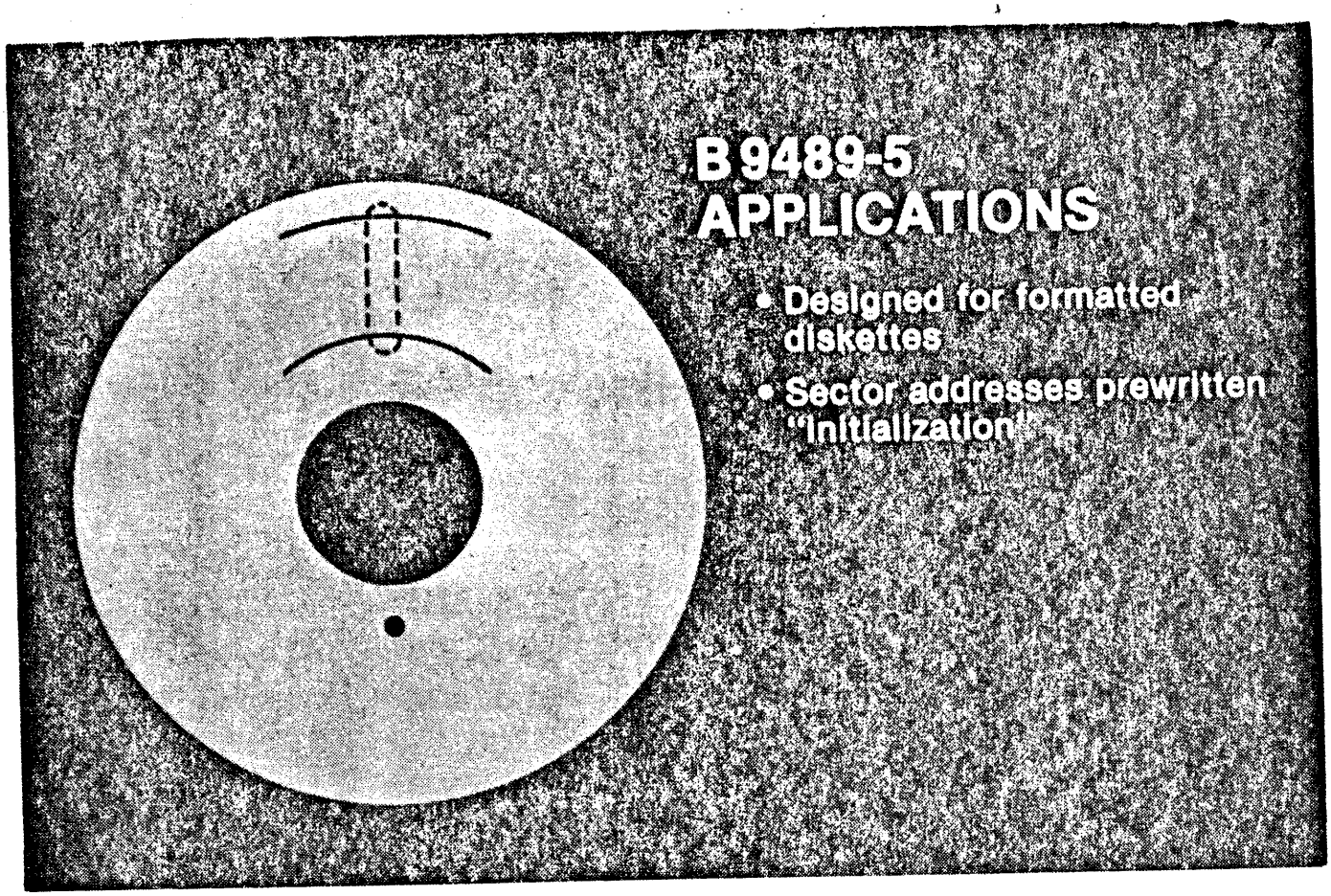
CHARACTERS FOLLOWED BY THE SYNCH MARK CHARACTER "FE" IDENTIFYING THE START OF THE NEXT ADDRESS FIELD.

33



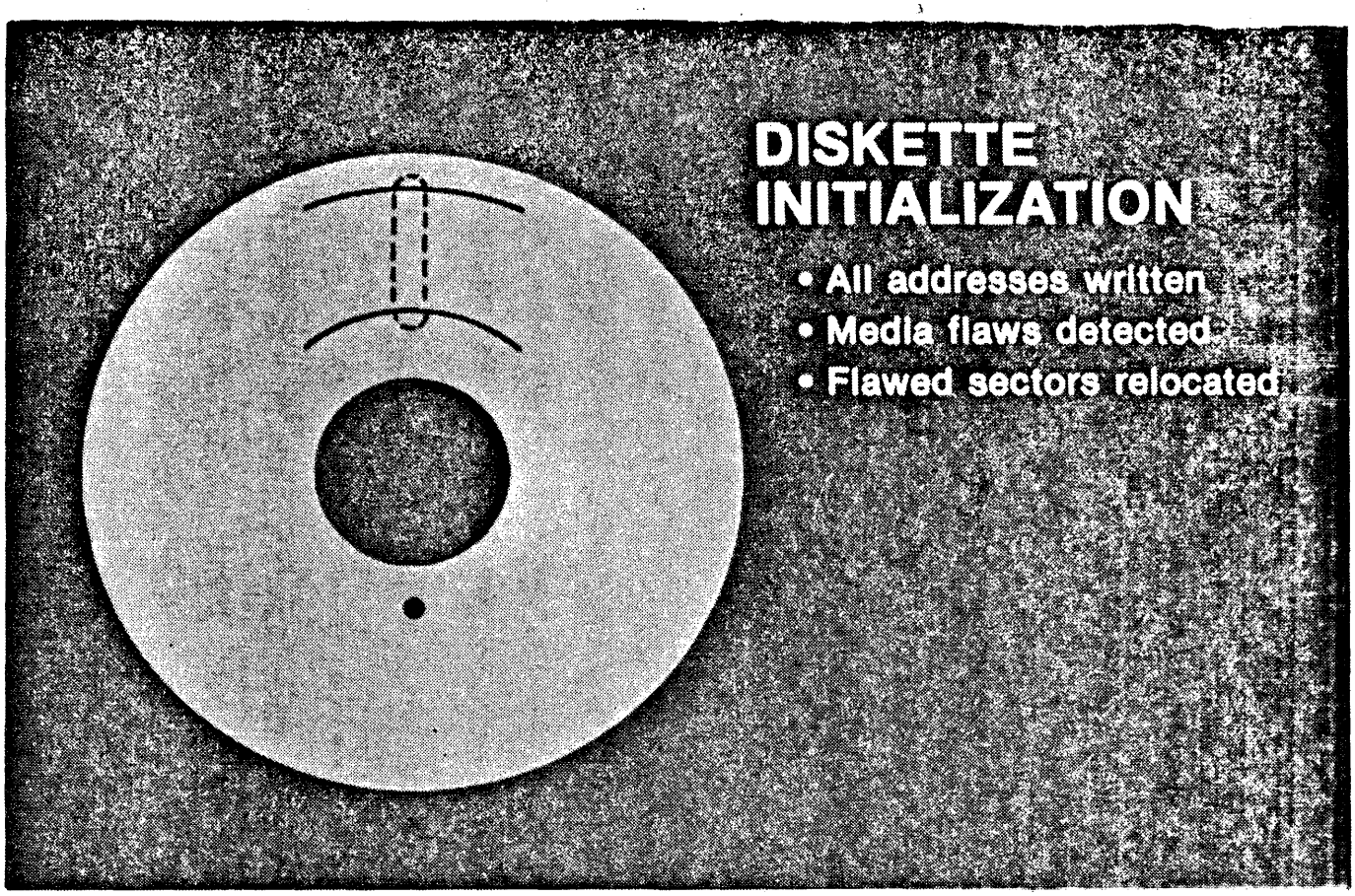
THE SEQUENCE OF ADDRESS FIELD, ADDRESS GAP FIELD, DATA FIELD AND DATA GAP FIELD REPEATS UNTIL THE 26TH SECTOR WHICH IS THE LAST SECTOR ON THE TRACK. THIS IS FOLLOWED IMMEDIATELY BY THE POSTAMBLE FIELD. THE POSTAMBLE FIELD CONSISTS OF "FF" OR "00" CHARACTERS WHICH FILL THE AREA OF TRACK BETWEEN THE END OF THE LAST DATA FIELD AND THE INDEX HOLE. REMEMBER, THE INDEX HOLE INDICATES THE START OF THE TRACK PREAMBLE. THE POSTAMBLE IS NOMINALLY ABOUT 274 CHARACTERS LONG BUT THIS NUMBER WILL VARY DEPENDING ON WRITE FREQUENCY AND DISK SPEED TOLERANCES.

34



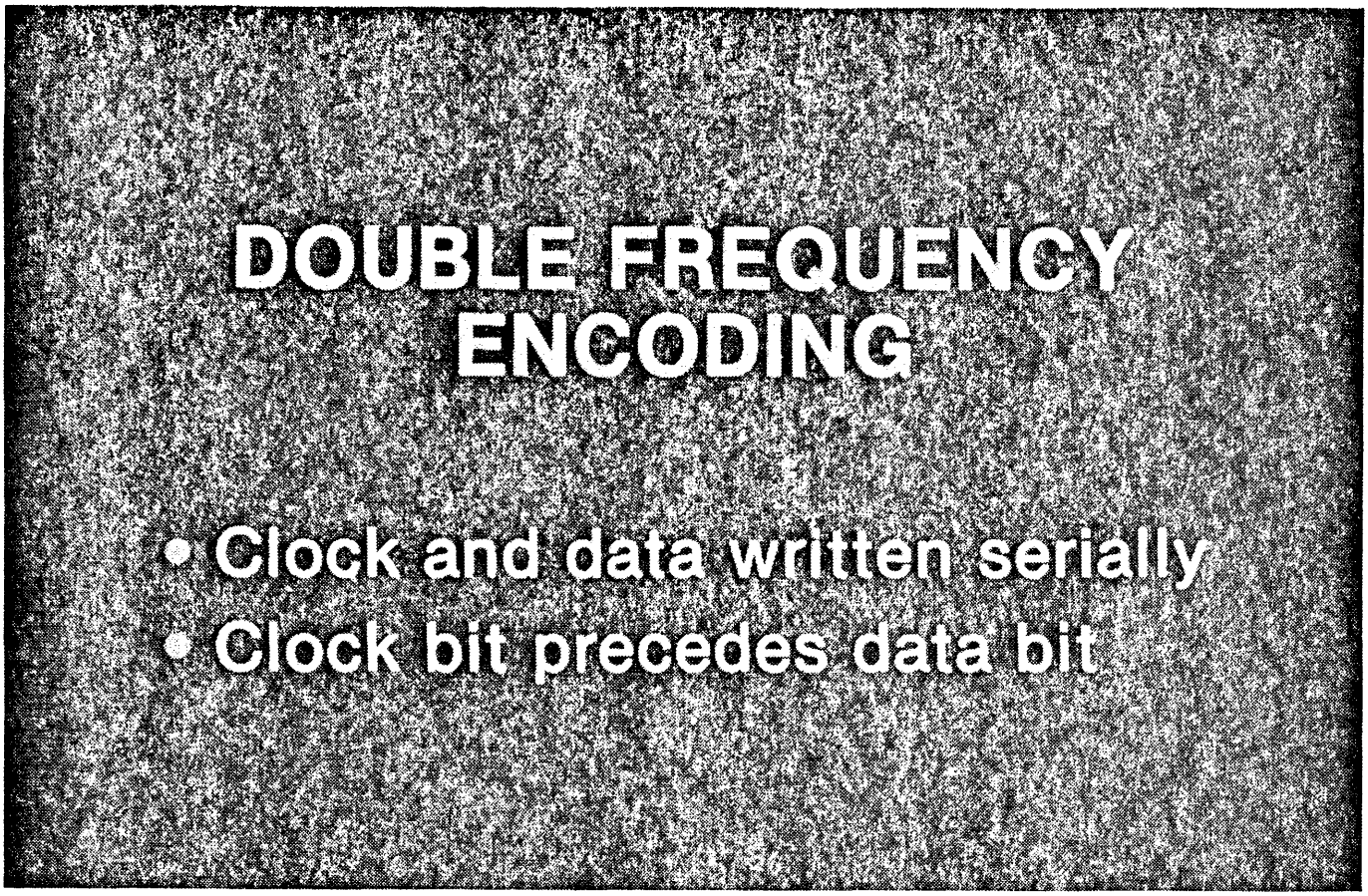
APPLICATIONS FOR WHICH BURROUGHS USES THE B 9489-5 FDD UNIT ARE DESIGNED FOR FORMATTED DISKETTES. FORMATTED DISKETTES HAVE THE SECTOR ADDRESSES PREWRITTEN ON THEM. THE PROCESS OF WRITING THESE ADDRESSES IS CALLED DISK INITIALIZATION.

35



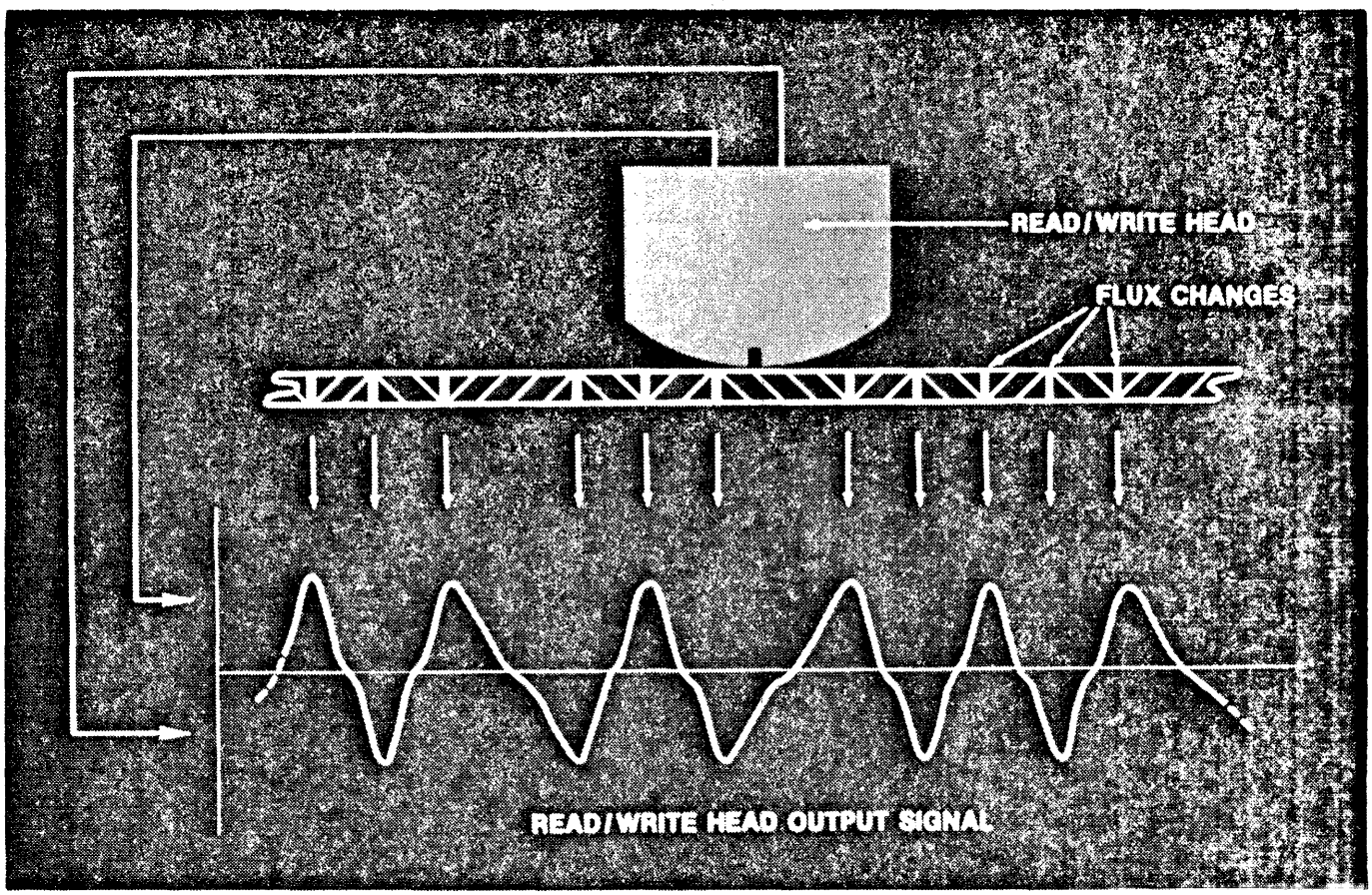
WHEN A DISKETTE IS INITIALIZED, EVERY TRACK IS WRITTEN FROM BEGINNING TO END WITHOUT INTERRUPTION TO ENSURE READABILITY FROM FDD TO FDD. ANOTHER PART OF THE DISKETTE INITIALIZATION SEQUENCE DETERMINES THE PRESENCE OF POSSIBLE MEDIA FLAWS IN EACH TRACK. WHEN A MEDIA FLAW IS ENCOUNTERED IN A TRACK, THE HOST SYSTEM WRITES A SPECIAL DELETED DATA SYNC MARK CHARACTER "F8" IN PLACE OF THE NORMAL "FB" DATA SYNC MARK CHARACTER. THE TRACK AND SECTOR ADDRESS IN WHICH THE MEDIA FLAW IS DETECTED ARE STORED IN THE INDEX TRACK 00 ERROR TRACK DIRECTORY AND AN ALTERNATIVE RECORD LOCATION GIVEN UTILIZING THE TWO SPARE TRACKS.

36



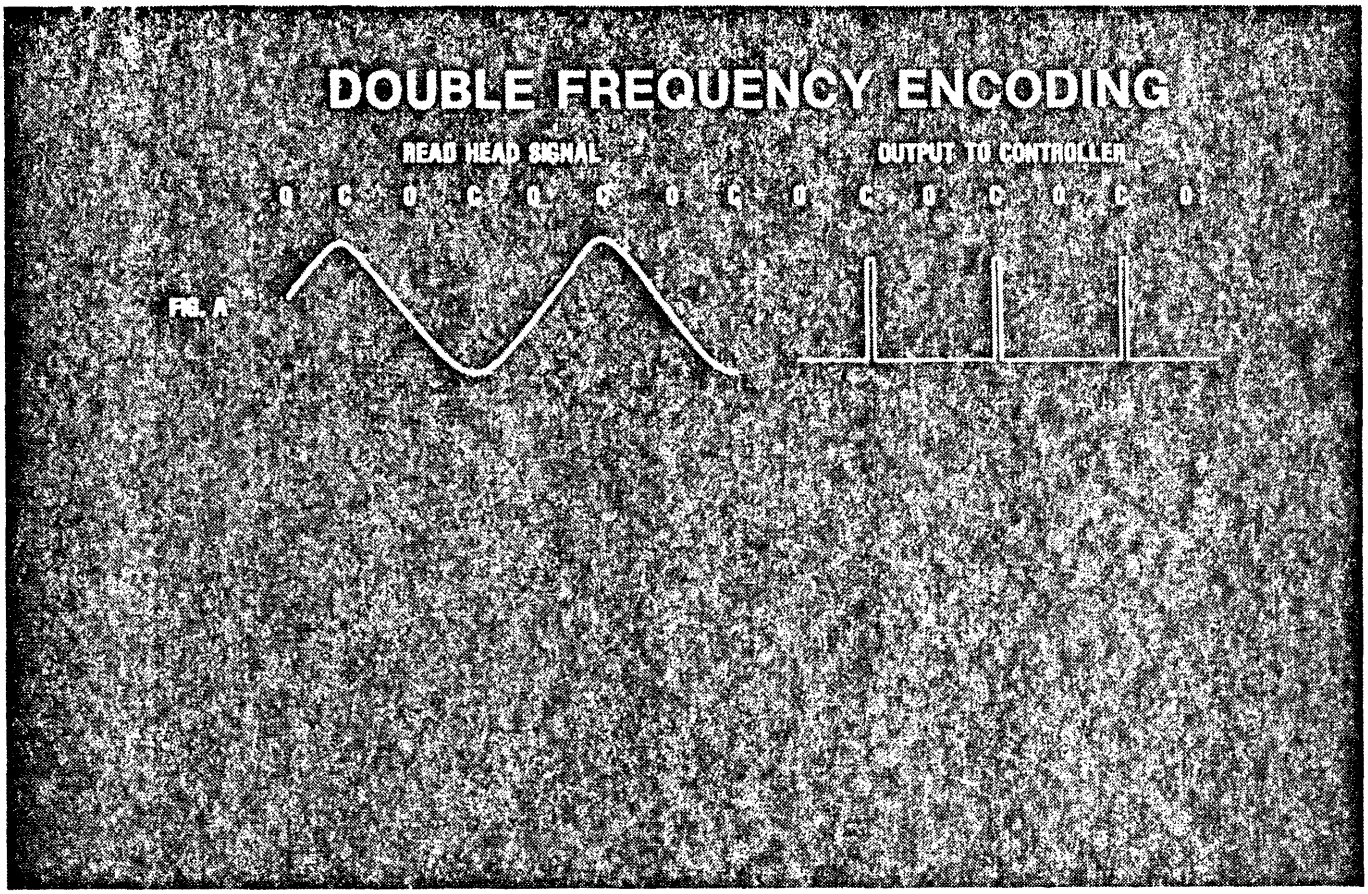
INFORMATION IS WRITTEN ON THE DISKETTE USING A DOUBLE FREQUENCY ENCODING METHOD IN WHICH CLOCK AND DATA BITS ARE WRITTEN SERIALLY WITH EACH DATA BIT PRECEDED BY A CLOCK BIT.

37



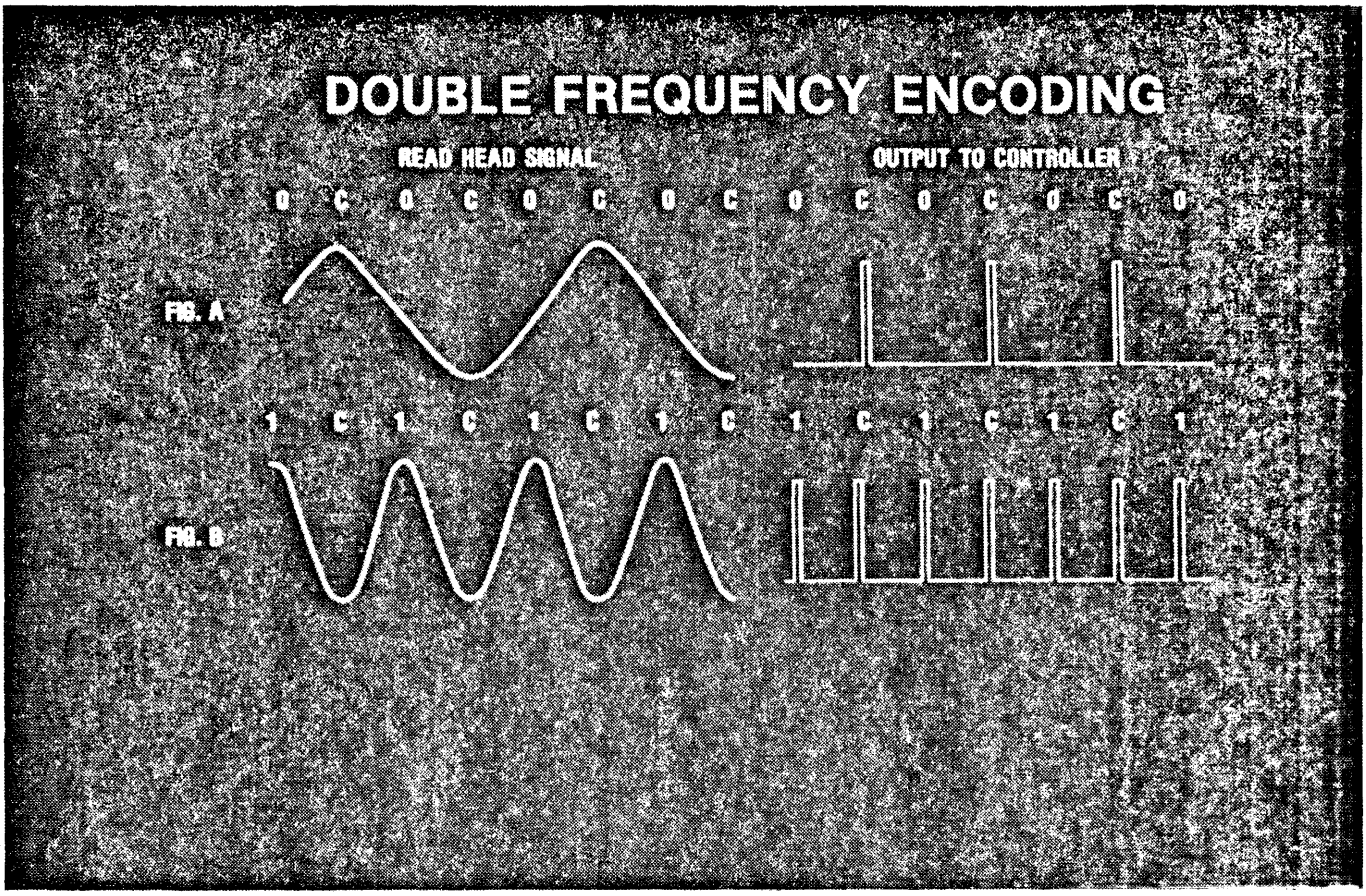
ONE BITS AND CLOCK BITS ARE REPRESENTED BY A CHANGE IN DIRECTION OF MAGNETIC FLUX RECORDED IN THE OXIDE COATING ON THE DISKETTE. WHEN THE DISKETTE ROTATES UNDER THE READ/WRITE HEAD DURING A READ OPERATION, THESE FLUX CHANGES PRODUCE EITHER POSITIVE OR NEGATIVE GOING PEAKS IN THE OUTPUT FROM THE READ/WRITE HEAD DEPENDING ON THE DIRECTION OF THE FLUX CHANGE.

38



THE CLOCKS ACT AS DATA WINDOWS. IF THERE IS NO PEAK BETWEEN CLOCKS, THE DATA BIT IS A ZERO. FIGURE "A" REPRESENTS THE DIFFERENTIAL READ HEAD OUTPUT SIGNAL FOR ALL ZERO BITS. ALL THE PEAKS SHOWN, BOTH POSITIVE AND NEGATIVE GOING, ARE CLOCK BITS. THE READ LOGIC WITHIN THE FDD UNIT PRODUCES A COMPOSITE DIGITAL READ DATA SIGNAL WHICH IS OUTPUT TO THE HOST SYSTEM CONTROLLER. THIS DIGITAL SIGNAL IS REPRESENTED ON THE RIGHT HAND SIDE OF FIGURE "A".

39



IF THERE IS A PEAK BETWEEN CLOCKS THE DATA BIT IS A ONE. FIGURE "B" SHOWS THE DIFFERENTIAL READ HEAD OUTPUT SIGNAL FOR ALL ONE BITS. ALTERNATE PEAKS REPRESENT CLOCK AND ONE BITS, WITH THE COMPOSITE DIGITAL READ SIGNAL OUTPUT TO THE CONTROLLER SHOWN TO THE RIGHT OF THE FIGURE.

40

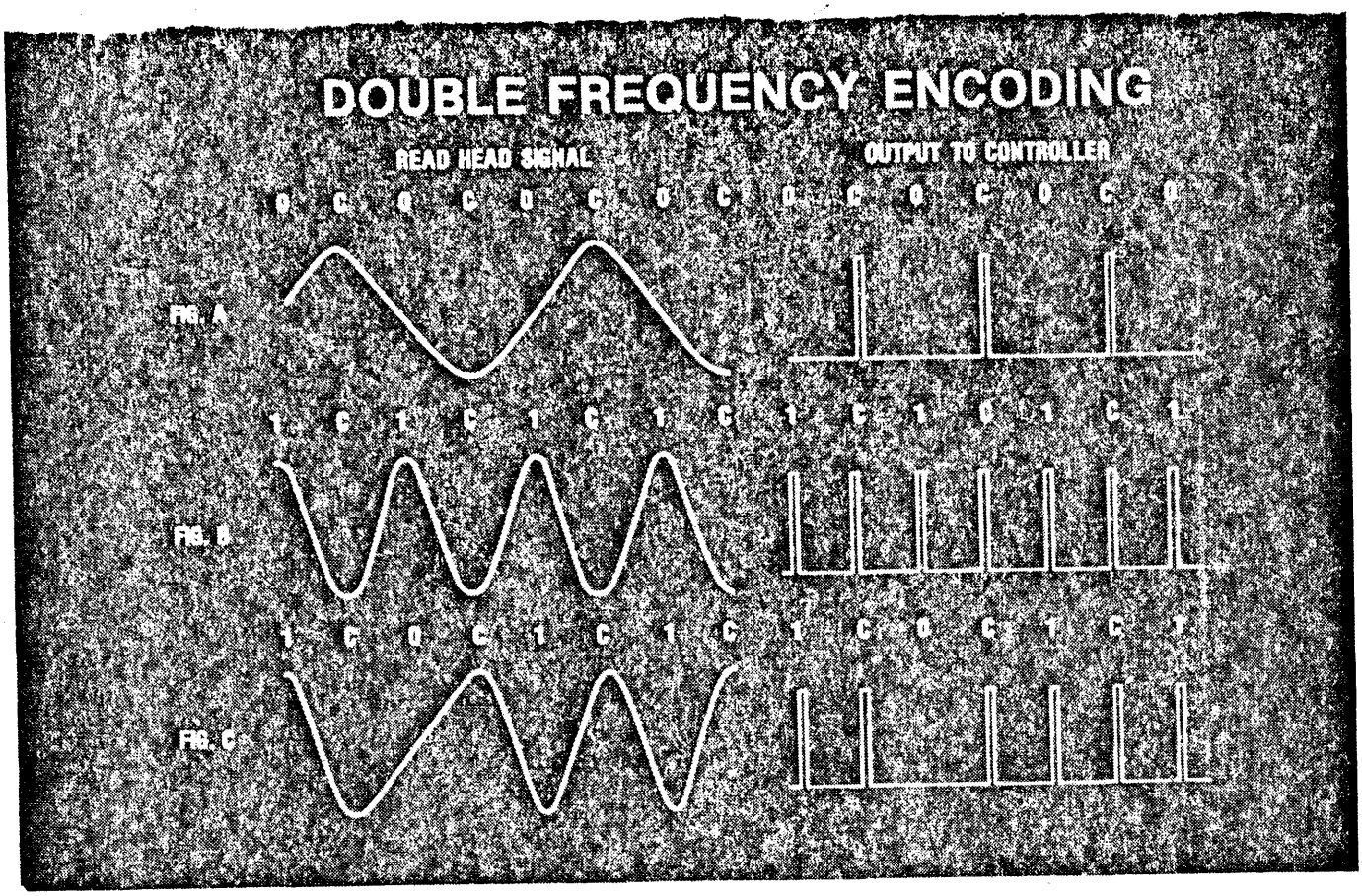
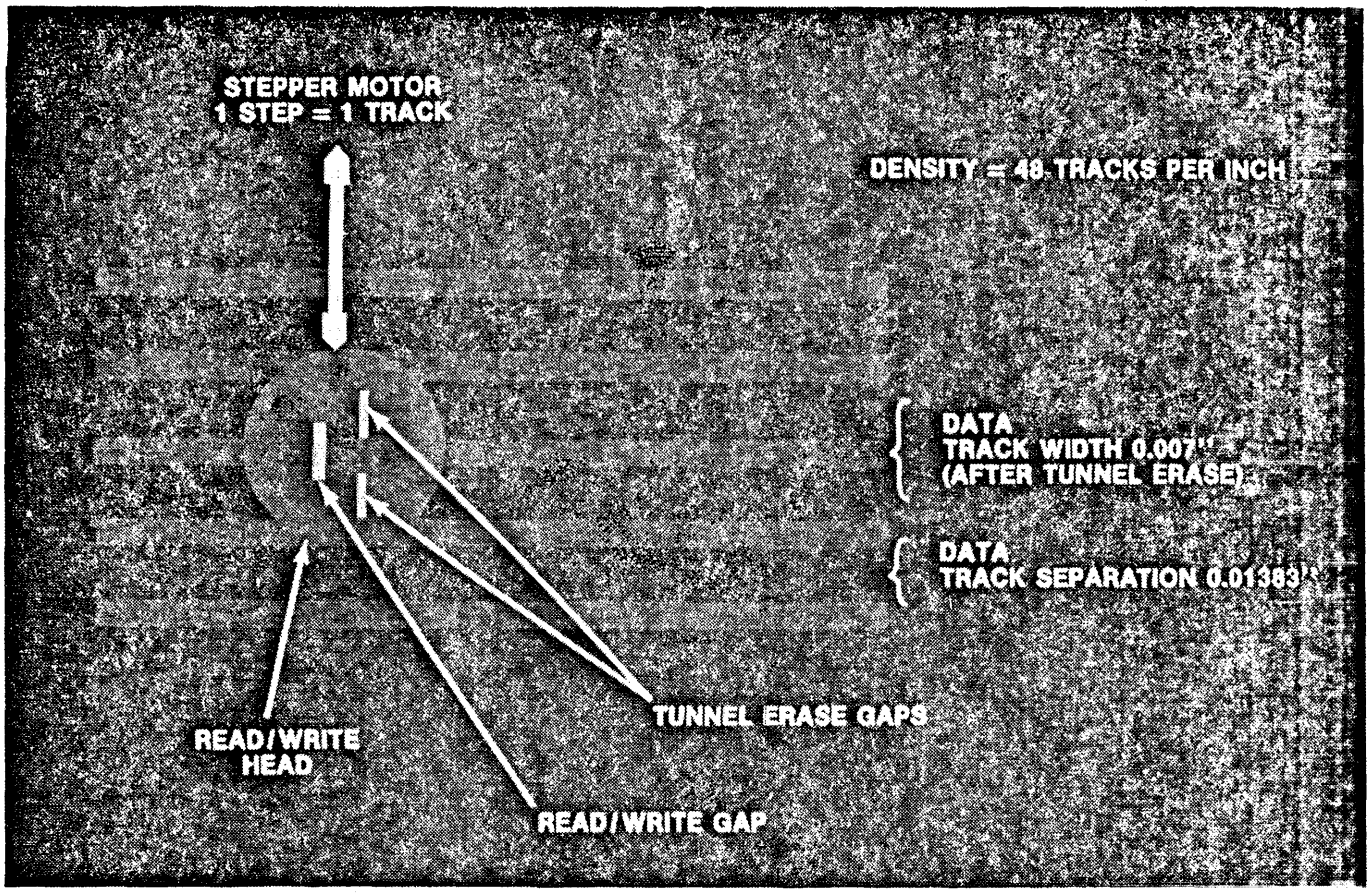


FIGURE "C" REPRESENTS THE DIFFERENTIAL READ HEAD OUTPUT SIGNAL WHEN ONES AND ZEROES ARE MIXED. THE SIGNAL APPEARS MORE COMPLEX BUT THE SAME PRINCIPLE APPLIES. A PEAK, EITHER NEGATIVE OR POSITIVE GOING, REPRESENTS A ONE BIT OR A CLOCK BIT. AGAIN THE DIGITAL READ SIGNAL OUTPUT IS SHOWN TO THE RIGHT OF THE FIGURE.

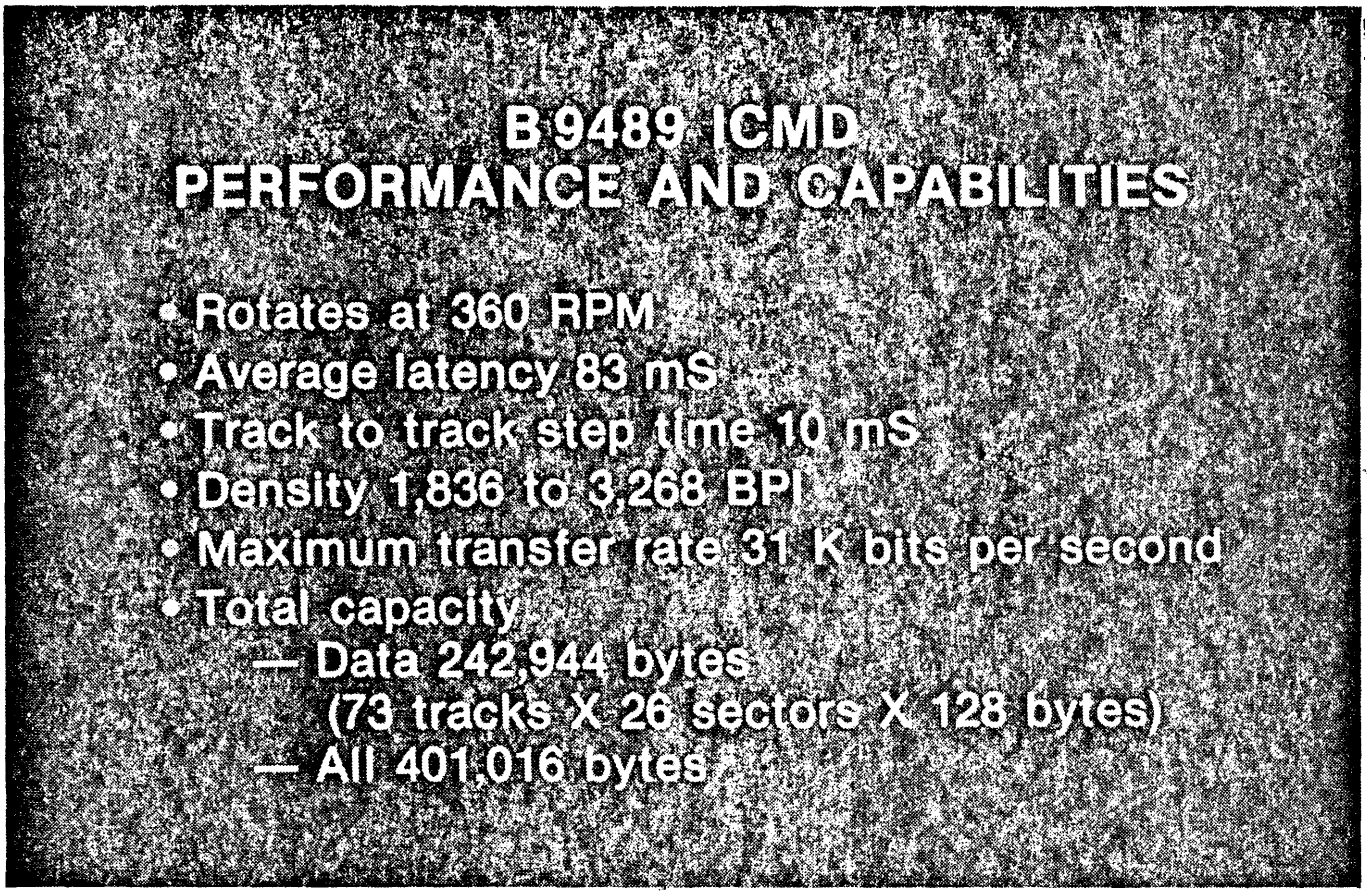
41



THE B 9489-5 ICMD UNIT CONTAINS A SINGLE GAP READ/WRITE HEAD WHICH STEPS BETWEEN TRACKS UNDER THE CONTROL OF A STEPPER MOTOR. BECAUSE HEAD POSITIONING IS FIXED, THE POSITIONING OF THE HEAD RELATIVE TO THE SPINDLE AND THE CORRECT REGISTRATION OF THE DISKETTE ON THE SPINDLE IS CRITICAL. THE TRACK DENSITY IS 48 TRACKS PER INCH, WITH A TRACK WIDTH OF 0.007 INCH.

TO TRIM THE INTER TRACK SPACE DURING A WRITE OPERATION, THE READ/WRITE HEAD PERFORMS A "TUNNEL ERASE" DURING THE WRITE. THIS ERASES 0.01383 OF AN INCH OF THE MAGNETIC OXIDE ON BOTH SIDES OF THE TRACK, MINIMIZING POSSIBLE NOISE FROM OLD DATA CAUSED BY TOLERANCES IN HEAD ALIGNMENT WITH EACH TRACK.

42



THIS IS A SUMMARY OF THE PERFORMANCE CHARACTERISTICS AND CAPACITIES OF THE ICMD FLEXIBLE DISK DRIVE UNIT. THE DISKETTE IS ROTATED BY THE SPINDLE AT 360 REVOLUTIONS PER MINUTE, GIVING AN AVERAGE LATENCY, THAT IS THE AVERAGE TIME TO REACH A GIVEN ADDRESS ON A TRACK WITHOUT HEAD MOVEMENT, OF 83 MILLISECONDS. THE TIME TAKEN FOR THE READ/WRITE HEAD TO

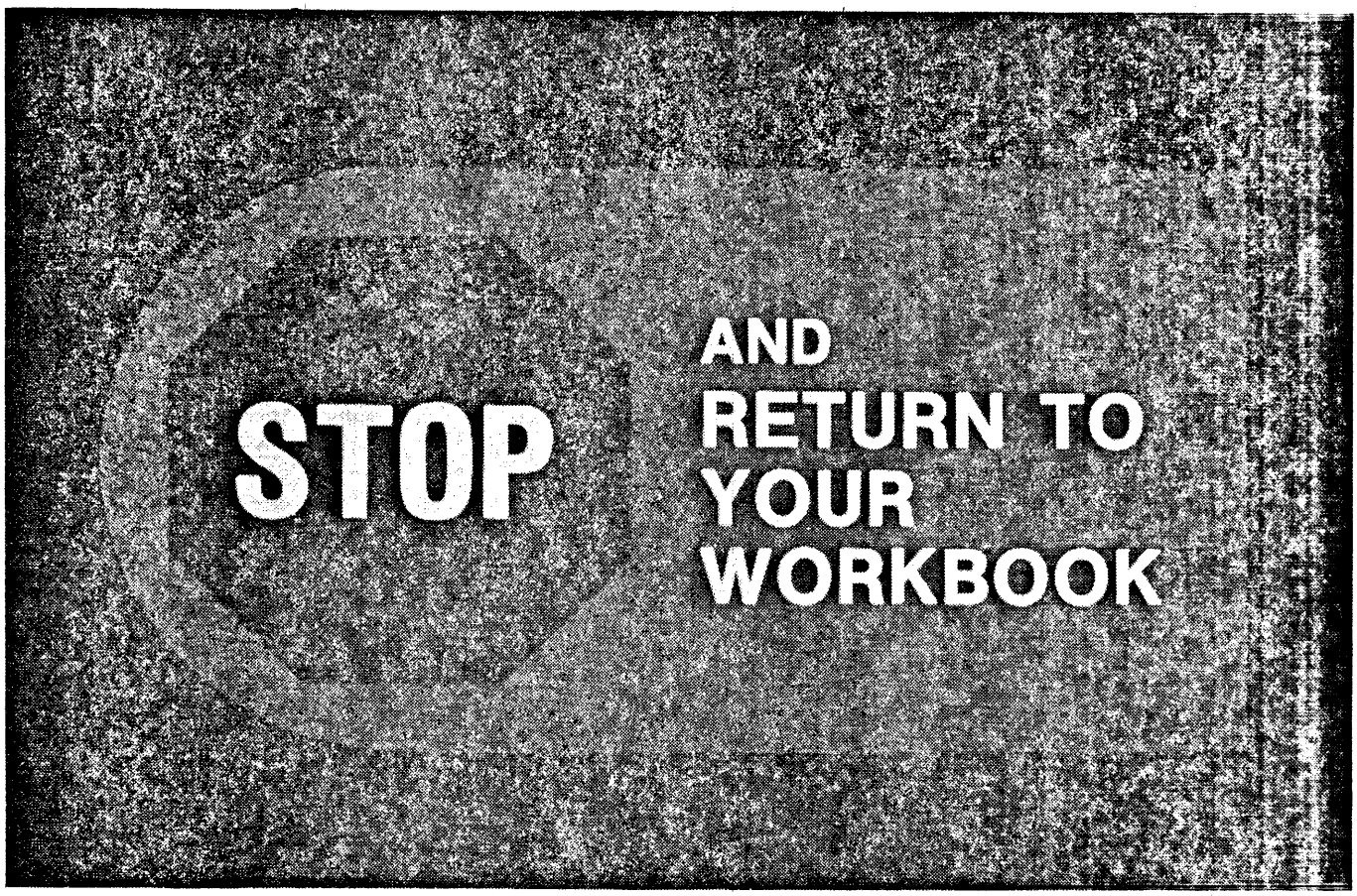
STEP BETWEEN TRACKS IS 10 MILLISECONDS PER TRACK.

THE RECORDING DENSITY INCREASES TOWARD THE INNER TRACKS FROM 1,836 BITS PER INCH ON THE OUTER TRACK TO 3,268 BITS PER INCH ON THE INNER TRACK.

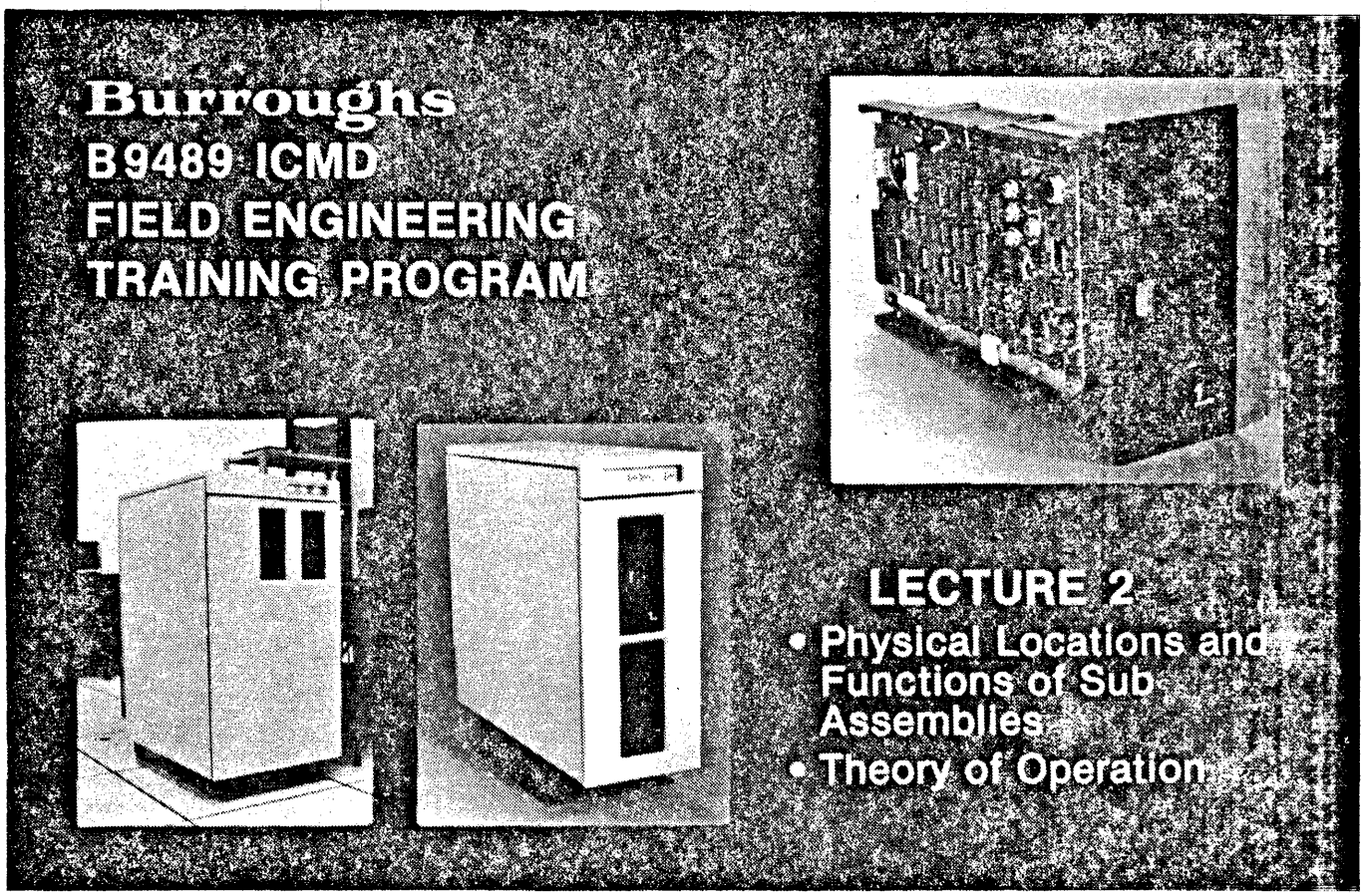
DURING A WRITE OR READ OPERATION, DATA IS TRANSFERRED TO OR FROM THE DISKETTE AT A RATE OF 31 KILOBYTES PER SECOND.

THE DATA CAPACITY OF THE DISKETTE IS A TOTAL OF 242,944 DATA BYTES, BEING 73 TRACKS OF 26 SECTORS EACH CONTAINING 128 BYTES. THE TOTAL CAPACITY OF THE DISK INCLUDING ALL ADDRESS FIELD, GAP FIELDS AND THE INDEX TRACK IS 401,016 BYTES.

43

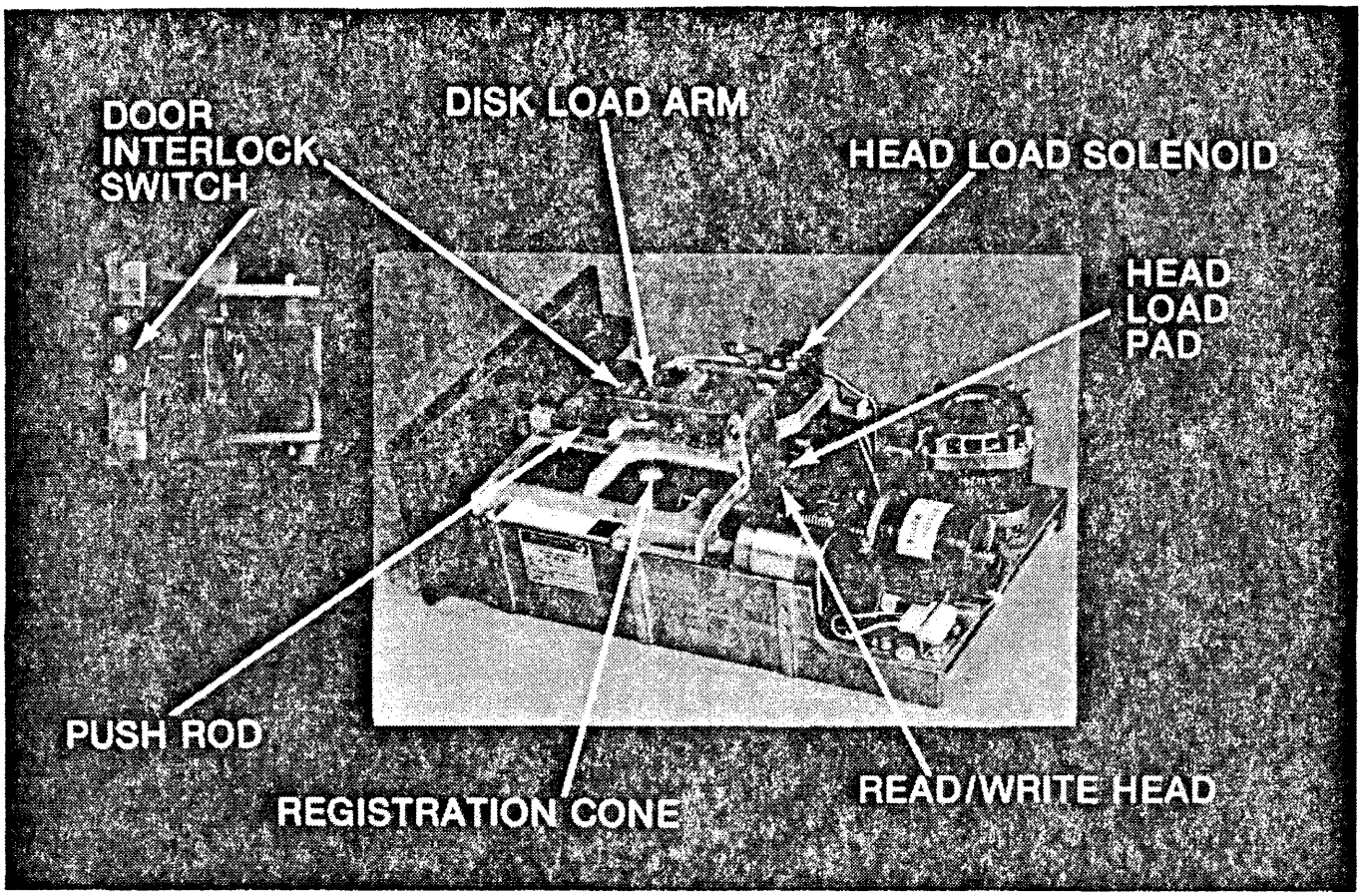


THE SUMMARY OF PERFORMANCE CHARACTERISTICS AND CAPACITIES OF THE UNIT COMPLETES THIS FIRST LECTURE IN THE BURROUGHS B 9489 ICMD TRAINING PROGRAM. RETURN TO YOUR WORKBOOK AND COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.



THIS IS THE SECOND LECTURE IN THE BURROUGHS B 9489 INDUSTRY COMPATABLE MINI DISK (ICMD) TRAINING PROGRAM. THE LECTURE IS DIVIDED INTO TWO SECTIONS. THE FIRST SECTION IDENTIFIES THE PHYSICAL LOCATIONS AND FUNCTIONS OF THE MAJOR SUBASSEMBLIES IN THE UNIT. THE SECOND SECTION DESCRIBES THE THEORY OF OPERATION OF THE UNIT.

2



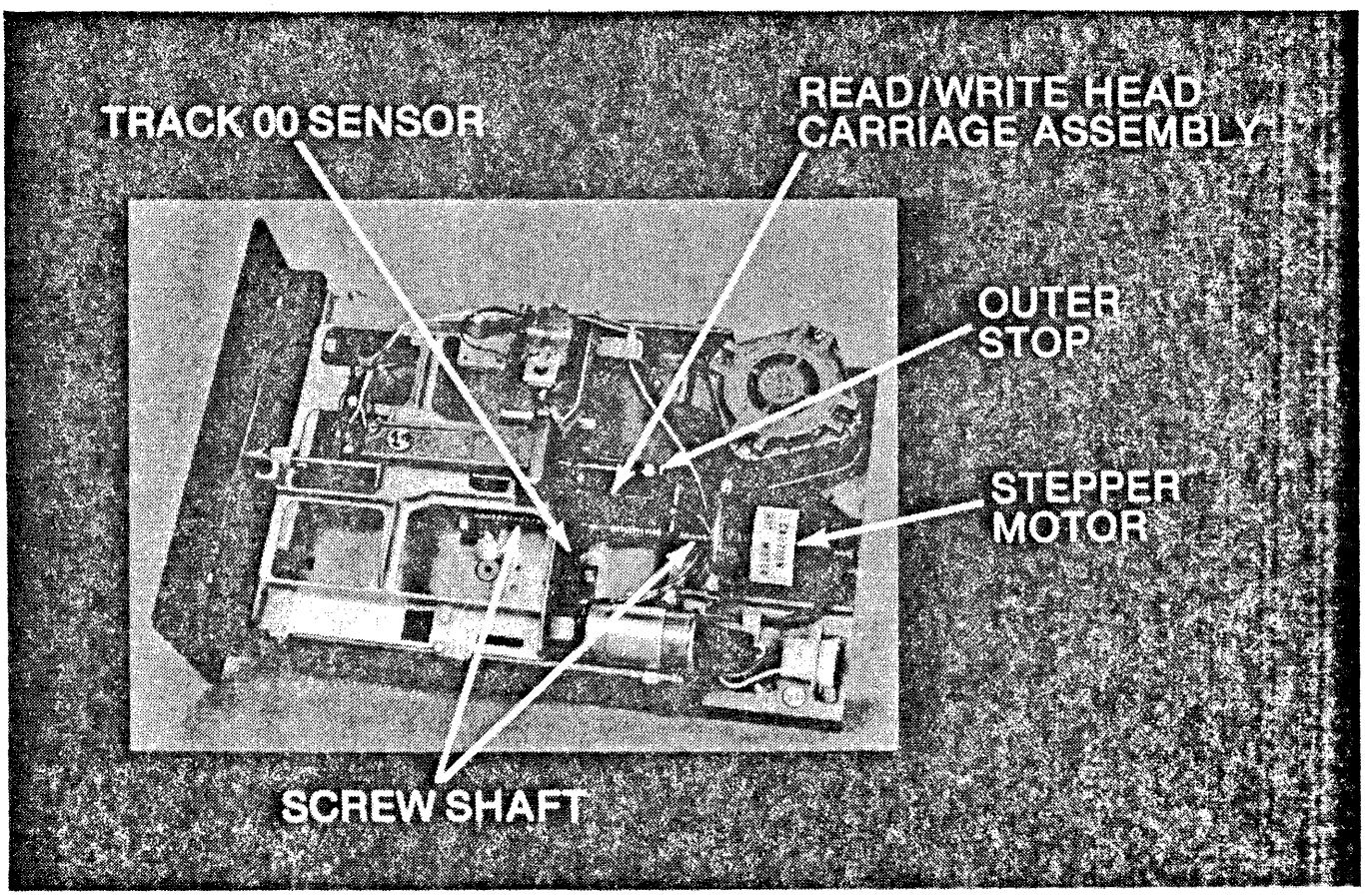
THE PICTURE SHOWS A B 9489-5 UNIT, REMOVED FROM THE HOST SYSTEM AND IDENTIFIES SOME OF THE MAJOR SUBASSEMBLIES. CLOSING THE DOOR MOVES THE PUSHROD WHICH ENGAGES THE DISK LOAD ARM. THE DISK LOAD ARM MOVES THE REGISTRATION CONE TO CLAMP THE DISKETTE TO THE SPINDLE.

THE REGISTRATION CONE IS NOT CLEARLY VISIBLE IN THIS PICTURE BUT IS SHOWN LATER WITH THE UNIT PARTIALLY DISASSEMBLED.

THE DISK LOAD ARM ALSO ACTIVATES THE DOOR INTERLOCK SWITCH. CLOSING THE DOOR INTERLOCK SWITCH ENABLES THE HOST SYSTEM CONTROLLER TO LOAD THE READ/WRITE HEAD BY ENERGIZING THE HEAD LOAD SOLENOID.

WHEN THE HEAD LOAD SOLENOID IS ENERGIZED, THE HEAD LOAD BAIL MOVES FORWARD ALLOWING THE SPRING LOADED HEAD LOAD PAD TO CONTACT THE BACK SURFACE OF THE DISKETTE. THE PRESSURE FROM THIS PAD MAINTAINS CLOSE CONTACT BETWEEN THE READ/WRITE HEAD AND THE MAGNETIC OXIDE SURFACE OF THE FLEXIBLE DISKETTE.

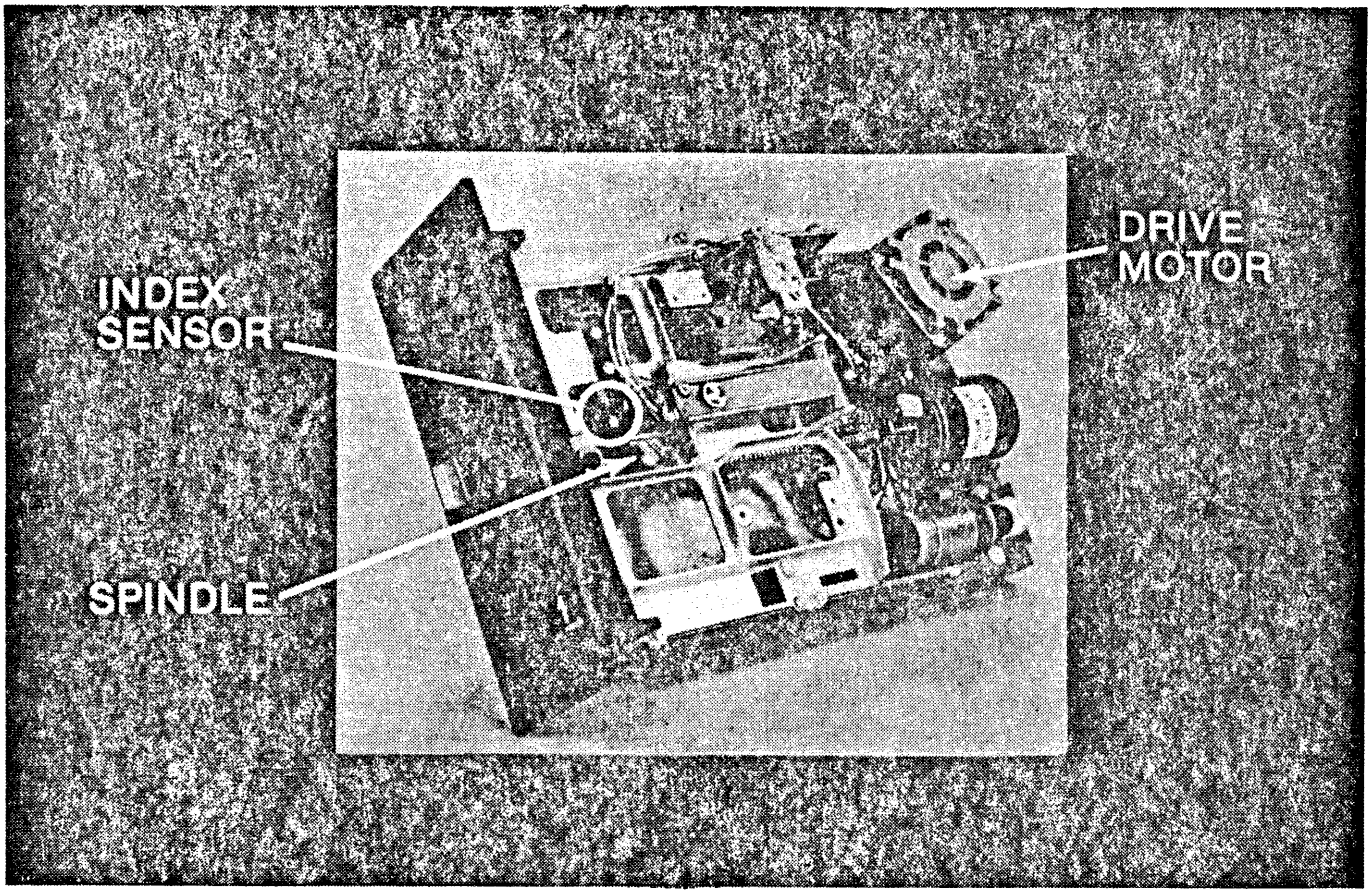
3



THE READ/WRITE HEAD IS MOUNTED ON THE CARRIAGE ASSEMBLY WHICH IS MOVED BETWEEN TRACKS BY THE STEPPER MOTOR THROUGH THE SCREW SHAFT. CARRIAGE MOVEMENT ON THE SHAFT IS LIMITED BY THE INNER STOP AND THE OUTER STOP. EACH STEP OF THE STEPPER MOTOR ROTATES THE SCREW SHAFT THROUGH 15 DEGREES WHICH MOVES THE HEAD BY ONE TRACK.

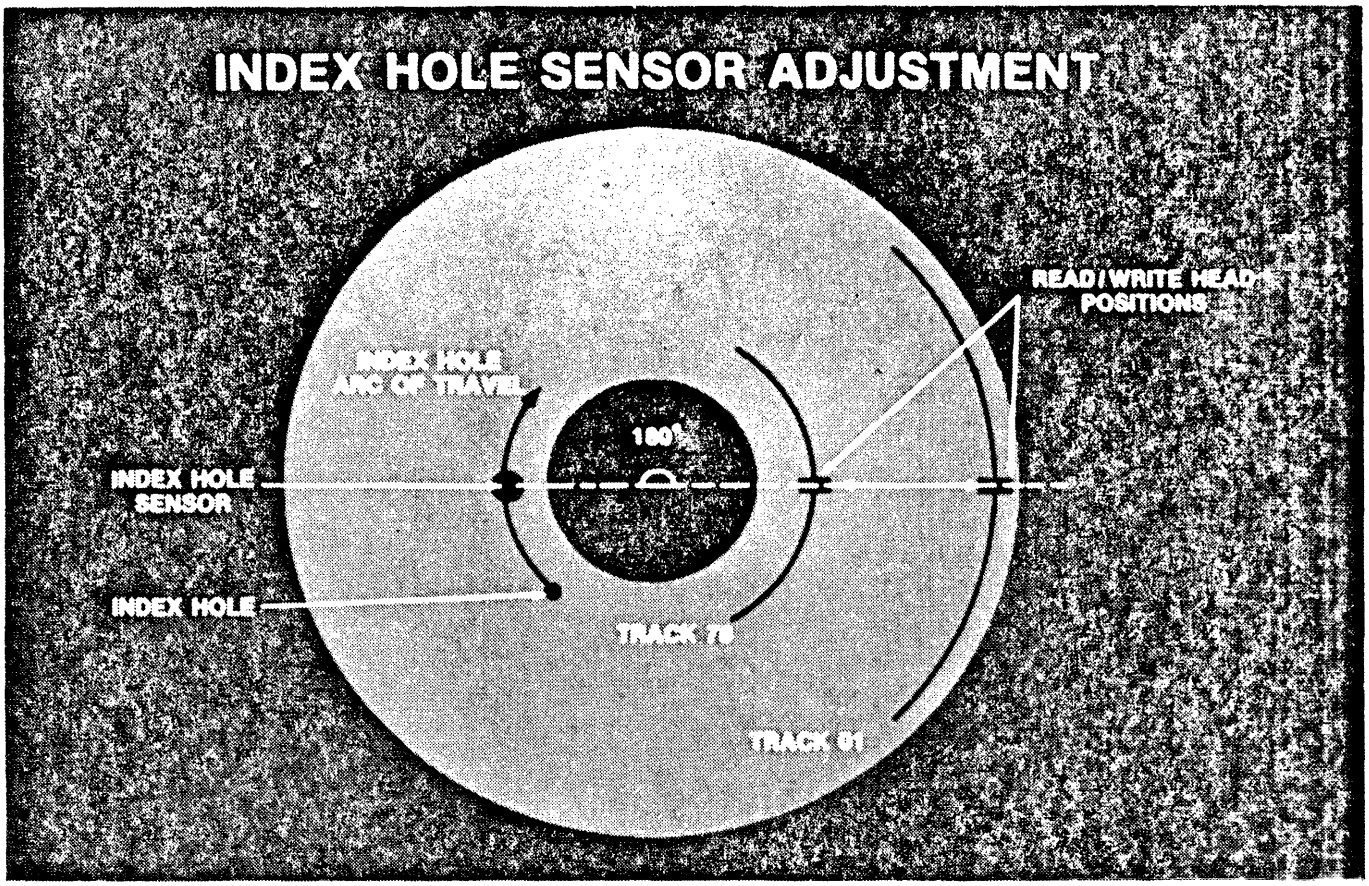
THE TRACK 00 SENSOR IS AN OPTICAL SENSOR WHICH DETERMINES WHETHER THE READ/WRITE HEAD IS POSITIONED TO TRACK 00.

4



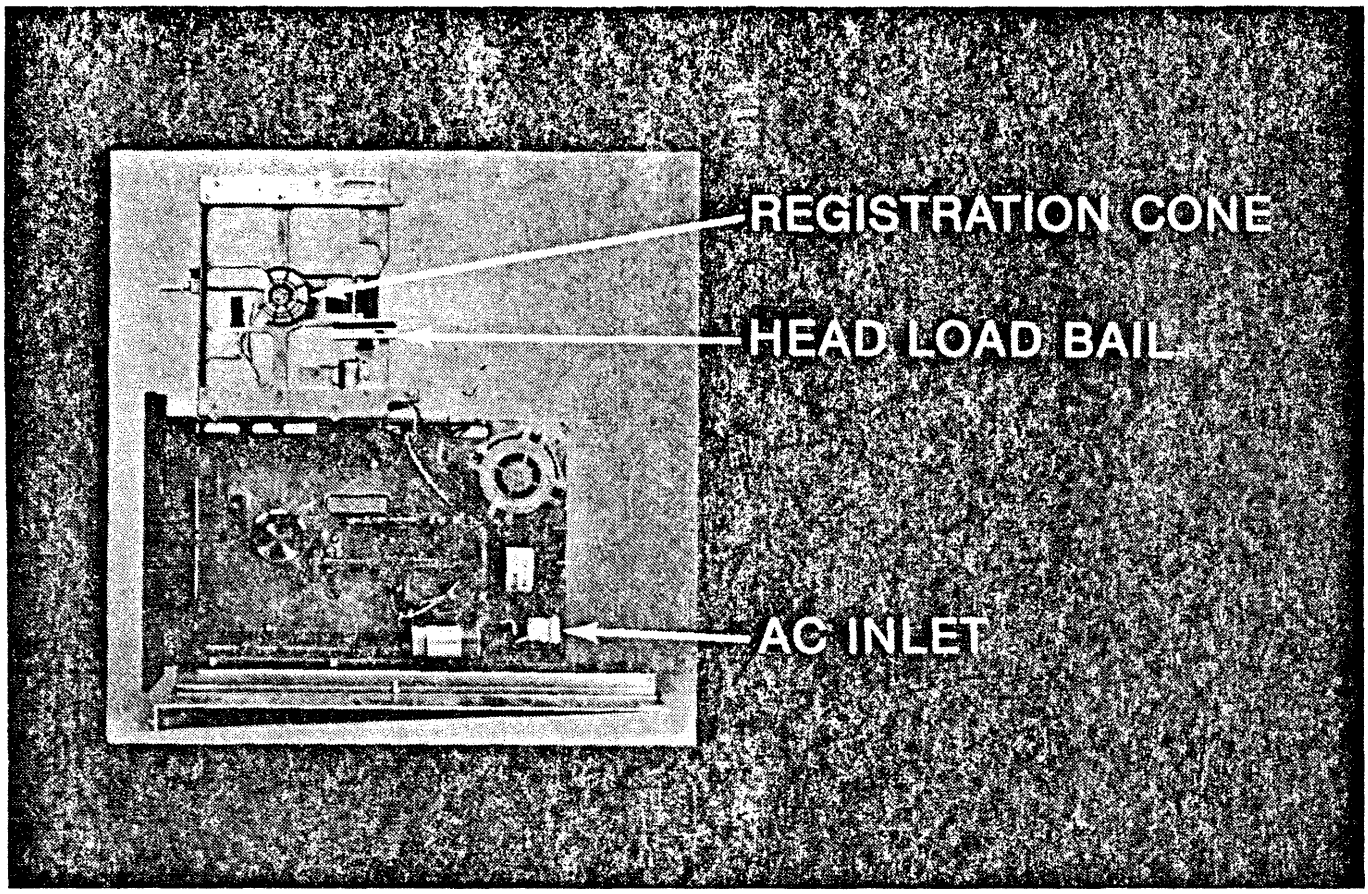
THE DISK DRIVE MOTOR IS CONNECTED TO THE SPINDLE BY A BELT AND PULLEY WHICH ARE GEARED TO ROTATE THE SPINDLE AT 360 RPM. THE OPTICAL INDEX SENSOR SENSES THE INDEX HOLE IN THE DISK TO PROVIDE THE TIMING REFERENCE SIGNAL "INDEX".

5



REMEMBER THAT THE INDEX HOLE DETERMINES THE POINT IN THE CIRCUMFERENCE OF THE DISKETTE THAT EACH TRACK STARTS. NOTICE THAT BECAUSE THE OPTICAL INDEX SENSOR IS ON THE OPPOSITE SIDE OF THE SPINDLE TO THE READ/WRITE HEAD, THE INDEX HOLE IS PHYSICALLY 180 DEGREES AROUND THE SURFACE OF THE DISKETTE FROM THE START OF EACH TRACK. THIS IS ALSO THE POINT DURING THE ROTATION OF THE DISKETTE AT WHICH THE READ/WRITE HEAD IS LOADED.

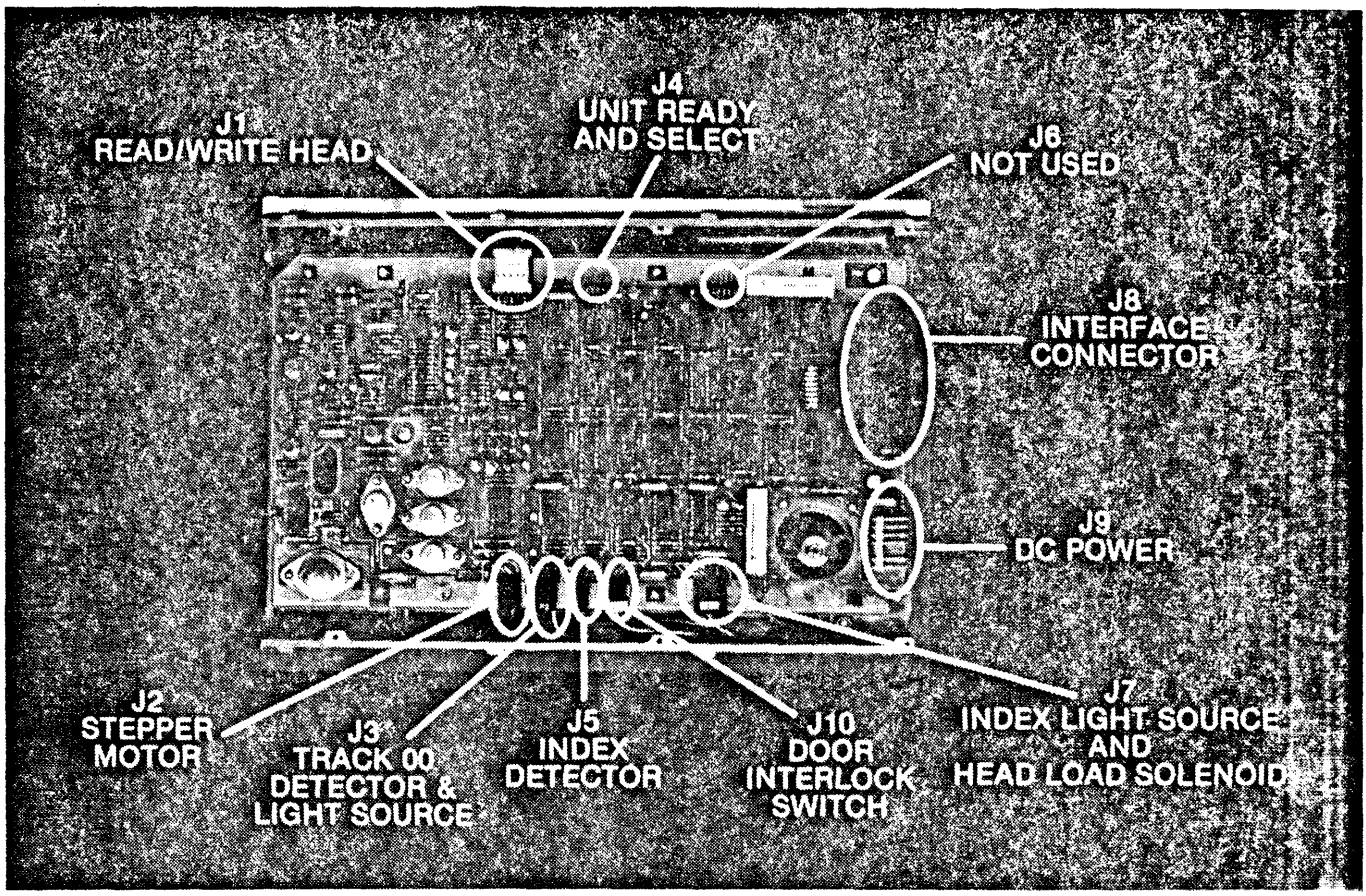
6



THE AC POWER INLET IS SHOWN TO THE BOTTOM RIGHT. THIS INLET CONNECTS AN EXTERNAL 120V AC SUPPLY TO THE DISK DRIVE MOTOR.

THE DISK LOAD ARM CASTING IS DISASSEMBLED FROM THE UNIT IN THIS ILLUSTRATION TO SHOW THE REGISTRATION CONE WHICH CENTERS AND CLAMPS THE DISKETTE TO THE SPINDLE. ALSO VISIBLE IS THE HEAD LOAD BAIL WHICH HELPS TO KEEP THE DISK FLAT AS WELL AS ENGAGING AND DISENGAGING THE HEAD LOAD PAD.

7



A VIEW OF THE OTHER SIDE OF THE UNIT SHOWS THE LOGIC PRINTED CIRCUIT BOARD. THE LOGIC BOARD MAY BE INTERFACED DIRECTLY TO THE HOST SYSTEM, THROUGH THE OPTIONAL LINE DRIVER/RECEIVER OR THROUGH THE OPTIONAL ADAPTOR CARD.

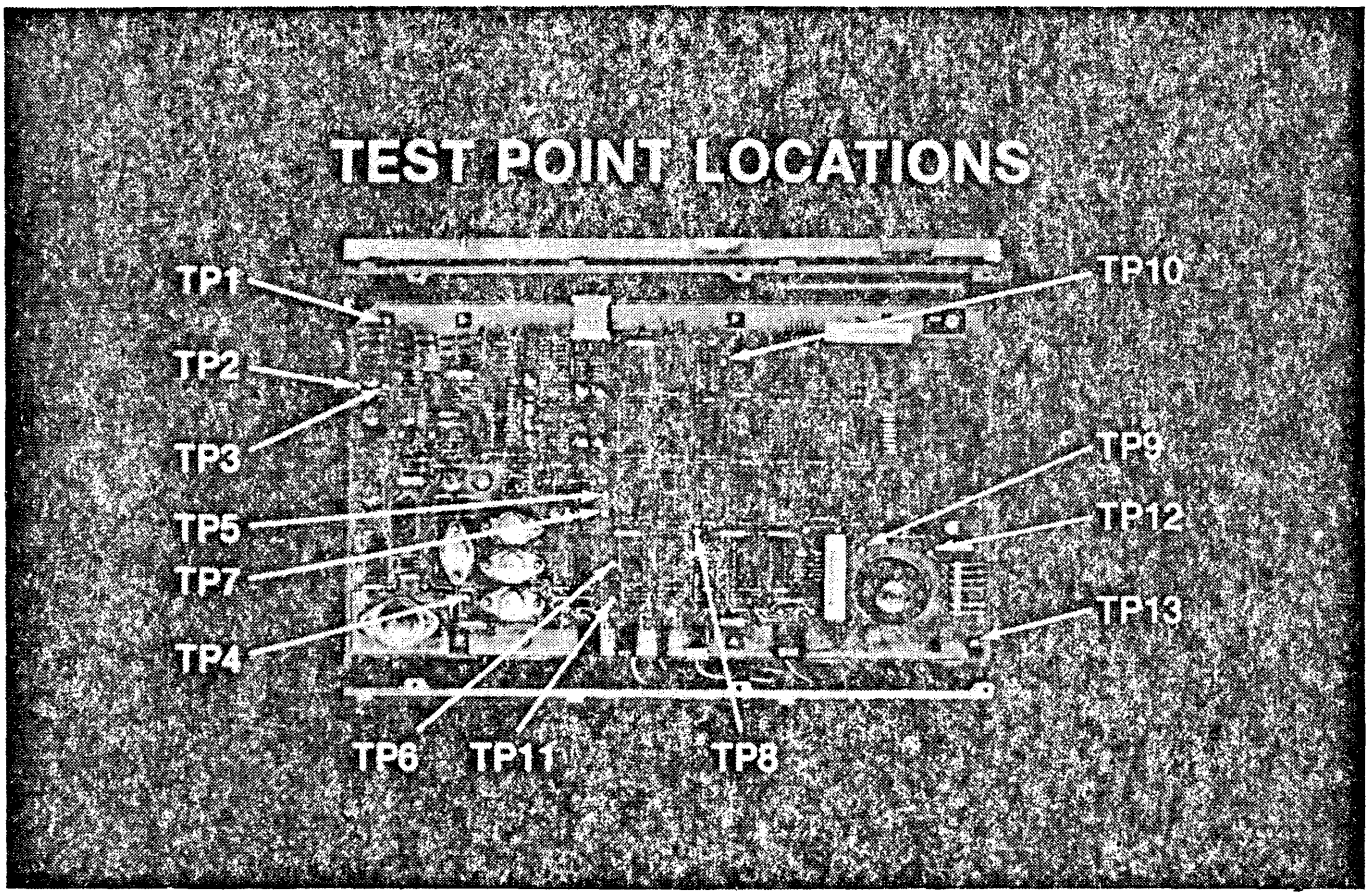
THE INTERFACE IS VIA A 50 WAY CONNECTOR, J8. THE CONNECTOR BELOW J8, J9 CONNECTS THE UNIT TO THE HOST SYSTEM OR OPTIONAL INTERNAL UNIT DC POWER SUPPLY.

MOVING CLOCKWISE AROUND THE PCB, J7 CONNECTS TO THE DIODE LIGHT SOURCE FOR THE OPTICAL INDEX HOLE DETECTOR AND THE HEAD LOAD SOLENOID. J10 CONNECTS WITH THE DOOR INTERLOCK SWITCH. J5 CONNECTS THE OPTICAL INDEX

HOLE DETECTOR TO THE LOGIC. J3 CONNECTS THE OPTICAL TRACK 00 DIODE LIGHT SOURCE AND DETECTOR TO THE LOGIC.

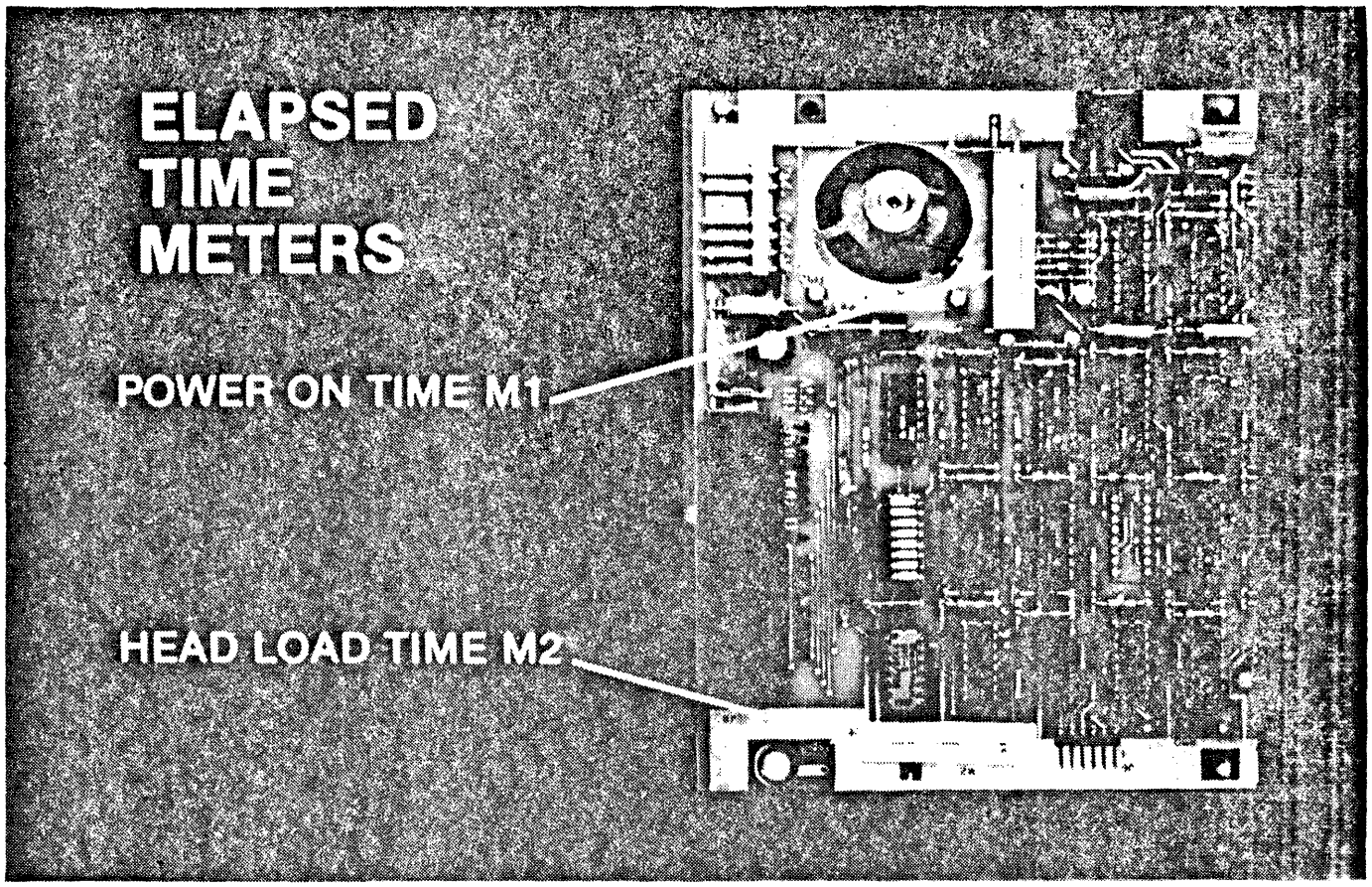
J2 CONNECTS THE STEPPER MOTOR TO THE STEPPER MOTOR DRIVER CIRCUITRY ON THE LOGIC PCB. J1 IS CONNECTED TO THE READ/WRITE HEAD. THE OPTIONAL UNIT READY AND SELECT INDICATORS CONNECT TO J4. J6 IS NOT USED.

8



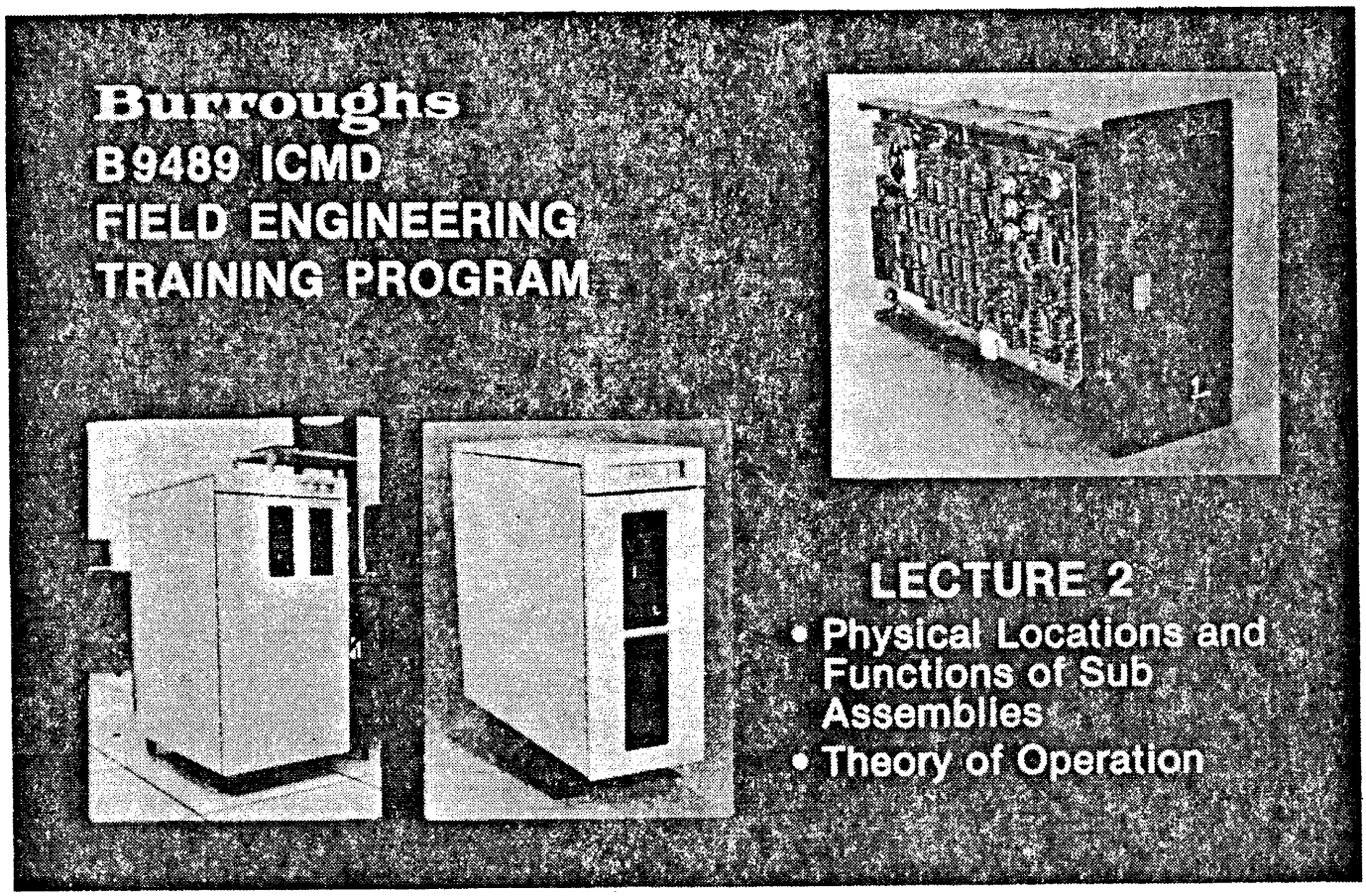
THIRTEEN TEST POINTS ARE PROVIDED ON THE PCB FOR TEST AND MAINTENANCE PURPOSES. LIKE MOST OTHER COMPONENTS, THEIR REFERENCE IDENTIFICATION IS PRINTED BESIDE THEM ON THE PCB. A DIAGRAM SHOWING THE LOCATION OF EACH OF THESE TEST POINTS CAN BE FOUND IN THE TECHNICAL MANUAL.

9



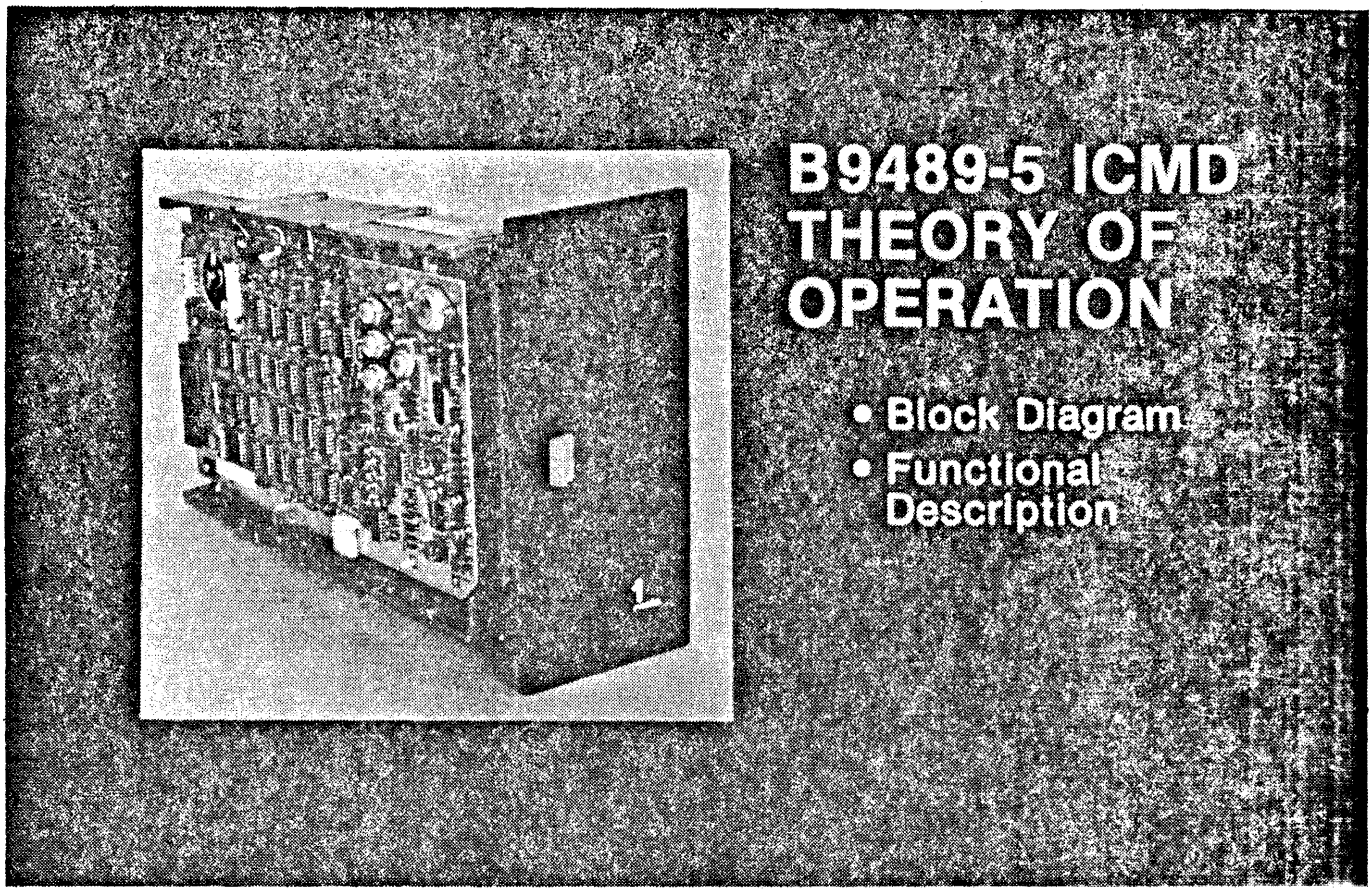
THE UNIT IS EQUIPPED WITH TWO ELAPSED TIME METERS. THE ELAPSED TIME METERS ARE OF THE MERCURY MIGRATION TYPE. M1, RECORDS THE TOTAL POWER ON HOURS FOR THE UNIT. M2, RECORDS THE NUMBER OF HOURS THE READ/WRITE HEAD HAS BEEN LOADED. THIS INFORMATION IS USED TO DETERMINE PREVENTATIVE MAINTENANCE REQUIREMENTS WHICH ARE DESCRIBED LATER.

10



STOP AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

11



A CLEAR COMPREHENSION OF THE FUNCTION AND OPERATION OF EACH CIRCUIT IN THE RELATIVELY SIMPLE LOGIC OF THE B 9489-5 UNIT WILL BE OF CONSIDERABLE ASSISTANCE WHEN USING THE MTR GUIDED PROCEDURES LATER AND SHOULD ENABLE YOU TO REDUCE THE NUMBER OF SUSPECTS FOR ANY GIVEN FAULT DIAGNOSIS.

THIS SECTION OF THE LECTURE DETAILS THE THEORY OF OPERATION OF THE B 9489 UNIT. THE FIRST PART INTRODUCES A BLOCK DIAGRAM OF THE LOGIC TO GIVE AN OVERALL DESCRIPTION OF THE UNIT BEFORE A MORE DETAILED FUNCTIONAL DESCRIPTION OF EACH SECTION.

12

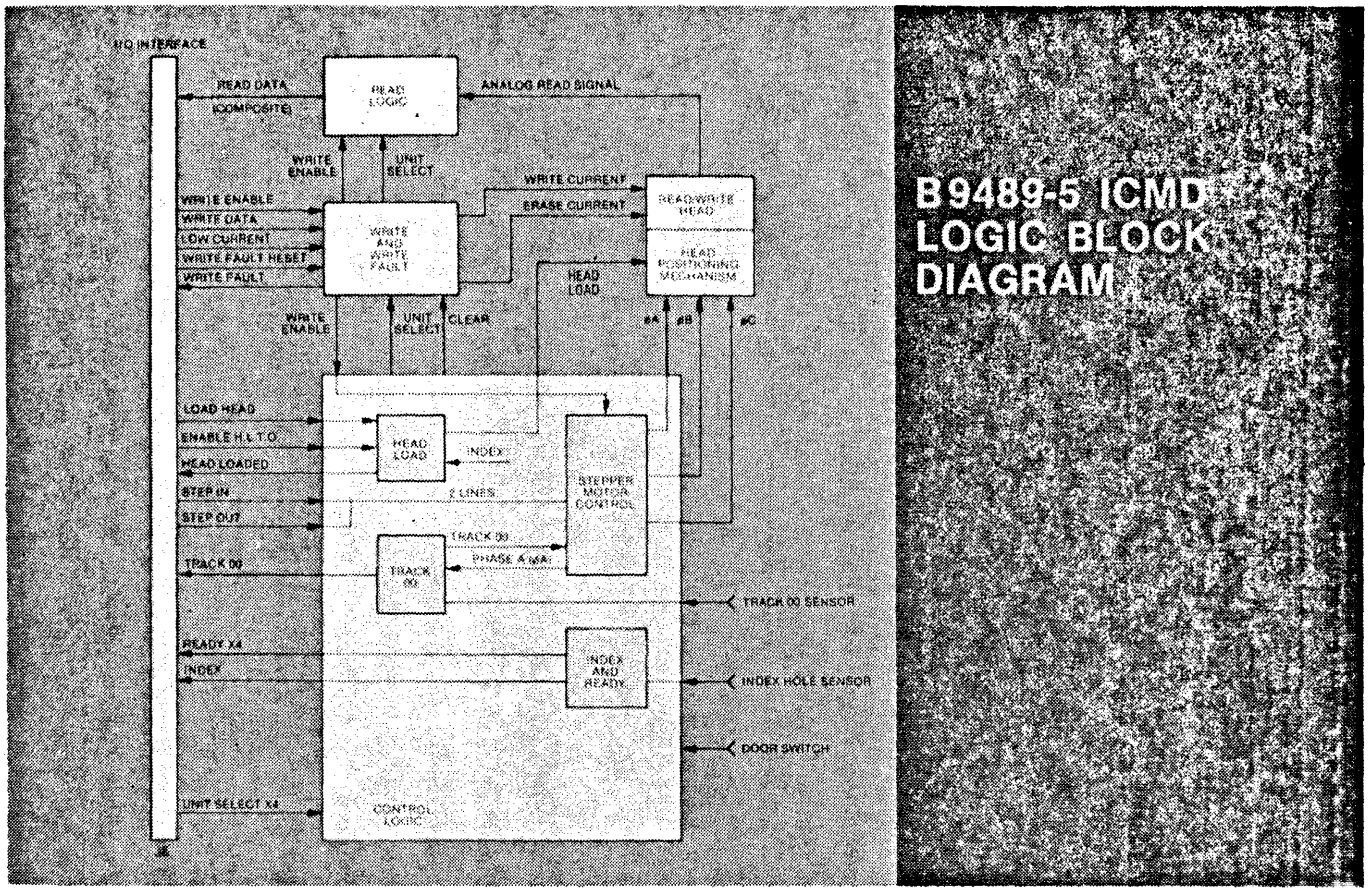
YOU ALREADY HAVE A GOOD APPRECIATION OF THE BASIC OPERATING FUNCTIONS AND CAPABILITIES OF THE B 9489-5 UNIT.

THE FUNCTIONS OF THE UNIT CAN BE SUMMARIZED INTO FOUR BASIC AREAS:

- FIRST, TO RECEIVE COMMAND SIGNALS FROM THE CONTROLLER AND RESPOND TO THE COMMANDS.
- SECOND, TO GENERATE CONTROL SIGNALS FOR USE BY BOTH THE DRIVE AND THE CONTROLLER TO DETERMINE THE STATUS OF THE DRIVE.
- THIRD, TO POSITION THE READ/WRITE HEAD TO THE SELECTED TRACK.
- AND FOURTH, TO READ OR WRITE DATA IN SERIAL BIT FORM FROM OR TO THE CONTROLLER.

ALL OPERATIONS OF THE UNIT ARE DEPENDENT UPON COMMANDS RECEIVED FROM THE CONTROLLER.

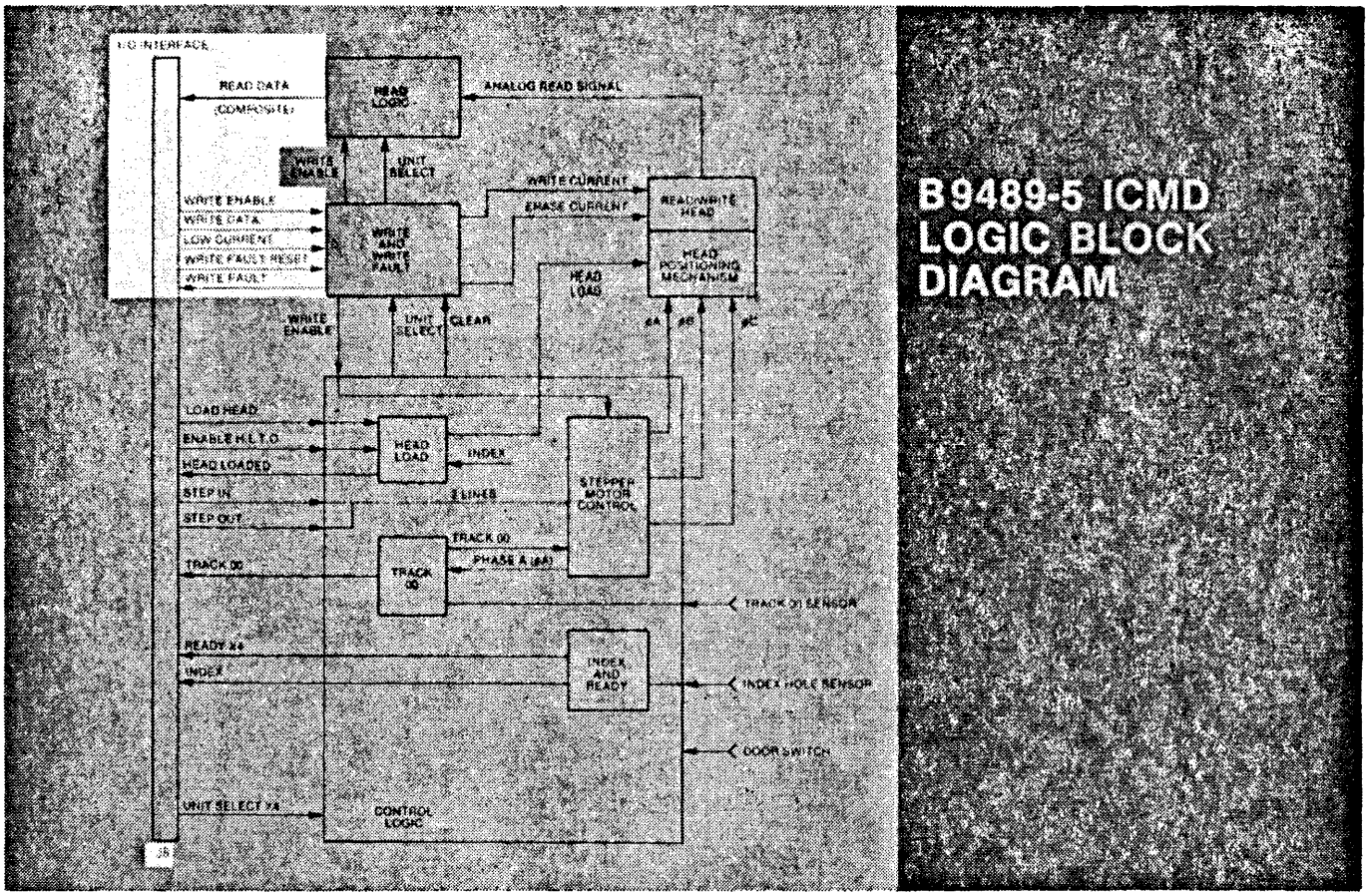
13



B9489-5 ICMD LOGIC BLOCK DIAGRAM

THIS DIAGRAM REPRESENTS THE COMPLETE LOGIC OF THE UNIT, DIVIDED INTO FIVE MAIN SECTIONS; THE I/O INTERFACE, THE READ LOGIC, THE WRITE AND WRITE FAULT LOGIC, THE HEAD POSITIONING MECHANISM WITH THE READ/WRITE HEAD ITSELF AND FINALLY THE CONTROL LOGIC, INCLUDING THE HEAD LOAD, TRACK 00, STEPPER MOTOR CONTROL AND INDEX AND READY LOGIC.

14



THE SIGNAL INTERFACE WITH THE HOST SYSTEM CONTROLLER OR POSSIBLY THE OPTIONAL ADAPTOR FOR MEDIUM AND LARGE SYSTEMS, IS VIA THE 50 WAY CONNECTOR, J8.

EXPLAINING EACH SIGNAL IN TURN, READ DATA IS THE DIGITAL SIGNAL FROM THE UNIT, CONSISTING OF THE COMPOSITE CLOCK AND DATA BITS READ FROM THE DISKETTE.

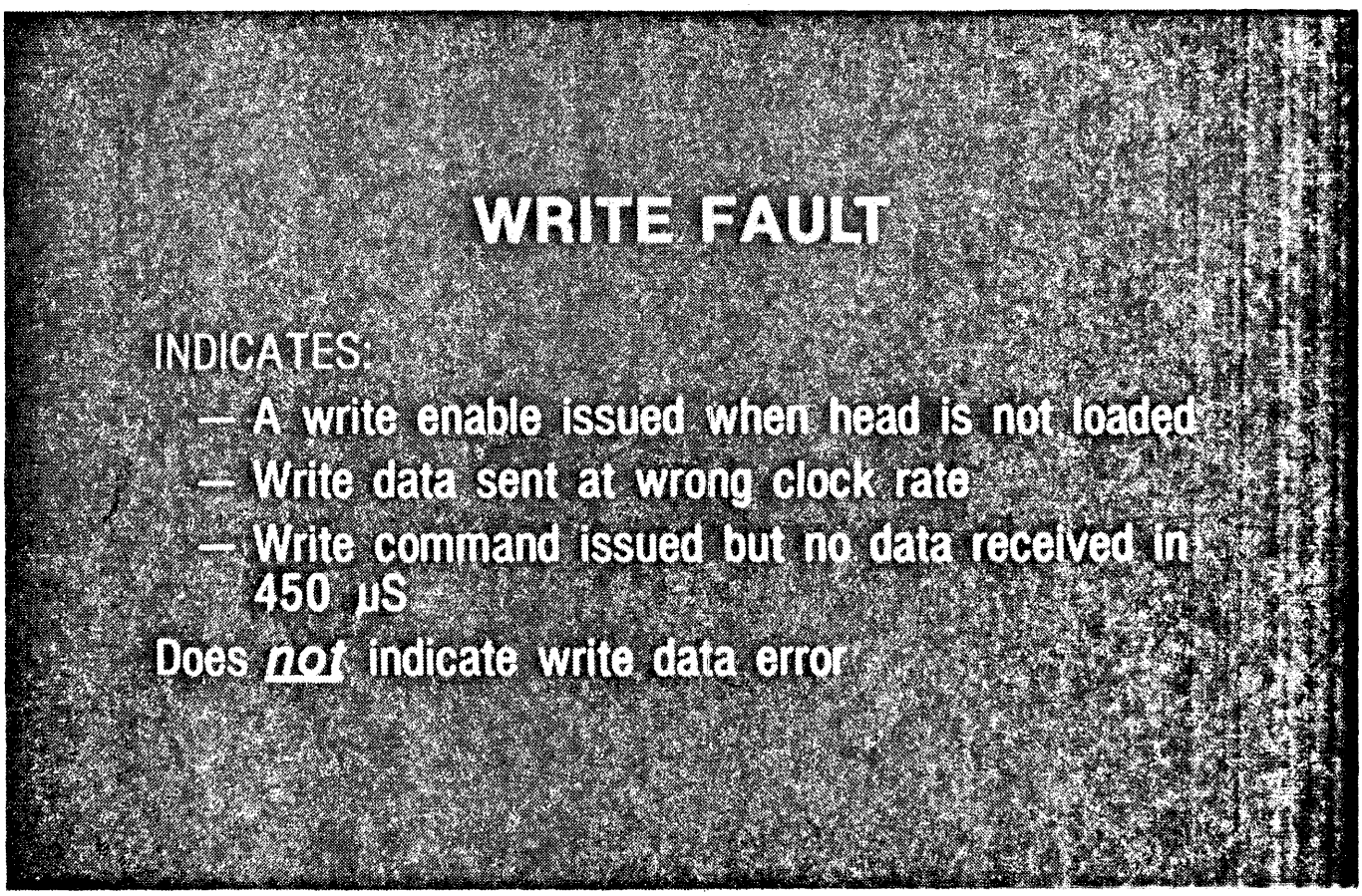
WRITE ENABLE, AS THE NAME IMPLIES, ENABLES THE WRITE LOGIC AND DISABLES THE READ LOGIC WHEN THE SIGNAL IS AT A LOGIC 1 LEVEL.

WRITE DATA RECEIVES THE COMPOSITE CLOCK AND DATA FROM THE CONTROLLER WHICH ARE TO BE WRITTEN TO THE DISKETTE.

LOW CURRENT IS A SIGNAL FROM THE CONTROLLER WHICH REDUCES THE CURRENT TO THE WRITE HEAD WHEN THE WRITE IS TAKING PLACE ON A TRACK ABOVE TRACK 43. THE LOWER WRITE CURRENT IS REQUIRED ABOVE TRACK 43 BECAUSE OF THE EFFECTS OF THE INCREASED PACKING DENSITY ON THE TRACKS TOWARDS THE CENTER OF THE DISKETTE.

THE WRITE FAULT SIGNAL INDICATES A WRITE FAULT CONDITION TO THE CONTROLLER.

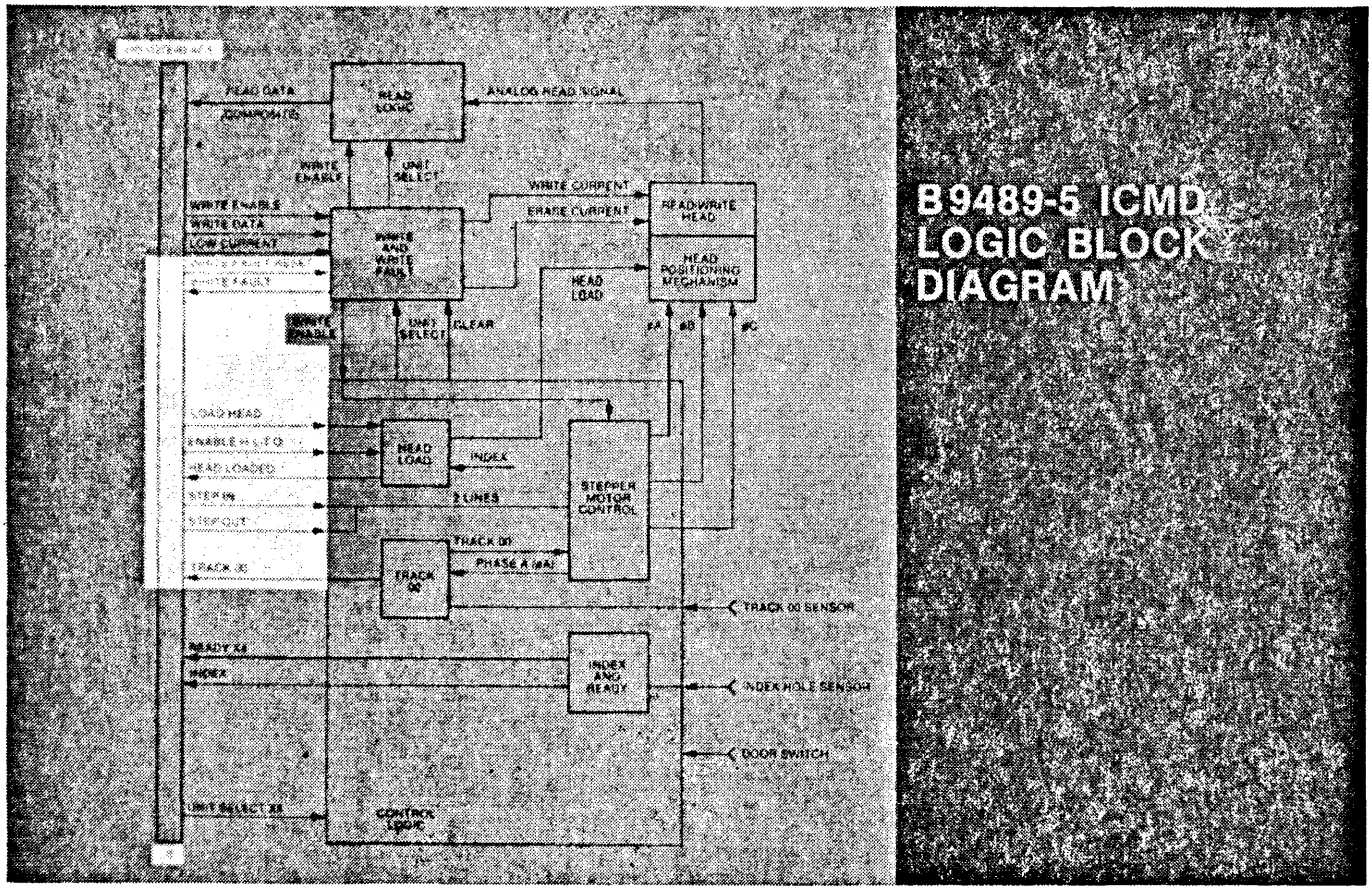
15



A WRITE FAULT INDICATES ONE OR MORE OF THESE CONDITIONS; A WRITE ENABLE IS ISSUED WHEN THE HEAD IS NOT LOADED, WRITE DATA ARE SENT AT THE WRONG CLOCK RATE OR A WRITE IS ISSUED AND DATA ARE NOT RECEIVED WITHIN A 450 MICROSECOND TIME PERIOD.

BECAUSE THE READ/WRITE HEAD IS A SINGLE GAP HEAD, THE DATA WRITTEN TO THE DISKETTE CANNOT BE CHECKED DURING A WRITE OPERATION. DATA CAN ONLY BE CHECKED BY THE HOST SYSTEM PERFORMING A READ IMMEDIATELY AFTER THE WRITE AND COMPARING DATA.

16



THE SIGNAL WRITE FAULT RESET CLEARS THE WRITE FAULT LATCH IN THE WRITE FAULT LOGIC.

LOAD HEAD IS A COMMAND FROM THE CONTROLLER WHICH CAUSES THE HEAD LOAD SOLENOID TO ENERGIZE. LOAD HEAD IS A LOGIC 1 LEVEL WHICH MUST BE INITIATED 60 MILLISECONDS BEFORE INITIATING A READ OR WRITE OPERATION TO ALLOW FOR HEAD LOAD SETTLING TIME. TO ENSURE INCREASED HEAD AND

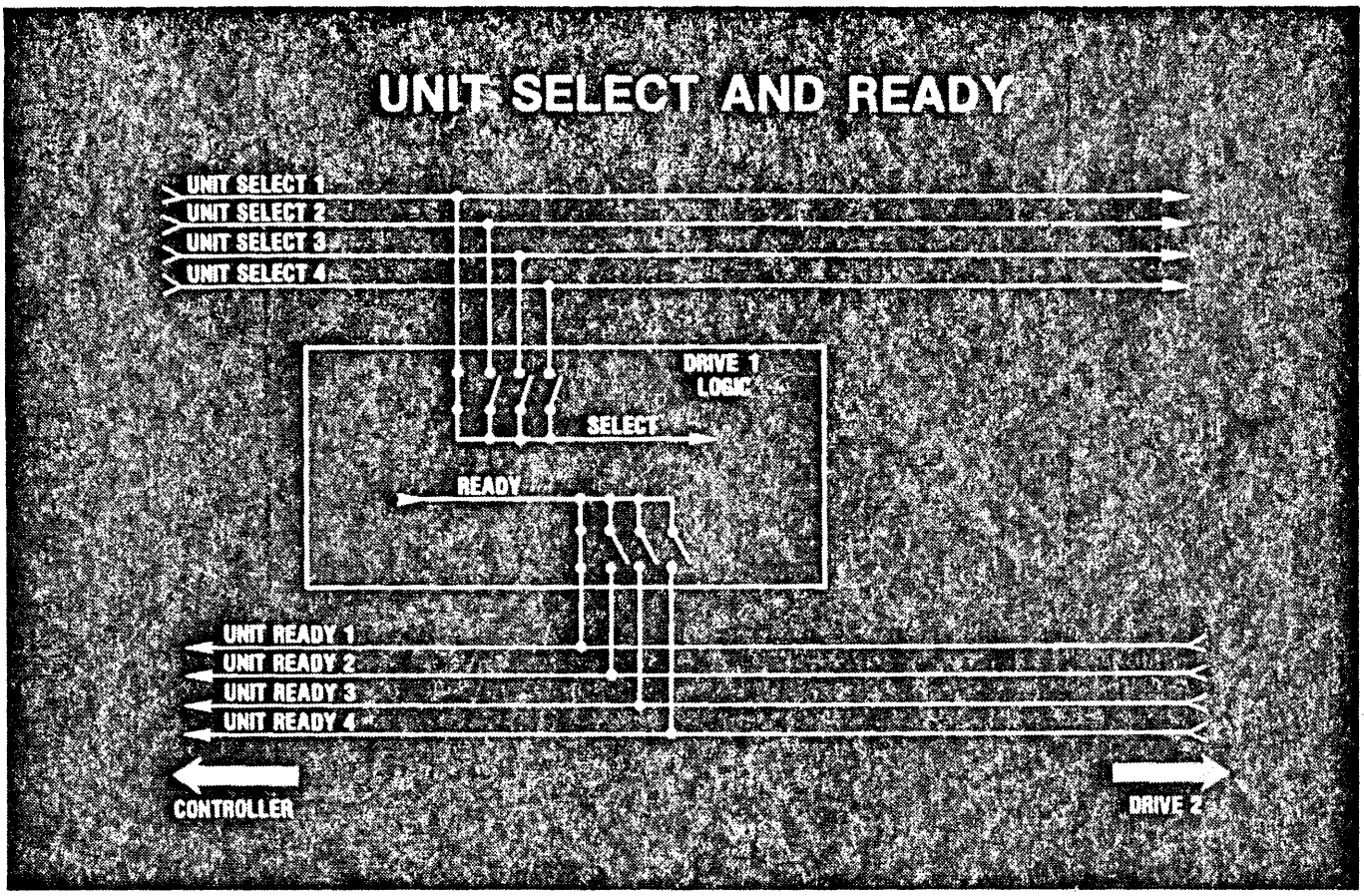
DISKETTE LIFE THIS SIGNAL SHOULD BE AT A LOGIC ZERO WHENEVER A DATA TRANSFER OPERATION IS NOT IN PROCESS OR PENDING.

ENABLE HEAD LOAD TIME OUT, (HLTO), IS USED ON UNITS WITH THE HEAD LOAD TIME-OUT OPTION. THIS OPTION USES A TIME-OUT COUNTER WITHIN THE DRIVE TO KEEP THE READ/WRITE HEAD LOADED FOR EIGHT INDEX PULSES AFTER THE DRIVE IS DESELECTED.

THE SIGNALS "STEP IN" AND "STEP OUT" CAUSE THE READ/WRITE HEAD TO STEP IN OR OUT BY ONE TRACK.

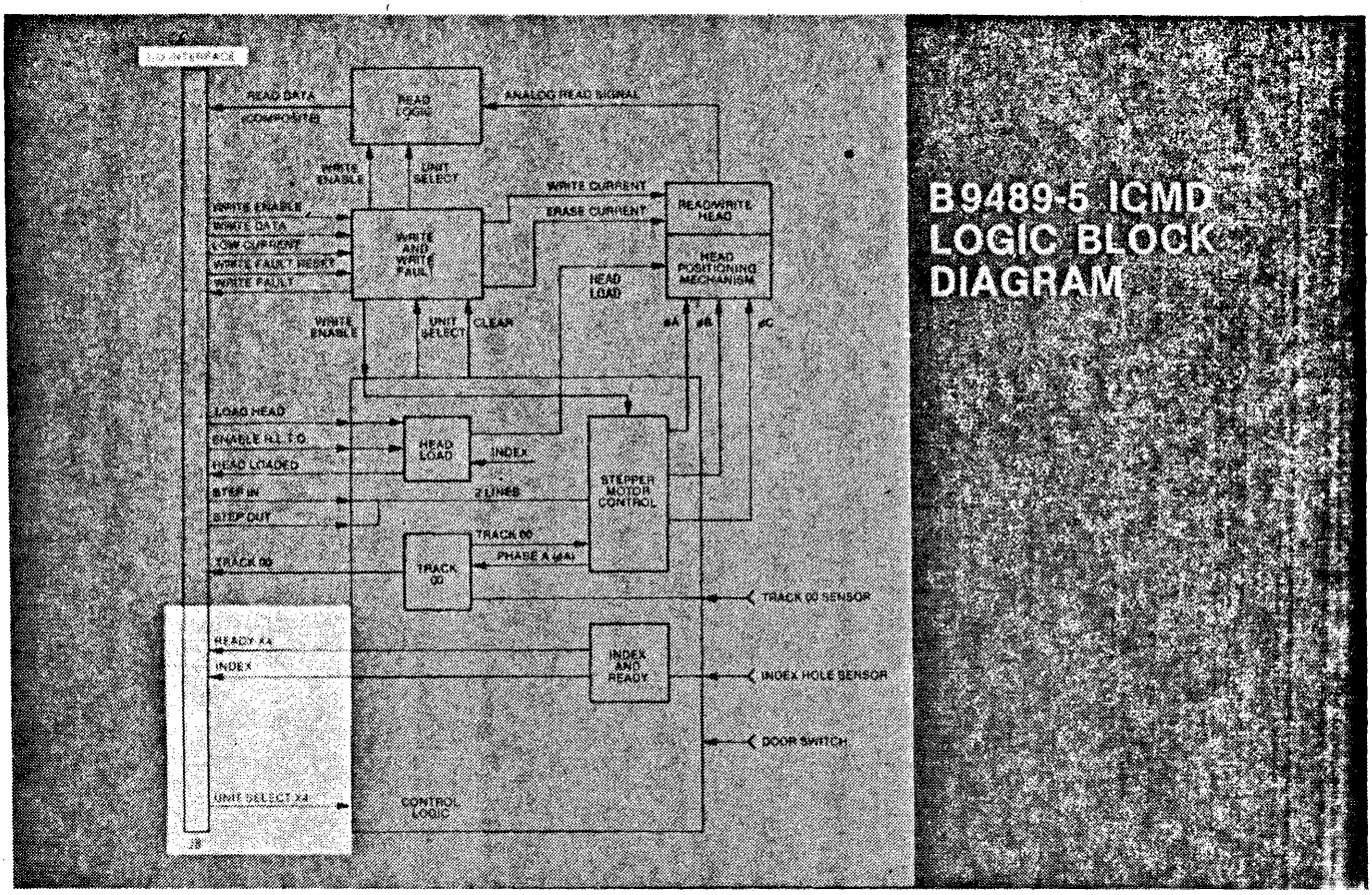
TRACK 00 IS AN OUTPUT SIGNAL TO THE CONTROLLER TO INDICATE THAT THE READ/WRITE HEAD CARRIAGE ASSEMBLY IS POSITIONED OVER TRACK 00.

17



THE B 9489-5 UNIT IS DESIGNED SO THAT A MAXIMUM OF FOUR UNITS COULD BE CONNECTED TO A SINGLE CONTROLLER. ALTHOUGH PRESENTLY A MAXIMUM OF TWO DRIVES ARE USED, THE UNIT INTERFACES TO FOUR SELECT SIGNALS AND FOUR READY SIGNALS. EACH UNIT IS ASSIGNED A CORRESPONDING DRIVE NUMBER BETWEEN ONE AND FOUR. ONCE THIS NUMBER IS ASSIGNED, THE CONTROL LOGIC IS CONNECTED TO THE ASSIGNED UNIT "SELECT" AND "READY" SIGNALS USING SWITCHES MOUNTED IN A DUAL IN LINE PACKAGE ON THE LOGIC PCB.

18

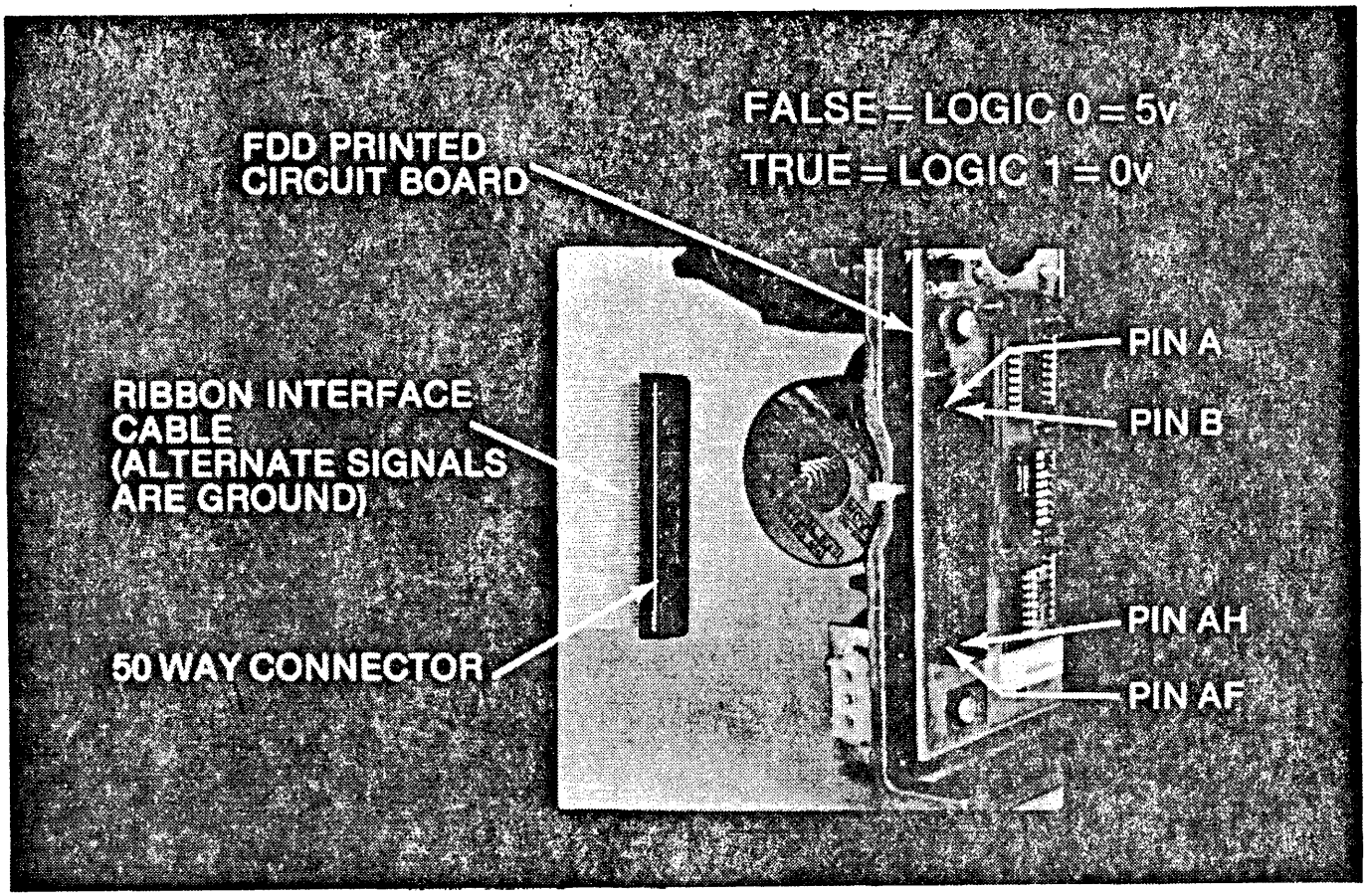


THE UNIT SELECT SIGNAL ENABLES ALL CONTROL AND STATUS COMMUNICATION, EXCEPT READ STATUS BETWEEN DRIVE 1 AND THE HOST SYSTEM CONTROLLER. A LOGIC 1 ON THE ASSIGNED SELECT LINE SELECTS THE DRIVE, A LOGIC 0 DECOUPLES THE DRIVE FROM THE CONTROLLER.

THE UNIT READY SIGNAL INDICATES THAT THE DISKETTE IS CORRECTLY INSERTED, THE DOOR IS CLOSED AND THE DISKETTE IS UP-TO-SPEED.

THE INDEX SIGNAL, AS PREVIOUSLY MENTIONED IS A TIMING SIGNAL TO THE HOST SYSTEM CONTROLLER INDICATING THE RELATIVE POSITION OF THE DISKETTE FROM THE OPTICAL SENSOR ONCE PER DISKETTE REVOLUTION.

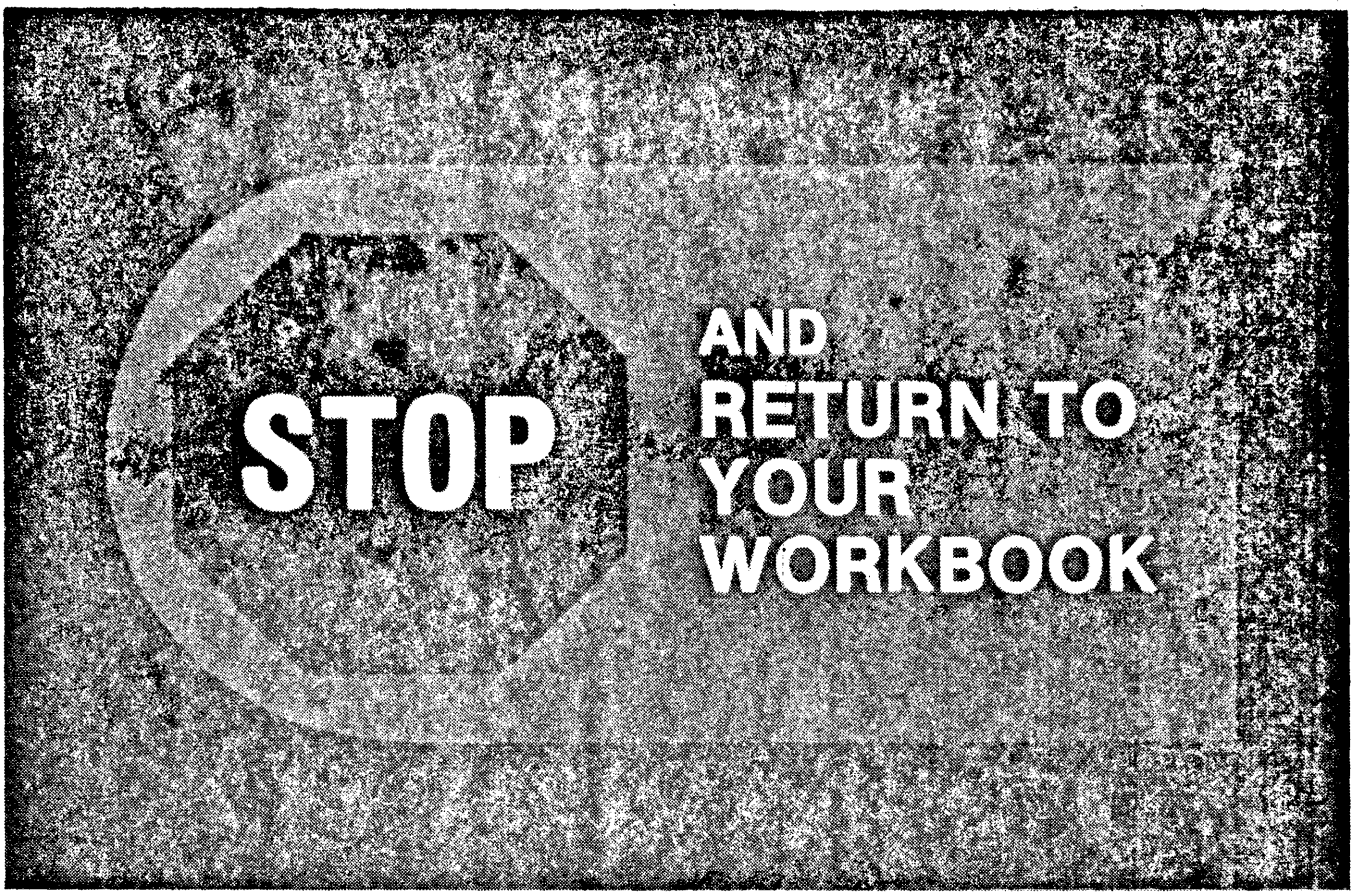
19



THE REMAINING SIGNALS IN THE FIFTY WAY INTERFACE ARE GROUND SIGNALS WHICH ARE USED IN THE FLAT INTERFACE CABLE TO PROVIDE ISOLATION BETWEEN ACTIVE SIGNAL PATHS.

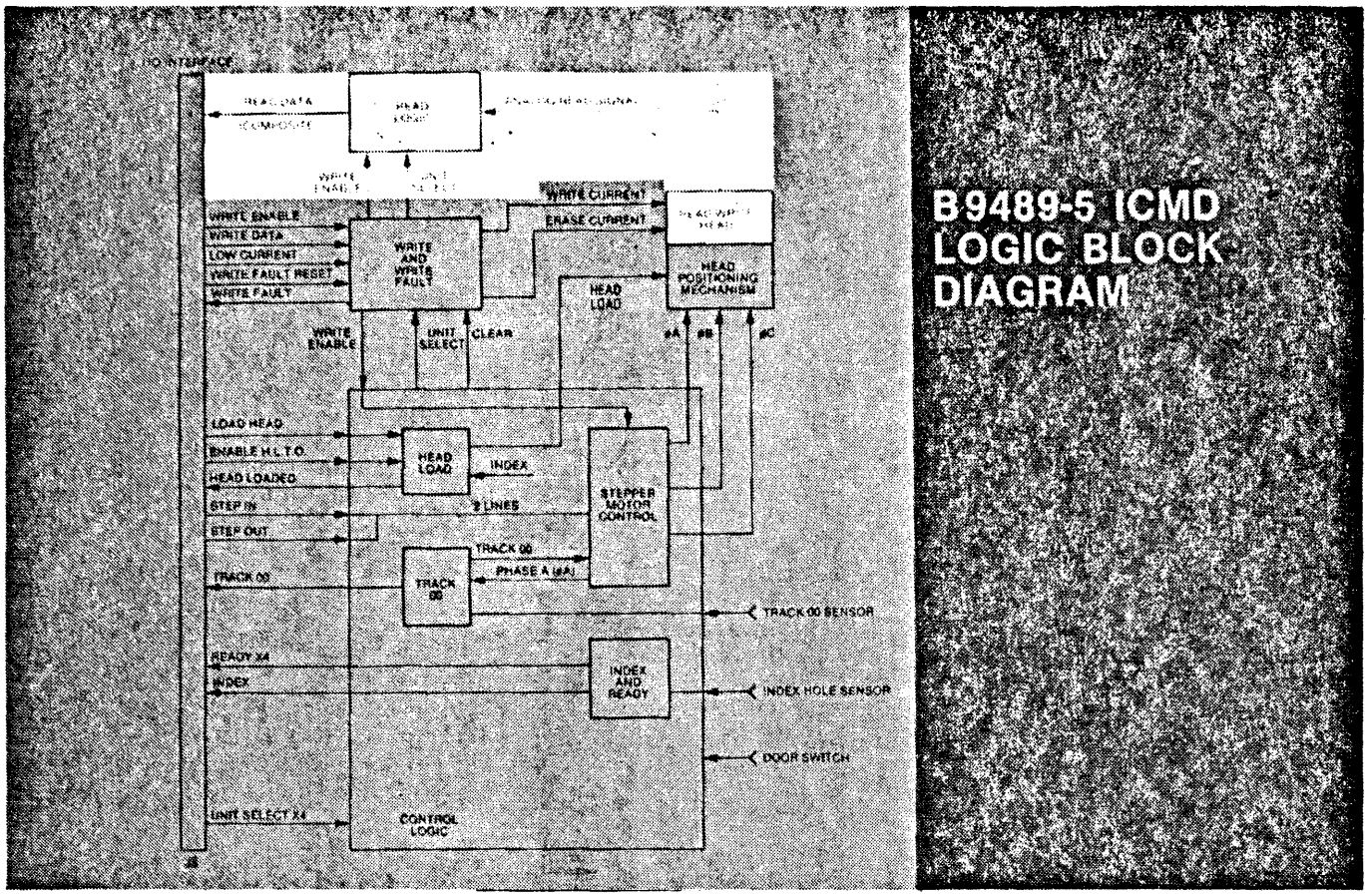
THE CONVENTION USED ON THE INTERFACE FOR THE UNIT IS THAT A FALSE OR LOGIC 0 IS REPRESENTED BY A 5V SIGNAL LEVEL. A TRUE OR LOGIC 1 IS REPRESENTED BY A 0V SIGNAL LEVEL.

20



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK, COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

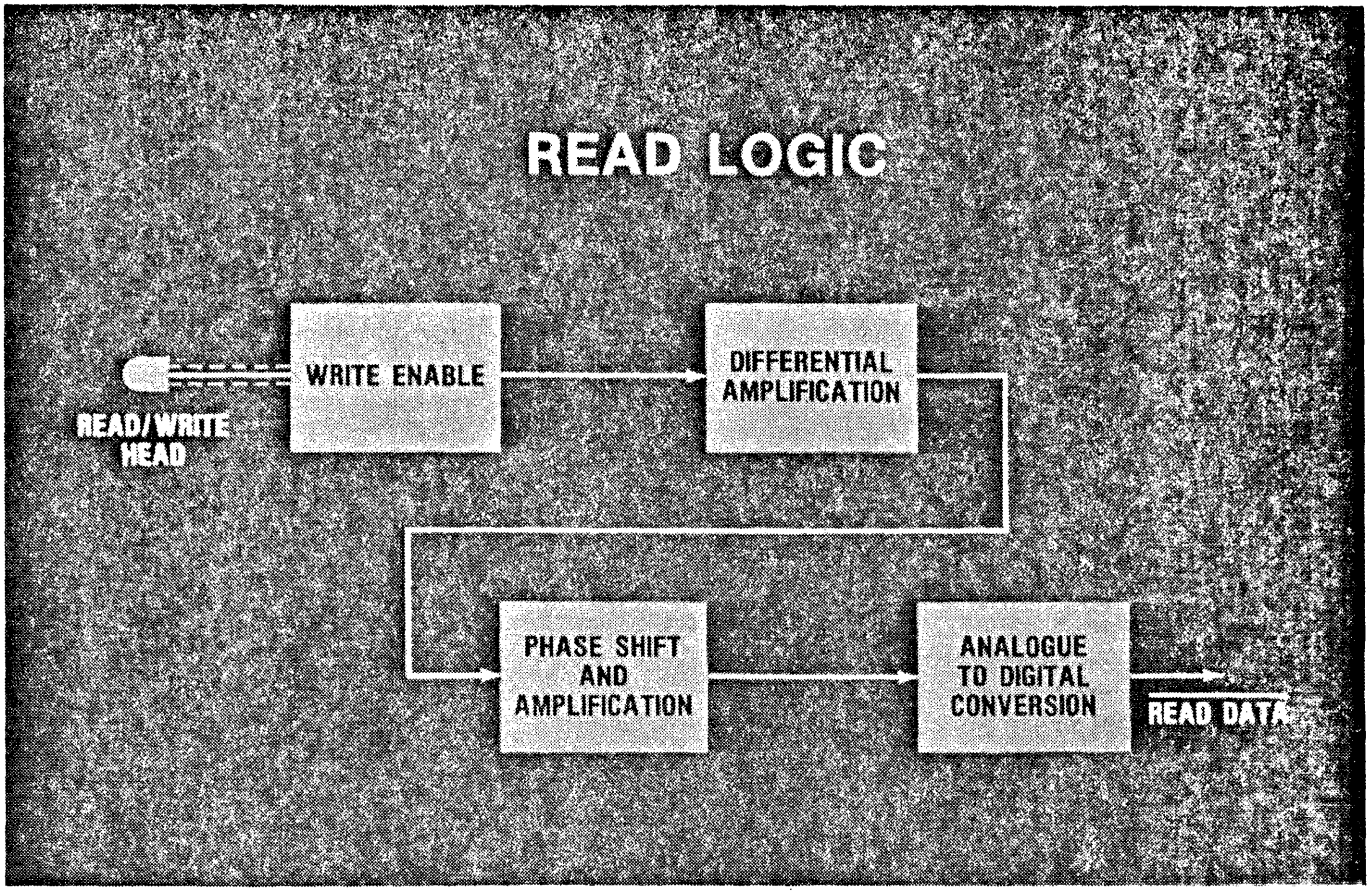
21



B9489-5 ICMD LOGIC BLOCK DIAGRAM

THE NEXT FUNCTIONAL BLOCK IN THE ICMD UNIT TO BE EXAMINED IS THE READ LOGIC. THE READ LOGIC TAKES THE ANALOGUE OUTPUT SIGNAL FROM THE READ HEAD AND CONVERTS IT INTO THE DIGITAL SIGNAL REQUIRED BY THE HOST SYSTEM CONTROLLER.

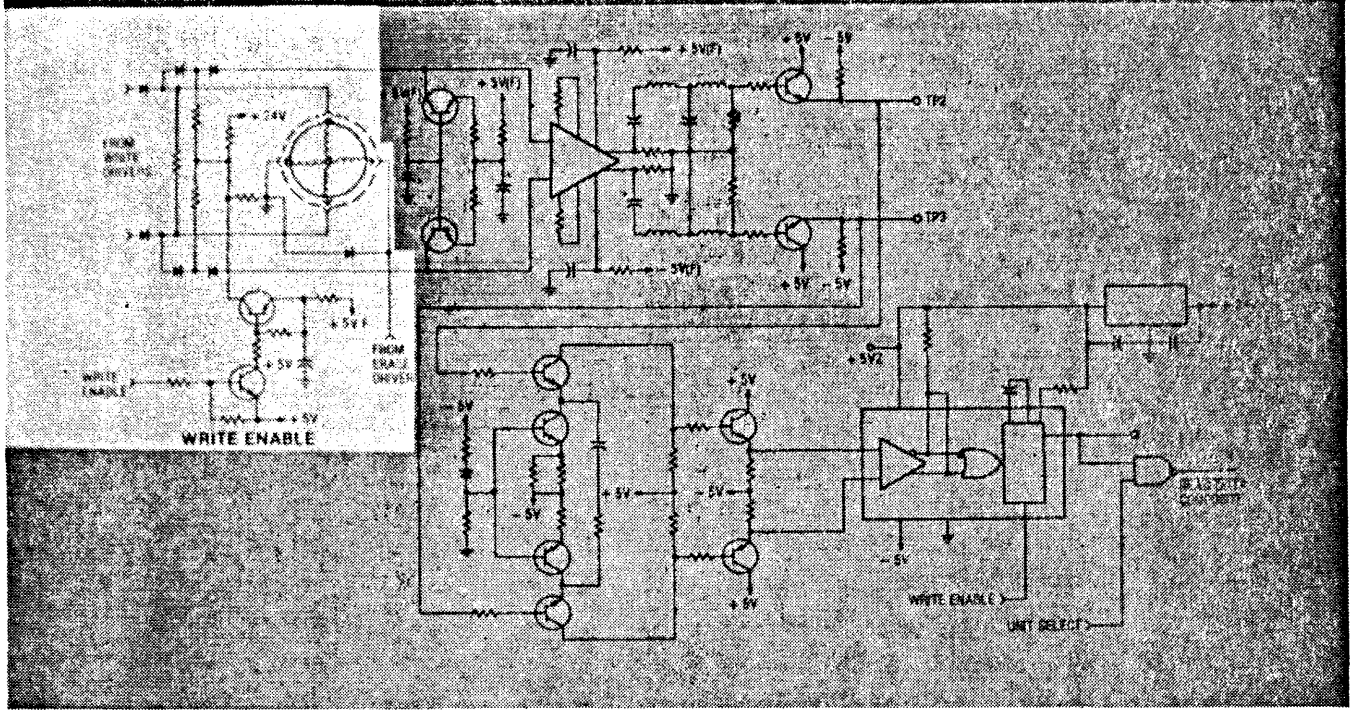
22



THE READ LOGIC CONSISTS OF FOUR MAIN FUNCTIONAL BLOCKS, WRITE ENABLE; DIFFERENTIAL AMPLIFICATION; PHASE SHIFT AND AMPLIFICATION; AND ANALOGUE TO DIGITAL CONVERSION. WE WILL HIGHLIGHT AND DESCRIBE EACH OF THESE FOUR FUNCTIONAL BLOCKS TO EXPLAIN THE OPERATION OF THE READ LOGIC IN DETAIL.

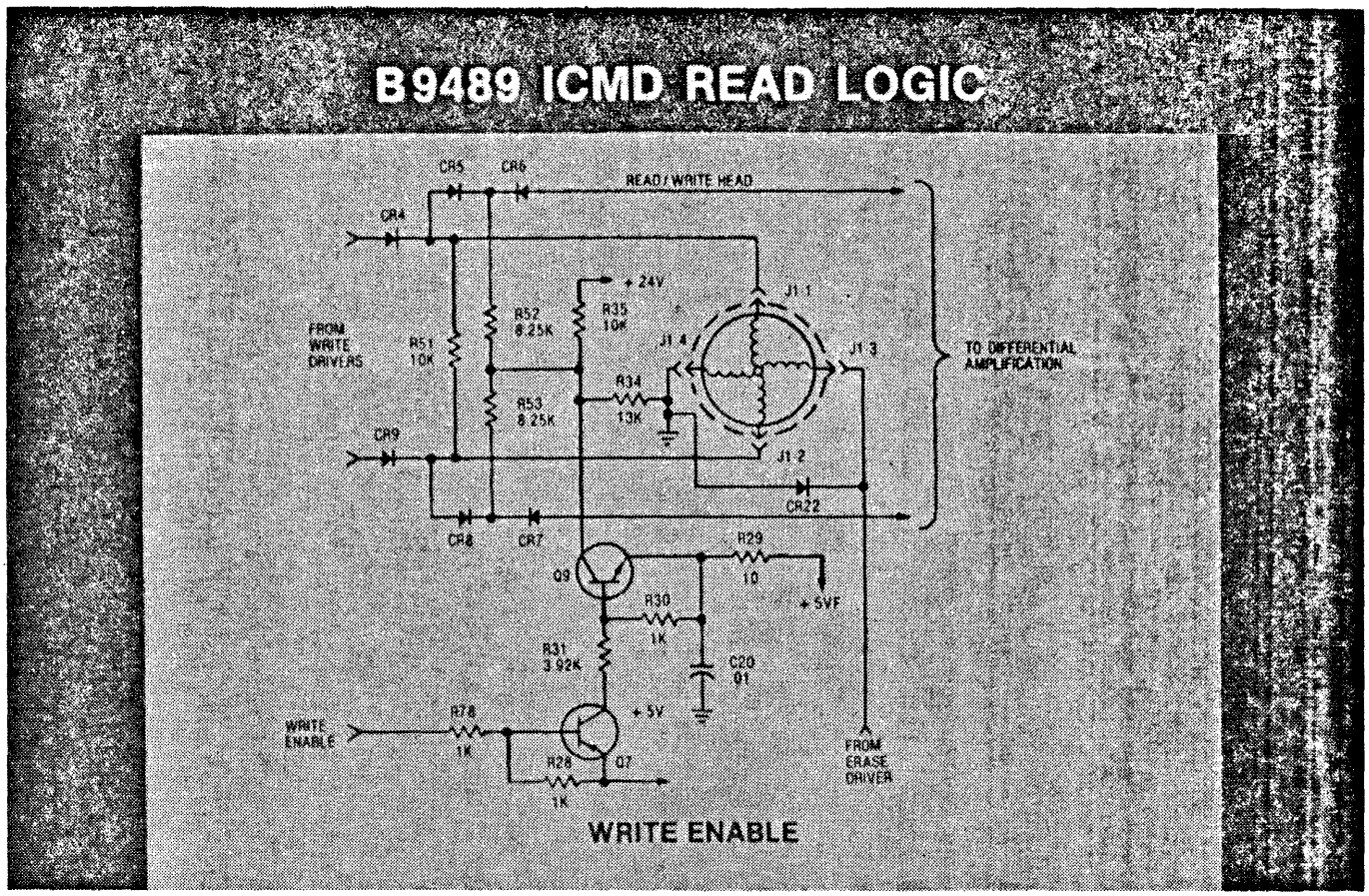
23

B9489 ICMD READ LOGIC



THIS DRAWING SHOWS THE COMPLETE READ LOGIC CIRCUIT. THE FUNCTIONAL BLOCK HIGHLIGHTED IN THIS DIAGRAM IS THE WRITE ENABLE CIRCUITRY. THE WRITE ENABLE CIRCUITRY DETERMINES WHETHER THE READ/WRITE HEAD IS WRITE ENABLED. IF THE READ/WRITE HEAD IS NOT WRITE ENABLED, THEN BY DEFAULT IT IS READ ENABLED.

24

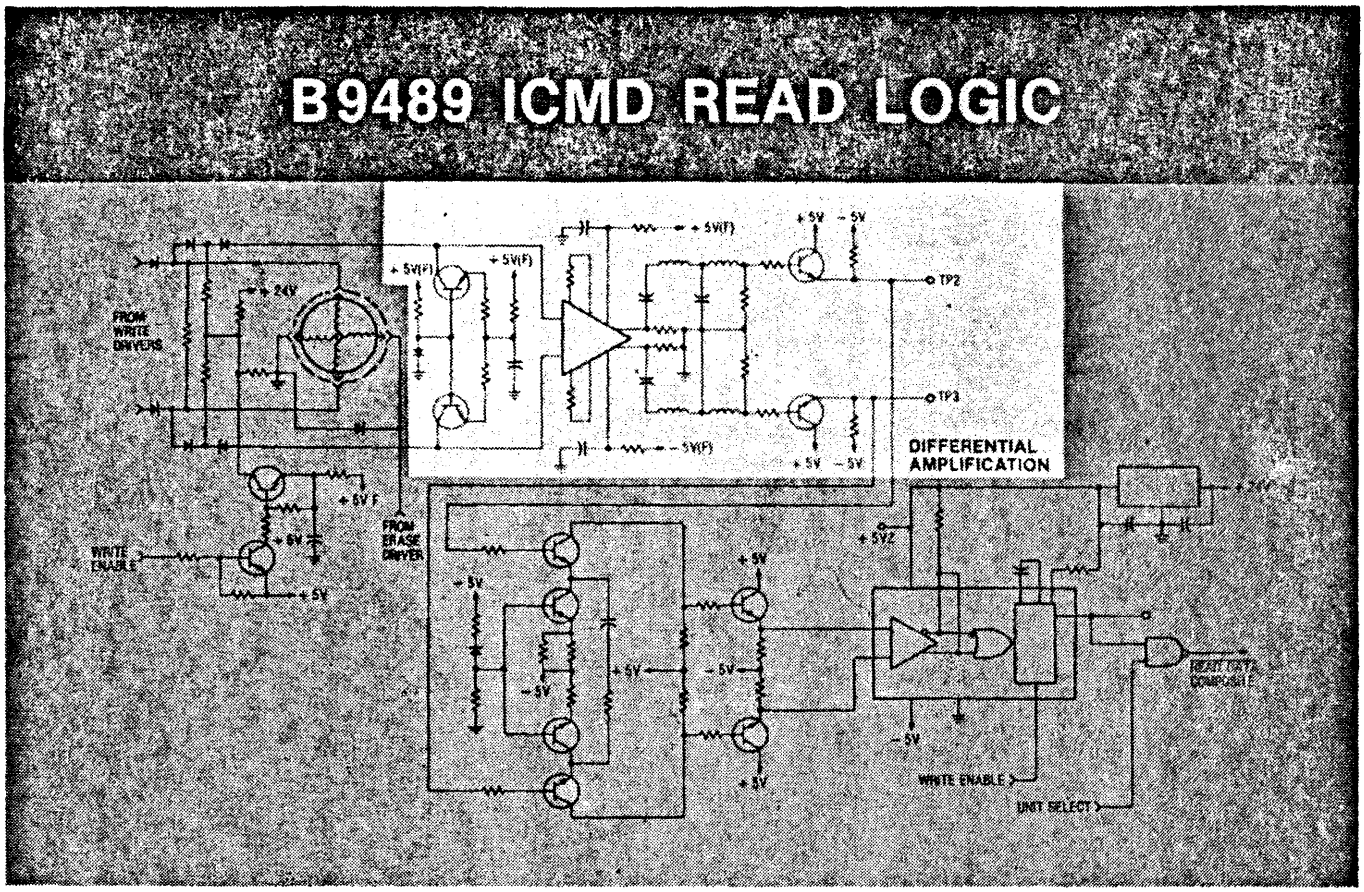


THE DETAIL IS CLARIFIED BY ENLARGING THE FUNCTIONAL BLOCK. THE SIGNAL SHOWN AT THE BOTTOM LEFT OF THE DRAWING IS WRITE ENABLE, DERIVED FROM THE INTERFACE SIGNAL. WRITE ENABLE IS A LOGICAL 1, THAT IS 5 VOLTS OR HIGH, TO ENABLE THE WRITE DRIVERS. WHEN WRITE ENABLE IS A LOGICAL 0, THAT IS 0 VOLTS OR LOW, THE WRITE DRIVERS ARE DISABLED AND CONSEQUENTLY THE READ LOGIC IS ENABLED.

WHEN WRITE ENABLE IS LOW, THE BLOCKING DIODES CR5 AND CR8 ARE FORWARD BIASED THROUGH THE ACTION OF Q7 AND Q9. THIS ALLOWS THE ANALOGUE SIGNAL FROM THE READ/WRITE HEAD TO PASS TO THE NEXT STAGE IN THE READ LOGIC, DIFFERENTIAL AMPLIFICATION.

25

B9489 ICMD READ LOGIC

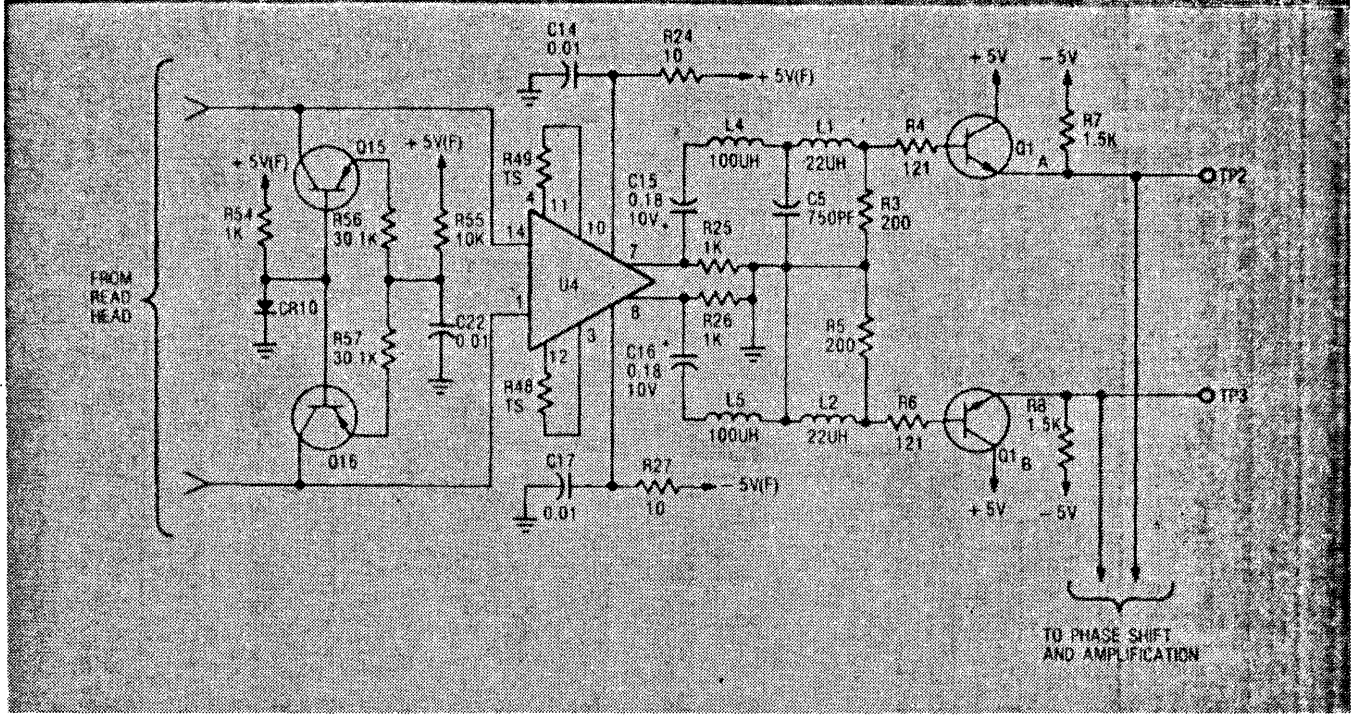


THE DIFFERENTIAL AMPLIFICATION CIRCUIT AMPLIFIES THE DIFFERENCE BETWEEN THE TWO 180 DEGREE OUT-OF-PHASE READ DATA SIGNALS OUTPUT FROM THE READ HEAD.

26

B9489 ICMD READ LOGIC

DIFFERENTIAL AMPLIFICATION



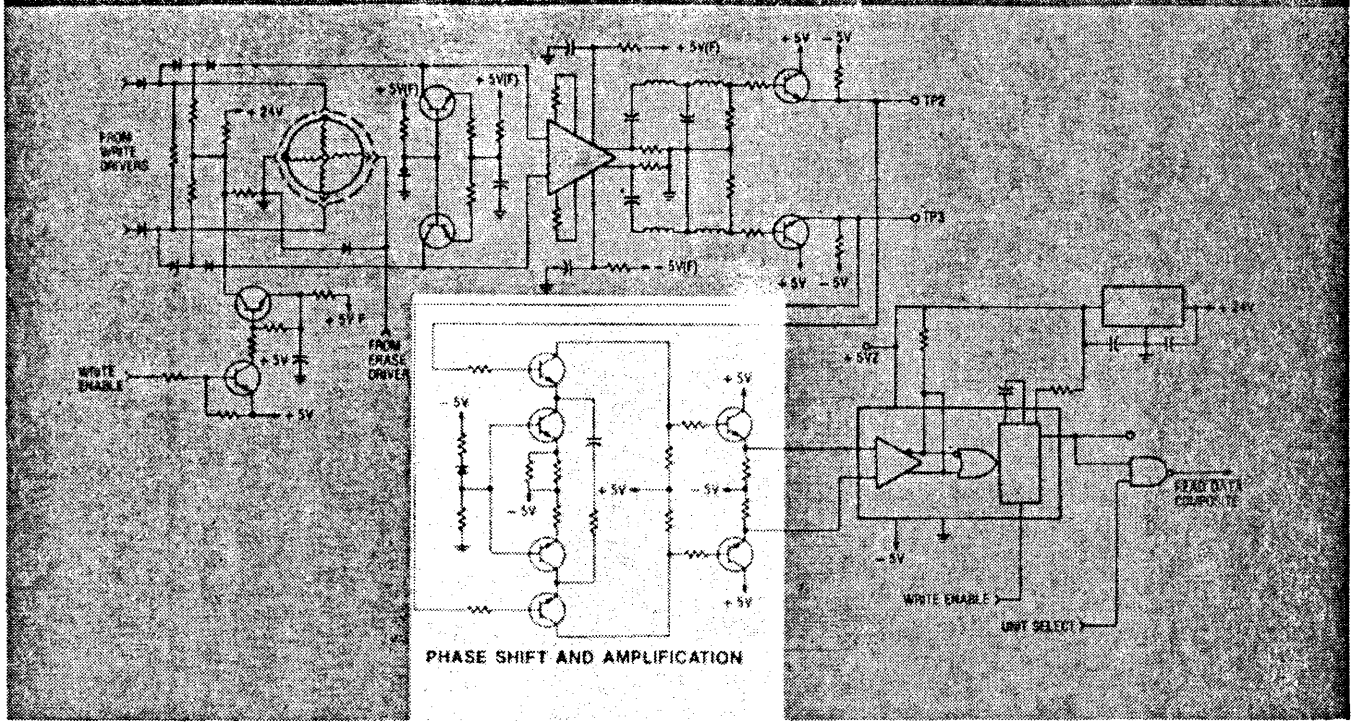
THE DIFFERENTIAL AMPLIFIER IS A MULTI-STAGE CIRCUIT THAT CONSISTS OF A DIFFERENTIAL VIDEO AMPLIFIER U4 AND THE DUAL PACKAGED TRANSISTORS Q1A AND Q1B. THE GAIN OF THE AMPLIFIER IS PRESET BY THE VALUE OF THE RESISTORS R49 AND R48. NOTICE THAT THE VALUE OF THESE RESISTORS IS INDICATED BY THE LETTERS "TS." TS MEANS THE VALUES ARE TEST SELECTED. DETAILED PROCEDURES FOR ESTABLISHING THE CORRECT VALUES FOR THESE COMPONENTS, IN CASE REPLACEMENT IS NECESSARY, ARE DESCRIBED IN A LATER LECTURE.

TWO TEST POINTS, TP2 AND TP3, ARE PROVIDED SO THAT THE SIGNAL OUTPUT FROM A1A AND Q1B CAN BE MEASURED FOR TEST PURPOSES.

THE OUTPUT FROM THE DIFFERENTIAL AMPLIFIER CIRCUIT IS THEN INPUT TO THE NEXT STAGE IN THE READ LOGIC, THE PHASE SHIFT AND AMPLIFICATION CIRCUIT.

27

B9489 ICMD READ LOGIC



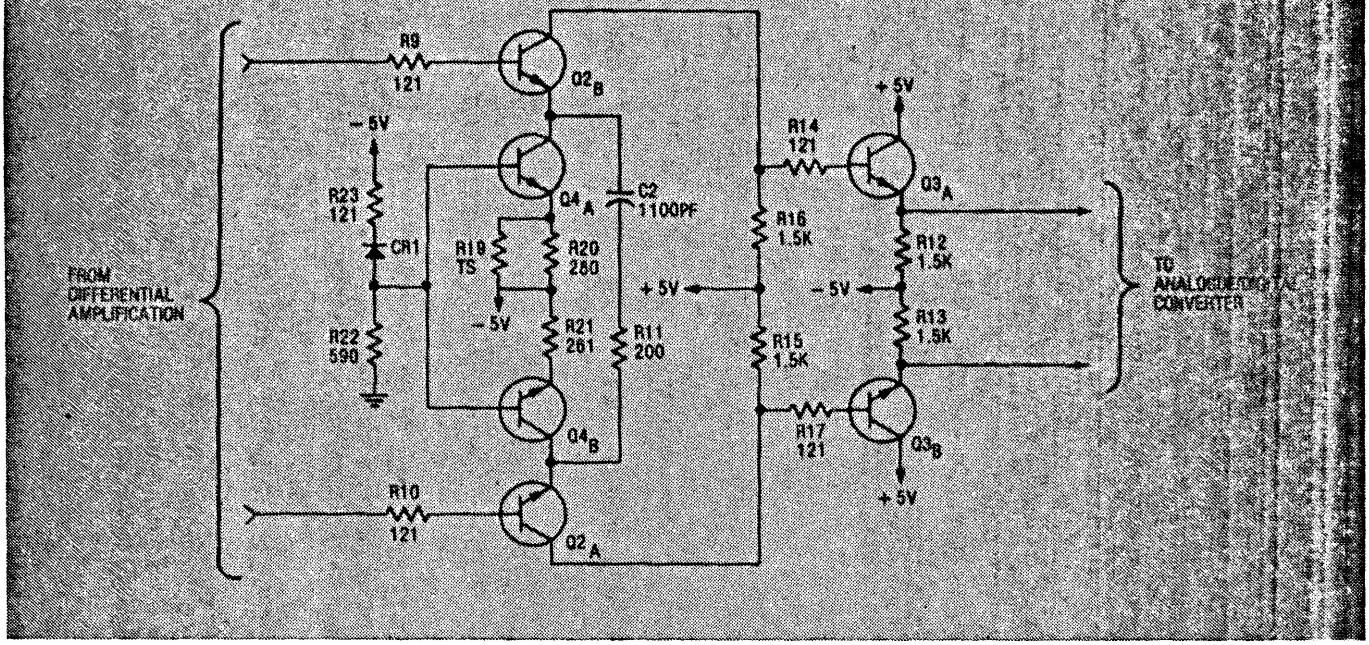
THE PHASE SHIFT AND AMPLIFICATION CIRCUIT, PHASE SHIFTS ONE OF THE SIGNALS FROM THE DIFFERENTIAL AMPLIFICATION CIRCUIT BY 90 DEGREES RELATIVE TO THE OTHER ONE.

THIS PHASE SHIFT, TOGETHER WITH A FURTHER STAGE OF AMPLIFICATION, IS THE FIRST STAGE IN THE CONVERSION FROM THE ANALOGUE SIGNAL, READ FROM THE DISKETTE, TO THE DIGITAL SIGNAL REQUIRED BY THE HOST SYSTEM CONTROLLER.

28

B9489 ICMD READ LOGIC

PHASE SHIFT AND AMPLIFICATION

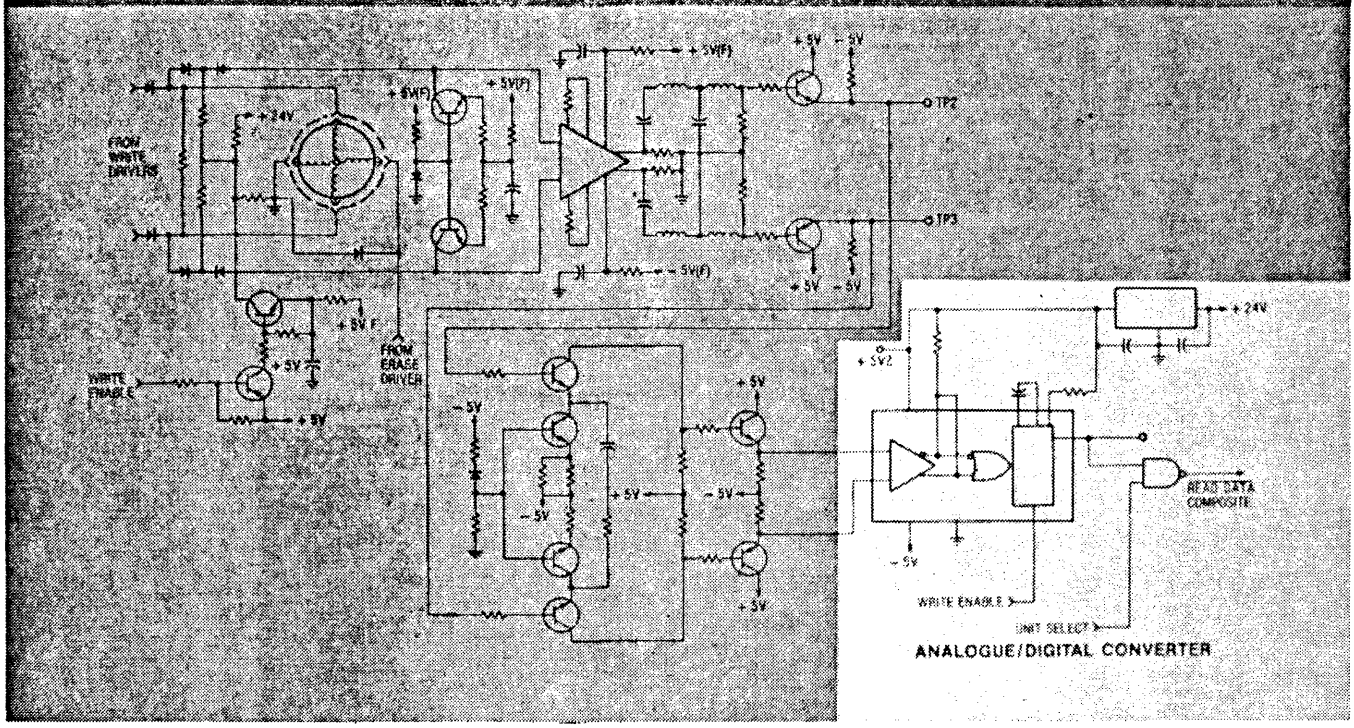


THE PHASE SHIFT CIRCUIT IS COMPRISED OF THE DUAL PACKAGED TRANSISTORS Q2A AND Q2B TOGETHER WITH THE RESISTANCE/CAPACITANCE NETWORK OF C2 AND R11, TO PHASE SHIFT THE TWO ANALOGUE READ SIGNALS, SO THAT THEY ARE 90 DEGREES OUT-OF-PHASE.

TRANSISTORS Q4A AND Q4B ARE THE CURRENT SOURCES FOR Q2A AND Q2B. THE RESISTOR R19 IS ANOTHER TEST SELECTED VALUE RESISTOR. R19 IS SELECTED TO CONTROL THE DC BALANCE OF THE TWO 90 DEGREE PHASE SHIFTED SIGNALS BEFORE THEY ARE APPLIED TO THE NEXT STAGE IN THE READ LOGIC CIRCUITRY. ADDITIONAL AMPLIFICATION OF THESE SIGNALS IS PROVIDED BY TRANSISTORS Q3A AND Q3B. THE NEXT STAGE IS ANALOGUE TO DIGITAL CONVERSION.

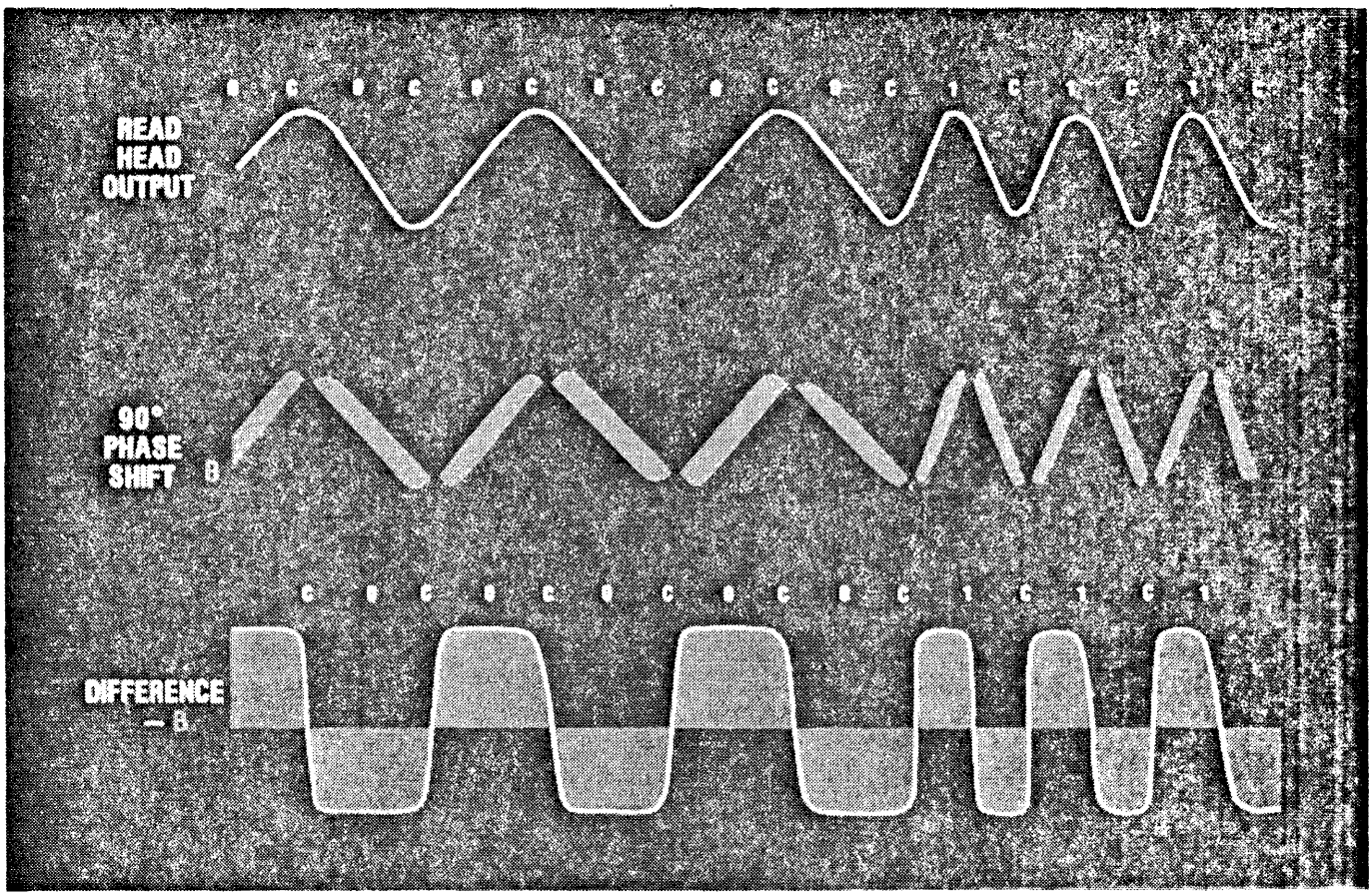
29

B9489 ICMD READ LOGIC



ANALOGUE TO DIGITAL CONVERSION IS THE FINAL STAGE IN THE READ LOGIC BEFORE THE RESULTING SERIAL DATA CAN BE TRANSFERRED TO THE HOST SYSTEM CONTROLLER. THE ANALOGUE TO DIGITAL CONVERTER USES THE TWO 90 DEGREE OUT-OF-PHASE SIGNALS TO PRODUCE A COMPOSITE READ DATA SIGNAL CONTAINING THE SERIAL CLOCK AND DATA PULSES AT NORMAL LOGIC LEVELS.

30



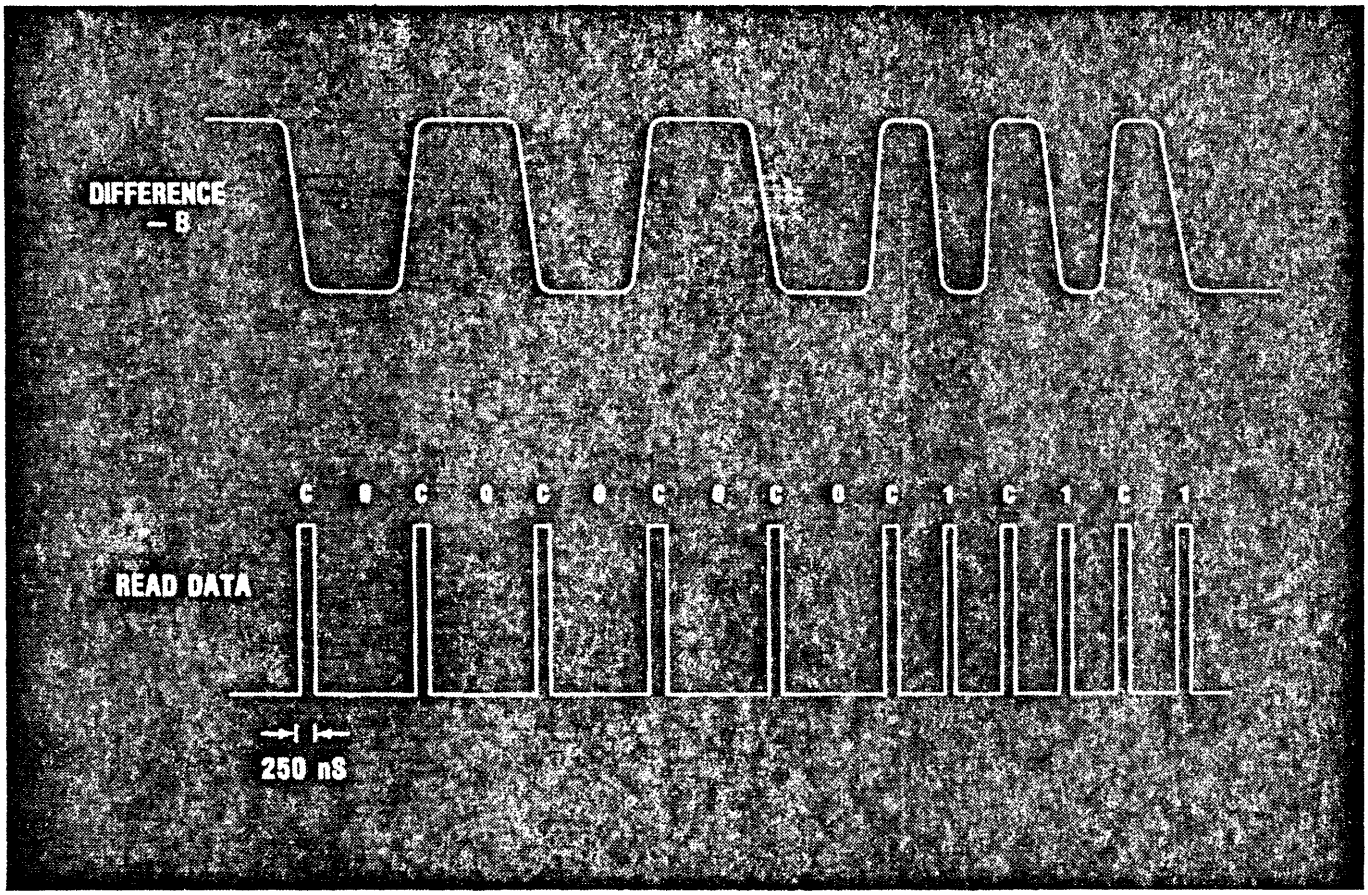
BEFORE EXAMINING THE CIRCUIT OF THE DIGITAL TO ANALOGUE CONVERTER IN DETAIL, LET US LOOK MORE CLOSELY AT TWO SIGNALS INPUT TO THE FIRST STAGE OF THE ANALOGUE TO DIGITAL CONVERTER.

THE UPPER PART OF THE DIAGRAM SHOWS A TYPICAL READ HEAD OUTPUT SIGNAL "A", WITH THE 90 DEGREE PHASE SHIFTED SIGNAL "B".

WHEN THESE TWO SIGNALS ARE SUPERIMPOSED AS SHOWN IN THE CENTER OF THE DIAGRAM, THE DIFFERENCE BETWEEN THE TWO AREAS CAN BE CLEARLY SEEN. INITIALLY, "A" IS MORE POSITIVE THAN "B", THEN "B" BECOMES MORE POSITIVE THAN "A" AND SO ON.

THE LOWER PART OF THE DIAGRAM REPRESENTS THE DIFFERENCE SIGNAL WHICH APPROXIMATES TO A SQUARE WAVE. IN THIS SIGNAL, BOTH CLOCK AND ONE BITS ARE REPRESENTED BY TRANSITIONS, EITHER POSITIVE OR NEGATIVE GOING, NOT THE LEVEL. THESE TRANSITIONS CORRESPOND TO THE PEAKS IN THE ORIGINAL READ HEAD OUTPUT SIGNAL.

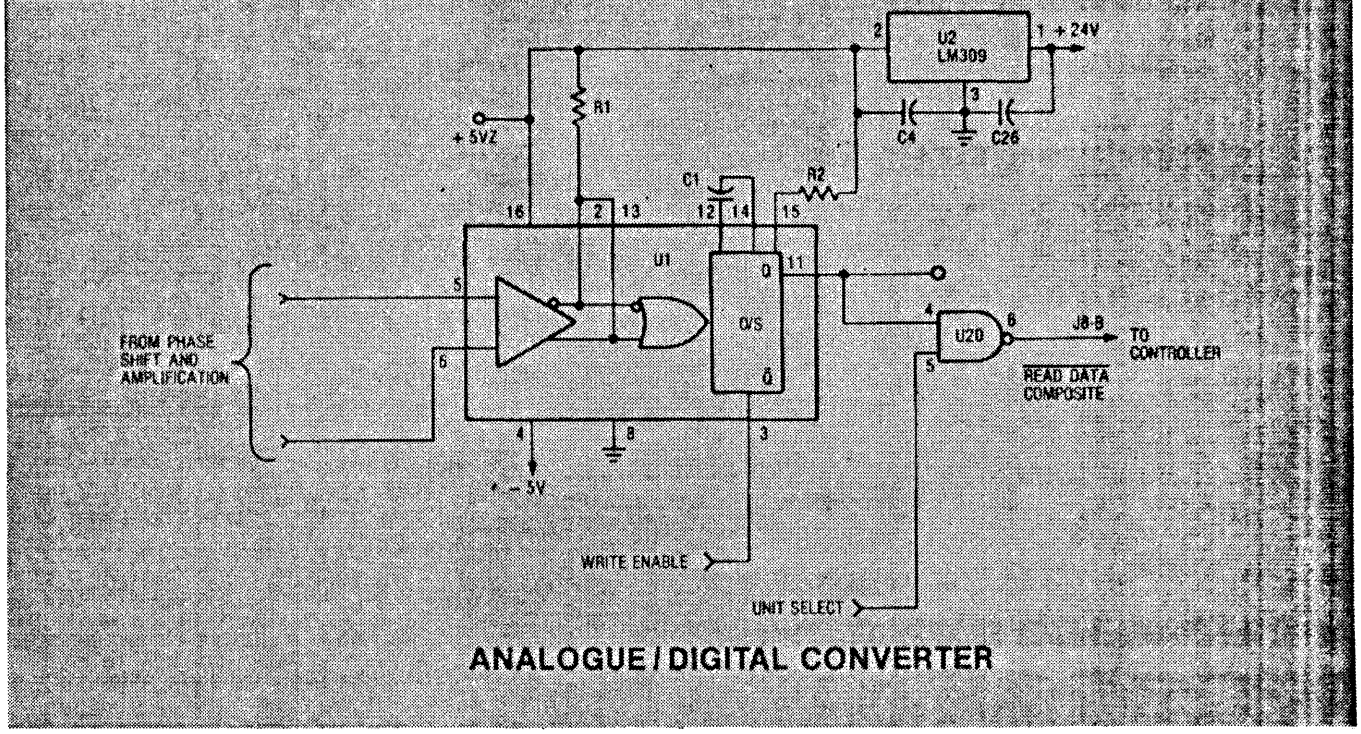
31



THE DIFFERENCE SIGNAL, IN WHICH BOTH CLOCK AND ONE BITS ARE REPRESENTED BY TRANSITIONS, IS INPUT TO A ONE SHOT MULTIVIBRATOR WHICH IS TRIGGERED TO PRODUCE A POSITIVE OUTPUT PULSE FOR BOTH NEGATIVE AND POSITIVE GOING INPUT PULSES. THESE 250 NANOSECOND OUTPUT PULSES BECOME THE DIGITAL INTERFACE SIGNAL, "READ DATA."

32

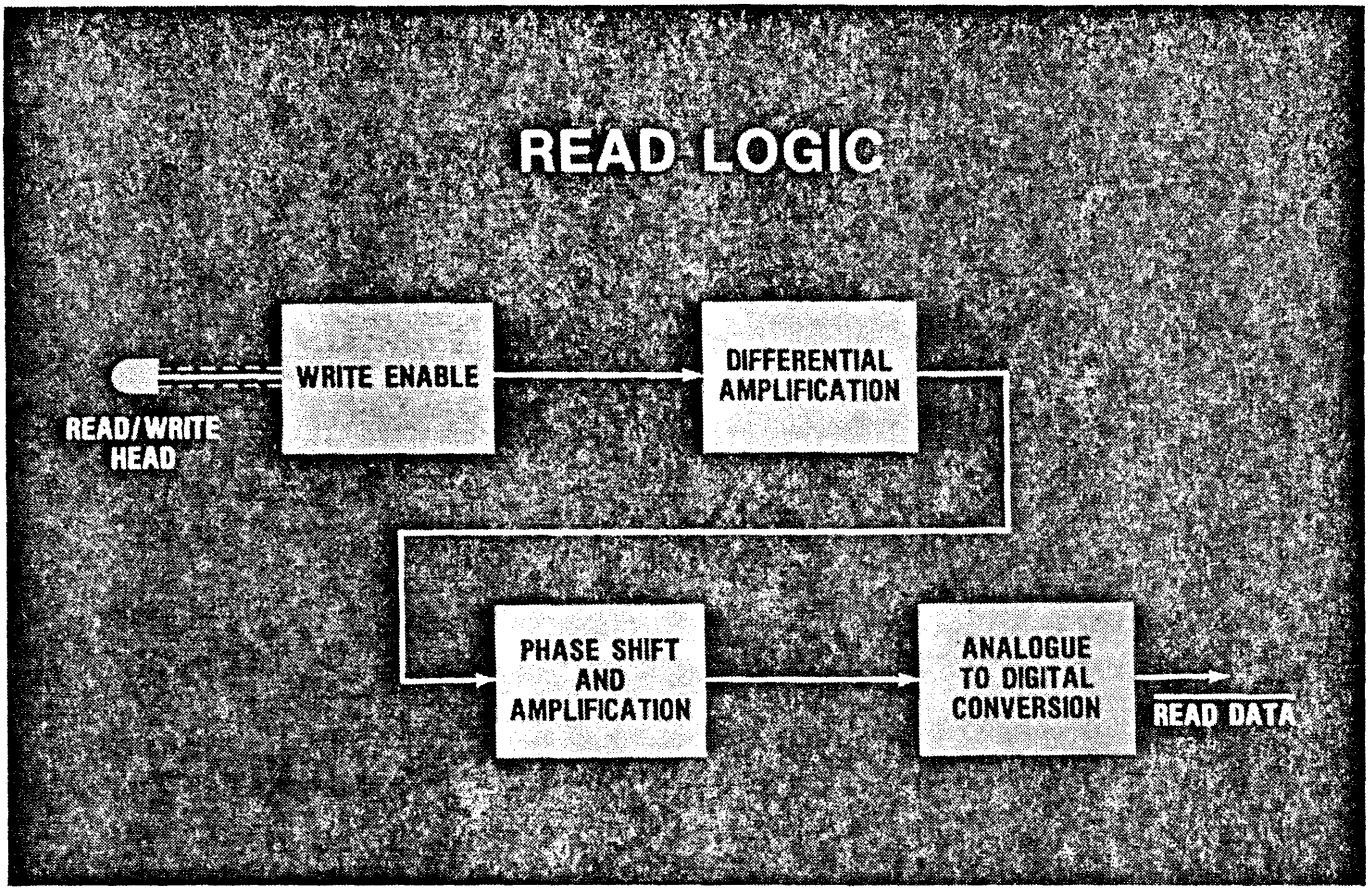
B9489 ICMD READ LOGIC



THE ANALOGUE TO DIGITAL CONVERSION IS ACCOMPLISHED BY ONE INTEGRATED CIRCUIT U1, WHICH IS A COMBINATION DIFFERENTIAL VOLTAGE COMPARATOR AND ONE SHOT MULTIVIBRATOR. THE 250 NANOSECOND PULSE DURATION IS DETERMINED BY THE TIMING CAPACITOR C1. U2 IS A VOLTAGE REGULATOR PROVIDING A WELL REGULATED 5 VOLTS FOR U1.

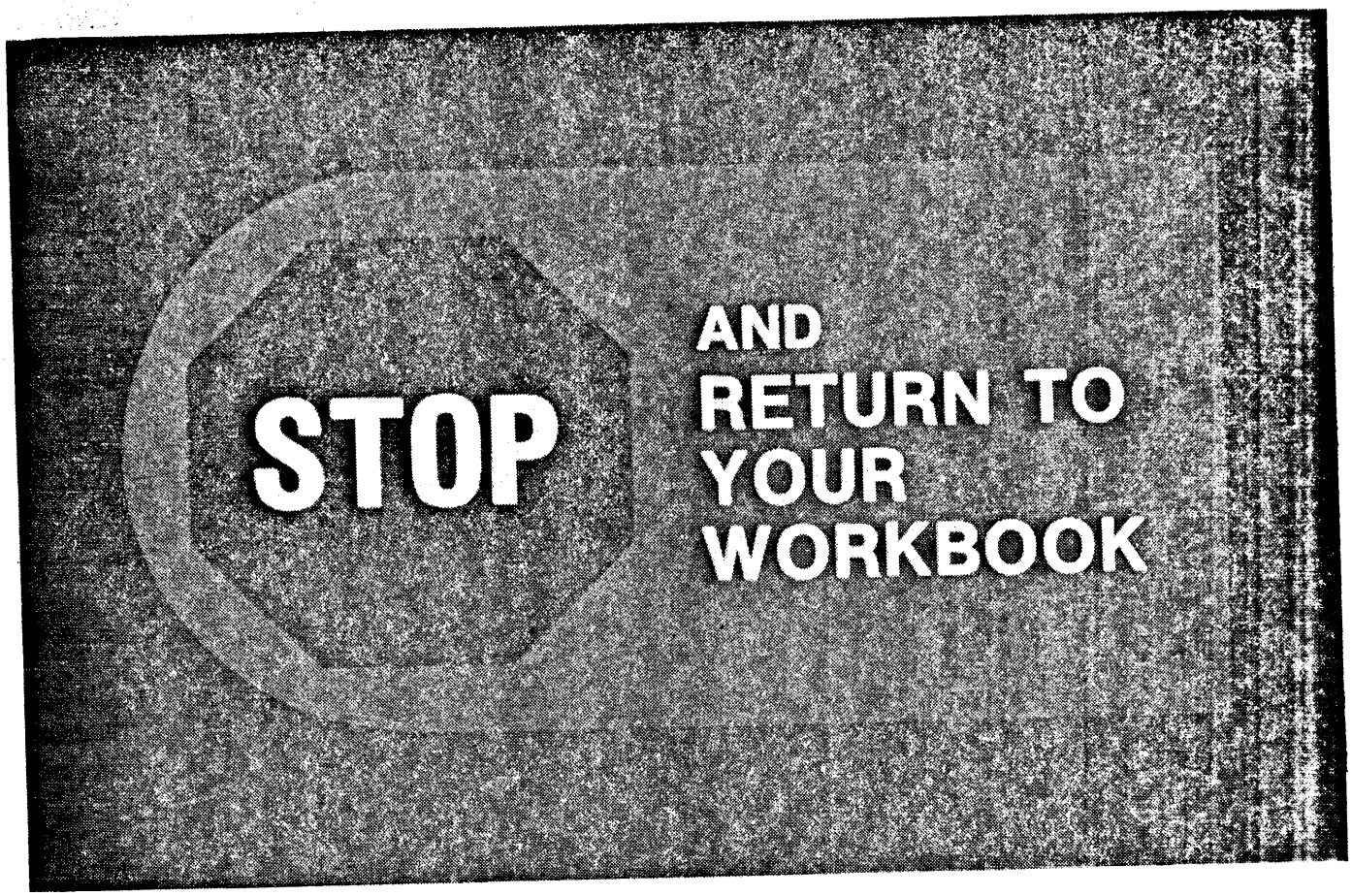
BEFORE THE READ DATA SIGNAL IS OUTPUT TO THE CONTROLLER, IT IS GATED WITH THE SIGNAL UNIT SELECT BY U20. U20 INVERTS THE SIGNAL AND UNIT SELECT PREVENTS ANY ERRONEOUS DATA SIGNALS FROM REACHING THE CONTROLLER WHEN THE UNIT IS NOT SELECTED.

33



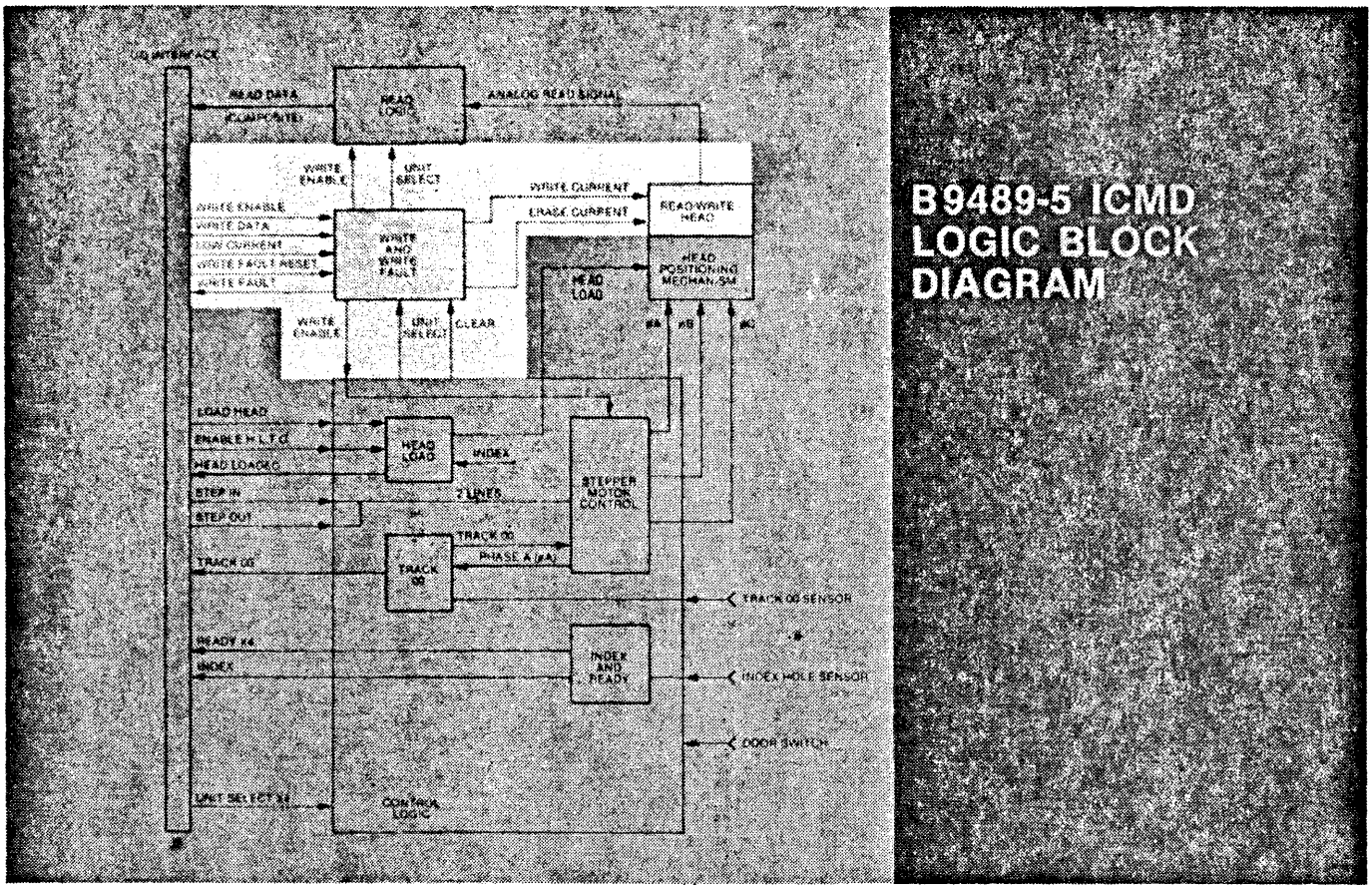
TO SUMMARIZE, THE WRITE ENABLE BLOCK DETERMINES WHETHER THE READ/WRITE HEAD IS READ OR WRITE ENABLED. THE OUTPUT SIGNAL PASSES THROUGH A DIFFERENTIAL AMPLIFIER. THE AMPLIFIED SIGNALS ARE PHASE SHIFTED TO PRODUCE TWO SIGNALS WITH A PHASE DIFFERENCE OF 90 DEGREES BEFORE BEING CONVERTED TO A DIGITAL SIGNAL, "READ DATA."

34



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

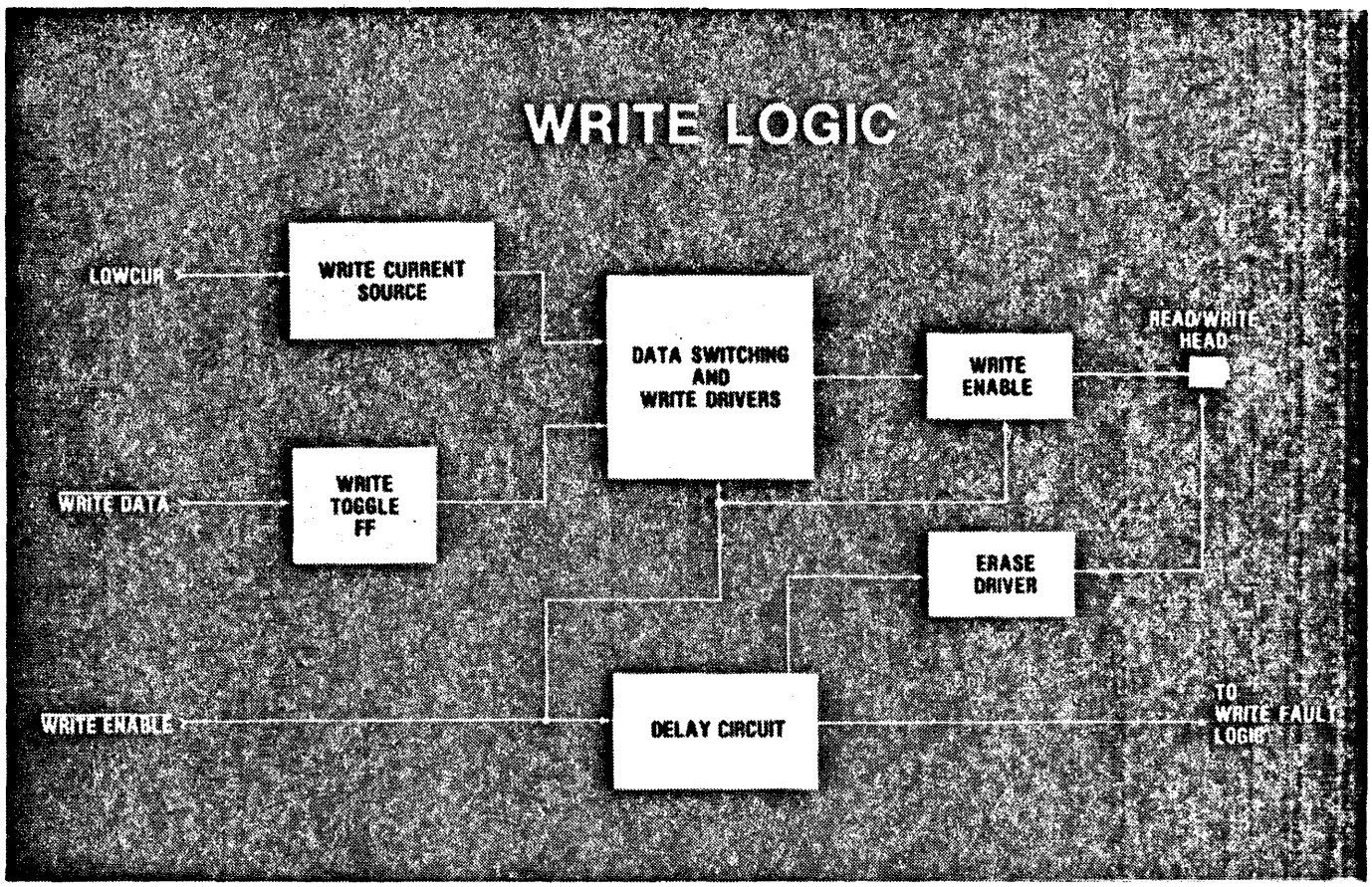
35



RETURNING TO THE LOGIC BLOCK DIAGRAM OF THE ICMD UNIT, THE NEXT FUNCTIONAL BLOCK IS THE WRITE AND WRITE FAULT LOGIC.

THE WRITE AND WRITE FAULT LOGIC USES THE SERIAL CLOCK AND DATA SIGNAL "WRITE DATA" FROM THE HOST SYSTEM CONTROLLER TO PRODUCE THE SIGNAL USED TO WRITE TO THE DISKETTE.

36



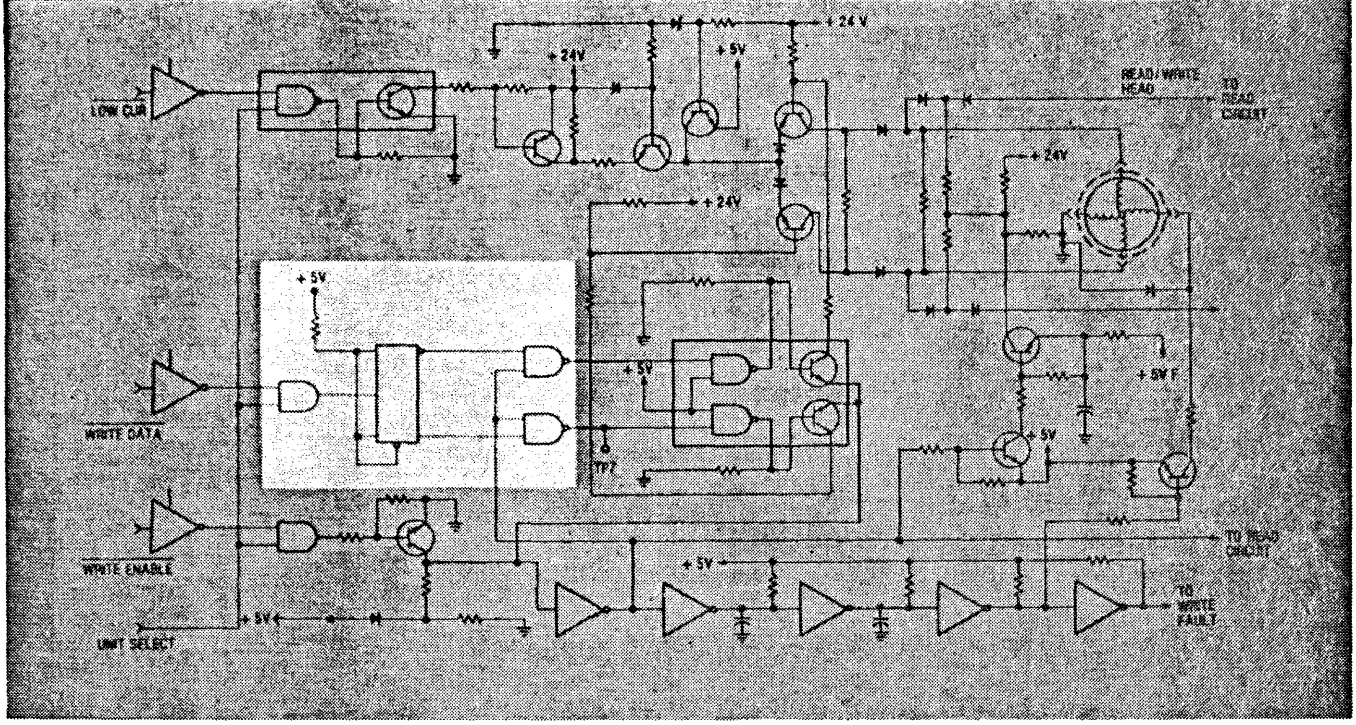
THE WRITE LOGIC CONSISTS OF SIX MAIN FUNCTIONAL AREAS. THESE ARE THE WRITE TOGGLE FLIP FLOP; DATA SWITCHING AND WRITE DRIVERS; THE WRITE CURRENT SOURCE; THE WRITE ENABLE LOGIC; A DELAY CIRCUIT; AND THE ERASE DRIVER.

THE WRITE FAULT LOGIC IS NOT SHOWN IN THIS DIAGRAM, BUT IS EXPLAINED LATER.

AS WITH THE READ LOGIC, EACH BLOCK IN THE DIAGRAM IS RELATED TO THE SCHEMATIC AND EXPLAINED INDIVIDUALLY, STARTING WITH THE WRITE TOGGLE FLIP FLOP.

37

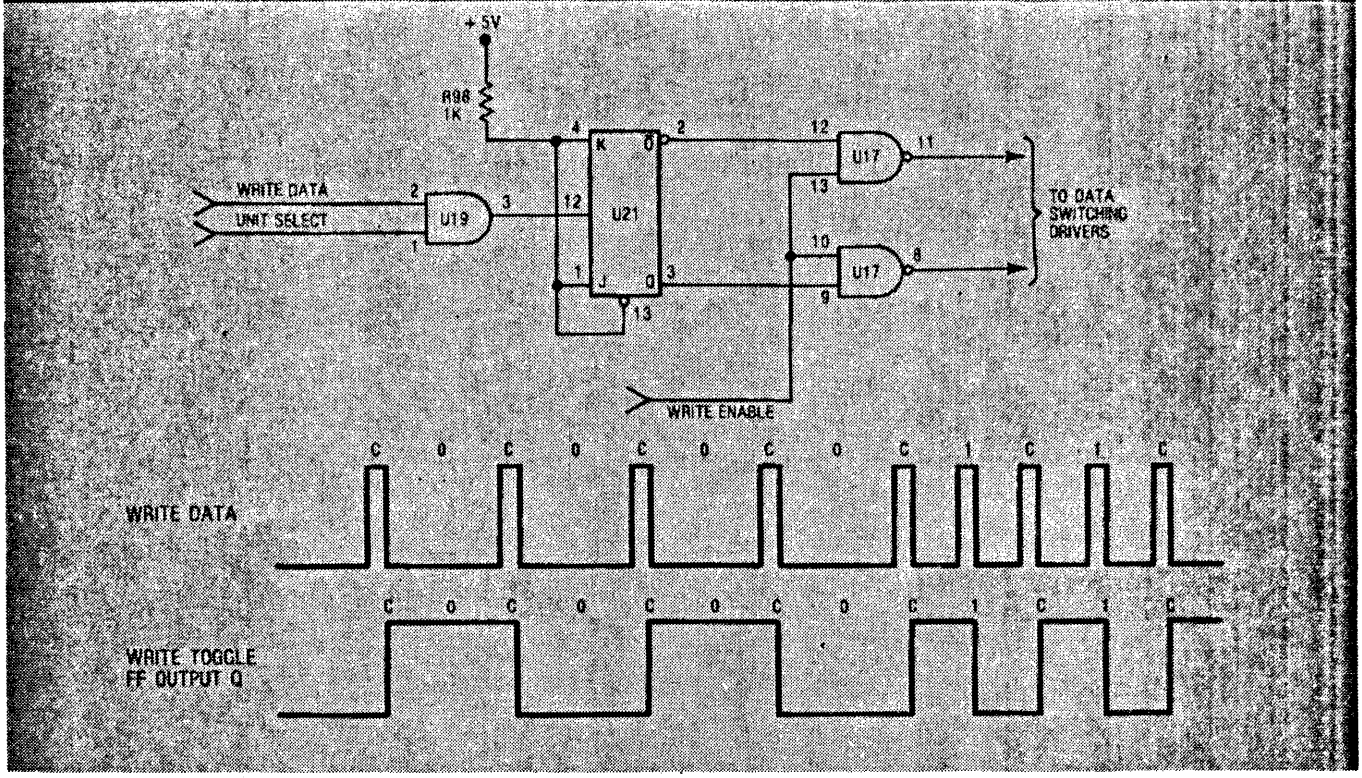
WRITE LOGIC — WRITE TOGGLE FLIP FLOP



THE WRITE TOGGLE FLIP FLOP IS THE FIRST STAGE IN CONVERSION OF THE COMPOSITE CLOCK AND DATA BIT SERIAL DATA SIGNAL FROM THE HOST SYSTEM CONTROLLER TO THE SIGNAL USED BY THE WRITE HEAD.

38

WRITE TOGGLE FLIP FLOP



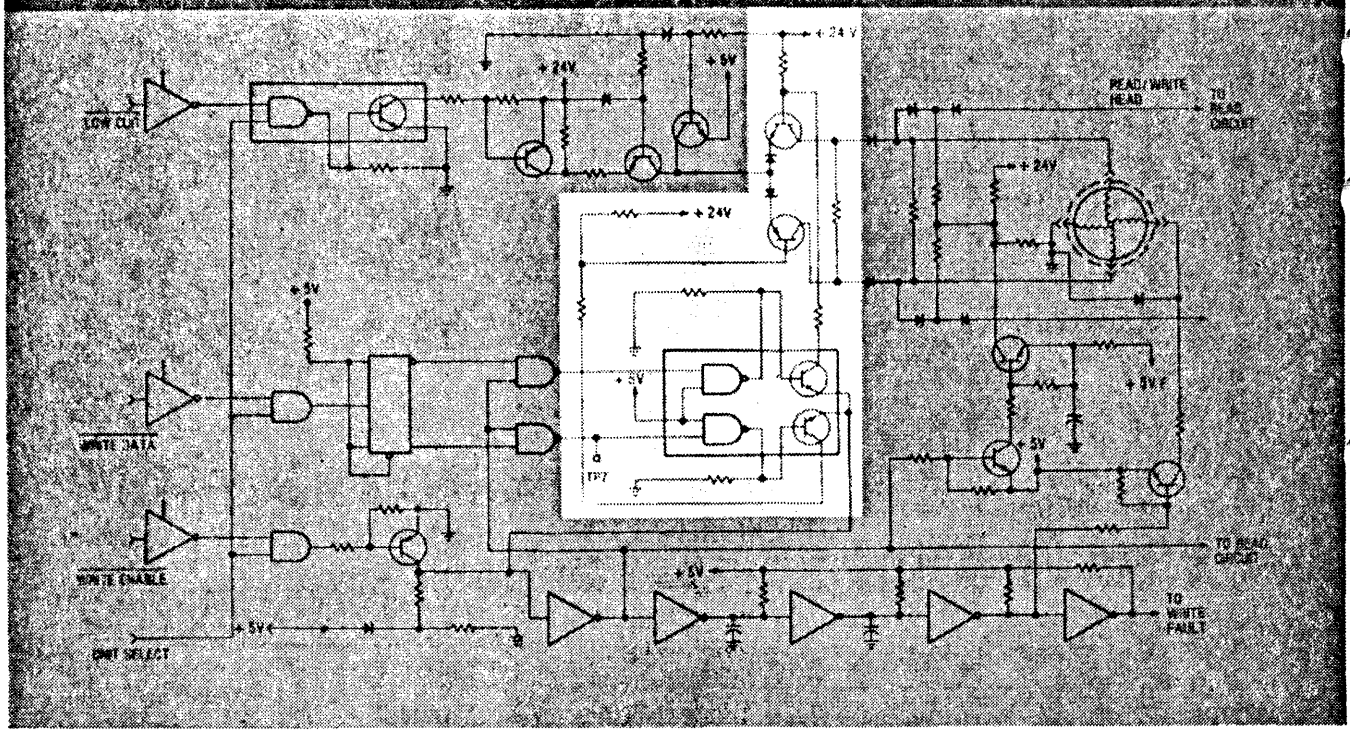
WRITE DATA IS FIRST GATED WITH THE UNIT SELECT TO ENSURE THAT THE DATA IS FOR THIS UNIT. THE WRITE TOGGLE FLIP FLOP U21, IS A JK FLIP FLOP WITH BOTH THE SET AND RESET INPUTS HELD HIGH AND WRITE DATA/ CONNECTED TO THE CLOCK INPUT. IN THIS CONDITION, THE JK FLIP FLOP COMPLIMENTS ON THE TRAILING EDGE OF EACH INPUT DATA PULSE AS SHOWN IN THE LOWER PART OF THE DIAGRAM.

THIS ACTION PRODUCES THE COMPOSITE SIGNAL, SHOWN BELOW THE WRITE DATA SIGNAL, IN WHICH EACH CLOCK AND DATA ONE BIT IS REPRESENTED BY A LEVEL CHANGE AND NOT THE SIGNAL LEVEL.

THE SET AND RESET OUTPUTS OF THE JK FLIP FLOP ARE GATED IN U17 WITH WRITE ENABLE BEFORE BEING OUTPUT TO THE DATA SWITCHING DRIVERS.

39

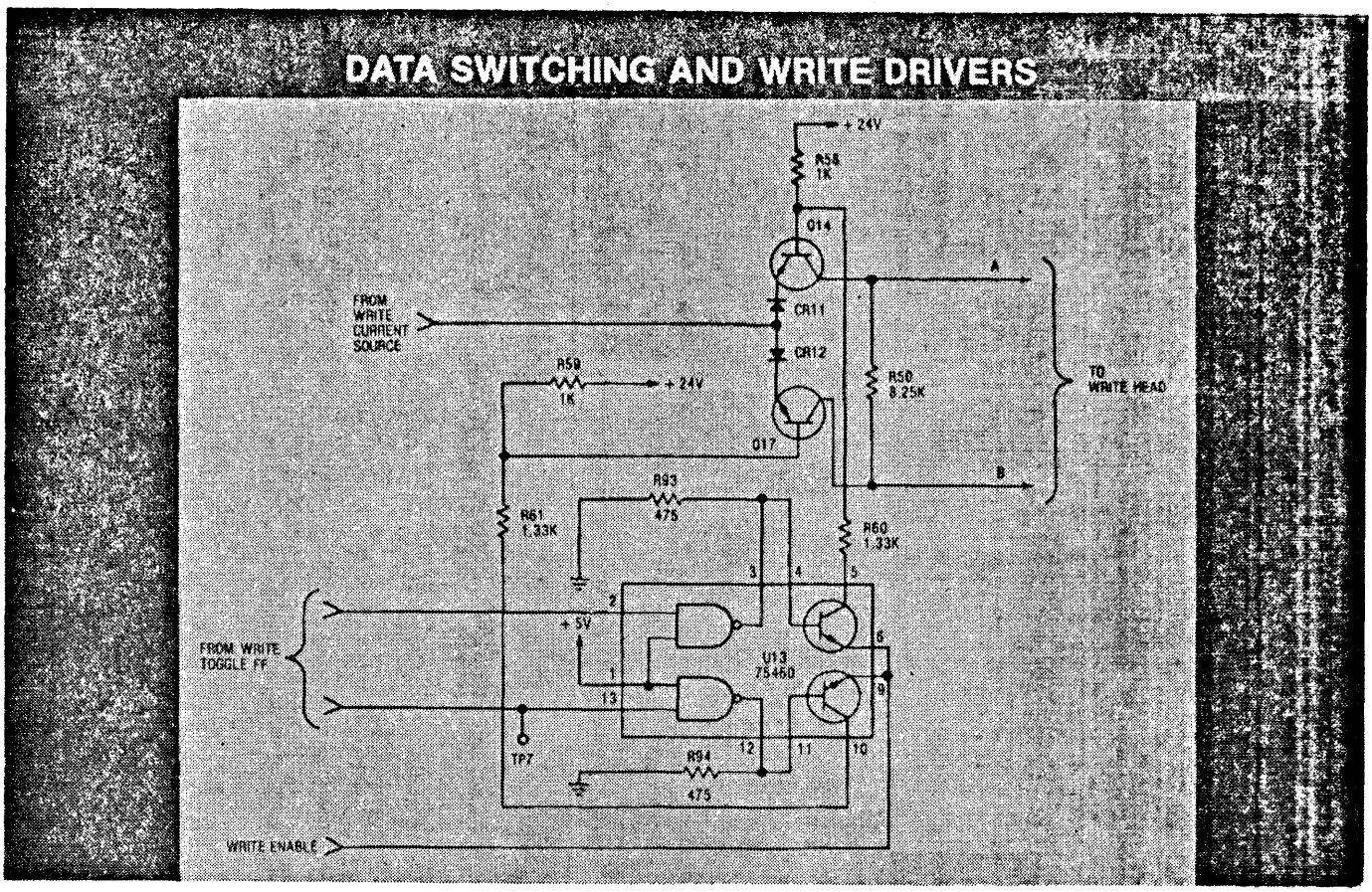
WRITE LOGIC — DATA SWITCHING AND WRITE DRIVERS



THE DATA SWITCHING AND WRITE DRIVERS, HIGHLIGHTED IN THIS DIAGRAM ARE THE NEXT STAGE IN THE WRITE LOGIC. THE DATA SWITCHING DRIVERS CONTROL THE CONDUCTION OF THE WRITE DRIVERS WHICH IN TURN PROVIDE CURRENT TO THE WRITE HEAD.

40

DATA SWITCHING AND WRITE DRIVERS

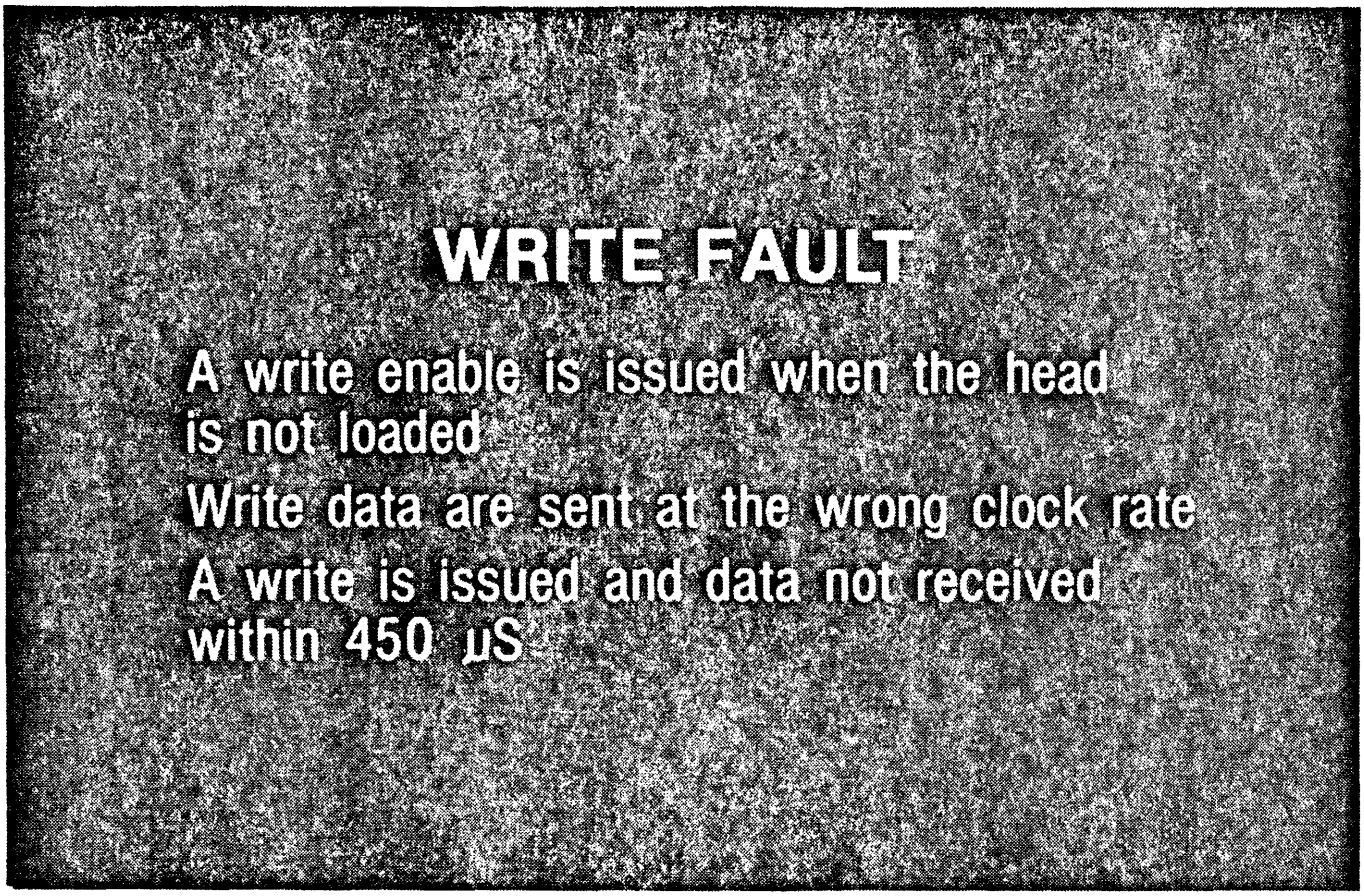


THE TWO DATA SWITCHING DRIVERS ARE LOCATED IN A SINGLE IC PACKAGE U13. BECAUSE THE TWO INPUTS TO U13 ARE THE SET AND RESET OUTPUTS OF THE WRITE TOGGLE FLIP FLOP, ONLY ONE DRIVER CAN CONDUCT AT A TIME. Q14 AND Q17 ARE THE WRITE DRIVER TRANSISTORS. AS ONLY ONE OF THEM CAN CONDUCT AT ANY TIME, Q14 AND Q17 ARE USED TO DETERMINE THE DIRECTION OF CURRENT FLOW THROUGH THE WRITE HEAD. WITH Q14 CONDUCTING, CURRENT FLOWS TO THE WRITE HEAD THROUGH "A" AND NOT "B." WITH Q17 CONDUCTING CURRENT FLOWS TO THE WRITE HEAD THROUGH "B" AND NOT "A."

THE CURRENT FOR THE WRITE DRIVERS IS SUPPLIED FROM THE WRITE CURRENT SOURCE WHICH IS DETAILED LATER.

THE DELAYED WRITE ENABLE SIGNAL IS ALSO USED BY THE WRITE FAULT LOGIC WHICH IS EXPLAINED LATER.

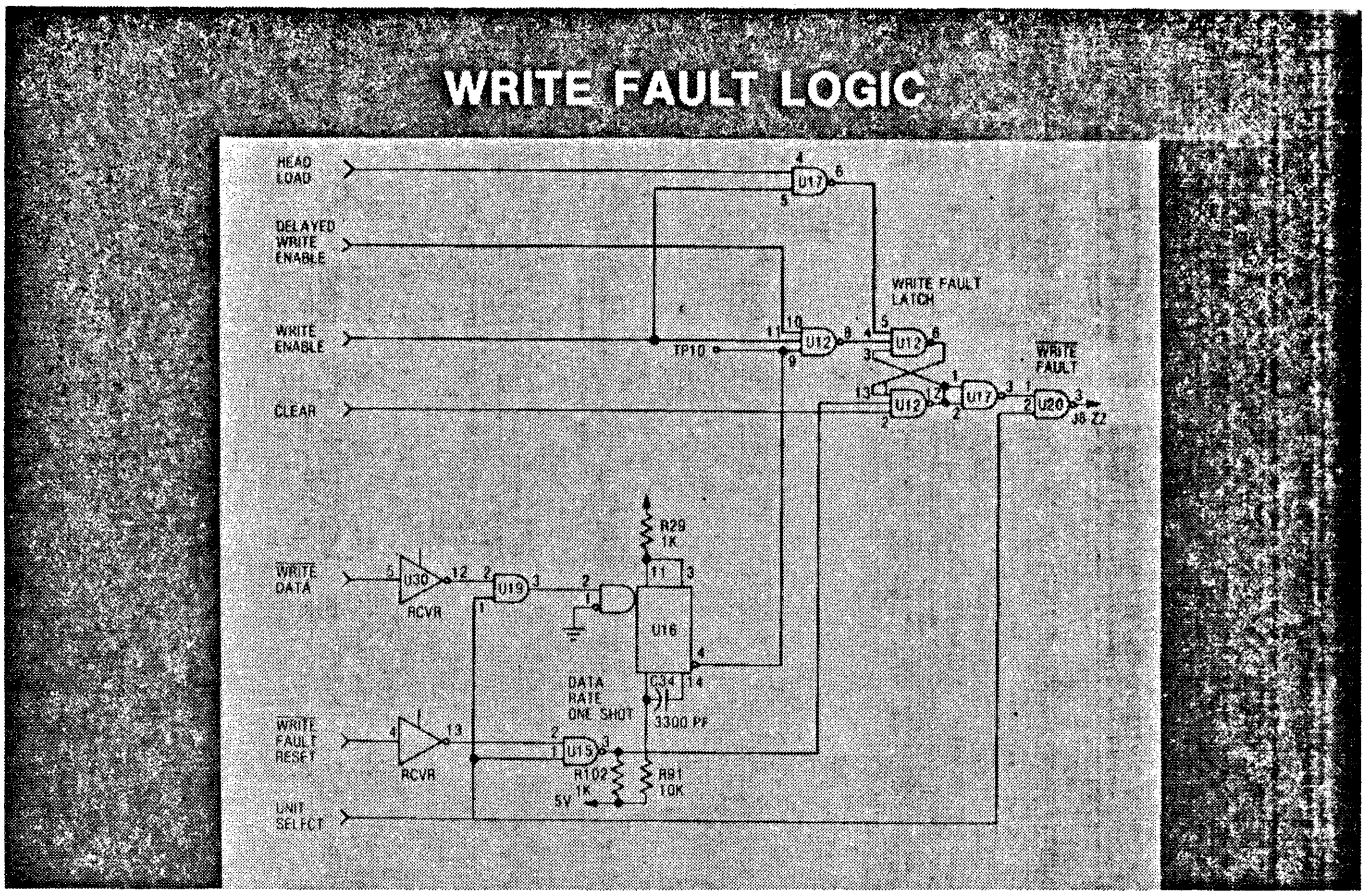
47



A WRITE FAULT IS DEFINED WHEN ONE OR MORE OF THESE CONDITIONS EXIST; A WRITE ENABLE IS ISSUED WHEN THE HEAD IS NOT LOADED; WRITE DATA ARE SENT AT THE WRONG CLOCK RATE; AND/OR A WRITE IS ISSUED AND DATA ARE NOT RECEIVED WITHIN A 450 MICROSECOND TIME PERIOD.

48

WRITE FAULT LOGIC



THE THREE POSSIBLE WRITE FAULT CONDITIONS ARE DETERMINED BY THE WRITE FAULT LOGIC. WHEN A WRITE FAULT OCCURS, THE WRITE FAULT LATCH IS SET TO INDICATE THE CONDITION TO THE HOST SYSTEM CONTROLLER.

THE WRITE FAULT LATCH CONSISTS OF TWO ELEMENTS OF U12.

THE INPUT SIGNAL, HEAD LOAD, IS GATED WITH WRITE ENABLE IN U17 AND THE OUTPUT IS APPLIED TO ONE OF THE SET INPUTS OF THE LATCH. THIS CAUSES THE LATCH TO SET IF WRITE ENABLE IS RECEIVED BEFORE HEAD LOAD.

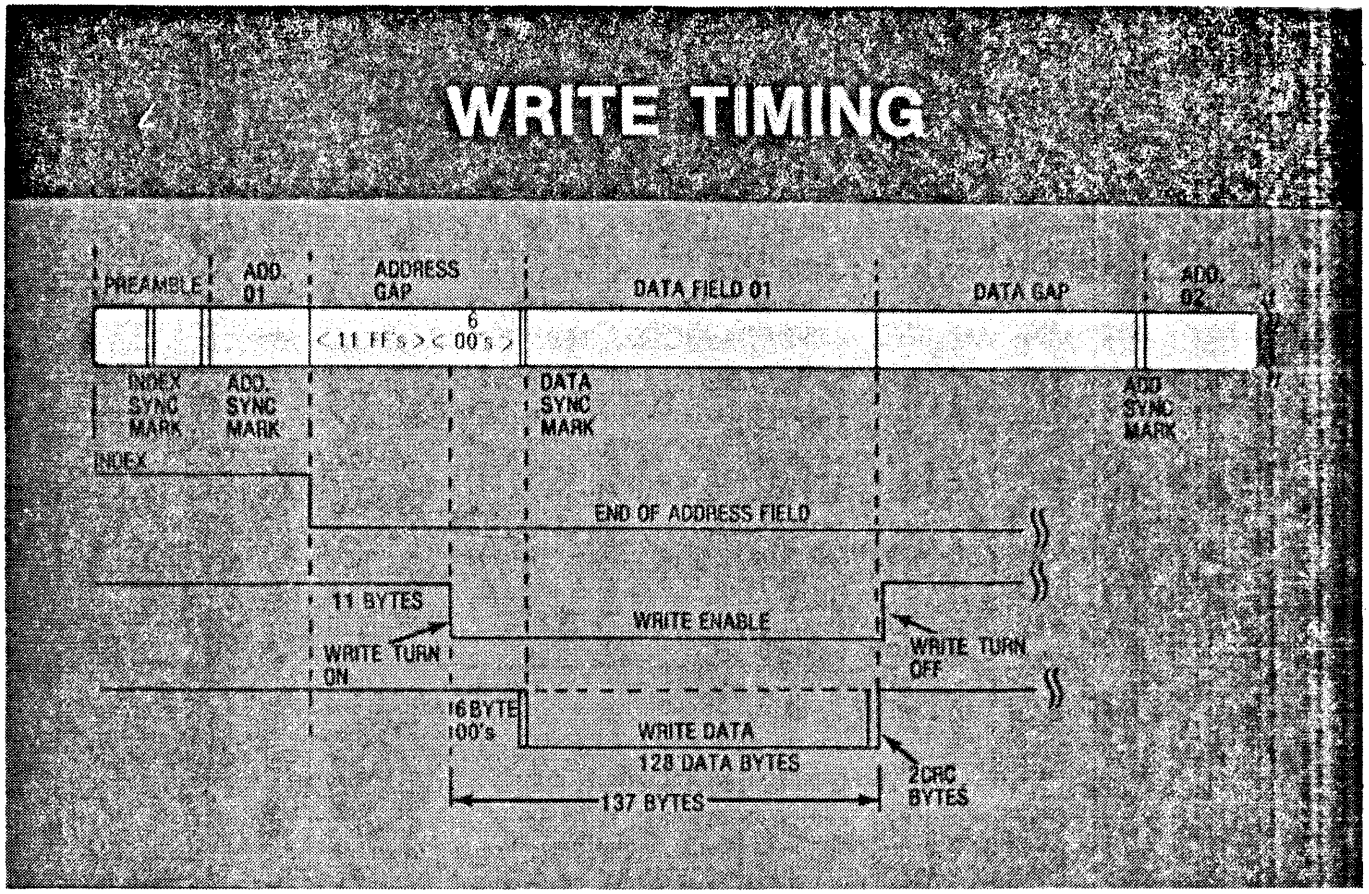
THE OTHER SET INPUT IS THE OUTPUT OF A THREE INPUT "NAND" GATE, ALSO AN ELEMENT OF U12. THE INPUTS TO THIS "NAND" GATE ARE WRITE ENABLE, WRITE

ENABLE DELAYED AND THE INVERTED OUTPUT OF THE DATA RATE ONE SHOT, U16.

U16, IS A RETRIGGERABLE ONE SHOT MULTIVIBRATOR THAT IS TRIGGERED BY THE DATA INPUT. THE FIRST DATA BIT MUST BE RECEIVED BEFORE WRITE ENABLE DELAYED, FROM THE 450 MICROSECOND DELAY CIRCUIT, APPLIES A HIGH TO THE THREE INPUT "NAND" GATE. THE FIRST DATA BIT CAUSES THE INVERTED OUTPUT OF THE ONE SHOT TO GO LOW AND STAY LOW IF THE NEXT DATA BIT IS RECEIVED BEFORE THE ONE SHOT TIMES OUT. IF NO DATA ARE RECEIVED TO TRIGGER THE ONE SHOT OR, IF THE DATA BITS ARE NOT RECEIVED AT A RATE WHICH KEEPS THE ONE SHOT FROM TIMING OUT, THE WRITE FAULT LATCH IS SET.

ONCE THE WRITE FAULT LATCH IS SET, IT CAN ONLY BE RESET BY A WRITE FAULT RESET FROM THE HOST SYSTEM CONTROLLER OR THE CLEAR SIGNAL.

49



THE TIMING OF A WRITE OPERATION IS DETERMINED BY THE HOST SYSTEM CONTROLLER. THIS TIMING DIAGRAM SHOWS THE WRITE SEQUENCE FOR SECTOR ONE WHICH IS BASICALLY THE SAME FOR ALL OTHER SECTORS.

REMEMBER THAT THE DISKETTE IS FORMATTED, MEANING THAT THE ADDRESS FIELDS ARE PREVIOUSLY ENCODED ON THE DISKETTE. THE TOP PART OF THE DIAGRAM SHOWS THE FORMAT AT THE START OF A TRACK ON THE DISKETTE. THE FORMATTED DISKETTE ALLOWS DATA TO BE WRITTEN BY A "WRITE SPLICE" OPERATION IN WHICH THE WRITE STARTS DURING THE ADDRESS GAP AND FINISHES IN THE DATA GAP IMMEDIATELY FOLLOWING THE DATA FIELD.

BEFORE A WRITE OPERATION COMMENCES, THE HOST SYSTEM CONTROLLER

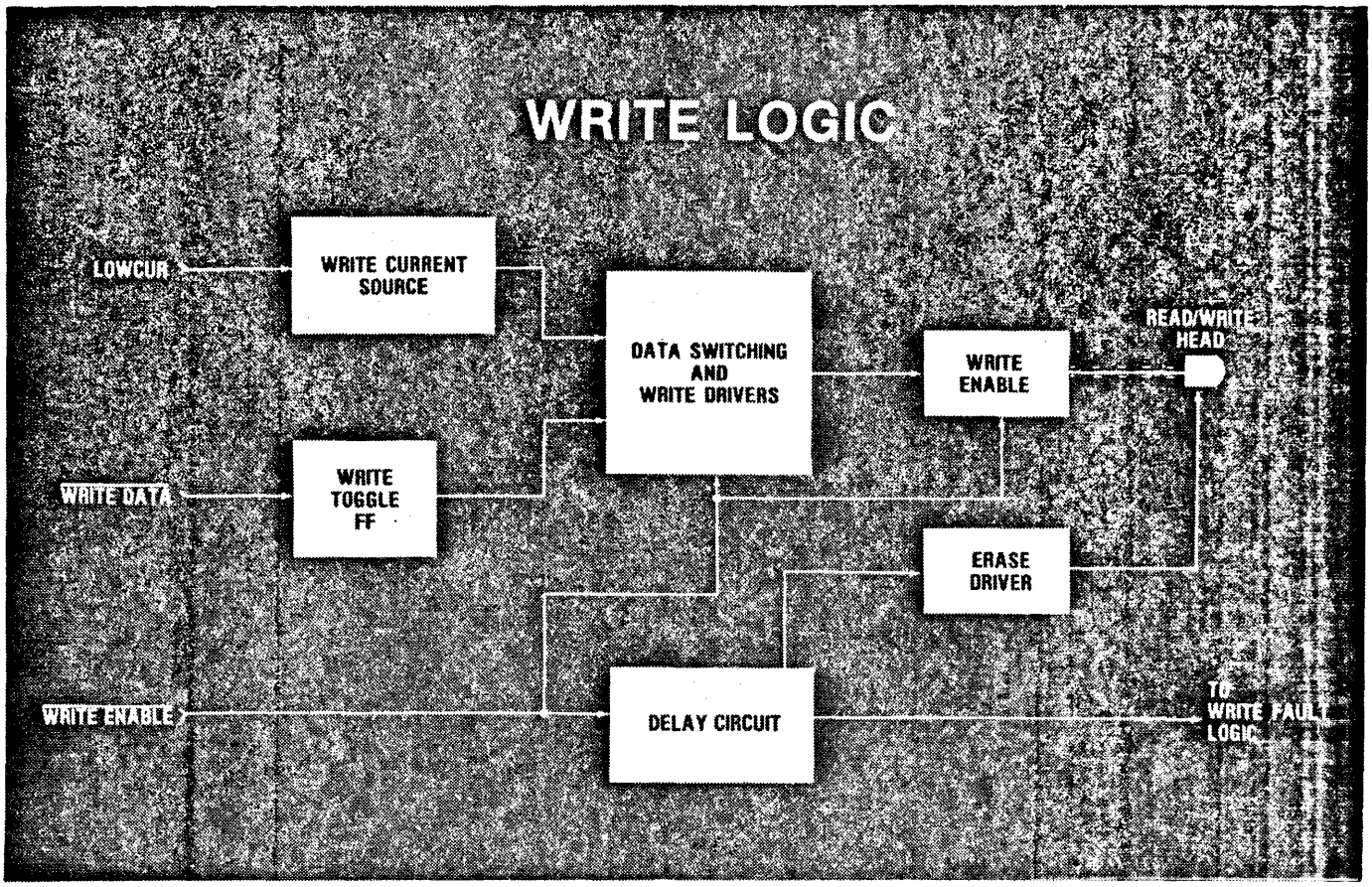
PERFORMS A "SEEK" OPERATION TO FIRST LOCATE THE CORRECT TRACK AND SECOND TO LOCATE THE CORRECT ADDRESS ON THAT TRACK.

WRITE TURN ON OCCURS WHEN WRITE ENABLE GOES LOW, 11 BYTES AFTER COMPLETING THE READ OF THE ADDRESS FIELD. THIS IS FOLLOWED BY THE GENERATION OF SIX BYTES OF ZEROES WHICH PROVIDE A BUFFER ZONE TO ALLOW THE WRITE CIRCUITRY TIME TO TURN ON BEFORE ACTUAL DATA ARE RECEIVED. AFTER THE SIX BYTES OF ZEROES, THE UNIT WRITES A DATA SYNC MARK FOLLOWED BY 128 BYTES OF DATA AND TWO CRC CHARACTERS.

WRITE TURN OFF OCCURS WHEN WRITE ENABLE GOES HIGH TWO BIT TIMES AFTER WRITING THE SECOND CRC BYTE. AFTER WRITING THE LAST BIT OF THE SECOND CRC BYTE, TWO CLOCK BITS WITH ZERO DATA BITS ARE WRITTEN IN THE DATA GAP FIELD.

WRITE ENABLE IS THEN TURNED OFF ON THE THIRD CLOCK BIT TRANSITION. THE REMAINDER OF THE DATA GAP PROVIDES TIME FOR THE WRITE CIRCUITRY TO TURN OFF BEFORE THE READ/WRITE HEAD REACHES THE NEXT ADDRESS FIELD.

50



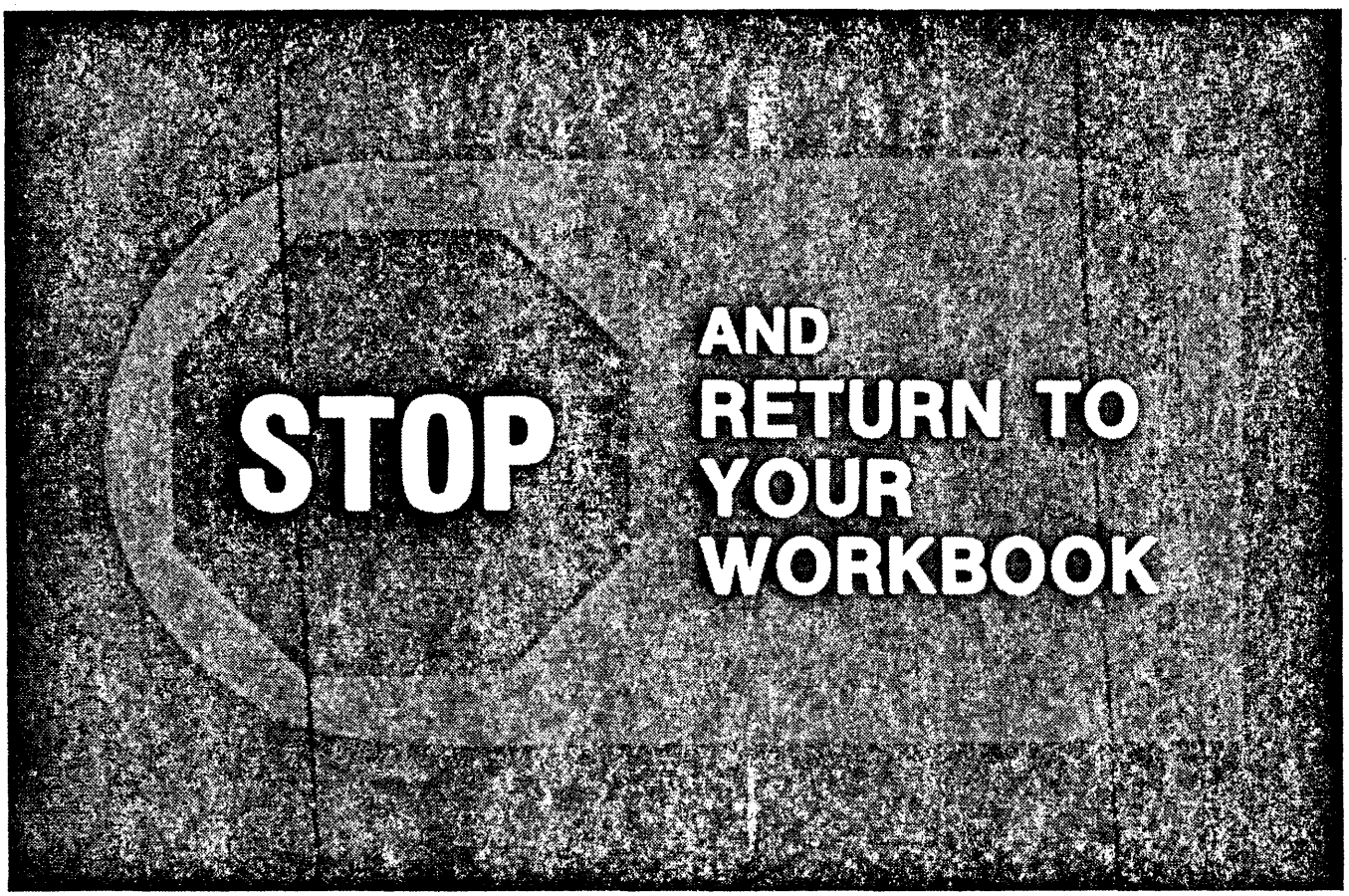
TO SUMMARIZE THE WRITE LOGIC, WRITE DATA/ IS INPUT TO THE WRITE TOGGLE FLIP FLOP WHICH COMPLIMENTS FOR EACH CLOCK OR DATA BIT. THE SET AND RESET OUTPUTS OF THE WRITE TOGGLE FLIP FLOP TOGGLE THE TWO WRITE DRIVERS THROUGH THE DATA SWITCHING DRIVERS WHICH CAUSES THE DIRECTION OF MAGNETIC FLUX IN THE WRITE HEAD TO CHANGE FOR EACH CLOCK OR DATA BIT. THE CURRENT FOR THE WRITE DRIVERS IS PROVIDED THROUGH THE WRITE CURRENT SOURCE WHICH REDUCES THE CURRENT WHEN WRITING TO TRACKS OVER TRACK 43.

THE DELAY CIRCUIT DELAYS THE WRITE ENABLE SIGNAL BY 450 MICROSECONDS BEFORE ENABLING THE ERASE DRIVER FOR THE TUNNEL ERASE.

THE DELAYED WRITE ENABLE SIGNAL IS ALSO USED BY THE WRITE FAULT LOGIC.

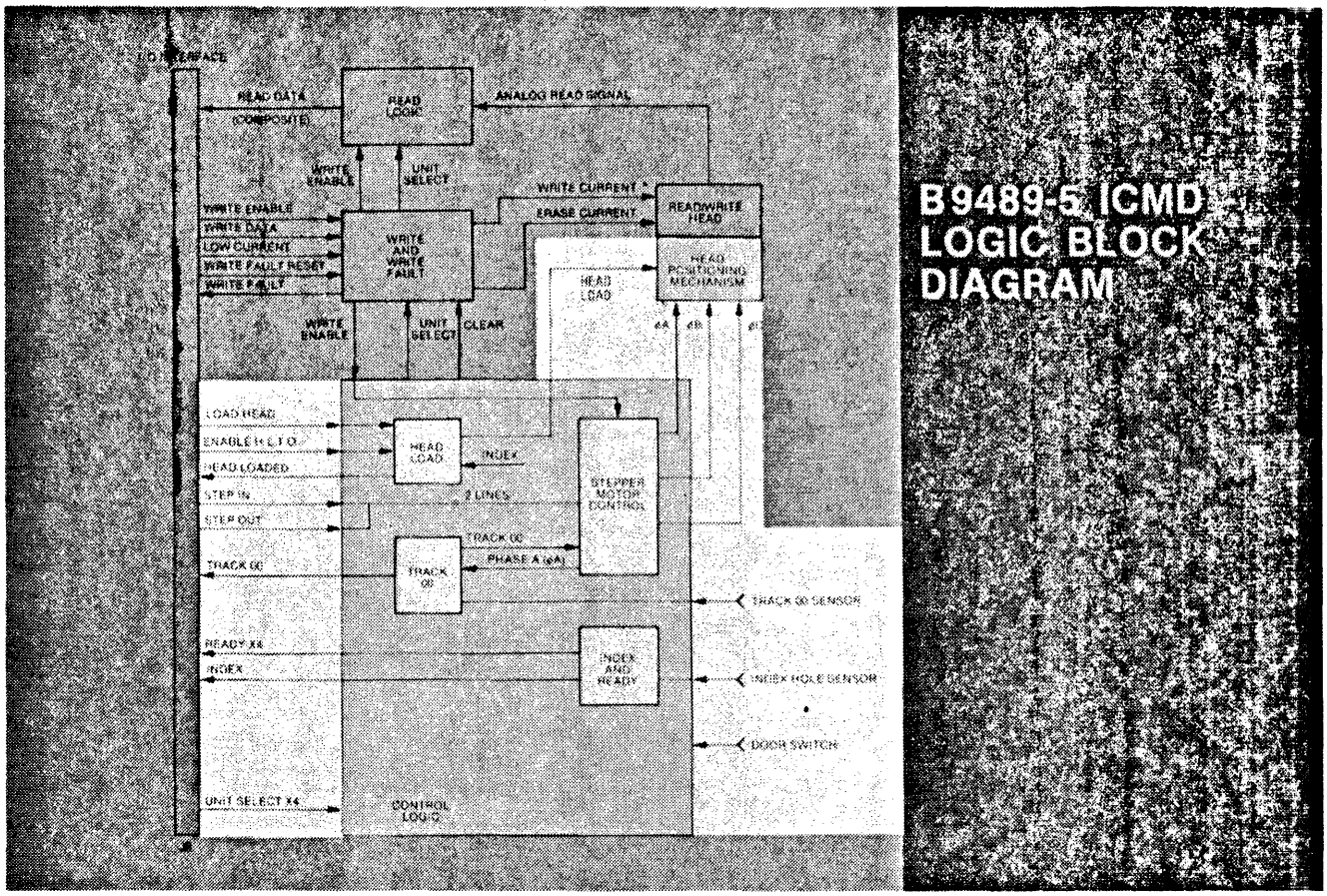
THE WRITE FAULT LOGIC DETECTS POSSIBLE WRITE ERROR CONDITIONS WHICH CAUSE THE WRITE ERROR FLIP FLOP TO LATCH UNTIL IT IS RESET BY THE CONTROLLER.

51



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

52

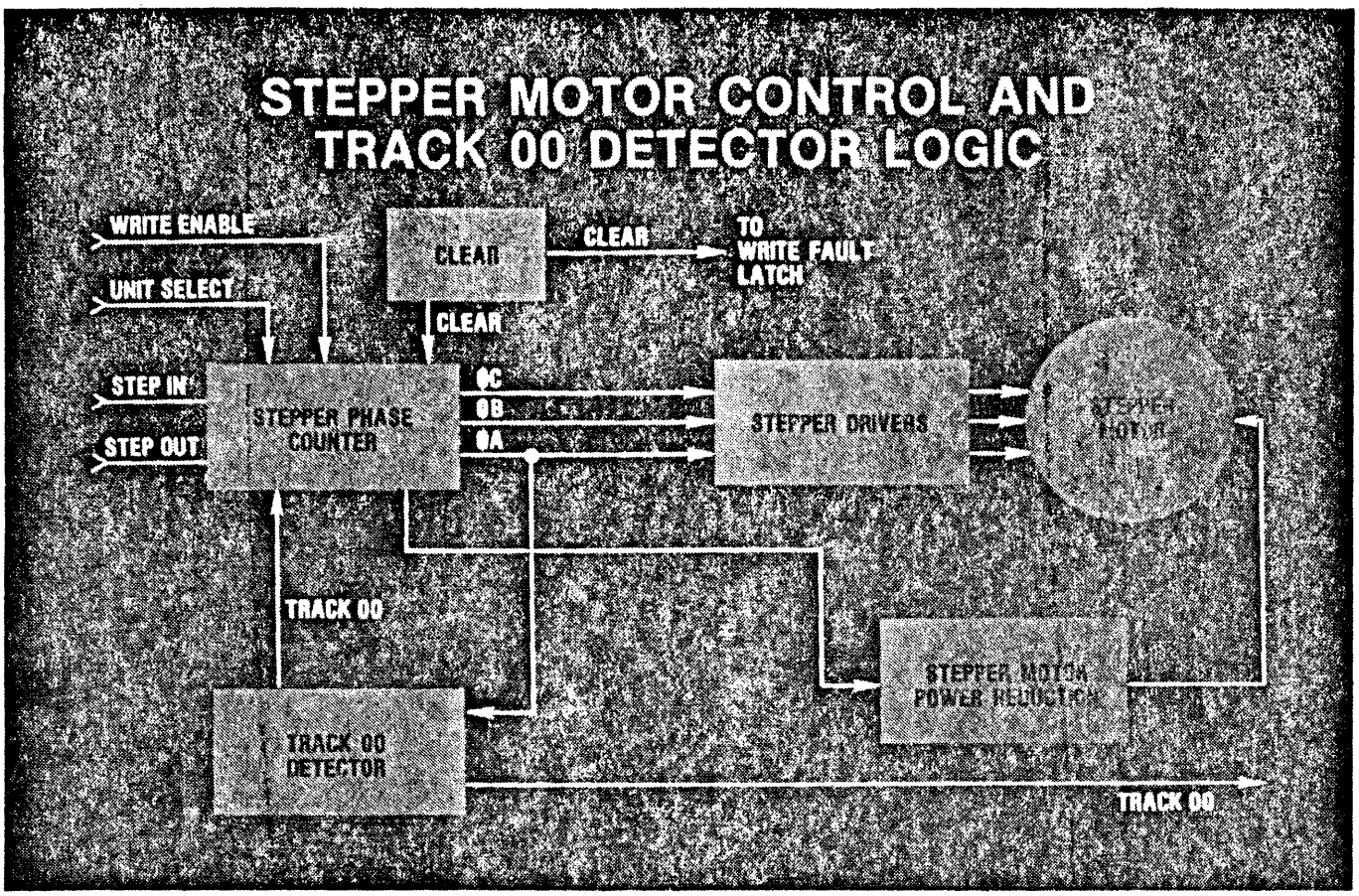


THE FINAL SECTION OF LOGIC TO BE DESCRIBED IN THE BLOCK DIAGRAM IS THE CONTROL LOGIC.

THERE ARE FOUR MAIN SECTIONS WITHIN THE CONTROL LOGIC, STEPPER MOTOR CONTROL; TRACK 00 DETECTION; HEAD LOAD; AND INDEX AND READY.

THE FIRST OF THESE SECTIONS DESCRIBED IS THE STEPPER MOTOR CONTROL AND TRACK 00 DETECTION LOGIC.

53



THE STEPPER MOTOR CONTROL LOGIC CONSISTS OF THE STEPPER PHASE COUNTER WHICH IS INCREMENTED BY THE STEP IN INPUT SIGNAL AND DECREMENTED BY THE STEP OUT INPUT SIGNAL. THE THREE OUTPUTS, PHASE "C", "B" AND "A" DRIVE THE STEPPER MOTOR THROUGH THE STEPPER DRIVERS.

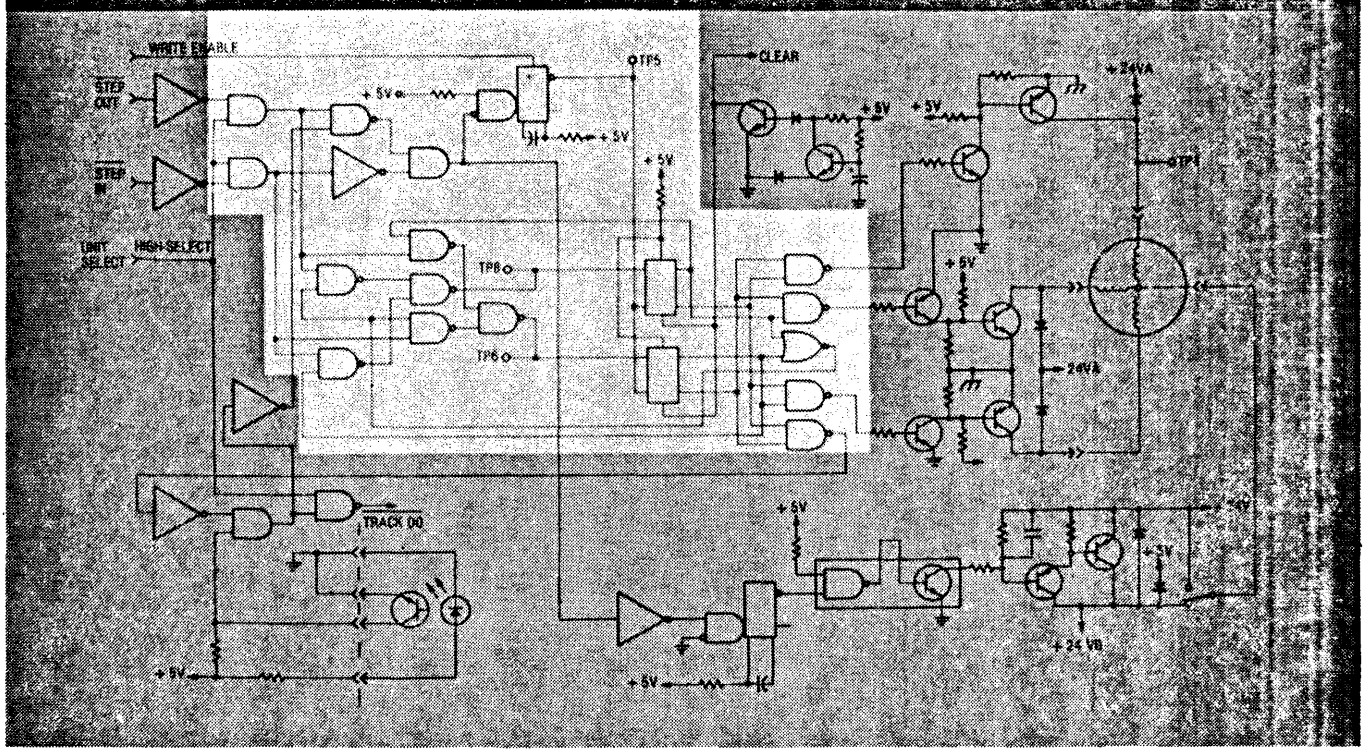
THE STEPPER MOTOR POWER REDUCTION LOGIC REDUCES THE CURRENT SUPPLIED TO THE ACTIVE PHASE WITHIN THE STEPPER MOTOR WHEN THE MOTOR IS NOT MOVING. THE REDUCTION IN CURRENT IS REQUIRED TO PREVENT OVERHEATING. A SMALL CURRENT CONTINUES TO BE SUPPLIED TO THE ACTIVE PHASE IN THE MOTOR WHEN IT IS NOT MOVING TO ELECTRICALLY DETENT THE MOTOR.

THE TRACK 00 DETECTOR DETERMINES THAT THE READ/WRITE HEAD IS AT TRACK

00 USING BOTH THE OPTICAL DETECTOR AND THE PHASE "A" SIGNAL. THE CLEAR LOGIC SHOWN AT THE TOP OF THE DIAGRAM RESETS THE STEPPER PHASE COUNTER ON POWER ON, AND AS MENTIONED IN AN EARLIER PART OF THE LECTURE, THE CLEAR LOGIC ALSO RESETS THE WRITE FAULT LATCH.

54

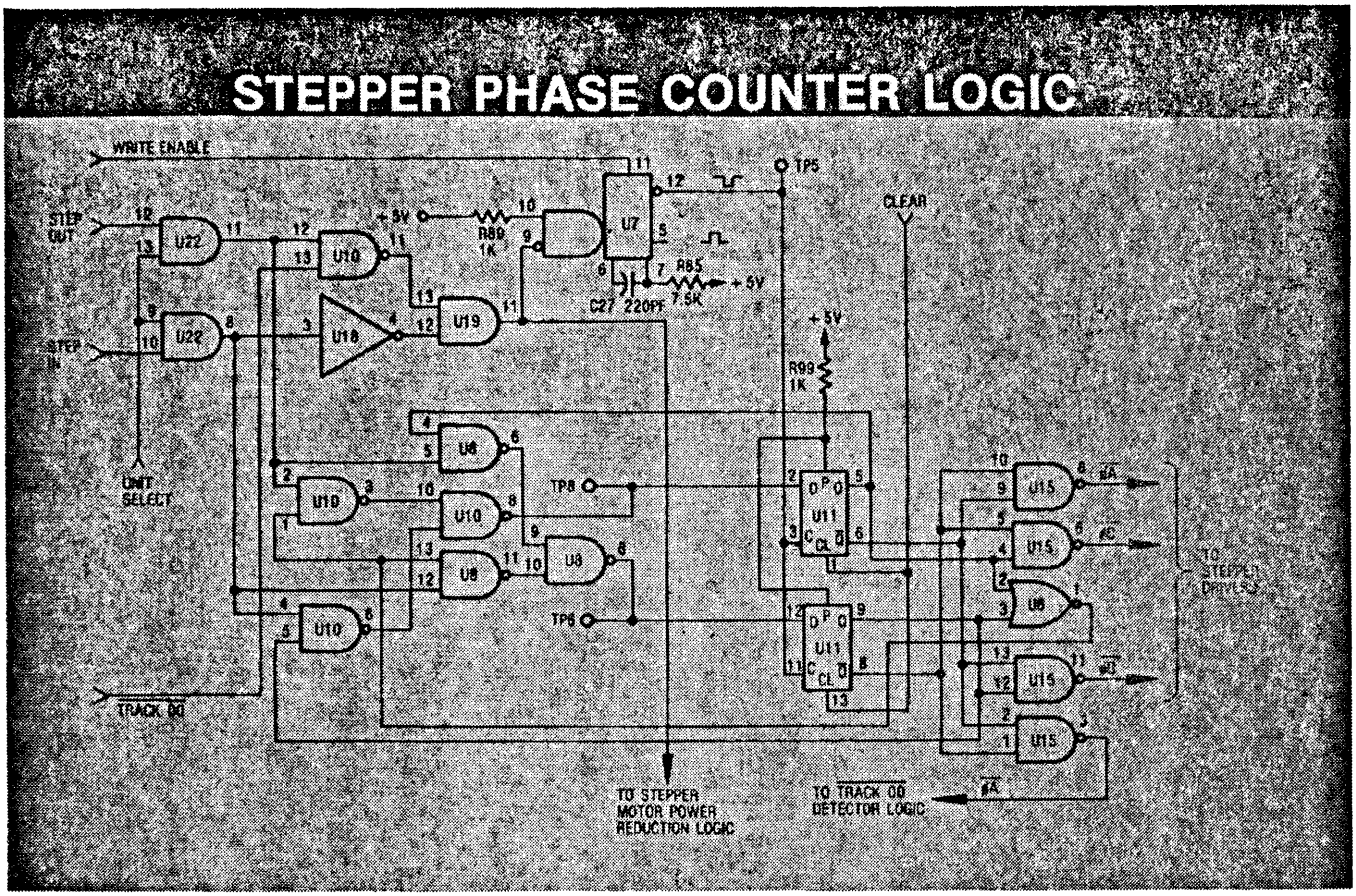
STEPPER PHASE COUNTER LOGIC



THIS DIAGRAM HIGHLIGHTS THE STEPPER PHASE COUNTER LOGIC WHICH SEQUENCES THE ACTIVE PHASES TO THE STEPPER MOTOR ACCORDING TO THE INPUT SIGNALS STEP OUT AND STEP IN.

55

STEPPER PHASE COUNTER LOGIC



THE STEPPER PHASE COUNTER ITSELF CONSISTS OF TWO "D" TYPE FLIP FLOPS, U11, SHOWN CLOSE TO THE CENTER OF THE DIAGRAM. THE OUTPUTS OF THE TWO "D" TYPE FLIP FLOPS ARE DECODED TO GIVE THE THREE PHASES "A", "B" AND "C" BY U15. THE SIGNALS PHASE "A", "B" AND "C" CONTROL THE STEPPER DRIVERS.

THE COUNT OUTPUT FROM THE TWO FLIP FLOPS IS INCREMENTED OR DECREMENTED UNDER THE CONTROL OF THE STEP OUT AND STEP IN SIGNALS, BY THE LOGIC GATING COMPRISING U8 AND U10.

NOTICE THAT THE "D" TYPE FLIP FLOPS ARE CLOCKED ON THE "C" INPUT BY THE RESET OUTPUT OF A RETRIGGERABLE ONE SHOT MULTIVIBRATOR, U7 SHOWN TOP CENTER. THE "D" TYPE FLIP FLOPS ARE CLOCKED BY THE POSITIVE GOING EDGE

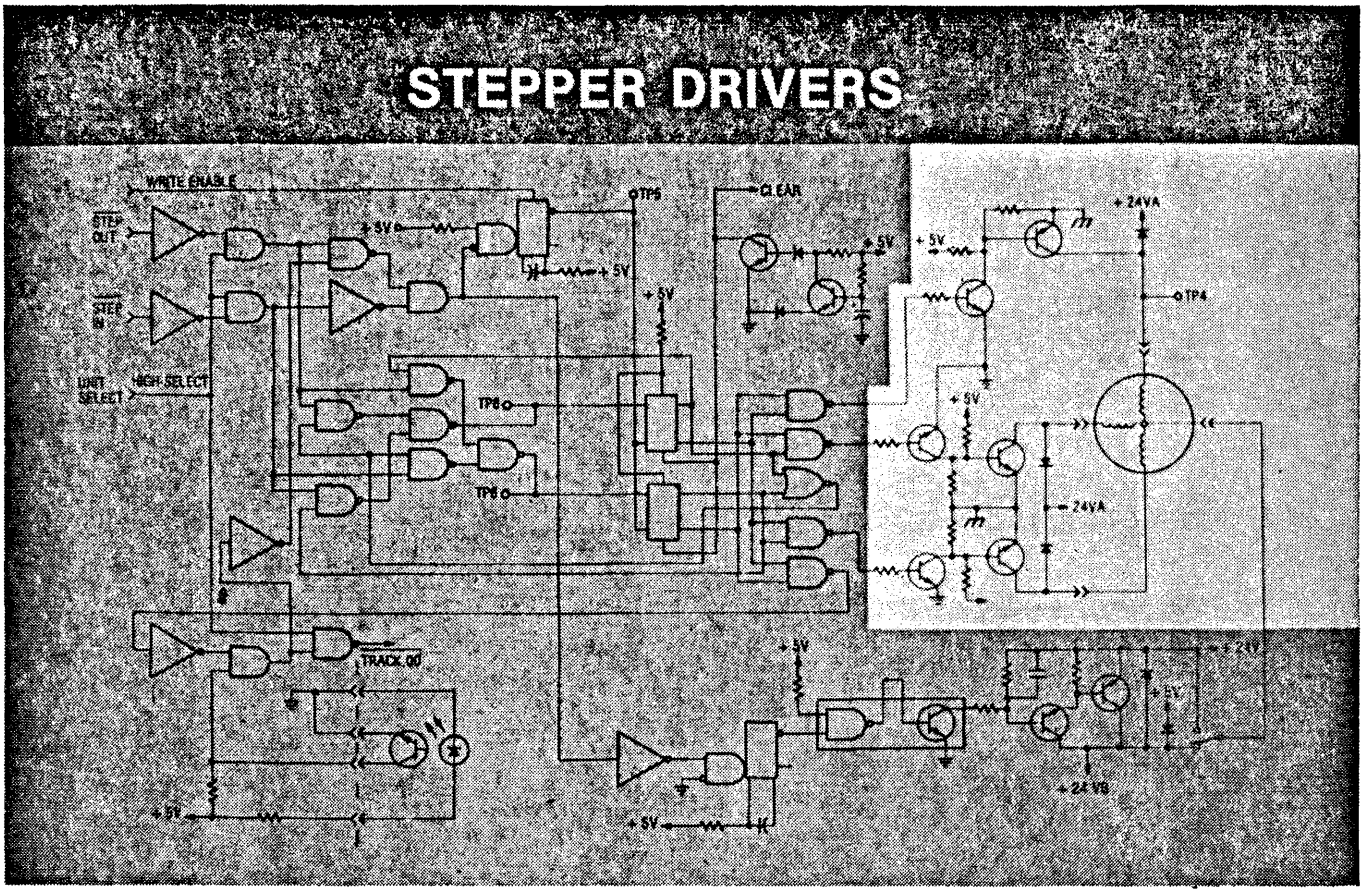
OF THE CLOCK SIGNAL. THIS ACTION DELAYS THE CLOCK SIGNAL BY 0.6 MICROSECONDS FROM THE ACTUAL STEP COMMAND TO ALLOW TIME FOR THE INPUTS TO THE "D" TYPE FLIP FLOPS TO BE CORRECTLY CONDITIONED BY THE INPUT LOGIC. THE STEP COMMAND SIGNALS HAVE A MINIMUM DURATION OF 1 MICROSECOND TO ENSURE CORRECT OPERATION.

GATING STEP OUT AND STEP IN WITH UNIT SELECT IN U22 ENSURES THAT ONLY THE STEPPER LOGIC IN THE SELECTED UNIT IS ACTIVATED.

THE TRACK 00/ SIGNAL IS GATED IN THE ELEMENT OF U10 SHOWN TOWARDS THE TOP LEFT OF THE DRAWING, TO DISABLE FURTHER STEP OUT COMMANDS ONCE THE READ/WRITE HEAD HAS REACHED TRACK 00.

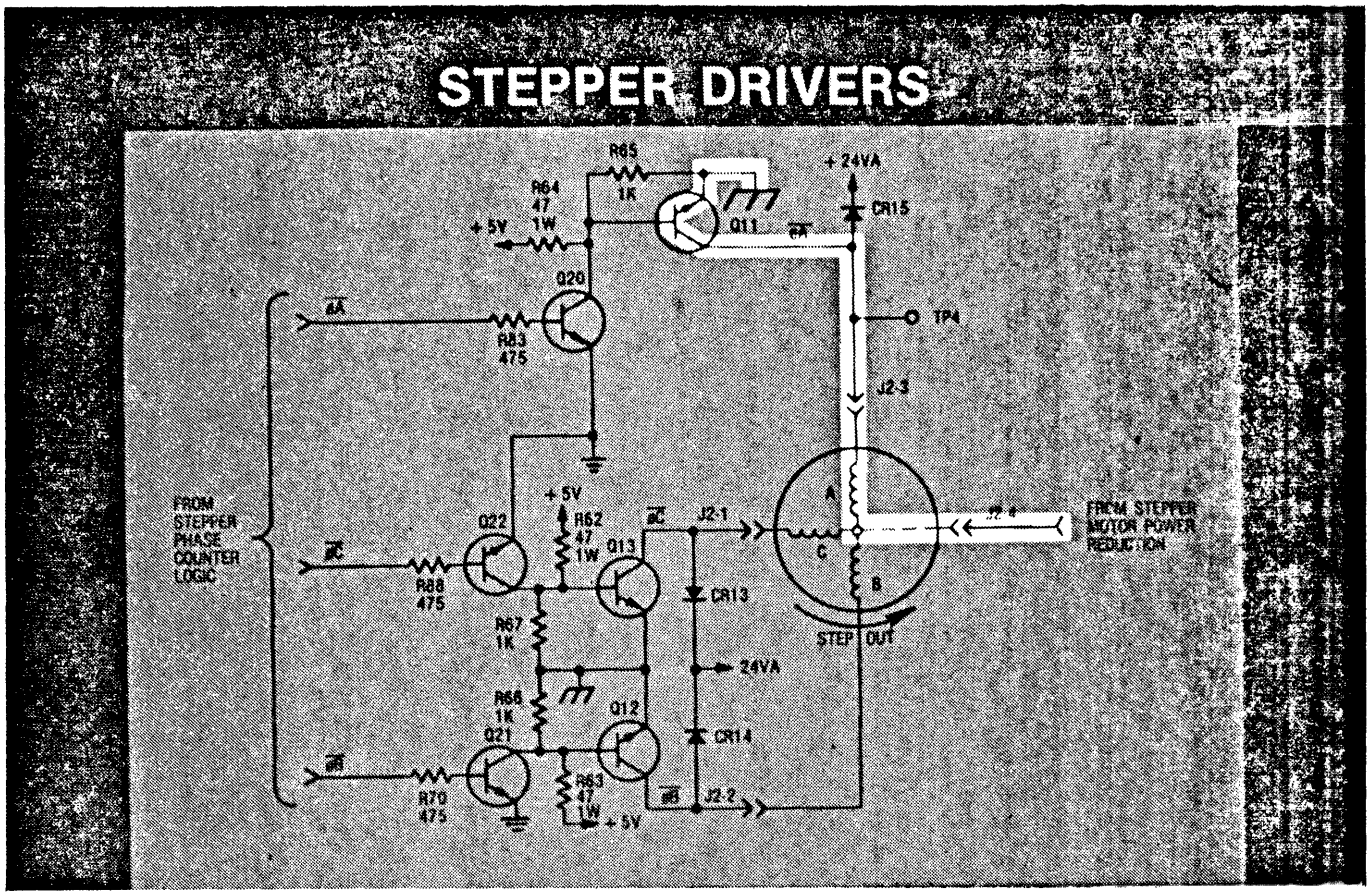
56

STEPPER DRIVERS



THE THREE STEPPER DRIVERS, HIGHLIGHTED IN THIS DRAWING WITH THE STEPPER MOTOR ITSELF, DRIVE EACH OF THE THREE STEPPER MOTOR PHASE WINDINGS IN SEQUENCE BY PROVIDING A CURRENT RETURN TO GROUND.

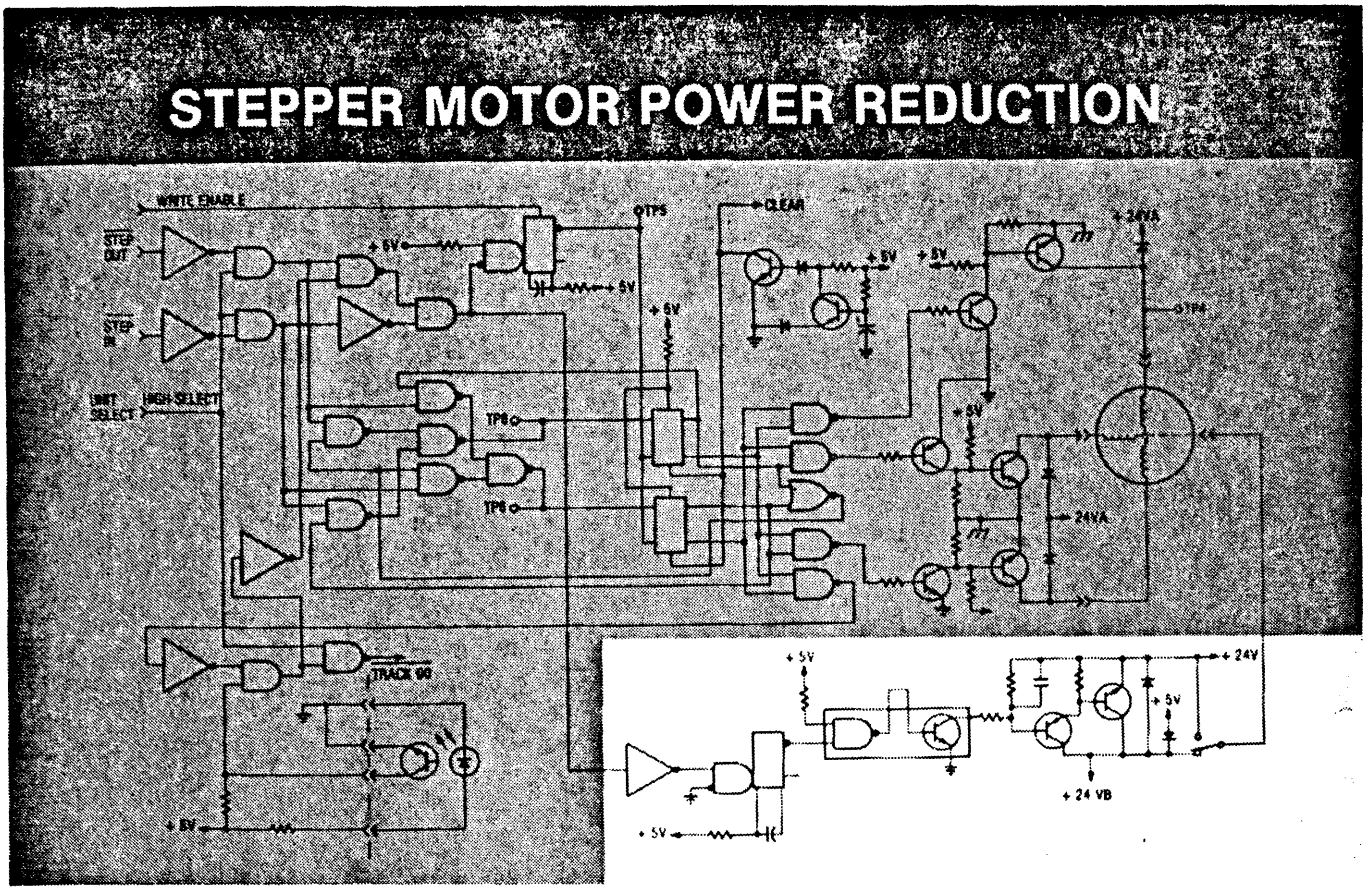
57



EACH OF THE THREE DRIVER CIRCUITS IS IDENTICAL, CONSISTING OF A PAIR OF TRANSISTORS. FOR EXAMPLE, PHASE A/ IS ACTIVE WHEN LOW. THIS SWITCHES Q20 ON WHICH SWITCHES Q11 ON PROVIDING THE CURRENT PATH SHOWN FROM THE CURRENT INPUT VIA THE STEPPER MOTOR POWER REDUCTION CIRCUIT THROUGH THE PHASE "A" MOTOR WINDING TO GROUND.

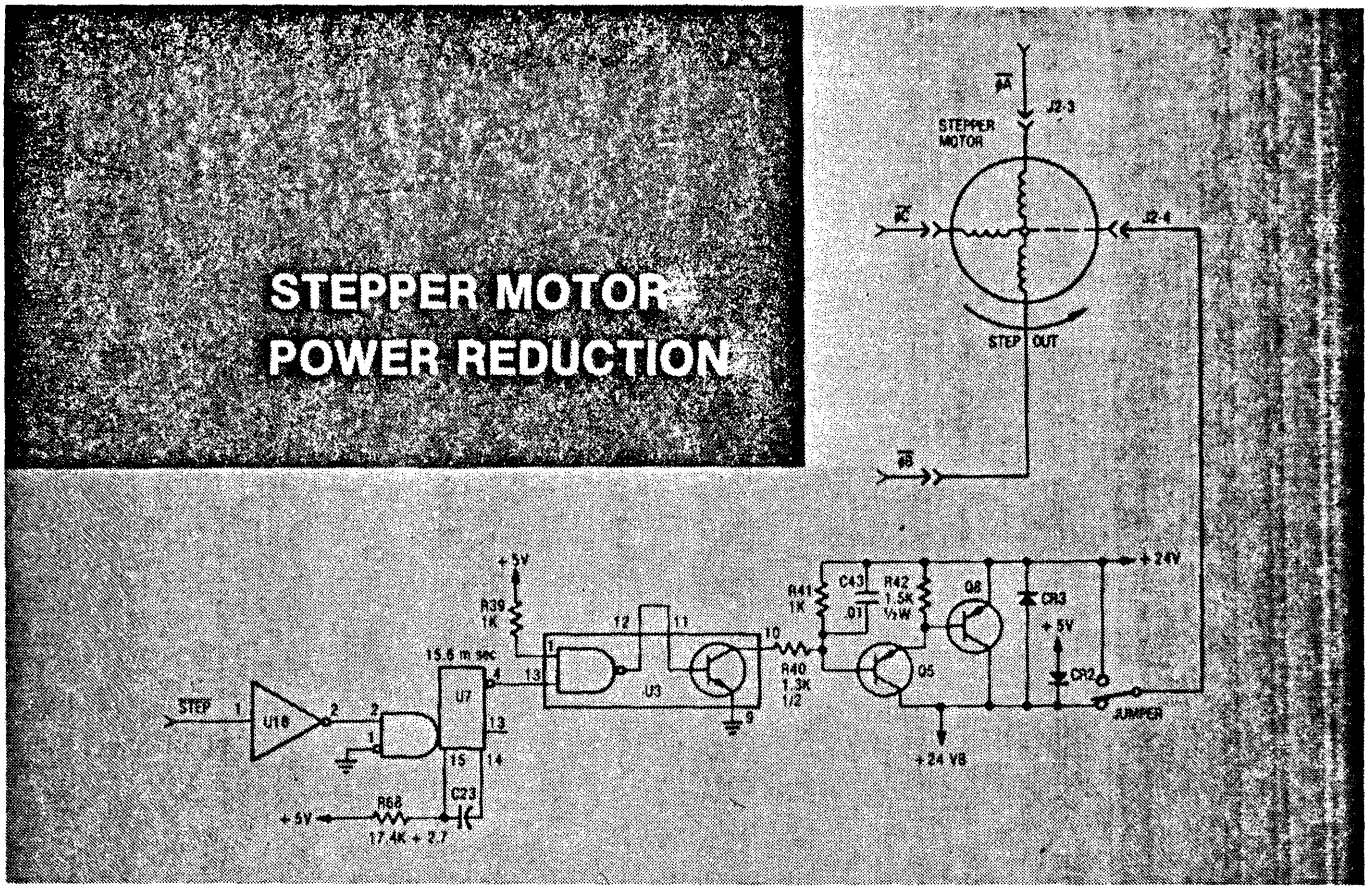
58

STEPPER MOTOR POWER REDUCTION



THE POWER SUPPLIED TO THE STEPPER MOTOR IS CONTROLLED BY THE STEPPER MOTOR POWER REDUCTION LOGIC. AS MENTIONED EARLIER, THE POWER SUPPLIED TO THE MOTOR WHEN IT IS NOT MOVING MUST BE REDUCED TO AVOID OVERHEATING.

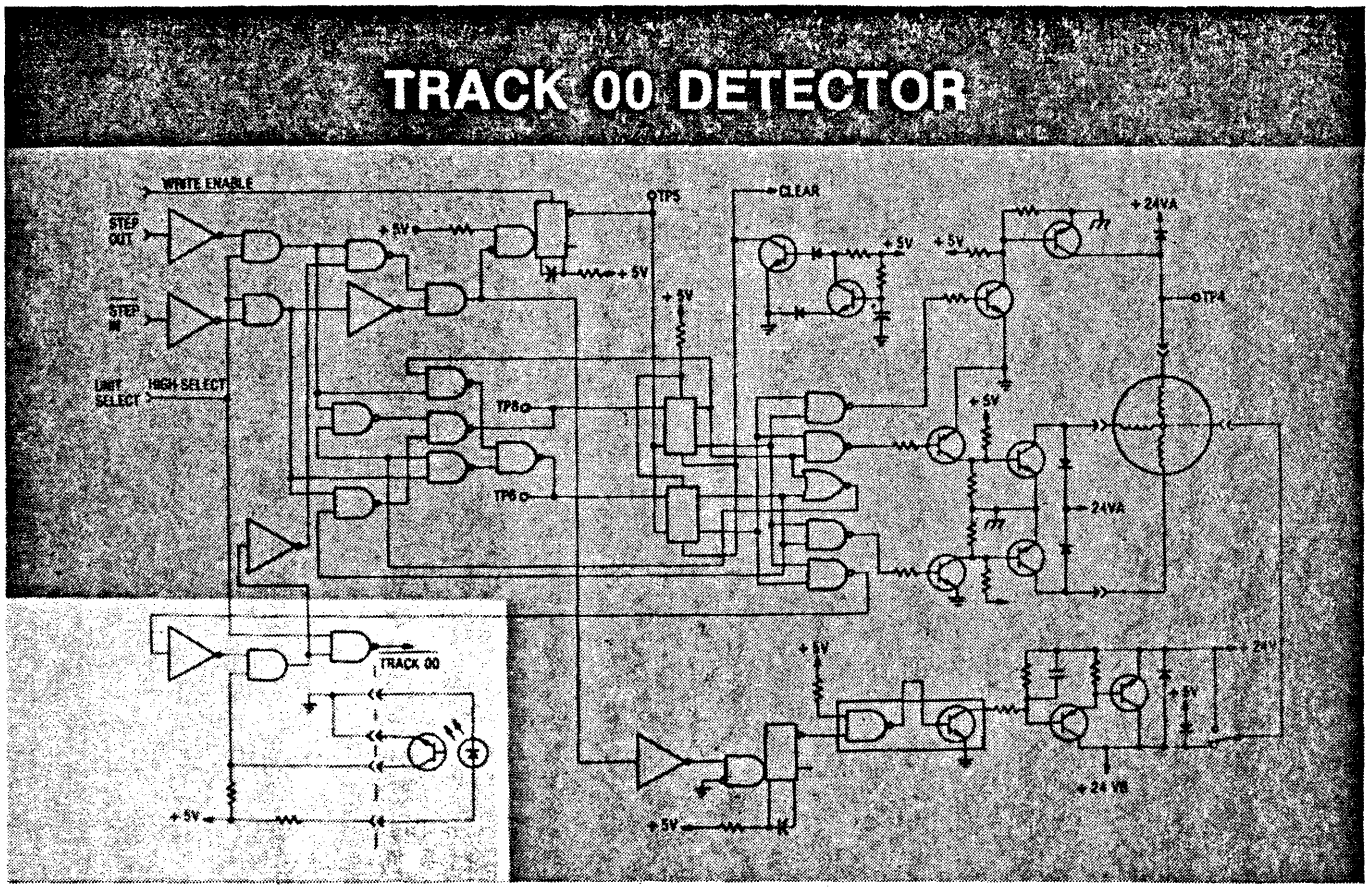
59



WHENEVER A STEP COMMAND IS RECEIVED, THE SIGNAL STEP/ FROM THE STEPPER PHASE COUNTER LOGIC GOES LOW. THROUGH INVERTER U18, THIS TRIGGERS ANOTHER RETRIGGERABLE ONE SHOT MULTIVIBRATOR U7 WHICH PROVIDES A 15.6 MILLISECOND PULSE TO THE DRIVER IC U3. THIS SWITCHES ON THE DARLINGTON PAIR Q5 AND Q8 TO CONNECT THE STEPPER MOTOR TO +24 VOLTS FOR 15.6 MILLISECONDS. AS THE NEXT STEPPER MOTOR PHASE IS SELECTED THE MOTOR SHAFT ROTATES BY ONE STEP OR 15 DEGREES.

IF ADDITIONAL STEP COMMANDS ARE RECEIVED, WITHIN THE 15.6 MILLISECOND TIME PERIOD, THE MULTIVIBRATOR U7 IS RETRIGGERED TO HOLD Q5 AND Q8 ON UNTIL 15.6 MILLISECONDS AFTER THE LAST STEP COMMAND.

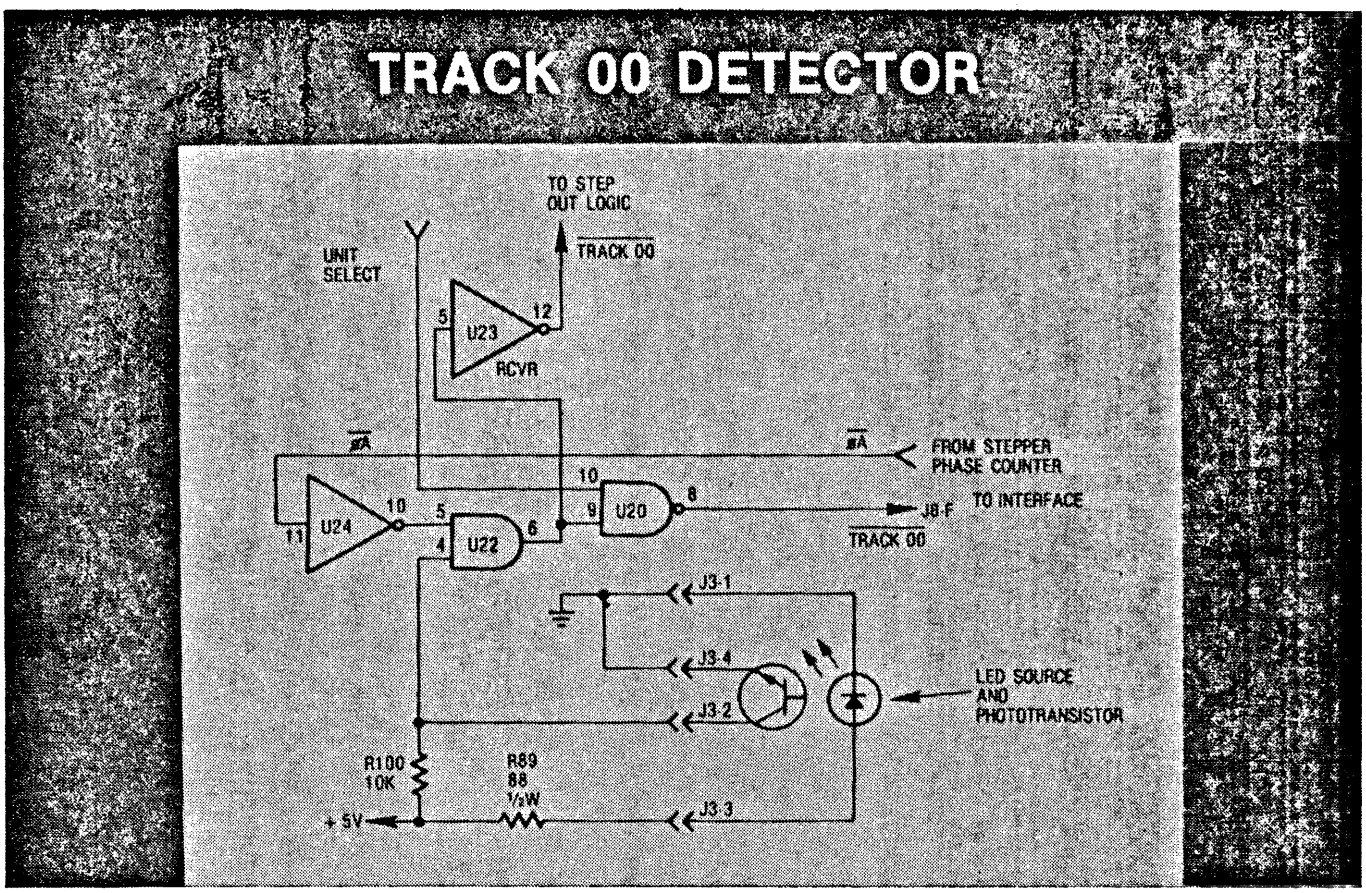
WHEN THE MULTIVIBRATOR TIMES OUT, Q5 AND Q8 TURN OFF TO DISCONNECT THE +24 VOLT SOURCE. A REDUCED CURRENT PATH IS NOW PROVIDED TO THE STEPPER MOTOR FROM THE +5 VOLT SUPPLY THROUGH THE BLOCKING DIODE CR2. THE REDUCED CURRENT ELECTRICALLY DETENTS THE STEPPER MOTOR IN THE ACTIVE PHASE POSITION.



THIS DIAGRAM HIGHLIGHTS THE TRACK 00 DETECTOR LOGIC WHICH ESTABLISHES THAT THE READ/WRITE HEAD IS AT TRACK 00.

61

TRACK 00 DETECTOR

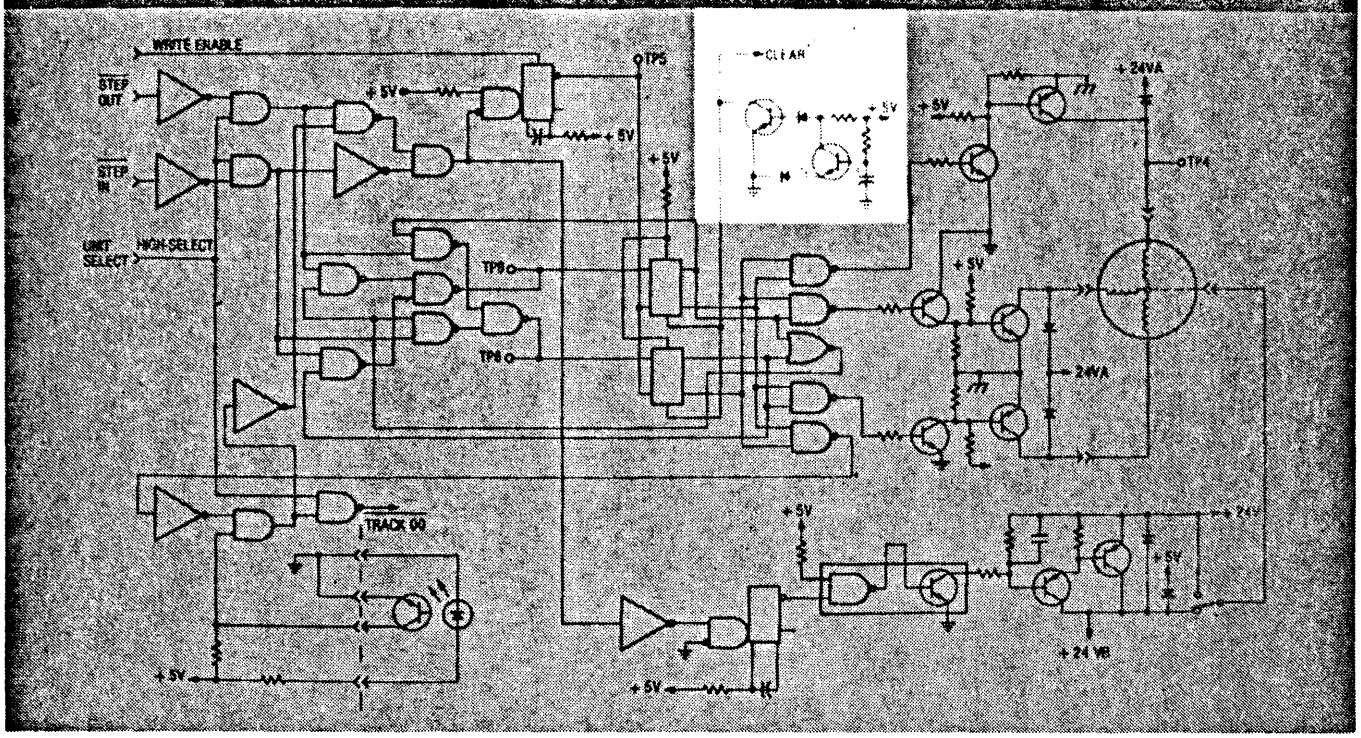


THE BOTTOM RIGHT OF THE DIAGRAM SHOWS THE "LED" LIGHT SOURCE AND PHOTO TRANSISTOR WHICH COMPRISE THE OPTICAL DETECTOR. A METAL TAB ON THE READ/WRITE HEAD CARRIAGE ASSEMBLY INTERRUPTS THE BEAM OF LIGHT WHEN THE READ/WRITE HEAD IS AT TRACK 00.

BECAUSE THE TRACKS ON THE DISKETTE ARE ONLY ONE FIFTIETH OF AN INCH APART, ADJUSTMENT FOR RELIABLE OPERATION OF THIS DETECTOR COULD BE VERY DIFFICULT TO ACHIEVE. TO OVERCOME THIS, THE OUTPUT FROM THE OPTICAL DETECTOR, WHICH MAY BE TRUE FOR MORE THAN TRACK 00, IS GATED WITH PHASE "A" IN U22 TO DETERMINE THE EXACT POSITION OF THE MOTOR AND PROVIDE A RELIABLE REFERENCE.

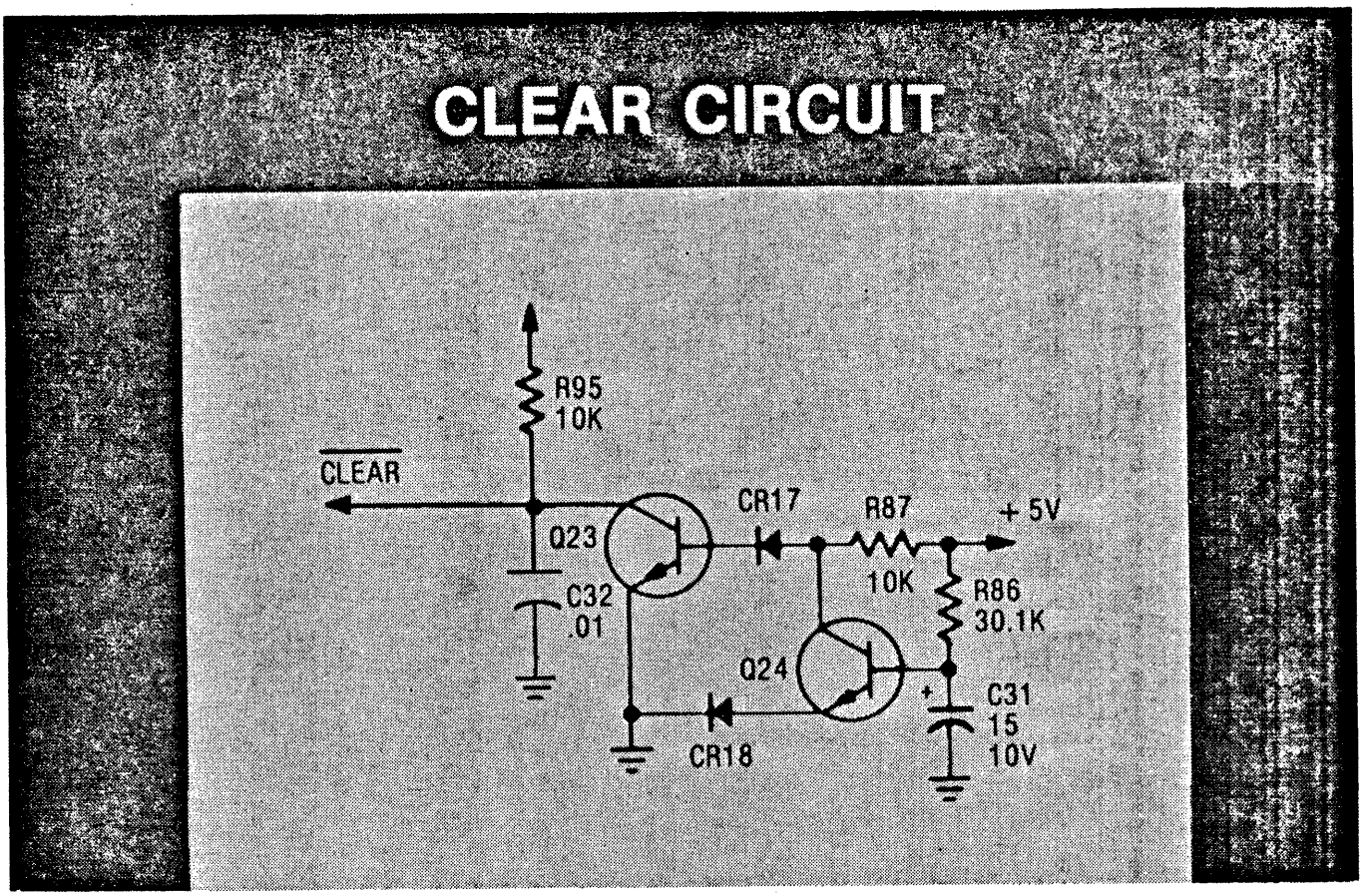
62

CLEAR CIRCUIT



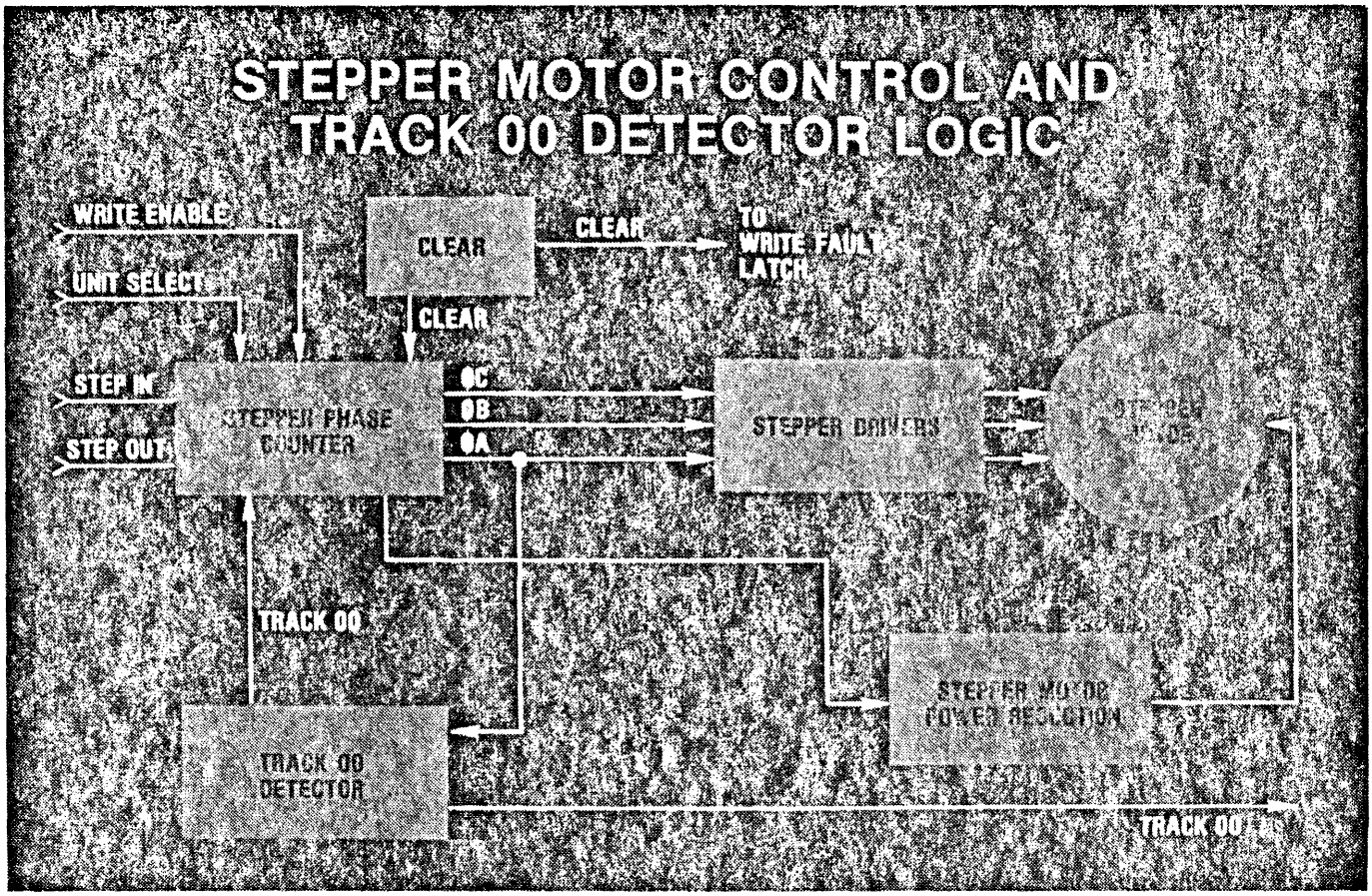
THE LAST PART OF THIS SECTION OF LOGIC IS THE CLEAR CIRCUIT WHICH RESETS THE STEPPER MOTOR PHASE COUNTER AND THE WRITE FAULT LATCH ON POWER ON.

63



AT POWER ON, Q24 IS HELD ON UNTIL CAPICATOR C31 HAS CHARGED THROUGH RESISTOR R86. Q23 IS HELD ON WITH Q24 CAUSING CLEAR/ TO REMAIN LOW UNTIL CAPACITOR C31 HAS CHARGED. CLEAR/ REMAINS LOW FOR APPROXIMATELY 0.1 SECOND AFTER THE +5 VOLT LEVEL IS ESTABLISHED.

64



TO BRIEFLY REVIEW THE STEPPER MOTOR CONTROL AND TRACK 00 DETECTOR LOGIC, THE STEPPER PHASE COUNTER DETERMINES THE ACTIVE STEPPER MOTOR PHASE AND SEQUENCES THE ACTIVE PHASE SIGNAL ACCORDING TO THE CONTROLLING SIGNALS STEP IN AND STEP OUT.

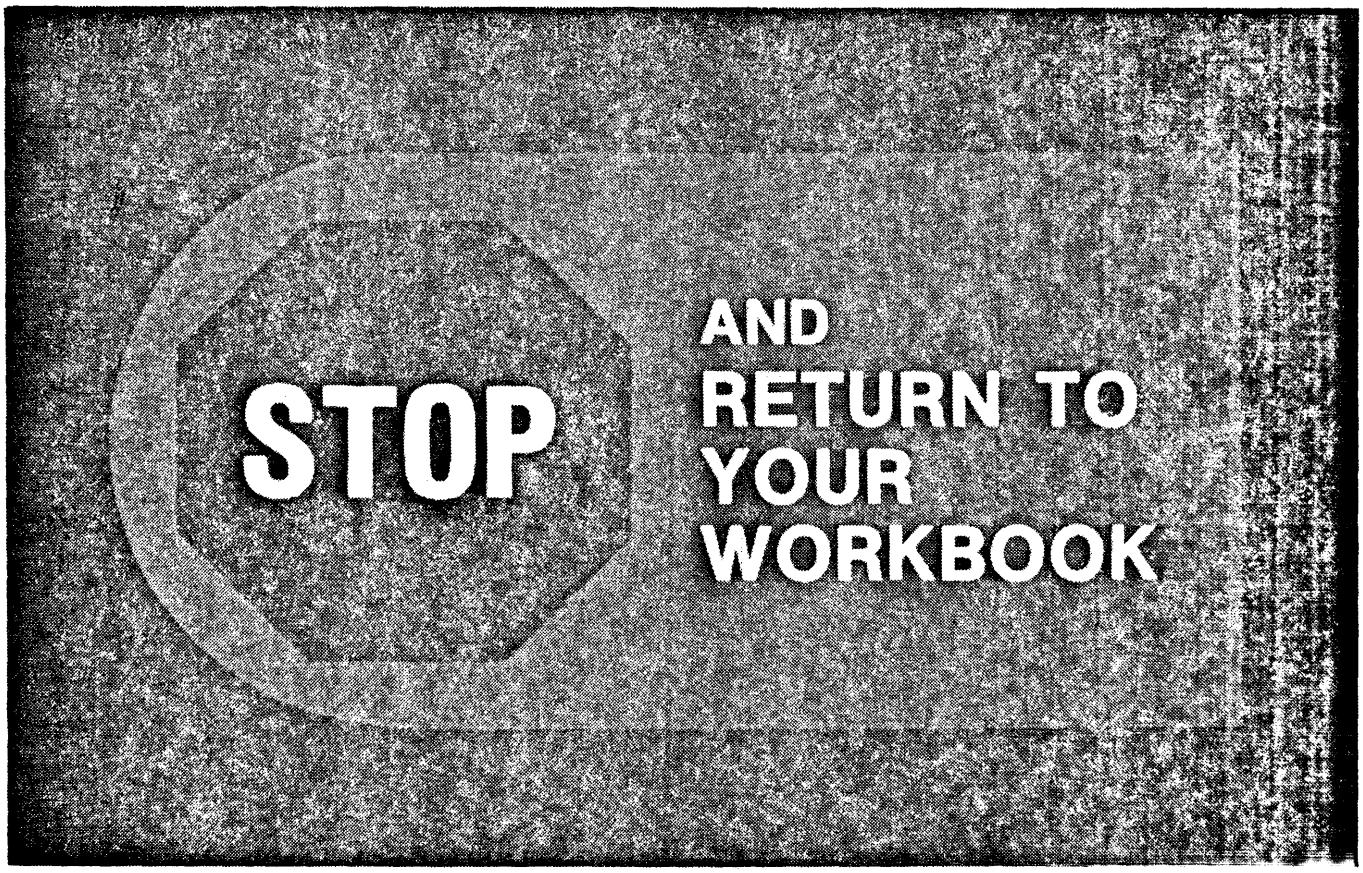
THE THREE STEPPER MOTOR PHASE SIGNALS DRIVE THE STEPPER MOTOR THROUGH THE DRIVER CIRCUIT.

WHEN THE MOTOR IS NOT ACTUALLY MOVING BETWEEN STEP POSITIONS, THE STEPPER MOTOR POWER REDUCTION CIRCUIT REDUCES THE CURRENT SUPPLIED TO THE ACTIVE STEPPER MOTOR PHASE TO PREVENT OVERHEATING. THE REDUCED CURRENT ELECTRICALLY DETENTS THE STEPPER MOTOR IN THE REQUIRED POSITION.

THE TRACK 00 DETECTOR USES THE PHASE "A" SIGNAL FROM THE STEPPER PHASE COUNTER TO DETERMINE THE EXACT LOCATION OF TRACK 00 SINCE PHASE "A" IS ALWAYS ACTIVE FOR TRACK 00 AND THE OPTICAL DETECTOR MAY BE TRUE FOR MORE THAN ONE TRACK POSITION.

THE CLEAR CIRCUIT ENSURES THAT THE STEPPER PHASE COUNTER AND WRITE FAULT LATCH ARE RESET DURING POWER ON AFTER THE POWER SUPPLY LEVELS ARE ESTABLISHED.

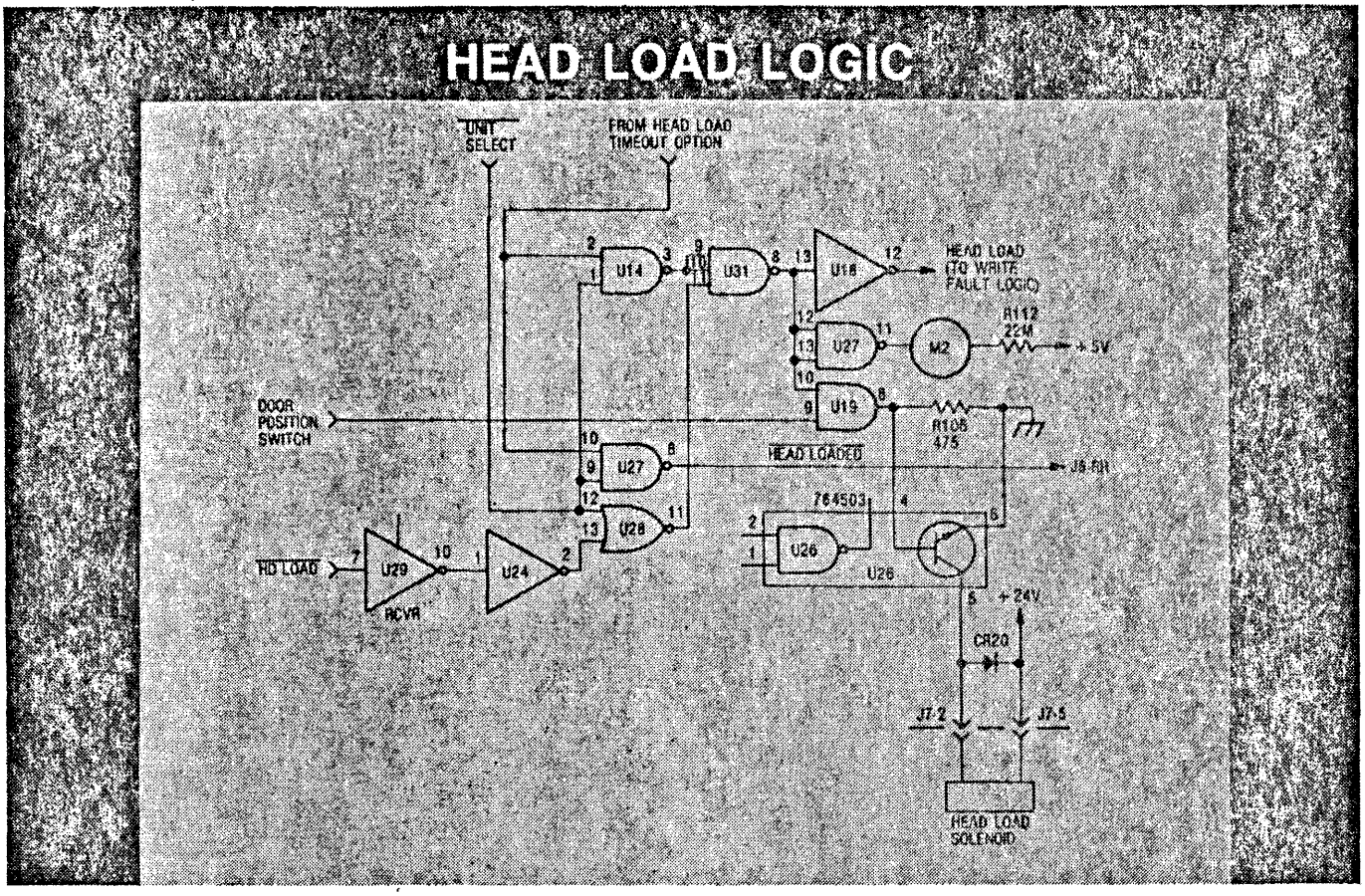
65



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

66

HEAD LOAD LOGIC



CONTINUING WITH THE DESCRIPTION OF THE CONTROL LOGIC, THIS DIAGRAM DETAILS THE HEAD LOAD LOGIC.

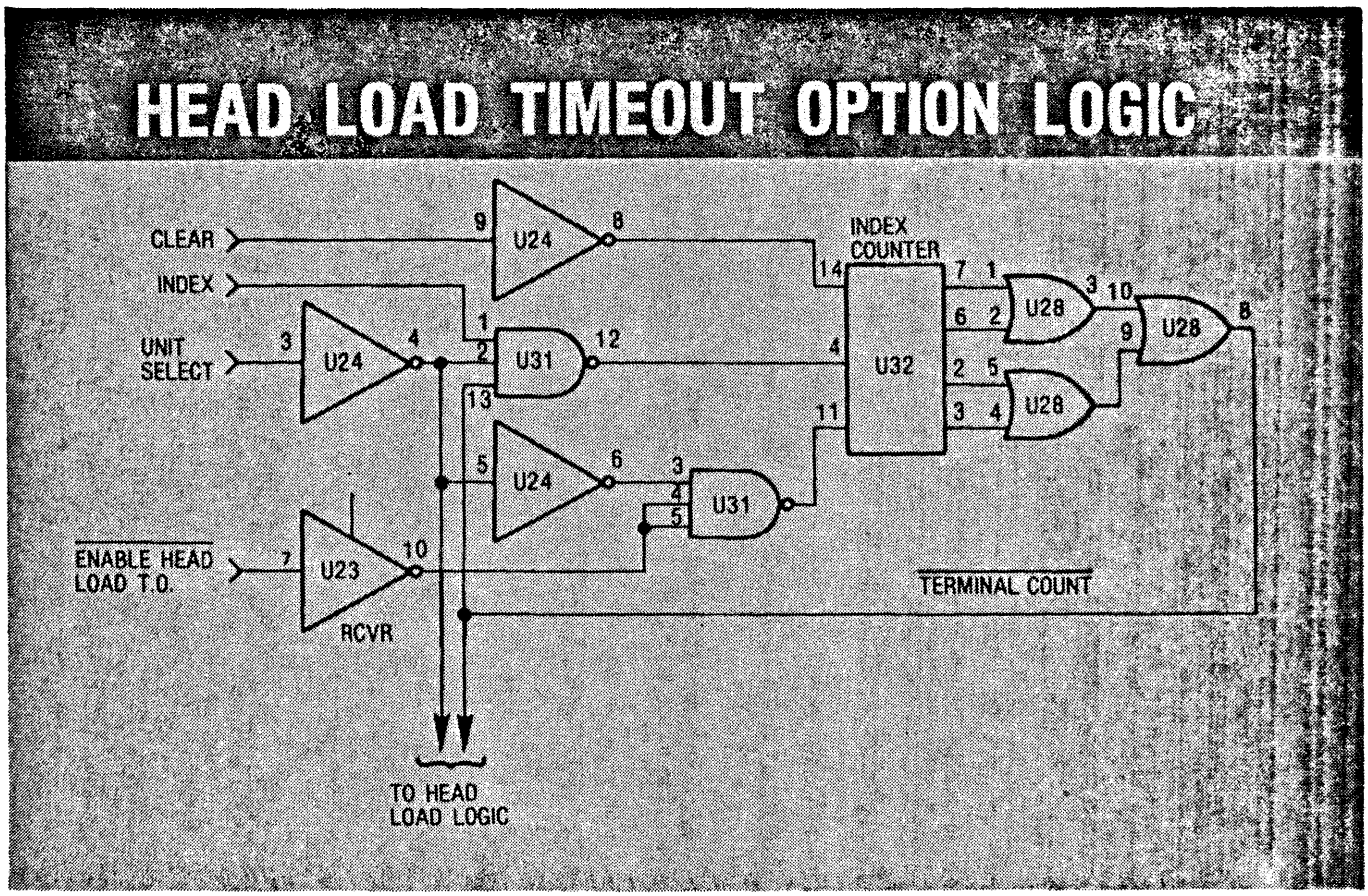
THE HEAD IS LOADED AGAINST THE DISK WHEN THE HEAD LOAD SOLENOID, SHOWN BOTTOM RIGHT, IS ENERGIZED.

TO ENERGIZE THE HEAD LOAD SOLENOID, A LOW LEVEL SIGNAL, HEAD LOAD NOT, IS RECEIVED BY RECEIVER IC U29 FROM THE HOST SYSTEM CONTROLLER. THIS SIGNAL IS INVERTED BY INVERTER U24 AND GATED WITH UNIT SELECT AT "OR" GATE U28. AFTER GATING WITH THE OUTPUT FROM THE DOOR POSITION SWITCH, THE HEAD LOAD SOLENOID IS ENERGIZED BY THE DRIVER IC U26.

THE HEAD LOAD SIGNAL IS ALSO ROUTED TO THE WRITE FAULT LOGIC AS EXPLAINED EARLIER TO DETERMINE POSSIBLE HEAD LOAD ERRORS AND THE ELAPSED TIME METER M2 TO RECORD THE TOTAL NUMBER OF HOURS FOR WHICH THE HEAD IS LOADED.

THE HEAD LOAD SOLENOID CAN BE HELD LOADED BY A SIGNAL FROM THE HEAD LOAD TIMEOUT OPTION LOGIC.

67



THE HEAD LOAD TIMEOUT OPTION IS DESIGNED TO ALLOW THE HEAD TO REMAIN LOADED FOR EIGHT INDEX TIMES, THAT IS DISKETTE REVOLUTIONS, AFTER THE DRIVE HAS BEEN DESELECTED.

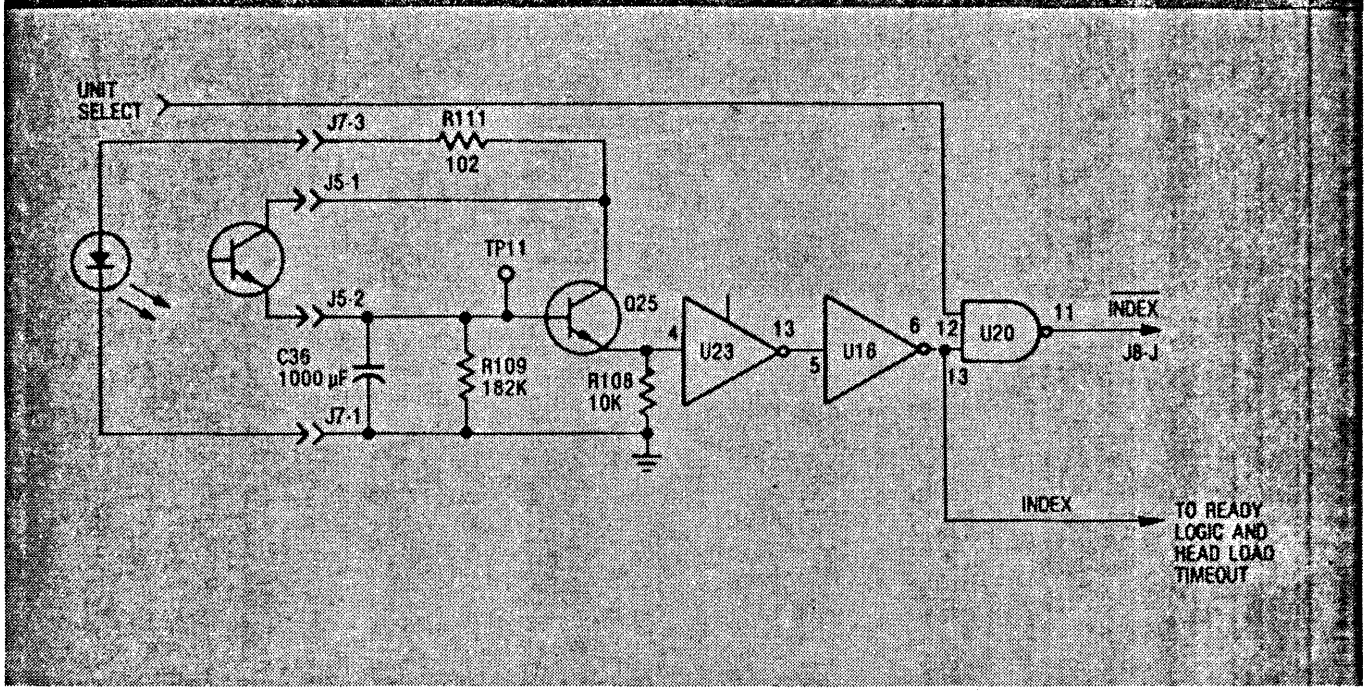
IN ORDER TO UTILIZE THIS FEATURE, THE COMMAND "ENABLE HEAD LOAD TIME-OUT" MUST BE RECEIVED PRIOR TO THE END OF THE "HEAD LOAD" SIGNAL AND THE DRIVE BEING DESELECTED.

THE SIGNAL "ENABLE HEAD LOAD TIMEOUT" IS A LOW GOING PULSE THAT IS USED TO PRESET THE INDEX COUNTER U32 TO SEVEN. THE INDEX COUNTER COUNTS DOWN ONE COUNT FOR EVERY INDEX PULSE AFTER THE UNIT IS DESELECTED.

THE TERMINAL COUNT/ SIGNAL GOES LOW WHEN THE COUNT REACHES ZERO TO DE-ENERGIZE THE HEAD LOAD SOLENOID.

68

INDEX CIRCUIT

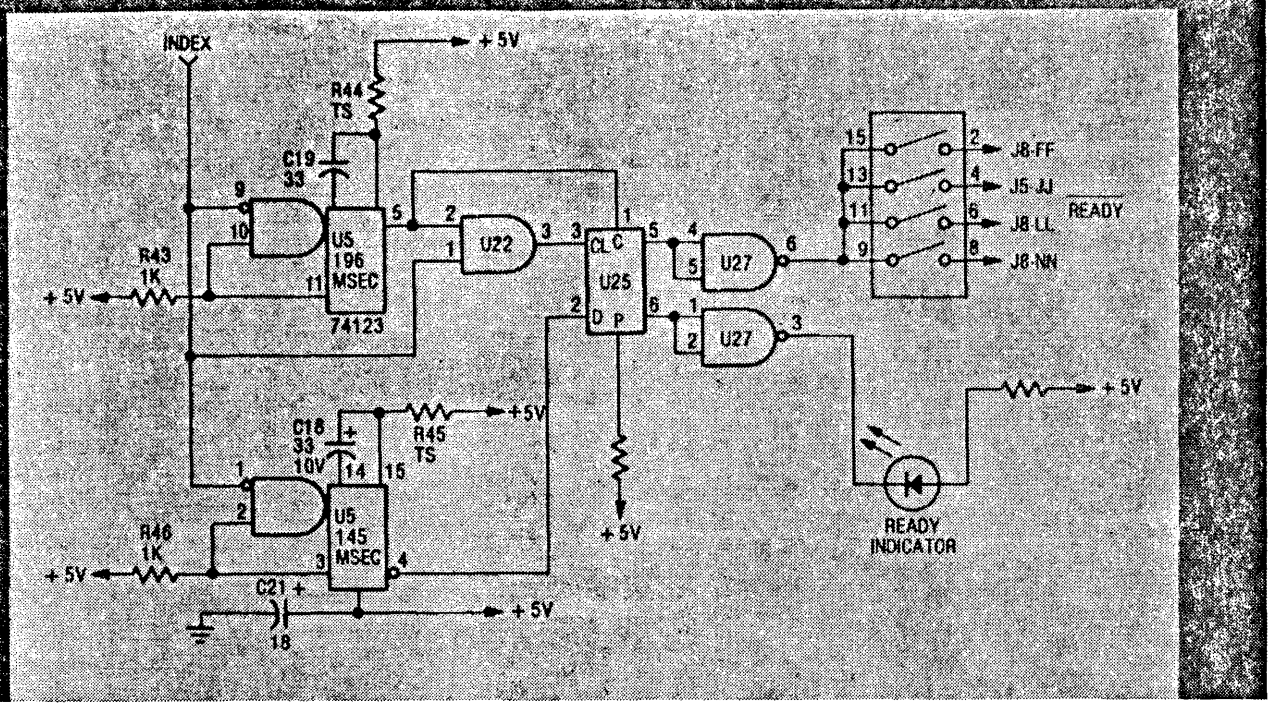


THE INDEX CIRCUIT USES AN "LED" LIGHT SOURCE AND PHOTO TRANSISTOR TO PRODUCE THE INDEX PULSE. INDEX IS ONLY RETURNED TO THE CONTROLLER WHEN THE UNIT IS SELECTED.

THE INDEX PULSE, WHICH IS NOMINALLY A 1.5 MILLISECOND PULSE EVERY 169 MILLISECONDS, IS ALSO ROUTED TO THE HEAD LOAD TIMEOUT LOGIC, PREVIOUSLY DESCRIBED, AND THE READY CIRCUIT.

69

READY CIRCUIT



THE READY CIRCUIT GENERATES A READY STATUS SIGNAL TO THE CONTROLLER WHEN THE DISKETTE IS ROTATING AT THE CORRECT SPEED. THIS SPEED IS 360 RPM PLUS OR MINUS 15%.

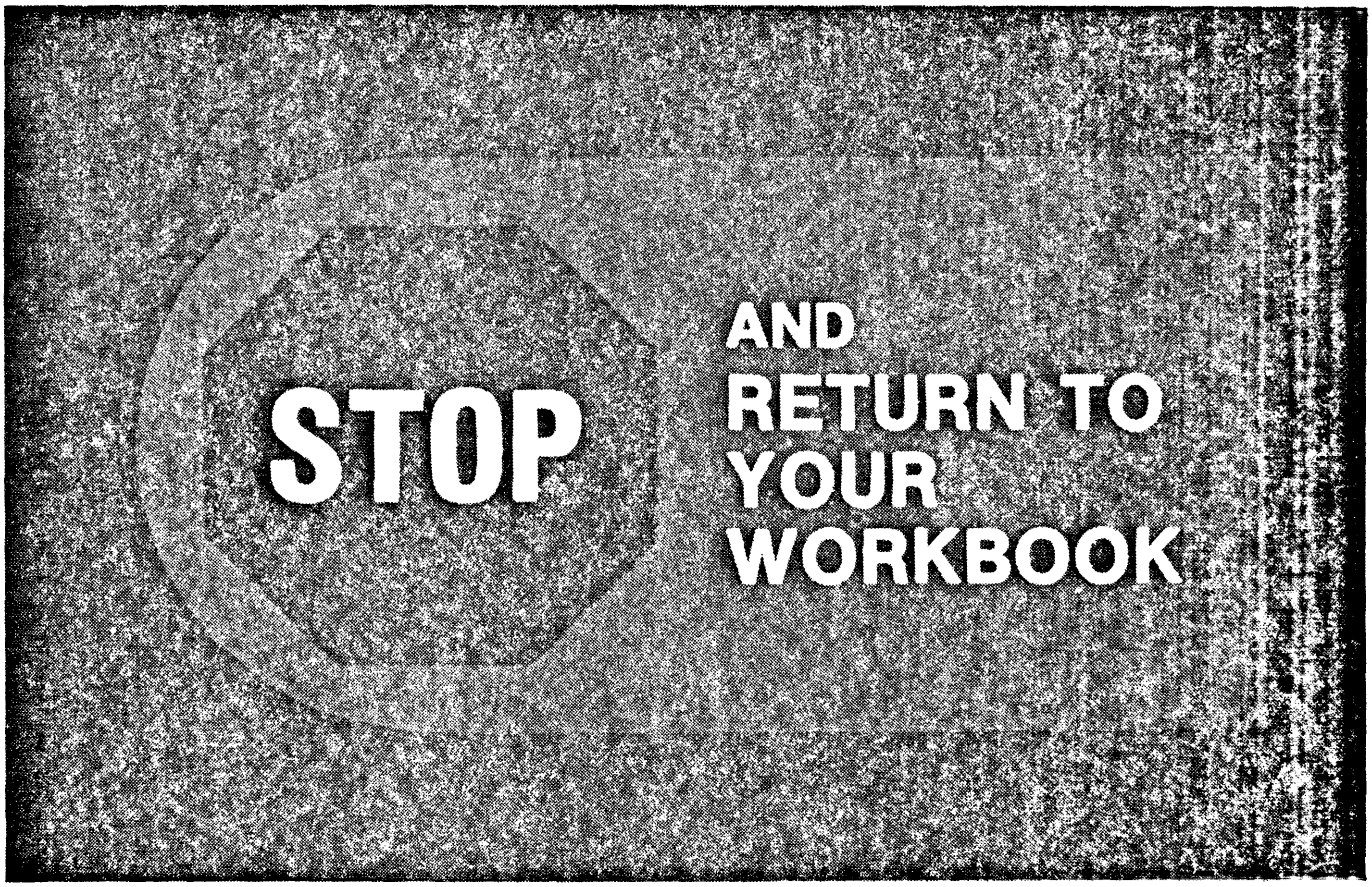
THE MAIN ELEMENTS OF THE CIRCUIT ARE TWO RETRIGGERABLE ONE SHOT MULTIVIBRATORS, BOTH PART OF U5, AND A "D" TYPE FLIP FLOP U25.

THE TIMING OF THE TWO ONE SHOT MULTIVIBRATORS IS SET UP SO THAT WHEN THE DISK SPEED IS WITHIN THE NORMAL LIMITS, THE LOW SPEED ONE SHOT SHOWN AT THE BOTTOM OF THE DIAGRAM ALWAYS TIMES OUT AND THE HIGH SPEED ONE SHOT ABOVE NEVER TIMES OUT.

THE TIMING OF THE TWO ONE SHOTS IS DETERMINED BY THE VALUES OF TEST SELECTED RESISTORS. R45 IS SELECTED TO GIVE 145 MILLISECONDS FOR THE LOW SPEED AND RESISTOR R44 IS SELECTED TO GIVE 196 MILLISECONDS FOR THE HIGH SPEED.

IF THE SPEED IS ABOVE OR BELOW THE SPECIFIED LEVEL, FLIP FLOP U25 IS RESET TO INDICATE THAT THE UNIT IS NOT READY.

70

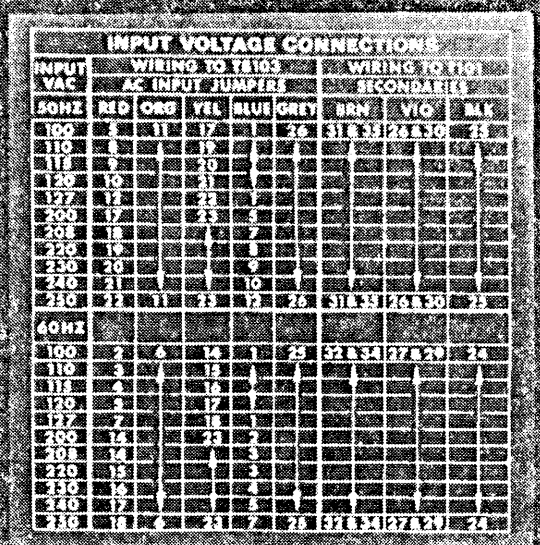


STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

71

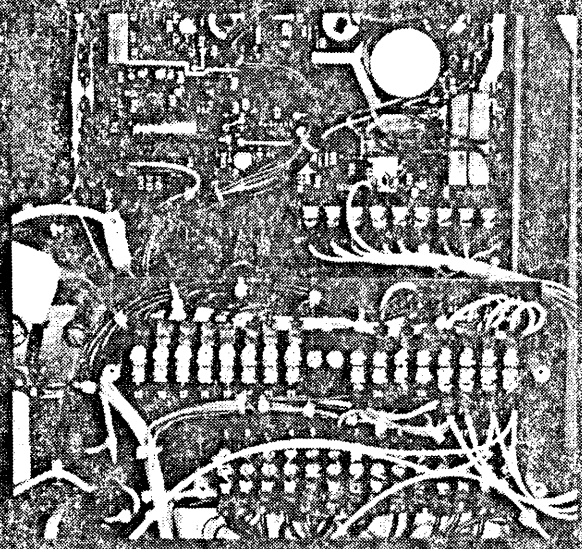
B9489 ICMD POWER SUPPLY

SUPPLIES: • +5V Regulated • +24V Unregulated
• −12V Regulated • 120VAC



INPUT VOLTAGE CONNECTIONS

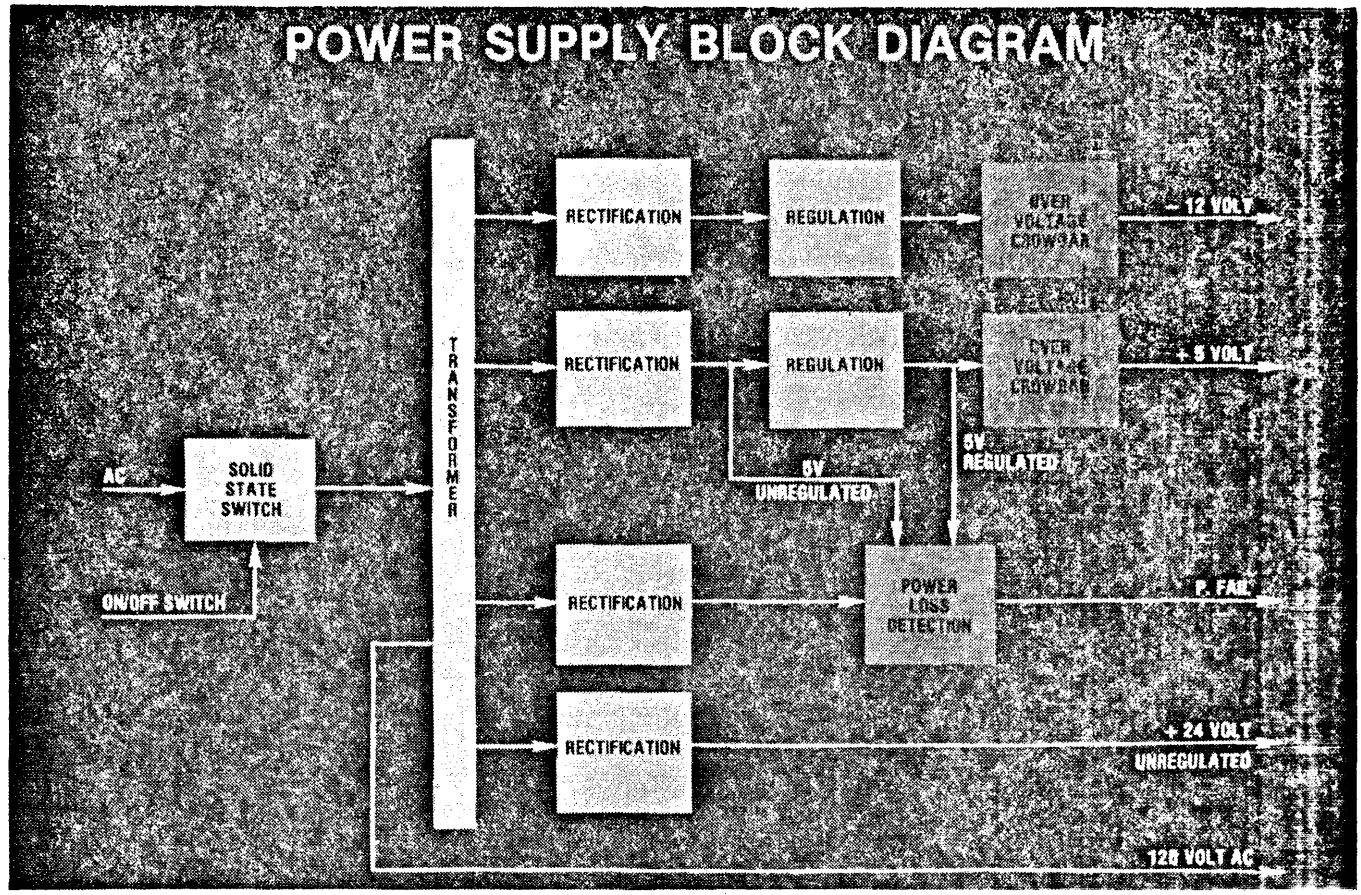
INPUT VAC	WIRING TO T1 J3 AC INPUT JUMPERS					WIRING TO T1 J2 SECONDARY		
50HZ	RED	ORG	YEL	BLUE	GREY	BRN	V/O	BLK
100			1	17		31	33	34 & 30
110				18				
115				20				
120	10			21				
127	11			22				
200	17			25	4			
208	18				7			
220	19				8			
230	20				9			
240	21				10			
250	22	1	23	7	26	31 & 33	34 & 30	29
60HZ								
100	2	6	14	1	25	32 & 34	27 & 29	26
110	3		15					
115	4		16					
120	5		17					
127	7		18					
200	14		23	2				
208	14			3				
220	15			5				
230	16			6				
240	17			8				
250	18	2	24	9	25	32 & 34	27 & 29	26



BOTH FREESTANDING CABINET VERSIONS OF THE B 9489 USE VERY SIMILAR POWER SUPPLIES TO PROVIDE +5 VOLT REGULATED, −12 VOLT REGULATED AND +24 VOLT UNREGULATED DC VOLTAGES TO THE ICMD LOGIC. 120 VOLT AC IS SUPPLIED FOR THE DISKETTE DRIVE MOTOR.

CONVERSION FOR OPERATION AT 50 OR 60 HERTZ AND THE APPROPRIATE LINE VOLTAGE IS MADE BY CHANGING JUMPERS. THIS PROCEDURE IS REFERRED TO AGAIN IN A LATER LECTURE DESCRIBING INSTALLATION.

72



THIS BLOCK DIAGRAM REPRESENTS THE COMPLETE POWER SUPPLY WHICH IS ALMOST IDENTICAL IN BOTH THE 30" AND 44" CABINET VERSIONS.

THE SOLID STATE SWITCH, TO THE LEFT OF THE DIAGRAM, IS CONTROLLED BY THE ON/OFF SWITCH ON THE FRONT OF THE UNIT.

THE SOLID STATE SWITCH APPLIES LINE VOLTAGE TO THE PRIMARY OF THE TRANSFORMER. THIS TRANSFORMER PRODUCES FOUR SECONDARY VOLTAGES AND HAS A TAP TO PROVIDE 120V AC FOR THE DISK DRIVE MOTORS. EACH OF THE FOUR SECONDARY AC VOLTAGES ARE THEN RECTIFIED.

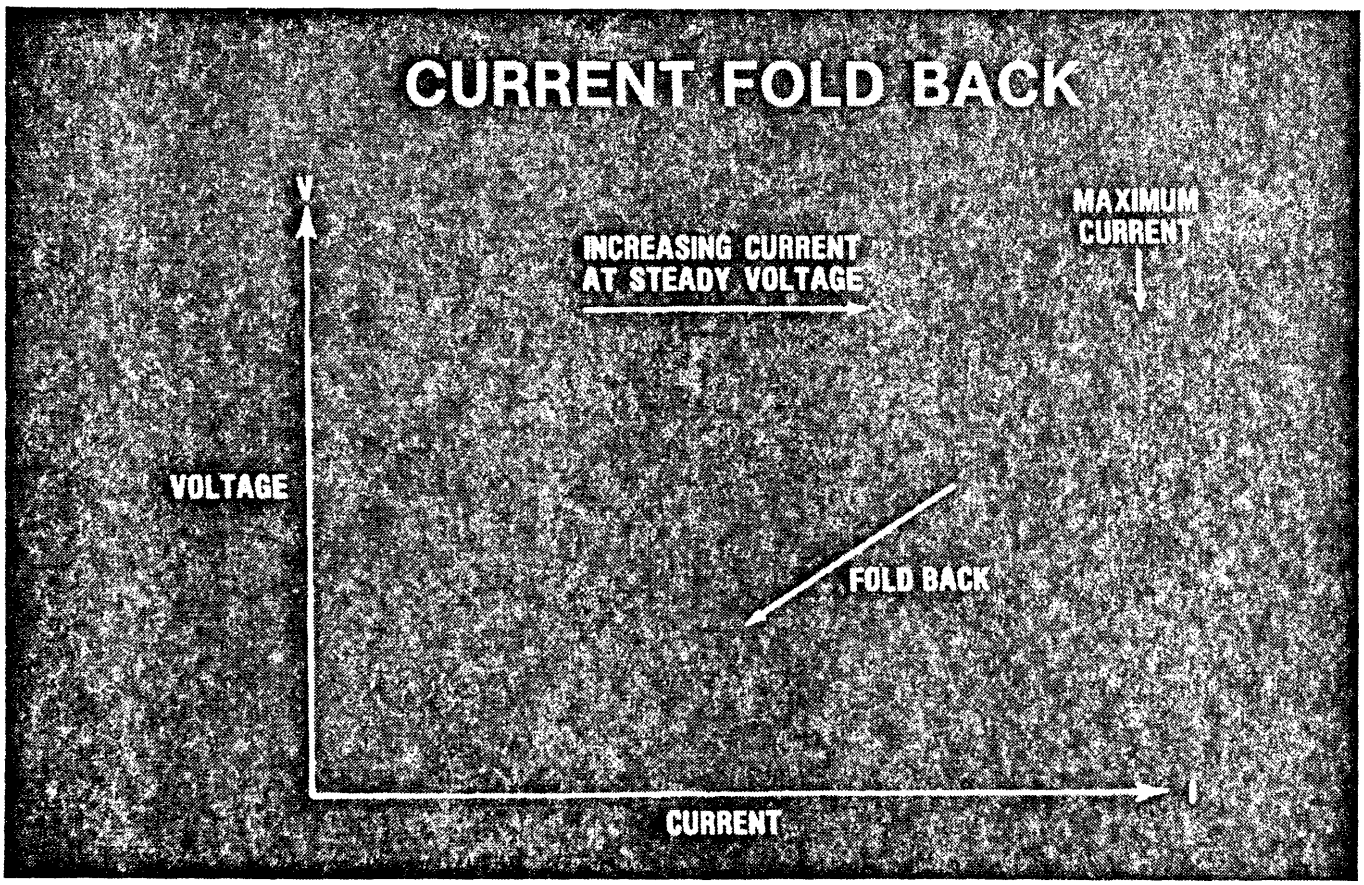
THE –12 VOLT AND THE +5 VOLT SUPPLIES ARE VOLTAGE CONTROLLED BY A REG-

ULATOR CIRCUIT WITH BUILT IN OVER CURRENT PROTECTION AND A CROWBAR CIRCUIT TO PROVIDE OVER VOLTAGE PROTECTION.

BOTH THE 5V UNREGULATED AND THE 5V REGULATED SUPPLIES ARE USED BY A CIRCUIT WHICH DETECTS AN UNDERVOLTAGE CONDITION FROM THE TRANSFORMER, AS IN THE CASE OF A POWER OFF, TO PRODUCE THE LOGIC SIGNAL "PFAIL," POWER FAILURE, USED ON THE OPTIONAL DRIVER RECEIVER AND ADAPTOR PCB'S.

THE +24 VOLT SUPPLY IS UNREGULATED.

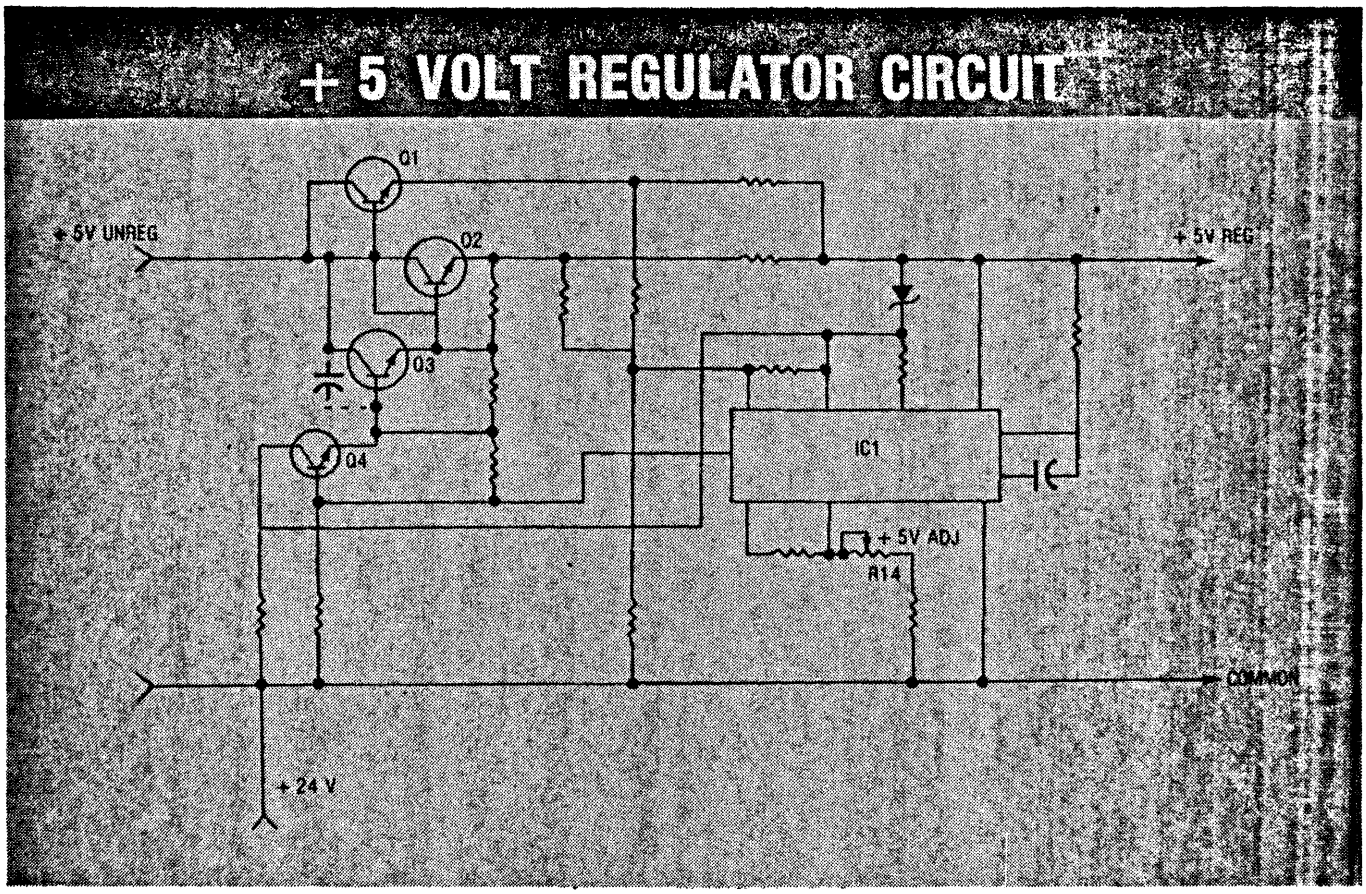
73



THE DESIGN OF THE REGULATOR CIRCUITS FOR THE −12 VOLT AND +5 VOLT REGULATORS IS SIMILAR, BOTH REGULATORS INCORPORATING CURRENT FOLD BACK. CURRENT FOLD BACK REDUCES THE AMOUNT OF CURRENT SUPPLIED IN AN OVER-

LOAD CONDITION AND EFFECTIVELY SHUTS DOWN THE POWER SUPPLY. THIS DIAGRAM SHOWS THE EFFECT OF CURRENT FOLD BACK. THE AMOUNT OF CURRENT SUPPLIED INCREASES AT A STEADY VOLTAGE AS THE DEMAND INCREASES UNTIL A SAFE MAXIMUM CURRENT IS REACHED. IF THIS LIMIT IS PASSED, THE SUPPLY OF CURRENT IS REDUCED UNTIL THE SUPPLY IS EFFECTIVELY SHUT DOWN.

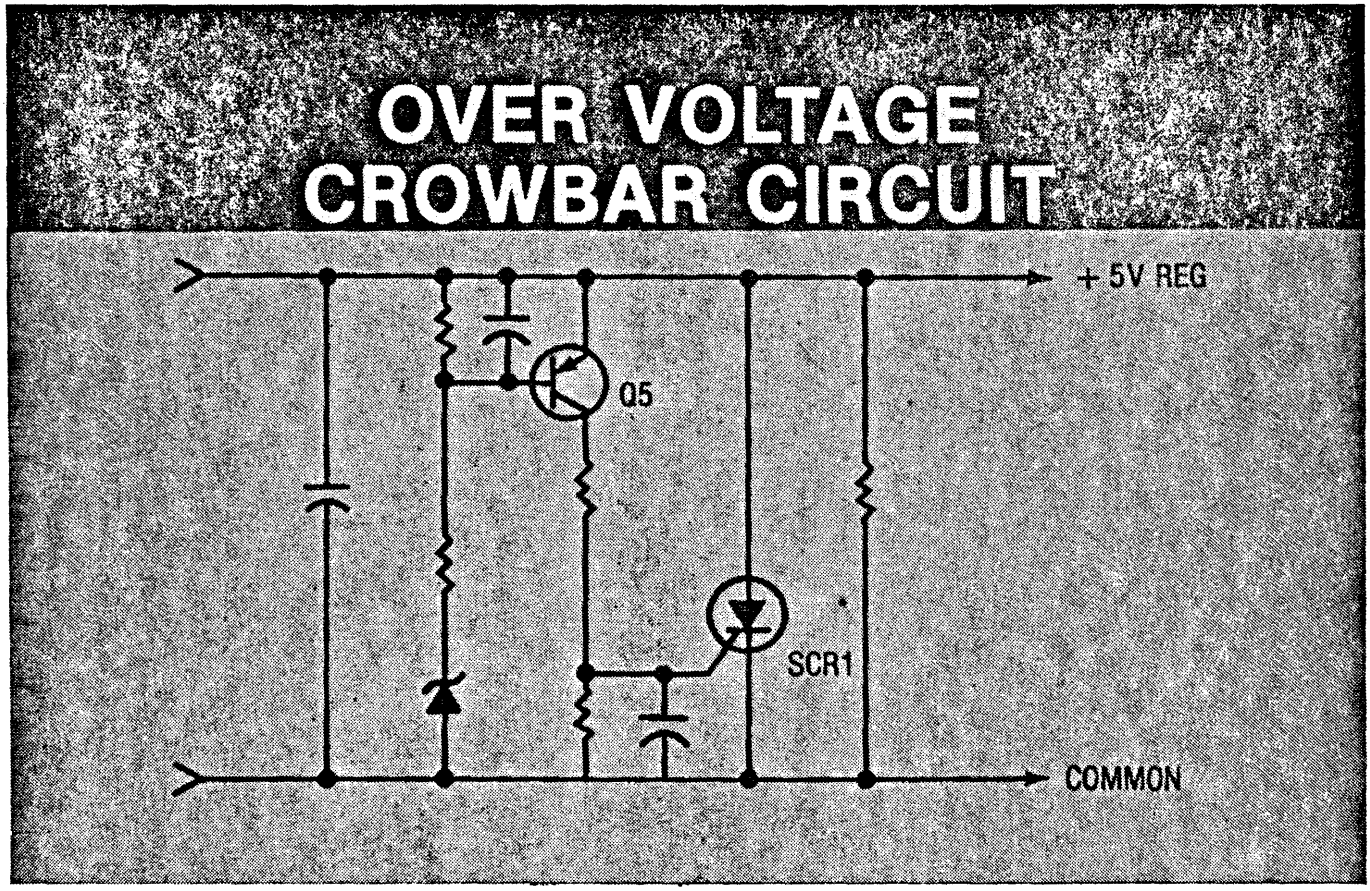
74



THE REGULATOR CIRCUIT, SHOWN FOR THE +5 VOLT SUPPLY, CONSISTS OF A REGULATOR, IC1 WHICH CONTROLS REGULATOR TRANSISTOR Q4. Q4 IN TURN CONTROLS THE MAIN SUPPLY REGULATION TRANSISTORS Q1, Q2 AND Q3. A POTENTIOMETER R14 ADJUSTS THE +5 VOLT LEVEL TO COMPENSATE FOR MINOR DIFFERENCES IN COMPONENT VALUES.

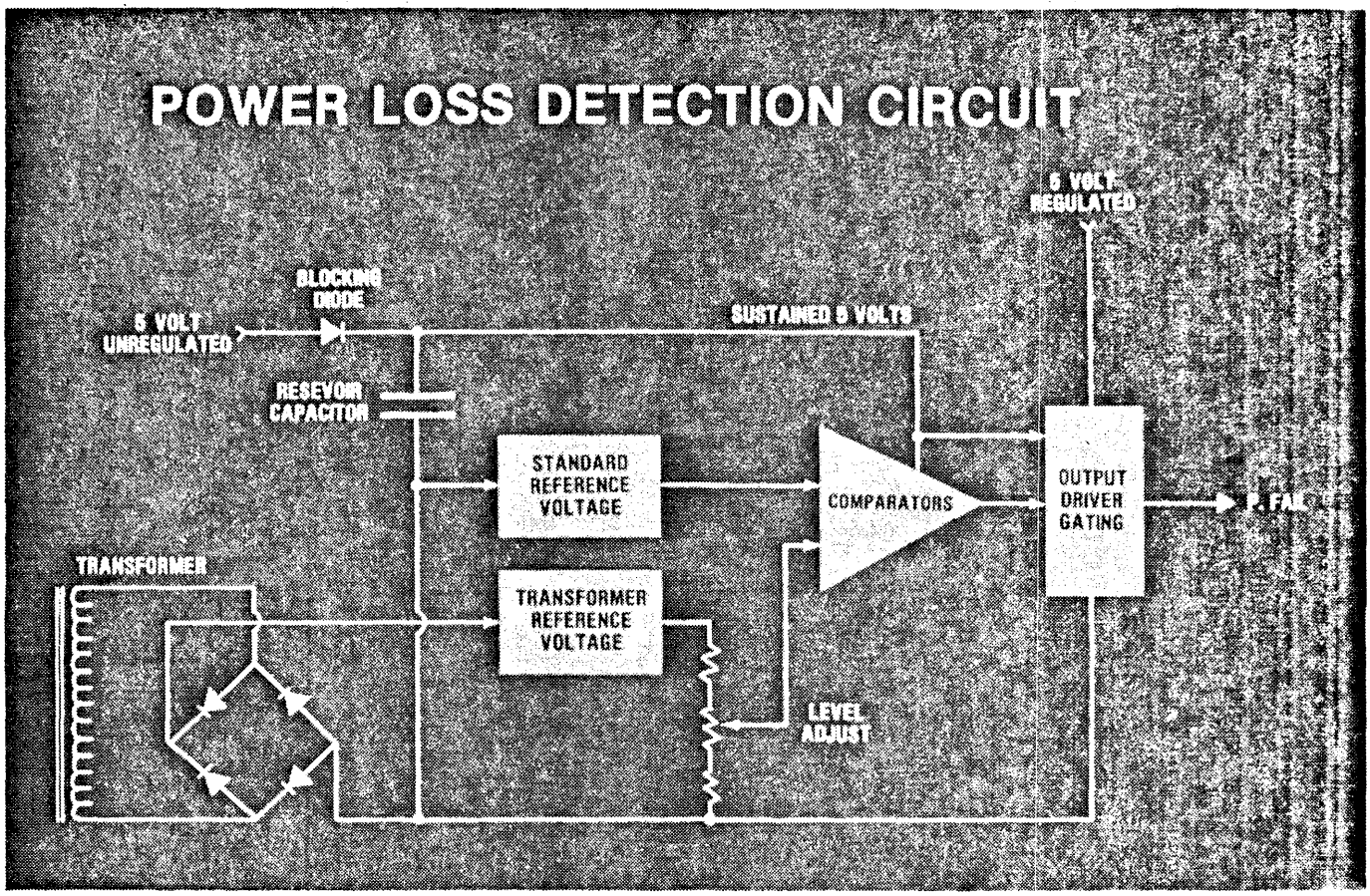
THE CIRCUIT FOR THE –12 VOLT SUPPLY IS SIMILAR, INCLUDING CURRENT FOLD BACK AND A VOLTAGE ADJUSTMENT. ADDITIONAL OVER CURRENT PROTECTION OF THE –12 VOLT SUPPLY IS INCORPORATED BY A FUSE. BECAUSE THE CURRENT SUPPLY REQUIRED OF THE –12 VOLT SUPPLY IS LESS THAN FOR THE +5 VOLT SUPPLY, ONLY ONE MAIN REGULATOR TRANSISTOR IS USED.

75



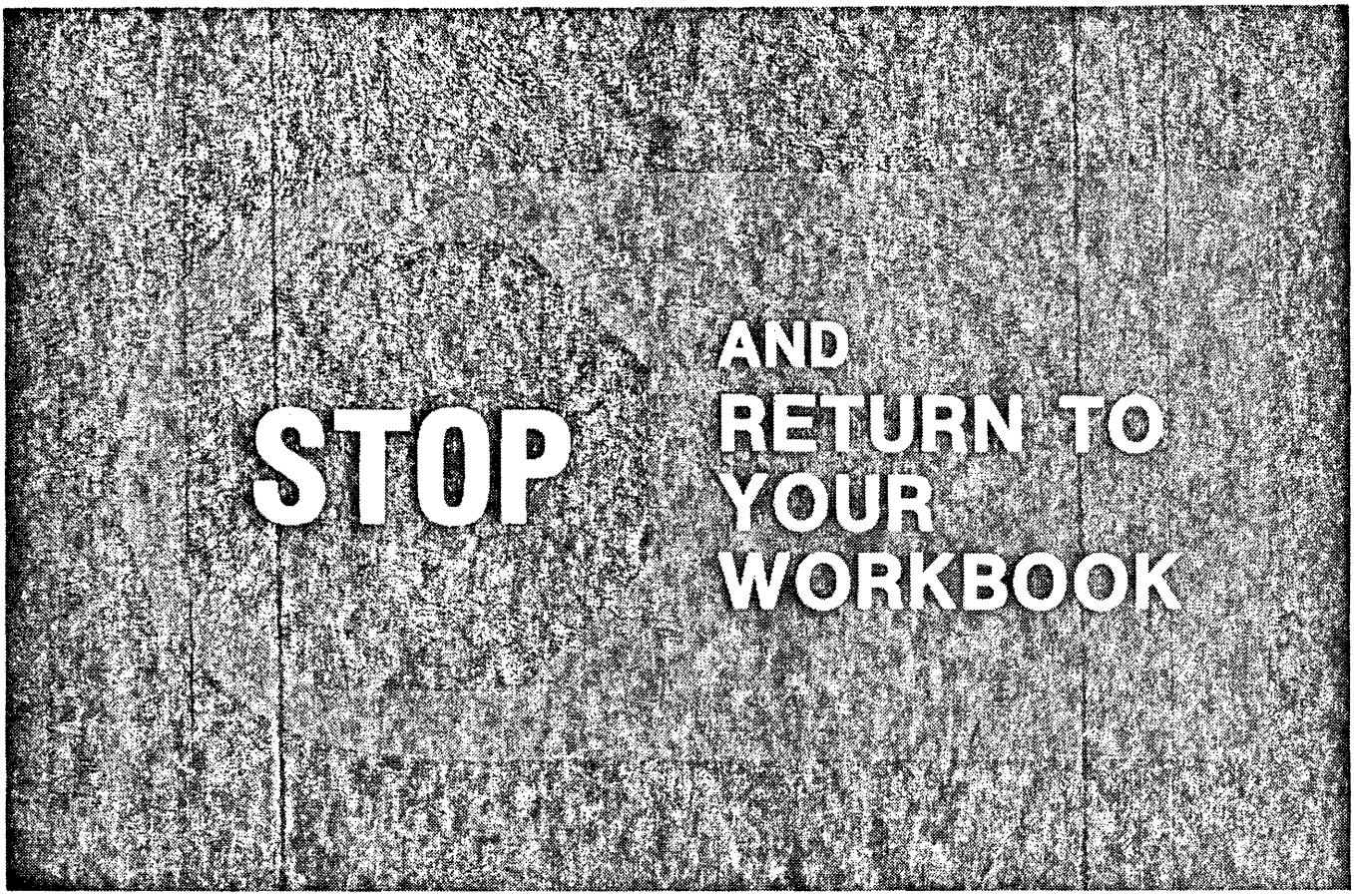
THE CROWBAR CIRCUITS FOR BOTH THE +5 VOLT AND –12 VOLT SUPPLIES ARE IDENTICAL EXCEPT FOR COMPONENT VALUES. IF THE SAFE VOLTAGE DETERMINED BY THE ZENER DIODE IS EXCEEDED, TRANSISTOR Q5 IS SWITCHED ON FIRING SCR1 TO SHORT CIRCUIT THE SUPPLY. THE RESULTANT OVER CURRENT CONDITION CAUSES THE REGULATOR CIRCUIT TO SHUT DOWN.

76

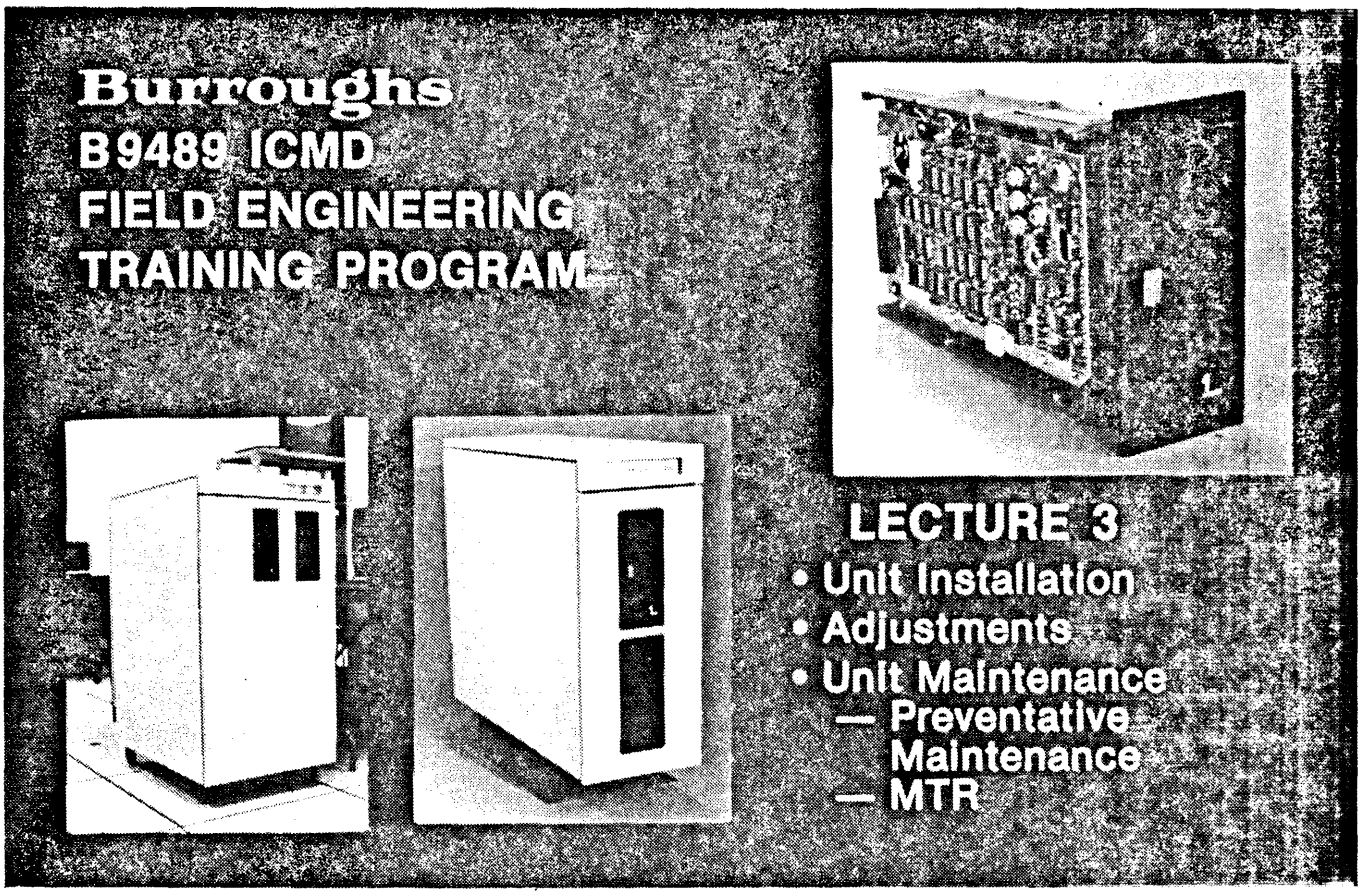


THE POWER LOSS DETECTION LOGIC COMPARES A REFERENCE VOLTAGE FROM A SECONDARY OUTPUT OF THE TRANSFORMER WITH A STANDARD REFERENCE VOLTAGE DERIVED FROM THE 5 VOLT UNREGULATED SUPPLY. IN THE EVENT OF ANY POWER LOSS, INCLUDING A NORMAL POWER OFF, THE OUTPUT FROM THE TRANSFORMER IS LOST ALMOST IMMEDIATELY. ALTHOUGH THE 5V UNREGULATED SUPPLY ALSO DECAYS QUICKLY, A TEMPORARY SUPPLY OF POWER IS AVAILABLE FROM A RESERVOIR CAPACITOR PROTECTED BY THE BLOCKING DIODE. THIS POWER SUSTAINS THE STANDARD REFERENCE VOLTAGE, COMPARATOR, OUTPUT DRIVER GATING LOGIC. AS SOON AS THE REFERENCE VOLTAGE FROM THE TRANSFORMER FALLS BELOW THE STANDARD REFERENCE VOLTAGE, THE COMPARITORS SWITCH THE "PFAIL" SIGNAL LOW TO TURN OFF SELECTED DRIVER IC'S ON THE OPTIONAL DRIVER RECEIVER OR ADAPTOR PCB'S.

77



THIS COMPLETES THE DESCRIPTION OF THE THEORY OF OPERATION OF THE UNIT AND LECTURE 2. STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.



THIS IS THE THIRD LECTURE IN THE BURROUGHS B 9489 INDUSTRY COMPATIBLE MINI DISK (ICMD) TRAINING PROGRAM. THE FIRST SECTION OF THIS THREE-PART LECTURE LOOKS AT UNIT INSTALLATION; THE SECOND SECTION DETAILS EACH OF THE ADJUSTMENTS; AND THE THIRD SECTION DESCRIBES UNIT MAINTENANCE, INCLUDING BOTH FAULT FINDING ASSISTED BY THE MTR PROCEDURES AND PREVENTATIVE MAINTENANCE.

2

B 9489-5 INSTALLATION

Unit cabling
60/50 Hz
Unit drive select number
Unit ready status number
Interface signal termination

THE INSTALLATION PROCEDURES FOR THE DIFFERENT STYLES OF ICMD UNITS ARE BASICALLY THE SAME. THERE ARE, HOWEVER, SOME SLIGHT CONFIGURATION VARIATIONS DEPENDING UPON HOST SYSTEM REQUIREMENTS. TO COVER THE DIFFERENT POSSIBLE CONFIGURATIONS, WE WILL START WITH THE BASIC –5 DRIVE AND THEN NOTE THE POSSIBLE DIFFERENCES FOR THE TWO FREE STANDING CABINET STYLES.

MOST B 9489-5 UNITS WILL ALREADY BE INSTALLED IN THEIR HOST SYSTEMS BEFORE DELIVERY. SOMETIMES, HOWEVER, IT MAY BE NECESSARY TO INSTALL A SECOND UNIT IN A HOST SYSTEM OR SINGLE DRIVE CABINET.

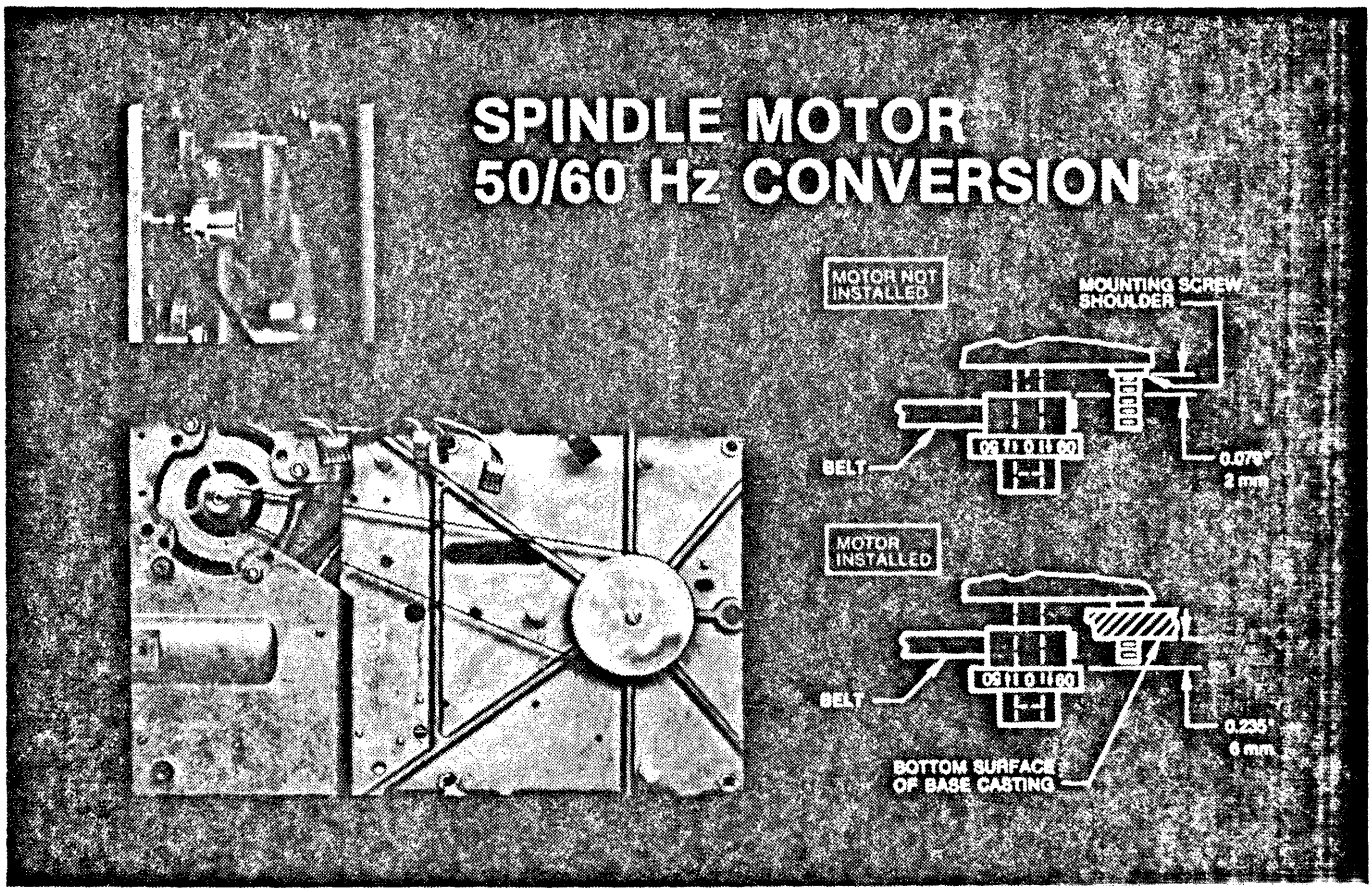
APART FROM THE INSTALLATION OF CABLES, THERE ARE FOUR HARDWARE OPTIONS WHICH REQUIRE POSSIBLE ATTENTION DURING INSTALLATION.

IN SOME LOCATIONS IT MAY BE NECESSARY TO CONVERT THE UNIT FROM 60 HERTZ TO 50 HERTZ OR VICE VERSA.

EACH UNIT MUST ALSO BE CONFIGURED WITH THE DESIGNATED UNIT NUMBER FOR THE DRIVE SELECT AND READY STATUS SIGNALS.

THE LAST DRIVE IN EACH STRING MUST ALSO HAVE A RESISTOR CHIP TERMINATOR INSTALLED TO CORRECTLY TERMINATE THE INTERFACE SIGNAL LINES.

3

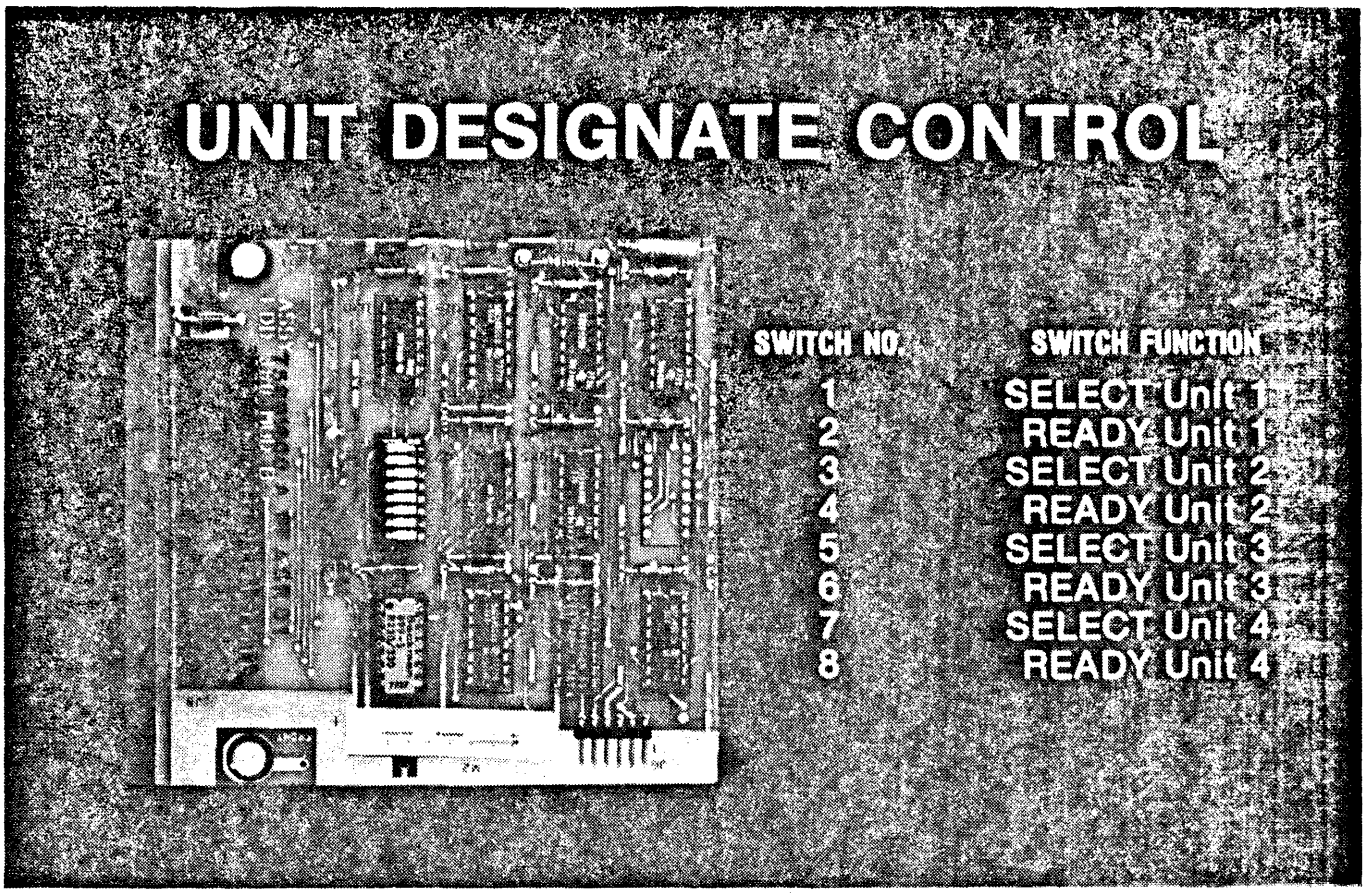


TO CONVERT THE OPERATING FREQUENCY BETWEEN 50 AND 60 HERTZ, THE PULLEY ON THE SPINDLE MOTOR HAS TWO DIAMETERS AND CAN BE REVERSED ON THE MOTOR SHAFT.

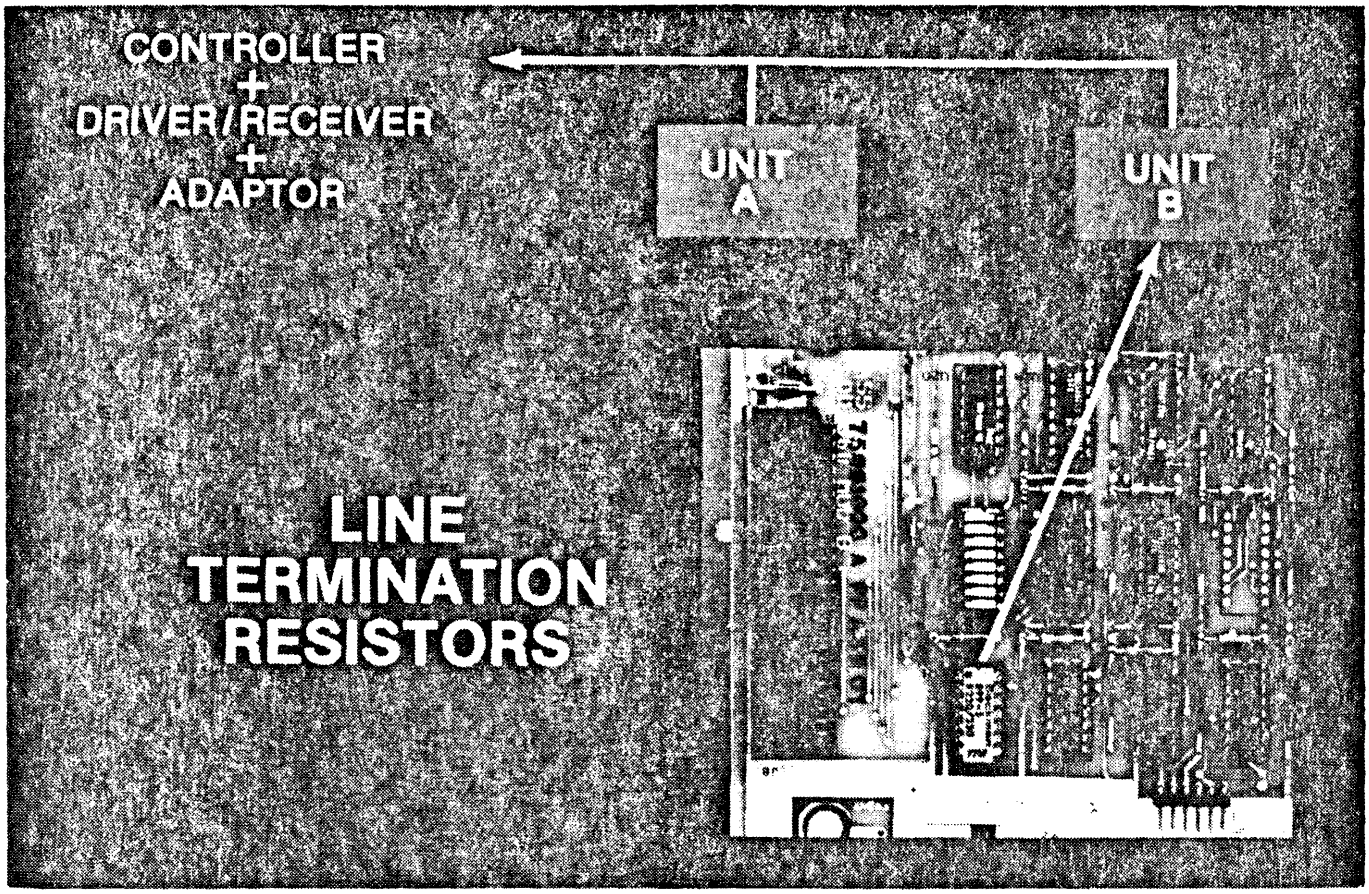
THE BELT RUNS ON THE SMALLER DIAMETER FOR 60 HERTZ AND THE LARGER DIAMETER FOR 50 HERTZ.

TO CONVERT FOR FREQUENCY, SIMPLY LOOSEN THE PULLEY SET SCREW, REMOVE THE PULLEY FROM THE SHAFT, REVERSE AND REPLACE. TO OBTAIN CORRECT ALIGNMENT FOR THE DRIVE BELT, WITH THE MOTOR NOT INSTALLED, THERE SHOULD BE 72 THOU PLUS OR MINUS 1 THOU BETWEEN THE SHOULDER OF THE MOTOR MOUNTING SCREW AND THE LINE OF THE INNER EDGE OF THE PULLEY. WITH THE MOTOR INSTALLED, THERE SHOULD BE 235 THOU BETWEEN THE BOTTOM SURFACE OF THE MOTOR BASE CASTING AND THE STEP IN THE DRIVE PULLEY.

4



THE DESIGNATED UNIT NUMBER IS CONFIGURED USING THE DUAL IN LINE PACKAGE SUBMINIATURE SWITCHES LOCATED ON THE CIRCUIT BOARD NEAR THE LOGIC CABLE CONNECTOR. A TABLE IN THE TECHNICAL MANUAL SHOWS THE TWO SWITCHES WHICH MUST BE CLOSED TO CONFIGURE THE REQUIRED DRIVE NUMBER.

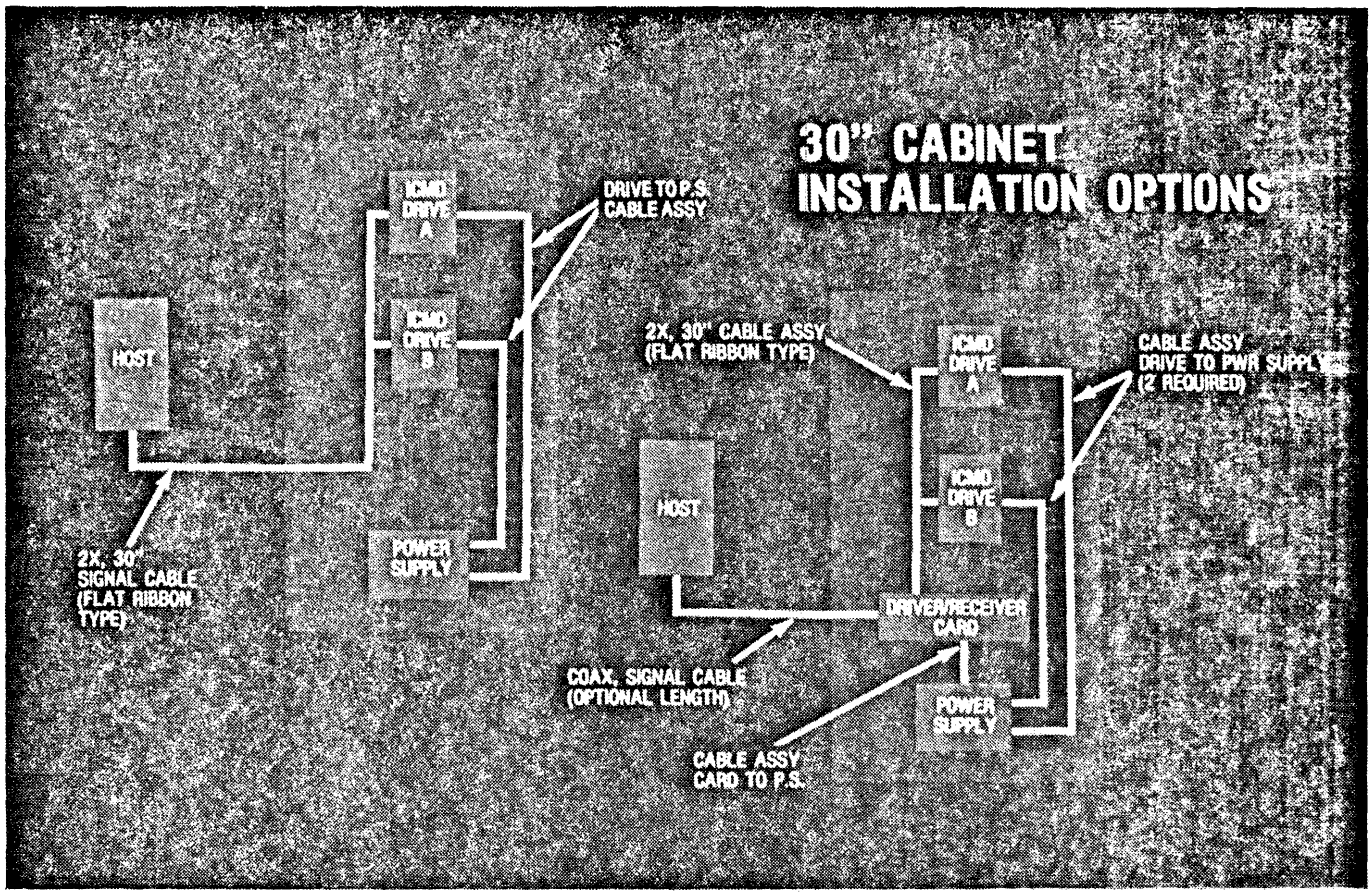


BECAUSE THE INTERFACE CIRCUITS USE "OPEN COLLECTOR" TYPE LOGIC, EACH SIGNAL MUST BE TERMINATED BY A RESISTOR. THIS IS ACHIEVED BY INSERTING A RESISTOR PACKAGE IN THE SOCKET PROVIDED ON THE LOGIC BOARD.

WHERE MORE THAN ONE UNIT IS CONNECTED EITHER DIRECTLY TO THE HOST SYSTEM CONTROLLER OR TO THE OPTIONAL DRIVER RECEIVER CARD OR OPTIONAL ADAPTOR, ONLY INSERT ONE RESISTOR PACKAGE IN THE DRIVE FURTHEST UPSTREAM IN THE STRING. FITTING RESISTOR PACKS IN BOTH DRIVES COULD CAUSE

MARGINAL OPERATION THROUGH EXCESSIVE PULL DOWN ON THE SIGNAL INTERFACE LINES.

6

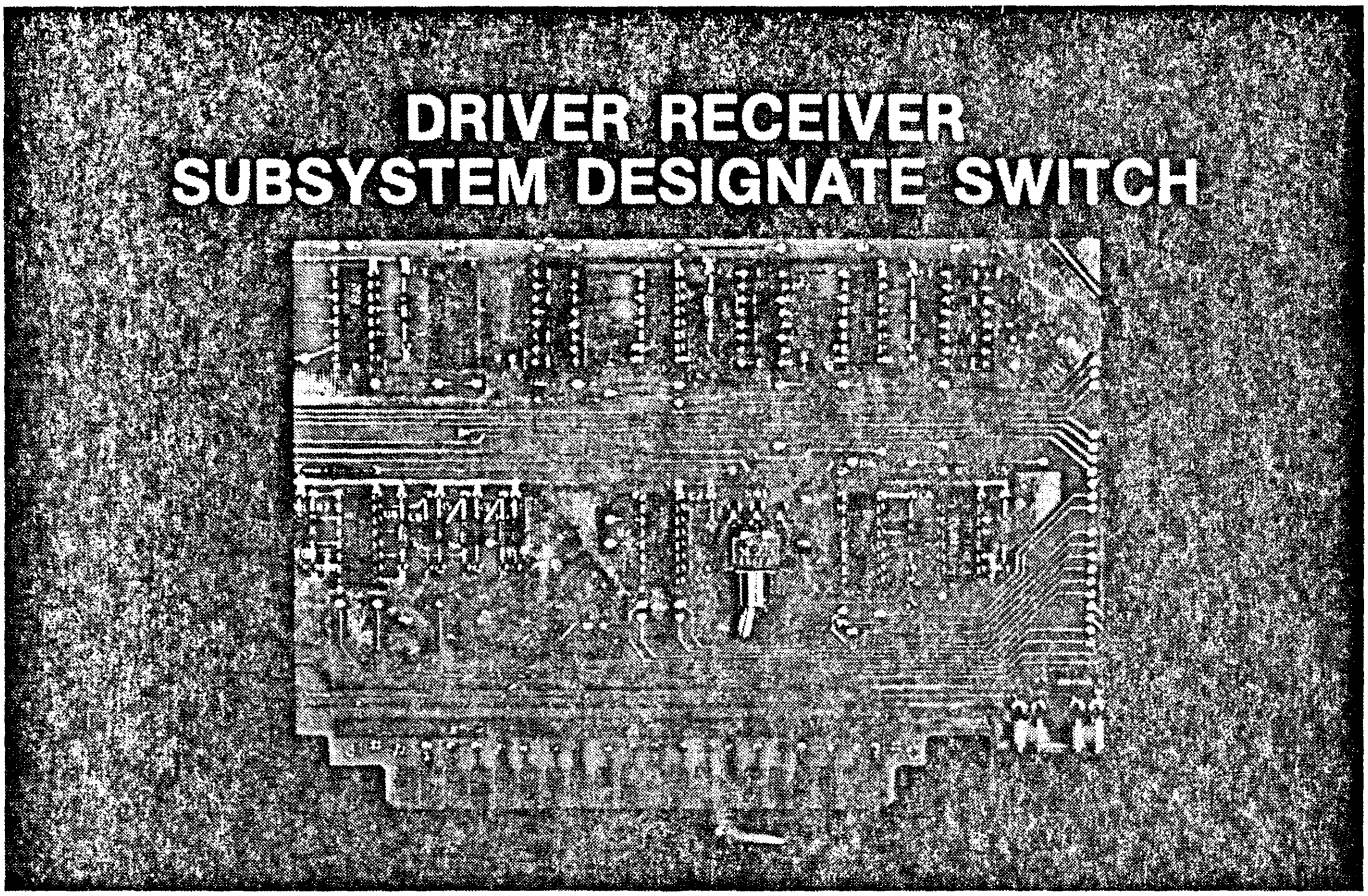


TO INSTALL THE 30" CABINET UNIT, THE SAME PROCEDURES ARE APPLIED TO EACH DRIVE.

IN SOME INSTALLATIONS, IT MAY BE POSSIBLE TO CONNECT THE DRIVE UNIT LOGIC DIRECTLY TO THE HOST SYSTEM CONTROLLER USING TWO 30" LONG FLAT RIBBON TYPE INTERFACE CABLES. WHERE THE LIMITED CABLE LENGTH IS INSUFFICIENT, THE DRIVER/RECEIVER PCB MUST BE INSTALLED.

THE DRIVER/RECEIVER PCB IS CONNECTED TO THE CONTROLLER BY A COAXIAL I/O CABLE. THE COAXIAL I/O CABLE IS AVAILABLE IN FOUR STANDARD LENGTHS BETWEEN 25 AND 100 FEET.

7



THE SUBSYSTEM DESIGNATE SWITCH IS MOUNTED ON THE DRIVER/RECEIVER PCB. AS IS IMPLIED BY THE NAME, THIS TOGGLE SWITCH IS USED TO DESIGNATE THE SUBSYSTEM NUMBER FOR THAT CABINET. THIS SWITCH MUST NORMALLY BE SET TO POSITION 1.

SOME UNITS HAVE AN ARTWORK ERROR ON THE PCB SO THAT THE LABELLING OF POSITIONS 1 AND 2 IS TRANSPOSED. IF A UNIT FAILS TO OPERATE, SET THE SWITCH TO THE POSITION MARKED 2.

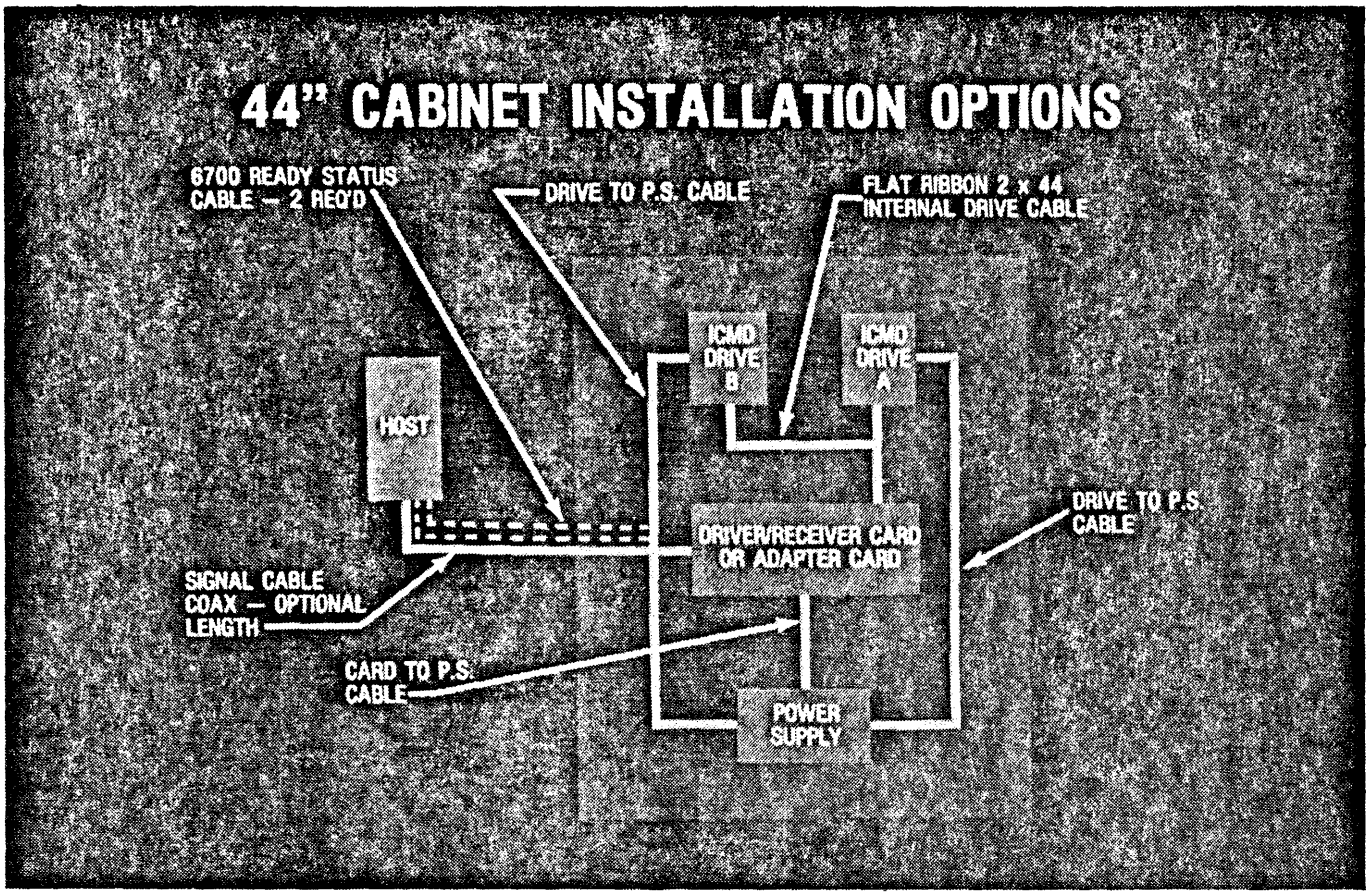
8

INPUT VOLTAGE/FREQUENCY CONVERSION CHART

Input Voltage Frequency	Jumper Connection Red TB103	Orange TB103	Yellow TB103	Blue TB103	Gray TB103	Brown T101	Violet T101	Black T101
100-50 Hz	5	11	17	1	26	31 and 35	26 and 30	25
110	8		19	1				
115	9		20	1				
120	10		21	1				
127	12		22	1				
200	17		23	5				
208	18			7				
220	19			8				
230	20			9				
240	21			10				
250-50 Hz	22	11	23	12	26	31 and 35	26 and 30	25
100-60 Hz	2	6	14	1	25	32 and 34	27 and 29	24
110	3		15	1				
115	4		16	1				
120	5		17	1				
127	7		18	1				
200	14		23	2				
208	14			3				
220	15			3				
230	16			4				
240	17			5				
250-60 Hz	18	6	23	7	25	32 and 34	27 and 29	24

THE REMAINING ITEM TO CHECK IS THE POWER SUPPLY. YOU WILL FIND AN INPUT VOLTAGE/FREQUENCY CONVERSION CHART SHOWING THE REQUIRED TAPPINGS FOR EACH GIVEN VOLTAGE AND FREQUENCY IN THE INSTALLATION SECTION OF THE TECHNICAL MANUAL. THIS CHART IS PARTICULARLY IMPORTANT AS UNITS ARE NORMALLY SHIPPED CONFIGURED FOR 208 VOLT 60 HERTZ OPERATION.

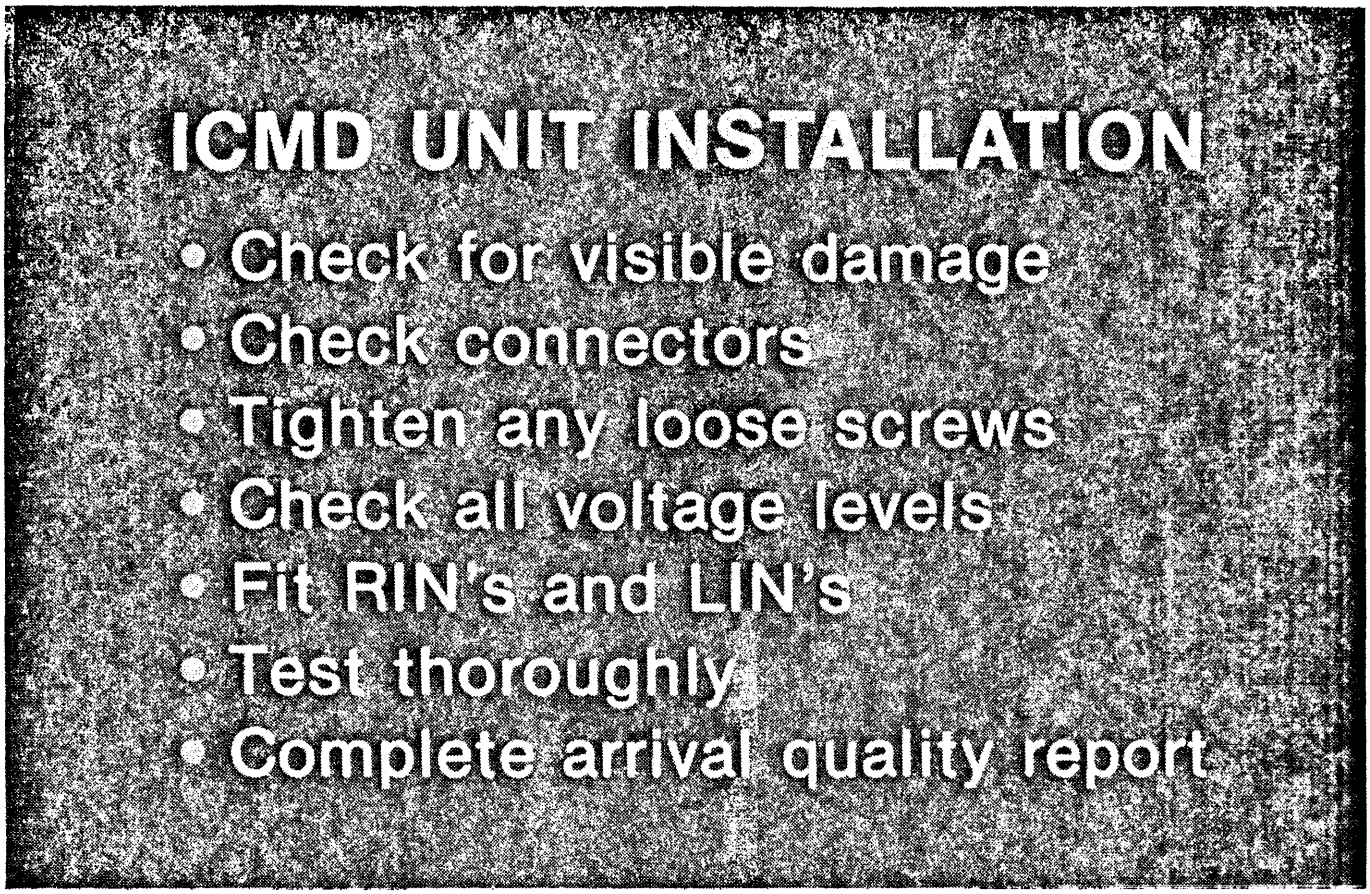
9



THE INSTALLATION PROCEDURE FOR THE 44" CABINET VERSION IS THE SAME AS THE 30" VERSION WITH TWO POSSIBLE EXCEPTIONS, FIRST THE OPTIONAL ADAPTOR PCB AND SECOND THE READY STATUS CABLES REQUIRED FOR OPERATION WITH THE B 6700 AND SOME OTHER LARGE SYSTEMS.

WHEN THE 44" CABINET VERSION IS USED WITH A MEDIUM OR LARGE SYSTEM, THE ADAPTOR PCB IS INSTALLED INSTEAD OF THE DRIVER/RECEIVER PCB. THE SAME COAXIAL INTERFACE CABLE IS USED.

10



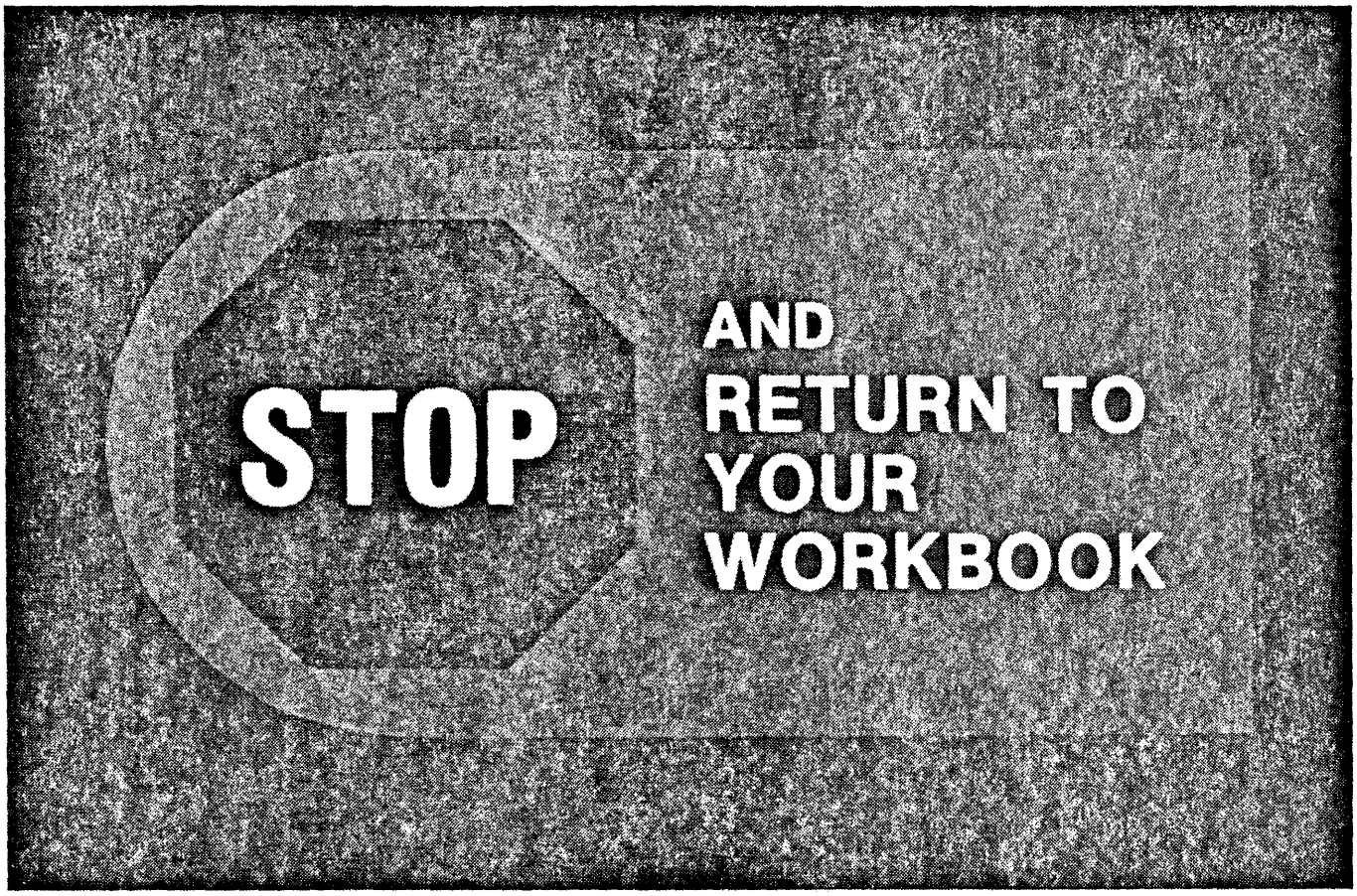
WHEN INSTALLING ANY ICMD UNIT, CHECK FOR VISIBLE SIGNS OF DAMAGE, ENSURE ALL CONNECTORS ARE TIGHT AND TIGHTEN ANY LOOSE SCREWS.

IMMEDIATELY AFTER POWERING ON, CHECK ALL VOLTAGE LEVELS, THESE ARE SPECIFIED IN THE DETAILED INSTALLATION PROCEDURES GIVEN IN THE TECHNICAL MANUAL, AND ADJUST IF NECESSARY.

AFTER YOU ARE SATISFIED THAT ALL IS WELL, FIT ALL "LIN'S" AND ANY REQUIRED "RIN'S" BEFORE THOROUGHLY TESTING EACH FUNCTION OF THE UNIT USING THE TEST ROUTINES PROVIDED THROUGH THE HOST SYSTEM. MAKE ANY NECESSARY ADJUSTMENTS OR CORRECTIONS AND RETEST.

FINALLY, DO NOT FORGET TO COMPLETE THE ARRIVAL QUALITY REPORT AND ENSURE THAT ALL DOCUMENTATION FOR THE UNIT IS SAFELY RETAINED FOR FUTURE USE.

11



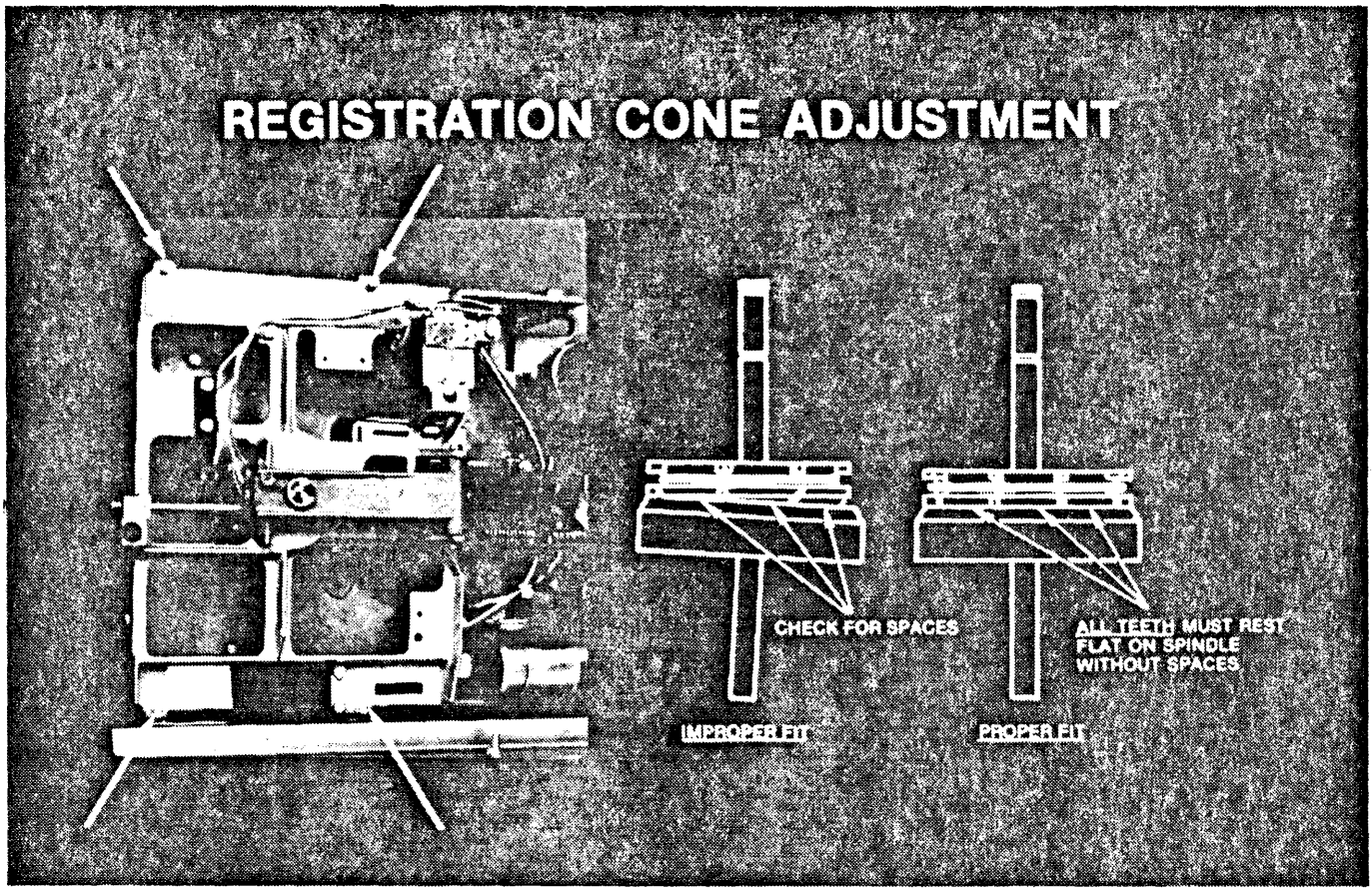
STOP THE LECTURE AT THIS POINT. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

12

THE SECOND PART OF THIS LECTURE DETAILS THE ADJUSTMENT PROCEDURES, WHICH MAY BE REQUIRED DURING MAINTENANCE OF THE ICMD UNIT. CORRECT ADJUSTMENT OF THE DRIVE IS ESSENTIAL NOT ONLY FOR GOOD OPERATION OF AN INDIVIDUAL UNIT, BUT ALSO TO ENSURE THAT THE MEDIA IS COMPATIBLE WITH OTHER UNITS AND CAN BE CROSS READ.

AS A GENERAL RULE, AVOID ALTERING ADJUSTMENTS UNLESS A FAILURE OR TEST INDICATES THAT AN ADJUSTMENT IS REQUIRED, OR A COMPONENT WHICH MAY CHANGE AN ADJUSTMENT IS REPLACED.

13



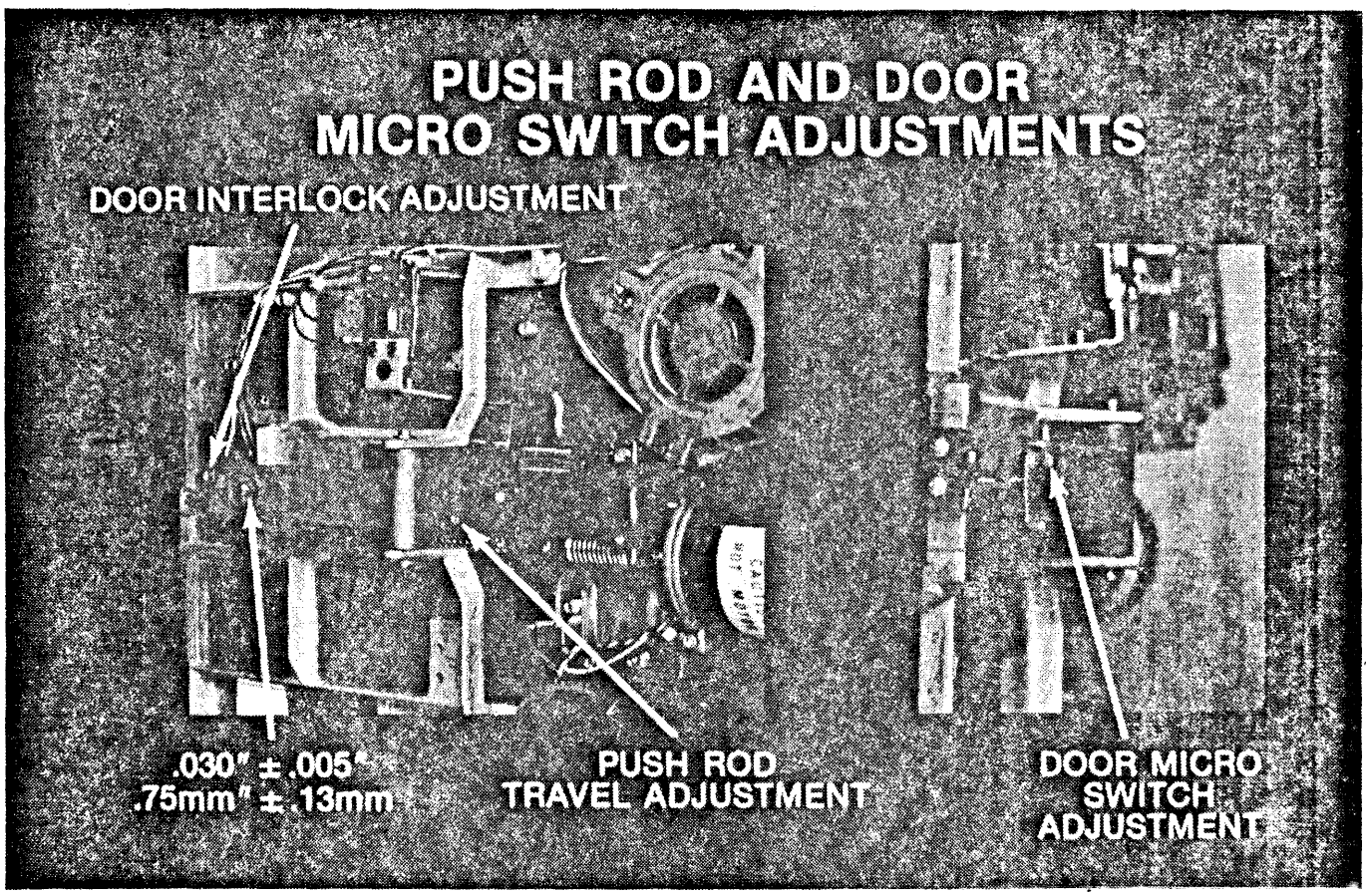
THE HEAD POSITION IN THE DRIVE IS REFERENCED MECHANICALLY TO THE DRIVE SPINDLE. THE DRIVE SPINDLE AND REGISTRATION CONE BOTH CENTER AND CLAMP THE DISKETTE IN A FIXED POSITION RELATIVE TO THE READ/WRITE HEAD. OBSERVE THE RELATIONSHIP OF THE REGISTRATION CONE AND SPINDLE AS THE DOOR IS SLOWLY CLOSED. ALL SEGMENTS ON THE CONE SHOULD SEAT FULLY INTO THE SPINDLE. REPEAT OPENING AND CLOSING THE DOOR SEVERAL TIMES WHILE SLOWLY ROTATING THE SPINDLE. VERIFY THAT ALL SEGMENTS SEAT UNIFORMLY AT THE SAME TIME. A "CLICKING" SOUND OR VISIBLE SEGMENT DISTORTION AS THE CONE ENGAGES IN THE TURNING SPINDLE, INDICATES THAT ADJUSTMENT IS NEEDED.

ADJUSTMENT IS MADE BY SLIGHTLY LOOSENING THE FOUR SCREWS WHICH HOLD

THE SUPPORT ASSEMBLY TO THE BASE AND MOVING THE SUPPORT ASSEMBLY WHICH INCLUDES THE REGISTRATION CONE.

AFTER FINDING THE CORRECT POSITION, TIGHTEN THE FOUR SCREWS AND RE-CHECK.

14



THE TRAVEL OF THE PUSH ROD WHICH ACTUATES THE DISK LOAD ARM, CLAMPING THE DISKETTE TO THE SPINDLE, MUST BE ADJUSTED TO ENSURE THE DISKETTE IS CLAMPED WITH THE PROPER PRESSURE. TOO LITTLE PRESSURE WILL RESULT IN MISPOSITIONING OR SLIPPAGE AND TOO MUCH PRESSURE WILL DISTORT THE DISKETTE.

A DISKETTE IS NOT REQUIRED TO CHECK THE ADJUSTMENT. CLOSE THE DRIVE

DOOR, MEASURE THE CLEARANCE BETWEEN THE RETAINING CLIP ON THE END OF THE ALIGNMENT CONE SHAFT AND THE BUSHING WHICH RIDES AGAINST THE DISK LOAD ARM. THE CORRECT CLEARANCE IS 30 THOU.

IF NECESSARY, INCREASE OR DECREASE THE CLEARANCE BY TURNING THE ADJUSTMENT SCREW IN THE DISK LOAD ARM.

THE FORWARD EXTENSION OF THE DISK LOAD ARM CONTAINS A SET SCREW WHICH ACTIVATES THE DOOR INTERLOCK MICROSWITCH WHEN THE DOOR IS CLOSED. BECAUSE THIS MECHANISM IS OPERATED BY THE PUSH ROD, ADJUSTMENT OF THE PUSH ROD TRAVEL TO GIVE CORRECT CLAMP PRESSURE WILL ALTER THE DOOR INTERLOCK MICROSWITCH ADJUSTMENT. BECAUSE OF THIS, ALWAYS MAKE THE PUSH ROD TRAVEL ADJUSTMENT FIRST.

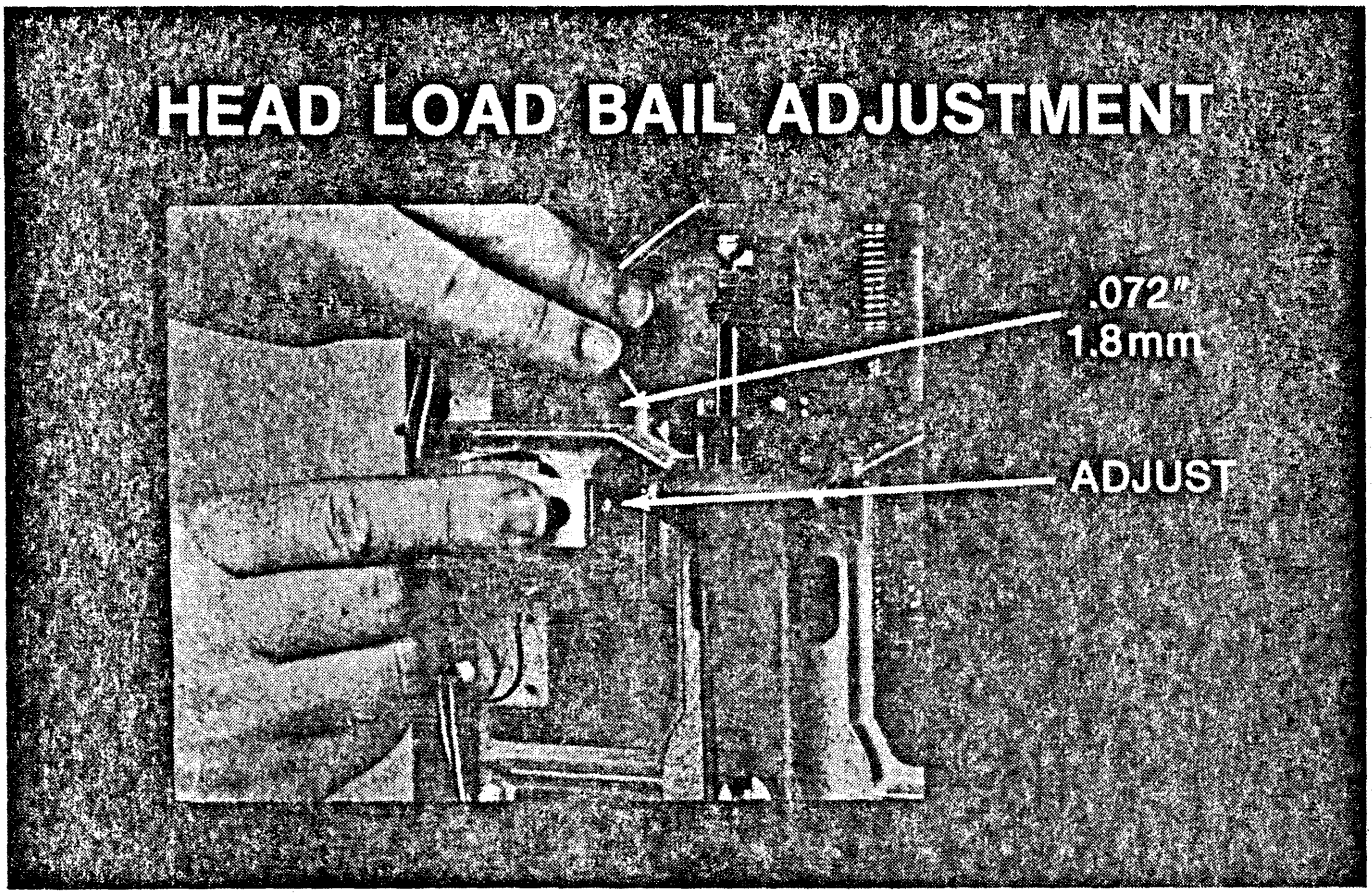
TO BOTH CHECK AND MAKE THIS ADJUSTMENT, CLOSE THE DRIVE DOOR AND TURN THE SET SCREW COUNTERCLOCKWISE UNTIL THE SWITCH OPENS. THEN, ROTATE CLOCKWISE UNTIL THE SWITCH CLOSES. TO ENSURE POSITIVE OPERATION, ROTATE THE SET SCREW AN ADDITIONAL HALF TURN CLOCKWISE.

5

THE HEAD LOAD BAIL IS ACTIVATED BY A SOLENOID UNDER CONTROL OF THE HOST SYSTEM CONTROLLER. THE HEAD LOAD BAIL HAS TWO FUNCTIONS, FIRST THE HEAD LOAD PAD CONTACTS THE REVERSE SURFACE OF THE DISKETTE HOLDING THE DISKETTE AGAINST THE HEAD BY SPRING TENSION. SECONDLY, THE HEAD LOAD BAIL LIGHTLY CLAMPS THE ENVELOPE OF THE DISKETTE TO REDUCE FLUTTER AND WOBBLE. IF THE CLAMPING ACTION IS TOO TIGHT, POOR REGISTRATION AND ERRATIC DISK SPEED WILL RESULT.

THIS ADJUSTMENT SHOULD ONLY REQUIRE ATTENTION WHEN THE HEAD LOAD SOLENOID OR THE FOAM PRESSURE PAD IS REPLACED.

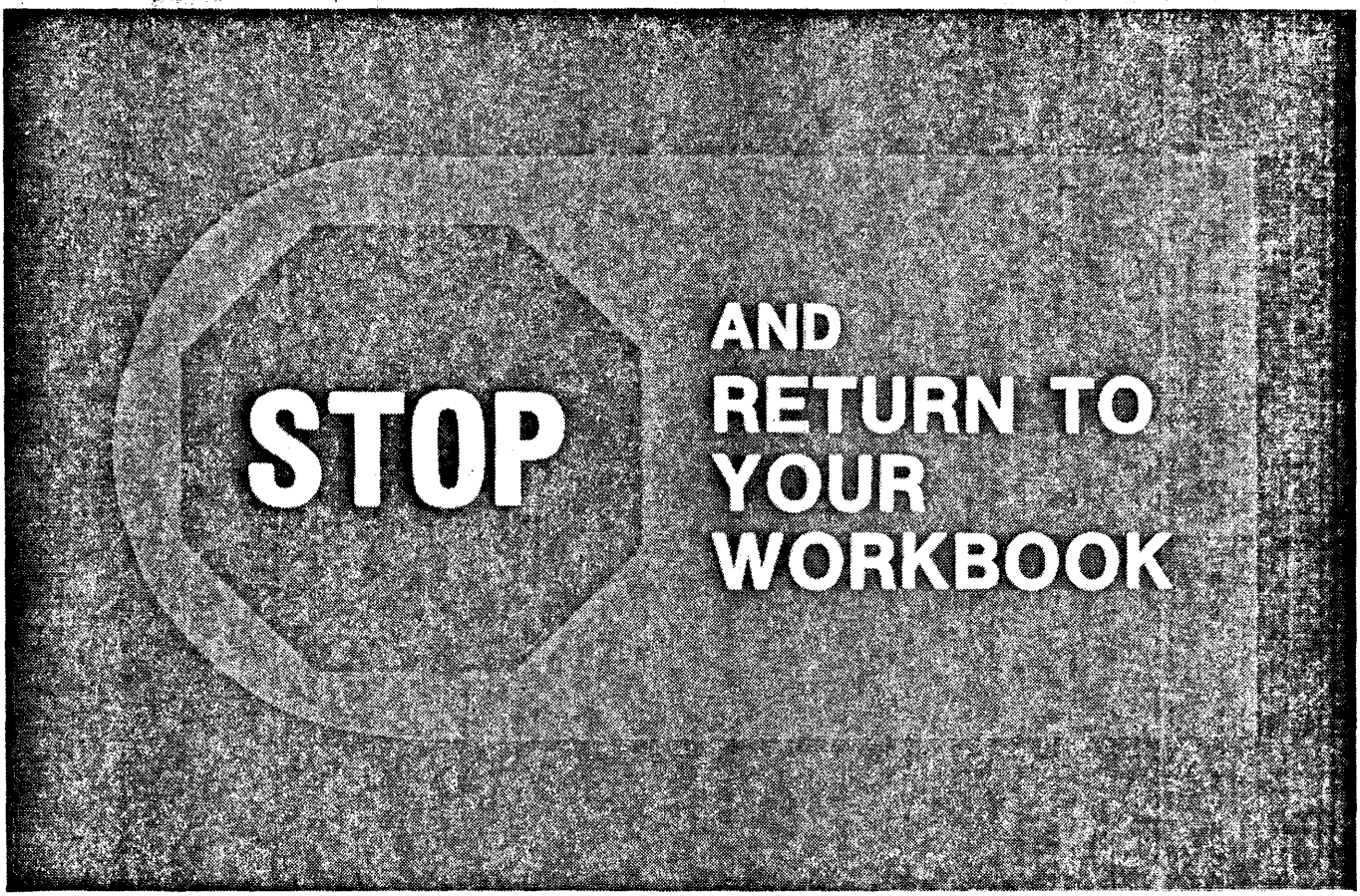
16



START BY LOOSENING THE BAIL MOUNTING SCREW AND THEN MANUALLY PRESS THE SOLENOID CLAPPER SIMULATING THAT THE SOLENOID IS ENERGIZED. INSERT A 72 THOU FEELER GAUGE BETWEEN THE BAIL AND THE BASE CASTING SUPPORT AVOIDING THE FOAM STRIP. NOTE THAT THE ADJUSTED DIMENSION IS BETWEEN THE CASTING AND THE METAL OF THE BAIL, NOT THE FOAM STRIP.

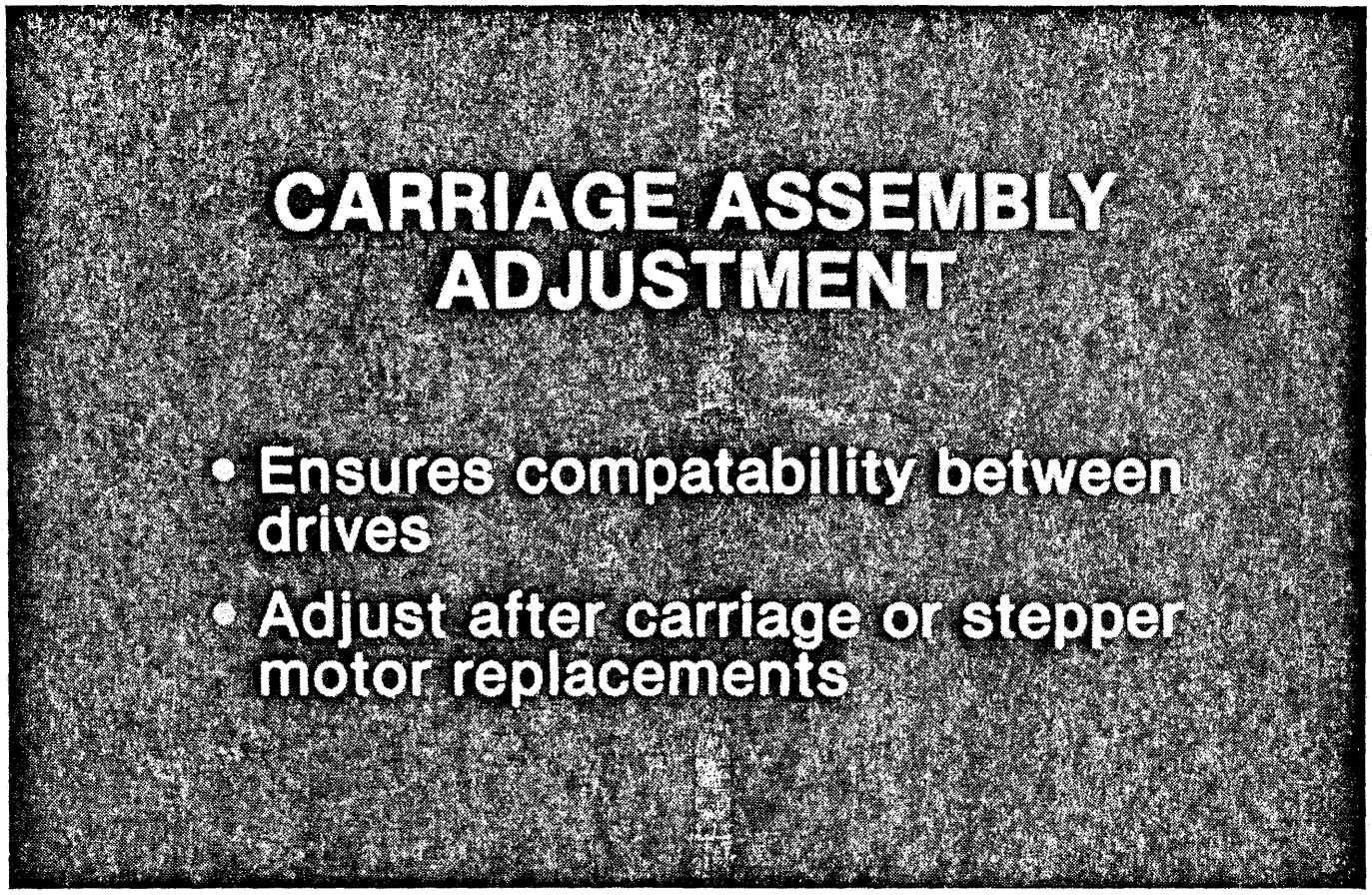
ENSURE THAT THE BAIL IS PARALLEL WITH THE BASE CASTING SUPPORT BY CHECKING THAT THE CLEARANCE IS EQUAL AT BOTH ENDS OF THE BAIL AND TIGHTEN THE BAIL MOUNTING SCREW.

17



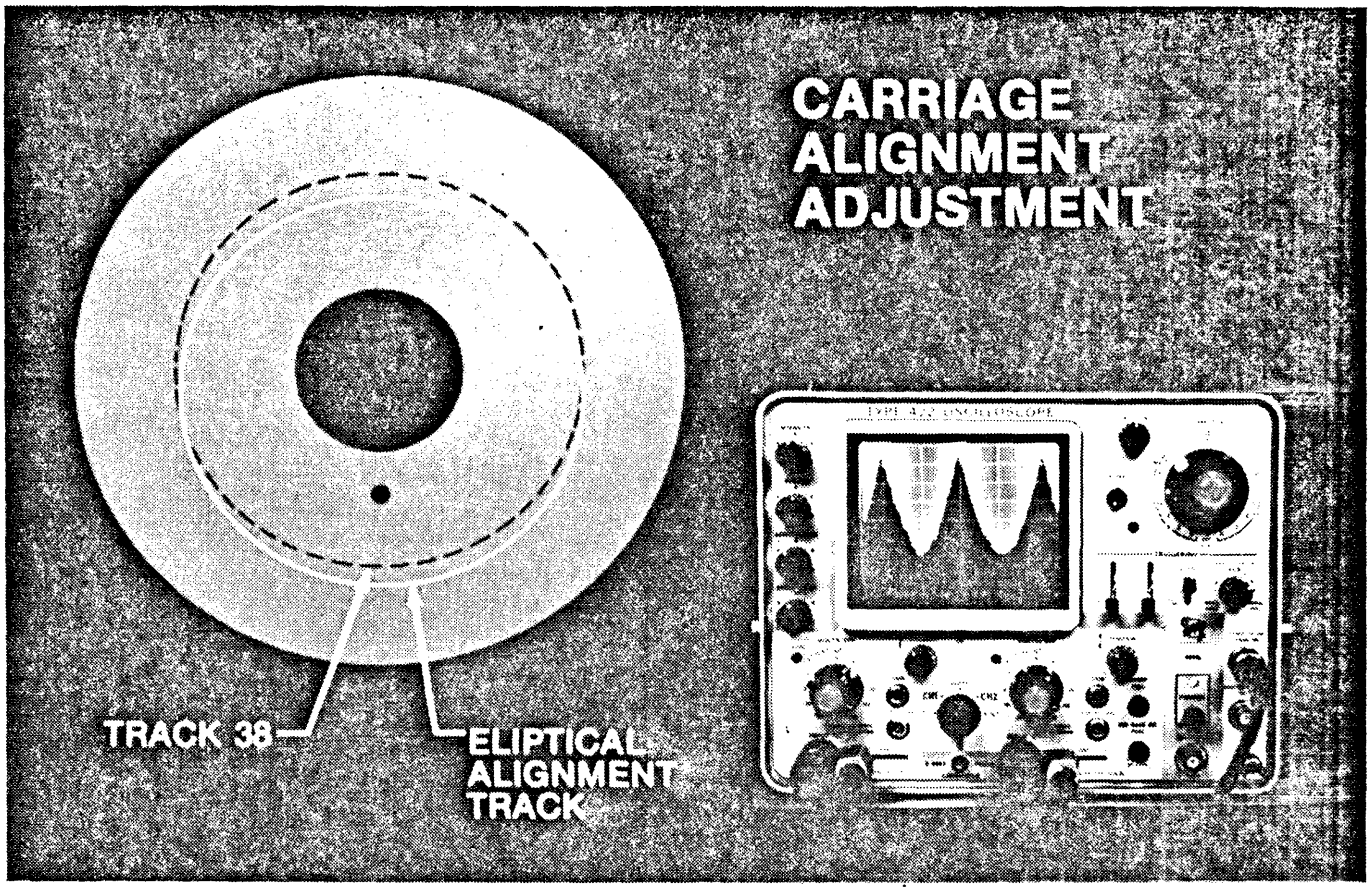
STOP THE LECTURE AT THIS POINT AND REFER TO THE WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

18



CORRECT ADJUSTMENT OF THE CARRIAGE ASSEMBLY IS ESSENTIAL TO PROVIDE COMPATABILITY BETWEEN DRIVE UNITS. EACH STEPPER MOTOR DETENT POSITION MUST ALIGN THE READ/WRITE HEAD PRECISELY AT EACH GIVEN TRACK LOCATION. THIS ALIGNMENT ADJUSTMENT SHOULD ONLY BE NECESSARY AFTER REPLACING THE CARRIAGE OR STEPPER MOTOR ASSEMBLY.

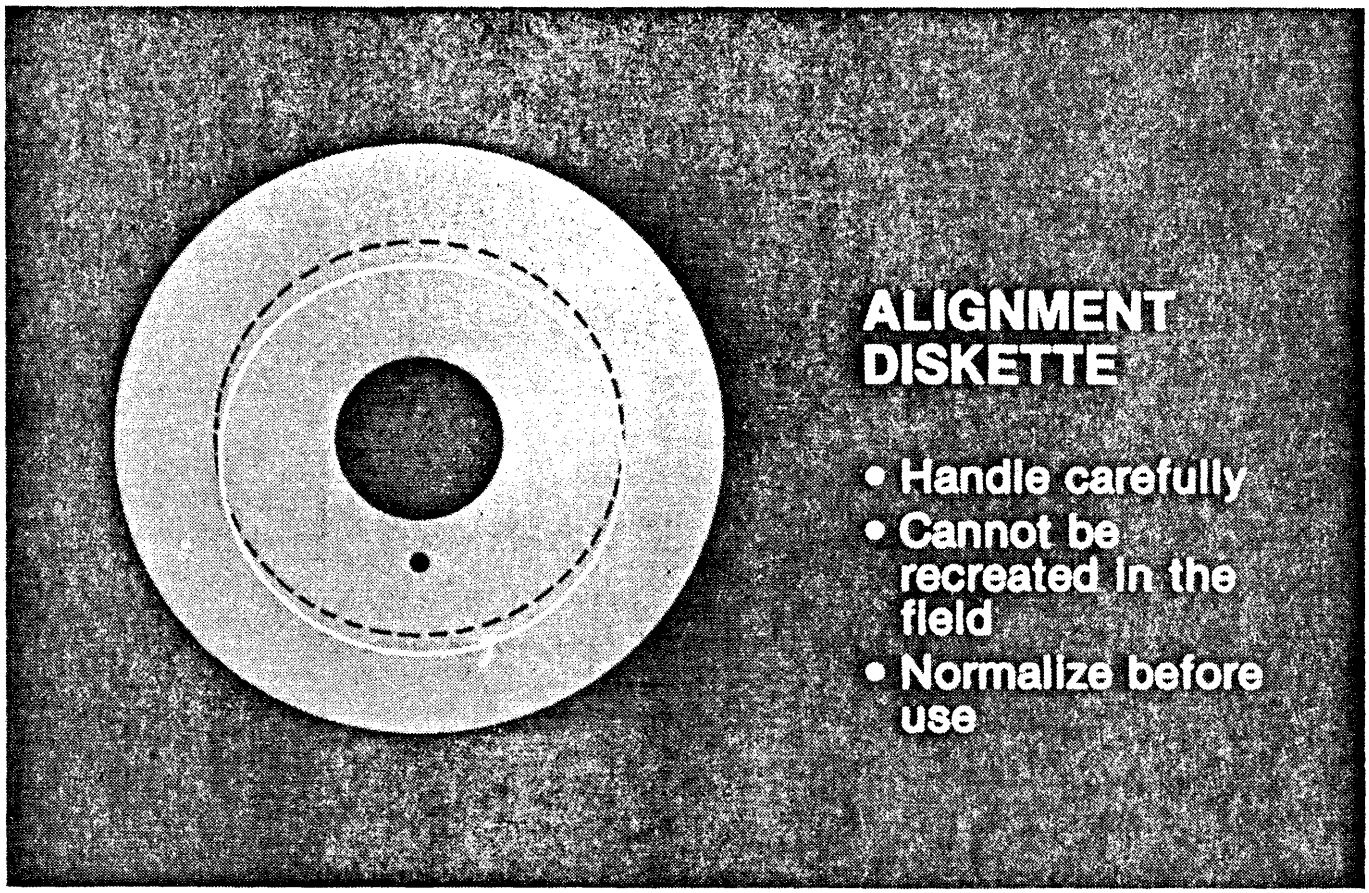
19



THE CARRIAGE ALIGNMENT ADJUSTMENT IS PERFORMED USING A SPECIALLY RECORDED ALIGNMENT DISKETTE. THIS DISKETTE HAS A DATA PATTERN RECORDED ON A TRACK WHICH IS ELLIPTICAL ON EITHER SIDE OF THE TRACK 38 LOCATION. THE DATA PATTERN IS RECORDED IN A SPECIAL WAY WITHOUT SECTORING SO THAT WHEN OBSERVED WITH AN OSCILLOSCOPE, THE READBACK CONSISTS OF TWO LOBES USUALLY REFERRED TO AS "CATEYES." THE CATEYES PATTERN PRODUCES A ZERO READBACK AMPLITUDE SIGNAL AT THE BEGINNING AND CENTER OF EACH TRACK.

CORRECT ALIGNMENT IS ACHIEVED WHEN THE OSCILLOSCOPE DISPLAY SHOWS THAT BOTH THE DISPLAYED LOBES OR CATEYES ARE THE SAME AMPLITUDE. ANY DIFFERENCE IN AMPLITUDE INDICATES AN "OFF-TRACK" CONDITION.

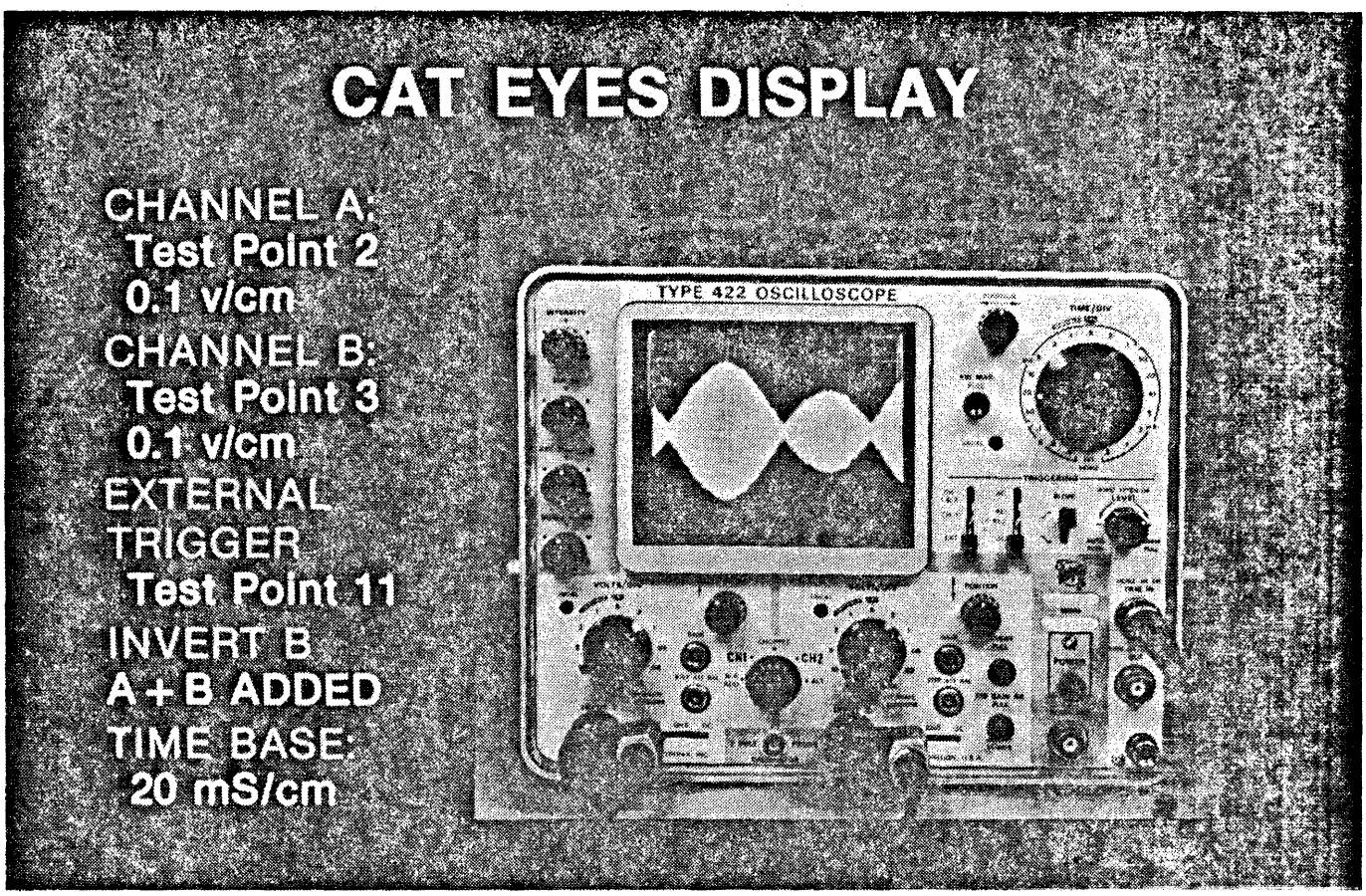
20



THE ALIGNMENT DISKETTE IS CRITICAL TO THIS ADJUSTMENT AND MUST BE HANDLED CAREFULLY BECAUSE IT IS COSTLY AND CANNOT BE RECREATED IN THE FIELD. ALWAYS TAKE EVERY PRECAUTION TO ENSURE THAT THE ALIGNMENT DISKETTE IS NOT OVERWRITTEN OR PHYSICALLY DAMAGED.

BEFORE USING THE ALIGNMENT DISKETTE, IT MUST BE "NORMALIZED" TO THE SAME TEMPERATURE AND HUMIDITY AS THE DRIVE TO BE ADJUSTED. BOTH TEMPERATURE AND HUMIDITY VARIATIONS CAUSE SLIGHT CHANGES IN THE DIMENSIONS OF THE DISKETTE. NORMALIZATION SHOULD BE ACHIEVED BY STORING THE DISKETTE IN THE SAME AREA AS THE DRIVE UNIT FOR ABOUT AN HOUR BEFORE USE.

21



CHECK THE ALIGNMENT ADJUSTMENT USING AN OSCILLOSCOPE AND THE PROCEDURE IN THE TECHNICAL MANUAL.

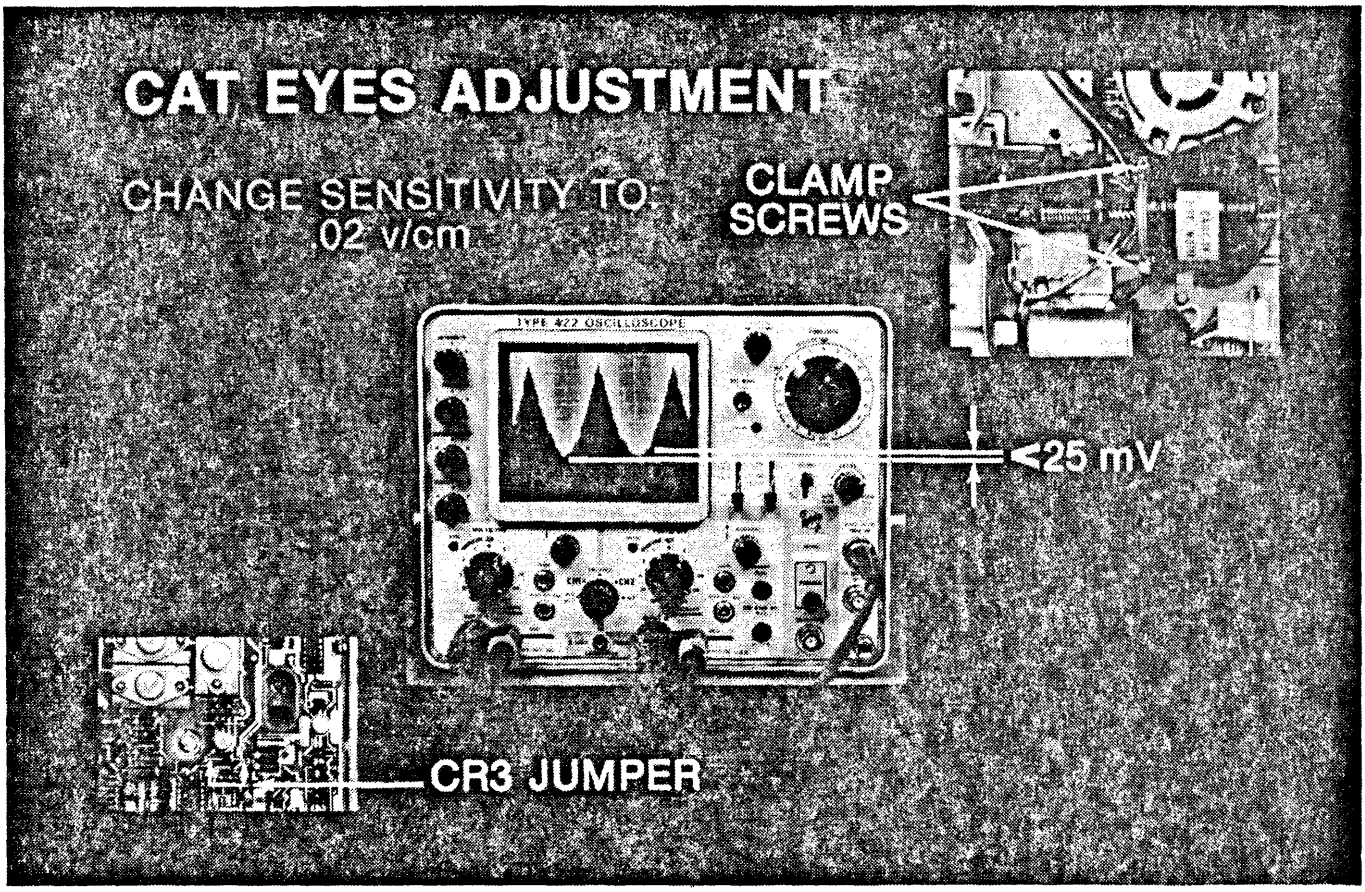
AS IS SHOWN IN THE PICTURE, CONNECT CHANNEL "A" TO TEST POINT 2, CHANNEL "B" TO TEST POINT 3, AND THE EXTERNAL TRIGGER TO TEST POINT 11. SET THE SENSITIVITY ON BOTH CHANNELS TO 0.1 VOLTS PER CM. AND SET THE TRIGGER TO POSITIVE GOING. INVERT CHANNEL "B" AND ADD "A" TO "B." FINALLY, SET THE TIME BASE TO 20 MILLISECONDS PER CM.

AFTER SETTING THE OSCILLOSCOPE, POWER THE DRIVE UNIT OFF AND ON TO RESET ALL LOGIC CIRCUITS. INSERT THE ALIGNMENT DISKETTE, STEP TO TRACK 38 AND EVOKE A CONTINUOUS READ.

IF AT THIS TIME THERE IS NO READBACK SIGNAL DISPLAYED, MANUALLY TURN THE SCREW SHAFT TO POSITION THE CARRIAGE IN OR OUT UNTIL THE PATTERN IS LOCATED.

ADJUST THE TRIGGER LEVEL TO DISPLAY A "CATEYE" ENVELOPE SIMILAR TO THE ONE SHOWN.

22



AFTER ESTABLISHING THE DISPLAY OF THE CATEYE PATTERN, CHANGE THE "A" AND "B" CHANNEL SENSITIVITY TO 0.02 VOLTS/CM. AND MOVE THE DISPLAY SO THAT THE BOTTOM OF THE LARGEST LOBE IS ON A BASE LINE AS SHOWN.

ADJUSTMENT IS REQUIRED WHEN THE PEAK AMPLITUDE DIFFERENCE BETWEEN THE LOBES IS GREATER THAN 25 MILLIVOLTS.

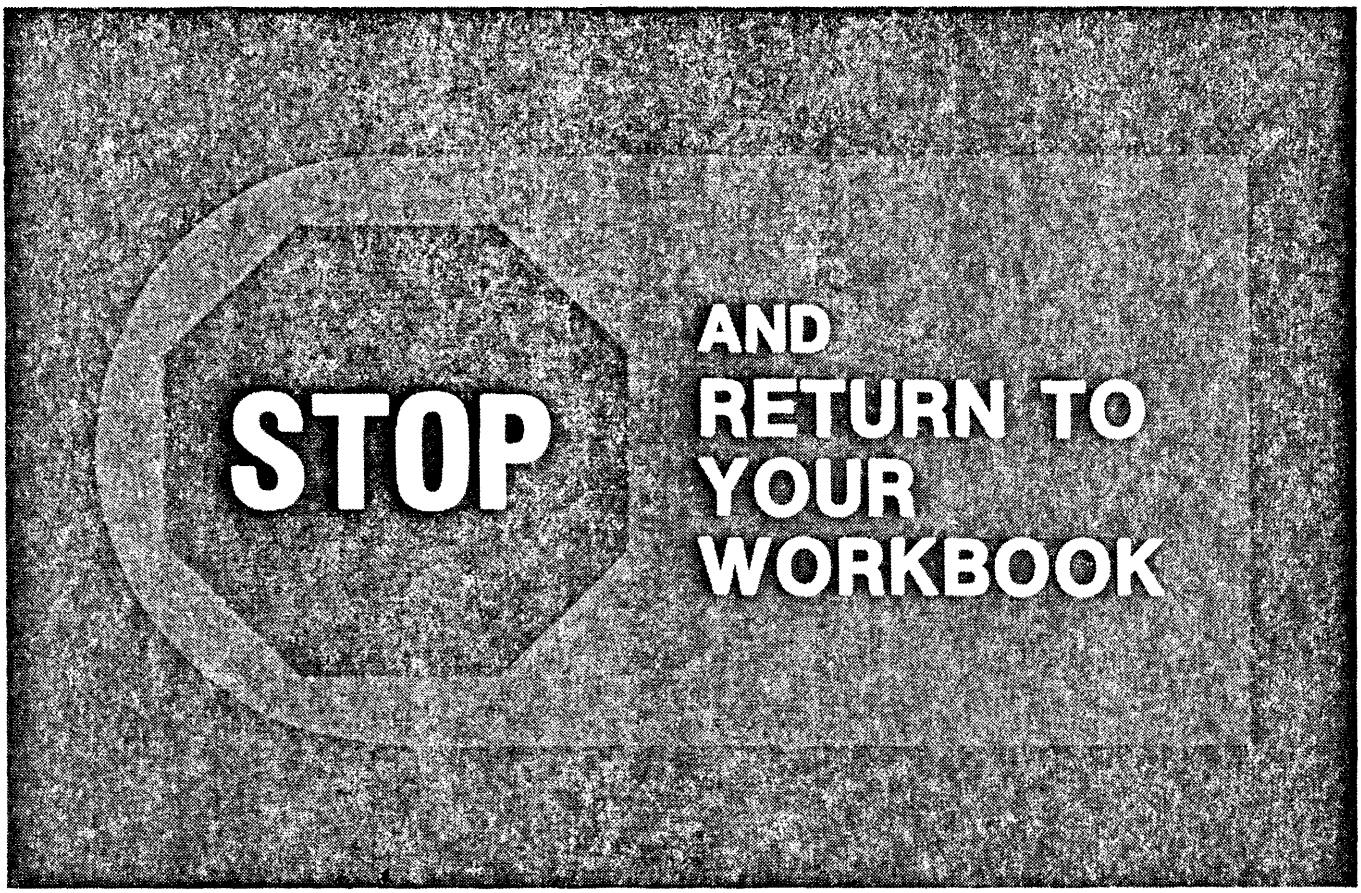
TO MAKE THE ADJUSTMENT, CONNECT A JUMPER LEAD ACROSS DIODE CR3. THIS OVERRIDES THE NORMAL 5 VOLT STEPPER MOTOR HOLD VOLTAGE WITH 24 VOLTS TO DETENT THE MOTOR FIRMLY.

LOOSEN THE STEPPER MOTOR CLAMP SCREWS AND SLOWLY ROTATE THE COMPLETE STEPPER MOTOR UNTIL THE LOBES ON THE OSCILLOSCOPE DISPLAY ARE EQUAL WITHIN 5 MILLIVOLTS. TIGHTEN THE MOTOR CLAMP SCREWS ENSURING THAT THE ADJUSTMENT DOES NOT CHANGE.

REMEMBER TO REMOVE THE JUMPER LEAD FROM CR3 TO AVOID OVERHEATING THE MOTOR.

FINALLY, CHECK THE ADJUSTMENT BY STEPPING BACK TO TRACK 00 AND THEN BACK TO TRACK 38. VERIFY THAT THE PEAK AMPLITUDE DIFFERENCE IS STILL WITHIN 5 MILLIVOLTS.

23



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

OPTICAL TRACK 00 SENSOR ADJUSTMENT PROCEDURES

PROCEDURE 1:

Adjustment referenced to Track 38 on alignment diskette

PROCEDURE 2:

Adjustment referenced to outer carriage stop

AFTER COMPLETING THE ALIGNMENT ADJUSTMENTS, IT IS NECESSARY TO CHECK THE OPTICAL TRACK 00 SENSOR ALIGNMENT, ESPECIALLY IF AFTER STEPPING 38 TRACKS IN THE CARRIAGE ALIGNMENT PROCEDURE IT WAS NECESSARY TO MANUALLY ROTATE THE LEADSCREW TO LOCATE THE ALIGNMENT TRACK.

THERE ARE TWO ALTERNATIVE PROCEDURES FOR ALIGNING THE TRACK 00 SENSOR. ONE PROCEDURE USES TRACK 38 ON THE ALIGNMENT DISKETTE AS A REFERENCE FROM WHICH TO STEP TO TRACK 00. THE OTHER PROCEDURE ASSUMES THAT THE HEAD CARRIAGE AND OUTER CARRIAGE STOP ARE CORRECTLY ALIGNED SO THAT THE OUTER CARRIAGE STOP CAN BE USED AS A MECHANICAL REFERENCE FOR LOCATING TRACK 00. THIS PROCEDURE SHOULD BE USED WHEN, FOR EXAMPLE, THE SENSOR HAS BEEN REPLACED AND NO ADJUSTMENT HAS BEEN MADE TO THE HEAD CARRIAGE, LEADSCREW AND STOP ASSEMBLIES.

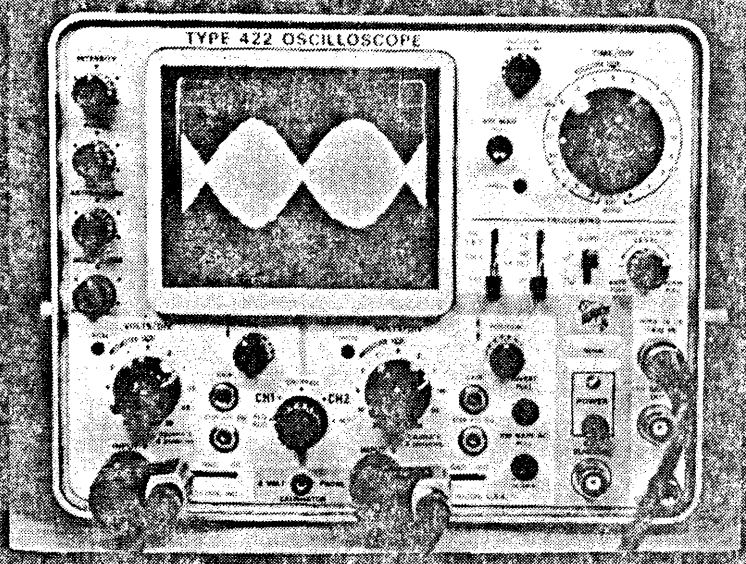
25

TRACK 00 SENSOR ADJUSTMENT

PROCEDURE 1:

— Locate Track 38 'Cat eyes'

— Step Out 38 Tracks

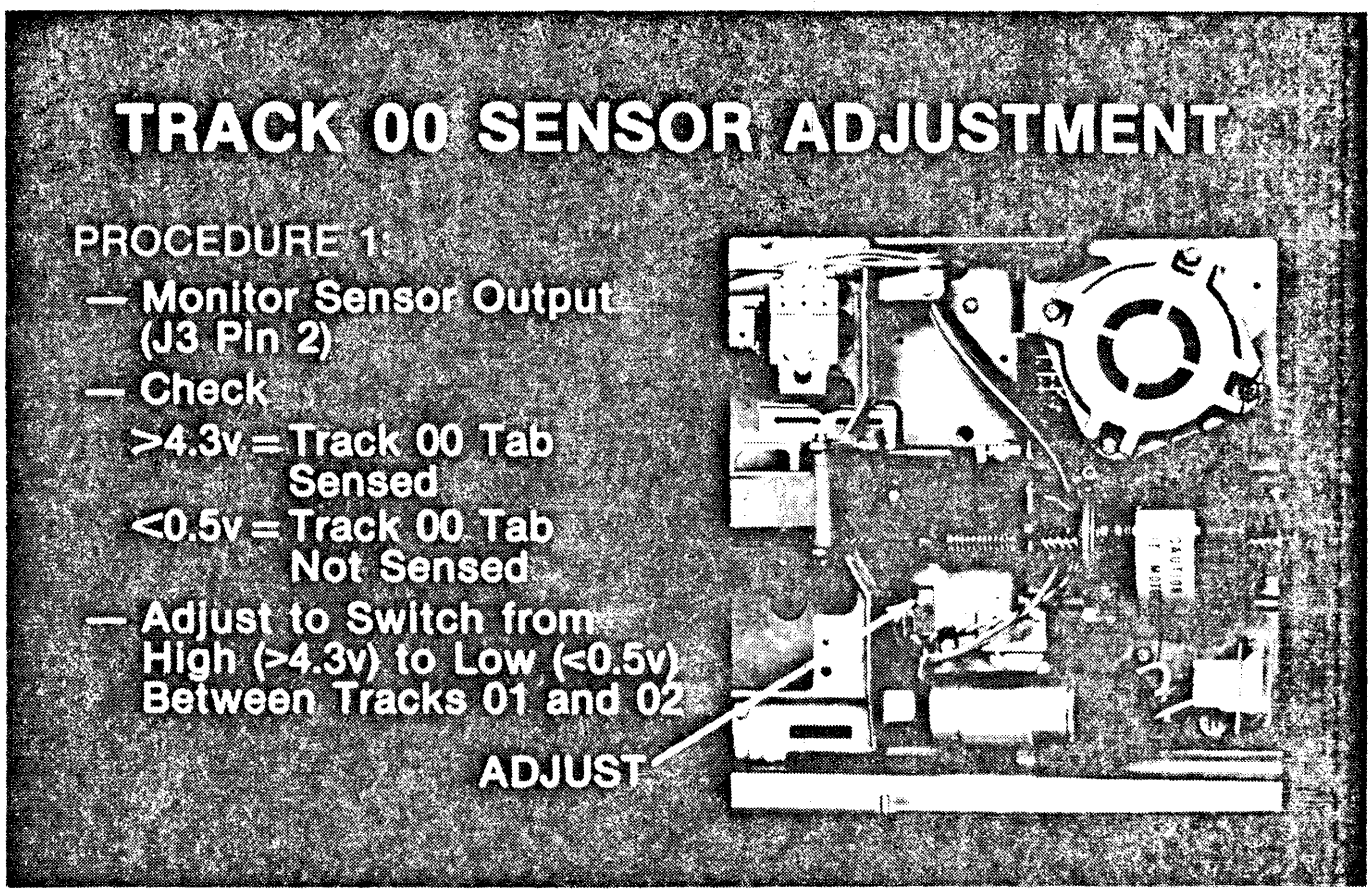


FOR THE FIRST ADJUSTMENT PROCEDURE, POWER THE UNIT OFF. LOCATE THE "CATEYES" BY MANUALLY ROTATING THE LEADSCREW CLOCKWISE, AS VIEWED FROM THE REAR OF THE STEPPER MOTOR, UNTIL THE HEAD CARRIAGE IS POSITIONED APPROXIMATELY 3/4 OF AN INCH FROM THE END OF THE STEPPER MOTOR. POWER THE UNIT ON AND INSERT THE ALIGNMENT DISKETTE.

STEP THE HEAD IN TO TRACK 38. MONITOR TEST POINTS 2 AND 3 WITH AN OSCILLOSCOPE, AS IN THE HEAD CARRIAGE ALIGNMENT PROCEDURE, TO ENSURE THAT THE HEAD CARRIAGE IS ACTUALLY AT TRACK 38. IF NOT, MANUALLY ROTATE THE LEAD SCREW IN AND OUT TO LOCATE THE "CATEYES" PATTERN.

FROM THIS POSITION, STEP OUT 38 TRACKS TO TRACK 00. THE ALIGNMENT DISKETTE HAS DATA WRITTEN ON TRACK 00 WHICH CAN ALSO BE USED TO LOCATE TRACK 00.

26



AFTER ESTABLISHING TRACK 00, MONITOR J3 PIN 2, WHICH IS THE OUTPUT OF THE OPTICAL SENSOR. A LOGICAL HIGH SIGNAL OF OVER 4.3 VOLTS INDICATES THAT THE TRACK 00 POSITION TAB ON THE HEAD CARRIAGE ASSEMBLY HAS BEEN SENSED. A LOW SIGNAL OF LESS THAN 0.5 VOLTS INDICATES THAT THE TRACK 00 POSITION TAB HAS NOT BEEN SENSED. IF THE SIGNAL IS LOW, LOOSEN THE OPTICAL SENSOR ASSEMBLY MOUNTING SCREW AND REPOSITION THE SENSOR SO THAT THE SIGNAL SWITCHES HIGH.

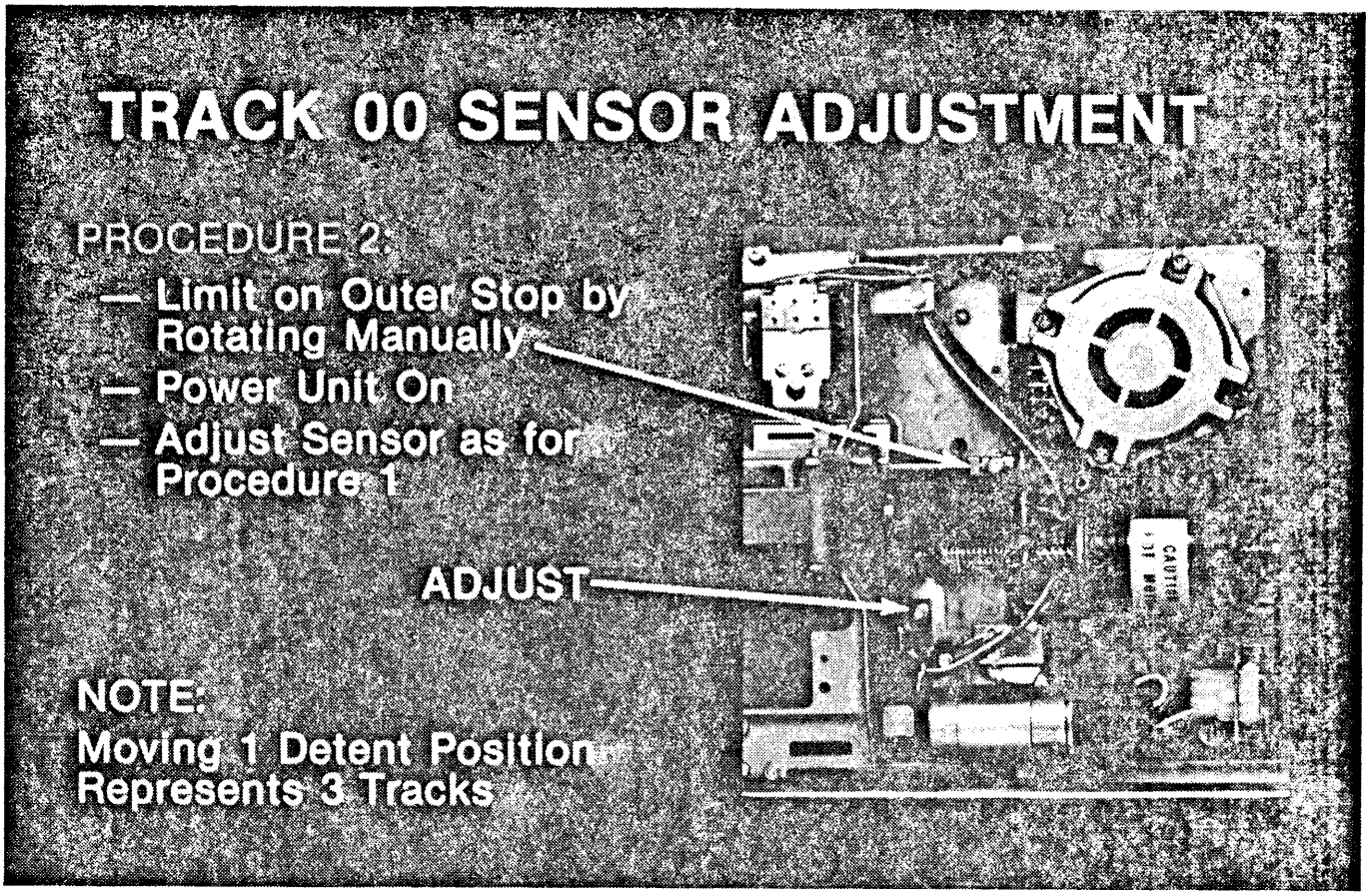
STEP IN ONE TRACK POSITION TO TRACK 01. THE SIGNAL VOLTAGE SHOULD STILL

BE HIGH. IF NOT, REPOSITION THE SENSOR.

STEP IN ONE MORE TRACK POSITION TO TRACK 02 AND THE SIGNAL SHOULD BE LOW, THAT IS LESS THAN 0.5 VOLTS. ADJUST IF NECESSARY AND TIGHTEN THE MOUNTING SCREWS.

FINALLY CHECK THE ADJUSTMENT BY STEPPING BETWEEN TRACKS 00, 01 AND 02 TO ENSURE THAT THE SIGNAL LEVEL CHANGES BETWEEN TRACKS 01 AND 02.

MISINDEXING OF TRACKS BY A FACTOR OF 3 IS SYMPTOMATIC OF AN INCORRECTLY ADJUSTED TRACK 00 SENSOR, CAUSED BECAUSE THE SENSOR SIGNAL IS GATED WITH PHASE "A." PHASE "A" IS ONLY TRUE FOR EVERY THIRD TRACK.



THE SECOND TRACK 00 SENSOR ADJUSTMENT PROCEDURE IS IDENTICAL EXCEPT THAT THE TRACK 00 POSITION IS ESTABLISHED FROM THE OUTER CARRIAGE STOP RATHER THAN THE ALIGNMENT DISKETTE.

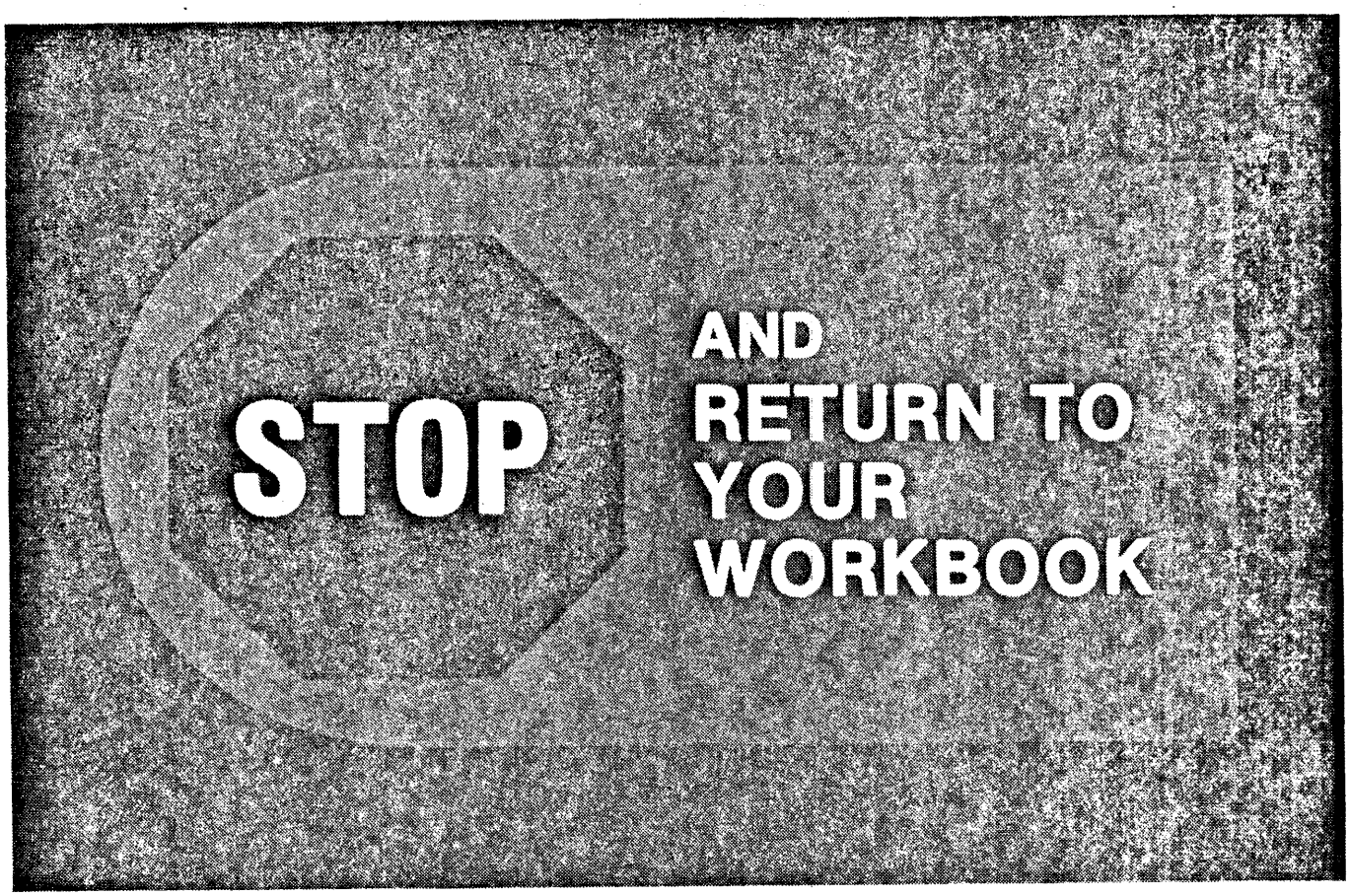
ESTABLISH TRACK 00 BY POWERING THE UNIT OFF, MANUALLY ROTATING THE LEAD SCREW CLOCKWISE, AS SEEN FROM THE REAR OF THE STEPPER MOTOR UNTIL THE HEAD CARRIAGE ASSEMBLY LIMITS ON THE OUTER STOP.

POWER THE UNIT ON AND THE HEAD CARRIAGE WILL DETENT AT TRACK 00. FROM THIS POINT, THE SENSOR ADJUSTMENT PROCEDURE IS IDENTICAL TO THE PREVIOUS PROCEDURE.

POWERING THE UNIT OFF AND ON IN EACH ADJUSTMENT ENSURES THAT THE LOGIC IS RESET AND STEPPER MOTOR PHASE "A" IS ACTIVE.

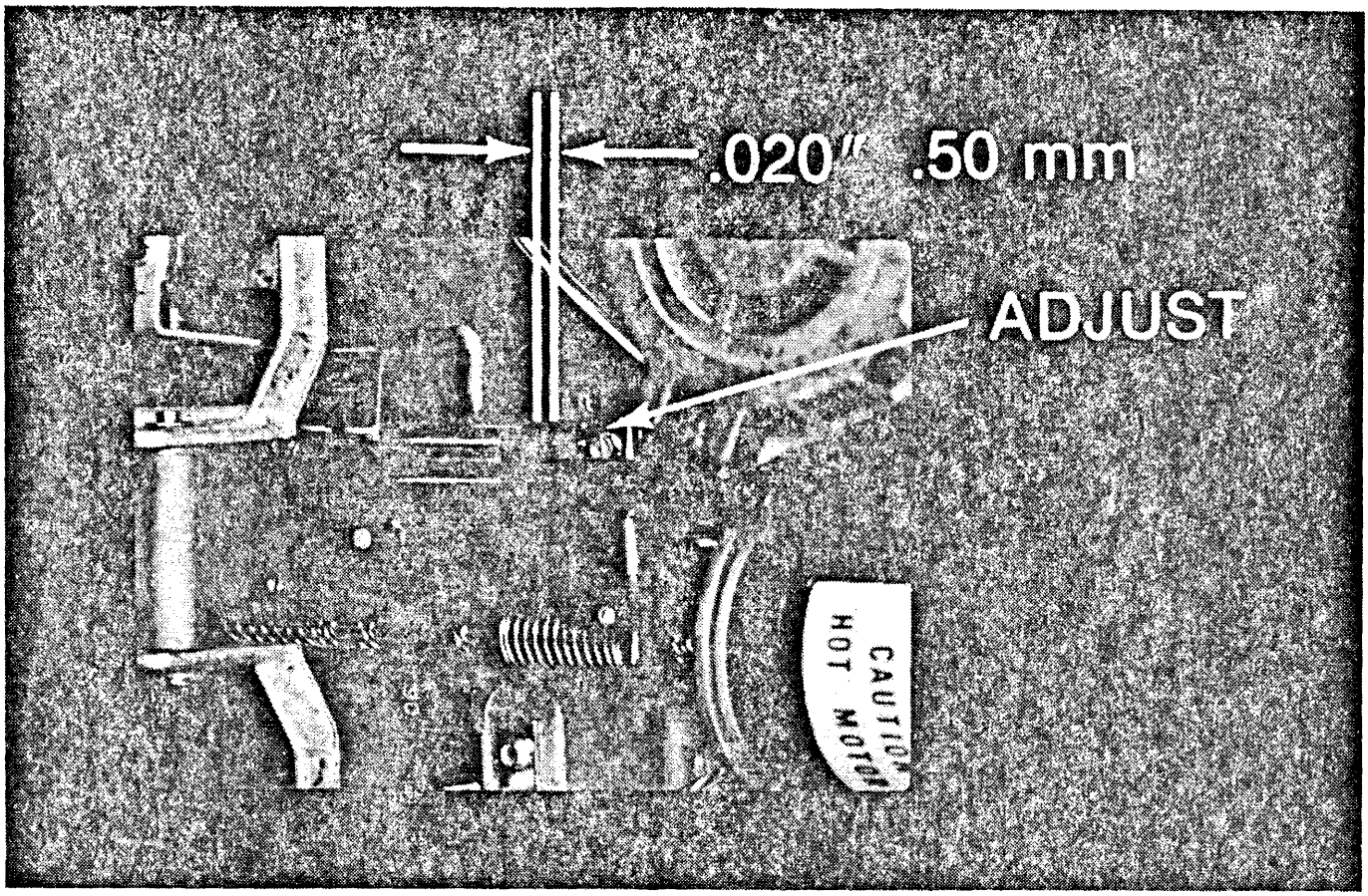
TURNING THE STEPPER MOTOR SHAFT MANUALLY REQUIRES SLIGHT PRESSURE TO OVERCOME THE EFFECT OF THE ELECTRICAL DETENT ON STEPPER MOTOR PHASE "A."

ALSO NOTE THAT WHEN THE SHAFT IS TURNED MANUALLY, EACH DETENT POSITION REPRESENTS A JUMP OF THREE TRACKS TO THE NEXT POSITION IN WHICH PHASE "A" IS ACTIVE.



STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

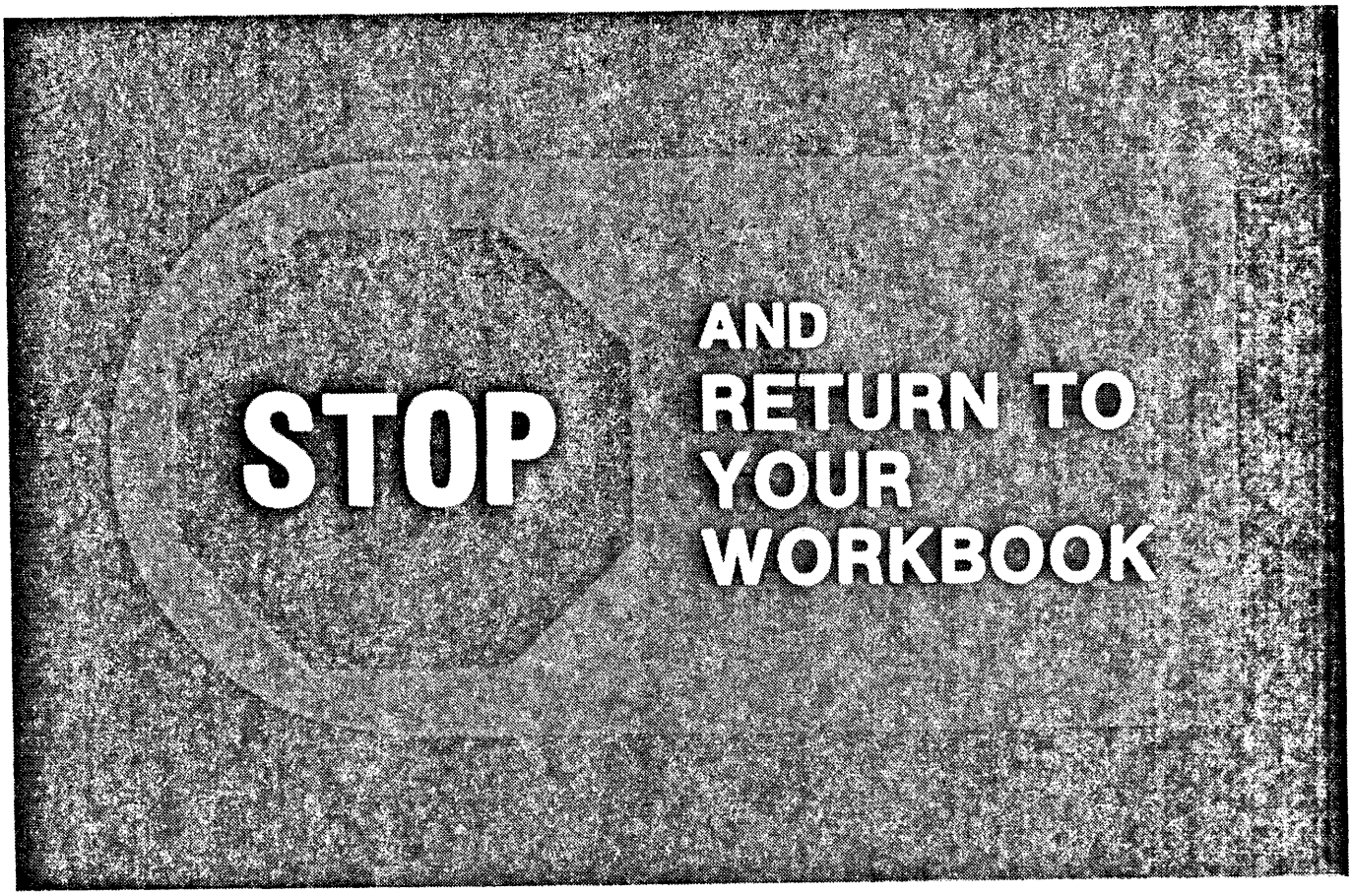
29



ADJUSTMENT OF THE HEAD CARRIAGE STOPS IS ACHIEVED BY MOVING THE STOP RAIL.

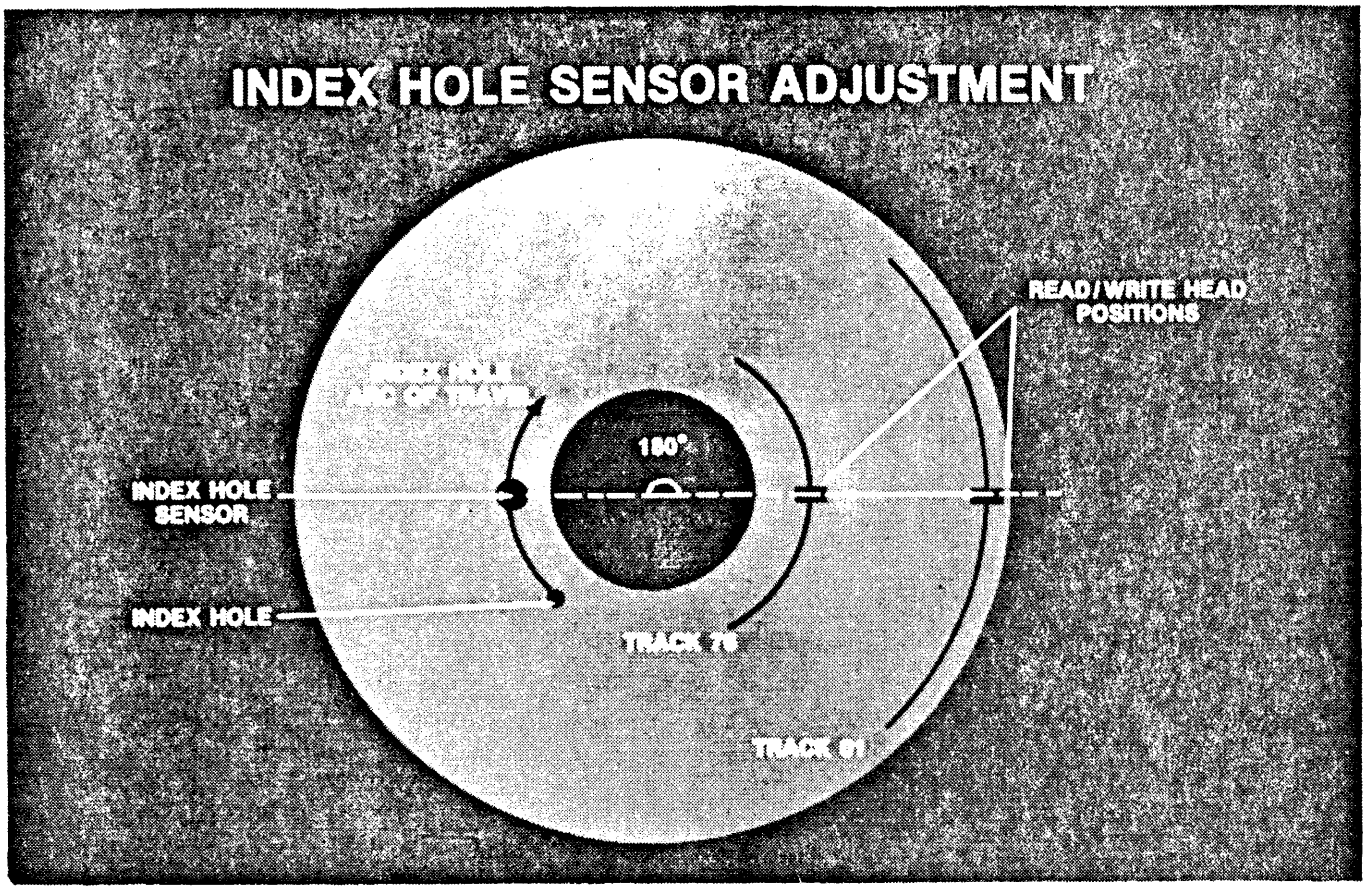
POSITION THE CARRIAGE ASSEMBLY TO TRACK 00. THERE SHOULD BE A 20 THOU CLEARANCE BETWEEN THE TAB ON THE STOP RAIL AND THE CARRIAGE ASSEMBLY. IF NECESSARY, LOOSEN THE CLAMPING SCREW AND MOVE THE RAIL ASSEMBLY TO PROVIDE THE CORRECT CLEARANCE.

NOTE THAT THERE IS AN INNER STOP AT THE OTHER END OF THE RAIL. THIS STOP PREVENTS ACCIDENTAL EXCESSIVE TRAVEL OF THE HEAD CARRIAGE ASSEMBLY.



STOP THE LECTURE AT THIS POINT AND COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

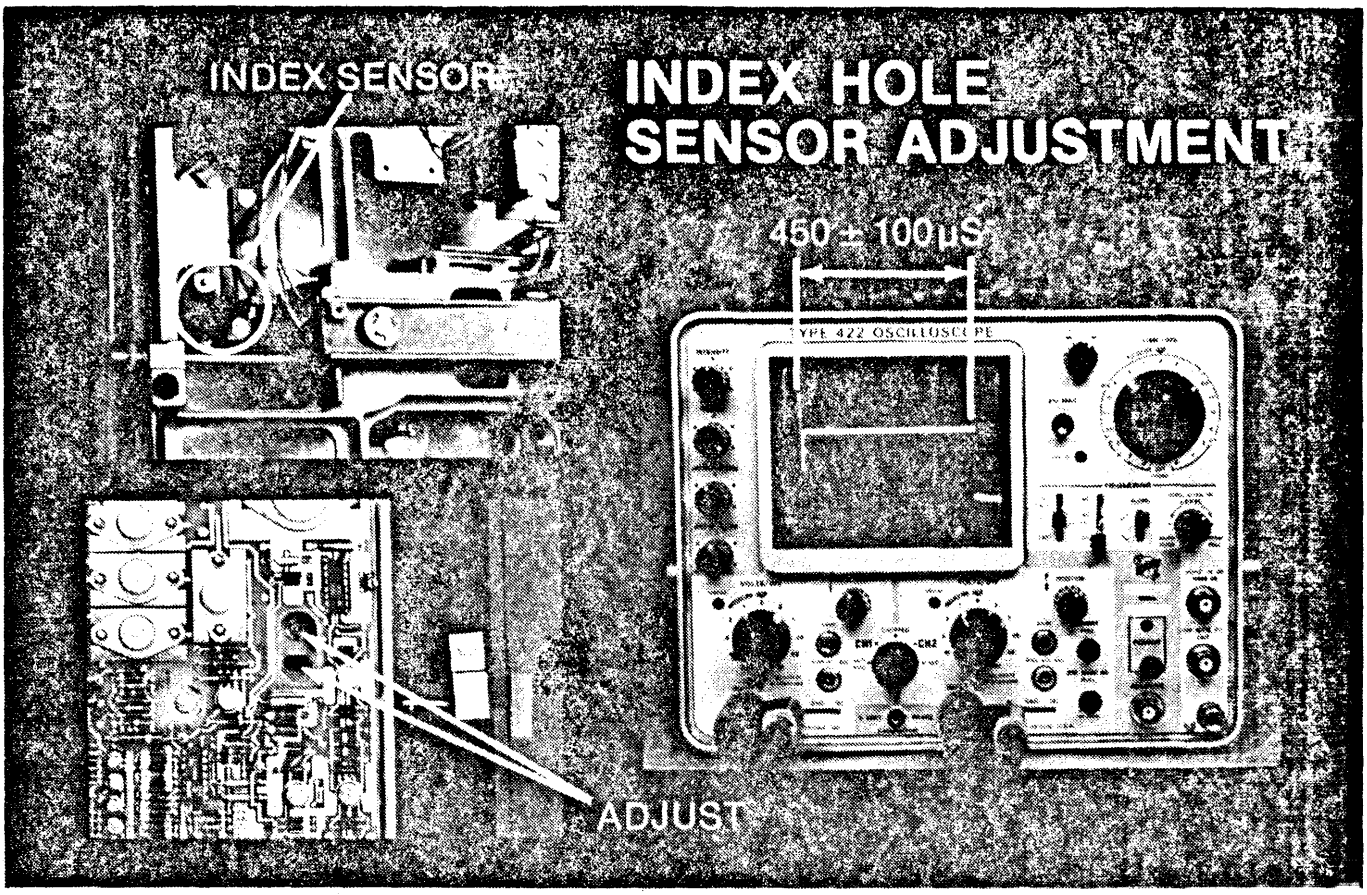
31



THE REMAINING ICMD ADJUSTMENT IS FOR THE INDEX HOLE SENSOR ASSEMBLY WHICH MUST BE LOCATED 180 DEGREES FROM THE READ/WRITE HEAD AND ALIGN WITH THE ARC OF TRAVEL OF THE INDEX HOLE IN THE DISKETTE.

THIS ADJUSTMENT AGAIN REQUIRES THE ALIGNMENT DISKETTE WHICH HAS A SINGLE FLUX CHANGE RECORDED AT THE END OF TRACKS 01 AND 76. THIS REFERENCE PULSE IS USED TO DETERMINE THE RELATIVE POSITION OF THE INDEX SENSOR. ANY DIFFERENCE BETWEEN THE RELATIVE TIMING OF THE PULSE READ FROM TRACK 01 AND TRACK 76 INDICATES THAT THE HEAD IS TRACKING ACROSS THE DISKETTE AT AN ANGLE.

32



TO PERFORM THE OPTICAL INDEX SENSOR ADJUSTMENT, SET UP THE OSCILLOSCOPE AS DESCRIBED IN THE ADJUSTMENT PROCEDURE IN THE TECHNICAL MANUAL. CHANNEL "A" SENSITIVITY IS SET TO 0.1 VOLTS/CM ON TEST POINT 2, CHANNEL "B" SENSITIVITY TO 2.0 VOLTS/CM ON U20 PIN 11, THE TIME BASE IS SET TO 50 MICROSECONDS/CM. THE SIGNAL ON CHANNEL "A" IS ADDED TO CHANNEL "B."

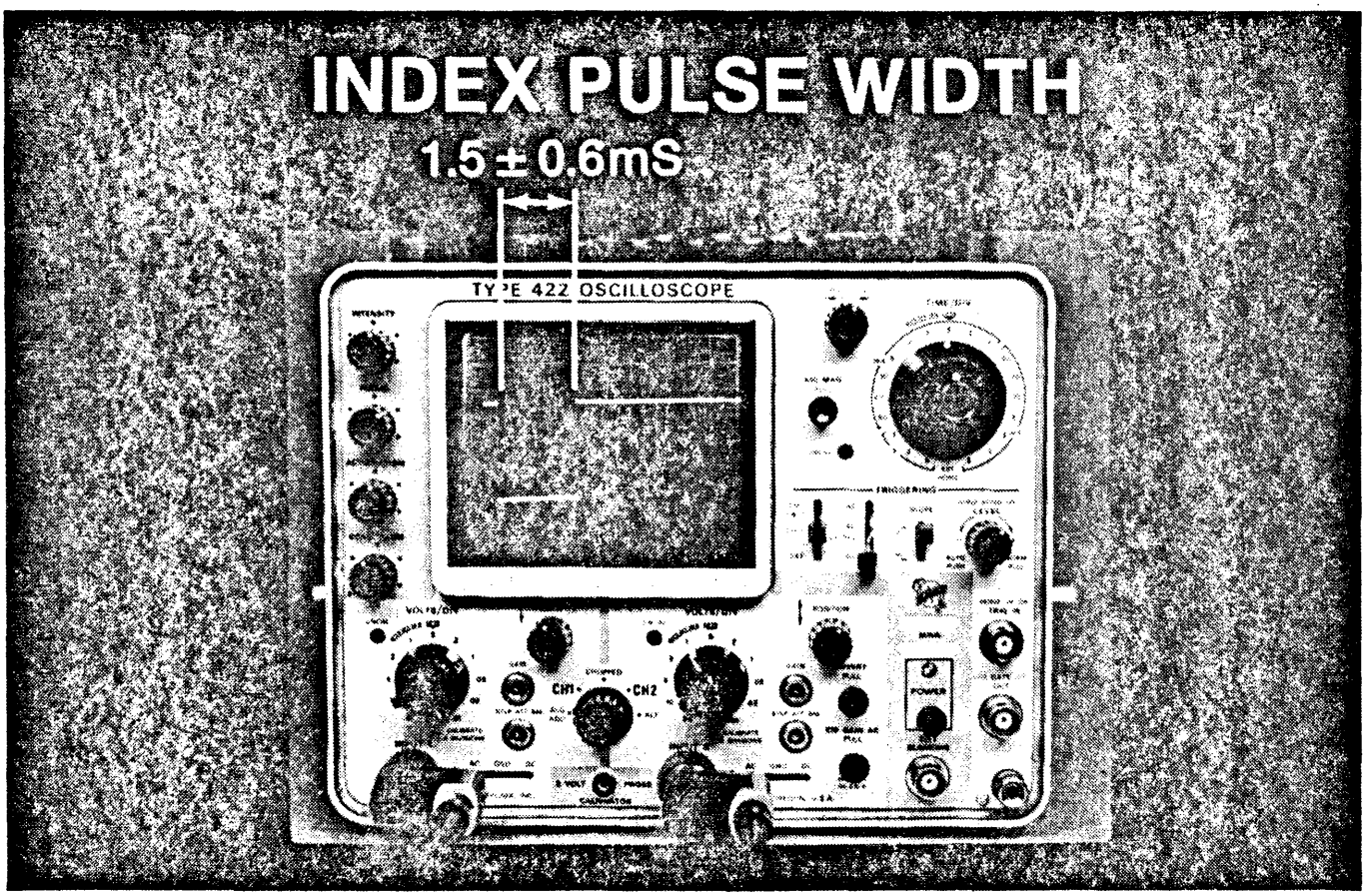
THE ALIGNMENT DISKETTE IS USED WITH A CONTINUAL READ OF TRACK 01. ADJUST THE TRIGGER ON INTERNAL POSITIVE TO GIVE A TRACE SIMILAR TO THE ONE SHOWN.

THE TIME BETWEEN THE PULSE READ FROM THE DISKETTE AND THE LEADING EDGE OF THE INDEX PULSE SHOULD BE 450 PLUS OR MINUS 100 MICROSECONDS.

IF THE TIMING OF THE INDEX PULSE IS OUTSIDE SPECIFICATION, LOOSEN THE ALLEN HEAD SCREW WHICH MOUNTS THE SENSOR TO THE LOWER BASE CASTING AND MOVE THE SENSOR TO ACHIEVE THE CORRECT TIMING.

ADJUSTMENT OF THE OPTICAL INDEX SENSOR MAY CHANGE THE ADJUSTMENT OF THE INDEX PULSE WIDTH.

33



MEASURING U20 PIN 11 WITH THE OSCILLOSCOPE SHOULD INDICATE A PULSE WIDTH OF 1.5 PLUS OR MINUS 0.6 MILLISECONDS. IF THE PULSE WIDTH IS OUTSIDE THESE LIMITS, MOVE THE "LED" ON THE TOP PLATE ASSEMBLY TO OBTAIN BETTER ALIGNMENT WITH THE SENSOR.

ONLY SLIGHT ADJUSTMENT CAN BE MADE. IF THE PULSE WIDTH IS STILL

INCORRECT, ENSURE THAT THE "LED" AND SENSOR ARE CLEAN. IF THERE IS STILL NO IMPROVEMENT IT IS PROBABLY NECESSARY TO REPLACE THE SENSOR.

34

TEST SELECTED RESISTORS

Circuit	Function	TS Location	Resistor Range	Select Value
U5 Ready Logic	Timing*	R44	13-25K	196 msec. ± 4 msec. positive output pulse U5-5*
U5 Ready Logic	Timing	R45	10-18K	145 msec. negative output pulse U5-4*
U9 Write Enable	Delay	R84	2K nominal	450 microsecond delay between Write Enable U30-6 and U9-6 (leading edges)*
U9 Write Enable	Delay	R82	2K nominal	450 microsecond delay between Write Enable U30 PIN 6 and U9-6 (trailing edges)*
Q4 Read Logic	Dc/offset	R19	2.2-13K	Select for ±3 millivolt balance of U1 pins 5 to 6**
U4 Read Amp	Gain	R49	80.6 nominal	Gain of 100**
U4 Read Amp	Gain	R48	Typically an open	Gain of 100**

TS

*This pulse can be seen only when disk is speeding up.
**Monitor waveforms at TP2 and TP3.

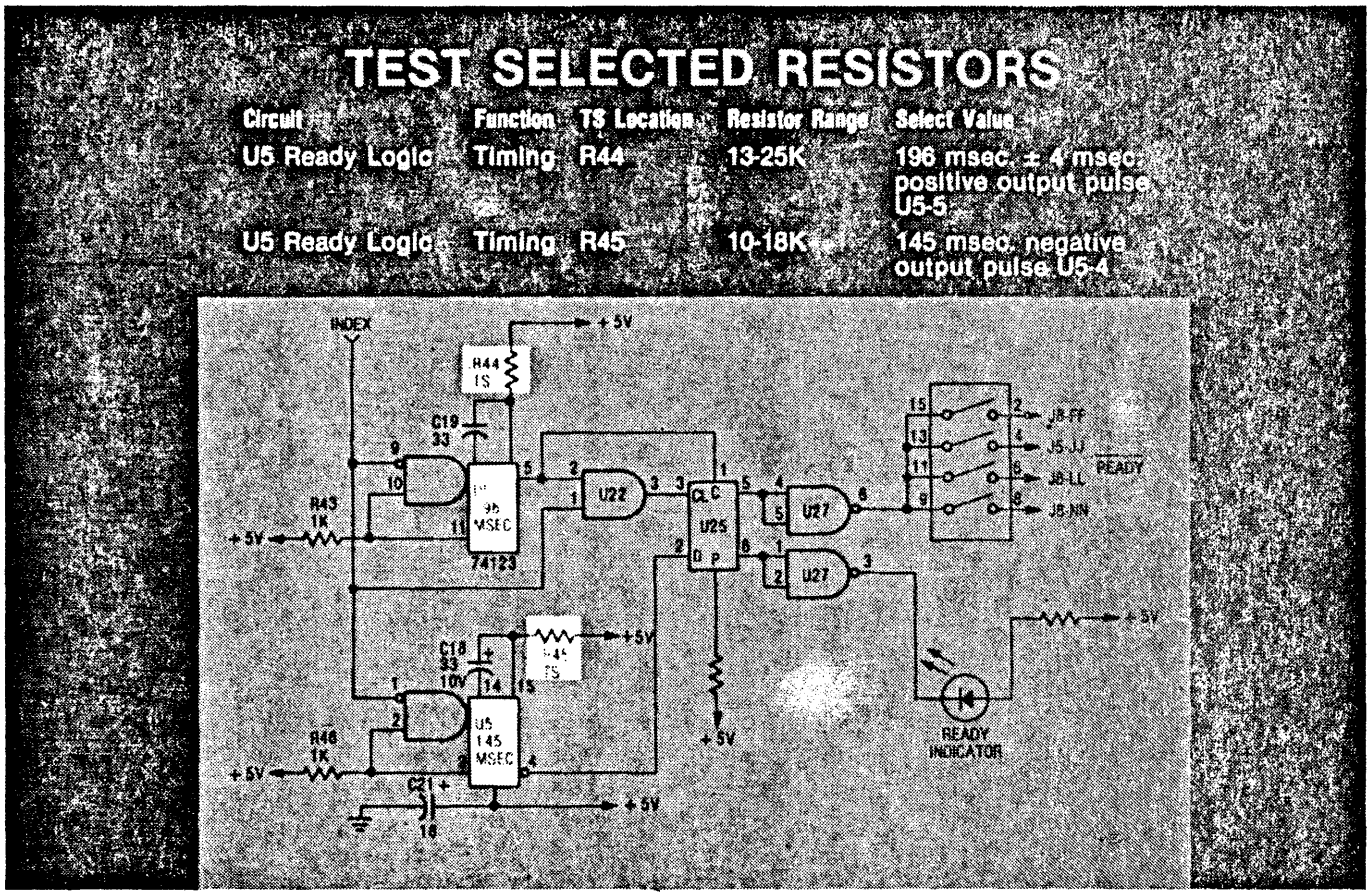
IN ADDITION TO THE ADJUSTMENT PROCEDURES PREVIOUSLY DESCRIBED, YOU WILL REMEMBER THAT DURING THE DESCRIPTION OF THE LOGIC CIRCUITS, WE MENTIONED A NUMBER OF TEST SELECTED RESISTORS.

TEST SELECTED RESISTORS ARE REQUIRED TO COMPENSATE FOR THE SLIGHT VARIATIONS IN THE CHARACTERISTICS OF CERTAIN INTEGRATED CIRCUITS OF THE SAME TYPE AND PART NUMBER.

THERE IS A TABLE IN VOLUME 1, SECTION FOUR OF THE TECHNICAL MANUAL WHICH DEFINES THE CIRCUIT, FUNCTION, LOCATION AND RESISTANCE RANGE FOR EACH

TEST SELECTED RESISTOR. THE SAME TABLE ALSO SPECIFIES THE MEASUREMENT REQUIRED TO DETERMINE THE CORRECT VALUE.

35



LET US LOOK MORE CLOSELY AT AN EXAMPLE. ASSUME IC U5 HAS BEEN CHANGED. THERE ARE TWO ASSOCIATED TEST SELECTED RESISTORS, R44 AND R45.

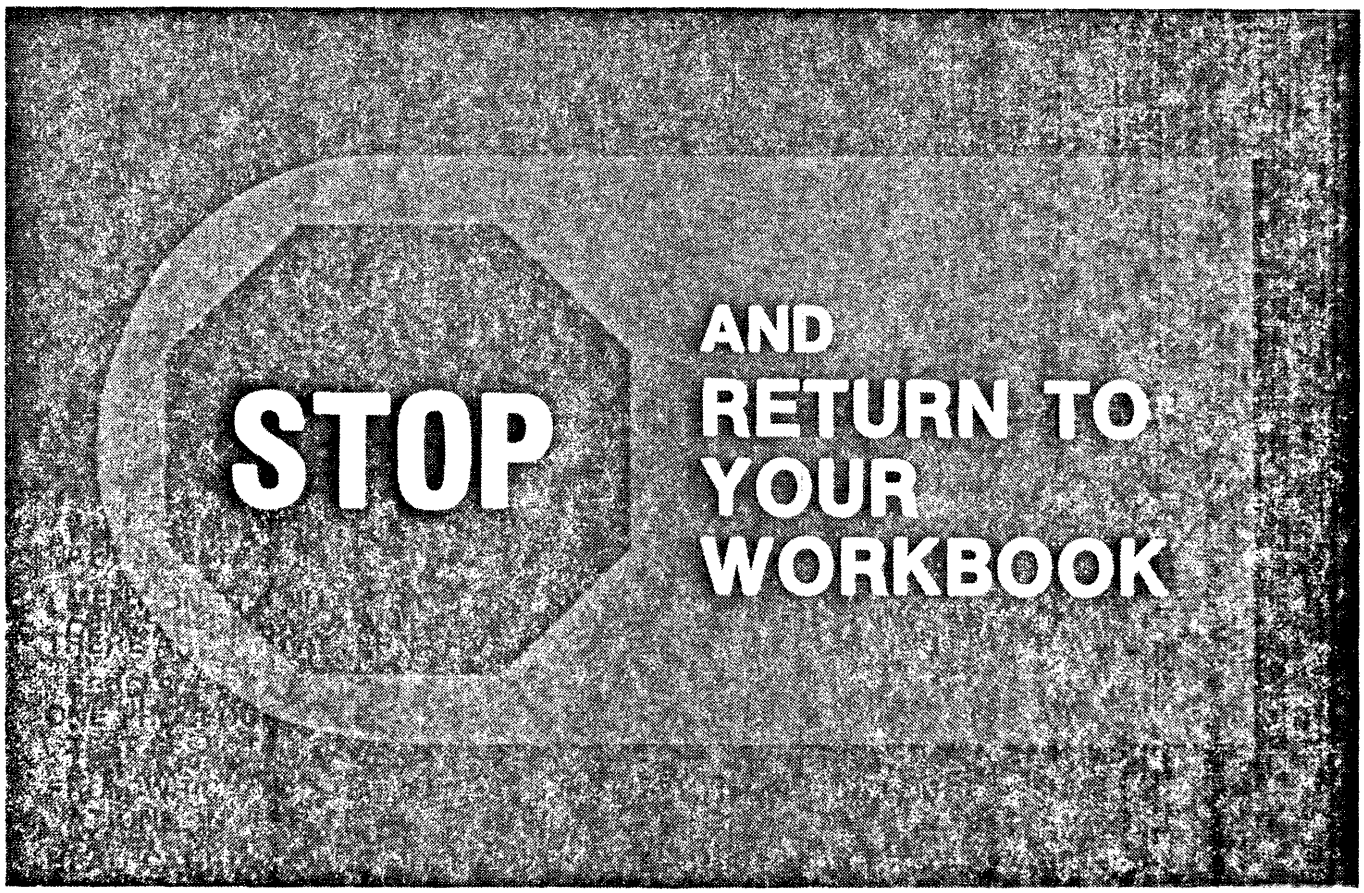
THE VALUE OF R44 IS DETERMINED BY MEASURING THE SIGNAL AT U5 PIN 5 TO GIVE A 196 mS POSITIVE PULSE, WITHIN A PLUS OR MINUS 4mS TOLERANCE. THERE IS ALSO A NOTE TO SAY THAT THIS PULSE CAN ONLY BE SEEN WHEN THE DISK IS SPEEDING UP.

IN FACT THIS RESISTOR DETERMINES THE TIMEOUT PERIOD FOR THE LOW SPEED ONE SHOT, WHICH SHOULD ONLY TIME OUT WHEN THE DISKETTE IS NOT UP TO SPEED.

THE VALUE OF R44 IS EXPECTED TO BE SOMEWHERE BETWEEN 13 AND 25K OHMS. THE PRECISE VALUE HAS TO BE DETERMINED LARGELY BY TRIAL AND ERROR, AND IN MANY CASES, NO CHANGE WILL BE REQUIRED.

THE PROCEDURE FOR R45 IS SIMILAR. MEASUREMENT OF U5 PIN 4 SHOULD INDICATE A 145 mS NEGATIVE OUTPUT PULSE. AS THIS IS THE HIGH SPEED ONE SHOT, IT SHOULD ALWAYS TIME OUT UNLESS THE DISKETTE IS OVER SPEED. CONSEQUENTLY THIS MEASUREMENT CAN BE MADE AT ANY TIME WHEN THE DISKETTE IS ROTATING.

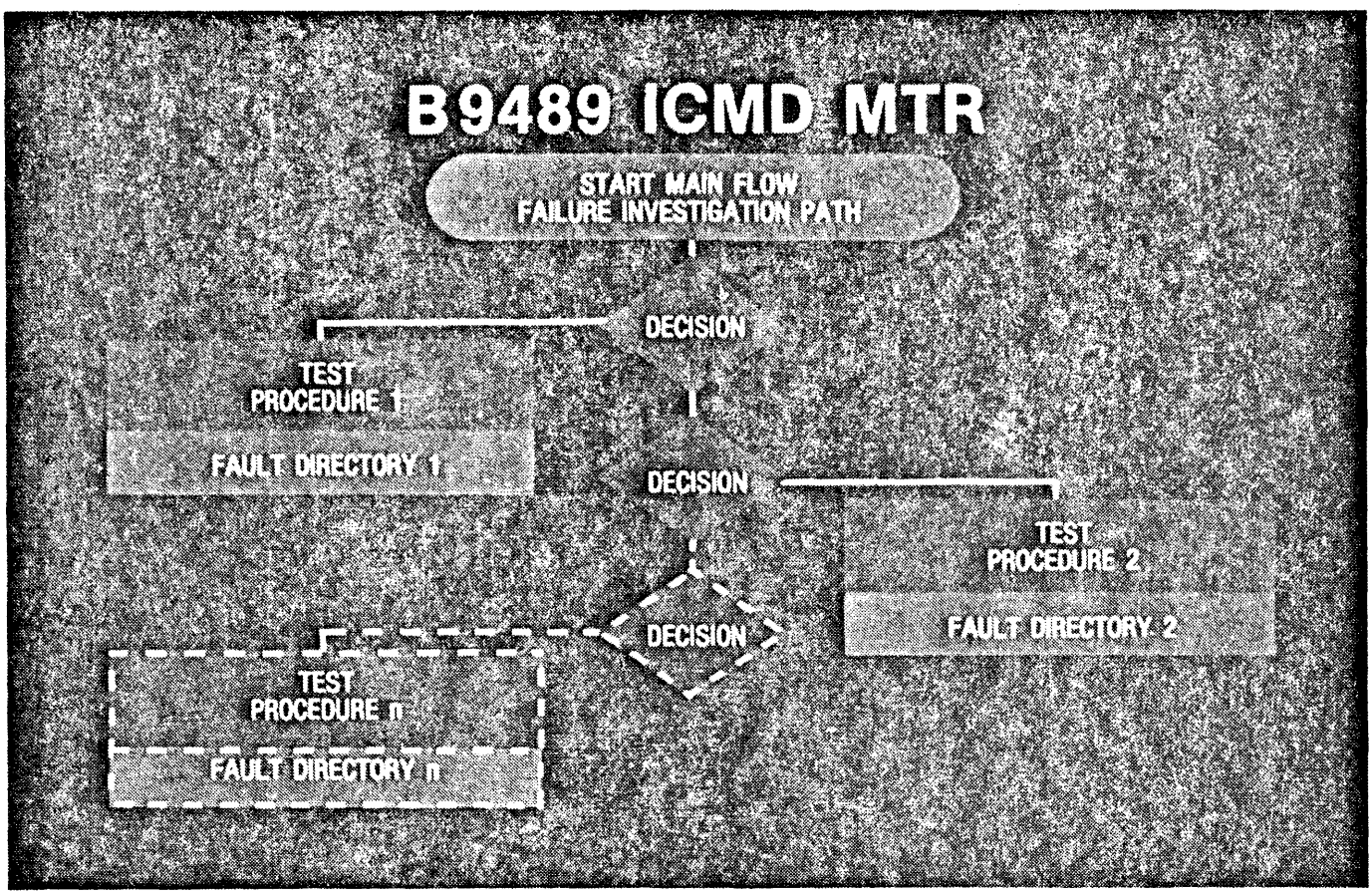
36



THIS CONCLUDES THE ADJUSTMENT PROCEDURES FOR THE ICMD UNIT.

STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION BEFORE CONTINUING.

37



THE MAINTENANCE PHILOSOPHY FOR THE ICMD UNIT, IS TO USE THE MAINTENANCE TEST ROUTINE TO DETECT AND IDENTIFY A FAILURE TO THE COMPONENT LEVEL ON SITE.

THE MTR CONSISTS OF A MAIN FLOW OR FAILURE INVESTIGATION PATH WHICH DIRECTS THE ENGINEER TO ONE OF A NUMBER OF GUIDED TEST PROCEDURES. EACH TEST PROCEDURE HAS AN ASSOCIATED FAILURE DIRECTORY.

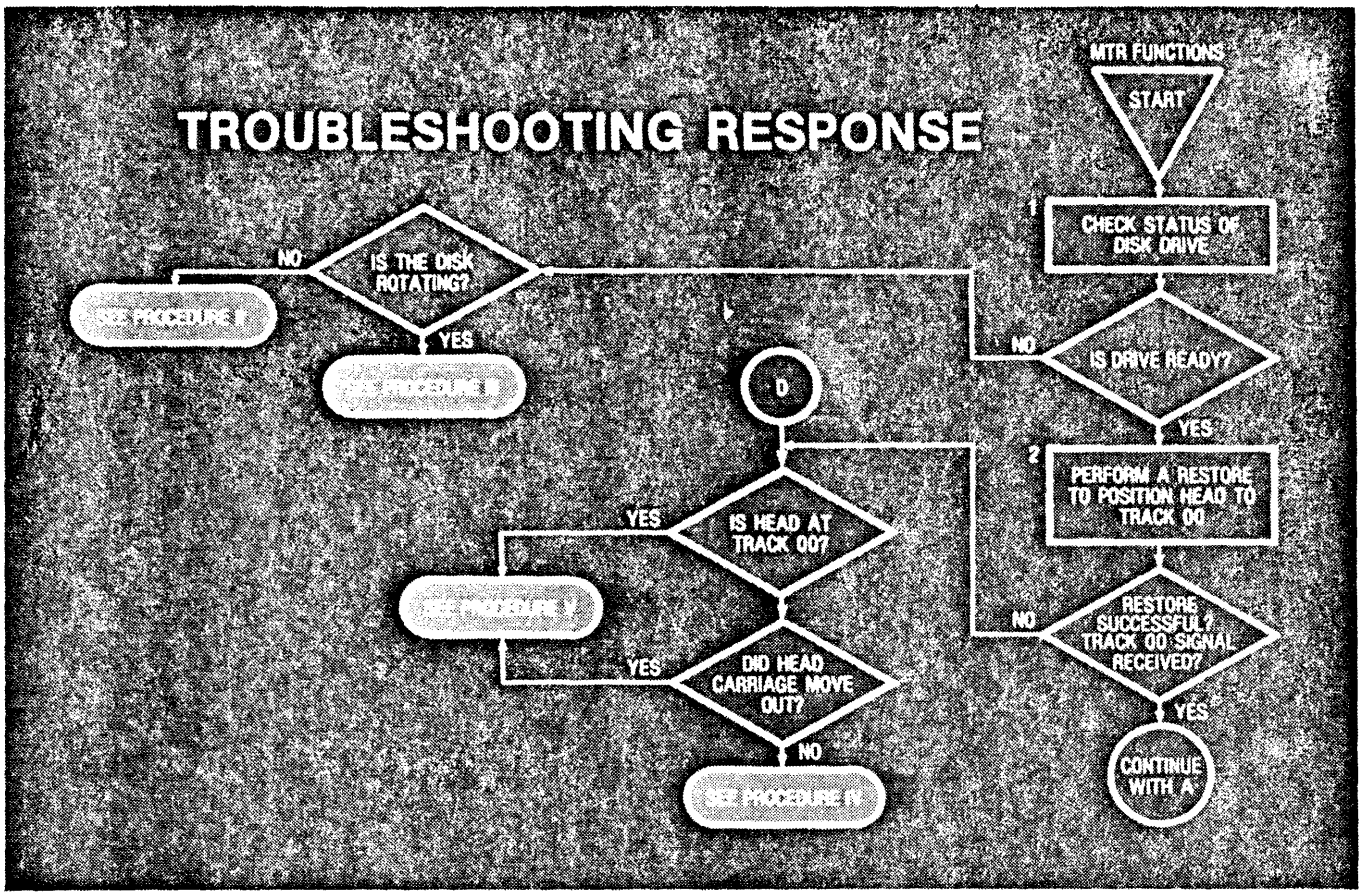
BECAUSE THE DRIVE ITSELF HAS NO LOCAL MAINTENANCE FUNCTIONS, THESE FUNCTIONS ARE PROVIDED BY TEST ROUTINES FROM THE HOST SYSTEM. PRECISE IMPLEMENTATION OF TEST ROUTINES MAY VARY SLIGHTLY FROM SYSTEM TO SYSTEM, BUT THIS SHOULD NOT AFFECT THE PROCEDURES THEMSELVES.

38

TO DEMONSTRATE HOW THESE PROCEDURES FUNCTION, LET US TAKE A SIMPLE EXAMPLE OF A FAILURE AND USE THE MTR TO DETERMINE THE CAUSE.

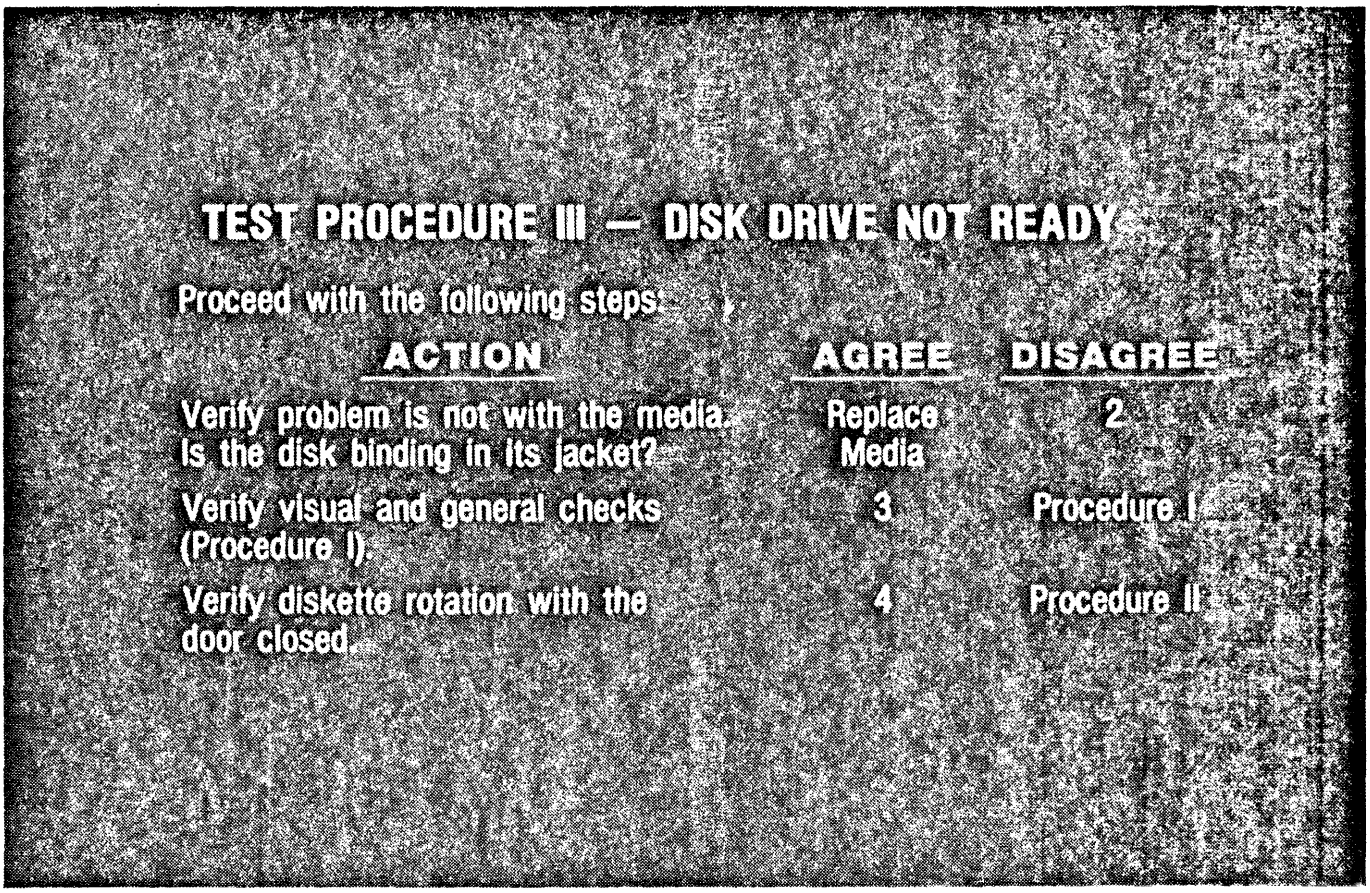
FOR OUR EXAMPLE, A DRIVE UNIT IS CONTINUALLY REPORTED BY THE SYSTEM AS "NOT READY." A QUICK VISUAL CHECK SHOWS THAT THE DOOR IS CLOSED CORRECTLY AND THE DISKETTE IS ROTATING.

39



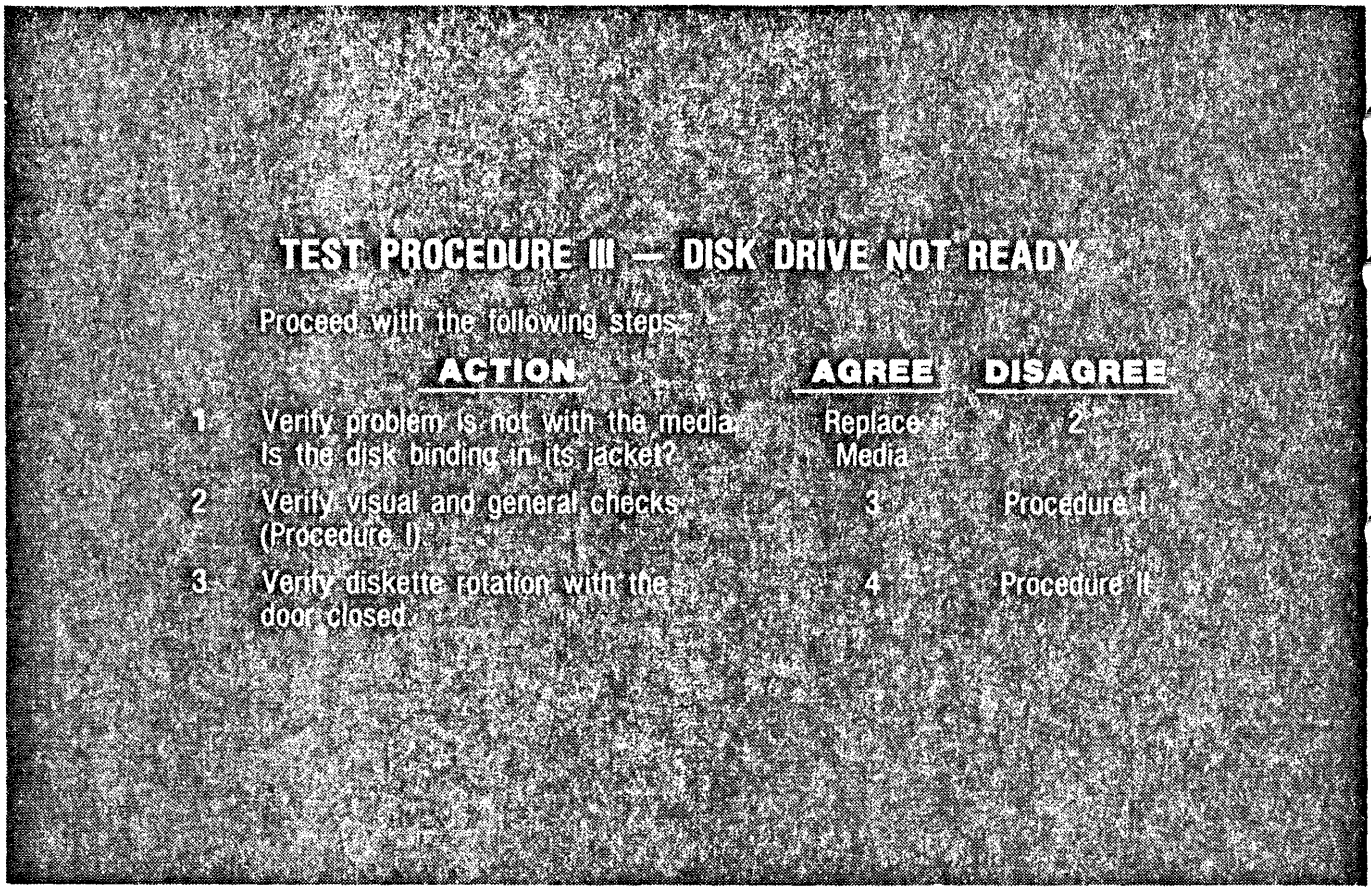
STARTING AT THE BEGINNING OF THE MAIN FLOW, THE FIRST QUESTION ASKS "IS DRIVE READY?" IN OUR CASE THE ANSWER IS NO. THE NEXT QUESTION ASKS "IS THE DISK ROTATING?" THE DISK IS ROTATING SO THE FLOW DIRECTS US TO GO TO TEST PROCEDURE 3.

40



TEST PROCEDURE 3, LIKE THE OTHER TEST PROCEDURES, IS A NARRATIVE FLOW WHICH GIVES EACH STEP A NUMBER, THE ACTION TO BE TAKEN AND THE EXPECTED RESULT. DEPENDENT ON THE RESULT, THE ENGINEER IS DIRECTED TO THE NEXT STEP, A PROCEDURE, OR A FAILURE DIRECTORY REFERENCE.

41



TEST PROCEDURE III — DISK DRIVE NOT READY

Proceed with the following steps:

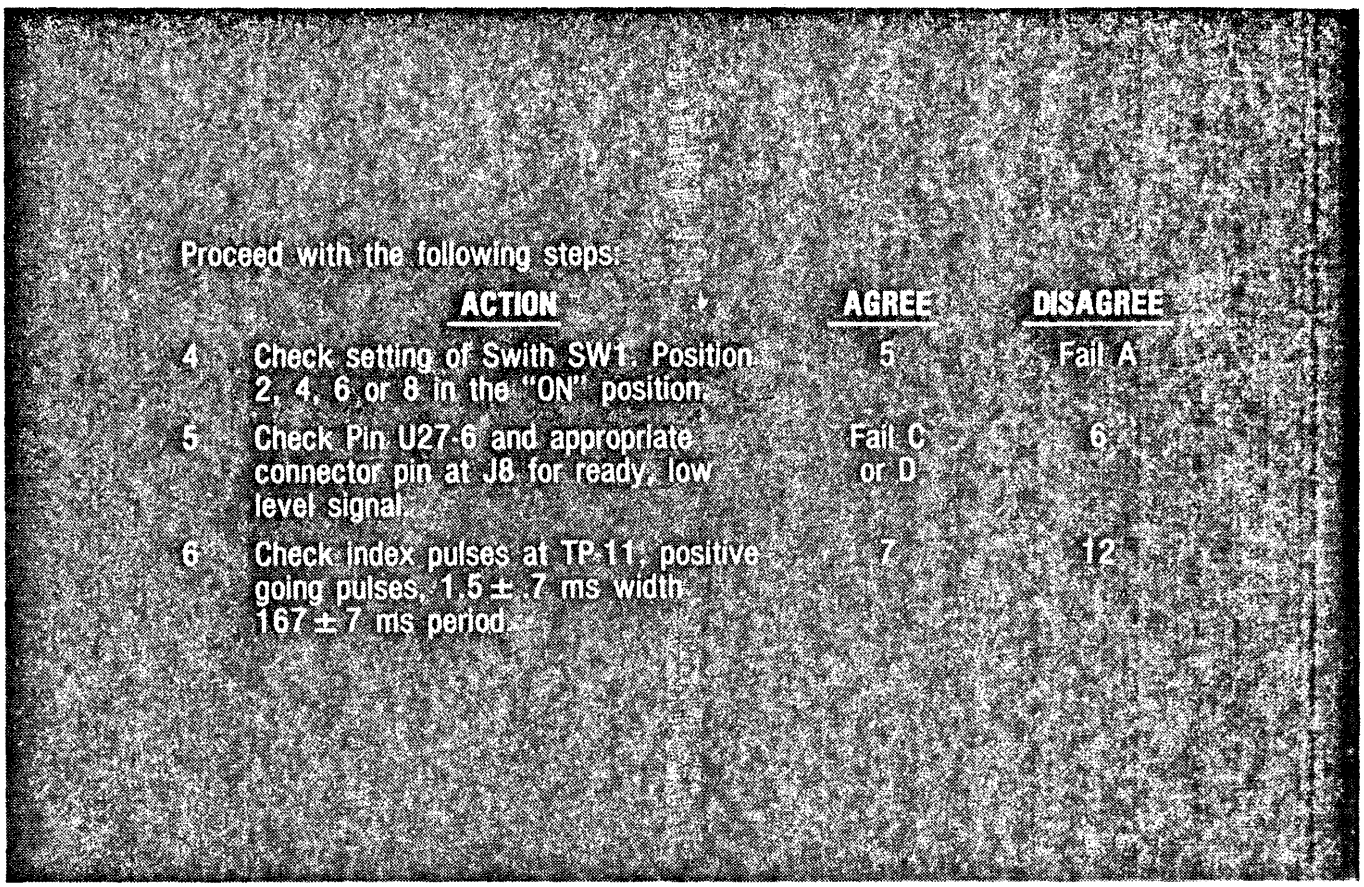
	ACTION	AGREE	DISAGREE
1	Verify problem is not with the media. Is the disk binding in its jacket?	Replace Media	2
2	Verify visual and general checks (Procedure I)	3	Procedure I
3	Verify diskette rotation with the door closed	4	Procedure II

STEP 1 ASKS US TO CHECK THE DISKETTE TO ENSURE THAT IT IS NOT WORN OR DAMAGED. IF IN DOUBT, TRY USING ANOTHER DISKETTE. SINCE IN OUR EXAMPLE THE DISKETTE IS IN GOOD CONDITION, WE GO TO STEP 2.

STEP 2 ASKS FOR VERIFICATION OF THE VISUAL AND GENERAL CHECKS WHICH ARE DEFINED IN PROCEDURE 1. THIS INCLUDES A CHECK OF OPTIONS, OBVIOUS MECHANICAL FAILURES, ETC. FOR THE PURPOSE OF OUR EXAMPLE, NO FAILURES ARE DETERMINED BY PROCEDURE 1, SO WE GO ON TO STEP 3.

STEP 3 ASKS FOR VERIFICATION THAT THE DISKETTE IS ROTATING AND THE DOOR IS CLOSED. THIS IS AGREED AND THE PROCEDURE DIRECTS US TO STEP 4.

42



Proceed with the following steps:

	ACTION	AGREE	DISAGREE
4	Check setting of Swith SW1. Position 2, 4, 6 or 8 in the "ON" position.	5	Fail A
5	Check Pin U27-6 and appropriate connector pin at J8 for ready, low level signal.	Fail C or D	6
6	Check index pulses at TP-11, positive going pulses, 1.5 ± .7 ms width 167 ± 7 ms period.	7	12

STEP 4 ASKS FOR THE POSITION OF THE UNIT DESGINATE SWITCHES WHICH RETURN THE READY STATUS SIGNAL TO THE CONTROLLER TO BE CHECKED. AS THIS IS CORRECT, WE PROCEED TO STEP 5.

STEP 5 MONITORS THE READY STATUS SIGNAL TO ENSURE THAT THE DRIVE REALLY IS "NOT READY" AND ENSURE THAT IT IS NOT AN INTERFACE OR CABLE FAILURE. IN OUR EXAMPLE THE SIGNAL IS HIGH SO WE DISAGREE AND GO TO STEP 6.

STEP 6 CHECKS THE INDEX PULSES AT TEST POINT 11. BUT FOR OUR EXAMPLE, NO PULSES ARE PRESENT AND THE MTR HAS DETECTED THE FAILURE. TO BETTER DEFINE THE CAUSE, THE PROCEDURE GOES TO STEP 12.

43

	ACTION	AGREE	DISAGREE
12	Check index sensor LED, J7-3 to J7-1, for an open or shorted junction.	Fail E	Fail F

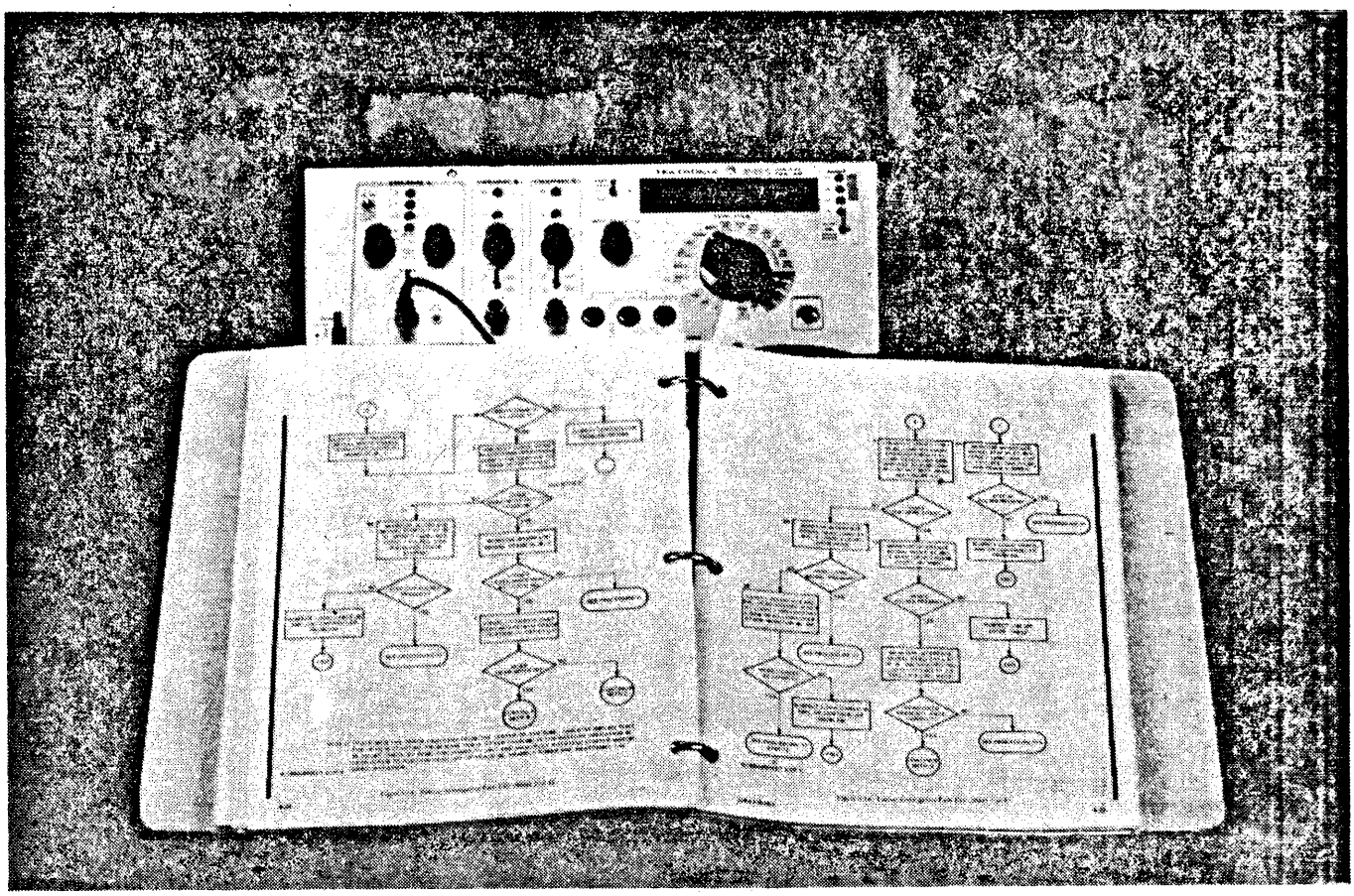
Failure Directory III

A. Set unit designate switch, SW-1.
B. Set drive motor pulley for either 50 or 60 Hz as needed.
C. Check Cable J8, loose or defective.
D. Check ready indicator lamp or Q27 and U27.
E. **Replace index sensor LED.**
F. Index sensor photo transistor.

STEP 12 CHECKS THE "LED" LIGHT SOURCE OF THE INDEX SENSOR. THE "LED" IS CHECKED FOR DIODE ACTION WITH A "BDM" OR OTHER OHM-METER. IN OUR EXAMPLE, THE "LED" IS OPEN CIRCUIT. FAILURE "E" IS INDICATED.

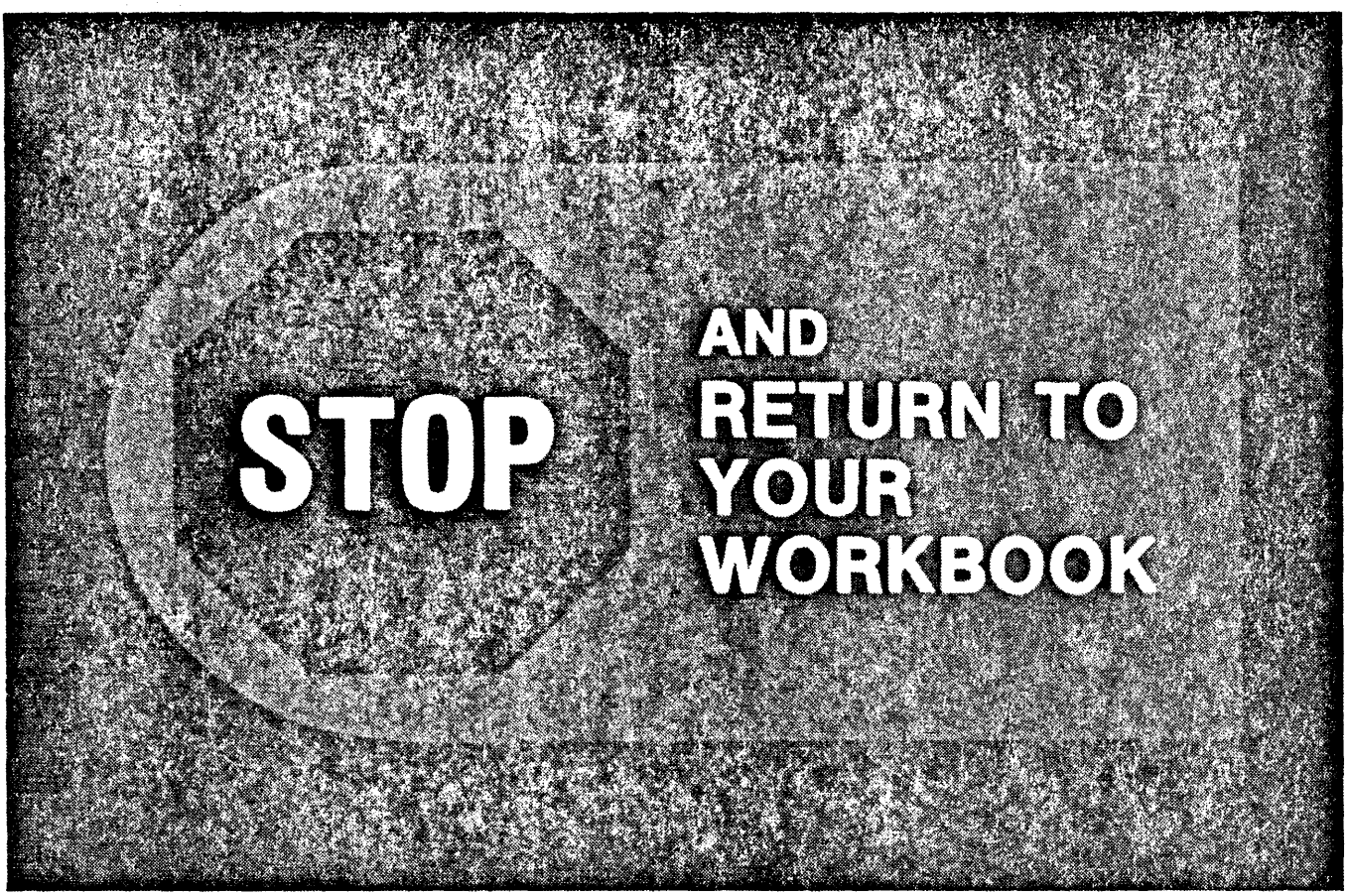
EACH TEST PROCEDURE HAS AN ASSOCIATED FAILURE DIRECTORY SIMILAR TO THE ONE SHOWN. NOT SURPRISINGLY FOR OUR SIMPLE EXAMPLE WITH FAILURE "E," WE ARE DIRECTED TO REPLACE THE FAILED "LED."

44



USE THE UNIT SCHEMATICS TO FOLLOW THE FAULT ISOLATION PROCEDURE AS YOU RUN THE MTR. THE KNOWLEDGE YOU HAVE GAINED DURING THE THEORY OF OPERATION PART OF THIS TRAINING PROGRAM WILL ASSIST YOU IN DETERMINING THE PRECISE CAUSE OF A FAILURE. OFTEN, YOU WILL BE ABLE TO MAKE ADDITIONAL MEASUREMENTS WHICH MAY HELP FURTHER REDUCE THE NUMBER OF SUSPECTS GIVEN IN THE FAILURE DIRECTORY.

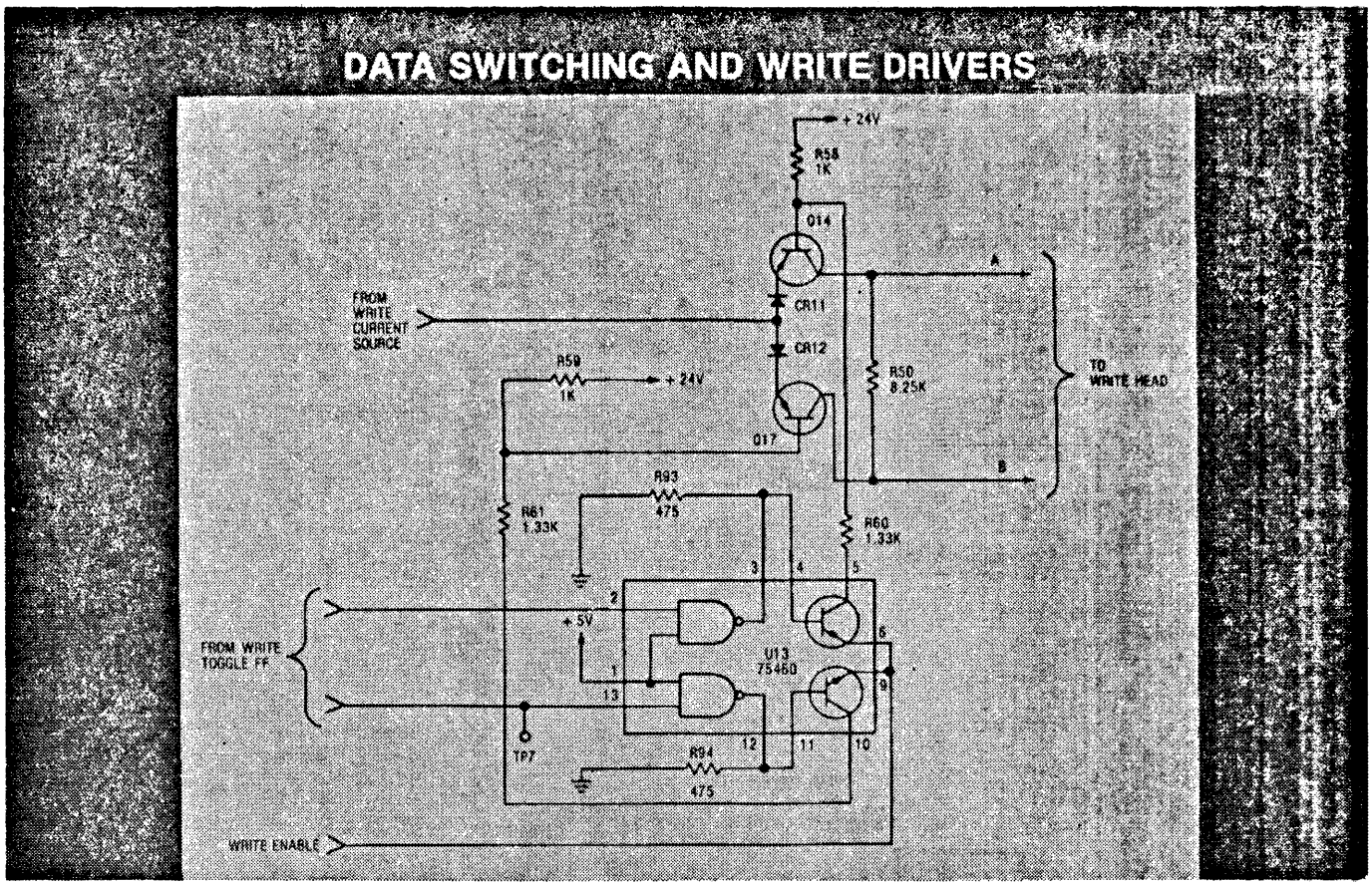
45



THIS CONCLUDES THE THIRD AND FINAL LECTURE. STOP THE LECTURE AT THIS POINT AND RETURN TO YOUR WORKBOOK. COMPLETE THE PRACTICE FOR THIS SECTION.

40

DATA SWITCHING AND WRITE DRIVERS

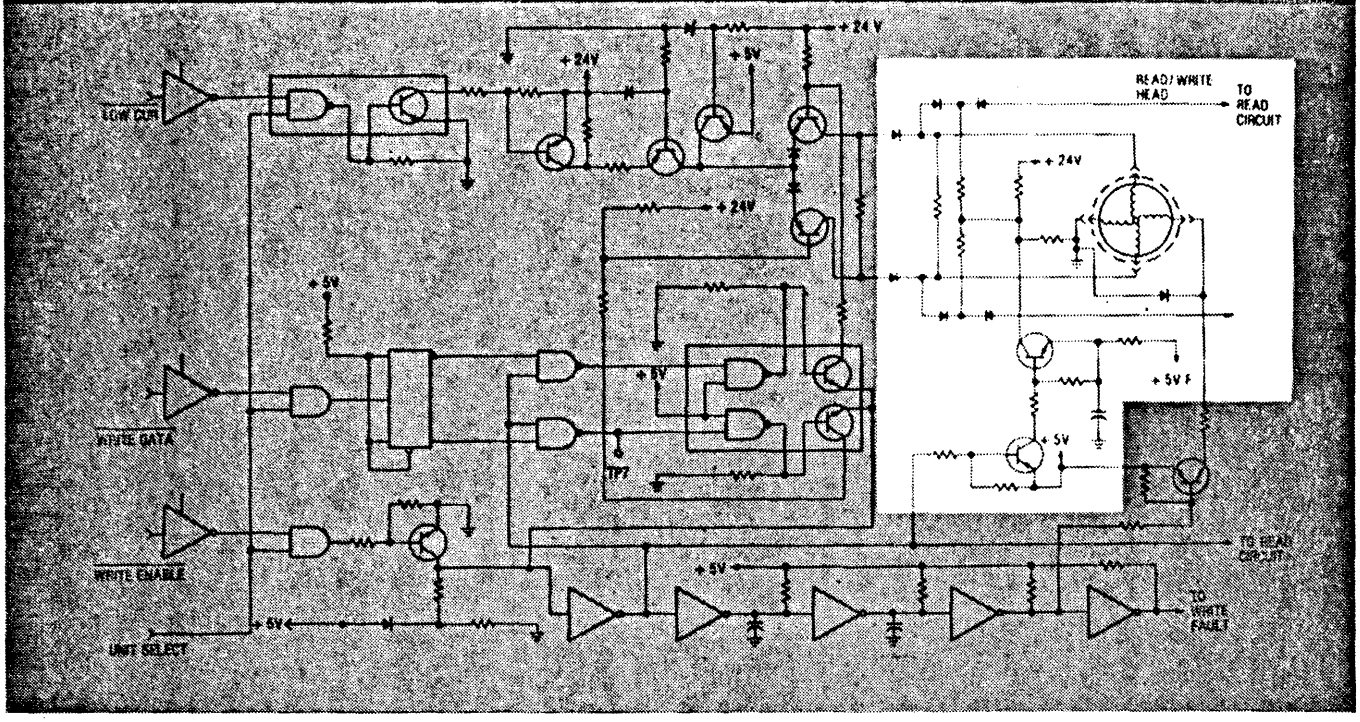


THE TWO DATA SWITCHING DRIVERS ARE LOCATED IN A SINGLE IC PACKAGE U13. BECAUSE THE TWO INPUTS TO U13 ARE THE SET AND RESET OUTPUTS OF THE WRITE TOGGLE FLIP FLOP, ONLY ONE DRIVER CAN CONDUCT AT A TIME. Q14 AND Q17 ARE THE WRITE DRIVER TRANSISTORS. AS ONLY ONE OF THEM CAN CONDUCT AT ANY TIME, Q14 AND Q17 ARE USED TO DETERMINE THE DIRECTION OF CURRENT FLOW THROUGH THE WRITE HEAD. WITH Q14 CONDUCTING, CURRENT FLOWS TO THE WRITE HEAD THROUGH "A" AND NOT "B." WITH Q17 CONDUCTING CURRENT FLOWS TO THE WRITE HEAD THROUGH "B" AND NOT "A."

THE CURRENT FOR THE WRITE DRIVERS IS SUPPLIED FROM THE WRITE CURRENT SOURCE WHICH IS DETAILED LATER.

41

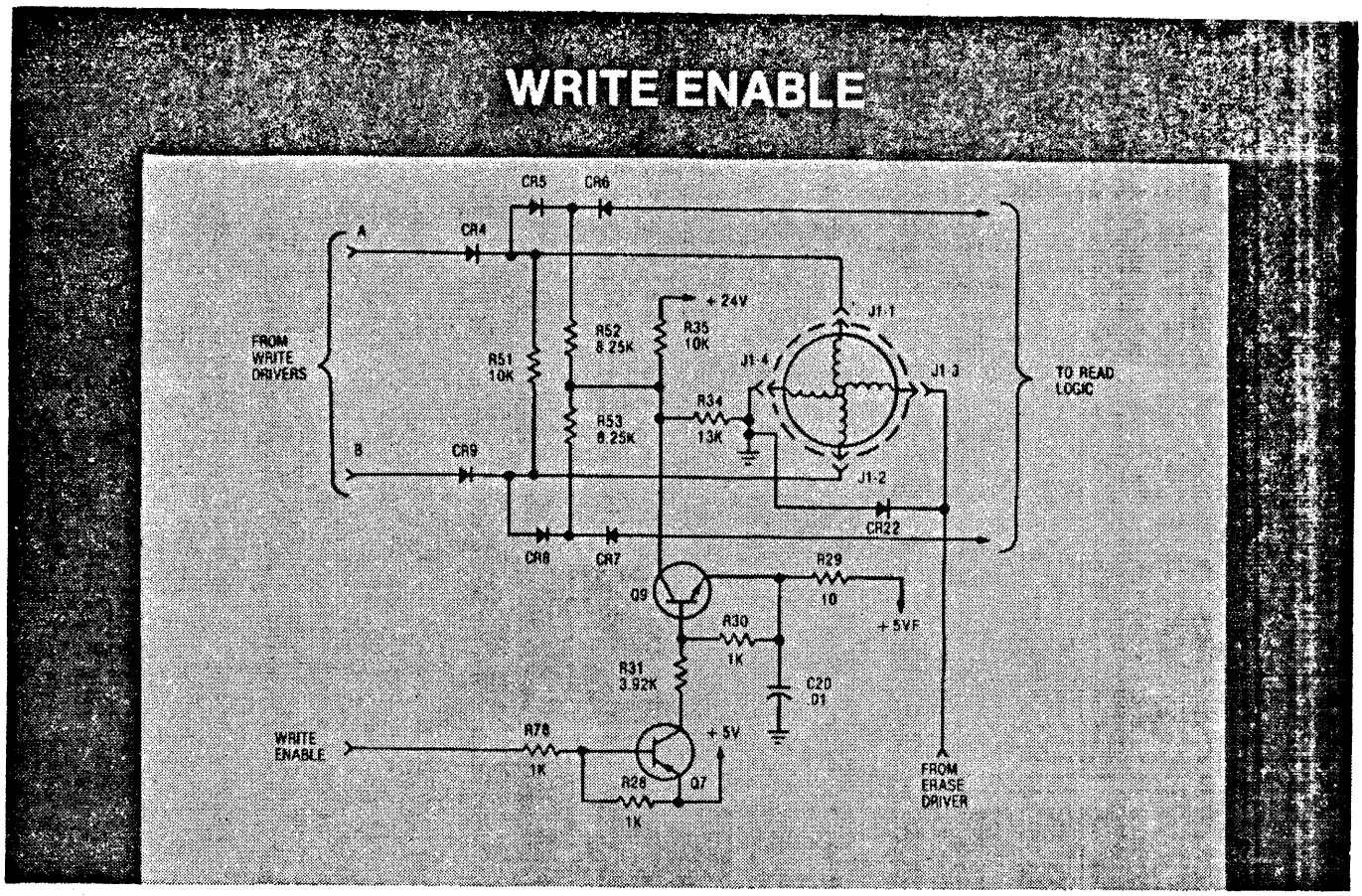
WRITE LOGIC — WRITE ENABLE



THE WRITE ENABLE LOGIC IS BASICALLY THE SAME AREA OF LOGIC DESCRIBED EARLIER IN THE READ LOGIC SECTION OF THIS LECTURE. AS YOU WILL REMEMBER, THE WRITE ENABLE LOGIC DETERMINES WHETHER THE READ/WRITE IS READ OR WRITE ENABLED ACCORDING TO THE CONDITION OF THE HOST SYSTEM CONTROLLER SIGNAL WRITE ENABLE.

42

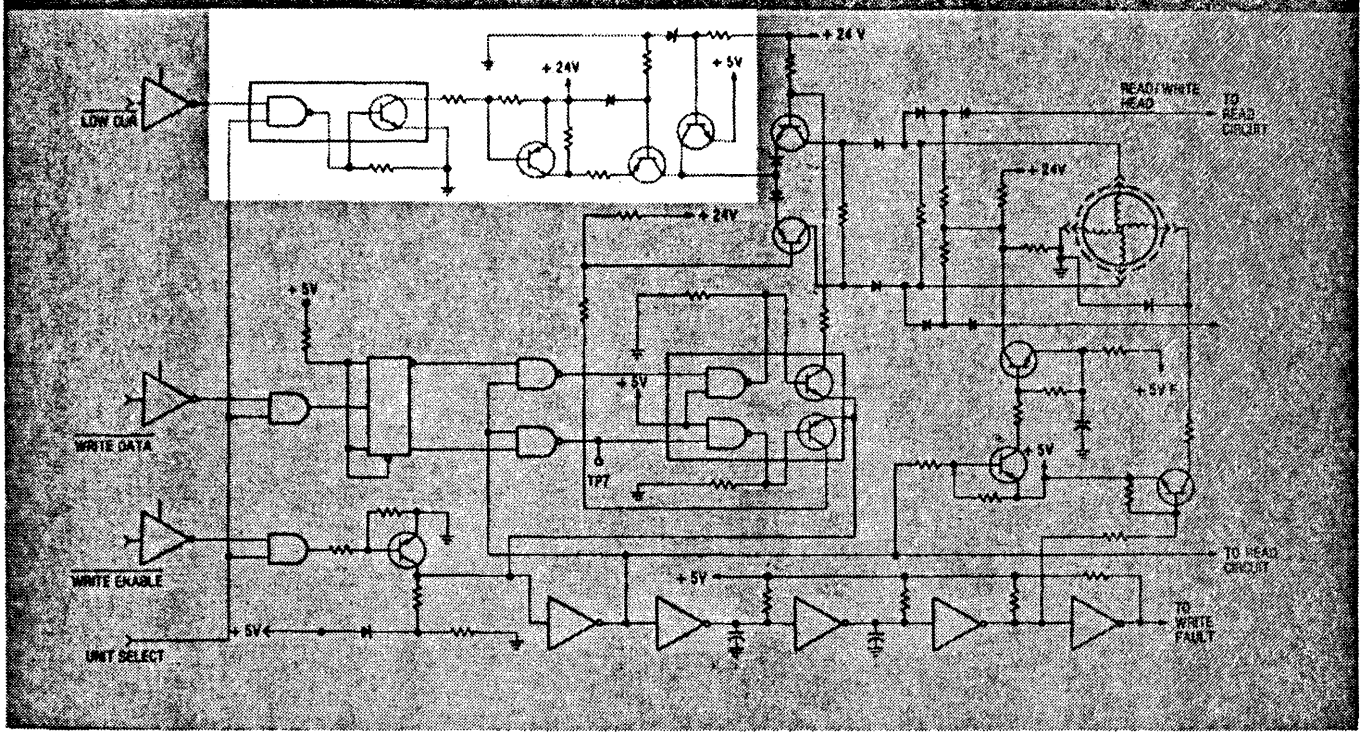
WRITE ENABLE



THE SIGNAL "WRITE ENABLE" ACTS THROUGH TRANSISTORS Q7 AND Q9 TO REVERSE BIAS CR5 AND CR8 WHICH DISABLES THE READ LOGIC. CURRENT FROM THE WRITE DRIVERS SWITCHES BETWEEN SIGNALS "A" AND "B" TO REVERSE THE CURRENT FLOW THROUGH THE WRITE HEAD FOR EACH CLOCK AND DATA ONE BIT. THE CHANGE IN THE DIRECTION OF CURRENT THROUGH THE READ HEAD CHANGES THE DIRECTION OF THE MAGNETIC FIELD PRODUCED BY THE HEAD. THE CHANGE IN THE DIRECTION OF THE MAGNETIC FIELD CAUSES A SIMULTANEOUS CHANGE IN THE DIRECTION OF MAGNETIC FLUX RECORDED ON THE DISKETTE.

43

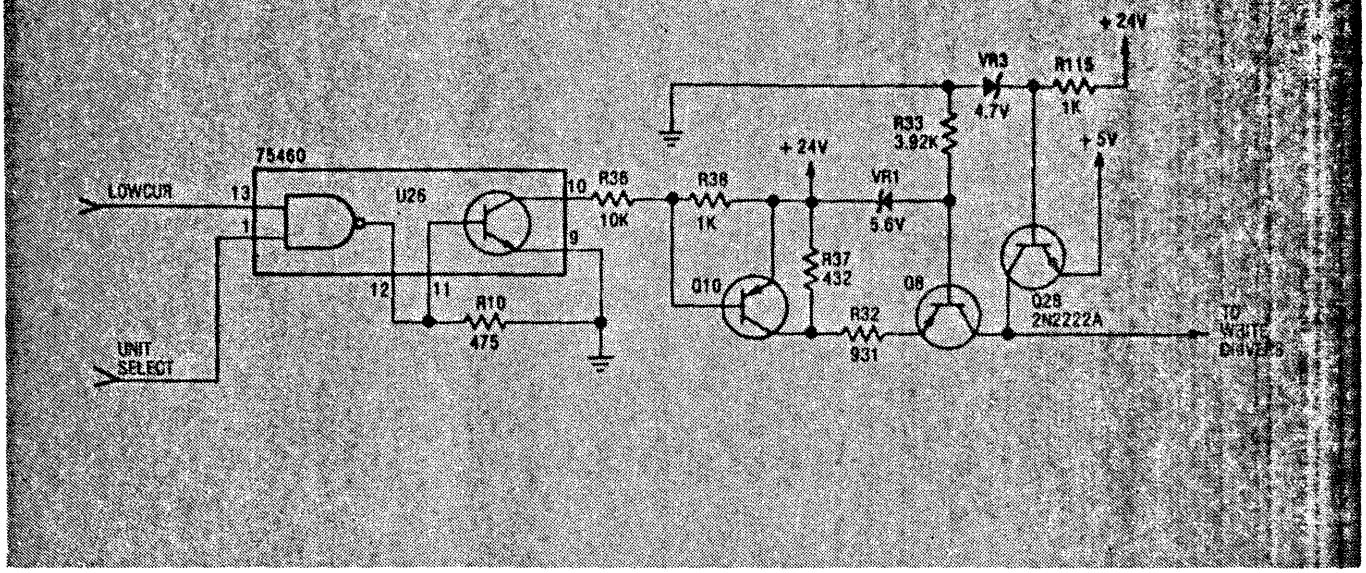
WRITE LOGIC — WRITE CURRENT SOURCE



DURING THE DESCRIPTION OF THE SIGNAL INTERFACE TO THE HOST SYSTEM CONTROLLER, WE MENTIONED THE NEED TO REDUCE THE WRITE CURRENT WHEN WRITING ABOVE TRACK 43. THIS IS NECESSARY BECAUSE OF THE EFFECTS OF INCREASED PACKING DENSITIES TOWARD THE CENTER OF THE DISKETTE. THE WRITE CURRENT SOURCE LOGIC, HIGHLIGHTED IN THIS DRAWING, PROVIDES THE TWO LEVELS OF CURRENT REQUIRED.

44

WRITE CURRENT SOURCE

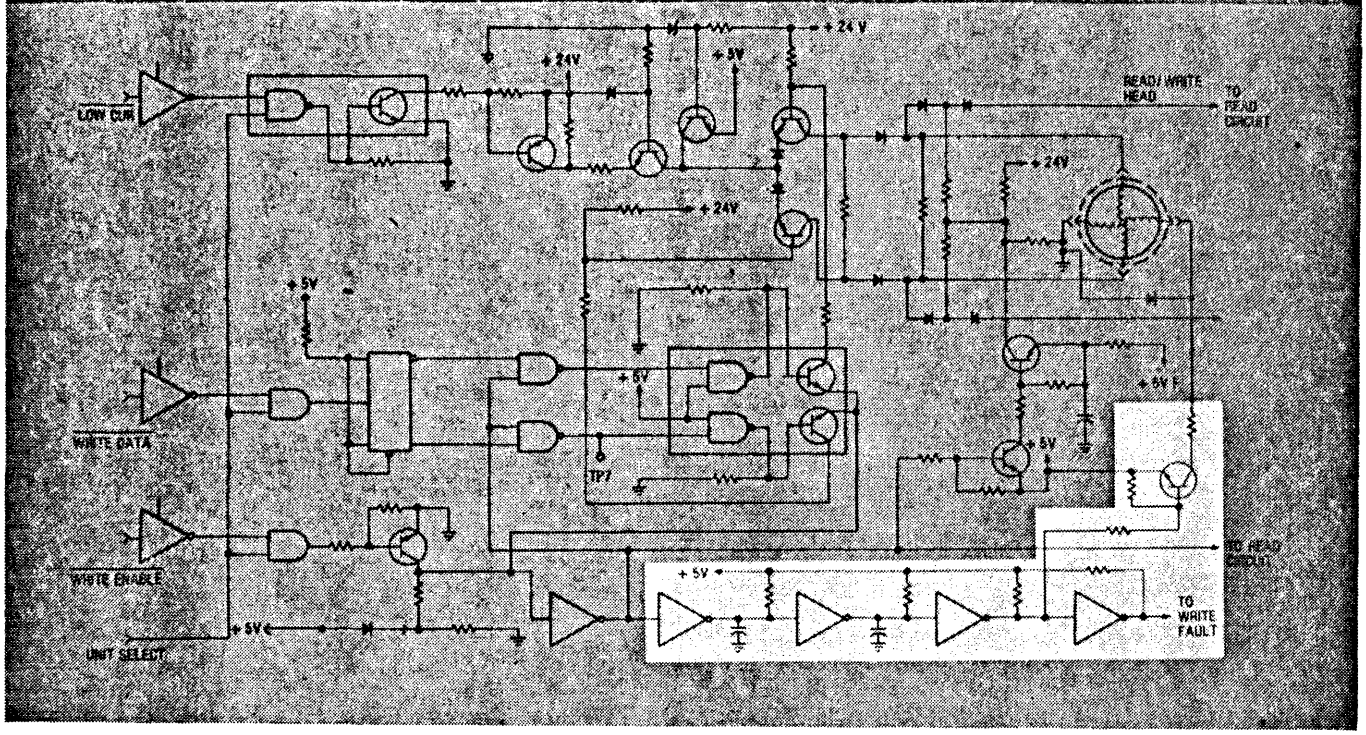


THE CONTROL SIGNAL "LOW CURRENT" IS GATED WITH UNIT SELECT IN THE IC DRIVER, U26. THE OUTPUT OF U26 SWITCHES TRANSISTOR Q10 ON FOR NORMAL CURRENT AND OFF FOR LOW CURRENT. WHEN TRANSISTOR Q10 IS ON, THE CURRENT PATH TO THE WRITE HEAD IS FROM THE +24 VOLT SUPPLY, SHOWN BETWEEN R38 AND VR1, USING Q10 TO BYPASS RESISTOR R37, THEN THROUGH RESISTOR R32 AND TRANSISTOR Q8 TO THE WRITE DRIVERS.

WHEN TRANSISTOR Q10 IS OFF FOR LOW CURRENT, RESISTOR R37 IS IN SERIES BETWEEN THE +24 VOLT SUPPLY AND R32, REDUCING THE CURRENT FLOW TO THE WRITE DRIVERS.

45

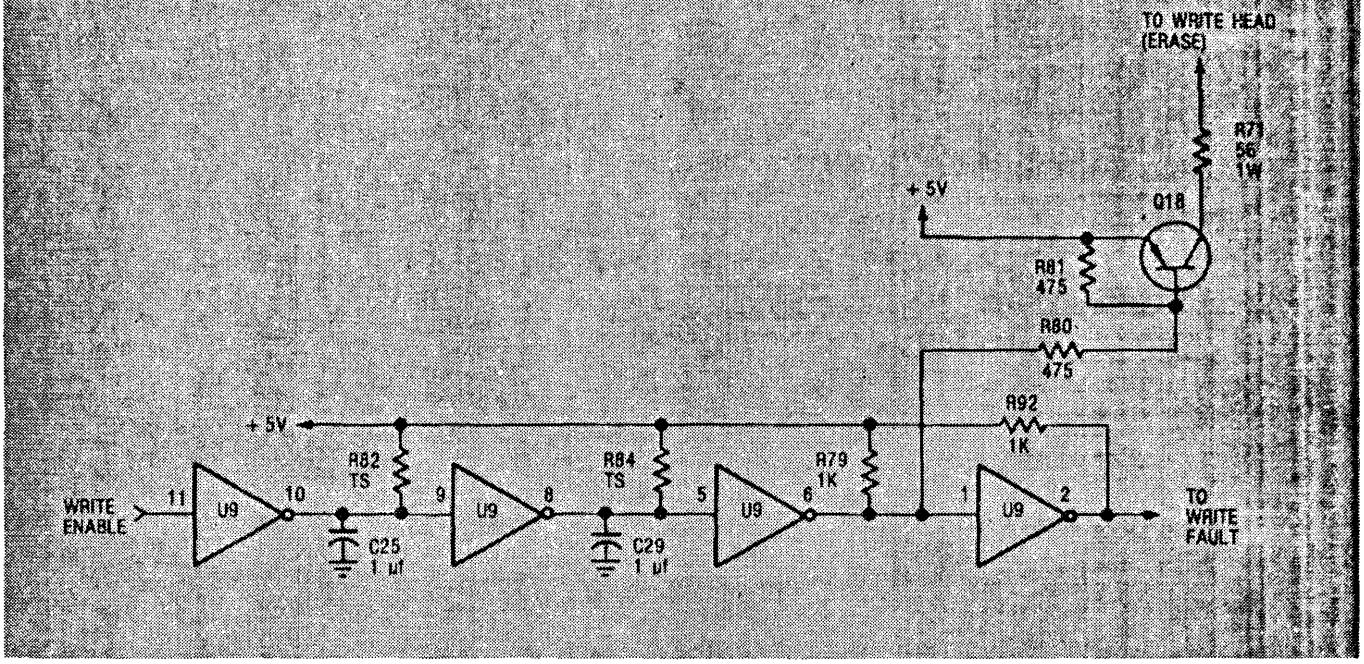
WRITE LOGIC — DELAY CIRCUIT AND ERASE DRIVER



THIS DRAWING HIGHLIGHTS THE DELAY CIRCUIT WHICH IS USED TO DELAY THE SIGNAL "WRITE ENABLE" AND THE ERASE DRIVER WHICH PROVIDES CURRENT FOR THE TUNNEL ERASE COIL IN THE WRITE HEAD DURING A WRITE OPERATION.

46

DELAY CIRCUIT AND ERASE DRIVER



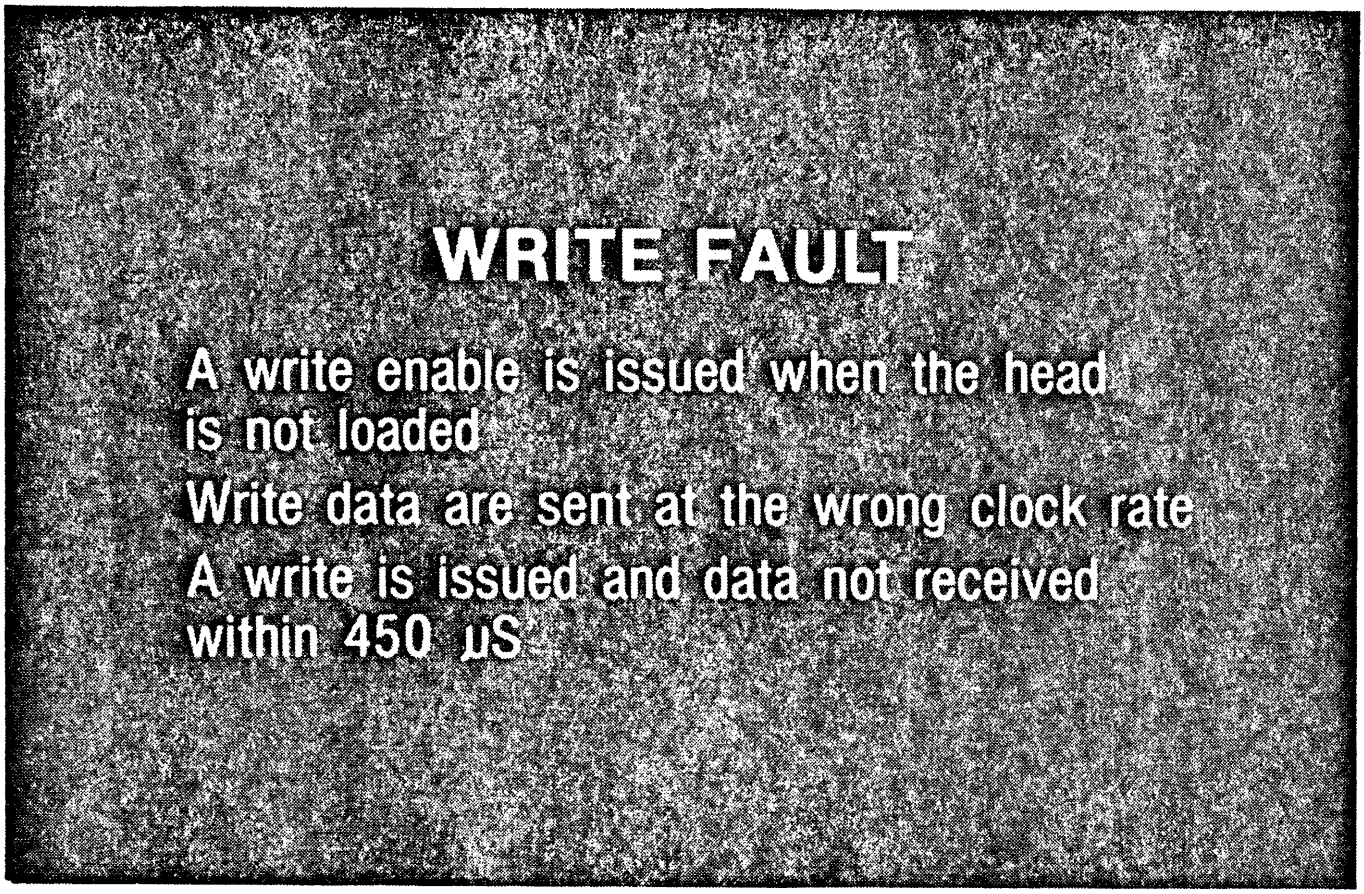
THE DELAY CIRCUIT CONSISTS OF TWO INVERTERS, IN SERIAL, PACKAGED IN U9, WITH 1 MICRO FARAD CAPACITORS C25 AND C29 ON THEIR RESPECTIVE OUTPUTS. TEST SELECTED RESISTOR R82 DETERMINES THE DELAY OF THE TRAILING EDGE OF THE WRITE ENABLE SIGNAL. TEST SELECTED RESISTOR R84 DETERMINES THE DELAY OF THE RISING EDGE OF THE WRITE ENABLE SIGNAL.

THE VALUES OF THE TWO TEST SELECTED RESISTORS ARE SELECTED TO DELAY THE WRITE ENABLE SIGNAL BY 450 MICRO SECONDS.

THE DELAYED WRITE ENABLE SIGNAL IS INVERTED AND TURNS ON THE ERASE DRIVER TRANSISTOR Q18 TO PROVIDE CURRENT TO THE TUNNEL ERASE COIL IN THE WRITE HEAD FROM THE 5V SUPPLY.

THE DELAYED WRITE ENABLE SIGNAL IS ALSO USED BY THE WRITE FAULT LOGIC WHICH IS EXPLAINED LATER.

47



A WRITE FAULT IS DEFINED WHEN ONE OR MORE OF THESE CONDITIONS EXIST; A WRITE ENABLE IS ISSUED WHEN THE HEAD IS NOT LOADED; WRITE DATA ARE SENT AT THE WRONG CLOCK RATE; AND/OR A WRITE IS ISSUED AND DATA ARE NOT RECEIVED WITHIN A 450 MICROSECOND TIME PERIOD.