60476010

CONTROL DATA CORPORATION

CDC® MAGNETIC TAPE TRANSPORT CONTROLLER

FA464, FA465

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE REFERENCE/MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released class A. This manual includes data previously contained in publications 89600271 and 89600866
(10/80)	which are obsolete.
B	Manual revised; includes ECO DS022022, providing a revised cable assembly drawing.
(1/81)	
C	Manual revised; includes ECO DS022126, providing clarification of the A-register bits and addition of an FCC non-tested
(9/81)	warning label.
D	Manual revised; includes ECO DS022175, providing miscellaneous corrections.
(8/82)	
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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FA464-A	04		
FA465-A	02		
FA465-B	02		

LIST OF EFFECTIVE PAGES

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PREFACE

This manual describes the Control Data® FA464 and FA465 Magnetic Tape Transport Controller (MTTC) used in CYBER 18 Processor Systems. The MTTC interfaces the CYBER 18 computer to the phase encode (PE) or nonreturn to zero-inverted (NRZI) magnetic tape transport (BW101, BW303, BW305, and FA107) via a DZ101 Magnetic Tape Formatter.

The magnetic tape formatter can interface with any combination of one to four magnetic tape transports in a daisy-chain configuration.

The descriptions, diagrams, and drawings contained in this manual relate specifically to the FA465-A MTTC. However, they are equally applicable to all FA464 and FA465 MTTCs unless specifically stated otherwise.

The publications listed below provide more detailed information relative to equipments, subsystems, and systems.

Description	Publication No.
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
CYBER 18 Computer Systems Central Processor Field Repair Guide	60475001
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
CYBER 18 Computer System Overview Manual	60475000
CYBER 18 Processor with MOS Memory (Macro Level) Reference Manual	96768300
Magnetic Tape Transport (NRZI) Subsystem Field Repair Guide	60475041
Magnetic Tape Transport Subsystem, Dual Mode (NRZI/PE) Field Repair Guide	60475042

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GENERAL DESCRIPTION 1

The magnetic tape transport controller (MTTC) contains the logic that: interprets the CYBER 18 central processing unit (CPU) function codes, assembles and disassembles the 16-bit words passed between the CPU and the DZ101-A magnetic tape formatter and provides the magnetic tape transport (MTT) status information to the CPU. The MTTC and the CPU communicate via the A/Q channel for status, control information, and test, and via the DMA channel for data transfer.

PHYSICAL DESCRIPTION

The MTTC, illustrated in figure 1-1, uses the concept of microprogramming. It contains TTL (transistor-to-transistor) logic components mounted on one CYBER 18, 11- by 14-inch (279- by 355-millimeter) printed wiring assembly (PWA) that occupies one A/Q-DMA slot in the CYBER 18 processor chassis.

FUNCTIONAL DESCRIPTION

The MTTC, via the magnetic tape formatter, can control up to four tape transports when the tape transports are connected in a daisy-chain arrangement (refer to figure 1-2). A cable assembly connects the MTTC with the formatter.

The MTTC, via the formatter, can handle any type of tape transport in any sequence of densities. It can control combinations of up to four MTTs having speeds of 25 or 50 inches per second (ips), 7- or 9-track, single or dual mode, with densities of 556 or 800 bits per inch (bpi) for 7-track transports, 800 bpi (NRZI) or 1600 bpi (PE) for 9-track transports.

The MTTC has the following capabilities:

- Provides interface control for one to four MTTs via the magnetic tape formatter
- Decodes the CPU function codes, selects the MTT, and controls the tape-motion direction
- Assembles, disassembles, and transfers data between the CPU and the magnetic tape formatter
- Detects operation and transmission errors
- Provides the processor with MTT status information
- Four on-line self-tests are available for checking:
  1. Internal data paths and arithmetic logic unit (ALU)
  2. Internal flip-flop and jump conditions
  3. Data read via the DMA channel and data transmitted via the A/Q channel
  4. The A/Q channel data path
- Off-line maintenance and test operation

REFERENCE DATA

Transfer Rate:

50 ips	Maximum transfer rate to the computer is 40 kilowords per second.
25 ips	Maximum transfer rate to the computer is 20 kilowords per second.

Density:

Low	556 bpi (7 track transport) 800 bpi (9 track transport)
High	800 bpi (7 track transport) 1600 bpi (9 track transport)

Power:	+5 V at 9 amps
Temperature:	40°F to 120°F (4°C to 49°C)
Humidity:	10 to 90 percent relative humidity with no condensation.
Warm-Up Time:	None

NONOPERATING ENVIRONMENT

Temperature:	-30°F to 150°F (-22°C to 65°C)
Humidity:	5 to 95 percent relative humidity with no condensation.

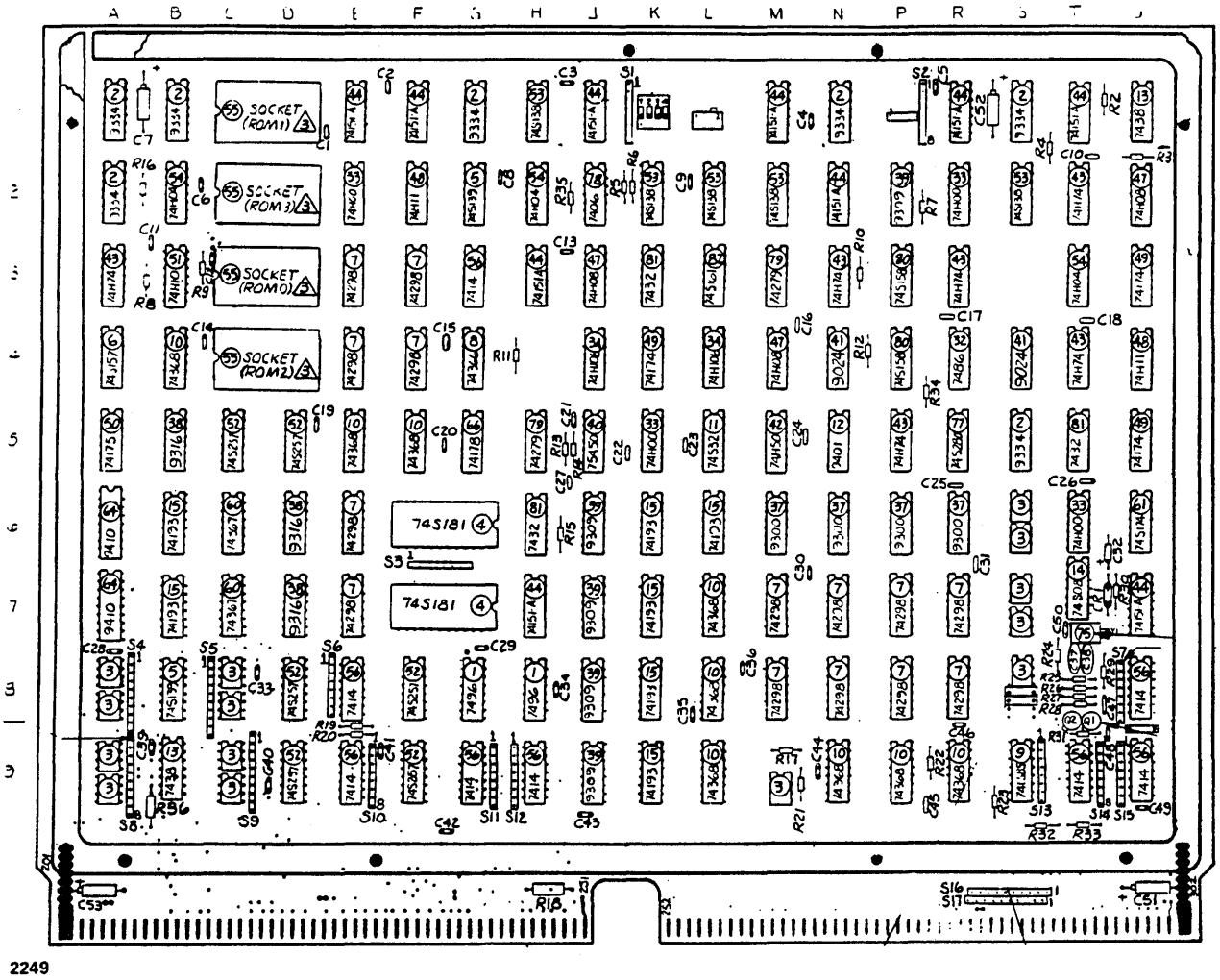


Figure 1-1. Magnetic Tape Transport Controller (MTTC)

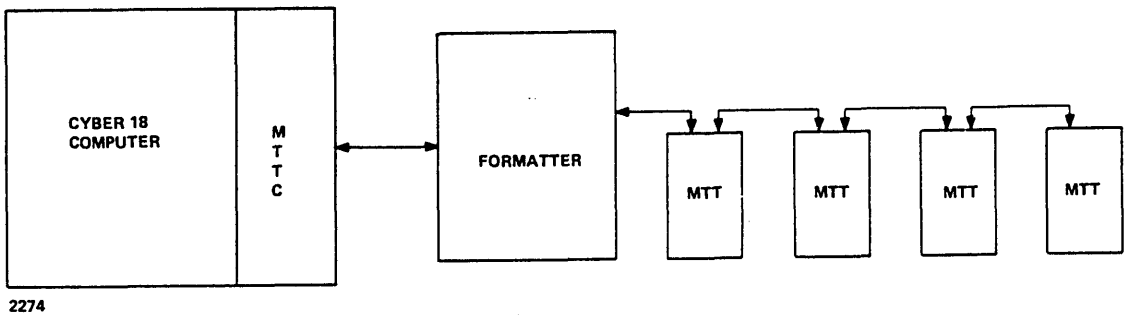


Figure 1-2. Typical System Configuration

OPERATION 2

This section describes the operating and maintenance jumpers and switches of the MTTC. The section also describes the programming instruction formats required to function the controller.

The magnetic tape transport controller (MTTC) switch and jumper positions are illustrated in figure 2-1. Table 2-1 indicates the jumper positions that designate subsystem address and enable/disable operational functions. For information on the maintenance switches that provide for selection of maintenance operations and test conditions, refer to table 2-2.

CONTROLLER JUMPER SELECTION

UNIT PROTECT (UP0 - UP3)

There are four unit protect jumpers, one per tape transport. To protect a transport, the jumper must be inserted. When a protected tape transport is selected, only status requests and protected instructions can access the MTTC.

The MTTC, after being connected to a protected tape transport, remains in the protected state until a deselect instruction is received or an unprotected transport is selected. Jumpers UP0, UP1, UP2, and UP3 select unit protect function for transports MTT0, MTT1, MTT2, and MTT3, respectively.

AUTOLOAD ENABLE (ALD)

This jumper when inserted allows the MTTC to be the autoload controller. When this jumper is removed, the MTTC is disabled from performing autoload operations. This operation is not supported in CYBER 18 systems; this jumper must be removed.

SINGLE/DUAL BUS (SB)

This jumper when inserted indicates dual CPU access to the magnetic tape formatter bus. For CYBER 18 operation, this jumper must be removed.

BUS PRIORITY (BP)

This jumper determines which controller gains control of the bus when there are simultaneous bus requests from both processors. Control goes to the controller that has the jumper removed. When operating in a dual CPU system, only one MTTC must have the jumper inserted. This operation is not supported by CYBER 18 systems; the jumper must be removed.

EQUIPMENT CODE (Q07 - Q10)

These four jumpers are used to represent any hexadecimal number from 0 to F. They are used to assign an

TABLE 2-1. JUMPER SELECTION

Jumper Name	Function	Position	
		Inserted	Removed
Q07 - Q10	Determine equipment code	Logic 1	Logic 0
ALD†	Autoload enable	--	--
SB†	Single/dual bus access	--	--
UP0 - UP3	Unit protect	Unit protected	Unit unprotected
SD0 - SD3	Not applicable to MTTC	--	--
BP†	Bus priority		
JM†	Mode jumper	--	--

†Must always be removed for MTTC operations.

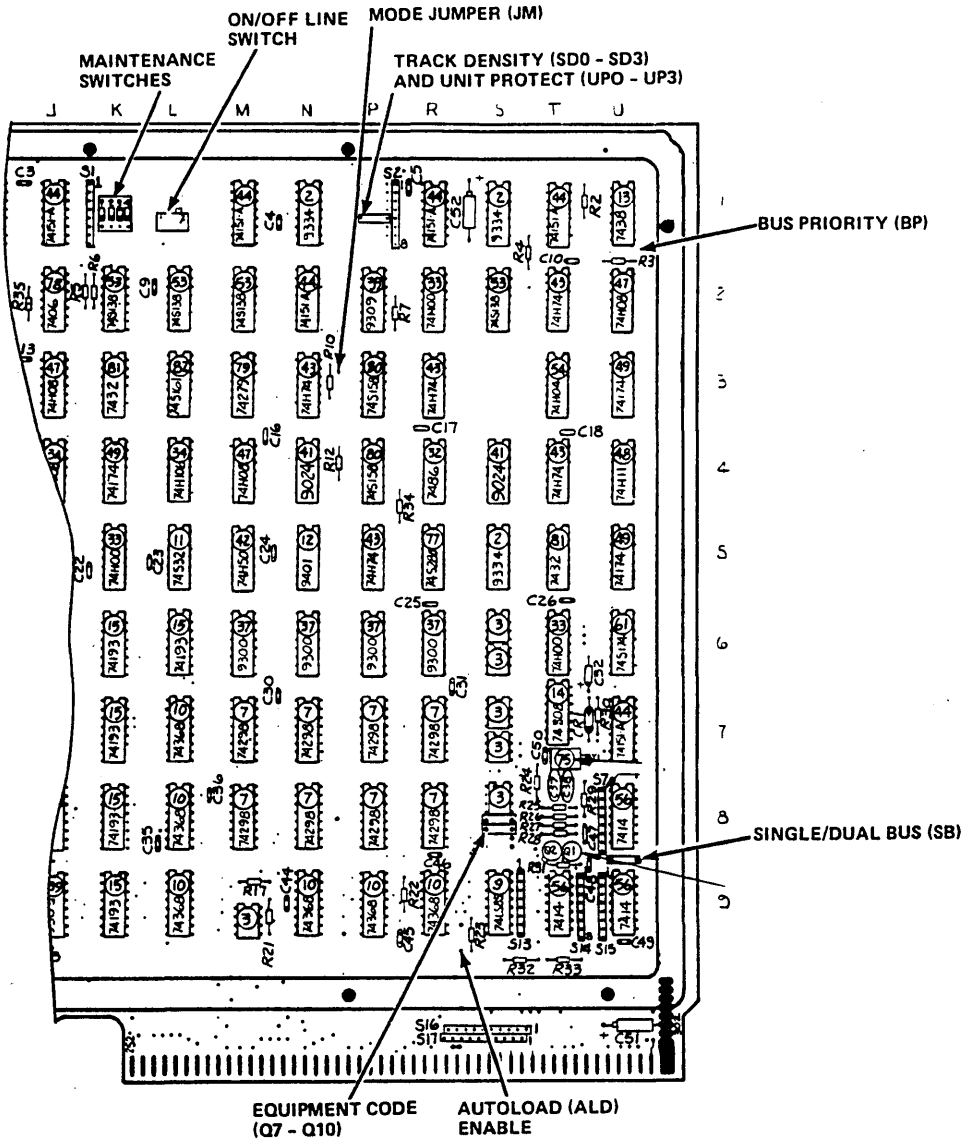


Figure 2-1. Switch and Jumper Locations

TABLE 2-2. OFF-LINE OPERATIONS

MS2	MS1	Off Line Operation Performed (LS Switch Off)
On	On	Continuous write - 0's
On	Off	Continuous write - 1's
Off	N/A	Continuous read
NOTE:	Place LS switch on while changing MS1 or MS2 switch conditions.	

equipment number to the MTTC. Any instruction sent by the computer must be accompanied by an equipment number (bits Q07 through Q10) that matches the setting of the plugs. The W field must be zero.

CONTROLLER SWITCH SELECTIONS

ON/OFF LINE SWITCH

When in the on-line position, this switch enables normal controller operation. When the switch is in the off-line position, the controller is disconnected from the controller CPU bus and is placed in maintenance mode. The type of off-line operation that is performed is a function of the maintenance switch positions.

MAINTENANCE SWITCHES

Table 2-2 shows the available off-line operations selected by maintenance switches MS1 and MS2. Switches MS1, MS2, and MS3 should be changed only when the on/off-line (LS) switch is in the on-line position.

Switch MS3 determines the density at which the off-line operation is performed. MS3 on indicates low density operation; MS3 off indicates high density operation.

The off-line operation is performed on the first unit that is ready, starting at unit 0. If no unit is ready, the controller aborts the off-line operation and remains busy until the controller is placed in the on-line mode. The unit on which the maintenance is to be performed should be made ready prior to placing the on/off-line switch in the off-line position. If the unit becomes not-ready during the maintenance operation, the operation is aborted. To restart the operation when the unit does become ready, the on/off-line switch must be set to the on-line position and then set again to the off-line position. Placing the on/off-line switch in the on-line position terminates the maintenance operation. The controller remains on bus, but a new unit select command must be issued.

Continuous Write Zeros

The controller writes a continuous record of 0000_{16} on the tape until an end-of-tape (EOT) marker is reached, the unit becomes not-ready, or the controller is placed in the on-line mode. If the unit is write-protected, no writing is done. When an EOT marker is detected, the controller terminates tape motion and exits from the maintenance routine. All data transfer errors are gated off.

Continuous Write Ones

This operation is the same as continuous write zeros except that the data written on the tape is $FFFF_{16}$.

Continuous Read

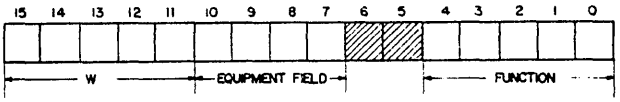
The controller continuously reads data from the tape. When the end of a record is reached, the controller will read the next record. Tape motion continues until the unit becomes not-ready, an EOT marker is detected, or the controller is placed in the on-line mode. When an EOT marker is detected, the controller terminates tape motion and exits from the maintenance routine. Data transfer errors and file marks are disregarded in this mode.

PROGRAMMING

The MTTC communicates with the central processing unit via the A/Q and direct memory access channels.

Q REGISTER

The Q register designates the equipment to be referenced and specifies the operation to be performed when an input or output instruction is executed. The Q-register format is shown below:



The W field (bits Q15 through Q11) must always be zero.

The equipment field (bits Q10 through Q07) selects the MTTC. These bits must match the equipment code setting of the MTTC. The equipment code is determined by jumper conditions on the MTTC assembly.

Bits Q05 and Q06 are ignored by the MTTC.

Bits Q00 through Q04 specify the function to be performed by the controller in response to an input or output instruction.

Refer to table 2-3 for the available functions and their corresponding codes. Any code not appearing in table 2-3 is illegal.

When the CPU executes output instructions with the Q register according to table 2-3, the controller loads the A register with the requested controller status.

Codes listed in table 2-3 as illegal are rejected by the MTTC. Status reading and all operation initiation takes place via the A/Q channel. Data is transferred via the DMA channel.

TABLE 2-3. Q-REGISTER FUNCTION CODE

Q04	Q03	Q02	Q01	Q00	Output	Input
1	0	0	0	0	Clear controller	Dynamic status
0	0	0	0	1	Director function	A-out status
0	0	0	1	0	First word address	Current word status
0	0	0	1	1	Bank select	Current bank status
0	0	1	0	0	Load file address	File status
0	0	1	0	1	Sense/assemble next ready	Transport status
0	0	1	1	0	Unit select	Illegal
0	0	1	1	1	Block length	Illegal
0	1	0	0	0	Bus connect	Illegal
0	1	0	0	1	Internal request	Illegal
0	1	0	1	1	Illegal	Illegal
0	1	1	0	0	Self-test 1	Illegal
0	1	1	0	1	Self-test 2	Illegal
0	1	1	1	0	Self-test 3	Illegal
0	1	1	1	1	Self-test 4	Illegal

A REGISTER

OUTPUT FROM A OPERATION

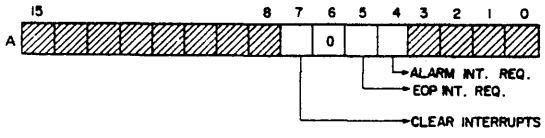
All operations initiated by an output instruction, with the exception of clear controller, are rejected if a protect fault is detected or if the MTTC is busy. Clear controller is rejected only if a protect fault occurs. Excessive noise on the A/Q channel may cause valid operations to be rejected.

Interrupt Request

The MTTC generates an interrupt for the following conditions:

- End of operation (EOP)
- Alarm

The interrupt request command allows the CPU to select the conditions under which the interrupt response (signal) becomes active. This command is also used for clearing the interrupt response. The A-register format is shown below:



The interrupt request command is rejected when the controller is busy or if a protect fault occurs. The controller does not become busy upon acceptance of this command.

The conditions for interrupt selected in the interrupt request command remain valid for all subsequent instructions. Master clear, clear controller, and clear interrupts deselect all interrupts and deactivate the interrupt response.

Clear Interrupts

When bit A07 is set, all EOP and alarm interrupt requests and status responses are cleared. Interrupt requests may be cleared and deselected in the same interrupt request command. The order of execution is to first clear all interrupt requests and then select them according to bits A05 and A04. If A07 is not set there is no change in interrupt select.

Master clear and clear controller clear all interrupt requests and responses. Bits A00 through A03 and A08 through A15 are ignored by the controller.

EOP Interrupt Request

When bit A05 is set an EOP interrupt is enabled. An interrupt is generated upon completion of an operation that caused the controller to go busy. An interrupt becomes active approximately 2 microseconds before end of operation (EOP) status is set. An EOP interrupt is generated, if one has been requested, upon completion of any of the following operations.

- Director function
- Bus connect
- Unit select
- Test modes 1, 2, 3, and 4
- Assemble/sense next ready

Once enabled in the interrupt request command, interrupts remain enabled for all subsequent instructions until disabled by clear interrupt, clear controller, or master clear.

If A05 is clear there is no change in EOP interrupt enable.

Alarm Interrupt Request

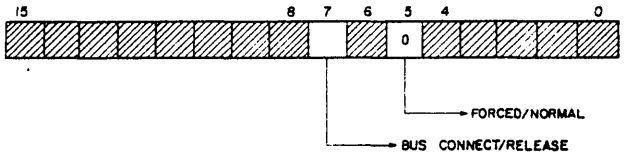
When bit A04 is set, an alarm interrupt is generated whenever an alarm condition is detected. The interrupt is sent 2 microseconds before the EOP status bit is set regardless of when the alarm status bit is set. If the alarm bit is active when an interrupt request command with A04 equal to 1 is received, an interrupt is generated immediately.

If A04 is clear there is no change in alarm interrupt enable.

Once enabled by the interrupt request command, alarm interrupt remains enabled until it is disabled by interrupt clear, clear controller, or master clear.

Bus Connect

The magnetic tape formatter can be shared by two MTTCs on a common bus. When it is necessary for the MTTC to reference the formatter, exclusive control of the formatter/controller bus must first be established. The bus connect command is used for this purpose. The A-register format for bus connect is shown below:



The bus connect command is rejected if the controller is busy or a protect fault occurs. Acceptance of the command causes the MTTC to become busy until bus control is established.

When the MTTC is off-bus (bus control has not been established) and not busy, the following commands are rejected:

- Director function
- Unit select
- Transport status
- Assemble/sense next ready

Bus Connect/Release

When bit A07 is set the MTTC establishes bus control. The MTTC is busy until bus control is established. The mode of the connect is determined by A05.

When A07 is clear, the MTTC releases the bus. The controller does not go busy for bus release. Clear controller does not affect on-bus status. Master clear causes a bus release.

Bus Connect Requests

When the bus connect request is active, bit A05 is clear. The MTTC first checks bus and usage and goes busy. When the bus becomes available, the MTTC gains control and notifies the CPU by setting on-bus status and by generating EOP status and EOP interrupt (if EOP interrupt was selected).

A force release signal from the alternate has the same effect on the MTTC as a master clear, except that EOP and alarm interrupt requests are not affected by this signal. They are cleared by master clear.

Unit Select

The unit select command is used to select one of the four tape transports. This command also selects operating conditions for the selected transport. Figure 2-2 shows the A-register format for unit select. Bits 4 and 5 select the operational unit.

Unit select commands are rejected if the controller is off-bus, a protect fault is detected, or the controller is busy.

Select/Deselect

When bit A07 is set, the transport specified by the code contained by bits A04 and A05 is selected.

When A07 is cleared, any transport that was previously selected is deselected. A04 and A05 have no meaning for deselect. The controller does not go busy for a unit deselect.

A master clear deselects all units.

If a change in operating conditions of the selected transport is desired, a new unit select command must be issued.

BCD/Binary Select

When bit A13 is set, binary coded decimal (BCD) format (7-track transport only) is selected. Data is written onto the tape with even parity and data read from the tape is checked for even parity. In BCD format, the all-zero character is illegal. If an attempt is made to write or read an all-zero character, a parity error is generated.

When A13 is not set, binary format (7- or 9-track) is selected. Data is written on the tape with odd parity. Data read from the tape is checked for odd parity.

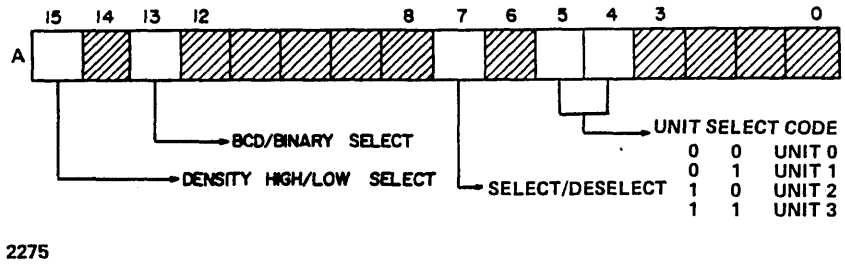


Figure 2-2. A-Register Format for Unit Select

For 9-track transports, A13 is ignored. Data is always read/written in the binary format.

A master clear selects binary format. Clear controller does not affect the format selection.

Density High/Low Select (A15)

Bit A15 selects the higher or lower of the two available densities (refer to table 2-4).

TABLE 2-4. DENSITY HIGH/LOW SELECT

A15	Density (Bpi)	9-Track Dual Mode	7-Track (NRZI)
1	Low	800 (NRZI)	556
0	High	1600 (PE)	800

Density selection can be changed only when the transport is at beginning of tape (BOT). If the density select is changed when the transport is in the middle of a tape reel, operations continue at the previous density selection until the transport reaches BOT, at which time a switch is made to the new density selection. A master clear selects high density. Clear controller does not affect the density selection.

When reading on a dual-mode transport, data is read in the NRZI mode if no identification (ID) burst is detected, or in PE mode if an ID burst is detected regardless of the state of A15.

A PE tape without an ID burst cannot be read in PE mode on a dual-mode transport.

Bank Select

The bank select command specifies one of four 65K banks in which the address of the first word of a buffer is to be found. The code of the bank is contained in A07 and A06. Figure 2-3 shows the A-register format. Bank select and the first word address together provide an 18-bit address, allowing the first word of the transferred data buffer to be located within 265K of memory. The bank select command is rejected if the controller is busy or a protect fault has occurred.

Block Length

The block-length instruction specifies the length of the buffer to be transferred starting at the first-word address. Bits 0 through 15 of the A register are used to specify a maximum block length of 65K.

Bank boundaries may be crossed during data transfers.

This command is rejected if the controller is busy or a protect fault occurs.

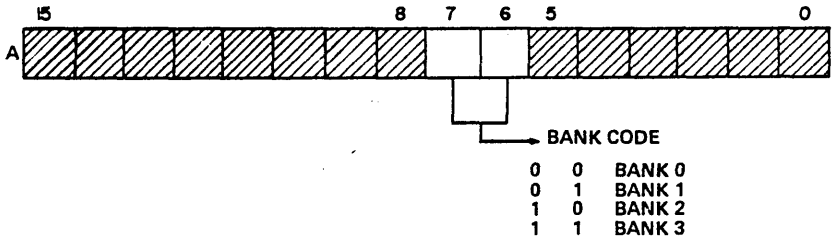
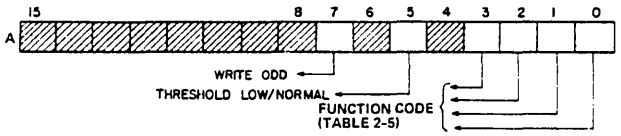


Figure 2-3. A-Register Format for Bank Select

Director Function

The director function command specifies the operation and motion that the selected transport is to perform. The director function A-register format is shown below. Table 2-5 details the director function codes.



Director function commands are rejected if the controller is busy, off-bus, or a protect fault is detected. A master clear or clear controller causes all transport motion to cease.

Functions listed in table 2-5 as illegal should not be used by the programmer. If an illegal code is received, the MTTC goes busy. Upon determining that the received code is illegal, EOP status is set followed by not busy status 1 microsecond after EOP. If an EOP interrupt was requested, an interrupt is sent to the CPU. Illegal director function codes act as NOPs.

Bit A05 specifies the read threshold. If A05 is set, it specifies a lower threshold within the read amplifier for recovering errors when normal read fails. If it is not set, it specifies a normal read.

Bit A07 is relevant only for write operations and specifies whether an odd (1) or an even (0) number of tape words is to be written.

With A07 set, only the upper portion of the last computer word is written onto the tape. (The lower portion is not written). This results in a record consisting of an odd number of tape words.

In this manner the record length to be written can be specified in tape words rather than in computer words.

Completion of the motion function, master clear, or clear controller selects normal read and write even.

The controller accepts a new motion function only after busy status is cleared and EOP status is set.

Table 2-6 provides the transport stop times following read and write operations for 50 ips and 25 ips tape speeds. New motion functions in the same direction as a previous motion received within the stop time interval is performed without stopping.

Read Data

Two 8-bit bytes are read from the tape and assembled into one 16-bit computer word. Data is written into the memory starting at the first word address and continues until the number of words specified in block length has

TABLE 2-5. DIRECTOR FUNCTION CODES

A03	A02	A01	A00	Function
0	0	0	0	Read data
0	0	0	1	Space forward
0	0	1	0	Search file mark (forward)
0	0	1	1	Search file mark (backward)
0	1	0	0	Back space
0	1	0	1	Write data
0	1	1	0	Write file mark
0	1	1	1	Rewind
1	0	0	0	Fixed erase
1	0	0	1	Variable erase
1	0	1	0	Controlled backspace
1	0	1	1	Rewind off-line
1	1	0	0	Illegal
1	1	1	0	Illegal

TABLE 2-6. TRANSPORT STOP TIME

MTT Speed	Command	
	Write	Read
25 ips	15 ms	19 ms
50 ips	7.5 ms	12.5 ms

been transferred or the end of record is reached. Upon acceptance of this command, the controller becomes busy and remains busy until the next interrecord gap is detected, after which EOP is set. Busy status is reset 1 microsecond after EOP.

If the first record following BOT is a file mark and not data, the controller does not continue to the next record.

Space Forward

The tape is moved forward until the next interrecord gap; if a file mark is detected, file mark status is set. Upon acceptance of this command, the controller becomes busy until the next interrecord gap or file mark is detected, after which EOP status is set and busy status is reset.

Search File Mark (Forward)

The tape is moved forward until the next file mark is detected. File mark status is set. The operation for EOP and busy is the same as for space forward.

Search File Mark (Backward)

The tape is moved backward to the previous file mark and file mark status is set. If no file mark is detected, motion stops at load point. The operation for EOP and busy is the same as for space forward.

Backspace

The tape is moved backward until the next interrecord gap; if a file mark is detected, file mark status is set. Upon acceptance of this command, the controller becomes busy until the next interrecord gap or file mark is detected, after which EOP status is set and busy status is reset.

Write Data

Starting at the first word address, 16-bit data words are read from the memory, disassembled into two 8-bit tape bytes, and written onto the tape. This process continues until the number of computer words specified in the block length have been written on the tape. If a write odd operation was specified (A07 = 1), writing stops after the upper byte of the last computer word. The lower byte is not written, resulting in an odd number of tape words in the record. This feature allows record-length specification to be done in tape words rather than in computer words. With A07 = 0, both the upper and lower portions of the last computer word are written on the tape. After completion of the write, an interrecord gap is created on the tape and tape motion stops. EOP and busy status operation are the same as for read data.

Write File Mark

The tape is erased forward approximately 6 inches (152 millimeters) and a file mark is written on the tape. Upon acceptance of this command, the controller becomes busy. After writing the file mark, EOP status is set and busy status is reset.

Rewind

The tape is rewound at high speed to load point. The controller is busy only long enough to validate the command and to initiate tape motion, after which EOP status is set and busy status is reset.

Fixed Erase

A 6-inch (152-millimeter) length of tape is erased, after which tape motion stops. EOP and busy status operations are the same as for write file mark.

Variable Erase

Variable erase allows a variable length of tape to be erased. The length is controlled by the block length and is equal to approximately twice the block length tape words. After erasing the specified number of words, tape motion ceases. EOP and busy status operation are the same as for write file mark.

Controlled Backspace

This feature allows the formatter to position the tape back to the previous interrecord gap for a record that has just been written in error. The amount of tape words backspaced is equal to twice the length specified in block length. When the last tape word is backspaced, the formatter goes through its normal termination sequence. The result is the positioning of the write head 0.13 inch (3.3 millimeters) ahead of its original position prior to the erroneous record. This function provides a means of reversing over dropouts without possible positioning errors.

The operation for EOP and busy status is the same as for space forward:

Rewind (Off-Line)

High-speed rewind motion to load point is initiated in the selected transport, after which the selected transport goes off-line. The controller is busy only long enough to initiate the rewind motion, after which the EOP status is set and busy status is reset. Once the rewind motion is initiated, the controller is able to accept motion functions to another transport. This command allows the rewind of one transport and motion functions in another transport to be carried out in parallel.

Clear Controller

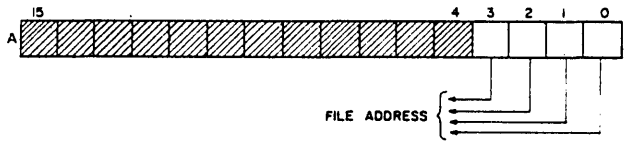
The clear controller command clears controller statuses, registers, interrupt requests, and responses. The A register contents do not affect this command.

This command is rejected only if a protect fault occurs.

Clear controller causes all motion (except rewind motion) in the selected transport to cease, but the unit select and on-bus status are not affected.

Load File Address

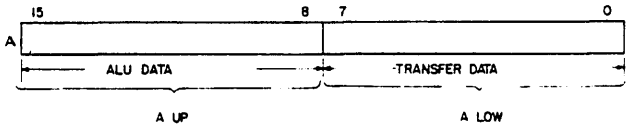
The load file address command specifies the address of the MTTC 16 register file, which will be read by a file registers status request. The load file address A-register format is shown below:



The load file address command is rejected if the controller is busy or a protect fault is detected.

Self-Test 1

Self-test 1 causes the MTTC to check its internal data paths and arithmetic logic unit ALU. The lower eight bits of the A register specify the data that is to be transferred (transfer data) along the internal data paths of the MTTC. The upper and lower eight bits of the A register specify the data that is to be operated on by the ALU. The self-test 1 A-register format is shown below:

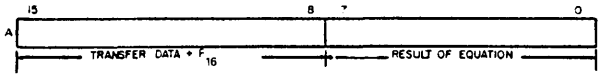


Upon acceptance of this command, the MTTC becomes busy and remains busy until the internal transfers and ALU operations are complete. After completion, the EOP status is set and busy status is reset 1 microsecond later. If EOP status is not set within 3 microseconds, this is an indication that the MTTC is defective.

After the busy status is reset, the A-out status should be read to determine the success of the test. The upper eight bits of the A register should contain the same data as that was originally sent in the lower eight bits of the A register in self-test 1, plus F_{16}. The lower eight bits should contain an expected result, which is a function of the data originally sent in the upper and lower eight bits of the A register during self-test 1 according to the following equation:

A Low = ((((A up - 1) x 2 + A low) + 1 - A up)·A low)
or A up carry-out is disregarded.

The self-test 1 result is shown below:



Self-test 1 also loads the 16 file registers in the following manner:

FILE (0) = Transfer data + F_{16}

FILE (1) = Transfer data

FILE (2) = Transfer data + 1

FILE (3) = Transfer data +2

FILE (4) = Transfer data + 3

FILE (5) = Transfer data + 4

FILE (6) = Transfer data + 5

FILE (7) = Transfer data + 6

FILE (8) = Transfer data + 7

FILE (9) = Transfer data + 8

FILE (A) = Transfer data + 9

FILE (B) = Transfer data + A_{16}

FILE (C) = Transfer data + B_{16}

FILE (D) = Transfer data + C_{16}

FILE (E) = Transfer data + D_{16}

FILE (F) = Transfer data + E_{16}

In general, FILE (N) contains the transfer data plus (n-1), except FILE (0), which contains transfer data plus F_{16}.

After reading A-out status, the contents of the 16 file registers should also be read and examined for the proper data.

Self-test 1 must be preceded by a clear controller command.

Self-Test 2

Self-test 2 checks the MTTC internal flip-flops, jump conditions, and dynamic status flip-flops. The A register

is not used for the self-test 2 command. Upon acceptance of this command, the controller becomes busy until the test is completed, after which EOP status is set. Busy is cleared 1 microsecond later. If EOP is not set 3 microseconds after the controller becomes busy, this is an indication that the controller is defective.

Prior to the execution of self-test 2, a clear controller command should be issued to ensure that all dynamic status flip-flops are in their quiescent state. Figure 2-4 illustrates the dynamic status after execution of clear controller and self-test 2.

When the test is complete (busy status reset), A-out status should be read immediately after the completion of the test to determine if the test is successful. A-out status $ACED_{16}$ indicates that the test is successful. A-out status $DEAD_{16}$ or any other status indicates that the controller is defective.

If A-out status gives the successful result ($ACED_{16}$), dynamic status should be read and compared to bit box B in figure 2-4. If these are not identical, the controller is defective.

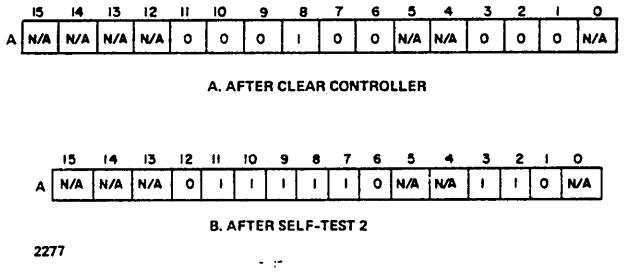


Figure 2-4. Dynamic Status

Since after the execution of self-test 2, the dynamic status does not indicate the true status of the controller, a clear controller command should be issued before performing any further operations.

Self-test 2 is rejected if the controller is busy or a protect fault is detected.

Self-Test 3

Self-test 3 checks the capability of the MTTC to read data via the DMA channel and transmit data via the A/Q channel. With the Q register loaded according to table 2-3, execution of an output instruction causes the MTTC to read data from the memory at the location specified by the first word address and bank select commands, and write the data into the MTTC A-out register.

Upon acceptance of the output instruction command, the controller becomes busy and remains busy until the operation is complete. EOP status is reset 1 microsecond after EOP.

After completion of the output instruction command, A-out status should be read. The A-out status should be compared with the original contents of the address specified by the last word address and bank select. If these two are not identical, the controller is defective.

Self-test 3 must be preceded by a clear controller command. Self-test 3 is rejected if the controller is busy or a protect fault is detected.

Self-Test 4

Self-test 4 checks the A/Q channel data path of the MTTC by reading data via the A/Q channel and writing the same data via the DMA channel. With the Q register loaded according to table 2-3, execution of an output instruction causes the MTTC to read the data contained in the A register and then write it into memory at the address specified by the first word address and bank select commands.

Upon acceptance of this command, the controller becomes busy and remains busy until the transfer into memory is complete, after which EOP status is set; busy status is reset 1 microsecond later. The CPU should then compare the word written into the memory by the MTTC with the one originally sent via the A/Q. If they are not identical, the controller is defective.

Self-test 4 must be preceded by a clear controller command. Self-test 4 is rejected if the MTTC is busy or a protect fault is detected.

Assemble/Sense Next Ready

The assemble/sense next ready command has two modes of operation selected by bit 15 of the A register. With A15 set, the assemble mode is selected. This allows the CPU to receive information about the ready status of each of the four units. With A15 clear, the sense mode is selected. This mode allows the CPU to receive notification when a change in the ready status occurs. Figure 2-5 shows the A-register format for assemble/sense next ready.

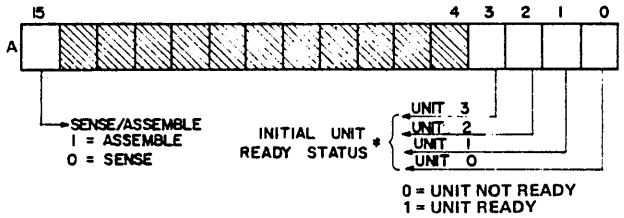


Figure 2-5. A Register Format for Assemble/Sense Next Ready

Assemble Ready Status

With the Q register loaded according to table 2-3 and A15 set to 1 (all other bits of the A register are irrelevant), execution of an output instruction causes the MTTC to go busy and sample unit ready status of each of the four MTTC units. The assemble status is then written into the register file at address E_{16}. The processor can read this status by executing a load file address command specifying file address E_{16} and then reading file status.

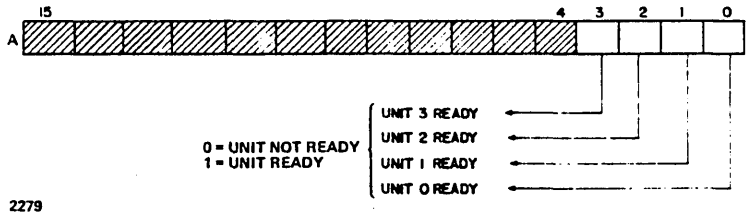


Figure 2-6. Read Status Format

Figure 2-6 illustrates the ready status format that is contained in file address E_{16} after execution of the assemble ready status command.

After execution of the command, all units are deselected, although controller protected status is not affected. The CPU must issue a new unit select command.

Sense Next Ready

This command allows rewinding to be performed in parallel (overlap rewind) with the CPU receiving notification (EOP interrupt) of the completion of each rewind by detecting any change in the unit ready status of the four units (that is, a unit that was previously not ready becoming ready). With the Q register loaded according to table 2-3 and with A15 reset to 0, bits 0 through 3 of the A register specify the initial unit ready status. Each bit corresponds to one of the units (A00 is unit 0, A01 is unit 1, A02 is unit 2, and A03 is unit 3). Upon acceptance of this command, the controller becomes busy and samples the ready status of each of the four units. The result of this sampling is then compared with the unit ready status originally received via the A register. The sample and compare operation continues until the original unit ready status and the actual (sampled) unit ready status are not equal, indicating that one or more of the units that was previously not ready has become ready, or vice versa.

EOP status and EOP interrupt, if requested, are generated when a change in the ready status is detected. Busy status is then reset 1 microsecond after EOP. After completion of this command, file address E_{16} contains the sampled status in which the change from the original was detected. The CPU should read this status to determine which of the units has become ready.

Execution of the sense next ready command causes all units to be deselected although controller protected status is not affected. The processor must issue a new unit select command.

The sense next ready command can be used for detecting either the completion of a rewind operation or the mounting of a new tape reel on one of the transports. When used together with the rewind command, the sense next ready command detects the completion of the rewind operation. When used with the rewind off-line command, the sense next ready command can detect when the operator mounts a new tape reel on the transport and manually places the transport on-line.

The assemble/sense next ready command is rejected if the controller is off-bus, the controller is busy, or a protect fault is detected.

INPUT TO A OPERATIONS

With the Q register loaded according to table 2-3, execution of an input instruction causes the controller to load the A register with the desired controller status. All status requests except dynamic status requests are rejected if the controller is busy.

Figure 2-7 shows the A-register format for status 1. Status 1 requests are always accepted.

Unit Ready Bit

If A00 is set, the selected transport is ready to receive commands. A00 not set indicates that the selected transport is either rewinding or off-line.

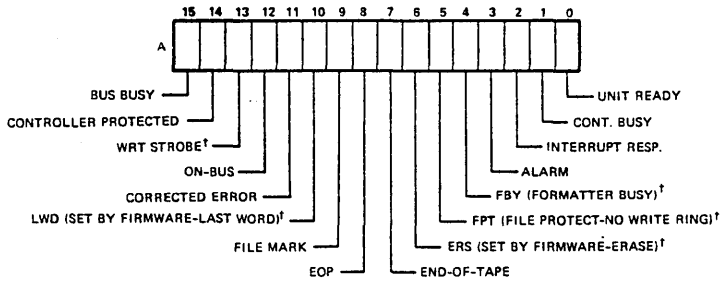


Figure 2-7. A-Register Format for Status 1

The following conditions should exist for the unit to be ready:

- All interlocks are satisfied
- Initial load or rewind sequence is completed
- Transport is on-line
- Transport is not rewinding or unloading

If the unit becomes not ready during any motion function except rewind, the motion terminates and the alarm status becomes active.

Controller Busy

When bit A01 is set, the controller is busy upon acceptance of the following commands:

- Unit select
- Bus connect
- Director function
- Test modes 1, 2, 3, and 4
- Assemble/sense next ready

All commands to the controller except clear controller and dynamic status requests are rejected when the busy status is set.

The busy status is cleared by the completion of the command, which caused the controller to become busy. A master clear controller also clears the busy status.

End-of-Operation

When EOP status (A08) is set, it indicates that the previous operations have been completed.

EOP status is reset approximately 1 microsecond after busy status is set and becomes set 1 microsecond before busy status is reset.

No new motion commands are accepted by the controller when it is busy. When EOP is set, it indicates that the controller will finish its current operation within 1 microsecond.

An EOP interrupt, if enabled, is sent to the CPU 1 microsecond before EOP status is set.

Interrupt Response

If bit A02 is set, the MTTC's interrupt signal is active. A02 is reset by clear interrupts, clear controller, and master clear.

File Mark

File mark status (A09) is set whenever the read head of the selected transport detects the code of a file mark during a read, space, write file mark, or search file mark operation.

End-of-Tape

EOT (end-of-tape) status (A07) is an indication that an end-of-tape marker was detected by the sensor. This is a warning that there is only approximately 18 feet (5.5 meters) of tape left on the reel. EOT can occur only during forward tape motion.

EOT status becomes active and causes alarm status to become active approximately 3 microseconds before the end of the current operation regardless of when the end of the tape marker was detected. An alarm interrupt is generated 2 microseconds after alarm status if alarm interrupt was enabled.

Once an EOT marker is detected, the transport continues sending EOT status until the EOT marker passes under the sensor in the reverse direction. Consequently, all director function operations initiated in the tape region following the EOT marker terminate with alarm and EOT status.

Corrected Error

Bit A11 becomes set whenever a single-channel dropout has been detected during a data transfer and the formatter performed an error correction. This status serves only as a warning since the data is correct.

Acceptance of a new motion function, clear controller, or master clear resets the corrected error status.

Alarm (A03)

A03 becomes active when an uncorrectable error occurs during a data transfer or conditions arise that require external intervention. Bus relinquish, ready, EOT status bits, and alarm status should be checked to determine the cause of alarm (note that the alarm status word may be checked only after the controller becomes not busy).

Any alarm condition except EOT causes a termination of the data transfer.

During write operations the record being written is terminated immediately after the error condition is detected, resulting in a shorter record than requested. The controller becomes not busy and the tape motion ceases after the appropriate post record delay.

During read operations DMA data transfers ceases immediately after the detection of the error, but the controller remains busy and tape motion continues until the next interrecord gap.

If alarm interrupt was enabled, an alarm interrupt is sent to the CPU approximately 1 microsecond before EOP status becomes active regardless of when alarm status became active.

The alarm status bit and the alarm status word are reset upon acceptance of any new command that causes the controller to become busy. Clear controller master clear does not clear the alarm status word.

On-Bus and Bus Busy

On-bus and bus busy status bits (A12 and A15) together determine the status and usage of the

TABLE 2-7. FORMATTER/CONTROLLER BUS STATUS

Bus Busy	On Bus	Formatter/Controller Bus Status
0	0	The bus is not being used by either MTTC
0	1	This MTTC has control of the bus and can access the formatter.
1	0	The other MTTC has control of the bus.
1	1	This MTTC has control of the bus, and the alternate controller is sending a bus request. This condition generates an interrupt if alternate bus request interrupt is selected.

formatter/controller bus according to table 2-7. These status conditions are not supported by CYBER 18 systems.

Unit select, director function, and transport status requests are rejected if on-bus status is not set.

On-bus status is cleared when:

- A bus release command is accepted
- A bus is relinquished due to a bus force from the other CPU
- A master clear is generated

Bus busy is reset when the alternate controller releases or relinquishes the bus.

Controller Protected

Bit A14, when active, indicates that a protected transport is selected. The controller rejects all unprotected output instructions. Unprotected status requests are accepted.

Deselecting the protected unit or selecting an unprotected unit clears A14.

Alarm Status

Figure 2-8 shows the alarm status A-register bit assignments. The alarm status word is valid only when the alarm status bit of dynamic status is active.

The alarm status word is cleared by the acceptance of any new command that causes the controller to become busy. Clear controller or master clear does not clear the alarm status word.

Alarm status requests are rejected if the controller is busy. Alarm status resides in the MTTC register file in address B_{16} and A_{16}. To read alarm status, A_{16} should be loaded by a load file address command, and then the status of the file registers should be read.

ES0 through ES4

ES0 through ES4 are uncorrectable hard errors that occur during data transfers. The transfer is terminated when one of these errors is detected. ES0 may occur during space, search, file mark, or read operations when no characters are detected within 25 feet of tape movement after initiation of the motion. Table 2-8 shows the meaning of ES0 through ES4 for both tape formats.

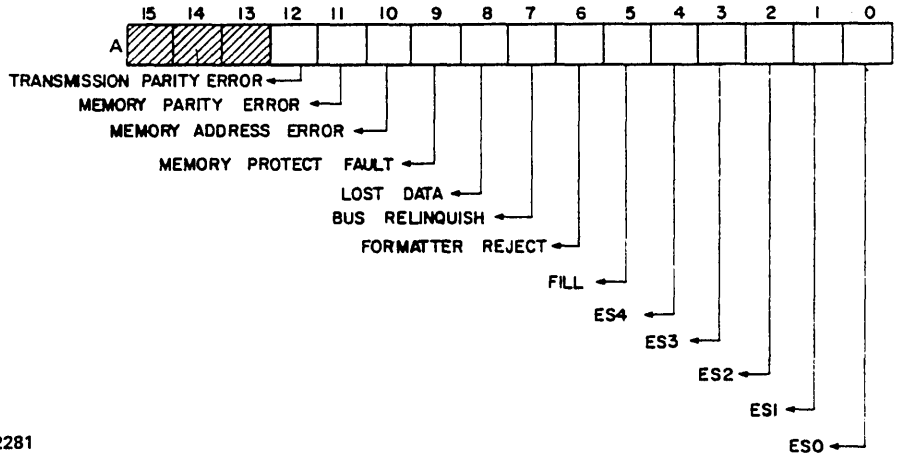


Figure 2-8. Alarm Status A-Register Bits

TABLE 2-8. ES0 THROUGH ES4 ALARM STATUS

Error Status	9-Track Phase Encoding	7-Track or 9-Track NRZI
ES0	False preamble or postamble	VRC error
ES1	Skew error or buffer overflow	CRC error
ES2	Multichannel dropout	LRC error
ES3	Parity error	Not assigned
ES4	No character read in 25 feet (7.62 meters)	No character read in 25 feet (7.62 meters)

Fill

Bit A05 is set if an odd number of bytes are read from the tape during a read operation. The controller fills the lower portion of the last word transferred into the memory with random data. Fill status is an indication that the last byte transferred into the memory originated from the controller, not the tape.

Formatter Reject

Bit A06, when active, indicates that the formatter rejected a command from the controller.

The following conditions activate the formatter reject:

- Reverse commands to a transport at BOT
- Write commands to a transport unit not having a write-enable ring inserted

Bus Relinquish

Bit A07 is set if bus control was relinquished by the controller in response to a bus-force signal from another controller.

The bus relinquish status bit has precedence over all other alarm status bits. If A07 is active, all other bits should be disregarded.

This condition is not supported by CYBER 18 systems.

Lost Data

Bit A08 is set if an attempt is made to transfer data at a faster rate than the controller can handle.

Memory Protect Fault

Bit A09 is set if a transfer initiated by an unprotected instruction attempts to write data into a protected area of memory. The original contents of the memory are not changed.

Memory Address Error

Bit A10 is set if an attempt is made to reference a nonexistent memory bank.

Memory Parity Error

Bit A11 is set if a parity error occurs during a read from memory.

Transmission Parity Error

Bit A12 is set if a parity error is detected during a data transmission between the formatter and controller.

Transport Status

The transport status describes the physical configuration and operating conditions of the selected transport. Figure 2-9 shows the A-register transport status bit assignments.

Transport status requests are rejected if the controller is off-bus or the controller is busy.

The transport mode code and speed option statuses are sampled during selection of the unit. If the unit is off-line when the transport is selected, reading transport status does not give the correct status for the previously mentioned status bits even though the unit may have been placed on-line. Transport status requests should be preceded by a unit select command to ensure that the status is correct.

NRZI

Bit A01, when active, indicates that the selected transport is in the NRZI operating mode. When not active, the selected transport is in the PE operating mode.

Speed Option

Bit A02, when active, indicates the selected transport is operating at 50 ips. When A02 is inactive, the selected transport is operating at 25 ips.

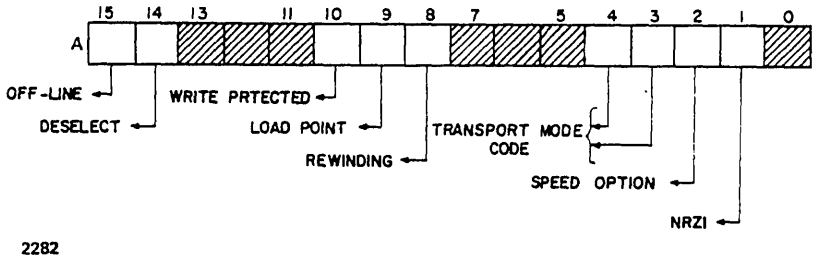


Figure 2-9. A-Register Transport Status

Transport Mode Code

Bits A03 and A04 describe the physical configuration of the selected transport. Table 2-9 defines the code.

TABLE 2-9. TRANSPORT MODE CODE

A04	A03	Transport Description
0	0	7-track NRZI
0	1	9-track dual mode (PE or NRZI)
1	0	9-track NRZI
1	1	9-track PE

Rewinding

Bit A08 is set whenever the selected transport is performing a rewind operation. A08 is cleared upon completion of the rewind.

Load Point

Bit A09, when active, indicates that the sensor of the selected transport is over a BOT reflective marker.

Write Protected

Bit A10, when active, indicates that the tape reel mounted on the selected transport does not have a write-enable ring inserted. Write, erase, or write file mark commands are rejected by the formatter.

Deselect

Bit A14, when active, indicates that no unit has been selected.

Off-Line

Bit A15, when active, indicates that the transport is off-line.

Current Bank Status

The lower two bits of the A register are filled with the code of the memory bank that was last referenced. The upper bits of the A register are filled with zeros.

This request is rejected if the controller is busy.

Current Word Status

This status provides the address of the last memory reference plus 1 (LWA + 1).

This request is rejected if the controller is busy.

Block Length Status

The block length status indicates how many data words remain to be transferred when the data transfer is terminated or when the end of record is reached. Block length status is resident in the MTTC register file at addresses 8 and 9 and is read in the same manner as alarm status. After a data transfer operation, the block length status specifies the number of words that remain to be transferred minus 1 (for example, if 100_{16} words remain to be transferred, block length status is FF_{16}). If the entire block length has been transferred, block length status is $FFFF_{16}$.

A-Out Status

A-out status is used for reading the results of the MTTC self-tests 1, 2, and 3. After execution of one of these self-tests, the result resides in the MTTC A-out register. Since the A-out register is also used for sending other data on the A-lines, self-test results should be read directly following the execution of the self-test to ensure that the result is not lost.

File Register Status

File register status requests allow the contents of the MTTC internal 16 register file to be read. The file address is specified by the load file address command. Since the file is 8 bits wide, two consecutive file words are loaded into the A register. The lower portion of the A register is loaded with the contents of the file at the address specified by the load file address command. The upper portion of the A register is loaded with the contents of the specified file address plus one.

Table 2-10 specifies the usage of the file registers.

LRC and CRC Status

After an NRZI read operation, file addresses 12 and 13 contain the CRC and LRC characters whenever the entire record was read. This status is read in the same manner as alarm status.

TABLE 2-10. FILE USAGE

File Address	Usage	
REG. 1 + 0	Return address†	
REG. 3 + 2	N/A	
REG. 5 + 4	Interrupt storage†	
REG. 7 + 6	Transport status	
REG. 9 + 8	Block length	
REG. B + A	Alarm status	
REG. D + C	CRC character (NRZI read) 9 track only	LRC character (NRZI read) 7 and 9 track
REG. F + E	N/A	Ready status

†Used for internal firmware operations only.

INSTALLATION AND CHECKOUT 3

Refer to the CYBER 18 Computer Systems with MOS Memory Installation Manual for installation of magnetic tape transport subsystems.

The magnetic tape transport controller (MTTC) provides the interface between the CYBER 18 Computer and the DZ101-A Magnetic Tape Formatter. The formatter in turn controls up to four magnetic tape transports.

The CYBER 18 sends functions or status requests to the MTTC via the A/Q channel. The functions received from the CYBER 18 are decoded by the MTTC. If the function requires the operation of the tape transport, the MTTC issues the appropriate command to the formatter. The formatter in turn transmits proper control signals to the transport to perform the operation. The MTTC is a microprogrammed controller. The hardware is of a general nature with the firmware providing the interface to the formatter. The controller contains on one standard PWA board: a 1K-by-16-bit PROM, an ALU for performing logical and arithmetic operations, a 16-by-8-bit register file, auxiliary registers, and other random logic necessary to read, decode, and execute microinstructions. Figure 4-1 illustrates the common device controller block diagram.

Data transfers between the CYBER 18 and the controller are made via the DMA channel. Control and status information is via the A/Q channel.

FORMAT/CONTROLLER INTERFACE SIGNALS

The following subsection describe the controller/formatter interface signals. All formatter and controller pulse signals are latched by the controller. The output from the latches are then input to jump condition multiplexers. Level signals are also input directly to jump condition multiplexers.

TRANSPORT ADDRESS (TADO, TADI)

These lines determine which one of the four transports has been selected for operation with the formatter. The codes correspond to the transport select lines as follows:

TADO	TADI	TRANSPORT UNIT SELECTION
False	False	Unit 0 select
False	True	Unit 1 select
True	False	Unit 2 select
True	True	Unit 3 select

INITIATE COMMAND (GO)

This is a pulse that initiates the commands specified by the command lines. The information to the command lines is transferred to the relevant command registers on the falling edge of the GO pulse. If the formatter and the selected transport are ready, the command is accepted and FBY (formatter busy) is set (active).

COMMAND LINES

The levels of these lines specify a command to the formatter. They are transferred to a command register on the trailing edge of the GO pulse. The levels should be held ready for 0.5 microseconds immediately before and after the trailing edge of the GO pulse. The command lines are as follows:

- REV
- WRT
- WFM
- ERASE
- THR
- SPM

REVERSE/FORWARD (REV)

This level if active specifies reverse tape motion, and if inactive, specifies forward tape motion.

WRITE/READ (WRT)

This level if active specifies the write mode of operation and if inactive specifies the read mode of operation.

WRITE FILE MARK (WFM)

If this level is active along with active WRT, it specifies a file mark to be written on tape.

ERASE (ERASE)

If this level is active in conjunction with WRT being active, it causes the formatter to execute a pseudo write command. A length of tape as defined by last word (LWD) will be erased.

Alternately, if the ERASE, WRT, and WFM command lines are all active, the formatter writes a fixed erase gap of approximately 6 inches (152 millimeters) of tape.

THRESHOLD (THR)

If the level of this line is active in conjunction with WRT being false, it specifies the read recovery mode. The read recovery mode specifies a lower threshold within the read amplifiers as defined by the threshold control.

SPACING MODE (SPM)

This level is active whenever a spacing operation is to be performed. Read strobe (RSTR) is not transferred over the read data bus lines to the controller during this mode of operation. A combination of write, reverse, and spacing mode causes a backspace until LWD goes active. During this time, write current is off in the selected tape unit. In this mode, only the tape runaway error is enabled.

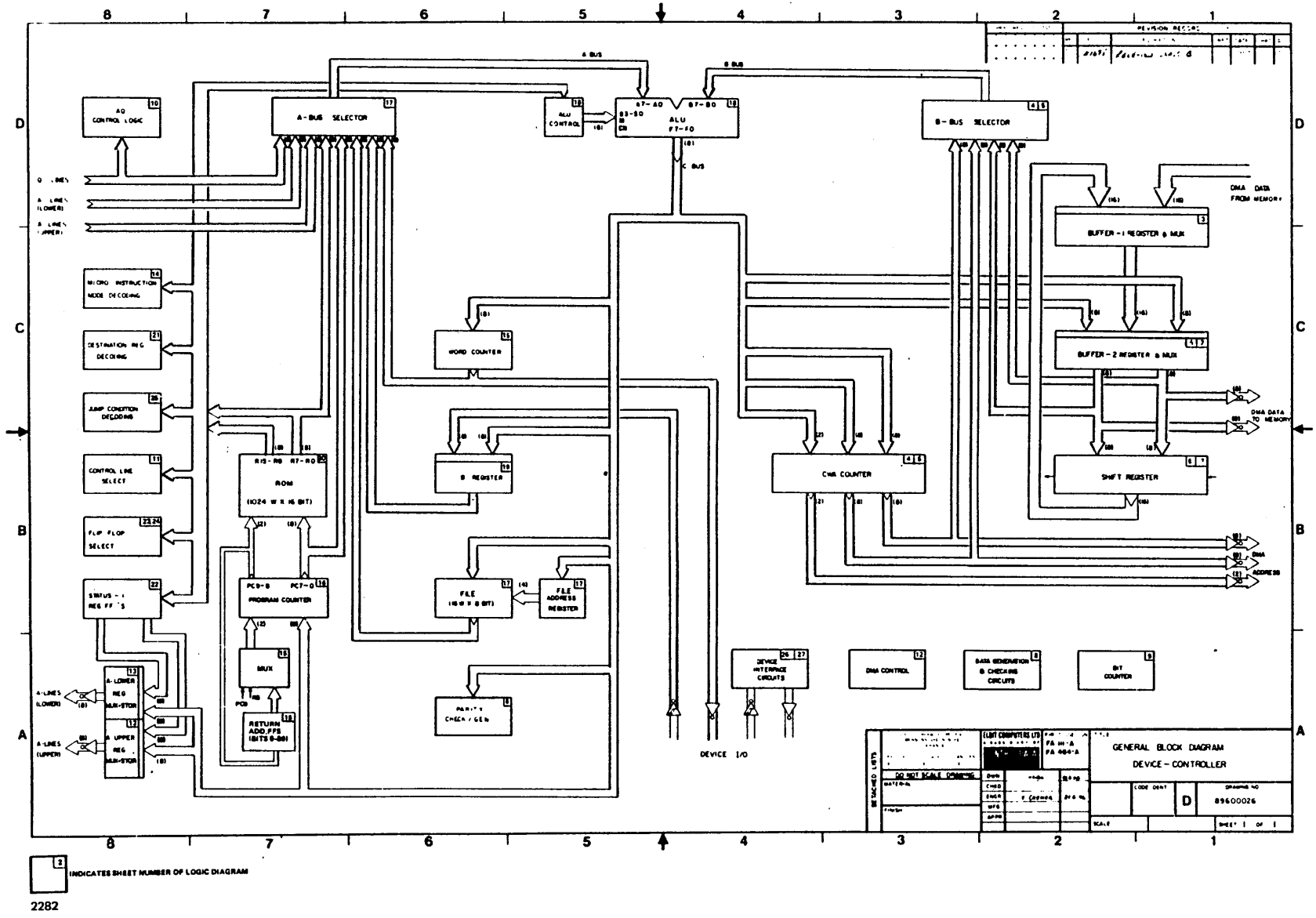


Figure 4-1. Common Device Controller Block Diagram

REWIND (REW)

When this pulse is active it causes the selected transport to revert to the off-line mode.

OFF-LINE (OFL)

This pulse, when active, causes the selected transport to revert to the off-line mode. It is redesignated as NR (not ready) at the transport interface. Issuing REW and OFL commands simultaneously causes the transport to rewind to beginning of tape (BOT) and go off-line.

LAST WORD (LWD)

When this level is active during a write or erase command indicates that the next character to be transferred is the last character of the tape record. This level should be set active at the time the last data character is placed on the interface lines.

FORMATTER ENABLE (FEN)

This level when false causes the formatter to reset to its quiescent state. This line may be used to clear the formatter if controller power is lost or other unusual conditions are encountered.

WRITE DATA LINES (W0 THROUGH W7 AND WP)

The eight write data lines, W0 through W7, are used to transmit data from the controller to the formatter. The formatter normally generates the parity bit (WP). A jumper option on the board allows the controller bit to be used as the parity bit, while the formatter checks it for proper parity. In the case of externally (controller) generated parity, an error status (TFER) is set if incorrect parity is sensed. W0 corresponds to the least significant bit, and W7 to the most significant bit of each character.

The first character of a record should be available on these lines less than 40 character periods after data busy (DBY) goes active until the trailing edge of the first write strobe (WSTR) issued by the formatter. The next character should be placed on the lines within one half of a character period.

Subsequent characters of a record are transferred in this manner until LWD is set active by the controller when the last character is transmitted.

LOW DENSITY (DEN)

This level when active selects the lower of two predetermined densities in a dual-mode transport during write operations and for all NRZI 7-track read/write operations.

ACKNOWLEDGE (ACK)

This pulse is used to acknowledge the transfer of data during a read or write operation.

During a write operation, the ACK signal should be used to acknowledge the data request as signified by the write strobe signal (WSTR). ACK indicates that the controller has accepted the last write strobe and is waiting for the next strobe.

During a read operation, the ACK signal should be used to indicate the readiness of the controller to receive data from the formatter. ACK indicates that the controller has accepted the last byte and is ready for a read strobe for the next byte.

INTERFACE OUTPUTS (FORMATTER TO CONTROLLER)

FORMATTER BUSY (FBY)

This level becomes active on the trailing edge of the GO pulse if the command issued by the controller is accepted by the formatter. The level remains true until the appropriate post-record delay has elapsed, after which the formatter is available to accept another command. The off-line and rewind commands cause the formatter to go busy long enough to validate the command or to complete a write jog if the write electronics are on.

IDENTIFICATION (IDENT)

This level goes true to identify phase encoded tapes. If an identification burst is detected as the BOT marker passes over the read head, this line is set true for a short period (approximately 40 through 64 character times). This line is timeshared with check character gate (CCG).

CHECK CHARACTER GATE (CCG)

This level brackets the CRC and/or LRC check characters on the read data lines during NRZI transport operations. The signal line is timeshared with IDENT. The lines can be used to distinguish data and check information by gating read strobes with CCG or its complement.

HARD ERROR (HER)

When this pulse or level is active it indicates that an uncorrectable read error has been detected by the formatter. The HER pulse should be used to sample the error status (ES0 through ES4) lines.

ES0 through ES4 indicates the detected error that caused the hard error (HER) indication. The status lines are defined as follows:

- 1600 PE

  ES0 - False preamble or postamble detected

  ES1 - Skew error or buffer overflow

  ES2 - Multichannel dropout

  ES3 - Parity error during read after write or without associated channel dropouts

  ES4 - No character read in 25 feet (7.62 meters)

- NRZI

  ES0 - VRC error

  ES1 - CRC error

  ES2 - LRC error

  ES3 - Not assigned

  ES4 - No characters read in 25 feet (7.62 meters)

CORRECTED ERROR (CER)

This line is set active (pulsed) when a single channel dropout has been detected and the formatter is performing error correction.

FILE MARK (FMK)

This line is set active (pulsed) whenever the formatter read logic has detected a file mark. This may be during any read forward, read reverse, or read after write file mark commands.

TRANSPORT STATUS AND CONFIGURATION

These lines indicate the relative status or configuration of the selected transport; their definitions are identical to the definitions in the transport to formatter input description. These lines are as follows:

- Transport Status

  RDY - Ready

  ONL - On-line

  RWS - Rewinding

  FPT - File protect

  LDP - Load point (BOT)

  EOT - End of tape

- Configuration

  MOP1 - Mode option 1

  MOP2 - Mode option 2

  SOP - Speed option

WRITE STROBE (WSTR)

This is a pulse generated for each data character to be written on tape. The write data lines (W0 through W7 and WP) are sampled by WSTR and are transferred into the write register of the formatter.

The first character must be available before the first WSTR is generated, and subsequent characters must be set up within one half of a character period after the trailing edge of each WSTR pulse.

Data transferred during erase commands, while the WSTR is still active, is ignored by the formatter.

READ STROBE (RSTR)

This is a pulse level that identifies each read character on the read lines (R0 through R7 and RP). RSTR pulses are nominally spaced at character intervals but vary due to skew and speed fluctuations. The RSTR pulse should be used to sample the read data lines.

READ DATA (R0 THROUGH R7 AND RP)

These levels are used to transmit the data from the formatter to the controller during a read operation. Each character should be sampled during the RSTR pulse time.

COMMAND REJECT (CRJ)

The command reject signal (pulse) is used to signify those commands that the formatter or transport cannot logically perform or respond to at this time. The following conditions cause the reject command signal to be active:

- Commands to a transport unit that is busy
- Reverse commands to a transport unit at BOT
- Write command issued to a transport not having a write-enable ring installed
- Read forward or space forward commands issued to a transport having a write WCON status condition (reading with write current on)
- Write and reverse commands issued at the same time unless spacing mode (SPM) is active

DATA TRANSFER ERROR (TFER)

When active this signal level indicates the controller failed to acknowledge the data request or transfer during either a write or read operation. This signal level is also used during a write operation to indicate the incorrect data/parity transfer from the controller for data bus options that include the parity bit.

READ MODE STATUS (RDM)

When active this signal level indicates that the formatter is performing a read operation (not writing or spacing).

NRZI MODE (NRZ)

When active this signal level indicates that the selected transport is in the NRZI operating mode.

7 TRACK (7-TR)

When active this signal level indicates that the selected transport is a 7-track unit.

MICROPROGRAMMING CONCEPT

INITIALIZATION

Power on, master clear, or clear controller clears the program counter (PC). Upon completion of the master clear or clear controller pulse, microcode execution of the master clear routine, whose starting address is zero, commences. Three possible conditions can reset the PC to zero:

- Master clear (power ON or from panel)
- Clear controller
- Force bus release

The master clear routine determines the reason for the PC reset so that appropriate action may be taken. First, the force bus line is sampled and, if active, a branch is made to a bus relinquish routine that sets bus relinquish status and alarm status. Next, the ROM execute flip-flop (ROM EXEC F/F), which is used to inform the microcodes that an A/Q command has been received from the processor, is sampled. The ROM EXEC F/F being active indicates that a clear controller command has been received. This causes a branch to a body of code that resets statuses not cleared by the clear controller pulse and issues a reply. If neither ROM EXEC or bus force are active, the reason for the PC reset is assumed to be master clear. For all three PC reset conditions, the program flows through the terminate busy routine. This is an initialization routine that sets the proper statuses and operating flip-flops. Control then passes to the waiting loop.

A/Q WAITING LOOP

The controller initiates all of its operations, with the exception of dynamic status requests and clear controller, from the waiting loop. This loop continuously samples the following jump conditions:

- A/Q execute flip-flop set - This flip-flop is set whenever an A/Q command, with Q04 = 0 and the proper equipment code are received.
- Autoload line active - This line is activated whenever the autoload switch is pushed. (Not supported by CYBER 18.)
- On/off-line switch - Whenever the off-line maintenance switch is placed in the off-line position this line goes low (active).
- Alternate bus request line active - If the controller is on bus, and alternate interrupt was requested, an interrupt is generated. (Not supported by CYBER 18.)

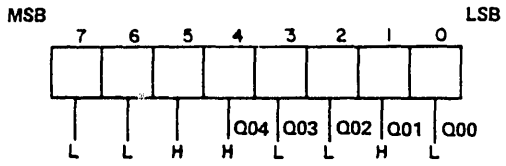
Whenever any one of the above conditions is active, an exit is made from the waiting loop and the required action is performed. All actions are terminated by a return to the waiting loop.

A/Q EXECUTE

The function code Q-bit lines Q00 through Q04 together with the WRITE signal are one input to the A-bus selector. When the A/Q execute flip-flop is detected as being active by the waiting loop routine, the Q input to the A bus selector is complemented, masked, and loaded directly into the PC. This preload causes a 32-way microprogram branch. Each of the 32 branch locations contains the starting address of the routine, which performs the function whose code is found in Q00 through Q04.

Not all of the 32 function codes are valid. The branch location of illegal codes contains a jump to the reject routine. This routine issues a reject and then jumps back to the waiting loop.

The following is an example of the preload. The first word address function (Q=60(2)) is received. Since this function is initiated by an output instruction, the WRITE signal is active. The complemented Q input to the A-bus selector is shown below.



Bits 6 and 7 are always low, bit 5 is high because the WRITE signal is active; bit 4 is made high by a program-mask operation; bits 3, 2, and 0 are low; and bit 1 is high. When this code (32_{16}) is loaded into the PC, a branch is made to ROM location 32_{16}, which contains a branch instruction to the start of the first word address routine. Bits 8, 9, and 10 of the PC are set to zero by the hardware for the preload operation.

The routines for executing each one of the A/Q functions can be divided into two categories: those that cause the controller to go busy, and those that do not.

NOT-BUSY ROUTINES

Routines that do not cause the controller to go busy (such as first word address) are checked for legality to determine whether they will be accepted (replied to) or rejected. Once a reply or reject is issued, a jump back to the waiting loop is made.

The following conditions cause the reject to be active:

- Commands to a transport that is busy
- Reverse commands to a tranport at BOT
- Write commands to a transport that does not have a write-enable ring installed.

First Word Address (CWA)

The data received from the CPU is transferred from the A lines (lower and upper) of the A-bus selector via the ALU

to the CWA registers (CWAU and CWAL). These registers provide 16 bits of the address during the DMA transfer operations. At the completion of a DMA transfer, the CWAL register is incremented. Overflow from CWAL increments the CWAU and overflow from the CWAU increments the CWAL.

Bank Select

Bits 6 and 7 of the A lines are transferred into the CWA upper upper (CWAUU) register of the CWA register. This register selects one of four 65K memory banks.

Load File Address

The lower 8 bits of the A lines are transferred to the B register. When the file status is requested, the contents of the B register are moved to the file address register.

Block Length

The data received on the A lines is complemented and transferred to file address 8 and 9. File address 8 contains the lower 8 bits, and address 9 contains the upper. During data transfers, file address 8 is incremented. If there is a carry out, this indicates that the lower 8 bits of the block length have reached zero, in which case the upper 8 bits (file 9) are incremented. If another carry out results, this indicates that the entire block length has reached zero and the data transfer is to be terminated.

Interrupt Request

A-line bits 5, 6, and 7 are tested to determine interrupt conditions. Corresponding flag flip-flops are set so that the requested interrupts may be activated when conditions warrant. If the alarm interrupt request (bit A05) is active, the alarm status bit is tested. If the alarm status bit is active, the interrupt response is activated.

A-Out Status

This routine simply issues a reply, sending the contents of the controlled A-out register to the CPU.

Current Word Status

CWAL will be moved to A-out lower and CWAU are moved to A-out upper, allowing the CPU to read the contents of the CWA registers.

Current Bank Status

The two bits of the CWAUU are decoded and 0, 1, 2, or 3 are placed in the A-out lower register according to the results of the decoded bits. The A-out upper is set to zero.

File Status

The contents of the B register are loaded into the file address register. The contents of the file at address B are loaded into the A-out lower register. The B address is then incremented by one and again loaded into the file address. The file contents of B+1 are moved into the A-out upper register.

Transport Status

The jump conditions of the device status lines are tested. If the line is active, a 1 is placed in the bit position corresponding to the device status. An inactive signal causes a 0 to be placed in the bit position. Transport status bits are assembled in this manner until the entire status word is assembled.

BUSY ROUTINES

For functions that cause the controller to go busy, a check is also made for the legality of the command. If all conditions for acceptance are present, a reply is issued and the flip-flop is set. This flip-flop informs the A/Q control logic to reject all commands with Q04=0. The busy flip-flop remains set for the duration of the operation.

Completion of the operation causes a branch to the terminate busy routine. This routine sets the initial conditions that were changed by execution of the previous command, checks whether an EOP or alarm interrupt is to be generated, resets the busy flip-flop, and returns control to the waiting loop.

The following two command routines are necessary for all tape transport operations:

Bus Connect Routine - The execution of this routine activates the on bus flip-flop. This flip-flop enables all the output lines to the formatter.

Unit Select Routine - This routine activates formatter lines TADO and TADI. These two lines provide the formatter with the code of the transport that the CPU selected. The DEN (low density) and PAR (even parity) lines may also be activated depending on the parity and density options selected by the CPU in the unit select command.

DIRECTOR FUNCTIONS

Once a bus connect and unit select are made, all operations with the tape transport are initiated via a director function command. When the Q function code is decoded as code 31_{16}, a branch is made to the director function routine. This routine checks that the controller is on-bus, a unit has been selected, and that the selected unit is ready. If any one of these conditions is not true, the command is rejected. If all the conditions are true a replay is issued, and the busy flip-flop is set.

The 4-bit director function field, A00 through A03, is decoded in the same manner as in the Q-function code. This field is masked and loaded directly into the PC causing a 16-way microprogram branch.

The MTTC issues commands to the formatter by activating the five formatter command lines in combinations. The command coding is given in table 4-1. Upon receipt of a GO pulse from the controller, the formatter initiates the execution of the command and becomes busy. The formatter remains busy for the duration of the operation. If a command to the formatter is illegal (for example, write commands to units not having the write-enable ring inserted), the formatter issues a command reject (CRJ) pulse.

All director function operations are terminated when the formatter busy (FBY) signal goes low. This termination is

TABLE 4-1. DIRECTOR FUNCTION COMMAND CODING

I/O Line	Function								
	Read REV	Space REV	Read FWD	Space FWD	Write	Controlled Backspace	Write File Mark	Erase Variable	Erase Fixed
GO (Pulse)	X	X	X	X	X	X	X	X	X
WRT					X	X	X	X	X
REV	X	X				X			
WFM							X		X
ERASE								X	X
SPM		X		X		X			

done through a terminate director function routine which checks the following conditions:

- File Mark (FMK) - To determine if a code of a file mark was encountered during the previous operation.
- Hard Error (HER) - Hard error statuses ES0 through ES3 are latched in the HER shift register. The output of this register goes active whenever a HER pulse is present. Upon detection of this latched HER pulse, a jump is made to a routine that shifts and samples the HER shift register to determine which ES condition causes the hard error. The ES conditions are assembled in the alarm status word where it is available to the CPU.
- End-of-Tape (EOT) - To determine if an end-of-tape marker passed under the sensor.
- Corrected Error (CER) - This is a warning that a PE error occurred that was corrected by the formatter.
- Command Reject (CRJ) - Alarm statuses are set to inform the CPU that the previous director function command was rejected by the formatter.

The terminate director function routine jumps into the terminate busy routine, which then flows back into the waiting loop.

Space Forward

The controller activates the SPM line, deactivates all other command lines to the formatter, and issues a GO pulse. The formatter goes busy and performs the operation.

Throughout the operation the controller checks the following conditions:

- RDY (Ready) - To determine that the unit continues to be ready throughout the operation
- FBY (Formatter Busy) - An indication that the formatter completed the operation (FBY goes low)

When FBY is low, the MTTC checks the HER (hard error) line. The only error that may occur during space operations is tape runaway (no data encountered within 25 feet (7.62 meters) of commencing tape motion).

Search File Mark Forward

This operation is similar to the space forward operation. The controller issues a space forward command to the formatter. At the completion of the space, the controller checks file mark status (FMK). If no file mark has been detected, the controller issues another space command. Spacing continues until either a FMK or HER (tape runaway error), or RDY = LOW (unit not ready) is detected.

Backspace

The backspace operation is the same as space forward except the reverse (REV) command flip-flop is activated by the controller prior to the GO pulse.

Search File Mark Backward

The controller issues successive backspace commands until one of the following formatter signals becomes active:

- FMK (file mark)
- HER (tape runaway)
- LDP (load point) - When performing reverse motion operations, tape motion always stops at load point.
- RDY - Low; unit becomes not ready.

Fixed Erase

The controller activates the WRT, WFM, and ERASE command lines and issues a GO pulse. The formatter goes busy and erases a 6-inch (152-millimeter) portion of tape. While the fixed erase operation is in progress, the controller samples the FBY and HER lines. When FBY is clear, a jump is made to the terminate director function routine.

Write File Mark

The controller issues a fixed erase command to the formatter. When the fixed erase is complete, the ERASE line is deactivated and another GO pulse is issued commanding the formatter to write a file mark. This two-step operation results in a 6-inch (152-millimeter) erased error followed by a file mark.

Figures 4-2 and 4-3 illustrate the write file mark controller formatter waveforms for NRZI and PE modes.

Read Data

Figures 4-4 and 4-5 illustrate the NRZI and PE read operation waveforms. The controller deactivates all the command lines and issues a GO pulse. The formatter goes busy and initiates forward motion in the selected transport. If the read is in PE and the motion started at BOT, the formatter pulses the IDENT line to inform the controller that a PE identification burst was detected. Once the tape is up to speed and the appropriate pre-record delay has transpired, the formatter issues the first read strobe (RSTR) to inform the controller that the first character is on the R0 through R7 interface lines.

Read data is multiplexed at the input of the B register with the ALU bus. During read operation, R0 through R7 are selected as the input to the B register. When the RTSR pulse is detected, the controller strobes the R0 through R7 data into the B register. The controller then pulses the ACK line to inform the formatter that the character has been received. The character in the B register is passed via the ALU through a parity generator. The output of the generator is compared with the parity bit (RP) received from the formatter. If these two are not equal, the transmission parity alarm status is activated and the alarm bit is set. In addition to parity checking, the controller samples the hard error (HER) line to detect errors in transport to the formatter transmission.

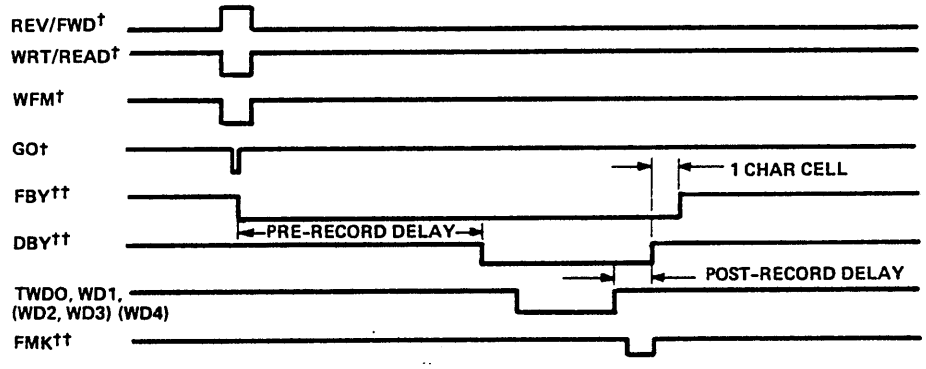
If no errors are detected, the data in the B register is transferred to the buffer 2 upper (BF2U) register. The second character received is transferred to the buffer 2 lower (BF2L) register. In this way two tape bytes are assembled into one processor memory word. Once both the upper and lower bytes are received, the controller initiates a DMA write cycle. The controller is capable of internally buffering four tape bytes. If a fifth byte is received and the DMA cycle is still not complete (BF2 full status is not set), lost data and alarm status are set.

The DMA address is provided by the CWAL; CWAU and CWAUU registers. These three registers form an 18-bit counter combination and the completion of each DMA write cycle increments this counter. The block length is contained in two file address registers at address 8 and 9.

The completion of each DMA write cycle activates a decrement block-length subroutine. This subroutine decrements the two file registers and checks for block length equal to 0.

The read operation continues until one of the following conditions is detected:

- FBY goes low indicating that the end of the record is reached
- HER goes high indicating that one of the ES0 through ES4 error conditions is detected
- RDY goes low indicating that the unit has become not ready
- A transmission parity error is detected
- A lost data condition is detected
- A block length = Zero condition is detected.



†CONTROLLER-TO-FORMATTER WAVEFORMS
††FORMATTER-TO-CONTROLLER WAVEFORMS
NOTES:

1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY FOR WRITE FILE MARK AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.
4. WD3 AND WD3 ARE APPLICABLE TO 7-TRACK TAPE TRANSPORTS ONLY.
5. WD4 IS APPLICABLE TO 9-TRACK TAPE TRANSPORTS ONLY.

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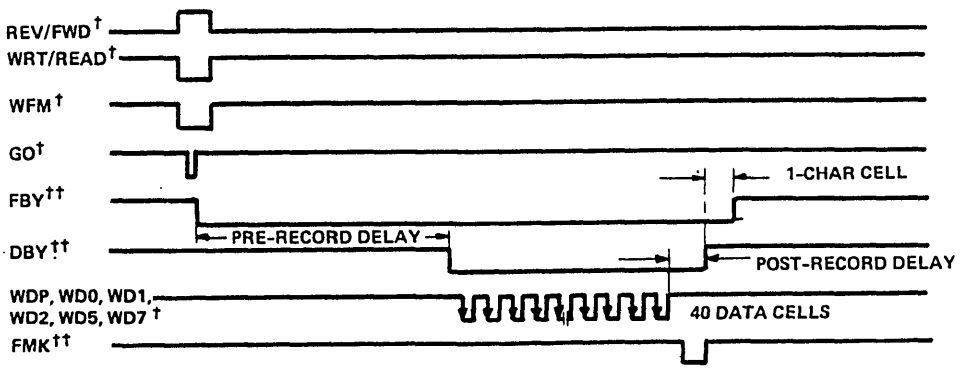
Figure 4-2. NRZI Write File Mark (7-Track)



†CONTROLLER-TO-FORMATTER WAVEFORMS
††FORMATTER-TO-CONTROLLER WAVEFORMS

NOTES:
1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY FOR WRITE, FILE MARK AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.

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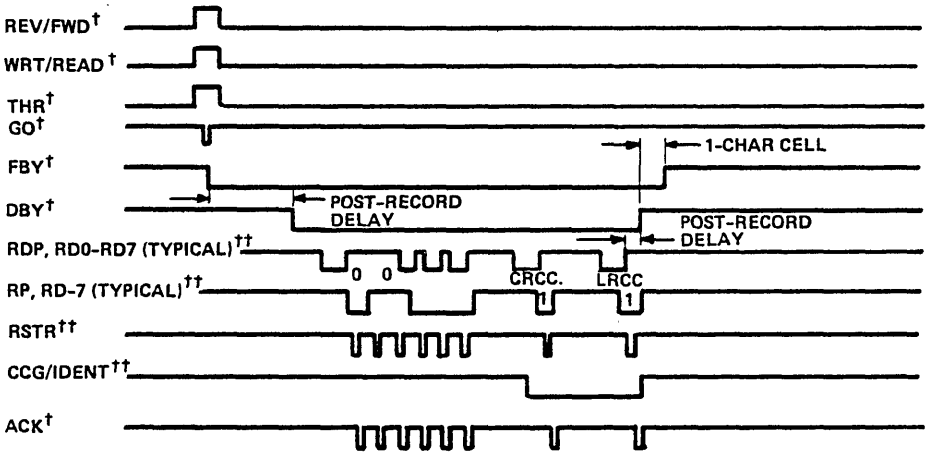
Figure 4-3. Phase Encode Write File Mark



†CONTROLLER-TO-FORMATTER WAVEFORMS
††FORMATTER-TO-CONTROLLER WAVEFORMS

NOTES:
1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY FOR READY OPERATION AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.

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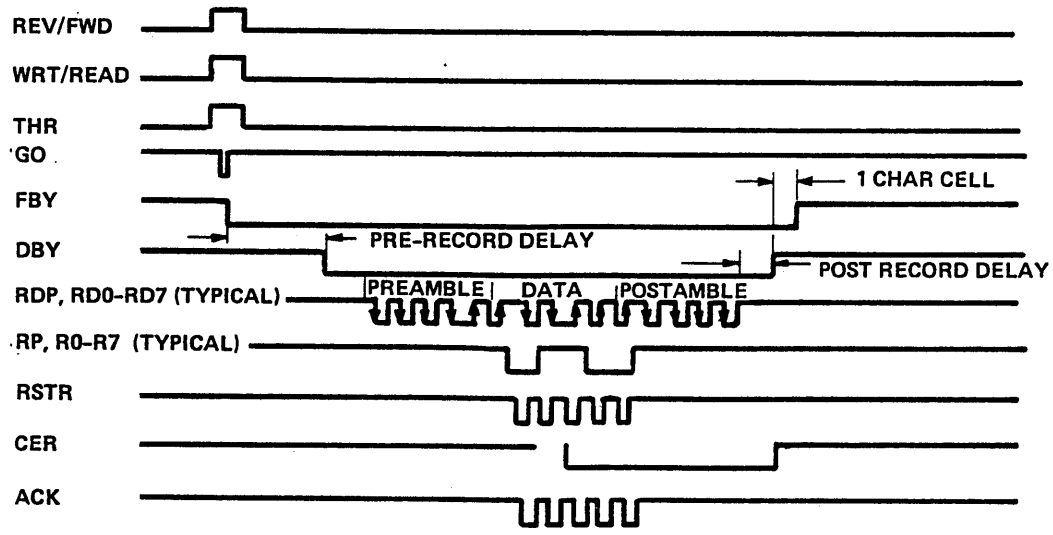
Figure 4-4. NRZI Read Operation



†CONTROLLER-TO-FORMATTER WAVEFORMS.
††FORMATTER-TO-CONTROLLER WAVEFORMS.

NOTES:
1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY FOR READY OPERATION AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.

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Figure 4-5. PE Read Operation

When the formatter reaches the end of a NRZI record, the check character gate (CCG) line is activated to indicate that the next two characters are the LRC and CRC check characters. The controller does not transfer these characters into the memory, but they are written in the file at addresses C_{16} and D_{16} where they are available to the CPU as status.

Write Data

Figures 4-6 and 4-7 show the formatter/controller waveforms for NRZI and PE write operations. The controller activates the WRT command line and issues a GO pulse; the formatter either issues a reject to the command, if the selected unit is not write enabled, or goes busy and intiates forward tape motion.

DMA data is multiplexed at the input of the buffer 2 lower (BF2L) and upper (BF2U) registers with the ALU output bus. During write operations, the DMA data is selected as the input. When the controller issues a DMA read request, the DMA control logic of the CPU strobes the DMA data into the BF2U and BF2L registers and sets BUF2 full status indicating completion of the DMA cycle.

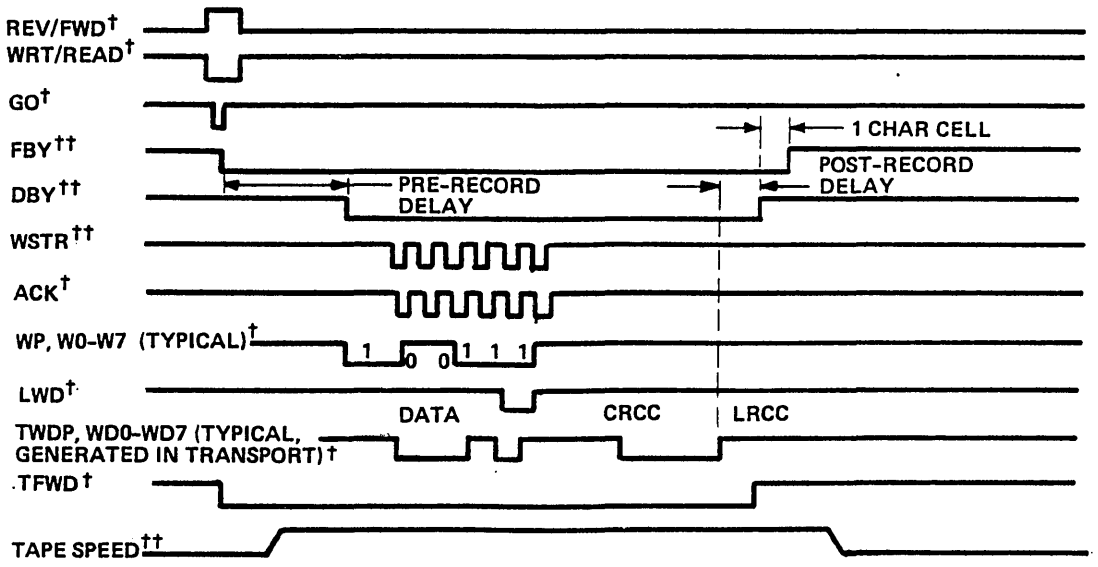
While the formatter is going through the pre-record delay, the controller issues a read request to the DMA. If a leading edge of a WSTR (write strobe) pulse is recieved from the formatter prior to the completion of the DMA cycle, this is a lost data error condition. Having received the DMA data prior to the WSTR, the controller places the first tape byte into the write character (WC) register and places the second tape byte into the B register. With the BF2U and BF2L registers cleared of data, a new DMA request is sent. In this way tape bytes are double-buffered in the WC, B, and BF2 registers.

The output of the WC register is connected to the write data interface lines. Data must be placed in the WC register prior to the leading edge of the WSTR pulse and can be changed only after the trailing edge of WSTR. For each byte placed into the WC register, a parity bit is generated. When the trailing edge of WSTR is detected, data is transferred from the B register into the WC register and the controller waits for the next WSTR. When two tape bytes have been transferred, the block length is decremented; and when block length reaches zero, the last word data (LWD) signal is activated to inform the formatter that the last word is being transferred.

All the error conditions listed in read data also cause premature termination of a write operation.

Controlled Backspace

The controlled backspace allows the tape to be positioned 0.13 inches (3.3 millimeters) ahead of its original position for a record that has been written in error. The controller



†CONTROLLER-TO-FORMATTER WAVEFORMS
††FORMATTER-TO-CONTROLLER WAVEFORMS

NOTES:
1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.

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Figure 4-6. NRZI Write Operation

activates WRT, REV, and SPM, and pulses the GO line. The formatter does a pseudo write in reverse. When the two WSTR pulses are received, the block length is decremented although no data is transferred. When the block length reaches zero, the last word detected (LWD) signal is activated, and the operation is terminated.

Variable Erase

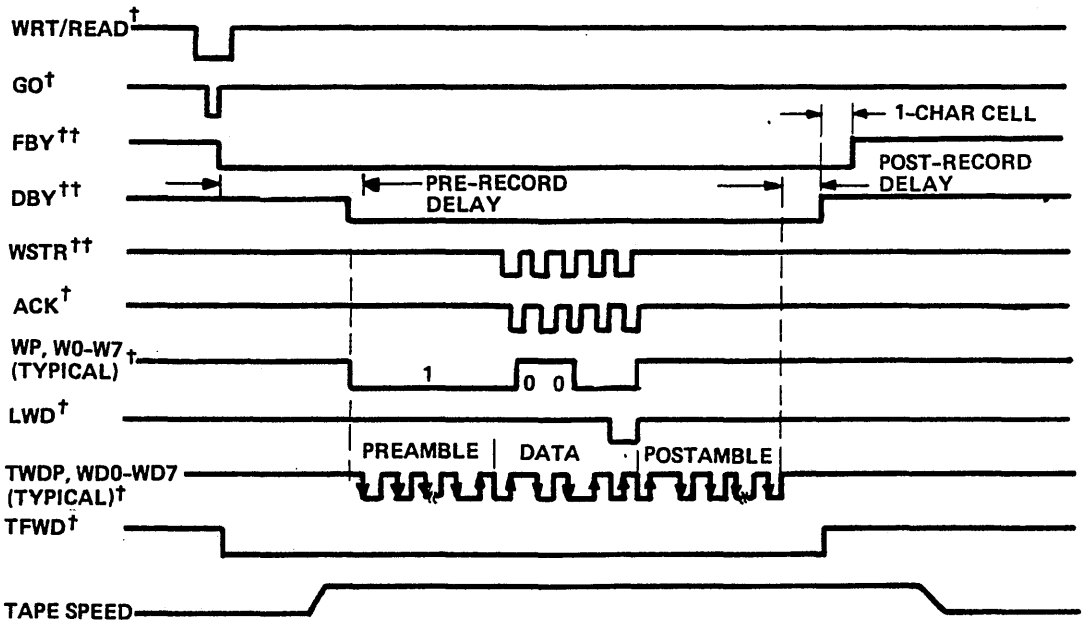
The controller activates the WRT and ERASE command lines and issues a GO pulse. The formatter either rejects the command if the unit is not write enabled, or goes busy and executes a pseudo-write onto the tape, erasing each character cell. For each cell erased, a WSTR is issued. For each two WSTRs received, the controller decrements the block length. When the block length reaches zero, the controller activates the LWD line to terminate the operation.

Autoload

Whenever the autoload switch is activated, the autoload jump condition goes low. When this condition is sensed in the waiting loop, the on-bus and unit-selected jump conditions are sampled. If either of these lines are active, the controller remains in the waiting loop and the autoload operation is not performed. If both of these conditions are not active, an exit is made from the waiting loop to the autoload initiation routine.

This routine sets the autoload flip-flop. This flip-flop is active during the entire autoload operation and ensures coordination of the various routines utilized during the autoload operation. The autoload initiation routine causes a branch to the bus connect routine. At the completion of bus connect, the autoload flip-flop is sampled and control returns to the autoload initiation routine. From autoload initiation, control passes to the assembled sense next ready routine to determine which is the first unit in the daisy-chain that is ready. If no units are ready, control passes back to the waiting loop. Once a unit is found ready, that unit is designated as the autoload device and a

† Not supported by CYBER 18



†CONTROLLER-TO-FORMATTER WAVEFORMS
††FORMATTER-TO-CONTROLLER WAVEFORMS

NOTES:
1. WAVEFORMS ARE SHOWN LOW TRUE.
2. PRE-RECORD DELAY AS SPECIFIED IN TABLE 4-1.
3. POST-RECORD DELAY AS SPECIFIED IN TABLE 4-1.

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Figure 4-7. PE Write Operation

branch is made to the rewind routine. This routine initiates rewind motion and passes control back to the autoload routine. The autoload routine waits until completion of the rewind (autoload unit becomes ready once more). The CWAU and CWAL registers together with the CWA are set to zero and the block length is set to $FFFF_{16}$, specifying the maximum block length. A branch is then made to the read data routine. This routine transfers data from the first record after BOT into the processor memory starting at address 0, bank 0. The transfer continues in the same manner as for normal read until the end of record is reached or an alarm condition occurs. The end of the read routine samples the autoload flip-flop and passes control back to the autoload routine. A check is made of alarm status in the autoload routine. If alarm is active, a determination is made of the number of times that the read failed. Four failures pass control back to the waiting loop. The density select (DEN), read threshold (THR), and parity mode (PAR) flip-flops are changed in the following manner:

	9-Track			7-Track	
	THR	DEN		DEN	PAR
Attempt 1	Normal	High	Attempt 1	High	Binary
Attempt 2	Normal	Low	Attempt 2	Low	Binary
Attempt 3	Low	High	Attempt 3	High	BCD
Attempt 4	Low	Low	Attempt 4	Low	BCD

Self-Tests

The controller has four self-tests for checking hardware via firmware. Self-test 1 checks the internal controller data paths and ALU operations. The data received from the CPU is divided into upper and lower portions, called A

upper and A lower, and transferred via the ALU to the B register and BF2L register. These registers feed the A and B sides of the ALU, respectively. The logical/arithmetic operations, specified by the self-test 1 equation, are performed on these two registers and the result is placed in the lower portion of the A-out register. The A lower data is then transferred and incremented through all 16 file registers and then through all of the controller registers. A-out upper is the final destination of the data. The CPU can examine the self-test 1 result (contained in the A-out register) by reading A-out status.

Self-test 2 checks flip-flops and jump conditions. A clear controller command must be received prior to self-test 2 to ensure that all the flip-flops are in the reset state. Every jump condition flip-flop that should be reset by a clear controller pulse is tested to determine that it is in a reset condition. Any active flip-flop causes the hexadecimal number DEAD to be placed in the A-out register and a return to the waiting loop.

After testing for the reset conditions, the flip-flops are set and then tested for the set condition. The parity generator and all other jump conditions that can be activated by microcode are also tested both in their set and reset states. If all tested conditions are in the proper state, the program loads $ACED_{16}$ into the A-out register and returns to the waiting loop via terminate busy.

Self-test 3 initiates a DMA read request. The data read is placed into the A-out register where it is available to the CPU as status.

Self-test 4 transfers the data in the A-in lower and A-in upper to the BF2L and BF2U registers, respectively and then initiates a DMA write cycle. When the cycle is complete, control passes back to the waiting loop.

Off-Line Maintenance

All of the off-line maintenance operations are initiated by the detection of an active signal caused by the on/off-line switch being in the off position during the waiting loop. An exit is made from the waiting loop to a maintenance initiation routine, which sets the initial conditions of the controller. Control then passes through the bus connect routine to connect onto the bus and the assemble/sense next ready routine, to select the unit on which the maintenance will be performed.

Maintenance switches 1, 2, and 3 are decoded and the selected operation is performed. Each of the operations continuously samples the EOT and on/off-line switch. Detection of EOT causes a termination of tape motion and entry into a loop that waits for the on/off-line switch to be placed in the on-line position so that a return to the waiting loop can be made.

Assemble/Sense Next Ready

This command is used either to assemble the ready status of each of the four units or to sense a change in the ready status. The controller selects each of the units starting with unit 0 and then samples its ready status. A 1 for ready or a 0 for not ready is placed in the bit position corresponding to that unit. This sampling continues until the ready status of all four units is assembled. This assembled status is written into file address E_{16}. If the command is an assemble command, control passes back to the waiting loop via the terminate busy routine. If the command is a sense command, the assembled ready status is compared with the status received from the CPU. As long as these two are identical, the controller remains in a loop sampling and comparing the status. Once a change from the original is detected, an exit is made from this loop and control passes to the waiting loop via the terminate busy routine.

The portion of this routine that samples the ready status of all four units starting from unit 0 is used by the autoload and the off-line maintenance routine to determine which is the first unit in the daisy chain that is ready.

MICROINSTRUCTION DESCRIPTION

Most of the control logic within the controller is implemented by microinstructions contained within read-only memory (ROM). This design approach replaces the more conventional hard-wired random logic.

To understand the controllers logic, the reader must first understand how the microcontrol section operates and then how to follow the logical program flow as shown in the flow charts.

The following description describes the microinstructions and their implementation. The microprogram flow charts are provided in appendix A.

THE MICROINSTRUCTION REPERTOIRE

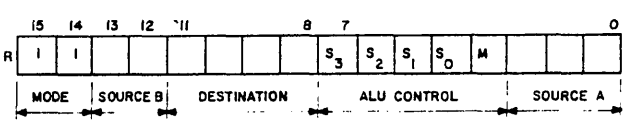
The microinstruction set is divided into four groups:

- Inter-register instructions
- Load constant instructions
- Control line and flip-flop instructions
- Jump instructions

The 16-bit microinstruction word is denoted R00 through R15, with R00 being the least significant bit. Figure 4-8 is a summary of the various microinstruction group formats.

INTER-REGISTER MICROINSTRUCTIONS

Inter-register microinstructions are identified by R14=1 and R15=1. These instructions cause data from a combination of two sources to be sent through the ALU to a destination register. Various logic and arithmetic operations, selected by the ALU control lines, are performed on the data as it passes through the ALU. The instruction format is shown below:



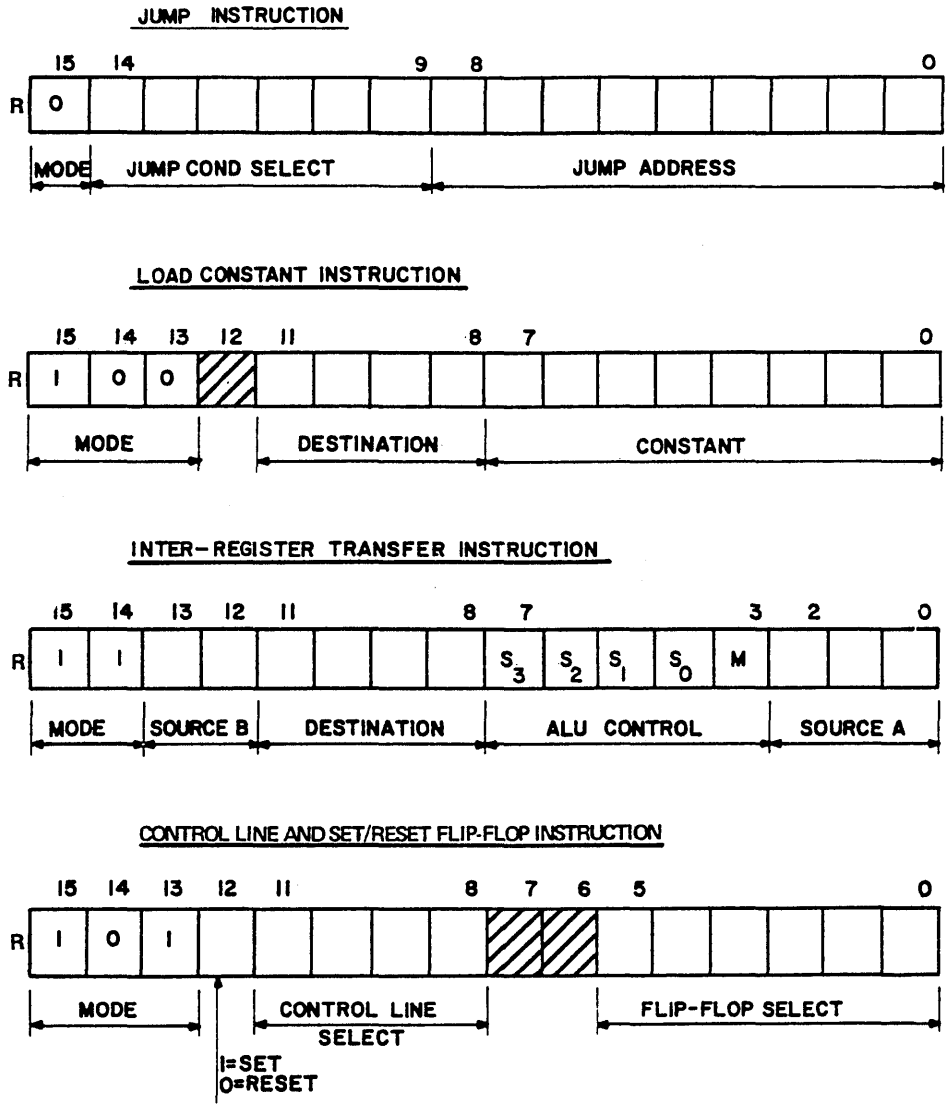


Figure 4-8. Microinstruction Groups

The source A field bits R00, R01, and R02 select one of eight available source A registers. Table 4-2 provides the source A codes.

TABLE 4-2. SOURCE A CODES

Sources = R15-R14			Source A
R02	R01	R00	
0	0	0	File (RAMS)
0	0	1	Word counter (WCS)
0	1	0	A-lines low (AINLS)
0	1	1	A-lines up (AINUS)
1	0	0	B-register (BREGS)
1	0	1	Q-lines (QS)
1	1	0	ROM (R0-R7)
1	1	1	Program counter (PCS)

The source B field, bits R13 and R12, select one of four available source B registers. Table 4-3 provides the source B codes.

TABLE 4-3. SOURCE B CODES

R13	R12	Source B
0	0	Current word address lower (CWALS)
0	1	Current word address upper (CWAUS)
1	0	Buffer 2 lower (BF2LS)
1	1	Buffer 2 upper (BF2US)

The destination field, bits R08 through R11, selects one of 12 destination registers. Table 4-4 provides the destination codes. The ALU control field, bits R03 through R07, activates five of the six ALU control lines. The remaining ALU control carry-in lines, are activated by a control flip-flop. Table 4-5 provides the ALU operation codes.

TABLE 4-4. DESTINATION REGISTER CODES

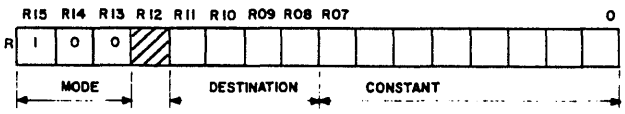
Destination	R11	R10	R09	R08	Destination
0	0	0	0	0	Not used
1	0	0	0	1	Not used
2	0	0	1	0	Not used
3	0	0	1	1	Not used
4	0	1	0	0	File address register (RAMADD)
5	0	1	0	1	Current word address upper upper (CWAUU)
6	0	1	1	0	File (RAMD)
7	0	1	1	1	Program counter (PCD)
8	1	0	0	0	Word counter (WCD)
9	1	0	0	1	A register upper (AOUTUD)
10	1	0	1	0	Current word address lower (CWALD)
11	1	0	1	1	Current word address upper (CWAUD)
12	1	1	0	0	A register lower (AOUTLD)
13	1	1	0	1	Buffer 2 lower (BF2LD)
14	1	1	1	0	Buffer 2 upper (BF2UD)
15	1	1	1	1	B register (BREGD)

TABLE 4-5. ALU CONTROL CODE INTER-REGISTER MICROINSTRUCTIONS

ALU Control				Logic	Arithmetic	
S3	S2	S1	S0	16=1	16 = 0, C = 1	16 = 0, C = 0
0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{A+B}$	A+B	(A+B) plus 1
0	0	1	0	$\overline{A}$•B	A+$\overline{B}$	(A+$\overline{B}$) plus 1
0	0	1	1	Logic 0	Minus 1 (2's comp)	Zero
0	1	0	0	$\overline{A•B}$	A plus A • $\overline{B}$	A plus A • $\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	(A+B) plus A • $\overline{B}$	(A+B) plus (A • $\overline{B}$) plus 1
0	1	1	0	A plus B	A minus B minus 1	A minus B
0	1	1	1	A•$\overline{B}$	A • $\overline{B}$ minus 1	A•$\overline{B}$
1	0	0	0	A+B	A plus A B	A plus A B plus 1
1	0	0	1	A plus B	A plus B	A plus B plus 1
1	0	1	0	B	(A+$\overline{B}$) plus A•B)	(A+$\overline{B}$) plus (A • B) plus 1
1	0	1	1	A•B	A • B minus 1	A•B
1	1	0	0	Logic 1	A plus A = 2xA	A plus A plus 1
1	1	0	1	A+$\overline{B}$	(A+B) plus A	(A+B) plus A plus 1
1	1	1	0	A+B	(A+$\overline{B}$) plus A	(A+$\overline{B}$) plus A plus 1
1	1	1	1	A	A minus 1	A

LOAD CONSTANT MICROINSTRUCTIONS

The load constant microinstruction, identified by R13=0, R14=0, and R15=1, loads an 8-bit character (constant) originating from the PROM into one of 12 destination registers. The instruction format is shown below:

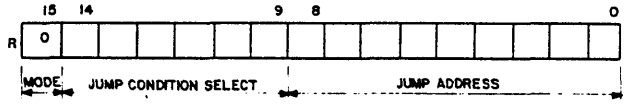


Bits R08 through R11 select the destination register. Table 4-4 provides the destination register codes.

Bits R00 through R07 designate the address in ROM that contains the constant to be transferred to the specified destination.

JUMP MICROINSTRUCTION

Jump-type microinstructions are identified by R15=0. The jump microinstruction format is shown below:



The jump condition select field consists of bits R09 through R14. There are 72 available jump conditions divided into 9 groups of 8. The jump condition group (JC GRP-9) enable flip-flop, which is set or reset by the flip-flop/control line instruction, selects the group. Bits R14 through R09 select the condition within the group. (For the group of eight, only R09 through R11 are valid). Table 4-6 shows the jump condition select codes and the corresponding jump conditions.

TABLE 4-6. JUMP CONDITION CODES

Jump Condition	R15	R14	R13	R12	R11	R10	R09	Magnetic Tape Transport
10	0	0	0	1	1	1	0	Autoload enable
11	0	0	0	1	1	0	0	Write add
12	0	0	0	1	0	1	0	
13	0	0	0	1	0	0	0	Check character flag
14	0	0	0	0	1	1	0	Program protect
15	0	0	0	0	1	0	0	ROM execute
16	0	0	0	0	0	1	0	Write strobe line
17	0	0	0	0	0	0	0	Hardwire high (unconditional jump)
20	0	1	0	1	1	1	1	Bus busy
21	0	1	0	1	1	0	1	CRC error
22	0	1	0	1	0	1	1	Load point
23	0	1	0	1	0	0	1	Read strobe latch
24	0	1	0	0	1	1	1	Autoload push-button
25	0	1	0	0	1	0	1	Write strobe latch
26	0	1	0	0	0	1	1	On/off-line switch
27	0	1	0	0	0	0	1	Read strobe line
30	0	0	1	1	1	1	1	DMA write complete
31	0	0	1	1	1	0	1	Half-word
32	0	0	1	1	0	1	1	Current word address bit 2-16
33	0	0	1	1	0	0	1	Buffer 1 full
34	0	0	1	0	1	1	1	Current word address bit 2-17
35	0	0	1	0	1	0	1	
36	0	0	1	0	0	1	1	First of data complemented
37	0	0	1	0	0	0	1	Read parity
40	0	0	0	1	1	1	1	ALU A=B
41	0	0	0	1	1	0	1	ALU carry out complemented
42	0	0	0	1	0	1	1	DMA protect fault
43	0	0	0	1	0	0	1	Hard error output
44	0	0	0	0	1	1	1	Buffer 2 full
45	0	0	0	0	1	0	1	DMA parity error
46	0	0	0	0	0	1	1	DMA address error
47	0	0	0	0	0	0	1	

TABLE 4-6. JUMP CONDITION CODES (Contd)

Jump Condition	R15	R14	R13	R12	R11	R10	R09	Magnetic Tape Transport
50	0	1	1	1	1	1	0	Mode operation 1
51	0	1	1	1	1	0	0	Formatter busy
52	0	1	1	1	0	1	0	Ready
53	0	1	1	1	0	0	0	On-line
54	0	1	1	0	1	1	0	File protect
55	0	1	1	0	1	0	0	Parity bit latch
56	0	1	1	0	0	1	0	Transfer error
57	0	1	1	0	0	0	0	File mark
60	0	1	0	1	1	1	0	
61	0	1	0	1	1	0	0	Disk error
62	0	1	0	1	0	1	0	Alarm
63	0	1	0	1	0	0	0	B-register bit 7
64	0	1	0	0	1	1	0	Index 2
65	0	1	0	0	1	0	0	Unit protected
66	0	1	0	0	0	1	0	
67	0	1	0	0	0	0	0	End of tape status
70	0	1	1	1	1	1	1	Identification burst
71	0	1	1	1	1	0	1	Mode operation 2
72	0	1	1	1	0	1	1	Speed option
73	0	1	1	1	0	0	1	7-track
74	0	1	1	0	1	1	1	Read mode
75	0	1	1	0	1	0	1	NRZI
76	0	1	1	0	0	1	1	Rewind status
77	0	1	1	0	0	0	1	Command reject
80	0	0	1	1	1	1	0	On-bus
81	0	0	1	1	1	0	0	Search file mark
82	0	0	1	1	0	1	0	Selected parity
83	0	0	1	1	0	0	0	
84	0	0	1	0	1	1	0	Selected
85	0	0	1	0	1	0	0	B-register bit 5
86	0	0	1	0	0	1	0	Check character flag
87	0	0	1	0	0	0	0	Corrected error status bit

TABLE 4-6. JUMP CONDITION CODES (Contd)

Jump Condition	R15	R14	R13	R12	R11	R10	R09	Magnetic Tape Transport
90†	0	0	0	1	1	1	0	End of tape
91	0	0	0	1	1	0	0	Corrected error
92	0	0	0	1	0	1	0	Maintenance switch 2
93	0	0	0	1	0	0	0	Maintenance switch 3
94	0	0	0	0	1	1	0	Unit single density
95	0	0	0	0	1	0	0	Maintenance switch 1
96	0	0	0	0	0	1	0	
97	0	0	0	0	0	0	0	Auxiliary

†Jump condition group 9 - ENB flip-flop must be set.

There are two types of jump instructions:

- Unconditional Jump - This type is identified by the fact that R14 through R09 equal zero. The program counter, bits 0 through 8, is loaded with R00 through R08. Program counter bit 9 is loaded with the contents of the ROM bank select (RMBNKS) flip-flop.
- Conditional Jump - If the selected condition is true, the program counter is loaded with R00 through R08 and the bank select (RMBNKS) flip-flop. If the selected condition is false, the program counter is incremented by one.

JUMPING TO SUBROUTINES

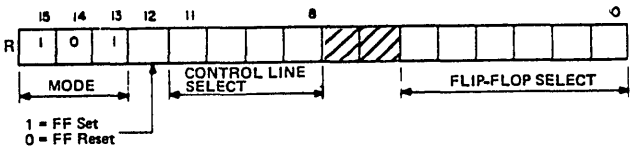
Jumping to subroutines is a two-step process. First the return address must be saved, and then a jump (conditional or unconditional) must be made to the starting address of the subroutine. (The RMBNKS flip-flop must be set according to the bank in which the subroutine is located prior to the jump.) Figure 4-9 shows the instruction sequence necessary for jumping to and returning from subroutines. P incremented by one (P+1) is loaded into the register file at address 0 via an inter-register instruction. Address 0 is provided to the file address register (RAMADD) by the hardware. Execution of this instruction also causes the upper two bits of the PC to be saved in flip-flops. Next, a jump is executed to the starting address of the subroutine. To return from the subroutine, zero is loaded into the file address register (RAMADD) via a load constant instruction. The contents of RAM 0 is incremented by one and loaded into the PC. This causes a jump to the return address (P+2). The upper two bits that were saved in flip-flops are loaded into the upper bit positions by hardware.

R08 through R00 specifies the jump address. The 1K ROM is divided into two banks of 512 words each (locations 0 through 511 are called the lower bank, locations 512 through 1023 are called the upper bank). R00 through R08 specifies the address within a bank. The ROM bank select (RMBNKS) flip-flop, which is set or reset by the flip-flop/control line instruction, selects the bank to which the jump will be made.

The jump instruction that causes the jump to the starting address of the subroutine cannot be located in ROM addresses 255, 256, 511, 512, 767, 768, 1023, or 1024 due to the structure of the PC.

CONTROL LINE AND SET/RESET FLIP-FLOP INSTRUCTIONS

These instructions, identified by R13=1, R14=0 and R15=1, are used for setting or resetting up to 64 control flip-flops and for providing a pulse on one of 16 available control lines. Both of these operations can be performed in the same microinstruction. The instruction format is shown below:



The flip-flop select field, R00 through R05, selects one of 56 available flip-flops. Table 4-7 provides the flip-flop codes. If bit R12 is clear, the selected flip-flop is reset. If it is set, the selected flip-flop is set.

The control line select field selects one of 16 available control lines to be strobed. Table 4-8 provides the control line codes. Table 4-9 provides tabulation of file register usage.

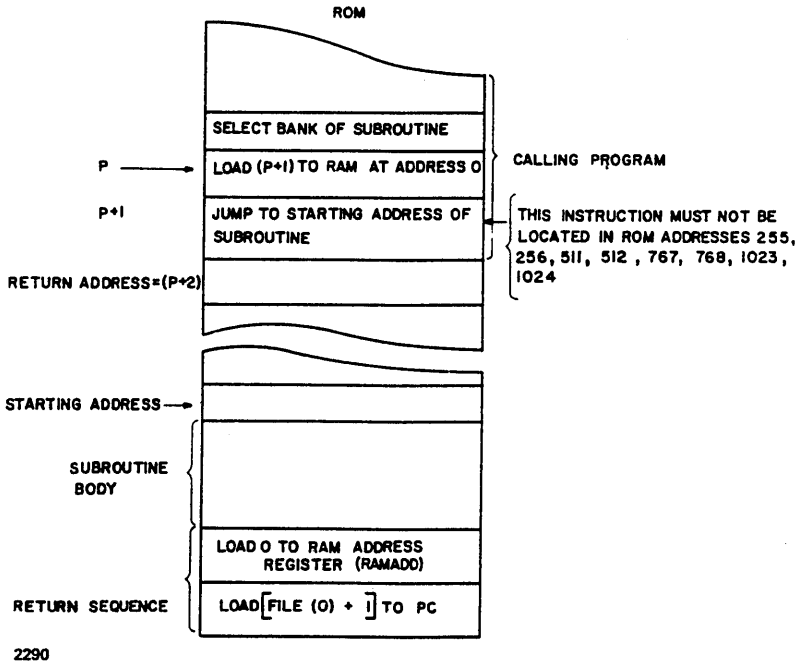


Figure 4-9. Subroutine Jump Instruction Sequence

TABLE 4-7. FLIP-FLOP CODES

FDD Group		R05	R04	R03	R02	R01	R00	Magnetic Tape Transport
1	0	1	1	0	1	1	1	Low threshold
	1	1	1	0	1	1	0	Write file mark
	2	1	1	0	1	0	1	Rewind
	3	1	1	0	1	0	0	Check character flag
	4	1	1	0	0	1	1	ROM bank select
	5	1	1	0	0	1	0	Search file mark flag
	6	1	1	0	0	0	1	Spacing mode
	7	1	1	0	0	0	0	Corrected error status
2	0	0	1	0	1	1	1	Select buffer 1
	1	0	1	0	1	1	0	Off-line
	2	0	1	0	1	0	1	Last word data
	3	0	1	0	1	0	0	Go
	4	0	1	0	0	1	1	Write
	5	0	1	0	0	1	0	Formatter enable
	6	0	1	0	0	0	1	Acknowledge
	7	0	1	0	0	0	0	Selecter buffer 2
3	0	0	1	1	1	1	1	Write/read processor
	1	0	1	1	1	1	0	Buffer 1 enable
	2	0	1	1	1	0	1	Enable double buffer
	3	0	1	1	1	0	0	Write parity
	4	0	1	1	0	1	1	Enable word sync
	5	0	1	1	0	1	0	Compare 1
	6	0	1	1	0	0	1	Read/write mode
	7	0	1	1	0	0	0	Parity mode

TABLE 4-7. FLIP-FLOP CODES (Contd)

FDD Group		R05	R04	R03	R02	R01	R00	Magnetic Tape Transport
4	0	1	0	1	1	1	1	Alarm
	1	1	0	1	1	1	0	Busy
	2	1	0	1	1	0	1	Select B register
	3	1	0	1	1	0	0	DMA write protect
	4	1	0	1	0	1	1	Hard error load mode
	5	1	0	1	0	1	0	
	6	1	0	1	0	0	1	Jump condition group 9 enabled
	7	1	0	1	0	0	0	Interrupt response
5	0	0	0	1	1	1	1	
	1	0	0	1	1	1	0	Erase
	2	0	0	1	1	0	1	Reverse
	3	0	0	1	1	0	0	Autoload enable protect system
	4	0	0	1	0	1	1	
	5	0	0	1	0	1	0	Off-line maintenance
	6	0	0	1	0	0	1	Write add
	7	0	0	1	0	0	0	
6	0	1	0	0	1	1	1	Auxiliary
	1	1	0	0	1	1	0	Transport address 1
	2	1	0	0	1	0	1	Density select
	3	1	0	0	1	0	0	Parity select
	4	1	0	0	0	1	1	On-bus
	5	1	0	0	0	1	0	
	6	1	0	0	0	0	1	Transport address 0
	7	1	0	0	0	0	0	ALU carry in
7	0	0	0	0	1	1	1	Parity
	1	0	0	0	1	1	0	Index 2
	2	0	0	0	1	0	1	Selected
	3	0	0	0	1	0	0	File mark status
	4	0	0	0	0	1	1	End of operation
	5	0	0	0	0	1	0	End of tape status
	6	0	0	0	0	0	1	
	7	0	0	0	0	0	0	Controller protected

TABLE 4-8. CONTROL LINE CODES

Control Line	R11	R10	R09	R08	Magnetic Tape Transport Controller
0	0	0	0	0	Not used
1	0	0	0	1	Set reject (REJ)
2	0	0	1	0	Set DMA request (DMAREQ)
3	0	0	1	1	Set reply (RPLY)
4	0	1	0	0	Clear data strobe(CLDSTR)
5	0	1	0	1	Clear DMA request (CREQ)
6	0	1	1	0	Set read strobe latch (SRSTR)
7	0	1	1	1	Reset MTT status latch (CLSTAT)
8	1	0	0	0	Set buffer 1 full (SBF1F)

TABLE 4-8. CONTROL LINE CODES (Contd)

Control Line	R11	R10	R09	R08	Magnetic Tape Transport Controller
9	1	0	0	1	Set buffer 2 full (SBF2F)
10	1	0	1	0	Clear hard error latch (CLHER)
11	1	0	1	1	Shift hard error latch (SFTHER)
12	1	1	0	0	Clear first of data (CFSTDT)
13	1	1	0	1	Clear DMA error (CDMAER)
14	1	1	1	0	Set write strobe latch (SWSTR)
15	1	1	1		Not used

TABLE 4-9. FILE REGISTER USAGE

File Register	RAM Address Register				Magnetic Tape Transport Controller
0	0	0	0	0	Return address†
1	0	0	0	1	Assembly/disassembly†
2	0	0	1	0	N/A
3	0	0	1	1	N/A
4	0	1	0	0	Interrupt storage†
5	0	1	0	1	N/A
6	0	1	1	0	Transport status lower
7	0	1	1	1	Transport status upper
8	1	0	0	0	Block length lower
9	1	0	0	1	Block length upper
10	1	0	1	0	Alarm status lower
11	1	0	1	1	Alarm status upper
12	1	1	0	0	LRC character
13	1	1	0	1	CRC character
14	1	1	1	0	Ready status
15	1	1	1	1	N/A

† Used for internal firmware operations only.

DIAGRAMS 5

This section contains the detailed circuit description of the magnetic tape transport controller logic diagrams included at the end of this section. The logic diagrams specifically reflect the FA465-A MTTC. However, they are applicable to all FA464 and FA465 MTTCs.

A/Q INTERFACE

INPUT/OUTPUT OPERATIONS

The necessary conditions for an A/Q input or output operation are as follows:

- The equipment code must match the equipment number.
- The W=0 field signal (WE0) must be true.
- The required read or write signal must be active (low).

Equipment Identification

The equipment number is determined by four jumper plugs individually inserted into (or removed from) socket terminals marked Q7, Q8, Q9, and Q10 at location S8B. Inserting a jumper plug into the Q7 terminal, for example, selects a zero for that bit. Removing a jumper plug from the Q8 terminal selects a one for that bit, and so on. The four hexadecimal bits of the equipment code are received from the computer on the ADR08/, ADR09/, ADR10/, and ADR11/ lines at pins 281, 282, 283, and 284, respectively. These four signals are compared with the equipment code jumper settings.

The equipment code bits from the computer are compared to the equipment number jumper plug settings by a 4-bit magnitude comparator at S9. If the compared bits match and the WE0/ signal is low (that is, A=B in is high), the A=B out comparator output (S9-6) goes high. The high output obtained at S9-6 is the first condition necessary for the activation of the A/Q interface sequencer (high level at U4-1).

W Field

The signal WE0/ must be low for read or write operations. If the W field = 0 condition exists, then WE0/ at pin 292 is low. This signal is received and inverted to a high level by a Schmitt-trigger inverter at T9-11/10; T9-10 is connected to the A=B in comparator input (S9-3).

READ Signal

The third condition for a read operation is an active (low) read signal from the computer at pin 248 (READ SSTB/). If read is active, then read at H9-13 is low, and the inverter output (READ BUF) is high at H9-12. The READ BUF signal is connected to the reply flip-flop (T4-12), a 2-input positive OR gate (T5-9), the A-bus selector (F8-6), and a 3-input positive NAND gate (B3-5).

When READ BUF is high, the output of the OR gate at T5-8 is high. This provides the second enable to the 3-input positive AND gate at U4-2.

WRITE Signal

The third condition for a write operation is an active (low) WRITE/ signal from the computer at pin 290. If the write signal is active, T9-3 is low and the output of this inverter at T9-4 is high. This output (T9-4) is connected to an OR gate (T5-10), a 3-input positive AND gate (U4-10), and a 2-input positive NAND gate at R2-9.

For a write operation, the output of the OR gate at T5-8 goes high and gives the second enable to U4-2.

Sequencer Enable

If the on/off-line switch (location L1) is in the on position, the sequencer at location U3 is able to initiate a sequence of pulses. The enable is effected by the release of the clear input at U3-1.

The hardware uses a digital filter formed by two hex D flip-flops at location U6. When U4-12 goes high, the OR gate output (T5-11) also goes high. U4-12 is connected to U6-4; U6-5 goes high after 0 to 50 nanoseconds (the clock of U6 is 20 MHz). U6-5 is connected to U6-14; U6-15 goes high after an additional 50 nanoseconds. The result is that the signal at T5-13 goes high 50 to 100 nanoseconds after the leading edge of U4-12.

Power-On Reset

This circuit generates a reset pulse at power-on. C32 is charged through R30; at this time inputs T7-2 and U6-1 are low.

NOTE

UM1, UM2, UM3, and UM4 are external connection points.

Diode D1 is used to discharge the capacitor at power-off. The master reset signal (MR/) from pin 46 is received at Schmitt-trigger inverter G9-13. Flip-flops U6-3/2 and U6-13/12 form a digital filter. When G9-12 is high, U6-3 and T6-5 are also high. U6-2 goes high after approximately 50 nanoseconds, raising U6-13 to a high level. U6-12 goes high after an additional 50 nanoseconds. If the MR/ signal at G9-13 is still active after the 100-nanosecond delay, T6-6 goes low, driving T7-3 low, which in turn generates a low level at T7-6. The GR/ signal from T7-6 drives U1-3 high, generating the master reset pulse (CCMR).

CLOCK CIRCUIT

The controller incorporates a 20-MHz crystal-controlled oscillator. The oscillator is built from transistors Q1 and Q2; gates T7-9, 10/8, T6-13, 12/11, and T6-9, 10/8; crystal Y1; capacitors; and resistors.

Phase Generator

The clock input at U6-9 is 20 MHz. Flip-flop U6-6/7 and NAND gate T6-1, 2/3 form the 20-MHz divider. The output is a 10-MHz clock that is connected to U5, a hex-D type flip-flop. The path from U5-5 through U5-6/7 and T3-13/12 to U5-4 forms the first part of a phase generator. G2 is a decoder/demultiplexer. Inputs 1A (G2-2) and 1B (G2-3) are connected to U5-5 and U5-7. G2-4, 5, 7, and 6 are phase-generator outputs ϕ0/, ϕ1/, ϕ2/, and ϕ3/ respectively. Figure 5-1 illustrates the phase pulses.

Sequencer

Flip-flop U3 is the sequencer used for A/Q commands. The sequencer is clocked at 10 MHz. When the controller receives an A/Q command in the on-line state, sequencer input U3-1 (clear) goes high. The leading edge of the first 10-MHz clock pulse (U3-9) initiates the sequencer operation. Figure 5-2 illustrates the sequencer pulses.

When an immediate reject condition exists, the controller generates the reject signal at S0 (U3-10) and the sequencer stops. A low level at AND gate U2-10 determines low at the U3-14 data input.

If an immediate reject condition does not exist, S0 causes the generation of S1 (U3-15).

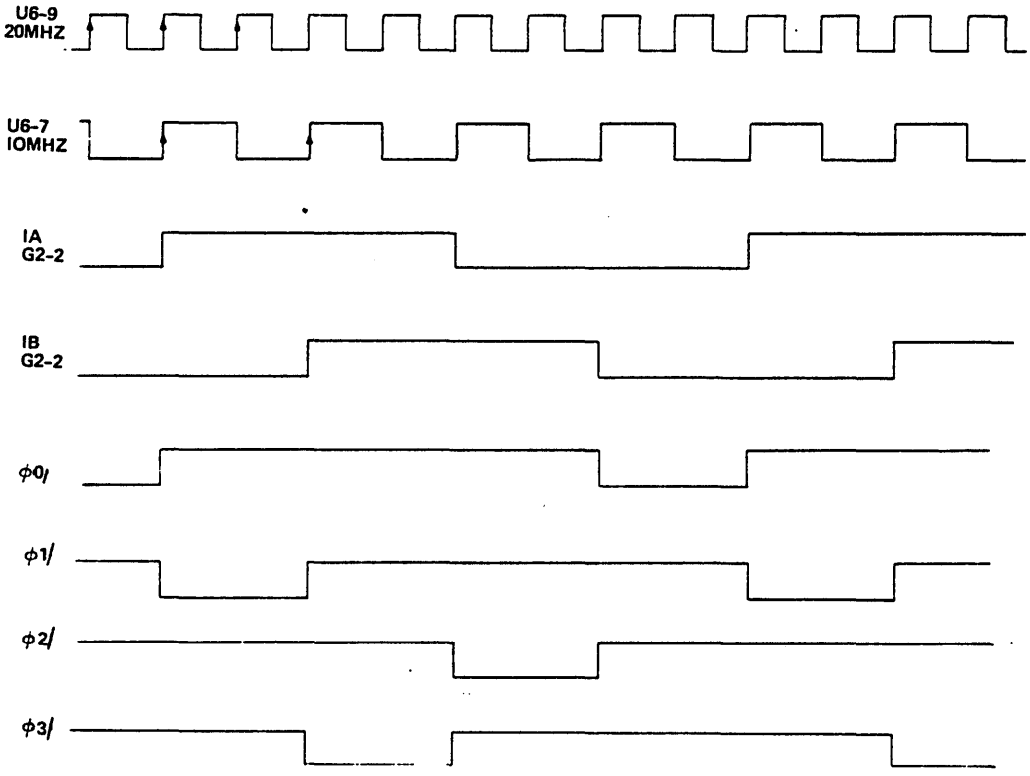
Pulse S2 is generated when the A/Q command is a clear controller or a read dynamic status command. For clear controller or dynamic status commands, ADR05/ is low (making Q04 equal to 1), AND gate input U2-13 is high, and data input U3-13 (S1 • Q4) is high.

If S1 • Q4 is high, the sequencer generates pulses S2 and S3. The leading edge of pulse S3 generates the reply pulse. The ending of the A/Q command determines the reset of all S pulses.

REJECT CIRCUIT

A/Q commands with Q04 = 0 (ADR05 high) cause a reject condition if the controller is in the busy state. In this case, flip-flop BUSY (G1-5) is high, U2-5 is high, U2-4 is high, and AND gate output U2-6 is high. Flip-flop U6-11/10 and AND gate U2-1, 2/3 form a digital filter for the Q4 line.

Another condition for reject is protect violation. If flip-flop CNTPRT (B1-12) is high, the controller is protected. An unprotected A/Q write command causes a protect violation (U4-8 is high). Flip-flop T4-2, 3/5 is the reject flip-flop. A reject condition (T4-2 high) causes the generation of the reject pulse at the leading edge of S0.



NOTE : PHASE PULSES ϕ0/, ϕ1/, ϕ2/, AND ϕ3/ HAVE A PULSE WIDTH OF 100 NSEC EACH.

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Figure 5-1. Phase Pulses

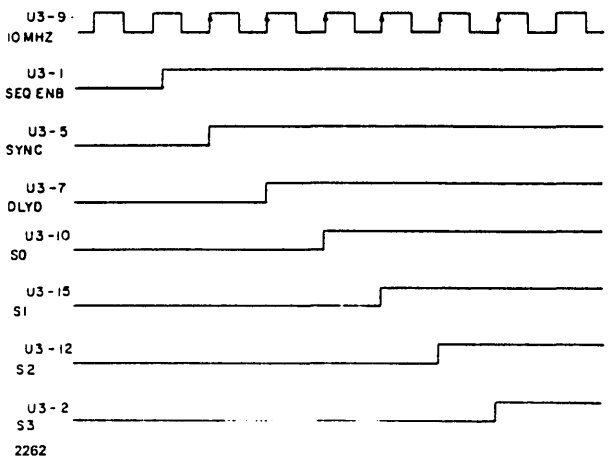


Figure 5-2. Sequencer Pulses

If the A/Q command requires microprogram intervention, the program determines if and when the controller will send a reject pulse to the CPU. In this case, control line SET REJECT/ sets the reject flip-flop (active low signal at T4-4). The reject pulse is transmitted to the CPU via driver B9-13, 12/11 to pin 220.

REPLY CIRCUIT

Flip-flop T4-12, 11/9 is the reply flip-flop. For A/Q commands with Q04=1, the reply condition (T4-12 high) causes generation of the reply pulse at the leading edge of S3.

If the A/Q command requires microprogram intervention, the program decides if and when the controller will generate a reply pulse. In this case, control line RPLY/ sets the reply flip-flop (active low signal at T4-10).

The reply pulse is transmitted through driver B9-9, 10/8 to pin 216. The reply and reject circuits are enabled only at the time of an A/Q command (T4-13 and T4-1 are both high).

MICROPROGRAM EXECUTE CIRCUIT

All A/Q commands with Q04=0 require microprogram intervention. Flip-flop T2-12, 11/9 is the microprogram execute flip-flop. The leading edge of S1 sets the flip-flop when T2-12 is high (Q04=0). The clear controller A/Q command (Q04=1) sets the RMEXEC flip-flop by an active low pulse at T2-10. REJ/, RPLY/, or GR/ pulses reset the RMEXEC flip-flop (T2-13 is low through action of AND gate U4-3, 4, 5/6). RMEXEC is connected as a jump condition (T1-14).

CONTROLLER RESET

The controller is reset by a GR/ pulse (T7-6) or by a clear controller A/Q command (Q04=1). The clear controller generates an active low pulse at NAND gate R2-8. This pulse, like the GR/ pulse, generates a CCMR1 active high pulse at U1-3 driver output and CCMR2/ and CCMR3/ active low pulses at J2-10 and J2-12 outputs. A clear controller or GR/ pulse clears the program counter and activates the program from the first PROM address (0000_{16}).

A-OUTPUT REGISTER

The multiplexers with latched outputs at F4, E3, E4, and F3 form the A-output register. F4 and E3 store the eight least significant bits, and E4 and F3 store the most significant bits of the controller A-channel outputs. The ALU output bus is multiplexed with the dynamic status flip-flops at the input to the A-out register.

When a dynamic status request is received by the controller, Q04 is high and the read signal is active; S1•Q4 is high; and the multiplexers select the dynamic status bits (F4-10, E3-10, E4-10, and F3-10 are high) as the input to the A-out register.

The exclusive OR gate (R4-1, 2/3) generates the SPLS pulse. This pulse is transmitted through the E2-9, 10/8 and E2-12, 13/11 NAND gates to clock the outputs of the dynamic status flip-flops into the A-out register on the trailing edge of the SPLS pulse. AOUTUD/ (K2-14) and AOUTLD/ (K2-11) are the clocks to select the ALU output bus data.

A-Out Register Buffer

The A-out register outputs are driven by inverting three-state buffers at locations E5, F5, and B4. The buffers are enabled by the active low output of the NAND gate at B3-6, which places the A-out register contents on the A-channel during A/Q read commands.

A-Bus Selector

The 8-bit A-bus selector (F9, D9, F8, D8, D5, and C5) selects the A input to the ALU during the execution of an inter-register microinstruction.

The selector is composed of an 8-to-48-line multiplexer with three-state outputs, an 8-bit three-state buffer for the word counter (WC) register, and the three-state outputs of the file RAMs. The A-bus selector is controlled by the A-bus source decoder.

The following is a list of the inputs to the A-bus selector:

- CPU A-channel inputs, lower, SD01/ through SD08/
- CPU A-channel inputs, upper, SD09/ through SD16/
- CPU Q-channel inputs ADR01/ through ADR04/, ADR06/, and READ BUF signal
- ROM outputs PR0 through PR7
- Program counter bits PA0 through PA7
- B-register outputs 2^0 through 2^4, 2^6, BMD7, and BMSB
- WC register outputs
- RAM outputs

A-Bus Source Decoder

The A-bus source decoder consists of a selector at location A4 and a decoder/demultiplexer at location B8. When a jump microinstruction is executed, PR15 is low. This selects the one inputs of the selector at A4, causing IR from A4-9 to go low and selecting PR0 through PR7 as the outputs of the multiplexers at locations D5 and C5. The output of AND gate F2-6 is also driven low by the IR signal. This enables the outputs of multiplexers D5 and C5 by placing a low signal in C5-15 and D5-15. Concurrently, the IR signal drives the inverter output at B2-12 high, disabling the outputs of the decoder (B8). Decoder output B8-11 goes high and disable the outputs of the WC register buffers (C7-1, C7-15, and C6-15 are high). With B2-12 high, buffer outputs C6-9, 5, 3, and 7 are disabled and are also high. The function select pins of the ALU (FG7-6, 5, 4, and 3 and FG6-6, 5, 4, and 3) are high. ALU mode input 16 (FG7-8 and FG6-8) is driven high by NAND gate output B3-8. With the function select and mode inputs to the ALU high, the ALU passes the A-bus data (PR0 through PR7) to ALU outputs FG7-9, 10, 11, and 13 and FG6-9, 10, 11, and 13.

For an inter-register microinstruction, B2-12 is low. The B8 decoder is enabled and PR0, PR1, and PR2 provide the data for the decoder select inputs (B8-2, 3, and 14). When the selected source is the RAM, B8-12, A6-8, and A7-8 are low. When the word counter is the selected source, B8-11 is low, and in turn C7-1, C7-15, and C6-15 are low.

PROGRAM COUNTER

Three synchronous 4-bit counters (D7, D6, and B5) provide a 10-bit address for the 1024-word PROM. This program counter (PC) receives its lower eight bits from the ALU-out bus. The two most significant bits are loaded either from a 2-bit return address register, which is used for returning from subroutines, or from PR8 and the output of the ROM bank select flip-flop (RMBNKS). The multiplexer at A4 selectes the input to the two most significant bits of the PC.

During a jump to subroutine operation, the lower eight bits of the PC are saved in address 0 of the register file (RAM) and the upper two bits of the PC are saved in the 2-bit return address register at A3.

During subroutine returns, the upper two bits of the PC are loaded from the two flip-flops at A3 by the A4 selector. The lower eight bits are loaded from RAM through the ALU.

Receipt of a low signal on the load PC line (D7-9, D6-9, and B5-9) causes the PC to be loaded on the trailing edge of $\phi 0/$. The PC outputs are connected to the PROM address input and to the A-bus selector.

PROM

The PROM is organized as an array of 512 words by 8 bits. Four PROMs are used to construct a micromemory of 1024 words by 16 bits.

The nine address bits of the PROM are provided by the nine lower program counter bits. The tenth bit of the PC selects between the lower 512-word bank (CD1, CD3) and the upper 512-word bank (CD2, CD4). When B5-13 is low, the lower bank is selected (CD1-20, 21 and CD3-20, 21 are low); when B5-13 is high, the upper bank is selected (CD2-18, 19 and CD4-18, 19 are high). The 16-bit, three-state outputs of the upper and lower PROM banks are wire-ORed together.

PROM bits PR0 through PR7 provide an A-source for the A-bus selector. PROM bits are also connected to various circuits to generate and control microprogram execution.

B REGISTER

The B register (locations E6 and E7) is a general-purpose 8-bit register on the A side of the controller. ALU-out bus data is multiplexed at the input to the B register with receivers of input pins 29, 28, 37, 30, 33, 38, 31, and 34. These pins are used to receive the R0 through R7 read data from the formatter.

Flip-flop G1-6 (SELBREG) selects the input to the B register. The trailing edge of the BREGD/ pulse (from K2-6) strobes the selected data into the register. The B register outputs are connected to the A-bus selector. B-register bits 2^5 (BMDL) and 2^7 (BMSB) are connected to jump conditions at E1-14 and F1-1, respectively.

WORD COUNTER REGISTER

Two synchronous, 4-bit up-down counters at B6 and B7 constitute the word counter (WC) register. This circuit is used as a general-purpose register. The WCD/ pulse loads the WC register.

The WC register outputs are connected as an A-side source through three-state buffers at C7 and C6. In addition, the LWC register outputs are connected via drivers at A8A, C8B, C9B, C8A, and C9A to pins 7, 18, 12, 14, 15, 19, 13, 17, and 11. This allows the WC to be used as data to the formatter register. The drivers are enabled and the write data (W7 through W0) is placed on the lines only when the on-bus flip-flop (ONBUSFF), which controls the ONBUSSTAT signal from J2-2, is set.

FILE ADDRESS REGISTER

Two 16-by-4 clocked RAMs with three-state latched outputs (at A6 and A7) constitute the file of the controller.

The address of the file is selected by a 4-bit file address register. The data to be written into the file is received from the ALU-out bus. The RAM three-state outputs are connected as a source to the ALU A-input.

An active low RAMD/ pulse from L2-9 acts as a write pulse at A6-2 and A7-2 during the time that A6-7 and A7-7 are held low. Figure 5-3 illustrates the operation mode of the file.

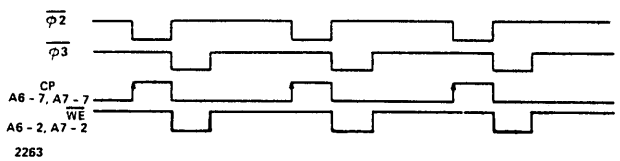


Figure 5-3. Timing for Operation Mode of File

The transition of the clock pulse (CP) from low to high causes the contents of the file location selected by address inputs A0 through A3 to be strobed into the RAM output register. A three-state output enable (EO) controls the RAM output buffers. When EO (A6-8, A7-8) input is low, the outputs are determined by the data in the output register.

The quad-D type flip-flops at A5 are used as the file address register. This register is loaded from the ALU-out bus with the address of the file register. The loading is executed on the trailing edge of a RAMADD/ (L2-11) active low pulse.

ARITHMETIC LOGIC UNIT

The heart of the MTTC consists of an 8-bit ALU (FG7 and FG6). The ALU is fed on the A side by the A-bus selector, which selects one of eight source A inputs. On the B side of the ALU, the B-bus selector selects one of four source B inputs. The ALU output bus is routed to one of 12 destination registers and to a parity generator/checker. The ALU performs 16 binary arithmetic operations that are selected by four function-select lines (1, 2, 4, and 8). The function select lines are received from the PROM through buffers (C6). These buffers are enabled during the execution of an inter-register instruction. In this case, the data selector multiplexer (A4) generates an IR signal: PR15 (A4-1) is high, PR14 (A4-10) is high, and IR (A4-9) is high. The IR signal is inverted by B2-13/12 and provides an enable for C6-1.

The internal carry (FG7-7) is provided by flip-flop CNALU (A1-12). PR3 is gated by the IR signal (B3-9) and inverted by B3-8. The output of NAND gate B3-8 supplies the input for the ALU (FG7-8, FG6-8).

The inverted carry output of the first ALU (FG7-16) is provided as a carry input to the second ALU (FG6-7).

Parity Generator/Checker

The controller includes a parity generator/checker (R5) that is provided with eight ALU-out bus bits. The ninth input (R5-4) is the parity mode flip (PARMD). This flip-flop is used to select even or odd parity mode.

The parity bit (R5-5) is sent to the formatter during write operations or is compared to the parity bit received from the formatter during read operations.

Carry Out A B and Parity Latch

A 4-bit register at G5 is used as a latch for the ALU carry output (G5-2/4), for the ALU comparator output A=B (G5-1/6), and for parity bit/error output (G5-13/8). During the execution of an inter-register microinstruction, the IR signal is high. This causes the latch load input (G5-9) to be high. Data is strobed into the latch with the leading edge of clock phase ϕ0/. The latch data remains valid until a new inter-register instruction is executed.

NOTE

The A=B ALU open collector outputs (FG7-14 and FG6-14) are wire-ORed together to give comparison for eight bits. A pull-up resistor S3 is used for the wire OR connection.

B-BUS SELECTOR

The dual 4-to-1-line data selectors/multiplexers at J9, J8, J7, and J6 constitute the B-bus selector. The B sources are the current word address register (CWAOUT) and buffer 2 register (BUF2OUT). PROM bits PR12B and PR13 select the B-side source during the execution of inter-register microinstructions.

The B-bus selector outputs are connected to the ALU B-inputs.

CURRENT WORD ADDRESS REGISTER

The synchronous 4-bit up-down counters K9, K8, K7, K6, and L6 constitute the current word address (CWA) register. This register is divided into three subregisters: CWAL (K9, K8), CWAU (K7, K6), and bank (L6). The inputs of each subregister are connected to the ALU-out bus. The CWAL and CWAU outputs provide the inputs for the B-side selector. The 2-bit bank outputs (L6-3 and L6-2) are connected as jump conditions to M1-2 and M1-15, respectively.

The CWA register is used as an 18-bit address register during DMA data transfers. This register provides the 16 bits of memory address and two bits of memory bank address through buffer gates to the DMA address pins. The 16 address bits and the least significant bit of bank address are enabled by a signal that is the result of a logical AND between the REQ ACC/ (G4-13, J3-12) pulse and the state of the jumper mode (inserted or removed).

When the controller executes a DMA transfer cycle, the DMAX-RA/ (G4-1) active low pulse generates an ENABLE ADD/ that enables the three-state buffer inverters L7, L8, and L9. Address bits DMA-MAB01/ through DMA-MAB17/ are connected at pins 53 through 62, 253 through 258, and pin 35.

NOTE

In the MTTC, the jumper mode state is always high (the jumper is removed). The memory bank address most significant bit is provided by L6-2 through buffer gate N9-14/13 to pin 36 (DMA-MAB18). The ENB DMA MR/ active low signal enables this memory bit during the DMA transfer cycle.

All of the memory address bits are active low signals.

The CWA subregisters are loaded from the ALU output bus. CWAL is loaded when an active low CWALD/ pulse from K2-13 is provided to K9-11 and K8-11. CWAU is loaded when an active low CWAUD/ pulse from K2-12 is provided to K7-11 and K6-11.

The bank is loaded when an active low BANKD/ pulse from L2-10 is provided to L6-11. The CWA registers are loaded asynchronously, independent of the register clock.

The clock for the CWA register/counter is the REQ ACC/ pulse with incrementation of the CWA registers taking place on the trailing edge of the pulse. Each time a DMA cycle is completed, the counter is clocked and the address for the next DMA transfer cycle is prepared. At the start of the DMA transfer operation, the CWA register is loaded with the first word address from the ALU output bus.

DMA BUFFER

Buffer 1 Register

The buffer 1 register is composed of four 4-bit registers with multiplexed inputs at M8, N8, P8, and R8. The 16 memory data bits, DFM01 to DFM16, from pins 264 to 279, are multiplexed at the input of the buffer 1 register with 16-bit parallel data from the shift register at M6, N6, P6, and R6. Flip-flop group 2 (S5-4) selects the input to buffer 1. Data is strobed into the register on the trailing edge of the CLKBUF1 pulse. The outputs of buffer 1 are connected to the inputs of buffer 2.

Buffer 2 Register

The buffer 2 register is composed of four 4-bit registers with multiplexed inputs at M7, N7, P7, and R7. The register is divided into two 8-bit subregisters called buffer 2 low (bits 1 through 8) and buffer 2 up (bits 9 through 16). Bits 9 through 16 of the buffer 1 register are multiplexed with the ALU-output bus at the input to buffer 2 low. Flip-flop S5-12 (SELBF2) selects the input to buffer 2 low and buffer 2 up. The loading of buffer 2 is controlled by the DMA buffer control.

The outputs of the buffer 2 register are connected as sources (buffer 2 low, M7 and N7, and buffer 2 up, P7 and R7) to the B-bus selector. In addition, the buffer 2 register is connected through buffer gates to the DMA data-to-memory pins (DMA-DTM01/ through DMA-DTM16/). The three-state bus drivers at R9, P9, and N9 transfer and invert the buffer 2 register data. These buffer gates are enabled by active low pulse STB-DTM/ from the DMA signal generator. The outputs of the buffer gates, DMA-DTM01/ through DMA-DTM16/, are connected to pins 64 through 79. The DMA buffer control circuit provides separate clocks for the buffer 2 subregisters. The clock for buffer 2 up is provided through K5-13, 12/11, and the clock for buffer 2 low is provided through K5-10, 9/8.

DMA Buffer Control

The buffer 1 full signal is generated by the J-K negative-edge-triggered flip-flop at location L4. The flip-flop is clocked by the CLKBUF1/ signal. The CLKBUF1/ signal is generated whenever a DFM (data from memory) strobe is received from DMA control. The program must set the BF1ENB (N1-5) flip-flop to allow the J input (L4-9) of the buffer 1 full flip-flop to be high.

The enable for DMA buffer activity is provided by the ENBDB flip-flop (N1-6). When ENBDB and K4-10 are high, L4-8, L4-3, J4-8, and J4-3 are high, allowing the flip-flops to be set.

The output of the buffer 1 full flip-flop (L4-11) is connected to the BF1F jump condition (M1-1) and to the J input of the buffer 1 lost data flip-flop (L4-4). If CLKBUF1/ is provided when the buffer 1 full flip-flop is set (buffer 1 register is full), flip-flop buffer 1 lost data is set. The buffer 1 lost data flip-flop output sets M3-4, which provides the LSTDT jump condition at M1-4. This condition informs the microprogram of the completion of a DMA write cycle.

The J-K negative-edge-triggered flip-flop (J4-9, 12, 6/11) comprises the buffer 2 full flip-flop. J4-4, 16, 1/14 comprises the buffer 2 lost data flip-flop.

Automatic control of the double buffer is based on the clock request generator. When the buffer 1 and buffer 2 registers are empty, L5-1 is high and L5-2 is low. The result is that L5-3 is low. Two flip-flops, K4-13/12 and K4-11/10, are cascaded (K4-12 to K4-11). These flip-flops are clocked by the 10-MHz clock. The clock request produces a 200-nanosecond low pulse, which resets the buffer 1 full and sets the buffer 2 full J-K flip-flops.

DMA Transfer Control

DMA data transfer is controlled by a circuit that provides the DMA memory request signal (DMA-MR/), receives the DMA request accept signal (DMAX-RA/), and commands the direction and timing of the data and function transfer (protect, error).

Write to Memory

The data is received from the formatter by the B register. The first character is loaded into the buffer 2 up register and the second character is loaded into the buffer 2 low register. The buffer 2 register sends the data to memory.

When the controller executes a write to memory cycle, the microprogram initially resets flip-flops COMP1 (N1-10), SELBF2 (S5-12), and WTRDMP (N1-4).

The microprogram resets flip-flop ENBDB (N1-6). When the controller sets the DMA request, flip-flop ENBDB is set. Control line DMAREQ/ (S2-13) sets request flip-flop T2-4, 1/5, 6. T2-6 goes low and drivers N9-12/11 and N9-14/13 are enabled, causing DMA-MR/ to go active (low) at pin 260 and DMA-MAB18/ to be enabled at pin 36. When CPU memory control is able to receive or transmit memory data, signal DMAX-RA/ (low active) is received by the controller at pin 261. This signal enables the DMA signal generator at G4. The low level at G4-13 (REQ ACC/) resets the DMA request flip-flop (T2) through AND gate J3-1, 2/3. Control line CREQ/ (S2-10) is used to reset the DMA request flip-flop when it is necessary to terminate a DMA request due to the detection of an error. The DMA WRITE signal is transmitted at pin 63. This signal is generated by the microprogram, which controls flip-flop WTRDMP (N1-4). The output of this flip-flop is inverted and buffered by G4-12/11. Flip-flop WTRDMP is also connected through inverter G3-11/10 to G4-4. The STB DTM/ pulse (active low) appears at the output of G4-5. This pulse enables a data transfer to the memory (R9-1, R9-15, P9-1, P9-15, and N9-1 go low). The STB DTM signal is provided by inverter T3-4/6 through selectors P3-11/9 and P4-14/12 to flip-flop J4-6/11, 10.

When the controller initiates a write to memory cycle, the ENBDB flip-flop resets flip-flops J4-6/11, 10 and J4-1/14.

For a DMA write cycle, the STB DTM pulse sets flip-flops J4-4, 1, 16/14. This sets S/R flip-flop M3-2, 3, 1/4. The microprogram checks jump condition DMAWCP (DMA write complete) to determine the end of a DMA write cycle.

Read from Memory

Data is received from memory by the buffer 1 register. This data is transferred from the buffer 2 register through the ALU to the word counter (WC), from which it is sent to the formatter.

When the controller executes a read from memory cycle, the microprogram resets flip-flop RWNOD (N1-11) and initially sets flip-flops WTRDMP (N1-4), COMP1 (N1-10), SELBF1 (S5-4), and SELBF2 (S5-12).

The microprogram resets flip-flop ENBDB (N1-6). When the controller sets the DMA request, flip-flop ENBDB is set.

The DMA-MDS active low pulse is received at pin 262 whenever the controller receives data from the memory. This pulse indicates the availability of memory data to the controller. The DMA-MDS pulse is received by a Schmitt-trigger receiver at G3-13/12 and is transferred through G4-6/7 (DMAX-RA/ is the enable) to the selector at P4.

The STBDFM/ pulse is selected at CLKBUF1 (P4-9). This clock strobes the data from memory into the buffer 1 register. The microprogram initially sets the BFIENB flip-flop (N1-5). The CLKBUF1 pulse sets flip-flop L4-9, 6, 12/11. L4-10 and L5-3 go low, generating a low-going pulse at K4-10. This pulse sets flip-flop L4-7/11. The microprogram checks this flip-flop at jump condition BF2F (H3-15) to determine the completion of the read cycle.

DMA Transfer Cycle Errors

The controller receives DMA-MPE/ (parity error), DMA-PFLT/ (protect fault), and DMA-MAE/ (address error) at pins 252, 237, and 263, respectively. OR gates at H6 enable these signals to be latched into three set/reset flip-flops at H5. Whenever the REQ ACC/ signal is active, H6-12, 2, 10 is active to allow coupling of the memory error signals to the latch inputs (H5-11, 12, 6, 15). Control line CDMAER/ (from M2-10) resets the memory error latches under microprogram control.

To attempt to prevent lost data during DMA transfer, the controller generates a PRIORITY/ signal to pin 227. This signal is activated when the microprogram sets flip-flop PRIOR (B1-4). The priority signal is enabled by the request flip-flop (whenever M9B is high).

NOTE

At pin 39 the controller provides the SLOW DMA signal to optimize the memory performance.

DUAL ACCESS TO THE DEVICES

(This function is not supported in CYBER 18 systems.)

The controller incorporates provisions for dual CPU access to devices. The BUS BUSY/ signal, received at pin 99, is active (low) when the second controller has control of the bus. A jumper double bus (SB) is inserted for dual access. The BUS BUSY/ signal is received by U8-13/12 and transferred (inverted) to jump condition BUSBY (R1-4).

The normal state of flip-flop RQBUS2 (S1-4) is high, thus the output at U1-6 is low.

The bus priority (BP) jumper is inserted or removed to determine which controller will gain bus control when both controllers are attempting to connect onto the bus simultaneously. Control goes to the controller that has the jumper removed.

If the controller has higher priority, the jumper is removed and driver S8A-2, 1/3 receives an enable (S8A-2 is high). Flip-flop RQBUS1 (A1-10) announces that the controller wants to connect onto the bus. If both controllers set their RQBUS1 flip-flop, both controllers generate a BUS NEED/ active low signal at pin 84. The bus busy is received (active low) at pin 99 of the respective controller. U1-6 goes low in both of the controllers.

In the controller that has the simultaneous bus determine jumper inserted, S8A-2 goes low and the BUS NEED/ signal is deactivated (pin 84 goes high). In this mode, the controller without the jumper remains on the bus.

For a normal bus connect operation, the controller transmits the BUS NEED/ signal to the second controller. The microprogram resets flip-flop RQBUS2; U1-6 goes high. The program sets flip-flop RQBUS1; S8A-3 goes low. When the alternate controller releases the bus, the first controller may connect onto it.

The controller can gain immediate bus control by forcing the alternate controller off the bus. Flip-flop FRCBUS (G1-10) through inverter J2-3/4 generates the FORCE BUS/ signal to the alternate at pin 242. The controller can be forced off the bus by the alternate in the following manner: at pin 80 the ALT FORCE/ active low signal is received. This signal is transferred by Schmitt-trigger inverter G3-9/8 and causes the input of NAND gate B9-5 to go high. At the same time, the alternate controller provides a BUS BUSY/ active low pulse at pin 99, causing B9-4 to go high. The output B9-6 generates a master clear active low pulse through AND gate T7-5, 4/6.

The D and S/R flip-flop (R3-4, 1/5) is used as the force bus release index. The microprogram sets this flip-flop via control line SRSTR/ (S2-9). This flip-flop informs the microroutines that the alternate controller has forced the release of the device bus. This index is reset by control line CLDSTR/ (S2-11).

DESTINATION DECODER

The decoder/demultiplexers at L2 and K2 make up the destination decoder. Select inputs L2-1, 2, 3, and K2-1, 2, 3 are connected to PR8, PR9, and PR10. PR11/ enables L2, and PR11 enables K2 (thus choosing between the two decoders); DEST DEC ENB/ from AND gate F2-8 enables L2 and K2. The active low pulse to clock the selected destination is generated when clock phase ϕ3/ enables the L2 and K2 decoder inputs.

The controller uses 12 of 16 destinations. The signal destination (active low pulse) enables the loading of the data into the designated register.

CONTROL LINES

The decoder/demultiplexers at S2 and M2 comprise the control line decoder. Select inputs S2-1, 1, 2 and M2-1, 2, 3 are connected to PR8, PR9, and PR10. PR11/ enables S2, and PR11 enables M2 (thus choosing between the two decoders); MODE CL/FF/ from mode decoder G2-11 enables S2 and M2. The active low pulse of the selected control line is generated when clock phase ϕ3/ enables the S2 and M2 decoder inputs.

The MTTC uses 14 of the 16 control lines. Control line 15 cannot be used due to the structure of the microprogram instruction.

FLIP-FLOP NETWORK

The 8-bit addressable latches (A2, S5, N1, G1, S1, A1, and B1) are multifunctional devices capable of storing single-line data in eight addressable latches.

The addressable latch address inputs (pins 1, 2, and 3) are connected to PR0, PR1, and PR2 through inverters G3-1/2, G3-3/4, and G3-5/6. PR12 determines the data to be stored: if set, the selected flip-flop is set, and if clear, it is reset.

The decoder/demultiplexer at H1 enables the selected group of eight flip-flops. PR3, PR4, and PR5 select the group; PR0, PR1, and PR2 select the flip-flop within the group.

Group selection is enabled when the controller executes a clear flip-flop (CL/FF) instruction. An active low MODE CL/FF/ signal enables H1 (H1-5 goes low). The H1 outputs, which are connected to enable pins (pin 14) of each of the flip-flop groups, generate an active low pulse on the selected output pin during the ϕ3/ clock phase at H1-4.

Groups 1, 2, 3, 4, and 5 are connected to the CCMR2/ signal. A clear controller signal clears the flip-flops in these groups. Groups 6 and 7 are connected only to the general reset (GR/) signal, and the clear controller command does not clear these two groups of flip-flops. The controller flip-flop network includes a total of 56 flip-flops.

JUMP CONDITION NETWORK

The jump condition network is made up of the 8-to-1 data selector/multiplexers T1, R1, M1, H3, H7, F1, U7, E1, J1, and N2; the 2-input AND-OR invert gate at M5; the OR gate at K3-1, 2/3; the inverters at H2 and T3-11/10; and the flip-flop at H5.

There are nine groups of jump conditions. PR10, PR11, and PR12 select the jump condition within one of the nine jump condition groups. Bits PR10, PR11, and PR12 are inverted by H2-9/8, H2-11/10, and H2-13/12 and are connected to input pins 11, 10, and 9 of T1, R1, M1, H3, H7, F1, U7, and E1 (jump condition groups 1 to 8) and J1 (group 9).

Jump condition groups 1 to 8 strobe inputs are constantly enabled via a connection to ground. Jump condition group 9 is enabled by an active low signal at K3-3 (PR15 ORed with ϕ3/).

PROM bits PR12, PR14, and PR9 select the jump condition group. The strobe to this selector (N2-7) comes from K3-3 when the controller executes a jump instruction (PR15 is low). OR gate K3-1, 2/3 provides this strobe signal with the ϕ3/ pulse. Flip-flop JGRP9 (G1-11) controls the selection of the jump condition. When the flip-flop is reset, the controller selects the jump condition within groups 1 to 8. When flip-flop JGRP9 is set, the microprogram selects the jump conditions in group 9 (J1). Inverter H2-5/6 and gate M5-13, 1, 9, 10/8 provide this selection. The state of the S/R flip-flop at H5 depends on the state of the selected jump condition.

The S/R flip-flop at H5 is also set by a PCD/ (L2-7) active low pulse whenever the program counter (PC) is the destination register for an inter-register instruction.

The flip-flop output (H5-4) is inverted by T3-11/10 and provides the LOAD PC/ pulse for the program counter. The program counter is loaded with the ALU-out data and the data selected by the multiplexer at A4, thus executing a microprogram jump.

The LOAD PC/ signal is active during the time interval from the leading edge of clock phase ϕ3/ to the leading edge of the next ϕ2/ clock phase (ϕ2/ resets the S/R flip-flop at H5).

The controller includes a total of 72 jump conditions.

UNIT PROTECT JUMPERS

The unit is protected whenever the respective protect jumper is inserted. The unit protect jumpers (SD4 through SD7) are located at P1 and are connected to the 4-input multiplexer at P2. Inverted output P2-14 is connected to jump condition UNTPRT (F1-14). Jumper SD7 is associated with unit 0 and jumper SD4 is associated with unit 3.

A removed jumper indicates an unprotected unit.

MAINTENANCE SWITCHES

The on/off-line (LS) switch is connected to jump condition ONOFLN. In the on position, the switch permits normal controller activity. In the off position, the switch disconnects the controller from the A/Q bus of the computer and places the controller in maintenance mode. In this mode, AND gate output U4-12 is low. Sequence input U6-4 is also low and disables sequencer operation. Consequently all A/Q commands received generate an internal reject.

The type of operation performed is determined by the positions of the maintenance switches (MS1 - MS3):

- MS1 is connected to jump condition MSW1 (J1-14).
- MS2 is connected to jump condition MSW2 (J1-2).
- MS3 is connected to jump condition MSW3 (J1-1).

The off-line operation initiated on the first tape that is ready conforms to table 5-1.

TABLE 5-1. OFF-LINE OPERATION

MS2	MS1	Operation
Off	Off	Continuous read
Off	On	Continuous read
On	Off	Continuous write - 1's
On	On	Continuous write - 0's

Switch MS3 determines the density at which the off-line operation is to be performed:

- MS3 on = Low density
- MS3 off = High density

JUMPER JM

The mode jumper (JM) determines the activity mode of the exclusive OR gates at R4. When the JM jumper is inserted, T3-2 is high and the gates invert the data transferred by the receivers (T9). When the JM jumper is removed, the gates transfer the data without inversion. For the MTTC, JM is removed.

Signal and termination conditions applicable to inputs from the formatter to the MTTC are listed in table 5-2. All input signals from the formatter are active low.

Signal and termination conditions applicable to outputs from the MTTC to the formatter are listed in table 5-3. The output signals are enabled only when the controller has the device bus; that is, the flip-flop ONBUSFF (A1-9) is set. All output signals to the formatter are active low.

NOTE

Gate S6B-6, 7/5 is wire-ORed with gate S6A-6, 7/5. With jumper JM removed, S6A-2 and S6A-7 are low. The outputs at pin 81 and 85 are OFL and WRT, respectively.

LOGIC DIAGRAMS

Figure 5-4 is the logic diagrams for the magnetic tape transport controller.

TABLE 5-2. INPUTS FROM FORMATTER

Pin Number	Signal Name	Termination Type	Receiver Location	Jump Condition Name of Location
16	FPT	220/330	H9-9/8	FPT (H7-15)
20	FMK	220/330	E9-11/10, H8-4/13	FMK (H7-12)
21	TFER	220/330	E9-13/12	TFER (H7-13)
22	RDY	220/330	H9-5/6	RDY (H7-2)
23	MOP1	220/330	H9-1/2	MOP1 (H7-4)
24	FBY	220/330	H9-3/4	FBY (H7-3)
25	ONL	220/330	E9-9/8	ONL (H7-1)
27	CER	220/330	E8-9/8	CER (J1-3)
28	R1	220/330	E8-3/4	B-register (E7-5)
29	R0	220/330	E8-5/6	B-register (E7-2)
30	R3	220/330	E9-1/2	B-register (E7-1)
31	R6	220/330	E9-3/4	B-register (E6-6)
33	R4	220/330	E8-13/12	B-register (E6-2)
34	R7	220/330	E8-11/10	B-register (E6-1)
37	R2	220/330	E8-1/2	B-register (E7-6)
38	R5	220/330	E9-5/6	B-register (E6-5)
40	ES0	220/330	G9-1/2	HEROUT (H3-1)
41	ES1	220/330	G9-3/4	HEROUT (H3-1)
43	ES3	220/330	G9-9/8	HEROUT (H3-1)
44	HER	220/330	G9-11/10	HEROUT (H3-1)
45	ES2	220/330	G9-5/6	HEROUT (H3-1)
91	RSTR	470 ohms	T9-13/12, R4-10,9/8, R3-2,3/5	RSTRLT (R1-1)
92	WSTR	470 ohms	T9-9/8, R4-13,12/11, R3-12,11/9	WSTRLT (R1-14)

TABLE 5-2. INPUTS FROM FORMATTER (Contd)

Pin Number	Signal Name	Termination Type	Receiver Location	Jump Condition Name of Location
93	LDP	220/330	U8-1/2	LDP (R1-2)
94	IDENT/ECG	470 ohms	U9-1/2	IDENT (U7-4)
95	MOP2	470 ohms	U9-3/4	MOP2 (U7-3)
96	SOP	470 ohms	U9-5/6	SOP (U7-2)
97	RDM	470 ohms	U9-11/10	RDM (U7-15)
98	RW-STAT	220/330	U8-9/8	RWS (U7-13)
295	EOT	220/330	U8-5/6	EOT (J1-4)
296	RP	220/330	U8-3/4	RP (M1-12)
297	7TRK	470 ohms	U9-9/8	TRK7 (U7-1)
298	NRZI	470 ohms	U9-13/12	NRZI (U7-14)
299	CRJ	220/330	U8-11/10	CRJ (U7-12)

TABLE 5-3. OUTPUTS TO FORMATTER

Pin Number	Signal Name	Origin	Driver Location
3	DEN	Flip-flop DEN	A9B-1,2/3
4	TADO	Flip-flop TADO	A9A-1,2/3
5	THR	Flip-flop THR	A8A-1,2/3
7	SPM	Flip-flop SPM	A8A-6,7/5
8	REW	Flip-flop REW	A8B-6,7/5
9	TAD1	Flip-flop TAD1	A9A-6,7/5
10	PAR	Flip-flop PARFF	A9B-6,7/5
11	W0	Word count B7-3	C8A-1,2/3
12	W6	Word count B6-6	C8B-1,2/3
13	W2	Word count B7-6	C9A-1,2/3
14	W5	Word count B6-2	C9B-1,2/3
15	W4	Word count B6-3	C9B-6,7/5
17	W1	Word count B7-2	C9A-6,7/5
18	W7	Word count B6-7	C8B-6,7/5
19	W3	Word count B7-7	C8A-6,7/5
49	ERS	Flip-flop ERS	J5-1,2/3,4/5
50	WFM	Flip-flop WFM	A8B-1,2/3

TABLE 5-3. OUTPUTS TO FORMATTER (Contd)

Pin Number	Signal Name	Origin	Driver Location
81	OFL	Flip-flop OFL	S6B-1,2/3
82	GO	Flip-flop GO	S7A-1,2/3
85	WRT	Flip-flop WRT	S6B-6,7/5
86	FEN	Flip-flop FEN	S7A-6,7/5
87	ACK	Flip-flop ACK	S7B-6,7/5
88	REV	Flip-flop REV	S8A-6,7/5
250	WP	Flip-flop	M9B-6,7/5
294	LWD	Flip-flop LWD	S7B-1,2/3

SIGNAL	PIN	[illegible]
[illegible]	[illegible]	[illegible]
ADR01/	[illegible]	0120
ADR02/	[illegible]	0120
ADR03/	[illegible]	0120
ADR04/	[illegible]	0120
ADR05/	212	0110
ADR06/	217	0120
ADR08/ (Q07)	281	0108
ADR09/ (Q08)	282	0108
ADR10/ (Q09)	283	0109
ADR11/ (Q10)	284	0108
ALT FØRCE/	80	0111
AUTØLØAD/	42	0124
BUS BUSY/	99	0111
BUS NEED/	84	0111
CER/	27	0127
CRJ/	299	0127
DEN/	3	0125
DFM01	264	0102
DFM02	265	0102
DFM03	266	0102
DFM04	267	0102
DFM05	268	0102
DFM06	269	0102
DFM07	270	0102
DFM08	271	0102
DFM09	272	0102
DFM10	273	0102
DFM11	274	0102
DFM12	275	0102
DFM13	276	0102
DFM14	277	0102
DFM15	278	0102
DFM16	279'	0102
DMA-DTM01/	64	0106
DMA-DTM02/	65	0106
DMA-DTM03/	66	0106
DMA-DTM04/	67	0106
DMA-DTM05/	68	0105
DMA-DTM06/	69	0105
DMA-DTM07/	70	0105
DMA-DTM08/	71	0105
DMA-DTM09/	72	0106
DMA-DTM10/	73	0106
DMA-DTM11/	74	0106
DMA-DTM12/	75	0106
DMA-DTM13/	76	0105
DMA-DTM14/	77	0105
DMA-DTM15/	78	0105
DMA-DTM16/	79	0105
DMA-MAB01/	53	0103
DMA-MAB02/	54	0103
DMA-MAB03/	55	0103
DMA-MAB04/	56	0104
DMA-MAB05/	57	0104
DMA-MAB06/	58	0104
DMA-MAB07/	59	0104
DMA-MAB08/	80	0104
DMA-MAB09/	81	0103

SIGNAL	PIN	[illegible]
DMA-MAB10/	62	0103
DMA-MAB11/	253	0103
DMA-MAB12/	254	0103
DMA-MAB13/	255	0104
DMA-MAB14/	256	0104
DMA-MAB15/	257	0104
DMA-MAB16/	258	0104
DMA-MAB17/	35	0103
DMA-MAB18/	36	0103
DMA-MAE/	263	0111
DMA-MDS/	262	0111
DMA-MPE/	252	0111
DMA-MR/	260	0103
DMA-PFLT/	237	0111
DMA-PRØT/	232	0111
DMA-WRITE	63	0111
DMAX-RA/	261	0111
ENPRTSYS/	293	0122
EØT/	295	0127
ERS/	49	0107
ES00/	40	0126
ES01/	41	0126
ES02/	45	0126
ES03/	43	0126
FBY/	24	0126
FEN/	86	0125
FMK/	20	0127
FØRCE BUS/	242	0111
FPT/	16	0127
GND	6	0101
GND	26	0101
GND	32	0101
GND	83	0101
GND	101	0101
GND	102	0101
GND	232	0101
GND	251	0101
GND	301	0101
GND	302	0101
GØ/	82	0125
HER/	44	0126
IDENT/ECG	94	0127
INTRPT/	249	0123
LDP/	93	0127
LWD	294	0125
MØP 1/	23	0126
MØP 2/	95	0127
MR/	46	0109
NRZI/	298	0127
ØFL/	81	0125
ØNL/	25	0126
PAR/	10	0125

SIGNAL	PIN	[illegible]
PRIØRITY/	227	0113
PRØGPRØT/	201	0110
RDM/	97	0127
RDY/	22	0126
RD01/	204	0112
RD02/	206	0112
RD03/	208	0112
RD04/	210	0112
RD05/	214	0112
RD06/	218	0112
RD07/	221	0112
RD08/	224	0112
RD09/	226	0112
RD10/	229	0112
RD11/	231	0112
RD12/	234	0112
RD13/	236	0112
RD14/	239	0112
RD15/	241	0112
RD16/	244	0112
READSSTB/	248	0110
REJECT	220	0110
REPLY/	216	0110
REV/	88	0125
REW/	8	0125
RP/	296	0126
RSTR	91	0127
RW-STAT/	98	0126
R0/	29	0118
R1/	28	0118
R2/	37	0118
R3/	30	0118
R4/	33	0118
R5/	38	0118
R6/	31	0118
R7/	34	0118
SD01/	203	0120
SD02/	205	0120
SD03/	207	0120
SD04/	209	0120
SD05/	211	0120
SD06/	215	0120
SD07/	219	0120
SD08/	223	0120
SD09/	225	0120
SD10/	228	0120
SD11/	230	0120
SD12/	233	0120
SD13/	235	0120
SD14/	238	0120
SD15/	240	0120
SD16/	243	0120
SLØW DMA	239	0111
SØP/	96	0127
SPM/	07	0114
TAD0/	4	0125
TAD1/	9	0125
TFER/	21	0127
THR/	5	0125

SIGNAL	PIN	[illegible]
WEØ/	292	0108
WFM/	50	0125
WP/	250	0125
WRITE/	290	0110
WRT/	85	0125
WSTR	92	0127
W0/	11	0114
W1/	17	0114
W2/	13	0114
W3/	19	0114
W4/	15	0114
W5/	14	0114
W6/	12	0114
W7/	18	0114
7TRK	297	0127
+5V	1	0101
+5V	2	0101
+5V	201	0101
+5V	202	0101

REV	ECO	DESCRIPTION	DFT	DATE	APP
A	05/9373	OL & RELEASED		6-7-82	

NØTES: UNLESS ØTHERWISE SPECIFIED

1. ALL RESISTØRS ARE IN ØHMS, ±5%, 1/4W.
2. IN SOME CIRCUIT ELEMENTS THE VENDOR'S NUMBER IS SHOWN WITHOUT THE PREFIX "74"- H00 = 74H00.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AAL030

LOGIC TYPE: EIFWT

CONTROL DATA CORPORATION — DATA STORAGE, LA JOLLA DIVISION, LA JOLLA, CA

FIRST USED ON: FA465-B

TITLE: LØGIC DIAGRAM- LCTT FØRMAT CØNTRØLLER

C | CODE IDENT 09132 | DWG NO. 96...

SHEET 1 ØF 28

NOTE: THIS LOGIC DIAGRAM IS APPLICABLE TO MTTC ASSEMBLIES 96890068 AND 96890071.

Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 1 of 28)

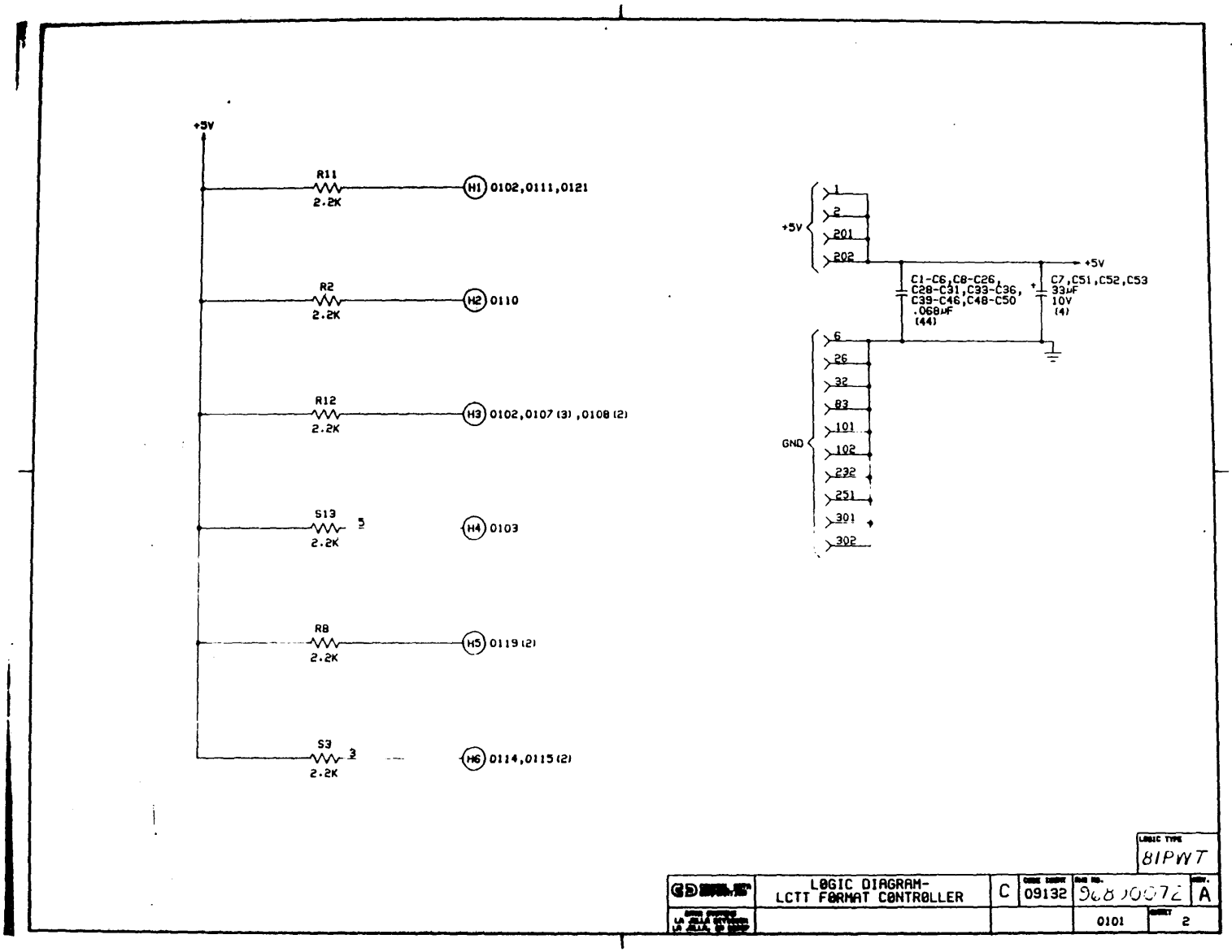


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 2 of 28)

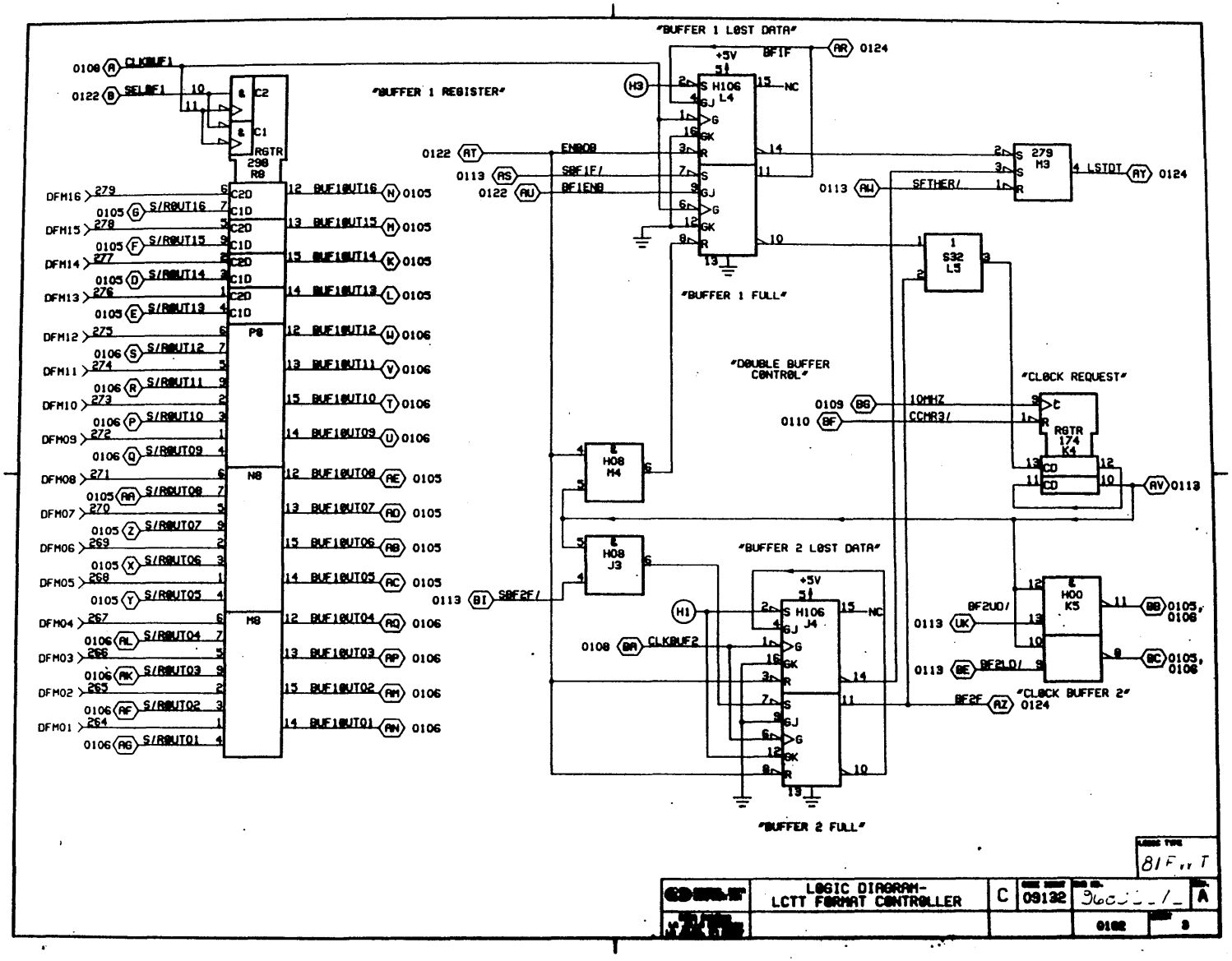


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 3 of 28)

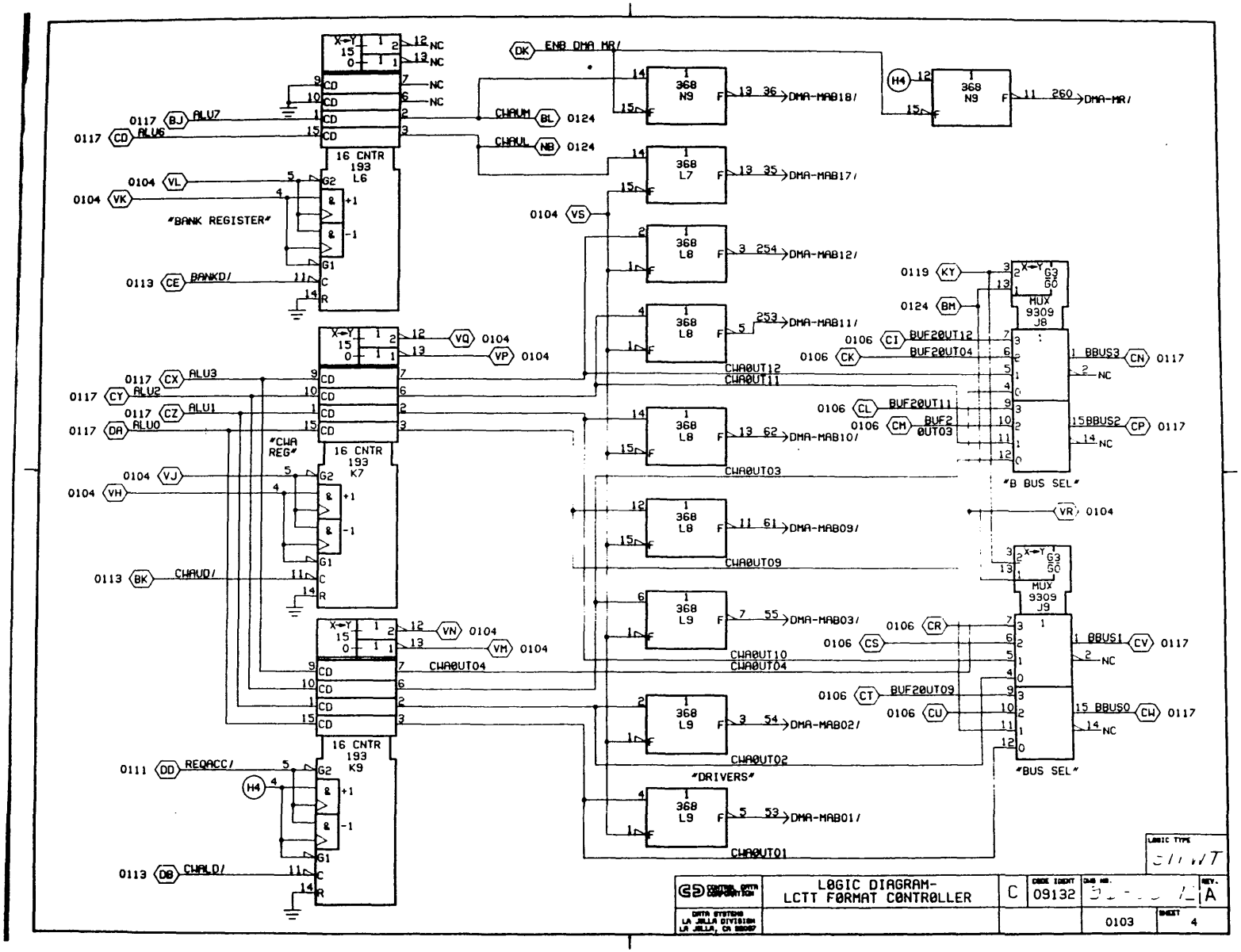


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 4 of 28)

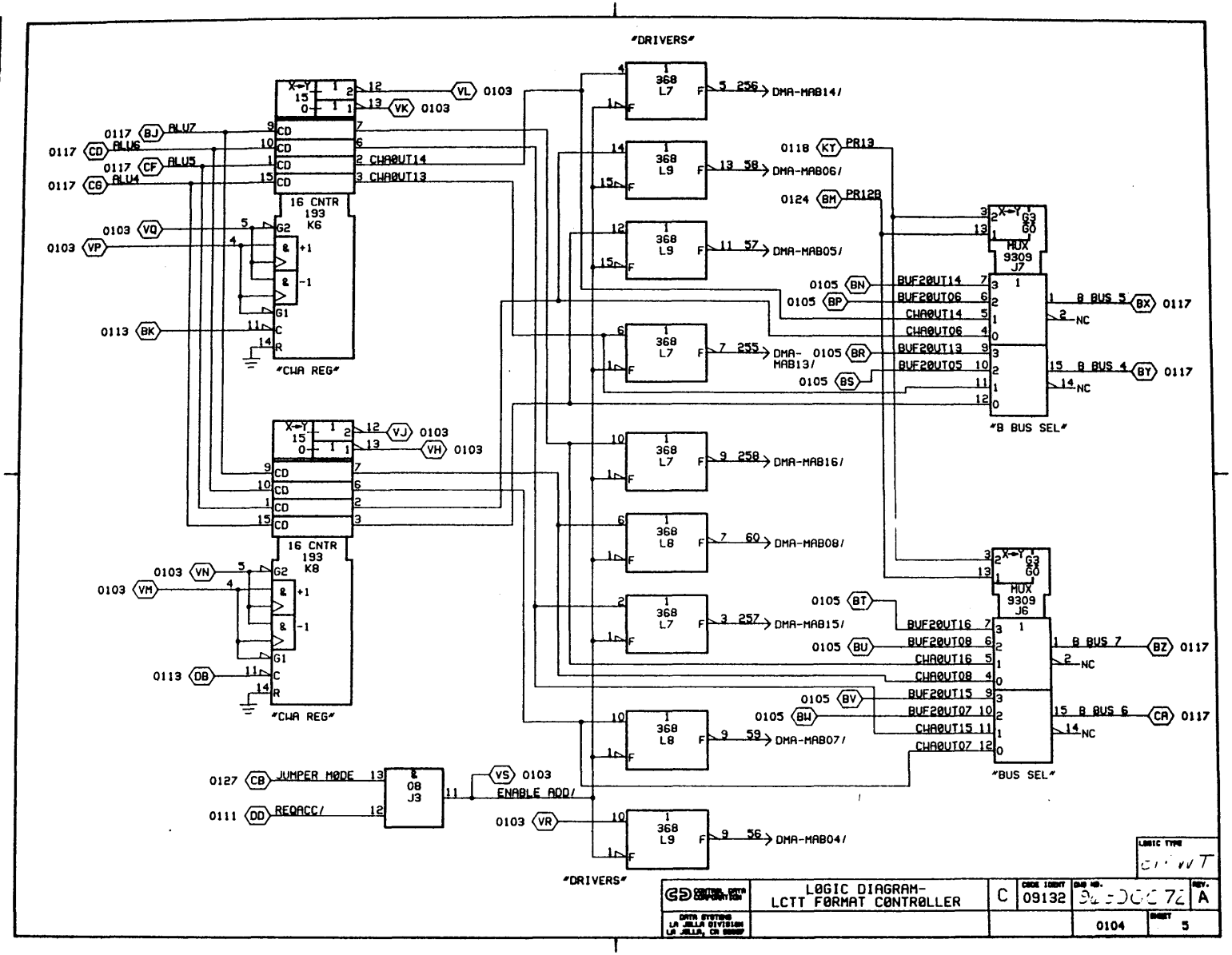


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 5 of 28)

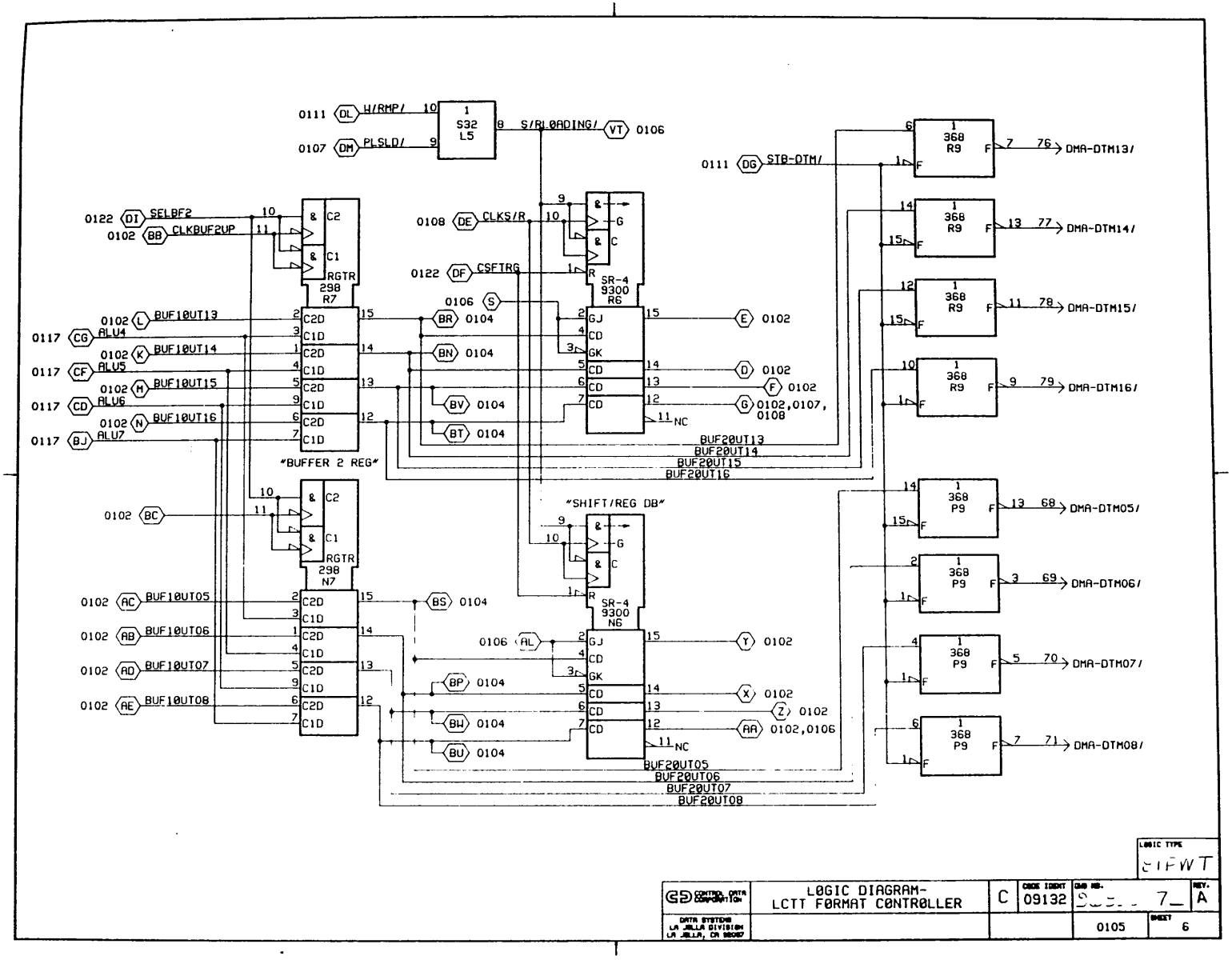


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 6 of 28)

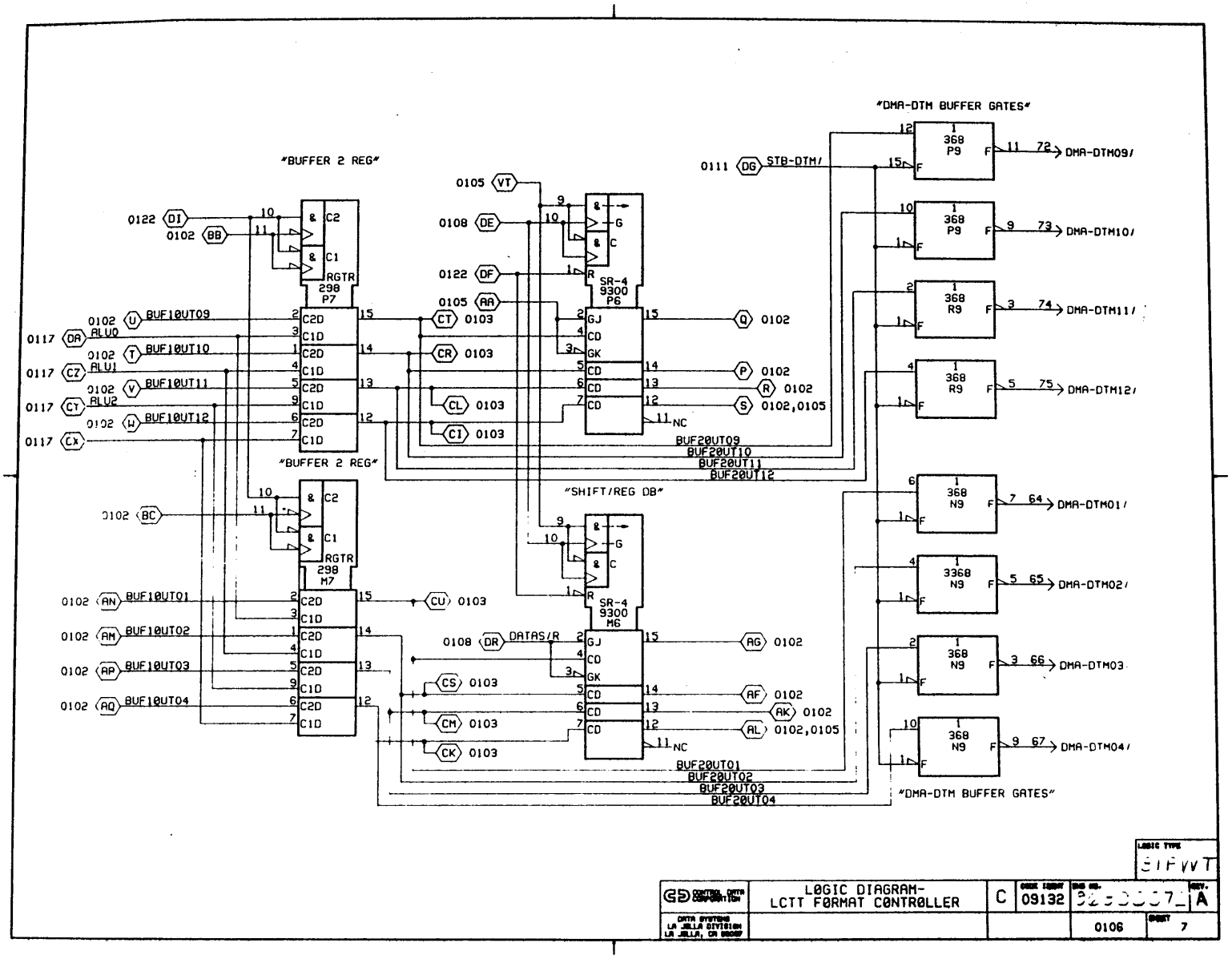


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 7 of 28)

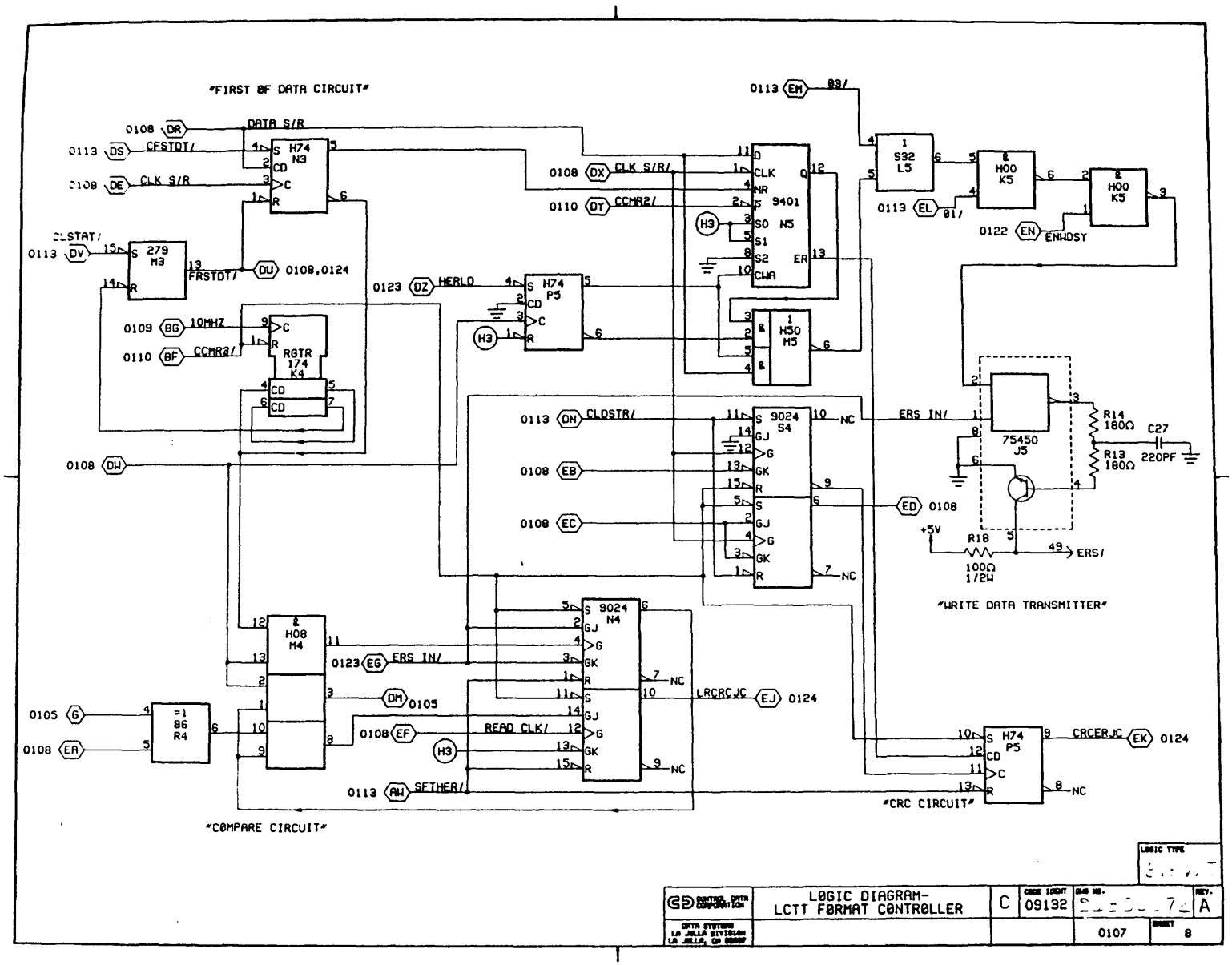


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 8 of 28)

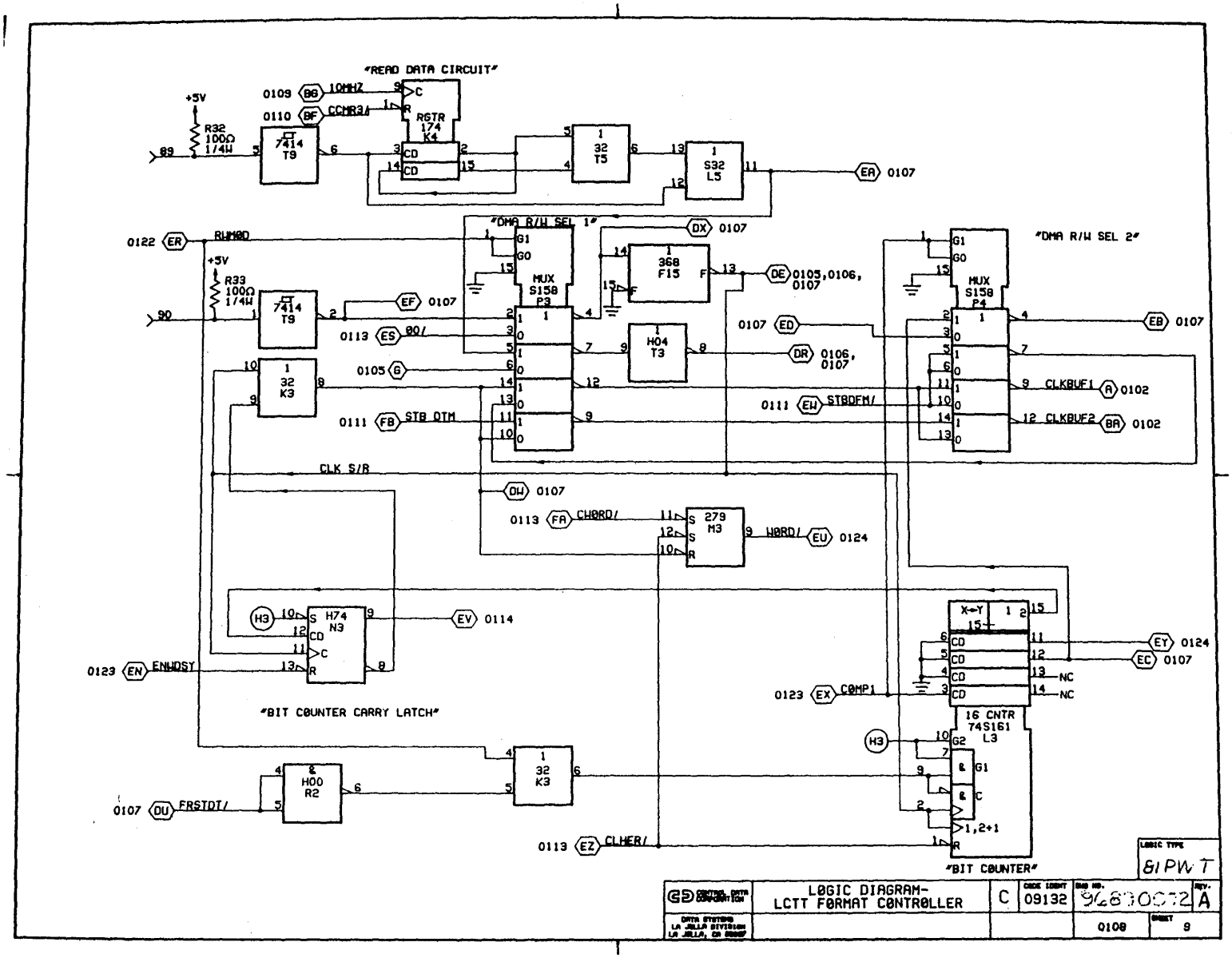


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 9 of 28)

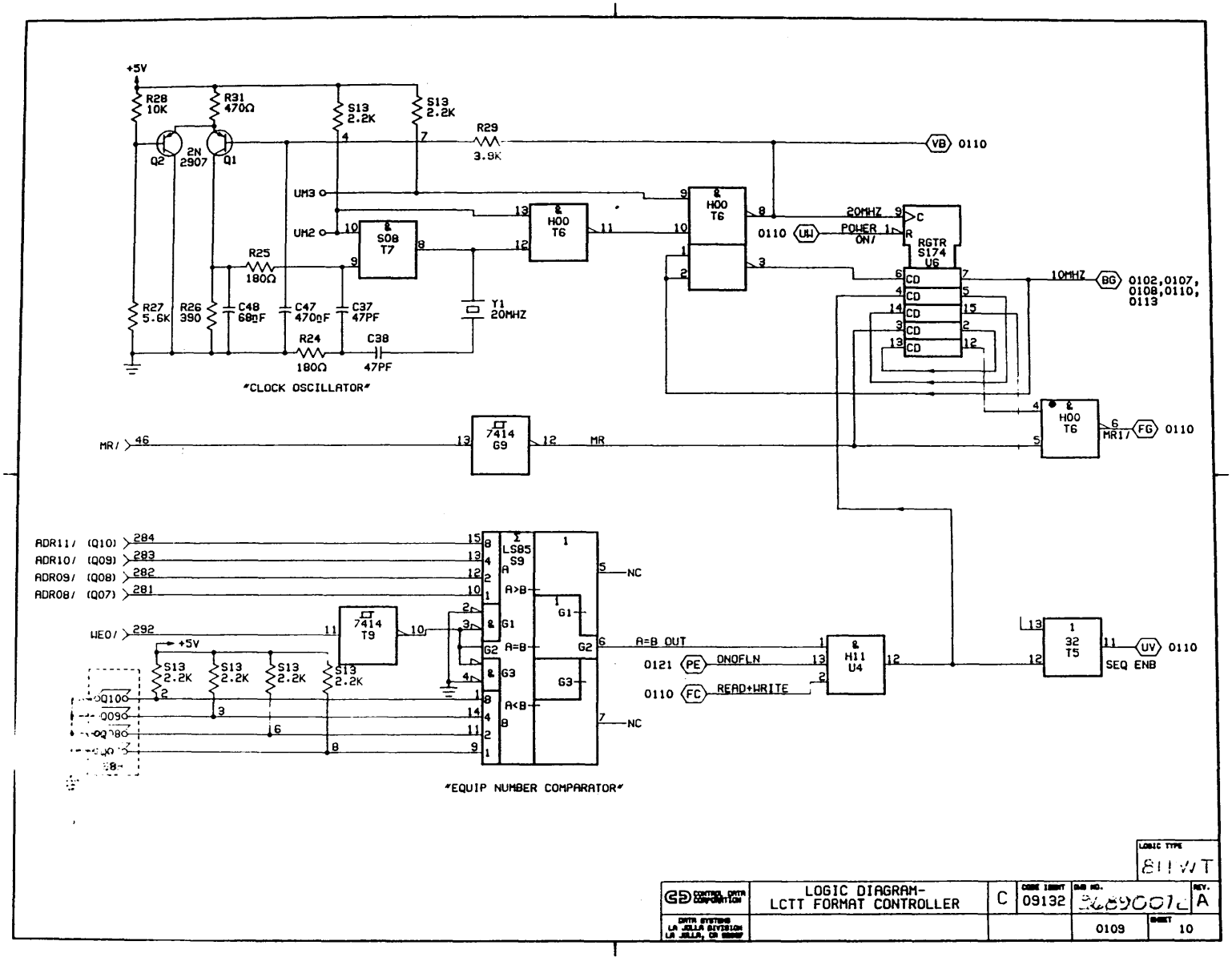


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 10 of 28)

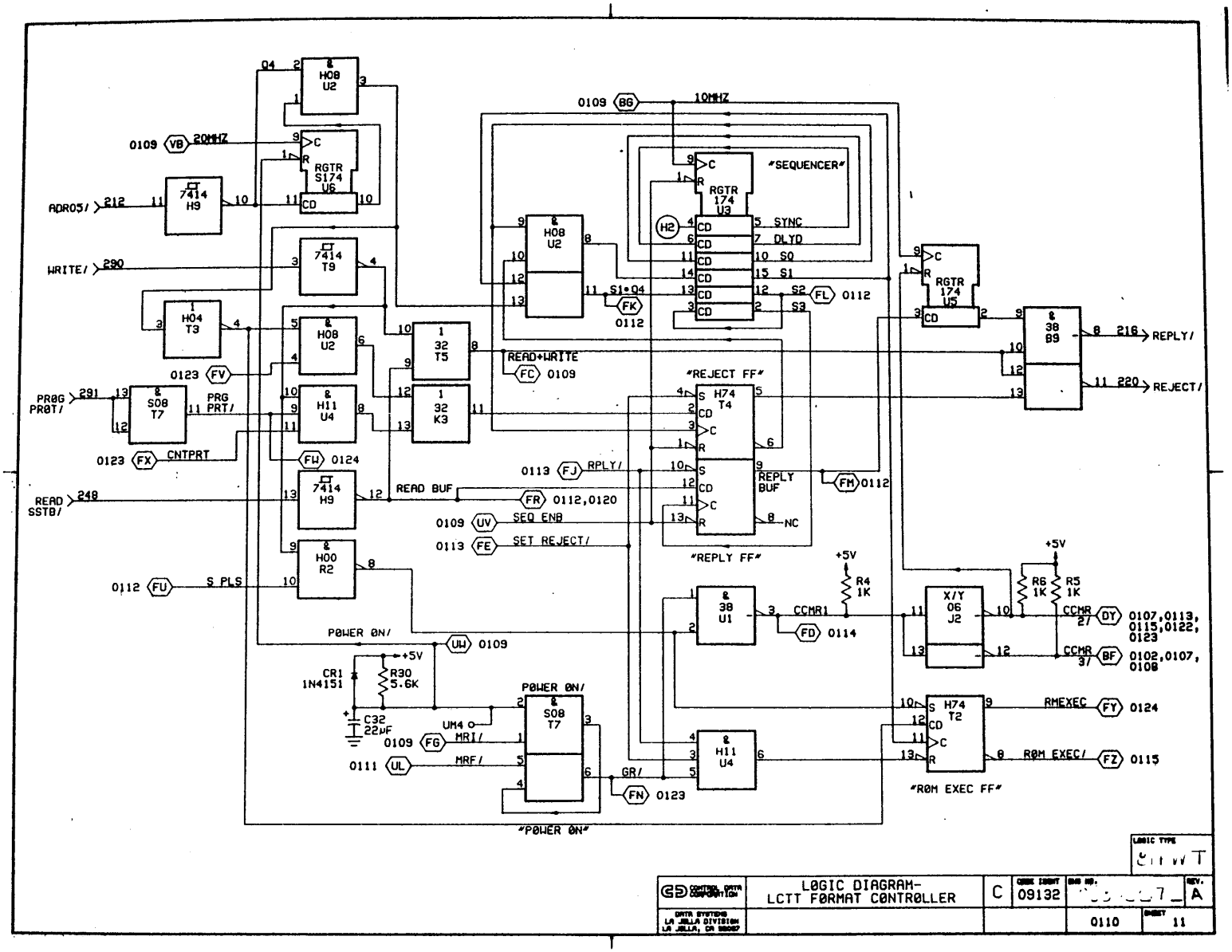


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 11 of 28)

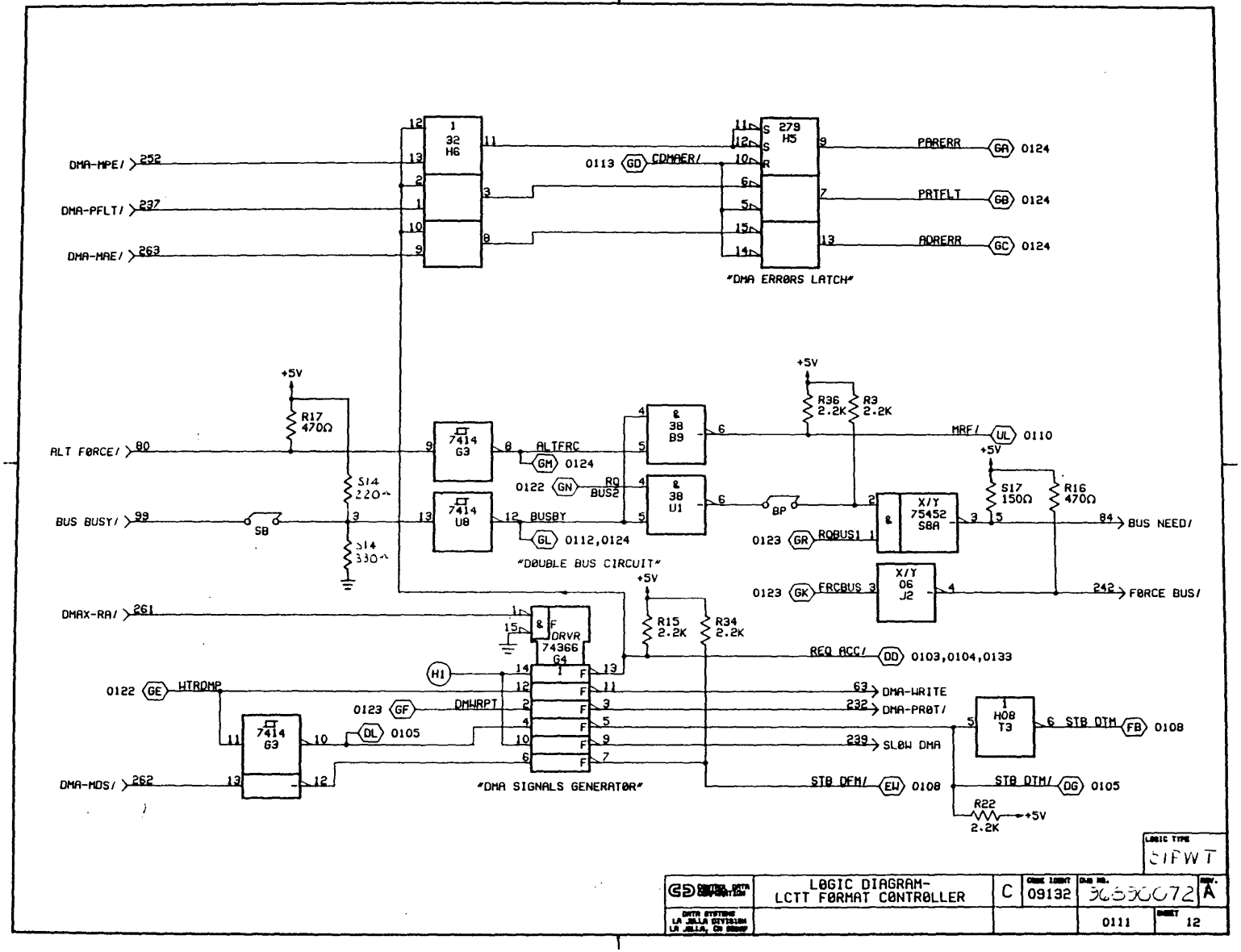


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 12 of 28)

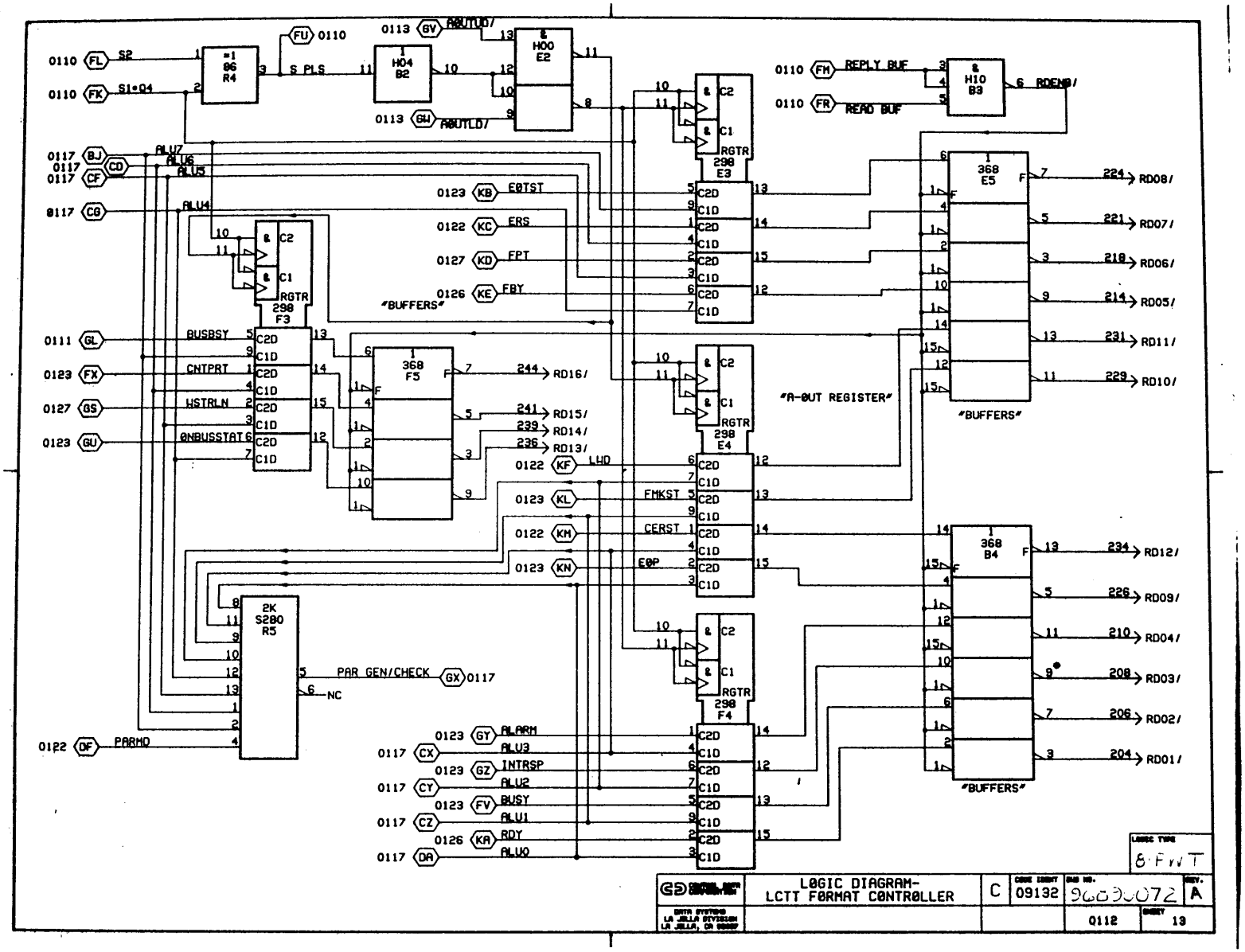


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 13 of 28)

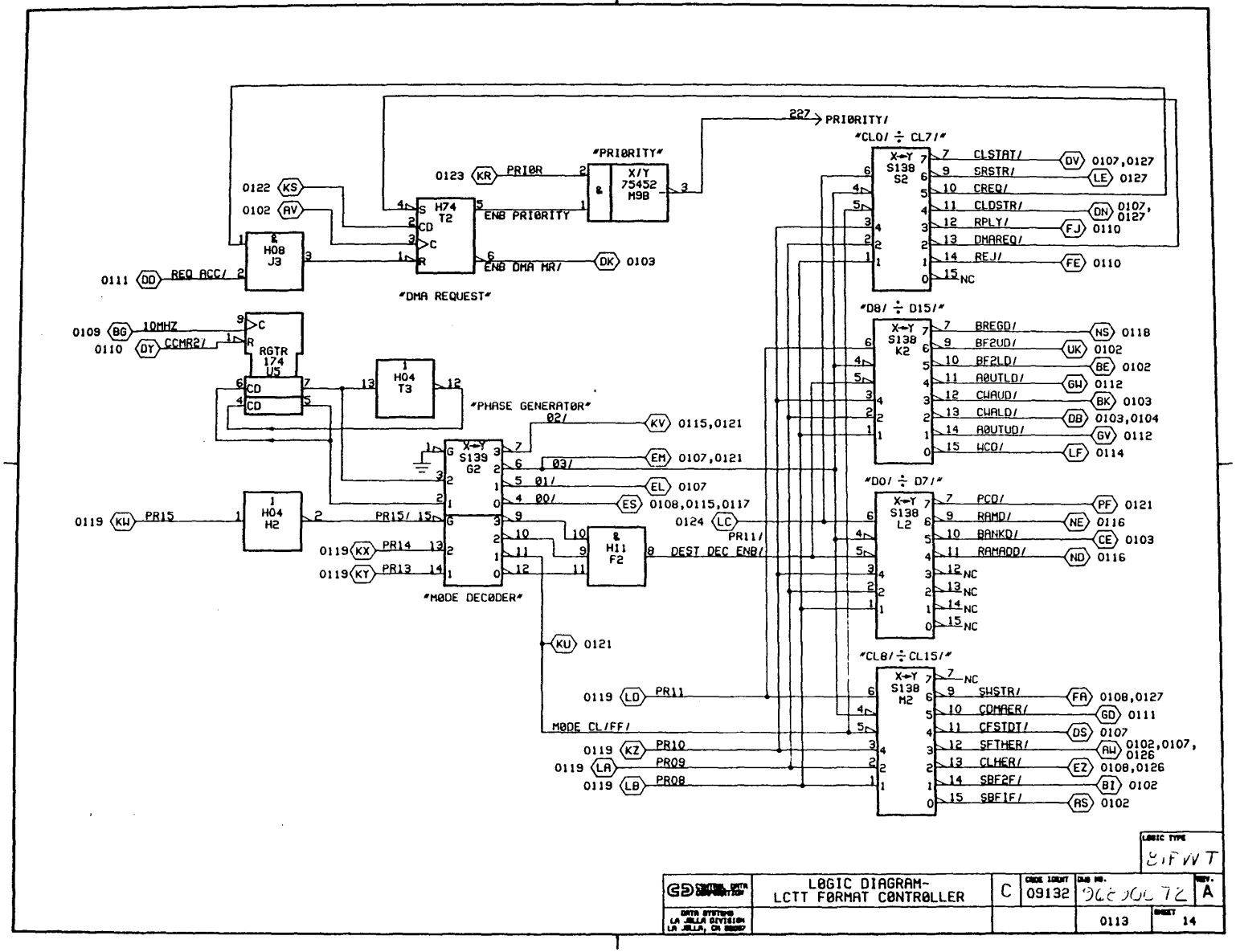


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 14 of 28)

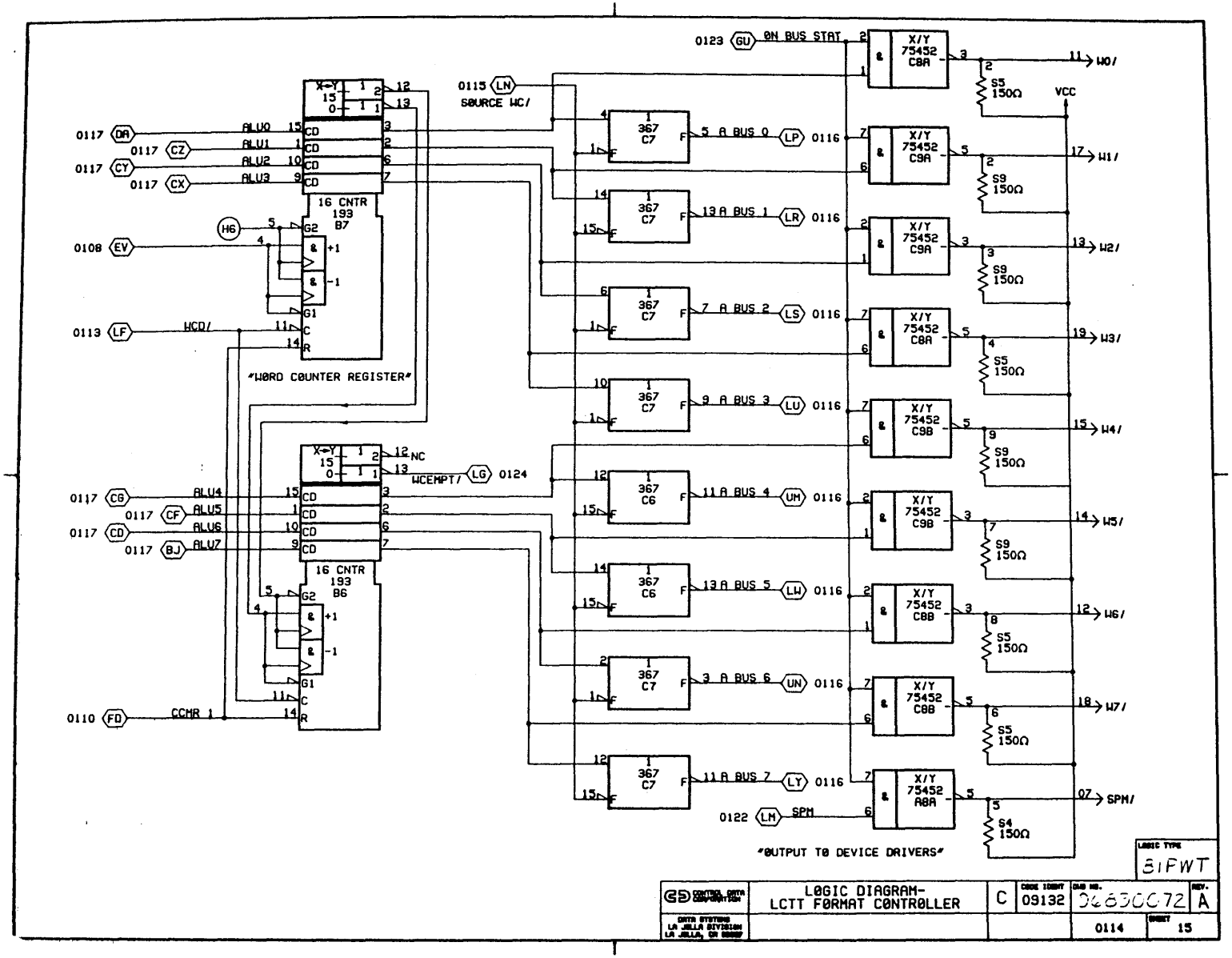


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 15 of 28)

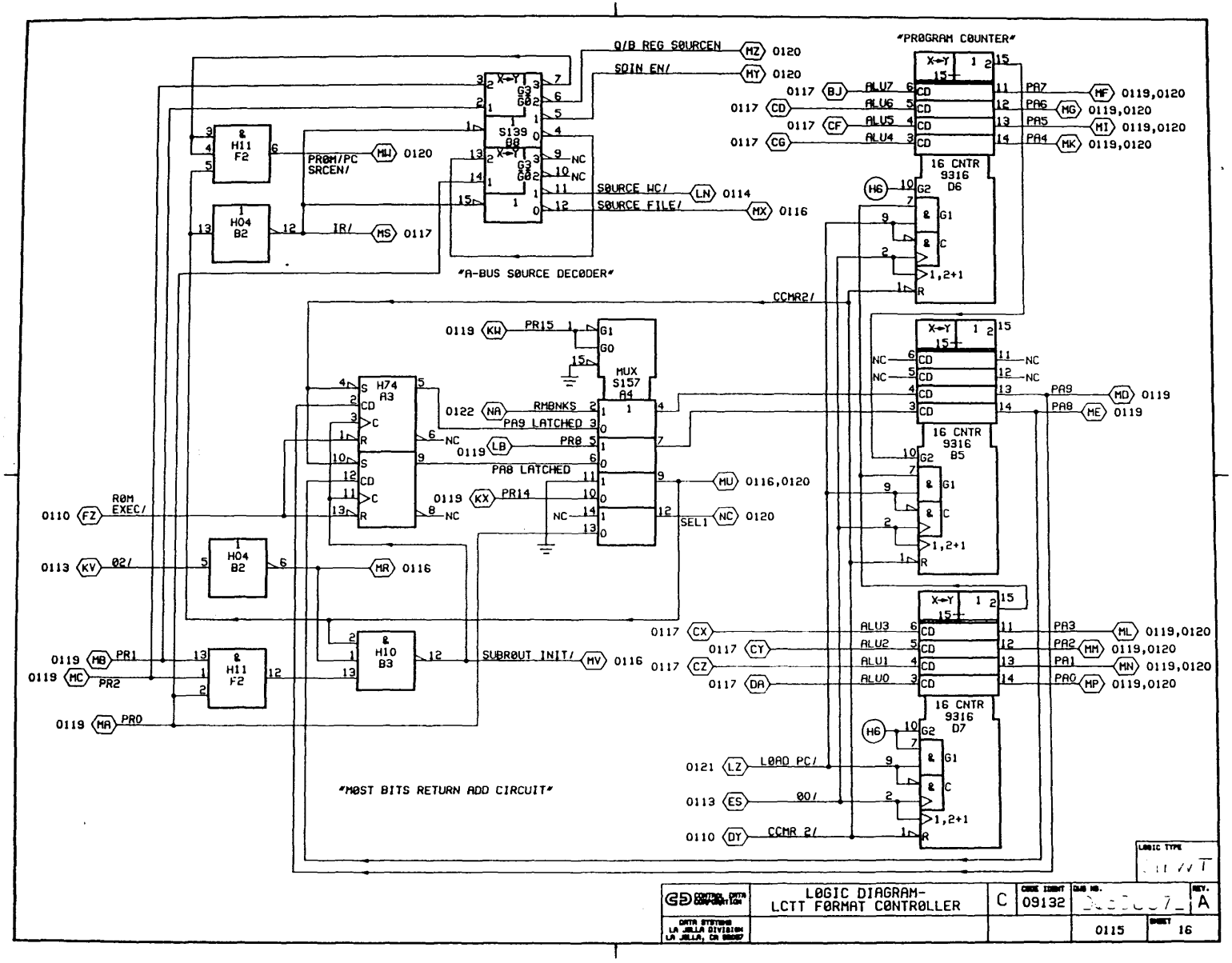


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 16 of 28)

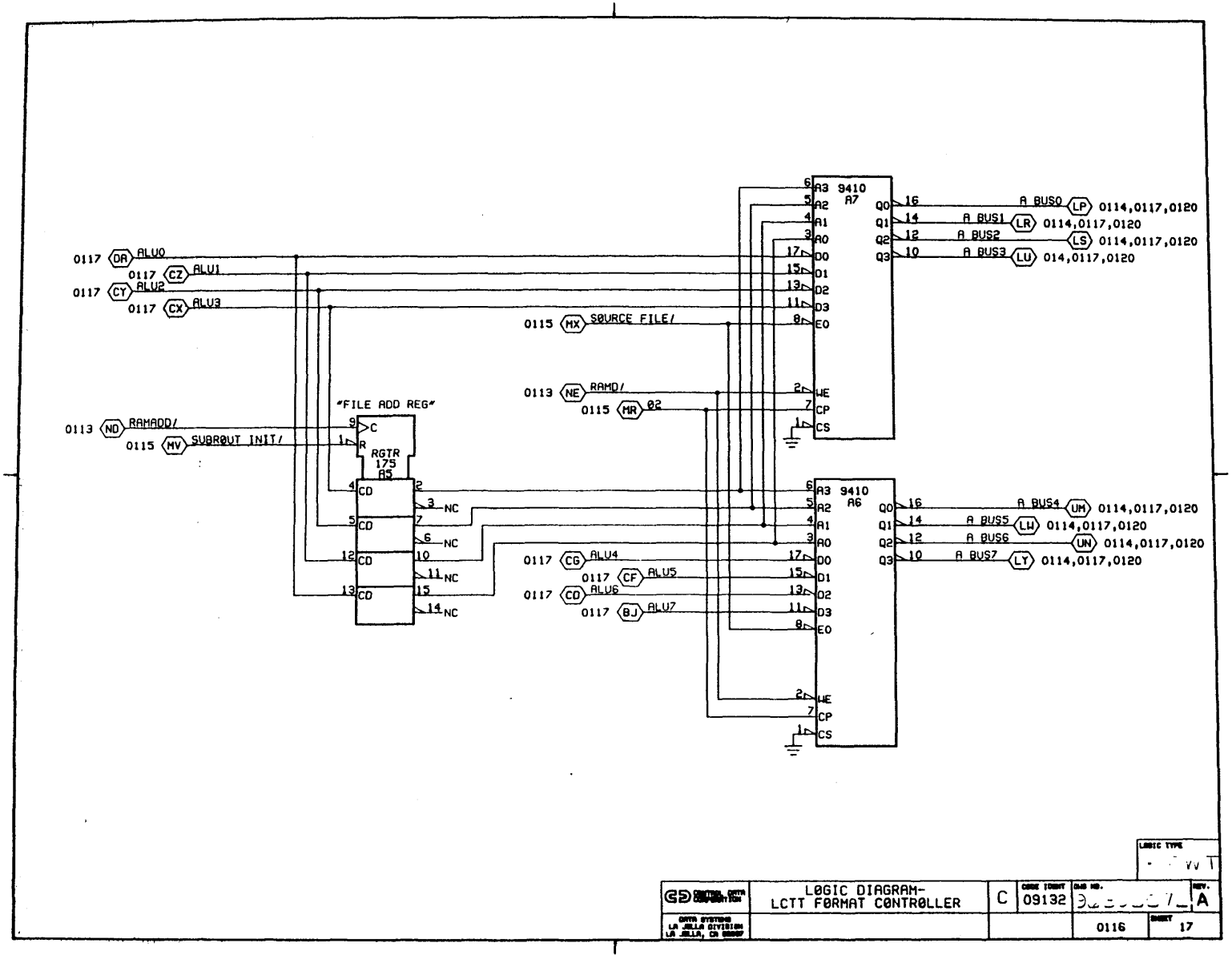


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 17 of 28)

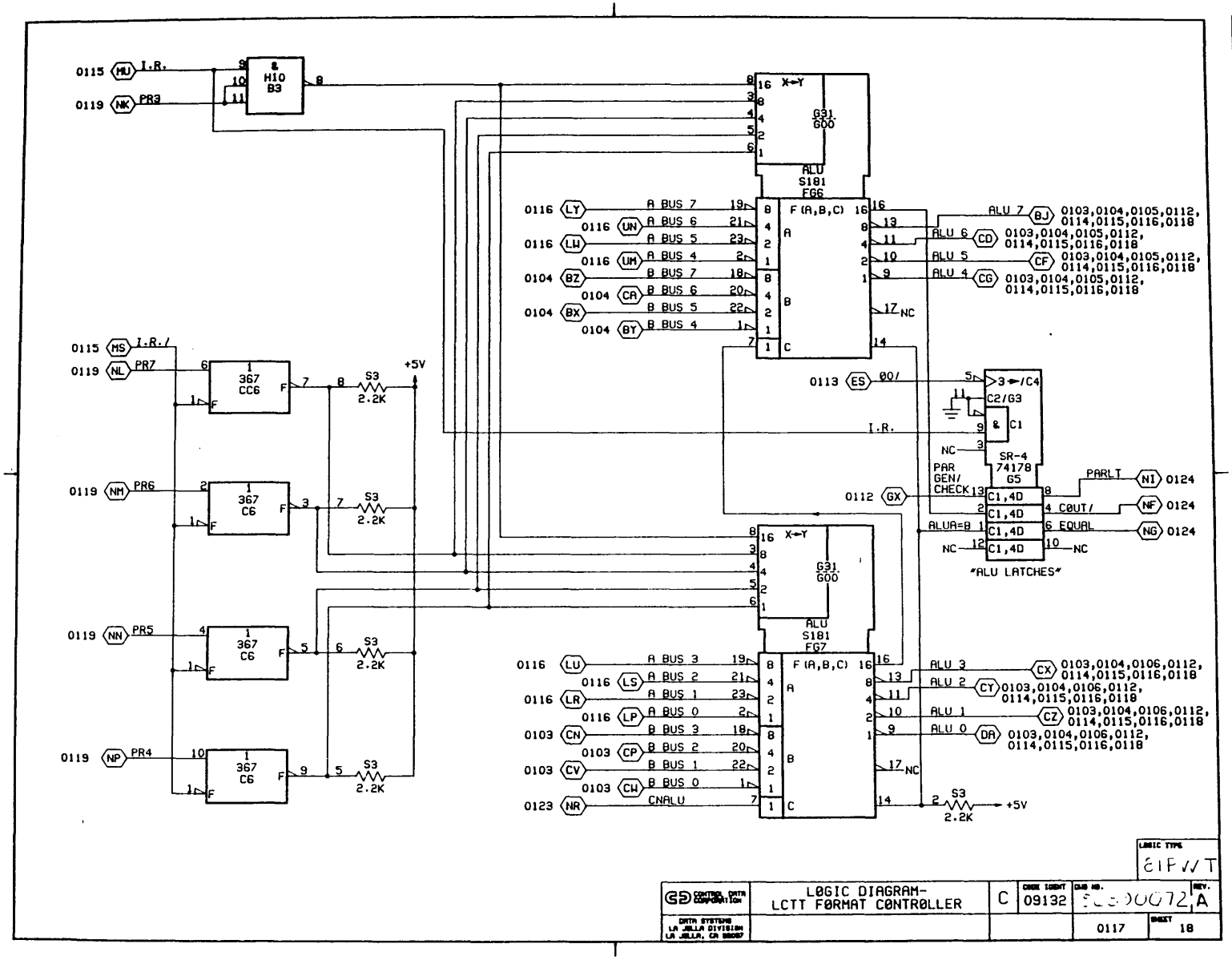


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 18 of 28)

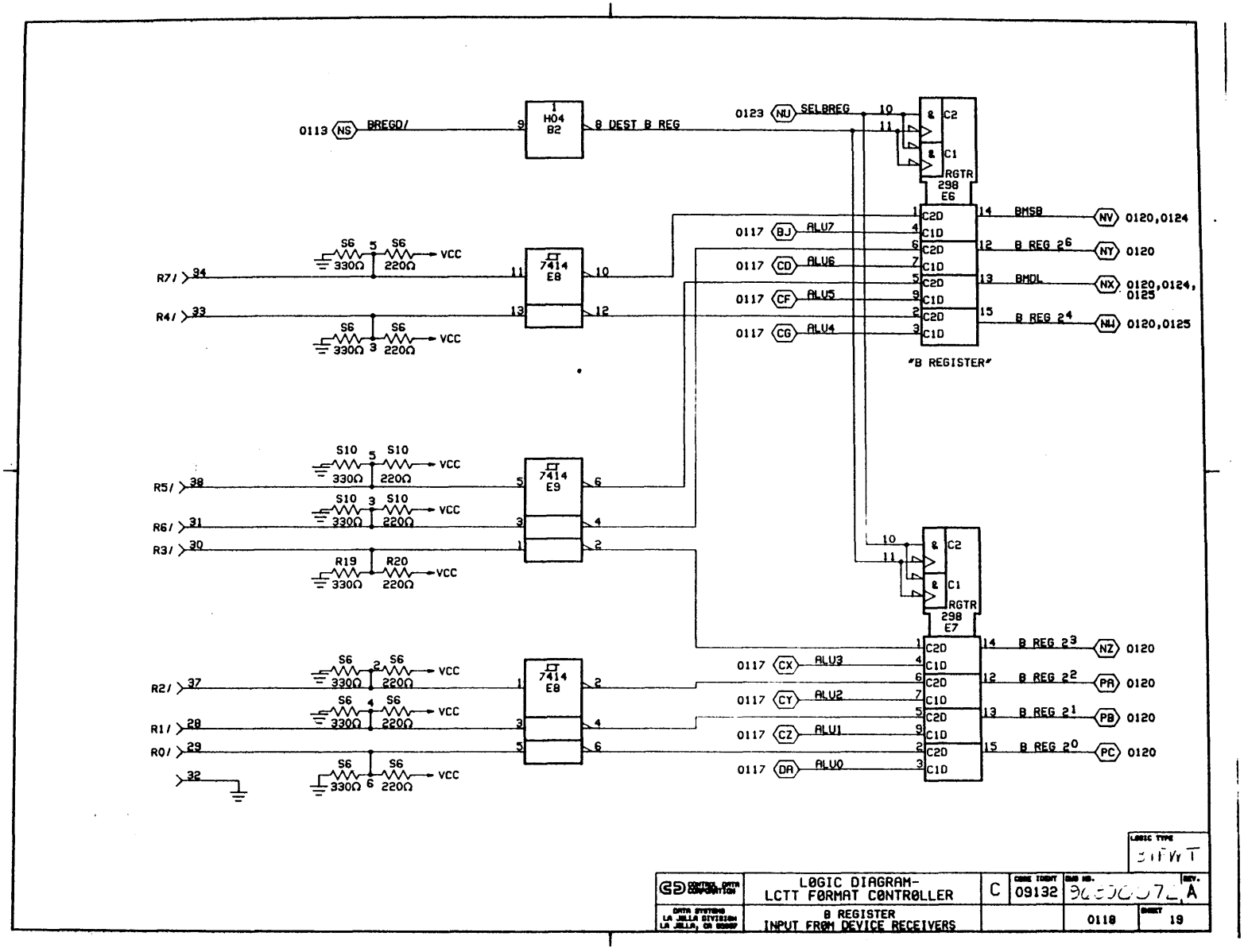


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 19 of 28)

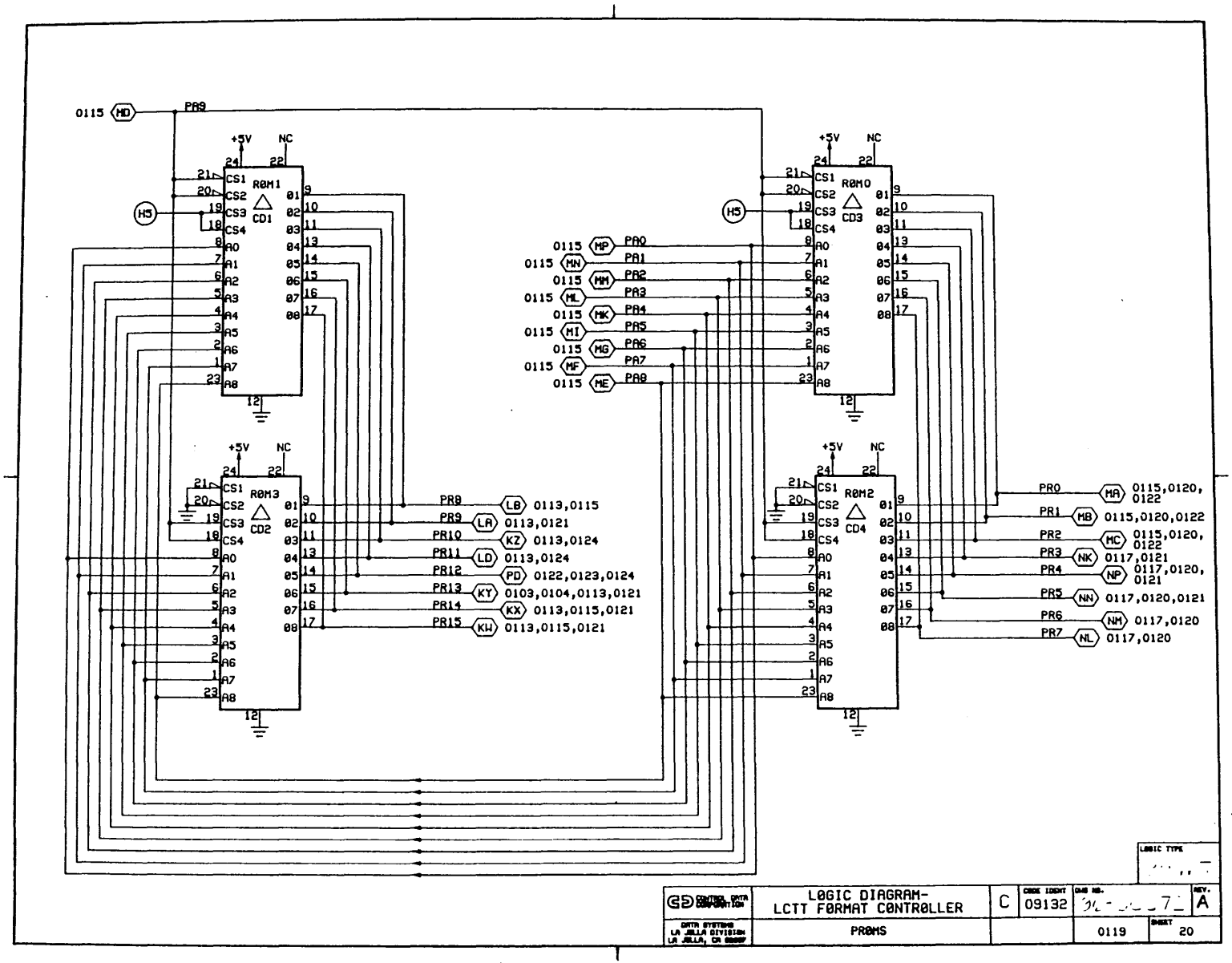


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 20 of 28)

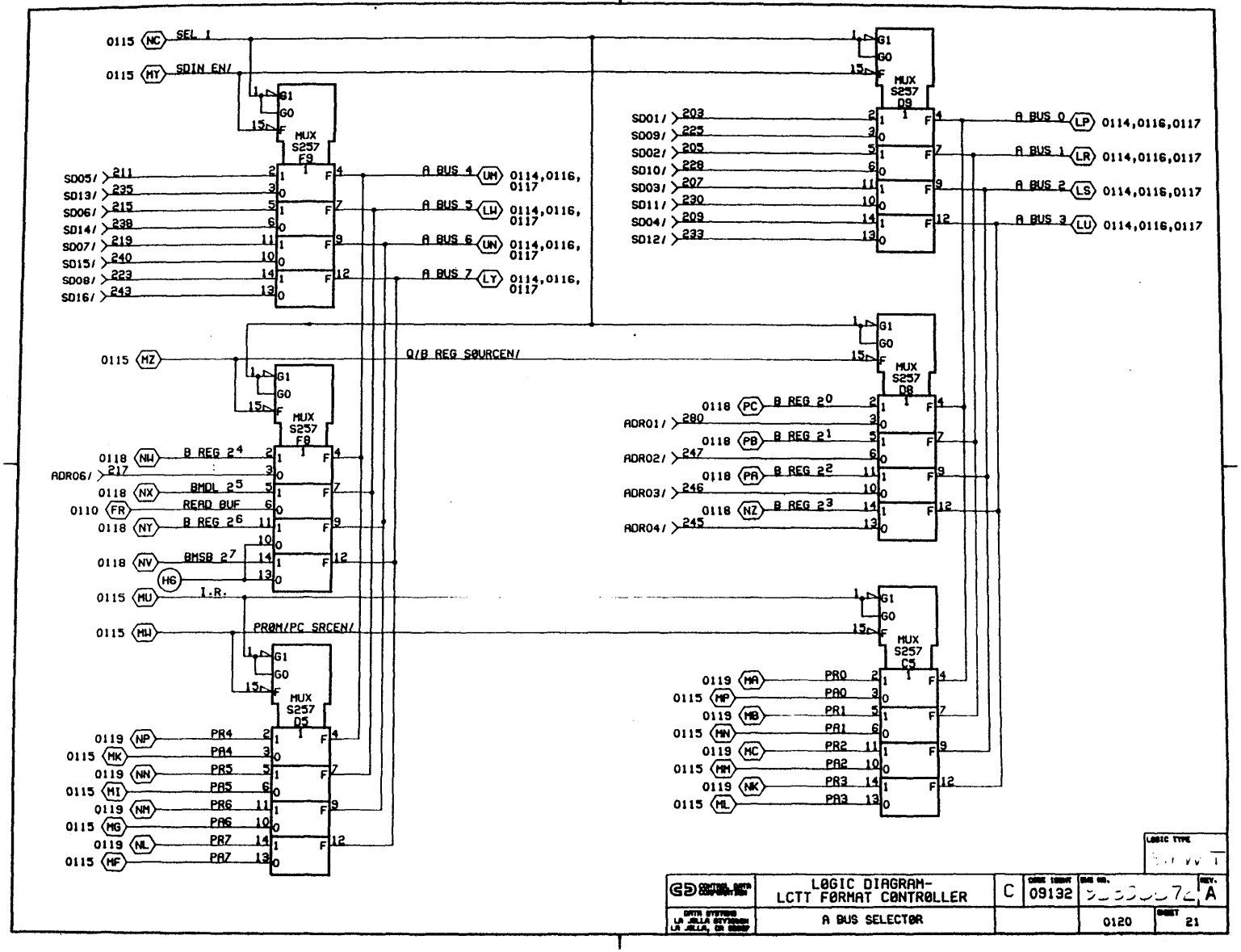


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 21 of 28)

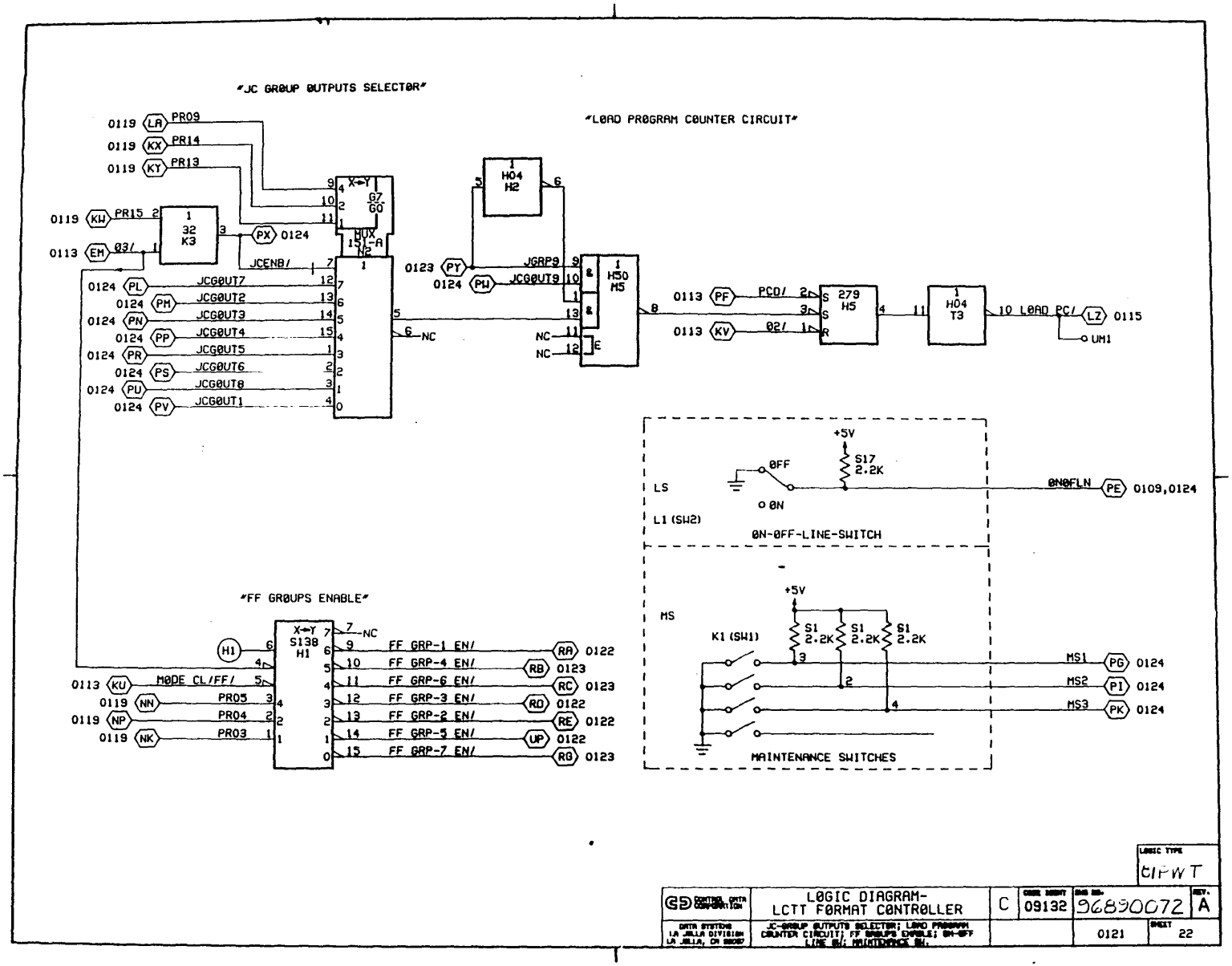


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 22 of 28)

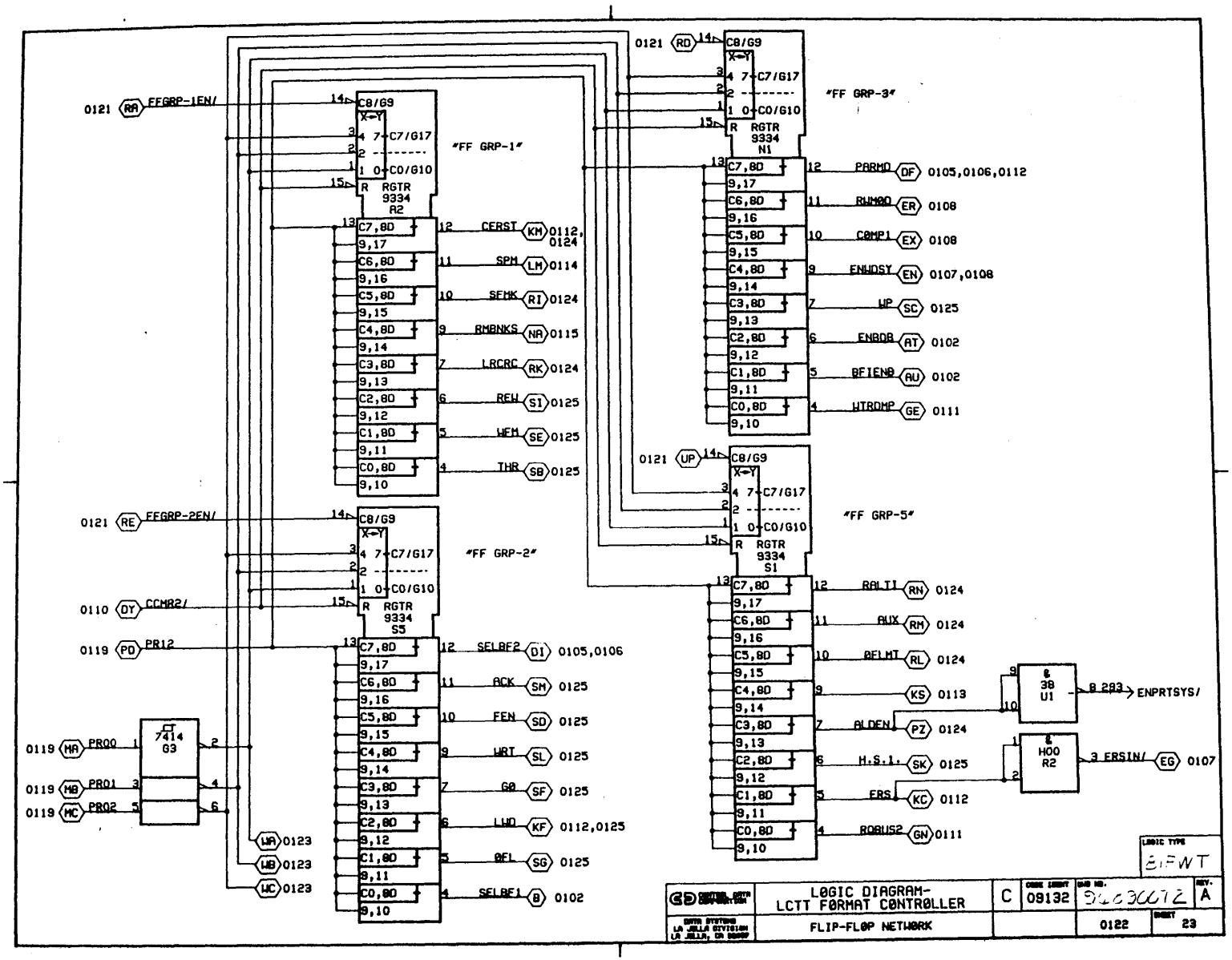


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 23 of 28)

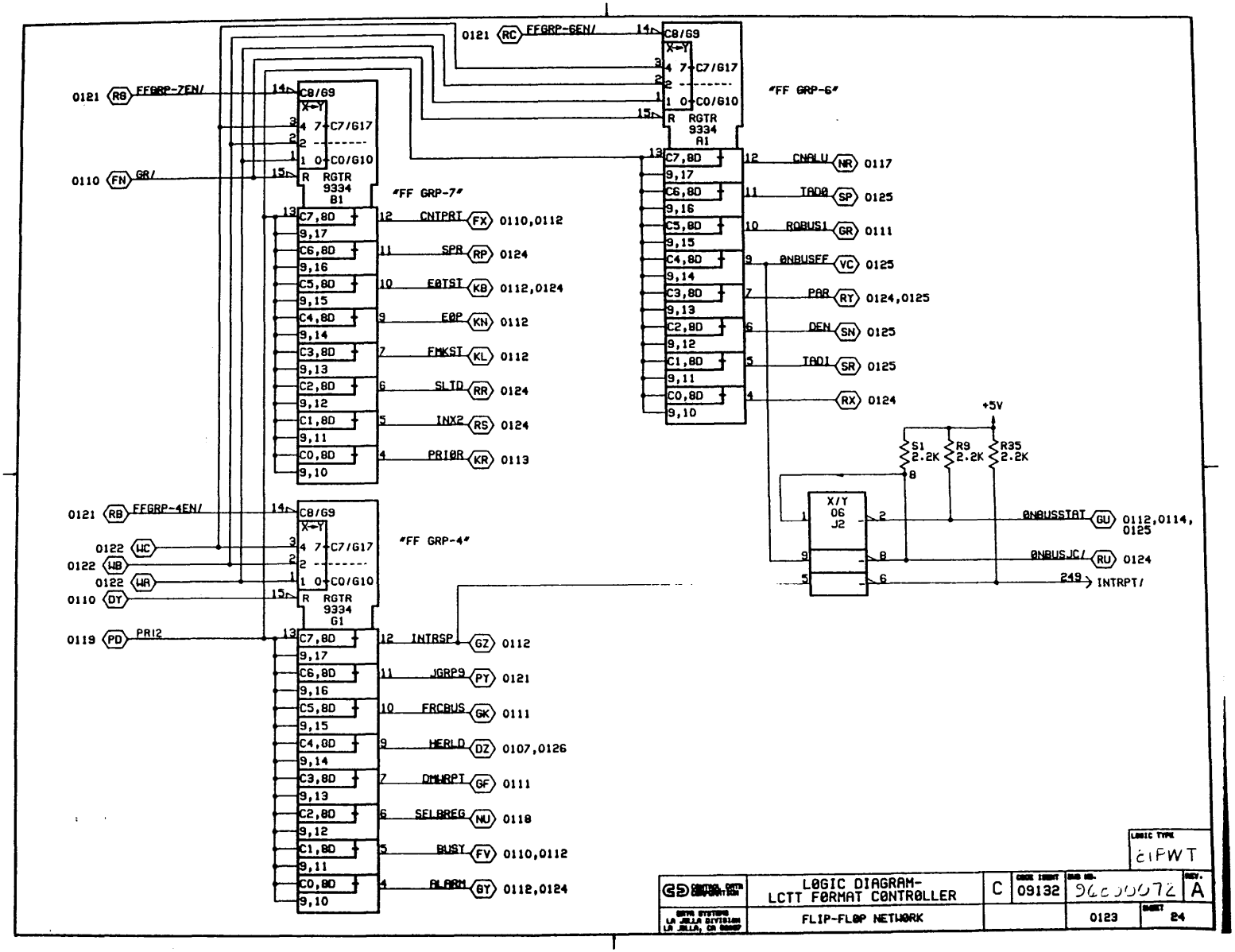


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 24 of 28)

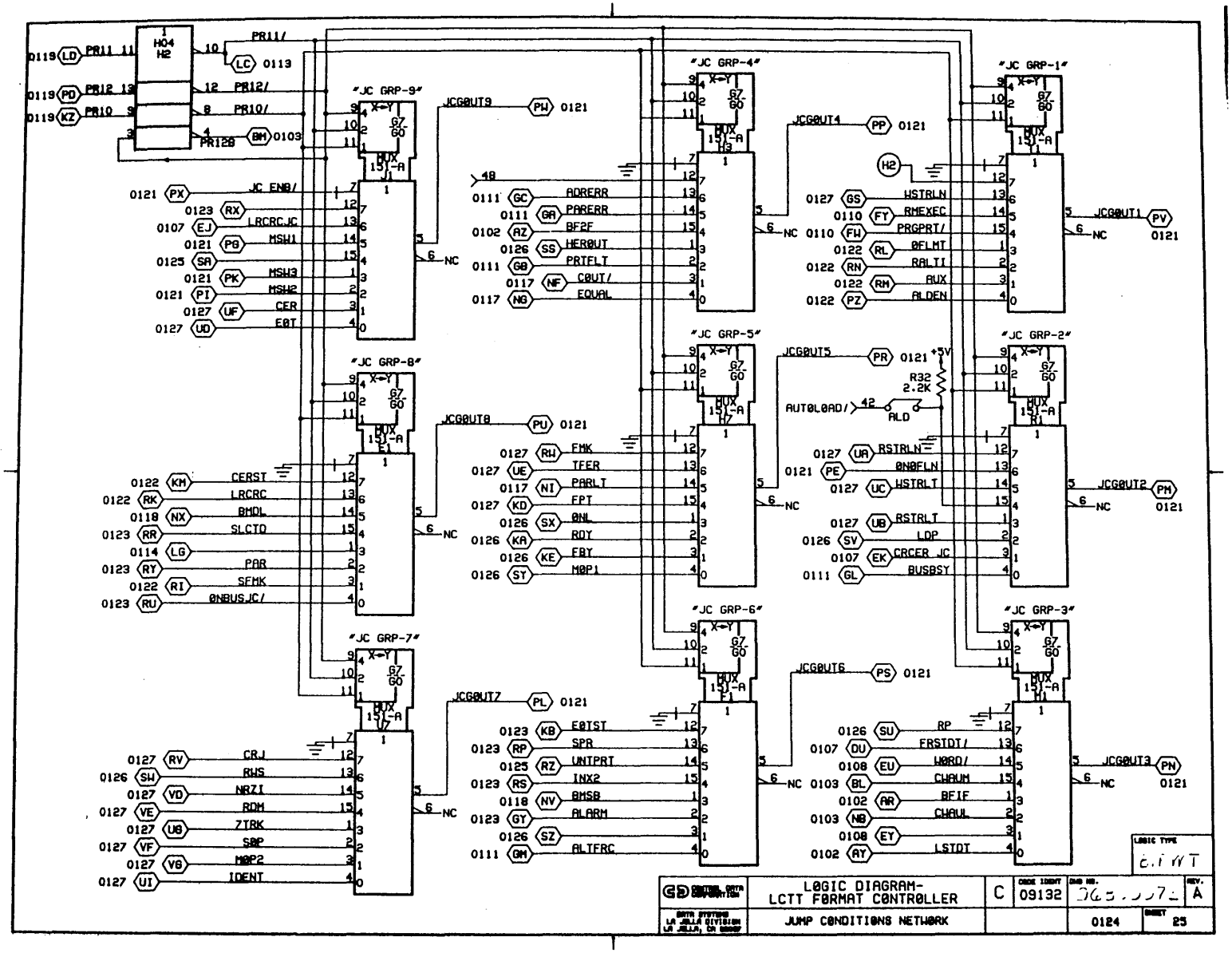


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 25 of 28)

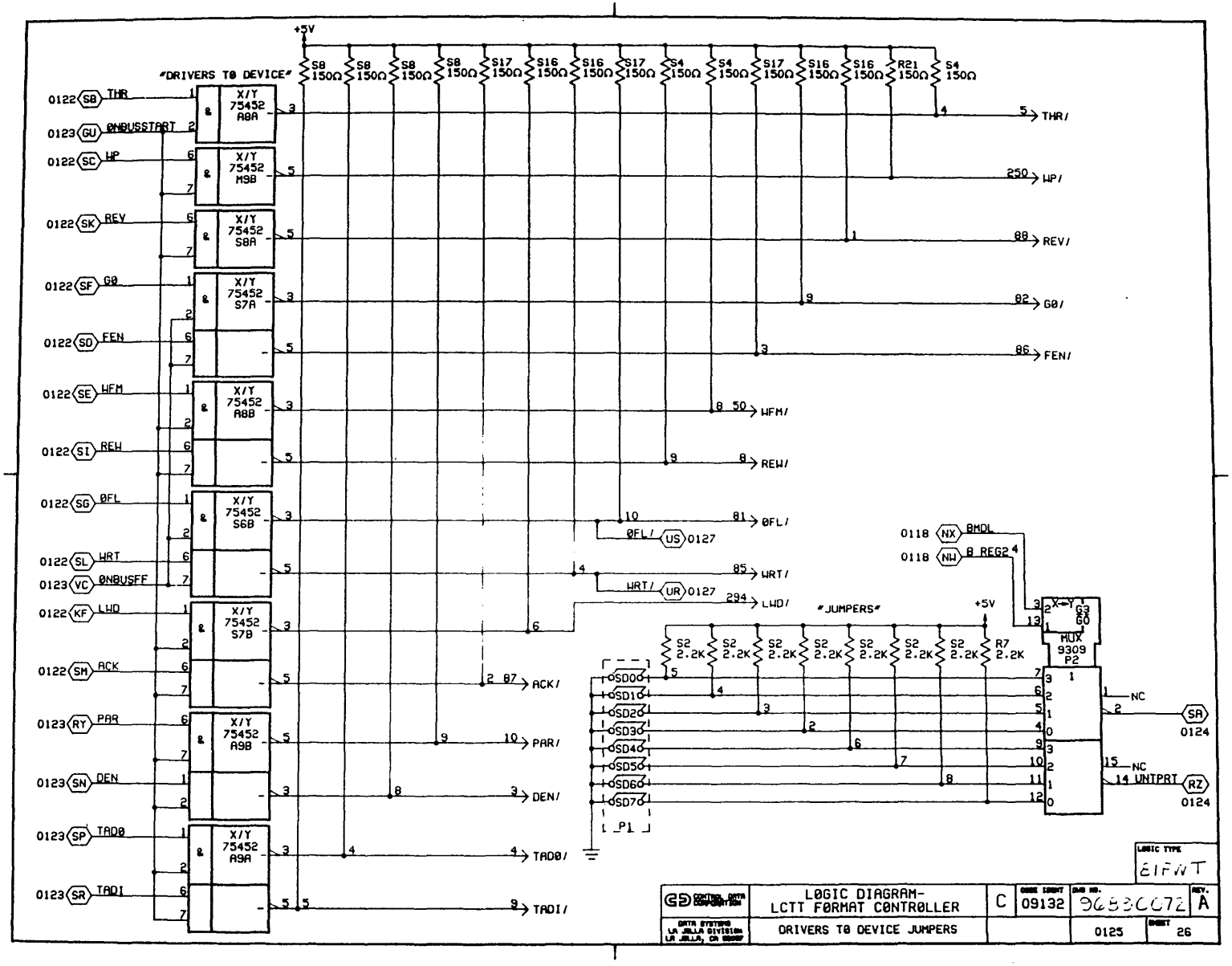


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 26 of 28)

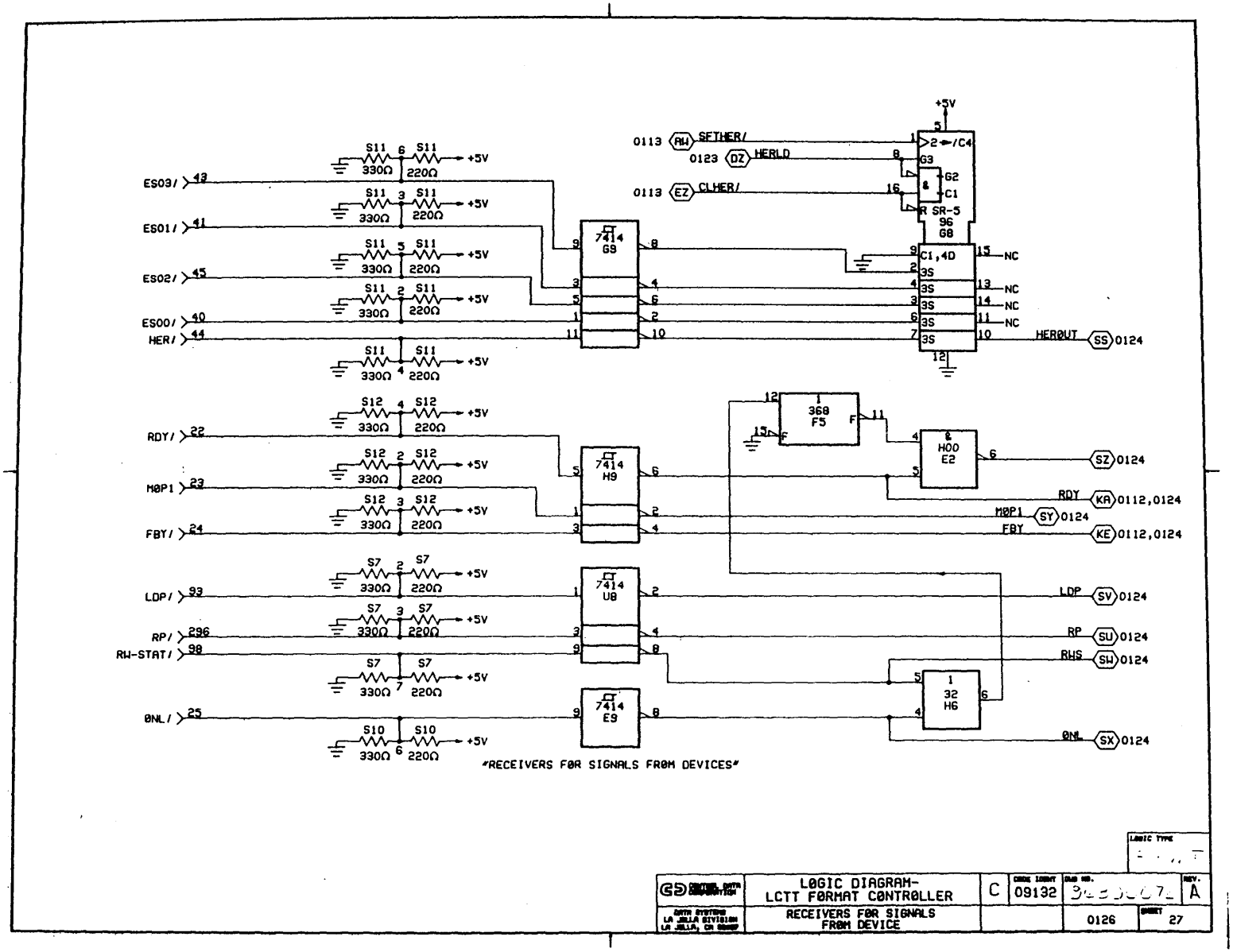


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 27 of 28)

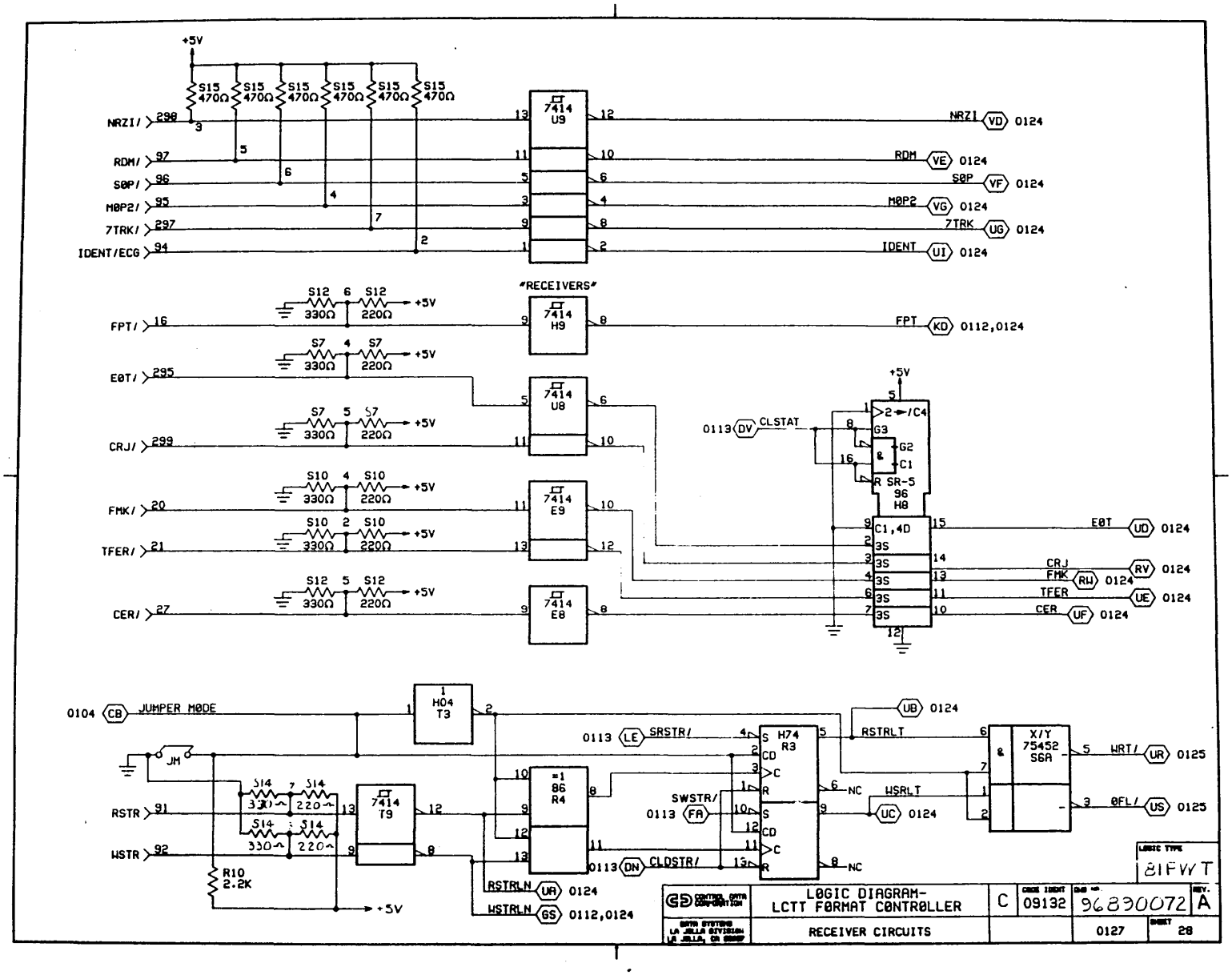


Figure 5-4. Magnetic Tape Transport Controller Logic Diagram (Sheet 28 of 28)

MAINTENANCE 6

MAINTENANCE PHILOSOPHY

The maintenance philosophy for the MTTC is to use diagnostics to determine if the controller is defective. The necessity for operator intervention, through the operators panel, is kept to a minimum.

The defective module should be replaced in the field and taken to a depot for repair.

OPERATING ADJUSTMENTS

No operating adjustments are required, except for the initial setting of the manual control jumpers. (Refer to section 2.)

PREVENTIVE MAINTENANCE

Preventive maintenance is limited to running diagnostics.

VOLTAGE MARGINS

The MTTC can operate with a ±5 percent voltage variation from nominal voltages.

A/Q-DMA SLOT PIN ASSIGNMENTS

Table 6-1 shows the A/Q-DMA pin assignments.

TABLE 6-1. A/Q-DMA SLOT PIN ASSIGNMENTS

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5VDC	21	TFER/	41	ESO1/	61	DMA-MAB09/
2	+5VDC	22	RDY/	42	AUTOLOAD/	62	DMA-MAB10/
3	DEN/	23	MOP1/	43	ESO3/	63	DMA-WRITE
4	TADO/	24	FBY/	44	HER/	64	DMA-DTM01/
5	THR/	25	ONL/	45	ESO2/	65	DMA-DTM02/
6	GND	26	GND	46	MR/	66	DMA-DTM03/
7	SPM/	27	CER/	47	CHARINPUT/ †	67	DMA-DTM04/
8	REW/	28	R1/	48	STERM/ †	68	DMA-DTM05/
9	TADI/	29	RO/	49	ERS/	69	DMA-DTM06/
10	PAR/	30	R3/	50	WFM/	70	DMA-DTM07/
11	WO/	31	R6/	51	-12VDC †	71	DMA-DTM08/
12	W6/	32	GND	52	+12VDC †	72	DMA-DTM09/
13	W2/	33	R4/	53	DMA-MAB01/	73	DMA-DTM10/
14	W5/	34	R7/	54	DMA-MAB02/	74	DMA-DTM11/
15	W4/	35	DMA-MAB17/	55	DMA-MAB03/	75	DMA-DTM12/
16	FPT/	36	DMA-MAB18/	56	DMA-MAB04/	76	DMA-DTM13/
17	W1/	37	R2/	57	DMA-MAB05/	77	DMA-DTM14/
18	W7/	38	R5/	58	DMA-MAB06/	78	DMA-DTM15/
19	W3/	39	SLOW-DMA	59	DMA-MAB07/	79	DMA-DTM16/
20	FMK/	40	ESO0/	60	DMA-MAB08/	80	ALT FORCE †

† These signals are not used by the controller and they may or may not be pre-wired on the processor backplane.

TABLE 6-1. A/Q-DMA SLOT PIN ASSIGNMENTS (Contd)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
81	OFL/	210	RD04/	241	RD15/	272	DFM09
82	GO/	211	SD05/	242	FORCE BUS	273	DFM10
83	GND	212	ADR05/	243	SD16/	274	DFM11
84	BUS NEED/	213	RTERM/†	244	RD16/	275	DFM12
85	WRT/	214	RD05/	245	ADR04/	276	DFM13
86	FEN/	215	SD06/	246	ADR03/	277	DFM14
87	ACK/	216	REPLY/	247	ADR02/	278	DFM15
88	REV/8	217	ADR06/	248	--	279	DFM16
89	N/A††	218	RD06/	249	INTRPT/	280	ADR01/
90	N/A††	219	SD07/	250	WP/	281	ADR08/ (Q07)
91	RSTR/	220	REJECT/	251	GND	282	ADR09/ (Q08)
92	WSTR/	221	RD07/	252	DMA-MPE/	283	ADR10/ (Q09)
93	LDP/	222	--	253	DMA-MAB11/	284	ADR11/ (Q10)
94	IDENT/ECG	223	SD08/	254	DMA-MAB12/	285	--
95	MOP2/	224	RD08/	255	DMA-MAB13/	286	--
96	SOP/	225	SD09/	256	DMA-MAB14/	287	--
97	RDM/	226	RD09/	257	DMA-MAB15/	288	--
98	RW-STAT/	227	PRIORITY/	258	DMA-MAB16/	289	--
99	BUS BUSY/†	228	SD10/	259	DMA-MCTM†	290	WRITE/
100	--	229	RD10/	260	DMA-MR/	291	PROGPROT/
101	GND	230	SD11/	261	DMAx-RA/	292	WEO/
102	GND	231	RD11/	262	DMA-MDS/	293	ENPRTSYS/
201	+5VDC	232	GND	263	DMA-MAE	294	LWD
202	+5VDC	233	SD12/	264	DFM01	295	EOT/
203	SD01/	234	RD12/	265	DFM02	296	RP/
204	RD01/	235	SD13/	266	DFM03	297	FTRK
205	SD02/	236	RD13/	267	DFM04	298	NRZI/
206	RD02/	237	--	268	DFM05	299	CRJ/
207	SD03/	238	SD14/	269	DFM06	300	--
208	RD03/	239	RD14/	270	DFM07	301	GND
209	SD04/	240	SD15/	271	DFM08	302	GND

†These signals are not used by the controller and they may or may not be pre-wired on the processor backplane.

††These pins are not used specifically by the MTTC. They are, however, used by the controller logic circuits. Therefore these pins must be free (not wired).

PARTS DATA 7

This section contains the parts lists and terminal connections for the MTTC and associated cable.

The assembly diagrams in this section reflect the FA464 and both versions of the FA465 MTTCs unless specifically stated otherwise.

ITD

DSN		TITLE	SPL - FA465-B LCTT/FORMATTER CONTROLLER	PREFIX: SP
CHKD				DOCUMENT NO.: 96721470
ENG				REV.: B
MFG		DATA SYSTEMS DIVISION	FIRST USED ON: FA465-B	SHEET: 1 OF 2
APPR		CODE IDENT 89132		

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS 19194	CL A. RELEASED		9-26-79		AW
B	DS22178	SEE ECO		6-29-82	A.S.	AW

NOTES: AA6030 TD

DETACHED LISTS

AA3100 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

Sh 2

ASSEMBLY NUMBER	REV	CC	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96721470	B	A	SPL-FA465-4 LCTT FORMTR CNTRLR	DSM	FA465B	09/22/79	022178	06/25/82	1/ 1 MF

FIND NUMBER	CHG CD	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	NAME/DWG PART TYPE	PC NO	S PEC
~~1~~	~~A~~	~~88951465~~	~~1.00~~	~~PC~~	~~PWA-LCTT/FORMATTER CNTRL PNLT~~	OUT	022178	080182	AYM4		N
2	A	96721485	1.00	PC	CABLE ASSY-LCTT/FORMATTER CONT	IN					N
1	A	96890071	1.00	PC	PWA-LCTT/FORMATTER CNTRL MIPWT	IN	022178	080182			N

NUMBER OF LINE ITEMS = 3
HIGHEST FIND NUMBER = 2

SCMD MFG INFO INTERDIVISIONAL DOCUMENT

Figure 7-1. FA465-B Magnetic Tape Transport Controller Spare Parts List

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS19373	CL. A. RELEASED		6-7-82		AW

1. IDENTIFY WITH TAG, LABEL, OR SIMILAR METHOD.

NOTES: UNLESS OTHERWISE SPECIFIED.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DWN		3/29/82
CHKD		3-16-82
ENG		3/24/82
MFG		3/31/82
APP		6-7-82

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA. 92037

TITLE *LCTT/FORMATTER CONTROLLER*

FA465-B | CODE IDENT 09132 | A | DWG No 96890079

SCALE | 96721469 | SHEET 1 OF 2

CONTROL DATA CORPORATION ASSEMBLY PARTS LIST

Sh 2

ASSEMBLY NUMBER	REV	CL		ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96890079	A	A	A	LCTT/FORMATTER CONTROLLER	DS	FA465B	06/02/82		06/02/82	1 MF

FIND NUMBER		PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE			
1	A	96721485	1.00	PC	CABLE ASSY-LCTT/FORMATTER CONT	IN					M
2	A	96890071	1.00	PC	PWA-LCTT/FORMATTER CNTRL BIRMT	IN					N

NUMBER OF LINE ITEMS = 2
HIGHEST FIND NUMBER = 2

SCMD MFG INFO

PRINTED IN U.S.A.

Figure 7-2. Magnetic Tape Transport Controller, Assembly Parts List

TAB		
PART NO.	LENGTH	TOL.±
96721485	258 IN.	6 IN.
96721486		
96721487		
96721488		
96721489		

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS19197	[illegible]	TWH	7-26-79	[illegible]	AM
B	DS22022	SEE ECO	RJR	12-15-80	[illegible]	MW

TABLE I (10)	
NOMINAL DIMENSION TOL TABLE	
DIM (INCHES)	TOL (INCHES)
0.5 TO 5.99	-0 +0.5
6.0 THRU 12.99	-0 +1.0
13.0 THRU 48.99	-0 +2.0
49.0 THRU 96.99	-0 +4.0
97.0 & UP	-0 +5.0

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DWN	[illegible]	7-30-79
CHKD	[illegible]	9-7-79
ENG	[illegible]	9-7-79
MFG	[illegible]	9-7-79
APP	[illegible]	9-26-79

CD DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037

TITLE CABLE ASSY- LCTT/FORMATTER CONTROLLER

CODE IDENT 09132 | A | DWG No 96721485/89

SCALE | SHEET 1 OF 14

AAL030

CD DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	SHEET 2	DOCUMENT NO 96721485/89	REV B

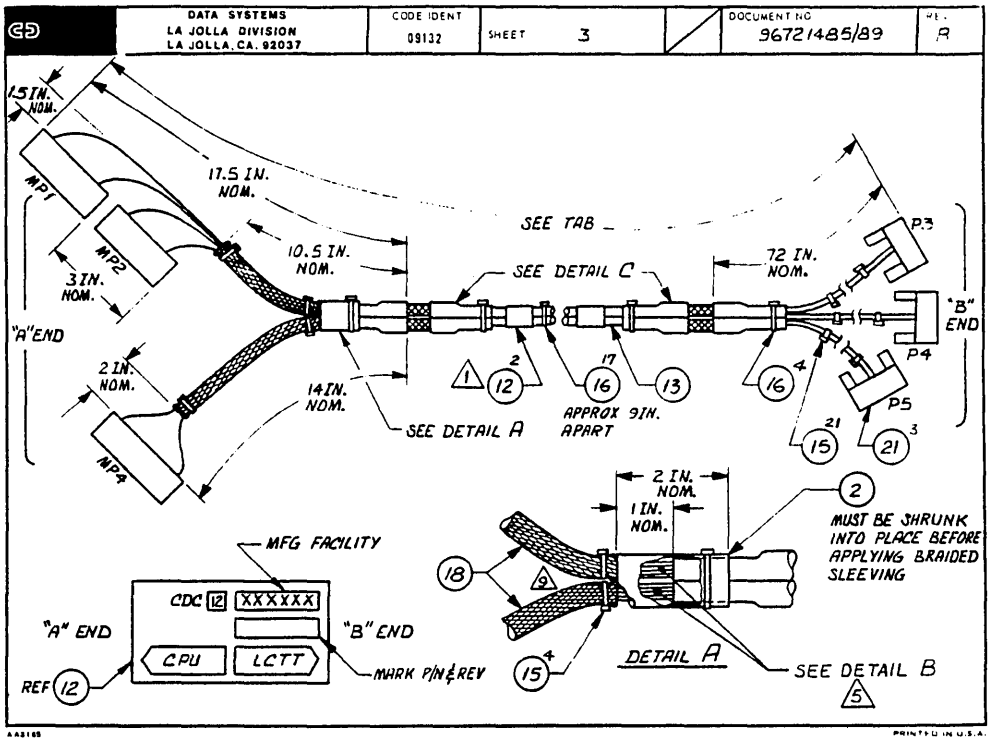
NOTES:

1. IDENTIFY CABLE PER CDC STD 1.30.008 WITH MFG FACILITY CODE.
2. INSERT PIN EXTENDER (F/N 19) INTO CONNECTOR CAVITY FOR PIN 249 AS SHOWN ON SH 5.
3. ATTACH LABELS (F/N 6,7,8,9,10 & 11) TO SIDES OF CONNECTORS AS SHOWN ON SH 5.
4. FILL ALL UNUSED CAVITIES IN "A" END CONNECTORS (F/N 21) WITH CRIMPED CONTACTS (F/N 14).
5. TERMINATE ALL GND AND UNUSED CONDUCTORS AT "A" END AS SHOWN AT SH 4 (DETAIL B). THESE TERMINATIONS CONSIST OF FIVE SOLDER CONNECTIONS LOCATED APPROX AS SHOWN. EACH SOLDER CONNECTION IS SLEEVED BY F/N 1 AND IS CONNECTED BY AN ADDED WIRE (F/N 4) TO THE PIN DESIGNATED IN THE WIRE LIST. FOR EXAMPLE, THE GND-A SOLDER CONNECTION IS WIRED TO MP1-6.
6. GND AND UNUSED WIRES AT "B" END TO BE SOLDERED TO GND STRIP AS SHOWN ON SH 6.
7. RUBBER STAMP "P" NO'S ON SIDE OF CONNECTOR AS SHOWN ON SH 6.
8. BAG (F/N 20) AND ATTACH TO CABLE.
9. FOLD END OF BRAIDED SLEEVING (F/N 18) INWARD TO FORM FISHMOUTH. FASTEN THIS END CLOSE TO SHRINK SLEEVING WITH CABLE TIE (F/N 15). THEN FORM FISHMOUTH AT OTHER END, AND STRETCH AND SMOOTH THE SLEEVING DOWN ITS ENTIRE LENGTH TOWARDS THE MP1, MP2 OR MP4 END. BEFORE TIE WRAPPING THAT END, CHECK PROPER DISTANCE OR SPACING AND ADJUST AS NECESSARY THE AMOUNT OF SLEEVING FOLDED INTO THE FISHMOUTH.
10. UNLESS OTHERWISE SPECIFIED, ALL NOMINAL DIMENSIONS COMPLY WITH TABLE I.

AA2185 PRINTED IN U.S.A.

NOTE: MTTC CABLE TERMINATION DATA IS APPLICABLE TO CABLE ASSEMBLIES 89600200, 89604657, 96720707, and 96721485.

Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 1 of 7)



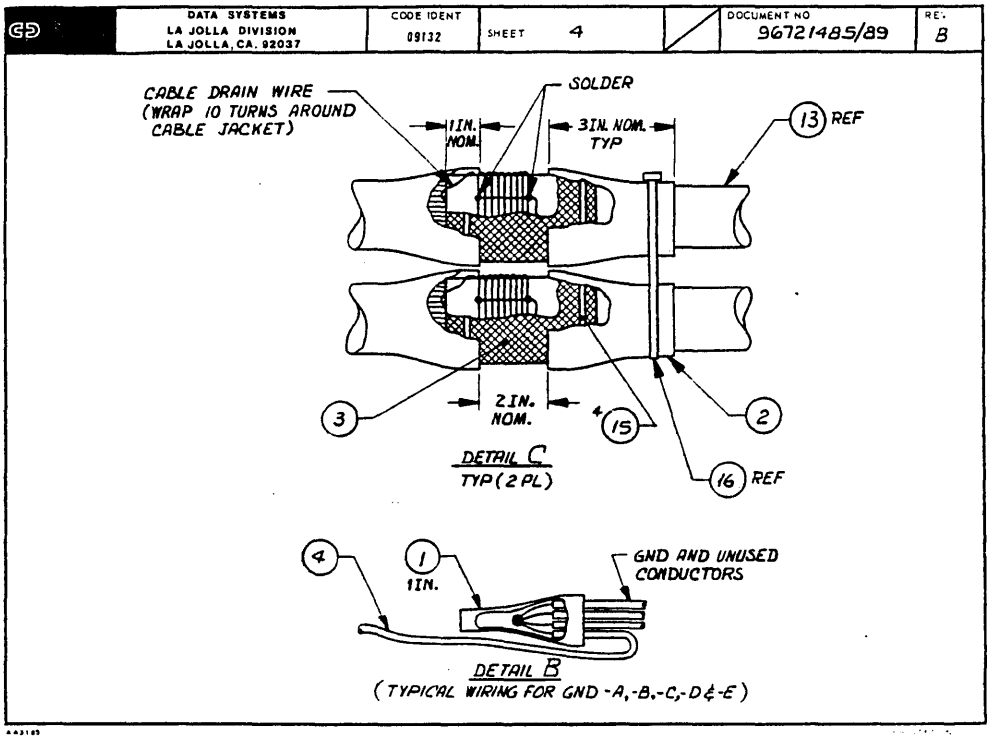
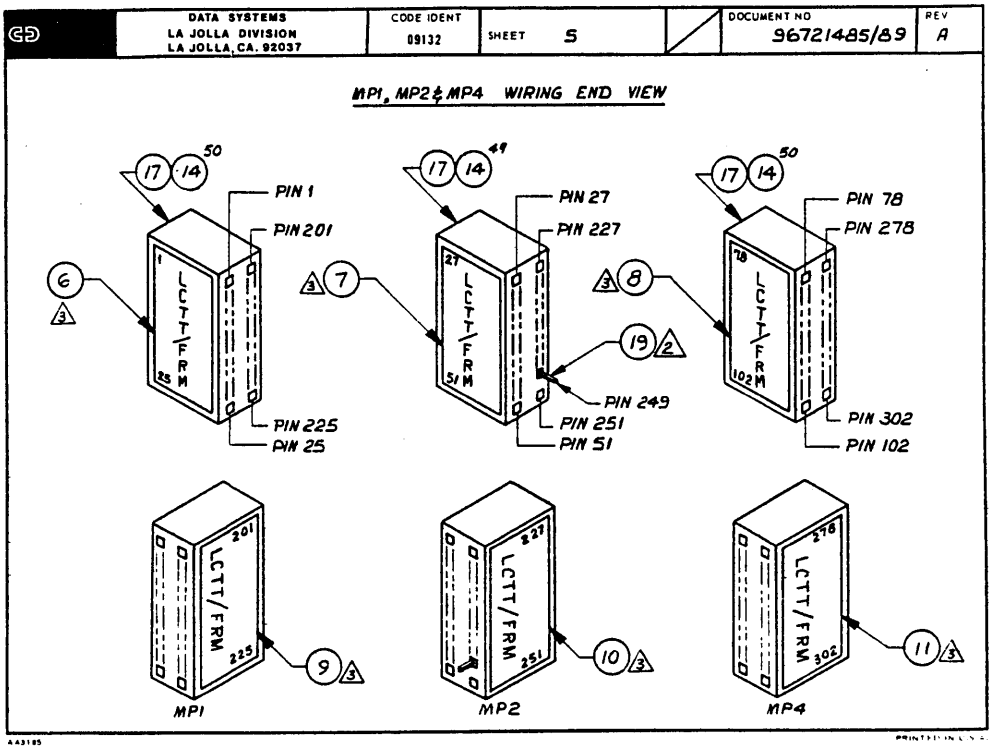


Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 2 of 7)



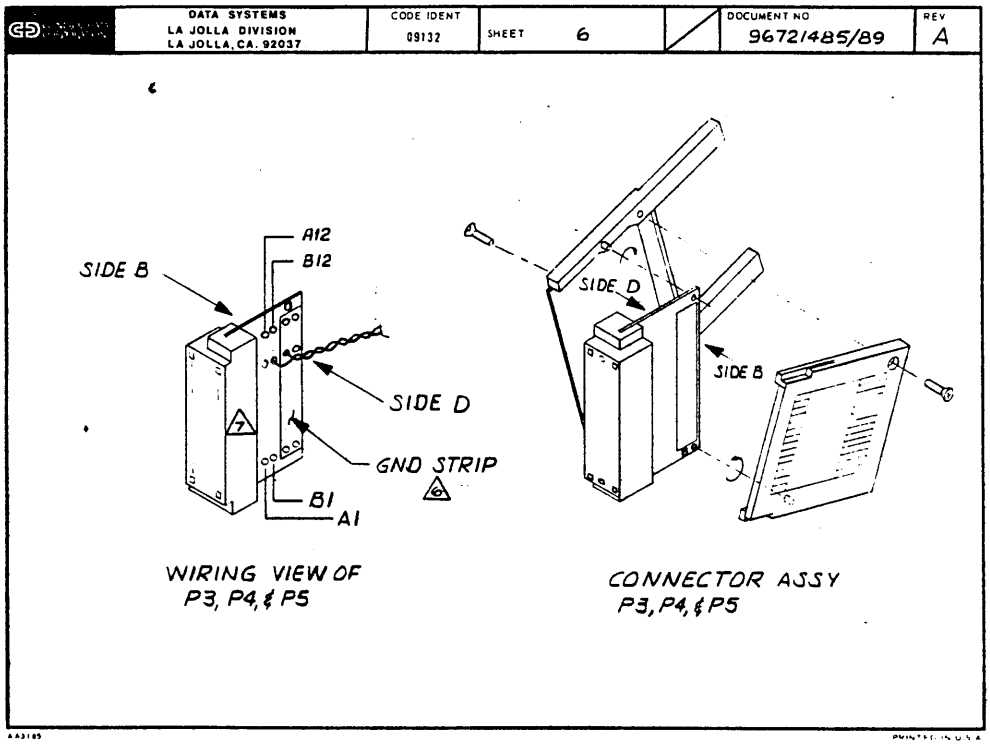


Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 3 of 7)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA,CA 92037	CODE IDENT 09132	SHEET 7	WL	DOCUMENT NO 96721485/89	REV A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
1	13	24	9	SEE TAB	P3	A1		MP2	29	14	R0
2			0			GND	6	MP2	32	5	GND-B
3			3			A2		MP2	28	14	R1
4			0			GND		MP2	32	5	GND-B
5			2			B2		MP4	87	14	ACK
6			0			GND		MP4	83	5	GND-D
7			4			A3		MP2	37	14	R2
8			0			GND		MP2	32	5	GND-B
9			1			B3		MP4	92	14	WSTR
10			0			GND		MP4	83	5	GND-D
11			6			A4		MP2	30	14	R3
12			0			GND		MP2	32	5	GND-B
13			5			B4		MP1	11	14	W0
14			0			GND		MP1	6	5	GND-A
15			7			A5		MP2	33	14	R4
16			0			GND		MP2	32	5	GND-B
17			3			B5		MP1	17	14	W1
18			9			GND		MP1	6	5	GND-A
19			2			A6		MP2	38	14	R5
20	13	24	9	SEE TAB	P3	GND		MP2	32	5	GND-B

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA,CA 92037	CODE IDENT 09132	SHEET 8	WL	DOCUMENT NO 96721485/89	REV A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
21	13	24	4	SEE TAB	P3	B6		MP1	13	14	W2
22	13	24	9	SEE TAB	P3	GND		MP1	6	5	GND-A
23	5	24	2	2"	P3	A7		P3	GND		GND STRIP P3
24											
25	13	24	1	SEE TAB	P3	B7		MP1	19	14	W3
26			9			GND		MP1	6	5	GND-A
27			6			A8		MP2	31	14	R6
28			9			GND		MP2	32	5	GND-B
29			5			B8		MP1	15	14	W4
30			9			GND		MP1	6	5	GND-A
31			7			A9		MP2	34	14	R7
32			9			GND		MP2	32	5	GND-B
33			3			B9		MP1	14	14	W5
34			6			GND		MP1	6	5	GND-A
35			2			B10		MP1	12	14	W6
36			6			GND		MP1	6	5	GND-A
37			4			A11		MP4	91	14	RSTR
38			6			GND		MP4	83	5	GND-D
39			1			B11		MP1	18	14	W7
40	13	24	6	SEE TAB	P3	GND		MP1	6	5	GND-A

Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 4 of 7)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA,CA 92037				CODE IDENT 09132	SHEET 9		WL	DOCUMENT NO 96721485/89		REV A
CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
41	13	24	5	SEE TAB	P5 B2		MP2	49	14	ERASE
42			6		GND	6	MP2	251	5	GND-C
43			7		A3		MP1	8	14	REW
44			6		GND			6	5	GND-A
45			5		B6			3	14	DEN
46			2		GND			6	5	GND-A
47			4		B4			7	14	SPM
48			2		GND		MP1	6	5	GND-A
49			1		A5		MP2	50	14	WFM
50			2		P5 GND			251	5	GND-C
51			7		P3 B12			250	14	WP
52			2		P3 GND			251	5	GND-C
53			4		P5 B9			43	14	ES3
54			5		GND			251	5	GND-C
55			3		B10			45	14	ES2
56			5		GND		MP2	251	5	GND-C
57			7		A11		MP1	9	14	TADI
58			5		GND		MP1	6	5	GND-A
59			1		B11		MP2	41	14	ES1
60	13	24	5	SEE TAB	P5 GND		MP2	251	5	GND-C

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA,CA 92037				CODE IDENT 09132	SHEET 10		WL	DOCUMENT NO 96721485/89		REV A
CONDUCTOR IDENT	FIND NO	GAUGE REF	COLOR REF	LENGTH APPROX	ORIGIN	ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
61	13	24	7	SEE TAB	P5 A12		MP1	4	14	TADO
62	13		1		GND		MP1	6	5	GND-A
63	13		3		B12		MP2	40	14	ESO
64	13		1	SEE TAB	GND		MP2	251	5	GND-C
65	5		2	2"	P5 A7		P5	GND		GND STRIP P5
66										
67	13		9	SEE TAB	P5 A1		MP4	82	14	GO
68			0		GND		MP4	83	5	GND-D
69			3		A2		MP4	88	14	REV
70			0		GND		MP4	83	5	GND-D
71			2		B3		MP1	5	14	THR
72			0		GND		MP1	6	5	GND-A
73			4		A8		MP4	86	14	FEN
74			0		GND			83	5	GND-D
75			1		A6			294	14	LWD
76			0		GND			83	5	GND-D
77			6		A4			85	14	WRT
78			0		GND			83	5	GND-D
79			5		B7			81	14	OFL
80	13	24	0	SEE TAB	P5 GND		MP4	83	5	GND-D

Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 5 of 7)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 11	WL	DOCUMENT NO 96721485/89	REV A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
81	13	24	7	SEE TAB	P5	B5		MP1	10	14	PAR
82			0		P5	GND		MP1	6	5	GND-A
83			3		P4	A1		MP4	94	14	IDENT
84			9		P4	GND	6		101	5	GND-E
85			2		P3	A12			84	14	BUS NEED
86			9		P3	GND			83	5	GND-D
87			4		P4	A2			98	14	RVS
88			9			GND			101	5	GND-E
89			1			B2			298	14	NRZ
90			9			GND		MP4	101	5	GND-E
91			6			A3		MP1	24	14	FBY
92			9			GND		MP1	6	5	GND-A
93			5			B3		MP1	20	14	FMK
94			9			GND		MP1	6	5	GND-A
95			7			A4		MP4	NC	14	DBY
96			9			GND			83	5	GND-D
97			3			B4			96	14	SOP
98			6			GND			101	5	GND-E
99			2			A5			97	14	ROM
100	13	24	6	SEE TAB	P4	GND		MP4	101	5	GND-E

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 12	WL	DOCUMENT NO 96721485/89	REV A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
101	13	24	4	SEE TAB	P4	B5		MP1	25	14	ONL
102			6		P4	GND		MP1	6	5	GND-A
103			1		P5	B1		MP4	99	14	BUS BUSY
104			6		P5	GND		MP4	101	5	GND-E
105			5		P4	B6		MP1	22	14	RDY
106			6			GND		MP1	6	5	GND-A
107			7			B7		MP4	93	14	LOP
108			6			GND			83	5	GND-D
109			5			A8			299	14	CRJ
110			2			GND			101	5	GND-E
111			4			B8			295	14	EOT
112			2			GND		MP4	101	5	GND-E
113			1			A9		MP2	44	14	HER
114			2			GND		MP2	32	5	GND-B
115			3			B9		MP4	297	14	ETR
116			2			GND		MP4	101	5	GND-E
117			7			A10		MP2	27	14	CER
118			2			GND		MP2	32	5	GND-B
119			4			B10		MP1	23	14	MOPI
120	13	24	5	SEE TAB	P4	GND		MP1	6	5	GND-A

Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 6 of 7)

GD	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	CODE IDENT 09132	SHEET 13	WL	DOCUMENT NO 9672485/89	REV A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
121	13	24	3	SEE TAB	P4	A11		MP1	21	14	TEER
122			5			GND		MP1	6	5	GND-A
123			7			B11		MP4	95	14	MOP2
124			5			GND		MP4	101	5	GND-E
125			1			B12		MP1	16	14	FPT
126	13		5	SEE TAB		GND		MP1	6	5	GND-A
127	5		2	2"	P4	A7		P4	GND		GND STRIP P4
128											
129	13		7	SEE TAB	P3	A10		MP4	296	14	RP
130			1		P3	GND		MP4	101	5	GND-E
131			3		P5	A10		MP2	242	14	FRC BUS
132			1		P5	GND		MP2	32	5	GND B
133			4		P4	A6		MP4	80	14	ALT FRC
134			1		P4	GND		MP4	101	5	GND-E
135			3		P3	GND		MP2	251		GND-C UNUSED
136			2		P4	GND		MP2	251		
137			4		P5	GND		MP2	251		
138	13	24	1	SEE TAB	P5	GND		MP2	251		GND-C UNUSED

Figure 7-3. FA465-B Magnetic Tape Transport Controller Cable Assembly (Sheet 7 of 7)

(CA-STA)

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	05/9373	CL. A. RELEASED	BB	6-7-82	B.J.	AW

CAUTION:

THIS PWA CONTAINS ELECTROSTATIC SENSITIVE DEVICES WHICH MAY BE PERMANENTLY DAMAGED BY IMPROPER HANDLING. OBSERVE HANDLING PROCEDURES OUTLINED IN CDC STD 1.60.010 & CDC ENGR SPEC 16013100 WHEN ASSEMBLING, INSTALLING, REMOVING OR TRANSPORTING THIS PWA.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DWN		3-24-82
CHKD		3-24-82
ENG		3/24/82
MFG		3/31/82
APP		6-7-82

CD DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037

TITLE PWA - 8IPWT LCTT/FORMATTER CONTROLLER

CODE IDENT 09132 | A | DWG NO 96890071

SCALE | 96890079 | SHEET 1 OF 4

AA6030

CD DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037 | 09132 | 96890071 | REV A

SHEET 2

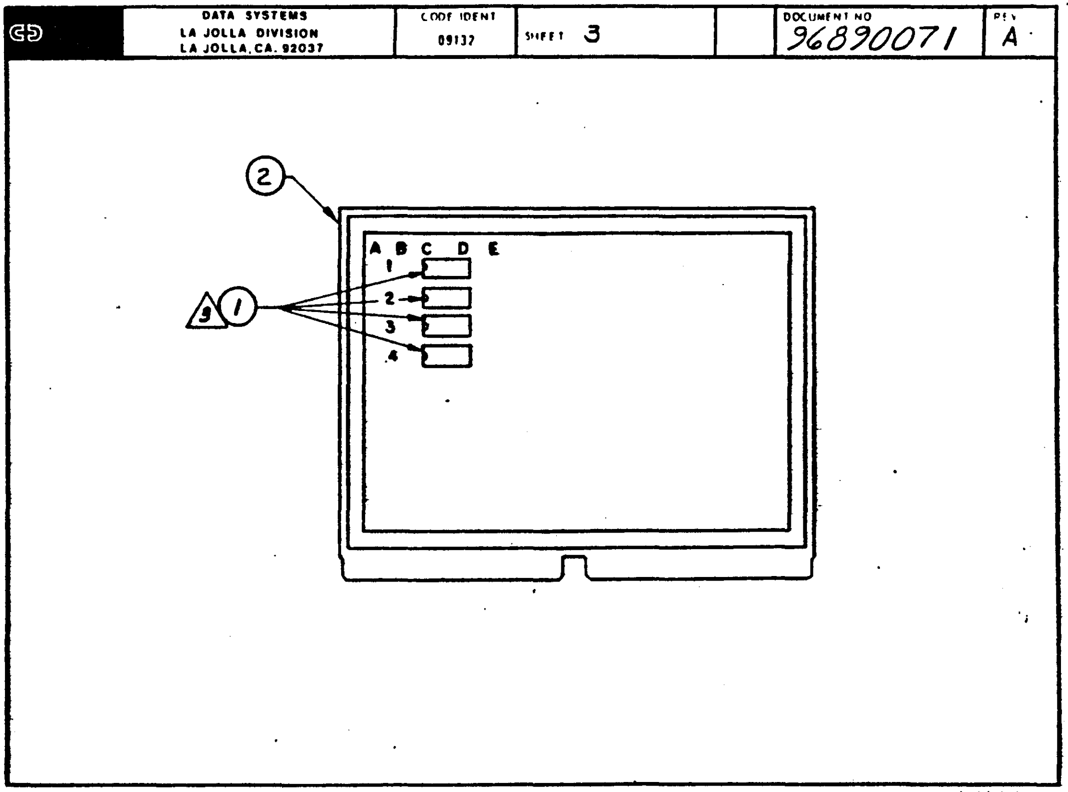
NOTES:

1. MARK PART NO. PER CDC SPEC 88818000.

3 INSTALL (F/N 1) ROM SET PER TABLE BELOW:
INSURE I.C. PIN 1 MATCHES SOCKET PIN 1

ROM SET	
PART NO.	LOCATION
96755065	CD1
96755066	CD2
96755067	CD3
96755068	CD4

Figure 7-4. Magnetic Tape Transport Controller PROM Set (Sheet 1 of 2)



CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

Sh 4

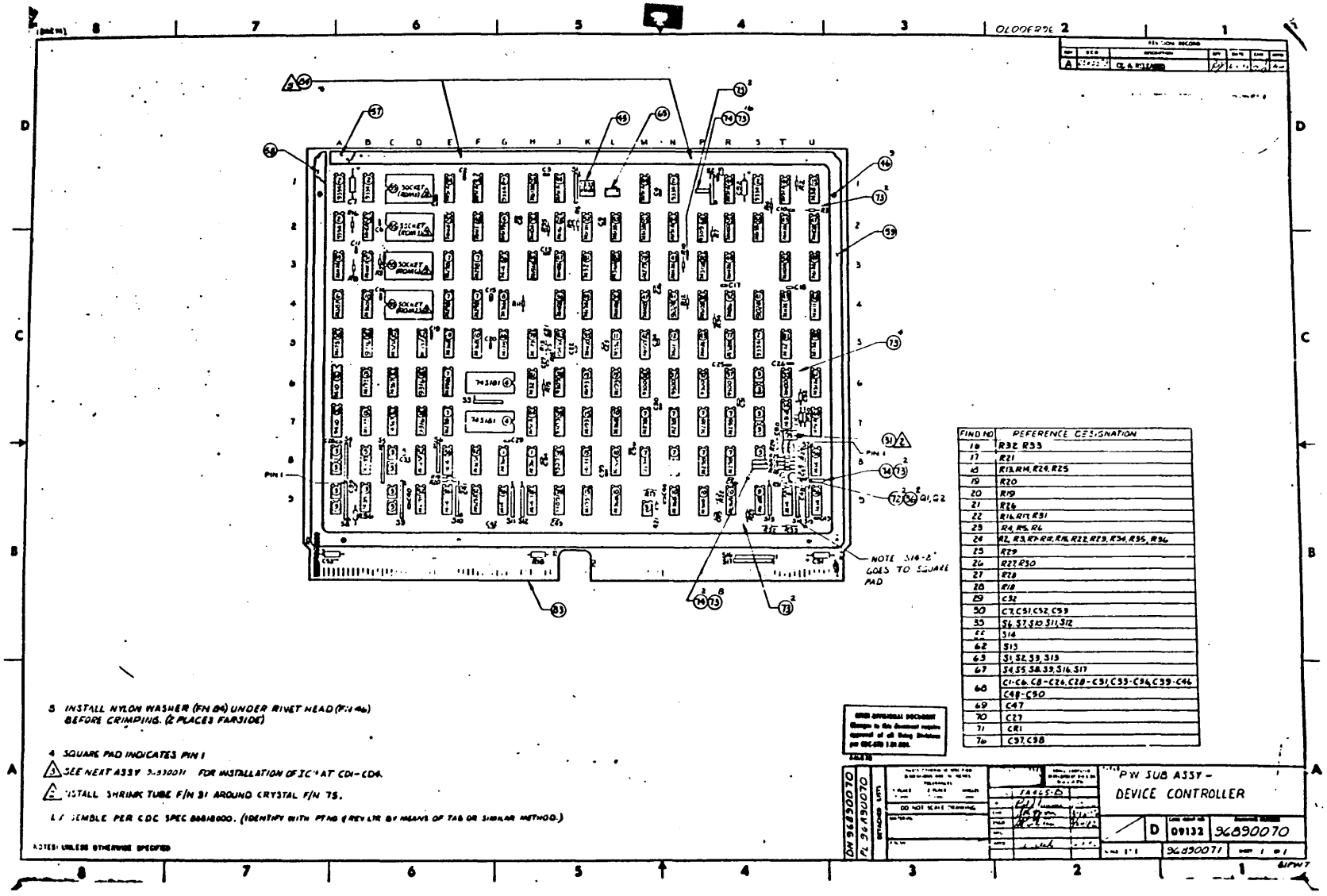
ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER	
96890071	A	A	A	PWA-LCTT/FORMATTER CNTRL HIPWT	DS	FA465B.	06/02/82		06/02/82	~~1 1~~	MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR RC	S OR N
1	A	96755063	1.00	PC	ROM SET,LCTT/FORMATTER CONTRLR	IN			AYMA		N
2	C	96890070	1.00	PC	PW SUBASSY-DEVICE CONTROLLER	IN					N
3	C	96890072	REF	PC	LOGIC-LCTT/FORM CONT 31PWT	IN					N

NUMBER OF LINE ITEMS = 3
HIGHEST FIND NUMBER = 3

SCMD MFG INFO

Figure 7-4. Magnetic Tape Transport Controller PROM Set (Sheet 2 of 2)



FIND NO	REFERENCE DESIGNATION
16	R32, R33
17	R21
18	R13, R14, R24, R25
19	R20
20	R19
21	R26
22	R15, R17, R31
23	R4, R5, R6
24	R1, R2, R7, R8, R9, R10, R22, R23, R34, R35, R36
25	R29
26	R27, R30
27	R28
28	R18
29	C32
30	C7, C51, C52, C59
35	S6, S7, S10, S11, S12
42	S14
62	S15
63	S1, S2, S3, S13
67	S4, S5, S8, S9, S16, S17
68	C1-C6, C8-C26, C28-C31, C33-C36, C39-C46, C48-C50
69	C47
70	C27
71	CR1
76	C37, C38

Figure 7-5. Magnetic Tape Transport Controller Assembly Parts List (Sheet 1 of 4)

DWN		
CHKD		
ENG		
MFG		3/3/82
QA		
		6-7-82

CONTROL DATA CORPORATION

DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA, CA 92037

TITLE: PW SUB ASSY-
DEVICE CONTROLLER

PREFIX: DN | DOCUMENT NO.: 96890070

EQUIPMENT NO.: FA465-B | SHEET 1 OF 2

FSCM NO.: 09132

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP	REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	DS/9373	CL. A. RELEASED		6-7-82							

NOTES:

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

DETACHED LISTS

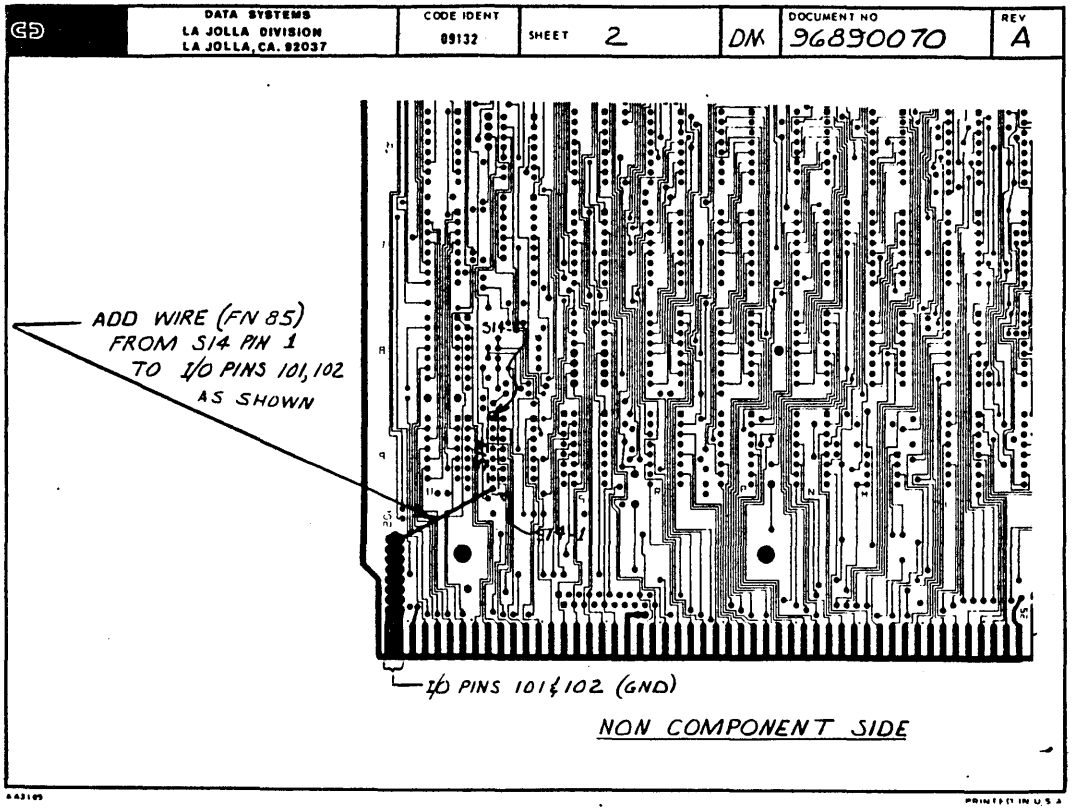


Figure 7-5. Magnetic Tape Transport Controller Assembly Parts List (Sheet 2 of 4)

ICA-7A

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

Assembly Number	Rev	CL	DW SZ	Assembly Description	Design Source	First Usage	Release Date	Change Ord. Number	Processing Date	Page Number	
96890070	A	A	D	PW SUBASSY-DEVICE CONTROLLER	DS	FA465B	06/02/82		06/02/82	1/ 3	MF

Find Number	DW SZ	Part Number	Quantity	Unit Meas.	Part Description	In/Out Status	Change Ord. Number	Date Effective	Make/Buy Part Type	PC No.	S or N
34	C	60027802	2.00	PC	WASHER, NONMETALLIC	IN			PPP1		N
1	A	15104100	2.00	PC	I.C. TTL 8 BIT SHIFT REG 7464	IN			PPP4		N
2	A	15106500	7.00	PC	IC LATCH,TTL 8-BIT 8334	IN			PPP4		N
3	A	15113001	14.00	PC	DRIVER 75452	IN			PPP4		N
5	C	15117200	2.00	PC	I-C TTL DRDR?	IN			PPP4		N
7	A	15122700	14.00	PC	IC TTL4 21 RSTR 564 DIC16	IN			PPP4		N
8	A	15124200	1.00	PC	16-BIT DUAL-IN-LINE	IN			PPP4		N
9	A	15147200	1.00	PC	IC-74LS85 TTL 4 BIT COMPARATOR	IN			PPP4		N
10	A	15154500	9.00	PC	74367/8095 HEX BUS DRIVERS	IN			PPP4		N
11	A	15154800	1.00	PC	IC 74S32	IN			PPP4		N
12	A	15155900	1.00	PC	IC-9401 CRC GENERATOR/CHECKER	IN			PPP4		N
13	A	15159300	2.00	PC	I C 7430	IN			PPP4		N
14	A	15163600	1.00	PC	IC 74S08	IN			PPP4		N
15	A	17184200	7.00	PC	INTEGRATED CIRCUIT TTL 74193	IN			PPP4		N
16	C	24500039	2.00	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
17	C	24500043	1.00	PC	RES FXD .25W 150 OHMS	IN			PPP4		N
18	C	24500045	4.00	PC	RES FXD .25W 180 OHMS	IN			PPP4		N
19	C	24500047	1.00	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
20	C	24500051	1.00	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
21	C	24500053	1.00	PC	RES FXD .25W 390 OHMS	IN			PPP4		N
22	C	24500055	3.00	PC	RES FXD .25W 470 OHMS	IN			PPP4		N
23	C	24500063	3.00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
24	C	24500071	14.00	PC	RES FXD .25W 2200 OHMS	IN			PPP4		N
25	C	24500077	1.00	PC	RES FXD .25W 3900 OHMS	IN			PPP4		N
26	C	24500081	2.00	PC	RES FXD .25W 5600 OHMS	IN			PPP4		N
27	C	24500087	1.00	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
28	C	24500139	1.00	PC	RES FXD COMP. .50W 100 OHM	IN			PPP4		N
29	C	24504342	1.00	PC	CAP FIXED SOLID TA 2.2UF,10V	IN			PPP4		N
30	C	24504353	4.00	PC	CAP FIXED SOLID TANTALUM	IN			PPP4		N
31	A	25196906	0.50	IN	INSUL SLEEVE SHRINK 3/8 CLEAR	IN			PPP3		N
33	A	36188700	4.00	PC	INT CKT 74H00 TTL QUAD 2 INPUT	IN			PPP4		N
42	A	39389000	1.00	PC	IC-TTL 74H50	IN			PPP4		N
34	B	39389400	2.00	PC	IC TTL DUAL J-K NEG EDG 74H106	IN			PPP4		N
36	A	51714600	2.00	PC	XSTR-2N2907,PNP,SI TO-18	IN			PPP4		N
37	A	51754700	4.00	PC	I.C. MST 4 BIT SHIFT REGISTER	IN			PPP4		N
38	A	51761500	3.00	PC	IC MST HEXIDECIMAL CNTR 9316	IN			PPP4		N

SCMD MFG INFO

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

Assembly Number	Rev	CL	DW SZ	Assembly Description	Design Source	First Usage	Release Date	Change Ord. Number	Processing Date	Page Number	
96890070	A	A	D	PW SUBASSY-DEVICE CONTROLLER	DS	FA465B	06/02/82		06/02/82	2/ 3	MF

Find Number	DW SZ	Part Number	Quantity	Unit Meas.	Part Description	In/Out Status	Change Ord. Number	Date Effective	Make/Buy Part Type	PC No.	S or N
39	A	51761700	5.00	PC	I.C. MST DUAL 4 INPUT MUX	IN			PPP4		N
40	A	51768200	1.00	PC	I.C. TTL DUAL LINE TRANSMITTER	IN			PPP4		N
85	C	52629940	1.50	IN	WIRE ELEC 30 GA WHITE	IN			PPP1		N
46	A	88812400	9.00	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
44	A	88881100	10.00	PC	IC 74151A TTL DATA SEL MUX	IN			PPP4		N
47	A	88881200	3.00	PC	IC 74H08 TTL QUAD 2-INPUT AND	IN			PPP4		N
48	A	88882300	2.00	PC	IC 74H11 TTL TRIPLE 3-INP AND	IN			PPP4		N
43	A	88882700	6.00	PC	IC 74H74 TTL DUAL D EDGE F/F	IN			PPP4		N
49	A	88882800	3.00	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
50	A	88882900	1.00	PC	IC 74175 TTL QUAD D F/F W/CLR	IN			PPP4		N
51	A	88883100	1.00	PC	IC 74H10 TTL TPL 3-I POS NAND	IN			PPP4		N
52	A	88883300	6.00	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
4	A	88884900	2.00	PC	IC 74S181 TTL ALU/FUNCTION GEN	IN			PPP4		N
53	A	88885100	5.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
41	A	88885400	2.00	PC	IC 9024 TTL DUAL FLIP/FLOP	IN			PPP4		N
32	A	88885700	1.00	PC	IC 7486 TTL QUAD 2-IN EXCL OR	IN			PPP4		N
54	A	88895600	3.00	PC	IC 74H04 TTL HEX INVERTER	IN			PPP4		N
56	A	88896100	8.00	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
57	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
58	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
59	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
60	A	88920200	2.00	PC	IC 74367 TTL TRI-STATE HEX BFR	IN			PPP4		N
61	A	88923100	1.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
62	A	88924704	2.00	PC	RES NETWORK-SIP,8 PIN,470 OHM	IN			PPP4		N
63	A	88924708	4.00	PC	RES NETWORK-SIP,8 PIN,2.2K OHM	IN			PPP4		N
64	A	89600296	2.00	PC	IC-9410 16X4 RAM 3 STATE REG	IN			PPP4		N
65	A	89600664	1.00	PC	SLIDE SWITCH,1 POLE 2 POSITION	IN			PPP4		N
66	A	89600667	1.00	PC	IC-74178 4 BIT PARA SHIFT REG	IN			PPP4		N
35	A	89601293	6.00	PC	RES NET-SIP,8 PIN 220/330 OHMS	IN			PPP4		N
68	A	89636154	44.00	PC	CAP, FXD CER .068 MFD	IN			PPP4		N
69	A	89636172	1.00	PC	CAP, FXD CER .47MFD 50VDCW	IN			PPP4		N
70	A	89636218	1.00	PC	CAP,FXD CER 220PF 50 VDCW	IN			PPP4		N
71	A	89636802	1.00	PC	DIODE,SILICON 75V 50MA 1N4151	IN			PPP4		N
72	A	89668200	2.00	PC	TRANSISTOR MOUNTING PAD TO-18	IN			PPP4		N
73	A	89676201	36.00	PC	CONNECTOR-SOCKET LOW PROFILE	IN			PPP4		N
74	A	89684100	4.00	PC	CONNECTOR PLUG TWO PIN JUMPER	IN			PPP4		N

SCMD MFG INFO

Figure 7-5. Magnetic Tape Transport Controller Assembly Parts List (Sheet 3 of 4)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	DOC ID	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE CONTROL NUMBER	PROCESSING DATE	PAGE NUMBER
96890070	A	A	D	PW SUBASSY-DEVICE CONTROLLER	DS	FA465B	06/02/82		06/02/82	3/ 3 MF

FIND NUMBER	REV LEVEL	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE CONTROL NUMBER	DATE EFFECTIVE	MANUFACTURER PART TYPE	PC NO	S OR M
75	A	89724302	1	PC	CRYSTAL UNIT-QUARTZ 20.0000MHZ	IN			PPP4		N
76	A	89760900	2	PC	CAP MICA 50V 47PF 5	IN			PPP4		N
77	A	89933400	1	PC	IC-74S280 9 BIT ODD/EVEN P GEN	IN			PPP4		N
55	A	94375110	1	PC	RES NETWORK, 8PIN SIP 330OHMS	IN			PPP4		N
45	A	94398002	1	PC	SWITCH,SLIDE-DIP-PCB,4 POS	IN			PPP4		N
6	A	95955700	1	PC	IC MULTIPLEXER 2IN TYPE74S157	IN					N
78	A	96744155	1	PC	IC 7406 TTL HEX INVERTER (OC)	IN			PPP4		N
79	A	96744157	2	PC	IC 74279 TTL S-R LATCH	IN			PPP4		N
80	A	96744166	2	PC	IC 74S158 TTL QUAD 2-INPUT MUX	IN			PPP4		N
81	A	96744172	3	PC	IC 7432 TTL QUAD 2-IN OR GATE	IN			PPP4		N
82	A	96745500	1	PC	IC 74S141 TTL 4-BIT BINARY CTR	IN			PPP4		N
67	A	96752425	6	PC	RESISTOR NETWORK,10 PIN SIP	IN			PPP4		N
83	D	96870220	1	PC	PWA-DEVICE CONTROLLER	IN			PPP4		N

NUMBER OF LINE ITEMS = 85
HIGHEST FIND NUMBER = 85

SCMD MFG INFO

Figure 7-5. Magnetic Tape Transport Controller Assembly Parts List (Sheet 4 of 4)

OPERATING PROCEDURES A

The following procedure may be followed to perform MTTC operations with the magnetic tape transport:

Step 1 - Mount the Tape

Mount the desired tape reel onto the desired magnetic tape transport (MTT). If writing is to be done onto the tape, a write enable ring should be inserted into the reel prior to mounting. If no writing is to be done, the write enable ring should be removed to prevent accidental erasure.

Step 2 - Connect into the Bus

1. Load Q-register bits 15 through 11 with 0, bits 10 through 7 with the proper equipment code of the MTTC, and bits 4 through 0 with the code of the bus connect command.
2. Load the A register with bit 7 = 1.
3. Execute an output instruction.

The following conditions cause a reject:

- The controller is already busy with a previous command.
- A protect fault was detected.

Step 3 - Select the Unit

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the unit select command.
2. Load A-register bit 7 with a 1, bits 4 and 5 with the code of the desired transport, and bits 15 and 13 with the desired operating conditions.
3. Execute an output instruction.

The following conditions cause a reject:

- A bus connect command was not executed prior to the unit select command.
- The bus was relinquished prior to the unit select command.
- A protect fault was detected.
- The controller is already busy with a previous command.

Step 4 - Position the Tape

With the controller on-bus and the transport selected, the tape must be positioned forward or backward until the point where the record to be read or written is under the read/write head.

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the director function command.
2. Load A register bits 0 through 3 with the desired motion.The following commands are used for tape positioning:

   Space Forward - Moves the tape forward one record to the next inter-record gap.

   Space Backward - Moves the tape backward one record to the previous inter-record gap.

   Search File Mark (Forward) - Moves the tape forward to the next file mark.

   Search File Mark (Backward) - Moves the tape backward to the previous file mark.

   Controlled Backspace - Allows the positioning of the tape back to the previous inter-record gap for a record that has just been written in error.

   Rewind - Moves the tape backwards at high speed to the beginning-of-tape (BOT) reflective marker.

   Rewind (off-line) - Same as rewind, but causes the transport to go off-line.
3. Execute an output instruction.

The following conditions cause a reject of the motion command:

- The controller is busy with a previous command.
- The transport was not selected prior to the motion command.
- A bus connect command was not executed or the bus was relinquished prior to the motion command.
- The selected transport is not ready.
- A protect fault is detected.

Steps 5 through 8 deal with reading or writing onto the tape.

Step 5 - Specify the First Word Address

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the first word address command.
2. Load the A register with the first word of data to be transferred.
3. Execute an output instruction.

Step 6 - Specify the Bank

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the bank select command.
2. Load the A register with the first word of bank in which the first word address is to be found.
3. Execute an output instruction.

Step 7 - Specify the Block Length

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the block length command.
2. Load the A register with the block length.
3. Execute an output instruction.

The following conditions cause any of the preceding commands to be rejected:

- The controller is busy with a previous command.
- A protect fault was detected.

Step 8 - Read or Write

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the director function command.
2. Load A-register bits 0 through 3 with the code of the read data or write data.
3. Execute an output instruction.

The command reject conditions for read or write operations are the same as for tape positioning commands.

Reading Status: After transferring data to or from the tape, status should be checked to determine that the transfer was successful. Proceed as follows:

1. Load Q-register bits 15 through 11 with 0s, bits 10 through 7 with the proper equipment code, and bits 4 through 0 with the code of the desired status.
2. Execute an input instruction.

Step 9 - Read Dynamic Status

Examine the contents of the A register. Bit 8 (EOP) and bit 0 (unit ready) should be set. Bit 3 (alarm) should be 0. If bit 3 is set, read alarm status to determine the cause of the alarm.

Step 10 - Read Block Length Status

Determine that the proper number of words was transferred.

Step 11 - Read Block Length Status

The A register should contain the last word address plus one.

Step 12 - Read Current Bank Status

A-register bits 0 and 1 should contain the code of the bank where the last word address plus one was found.

All status requests except Status 1 are rejected if the controller is busy.

FLOW CHARTS B

This appendix contains the flow charts for the magnetic tape transport controller. They are applicable to all FA464 and FA465 MTTCs.

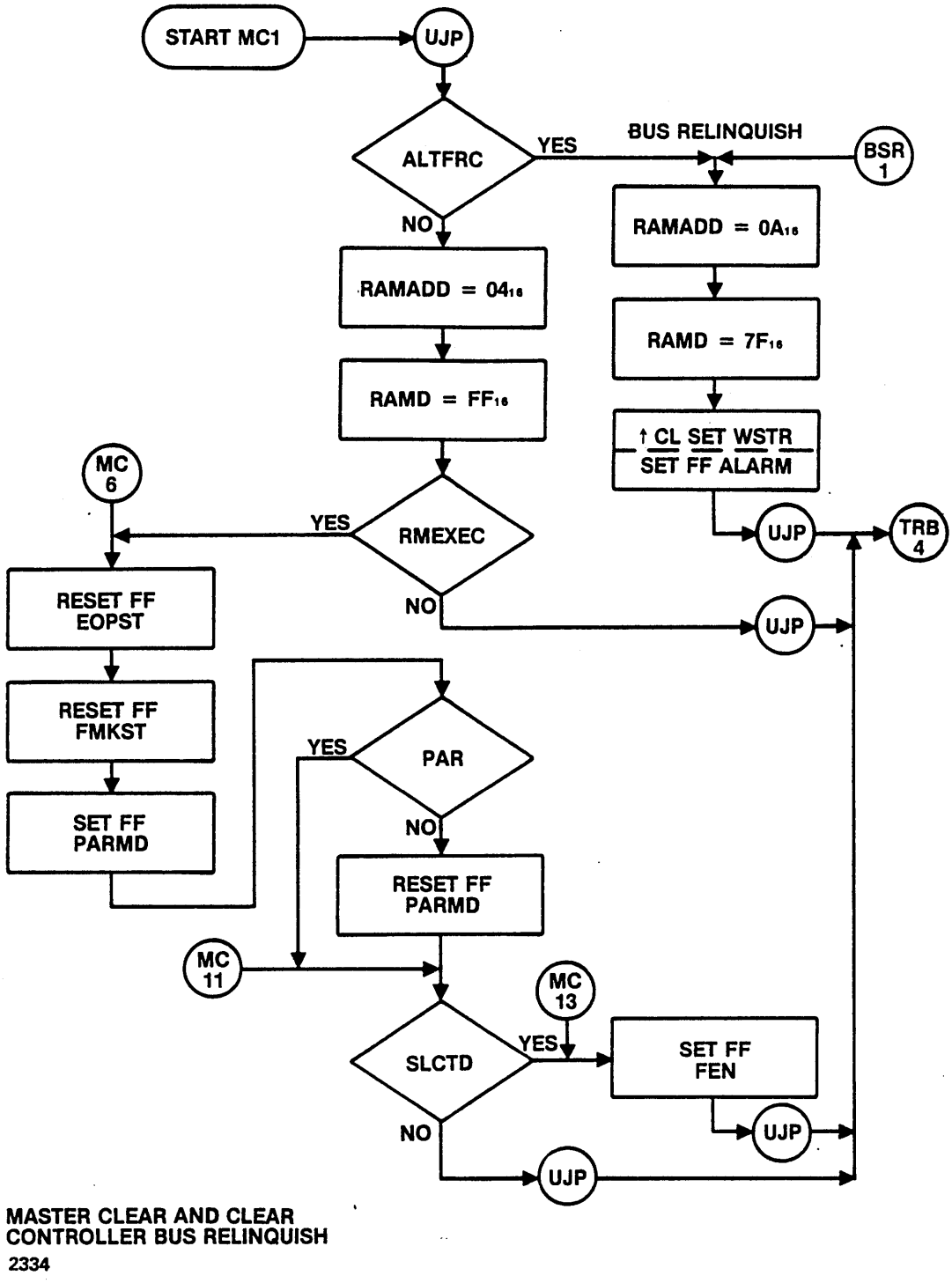


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 1 of 75)

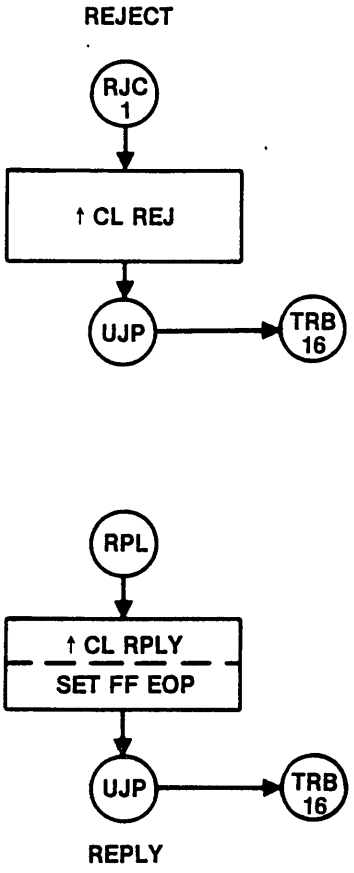
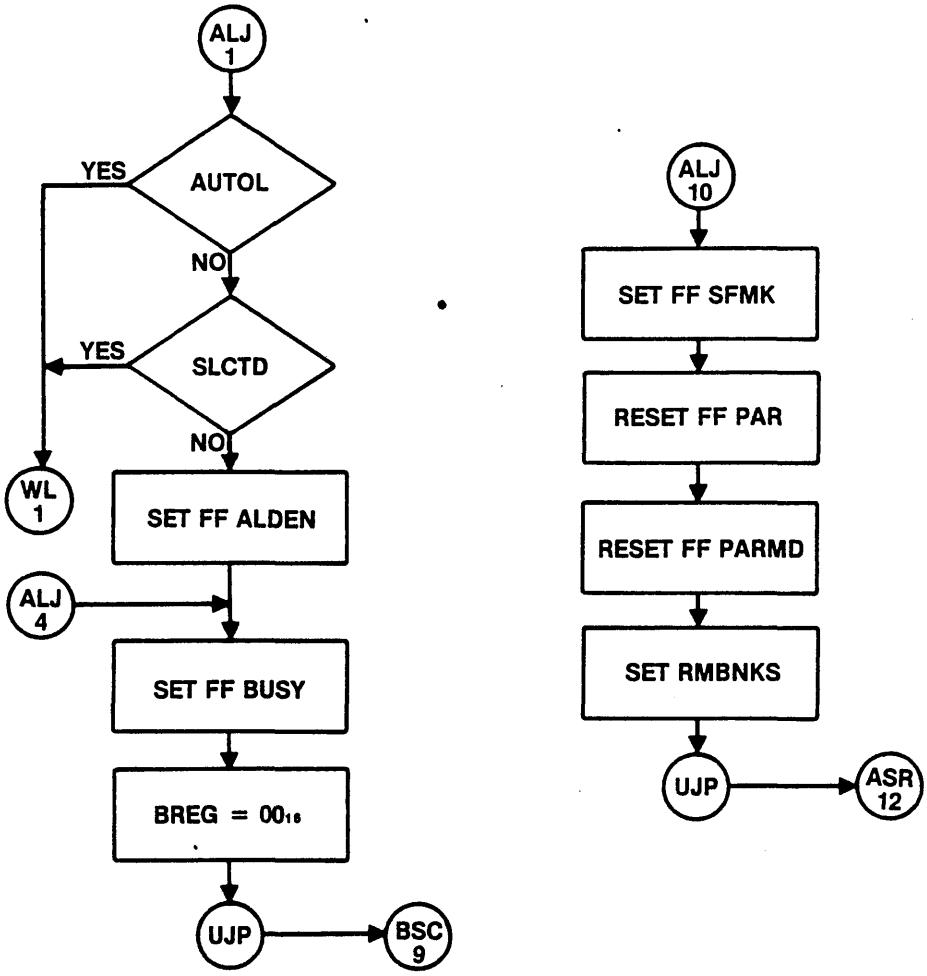


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 2 of 75)



AUTOLOAD JUMP

2336

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 3 of 75)

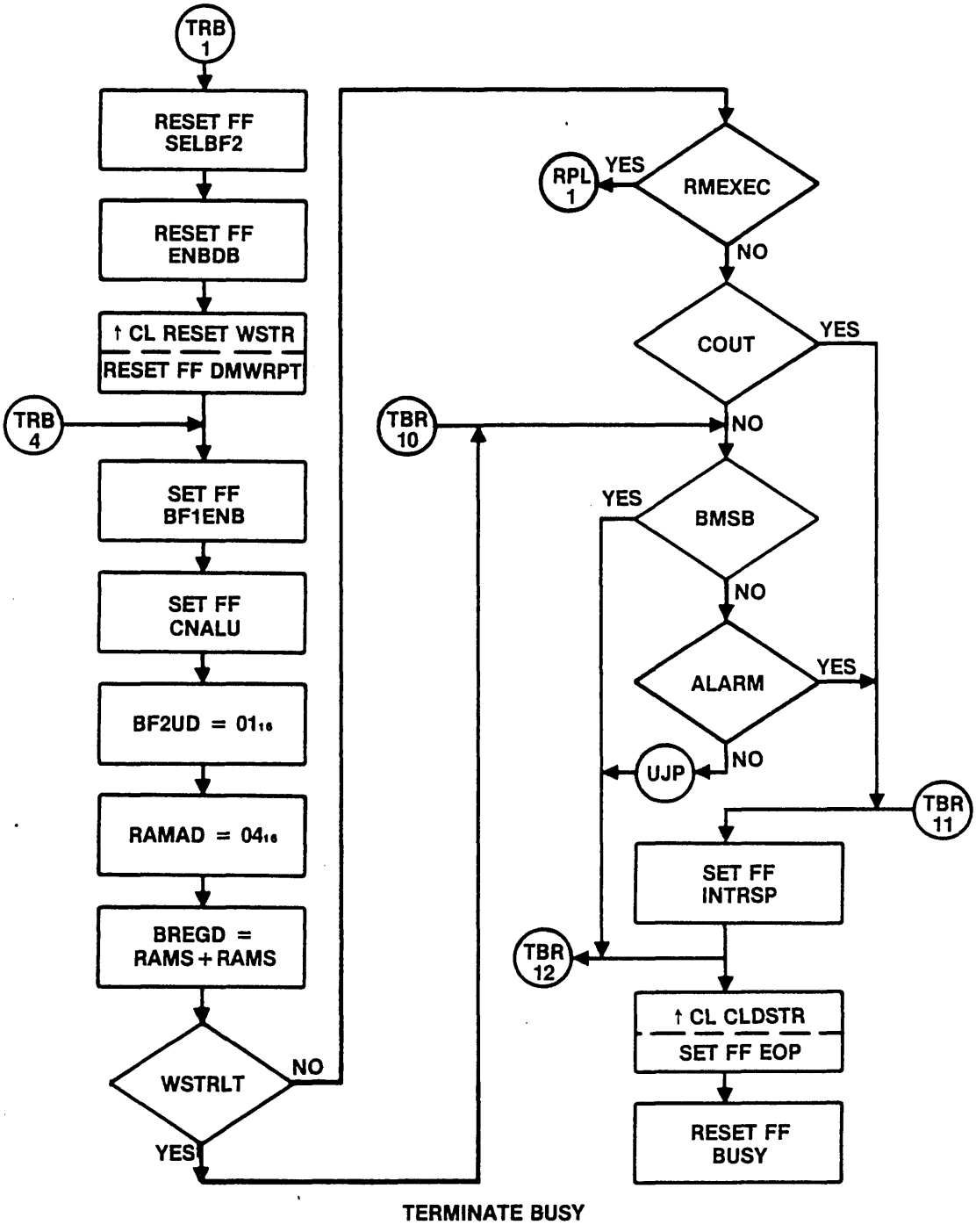
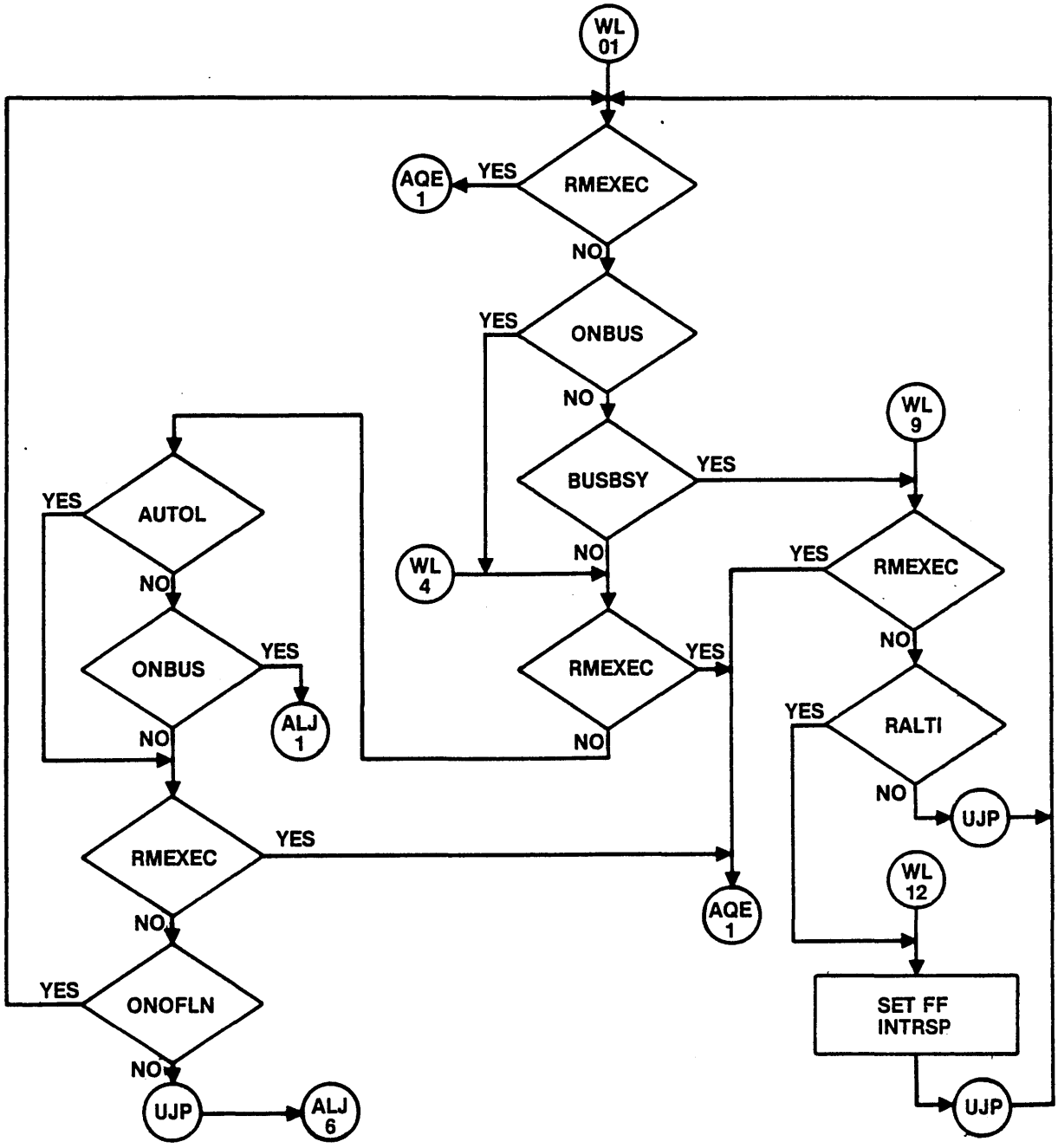


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 4 of 75)



A/Q WAITING LOOP

2337

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 5 of 75)

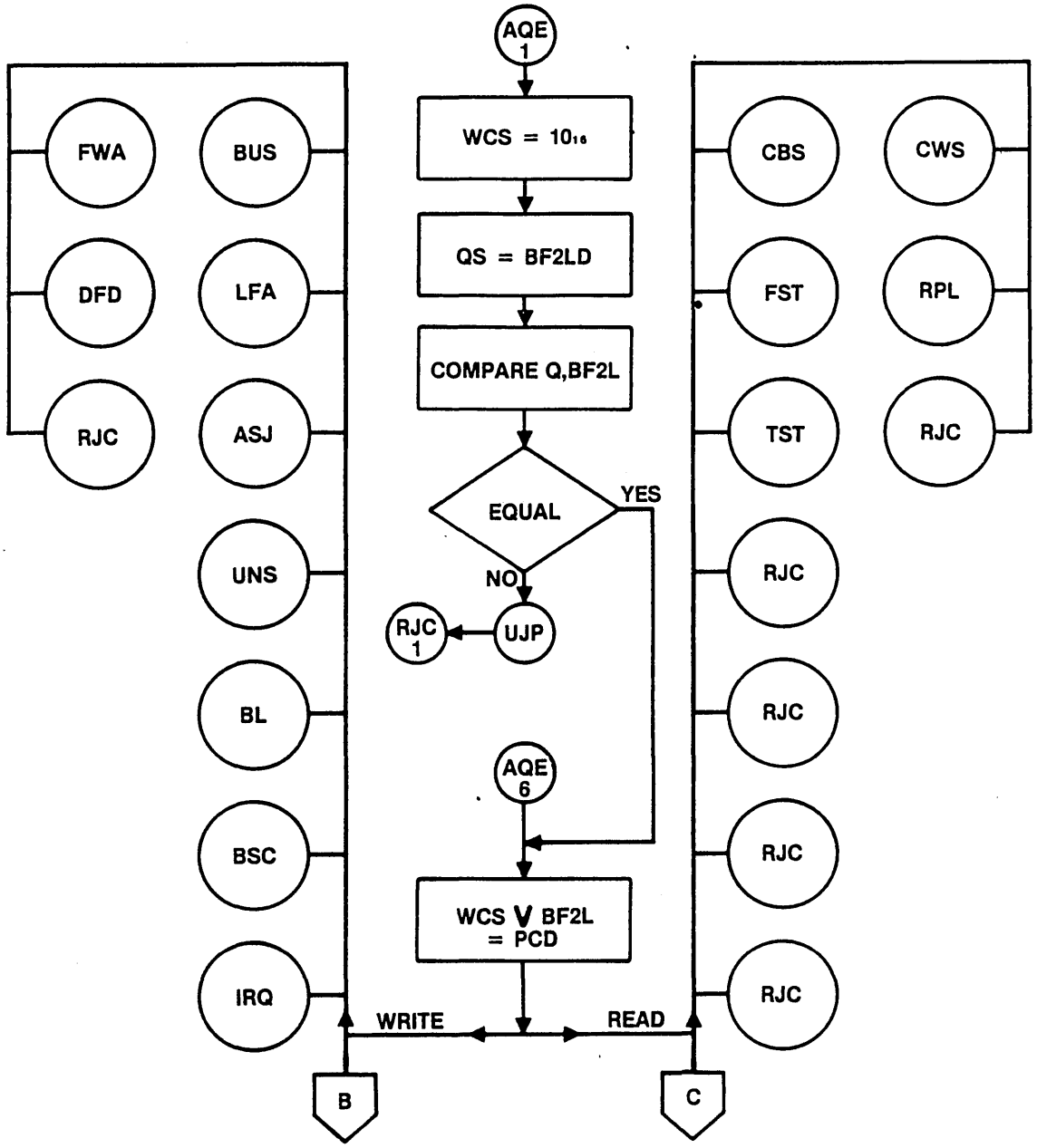
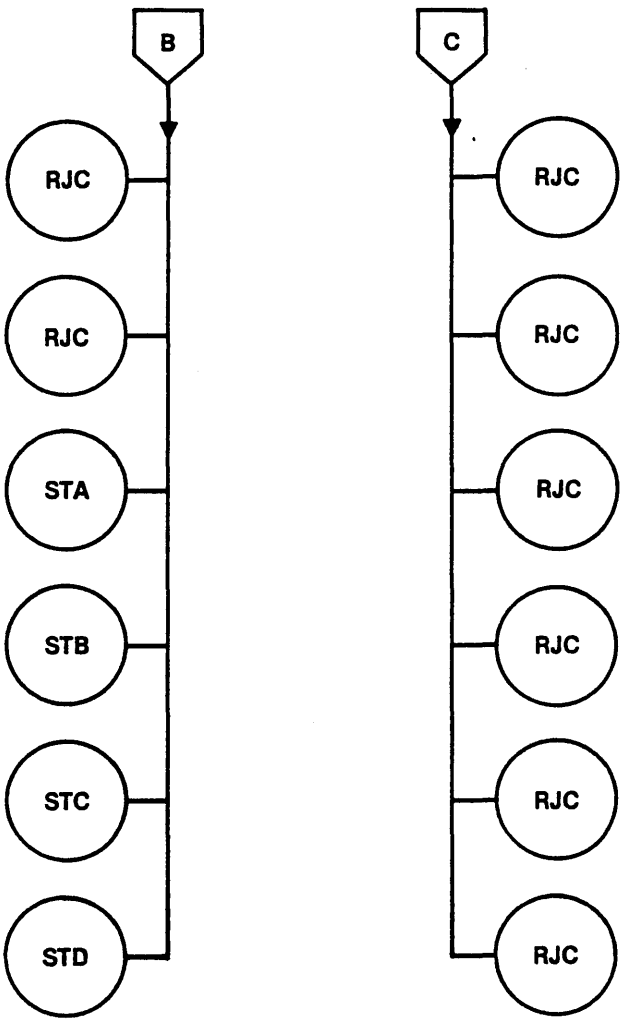


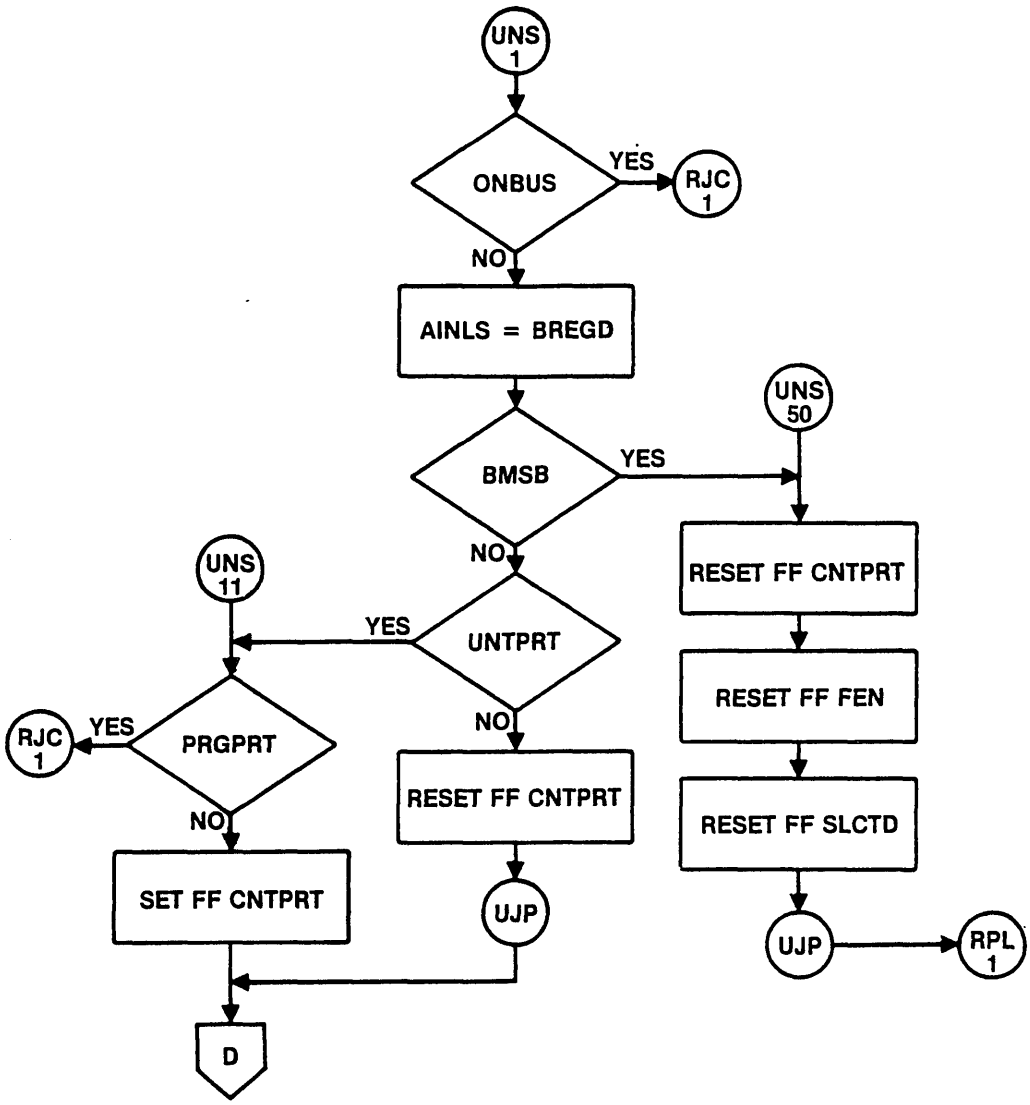
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 6 of 75)



A/Q EXECUTE (CONTD)

2338A

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 7 of 75)



UNIT SELECT

2339

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 8 of 75)

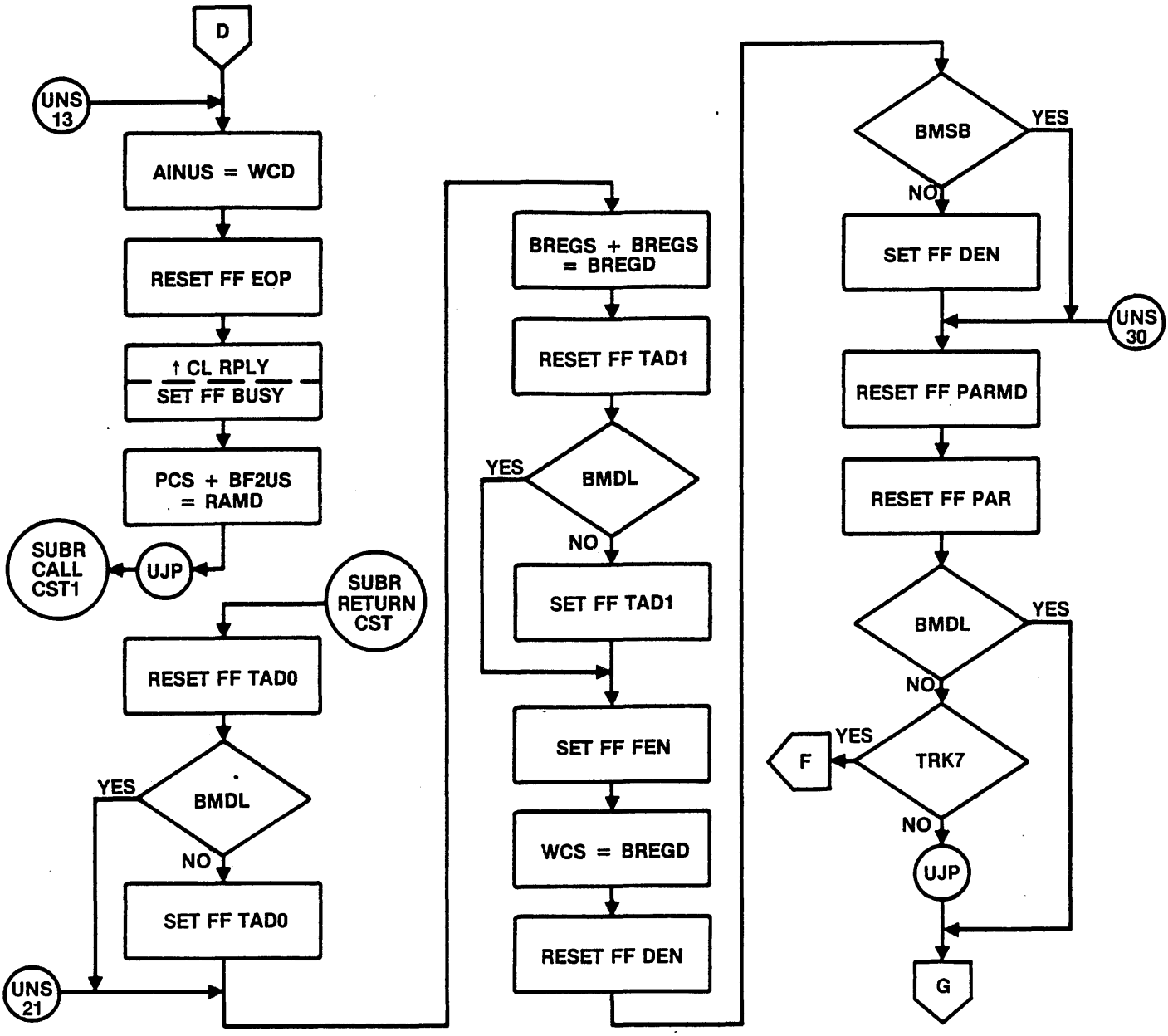
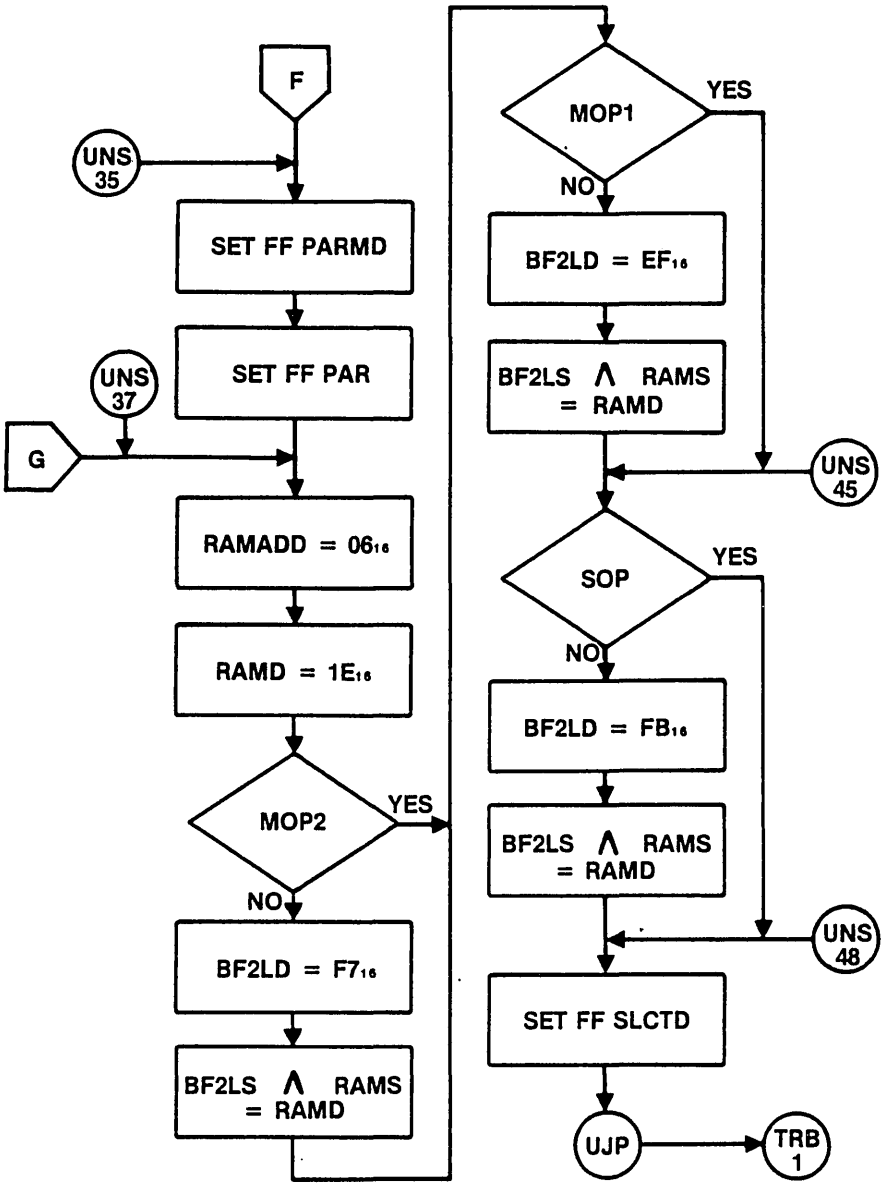


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 9 of 75)



UNIT SELECT (CONTD)

2339B

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 10 of 75)

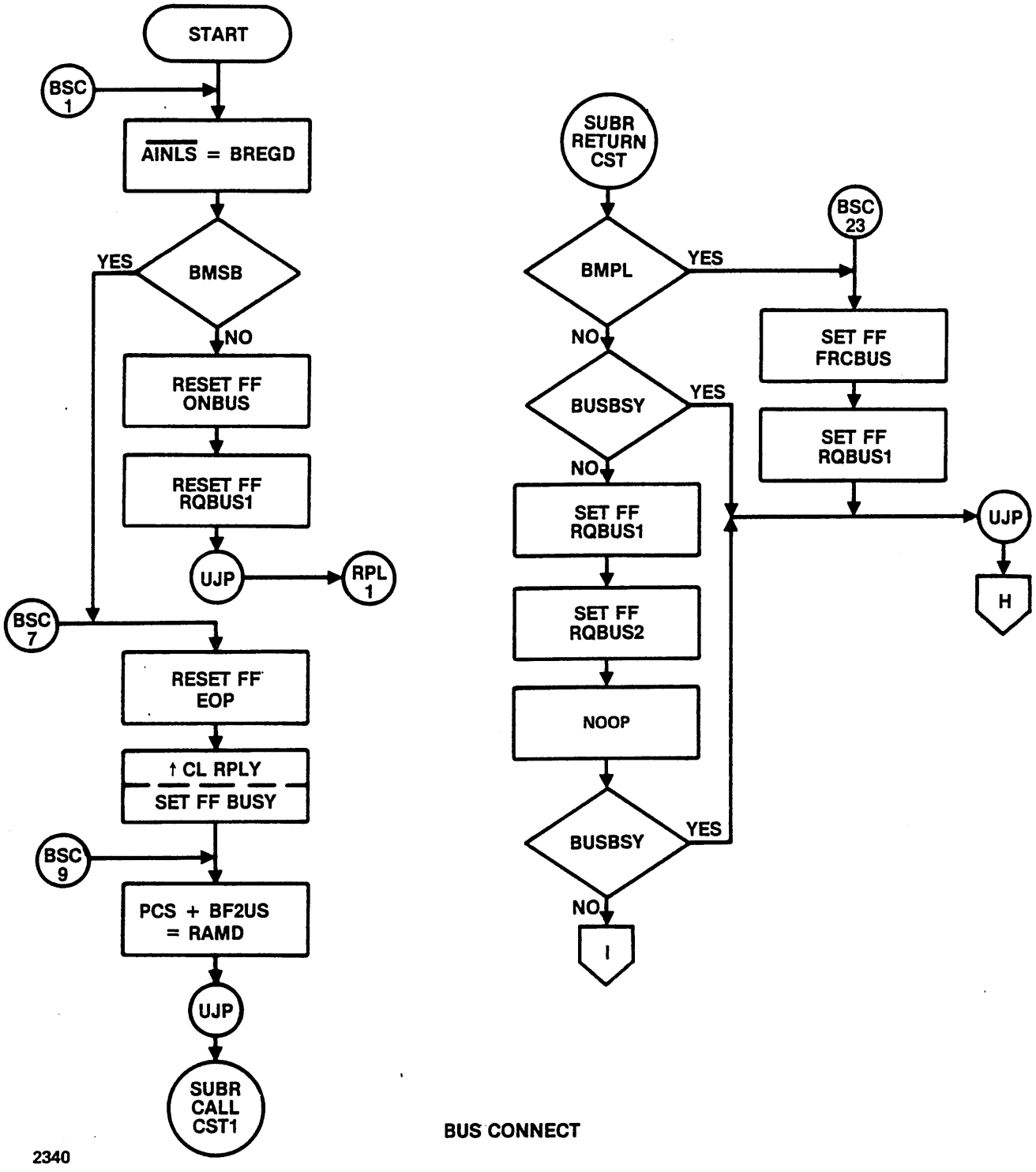
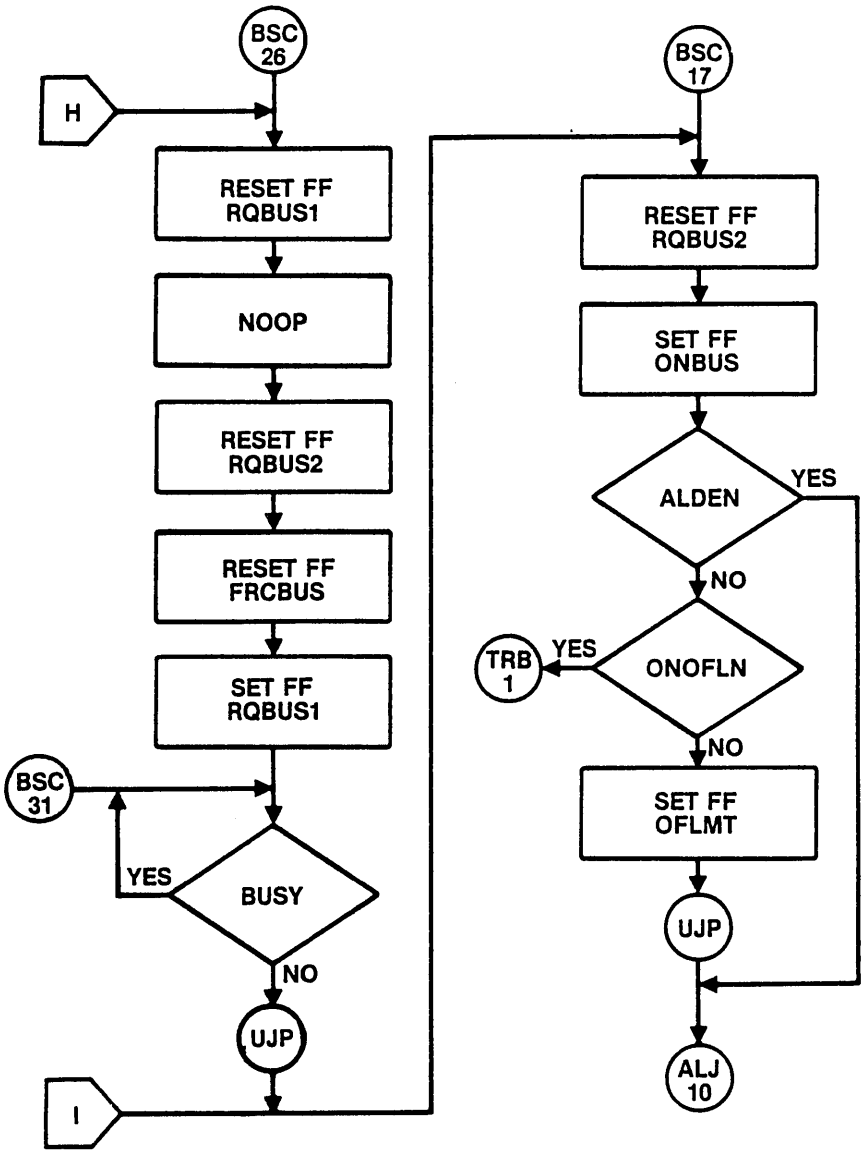


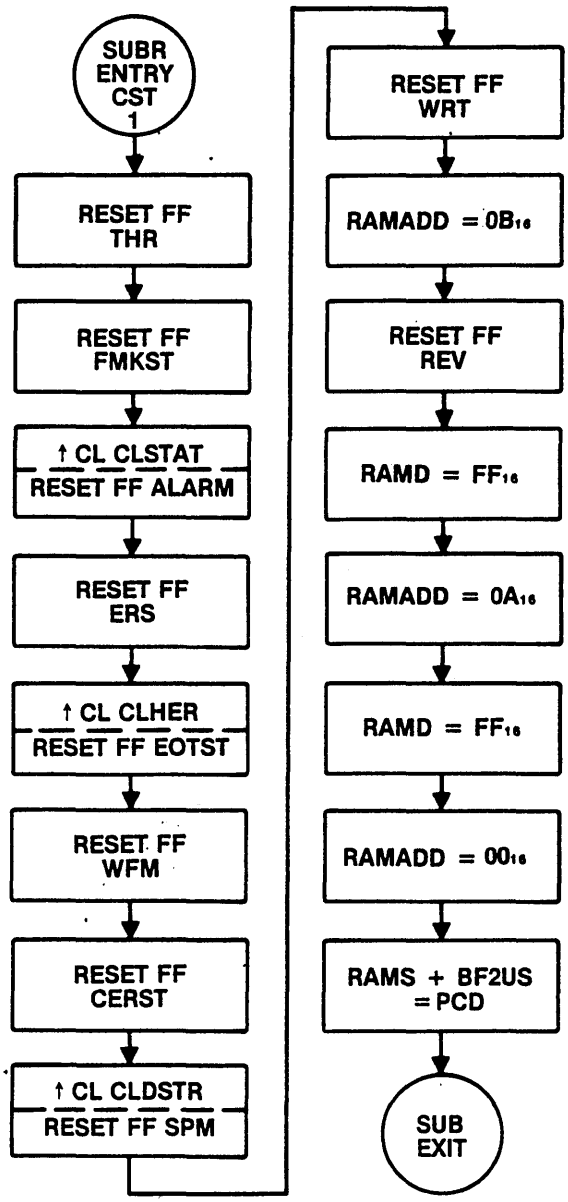
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 11 of 75)



BUS CONNECT (CONTD)

2340A

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 12 of 75)



CLEAR STATUS

2341

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 13 of 75)

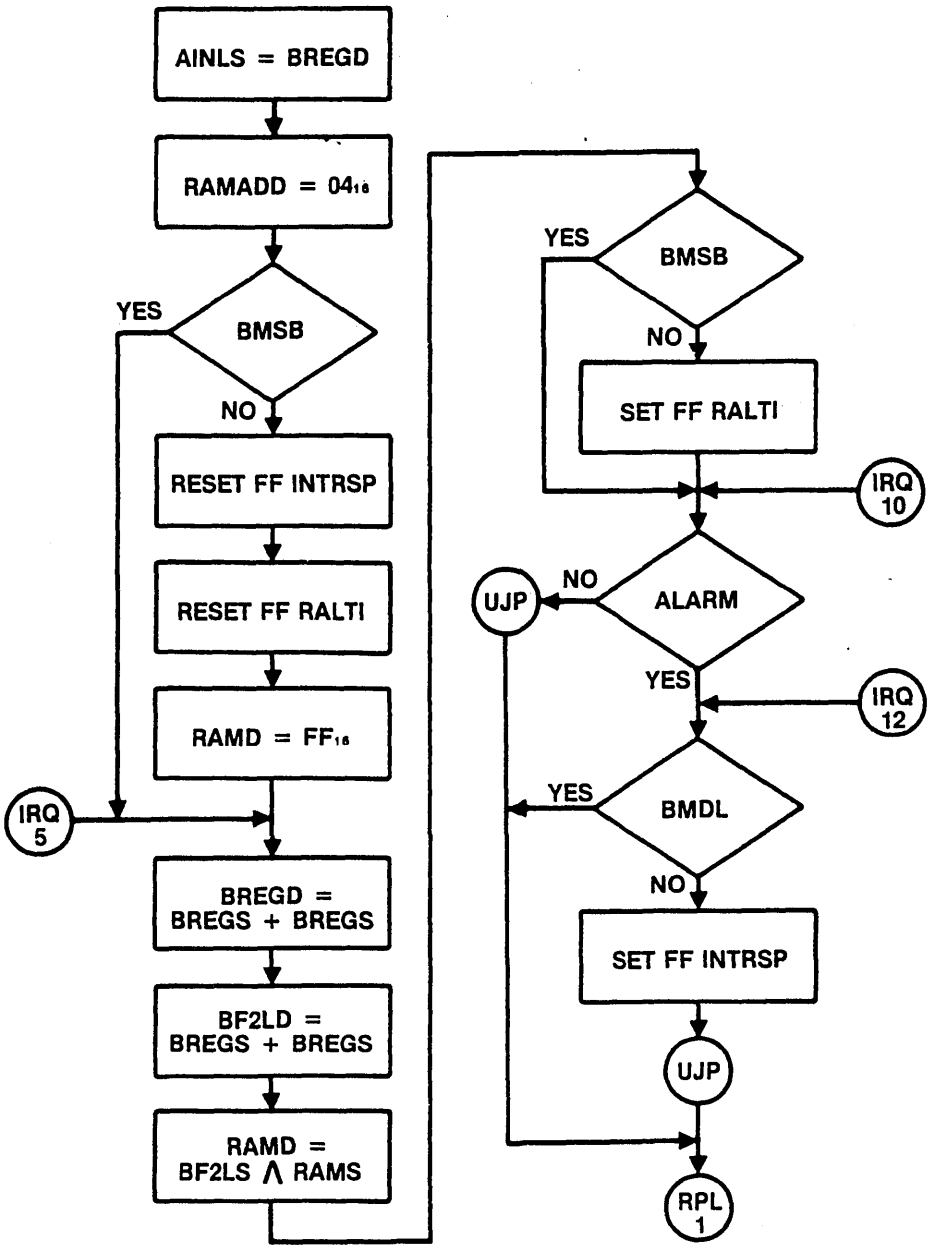


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 14 of 75)

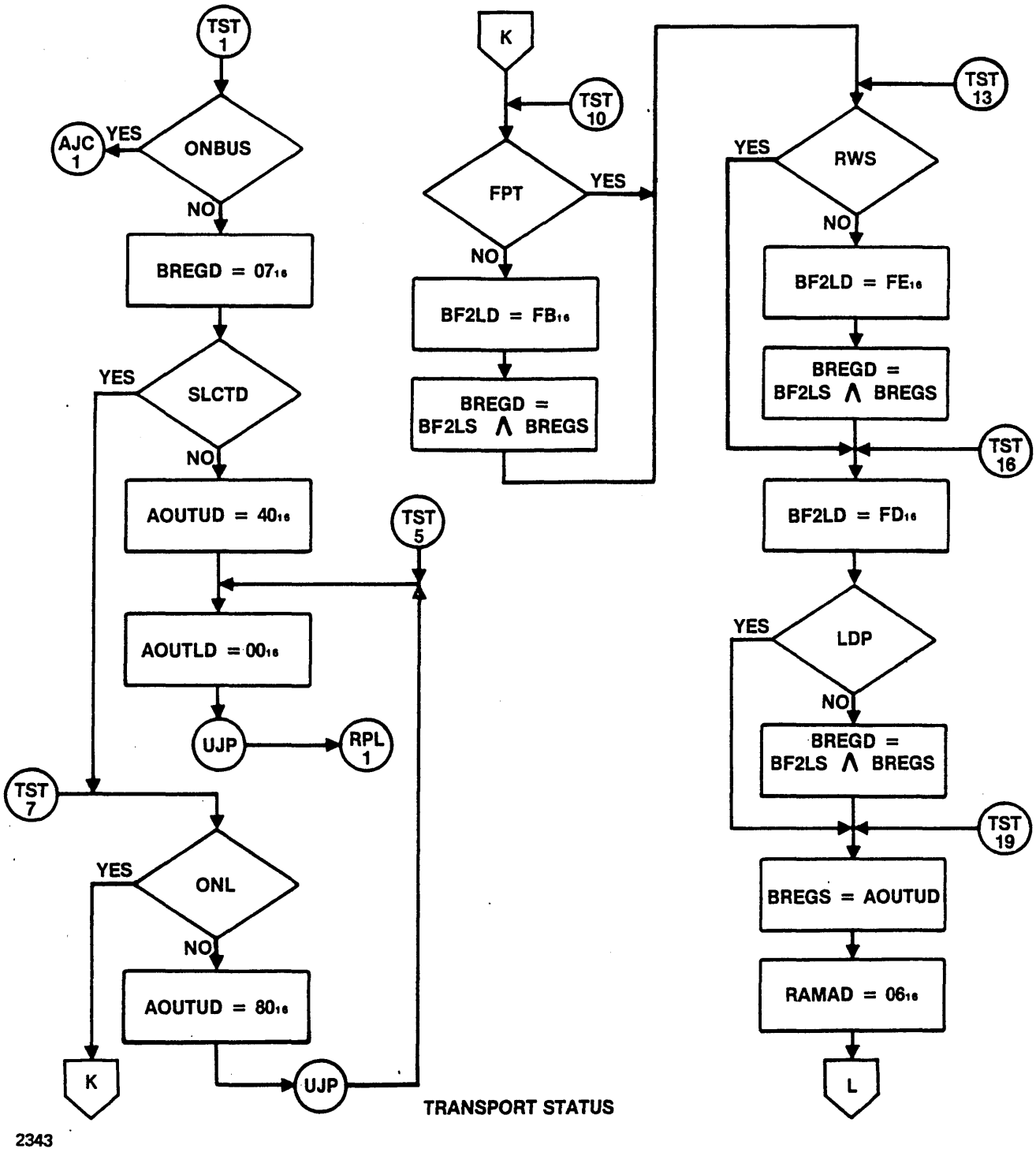


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 15 of 75)

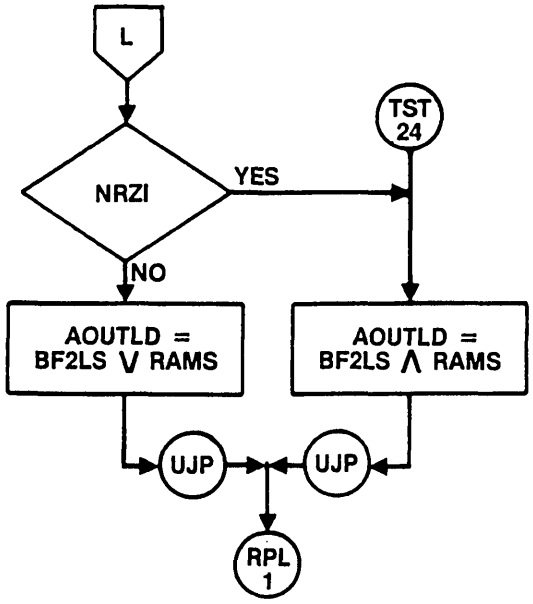


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 16 of 75)

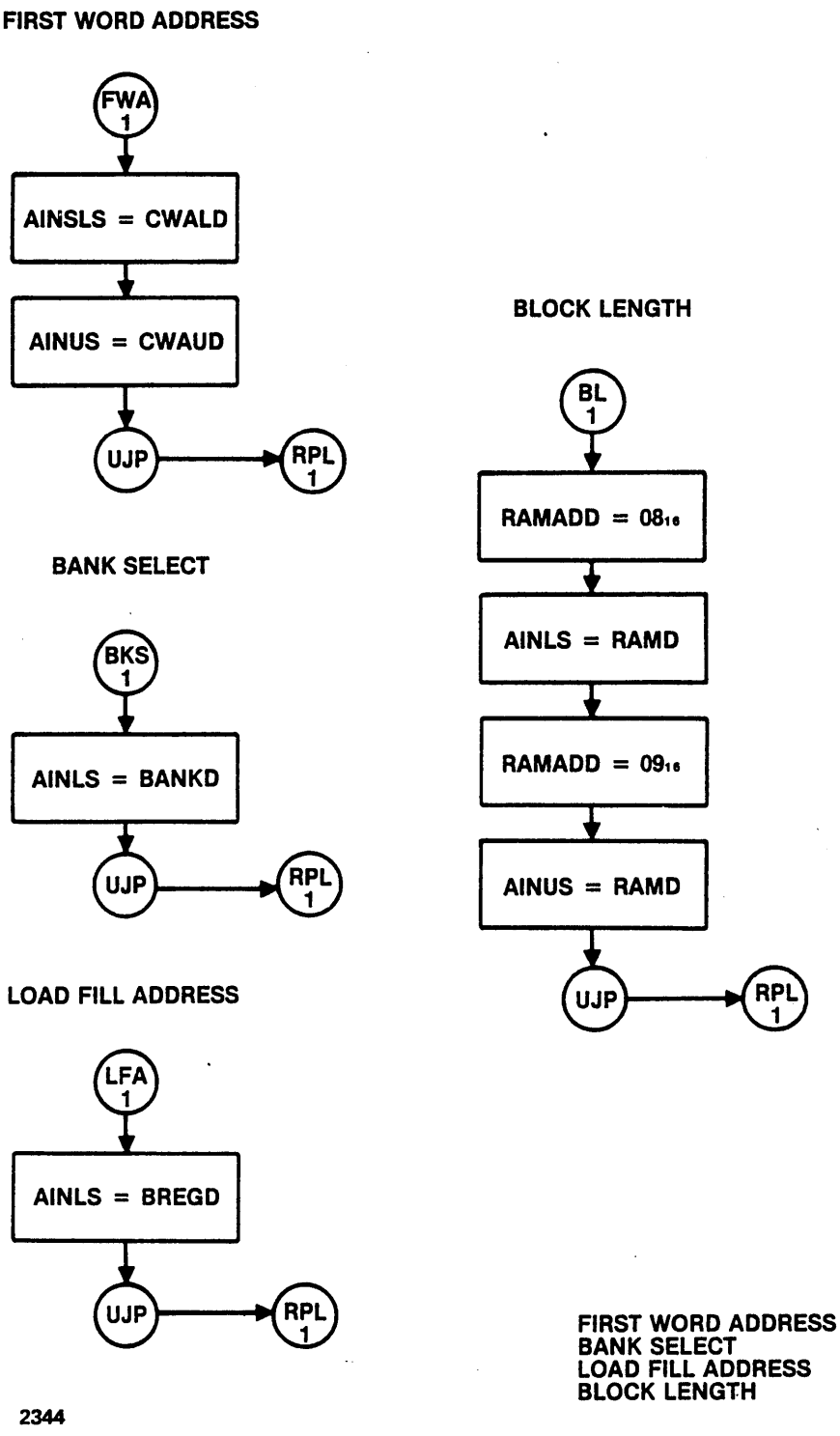


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 17 of 75)

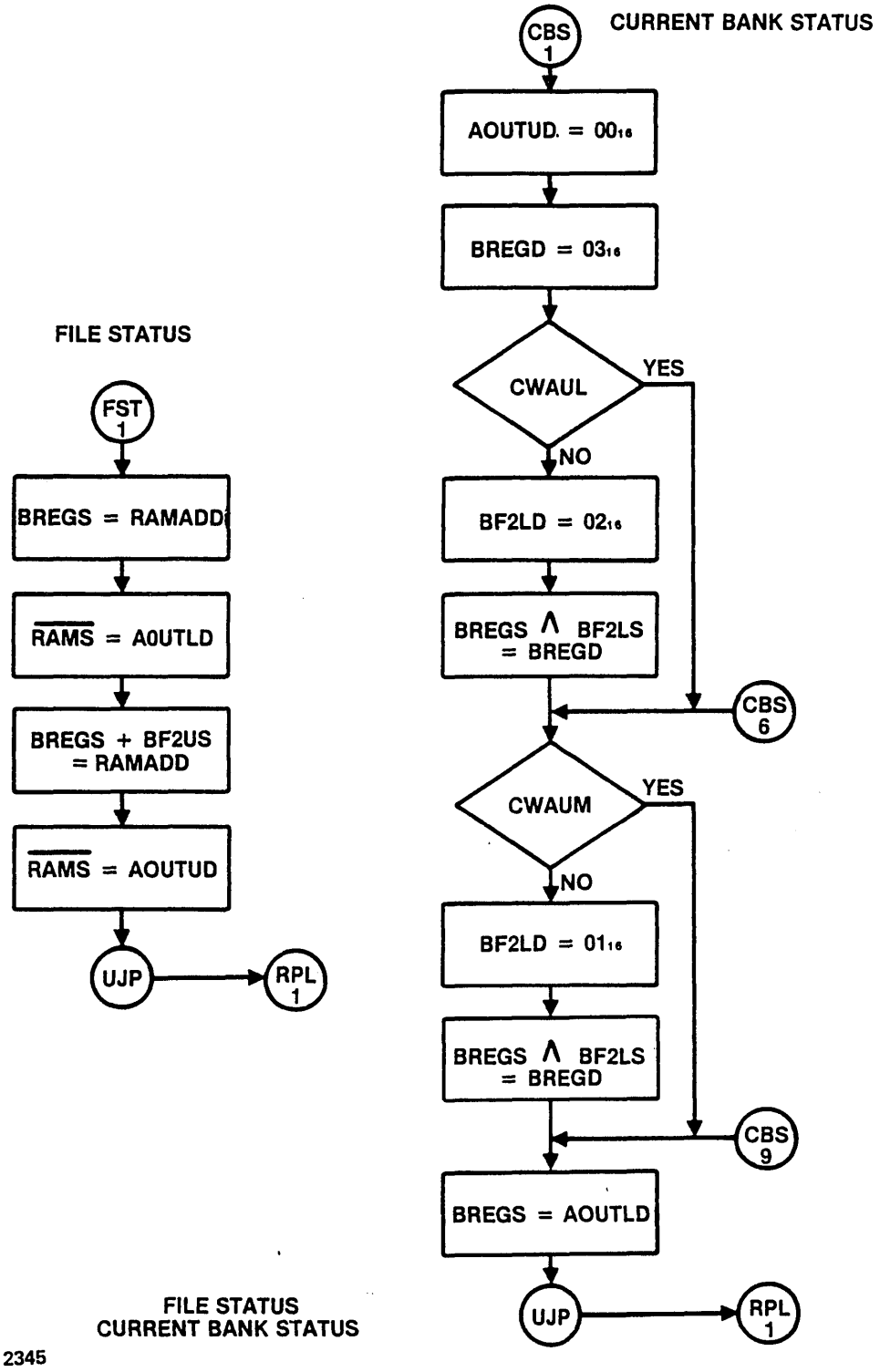
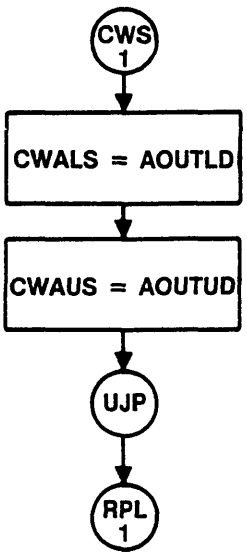


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 18 of 75)



CURRENT WORD STATUS

2346

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 19 of 75)

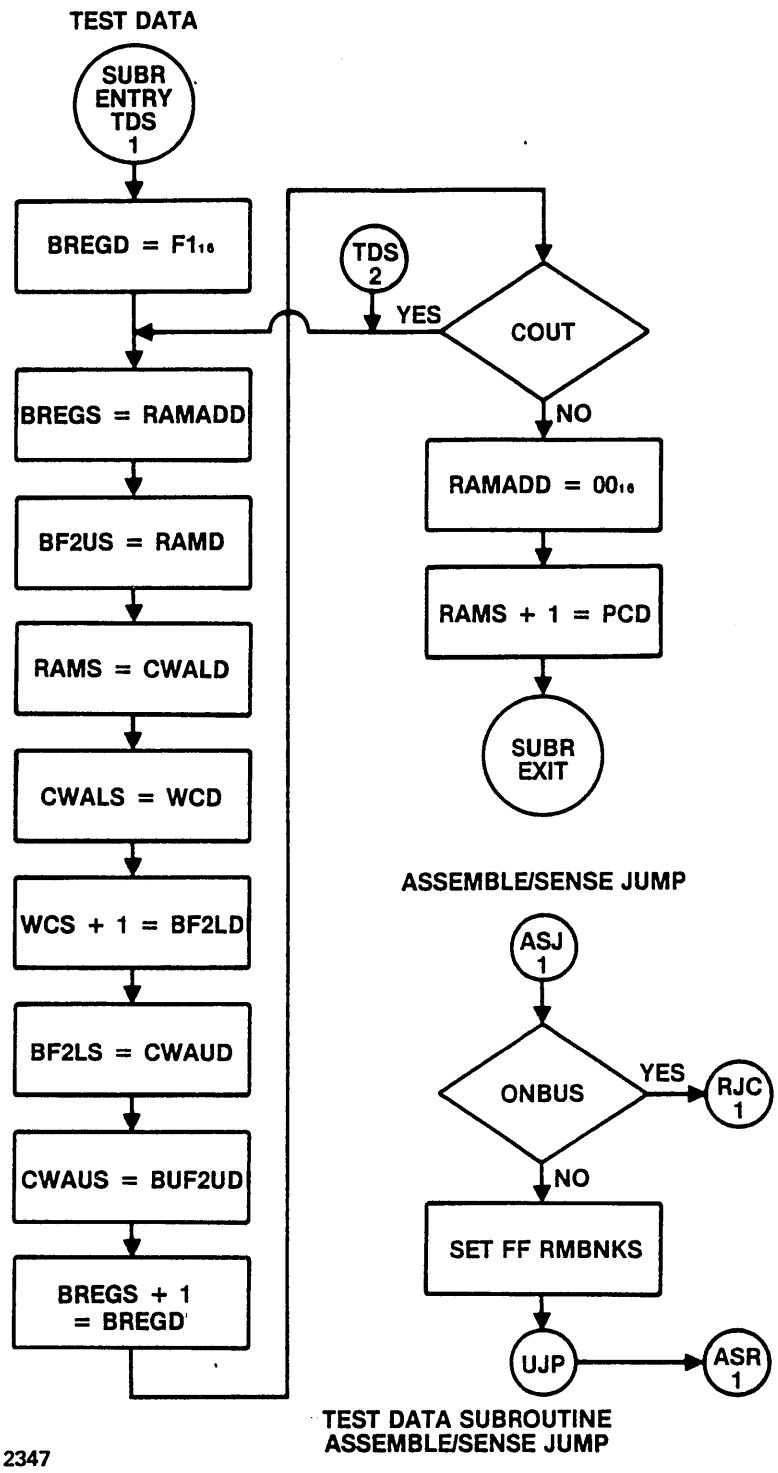
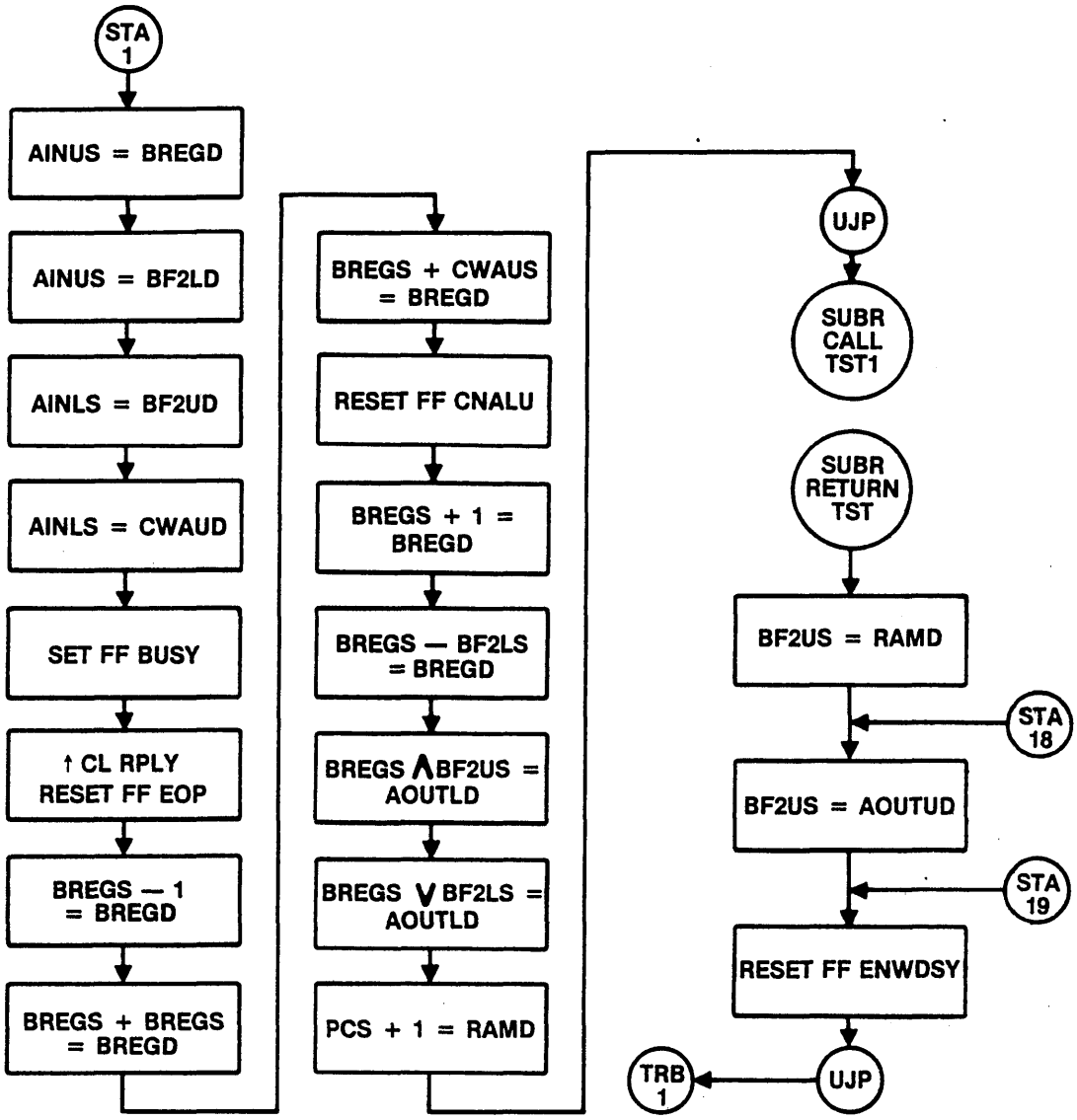


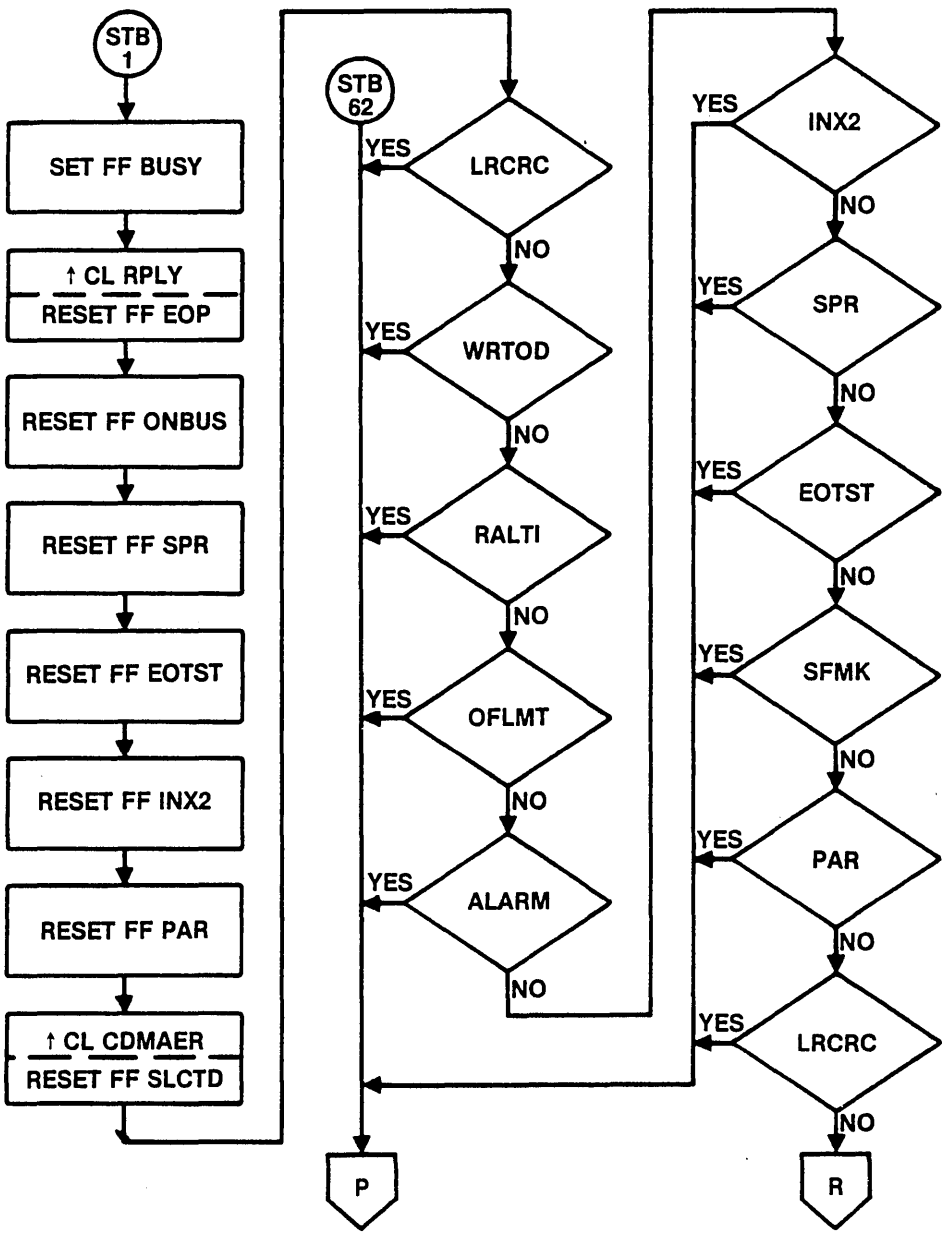
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 20 of 75)



SELF TEST 1

2348

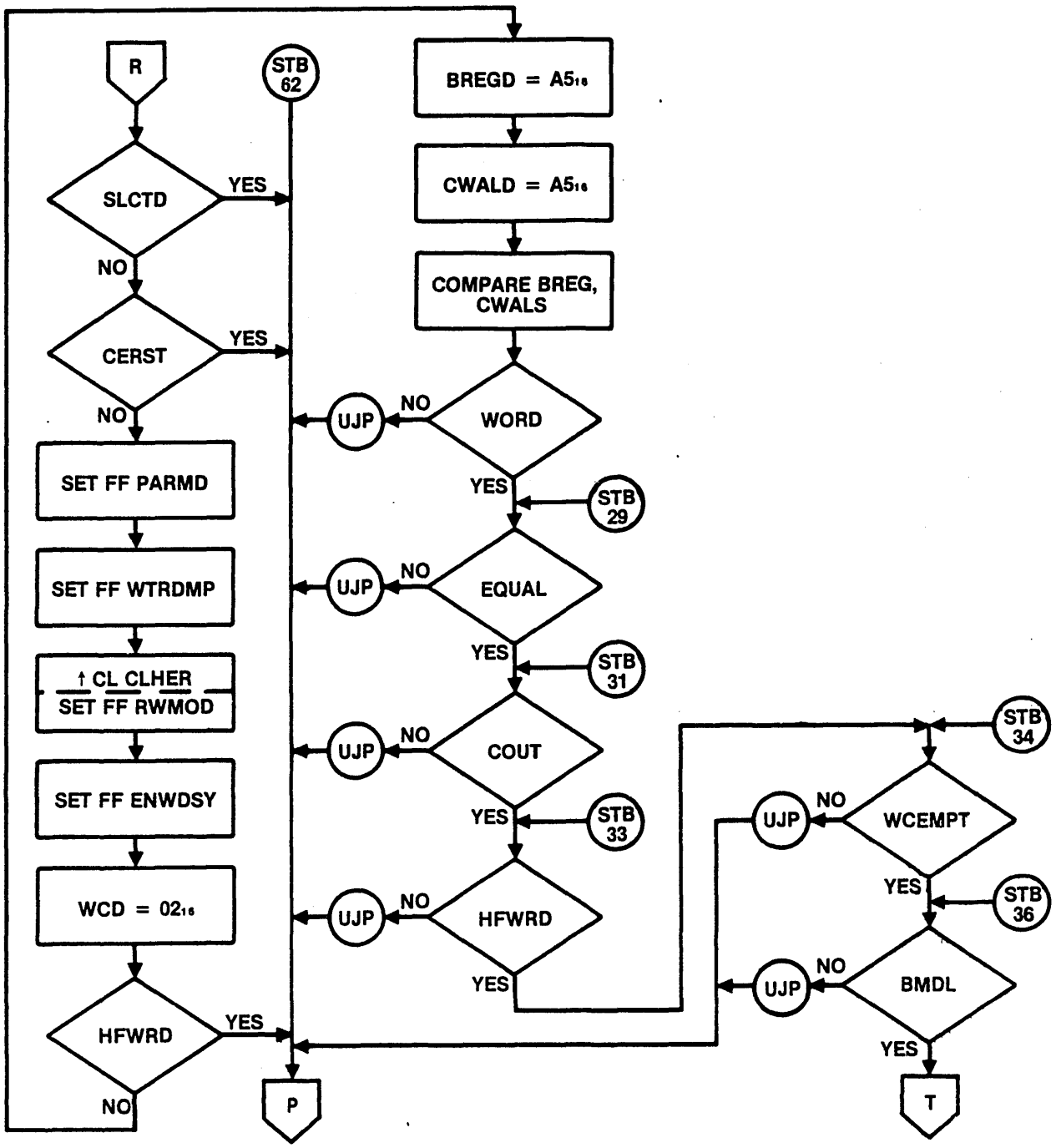
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 21 of 75)



SELF TEST 2

2349

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 22 of 75)



SELF TEST 2 (CONTD)

2349A

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 23 of 75)

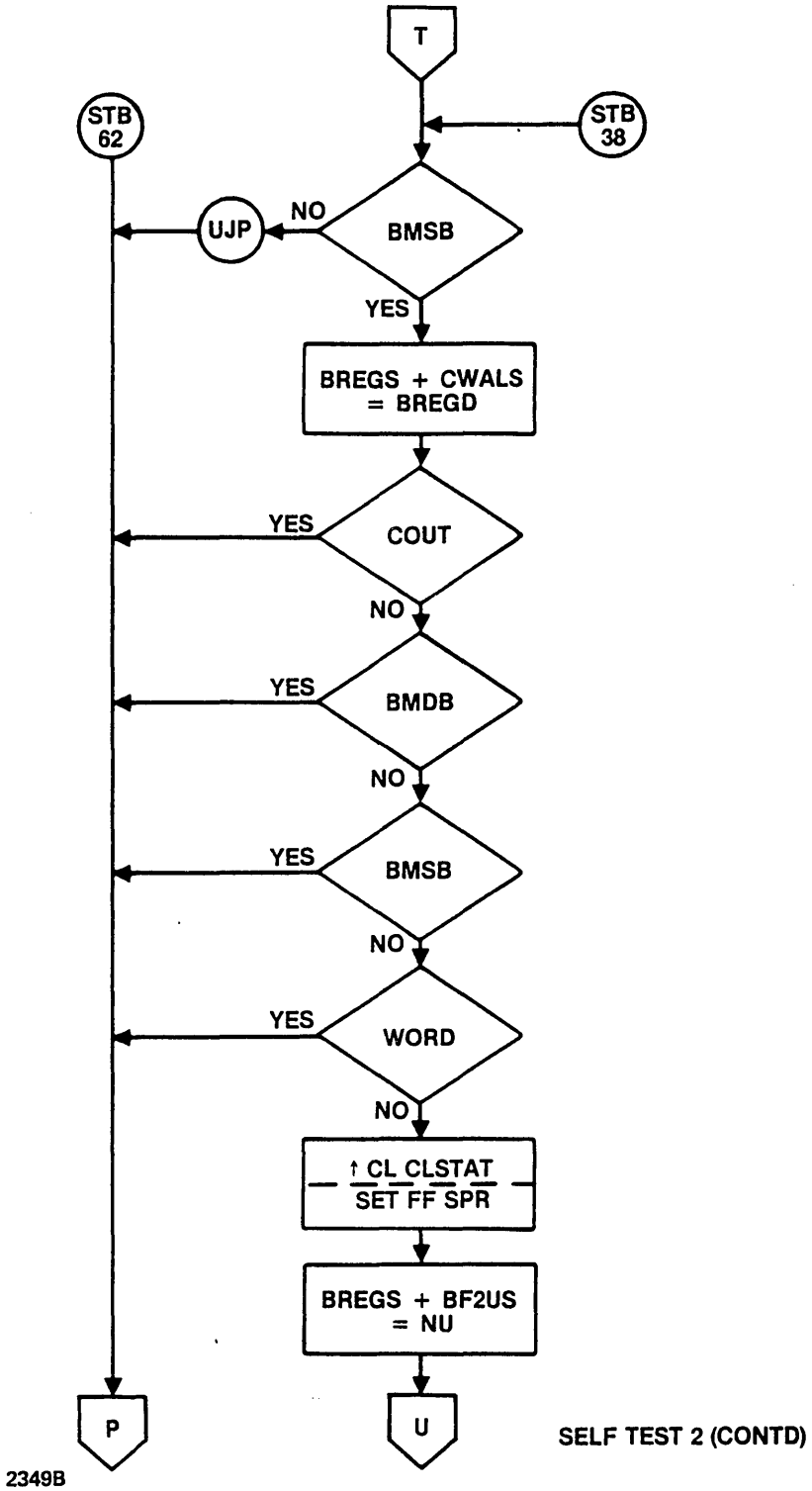
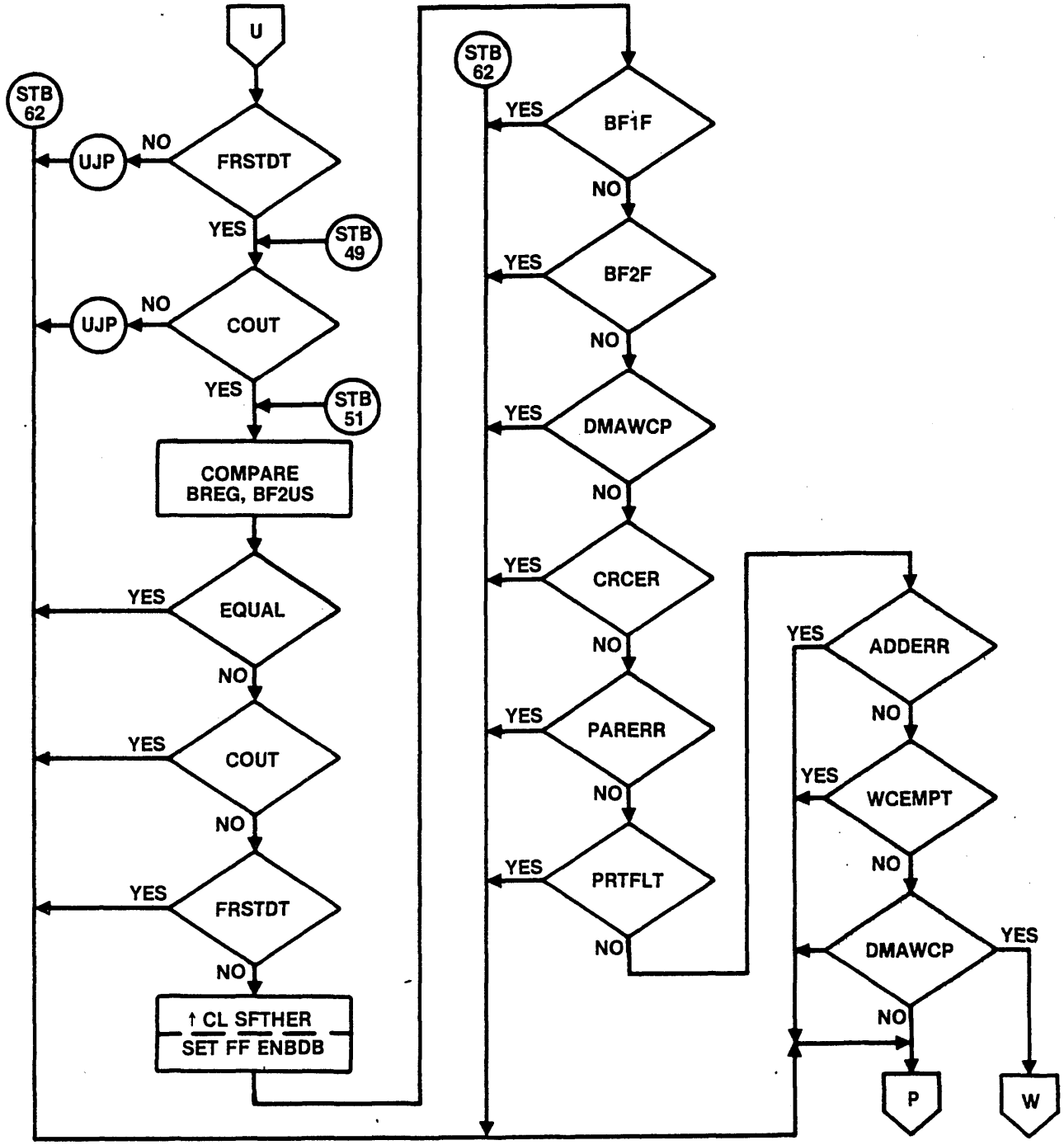


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 24 of 75)



SELF TEST 2 (CONTD)

2349C

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 25 of 75)

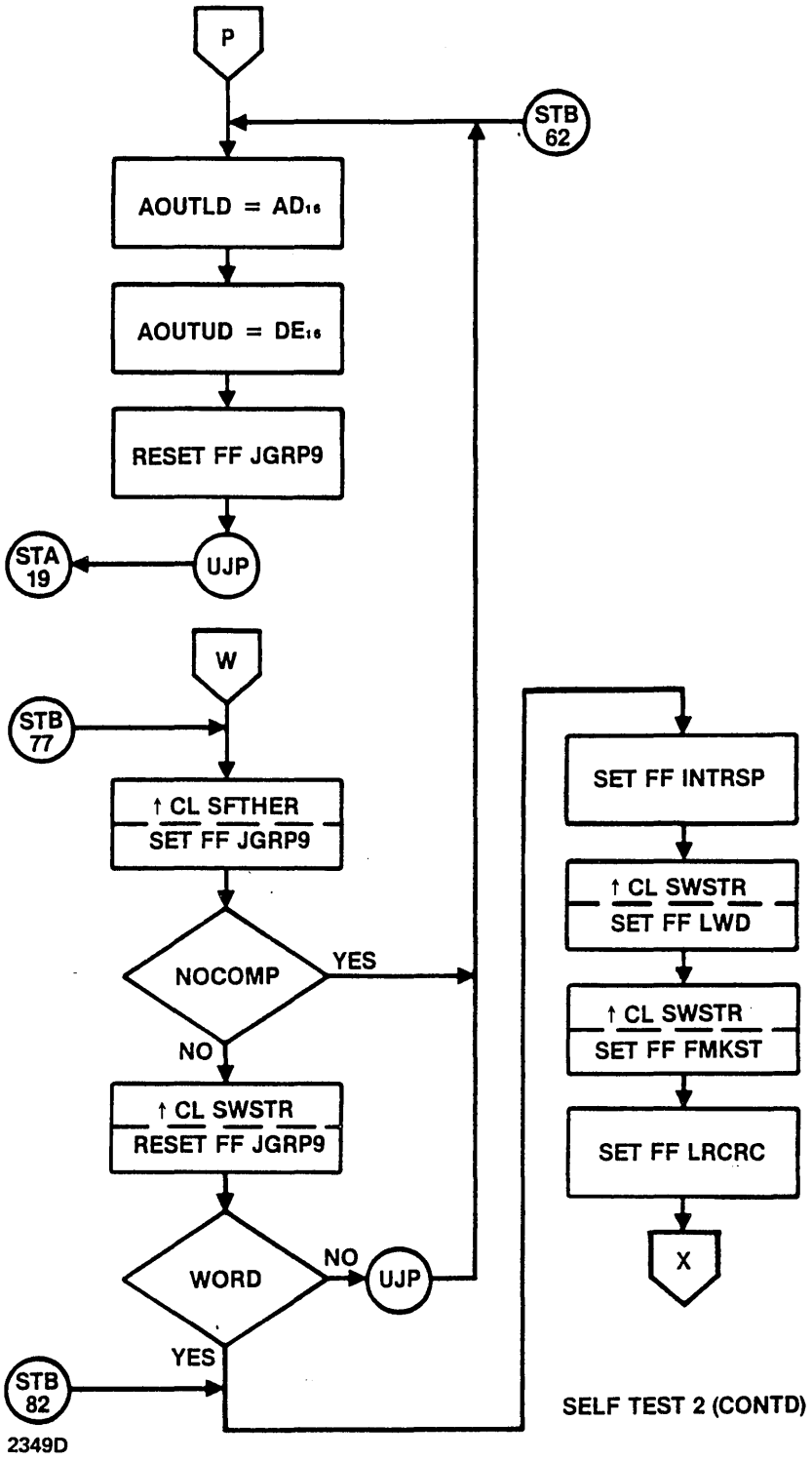
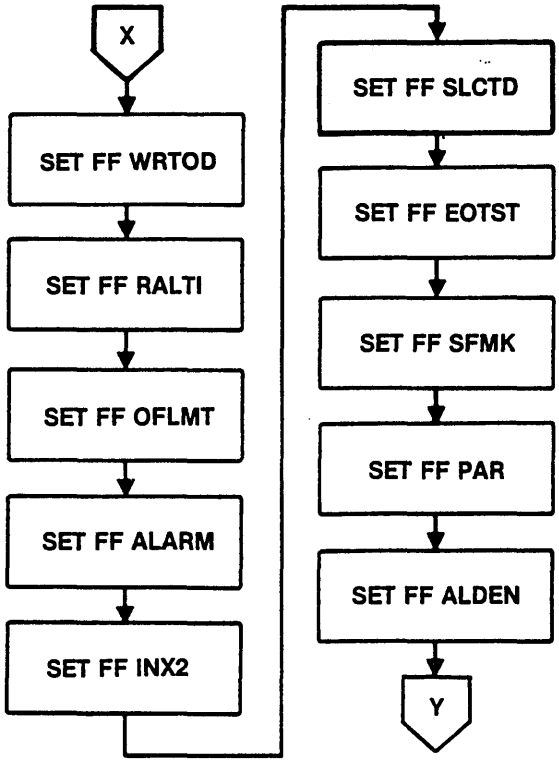


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 26 of 75)



SELF TEST 2 (CONTD)

2349E

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 27 of 75)

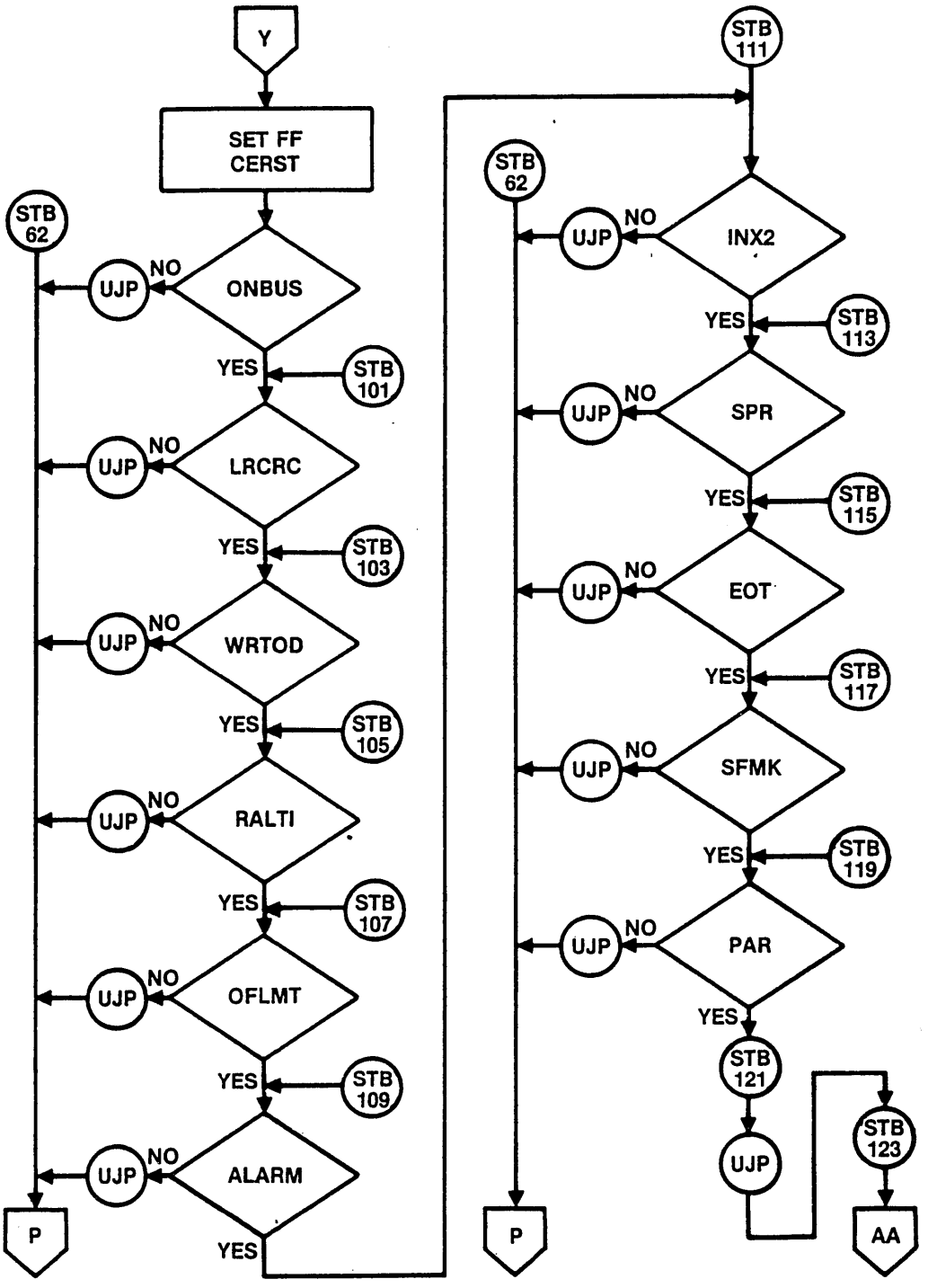
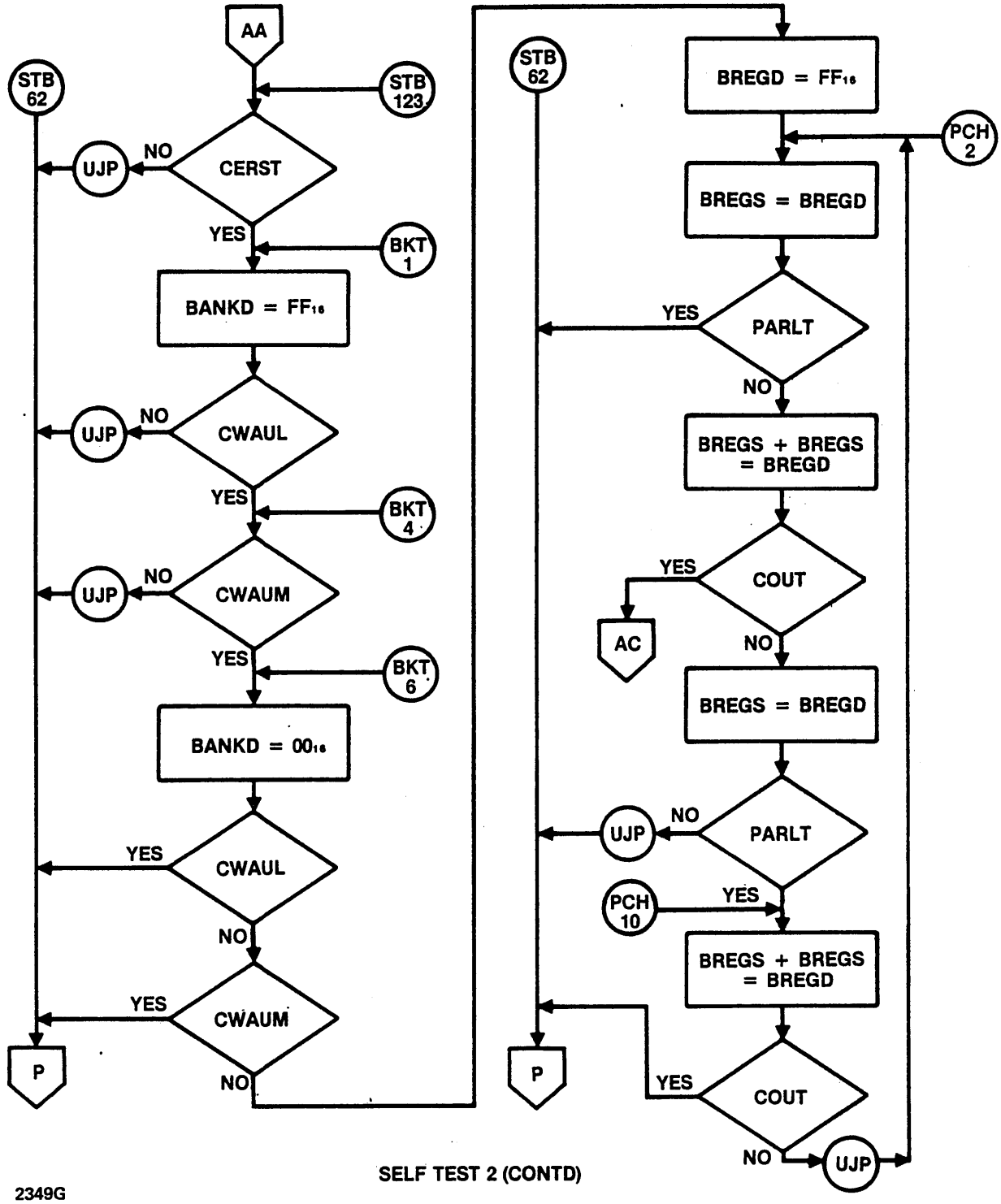


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 28 of 75)



SELF TEST 2 (CONTD)

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 29 of 75)

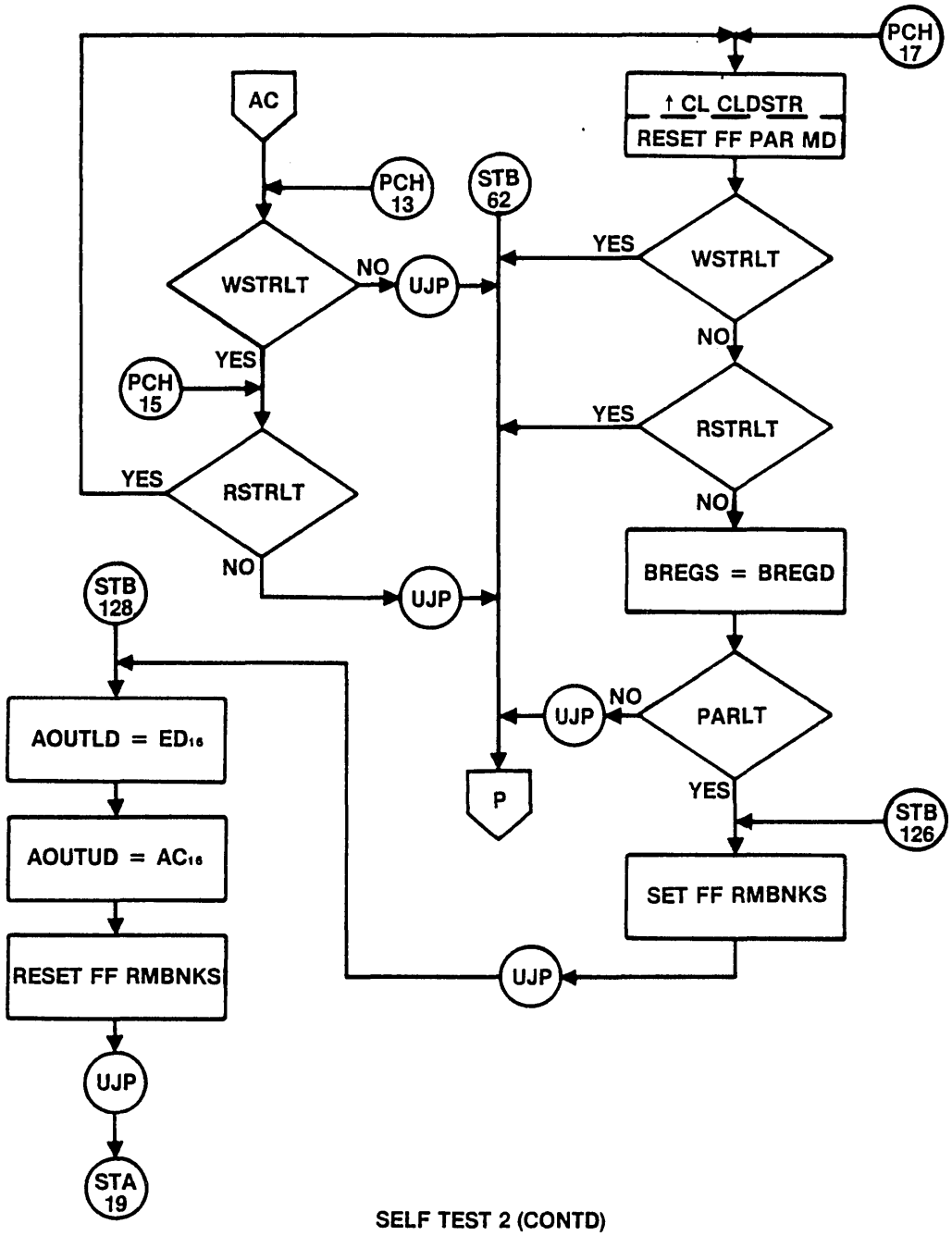
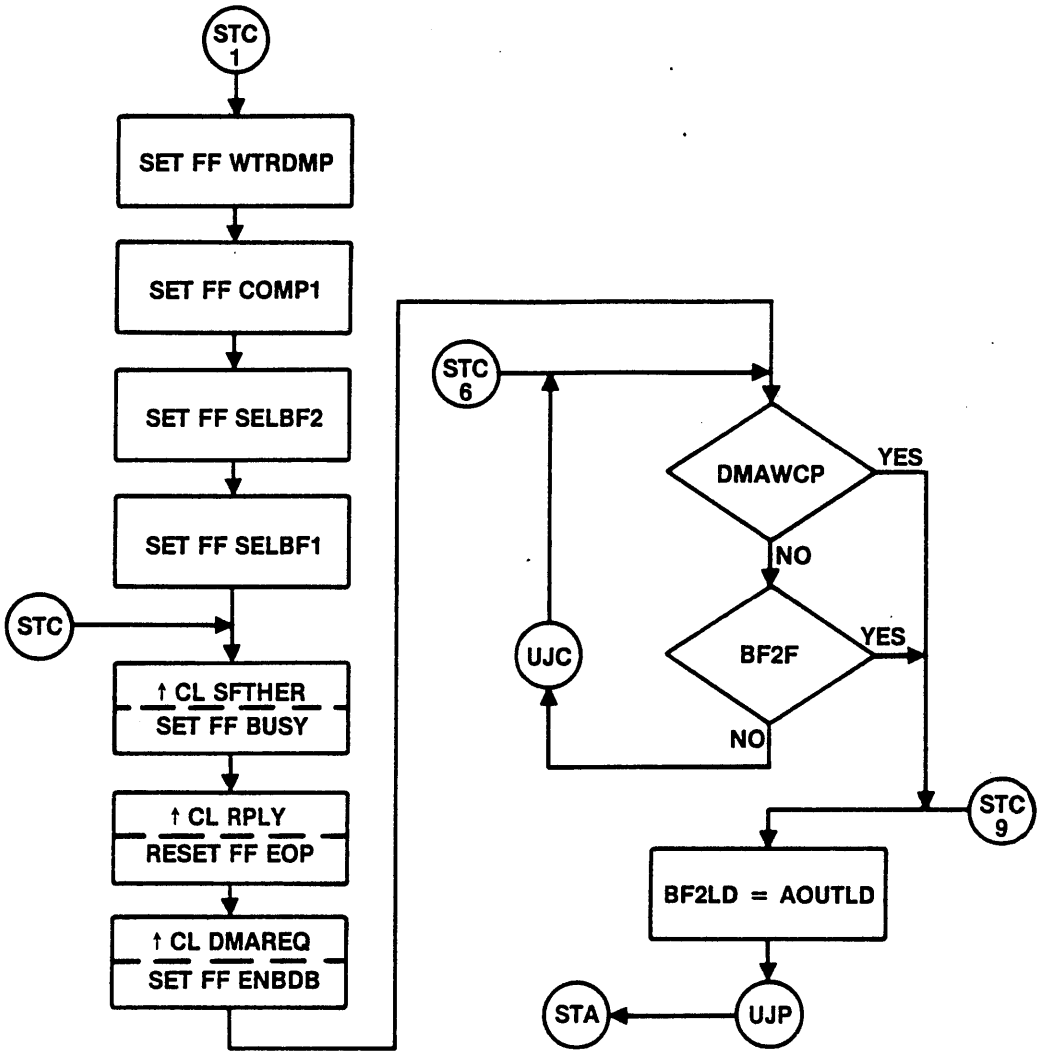


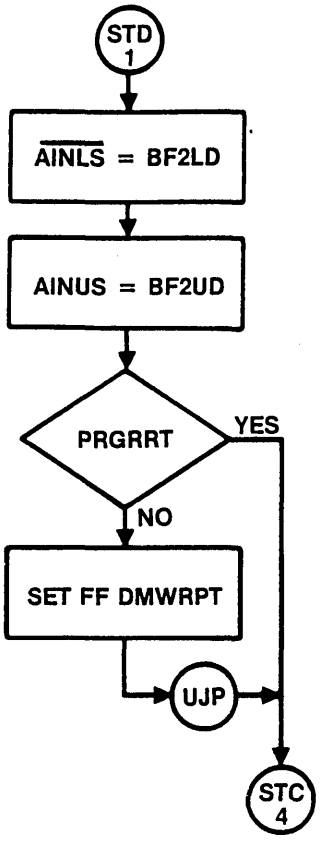
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 30 of 75)



SELF TEST 3

2350

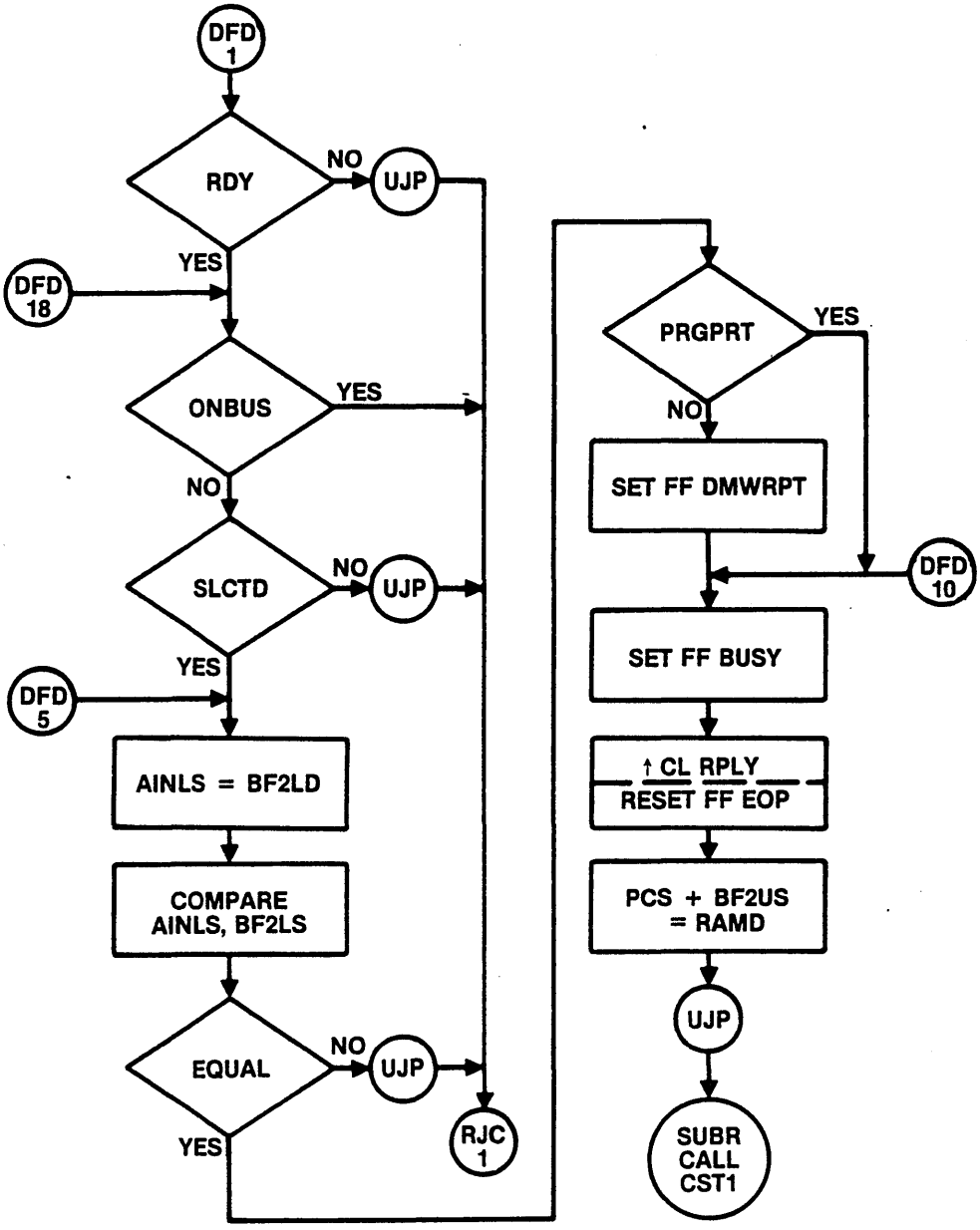
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 31 of 75)



SELF TEST 4

2351

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 32 of 75)



DIRECTOR FUNCTION DECODE

2352

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 33 of 75)

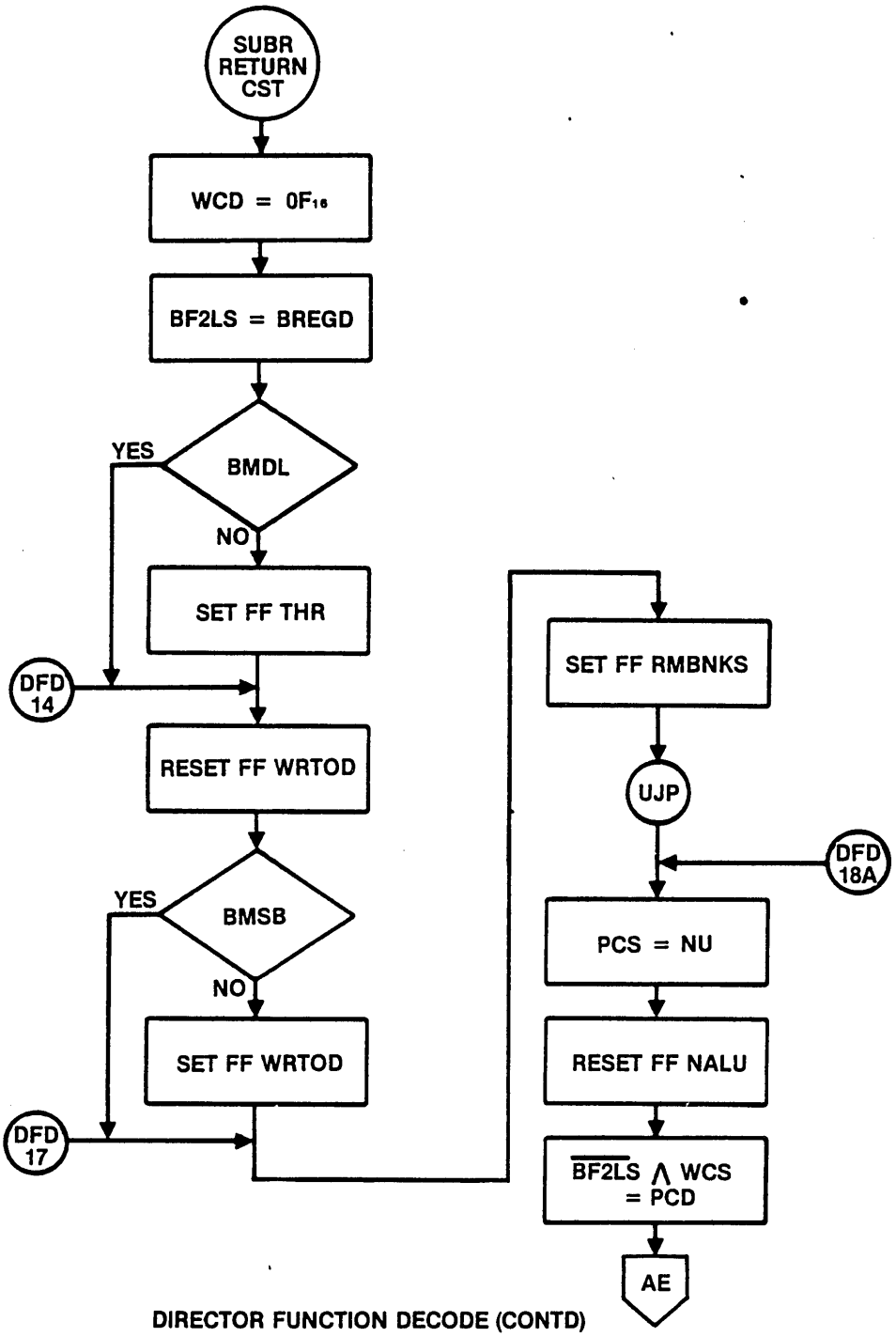


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 34 of 75)

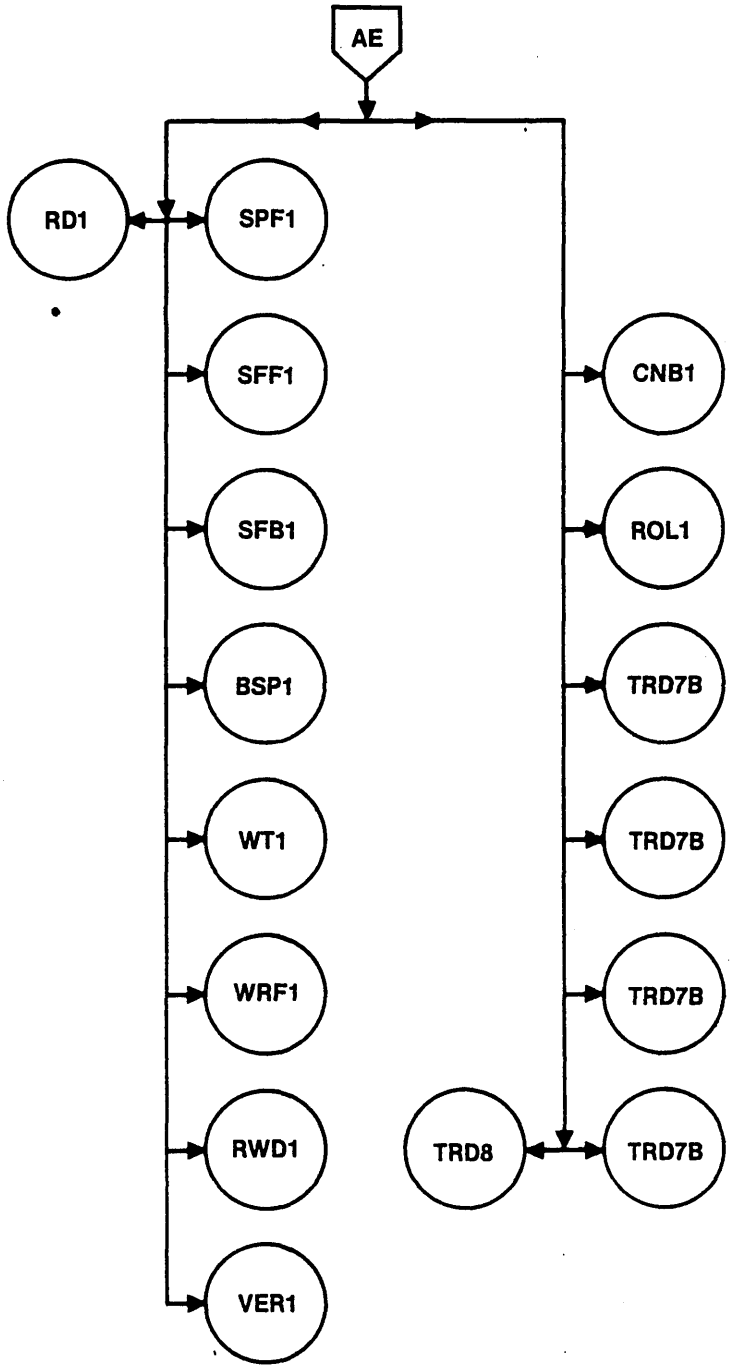
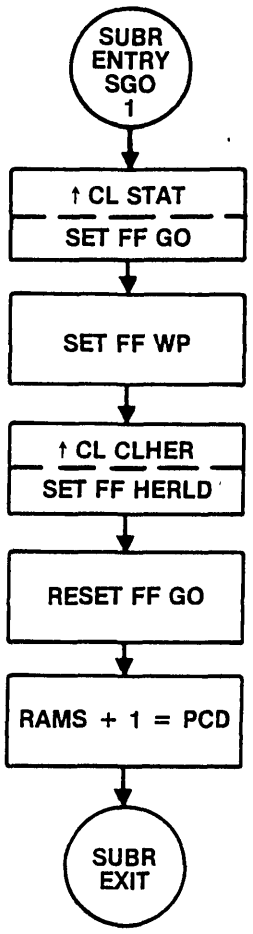


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 35 of 75)



SET GO

2354

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 36 of 75)

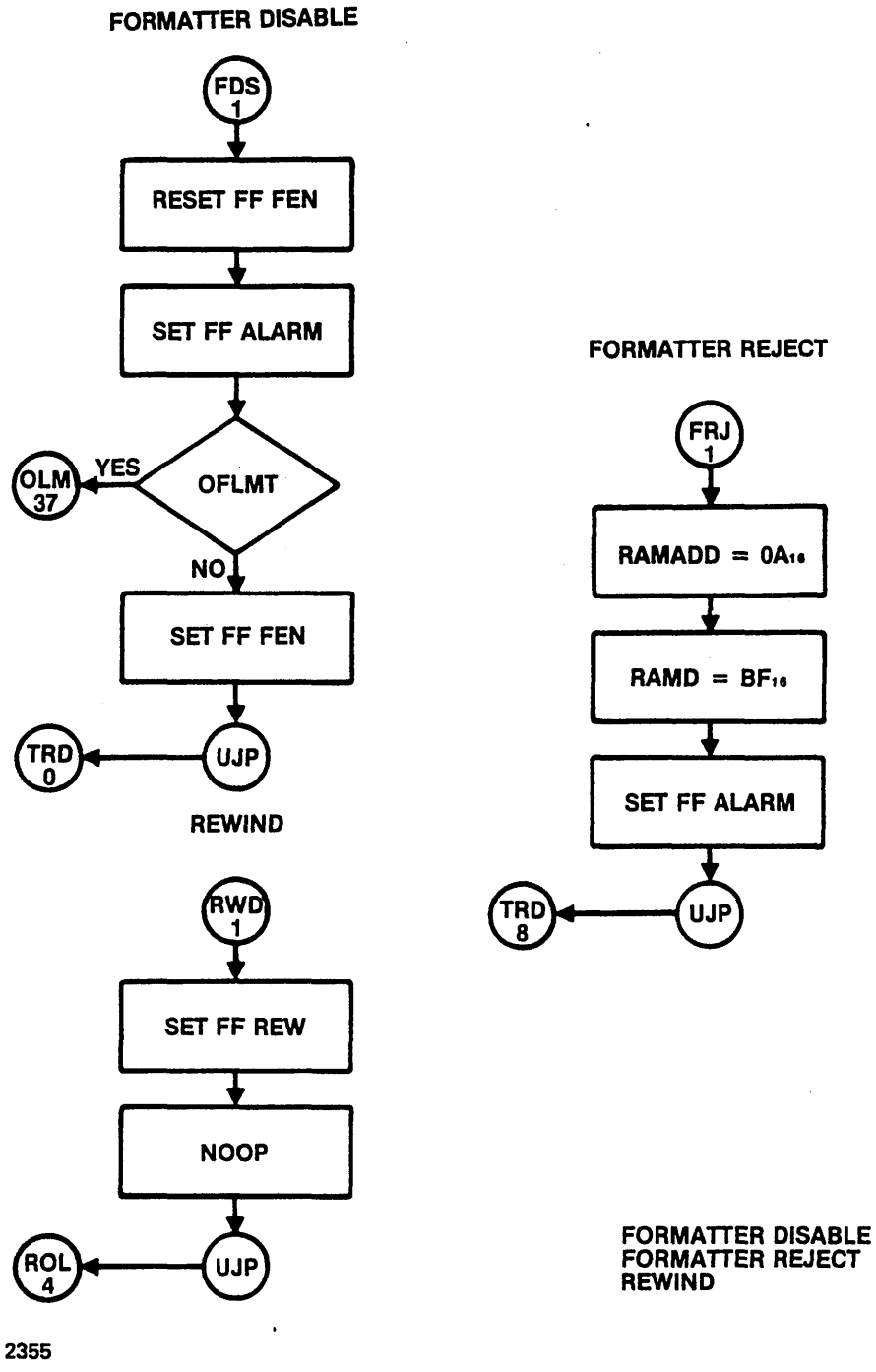
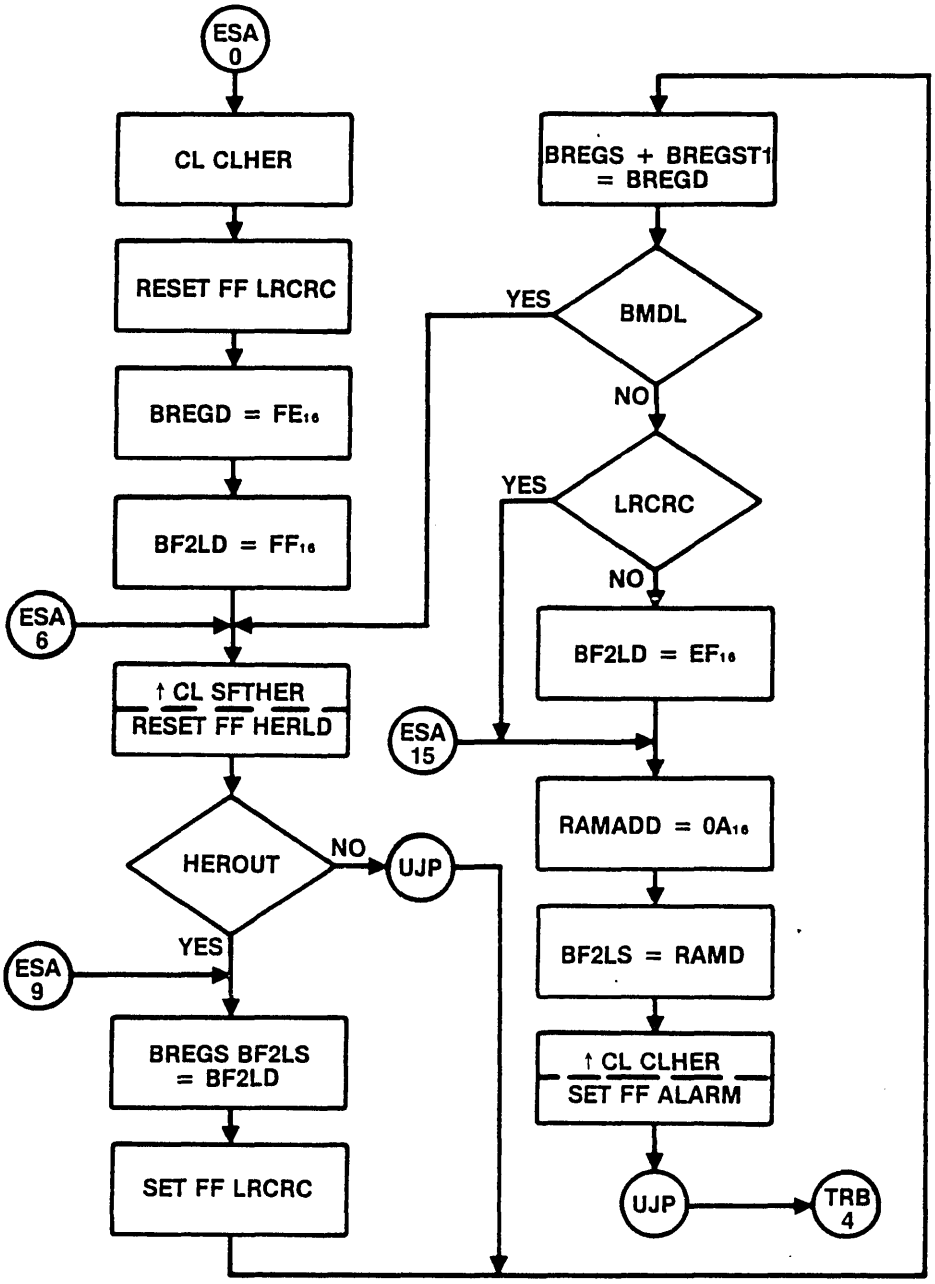


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 37 of 75)



ESO-4 ASSEMBLE

2356

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 38 of 75)

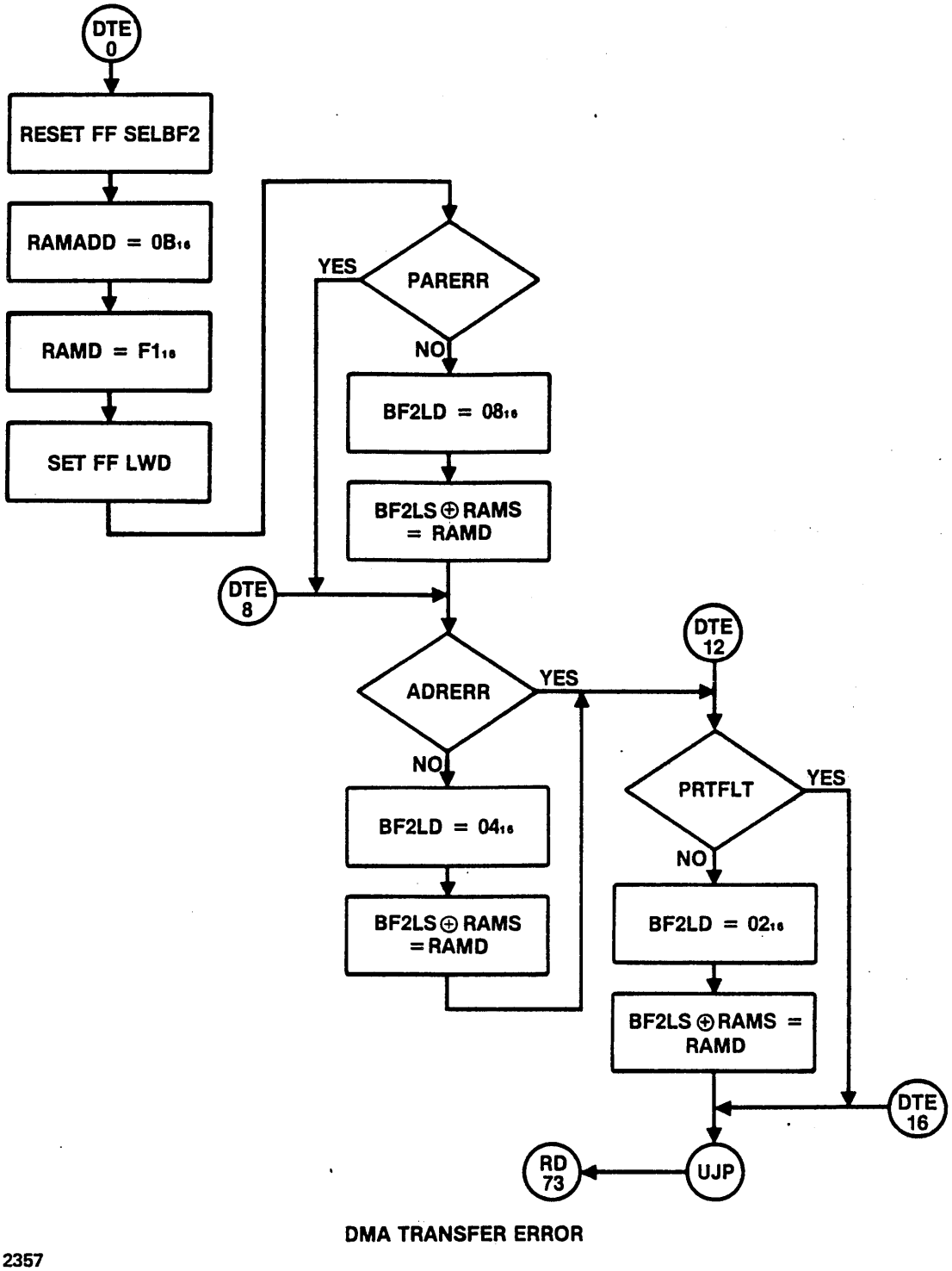
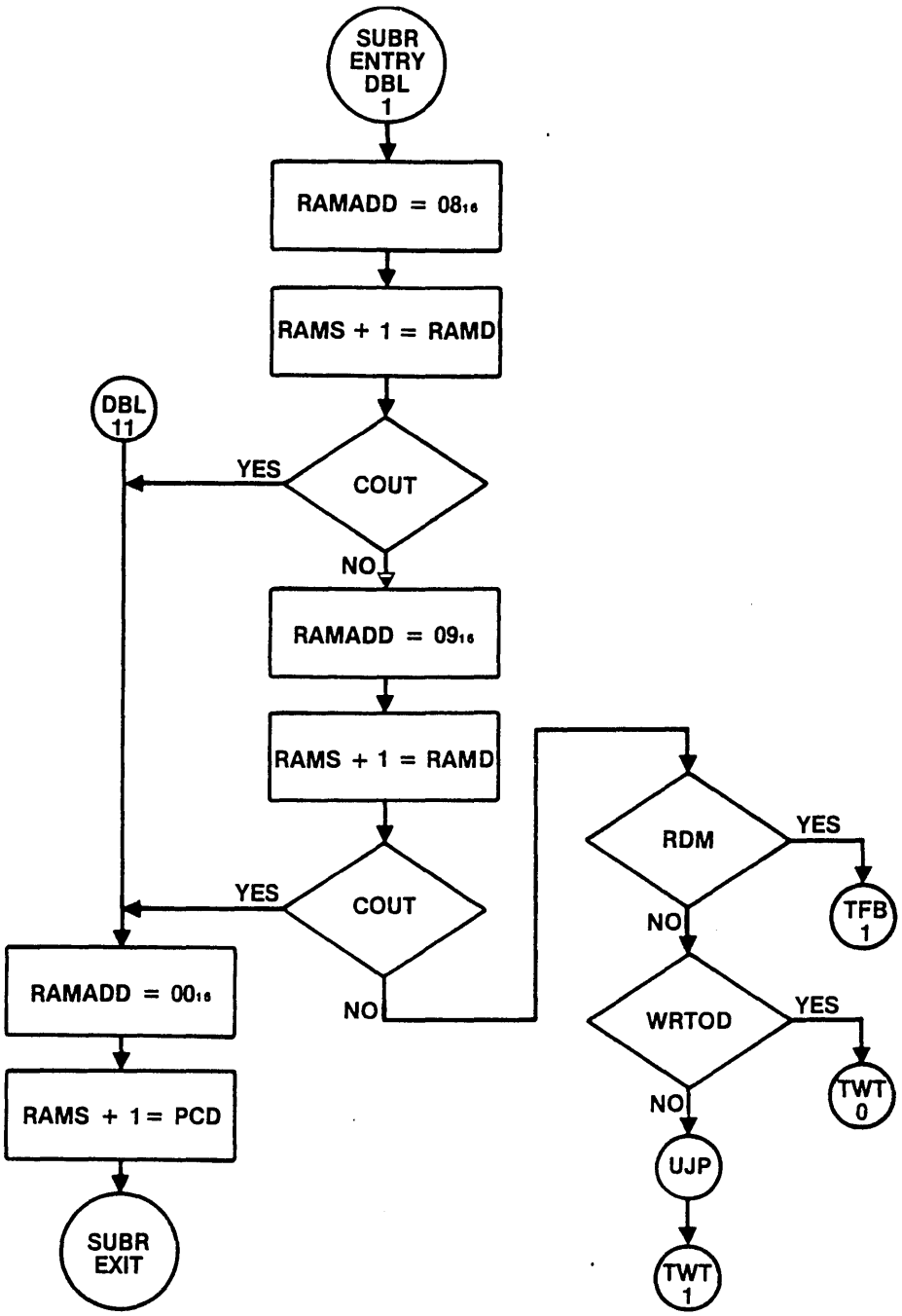


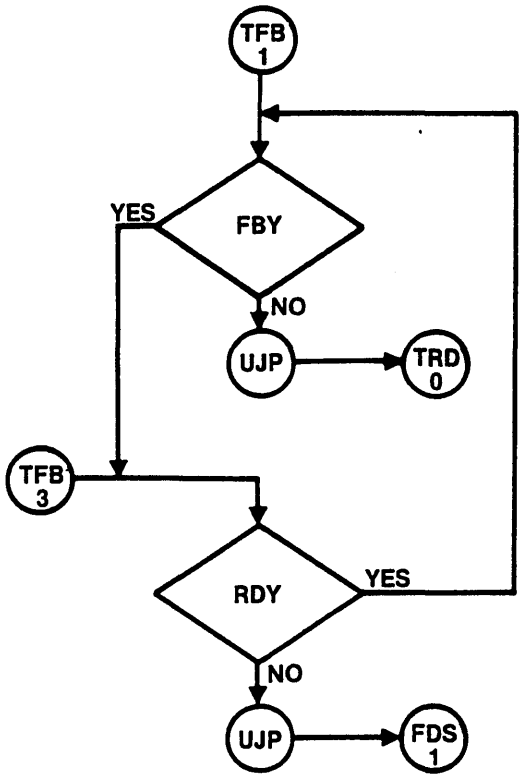
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 39 of 75)



DECREMENT BLOCK LENGTH

2358

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 40 of 75)



TERMINATE FORMATTER BUSY

2359

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 41 of 75)

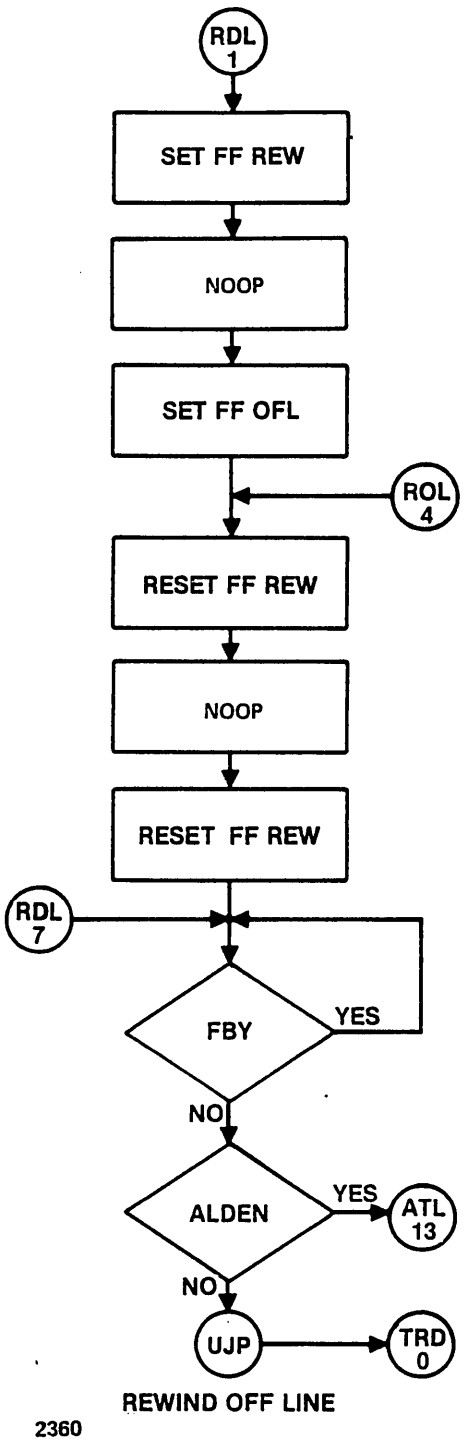


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 42 of 75)

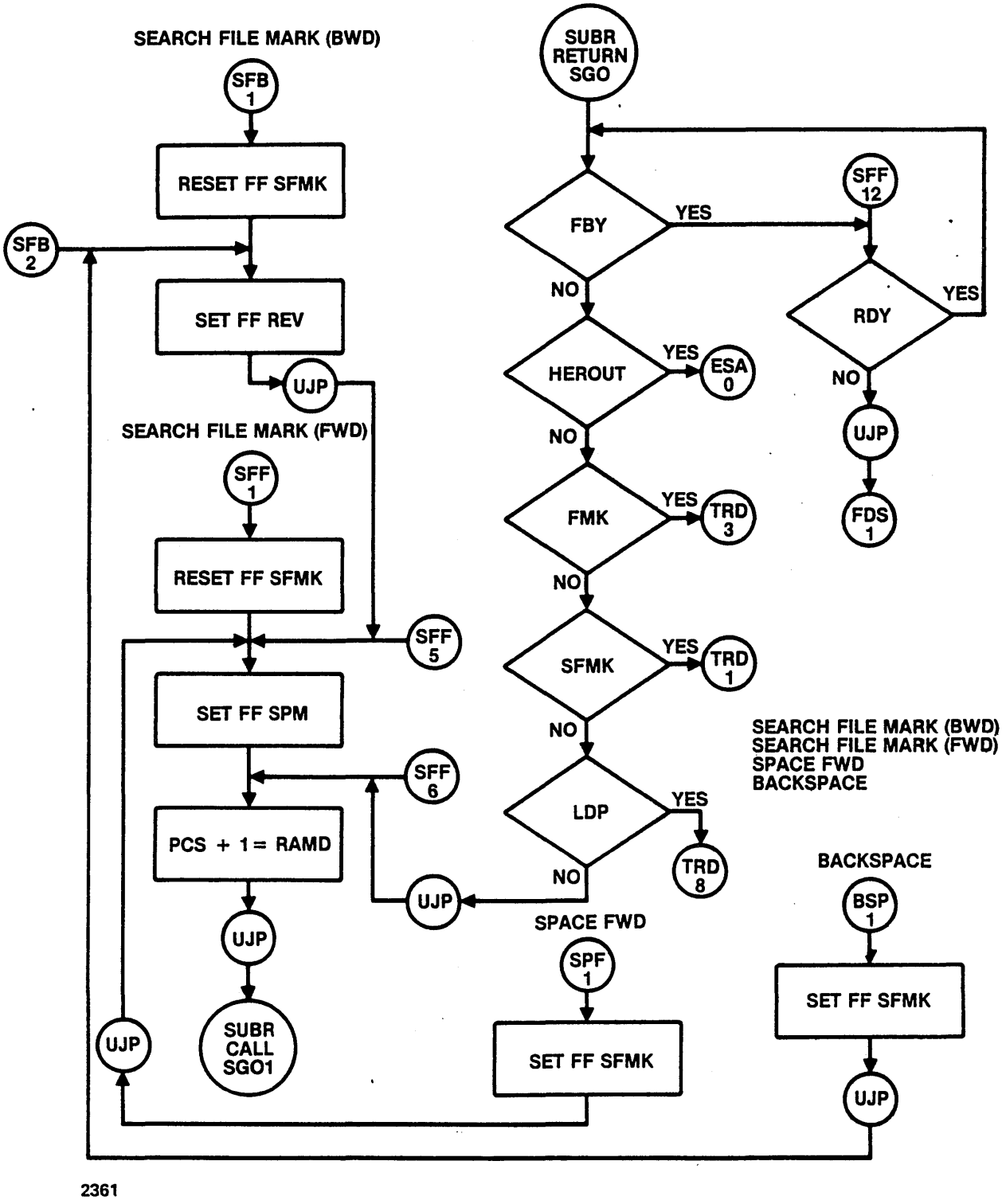


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 43 of 75)

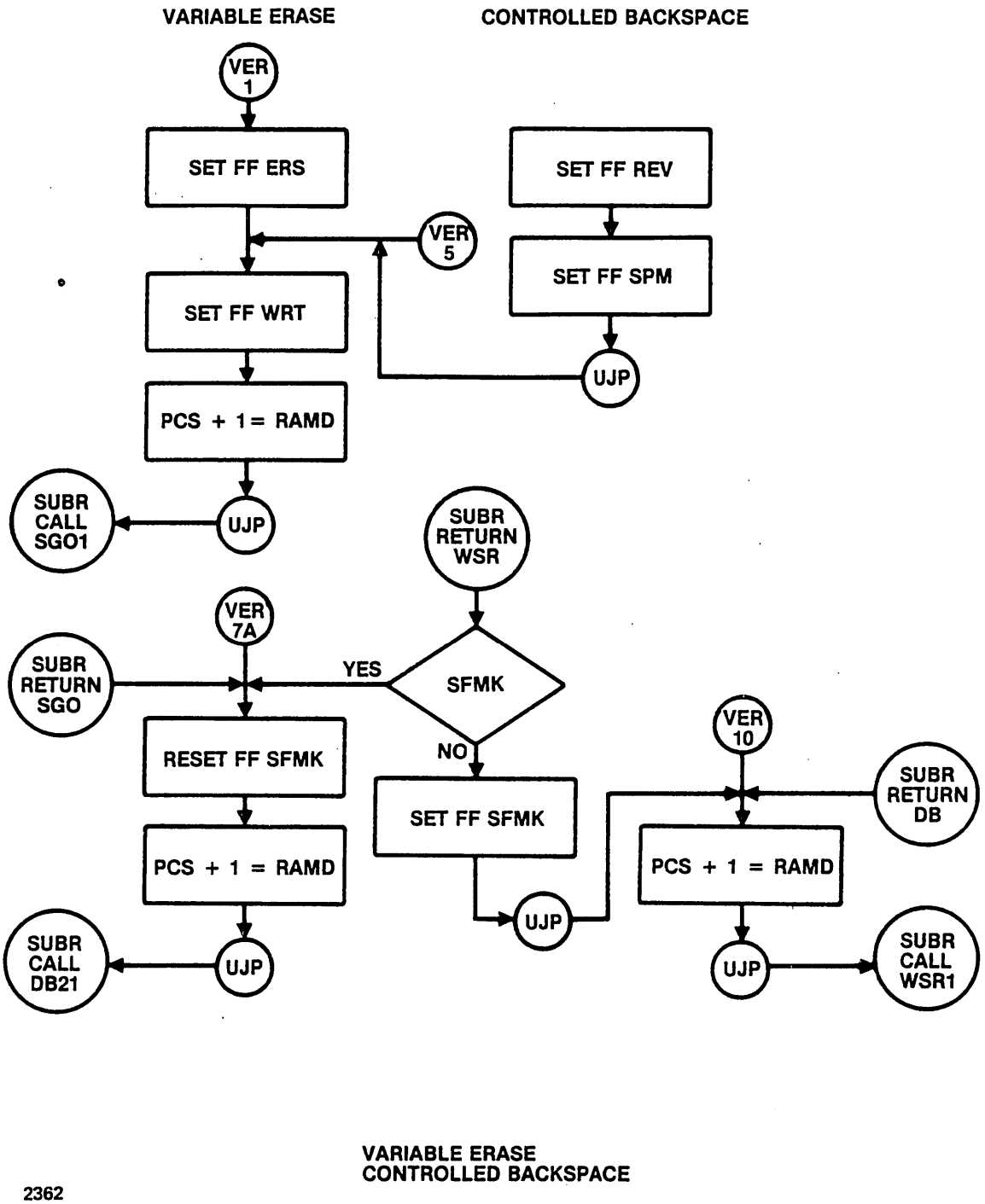


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 44 of 75)

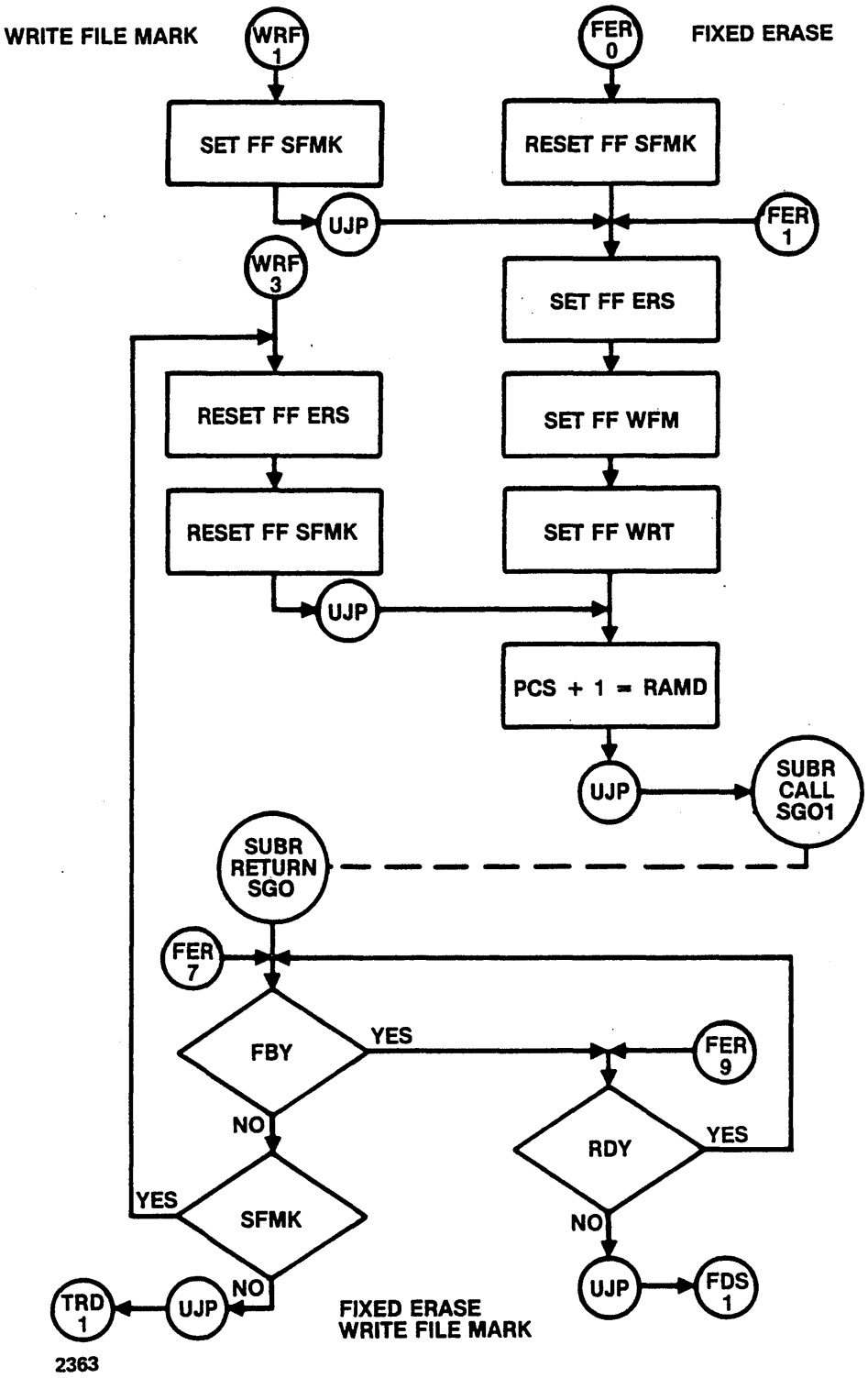
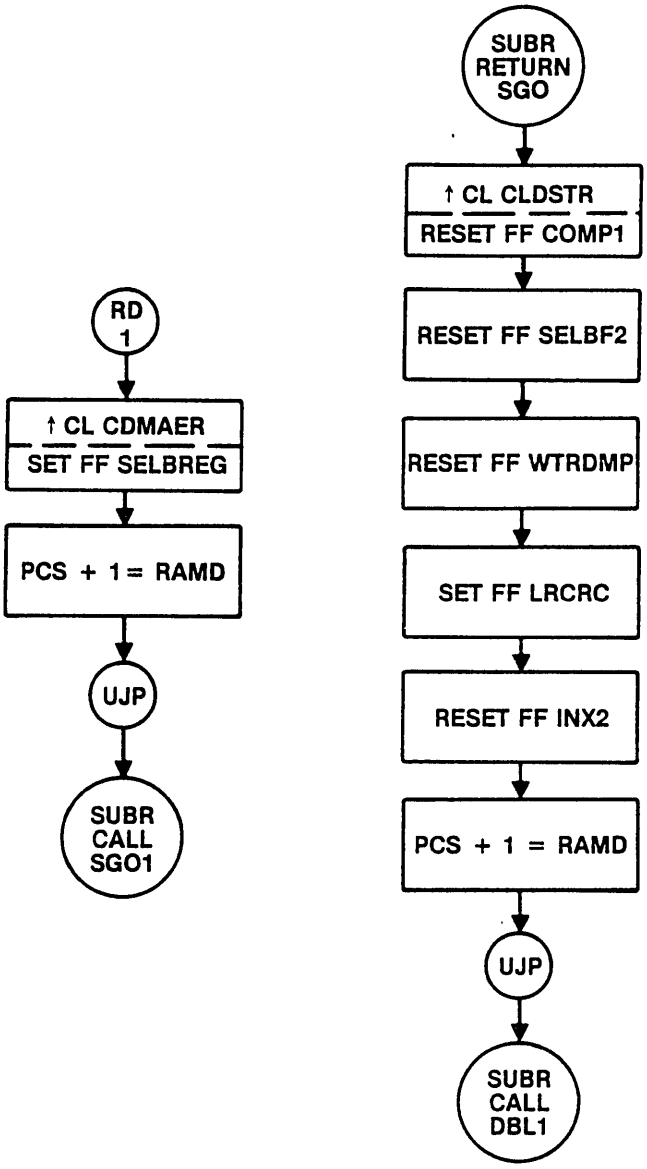


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 45 of 75)



READ DATA

2364

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 46 of 75)

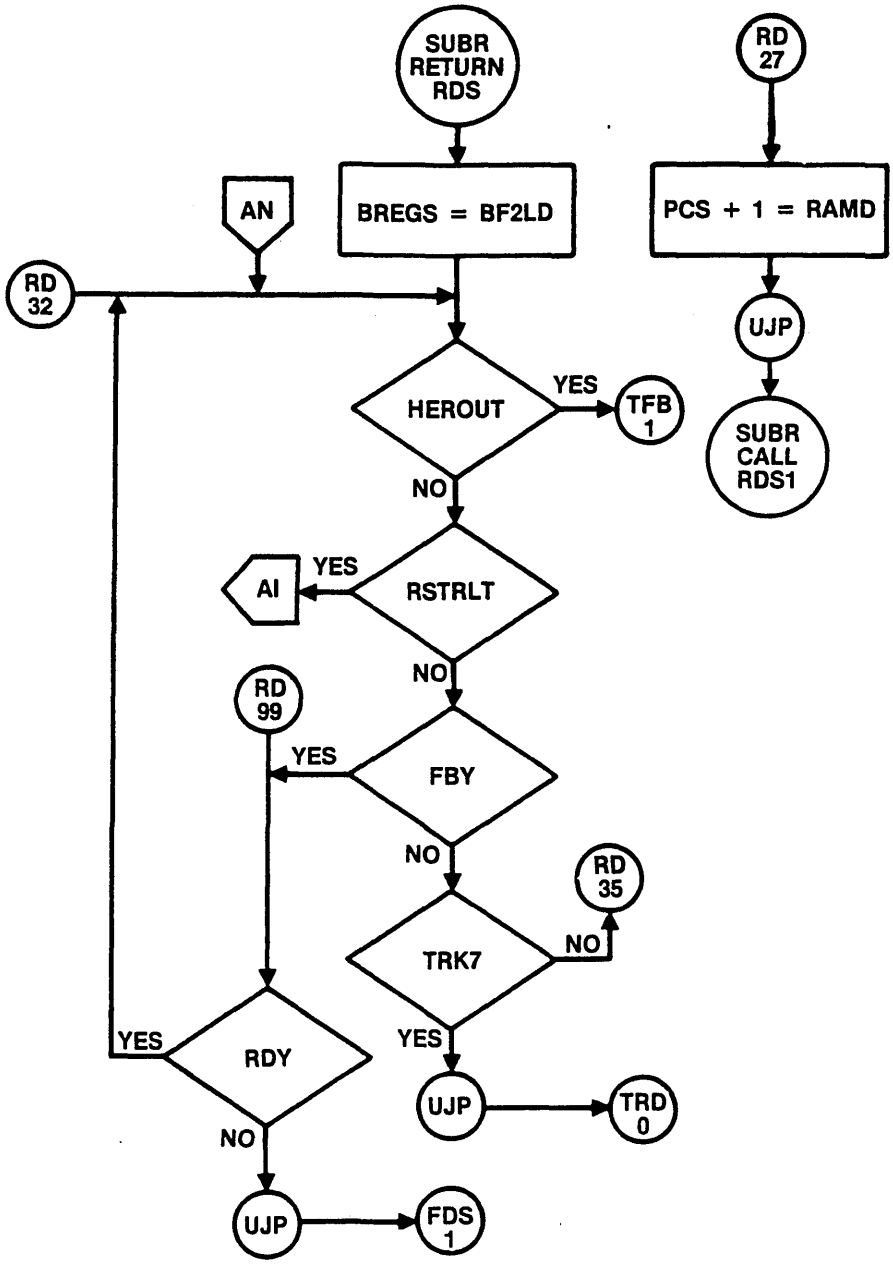


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 47 of 75)

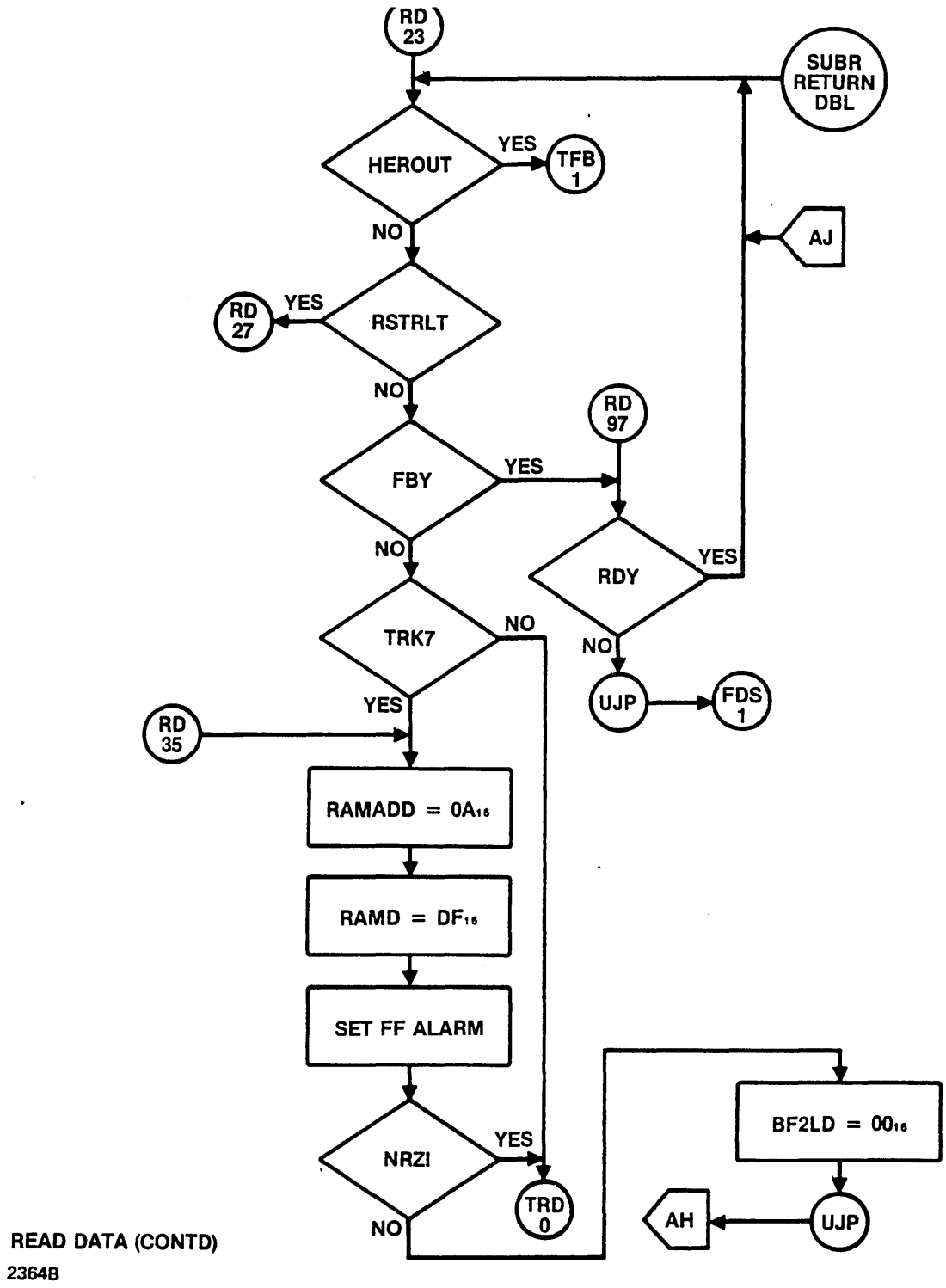
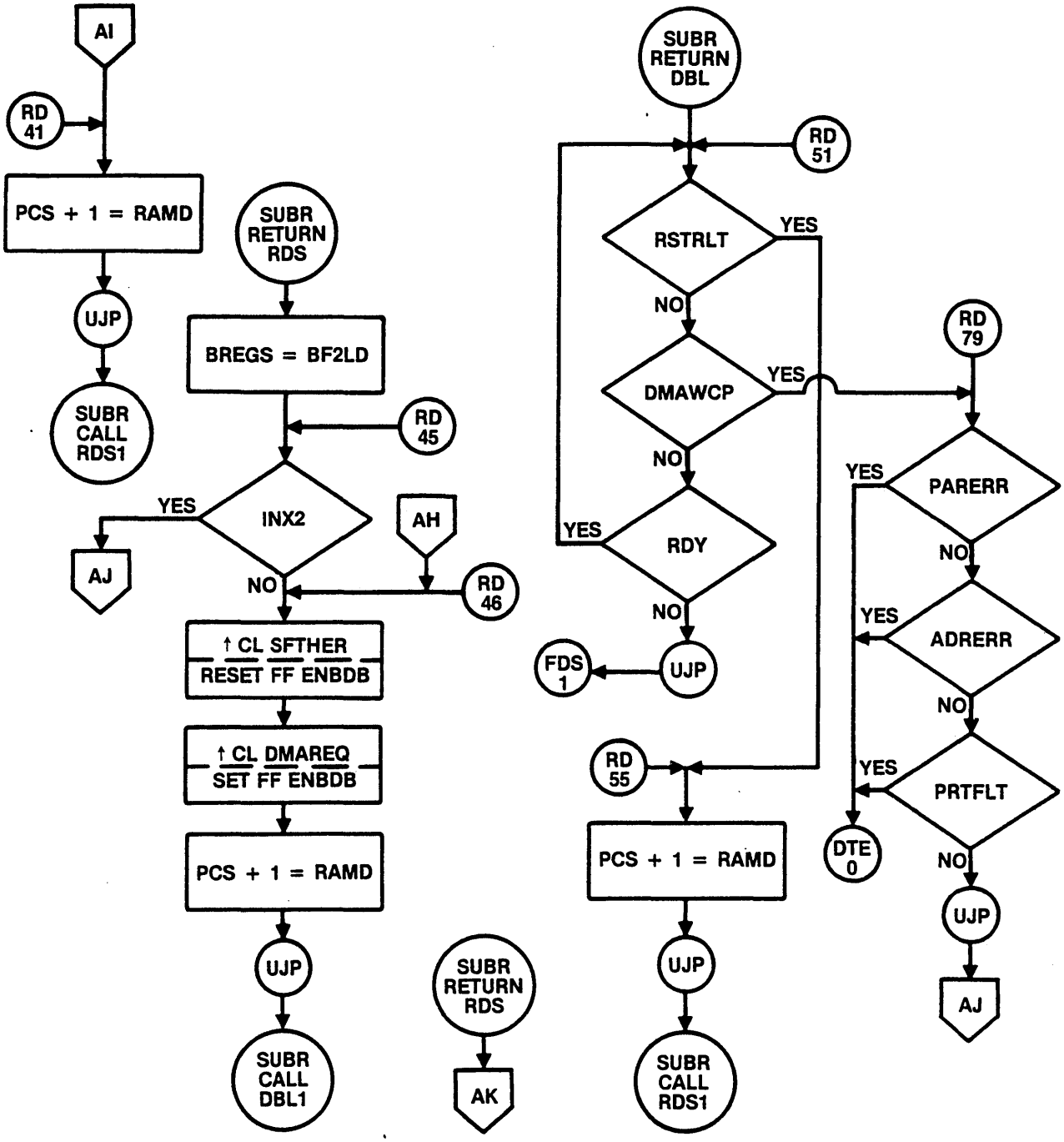


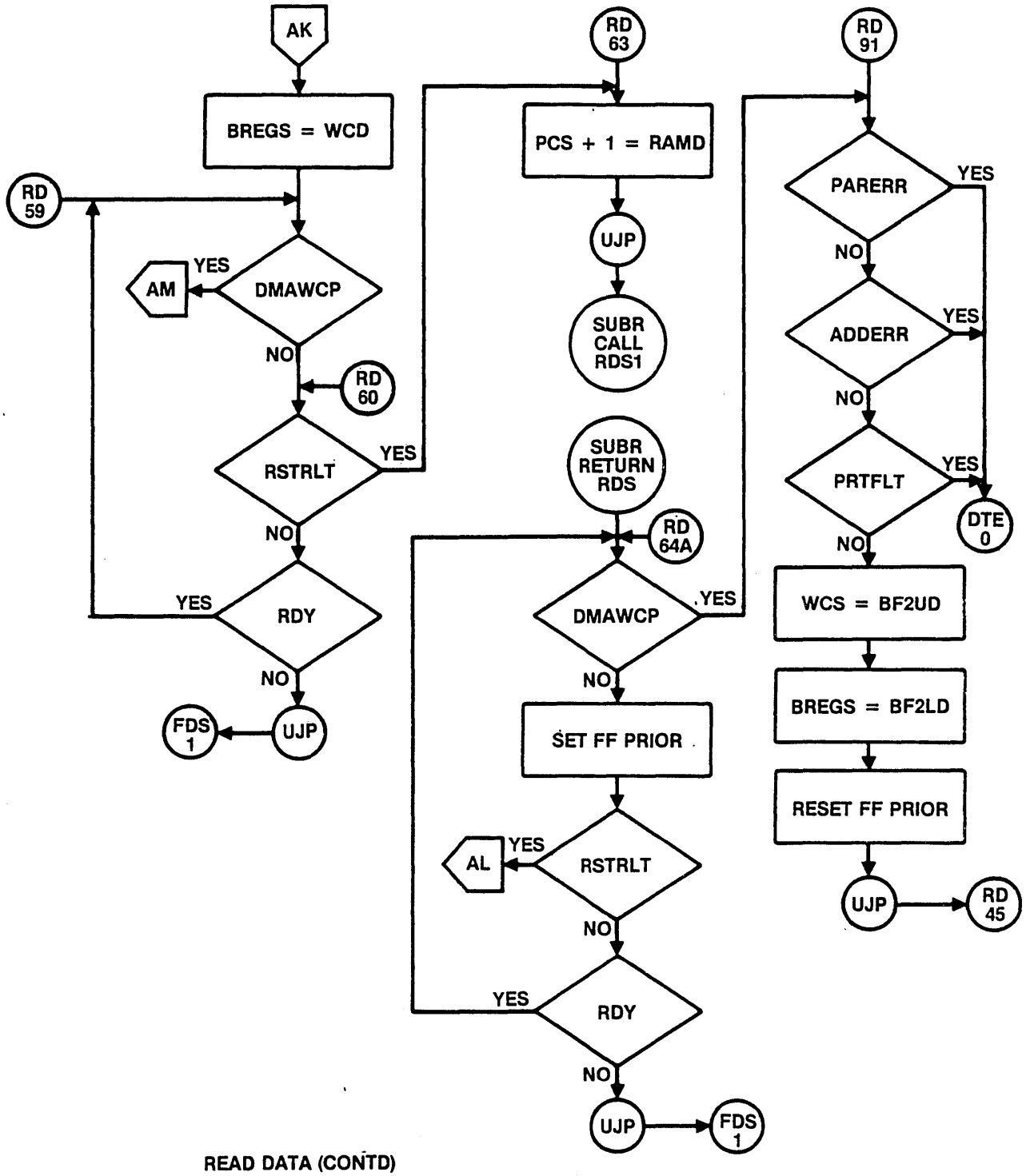
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 48 of 75)



READ DATA (CONTD)

2364C

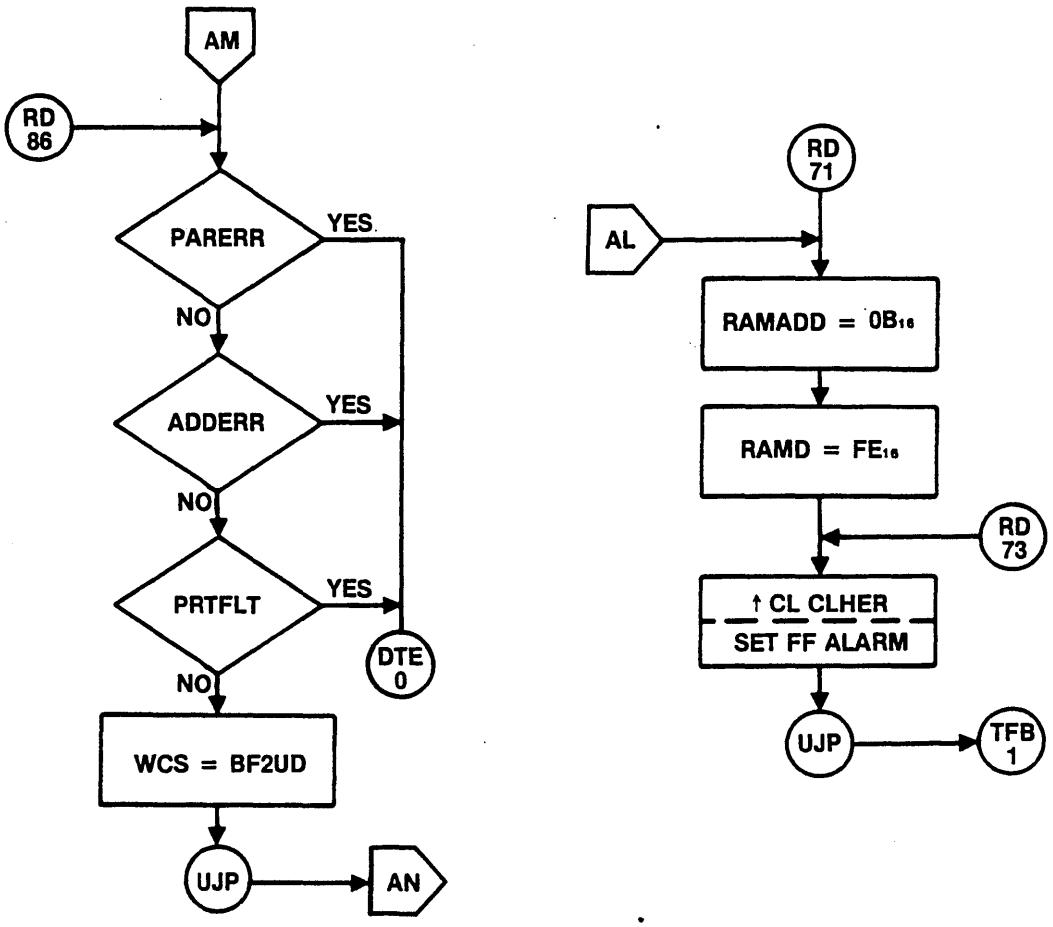
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 49 of 75)



READ DATA (CONTD)

2364D

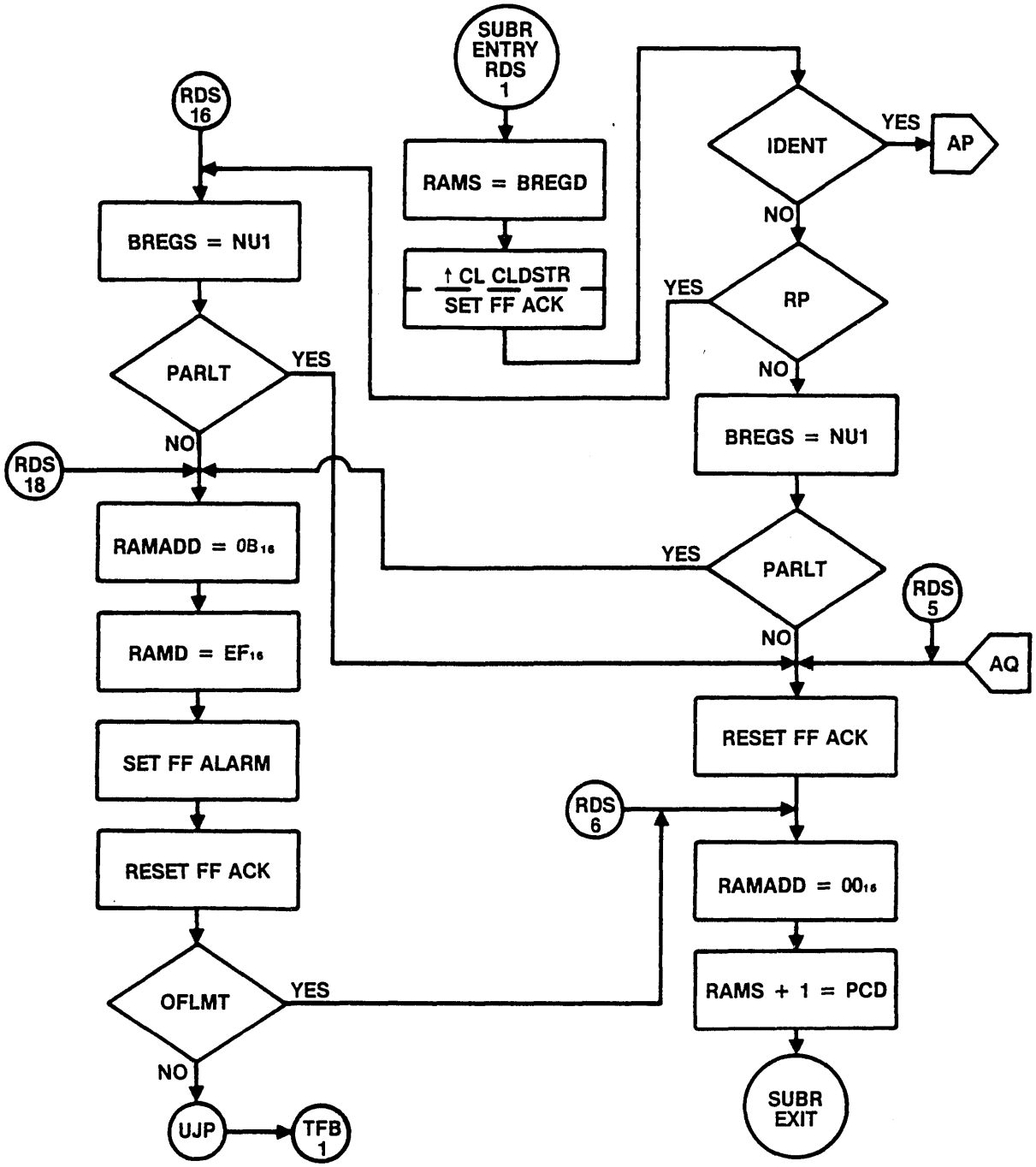
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 50 of 75)



READ DATA (CONTD)

2364E

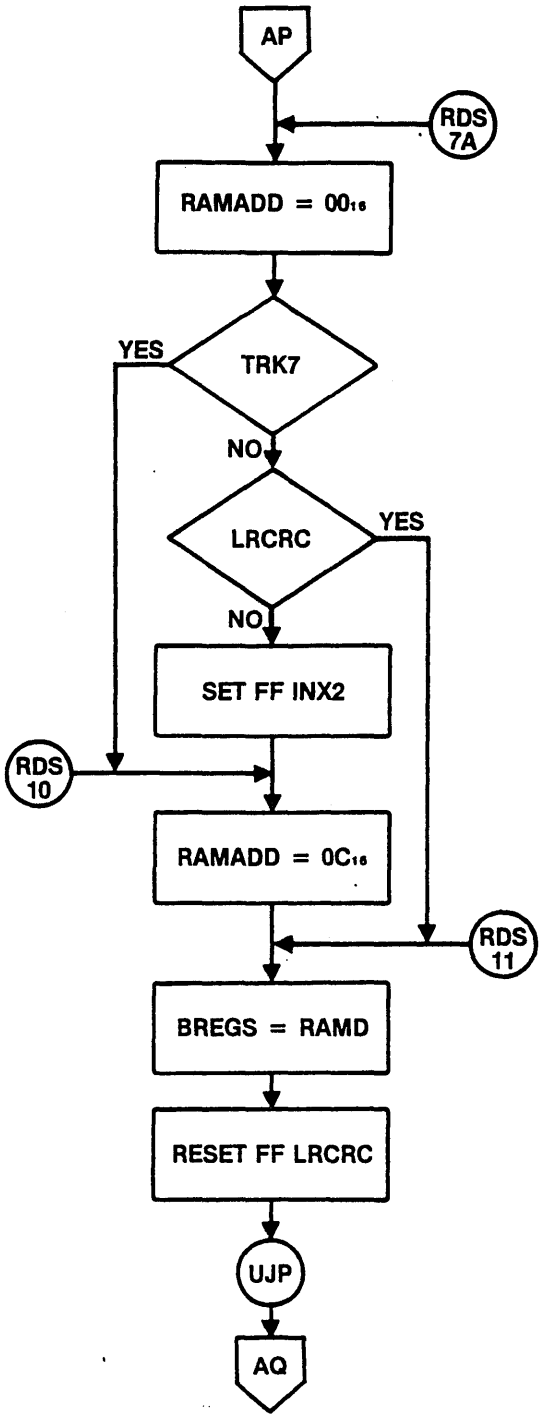
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 51 of 75)



READ STROBE SUBROUTINE

2365

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 52 of 75)



READ STROBE SUBROUTINE (CONTD)

2365A

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 53 of 75)

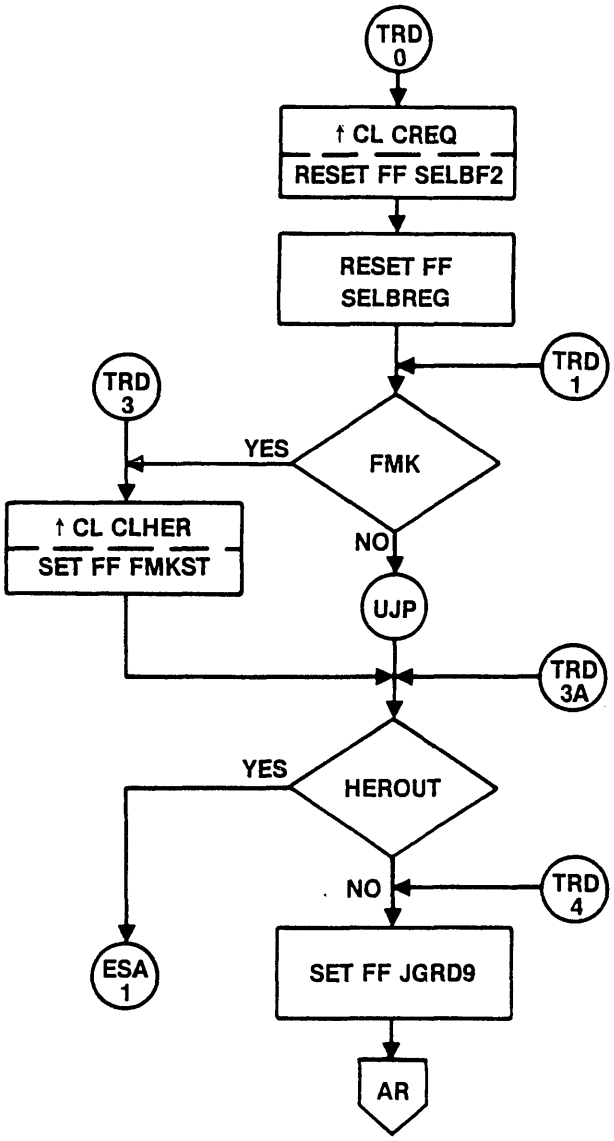
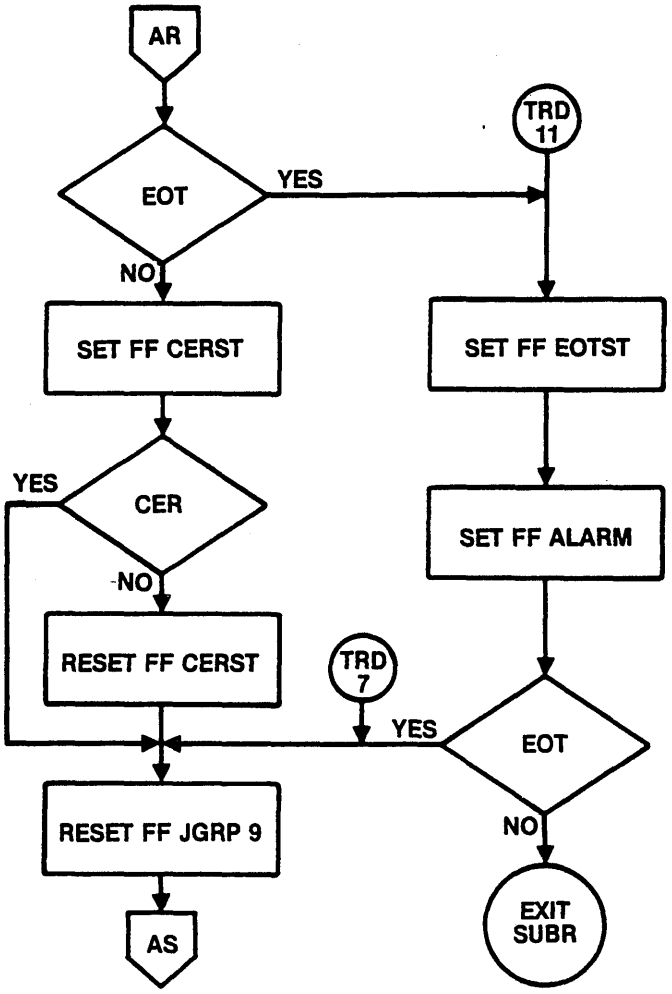


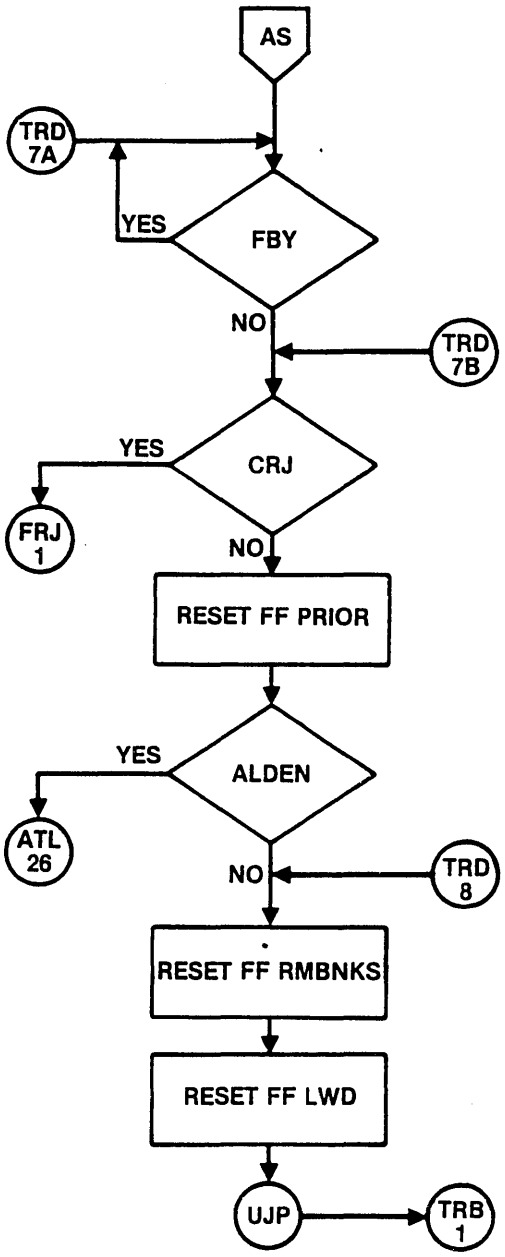
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 54 of 75)



TERMINATE READ (CONTD)

2366A

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 55 of 75)



TERMINATE READ (CONTD)

2366B

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 56 of 75)

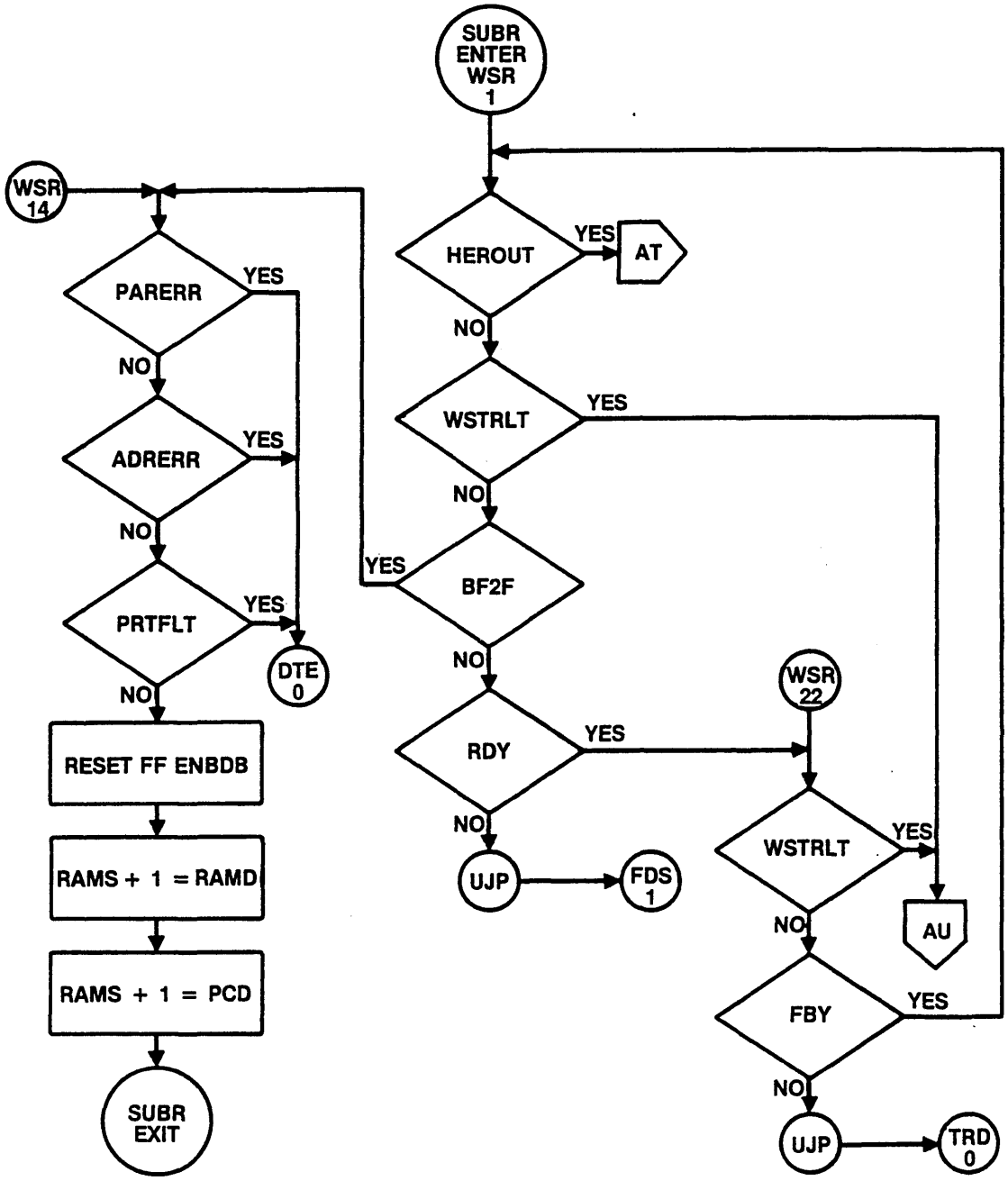


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 57 of 75)

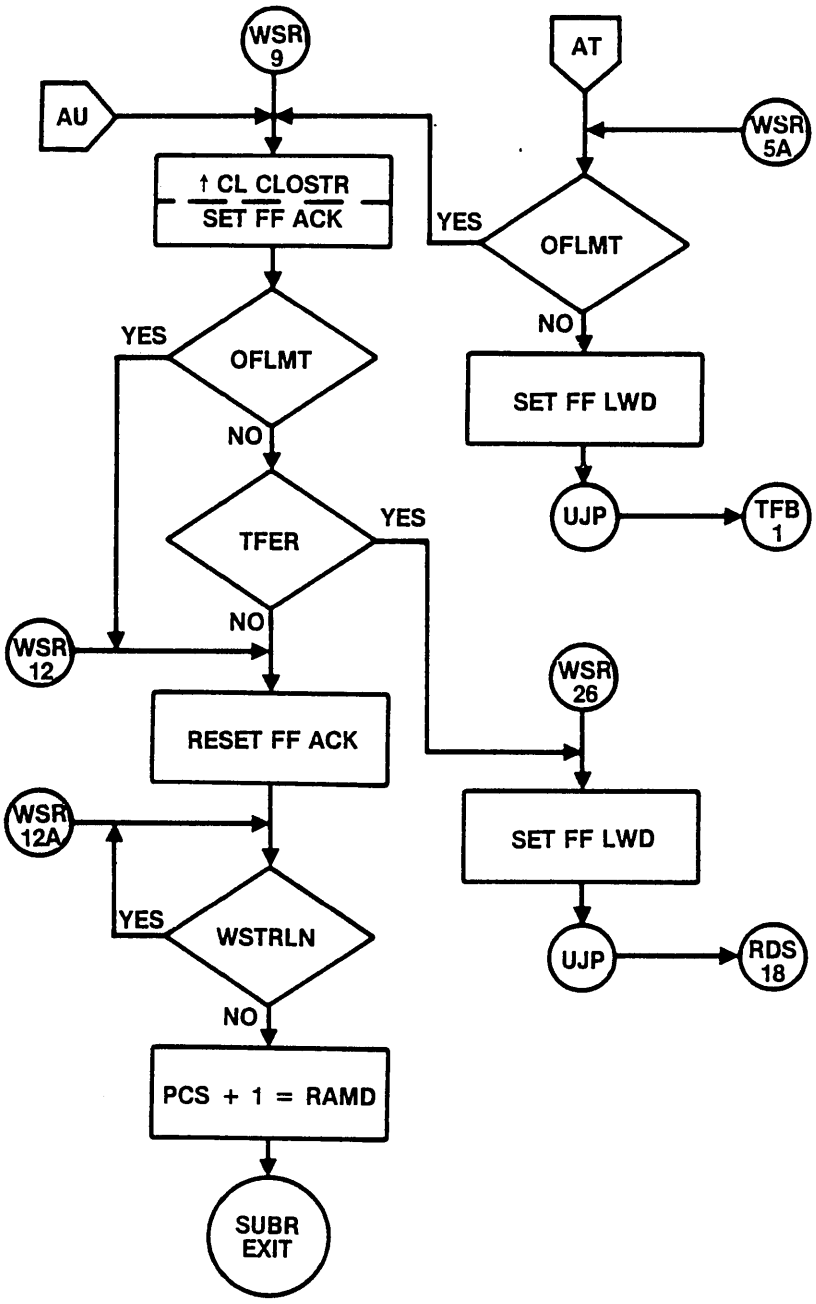


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 58 of 75)

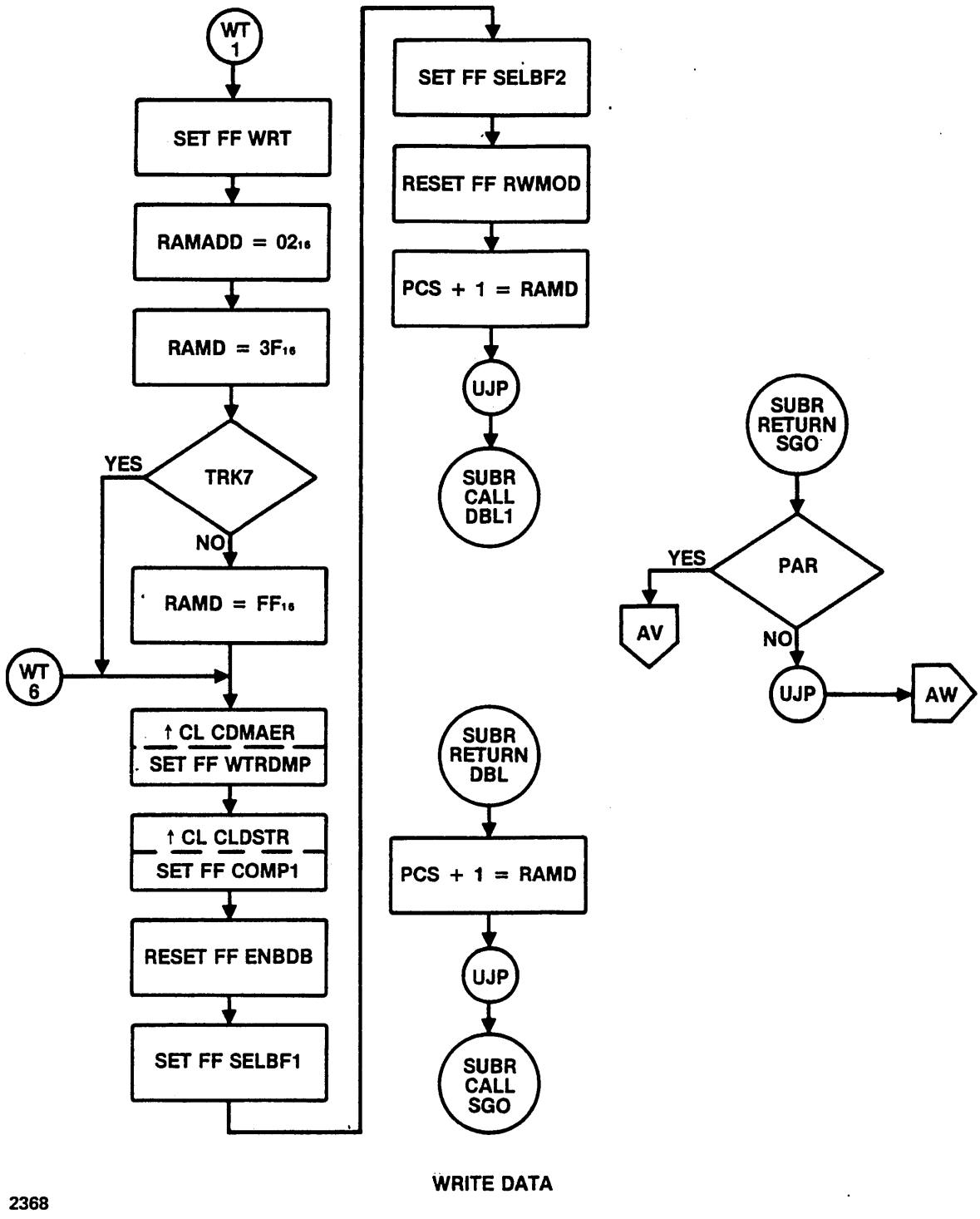
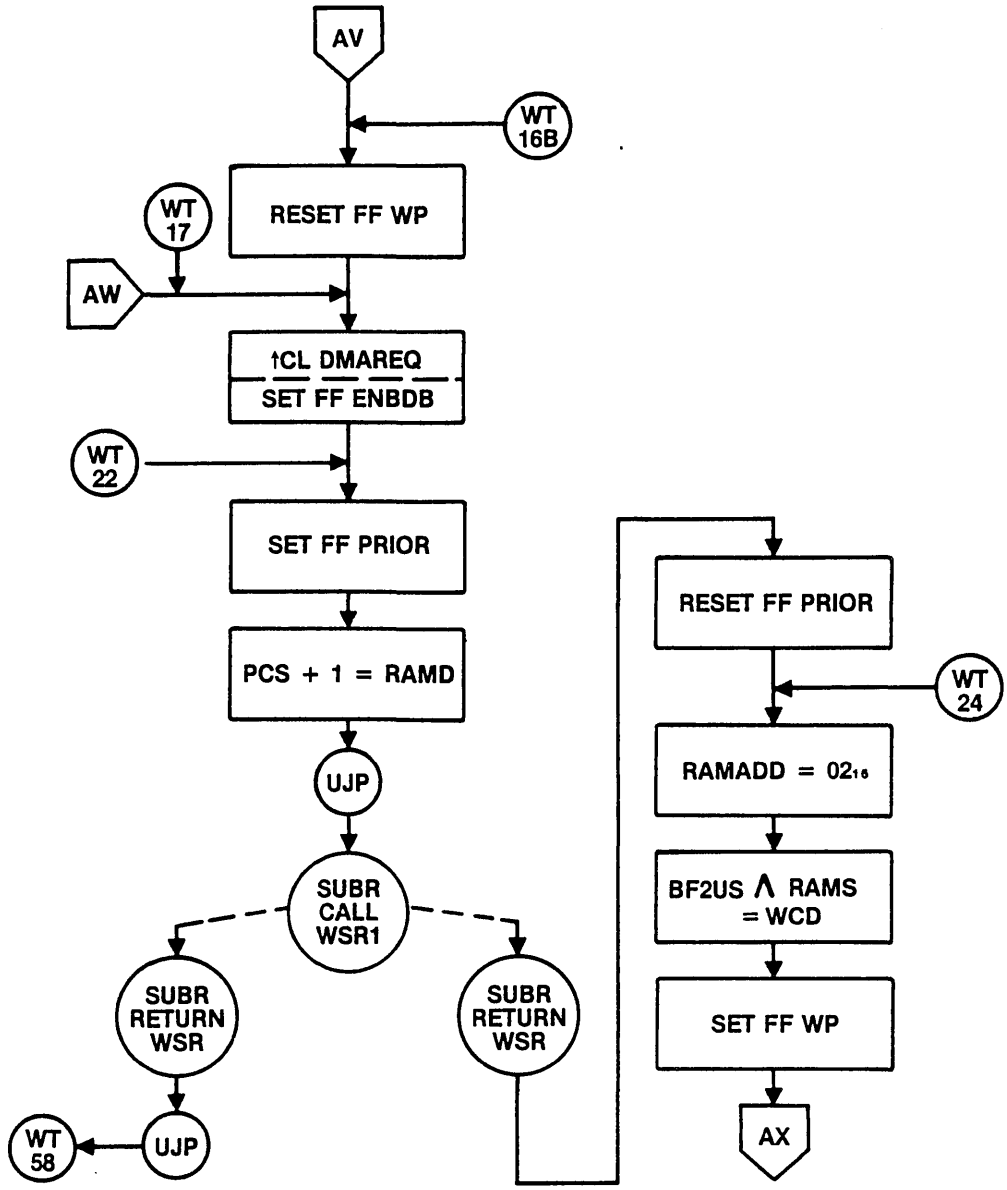


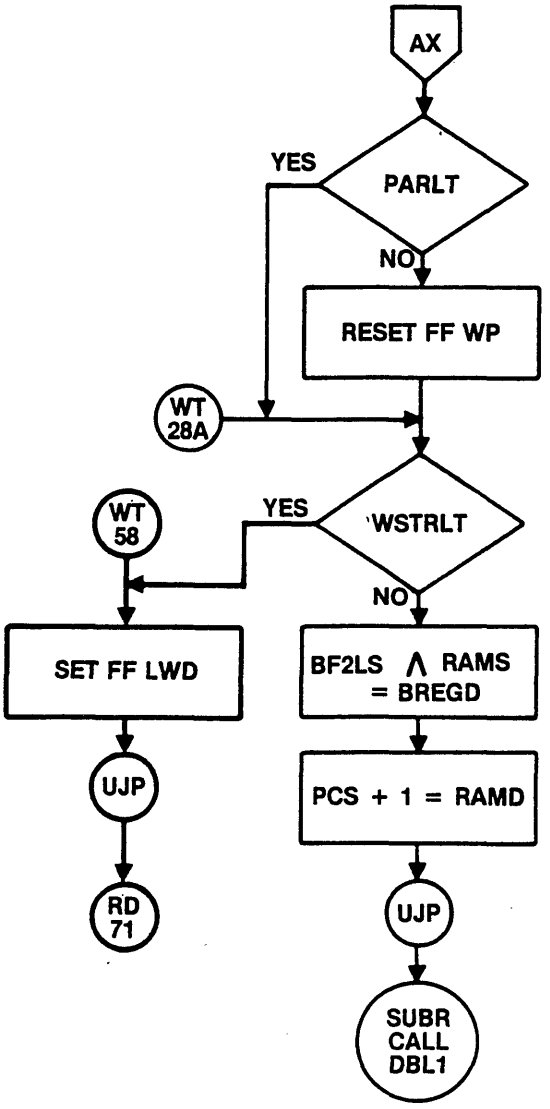
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 59 of 75)



WRITE DATA (CONTD)

2368A

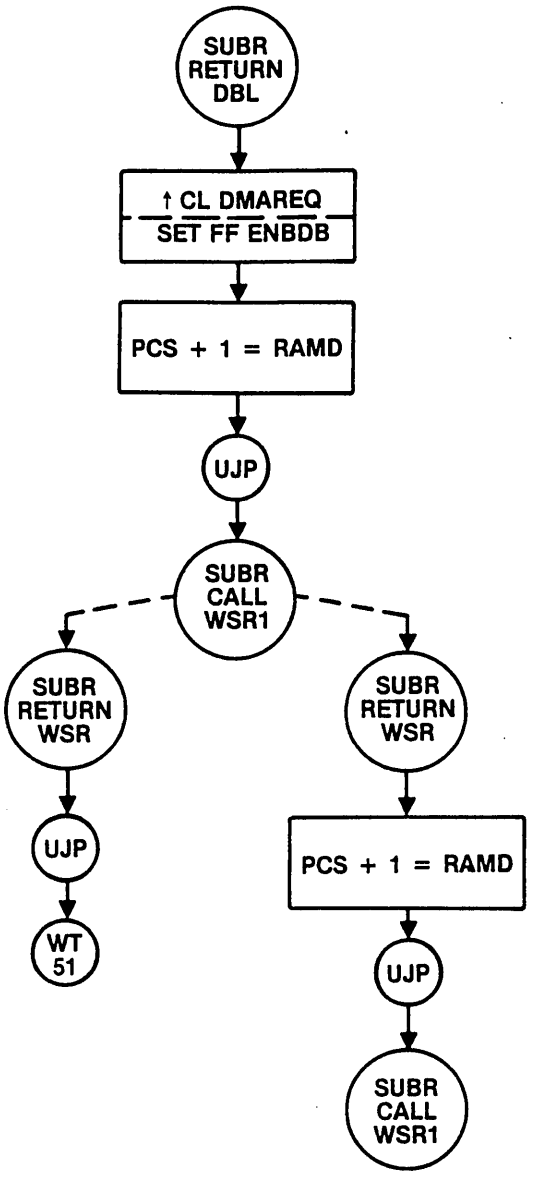
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 60 of 75)



WRITE DATA (CONTD)

2368B

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 61 of 75)



WRITE DATA (CONTD)

2368C

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 62 of 75)

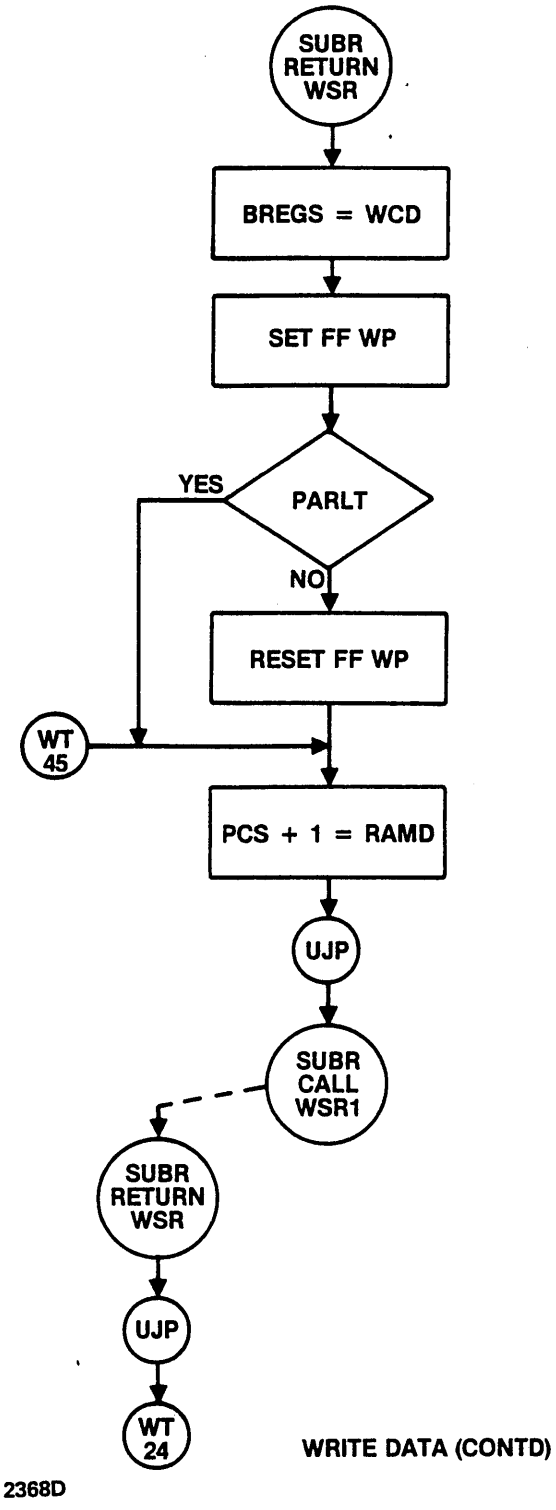


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 63 of 75)

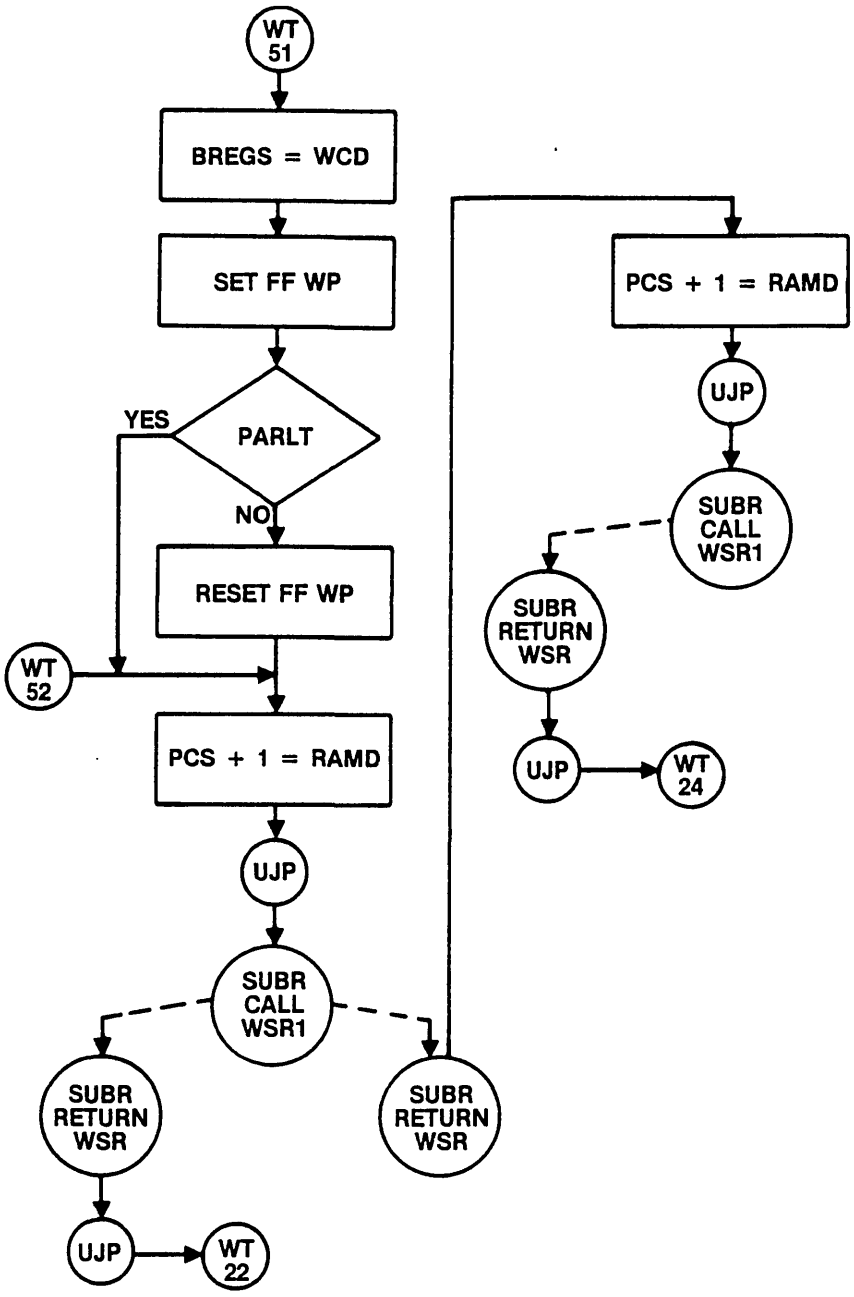


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 64 of 75)

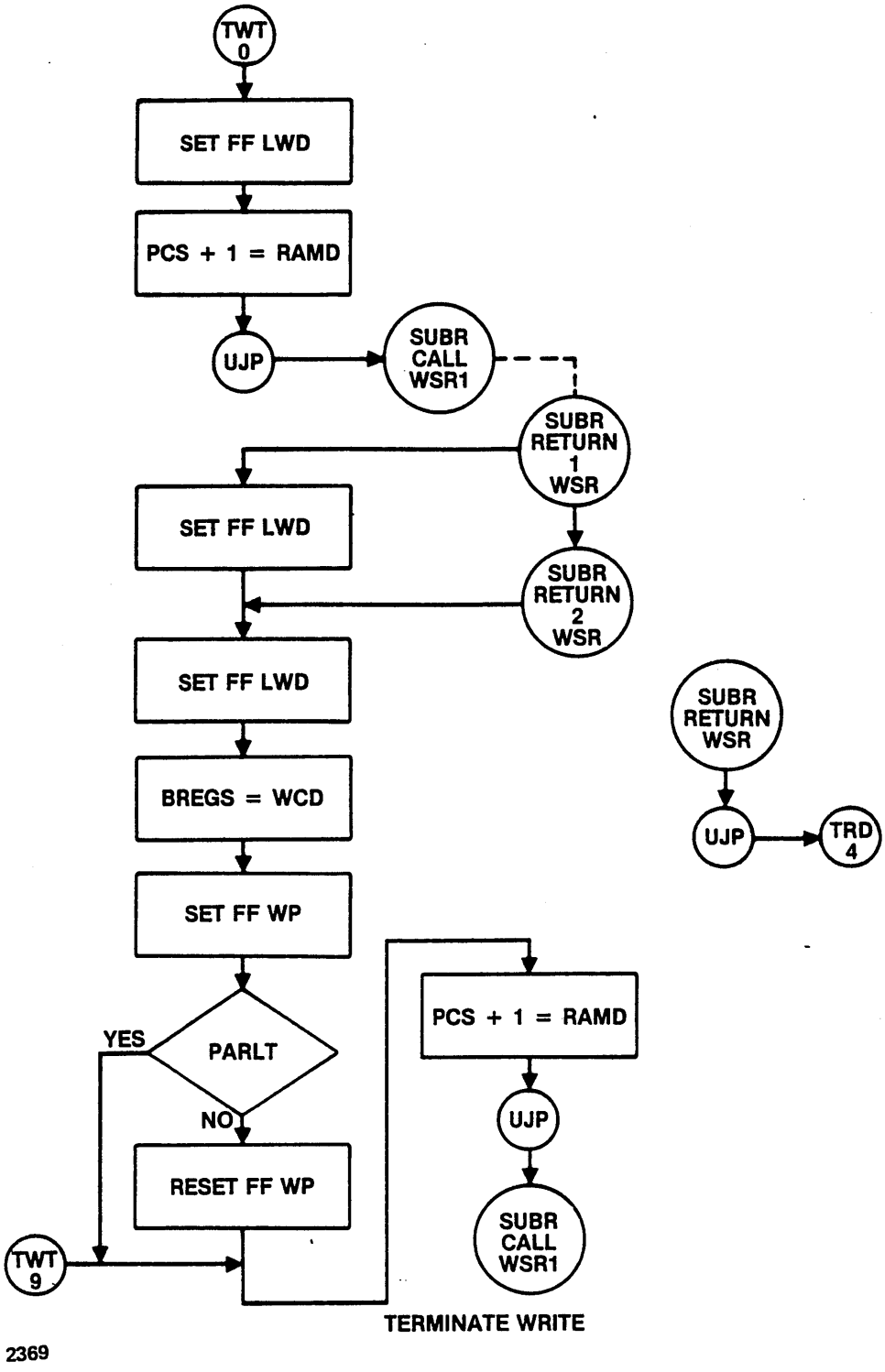
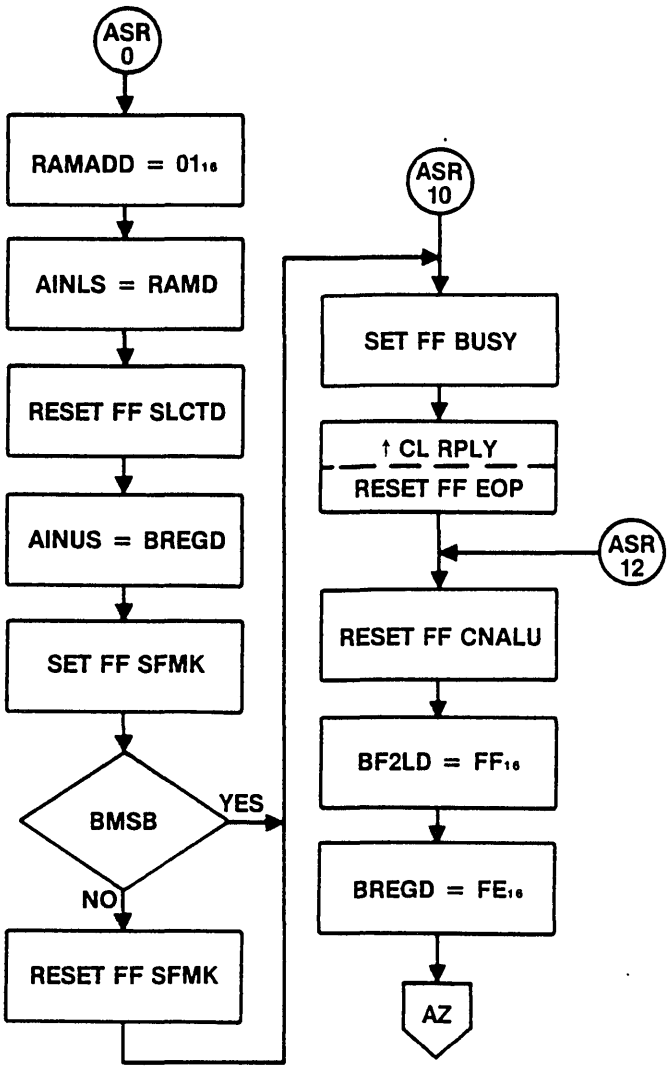


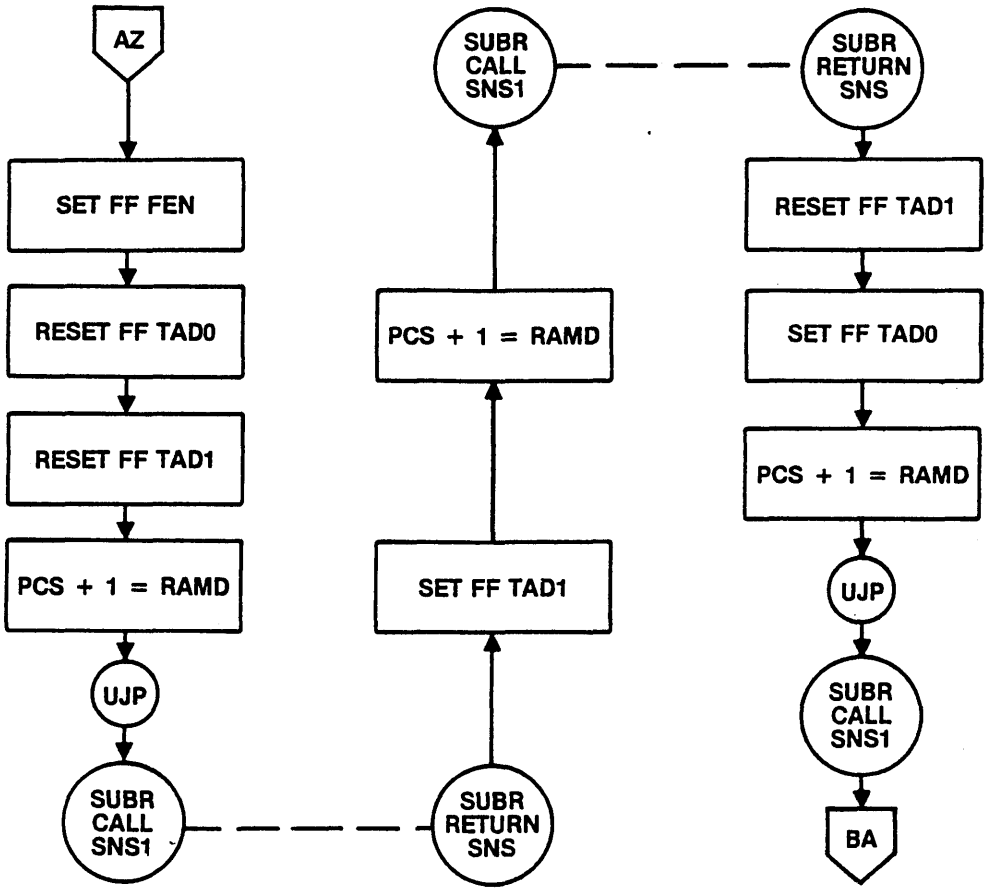
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 65 of 75)



ASSEMBLE/SENSE NEXT READY

2370

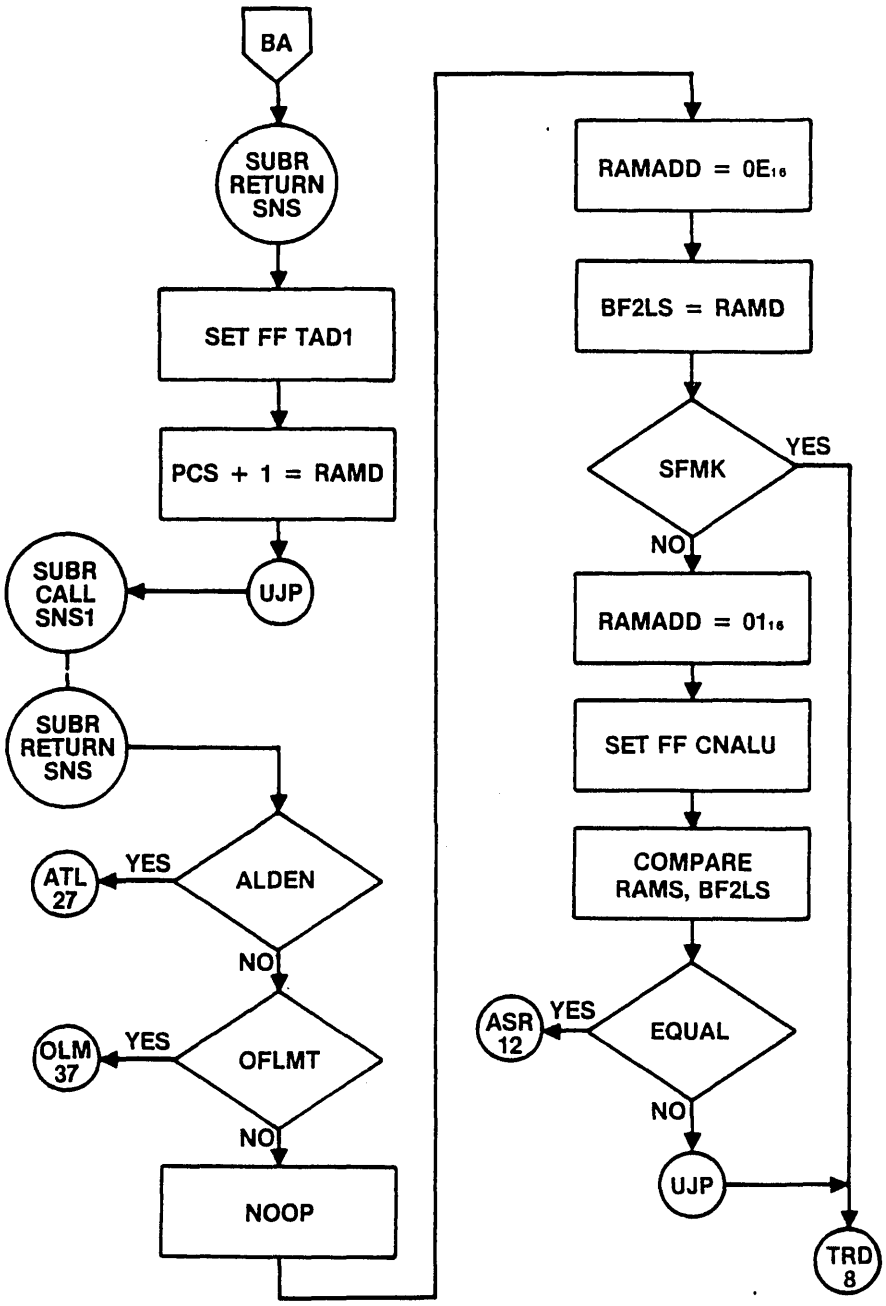
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 66 of 75)



ASSEMBLE/SENSE NEXT READY (CONTD)

2370 A

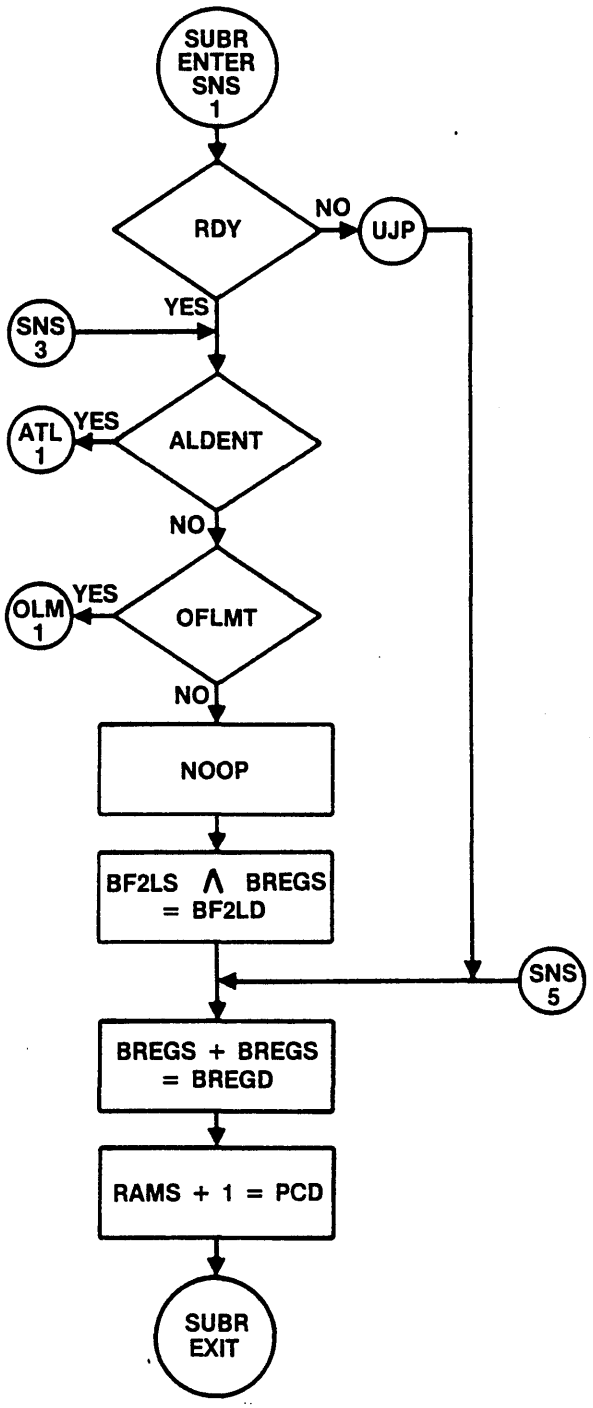
Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 67 of 75)



ASSEMBLE/SENSE NEXT READY (CONTD)

2370B

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 68 of 75)



SENSE SUBROUTINE

2371

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 69 of 75)

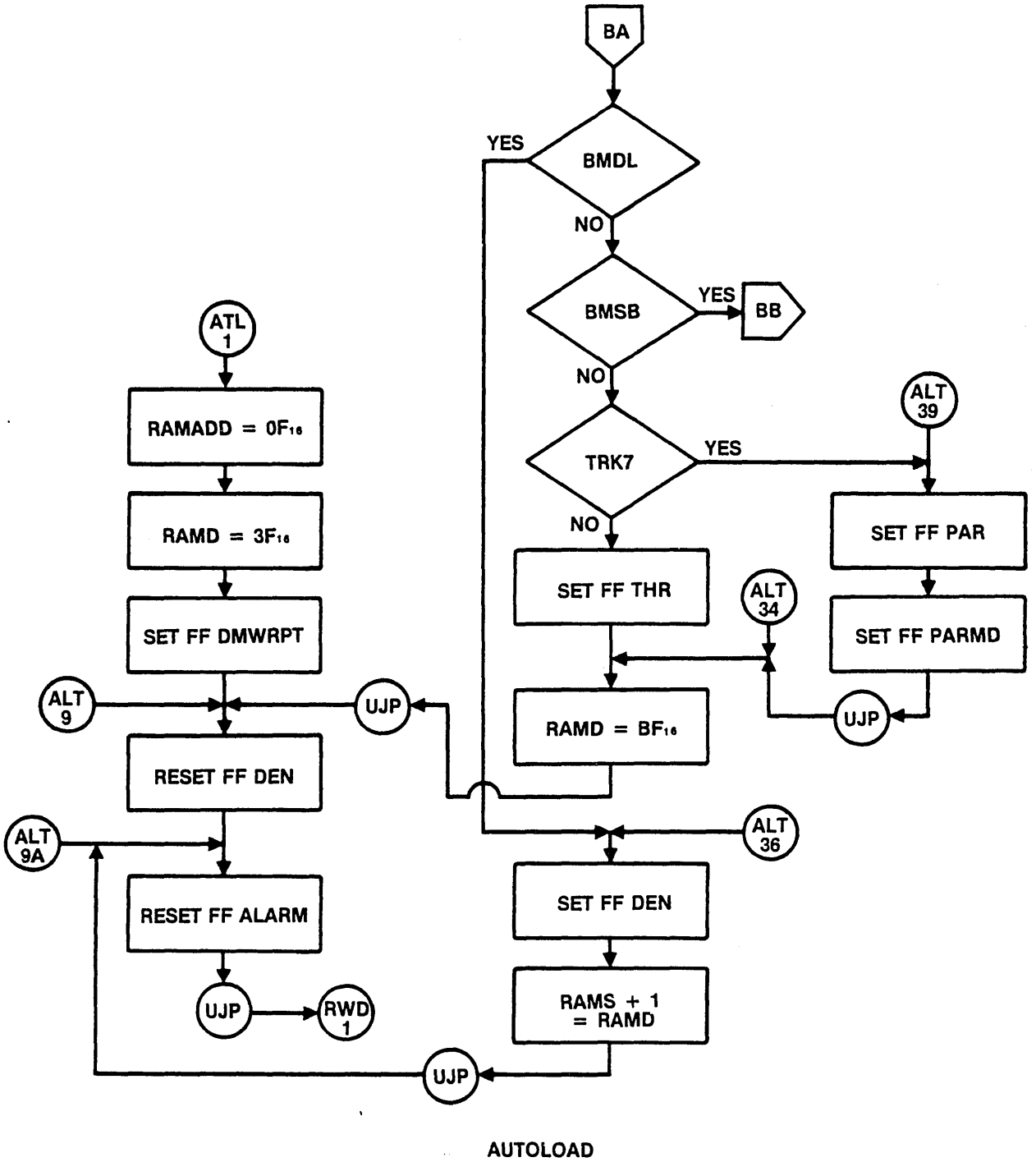


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 70 of 75)

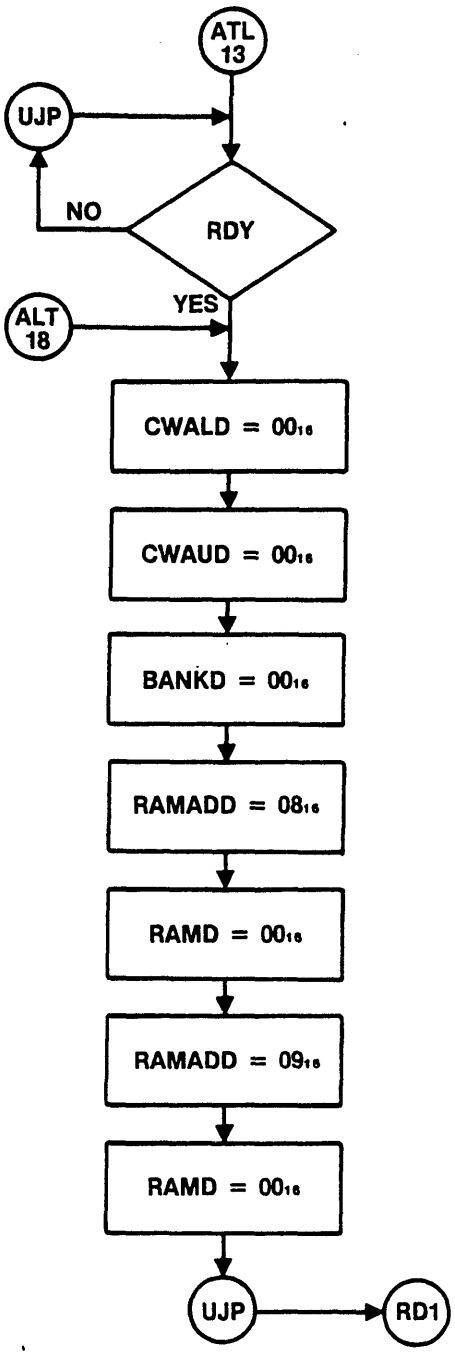
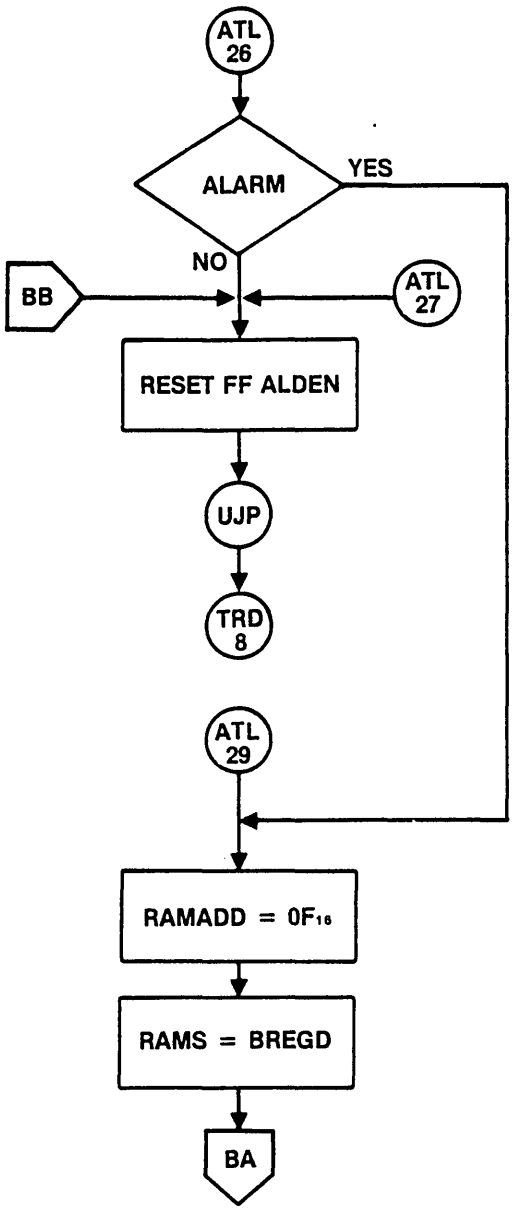


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 71 of 75)



AUTOLOAD (CONTD)

2372B

Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 72 of 75)

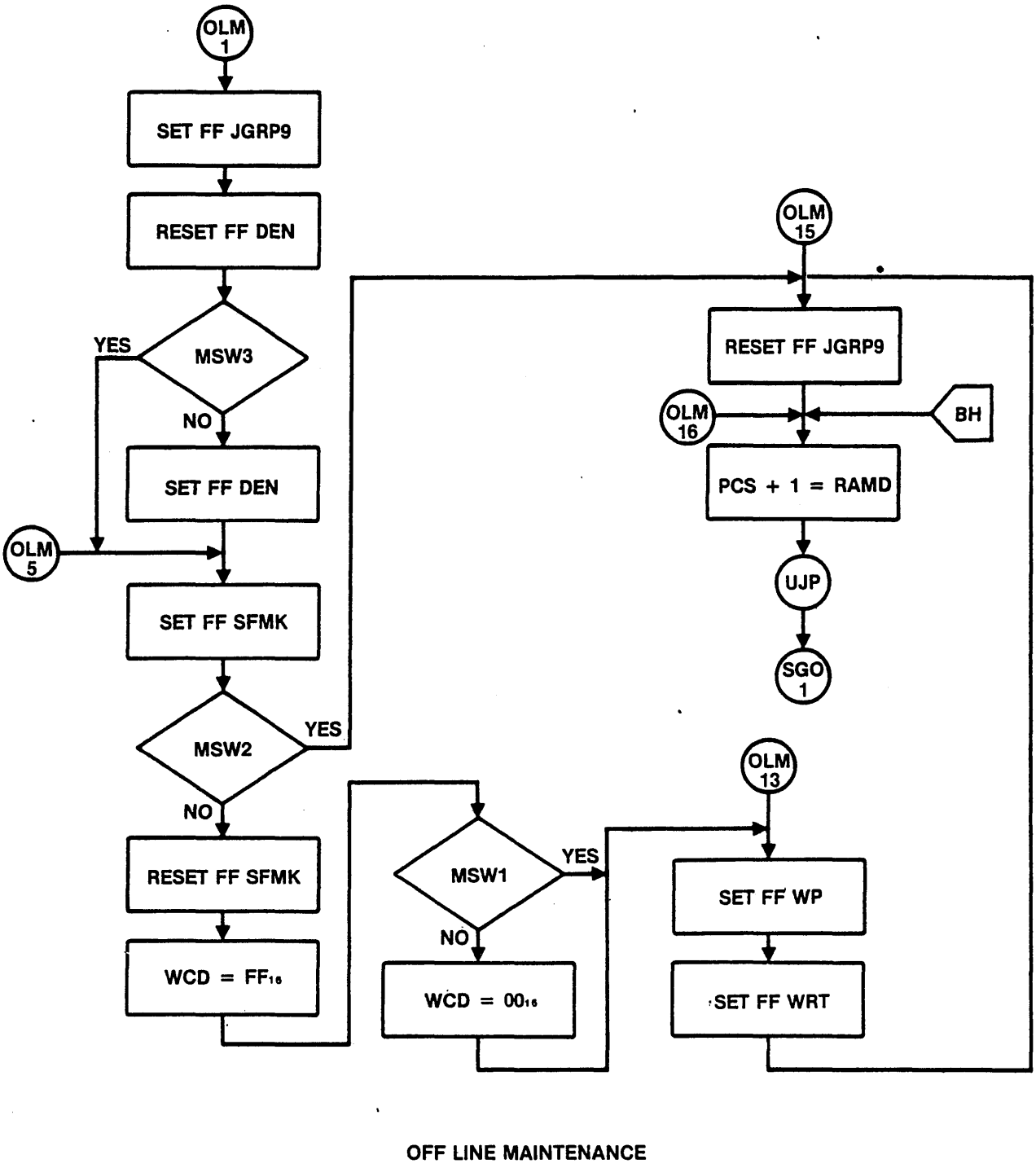


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 73 of 75)

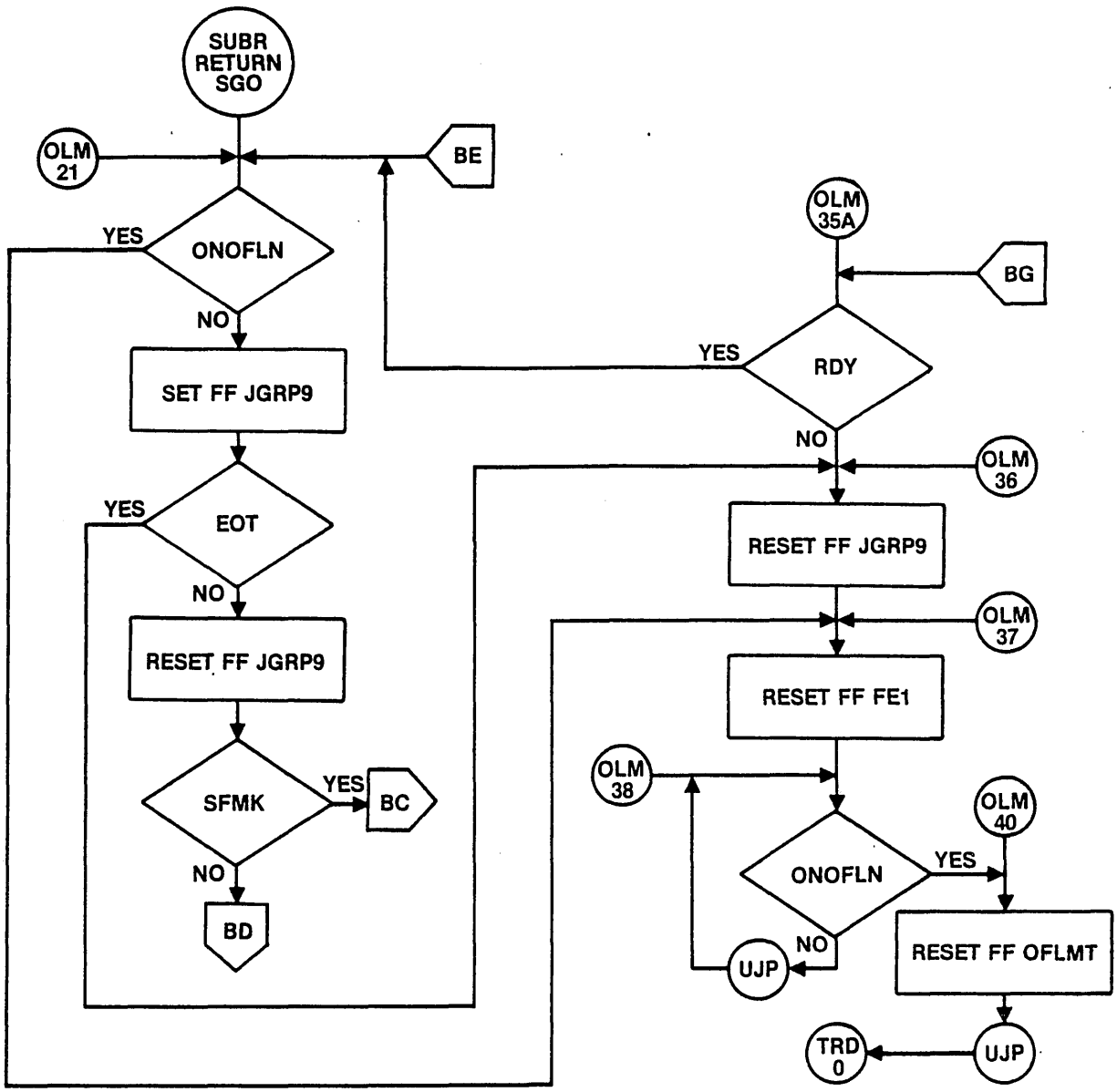


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 74 of 75)

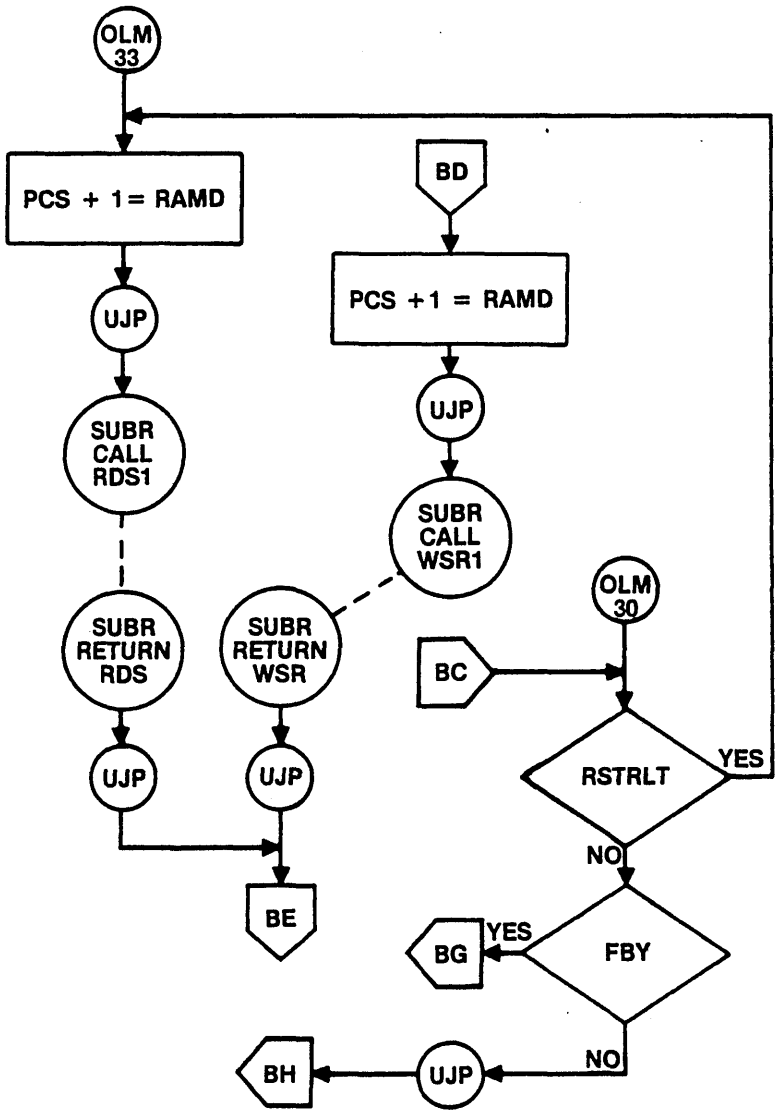


Figure B-1. Magnetic Tape Transport Controller Flow Charts (Sheet 75 of 75)

FIRMWARE LIST C

This appendix contains the firmware list for the magnetic tape transport controller. Although the firmware list specifically reflects the FA464-A MTTC, it is equally applicable to all FA464 and FA465 MTTCs.

```
FA464A          PAGE  1          DATE: 11/11/11

0001                    NAM FA464A                                      000002
0002            *                                                       000003
0003            *                                                       000004
0004            *                                                       000005
0005            ************************************************        000006
0006            ************************************************        000007
0007            **                                              **      000008
0008            **                                              **      000009
0009            **              MICRO PROGRAM ASSEMBLER         **      000010
0010            **        LCTI/FORMATTER CONTROLLER  FA464-A     **      000011
0011            **              R9601266 REVISION 04            **      000012
0012            **                                              **      000013
0013            ************************************************        000014
0014            ************************************************        000015
0015            *                                                       000016
0016            *                                                       000017
0017            *                                                       000018
0018            *               **** MACROS DEFINITIONS ****            000019
0019            *                                                       000020
0020            *                                                       000021
0021            *                                                       000022
0022            CJP     MAC     JC,JA           CONDITIONAL JUMP-IF 'JC' GO TO 'JA'     000023
0023                    VFD     N1/0,X6/'JC',X9/'JA'-START1             000024
0024                    EMC                                             000025
0025            UJP     MAC     JA              UNCONDITIONAL JUMP-GO TO 'JA'           000026
0026                    VFD     N7/0,X9/'JA'-START1                     000027
0027                    EMC                                             000028
0028            LDC     MAC     D,C             LOAD CONSTANT-LOAD 'D' BY 'C'           000029
0029                    VFD     N4/$B,X4/'D',X8/'C'                     000030
0030                    EMC                                             000031
0031            LADDR   MAC     D,AD            LOAD ADDRESS-LOAD 'D' BY                000032
0032            *                                       VALUE OF LABEL 'AD'             000033
0033                    VFD     N4/$B,X4/'D',X8/'AD'-START1             000034
0034                    EMC                                             000035
0035            SEFCL   MAC     FF,CL           SET FLIP FLOP & CONTROL LINE            000036
0036            *                               SET 'FF' & PROVIDE PULSE ON 'CL'        000037
0037                    VFD     N4/$B,X4/'CL',N2/0,X6/'FF'              000038
0038                    EMC                                             000039
0039            *                                                       000040
0040            *                                                       000041
0041            *                                                       000042
0042            *                                                       000043
0043            *                                                       000044
0044            *                                                       000045
0045            *                                                       000046
0046            *                                                       000047
0047            *                                                       000048
0048            *                                                       000049
0049            *                                                       000050
0050            *                                                       000051
0051            *                                                       000052
0052            *                                                       000053
0053            *                                                       000054
```

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0054        RFFCL  MAC   FF,CL                RESET FLIP FLOP & CONTROL LINE      000055
0055        *                          RESET 'FF' & PROVIDE  PULSE ON 'CL'         000056
0056               VFD   N4/$A,X4/'CL',N2/0,X6/'FF'                                000057
0057               EMC                                                             000058
0058        CLO    MAC   CL                  CONTROL LINE (ONLY)-                 000059
0059        *                                      PROVIDE  PULSE ON 'CL'          000060
0060               VFD   N4/$B,X4/'CL',N8/$FF                                      000061
0061               EMC                                                             000062
0062        CLO1   MAC   CL                  CONTROL LINE (ONLY)-                 000063
0063        *                                      PROVIDE  PULSE ON 'CL'          000064
0064               VFD   N4/$A,X4/'CL',N8/$FF                                      000065
0065               EMC                                                             000066
0066        SFF    MAC   FF                  SET FLIP FLOP-SET 'FF'              000067
0067               VFD   N10/$2FC,X6/'FF'                                          000068
0068               EMC                                                             000069
0069        RFF    MAC   FF                  RESET FLIP FLOP-RESET 'FF'          000070
0070               VFD   N10/$2BC,X6/'FF'                                          000071
0071               EMC                                                             000072
0072        *                                                                      000073
0073        *                                                                      000074
0074        *                                                                      000075
0075        *                ** INTER REGISTER LOGICAL FUNCTIONS **                000076
0076        *                                                                      000077
0077        *                                                                      000078
0078        *                                                                      000079
0079        TA     MAC   SA,D                 TRANSFER A:   SA--->D               000080
0080               VFD   N4/$C,X4/'D',N5/$1E,X3/'SA'                               000081
0081               EMC                                                             000082
0082        CA     MAC   SA,D                 COMPLEMENT A:  SA/--->D             000083
0083               VFD   N4/$C,X4/'D',N5/$0,X3/'SA'                                000084
0084               EMC                                                             000085
0085        TB     MAC   SB,D                 TRANSFER B:    SB--->D              000086
0086               VFD   N2/$3,X2/'SB',X4/'D',N8/$A0                               000087
0087               EMC                                                             000088
0088        TB1    MAC   SB,D                 TRANSFER B:    SB--->D              000089
0089               VFD   N2/$3,X2/'SB',X4/'D',N8/$A7                               000090
0090               EMC                                                             000091
0091        CB     MAC   SB,D                 COMPLEMENT B:  SB/--->D             000092
0092               VFD   N2/$3,X2/'SB',X4/'D',N8/$50                               000093
0093               EMC                                                             000094
0094        *                                                                      000095
0095        *                                                                      000096
0096        *                                                                      000097
0097        *                                                                      000098
0098        *                                                                      000099
0099        *                                                                      000100
0100        *                                                                      000101
0101        *                                                                      000102
0102        *                                                                      000103
0103        *                                                                      000104
0104        *                                                                      000105
0105        *                                                                      000106
0106        *                                                                      000107
```

```
            *
            CLEAR    MAC    D                          CLEAR     :   00--->D
                     VFD    N4/$F,X4/'D',N8/$35
                     EMC
            SETONE   MAC    D                          SET TO ONE:   FF--->D
                     VFD    N4/$F,X4/'D',N8/$C5
                     EMC
            OR       MAC    SA,SB,D                    OR:   SA.OR.SB--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$1C,X3/'SA'
                      EMC
            COR      MAC    SA,SB,D          COMPLEMENT OR (NOR): (SA.OR.SB)/--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$2,X3/'SA'
                     EMC
            ORCA     MAC    SA,SB,D              OR COMPLEMENT B: SA.OR.(SB/)--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$10,X3/'SA'
                     EMC
            ORCB     MAC    SA,SB,D            OR COMPLEMENT A: (SA/).OR.SB--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$1A,X3/'SA'
                     EMC
            XOR      MAC    SA,SB,D                    EXCLUSIVE OR:  SA.XOR.SB--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$C,X3/'SA'
                     EMC
            CXOR     MAC    SA,SB,D                    COMPLEMENT EXCLUSIVE OR:
            *                                                 (SA.XOR.SB)/--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$12,X3/'SA'
                     EMC
            ANDAB    MAC    SA,SB,D                    AND A B:   SA.AND.SB--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$16,X3/'SA'
                     EMC
            CAND     MAC    SA,SB,D                    COMPLEMENT AND (NAND):
            *                                                 (SA.AND.SB)/--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$8,X3/'SA'
                     EMC
            ANDCA    MAC    SA,SB,D            AND COMPLEMENT A: (SA/).AND.SB--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$4,X3/'SA'
                     EMC
            ANDCB    MAC    SA,SB,D                    AND COMPLEMENT B:
            *                                               SA.AND.(SB/)--->D
                     VFD    N2/$3,X2/'SB',X4/'D',N5/$E,X3/'SA'
                     EMC
            *
            *
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0160          *                ** INTER REGISTER ARITHMETIC OPERATIONS **                000161
0161          *                                                                          000162
0162          *                                                                          000163
0163          *                                                                          000164
0164          *                                  FLIP-FLOP CN SHOULD                     000165
0165          *                                  BE PROPERLY SET OR RESET                000166
0166          *                                BEFORE AN ARITHMETIC OPERATION            000167
0167          *                                  IS EXECUTED.                            000168
0168          *                                                                          000169
0169          *                                                                          000170
0170          IA      MAC   SA,D                 INCREMENT A:  SA+1--->D                 000171
0171          *                                  CONDITION  CN=1                         000172
0172                  VFD   N4/$C,X4/'D',N5/$1,X3/'SA'                                   000173
0173                  EMC                                                                000174
0174          DA      MAC   SA,D                 DECREMENT A:  SA-1--->D                 000175
0175          *                                  CONDITION  CN=1                         000176
0176                  VFD   N4/$C,X4/'D',N5/$1F,X3/'SA'                                  000177
0177                  EMC                                                                000178
0178          PLUS    MAC   SA,SB,D              PLUS:   SA+SB--->D                      000179
0179          *                                  CONDITION  CN=0                         000180
0180                  VFD   N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'                          000181
0181                  EMC                                                                000182
0182          MINUS   MAC   SA,SB,D              MINUS:  SA-SB--->D                      000183
0183          *                                  CONDITION  CN=1                         000184
0184                  VFD   N2/$3,X2/'SB',X4/'D',N5/$0,X3/'SA'                           000185
0185                  EMC                                                                000186
0186          PLUSI   MAC   SA,SB,D              PLUS INCREMENT:  SA+SB+1--->D           000187
0187          *                                  CONDITION  CN=1                         000188
0188                  VFD   N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'                          000189
0189                  EMC                                                                000190
0190          LSFT    MAC   SA,D                 LEFT SHIFT:   SA+SA--->D                000191
0191          *                                  CONDITION  CN=0                         000192
0192                  VFD   N4/$C,X4/'D',N5/$19,X3/'SA'                                  000193
0193                  EMC                                                                000194
0194          LSFTI   MAC   SA,D           LEFT SHIFT INCREMENT:  SA+SA+1--->D           000195
0195          *                                  CONDITION  CN=1                         000196
0196                  VFD   N4/$C,X4/'D',N5/$19,X3/'SA'                                  000197
0197                  EMC                                                                000198
0198          *                                                                          000199
0199          *                                                                          000200
0200          *                                                                          000201
0201          *                                                                          000202
0202          *                                                                          000203
0203          *                                                                          000204
0204          *                                                                          000205
0205          *                                                                          000206
0206          *                                                                          000207
0207          *                                                                          000208
0208          *                                                                          000209
0209          *                                                                          000210
0210          *                                                                          000211
0211          *                                                                          000212
0212          *                                                                          000213
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0213            COMPR  MAC    SA,SB                    COMPR:    SA=SB ?          000214
0214            *                                       CONDITION  CN=1          000215
0215            *                                       THE RESULT IS SENSED ON THE 000216
0216            *                                  A=B PIN OF THE ALU. THE DESTINATION 000217
0217            *                                       IS AN UNUSED REGISTER;     000218
0218            *                                       THEREFORE DATA REMAINS     000219
0219            *                                       UNCHANGED                  000220
0220                   VFD    N2/$3,X2/'SB',N9/$6D,X3/'SA'                          000221
0221                   EMC                                                          000222
0222            *                                                                   000223
0223            *                                                                   000224
0224            *                                                                   000225
0225            IRAR   MAC    M,SA,SB,D          INTER REGISTER ARITHMETIC (GENERAL) 000226
0226            *                                    THIS INSTRUCTION COVERS  ALL 16 000227
0227            *                                       AVAILABLE MODES OF ARITHMETIC 000228
0228            *                                       OPERATIONS. ALL 16 MODES   000229
0229            *                                       DEPEND ON THE STATE OF     000230
0230            *                                       THE CN FLIP-FLOP.          000231
0231            *                                       REFFER TO IRAR MODE DEF.   000232
0232            *                                                                   000233
0233            *                                                                   000234
0234            *                                                                   000235
0235                   VFD    N2/$3,X2/'SB',X4/'D',X4/'M',N1/$1,X3/'SA'            000236
0236                   EMC                                                          000237
0237            *                                                                   000238
0238            NOOP   MAC                                                         000239
0239            *                                       NO OPERATION               000240
0240            *                                                                   000241
0241                   VFD    N16/$BFFF                                            000242
0242                   EMC                                                          000243
0243            SPARE  MAC                                                         000244
0244            *                                       SPARE-                     000245
0245            *                                  PROM WORD REMAINS UNBURNED      000246
0246                   VFD    N16/$FFFF                                            000247
0247                   EMC                                                          000248
```

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0249                *                        **** IRAR  MODE DEFINITIONS ****                    000250

0251            0000            EQU     MODE0($0)          MODE0: SA+Z+CN--->D                  000252
0252            0001            EQU     MODE1($1)          MODE1: (SA.OR.SB)+CN--->D            000253
0253            0002            EQU     MODE2($2)          MODE2: (SA.OR.(SB/))+CN--->D         000254
0254            0003            EQU     MODE3($3)          MODE3: FFFF+CN--->D                  000255
0255            0004            EQU     MODE4($4)       MODE4: SA+(SA.AND.(SB/))+CN--->D        000256
0256            0005            EQU     MODE5($5)          MODE5:                               000257
0257                *                                   (SA.OR.SB)+(SA.AND.(SB/)+CN--->D     000258
0258            0006            EQU     MODE6($6)          MODE6: SA-SB-1+CN--->D               000259
0259            0007            EQU     MODE7($7)       MODE7: (SA.AND.(SB/))-1+CN--->D         000260
0260            0008            EQU     MODE8($8)          MODE8: SA+(SA.AND.SB)+CN--->D        000261
0261            0009            EQU     MODE9($9)          MODE9: SA+SB+CN--->D                 000262
0262            000A            EQU     MODEA($A)          MODEA:                               000263
0263                *                                   (SA.OR.(SB/))+(SA.AND.SB)+CN--->D    000264
0264            000B            EQU     MODEB($B)          MODEB: (SA.AND.SB)-1+CN--->D         000265
0265            000C            EQU     MODEC($C)          MODEC: SA+SA+CN--->D                 000266
0266            000D            EQU     MODED($D)          MODED: (SA.AND.SB)+SA+CN--->D        000267
0267            000E            EQU     MODEE($E)       MODEE: (SA.AND.(SB/))+SA+CN--->D        000268
0268            000F            EQU     MODEF($F)          MODEF: SA-1+CN--->D                  000269
```

```
                *                **** DESTINATION REGISTERS ****
        0003        EQU    NU($3)               NOT USED
        0004        EQU    RAMADD($4)           RAM ADDRESS
        0005        EQU    BANKD($5)            COMPUTER MEMORY BANK
        0006        EQU    RAMD($6)             RAM
        0007        EQU    PCD($7)              PROGRAM COUNTER
        0008        EQU    WCD($8)              WORD COUNTER
        0009        EQU    AOUTUD($9)           A REGISTER OUT UPPER BYTE
        000A        EQU    CWALD($A)            CURRENT WORD ADDRESS-
                *                                                 LOWER BYTE
        000B        EQU    CWAUD($B)            CURRENT WORD ADDRESS-
                *                                                 UPPER BYTE
        000C        EQU    AOUTLD($C)           A REGISTER OUT LOWER BYTE
        000D        EQU    BF2LD($D)            BUFFER 2 LOWER BYTE
        000E        EQU    BF2UD($E)            BUFFER 2 UPPER BYTE
        000F        EQU    BREGD($F)            B REGISTER
        0000        EQU    NU1($0)              NOT USED
```

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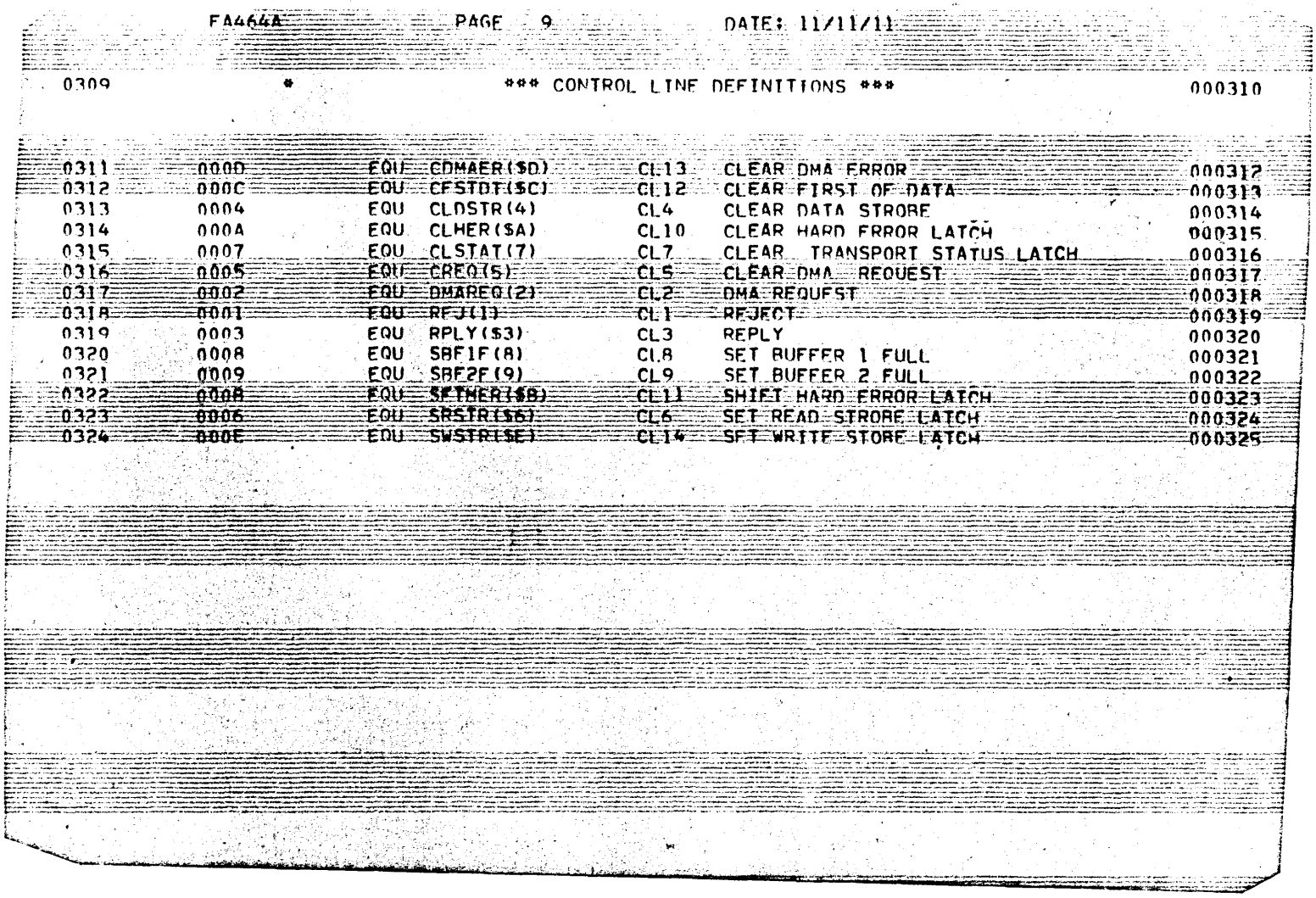
0290                *                        **** SOURCE A-REGISTERS ****                    000291


0292        0000            EQU     RAMS($0)            RAM                                 000293
0293        0001            EQU     WCS($1)             WORD COUNTER                        000294
0294        0002            EQU     AINLS($2)           A LINES IN LOWER BYTE               000295
0295        0003            EQU     AINUS($3)           A LINES IN UPPER BYTE               000296
0296        0004            EQU     BREGS($4)           B REGISTER                          000297
0297        0005            EQU     QS($5)              Q LIN                               000298
0298        0007            EQU     PCS($7)             PROGRAM COUNTER                     000299


0300                *                        **** SOURCE B REGISTERS ****                    000301


0302        0000            EQU     CWALS($0)           COURENT-WORD ADDRESS-               000303
0303                *                                                   LOWER BYTE          000304
0304        0001            EQU     CWAUS($1)           COURENT-WORD ADDRESS-               000305
0305                *                                                   UPPER BYTE          000306
0306        0002            EQU     BF2LS($2)           BUFFER 2 LOWER BYTE                 000307
0307        0003            EQU     BF2US($3)           BUFFER 2 UPPER BYTE                 000308
```



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0309            *          *** CONTROL LINE DEFINITIONS ***                    000310


0311    000D        EQU  CDMAER($D)     CL13   CLEAR DMA ERROR                 000312
0312    000C        EQU  CFSTDT($C)     CL12   CLEAR FIRST OF DATA             000313
0313    0004        EQU  CLDSTR(4)      CL4    CLEAR DATA STROBE               000314
0314    000A        EQU  CLHER($A)      CL10   CLEAR HARD ERROR LATCH          000315
0315    0007        EQU  CLSTAT(7)      CL7    CLEAR  TRANSPORT STATUS LATCH   000316
0316    0005        EQU  CREQ(5)        CL5    CLEAR DMA  REQUEST              000317
0317    0002        EQU  DMAREQ(2)      CL2    DMA REQUEST                     000318
0318    0001        EQU  REJ(1)         CL1    REJECT                          000319
0319    0003        EQU  RPLY($3)       CL3    REPLY                           000320
0320    0008        EQU  SBF1F(8)       CL8    SET BUFFER 1 FULL               000321
0321    0009        EQU  SBF2F(9)       CL9    SET BUFFER 2 FULL               000322
0322    000B        EQU  SFTHER($B)     CL11   SHIFT HARD ERROR LATCH          000323
0323    0006        EQU  SRSTR($6)      CL6    SET READ STROBE LATCH           000324
0324    000E        EQU  SWSTR($E)      CL14   SET WRITE STORE LATCH           000325
```

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0327                *                  *** JUMP CONDITION DEFINITIONS ***                    000328

0329    0003        EQU  ADRERR(3)     JC46   DMA ADDRESS ERROR                             000330
0330    002A        EQU  ALARMJC($2A)  JC62   ALARM                                        000331
0331    000E        EQU  ALDFNJC($E)   JC10   AUTOLOAD                                     000332
0332    002E        EQU  ALTFRC($2E)   JC60   ALTERNATE FORCE                              000333
0333    0027        EQU  AUTOLD($27)   JC24   AUTOLOAD SWITCH                            000334
0334    0000        EQU  AUXJC($0)     JC97   AUXILIARY                                   000335
0335    0019        EQU  BF1F($19)     JC33   BUFFER 1 FULL                               000336
0336    0007        EQU  BF2F(7)       JC44   BUFFER 2 FULL                               000337
0337    0014        EQU  BMDL($14)     JC85   B REGISTER BIT 5                            000338
0338    0028        EQU  BMSB($28)     JC43   B REGISTER BIT 7                            000339
0339    002F        EQU  BUSBSY($2F)   JC20   BUS BUSY                                   000340
0340    000C        EQU  CER($C)       JC91   CORRECTED ERROR                            000341
0341    0010        EQU  CERSTJC($10)  JC87   CORRECTED ERROR STATUS BIT                 000342
0342    000D        EQU  COUT($D)      JC41   ALU CARRY OUT                               000343
0343    002D        EQU  CRCERJC($2D)  JC21   N/A TO LCTT                                 000344
0344    0031        EQU  CRJ($31)      JC77   COMMAND REJECT                              000345
0345    001B        EQU  CWAUL($1B)    JC32   CURRENT WORD REG BIT 16                     000346
0346    0017        EQU  CWAUM($17)    JC34   CURRENT WORD REG 17                         000347
0347    001F        EQU  DMAWCP($1F)   JC30   DMA WRITE COMPLETE                          000348
0348    000E        EQU  EOT($E)       JC90   END OF TAPE                                 000349
0349    0020        EQU  EOTSTJC($20)  JC67   END OF TAPE STATUS BIT                     000350
0350    000F        EQU  EQUAL($F)     JC40   ALU A EQUAL B                              000351
0351    003C        EQU  FBY($3C)      JC51   FORMATTER BUSY                            000352
0352    0030        EQU  FMK($30)      JC57   FILE MARK                                  000353
0353    0036        EQU  FPT($36)      JC54   FILE PROTECT                               000354
0354    0013        EQU  FRSTDT($13)   JC36   FIRST DATA (N/A TO LCTT)                  000355
0355    0009        EQU  HEROUT(9)     JC43   HER OUTPUT                                 000356
0356    001D        EQU  HFWRD($1D)    JC31   HALF WORD (N/A TO LCTT)                   000357
0357    003F        EQU  IDENT($3F)    JC70   IDENTIFICATION BURST                       000358
0358    0026        EQU  INX2JC($26)   JC64   INDEX 2                                   000359
0359    002B        EQU  LDP($2B)      JC22   LOAD POINT                                 000360
*0360   0012        EQU  LRCRCJC($12)  JC86   CHECK CHARACTER FLAG                       000361
0361    003E        EQU  MOP1($3E)     JC50   MODE OPTION 1                              000362
0362    003D        EQU  MOP2($3D)     JC71   MODE OPTION 2                              000363
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0364            *       *** JUMP CONDITION DEFINITIONS (CONT.) ***      000365


0366    0004    EQU  MSW1($4)      JC95   MAINTANENCE SWITCH 1           000367
0367    000A    EQU  MSW2($A)      JC92   MAINTENANCE SWITCH 2           000368
0368    0008    EQU  MSW3($8)      JC93   MAINTANENCE SWITCH 3           000369
0369    0002    EQU  NOCOMP($2)    JC96   N/A TO LCTT                    000370
0370    000B    EQU  OFLMTJC($B)   JC13   OFF LINE  MAINTENENCE         000371
0371    001E    EQU  ONBUSJC($1E)  JC80   ON BUS                        000372
0372    0038    EQU  ONL($38)      JC53   ON LINE                       000373
0373    0023    EQU  ONOFLN($23)   JC26   ON/OFF LINE SWITCH            000374
0374    0035    EQU  NRZI($35)     JC75   NRZI                          000375
0375    0034    EQU  PARLT($34)    JC55   PARITY BIT LATCH              000376
0376    0005    EQU  PARERR(5)     JC45   DMA PARITY ERROR              000377
0377    001A    EQU  PARJC($1A)    JC82   SELECTED PARITY               000378
0378    0006    EQU  PROPRT(6)     JC14   PROGRAM PROTECT               000379
0379    000B    EQU  PRTFLT($B)    JC42   DMA PROTECT FAULT             000380
0380    000A    EQU  RALTIJC($A)   JC12   REQUEST ALTERNATE INTERRUPT    000381
0381    0037    EQU  RDM($37)      JC74   READ MODE                     000382
0382    003A    EQU  RDY($3A)      JC52   READY                         000383
0383    0004    EQU  RMEXEC($4)    JC15   ROM EXECUTE                   000384
0384    0011    EQU  RP($11)       JC37   READ PARITY                   000385
0385    0021    EQU  RSTRLN($21)   JC27   READ STROBE LINE              000386
0386    0029    EQU  RSTRLT($29)   JC23   READ STROBE LATCH             000387
0387    0033    EQU  RWS($33)      JC76   REWIND STATUS                 000388
0388    001C    EQU  SFMKJC($1C)   JC81   SEARCH FILE MARK              000389
0389    0016    EQU  SLCTDJC($16)  JC84   SELECTED                      000390
0390    0038    EQU  SOP($38)      JC72   SPEED OPTION                  000391
0391    0022    EQU  SPRJC($22)    JC66   SPARE                         000392
0392    0032    EQU  TFER($32)     JC56   TRANSFER ERROR                000393
0393    0039    EQU  TRK7($39)     JC73   7 TRACK                       000394
0394    0024    EQU  UNTPRT($24)   JC65   UNIT PROTECTED               000395
0395    0018    EQU  WCEMPT($18)   JC83   N/A TO LCTT                   000396
0396    0015    EQU  WORD($15)     JC35   WORD (N/A TO LCTT)            000397
0397    000C    EQU  WRTODJC($C)   JC11   WRITE ODD                     000398
0398    0002    EQU  WSTRLN(2)     JC16   WRITE STROBE LINE             000399
0399    0025    EQU  WSTRLT($25)   JC25   WRITE STROBE LATCH            000400
```

0403		*	*** FILP FLOP DEFINITIONS ***			000404
0405	0011	EQU	ACK($11)	FF26	ACKNOWLEDGE	000406
0406	002F	EQU	ALARMFF($2F)	FF40	ALARM	000407
0407	000C	EQU	ALDENFF($C)	FF53	AUTOLOAD ENPRTSYS	000408
0408	0027	EQU	AUXFF($27)	FF60	AUXILIARY	000409
0409	001E	EQU	BF1ENB($1E)	FF31	BUFFER1 ENABLE	000410
0410	002F	EQU	BUSY($2F)	FF41	BUSY	000411
0411	0030	EQU	CERST($30)	FF17	CORRECTED ERROR STATUS	000412
0412	001A	EQU	COMP1($1A)	FF35	COMPARE1	000413
0413	0020	EQU	CNALU($20)	FF67	ALU CARRY IN	000414
0414	0000	EQU	CNTPRT(0)	FF77	CONTROLLER PROTECTED	000415
0415	0025	EQU	DEN($25)	FF62	DENSITY SELECT	000416
0416	002C	EQU	DMWRPT($2C)	FF43	DMA WRITE PROTECT	000417
0417	001D	EQU	ENBDB($1D)	FF32	ENABLE DOUBLE BUFFER	000418
0418	001B	EQU	ENWDSY($1B)	FF34	ENABLE WORD SYNC	000419
0419	0003	EQU	EOP(3)	FF74	END OF OPERATIONS	000420
0420	0002	EQU	EOTST(2)	FF75	END OF TAPE STATUS	000421
0421	000E	EQU	ERS($E)	FF51	ERASE	000422
0422	0012	EQU	FEN($12)	FF25	FORMATTER ENABLE	000423
0423	0004	EQU	FMKST(4)	FF73	FILE MARK STATUS	000424
0424	002A	EQU	FRCBUS($2A)	FF45	FORCE BUS	000425
0425	0014	EQU	GO($14)	FF23	GO	000426
0426	002B	EQU	HERLD($2B)	FF44	HARD ERROR LOAD MODE	000427
0427	0028	EQU	INTRSP($28)	FF47	INTERRUPT RESPONSE	000428
0428	0006	EQU	INX2FF(6)	FF71	INDEX 2	000429
0429	0029	EQU	JCGRP9($29)	FF46	JUMP CONDITION GROUP 9 ENABLE	000430
0430	0034	EQU	LRCRCFF($34)	FF13	CHECK CHARACTER FLAG	000431
0431	0015	EQU	LWD($15)	FF22	LAST WORD DATA	000432
0432	0016	EQU	OFL($16)	FF21	OFF LINE	000433

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0434            *           *** FLIP FLOP DEFINITIONS (CONT.) ***                   000435


0436    000A    EQU  OFLMTFF($A)    FF55    OFF LINE MAINTENANCE                    000437
0437    0023    EQU  ONBUSFF($23)   FF64    ON BUS                                  000438
0438    0024    EQU  PARFF($24)     FF63    PARITY  SELECT                          000439
0439    0018    EQU  PARMD($18)     FF37    PARITY MODE                             000440
0440    0007    EQU  PRIOR(7)       FF70    PRIORITY                                000441
0441    0008    EQU  RALTIFF(8)     FF57    REQUEST ALTERNATE INTERRUPT             000442
0442    000D    EQU  REV($D)        FF52    REVERSE                                 000443
0443    0035    EQU  REW($35)       FF12    REWIND                                  000444
0444    0022    EQU  RQBUS1($22)    FF65    REQUEST BUS 1                           000445
0445    000F    EQU  RQBUS2($0F)    FF50    REQUEST BUS 2                           000446
0446    0033    EQU  RMBNKS($33)    FF14    ROM BANK SELECT                         000447
0447    0019    EQU  RWMOD($19)     FF36    READ/WRITE MODE                         000448
0448    0032    EQU  SFMKFF($32)    FF15    SEARCH FILE MARK FLAG                   000449
0449    0017    EQU  SELBF1($17)    FF20    SELECT BUFFER 1                         000450
0450    0010    EQU  SELBF2($10)    FF27    SELECT BUFFER2                          000451
0451    002D    EQU  SELBREG($2D)   FF42    SELECT B REGISTER                       000452
0452    0005    EQU  SLCTDFF(5)     FF72    SELECTED                                000453
0453    0031    EQU  SPM($31)       FF16    SPACING MODE                            000454
0454    0001    EQU  SPRFF($1)      FF76    SPARE                                   000455
0455    0021    EQU  TAD0($21)      FF66    TRANSPORT ADDRESS 0                     000456
0456    0026    EQU  TAD1($26)      FF61    TRANSPORT ADDRESS 1                     000457
0457    0037    EQU  THR($37)       FF10    LOW THRESHOLD                           000458
0458    0036    EQU  WFM($36)       FF11    WRITE FILE MARK                         000459
0459    001C    EQU  WP($1C)        FF33    WRITE PARITY                            000460
0460    0013    EQU  WRT($13)       FF24    WRITE                                   000461
0461    001F    EQU  WTRDMP($1F)    FF30    WRITE/READ MP                           000462
0462    0009    EQU  WRTODFF($9)    FF56    WRITE ODD                               000463
```

```
0464                *   *** ROUTINE NAME LABEL ABBREVIATIONS                    000465
0465                *   ALJ     AUTOLOAD JUMP ROUTINE                          000466
0466                *   AOS     A OUT STATUS                                   000467
0467                *   AOE     A/O EXECUTE ROUTINE                            000468
0468                *   ASJ     ASSEMBLE/SENSE JUMP                            000469
0469                *   ASR     ASSEMBLE/SENSE NEXT READY                      000470
0470                *   ATL     AUTOLOAD ROUTINE                               000471
0471                *   BKS     BANK SELECT                                    000472
0472                *   BL      BLOCK LENGTH                                   000473
0473                *   BSC     BUS CONNECT/RELEASE                            000474
0474                *   BSP     BACKSPACE                                      000475
0475                *   BSR     BUS RELINQUISH ROUTINE                         000476
0476                *   CBS     CURRENT BANK STATUS                            000477
0477                *   CNR     CONTROLLED BACKSPACE                           000478
0478                *   CST     CLEAR STATUS SUBROUTINE                        000479
0479                *   CWS     CURRENT WORD STATUS                            000480
0480                *   DBL     DECREMENT BLOCK LENGTH SUBROUTINE              000481
0481                *   DFD     DIRECTOR FUNCTION DECODE ROUTINE               000482
0482                *   DTE     DMA TRANSFER ERROR ROUTINE                     000483
0483                *   ESA     FORMATTER ERROR STATUS ASSEMBLY ROUTINE        000484
0484                *   FDS     FORMATTER DISABLE ROUTINE                      000485
0485                *   FFR     FIXED ERASE                                    000486
0486                *   FRJ     FORMATTER REJECT ROUTINE                       000487
0487                *   FST     FILE STATUS                                    000488
0488                *   FWA     FIRST WORD ADDRESS                             000489
0489                *   IRQ     INTERRUPT REQUEST                              000490
0490                *   LFA     LOAD FILE ADDRESS                              000491
0491                *   MC      MASTER CLEAR AND CLEAR CONTROLLER              000492
0492                *   OLM     OFF LINE MAINTENANCE ROUTINE                   000493
0493                *   PCH     PARITY GENERATOR CHECK SUBSECTION              000494
0494                *   PKS     RANK TEST SUBSECTION                           000495
0495                *   RD      READ DATA                                      000496
0496                *   RDS     READ STROBE SUBROUTINE                         000497
```

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0498                *       *** ROUTINE NAME LABLE ABREVIATIONS (CONT.) ***          000499


0500                *       RJC     REJECT ROUTINE                                   000501
0501                *       ROL     REWIND OFF LINE                                  000502
0502                *       RPL     REPLY ROUTINE                                    000503
0503                *       RWD     REWIND                                           000504
0504                *       SFB     SEARCH FILE MARK BACKWARD                        000505
0505                *       SFF     SEARCH FILE MARK FORWARD                         000506
0506                *       SGO     SET GO SUBROUTINE                                000507
0507                *       SNS     SENSE SUBROUTINE                                 000508
0508                *       SPF     SPACE FOWARD                                     000509
0509                *       STA     SELF TEST 1                                      000510
0510                *       STB     SELF TEST 2                                      000511
0511                *       STC     SELF TEST 3                                      000512
0512                *       STD     SELF TEST 4                                      000513
0513                *       TDS     TEST DATA SUBROUTINE                             000514
0514                *       TFB     TERMINATE FORMATTER BUSY                         000515
0515                *       TRB     TERMINATE BUSY ROUTINE                           000516
0516                *       TRD     TERMINATE READ/DIRECTOR FUNCTION                 000517
0517                *       TST     TRANSPORT STATUS                                 000518
0518                *       TWT     TERMINATE WRITE                                  000519
0519                *       UNS     UNIT SELECT/DESELECT                             000520
0520                *       VER     VARIABLE ERASE                                   000521
0521                *       WL      A/Q WAITING LOOP                                 000522
0522                *       WRF     WRITE FILE MARK                                  000523
0523                *       WSR     WRITE STROBE SUBROUTINE                          000524
0524                *       WT      WRITE DATA                                       000525


0527                        ENT  START1                                              000528
```

```
0529            ***************************************************************   000530
0530            *                                                             *   000531
0531            *               *** MASTER CLEAR AND CLEAR CONTROLLER ***     *   000532
0532            *                                                             *   000533
0533            ***************************************************************   000534

0535            START1 UJP   MC1                                                  000536
0535 P0000 0001
0536            MC1    CJP   ALTFRC,BSR1        FORCE BUS RELINQUISH?            000537
0536 P0001 5D28
0537                   LDC   RAMADD,$04                                          000538
0537 P0002 8404
0538                   LDC   RAMD,$FF           CLEAR INTERRUPT REQUESTS         000539
0538 P0003 86FF
0539                   CJP   RMEXEC,MC6         CLEAR CONTROLLER?                000540
0539 P0004 0806
0540                   UJP   TRB4               MASTER CLEAR - GO TO TERM. BSY   000541
0540 P0005 0043
0541            MC6    RFF   EOTST              RESET STATUSES                   000542
0541 P0006 AF02
0542                   RFF   FMKST                                               000543
0542 P0007 AF04
0543                   SFF   PARMD              REINITIALIZE PARITY MODE         000544
0543 P0008 BF18
0544                   CJP   PARJC,MC11                                          000545
0544 P0009 340B
0545                   RFF   PARMD                                               000546
0545 P000A AF18
0546            MC11   CJP   SLCTDJC,MC13                                        000547
0546 P000B 2C0D
0547                   UJP   TRB4                                                000548
0547 P000C 0043
0548            MC13   SFF   FEN                                                 000549
0548 P000D BF12
0549                   UJP   TRB4                                                000550
0549 P000E 0043
0550                   SPARE                                                     000551
0550 P000F FFFF
```

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0552              ****************************************************************        000553
0553              *                                                              *        000554
0554              *                 *** REPLY ROUTINE ***                        *        000555
0555              *                                                              *        000556
0556              ****************************************************************        000557


0558        0020 P        ORG   START1+$20                                                000559
0559              RPL1    SFFCL  FOP+RPLY                                                 000560
0559 P0020 B303
0560                      UJP   WL1                                                       000561
0560 P0021 0051


0562              ****************************************************************        000563
0563              *                                                              *        000564
0564              *                 *** REJECT ROUTINE ***                       *        000565
0565              *                                                              *        000566
0566              ****************************************************************        000567


0568              RJC1    CL01 REJ                  ISSUE REJECT                          000569
0568 P0022 A1FF
0569                      UJP   WL1                                                       000570
0569 P0023 0051
0570                      SPARE                                                           000571
0570 P0024 FFFF
```

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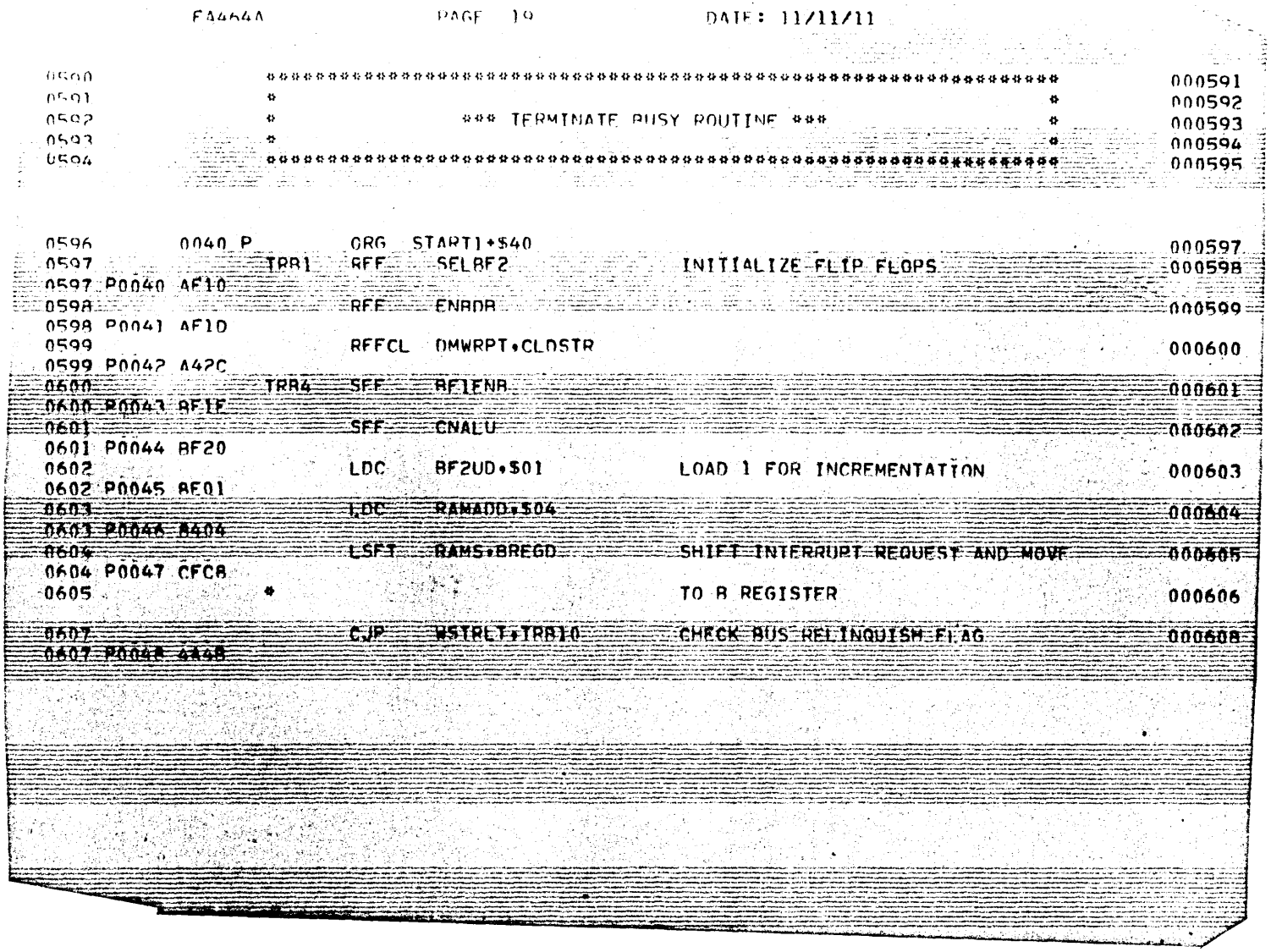
0572          ********************************************************************** 000573
0573          *                                                                    * 000574
0574          *                 *** AUTOLOAD JUMP ROUTINE ***                      * 000575
0575          *                                                                    * 000576
0576          ********************************************************************** 000577


0578          ALJ1  CJP    AUTOLD,WL1          SAMPLE AUTOLD SWITCH TWICE          000579
0578 P0025 4E51
0579                CJP    SLCTDJC,WL1         UNIT SELECTED? YES:ABORT AUTOLD     000580
0579 P0026 2C51
0580                SFF    ALDFNFF             SET AUTOLD FLAG                     000581
0580 P0027 BF0C
0581          ALJ4  SFF    BUSY                ENTER BUSY                          000582
0581 P0028 BF2E
0582                LDC    BREGD,$00           NORMAL BUS CONNECT FLAG             000583
0582 P0029 BF00
0583                UJP    BSC9                ENTER BUS CONNECT                   000584
0583 P002A 00A0
0584          ALJ10 SFF    SFMKFF                                                  000585
0584 P002B BF32
0585                RFF    PARFF               SELECT ODD PARITY                   000586
0585 P002C AF24
0586                RFF    PARMD                                                   000587
0586 P002D AF18
0587                SFF    RMRNKS                                                  000588
0587 P002E BF33
0588                UJP    ASR12               JUMP TO SELECT FIRST UNIT READY     000589
0588 P002F 0165
```



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0590          ********************************************************************      000591
0591          *                                                                  *      000592
0592          *                  *** TERMINATE BUSY ROUTINE ***                  *      000593
0593          *                                                                  *      000594
0594          ********************************************************************      000595


0596     0040 P       ORG   START1+$40                                              000597
0597          TRB1    RFE   SELBF2              INITIALIZE FLIP FLOPS               000598
0597 P0040 AF10
0598                  RFE   ENBDB                                                   000599
0598 P0041 AF1D
0599                  RFFCL DMWRPT+CLDSTR                                           000600
0599 P0042 A42C
0600          TRB4    SFF   BF1ENB                                                  000601
0600 P0043 BF1F
0601                  SFF   CNALU                                                   000602
0601 P0044 BF20
0602                  LDC   BF2UD+$01           LOAD 1 FOR INCREMENTATION           000603
0602 P0045 BE01
0603                  LDC   RAMADD+$04                                              000604
0603 P0046 B404
0604                  LSFT  RAMS+BREGD          SHIFT INTERRUPT REQUEST AND MOVE    000605
0604 P0047 CFC8
0605             *                              TO B REGISTER                       000606

0607                  CJP   RSTRET+TRB10        CHECK BUS RELINQUISH FLAG           000608
0607 P0048 4A4B
```

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0609                        CJP     RMFXEC,RPL1         PREVIOUS COMMAND CLEAR          000610
0609 P0049 0820
0610                  *.                                CONTROLLER? YES-ISSUE REPLY     000611
0612                        CJP     COUT,TRB11          EOP INTERRUPT REQUESTED? YES-   000613
0612 P004A 1A4F
0613                  *                                 SET INTERRUPT RESPONSE          000614
0615                  TRB10 CJP     BMSB,TRB12          ALARM INTERRUPT REQUESTED?      000616
0615 P004B 504F
0616                        CJP     ALARMJC,TRB11       YES - CHECK ALARM IF ACTIVE     000617
0616 P004C 544F
0617                  *                                 SET INTERRUPT RESPONSE          000618
0618                        UJP     TRB12                                               000619
0618 P004D 004F
0619                  TRB11 SFF     INTRSP              SET INTERRUPT RESPONSE          000620
0619 P004E BF28
0620                  TRB12 SFFCL   EOP,CLOSTR          EXIT FROM BUSY                  000621
0620 P004F B403
0621                        RFF     BUSY                                                000622
0621 P0050 AF2E
```

```
                ********************************************************************      000624
                *                                                                  *      000625
                *                  *** A/Q WAITING LOOP ***                        *      000626
                *                                                                  *      000627
                ********************************************************************      000628


                WL1     CJP     RMEXEC*AQE1     A/Q COMMAND RECEIVED?                     000630
0629 P0051 085F
                        CJP     ONBUSJC*WL4     CHECK CONDITIONS FOR ALTERNATE            000631
0630 P0052 3C54
                *                               BUS REQUEST INTERRUPT                     000632
                        CJP     BUSBSY*WL9                                                000633
0632 P0053 5E5A
                WL4     CJP     RMEXEC*AQE1                                               000634
0633 P0054 085F
                        CJP     AUTOLD*WL6      AUTOLOAD SWITCH PRESSED?                  000635
0634 P0055 4E57
                        CJP     ONBUSJC*ALJ1    DO NOT PERFORM AUTOLOAD IF                000636
0635 P0056 3C25
                *                               CONTROLLER IS ON BUS                      000637
                WL6     CJP     RMEXEC*AQE1                                               000638
0637 P0057 085F
                        CJP     ONOFLN*WL1      LINE SWITCH OFF? YES - PERFORM            000639
0638 P0058 4651
                *                               OFF LINE MAINTENANCE                      000640
                        UJP     ALJ4                                                      000641
0640 P0059 0028
                WL9     CJP     RMEXEC*AQE1                                               000642
0641 P005A 085F
                        CJP     RALTIJC*WL12                                              000643
0642 P005B 1450
                        UJP     WL1             CONTINUE LOOP                             000644
0643 P005C 0051
                WL12    SFE     INTRSP          SET INTERRUPT RESPONSE FOR                000645
0644 P005D BF28
                *                               ALTERNATE BUS REQUEST                     000646
                        UJP     WL1                                                       000647
0646 P005E 0051
```

```
0648              ********************************************************************      000649
0649              *                                                                  *      000650
0650              *                  *** A/O EXECUTE ROUTINE ***                     *      000651
0651              *                                                                  *      000652
0652              ********************************************************************      000653

0654              AQE1   LDC    WCO,$10          LOAD MASK                                  000655
0654 P005F 8810
0655                     TA     QS,BF2LD         SAMPLE Q LINES TWICE                       000656
0655 P0060 CDF5
0656                     COMPR  QS,BF2LS                                                    000657
0656 P0061 E36D
0657                     CJP    EQUAL,AQE6       COMPARE BOTH Q LINE SAMPLES-               000658
0657 P0062 1F64
0658                     UJP    RJC1             REJECT IF NOT EQUAL                        000659
0658 P0063 0022
0659              AQE6   ORCB   WCS,BF2LS,PCO     MASK AND PRELOAD Q LINE                    000660
0659 P0064 E7D1
0660              *                               FUNCTION CODE TO PC                        000661
```

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0663          ****************** INPUT INSTRUCTION DECODE **********************          000664

0665      0010 P        ORG   START1+$10                                              000666
0666                    UJP   RJC1          ILLEGAL CODE                              000667
0666 P0010 0022
0667                    UJP   RPL1          AOUT STATUS                               000668
0667 P0011 0020
0668                    UJP   CWS1          CURRENT WORD STATUS                       000669
0668 P0012 0105
0669                    UJP   CBS1          CURRENT BANK STATUS                       000670
0669 P0013 00F8
0670                    UJP   FST1          FILE STATUS                               000671
0670 P0014 00F5
0671                    UJP   TST1          TRANSPORT STATUS                          000672
0671 P0015 00D2
0672                    UJP   RJC1          ILLEGAL CODE                              000673
0672 P0016 0022
0673                    UJP   RJC1          ILLEGAL CODE                              000674
0673 P0017 0022
0674                    UJP   RJC1          ILLEGAL CODE                              000675
0674 P0018 0022
0675                    UJP   RJC1          ILLEGAL CODE                              000676
0675 P0019 0022
0676                    UJP   RJC1          ILLEGAL CODE                              000677
0676 P001A 0022
0677                    UJP   RJC1          ILLEGAL CODE                              000678
0677 P001B 0022
0678                    UJP   RJC1          ILLEGAL CODE                              000679
0678 P001C 0022
0679                    UJP   RJC1          ILLEGAL CODE                              000680
0679 P001D 0022
0680                    UJP   RJC1          ILLEGAL CODE                              000681
0680 P001E 0022
0681                    UJP   RJC1          ILLEGAL CODE                              000682
0681 P001F 0022
```

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0684                ********** OUTPUT INSTRUCTION DECODE **********                000685

0686      0030 P      ORG  START1+$30                                              000687
0687                  UJP    RJC1          ILLEGAL CODE                           000688
0687 P0030 0022
0688                  UJP    DFD1          DIRECTOR FUNCTION                      000689
0688 P0031 0105
0689                  UJP    FWA1          FIRST WORD ADDRESS                     000690
0689 P0032 00E9
0690                  UJP    BKS1          BANK SELECT                            000691
0690 P0033 00FC
0691                  UJP    LFA1          LOAD FILE ADDRESS                      000692
0691 P0034 00F3
0692                  UJP    ASJ1          ASSEMBLE/SENSE NEXT READY              000693
0692 P0035 0108
0693                  UJP    UNS1          UNIT SELECT                            000694
0693 P0036 0069
0694                  UJP    BL1           BLOCK LENGTH                           000695
0694 P0037 00FF
0695                  UJP    BSC1          BUS CONNECT                            000696
0695 P0038 0099
0696                  UJP    IRQ1          INTERRUPT REQUEST                      000697
0696 P0039 00C5
0697                  UJP    RJC1          ILLEGAL CODE                           000698
0697 P003A 0022
0698                  UJP    RJC1          ILLEGAL CODE                           000699
0698 P003B 0022
0699                  UJP    STA1          SELF TEST 1                            000700
0699 P003C 0150
0700                  UJP    STB1          SELF TEST 2                            000701
0700 P003D 0141
0701                  UJP    STC1          SELF TEST 3                            000702
0701 P003E 0166
0702                  UJP    STD1          SELF TEST 4                            000703
0702 P003F 0126
```

```
0704                ************************************************************                000705
0705                *                                                          *                000706
0706                *              *** UNIT SELECT/DESELECT ***                *                000707
0707                *                                                          *                000708
0708                ************************************************************                000709


0710        0069 P          ORG   START1+$69                                                    000711
0711                UNS1    CJP     ONBUSJC+RJCI          ON BUS?  NO: REJECT                  000712
0711 P0069 3C22
0712                        TA      AINLS+BREGD           SAVE A LINES LOW IN B REGISTER       000713
0712 P006A CFF2
0713                        CJP     BMSB+UNS50            DESELECT?                            000714
0713 P006B 5065
0714                        CJP     UNITPRT+UNS11         SELECT PROTECTED UNIT?               000715
0714 P006C 486F
0715                        RFF     CNTPRT                                                     000716
0715 P006D AF00
0716                        UJP     UNS13                                                      000717
0716 P006E 0071
0717                UNS11   CJP     PRGPRT+RJCI           ATTEMPT TO SELECT PROTECTED          000718
0717 P006F 0C22
0718                        SFF     CNTPRT                SET CONTROLLER PROTECTED             000719
0718 P0070 BF00
0719                UNS13   TA      AINUS+WCD             SAVE A LINES UPPER                   000720
0719 P0071 C8F3
0720                        RFF     EOP                   ENTER BUSY                           000721
0720 P0072 AF03
0721                        SPFCL   BUSY+RPLY                                                  000722
0721 P0073 B32E
0722                        PLUS    PCS+BF2US+RAMD                                             000723
0722 P0074 F69F
0723                        UJP     CST1                  CALL CLEAR STATUS SUBROUTINE         000724
0723 P0075 0085
```

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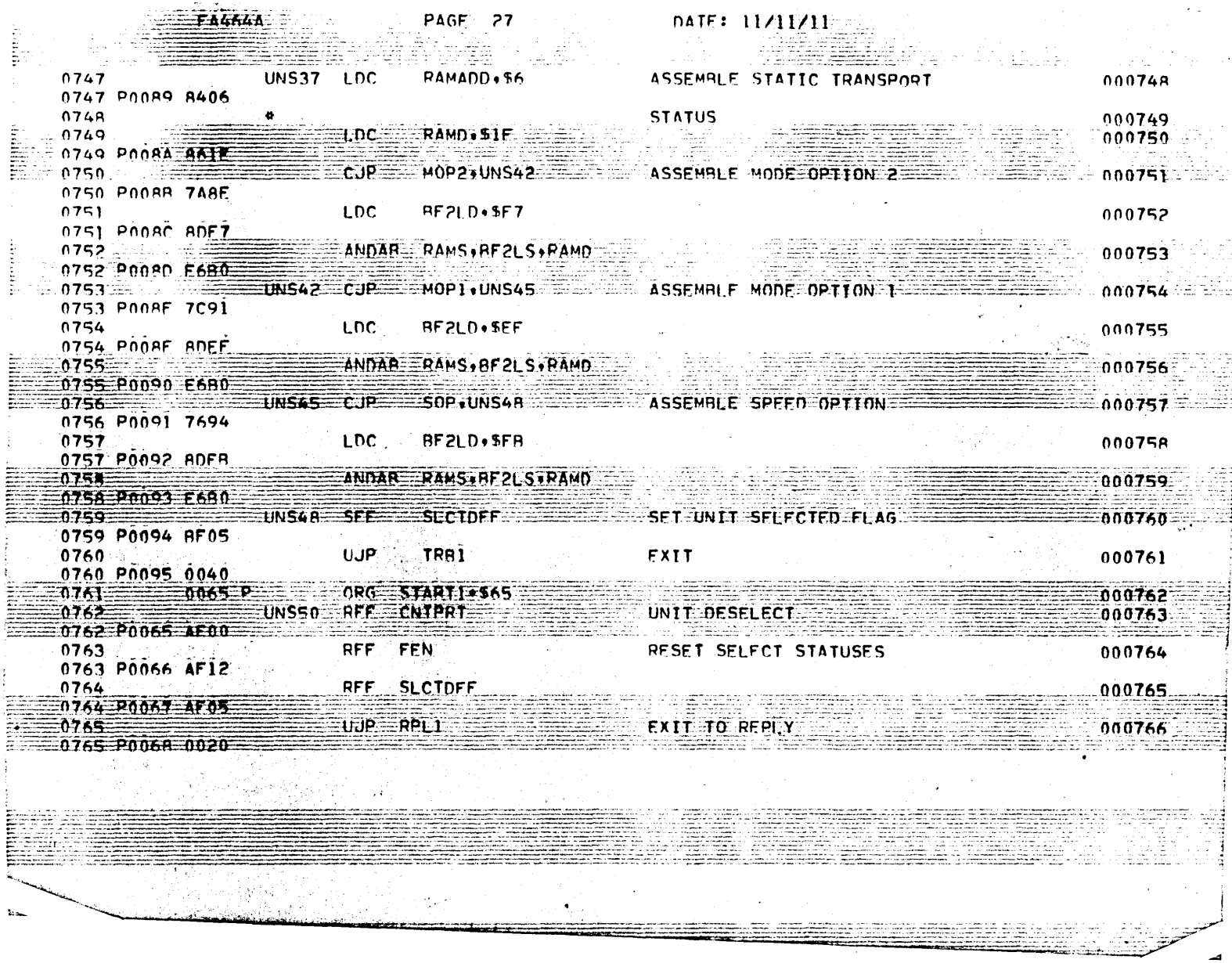
0725                       RFF   TAD0        SET UNIT  SELECT CODE ACCORDING      000726
0725 P0076 AF21
0726                  *                      A LINE BITS 5 AND 4                  000727
0727                       CJP   BMDL,UNS21                                        000728
0727 P0077 2879
0728                       SFF   TAD0                                              000729
0728 P0078 BF21
0729                  UNS21 LSFT  BREGS,BRFGD                                      000730
0729 P0079 CFCC
0730                       RFF   TAD1                                              000731
0730 P007A AF26
0731                       CJP   BMDL,UNS25                                        000732
0731 P007B 287D
0732                       SFF   TAD1                                              000733
0732 P007C BF26
0733                  UNS25 SFF   FEN           ENABLE FORMATTER                  000734
0733 P007D BF12
0734                       TA    WCS,BREGD     MOVE SAVED A LINE UPPER FOR       000735
0734 P007E CFF1
0735                  *                      EXAMINATION                          000736
0736                       RFF   DEN                                               000737
0736 P007F AF25
0737                       CJP   BMSB,UNS30    SELECT DENSITY                    000738
0737 P0080 5082
0738                       SFF   DEN                                               000739
0738 P0081 BF25
0739                  UNS30 RFF   PARMD         SET BINARY MODE FOR 9 TRACK       000740
0739 P0082 AF18
0740                       RFF   PARFF                                             000741
0740 P0083 AF24
0741                       CJP   BMDL,UNS37                                        000742
0741 P0084 2889
0742                       CJP   TRK7,UNS35    SELECT BCD MODE FOR 7 TRACK?      000743
0742 P0085 7287
0743                       UJP   UNS37                                             000744
0743 P0086 0089
0744                  UNS35 SFF   PARMD         BCD MODE SELECTED FOR 7 TRACK     000745
0744 P0087 BF18
0745                       SFF   PARFF                                           . 000746
0745 P0088 BF24
```



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0747                UNS37  LDC    RAMADD,$6          ASSEMBLE STATIC TRANSPORT          000748
0747 P0089 8406
0748                       *                         STATUS                             000749
0749                       LDC    RAMD,$1F                                              000750
0749 P008A AA1F
0750                       CJP    MOP2,UNS42         ASSEMBLE MODE OPTION 2             000751
0750 P008B 7A8E
0751                       LDC    BF2LD,$F7                                             000752
0751 P008C ADF7
0752                       ANDAR  RAMS,BF2LS,RAMD                                       000753
0752 P008D E6B0
0753                UNS42  CJP    MOP1,UNS45         ASSEMBLE MODE OPTION 1             000754
0753 P008E 7C91
0754                       LDC    BF2LD,$EF                                             000755
0754 P008F ADEF
0755                       ANDAR  RAMS,BF2LS,RAMD                                       000756
0755 P0090 E6B0
0756                UNS45  CJP    SOP,UNS48          ASSEMBLE SPEED OPTION              000757
0756 P0091 7694
0757                       LDC    BF2LD,$FB                                             000758
0757 P0092 ADFB
0758                       ANDAR  RAMS,BF2LS,RAMD                                       000759
0758 P0093 E6B0
0759                UNS48  SFE    SLCTDFF            SET UNIT SELECTED FLAG             000760
0759 P0094 BF05
0760                       UJP    TRB1               EXIT                               000761
0760 P0095 0040
0761          0065 P       ORG    START1,$65                                            000762
0762                UNS50  RFF    CNTPRT             UNIT DESELECT                      000763
0762 P0065 AE00
0763                       RFF    FEN                RESET SELECT STATUSES              000764
0763 P0066 AF12
0764                       RFF    SLCTDFF                                               000765
0764 P0067 AF05
0765                       UJP    RPL1               EXIT TO REPLY                      000766
0765 P006A 0020
```

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0767          ********************************************************************      000768
0768          *                                                                  *      000769
0769          *                  *** BUS CONNECT/RELEASE ***                     *      000770
0770          *                                                                  *      000771
0771          ********************************************************************      000772


0773     0099 P       ORG   START1+$99                                             000774
0774           BSC1   CA    AINLS,BREGD          SAVE A LINES LOWER               000775
0774 P0099 CF02
0775                  CJP   BMSB,BSC7            BUS CONNECT OR RELEASE?          000776
0775 P009A 509E
0776                  RFF   ONBUSFF              RELEASE BUS                      000777
0776 P009B AF23
0777                  RFF   RQBUS1                                                000778
0777 P009C AF22
0778                  UJP   RPL1                 EXIT TO REPLY                    000779
0778 P009D 0020
0779           BSC7   RFF   EOP                  BUS CONNECT-ENTER BUSY           000780
0779 P009E AF03
0780                  SFEQL BUSY,RPLY                                             000781
0780 P009F B32E
0781           BSC9   PLUS  PC5,BF2US,RAMD                                        000782
0781 P00A0 F69F
0782                  UJP   CST1                 CALL CLEAR STATUS SUBROUTINE     000783
0782 P00A1 0085
0783                  CJP   BMBL,BSC23           FORCE BUS?                       000784
0783 P00A2 29ED
0784                  CJP   BUSBSY,BSC25         BUS BUSY?                        000785
0784 P00A3 5FFF
0785                  SFF   RQBUS1               NO: SIGNAL ALTERNATE THAT BUS    000786
0785 P00A4 BF22
0786                  *                          CONNECT IS IN PROGRESS           000787
0787                  SFF   RQBUS2                                                000788
0787 P00A5 BF0F
0788                  NOOP                                                        000789
0788 P00A6 BFFF
```

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0790                        CJP   BUSBSY,BSC25      SIMULTANEOUS REQUEST?          000791
0790 P00A7 5FFF
0791                  BSC17 RFF   RQBUS2            NO: GAIN BUS CONTROL           000792
0791 P00A8 AF0F
0792                        SFF   ONBUSFF                                          000793
0792 P00A9 BF23
0793                        CJP   ALDENJC,ALJ10     AUTOLOAD FLAG? YES-RETURN TO   000794
0793 P00AA 1C2B
0794                  *                             AUTOLOAD ROUTINE               000795

0796                        CJP   ONOFLN,TRB1       OFF LINE MAINTENANCE? NO:EXIT  000797
0796 P00AB 4640
0797                        SFF   OFLMTFF                                          000798
0797 P00AC BF0A
0798                        UJP   ALJ10             RETURN TO MAINTENANCE ROUTINE  000799
0798 P00AD 002B
0799        01FD P          ORG   START1+$1FD                                      000800
0800                  BSC23 SFF   FRCBUS            FORCE BUS CONNECT              000801
0800 P01FD BF2A
0801                        SFF   RQBUS1                                           000802
0801 P01FE BF22
0802                  BSC25 UJP   BSC2A                                            000803
0802 P01FF 00AE
0803        00AE P          ORG   START1+$AE                                       000804
0804                  BSC26 RFF   RQBUS1                                           000805
0804 P00AE AF22
0805                        NOOP                                                   000806
0805 P00AF RFFF
0806        00B0 P          ORG   START1+$B0                                       000807
0807                        RFF   RQBUS2                                           000808
0807 P00B0 AF0F
0808                        RFF   FRCBUS                                           000809
0808 P00B1 AF2A
0809                        SFF   RQBUS1                                           000810
0809 P00B2 BF22
0810                  BSC31 CJP   BUSBSY,BSC31      WAIT FOR BUS TO BE AVAILABLE   000811
0810 P00B3 5EB3
0811                        UJP   BSC17                                            000812
0811 P00B4 00A8
```

```
0813          ********************************************************************   000814
0814          *                                                                  *   000815
0815          *                *** BUS RELINQUISH ROUTINE ***                    *   000816
0816          *                                                                  *   000817
0817          ********************************************************************   000818


0819      012B P      ORG   START1+$12B                                              000820
0820          BSR1    LDC   RAMADD,$0A                                               000821
0820 P012B 840A
0821                  LDC   RAMD,$7F            SET BUS RELINQUISH STATUS BIT        000822
0821 P012C 867F
0822                  SEFCL   ALARMFF,SWSTR     SET ALARM                            000823
0822 P012D BE2F
0823                  UJP   TRB4                EXIT                                 000824
0823 P012E 0043


0825          ********************************************************************   000826
0826          *                                                                  *   000827
0827          *             *** CLEAR STATUS SUBROUTINE ***                      *   000828
0828          *                                                                  *   000829
0829          ********************************************************************   000830


0831      00B5 P      ORG   START1+$B5                                               000832
0832          CSTI    RFF   THR                 RESET DYNAMIC STATUS F/F'S           000833
0832 P00B5 AF37
0833          *                                 AND FORMATTER COMMAND F/F'S          000834
0834                  RFF   FMKST                                                    000835
0834 P00B6 AF04
```

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0836                      RFFCL ALARMFF,CLSTAT                                  000837
0836 P00B7 A72F
0837                      RFF   ERS                                             000838
0837 P00B8 AF0F
0838                      RFFCL  EOTST,CLHER                                    000839
0838 P00B9 AA02
0839                      RFF   WFM                                             000840
0839 P00BA AF36
0840                      RFF   CERST                                           000841
0840 P00BB AF30
0841                      RFFCL  SPM,CLDSTR                                     000842
0841 P00BC A431
0842                      RFF   WRT                                             000843
0842 P00BD AF13
0843                      LDC   RAMADD,$0B          CLEAR ALARM STATUS WORD     000844
0843 P00BE 840B
0844                      RFF   REV                                             000845
0844 P00BF AF0D
0845                      LDC   RAMD,$FF                                        000846
0845 P00C0 86FF
0846                      LDC   RAMADD,$0A                                      000847
0846 P00C1 840A
0847                      LDC   RAMD,$FF                                        000848
0847 P00C2 86FF
0848                      LDC   RAMADD,$00                                      000849
0848 P00C3 8400
0849                      PLUS  RAMS,BF2US,PCD      RETURN                      000850
0849 P00C4 F798
```

```
0851              ******************************************************************     000852
0852              *                                                                *     000853
0853              *                    *** INTERRUPT REQUEST ***                   *     000854
0854              *                                                                *     000855
0855              ******************************************************************     000856

0857              IRQ1   TA    AINLS,BREGD            MOVE A LINES LOWER TO B REG.          000858
0857 P00C5 CFF2
0858                     LDC   RAMADD,$04                                                   000859
0858 P00C6 8404
0859                     CJP   BMSB,IRQ5              CLEAR INTERRUPTS?                     000860
0859 P00C7 50CB
0860                     RFF   INTRSP                 YES-RESET INTEPRUPT REQUESTS          000861
0860 P00C8 AF28
0861              *                                   AND RESPONSE                          000862
0862                     RFF   RALTIFF                                                      000863
0862 P00C9 AF08
0863                     LDC   RAMD,$FF                                                     000864
0863 P00CA 86FF
0864              IRQ5   LSFT  BREGS,BREGD                                                  000865
0864 P00CB CFCC
0865                     LSFT  BREGS,BF2LD                                                  000866
0865 P00CC CDCC
0866                     ANDAB RAMS,BF2LS,RAMD        SAVE ALARM AND FOP INTERRUPT          000867
0866 P00CD E6B0
0867              *                                   REQUESTS IN FILE                      000868
0869                     CJP   BMSB,IRQ10             ALTERNATE INTERRUPT REQUESTED?        000870
0869 P00CE 50D0
0870                     SFF   RALTIFF                                                      000871
0870 P00CF BF08
0871              IRQ10  CJP   ALARMJC,IRQ12                                                000872
0871 P00D0 552F
0872                     UJP   RPL1                   EXIT TO REPLY                         000873
0872 P00D1 0020
```

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0874        012F P          ORG   START1+$12F                                  000875
0875                IRQ12   CJP   BMDL+RPL1          SET INTERRUPT RESPONE IF ALARM   000876
0875 P012F 2820
0876                *                                IS ACTIVE AND ALARM INT IS       000877

0878                        SEF   INTRSP              REQUESTED                        000879
0878 P0130 BF28
0879                        UJP   RPL1                EXIT TO REPLY                    000880
0879 P0131 0020
0880                      SPARE                                                      000881
0880 P0132 FFFF


0882                ********************************************************       000883
0883                *                                                      *       000884
0884                *                *** TRANSPORT STATUS ***             *       000885
0885                *                                                      *       000886
0886                ********************************************************       000887


0888        00D2 P          ORG   START1+$D2                                     000889
0889                TST1    CJP   ONBUSJC+RJC1        ON BUS? NO=REJECT                000890
0889 P00D2 3C22
0890                        LDC   BREGD+$07                                      000891
0890 P00D3 BF07
0891                        CJP   SLCTDJC+TST7        TRANSPORT SELECTED?              000892
0891 P00D4 2CD8
0892                        LDC   AOUTUD+$40          SET DESELECT STATUS              000893
0892 P00D5 8940
0893                TST5.   LDC   AOUTLD+$00                                     000894
0893 P00D6 8C00
0894                        UJP   RPL1                EXIT                             000895
0894 P00D7 0020
0895                TST7    CJP   ONL+TST10           TRANSPORT ON LINE ?              000896
0895 P00D8 70DB
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0897                          LDC   AOUTUD,$80        SET OFF LINE STATUS                000898
0897 P00D9 8980
0898                          UJP   TST5                                                 000899
0898 P00DA 00D6
0899                TST10     CJP   FPT,TST13         SAMPLE FILE PROTECT STATUS         000900
0899 P00DB 6CDE
0900                          LDC   BF2LD,$FB                                            000901
0900 P00DC 8DFB
0901                          ANDAB BREGS,BF2LS,BREGD                                    000902
0901 P00DD EF84
0902                TST13     CJP   RWS,TST16         SAMPLE REWIND STATUS               000903
0902 P00DE 66E1
0903                          LDC   BF2LD,$FE                                            000904
0903 P00DF 8DFE
0904                          ANDAB BREGS,BF2LS,BREGD                                    000905
0904 P00E0 EF84
0905                TST16     LDC   BF2LD,$FD                                            000906
0905 P00E1 8DFD
0906                          CJP   LDP,TST19         SAMPLE LOAD POINT STATUS           000907
0906 P00E2 56E4
0907                          ANDAB BREGS,BF2LS,BREGD                                    000908
0907 P00E3 EF84
0908                TST19     YA    BREGS,AOUTUD                                         000909
0908 P00E4 C9F4
0909                          LDC   RAMADD,$06                                           000910
0909 P00E5 8406
0910                          CJP   NRZI,TST24        SAMPLE NRZI STATUS                 000911
0910 P00E6 6A96
0911                          ANDAB RAMS,BF2LS,AOUTLD                                    000912
0911 P00E7 ECB0
0912                          UJP   RPL1                                                 000913
0912 P00E8 0020
0913          0096 P          ORG   START1+$96                                           000914
0914                TST24     ORCB  RAMS,BF2LS,AOUTLD                                    000915
0914 P0096 ECD0
0915                          UJP   RPL1                                                 000916
0915 P0097 0020
0916                          SPARE                                                      000917
0916 P0098 FFFF
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0918            ********************************************************************      000919
0919            *                                                                  *      000920
0920            *                 *** FIRST WORD ADDRESS ***                       *      000921
0921            *                                                                  *      000922
0922            ********************************************************************      000923


0924      00E9 P        ORG  START1+$E9                                              000925
0925           FWA1   CA   AINLS,CWALD                                               000926
0925 P00E9 CA02
0926                  CA   AINUS,CWAUD          MOVE A LINES TO CWA REGISTER        000927
0926 P00EA CB03
0927                  UJP  RPL1                 EXIT                                000928
0927 P00EB 0020


0929            ********************************************************************      000930
0930            *                                                                  *      000931
0931            *                  *** BANK SELECT ***                             *      000932
0932            *                                                                  *      000933
0933            ********************************************************************      000934


0935           BKS1   CA   AINLS,BANKD          MOVE A LINES TO BANK REGISTER       000936
0935 P00EC C502
0936                  UJP  RPL1                 EXIT                                000937
0936 P00ED 0020
```

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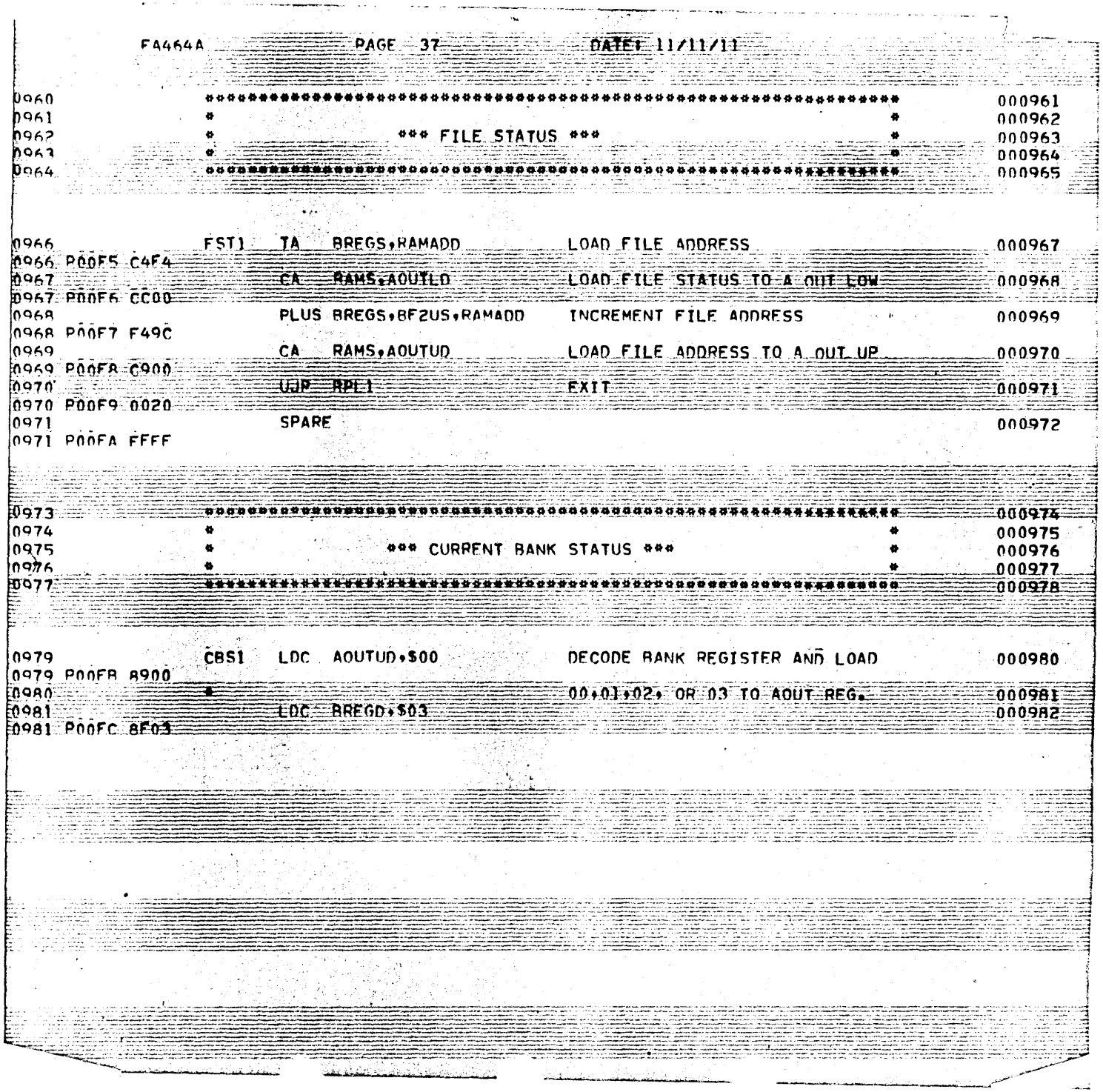
0938            ********************************************************************  000939
0939            *                                                                  *  000940
0940            *                    *** BLOCK LENGTH ***                          *  000941
0941            *                                                                  *  000942
0942            ********************************************************************  000943


0944            BL1   LDC  RAMADD,$08          MOVE A LINES TO FILE(8)AND            000945
0944 P00FE 8408
0945            *                              FILE(9)                               000946
0946                  TA   AINLS,RAMD                                                 000947
0946 P00FF C6F2
0947                  LDC  RAMADD,$09                                                 000948
0947 P00F0 8409
0948                  TA   AINUS,RAMD                                                 000949
0948 P00F1 C6F3
0949                  UJP  RPL1                FXIT                                   000950
0949 P00F2 0020


0951            ********************************************************************  000952
0952            *                                                                  *  000953
0953            *                *** LOAD FILE ADDRESS ***                         *  000954
0954            *                                                                  *  000955
0955            ********************************************************************  000956


0957            LFA1  CA   AINLS,BREGD         MOVE A LINES TO B REGISTER            000958
0957 P00F3 CF02
0958                  UJP  RPL1                                                       000959
0958 P00F4 0020
```



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0960                ************************************************************      000961
0961                *                                                          *      000962
0962                *                  *** FILE STATUS ***                     *      000963
0963                *                                                          *      000964
0964                ************************************************************      000965


0966                FST1   TA    BREGS,RAMADD          LOAD FILE ADDRESS                000967
0966 P00F5 C4F4
0967                       CA    RAMS,AOUTLD           LOAD FILE STATUS TO A OUT LOW    000968
0967 P00F6 CC00
0968                       PLUS  BREGS,8F2US,RAMADD    INCREMENT FILE ADDRESS           000969
0968 P00F7 F49C
0969                       CA    RAMS,AOUTUD           LOAD FILE ADDRESS TO A OUT UP    000970
0969 P00F8 C900
0970                       UJP   RPL1                  EXIT                             000971
0970 P00F9 0020
0971                       SPARE                                                      000972
0971 P00FA FFFF


0973                ************************************************************      000974
0974                *                                                          *      000975
0975                *              *** CURRENT BANK STATUS ***                 *      000976
0976                *                                                          *      000977
0977                ************************************************************      000978


0979                CBS1   LDC   AOUTUD,$00           DECODE BANK REGISTER AND LOAD    000980
0979 P00FB 8900
0980                *                                 00,01,02, OR 03 TO AOUT REG.     000981
0981                       LDC   BREGD,$03                                            000982
0981 P00FC 8F03
```

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0983                        CJP   CWAUL,CBS6                                  000984
0983 P00FD 3700
0984                        LDC   BF2LD,$02                                   000985
0984 P00FE 8D02
0985                        ANDAB BREGS,BF2LS,BREGD                           000986
0985 P00FF EFB4
0986                  CBS6  CJP   CWAUM,CBS9                                  000987
0986 P0100 2F03
0987                        LDC   BF2LD,$01                                   000988
0987 P0101 8D01
0988                        ANDAB BREGS,BF2LS,BREGD                           000989
0988 P0102 EFB4
0989                  CBS9  TA    BREGS,AOUTLD                              000990
0989 P0103 CCF4
0990                        UJP   RPL1                  EXIT                  000991
0990 P0104 0020

0992                  ********************************************************* 000993
0993                  *                                                       * 000994
0994                  *              *** CURRENT WORD STATUS ***              * 000995
0995                  *                                                       * 000996
0996                  ********************************************************* 000997

0998                  CWS1  TB    CWALS,AOUTLD      MOVE CWA LOWER AND CWA UPPER 000999
0998 P0105 CCA0
0999                  *                             REGISTERS TO AOUT REGISTER  001000
1000                        TB    CWAUS,AOUTUD                                  001001
1000 P0106 D9A0
1001                        UJP   RPL1                  EXIT                  001002
1001 P0107 0020
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1003            ********************************************************************      001004
1004            *                                                                  *      001005
1005            *          *** ASSEMBLE/SENSE NEXT READY JUMP ROUTINE ***          *      001006
1006            *                                                                  *      001007
1007            ********************************************************************      001008


1009            ASJ1   CJP  ONBUSJC,RJC1          ON BUS? NO-REJECT                     001010
1009 P0108 3C22
1010                   SEF  RMBNKS                SET ROM BANK SELECT F/F               001011
1010 P0109 BF33
1011                   UJP  ASR1                  JUMP TO UPPER BANK                    001012
1011 P010A 015C

1013                   SEF  ONBUSFF               NOT USED SPARE COMMAND                001014
1013 P010B BF23
1014                   UJP  TRB1                  NOT USED SPARE COMMAND                001015
1014 P010C 0040

1016            ********************************************************************      001017
1017            *                                                                  *      001018
1018            *                  *** SELF TEST 1 ***                             *      001019
1019            *                                                                  *      001020
1020            ********************************************************************      001021


1022       0150 P       ORG  START1+$150                                               001023
1023            STA1    CA   AINUS,BREGD           SAVE A LINES                        001024
1023 P0150 CF03
1024                    CA   AINUS,BF2LD                                               001025
1024 P0151 CD03
1025                    CA   AINLS,BF2UD                                               001026
1025 P0152 CE02
1026                    TA   AINLS,CWAUD                                               001027
1026 P0153 CBF2
```

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1028                        SFF  BUSY                ENTER BUSY                    001029
1028 P0154 BF2E
1029                         RFFCL  EOP,RPLY                                      001030
1029 P0155 A303
1030                        DA   BREGS,BREGD        PERFORM ALU OPERATIONS AS PER 001031
1030 P0156 CFFC
1031                  *                             SELF TEST 1 EQUATION          001032
1032                        LSFT  BREGS,BREGD                                     001033
1032 P0157 CFCC
1033                        PLUS BREGS,CWAUS,BREGD                                001034
1033 P0158 DF9C
1034                        RFF  CNALU                                            001035
1034 P0159 AF20
1035                        IA   BREGS,BREGD                                      001036
1035 P015A CF0C
1036                        MINUS BREGS,BF2LS,BREGD                               001037
1036 P015B EF6C
1037                              ANDAR BREGS,BF2US,BREGD                         001038
1037 P015C FF84
1038                        OR   BREGS,BF2LS,AOUTLD                               001039
1038 P015D ECE4
1039                        IA   PCS,RAMD                                         001040
1039 P015E C60F
1040                        UJP  TDS1               CALL SUBROUTINE TO PERFORM    001041
1040 P015F 0172
1041                  *                             REGISTER TRANSFER AND FILE LOAD 001042
1042                        CB   BF2US,RAMD                                       001043
1042 P0160 F650
1043                  STA18 TB   BF2US,AOUTUD       LOAD TRANSFER DATA TO AOUT    001044
1043 P0161 F9A0
1044                  STA19 RFF  ENWDSY                                           001045
1044 P0162 AF1B
1045                        UJP  TRB1               EXIT                          001046
1045 P0163 0040
1046                        SPARE                                                 001047
1046 P0164 FFFF
1047                        SPARE                                                 001048
1047 P0165 FFFF
```

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1049          ********************************************************************** 001050
1050          *                                                                    * 001051
1051          *                  *** TEST DATA SUBROUTINE ***                      * 001052
1052          *                                                                    * 001053
1053          ********************************************************************** 001054

1055     0172 P       ORG  START1+$172                                              001056
1056          TDS1    LDC  BREGD,$F1                                                001057
1056 P0172 8FF1
1057          TDS2    TA   BREGS,RAMADD        LOAD INITIAL FILE ADDRESS            001058
1057 P0173 C4F4
1058                  CB   BF2US,RAMD          MOVE TRANSFER DATA THROUGH ALL       001059
1058 P0174 F650
1059          *                                REGISTERS                            001060
1060                  CA   RAMS,CWALD                                               001061
1060 P0175 CA00
1061                  TB   CWALS,WCD                                                001062
1061 P0176 C8A0
1062                  IA   WCS,BF2LD           INCREMENT TRANSFER DATA              001063
1062 P0177 CD09
1063                  TR   BF2LS,CWAUD                                              001064
1063 P0178 E8A0
1064                  TB1  CWAUS,BF2UD                                              001065
1064 P0179 DEA7
1065                  IA   BREGS,BREGD                                              001066
1065 P017A CF0C
1066                  CJP  COUT,TDS2           DATA INCREMENTED BY 16?              001067
1066 P017B 1873
1067          *                                NO - CONTINUE                        001068
1068                  LDC  RAMADD,$00                                               001069
1068 P017C 8400
1069                  IA   RAMS,PCD            RETURN                               001070
1069 P017D C708
1070                  SPARE                                                         001071
1070 P017E FFFF
1071                  SPARE                                                         001072
1071 P017F FFFF
1072                  SPARE                                                         001073
1072 P0180 FFFF
```

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1074            ****************************************************************   001075
1075            *                                                              *   001076
1076            *                    *** SELF TEST 2 ***                       *   001077
1077            *                                                              *   001078
1078            ****************************************************************   001079


1080            STB1   SFF   BUSY                   ENTER BUSY                     001081
1080 P0181 AF2E
1081                   RFFCL EOP,RPLY                                              001082
1081 P0182 A303
1082                   RFF   ONBUSFF                RESET FLIP FLOPS               001083
1082 P0183 AF23
1083                   RFF   SPRFF                                                 001084
1083 P0184 AF01
1084                   RFF   EOTST                                                 001085
1084 P0185 AF02
1085                   RFF   INX2FF                                                001086
1085 P0186 AF06
1086                   RFF   PARFF                                                 001087
1086 P0187 AF24
1087                   RFFCL SLCTDFF,CDMAER                                        001088
1087 P0188 AD05
1088                   CJP   LRCRCJC,STB62          CHEECK FOR RESET STATE         001089
1088 P0189 25C6
1089                   CJP   WRTODJC,STB62                                         001090
1089 P018A 19C6
1090                   CJP   RALTIJC,STB62                                         001091
1090 P018B 15C6
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1092                    CJP  OFLMTJC,STB62                              001093
1092 P018C 11C6
1093                    CJP  ALARMJC,STB62                             001094
1093 P018D 55C6
1094                    CJP  INX2JC,STB62                              001095
1094 P018F 4DC6
1095                    CJP  SPRJC,STB62                               001096
1095 P01AF 45C6
1096                    CJP  EOTSTJC,STB62                             001097
1096 P0190 41C6
1097                    CJP  SFMKJC,STB62                              001098
1097 P0191 39C6
1098                    CJP  PARJC,STB62                               001099
1098 P0192 35C6
1099                    CJP ALDENJC,STB62                              001100
1099 P0193 10C6
1100                    CJP  SLCTDJC,STB62                             001101
1100 P0194 2DC6
1101                    CJP  CERSTJC,STB62                             001102
1101 P0195 21C6
1102                    SFF  PARMD              SET FLIP FLOPS AND JUMP 001103
1102 P0196 BF18
1103                                            CONDITIONS             001104
1104                    SFF  WTRDMP                                    001105
1104 P0197 BF1F
1105                    SFFCL RWMOD,CLHER                              001106
1105 P0198 BA19
1106                    SFF  ENWDSY                                    001107
1106 P0199 BF1B
1107                    LDC  WCD,$02                                   001108
1107 P019A 8802
1108                    CJP  HFWRD,STB62                               001109
1108 P019B 3BC6
1109                    LDC  BREGD,$A5                                 001110
1109 P019C BFA5
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1111                    LDC  CWALD,$A5                                  001112
1111 P019D 8AA5
1112                    COMPR BREGS,CWALS                               001113
1112 P019F C36C
1113                    CJP  WORD,STB29      CHECK FOR SET STATE        001114
1113 P019F 28A1
1114                    UJP  STB62                                      001115
1114 P01A0 01C6
1115              STB29 CJP  EQUAL,STB31                                001116
1115 P01A1 1EA3
1116                    UJP  STB62                                      001117
1116 P01A2 01C6
1117              STB31 CJP  COUT,STB33                                 001118
1117 P01A3 18A5
1118                    UJP  STB62                                      001119
1118 P01A4 01C6
1119              STB33 CJP  HFWRD,STB34                                001120
1119 P01A5 38A7
1120                    UJP  STB62                                      001121
1120 P01A6 01C6
1121              STB34 CJP  WCEMPT,STB36                               001122
1121 P01A7 31A9
1122                    UJP  STB62                                      001123
1122 P01A8 01C6
1123              STB36 CJP  BMDL,STB38                                 001124
1123 P01A9 29AB
1124                    UJP  STB62                                      001125
1124 P01AA 01C6
1125              STB38 CJP  BMSB,STB40                                 001126
1125 P01AB 51A0
1126                    UJP  STB62                                      001127
1126 P01AC 01C6
1127              STB40 PLUS BREGS,CWALS,BREGD     CHECK FOR SET STATE  001128
1127 P01AD CF9C
1128                    CJP  COUT,STB62                                 001129
1128 P01AE 18C6
```

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1130                        CJP   AMDL,STB62                          001131
1130 P01AF 29C6
1131                        CJP   BMSR,STB62                          001132
1131 P01B0 51C6
1132                        CJP   WORD,STB62                          001133
1132 P01B1 28C6
1133                        SFFCL SPRFF,CLSTAT                        001134
1133 P01B2 B701
1134                        PLUS  BREGS,BF2US,NU                      001135
1134 P01B3 F39C
1135                        CJP   FRSTDT,STB49                        001136
1135 P01B4 27B6
1136                        UJP   STB62                               001137
1136 P01B5 01C6
1137                  STB49 CJP   COUT,STB51                          001138
1137 P01B6 1888
1138                        UJP   STB62                               001139
1138 P01B7 01C6
1139                  STB51 COMPR BREGS,BF2US                         001140
1139 P01B8 F36C
1140                        CJP   EQUAL,STB62                         001141
1140 P01B9 1FC6
1141                        CJP   COUT,STB62                          001142
1141 P01BA 1BC6
1142                        CJP   FRSTDT,STB62                        001143
1142 P01BB 27C6
1143                        SFFCL ENBDB,SETHER                        001144
1143 P01BC BB1D
1144                        CJP   BF1F,STB62                          001145
1144 P01BD 33C6
1145                        CJP   BF2F,STB62                          001146
1145 P01BE 0FC6
1146                        CJP   DMAWCP,STB62                        001147
1146 P01BF 3FC6
1147                        CJP   CRCERJC,STB62                       001148
1147 P01C0 5BC6
1148                        CJP   PARERR,STB62                        001149
1148 P01C1 0BC6
```

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1150                      CJP   PRTFLT,STB62                              001151
1150 P01C2 17C6
1151                      CJP   ADRERR,STB62                              001152
1151 P01C3 07C6
1152                      CJP   WCEMPT,STB62                              001153
1152 P01C4 31C6
1153                      CJP   DMAWCP,STB77                              001154
1153 P01C5 3FCA
1154                STB62 LDC   AOUTLD,$AD    ERROR DETECTED - LOAD "DEAD"  001155
1154 P01C6 8CAD
1155                      LDC   AOUTUD,$DE                                001156
1155 P01C7 B9DE
1156                      RFF   JGRP9                                     001157
1156 P01C8 AF29
1157                      UJP   STA19         EXIT                        001158
1157 P01C9 0162
1158                STB77 SFFCL JGRP9,SFTHER                              001159
1158 P01CA BB29
1159                      CJP   NOCOMP,STB62                              001160
1159 P01CB 05C6
1160                      RFFCL JGRP9,SWSTR                               001161
1160 P01CC AF29
1161                      CJP   WORD,STB82                                001162
1161 P01CD 2BCF
1162                      UJP   STB62                                     001163
1162 P01CE 01C6
1163                STB82 SFF   INTRSP                                    001164
1163 P01CF BF2B
1164                      SFFCL LWD,SWSTR                                 001165
1164 P01D0 BF15
1165                      SFFCL FMKST,SRSTR   SET FLIP FLOPS              001166
1165 P01D1 B604
```

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1167                    SFF   LRCRCFF                                          001168
1167 P01D2 BF34
1168                    SFF   WRTODFF                                         001169
1168 P01D3 BF09
1169                    SFF   RALTIFF                                         001170
1169 P01D4 BF08
1170                    SFF   OFLMTFF                                         001171
1170 P01D5 BF0A
1171                    SFF   ALARMFF                                         001172
1171 P01D6 BF2F
1172                    SFF   INX2FF                                          001173
1172 P01D7 BF06
1173                    SFF   SLCTDFF                                         001174
1173 P01D8 BF05
1174                    SFF   FOTST                                           001175
1174 P01D9 BF02
1175                    SFF   SFMKFF                                          001176
1175 P01DA BF32
1176                    SFF   PARFF                                           001177
1176 P01DB BF24
1177                    RFF   ALDENFF                                         001178
1177 P01DC AF0C
1178                    SFF   CERST                                           001179
1178 P01DD BF30
1179                    CJP   ONBUSJC,STB101      CHECK FOR SET STATE         001180
1179 P01DE 3DE0
1180                    UJP   STB62                                           001181
1180 P01DF 01C6
1181            STB101  CJP   LRCRCJC,STB103                                  001182
1181 P01E0 25E2
1182                    UJP   STB62                                           001183
1182 P01E1 01C6
1183            STB103  CJP   WRTODJC,STB105                                  001184
1183 P01E2 19E4
1184                    UJP   STB62                                           001185
1184 P01E3 01C6
1185            STB105  CJP   RALTIJC,STB107                                  001186
1185 P01E4 15E6
```

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1187                  UJP  STB62                              001188
1187 P01F5 01C6
1188           STB107 CJP  OFLMTJC,STB109                     001189
1188 P01F6 11E8
1189                  UJP  STB62                              001190
1189 P01F7 01C6
1190           STB109 CJP  ALARMJC,STB111                     001191
1190 P01F8 55EA
1191                  UJP  STB62                              001192
1191 P01F9 01C6
1192           STB111 CJP  INX2JC,STB113                      001193
1192 P01EA 4DEC
1193                  UJP  STB62                              001194
1193 P01EB 01C6
1194           STB113 CJP  SPRJC,STB115                       001195
1194 P01EC 45EE
1195                  UJP  STB62                              001196
1195 P01ED 01C6
1196           STB115 CJP  EOTSTJC,STB117                     001197
1196 P01EE 41F0
1197                  UJP  STB62                              001198
1197 P01EF 01C6
1198           STB117 CJP  SEMKJC,STB119                      001199
1198 P01F0 39F2
1199                  UJP  STB62                              001200
1199 P01F1 01C6
1200           STB119 CJP  PARJC,STB121                       001201
1200 P01F2 35F4
1201                  UJP  STB62                              001202
1201 P01F3 01C6
1202           STB121 UJP  STB123                             001203
1202 P01F4 01F6
1203                  UJP  STB62                              001204
1203 P01F5 01C6
1204           STB123 CJP  CERSTJC,BKT1                       001205
1204 P01F6 2133
```

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1206                    UJP   STB62                                        001207
1206 P01E7 01C6
1207                    UJP   STB62                                        001208
1207 P01E8 01C6
1208              STB126 SEF   RMBNKS                                      001209
1208 P01E9 AF33
1209                    UJP   STB128      JUMP TO UPPER ROM BANK           001210
1209 P01EA 01F8

1211                    LDC   AOUTUD*$AC  NOT USED SPARE COMMAND           001212
1211 P01EB 89AC
1212                    UJP   TRB11       NOT USED SPARE COMMAND           001213
1212 P01EC 004E

1214       03F8 P       ORG   START1+$3F8                                  001215
1215              STB128 LDC   AOUTLD*$ED  NO ERRORS - LOAD "ACED"          001216
1215 P03F8 ACED
1216                    *                 TO AOUT REGISTER                 001217
1217                    LDC   AOUTUD*$AC                                   001218
1217 P03F9 89AC
1218                    REF   RMBNKS                                       001219
1218 P03FA AF33
1219                    UJP   STA19       EXIT                             001220
1219 P03FB 0162
1220                    SPARE                                              001221
1220 P03FC FFFF
1221                    SPARE                                              001222
1221 P03FD FFFF
1222                    SPARE                                              001223
1222 P03FE FFFF
1223                    SPARE                                              001224
1223 P03FF FFFF
```

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1225                ******** SELF TEST 2  BANK REG CHECK SUBSECTION ******************   001226


1227        0133 P          ORG  START1+$133                                            001228
1228                BKT1    LDC  BANKD,$FF          LOAD 3 TO BANK REGISTER            001229
1228 P0133 85FF
1229                        CJP  CWAUL,BKT4          VERIFY                             001230
1229 P0134 3736
1230                        UJP  STB62                                                  001231
1230 P0135 01C6
1231                BKT4    CJP  CWAUM,BKT6                                             001232
1231 P0136 2F38
1232                        UJP  STB62                                                  001233
1232 P0137 01C6
1233                BKT6    LDC  BANKD,$00          LOAD 0 TO BANK REGISTER            001234
1233 P0138 8500
1234                        CJP  CWAUL,STB62         VERIFY                             001235
1234 P0139 37C6
1235                        CJP  CWAUM,STB62                                            001236
1235 P013A 2FC6


1237                ******** SELF 2 PARITY GENERATOR CHECK SUBSECTION *************      001238


1239                        LDC  BREGD,$FF           INITIALIZE DATA                    001240
1239 P013B 8FFF
1240                PCH2    TA   BREGS,BREGD         PASS DATA THROUGH PARITY GEN.      001241
1240 P013C CFF4
1241                        CJP  PARLT,STB62         CHECK PARITY BIT OUTPUT LOW        001242
1241 P013D 69C6
1242                        LSFT BREGS,BREGD                                            001243
1242 P013E CFCC
1243                        CJP  COUT,PCH13          DATA SHIFTED 8 TIMES? YES-EXIT     001244
1243 P013F 1B46
```

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1245                        TA    BREGS,BREGD          PASS DATA THROUGH PARITY GEN.    001246
1245 P0140 CFF4
1246                        CJP   PARLT,PCH10          CHECK PARITY OUTPUT HIGH         001247
1246 P0141 6943
1247                        UJP   STB62                                                 001248
1247 P0142 01C6
1248                  PCH10 LSFT  BREGS,BREGD                                         001249
1248 P0143 CFCC
1249                        CJP   COUT,STB62                                          001250
1249 P0144 1BC4
1250                        UJP   PCH2                 CONTINUE SHIFT LOOP            001251
1250 P0145 013C
1251                  PCH13 CJP   WSTRLT,PCH15         CHECK RSTR AND WSTR LATCH HIGH 001252
1251 P0146 4B48
1252                        UJP   STB62                                               001253
1252 P0147 01C6
1253                  PCH15 CJP   RSTRLT,PCH17                                        001254
1253 P0148 534A
1254                        UJP   STB62                                               001255
1254 P0149 01C6
1255                  PCH17 RFFCL PARMD,CLOSTR         CHANGE PARITY MODE             001256
1255 P014A A41B
1256                        CJP   RSTRLT,STB62         CHECK RSTR WSTR LATCH LOW      001257
1256 P014B 4BC6
1257                        CJP   RSTRLT,STB62                                        001258
1257 P014C 53C6
1258                        TA    BREGS,BREGD                                         001259
1258 P014D CFF4
1259                        CJP   PARLT,STB126         CONTINUE                       001260
1259 P014E 69F9
1260                        UJP   STB62                                               001261
1260 P014F 01C6
```

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1262                ********************************************************************      001263
1263                *                                                                  *      001264
1264                *                        *** SELF TEST 4 ***                       *      001265
1265                *                                                                  *      001266
1266                ********************************************************************      001267


1268          0126 P        ORG START1+$126                                              001269
1269                  STD1    CA    AINL5+BF2LD          LOAD A LINES TO DMA INTERFACE     001270
1269 P0126 CD02
1270                  *                                  REGISTER                          001271
1271                          CA    AINUS+BF2UD                                            001272
1271 P0127 CE03
1272                          CJP   PRGPRT+STC4          SAMPLE PROTECT BIT OF             001273
1272 P0128 0D6A
1273                  *                                  INSTRUCTION                       001274
1274                          SFF   DMWRPT                                                 001275
1274 P0129 BF2C
1275                          UJP   STC4                 CONTINUE                          001276
1275 P012A 016A
```

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1277        ********************************************************************      001278
1278        *                                                                  *      001279
1279        *                    *** SELF TEST 3 ***                           *      001280
1280        *                                                                  *      001281
1281        ********************************************************************      001282


1283    0166 P      ORG  START1+$166                                             001284
1284          STC1  SFF  WTRDMP          SET F/F'S FOR DMA READ                  001285
1284 P0166 BF1F
1285                SFF  COMP1                                                   001286
1285 P0167 BF1A
1286                SFF  SELBF2                                                  001287
1286 P0168 BF10
1287                SFF  SELRF1                                                  001288
1287 P0169 BF17
1288          STC4  SFFCL BUSY,SFTHFR    ENTER BUSY                              001289
1288 P016A BB2F
1289                RFFCL EOP,RPLY                                               001290
1289 P016B A303
1290                SFFCL ENRDR,DMAREQ     SEND DMA REQUEST                      001291
1290 P016C B210
1291          STC6A CJP  DMAWCP,STC9       WAIT FOR END OF DMA CYCLE             001292
1291 P016D 3F70
1292                CJP  BF2F,STC9                                               001293
1292 P016E 0F70
1293                UJP  STC6A                                                   001294
1293 P016F 0160
1294          STC9  TB   BF2LS,AOUTLO      MOVE DMA DATA TO AOUT REG.            001295
1294 P0170 ECA0
1295                UJP  STA18             EXIT                                  001296
1295 P0171 0161
```

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1297                 ****************************************************************   001298
1298                 *                                                              *   001299
1299                 *                 *** DIRECTOR FUNCTION DECODE ***             *   001300
1300                 *                                                              *   001301
1301                 ****************************************************************   001302

1303        010D P          ORG   START1+$10D                                          001304
1304                 DFD1   CJP   RDY,DFD1B             CHECK UNIT READY               001305
1304 P010D 750F
1305                        UJP   RJC1                  UNIT NOT READY-REJECT          001306
1305 P010F 0022
1306                 DFD1B  CJP   ONBUSJC,RJC1          CHECK ON BUS                   001307
1306 P010F 3C22
1307                        CJP   SLCTDJC,DFD5          CHECK IF UNIT SELECTED         001308
1307 P0110 2D12
1308                        UJP   RJC1                  UNIT DESELECTED,REJECT         001309
1308 P0111 0022
1309                 DFD5   TA    AINLS,BF2LD                                          001310
1309 P0112 CDF2
1310                        COMPR AINLS,BF2LS                                          001311
1310 P0113 F36A
1311                        CJP   EQUAL,DFD9            COMPARE TWO A LINE SAMPLES     001312
1311 P0114 1F16
1312                        UJP   RJC1                  NO COMPARE,REJECT              001313
1312 P0115 0022
1313                 DFD9   CJP   PRGPRT,DFD10          CHECK IF INSTRUCTION PROTECTED 001314
1313 P0116 0D18
1314                        SFF   DMWRPT                YES,SET DMA PROTECT            001315
1314 P0117 BF2C
1315                 DFD10  SFF   BUSY                  ENTER BUSY                     001316
1315 P0118 BF2E
1316                        REFCL FOP,RPLY              ISSUE REPLY                    001317
1316 P0119 A303
1317                        PLUS  PCS,BF2US,RAMD                                       001318
1317 P011A F69F
1318                        UJP   CST1                  INITIALIZE STATUSES            001319
1318 P011B 0085
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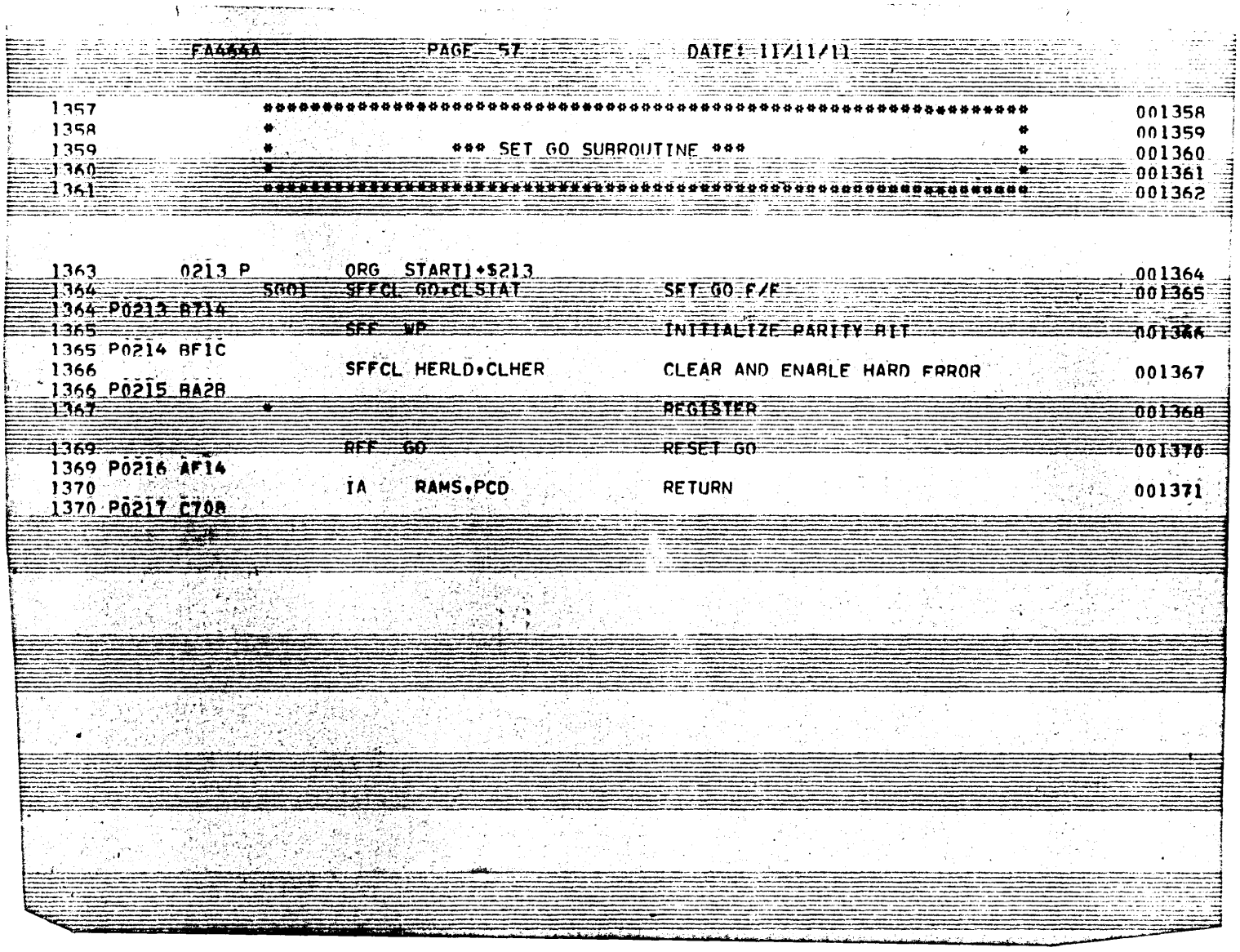
1320                            LDC   WCD,$F          LOAD MASK FOR PRELOAD                001321
1320 P011C 880F
1321                            TB    RF2LS,RREGD                                          001322
1321 P011D EFA0
1322                            CJP   BMDL,DFD14      CHECK THRESHOLD LEVEL SELECT         001323
1322 P011E 2920
1323                            SFF   THR             LOW THRESHOLD                        001324
1323 P011F BF37
1324                  DFD14     REF   WRTODFF                                              001325
1324 P0120 AF09
1325                            CJP   BMSB,DFD17      CHECK IF WRITE IS ODD                001326
1325 P0121 5123
1326                            SFF   WRTODFF         WRITE ODD                            001327
1326 P0122 BF09
1327                  DFD17     SFF   RMBNKS          PREPARE JUMP TO UPPER BANK           001328
1327 P0123 BF33
1328                            UJP   DFD18A          JUMP TO UPPER BANK                   001329
1328 P0124 0010
1329                            SPARE                                                      001330
1329 P0125 FFFF
1330          0210 P            ORG   START1,$210                                         001331
1331                  DFD18A    TA    PCS,NU          INITIALIZE BITS 9 AND A OF PC        001332
1331 P0210 C3F7
1332                            REF   CNALU                                                001333
1332 P0211 AF20
1333                            ANDCB WCS,RF2LS,PCD   MASK AND PRELOAD DIRECTOR            001334
1333 P0212 E771
1334                  *                               FUNCTION CODE BITS A0-A3             001335
1335                            SPARE                                                      001336
1335 P0213 FFFF
```

```
1337                ********** DIRECTOR FUNCTION A0-A3 DECODE **********                001338


1339      0200 P    ORG  START1*$200                                                    001340
1340                UJP  RD1          READ DATA                                        001341
1340 P0200 0097
1341                UJP  SPF1         SPACE FORWARD                                    001342
1341 P0201 0072
1342                UJP  SFF1         SEARCH FILE MARK FORWARD                         001343
1342 P0202 005F
1343                UJP  SFB1         SEARCH FILE MARK BACKWARD                        001344
1343 P0203 006D
1344                UJP  BSP1         BACKSPACE                                        001345
1344 P0204 0070
1345                UJP  WT1          WRITE DATA                                       001346
1345 P0205 01DB
1346                UJP  WRF1         WRITE FILE MARK                                  001347
1346 P0206 0084
1347                UJP  RWD1         REWIND                                           001348
1347 P0207 0052
1348                UJP  FER0         FIXED ERASE                                      001349
1348 P0208 008A
1349                UJP  VER1         VARIABLE ERASE                                   001350
1349 P0209 0077
1350                UJP  CNB1         CONTROLLED BACKSPACE                             001351
1350 P020A 0074
1351                UJP  ROL1         REWIND OFF LINE                                  001352
1351 P020B 0055
1352                UJP  TRD7B        ILLEGAL COMMAND*NOP                              001353
1352 P020C 0106
1353                UJP  TRD7B        ILLEGAL COMMAND*NOP                              001354
1353 P020D 0106
1354                UJP  TRD7B        ILLEGAL COMMAND*NOP                              001355
1354 P020E 0108
1355                UJP  TRD7B        ILLEGAL COMMAND*NOP                              001356
1355 P020F 0106
```



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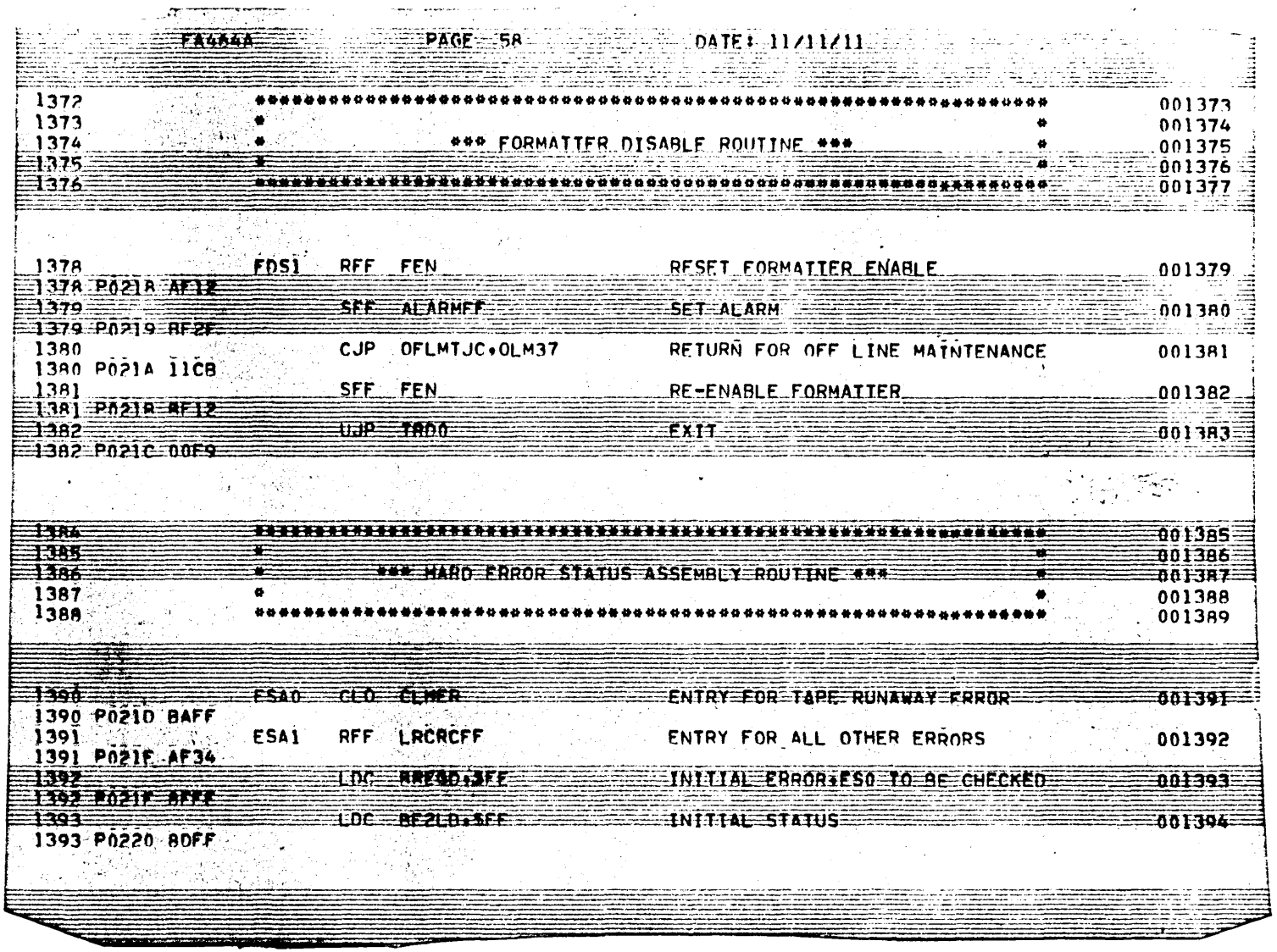
1357          ********************************************************************          001358
1358          *                                                                  *          001359
1359          *                  *** SET GO SUBROUTINE ***                       *          001360
1360          *                                                                  *          001361
1361          ********************************************************************          001362


1363     0213 P       ORG   START1+$213                                                     001364
1364               5001  SFFCL GO+CLSTAT          SET GO F/F                             001365
1364 P0213 B714
1365                     SFF   WP                 INITIALIZE PARITY BIT                  001366
1365 P0214 BF1C
1366                     SFFCL HERLD+CLHER        CLEAR AND ENABLE HARD ERROR            001367
1366 P0215 BA2B
1367          *                                   REGISTER                               001368

1369                     RFF   GO                 RESET GO                               001370
1369 P0216 AF14
1370                     IA    RAMS+PCD           RETURN                                 001371
1370 P0217 C708
```



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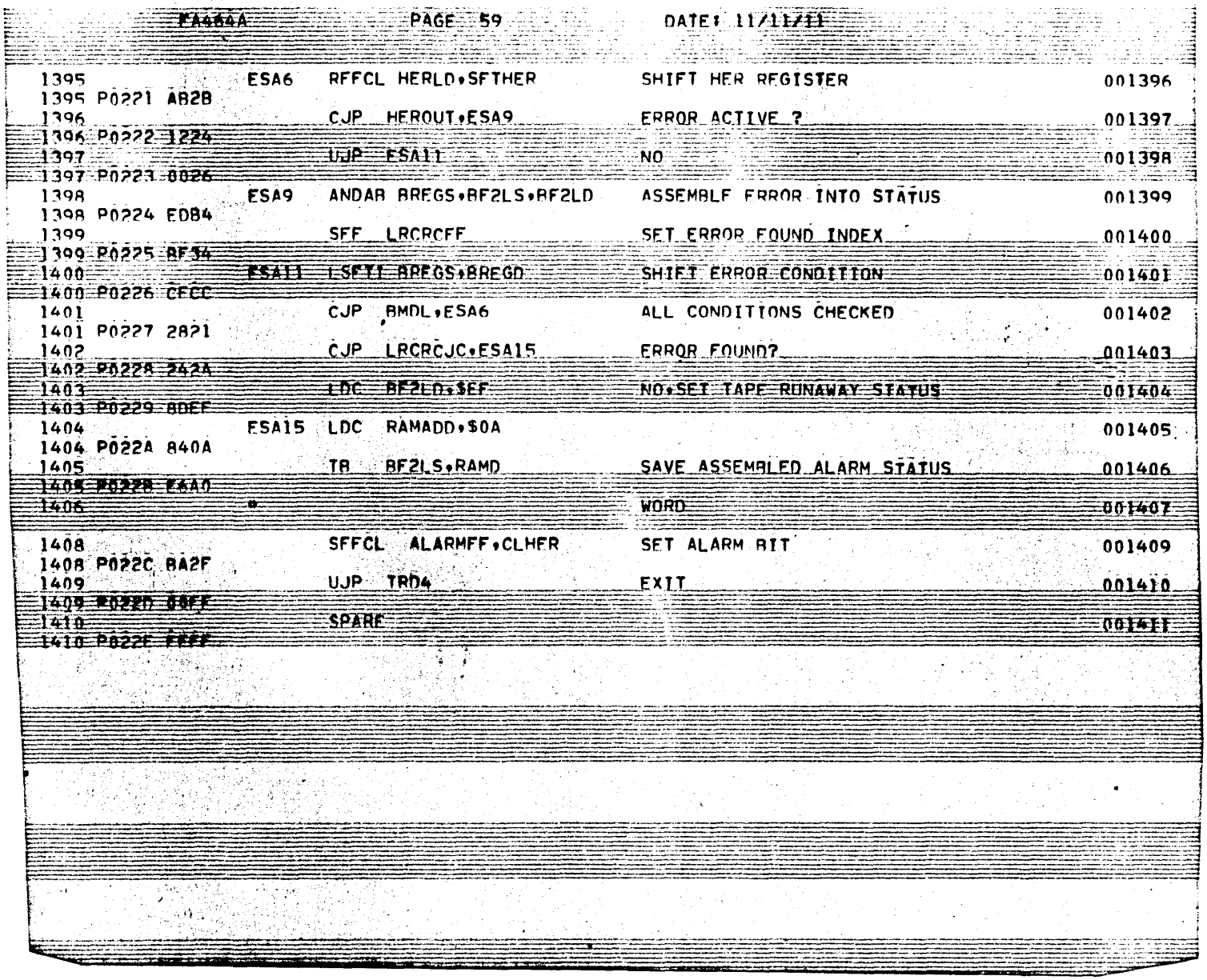
1372        ********************************************************************** 001373
1373        *                                                                    * 001374
1374        *                *** FORMATTER DISABLE ROUTINE ***                   * 001375
1375        *                                                                    * 001376
1376        ********************************************************************** 001377


1378        FDS1  RFF  FEN                 RESET FORMATTER ENABLE               001379
1378 P021B AF12
1379              SFF  ALARMFF             SET ALARM                            001380
1379 P021D AF2F
1380              CJP  OFLMTJC+OLM37       RETURN FOR OFF LINE MAINTENANCE      001381
1380 P021A 11CB
1381              SFF  FEN                 RE-ENABLE FORMATTER                  001382
1381 P021B AF12
1382              UJP  TADD                EXIT                                 001383
1382 P021C 00F9


1384        ********************************************************************** 001385
1385        *                                                                    * 001386
1386        *        *** HARD ERROR STATUS ASSEMBLY ROUTINE ***                  * 001387
1387        *                                                                    * 001388
1388        ********************************************************************** 001389


1390        ESA0  CLO  CLMER               ENTRY FOR TAPE RUNAWAY ERROR         001391
1390 P021D BAFF
1391        ESA1  RFF  LRCRCFF             ENTRY FOR ALL OTHER ERRORS           001392
1391 P021F AF34
1392              LDC  RRESD+3FF           INITIAL ERROR+ESD TO BE CHECKED      001393
1392 P021F BFFF
1393              LDC  BF2LD+3FF           INITIAL STATUS                       001394
1393 P0220 80FF
```



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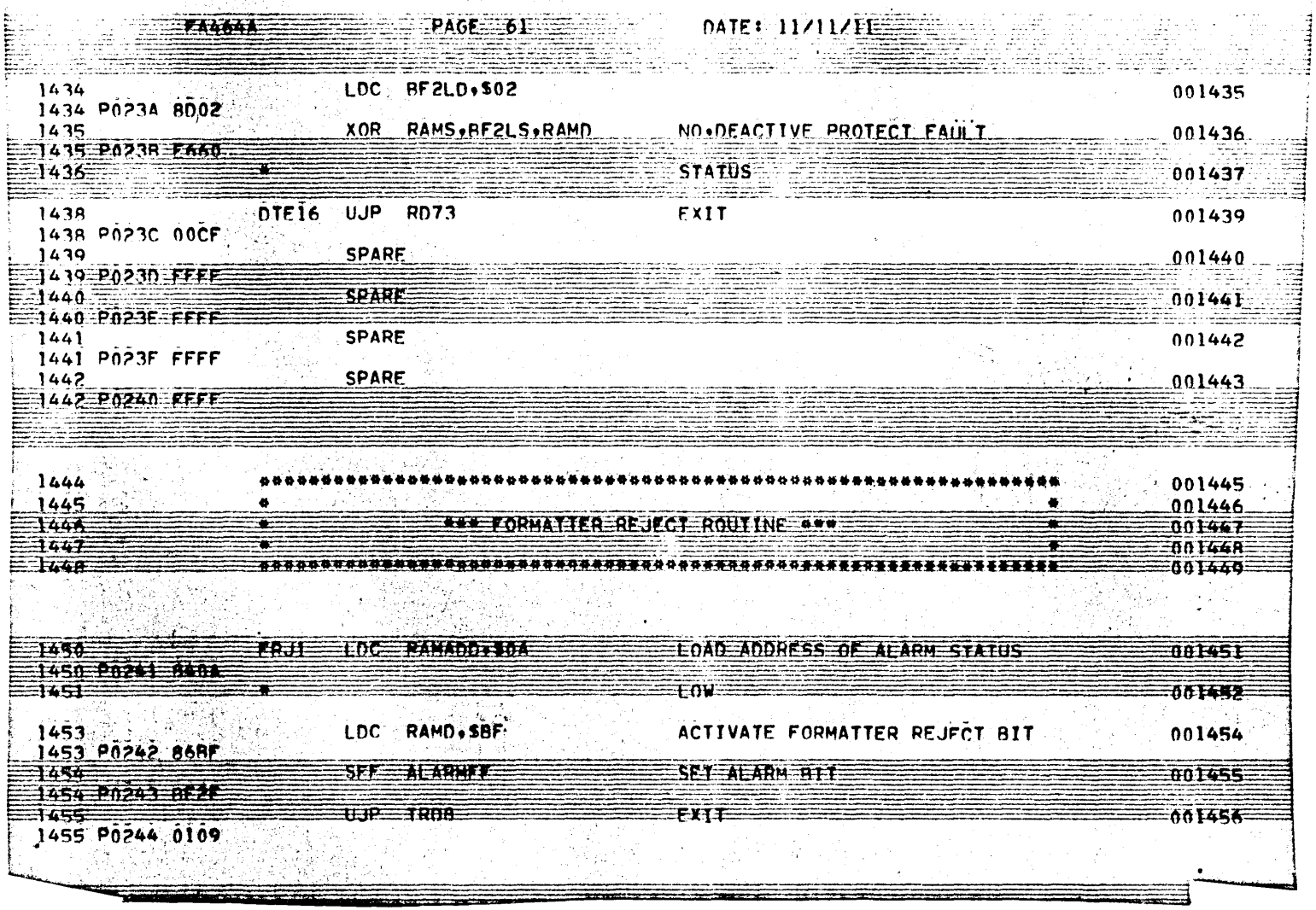
1395                ESA6  RFFCL HERLD,SFTHER        SHIFT HER REGISTER                001396
1395 P0221 AB2B
1396                      CJP   HEROUT,ESA9          ERROR ACTIVE ?                    001397
1396 P0222 1224
1397                      UJP   ESA11               NO                                001398
1397 P0223 0026
1398                ESA9  ANDAR BREGS,BF2LS,BF2LD     ASSEMBLE ERROR INTO STATUS        001399
1398 P0224 E0B4
1399                      SFF   LRCRCFF             SET ERROR FOUND INDEX             001400
1399 P0225 BF34
1400                ESA11 LSFTI BREGS,BREGD         SHIFT ERROR CONDITION             001401
1400 P0226 CFCC
1401                      CJP   BMDL,ESA6           ALL CONDITIONS CHECKED            001402
1401 P0227 2821
1402                      CJP   LRCRCJC,ESA15       ERROR FOUND?                      001403
1402 P0228 242A
1403                      LDC   BF2LD,$EF           NO,SET TAPE RUNAWAY STATUS        001404
1403 P0229 8DEF
1404                ESA15 LDC   RAMADD,$0A                                            001405
1404 P022A 840A
1405                      TB    BF2LS,RAMD          SAVE ASSEMBLED ALARM STATUS       001406
1405 P022B E6A0
1406                *                               WORD                              001407

1408                      SFFCL ALARMFF,CLHER       SET ALARM BIT                     001409
1408 P022C BA2F
1409                      UJP   TRD4                EXIT                              001410
1409 P022D 00FF
1410                      SPARE                                                       001411
1410 P022E FFFF
```

```
1412            ******************************************************************   001413
1413            *                                                                *   001414
1414            *          *** DMA TRANSFER ERROR  ROUTINE ***                   *   001415
1415            *                                                                *   001416
1416            ******************************************************************   001417

1418            DTE0   RFF   SELBF2                                                  001419
1418 P022F AF10
1419                   LDC   RAMADD,$08           LOAD ADDRESS OF ALARM STATUS UP    001420
1419 P0230 8408
1420                   LDC   RAMD,$F1             ACTIVATE ALL ERROR STATUSES        001421
1420 P0231 86F1
1421                   SFF   LWD                  TERMINATE ANY WRITE OPERATION      001422
1421 P0232 BF15
1422                   CJP   PARERR,DTE8          PARITY ERROR?                      001423
1422 P0233 0A36
1423                   LDC   BF2LD,$08                                               001424
1423 P0234 8D08
1424                   XOR   RAMS,BF2LS,RAMD      NO,DEACTIVATE PARITY ERROR         001425
1424 P0235 E660
1425            *                                 STATUS                             001426
1427            DTE8   CJP   ADRERR,DTE12         ADDRESS ERROR?                     001428
1427 P0236 0639
1428                   LDC   BF2LD,04                                                001429
1428 P0237 8D04
1429                   XOR   RAMS,BF2LS,RAMD      NO,DEACTIVATE ADDRESS ERROR        001430
1429 P0238 E660
1430            *                                 STATUS                             001431
1432            DTE12  CJP   PRTFLT,DTE16         PROTECT FAULT?                     001433
1432 P0239 163C
```



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1434                      LDC  BF2LD,$02                                    001435
1434 P023A 8D02
1435                      XOR  RAMS,BF2LS,RAMD   NO.DEACTIVE PROTECT FAULT  001436
1435 P023B FA60
1436                 *                           STATUS                    001437

1438                 DTE16 UJP  RD73             EXIT                      001439
1438 P023C 00CF
1439                      SPARE                                             001440
1439 P023D FFFF
1440                      SPARE                                             001441
1440 P023E FFFF
1441                      SPARE                                             001442
1441 P023F FFFF
1442                      SPARE                                             001443
1442 P0240 FFFF


1444                 ********************************************************* 001445
1445                 *                                                       * 001446
1446                 *          *** FORMATTER REJECT ROUTINE ***             * 001447
1447                 *                                                       * 001448
1448                 ********************************************************* 001449


1450                 FRJ1 LDC  RAMADD,$0A        LOAD ADDRESS OF ALARM STATUS 001451
1450 P0241 8A0A
1451                 *                           LOW                       001452

1453                      LDC  RAMD,$BF          ACTIVATE FORMATTER REJECT BIT 001454
1453 P0242 86BF
1454                      SFF  ALARMFF           SET ALARM BIT              001455
1454 P0243 8F2F
1455                      UJP  TRDB              EXIT                       001456
1455 P0244 0109
```

```
1457                ********************************************************************          001458
1458                *                                                                  *          001459
1459                *          *** DECREMENT BLOCK LENGTH SUBROUTINE ***               *          001460
1460                *                                                                  *          001461
1461                ********************************************************          001462
1462                DBL1   LDC  RAMADD,$08          LOAD ADDRESS OF BLK LENGTH          001463
1462 P0245 8408
1463                *                               LOWER                               001464

1465                       IA   RAMS,RAMD           DECREMENT BLOCK LENGTH LOWER        001466
1465 P0246 C608
1466                       CJP  COUT,DBL11          CARRY OUT ACTIVE?                   001467
1466 P0247 1A4E
1467                       LDC  RAMADD,$09          YES,LOAD ADDRESS OF BLK LENGTH      001468
1467 P0248 8409
1468                *                               UPPER                               001469

1470                       IA   RAMS,RAMD           DECREMENT BLK LENGTH UPPER          001471
1470 P0249 C608
1471                       CJP  COUT,DBL11          CARRY OUT ACTIVE?                   001472
1471 P024A 1A4F
1472                       CJP  RDM,IFB1            BLK LENGTH=0;READ OPERATION?        001473
1472 P024B 6F50
1473                       CJP  WRTODJC,TWTO        WRITE ODD? WRITE ONLY UPPER         001474
1473 P024C 19EC
1474                *                               PART OF LAST WORD                   001475

1475                       UJP  TWT1                TERMINATE NORMAL WRITE              001477
1476 P024D 61ED
1477                DBL11  LDC  RAMADD,$00          BLK LENGTH NOT EQUAL 0;RETURN       001478
1477 P024E 8400
1478                       IA   RAMS,PCD                                                001479
1478 P024F C70A
```

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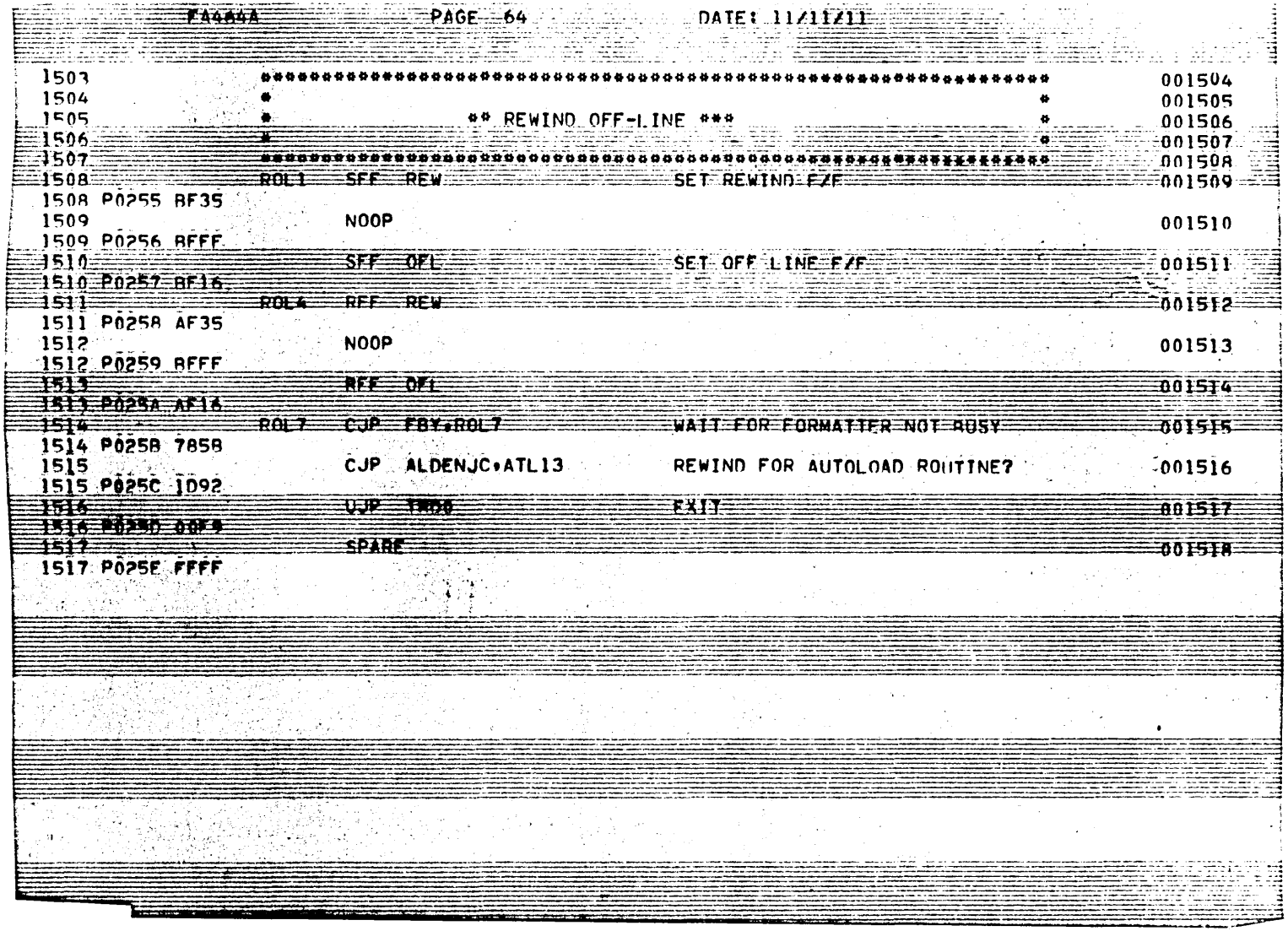
1480        ********************************************************************
1481        *                                                                  *
1482        *          *** TERMINATE FORMATTER BUSY ROUTINE ***                *
1483        *                                                                  *
1484        ********************************************************************


1486        TFB1    CJP   FBY,TFB3          FORMATTER BUSY?
1486 P0250 7868
1487                UJP   TR00              NO:EXIT
1487 P0251 00E9
1488      026B P    ORG   START1+$26B
1489        TFB3    CJP   RDY,TFB1          UNIT READY?
1489 P026B 7450
1490                UJP   FDS1              NO:DISABLE FORMATTER
1490 P026C 0018


1492        ********************************************************************
1493        *                                                                  *
1494        *                    *** REWIND ***                                *
1495        *                                                                  *
1496        ********************************************************************


1498      0252 P    ORG   START1+$252
1499        RWD1    SFF   REW               SET REWIND F/F
1499 P0252 8F35
1500                NOOP
1500 P0253 8FFF
1501                UJP   RDL4              CONTINUE
1501 P025A 0058
```



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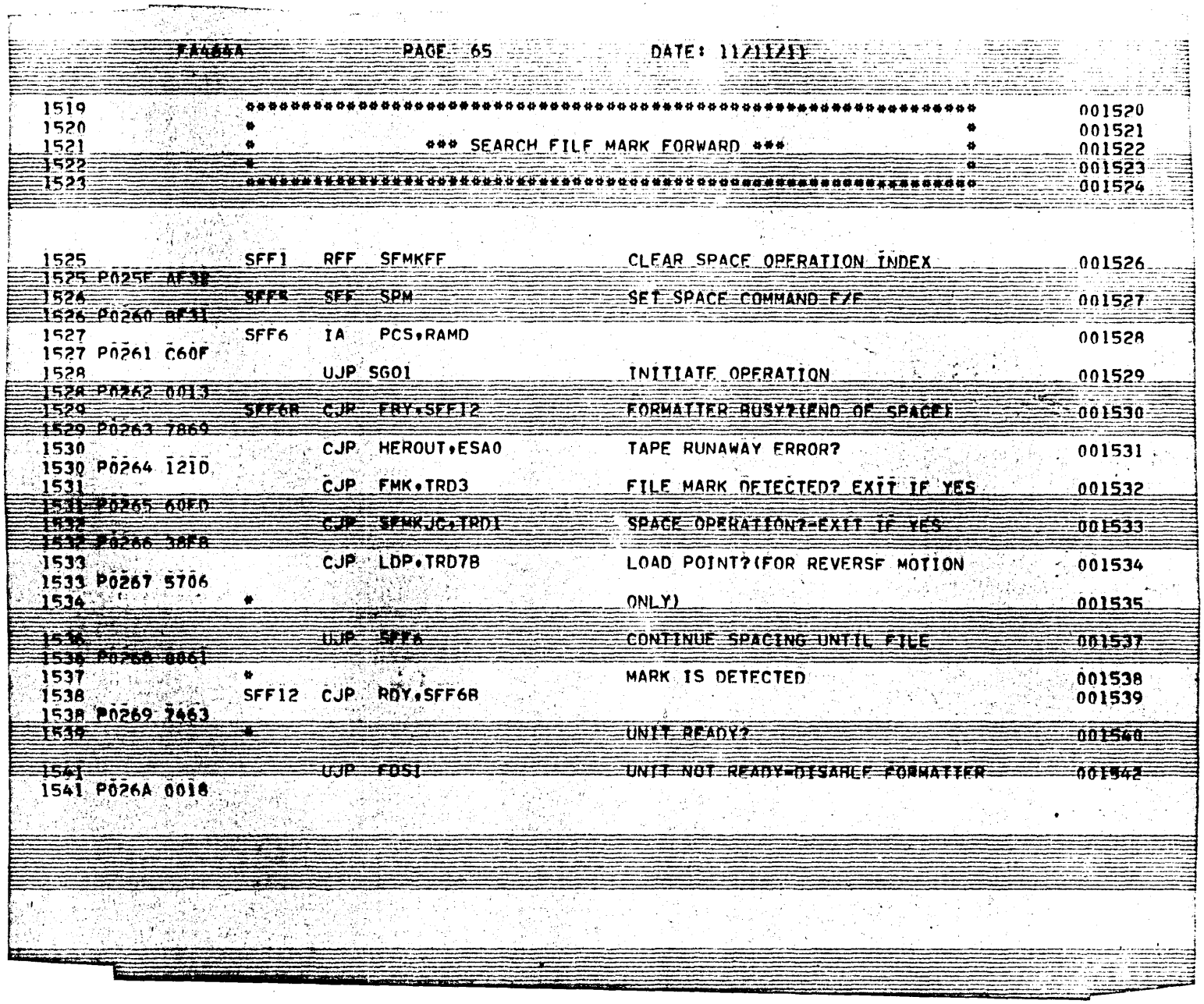
1503        ********************************************************************** 001504
1504        *                                                                    * 001505
1505        *                  ** REWIND OFF-LINE ***                            * 001506
1506        *                                                                    * 001507
1507        ********************************************************************** 001508
1508        ROL1  SFF  REW              SET REWIND F/F                          001509
1508 P0255 BF35
1509              NOOP                                                          001510
1509 P0256 BFFF
1510              SFF  OFL              SET OFF LINE F/F                        001511
1510 P0257 BF16
1511        ROL4  RFF  REW                                                      001512
1511 P0258 AF35
1512              NOOP                                                          001513
1512 P0259 BFFF
1513              RFF  OFL                                                      001514
1513 P025A AF18
1514        ROL7  CJP  FBY,ROL7         WAIT FOR FORMATTER NOT BUSY             001515
1514 P025B 785B
1515              CJP  ALDENJC,ATL13    REWIND FOR AUTOLOAD ROUTINE?            001516
1515 P025C 1D92
1516              UJP  EXIT             EXIT                                    001517
1516 P025D 08F9
1517              SPARE                                                         001518
1517 P025E FFFF
```



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1519  ********************************************************************** 001520
1520  *                                                                    * 001521
1521  *                *** SEARCH FILE MARK FORWARD ***                    * 001522
1522  *                                                                    * 001523
1523  ********************************************************************** 001524


1525          SFF1   RFF  SFMKFF          CLEAR SPACE OPERATION INDEX       001526
1525 P025F AF3E
1526          SFF8   SFF  SPM             SET SPACE COMMAND F/F             001527
1526 P0260 8F31
1527          SFF6   IA   PCS,RAMD                                          001528
1527 P0261 C60F
1528               UJP  SG01              INITIATE OPERATION                001529
1528 P0262 0013
1529          SFF6R  CJP  FRY,SFF12       FORMATTER BUSY?(END OF SPACE)     001530
1529 P0263 7869
1530               CJP  HEROUT,ESA0       TAPE RUNAWAY ERROR?               001531
1530 P0264 1210
1531               CJP  FMK,TRD3          FILE MARK DETECTED? EXIT IF YES   001532
1531 P0265 60ED
1532               CJP  SFMKJG,TRD1       SPACE OPERATION?-EXIT IF YES      001533
1532 P0266 38F8
1533               CJP  LDP,TRD7B         LOAD POINT?(FOR REVERSE MOTION    001534
1533 P0267 5706
1534          *                           ONLY)                             001535

1536               UJP  SFF6              CONTINUE SPACING UNTIL FILE       001537
1536 P0268 0861
1537          *                           MARK IS DETECTED                  001538
1538          SFF12  CJP  RDY,SFF6B                                         001539
1538 P0269 7463
1539          *                           UNIT READY?                       001540

1541               UJP  FDS1              UNIT NOT READY-DISABLE FORMATTER  001542
1541 P026A 0018
```

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1543                ****************************************************************         001544
1544                *                                                              *         001545
1545                *              *** SEARCH FILF MARK   BACKWARD ***             *         001546
1546                *                                                              *         001547
1547                ****************************************************************         001548


1549       026D P          ORG  START1+$26D                                                   001550
1550                SFR1   RFF  SFMKFF                CLEAR SPACE OPERATION INDEX F/F         001551
1550 P026D AF32
1551                SFR2   SFF  REV                   SET REVERSE COMMAND F/F                 001552
1551 P026E BF0D
1552                       UJP  SFF5                  CONTINUE                                001553
1552 P026F 0060


1554                ****************************************************************         001555
1555                *                                                              *         001556
1556                *              *** BACKSPACE ***                               *         001557
1557                *                                                              *         001558
1558                ****************************************************************         001559


1560                BSP1   SFF  SFMKFF                SET SPACE OPERATION INDEX F/F           001561
1560 P0270 AF32
1561                       UJP  SFR2                  CONTINUE                                001562
1561 P0271 006E
```

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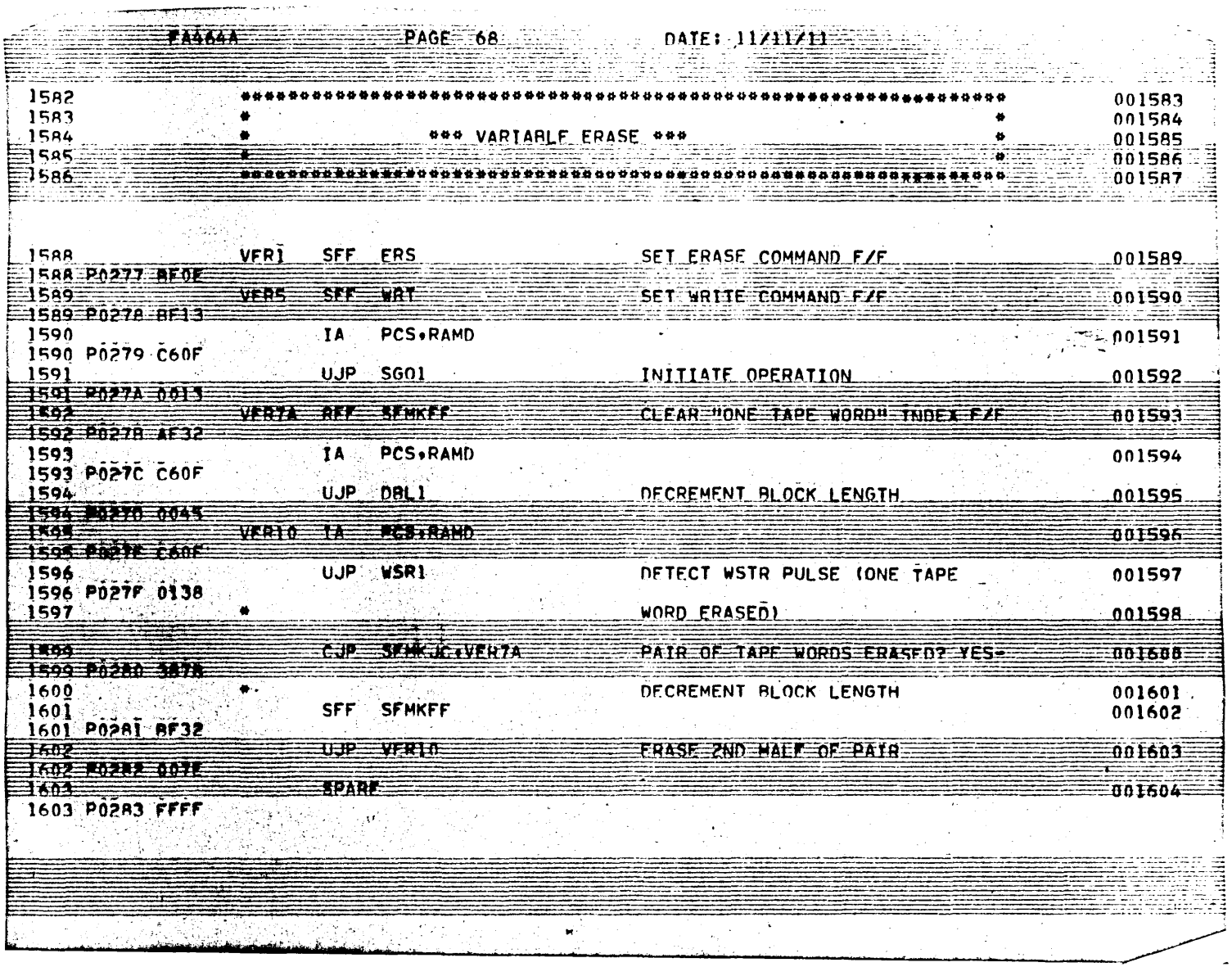
1563        ************************************************************      001564
1564        *                                                          *      001565
1565        *              *** SPACE FORWARD ***                       *      001566
1566        *                                                          *      001567
1567        ************************************************************      001568


1569        SPF1  SFF  SFMKFF              SET SPACE OPERATION INDEX F/F      001570
1569 P0272 BF32
1570              UJP  SFF5                CONTINUE                           001571
1570 P0273 0060


1572        ************************************************************      001573
1573        *                                                          *      001574
1574        *          *** CONTROLLED BACKSPACE ***                    *      001575
1575        *                                                          *      001576
1576        ************************************************************      001577


1578        CNB1  SFF  REV                 SET REVERSE COMMAND F/F            001579
1578 P0274 BF0D
1579              SFF  SPM                 SET SPACE MODE COMMAND F/F         001580
1579 P0275 BF3I
1580              UJP  VER5                CONTINUE                           001581
1580 P0276 0078
```



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1582  ********************************************************************  001583
1583  *                                                                  *  001584
1584  *                  *** VARIABLE ERASE ***                          *  001585
1585  *                                                                  *  001586
1586  ********************************************************************  001587


1588          VER1   SFF  ERS                 SET ERASE COMMAND F/F       001589
1588 P0277 BF0F
1589          VER5   SFF  WRT                 SET WRITE COMMAND F/F       001590
1589 P0278 BF13
1590                 IA   PCS+RAMD                                        001591
1590 P0279 C60F
1591                 UJP  SG01               INITIATE OPERATION          001592
1591 P027A 0013
1592          VER7A  RFF  SFMKFF              CLEAR "ONE TAPE WORD" INDEX F/F 001593
1592 P027B AF32
1593                 IA   PCS+RAMD                                        001594
1593 P027C C60F
1594                 UJP  DBL1               DECREMENT BLOCK LENGTH      001595
1594 P027D 0045
1595          VER10  IA   PCS+RAMD                                        001596
1595 P027E C60F
1596                 UJP  WSR1               DETECT WSTR PULSE (ONE TAPE 001597
1596 P027F 0138
1597          *                              WORD ERASED)                001598

1599                 CJP  SFMKJC+VER7A       PAIR OF TAPE WORDS ERASED? YES- 001600
1599 P0280 3B7A
1600          *                              DECREMENT BLOCK LENGTH      001601
1601                 SFF  SFMKFF                                         001602
1601 P0281 BF32
1602                 UJP  VER10              ERASE 2ND HALF OF PAIR      001603
1602 P0282 007E
1603                 SPARE                                               001604
1603 P0283 FFFF
```

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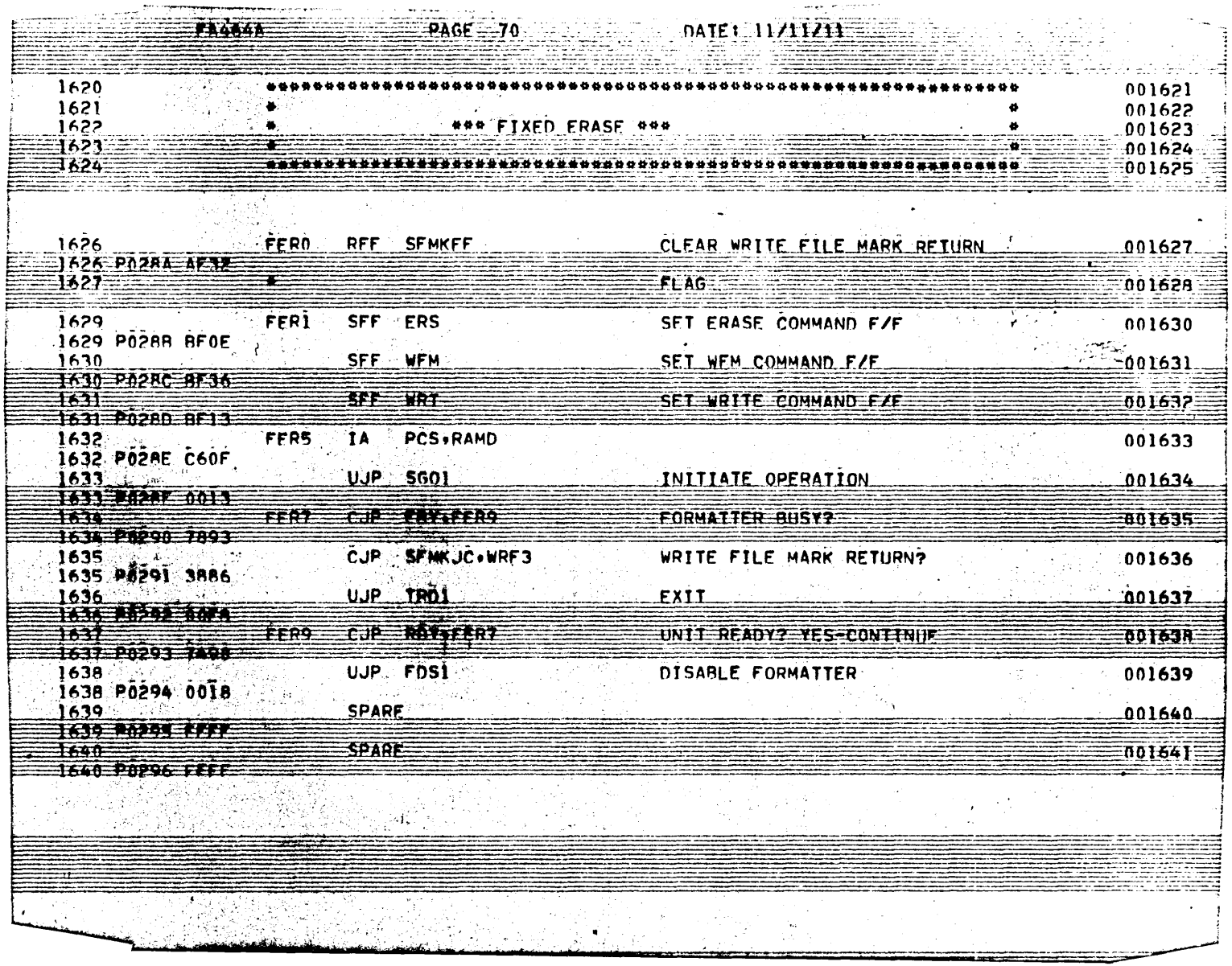
1605               ******************************************************************     001606
1606               *                                                                *     001607
1607               *                *** WRITE FILE MARK ***                         *     001608
1608               *                                                                *     001609
1609               ******************************************************************     001610

1611               WRF1    SFF   SFMKFF                SET WRITE FILE MARK RETURN FLAG    001612
1611 P0284 BF32
1612                       UJP   FER1                  ERASE 6 INCH GAP (FIXED ERASE)     001613
1612 P0285 008B
1613               WRF3    RFF   ERS                   CLEAR ERASE COMMAND F/F            001614
1613 P0286 AF0E
1614                       RFF   SFMKFF                CLEAR WRITE FILE MARK RETURN       001615
1614 P0287 AF32
1615               *                                   FLAG                               001616
1617                       UJP   FERS                  CONTINUE (WRITE FILE MARK)         001618
1617 P0288 008E
1618                       SPARE                                                          001619
1618 P0289 FFFF
```



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1620  ************************************************************************  001621
1621  *                                                                      *  001622
1622  *                  *** FIXED ERASE ***                                 *  001623
1623  *                                                                      *  001624
1624  ************************************************************************  001625


1626          FER0   RFF  SFMKFF                CLEAR WRITE FILE MARK RETURN    001627
1626 P028A AF32
1627          *                                 FLAG                            001628

1629          FER1   SFF  ERS                   SET ERASE COMMAND F/F           001630
1629 P028B BF0E
1630                 SFF  WFM                   SET WFM COMMAND F/F             001631
1630 P028C BF36
1631                 SFF  WRT                   SET WRITE COMMAND F/F           001632
1631 P028D BF13
1632          FER5   IA   PCS*RAMD                                               001633
1632 P028E C60F
1633                 UJP  SG01                  INITIATE OPERATION              001634
1633 P028F 0013
1634          FER7   CJP  FRY*FER9              FORMATTER BUSY?                 001635
1634 P0290 7893
1635                 CJP  SFMKJC*WRF3           WRITE FILE MARK RETURN?         001636
1635 P0291 3886
1636                 UJP  TR01                  EXIT                            001637
1636 P0292 6BF4
1637          FER9   CJP  RDY*FER7              UNIT READY? YES-CONTINUE        001638
1637 P0293 7A88
1638                 UJP  FDS1                  DISABLE FORMATTER               001639
1638 P0294 0018
1639                 SPARE                                                      001640
1639 P0295 FFFF
1640                 SPARE                                                      001641
1640 P0296 FEEF
```

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1642              ************************************************************   001643
1643              *                                                          *   001644
1644              *                   *** READ DATA ***                      *   001645
1645              *                                                          *   001646
1646              ************************************************************   001647

1648              RD1   SFFCL  SELBREG,CDMAER    SELECT READ DATA AS INPUT TO    001649
1648 P0297 BD2D
1649              *                              B REGISTER                      001650
1650                    IA     PCS,RAMD                                          001651
1650 P0298 C60F
1651                    UJP    SG01              INITIATE OPERATION              001652
1651 P0299 0013
1652                    RFFCL  COMP1,CLDSTR      INITIALIZE DMA WRITE F/F'S      001653
1652 P029A A41A
1653                    RFF    SELBF2                                            001654
1653 P029B AF10
1654                    RFF    WTRDMP                                            001655
1654 P029C AF1F
1655                    SFF    LRCRCFF           SET CHECK CHARACTER FLAG 1      001656
1655 P029D BF34
1656                    RFF    INX2FF            CLEAR CHECK CHARACTER FLAG 2    001657
1656 P029E AF06
1657                    IA     PCS,RAMD                                          001658
1657 P029F C60F
1658                    UJP    DBL1              INITIAL BLOCK LENGTH DECREMENT  001659
1658 P02A0 0045
```

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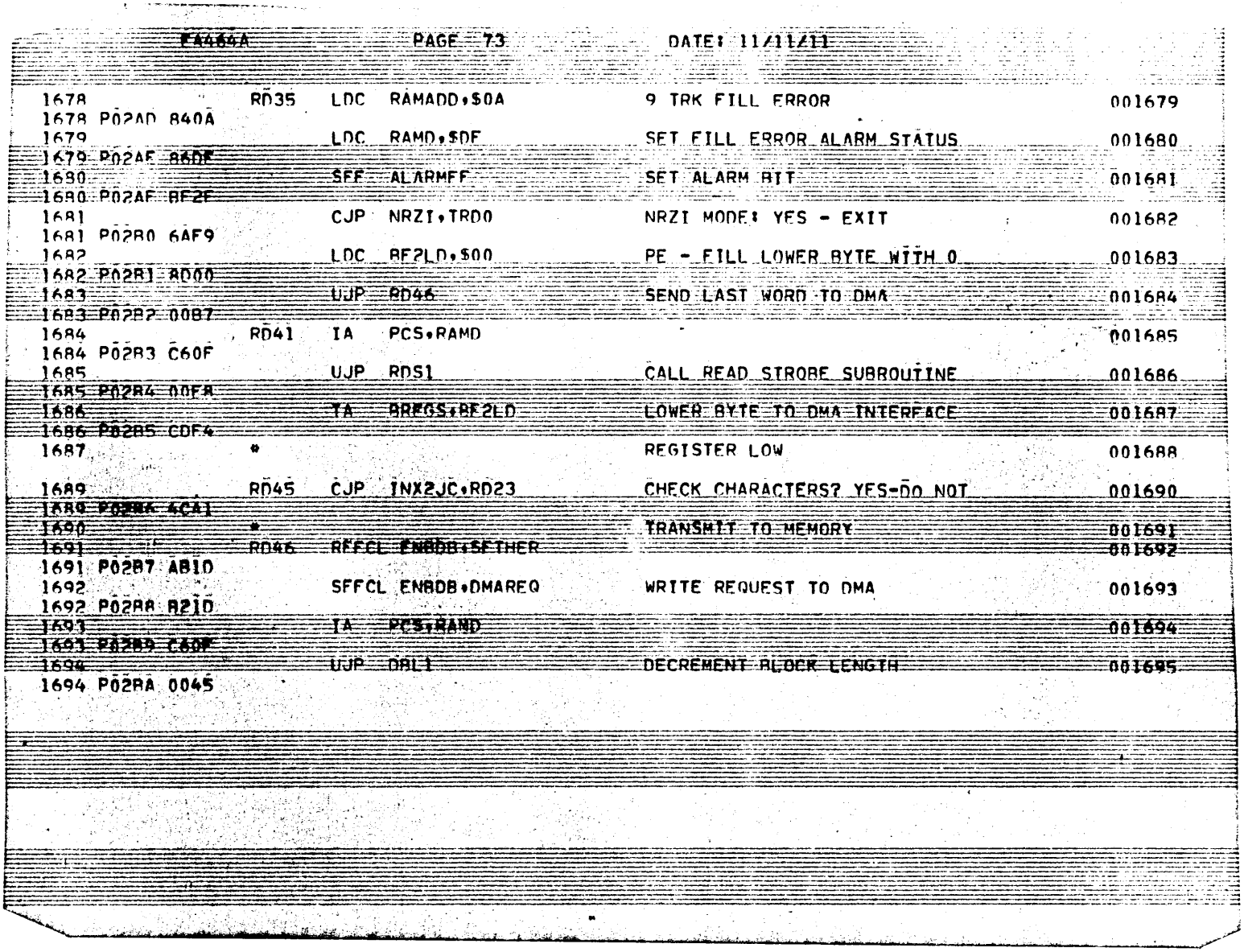
1660            ********** READ UPPER BYTE LOOP **********                001661


1662            RD23  CJP   HEROUT,TFB1          HARD ERROR? YES, EXIT      001663
1662 P02A1 1258
1663                  CJP   RSTRLT,RD27          READ STROBE?               001664
1663 P02A2 52A6
1664                  CJP   FBY,RD97             FORMATTER BUSY? YES-CONTINUE 001665
1664 P02A3 78E4
1665                  CJP   TRK7,RD35            END OF RECORD!? TRK FTLI ERROR 001666
1665 P02A4 72AD
1666                  UJP   TRD0                 9 TRACK NORMAL EXIT        001667
1666 P02A5 00F9
1667            RD27  IA    PCS,RAMD                                        001668
1667 P02A6 C60F
1668                  UJP   RDS1                 CALL READ STROBE SUBROUTINE 001669
1668 P02A7 00E8
1669                  TA    BREGS,BF2UD          UPPER BYTE TO DMA INTERFACE UP 001670
1669 P02A8 CEF4

1671            ********** READ LOWER BYTE LOOP **********                001672


1673            RD32  CJP   HEROUT,TFB1          HARD ERROR ?               001674
1673 P02A9 1258
1674                  CJP   RSTRLT,RD41          READ STROBE ?              001675
1674 P02AA 52B3
1675                  CJP   FBY,RD99             FORMATTER BUSY! YES-CONTINUE 001676
1675 P02AB 78E6
1676                  CJP   TRK7,TRD0            END OF RECORD!? TRK NORMAL EXIT 001677
1676 P02AC 72F9
```



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1678                RD35  LDC  RAMADD,$0A            9 TRK FILL ERROR                    001679
1678 P02AD 840A
1679                      LDC  RAMD,$DF              SET FILL ERROR ALARM STATUS         001680
1679 P02AF 86DF
1680                      SFF  ALARMFF               SET ALARM BIT                       001681
1680 P02AF BF2F
1681                      CJP  NRZI,TRD0             NRZI MODE: YES - EXIT               001682
1681 P02B0 6AF9
1682                      LDC  BF2LD,$00             PE - FILL LOWER BYTE WITH 0         001683
1682 P02B1 8D00
1683                      UJP  RD46                  SEND LAST WORD TO DMA               001684
1683 P02B2 00B7
1684                RD41  IA   PCS,RAMD                                                   001685
1684 P02B3 C60F
1685                      UJP  RDS1                  CALL READ STROBE SUBROUTINE         001686
1685 P02B4 00FA
1686                      TA   BREGS,BF2LD           LOWER BYTE TO DMA INTERFACE         001687
1686 P02B5 CDF4
1687                *                                REGISTER LOW                        001688

1689                RD45  CJP  INX2JC,RD23           CHECK CHARACTERS? YES-DO NOT        001690
1689 P02B6 4CA1
1690                *                                TRANSMIT TO MEMORY                  001691
1691                RD46  RFFCL ENBDB,SETHER                                              001692
1691 P02B7 AB1D
1692                      SFFCL ENBDB,DMAREQ         WRITE REQUEST TO DMA                001693
1692 P02B8 B21D
1693                      IA   PCS,RAMD                                                   001694
1693 P02B9 C60F
1694                      UJP  DBL1                  DECREMENT BLOCK LENGTH              001695
1694 P02BA 0045
```

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1696                * READ NEW UPPER CHAR - WAIT FOR DMA WRITE COMPLETE LOOP *          001697

1698          RD51  CJP  RSTRLT,RD55          NEW UPPER CHAR?                        001699
1698 P02BB 52BF
1699                CJP  DMAWCP,RD79          DMA WRITE COMPLETE                     001700
1699 P02BC 3ED1
1700                CJP  RDY,RD51             UNIT READY;YES-CONTINUE LOOP           001701
1700 P02BD 74BB
1701                UJP  FDS1                 DISABLE FORMATTER; EXIT                001702
1701 P02BE 0018
1702          RD55  IA   PCS,RAMD                                                      001703
1702 P02BF C60F
1703                UJP  RDS1                 CALL READ STROBE SUBROUTINE            001704
1703 P02C0 00E8
1704                IA   RREGS,WCD            BUFFER NEW UPPER CHAR IN WC REG        001705
1704 P02C1 C8F4

1706                * READ NEW LOWER BYTE - WAIT FOR DMA READ COMPLETE LOOP *           001707

1708          RD59  CJP  DMAWCP,RD86          DMA WRITE COMPLETE                     001709
1708 P02C2 3E08
1709          RD60  CJP  RSTRLT,RD63          NEW LOWER BYTE?                        001710
1709 P02C3 52C6
1710                CJP  RDY,RD59             UNIT READY? YES;CONTINUE LOOP          001711
1710 P02C4 74C2
1711                UJP  FDS1                 DISABLE FORMATTER                      001712
1711 P02C5 0018
1712          RD63  IA   PCS,RAMD                                                      001713
1712 P02C6 C60F
1713                UJP  RDS1                 CALL READ STROBE SUBROUTINE            001714
1713 P02C7 00E8
```

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1715                * NEW LOWER BYTE IS BUFFERED IN B REGISTER *                001716
1716                * WAIT FOR DMA WRITE COMPLETE OR LOST DATA *                001717

1718                RD64A  CJP  DMAWCP,RD91          DMA WRITE COMPLETE?        001719
1718 P02C8 3EDD
1719                       SFF  PRIOR                SET DMA PRIORITY           001720
1719 P02C9 BF07
1720                       CJP  RSTRLT,RD71          READ STROBE? YES:LOST DATA 001721
1720 P02CA 52CD
1721                       CJP  RDY,RD64A            UNIT READY? YES: CONTINUE LOOP 001722
1721 P02CB 74CA
1722                       UJP  FDS1                 DISABLE FORMATTER          001723
1722 P02CC 0018
1723                RD71   LDC  RAMADD,$0B                                       001724
1723 P02CD 840B
1724                       LDC  RAMD,$FE             SET LOST DATA ALARM STATUS BIT 001725
1724 P02CE A6FE
1725                RD73   SFFCL ALARMFF,CLHER       SET ALARM BIT              001726
1725 P02CF 8A2F
1726                       UJP  TFB1                 EXIT                       001727
1726 P02D0 0850
1727                RD79   CJP  PARERR,DTE0          CHECK PARITY ERROR         001728
1727 P02D1 0A2F
1728                       CJP  ADRERR,DTE0          CHECK ADDRESS ERROR        001729
1728 P02D2 062F
1729                       CJP  PRTFLT,DTE0          CHECK PROTECT FAULT        001730
1729 P02D3 162F
1730                       UJP  RD23                 NO ERRORS: GO TO READ UPPER 001731
1730 P02D4 00A1
1731                       SPARE                                                001732
1731 P02D5 FFFF
1732                       SPARE                                                001733
1732 P02D6 FFFF
1733                       SPARE                                                001734
1733 P02D7 FFFF
```

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1735                RD86    CJP   PARERR,DTE0          CHECK PARITY ERROR                  001736
1735 P02D8 0A2F
1736                        CJP   ADRERR,DTE0          CHECK ADDRESS ERROR                 001737
1736 P02D9 062F
1737                        CJP   PRTFLT,DTE0          CHECK PROTECT FAULT                 001738
1737 P02DA 162F
1738                        TA    WCS,BF2UD            MOVE BUFFERED UPPER BYTE TO DMA     001739
1738 P02DB CEF1
1739                *                                  INTERFACE UP                        001740

1741                        UJP   RD32                 GO TO READ LOWER BYTE LOOP          001742
1741 P02DC 00A9
1742                RD91    CJP   PARERR,DTE0          CHECK PARITY ERROR                  001743
1742 P02DD 0A2F
1743                        CJP   ADRERR,DTE0          CHECK ADDRESS ERROR                 001744
1743 P02DE 062F
1744                        CJP   PRTFLT,DTE0          CHECK PROTECT FAULT                 001745
1744 P02DF 162F
1745                        TA    WCS,BF2UD            MOVE BUFFERED UPPER BYTE TO DMA     001746
1745 P02E0 CEF1
1746                *                                  INTERFACE REGISTER UPPER            001747

1748                        TA    BREGS,BF2LD          MOVE BUFFERED LOWER BYTE TO DMA     001749
1748 P02E1 C0F4
1749                *                                  INTERFACE LOWER                     001750

1751                        RFF   PRIOR                CLEAR PRIORITY                      001752
1751 P02E2 8F07
1752                        UJP   RD45                 GO TO SEND NEW DMA REQUEST          001753
1752 P02E3 0086
1753                RD97    CJP   RDY,RD23             UNIT READY? YES;CONTINUE LOOP       001754
1753 P02E4 74A1
1754                        UJP   FDS1                 DISABLE FORMATTER                   001755
1754 P02E5 0018
1755                RD95    CJP   RDY,RD32             UNIT READY? YES; CONTINUE LOOP      001756
1755 P02E6 74A9
1756                        UJP   FDS1                 DISABLE FOMATTER                    001757
1756 P02E7 0018
```

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1758  ********************************************************************** 001759
1759  *                                                                    * 001760
1760  *                *** READ STROBE SUBROUTINE ***                     * 001761
1761  *                                                                    * 001762
1762  ********************************************************************** 001763


1764        RDS1  CA   RAMS,BREGD          STROBE DATA INTO B.REGISTER      001765
1764 P02E8 CF06
1765              SFFCL ACK,CLDSTR         ACKNOWLEDGE READ STROBE          001766
1765 P02E9 B411
1766              CJP  IDENT,RDS7A         CRC OR LR  CHECK CHARACTERS?     001767
1766 P02EA 7EF1
1767              CJP  RP,RDS16            PARITY BIT HIGH?                 001768
1767 P02EB 23D0


1769        * PARITY BIT LOW *                                               001770

1771              IA   BREGS,NU1           GENERATE PARITY BIT              001772
1771 P02EC C0F4
1772        *                                                               001773
1773              CJP  PARLT,RDS18         GENERATED PARITY HIGH? YES -     001774
1773 P02ED 69D2
1774        *                              TRANSMISSION PARITY ERROR        001775
1775        RDS5  RFF  ACK                                                  001776
1775 P02EE AF11
1776        RDS6  LDC  RAMADD,$00                                           001777
1776 P02EF 8400
1777              IA   RAMS,PCD            NORMAL SUBRT RETURN              001778
1777 P02F0 C708
1778        RDS7A LDC  RAMADD,$0D          LOAD ADDRESS OF CRC STATUS       001779
1778 P02F1 840D
1779              CJP  TRK7,RDS10          TRK7 YES - LOAD LRC STATUS       001780
1779 P02F2 72F5
1780              CJP  LRCRCJC,RDS11       CRC INDEX HIGH: NO - LRC CHAR    001781
1780 P02F3 24F6
```

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1782                        SFF   INX2FF          SET   INDEX TO PREVENT          001783
1782 P02F4 BF06
1783                  *                           TRANSMISSION TO DMA             001784

1785                  *                           CHECK CHARACTERS                001786

1787                  RDS10 LDC   RAMADD,$0C      LOAD LRC STATUS ADDRESS         001788
1787 P02F5 840C
1788                  RDS11 CA    BREGS,RAMD      LOAD LRC/CRC STATUS TO FILE     001789
1788 P02F6 C604
1789                        RFF   LRCRCFF         CLEAR INDEX FOR CRC STATUS      001790
1789 P02F7 AF34
1790                        UJP   RDS5            CONTINUE                        001791
1790 P02F8 00EE

1792                  * READ PARITY BIT HIGH *                                    001793

1794        03D0 P          ORG   START1+$3D0                                     001795
1795                  RDS16 TA    BREGS,NU1       GENERATE PARITY                 001796
1795 P03D0 C0F4
1796                        CJP   PARLT,RDS5      GEENRATED BIT HIGH? YES-        001797
1796 P03D1 68EE
1797                  *                           CONTINUE                        001798

1799                  RDS18 LDC   RAMADD,$0B      TRANSMISSION PARITY ERROR       001800
1799 P03D2 840B
1800                        LDC   RAMD,$EF        SET TRANSMISSION PARITY ERROR   001801
1800 P03D3 86EF
1801                        SFF   ALARMFF         SET ALARM                       001802
1801 P03D4 BF2F
1802                        RFF   ACK                                             001803
1802 P03D5 AF11
1803                        CJP   OFLMTJC,RDS6    OFF LINE MAINTENANCE? YES -     001804
1803 P03D6 10EF
1804                  *                           RETURN                          001805

1806                        UJP   TFR1            EXIT                            001807
1806 P03D7 0050
```

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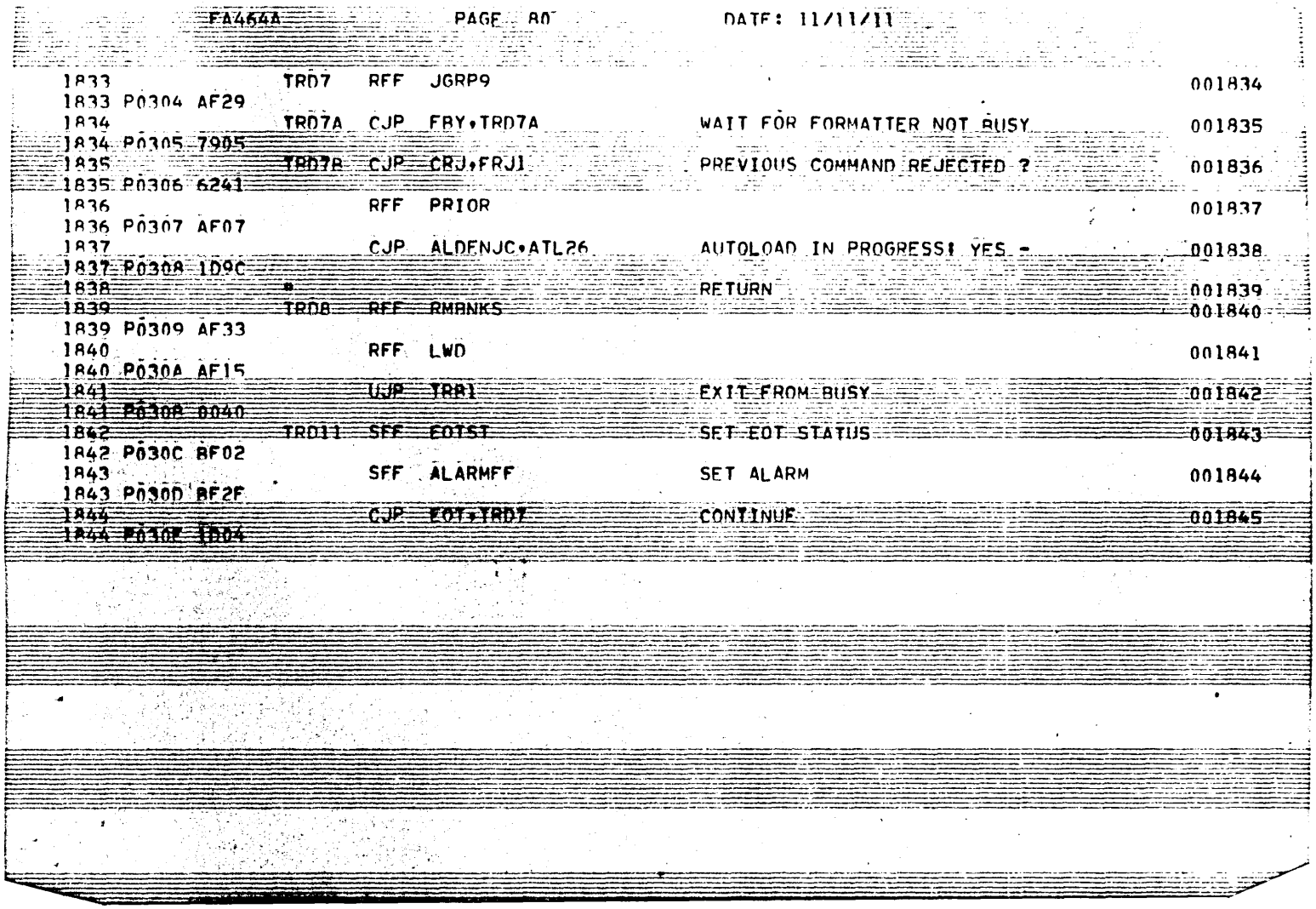
1808          ********************************************************************      001809
1809          *                                                                  *      001810
1810          *    *** TERMINATE READ AND DIRECTOR FUNCTION ROUTINE ***          *      001811
1811          *                                                                  *      001812
1812          ********************************************************************      001813


1814    02F9 P        ORG  START1+$2F9                                              001815
1815          TRD0    RFFCL SELBF2+CREQ          ENABLE ALU BUS INPUT TO BUFFER     001816
1815 P02F9 A510
1816          *                                  2 REGISTER                         001817

1818                  RFF  SELBREG               ENABLE ALU BUS INPUT TO B REG.     001819
1818 P02FA AF20
1819          TRD1    CJP  FMK+TRD3              FILE MARK DETECTED?                001820
1819 P02FB 60FD
1820                  UJP  TRD3A                 CONTINUE                           001821
1820 P02FC 00FE
1821          TRD3    SFFCL FMKST+CLHER          SET FILE MARK STATUS               001822
1821 P02FD BA04
1822          TRD3A   CJP  HEROUT+ESA1           HARD ERROR? YES - ASSEMBLE         001823
1822 P02FE 121F
1823          *                                  HARD ERROR STATUS                  001824

1825          TRD4    SFF  JGRP9                 SET JUMP CONDITION GROUP 9         001826
1825 P02FF BF29
1826          *                                  ENABLE                             001827

1828                  CJP  EOT+TRD11             END OF TAPE MARKER DETECTED?       001829
1828 P0300 100C
1829                  SFF  CERST                 SET CER STATUS                     001830
1829 P0301 BF30
1830                  CJP  CER+TRD2              CORRECTED ERROR DETECTED           001831
1830 P0302 190A
1831                  RFF  CERST                 NOT RESET CER STATUS               001832
1831 P0303 AF30
```



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          FA464A          -          PAGE  80          DATE: 11/11/11

1833                TRD7    RFF   JGRP9                                          001834
1833 P0304 AF29
1834                TRD7A   CJP   FBY,TRD7A      WAIT FOR FORMATTER NOT BUSY     001835
1834 P0305 7905
1835                TRD7B   CJP   CRJ,FRJ1       PREVIOUS COMMAND REJECTED ?     001836
1835 P0306 6241
1836                        RFF   PRIOR                                          001837
1836 P0307 AF07
1837                        CJP   ALDENJC,ATL26   AUTOLOAD IN PROGRESS! YES -     001838
1837 P0308 1D9C
1838                *                             RETURN                         001839
1839                TRD8    RFF   RMBNKS                                        001840
1839 P0309 AF33
1840                        RFF   LWD                                            001841
1840 P030A AF15
1841                        UJP   YRR1            EXIT FROM BUSY                 001842
1841 P030B 0040
1842                TRD11   SFF   EOTST          SET EOT STATUS                 001843
1842 P030C BF02
1843                        SFF   ALARMFF         SET ALARM                      001844
1843 P030D BF2F
1844                        CJP   EOT,YRD7        CONTINUE                       001845
1844 P030E 1D04
```

```
1846                 ********************************************************************** 001847
1847                 *                                                                    * 001848
1848                 *                 *** WRITE STROBE SUBROUTINE ***                    * 001849
1849                 *                                                                    * 001850
1850                 ********************************************************************** 001851


1852       0338 P          ORG   START1+$338                                               001853
1853                 WSR1  CJP   HEROUT,WSR5A      HARD ERROR?                           001854
1853 P0338 133D
1854                       CJP   WSTRLT,WSR9       WRITE STROBE? YES - ACKNOWLEDGE       001855
1854 P0339 4840
1855                       CJP   BF2F,WSR14        DMA READ COMPLETE?                    001856
1855 P033A 0F46
1856                       CJP   RDY,WSR22         UNIT READY? YES - CONTINUE LOOP       001857
1856 P033B 754C
1857                       UJP   FDS1              DISABLE FORMATTER                     001858
1857 P033C 0018
1858                 WSR5A CJP   OFLMTJC,WSR9      DO NOT EXIT FOR OFF LINE MAINT.       001859
1858 P033D 1140
1859                       SFF   LWD               TERMINATE WRITE DUE TO ERROR          001860
1859 P033E BF15
1860                       UJP   TFB1              EXIT                                  001861
1860 P033F 0050
1861                 WSR9  SFFCL ACK,CLDSTR        ACKNOWLEDGE WRITE STROBE              001862
1861 P0340 B411
1862                       CJP   OFLMTJC,WSR12                                           001863
1862 P0341 1143
1863                       CJP   TPER,WSR26        TRANSMISSION PARITY ERROR?            001864
1863 P0342 654E
1864                 WSR12 RFF   ACK                                                     001865
1864 P0343 AF11
1865                 WSR12A CJP  WSTRLN,WSR12A     WAIT FOR TRAILING EDGE OF WSTR        001866
1865 P0344 0544
1866                       IA    RAMS,PCD          RETURN PLUS 1                         001867
1866 P0345 C708
1867                 WSR14 CJP   PARERR,DTE0       CHECK DMA ERRORS                      001868
1867 P0346 0A2F
1868                       CJP   ADRERR,DTE0                                             001869
1868 P0347 062F
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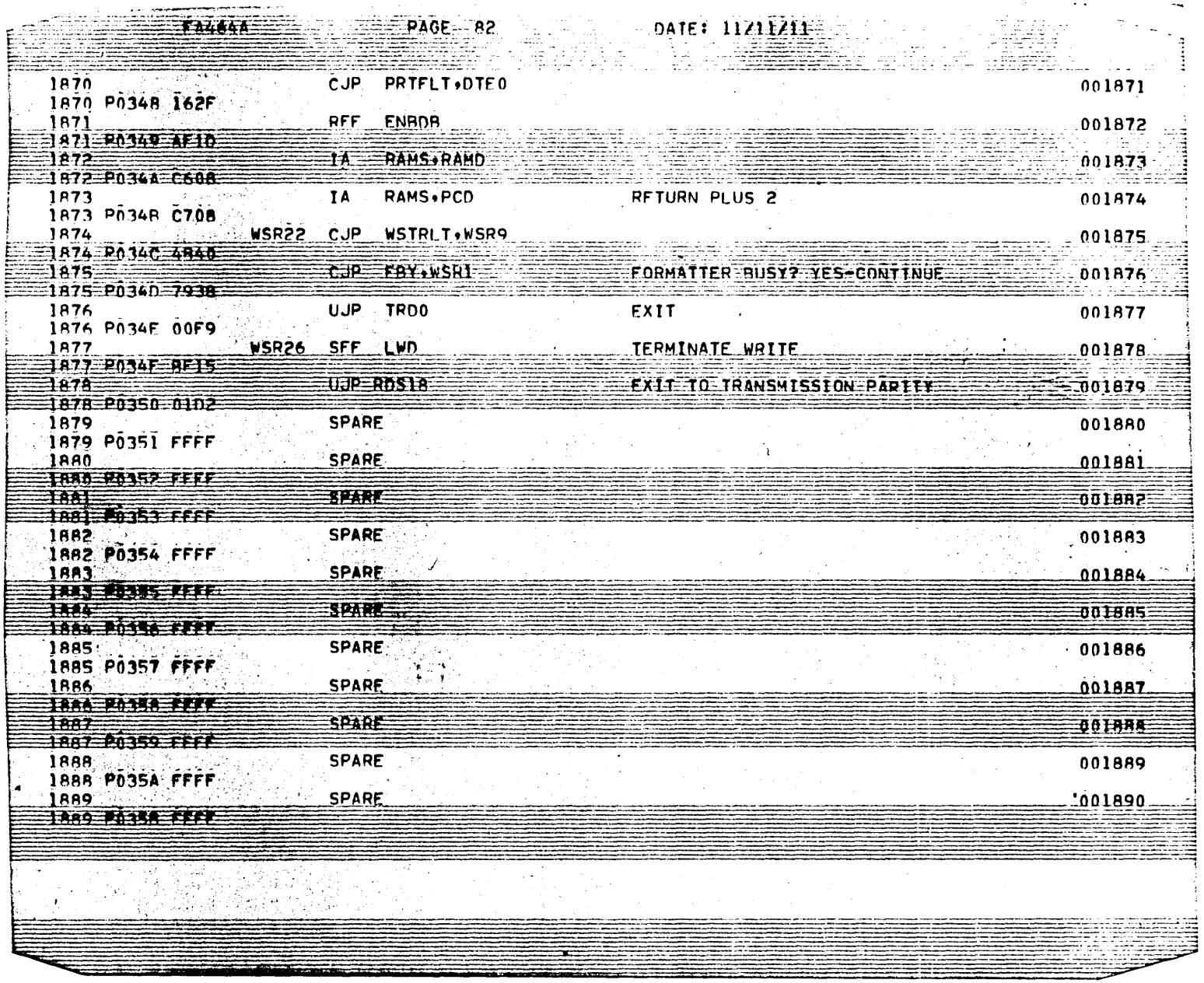

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1870                      CJP   PRTFLT,DTE0                                  001871
1870 P0348 162F
1871                      RFF   ENRDR                                        001872
1871 P0349 AF1D
1872                      IA    RAMS,RAMD                                    001873
1872 P034A C608
1873                      IA    RAMS,PCD          RETURN PLUS 2              001874
1873 P034B C708
1874                WSR22 CJP   WSTRLT,WSR9                                  001875
1874 P034C 4848
1875                      CJP   FBY,WSR1          FORMATTER BUSY? YES-CONTINUE 001876
1875 P034D 7938
1876                      UJP   TRD0              EXIT                       001877
1876 P034E 00F9
1877                WSR26 SFF   LWD               TERMINATE WRITE            001878
1877 P034F AF15
1878                      UJP   RDS18             EXIT TO TRANSMISSION PARITY 001879
1878 P0350 0102
1879                      SPARE                                              001880
1879 P0351 FFFF
1880                      SPARE                                              001881
1880 P0352 FFFF
1881                      SPARE                                              001882
1881 P0353 FFFF
1882                      SPARE                                              001883
1882 P0354 FFFF
1883                      SPARE                                              001884
1883 P0355 FFFF
1884                      SPARE                                              001885
1884 P0356 FFFF
1885                      SPARE                                              001886
1885 P0357 FFFF
1886                      SPARE                                              001887
1886 P0358 FFFF
1887                      SPARE                                              001888
1887 P0359 FFFF
1888                      SPARE                                              001889
1888 P035A FFFF
1889                      SPARE                                              001890
1889 P035B FFFF
```

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1891              ******************************************************************   001892
1892              *                                                                *   001893
1893              *                      *** WRITE DATA ***                        *   001894
1894              *                                                                *   001895
1895              ******************************************************************   001896

1897        03DB P         ORG   START1+$3DB                                           001898
1898              WT1      SFF   WRT            SET WRITE COMMAND F/F                  001899
1898 P03DB BF13
1899                       LDC   RAMADD,$02                                            001900
1899 P03DC 8402
1900                       LDC   RAMD,$3F       LOAD MASK FOR 7 TRACK                  001901
1900 P03DD 863F
1901                       CJP   TRK7,WT6       7 TRACK? YES=CONTINUE                  001902
1901 P03DE 73E0
1902                       LDC   RAMD,$FF       LOAD MASK FOR 9 TRACK                  001903
1902 P03DF 86FF
1903              WT6      SFFCL WTRDMP,CDMAER  INITIALIZE DMA READ F/F'S              001904
1903 P03E0 BD1F
1904                       SFFCL COMP1,CLDSTR                                          001905
1904 P03E1 841A
1905                       RFF    ENBDB                                                001906
1905 P03E2 AF1D
1906                       SFF    SELBF1                                               001907
1906 P03E3 BF17
1907                       SFF    SELBF2                                               001908
1907 P03E4 BF18
1908                       RFF    RWMOD                                                001909
1908 P03E5 AF19
1909                       IA     PCS,RAMD                                             001910
1909 P03E6 C60F
1910                       UJP   DBL1           INITIAL BLOCK LENGTH DECREMENT         001911
1910 P03E7 8045
1911                       IA    PCS,RAMD                                              001912
1911 P03E8 C60F
```

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1913                        UJP   SG01          INITIATE OPERATION                001914
1913 P03E9 0013
1914                        CJP   PARJC,WT16B   INITIALIZE WRITE PARITY BIT IN     001915
1914 P03EA 350F
1915                        UJP   WT17                                             001916
1915 P03EB 0110
1916       030F P           ORG   START1+$30F                                      001917
1917             WT16B      RFF   WP                                              001918
1917 P030F AF1C
1918                 WT17   SFFCL FNRDR,DMAREQ     DMA READ REQUEST              001919
1918 P0310 B210
1919                 WT22   SFF   PRIOR           SET PRIORITY                  001920
1919 P0311 BF07
1920                        IA    PCS,RAMD                                        001921
1920 P0312 C60F
1921                        UJP   WSR1            CALL WRITE STROBE SUBROUTINE  001922
1921 P0313 0138
1922                 *                           WSTR BEFORE DMA DATA          001923

1924                        UJP   WT58            LOST DATA                     001925
1924 P0314 0136
1925                        RFF   PRIOR           DMA READ COMPLETE             001926
1925 P0315 AF07
1926                 WT24   LDC   RAMADD,$02                                     001927
1926 P0316 8402
1927                        ANDAB RAMS,BF2US,WCD  MASKED UPPER BYTE TO OUTPUT   001928
1927 P0317 F880
1928                 *                           REGISTER                      001929

1930                        SFF   WP              GENERATE PARITY BIT           001931
1930 P0318 BF1C
1931                        CJP   PARLT,WT28A                                    001932
1931 P0319 691B
1932                        RFF   WP                                            001933
1932 P031A AF1C
1933                 *                           DMA DATA TOO LATE             001934
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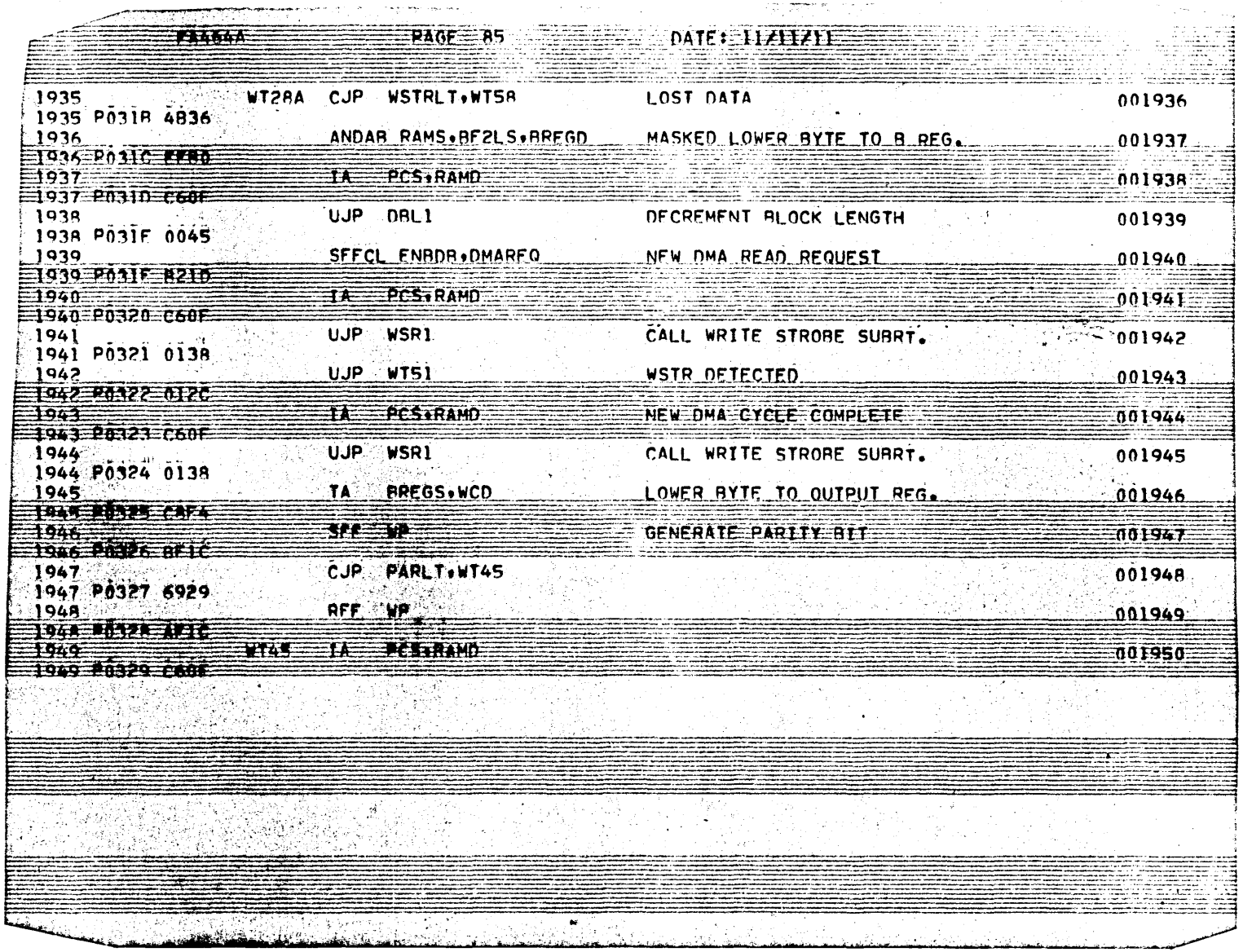

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P3464A          PAGE 85          DATE: 11/11/11

1935            WT28A  CJP  WSTRLT,WT58          LOST DATA                          001936
1935 P031B 4836
1936                   ANDAB RAMS,BF2LS,BREGD     MASKED LOWER BYTE TO B REG.        001937
1936 P031C FF80
1937                   IA   PCS,RAMD                                                 001938
1937 P031D C60F
1938                   UJP  DBL1                  DECREMENT BLOCK LENGTH             001939
1938 P031E 0045
1939                   SFFCL ENBDR,DMAREQ         NEW DMA READ REQUEST               001940
1939 P031F B21D
1940                   IA   PCS,RAMD                                                 001941
1940 P0320 C60F
1941                   UJP  WSR1                  CALL WRITE STROBE SUBRT.           001942
1941 P0321 0138
1942                   UJP  WT51                  WSTR DETECTED                      001943
1942 P0322 012C
1943                   IA   PCS,RAMD              NEW DMA CYCLE COMPLETE             001944
1943 P0323 C60F
1944                   UJP  WSR1                  CALL WRITE STROBE SUBRT.           001945
1944 P0324 0138
1945                   TA   BREGS,WCD             LOWER BYTE TO OUTPUT REG.          001946
1945 P0325 CAF4
1946                   SFF  WP                    GENERATE PARITY BIT                001947
1946 P0326 BF1C
1947                   CJP  PARLT,WT45                                               001948
1947 P0327 6929
1948                   RFF  WP                                                       001949
1948 P0328 AF1C
1949            WT45   IA   PCS,RAMD                                                 001950
1949 P0329 C60F
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1951                      UJP   WSR1        CALL WRITE STROBE SUBRT.          001952
1951 P032A 0138
1952                      UJP   WT24        BOTH BYTES SENT - CONTINUE        001953
1952 P032B 0116
1953                WT51  TA    BREGS,WCD   LOWER BYTE TO OUTPUT REG.         001954
1953 P032C C8F4
1954                      SFF   WP          GENERATE PARITY BIT               001955
1954 P032D BF1C
1955                      CJP   PARLT,WT52                                    001956
1955 P032E 6930
1956                      RFF   WP                                            001957
1956 P032F AF1C
1957                WT52  IA    PCS,RAMD                                      001958
1957 P0330 C60F
1958                      UJP   WSR1        CALL WRITE STROBE SUBRT.          001959
1958 P0331 0138
1959                      UJP   WT22        RETURN FOR WSTR - NO BYTES IN     001960
1959 P0332 0111
1960                *                       BUFFERS                           001961

1962                      IA    PCS,RAMD    DMA READ COMPLETE                 001963
1962 P0333 C60F
1963                      UJP   WSR1        CALL WRITE STROBE SUBRT           001964
1963 P0334 0138
1964                      UJP   WT24        CONTINUE                          001965
1964 P0335 0116
1965                WT58  SFF   LWD         TERMINATE WRITE FOR LOST DATA     001966
1965 P0336 BF1B
1966                      UJP   RD71        EXIT                              001967
1966 P0337 00CD
```

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1968               ******************************************************************   001969
1969               *                                                                *   001970
1970               *                 *** TERMINATE WRITE ROUTINE ***                *   001971
1971               *                                                                *   001972
1972               ******************************************************************   001973

1974       03EC P           ORG  START1+$3EC                                           001975
1975               TWT0     SFF  LWD                ENTRY FOR WRITE ODD                001976
1975 P03EC BF15
1976               TWT1     IA   PCS,RAMD           ENTRY FOR NORMAL WRTIE             001977
1976 P03ED C60F
1977                        UJP  WSR1               CALL WRITE STROBE SUBRT TO MOVE    001978
1977 P03EF 0138
1978               *                                OUT UPPER BYTE OF LAST WORD        001979

1980                        SFF  LWD                LAST BYTE TO BE SENT               001981
1980 P03EF BF15
1981                        SFF  LWD                                                   001982
1981 P03F0 BF15
1982                        IA   RRE05,WCD          LAST BYTE TO OUTPUT REG.           001983
1982 P03F1 C8F4
1983                        SFF  WP                 GENERATE PARITY                    001984
1983 P03F2 BF1C
1984                        CJP  PARLT,TWT9                                            001985
1984 P03F3 69F5
1985                        RFF  WP                                                    001986
1985 P03F4 AF1C
1986               TWT9     IA   PCS,RAMD                                              001987
1986 P03F5 C60F
1987                        UJP WSR1                CALL WRITE STROBE SUBRT.           001988
1987 P03F6 0138
1988                        UJP  TFR1               EXIT                               001989
1988 P03F7 0050
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6047601 0A

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1990            *************************************************************            001991
1991            *                                                           *            001992
1992            *              *** ASSEMBLE/SENSE NEXT READY ***            *            001993
1993            *                                                           *            001994
1994            *************************************************************            001995

1996       035C P      ORG  START1+$35C                                                  001997
1997            ASR1   LDC  RAMADD,$01                                                   001998
1997 P035C 8401
1998                   TA   AINLS,RAMD                SAVE INITIAL READY STATUS          001999
1998 P035D C6F2
1999                   RFF  SLCTDFF                                                      002000
1999 P035F AF05
2000                   CA   AINUS,BREGD                                                  002001
2000 P035F CF03
2001                   SFF  SFMKFF                    SET ASSEMBLE INDEX                 002002
2001 P0360 BF32
2002                   CJP  BMSB,ASR10                ASSEMBLE OR SENSE?                 002003
2002 P0361 5163
2003                   RFF  SFMKFF                    SENSE - CLEAR ASSEMBLE INDEX       002004
2003 P0362 AF32
2004            ASR10  SFF  BUSY                      ENTER BUSY                         002005
2004 P0363 BF2E
2005                   RFFCL EOP,RPLY                                                    002006
2005 P0364 A303
2006            ASR12  RFF  CNALU                     INITIALIZE ASSEMBLY OF READY       002007
2006 P0365 AF20
2007            *                                     STATUS                             002008
2008                   LDC  BF2LD,$FF                                                    002009
2008 P0366 8DFF
2009                   LDC  BREGD,$FE                                                    002010
2009 P0367 8FFE
2010                   SFF  FEN                                                          002011
2010 P0368 BF12
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2012                    RFF  TAD0                                        002013
2012 P0369 AF21
2013                    RFF  TAD1          SELECT UNIT 0                002014
2013 P036A AF26
2014                    IA   PCS,RAMD                                   002015
2014 P036B C60F
2015                    UJP  SNS1          CALL SENSE SUBROUTINE        002016
2015 P036C 0182
2016                    SFF  TAD1          SELECT UNIT 1                002017
2016 P036D AF26
2017                    IA   PCS,RAMD                                   002018
2017 P036E C60F
2018                    UJP  SNS1          CALL SENSE SUBROUTINE        002019
2018 P036F 0182
2019                    RFF  TAD1                                       002020
2019 P0370 AF26
2020                    SFF  TAD0          SELECT UNIT 2                002021
2020 P0371 AF21
2021                    IA   PCS,RAMD                                   002022
2021 P0372 C60F
2022                    UJP  SNS1          CALL SENSE SUBROUTINE        002023
2022 P0373 0182
2023                    SFF  TAD1          SELECT UNIT 3                002024
2023 P0374 AF26
2024                    IA   PCS,RAMD                                   002025
2024 P0375 C60F
2025                    UJP  SNS1          CALL SENSE SUBROUTINE        002026
2025 P0376 0182
2026                    CJP  ALDENJC,ATL27 RETURN FOR AUTOLOAD          002027
2026 P0377 1D90
2027                    CJP  OFLMTJC,OLM37 RETURN FOR OFF LINE MAINT.   002028
2027 P0378 11C8
2028                    NOOP                                            002029
2028 P0379 8FFF
```

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        FA464A              PAGE  90              DATE: 11/11/11

2030                    LDC   RAMADD,$0F                                  002031
2030 P037A 840E
2031                    TR    BF2LS,RAMD        SAVE ASSEMBLED READY STATUS  002032
2031 P037B F6A0
2032                    CJP   SFMKJC,TRD8       ASSEMBLE? YES-EXIT           002033
2032 P037C 3909
2033                    LDC   RAMADD,$01        SENSE READY CHANGE           002034
2033 P037D 8401
2034                    SFF   CNALU                                          002035
2034 P037E BF20
2035                    COMPR RAMS,BF2LS        COMPARE ORIGINAL AND ASSEMBLED 002036
2035 P037F F368
2036              *                             READY STATUS                 002037

2038                    CJP   EQUAL,ASR12       IF EQUAL,CONTINUE SAMPLING   002039
2038 P0380 1F65
2039                    UJP   TRD8              CHANGE DETECTED, EXIT        002040
2039 P0381 0109


2041              ***************************************************       002042
2042              *                                                 *       002043
2043              *          *** SENSE SUBROUTINE ***               *       002044
2044              *                                                 *       002045
2045              ***************************************************       002046


2047              SNS1  CJP   RDY,SNS3          UNIT READY                   002048
2047 P0382 7584
2048                    UJP   SNS5              UNIT NOT READY               002049
2048 P0383 0188
2049              SNS3  CJP   ALDENJC,ATL1      AUTOLOAD? YES-RETURN         002050
2049 P0384 1D8C
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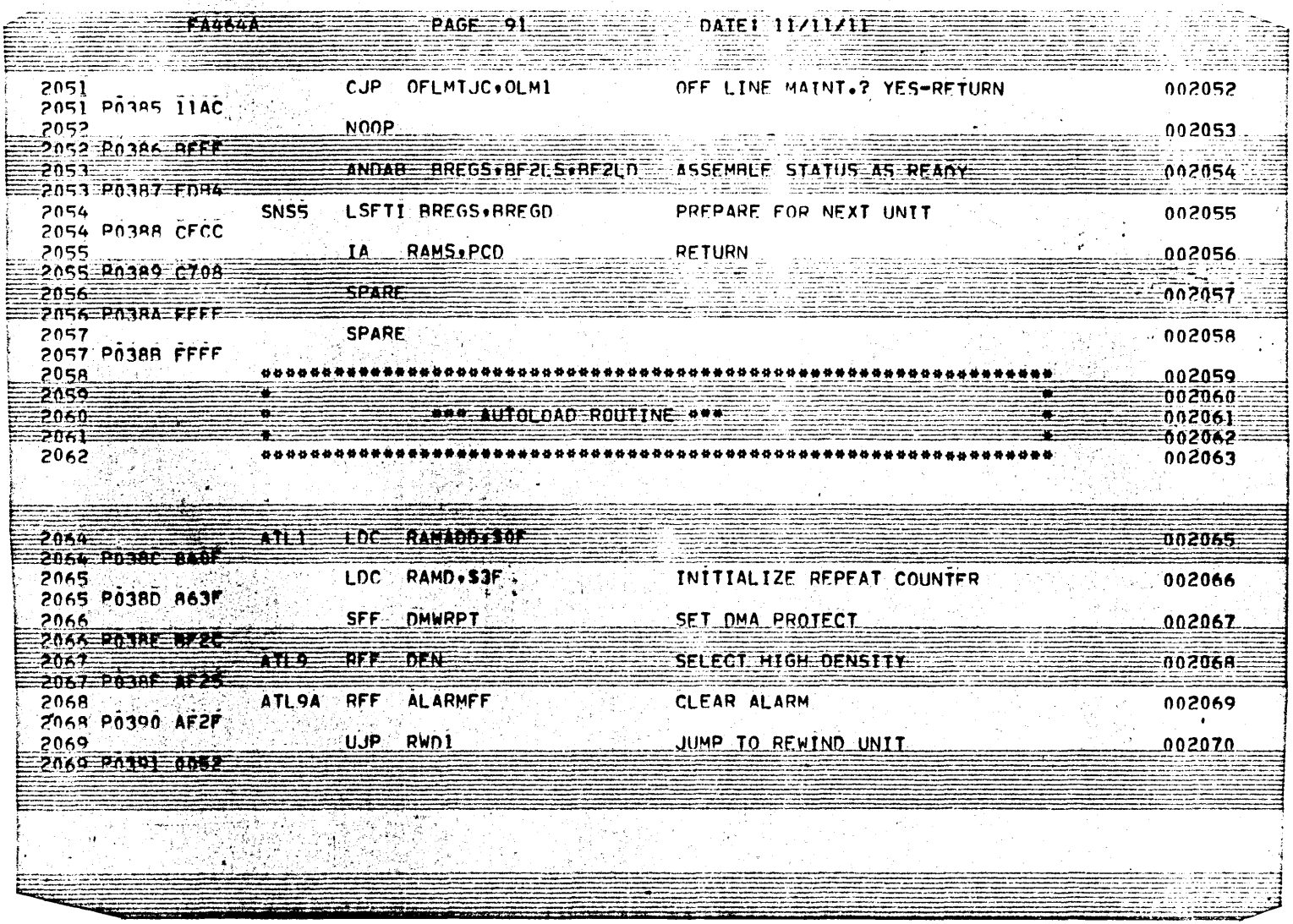

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2051                      CJP   OFLMTJC,OLM1         OFF LINE MAINT.? YES-RETURN          002052
2051 P0385 11AC
2052                      NOOP                                                            002053
2052 P0386 BFFF
2053                      ANDAB  BREGS,BF2LS,BF2LD   ASSEMBLE STATUS AS READY             002054
2053 P0387 FDB4
2054                SNS5  LSFTI BREGS,BREGD          PREPARE FOR NEXT UNIT                002055
2054 P0388 CFCC
2055                      IA    RAMS,PCD             RETURN                               002056
2055 P0389 C708
2056                      SPARE                                                           002057
2056 P038A FFFF
2057                      SPARE                                                           002058
2057 P038B FFFF
2058                ********************************************************************* 002059
2059                *                                                                   * 002060
2060                *              *** AUTOLOAD ROUTINE ***                             * 002061
2061                *                                                                   * 002062
2062                ********************************************************************* 002063


2064                ATL1  LDC   RAMADD,$0F                                                002065
2064 P038C 860F
2065                      LDC   RAMD,$3F             INITIALIZE REPEAT COUNTER            002066
2065 P038D 863F
2066                      SFF   DMWRPT               SET DMA PROTECT                      002067
2066 P038E BF2C
2067                ATL9  RFF   DEN                  SELECT HIGH DENSITY                  002068
2067 P038F AF25
2068                ATL9A RFF   ALARMFF              CLEAR ALARM                          002069
2068 P0390 AF2F
2069                      UJP   RWD1                 JUMP TO REWIND UNIT                  002070
2069 P0391 8052
```

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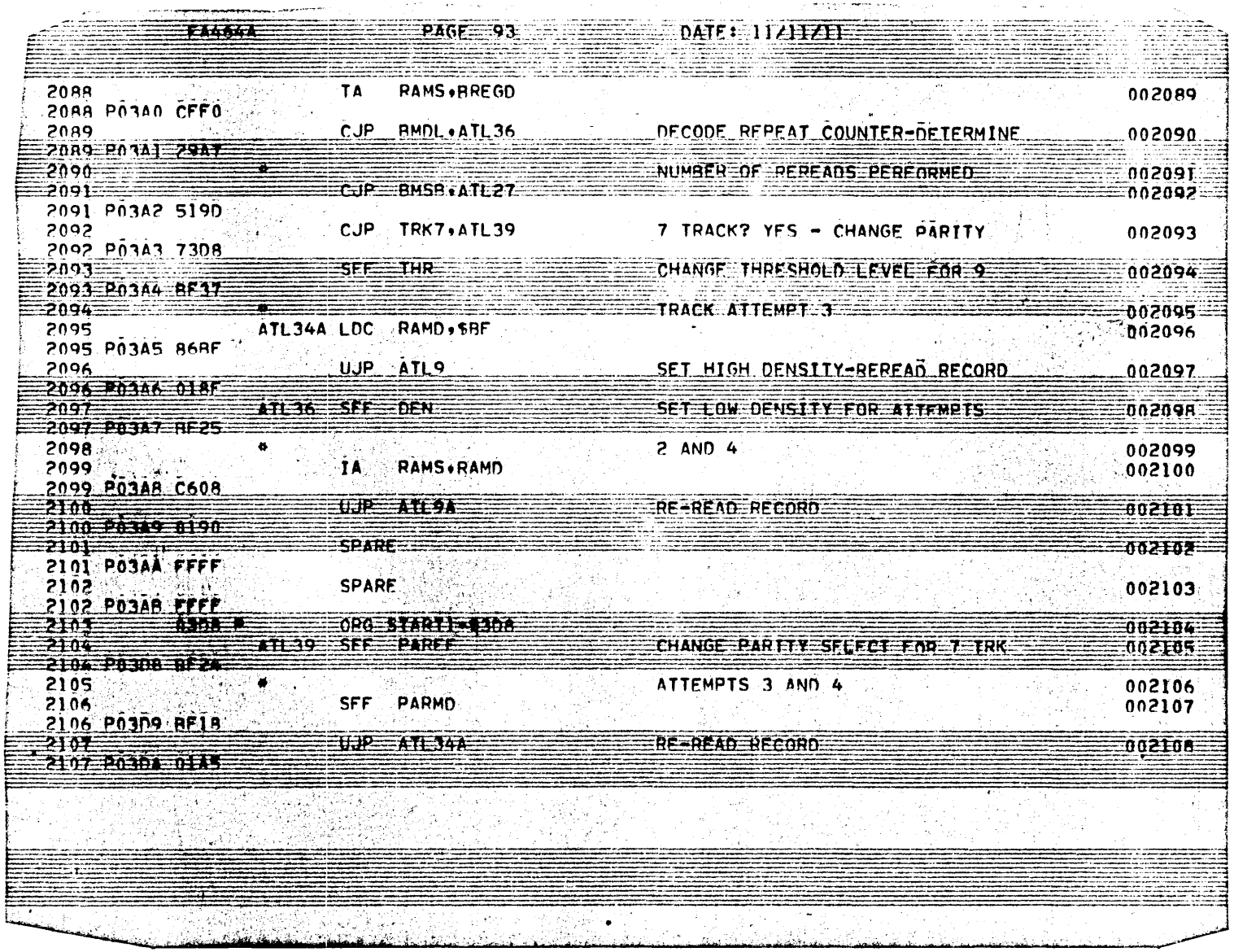
2071                ATL13  CJP  RDY,ATL18            REWIND COMPLETE? YES-CONTINUE          002072
2071 P0392 7594
2072                       UJP  ATL13                WAIT FOR END OF REWIND                 002073
2072 P0393 0192
2073                ATL18  LDC  CWALD,$00            INITIALIZE MEMORY ADDRESS,BANK         002074
2073 P0394 8A00
2074                *                                AND BLOCK LENGTH                       002075

2076                       LDC  CWAUD,$00            INITIAL MEMORY ADDRESS 0               002077
2076 P0395 8B00
2077                       LDC  BANKD,$00            INITIAL MEMORY BANK 0                  002078
2077 P0396 8500
2078                       LDC  RAMADD,$08                                                  002079
2078 P0397 8408
2079                       LDC  RAMD,$00                                                    002080
2079 P0398 8600
2080                       LDC  RAMADD,$09                                                  002081
2080 P0399 8409
2081                       LDC  RAMD,$00             LOAD MAXIMUM BLOCK LENGTH              002082
2081 P039A 8600
2082                       UJP  RD1                  JUMP TO READ FIRST RECORD              002083
2082 P039B 8097
2083                ATL26  CJP  ALARMJC,ATL29        ALARM DURING READ?                     002084
2083 P039C 559F
2084                ATL27  RFF  ALDENFF                                                     002085
2084 P039D AF0C
2085                       UJP  TRD8                 NO ALARM, EXIT                         002086
2085 P039F 0109
2086                ATL29  LDC  RAMADD,$0F                                                   002087
2086 P039F 840F
```



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2088                      TA    RAMS,BREGD                                    002089
2088 P03A0 CFF0
2089                      CJP   BMDL,ATL36      DECODE REPEAT COUNTER-DETERMINE 002090
2089 P03A1 29A7
2090                *                           NUMBER OF REREADS PERFORMED     002091
2091                      CJP   BMSB,ATL27                                      002092
2091 P03A2 519D
2092                      CJP   TRK7,ATL39      7 TRACK? YES - CHANGE PARITY    002093
2092 P03A3 73D8
2093                      SFF   THR             CHANGE THRESHOLD LEVEL FOR 9    002094
2093 P03A4 BF17
2094                *                           TRACK ATTEMPT 3                 002095
2095                ATL34A LDC  RAMD,$BF                                        002096
2095 P03A5 86BF
2096                      UJP   ATL9            SET HIGH DENSITY-REREAD RECORD  002097
2096 P03A6 018F
2097                ATL36 SFF   DEN             SET LOW DENSITY FOR ATTEMPTS    002098
2097 P03A7 BF25
2098                *                           2 AND 4                         002099
2099                      IA    RAMS,RAMD                                     002100
2099 P03A8 C608
2100                      UJP   ATL9A           RE-READ RECORD                  002101
2100 P03A9 8190
2101                      SPARE                                               002102
2101 P03AA FFFF
2102                      SPARE                                               002103
2102 P03AB FFFF
2103          03D8 *      ORG   START1+$3D8                                   002104
2104                ATL39 SFF   PAREF           CHANGE PARITY SELECT FOR 7 TRK  002105
2104 P03D8 BF2A
2105                *                           ATTEMPTS 3 AND 4                002106
2106                      SFF   PARMD                                         002107
2106 P03D9 BF18
2107                      UJP   ATL34A          RE-READ RECORD                  002108
2107 P03DA 01A5
```

```
2109                ************************************************************************          002110
2110                *                                                                      *          002111
2111                *              *** OFF LINE MAINTENANCE ROUTINE ***                    *          002112
2112                *                                                                      *          002113
2113                ************************************************************************          002114


2115      03AC P            ORG   START1+$3AC                                                        002116
2116                OLM1    SFF   JGRP9           ENABLE JUMP CONDITION GROUP 9                      002117
2116 P03AC BF29
2117                        RFF   DEN             SELECT DENSITY ACCORDING TO                        002118
2117 P03AD AF25
2118                *                             TO MSW3                                            002119
2119                        CJP   MSW3+OLM5                                                          002120
2119 P03AF 1180
2120                        SFF   DEN                                                                002121
2120 P03AF BF25
2121                OLM5    SFF   SFMKFF          SET READ INDEX ACCORDING                           002122
2121 P03B0 BF32
2122                *                             MSW2                                               002123
2123                        CJP   MSW2+OLM15                                                         002124
2123 P03B1 1588
2124                        RFF   SFMKFF          WRITE OPERATION                                    002125
2124 P03B2 AF32
2125                        LDC   WCD+$FF         ALL 0'S OR ALL  1'S TO OUTPUT                      002126
2125 P03B3 88FF
2126                *                             REGISTER ACCORDING TO MSW1                         002127
2127                        CJP   MSW1+OLM13                                                         002128
2127 P03B4 8986
2128                        LDC   WCD+$00                                                            002129
2128 P03B5 8800
2129                *                             SET WRITE COMMAND F/F                              002130
2130                OLM13   SFF   WP                                                                 002131
2130 P03B6 BF1C
2131                        SFF   WRT                                                                002132
2131 P03B7 BF13
2132                OLM15   RFF   JGRP9                                                              002133
2132 P03B8 AF29
```

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 2134              OLM16  IA   PCS,RAMD                                                     002135
 2134 P03B9 C60F
 2135                     UJP  SG01                INITIATE OPERATION                        002136
 2135 P03BA 0013
 2136              OLM21  CJP  ONOFLN,OLM37        MAINTENANCE LOOP - LINE SWITCH IN         002137
 2136 P03BB 47CB
 2137              *                               ON POSITION? YES-EXIT                     002138

 2139                     SFF  JGRP9               ENABLE JUMP CONDITION GROUP 9             002140
 2139 P03BC BF29
 2140                     CJP  EOT,OLM36           END OF TAPE? YES-EXIT                     002141
 2140 P03BD 1DCA
 2141                     RFF  JGRP9               DISABLE JC GROUP 9                        002142
 2141 P03BE AF29
 2142                     CJP  SFMKJC,OLM30        READ OPERATION? YES-CONTINUE              002143
 2142 P03BF 39C3
 2143                     IA   PCS,RAMD            WRITE OPERATION                           002144
 2143 P03C0 C60F
 2144                     UJP  WSR1                CALL WRITE STROBE SUBROUTINE              002145
 2144 P03C1 0138
 2145                     UJP  OLM21               CONTINUE LOOP                             002146
 2145 P03C2 0188
 2146              OLM30  CJP  RSTRLT,OLM33        READ OPERATION                            002147
 2146 P03C3 53C6
 2147                     CJP  FBY,OLM35A          FORMATTER BUSY? YES-CONTINUE              002148
 2147 P03C4 79C9
 2148                     UJP  OLM16               END OF RECORD - RESTART READ              002149
 2148 P03C5 0189
 2149              OLM33  IA   PCS,RAMD                                                     002150
 2149 P03C6 C60F
```

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2151                      UJP RDS1          CALL READ STROBE SUBROUTINE          002152
2151 P03C7 00E8
2152                      UJP OLM21         CONTINUE MAINTENANCE LOOP            002153
2152 P03C8 0188
2153            OLM35A CJP  RDY,OLM21       UNIT READY? YES-CONTINUE             002154
2153 P03C9 75B8
2154            OLM36  RFF  JGRP9                                                002155
2154 P03CA AF29
2155            OLM37  RFF  FEN             TERMINATE TAPE MOTION                002156
2155 P03CB AF12
2156            OLM38  CJP  ONOFLN,OLM40    WAIT FOR LINE SWITCH "ON" LOOP       002157
2156 P03CC 47CE
2157            OLM39  UJP  OLM38           CONTINUE LOOP                        002158
2157 P03CD 01CC
2158            OLM40  RFF  OFLMTFF                                              002159
2158 P03CE AF0A
2159                      UJP  YRDB         EXIT FROM MAINTENANCE                002160
2159 P03CF 00F9
2160       0400 P         ORG  START1+$400                                       002161
2161                      END  START1                                            002162

PGM= 0400 ( 1024)   COM = 0000 (    0)   DAT = 0000 (    0)
```

ACK	0405	ADRERR	0329	AINLS	0294	AINUS	0295	ALARMF	0406
ALARMJ	0330	ALDENF	0407	ALDENJ	0331	ALJ1	0578	ALJ10	0584
ALJ6	0581	ALTERC	0332	AOUTLD	0284	AOUTUD	0279	AOE1	0654
AOE6	0659	ASJ1	1009	ASR1	1997	ASR10	2004	ASR12	2006
ATL1	2064	ATL13	2071	ATL18	2073	ATL26	2083	ATL27	2084
ATL29	2086	ATL34A	2095	ATL36	2097	ATL39	2104	ATL9	2067
ATL9A	2068	AUTOLD	0333	AUXFF	0408	AUXJC	0334	BANKD	0275
BE1FNR	0409	BE1F	0335	BE2F	0336	BE2LD	0285	BE2LS	0306
BE2UD	0286	BE2US	0307	BKS1	0935	BKT1	1228	BKT4	1231
BKT6	1233	BL1	0944	BMDL	0337	BMSB	0338	BREGD	0287
BREGS	0296	BSC1	0774	BSC17	0791	BSC23	0800	BSC25	0802
BSC26	0804	BSC31	0810	BSC7	0779	BSC9	0781	BSP1	1560
BSR1	0820	BUSBSY	0339	BUSY	0410	CBS1	0979	CBS6	0986
CBS9	0989	CDMAER	0311	CER	0340	CERST	0411	CERSTJ	0341
CESTDT	0312	CLOSTP	0313	CLHER	0314	CLSTAT	0315	CNALU	0413
CNB1	1578	CNTPRT	0414	COMP1	0412	COUT	0342	CRCERJ	0343
CREQ	0316	CRJ	0344	CST1	0832	CWALD	0280	CWALS	0302
CWAUD	0282	CWAUL	0345	CWAUM	0346	CWAUS	0304	CWS1	0998
DBL1	1462	DBL11	1477	DEN	0415	DFD1	1304	DFD10	1315
DFD14	1324	DFD17	1327	DFD18A	1331	DFD1B	1306	DFD5	1309
DFD9	1313	DMAREQ	0317	DMAWCP	0347	DMWRPT	0416	DTE0	1418
DTE12	1432	DTE16	1438	DTE8	1427	ENRDB	0417	ENWDSY	0418
EOP	0419	EOT	0348	EOTST	0420	EOTSTJ	0349	EQUAL	0350
ERS	0421	ESA0	1390	ESA1	1391	ESA11	1400	ESA15	1404
ESA6	1395	ESA9	1398	FBY	0351	FDS1	1378	FEN	0422
FER0	1628	FER1	1629	FER5	1632	FER7	1634	FER9	1637
FMK	0352	FMKST	0423	FPT	0353	FRCBUS	0424	FRJ1	1450
FRSTDT	0354	FST1	0966	FWA1	0925	GO	0425	HERLD	0426
HEROUT	0355	HFWRD	0356	I	0000	IDENT	0357	INTRSP	0427
INX2FF	0428	INX2JC	0358	IRQ1	0857	IRQ10	0871	IRQ12	0875
IRQ5	0864	JGRP9	0429	LDP	0359	LFA1	0957	LRCRCF	0430
LRCRCJ	0360	LWD	0431	MC1	0536	MC11	0546	MC13	0548
MC6	0541	MODE0	0251	MODE1	0252	MODE2	0253	MODE3	0254
MODE4	0255	MODE5	0256	MODE6	0258	MODE7	0259	MODE8	0260
MODE9	0261	MODEA	0262	MODEB	0264	MODEC	0265	MODED	0266
MODEE	0267	MODEF	0268	MOP1	0361	MOP2	0362	MSW1	0366
MSW2	0367	MSW3	0368	NOCOMP	0369	NRZI	0374	NU	0273
NU1	0288	OFL	0432	OFLMTF	0436	OFLMTJ	0370	OLM1	2116
OLM13	2130	OLM15	2132	OLM16	2134	OLM21	2136	OLM30	2146
OLM33	2149	OLM35A	2153	OLM36	2154	OLM37	2155	OLM38	2156
OLM39	2157	OLM40	2158	OLM5	2121	ONBUSF	0437	ONBUSJ	0371
ONL	0372	ONOFLN	0373	PARERR	0376	PARFF	0438	PARJC	0377
PARLT	0375	PARMD	0439	PCD	0277	PCH10	1248	PCH13	1251
PCH15	1253	PCH17	1255	PCH2	1240	PCS	0298	PRGPRT	0378
PRTOR	0440	PRTFLT	0379	QS	0297	RALTIF	0441	RALTIJ	0380
RAMADD	0274	RAMD	0276	RAMS	0292	RD1	1648	RD23	1662
RD27	1667	RD32	1673	RD35	1678	RD41	1684	RD45	1689
RD46	1691	RD51	1698	RD55	1702	RD59	1708	RD60	1709
RD63	1712	RD64A	1718	RD71	1723	RD73	1725	RD79	1727
RD86	1735	RD91	1742	RD97	1753	RD99	1755	RDM	0381
RDS1	1784	RDS10	1787	RDS11	1788	RDS16	1795	RDS18	1799

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REV	0442	REW	0443	RJC1	0568	RMBNKS	0446	RMEXEC	0383
ROL1	1508	ROL4	1511	ROL7	1514	RP	0384	RPL1	0559
RPLY	0319	RQBUS1	0444	RQBUS2	0445	RSTRLN	0385	RSTRLT	0386
RWD1	1499	RWMOD	0447	RWS	0387	SBF1F	0320	SBF2F	0321
SELBF1	0449	SELBF2	0450	SELBRE	0451	SFB1	1550	SFB2	1551
SFF1	1525	SFF12	1538	SFF5	1526	SFF6	1527	SFF6B	1529
SFMKFF	0448	SFMKJC	0388	SFTHFR	0322	SG01	1364	SLCTDF	0452
SLCTDJ	0389	SNS1	2047	SNS3	2049	SNS5	2054	SOP	0390
SPF1	1569	SPM	0453	SPRFF	0454	SPRJC	0391	SRSTR	0323
STA1	1023	STA1A	1043	STA19	1044	START1	0527	STB1	1080
STB101	1181	STB103	1183	STB105	1185	STB107	1188	STB109	1190
STB111	1192	STB113	1194	STB115	1196	STB117	1198	STB119	1200
STB121	1202	STB123	1204	STB126	1208	STB128	1215	STB29	1115
STB31	1117	STB33	1119	STB34	1121	STB36	1123	STB38	1125
STB40	1127	STB49	1137	STB51	1139	STB62	1154	STB77	1158
STB82	1163	STC1	1284	STC4	1288	STC6A	1291	STC9	1294
STD1	1269	SWSTR	0324	TAD0	0455	TAD1	0456	TDS1	1056
TDS2	1057	TFB1	1486	TFB3	1489	TFER	0392	THR	0457
TRB1	0597	TRB10	0615	TRB11	0619	TRB12	0620	TRB4	0600
TRD0	1815	TRD1	1819	TRD11	1842	TRD3	1821	TRD3A	1822
TRD4	1825	TRD7	1833	TRD7A	1834	TRD7B	1835	TRD8	1839
TRK7	0393	TST1	0889	TST10	0899	TST13	0902	TST16	0905
TST19	090B	TST24	0914	TST5	0893	TST7	0895	TWI0	1975
TWT1	1976	TWT9	1986	UNS1	0711	UNS11	0717	UNS13	0719
UNS21	0729	UNS25	0733	UNS30	0739	UNS35	0744	UNS37	0747
UNS42	0753	UNS45	0756	UNS48	0759	UNS50	0762	UNTPRT	0394
VER1	1588	VER10	1595	VER5	1589	VER7A	1592	WCD	0278
WCEMPT	0395	WCS	0293	WFM	0458	WL1	0629	WL12	0644
WL4	0633	WL6	0637	WL9	0641	WORD	0396	WP	0459
WRF1	1611	WRF3	1613	WRT	0460	WRTODF	0462	WRTODJ	0397
WSR1	1853	WSR12	1864	WSR12A	1865	WSR14	1867	WSR22	1874
WSR26	1877	WSR5A	1858	WSR9	1861	WSTRLN	0398	WSTRLT	0399
WT1	1898	WT16B	1917	WT17	1918	WT22	1919	WT24	1926
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WT6	1903	WTROMP	0461						

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Hardware Reference/Maintenance Manual

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