



CDC[®] EMULATION COUPLER

DY159-A/B



CDC[®] EMULATION COUPLER
DY159-A/B

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an ECO or FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
DY159-A	01 02 03 04	06001 06568 06612	
DY159-B	01		



LIST OF EFFECTIVE PAGES

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PREFACE

This manual provides basic information on the CDC® Emulation Couplers DY159-A and DY159-B which are part of a Network Processor Unit. Sufficient data is included in this document to enable customer engineers to install and service the coupler.

The network processor unit with the emulation coupler emulates 6671 and 6676 data set controllers to permit direct replacement.

The A and B version cabinets referenced in this manual are described in the Network

Processor Unit Equipment Cabinets manual. Changes to the coupler cables were made to accommodate the B version cabinet, which contains electromagnetic interference protection features.

The related publications listed below are available through the CDC Literature and Distribution Services, 308 North Dale Street, St. Paul, Minnesota 55103.

<u>Publication Title</u>	<u>Publication Number</u>
6671/6676 Emulation Controlware, Reference Manual	74750800
2550-100 Emulator 6671/6676, Installation Handbook	74750900
255X Network Processor Unit, Hardware Maintenance Manual	60472000
255X Network Processor Unit, Hardware Reference Manual	60472800
255X Network Processor Unit, Site Preparation Manual	74641200
Controlware Product Configurator 2550-100	74750600
CYBER 70, Models 72/73/74 Computer Systems, Instruction Description	60347300
6000/CYBER 70 System Maintenance Monitor, Reference Manual, Volume 5	60160600
CYBER 70, Model 72 Computer System, Reference Manual, Volume 1	60347000
6400/6500/6600 Computer Systems, Reference Manual	60100000
MP17 I/O Extender Unit, Hardware Reference Manual	39566900
255X Network Processor Unit Equipment Cabinets, Hardware Maintenance Manual	74873971



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The network processor unit (NPU) handles all communications between a host and a network of terminals. The coupler acts as a go-between for the host and the processor within the NPU. In this capacity the coupler buffers all signals from the host to the processor and all signals from the processor to the host.

A typical NPU is illustrated in figure 1-1. As shown in figure 1-2, the NPU contains eight basic blocks: the coupler, processor, memory, cassette, multiplexer, cyclic encoder, line adapter, and multiplex adapter. A separate hardware maintenance manual is available on each of these items. The overall function of the coupler is clearly shown in figure 1-3. The following paragraphs describe the physical and functional characteristics of the coupler.

PHYSICAL DESCRIPTION

The coupler consists of two circuit cards and associated cables. Each circuit card fits into the processor card cage, which is located at the top of the NPU cabinet. See figure 1-4.

The coupler occupies slots C and B. If two couplers are included in the NPU, the second one occupies slots AA and AB. The circuit card on the left or in slot C is the NPU interface. The circuit card on the right or in slot B is the channel synchronizer. Circuit card locations are shown in figure 1-5.

Both circuit cards have edge connectors which plug into mating connectors in the backplane of the card cage. Three jumper cables at the front of the bay connect the two cards together. Backplane wiring and a jumper cable connect the interface to the processor. Cables from the host connect to the synchronizer at the back of the card cage. The following paragraphs describe the synchronizer, the interface, and major cables.

SYNCHRONIZER

The synchronizer is a printed circuit card containing mostly integrated circuits in standard packages. Some discrete-component circuits are also on the card. Five DIP-type switches on the synchronizer must be set prior to installation. A potentiometer is located on the front edge

of the card so that it is accessible after the coupler is installed. All connections between the host and coupler are made to the synchronizer.

INTERFACE

The interface is a printed circuit card containing mostly integrated circuits in standard packages. A toggle switch is located on the front edge of the card so that it is accessible after the coupler is installed. All connections between the coupler and the processor are made to the interface.

MAJOR CABLES

Three short ribbon cables connect J1, J2, and J3 of the synchronizer to J1, J2, and J3 of the interface. The J cable has 20 conductors and is mainly used for spares and modifications. Both the J2 and J3 cables contain 50 conductors each and carry the major signals between circuit cards. J1, J2, and J3 are mounted on the front edge of each circuit card.

Two 19-conductor coaxial cables connect the synchronizer to the host. The length of each cable must be exactly 75 feet (22.8 m) and is made from three sections. A 5-foot (1.5-m) section is directly connected to the coupler for each cable, or in the B version NPU cabinets, the 5-foot cable connects to a cable enclosure assembly and then to the 65-foot (19.8-m) cable. This section is then connected to a 65-foot section, which would be connected to another 5-foot section before connecting to the host.

A typical installation of two couplers is shown in figure 1-6; cabling to coupler 1 shows the 65-foot cable combined with an optional 5-foot cable provided in the cable set.

FUNCTIONAL DESCRIPTION

The host can be connected to from one to eight external equipments. Each equipment connected to it is assigned a mutually exclusive address number of 0 to 7. The coupler has four such addresses, which the host recognizes as four separate equipments. One or more of these addresses can be turned off if it is not to be used. Equipment switches on the synchronizer are preset to the addresses assigned to the NPU.

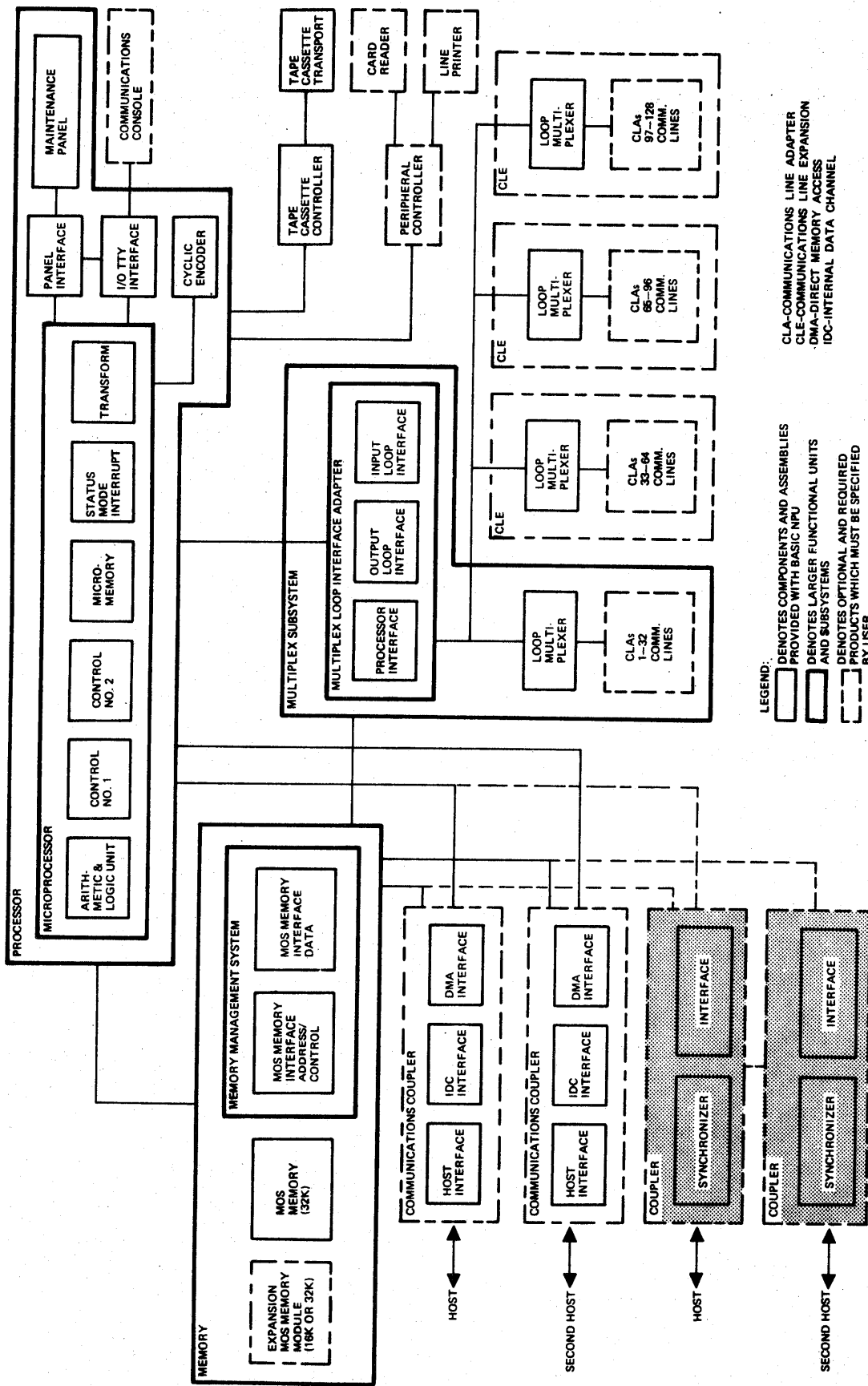


Figure 1-1. Network Processor Unit

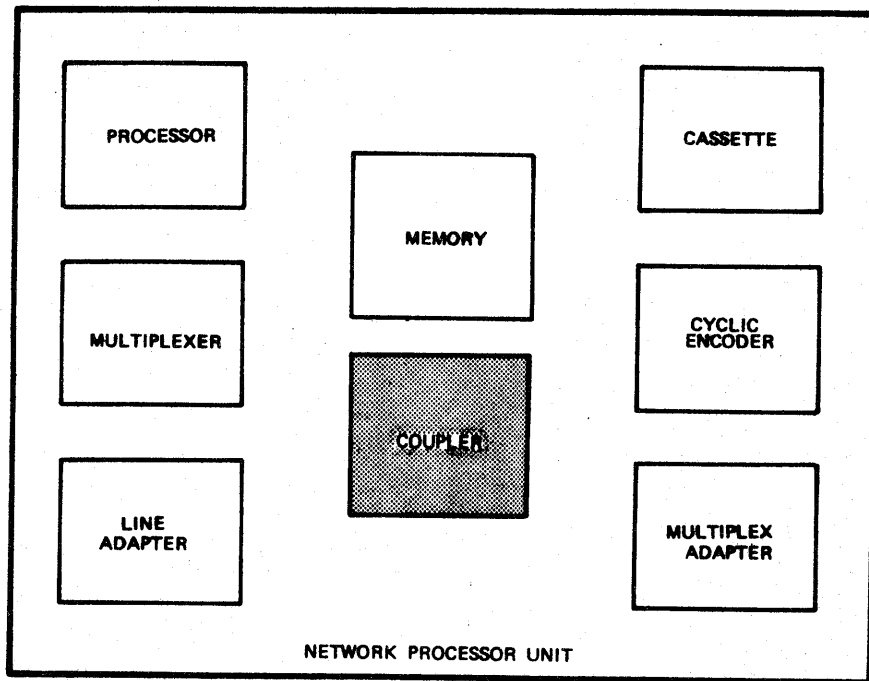


Figure 1-2. Functional Blocks of the NPU

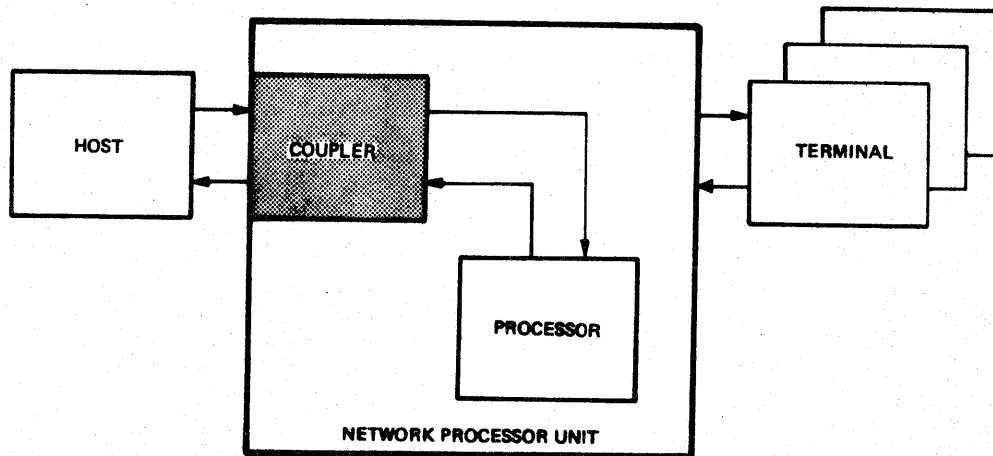
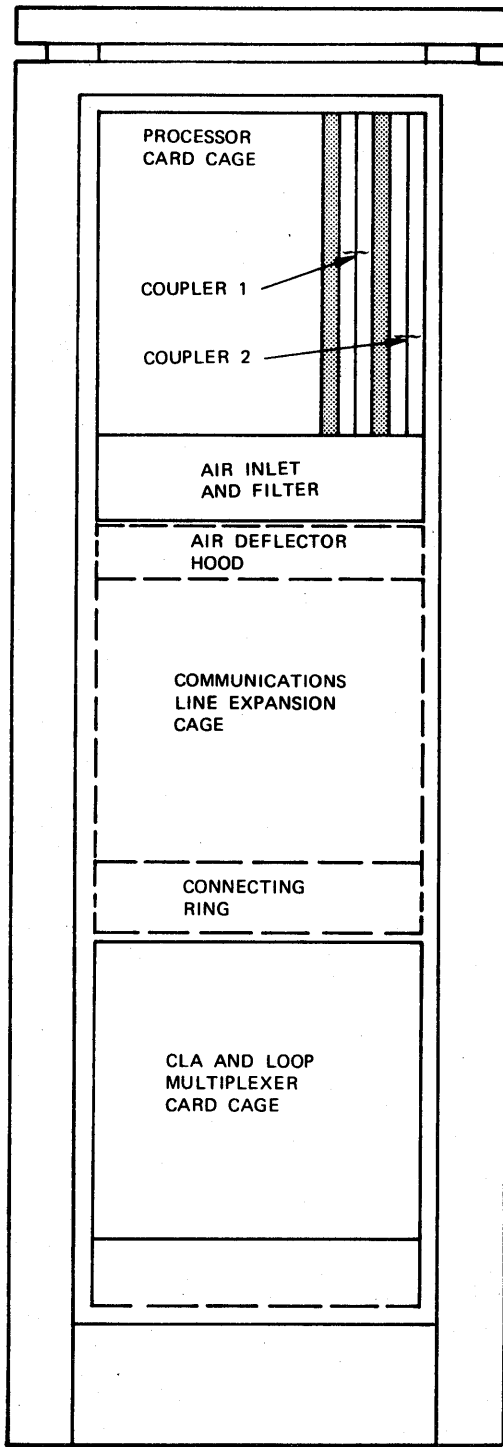


Figure 1-3. Coupler Function



M-586

Figure 1-4. Front View of NPU Cabinet

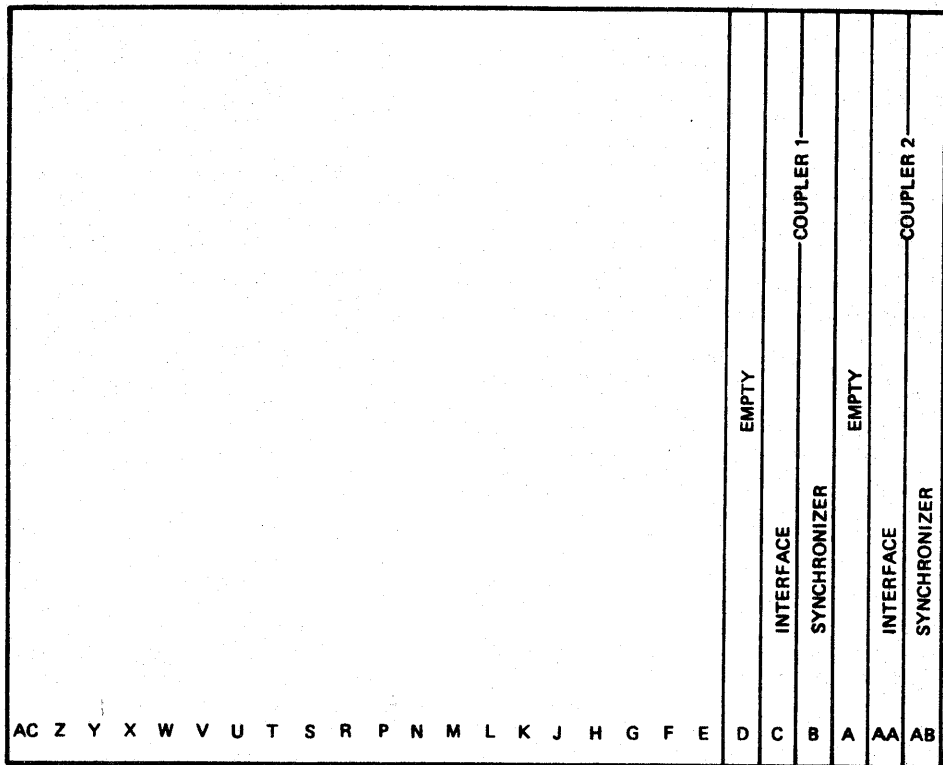


Figure 1-5. Circuit Card Locations

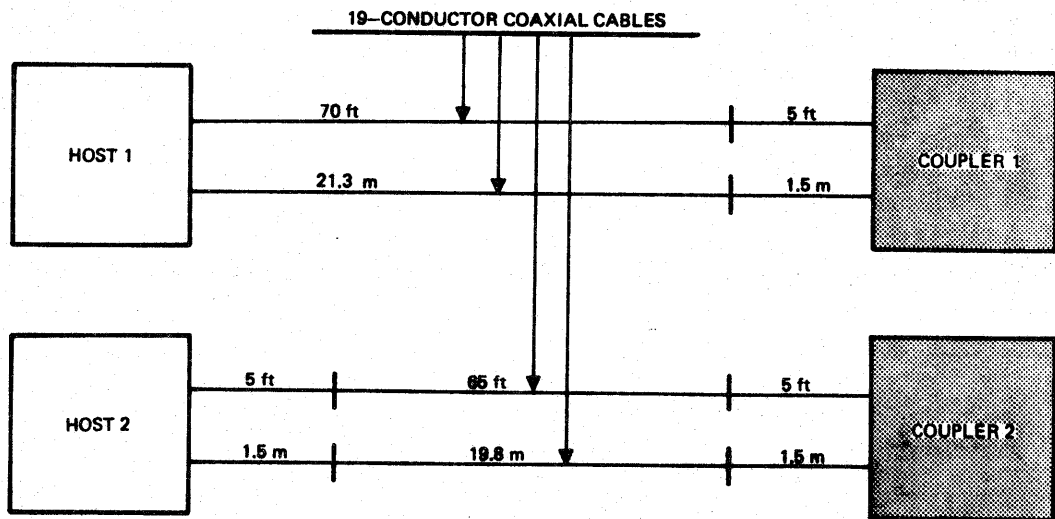


Figure 1-6. Two Couplers in a Typical Installation

All external equipments connected to the host are daisy chained and separated by 75 feet (22.8 m) of coaxial cable. The NPU may be directly connected to the host as shown in figure 1-6 or it may be anywhere in the daisy chain. The precise requirement of 75 feet (22.8 m) for cable length constitutes a propagation delay of 100 nanoseconds. When the host puts a word on the communications channel, it asks of each equipment, "Are you the equipment that I want to talk to? If you are or not, pass on this word to the next equipment in exactly 100 nanoseconds. If you are, then process this word and pass back the information that I want." See figure 1-7.

The coupler is controlled by the host, and the direction of data and signals refer to the host. Output data travels from the host to the coupler via the pass-on cable. Input data travels to the host from the coupler via the pass-back cable.

Before sending or receiving data, the host sends a function signal and a 12-bit function word to the coupler. Bits 9 through 11 contain the equipment number, Bits 0 and 1 contain one of three commands: output data, send status, or input data. If the equipment number is one that has been assigned to the coupler, the coupler will send an inactive signal to the host. Further transmission between coupler and host depends on the command in the function word.

OUTPUT DATA

If the command is to output data, the host sends a full signal and a data word to the coupler. The coupler then sends an empty signal to the host, stores the data word, and waits for the next data word. This process is repeated until all data has been transmitted, which is indicated when the host sends an inactive signal to the coupler. Data may be transferred at a rate of one million characters per second or two million characters per second

depending on the type of host. Both transfer rates use the same basic timing sequence for data output. See figure 1-8.

Because terminals connected to the NPU may transfer data at a slower rate than the host, the output data must be protected. This is done as follows. When the coupler stores the output data, a protect bit is set. When this same data goes out to a terminal device, the protect bit is cleared. If the host tries to output additional data to the same terminal device before the protect bit is cleared, a character reject bit is set. The new data is rejected, and this fact is sent to the host on the next input data command. The host will then keep sending the same data until the protect bit is cleared.

INPUT DATA

If the command is to input data, the coupler sends a full signal and a data word to the host. The host then sends an empty signal to the coupler. This process is repeated until all data has been transmitted, which is indicated when the coupler sends an inactive signal to the host. However, the input data process can be terminated at any time by the host sending an inactive signal to the coupler. The timing sequence for data input is shown in figure 1-9.

Because terminals connected to the NPU may transfer data when the host is busy, the input data must be protected. This is done as follows. When the coupler stores the input data, a protect bit is set. When this same data is transferred to the host, the protect bit is cleared. If the terminal device sends input data before the protect bit is cleared, the coupler will reject the data. However, the new input data is held in the processor until the protect bit is cleared.

SEND STATUS

If the command is to send status, the coupler sends a full signal and a data word

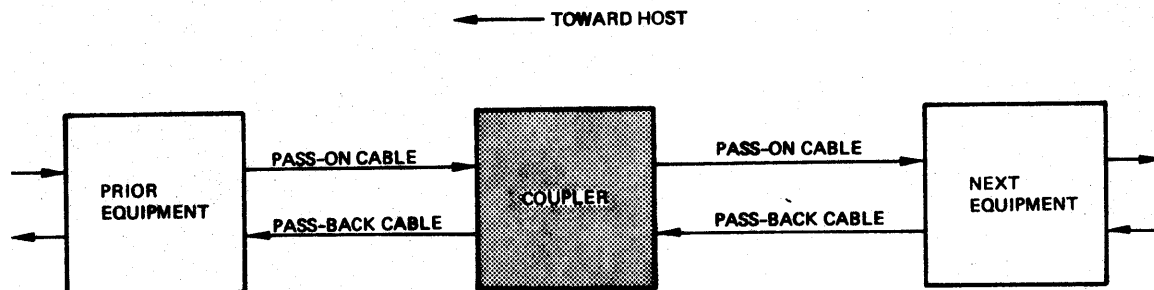
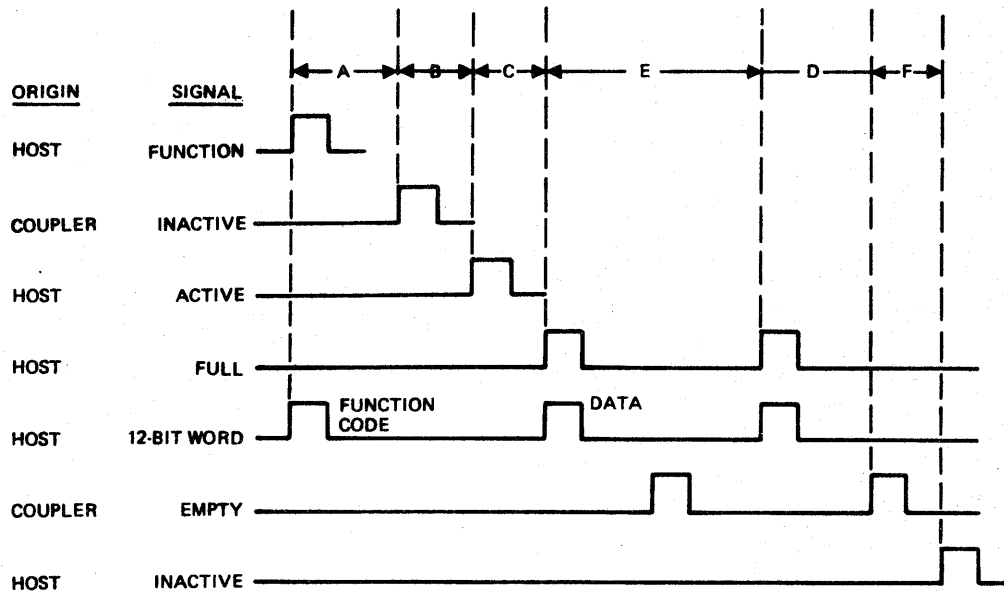


Figure 1-7. Coupler in a Typical Daisy Chain



TIME	FUNCTION OF	1 Mc/s	2 Mc/s	NOTES
A	COUPLER	1.0 μ s	0.5 μ s	2
B	HOST	100 ns	50 ns	
C	HOST	2 or 4 μ s	1 or 2 μ s	
D	COUPLER		50 ns	2, 3
E	COUPLER	1.0 μ s	0.5 μ s	
F	HOST	2.0 μ s	1.0 μ s	

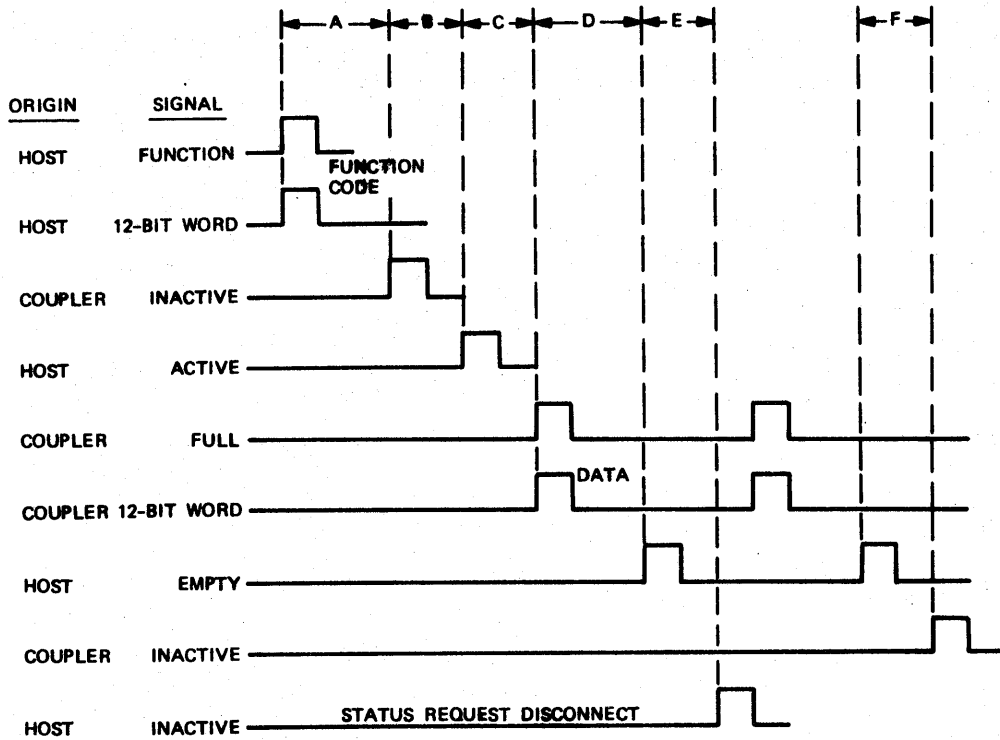
- NOTES: 1. MINIMUM TIMES ARE GIVEN ABOVE FOR TWO RATES OF DATA TRANSFER. THE ACTUAL TIMES ARE DEPENDENT ON SOFTWARE.
2. ACTUAL TIME IS A MULTIPLE OF THE MINIMUM TIME.
3. MAXIMUM TIME IS 450 ns FOR THE TRANSFER RATE OF 2 Mc/s.

Figure 1-8. Data Output Sequence

to the host. This data word contains the requested status. The host will then terminate the communications by sending an inactive signal to the coupler. The timing sequence for status requests is the same as for data input (figure 1-9).

CHARACTERISTICS

The electrical, physical, and environmental characteristics of the coupler are given in table 1-1.



TIME	FUNCTION OF	1 Mc/s	2 Mc/s	NOTES
A	COUPLER	1.0 μ s	0.5 μ s	2
B	HOST	100 ns	50 ns	
C	COUPLER			
D	HOST			2, 3
E	HOST	100 ns	50 ns	4
F	COUPLER	3.0 μ s	1.5 μ s	

- NOTES:
1. MINIMUM TIMES ARE GIVEN ABOVE FOR TWO RATES OF DATA TRANSFER. THE ACTUAL TIMES ARE DEPENDENT ON SOFTWARE.
 2. ACTUAL TIME IS A MULTIPLE OF THE MINIMUM TIME.
 3. MAXIMUM TIME IS 450 ns FOR THE TRANSFER RATE OF 2 Mc/s.
 4. MAXIMUM TIME IS A MULTIPLE OF ONE-THIRD THE MINIMUM TIME.

Figure 1-9. Data Input Sequence

TABLE 1-1. COUPLER CHARACTERISTICS

Parameter	Value
<u>Electrical</u>	
Input Voltage	+5.0 \pm .25 V dc, 6.0 amp
Logic Levels	standard TTL
Logic Polarity	positive
Data Transfer Rate	1M or 2M C/S maximum
<u>Physical</u>	
Circuit Cards	2 each
Length	14 inches (356 mm)
Width	11 inches (279 mm)
Thickness	0.063 inches (1.6 mm)
Weight (2 cards)	2.4 lb (1.1 kg)
Coaxial Cables	2 each 70 feet (21.3 m) or 65 feet (19.8 m)
	4 each 5 feet (1.5 m)
Ribbon Cables	1 each 20-conductors 2 each 50-conductors
Jumper Cable	1 each
Power Jumper	1 each (optional)
<u>Environmental</u>	
Temperature Range	50 to 95°F (10 to 35°C) operating 14 to 122°F (-10 to 50°C) nonoperating
Temperature Change	18°F/h (10°C/h) operating 27°F/h (15°C/h) nonoperating
Humidity Range	20 to 80% operating 10 to 90% nonoperating
Humidity Change	10%/h operating
Dew-point Temperature	79°F (26°C) maximum 25°F (-4°C) minimum
Altitude above Sea Level	6000 ft (1830 m) maximum
Altitude below Sea Level	1000 ft (305 m) maximum



The coupler has no operating controls and does not require programming. However, there are seven controls in the coupler; and the Network Processor Unit, of which the coupler is a part, does require programming. This section describes controls and delineates word formats.

CONTROLS

The location and function of the controls on the two circuit cards are given in the following paragraphs. These controls are the equipment switches, the clock adjustment controls, and the coupler select switch.

EQUIPMENT SWITCHES

The four equipment switches, S1 through S4, are located on the synchronizer. See figure 2-1. Each of these switches have eight individually selectable positions contained in a single package. See figure 2-2. The positions are numbered from 0 to 7, and one of them may be selected by setting it to ON. After selecting one position, set all other positions of that switch to OFF. No two switches should have the same position selected.

Each equipment switch if selected by the host will in effect connect the host to a particular set of terminals. Switch S1 is associated with one set of terminals; switch S2 is associated with another set; and switches S3 and S4 are each associated with still other sets. The position to which each switch is set depends on the program in the host. Setting all positions of an equipment switch of OFF will in effect disconnect a set of terminals.

CLOCK ADJUSTMENT

The clock adjustment switch S5 and the clock adjustment R6 are located on the synchronizer. Switch S5 has eight individually-selectable positions contained in a single package (figure 2-2). The positions are labeled A through H, and one or more of them may be selected by setting them to ON. This switch, which is preset at the factory, provides for an adjustment of clock pulse width and leading edge. Potentiometer R6, which is also preset at the factory, is a fine adjustment of the leading edge of the clock pulse. This adjustment can be made with the coupler installed.

COUPLER SELECT SWITCH

The coupler select switch S1 is a two position toggle located on the interface. See figure 2-3. Switch S1 enables the processor to differentiate between two couplers in the same network processor unit. The two switch positions are labeled 3 (for up) and 2 (for down). The position to which the switch is set depends on the program in the NPU.

WORD FORMATS

The formats of the function word and the status word are given in the following paragraphs.

FUNCTION WORD

The function word contains 12 bits and originates in the host. Bit zero is the least significant. The format of the function word is shown in figure 2-4. Binary command codes contained in bits 0 and 1 are: 00 is no action; 01 is output data; 10 is send status; and 11 is input data. Bits 3 through 8 are used for maintenance. The equipment number, as defined by the host program, is contained in bit 9 through 11.

The word stored in the F register is principally the same as the function word with the following exceptions. Bits 9 and 10 contain an equipment address which defines which set of terminals the host is addressing. Bit 11 indicates that the coupler has been selected by the host for communications.

STATUS WORD

The status word contains 12 bits and originates in the coupler. Bit zero is the least significant. The format of the status word is shown in figure 2-5. Status bits 0, 1, 4, and 5 carry information on one of four sets of terminals. Bit 1 indicates that data from one of the terminals is waiting to be transmitted to the host. Bit 0 says that the host did not input data before additional data arrived from that same terminal; as a result, the new data was lost. Actually the new data was retained in a register.

If the host does not output data within a specific time frame, bit 4 indicates that an output data failure has occurred.

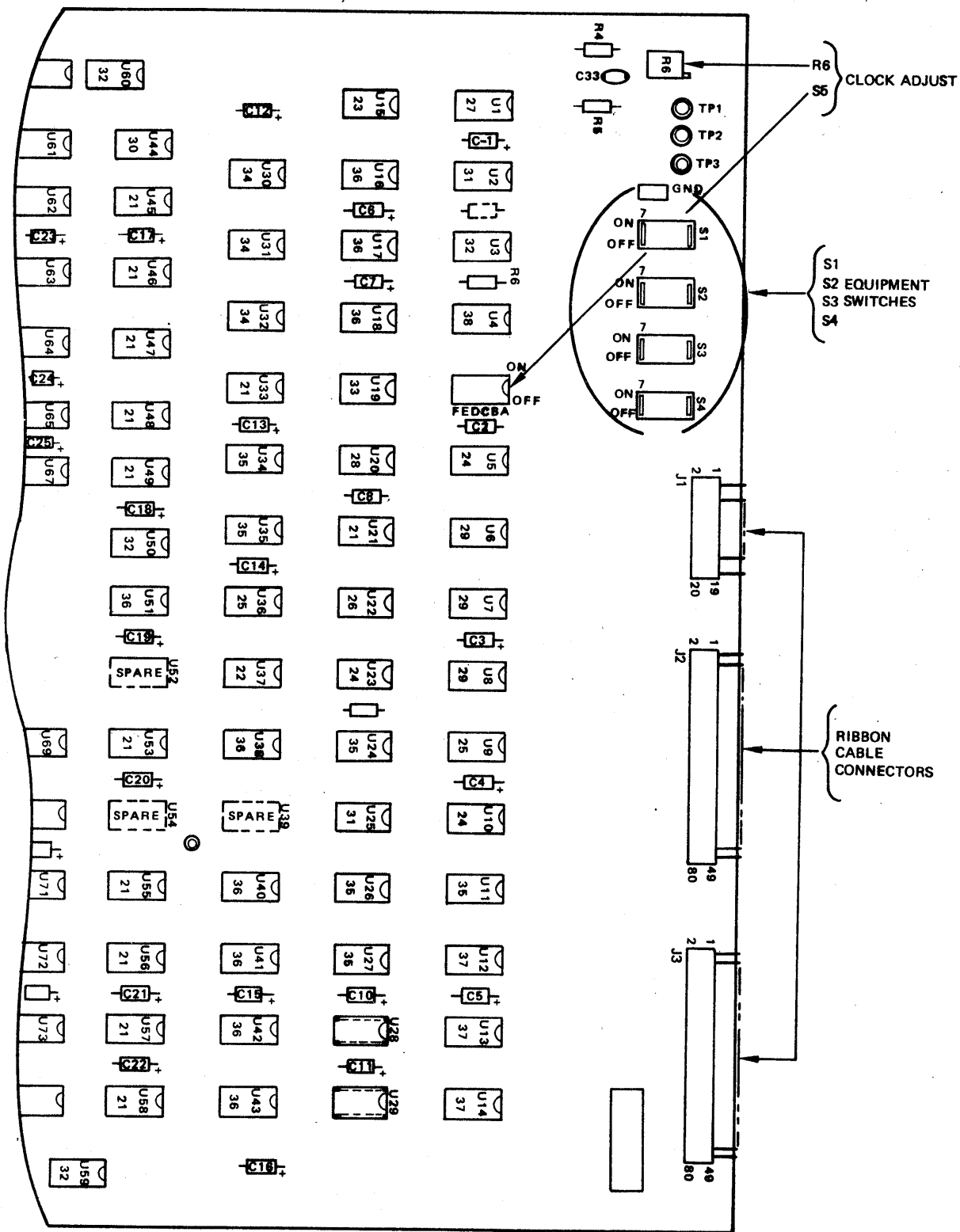
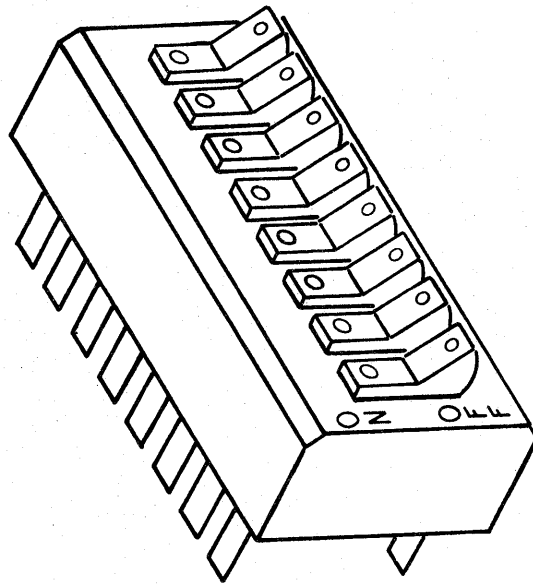


Figure 2-1. Synchronizer Controls

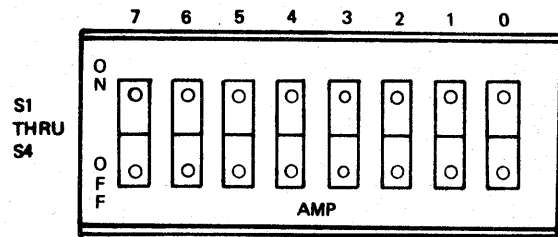
This time frame is determined by the data transfer rate of the receiving terminal. Bit 5 indicates that a parity error exists in memory.

Function word commands clear the status bits. Input data clears bits 0 and 1; output data clear bit 4; and send status clear bit 5.

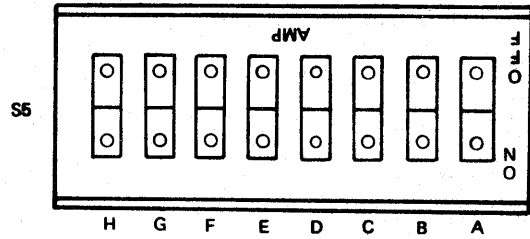
A. SYNCHRONIZER 7487303B



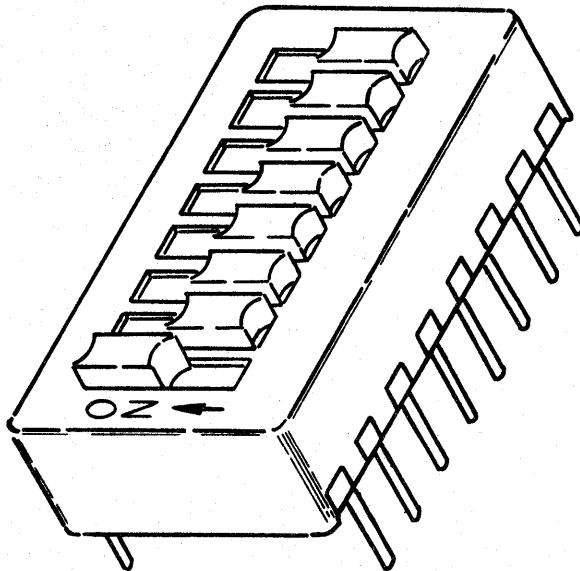
EQUIPMENT SWITCHES



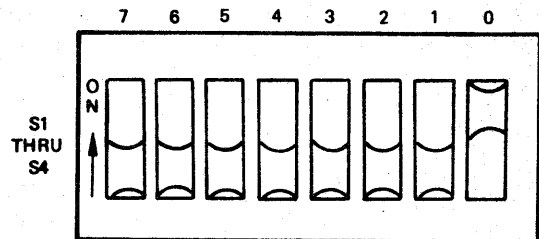
CLOCK ADJUST. SWITCH



B. SYNCHRONIZER 7487304I



EQUIPMENT SWITCHES



CLOCK ADJUST. SWITCH

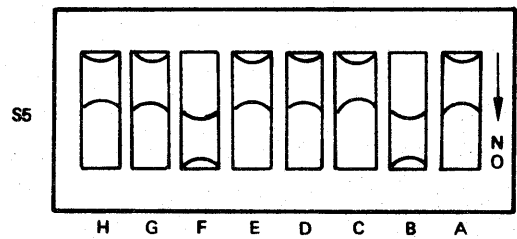


Figure 2-2. DIP Switches

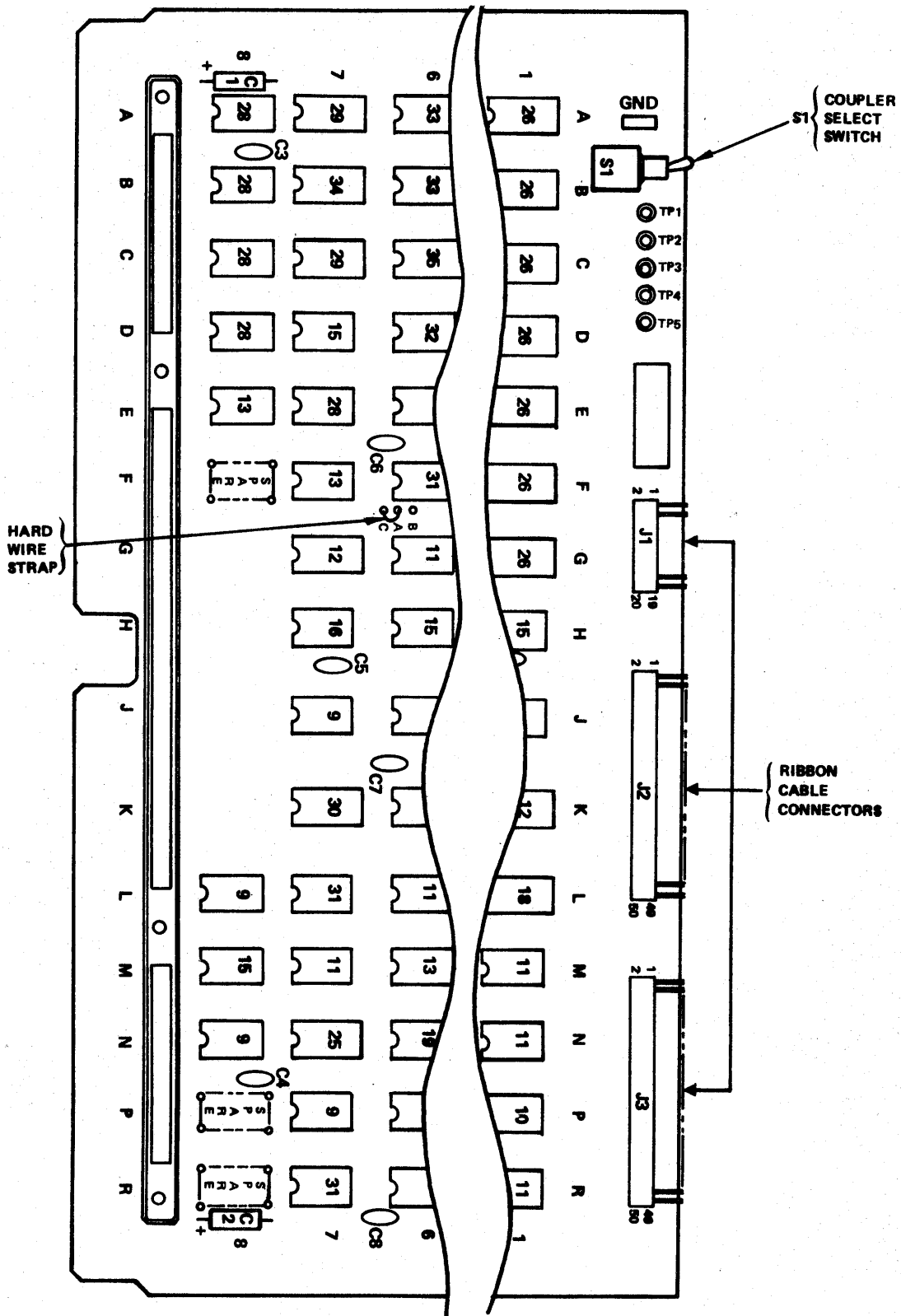
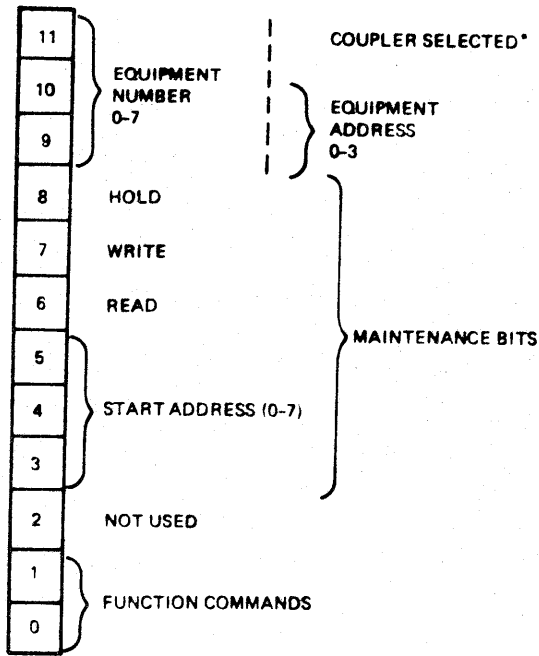


Figure 2-3. Interface Controls



*CHANGES IN FUNCTION WORD AS STORED IN F REGISTER.

Figure 2-4. Function Word Format

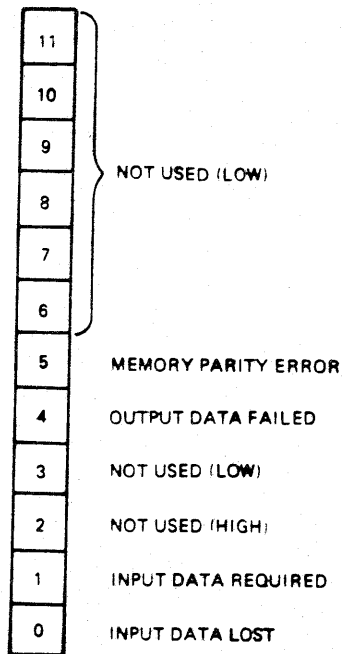


Figure 2-5. Status Word Format



Installation and checkout of the coupler is usually performed as a part of the installation and checkout of a Network Processor Unit. The NPU installation procedure includes a thorough checkout at the factory and on the site. The procedures in this section are for installing a coupler as an add-on or replacement to an existing subsystem. The following paragraphs contain data on uncrating, installing and checking out a coupler.

UNCRATING

If the coupler is received already installed in a card cage, refer to the NPU hardware maintenance manual for uncrating instructions. If the coupler is received in a padded container, carefully unpack the major parts and check them for damage. See tables 3-1 and 3-2. If anything is damaged, refer to the field procedures guide for disposition of damaged equipment.

INSTALLATION

Perform the installation in the order given, skipping over paragraphs that are not applicable. Refer to the site preparation documents as needed. The installation sequence is given first, and then each item in the sequence is expanded to a complete procedure. Identify each item from the

table of major components, tables 3-1 and 3-2.

INSTALLATION SEQUENCE

1. Install power jumper cable (figure 3-1) at rear of card cage.

NOTE

The power jumper is only installed if an external 5 V dc supply is not wired to the coupler. Normally the external supply is used to permit pass-on and pass-back operations when NPU power is removed.

2. Install jumper cable (figure 3-1) at rear of card cage.
3. Install coaxial cables (figure 3-2) on connectors at rear of card cage.
4. Set equipment switches (figure 2-1) on synchronizer.
5. Install ribbon cables (figure 3-3) between synchronizer and interface.
6. Install both circuit cards concurrently into card cage (figure 1-5).
7. Set coupler select switch on interface card.

TABLE 3-1. DY159-A EMULATION COUPLER AND CABLE SET, MAJOR COMPONENTS

Description	Part Number	Quantity
Synchronizer circuit card } 1st version [†]	74873038	1
Interface circuit card } 1st version [†]	74872961	1
or		
Synchronizer circuit card } 2nd version [†]	74873040	1
Interface circuit card } 2nd version [†]	74872963	1
Ribbon cable, 50 conductors	74843700	2
Ribbon cable, 20 conductors	74845800	1
Jumper cable, 3 connectors	74870828	1
Power jumper (optional)	88964500	1
Cable set (purchased separately with DY159-A)		
- Coaxial cable, 65 ft (19.8 m)	19191600	2
- Coaxial cable, 5 ft (1.5 m)	52675100	2
- Coaxial cable, 5 ft (1.5 m)	88947800	4
	††74875766	
[†] Only one first version or second version card set is required. First version and second version cards in combination are not compatible. ^{††} Used with EMI (B version) cabinets		

TABLE 3-2. DY159-B EMULATION COUPLER, MAJOR COMPONENTS

Description	Part Number	Quantity
Synchronizer circuit card	74873040	1
Interface circuit card	74872963	1
Ribbon cable, 50 conductors	74843700	1
Ribbon cable, 20 conductors	74845800	1
Jumper cable, 3 connectors	74870828	1
Power cable (optional)	88964500	1
Cable set (supplied with DY159-B)		
- Coaxial cable, 65 ft (19.8 m)	19191600	2
- Coaxial cable, 5 ft (1.5 m)	52675100	2
- Coaxial cable, 5 ft (1.5 m)	74875766	4

POWER JUMPER

1. Plug power jumper 88964500 into pins 1 through 4 of slot B. See figure 3-1.
2. If two couplers are to be installed, plug another power jumper 88964500 into pins 1 through 4 of slot AB (figure 3-1).

JUMPER CABLE

1. Plug P1 of jumper cable 74870828 into pins 280 through 294 of slot AA (figure 3-2). The top conductor should be connected to the top pin.
2. Plug P2 of the jumper cable into pins 280 through 294 of slot C.
3. Plug P3 of the jumper cable into pins 280 through 294 of slot G.

COAXIAL CABLES

The DY159-A coupler cables are installed in the A version cabinet as shown in figure

3-4. The DY159-B coupler cables are installed in the B version cabinet as shown in figure 3-5.

CAUTION

When installing pass-on and pass-back cable connectors to the backplane pins, tie each 5-foot coaxial cable to the supporting structure of the bay. If this is not done, backplane pins may be bent or permanently damaged.

NOTE

If the coupler is the only equipment to be connected to the host or the last one on the daisy chain, the pass-on and pass-back cables to the next equipment are not required.

If the host is provided with two 5-foot cables, they can be used in place of the 5-foot cables extending from the 65-foot pass-on and pass-back cables to the host.

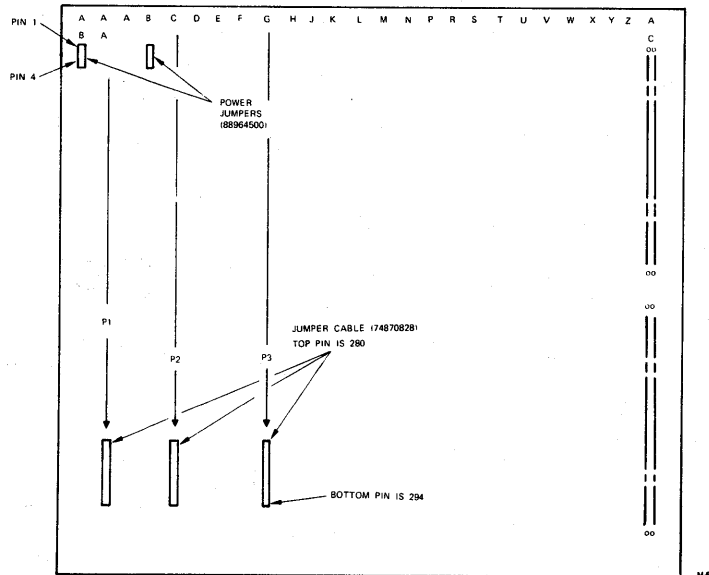


Figure 3-1. Jumper Cable Connectors

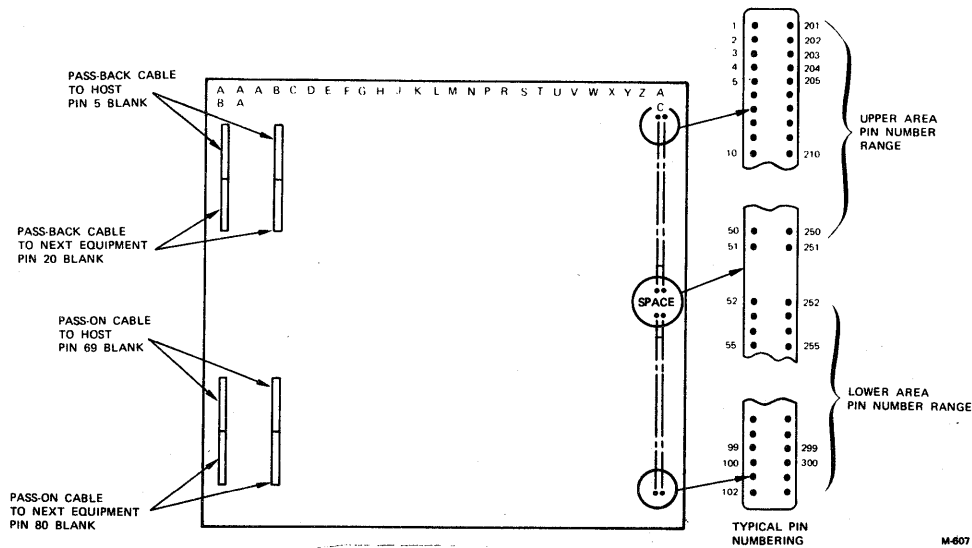


Figure 3-2. 5-Foot Coaxial Cables on Synchronizer

EQUIPMENT SWITCHES

1. Set all positions of equipment switch S1 to OFF (figures 2-1 and 2-2).
2. Set all positions of S2 to OFF.
3. Set all positions of S3 to OFF.
4. Set all positions of S4 to OFF.
5. Refer to NPU program and determine which of four sets of terminals are connected, and to which equipment switch each set of terminals correspond.
6. Refer to host program and determine which equipment addresses are assigned to the coupler.
7. Select an equipment switch to be used (step 5) and set its host-assigned position (step 6) to ON.
8. Repeat step 7 for each assigned equipment switch.

NOTE

All equipment switches cannot be used. Those switches not in use must be set to OFF. No switch in use can have more than one position set to ON. No two switches can have the same position set to ON.

9. If two couplers are to be installed, repeat steps 1 through 8 for the second coupler.

RIBBON CABLES

1. Place synchronizer (figure 2-1) on a flat surface with its components facing up.

2. Connect three ribbon cables to synchronizer as follows (figure 3-3):

NOTE

If no modifications have been made to the coupler, omit steps 2a and 4a which install the J1 cable. The J1 cable is provided for spares.

- a. Plug cable 74845800 into J1 of synchronizer so that blue stripe is facing away from J2.
 - b. Plug cable 74843700 into J2 of synchronizer so that blue stripe is facing J1.
 - c. Plug cable 74843700 into J3 of synchronizer so that blue stripe is facing J2.
3. Place interface (figure 2-3) on top of synchronizer with components facing up so that J1 of the interface is directly over J1 of synchronizer.
 4. Connect three ribbon cables to interface as follows (figure 3-3):
 - a. Plug cable from J1 of synchronizer into J1 of interface.
 - b. Plug cable from J2 of synchronizer into J2 of interface.
 - c. Plug cable from J3 of synchronizer into J3 of interface.
 5. If two couplers are to be installed, repeat steps 1 through 4 for the second coupler.

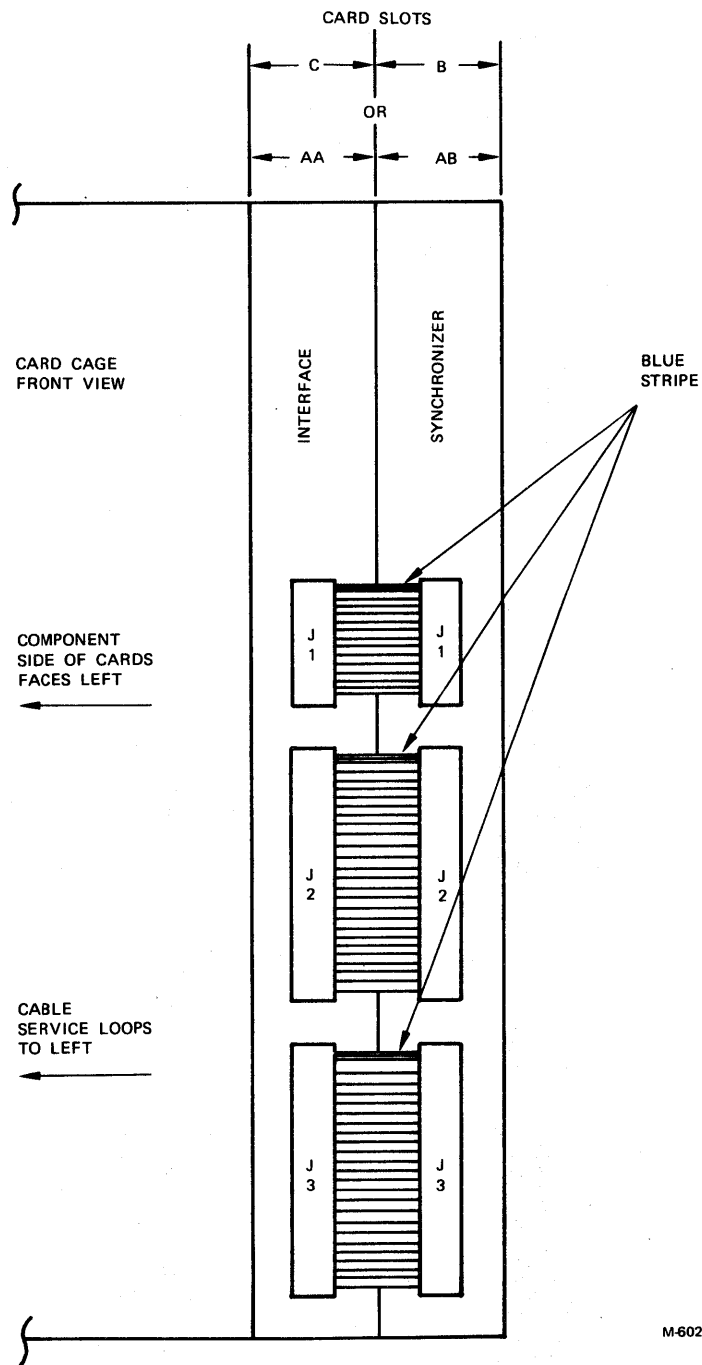
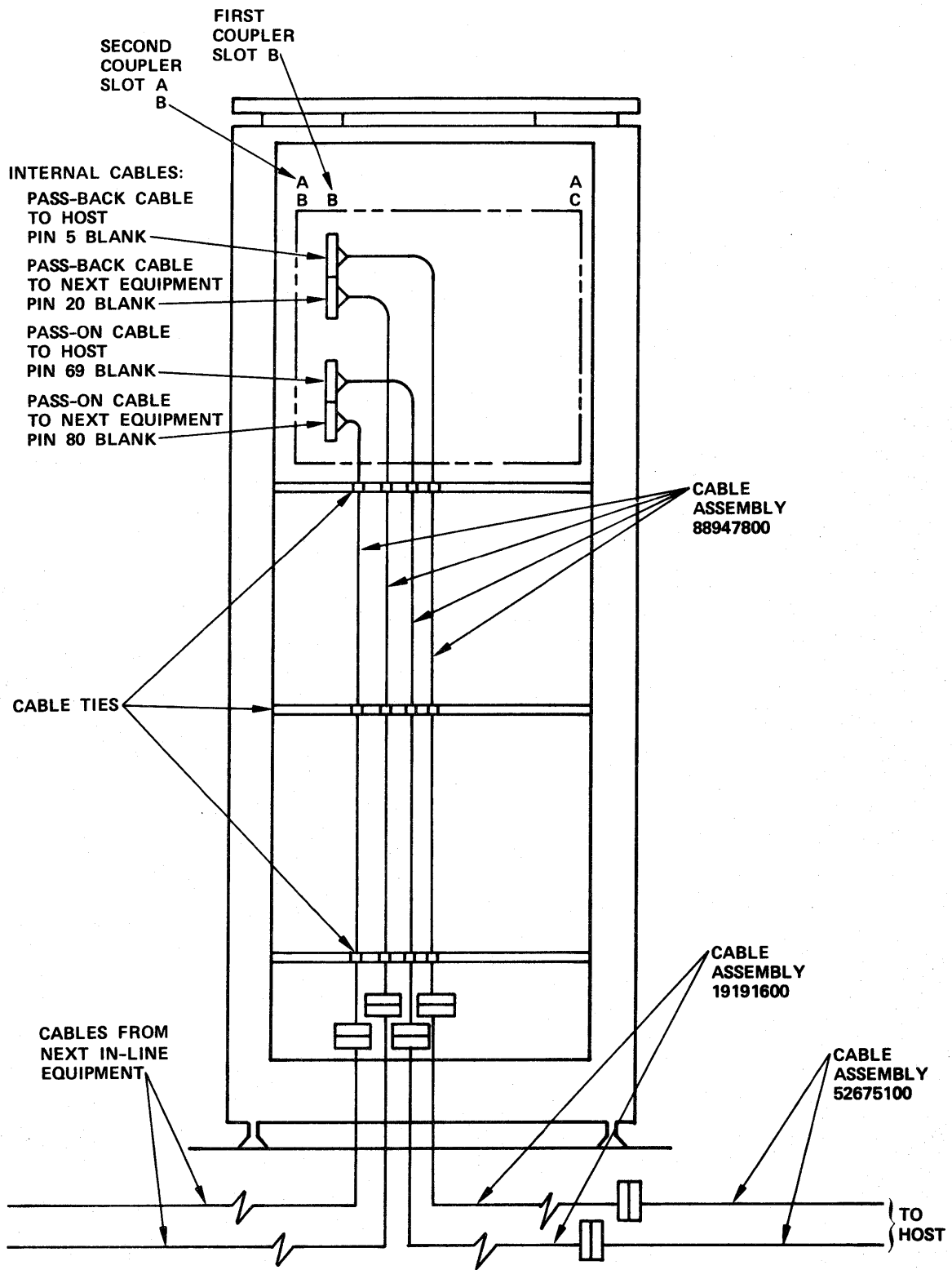
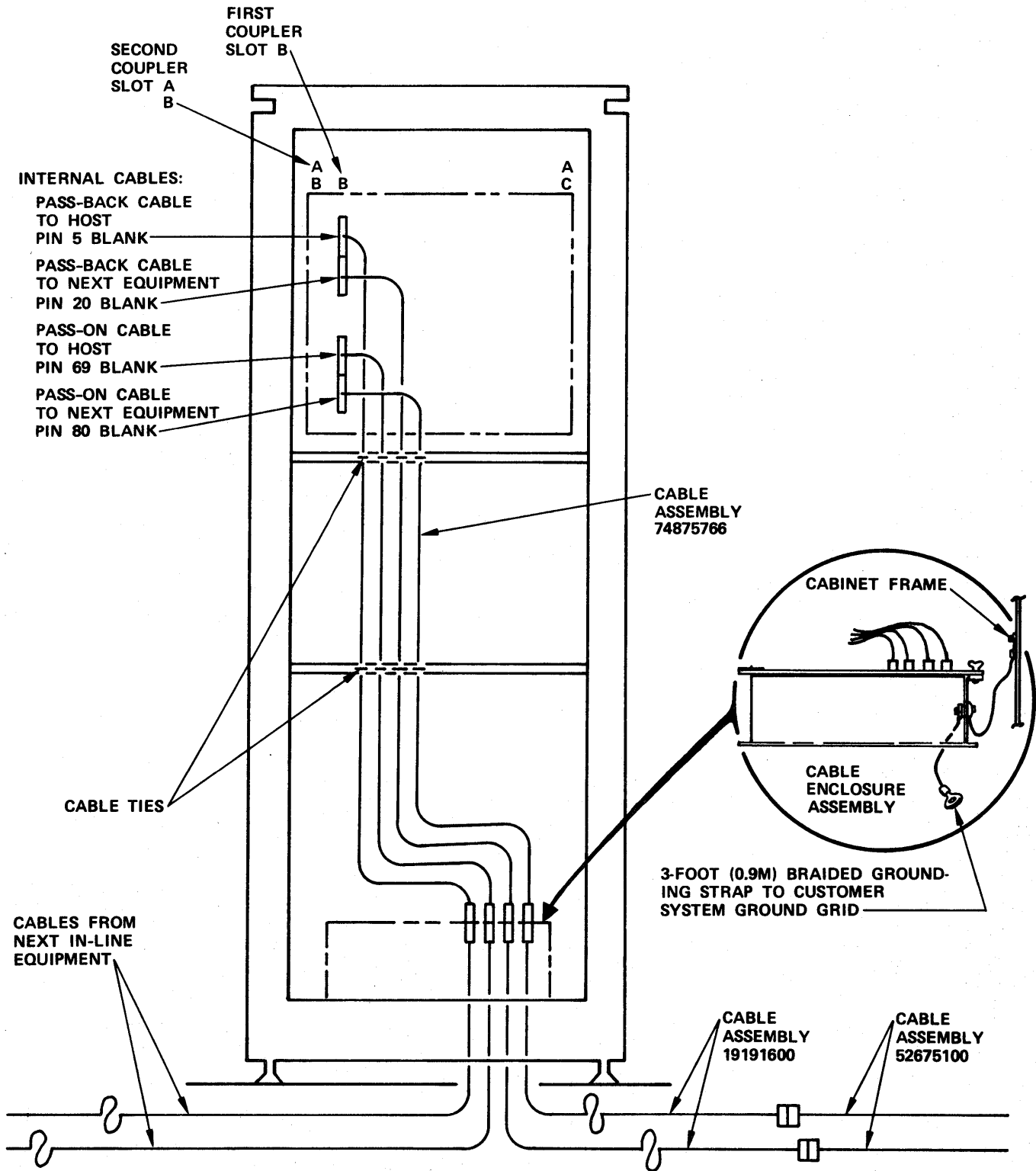


Figure 3-3. Ribbon Cables Installed



M-604

Figure 3-4. DY159-A Coupler Coaxial Cable Layout
(A Version Cabinet, Rear View)



M-605

Figure 3-5. DY159-B Coupler Coaxial Cable Layout (B Version Cabinet, Rear View)

CIRCUIT CARDS

1. Insert the two circuit cards into slots B and C of the card cage (figure 1-5). Continue insertion until connectors mate with connectors at rear of card cage.
2. If two couplers are to be installed, insert second coupler into slots AA and AB of card cage (figure 1-5). Continue insertion until tab connectors mate with connectors at rear of card cage.

COUPLER SELECT SWITCH

1. Refer to NPU program and determine which coupler address has been assigned to coupler 1.

2. Set coupler select switch S1 on coupler 1 (figure 2-3) to its assigned position: up for 2, down for 3.
3. If two couplers have been installed, set S1 of interface on coupler 2 to opposite position of S1 of interface on coupler 1.

CHECKOUT

After completing all installation procedures, perform subsystem diagnostics to check out the coupler. Refer to the NPU hardware maintenance manual for complete checkout procedures using the proper diagnostics.



The coupler temporarily stores data that is being transferred between the host and a terminal. At a precise time and under control of the host, it releases this data in the proper direction. The words input and output are always used in reference to the host. Thus output data travels from the host, through the coupler, to the processor, and eventually to a terminal. And input data comes from a terminal, eventually to the processor, through the coupler, and to the host.

This section contains descriptions of the circuits that make up the coupler. The theory of operation is divided into discussions of: the pass-on and pass-back block diagram; the coupler block diagram; and timing and control. Each circuit is discussed as a block within a block diagram. Detail circuit logic can be found on the logic diagrams of the two circuit cards: the synchronizer and the interface. A particular circuit can be located within the logic diagrams by referring to the block diagrams. A corner of each block contains the logic diagram sheet number. If the circuit is on the synchronizer, the number appears in the lower right-hand corner. If the circuit is on the interface, the number appears in the upper left-hand corner.

The distribution of signals to and from each circuit is shown on the block diagram. These signals are only described in this section when referring to their source or to their ultimate use. The number on the lines within the block diagram refer to the number of signals entering or leaving a particular block or circuit. Where no number is shown, only one signal is on that particular line.

To clarify the meaning of abbreviation, in the text and on logic diagrams, refer to the list of mnemonics in the appendix. Wherever a word or group of bits is described, bit zero is the least significant unless noted otherwise.

PASS-ON & PASS-BACK BLOCK DIAGRAM

The following paragraphs describe the functions of individual circuits within the pass-on and pass-back block diagram. These circuits form three major groups: the pass-on circuits, the pass-back circuits, and the clock circuits. To clarify the relationship of these circuits to one another, refer to figure 4-1.

PASS-ON CIRCUITS

Receivers, registers, and drivers constitute the pass-on circuits. The detail logic for all of these circuits is on synchronizer logic sheet 4. The pass-on cable to the host brings 19 lines into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the host into TTL compatible levels. A logic 1 from the host is a positive pulse that is 25 to 40 ns wide and 1.3 V in amplitude. A logic 0 is merely the absence of a pulse. The receiver sends the converted pulse to a catch register.

Catch Register

The catch register captures the pulse from the host to enable the coupler to operate over a wide range of pulse widths and pulse skew. The catch register is connected to a transfer register.

Transfer Register

When a $T70$ clock pulse occurs, the transfer register stores the signal for 100 ns, the time between clock pulses. During this time, the signal is made available to other coupler circuits and to a driver.

Only 18 of the 19 lines are made available to the other coupler circuits, as the coupler has no use for the parity signal. The coupler does use the 12 data lines and the 6 signals: active, inactive, full, empty, function, and master clear. These 18 lines plus the parity line are connected to drivers.

Driver

The driver converts the TTL level to the logic level compatible with the communication channel. A logic 1 is a positive pulse that is 35 ns wide and 1.4 V in amplitude. A logic 0 is merely the absence of a pulse. The driver is connected to the pass-on cable to the next equipment.

PASS-BACK CIRCUITS

Receivers, registers, drivers, and multiplexers constitute the pass-back circuits.

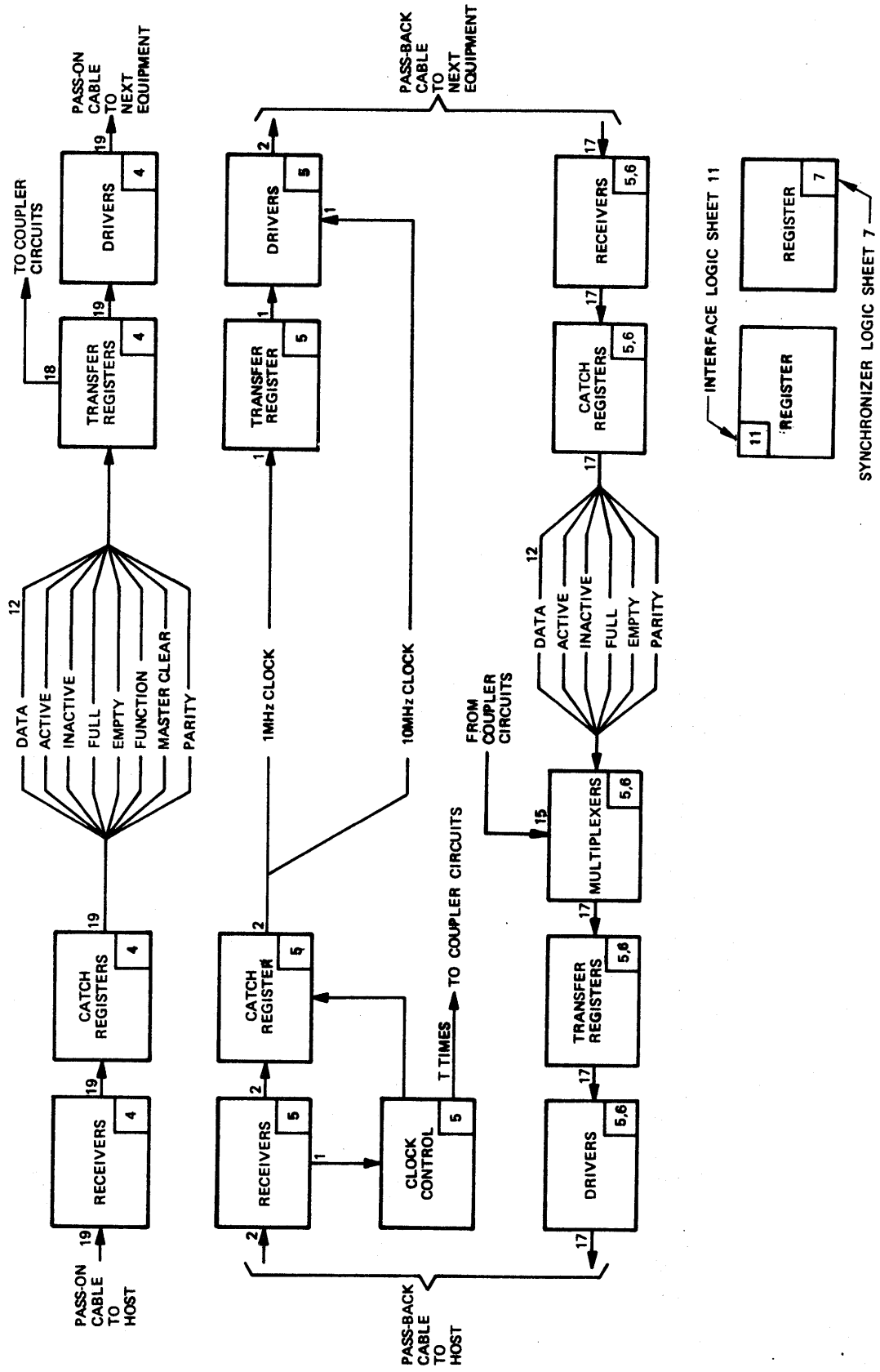


Figure 4-1. Pass-on and Pass-back Block Diagram

The pass-back cable to the next equipment brings 17 lines into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the next equipment into TTL compatible levels. A logic 1 from the next equipment is a positive pulse that is 25 to 40 ns wide and 1.3 V in amplitude. A logic 0 is merely the absence of a pulse. The receiver sends the converted pulse to a catch register.

Catch Register

The catch register captures the pulse from the next equipment to enable the coupler to operate over a wide range of pulse widths and pulse skew. The catch register is connected to a multiplexer.

Multiplexers

From the catch registers, the multiplexers receive 12 data lines and 5 signals: active, inactive, full, empty, and parity. From other coupler circuits, they receive 12 data lines and 3 signals: inactive, full, and empty.

The data lines from the catch registers are connected by the multiplexer to transfer registers unless the coupler is selected for communication by the host. In this case a SENDF signal causes the multiplexer to disconnect data from the catch registers and connect data from the coupler circuits to the transfer registers.

The multiplexers handle the signal lines differently. Only the equipment that is communicating with the host will have high signals. Therefore, the multiplexers select signals from the coupler circuits or the catch register by connecting the high signals to the transfer registers.

Transfer Register

When a T70 clock pulse occurs, the transfer stores the signal for 100 ns, the time between clock pulses. During this time, the signal is made available to a driver.

Driver

The driver converts the TTL level to the logic level compatible with the communication channel. A logic 1 is a positive pulse that is 35 ns wide and 1.4 V in amplitude. A logic 0 is merely the absence of a pulse. The driver is connected to the pass-back cable to the host.

CLOCK CIRCUITS

Receivers, registers, drivers, and clock control constitute the clock circuits. The detail logic for all of these circuits is on synchronizer logic sheet 5. The pass-back cable to the host brings two lines, a 10 MHz clock and a 1 MHz clock, into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the host into TTL compatible levels. The clock pulse from the host is a positive 1.3 V in amplitude and 35 ns wide. The receiver sends the converted pulse to a catch register. The receiver for the 10 MHz clock also sends the clock pulse to clock control.

Catch Register

The catch register captures the clock pulse to enable the coupler to operate over a wide range of pulse widths and pulse skew. The catch register for the 1 MHz clock is connected to a transfer register.

Transfer Register

When a $\overline{T70}$ clock pulse occurs, the transfer register stores the 1 MHz clock pulse for 100 ns, the time between $\overline{T70}$ clock pulses. During this time, the 1 MHz clock pulse is made available to a driver.

Driver

The driver converts the TTL level to the logic compatible with the communications channel. The converted clock pulse is a positive 1.4 V in amplitude and 35 ns wide. The driver is connected to the pass-back cable to the next equipment. Both the 1 MHz and the 10 MHz clocks are sent to the next equipment 70 ns after they arrive from the host.

Clock Control

Clock control provides timing signals or clocks for all coupler operations. These clocks are derived from the 10 MHz clock. One adjustable delay circuit and one fixed delay line split the 100 ns period of the 10 MHz clock into 5 ns intervals. At each one of these intervals which are called T times, a 10 MHz positive-going clock pulse of 25 ns duration may be derived.

Only a few of the T times are used in the coupler and some of these are inverted or negative-going clocks. Whenever a clock is inverted, 5 ns is added to its T time. Some of the clocks used in the coupler are T_0 , T_{40} , T_{90} , $\overline{T_0}$, $\overline{T_{35}}$, and $\overline{T_{70}}$.

There are two adjustments in clock control. Switch S5 provides for an adjustment of clock pulse width and a coarse adjustment of leading edge. Potentiometer R6 provides for a finer adjustment of the leading edge. Both of these controls are adjusted at the factory and should not be changed during installation. Clock pulse width is adjusted by setting to ON one of four S5 positions: A, B, C, or D. Leading edge is adjusted by setting to ON one of the other four S5 positions: E, F, G, or H.

COUPLER BLOCK DIAGRAM

The following paragraphs describe the functions of individual circuits within the coupler block diagram. These circuits form several major groups: the equipment address circuits; the memory address circuits; the data-to-memory circuits; the memory circuits. To clarify the relationship of these circuits to one another, refer to figure 4-2. This figure and the pass-on and pass-back block diagram contain all of the circuits that make up the coupler.

EQUIPMENT ADDRESS CIRCUITS

A decoder, 4 switches, a converter, and the select control constitute the equipment address circuits. The detail logic for all of these circuits is on synchronizer logic sheet 7. Circuit functions are shown on figure 4-3. The pass-on circuits send a function signal and 3 data lines to the decoder.

Decoder

From the transfer registers, the decoder receives the function signal and the 3 data lines that carry the equipment address. These lines, PO09X through PO11X, are decoded from binary to decimal. The 8 decimal outputs, 0 through 7, of the decoder are connected respectively to the 8 positions of each equipment switch. The one line that corresponds to the correct equipment address will have a signal transition from 1 to 0 when the function signal POFNX is high.

Equipment Switches

The four equipment switches have each been preset prior to installation. If any of them is set to the equipment address received from the decoder, this information is sent to the converter and select control.

Converter

If the converter receives a signal from the equipment switches, it converts that signal from decimal into binary. This 2-bit equipment address is sent to the F register to become signals FR09 and FR10. The number,

0 to 3, contained in these two bits correspond directly to the number assigned to one of four sets of terminals connected to the NPU. It is these four sets of terminals that are referred to as internal equipment. Address switches 1 through 4 are respectively related to internal equipments 0 through 3.

Select Control

The select control generates signal CSEL if the coupler has been selected to communicate with the host. A signal from any equipment switch would indicate that fact. Signal CSEL is sent to the F register to become signal FR11, and to coupler control where it enables the decoding of the function command.

MEMORY ADDRESS CIRCUITS

The F register, two ROMs, the counter, the MAB multiplexer, and 15 Y-line inverters constitute the memory address circuits. The pass-on circuits send 9 data lines to the F register. The equipment address circuits send an additional three delta lines to the F register.

F Register

The F register stores a 12-bit function word slightly modified from the one received from the host (figure 2-4). The equipment address circuits have converted the 3-bit equipment number, which was in bits 9 through 11, to a 2-bit equipment address. These two bits stored in bits 9 and 10, and the CSEL signal is stored in bit 11. The F register sends one or more of its bits, FR00 through FR11, to the ROMs, the counter, coupler control, and the MH register.

The ROMS

The two ROMs store starting locations for the coupler buffer. One ROM is for normal operation, and the other ROM is for maintenance. Each ROM depends on bits from the F register to determine which starting address it sends to the counter.

The operational ROM provides the starting address, location 0, for one of eight areas in the coupler buffer. Four of these areas store output data (from the host), and the other four areas store input data (from the processor). Two areas, input and output, are assigned to each equipment. Bits FR09 and FR10 select an equipment address from 0 through 3. Whether an input or an output area for that equipment is selected depends on the command in bits FR00 and FR01. Command 1 selects an output area; commands 2 and 3 select an input area. Figure 4-4 illustrates the eight areas addressed by the operational ROM and the signals required by the ROM to send an address to the counter. Each area in the coupler buffer contains 64 word locations.

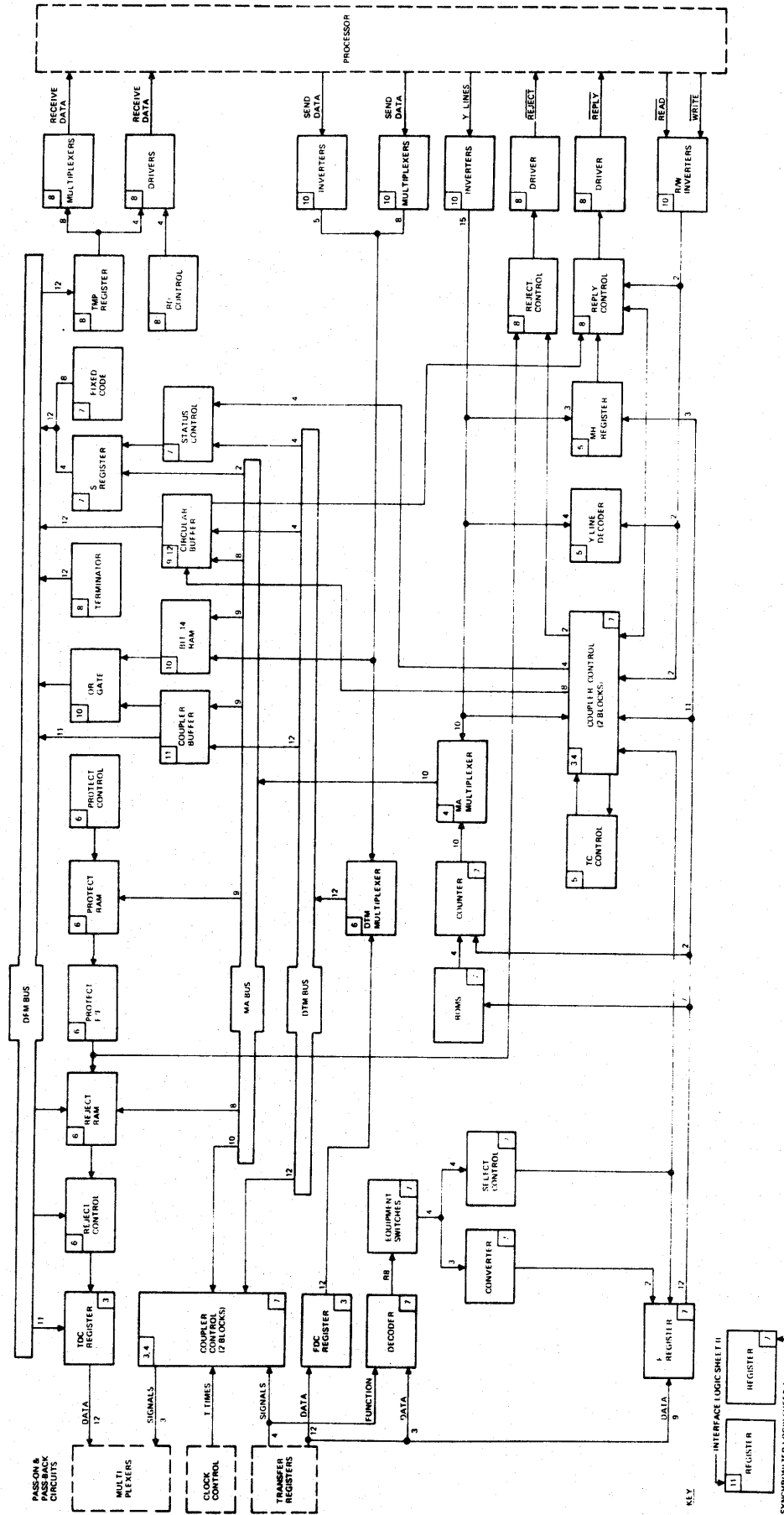


Figure 4-2. Coupler Block Diagram

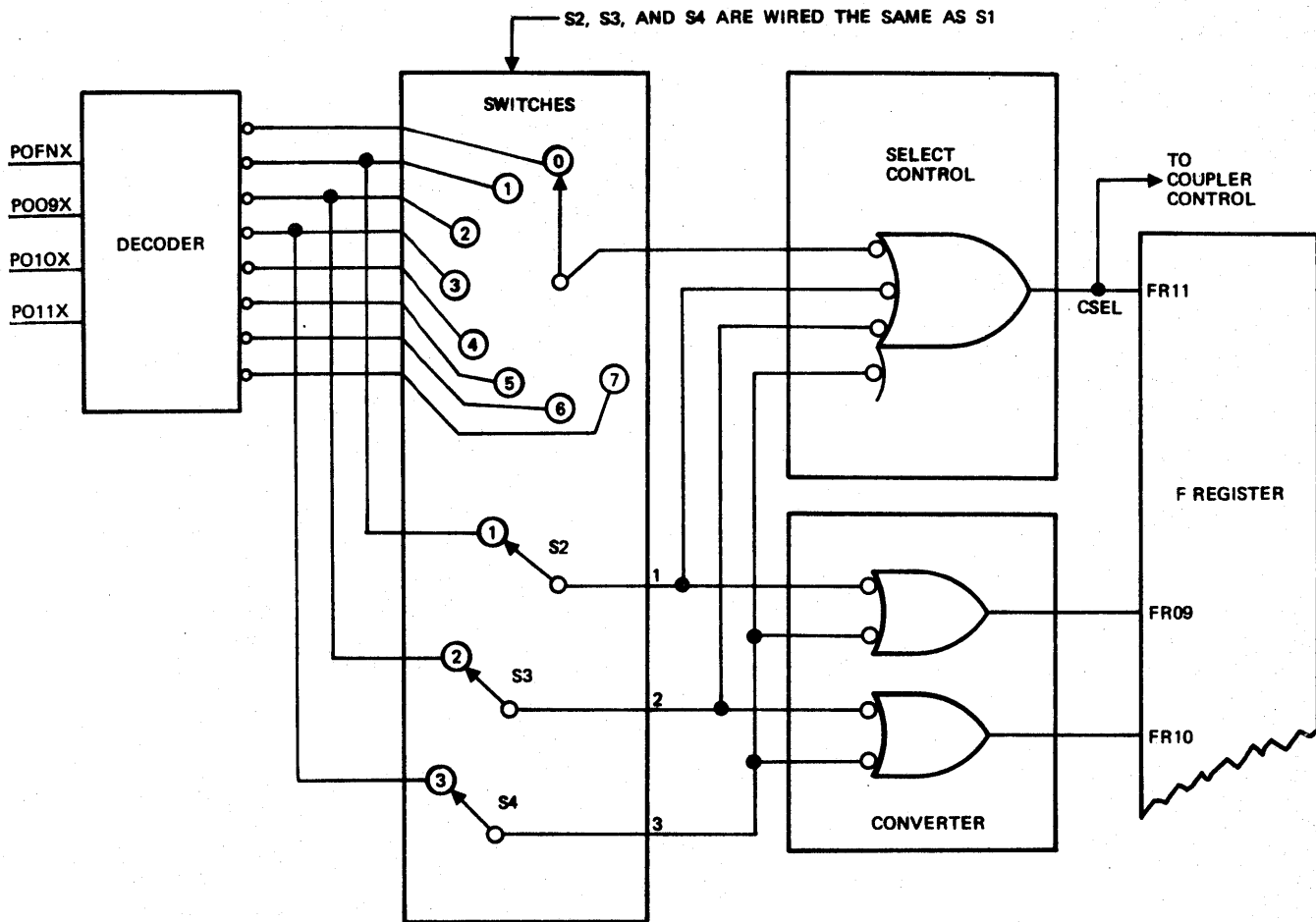


Figure 4-3. Equipment Address Circuits

The maintenance ROM provides the starting address, location 0, for one of 32 bytes in the coupler buffer. For the purpose of running diagnostics, the 128 word locations for each equipment have been divided into bytes of 16 locations each. These bytes are numbered 0 through 7. Bits FR09 and FR10 select an equipment address from 0 through 3. Bits FR03, FR04, and FR05 select a byte from 0 through 7. Figure 4-5 illustrates the 32 bytes addressed by the maintenance ROM and the signals required by the ROM to send an address to the counter.

Counter

The counter contains the address of data to be transferred into or out of the coupler buffer. This 10-bit binary counter parallel loads the starting address received from the ROM and is incremented following each read

or write command from the host. Note that output data is a write command; also note that input data and send status are both read commands. The counter sends its 10 bits, MAC00 through MAC09, to the MAB multiplexer (figures 4-4 and 4-5).

MAB Multiplexer

The MAB multiplexer selects one of two addresses to be sent to the MA bus. One of these addresses is stored in the counter. The other address is on the Y lines from the processor. When the host accesses the coupler, the MAB multiplexer selects the address in the counter. When the processor accesses the coupler, the MAB multiplexer selects the address on the Y lines.

Each of the two address sources supply 10 bits of information to the MAB multiplexer.

A. ADDRESSED AREAS OF THE COUPLER BUFFER

EQUIPMENT 0	EQUIPMENT 1	EQUIPMENT 2	EQUIPMENT 3
OUTPUT	OUTPUT	OUTPUT	OUTPUT
EQUIPMENT 0	EQUIPMENT 1	EQUIPMENT 2	EQUIPMENT 3
INPUT	INPUT	INPUT	INPUT

NOTE Each area contains locations 0-63.

B. REQUIRED SIGNALS FOR ADDRESSING

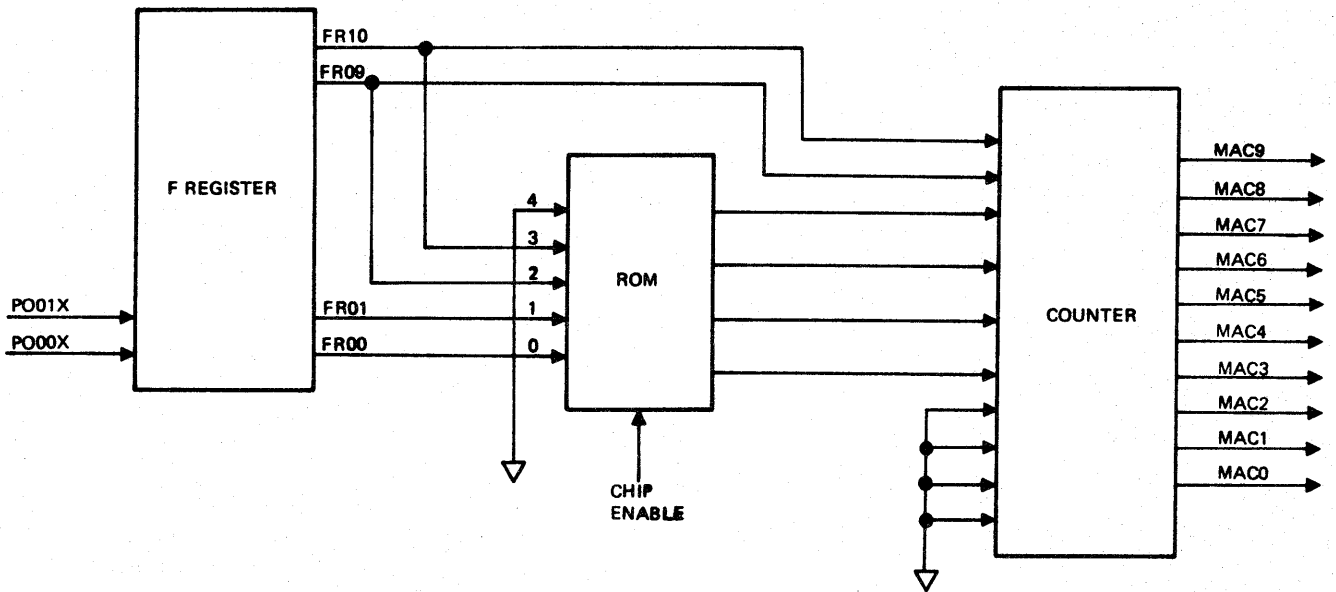


Figure 4-4. Operational ROM

A. ADDRESSED BYTES OF THE COUPLER BUFFER

EQUIPMENT: 0	1	2	3
↓	↓	↓	↓
BYTE 0	BYTE 0	BYTE 0	BYTE 0
BYTE 1	BYTE 1	BYTE 1	BYTE 1
BYTE 2	BYTE 2	BYTE 2	BYTE 2
BYTE 3	BYTE 3	BYTE 3	BYTE 3
BYTE 4	BYTE 4	BYTE 4	BYTE 4
BYTE 5	BYTE 5	BYTE 5	BYTE 5
BYTE 6	BYTE 6	BYTE 6	BYTE 6
BYTE 7	BYTE 7	BYTE 7	BYTE 7

NOTE: EACH BYTE CONTAINS LOCATIONS 0-15.

B. REQUIRED SIGNALS FOR ADDRESSING

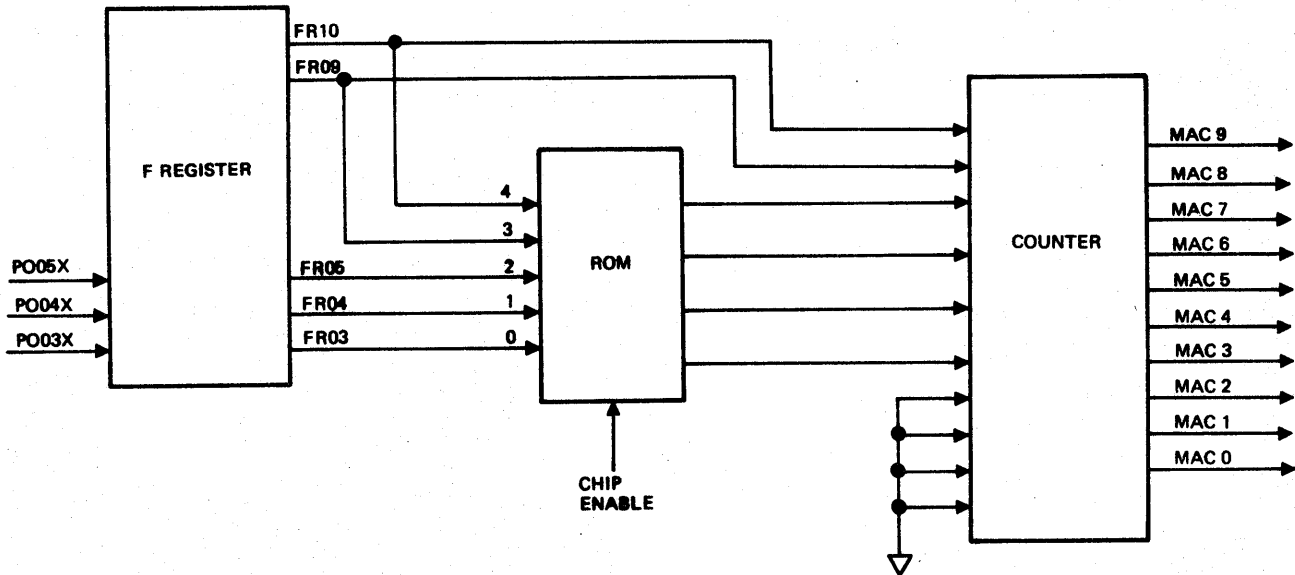


Figure 4-5. Maintenance ROM

The 10 address bits that are sent to the MA bus are shown in figure 4-6. Bit zero is the least significant. From the MA bus this address, MAB00 through MAB09, is distributed to the: reject RAM, protect RAM, bit 14 RAM, S register, coupler control, coupler buffer, and circular buffer. When the circular buffer is selected, the MAB lines contain data rather than an address. Figure 4-7 shows all uses of the MAB lines.

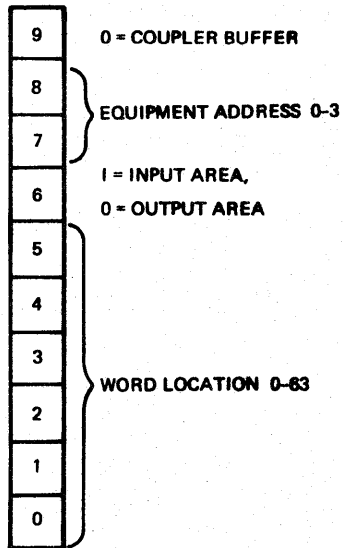


Figure 4-6. MAB Address Format

Y Lines

The Y lines bring addressing information from the processor into the coupler. These 15 Y-bits, $\bar{Y}0$ through $\bar{Y}14$, are sent directly to inverters. Bit zero is the least significant.

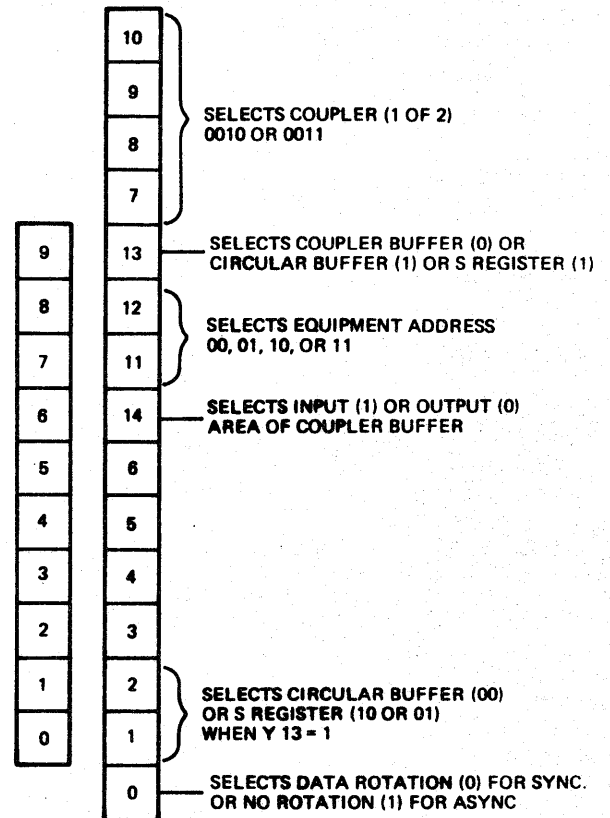


Figure 4-7. Uses of MAB and Y Lines

Inverter

The inverter receives a Y bit, inverts it, and sends it to one or more of four destinations. Ten Y bits go directly to the MAB multiplexer. Three of these same ten bits are used by the MH register. Coupler control uses Y0, and the decoder uses Y7 through Y10 (figure 4-7).

DATA TO MEMORY CIRCUIT

The FDC register, the DTM multiplexer, and the send data inverters and multiplexers constitute the data-to-memory circuits. The pass-on circuits send 12 data lines to the FDC register.

FDC Register

The FDC register holds 12 bits of data from the host. These 12 bits, P000X through P011X, come directly from the transfer registers. These same 12 bits change to FDC0 through FDC11 before they are sent to the DTM multiplexer.

DTM Multiplexer

The DTM multiplexer selects one of two sets of data to be sent to the DTM bus. One set of data is held in the FDC register. The other data is on the FMP lines from the processor. When the host accesses the coupler, the DTM multiplexer selects the data in the FDC register. When the processor accesses the coupler, the DTM multiplexer selects the data on the FMP lines. Each of the two data sources supply 12 bits of information to the DTM multiplexer. The 12 data bits that are sent to the DTM bus are DTM00 through DTM11.

FMP Lines

The FMP lines do not bring data directly from the processor but via inverters and multiplexers. The SD lines from the processor bring the data into the coupler. SD bits 1 through 8 go to multiplexers; 9 through 12 and 15 go to inverters.

Inverters

The inverters receive SD09 through SD12 and SD15, invert each of these data lines, and send FMP08 through FMP11 to the DTM multiplexer. Note that the FMP data bits are renumbered by subtracting one from the number of each corresponding SD bit. Bit SD15 is inverted and sent to the bit 14 RAM.

Multiplexers

The multiplexers either send the data on the SD lines directly to the DTM multiplexer or rotate the data before sending it. See

figure 4-8. Whether bits SD01 through SD08 are rotated or not depends on whether or not the host is communicating with an asynchronous terminal. The selection of direct data or rotated data is controlled by signal Y0.

MEMORY CIRCUITS

The coupler buffer, the bit 14 RAM, the circular buffer, the protect RAM, and the reject RAM constitute the memory circuits. With the exception of the circular buffer, each of these circuits receive an address from the MA bus.

Coupler Buffer

The coupler buffer is a random access memory with capacity for 512 12-bit words. It can be addressed by the host or by the processor. For the purpose of addressing, the coupler buffer is divided into 8 areas: one input area and one output area for each of 4 equipments (figure 4-4). Each of the 8 areas contain 64 word locations.

The 9 MAB bits address one of the 512 locations in the coupler buffer. Then the 12 bits of data on the DTM bus may be written into the addressed location and stored until needed. Or data may be read from the selected location and sent to the DFM bus. Data from the coupler buffer to the DFM bus is contained in bits DFM0 through DFM9 and bit DFM11. An additional bit, CBM10, is ORed with the CBM14 to become bit DFM10.

When diagnostics are being performed on the NPU, the coupler buffer is divided into 32 bytes: 8 bytes for each of 4 equipments (figure 4-5). Each of the 32 bytes contain 16 word locations.

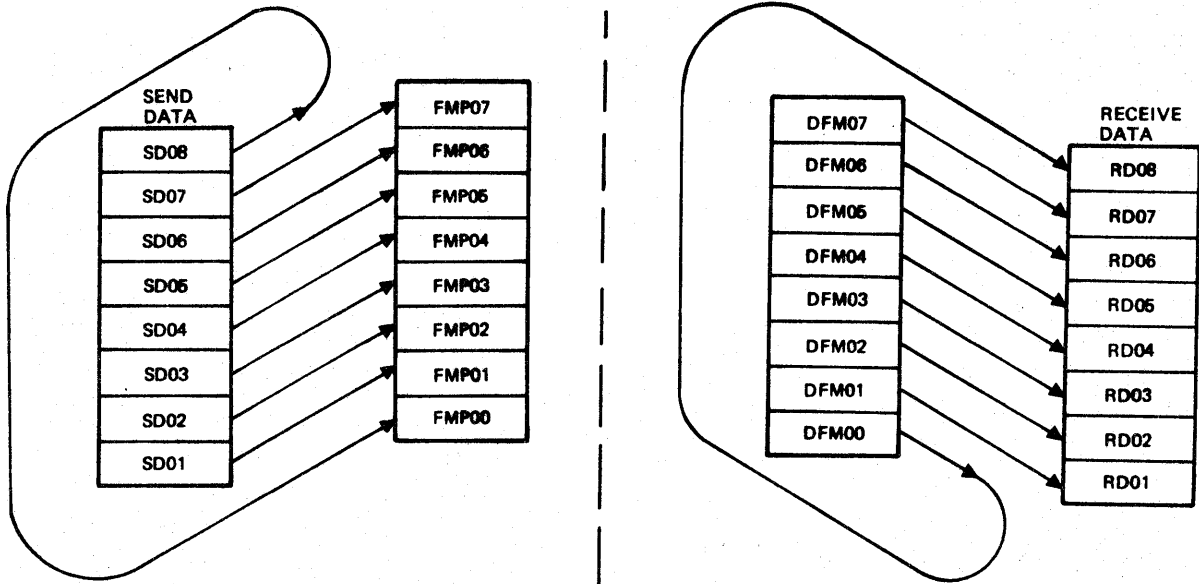
Bit 14 RAM

The bit 14 RAM is a random access memory with capacity for 512 single bits. It receives the result of ANDing signals SD15 and MPWC. This result is written into the location addressed by the 9 MAB bits. When data is read from the bit 14 RAM, signal CBM14 is sent from the selected location to an OR gate where it is ORed with signal CBM10. The resultant signal DFM10, is sent to the DFM bus.

Circular Buffer

The circular buffer is a random access memory with capacity for 256 12-bit words. It is addressed by the 8 CBA bits from coupler control. Figure 4-9 shows a partial block diagram of coupler control. The CBA lines originate in one of two counters selected by the CBA multiplexer. Both counters are returned to zero by the processor during an initialization process. After the host

A. ROTATE MODE FOR ASYNCHRONOUS TERMINALS



B. DIRECT MODE FOR SYNCHRONOUS TERMINALS

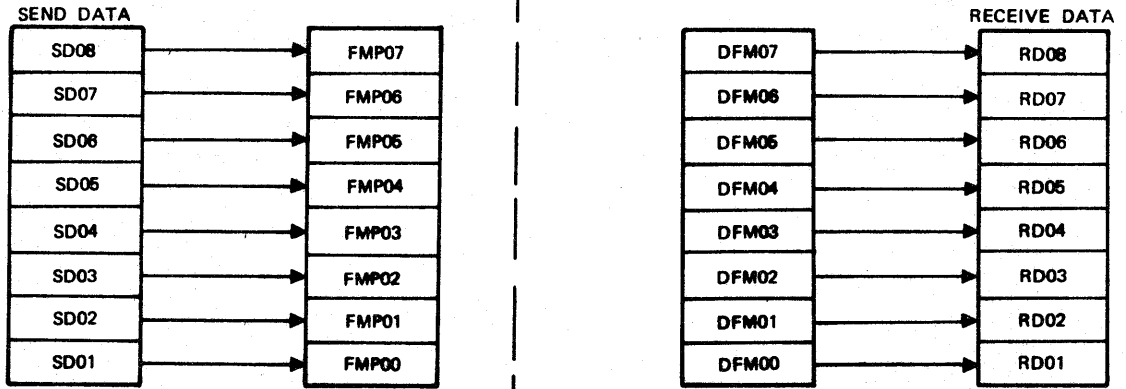


Figure 4-8. Send and Receive Data Modes

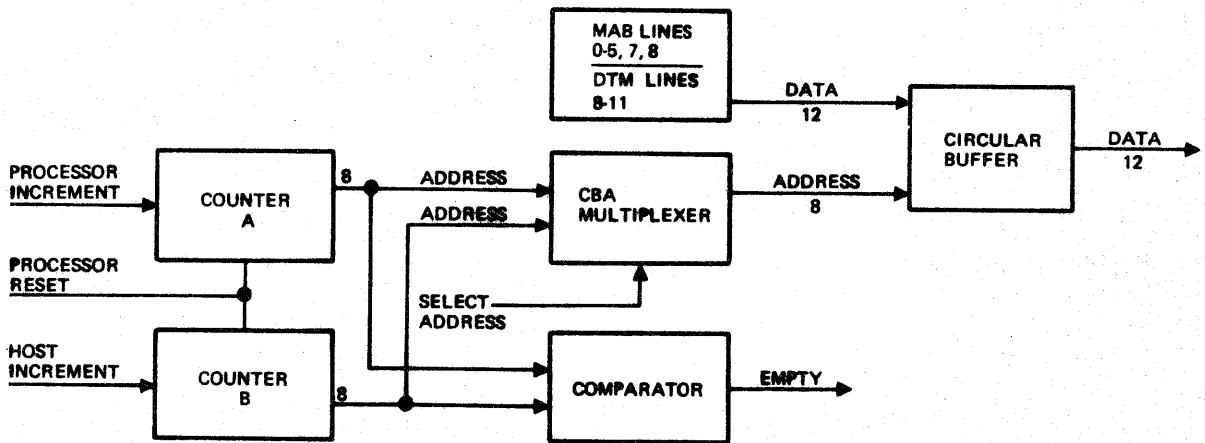


Figure 4-9. Signals of Circular Buffer

writes into the circular buffer, counter A is incremented. After the processor reads the output data, counter B is incremented. Under the direction of memory cycle control, the CBA multiplexer selects one of these counters as the source for an address. A comparator determines whether the circular buffer is full or empty and sends this information to the processor.

The 12 data bits received by the circular buffer come from the MAB and DTM lines. MAB lines 0 through 5 and 7 and 8 locate the area of the coupler buffer that has output data being written into it (figure 4-7). DTM lines 8 through 11 are I/O control bits. The format of the data bits in the circular buffer is shown in figure 4-10.

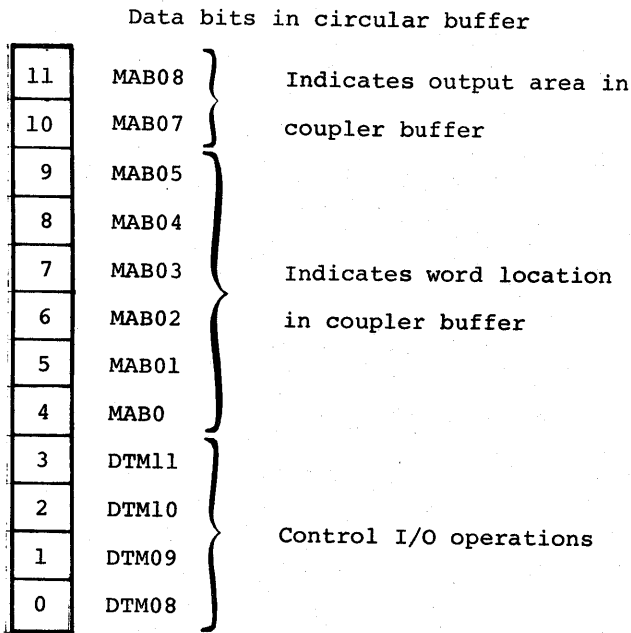


Figure 4-10. Word Format in Circular Buffer

Protect RAM

The protect RAM is a random access memory with capacity for 512 single bits. Whenever data is written into the coupler buffer, signal PROT is written into the protect RAM location addressed by the 9 MAB bits. This signal is generated in protect control. From the protect RAM signal PROT is used to set the protect flip-flop, which then sends signal PROTF to the reject RAM.

Reject RAM

The reject RAM is a random access memory with capacity for 256 single bits. When output data is written into the coupler buffer, signal PROTF is written into the

reject RAM location addressed by the 8 MAB bits. Note that MAB06 is not needed. During a read cycle by the host, the reject signal in the selected location is sent to reject control. There it is ORed with signal DFM8, and the resultant signal, DFM8M, is sent to the TDC register.

DATA FROM MEMORY CIRCUITS

The RCD register, the S register, the TMP register, a terminator, RD control, and receive data multiplexers and drivers constitute the data from memory circuits. The DFM bus sends 11 lines of data to the TDC register. An additional line of data is sent from reject control.

TDC Register

The TDC register stores a 12-bit word that is to be transferred to the host. Its immediate destination is the multiplexers in the pass-back circuits. These 12 bits are TDC00 through TDC11. The TDC register receives its word from one of two sources: the coupler buffer or the S register.

S Register

The S register stores 4 bits of the status word: bits 0, 1, 4 and 5 (figure 2-5). It has four sections which correspond to the four equipments, 0 through 3. When a send status command is received from the host, status control selects the proper section of the S register. The pertinent 4 bits are then sent to the DFM bus. The other 8 bits that make up the status word are a fixed code.

The processor can also access the S register. A request for status from the processor is handled in the same manner as one from the host. In this case the destination of the status word would be the TMP register.

TMP Register

The TMP register stores a 12-bit word that is to be transferred to the processor. Its immediate destination is the multiplexers and drivers for the receive data lines. The TMP register receives its word from one of three sources: the circular buffer, the coupler buffer, or the S register.

Drivers

The drivers receive the upper 4 bits from the TMP register and the 4 upper most bits of the RD lines from driver control. Each driver inverts its data bit and sends it to the processor on an RD line. The 8 bits from the drivers are RD09 through RD16.

Multiplexers

The multiplexers either send the data directly out on the RD lines or rotate the data before sending it (figure 4-8). Whether bits RD01 through RD08 are rotated or not depends on whether or not the host is communicating with an asynchronous terminal. The selection of direct data or rotated data is controlled by signal Y0.

Terminators

The DFM bus is terminated through resistors to plus five volts at the terminator.

CONTROL CIRCUITS

The coupler control, TC control, the Y-line decoder, the MH register, reject control and driver, reply control and driver, and the R/W inverters constitute the control circuits. Most of the operations that take place in the coupler are controlled by circuitry of the coupler control.

Coupler Control

Coupler control receives T times from clock control, signals from transfer registers and Y lines, and several other signals from within the coupler. With these control and timing signals, coupler control establishes the direction of data flow between the host and the processor.

Either the processor or the host may request a memory cycle or both requests may come simultaneously. In any case, only one is allowed at one time. In the case of simultaneous requests, the processor must wait up to 450 ns until the host's request has been serviced. When one of these requestors is allowed access, coupler control sends a signal to the MAB and DTM multiplexers that selects the proper source of address and data.

TC Control

TC control counts the number of locations read in the coupler buffer until the maximum is reached. When the terminal count is complete for that particular equipment, signal TCC is generated. See figure 4-11. A counter supplies inputs to two gates: a 64 count and a 16 count. One gate is enabled by an operational read from the host. The other gate is enabled by a maintenance read from the host. When 64 locations have been read during normal operations, the TCC flip-flop is set and signal TCC is generated. Reading 16 locations during diagnostics causes the setting of the TCC flip-flop. Signal TCC clears the F register and inhibits write enable to the coupler buffer. The counter is incremented by signal MACI which also increments the counter in memory address circuits. The counter is cleared by signal TCC or by a new function word.

Y-Line Decoder

The Y-line decoder receives signals Y07 through Y10 and decodes them to select one of two couplers. The coupler select switch has been set to the position assigned by the processor. This position is either address 2 or address 3. If the hexadecimal address on the Y lines is the same as the address of the positioned switch, this coupler is selected for processor operations. The presence of a write or read signal along with the proper address indicates that the processor desires communication.

R/W Inverters

An inverter receives the read signal from the processor, inverts it, and sends it to coupler control and other circuits. An identical inverter treats the write signal in an identical manner.

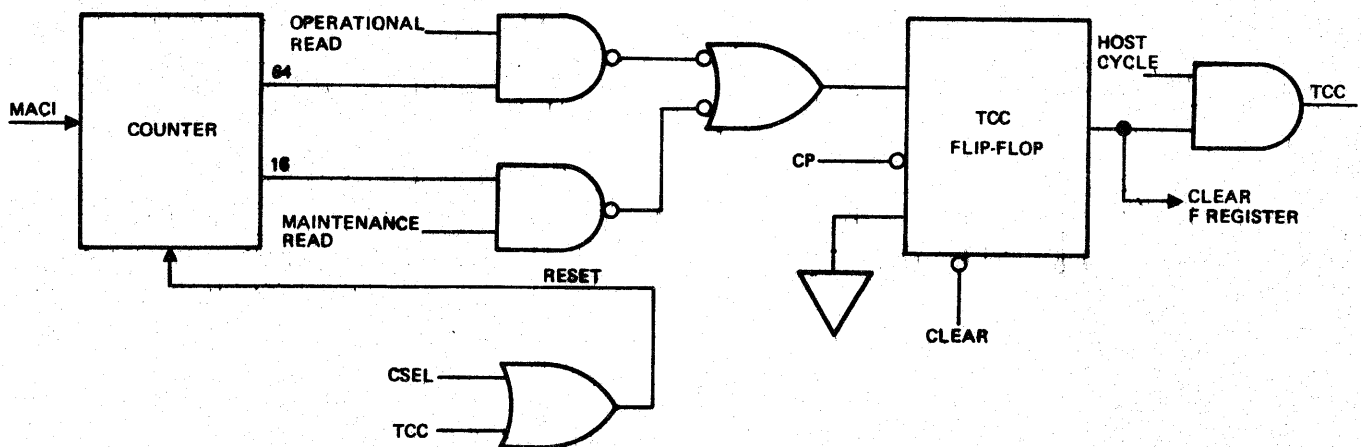


Figure 4-11. Terminal Count Logic

MH Register

The MH register stores signal FR08 in one of four sections that correspond to the four equipments. During diagnostics this signal holds the coupler buffer for maintenance tests (figure 2-4). The state of the MH register is sent to reply control where a negative reply is generated in response to an access request from the processor.

Reply Control

Reply control answers a request from the processor with either a positive or a negative reply. The types of requests are: read the coupler buffer, write in the coupler buffer, write in the status register, and read the circular buffer. Reply control sends a negative response to a read or write request for the coupler buffer when the MH bit is set. The processor also gets a negative response to a request to read the circular buffer when the circular buffer is empty. Signal REPLY is sent through a driver to the processor.

Controlware interprets the RD lines to determine the reply from the coupler. When a negative response is sent, all 16 RD lines are at the 0 level. This is read as a hexadecimal 0000. When a positive response is sent, a hexadecimal Fxxx is on the RD lines: RD13 through RD16 are set to the 1 level.

Reject Control

Reject control contains the reject flip-flop which is set during a processor write request if the protect bit is set. The state of the reject flip-flop is sent through a driver to the processor as signal REJECT.

MEMORY CYCLE FLOW DIAGRAM

The following paragraphs describe the sequence of events within the memory cycle flow diagram. These events form four major groups: processor write cycle, processor read cycle, host write cycle, and host read cycle. To clarify the relationship of these events to one another, refer to figure 4-12.

To better understand the overall operation of the coupler, a short review is given here of some pertinent facts. The coupler is a slave to the programs of the host and the processor. Its task is to transfer data between the host and the processor upon command. The coupler and the processor are merely parts of the NPU which enables the host to communicate with up to 256 terminals. Up to 64 of these terminals are assigned to one of four equipments. When data is transferred, it is done a

block at a time. That is, one character from or to each of 64 terminals is transferred in a block of data.

Either the processor or the host may request a memory cycle or both requests may come simultaneously. In any case only one is allowed at one time. In the case of simultaneous requests, the processor must wait until the host's request has been serviced. The memory that is being accessed is the coupler buffer and related memories within the coupler.

PROCESSOR WRITE CYCLE

From the start of the flow diagram, the first decision is whether or not the host or the processor is selecting. If the answer is neither, then return to start. If the answer is yes, it must be decided which of the two is selecting to communicate. Assume for now that the processor selects the coupler.

Do negative response conditions exist? If the answer is yes, send a hexadecimal 0000 back to the processor and return to start. If the circular buffer is not empty and there is not a maintenance hold on the coupler, then answer will be no. The processor then requests a memory cycle.

The processor may be locked out from accessing the coupler buffer because the host is being serviced. If it is, it will continually ask whether it is locked out until the answer is no. Then the memory cycle will start and the host will be locked out. The next decision is whether a read or write cycle is desired. Assume for now that the processor requests a write cycle.

Is the S register selected? Does the processor wish to store status? If the answer is yes, the data on the FMP lines are stored in the S register. If the answer is no, another decision is made.

Is the protect flip-flop set? If the data character previously written into memory has not been ready by the host, the answer will be yes. This data must be protected; therefore, further writing is inhibited at this point in time. A reject is sent to the processor, and host access to memory is unlocked. If the protect flip-flop is not set, the data on the FMP lines are stored in input areas of the coupler buffer. Host access is then unlocked, and a positive reply of hexadecimal Fxxx is sent to the processor.

PROCESSOR READ CYCLE

Is a read cycle or a write cycle desired by the processor? Assume for now that the processor requests a read cycle. The circular buffer is read. Then the output

areas of the coupler buffer are read and loaded into the TMP register. After memory has been read, the processor clears both the coupler buffer and the protect RAM. Host access is then unlocked, and a positive reply of hexadecimal Fxxx is sent to the processor.

HOST WRITE CYCLE

Is it the host or the processor that is selecting? Assume for now that the host is selecting. Is there a match between the equipment number sent by the host and the equipment number assigned to the coupler? If the answer is no, ignore the host and return to start. If the answer is yes, load the F register with the function word and send an inactive signal back to the host. Also decode the function word and load the MA counter with a memory address. The next decision is whether a read or write cycle is desired. Assume for now that the host requests a write cycle.

Has the host sent an active signal and a full signal? If the answer is no, has the host sent an inactive signal signifying the end of communications? If an inactive signal has been received, reset the F register and go back to start. If an inactive signal has not been received, recheck for active and full signals. If these two signals are present, load data into the FDC register and send an empty signal to the host. The host will then request a memory cycle.

The host may be locked out from accessing the coupler buffer because the processor is being serviced. If it is, it will continually ask whether it is locked out until the answer is no. Then the memory cycle will start and the processor will be locked out.

The next question is whether or not the protect flip-flop has been set. If the data character previously written into memory has not been read by the processor, the answer will be yes. This data must be protected; therefore, further writing is inhibited at this point in time. A reject is sent to the host, and processor access to memory is unlocked. If the protect flip-flop is not set, data is written into the output areas of the coupler buffer. Information is also written into the circular buffer, and the counter of the circular buffer is incremented. The MA counter is then incremented, and the processor access to memory is unlocked.

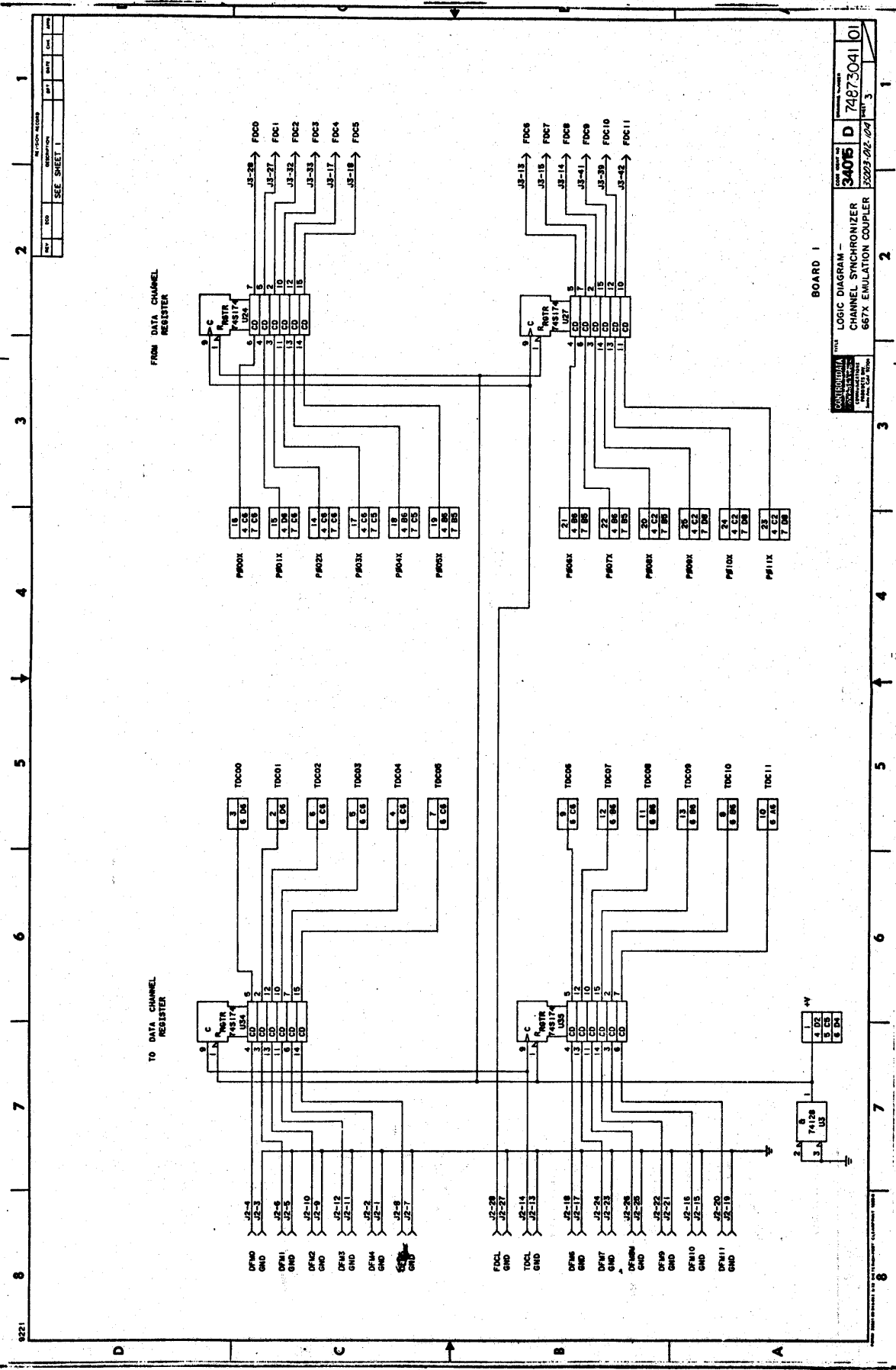
HOST READ CYCLE

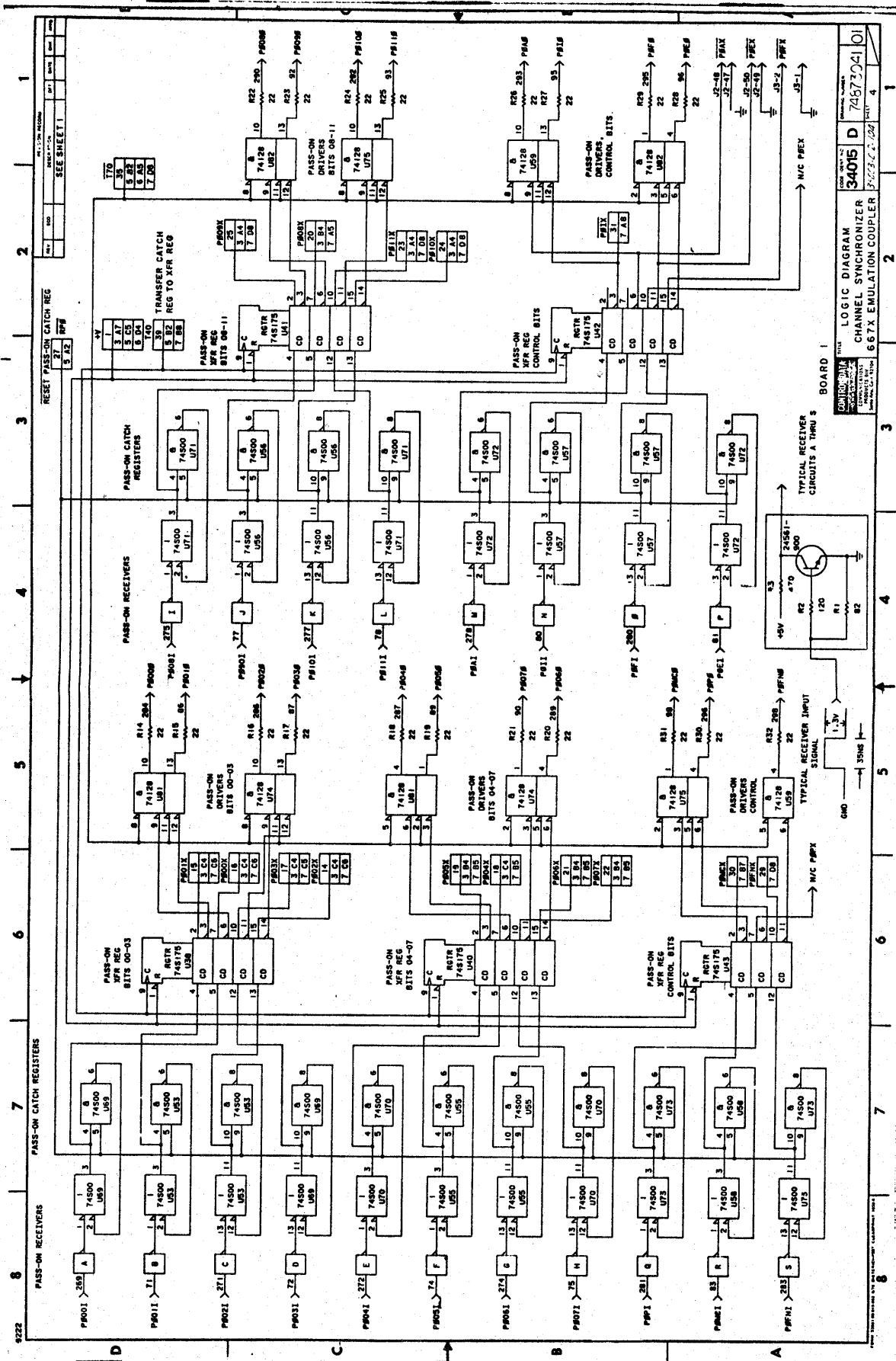
Is a read cycle or a write cycle desired by the host? Assume for now that the host requests a read memory cycle. If the host is not locked out, a memory cycle will start and the processor will be locked out. Data from an input area of the coupler buffer or status from the status register will be loaded into the TDC register. After memory has been read, the host clears both the coupler buffer and the protect RAM. Processor access to memory is then unlocked.

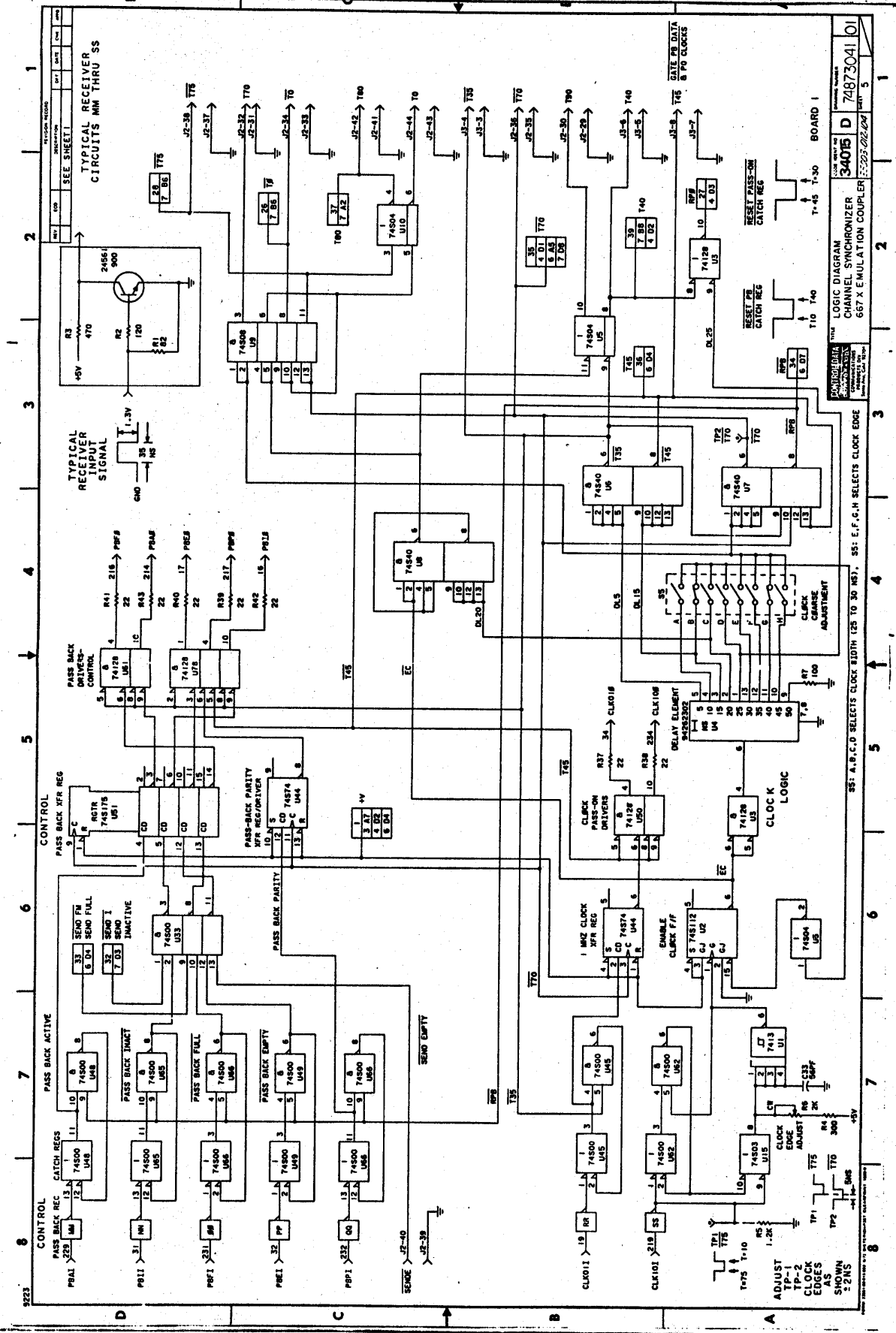
Has the host sent an active signal and an empty signal? If the answer is no, has the host sent an inactive signal signifying the end of communications? If an inactive signal has been received, reset the F register and go back to start. If an inactive signal has not been received, recheck for active and empty signals. If these two signals are present, send a full signal to the host and increment the MA counter. The memory cycle request will then be serviced as in the previous paragraph.

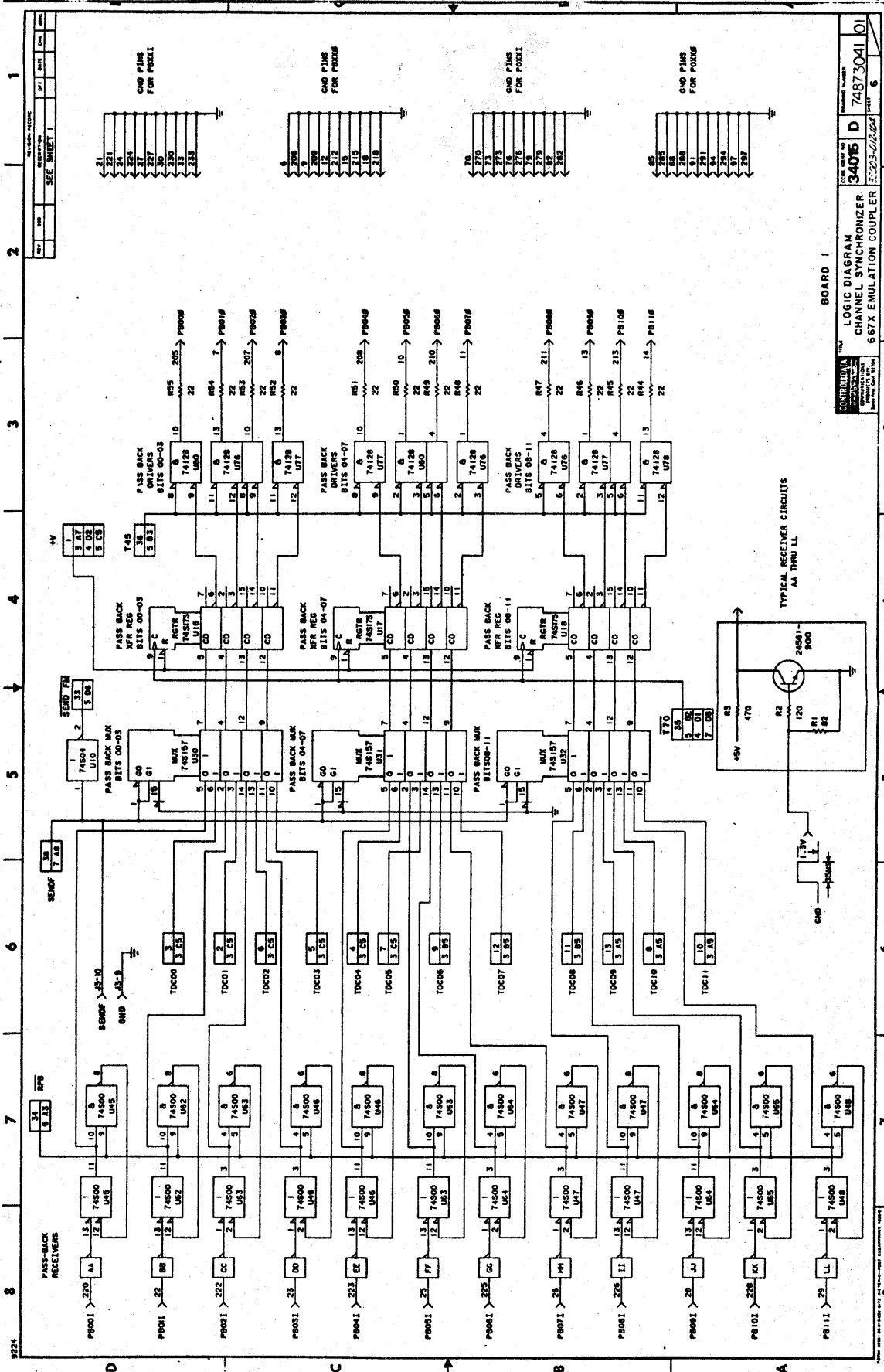
There are two versions of the coupler. Logic diagrams for both versions are included in this section. When using the diagrams as a trouble-shooting aid, verify that the component locators on the circuit card agree with those on the logic diagram.

The logic diagram for the first version of the synchronizer is drawing number 74850100. The logic diagram for the first version of the interface is drawing number 74846100. The second version of the coupler is logically shown in drawings numbered 74850101 and 74846101.

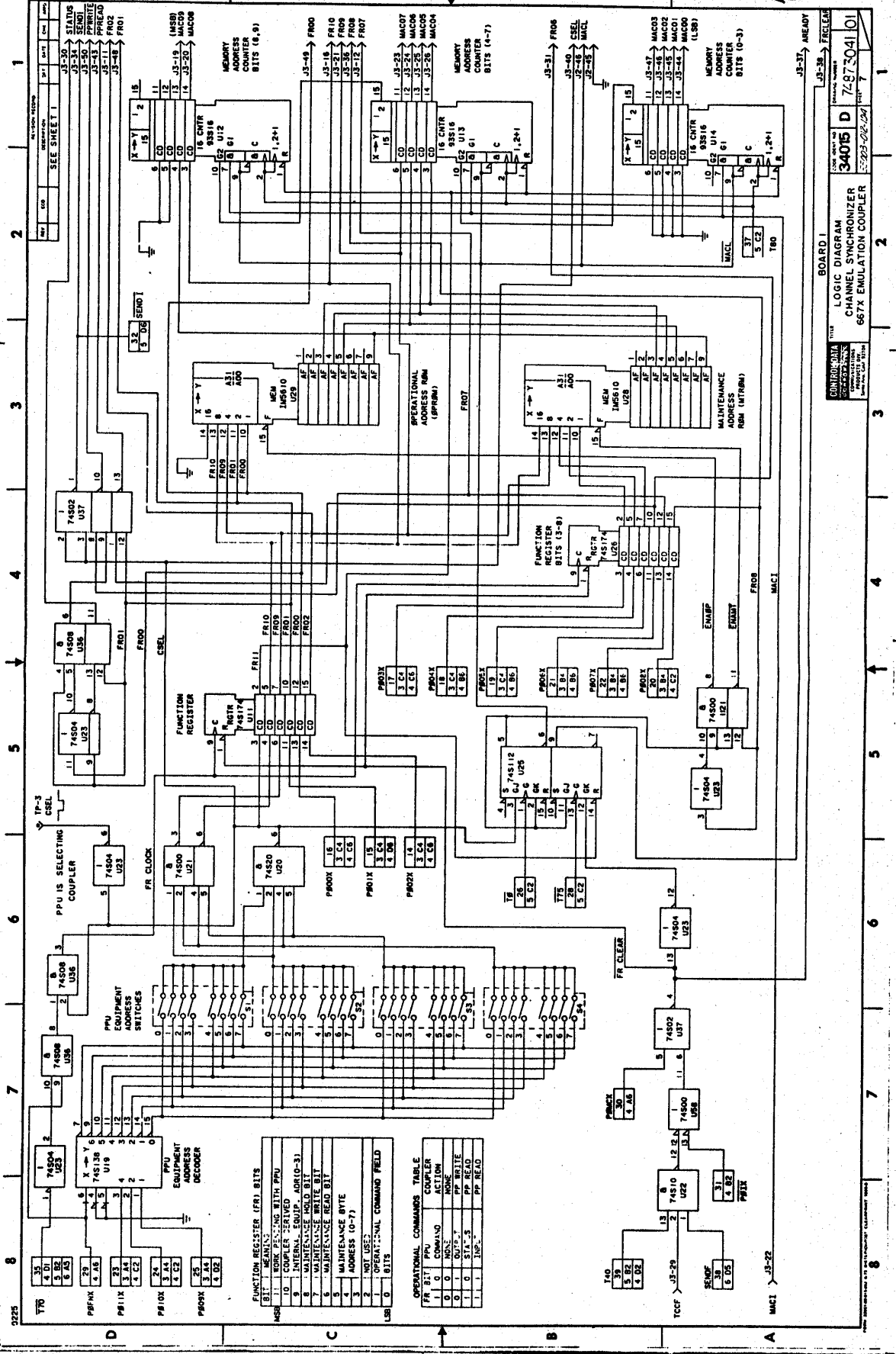








BOARD 1
 LOGIC DIAGRAM
 CHANNEL SYNCHRONIZER
 667X EMULATION COUPLER
 34075 D
 74873041 01
 DATE: 12/23/72
 REV: 6



FUNCTION REGISTER (FR) BITS

BIT	MEANING
1	WORK PENDING WITH PPU
2	COUPLER SERVED (000(0-3))
3	MAINTENANCE HOLD BIT
4	MAINTENANCE WRITE BIT
5	MAINTENANCE READ BIT
6	MAINTENANCE BYTE ADDRESS (0-7)
7	NOT USED
8	OPERATIONAL COMMAND FIELD
9	NOT USED
10	NOT USED
11	NOT USED
12	NOT USED
13	NOT USED
14	NOT USED
15	NOT USED
16	NOT USED
17	NOT USED
18	NOT USED
19	NOT USED
20	NOT USED
21	NOT USED
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27	NOT USED
28	NOT USED
29	NOT USED
30	NOT USED
31	NOT USED
32	NOT USED
33	NOT USED
34	NOT USED
35	NOT USED

OPERATIONAL COMMANDS TABLE

FR BIT	PPU ACTION
1	0
2	0
3	0
4	0
5	0
6	0
7	0
8	0
9	0
10	0
11	0
12	0
13	0
14	0
15	0
16	0
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24	0
25	0
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BOARD 1

LOGIC DIAGRAM

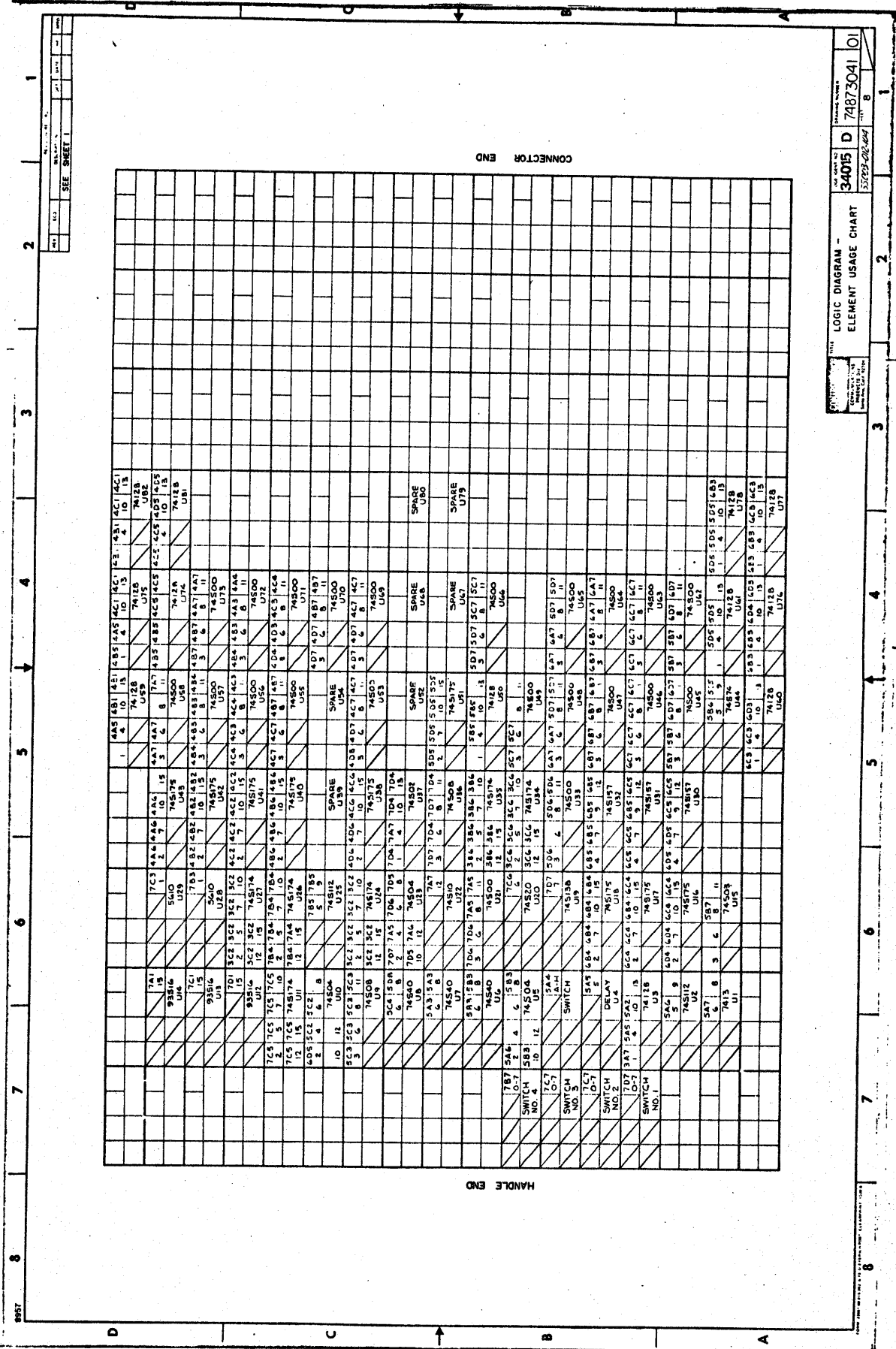
CHANNEL SYNCHRONIZER

667X EMULATION COUPLER

CONTRACT NO. 34015 D

7-87-3041 01

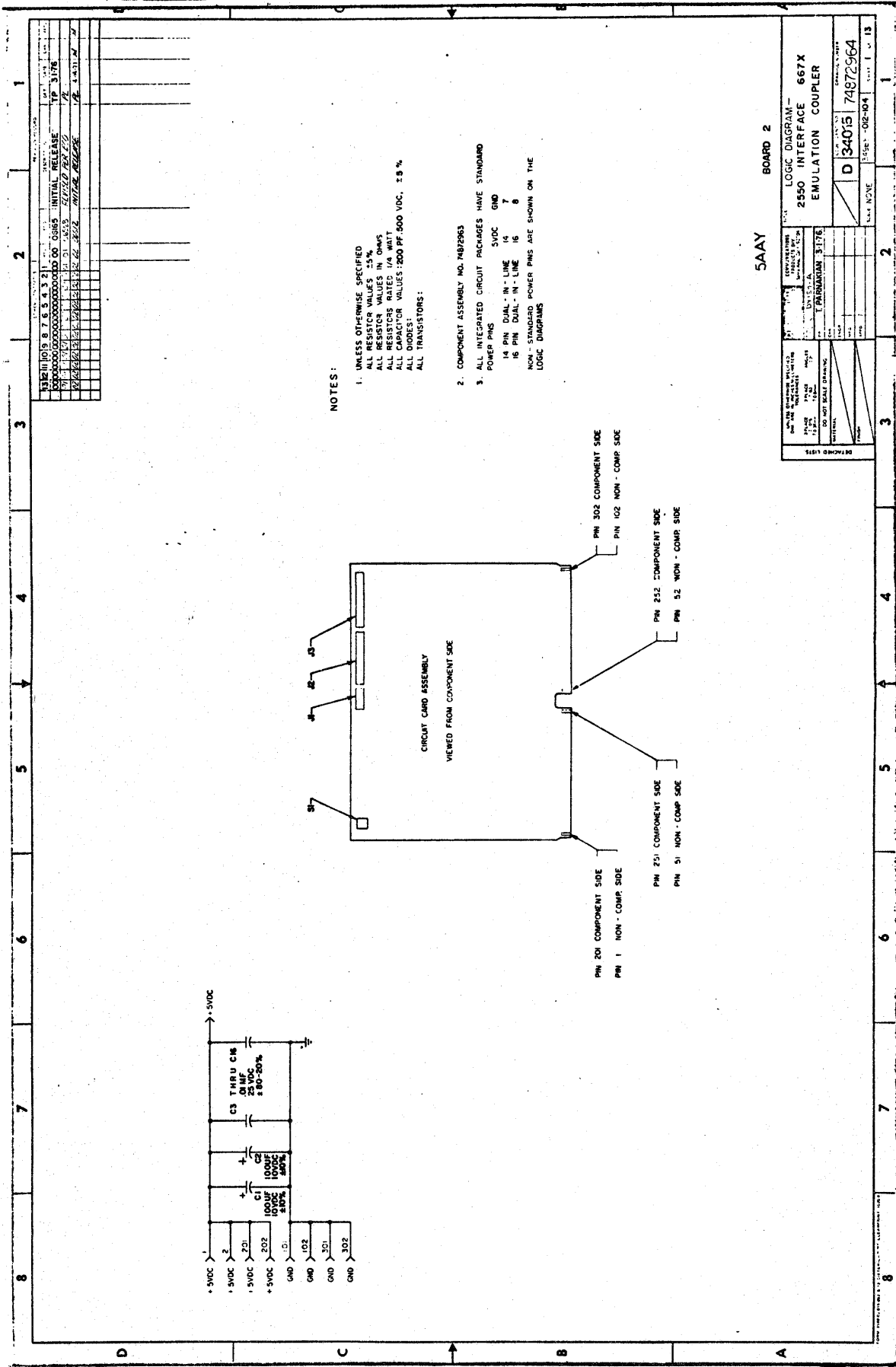
REV. 7



LOGIC DIAGRAM -
ELEMENT USAGE CHART

34015 D 74873041 01





NOTES:

- UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES 25% ALL RESISTOR VALUES IN OHMS ALL RESISTOR RATED 1/4 WATT ALL DIMENSIONS FOR VALUES > 200 PP-500 VOC, ±.5% ALL TRANSISTORS:
- COMPONENT ASSEMBLY NO. 4832983
- ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS
 - 14 PIN DUAL - IN - LINE 15 7
 - 16 PIN DUAL - IN - LINE 16 8
 NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

1	2	3	4	5	6	7	8
9	8	7	6	5	4	3	2
1	2	3	4	5	6	7	8
9	8	7	6	5	4	3	2

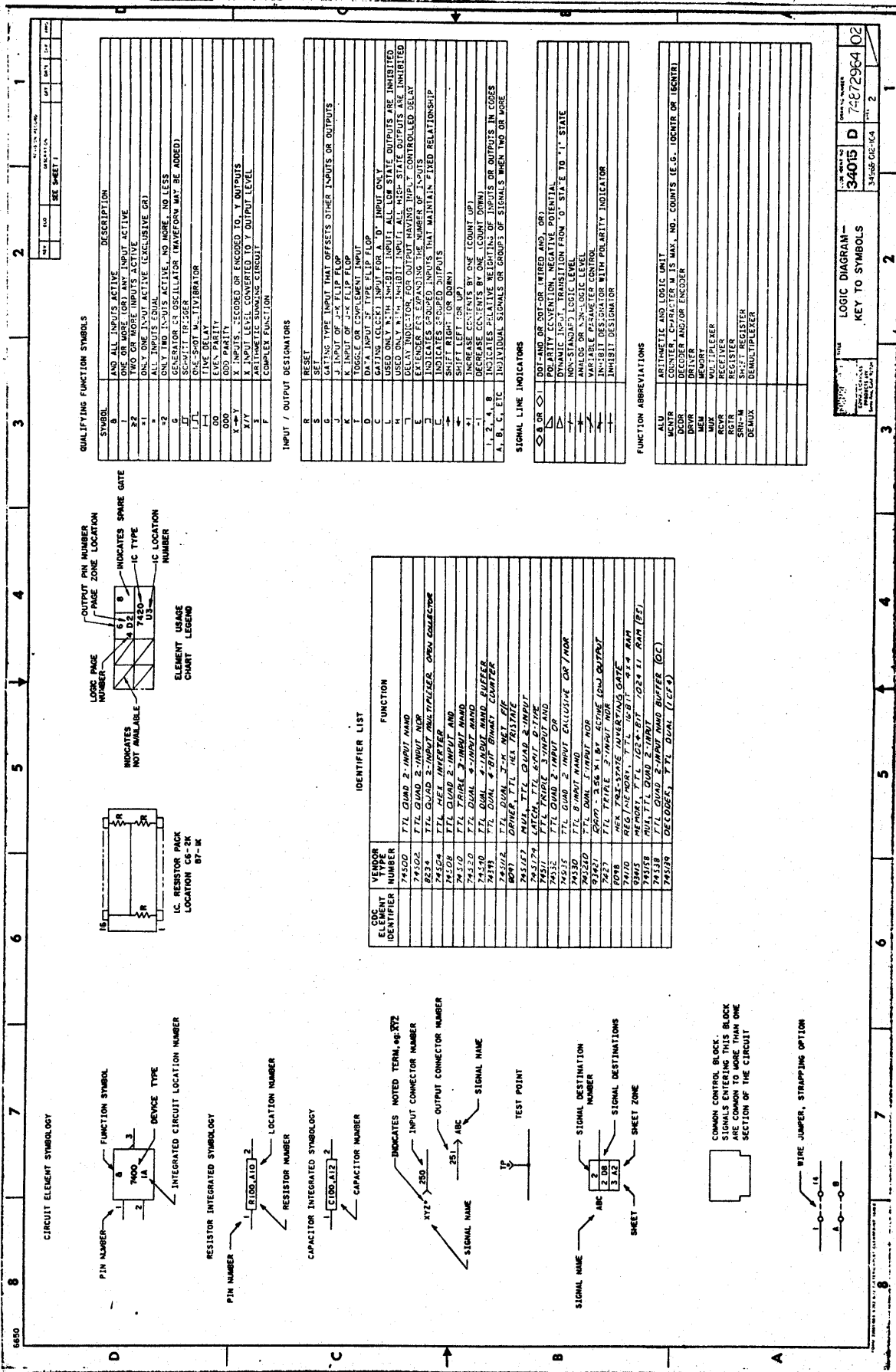
BOARD 2
5AAY

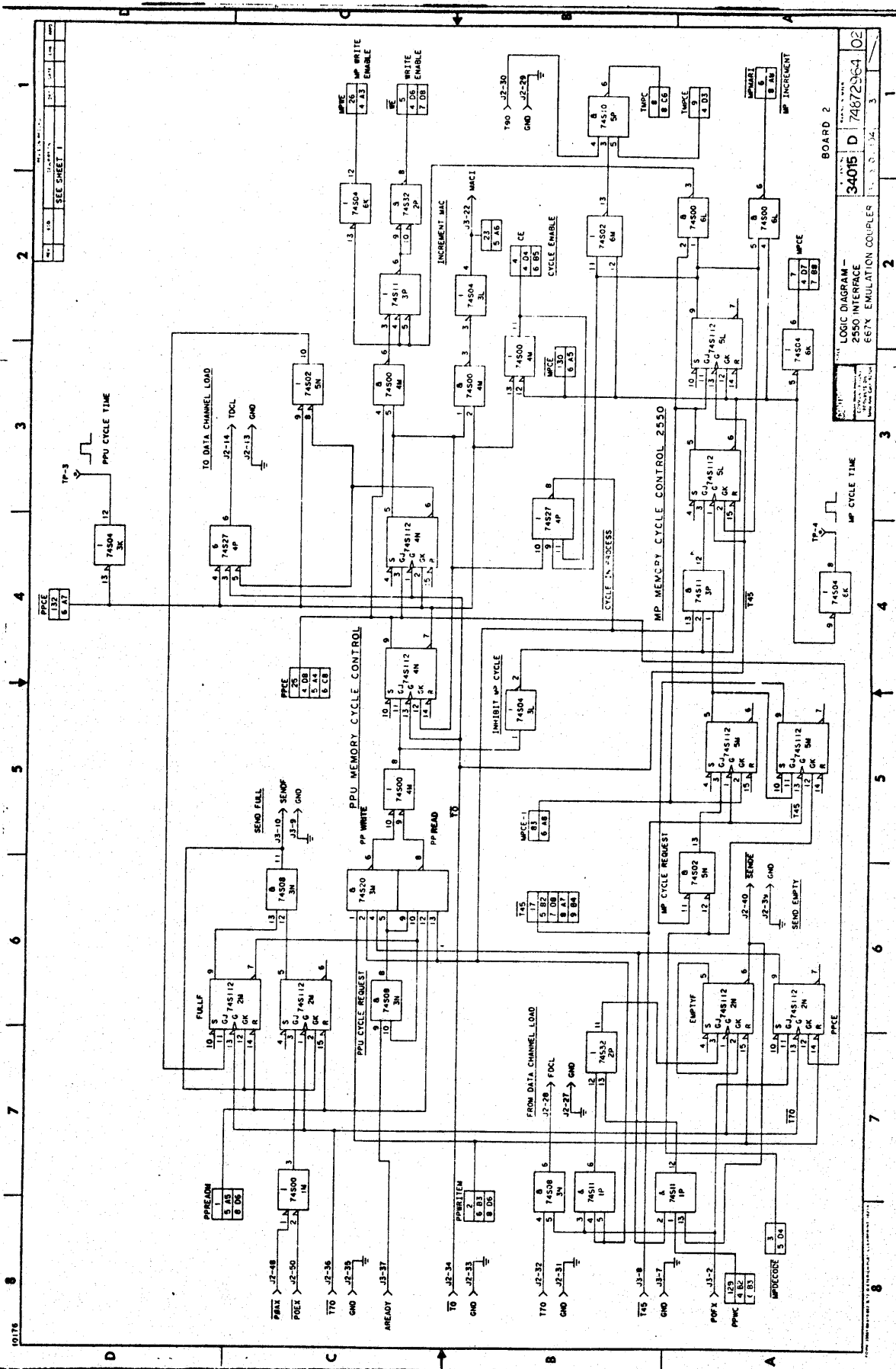
LOGIC DIAGRAM -
2550 INTERFACE
EMULATION COUPLER

PERMANENT 3176

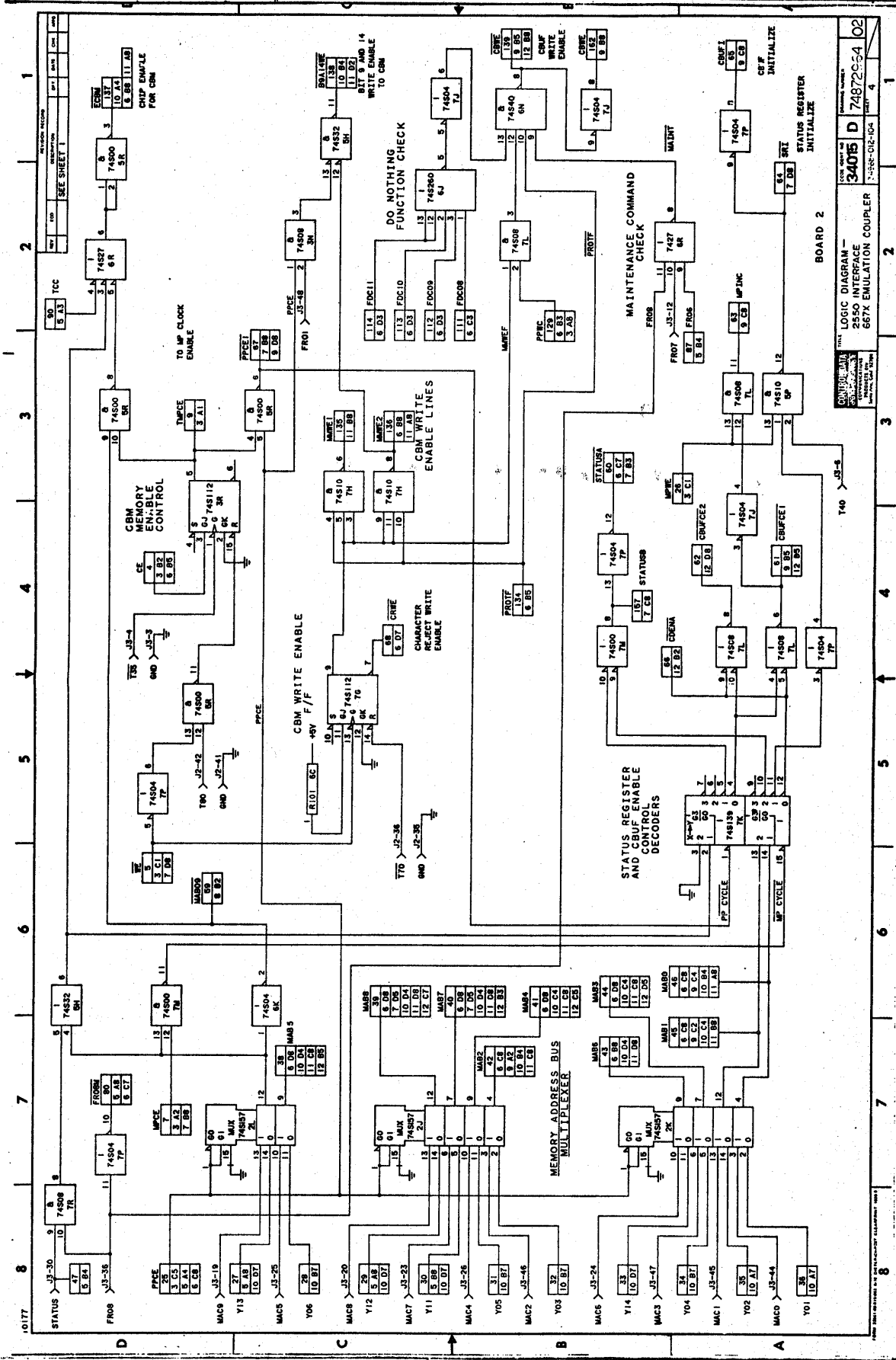
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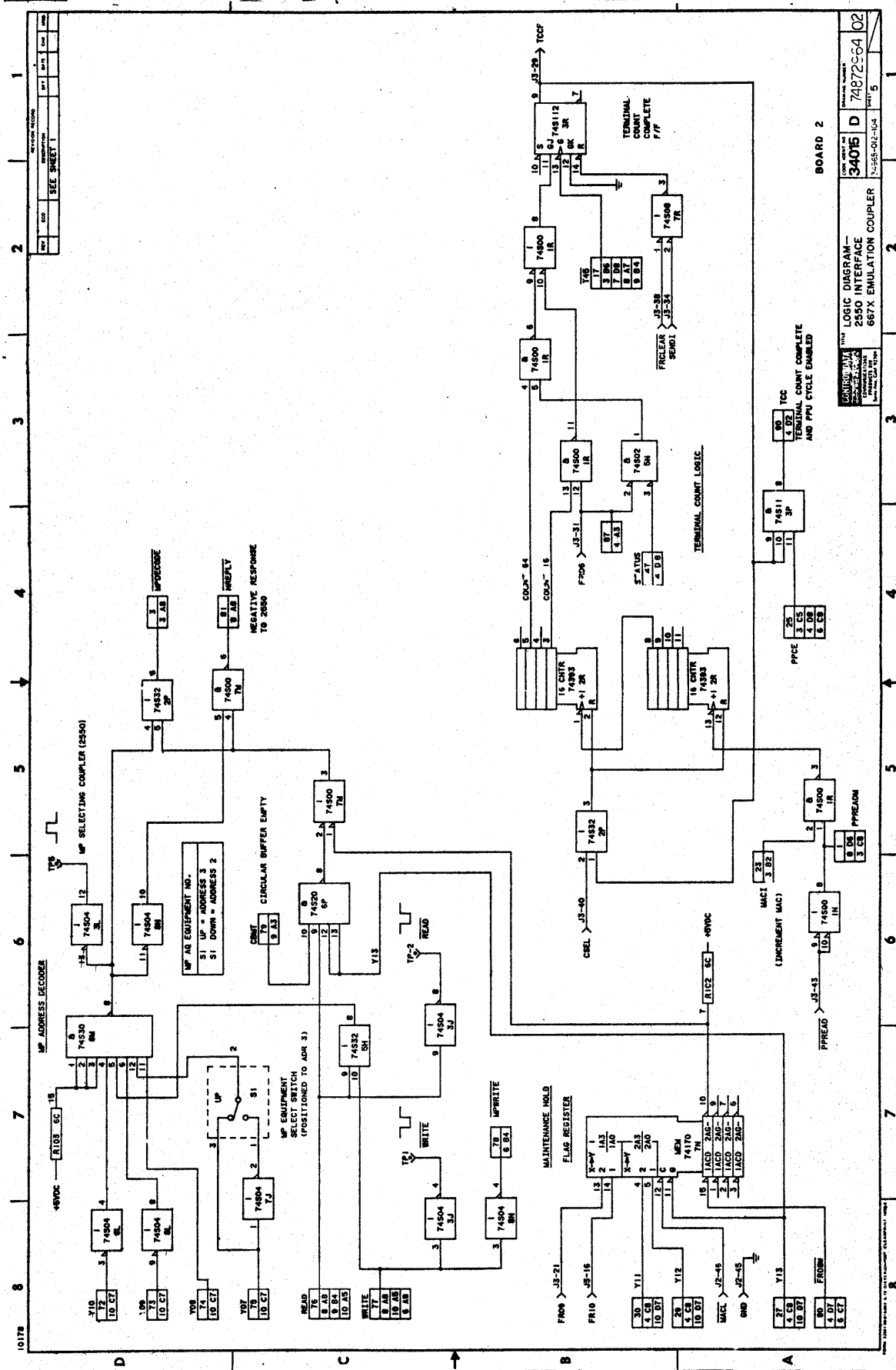




BOARD 2
 LOGIC DIAGRAM -
 2550 INTERFACE
 667K EMULATION COUPLER
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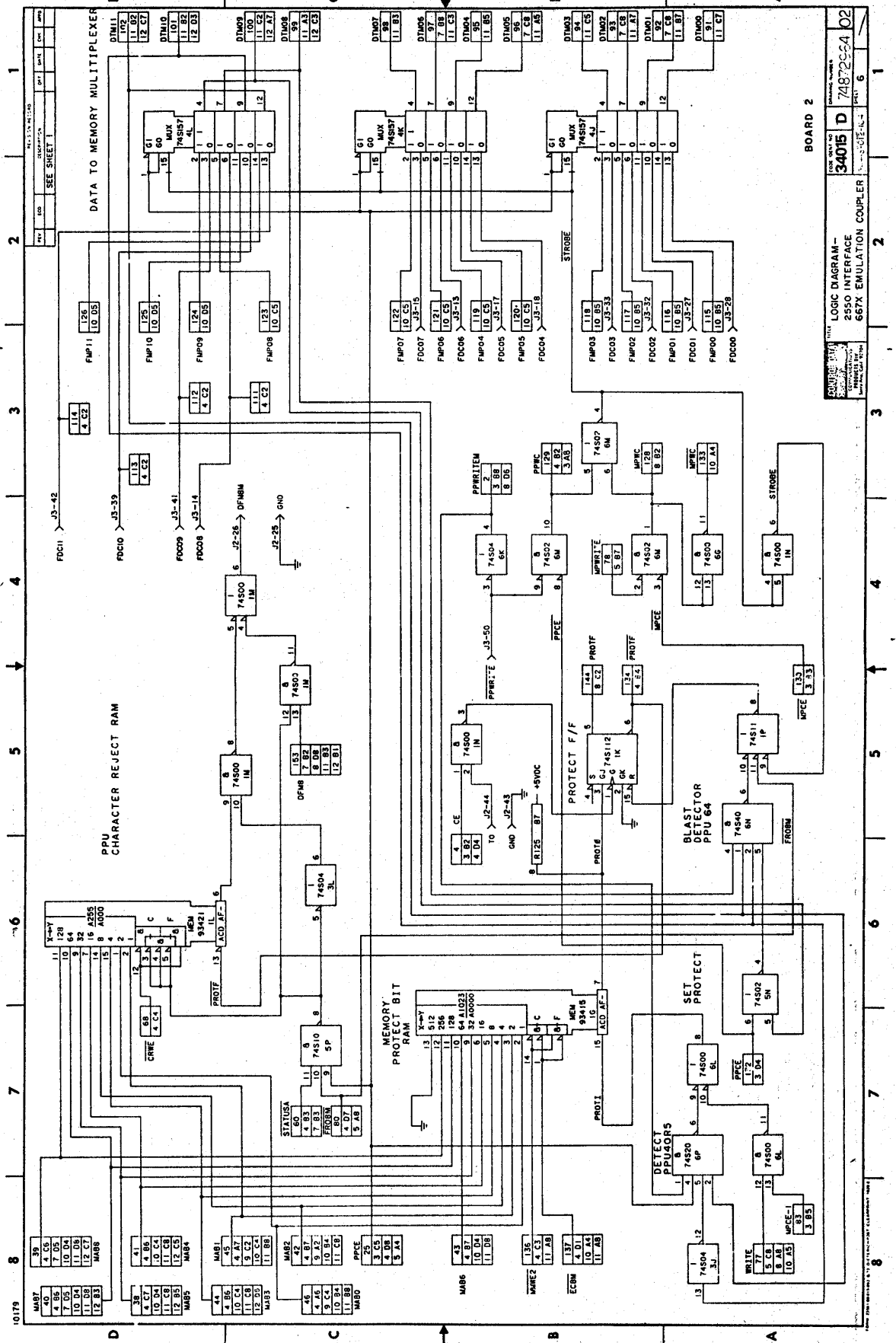


BOARD 2
 LOGIC DIAGRAM -
 2550 INTERFACE
 667X EMULATION COUPLER
 34015 D 74872554 02
 34015 D 74872554 02
 667X-012-104
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BOARD 2
 LOGIC DIAGRAM—
 2850 INTERFACE
 687X EMULATION COUPLER

3405 D 74872564 02
 1-565-02-104



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793 05
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856 05
859 05
862 05
865 05
868 05
871 05
874 05
877 05
880 05
883 05
886 05
889 05
892 05
895 05
898 05
901 05
904 05
907 05
910 05
913 05
916 05
919 05
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925 05
928 05
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937 05
940 05
943 05
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952 05
955 05
958 05
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982 05
985 05
988 05
991 05
994 05
997 05
1000 05

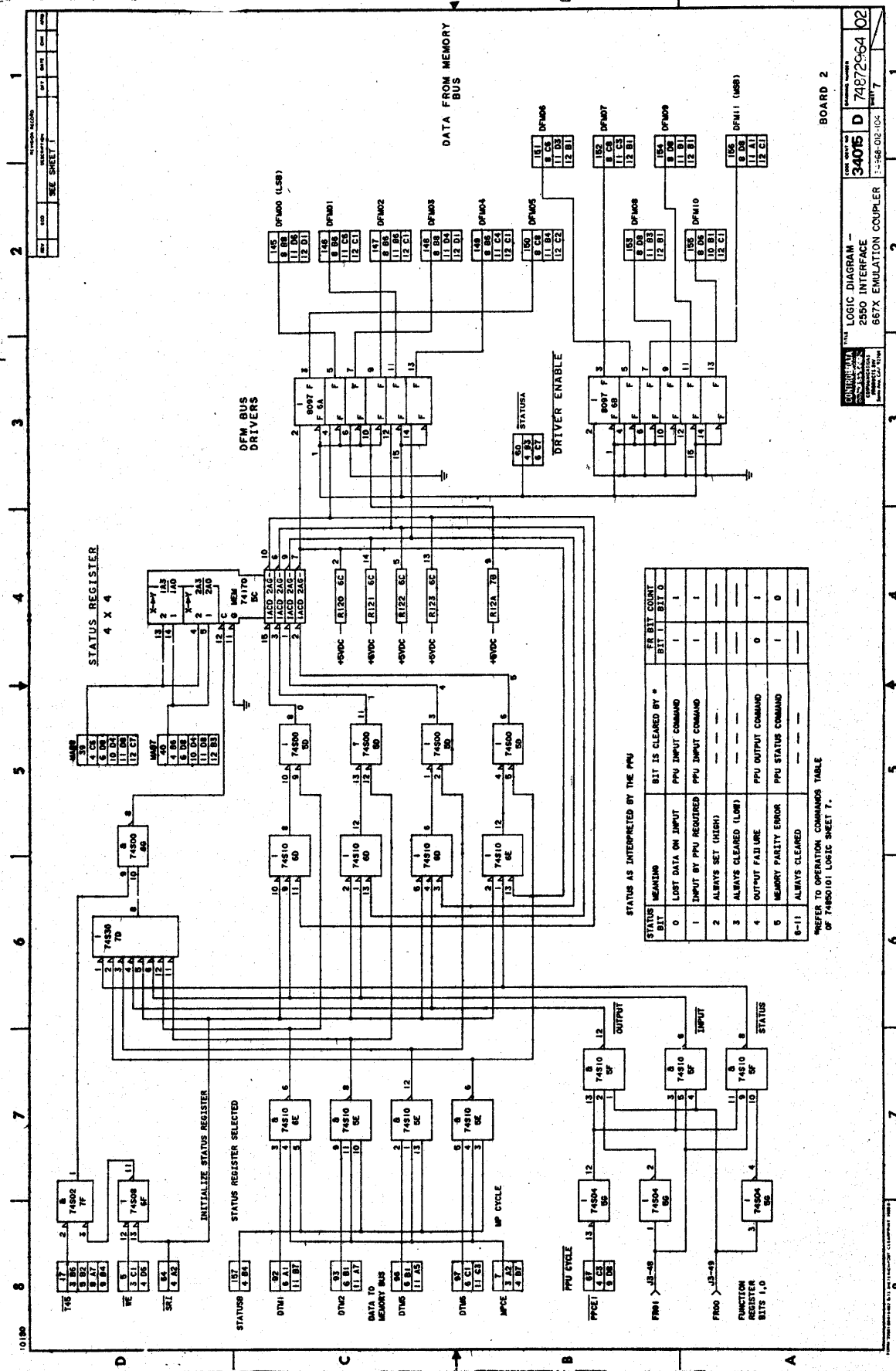
SEE SHEET 1

BOARD 2

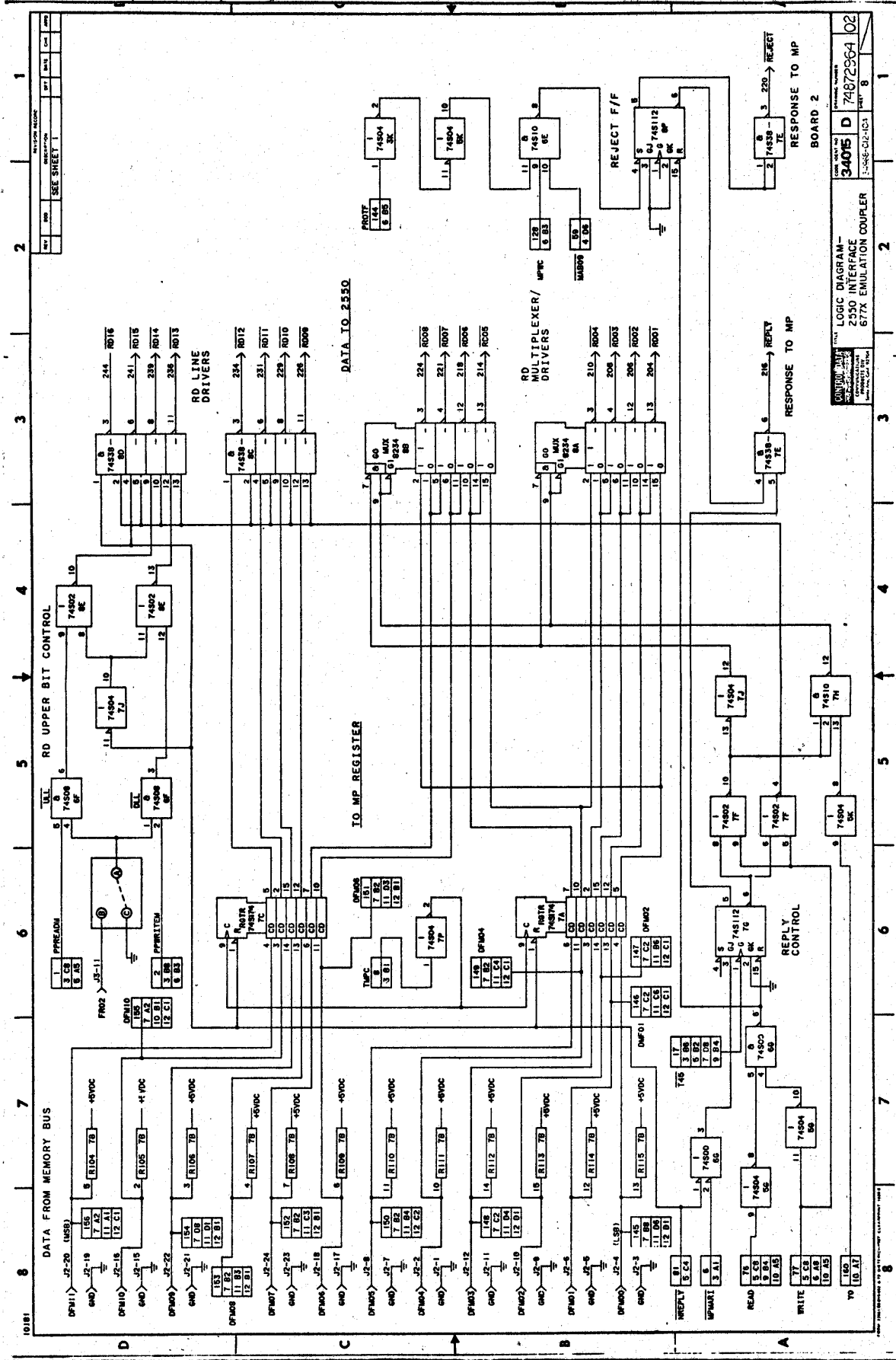
LOGIC DIAGRAM - 2550 INTERFACE - 687X EMULATION COUPLER

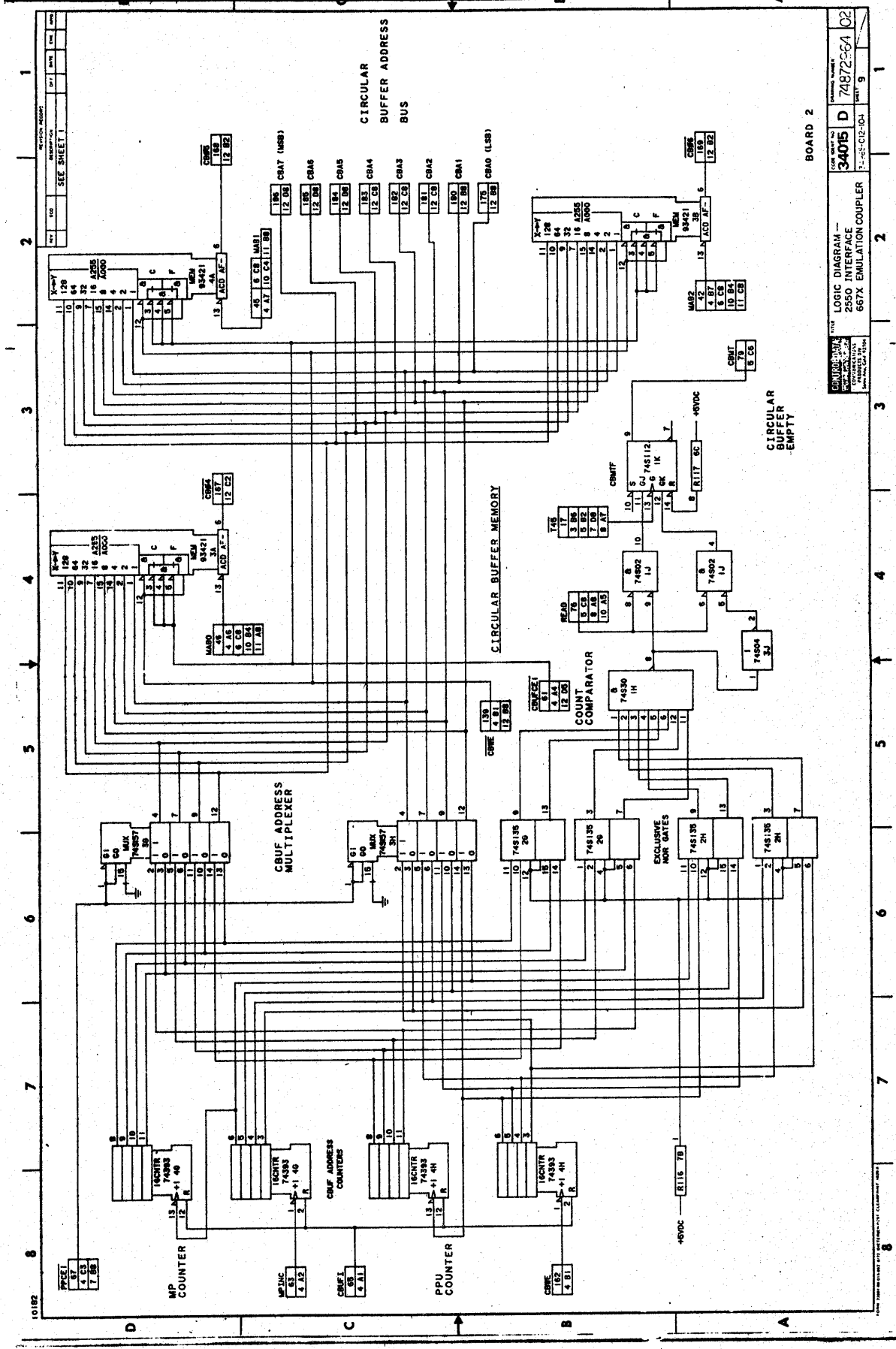
34015 D

74879600 C

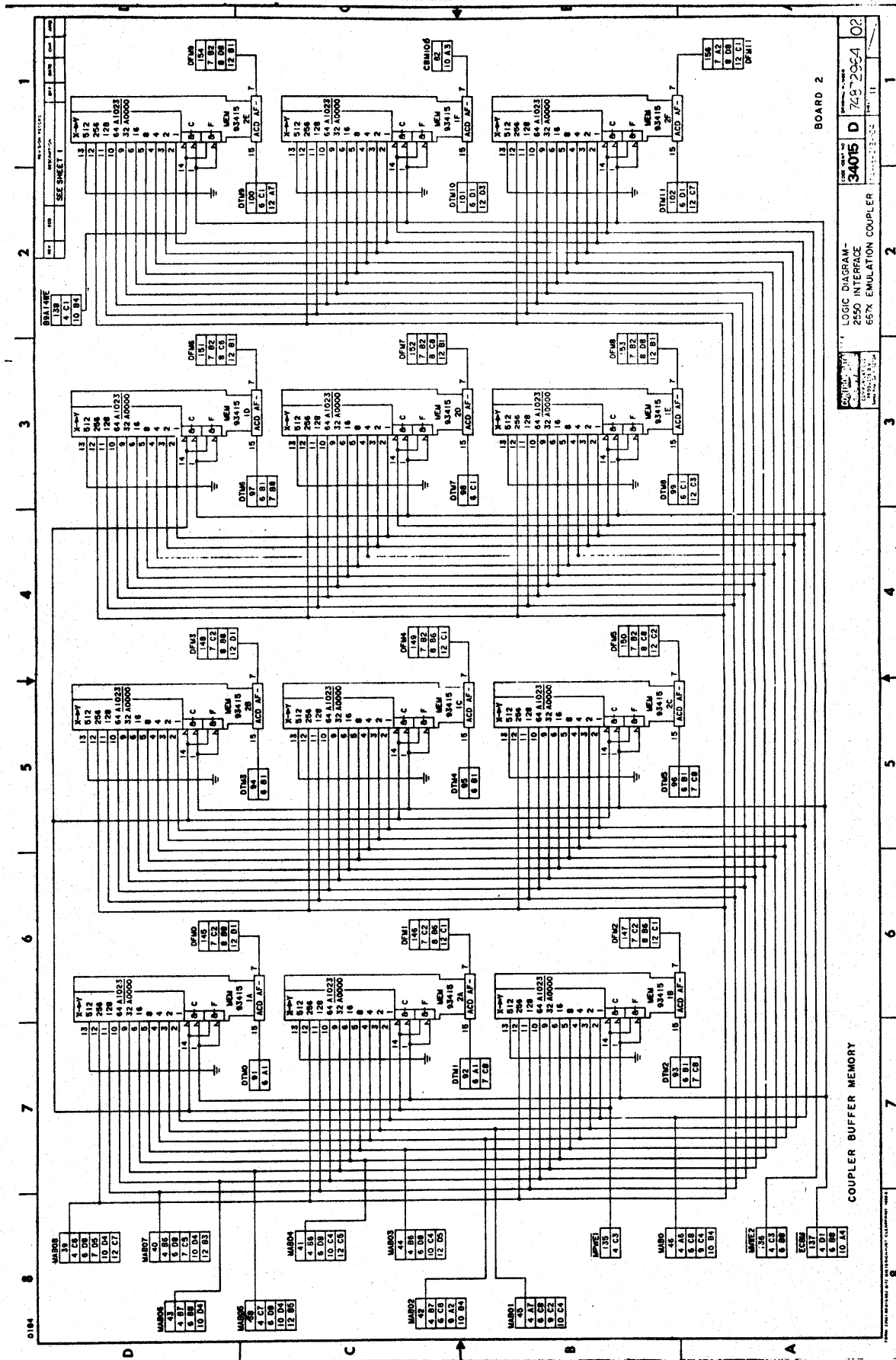


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 LOGIC DIAGRAM -
 2550 INTERFACE
 667X EMULATION COUPLER
 BOARD 2

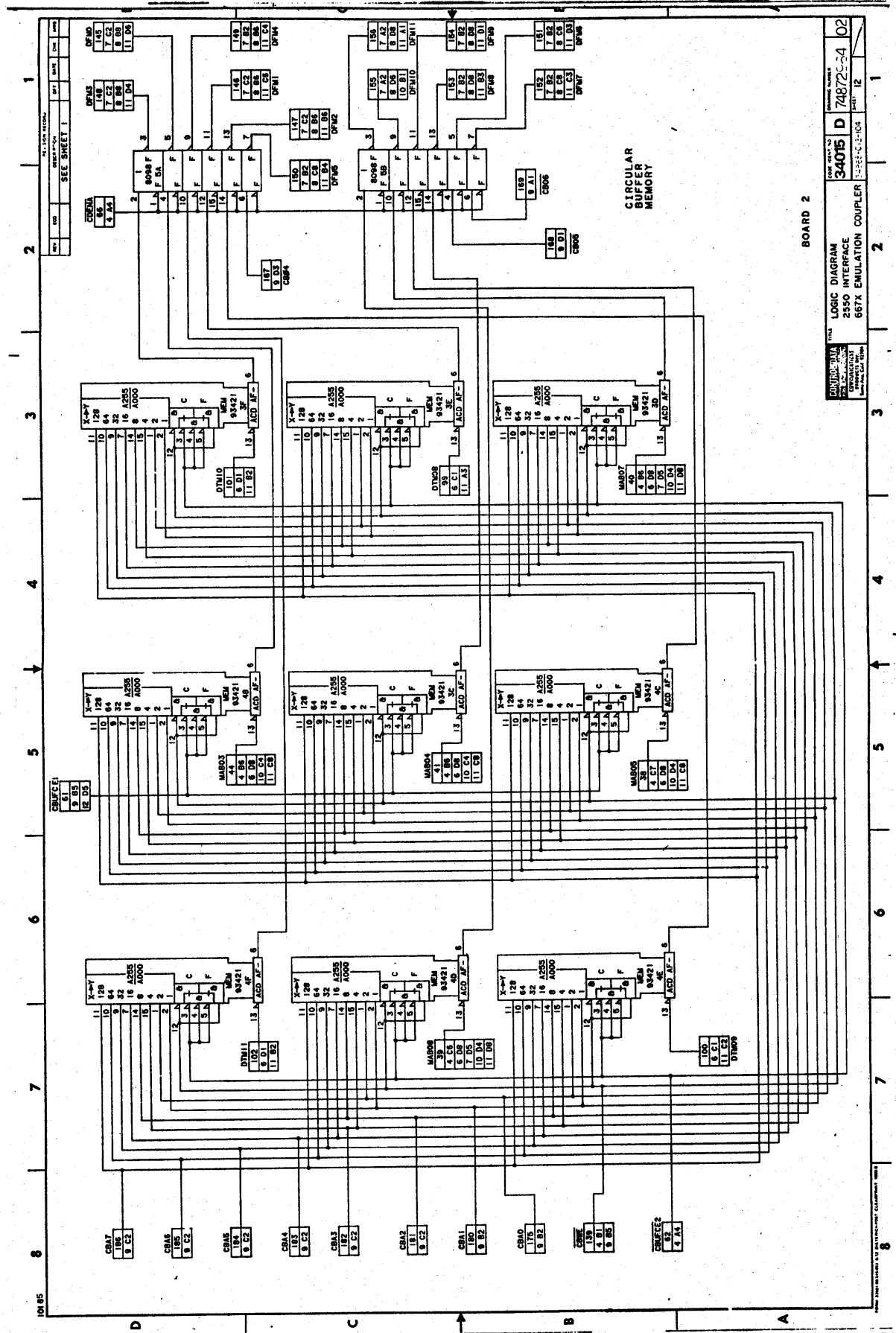


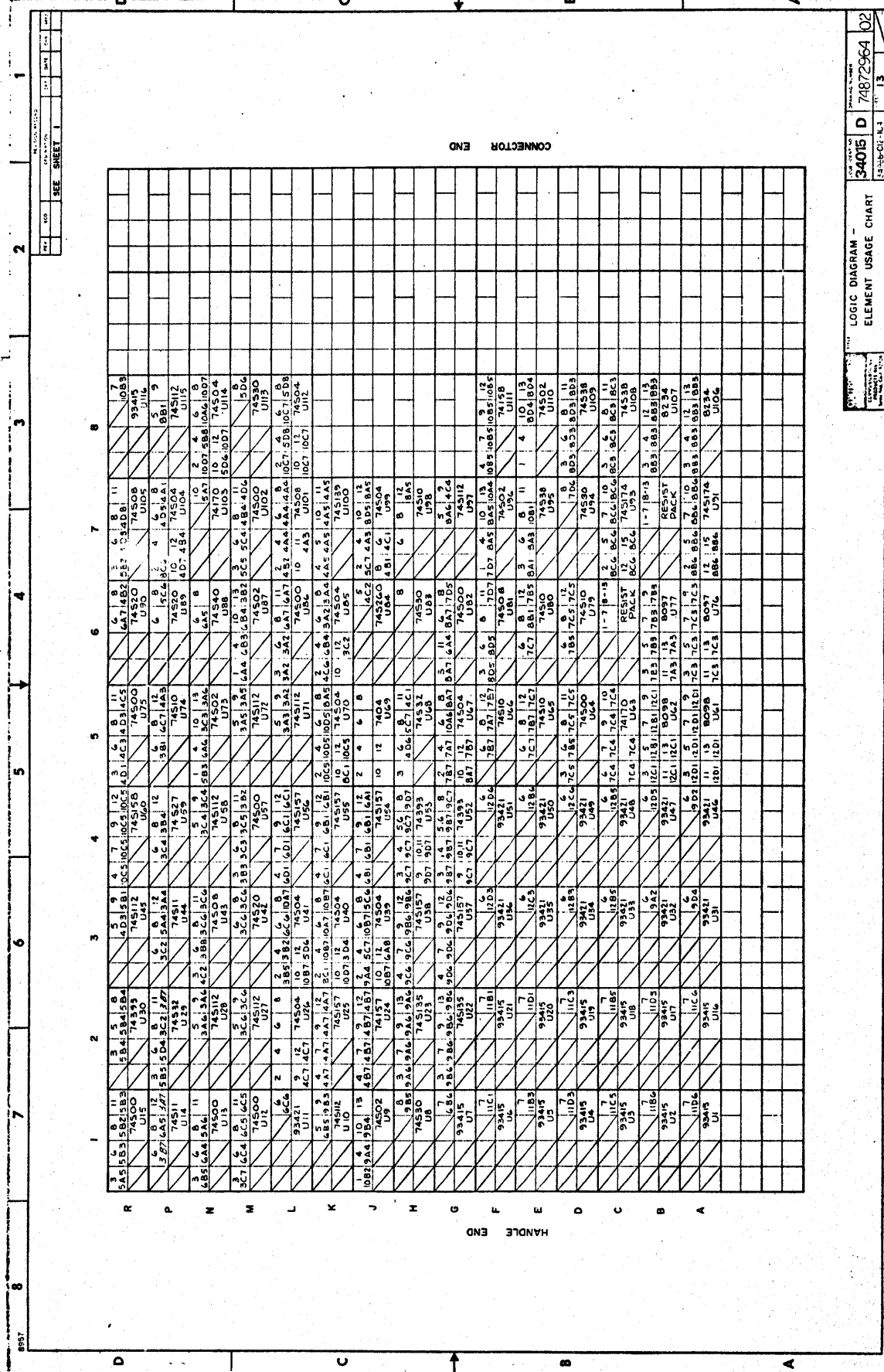


BOARD 2
 LOGIC DIAGRAM -
 2550 INTERFACE
 667X EMULATION COUPLER
 34015 D 74872-64 02
 REV. 9



BOARD 2
 LOGIC DIAGRAM -
 2550 INTERFACE
 657X EMULATION COUPLER
 34015 D
 74872954 02
 REV. 11



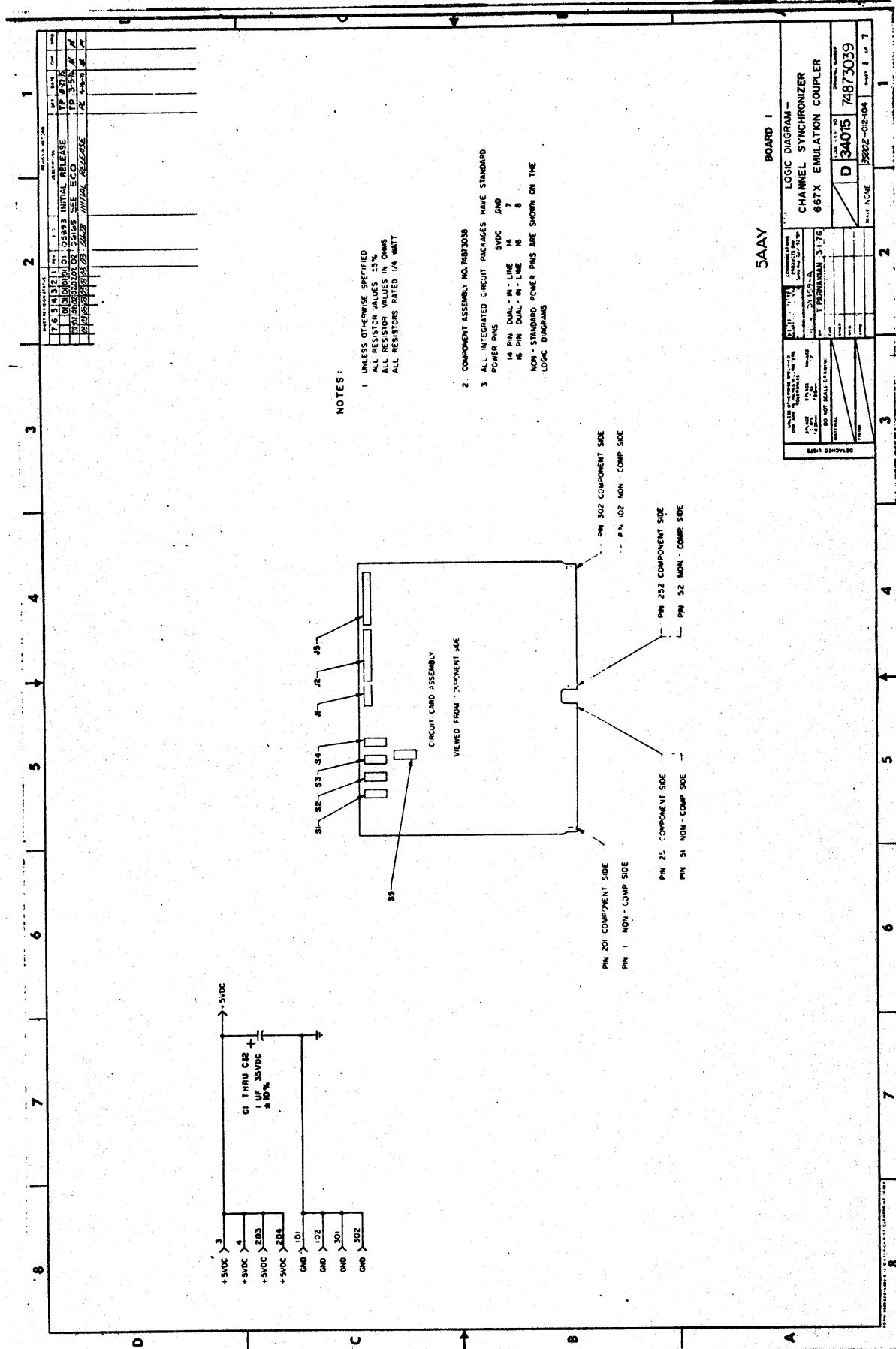


SEE SHEET 1

LOGIC DIAGRAM -
ELEMENT USAGE CHART

34015 D 74879604 02





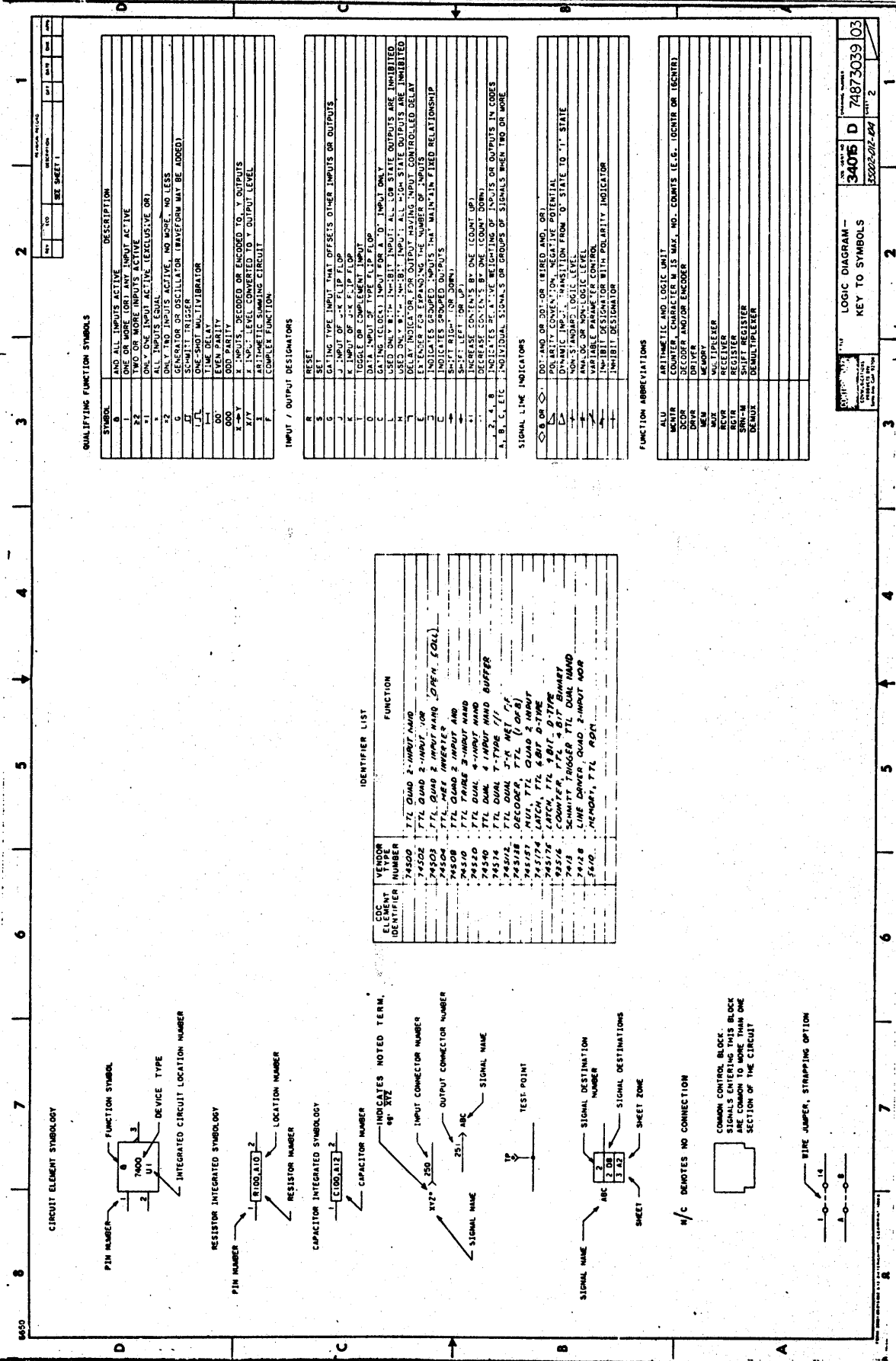
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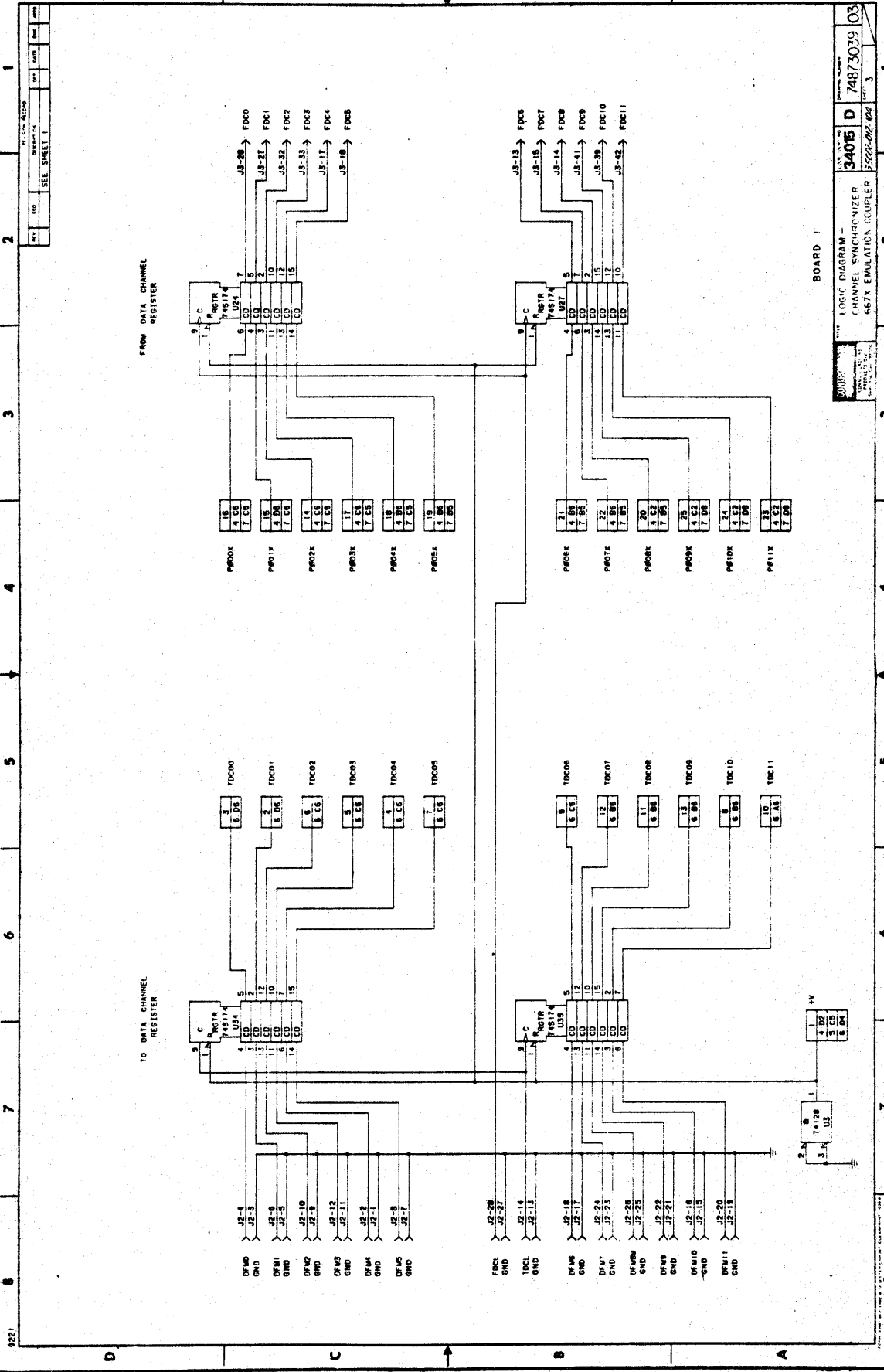
- 1 UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES .25% ALL RESISTOR VALUES IN OHMS ALL RESISTORS RATED 1/4 WATT
- 2 COMPONENT ASSEMBLY NO. M873033
- 3 ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS
 GND 5VDC
 14 PIN DUAL - IN - LINE 14
 16 PIN DUAL - IN - LINE 16
 NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

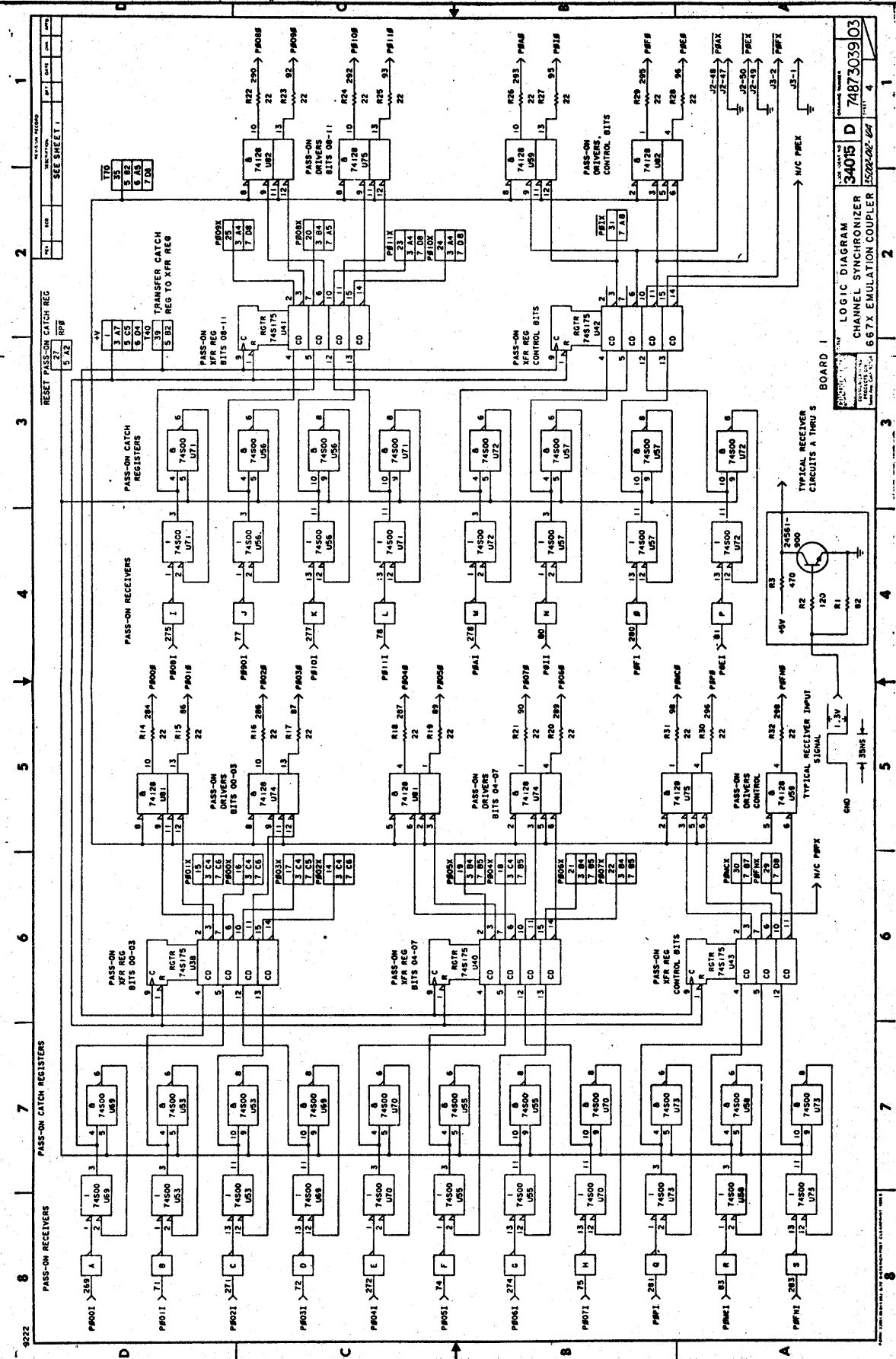
5AAY

BOARD 1

LOGIC DIAGRAM - CHANNEL SYNCHRONIZER	
667X EMULATION COUPLER	
DATE: NONE	REV: D
34015	74873039
39922-02-104	1 of 7







3222

SEE SHEET 1

DATE

REV

REV

REV

REV

BOARD 1

LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
34015 D 74873039103

66TX EMULATION COUPLER
5502-002-001

REV 1

REV 2

REV 3

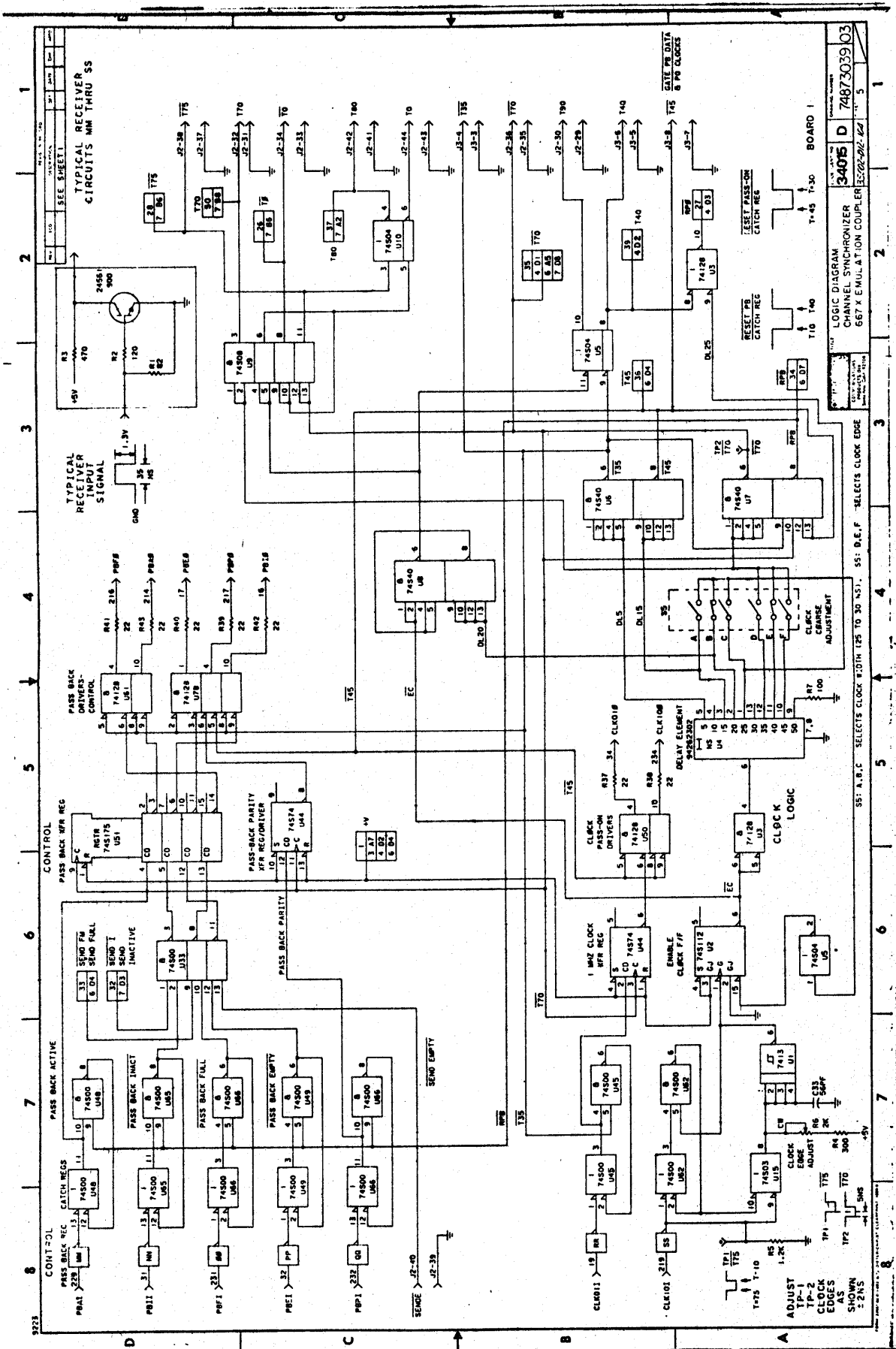
REV 4

REV 5

REV 6

REV 7

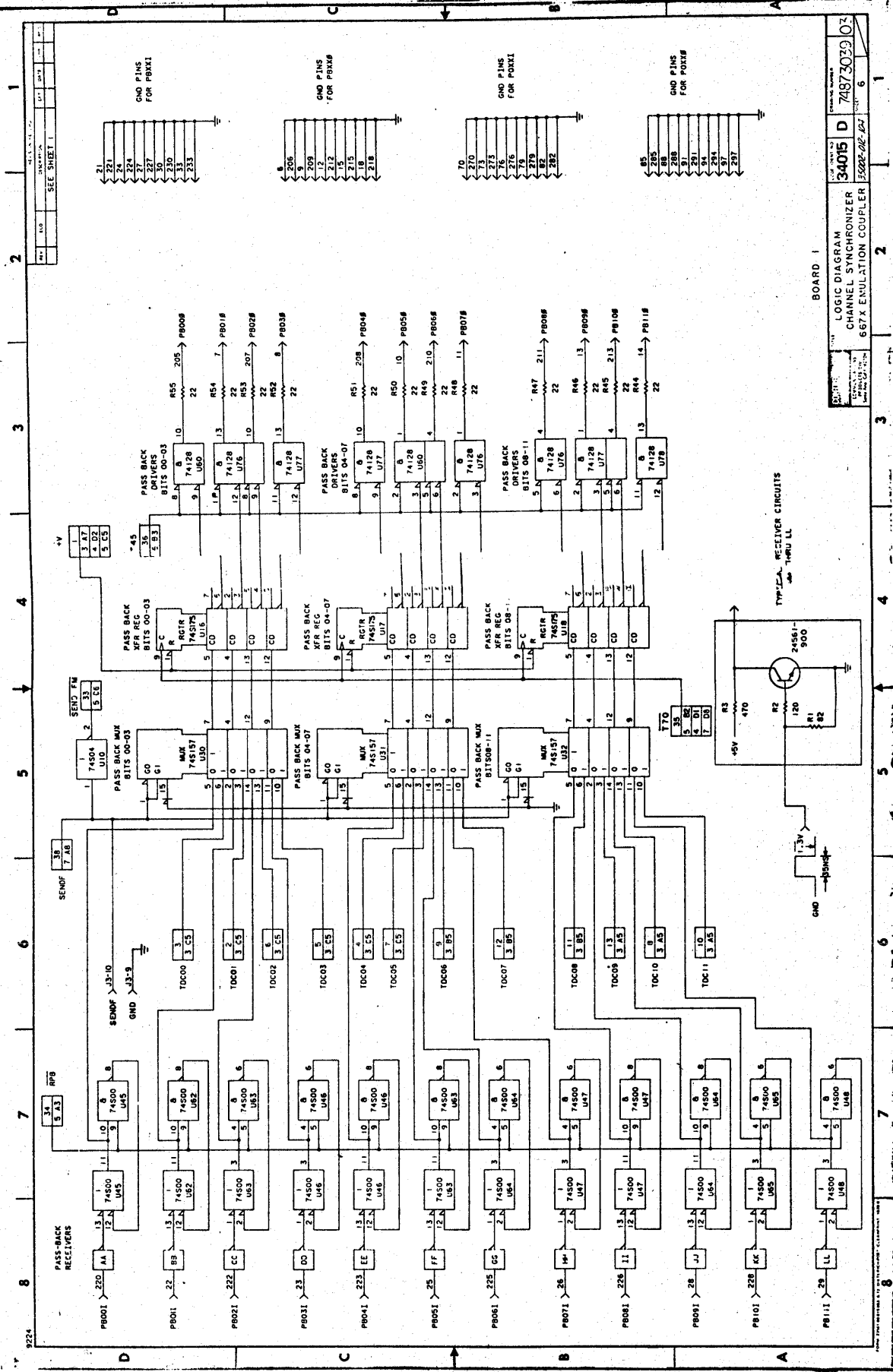
REV 8



LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667 X EMULATION COUPLER

3405 D 74873039 03

SS: A, B, C SELECTS CLOCK WIDTH 125 TO 30 NS. SS: D, E, F SELECTS CLOCK EDGE



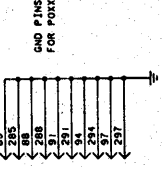
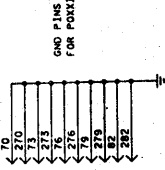
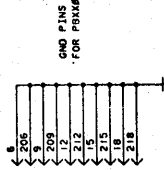
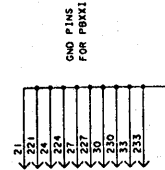
BOARD 1

LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER

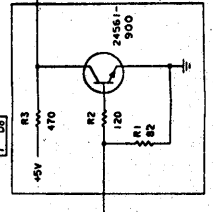
34015 D
74873039 07
1302E-02-07
6

21	22	23	24	25	26	27	28	29	30	31	32	33	34
35	36	37	38	39	40	41	42	43	44	45	46	47	48

SEE SHEET 1

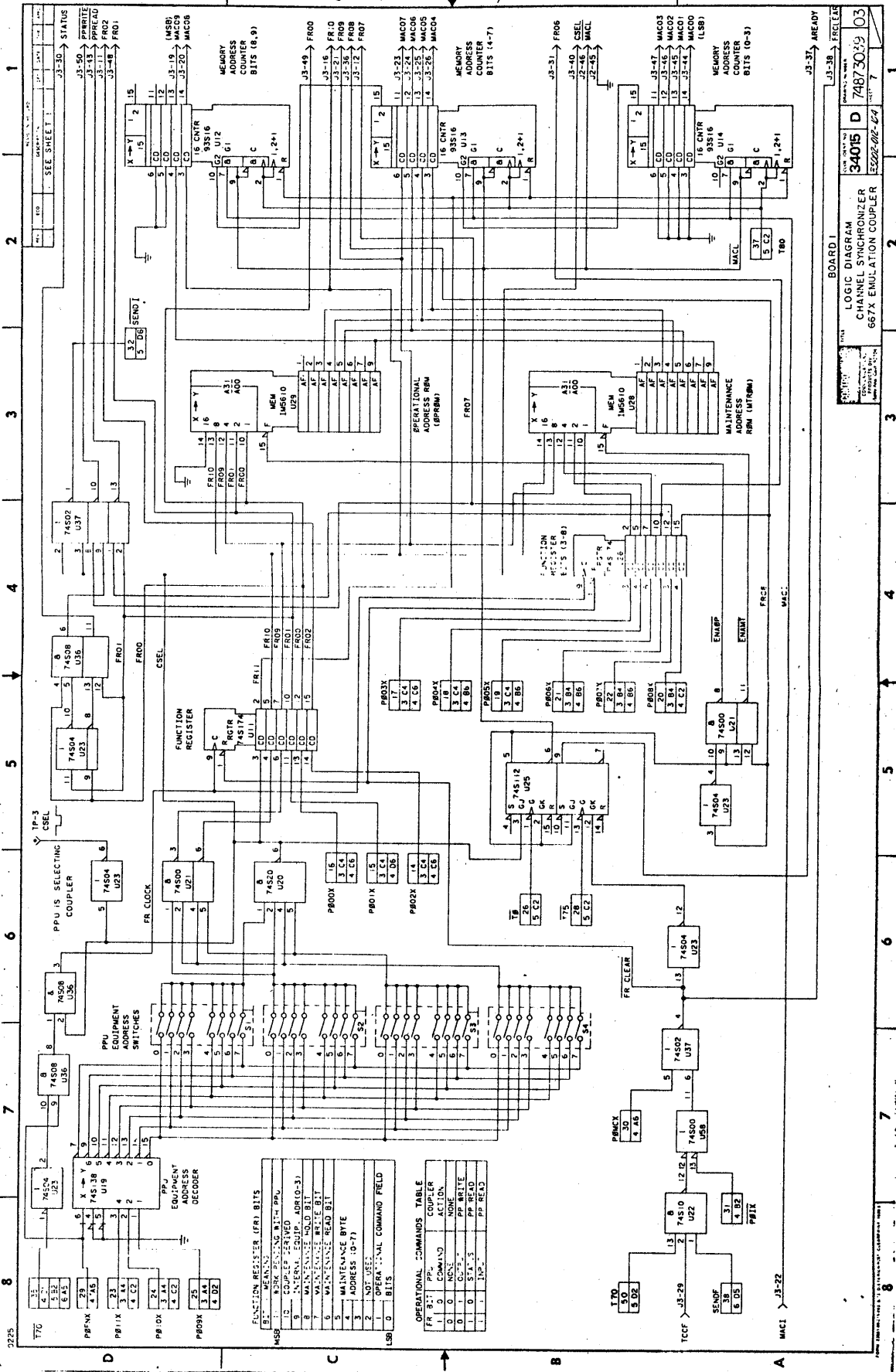


TYPICAL RECEIVER CIRCUITS
THRU LL



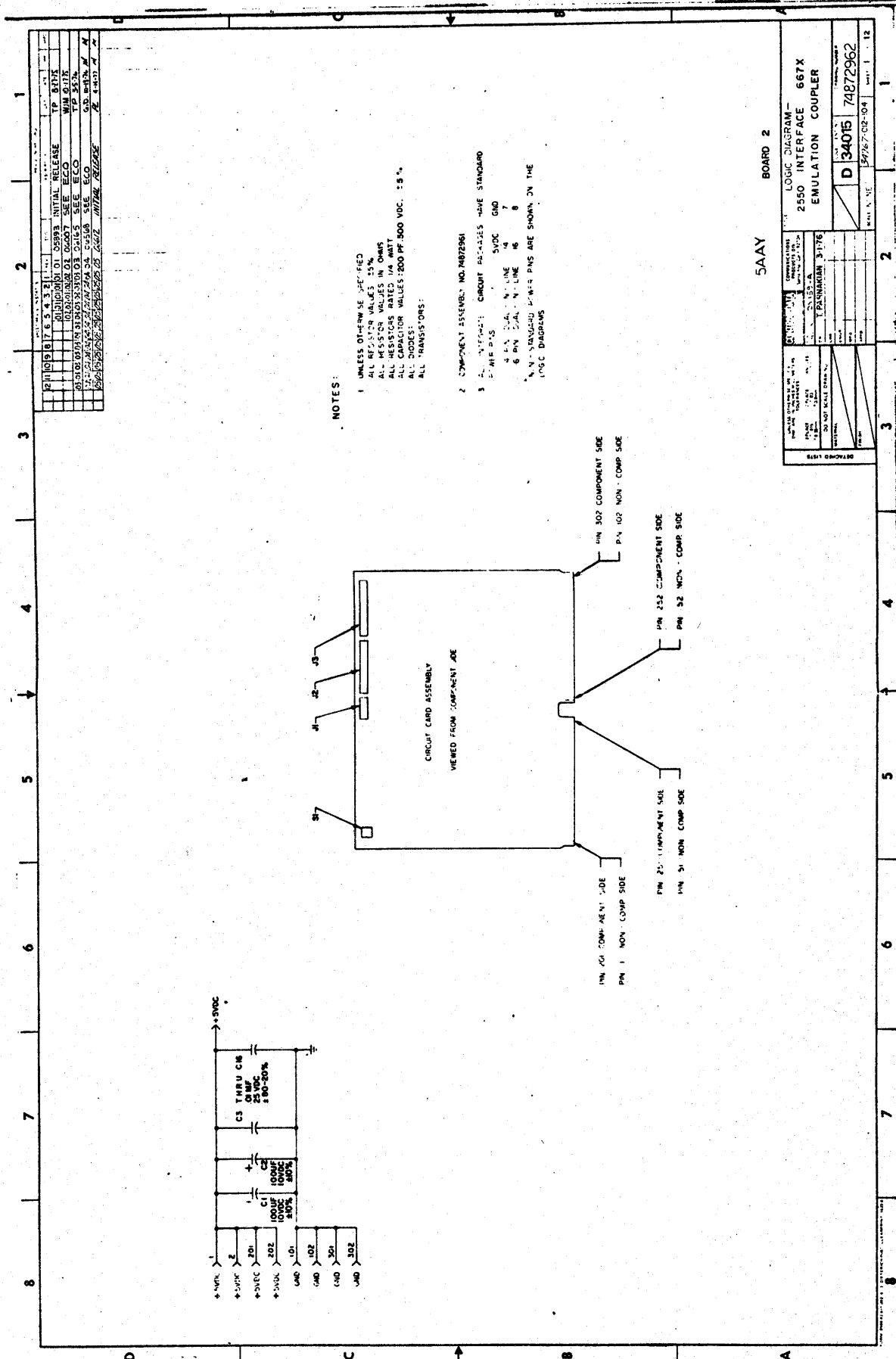
2224

667X EMULATION COUPLER



BOARD I
 LOGIC DIAGRAM
 CHANNEL SYNCHRONIZER
 667X EMULATION COUPLER
 34015 D 748730:19 03
 5202-02-27





NOTES:

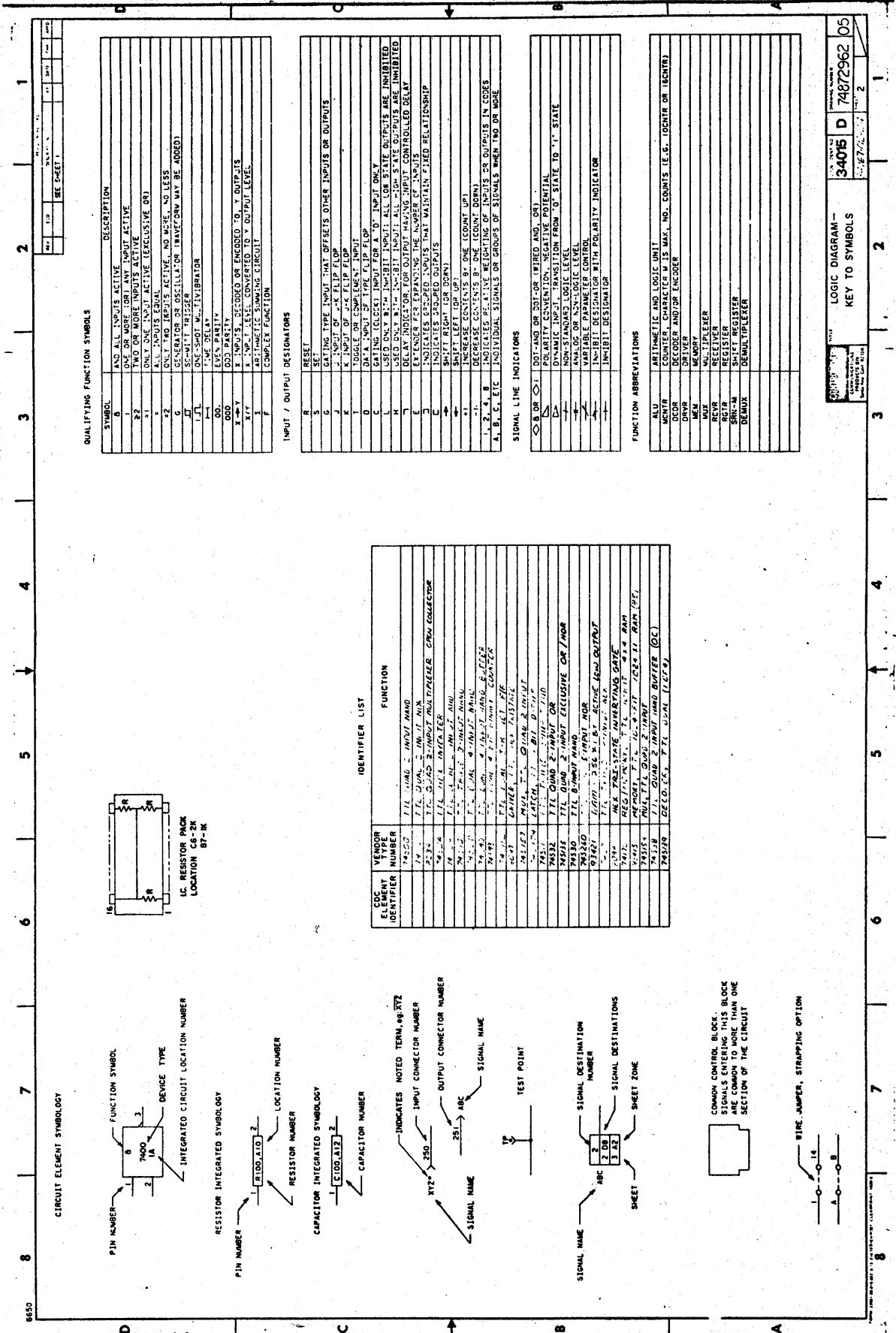
- 1 UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES 5%, ALL RESISTOR VALUES IN OHMS ALL CAPACITOR VALUES IN MICROFARADS ALL CAPACITOR VALUES 500 PF 500 VDC, 5.5%, ALL DIODES: ALL TRANSISTORS:
- 2 COMPONENT ASSEMBLY NO. M022961
- 3 ALL DIMENSIONS ARE STANDARD UNLESS OTHERWISE SPECIFIED
- 4 ALL DIMENSIONS ARE IN INCHES
- 5 ALL DIMENSIONS ARE IN MILLIMETERS
- 6 ALL DIMENSIONS ARE IN MILLIMETERS
- 7 ALL DIMENSIONS ARE IN MILLIMETERS
- 8 ALL DIMENSIONS ARE IN MILLIMETERS

REV. NO.	1	DATE	11/1/68
BY	...	CHECKED	...
DATE	...	DATE	...
REV. NO.	1	DATE	11/1/68
BY	...	CHECKED	...
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REV. NO.	1	DATE	11/1/68
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DATE	...	DATE	...

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BY	...	CHECKED	...
DATE	...	DATE	...

BOARD 2
 LOGIC DIAGRAM -
 2550 INTERFACE 667X
 EMULATION COUPLER
 D 34015 7487962
 DATE 11/1/68
 BY ...
 CHECKED ...
 DATE ...



QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
B	AND ALL INPUTS ACTIVE
C	ONE OR MORE INPUTS ACTIVE
D	ONE OR MORE INPUTS ACTIVE
E	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
F	ALL INPUTS EQUAL
G	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
H	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
I	COMPARATOR
J	ONE OR MORE INPUTS ACTIVE
K	EVEN PARITY
L	ODD PARITY
M	X INPUTS, DECODED OR ENCODED TO Y OUTPUTS
N	X INPUTS, LEVEL CONVERTED TO Y OUTPUT LEVEL
O	INVERTING CIRCUIT
P	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

SYMBOL	DESCRIPTION
R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF JK FLIP FLOP
K	K INPUT OF JK FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
C	CLOCK INPUT
L	USED ONLY WITH INHIBIT INPUT FOR AND INPUT ONLY
H	USED ONLY WITH INHIBIT INPUT. ALL LOW STATE OUTPUTS ARE INHIBITED
M	DELAY INDICATOR. FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
C	INDICATES SIGNALS THAT MAINTAIN FIXED RELATIONSHIP
+	SHIFT RIGHT (OR ON)
-	SHIFT LEFT (OR ON)
+	INCREASE CONTENTS BY ONE (COUNT UP)
-	DECREASE CONTENTS BY ONE (COUNT DOWN)
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

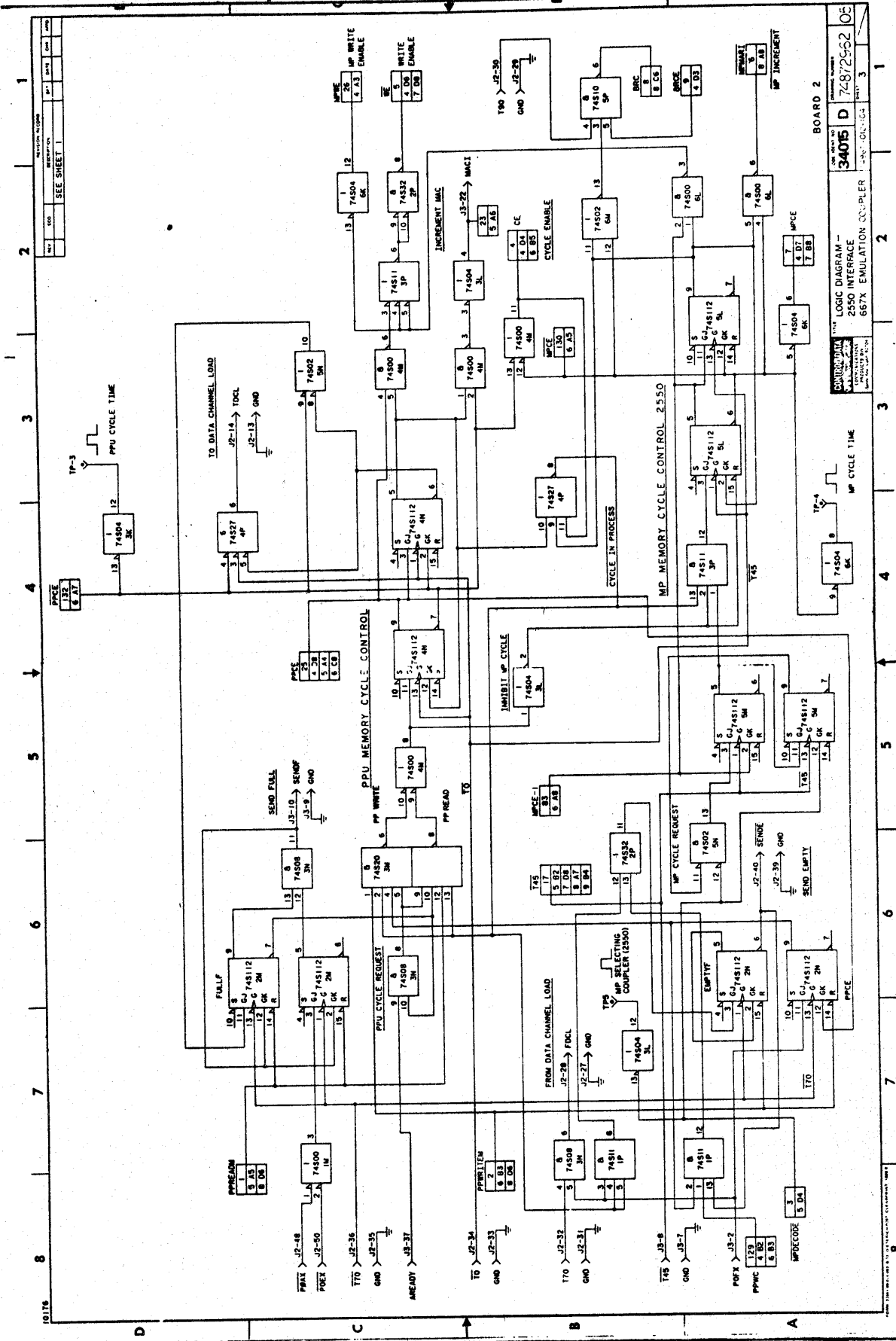
⊙	DOT-AND OR DOT-OR (WIRED AND, OR)
⊙	NON-STANDARD LOGIC LEVEL
⊙	ANALOG OR NON-LOGIC LEVEL
⊙	VARIABLE PARAMETER CONTROL
⊙	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
⊙	INHIBIT DESIGNATOR

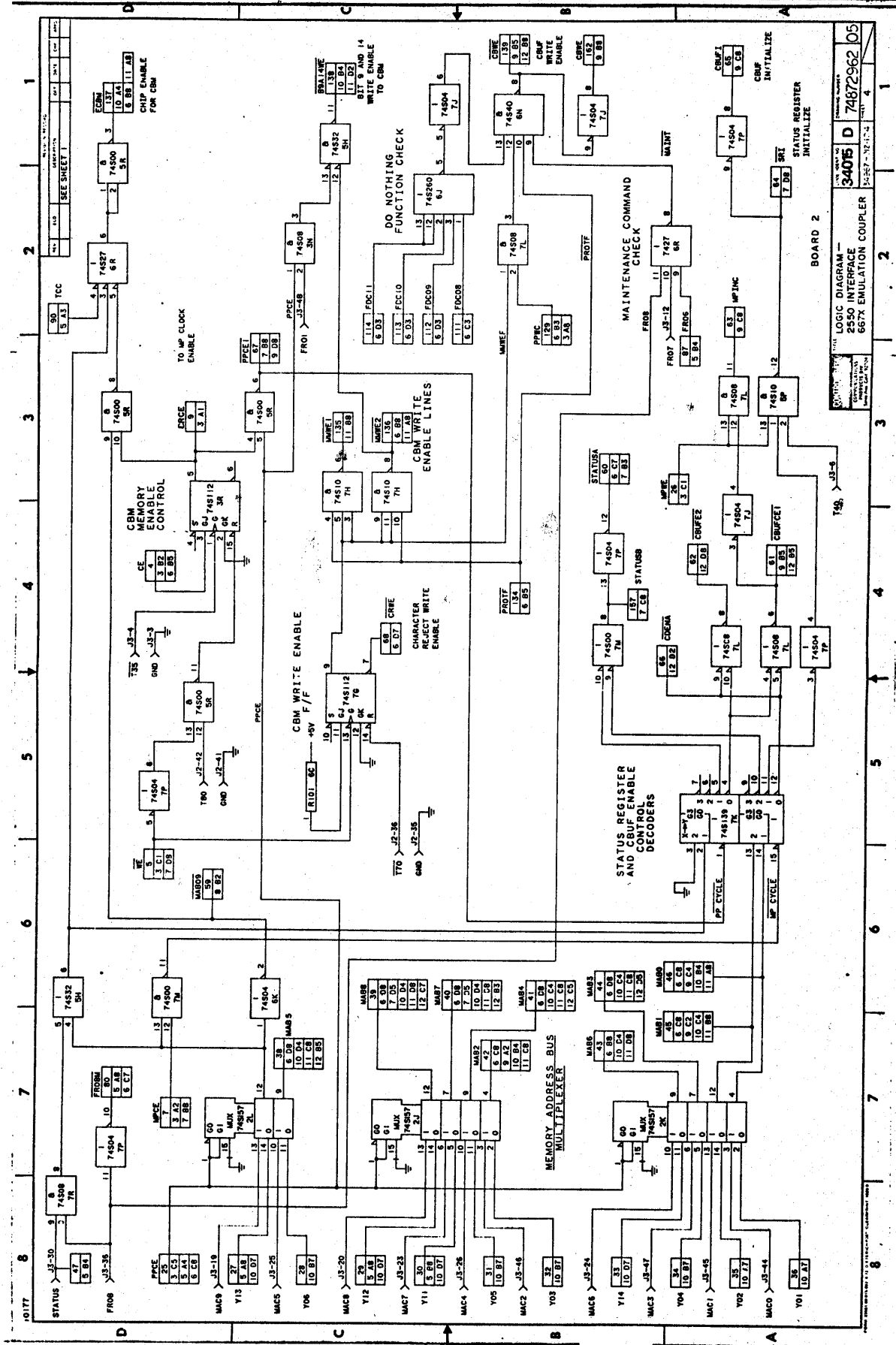
FUNCTION ABBREVIATIONS

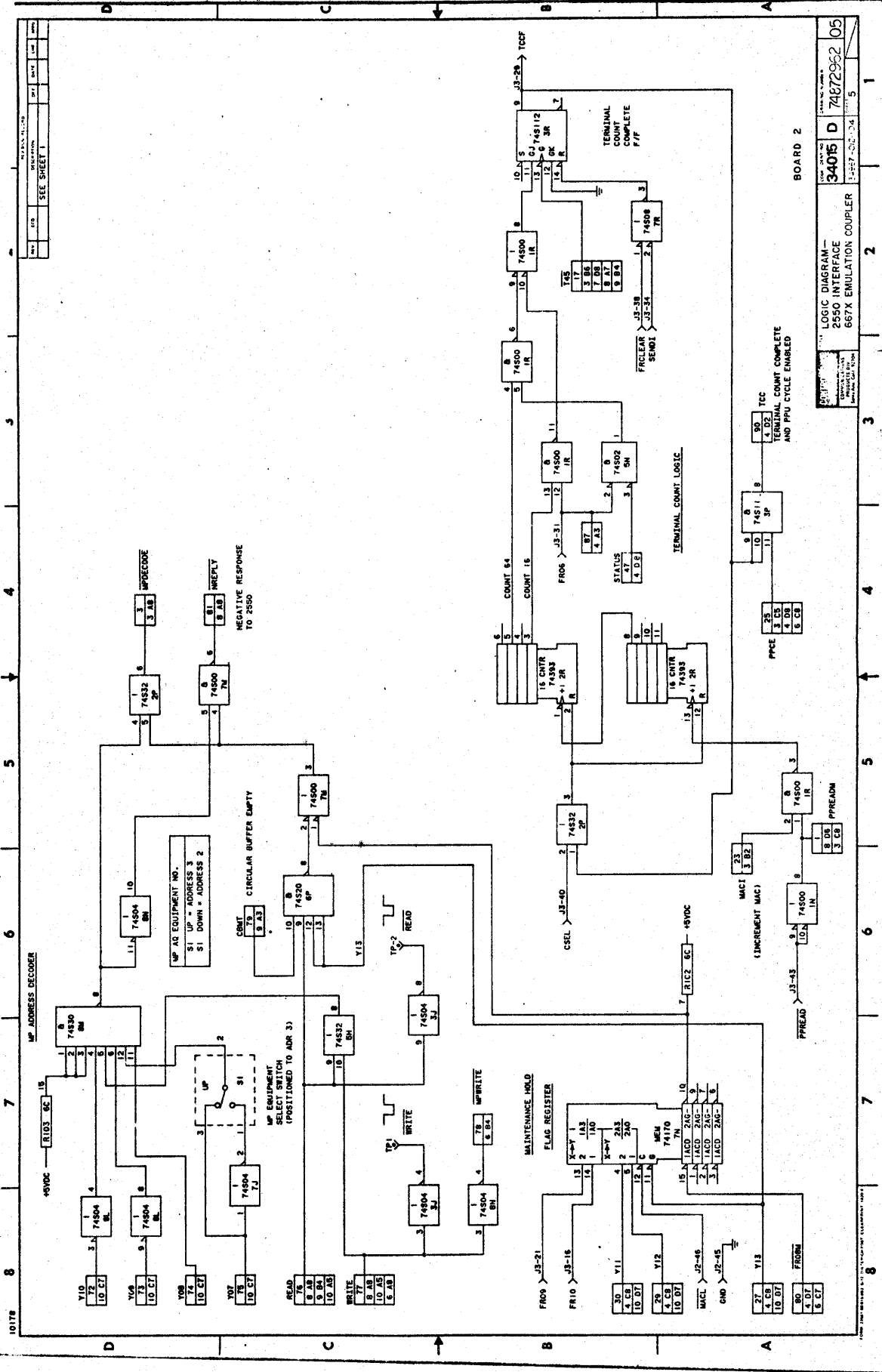
ADD	ARITHMETIC AND LOGIC UNIT
DEC	DECODE
DR	DRIVER
DR	DRIVER AND/OR ENCODER
MEM	MEMORY
MUX	MULTIPLIER
RECV	RECEIVER
REG	REGISTER
SR	SHIFT REGISTER
DEM	DEMULTIPLIER

LOGIC DIAGRAM—
KEY TO SYMBOLS

34015 D 74872962 05





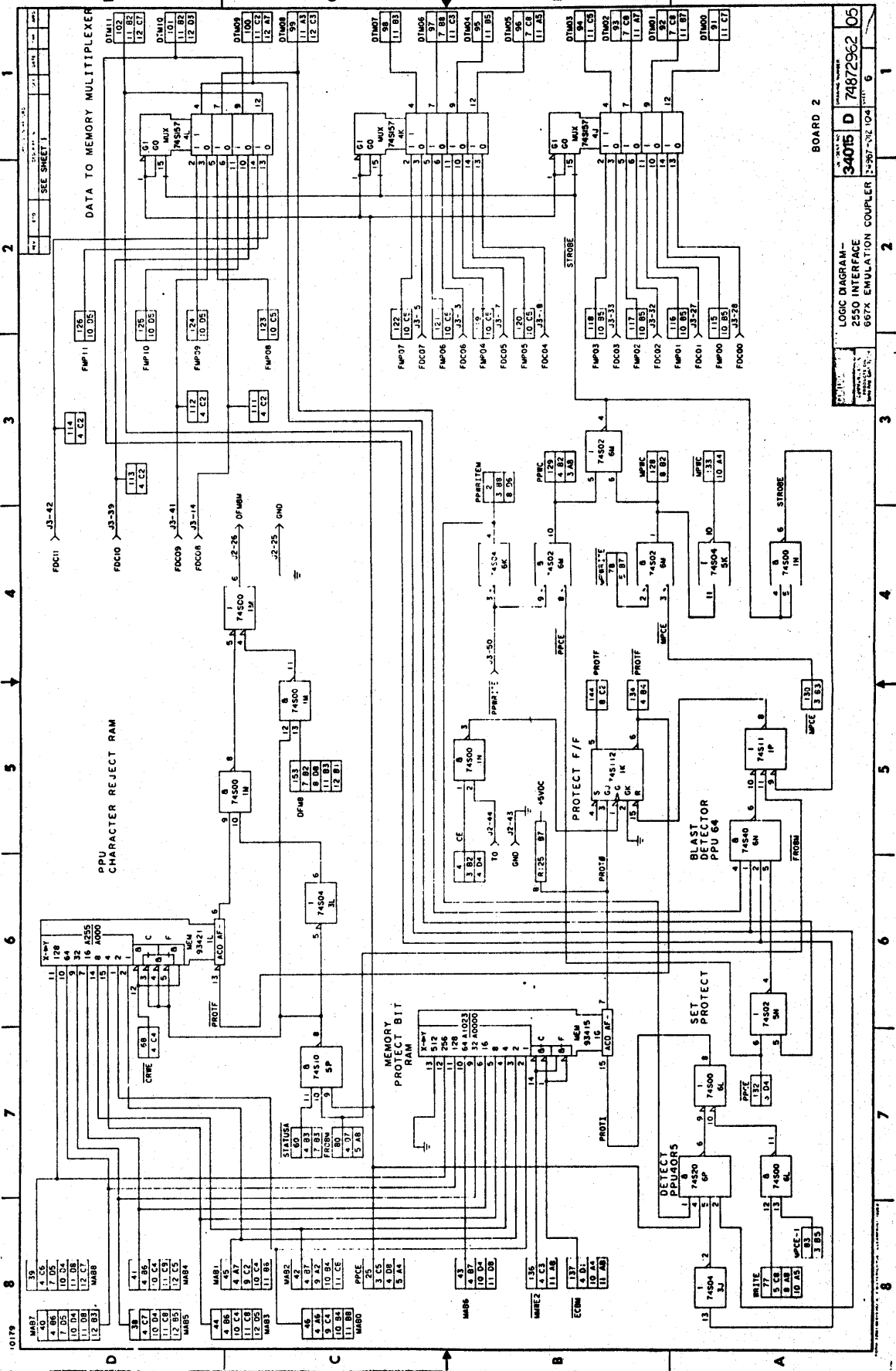


REV.	NO.	DESCRIPTION	DATE	BY

SEE SHEET 1

BOARD 2
34015 D
 LOGIC DIAGRAM
 2550 INTERFACE
 65TK EMULATION COUPLER

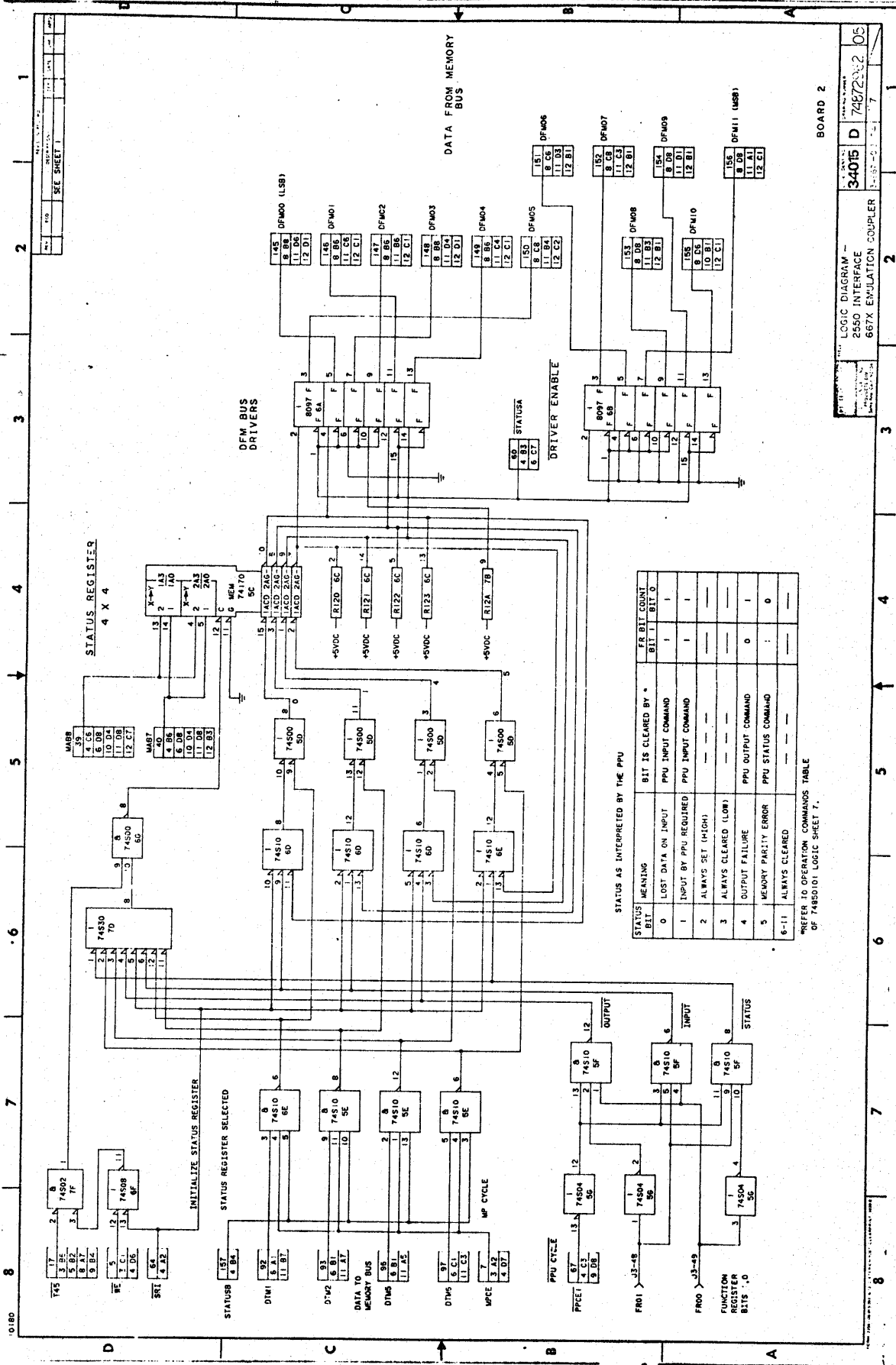
30	Y11
4	CE
10	07
29	Y12
10	07
27	Y13
4	CE
10	07
80	FROM
4	07
6	CT



LOGIC DIAGRAM-
2550 INTERFACE
567A EMULATION COUPLER

BOARD 2

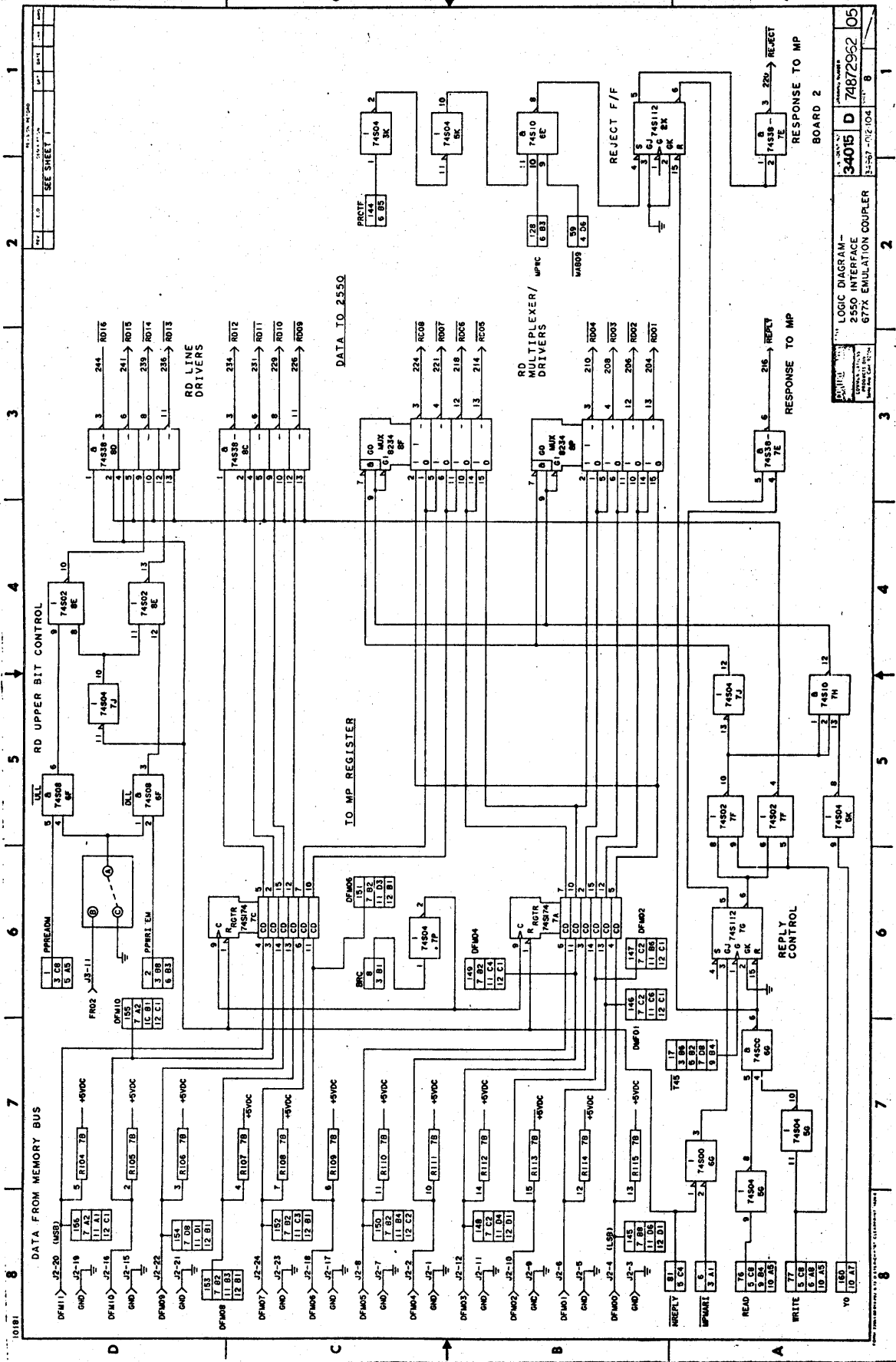
34015 D 74872962 05



LOGIC DIAGRAM -
2550 INTERFACE
667X EMULATION COUPLER

34015 D 748723.2 05

BOARD 2

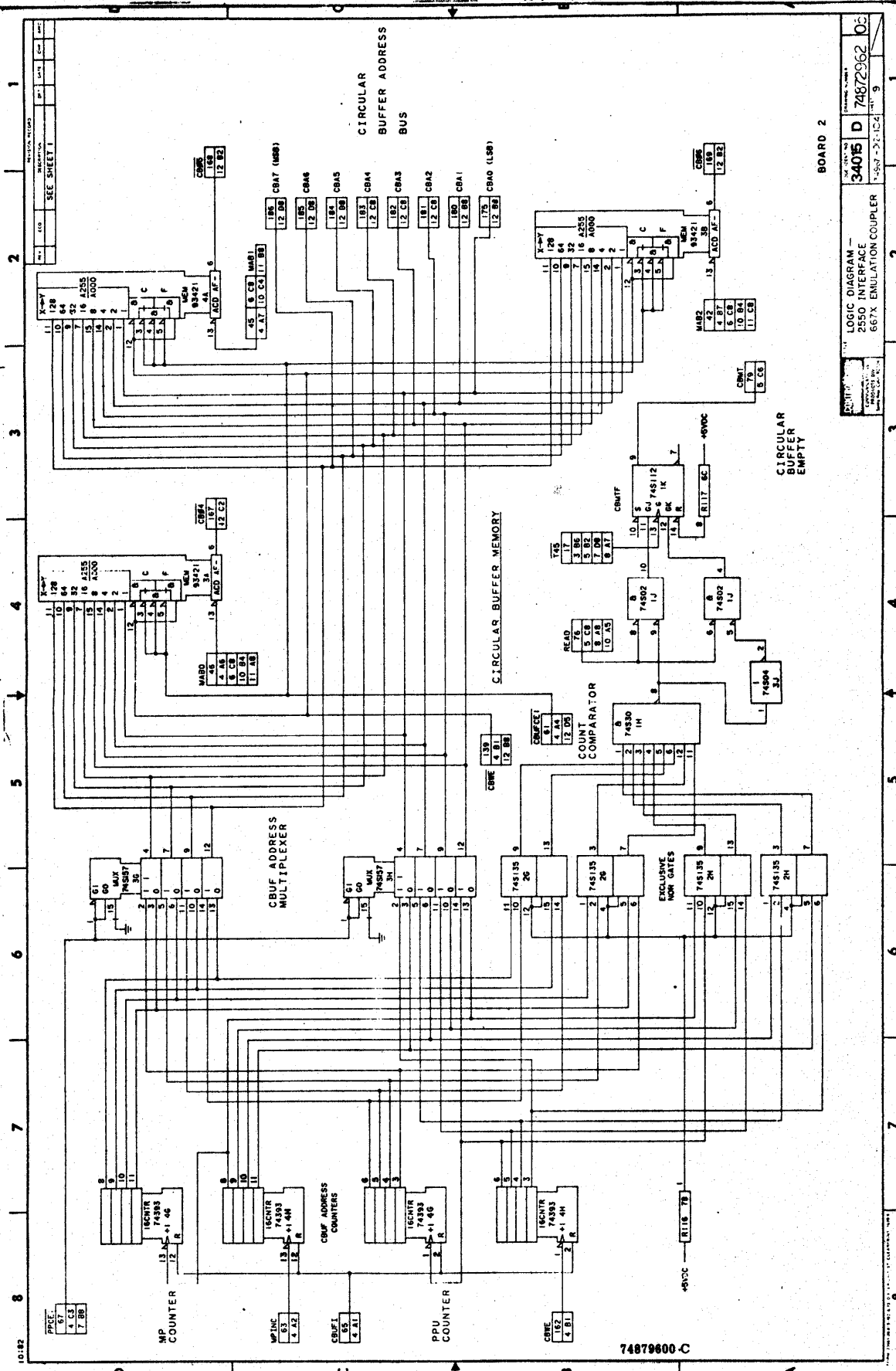


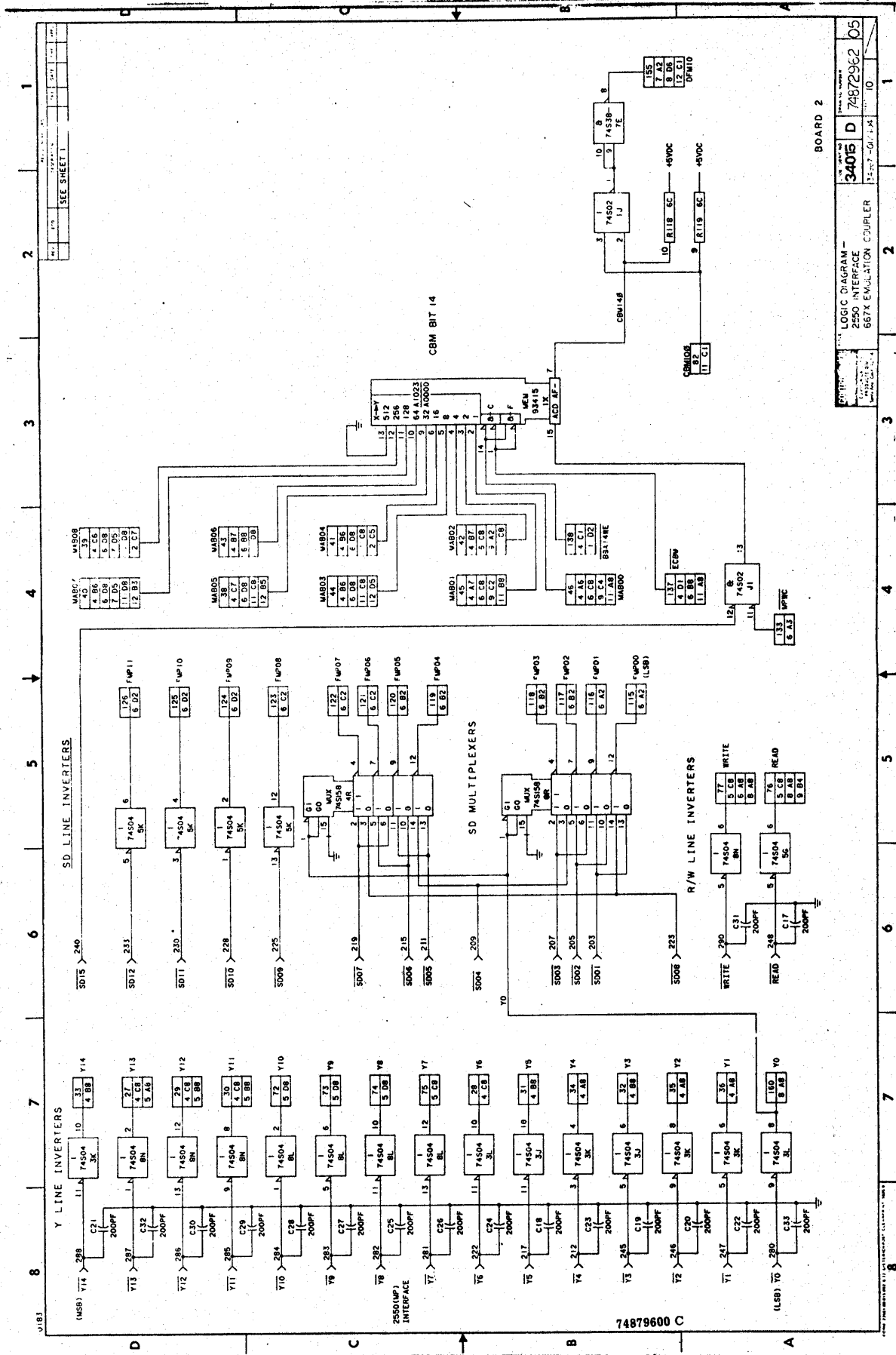
LOGIC DIAGRAM -
2550 INTERFACE
677X EMULATION COUPLER

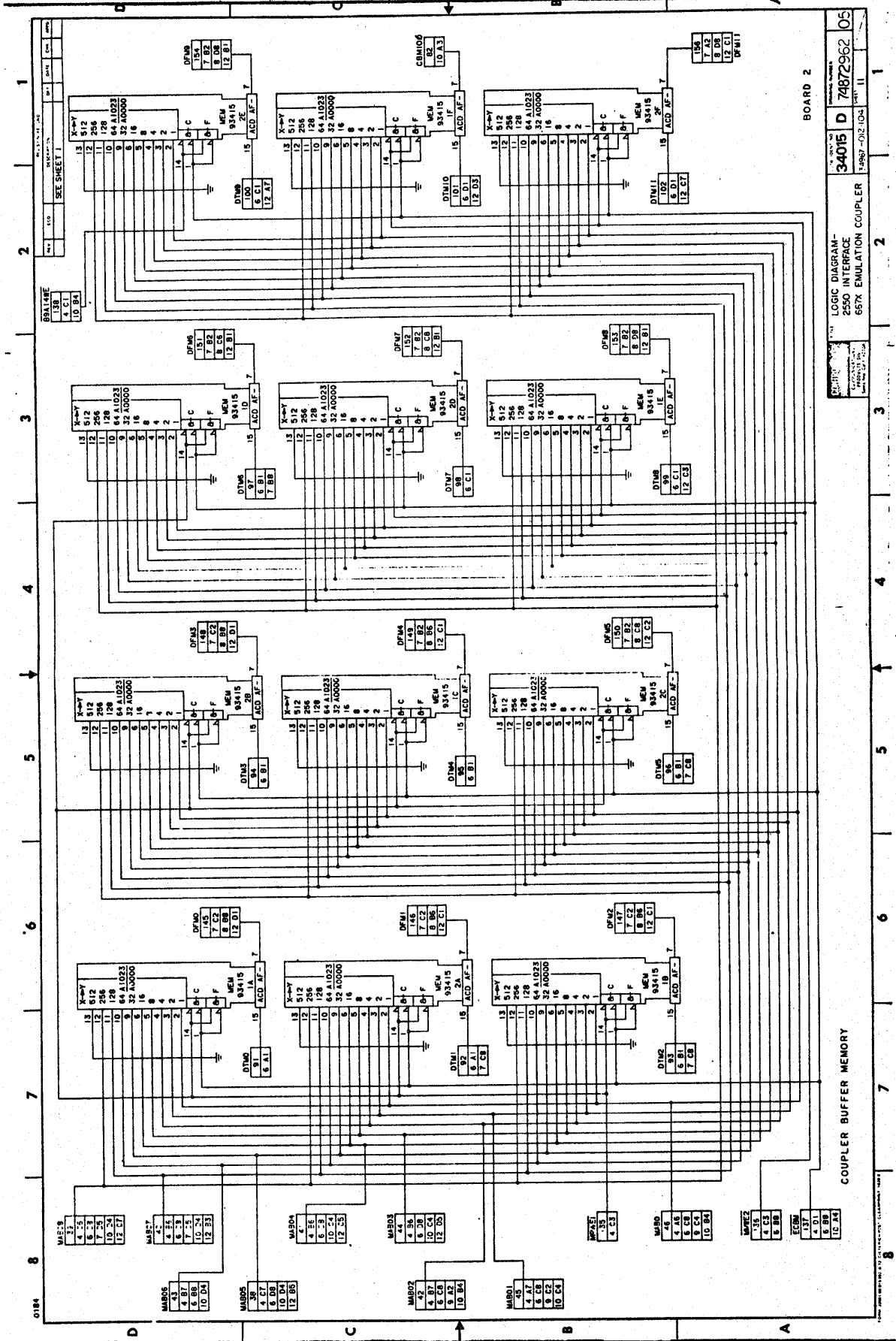
34015 D 74872962 05

BOARD 2

1 2 3 4 5 6 7 8





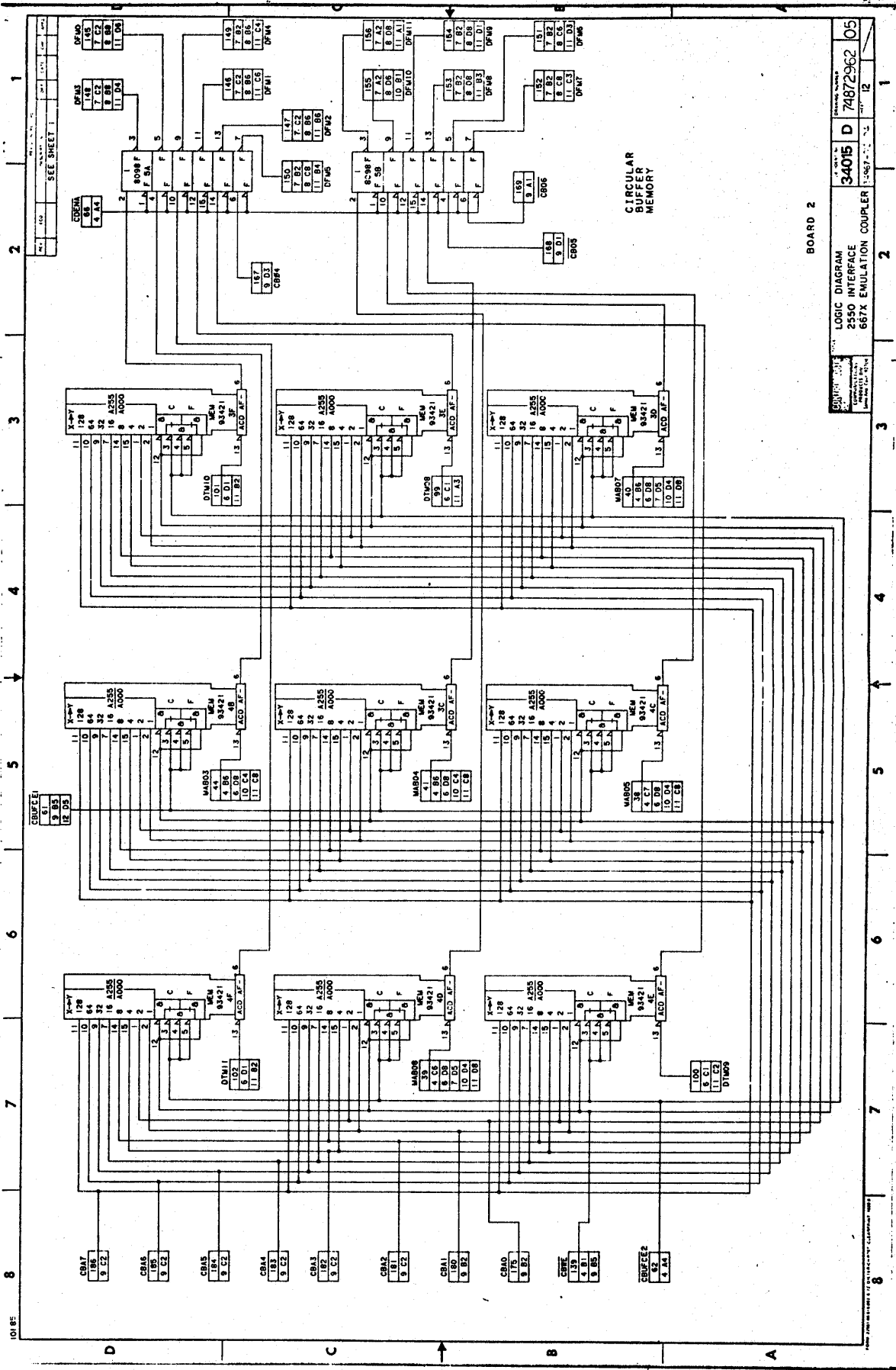


SHEET NO. 1
 SHEET 1
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 74879600 05
 1-8897-02-104
 11

LOGIC DIAGRAM -
 2500 INTERFACE
 65K EMULATION COUPLER

BOARD 2

COUPLER BUFFER MEMORY



BOARD 2

LOGIC DIAGRAM	34015 D	74872962 05
2550 INTERFACE		
887X EMULATION COUPLER		

This section contains preventive maintenance procedures and corrective maintenance aids. When trouble-shooting a defective coupler, refer to theory of operation and logic diagrams. Supplementary maintenance aids are included in appendices.

PREVENTIVE MAINTENANCE

The following paragraphs contain procedures which if performed periodically will minimize subsystem down-time due to coupler malfunctions. Maintain a log to ensure faithful observance of maintenance periods. Wherever maintenance periods are not given, refer to subsystem maintenance procedures.

TEST EQUIPMENT

The following items are needed to maintain the coupler.

1. One spare coupler including items 1 through 4 in table 3-1.
2. Two card extenders, part number 74537300.
3. One hardware maintenance manual, number 74849600.
4. One dual-trace, high-frequency oscilloscope, Tektronix 453 for example.
5. One complete set of subsystem diagnostic tapes, listed in NPU hardware maintenance manual.
6. One set of tools including a DIP clip and an acid brush.

EDGE CONNECTOR CLEANING

1. Remove subsystem power when cleaning edge connectors.
2. Pull the two circuit cards approximately two inches (50 mm) away from their mating connectors.
3. Re-insert the circuit cards until they once again mate with the connectors at the back of the card cage. Thus the connectors are cleaned by the wiping action of the connector contacts.
4. Whenever circuit cards are removed from the card cage, further clean

the edge connectors with a magic-rub eraser. Use a clean acid brush to remove all eraser crumbs before re-inserting the circuit cards.

DIAGNOSTIC PROGRAMS

Perform subsystem diagnostics to check out the coupler at regular intervals. Refer to the NPU hardware maintenance manual for complete checkout procedures using the proper diagnostics. Perform these same checks substituting the spare coupler to ensure the integrity of the spare.

CLOCK ADJUSTMENTS

Annually check the clock adjustments on the synchronizer (figure 2-1) as follows.

1. Connect the channel 1 probe of the oscilloscope to TP-2.
2. Connect the channel 2 probe of the oscilloscope to TP-1.
3. Sync the oscilloscope on channel 1 on the negative-going edge.
4. Adjust R6 until the negative-going edge of channel 2 waveform lags the negative-going edge of channel 1 waveform by 5 ± 2 ns.
5. Verify that the width of the negative pulse of channel 1 is between 25 and 35 ns.

NOTE

This pulse width has been set at the factory. If it is less than 25 ns, it can be increased by changing the setting of S5 (figure 2-2). To do this, it may be necessary to remove power and pull the synchronizer out until S5 is accessible. S5-A through S5-D adjust pulse width. Position A is the narrowest, and each succeeding position increases pulse width by 5 ns. Only one of four positions should be ON.

6. If the clock adjustments cannot be made, check pin 219 of the synchronizer edge connector for a minimum pulse amplitude of 1.3 volts. If this 10 MHz incoming clock amplitude is OK, replace the synchronizer.

CORRECTIVE MAINTENANCE

The following paragraphs contain information that will aid you in trouble-shooting a suspected coupler malfunction. On-site maintenance consists of isolating and replacing a defective circuit card. The defective circuit card is then sent to a repair center where the defect is further isolated and repaired. The repaired circuit card is thoroughly tested before it is returned to the site.

TEST POINTS

The synchronizer has three test points which are accessible from the front of the card cage with the circuit card installed (figure 2-1). The interface has five test points which are similarly accessible (figure 2-2). Both circuit cards also have an accessible ground point. These eight test points are listed and explained.

Synchronizer Test Points

1. Signal $\overline{T75}$ is a 10 MHz clock. TP-1 is on sheet 5 of the logic diagram.
2. Signal $\overline{T70}$ is a 10 MHz clock. TP-2 is on sheet 5 of the logic diagram.
3. Signal \overline{CSEL} goes low for the duration of the function signal when the host has selected the coupler for communications. TP-3 is on sheet 7 of the logic diagram.

Interface Test Points

1. Signal \overline{WRITE} goes low when the processor requests a write memory cycle. TP-1 is on sheet 5 of the logic diagram.
2. Signal \overline{READ} goes low when the processor requests a read memory cycle. TP-2 is on sheet 5 of the logic diagram.
3. Signal \overline{PPCE} goes high when the coupler services a memory cycle request from the host. TP-3 is on sheet 3 of the logic diagram.
4. Signal \overline{MPCE} goes high when the coupler services a memory cycle request from the processor. TP-4 is on sheet 3 of the logic diagram.
5. Signal $\overline{MPDECODE}$ goes high when the processor selects the coupler for communications. TP-5 is on sheet 5 of the logic diagram.

CIRCUIT CARD EXTENSION

1. Remove subsystem power when extending circuit cards.
2. Remove both circuit cards from the card cage at the same time without removing ribbon cables.
3. Install two card extenders in the card cage in place of the circuit cards.
4. Insert both circuit cards into the card extenders at the same time.

CONNECTOR PIN ASSIGNMENTS

A list of signals assigned to the connector pins of the ribbon cables is given in table 6-1. The pin assignments for the edge connectors of the synchronizer is given in table 6-2. Signals assigned to the edge connectors of the interface are listed in table 6-3. Edge connector signals can be accessed at the back of the card cage (figure 3-2).

CIRCUIT CARD SUBSTITUTION

Whenever a circuit card is suspected to be defective, the quickest way to test it is to substitute one of the spare circuit cards. It is recommended that both spare circuit cards be substituted at the same time as an initial test. If the substitution results in a correction of the malfunction, the defect can be further isolated to a single circuit card. Follow installation procedure when substituting the spares. It may not be desirable to further isolate the malfunction at the site, as removal of the synchronizer for any length of time may disturb channel communications. Both suspect circuit cards may be shipped to a repair center with the ribbon cables installed.

SHIPPING CONSIDERATIONS

1. Tag the two boards with a red defective parts tag.
2. Thoroughly describe all fault symptoms on the red tag or attach the description to it.
3. Carefully pack the two circuit boards so that no damage can result during transit.
4. Conform to packaging procedure, CDC 13-004.

TABLE 6-1. RIBBON CABLES CONNECTOR PINS

J1		J2				J3			
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	Spare	1	GND	26	DFM8M	1	GND	26	MAC4
2	Spare	2	DFM4	27	GND	2	POFX	27	FDC1
3	Spare	3	GND	28	FDCL	3	GND	28	FDC0
4	Spare	4	DFM0	29	GND	4	T35	29	TCCF
5	Spare	5	GND	30	T90	5	GND	30	STATUS
6	Spare	6	DFM1	31	GND	6	T40	31	FRO6
7	Spare	7	GND	32	T70	7	GND	32	FDC2
8	Spare	8	DFM5	33	GND	8	T45	33	FDC3
9	Spare	9	GND	34	T0	9	GND	34	SENDI
10	Spare	10	DFM2	35	GND	10	SENDF	35	SPARE
11	Spare	11	GND	36	T70	11	FRO2	36	FRO8
12	Spare	12	DFM3	37	GND	12	FRO7	37	AREADY
13	Spare	13	GND	38	T75	13	FDC6	38	FRCLEAR
14	Spare	14	TDCL	39	GND	14	FDC8	39	FDC10
15	Spare	15	GND	40	SENDE	15	FDC7	40	CSEL
16	Spare	16	DFM10	41	GND	16	FR10	41	FDC9
17	Spare	17	GND	42	T80	17	FDC4	42	FDC11
18	Spare	18	DFM6	43	GND	18	FDC5	43	PPREAD
19	Spare	19	GND	44	T0	19	MAC9	44	MAC0
20	Spare	20	DFM11	45	GND	20	MAC8	45	MAC1
		21	GND	46	MACL	21	FRO9	46	MAC2
		22	DFM9	47	GND	22	MACI	47	MAC3
		23	GND	48	POAX	23	MAC7	48	FRO1
		24	DFM7	49	GND	24	MAC6	49	FR00
		25	GND	50	POEX	25	MAC5	50	PPWRITE

TABLE 6-2. PIN ASSIGNMENTS FOR SYNCHRONIZER

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1		201		27	GND	227	GND
2		202		28	PB09I	228	PB10I
3	+5V	203	+5V	29	PB11I	229	PBAI
4	+5V	204	+5V	30	GND	230	GND
5		205	PB00O	31	PB11I	231	PBFI
6	GND	206	GND	32	PBEI	232	PBPI
7	PB01O	207	PB02O	33	GND	233	GND
8	PB03O	208	PB04O	34	CLK01O	234	CLK10O
9	GND	209	GND	35		235	
10	PB05O	210	PB06O	36		236	
11	PB07O	211	PB08O	37		237	
12	GND	212	GND	38		238	
13	PB09O	213	PB10O	39		239	
14	PB11O	214	PBAO	40		240	
15	GND	215	GND	41		241	
16	PBIO	216	PBFO	42		242	
17	PBEO	217	PBPO	43		243	
18	GND	218	GND	44		244	
19	CLK01I	219	CLK10I	45		245	
20		220	PB00I	46		246	
21	GND	221	GND	47		247	
22	PB01I	222	PB02I	48		248	
23	PO03I	223	PB04I	49		249	
24	GND	224	GND	50		250	
25	PB05I	225	PB06I	51		251	
26	PB07I	226	PB08I				

TABLE 6-2. PIN ASSIGNMENTS FOR SYNCRHONIZER (contd)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
52		252		78	PO11I	278	POAI
53		253		79	GND	279	GND
54		254		80	PO12I	280	POFI
55		255		81	POEI	281	POPI
56		256		82	GND	282	GND
57		257		83	POMCI	283	POFNI
58		258		84		284	PO000
59		259		85	GND	285	GND
60		260		86	PO010	286	PO020
61		261		87	PO030	287	PO040
62		262		88	GND	288	GND
63		263		89	PO050	289	PO060
64		264		90	PO070	290	PO080
65		265		91	GND	291	GND
66		266		92	PO090	292	PO100
67		267		93	PO110	293	POAO
68		268		94	GND	294	GND
69		269	PO00I	95	POIO	295	POFO
70	GND	270	GND	96	POEO	296	POPO
71	PO01I	271	PO02I	97	GND	297	GND
72	PO03I	272	PO04I	98	POMCO	298	POFNO
73	GND	273	GND	99		299	
74	PO05I	274	PO06I	100		300	
75	PO07I	275	PO08I	101	GND	301	GND
76	GND	276	GND	102	GND	302	GND
77	PO09I	277	PO10I				

TABLE 6-3. PIN ASSIGNMENTS FOR INTERFACE

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	+5V	201	+5V	27		227	
2	+5V	202	+5V	28		228	$\overline{\text{SD10}}$
3		203	$\overline{\text{SD01}}$	29		229	$\overline{\text{RD10}}$
4		204	$\overline{\text{RD01}}$	30		230	$\overline{\text{SD11}}$
5		205	$\overline{\text{SD02}}$	31		231	$\overline{\text{RD11}}$
6		206	$\overline{\text{RD02}}$	32		232	
7		207	$\overline{\text{SD03}}$	33		233	$\overline{\text{SD12}}$
8		208	$\overline{\text{RD03}}$	34		234	$\overline{\text{RD12}}$
9		209	$\overline{\text{SD04}}$	35		235	
10		210	$\overline{\text{RD04}}$	36		236	$\overline{\text{RD13}}$
11		211	$\overline{\text{SD05}}$	37		237	
12		212	$\overline{\text{Y04}}$	38		238	
13		213		39		239	$\overline{\text{RD14}}$
14		214	$\overline{\text{RD05}}$	40		240	$\overline{\text{SD15}}$
15		215	$\overline{\text{SD06}}$	41		241	$\overline{\text{RD15}}$
16		216	$\overline{\text{REPLY}}$	42		242	
17		217	$\overline{\text{Y05}}$	43		243	
18		218	$\overline{\text{RD06}}$	44		244	$\overline{\text{RD16}}$
19		219	$\overline{\text{SD07}}$	45		245	$\overline{\text{Y3}}$
20		220	$\overline{\text{REJECT}}$	46		246	$\overline{\text{Y2}}$
21		221	$\overline{\text{RD07}}$	47		247	$\overline{\text{Y1}}$
22		222	$\overline{\text{Y06}}$	48		248	$\overline{\text{READ}}$
23		223	$\overline{\text{SD08}}$	49		249	
24		224	$\overline{\text{RD08}}$	50		250	
25		225	$\overline{\text{SD09}}$	51		251	
26		226	$\overline{\text{RD09}}$				

TABLE 6-3. PIN ASSIGNMENTS FOR INTERFACE (contd)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
52		252		78		278	
53		253		79		279	
54		254		80		280	$\overline{Y0}$
55		255		81		281	$\overline{Y07}$
56		256		82		282	$\overline{Y08}$
57		257		83		283	$\overline{Y09}$
58		258		84		284	$\overline{Y10}$
59		259		85		285	$\overline{Y11}$
60		260		86		286	$\overline{Y12}$
61		261		87		287	$\overline{Y13}$
62		262		88		288	$\overline{Y14}$
63		263		89		289	$\overline{Y15}$
64		264		90		290	\overline{WRITE}
65		265		91		291	
66		266		92		292	
67		267		93		293	
68		268		94		294	
69		269		95		295	
70		270		96		296	
71		271		97		297	
72		272		98		298	
73		273		99		299	
74		274		100		300	
75		275		101	GND	301	GND
76		276		102	GND	302	GND
77		277					



PARTS DATA

7

This section contains the assembly drawings
and parts lists for the Emulation Coupler
and Cable Set.

DWN	T. PARNAKIAN	2-78	CONTROL DATA	TITLE	TOP ASSEMBLY 667X COUPLER	REFIX	DOCUMENT NO.	74873722	REV	A																		
ENG	J. HURST	4-13-77	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	FIRST USED ON	DY159-A	35398-111-504	SHEET		1 OF 1																			
MFG			CODE IDENT																									
APP			34015																									
SHEET REVISION STATUS						REVISION RECORD																						
<table border="1"> <tr> <th>REV</th> <th>ECO</th> <th>DESCRIPTION</th> <th>DRFT</th> <th>DATE</th> <th>APP</th> </tr> <tr> <td>03</td> <td>06612</td> <td>INITIAL RELEASE</td> <td>PL</td> <td>4-18-77</td> <td></td> </tr> <tr> <td>A</td> <td>08063</td> <td>CL. A RELEASE CBM</td> <td>TP</td> <td>2-2-78</td> <td></td> </tr> </table>						REV	ECO	DESCRIPTION	DRFT	DATE	APP	03	06612	INITIAL RELEASE	PL	4-18-77		A	08063	CL. A RELEASE CBM	TP	2-2-78						
						REV	ECO	DESCRIPTION	DRFT	DATE	APP																	
						03	06612	INITIAL RELEASE	PL	4-18-77																		
A	08063	CL. A RELEASE CBM	TP	2-2-78																								
<p>INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA</p> <p>AA6030</p>																												
NOTES:																												
						PL 74873722																						
						DETACHED LISTS																						

FORM 19246-01-016-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.



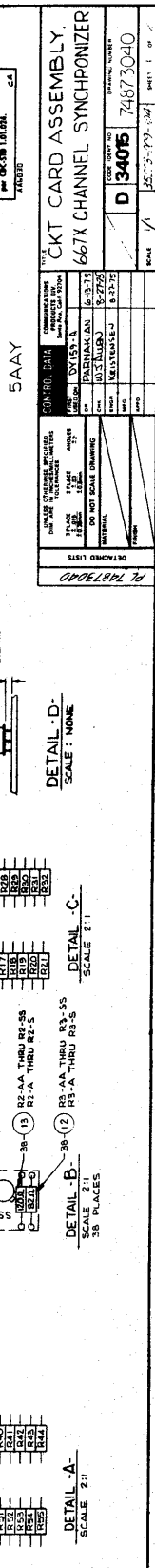
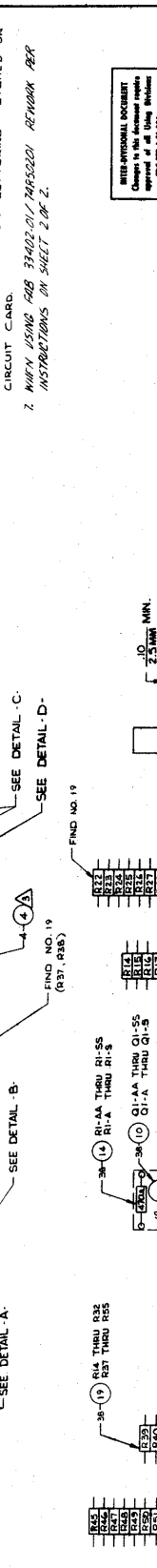
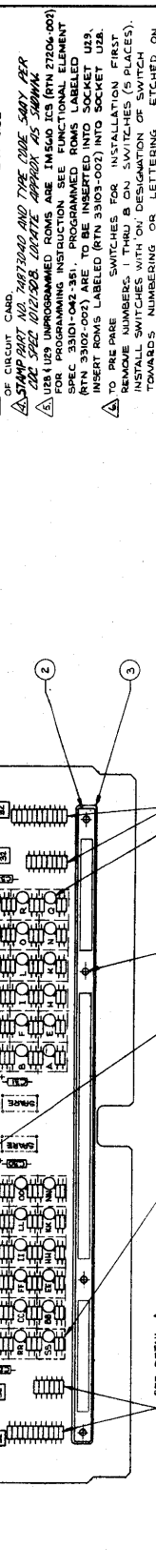
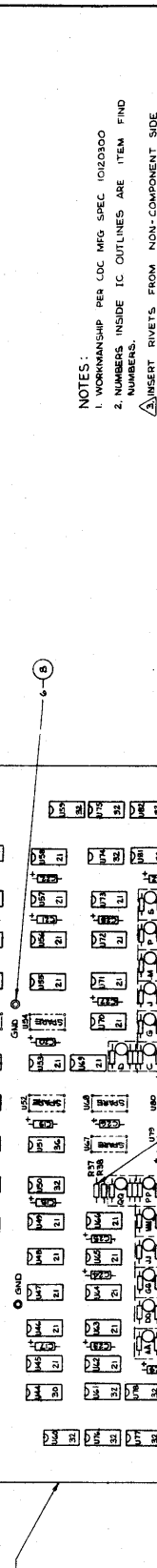
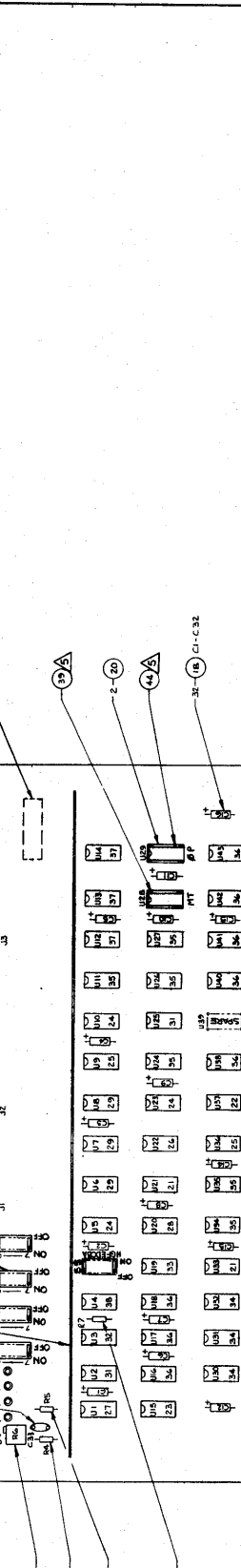
ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74873722	A	CLA	A	667X COUPLER	DM	2551	02/04/78	02/04/78	1/1	MF
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER	
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNITS MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC
3	C	74843700	2		PC CBL ASSY FLAT 50 CONDUCTOR	IN				N
4	C	74845800	1		PC CBL ASSY FLAT 20 CONDUCTOR	IN				N
5	A	74870828	1		PC DAISY CHAINED 667X EMULATION	IN				N
2	D	74872963	1		PC COUPLER 667X EMULTR 2550 INTRF	IN				N
1	D	74873040	1		PC 667X CHANNEL SYNC	IN				N
6	A	88964500	1		PC JUMPER INTERNAL 5V CYBER COUPL	IN			AYM4	N
<p>NUMBER OF LINE ITEMS = 6 HIGHEST FIND NUMBER = 6</p>										
<p>PROJECT ENGINEER ARDEN HILLS</p>										

AA 2709 REV. 7-78

DATE	TIME	BY	DESCRIPTION	REV.	DATE	BY
			PRELIMINARY RELEASE			
			BOARD DETAIL - C			
			INITIAL RELEASE			
			SEE EGO			
			INITIAL RELEASE			
			INITIAL RELEASE			
			REVISE PARTS LIST			
			ADD NOTE #4			



NOTES:

- WORKMANSHIP PER CDC MFG SPEC 1012300
- NUMBERS INSIDE IC OUTLINES ARE ITEM FIND NUMBERS.
- INSERT RIVETS FROM NON-COMPONENT SIDE OF CIRCUIT CARD.
- STAMP PART NO. 7417340 AND THE DATE 5/27/67 PER THE SPEC 1012300. LOCATE APPROX AS SHOWN.
- FOR 168 UNPROGRAMMED ROMS ARE IM540 IC'S (RTN 27206-002) INSTRUCTIONS FOR PROGRAMMING THESE FUNCTIONAL ELEMENTS SPEC. 33101-042-381. PROGRAMMING ROMS LABELLED U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100.
- TO PREPARE SWITCHES FOR INSTALLATION FIRST REMOVE NUMBERS 1 THRU 8 ON SWITCHES (5 PLACES). INSTALL SWITCHES WITH ON DESIGNATION OF SWITCH CIRCUIT CARDS NUMBERING OR LETTERING ETCHED ON CIRCUIT CARDS.
- WHEN USING TAB 33402-017, MAR-20201 REMOVE PER INSTRUCTIONS ON SHEET 2-04-2.

INTERNATIONAL SOCIETY
Changes in this document require
approval by the following
per CK-578 1.0.0.0. 2.4

5AAY

667X CHANNEL SYNCHRONIZER
D 3405 74873040

REV.	DESCRIPTION	DATE	BY
1	INITIAL RELEASE	5-27-67	
2	REVISE PARTS LIST	5-27-67	
3	ADD NOTE #4	5-27-67	

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74R73040	C	CLA	D	667X CHANNEL SYNCH	DM	2551	02/04/78	10/04/78	1 / 2
ASSEMBLY NUMBER	REV	CLASS	DW 52	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF
15003-009

FIND NUMBER	DW 52	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH	OR N
24	A	15109200	300	PC	IC WFX INVERTER TYPE 74S04	OUT	00A210	06/20/78	PPP5	N	N
31	A	15109400	200	PC	IC DUAL J-K EDGE TR FF 74S112	OUT	00A210	06/20/78	PPP5	N	N
30	A	15109700	100	PC	I.C. DUAL D-TYPE FDRF TRIG F.F	OUT	00A210	06/20/78	PPP5	N	N
27	A	15110100	100	PC	INT CKT 7413	IN			PPP4	N	N
32	A	15115800	1200	PC	DRIVER, QUAD 2-INPIT NOR LTNE	IN			PPP5	N	N
34	A	15117400	300	PC	I-C TTL AMUX 2-1	IN			PPP5	N	N
22	A	15125300	100	PC	MICROCIRCUIT	IN			PPP5	N	N
23	A	15128800	100	PC	INTEGRATED CIRCUIT	IN			PPP4	N	N
36	A	15132000	900	PC	I.C. 74S175	IN			PPP5	N	N
35	A	15138800	600	PC	IC 74S174J	IN			PPP4	N	N
33	A	15142500	100	PC	I-C DECODER 74S13A	IN			PPP4	N	N
27	A	15150400	300	PC	MICROCIRCUIT TYPE 94S16 4 BIT	IN			PPP4	N	N
15	A	15150900	200	PC	I.C. 74S08	OUT	00A210	06/20/78	PPP4	N	N
31	A	15158600	200	PC	I C 74S112	IN	00A210	06/20/78	PPP4	N	N
29	A	15161400	300	PC	I.C. 74S40	IN	00A210	06/20/78	PPP4	N	N
25	A	15163600	200	PC	IC 74S08	IN	00A210	06/20/78	PPP4	N	N
19	C	24500023	3800	PC	RES FXD .25W 22 OHMS	IN			PPP5	N	N
12	C	24500037	3800	PC	RES FXD .25W 82 OHMS	IN			PPP5	N	N
16	C	24500039	100	PC	RES FXD .25W 100 OHMS	IN			PPP5	N	N
13	C	24500041	3800	PC	RES FXD .25W 120 OHMS	IN			PPP5	N	N
15	C	24500050	100	PC	RES FXD .25W 300 OHMS	IN			PPP4	N	N
14	C	24500055	3800	PC	RES FXD .25W 470 OHMS	IN			PPP5	N	N
43	C	24500065	100	PC	RES FXD .25W 1200 OHMS	IN			PPP5	N	N
18	C	24505229	3200	PC	CAP.FXD SOL TA 35V 1.0UF 10PCT	IN			PPP4	N	N
45	C	24548306	1800	IN	WIRE,ELECT.24 GA,PVC,UL,GRN	IN			PPP5	N	N
10	C	24561900	3800	PC	TRANSISTOR SILICON NPN,PLANAR	IN			PPP5	N	N
8	A	38807901	500	PC	TERMINAL HOLLOW STNRIE END.105	IN			PPP3	N	N
40	A	39996406	500	PC	SWTCH,ROCKER-DIAL,RPST 9POSNS	IN			PPP4	N	N
21	A	50254600	2200	PC	TTL QUAD 2 INPUT NAND 74S00	OUT	00A210	06/20/78	PPP5	N	N
26	A	50254700	100	PC	INTEGRATED CIRCUIT 74S10	OUT	00A210	06/20/78	PPP4	N	N
29	A	50254800	300	PC	IC DUAL-4 INPUT PMS-NAND	OUT	00A210	06/20/78	PPP4	N	N
28	A	50254900	100	PC	I.C. DUAL 4-IN NAND (74S20)	OUT	00A210	06/20/78	PPP4	N	N
1	D	74850201	100	PC	667X EMULATOR SYNCH FAB	IN			PYP4	N	N
41	A	748A2000	OFF	PC	667X EMULATOR COUPLER ADDRESS	IN			RFE4	N	N
44	A	748A2001	100	PC	PROGRAMED PROM OPROM OPERATI	IN			PPP4	N	N
39	A	748A2002	100	PC	PROGRAMED PROM MTDOM MAINTEN	IN			PPP4	N	N

PROJECT ENGINEER ARDEN WILK

AA 2708 REV. 7-78

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74R73040	C	CLA	D	667X CHANNEL SYNCH	DM	2551	02/04/78	10/04/78	2 / 2
ASSEMBLY NUMBER	REV	CLASS	DW 52	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF

FIND NUMBER	DW 52	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH	OR N
42	D	74R73041	OFF	PC	667X EMULATOR SYNCH LOGIC	IN			RFE4	N	N
11	A	84605207	100	PC	POT, TRIM, CER, 2K OHMS	IN			PPP4	N	N
17	A	84996709	100	PC	CAP.CER 100V 56 PF	IN			PPP4	N	N
4	A	88812400	400	PC	RIVET-SEMI-TUBULAR,RRS .312 LG	IN			PPP3	N	N
9	D	88875500	100	PC	BUS BAR (13 IN)	IN			PPP5	N	N
24	A	88883700	300	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN	00A210	06/20/78	PPP5	N	N
26	A	88884200	100	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN	00A210	06/20/78	PPP5	N	N
21	A	88884500	2200	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN	00A210	06/20/78	PPP5	N	N
28	A	88885300	100	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN	00A210	06/20/78	PPP5	N	N
2	D	88895400	100	PC	STIFFENER-PC BOARD (CASTING)	IN			PPP5	N	N
3	C	88895500	100	PC	INSULATOR-CARD STIFFENER	IN			PPP5	N	N
30	A	88923000	100	PC	IC 74S74 TTL DUAL D EDGE F/F	IN	00A210	06/20/78	PPP5	N	N
20	C	94260301	200	PC	SOCKET I.C.	IN			PPP4	N	N
38	A	94262302	100	PC	DELAYLINE TAPPED	IN			PPP4	N	N
5		94369803	200	PC	HEADER RT ANGL 50 PAS	IN			PPP4	N	N
6		94369805	100	PC	HEADER RT ANGL 20 PAS	IN			PPP4	N	N

NUMBER OF LINE ITEMS = 52
HIGHEST FIND NUMBER = 45

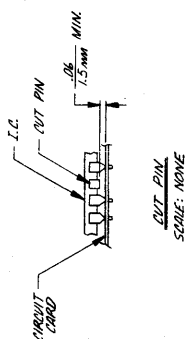
PROJECT ENGINEER ARDEN WILK

AA 2708 REV. 7-78



REV	NO	DATE	BY	CHKD	APP'D

REVISIONS
 1. SEE SHEET 1



1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

I.C. NOS.	PIN NOS.
2N	4
2N	5

2. ADD THE FOLLOWING JUMPERS:

FROM	TO	PIN NOS.
1	2	4
1	3	5
2	3	4
3	4	5
4	5	4
5	6	5
6	7	6
7	8	7
8	9	8
9	10	9
10	11	10
11	12	11
12	13	12
13	14	13
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96	97	96
97	98	97
98	99	98
99	100	99

CONTROL DATA	TYPE	34016	DATE	11/27/63	REV	A
CIRCUIT BOARD ASSEMBLY -						
CIRCUIT BOARD - 2500 INTERFACER						
QUANTITY	34016	DATE	11/27/63	REV	A	

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74872963	D	CLA	D	COUPLER 667X EMULTR 2550 INTRF	DM	2551	02/06/78	10/09/78	1 / 2
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF
24765-009

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	NC	ON
25	A	15104000	200	PC	4X4 REGISTER FILE,16PIN	IN			PPP4		N
22	C	15106800	200	PC	IC GATE	IN			PPP4		N
9	A	15109200	1100	PC	IC HEX INVERTER TYPF 74S04	OUT	008210	062678	PPP5		N
12	A	15109400	900	PC	IC DUAL J-K EDGE TR FF 74S112	OUT	008210	062678	PPP5		N
26	A	15114900	1400	PC	IC TTL 1024 BIT RAM 93415	IN			PPP5		N
10	A	15116400	200	PC	IC GATE TPL 3 INP POS-AND	IN			PPP5		N
30	A	15117200	100	PC	1-C TTL DCRD2	IN			PPP4		N
17	A	15117400	800	PC	1-C TTL 8MUX 2-1	IN			PPP5		N
27	A	15117500	200	PC	INTEGRATED CIRCUIT	IN			PPP4		N
20	A	15125100	100	PC	1-C TTL2 5I-1A NOR 2265 D1C14	IN			PPP5		N
13	A	15125300	500	PC	MICROCIRCUIT	IN			PPP5		N
15	A	15125400	400	PC	I.C. 74S30	IN			PPP5		N
18	A	15132100	1300	PC	IC TTL RAM 256 BIT R2506	IN	008411	092678			N
29	A	15138800	200	PC	IC 74S174J	IN			PPP4		N
33	A	15140400	200	PC	IC 8097, 939 TTL TRI-ST HEX	IN			PPP5		N
31	A	15150900	400	PC	I.C. 74S08	OUT	008210	062678	PPP4		N
28	A	15151100	300	PC	I.C. 74S38	IN			PPP5		N
23	A	15151800	200	PC	IC 74S135	IN			PPP4		N
24	A	15154500	200	PC	74368/8098 HEX BUS DRIVERS	IN			PPP4		N
14	A	15154800	200	PC	IC 74S32	IN			PPP4		N
12	A	15158600	900	PC	I C 74S112	IN	008210	062678	PPP4		N
21	A	15160000	300	PC	IC-74393 DUAL 4 BIT BIN COUNTER	IN			PPP5		N
34		15160100	200	PC	I.C. 8234 TYPE	IN			PPP4		N
19	A	15161400	100	PC	I.C. 74S40	IN	008210	062678	PPP4		N
31	A	15163600	400	PC	IC 74S08	IN	008210	062678	PPP4		N
45	C	18563105	300	IN	WIRE ELEC 25 AWG INSULATED	IN			PPP2		N
41	C	24548306	200	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
40	A	25186108	300	PC	TERMINAL, BIFURCATED L=.115	IN			PPP4		N
7	A	38807901	800	PC	TERMINAL HOLLOW SINGLE END,105	IN			PPP3		N
39	A	38836933	1700	PC	CAP SILVERED MICA 200PF 500V	IN			PPP4		N
11	A	50254600	900	PC	TTL QUAD 2 INPUT NAND 74S00	OUT	008210	062678	PPP5		N
16	A	50254700	600	PC	INTEGRATED CIRCUIT 74S10	OUT	008210	062678	PPP4		N
19	A	50254800	100	PC	IC DUAL-4 INPUT POS-NAND	OUT	008210	062678	PPP4		N
32		50254900	200	PC	I.C. DUAL 4-IN NAND (74S20)	OUT	008210	062678	PPP4		N
36	A	62012906	100	PC	RES MOD DUAL 1K OHMS 125MW	IN			PPP4		N
35	A	62012907	100	PC	RES MOD DUAL 2K OHMS 125MW	IN			PPP4		N

PROJECT ENGINEER ARDEN HILLS

AA 2709 REV. 7-78

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74872963	D	CLA	D	COUPLER 667X EMULTR 2550 INTRF	DM	2551	02/06/78	10/09/78	2 / 2
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF

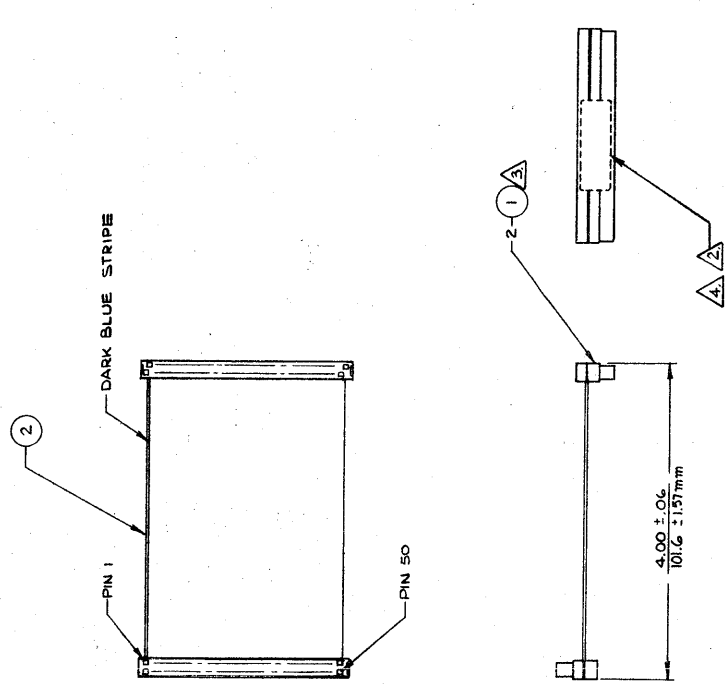
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	NC	ON
37	A	72003528	200	PC	CAPACITOR 100 UF 10V	IN			PPP4		N
1	D	74846201	100	PC	667X EMULATOR 2550 INTFC FAB	IN			PPP4		N
38	A	74870616	1400	PC	CAPACITOR CER DISC .01UF 25VDC	IN			PPP5		N
43	D	74872964	REF	PC	667X EMULATOR 2550 INTFC LOGIC	IN			RFE4		N
6	A	88812400	400	PC	RIVET-SEMI-TUBULAR,RRS .312 LG	IN			PPP3		N
44	D	88875500	100	PC	BUS BAR (13 IN)	IN			PPP5		N
9	A	88883700	1000	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN	008454	100478	PPP5		N
16	A	88884200	600	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN	008210	062678	PPP5		N
11	A	88884500	900	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN	008210	062678	PPP5		N
32	A	88885300	200	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN	008210	062678	PPP5		N
4	D	88895400	100	PC	STIFFENER-PC BOARD (CASTING)	IN			PPP5		N
5	C	88895500	100	PC	INSULATOR-CARD STIFFENER	IN			PPP5		N
3		94263907	100	PC	SWITCH TOGGLE	IN			PPP4		N
2		94369803	200	PC	HEADER RT ANGL 50 POS	IN			PPP4		N
8		94369805	100	PC	HEADER RT ANGL 20 POS	IN			PPP4		N

NUMBER OF LINE ITEMS = 51
HIGHEST FIND NUMBER = 45

PROJECT ENGINEER ARDEN HILLS

AA 2709 REV. 7-78

SHEET REVISION STATUS		REVISION RECORD				
REV	ECD	DESCRIPTION	DFT	DATE	CHK	APPD
00	02/8/73	INITIAL RELEASE	TP	6-24-75	M	M
01	0808Z	REVISED PL ONLY	TP	11-21-77	M	M
A	0806Z	CLASS 'A' RELEASE	TP	1-27-78	M	M
B	0950Z	REVISED NOTE 4	TP	11-7-78	M	M



- NOTES:
1. WORKMANSHIP PER CDC MFG SPEC 10120300
 2. LOCATE APPROX AS SHOWN
 3. ASSEMBLE ITEM 2 TO ITEM 1 USING 3M NO. 3440 PRESS RTN 18544 WITH 3M NO. 3425-0000 RTN 27614 LOCATOR PLATE OR EQUIVALENT TOOLING.
 4. MARK PER CDC SPEC 1012150B WITH PART NO. 74843700 AND REVISION.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
748030
CA

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS 3 PLACE TOLERANCE ± 0.005 ± 0.30mm		CONTROL DATA		COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	
DO NOT SCALE DRAWING		DESIGNER	DATE	REV	DESCRIPTION
MATERIAL		CHK	6-24-75	01	INITIAL RELEASE
FINISH		ENGR	8-15-76	A	CLASS 'A' RELEASE
DETACHED LISTS		MFG	9-15-76	B	REVISED NOTE 4
PL 74843700		APPD			
TITLE		CABLE ASSY, FLAT 50-CONDUCTOR			
DRAWING NUMBER		C 34015 74843700			
SCALE		1/1			
SHEET		1 OF 1			

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74843700	B	CLA	C	CBL ASSY FLAT 50-CONDUCTOR	DM	2551	02/04/78	11/06/78	1 / 1
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF

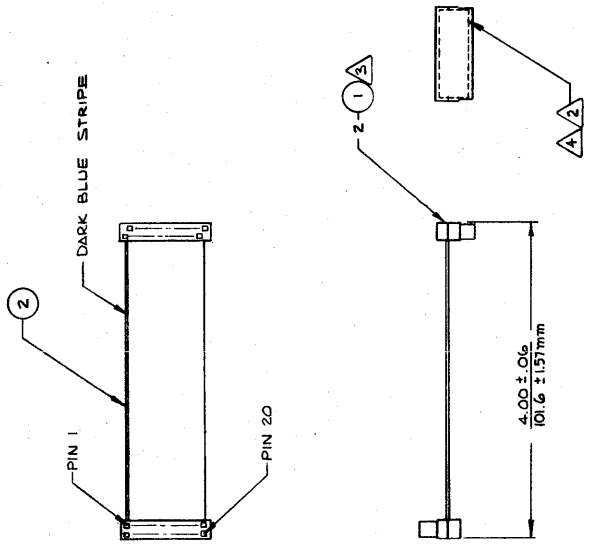
FINJ NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT HEAD	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NO	OR N
2	C	65832240	600	IN	CABLE	IN			PPP4		N
1	A	65853411	200	PC	CONNECTOR	IN	008502	110678			N
					NUMBER OF LINE ITEMS = 2						
					HIGHEST FINJ NUMBER = 2						

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-78

SHEET REVISION STATUS		REVISION RECORD			
REV	ECO	DESCRIPTION	DFT	DATE	CHK
00	05893	INITIAL RELEASE	JTP	6-24-75	M
A	08063	CLASS 'A' RELEASE	TP	12-7-78	G
B	08502	REVISED NDTE 4	TP	11-7-78	VK



NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. LOCATE APPROX AS SHOWN
3. ASSEMBLE ITEM 2 TO ITEM 1 USING 3M NO. 3440 PRESS RTN 1B844 WITH 3M NO. 3425-0000 RTN 27614 LOCATOR PLATE OR EQUIVALENT TOOLING.
4. MARK PER CDC SPEC 10121508 WITH PART NO. 74845800 AND REVISION.

INTER-DIVISIONAL DOCUMENT
 Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONAL DECIMAL MILLIMETER		COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	
DO NOT SCALE DRAWING	FIRST DESIGN	DATE	6-24-75
MATERIAL	CHK	ENGR	8-25-76
FINISH	MFG	APPD	6-25-75
DETACHED LISTS		CODE (PART NO)	DRAWING NUMBER
PL 74845800		C 34015	74845800
TITLE		SCALE	SHEET 1 OF 1
CABLE ASSY, FLAT		1 / 1	32915-009-070
20-CONDUCTOR			

ASSEMBLY PARTS LIST

SPARE CODE
S - SPARE PARTS
N - NON SPARE PARTS

7484580J	B	CLA	C	CHL ASSY FLAT 20-CONDUCTOR	UM	2551	02/08/78	11/06/78	1 / 1
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF

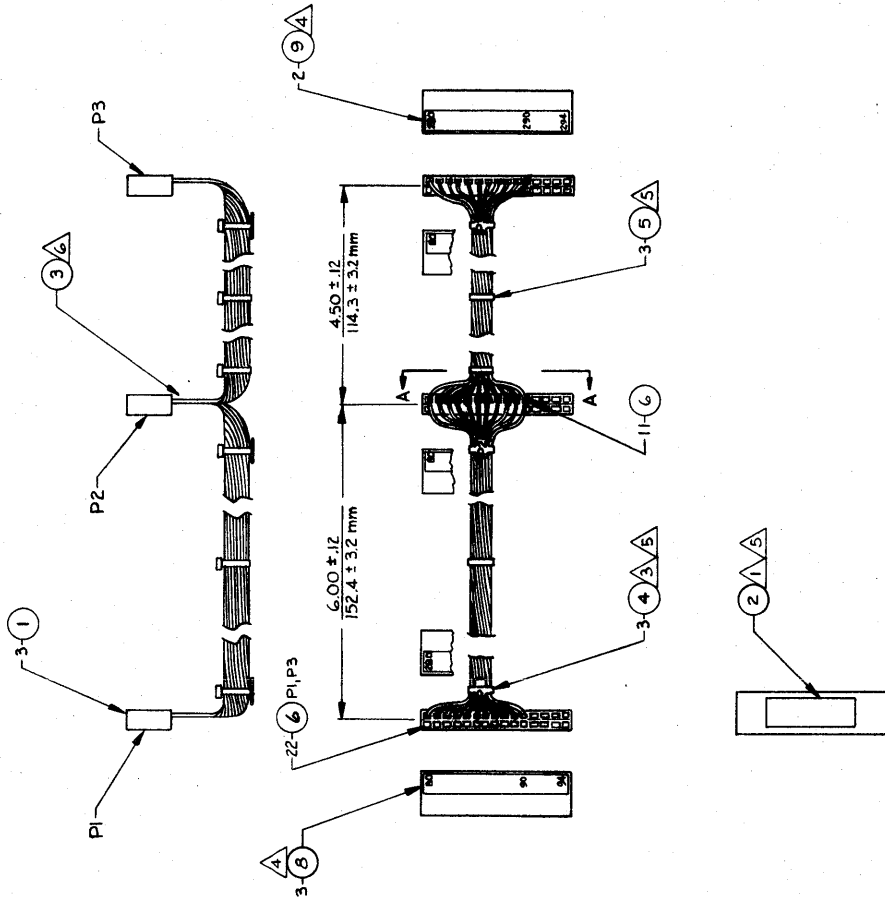
FINJ NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	DN KC	CH N
2	C	52532210	500	IN	CABLE	IN					
1	A	52533405	200	PC	CONNECTOR	IN	008502	110678	P-P4 CAWA		N
					NUMBER OF LINE ITEMS = 2						
					HIGHEST FINJ NUMBER = 2						

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

SHEET REVISION STATUS		REVISION RECORD			
REV	ECO	DESCRIPTION	DATE	CHK	APPD
D1	06001	INITIAL RELEASE	TP 11-21-75	LA	LA
C	06287	SEE ECO	LA 9-2-76	MI	MI
D	06331	SEE ECO	LA 9-2-76	MI	MI
E	08063	CLASS. A RELEASE	TP 1-17-78	MI	MI
F	08454	REV. PL & NOTE #6	CT 9-3-78	JK	JK



- NOTES:
- MARK PART NO. 74870828 AND SERIAL NUMBER PER CDC SPEC 10121508.
 - WORKMANSHIP PER CDC MFG SPEC 10120300.
 - INK STAMP PER CDC SPEC 10121502 LOCATE APPROX AS SHOWN.
 - TRIM TO FIT CONNECTOR AS SHOWN.
 - LOCATE APPROX AS SHOWN
 - WIRE P2 PINS 280 THRU 290 TO P1 AND P3 PINS 280 THRU 290 AS SHOWN USING FIND NO. 3. NOTE : 24 AWG CRIMPS (FIND NO.6) ARE USED IN CONNECTOR P2 TO HOLD TWO 26AWG WIRES IN EACH PIN POSITION GOING TO P1 AND P3.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CGC-STD 1.01.02A.
A48030 CA

VIEW-AA
SCALE 1:1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES		DRAWING NUMBER	
3 PLACE ±0.00mm	2 PLACE ±0.08mm	C 34015	74870828
DO NOT SCALE DRAWING		DRAWING NUMBER	
MATERIAL		C 34015 74870828	
FINISH		SCALE 1/1	
DETAILED LISTS		33750-009-070	
CONTROL DATA		SHEET 1 OF 1	
FIRST USED ON		T. PARNACIUN 11-3-75	
BY		2-9-76	
CHK		2-9-76	
ENGR		2-9-76	
MFG		2-9-76	
APPD		2-9-76	
DRAWN BY		2-9-76	
CHECKED BY		2-9-76	
APPROVED BY		2-9-76	
DATE		2-9-76	
TITLE		CABLE ASSY, DAISY CHAINED 667X EMULATION (REAR PANEL)	

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74R70R2R	F	CLA	A	PAISY CHAINFD 667X EMULATION	DM	2551	01/25/78	10/04/78	1 / 1
ASSEMBLY NUMBER	REV	CLASS	DN S2	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF
31750-009

FIND NUMBER	DN S2	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	3 OR 4
3	C	18543109	15400	IN	WIREF ELEC 26 AWG INSULATED	IN	00R454	10047R	PPP2		N
8	C	74R42R00	300	PC	LARFL CONTACT CAVITY 52 102	IN			PPP4		N
9	C	74R43000	200	PC	LARFL CONTACT CAVITY 252 302	IN			PPP4		N
6	C	94245601	3300	PC	CONTACT-CRIMP INSERT SOCKET	IN	00R454	10047R	PPP4		N
4	C	94277407	300	PC	STRAP CABLE TIE	IN			PPP1		N
5	C	94277416	300	PC	STRAP CABLE TIE	IN			PPP1		N
1	C	94360807	300	PC	HOUSING-CONV. SOCKET .125 30CAV	IN			PPP4		N

NUMBER OF LINE ITEMS = 7
HIGHEST FIND NUMBER = 9

PROJECT ENGINEER

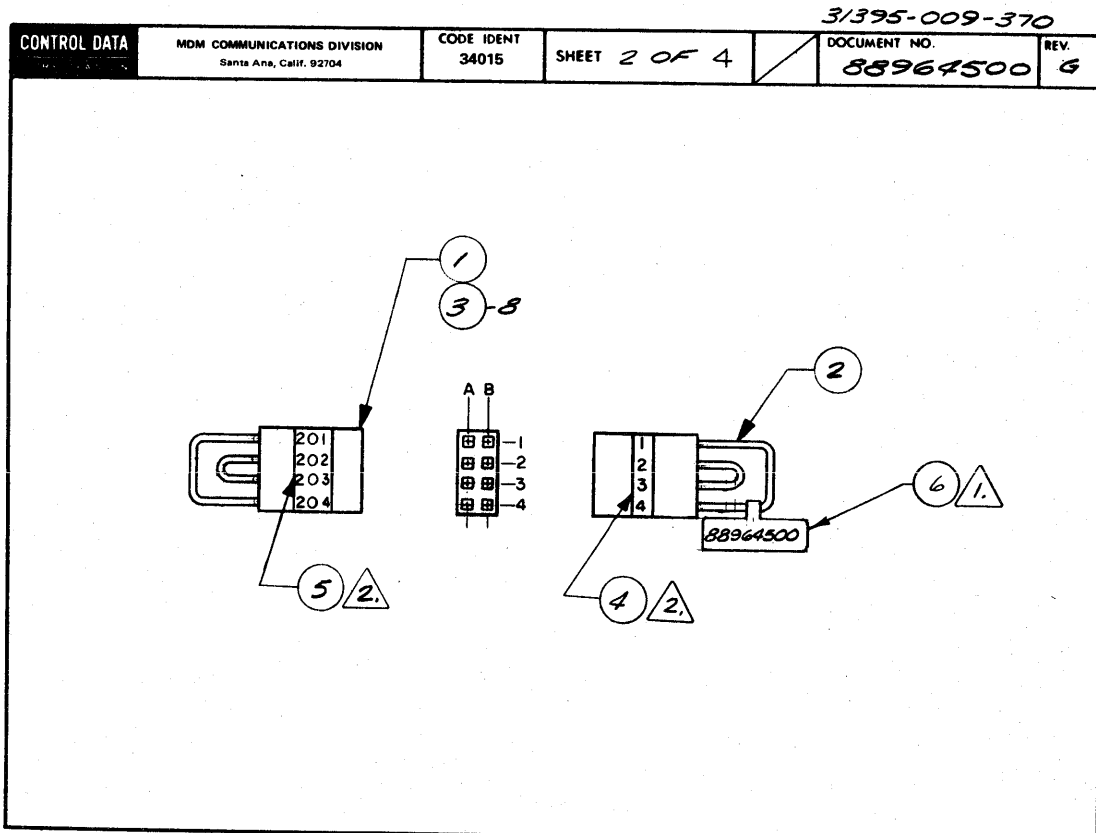
ARDEN HILL

AA 2700 REV. 7-78

DWN	Hostell	CONTROL DATA	TITLE	JUMPER, INTERNAL 5V- CYBER COUPLER	PREFIX	DOCUMENT NO.	REV			
CMD		COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	FIRST USED ON	DK106		88964500	H			
ENG		CODE IDENT		34015						
MFG										
APPR										
SHEET REVISION STATUS				REVISION RECORD						
				2 /	REV	ECO	DESCRIPTION	DRFT	DATE	APP
				DPM	04	05549	SEE ECO	DPM	5-19-75	[Signature]
				DPM	05	05743	SEE ECO	DPM	5-20-75	[Signature]
				G	G	06410	SEE ECO	H	6-24-76	[Signature]
				H	H	08063	CLASS "A" RELEASE	TP	1-27-78	[Signature]
<p>INTER-DIVISIONAL DOCUMENT</p> <p>Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.</p> <p>AA6030 CA</p>										
				NOTES:						
								PL 88964500		
								DETACHED LISTS		

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.



FORM 19246-00-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

88964500	M	CLA	A	JUMPER INTERNAL 5V CYBER COIHL	DM	2551	01/25/78	01/25/78	1 / 1
ASSEMBLY NUMBER	REV	CLASS	DW SE	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF
31395-009

FIND NUMBER	DW SE	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH NC	A OR N
2	C	24548303	100	IN	WIRE, ELECT, 24 GA, PVC, UL, RED	IN			PPP5		N
3	A	74718400	100	PC	CONTACT	IN			PPP4		N
1	A	74718500	100	PC	CONN HOUSING 8 CAVITY	IN			PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN			PPP4		N
5	C	74842900	100	PC	LABEL CONTACT CAVITY 201 251	IN			PPP4		N
6	C	94277407	100	PC	STRAP CABLE TIE	IN			PPP1		N

NUMBER OF LINE ITEMS = 6
HIGHEST FIND NUMBER = 6

PROJECT ENGINEER: ARDEN HILLS

DWN	E. Ganser	8-2-77	CONTROL DATA	TITLE	TOP ASSEMBLY - CABLE SET EMULATION COUPLER	PREFIX	DOCUMENT NO.	REV
CHKD	A	9-1-77	COMMUNICATIONS PRODUCTS DIV. SANTA ANA, CA 92704	FIRST USED ON	XA 226-A		74873995	B
ENG	MIB	8-77	CODE IDENT		35685-009-070			SHEET 1 OF 1
MFG			34015					
APP								

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	APP		
01	06965	INITIAL REL- CL 'B'	ELG	9-1-77	M		
A	08063	CLASS A RELEASE	TP	1-20-78	P		
B	08511	CORRECT PN FIND NO. 1	TD	13 FEB 79	J/K		

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

AA6030

NOTES: FOR INSTALLATION INSTRUCTIONS SEE 74873993 (35685-080-151)

PL 74873995
DETACHED LISTS

FORM 19246-01-015-092 DIETRICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

CD CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74873995	B	CLA	A	CBL SET EMULATION COUPLER	DM	2551	01/25/78	02/20/79	1/1	MF
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER	

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORG. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	SPARE	S OF N
2	A	19191600	200	PC	I/O COAXIAL CABLE ASSY	IN				N	N
1	A	52675000	200	PC	COAXIAL CABLE WITH CUNN 5 FT	OUT	008511	021579		N	N
1	A	52675100	200	PC	COAXIAL CABLE WITH CONNECTOR	IN	008511	021579		N	N
3	A	88947800	400	PC	CABLE, COAX - 5 FT.	IN			AYM4	N	N

NUMBER OF LINE ITEMS = 4
HIGHEST FIND NUMBER = 3

PROJECT ENGINEER SANTA ANA

AA 2700 REV. 7-78

Printed in U.S.A.

GENERAL SUPPLEMENT SHEET

COMPUTER DIVISION	COAXIAL CABLE WITH CONNECTOR	DOCUMENT NO. A 52675100	REV. R
		SHEET / OF	

TO MAKE	DIMENSION A	
52675000	5 FT ± 2"	Machine crimp taper pin P/N 24500707 using the standard AMP taper pin machine, adjusted to a wire crimp height of 0.039 ± 0.002 on center conductor and 0.080 ± 0.005 insulation crimp height for insulator on center conductor. Wire crimp height for the shield should be adjusted to 0.045 ± 0.002, with the shield visible in both inspection windows. NOTE: Strip length for conductor should be 11/64 ± 1/64.
52675001	70 FT ± 2"	
52675002	45 FT ± 2"	
52675003	38 FT ± 2"	
52675004	50 FT ± 2"	
52675005	7 FT ± 2"	

NOTES: 1. FOR REPAIR ONLY, USE TAPER PIN P/N 24500717 AND CRIMP WITH HAND CRIMPER, AMP NUMBER 90115.
2. TYRAP GUN SHALL BE TIGHTENED WITH A "THOMAS & BETTS" TYRAP GUN WITH A NUMBER 4 TENSION SETTING.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

ASSY 52675100		CODE IDENT	SHEET 2	DOCUMENT NO. WL 52675100	REV. E				
CONDUCTOR IDENT	FIND NO	GAUGE (REF.)	COLOK (REF.)	LENGTH (APPROX)	ORIGIN	ACCESS FIND NO	DESTINATION	ACCESS FIND NO	REMARKS
		30	90	5FT	PI A				
		91			B				
		92			C				
		93			D				
		94			E				
		95			F				
		96			H				
		97			J				
		98			K				
		99			L				
		900			M				
		910			N				
		920			P				
		930			R				
		940			S				
		950			T				
		960			U				
		970			V				
		30	980	5FT	PI W				

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

ASSEMBLY PARTS LIST

NON-SPARE PARTS

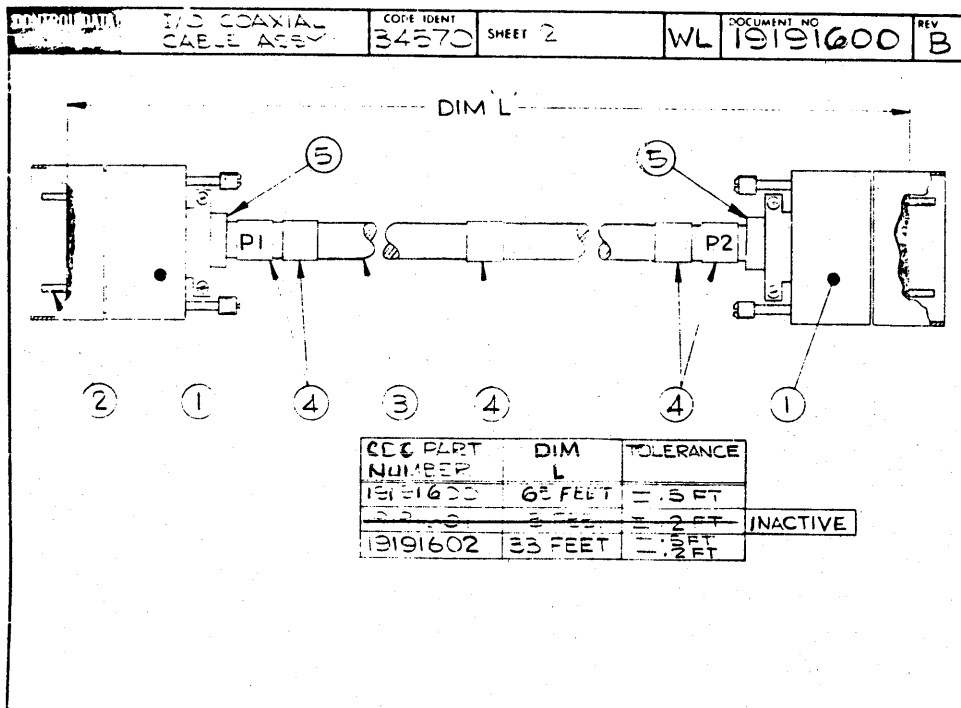
52675100	S	CLA	A	COAXIAL CABLE WITH CONN 5-FT	ICAM	6A3X	34/11/69	34/12/77	1 / 1
ASSEMBLY NUMBER	REV.	CLASS	CD	ASSEMBLY DESCRIPTION	DESIGN SOURCE	DATE	ISSUE DATE	PROCESSING DATE	PAGE NUMBER

LINE NO.	QTY	PART NUMBER	QUANTITY	UNIT	PART DESCRIPTION	DATE	STATUS	REVISION	DATE	REVISION
13	A	09031211	100	PC	RIVET POP OPEN-END .127 DIA	IN	037799	022677		
14	A	10125606	100	PC	PLAIN WASHERS	IN	037799	022677		0001
	C	17620300	300	PC	STRAP CABLE ADJUSTABLE	CUT	037799	022677		0003
	C	17620301	200	PC	STRAP CABLE ADJUSTABLE	CUT	037799	022677		0003
11	C	17620303	100	PC	STRAP CABLE ADJUSTABLE	IN	037799	022677		0003
10	C	17620307	100	PC	STRAP CABLE ADJUSTABLE	IN	037799	022677		0003
12	C	17780211	100	PC	CABLE LOOP END	IN	037799	022677		0004
4	C	17944062	100	PC	LABEL, CABLE LENGTH MARKING	IN	027458	020771		0001
2	C	18752802	100	PC	CONN BODY, HOOD ASY, 20 PCS	IN	026130	020771		0004
5	C	18752811	1900	PC	SINGLE PIECE CONTACT - COAX	IN	029901	020771		0001
7	C	18974300	100	PC	MARKER, IDENT-CABLE STRAP	IN	027458	020771		0001
4	C	24500707	3800	PC	PIN TAPER	IN	029901	020771		0001
3	C	24500902	1900	PC	INSULATION SLEEVING ELECT	IN	037767	020771		0003
1	C	24567000	500	FT	CABLE, COAXIAL, 19-CONDUCTOR	IN	029982	020771		0001

NUMBER OF LINE ITEMS = 14
HIGHEST LINE NUMBER = 14

BILL STORM ARDEN HILLS DATE: 11/11/69

DWG	34570	DESCRIPTION	I/O COAXIAL CABLE ASSY		REV	WL	DOCUMENT NO	19191600	REV	B	
ENGR	W. J. M.	DATE	CANADIAN DEVELOPMENT		APP	W. J. M.	DATE				
APP	W. J. M.	DATE	34570		FIRST USED ON	AA107A		SHEET 1 OF 3			
SHEET REVISION STATUS					REVISION RECORD						
1	2	3			REV	APP	DESCRIPTION	DATE	DATE	APP	
							CLASS B DWG	12-27-67		WJ	
2	2	2					REVISIONS TO BE MADE TO BE ADDED				
3	2	2					REVISIONS TO BE MADE TO BE ADDED				
4	2	2					REVISIONS TO BE MADE TO BE ADDED				
A	A	A					CLASS A DWG	EMG 29 OCT 74			
E	B	A					TAE OF INACTIVATED	RW 12-27-67			
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> <p>INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01-024.</p> </div>											
<p>NOTES 1. NO ASSY DWG AVAILABLE. 2. FOR ALL SOLDERING USE 60/40 RESIN CORE SOLDER.</p>											
INACTIVE								PL 19 91600			
DETACHED LISTS											



CONTROL DATA				I/O COAXIAL CABLE ASSY		CODE IDENT	SHEET 3		WL	DOCUMENT NO.	REV.
						34570				19191600	A
CONDUCTOR IDENT	FIND NO	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		DESTINATION		ACCESS FIND NO	REMARKS	
	3		90		P1	A	P2	A	2		
	↑		91		↑	B	↑	B	↑		
			92			C		C			
			93			D		D			
			94			E		E			
			95			F		F			
			96			H		H			
			97			J		J			
			98			K		K			
			99			L		L			
			900			M		M			
			910			N		N			
			920			P		P			
			930			R		R			
			940			S		S			
			950			T		T			
			960			U		U			
	↓		970		↓	V	↓	V	↓		
	3		980		P1	W	P2	W	2		

TABULATION			REVISION RECORD						
PART NO.	LENGTH	RTU NO	REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
88947800	5' ± 3"	3/394	E		FOR REVISIONS SEE JHT 8				
01	70' ± 6"	3/398							

- ④ FIND N° 21 TO BE MARKED PER CDC STD 1.030.008
- ③ TRIM FIND NUMBER 4 LABEL TO DESIRED LENGTH AND AFFIX TO CONNECTOR HOUSING MAINTAINING CONTACT ORIENTATION.
- ② LENGTH OF WIRE INSULATION TO BE 1.75" BETWEEN FERRULE AND CONTACT.
- ① FIND N° 10 TO BE MARKED PER CDC SPEC 10121508 WITH APPLICABLE PART NUMBER, REVISION, DATE CODE AND PI OR JI AS APPLICABLE.

INTER-DIVISIONAL DOCUMENT
 Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

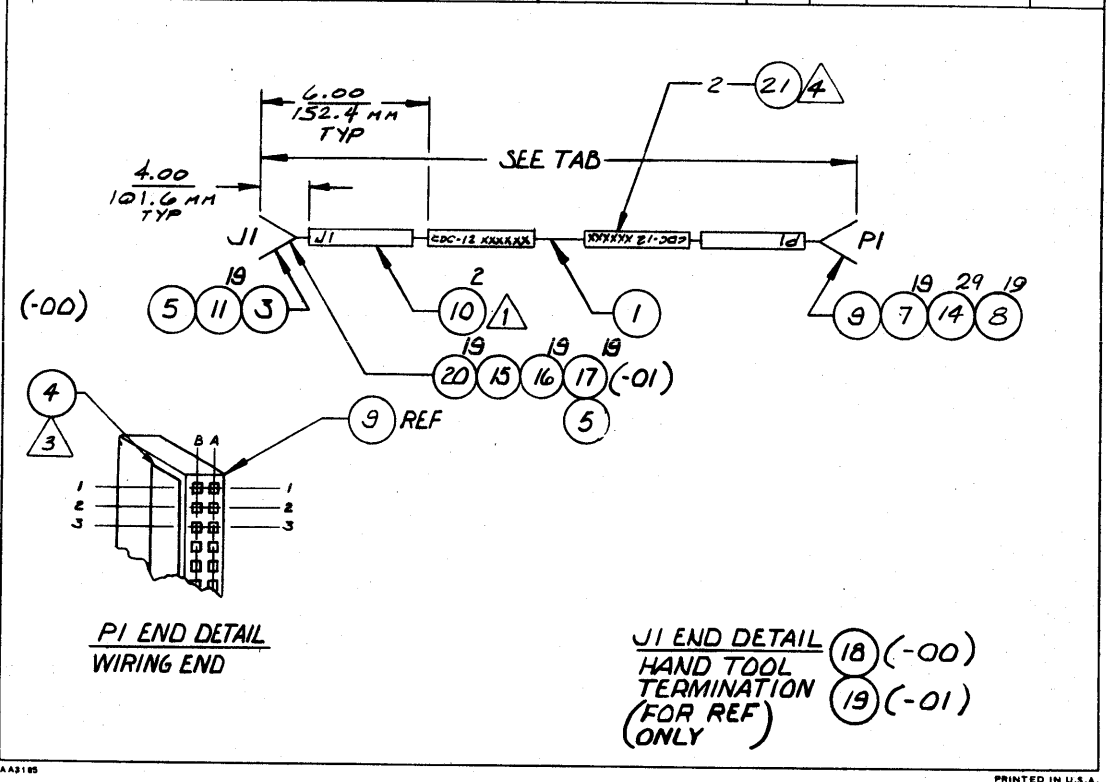
NOTES UNLESS OTHERWISE SPECIFIED

DWN	<i>B. Johnson Jr</i>	4/17/74	CONTROL DATA	TITLE			
CHKD	<i>B. Johnson Jr</i>	6-27-74		COAX CABLE, 19-COND			
ENG	<i>B. Johnson Jr</i>	6-28-74					
MFG	<i>E. Kern</i>		SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037		CODE IDENT	DWG No	
APP	<i>E. Kern</i>	7.8.74			09132	A	88947800/01
AA4291			SCALE				SHEET 1 OF 8

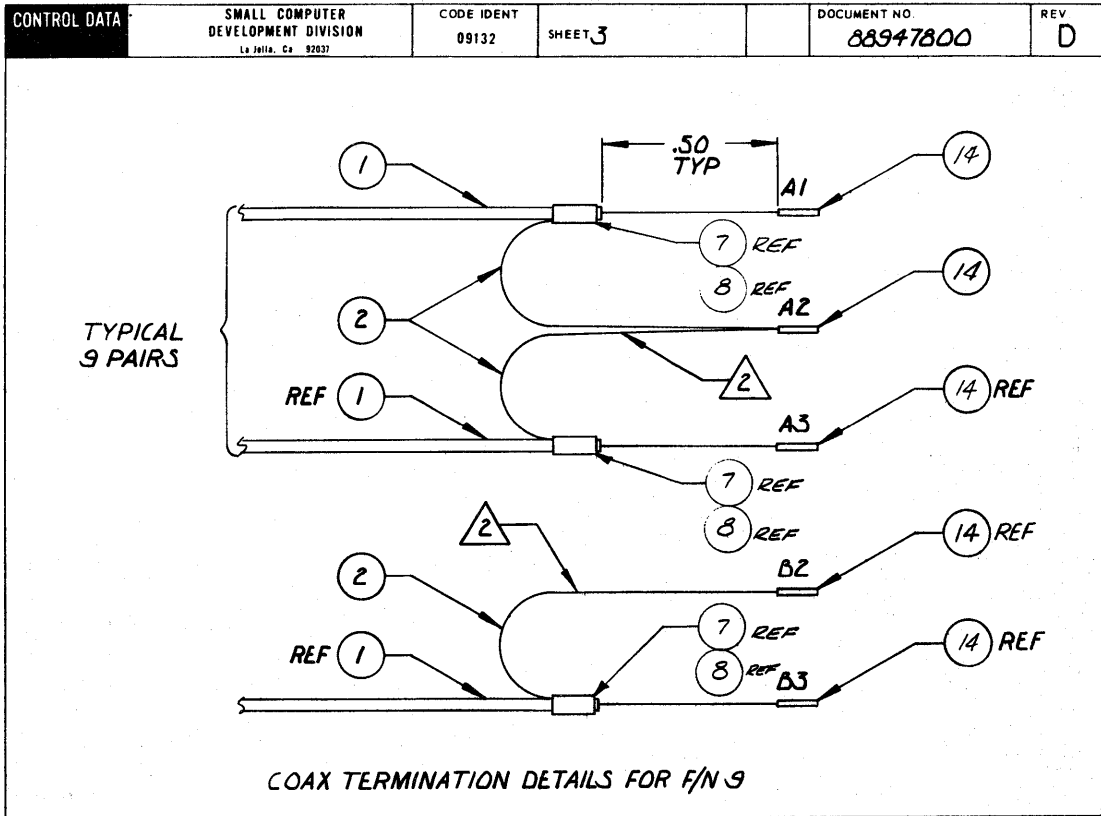
STAOPS Division controls this document as of **JULY 2, 1974**

31394-009-370
31398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Ca 92037	CODE IDENT 09132	SHEET 2	DOCUMENT NO. 88947800	REV. E
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31394-009-370
31398



AA3185

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31394-009-370
31398

CONTROL DATA				SMALL COMPUTER DEVELOPMENT DIVISION <small>La Jolla, Ca 92037</small>			CODE IDENT 09132		SHEET 4		WL		DOCUMENT NO. 88947800		REV D
CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS				
1	1	30	90	5FT	J1	A	11	PI	A1	14,78	COND } TYP 10 PLCS SHIELD }				
2									A2	14,2					
3			91			B			B3	14,78					
4									B2	14,2					
5			92			C			A3	14,78					
6									A2	14,2					
7			93			D			B4	14,78					
8									B5	14,2					
9			94			E			A4	14,78					
10									A5	14,2					
11			95			F			B6	14,78					
12									B5	14,2					
13			96			H			A6	14,78					
14									A5	14,2					
15			97			J			B7	14,78					
16									B8	14,2					
17			98			K			A7	14,78					
18									A8	14,2					
19	1	30	9	5FT	J1	L	11	PI	B9	14,78					
20									B8	14,2					

AA3183 REV. 8/71

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3/399-009-370
3/398

CONTROL DATA		SMALL COMPUTER DEVELOPMENT DIVISION <small>La Jolla, Ca 92037</small>			CODE IDENT 09132	SHEET 5		WL	DOCUMENT NO 88947800	REV D	
CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
21	1	30	900	5FT	J1	M	11	PI	A9	14,7,8	COND SHIELD } TYP 9 PLCS
22	↑	↑	↑	↑	↑	↑	↑	↑	A8	14,2	
23	↑	↑	910	↑	↑	N	↑	↑	B10	14,7,8	
24	↑	↑	↑	↑	↑	↑	↑	↑	B11	14,2	
25	↑	↑	920	↑	↑	P	↑	↑	A10	14,7,8	
26	↑	↑	↑	↑	↑	↑	↑	↑	A11	14,2	
27	↑	↑	930	↑	↑	R	↑	↑	B12	14,7,8	
28	↑	↑	↑	↑	↑	↑	↑	↑	B11	14,2	
29	↑	↑	940	↑	↑	S	↑	↑	A12	14,7,8	
30	↑	↑	↑	↑	↑	↑	↑	↑	A11	14,2	
31	↑	↑	950	↑	↑	T	↑	↑	B13	14,7,8	
32	↑	↑	↑	↑	↑	↑	↑	↑	B14	14,2	
33	↑	↑	960	↑	↑	U	↑	↑	A15	14,7,8	
34	↑	↑	↑	↑	↑	↑	↑	↑	A14	14,2	
35	↑	↑	970	↑	↑	V	↑	↑	B15	14,7,8	
36	↓	↓	↓	↓	↓	↓	↓	↓	B14	14,2	
37	1	30	980	5FT	J1	W	11	PI	A13	14,7,8	
38	↑	↑	↑	↑	↑	↑	↑	↑	A14	14,2	
39	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	
40	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	

AA3183 REV. 8-71

PRINTED IN U.S.A.

3/399-009-370
3/398

CONTROL DATA		SMALL COMPUTER DEVELOPMENT DIVISION <small>La Jolla, Ca 92037</small>			CODE IDENT 09132	SHEET 6		WL	DOCUMENT NO 88947800	REV D	
CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
41	1	30	90	70FT	J1	A	16,17,20	PI	A1	14,7,8	COND SHIELD } TYP 10 PLCS
42	↑	↑	↑	↑	↑	↑	↑	↑	A2	14,2	
43	↑	↑	91	↑	↑	B	↑	↑	B3	14,7,8	
44	↑	↑	↑	↑	↑	↑	↑	↑	B2	14,2	
45	↑	↑	92	↑	↑	C	↑	↑	A3	14,7,8	
46	↑	↑	↑	↑	↑	↑	↑	↑	A2	14,2	
47	↑	↑	93	↑	↑	D	↑	↑	B4	14,7,8	
48	↑	↑	↑	↑	↑	↑	↑	↑	B5	14,2	
49	↑	↑	94	↑	↑	E	↑	↑	A4	14,7,8	
50	↑	↑	↑	↑	↑	↑	↑	↑	A5	14,2	
51	↑	↑	95	↑	↑	F	↑	↑	B6	14,7,8	
52	↑	↑	↑	↑	↑	↑	↑	↑	B5	14,2	
53	↑	↑	96	↑	↑	H	↑	↑	A6	14,7,8	
54	↑	↑	↑	↑	↑	↑	↑	↑	A5	14,2	
55	↑	↑	97	↑	↑	J	↑	↑	B7	14,7,8	
56	↑	↑	↑	↑	↑	↑	↑	↑	B8	14,2	
57	↑	↑	98	↑	↑	K	↑	↑	A7	14,7,8	
58	↓	↓	↓	↓	↓	↓	↓	↓	A8	14,2	
59	1	30	9	70FT	J1	L	16,17,20	PI	B9	14,7,8	
60	↑	↑	↑	↑	↑	↑	↑	↑	B8	14,2	

AA3183 REV. 8-71

PRINTED IN U.S.A.

31394-009-370
31398

CONTROL DATA		SMALL COMPUTER DEVELOPMENT DIVISION <small>LA JOLLA CA 92037</small>		CODE IDENT 09132	SHEET 7	WL	DOCUMENT NO 88947800	REV D			
CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION	ACCESS FIND NO	REMARKS	
61	1	30	900	70FT	J1	M	16,17,20	PI	A9	14,78	COND } TYP 9 PLCS
62	↑	↑	↑	↑	↑	↑	↑	↑	A8	14,2	SHIELD }
63			910			N			B10	14,78	
64									B11	14,2	
65			920			P			A10	14,78	
66									A11	14,2	
67			930			R			B12	14,78	
68									B11	14,2	
69			940			S			A12	14,78	
70									A11	14,2	
71			950			T			B13	14,78	
72									B14	14,2	
73			960			U			A15	14,78	
74									A14	14,2	
75			970			V			B15	14,78	
76	↑	↑	↑	↑	↑	↑	↑	↑	B14	14,2	
77	1	30	980	70FT	J1	W	16,17,20	PI	A13	14,78	
78									A14	14,2	
79											
80											

AA3183 REV. 8-71

PRINTED IN U.S.A.

31394-009-370
31398

CONTROL DATA		TITLE	PREFIX	DOCUMENT NO.	REV								
LA JOLLA DIVISION LA JOLLA CALIF 92037 CODE IDENT 09132		COAX CABLE, 19COND		88947800/01	F								
FIRST USED ON			SHEET 8 OF 8										
SHEET REVISION STATUS								REVISION RECORD					
								REV	ECO	DESCRIPTION	DRFT	DATE	APP
								A		RELEASED CL.A.	5/2	7-8-74	JK
								B	13344	TRNSFRD. TO STROPS	LVP	7-8-74	JK
								00	-	INITIAL RELEASE - STADPS			
								01	-	DELETE PD NO. 5, MADE P/L DETACHED LIST	LA	12-4-74	
								02	02	CL. B PRERELEASE	LA	12-5-74	
								03	03	SEE E.C.O.	DPM	2-17-75	
								04	03	SEE E.C.O.	DPM	4-18-75	
								05	03	SEE E.C.O.	LA	8-14-75	JK
								06	03	SEE E.C.O.	LA	11-14-75	JK
								07	03	CL.I COMM. LABEL CHG	DPM	1-11-77	JK
								C	C	REVISED PL. SEE ECO	TP	4-7-78	JK
								D	D	REV. PL PART N°	RN	9-28-78	JK
								E	D	REV. PL F/N 5 & 21	AV	11-78	JK
								F	D	REV. PL F/N 11	CT	4-16-79	JK

NOTES:

PL 88947801
PL 88947800
DETACHED LISTS

AA3180 REV. 8-71

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ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

88947800		F	CLA	A	CABLE, COAX - 5 FT.	DM	CYBR70	06/21/74	04/17/79	1/ 1	
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION		DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER	
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	DN NC	OR N
21	A	10123800	200	PC	LABEL, CABLE MARKING	IN	008476	110278	PPP4		N
2	C	18563100	4800	IN	WIPE ELEC 26 AWG INSULATED	IN	008456	092978	PPP4		N
18	C	18752700	REF	PC	CONN COAX KEVED JACKS MULT POS	IN	013303	070874	RFE4		N
3	C	18752702	100	PC	CONN BODY, HOOD ASSY 20 POS	IN			PPP4		N
11	C	18752711	1000	PC	SINGLE PIECE CONTACT - COAX	IN	008414	041679	PPP4		N
5	C	24534714	1000	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008476	110278	PPP4		N
1	C	24567000	500	FT	CABLE, COAXIAL 19 COND., 730HM	IN			PPP4		N
10		51904701	200	PC	CABLE LABEL	IN	008218	041178	PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN	008500	110777	PYP4		N
14	C	94245601	2900	PC	CONTACT-CRIMP INSERT SOCKET	IN	008456	092978	PPP4		N
8	A	94278613	1900	PC	FERRULE INSULATOR	IN	008500	110777	PPP4		N
9	C	94360807	100	PC	HOUSING-CONN, SOCKET .125 30CAV	IN			PPP4		N
7	C	94871108	1900	PC	FERRULES GRN UNINSULATED	IN	008218	040778	PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 21

AA 2709 REV. 7-76

GEORGE BURN SANTA ANA

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ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

88947801		F	CLA	A	CABLE, COAX - 70 FT.	DM	CYBR70	06/21/74	04/18/79	1/ 1	
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION		DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER	
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	DN NC	OR N
21	A	10123800	200	PC	LABEL, CABLE MARKING	IN	008476	110278	PPP4		N
2	C	18563100	4800	IN	WIPE ELEC 26 AWG INSULATED	IN	008456	092978	PPP4		N
19	C	18752800	REF	PC	CONN COAX JACK SCREW MULT POS	IN					N
15	C	18752802	100	PC	CONN BODY, HOOD ASSY, 20 POS	IN			PPP4		N
16	C	18752803	1900	PC	FEMALE CONTACT	IN					N
17	C	18752804	1900	PC	OUTER BODY, FEMALE CONTACT	IN					N
20	C	18752805	1900	PC	FERRULE	IN					N
5	C	24534714	1000	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008476	110278	PPP4		N
1	C	24567000	7000	FT	CABLE, COAXIAL 19 COND., 730HM	IN			PPP4		N
10		51904701	200	PC	CABLE LABEL	IN	008218	040778	PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN	008500	110777	PYP4		N
14	C	94245601	2900	PC	CONTACT-CRIMP INSERT SOCKET	IN	008456	092978	PPP4		N
8	A	94278613	1900	PC	FERRULE INSULATOR	IN	008500	110777	PPP4		N
9	C	94360807	100	PC	HOUSING-CONN, SOCKET .125 30CAV	IN			PPP4		N
7	C	94871108	1900	PC	FERRULES GRN UNINSULATED	IN	008218	040778	PPP4		N

NUMBER OF LINE ITEMS = 15
HIGHEST FIND NUMBER = 21

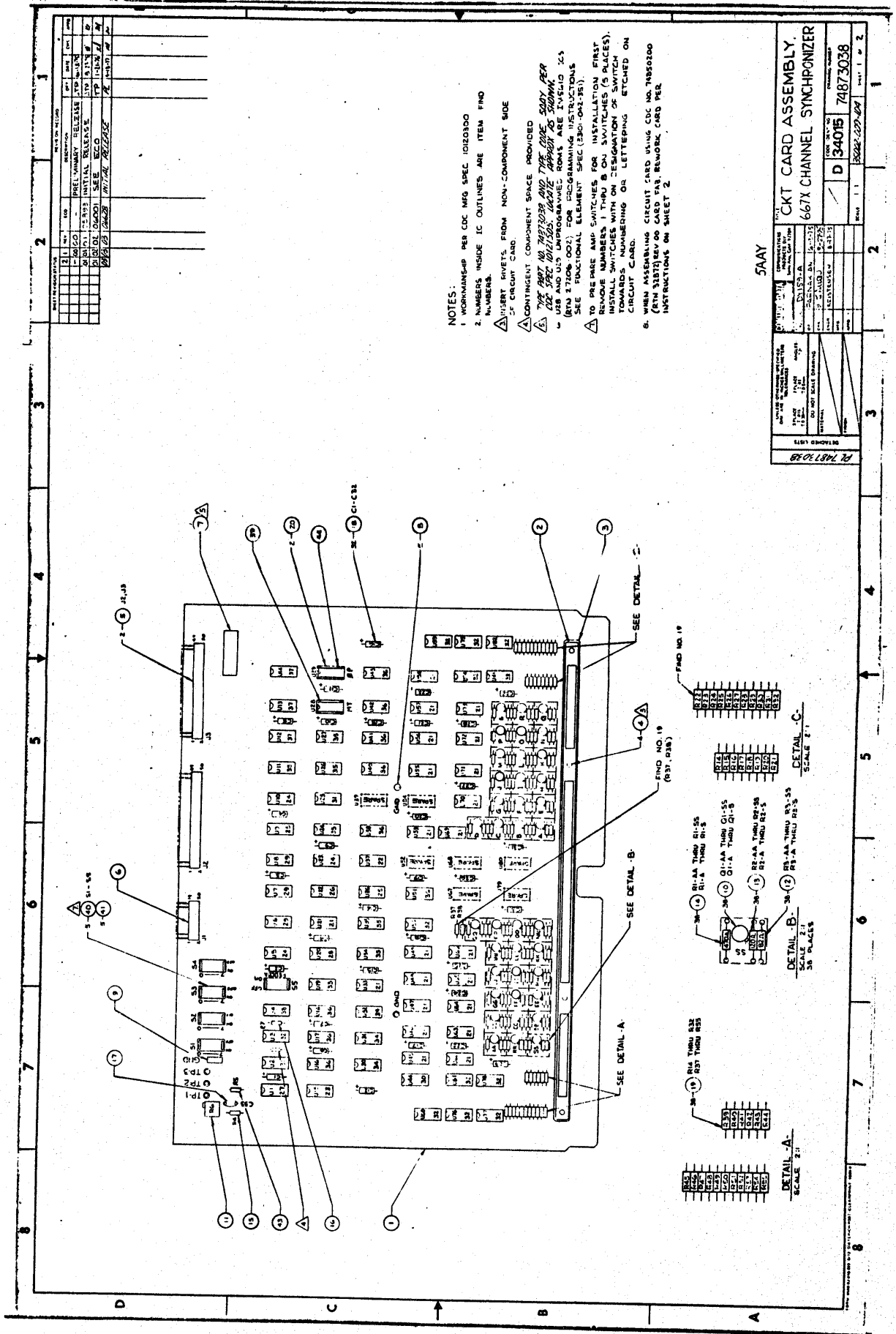
AA 2709 REV. 7-76

GEORGE BURN SANTA ANA

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PAGES 7-29 THROUGH 7-54 ARE DELETED.





- NOTES:**
- WORKING-UP PER CDC MFG SPEC 10120300
 - NUMBERS INSIDE IC OUTLINES ARE ITEM FIND NUMBERS.
 - INSERT RIVETS FROM NON-COMPONENT SIDE
 - CONTINGENT COMPONENT SPACE PROVIDED
 - THE PART NO. 74879600 AND THE CODE 5000 PER CDC SPEC 10121500. LARGE APPROX. 20 SQUARE INCH AND US UNPROGRAMMABLE ROMS ARE I.V.S.W.I.G. 2.5 SEE FUNCTIONAL ELEMENT SPEC (380-041-95).
 - TO PREPARE AMP SWITCHES FOR INSTALLATION FIRST REMOVE THE AMP SWITCHES FROM THE SWITCHES (5 PLACES). INSTALL SWITCHES WITH THE NUMBERING OR LETTERING ON TOWARDS NUMBERING OR LETTERING ETCHED ON CIRCUIT CARD.
 - WHEN ASSEMBLING CIRCUIT CARD USING CDC NO. 74850300 (RTH 3187) REV 00 CARD FAB. NETWORK CARD PER INSTRUCTIONS ON SHEET 2.

REV	DATE	BY	CHKD	DESCRIPTION
1	10/1/68	INITIAL RELEASE
2	10/1/68	SEE ECO
3	10/1/68
4	10/1/68
5	10/1/68
6	10/1/68
7	10/1/68
8	10/1/68

5AAY

74879600

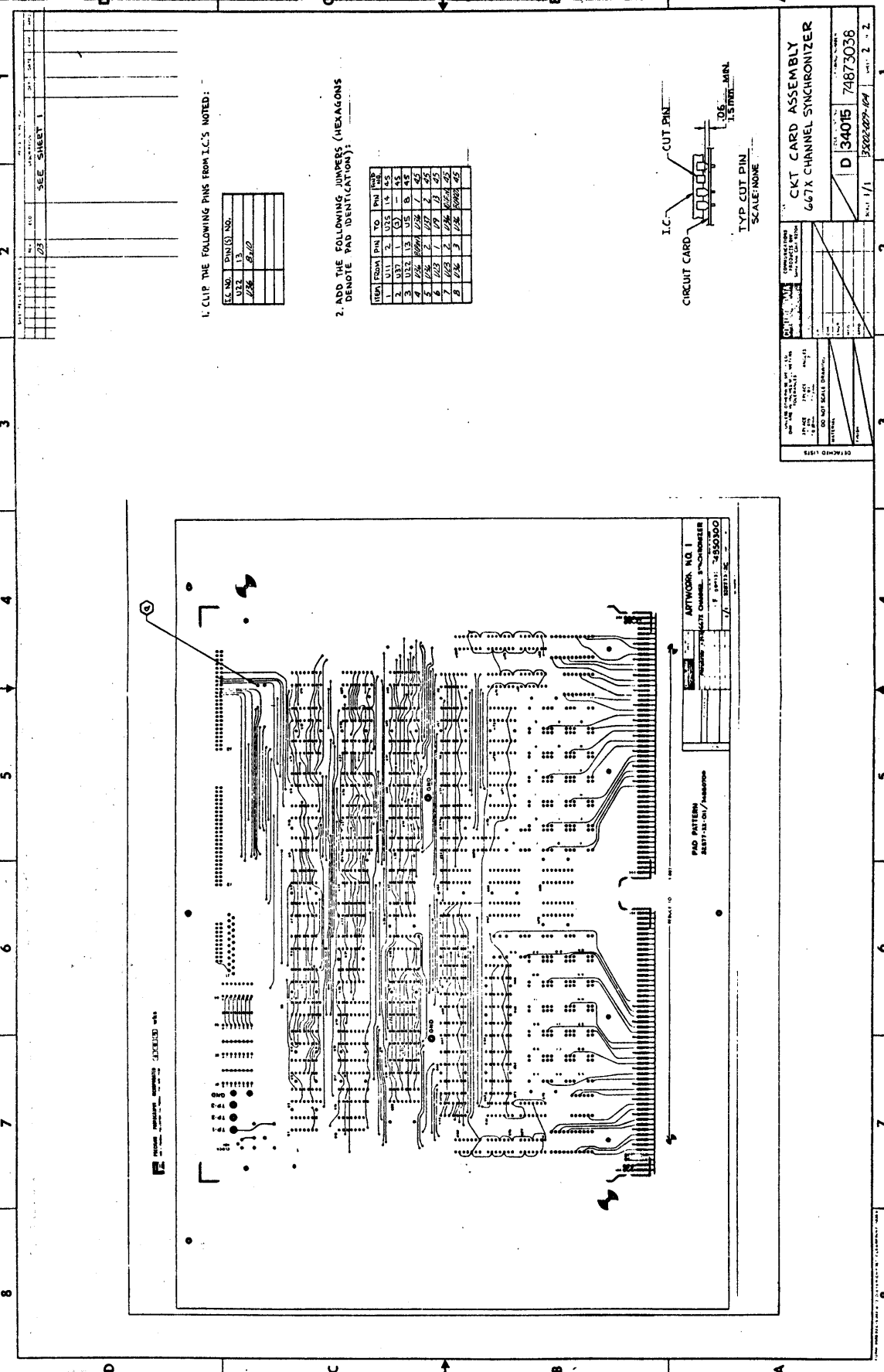
667X CHANNEL SYNCHRONIZER

REV 1.1

30282-229-604

74873038

SCALE 2:1



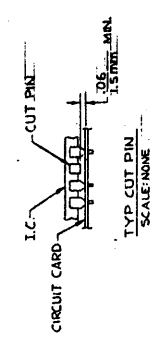
REV	DATE	BY	CHK	APP	DESCRIPTION
1					SEE SHEET 1

1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

I.C. NO.	PIN(S) NO.
U11	13
U12	8, 10

2. ADD THE FOLLOWING JUMPERS (HEXAGONS DENOTE PAD IDENTIFICATION):

ITEM	FROM PIN	TO PIN	NO.		
1	U11	2	U25	16	45
2	U17	1	U2	1	45
3	U12	13	U2	1	45
4	U12	13	U2	7	45
5	U12	2	U7	2	45
6	U13	1	U9	1	45
7	U13	5	U18	1	45
8	U12	3	U28	1	45



CKT CARD ASSEMBLY 667X CHANNEL SYNCHRONIZER	
D 34015 74873036	PART 1/1 35022-029-004 REV. 2 - 72

ARTWORK NO. 1
 PART 1 OF 1
 DATE: 11/11/72
 BY: BMT/12

PAD PATTERN
 ASSY-12-01/14-0000

DESIGN	PARAKIAN	6-11-75	COMMUNICATIONS	PREFIX	DOCUMENT NO.	REV
CHG	(J.S. Aug)	8-27-75	PRODUCTS DIV.	PL	74873038	03
ENG	KRISTENSEN	8-27-75	Series A12, C1, 92704			
MFG			CODE IDENT			
APP			34015			
		FIRST USED ON		SHEET 1 OF 4		
		DY159-A		35002-009-104		

SHEET REVISION STATUS											REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	APP	4	3	2	1	REV				
00	—	PRELIMINARY RELEASE	JTP	6-11-75		00	00	00	00	00				
01	05893	INITIAL RELEASE	JTP	8-27-75	✓	01	01	01	01	01				
02	06001	SEE ECO	TP	1-21-76	M	01	01	01	02	02				
03	06628	INITIAL RELEASE	PL	4-18-77	✓	03	03	03	03	03				

NOTES:

DETACHED LISTS

35002-009-104

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704		CODE IDENT 34015	SHEET 2 OF 4	PL	DOCUMENT NO 74873038	REV 03				
LINE NO.	PART IDENTIFICATION	QUANTITY REQUIRED						UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	74850200	1						PC	CKT. CARD FAB.	32872-010
2	88895400	1						PC	STIFFENER	27299-002
3	88895500	1						PC	INSULATOR	27300-002
4	88812400	4						PC	RIVETS 1/8" x 5/16"	27301-002
5		2						PC	HEADER, RT ANGLE -50	27926-002
6		1						PC	HEADER, RT ANGLE -20	28634-002
7	73954300	1						PC	NAMEPLATE	15486-010
8		5						PC	TERMINAL	01628-002
9		1						PC	TEST JACK	27765-002
10		38						PC	TRANSISTOR	23831-002
11		1						PC	RESISTOR, 2K, POT	27814-002
12	24500037	38						PC	RESISTOR, 82Ω, 1/4W	05208-002
13	24500041	38						PC	RESISTOR, 120Ω, 1/4W	03704-002
14	24500055	38						PC	RESISTOR, 470Ω, 1/4W	03708-002
15	24500050	1						PC	RESISTOR, 300Ω, 1/4W	05771-002
16	24500039	1						PC	RESISTOR, 100Ω, 1/4W	00924-002
17		1						PC	CAPACITOR, 56 Pf	27768-002
18		32						PC	CAPACITOR, 1MF, 35V	20771-002
19	24500023	38						PC	RESISTOR, 22Ω, 1/4W	05761-002
20		2						PC	SOCKET, IC, 16 PIN	24158-002

FORM 19247 01 015 092 DIE TRICH POINT CLEARPRINT 1020

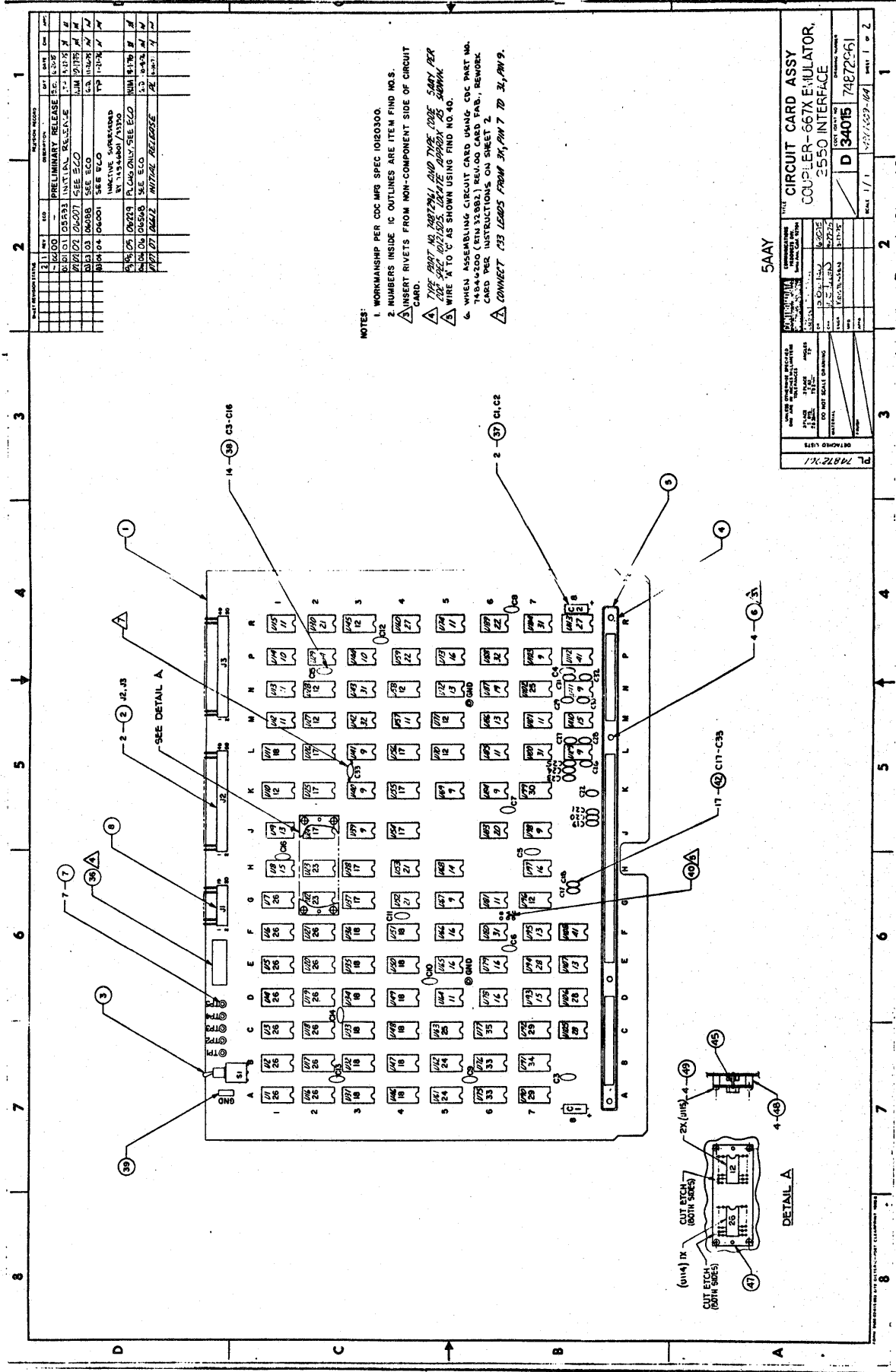
PRINTED IN U.S.A.

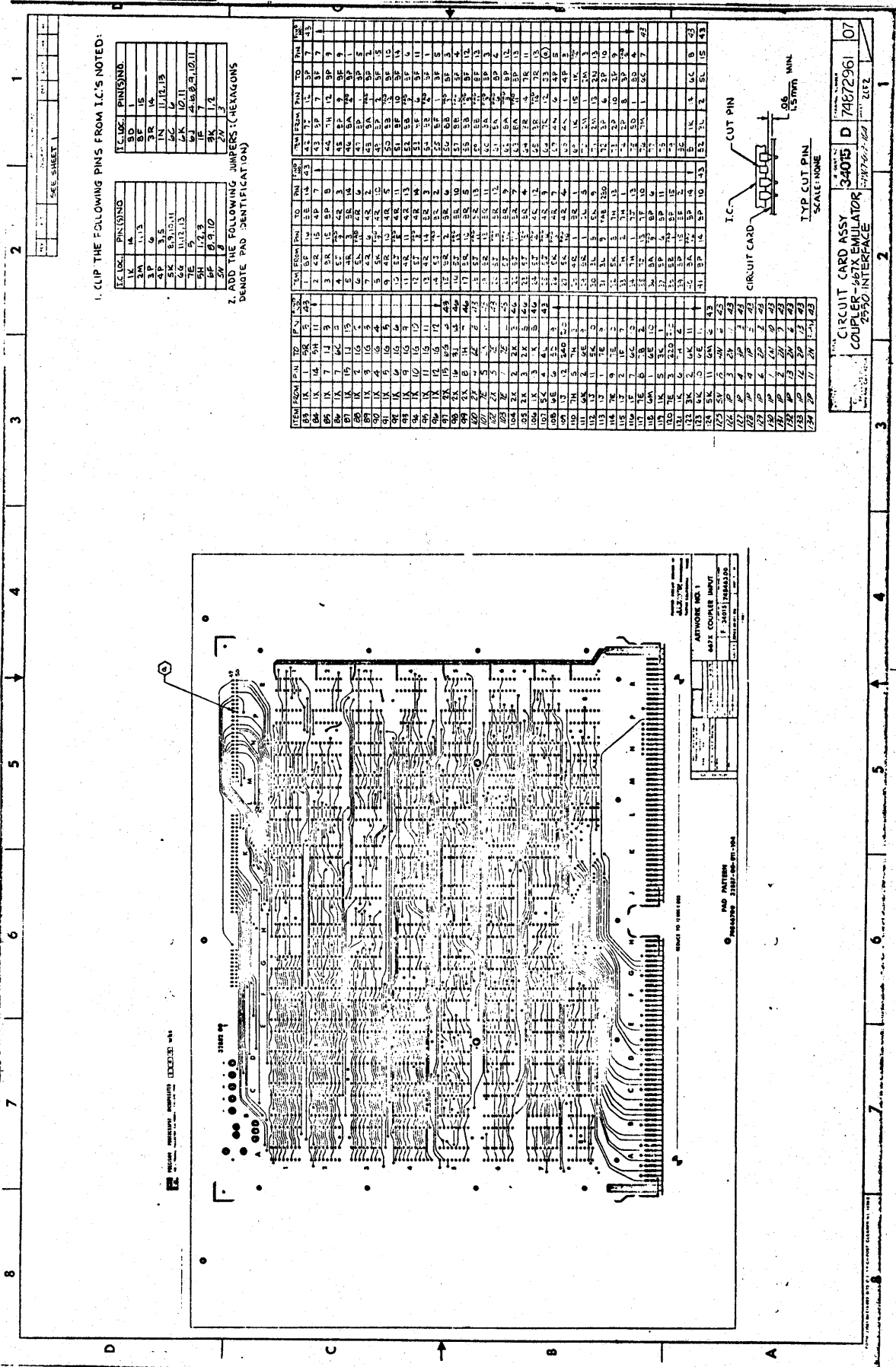
55002-009-104

COMMUNICATIONS PRODUCTS DIV. Santa Ana Calif 92704		CODE IDENT 34015	SHEET 3 OF 4		PL	DOCUMENT NO 74873038	REV 03	
LINE NO	PART IDENTIFICATION	QUANTITY REQUIRED			UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	TYPE	SPECIFICATIONS, NOTES, OR MATERIAL
21		22			PC	IC 74500	22124-002	
22		1			PC	74502	26100-002	
23		1			PC	74503	22948-002	
24		3			PC	74504	22125-002	
25		2			PC	74508	28452-002	
26		1			PC	74510	22949-002	
27		1			PC	7413	22737-002	
28		1			PC	74520	23745-002	
29		3			PC	74540	25105-002	
30		1			PC	74574	22126-002	
31	15109400	2			PC	745112	21074-002	
32		12			PC	74128	27743-002	
33		1			PC	745138	27678-002	
34		3			PC	745157	27689-002	
35		6			PC	745174	25121-002	
36		9			PC	745175	25122-002	
37		3			PC	93516	27645-002	
38	94262302	1			PC	DELAY LINE	27774-002	
39	74861002	1			PC	IC PROGRAMMED ROM 1M5G10 TYPE	33103-002 (U2B)	
40		5			PC	SWITCH, 8 POS, AMP	23587-002	

FORM 19247-01 01-69 092 DIE TECH PROC CLEARPRINT 1020

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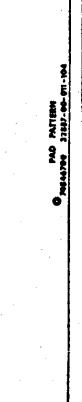
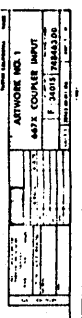


1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

IC LOG	PN(S)ND	PN(S)ND
1K	1	1
2A	2	2
3P	3	3
4P	4	4
5P	5	5
6P	6	6
7E	7	7
8H	8	8
9P	9	9
10A	10	10
11E	11	11
12K	12	12
13R	13	13
14S	14	14
15	15	15
16	16	16
17	17	17
18	18	18
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89	89	89
90	90	90
91	91	91
92	92	92
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94	94	94
95	95	95
96	96	96
97	97	97
98	98	98
99	99	99
100	100	100

2. ADD THE FOLLOWING JUMPERS (HEXAGONS DENOTE PAD IDENTIFICATION)

ITEM	FROM	TO	PN	PN	PN	PN	PN	PN	PN
101	1K	1	1	1	1	1	1	1	1
102	1K	2	2	2	2	2	2	2	2
103	1K	3	3	3	3	3	3	3	3
104	1K	4	4	4	4	4	4	4	4
105	1K	5	5	5	5	5	5	5	5
106	1K	6	6	6	6	6	6	6	6
107	1K	7	7	7	7	7	7	7	7
108	1K	8	8	8	8	8	8	8	8
109	1K	9	9	9	9	9	9	9	9
110	1K	10	10	10	10	10	10	10	10
111	1K	11	11	11	11	11	11	11	11
112	1K	12	12	12	12	12	12	12	12
113	1K	13	13	13	13	13	13	13	13
114	1K	14	14	14	14	14	14	14	14
115	1K	15	15	15	15	15	15	15	15
116	1K	16	16	16	16	16	16	16	16
117	1K	17	17	17	17	17	17	17	17
118	1K	18	18	18	18	18	18	18	18
119	1K	19	19	19	19	19	19	19	19
120	1K	20	20	20	20	20	20	20	20
121	1K	21	21	21	21	21	21	21	21
122	1K	22	22	22	22	22	22	22	22
123	1K	23	23	23	23	23	23	23	23
124	1K	24	24	24	24	24	24	24	24
125	1K	25	25	25	25	25	25	25	25
126	1K	26	26	26	26	26	26	26	26
127	1K	27	27	27	27	27	27	27	27
128	1K	28	28	28	28	28	28	28	28
129	1K	29	29	29	29	29	29	29	29
130	1K	30	30	30	30	30	30	30	30
131	1K	31	31	31	31	31	31	31	31
132	1K	32	32	32	32	32	32	32	32
133	1K	33	33	33	33	33	33	33	33
134	1K	34	34	34	34	34	34	34	34
135	1K	35	35	35	35	35	35	35	35
136	1K	36	36	36	36	36	36	36	36
137	1K	37	37	37	37	37	37	37	37
138	1K	38	38	38	38	38	38	38	38
139	1K	39	39	39	39	39	39	39	39
140	1K	40	40	40	40	40	40	40	40
141	1K	41	41	41	41	41	41	41	41
142	1K	42	42	42	42	42	42	42	42
143	1K	43	43	43	43	43	43	43	43
144	1K	44	44	44	44	44	44	44	44
145	1K	45	45	45	45	45	45	45	45
146	1K	46	46	46	46	46	46	46	46
147	1K	47	47	47	47	47	47	47	47
148	1K	48	48	48	48	48	48	48	48
149	1K	49	49	49	49	49	49	49	49
150	1K	50	50	50	50	50	50	50	50



ARTWORK NO. 1
447X COUPLER MOUNT
F 34011 ZHARASJZ
REV. 10/74

PAD PATTERN
REQD. 2187-00-01-104

SEND TO 1047-104

101	1K	1	1	1	1
102	1K	2	2	2	2
103	1K	3	3	3	3
104	1K	4	4	4	4
105	1K	5	5	5	5
106	1K	6	6	6	6
107	1K	7	7	7	7
108	1K	8	8	8	8
109	1K	9	9	9	9
110	1K	10	10	10	10
111	1K	11	11	11	11
112	1K	12	12	12	12
113	1K	13	13	13	13
114	1K	14	14	14	14
115	1K	15	15	15	15
116	1K	16	16	16	16
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118	1K	18	18	18	18
119	1K	19	19	19	19
120	1K	20	20	20	20
121	1K	21	21	21	21
122	1K	22	22	22	22
123	1K	23	23	23	23
124	1K	24	24	24	24
125	1K	25	25	25	25
126	1K	26	26	26	26
127	1K	27	27	27	27
128	1K	28	28	28	28
129	1K	29	29	29	29
130	1K	30	30	30	30
131	1K	31	31	31	31
132	1K	32	32	32	32
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135	1K	35	35	35	35
136	1K	36	36	36	36
137	1K	37	37	37	37
138	1K	38	38	38	38
139	1K	39	39	39	39
140	1K	40	40	40	40
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142	1K	42	42	42	42
143	1K	43	43	43	43
144	1K	44	44	44	44
145	1K	45	45	45	45
146	1K	46	46	46	46
147	1K	47	47	47	47
148	1K	48	48	48	48
149	1K	49	49	49	49
150	1K	50	50	50	50

CIRCUIT CARD ASSY
COUPLER-667X EMULATOR
2550 INTERFACE

34015 D 74872961 07

REV. 10/74

SCALE: NONE

SEE SHEET 1

1 2 3 4 5 6 7 8

A B C D

1 2 3 4 5 6 7 8

OWN	KIAN	6-18-75	K. KIAN	TITLE	CIRCUIT CARD ASSY	DOCUMENT NO.	74872961	REV	07
CHKD	W. J. FLO	8-27-75			COUPLER-66TX EMULATOR, 2550 INTERFACE	PREFIX	PL		
ENG	K. W. JENSEN	3-21-75		FIRST USED ON	34967-009-104				SHEET 1 OF 4
MTG				DY159-A					
APPR				CODE IDENT					
				34015					

SHEET REVISION STATUS										REVISION RECORD									
4	3	2	1	REV	ECO	DESCRIPTION	DRFT	DATE	APP	4	3	2	1	REV	ECO	DESCRIPTION	DRFT	DATE	APP
				00	00	PRELIMINARY RELEASE	JTP	6-18-75						00	00	PRELIMINARY RELEASE	JTP	6-18-75	
				01	01	INITIAL RELEASE	JTP	8-27-75	KL					01	01	INITIAL RELEASE	JTP	8-27-75	KL
				02	02	SEE ECO	WJM	10-17-75	KL					02	02	SEE ECO	WJM	10-17-75	KL
				02	03	SEE ECO	G.D.	11-26-75	KL					02	03	SEE ECO	G.D.	11-26-75	KL
				02	04	SEE ECO	T.P.	1-21-76	KL					02	04	SEE ECO	T.P.	1-21-76	KL
						INACTIVE SUPERSEDED BY 7484-6001 / 33390										INACTIVE SUPERSEDED BY 7484-6001 / 33390			
				05	05	SEE ECO	WJM	3-17-76	KL					05	05	SEE ECO	WJM	3-17-76	KL
				06	06	REVISED PER ECO	PL	10-28-76	KL					06	06	REVISED PER ECO	PL	10-28-76	KL
				07	07	INITIAL RELEASE	PL	4-14-77	KL					07	07	INITIAL RELEASE	PL	4-14-77	KL

NOTES:

DETACHED LISTS

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FORM 10248 01-01-012 DIETZICH POST CLEARPRINT 1020

34967-009-104

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704		CODE IDENT 34015	SHEET 2 OF 4	PL	DOCUMENT NO 74872961	REV 07	
FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED			UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	74846200	1			PC	CKT CARD FAB	32882-010
2		2			PC	HEADER, RT ANGLE -50	27926-00Z
3		1			PC	SWITCH TOGGLE, (SPDT)	28629-00Z
4	88895400	1			PC	STIFFENER	27299-00Z
5	88895500	1			PC	INSULATOR	27300-00Z
6	88812400	4			PC	RIVET	27301-00Z
7		7			PC	TERMINAL	01628-00Z
8		1			PC	HEADER RT ANGLE -20	28634-00Z
9		10			PC	IC 74S04 TYPE	22125-00Z
10		2			PC	74S11	23305-00Z
11		9			PC	74S00	22124-00Z
12		9			PC	74S112	21074-00Z
13		5			PC	74S02	26100-00Z
14		2			PC	74S32	28459-00Z
15		3			PC	74S30	27440-00Z
16		6			PC	74S10	22949-00Z
17		8			PC	74S157	27689-00Z
18		13			PC	93421	27643-00Z
19		1			PC	74S40	25105-00Z
20		1			PC	IC 74S260 TYPE	26098-00Z

FORM 19247 01 015 002 THE TELETYPE UNIT CLAIRPRINT 1020

PRINTED IN U.S.A.

34967-009-104

CONTROL DATA		COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704		CODE IDENT 34015	SHEET 3 OF 4	PL	DOCUMENT NO 74872961	REV 07
FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED			UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	TYPE	SPECIFICATIONS, NOTES, OR MATERIAL
21		3				IC 74393	IC	28513-002
22		2				7427		22736-002
23		2				745135		25114-002
24		2				DM8098		27446-002
25		2				74170		28511-002
26		14				93415		23869-002
27		2				745158		28512-002
28		3				74538		27955-002
29		2				745174		25121-002
30		1				745139		25116-002
31		4				74508		28452-002
32		3				74520		23745-002
33		2				IC DM6097	IC	27447-002
34		1				RESISTOR PACK 1KΩ	RESISTOR PACK	27309-002
35		1				RESISTOR PACK 2KΩ	RESISTOR PACK	27310-002
36		1				NAMEPLATE		15486-010
37		2				CAPACITOR, 100μF, 10V		19620-002
38		14				CAPACITOR, .01μF		21616-002
39		1				TEST JACK		27765-002
40		1				WIRE 24AWG, GRN		15167-002

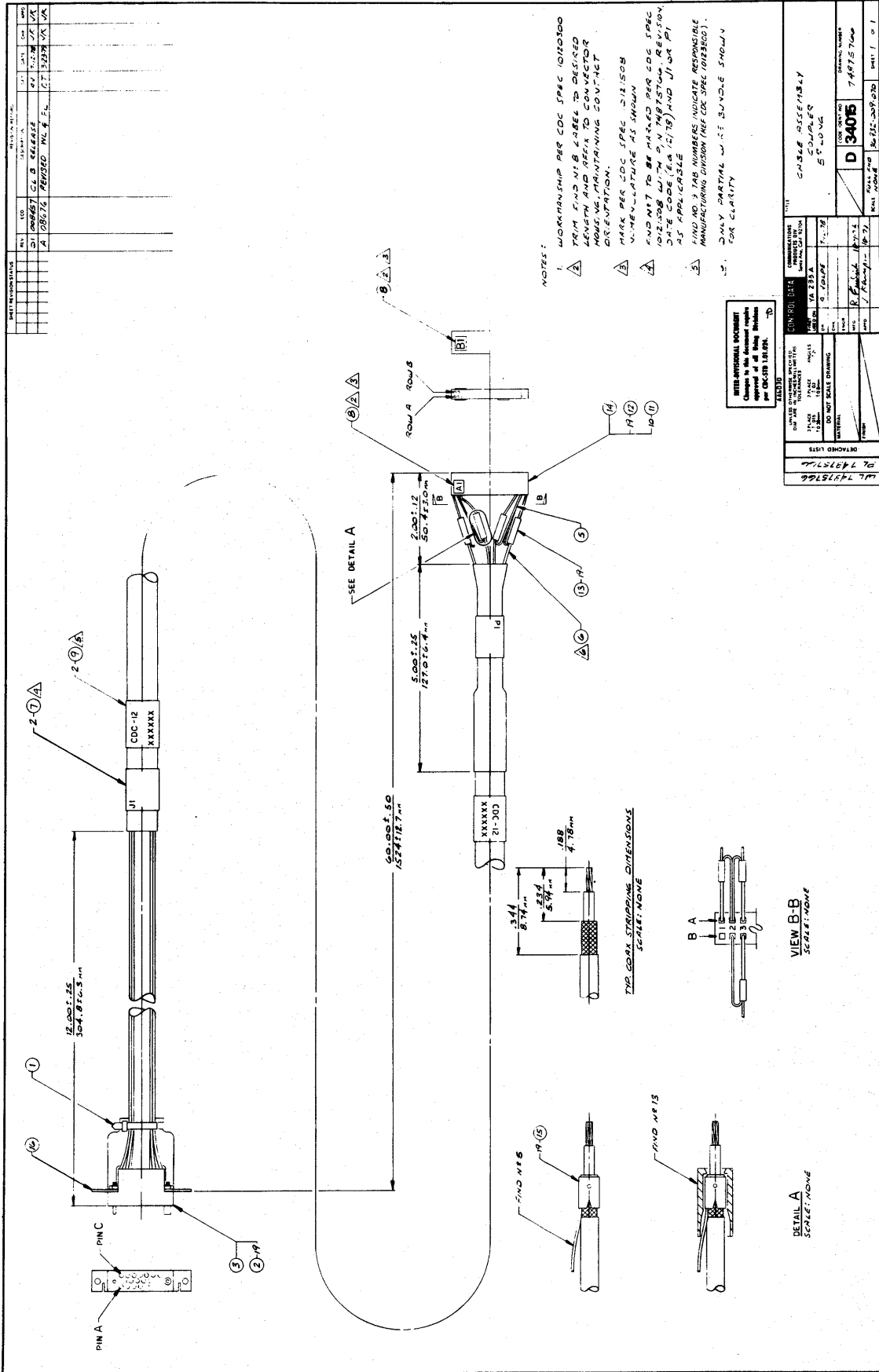
FORM 19247 01 016 002 BILTECH POST CLEARPRINT 1020

PRINTED IN U.S.A.

34967-009-104

COMMUNICATIONS PRODUCTS DIV. <small>Santa Ana, Calif. 92704</small>		CODE IDENT 34015	SHEET 4 OF 4	PL	DOCUMENT NO 74872961	REV 07		
FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED				UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
		✓						
41		2				PC	IC 8234 TYPE	28690-002
42		17				PC	CAPACITOR, 200PF	08278-002
43		5.0				FT	WIRE, 26GA, GRN	07952-002
44	74872962 REF					-	LOGIC DIAGRAM	RTN34967-012
45		0.2				FT	WIRE, 22GA BUSS	0930-002
46		1.0				FT	WIRE, 22GA, GRN	15009-002
47		1				PC	ADAPTER CARD	15865-010
48		4				PC	STANDOFF	15183-002
49		4				PC	SCREW, 2-56	06293-002

FORM 1924/ 01 010 002 FBI TELETYPE CENTER PRINT 1020 PRINTED IN U.S.A.



REV	DATE	BY	CHK	APP
1	08/27/74	REVISED	MLG	FK
2	07/15/74	REVISED	MLG	FK
3	07/15/74	REVISED	MLG	FK

WORKSHIP PER CDC SPEC 1010300
 TRIM FIND NIB LABEL TO DESIRED
 LENGTH AND REFER TO CONNECTOR
 HOWELV. MAINTAINING COV-1CT
 CREATION.

MARK PER CDC SPEC 1010300
 V-MEN-LATURE AS SHOWN

FIND NIB TO BE MARKED PER CDC SPEC
 1010300 WITH 5 N PARTITION, REVISION,
 AS APPLICABLE (1-17) AND U/J OR M

FIND NO 3 FOR NUMBERS INDICATE RESPONSIBLE
 MANUFACTURING DIVISION (PER CDC SPEC 1010300).

ONLY PARTIAL W. SEE BUDDLE SHOW N
 FOR CLARITY

REV	DATE	BY	CHK	APP
1	08/27/74	REVISED	MLG	FK
2	07/15/74	REVISED	MLG	FK
3	07/15/74	REVISED	MLG	FK

CONTROL DATA	
DATE OF ISSUE	17/82
DATE OF REVISION	17/82
ISSUE NO.	1
REV NO.	1
SCALE	DO NOT SCALE DRAWING
DESIGNER	W. J. JONES
DRWING NUMBER	74875706
SCALE	1:1
DATE	10/12/74
BY	W. J. JONES
CHKD	W. J. JONES
APPD	W. J. JONES

INTERNAL DOCUMENT
 Change in all dimensions
 per 62-218 I.R.S.P.

74875706
 62-218 I.R.S.P.

ENCLOSURE LIST

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE

SCALE: NONE



ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

74875766	A	CLA	A	CABLE W/ASY CYRFX COUPLER	DM	2551	08/30/78	03/27/79	1 / 1
ASSEMBLY NUMBER	REV	CLASS	QW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

FIND NUMBER	QW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IS/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PU NC	Q OF N
1	A	10123801	200	PC	LABEL - CABLE MARKING	IN	008676	032770			N
2	A	10123805	200	PC	LABEL CABLE W/4 CIRC 12 STAPPS	IN	008676	032770			N
1	C	17620301	100	PC	STAP CABLE ADJUSTABLE	IN			PPP4		N
2	C	14752711	1400	PC	SINGLE PTFE CONTACT - COAX	IN			PPP4		N
3	C	14752719	100	PC	CONN COAX KEYED JACKS MULTI POS	IN			PPP4		N
4	C	24544714	700	IN	SLEEVING FLEC SHRINKABLE HULK	IN			PPP4		N
5	C	24544901	4400	IN	WTFE PLECT+24 GA+VVCUL+BLK	IN			PPP4		N
6	C	24547000	500	ET	CABLE COAXIAL 19 COND. 0.730MM	IN			PPP4		N
7	C	51984701	200	PC	CABLE LABEL	IN			PPP4		N
8	C	74789300	100	PC	LABEL CONTACT CAVITY	IN			PPP4		N
11	C	94245601	1000	PC	CONTACT-CRIMP INSERT SOCKET	IN			PPP4		N
12	C	94245604	1400	PC	CONTACT-CRIMP INSERT SOCKET	IN	008676	032770			N
13	A	94278A13	1900	PC	FERRULE INSULATOR	IN			PPP4		N
14	C	94260A07	100	PC	HOUSING-CONN. SOCKET #125 30CAV	IN			PPP4		N
15	C	94271108	1400	PC	FERRULES GW UNINSULATED	IN			PPP4		N
16	C	97177604	100	PC	STRAIN RELIEF	IN					N

NUMBER OF LINE ITEMS = 16
HIGHEST FIND NUMBER = 16

AA 2700 REV. 7-78

PROJECT ENGINEER SANTA ANA

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DWN	C TICE	3-79	TITLE	CABLE, 19-CONDUCTOR COAX	PREFIX	WL	DOCUMENT NO.	74875766	REV	A																		
CHKD	KK	3/79	COMMUNICATIONS SYSTEMS DIV.	Santa Ana, Ca. 92704	FIRST USED ON	YA233-A	SHEET 1 OF 3																					
ENG	EDC	3/79	CODE IDENT	34015	REVISION RECORD																							
MFG	R. R. ...	3-79	SHEET REVISION STATUS																									
APP	✓ K. M. P.	3-79	<table border="1"> <thead> <tr> <th>REV</th> <th>ECO</th> <th>DESCRIPTION</th> <th>DRFT</th> <th>DATE</th> <th>APP</th> </tr> </thead> <tbody> <tr> <td>3</td> <td>2</td> <td>1</td> <td>CT</td> <td>3-23-79</td> <td>JK</td> </tr> <tr> <td>A</td> <td>A</td> <td>A</td> <td>CT</td> <td>3-23-79</td> <td>JK</td> </tr> </tbody> </table>								REV	ECO	DESCRIPTION	DRFT	DATE	APP	3	2	1	CT	3-23-79	JK	A	A	A	CT	3-23-79	JK
REV	ECO	DESCRIPTION	DRFT	DATE	APP																							
3	2	1	CT	3-23-79	JK																							
A	A	A	CT	3-23-79	JK																							
NOTES:																												
DETACHED LISTS																												

CONTROL DATA				COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704		CODE IDENT 34015	SHEET 2 OF 3		WL	DOCUMENT NO. 74875766	REV. A
CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	6	30	90	5 FT	J1	A	2	P1	A1	12,13,15	COND. } TYP. 13 PLCS SHIELD
2	↑	↑		↑					A2	5,11	
3			91			B			B3	12,13,15	
4									B2	5,11	
5			92			C			A3	12,13,15	
6									A2	5,11	
7			93			D			B4	12,13,15	
8									B5	5,11	
9			94			E			A4	12,13,15	
10									A5	5,11	
11			95			F			B6	12,13,15	
12									B5	5,11	
13			96			H			A6	12,13,15	
14									A5	5,11	
15			97			J			B7	12,13,15	
16									B8	5,11	
17			98			K			A7	12,13,15	
18									A8	5,11	
19			9			L			B9	12,13,15	
20									B8	5,11	
21			900			M			A9	12,13,15	
22									A8	5,11	
23			910			N			B10	12,13,15	
24									B11	5,11	
25			920			P			A10	12,13,15	
26	6	30		5 FT	J1			P1	A11	5,11	

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020

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COMMUNICATIONS SYSTEMS DIV. Santa Ana, Calif. 92704				CODE IDENT 34015	SHEET 3 OF 3		WL	DOCUMENT NO. 74875766	REV. A		
CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
27	6	30	930	5 FT	J1	R	2	P1	B12	12,13,15	COND. } TYP. 6 PLCS SHIELD
28	↑	↑		↑					B11	5,11	
29			940			S			A12	12,13,15	
30									A11	5,11	
31			950			T			B13	12,13,15	
32									B14	5,11	
33			960			U			A15	12,13,15	
34									A14	5,11	
35			970			V			B15	12,13,15	
36									B14	5,11	
37			980			W			A13	12,13,15	
38	6	30		5 FT	J1		2	P1	A14	5,11	

FORM 23562-01-015-092 DIETERICH-POST CLEARPRINT 1020

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GLOSSARY

A

Some of the terminology used in the manual was shortened to simplify explanations.

This glossary relates the shortened terms to the terms used on the logic diagrams.

Circular buffer	circular buffer memory	MA bus	memory address bus
CLA	communications line adapter	Maintenance ROM	maintenance address ROM
CLE	communications line expansion	MH register	maintenance hold flag register
Coupler	667X Emulation Coupler	Modems	modulator and demodulator
Coupler buffer	coupler buffer memory	MP	microprocessor
Coupler select switch	MP equipment select switch	NPU	network processor unit
DFM bus	data from memory bus	Operational ROM	operational address ROM
DIP	dual in-line package	PPU	peripheral processor unit
DMA	direct memory access	Processor	microprocessor
DTM bus	data to memory bus	Protect RAM	memory protect bit RAM
F register	function register	RAM	random-access memory
FDC register	from data channel register	Reject RAM	PPU character reject RAM
Host	peripheral processor	ROM	read-only memory
IDC	internal data channel	S register	status register
Interface	2550 interface circuit card	Synchronizer	channel synchronizer circuit card
Inverter	line inverter	TC control	terminal count logic
		TDC register	to data channel register
		Y-line decoder	MP address decoder



MNEMONIC LISTING

B

Some of the mnemonics used in the logic diagrams of the coupler are built from a prefix, a signal, and a suffix. The prefix gives the source of the signal, and the suffix gives the location of the signal. While a third type of mnemonic includes a number which indicates that it is one of

a series of bits emanating from the source. Rather than offer a complete (and redundant) list of mnemonics, this appendix lists all of the building blocks which are used to make up mnemonics. Wherever confusion could exist, entire mnemonics are listed.

AREADY	address ready	FRCLEAR	function register
B9A14WE	bits 9 and 14 write enable	FULLF	full flip-flop
CBA5	circular buffer address bit 5, 1 of 8	GND	ground
CBM100	coupler buffer memory bit 10 out	...I	in or increment (counter) or initialize (memory)
CBMT	circular buffer empty	...L	load
CBMTF	circular buffer empty flip-flop	...M	modified
CBUF	circular buffer	MAB02	memory address bus bit 2, 1 of 10
CBUFCE	circular buffer cycle enable	MAC03	memory address counter bit 3, 1 of 10
CBUFI	circular buffer initialize	MACI	memory address counter increment
CBWE	circular buffer write enable	MAINT	maintenance
CDENA	control decoder enable	MMWE	master memory write enable
...CE	cycle enable	MP...	microprocessor (the processor)
CLK01I	clock 1 MHz in	MPINC	microprocessor increment counter
CLK10I	clock 10 MHz in	MPMARI	MP memory access reply initiate
CRWE	character reject write enable	NREPLY	negative reply
CSEL	coupler selected	...O	out
DFM6	data from memory bit 6, 1 of 12	PB...	pass back
DTM7	data to memory bit 7, 1 of 12	PB04I	pass-back data bit 4 in, 1 of 12
ECBM	enable coupler buffer memory	PO...	pass on
ENAMT	enable maintenance	SEND...	send
ENAOP	enable operation	...A...	active
...F	flip-flop	...E...	empty
FDC8	from data channel bit 8, 1 of 12	...F...	full
FDCL	from data channel load	...FN...	function
FMP01	from microprocessor bit 1, 1 of 12	...I...	inactive
FR09	function register bit 9, 1 of 12		

...MC... master clear
...P... parity
PP... peripheral processor (the host)
PROT protect
RD05 receive data bit 5, 1 of 16
SD06 send data bit 6
SRI status register initialize
T40 time 40, 1 of several 10 MHz
clocks

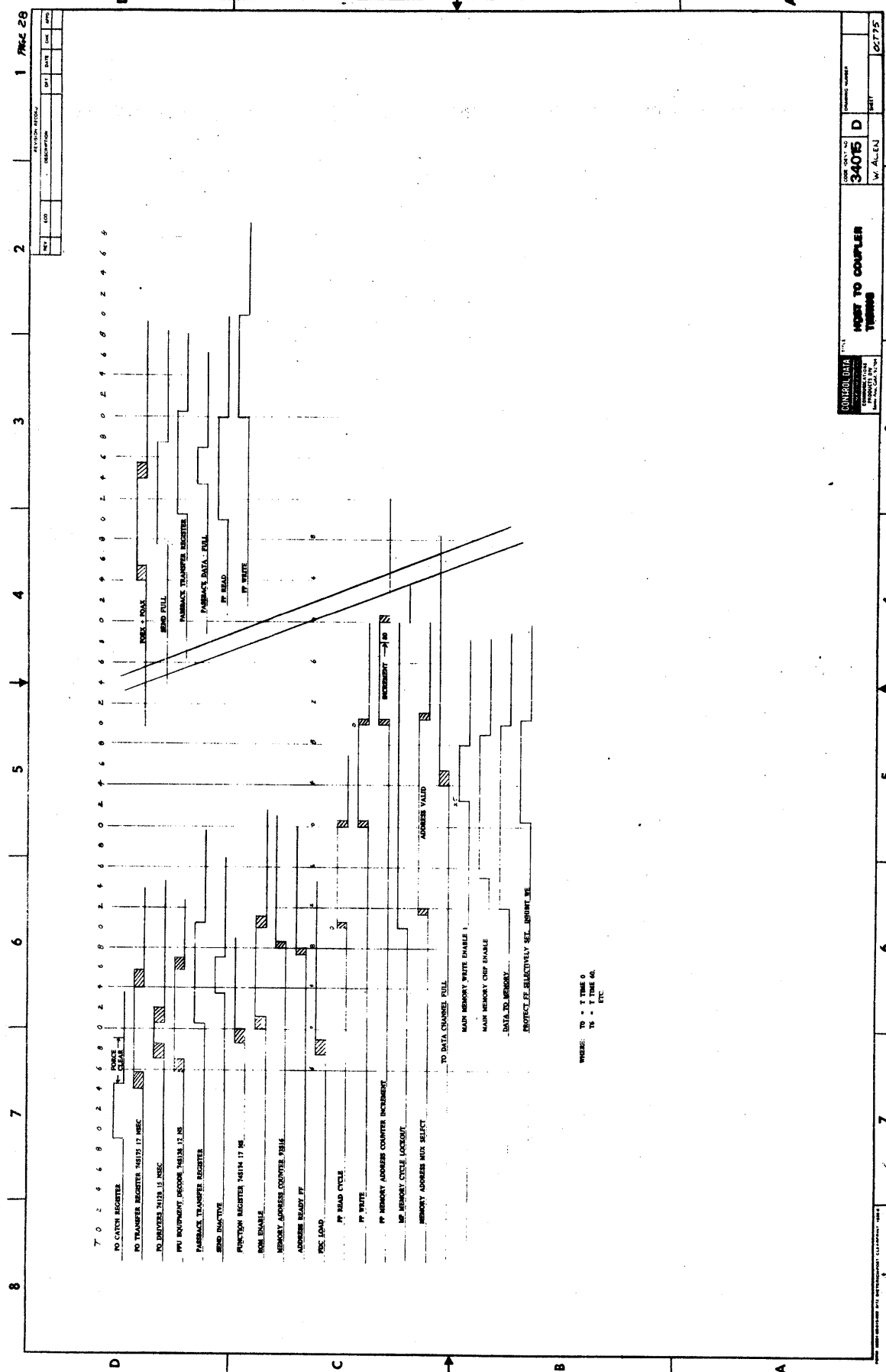
TC terminal count
TCC terminal count complete
TDC07 to data channel bit 7, 1 of 12
TMPC timed microprocessor cycle
TMPCE timed microprocessor cycle enable
...WE write enable
...X coupler internal
Y12 Y line bit 12

TIMING DIAGRAMS

C

The timing diagrams in this appendix relate signals to time in nanoseconds. Multiply

the number at the top of the diagram by 10 to arrive at the relative time in nanoseconds.

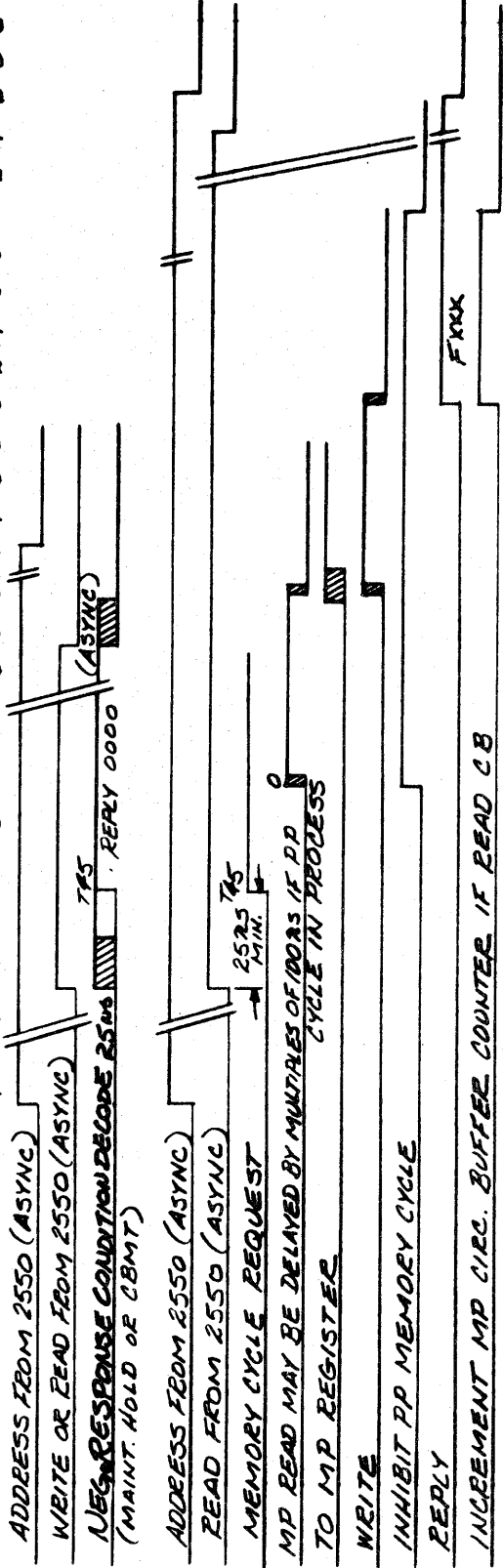


WHERE: T0 = 1 TIME 0
 T1 = 1 TIME 0
 ETC

REV	LOG	DESCRIPTION	DATE	BY	CHK	APP
1						

CONTROL DATA
 MODEL NO. 34015 D
 W. ALLEN
 6/17/75

T 0 2 4 6 8 0 2 4 6 8 0 2 4 6 8 0 2 4 6 8 0 2 4 6 8 0 2 4 6 8 0



WHERE :

$T_0 = T \text{ TIME } 0$
 $T_6 = T \text{ TIME } 60, \text{ ETC.}$

Processor to Coupler Timing



DATA WORD FUNCTION CODES

D

The upper 4 bits (8 through 11) of the output word provide I/O control and act, in various combinations, either as a flag for data characters or as a control for the modem. Any data to be transmitted

must be accompanied by either a 4XXX or a 5XXX function code.

Table D-1 describes the meaning of the upper four control bits. The output data word is in reference to data from the host.

TABLE D-1. DATA WORD FUNCTION CODES

Code	General Description
0XXX	A do-nothing function; no data is transferred.
1XXX	Enables the receiver section of the DCS to resync. Does not affect the carrier or the line connection. No data should be contained in this word.
2XXX	Turns off the carrier. No data should be contained in this word.
3XXX	Turns off the carrier and allows the receiver to resync. No data should be contained in this word. The valid data character preceding this function code is transmitted prior to carrier turn-off. Note that MPC's appended to a clocked-data modem message are considered to be valid data characters.
4XXX	Turns on the carrier. Must be appended to all data words (see 5XXX code description).
5XXX	Turns on the carrier and resyncs the receiver. Can contain data to be transmitted; primarily a function for Full-Duplex operation. Should be used whenever it is desirable to resync the receiver and transmit data simultaneously.
6XXX	Resyncs the receiver, turns off the carrier, and disconnects the telephone connection. No data should be contained in this word. Used primarily to disconnect the phone line.
	NOTE
	The 2XXX, 3XXX, and 6XXX codes await the disassembly of the previous valid character before they affect the carrier; 4XXX and 5XXX codes act immediately. The 6XXX code does not wait for completion of the last bit of the last output character before becoming active. Software timing for the use of the 6XXX code is desirable.
7XXX	Resyncs the receiver and enables the telephone connections for data transmissions. This word contains no information to be transmitted.
X (lxx) XX (Bit 8 set)	Used to disconnect a modem when output operation has failed in the middle of a character. Indicates that any valid character in the Output Buffer should be ignored, and that any data accompanying the function code should be transferred into the buffer memory. The DSC does not recognize that it is disassembling a character on this terminal and it executes the incoming function.



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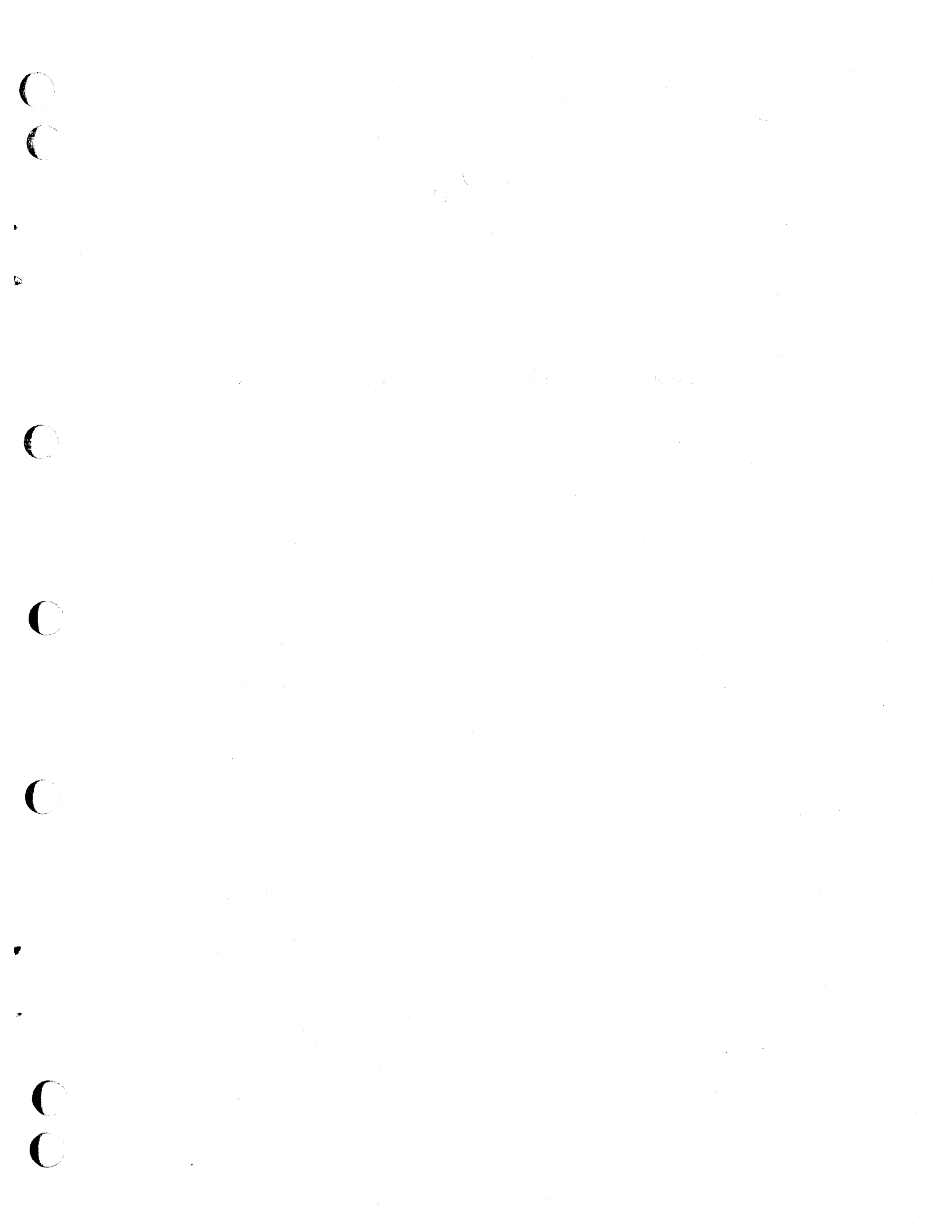
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