

6638 DISK FILE SUBSYSTEM

TRAINING SUPPLEMENT

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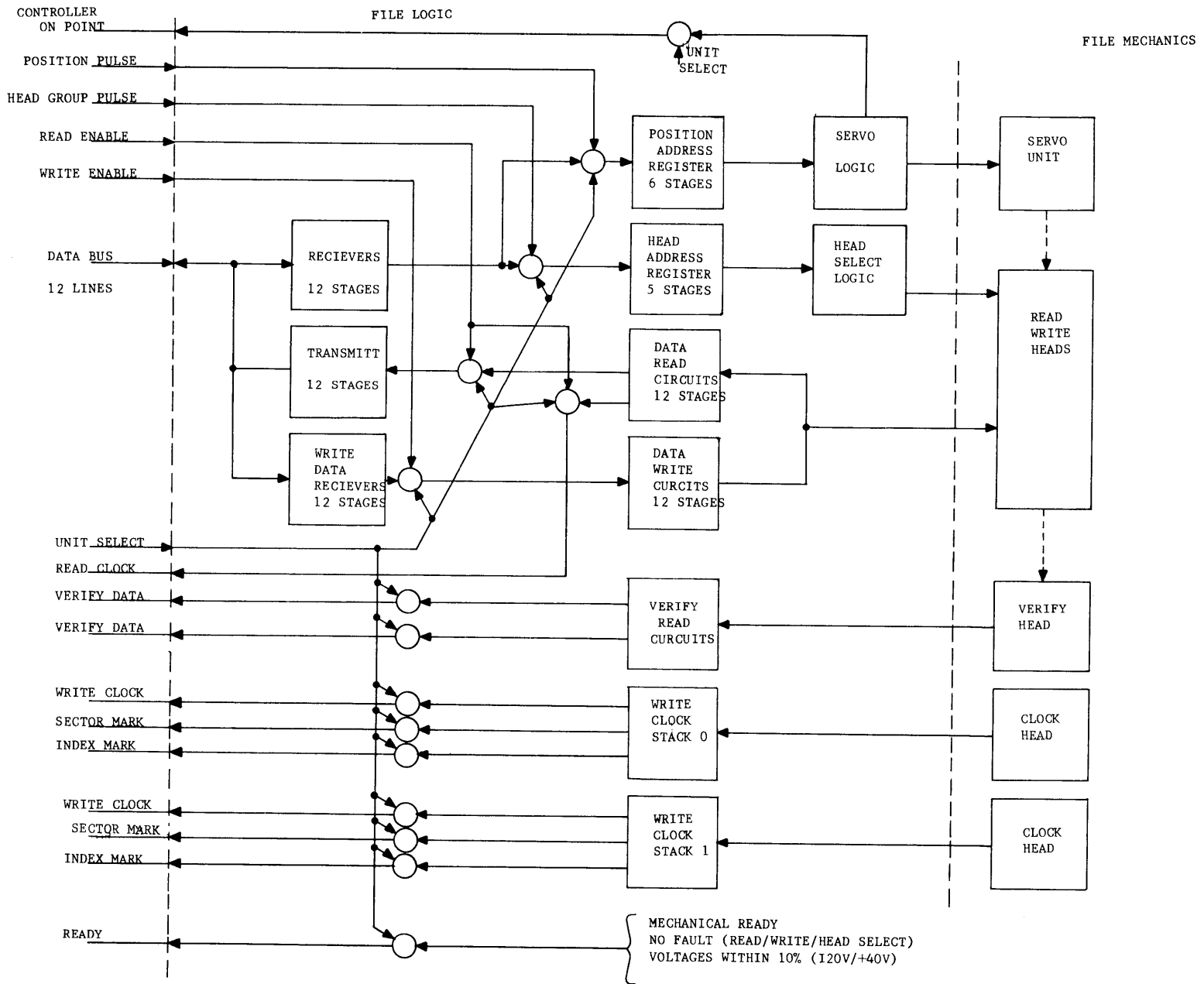
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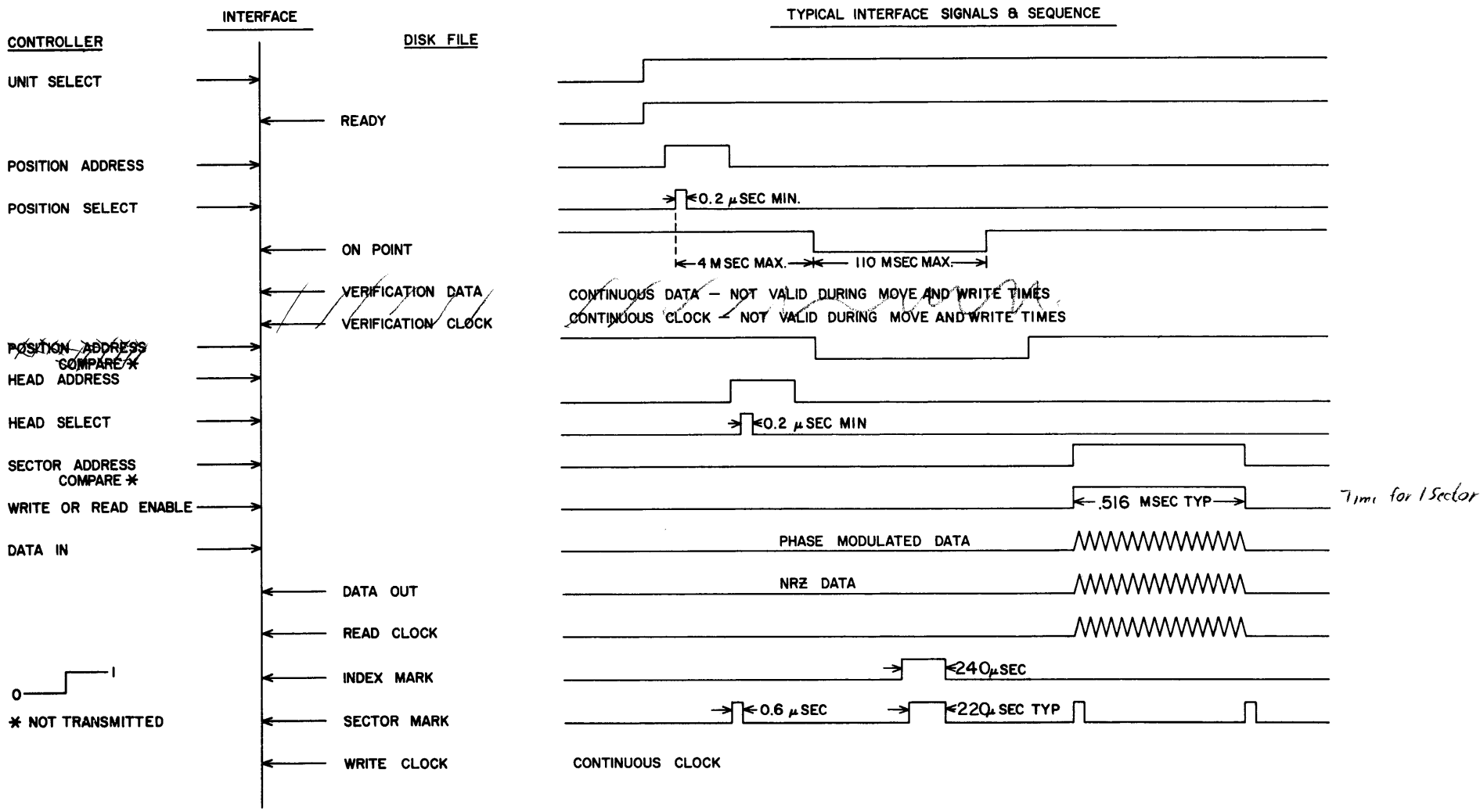
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CONTROL DATA CORPORATION

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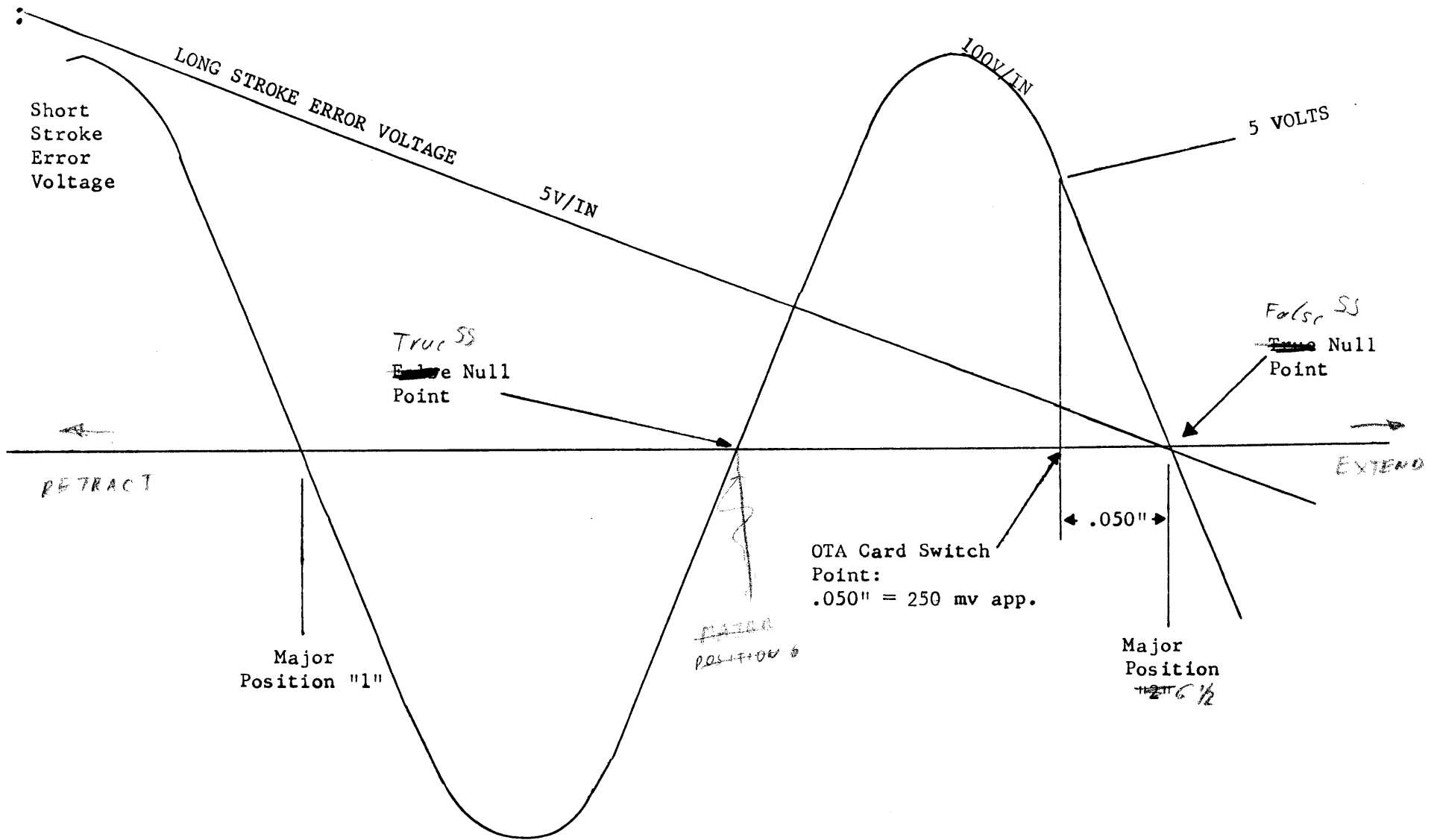


807/808 BLOCK DIAGRAM



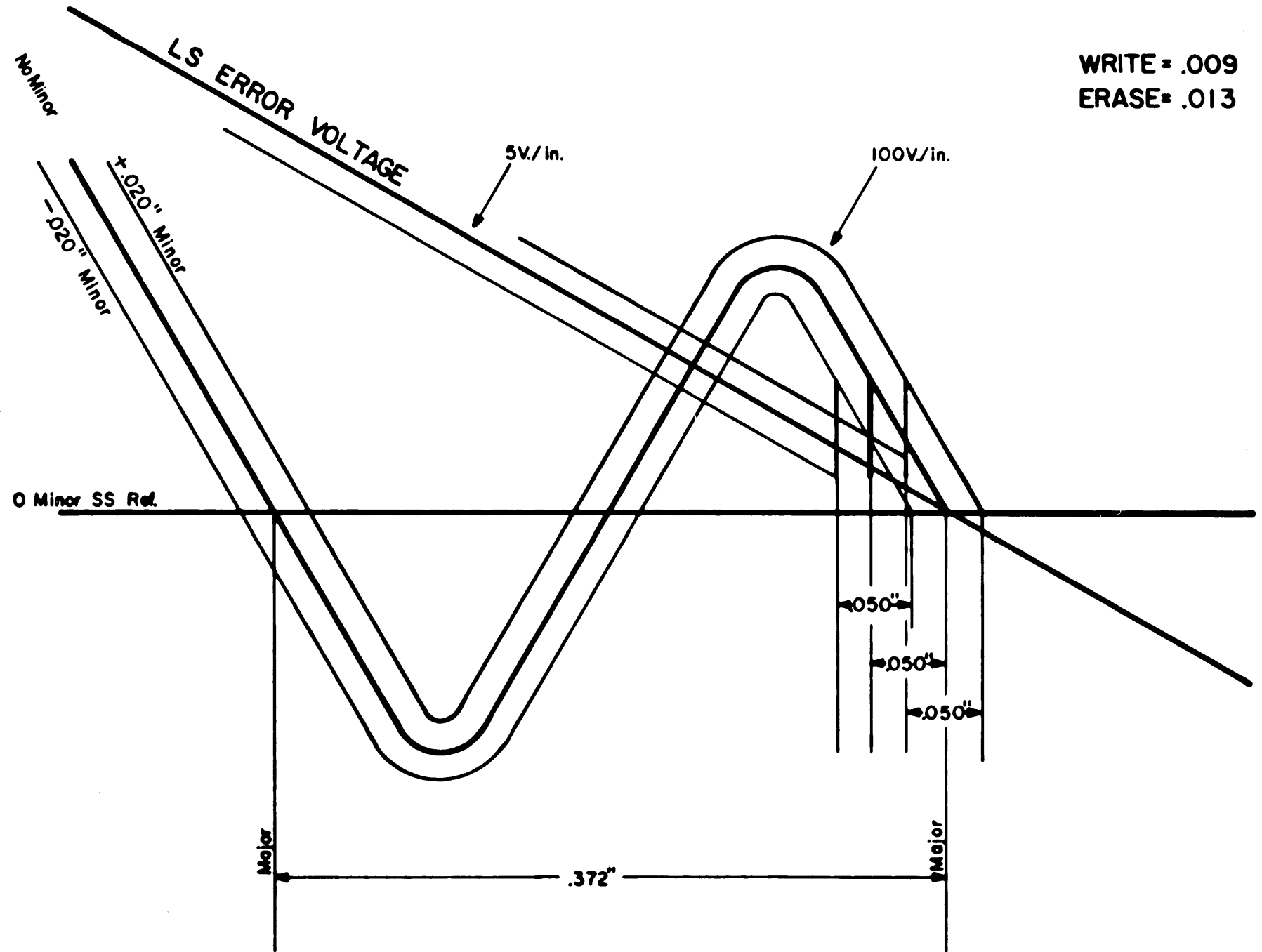
Typical Interface Signals





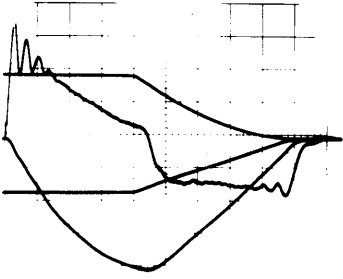
LONG STROKE, SHORT STROKE ERROR VOLTAGES

WRITE = .009  
ERASE = .013

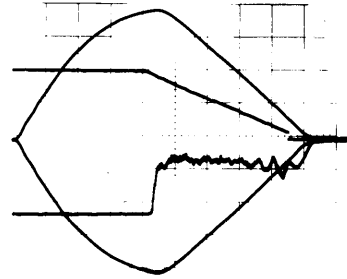




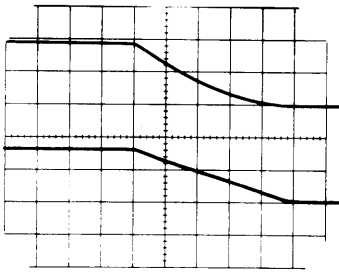
SERVO WAVEFORMS



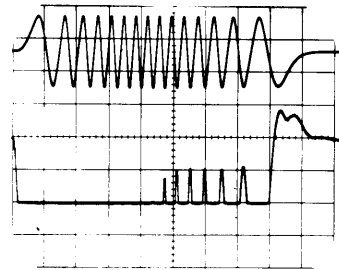
1. V(2v) A(2v) LS(5v) correct  
Seek 0 to 15 10 ms/cm



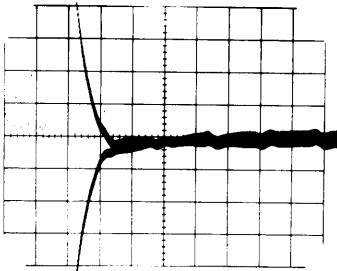
2. V(2v) IL(.5v) correct  
Seek 0 to 15 10ms/cm



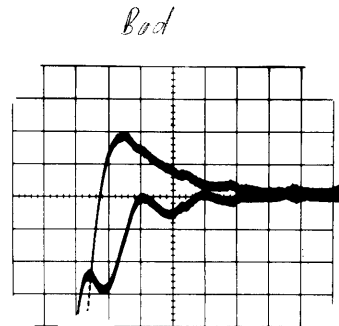
3. LS(5v) FG(5v) inverted correct  
Seek 0 to 15 10ms/cm



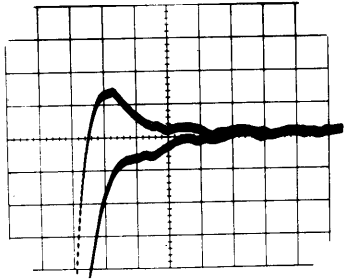
4. SS(5v) SM(5v) correct  
Seek 0 to 15 10ms/cm



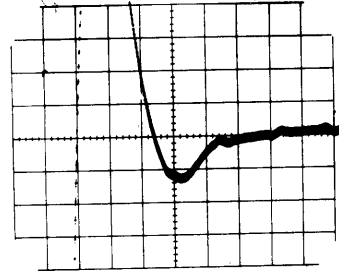
5. SS(.1v) correct  
Seek  $\pm$  22.5 5ms/cm



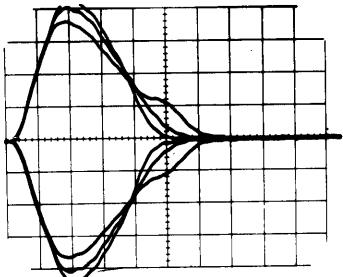
6. SS(.1v) approx. 4 turns either  
way E39B Seek  $\pm$  22.5 5ms/cm



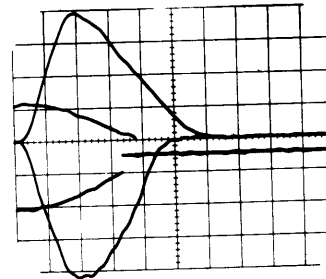
7. SS(.1v) approx. 8 turns either way F42 Seek  $\pm$  22.5 5ms/cm



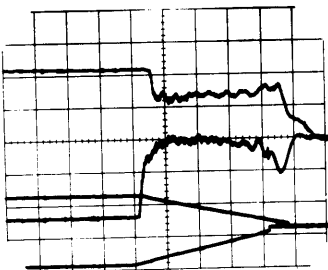
8. SS(.1v) many turns out F42 Seek  $\pm$  22.5 5ms/cm



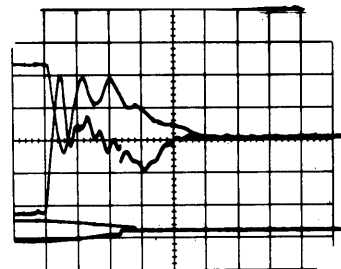
9. V(.5v) adjustment of C46A correct and bad Seek 8 to 9 5ms/cm



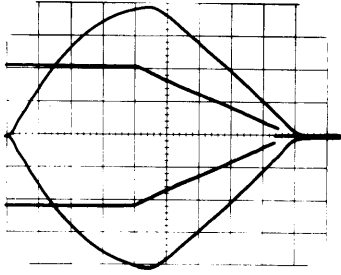
10. V(.5v) IL(.2v) approx 8 turns D23 Seek 8 to 9 5ms/cm



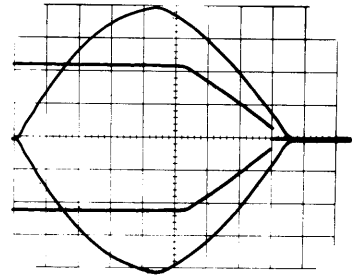
11. IS(.5v) IL(1v) approx 8 turns D23 Seel 8 to 9 5ms/cm



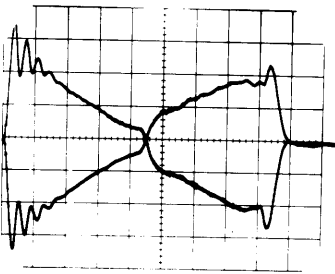
12. IS(.5v) IL(1v) approx 8 turns D23 Seek 8 to 9 5ms/cm



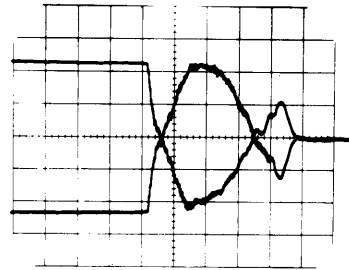
13. V(2v) IL(5v) Seek 0 to 15  
Correct 10ms/cm



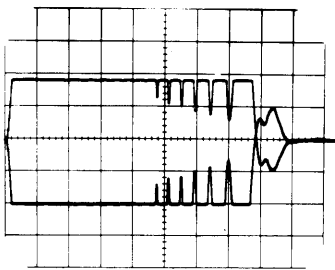
14. V(2v) IL(.5v) 20 turns cw  
C43 Seek 0 to 15 10ms/cm



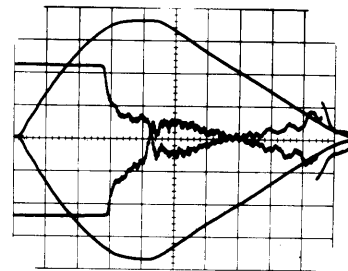
15. A(2v) 20 turns cw C43  
Seek 0 to 15 10ms/cm



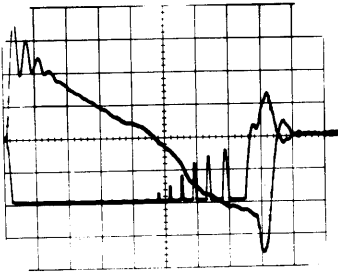
16. IS(15v) 20 turns cw C43  
Seek 0 to 15 10ms/cm



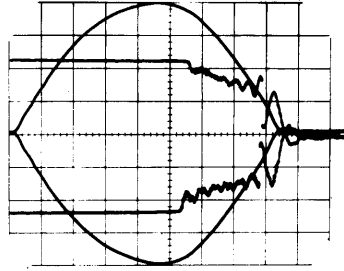
17. SM(5v) 20 turns cw C43  
Seek 0 to 15 10ms/cm



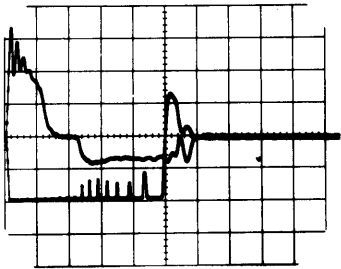
18. V(2v) IS(.5v) 6 turns cw F47  
Seek 0 to 15 10ms/cm



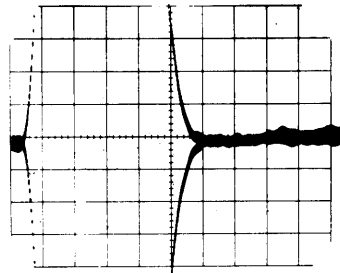
19. A(2v) SM(5v) 10 turns ccw F47  
Seek 0 to 15 10ms/cm



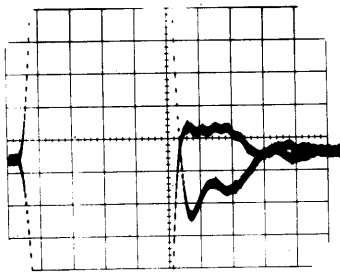
20. V(2v) IS(.5v) 10 turns ccw F47  
Seek 0 to 15 10ms/cm



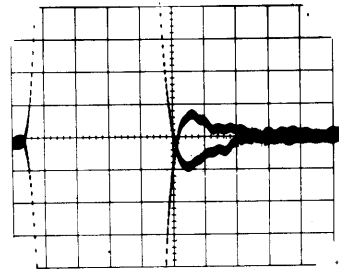
21. SM(5v) A(5v) 10 turns ccw F47  
Seek 0 to 15 10ms/cm



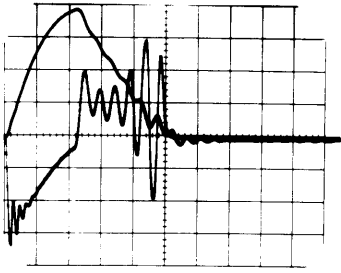
22. SS(.1v) correct  
Seek 8 to 9 5ms/cm



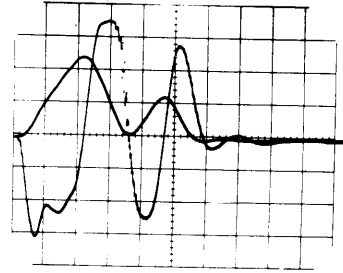
23. SS(.1v) 13 turns ccw C46B  
Seek 8 to 9 5ms/cm



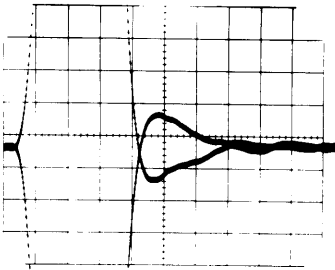
24. SS(.1v) 18 turns ccw C46B  
Seek 8 to 9 5ms/cm



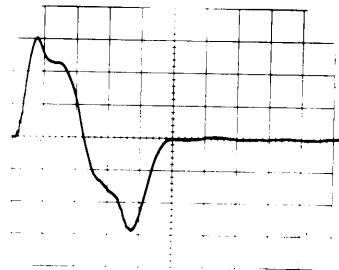
25. V(2v) A(2v) 13 turns ccw C46B  
Seek 0 to 15 20ms/cm



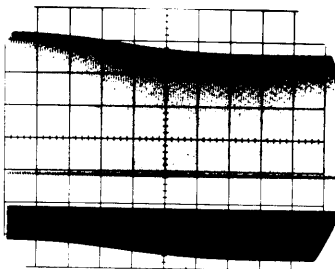
26. V(1v) A(2v) 13 turns ccw C46B  
Seek 0 to 1 5ms/cm



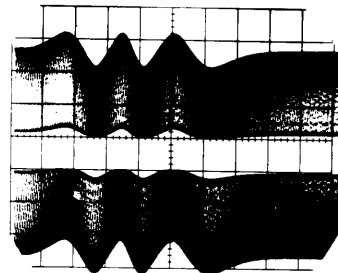
27. SS(.2v) 10 turns ccw F47  
Seek 8 to 9 5ms/cm



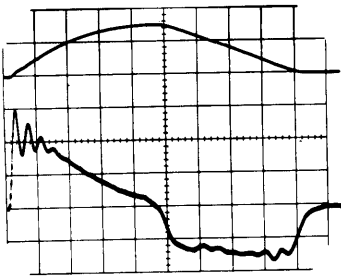
28. A(2v) 13 turns ccw C46B  
Seek 8 to 9 5ms/cm



29. LS x'ducer at TP A&C of FKA card  
Seek 0 to 3 (5v) 5ms/cm



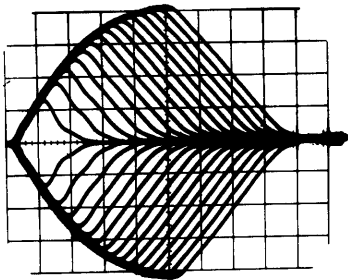
30. SS x'ducer at TP A&C of FKA card  
Seek 0 to 3 (5v) 5ms/cm



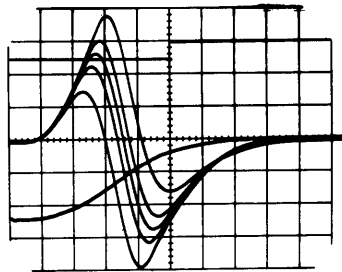
31. V(5v) P(.5v)  
Seek 0 to 15 10ms/cm



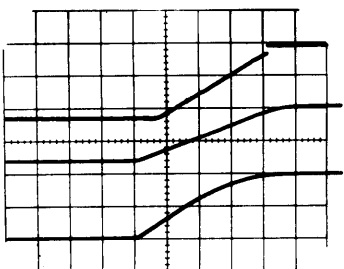
32. A(.5v) diff. P(.1v) diff. spikey  
Seek 0 to 15 10ms/cm



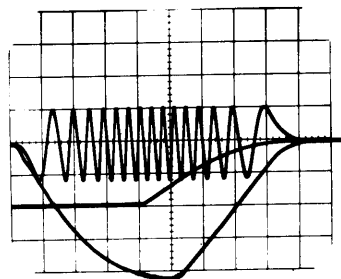
33. V(2v) profile seeks  
15 thru 1 to 0 10ms/cm



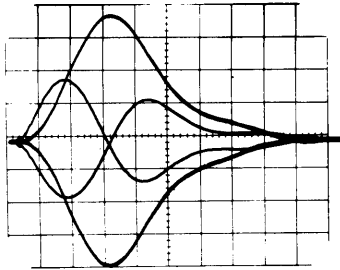
34. SS(2v) LS(.5v) LS-SS(5v) rela-  
tionships of all minor positions  
uncalibrated



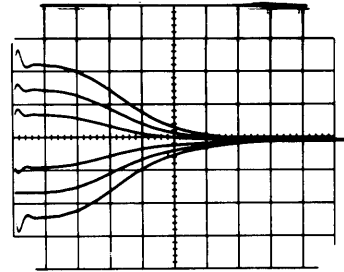
35. FG(5v) IL(.5v) LS(5v) inverted  
Seek 0 to 15 10ms/cm



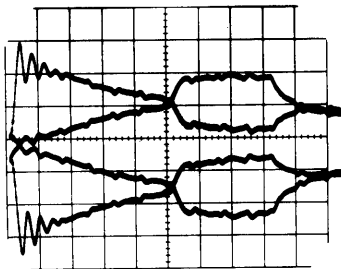
36. SS(5v) LS(5v) inverted  
Seek 0 to 15 10ms/cm



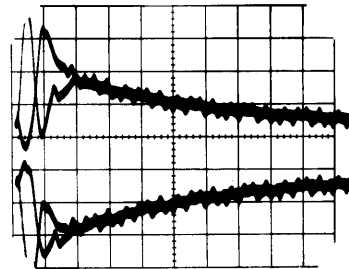
37. A(2v) V(.2v)  
Seek  $\pm 22.5$  2ms/cm



38. SS(2v)  $\pm 22.5$ ,  $\pm 7.5$ , and  
 $\pm 7.5$  to  $-22.5$  2ms/cm

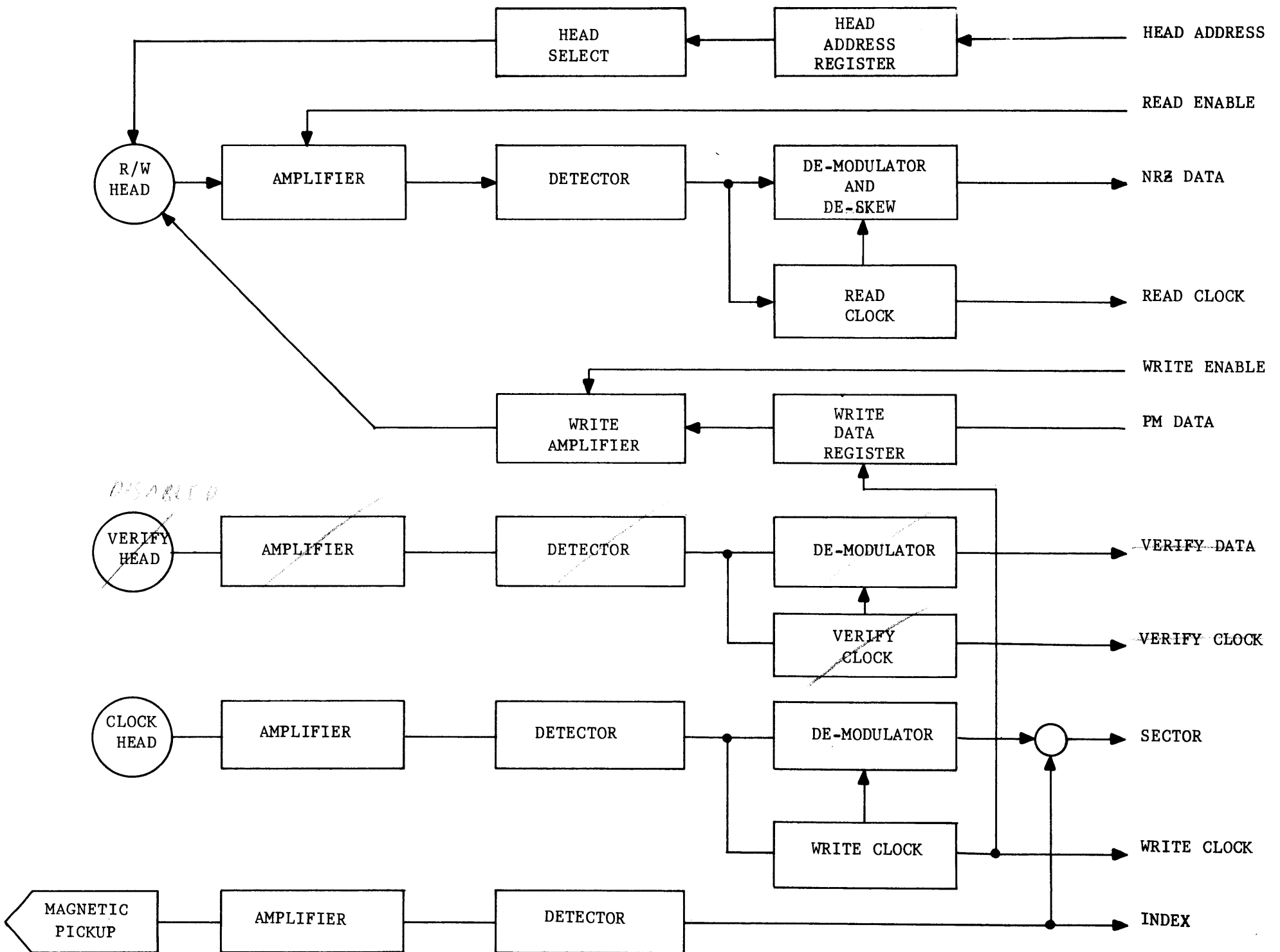


39. F53(.05v) F55(.05v)  
Seek 0 to 15 10ms/cm  
(Pressure)

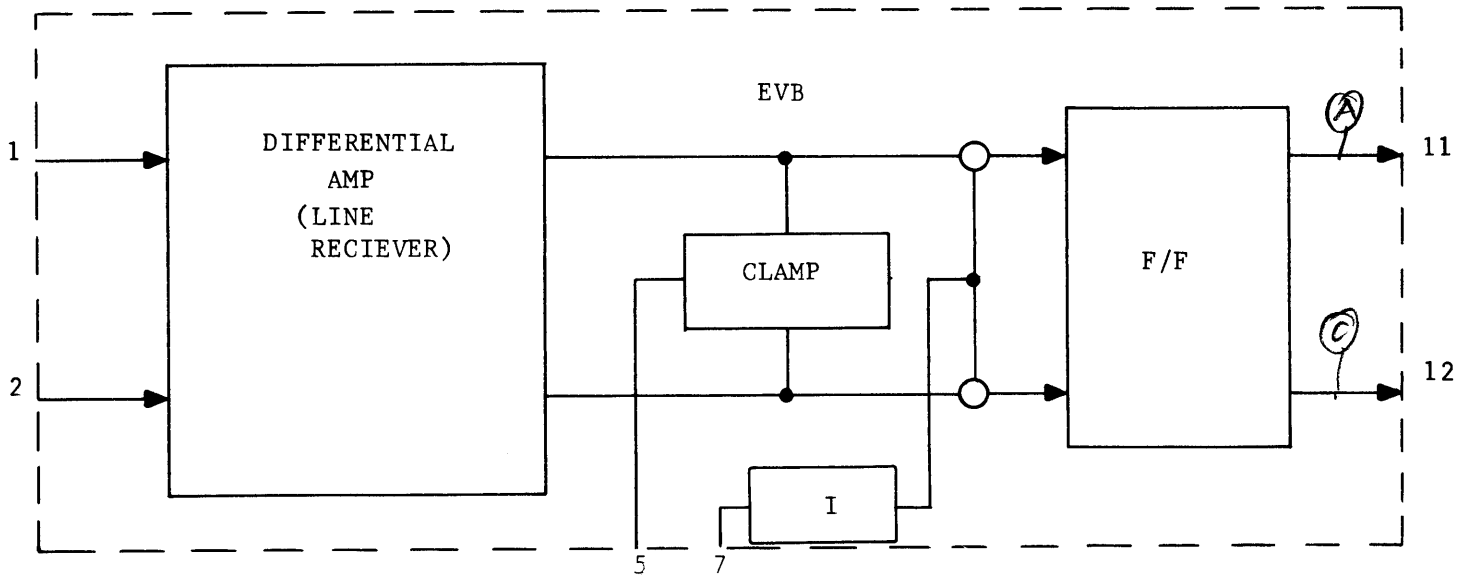
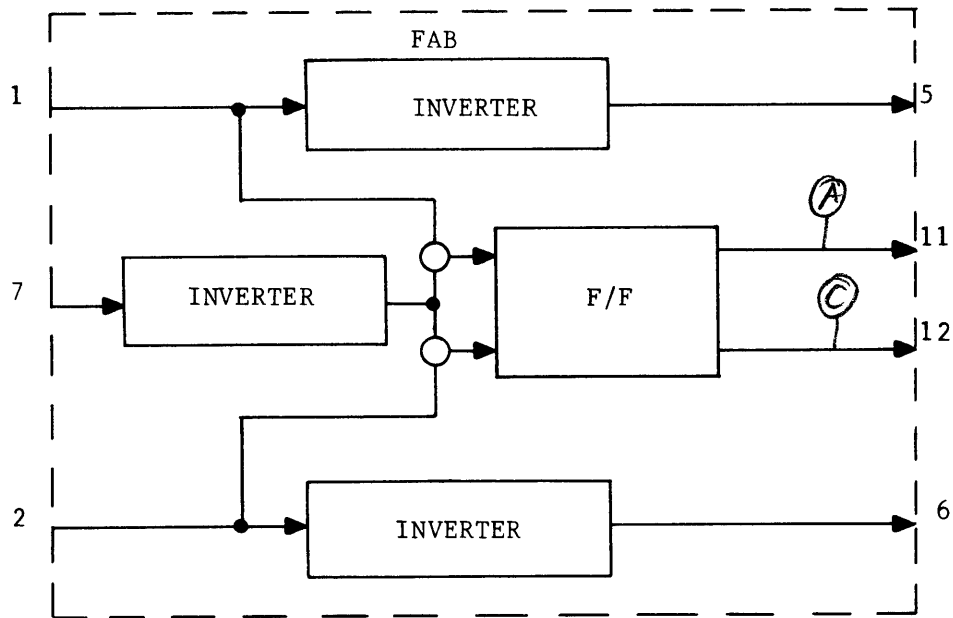
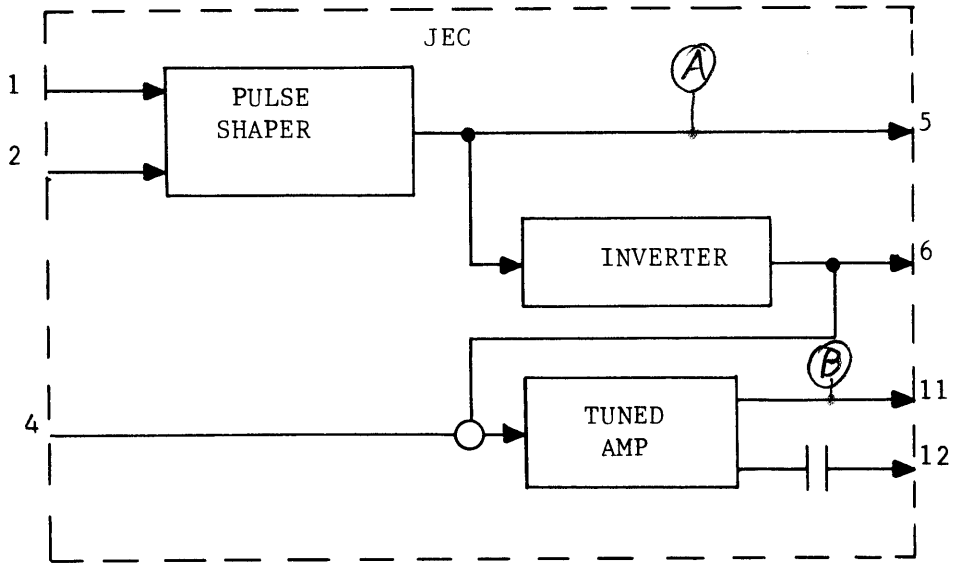


40. F53(.02v) F55(.02v)  
Seek  $\pm 22.5$  10ms/cm  
(Pressure)



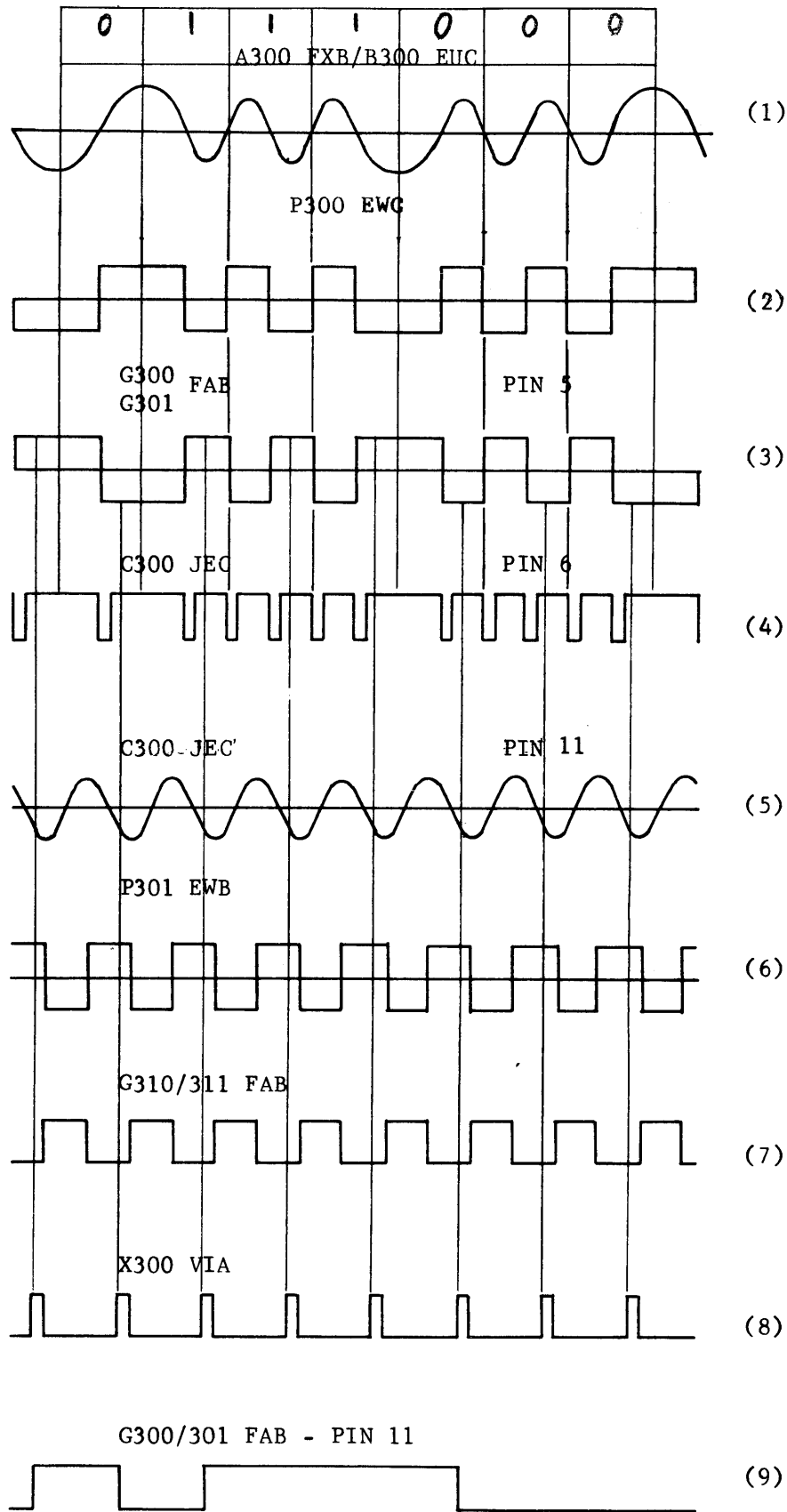


807/808 DATA CIRCUITS BLOCK DIAGRAM



SPECIAL CIRCUITS

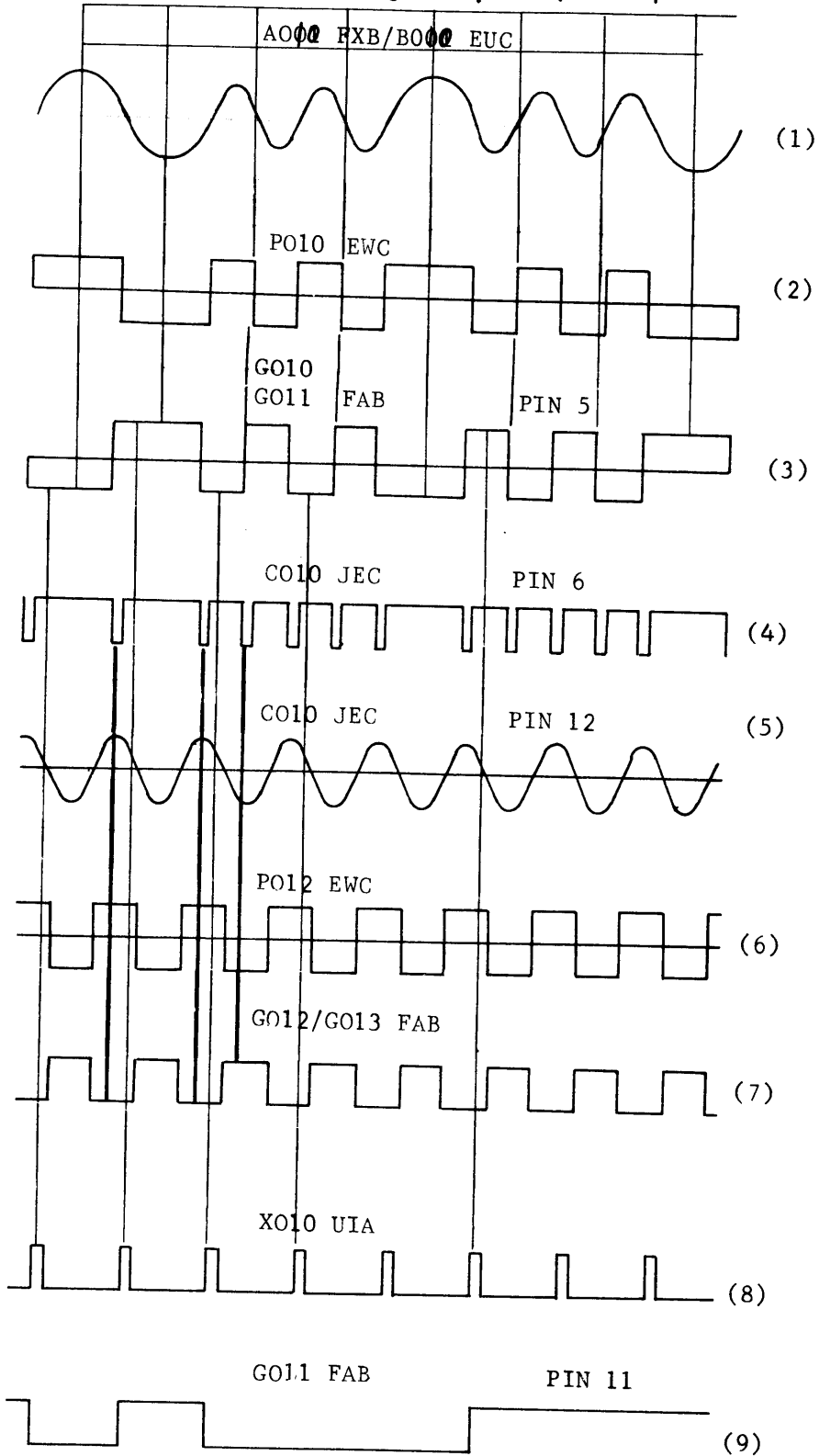
TRACK VERIFICATION WAVEFORMS



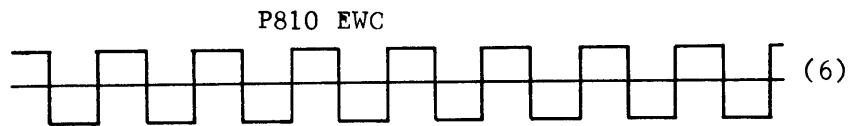
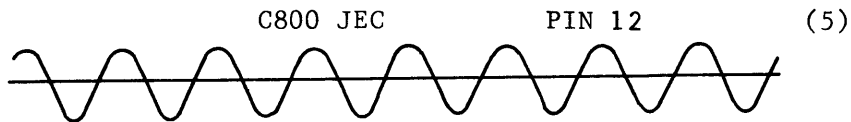
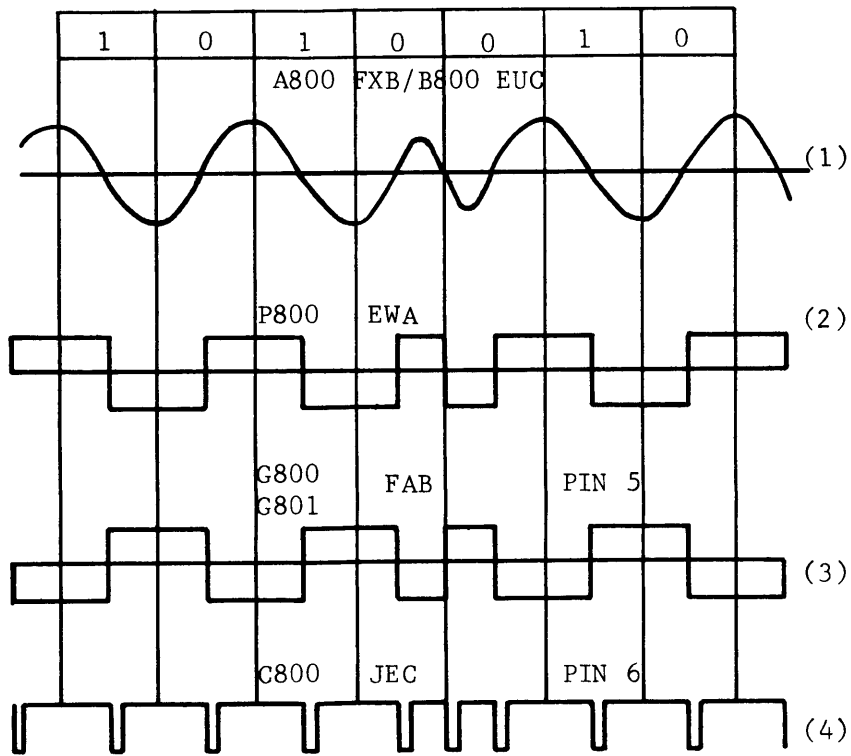
READ DATA WAVEFORMS

1 0 0 0 1 1 1

500 MV PP  
A11 +  
0  
(C) (12)-



WRITE CLOCK AND SECTOR



WRITE DATA WAVE FORMS

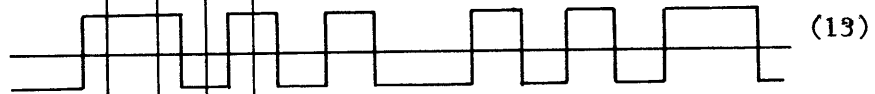
X800 UIA



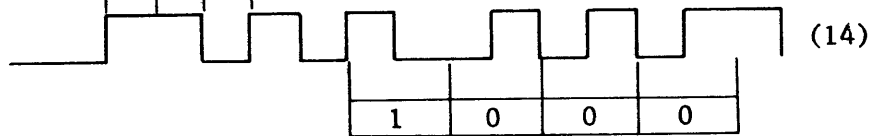
Z220 AIB



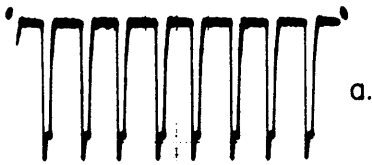
WRITE DATA FROM CONTROLLER



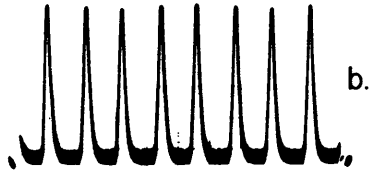
FOOO EVB



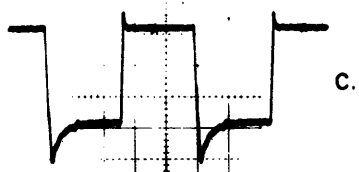
## WRITE DATA WAVEFORMS



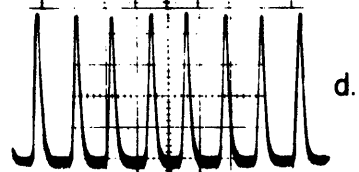
Waveform a: The output of the pulse shaper UIA, X800 (E22), showing the 200 ns Write Transfer pulses occurring every 600 ns.



Waveform b: The output of the Shift Driver AIB Z210, Z220 (E25B & C) showing the shaped Write Transfer pulses applied to pin 7 of the EVB data receiver flip-flops.



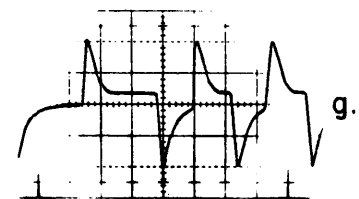
Waveform c: The input to the EVB data receivers. Oscilloscope setting, .5 usec/cm shows a 1.2 usec alternate "1" and "0" data pattern.



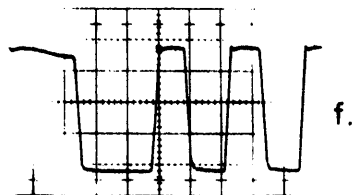
Waveform d: Write Transfer Pulse outputs of the AIB shift drivers applied to pin 7 of the data receiver flip-flops.



Waveform e: Data in the EVB flip-flops. Gating being done by Write Transfer pulses applied to pin 7.

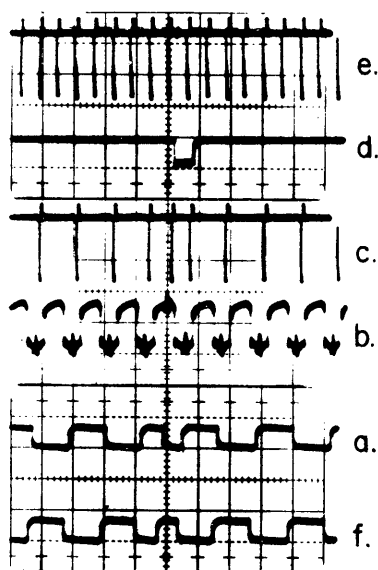


Waveform f: The output voltages of a Write Driver Amplifier AMH (W000-W110). Signals are shown at the end of the preamble and beginning of an all 1's data pattern.



Waveform g: The signals applied to the R/W head via the Resistor/Diode card AVD (H07-H22).

## TIMING WAVEFORMS



Waveform a: The output of EWC, P800 (A-38) showing the high frequency swing indicating a sector mark. This is sector mark #1. Waveforms b through e are generated in the logic chain from this signal.

Waveform f: The output of EWC P800 (A-38) showing the high frequency swing indicating sector mark #2. Note sector mark #1 consists of 2 "1" bits and sector mark #2 consists of 2 "0" bits.

Waveform c: The output of JED, C800 (A41) pin 5 showing the 150 ns pulse developed by each transition of the input signal. The half cell pulse is developed by the double frequency sector mark bit.

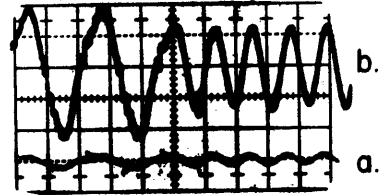
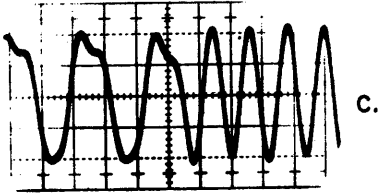
Waveform d: The output of FAB, G820/821 (A-46) pin 11 showing the sector mark developed by gating the inputs to the flip-flop with the pulses from pin 5 of the JED card. The flip-flop remains clear except for the 600 ns sector mark when it is set by the half cell output pulse of the JED, C800 and cleared again at full cell time.

Waveform b: The output of EWC, P810 (A44) showing the 600 ns square wave developed from the tuned amplifier of JED C800 (A41). This signal inverted by FAB, G810/811 (A45) pin 12 provides the Write Clock to the controller.

Waveform e: The output of JED A47 (A51) showing the 150 ns pulses formed from the 600 ns Write Clock. These pulses will generate the Write Transfer pulses via the delay chain A50, B26, B25C, E21 and E22.



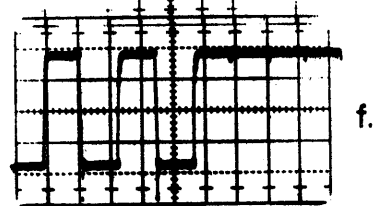
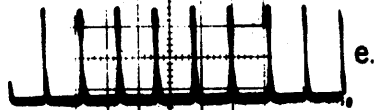
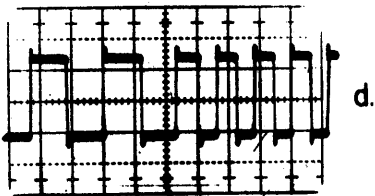
## READ DATA WAVEFORMS



**Waveform a:** Read data detected by the R/W head. Pattern is shown at end of preamble and beginning of data 1's pattern. Oscilloscope setting, .05 volts/cm.

**Waveform b:** Same data as waveform a at output of FXB Preamplifier (A000-A110) oscilloscope setting .05 v/cm.

**Waveform c:** Same data as a and b at output of EUC differential amplifiers (B000-B110). Oscilloscope setting 1 v/cm.

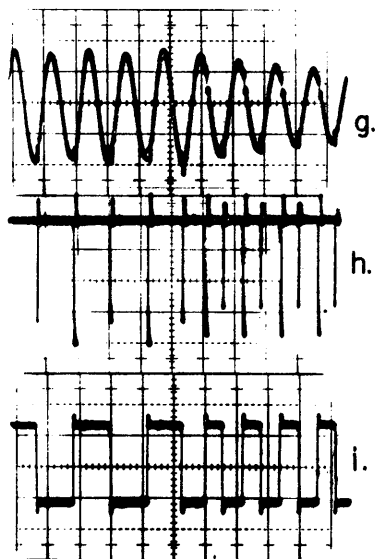


**Waveform d:** Output of Crossover Detector P000-P110 (C30-C48 C50-C58).

**Waveform e:** Output of UIA Pulse Shapers, X010, X040, X070, X100 (D33, D41, D49, D57). Read strobe pulses applied to pin 7 of the FAB data storage flip-flops G000=G110 (D30-D58).

**Waveform f:** NRZ data output of the above listed data storage flip-flops.

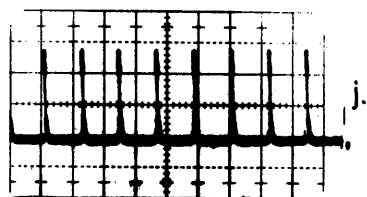
## READ DATA WAVEFORMS (Cont)



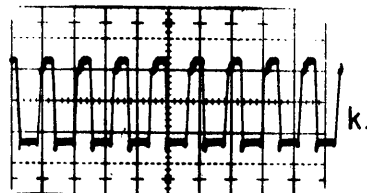
Waveform i: Same as d. This signal inverted through the FAB Data flip-flops is the input to the JED cards C010, C040, C070, C100. (D28, D36, D44, D52). This is the initial stage in developing the Read Clock and Read Strobe pulses.

Waveform g: Sinusoidal output of JED, C010 etc. pin 12. Output is adjusted for a 1.2 usec transition of the sine wave.

Waveform h: Pin 6 output of JED cards C010 etc. showing the 150 ns pulses developed by each excursion of the input signal. The full cell pulses trigger the tuned amplifier of the card. Half cell pulses are inhibited from triggering the amplifier by the "0" applied to pin 4 at this time.



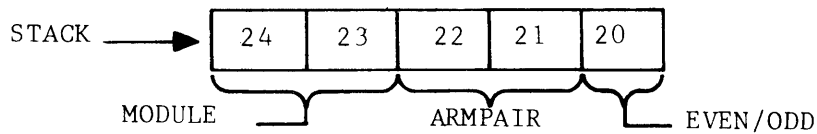
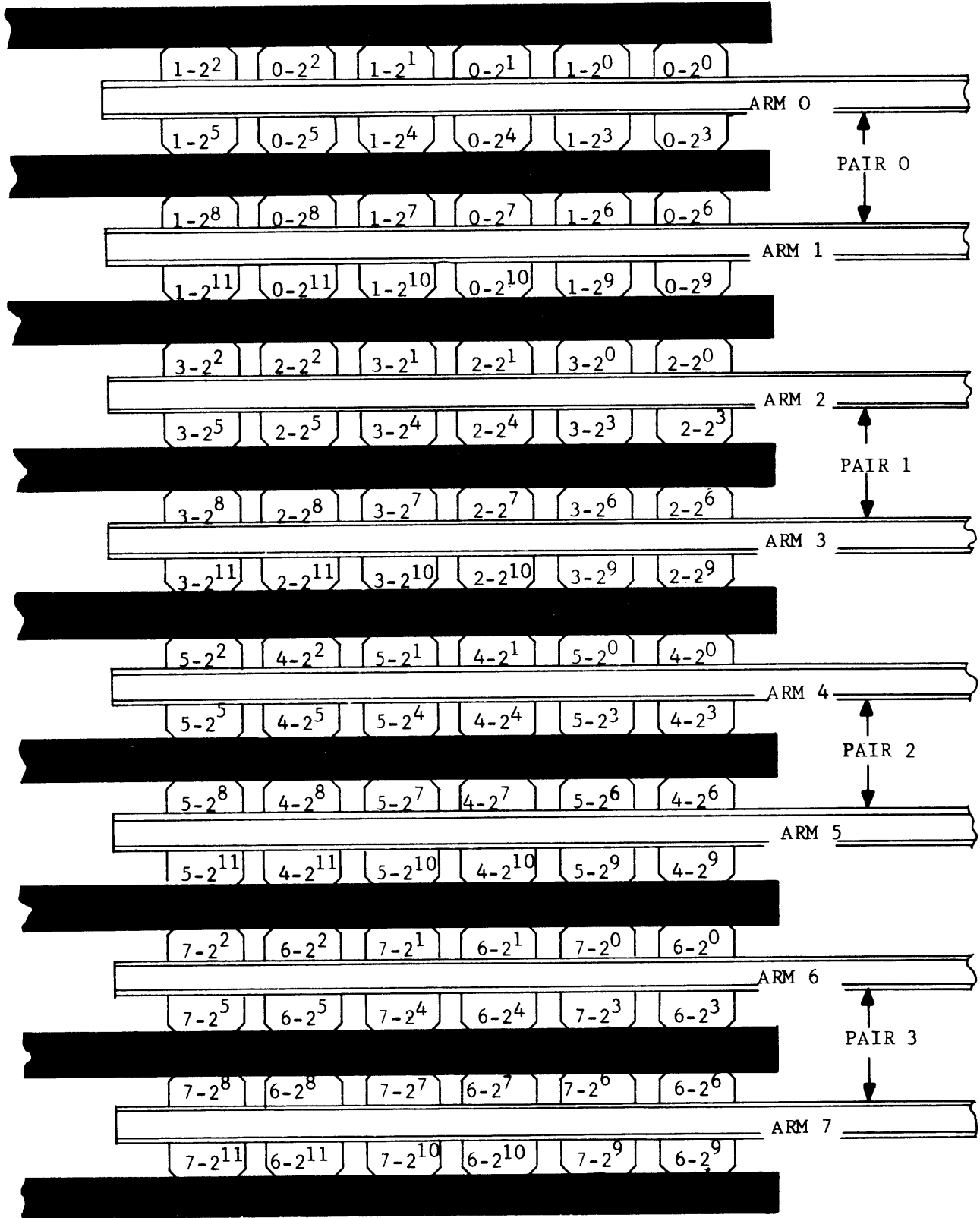
Waveform k: Output of I120 (F28A) showing the 600 ns symmetrical square wave Read Clock signal transmitted to the controller. This signal is developed from that shown in waveform g by the Crossover Detector P012, P042, P072, P102 and FAB Gated flip-flops G012, G042, G072, G102.



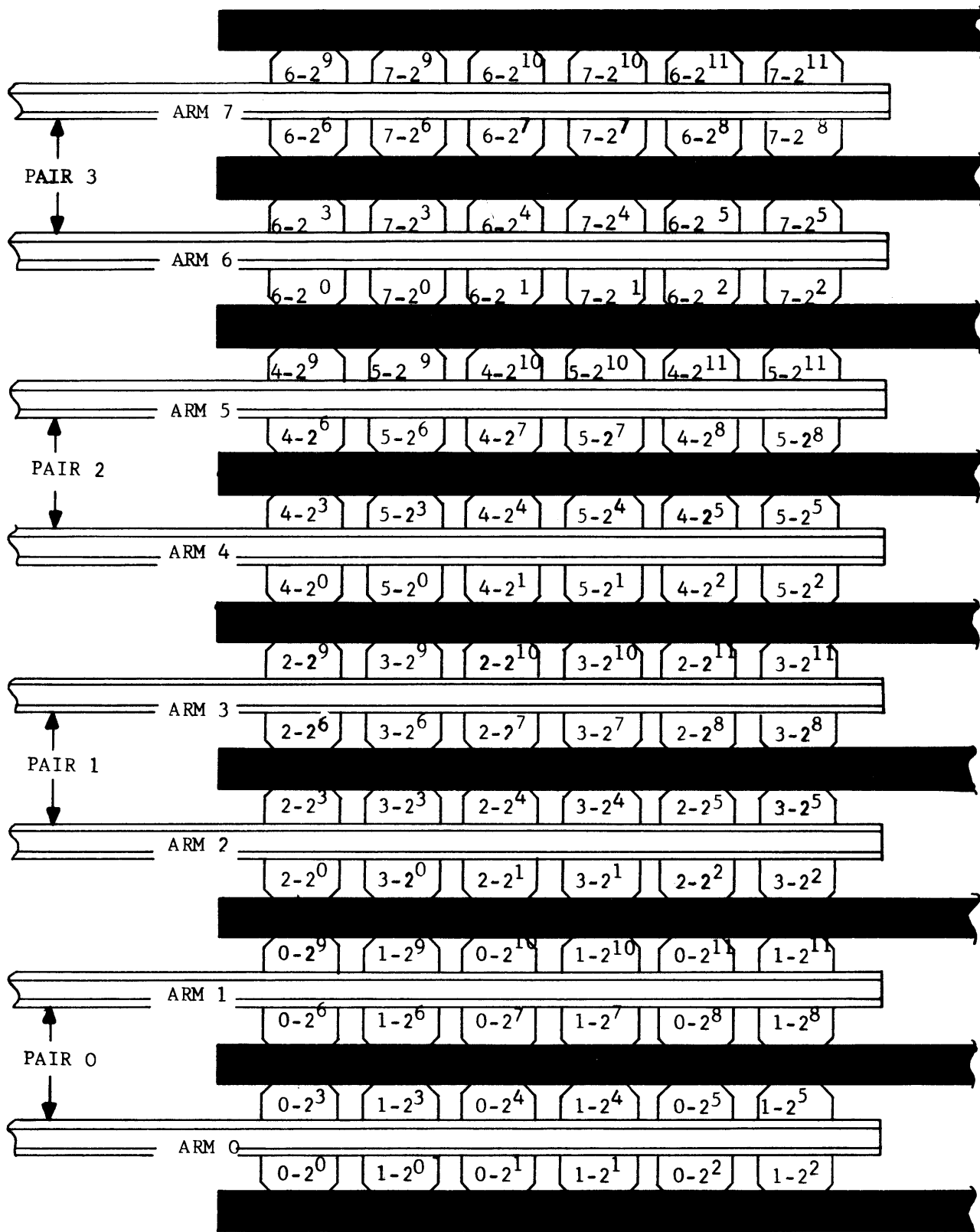
Waveform j: The 80 ns output pulses of Pulse Shapers UIA X010, X040, X070, X100. Developed from each zero going excursion of the 600 ns square wave. Used to gate data into the flip-flops of the FAB Data Storage flip-flops.



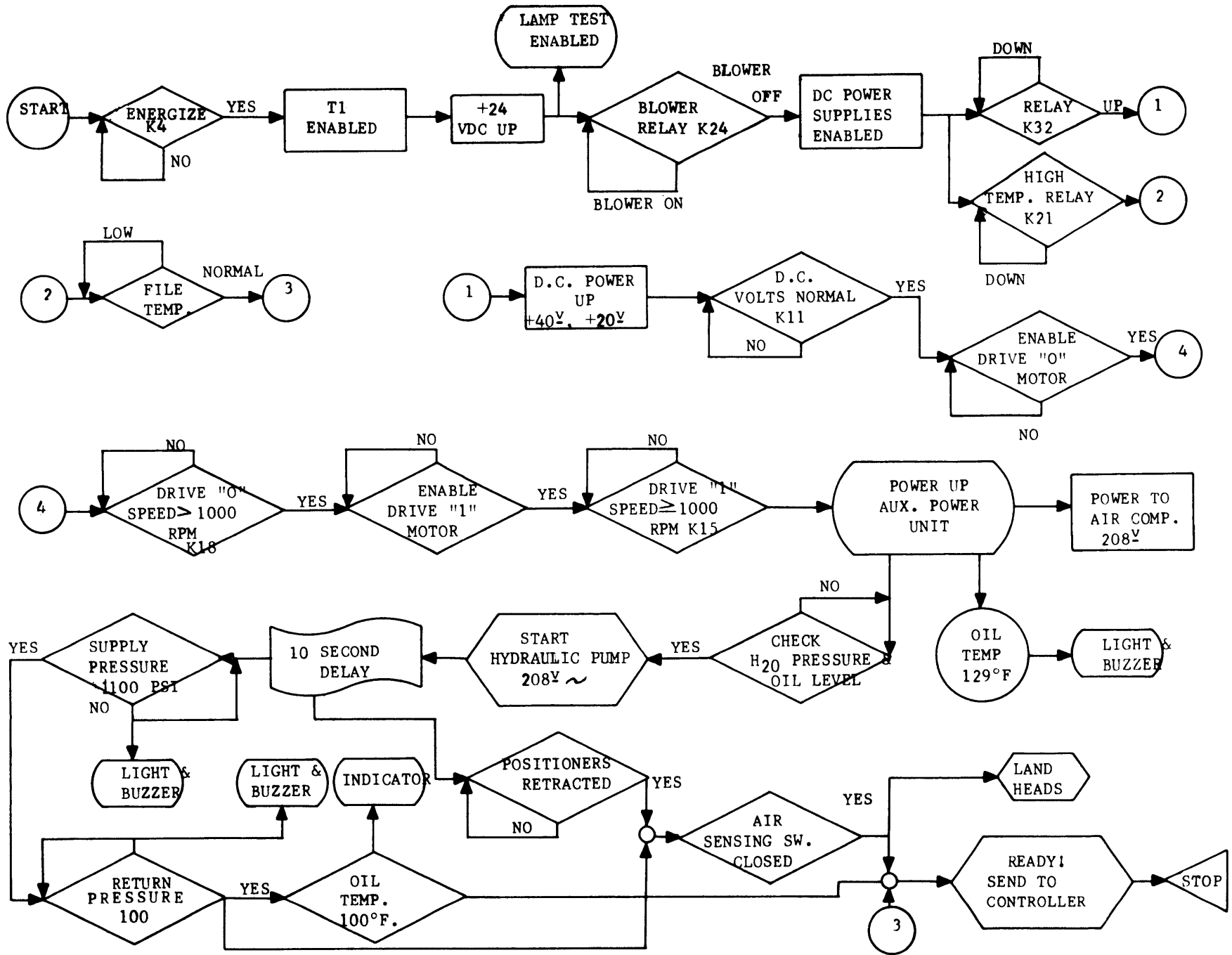
STACK 0 HEAD MODULE HEAD GROUP AND BIT ASSIGNMENTS



STACK 1 HEAD MODULE HEAD GROUP AND BIT ASSIGNMENTS



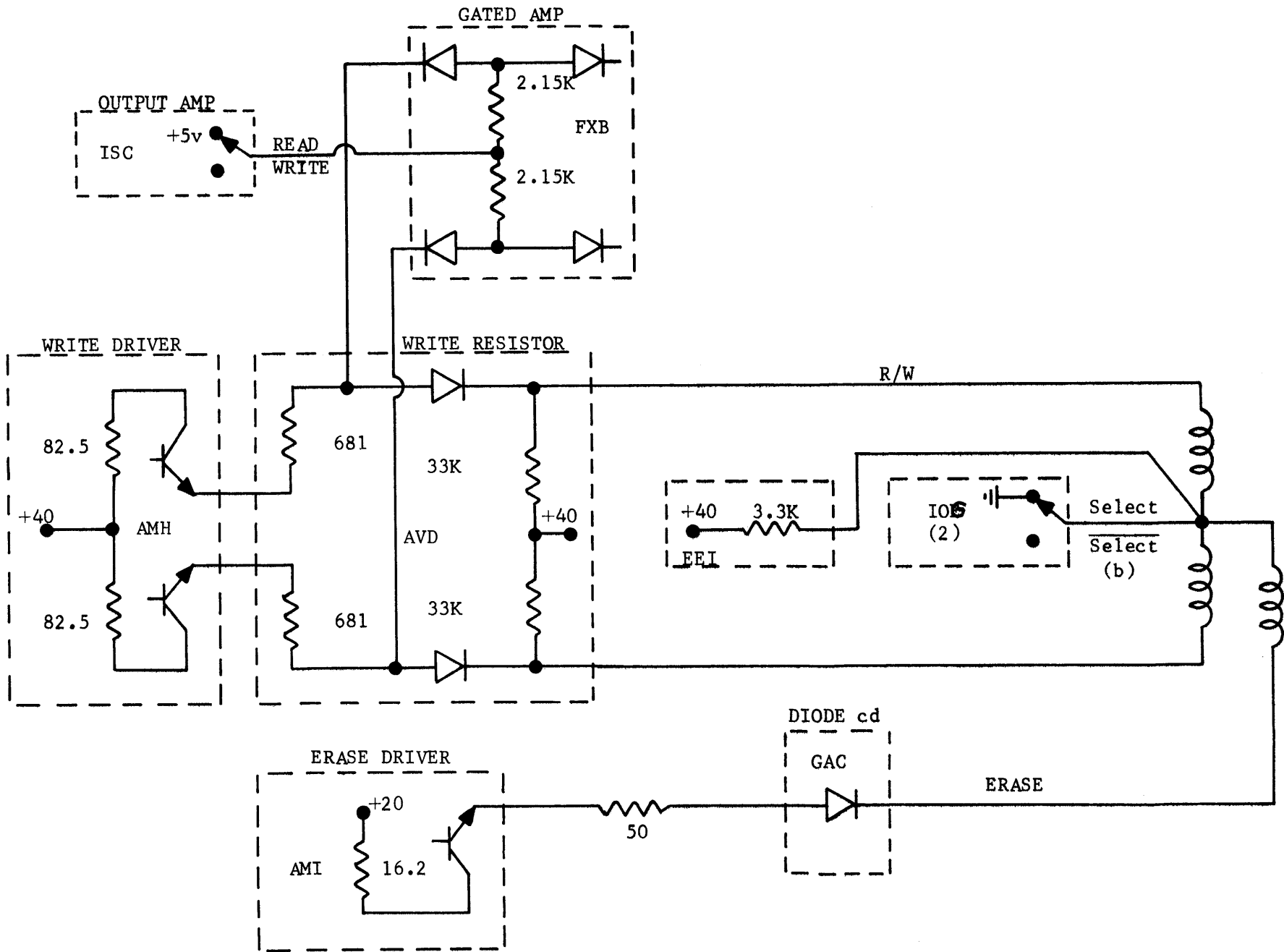
STACK 0	1
MOD 0	MOD 1
MOD 1	MOD 0



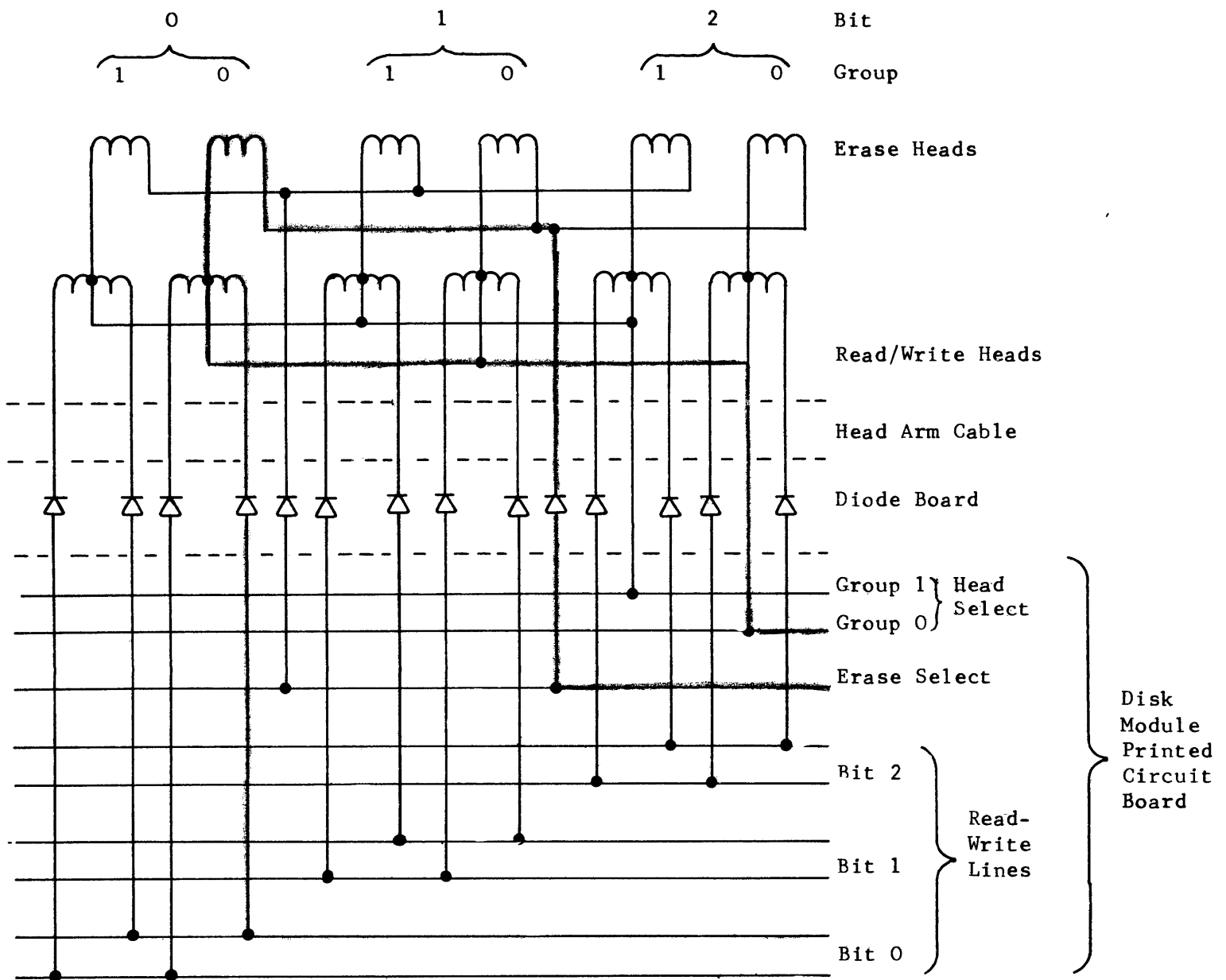


POSITION					
OCT	XLAT	OCT	MAJOR	MINOR	CONFIGURATION
0	0X	X0	0	Minus	A
1	0X	X1	0	N	
2	0X	X2	0	Plus	
3	0X	X3	1	Minus	
4	1X	X0	1	N	B
5	1X	X1	1	Plus	
6	1X	X2	2	Minus	
7	1X	X3	2	N	
10	2X	X0	2	Plus	C
11	2X	X1	3	Minus	
12	2X	X2	3	N	
13	2X	X3	3	Plus	
14	3X	X0	4	Minus	A
15	3X	X1	4	N	
16	3X	X2	4	Plus	
17	3X	X3	5	Minus	
20	4X	X0	5	N	B
21	4X	X1	5	Plus	
22	4X	X2	6	Minus	
23	4X	X3	6	N	
24	5X	X0	6	Plus	C
25	5X	X1	7	Minus	
26	5X	X2	7	N	
27	5X	X3	7	Plus	
30	6X	X0	8	Minus	A
31	6X	X1	8	N	
32	6X	X2	8	Plus	
33	6X	X3	9	Minus	
34	7X	X0	9	N	B
35	7X	X1	9	Plus	
36	7X	X2	10	Minus	
37	7X	X3	10	N	

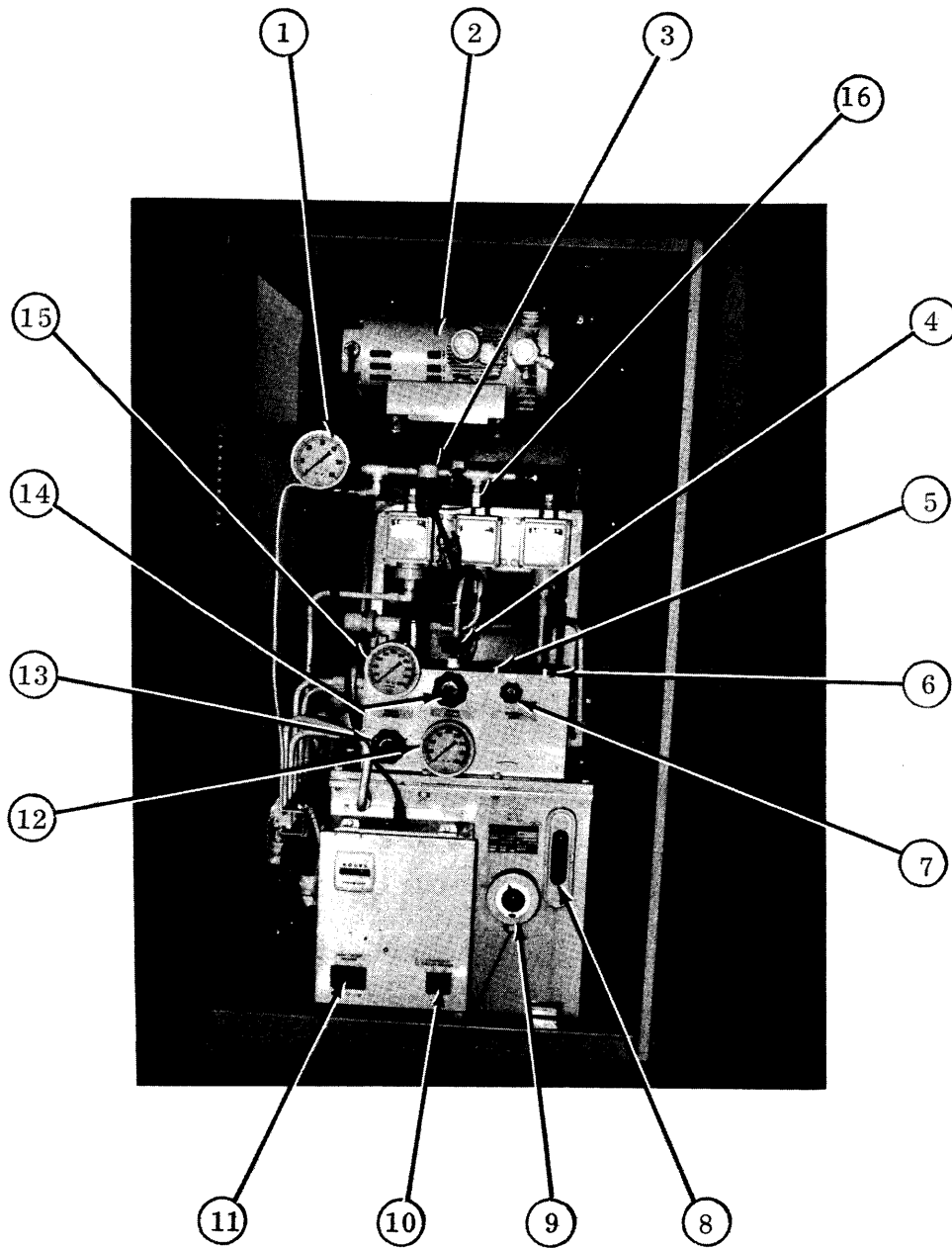




SIMPLIFIED R/W ERASE CIRCUIT



Wiring of the top head-pad assembly of head arm assembly 0 (typical)



HYDRAULIC UNIT  
ILLUSTRATION 1

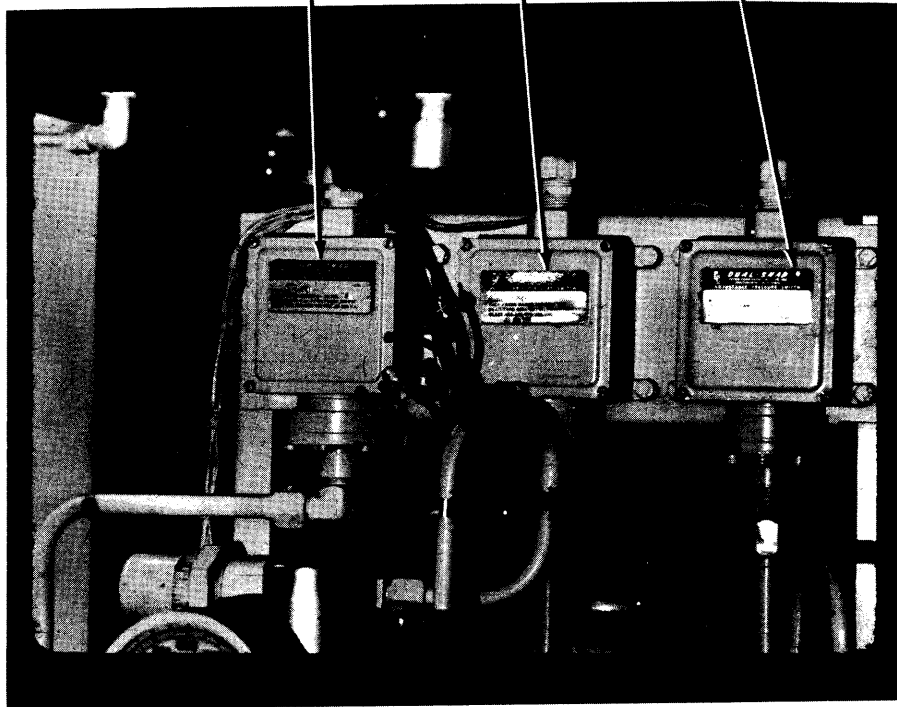
FOR ILLUSTRATION # 1

1. AIR PRESSURE GAUGE
2. AIR COMPRESSOR
3. CONDENSATION DISCHARGE VALVE
4. MANUAL BY PASS VALVE
5. SUPPLY OIL FILTER
6. RETURN OIL FILTER
7. OIL SAMPLE VALVE
8. OIL TEMP AND LEVEL INDICATOR
9. OIL TEMP THERMOSTAT
10. AIR COMPRESSOR CIRCUIT BREAKER
11. MAIN CIRCUIT BREAKER
12. RETURN OIL PRESSURE GAUGE
13. SUPPLY OIL PRESSURE GAUGE SNUBBER
14. RETURN OIL PRESSURE GAUGE SNUBBER
15. SUPPLY OIL PRESSURE GAUGE
16. AIR PRESSURE RELIEF VALVE

RETURN OIL PRESSURE SENSOR

SUPPLY OIL PRESSURE SENSOR

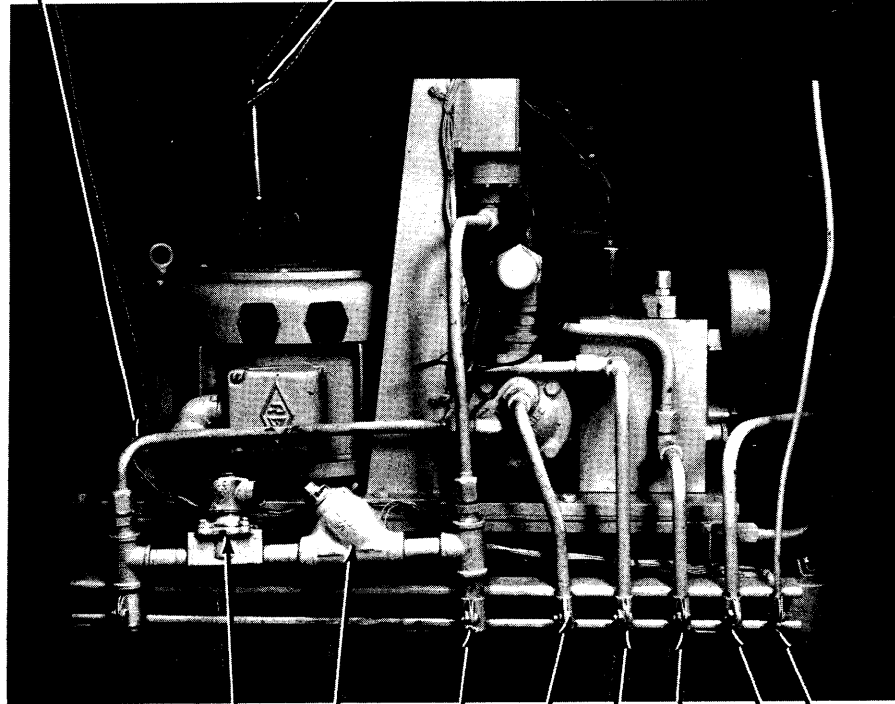
WATER PRESSURE SENSOR



HYDRAULIC UNIT  
ILLUSTRATION 2

OIL RESERVOIR VENT FILTER

OIL LEVEL SWITCH



WATER FLOW SOLENOID

WATER FILTER

WATER SUPPLY LINE

WATER RETURN LINE

OIL RETURN LINE

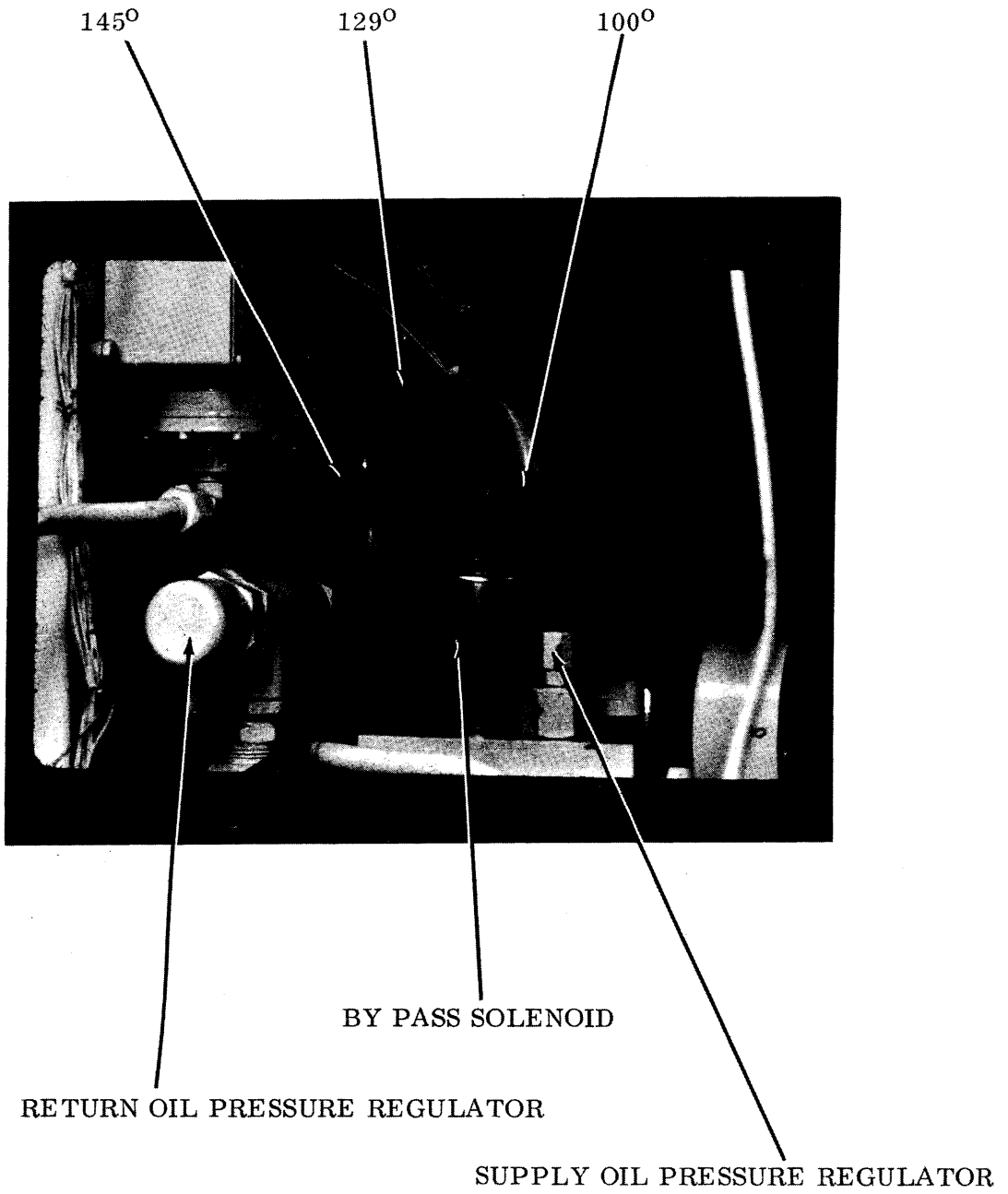
OIL SUPPLY LINE

OIL DRAIN RETURN LINE

AIR PRESSURE LINE

HYDRAULIC UNIT  
ILLUSTRATION 3

OIL TEMP SENSORS



HYDRAULIC UNIT  
ILLUSTRATION 4

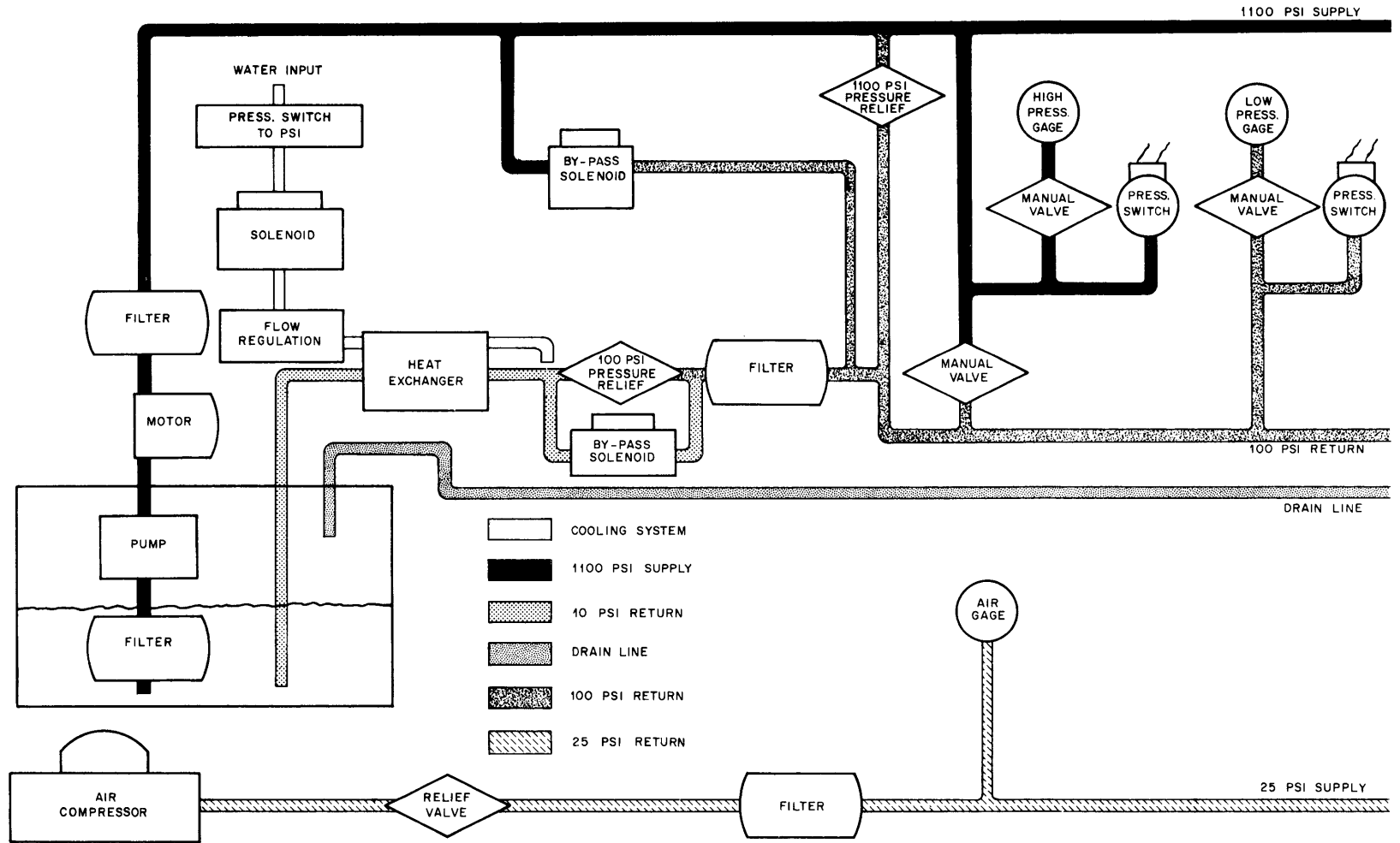


FIGURE 3-21. HYDRAULIC CABINET ASSEMBLY - FLOW DIAGRAM



## PARITY GENERATION

The parity word developed during data transfers and eventually written on the disk is a modified form of cyclic coding. Each new input is checked for equivalence with the current contents and the result left shifted. When the write operation terminates, the resultant word is sent to the write reg. with odd bits complimented. Figure 11 shows an example of parity word generation for a 2 word transfer.

	ON DISK	000 000 000 000	Original Contents
		100 001 000 010	1st Word
1st Word	4102	<u>011 110 111 101</u>	Equivalence
2nd Word	6670	111 101 111 010	Left Shift 1
Guard	0000	<u>110 110 111 000</u>	2nd Word
Parity	0642	110 100 111 101	Equivalence
		101 001 111 011	Left Shift 1
		<u>000 000 000 000</u>	Guard
		010 110 000 100	Equivalence
		101 100 001 000	Left Shift 1
		000 110 100 010	To Disk

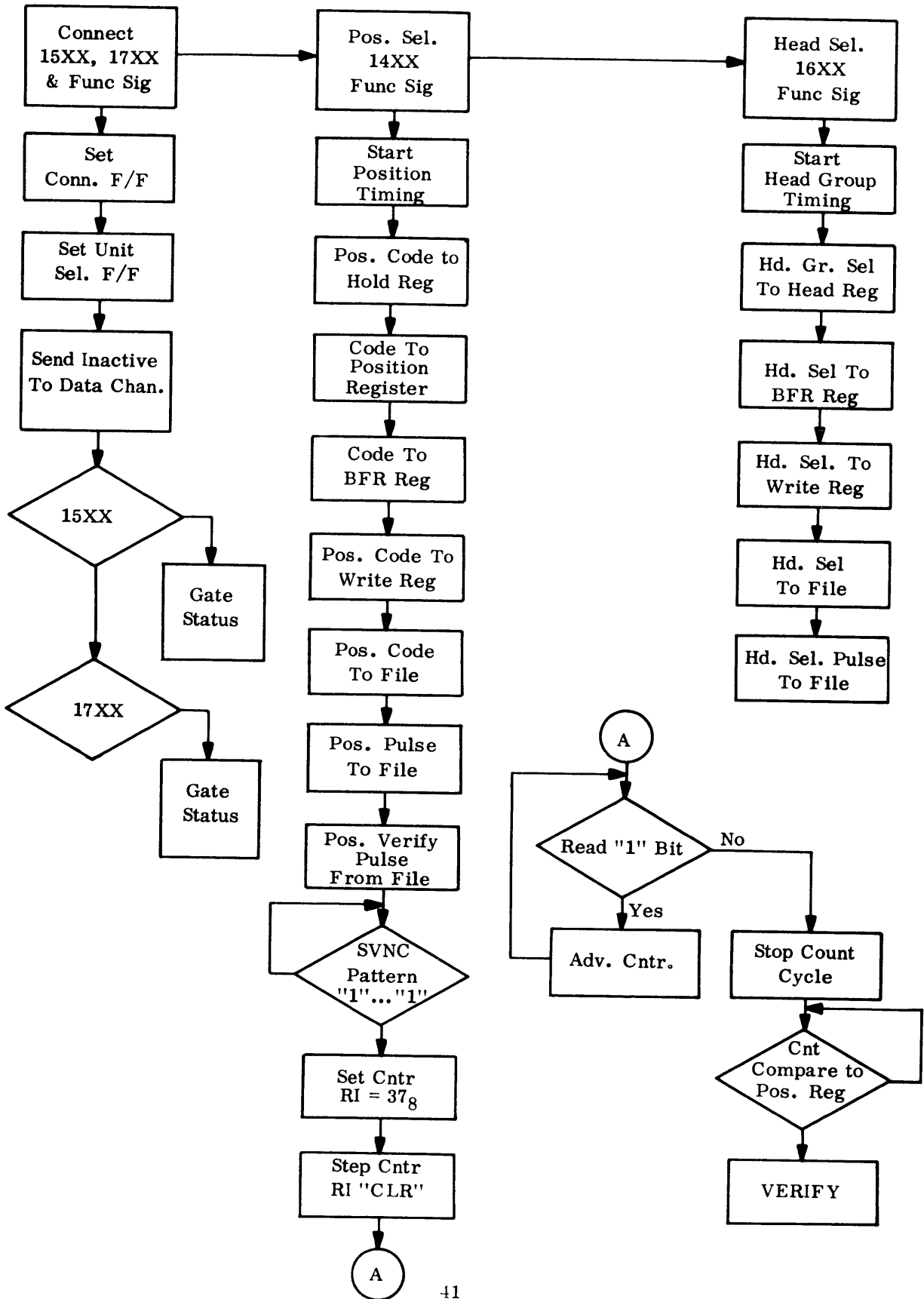
## WRITE PARITY GENERATION

During the read operation the parity circuits operate in the same manner. The data read from the disk including the parity word develop a check word which should have a 5252 pattern. If the pattern does not exist, a parity error status is set up. Figure 12 shows the same data as was written in figure 11 being read. Note that a valid parity check can only be made if the exact number of words written are read.

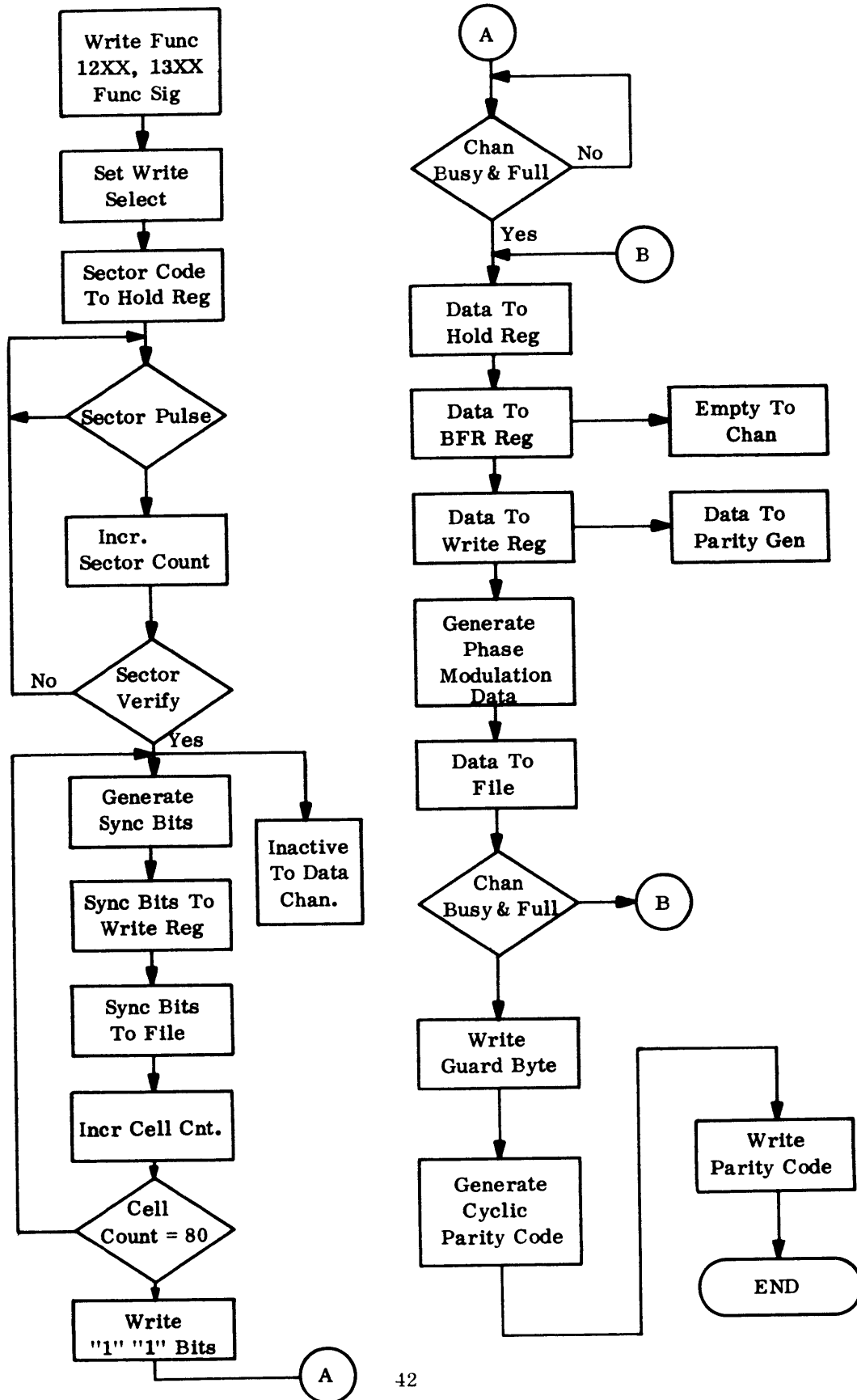
	FROM DISK	000 000 000 000	Original Contents
		100 001 000 010	1st Word
1st Word	4102	<u>011 110 111 101</u>	Equivalence
2nd Word	6670	111 101 111 010	Left Shift 1
Guard	0000	<u>110 110 111 000</u>	2nd Word
Parity	0642	110 100 111 101	Equivalence
		101 001 111 011	Left Shift 1
		<u>000 000 000 000</u>	Guard
		010 110 000 100	Equivalence
		101 100 001 000	Left Shift 1
		000 110 100 010	Parity
		<u>010 101 010 101</u>	Equivalence
		101 010 101 010	Left Shift 1

## READ PARITY GENERATION

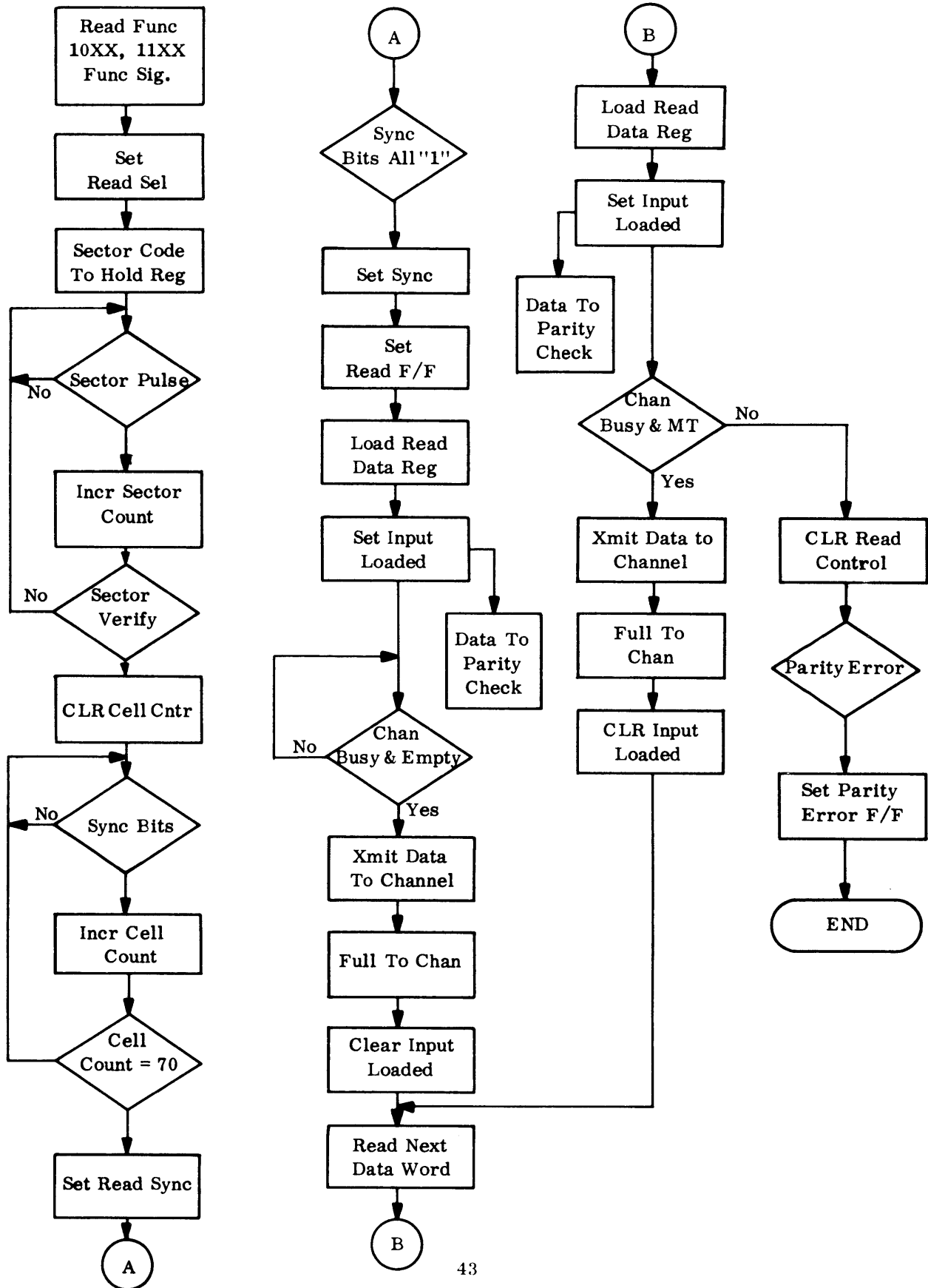
# 6639 FUNCTION



# 6639 WRITE



# 6639 READ



PROGRAMMING

CODES

TABLE 2. 6639 DISK CODES

FUNCTION CODES	
Connect and Status	15XX or 17XX
Position Select	14XX
Head Group Select	16XX
Write	12XX or 13XX
Read	10XX or 11XX
Disconnect	154X or 174X
STATUS WORDS	
First Status Word	XXXX
Second Status Word	XXXX

Function Codes

Connect and Status (15XX or 17XX)

This code interconnects the Data Channel, controller, and disk file. It also causes the controller to return one of two status words to the Data Channel.

The code bit assignment is shown in Figure 5.

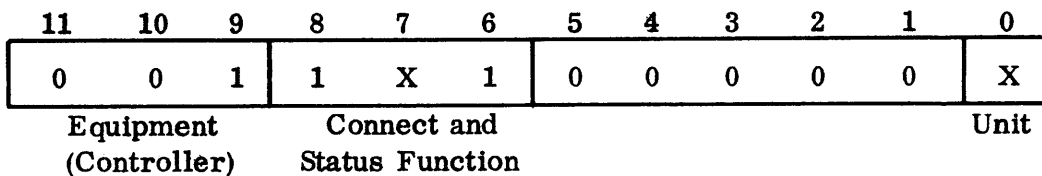


Figure 5. Connect and Status Function Code

Bits 9-11: These bits designate the equipment code number (controller) to which two Data Channels are wired. If desired, the equipment code number can be altered by a small wiring change.

Bits 6-8: This bit combination attempts to connect the controller to the Data Channel and it designates one of two formats of a status word to be returned by the controller. If bit 7 (17XX) is a "1", the controller responds with the first status word. If bit 7 (15XX) is a "0", the controller responds with the second status word. Either bit combination attempts to connect the controller to the Data Channel. Whether or not a connect is made, the controller responds with the status word designated by bit 7. If a connect is not made, any functions other than status hang up the channel.

Bits 1-5: These bits are not used.

Bit 0: (Not applicable if Standard Option 10037 is used.) This bit designates one of two disk file units to be selected. All further operations are performed on the selected unit.

Position Select (14XX)

This code causes the access mechanism to seek one of 32 positions in the disk file (refer to Figure 6).

11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	R	X	X	X	X	X
Equipment (Controller)			Position Select Function			Retract	Position Address				

Figure 6. Position Select Function Code

Bits 9-11: These bits designate the controller to which the Data Channels are wired.

Bits 6-8: These bits designate the Position Select function.

Bit 5: When this bit is a "1", it causes the positioner to withdraw the read/write heads from the data zone to a non-data zone. This withdraw position is provided as a standby location in which the read/write heads may reside with a low risk of data loss in the event of hardware failure.

Bits 0-4: These bits designate one of 32 positions in the disk file which are available to the access mechanism.

### Head Group Select (16XX)

This code causes the selection of one of 32 head groups in the disk file (refer to Figure 7).

11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	X	X	X	X	X

Equipment                      Head Group      Not                      Head Group  
(Controller)      Select Function      Used

Figure 7. Head Group Select Function Code

Bits 9-11: These bits designate the controller to which the Data Channel is wired.

Bits 6-8: These bits designate the Head Group Select function.

Bit 5: This bit is not used.

Bits 0-4: These bits select one of 32 head groups in the disk file. When bit 4 is a "0", a head group in stack 0 (head groups 0 through 15) is being selected, and when bit 4 is a "1", a head group in stack 1 (head groups 16 through 31) is being selected.

### Write (12XX or 13XX)

This code initiates a variable-length Write operation in the disk file (refer to Figure 8). The controller automatically generates and writes a check byte at the end of the write buffer. This byte is checked at the end of each Read operation to verify the accuracy of data transmission. Writing is end-around within a head group.

11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	X	X	X	X	X	X	X

Equipment                      Write                      Sector Address  
(Controller)      Function

Figure 8. Write Function Code

Bits 9-11: These bits designate the controller to which the Data Channel is wired.

Bits 7-8: These bits designate the Write function.

Bits 0-6: These bits designate the address of the sector mark at which the Write operation is to being.

Read (10XX or 11XX)

This code initiates a variable-length Read operation in the disk file (refer to Figure 9). At the end of the input buffer, the controller checks the next byte read from the disk file to verify the accuracy of data transmission. This byte was generated and written by the controller during the Write operation. Reading is end-around within a head group.

11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	X	X	X	X	X	X	X
Equipment (Controller)			Read Function		Sector Address						

Figure 9. Read Function Code

Bits 9-11: These bits designate the controller to which the Data Channel is wired.

Bits 7-8: These bits designate the Read function.

Bits 0-6: These bits designate the address of the sector mark at which the Read operation is to begin.

Disconnect (154X or 174X)

This code disconnects the Data Channel from the controller approximately 100 microseconds after the instruction is executed. The controller will not respond with a status word after the Disconnect function (refer to Figure 10).

11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	X	1	1	0	0	0	0	0
Equipment (Controller)			Disconnect								

Figure 10. Disconnect Code



Bits 9-11: These bits designate the controller to which the Data Channel is wired.

Bits 5-8: These bits designate the Disconnect function.

Bits 0-4: These bits are not used.

### Status Words

#### First Status Word (XXXX)

When bit 7 of the Connect and Status function code is a "1", the controller returns the status word shown in Figure 11.

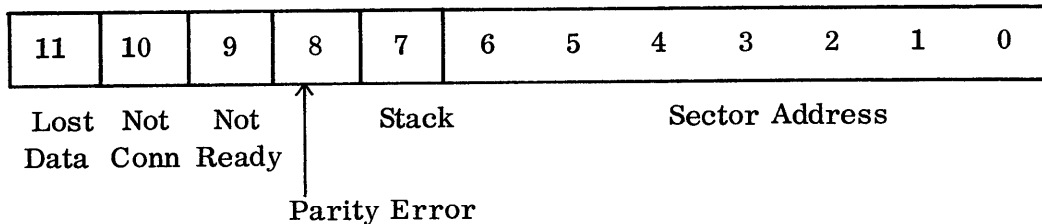


Figure 11. First Status Word

Bit 11: This bit is a "1" if a Lost Data condition occurs during a Read or Write operation. For example, the input or output buffer must follow a Read or Write function, respectively, within 90 microseconds or data is lost. The lost data bit remains present until a new Read or Write function is issued. If a lost data error occurs, the controller returns an Inactive signal to the Data Channel.

Bit 10: This bit is a "1" if the Data Channel has failed to connect to the controller because the controller has already been connected by the other Data Channel. No function other than status can be performed until a connect has been made.

Bit 9: This bit is a "1" when a Disk File Fault condition exists or when the disk file accessing mechanism is not yet verified as being "on track". No functions other than status can be performed when a Disk File Fault condition exists. All functions except a Read, Write, or Position Select can be performed when not on track. Any Read or Write function that is attempted when the disk file accessing mechanism is not on track is held up until on track is verified. A Position Select function is issued to the disk file only when an On-Point signal is present.

Bit 8: This bit is a "1" if a parity error was detected at the end of a Read operation and it remains present until a new Read or Write function is issued by program control.

Bit 7: This bit indicates to which stack the sector address (bits 0-6) refers. When this bit is a "0", stack 0 was the last stack used; when the bit is a "1", stack 1 was last used. This bit is always equal to bit 4 of the last Head Group Select function code.

Bits 0-6: These bits indicate the sector count plus one of the sector currently under the read/write heads. These bits are derived from the sector mark counters, and they reflect the sector address from the stack designated by bit 7.

Second Status Word (XXXX)

When bit 7 (15XX) of the Connect and Status function code is a "0", the controller returns the status word shown in Figure 12. This word indicates the last position addresses issued from the controller to each of the disk file units.

11	10	9	8	7	6	5	4	3	2	1	0
Retract		Position Address				Retract		Position Address			
		Unit 1						Unit 0			
		(See Note)									

NOTE

If Standard Option 10037 is used, bits 6 through 11 are "0's".

Figure 12. Second Status Word

PROGRAMMING CONSIDERATIONS

Sequencing Operations

After a connect has been made, functions can be issued in any order. Normally, functions are issued in the following sequence: Connect and Status, Position Select, Head Group Select, and Read or Write. Once a position and a head group have been selected, it is not necessary to reselect them for subsequent operations. For optimum use of the disk file system, two processors should be used.

At the end of a Read or Write operation, a status check should be performed to check for abnormal conditions such as Lost Data, Not Connected, Parity Error, or Not Ready. Status checks performed between sectors must be part of a very rapid sequence. If the postamble is of minimum size (28 bits), there will be only about 30 microseconds to perform the following:

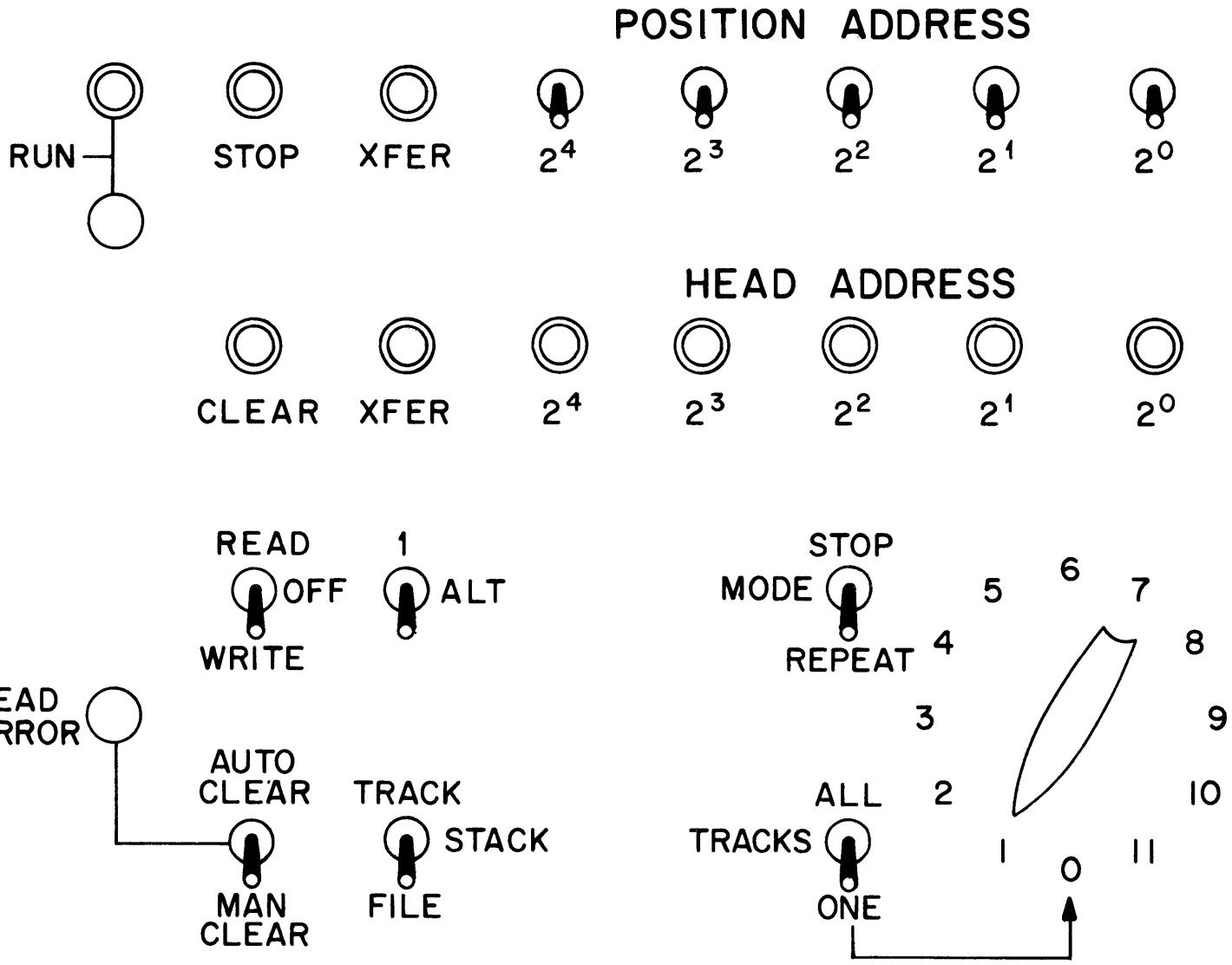
- 1) Check Data Channel activity to see if the Data Channel was deactivated by the controller.
- 2) Deactivate the Data Channel if at the end of the buffer and the Data Channel is still active.
- 3) Issue Connect and Status function word.
- 4) Activate the Data Channel.
- 5) Input the status word.
- 6) Check the status word.
- 7) Deactivate the Data Channel.
- 8) Issue a new function word.

### Positioning Times

There are 11 major positions spaced 0.370 inch apart. Each major position includes two minor positions spaced 0.020 inch to the right or left of each major position. This results in 33 possible positions of which 32 (positions 0 through 31) are available as data positions under program control. Refer to Figure 13 for position assignments. Position and access time are as follows:

<u>Position</u>	<u>Milliseconds (maximum)</u>
Adjacent major move	45
Average of several maximum positioning times between extreme major positions	110
Single minor move (0.020 inch)	20
Double minor move (0.040 inch)	25
Verification time	250 (microseconds maximum)
Latency time	52
Average of several worst-case access times (access time includes positioning, verification, and latency times)	162.25

# OPERATING PANEL



## OPERATION

### POSITION ADDRESS

The position address transfer will transfer the contents of the position address switches to the file. This will cause the heads to move to the requested position.

NOTE: Exerciser must be stopped. File may be ready or not ready.

### HEAD ADDRESS

The head address switches will set a head address counter. The head address transfer will transfer the contents of the head address counter to the file and select the requested head group.

NOTE: Exerciser must be stopped.

### READ/WRITE

Read: When run is depressed, data will be read from the file and checked. A data error will set read error.

Write: When run is depressed, data will be written on the disk.

### 1/ALT/0

The write data pattern or the read check pattern will be: All ones, alternate 1's and 0's, or all 0's.

### AUTO CLEAR/MAN CLEAR

Auto clear: Will clear read error at index time.

Man clear: Will hold read error clear.

### TRACK/STACK/FILE

Track: Will prevent head address increment.

Stack: Will allow all but the upper head address but to increment.

File: Will allow the head address to increment through all addresses.

### STOP/REPEAT

Stop: Will force stop if read error or at end of selected track, stack or file.

Repeat: Will allow continuous operation.

### ALL TRACKS/ONE TRACK

All tracks: Will read check all 12 tracks.

One track: Only the selected track will be check read. Errors on the remaining tracks will not be detected.

NOTE: Stop will be forced if file ready drops.