

CONTROL DATA[®] DISK STORAGE UNIT

**84X-ENHANCED
975X-ENHANCED**

LOGIC CARDS

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

PREFACE

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the disk storage unit (drive).

Logic card information is provided by four sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - Introduction to logic symbology and card construction.

Section 2 - Description of integrated circuits used in the drive. Includes pin assignments along with truth tables and/or typical waveforms.

Section 3 - Description of discrete components and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ) explains these functions and illustrates the actual discrete elements.

Section 4 - Schematics of logic cards. These schematics are arranged in alphabetical sequence of the last three characters of the card type. The first character of the card type is for internal control of card revisions.

CONTENTS

<p>1. INTRODUCTION</p> <p>General 1-1</p> <p>Back Panel 1-1</p> <p>Logic Cards 1-3</p> <p style="padding-left: 20px;">Physical Description 1-3</p> <p style="padding-left: 20px;">Pin Assignments 1-3</p> <p style="padding-left: 20px;">Test Points 1-5</p> <p>Logic Symbology 1-5</p> <p style="padding-left: 20px;">Input/Output State Indicators 1-5</p> <p style="padding-left: 20px;">Dynamic Indicator 1-6</p> <p style="padding-left: 20px;">Signal Line Indicators 1-6</p> <p style="padding-left: 40px;">Non-Standard Levels 1-6</p> <p style="padding-left: 40px;">Inhibit 1-7</p> <p style="padding-left: 40px;">Miscellaneous 1-7</p> <p>Function Symbols 1-7</p> <p>Input/Output Designators 1-10</p> <p>Common Control Block 1-11</p> <p>Wired Functions 1-12</p> <p>Integrated Circuits 1-12</p> <p>Operational Amplifiers 1-13</p> <p style="padding-left: 20px;">Introduction 1-13</p> <p style="padding-left: 20px;">Basic Circuit Elements 1-14</p> <p style="padding-left: 20px;">Input Stage 1-14</p> <p style="padding-left: 20px;">Second Stage 1-14</p> <p style="padding-left: 20px;">Base Circuit Functions 1-16</p> <p style="padding-left: 20px;">Schmitt Trigger Circuits 1-17</p> <p>Discrete Component Circuits 1-22</p> <p>2. INTEGRATED CIRCUIT PACKAGE CONFIGURATIONS</p> <p>Integrated Circuit Index 2-1/2-2</p> <p>Circuit Type</p> <p style="padding-left: 20px;">140 2-3</p> <p style="padding-left: 20px;">140S 2-3</p> <p style="padding-left: 20px;">141 2-4</p> <p style="padding-left: 20px;">143 2-5</p> <p style="padding-left: 20px;">143S 2-5</p> <p style="padding-left: 20px;">144 2-6</p> <p style="padding-left: 20px;">145 2-7</p> <p style="padding-left: 20px;">146 2-8</p> <p style="padding-left: 20px;">147 2-9</p> <p style="padding-left: 20px;">149H 2-10</p> <p style="padding-left: 20px;">158 2-11</p> <p style="padding-left: 20px;">159 2-13</p> <p style="padding-left: 20px;">161 2-15</p>	<p>Circuit Type</p>	<p>162</p> <p>164H</p> <p>164S</p> <p>166</p> <p>172H</p> <p>173H</p> <p>175H</p> <p>176</p> <p>182</p> <p>188</p> <p>189</p> <p>191</p> <p>193</p> <p>195</p> <p>200</p> <p>208S</p> <p>218</p> <p>321S</p> <p>502</p> <p>519</p> <p>521</p> <p>579</p> <p>3. DISCRETE COMPONENT CIRCUIT DESCRIPTIONS</p> <p>Effectivity Index 3-1/3-2</p> <p>FAE-Gated Amplifier 3-3</p> <p>FAF-Amplifier 3-4</p> <p>FAG-Controlled Voltage Source 3-6</p> <p>FAH-Voltage Switch 3-7</p> <p>FBH-Voltage Switch 3-8</p> <p>GJB-Gated Analog Clamp 3-9</p> <p>GJC-Multiple Gate Analog Clamp 3-11</p> <p>GJF-Low Pass Filter & Amplifier 3-12</p> <p>GJK-Low Pass Filter & Amplifier 3-14</p> <p>GKA-Level Translator 3-16</p> <p>GKB-Digital to Analog Converter 3-16</p> <p>GKC-Level Translator 3-18</p> <p>GKD-Digital to Analog Converter 3-19</p> <p>GKF-Digital to Analog Converter 3-21</p> <p>HAJ-Differential Low Pass Filter 3-23</p> <p>HAK-Amplifier 3-24</p> <p>HAL/HAM-Summing Amplifier 3-26</p> <p>HAN-Peak Holding Amplifier 3-28</p> <p>HAP-AGC Amplifier 3-30</p> <p>HAQ-Differentiator/Amplifier 3-32</p>	<p>2-16</p> <p>2-18</p> <p>2-18</p> <p>2-19</p> <p>2-20</p> <p>2-21</p> <p>2-22</p> <p>2-23</p> <p>2-24</p> <p>2-24.1/2-24.2</p> <p>2-25</p> <p>2-26</p> <p>2-27</p> <p>2-28</p> <p>2-29</p> <p>2-30</p> <p>2-30.1</p> <p>2-30.2</p> <p>2-31</p> <p>2-32</p> <p>2-33</p> <p>2-34</p>
--	----------------------------	---	--

HAR-Differential Amplifier	3-34	UC-Delay	3-106
HAS/HAT-Amplifier	3-36	UEB-Delay	3-107
HAU-Buffer Amplifier	3-37	VAF-Level Shifter	3-108
HAV-Averaging Amplifier	3-38	VHI-Relay Driver	3-110
HAW-Summing Rectifier	3-40	VHJ-Level Translator	3-111
HAX-Summing Rectifier	3-42	VHK-Integrating Level Translator	3-112
HBA-Rectifier	3-44	VHL-AND Gate	3-113
HBB-Rectifier	3-46	VHM-Fault Detector	3-114
HBD-Buffer Amplifier	3-48	VHP-Erase Current Driver	3-115
HBE-Rectifier	3-50	VHQ-Level Translator	3-117
HBI-Amplifier	3-52	VHR-Time Constant Switch	3-118
HBJ-Buffer Amplifier	3-53	VKK-Relay Driver	3-120
HCA-Differential Amplifier	3-54	VKM-AND Gate	3-121
HCB-Differential Amplifier	3-55	VKN-Two Input AND Gate	3-122
HCE-Buffer Amplifier	3-56	XAF-Pulse Former	3-123
HCF-Buffer Amplifier	3-57	XAG-Pulse Generator	3-125
HCK-Voltage Follower	3-58	XAH-Delay	3-127
HCL-Integrating Amplifier	3-59		
HCP-Low Pass Filter	3-60	4. CARD DIAGRAMS	
HCQ-Filter and Amplifier	3-62	Head Connector and Preamp	4-1
HCU-AGC Amplifier	3-64	DZPN-Head Connector and Preamp	4-2.3
HJD-Amplifier/Level Translator	3-66	Track Servo Preamp	4-4
HJE-Level Translator	3-67	AAFV-Channel I/O and Cable Interlock	4-6
ICB-Lamp Driver	3-68	AAHV-Head (Odd-Even) Coding	4-8
ICC-Lamp Driver	3-69	1AJV-9 Bit Multiplexer	4-9
JAG-Write Driver	3-70	1ALV-Select, Reserve, Start-Up	4-10
JAK-AGC Amplifier	3-72	1APV-Mean Baseline Generator	4-11
JAM-Auto Null Circuit	3-73	2AQV-Buffer Amplifier	4-13
LCF-Transmitter	3-74	1ARV-Read Recovery PLO	4-14
MAF/MAH-Voltage Controlled Oscillator	3-76	1ASV-Data Separator	4-16
QDE-Speed Detector	3-79	1ATV-Head and Channel Selector	4-19
QEH-Voltage Checker	3-81	AAUV-Write, Erase, and Fault	4-21
QEJ-Voltage Checker	3-83	1AVV-Read Amplifier	4-25
QEK-Switch Receiver	3-85	2BBV-Index Detector	4-29
QEL-Symmetry Restored	3-87	ABPV-Write Oscillator	4-31
QEM-Voltage Follower	3-89	2BPV-Write Oscillator	4-35
QGD-Function Generator	3-90	ECGV-Track Servo Voltage Generator	4-39
RCB-Switch Receiver	3-92	JCGV-Servo Track Voltage Generator	4-41
SAA-Bipolar Current Buffer	3-94	KCGV-Servo Track Voltage Generator	4-42.1
SCC-Low Pass Filter & Amplifier	3-95	OCSV-D/A Converter	4-43
SCD-Voltage Comparator	3-97	3CTV-Velocity and Desired Velocity Function	4-45
SCE-Summing Ladder	3-98	CCUV-Coarse and Fine Summing Amp	4-47
SCG-Buffer Amplifier	3-99	1CVV-Power Amplifier/Preamplifier	4-49
SCL-Terminator/Divider	3-100	2CVV-Power Amplifier/Preamplifier	4-50
SCM-Divider Network	3-102	AEGV-Offset Control	4-51
SCN-Frequency Control Network	3-104	AEHV-Index Error	4-52
UBD/UBE/UBF/UBH-Delay	3-105	AEJV-806 PLO	4-53
		3EJV-806 PLO	4-55

3EQV-Parity Error Cover Latch	4-57	AHEV-Carriage Offset	4-156
AERV-Operator Interface	4-59	AHNV-Data Separator	4-158
3ERV-Operator Interface	4-60.3	AHPV-Phase Lock Oscillator	4-160
2ESV-Sector Counter/Register	4-62	1HQV-Write Compensation	4-162
2ETV-Function Decode 2 and Channel Select	4-65	3JCV-Power Interrupt	4-164
2EUV-Function Decode 1	4-67	3JLV-Device Clock & Fault Gating	4-166
2EVV-Multiplexer	4-69	3JMV-Diagnostic and Offset	4-169
1FCV-806 kHz Oscillator	4-71	3JNV-Index/Sector	4-172
2FEV-Motor Enable and On Line Clear	4-73	3JPV-Dialog	4-175
AFJV-Data Latch	4-74	3JQV-Miscellaneous	4-179
1FLV-AGC Amplifier	4-76	3JRV-Serializer/Deserializer	4-182
2FLV-AGC Amplifier	4-79	3JSV-Receiver/Transmitter	4-185
2FMV-Level Detector	4-82	2JYV-Absolute Addressing	4-190
2FNV-Differentiator and Amplifier	4-85	3PBV-Lamp/Relay Driver	4-194
DFPV-Write Driver and Fault Circuit	4-87	AQZV-Voltage Fault Detect & Address Control	4-196
FFPV-Write Driver and Fault Circuit	4-90	BQZV-Voltage Fault Detect & Address Control	4-198
CFRV-Fine Servo Decoder	4-92.1	1RCV-Receiver	4-200
2FRV-Fine Servo Decoder	4-93	3RLV-Receiver	4-201
3FRV-Fine Servo Decoder	4-97	ARWV-Receivers	4-202
BFSV-Head Alignment	4-100.1	BSAV-Switch Receiver	4-204
CFSV-Head Alignment	4-100.5	1TCV-Transmitter	4-206
EFSV-Head Alignment	4-100.9	2TLV-Transmitter	4-207
3FTV-Data Clock-Transmitter & Receiver	4-101	3TWV-I/O Transmitters	4-208
AFUV-Index Detector and Sector Generator	4-103	1UCV-Speed Detector	4-210
CFUV-Index and Sector Generator	4-106	OWAV/1WAV-Ten Bit Counter	4-212
2FVV-Fine, EOT Enable & Offset Control	4-109	1WBV-Four Bit Input Steering	4-213
1FWV-Access Control	4-112	0WCV-9 Bit Comparator	4-214
2FZV-R/W/E Enable and Fault Detect	4-114	0WDV-Fault Register	4-215
3GJV-CE Alignment Delay	4-116	GWEV-R/W/E Enable & Fault Detection	4-216
2GKV-Static Diagnostic	4-118	0WGV-Unit Reserve	4-217
2GLV-Motor Control and Speed Detection	4-122	1WGV-Unit Reserve	4-218
2GNV-State Latches	4-125	2WGV-Dual Channel Reserve	4-219
2GPV-Monitor Latch and Control	4-127	1WHV-Latency	4-220
2GSV-Intr/Reset and Parity Generator	4-130	1WJV-Sector/Index Separator	4-221
2GTV-Fault Detection	4-133	1WMV-Buffer	4-222
3GTV-Fault Detection	4-136	AWMV-Buffer	4-223
2GUV-Seek Control	4-139	2WWV-Multiplexer	4-224
2GVV-Tag Decode	4-141	0WYV-Counter Control	4-227
2GWV-Sector Counter and Register	4-144	BWZV-Difference Counter, Odd/Even and Slope	4-229
2GXV-Input Steering	4-147	DWZV-Difference Counter, Odd/Even and Slope	4-231
2GYV-Bus Parity and Lap Decode	4-150		
2GZV-Head Register Decode	4-152		
1HAV-Triple 4-Bit Multiplexer	4-155		

FIGURES

1-1 Wire Wrap Board Assembly	1-2	1-6 Integrated Circuit	1-13
1-2 Logic Card Detail	1-4	1-7 Simplified Op Amp Circuit	1-15
1-3 Inversion Conventions	1-6	1-8 Op Amp Circuit Functions	1-18
1-4 Common Control Block	1-11	1-9 Op Amp Used as a Schmitt Trigger	1-21
1-5 Wired Functions	1-12	1-10 Discrete Component Circuit	1-23

SECTION 1

INTRODUCTION

MAINTENANCE AIDS

GENERAL

Section 1 contains information on logic symbology, operational amplifiers, integrated circuit package configuration, discrete component descriptions and logic card diagrams.

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

Standard logic levels used are: "1" = +3 volts and "0" = 0 volts. All signals are named for their function when a "1". For non-standard logic levels or analog signal voltages, refer to applicable circuit description.

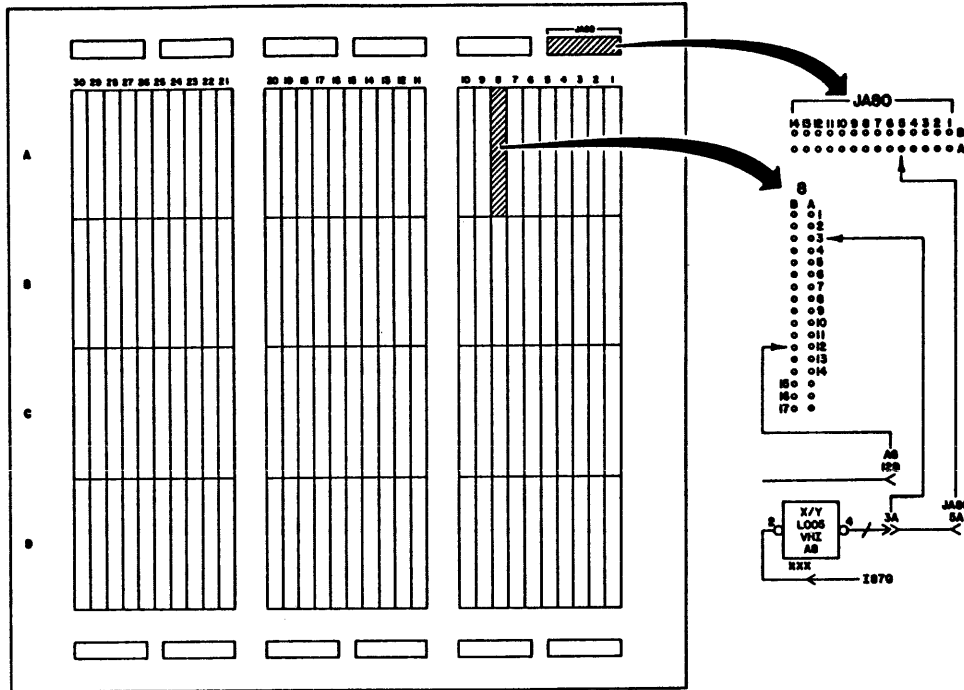
BACK PANEL

The Back Panel consists of the logic board wire wrap assembly and guiding piece parts for the logic cards.

Logic cards are plugged into the logic board wire wrap assembly. Guide rails connected to perpendicular panels guide the cards into place and restrict horizontal or vertical movement.

Wire wrap pins extend through the back panel. The logic cards mate with these pins on one side of the back panel. On the other side, the "wire wrap" side, wiring interconnects the logic functions between cards. This wiring is secured to the pins by the wire wrap technique. These pins also provide convenient test points for monitoring logic levels of all signals entering and leaving each card.

The wire wrap surface of the logic board wire wrap assembly contains wire wrap pin identification (Figure 1-1). Logic cards are designated by horizontal row (A, B, C, or D) and vertical column (1 through 30). Wire wrap pins are then called out by pin number and column A or B. For example, A8-12B is the back panel pin at logic row A, position 8, pin 12 of column B.



Wire Wrap Pin Identification

A8	Position 8 in Chassis Row A	A8	Location of Logic Card. Connector 8 of Row A. Location of full size cards identified with top connector.
12B	Pin number 12 in Column B	xxx	Special circuit characteristics. (Oscillator frequency, delay period, etc.)
3A	Pin number 3 in Column A. When Chassis Row and Position are not listed it is identical to the one above it.	2	Input applied to transistor Q2.
JA80	Auxiliary connector used to input or output signals to/from Back Panel.	4	Output transistor (if applicable) Q4.
5A	Pin number 5 in Row A	—/—	non Logic Level
	<u>Logic Representation</u>	>>, <	Pin connections.
X/Y	Function symbol	←	Indicates direction of signal flow.
L005	Logic term or identifier	—1870	When no pin connections are indicated, it is a continuous fail going from preceding term to indicated term. Page number will be given if different, (xx-1870).
VHI	Circuit type designator. Alpha characters indicate discrete components, (see Part 3). Numeric characters indicate integrated circuits (see Part 2).		

7J192

Figure 1-1. Wire Wrap Board Assembly

JA80 through JA85 and JA90 through JA95 are auxiliary connectors used to interface logic cards with maintenance panel, I/O connectors, etc. Pin identification is by pin number (1 through 14) and row (A or B). (JA80-5A is auxiliary connector JA80, pin 5, row A).

LOGIC CARDS

PHYSICAL DESCRIPTION

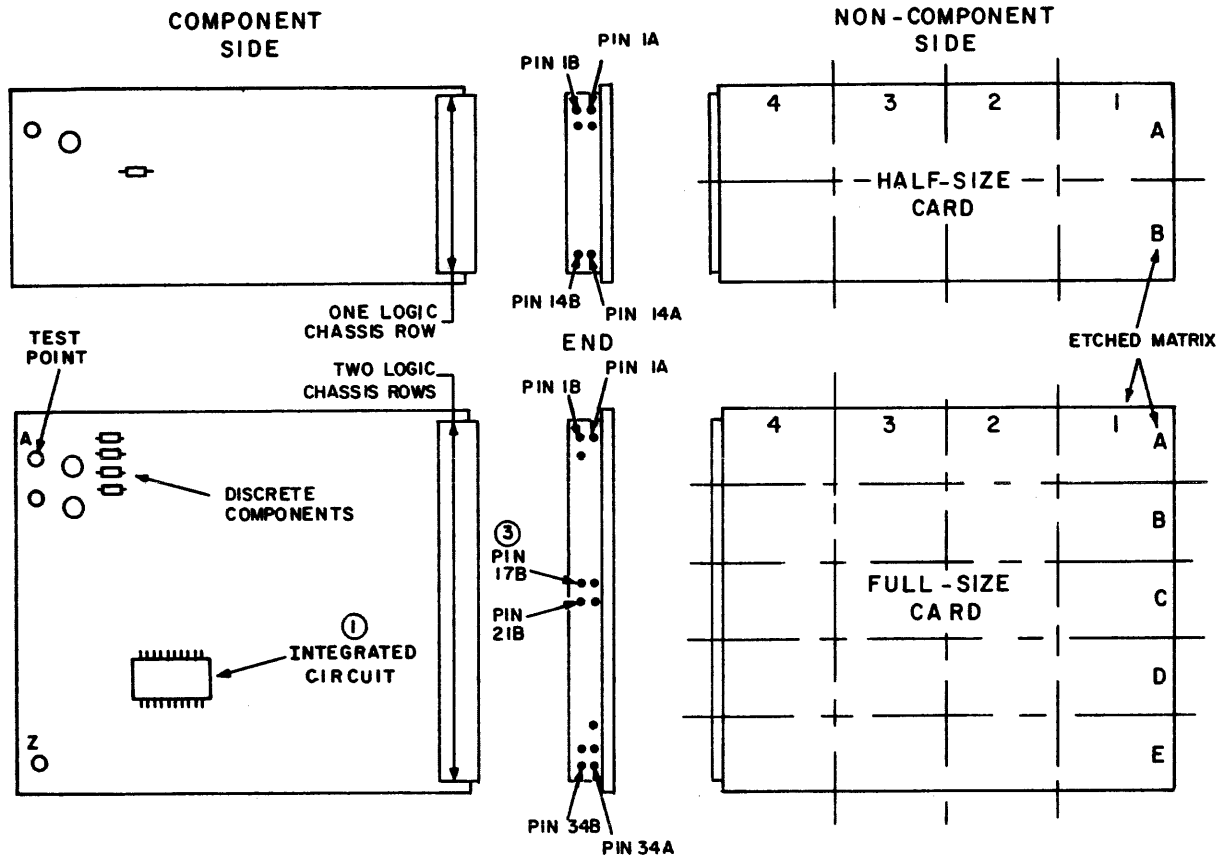
All components of the logic cards (Figure 1-2) are mounted on one side of a printed circuit board (PCB). Two sizes of PCB are used. The 6.075 x 2.3 inch PCB is called the half-size card (plugs into one logic row). The 6.075 x 4.85 inch PCB is the full-size card. The latter card spans two rows of the logic chassis.

Numerical designators (1 through 99) are etched on the non-component side of the board identify each transistor. A 4-character alpha-numeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alphanumeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

PIN ASSIGNMENTS

Half-size cards are equipped with a 28-pin (sockets) connector, while the full-size card contains a 62-pin connector. Connectors are mounted along the shorter dimension on the component side of the board.

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34, however pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.



NOTES:

- ① INTEGRATED CIRCUIT LOCATED AT BOARD MATRIX D2
2. ON LOGIC DRAWINGS, CARD PINS AND MATRIX LOCATIONS, ARE PRECEDED BY 3 DIGITS THAT IDENTIFY LOCATION OF CARD IN LOGIC CHASSIS (A23, POSITION 23 IN CHASSIS ROW A)
- ③ PINS 18, 19, 20, (A AND B) NOT PRESENT

676

Figure 1-2. Logic Card Detail

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

TEST POINTS

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alphanumerically starting with A on the top, outer edge. Test points A and Z are available for ground reference on full-size cards. Only test point Z is available for ground reference on half-size cards.

LOGIC SYMBOLOLOGY

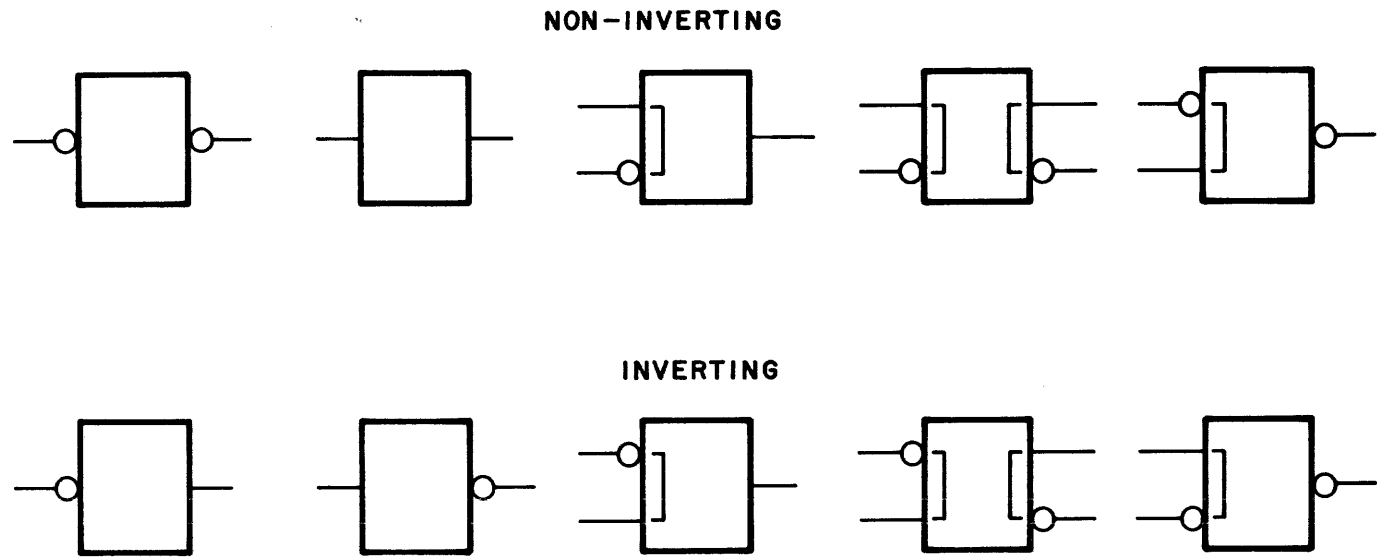
INPUT/OUTPUT STATE INDICATORS

Input/output state indicators are the polarity indicator ($\text{---}\triangleright$ or $\text{---}\triangleleft$) and the logic negation indicator ($\text{---}\neg$ or $\text{---}\bar{\text{---}}$).

The input polarity indicator indicates the most negative potential is required to satisfy the logic function represented by the qualifying symbol. The output polarity indicator indicates the most negative potential is present at the output when the logic function is satisfied. The absence of the polarity indicator indicates the most positive potential is present.

The logic negation indicator is a small circle located at the origin or termination of a signal line, and tangent to a logic symbol. The presence or absence of this indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a "0" logic level on that line is needed to satisfy the function. The absence of the circle represents a logical "1" as needed to satisfy the function.

The relative level indicator depicts the occurrence of inversion. Figure 1-3 shows some representative examples of the relative level indicator being used in this manner.



677

Figure 1-3. Inversion Conventions

DYNAMIC INDICATOR


The presence of a dynamic indicator (\triangleright) just inside a symbol indicates the inputs are gated (satisfied) with the dynamic positive-going transition of the input line to the state shown. A logic negation indicator (circle) accompanying the dynamic indicator signifies that a negative-going transition is required to gate in the inputs. Absence of the dynamic indicator indicates the inputs are gated (satisfied) with the static state of the input line.

SIGNAL LINE INDICATORS

Non-Standard Levels

Some signal line indicators indicate non-standard levels on input/output lines. These signal line indicators are as follows:

 non-standard logic levels

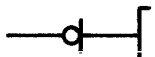
 analog or non-logic levels

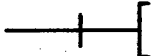
 variable control

Absence of these indicators shown above indicates a standard logic level.

Inhibit

The inhibit line indicates gating of the logic function will be inhibited whenever the line is at the level indicated by the logic negation indicator. Inhibit line symbols are as follows:


 with logic negation indicator

 without logic negation indicator

Miscellaneous

Other signal line indicators are as follows:

 test point

 twisted pair

FUNCTION SYMBOLS

Circuit function symbols for discrete components and integrated circuits are as follows:

1 OR gate or inverter

8 AND gate

=1	exclusive OR
▷	amplifier (with or without gain)
▷	amplifier with adjustable gain
Σ▷	summing amplifier
∫▷	integrating amplifier
∂▷	differentiating amplifier
X/▷	digital to analog conversion
X/▷	digital to analog conversion with adjustable gain
▷/Y	analog to digital conversion
▷ X/Y	amplifying level translator (gain noted outside box)
▷	positive analog rectifier (symbol preceded by a minus sign if negative rectification is used)
ΣX/▷	analog summation of digital inputs. Reference voltage outside box indicates output signal level resulting when specified input(s) are negated
▷ □ Y	Schmitt trigger
✕▷	saturable, non-linear, gain controlled amplifier
F▷	function generator
∩▷	active bandpass filter
∩	bandpass or resonant circuit

- $X \rightarrow Y$ coder

- X/Y Level conversion - transmission line to logic level, switch state (ground or open) to logic level, logic level to power output (to drive lamp, relay, solenoid, etc.)

- $\int X/Y$ integrating level translator

- $X/Y \int$ variable gain source amplifier

- $\int X \square Y$ switch receiver with integrating of digital signal and hysteresis


- $1 \square$ retriggerable multivibrator (single shot)

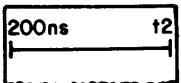
- \square voltage controlled, free running multivibrator

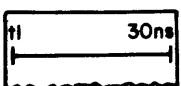
- $> 50 \text{ HZ}$ frequency sensor

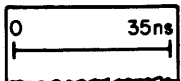
- 000 odd parity generator

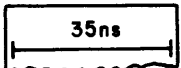
- 00 even parity generator

 symmetry restoration circuit

 ones delay - when input changes to a "1" a 200 nsec delay occurs before the "1" is passed on

 zeros delay - when input changes to a "0" a 30 nsec delay occurs before the "0" is passed on

 0 \rightarrow 1 is not delayed. 1 \rightarrow 0 delayed by 35 nsec

 both transistors are delayed by 35 nsec.

INPUT/OUTPUT DESIGNATORS

Inputs are individually identified as necessary by an input designator inside the symbol block and adjacent to the left side following all prefixes indicating dependency. These input designators follow:

R	reset or clear
S	set
G	gating type input that affects other inputs or outputs
J	J input of J-K flip-flop
K	K input of J-K flip-flop
Z	used to link gating (clock) input of control block to J and K inputs of J-K flip flops
T	toggle or complement input
D	data input of D-type flip-flops
C	a gating (clock input for D-type flip-flops
→	shift right (or down)
←	shift left (or up)
+1	increase contents by one (count up)
-1	decrease contents by one (count down)
]OR[indicates grouped inputs that maintain a fixed relationship in states and always change together

1, 2, 4, 8 indicates relative weighting of inputs or outputs in codes. They may be consecutive, binary, decimal representation of binary values, etc.

A, B, C, ETC. when two or more of these are used together in inputs to a symbol, it indicates individual signals or individual groups of signals to be identified for further operations such as arithmetic functions

Certain input designators (C and G) may also be used as prefixes to other input designators, but not to each other, C and G indicate dependency of every designator, such as D, they prefix, and are referred to as dependency notation. For example, CD indicates that the input is gated to a D-type flip-flop only when the C input is active. Gate dependent inputs (G) may be distinguished from each other by 1, 2, etc. following the G. Where more than a single G term is involved, commas are used to separate the numbers. Clock dependent inputs for loading data are denoted by a "C". Different C inputs are distinguished by a number following the C.

COMMON CONTROL BLOCK

Signals entering the common control block (Figure 1-4) are common to more than one section of the circuit. The neck of the common control block abuts the top or bottom of the sections it controls. Input designators may include C, G, R, →, ←, +1, -1, plus select lines with or without decoding.

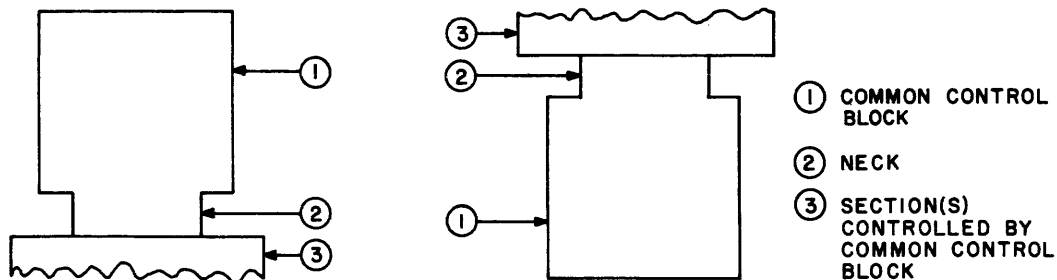
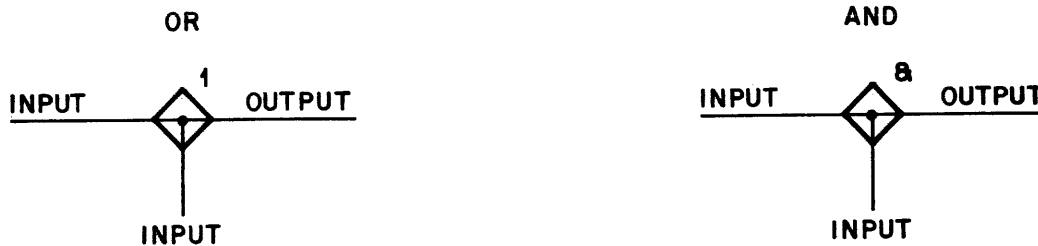


Figure 1-4. Common Control Block

WIRED FUNCTIONS

The logical representation for wired functions is shown in Figure 1-5. These functions are used where circuits have the capability of being combined as an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function simply requires that one of the inputs be a logic "0" before the output can be a logic "0". The wired AND output will be a logic "1" only when both inputs are logic "1's".



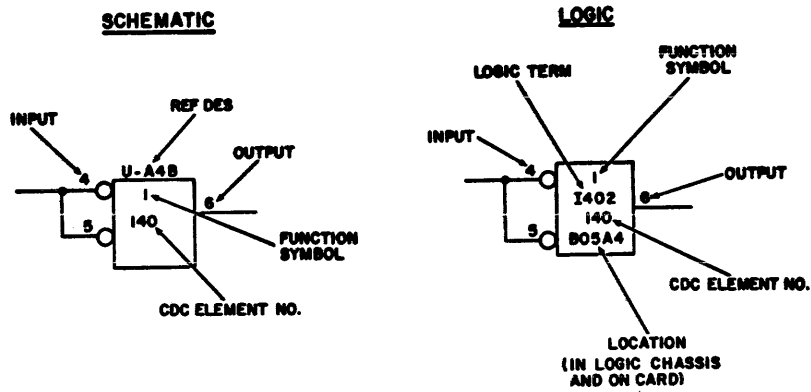
6710

Figure 1-5. Wired Functions

INTEGRATED CIRCUITS

Figure 1-6 shows the schematic version (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

Referring to Figure 1-6 it is apparent that the two versions are essentially the same. Both views identify pin numbers, the function symbol, and the CDC element number for the circuit. Refer to Section 2 for manufacturer's information on the various element numbers. One line of information appears on the logic version that does not appear on the schematic block. This is the logic term designator which identifies this term on a logic drawing. No other logic term has the same term designator as another term.



6704

Figure 1-6. Integrated Circuit

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbols reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5 of row B.

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can amplify signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used extensively in the drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain.
2. Infinite input resistance.
3. Zero output resistance.
4. Zero offset; output is zero when input is zero.
5. High bandwidth frequency response.

BASIC CIRCUIT ELEMENTS

Figure 1-7 is a highly simplified schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

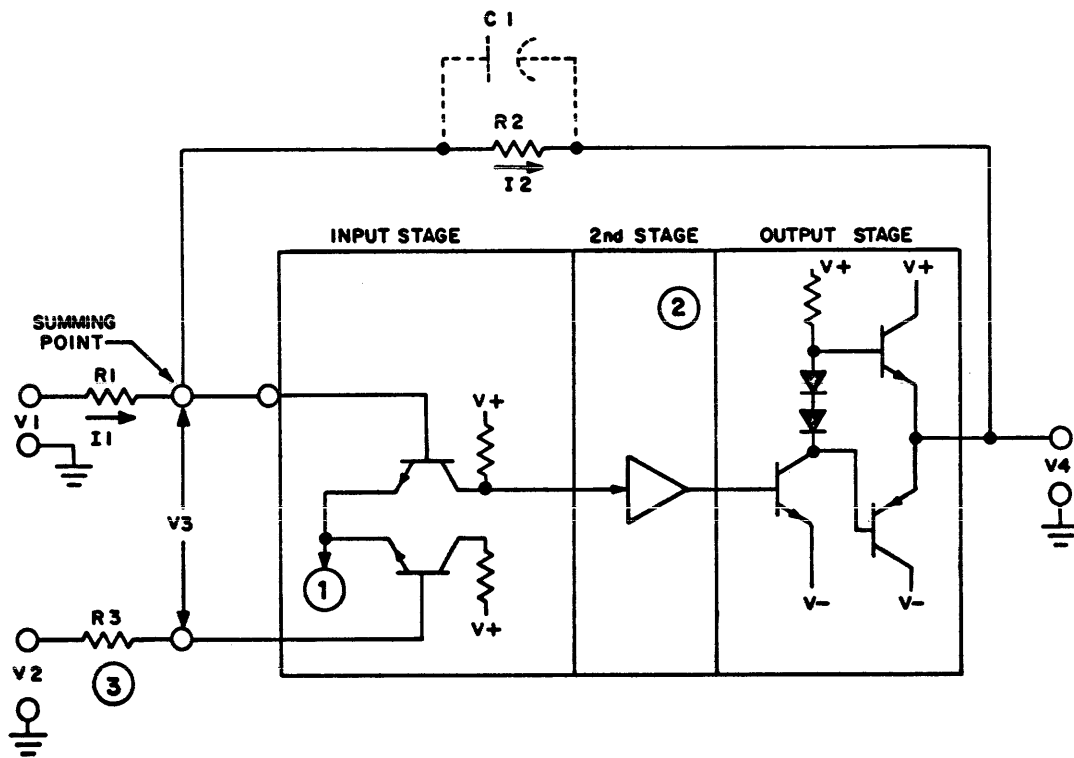
INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FETs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 millivolts are applied to the non-inverting input while 9 millivolts are applied to the inverting input, the extra 1 millivolt difference is amplified. The amplification, which may be a voltage gain of up to 100,000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the "common-mode" input signal. In the preceding example, the 9 mv are the common-mode input, while 1 mv is the differential input. In the ideal op amp, the output is zero with identical inputs. Only the difference (1 mv) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.



NOTES; (1) TO COMMON CONSTANT-CURRENT SOURCE.

(2) NOT APPLICABLE TO ALL TYPES. REFER TO MANUFACTURER'S DATA SHEET.

(3) FOR BALANCED INPUT IMPEDANCE,

$$R3 = \frac{R1 R2}{R1+R2}$$

7J133

Figure 1-7. Simplified Op Amp Schematic

BASIC CIRCUIT FUNCTIONS (FIGURE 1-7)

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio of R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; it can be assumed to be zero.
2. The differential voltage (V3) is insignificant and can be assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current I1) entering the summing point must leave it (I2). These currents are:

$$I1 = V1/R1$$

$$I2 = -V4/R2$$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohms Law:

$$V4/V1 = -R2/R1 \text{ or } V4 = -V1(R2/R1)$$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, as frequency increases, the effective impedance of R2-C1 decreases to reduce overall gain.

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset, that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made to be equal, that is, they see equal input impedances, they are common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule #2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a "virtual" ground, that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

Typical op amp circuit functions are illustrated in Figure 1-8.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (Figure 1-9). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open loop configuration; if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

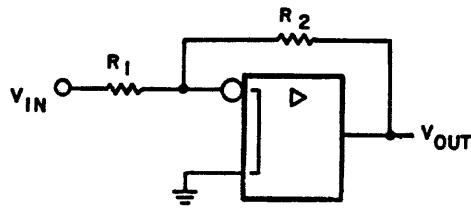
All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

CIRCUIT TYPE

SYMBOL

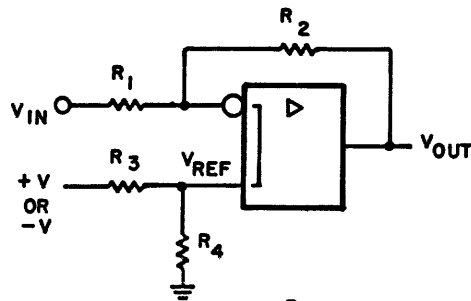
OUTPUT ^①

INVERTING AMP



$$V_{OUT} = - \frac{R_2}{R_1} V_{IN}$$

INVERTING AMP WITH REFERENCE VOLTAGE



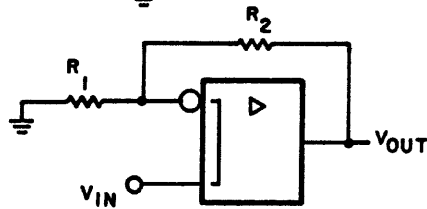
$$V_{OUT} = V_{REF} + \frac{R_2 (V_{REF} - V_{IN})}{R_1}$$

OBSERVE ALGEBRAIC SIGNS IF COMPUTING

$$V_{OUT} = 0 \text{ IF } V_{IN} = V_{REF}$$

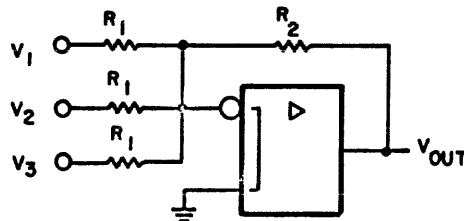
$$V_{REF} = \pm V \left(\frac{R_3}{R_3 + R_4} \right)$$

NON INVERTING AMPLIFIER



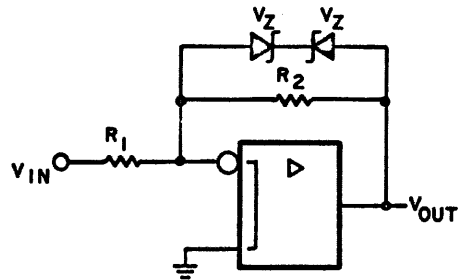
$$V_{OUT} = \frac{V_{IN} (R_1 + R_2)}{R_1}$$

SUMMING AMPLIFIER



$$V_{OUT} = - \left[\frac{R_2}{R_1} (V_1 + V_2 + V_3) \right]$$

INVERTING AMPLIFIER WITH OUTPUT LIMITING



$$V_{OUT} = - \frac{R_2}{R_1} V_{IN}$$

$$\text{IF } \pm V_{OUT} \leq V_Z$$

NOTE:

① MINUS SIGN (-) INDICATES THAT OUTPUT IS INVERTED.

7J91-1

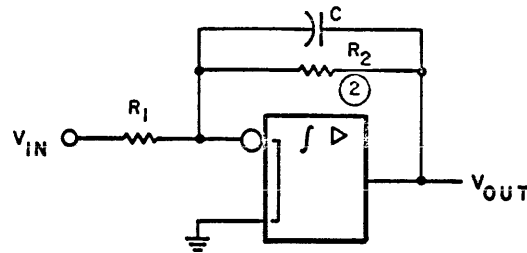
Figure 1-8. Op Amp Circuit Functions (Sheet 1 of 3)

CIRCUIT TYPE

SYMBOL

OUTPUT ①

INTEGRATING
AMPLIFIER

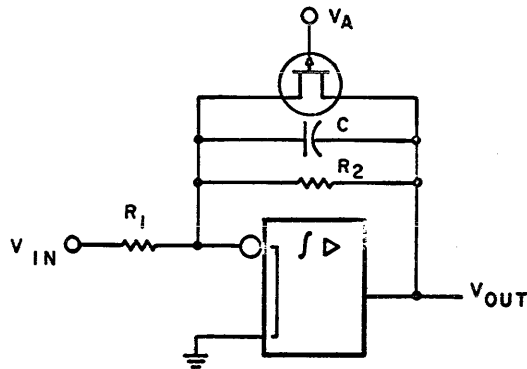


$$V_{OUT} = - \frac{1}{R_1 C} \int V_{IN} dt$$

IF V_{IN} IS CONSTANT,

$$V_O = - \frac{V_{IN} \times \text{TIME}}{R_1 C}$$

INTEGRATING
AMPLIFIER CONTROLLED
BY P-CHANNEL
JFET



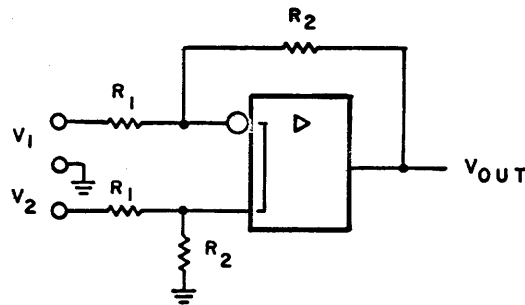
(A) IF V_A IS 0V

$$V_{OUT} = 0V$$

(B) IF V_A IS +14V

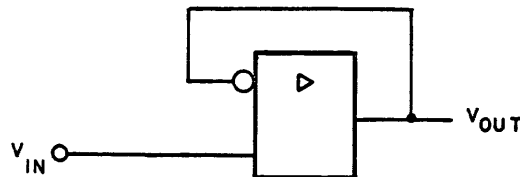
$$V_{OUT} = - \frac{1}{R_1 C} \int V_{IN} dt$$

DIFFERENTIAL
AMPLIFIER



$$V_{OUT} = \frac{R_2 (V_2 - V_1)}{R_1}$$

VOLTAGE
FOLLOWER



$$V_{OUT} = V_{IN}$$

NOTES:

- ① MINUS SIGN(-) INDICATES THAT OUTPUT IS INVERTED.
- ② R_2 USED TO PROVIDE DC FEEDBACK TO KEEP OUTPUT SYMMETRICAL ABOUT GROUND.

7J91-2

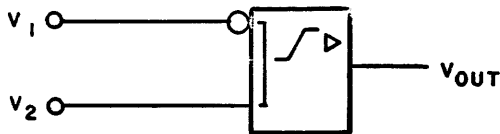
Figure 1-8. Op Amp Circuit Functions (Sheet 2 of 3)

CIRCUIT TYPE

SYMBOL

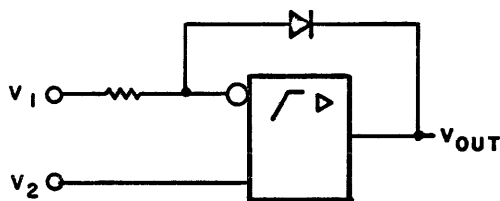
FUNCTION

OPEN LOOP
(COMPARATOR)



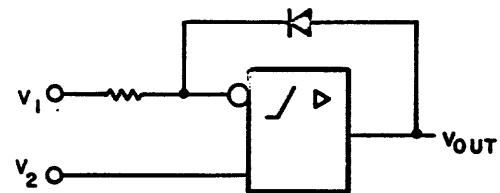
$$\begin{aligned}
 V_{OUT} &= +V_{SAT} && \text{IF } V_1 < V_2 \\
 V_{OUT} &= 0V && \text{IF } V_1 = V_2 \\
 V_{OUT} &= -V_{SAT} && \text{IF } V_1 > V_2
 \end{aligned}$$

SATURABLE
COMPARATOR



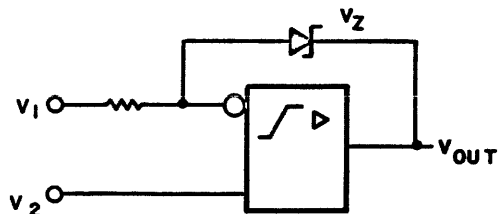
$$\begin{aligned}
 V_{OUT} &= +V_{SAT} && \text{IF } V_1 < V_2 \\
 V_{OUT} &= 0V && \text{IF } V_1 = V_2 \\
 V_{OUT} &= V_2 && \text{IF } V_1 > V_2
 \end{aligned}$$

SATURABLE
COMPARATOR



$$\begin{aligned}
 V_{OUT} &= V_2 && \text{IF } V_1 < V_2 \\
 V_{OUT} &= 0V && \text{IF } V_1 = V_2 \\
 V_{OUT} &= -V_{SAT} && \text{IF } V_1 > V_2
 \end{aligned}$$

NONLINEAR
COMPARATOR



$$\begin{aligned}
 V_{OUT} &= V_Z && \text{IF } V_1 < V_2 \\
 V_{OUT} &= 0V && \text{IF } V_1 = V_2 \\
 V_{OUT} &= V_2 && \text{IF } V_1 > V_2
 \end{aligned}$$

NOTE:

① V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10,000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

7J91-3

Figure 1-8. Op Amp Circuit Functions (Sheet 3 of 3)

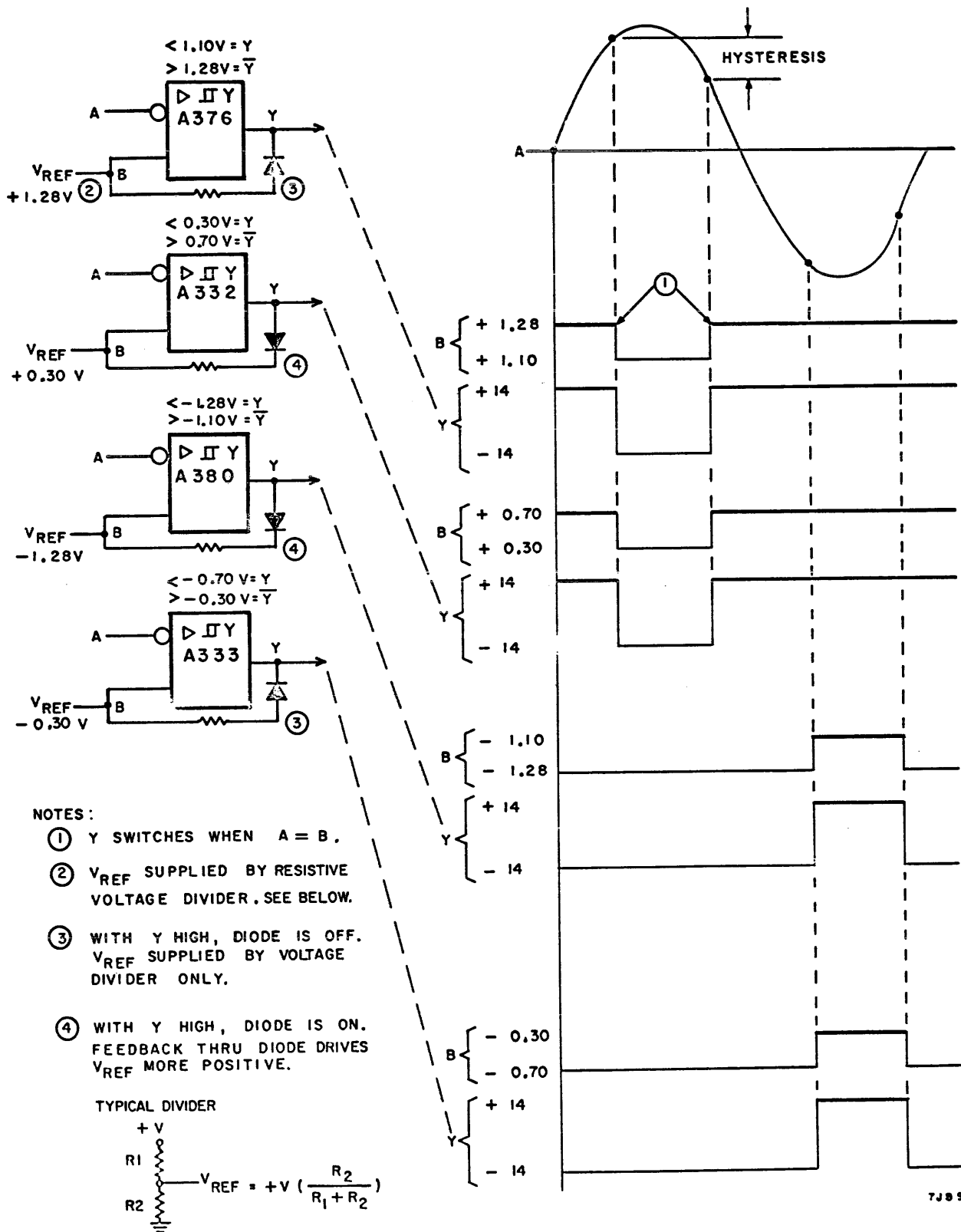


Figure 1-9. Op Amp used as a Schmitt Trigger

Consider A376 of Figure 1-9. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28V. Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

As the input A goes more positive, the output does not change until A equals B (+1.28V). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14V available at Y, the voltage at B is reduced to +1.10V. The input must now swing to less than +1.10V for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

DISCRETE COMPONENT CIRCUITS

Figure 1-10 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Four lines of information are contained within the logic symbol. The top line is the function symbol and designates the board logic function of that particular symbol. In this case, represents an amplifier, the logic function performed by the circuit. The third line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator, detailed information on that particular circuit may be obtained by referring to Section 3.

The second line within the symbol is used to differentiate that particular symbol from similar symbols that appear on the logic diagram. It is called the logic term and consists of a one-letter prefix and an assigned identification number (in this case, A705).

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (i. e., Q22 on the card schematic diagram).

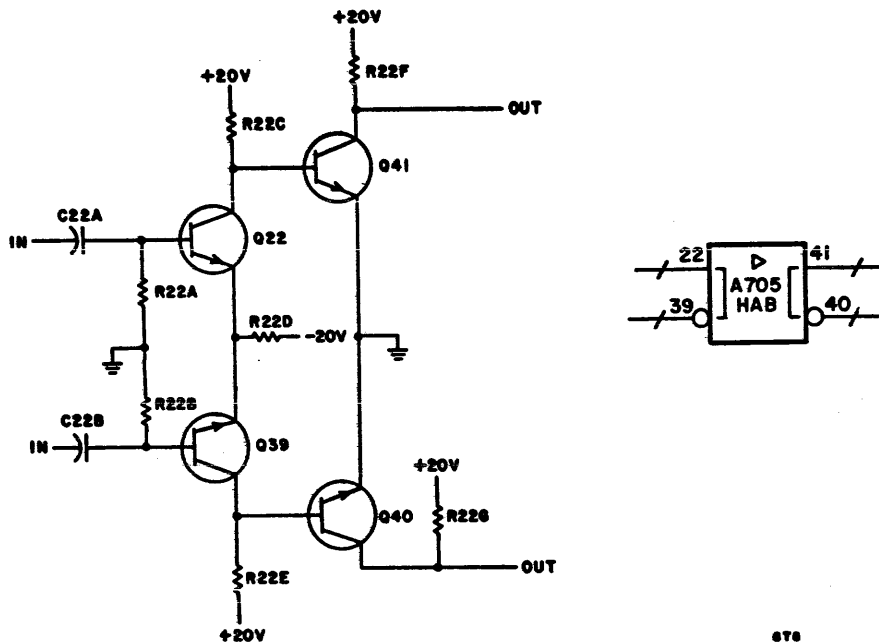


Figure 1-10. Discrete Component Circuit

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

The lines on the interior of the logic block that bracket both inputs and both outputs show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

For schematic diagrams of discrete component circuits used in this device see Section 3. An analysis of circuit operation supports each circuit diagram. The order of presentation is in accordance with the 3-letter alphabetical circuit type designator.

SECTION 2

INTEGRATED CIRCUIT PACKAGE CONFIGURATIONS

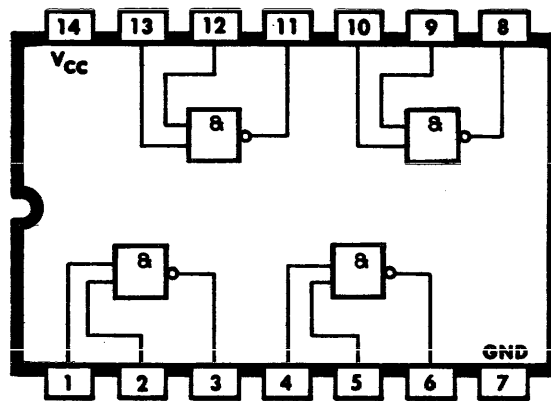
INTEGRATED CIRCUIT INDEX				
CDC Circuit Type	CDC Part No.	MFGR **	MFGR's Part No.	Revision Date
139*	51657100	F	U5F771139X	9-29-72
140	51651900	F	9002	4-10-72
140S	50254600	T	74S00	4-10-72
141	50250700	F	9003	4-10-72
143	51639900	F	9009	4-10-72
143S	50254800	T	74S40	4-10-72
144	41523200	F	9001	4-10-72
145	51701900	F	9005	4-10-72
146	51701800	F	9016	4-10-72
147	50251900	F	9007	4-10-72
149H	50251800	M	3021	4-10-72
158	51761500	F	9316	4-10-72
159	51754700	F	9300	4-10-72
161	51718600	F	9601	4-10-72
162	50252900	T	75107	12-1-72
164H	50250900	M	3062	4-10-72
164S	50255000	T	74S113	4-10-72
166	50252200	F	9312	4-10-72
172H	50251600	M	3002	4-10-72
173H	50251700	M	3004	9-29-72
175H	50251500	M	3060	12-1-72
176	50252800	T	75110	4-10-72
182	50252000	T	74197	9-29-72
182	50252000	S	8291	9-29-72
188	51783900	F	9015	5-7-74
189	51784000	F	9322	4-10-72
191	95305700	F	9301	4-10-72
193	50254300	T	74123	12-1-72
195	15104300	F	9602	12-1-72
200	50254200	T	7406	9-29-72
208S	50254900	T	74S20	4-10-72
218	15107500	M	3003	5-7-74
300*	84667800	F	UB5770939X	9-29-72
301*	50251300	F	U5B7741393	9-29-72
304*	50254400	F	U5F7715393	9-29-72
307*	51753300	F	U5B771039X	9-29-72
308*	15106100	S	NE531	9-29-72
309*	95817600	RCA	CA3001	9-29-72
315*	15110800	RCA	CA3040	9-29-72
316*	15110900	N	LH0002CH	9-29-72
321S	15115400	TE	TSC4711	12-1-72
350*	50254100	M	MC1463R	9-29-72
351*	50254000	M	MC1469R	9-29-72
380*	50256900	RCA	RCA51258	9-29-72
502	15105400	T	74180	4-10-72
519	15104400	T	74174	12-1-72
521	36188100	T	7483	9-29-72
579	15106400	S	NE562	4-10-72
AMP-1*	11844900	CDC		9-29-72
AMP-2*	40132000	CDC		9-29-72

*Integrated circuit operational amplifiers (op-amps) are not considered field replaceable due to balancing problems and are not included within this section. Refer to Manufacturer's Data Handbook for op-amp circuit information.

**MFGR's - F = Fairchild Semiconductors
- T = Texas Instruments
- M = Motorola Semiconductor Products, Inc.
- S = Signetics Corporation
- N = National Semiconductor
- TE = Transiltron Electronics



LOGIC SYMBOL



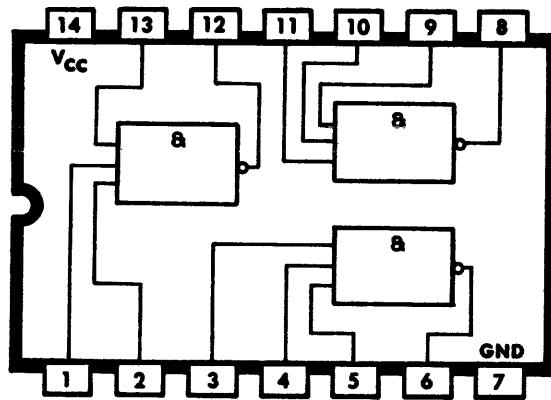
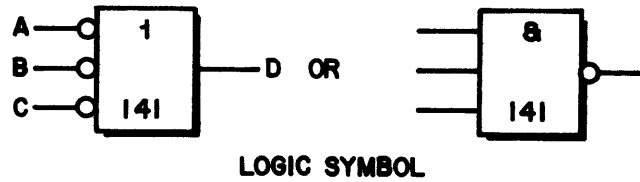
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE
(FOR ONE GATE)

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 140 manufactured by Fairchild Semiconductors (P/N 9002) used for low speed applications.
4. Type 140S manufactured by Texas Instruments (P/N 74S00) used for high speed applications.

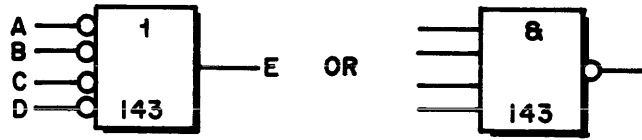


A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

**TRUTH TABLE
(FOR ONE GATE)**

NOTES:

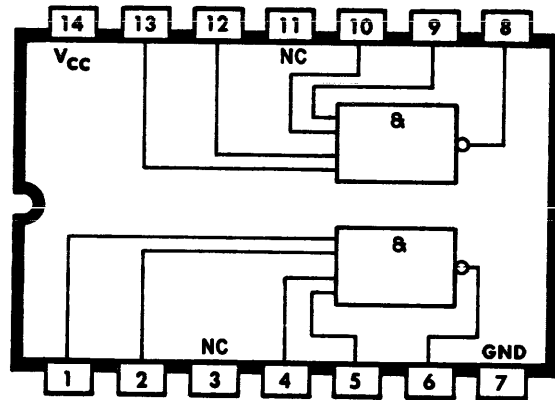
1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 141 manufactured by Fairchild Semiconductors (P/N 9003).



LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	0
0	0	0	1	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
1	1	0	0	0
1	1	0	0	1
1	1	0	1	0
1	1	0	1	1
1	1	1	0	0
1	1	1	0	1
1	1	1	1	0
1	1	1	1	1

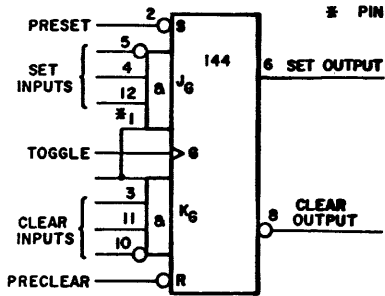
TRUTH TABLE
(FOR ONE GATE)



PACKAGE PIN CONFIGURATION

NOTES:

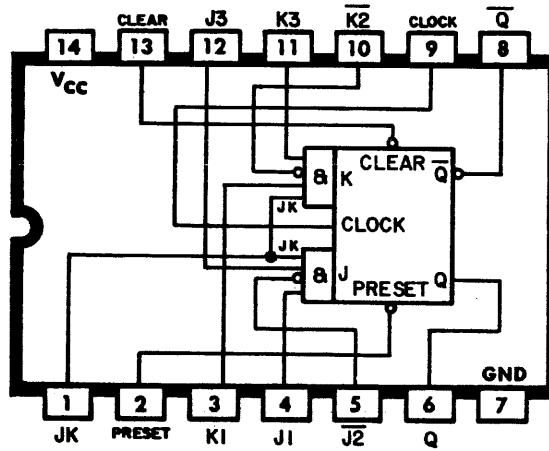
1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 143 manufactured by Fairchild semiconductors (P/N 9009) used for low speed switching applications.
4. Type 143S manufactured by Texas Instruments (P/N 74S40) used for high speed switching applications.



⊗ PIN 1 IS CONNECTED INTERNALLY TO BOTH INPUTS

- J - J OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE (⊗)
- K - K OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE (⊗)
- ⊗ - GATE INPUT, HAS NO DIRECT EFFECT ON CIRCUIT, BUT MUST PRESENT BEFORE SIGNALS PRESENT ON INPUT(S) CAN BE TRANSFERRED TO OUTPUT(S)
- S - SET INPUT, WHEN "0", FF IS SET REGARDLESS OF INPUTS AND GATE STATES
- R - RESET(CLEAR) INPUT. WHEN "0", FF IS CLEARED REGARDLESS OF INPUTS AND GATE STATES

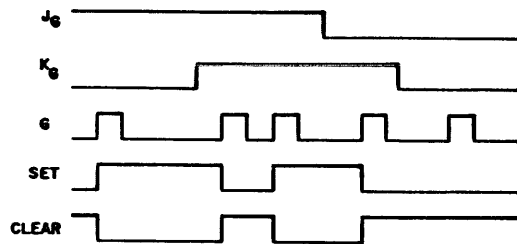
LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

INPUTS		OUTPUTS BEFORE TOGGLE		OUTPUTS AFTER TOGGLE	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

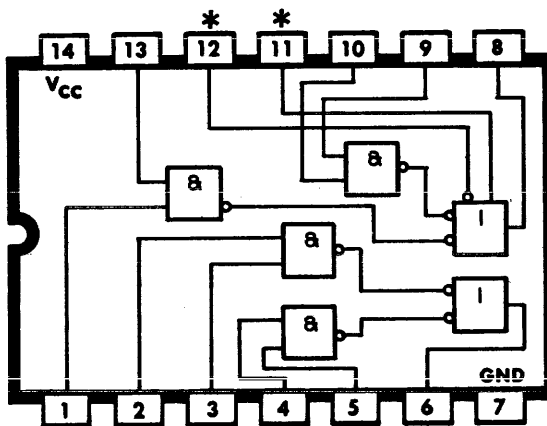
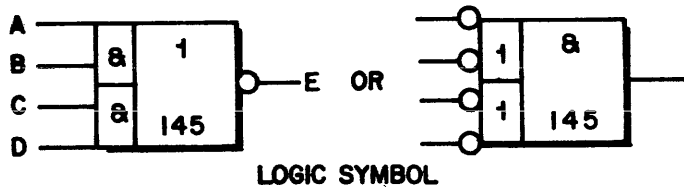
TRUTH TABLE



TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 144 manufactured by Fairchild Semiconductors (P/N 9001).



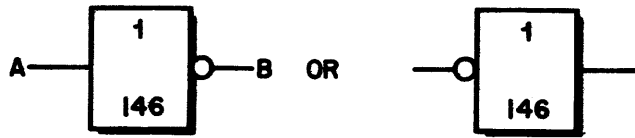
* PINS USED FOR
CONNECTING EXTENDERS

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

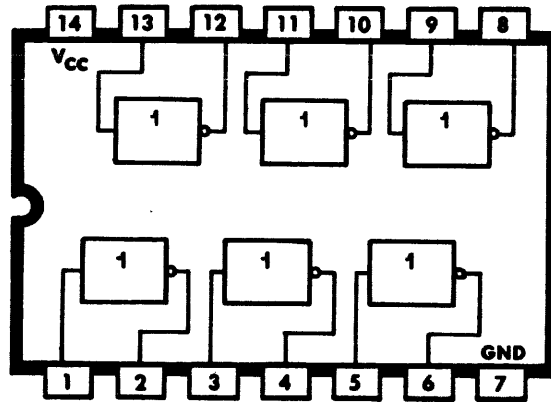
NOTES:

TRUTH TABLE

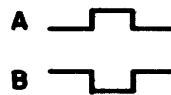
1. Symbol shown as it would appear on logic diagrams.
2. Type 145 manufactured by Fairchild Semiconductors (P/N 9005).



LOGIC SYMBOL



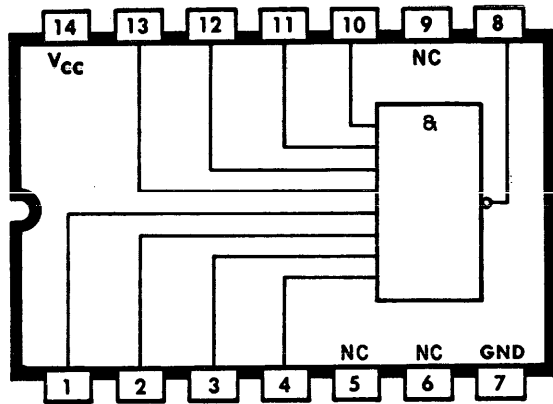
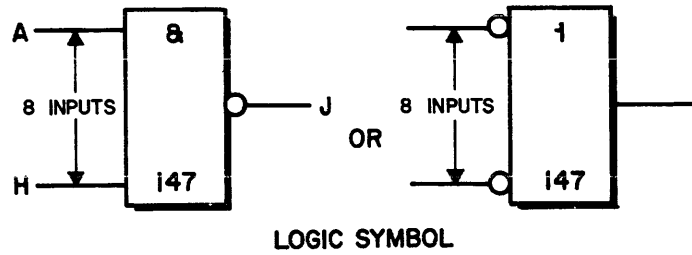
PACKAGE PIN CONFIGURATION



TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 146 manufactured by Fairchild Semiconductors (P/N 9016).



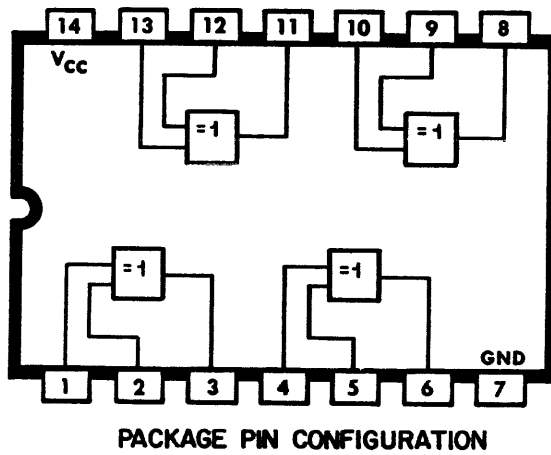
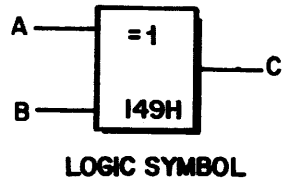
PACKAGE PIN CONFIGURATION

A	B	H	J
1	0	0	0
0	1	1	0
0	0	0	1
1	1	1	0

TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 147 manufactured by Fairchild Semiconductors (P/N 9007).

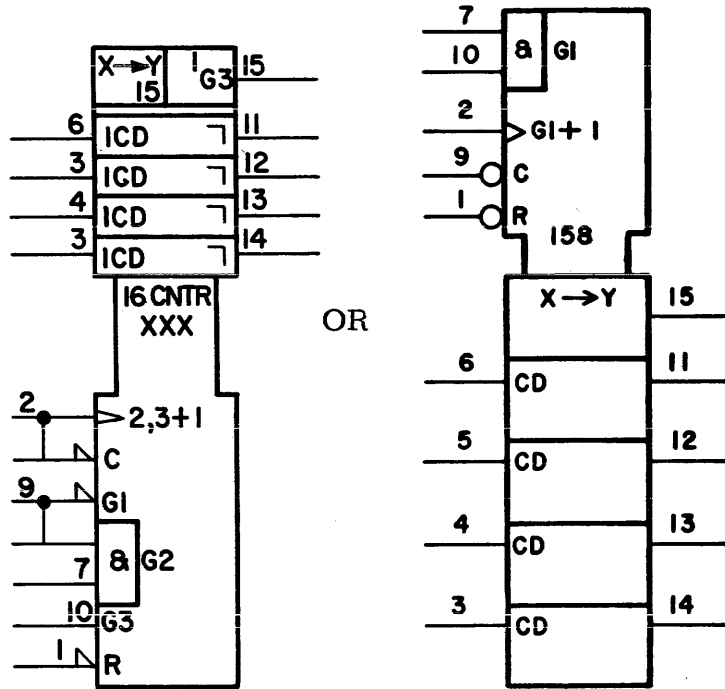


A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

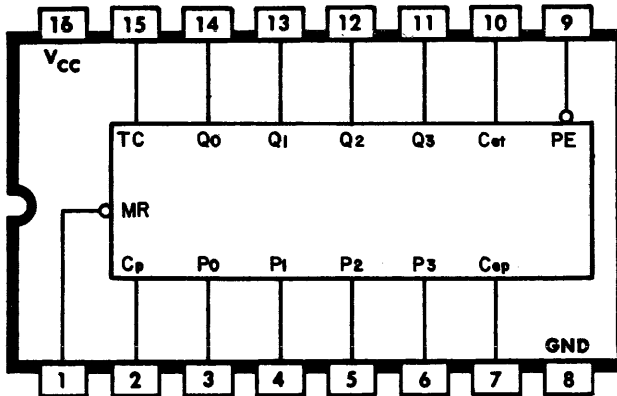
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 149H manufactured by Motorola Semiconductor Products, Inc., (P/N 3021).



LOGIC SYMBOL

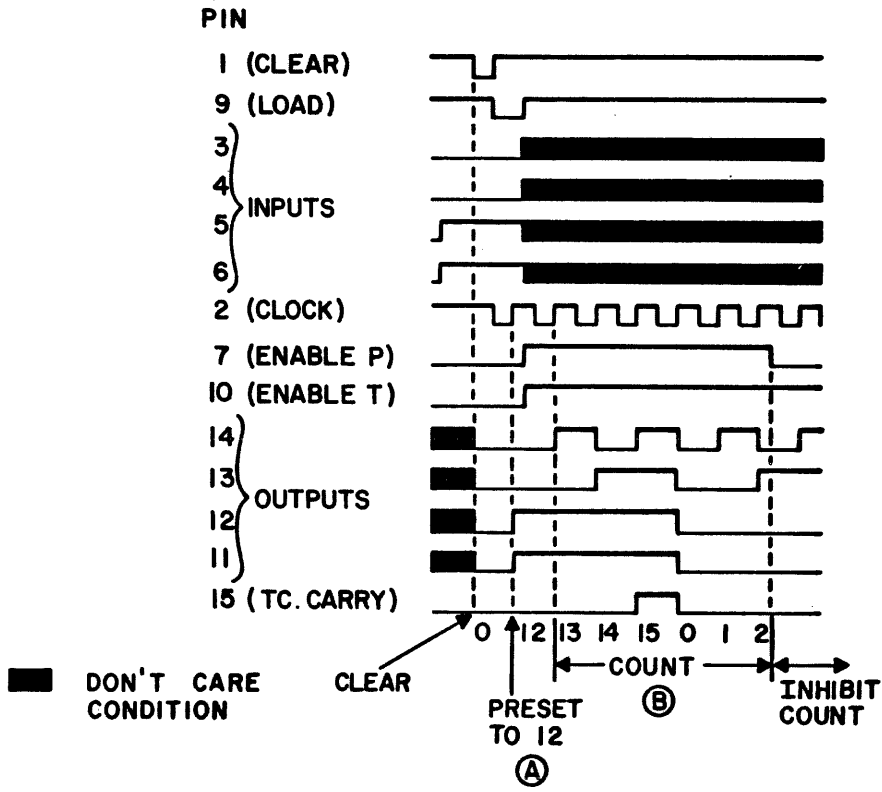


PIN(S)

FUNCTION

1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

PACKAGE PIN CONFIGURATION



(A) MODE SELECTION WITH POSITIVE - GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

(B) PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

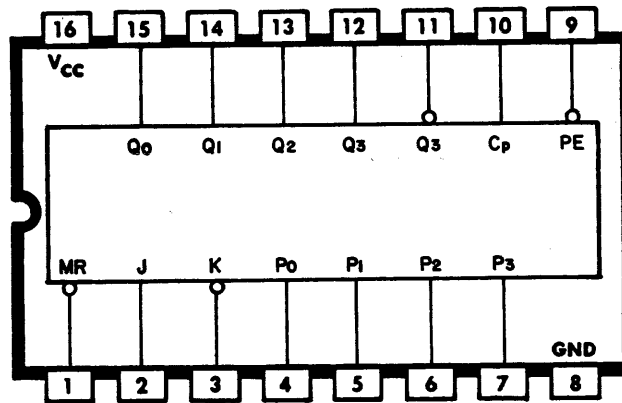
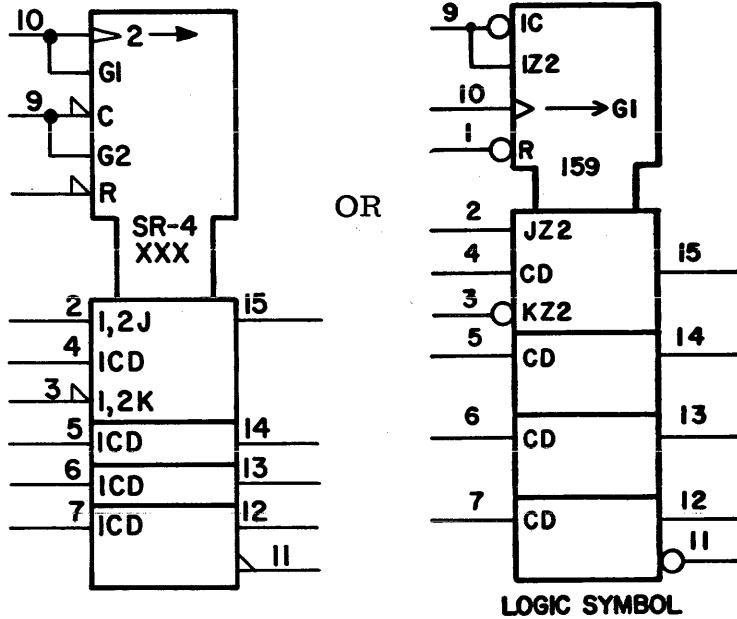
(C) ILLUSTRATED ABOVE IS THE FOLLOWING:

1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

TIMING SEQUENCE

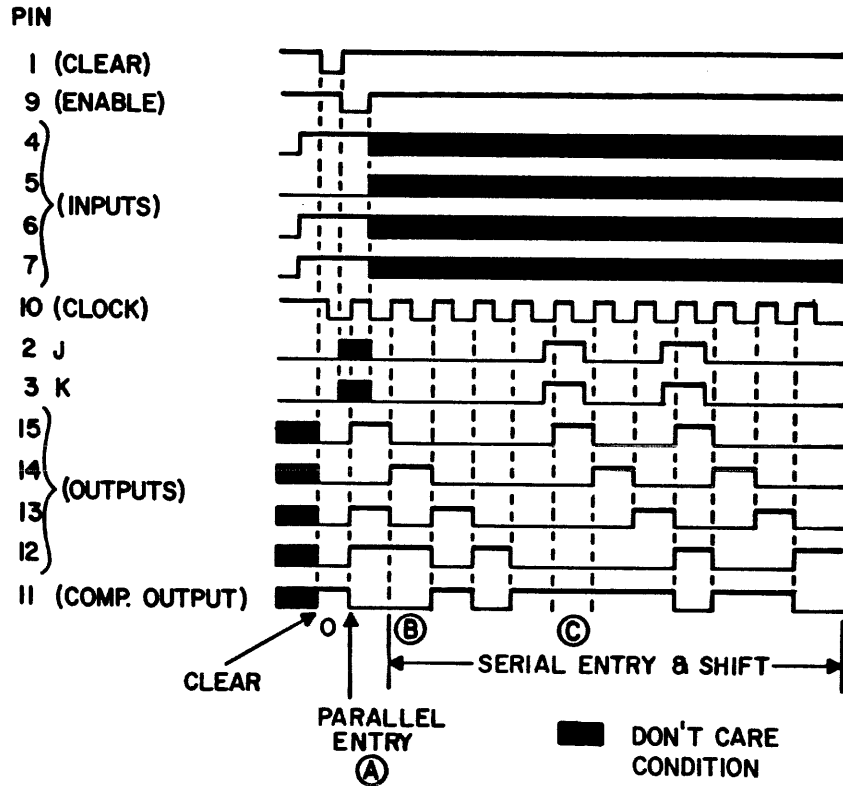
NOTES:

1. Symbol shown as it would appear on logic drawings.
2. Type 158 manufactured by Fairchild Semiconductors (P/N 9316).



<u>PIN(S)</u>	<u>FUNCTION</u>
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	FIRST STAGE J (ACTIVE HIGH) INPUT
3	FIRST STAGE K (ACTIVE LOW) INPUT
4, 5, 6, 7	PARALLEL INPUTS
9	PARALLEL ENABLE (ACTIVE LOW) INPUT (SHIFT/LOAD)
10	CLOCK (ACTIVE HIGH GOING EDGE) INPUT
11	COMPLEMENTARY LAST STAGE OUTPUT
12, 13, 14, 15	PARALLEL OUTPUTS

PACKAGE PIN CONFIGURATION



NOTES:

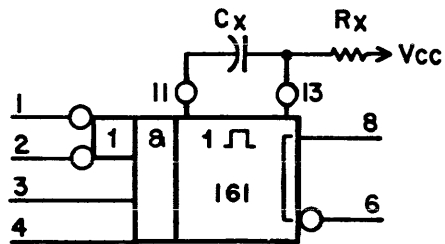
- Ⓐ DATA ENTERED INTO D-INPUT VIA PIN 4 BY PIN 9 LOW AND POSITIVE - GOING SIGNAL ON PIN 10.
- Ⓑ DATA ENTERED INTO JK(Z) INPUT BY PIN 9 HIGH AND POSITIVE - GOING SIGNAL ON PIN 10. PIN 4 INPUT INHIBITED BECAUSE OF PIN 9 HIGH. OUT IS THEN AS FOLLOWS:

INPUT PIN		OUTPUT PIN
2	3	15
0	0	0
0	1	NO CHANGE
1	0	TOGGLES
1	1	1

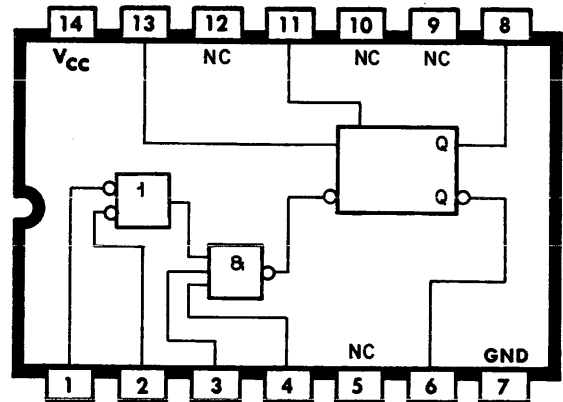
- Ⓒ DATA SHIFTS DOWN (PIN 15 — 14, ETC.) WITH CLOCK.
- TIMING SEQUENCE**

NOTES:

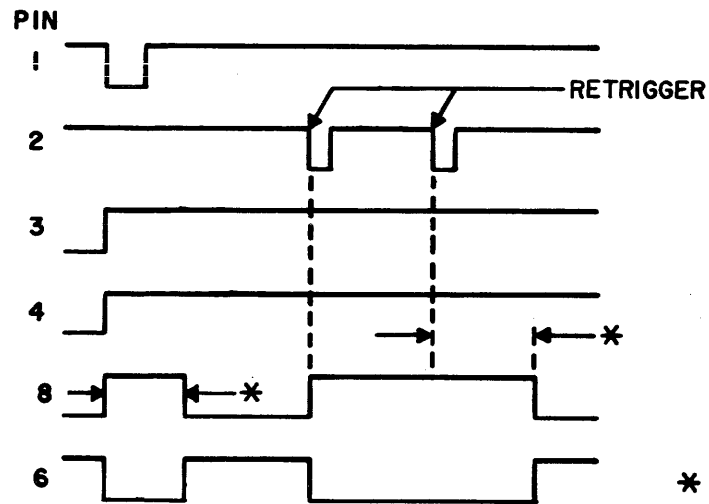
1. Symbol shown as it would appear on logic diagrams.
2. Type 159 manufactured by Fairchild Semiconductors, (P/N 9300).



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

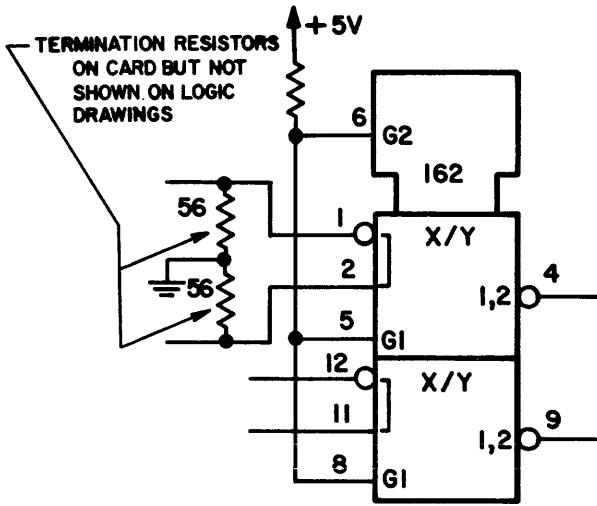


TIMING SEQUENCE

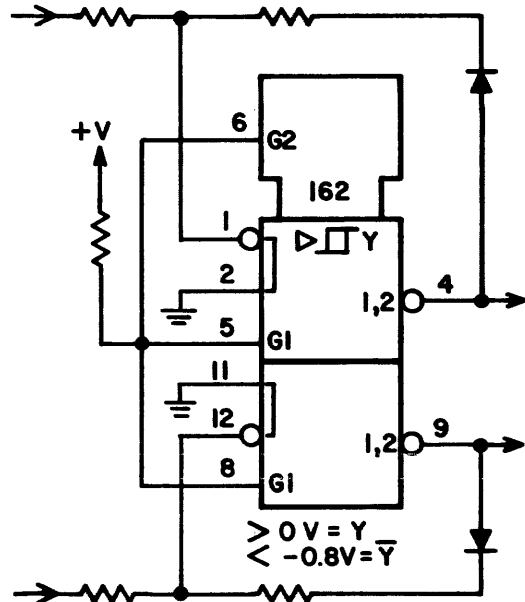
* PULSE WIDTH
DETERMINED BY
RC TIMING NETWORK

NOTES:

1. Symbol shown as it would appear on logic diagrams, except for timing network.
2. Type 161 manufactured by Fairchild Semiconductors (P/N 9601).

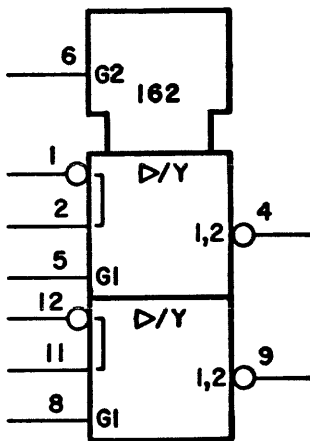


TWISTED PAIR RECEIVER APPLICATION

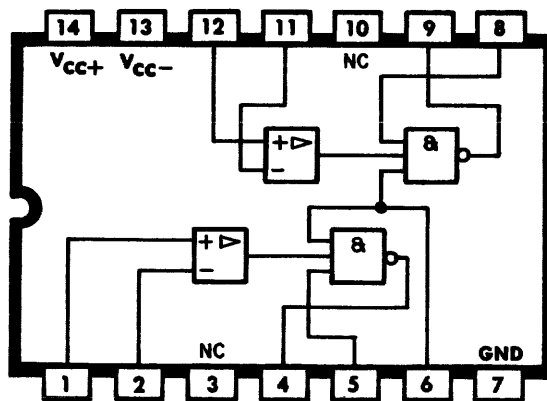


162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS.

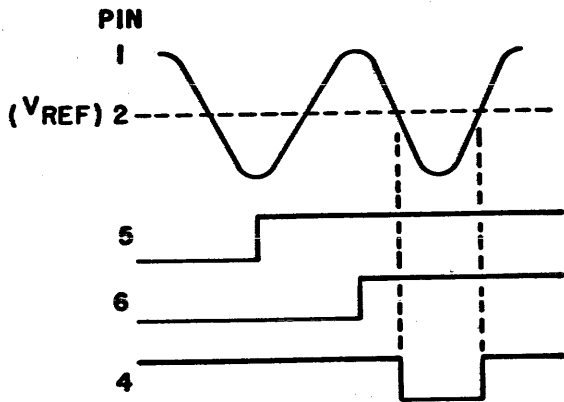
LOGIC SYMBOL



ANALOG TO DIGITAL CONVERTER APPLICATION

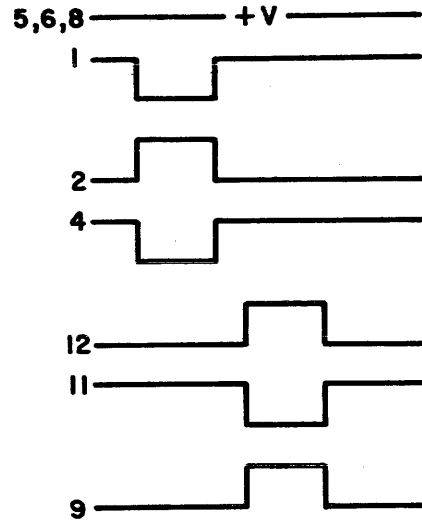


PACKAGE PIN CONFIGURATION

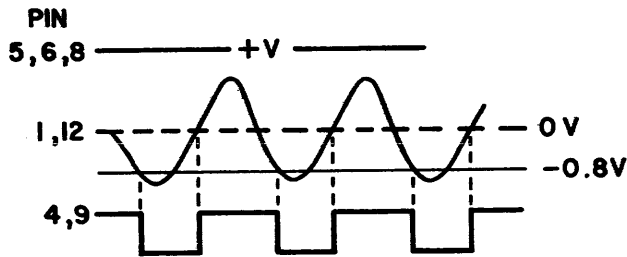


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH
AND PIN 1 IS MORE NEGATIVE THAN PIN 2.
G2 IS COMMON TO BOTH CONVERTERS.

162 DIGITAL TO ANALOG CONVERTER APPLICATION



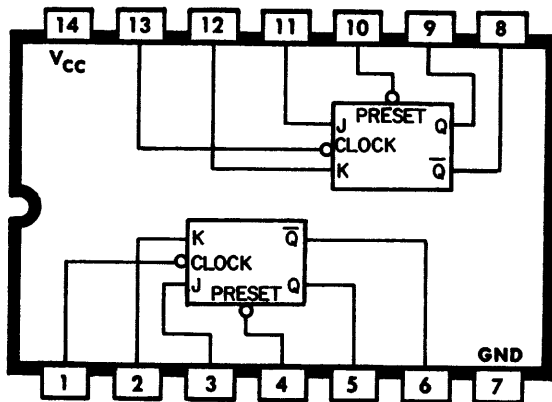
162 TWISTED PAIR RECEIVER APPLICATION



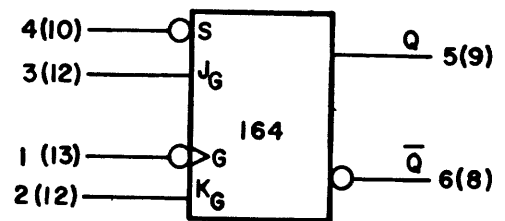
162 SCHMITT TRIGGER

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 162 manufactured by Texas Instruments (P/N 75107).



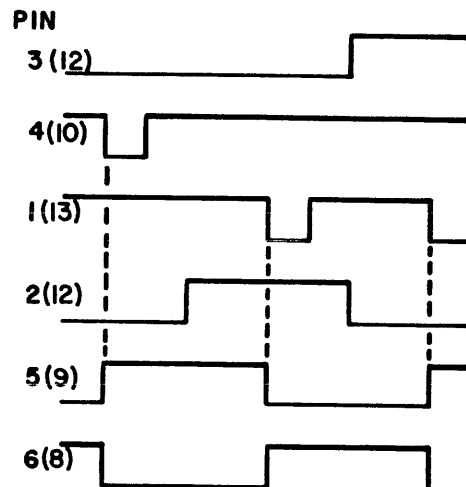
PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

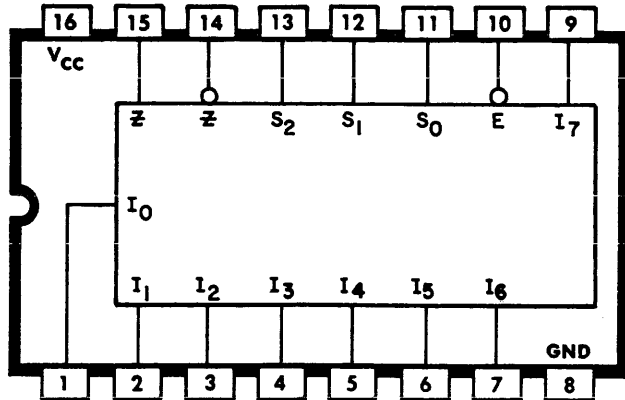
TRUTH TABLE



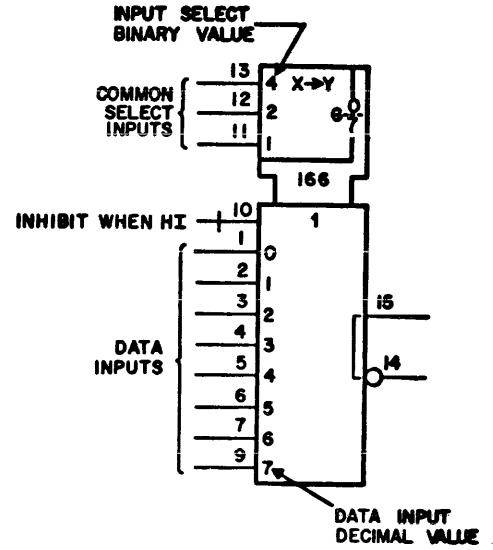
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 164H manufactured by Motorola Semiconductor Products, Inc., (P/N 3062) used for low speed applications.
4. Type 164S manufactured by Texas Instruments (P/N 74S113) used for high speed applications.



PACKAGE PIN CONFIGURATION

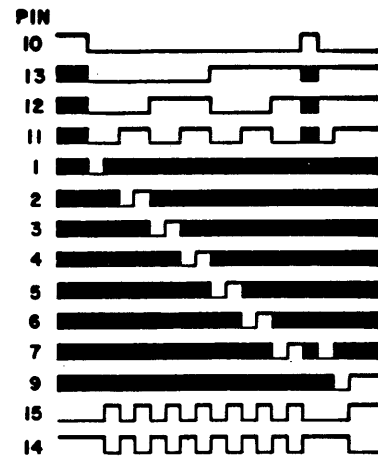


LOGIC SYMBOL

COMMON SELECT PIN			INPUT PIN GATED TO OUTPUT PIN 15 [‡] (PIN 10 LOW)
13	12	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	9

[‡] 1.) OUTPUT IS HIGH IF DATA INPUT IS HIGH.
 2.) OUTPUT IS LOW IF DATA INPUT IS LOW.
 3.) PIN 14 OUTPUT IS INVERSE OF PIN 15.
 4.) IF PIN 10 IS HIGH, PIN 15 IS LOW AND 14 IS HIGH (REGARDLESS OF SELECT/DATA INPUTS).

TRUTH TABLE

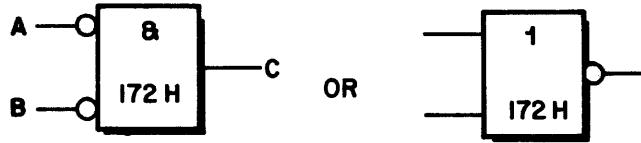


■ = DON'T CARE CONDITION

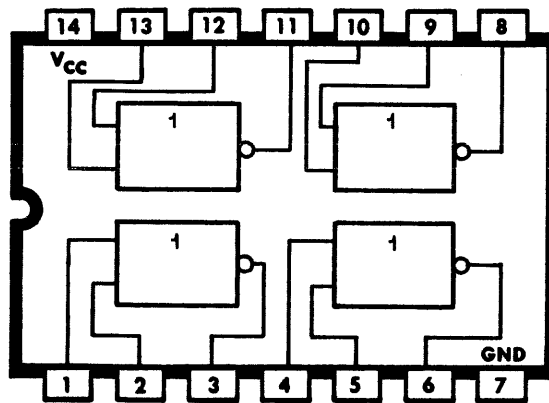
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 166 manufactured by Fairchild Semiconductors (P/N 9312).



LOGIC SYMBOL



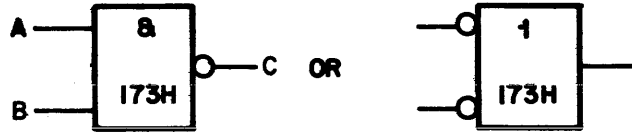
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

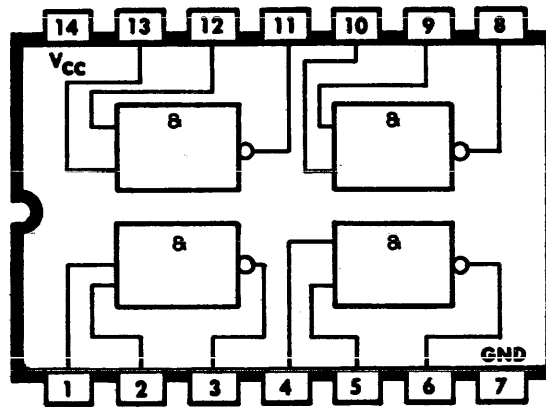
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 172H manufactured by Motorola Semiconductor Products, Inc., (P/N 3002).



LOGIC SYMBOL



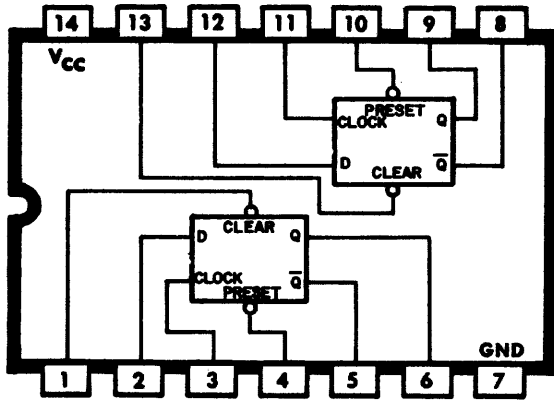
PACKAGE PIN CONFIGURATION

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

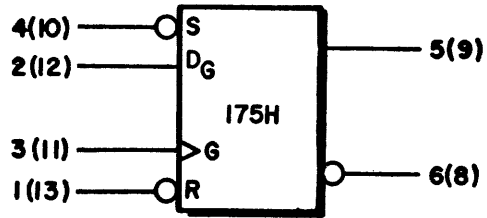
TRUTH TABLE

NOTES:

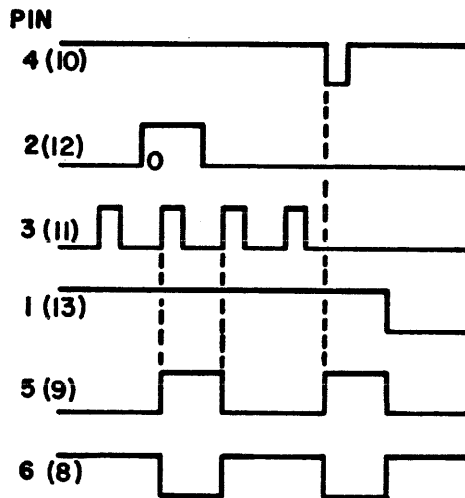
1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 173H manufactured by Motorola Semiconductor Products, Inc., (P/N 3004).
4. The output of each gate is an open collector.



PACKAGE PIN CONFIGURATION



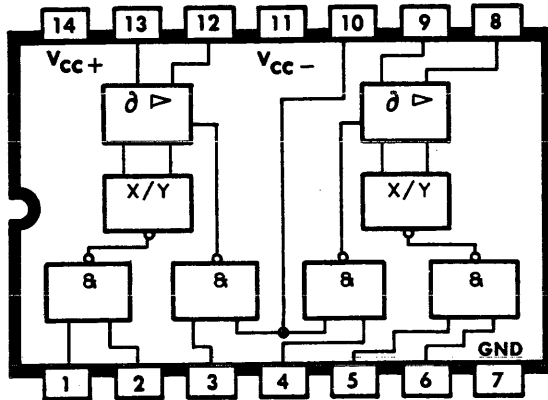
LOGIC SYMBOL



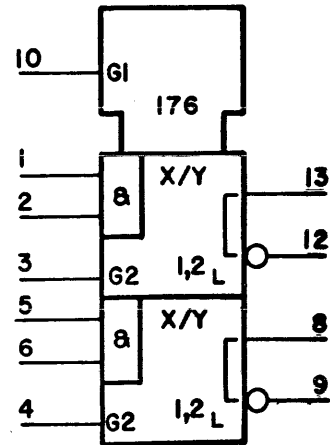
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 175H manufactured by Motorola Semiconductor Products, Inc., (P/N 3060).



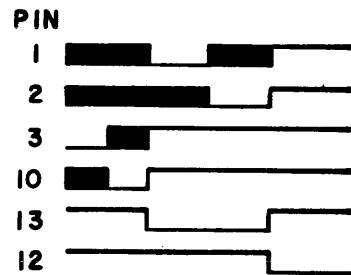
PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
1	2	3	10	12	13
1 or 0	1 or 0	1	1 or 0	1	1
1 or 0	1 or 0	1 or 0	0	0	1
0	1 or 0	1	1	0	1
1 or 0	0	1	1	0	1
1	1	1	1	1	0

TRUTH TABLE

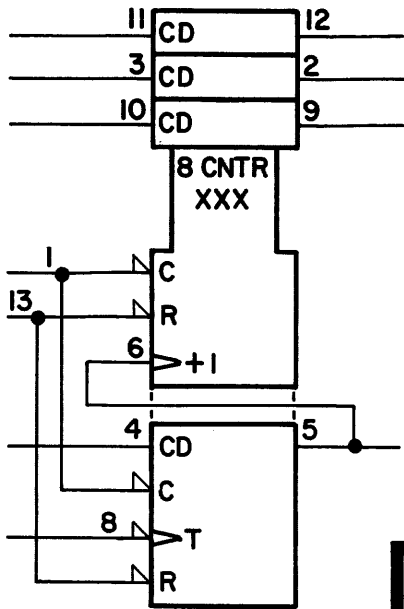


■ = DON'T CARE CONDITION

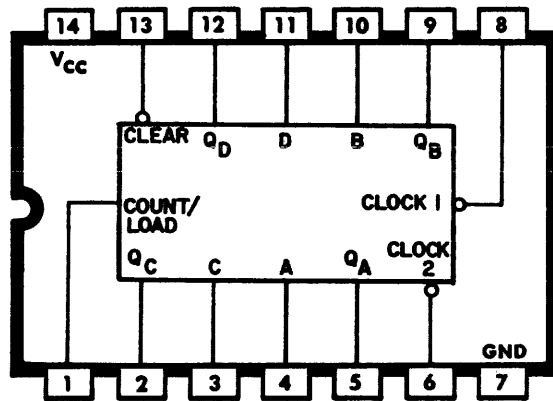
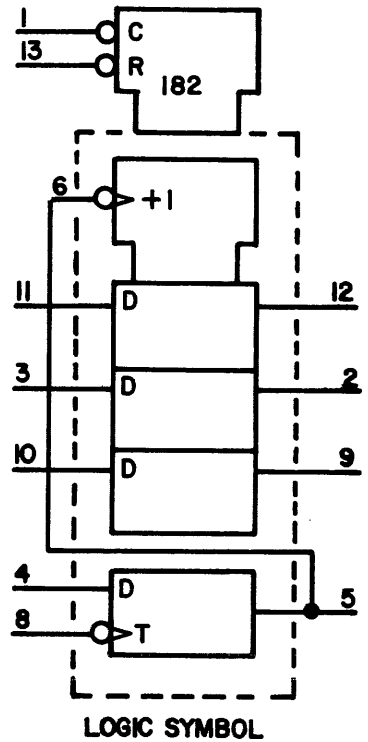
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 176 manufactured by Texas Instruments (P/N 75110).



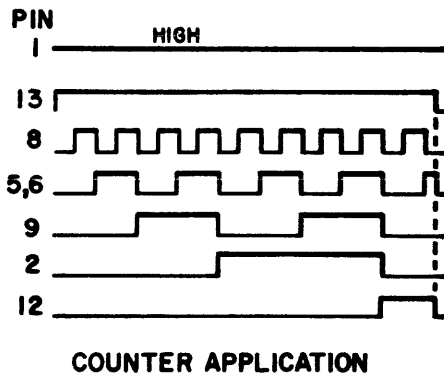
OR



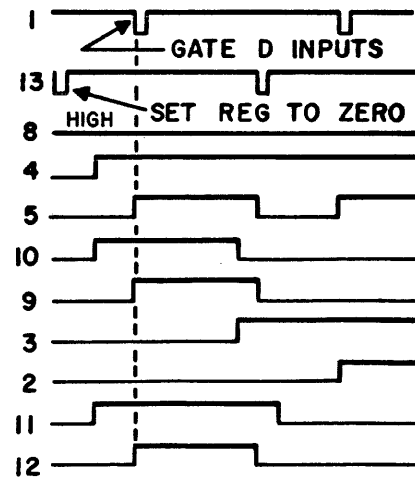
PACKAGE PIN CONFIGURATION

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TRUTH TABLE



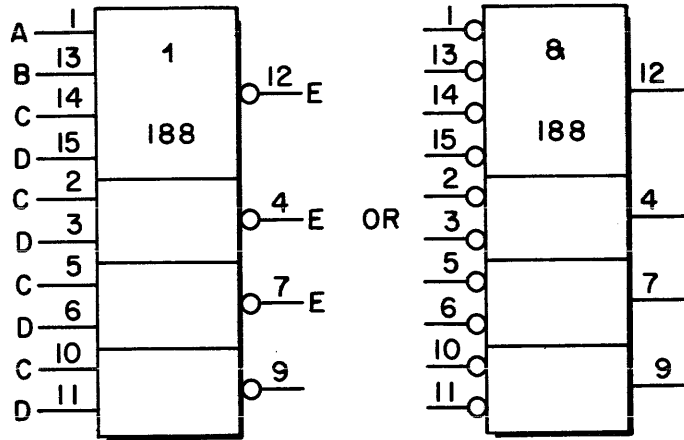
COUNTER APPLICATION



REGISTER APPLICATION

NOTES:

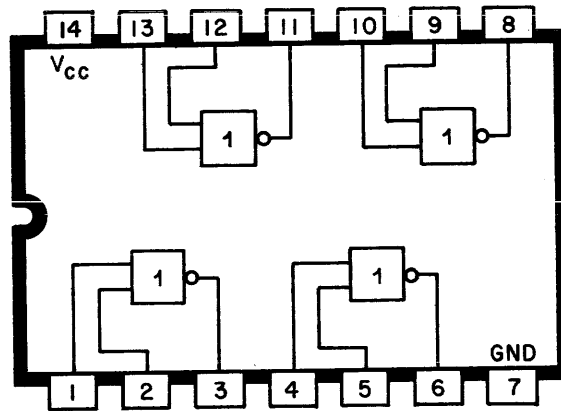
1. Symbol shown as it would appear on logic diagrams.
2. Type 182 manufactured by Texas Instruments (P/N 74197) or Signetics Corporation (P/N 8291).



LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

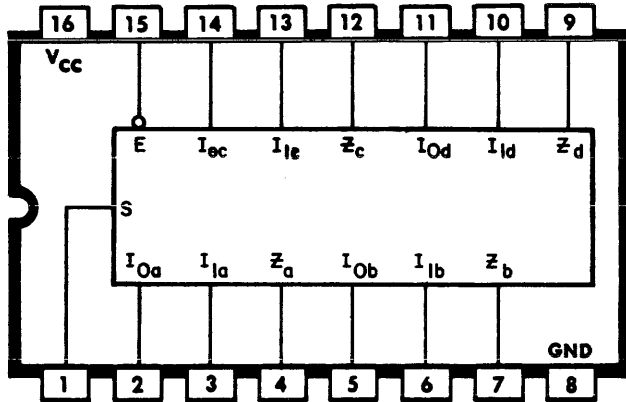
TRUTH TABLE



PACKAGE PIN CONFIGURATION

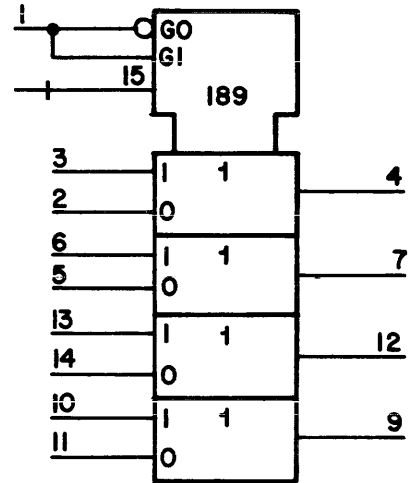
NOTES:

1. Symbol shown as it would appear on logic diagram.
2. Type 188 manufactured by Fairchild Semiconductor (P/N 9015).



PIN	FUNCTION
1	COMMON SELECT INPUT
15	ENABLE (ACTIVE LOW) INPUT
2,3,5,6,10,11,13,14	MULTIPLEXER INPUTS (a,b,c,d)
4,7,9,12	MULTIPLEXER OUTPUTS (a,b,c,d)

PACKAGE PIN CONFIGURATION



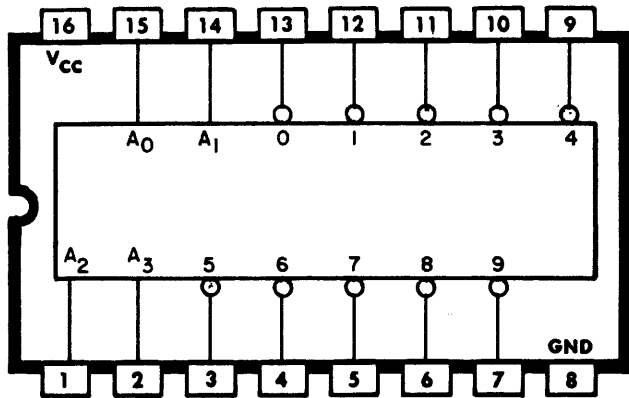
LOGIC SYMBOL

15	1	3,6,13,10	2,5,14,11	4,7,12,9
1	*	*	*	*
0	0	*	1	1
0	0	*	0	0
0	1	1	*	1
0	1	0	*	0
* = NO EFFECT ON OUTPUT				

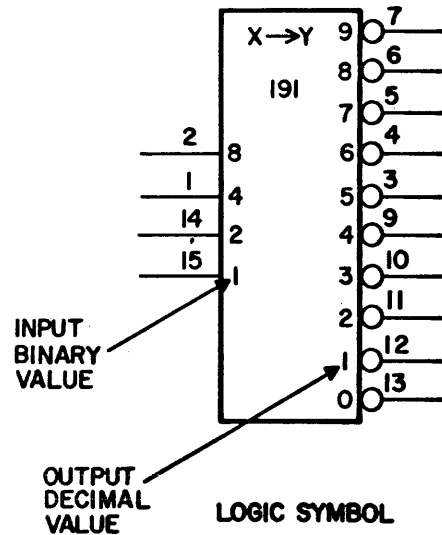
TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagram.
2. Type 189 manufactured by Fairchild Semiconductors (P/N 9322).



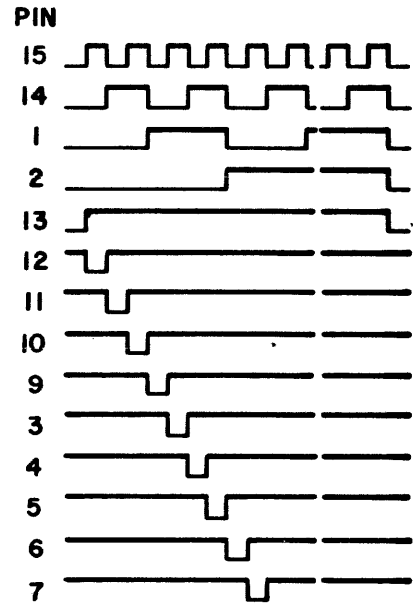
PIN FUNCTION
 1,2,14,15 ADDRESS INPUTS
 3-7,9-13 OUTPUTS (ACTIVE LOW)
PACKAGE PIN CONFIGURATION



INPUT PIN				LO("0") OUTPUT PIN (OTHER OUTPUTS = "1")
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	*

* ALL OUTPUTS ARE HIGH

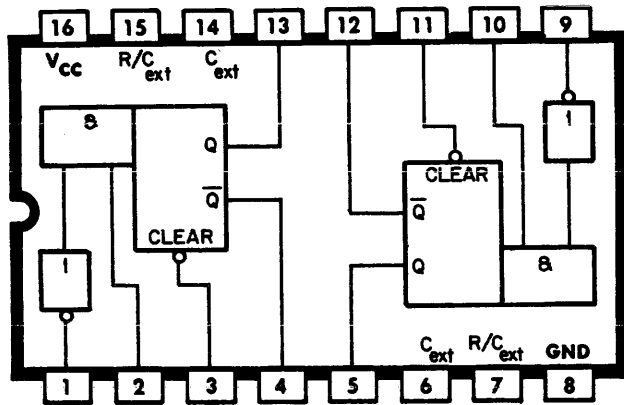
TRUTH TABLE



TIMING SEQUENCE

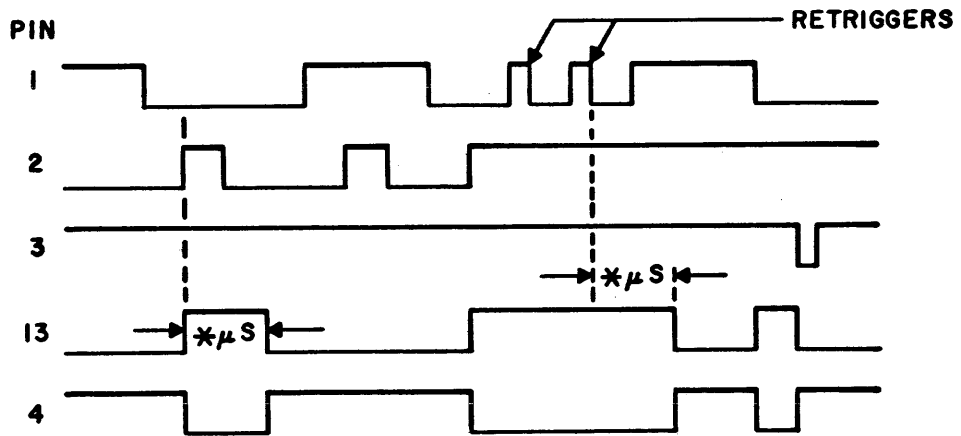
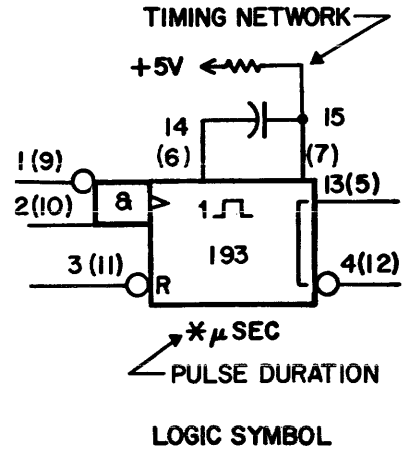
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 191 manufactured by Fairchild Semiconductors (P/N 9301).



PINS 6,7,14,15 ARE USED FOR EXTERNAL TIMING NETWORK

PACKAGE PIN CONFIGURATION

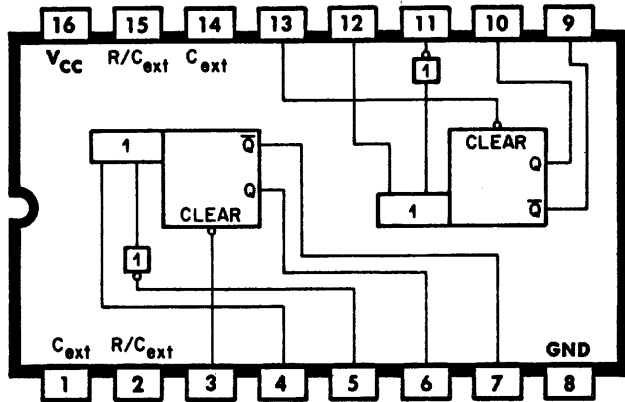


* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK

TIMING SEQUENCE

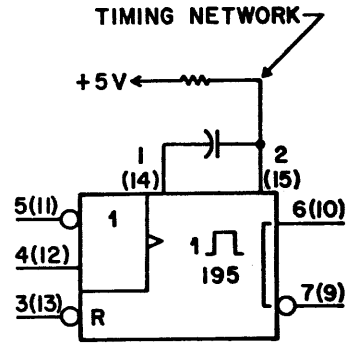
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 193 manufactured by Texas Instruments (P/N 74123).



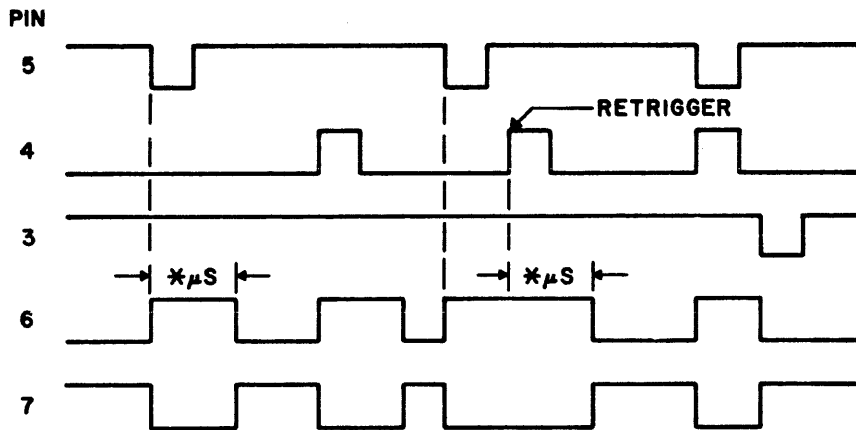
PINS 1, 2, 14, 15 ARE USED FOR EXTERNAL TIMING NETWORK

PACKAGE PIN CONFIGURATION



*μSEC
PULSE DURATION

LOGIC SYMBOL

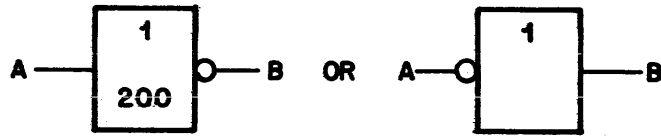


* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK

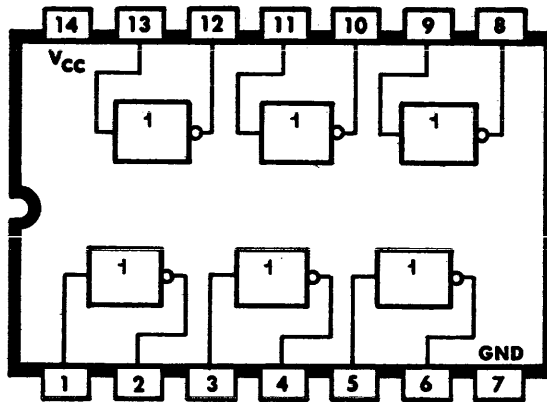
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 195 manufactured by Fairchild Semiconductors (P/N 9602).



LOGIC SYMBOL



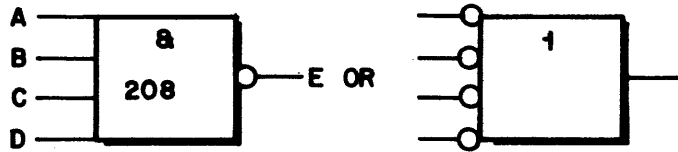
PACKAGE PIN CONFIGURATION



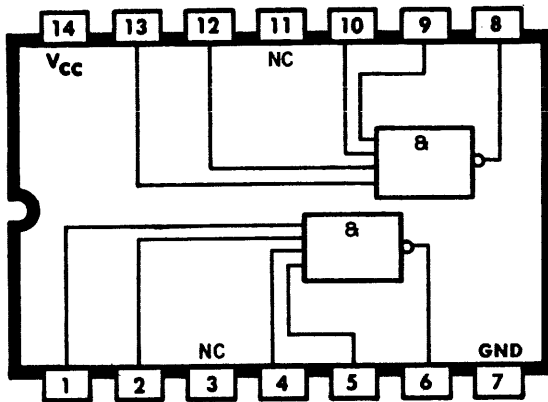
TIMING SEQUENCE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 200 manufactured by Texas Instruments (P/N 7406).
4. The output of each gate is an open collector.



LOGIC SYMBOL



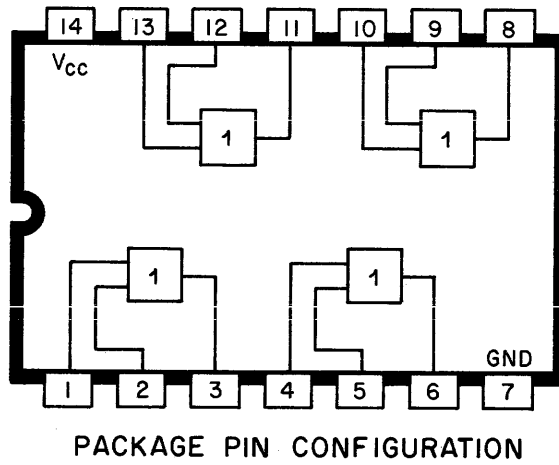
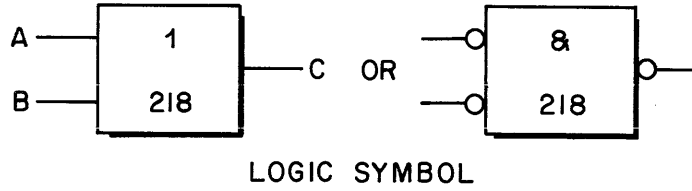
PACKAGE PIN CONFIGURATION

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each NAND gate.
3. Type 208S manufactured by Texas Instruments (P/N 74S20).

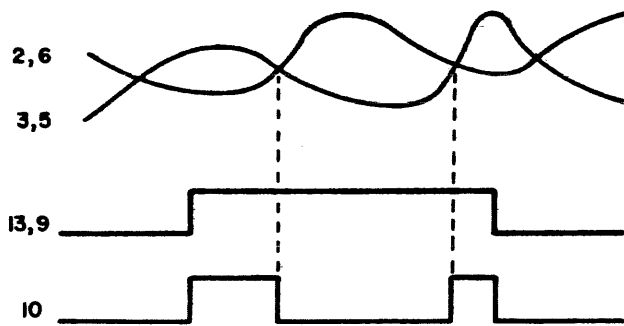
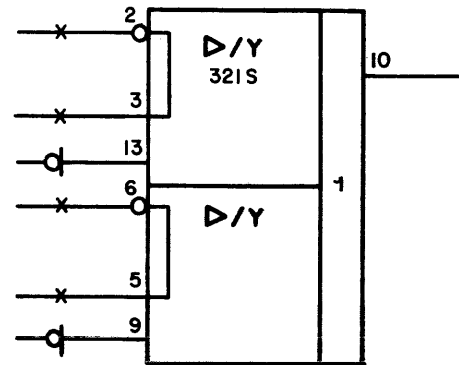
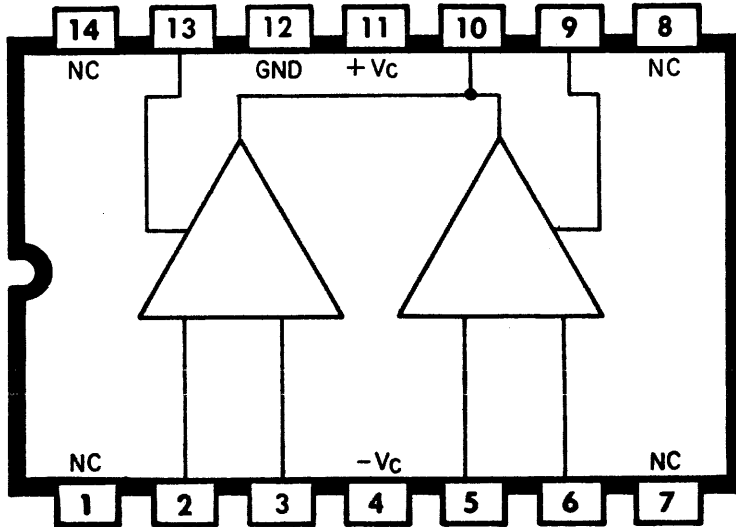


A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

TRUTH TABLE

NOTES:

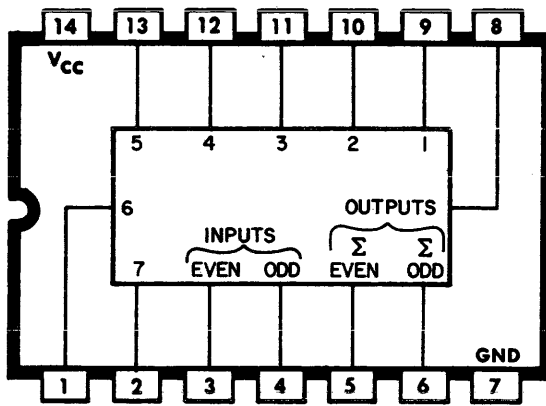
1. Symbol shown as it would appear on logic diagram.
2. Type 218 manufactured by Motorola Semiconductor (P/N 3003).



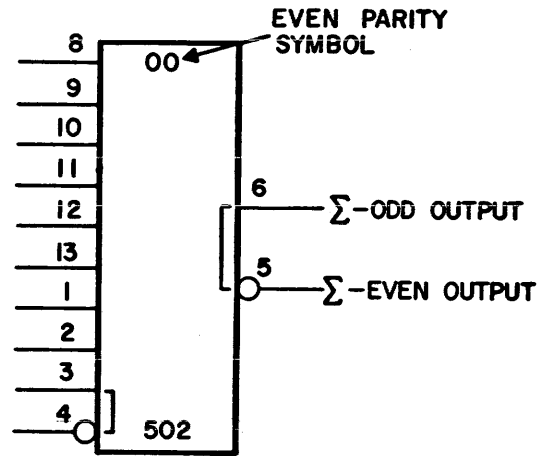
The 321S is a dual comparator. Output (pin 10) is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 321S manufactured by Transistron Electron (P/N TSC5711).



PACKAGE PIN CONFIGURATION



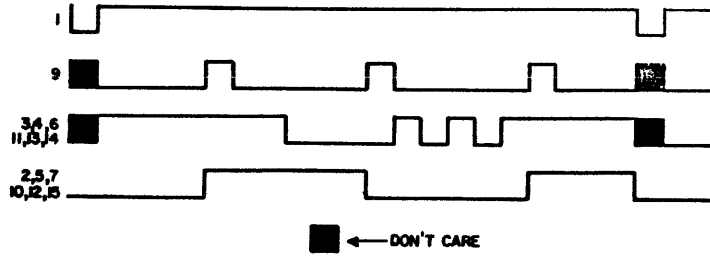
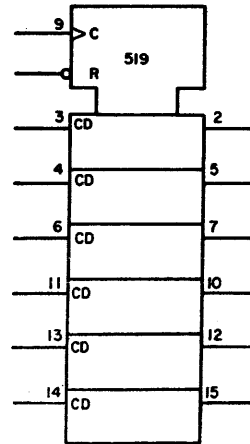
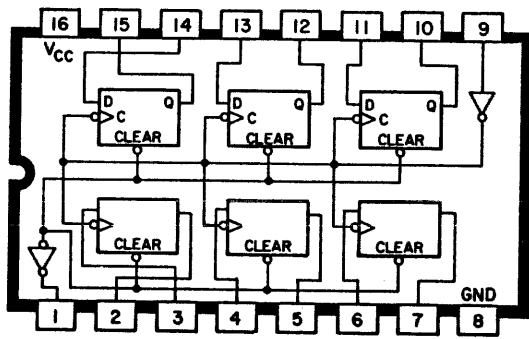
LOGIC SYMBOL

Σ OF 1's AT PINS 1,2,8 THRU 13	INPUTS		OUTPUTS	
	PIN 3	PIN 4	PIN 5	PIN 6
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
EVEN OR ODD	1	1	0	0
EVEN OR ODD	0	0	1	1

TRUTH TABLE

NOTES:

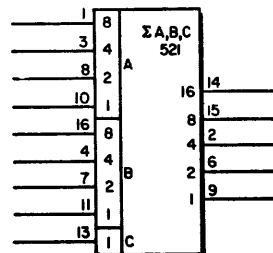
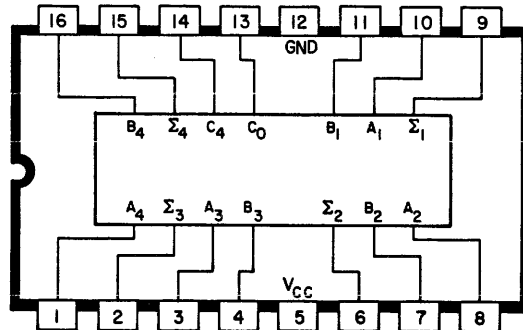
1. Symbol shown as it would appear on logic diagrams.
2. Type 502 manufactured by Texas Instruments (P/N 74180).



NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 519 manufactured by Texas Instruments (P/N 74174).

INPUT								OUTPUT											
				WHEN $C_0=0$				WHEN $C_0=1$											
				WHEN $C_2=0$				WHEN $C_2=1$											
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2	A_3	B_3	A_4	B_4	Σ_3	Σ_4	C_4	Σ_3	Σ_4	C_4
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

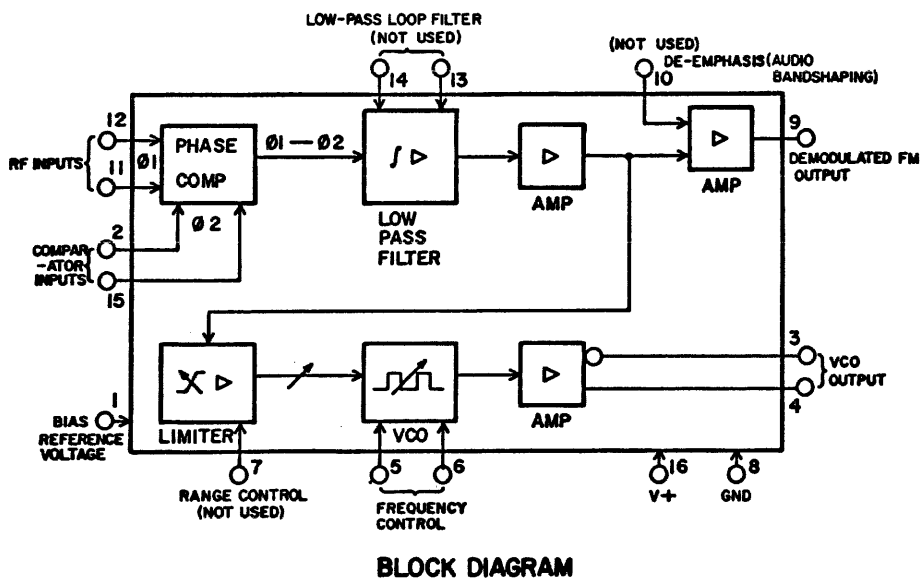
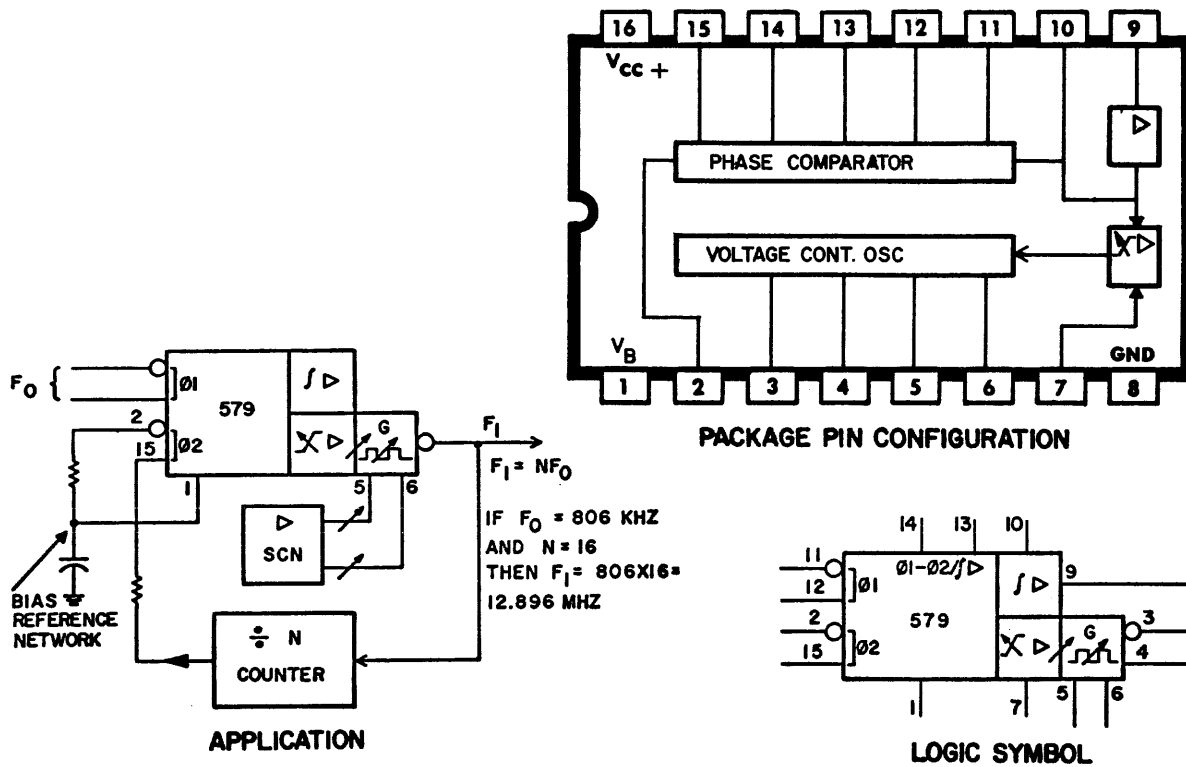


The 521 circuit type is a 4-bit binary full adder. A is added to B with C (a carry) added in at the least significant digit.

Input conditions at A_1 , B_1 , A_2 , B_2 , and C_0 are used to determine outputs E_1 , E_2 , and the value of an internal carry C_2 (not shown). The values at C_2 , A_3 , B_3 , A_4 , and B_4 are then used to determine outputs E_3 , E_4 , and C_4 .

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 521 manufactured by Tecas Instruments (P/N 7483).



NOTES:

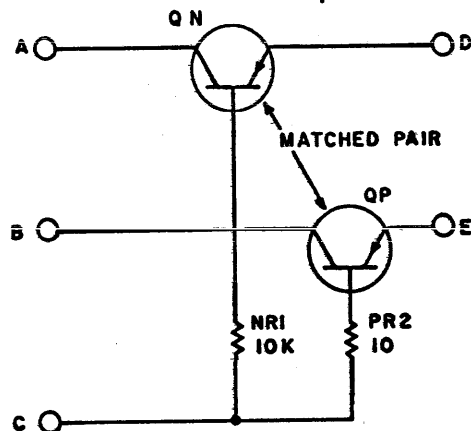
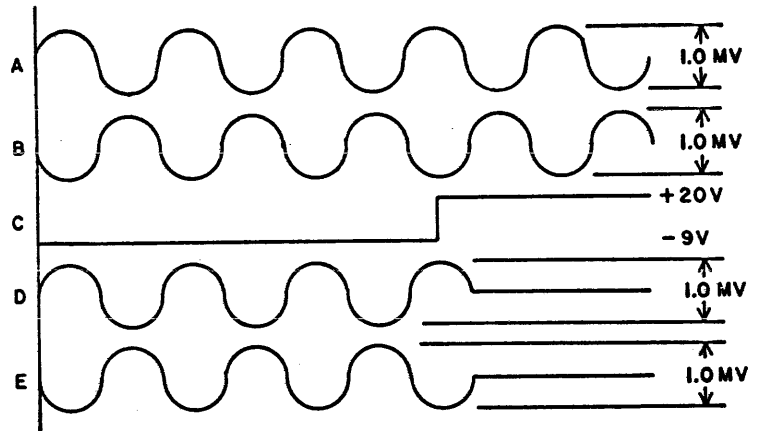
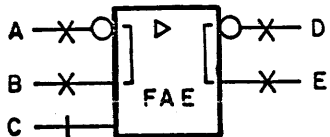
1. Symbol shown as it would appear on logic diagrams.
2. Type 579 manufactured by Signetics Corporation (P/N NE562).

SECTION 3

DISCRETE COMPONENT CIRCUIT DESCRIPTIONS

DISCRETE CIRCUIT EFFECTIVITY INDEX

Circuit Type	Revision Date	Circuit Type	Revision Date	Circuit Type	Revision Date
FAE	3-6-72	HBI	10-13-72	SCC	6-1-72
FAF	3-6-72	HBJ	10-13-72	SCD	3-6-72
FAG	4-20-72	HCA	3-6-72	SCE	4-20-72
FAH	9-29-72	HCB	3-6-72	SCG	6-12-72
FBH	9-29-72	HCE	3-6-72	SCL	6-12-72
GJB	3-6-72	HCF	3-6-72	SCM	3-6-72
GJC	3-6-72	HCK	3-6-72	SCN	3-6-72
GJF	3-6-72	HCL	3-6-72	UBD/E/F/H	9-29-72
GJK	6-1-72	HCP	3-6-72	UBG	3-6-72
GKA/GKB	3-6-72	HCQ	3-6-72	UC-	3-20-73
GKC	3-6-72	HCU	6-12-72	UEB	3-20-73
GKD	3-6-72	HJD	3-6-72	VAF	3-6-72
GKF	3-6-72	HJE	3-6-72	VHI	3-6-72
HAK	9-29-72	ICB	3-6-72	VHJ	3-6-72
HAL/HAM	3-6-72	ICC	3-6-72	VHK	3-6-72
HAN	3-6-72	JAG	9-29-72	VHL	4-20-72
HAP	4-20-72	JAK	9-29-72	VHM	3-6-72
HAQ	4-20-72	JAM	9-24-73	VHP	3-6-72
HAR	6-12-72	LCF	3-6-72	VHQ	3-6-72
HAS/HAT	3-6-72	MAF/MAH	6-1-72	VHR	3-6-72
HAU	3-6-72	QDE	3-6-72	VKK	3-20-73
HAV	3-6-72	QEH	3-6-72	VKN	3-6-72
HAW	3-6-72	QEJ	3-6-72	VKM	3-6-72
HAX	9-29-72	QEK	3-6-72	XAF	6-12-72
HBA	9-29-72	QEL	3-6-72	XAG	3-6-72
HBB	9-29-72	QEM	9-29-72	XAH	3-6-72
HBD	6-12-72	QGD	3-6-72		
HBE	9-29-72	RCB	3-6-72		
		SAA	12-1-72		

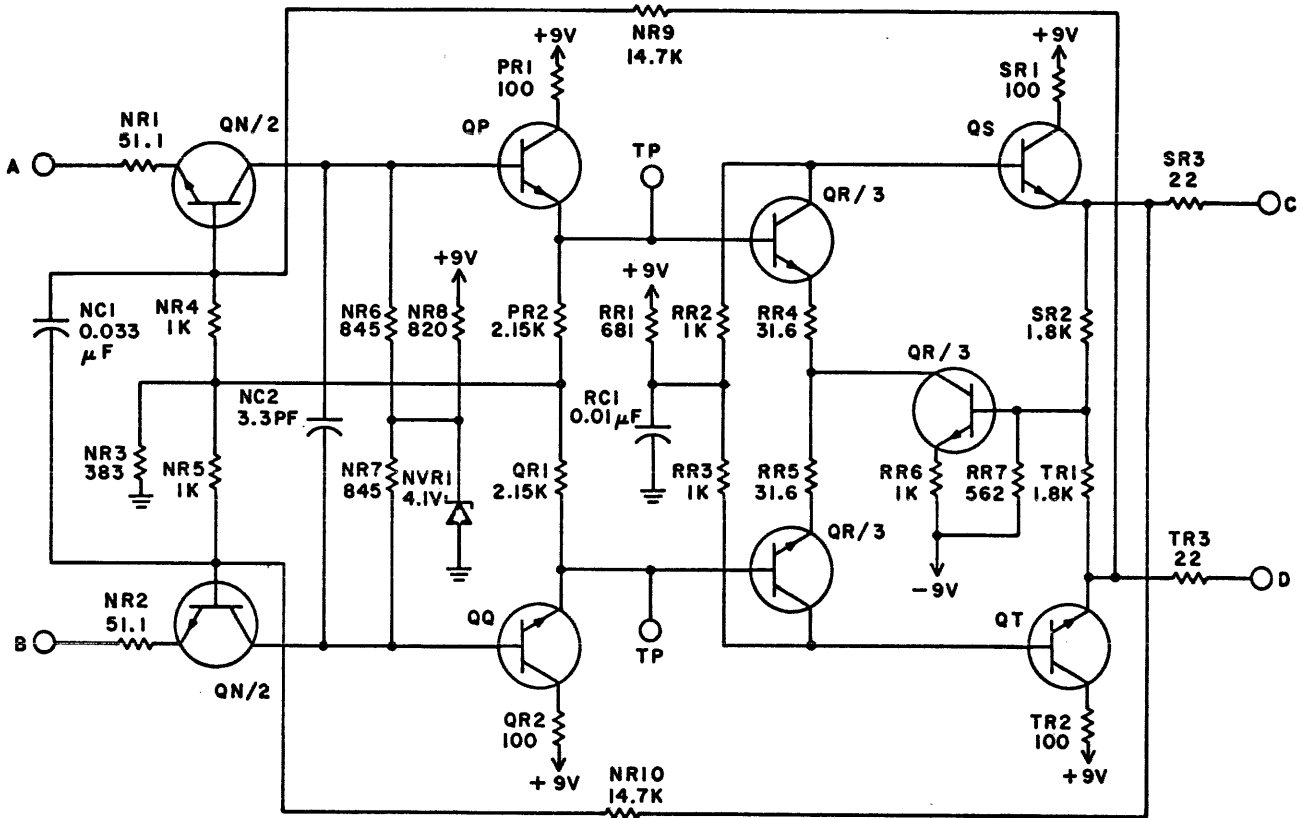
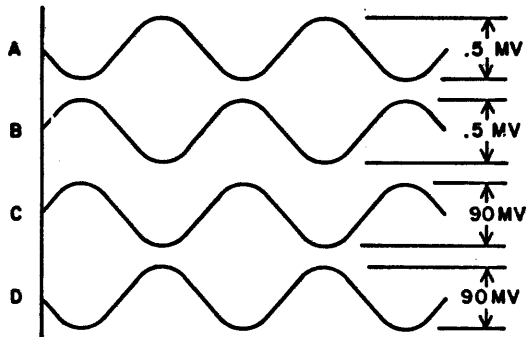
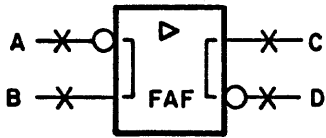


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J10

GATED AMPLIFIER - FAE

The FAE circuit consists of two matched transistors acting as low level analog gates. Inputs A and B receive the output of differential windings of a read head. Output points D and E drive the input of a low level amplifier such as an FAF. The outputs are gated by input C. When point C is at -9 volts, QN and QP turn on enabling data to flow from points A and B to ~~C~~ D and E respectively. At +20 volts on point C QN and OP turn off inhibiting the output.



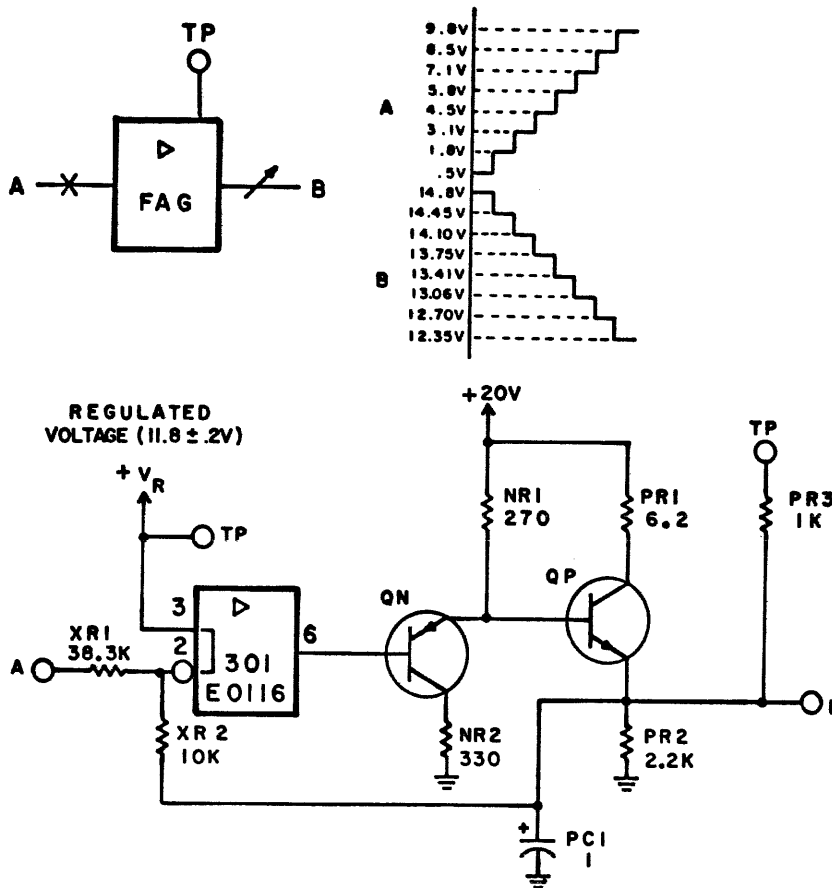
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J11

AMPLIFIER - FAF

The FAF circuit is a low level amplifier that amplifies analog read signals. Points A and B are typically connected to Gated Amplifiers which provides biasing for the common base input stage.

The amplifier consists of two stages, common base first stage (QN matched pair) and common emitter second stage (QR matched pair) with emitter follower outputs (QS and QT) for low output impedance. The gain of the first stage is dependent upon the signal source resistance and is approximately 9 with 9750 type heads as a signal source. The gain of the second stage is approximately 20, therefore, the overall amplifier gain is approximately 180.

DC feedback is provided by NR9, NR10, PR2 and QR1 to the base circuitry of the QN matched pair. This feedback helps to stabilize the DC operating points in the circuit. Capacitor NC1 provides a lower impedance path between bases of the input transistors which presents a low amplifier input impedance for AC signals over the passband of the amplifier.



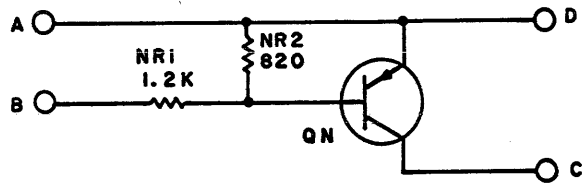
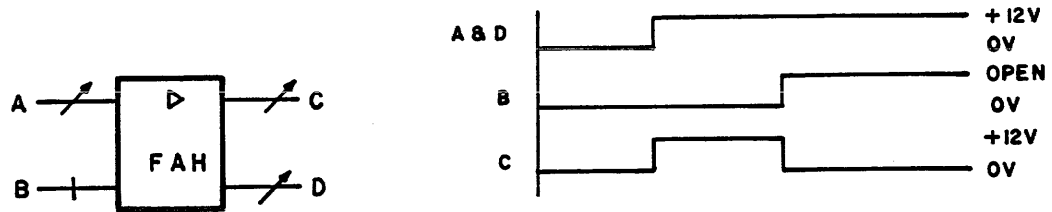
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J12B

Controlled Voltage Source - FAG

The FAG circuit is a controlled voltage source providing a controlled voltage to Write Driver - JAG.

The circuit consists of an operational amplifier and a two transistor buffer extends the output current capability. The transistor buffer is included in the negative feedback circuit to reduce the output voltage change due to temperature variation.

The output at B (V_B) is related to the two inputs V_R and $A(V_A)$ by the following expression:
$$V_B = V_R \left(1 + \frac{XR2}{XR1} \right) - \frac{XR2}{XR1} V_A$$

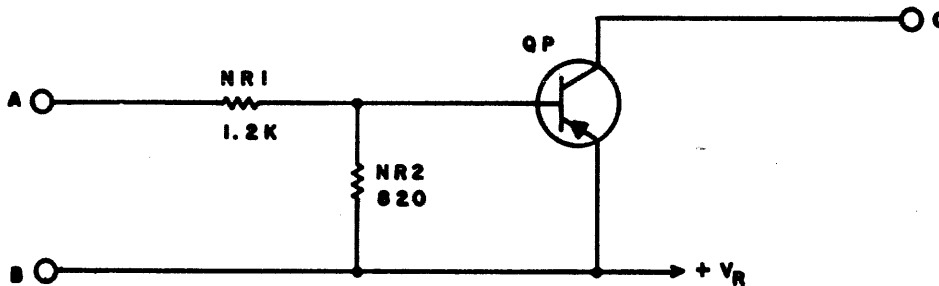
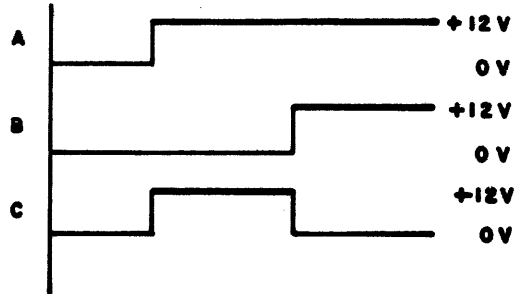
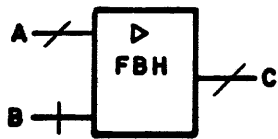


NOTE.
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J13

VOLTAGE SWITCH - FAH

The FAH circuit is a voltage switch which transfers a voltage at point A to point C when QN is turned on by the proper voltage condition at point B.

In a typical circuit the voltage at point A (V_a) is +12 volts. With 0 volts applied to point B ($V_b = 0$ volts), transistor QN turns on and point C goes to +12 volts ($V_c = +12$ volts). When point B is open (as when connected to an open collector IC that is turned off) QN will turn off and point C will be disconnected from point A and return to any quiescent potential in the circuit it is connected to.



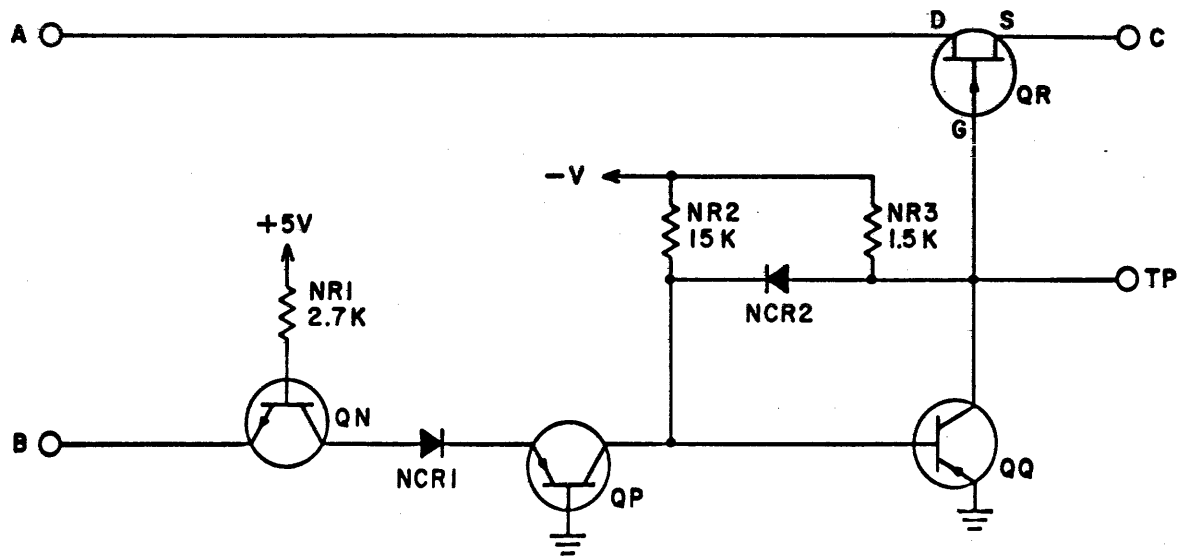
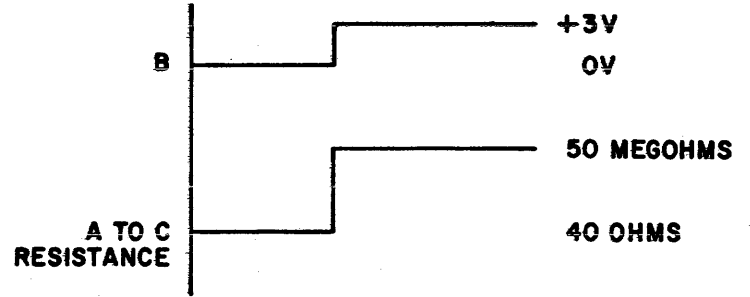
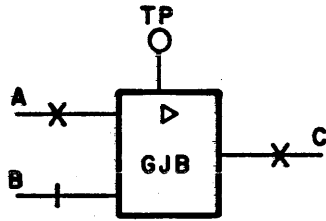
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J114

VOLTAGE SWITCH - FBH

The FBH is a voltage switch which transfers a voltage at input B to output C when QP is turned on by the proper voltage condition at input A.

In a typical circuit the voltage at input B is +12 volts. With 0 volts applied to input A, transistor QP turns on and output C goes to +12 volts. When input B is open (as when connected to an open collector IC that is turned off) QP will turn off and output C will be disconnected from input B and return to any quiescent potential in the circuit it is connected to.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

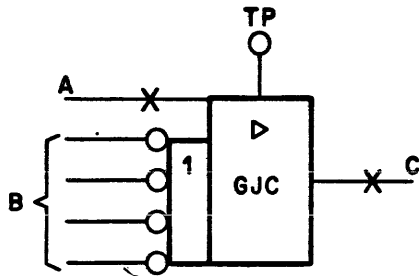
6T182

GATED ANALOG CLAMP - GJB

The GJB circuit functions to turn QR (an N channel junction field effect transistor) on when a logical 0 is applied at input B and to turn QR off when a logical 1 is applied at input B.

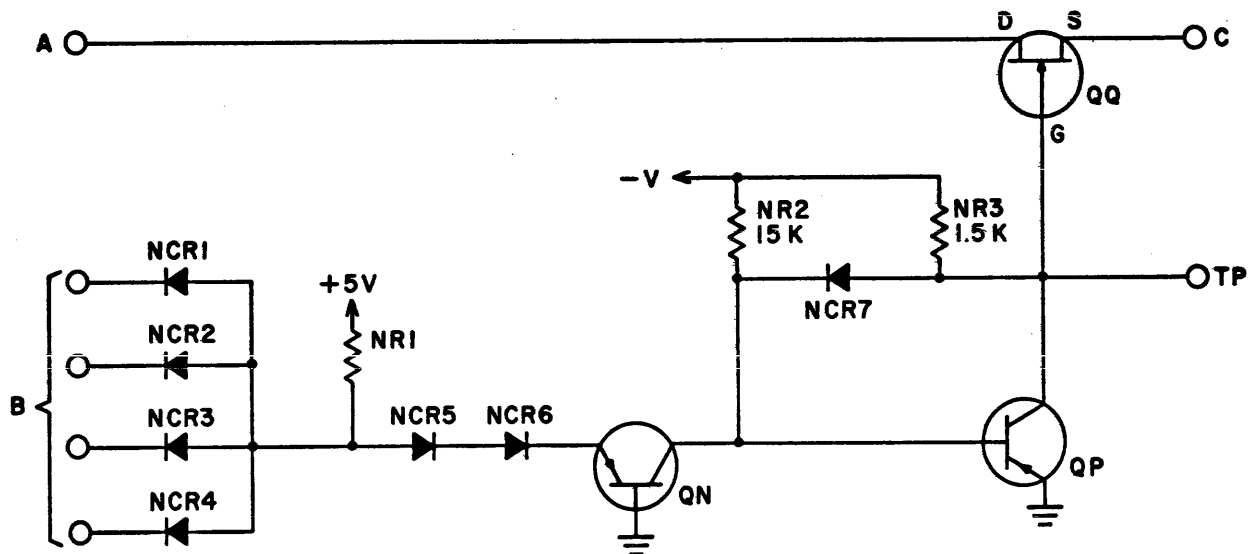
In actual application input A is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal C is connected to the output of the operational amplifier. When QR turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QR are 40 ohms and 50 megohms respectively.



IF ANY INPUT B EQUALS 0 VOLTS,
THE A TO C RESISTANCE EQUALS 40 OHMS.

IF ALL INPUT B'S EQUAL +3 VOLTS,
THE A TO C RESISTANCE EQUALS 50 MEGOHMS.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

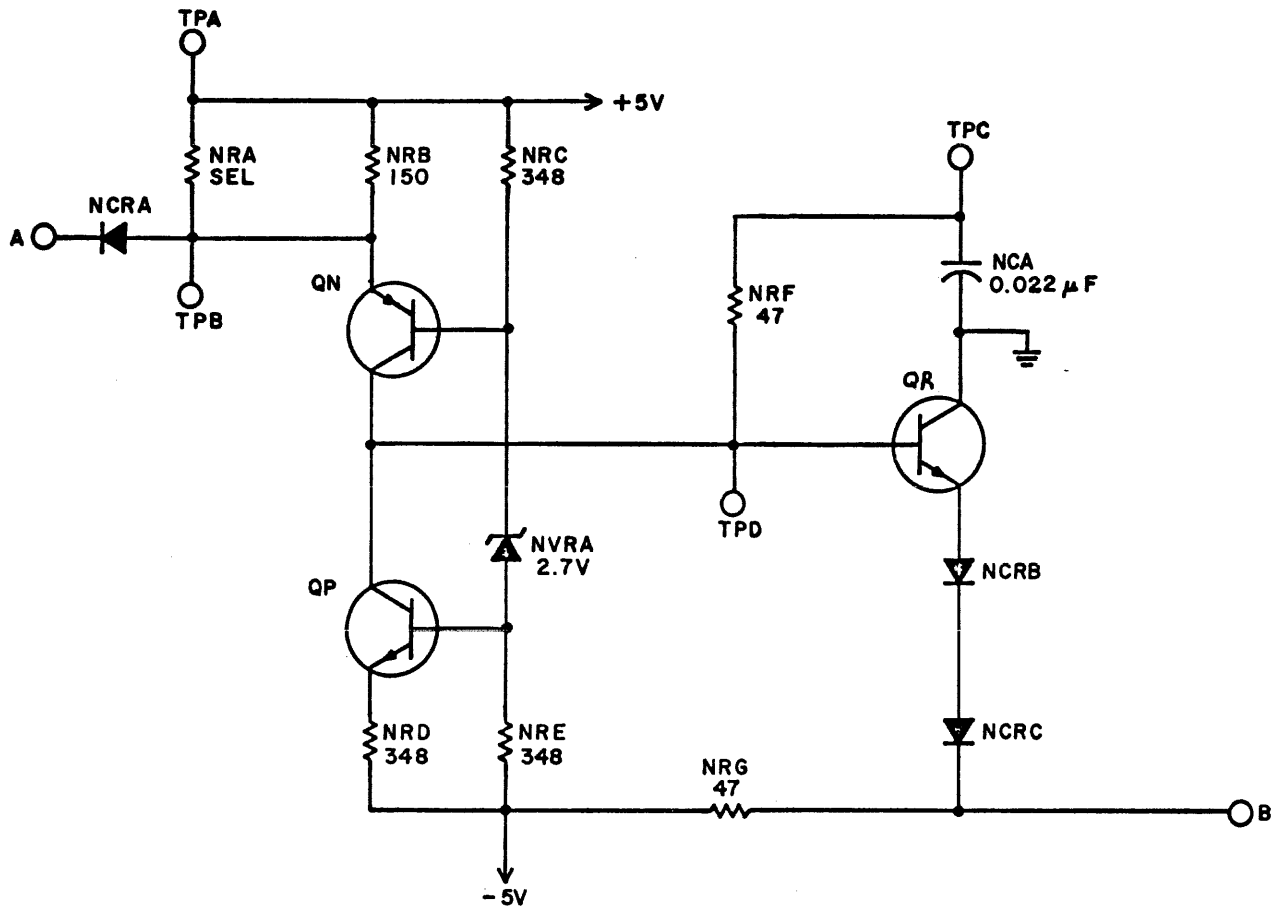
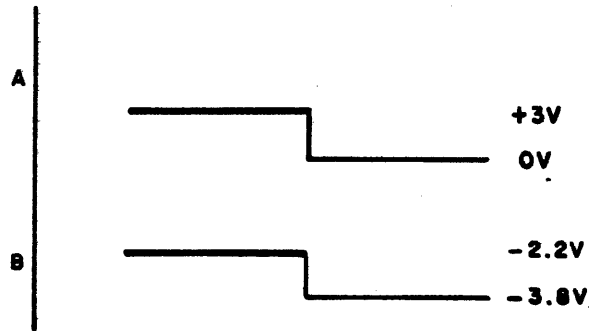
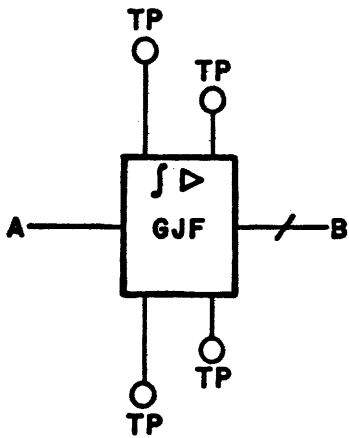
GT133

MULTIPLE GATE ANALOG CLAMP - GJC

The GJC circuit functions to turn QQ (an N channel junction field effect transistor) on when a logical 0 is applied at any of the B inputs and to turn QQ off when all of the B inputs are at a logical 1.

In actual application input A is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal C is connected to the output of the operation amplifier. When QQ turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QQ are 40 ohms and 50 megohms respectively.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7855

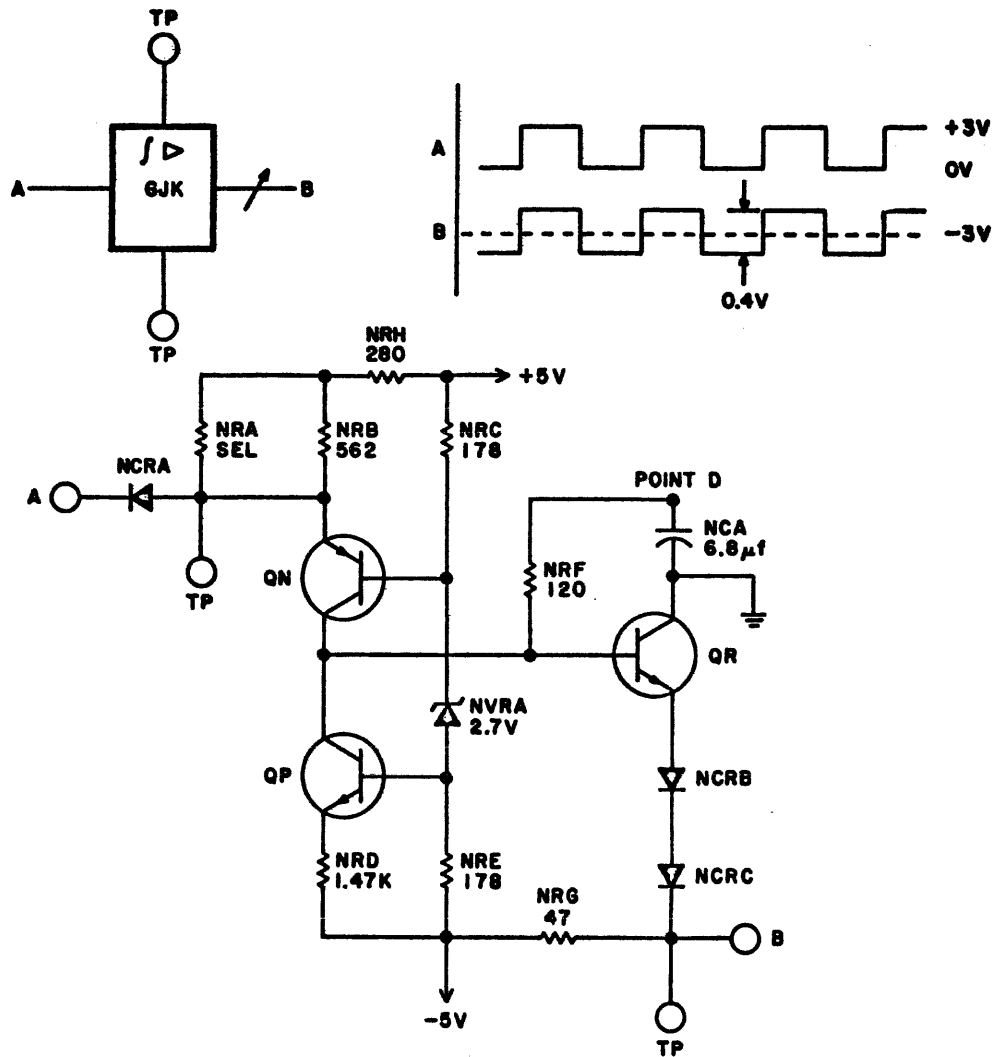
LOW PASS FILTER AND AMPLIFIER – GJF

The GJF circuit consists of a bidirectional current pump, a filter, and a level shifter. The circuit converts TTL input signals from a comparator circuit and integrates these signals to produce a dc voltage level at TPC. Because of the phase locked oscillator closed loop, the current pump drives the dc level at TPC to reach a steady state when the signal at input A is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency causes a change in voltage at TPC.

NRC, NVRA, and NRE form a reference voltage divider for the current pump. NRD and QN is the negative going current sink. This sinks a current of approximately 7.5 ma continually. NCRA, NRA, NRB, and QN form a switchable current source of approximately 15 ma. When a square wave of TTL logic levels is applied to input A, NCA alternately is charged and discharged by 7.5 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times, therefore, the voltage at TPC has very little ac component in it.

Resistor NRF generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRF and the currents from the bidirectional pump. The net result at TPD is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QR, NCRB, NCRC, and NRG form a buffer and level shifting circuit. They shift the waveform at TPD negatively to a level appropriate for controlling voltage controlled oscillator.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J170

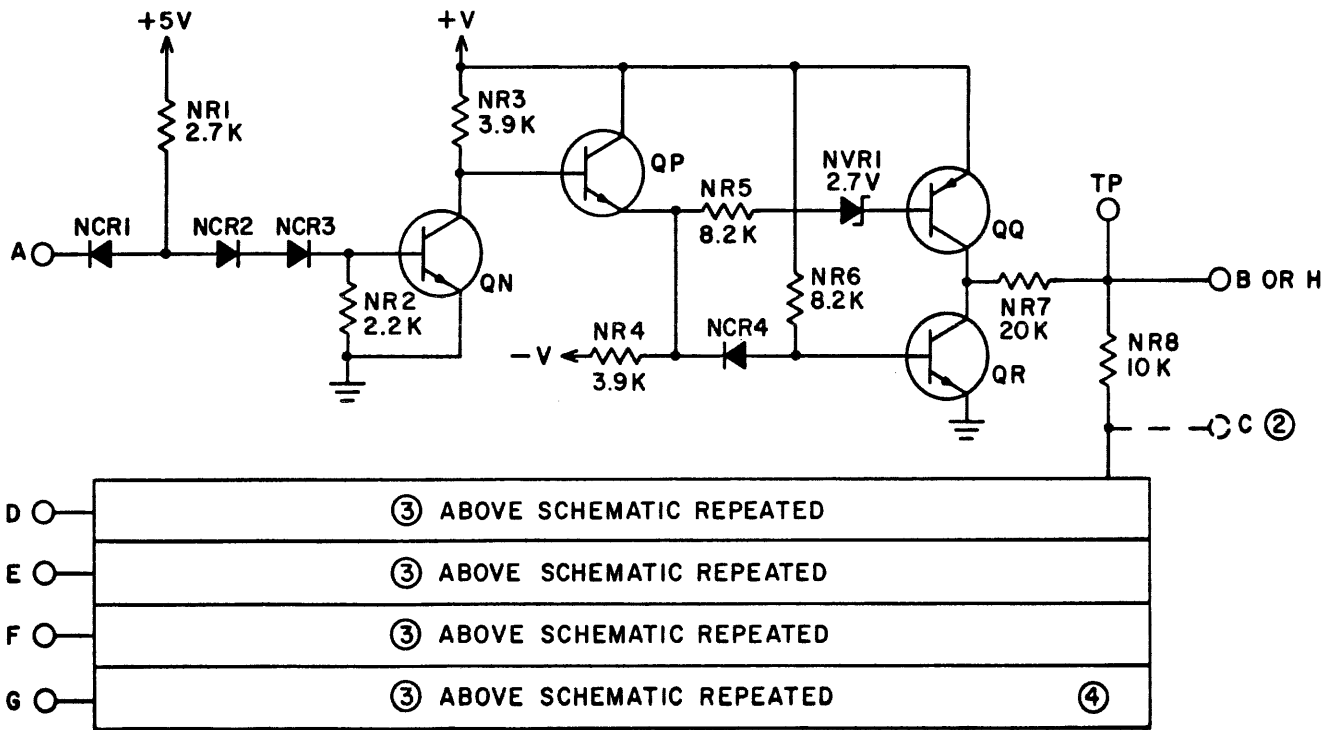
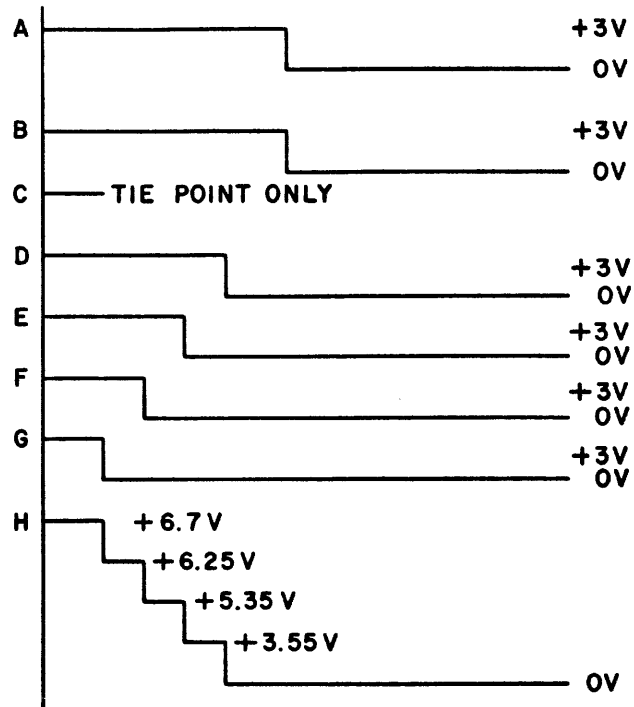
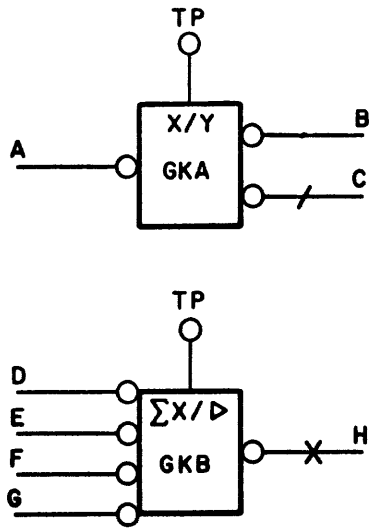
LOW PASS FILTER AND AMPLIFIER - GJK

The GJK circuit consists of a bidirectional current pump, a filter, and a level shifter. The circuit converts TTL input signals from a comparator circuit and integrates these signals to produce a dc voltage level at output B. Because of the phase locked oscillator closed loop, the current pump drives the dc level at point D to reach a steady state when the signal at input A is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency (duty cycle) causes a change in average ac voltage across NRF.

NRC, NVRA, and NRE form a reference voltage divider for the current pump. NRD and QP is the negative-going current sink. This sinks a current of approximately 2 ma continually. NCRA, NRA, NRB, and QN form a switchable current source of approximately 15 ma. When a square wave TTL logic level is applied to input A, NCA alternately is charged and discharged by 5 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times, therefore, the voltage across NCA has very little ac component in it.

Resistor NRF generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRF and the currents from the bidirectional pump. The net result at the base of QR is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QR, NCRB, NCRC, and NRG form a buffer and level shifting circuit. They shift the waveform at the base of QR negatively to a level appropriate for voltage control oscillator frequency.



D	③ ABOVE SCHEMATIC REPEATED
E	③ ABOVE SCHEMATIC REPEATED
F	③ ABOVE SCHEMATIC REPEATED
G	③ ABOVE SCHEMATIC REPEATED ④

NOTES: 1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.

② APPLICABLE TO GKA ONLY.

③ APPLICABLE TO GKB ONLY.

④ NR8 IN THIS SECTION IS 20K WITH LOWER END TO GROUND.

6T155

LEVEL TRANSLATOR - GKA AND DIGITAL TO ANALOG CONVERTER - GKB

The GKA and GKB circuits when used together comprise a 5-bit D/A converter. The GKB circuit used singly is a 4-bit converter.

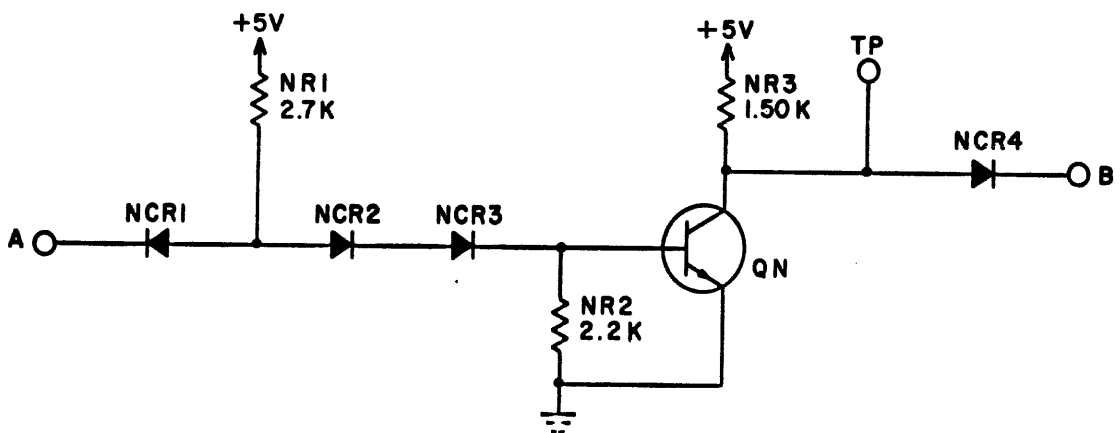
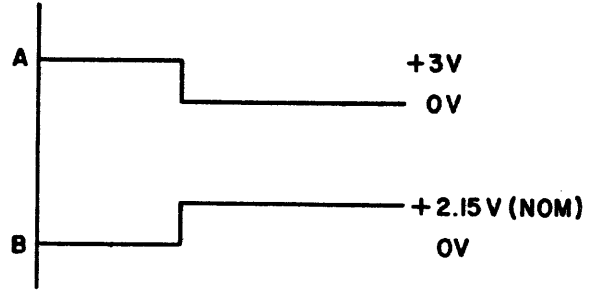
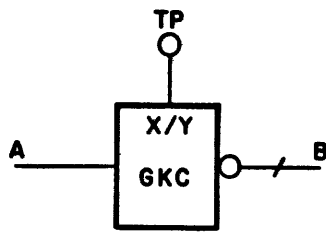
The GKB consists of four voltage switches and a 4-bit R-2R D/A ladder network. Each voltage switch circuit applies positive voltage to the related ladder input when its input is a logical 1. A voltage switch applies ground to the related ladder network input when its input is a logical 0.

In the GKB circuit, the digital inputs G, F, E, and D are ordered from least to most significant. When all digital inputs are "1's", the voltage at H is +6.7 v (assuming a 10k ohm load is provided by the following circuit). When all digital inputs are "0's" the analog output is 0v (except for a +6 mv, max., dc offset). The analog output for an increase of one in the digital input code is +446 mv, nominal.

QN and QP operate as a saturated switch and an emitter follower, respectively, in the voltage switch circuit. QQ and QR operate as low offset saturated switches, only one of which is on at a time.

The R-2R D/A ladder has a resistance of 10k ohms from any node to ground and divides by two the voltage at the next lower in significant note.

The GKA circuit is identical to one stage of the GKB.



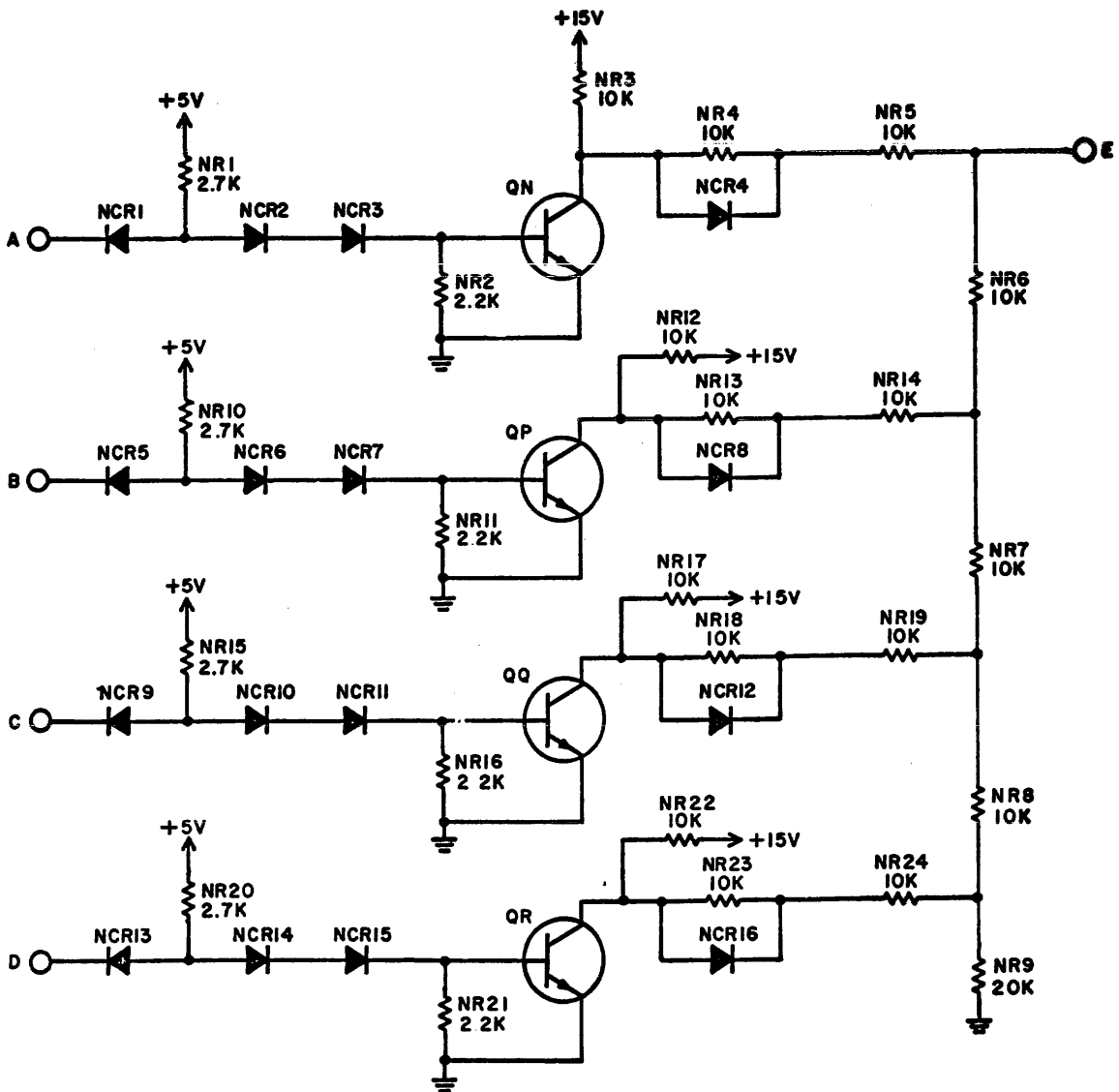
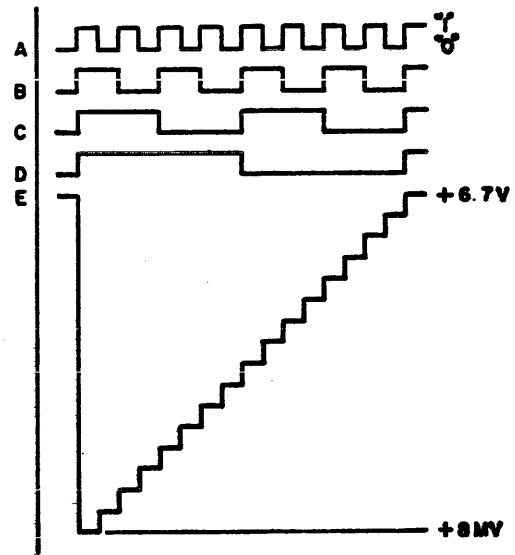
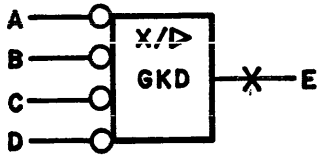
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

67136

LEVEL TRANSLATOR - GKC

The GKC circuit converts a logical 0 to a +2.15 (nominal) level used to inject a current signal into the summing point of an operational amplifier. Typically a resistor is connected between point B and the operational amplifier summing point to establish the magnitude of this current.

When a logical 1 is present at input A, transistor QN saturates, the output diode NCR4 shuts off, and output B drops to 0 volts removing the current to the operational amplifier summing point.



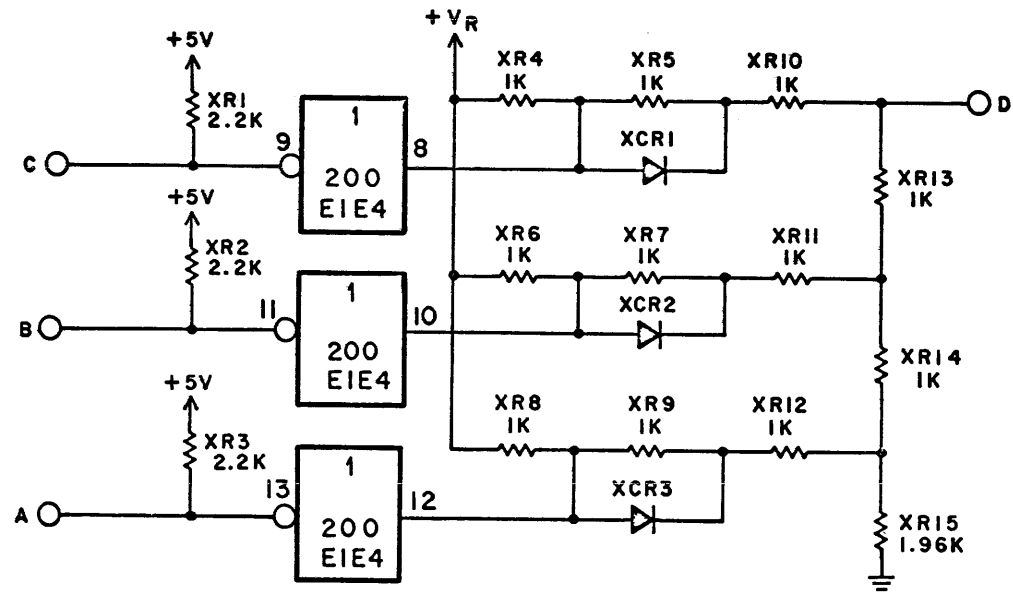
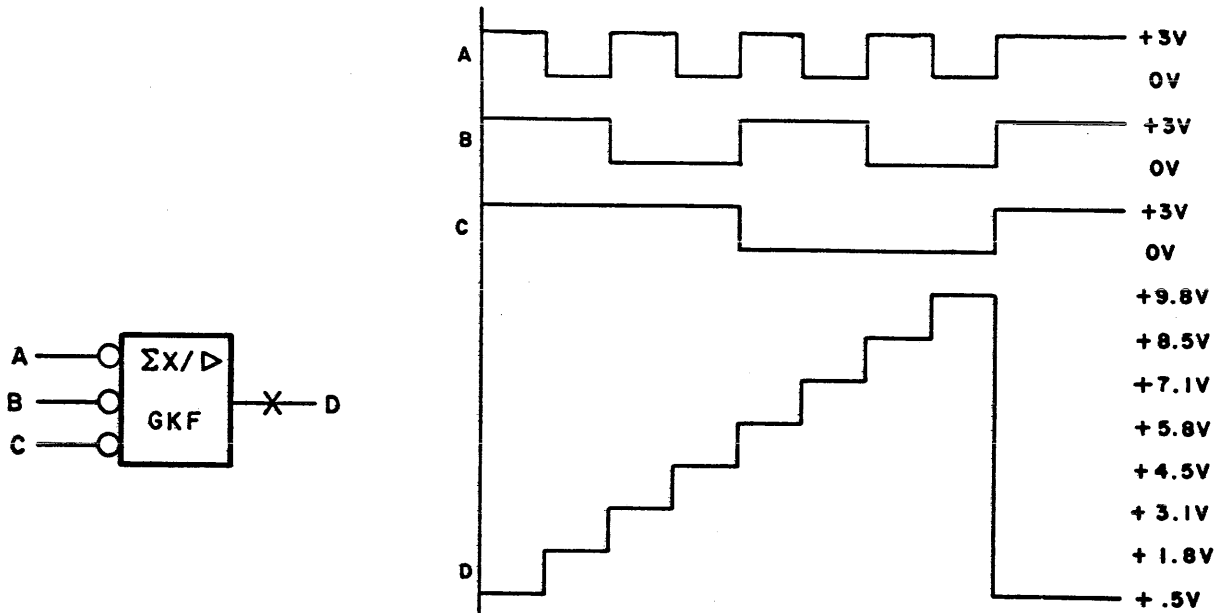
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7963

DIGITAL TO ANALOG CONVERTER – GKD

The GKD circuit is a 4-bit digital to analog converter. The circuit consists of four voltage switches and a resistance ladder network.

The digital inputs A, B, C, and D are ordered from most to least significant. When all digital inputs are "0's", the output at E is approximately +6.7V. When all digital inputs are "1's", the output goes to approximately +8 mv. The analog output increases approximately 420 mv for an increase of one in the digital code.



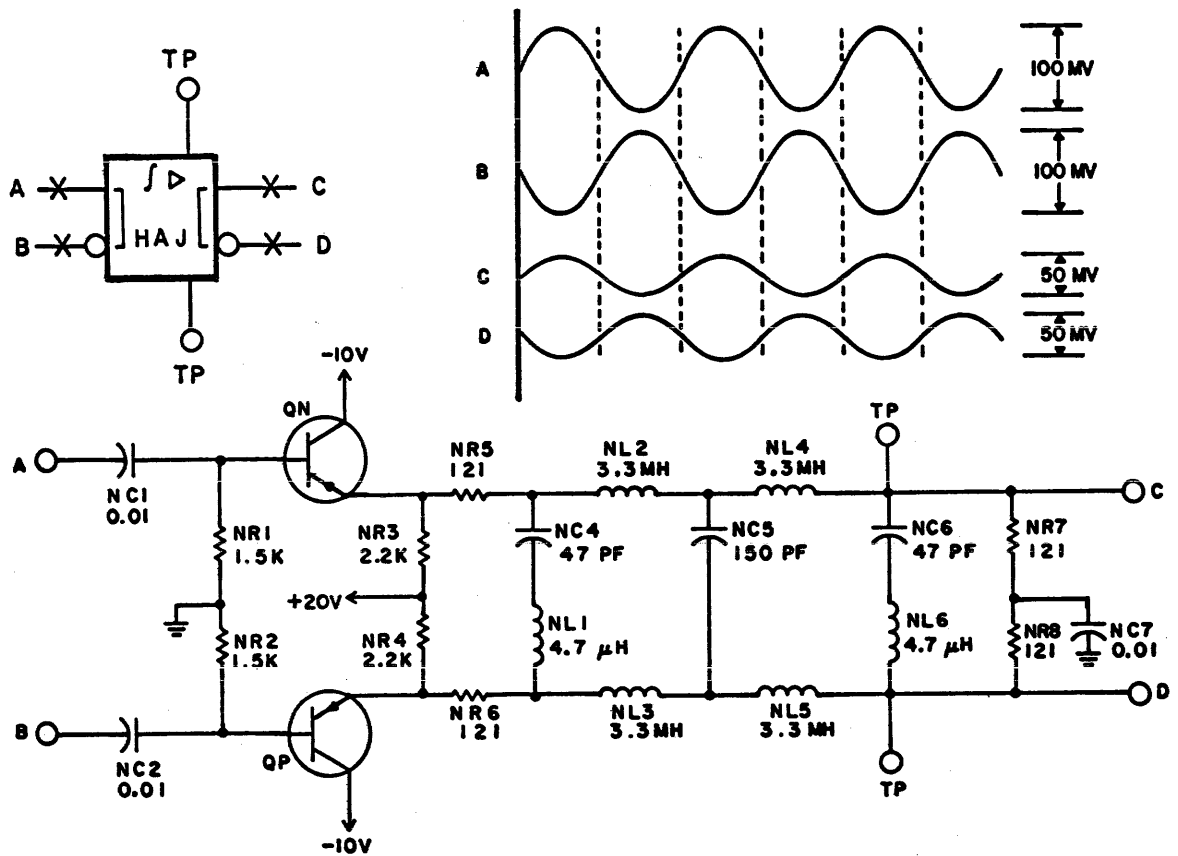
NOTE:
 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J14

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_R determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_R is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

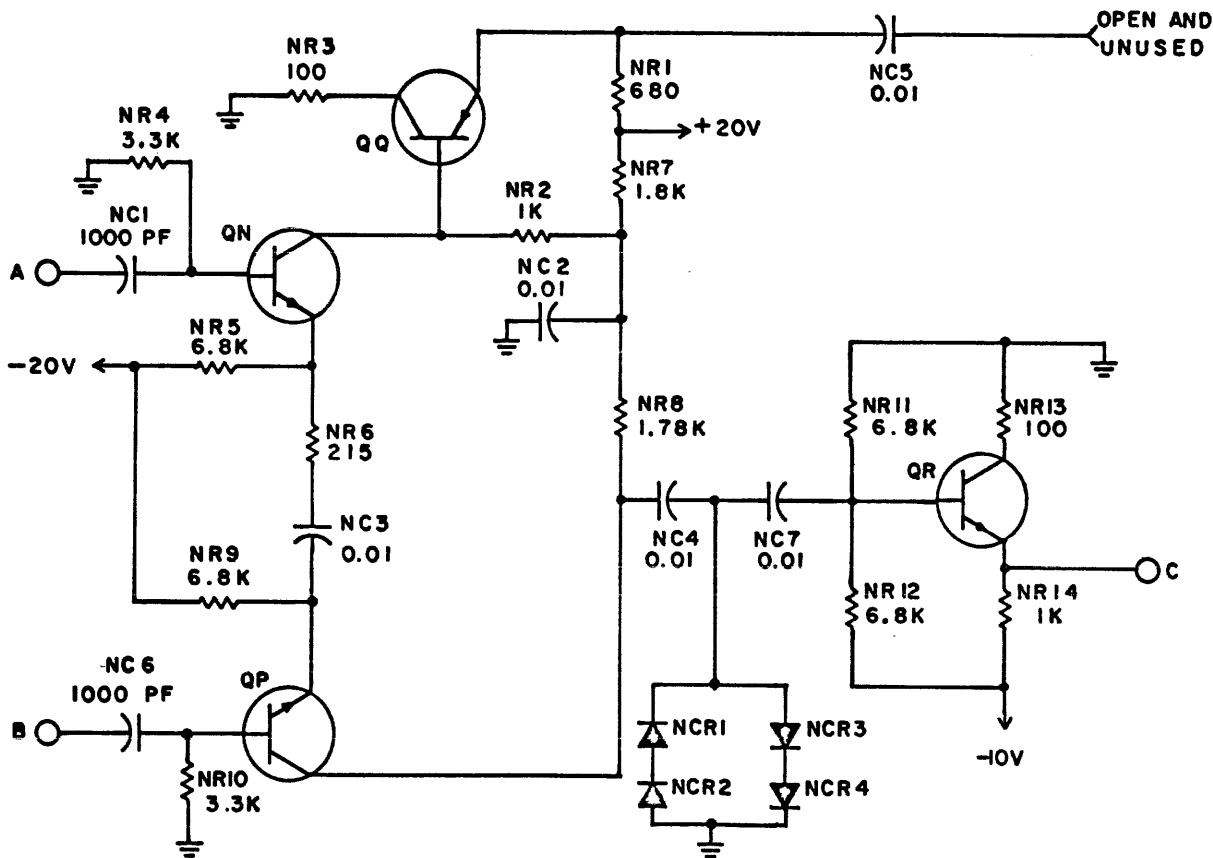
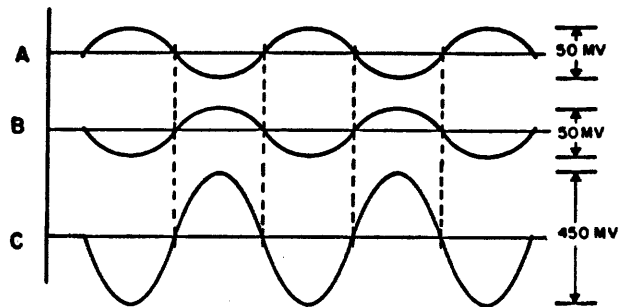
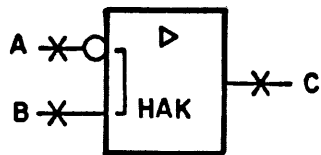
7J18A

Differential Low Pass Filter - HAJ

The HAJ circuit is a differential low pass filter buffered on the input by emitter followers.

The upper cutoff frequency of the filter is approximately 8.5 MHz at -3 db. Attenuation above the cutoff frequency is approximately -36 db/octave.

Input capacitors NC1 and NC2 in conjunction with resistor NR1 and NR2 give the circuit a low frequency cutoff of about 10 KHz at -3 db.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J16A

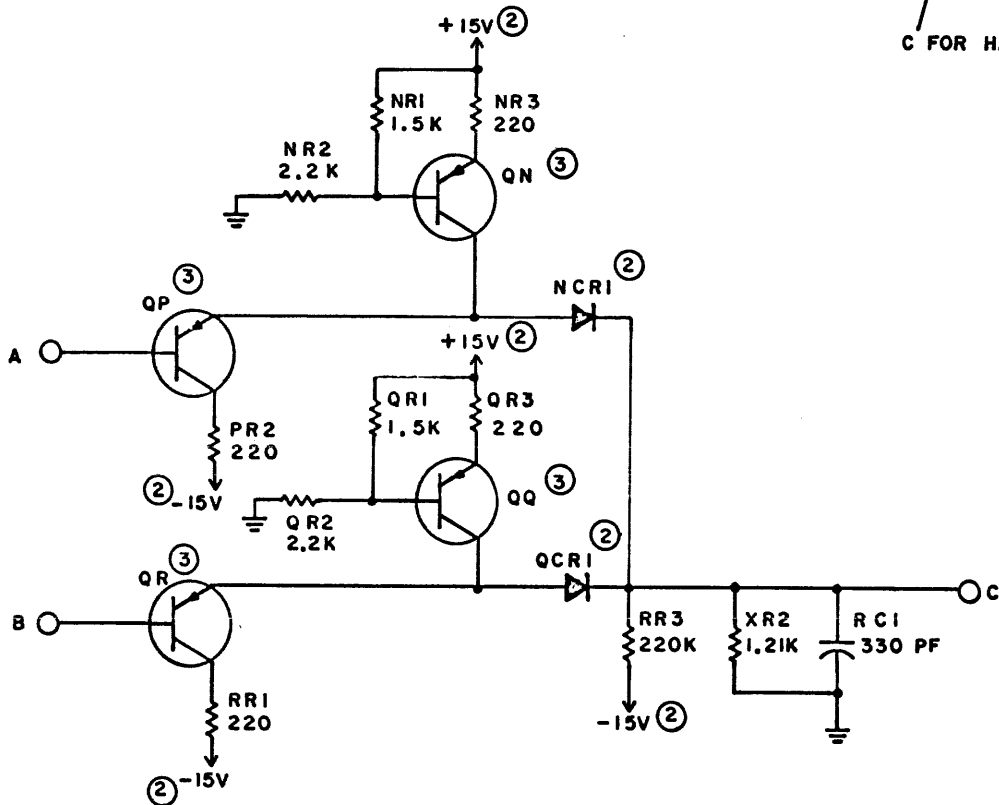
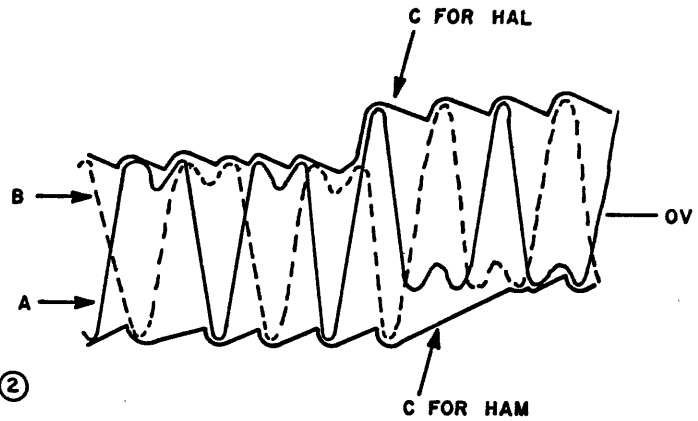
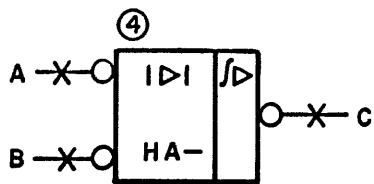
Amplifier - HAK

The HAK circuit is a differential input amplifier with a clamped single-ended output.

Points A and B are differential inputs to the circuit with NC1 and NC6 acting as coupling capacitors. QN and QP are the amplifying transistors in the common emitter configuration and QQ and QR are emitter followers providing a low impedance output.

NC4 and NC7 isolate DC voltages entering NCR1 through NCR4 from the collector circuit of QP and acts as a clamp to the amplified AC signal if it is larger than the diodes threshold voltage.

Output C is typically connected to the input (A) of the HAN circuit. Output C has a single-ended output to differential input voltage gain of approximately 10 (before clamping).



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② POLARITY REVERSED ON HAM,
- ③ NPN USED ON HAM.
- ④ HAM RECTIFICATION IS NEGATIVE (-|D|)

7J17

SUMMING RECTIFIER - HAL/HAM

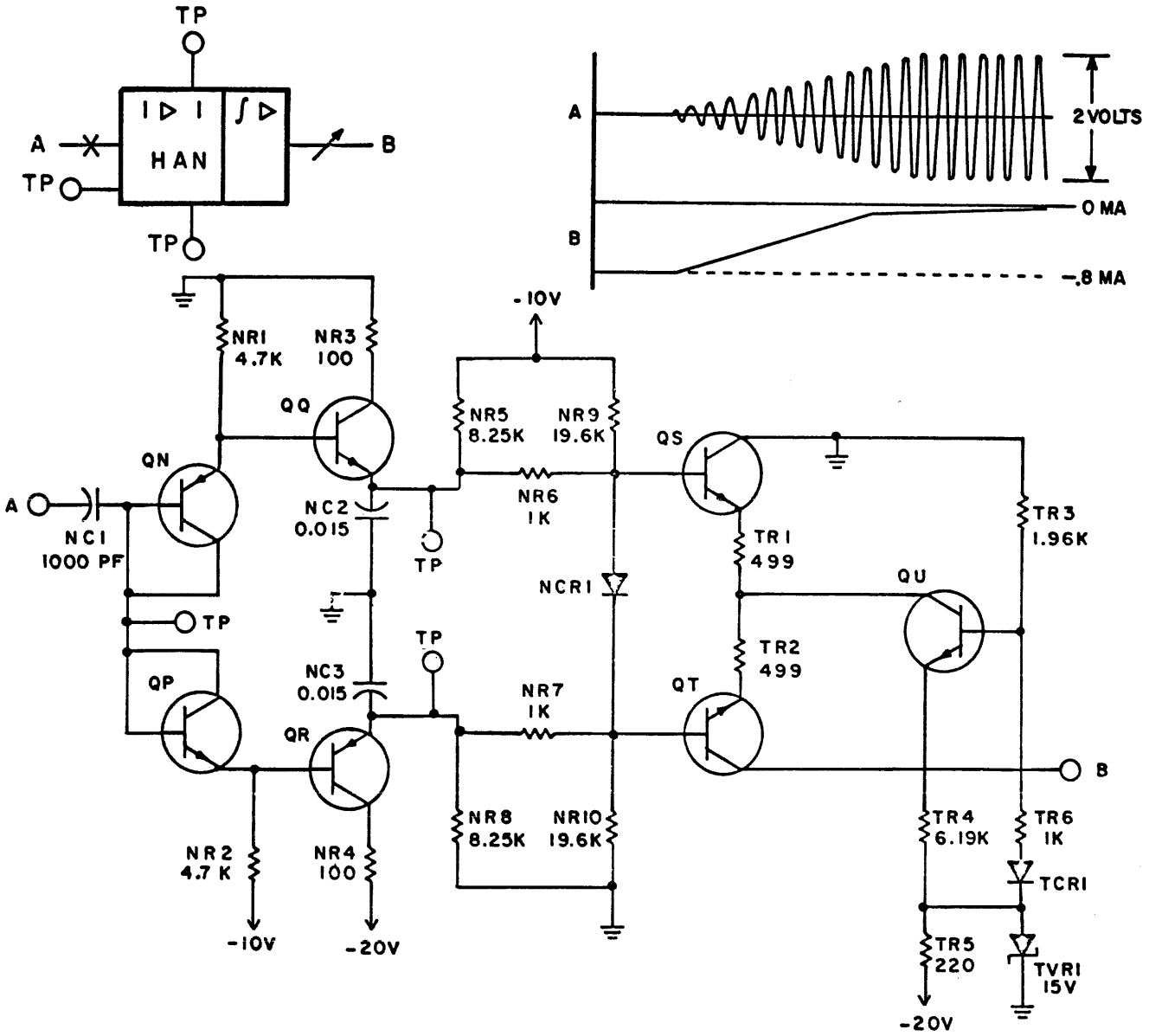
The HAL/HAM circuit is a summing rectifier that receives the MFM (modified frequency modulation) differentiated read signal and a delayed (150 ns) version of the same signal. The circuit OR's the two signals such that the output follows the more positive (HAL) or negative (HAM) signal excursion, giving the appearance of a rectified output. When the outputs of both circuits are observed simultaneously, what results is a silhouette of the two input waveforms. An output capacitor provides integration to maintain most of the positive (HAL) or negative (HAM) charge until the next peak arrives.

An emitter follower at each input receives the delayed or the nondelayed version of the differentiated read signal. Current generators tied to the emitters provide sufficient current for the input transistors and charge the output capacitor during a signal peak.

Assume a positive signal peak occurring at input A of the HAL circuit. As the signal increases toward a peak the QP emitter follows, causing diode NCR1 to turn on and conduct current from QN into the capacitor RC1. At this time the signal at input B is less positive than that at A. Since the QR emitter follows input B, diode QCR1 is back biased off. The capacitor voltage at output C follows the input A signal closely until it peaks. As the signal at A starts decreasing, diode NCR1 starts turning off, due to the stored capacitor charge. The capacitor begins discharging through XR2. At this time output C is more positive than either A or B, and both diodes are cut off.

Now assume the delayed signal at B approaches its peak and becomes more positive than C. The QR emitter follows and turns on diode QCR1 which conducts current from QQ into capacitor NC1. The capacitor voltage at output C now follows input B closely until it peaks. When B begins decreasing, diode QCR1 turns off and the capacitor again starts discharging through XR2.

The HAM circuit operates in a similar manner, except that all polarities are reversed.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

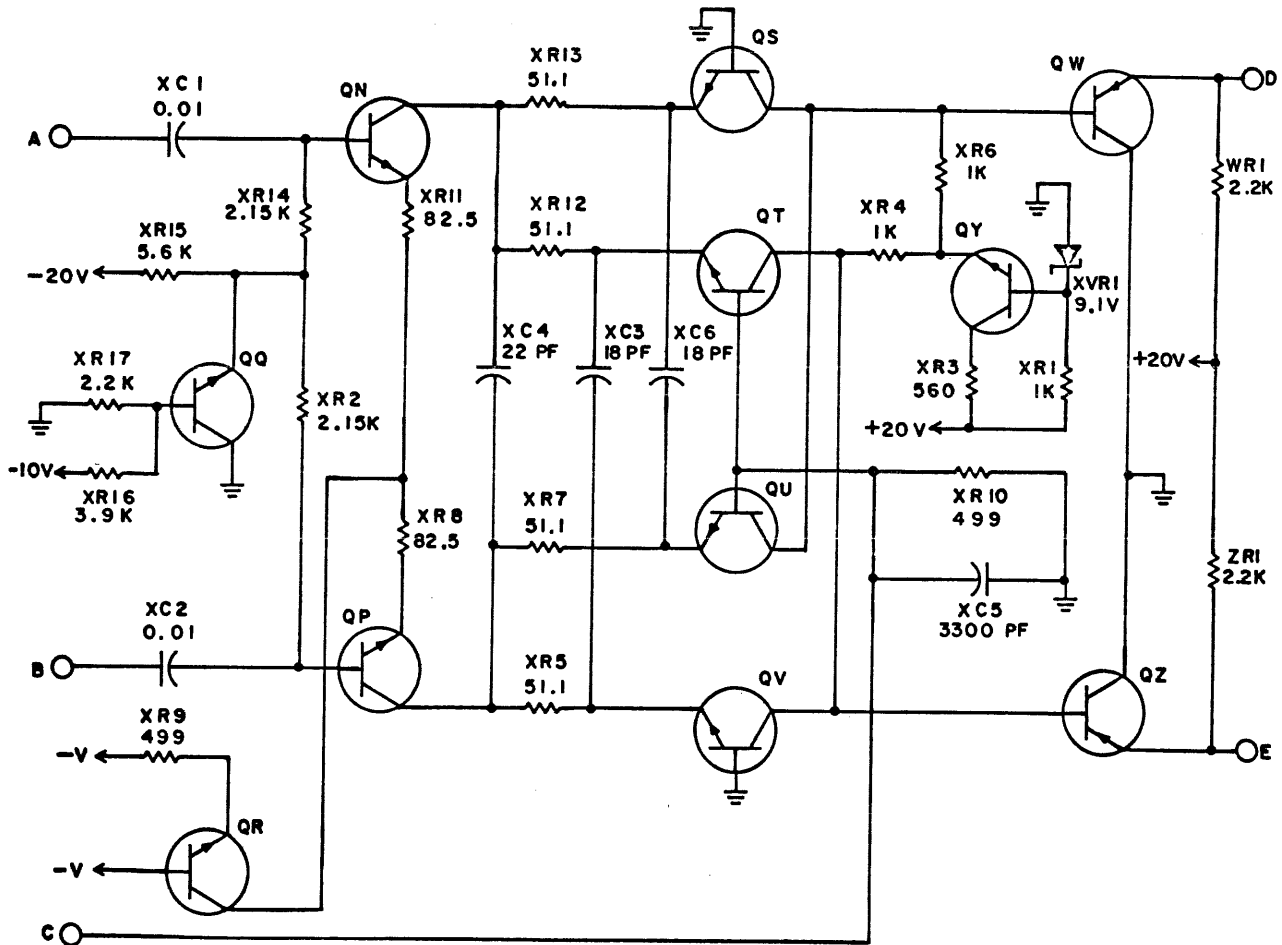
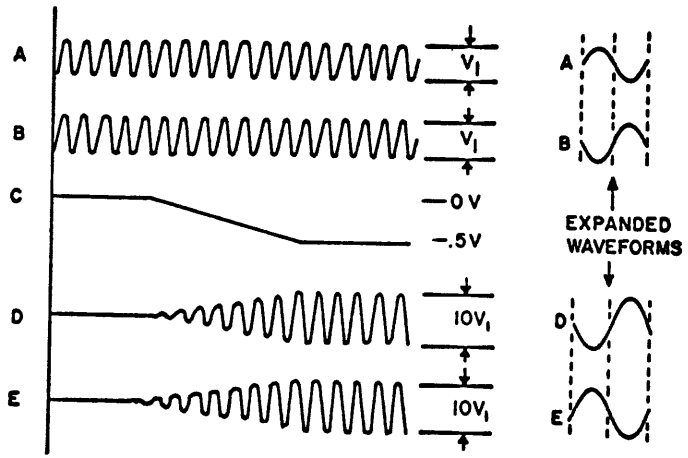
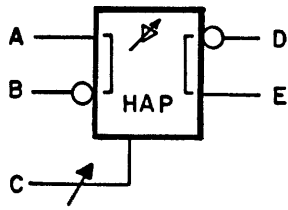
7J18A

Peak Holding Amplifier - HAN

The HAN circuit provides a DC sink current with a magnitude inversely proportional to the magnitude of the AC input signal. Typically the input signal at point A is an amplified read head signal coming from output C of the HAK circuit. Output B is connected to point C of the HAP circuit and controls the gain of that circuit.

QN, QQ, QP and QR form a positive and a negative rectifier. When an AC signal is applied to the input, QQ charges NC2 to a positive peak value and QR charges NC3 to a negative peak value. These peak values are held by the two capacitors which discharge with a time constant determined by NC3 and NR8 in parallel with NR7 and NR10. With a long time constant compared with the frequency of the input AC signal, the voltage on the two capacitors is a DC voltage.

The voltage difference across NC2 and NC3 is directly proportional to the peak-to-peak amplitude of the input waveform and is applied through resistor dividers to current amplifier QS and QT. With no signal at input A, the current amplifier is biased to permit QT to pass all the current supplied by current sink QU. As the AC input signal increases in amplitude the peak difference appearing across NC2 and NC3 is applied to the current amplifier, and QS starts to pass sink current which cuts down current flow through QT.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J19A

AGC AMPLIFIER - HAP

The HAP circuit is a differential amplifier with gain controlled by a negative voltage at input C.

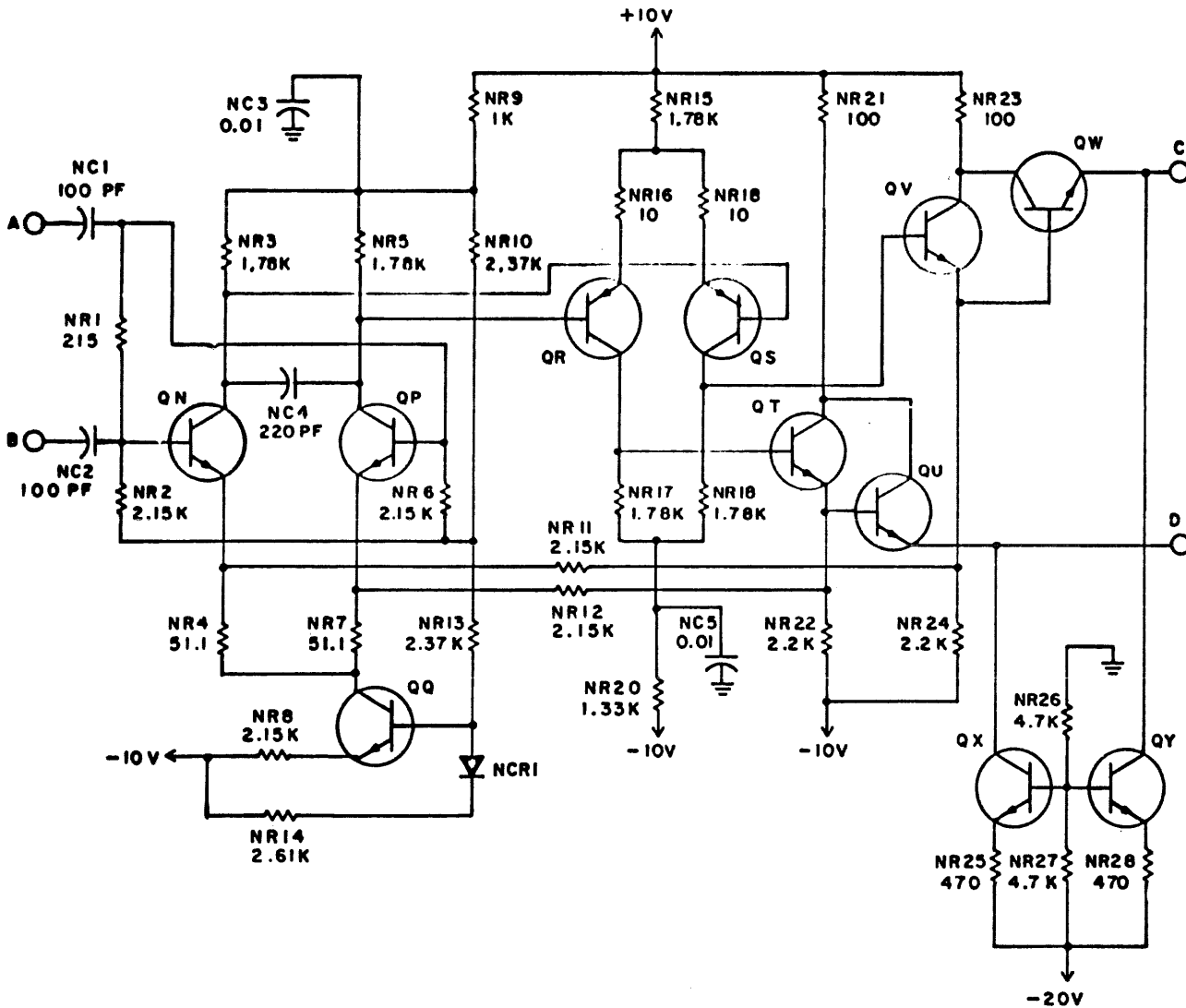
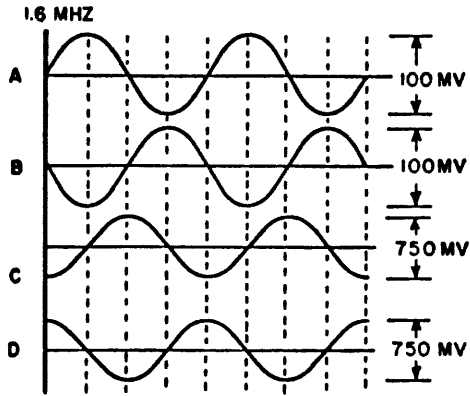
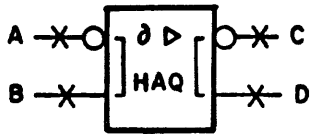
QN and QP are amplifying transistors with their maximum gain determined by the ratio of XR8 and XR11 to XR4 and XR6.

Common base amplifiers, QS, QT, QU, and QV pass amplified current signals to resistors XR4 and XR6. QS and QU pass out of phase signals to collector resistor XR6. Likewise, QT and QV pass out of phase signals to collector resistor XR4.

Control voltages on the bases of QT and QU control circuit gain. With 0 volts for control voltage, QS, QT, QU, and QV turn on equally, causing out of phase voltage to cancel, leaving a net output or gain of 0 volts. Increasing the control voltage negatively starts turning off QT and QU causing the amplifier gain to increase. Turning off QS, QT, QU, and QV requires that the control voltage be approximately -0.5 volts, which allows an amplifier gain of 10.

Emitter followers QW and QZ provide low output impedance.

QQ, XR15, QR16 and XR17 make up a current sink network which controls the collector current of QN and QP.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J20A

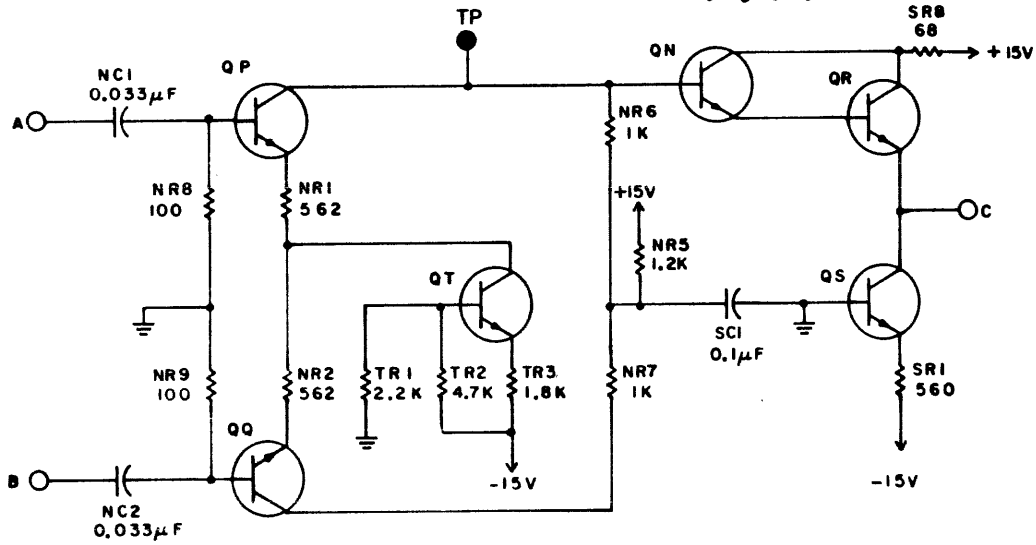
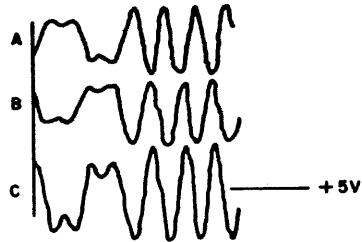
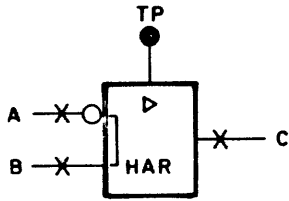
Differentiator/Amplifier - HAQ

The HAQ circuit consists of a passive RC network (used as a differentiator and a differential amplifier) to boost the attenuated signal level.

The HAQ, inputs A and B, are connected to outputs D and E of circuit HAP, which supplies an amplified read head signal. NC1, NR1 and NR2 make up the differentiator which has a break frequency at 15 MHz.

The two stage differential amplifier consists of first stage QN and QP with current sink QQ direct coupled to second stage QR and QS. QT, QU and QV, QW form darlington emitter followers for low output impedance capable of driving coax lines terminated by 100 ohm resistors. QX and QY are constant current sources.

NR11 and NR12 provide AC/DC feedback from the output to input emitters of the first stage. Closed loop voltage gain is proportional to the ratio, NR11 to NR4 (and NR12 to NR7). Capacitor NC4 provides rolloff at the upper cutoff frequency.



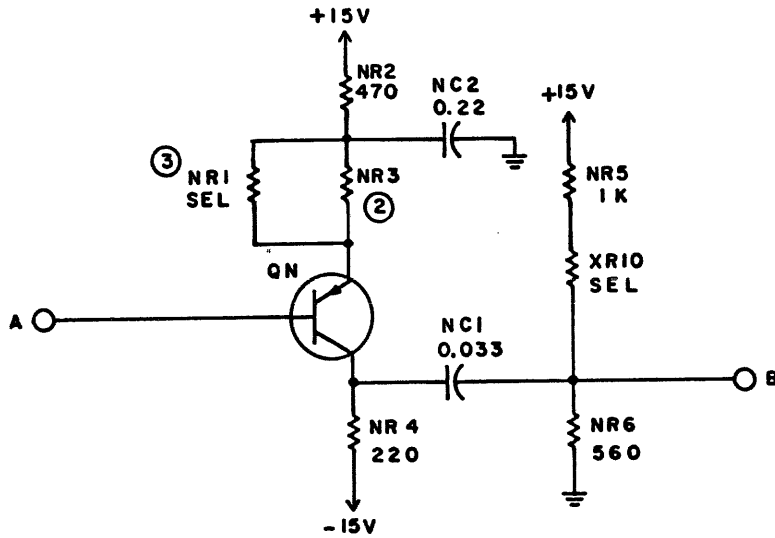
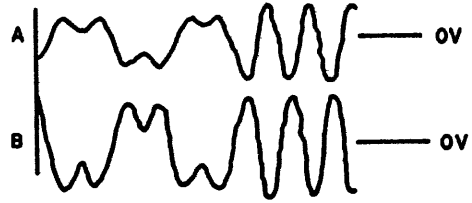
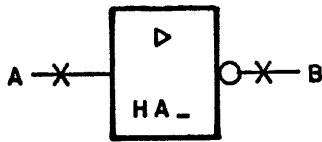
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY

7J21B

DIFFERENTIAL AMPLIFIER - HAR

The HAR circuit accepts a double-ended MFM (modified frequency modulation) differentiated signal and provides a single-ended output suitable for driving a delay line. The maximum input differential voltage is approximately 1.8 volts. The overall circuit gain is approximately 1.6.

Transistors QP, QQ and constant current source QT form the differential amplifier stage and give common mode signal rejection. Voltage gain is given approximately by $NR6$ divided by $NR1$ or $NR7$ divided by $NR2$. The collector of QP drives transistors QN and QR which are connected in a low loading Darlington pair (high current amplification configuration). This circuit in conjunction with a second constant current source, QS, gives a single-ended output.



NOTES:

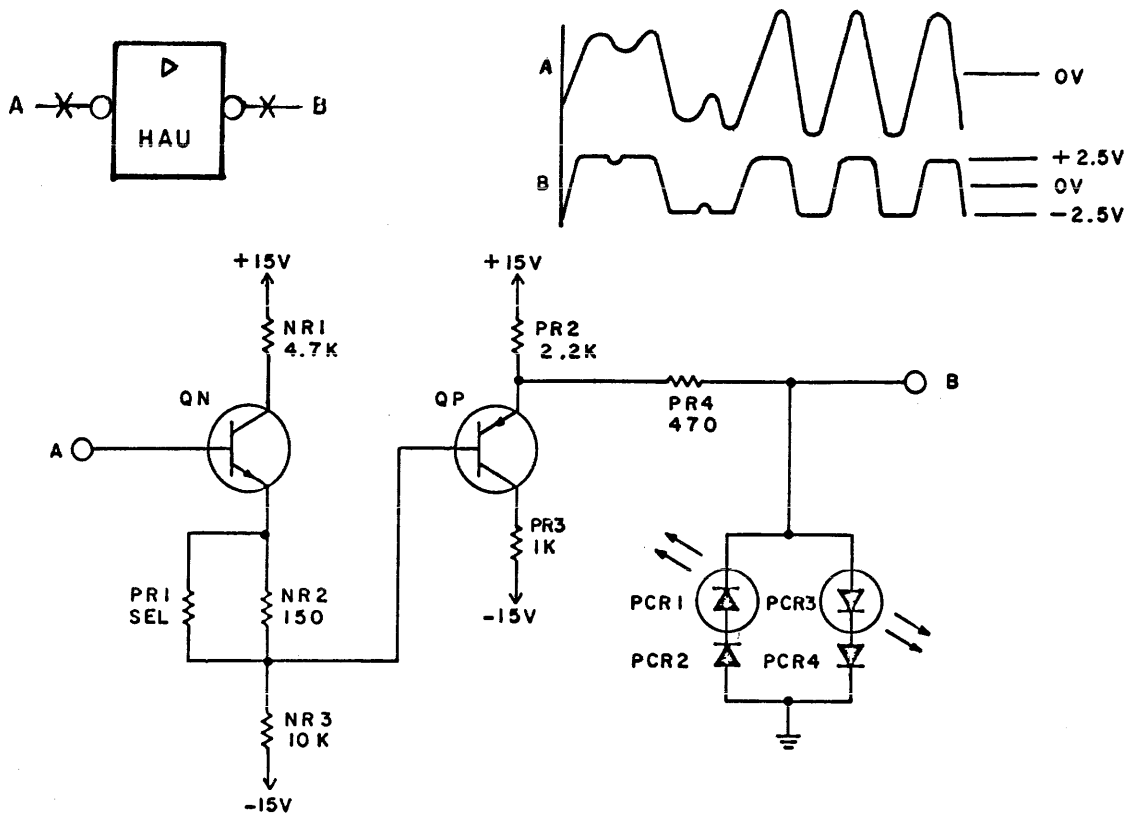
1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② 100-OHMS ON HAT, 22-OHMS ON HAS.
- ③ NOT USED ON HAS.

7J22

AMPLIFIER - HAS/HAT

The HAS/HAT circuit amplifies the MFM(modified frequency modulation) differentiated read signal. The circuit gain is approximately 6.5 for the HAS and 3 for the HAT.

Transistor QN functions as a simple common emitter amplifier. Capacitor NC2 applies ac ground to the junction of NR3 and NR4. Capacitor NC1 provides ac coupling to the output and enables the output bias level to be adjusted to zero volts by selecting resistor XR10.

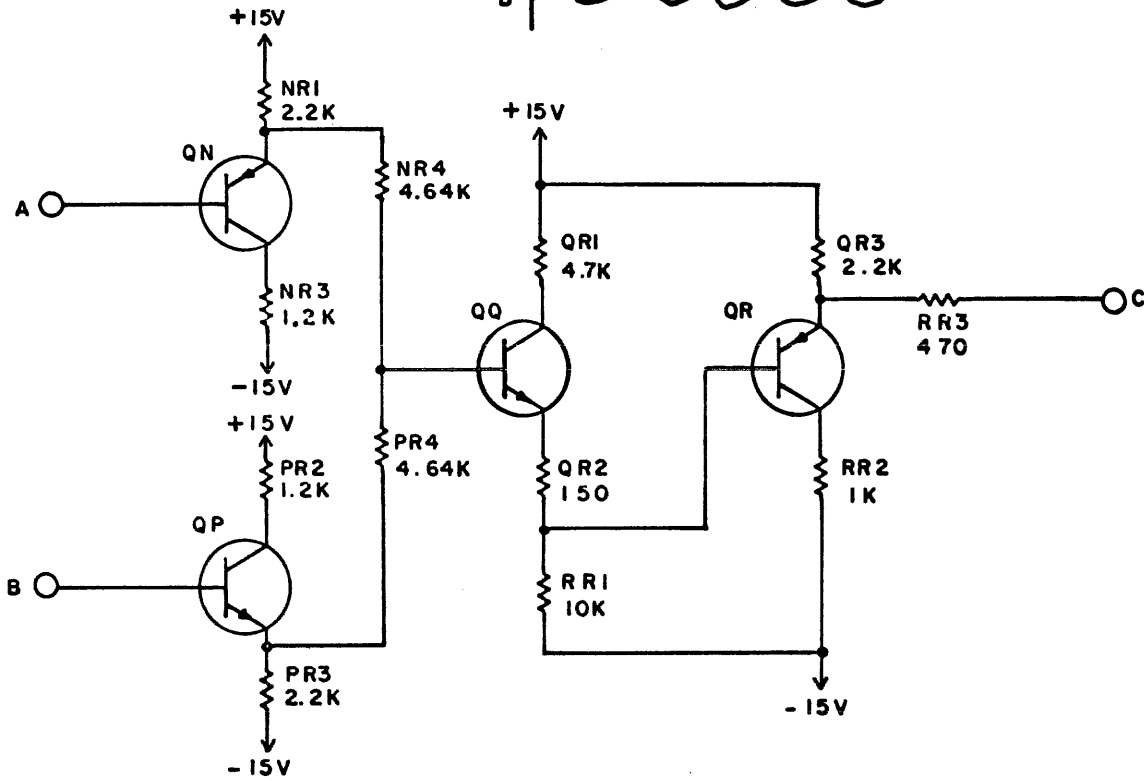
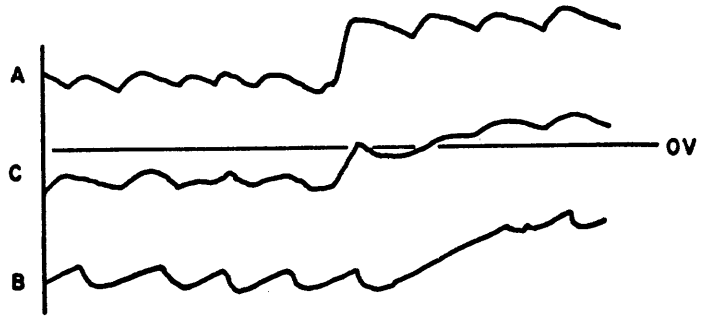
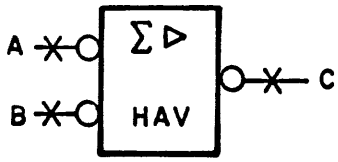


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J23

BUFFER AMPLIFIER - HAU

The HAU circuit incorporates two emitter followers in series to provide a buffer with high input impedance and low output impedance. The circuit is used to drive a zero crossover detector. Diode clamps are used to provide protection against large signal swings at the crossover detector input.

An MFM (modified frequency modulation) differentiated signal at the input encounters a silicon junction voltage drop at QN and a further voltage drop due to NR2 and the selected resistor PR1. This second drop is approximately 250 mv. A voltage rise is seen at QP such that the output is left biased approximately 180 mv negative. The selected resistor is chosen to match this dc bias with the bias at the output of the averaging amplifier, HAV. The diode clamps limit output signal amplitude to 2.5 volts above and below ground.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

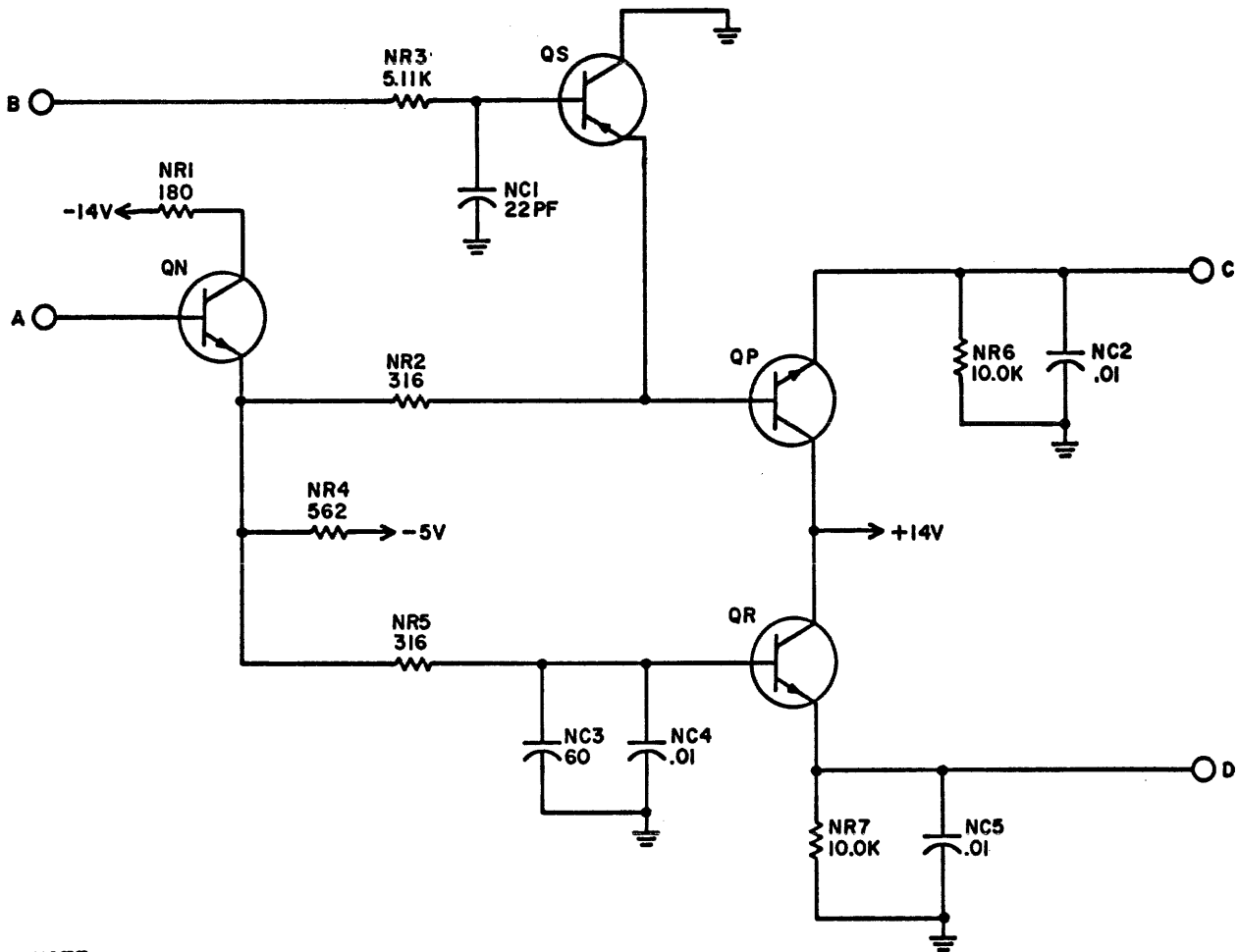
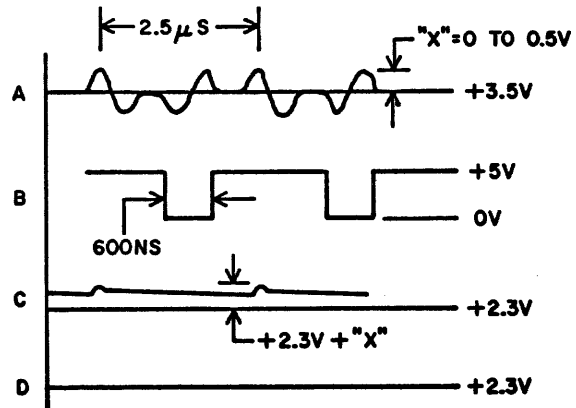
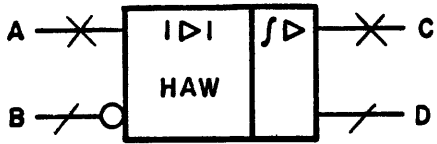
7J24

AVERAGING AMPLIFIER - HAV

The HAV circuit is an averaging amplifier that receives two waveforms representing the differentiated MFM (modified frequency modulation) read signal peak amplitude. The circuit forms the instantaneous average or mean baseline of the two inputs. The mean baseline is used later in the read circuit to extract the information from the delayed differentiated read signal.

Input A is always biased in the positive direction. Input B is biased by a similar amount in the negative direction. The amount of biasing is a function of the peak amplitude of the amplified differentiated read signal. Transistors QN and QP are emitter followers which reduce the loading on the previous circuit. These elements feed a voltage divider formed by equal valued resistors NR4 and PR4. Since current through the divider is always in the direction from NR4 to PR4, the divider output voltage is the instantaneous average of the inputs.

Transistors QQ and QR form a buffer stage to reduce loading on the divider output. Transistor QR2 adds a slight negative dc bias to the output signal. The buffer output is suitable for driving a zero crossover detector.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J108

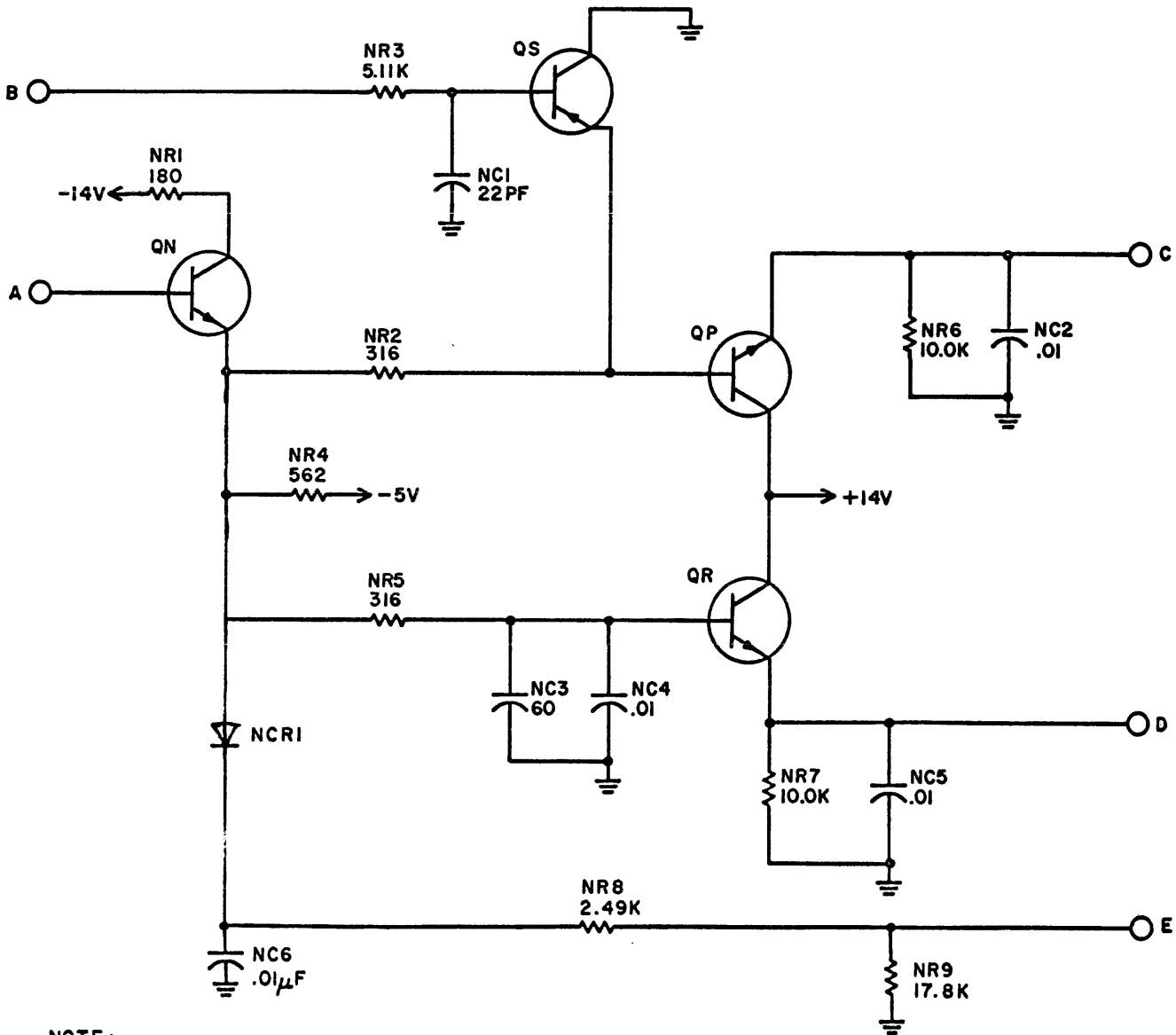
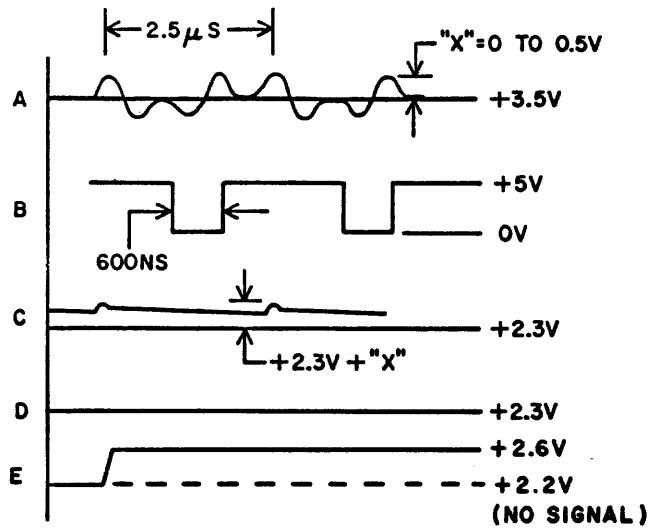
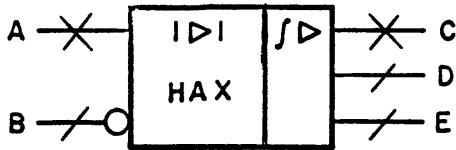
SUMMING RECTIFIER – HAW

The HAW circuit is a summing rectifier that receives the differentially-amplified dibit signals read from the servo head. The outputs are applied to an operational amplifier connected as a differential amplifier to generate a rectified signal proportional to the average amplitude of the dibit signal. The HAW circuit rectifies positive dibits and the HAX circuit rectifies negative dibits. These two output signals are applied to a summing amplifier to generate the track servo signal. When the servo head is centered between servo tracks providing positive and negative dibits, their relative amplitudes are equal. The track servo signal is then at null.

Input A receives the dibit signals. Buffer/driver transistor QN is connected as an emitter follower to provide isolation with a gain of one.

QP and QR are matched transistors in a single can, thus eliminating temperature and offset drifts from the peak detector. The signal passing through QR has the information pulses filtered out of it by NR5, NC3, and NC4 to generate the true base line voltage on output D. This same input signal fed to QR is also given to QP; however, the QP input is not filtered. This allows QP to respond to the highest peak values. Output C is, therefore, a voltage that is the baseline voltage plus the highest positive information peaks. The difference between C and D is the true information.

QS is used to gate out unwanted information. When input B is at +5V, QS is turned off to allow all signals to pass to QP. When input B is at ground, QS is turned off, thus shorting out all information on the base of QP. The waveform illustrates a typical application for the HAW circuit that rectifies the positive dibit signals. Note that the positive peaks of the negative dibits are now allowed to affect the output.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

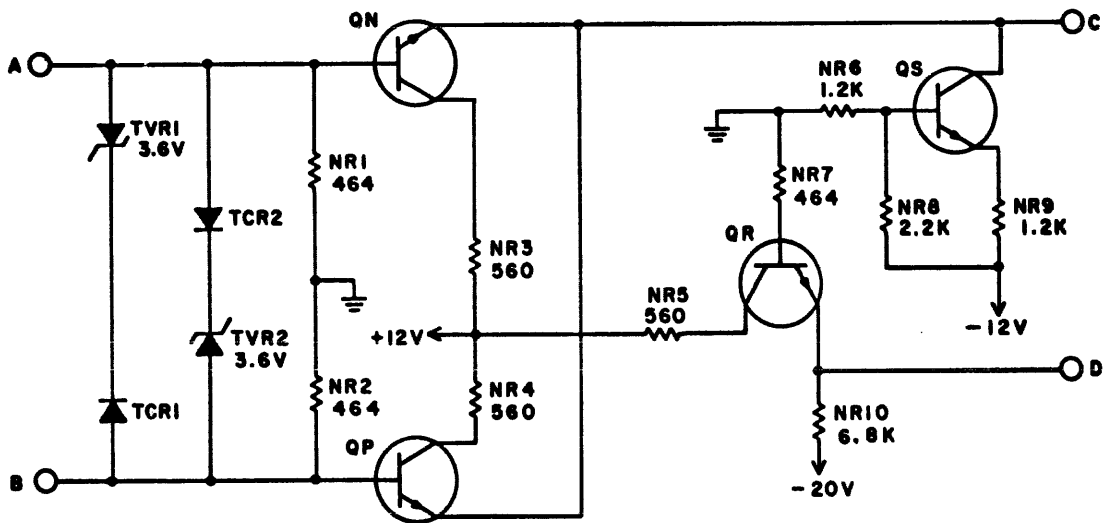
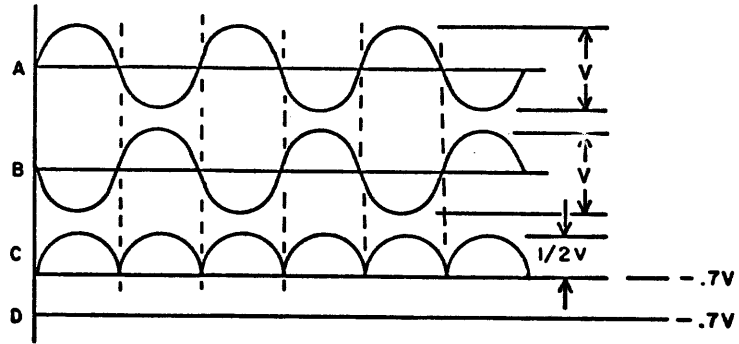
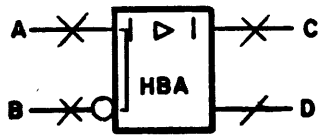
7J193

SUMMING RECTIFIER -- HAX

The HAX circuit is identical to the HAW summing rectifier, except that output E and its associated circuitry has been added.

In its typical application, outputs D and E are applied to the inverting and noninverting inputs of an open loop operational amplifier. When the voltage at E is greater than the voltage at D, the op amp output indicates that dibits are being sensed.

NCR1 and NC6 rectify the signal applied to input A. The voltage on NC6 is equivalent to the peak voltage of the positive swing of the dibits. Before dibits are sensed, this voltage is equal to the input baseline voltage minus the diode drops across QN and NCR1. With NR8 and NR9 acting as a voltage divider, output E is less positive than output D. When dibits are sensed, NC6 is charged by the dibits, driving output E to a more positive value.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7 J104

RECTIFIER - HBA

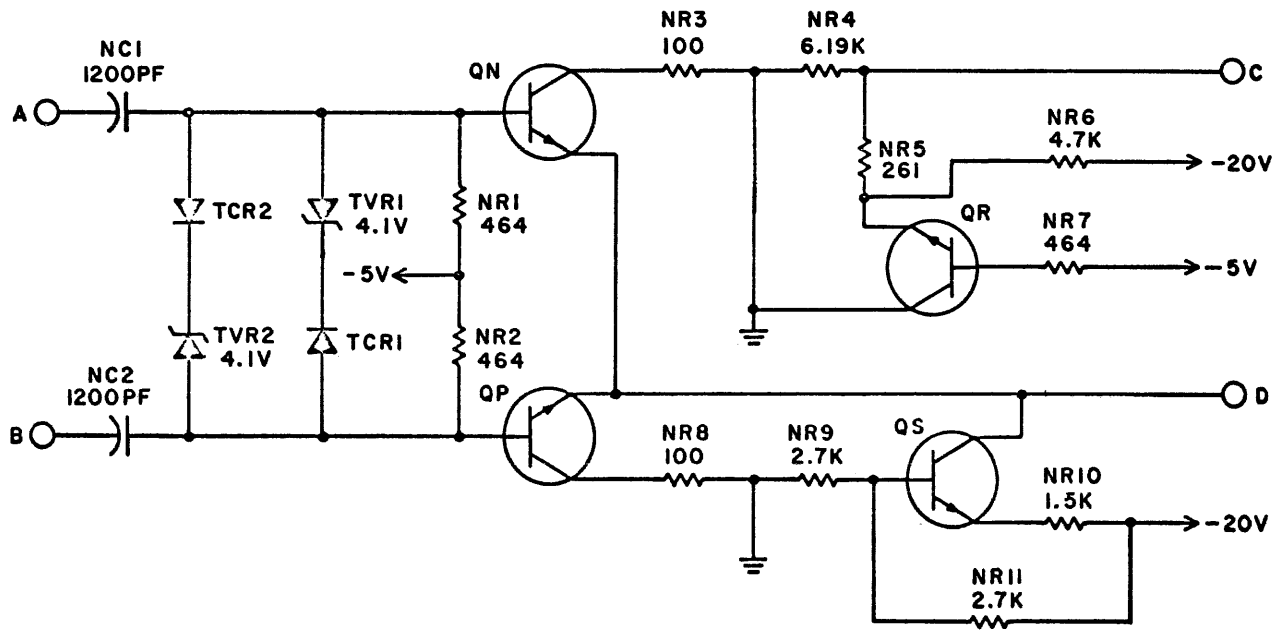
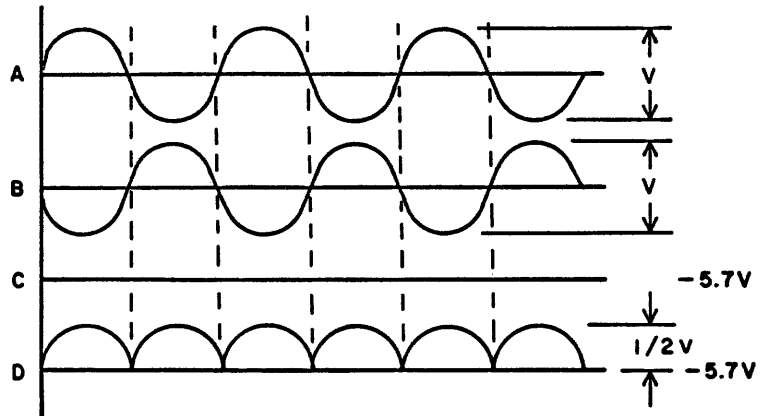
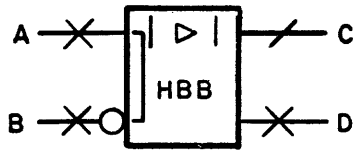
The HBA circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at ground potential by NR1 and NR2. With no signal input, point C rests at -.7 volts. NR6, NR8, NR9, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point C (waveform C).

Network NR5, NR7, NR10, and QR set up a DC reference voltage at point D which matches the "no signal" DC voltage at point C (QN, QP, and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent over-voltage damage to reverse biased base-emitter junctions of QN and QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7JI03

RECTIFIER - HBB

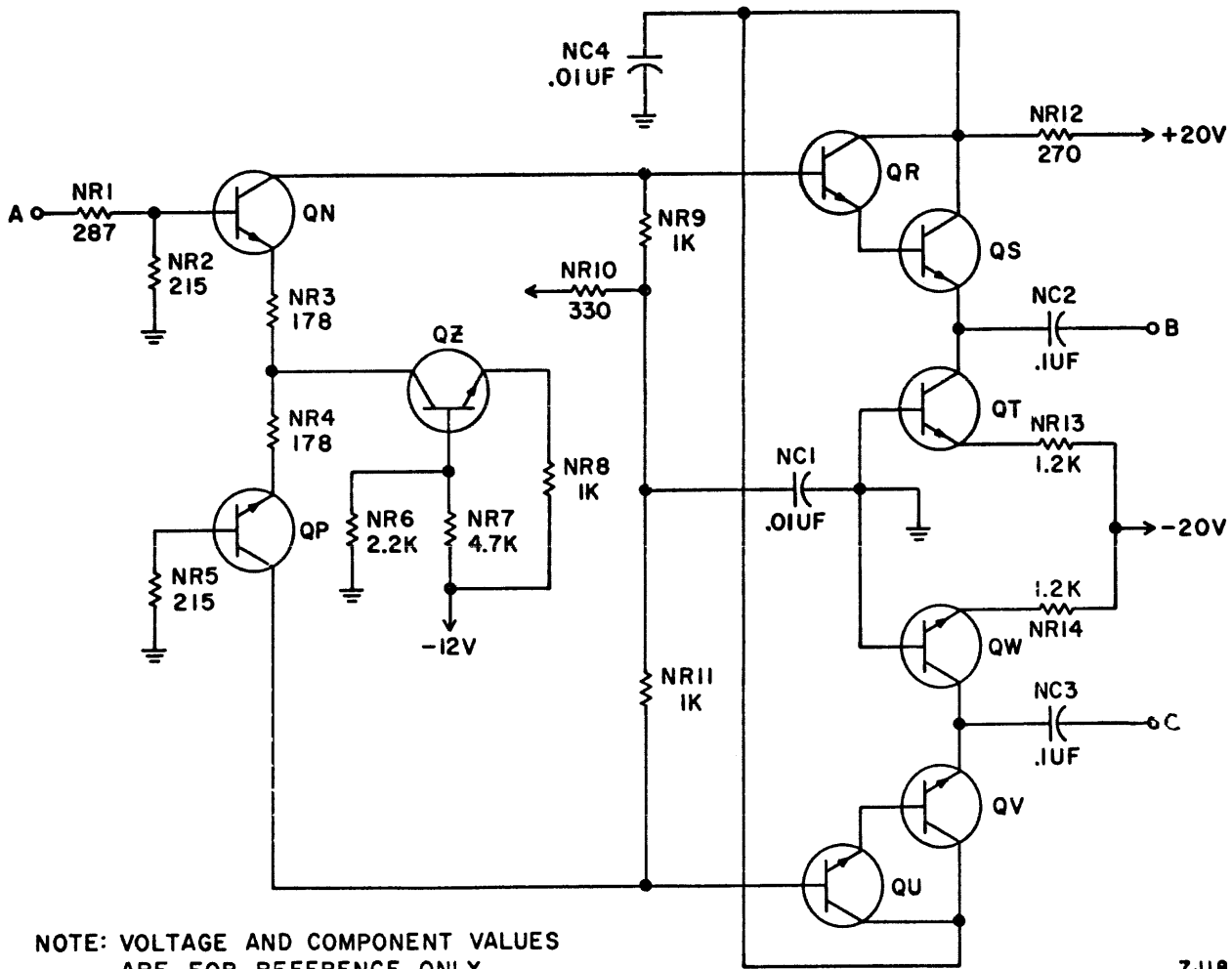
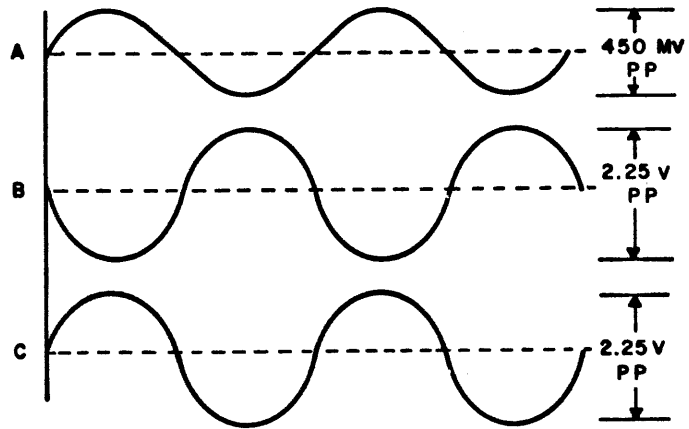
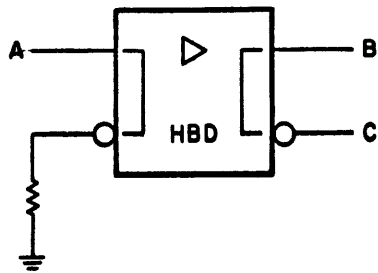
The HBB circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at -5 volts by NR1 and NR2. With no signal input, point D rests at -5.7 volts. NR9, NR10, NR11, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point D (waveform D).

Network NR4, NR5, NR6, NR7, and QR set up a DC reference voltage at point C which proportionally tracks the "no signal" DC voltage at point D (QN, QP and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent overvoltage damage to reverse biased base-emitter junctions of QN and QP.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J101

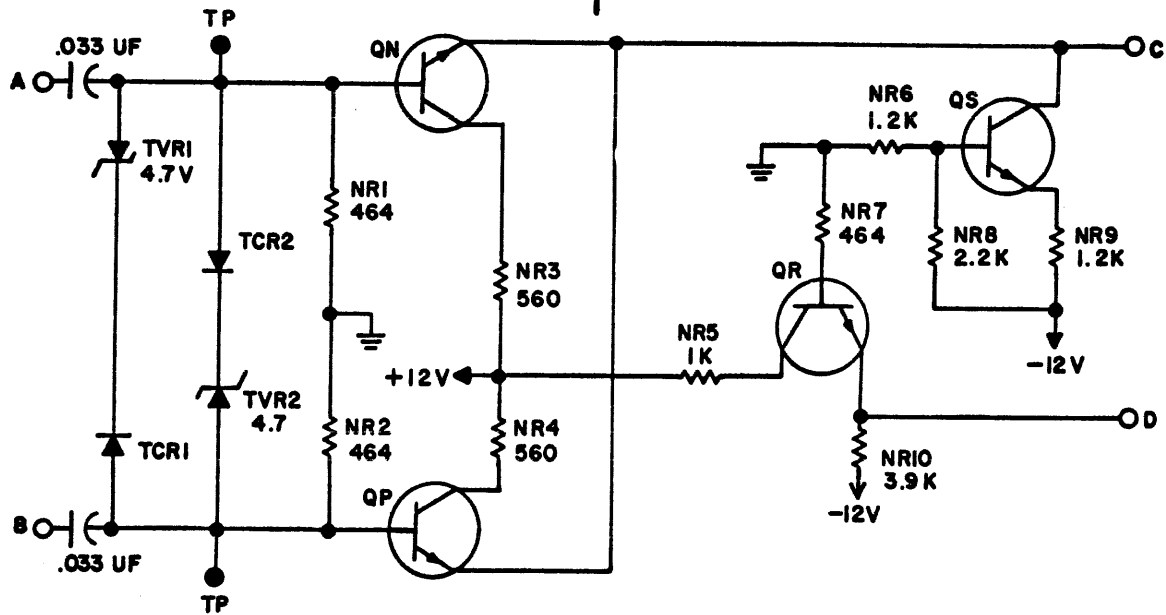
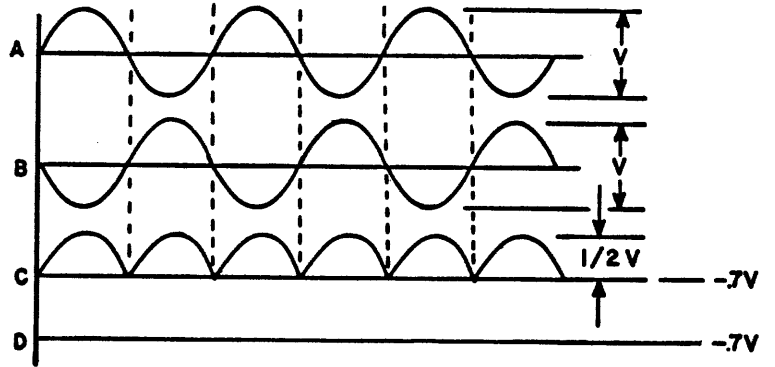
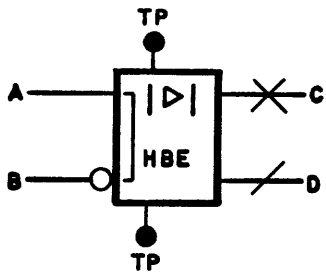
BUFFER AMPLIFIER - HBD

The HBD circuit is a single input, differential output buffer amplifier.

QN and QP are the amplifying transistors. The gain of the circuit is largely determined by the ratio of NR9 to NR3 and NR11 to NR4. Because the base of QP is at ground potential, the voltage at the collector of QP proportionally follows the voltage at the emitter of QN.

QZ, NR6, NR7, and NR8 are a current sink network which provides collector current for QN and QP.

Each output consists of two transistors connected as a common emitter darlington pair (QR and QS, QU and QV) with current supplied from a current sink (QT and QW).



NOTE;
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J148A

RECTIFIER - HBE

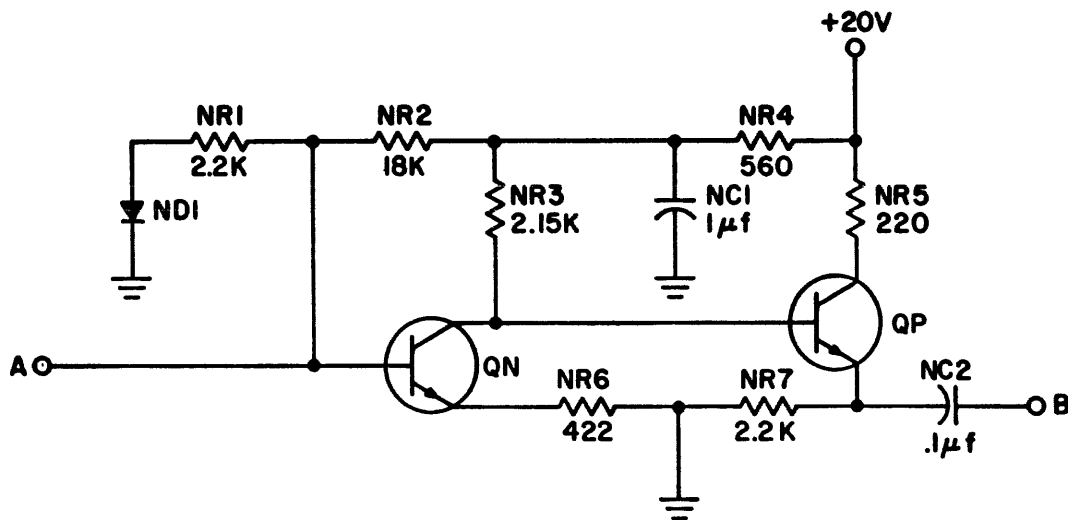
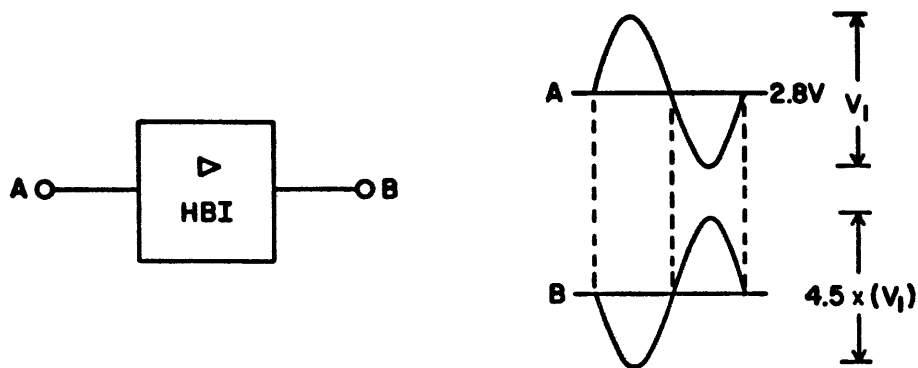
The HBE circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at ground potential by NR1 and NR2. With no signal input, point C rests at -.7 volts. NR6, NR8, NR9, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point C (waveform C).

Network NR5, NR7, NR10, and QR set up a DC reference voltage at point D which matches the "no signal" DC voltage at point C (QN, QP, and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent over-voltage damage to reverse biased base-emitter junctions of QN and QP.



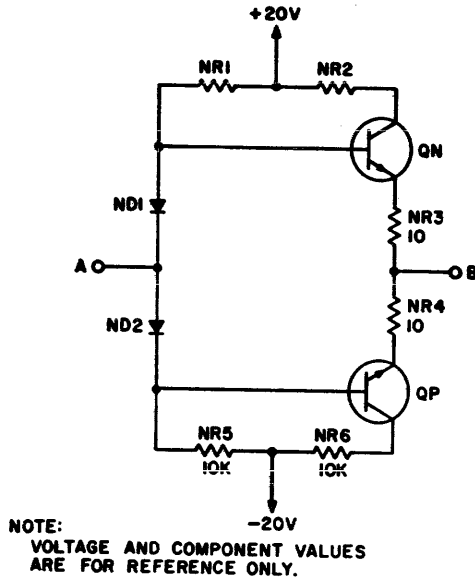
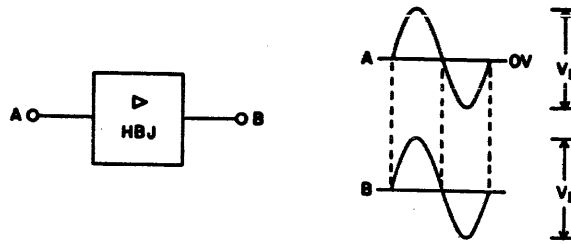
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

8D48

AMPLIFIER - HBI

The HBI circuit is a low gain amplifier with a fixed gain of 4.5. NR1, NR2, and ND1 form a biasing network for transistor QN. QN is the amplifying transistor with voltage gain determined by the ratio of NR3 to NR6.

Transistor QP is an emitter follower to provide a low output impedance. NC2 is a ac coupling capacitor which provides dc isolation between circuits.



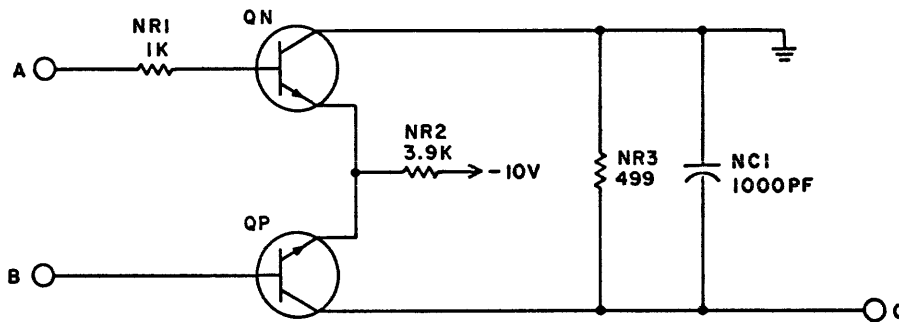
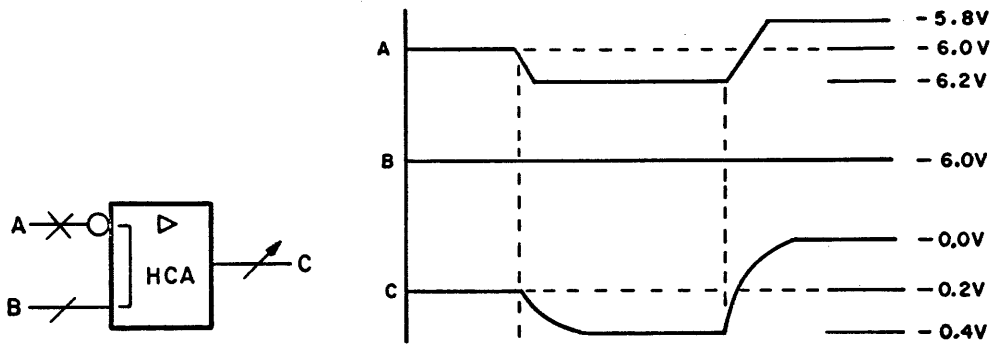
8D47

BUFFER AMP - HBJ

The HBJ circuit is a current/buffer amplifier used for buffering a high impedance output signal source from a low impedance source with an increase in output drive capability.

NR1, ND1, ND2, and NR5 form a biasing network for QN and QP. The voltage drop across the base-emitter junction of QN. Similarly, the voltage drop across ND2 compensates for the voltage across the base-emitter junction of QP.

The biasing networks of QN and QP allow the voltage level at output B follows the voltage level at input A.



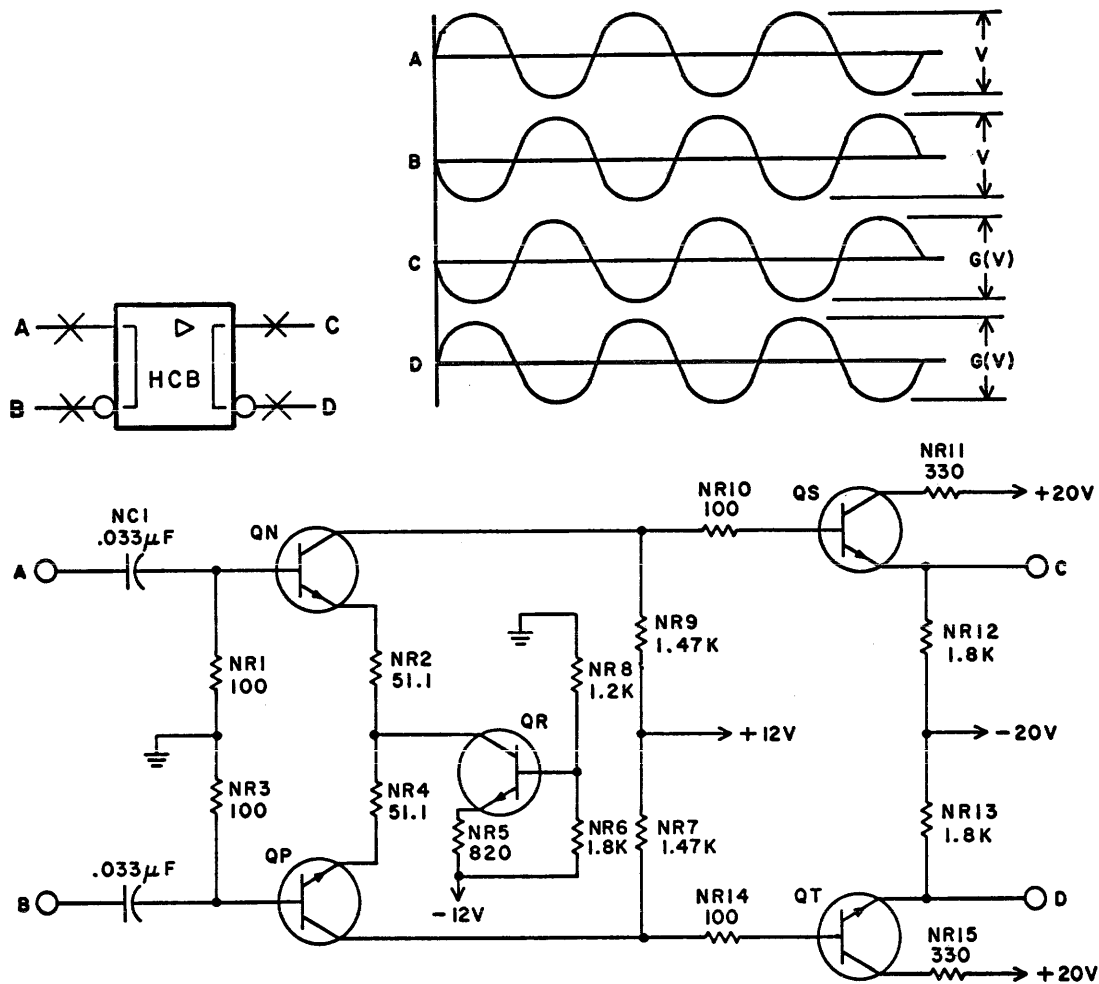
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J101

DIFFERENTIAL AMPLIFIER - HCA

The HCA circuit is a differential amplifier which is used as a control element in an AGC amplifier feedback loop.

Input B is connected to a fixed reference voltage and input A is connected to an integrated DC voltage which is proportional to the output amplitude of an AGC amplifier. When the voltage on input A is greater than that at input B, the current from emitter resistor NR2 goes through QN to ground. When the voltage on input A is less than at B, the current from NR2 goes through QP to output C. When input A equals input B, the current from NR2 is split between QN and QP. The voltage at point C is established by the current through QP times resistor NR3. Point C is the control voltage input for input E on the HCU (AGC amplifier) circuit. NC1 is used as an integrator and helps stabilize the response time.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7 J97

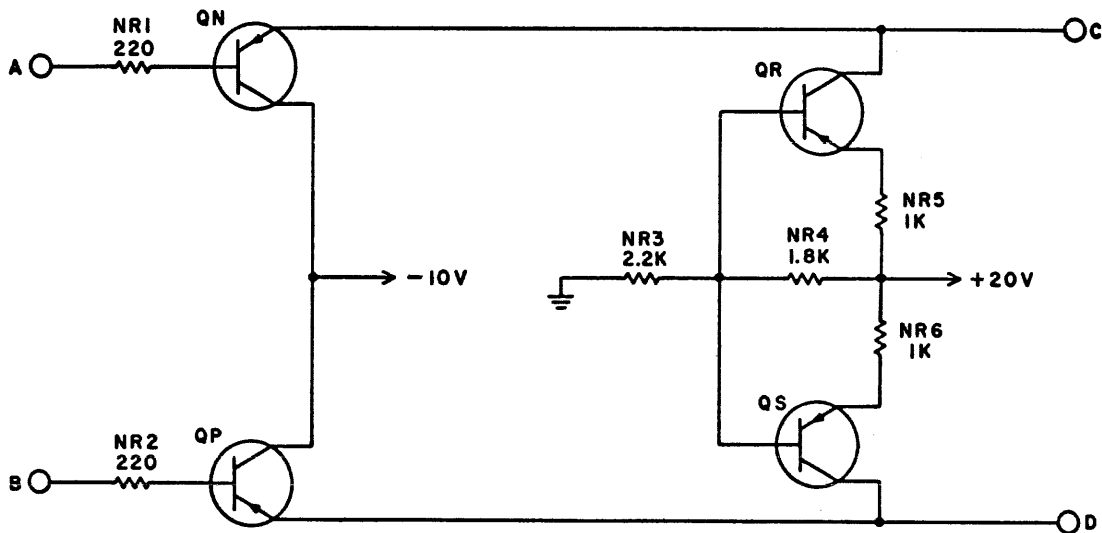
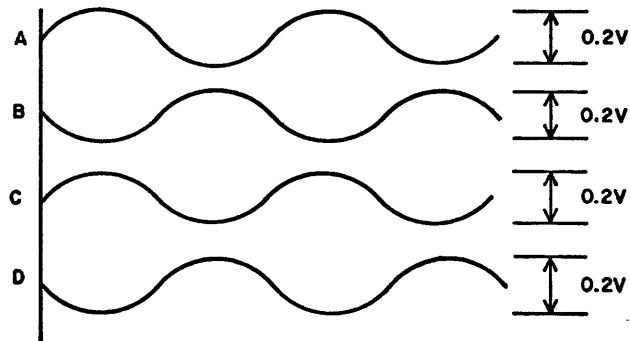
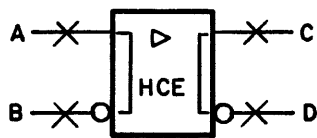
DIFFERENTIAL AMPLIFIER - HCB

The HCB circuit is a single stage differential input, differential output amplifier.

QN and QP are the amplifying transistors. The gain of the amplifier is largely determined by the ratio of NR9 to NR2 and NR7 to NR4.

QR, NR5, NR6, and NR8 are a current sink network which provides collector current for QN and QP.

QS and QT with emitter resistors NR12 and NR13 are emitter followers for low impedance outputs.



NOTE:

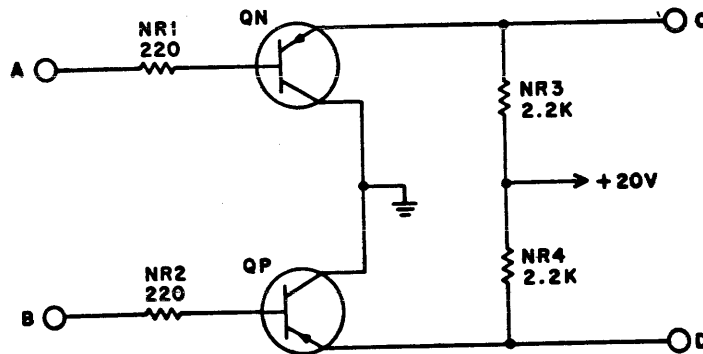
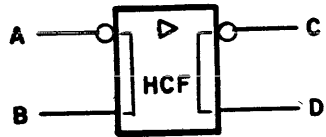
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J98

BUFFER AMPLIFIER – HCE

The HCE circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

Emitter followers QN and QP present comparatively high input impedance at A and B, and low output impedance at C and D. Current sources QR and QS with NR3, NR4, NR5, and NR6 supply constant emitter current to QN and QP.



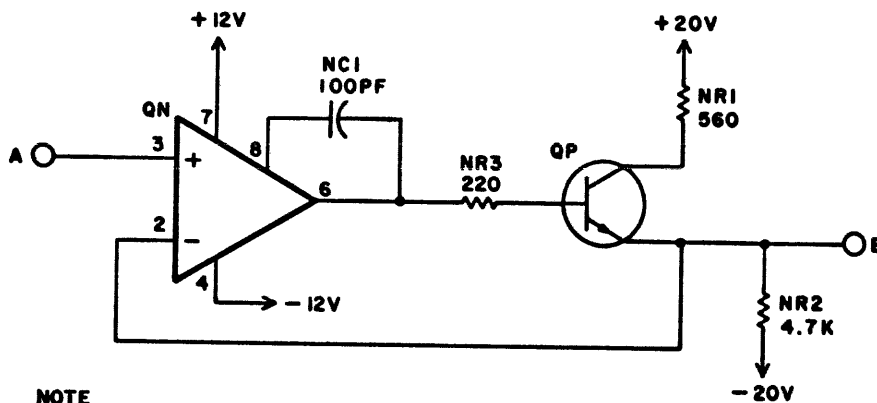
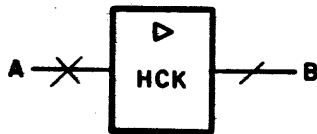
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J95

BUFFER AMPLIFIER – HCF

The HCF circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

QN and QP are emitter followers which present comparatively high input impedance at A and B, and low output impedance at C and D.



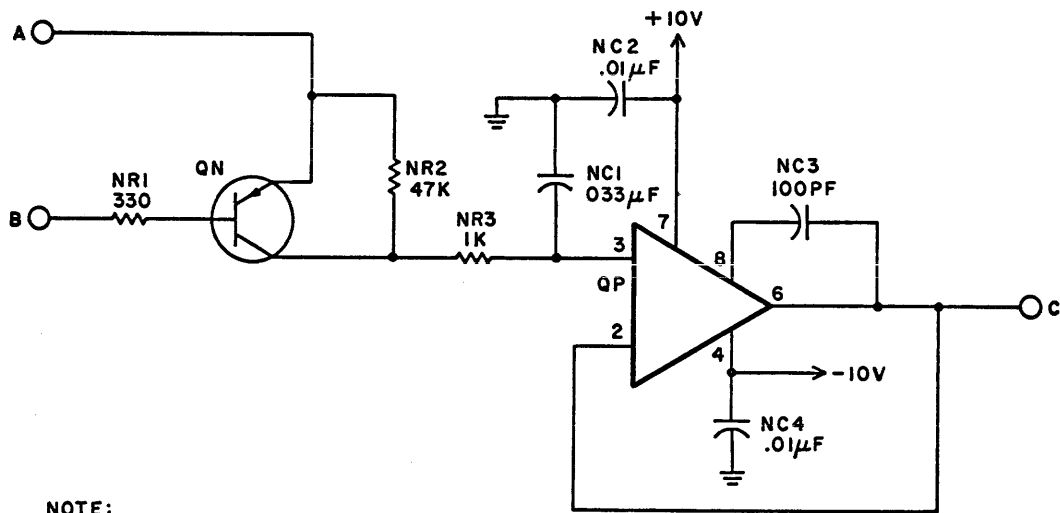
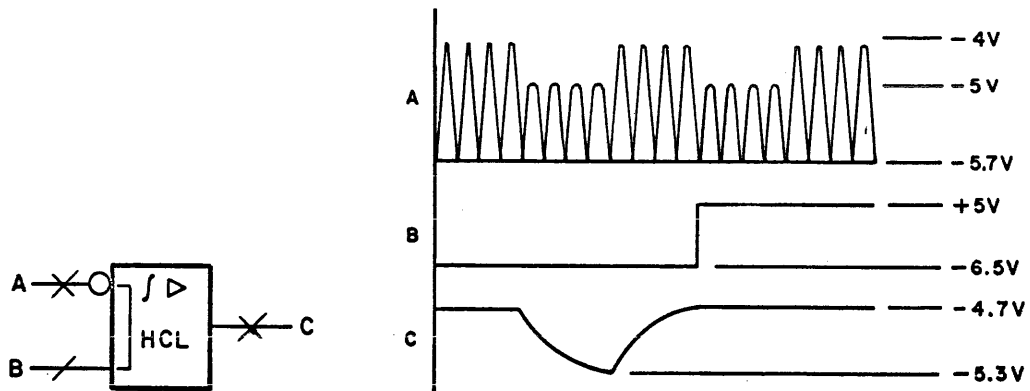
NOTE
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J108

VOLTAGE FOLLOWER – HCK

The HCK circuit consists of an operational amplifier in a voltage follower configuration. An NPN emitter follower (QP) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QP in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QP.

NR2 provides a minimum load current for QP under no output load conditions. NR1 is a current limit resistor. Resistor NR3 and capacitor NR1 stabilize the circuit.



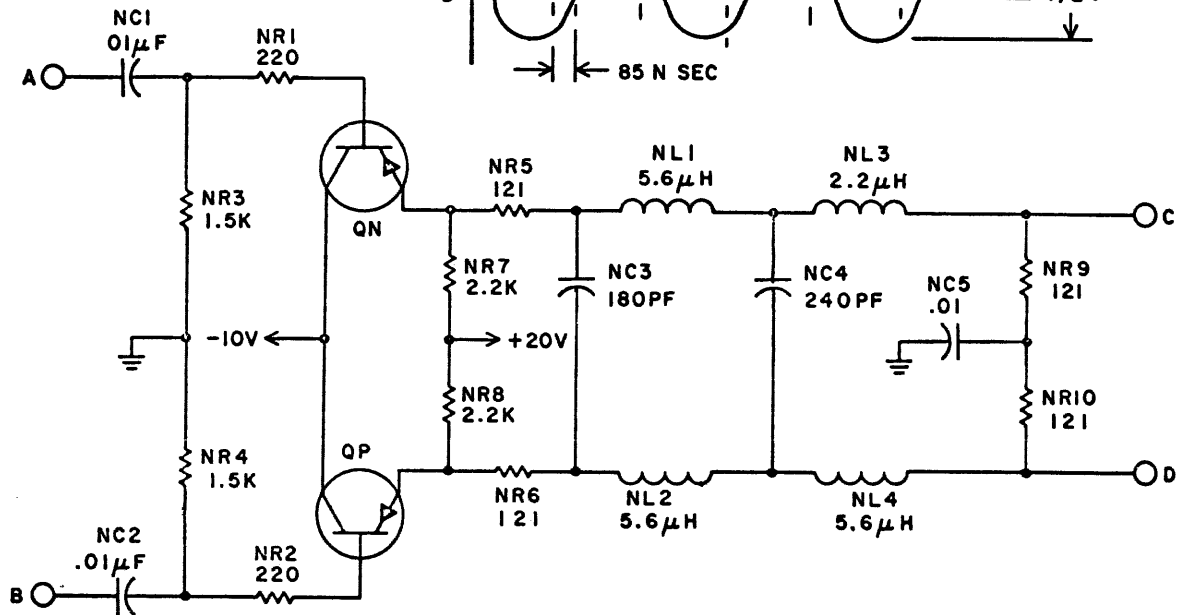
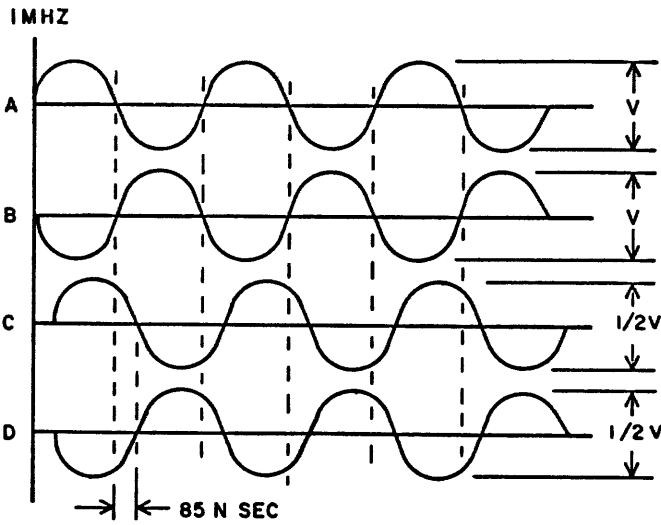
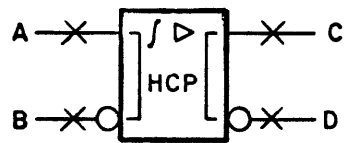
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J102

INTEGRATING AMPLIFIER - HCL

The HCL circuit converts a rectified signal input to a DC output that is an average value of the input signal waveform.

The integrating elements are NR2, NR3, and NC1. The analog signal (rectified waveform) is entered at input A. With digital voltage control at input B, QN can be turned on which would bypass NR2. This would leave (NR3) X (NC1) to determine the relatively short response time of the integrator. When QN is turned off, NR2 is included in the integrating circuit and the (NR2 + NR3) X (NC1) long response time results. QP (element 531) is an operational amplifier connected in a voltage follower mode of operation and acts as a buffer amplifier. NC3 is a compensation capacitor for QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J106

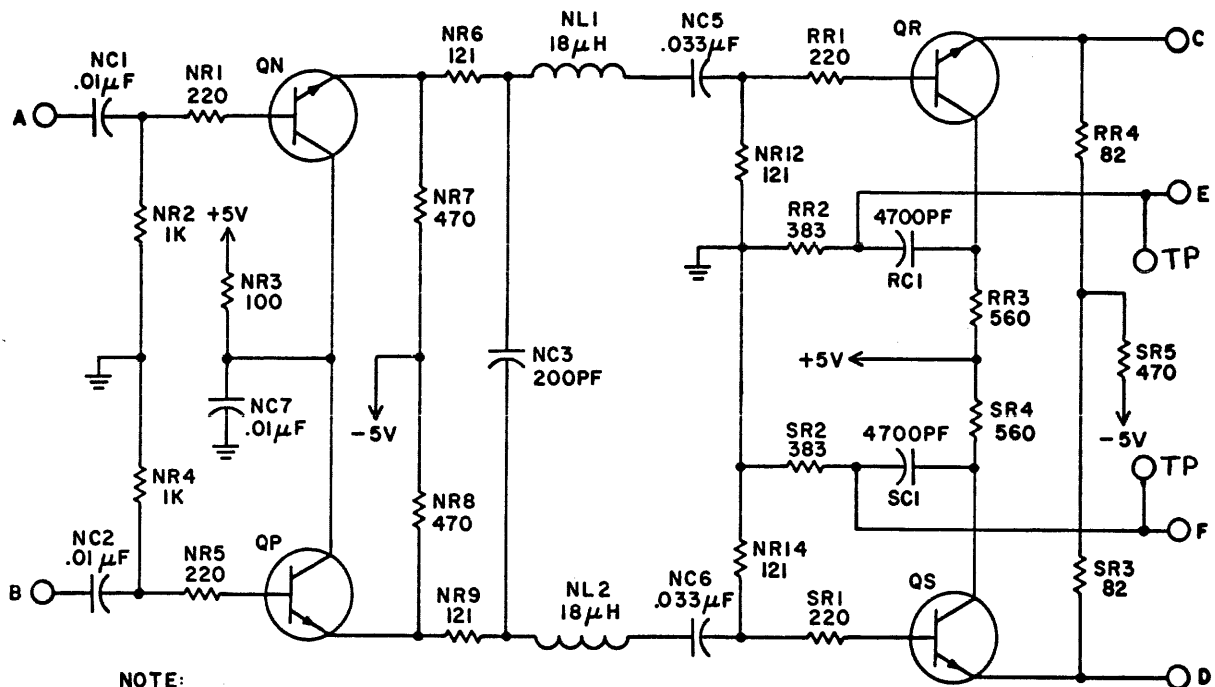
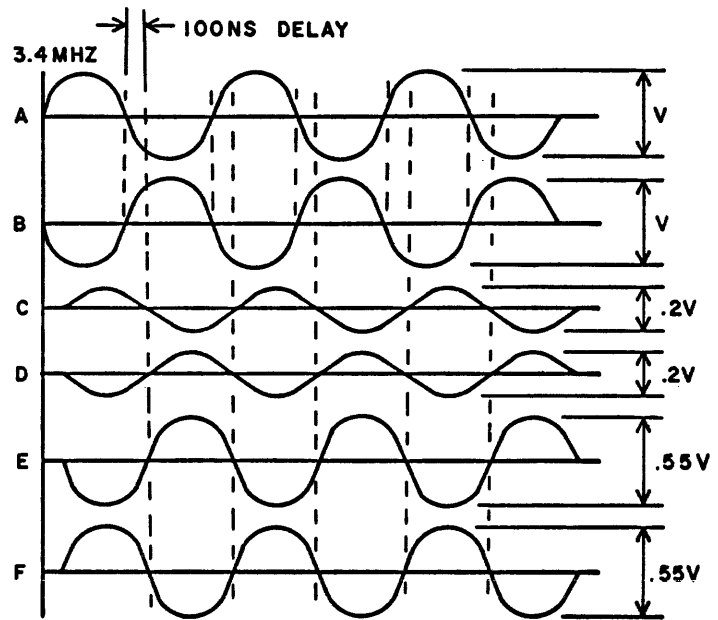
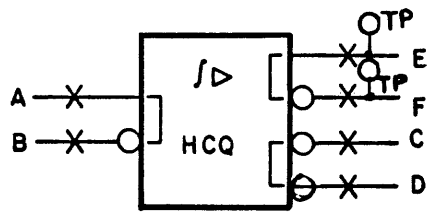
LOW PASS FILTER - HCP

The HCP circuit is a low pass differential filter with a buffer amplifier input (emitter followers). The filter provides attenuation of high unwanted frequencies (noise) in the read back signal with a linear phase response over the frequencies concerning read data.

NL1, NL2, NC3, NC4, NL3, and NL4 make up the differential filter with outputs at C and D. NR9 and NR10 are terminating (impedance-matching) resistors for the filter. NR5 and NR6 are impedance matching resistors to the input of the filter.

QN and QP with their emitter and base resistors form the buffer amplifiers for driving the relatively low input impedance filter.

The upper cutoff frequency of the filter is approximately 5.5 MHz (media compatible data rate of 6.44 MHz). The signal attenuation from inputs A, B, to outputs C, D is about 50% at 1 MHz.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J112A

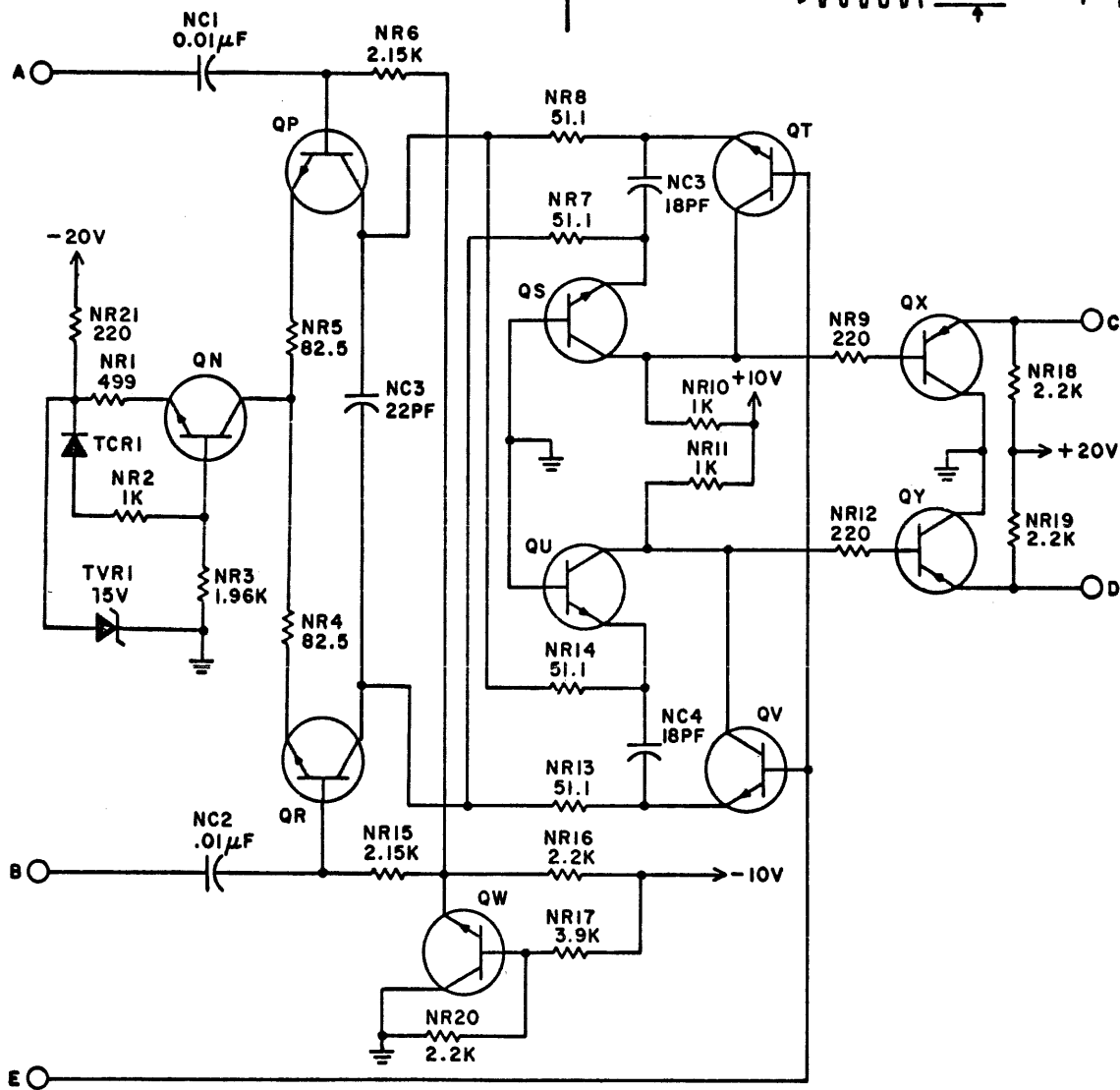
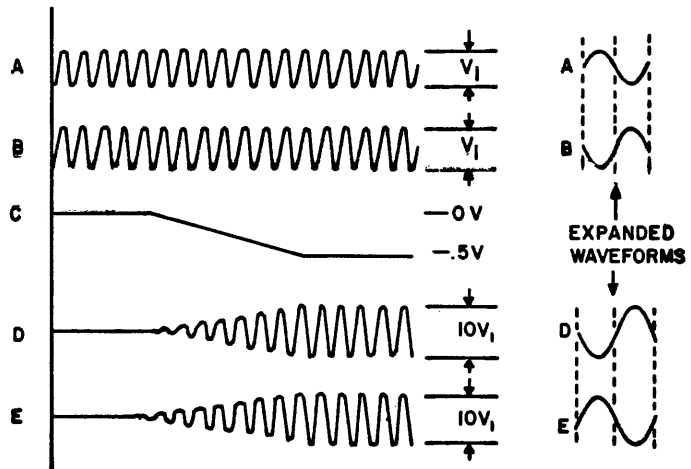
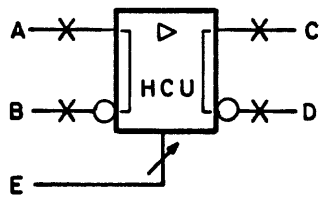
FILTER AND AMPLIFIER - HCQ

The HCQ circuit is a differential, 2 pole low pass filter followed by a differential amplifier with a gain of approximately 2.5.

NL1, NC3, and NL2 make up the 2 pole low pass filter. The upper cutoff frequency is approximately 2.5 MHz for media compatible data rate (6.44 MHz). NR6, NR9, NR12 and NR14 are impedance matching resistors for the filter.

QN and QP are buffer amplifiers (emitter followers) for driving the relatively low impedance filter.

QR, QS, and their associated circuitry perform dual roles as differential buffer amplifiers (emitter followers) and as differential amplifiers. Outputs C and D are the buffered outputs that connect to level detection circuitry with further amplification. Outputs E and F are amplified outputs which connect to a zero cross network (low resolution channel). This signal channel is amplified to make up for the attenuation loss of the filter. The gain of the amplifier is largely determined by the ratio of $RR2//RR3$ to $RR4$ and $SR2//SR4$ to $SR3$.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J115B

AGC AMPLIFIER - HCU

The HCU circuit is a differential amplifier with gain controlled by a negative voltage at input E.

QP and QR are amplifying transistors with their maximum gain determined by the ratio of NR10 to NR5 and NR11 to NR4.

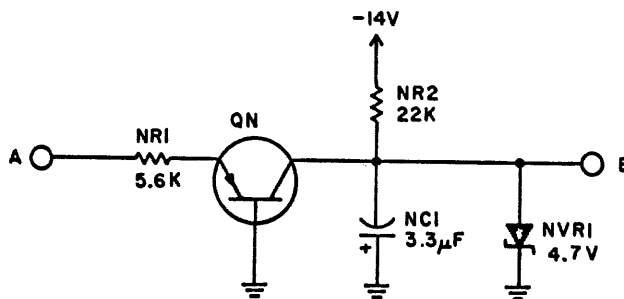
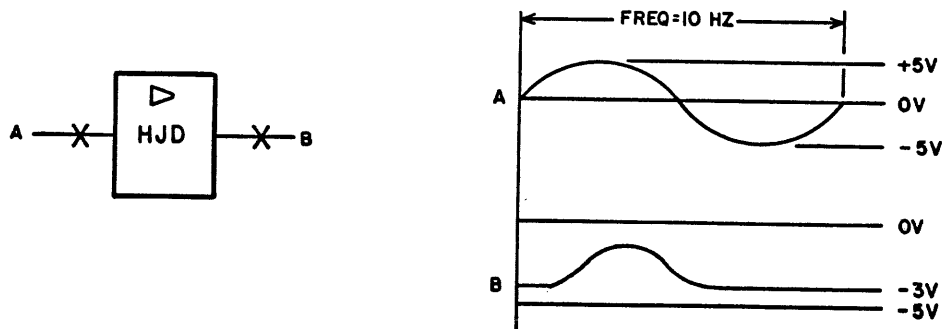
Common base amplifiers, QS, QT, QU, and QV pass amplified current signals to resistors NR10 and NR11. QS and QT pass out of phase signals to collector resistor NR10. Likewise, QU and QV pass out of phase signals to collector resistor NR11.

Control voltages on the bases of QT and QV control circuit gain. With 0 volts for control voltage, QS, QT, QU, and QV turn on equally, causing out of phase voltage to cancel, leaving a net output or gain of 0 volts. Increasing the control voltage negatively starts turning off QT and QV causing the amplifier gain to increase. Turning off QS, QT, QU, and QV requires that the control voltage be approximately -0.5 volts, which allows an amplifier gain of 10.

Emitter followers QX and QY provide low output impedance.

QN, NR1, NR2, NR3, and TCR1 make up a current sink network which controls the collector current of QP and QR.

NR21 and TVR1 form a -15 volt regulated voltage for the current sink circuit.



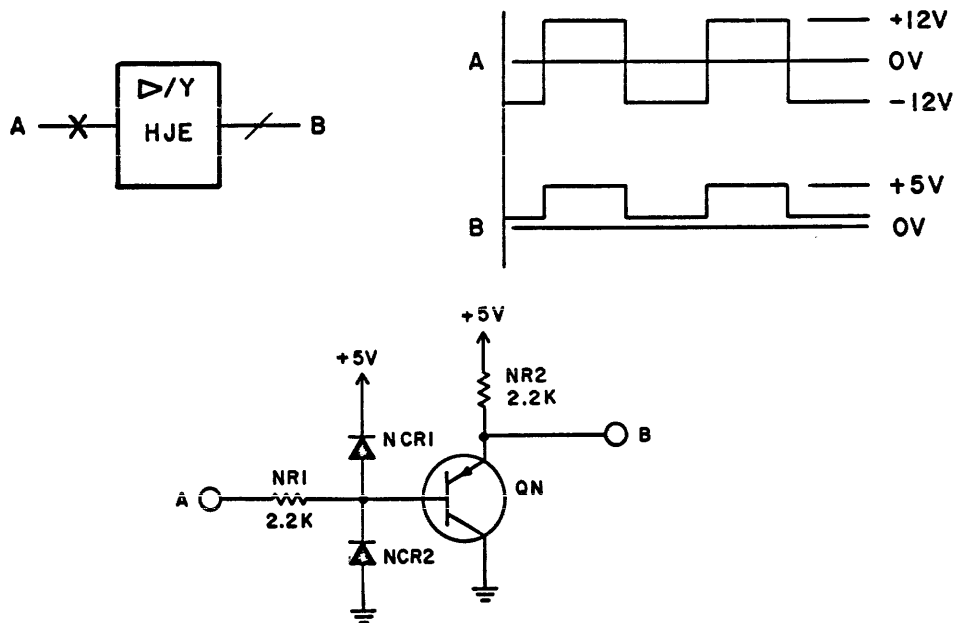
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY

6T167A

AMPLIFIER/LEVEL TRANSLATOR - HJD

The HJD circuit is an amplifier that provides a half-wave rectifier, shifted output signal.

The output signal at B increases in a positive direction from a -3 vdc level. The output signal controls a N-channel JFET in an AGC loop that regulates the amplitude of the fine position servo signal.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

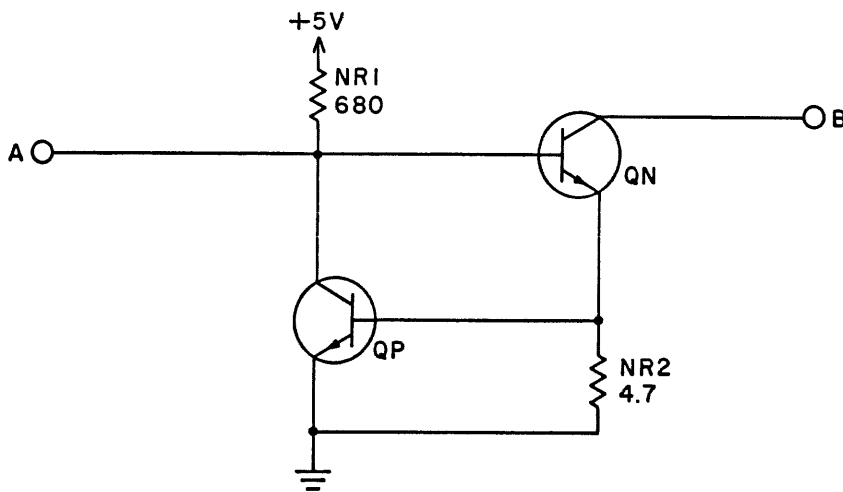
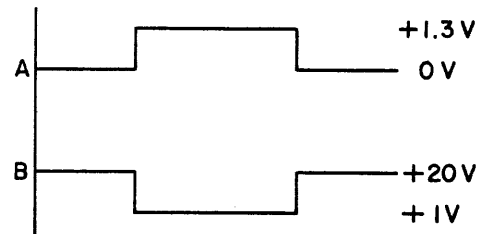
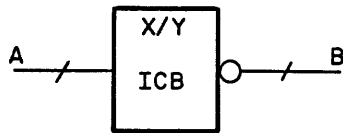
6T166A

LEVEL TRANSLATOR - HJE

The HJE circuit converts the output of an operational amplifier to a standard logic level.

When input A is at -12 volts, transistor QN is on. Diode NCR2 limits the input voltage at the base of QN to approximately -0.7 volt. Since the base to emitter voltage of QN is +0.8 volt, output B is at a level of approximately +0.1 volt.

When input A switches to +12 volts, QN becomes reverse biased and output B approaches +5 volts. The base voltage of QN is limited to approximately +5.7 volts by diode NCR1.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T148

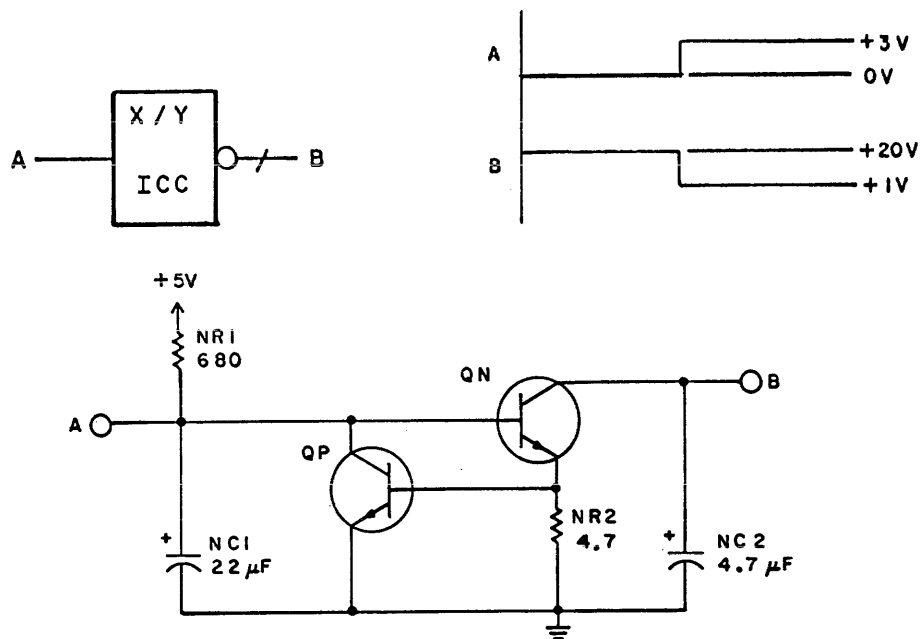
LAMP DRIVER - ICB

The ICB circuit drives a lamp which terminates at +20 volts. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

QP and NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

When a high, logic 1, is provided to the circuit input, transistor QN (and the lamp) turns on.

A low (logical 0) at the input turns QN off causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off.



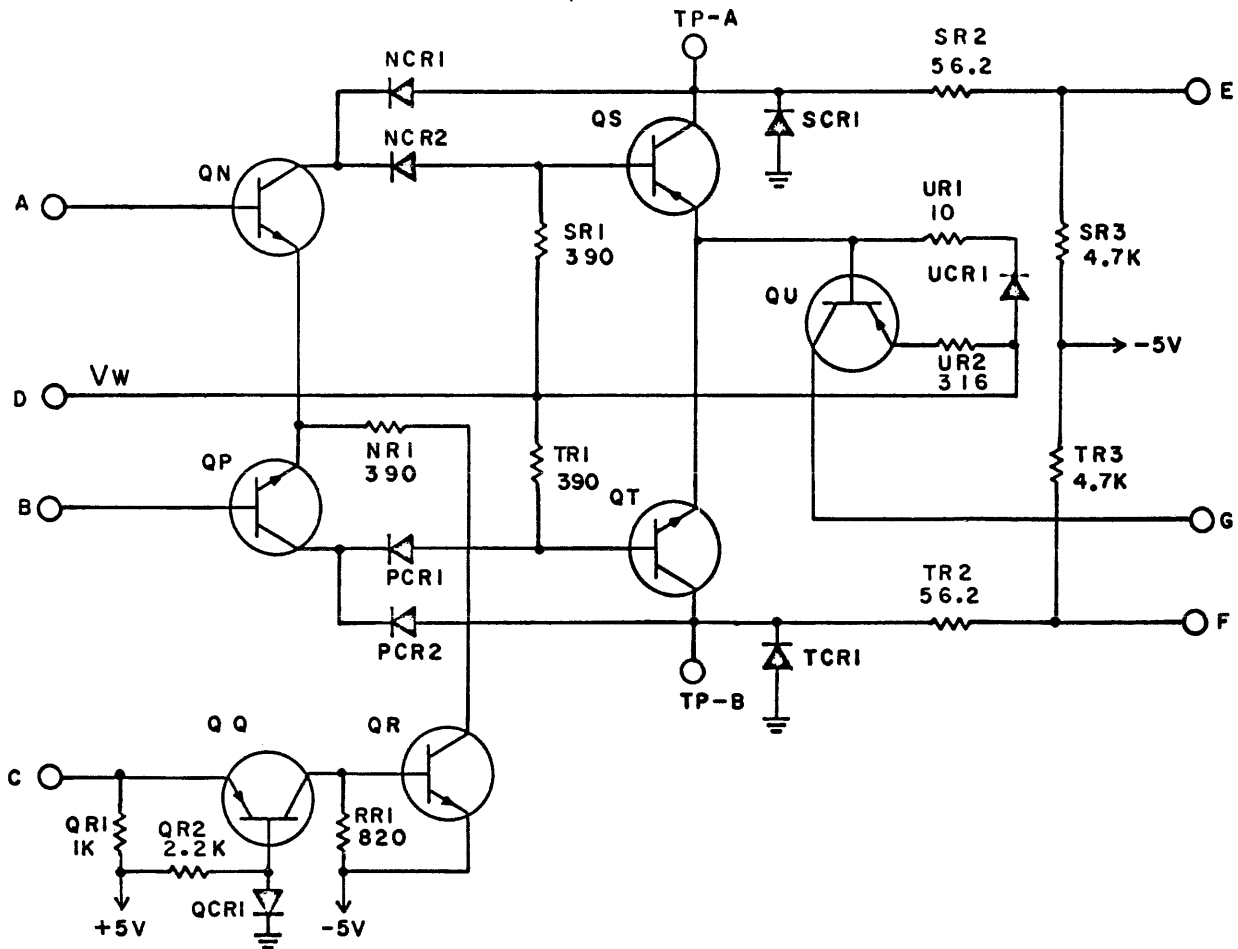
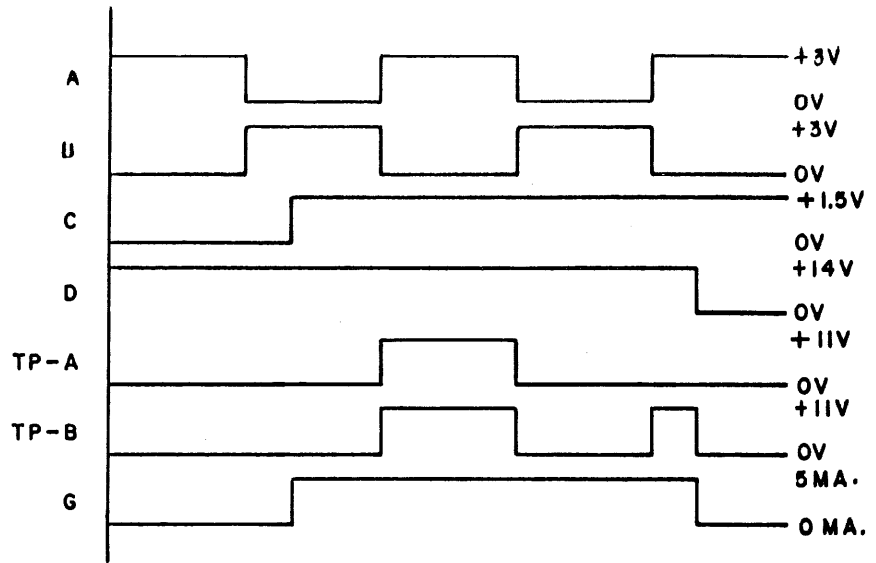
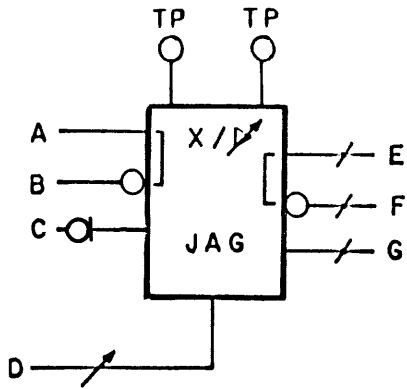
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J25

LAMP DRIVER - ICC

The ICC circuit drives a lamp which terminates at +20 volts. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

When a high, logic 1, is provided to the circuit input, transistor QN (and the lamp) turns on. Transistor QP and resistor NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

A low, logic 0, at the input, turns QN off causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off. Capacitors NC1 and NC2 are used to slow the rise and fall times of the output voltage swings at B.



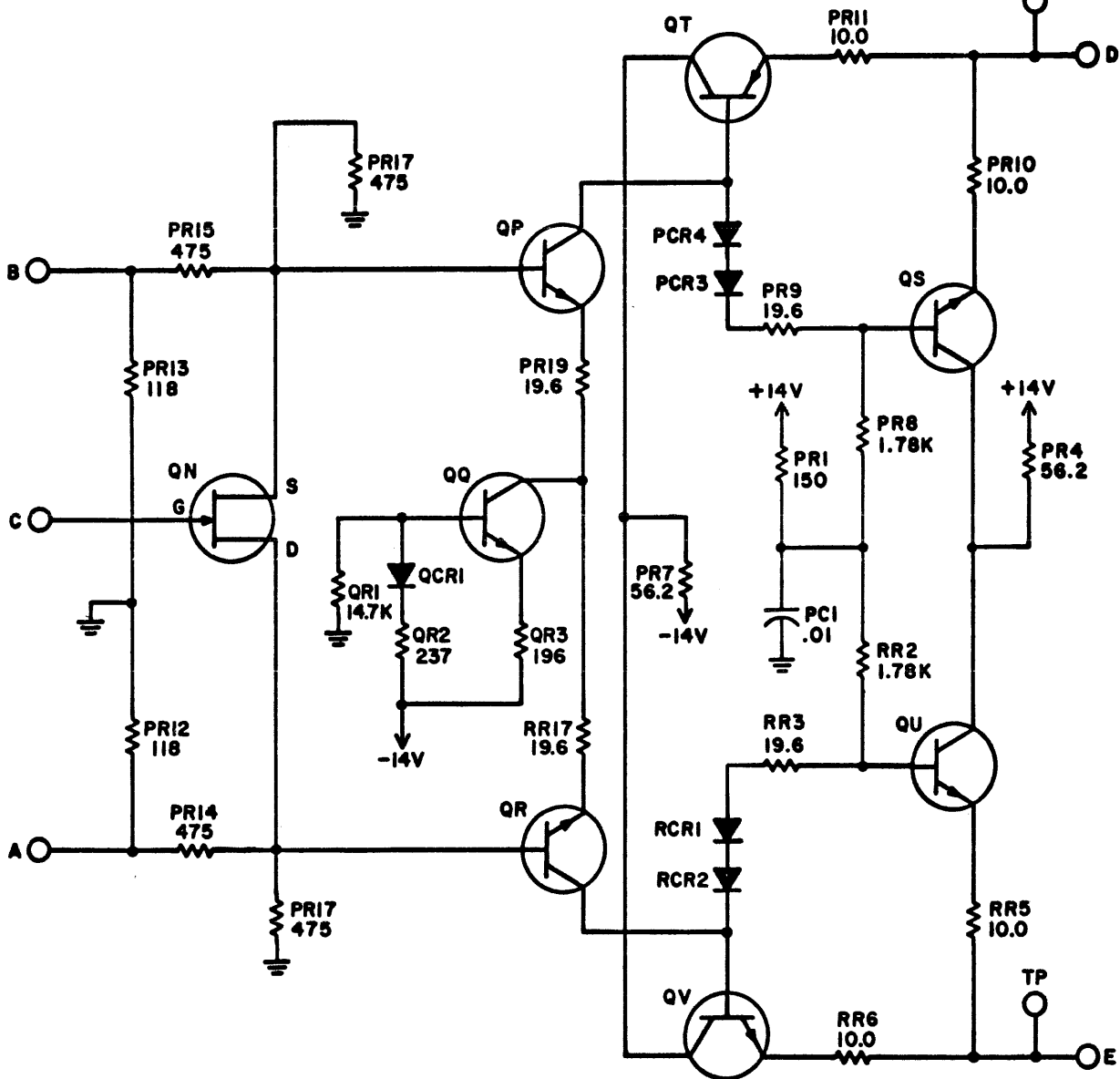
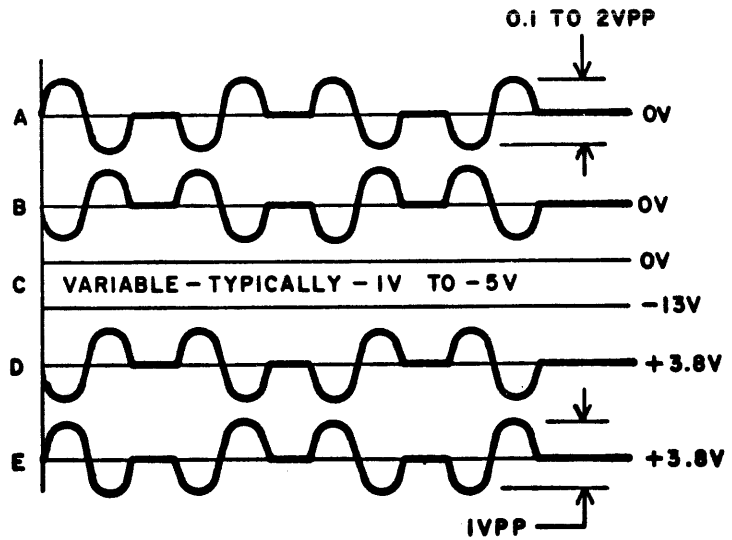
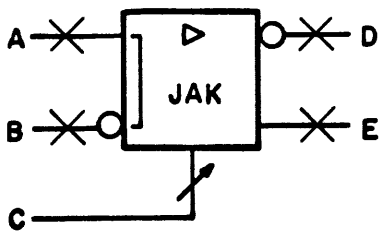
NOTE:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J26
2. WAVEFORMS ABOVE ARE FOR REFERENCE ONLY AND VALID ONLY WHEN OUTPUTS E AND F ARE CONNECTED TO A READ/WRITE HEAD WITH CENTER TAP TO GROUND.

WRITE DRIVER - JAG

Write driver JAG is a differential voltage switch which converts voltage (across termination resistors) to current to drive a differential recording head.

Circuit operation is dependent upon signal level shifter QQ converting an open collector TTL output of "0" or "1" to turning QR "off" and "on". With QR on, -5 volts flows through QR and NR1 to supply current for the differential switches QN and QP. With input A high and B low, QN turns on and QP is off. QN turning on causes QS to turn on which applies a voltage (from D through UCR1 and UR1) to termination resistor SR2 and current to output E. When A is low and B is high QN and QS turn off, QP and QT turn on applying voltage to termination resistor TR2 and current to output F. Current sensing network UR1, UR2, UCR1 and QU supply current at G which is used for fault detection. NCR1, NCR2, PCR1, PCR2 prevent QS and QT from saturating when the write driver is turned off. SCR1, SR3, TCR1, and TR3 provide back biasing of the write matrix diodes during a write operation.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J107

AGC AMPLIFIER – JAK

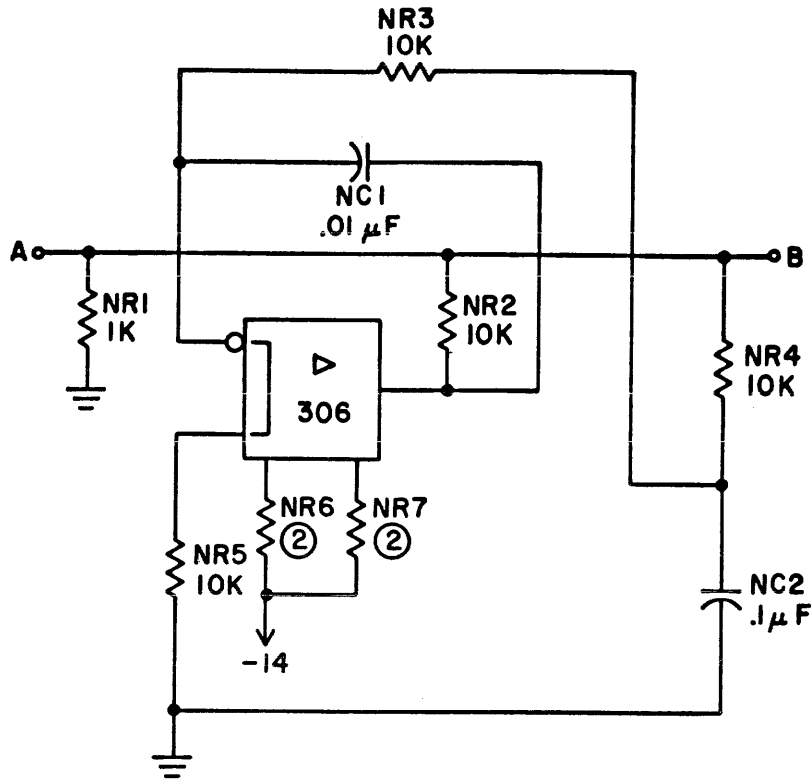
The JAK circuit amplifies the differential dibit signal read from the servo head. This AGC amplifier is a differential in, differential out amplifier with a variable input attenuator.

The differential signals are applied to inputs A and B. Resistors PR12 and PR13 are line terminating resistors.

AGC action is provided by input C. This control voltage, generated farther down the servo signal chain, is proportional to the amplitude of the dibit signals. The stronger the signal, the less negative the AGC voltage. Resistors PR15, PR17, PR14, and PR16, along with N-JFET QN form a balanced differential attenuator. The more negative the input, the greater the effective source-to-drain resistance across QN. This reduces the attenuation of the network. The voltages available at C can vary from 0V to -13V. At 0V, the D-S resistance is about 40 ohms; practically shorting out the input to reduce the net gain available. At -13V, the D-S resistance is about 50 megohms, permitting full gain. In actual practice, the servo action of the loops holds input C at about -1V to -5V.

Transistors QP and QR form the inputs to a differential amplifier. Transistor QQ functions as a high-resistance common current source; diode QCR1 provides temperature compensation. The resultant constant-current source greatly reduces common mode error.

Transistor pairs QS/QT and QU/QV form unity-gain, noninverting power drivers for outputs D and E.



NOTES:

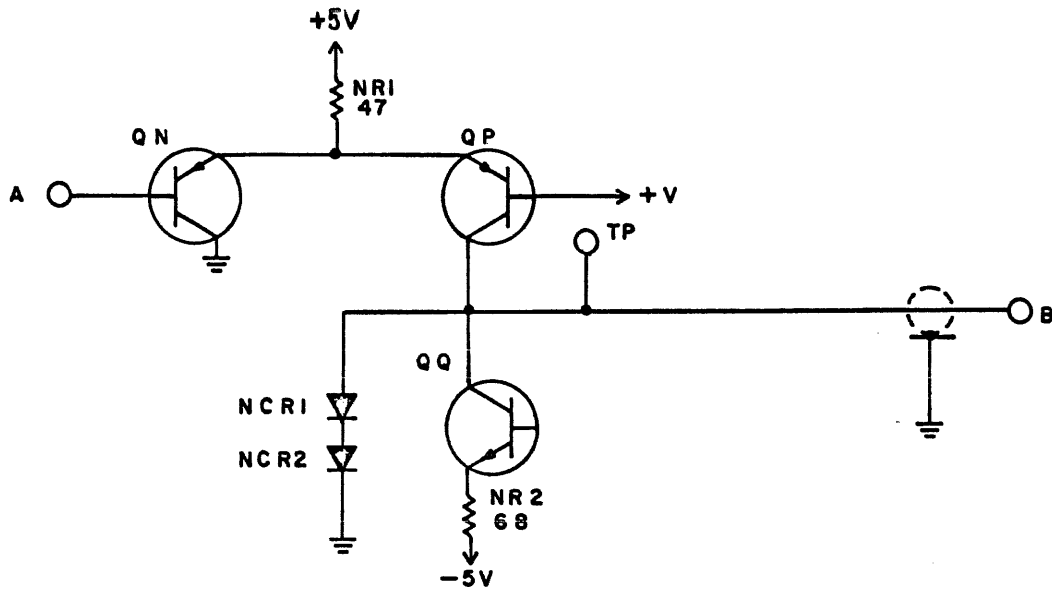
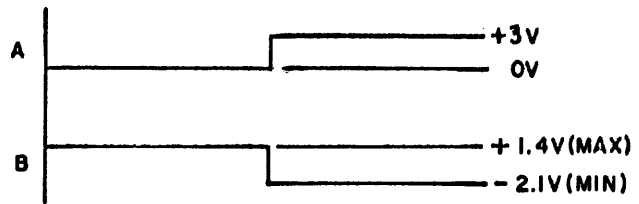
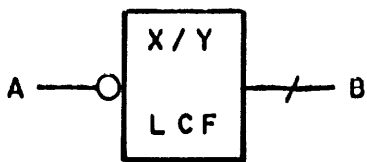
- 1 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② VALUES CHOSEN PER CIRCUIT REQUIREMENTS.

7J199

Auto Null Circuit - JAM

The JAM circuit provides a DC null for the AC signal on line AB. This circuit compensates for a fluctuation in DC reference of the AC signal due to temperature and chip-to-chip parameters.

The operational amplifier senses the DC level on line AB and compares this voltage level against a zero volt reference. It then supplies the proper DC current to maintain a DC null on line AB.

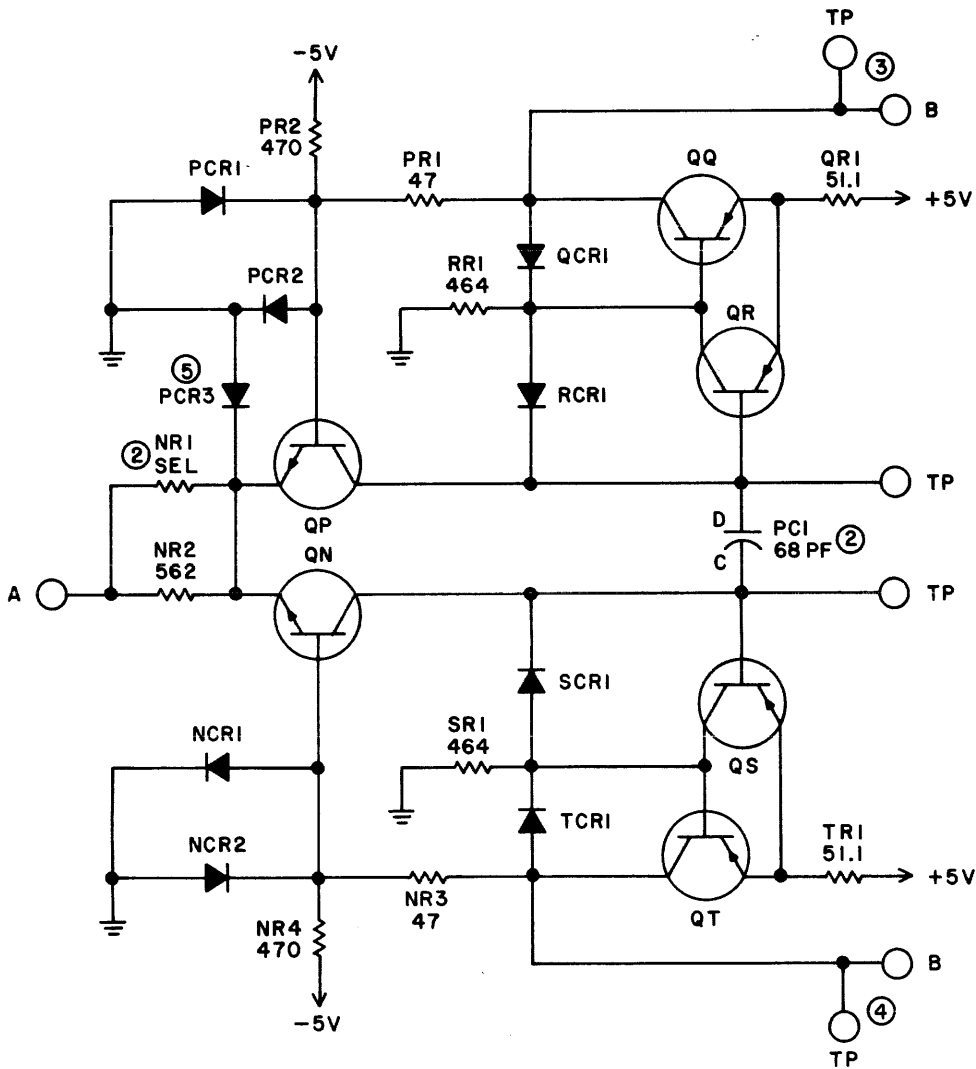
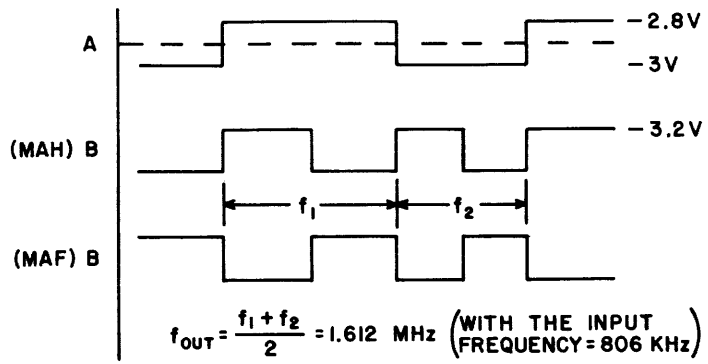
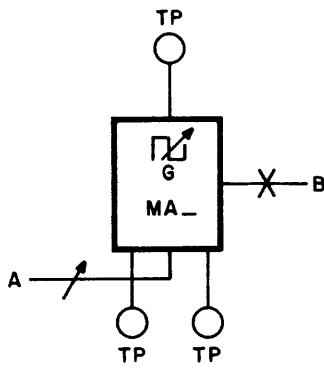


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J27

TRANSMITTER - LCF

The LCF circuit provides a sink current at output B when the input at A is low. When the input is high, the output current becomes a source current. Input A is driven by a standard TTL logic gate. Resistor NR1 and transistors QN and QP operate as a switch. When the voltage at A goes below +V, transistor QN turns on and QP turns off. The constant current circuit, QQ and NR2, sinks current through the line and terminator and drives the voltage at the collector of QQ negative. External resistors and Zener diodes between the plus and minus voltage supply lines serve as a voltage divider common to all LCF circuits on a given card and provide bias voltage to the bases of QP and QQ. The sink current level is determined by -V, VBE of QQ, and NR2.

When the voltage at A goes above +V, transistor QN turns off and QP turns on. A source current is now developed by +V, VEB of QP, and NR1. The current level is such that it is greater than the sink current into QQ by an amount sufficient to drive the output positive. This positive voltage excursion is limited by diodes NCR1 and NCR2. Limiting is necessary to keep QP from saturating. Because of the nonsaturating mode of operation, the propagation delay through LCF is small. Accidental grounding of the test point or output of the circuit has no damaging effect on the circuit.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② VARIES WITH DATA FREQUENCY. THESE COMPONENTS CONTROL FREQUENCY.
- ③ OUTPUT LOCATED ON MAH CIRCUIT.
- ④ OUTPUT LOCATED ON MAF CIRCUIT.
- ⑤ DIODE PCR3 ON MAH ONLY.

7J28A

VOLTAGE CONTROLLED OSCILLATOR - MAF/MAH

The MAF/MAH circuit consists of two Schmitt trigger circuits (QQ, QR and QS, QT) and a differential switch/current limiter circuit (QN, QP, NR1, AND NR2). The values of capacitor PC1, resistors NR1 and NR2, and the input voltage, determines the output frequency of the circuit. Operating frequency is listed on the Logic Diagram (see Section 5).

For the following discussion, assume that voltage E3 is more positive than E2, E2 is more positive than E1, and E0 is the lowest voltage (refer to Figure 1).

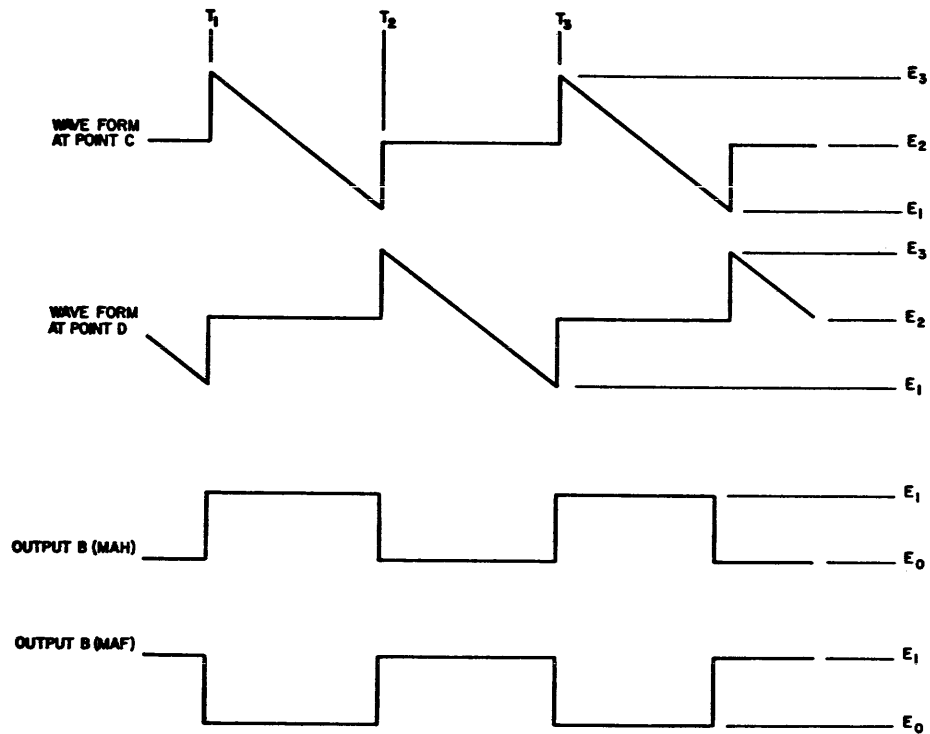


Figure 1

Assume that point C of PC1 is more positive than point D. At this time, QP and QS are both conducting and QT is off (base-emitter junction is reverse biased). The output voltage at B is high. The other half of the circuit (QN, QQ, and QR) is in the opposite state at this time.

The D terminal of capacitor PC1 is held low by the forward drop of the base-emitter junction of QR. Therefore, current through PC1 alters its charge linearly until the voltage at C reaches the high output voltage. At this point, the lower Schmitt trigger circuit (QS, QT) switches off and the output voltage at B goes to ground. QP now switches off and point C is driven rapidly positive by the forward biased base-emitter junction of QS.

At the instant that the lower Schmitt trigger circuit switched off, the voltage at point D was at E3. The sudden increase of point D to E3 potential reverse biases the base-emitter junction of QR and triggers the upper Schmitt trigger circuit. Therefore, QN and QQ turn on and draw current from terminal D of capacitor PC1. When the voltage at D reaches E1, the upper Schmitt trigger circuit switches off. QN switches off and point C is again raised to E3. This completes the multivibrator cycle and brings it back to the initial condition. The cycle is then repeated.

As input A becomes more negative the output frequency at B, increases linearly (refer to Figure 2).

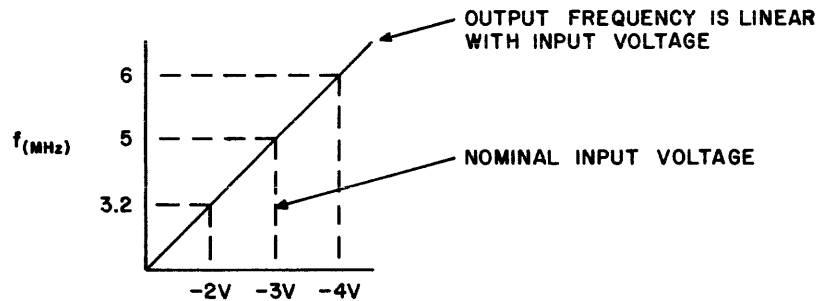
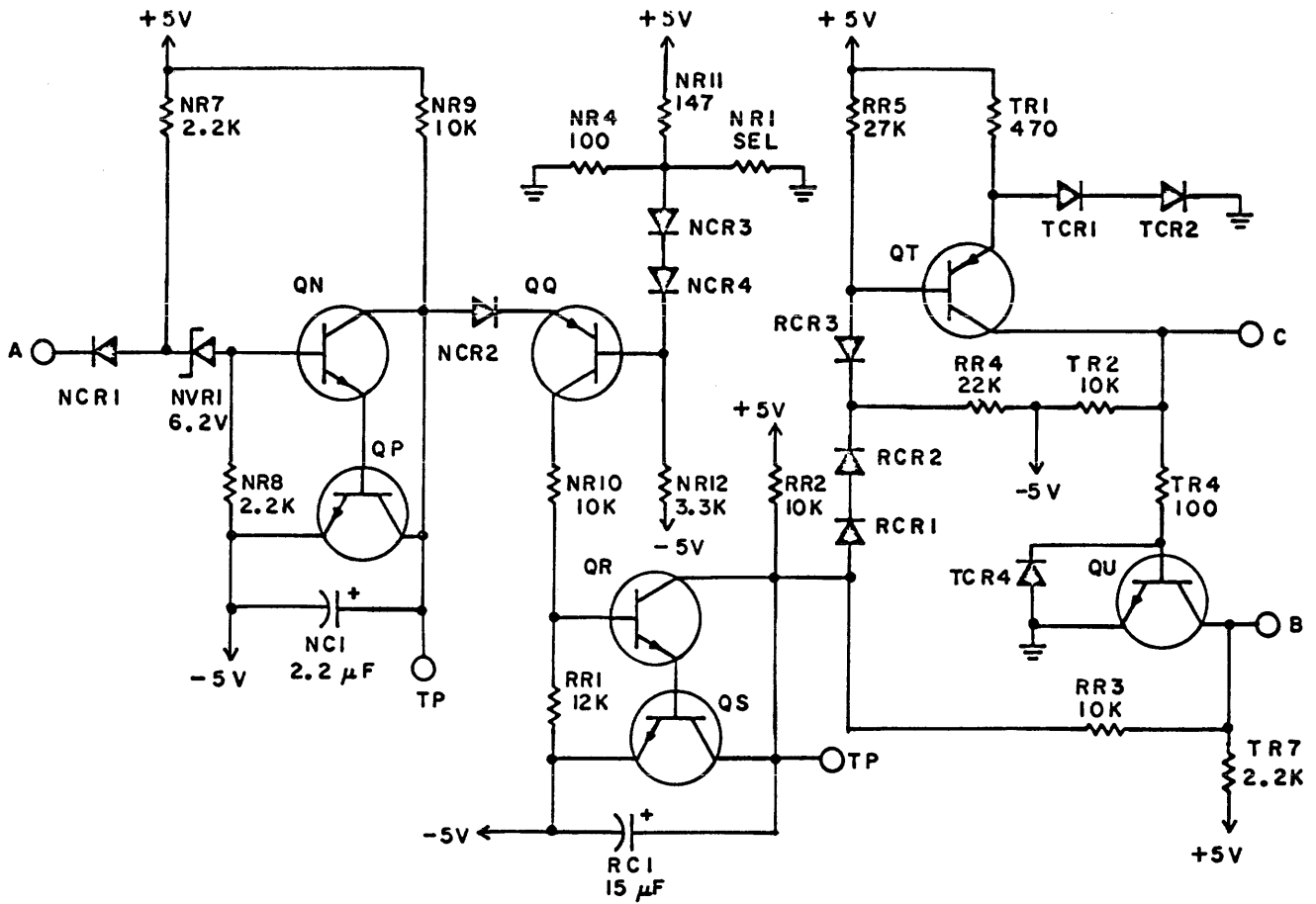
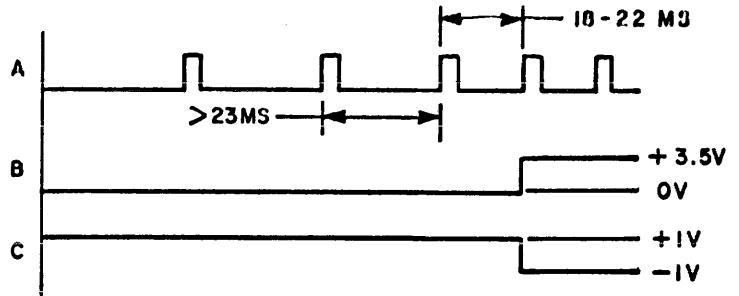
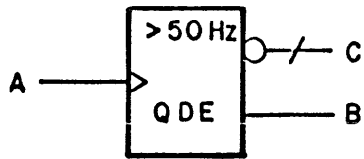


Figure 2

Diode PCR3 prevents the emitters of QN and QP from falling to a voltage that would cause both transistors to conduct when power is first applied. Such a condition would prevent the circuit from oscillating. Diodes QCR1, RCR1, SCR1, and TCR1 prevent the Schmitt transistors (QQ, QR, QS, and QT) from going into full saturation. This helps the circuit to oscillate at the higher frequencies.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J29

SPEED DETECTOR - QDE

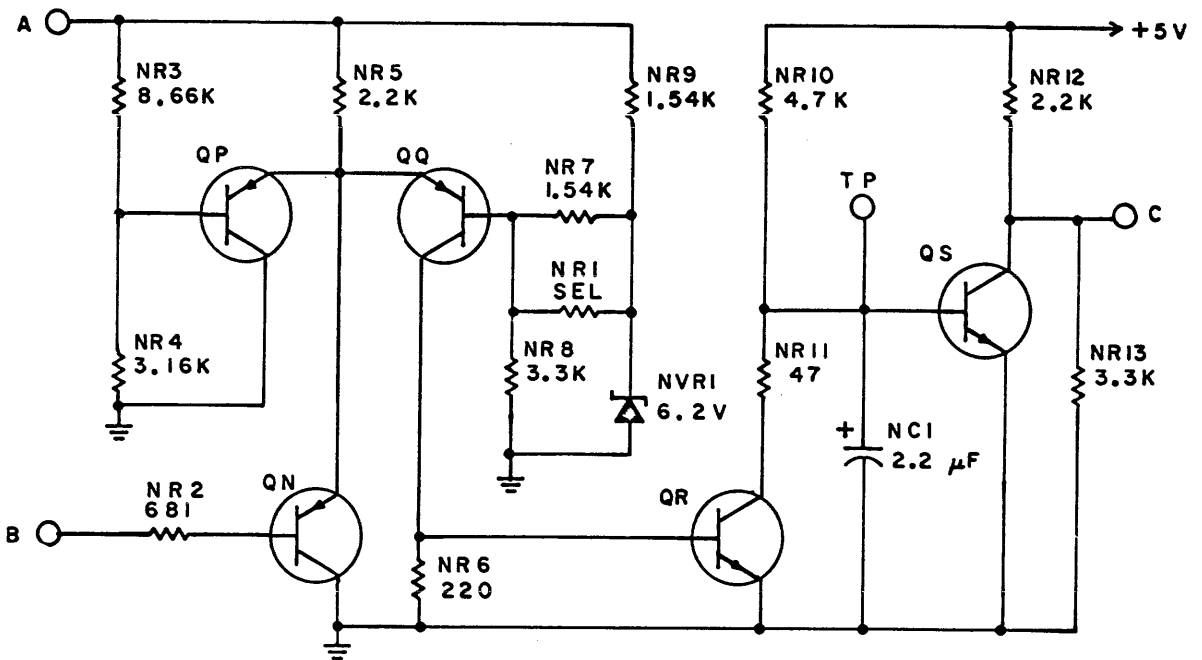
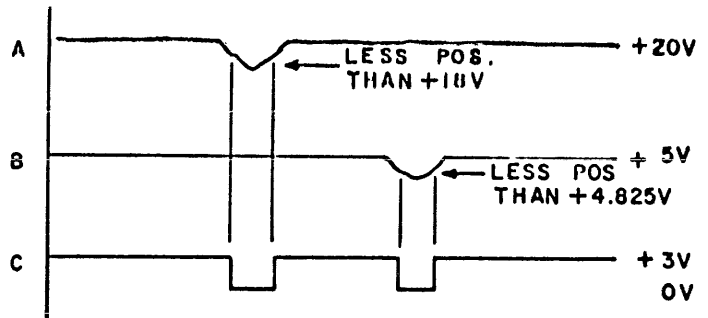
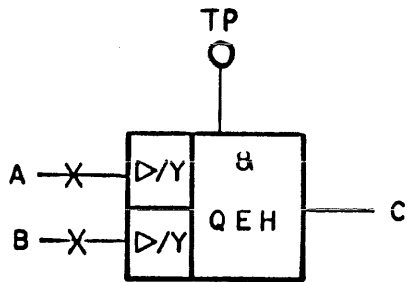
The QDE circuit monitors the sector pulses to determine whether or not the spindle is at a specified speed.

Each time a sector is sensed, a 55- μ sec pulse appears at input A. Transistors QN and QP conduct and completely discharge capacitor NC1 to -5v. When the pulse drops, NC1 begins charging through NR9. When the voltage on the collectors of QN and QP reaches the threshold of NCR2 and QQ, QQ turns on. This causes transistors QR and QS to conduct and discharge RC1. With QR and QS on, RCR1 and RCR2 are back biased and the voltage at the base of QT drops, turning QT on. The collector voltage of QT rises enough to turn QU on and the output voltage at B goes low to indicate a not up to speed condition.

If the disk pack is below speed, pulses at input A are at low repetition rate. Capacitor NC1 discharges and charges turning transistors QQ, QR, and QS off and on, respectively. This in turn causes RC1 to charge and discharge. Every time NC1 charges to the threshold, QQ, QR, and QS turn on and discharge RC1. This prevents RCR1 and RCR2 from ever becoming forward biased. As a result, QT remains on and the output at B remains low, indicating not up to speed.

When the disk pack reaches the required speed, the charging time of NC1 is such that the charging voltage on NC1 remains below the threshold of NCR2 and QQ, keeping QQ, QR, and QS off. Now RC1 has time to charge and when RCR1 and RCR2 become forward biased, the voltage at the base of QT increases sufficiently for QT to turn off. The resulting reverse bias on QU turns QU off and the output at B goes high. The feedback through RR3 reduces the charge time of RC1 and the switchover goes to completion with the high output at B indicating an up to speed condition. The output signal at C is always complementary and is used by a relay driver circuit.

The voltage on the base of QQ is determined by the voltage divider comprised of NR1, NR4, NR11, NR12, NCR3, and NCR4. Resistor NR1 is a test selected resistor to fine tune the threshold of NCR2 and QQ and to compensate for the tolerances of NR9 and NC1.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J30

VOLTAGE CHECKER - QEH

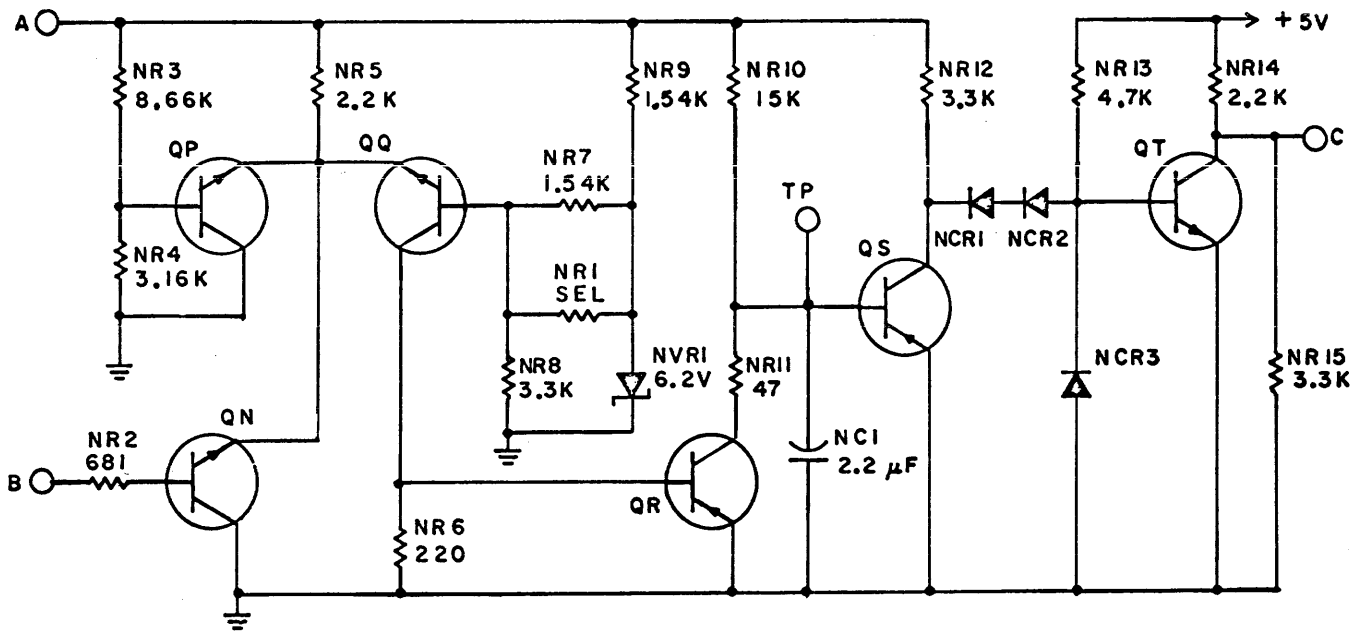
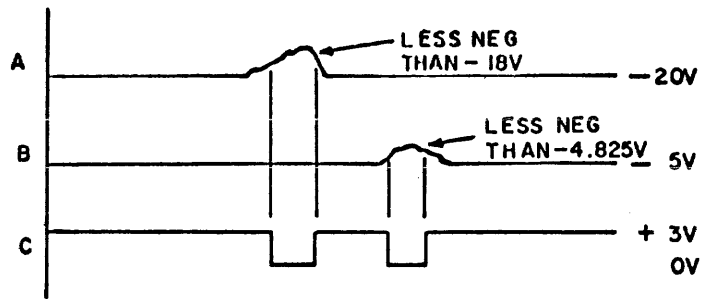
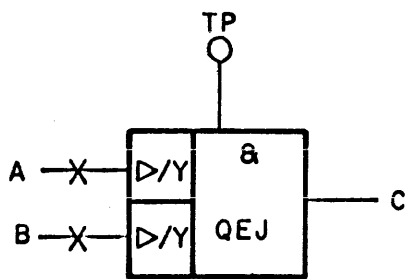
The QEH circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

1. +5 volt supply becomes less positive than +4.825 volts, or
2. +20 volt supply becomes less positive than +18.0 volts

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at +4.825 volts. If the positive supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting positive level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop to near zero volts switching QS off and establishing a +3 volt level at output C.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less positive than the base voltage on QQ (+4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS positive and turning it on. As a result, output C approaches a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the +20 volt input at A goes less positive than +18 volts, transistor QP turns on and output C goes low.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J31

VOLTAGE CHECKER - QEJ

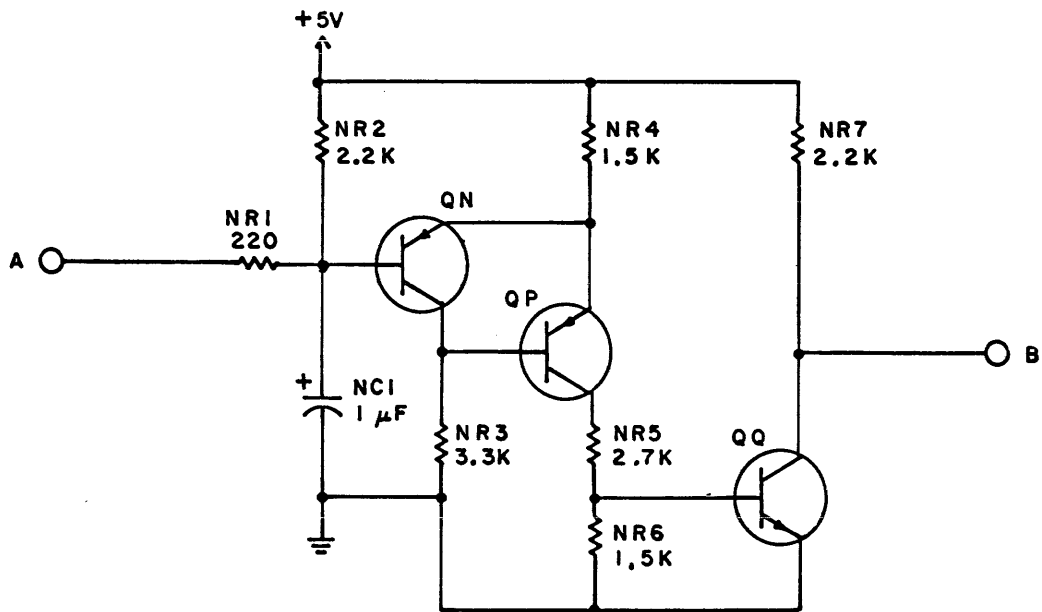
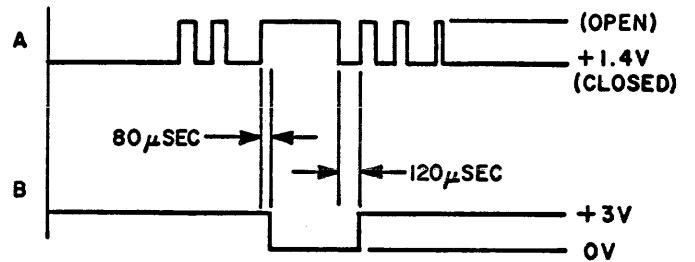
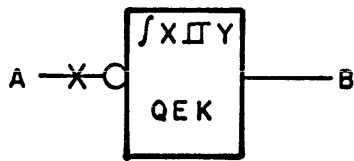
The QEJ circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

1. -5 volt supply becomes less negative than -4.825 volts or
2. -20 volt supply becomes less negative than -18.0 volts

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at -4.825 volts. If the negative supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting negative level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop to near zero volts switching QS off and developing a reverse bias across diode NCR3. This turns off transistor QT and sets the output at C to +3 volts.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less negative than the base voltage on QQ (-4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS negative and turning it on. Diodes NCR1 and NCR2 raise the base voltage of transistor QT to a point where it turns on and causes output C to approach a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the -20 volt input at A goes less negative than -18 volts, transistor QP turns on and output C goes low.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J32

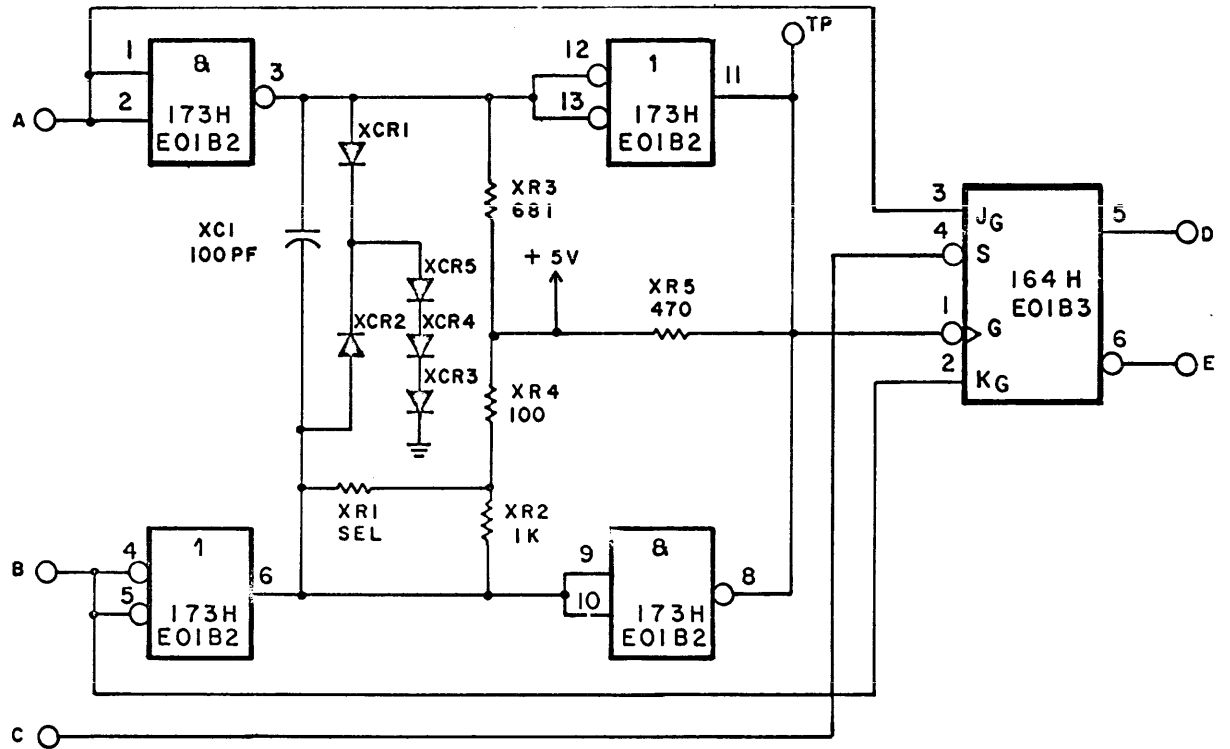
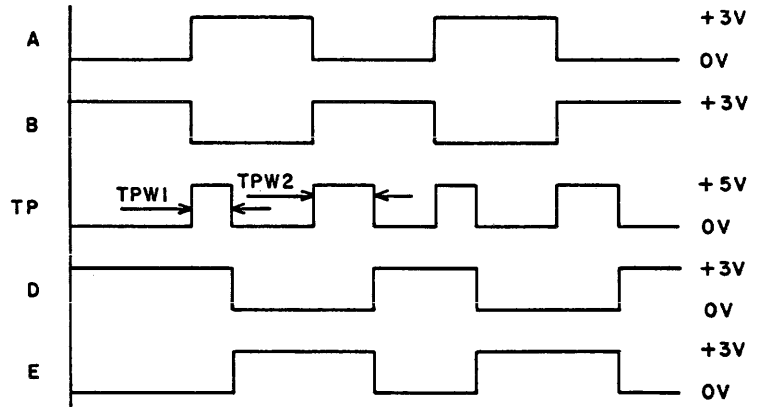
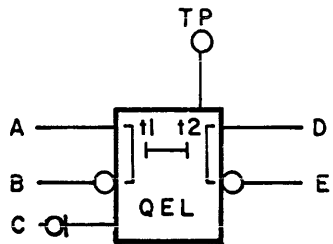
SWITCH RECEIVER - QEK

The QEK circuit produces a "1" (+3v) output at B when the solid-state switch connected to input A is closed. When the switch is open a "0" (0v) appears at output B.

A transistor switch is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN turns off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR5. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage flow through NR1, the switch, and across NC1 increases rapidly because of the short time constant of NR1 and NC1. Any spurious switching that precedes the state change increases the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP decreases and QP begins to turn off. As QP turns off, the current through NR4 decreases due to the higher lead resistance (NR3) of QN compared with QP (NR5). The current drop through NR4 causes a decrease in the voltage drop across NR4. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is turned off. With QP off, the base of QQ is near ground, causing QQ to turn off. This allows the +5v supply to flow through NR7 to output B raising the output to +3v, "1".

When the transistor switch driving the input is not conducting, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Again, any preliminary switching that precedes the actual state change will hold NC1 well below the switching level of QN. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of the positive feedback. The output then becomes "0".



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7 J33

SYMMETRY RESTORER-QEL

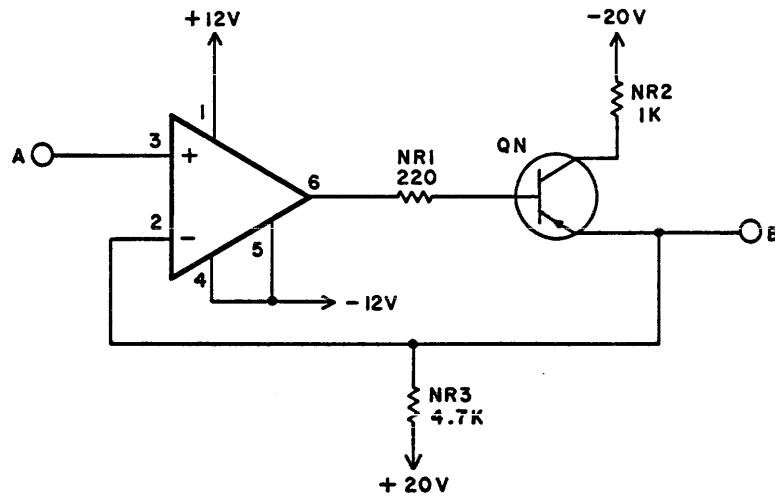
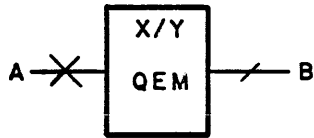
In a write driver chain where complementary TTL input signals become asymmetrical by ± 8 nsec, the QEL circuit is used to restore symmetry to these signals.

A "0" TTL level at point C will set the flip-flop insuring the same start-up conditions on inputs D and E when released by a "1" level at C.

With input A high and B low, pin 3 of 173H goes to ground and pin 6 goes to +5v through XR1, XR2, and XR4. The ground transition at pin 3 is coupled through XC1 and forces a negative spike on pin 6. Starting from a negative potential pin 6 voltage rises toward +5 volts at an RC time rate determined by XC1 and the combination of XR1, XR2, and XR4. This causes the pulse to be delayed in reaching the switching threshold of the following inverter (pins 9 and 10), and produces a positive pulse at "ored" pins 8 and 11 for the duration of the delay. The negative edge of this pulse triggers pin 1 of flip-flop 164H changing the state of outputs D and E.

The opposite conditions on inputs A and B (A low and B high) form the positive pulse at "ored" points 8 and 11 which is determined by the RC combination of XC1 and XC3. Thus, the negative edge which triggers the J-K flip-flop is controlled by alternate RC time constants, one of which can be adjusted by selection of XR1 with reference to the other resistors.

Diodes XCR1, XCR2, XCR3, XCR4, and XCR5 clamp the positive excursion on pins 3 and 6 at +2.5 volts to make delays insensitive to frequency variations up to data rates of 4 MHz.



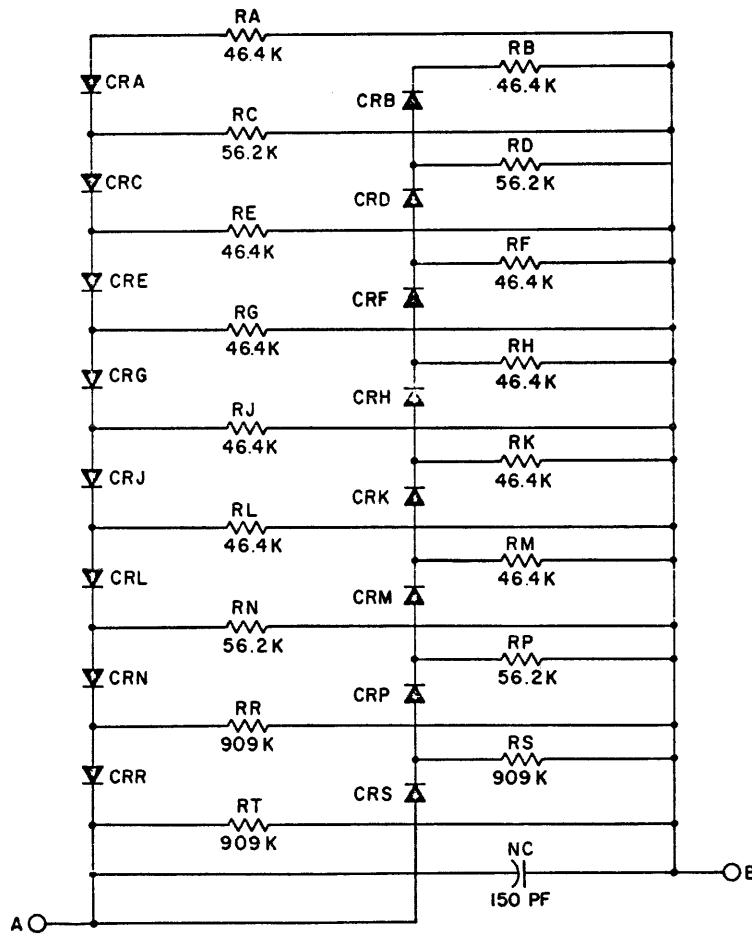
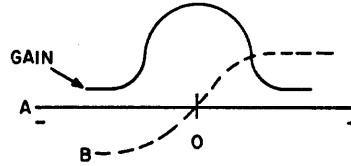
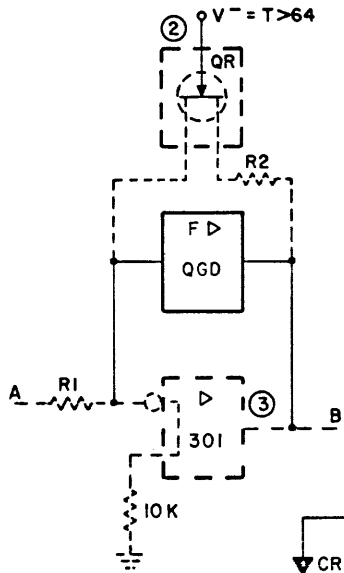
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J100

VOLTAGE FOLLOWER – QEM

The QEM circuit consists of an operational amplifier in a voltage follower configuration. A PNP emitter follower (QN) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QN in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QN.

NR3 provides a minimum current to the emitter of QN under no load conditions. NR2 is a current limit resistor. NR1 is a buffer resistor to eliminate possible oscillation tendencies.



- NOTES: 1 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
 ② PART OF GJB CIRCUIT (REF ONLY), NEG INPUT TURNS QR OFF.
 ③ SHOWN FOR REFERENCE ONLY.

6Y139A

FUNCTION GENERATOR - QGD

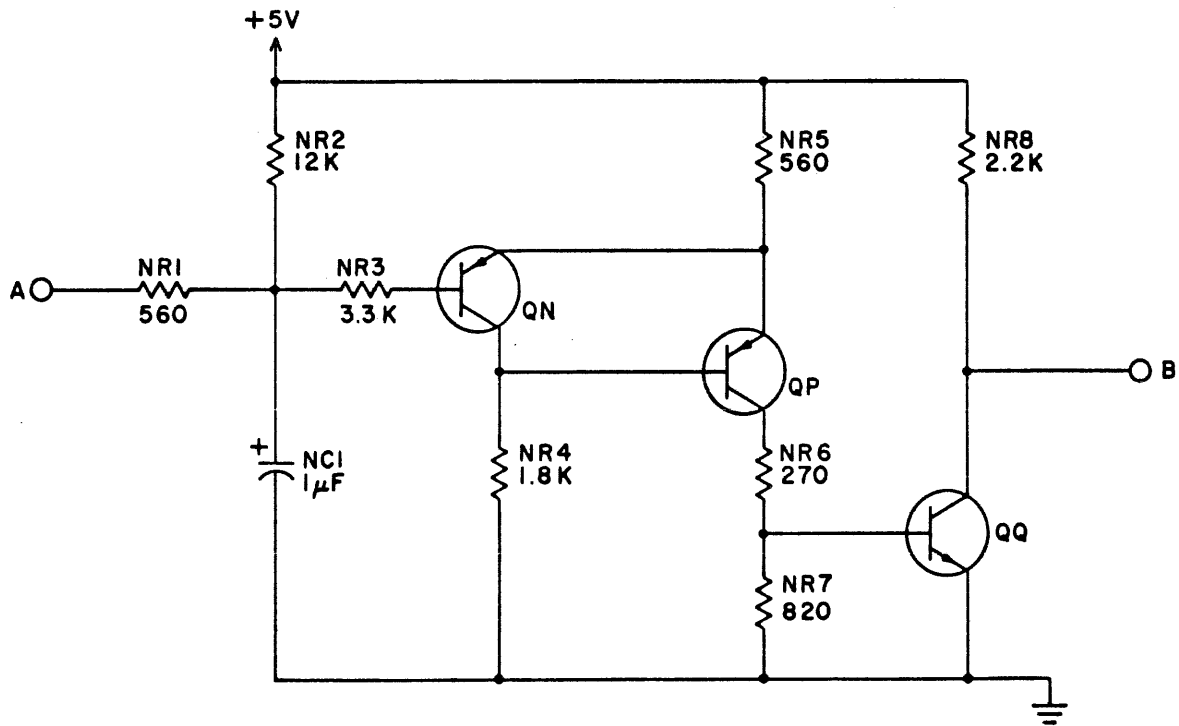
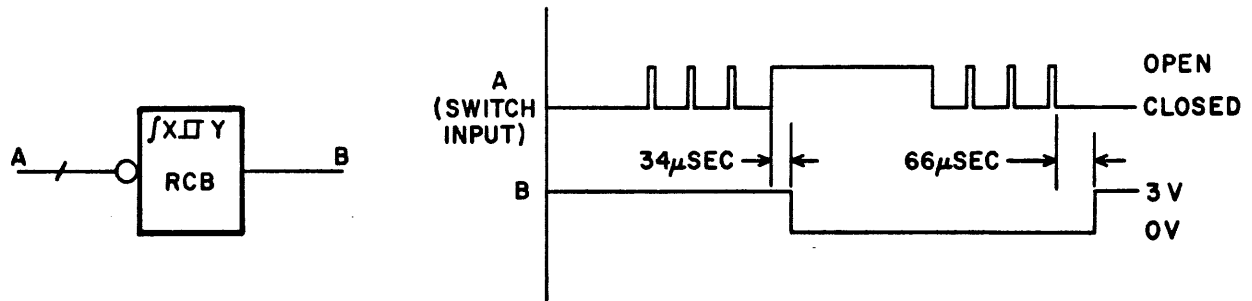
The QGD circuit is a nonlinear feedback network used as the gain determining element of an operational amplifier.

In actual circuit use, the op amp generates a voltage proportional to the desired velocity of the read/write head positioner. The amplitude of this signal is the analog representation of the number of tracks to go (position error) and will be compared with velocity to achieve maximum deceleration control without overshoot of the positioner when on cylinder ($T=0$).

Field effect transistor QR is part of the GJB circuit to function as a logic switch. Prior to $T=64$, the input is at ± 10 volts with the switch open. With this input voltage, the voltage drops across all of the forward-biased diodes are overcome so that the equivalent resistance of the parallel resistor network in the QGD circuit is about equal to the input resistor R1. The gain is, therefore, unity (output is 10 volts, inverted from input).

When there are less than 64 tracks to go, the input to the gate of QR changes from a negative voltage to ground potential. QR turns on, adding R2 into the feedback loop. R2 has the same resistance as R1. This reduces the feedback resistance to one-half of its former value, thus reducing the gain by 50% (output = ± 5 volts).

After $T=32$, input A begins to decrease in proportion to the remaining position error. The QGD/op amp circuit maintains an output voltage for optimum deceleration. The optimum deceleration is obtained by taking the square root of the position signal and comparing it with the velocity signal. The resistor-diode circuits in the QGD supply the position signal: as the input is reduced, the output is reduced correspondingly. Fewer diodes conduct, removing some of the parallel resistors in the QGD circuit from the feedback loop. This increases the effective feedback resistance, increasing circuit gain. Gain is maximum (but not greater than one) when the output is below about ± 0.5 volt.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T148

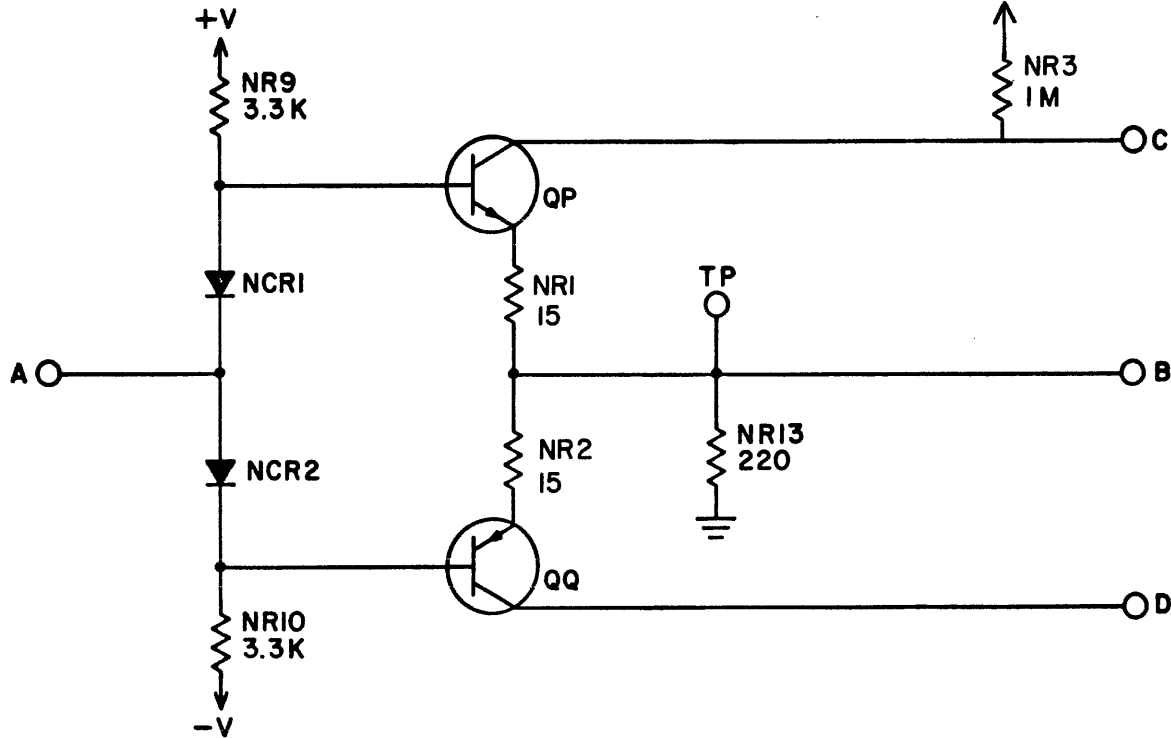
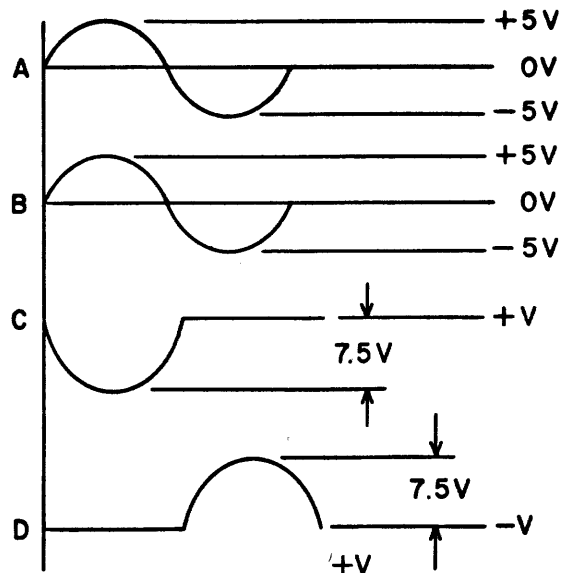
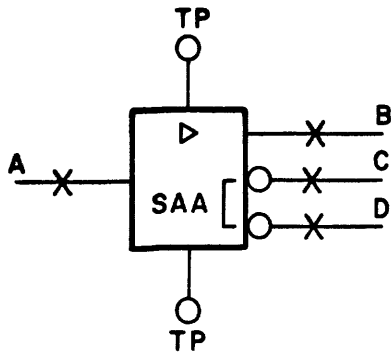
SWITCH RECEIVER - RCB

Switch Receiver RCB produces a "1" (+3v) output at B when the grounded switch connected to input A is closed. When the switch is open a "0" (0v) is felt at output B.

A switch to ground is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN is shut off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR6. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage across NC1 rapidly increases through NR1 and the switch to ground because of the short time constant of NR1 and NC1. Any contact bounce on the switch will increase the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP is decreased and QP begins to turn off. As QP turns off, the current through NR5 decreases due to the higher lead resistance (NR4) of QN compared with QP (NR6). The current drop through NR5 causes a decrease in the voltage drop across NR5. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is shut off. With QP off, the base of QQ is near ground, causing QQ to shut off. This allows the +5v supply to flow through NR8 to output B raising the output to +3v, "1".

When the switch is opened again, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Any contact bounce on the switch will hold NC1 well below the switching level of QN until the bouncing ceases. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of this positive feedback. The output then returns to "0".



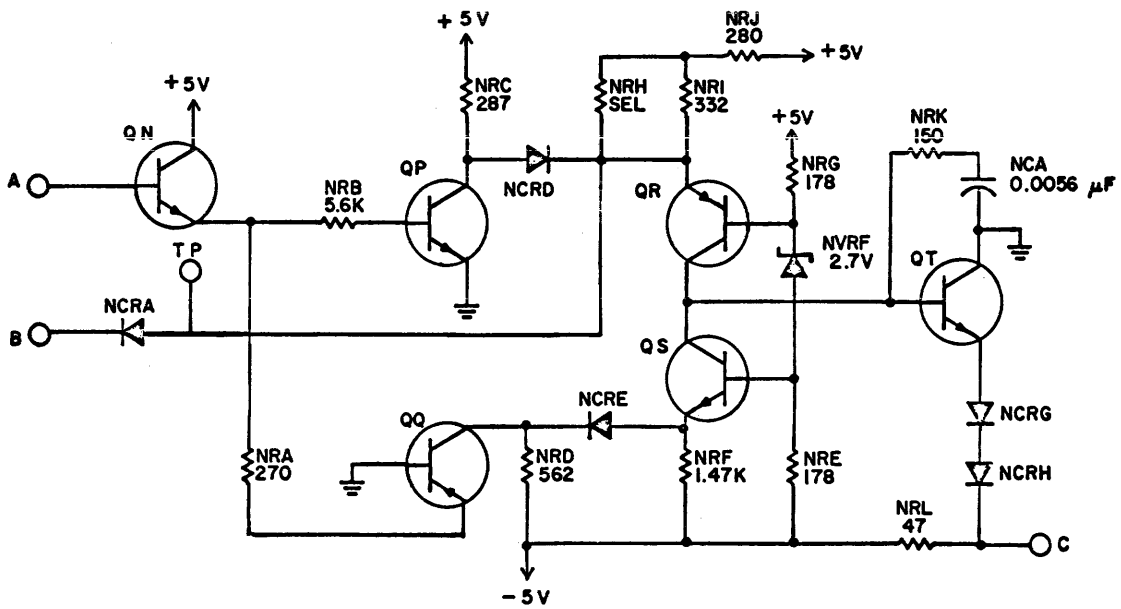
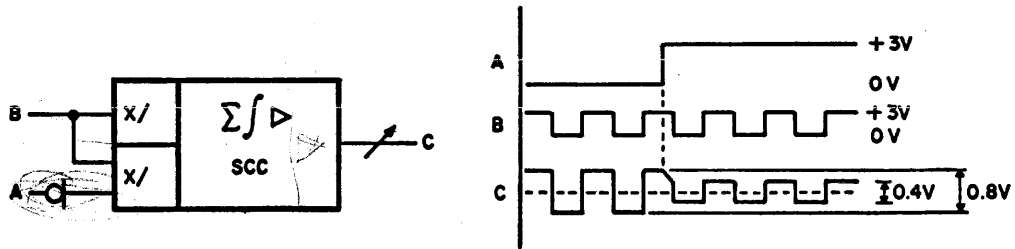
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T140

BIPOLAR CURRENT BUFFER - SAA

The SAA circuit is a power output stage for an operational amplifier. Transistors QP and QQ comprise a complementary output driver and are always biased slightly on by diodes NCR1 and NCR2.

The quiescent current in the output driver is nominally 6.5 ma and the maximum signal amplitude for the circuit is ± 5 volts.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J34B

LOW PASS FILTER AND AMPLIFIER - SCC

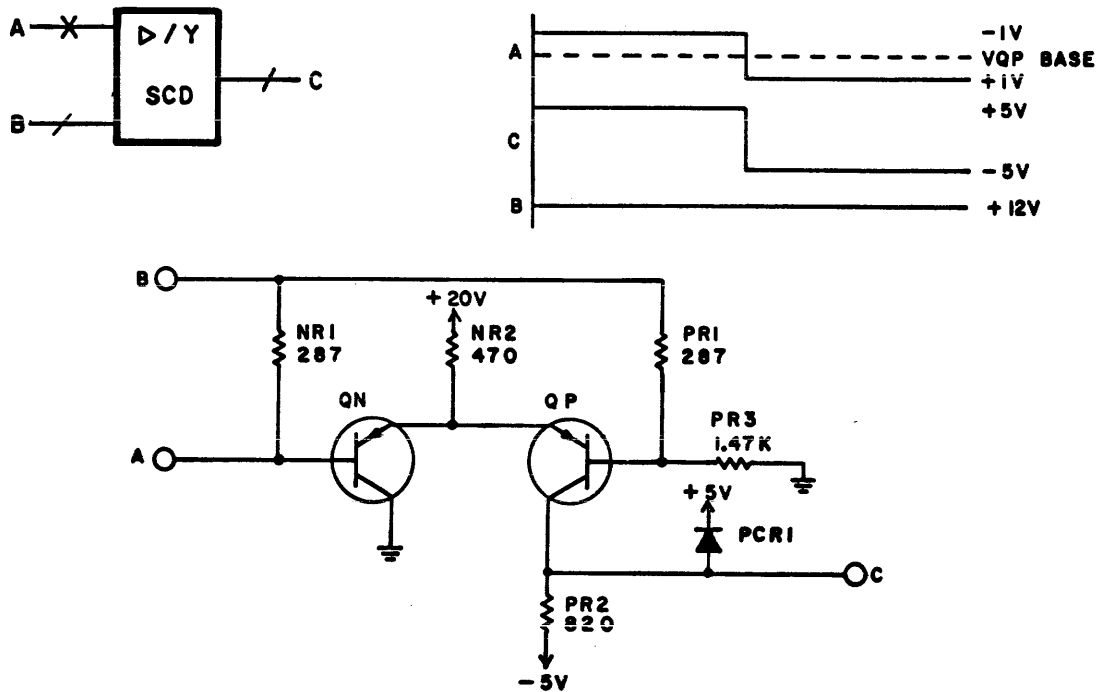
The SCC circuit consists of a bilevel current switch with a bidirectional current pump, a filter capacitor, and a level shifter. The circuit converts TTL input signals from a comparator circuit to produce a dc voltage level at TPB. Because of the phase locked oscillator closed loop, the current pump drives the dc level at TPB to reach a 50/50 duty cycle when the signal at input B is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency causes a change in voltage at TPB. A separate TTL input signal selects one of two possible current levels for the current pump.

QN, QP, QQ, NRA, NRB, NRC, NRD, NCRB, and NCRC form the bilevel current switch. For fast frequency synchronism, input A is a TTL "zero", turning all three transistors off and forward biasing NCRB and NCRC. This adds the current from NRC and NRD to the normal current pump level resulting in a high drive current. In the normal operating mode, input A is a "one", turning on QN, QP, and QQ. This back biases NCRB and NCRC, resulting in normal current pump drive.

NRG, NVRF, and NRE form a reference voltage divider for the current pump. NRF and QS is the negative-going current sink. This sinks a current of approximately 2 ma continually. NCRA, NRH, RNI, and QR form a switchable current source of approximately 5 ma. When a square wave of TTL logic level is applied to the zero "OR" gate of input B, NCA alternately is charged and discharged by 2 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times; therefore, the voltage across NCA has very little ac component in it.

Resistor NRK generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRK and the currents from the bidirectional pump. The net result at output C is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QT, NCRE, NCRF, and NRL form a buffer and level shifting circuit. They shift the waveform at base of QT negatively to a level appropriate for controlling the voltage controlled oscillator.

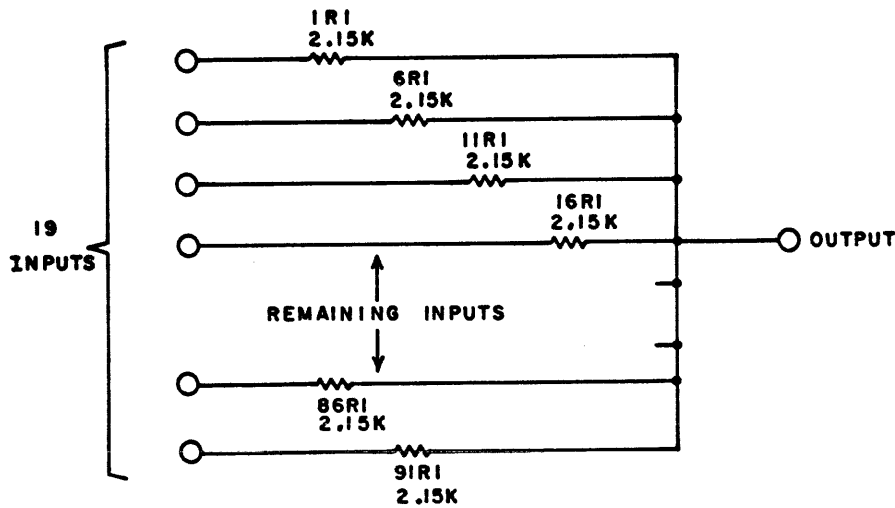
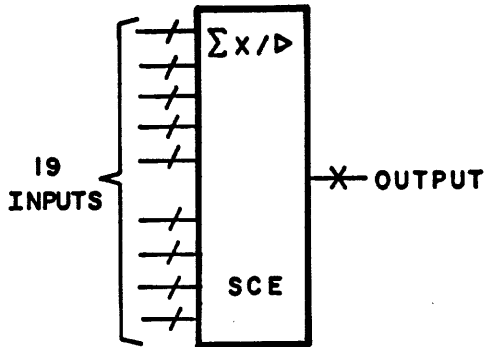


NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J36A

VOLTAGE COMPARATOR - SCD

The SCD circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

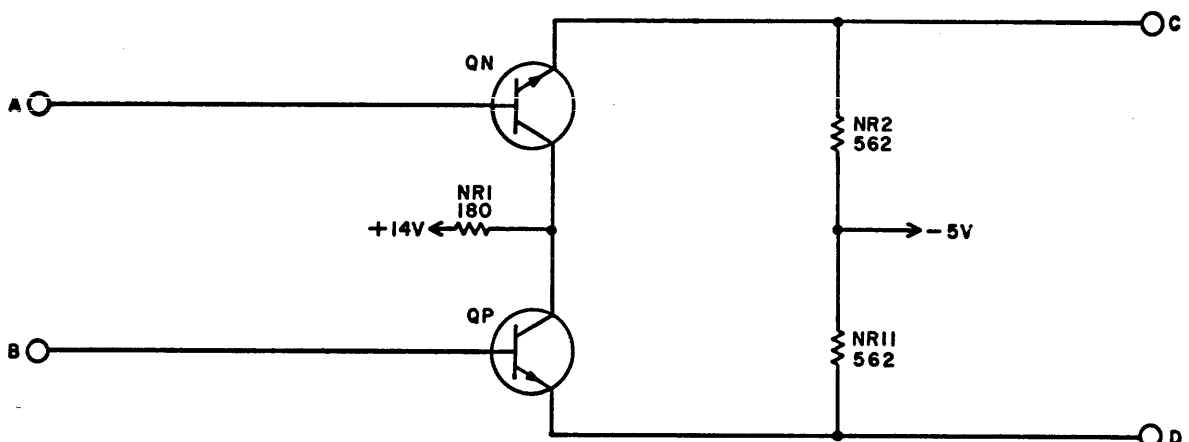
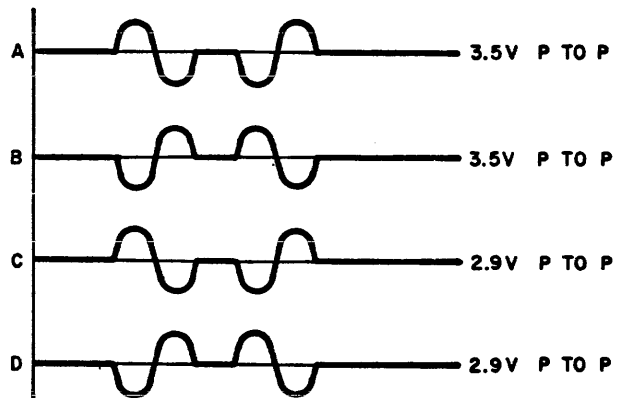
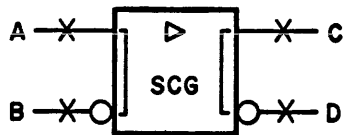
Input A typically is connected to the output of circuit SCE. Input B is typically +12 volts, and normal or "no fault" condition would be for 0 or 1 of the inputs of the summing ladder (SCE) to be grounded and the remaining inputs to be open. SCE would then output a voltage (to input A) higher than the reference voltage at the base of QP. QN then would be turned off and QP turned on driving output C to +5 volts. An abnormal or "fault" condition would be for 2 or more inputs of the summing ladder (SCE) to be grounded with the remaining inputs open. This would cause the voltage at point A to be lower than the reference voltage at the base of QP. QN would then be turned on and QP turned off. Point C would then switch to -5 volts.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J36A

Summing Ladder - SCE

The summing ladder SCE circuit is a network of resistors with the output connected to a voltage source through a common resistor such as input A on the SCD circuit. This forms a resistor divider circuit with an output voltage dependent upon the number of inputs (resistors) being connected to ground potential. One or more comparators could be connected to the output to check for a particular number of inputs being connected to ground.



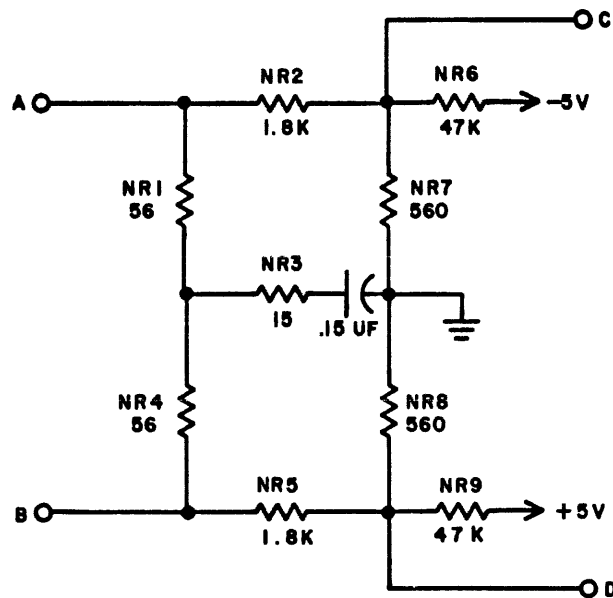
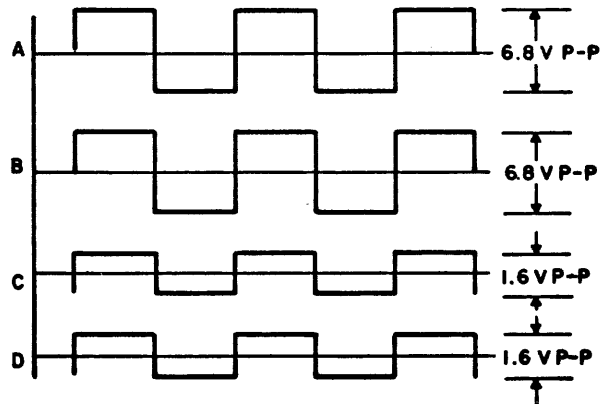
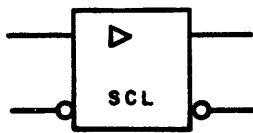
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J113A

BUFFER AMPLIFIER - SCG

The SCG circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal read from the servo head.

QN and QP are emitter followers that present comparatively high input impedance and low out impedance.



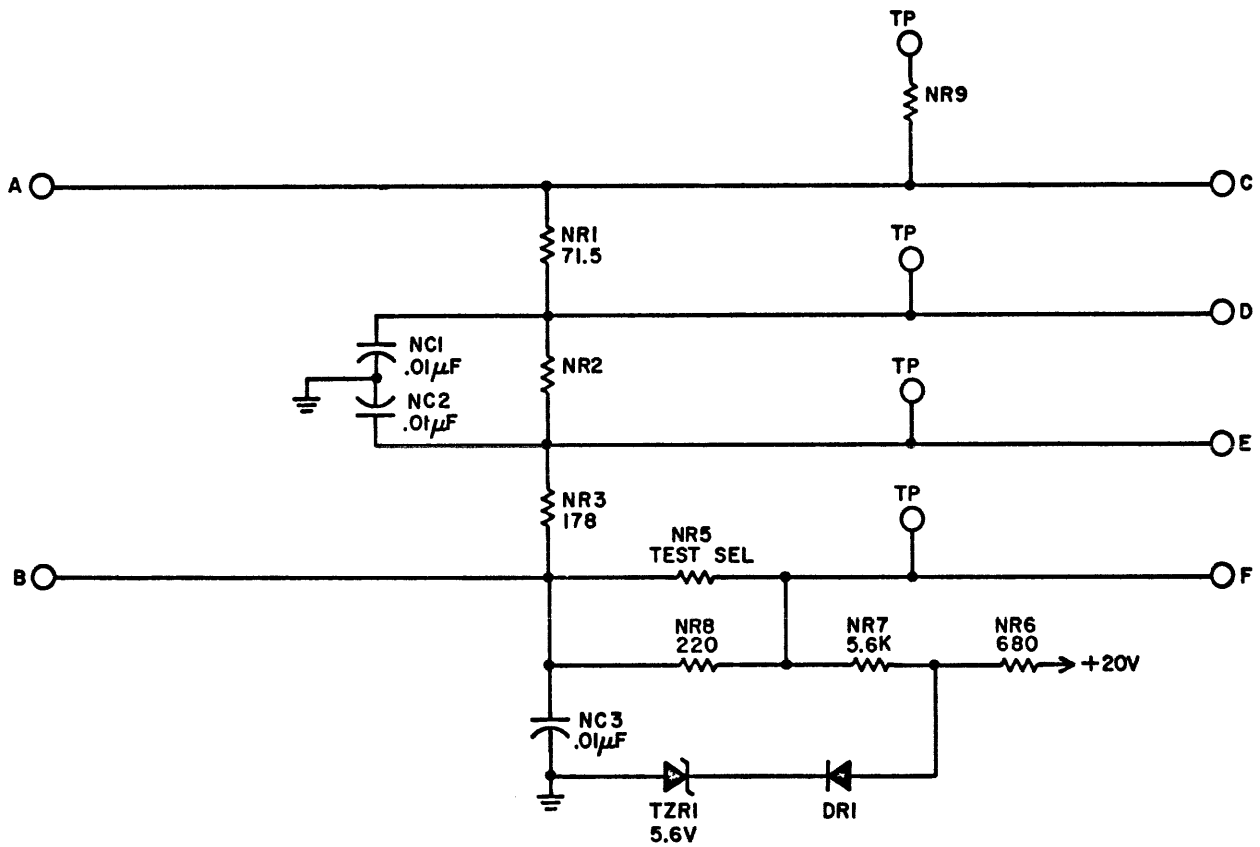
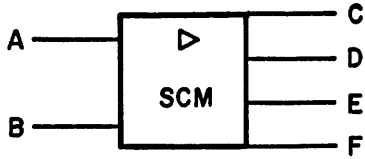
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J166A

TERMINATOR/DIVIDER SCL

The SCL circuit consists of a line terminator network (NR1 and NR4) and a resistor divider network (NR2, NR5, NR7, and NR8). Resistors NR6 and NR9 supply a bias voltage to outputs C and D. This bias voltage insures a definite state for the following receiver circuit.

NR3 and NC1 offer a high DC resistance and provide a low AC impedance to ground.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

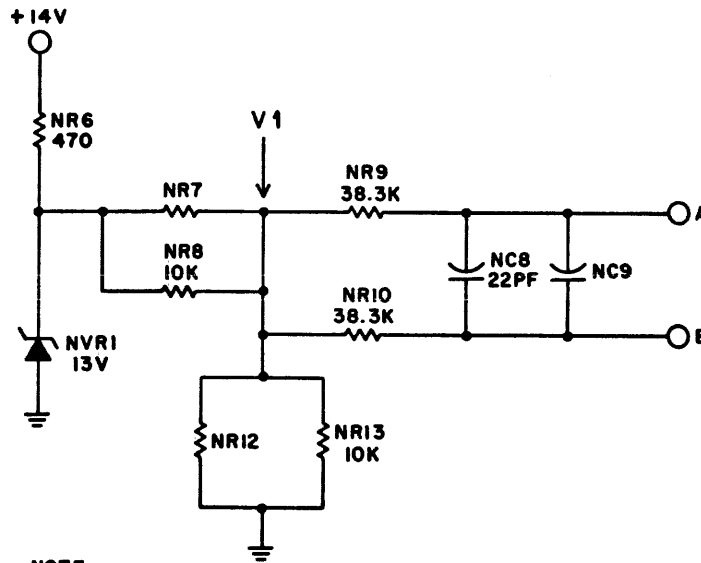
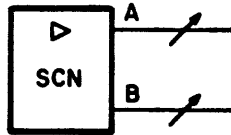
7J110

DIVIDER NETWORK – SCM

Resistor divider network SCM supplies various reference voltages for comparator circuits.

Input B (V_B) is typically -.7 volts. Input A (V_A) varies from -.7 to +1.5 volts, depending on read back voltage amplitude.

Output D will be $.72 \times (V_A - V_B)$. TZR1, DR1 and NR6 provides a regulated voltage which keeps the reference voltage at output E stable after NR5 has been test selected. Output E will be approximately -.6 volts.

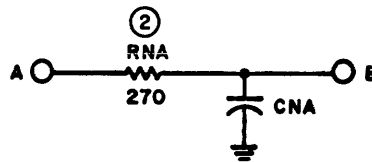
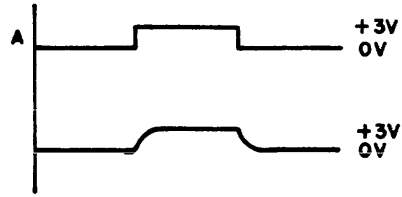
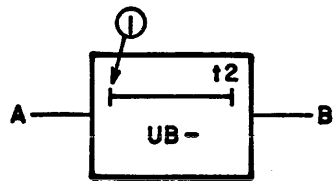


NOTE: 7J111
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

FREQUENCY CONTROL NETWORK - SCN

The SCN circuit is used to control the free-running frequency of the type 579 voltage controlled oscillator integrated circuit. The free-running frequency is the nominal frequency of the 579 without data inputs. The actual frequency of the 579 will deviate from nominal because of minor variations in the disk pack rotational speed.

Resistors NR7 and NR12 are selected (both may not be required) to set the voltage at V1 equal to +6.5 volts. This voltage, plus the capacitance introduced by NC8 and NC9, are applied to pins 5 and 6 of the 579 to set the free-running frequency. Capacitor NC9 is selected for precise frequency control. The frequency is approximately 12 MHz if NC9 is 3 picofarads; it is about 1.6 MHz if NC9 is 150 picofarads.



NOTES:

- ① COMPONENT VALUES VARY
- ② NOT USED ON UBF

6T155

DELAY - UBD/UBE/UBF/UBH

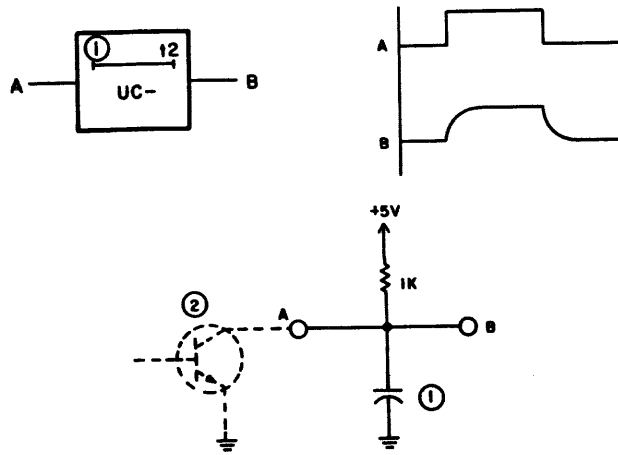
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms
UBH	100 nsec



NOTES:

- ① VALUE DEPENDENT ON CIRCUIT TYPE.
- ② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

67169

Delay - UC-

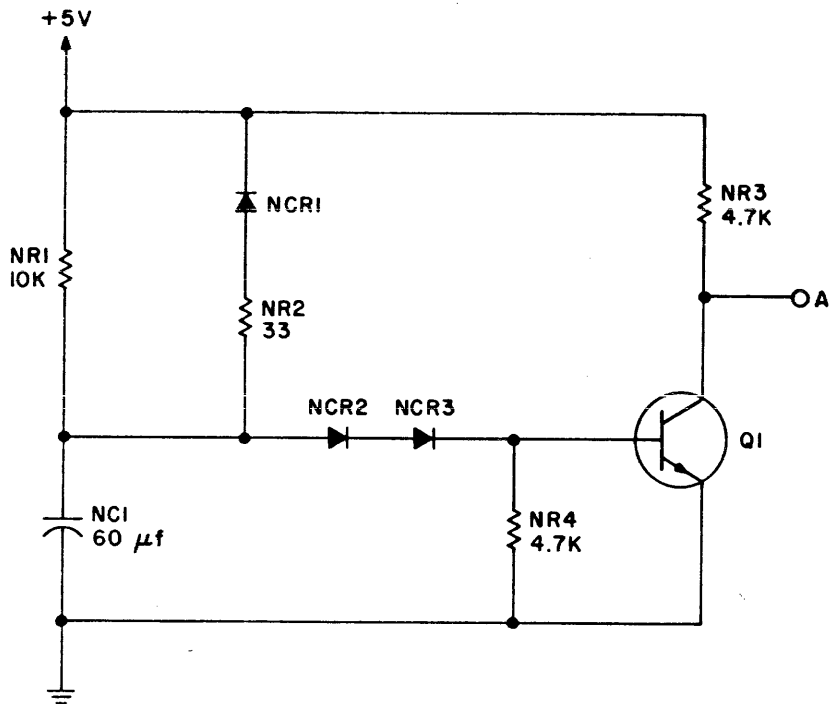
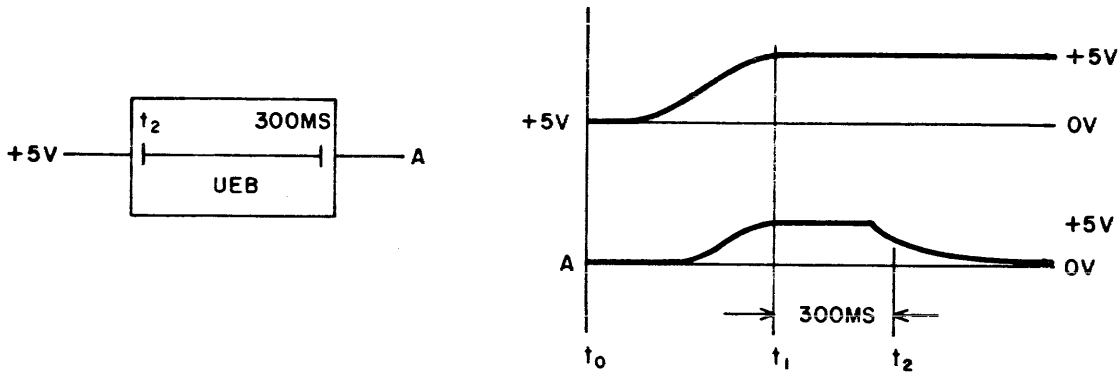
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5 volts and a capacitor connected to ground.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

<u>Circuit Type</u>	<u>Capacitance</u>	<u>Resistance</u>	<u>Delay</u>
UCF	1500 PF	1K	350 nsec
UCH	390 PF	1K	100 nsec
UCJ	22 μ F	2.7K	10 μ sec
UCL	390 PF	2.2K	155 nsec
UCN	3300 PF	2.7K	1.5 μ sec
UCT	2200 PF	2.7K	1.0 μ sec



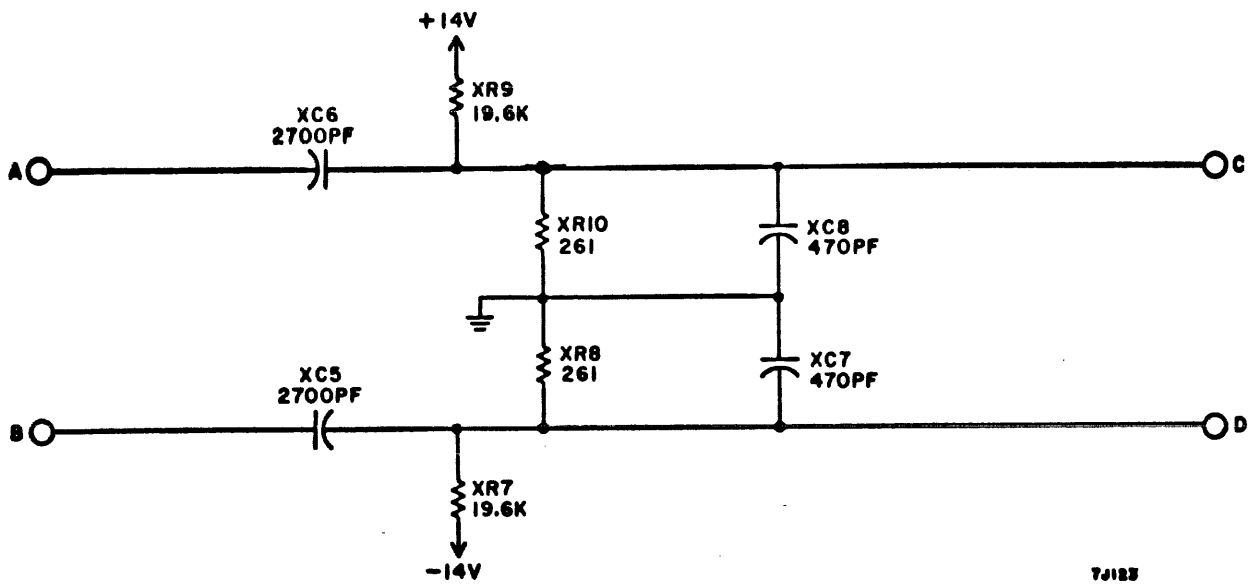
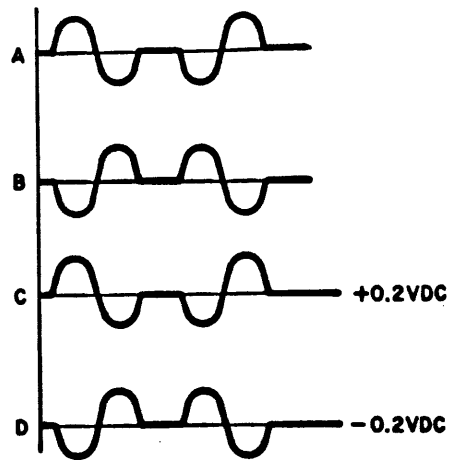
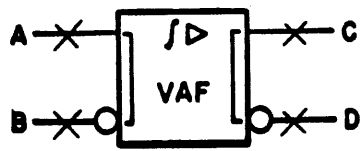
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

8D62A

DELAY - UEB

The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor NC1 is discharged by NR4, NCR2 and NCR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and NC1 is charging. As the voltage across NC1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

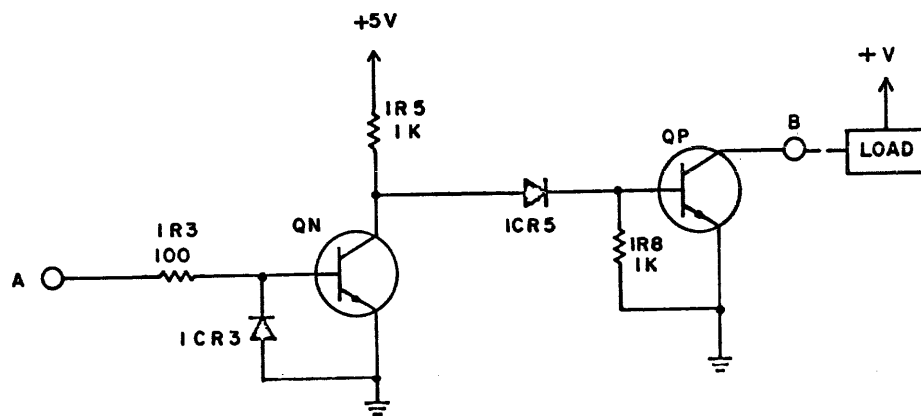
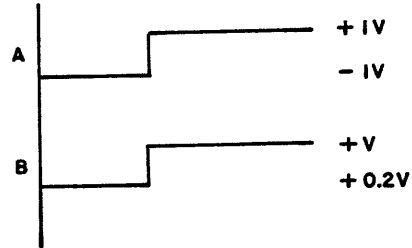
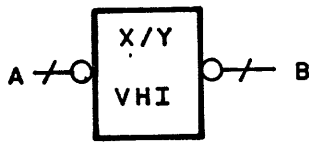
7J125

LEVEL SHIFTER – VAF

The VAF circuit receives the differentially amplified signal read by the servo head. It level-shifts the dc baseline of this signal to permit it to be analyzed by a differential voltage comparator.

Capacitors XC5 and XC6 block the dc level of the input while permitting the ac signal to pass. The resistors set the new dc baselines of the signal as shown in the illustration. Capacitors XC7 and XC8 shunt noise to ground.

The dc levels establish the switching point of the following comparator circuit. In its typical application, the next circuit switches state when output C is negative with respect to output D. The bias provided by the VAF circuit permits the comparator to switch state for about 50% of the time that input A is negative with respect to input B.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

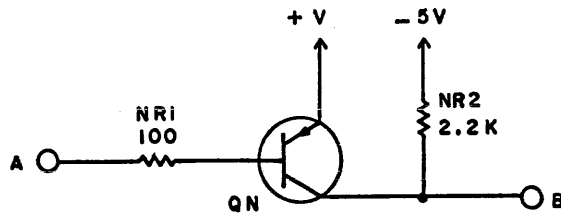
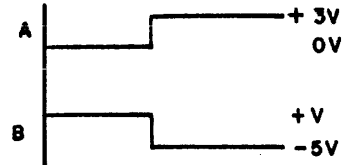
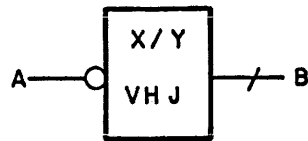
7J38

RELAY DRIVER - VHI

The VHI circuit drives a relay armature terminated at +V volts. Output B of the circuit functions to apply or remove ground so that the +V source may pull or drop the relay.

An input of +1 volt at A turns transistor QN on. The collector of QN goes low which turns transistor QP off. As a result, output B goes to +V and the relay is de-energized.

A -1 volt at input A turns off transistor QN. (Diode CR3 limits the reverse bias on QN to -0.7 volts.) The collector of QN now goes high which turns on transistor QP. This causes output B to go low, near 0 volts, energizing the load.



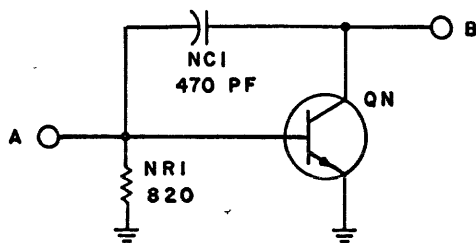
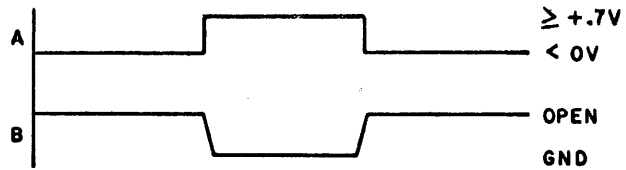
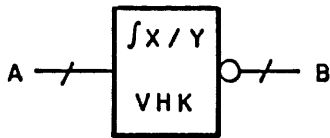
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7399

LEVEL TRANSLATOR - VHJ

The VHJ circuit converts TTL logic levels to +V and -5 volt levels where +V = 1.4 to 2.4 volts.

When a "0" (0v to +.4v) is applied to input A, QN turns on and applies +V (minus $V_{ce\ sat}$) to output B. When a "1" (+2.4v to +5v) is applied to A, QN turns off and output B switches to -5 volts.



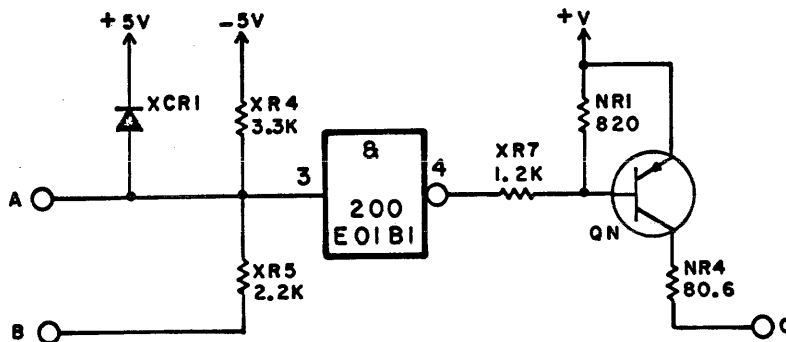
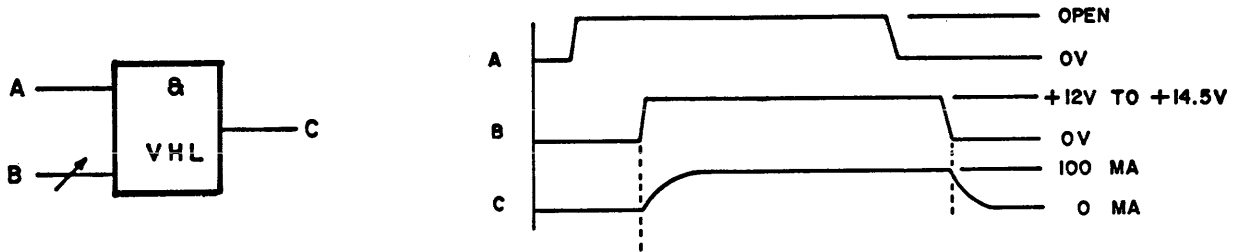
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J40

INTEGRATING LEVEL TRANSLATOR - VHK

The VHK circuit is a voltage level shifter that slows down and controls "turn on" and "turn off" transition times.

With an input to A of +.7 volts or greater (current limited to 20 ma), QN turns on with output B going to ground at a rate controlled by collector-base feedback capacitor NC1. With an input of 0 volts to -3 volts, QN turns off and output B is disconnected from ground.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J41A

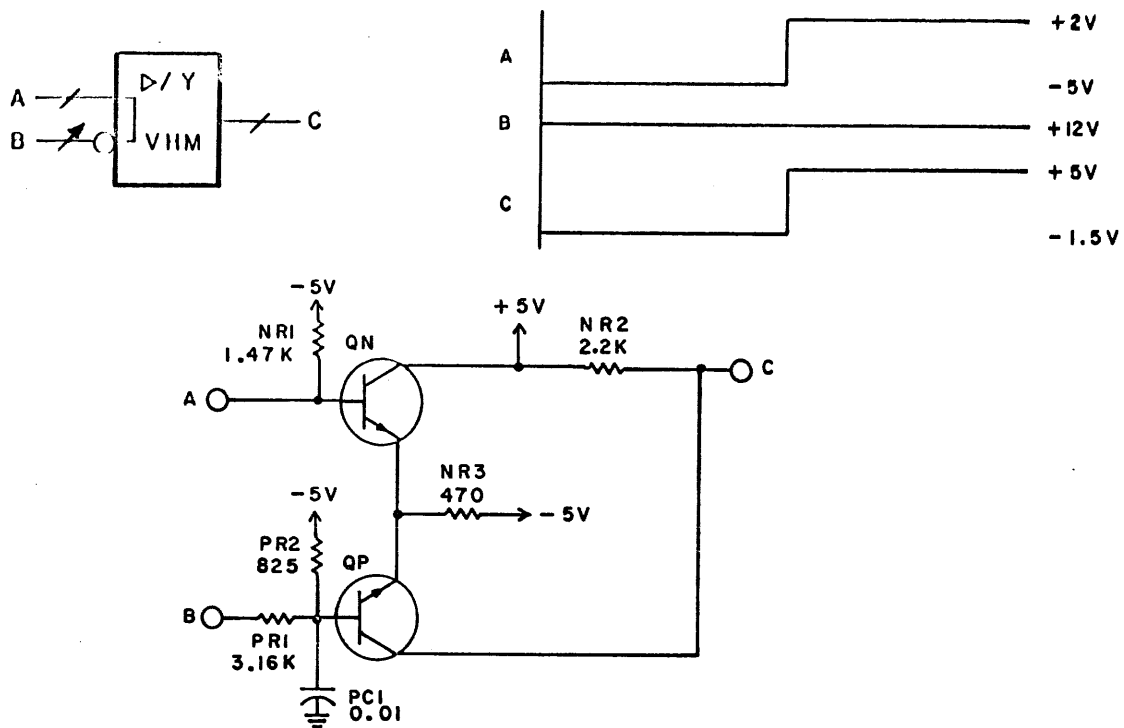
AND GATE - VHL

The VHL circuit is an erase current driver with a two AND function input.

Input A is normally connected to the output of a TTL open collector gate. Input B is normally connected to pin B of the FAG circuit which can vary from +12 volts to +15 volts. Output C gets connected to an erase head winding.

When input A is open ("1" output condition of open collector TTL gate) and input B is high (+12 v to +15 v), divider XR5 and XR4 insures a "1" condition at gate input pin 3. With inversion of the gate, pin 4 is a "0" (0 volts). This turns QN "on" and applies +V (approximately +12v) to the erase termination resistor NR4 which determines the amount of erase current to the head.

If either input A or B is held at a "0" condition, the output of gate 200 (pin 4) will go to +V (open collector output), QN will be turned "off" and no erase current will flow.



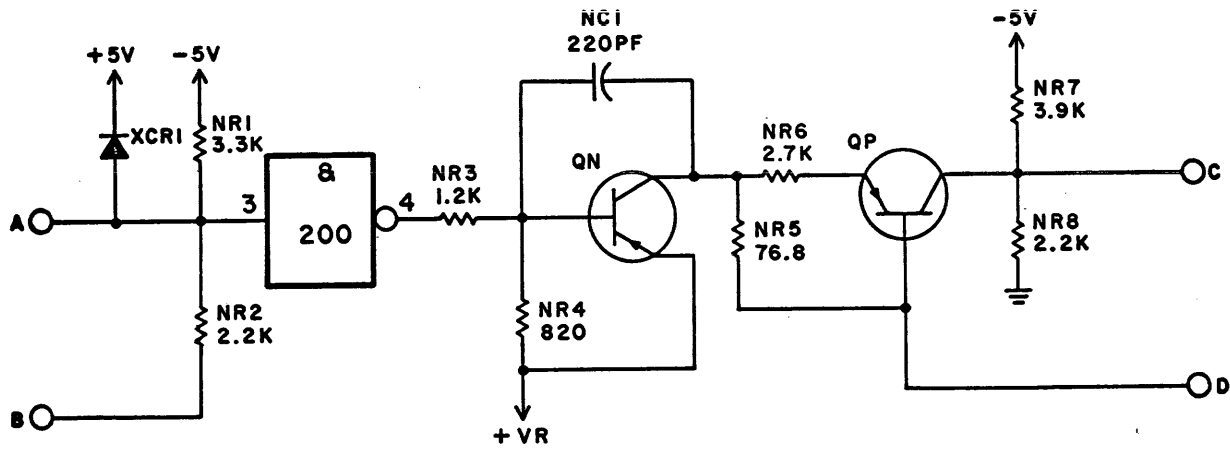
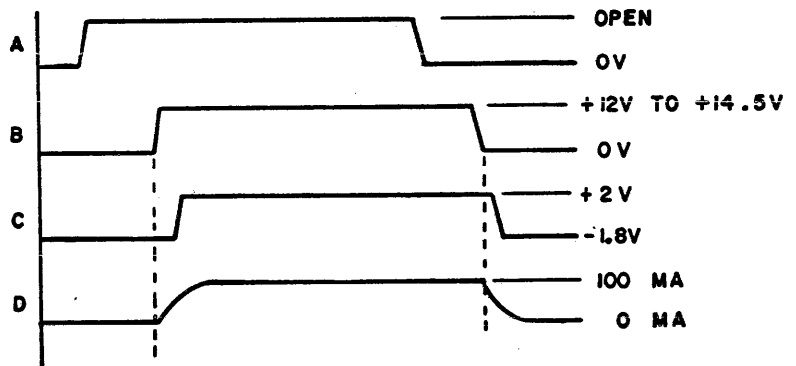
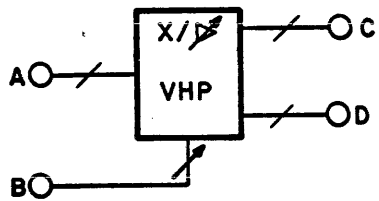
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J42

FAULT DETECTOR - VHM

The VHM circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

Input A is typically connected to output G of a write driver (JAG) circuit. Input B is connected to a controlled current source (FAG) with an output between +12 to +15 volts, dependent upon the current drain at QP.

The voltage level at input A is determined by the current flow into A through NR1 to -5 volts. With no current into A (A low) the voltage at A is -5 volts which is less than the voltage at the base of QP. QN is off, QP is on, and output C gets clamped at the saturated level of about -1.5 volts or at -.7 volts if output C is connected to a TTL gate input that has a diode clamp. When current flow into A exceeds approximately 2.7 ma, the voltage at A becomes more positive than at the base of QP. QN turns on, QP turns off, and output C rises to +5 volts.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J96

ERASE CURRENT DRIVER - VHP

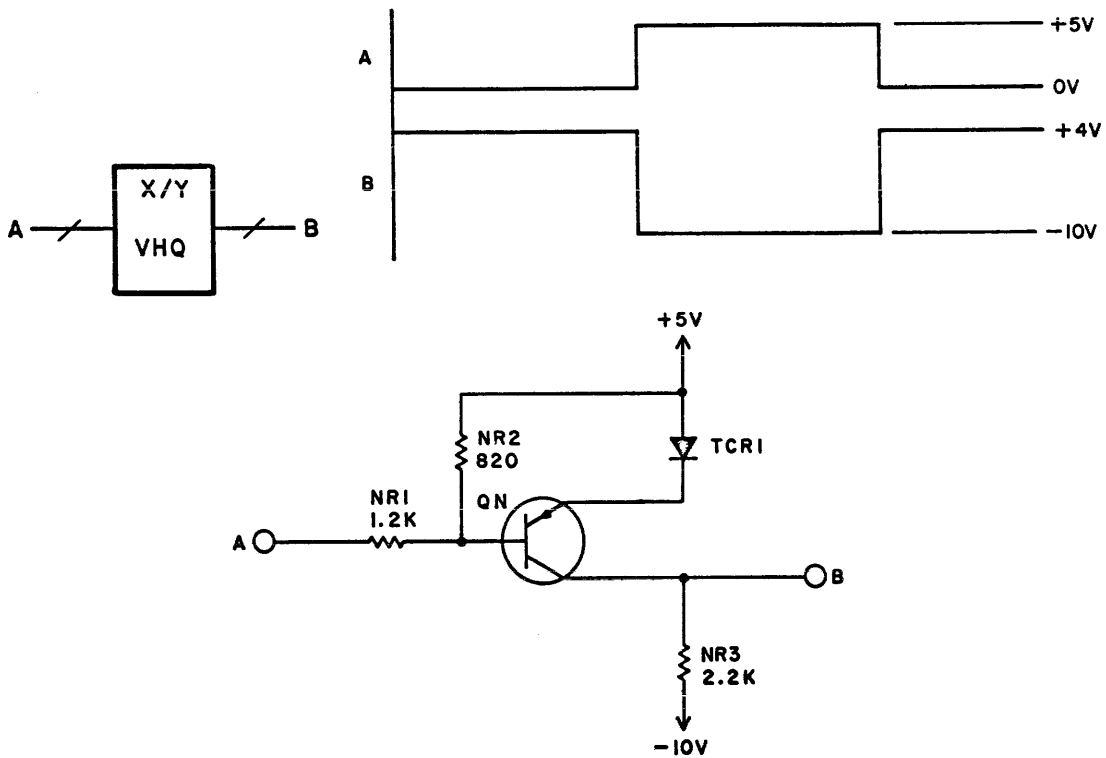
The VHP circuit provides approximately 100 ma of current (output D) for the erase coil of a read/write head. The circuit includes an output (C) bi-level signal to indicate whether the erase current is on or off.

Input A is connected to the output of an open collector IC TTL gate. Input B is connected to the write voltage (Vw) which can vary from 12 to 14.5 volts or it can be shut off (0 volts).

Both input A and B have to be "1's" to activate QN which provides erase current through NR5 to output D. A "1" at A is the "open" state of the open collector IC. A "1" at B is Vw = 12 to 14.5 volts. These input conditions cause a "0" at pin 4 of 200 element which will turn QN "on". When QN is on, Vr is applied to NR5 and NR6. Output D is connected to an erase coil winding so the current is controlled by the ratio of Vr to NR5. The voltage drop across NR5 is across NR6 and emitter-base of QP. This turns on QP which supplies a collector current of .028X (current at output D). This changes the voltage at output C from -1.8 volts to +2 volts.

A "0" (0 volts) at either input A or B will cause a "1" at pin 4 output of element 200. QN will turn off eliminating erase current at output D. No voltage drop across NR5 causes QP to turn off and output C goes back to -1.8 volts.

NQ1 slows down the rise and fall times of erase current transitions.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J94

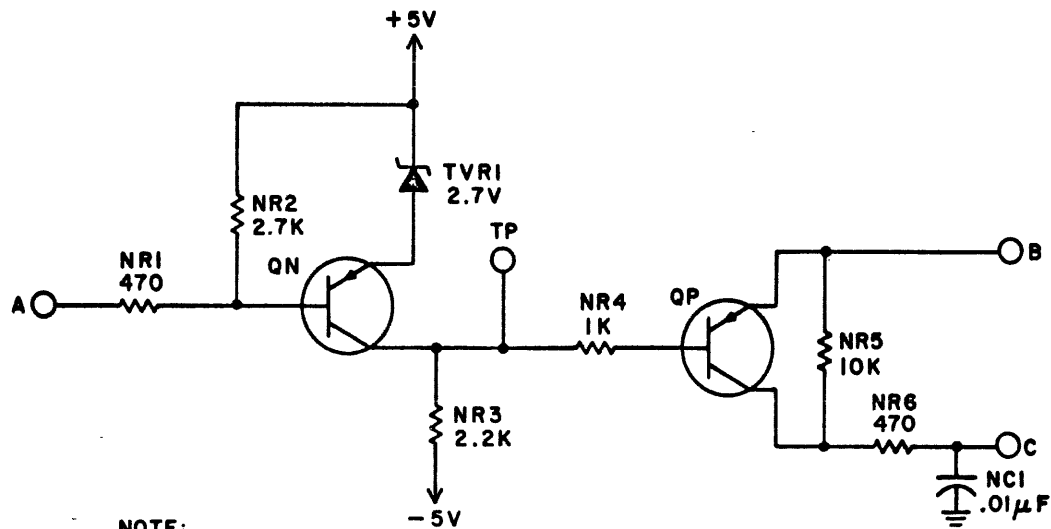
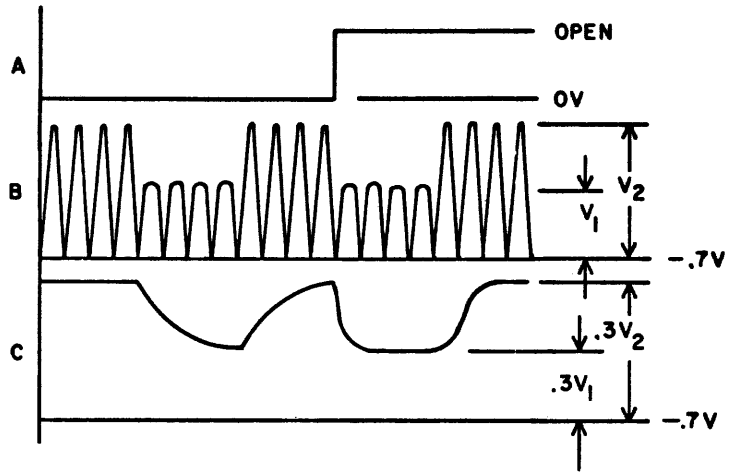
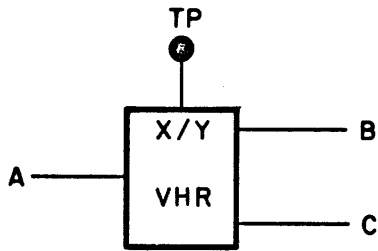
LEVEL TRANSLATOR – VHQ

The VHQ circuit translates digital signal levels of 0V and +5V to digital levels of +4V and -10V respectively.

A "0" (0V to +.5V) at input A causes QN to turn on and apply +5V minus V_{TCR1} or about +4 volts at output B.

A "1" (input open or +5 volts) at input A causes QN to turn off and output B goes to -10 volts through load resistor NR3.

An open collector IC or discrete transistor is used to provide the described input conditions at input A.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J99A

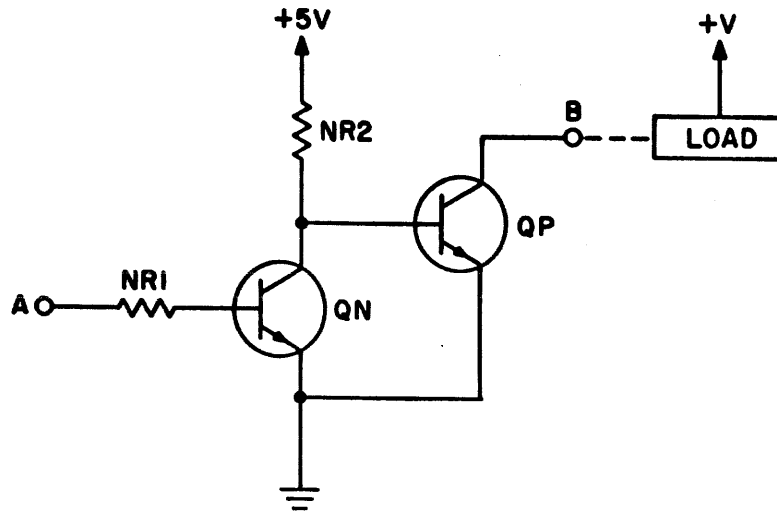
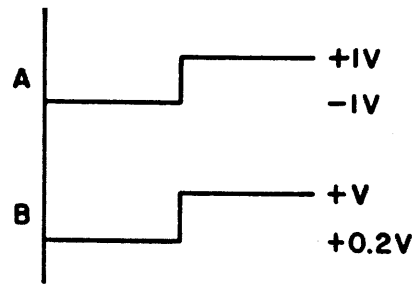
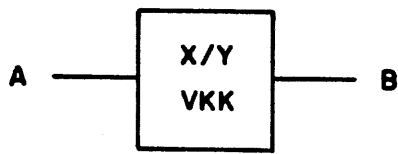
TIME CONSTANT SWITCH - VHR

The VHR circuit converts digital signals to integrator response times by switching a resistor in and out of an RC circuit. The integrator is made up of NR5, NR6, and NC1 with the input at B and output at C. The response time of this integrator can be changed by causing QP to switch NR5 in or out of the circuit.

Full wave rectification of read head signals is entered at B. The integrated output at C is a DC level which is an average value of the input signal waveform.

A "0" (0V to +.5V) at input A causes QN to turn on and apply +5V minus V_{TVR1} or about +2 volts at the base of QP. This causes QP to turn off which puts NR5 in series with NR6 and the time constant (response time) of the integrator becomes (NR5 + NR6) times (NC1).

A "1" (input open or +5 volts) at input A causes QN to turn off. QN collector goes toward -5 volts through NR3. This causes QP to turn on which "shorts out" NR5 leaving NR6 and NC1 to form the integrator. The time constant (response time) then becomes (NR6) times (NC1).



NOTE:
VOLTAGE AND COMPONENT VALUES
ARE FOR REFERENCE ONLY.

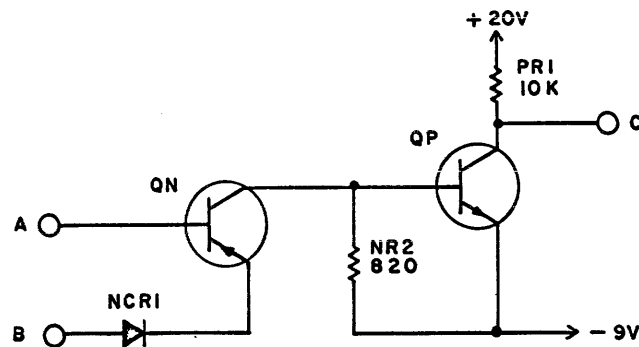
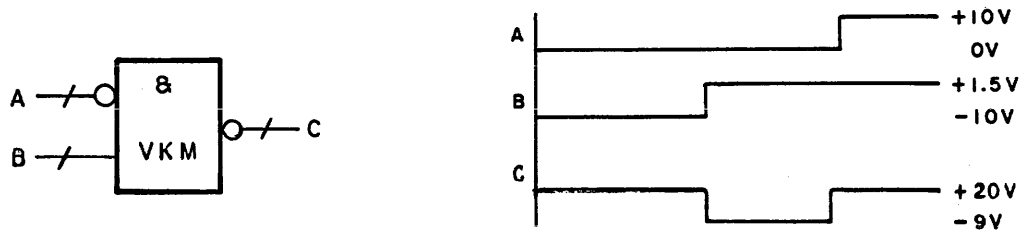
8D57

RELAY DRIVER - VKK

The VKK circuit drives a relay armature terminated at +V volts. Output B of the circuit functions to apply or remove ground so that the +V source may pull or drop the relay.

An input of about +1 volt at A turns QN on. The collector of QN goes low which turns QP off. As a result, output B goes to +V and the relay is de-energized.

A -1 volt turns QN off. The collector of QN goes high which turns QP on. This causes output B to go low, energizing the load.



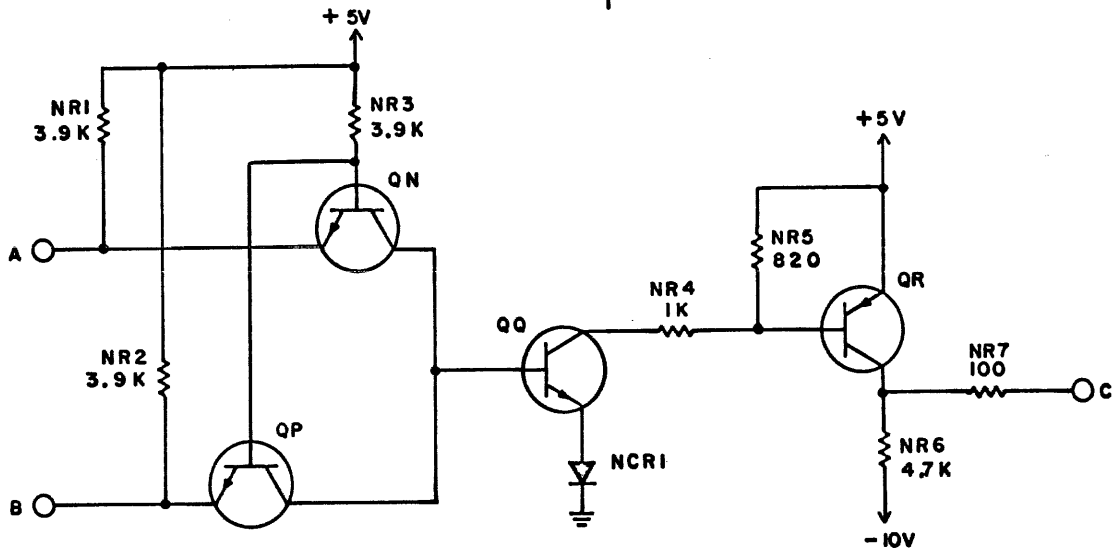
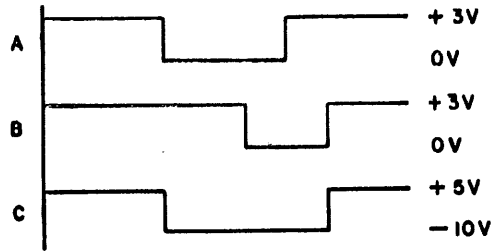
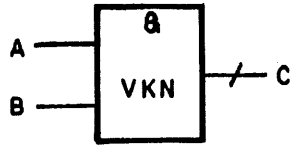
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J43

AND GATE - VKM

The VKM circuit is a two input gate with output levels of +20 volts and -9 volts.

Input A is typically connected to output B of VHK circuit and input B is connected to output C of VKN circuit through an 820 ohm current limiting resistor.

Diode NCR1 provides breakdown protection for the base emitter junction of QN when inputs A and B conditions cause reverse bias.



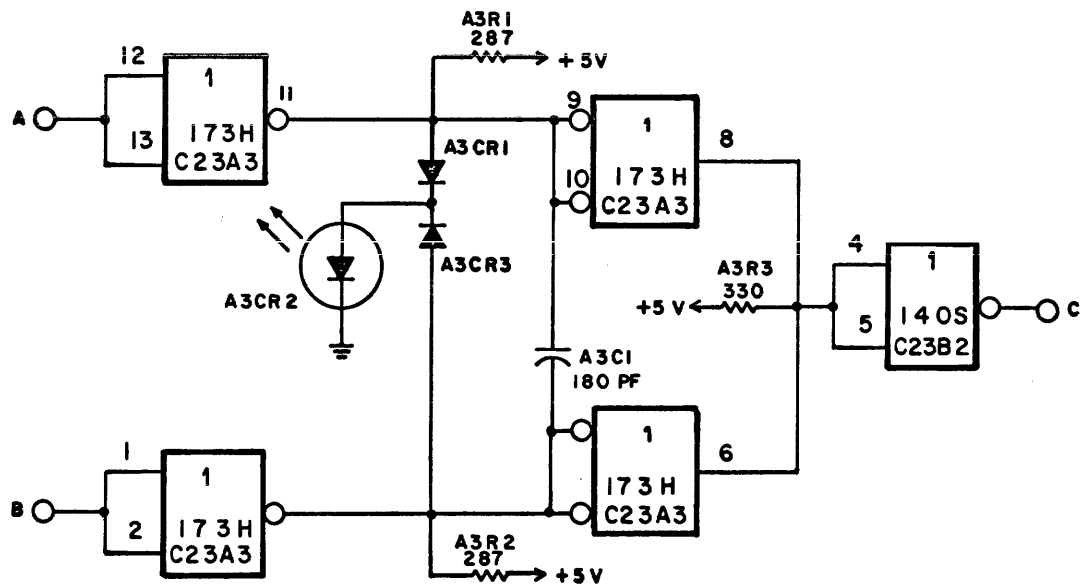
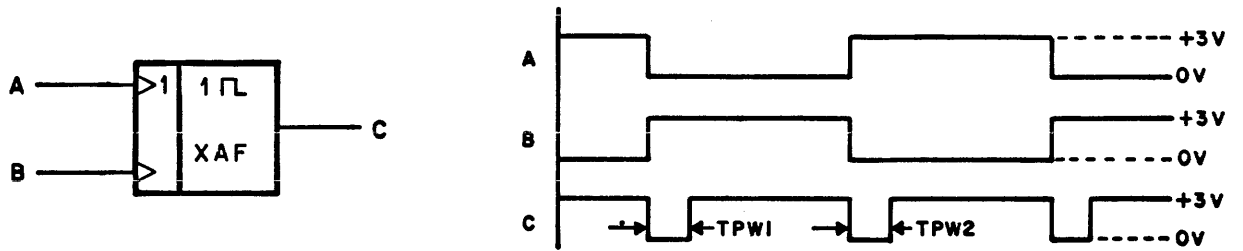
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7 J44

TWO INPUT AND GATE - VKN

The VKN circuit is a two input AND gate with input voltage levels matched to TTL threshold levels (approximately 1.4 volts) by NCR1.

Output voltages of +5 or -10 volts are current limited by resistors NR7 and NR6.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J53A

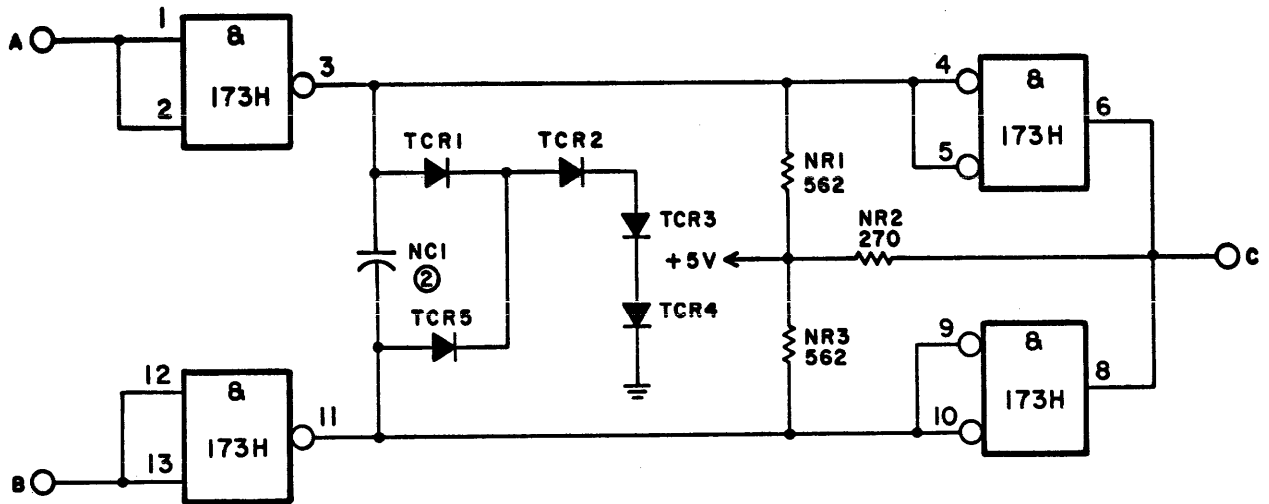
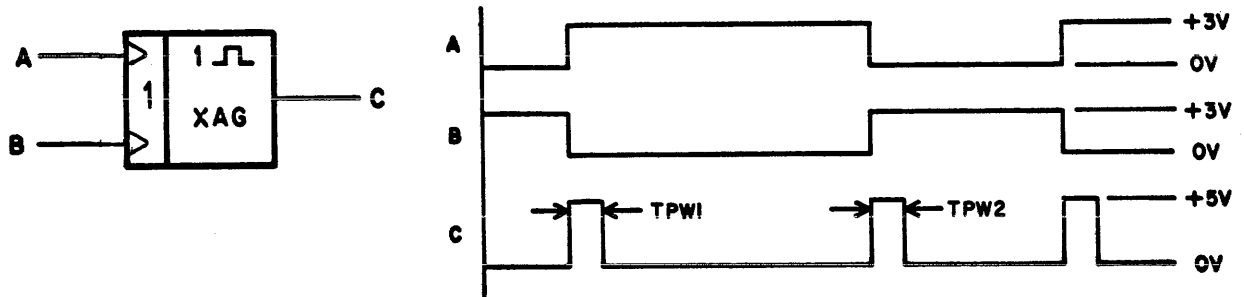
PULSE FORMER-XAF

The XAF circuit generates a negative pulse at output C for each positive going transition at either input A or B. Inputs and outputs are TTL compatible levels.

A negative going transition ("0") on input A and a positive going transition ("1") on input B cause a transition to ground at pin 3 of 173H (open collector IC) and a transition toward +5 volts at pin 11 through resistor A3R1. The "0" going transition is coupled through capacitor A3C1 and forces a negative spike on pin 11. This causes a delay in reaching the switching threshold of the output inverter, producing a negative pulse (TPW1) at output C for the duration of the delay (pulse width is determined by RC network A3C1 and A3R1).

The opposite condition on inputs A and B form the next pulse except using the RC network A3C1 and A3R2.

A3CR1, A3AR2 and A3CR3 clamp the positive excursion on pins 3 and 11 at approximately +2.2 volts to make the pulse width insensitive to repetition frequency variation up to 4 MHz and 50% duty cycle.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② D2 = 150PF
E2 = 100PF

7J02A

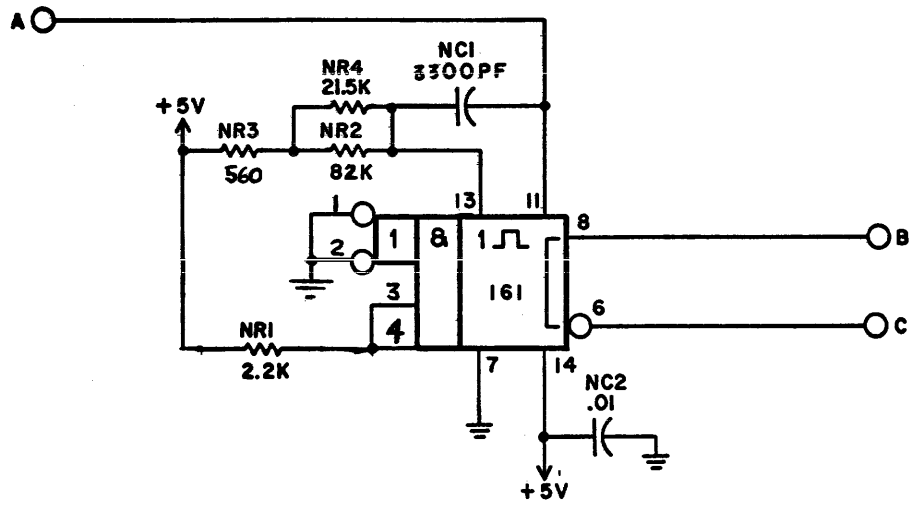
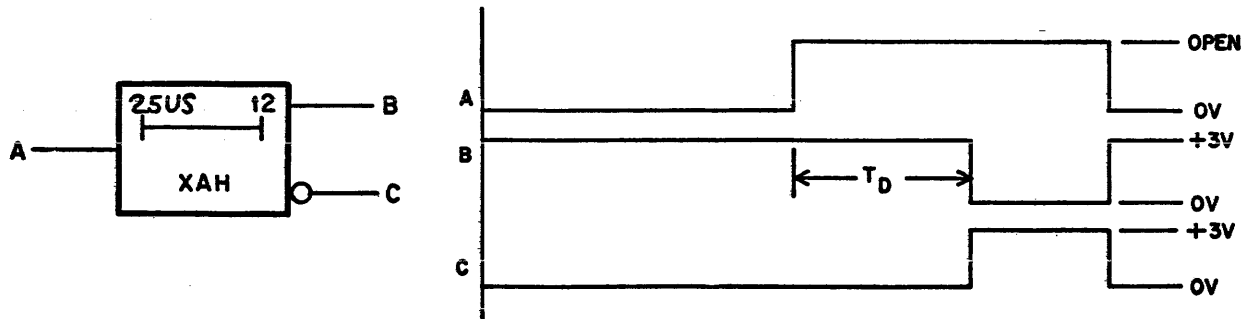
PULSE GENERATOR – XAG

The XAG circuit generates a positive pulse output at C for each positive going transition at either input A or B. Inputs and outputs are TTL compatible levels.

A positive going transition ("1") on input A and a negative going transition ("0") on input B cause a transition to ground at pin 3 of 173H (open collector IC) and a transition toward +5 volts at pin 11 of 173H through resistor NR3. The "0" going transition is coupled through capacitor NC1 and forces a negative spike on pin 11. Therefore, the voltage at pin 11 starts from a negative level and rises toward +5 volts at an RC time rate determined by NC1 and NR3. This causes a delay in reaching the switching threshold of the following inverter and produces a positive pulse at "OR'ed" output C for the duration of this delay (TPW1).

The opposite conditions on inputs A and B form the positive pulse (TPW2) at "OR'ed" output C determined by the RC network of NC1 and NR1.

TCR1, TCR2, TCR3, TCR4, and TCR5 clamp the positive excursion on pins 3 and 11 at approximately +2.5 volts to make the pulse width insensitive to repetition frequency variation up to 4 MHz and 50% duty cycle.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J109

DELAY - XAH

The XAH circuit consists of a one shot integrated circuit (with external RC network) used in an application which results in delayed outputs rather than one shot pulse outputs.

A "0" (0V to +.5V) at input A (pin 11) causes outputs B and C to remain in an inactive state, "1" and "0" respectively.

When input A is released or open, the delay time out begins. At the end of the delay time, outputs B and C change state to a "0" and "1" respectively. The delay time is approximated by $TD = .32 RC$, where $C = NC1$ and $R = NR3 + NR2 // NR4$. A return to a "0" at input A immediately resets outputs B and C to their original states of "1" and "0" respectively.

An open collector output integrated circuit such as a 173H or 200 is used to provide the described input conditions at A.

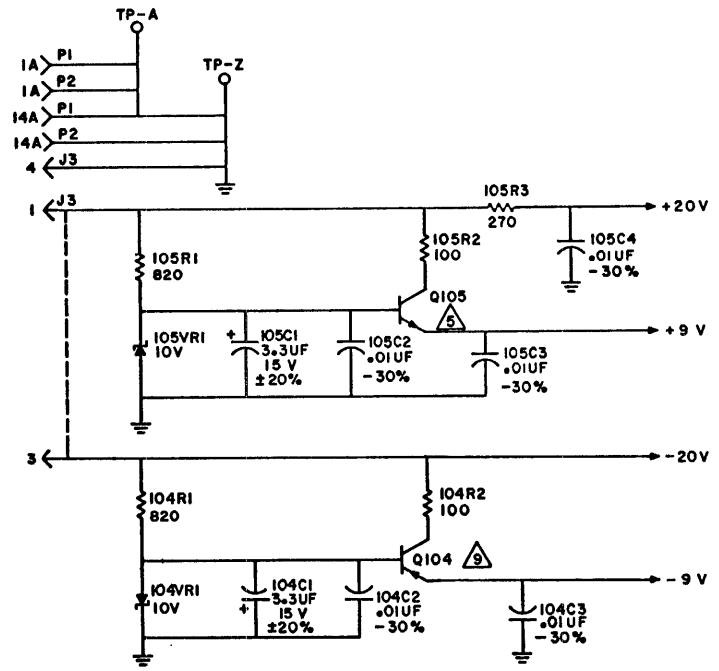
Resistor RN1 is an input gate pullup to insure a constant "1" condition on pins 3 and 4.

SECTION 4

CARD DIAGRAMS

70629100 E

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	123000	RELEASED		5-4-72			



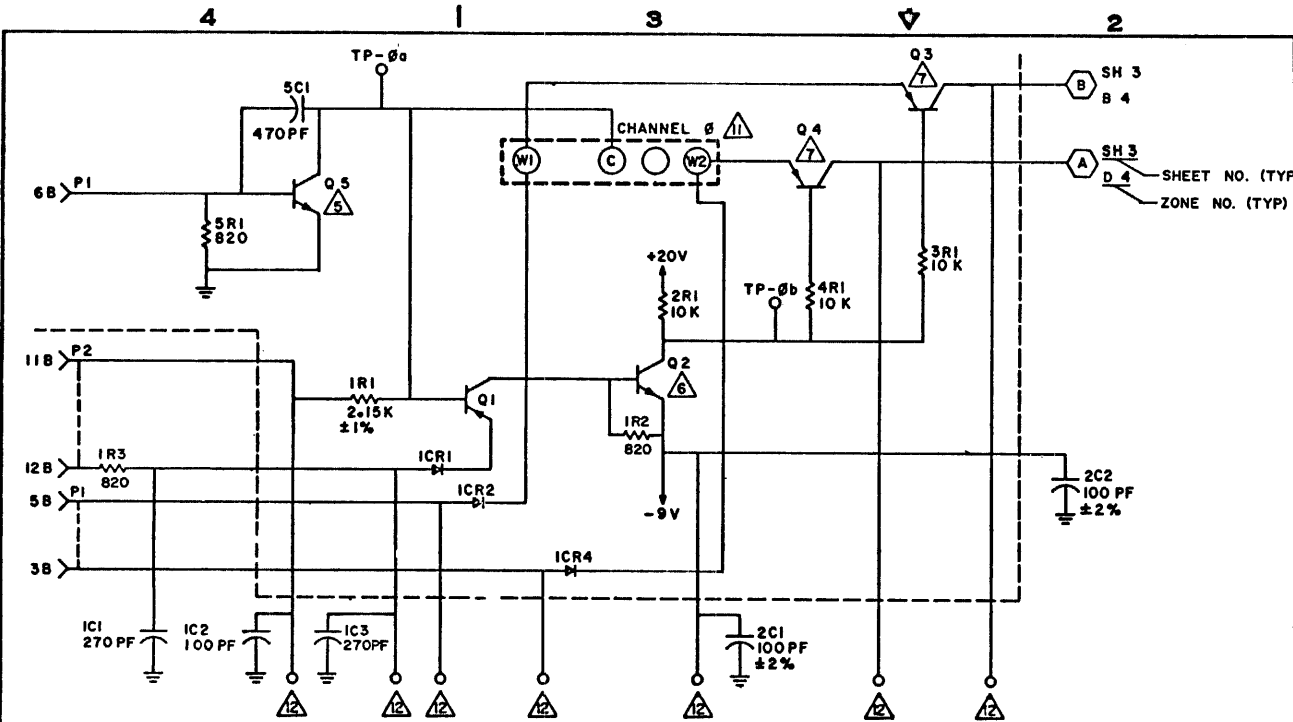
- NOTE:
- 1. UNLESS OTHERWISE SPECIFIED :
 ALL ZENER DIODE VOLTAGE TOLERANCES: ±5%
 ALL TRANSISTORS, SPNP, 2N4916, 50211610.
 ALL DIODES, SILICON, 24553500.
 - 2. IC, TSTR ARRAY, CA3018, 50251100.
 - 3. TSTR, DUAL SNPN, 24551000.
 - 4. TSTR, SNPN, 2N3646, 50210310.
 - 5. TSTR, SNPN, 2N3569, 50210811.
 - 6. TSTR, SNPN, 50210104.
 - 7. TSTR, SPNP, MATCHED PAIR, 50212201.
 - 8. DIODE, SILICON, ZENER, 4.1V, 92115027.
 - 9. TRANSISTOR, SPNP, 2N3638, 50210610.
 - 10. TRANSISTOR, SPNP, 2N4258, 50211510.
 - 11. SEE TABLE I FOR CHANNELS 0 THRU 18,
 TRANSISTOR, TEST POINT, RESISTOR, DIODE,
 AND CAPACITOR TRANSPOSITION.
 - 12. BUS LINES TO CHANNELS 1 THRU 18.
 - 13. PIN 10, U-103, IS CONNECTED TO -9V.

REFERENCE DRAWINGS		NORMANDALE DIVISION		TITLE	
COMP ASSY: 72829606		BR3A3		SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP	
COMPONENTS, EXCEPT AS NOTED		FIRST USED ON	DATE	CODE IDENT	DRAWING NUMBER
		DWN	4-24-72	19333	72829706
		CHK	5-4-72		
		ENGR	5-4-72		
		MFG			
		APPR			
RES	±5%	OHMS	1/4 W		
CAP	±10%				
				SHEET 1	OF 3

4-1

W72829706

1100



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

SH 3 B 4
SH 3 D 4
SHEET NO. (TYP)
ZONE NO. (TYP)

TABLE I

CHANNEL	I/P PIN	TSTR	TSTR	TSTR	TSTR	TSTR	TEST POINT	TEST POINT	RES	RES	RES	RES	RES	RES	DIODE	DIODE	CAP	DIODE
0	PI-6B	Q1	Q2	Q3	Q4	Q5	0a	0b	1R1	2R1	4R1	3R1	5R1	1R2	1CR1	1CR2	5C1	1CR4
1	7B	Q6	Q7	Q8	Q9	Q10	1a	1b	6R1	7R1	9R1	8R1	10R1	6R2	6CR1	6CR2	10C1	6CR4
2	8A	Q11	Q12	Q13	Q14	Q15	2a	2b	11R1	12R1	14R1	13R1	15R1	11R2	11CR1	11CR2	15C1	11CR4
3	8B	Q16	Q17	Q18	Q19	Q20	3a	3b	16R1	17R1	19R1	18R1	20R1	16R2	16CR1	16CR2	20C1	16CR4
4	10A	Q21	Q22	Q23	Q24	Q25	4a	4b	21R1	22R1	24R1	23R1	25R1	21R2	21CR1	21CR2	25C1	21CR4
5	11B	Q26	Q27	Q28	Q29	Q30	5a	5b	26R1	27R1	29R1	28R1	30R1	26R2	26CR1	26CR2	30C1	26CR4
6	11A	Q31	Q32	Q33	Q34	Q35	6a	6b	31R1	32R1	34R1	33R1	35R1	31R2	31CR1	31CR2	35C1	31CR4
7	12B	Q36	Q37	Q38	Q39	Q40	7a	7b	36R1	37R1	39R1	38R1	40R1	36R2	36CR1	36CR2	40C1	36CR4
8	12A	Q41	Q42	Q43	Q44	Q45	8a	8b	41R1	42R1	44R1	43R1	45R1	41R2	41CR1	41CR2	45C1	41CR4
9	PI-13A	Q46	Q47	Q48	Q49	Q50	9a	9b	46R1	47R1	49R1	48R1	50R1	46R2	46CR1	46CR2	50C1	46CR4
10	P2-2A	Q51	Q52	Q53	Q54	Q55	10a	10b	51R1	52R1	54R1	53R1	55R1	51R2	51CR1	51CR2	55C1	51CR4
11	3A	Q56	Q57	Q58	Q59	Q60	11a	11b	56R1	57R1	59R1	58R1	60R1	56R2	56CR1	56CR2	60C1	56CR4
12	3B	Q61	Q62	Q63	Q64	Q65	12a	12b	61R1	62R1	64R1	63R1	65R1	61R2	61CR1	61CR2	65C1	61CR4
13	4B	Q66	Q67	Q68	Q69	Q70	13a	13b	66R1	67R1	69R1	68R1	70R1	66R2	66CR1	66CR2	70C1	66CR4
14	6B	Q71	Q72	Q73	Q74	Q75	14a	14b	71R1	72R1	74R1	73R1	75R1	71R2	71CR1	71CR2	75C1	71CR4
15	7B	Q76	Q77	Q78	Q79	Q80	15a	15b	76R1	77R1	79R1	78R1	80R1	76R2	76CR1	76CR2	80C1	76CR4
16	8B	Q81	Q82	Q83	Q84	Q85	16a	16b	81R1	82R1	84R1	83R1	85R1	81R2	81CR1	81CR2	85C1	81CR4
17	9A	Q86	Q87	Q88	Q89	Q90	17a	17b	86R1	87R1	89R1	88R1	90R1	86R2	86CR1	86CR2	90C1	86CR4
18	P2-10B	Q91	Q92	Q93	Q94	Q95	18a	18b	91R1	92R1	94R1	93R1	95R1	91R2	91CR1	91CR2	95C1	91CR4

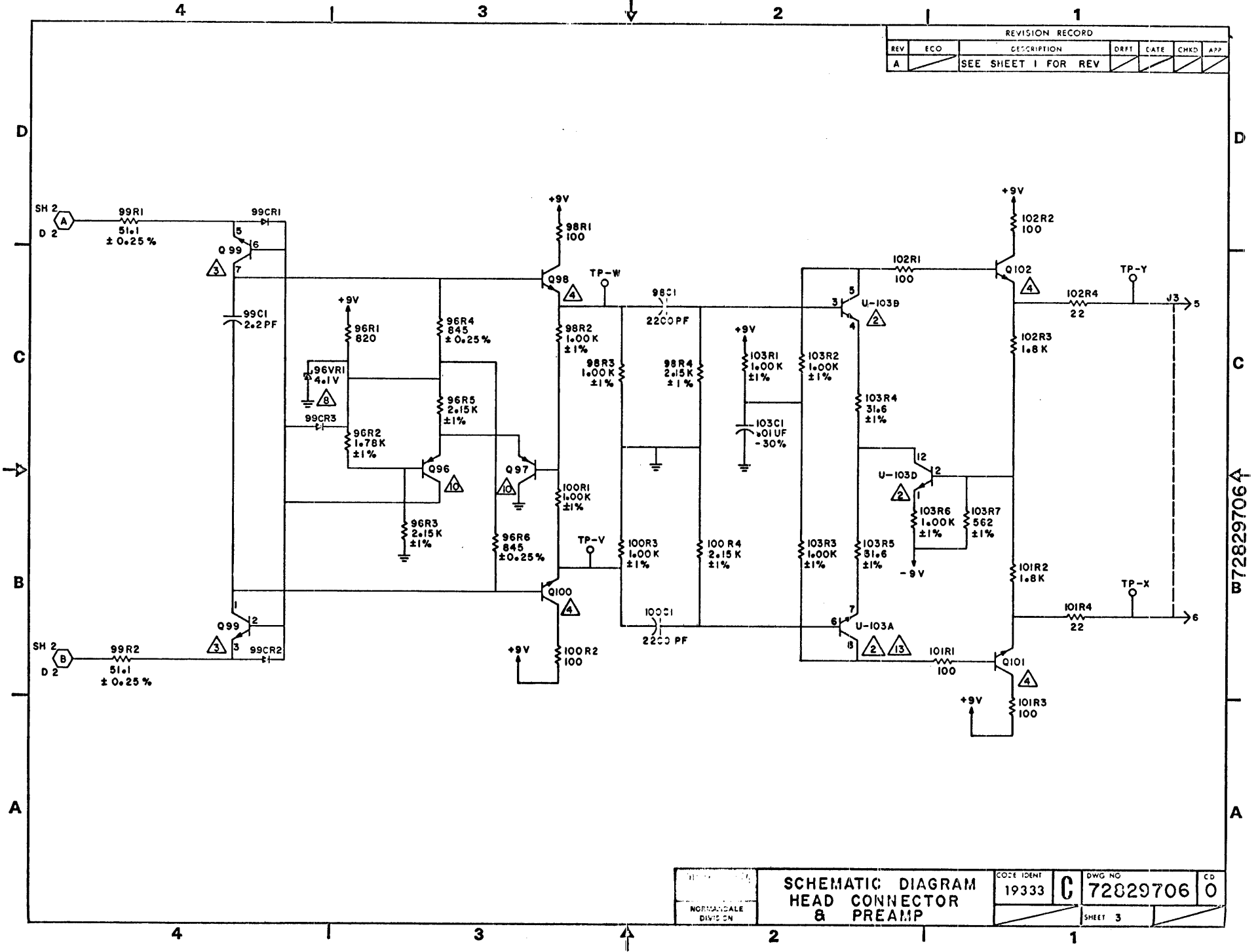
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP	CODE IDENT	DWG NO	CD
		19333	72829706	0
		SHEET 2		

W 728297064

70629100 G

4-2.1/4-2.2

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CMKD	APP
A		SEE SHEET 1 FOR REV				

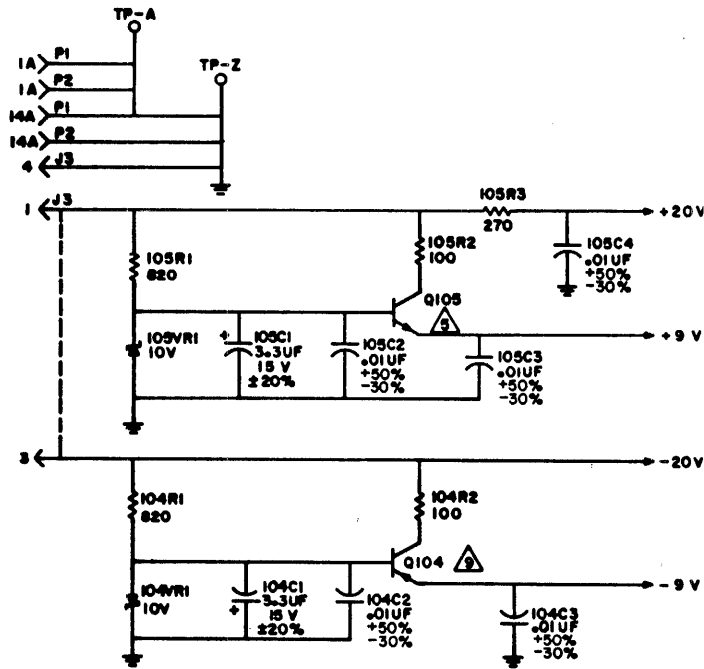


NORMAN DALE DIVISION	SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP		CODE IDENT 19333	C	DWG NO 72829706	CD 0
					SHEET 3	

70629100 G

4-2.3

SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	REV	ECO	DESCRIPTION
A		RELEASED							



NOTE:

- 1. UNLESS OTHERWISE SPECIFIED :
 ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$
 ALL TRANSISTORS, SPNP, 2N4916, 50211610.
 ALL DIODES, SILICON, 24553500.
- △ IC, TSTR ARRAY, CA3018, 50251100.
- △ TSTR, DUAL SNPN, 24551000.
- △ TSTR, SNPN, 2N3646, 50210310.
- △ TSTR, SNPN, 2N3569, 50210811.
- △ TSTR, SNPN, 50210104.
- △ TSTR, SPNP, MATCHED PAIR, 50212201.
- △ DIODE, SILICON, ZENER, 4.1V, 92115027.
- △ TRANSISTOR, SPNP, 2N3638, 50210610.
- △ TRANSISTOR, SPNP, 2N4258, 50211610.
- △ SEE TABLE I FOR CHANNELS 0 THRU 18,
 TRANSISTOR, TEST POINT, RESISTOR, DIODE,
 AND CAPACITOR TRANSPOSITION.
- △ BUS LINES TO CHANNELS 1 THRU 18.
- △ PIN 10, U-105, IS CONNECTED TO -9V.

REFERENCE DRAWINGS	CONTROL DATA	NORMAN DALE DIVISION	TITLE
COMP 2312	PART USED ON BR3A3		SCHEMATIC DIAGRAM HEAD CONNECTOR & PREAMP TYPE DZPN
	DWN <i>Monahan</i> 5-2-74		
	CHK <i>DiKithoff</i> 5-14-74		
	ENGR <i>W. J. ...</i> 5-16-74		
	MFG <i>...</i> 5-20-74		
	APP <i>...</i> 5-22-74		
COMPONENTS LIST AS NOTED		CODE IDENT	DRAWING NUMBER
TOLERANCE		19333	C 72829712
RES $\pm 5\%$	2-43 1/4 W		8
CAP $\pm 10\%$			

4-2.4

REVISION RECORD						
REV	ECO	DESCRIPTION	DEPT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

D

I

C

B

A

W 72829712

A

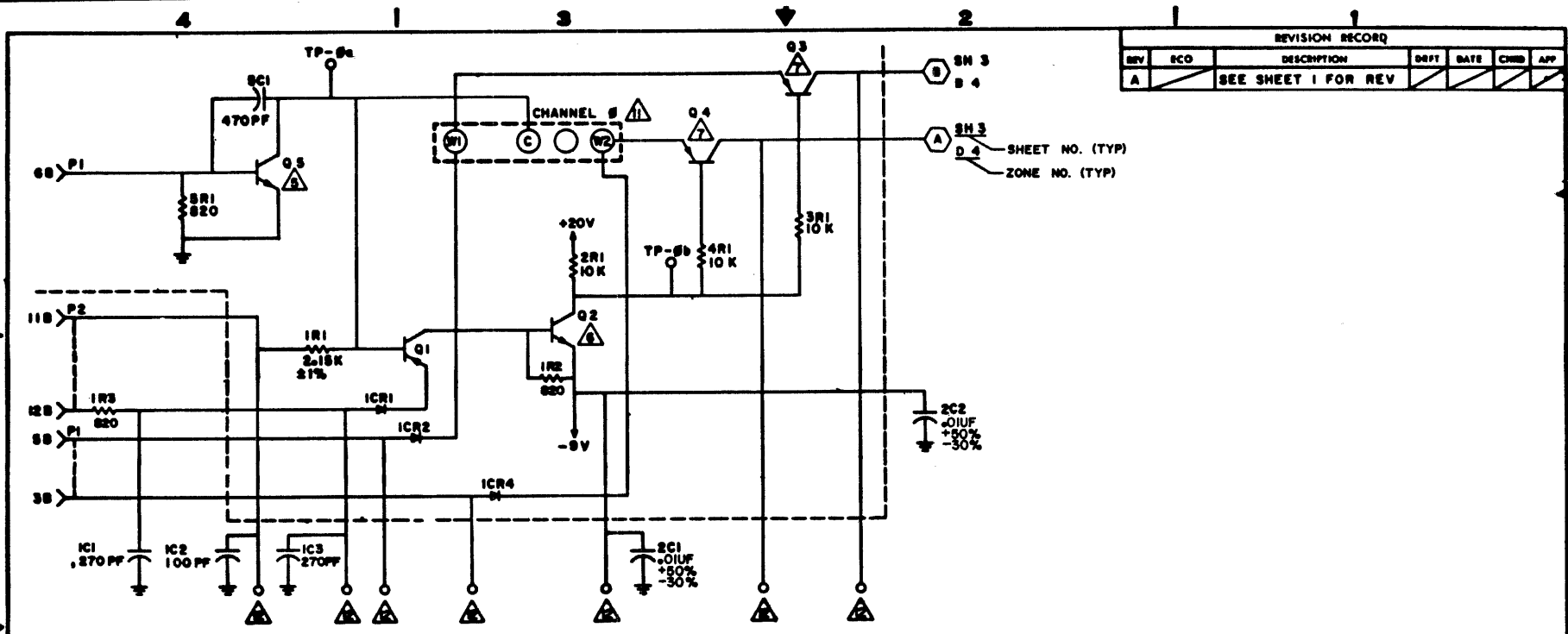


TABLE I

CHANNEL	I/P PIN	TSTR	TSTR	TSTR	TSTR	TSTR	TEST POINT	TEST POINT	RES	RES	RES	RES	RES	RES	DIODE	DIODE	CAP	DIODE
8	P1-8B	Q1	Q2	Q3	Q4	Q5	8a	8b	1R1	2R1	4R1	3R1	5R1	1R2	1CR1	1CR2	5C1	1CR4
1	7B	Q6	Q7	Q8	Q9	Q10	1a	1b	6R1	7R1	9R1	8R1	10R1	6R2	6CR1	6CR2	10C1	6CR4
2	8A	Q11	Q12	Q13	Q14	Q15	2a	2b	11R1	12R1	14R1	13R1	15R1	11R2	11CR1	11CR2	15C1	11CR4
3	8B	Q16	Q17	Q18	Q19	Q20	3a	3b	16R1	17R1	19R1	18R1	20R1	16R2	16CR1	16CR2	20C1	16CR4
4	10A	Q21	Q22	Q23	Q24	Q25	4a	4b	21R1	22R1	24R1	23R1	25R1	21R2	21CR1	21CR2	25C1	21CR4
5	11B	Q26	Q27	Q28	Q29	Q30	5a	5b	26R1	27R1	29R1	28R1	30R1	26R2	26CR1	26CR2	30C1	26CR4
6	11A	Q31	Q32	Q33	Q34	Q35	6a	6b	31R1	32R1	34R1	33R1	35R1	31R2	31CR1	31CR2	35C1	31CR4
7	12B	Q36	Q37	Q38	Q39	Q40	7a	7b	36R1	37R1	39R1	38R1	40R1	36R2	36CR1	36CR2	40C1	36CR4
8	12A	Q41	Q42	Q43	Q44	Q45	8a	8b	41R1	42R1	44R1	43R1	45R1	41R2	41CR1	41CR2	45C1	41CR4
9	P1-13A	Q46	Q47	Q48	Q49	Q50	9a	9b	46R1	47R1	49R1	48R1	50R1	46R2	46CR1	46CR2	50C1	46CR4
10	P2-2A	Q51	Q52	Q53	Q54	Q55	10a	10b	51R1	52R1	54R1	53R1	55R1	51R2	51CR1	51CR2	55C1	51CR4
11	3A	Q56	Q57	Q58	Q59	Q60	11a	11b	56R1	57R1	59R1	58R1	60R1	56R2	56CR1	56CR2	60C1	56CR4
12	3B	Q61	Q62	Q63	Q64	Q65	12a	12b	61R1	62R1	64R1	63R1	65R1	61R2	61CR1	61CR2	65C1	61CR4
13	4B	Q66	Q67	Q68	Q69	Q70	13a	13b	66R1	67R1	69R1	68R1	70R1	66R2	66CR1	66CR2	70C1	66CR4
14	6B	Q71	Q72	Q73	Q74	Q75	14a	14b	71R1	72R1	74R1	73R1	75R1	71R2	71CR1	71CR2	75C1	71CR4
15	7B	Q76	Q77	Q78	Q79	Q80	15a	15b	76R1	77R1	79R1	78R1	80R1	76R2	76CR1	76CR2	80C1	76CR4
16	8B	Q81	Q82	Q83	Q84	Q85	16a	16b	81R1	82R1	84R1	83R1	85R1	81R2	81CR1	81CR2	85C1	81CR4
17	9A	Q86	Q87	Q88	Q89	Q90	17a	17b	86R1	87R1	89R1	88R1	90R1	86R2	86CR1	86CR2	90C1	86CR4
18	P2-10B	Q91	Q92	Q93	Q94	Q95	18a	18b	91R1	92R1	94R1	93R1	95R1	91R2	91CR1	91CR2	95C1	91CR4

70629100 G

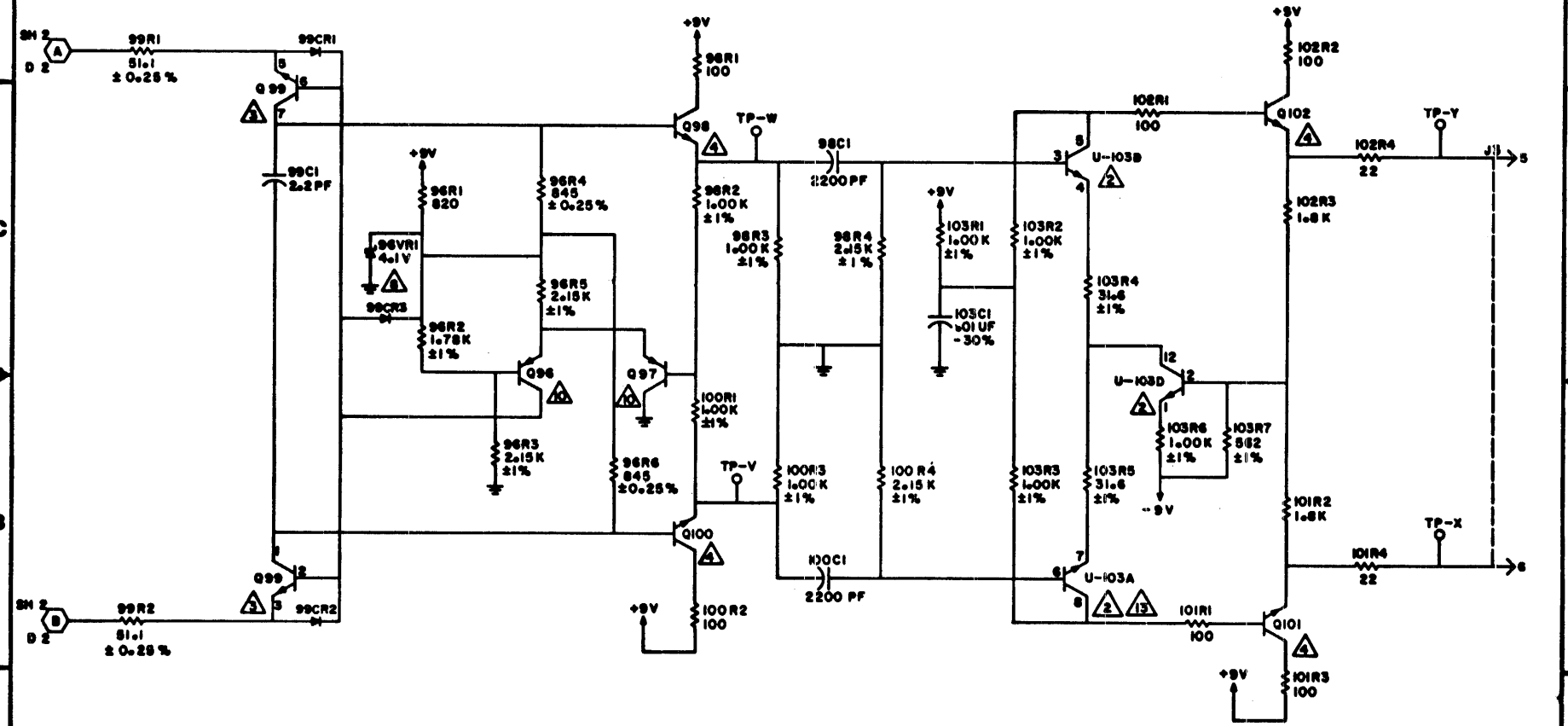
	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CS
	TYPE DZPN		19333	72829712	8
			SHEET 2		

4 1 3 4 2 1 1

70629100 G

4-3

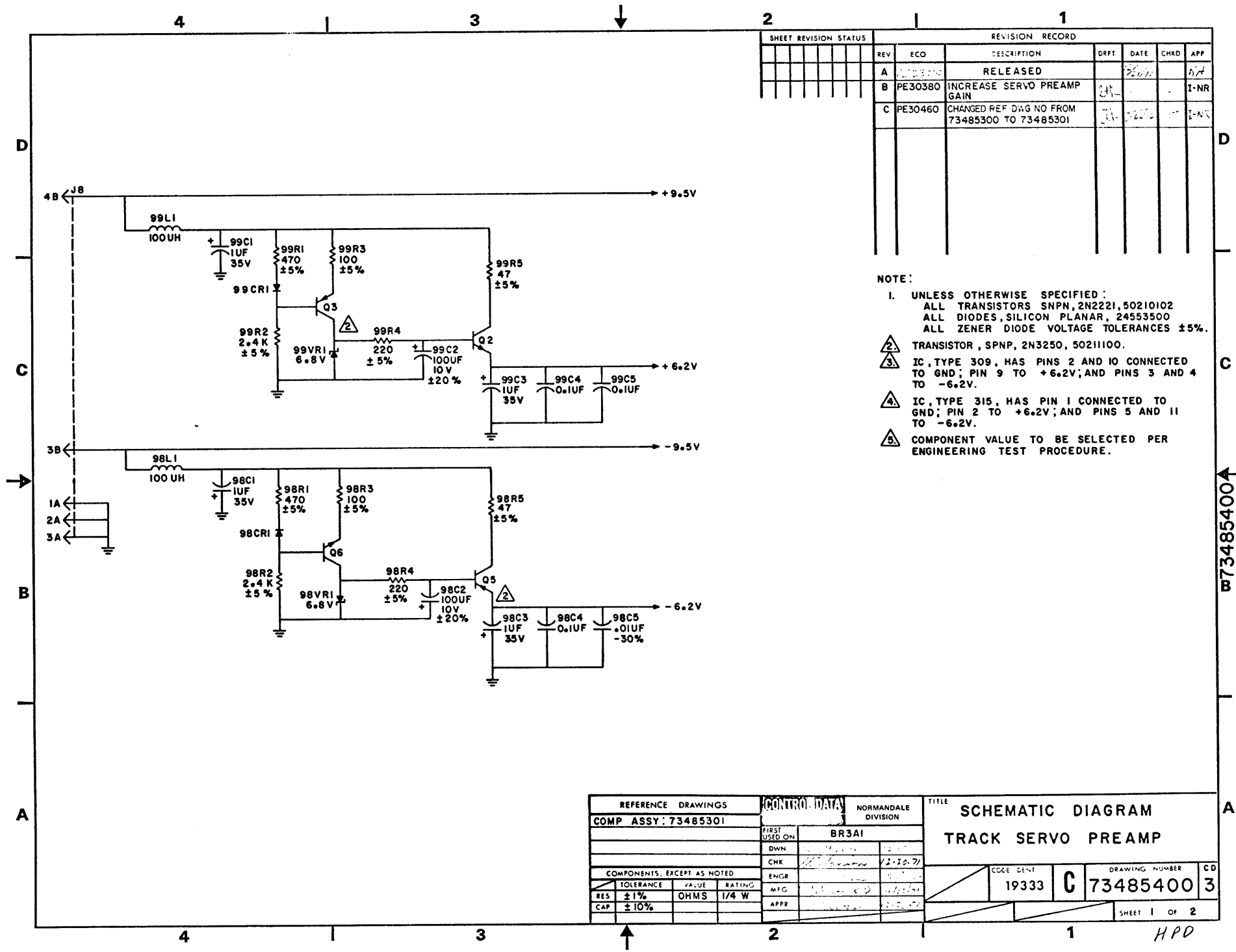
REVISION RECORD						
REV	ECO	DESCRIPTION	DEPT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



SCHEMATIC DIAGRAM
TYPE DZPN

CODE IDENT	DWG NO	CD
19333	72829712	8
SHEET 3		

72829712



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED		12/20/71		HJH	
B	PE30380	INCREASE SERVO PREAMP GAIN				I-NR	
C	PE30460	CHANGED REF DWG NO FROM 73485300 TO 73485301		12/20/71		I-NR	

NOTE:

- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS SNPN, 2N2221, 50210102
ALL DIODES, SILICON PLANAR, 24553500
ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$.
- TRANSISTOR, SPNP, 2N3250, 50211100.
- IC, TYPE 309, HAS PINS 2 AND 10 CONNECTED TO GND; PIN 9 TO +6.2V; AND PINS 3 AND 4 TO -6.2V.
- IC, TYPE 315, HAS PIN 1 CONNECTED TO GND; PIN 2 TO +6.2V; AND PINS 5 AND 11 TO -6.2V.
- COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.

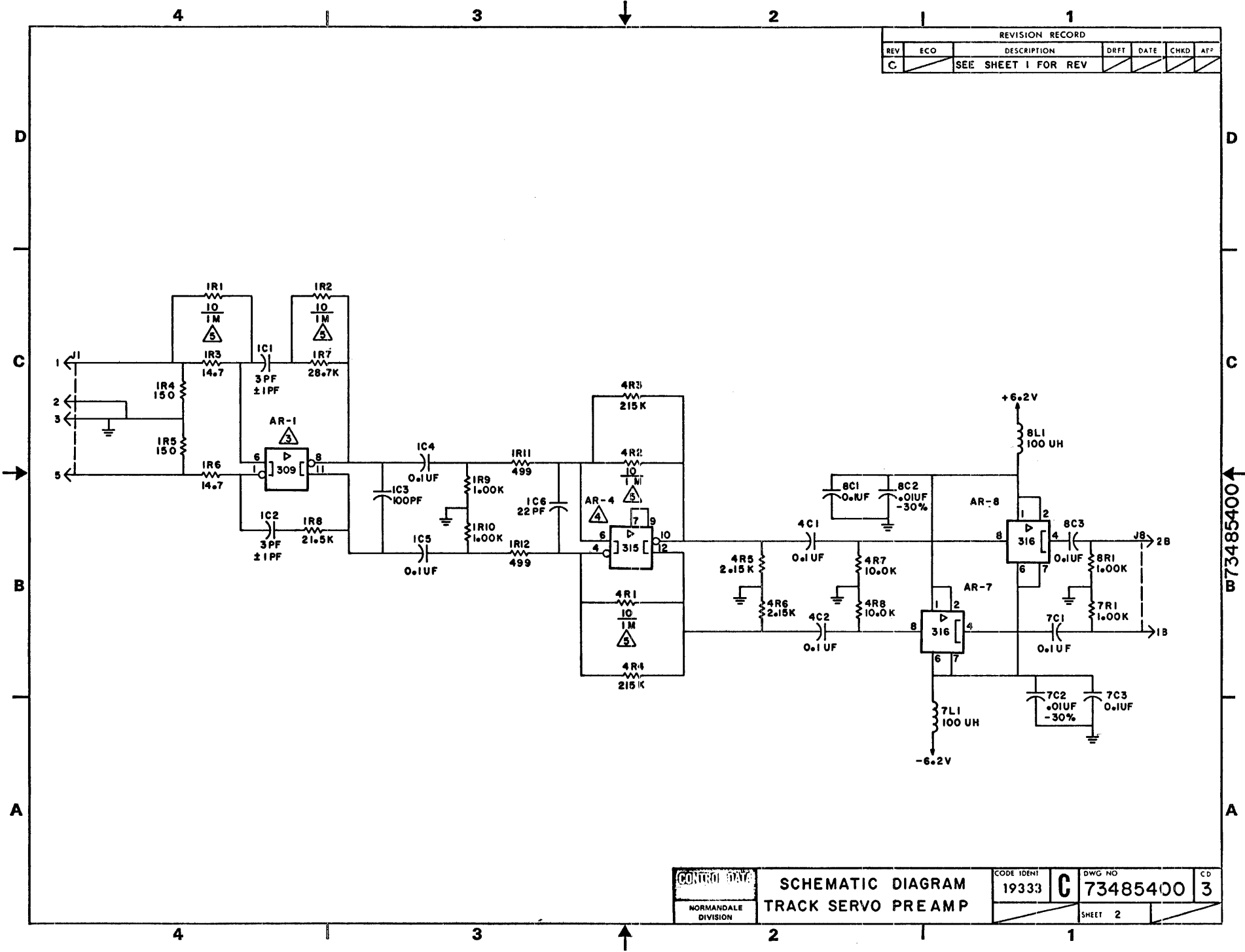
REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMP ASSY: 73485301		FIRST USED ON		BR3A1		SCHEMATIC DIAGRAM	
		DWN				TRACK SERVO PREAMP	
		CHK		12-20-71		CODE IDENT	
		ENGR				DRAWING NUMBER	
		MFG				19333 C 73485400 3	
		APPR				SHEET 1 OF 2	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES		$\pm 1\%$		OHMS		1/4 W	
CAP		$\pm 10\%$					

HPD

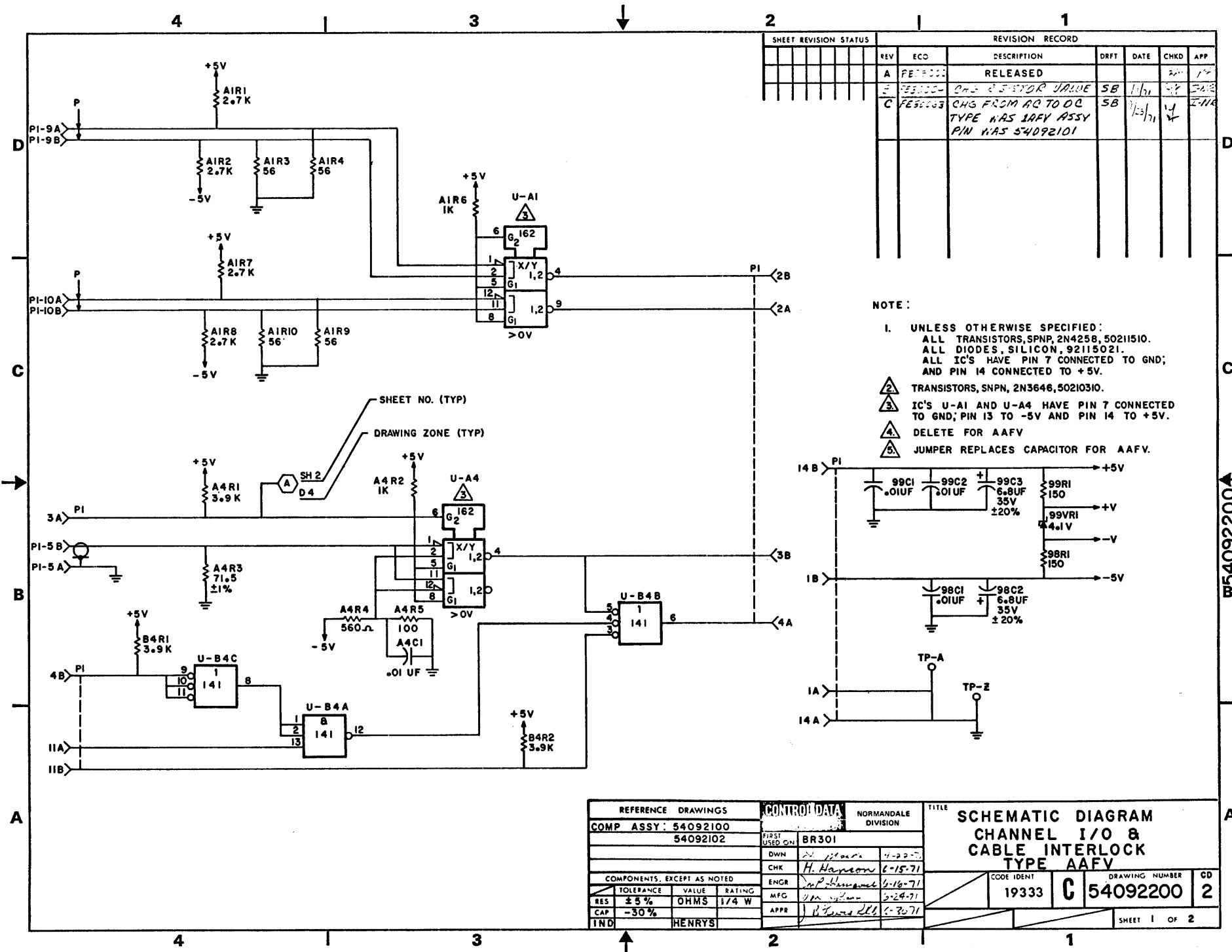
70629100 E

4-5

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
C		SEE SHEET 1 FOR REV				

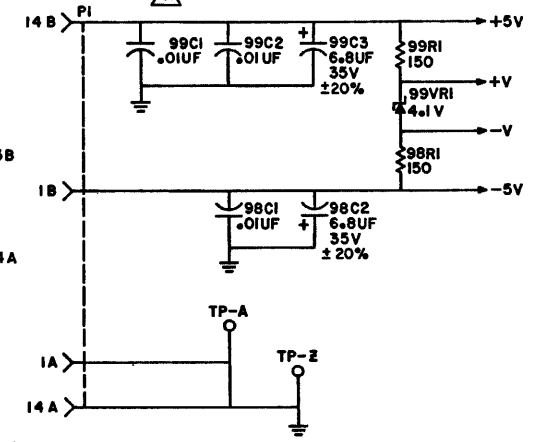


CONTROL DATA NORMANDE DIVISION	SCHEMATIC DIAGRAM TRACK SERVO PREAMP		CODE IDENT 19333	DWG NO C 73485400	CD 3
			SHEET 2		



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE0001	RELEASED					
B	FE0002	CHG RESISTOR VALUE	SB	1/1/71			
C	FE0003	CHG FROM AC TO DC TYPE WAS 14V ASSY PIN WAS 54092101	SB	1/13/71			

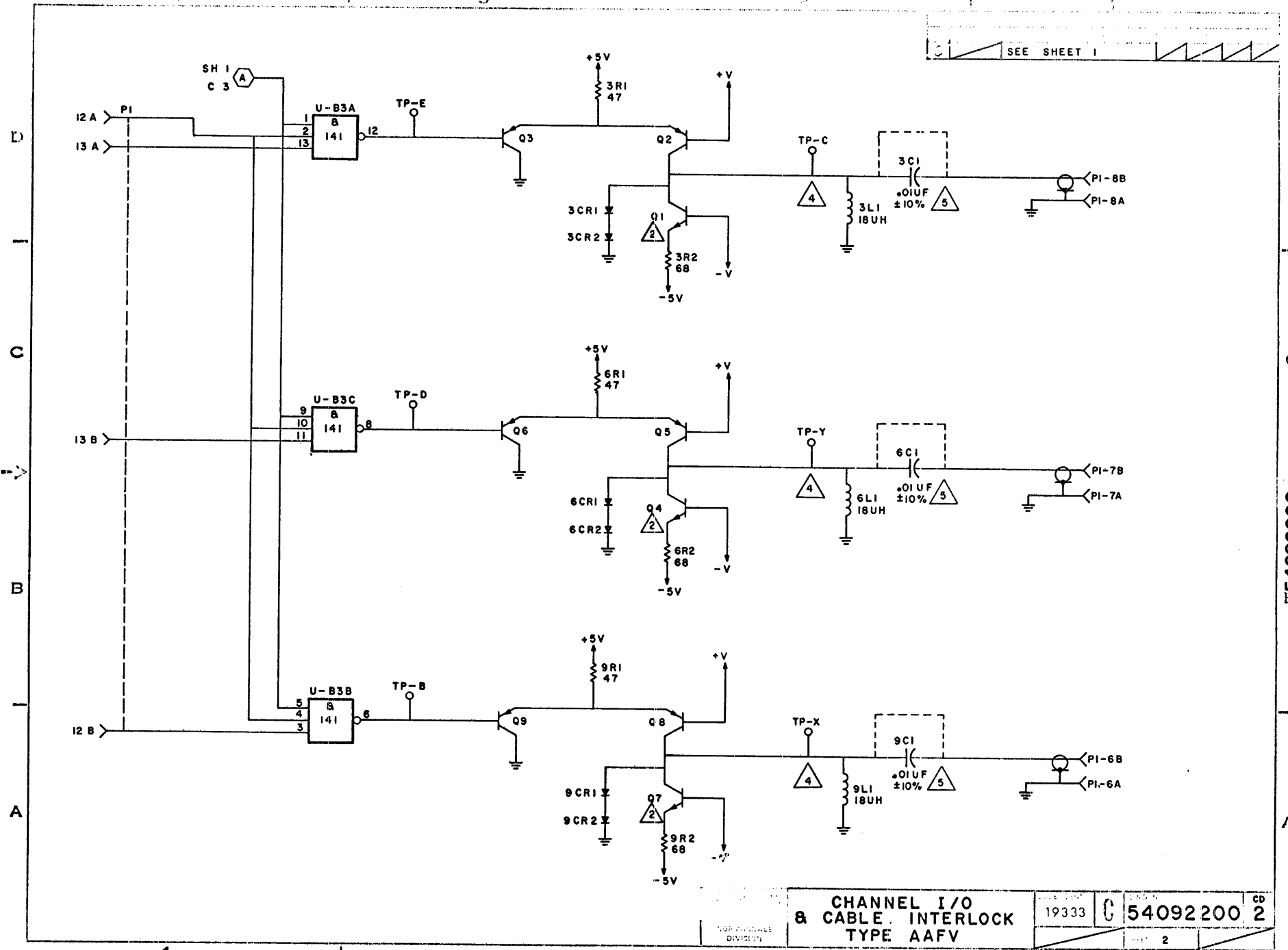
- NOTE:
- 1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SPNP, 2N4256, 50211510.
 ALL DIODES, SILICON, 92115021.
 ALL IC'S HAVE PIN 7 CONNECTED TO GND;
 AND PIN 14 CONNECTED TO +5V.
 - 2. TRANSISTORS, SPNP, 2N3646, 50210310.
 - 3. IC'S U-A1 AND U-A4 HAVE PIN 7 CONNECTED TO GND; PIN 13 TO -5V AND PIN 14 TO +5V.
 - 4. DELETE FOR AAFV
 - 5. JUMPER REPLACES CAPACITOR FOR AAFV.



54092200

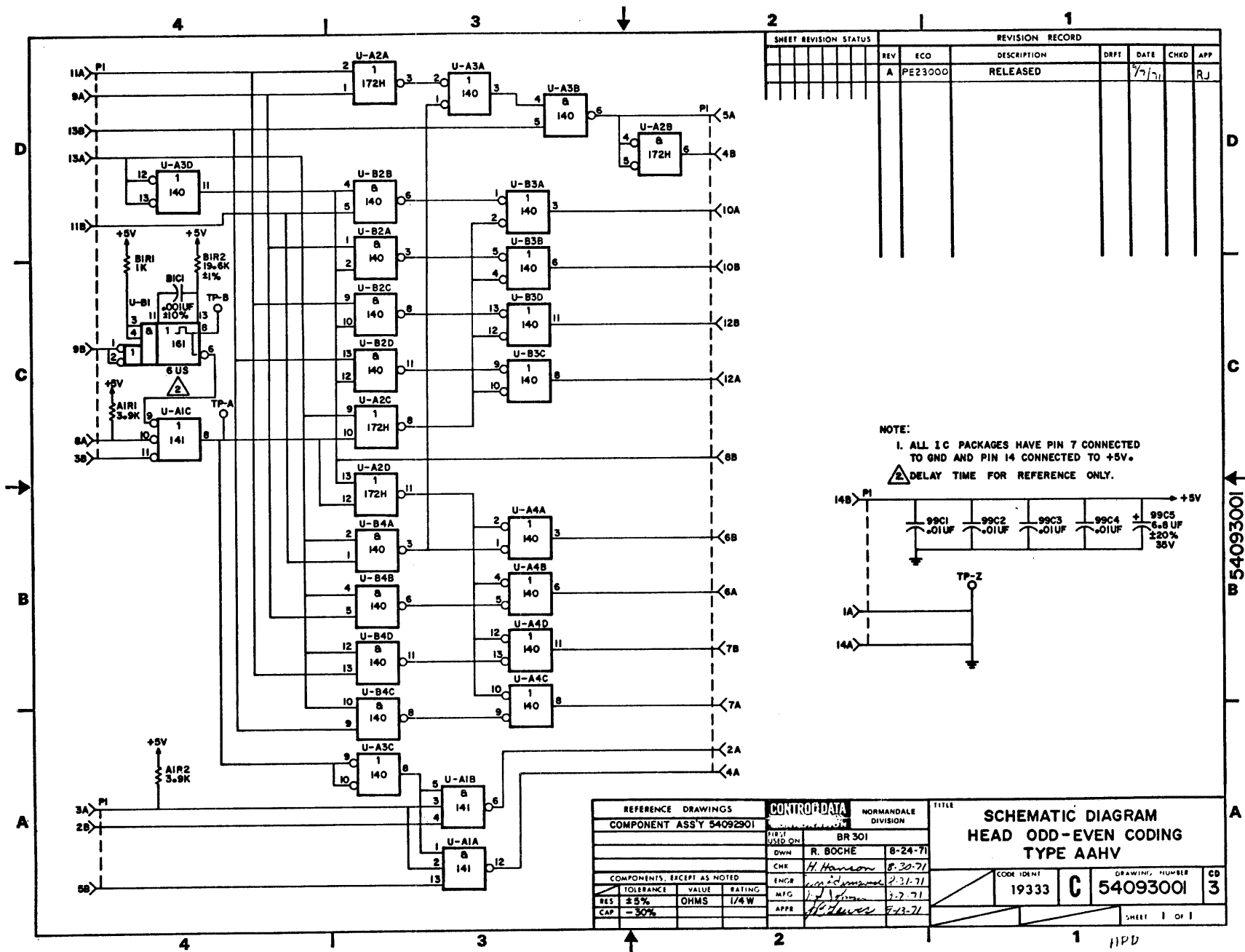
REFERENCE DRAWINGS			CONTROL DATA		NORMANDELE DIVISION		TITLE		
COMP ASSY: 54092100			FIRST USED ON		BR301		SCHEMATIC DIAGRAM		
54092102			OWN		4-22-71		CHANNEL I/O &		
			CHK		H. Hanson 6-15-71		CABLE INTERLOCK		
			ENGR		6-16-71		TYPE AAFV		
			MFG		2-24-71		CODE IDENT		
			APPR		6-30-71		19333		
COMPONENTS, EXCEPT AS NOTED			DRAWING NUMBER		CD		SHEET 1 OF 2		
RES	± 5%	OHMS	1/4 W						
CAP	-30%								
IND	HENRYS								

SEE SHEET 1



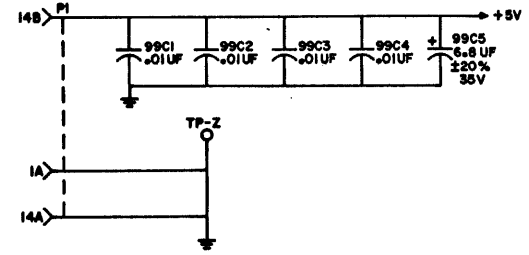
54092200

TOP SECRET DIVISION	CHANNEL I/O & CABLE INTERLOCK TYPE AAFV		19333	54092200	2	CD
			2			



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED		7/7/71		RJ	

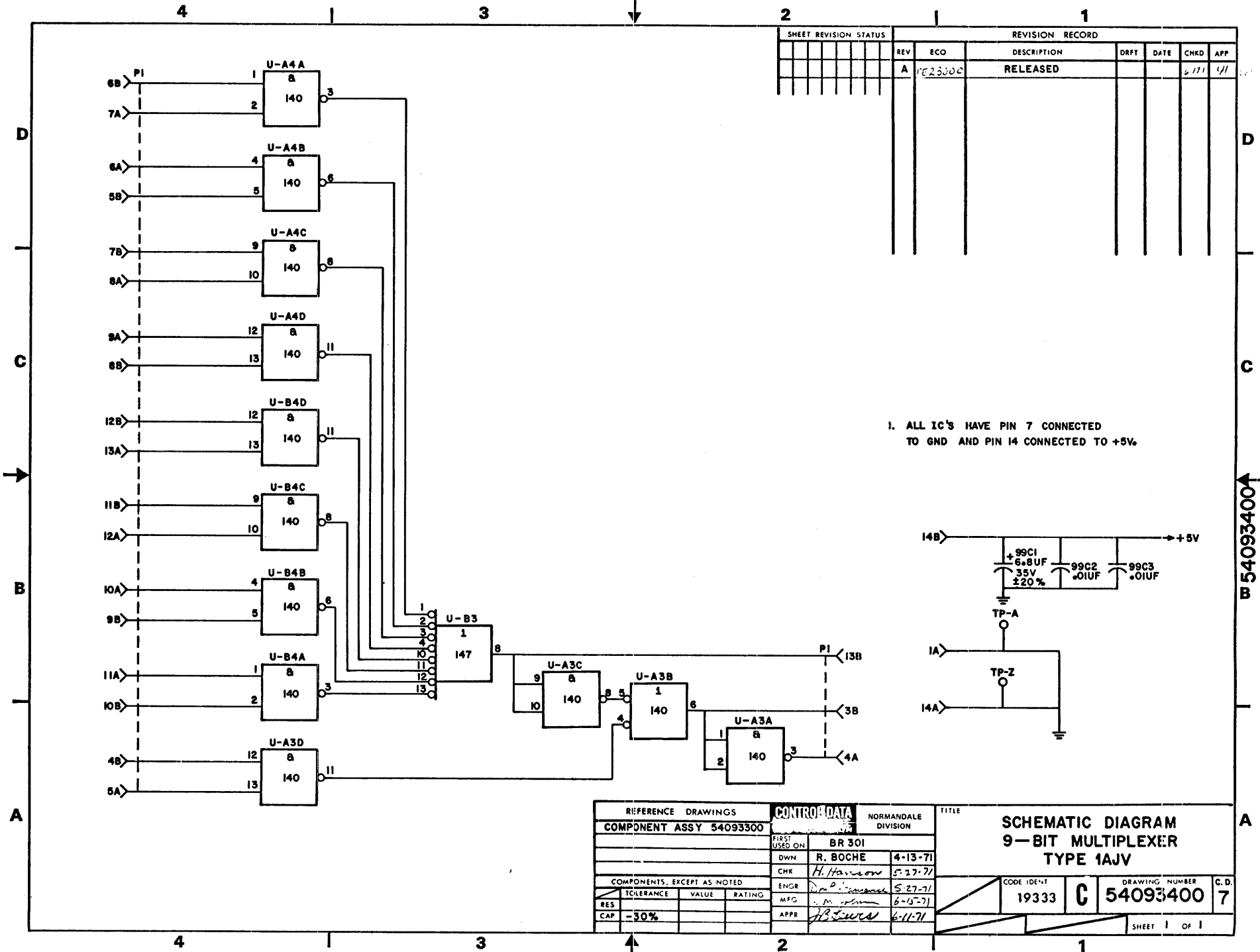
NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ⚠ DELAY TIME FOR REFERENCE ONLY.



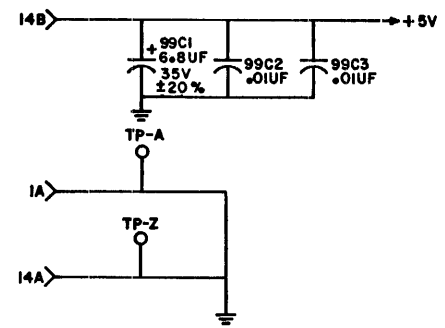
REFERENCE DRAWINGS	CONTROL DATA	NORMANDAILE DIVISION	TITLE	
COMPONENT ASS'Y 54092901	FIRST USED ON	BR 301	SCHEMATIC DIAGRAM	
	DWN	R. BOCHÉ	HEAD ODD-EVEN CODING	
	CHK	H. Hanson	TYPE AAHV	
COMPONENTS, EXCEPT AS NOTED		ENGR	CODE IDENT	DRAWING NUMBER
TOLERANCE	VALUE	RATING	19333	C 54093001
RES ±5%	OHMS	1/4 W	APPR	CD 3
CAP -30%				

B 54093001

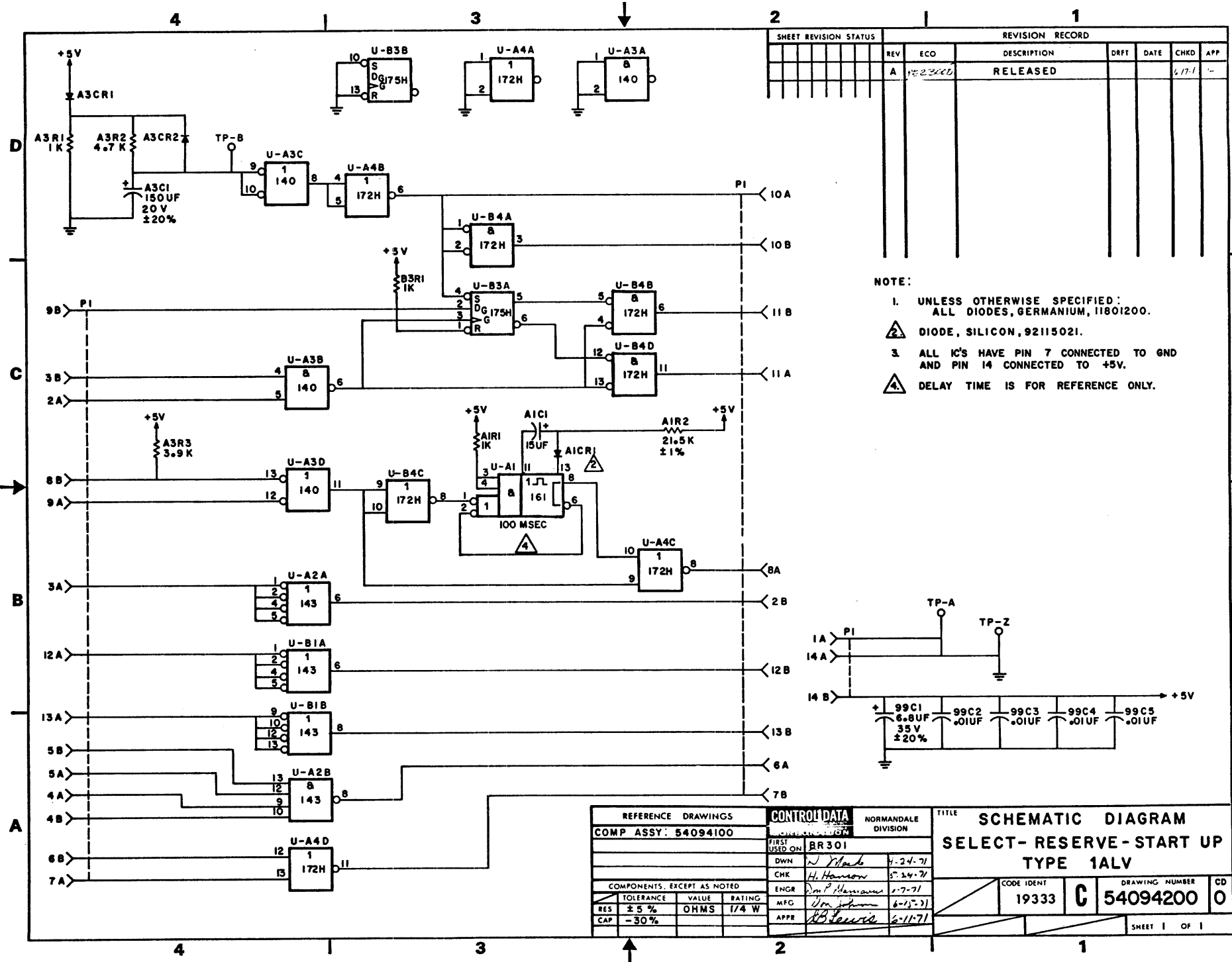
SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	162500c	RELEASED				6/11/71	1/1



1. ALL IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

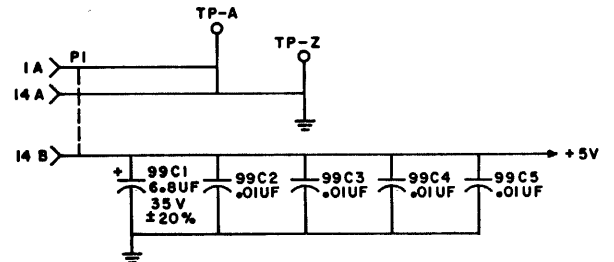


REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54093300			BR 301				SCHEMATIC DIAGRAM 9-BIT MULTIPLEXER TYPE 1AJV	
			FIRST USED ON					
			DWN	R. BOCHE	4-13-71			
			CHK	H. Harrison	5-27-71			
			ENGR	D. P. [Signature]	5-27-71			
			MFG	M. [Signature]	6-15-71			
			APPR	J.B. [Signature]	6-11-71			
COMPONENTS, EXCEPT AS NOTED							CODE IDENT	DRAWING NUMBER
RES	TOLERANCE	VALUE	RATING			19333	C 54093400	C.D. 7
CAP	-50%							
								SHEET 1 OF 1



SHEET REVISION STATUS				REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	122300	RELEASED						

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL DIODES, GERMANIUM, 11801200.
 - DIODE, SILICON, 92115021.
 - ALL IC'S HAVE PIN 7 CONNECTED TO GND
AND PIN 14 CONNECTED TO +5V.
 - DELAY TIME IS FOR REFERENCE ONLY.

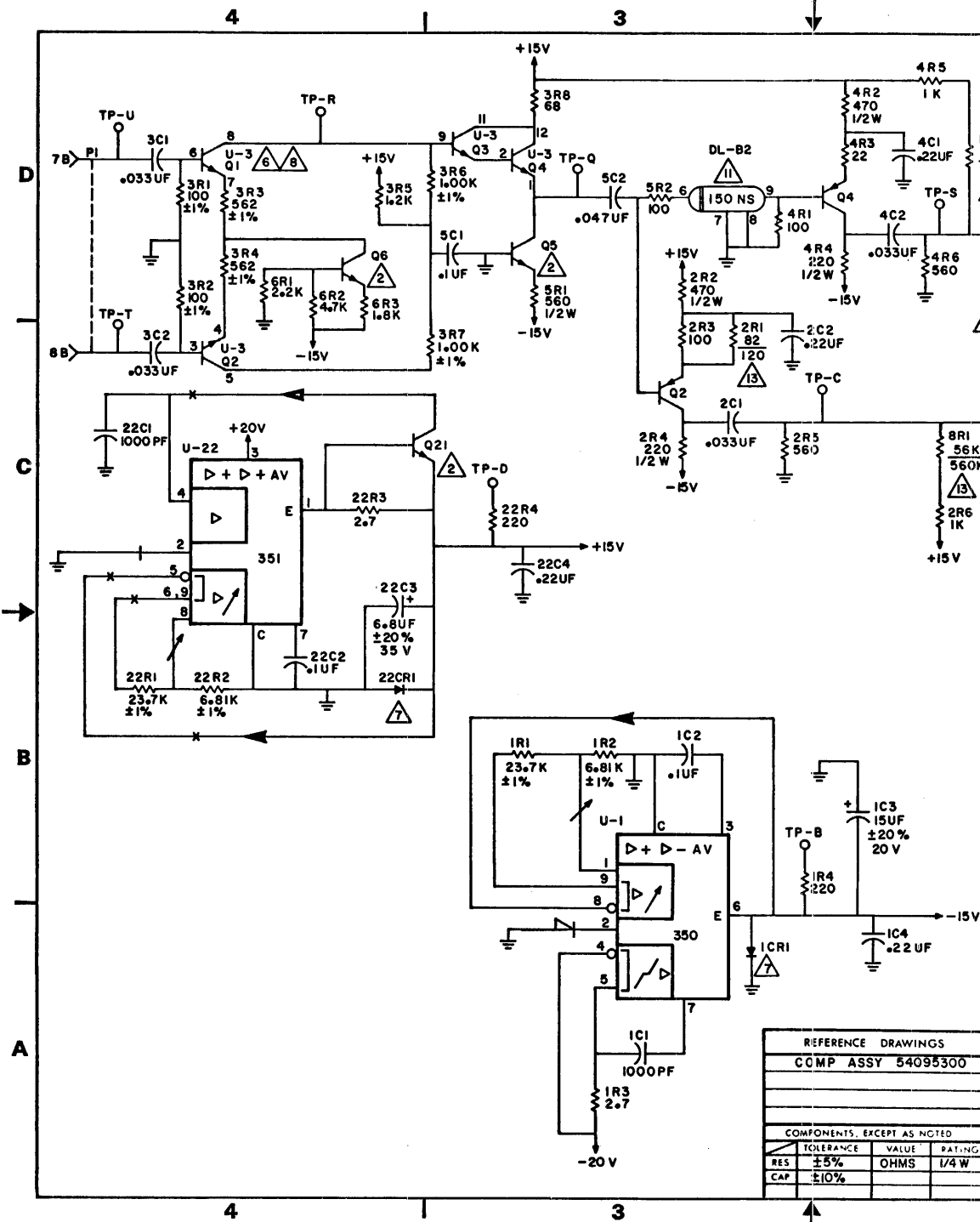
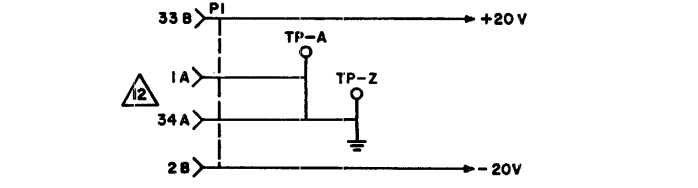


REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE		
COMP ASSY: 54094100			FIRST USED ON	BR 301			SCHEMATIC DIAGRAM		
			DWN	<i>N. Mank</i>	4-24-71		SELECT-RESERVE-START UP		
			CHK	<i>H. Hanson</i>	5-24-71		TYPE 1ALV		
			ENGR	<i>W.P. Harrison</i>	1-7-71		CODE IDENT	DRAWING NUMBER	CD
COMPONENTS, EXCEPT AS NOTED			MFG	<i>Van Johnson</i>	6-15-71		19333	C 54094200	0
TOLERANCE	VALUE	RATING	APPR	<i>B.B. Lewis</i>	6-11-71		SHEET 1 OF 1		
RES ± 5 %	OHMS	1/4 W							
CAP -30 %									

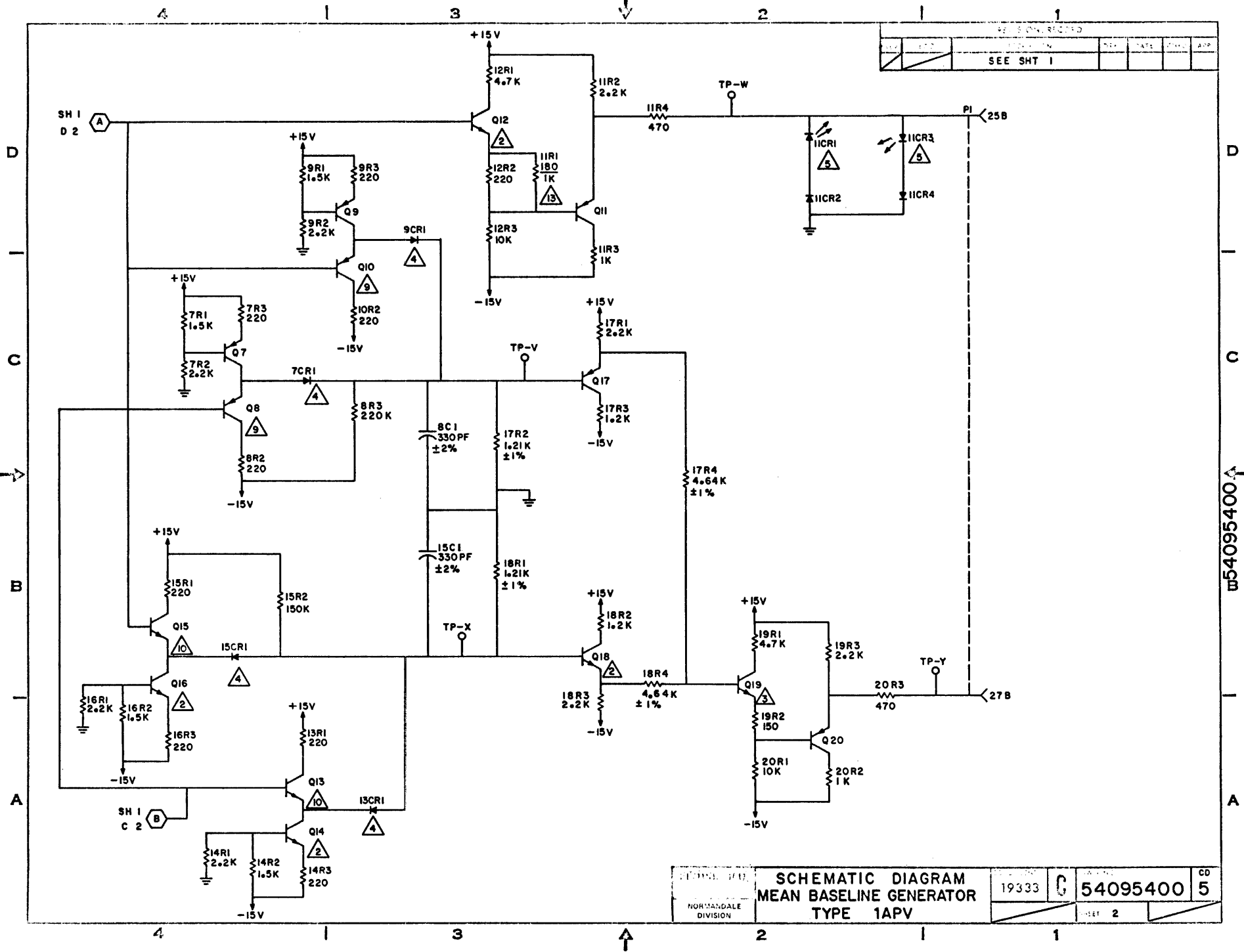
B54094200

SHEET REVISION STATUS				REVISION RECORD				
REV	ECD	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	PEL3000	RELEASED						

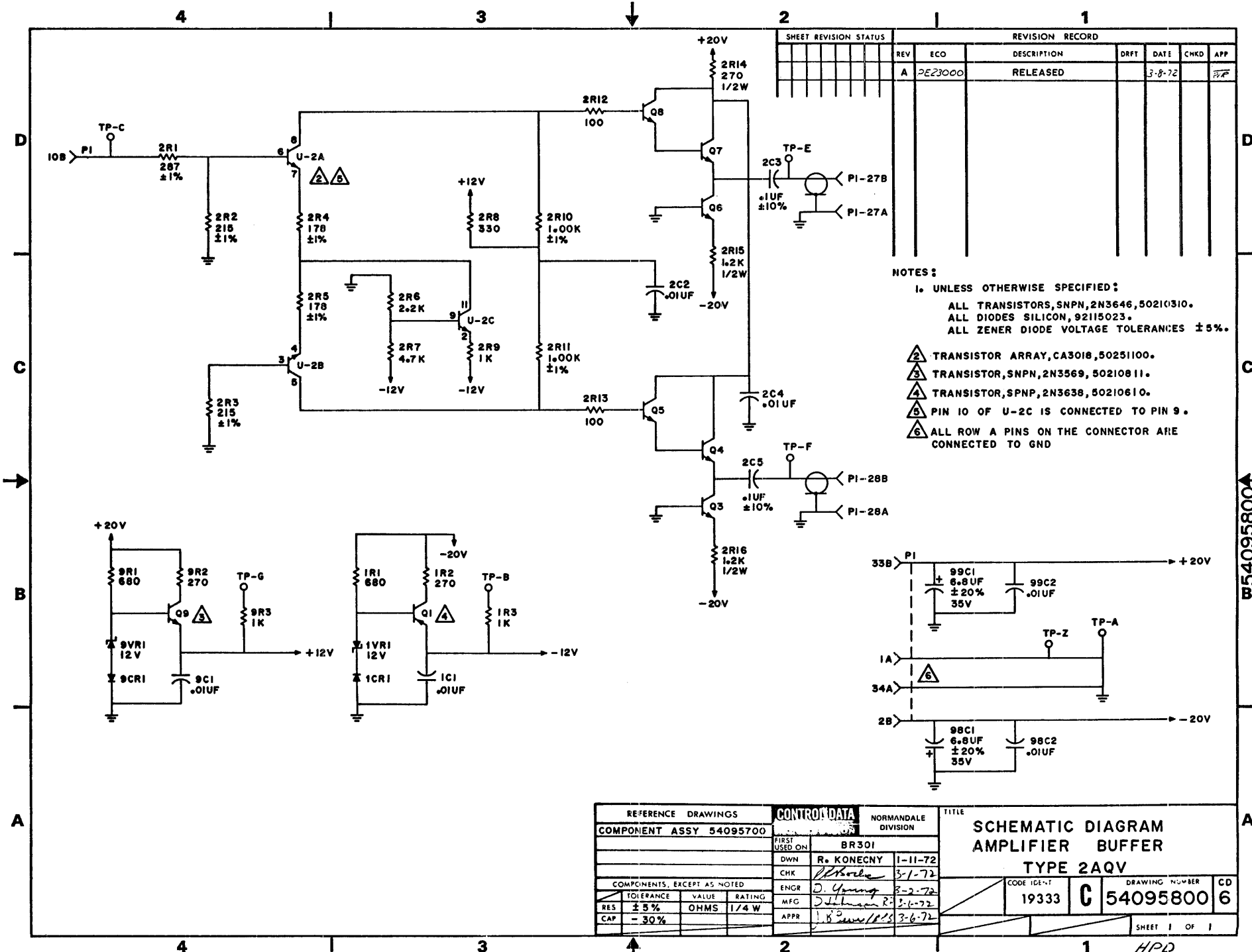
- I. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SPNP, 2N4916, 50211610.
 ALL DIODES, SILICON, 92115021
- ② TRANSISTOR, SPNP, 2N3646, 50210310.
 - ③ TRANSISTOR, SPNP, 2N3642, 50210510,
 - ④ DIODES 9C1, 7C1, 15C1, 13C1 ARE SILICON MATCHED QUAD, 92115039.
 - ⑤ DIODE, LIGHT EMITTING 94256300.
 - ⑥ IC U-3, TRANSISTOR ARRAY, HAS PIN 10 CONNECTED TO BASE OF Q6.
 - ⑦ DIODE, GERMANIUM, 11801200.
 - ⑧ TRANSISTOR ARRAY, 50251100.
 - ⑨ TRANSISTORS Q8, Q10 ARE SPNP, MATCHED PAIR, 50211612.
 - ⑩ TRANSISTORS Q13, Q15 ARE SPNP, MATCHED PAIR, 50210311.
 - ⑪ DELAY LINE, 94262304
 - ⑫ ALL "A" ROW PINS GROUNDED.
 - ⑬ RESISTORS 2R1, 8R1, 10R1 AND 11R1 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.



REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY 54095300	BR501		SCHEMATIC DIAGRAM MEAN BASELINE GENERATOR TYPE 1APV
FIRST USED ON	DWN	D. G. TUTTLE	5-25-71
CHK	CHK	R. Both	7-26-71
ENGR	MFC		
APPR			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES	±5%	OHMS	1/4 W
CAP	±10%		
19333	19333	C	54095400
DRAWING NUMBER		CD	5
SHEET 1 OF 2			HPD



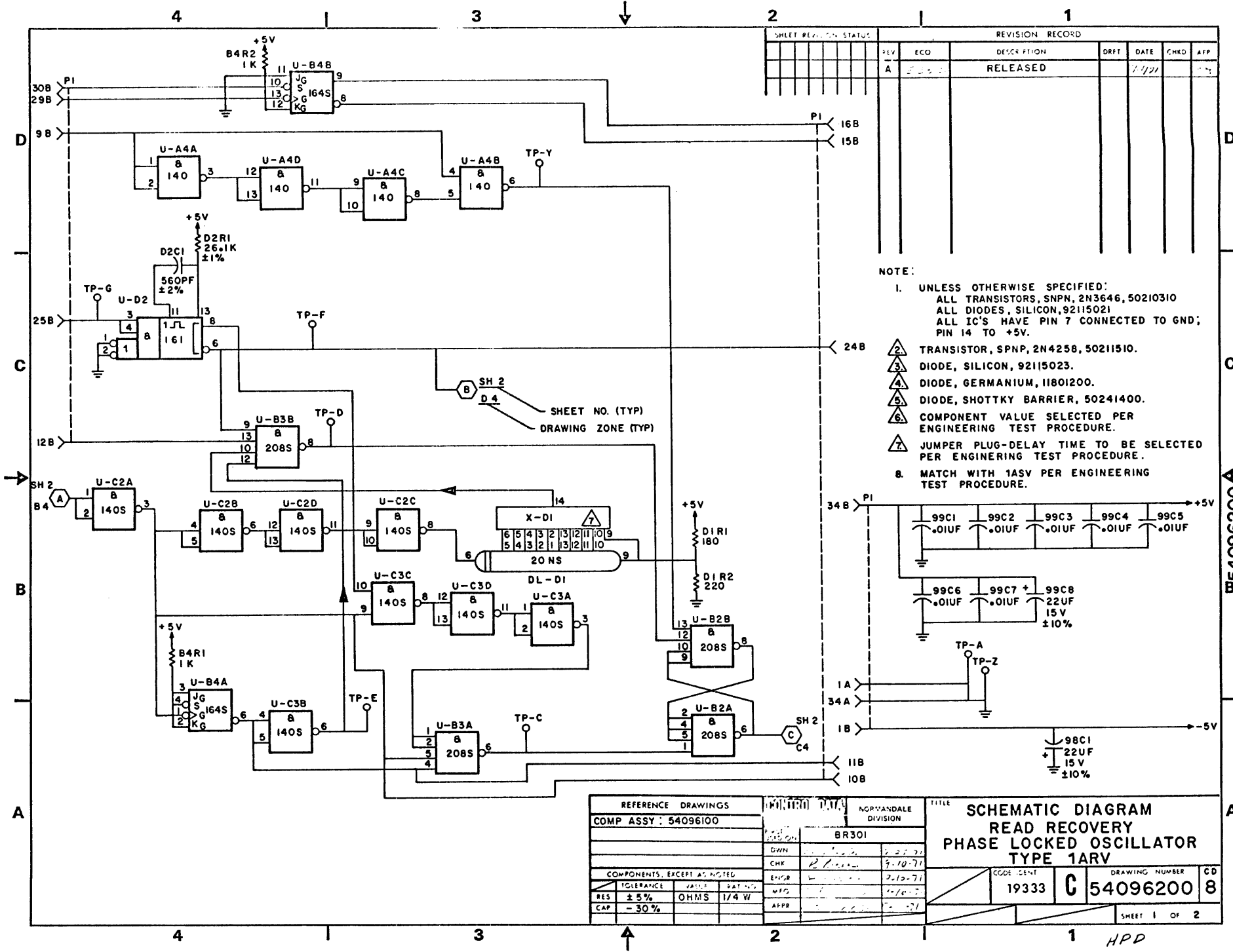
54095400



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED		3-8-72		PP	

- NOTES:
- 1. UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SNPN, 2N3646, 50210310.
ALL DIODES SILICON, 92115023.
ALL ZENER DIODE VOLTAGE TOLERANCES ± 5%.
 - 2. TRANSISTOR ARRAY, CA3018, 50251100.
 - 3. TRANSISTOR, SNPN, 2N3569, 50210811.
 - 4. TRANSISTOR, SPNP, 2N3638, 50210610.
 - 5. PIN 10 OF U-2C IS CONNECTED TO PIN 9.
 - 6. ALL ROW A PINS ON THE CONNECTOR ARE CONNECTED TO GND

REFERENCE DRAWINGS		CONTRON DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54095700		FIRST USED ON		BR 301		SCHEMATIC DIAGRAM	
		DWN		R. KONECNY		AMPLIFIER BUFFER	
		CHK		<i>[Signature]</i>		TYPE 2A QV	
		ENGR		D. Young		CODE IDENT	
		MFG		D. Johnson		DRAWING NUMBER	
		APPR		J. B. [Signature]		CD	
COMPONENTS, EXCEPT AS NOTED		RES ± 5%		OHMS		19333	
		CAP - 30%		1/4 W		C 54095800	
						6	
						SHEET 1 OF 1	
						HPD	



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED		11/77			

NOTE:

- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SNPN, 2N3646, 50210310
ALL DIODES, SILICON, 92115021
ALL IC'S HAVE PIN 7 CONNECTED TO GND;
PIN 14 TO +5V.
- TRANSISTOR, SPNP, 2N4258, 50211510.
- DIODE, SILICON, 92115023.
- DIODE, GERMANIUM, 11801200.
- DIODE, SHOTTKY BARRIER, 50241400.
- COMPONENT VALUE SELECTED PER
ENGINEERING TEST PROCEDURE.
- JUMPER PLUG-DELAY TIME TO BE SELECTED
PER ENGINEERING TEST PROCEDURE.
- MATCH WITH 1ASV PER ENGINEERING
TEST PROCEDURE.

REFERENCE DRAWINGS		NORMANDAILE DIVISION	
COMP ASSY : 54096100		BR301	
COMPONENTS, EXCEPT AS NOTED		CHK	9-10-77
RES ± 5%	OHMS 1/4 W	ENGR	2-12-77
CAP - 30%		APP	1-10-77

TITLE			
SCHEMATIC DIAGRAM READ RECOVERY PHASE LOCKED OSCILLATOR TYPE 1ARV			
CODE IDENT	DRAWING NUMBER	CD	
19333	C 54096200	8	
SHEET 1 OF 2			

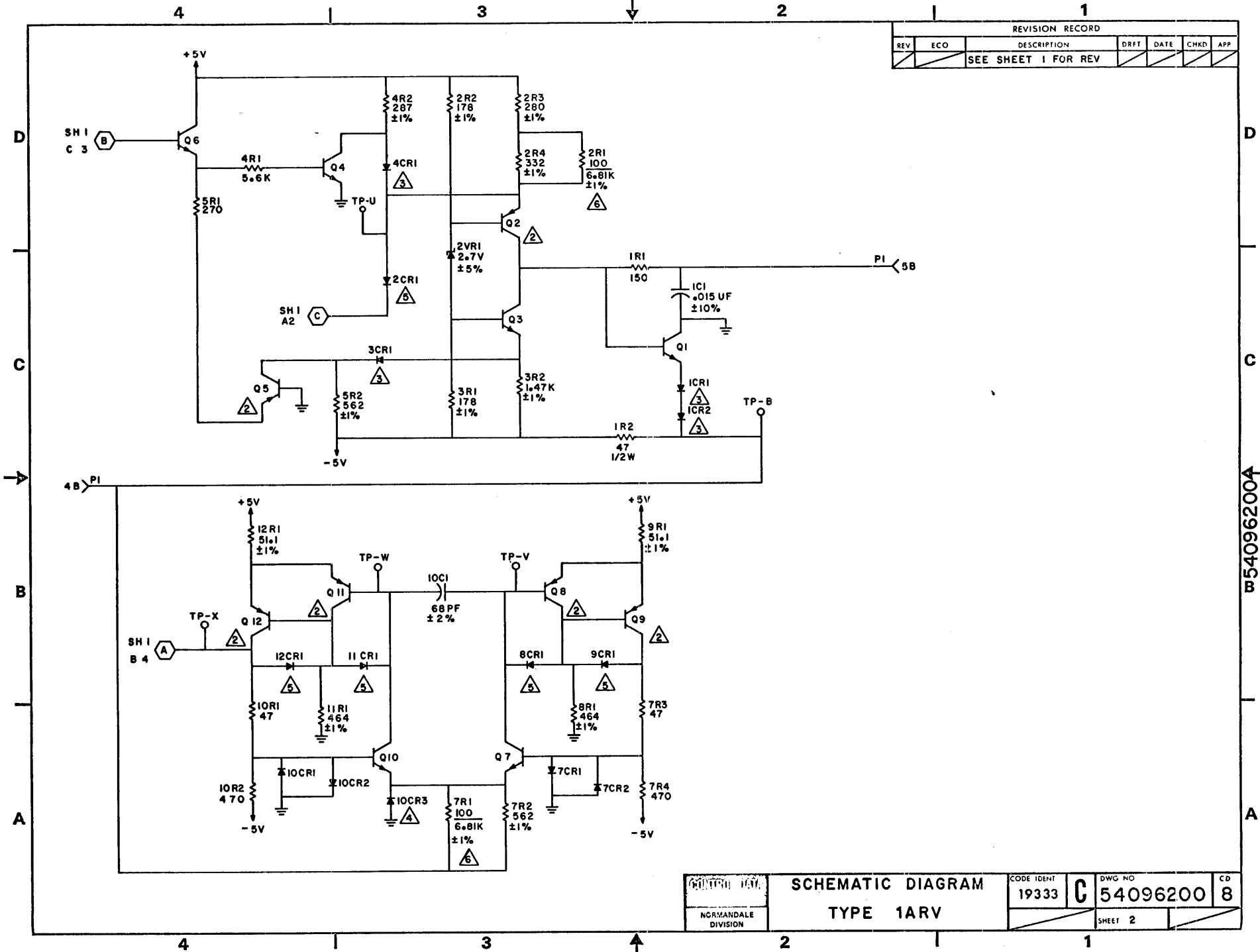
54096200

HPP

70629100 E

4-15

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				

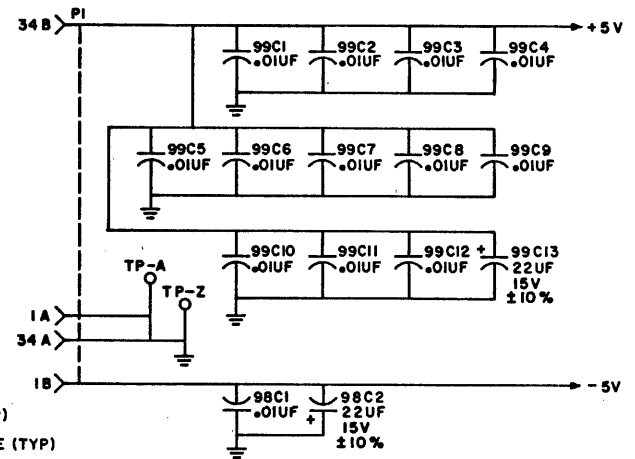
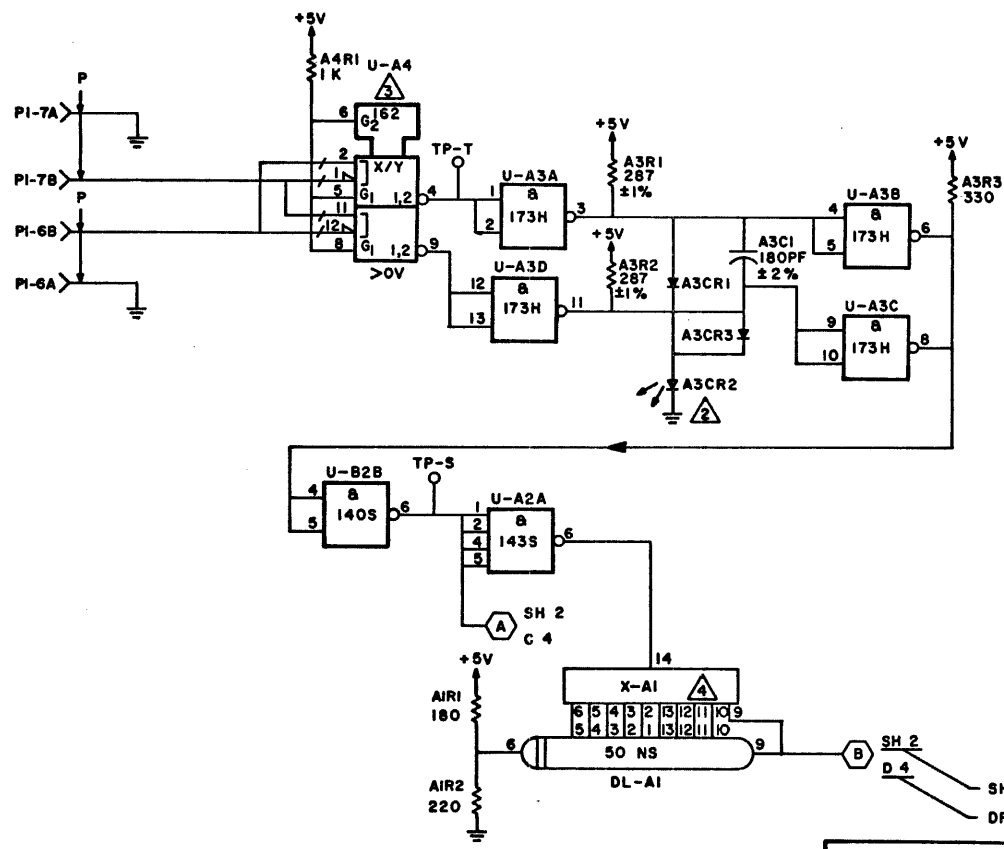


NORMAN DALE DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
	TYPE 1ARV		19333	C 54096200	8
			SHEET 2		

54096200A

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23000	RELEASED		7/17/71		RH	

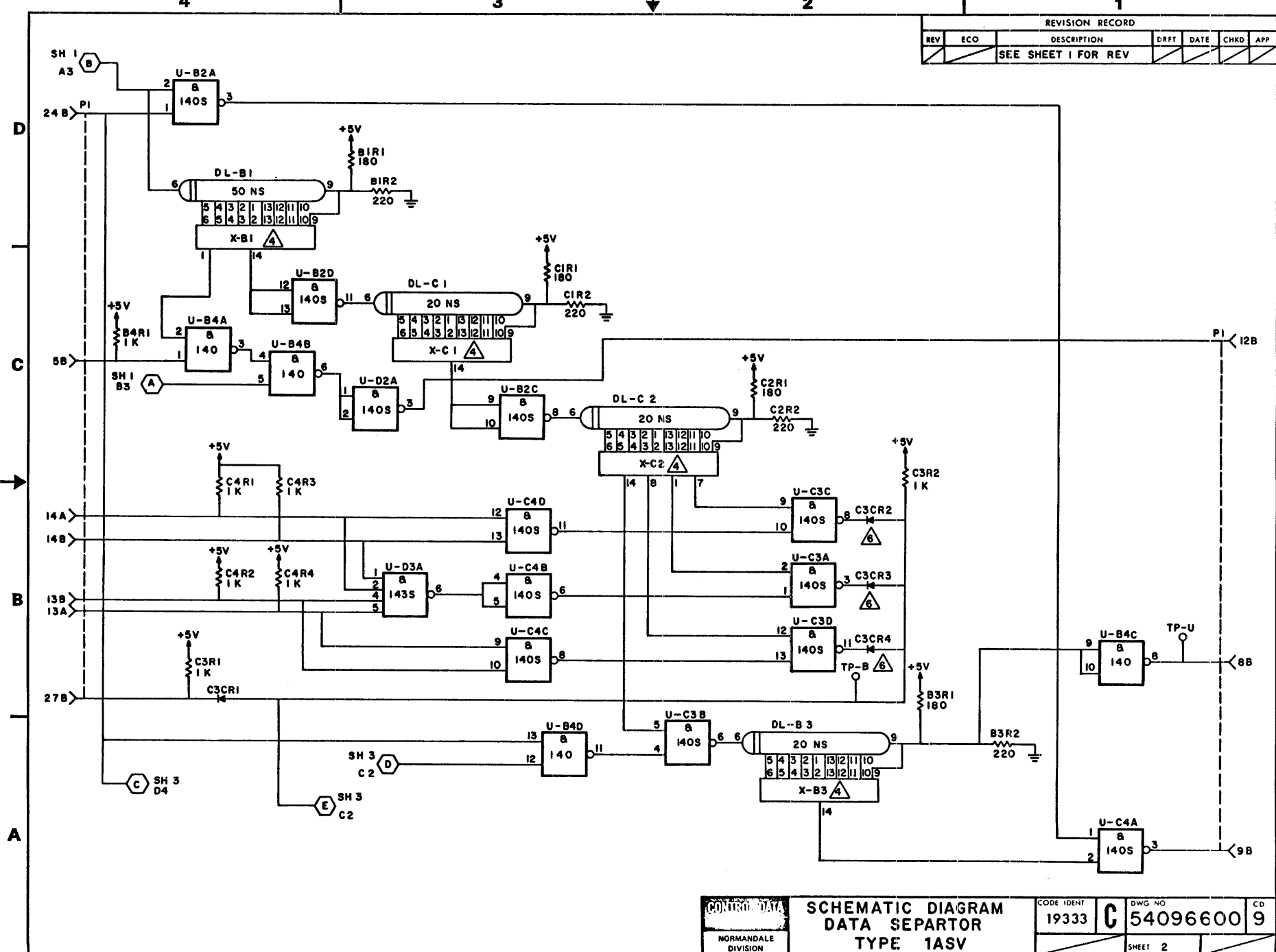
- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL DIODES, SILICON, 92115023.
ALL IC'S HAVE PIN 7 CONNECTED TO GND, PIN 14 CONNECTED TO +5V.
 - DIODE, LIGHT EMITTING, 94256300.
 - IC U-A4 HAS PIN 13 CONNECTED TO -5V.
 - JUMPER PLUG - DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 - MATCHED WITH 1ARV PER ENG. TEST PROCEDURE
 - DIODE, SHOTTKY BARRIER, 50241400.



SHEET NO. (TYP)
DRAWING ZONE (TYP)

REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY : 54096500	BR301		SCHEMATIC DIAGRAM DATA SEPARATOR TYPE 1ASV
COMPONENTS, EXCEPT AS NOTED	ENGR	MFG	CODE IDENT
TOLERANCE	VALUE	RATING	19333
RES ±5%	OHMS	1/4 W	DRAWING NUMBER C 54096600
CAP -30%			
SHEET 1 OF 3			HPD

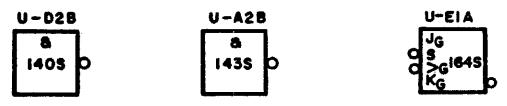
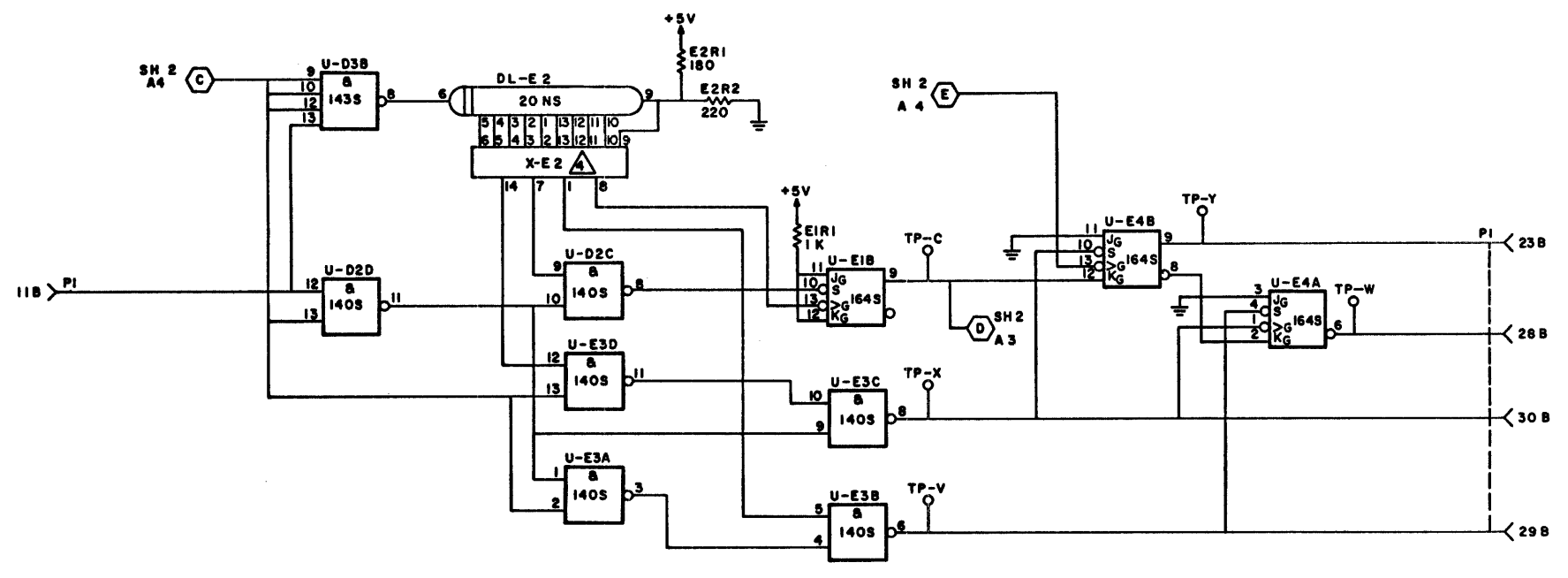
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDE DIVISION	SCHEMATIC DIAGRAM DATA SEPARATOR TYPE 1ASV		CODE IDENT 19333	C	DWG NO 54096600	9
			SHEET 2			

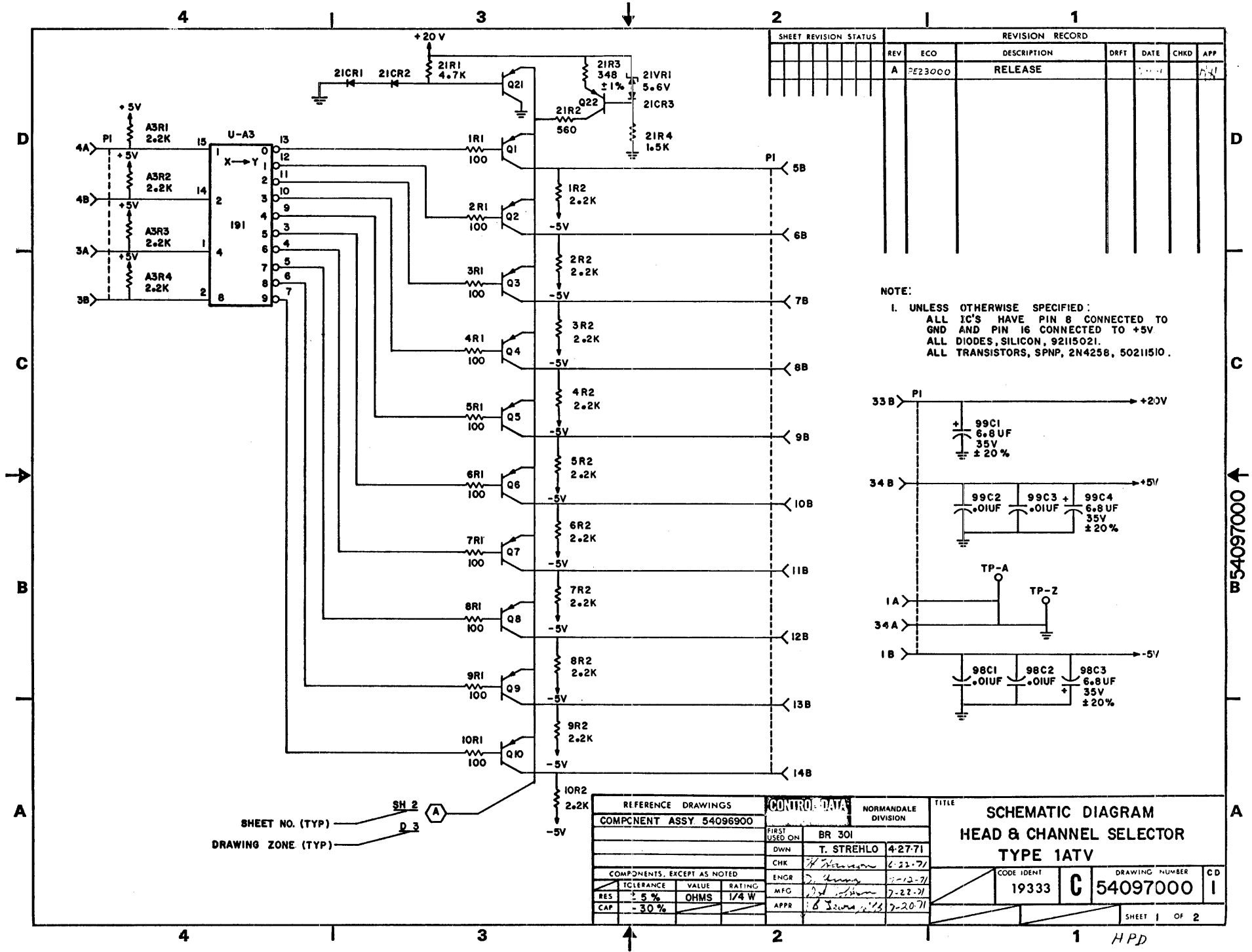
54096600

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



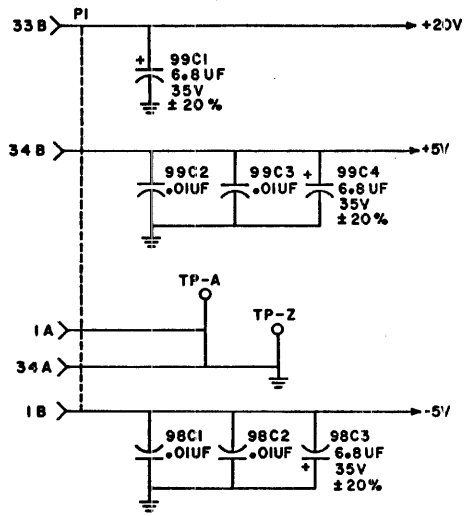
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM DATA SEPARATOR TYPE 1ASV		CODE IDENT 19333	DWG NO 54096600	CD 9
			SHEET 3		

54096600



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE23000	RELEASE					

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL IC'S HAVE PIN 6 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V
 ALL DIODES, SILICON, 92115021.
 ALL TRANSISTORS, SPNP, 2N4258, 50211510.

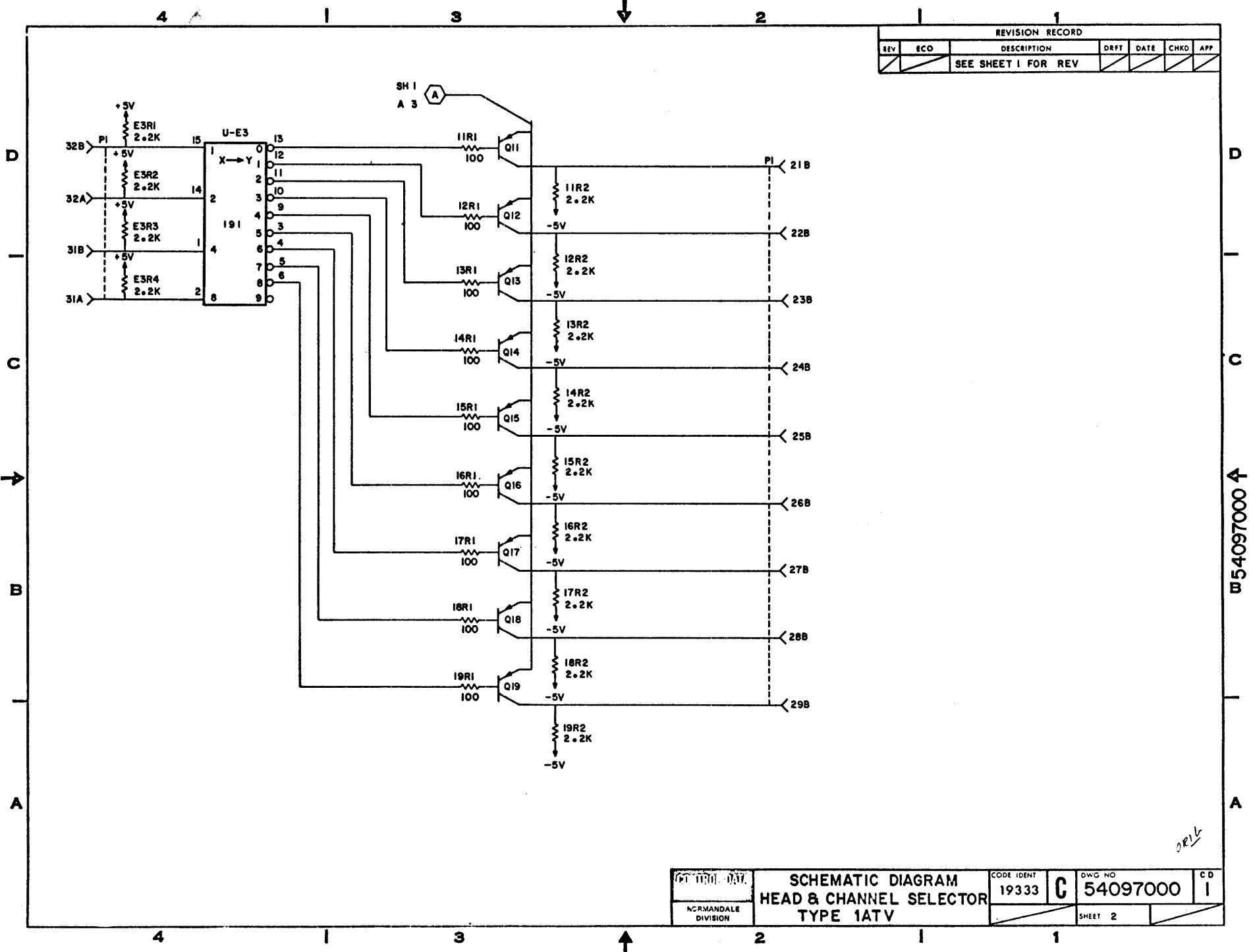


SHEET NO. (TYP) SH 2
 DRAWING ZONE (TYP) D 3

REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54096900			FIRST USED ON		BR 301		SCHEMATIC DIAGRAM	
			DWN		T. STREHLO 4-27-71		HEAD & CHANNEL SELECTOR	
			CHK		7/2/71		TYPE 1ATV	
COMPONENTS, EXCEPT AS NOTED			ENGR		7-12-71		CODE IDENT	
RES ± 5 %			MFG		7-22-71		DRAWING NUMBER	
CAP - 30 %			APPR		7-20-71		19333 C 54097000 I	
							SHEET 1 OF 2	

HPD

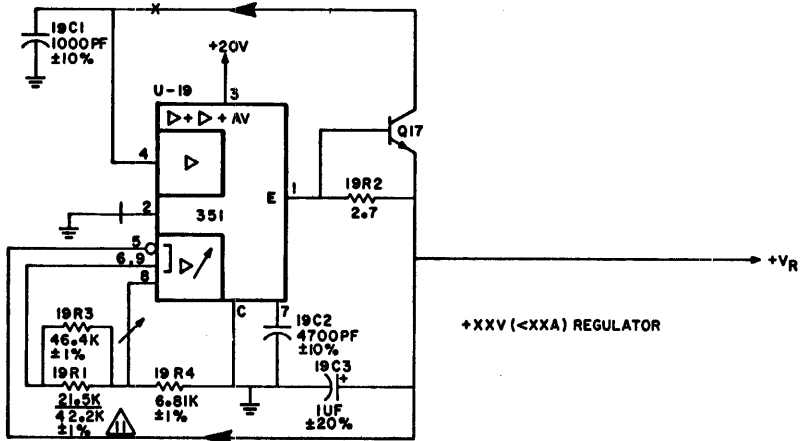
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



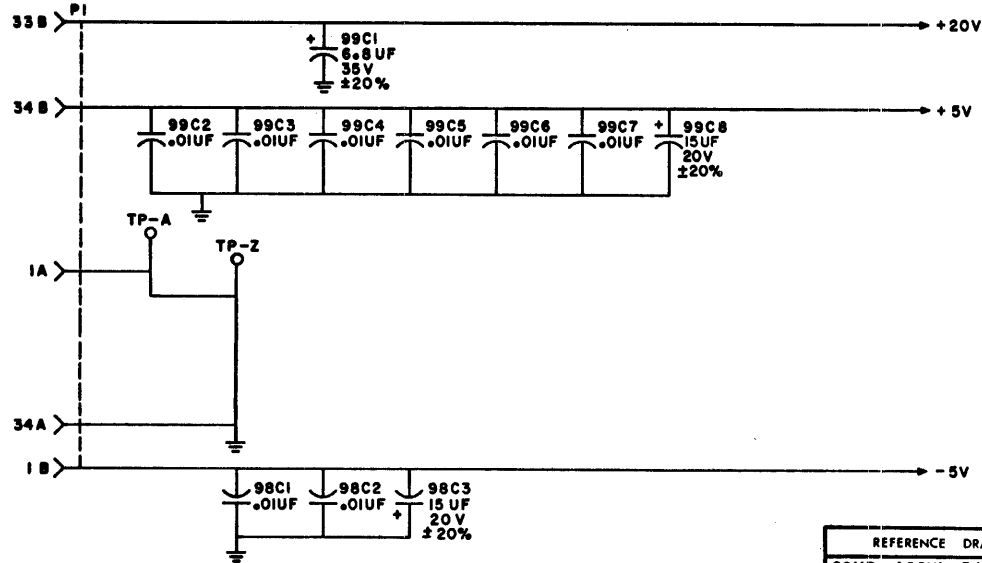
<small>19333</small> NCRMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD & CHANNEL SELECTOR TYPE 1ATV		<small>CODE IDENT</small> 19333	<small>DWG NO</small> C 54097000	<small>CD</small> 1
				<small>SHEET 2</small>	

DRILL

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	223000	RELEASED		1/14/62			



- NOTE:
1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N3646, 50210310
 ALL DIODES, SILICON, PLANAR, 24553500
 ALL IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V.
 2. TRANSISTOR, SPNP, 2N5456, 50212100
 3. TRANSISTOR, SPNP, 2N4916, 50211610.
 4. TRANSISTOR, SPNP, 2N4258, 50211510.
 5. TRANSISTOR, SPNP, 2N3645, 50211210.
 6. TRANSISTOR, SPNP, 2N3638, 50210610.
 7. TRANSISTOR, SNPN, 2N4923, 50220902.
 8. TRANSISTOR, SNPN, PLANAR, 24562100.
 9. DIODE, SILICON, 50241400.
 10. DIODE, GERMANIUM, 11801200.
 11. RESISTOR SELECTED PER ENGINEERING TEST PROCEDURE.
 12. IC'S U-B4 AND U-D3 HAVE PIN 7 CONNECTED TO GND, PIN 13 CONNECTED TO -5V AND PIN 14 CONNECTED TO +5V



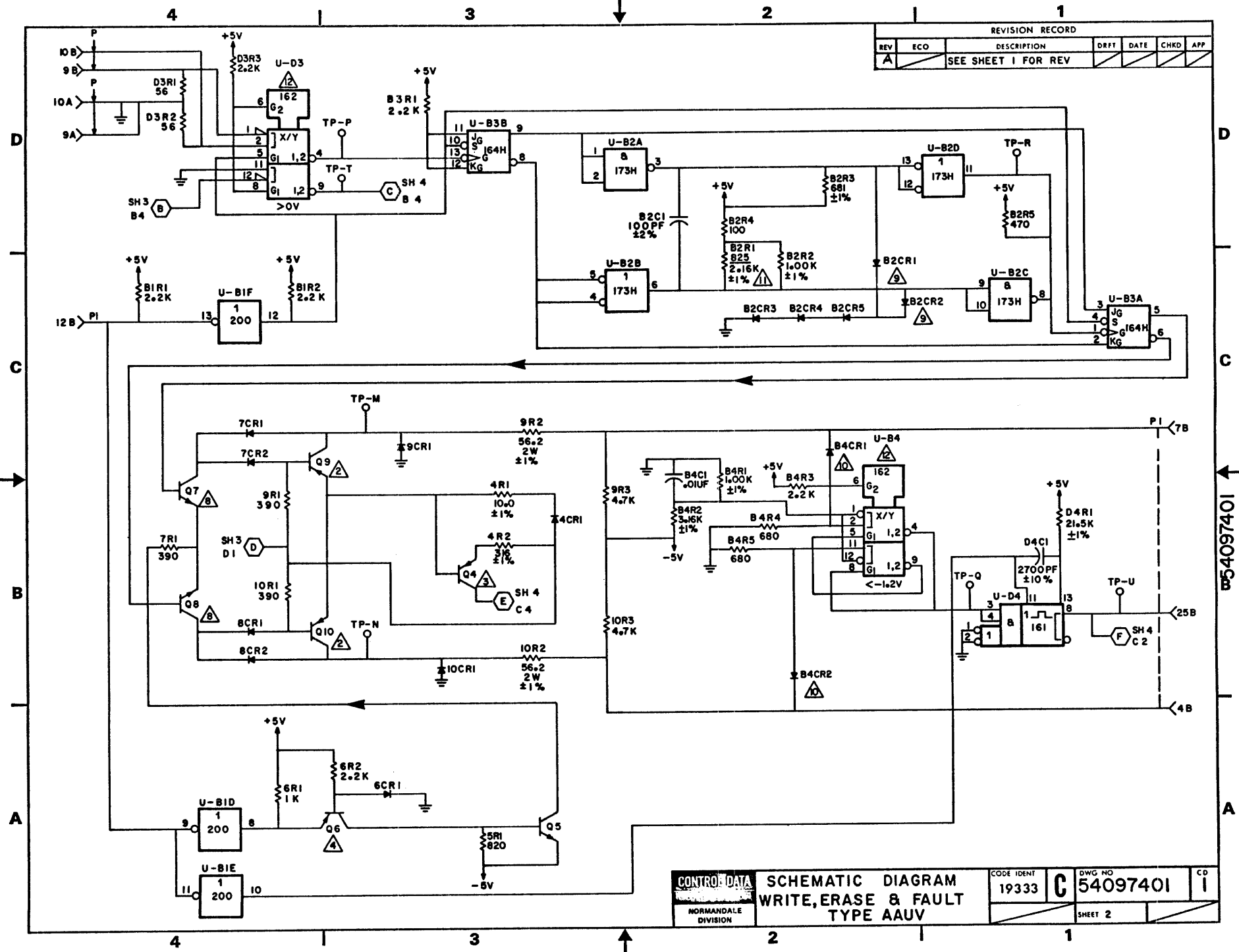
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54097301		FIRST USED ON: BR301				SCHEMATIC DIAGRAM WRITE, ERASE & FAULT TYPE AAUV	
COMPONENTS, EXCEPT AS NOTED		ENGR		DRAWING NUMBER		CD	
TOLERANCE	VALUE	RATING	MTG	19333	C	54097401	I
RES ±5%	OHMS	1/4 W	APPR				
CAP -30%							
						SHEET 1 OF 4	

D
C
B
A

B54097401

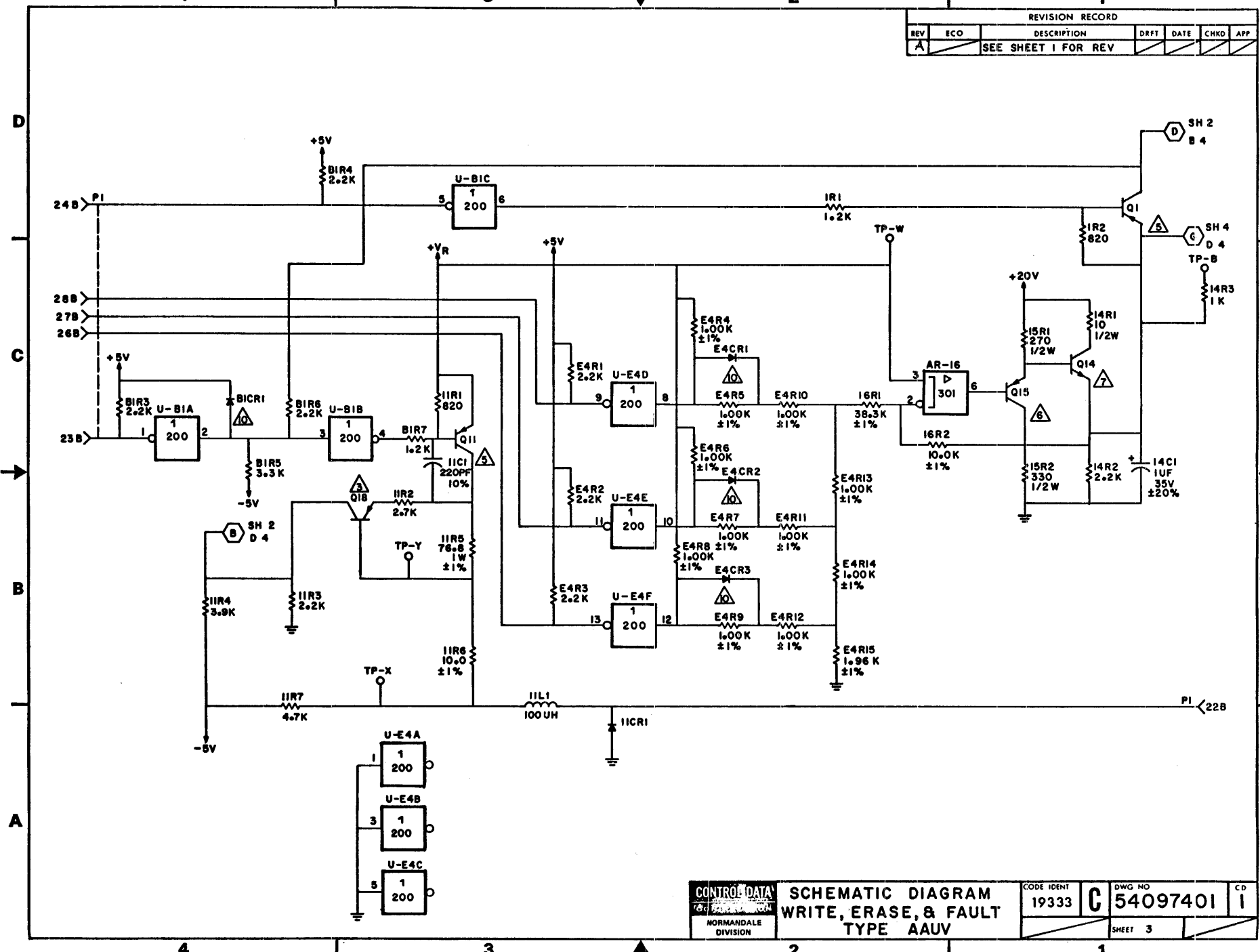
HVD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM WRITE, ERASE & FAULT TYPE AAUV		CODE IDENT 19333	DWG NO C 54097401	CD 1
			SHEET 2		

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

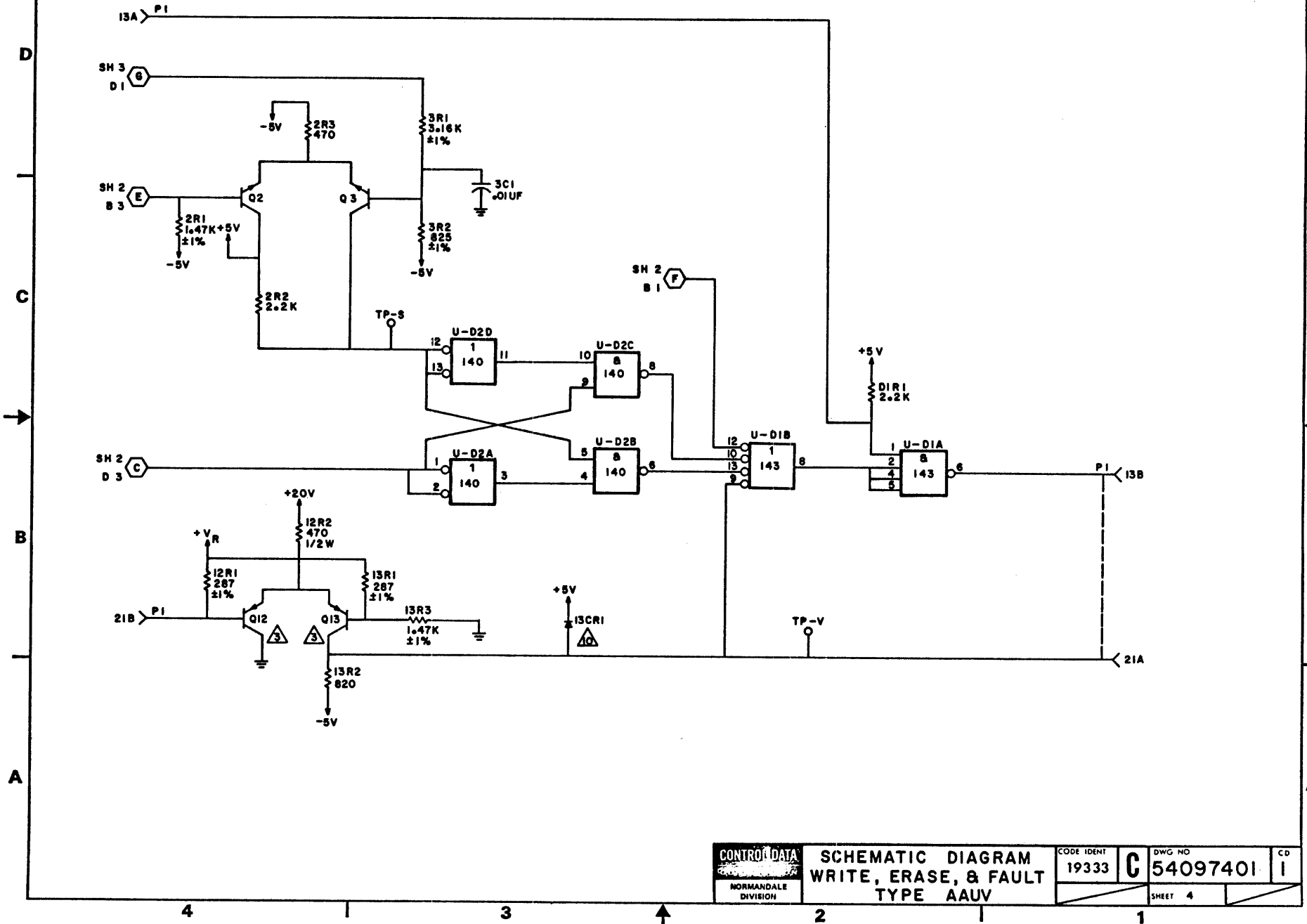


CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE, ERASE, & FAULT TYPE AAUV		CODE IDENT 19333	DWG NO C 54097401	CD 1
				SHEET 3	

4-24

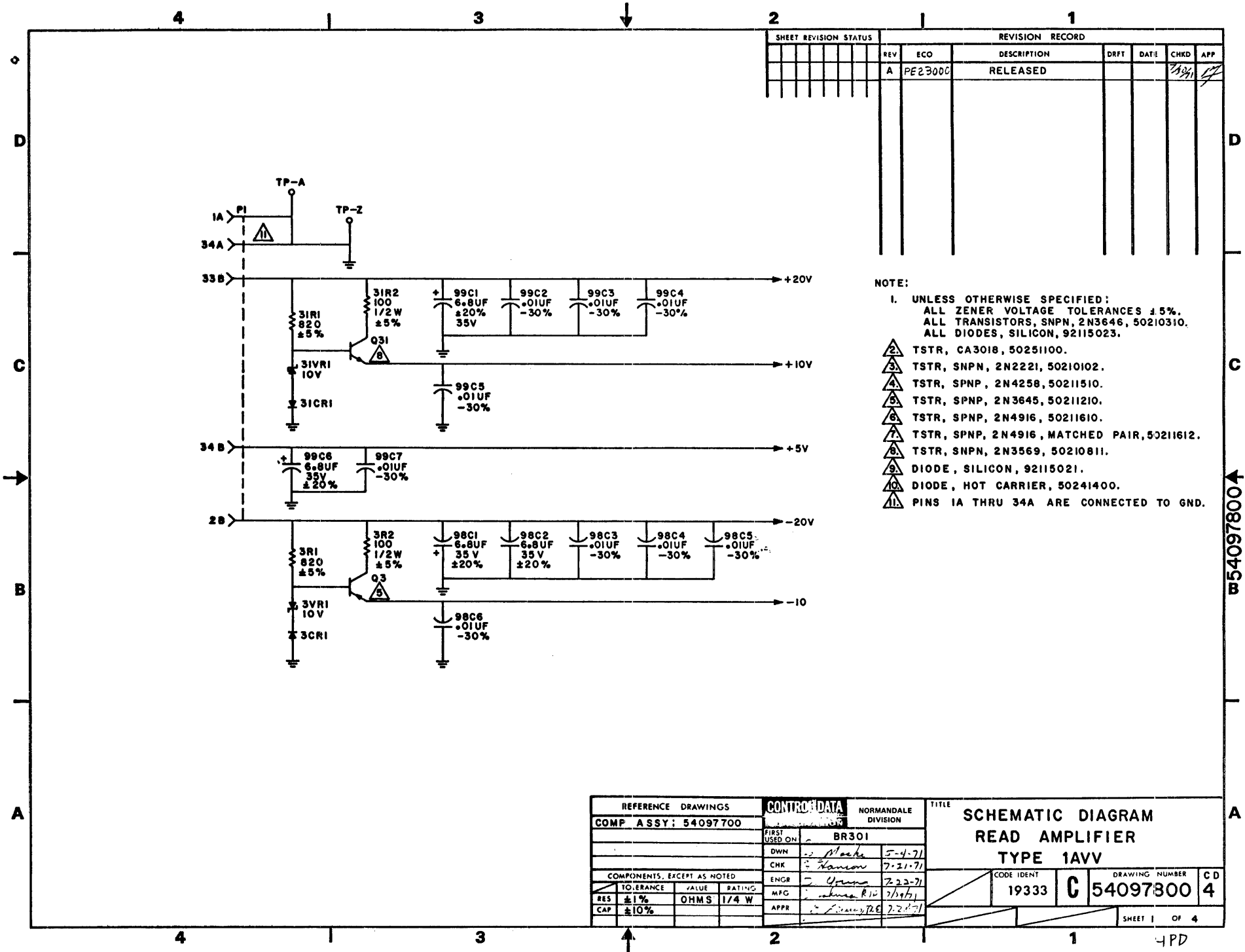
70629100 F

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE, ERASE, & FAULT TYPE AAUV		CODE IDENT 19333	DWG NO C 54097401	CD 1
				SHEET 4	

54097401



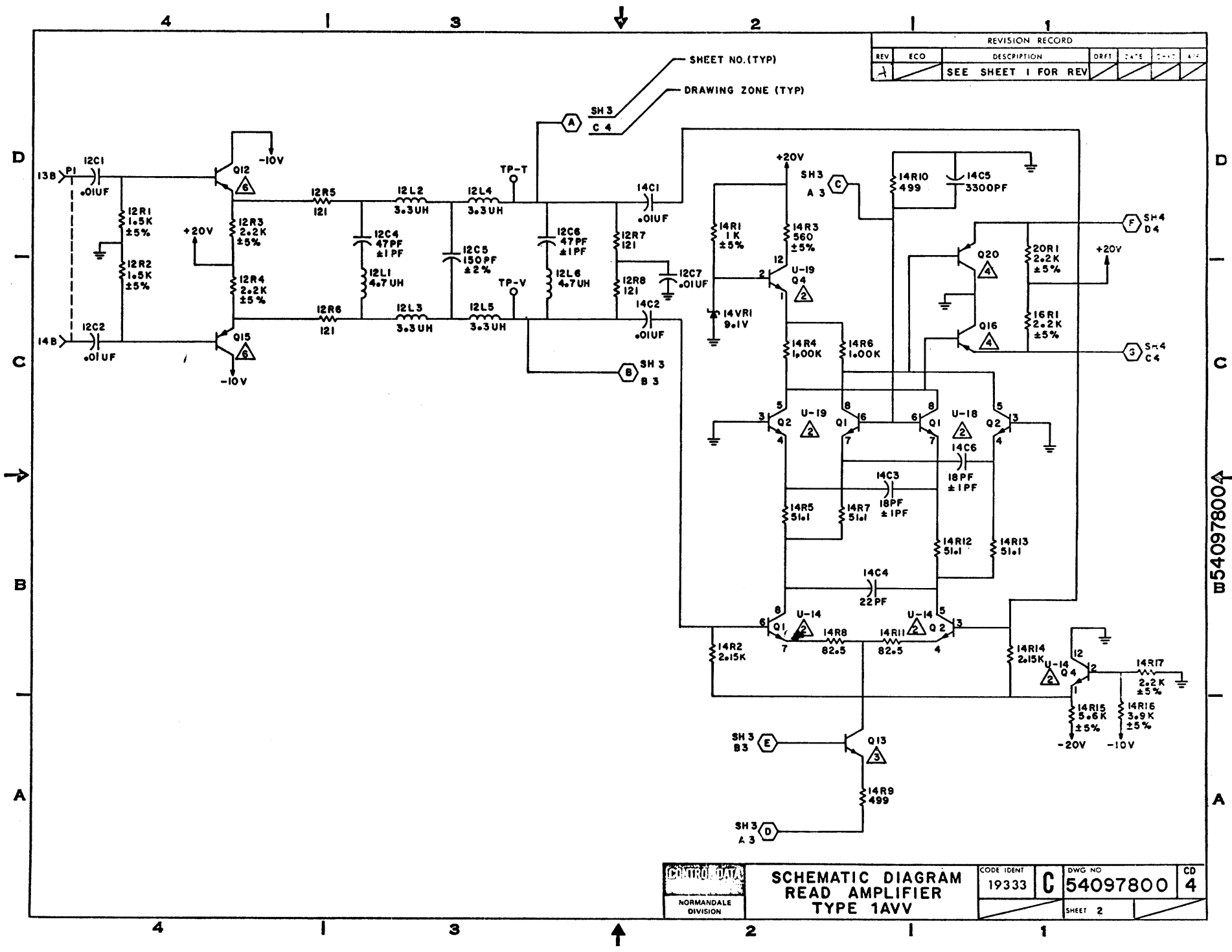
NOTE:

- 1. UNLESS OTHERWISE SPECIFIED:
 ALL ZENER VOLTAGE TOLERANCES ± 5%.
 ALL TRANSISTORS, SNPN, 2N3646, 50210310.
 ALL DIODES, SILICON, 92115023.
- △ TSTR, CA3018, 50251100.
- △ TSTR, SNPN, 2N2221, 50210102.
- △ TSTR, SPNP, 2N4258, 50211510.
- △ TSTR, SPNP, 2N3645, 50211210.
- △ TSTR, SPNP, 2N4916, 50211610.
- △ TSTR, SPNP, 2N4916, MATCHED PAIR, 50211612.
- △ TSTR, SNPN, 2N3569, 50210811.
- △ DIODE, SILICON, 92115021.
- △ DIODE, HOT CARRIER, 50241400.
- △ PINS 1A THRU 34A ARE CONNECTED TO GND.

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54097700		BR301				SCHEMATIC DIAGRAM	
		FIRST USED ON		5-4-71		READ AMPLIFIER	
		DWN		7-21-71		TYPE 1AVV	
		CHK				CODE IDENT	
		ENGR		7-23-71		DRAWING NUMBER	
		MFG		7/19/71		19333 C 54097800 4	
		APPR		7-22-71		C D	
COMPONENTS, EXCEPT AS NOTED				SHEET 1 OF 4			
RES	±1%	OHMS	1/4 W				
CAP	±10%						

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	BY	APP
1		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM READ AMPLIFIER TYPE 1AVV		CODE IDENT 19333	DWG NO C 54097800	CD 4
				SHEET 2	

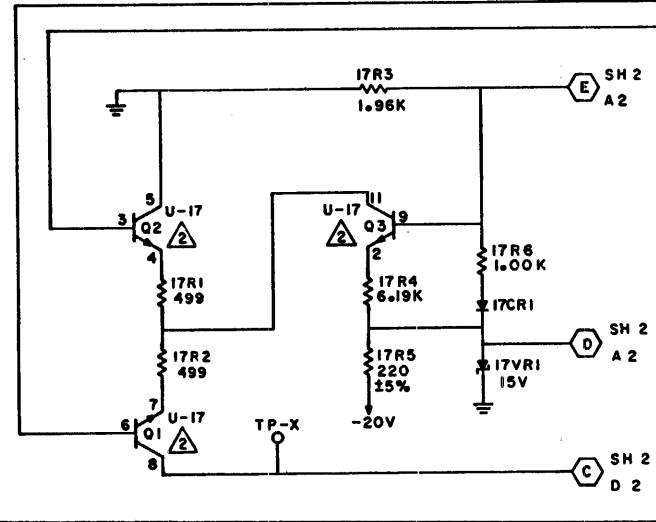
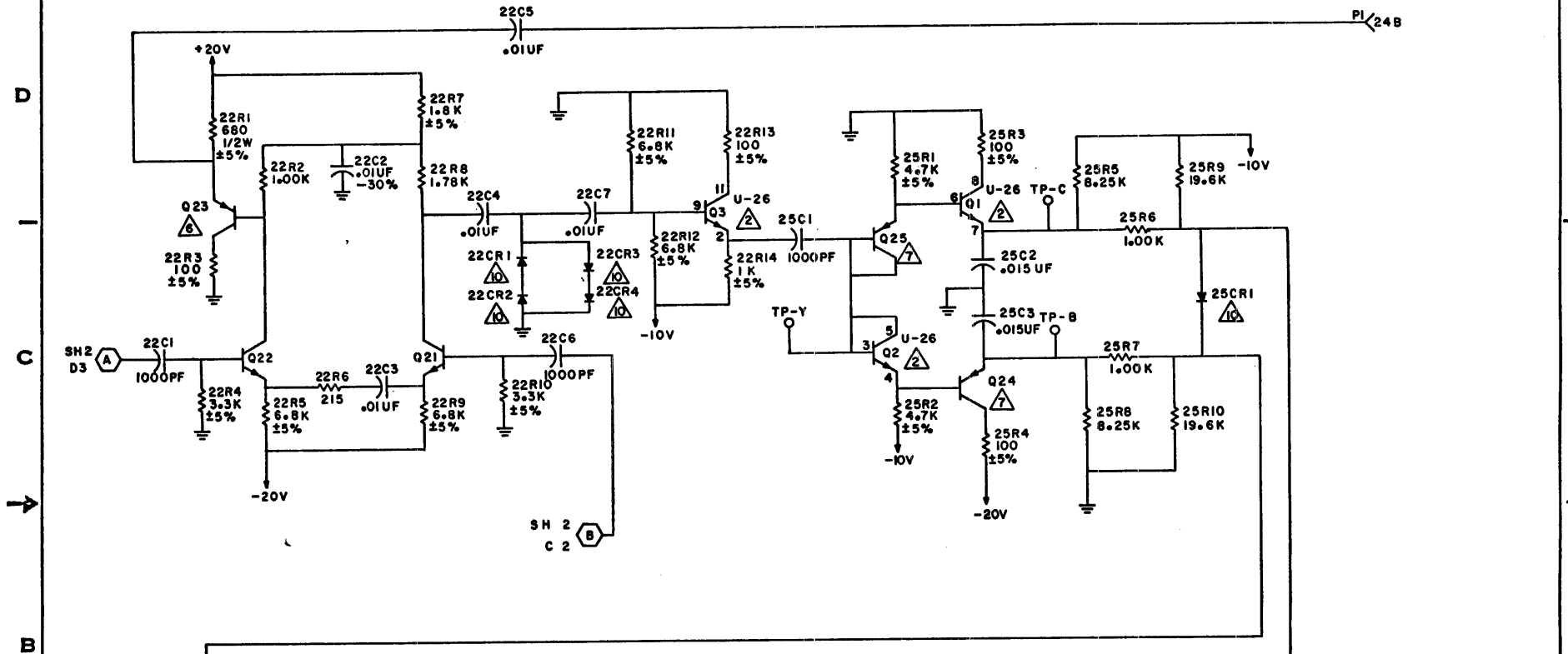
W54097800A

70629100 E

4-27

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

PI 24 B

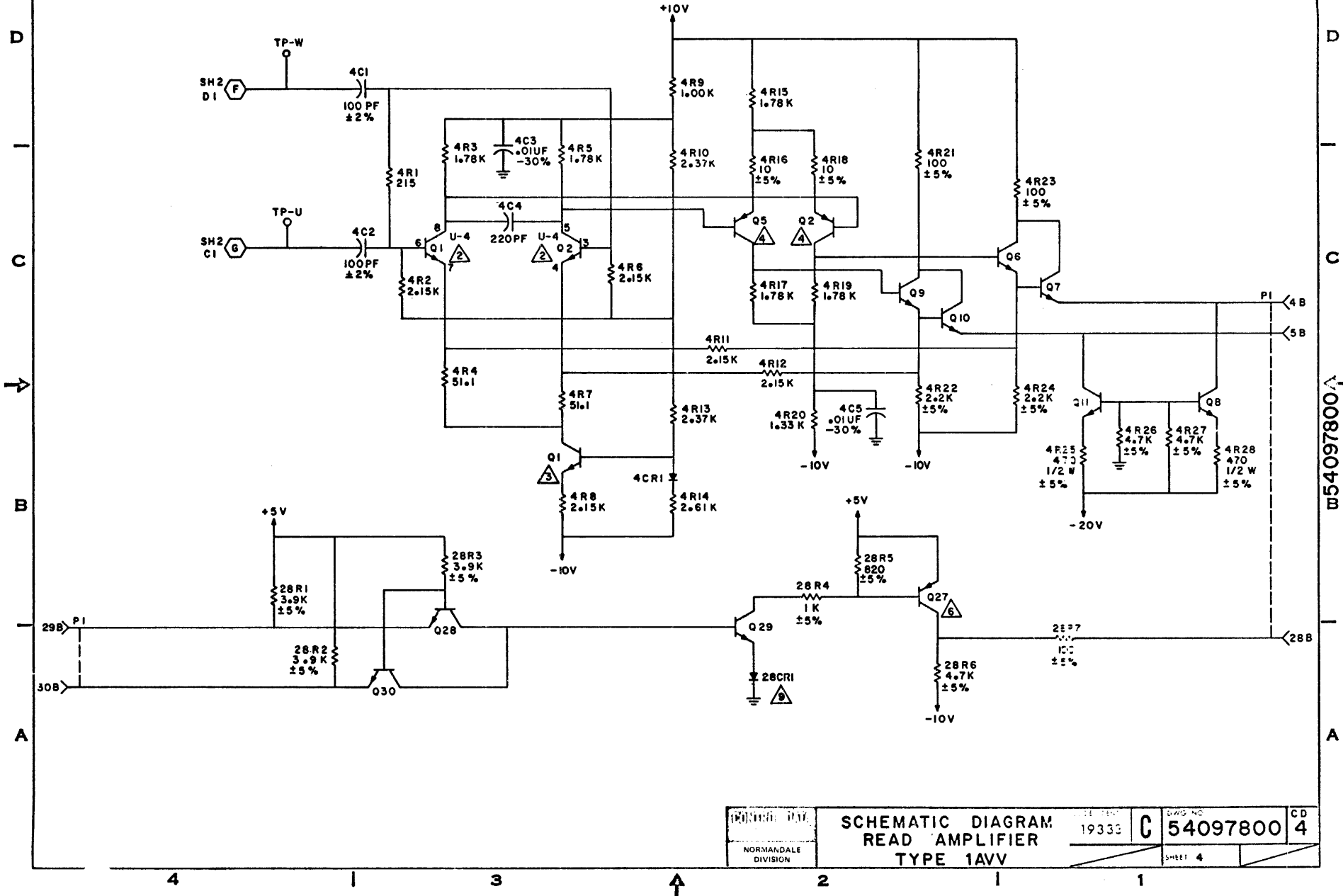


CONTROL DATA NORMAN DALE DIVISION	SCHEMATIC DIAGRAM READ AMPLIFIER TYPE 1AVV		CODE IDENT 19333	DWG NO C 54097800	CD 4
				SHEET 3	

W54097800

REV	ECO	DATE	BY	CHKD	APPD
A					

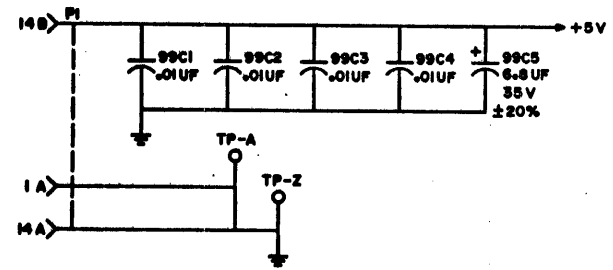
SEE SHEET 1 FOR REV



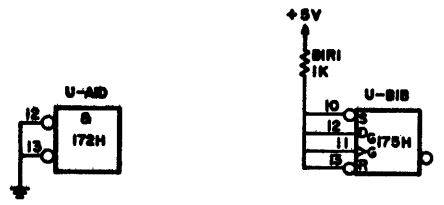
NORMANDE DIVISION	SCHEMATIC DIAGRAM READ AMPLIFIER TYPE 1AVV	REV	ECO	DATE	BY	CHKD	APPD
				19333			
DWS NO. 54097800							CD 4
SHEET 4							

54097800

SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE 23000	RELEASED		0-3-72			



- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 - ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 - DELAY FOR REFERENCE ONLY.

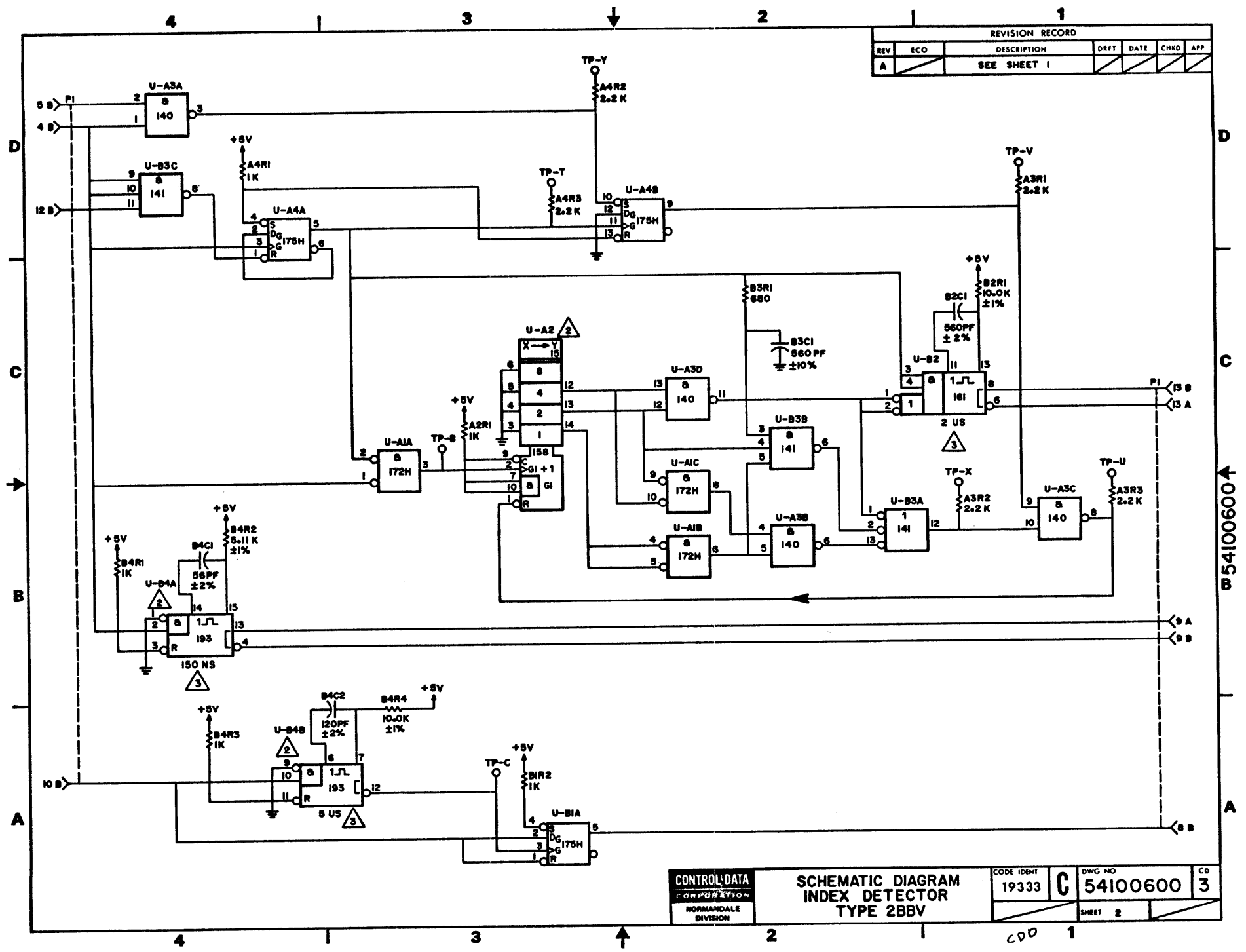


REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54100500		BR3A8B		D. G. TUTTLE 9-5-72		SCHEMATIC DIAGRAM	
COMPONENTS, EXCEPT AS NOTED		ENGR <i>[Signature]</i> 9/19/72		MFG <i>[Signature]</i> 9-26-72		INDEX DETECTOR	
MFG <i>[Signature]</i> 9-26-72		APPR <i>[Signature]</i> 9-26-72		CODE IDENT 19333 C		DRAWING NUMBER 54100600	
TOLERANCE VALUE RATING		RES ±5% OHMS 1/4W		CAP -30%		C.D. 3	
						SHEET 1 OF 2	

B 54100600

DD 1

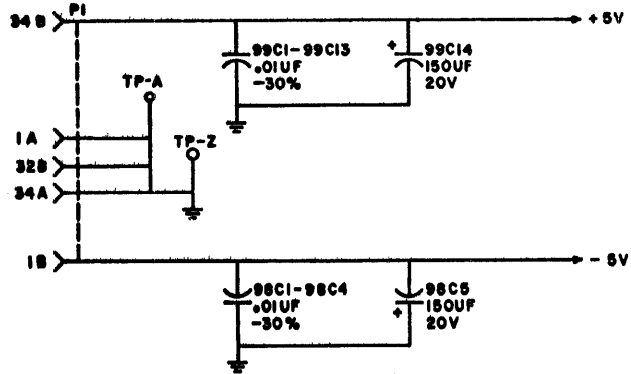
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA CORPORATION NORMANVILLE DIVISION	SCHEMATIC DIAGRAM INDEX DETECTOR TYPE 2BBV			CODE IDENT 19333	DWG NO 54100600	CD 3
				SHEET 2		

54100600

D
C
B
A



SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRAFT	DATE	CHKD	APP			
A	PE 23000	RELEASED							

NOTE:

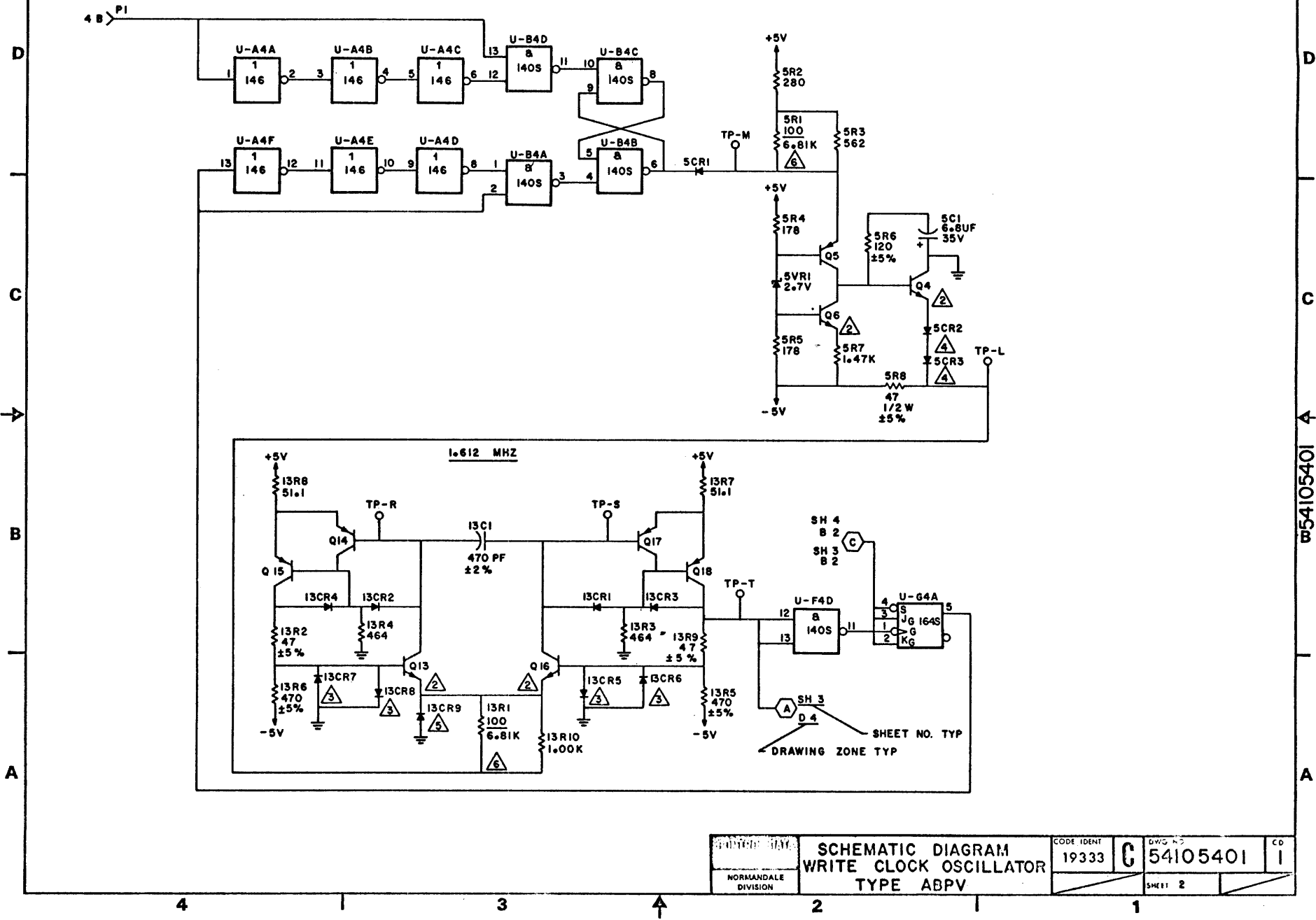
- I. UNLESS OTHERWISE SPECIFIED:
 - ALL TRANSISTORS, SPNP, 2N4258, 50211510.
 - ALL DIODES, SCHOTTKY BARRIER, 50241400.
 - ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$
 - ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
- ⚠ TRANSISTOR, SNPN, 2N3646, 50210310.
- ⚠ DIODE, SILICON, 92115021.
- ⚠ DIODE, SILICON, 92115023.
- ⚠ DIODE, GERMANIUM, 11801200.
- ⚠ TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
- ⚠ DELAY TIME TO BE SELECTED IN PRODUCTION PER RECOMMENDED TEST PROCEDURE.

W54105401

REFERENCE DRAWINGS			CONTROL DATA		NORMANDEALE DIVISION		TITLE		
COMP ASSY: 54105301			FIRST USED ON		BR3A3		SCHEMATIC DIAGRAM		
			DWN		RKR		11-27-72		DRAWING NUMBER
			CHK				12-13-72		C D
COMPONENTS, EXCEPT AS NOTED			ENGR				CODE IDENT		DRAWING NUMBER
			MFG				19333		54105401
			APPR						1
RES	3-1%	OHMS	1/4 W						
CAP	±20%								
									SHEET 1 OF 4

HPE

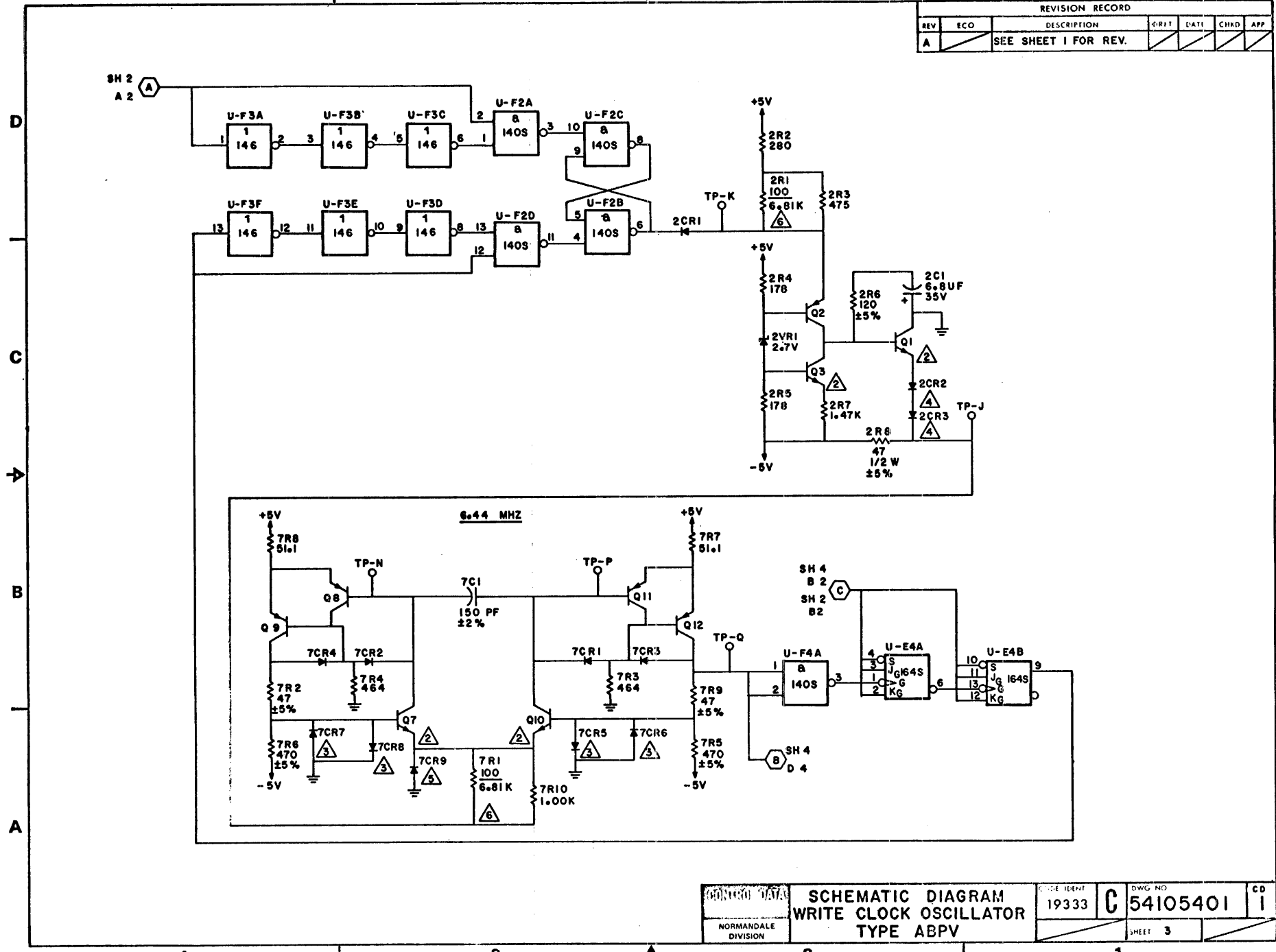
REVISION RECORD						
REV	ECO	DESCRIPTION	CHGT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV.				



NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV		CODE IDENT 19333	DWG NO 54105401	CO 1
			SHEET 2		

54105401

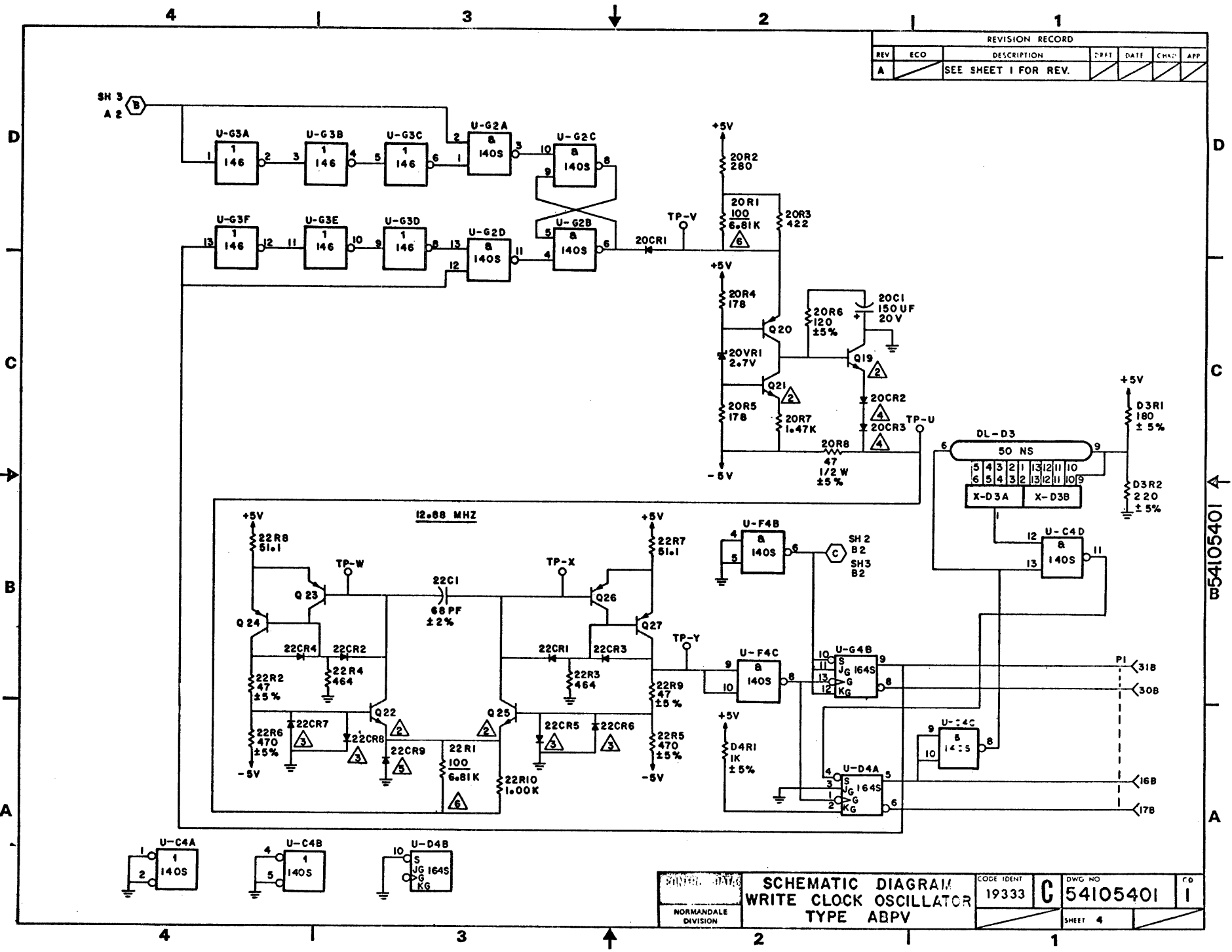
REVISION RECORD						
REV	ECO	DESCRIPTION	CRIT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV.				



NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV		DATE IDENT 19333	DWG NO C 54105401	CD 1
			SHEET 3		

W54105401

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV.				



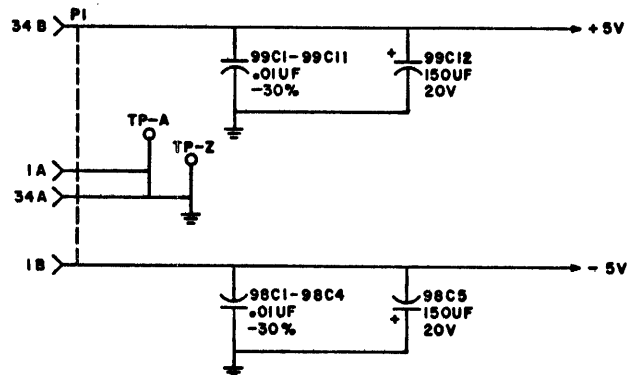
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE ABPV		CODE IDENT 19333	DWG NO 54105401	CD 1
			SHEET 4		

54105401

70629100 E

4-35

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23000	RELEASED		5-7-72		PR	



NOTE :

- UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SPNP, 2N4258, 50211510.
 ALL DIODES, SCHOTTKY BARRIER, 50241400.
 ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$.
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
- TRANSISTOR, SPNP, 2N3646, 50210310.
- DIODE, SILICON, 92115021.
- DIODE, SILICON, 92115023.
- DIODE, GERMANIUM, 11801200.
- COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.

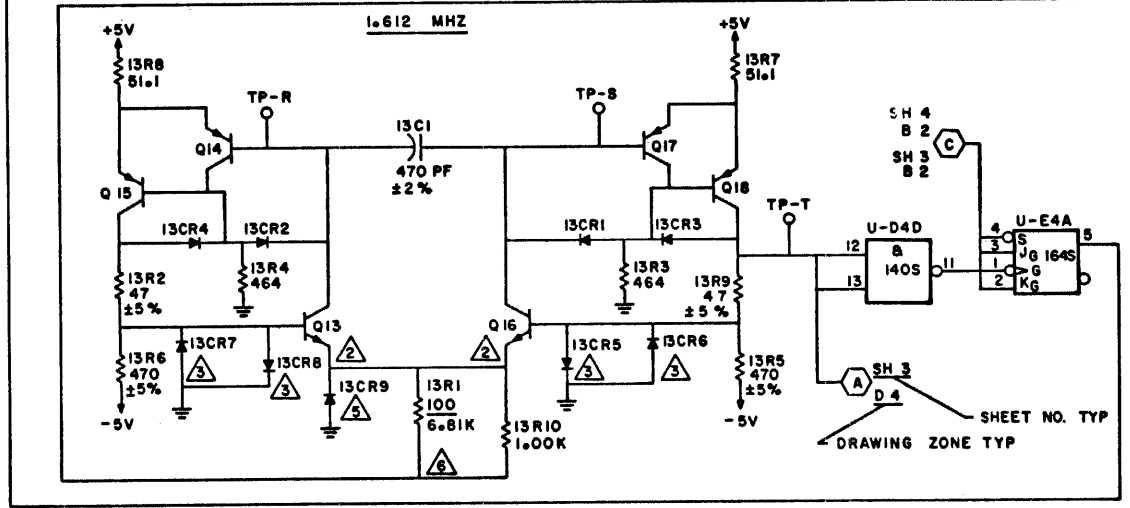
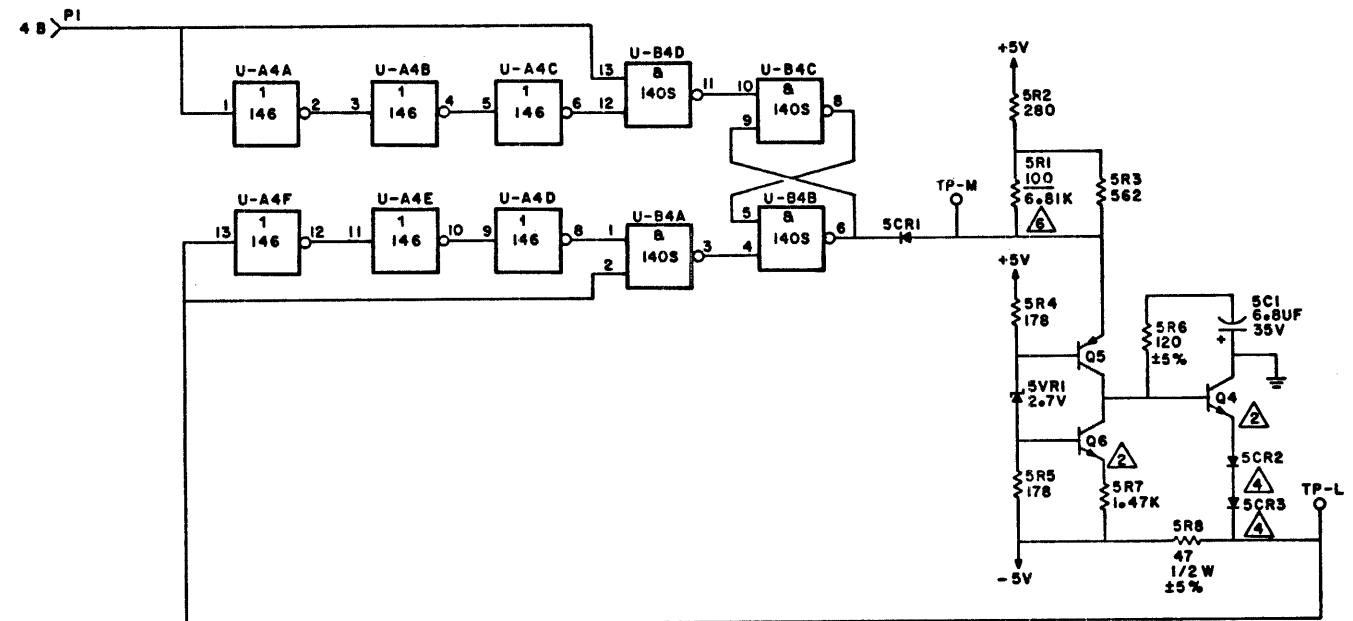
REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE			
COMP ASSY : 54105300			BR3A3				SCHEMATIC DIAGRAM			
			DWN				WRITE CLOCK OSCILLATOR			
			CHK				TYPE 2BPV			
COMPONENTS EXCEPT AS NOTED			ENER				CODI IDEN#		DRAWING NUMBER	CD
TOL	TOLERANCE	VALU	RATING	MFG			19333	G	54105400	3
RES	$\pm 1\%$	OHMS	1/4 W	APPR						
CAP	$\pm 20\%$									
							SHEET 1 OF 4		HPD	

54105400

4-36

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV.				



NORMANDE DIVISION	SCHEMATIC DIAGRAM WRITE CLOCK OSCILLATOR TYPE 2BPV		CDR# IDENT 19333	DWG NO C 54105400	CD 3
				SHEET 2	

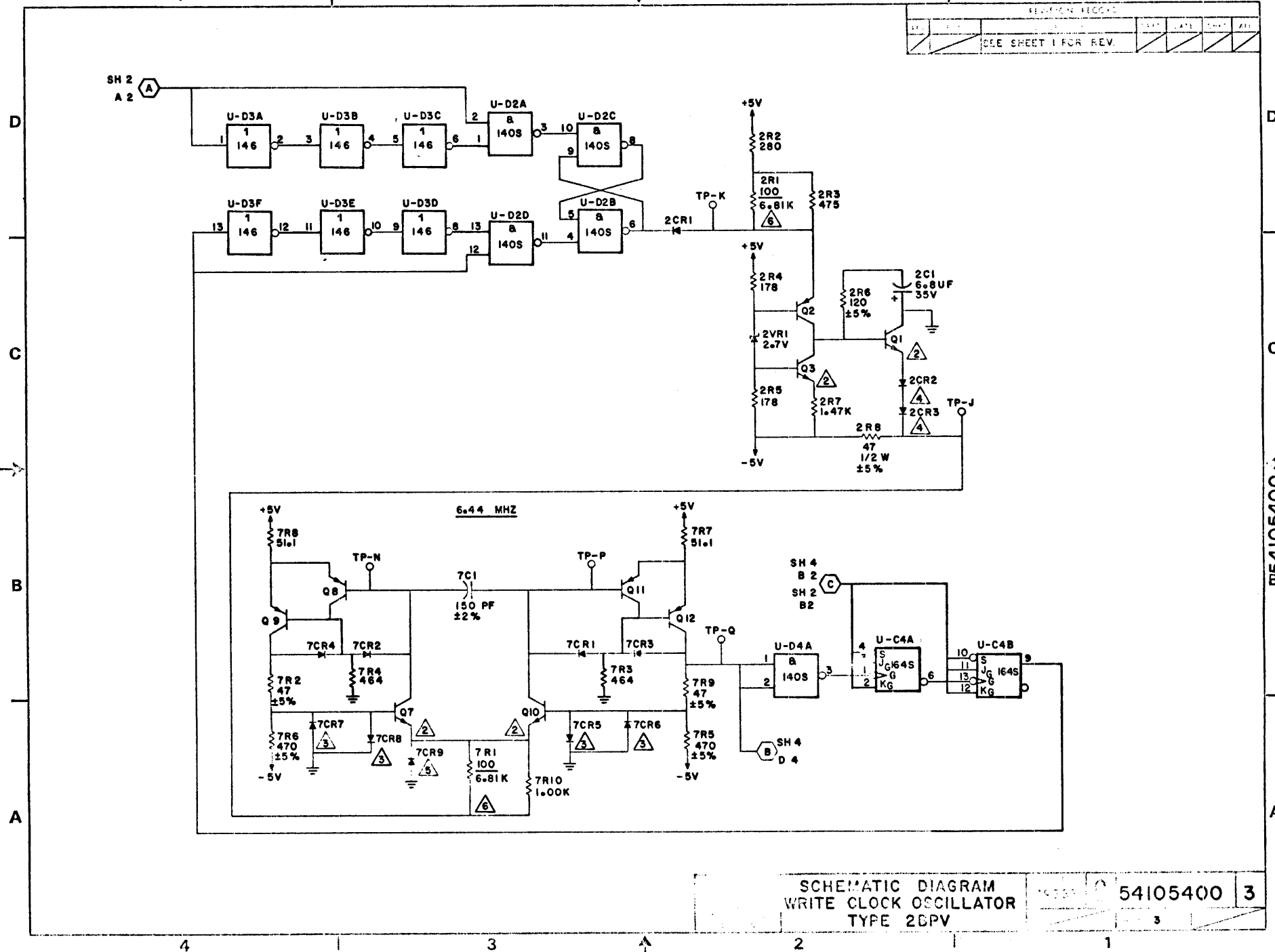
54105400

70629100 E

4-37

REVISION RECORD			
REV.	DATE	BY	APP.
1			

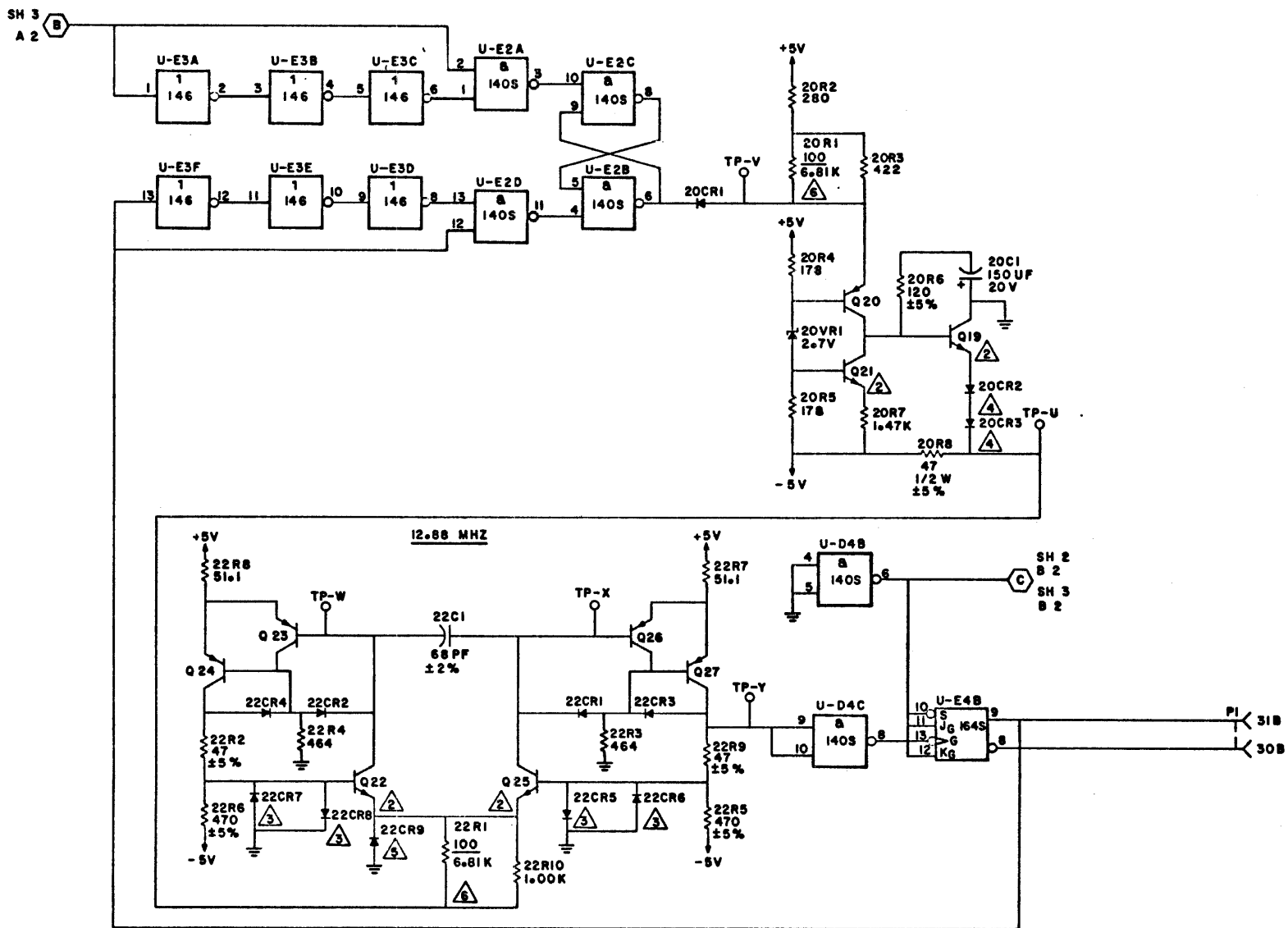
SEE SHEET 1 FOR REV.



SCHEMATIC DIAGRAM
WRITE CLOCK OSCILLATOR
TYPE 2BPV

54105400 3

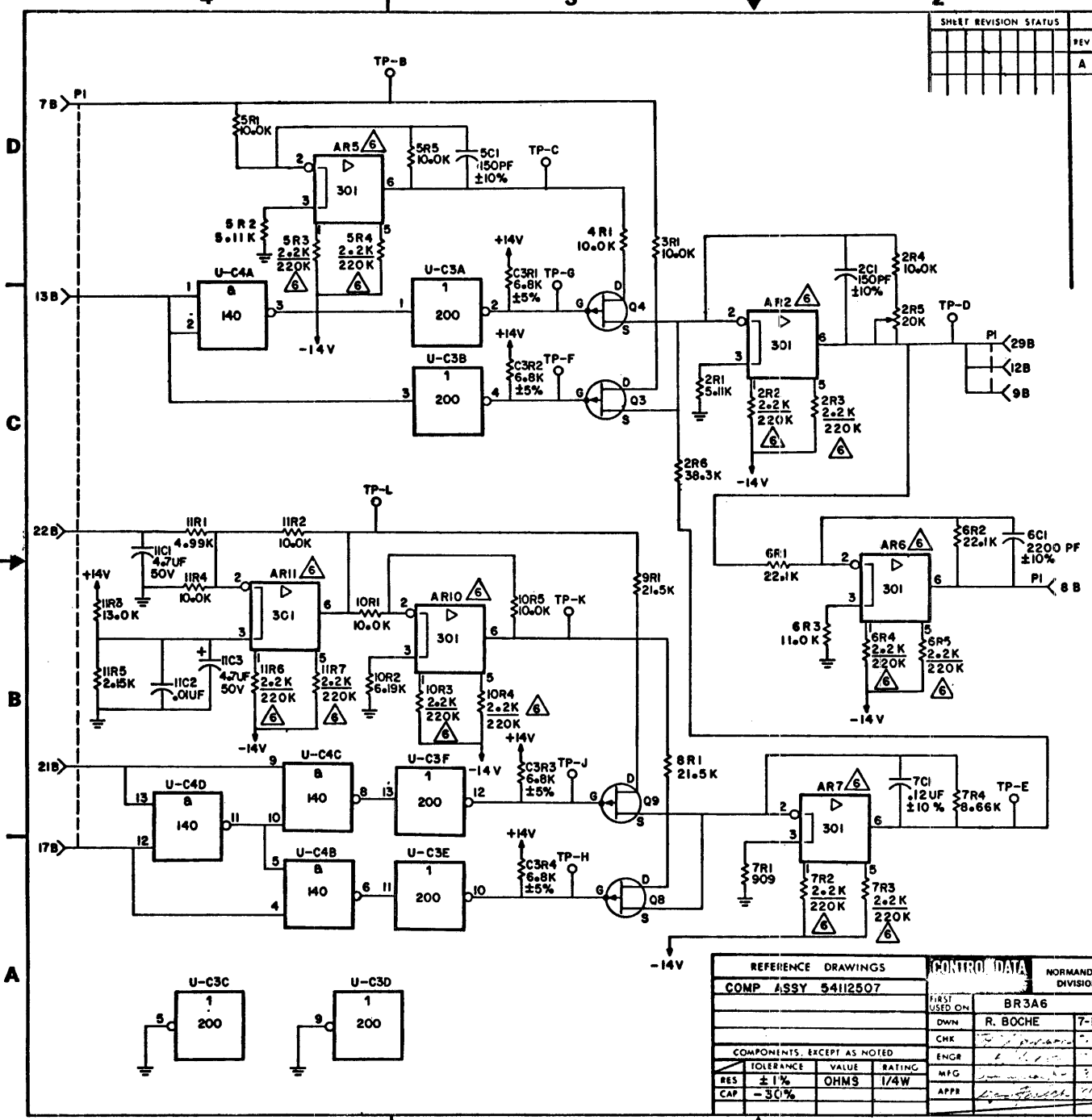
REVISION RECORD					
REV.	ECO	DESCRIPTION	DATE	CHKD	APP
1		SEE SHEET 1 FOR REV.			



SCHEMATIC DIAGRAM		REV. NO.	DATE	CHKD	APP
WRITE CLOCK OSSILLATOR		19333			
TYPE 2BPV					
54105400			3		

54105400

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE 23000	RELEASED					12/72

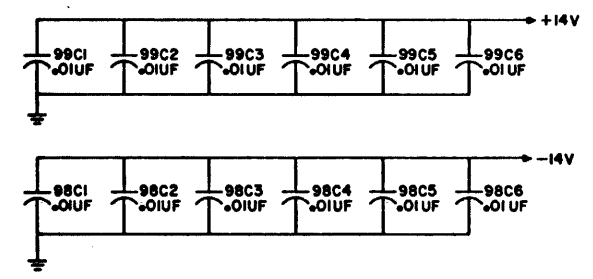
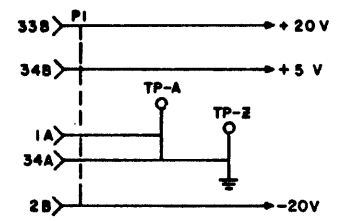
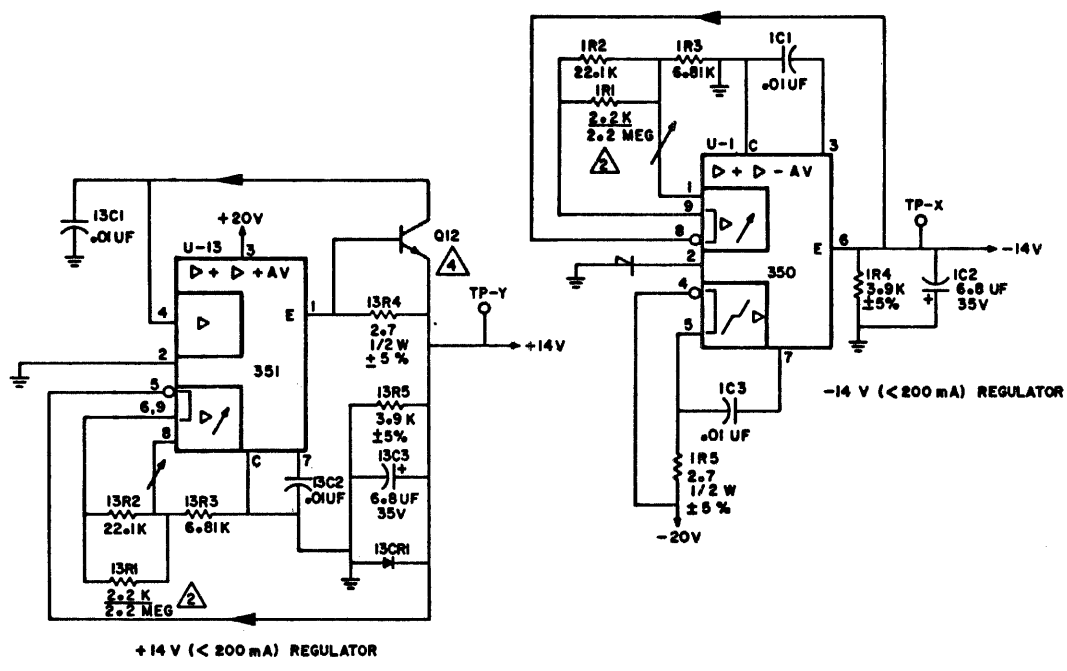


- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, FET'S 50218200
ALL DIODES, GERMANIUM, 11801200
 - SEE 46325900 FOR SELECTION OF IR1 AND I3R1.
 - TRANSISTOR, SNPN, 2N3646, 50210310.
 - IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
 - MATCHED COMPONENTS. SEE 70740800.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54112507		FIRST USED ON		BR3A6		SCHEMATIC DIAGRAM	
		DWN		R. BOCHE		7-12-72	
		CHK					
		ENGR					
		MFG					
		APPR					
COMPONENTS, EXCEPT AS NOTED				CODE IDENT		DRAWING NUMBER	
RES	± 1%	VALUE	OHMS	19333	C	54112607	CD
CAP	-30%	RATING	1/4W				4

54112607

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

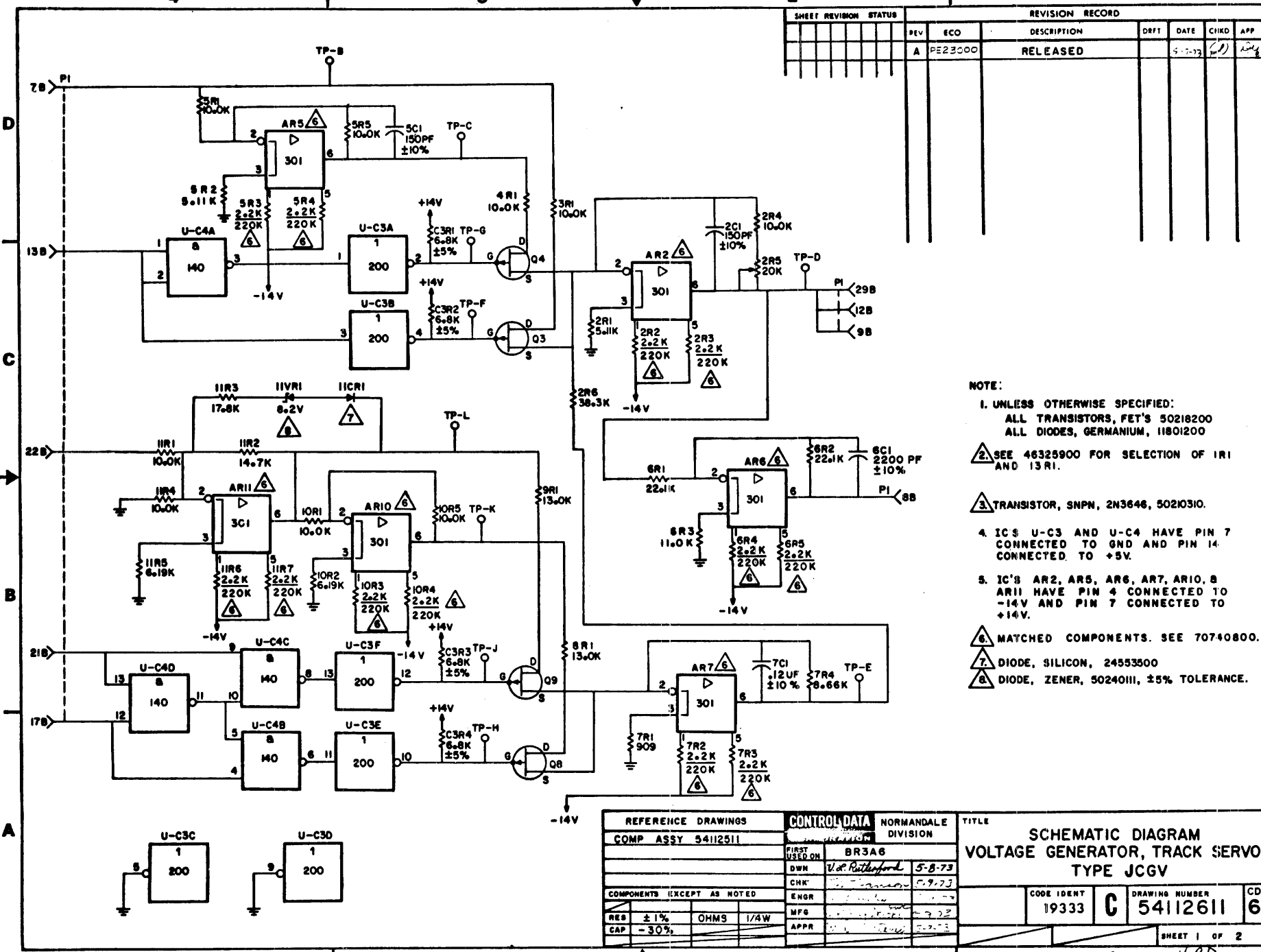


CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM VOLTAGE GENERATOR, TRACK SERVO TYPE ECGV		CODE IDENT 19333	C	DWG NO 54112607	CD 4
			SHEET 2			

70629100 E

4-41

SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED		5-1-73			

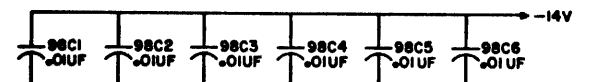
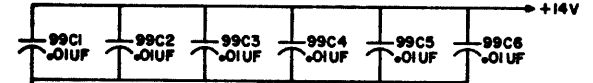
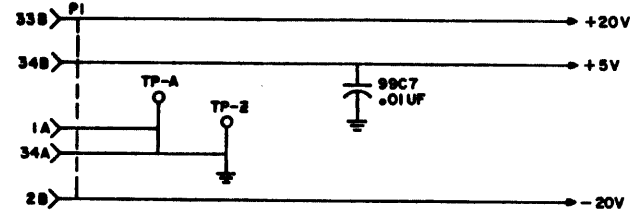
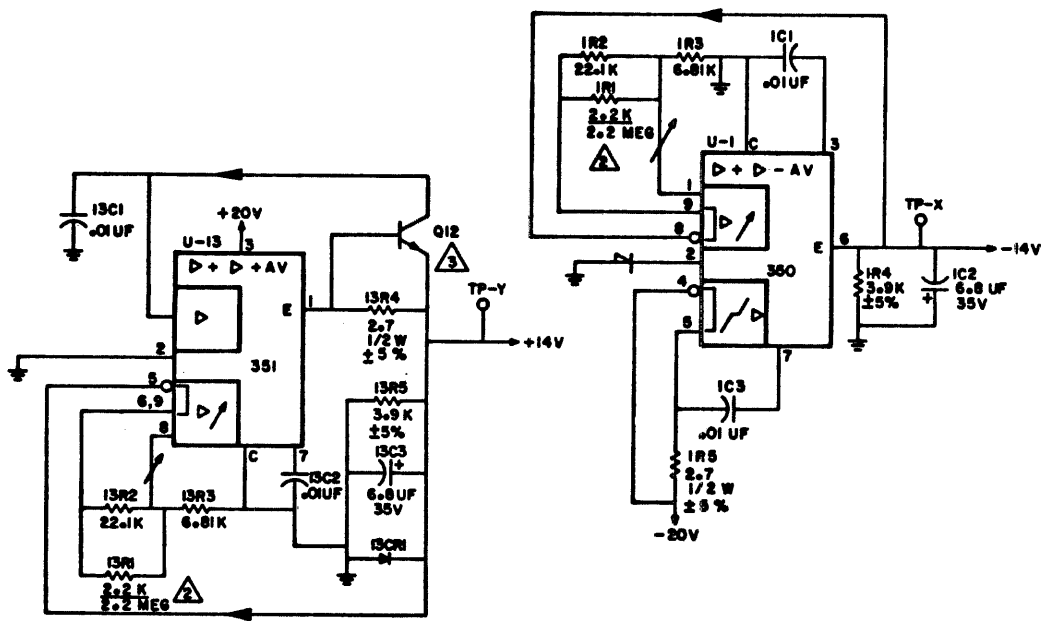


- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, FET'S 50218200
ALL DIODES, GERMANIUM, 11801200
 - SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.
 - TRANSISTOR, SNPN, 2N3646, 50210310.
 - IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - IC'S AR2, AR5, AR6, AR7, AR10, 8 AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
 - MATCHED COMPONENTS. SEE 70740800.
 - DIODE, SILICON, 24553500
 - DIODE, ZENER, 50240111, ±5% TOLERANCE.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54112511		FIRST USED ON BR3A6		DIVISION		SCHEMATIC DIAGRAM	
		DWN <i>U.S. Rutherford</i>		5-8-73		VOLTAGE GENERATOR, TRACK SERVO	
		CHK		5-9-73		TYPE JGV	
COMPONENTS (EXCEPT AS NOTED)		ENGR				CODE IDENT	
RES ± 1%		OHMS		1/4W		19333	
CAP - 30%						DRAWING NUMBER	
		MFG		5-7-73		54112611	
		APPR		5-7-73		CD	
						6	
						SHEET 1 OF 2	

HPD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

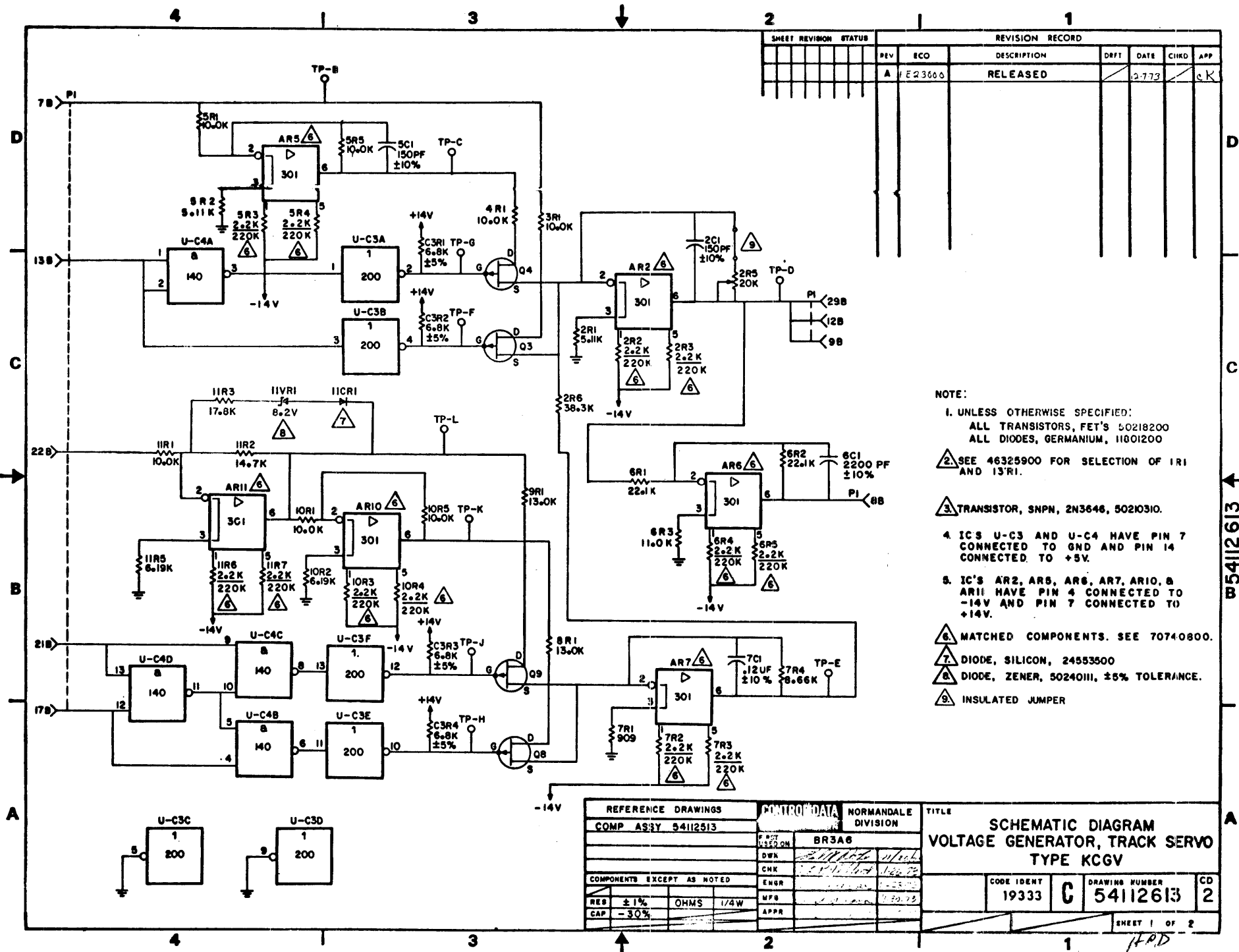


1192115CM

CONTROL DATA
NORMANDALE
DIVISION

**SCHEMATIC DIAGRAM
VOLTAGE GENERATOR,
TRACK SERVO
TYPE JCGV**

CODE IDENT 19333	DWG NO C 54112611	CD 6
SHEET 2		



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	E23600	RELEASED		2-7-73		CK

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, FET'S 50218200
ALL DIODES, GERMANIUM, 11801200
 - SEE 46325900 FOR SELECTION OF 1R1 AND 13R1.
 - TRANSISTOR, SNPN, 2N3646, 50210310.
 - IC'S U-C3 AND U-C4 HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - IC'S AR2, AR5, AR6, AR7, AR10, & AR11 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
 - MATCHED COMPONENTS. SEE 70740800.
 - DIODE, SILICON, 24553500
 - DIODE, ZENER, 50240111, ±5% TOLERANCE.
 - INSULATED JUMPER

REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY 54112513	BR3A6		SCHMATIC DIAGRAM VOLTAGE GENERATOR, TRACK SERVO TYPE KCGV
COMPONENTS EXCEPT AS NOTED	ENGR	MFR	CD
RES ± 1%	OHMS 1/4W	APPR	19333
CAP -30%			C 54112613
			DRAWING NUMBER
			CD 2
			SHEET 1 OF 2

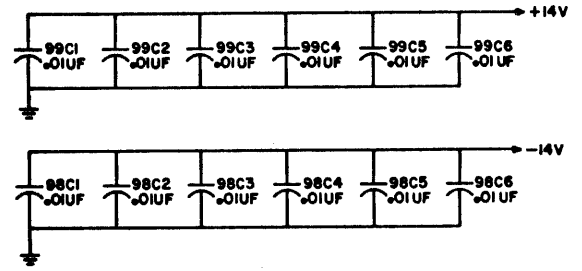
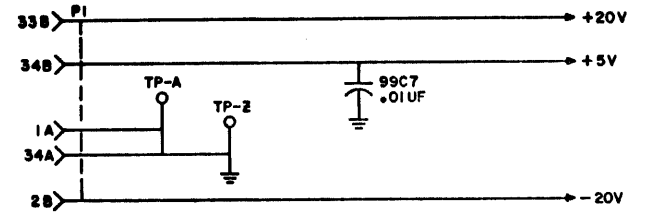
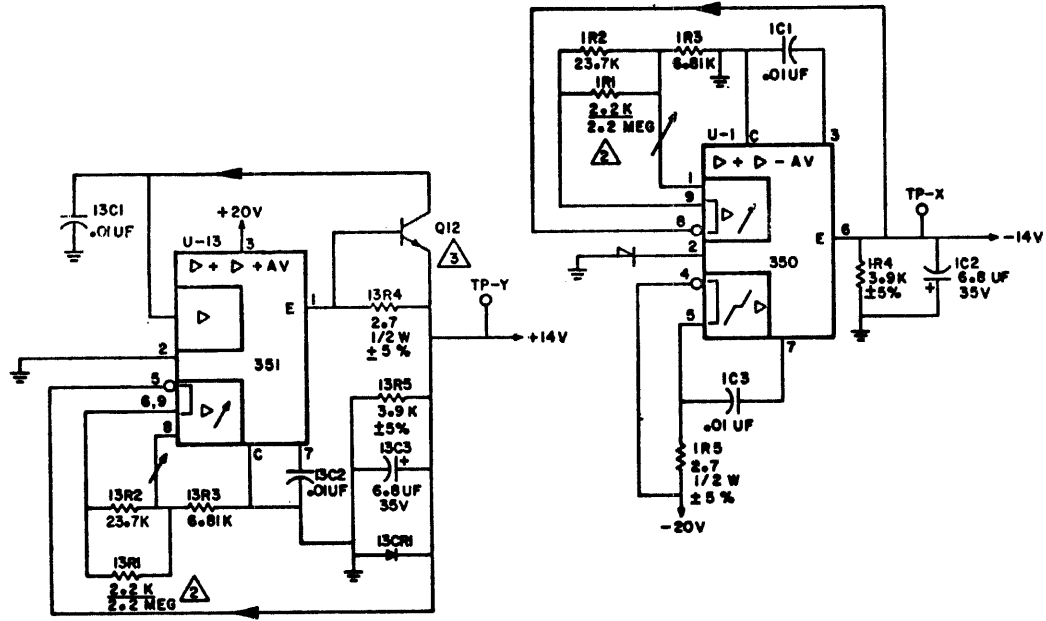
W54112613

HPD

4-42.2

70629100 F

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHNG	APP
A		SEE SHT 1 FOR REV				

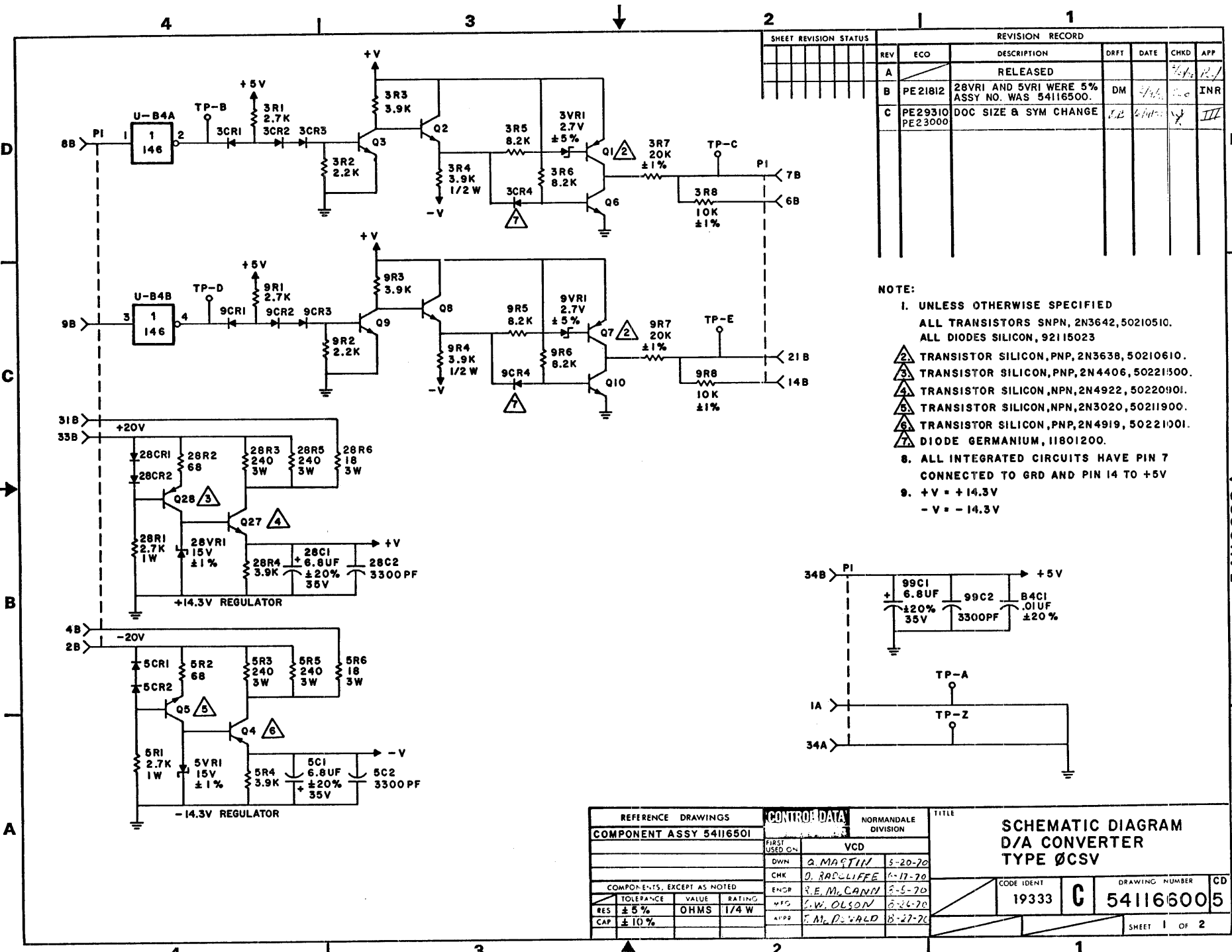


CONTROL DATA
NORMANDALE
DIVISION

**SCHEMATIC DIAGRAM
VOLTAGE GENERATOR,
TRACK SERVO
TYPE KCGV**

CODE IDENT 19333	CD C	DWG NO 54112613	CD 2
SHEET 2			

54112613



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					
B	PE21812	28V1 AND 5V1 WERE 5% ASSY NO. WAS 54116500.	DM	7/4/70		INR	
C	PE29310 PE23000	DOC SIZE & SYM CHANGE	JLB	6/10/70		III	

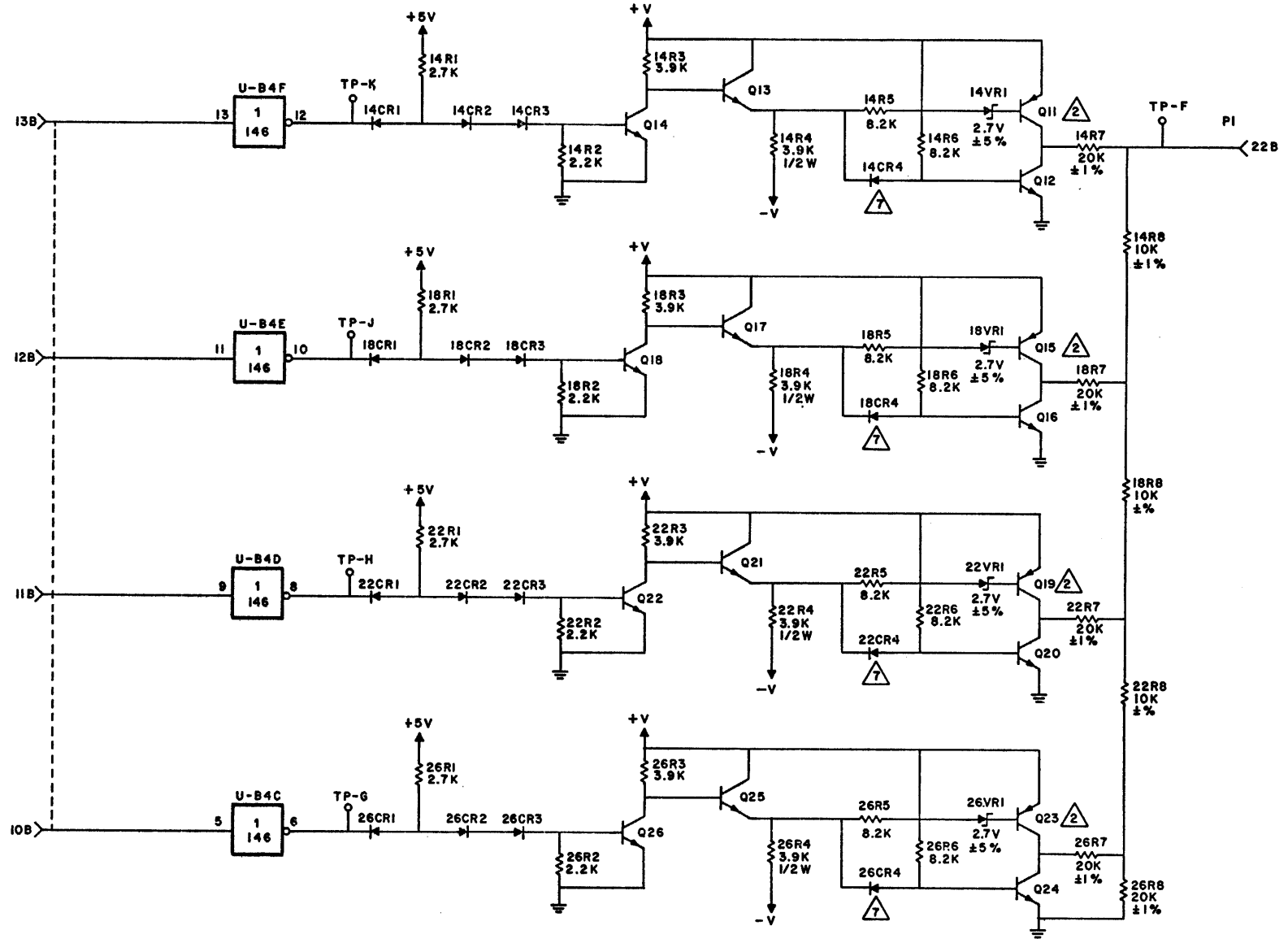
NOTE:
 1. UNLESS OTHERWISE SPECIFIED
 ALL TRANSISTORS SNPN, 2N3642, 50210510.
 ALL DIODES SILICON, 92115023
 1. TRANSISTOR SILICON, PNP, 2N3638, 50210610.
 2. TRANSISTOR SILICON, PNP, 2N4406, 50221500.
 3. TRANSISTOR SILICON, NPN, 2N4922, 50220401.
 4. TRANSISTOR SILICON, NPN, 2N3020, 50211900.
 5. TRANSISTOR SILICON, PNP, 2N4919, 50221001.
 6. DIODE GERMANIUM, 11801200.
 8. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GRD AND PIN 14 TO +5V
 9. +V = +14.3V
 -V = -14.3V

REFERENCE DRAWINGS	CONTROL DATA	NORMANDEALE DIVISION	TITLE
COMPONENT ASSY 54116501			SCHMATIC DIAGRAM D/A CONVERTER TYPE ØCSV
FIRST USED ON:	VCD		
DWN	A. MARTIN	5-20-70	
CHK	D. RASCHLIEFF	6-17-70	
ENGR	R. E. Mc CANIN	7-5-70	
WFO	L. W. OLSON	8-26-70	
APPD	F. M. DE WARD	8-27-70	
COMPONENTS, EXCEPT AS NOTED		CODE IDENT	DRAWING NUMBER
TOLERANCE	VALUE	RATING	
RES ± 5%	OHMS	1/4 W	
CAP ± 10%			
		19333	541166005
		SHEET 1 OF 2	

54116600

A

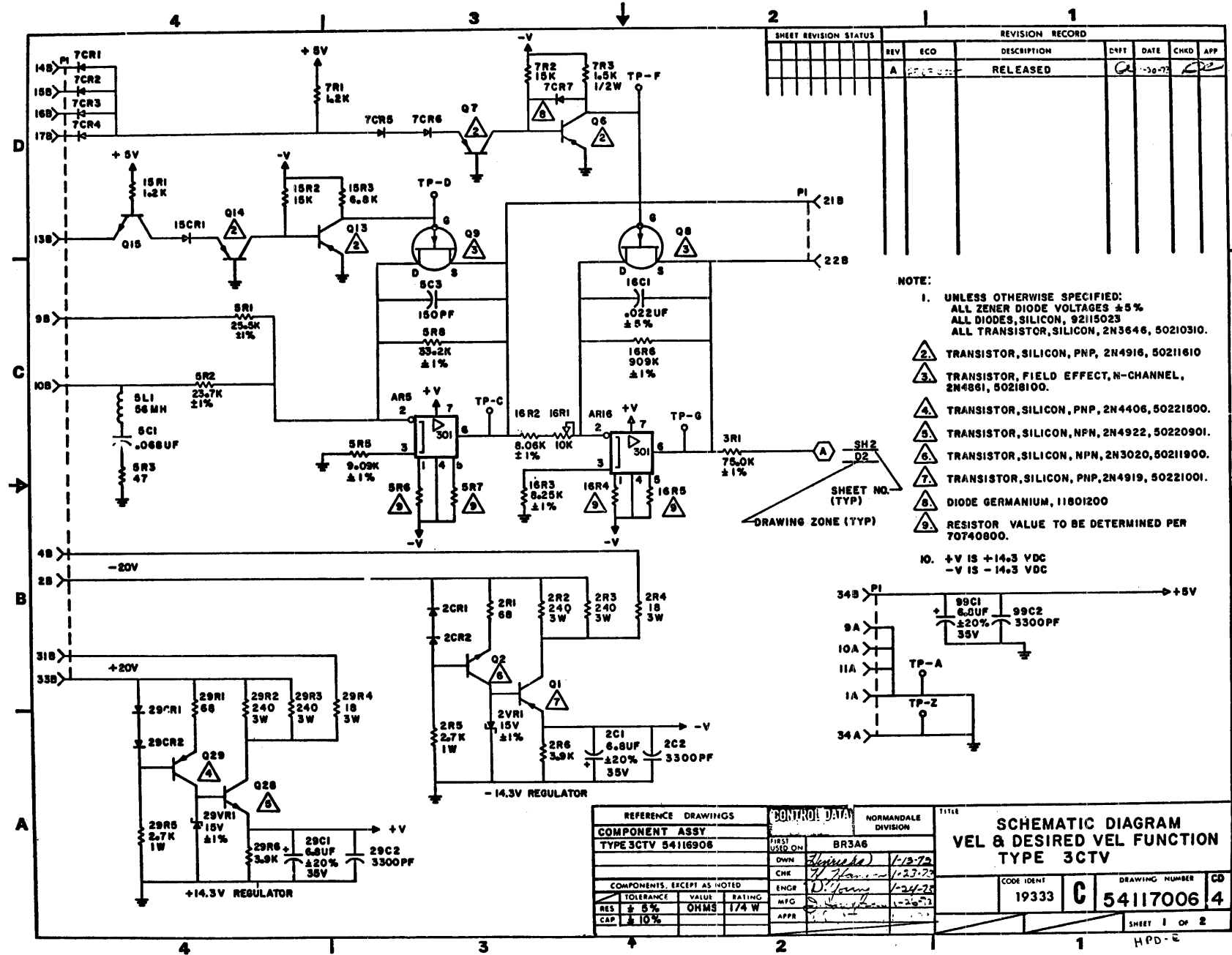
REVISION RECORD					
REV	ECO	DESCRIPTION	DATE	CHKD	APPD
1		SEE SHEET I FOR REV			



**SCHEMATIC DIAGRAM
D/A CONVERTER
TYPE ØCSV**

10000	54116600	CD 5
2		

54116600



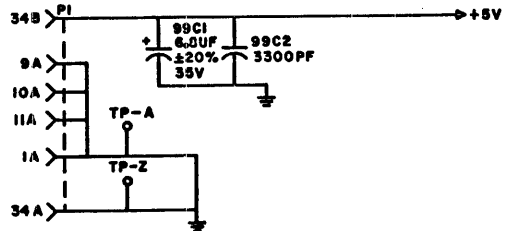
SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	ENFT	DATE	CHKD	APP	
A		RELEASED		1-30-73			

NOTE:

- UNLESS OTHERWISE SPECIFIED:
ALL ZENER DIODE VOLTAGES $\pm 5\%$
ALL DIODES, SILICON, 92115023
ALL TRANSISTOR, SILICON, 2N3646, 50210310.
- TRANSISTOR, SILICON, PNP, 2N4916, 50211610
- TRANSISTOR, FIELD EFFECT, N-CHANNEL, 2N4861, 50218100.
- TRANSISTOR, SILICON, PNP, 2N4406, 50221600.
- TRANSISTOR, SILICON, NPN, 2N4922, 50220901.
- TRANSISTOR, SILICON, NPN, 2N3020, 50211900.
- TRANSISTOR, SILICON, PNP, 2N4919, 50221001.
- DIODE GERMANIUM, 11601200
- RESISTOR VALUE TO BE DETERMINED PER 70740800.

10. +V IS +14.3 VDC
-V IS -14.3 VDC

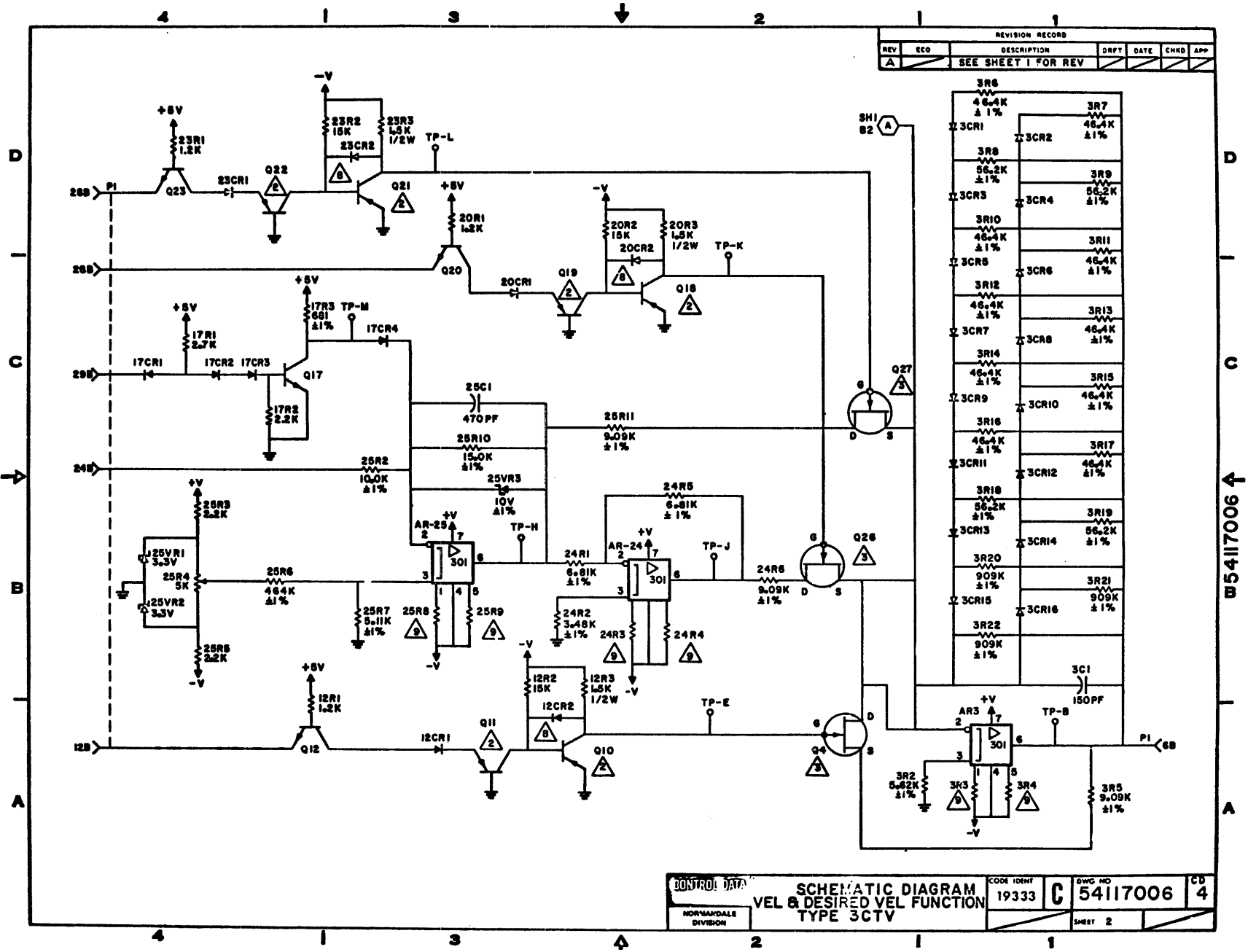
SHEET NO. (TYP)
DRAWING ZONE (TYP)



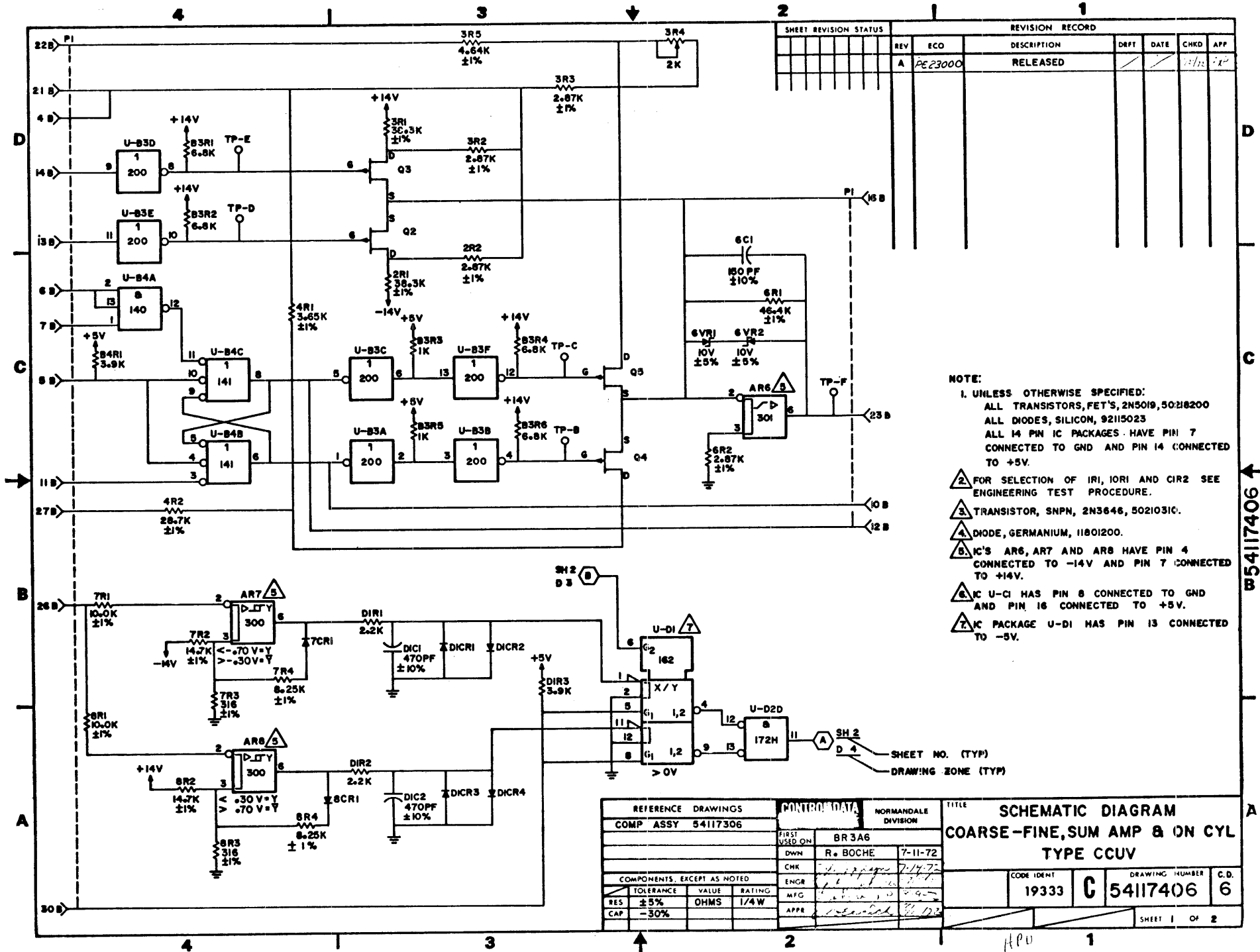
REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMPONENT ASSY TYPE 3CTV 54116908	FIRST USED ON BR3A6		SCHMATIC DIAGRAM VEL & DESIRED VEL FUNCTION TYPE 3CTV
COMPONENTS, EXCEPT AS NOTED		ENGR	CODE IDENT
RES $\pm 5\%$	OHMS	1/4 W	19333
CAP $\pm 10\%$			C
		APP	DRAWING NUMBER
			54117006
			CD
			4
			SHEET 1 OF 2
			HPD-C

B 54117006

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM VEL & DESIRED VEL FUNCTION TYPE 3CTV		CODE IDENT 19333	DWG NO C 54117006	CD 4
				SHEET 2	



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					

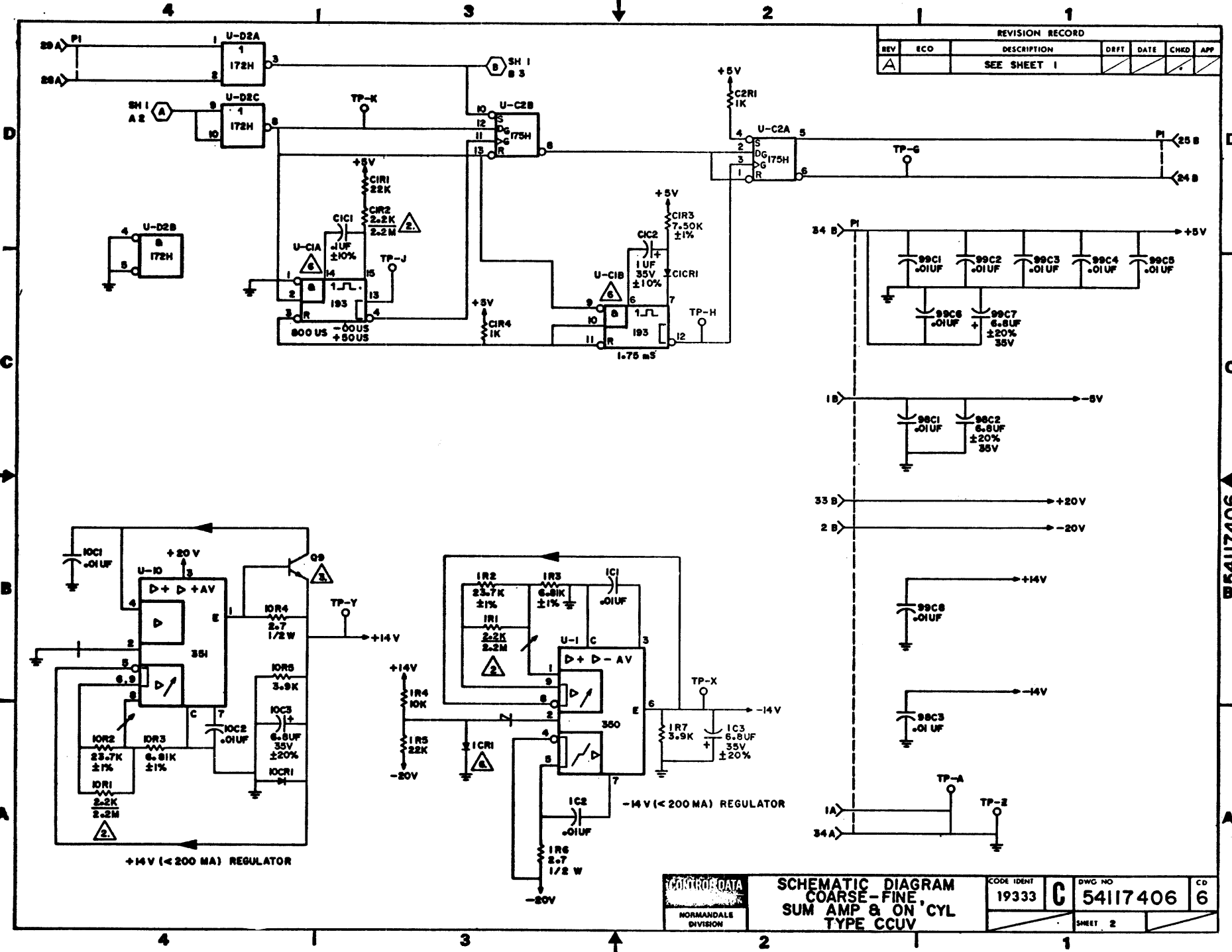
- NOTE:**
1. UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, FET'S, 2N5019, 50218200
ALL DIODES, SILICON, 92115023
ALL 14 PIN IC PACKAGES HAVE PIN 7
CONNECTED TO GND AND PIN 14 CONNECTED
TO +5V.
 2. FOR SELECTION OF IRI, IORI AND CIR2 SEE
ENGINEERING TEST PROCEDURE.
 3. TRANSISTOR, SNPN, 2N3646, 5021031C.
 4. DIODE, GERMANIUM, 11801200.
 5. IC'S AR6, AR7 AND AR8 HAVE PIN 4
CONNECTED TO -14V AND PIN 7 CONNECTED
TO +14V.
 6. IC U-C1 HAS PIN 8 CONNECTED TO GND
AND PIN 16 CONNECTED TO +5V.
 7. IC PACKAGE U-D1 HAS PIN 13 CONNECTED
TO -5V.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54117306		FIRST USED ON		BR 3A6		SCHEMATIC DIAGRAM	
		DWN		R. BOUCHE		COARSE-FINE, SUM AMP & ON CYL	
		CHK		7-11-72		TYPE CCUV	
		ENGR				CODE IDENT	
		MFG				DRAWING NUMBER	
		APPR				C.D.	
COMPONENTS, EXCEPT AS NOTED		RES ±5%		19333		C 54117406	
CAP -30%		TOLERANCE		VALUE		RATING	
		OHMS		1/4 W		SHEET 1 OF 2	

W54117406

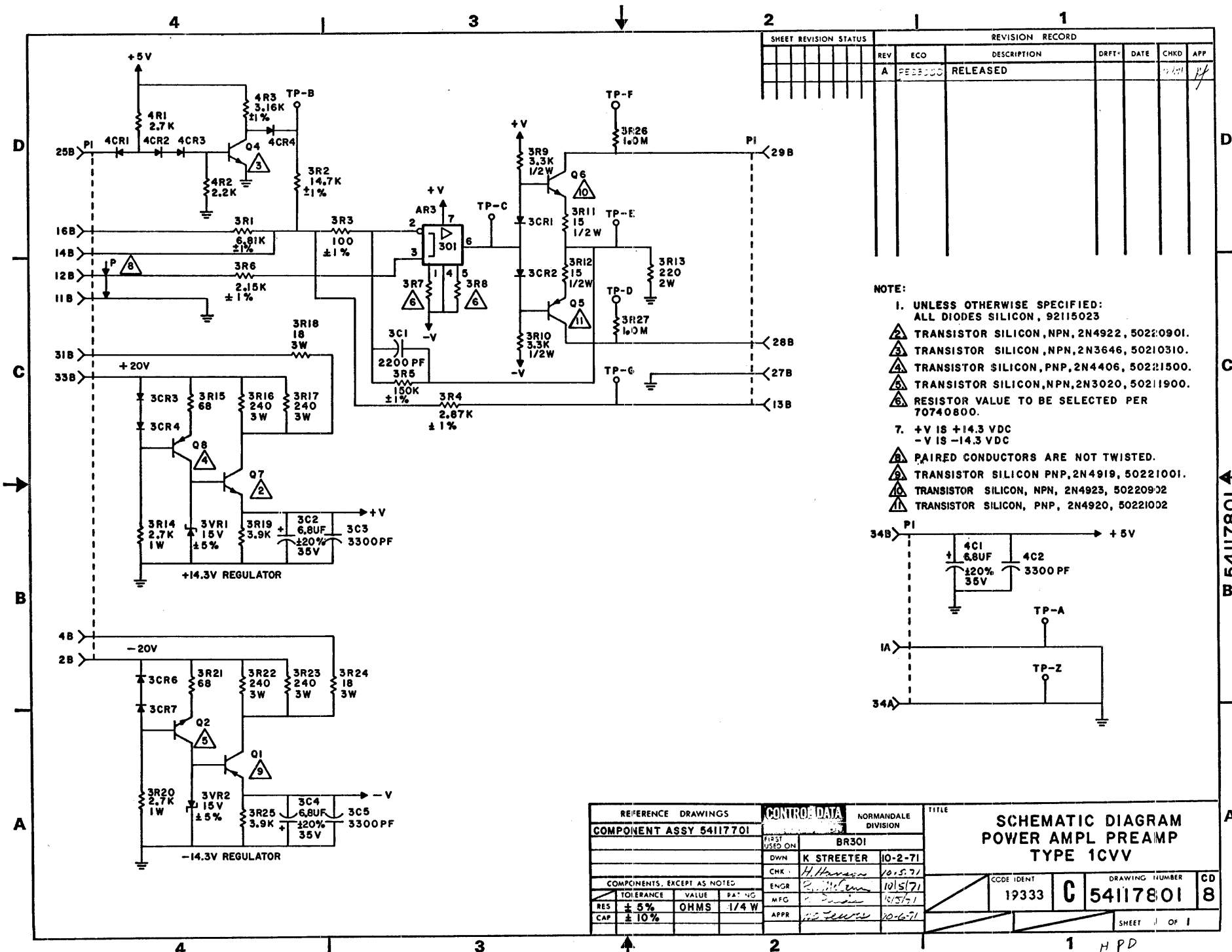
HPU

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

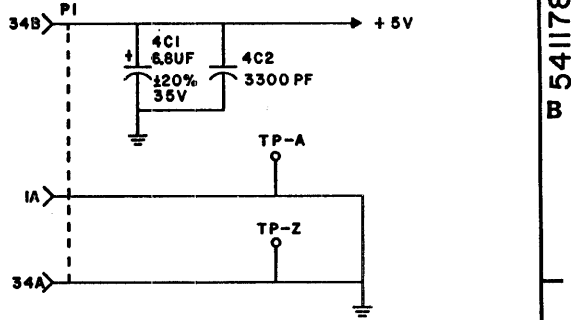


NORMANDALE DIVISION	SCHEMATIC DIAGRAM COARSE-FINE SUM AMP & ON CYL TYPE CCUV		CODE IDENT 19333	DWG NO 54117406	CD 6
				SHEET 2	

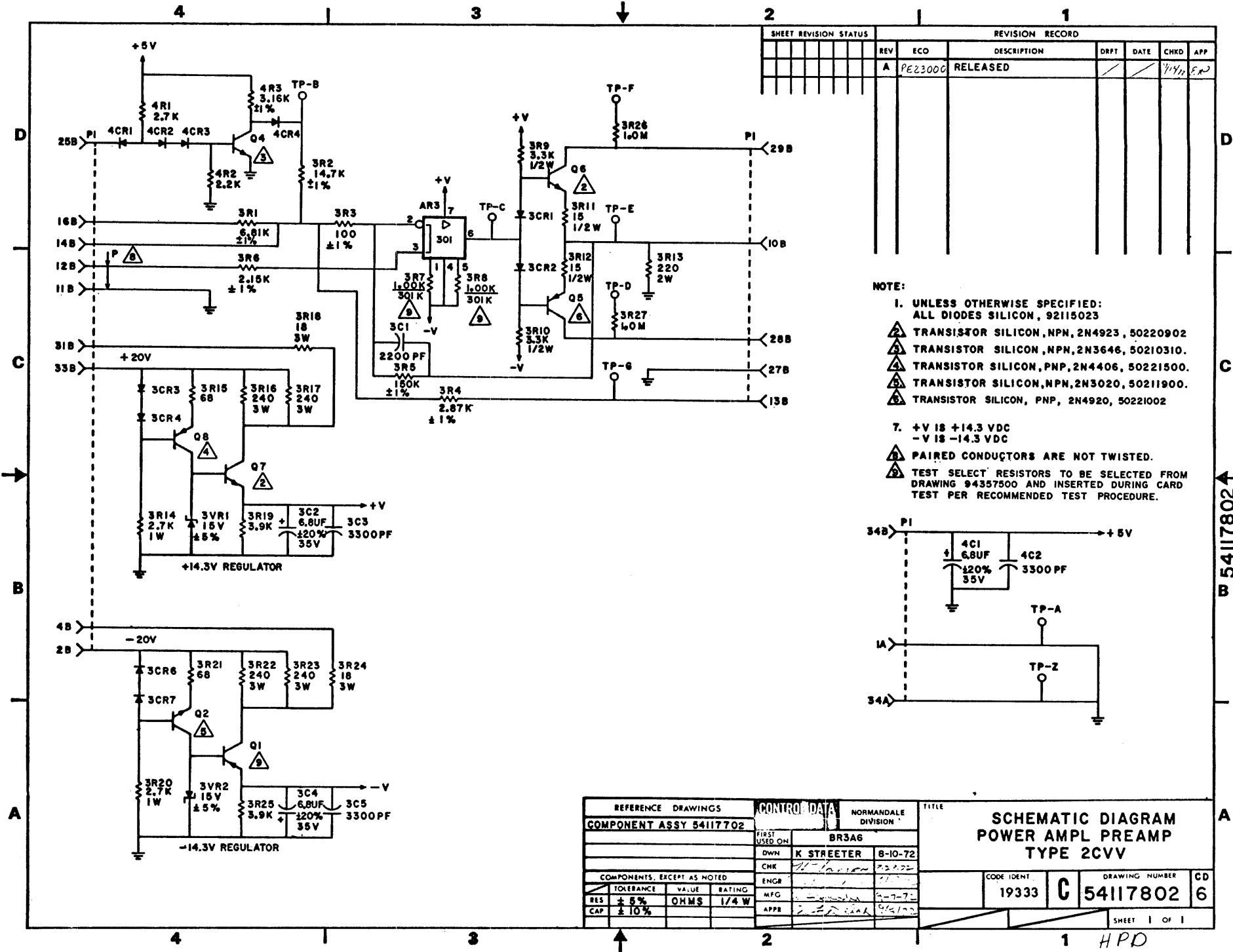
54117406



- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL DIODES SILICON, 92115023
 - TRANSISTOR SILICON, NPN, 2N4922, 50220901.
 - TRANSISTOR SILICON, NPN, 2N3646, 50210310.
 - TRANSISTOR SILICON, PNP, 2N4406, 50221500.
 - TRANSISTOR SILICON, NPN, 2N3020, 50211900.
 - RESISTOR VALUE TO BE SELECTED PER 70740800.
 - +V IS +14.3 VDC
-V IS -14.3 VDC
 - PAIRED CONDUCTORS ARE NOT TWISTED.
 - TRANSISTOR SILICON PNP, 2N4919, 50221001.
 - TRANSISTOR SILICON, NPN, 2N4923, 50220902
 - TRANSISTOR SILICON, PNP, 2N4920, 50221002

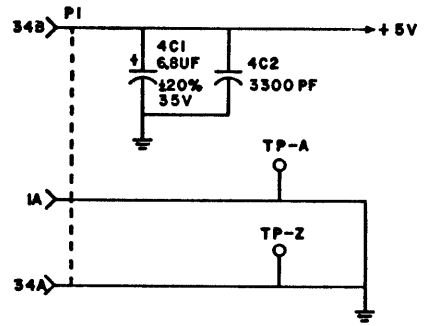


REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 5411701			BR301				SCHEMATIC DIAGRAM POWER AMPL PREAMP TYPE 1CVV	
FIRST USED ON			CHK		ENGR		CODE IDENT	
DWN			K STREETER		10-5-71		DRAWING NUMBER	
COMPONENTS, EXCEPT AS NOTED			ENGR		10/5/71		CD	
TO TOLERANCE			VALUE		PAT' NG		19333	
RES ± 5%			OHMS		1/4 W		C 54117801	
CAP ± 10%							8	
APPR			10-6-71				SHEET 1 OF 1	



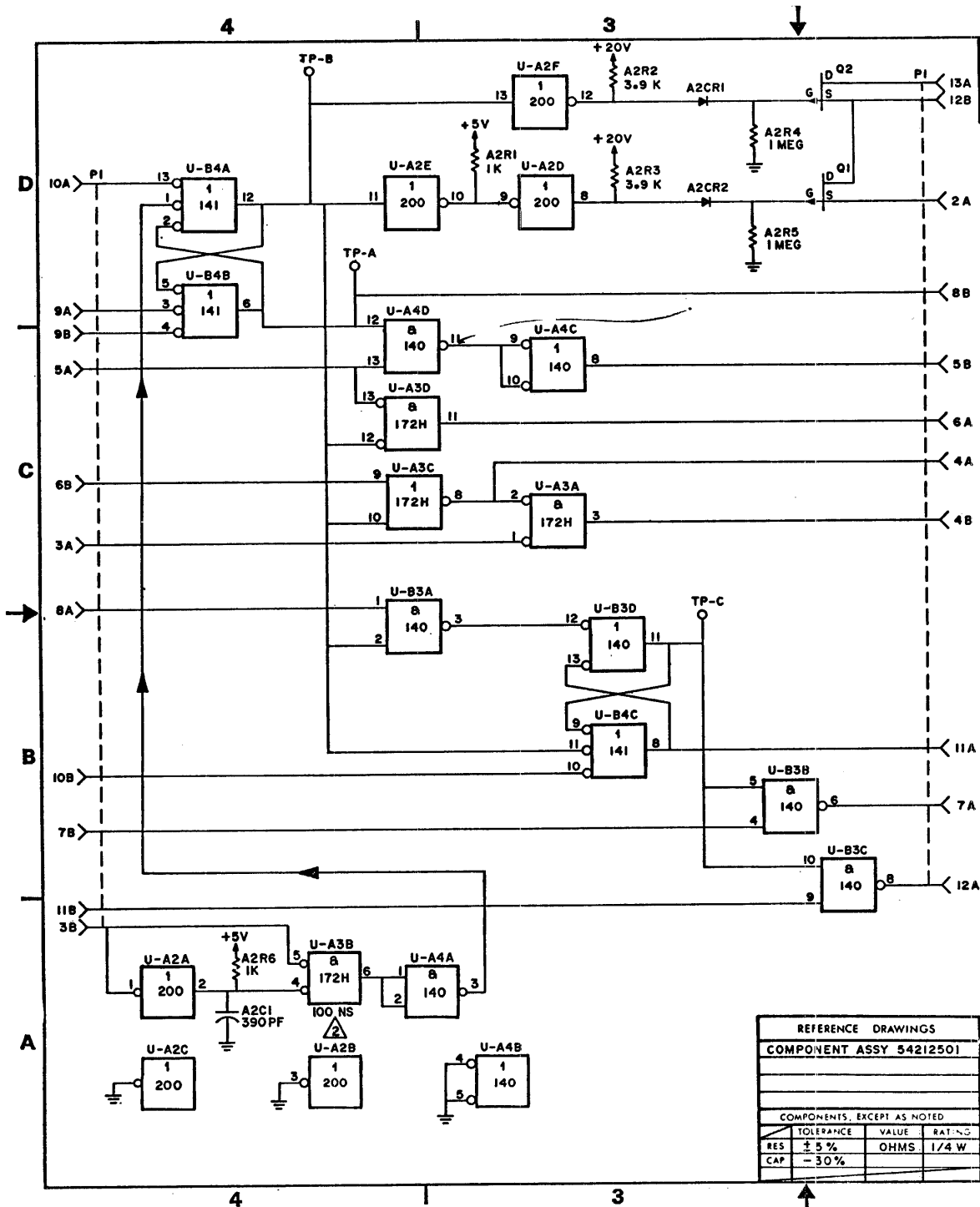
SHEET REVISION STATUS				REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	PE23000	RELEASED						

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL DIODES SILICON, 92115023
 - TRANSISTOR SILICON, NPN, 2N4923, 50220902
 - TRANSISTOR SILICON, NPN, 2N3646, 50210310.
 - TRANSISTOR SILICON, PNP, 2N4406, 50221500.
 - TRANSISTOR SILICON, NPN, 2N3020, 50211900.
 - TRANSISTOR SILICON, PNP, 2N4920, 50221002
7. +V IS +14.3 VDC
-V IS -14.3 VDC
- PAIRED CONDUCTORS ARE NOT TWISTED.
- TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.



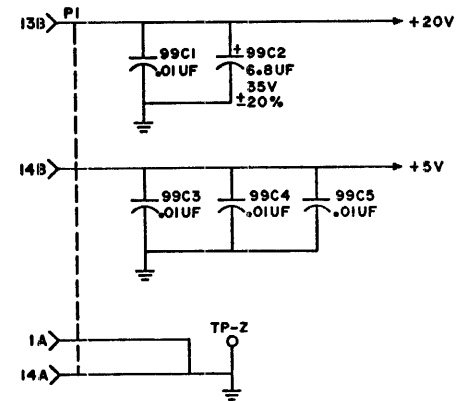
REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMPONENT ASSY 54117702		FIRST USED ON BR3A6		DWN K STREETER 8-10-72		SCHEMATIC DIAGRAM POWER AMPL PREAMP TYPE 2CVV	
COMPONENTS, EXCEPT AS NOTED		ENGR		MFG		APPR	
TOLERANCE	VALUE	RATING					
RES ± 5%	OHMS	1/4 W					
CAP ± 10%							
CODE IDENT. 19333		DRAWING NUMBER C 54117802		CD 6		SHEET 1 OF 1	

HPD



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE 23000	RELEASED		4-28-72			

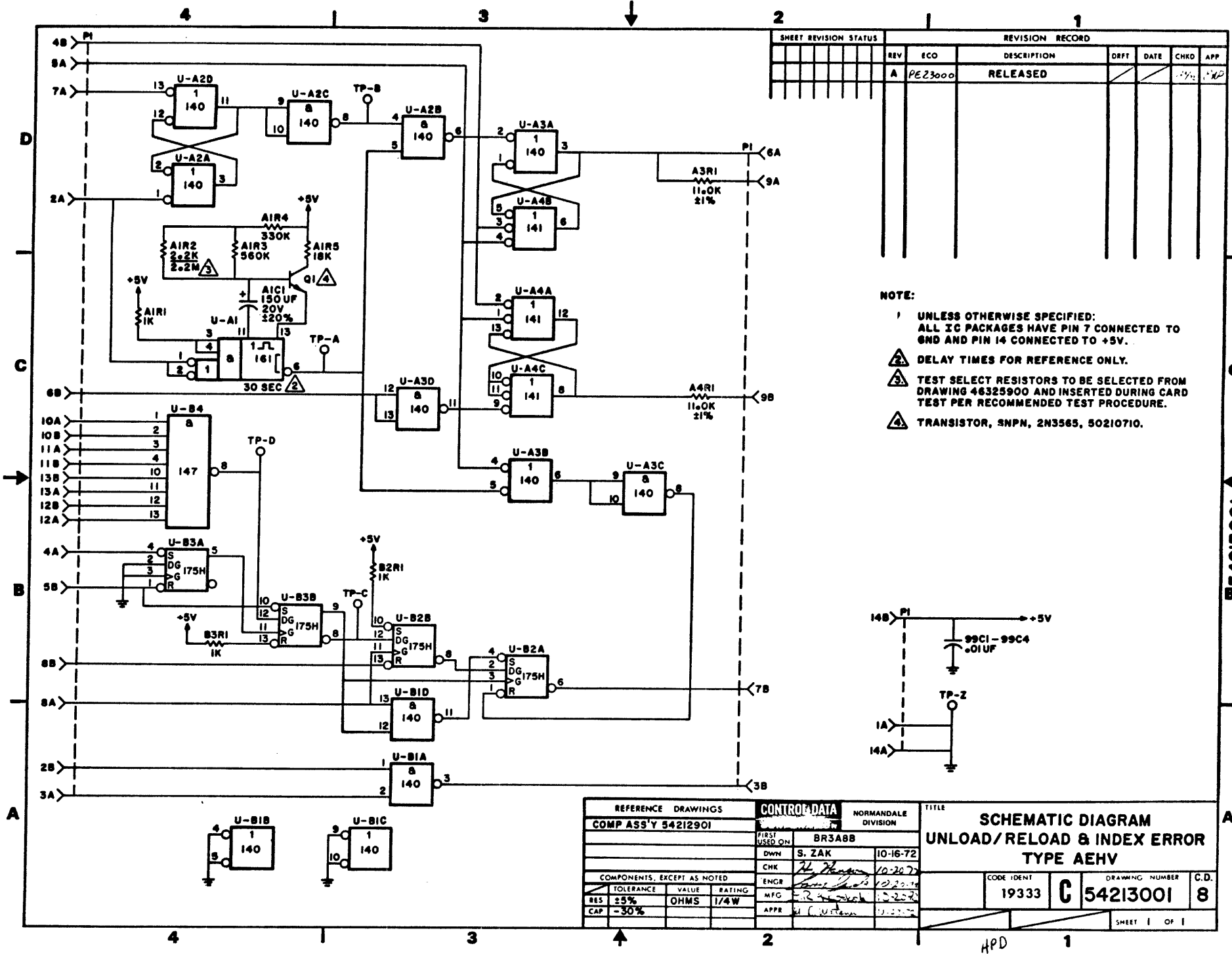
NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, P CHANNEL J FET, 50218200.
 ALL DIODES, SILICON, 24553500.
 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ⚠ DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54212501		FIRST USED ON		BR3AIG		SCHEMATIC DIAGRAM OFFSET CONTROL TYPE AEGV	
COMPONENTS, EXCEPT AS NOTED		DWN		R. KONECNY		CODE IDENT	
TOLERANCE		CHK		7/2/72		DRAWING NUMBER	
RES ± 5%	VALUE OHMS	ENGR		7/2/72		CD	
CAP - 30%	RAT. 1/4 W	MFG		7/2/72		19333 C 54212601 6	
		APPR		7/6/72		SHEET 1 OF 1	

54212601

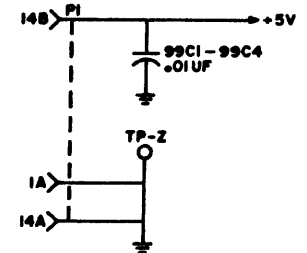
HPO



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					

NOTE:

- 1 UNLESS OTHERWISE SPECIFIED:
ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
- 2 DELAY TIMES FOR REFERENCE ONLY.
- 3 TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 46325900 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
- 4 TRANSISTOR, 9NPN, 2N3565, 50210710.



REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASS'Y 54212901			FIRST USED ON		BR3A8B		SCHEMATIC DIAGRAM	
			DWN		S. ZAK		UNLOAD/RELOAD & INDEX ERROR	
			CHK		10-20-72		TYPE AEHV	
COMPONENTS, EXCEPT AS NOTED			ENGR		12-20-72		CODE IDENT	
			MFG		12-20-72		DRAWING NUMBER	
			APPR		12-20-72		19333 C 54213001 8	
TOLERANCE	VALUE	RATING						
RES ±5%	OHMS	1/4W						
CAP -30%								
							SHEET 1 OF 1	

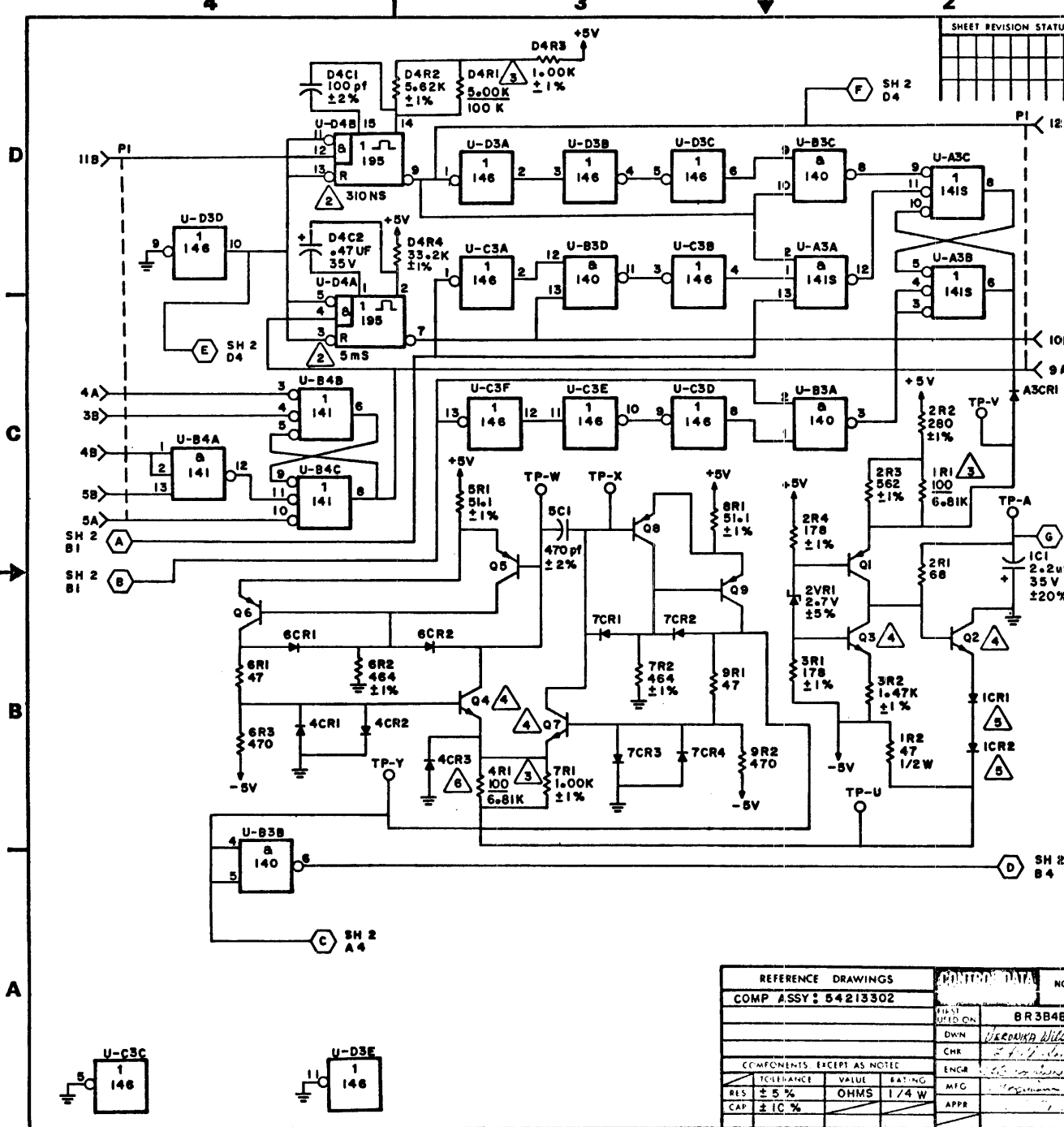
54213001 ↑

HPD

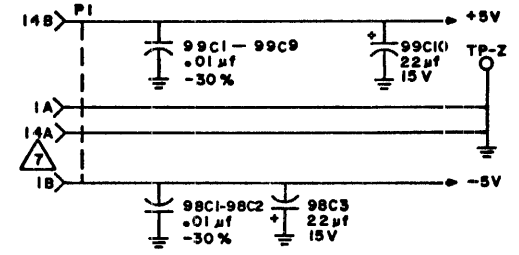
70629100 E

4-53

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHRD	APP	
A	PE23000	RELEASED		1-5-75		CR	



- NOTES
- UNLESS OTHERWISE SPECIFIED:
ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
ALL TRANSISTORS, SPNP, 2N4258, 50211510.
ALL DIODES, SILICON, SCHOTTY, 50241400.
 - DELAY TIME FOR REFERENCE ONLY.
 - TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
 - ALL TRANSISTORS, SPNP, 2N3646, 50210310.
 - DIODES, SILICON, 92115023.
 - DIODES, SILICON, 92115021.
 - CONNECTOR PINS 2,3,10,11,12,13, ROW A ARE GROUNDED.
 - IC U-A2, ELEMENT NO. 162, HAS PIN 13 CONNECTED TO -5V.



REFERENCE DRAWINGS		NORMANDEALE DIVISION		TITLE		
COMP ASSY: 54213302		8 R 3B4B		SCHEMATIC DIAGRAM		
		DWN		8/30/75		
		CHR		8/30/75		
		ENGR		8/30/75		
		MFG		8/30/75		
		APPR		8/30/75		
COMPONENTS EXCEPT AS NOTED				CODE IDENT	LEAVING NUMBER	CD
TOLERANCE	VALUE	RATING	19333	C 54213402	8	
RES	± 5 %	OHMS	1/4 W			
CAP	± 10 %					
				SHEET 1	OF 2	

HPD

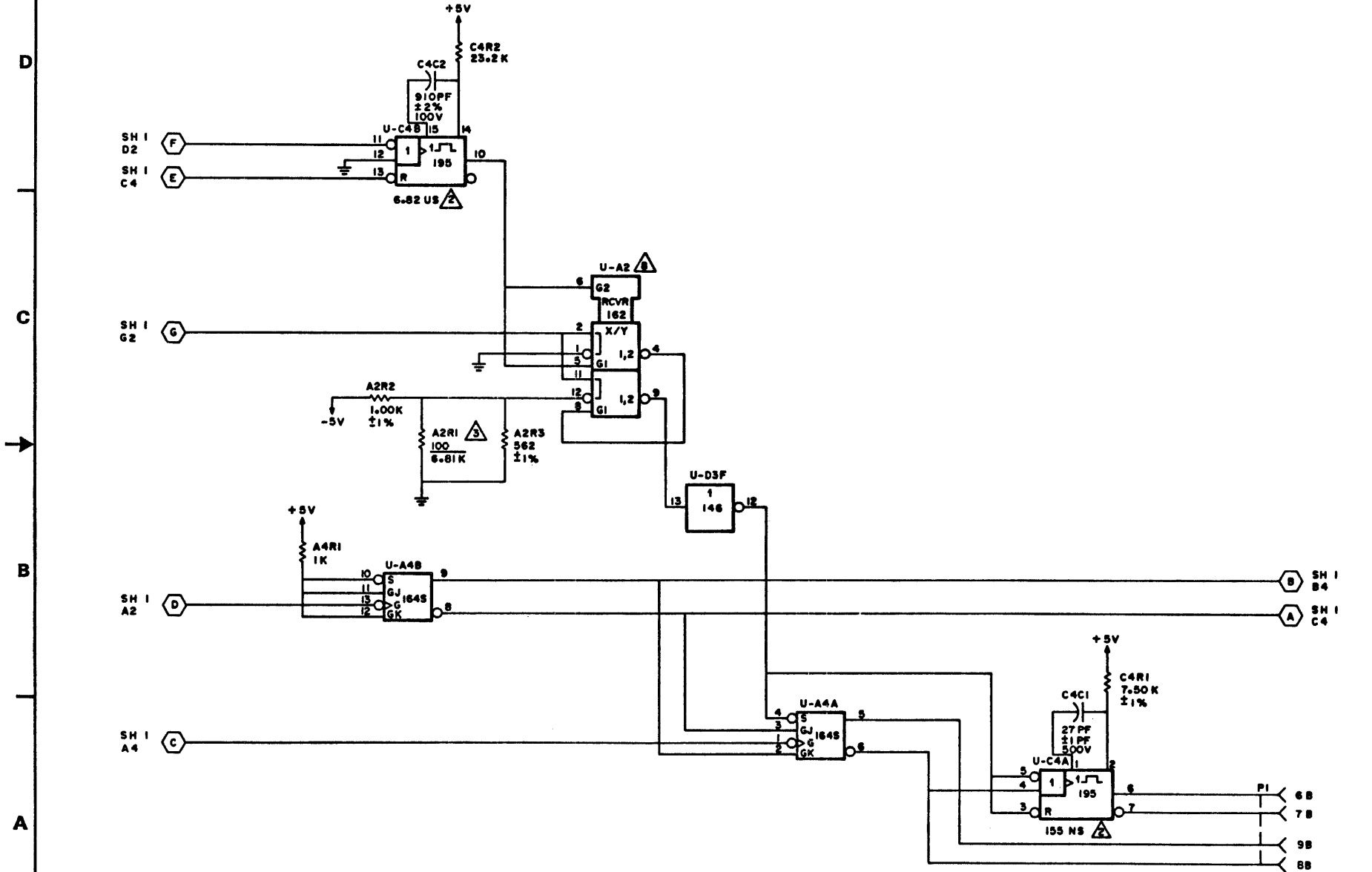
1

54213402

4-54

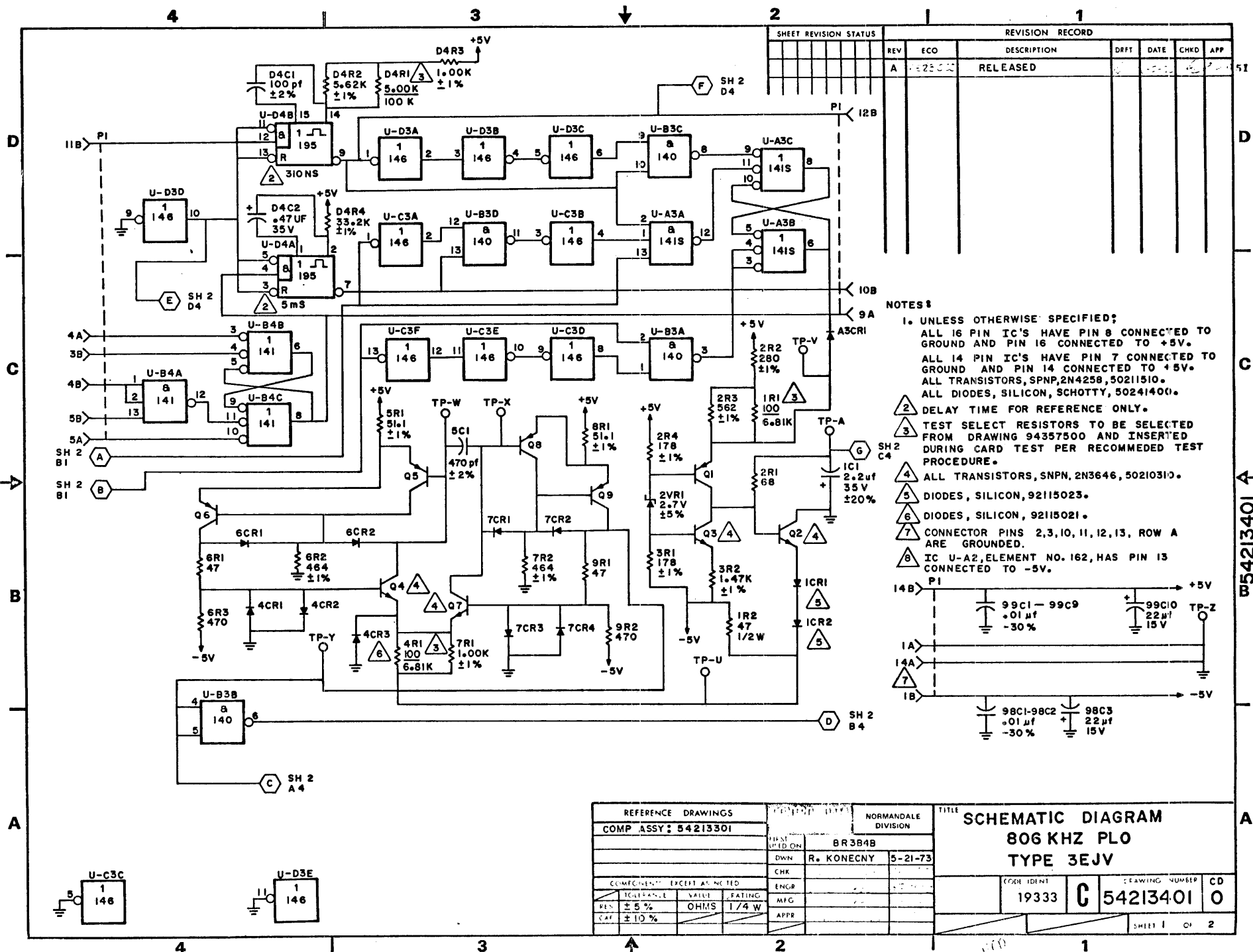
70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



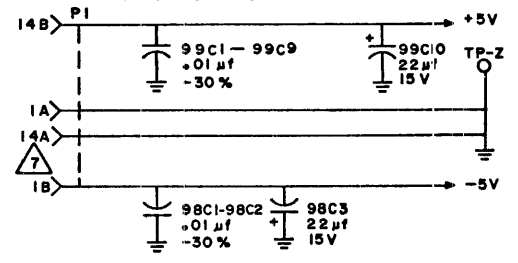
NORMANDE DIVISION	SCHEMATIC DIAGRAM TYPE AEJV		CODE IDENT 19333	C	DWG NO 54213402	CD 8
			SHEET 2			

54213402



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	22000	RELEASED					

- NOTES:
- UNLESS OTHERWISE SPECIFIED; ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V. ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V. ALL TRANSISTORS, SPNP, 2N4258, 50211510. ALL DIODES, SILICON, SCHOTTY, 50241400.
 - DELAY TIME FOR REFERENCE ONLY.
 - TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
 - ALL TRANSISTORS, SPNP, 2N3646, 50210310.
 - DIODES, SILICON, 92115023.
 - DIODES, SILICON, 92115021.
 - CONNECTOR PINS 2,3,10,11,12,13, ROW A ARE GROUNDED.
 - IC U-A2, ELEMENT NO. 162, HAS PIN 13 CONNECTED TO -5V.

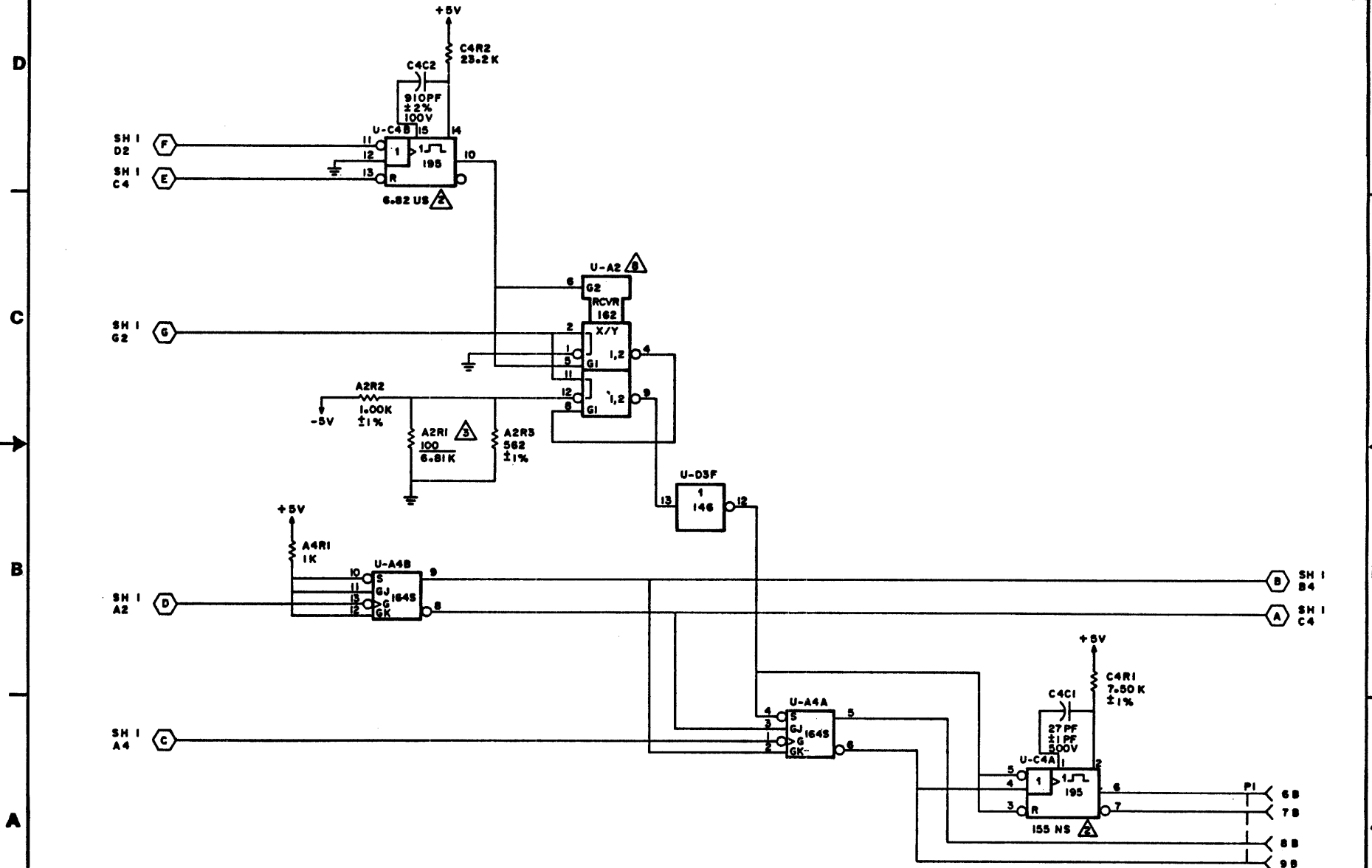


REFERENCE DRAWINGS		NORMANDEALE DIVISION		TITLE	
COMP ASSY: 54213301		BR3B4B		SCHEMATIC DIAGRAM	
		R. KONECNY		806 KHZ PLO	
		5-21-73		TYPE 3EJV	
CONNECTOR: EXCEPT AS NOTED		ENGR		CODE IDENT	
TOLERANCE: VALUE: RATING:		MFG		DRAWING NUMBER	
RES ± 5% OHMS 1/4 W		APPR		19333 C 54213401 0	
CAP ± 10%				SHEET 1 OF 2	

4-56

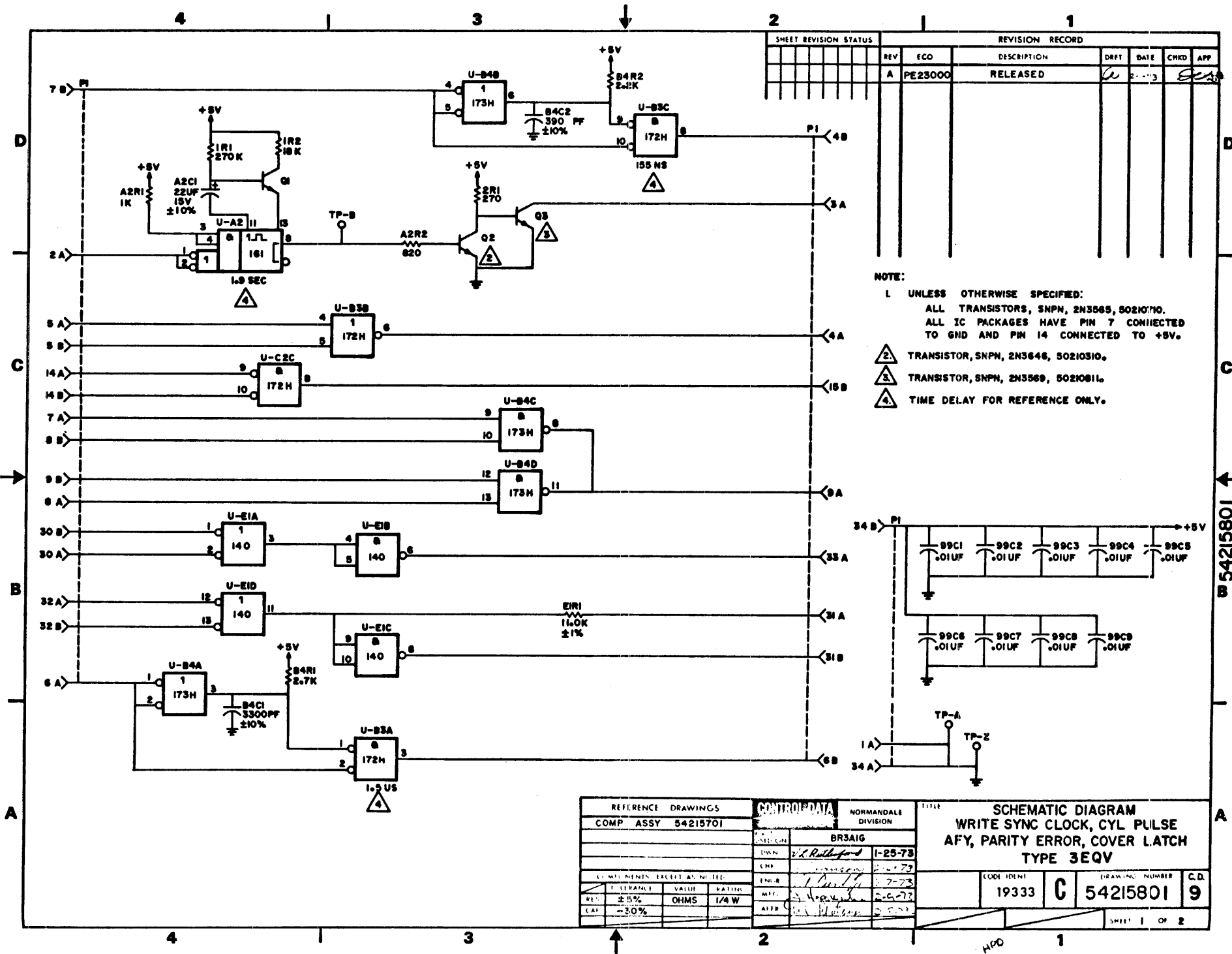
70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3EJV		CODE IDENT 19333	DWG NO 54213401	CD 0
				SHEET 2	

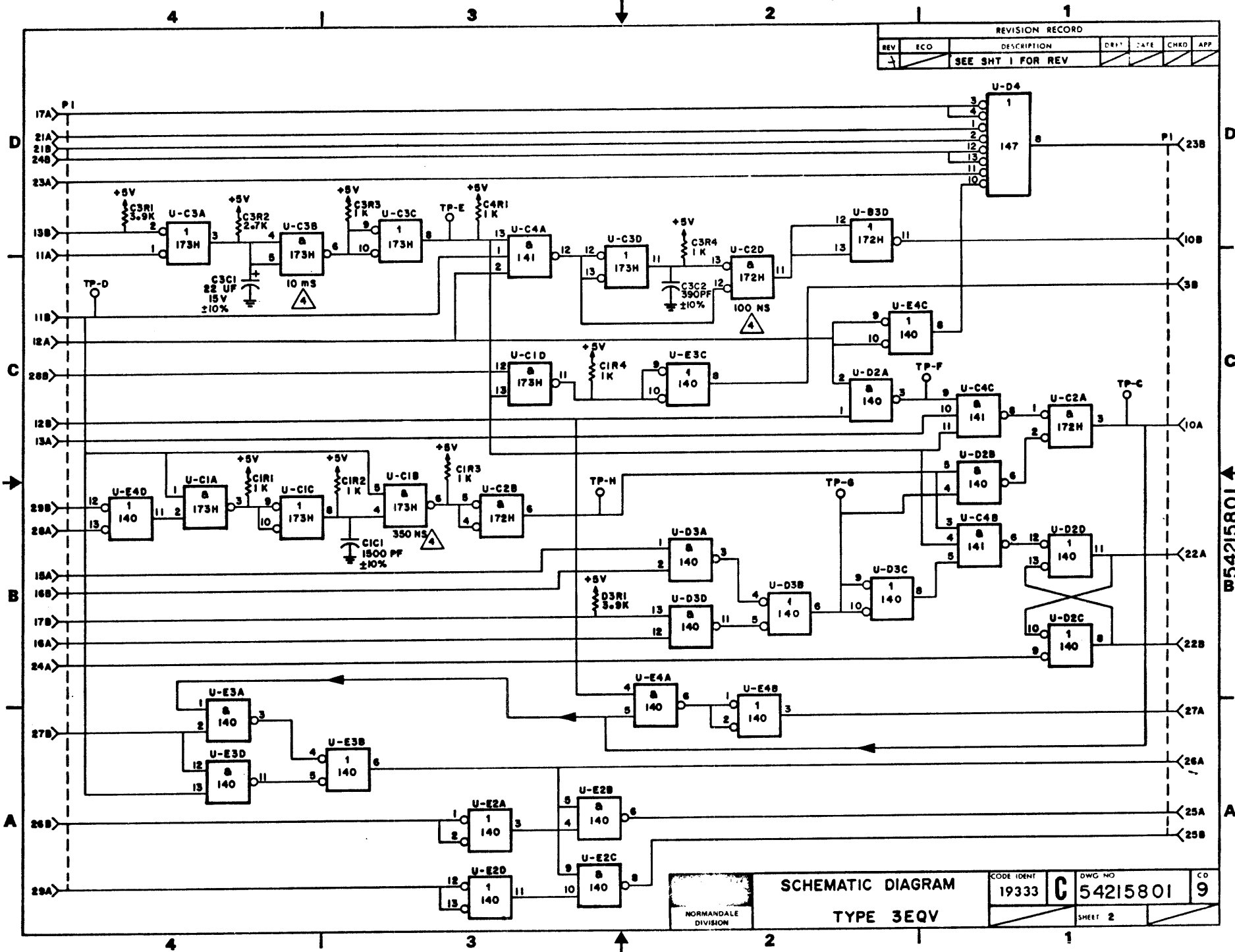
W54213401



REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE
COMP ASSY 54215701	BR3AIG		SCHMATIC DIAGRAM
			WRITE SYNC CLOCK, CYL PULSE
			AFY, PARITY ERROR, COVER LATCH
			TYPE 3EQV
U. Mfg. REVISIONS EXCEPT AS NOTED	DATE	BY	CODE IDENT
REV. ±5%	VALUE	RATING	19333
RES. ±20%	OHMS	1/4 W	C 54215801
			9
			SHEET 1 OF 2

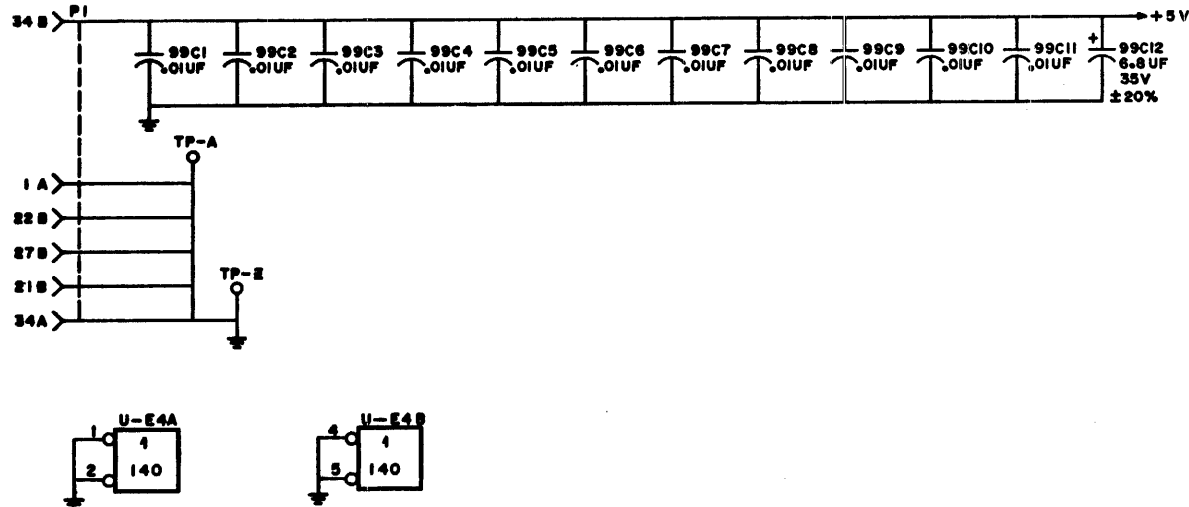
4-58

70629100 E



54215801

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE13000	RELEASED					

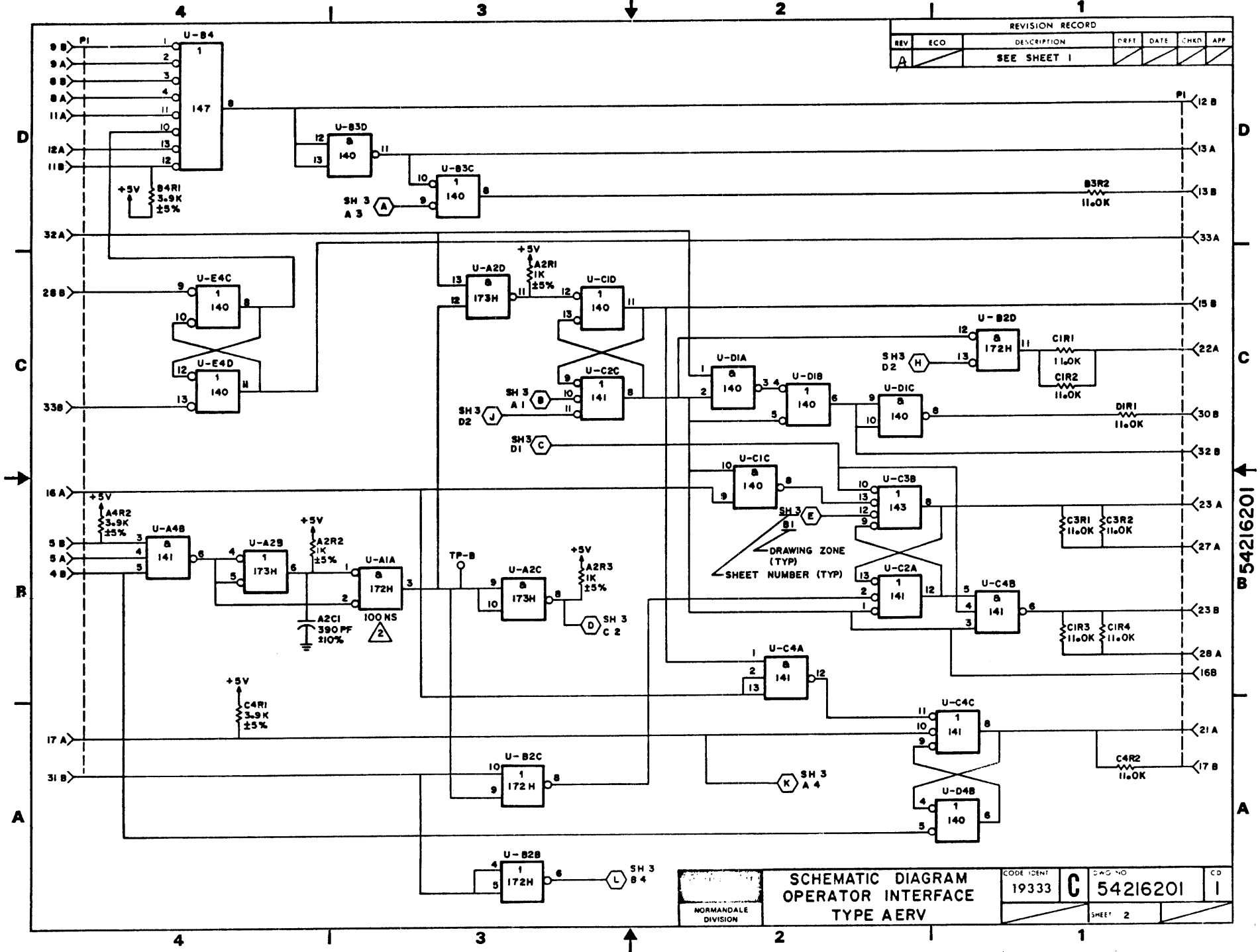


NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N2221, 50210102.
 ALL DIODES, SILICON, 24553500.
 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIMES FOR REF ONLY.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54216101		FIRST USED ON		BR3AIG		SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE AERV	
		DWN		D. G. TUTTLE		1-25-72	
		CHK		[Signature]		12-14-72	
COMPONENTS, EXCEPT AS NOTED		ENGR		[Signature]		12-14-72	
		MFG		[Signature]		12-14-72	
		APPR					
TOLERANCE		VALUE		RATING		CODE IDENT	
RES ±1%		OHMS		1/4 W		19333 C	
CAP -30%						DRAWING NUMBER	
						54216201	
						C. D.	
						1	
						SHEET 1 OF 3	

54216201

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

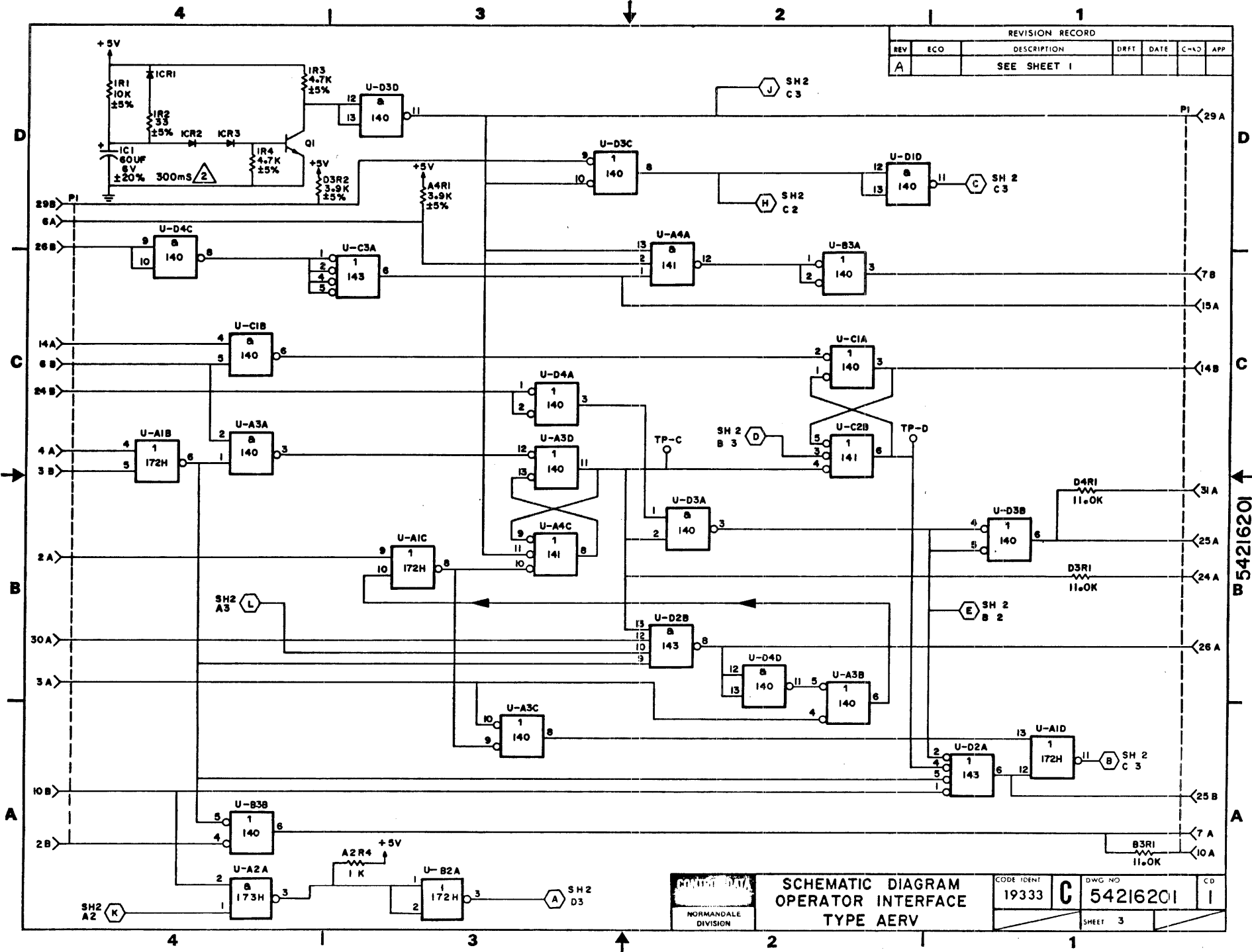


NORMANDE DIVISION	SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE AERV		CODE IDENT 19333	DWG NO C 54216201	CD 1
				SHEET 2	

70629100 F

4-60.1/4-60.2

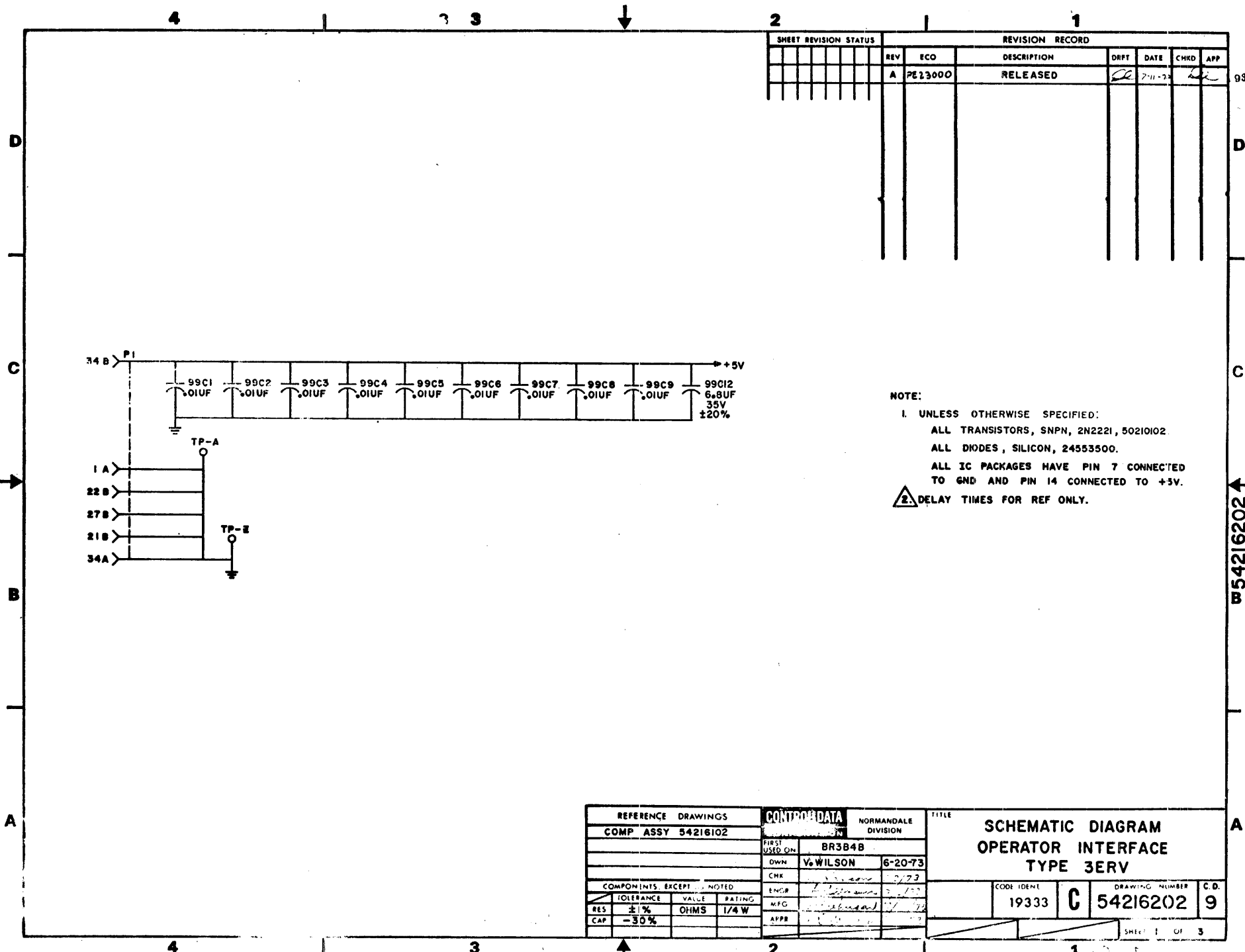
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	C-NO	APP
A		SEE SHEET 1				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE AERV		CODE IDENT 19333	DWG NO 54216201	CD 1
			SHEET 3		

70629100 F

4-60.3



NOTE:

- 1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N2221, 50210102.
 ALL DIODES, SILICON, 24553500.
 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
- 2. DELAY TIMES FOR REF ONLY.

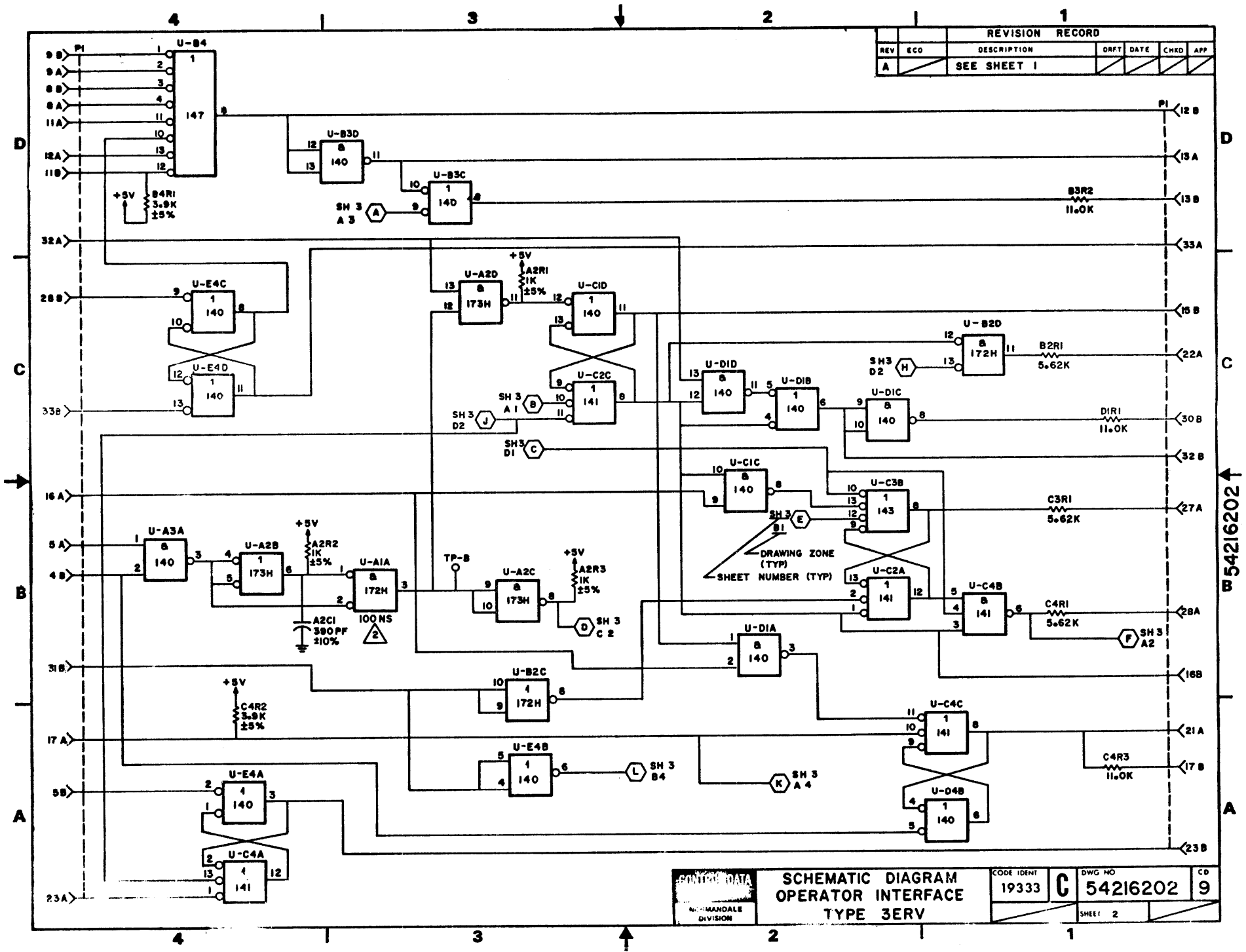
SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE13000	RELEASED		7-11-73			93

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54216102		FIRST USED ON		BR3B4B		SCHEMATIC DIAGRAM	
		DWN		V. WILSON		OPERATOR INTERFACE	
		CHK		6-20-73		TYPE 3SERV	
COMPONENTS, EXCEPT NOTED		ENGR				CODE IDENT	
TOLERANCE		MFG				DRAWING NUMBER	
RES	±1%	OHMS	1/4 W			C.D.	
CAP	-30%					9	
						19333	
						C 54216202	
						Sheet 1 of 3	

4-60.4

70629100 F

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



**SCHEMATIC DIAGRAM
OPERATOR INTERFACE
TYPE 3ERV**

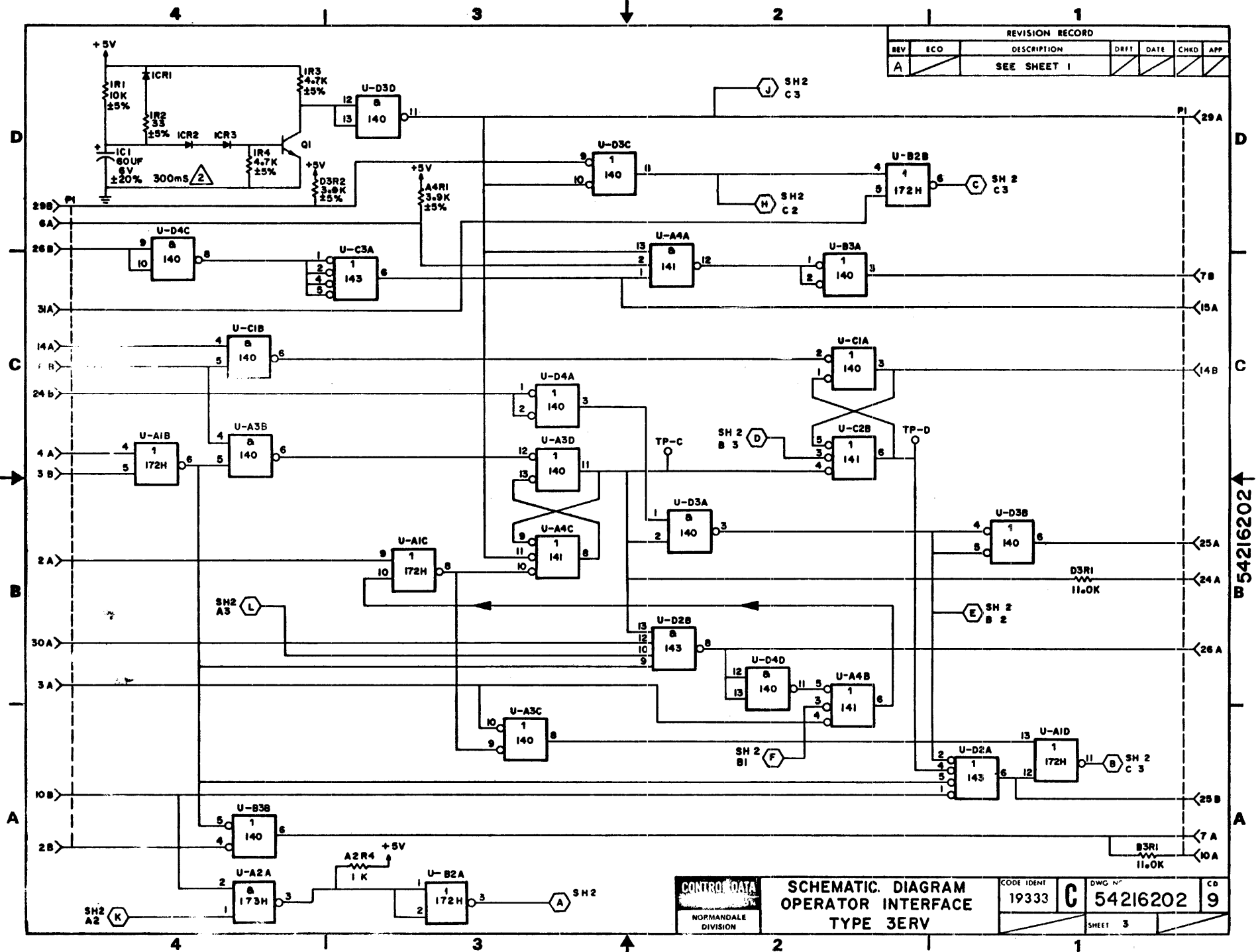
CODE IDENT 19333	DWG NO 54216202	CD 9
SHEET 2		

54216202

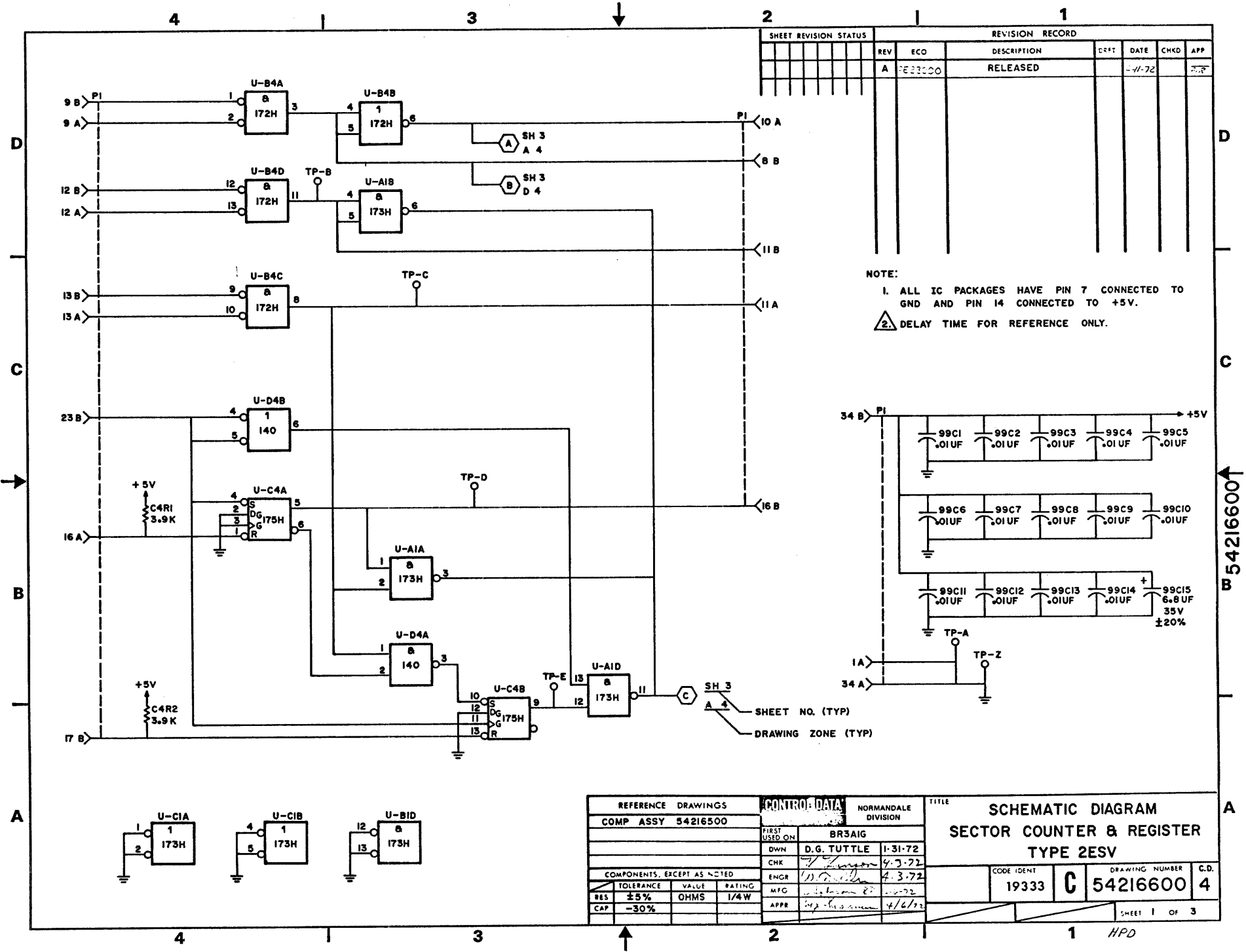
70629100 F

4-61

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

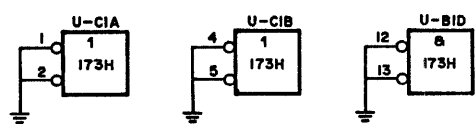
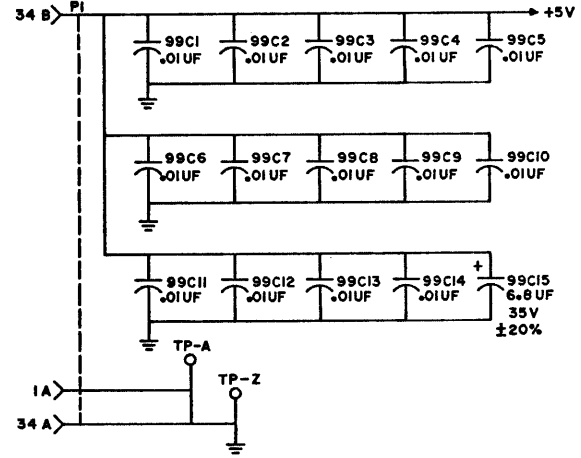


CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM OPERATOR INTERFACE TYPE 3ERV		CODE IDENT 19333	DWG. NO. C 54216202	CD 9
				SHEET 3	



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DEFT	DATE	CHKD	APP
A	FE23000	RELEASED		1-1-72		

NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIME FOR REFERENCE ONLY.

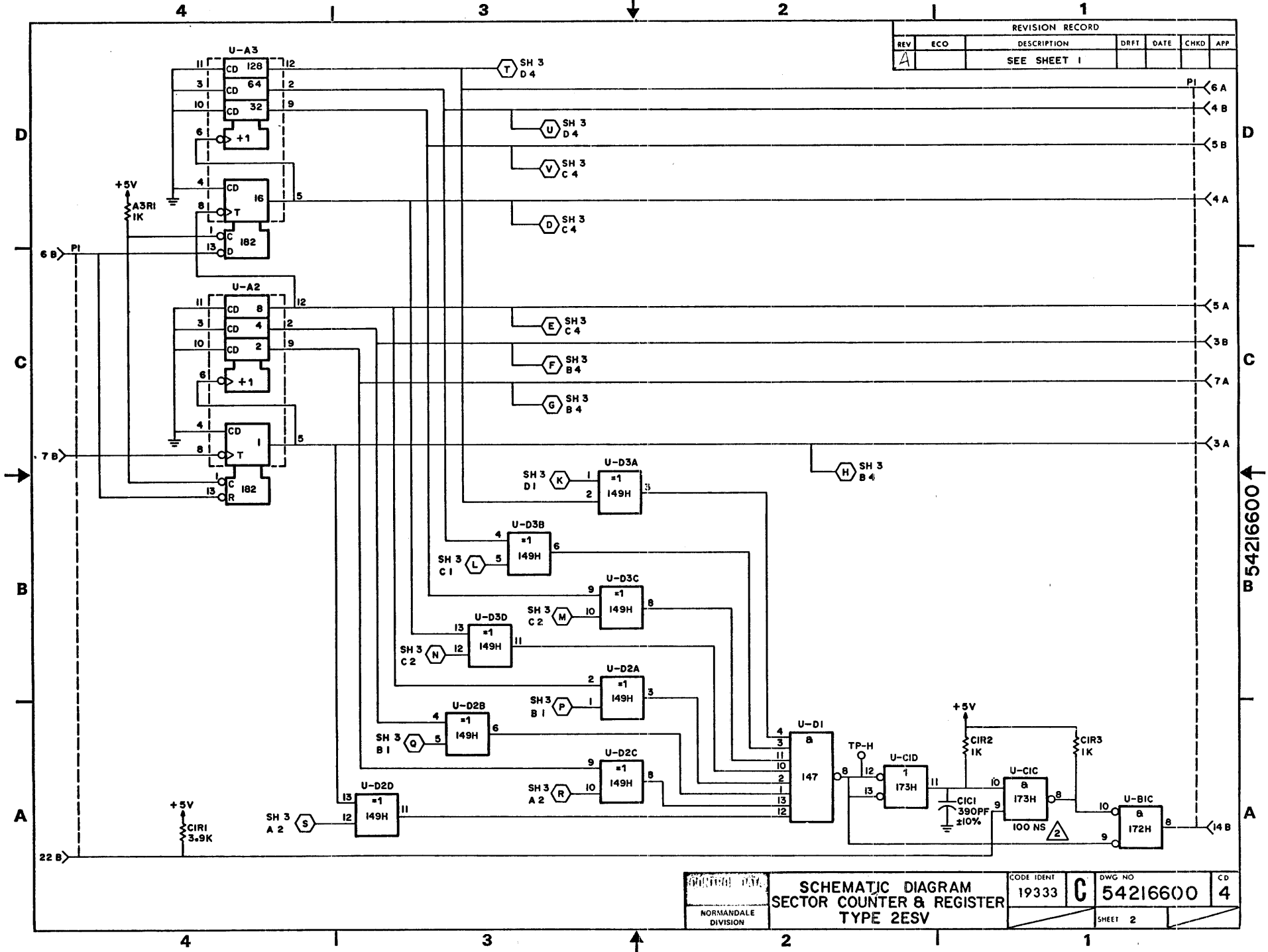


REFERENCE DRAWINGS	CONTROL DATA	NORMANDEALE DIVISION	TITLE	
COMP ASSY 54216500	FIRST USED ON	BR3AIG	SCHEMATIC DIAGRAM	
	OWN	D.G. TUTTLE	SECTOR COUNTER & REGISTER	
	CHK	4-3-72	TYPE 2ESV	
	ENGR	4-3-72	CODE IDENT	DRAWING NUMBER
COMPONENTS, EXCEPT AS NOTED			19333	C 54216600 4
TOLERANCE	VALUE	RATING		
RES ±5%	OHMS	1/4W		
CAP -30%				
	MFG			
	APPR			

70629100 E

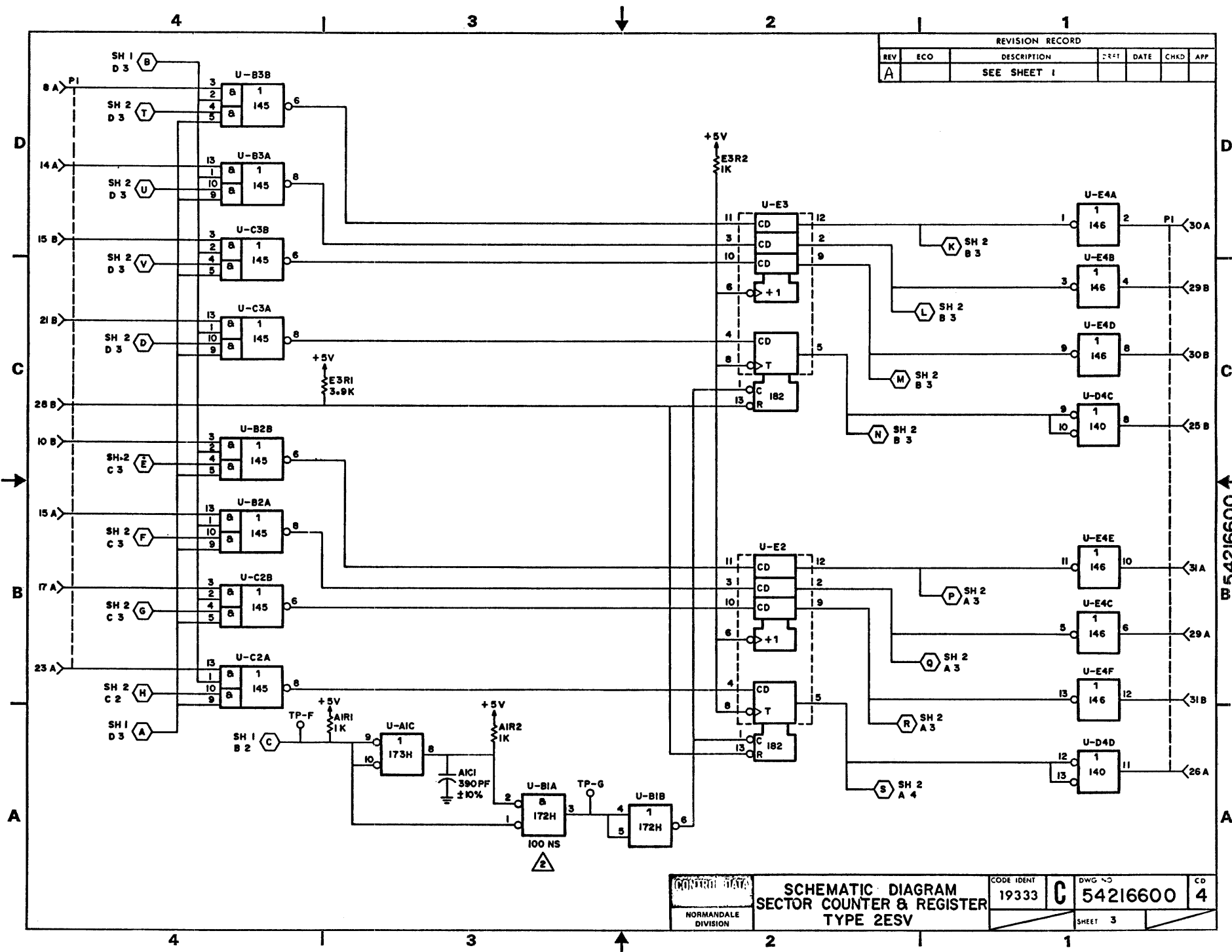
4-63

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

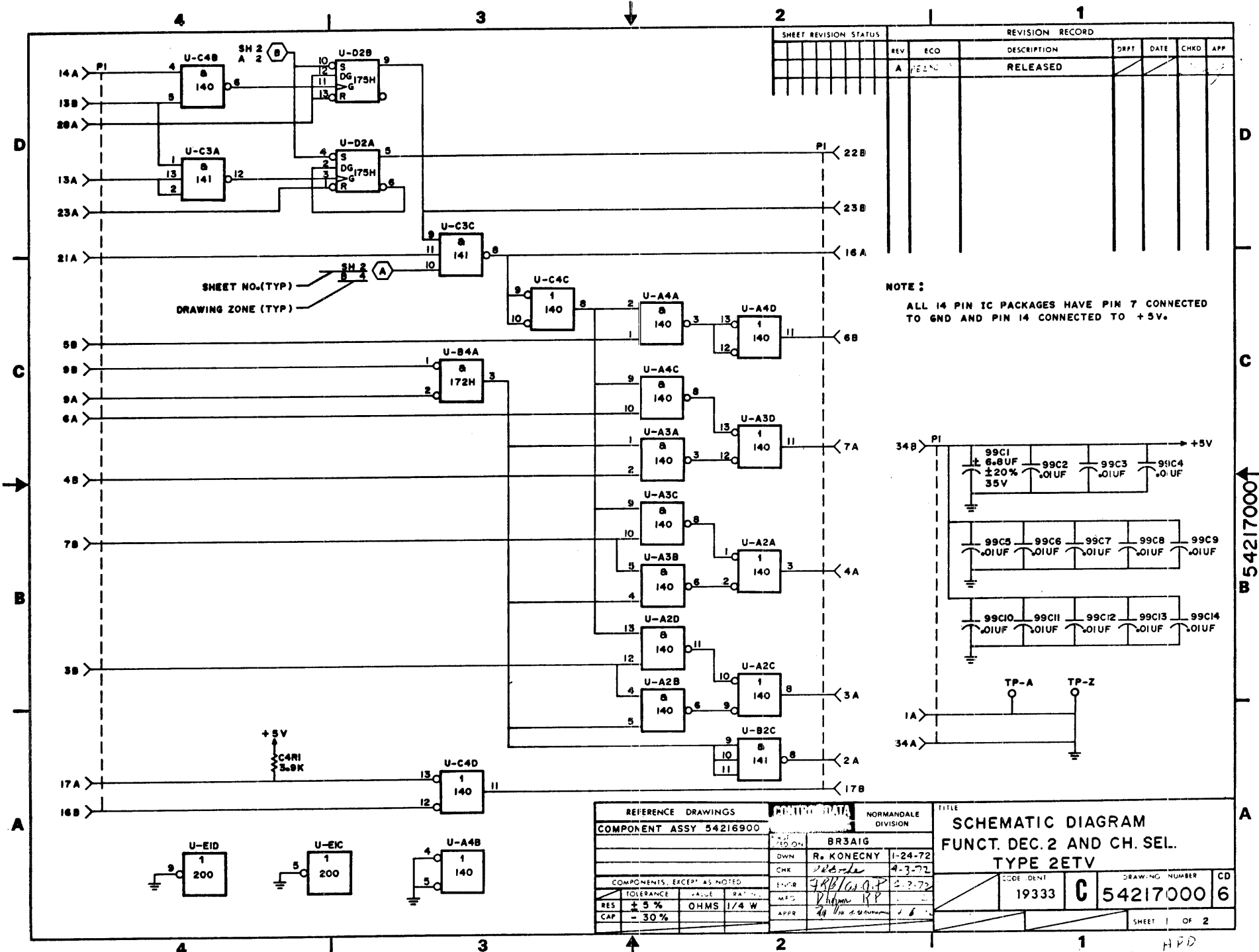


NORMANDE DIVISION	SCHEMATIC DIAGRAM SECTOR COUNTER & REGISTER TYPE 2ESV	CODE IDENT	DWG NO	CD
		19333	C 54216600	4
		SHEET 2		

REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHEET 1				

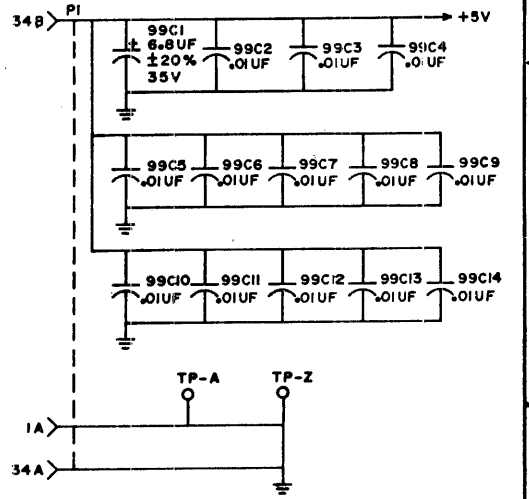


NORMANDE DIVISION	SCHEMATIC DIAGRAM SECTOR COUNTER & REGISTER TYPE 2ESV		CODE IDENT 19333	DWG NO 54216600	CD 4
				SHEET 3	



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					

NOTE:
ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



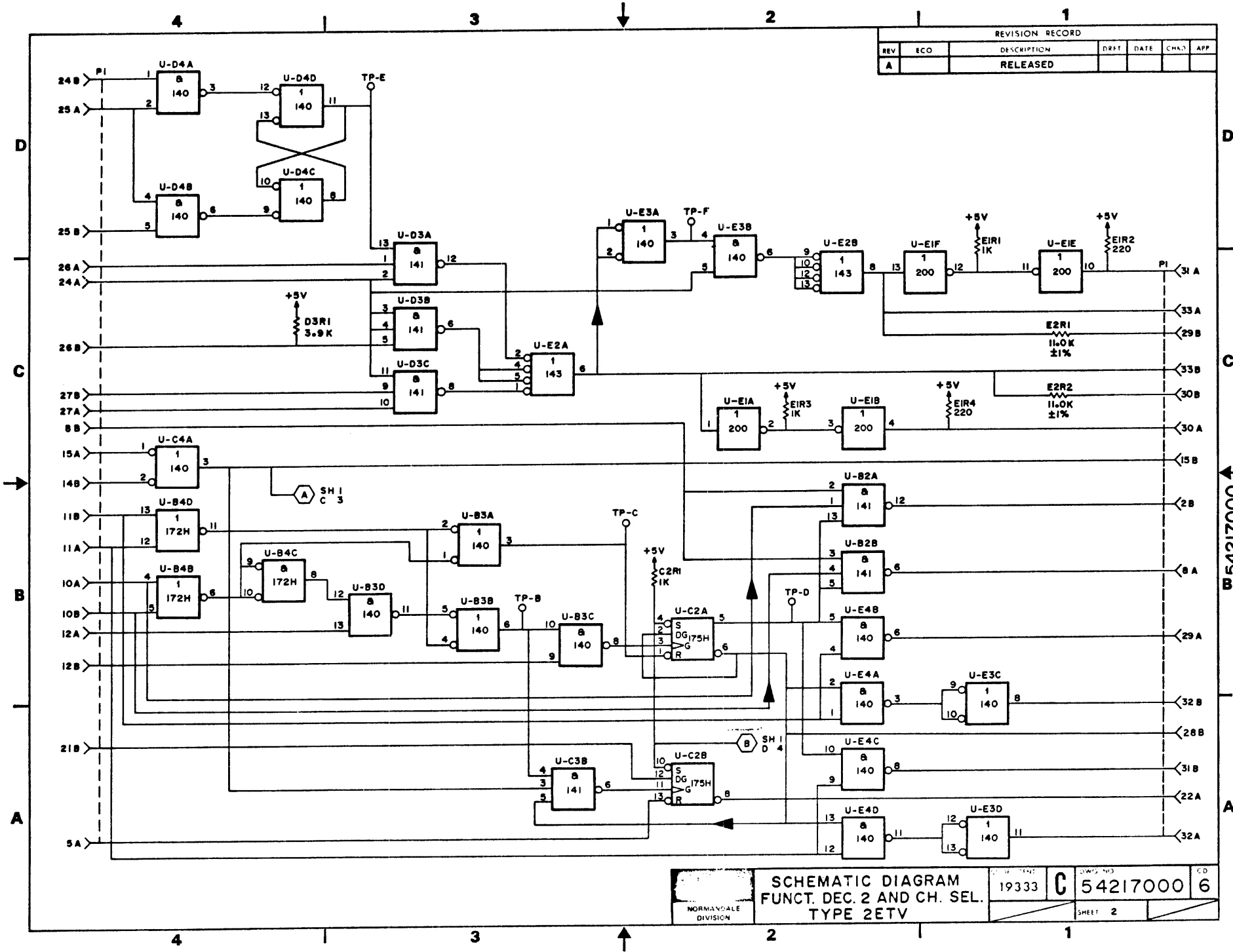
REFERENCE DRAWINGS	BR3AIG	NORMANDEALE DIVISION	TITLE
COMPONENT ASSY 54216900	BR3AIG		SCHEMATIC DIAGRAM
	DWN R. KONECNY 1-24-72		FUNCT. DEC. 2 AND CH. SEL.
	CHK 4-3-72		TYPE 2ETV
COMPONENTS, EXCEPT AS NOTED	ENGR 2-2-72		CODE IDENT 19333
TOLERANCE VALUE RAT	MFG		DRAWING NUMBER 54217000
RES ± 5% OHMS 1/4 W	APPR		CD 6
CAP - 30%			SHEET 1 OF 2

HPD

4-66

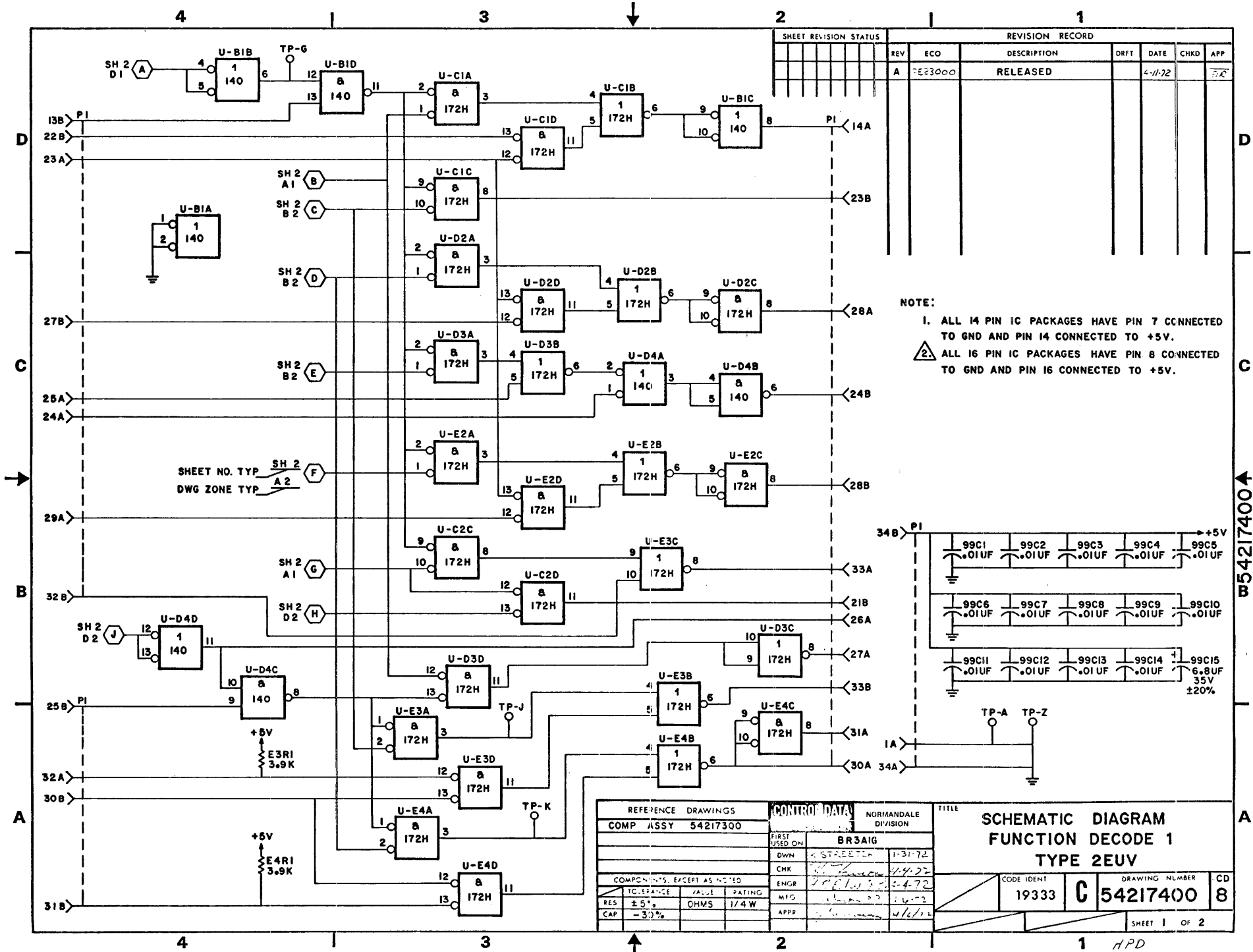
70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHG	APP
A		RELEASED				



NORMAN DALE DIVISION	SCHEMATIC DIAGRAM FUNCT. DEC. 2 AND CH. SEL. TYPE 2ETV		19333	C	54217000	6
			SHEET 2			

B 54217000



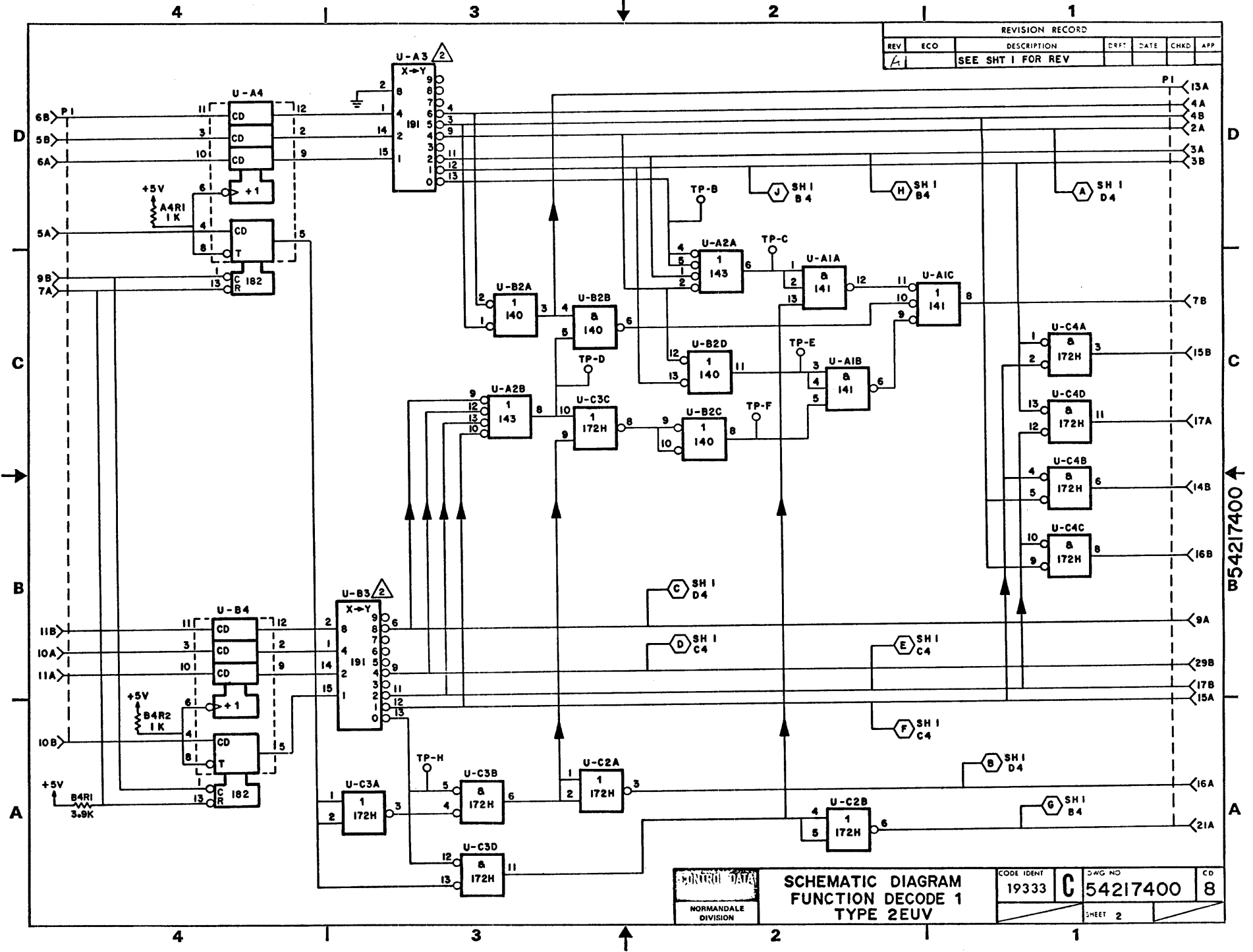
SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	E23000	RELEASED		4-11-72		SK	

NOTE:
 1. ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.

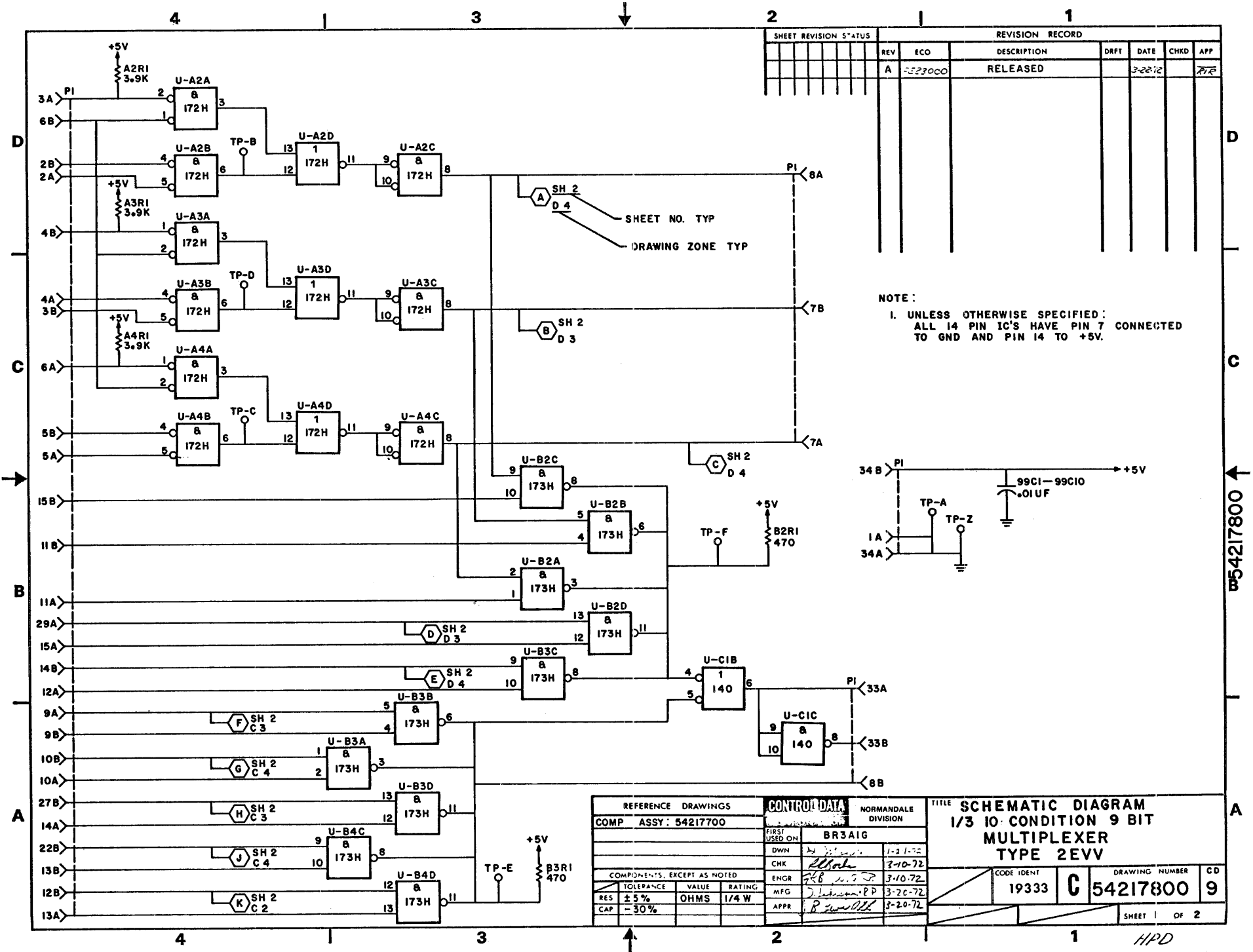
SHEET NO. TYP SH 2 F
 DWG ZONE TYP A 2

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54217300		FIRST USED ON BR 3A1G				SCHEMATIC DIAGRAM FUNCTION DECODE 1 TYPE 2EUV	
COMPONENTS, EXCEPT AS NOTED		DWN R. STREETER 11-31-72				CODE IDENT	
TC. TOLERANCE		ENGR J.P.C. 11-31-72				DRAWING NUMBER	
RES ± 5%		MFG				19333 C 54217400 8	
CAP - 30%		APP				CD	
						SHEET 1 OF 2	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
4		SEE SHT 1 FOR REV				

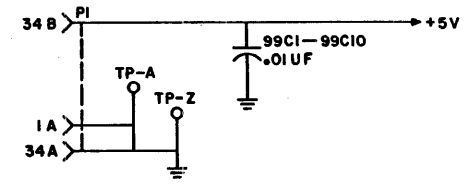


NORMANDE DIVISION	SCHEMATIC DIAGRAM FUNCTION DECODE 1 TYPE 2EUV		CODE IDENT 19333	C	DWG NO 54217400	CD 8



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	223000	RELEASED		3-28-72		PP	

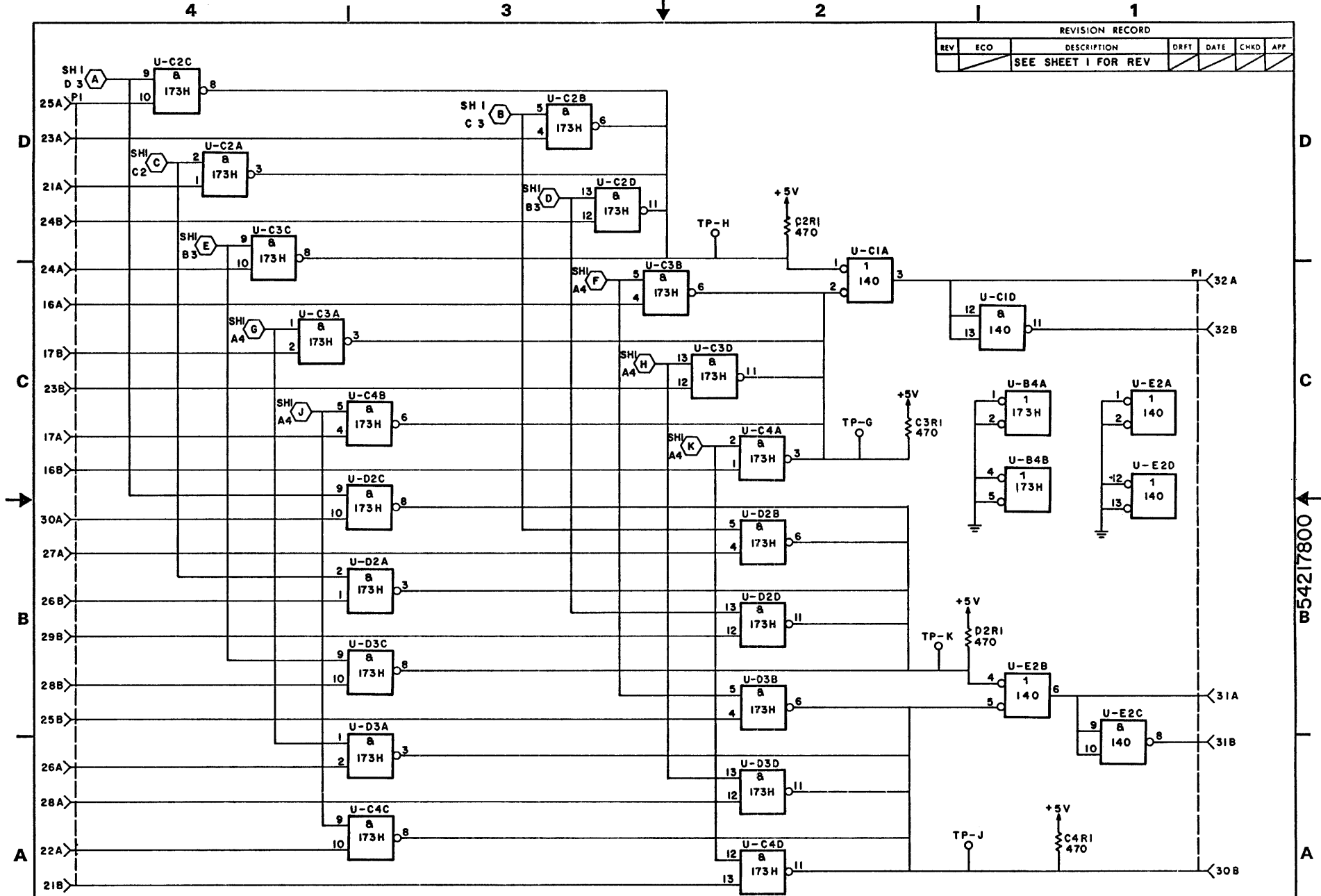
NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED
 TO GND AND PIN 14 TO +5V.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE		
COMP	ASSY: 54217700	FIRST USED ON	BR3A1G			SCHEMATIC DIAGRAM		
		DWN				1/3 10-CONDITION 9 BIT		
		CHK				MULTIPLEXER		
		ENGR				TYPE 2EVV		
		MFG				CODE IDENT	DRAWING NUMBER	CD
		APPR				19333	C 54217800	9
RES	± 5%	OHMS	1/4 W					
CAP	- 30%							
						SHEET 1 OF 2		

HPD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



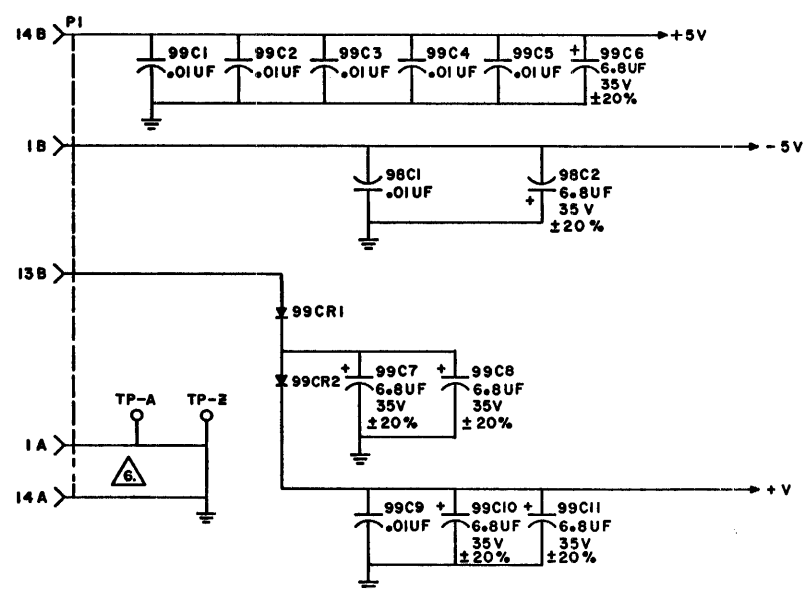
DATE: 10/1/68
 NORMANDE
 DIVISION

**SCHEMATIC DIAGRAM
 MULTIPLEXER
 TYPE 2EVV**

CODE IDENT 19333	C	DWG NO 54217800	CD 9
SHEET 2			

W54217800

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	2300	RELEASED		5-2		1/7	
B	30523	INCREASE YIELD		5-10	DIS		

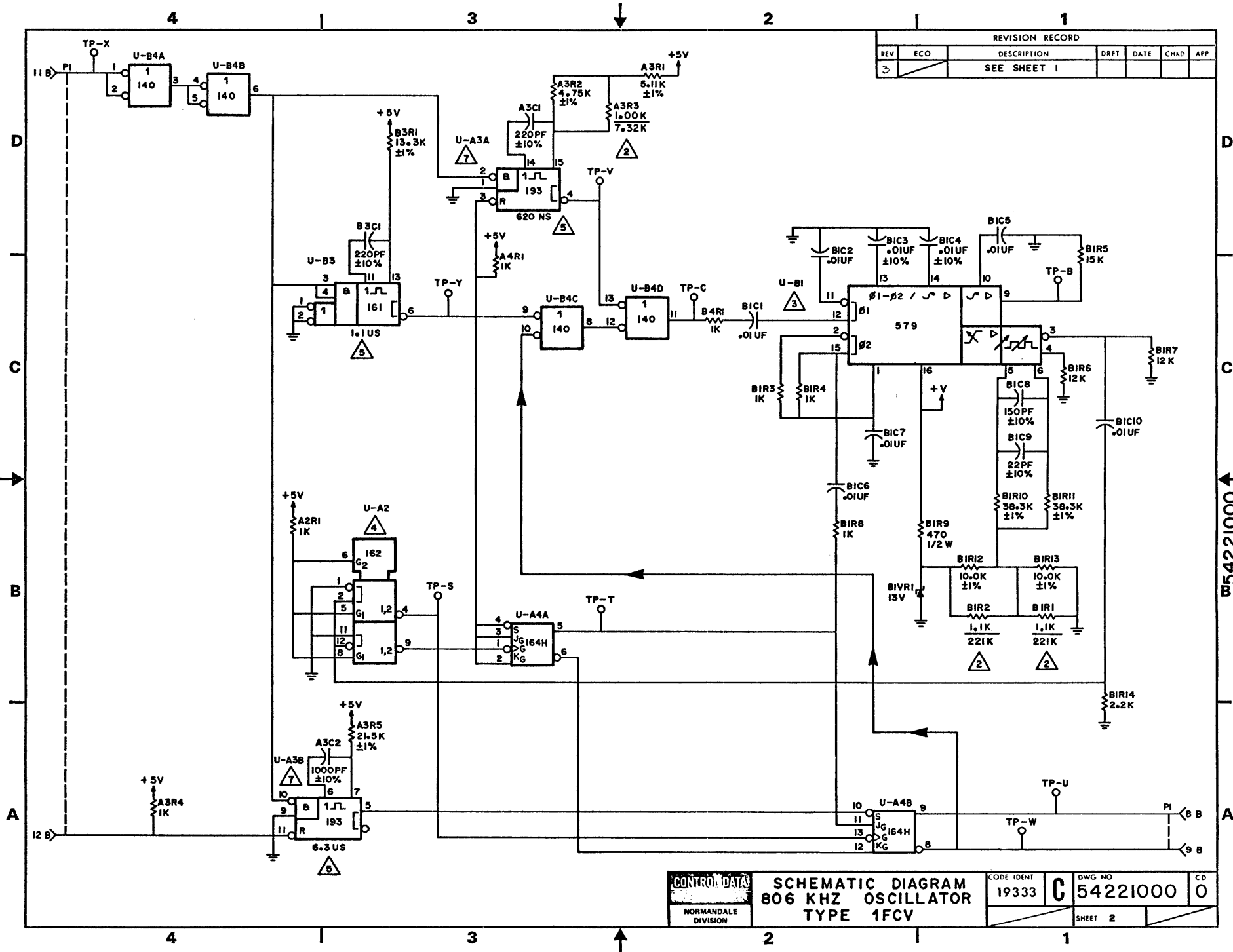


- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL DIODES, SILICON, 24553500
ALL ZENER DIODE VOLTAGE TOL. $\pm 5\%$
ALL 14 PIN IC PACKAGES HAVE PIN 7
CONNECTED TO GND; PIN 14 TO +5V
 - COMPONENT VALUE TO BE SELECTED
PER ENGINEERING TEST PROCEDURE.
 - IC, TYPE 579, HAS PIN 8 CONNECTED TO
GND; PIN 16 TO +V.
 - IC, TYPE 162, HAS PIN 13 CONNECTED TO
-5V.
 - DELAY TIME FOR REFERENCE ONLY.
 - ALL UNUSED PINS ARE GROUNDED.
PIN 2B IS A SPARE.
 - IC, TYPE 193, HAS PIN 8 CONNECTED TO GND;
PIN 16 TO +5V.

REFERENCE DRAWINGS	COMP ASSY : 54220900	FIRST USED ON	BR3A3	NORMANDELE DIVISION	TITLE	SCHEMATIC DIAGRAM
COMPONENTS, EXCEPT AS NOTED				ENGR	CODE IDENT	DRAWING NUMBER
TOLERANCE	VALUE	RATING	MFG	19333	C	54221000
RES $\pm 5\%$	OHMS	1/4 W	APPR			0
CAP -30%						
SHEET 1 OF 2						HPD

54221000

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHAD	APP
3		SEE SHEET 1				

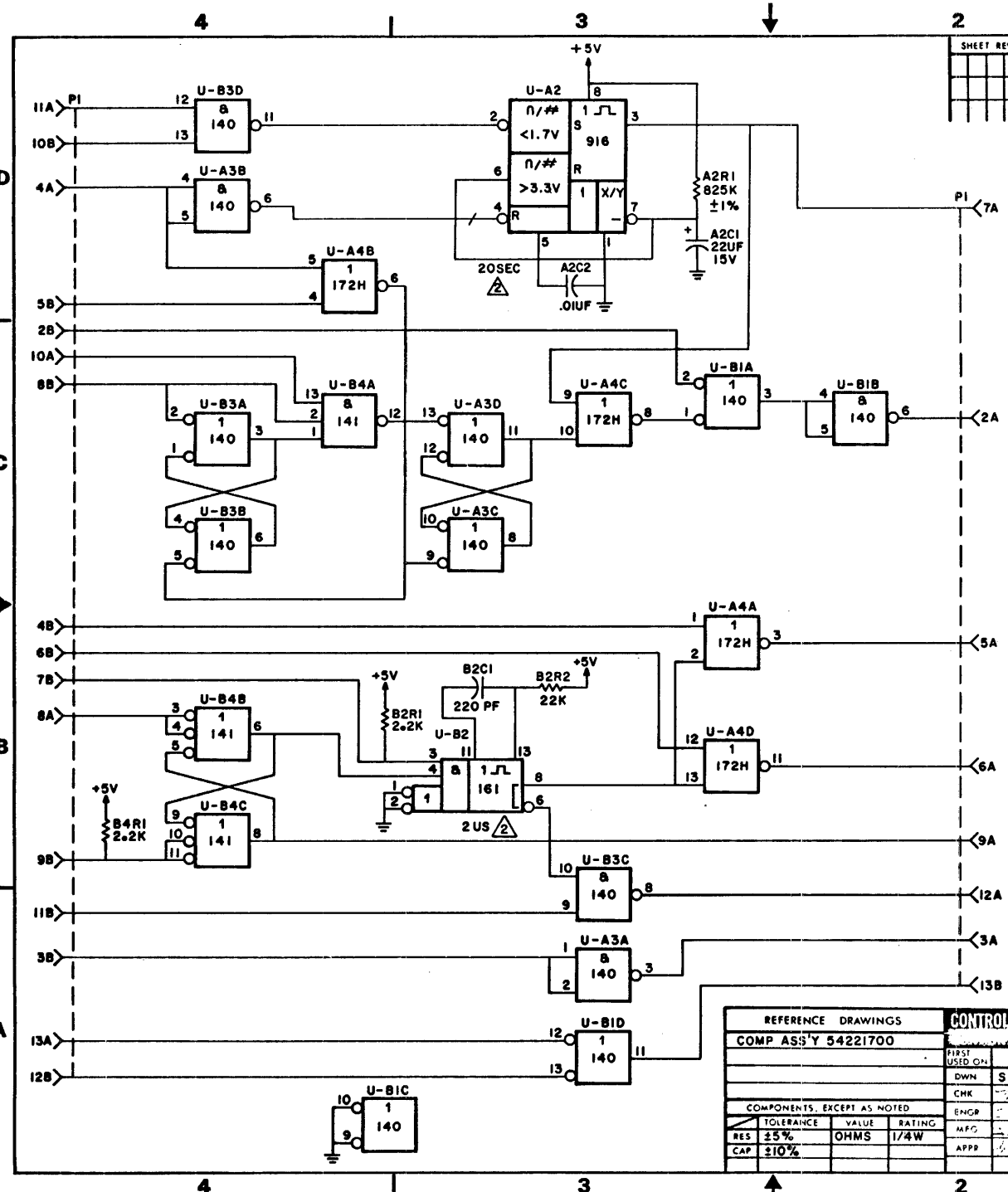


CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
806 KHZ OSCILLATOR
TYPE 1FCV

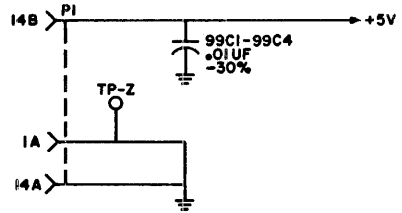
CODE IDENT	DWG NO	CD
19333	54221000	0
SHEET 2		

W54221000



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		RELEASED				
B	PE35028	RESISTOR VALUE CHANGE	RB	2/22/73	16	INR
C	PE35118	CHG 916 ELEMENT SYMBOL	VW	4-24-73	26	II

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ⚠ DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE		
COMP ASS'Y 54221700		FIRST USED ON BR302				SCHEMATIC DIAGRAM		
		DWN S. ZAK		10-23-72		MOTOR ENABLE & ON LINE CLEAR		
		ENGR				TYPE 2FEV		
COMPONENTS, EXCEPT AS NOTED		MFG		11-1-72		CODE IDENT	DRAWING NUMBER	C.D.
TOLERANCE	VALUE	RATING	APPR	11-1-72	19333	C 54221800	3	
RES ±5%	OHMS	1/4W						
CAP ±10%								

D

C

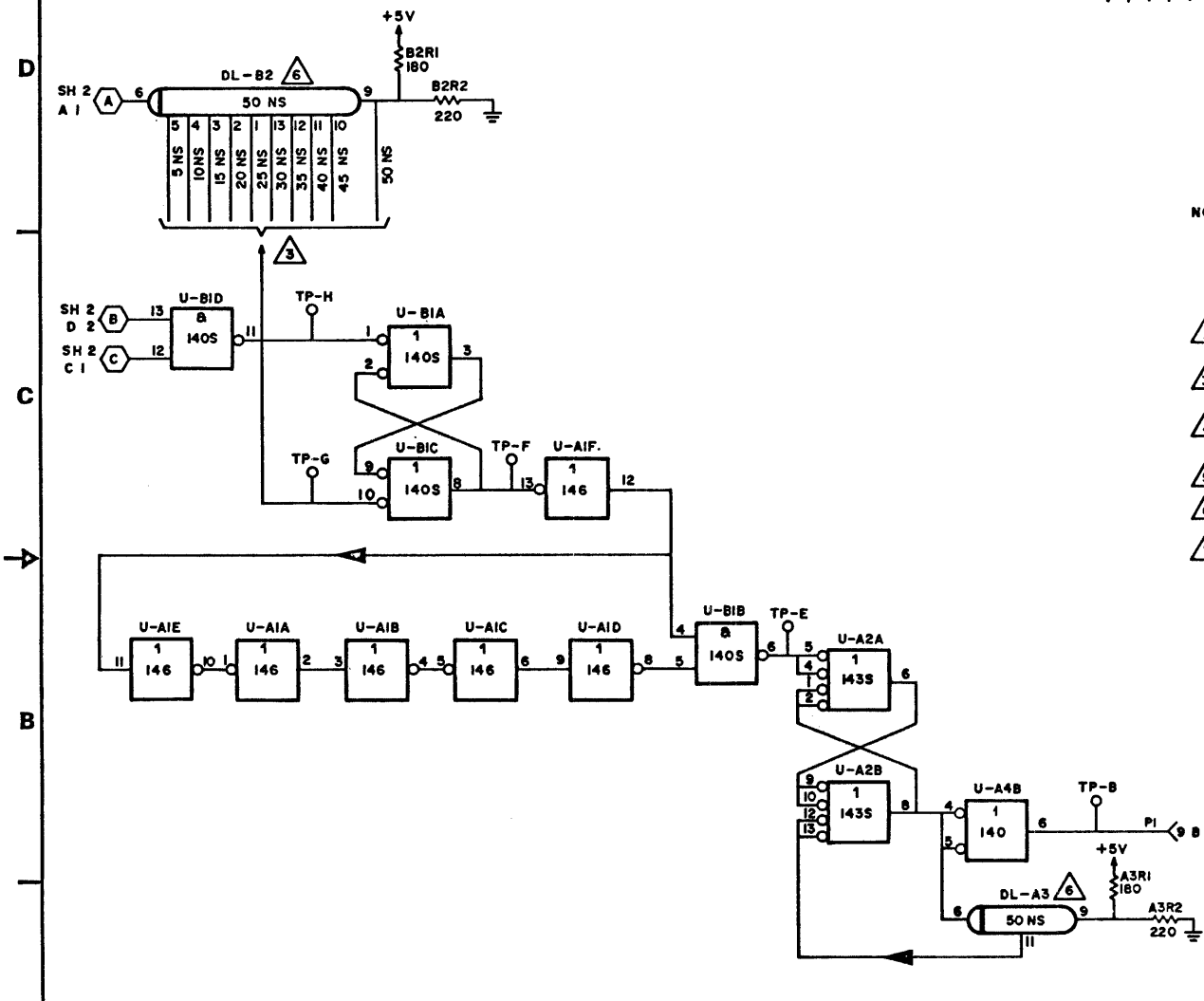
B

A

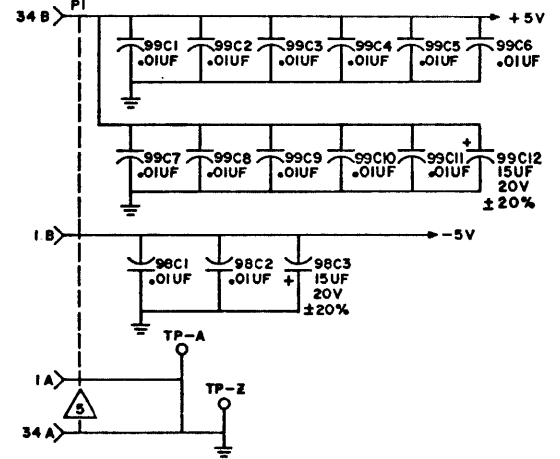
A

54221800

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE23J00	RELEASED		5-11-72			



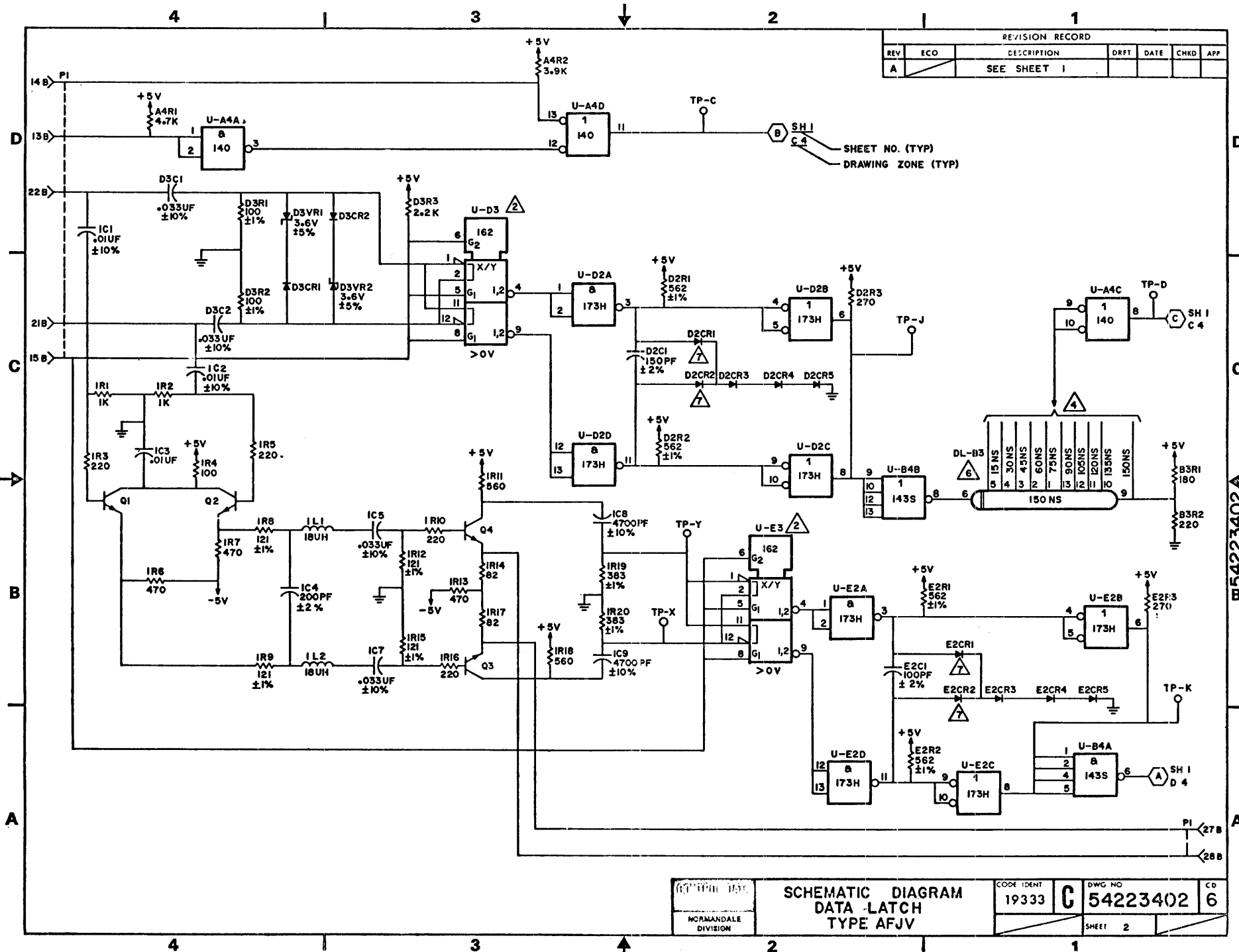
NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ALL TRANSISTORS, SILICON, NPN, 2N3646, 50210310.
 ALL DIODES 24553500.
 2. IC PACKAGES U-D3 AND U-E3 HAVE PIN 13 CONNECTED TO -5V.
 3. DELAY TAPS ARE EVERY 5.00 NS ± 10% DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 4. DELAY TAPS ARE EVERY 15.00 NS ± 10% DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 5. CONNECTOR PINS 1A THRU 34A ARE GROUNDED.
 6. DELAY LINES B2, B3, AND A3 HAVE PINS 7 AND 8 CONNECTED - TO GND.
 7. DIODES, SCHOTKY 50241400.



REFERENCE DRAWINGS				NORMANDALE DIVISION		TITLE	
COMP ASSY 54223302				BR3A1		SCHEMATIC DIAGRAM DATA LATCH TYPE AFJV	
COMPONENTS, EXCEPT AS NOTED				ENGR	5-10-72	CODE IDENT	DRAWING NUMBER
TOLERANCE	VALUE	RATING	CHK	5-10-72	19333	C	54223402
RES ±5%	OHMS	1/4W	APP	5-10-72			6
CAP -30%							
IND ±10%							

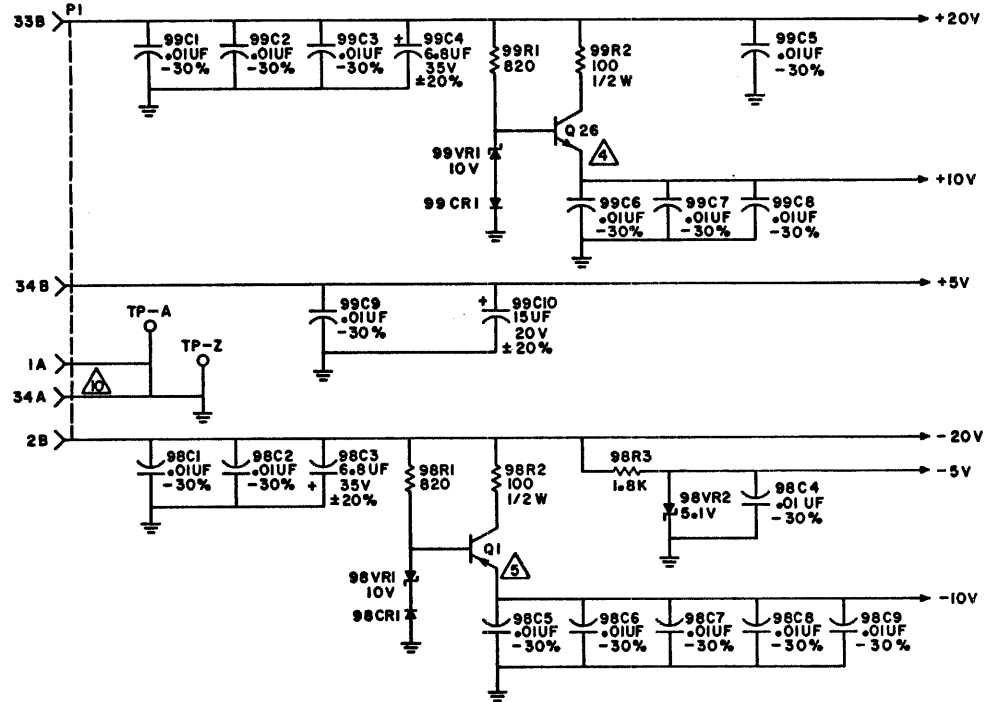
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

SHEET NO. (TYP)
DRAWING ZONE (TYP)



NORMANDEALE DIVISION	SCHEMATIC DIAGRAM DATA LATCH TYPE AFJV	CODE IDENT	DWG NO	CD
		19333	54223402	6
		SHEET 2		

SHEET REVISION STATUS				REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	23-77	RELEASED		2-17-77		RH		



- NOTE:
- UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SPNP, 2N4916, 50211610
 ALL DIODES, SILICON, 92115023
 ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$
- ② TRANSISTOR, SNPN, 2N2221, 50210102.
 - ③ TRANSISTOR, ARRAY, QUAD, CA3018, 50251100.
 - ④ TRANSISTOR, SNPN, 2N3569, 50210811.
 - ⑤ TRANSISTOR, SPNP, 2N3638, 50210610.
 - ⑥ TRANSISTOR, SNPN, 2N3646, 50210310.
 - ⑦ TRANSISTOR, SPNP, 2N4258, 50211510.
 - ⑧ TRANSISTOR, SPNP, 2N5230, 50212200.
 - ⑨ DIODE, SILICON, 92115021.
 - ⑩ PINS 1A THRU 34A ARE CONNECTED TO GND.
 - ⑪ IC, TYPE 308, HAS PIN 7 CONNECTED TO +10V AND PIN 4 CONNECTED TO -10V.
 - ⑫ PIN 10 OF U-12 AND U-14 CONNECTED TO GND.
 - ⑬ PIN 10 OF U-2, U-19 AND U-25 CONNECTED TO -10V.

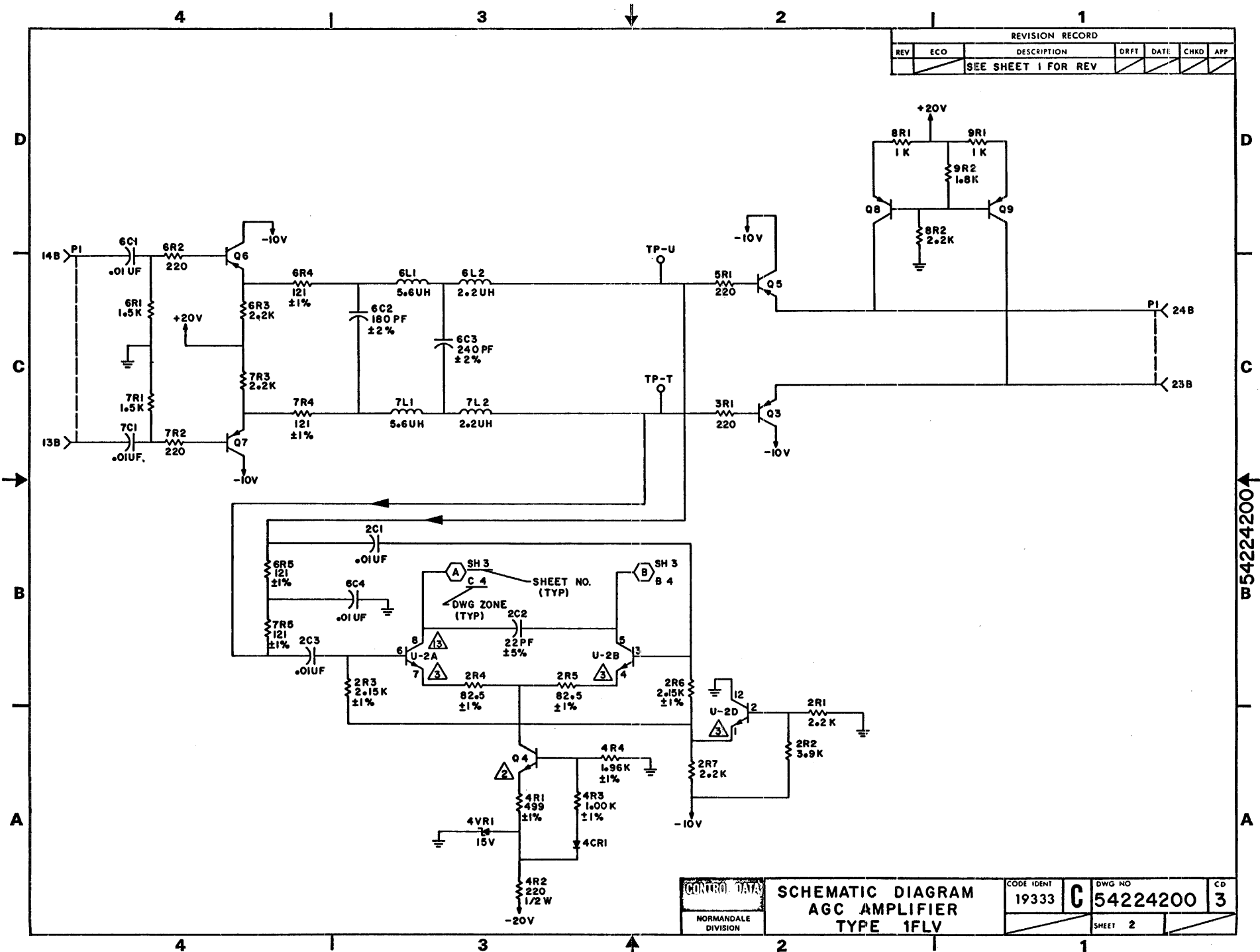
B54224200

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54224100		FIRST USED ON		BR3A1		SCHEMATIC DIAGRAM ACG AMPLIFIER TYPE 1FLV	
COMPONENTS, EXCEPT AS NOTED		CHK		ENGR		CODE IDENT	
TOLERANCE	VALUE	RATING	MFG	APPR	19333	DRAWING NUMBER	CD
RES $\pm 5\%$		OHMS	1/4 W		C	54224200	3
CAP $\pm 10\%$							

SHEET 1 OF 3
HPD

70629100 E

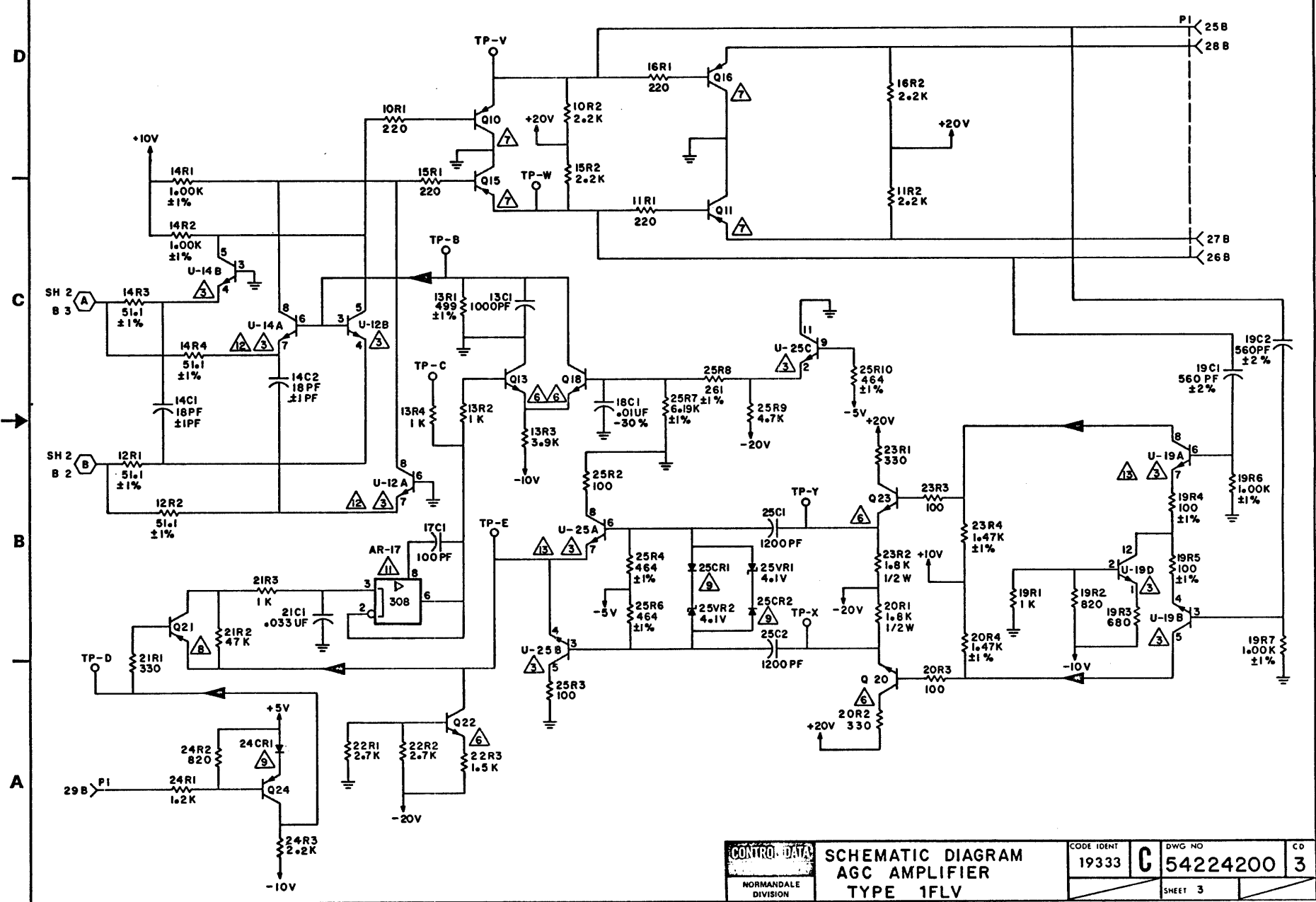
4-77



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
SEE SHEET 1 FOR REV						

CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM AGC AMPLIFIER TYPE 1FLV		CODE IDENT 19333	C	DWG NO 54224200	CD 3
					SHEET 2	

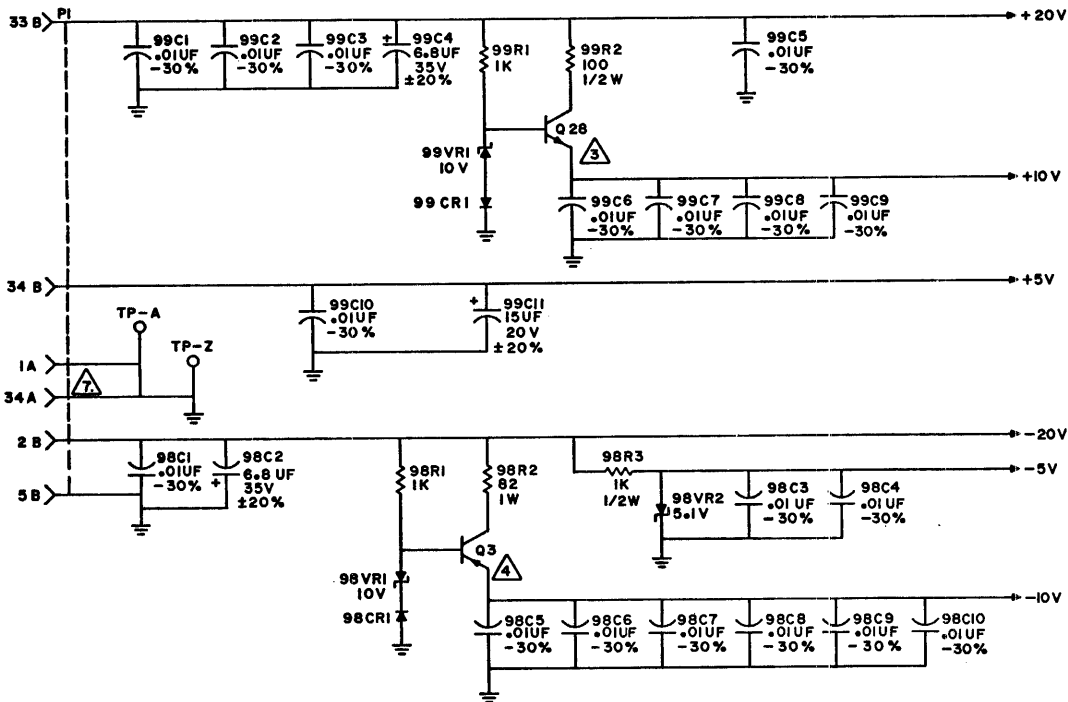
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDELE DIVISION	SCHEMATIC DIAGRAM AGC AMPLIFIER TYPE 1FLV			CODE IDENT 19333	DWG NO C 54224200	CD 3
			SHEET 3			

W54224200

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					



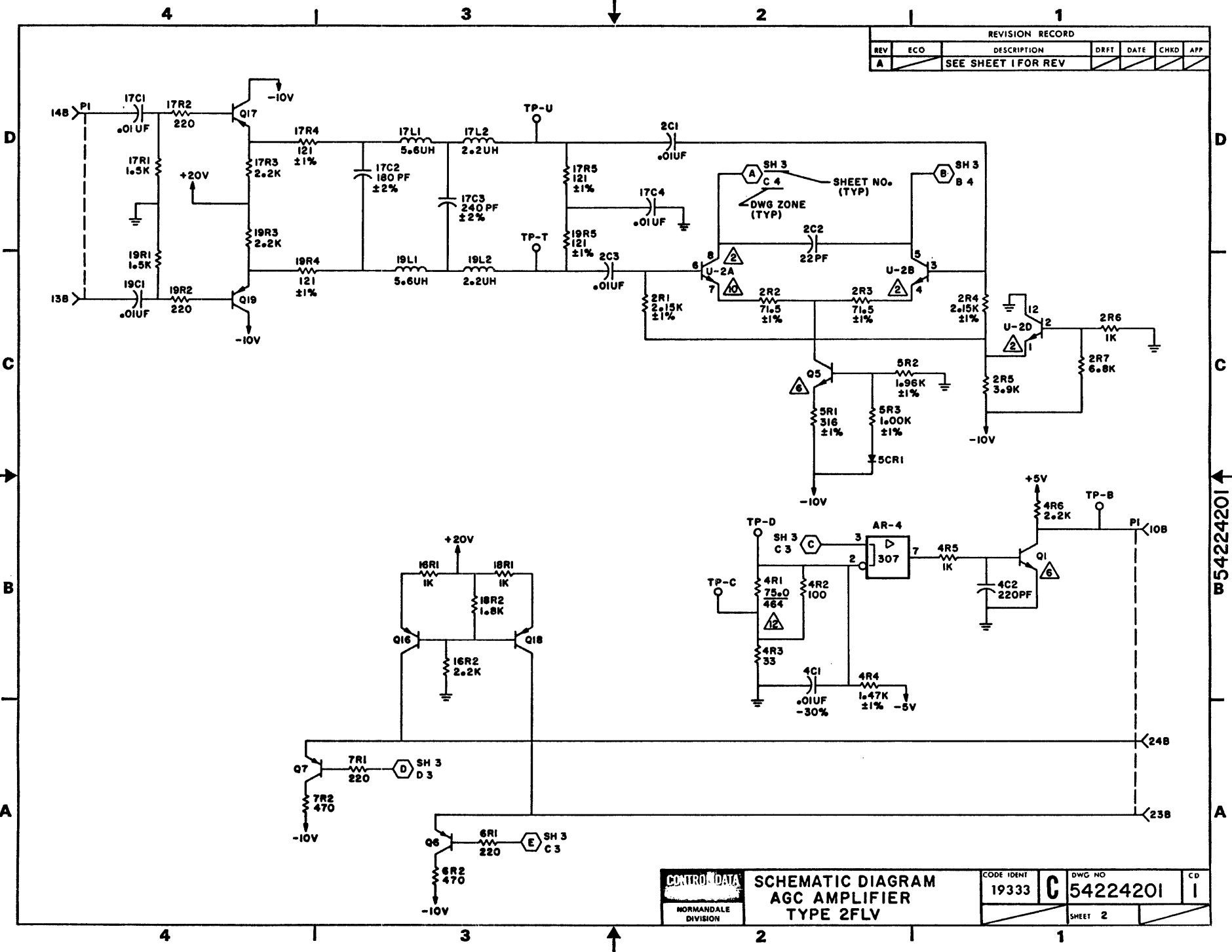
- NOTE:
1. UNLESS OTHERWISE SPECIFIED:
 - ALL TRANSISTORS, SPNP, 2N4916, 50211610.
 - ALL DIODES, SILICON, 24553500.
 - ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$.
 2. TRANSISTOR, ARRAY, QUAD, CA3018, 50251100.
 3. TRANSISTOR, SNPN, 2N3569, 50210811.
 4. TRANSISTOR, SPNP, 2N4919, 50221001.
 5. TRANSISTOR, SPNP, 2N4258, 50211510.
 6. TRANSISTOR, SNPN, 24562100.
 7. PINS 1A THRU 34A ARE CONNECTED TO GND.
 8. IC, TYPE 308, HAS PIN 7 CONNECTED TO +10V AND PIN 4 CONNECTED TO -10V.
 9. PIN 10 OF U-10 AND U-11 CONNECTED TO GND.
 10. PIN 10 OF U-2, U-9 AND U-27 CONNECTED TO -10V.
 11. TRANSISTOR, SPNP, 2N5230, 50212200.
 12. TEST SELECT RESISTOR TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54224101		FIRST USED ON		BR3A6		SCHEMATIC DIAGRAM AGC AMPLIFIER TYPE 2FLV	
		DWN		D. G. TUTTLE		7-20-72	
		CHK		<i>[Signature]</i>		3-14-72	
		ENGR		D. Young		7-9-72	
		MFG		<i>[Signature]</i>		5-12-72	
		APPR					
COMPONENTS, EXCEPT AS NOTED		CODE IDENT		DRAWING NUMBER		C.D.	
TOLERANCE	VALUE	RATING	19333	C	54224201	1	
RES $\pm 5\%$	OHMS	1/4 W					
CAP $\pm 10\%$							
						SHEET 1 OF 3	

4-80

70629100 E

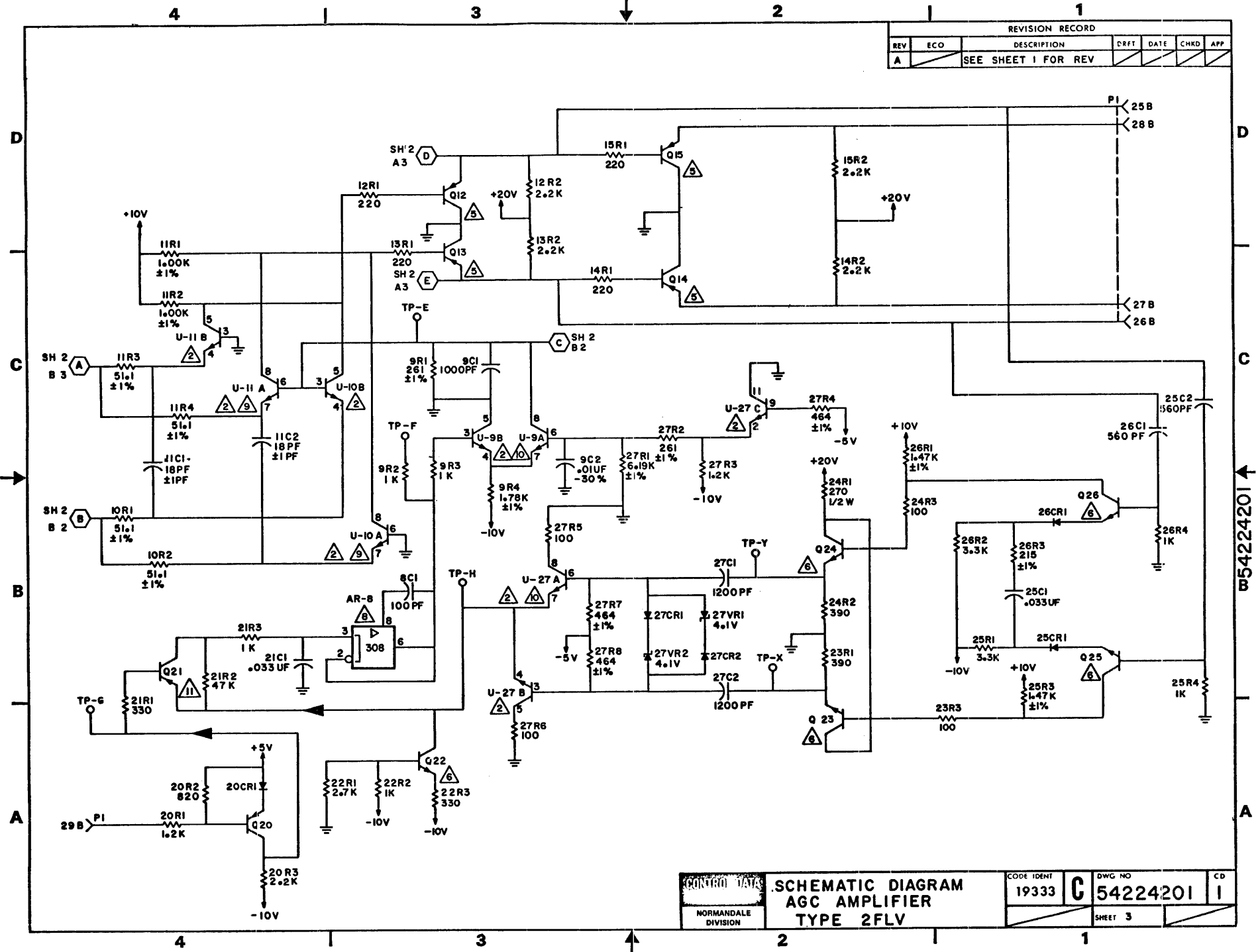
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM AGC AMPLIFIER TYPE 2FLV		CODE IDENT 19333	DWG NO 54224201	CD 1
			SHEET 2		

W 54224201

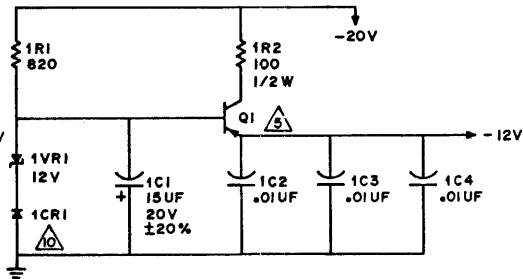
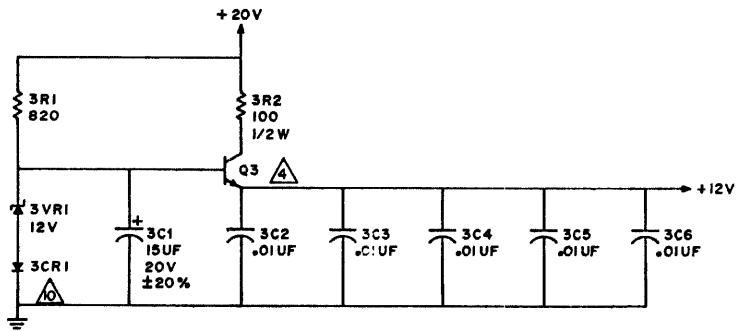
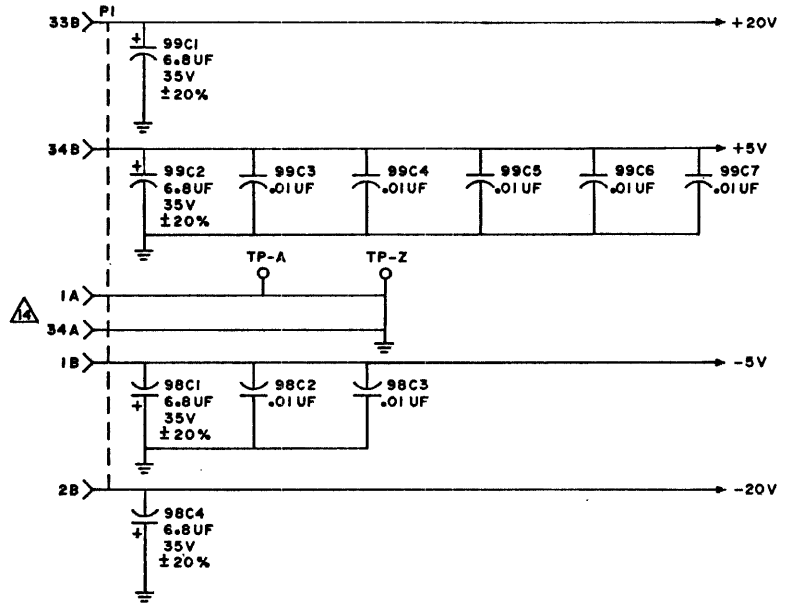
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



SCHMATIC DIAGRAM
AGC AMPLIFIER
TYPE 2FLV

CODE IDENT	DWG NO	CD
19333	C 54224201	1
SHEET 3		

SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PC23000	RELEASED		2-24-72		HPD	

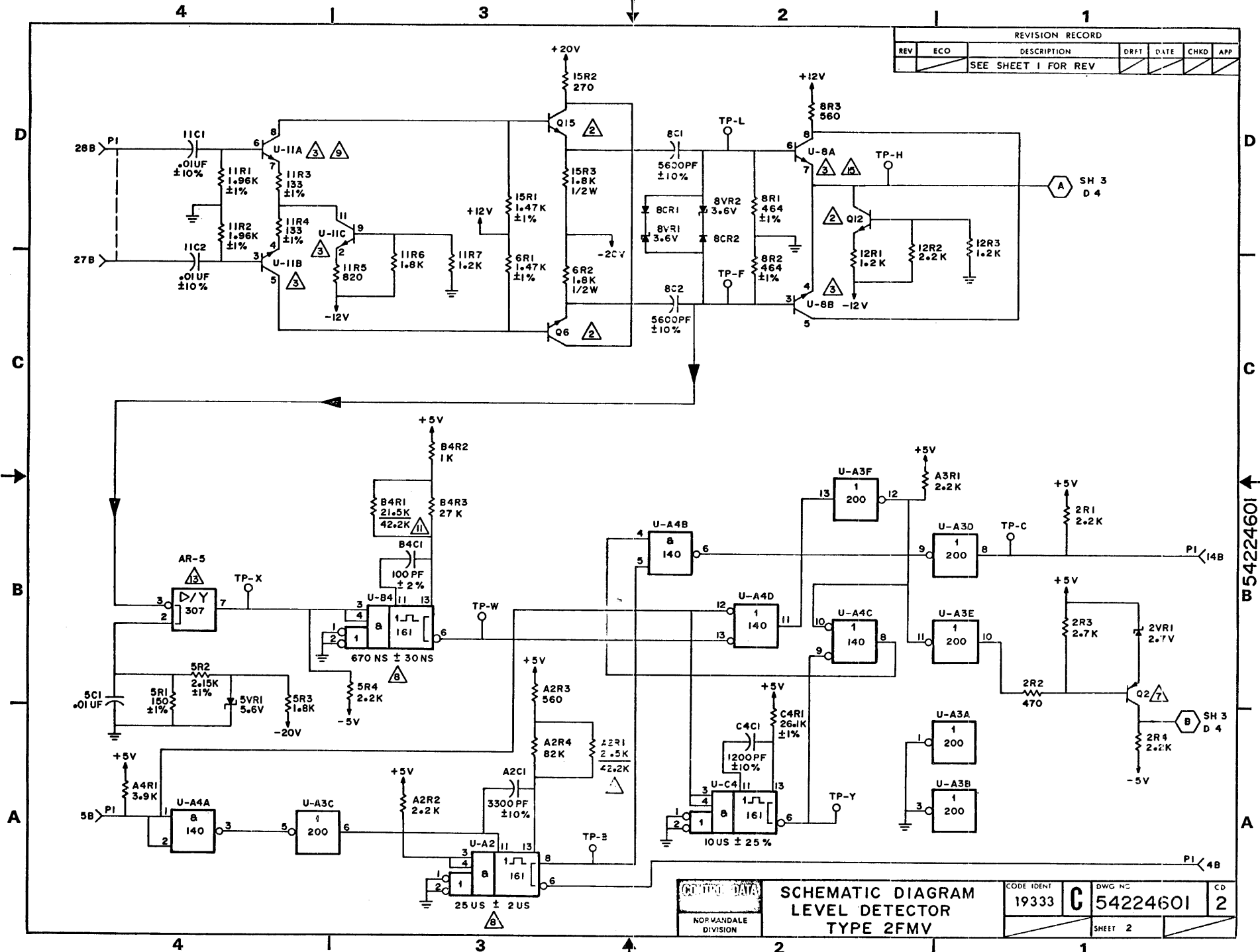


- NOTE:
- UNLESS OTHERWISE SPECIFIED:
 - ALL TRANSISTORS, SNPN, 2N3646, 50210310
 - ALL DIODES, SILICON, 92115021
 - ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$
 - ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V.
 - TRANSISTOR, SNPN, 2N2221, 50210102.
 - TRANSISTOR, CA3018, QUAD, 50251100.
 - TRANSISTOR, SNPN, 2N3569, 50210811.
 - TRANSISTOR, SPNP, 2N3638, 50210610.
 - TRANSISTOR, SPNP, 2N3645, 50211210.
 - TRANSISTOR, SPNP, 2N4916, 50211610.
 - TIME DELAY FOR REFERENCE ONLY.
 - PINS 9 AND 10 OF U-11 ARE INTERCONNECTED.
 - DIODE, SILICON, 92115023.
 - COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 - 8 PIN IC, TYPES 301 AND 308, HAVE PIN 7 CONNECTED TO +12V; PIN 4 TO -12V
 - 8 PIN IC, TYPE 307, HAS PIN 8 CONNECTED TO +12V; PIN 4 TO -5V.
 - CONNECTOR PINS 1A THRU 34A ARE CONNECTED TO GND.
 - PIN 10 OF U-8 IS CONNECTED TO GND.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54224501		BR3A1				SCHEMATIC DIAGRAM	
		FIRST USED ON				LEVEL DETECTOR	
		DWN		R. KONECNY		TYPE 2FMV	
		CHK		J. Hanson			
		ENGR		D. Young			
		MFG		Kiel			
		APPR		J. Hanson			
COMPONENTS, EXCEPT AS NOTED:		TOLERANCE		VALUE		DRAWING	
RES		$\pm 5\%$		OHMS		1/4W	
CAP		-30%					
		CODE IDENT		DRAWING NUMBER		CD	
		19333		C 54224601		2	
				SHEET 1 OF 3		HPD	

70629100 F

4-83



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				

CONTROL DATA NOR MANDALE DIVISION	SCHEMATIC DIAGRAM LEVEL DETECTOR TYPE 2FMV		CODE IDENT 19333	DWG NO C 54224601	CD 2
			SHEET 2		

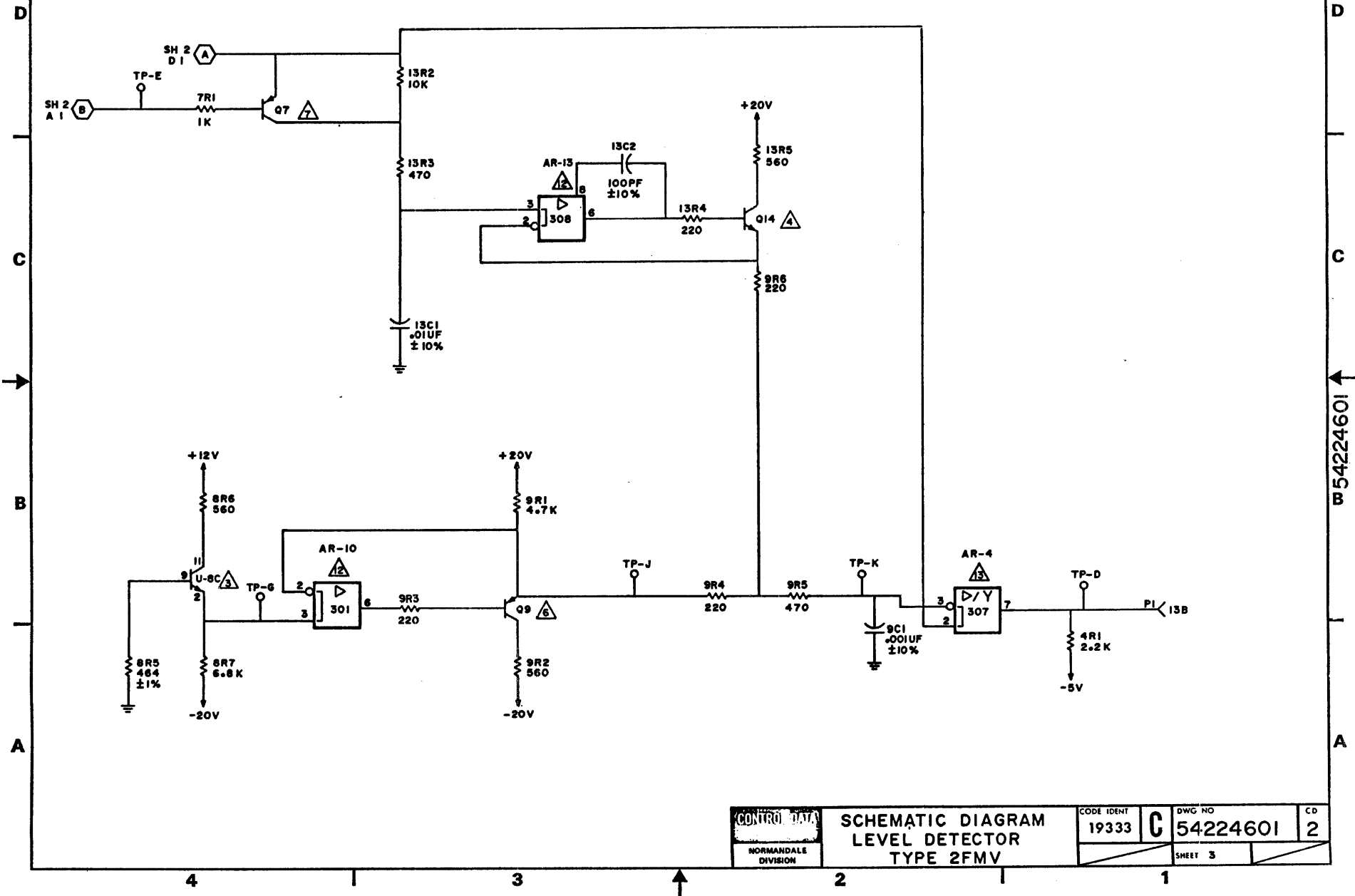
W 54224601

A

4-84

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1 FOR REV				



SCHEMATIC DIAGRAM
LEVEL DETECTOR
TYPE 2FMV

CODE IDENT
 19333

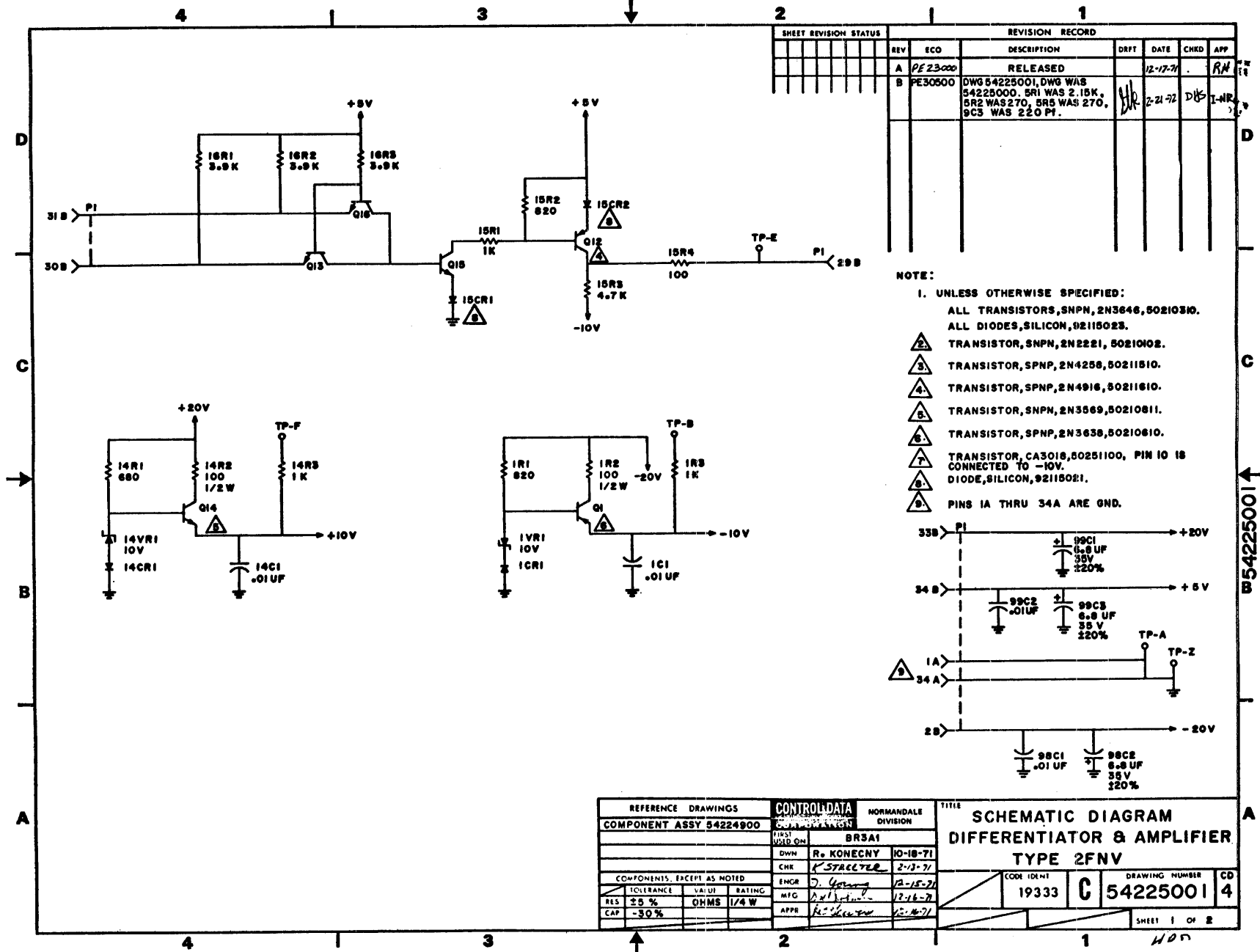
DWG NO
C 54224601

CD
 2

SHEET 3

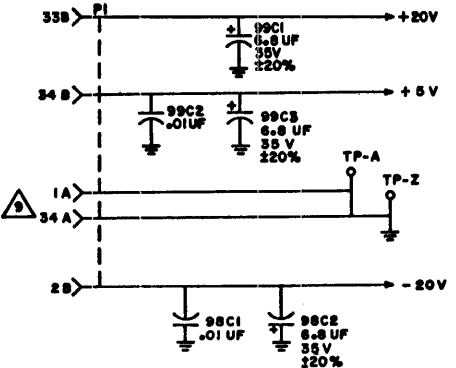
70629100 E

4-85



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED		12-17-71		RM
B	PE30500	DWG 54225001, DWG WAS 54225000. 5R1 WAS 2.15K. 5R2 WAS 270, 5R5 WAS 270, 9C3 WAS 220 PF.		2-21-72	DB	I-NR

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SNPN, 2N3646, 50210310.
ALL DIODES, SILICON, 92115023.
 - TRANSISTOR, SNPN, 2N2221, 50210402.
 - TRANSISTOR, SPNP, 2N4258, 50211510.
 - TRANSISTOR, SPNP, 2N4916, 50211610.
 - TRANSISTOR, SNPN, 2N3569, 50210811.
 - TRANSISTOR, SPNP, 2N3638, 50210610.
 - TRANSISTOR, CA3018, 50251100, PIN 10 IS CONNECTED TO -10V.
 - DIODE, SILICON, 92115021.
 - PINS 1A THRU 34A ARE GND.

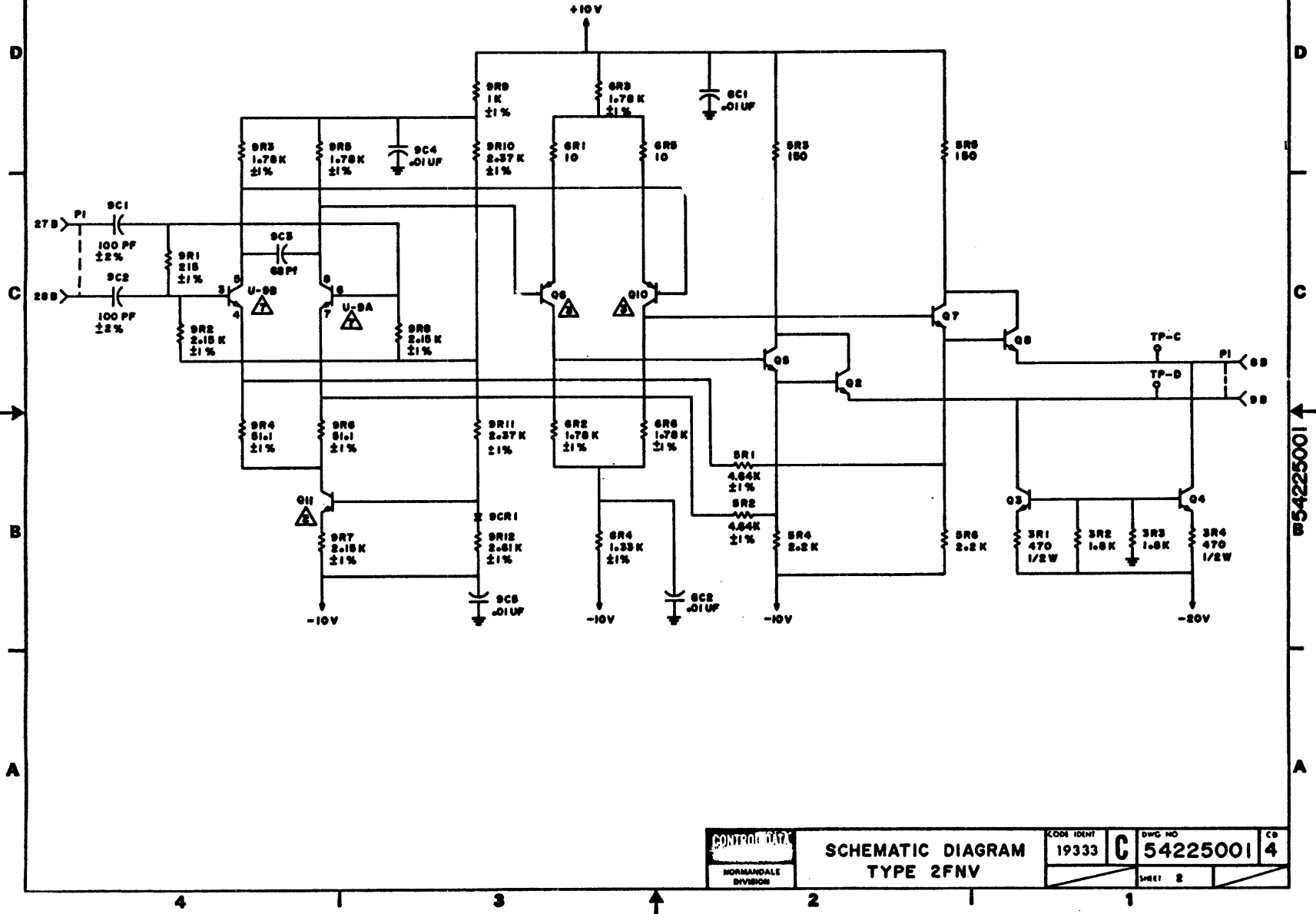


REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54224900		54224900		BR3A1		SCHEMATIC DIAGRAM DIFFERENTIATOR & AMPLIFIER TYPE 2FNV	
COMPONENTS, EXCEPT AS NOTED		DWN R. KONECNY 10-18-71		ENCR K. STREETER 2-13-72		CODE IDENT 19333	
TOLERANCE	VAL US	RATING	MFG	DATE	DRAWING NUMBER	CD	
RES	25%	OHMS	1/4 W	12-18-71	54225001	4	
CAP	-30%			15-11-71			
						SHEET 1 OF 2	

B 54225001 ↑

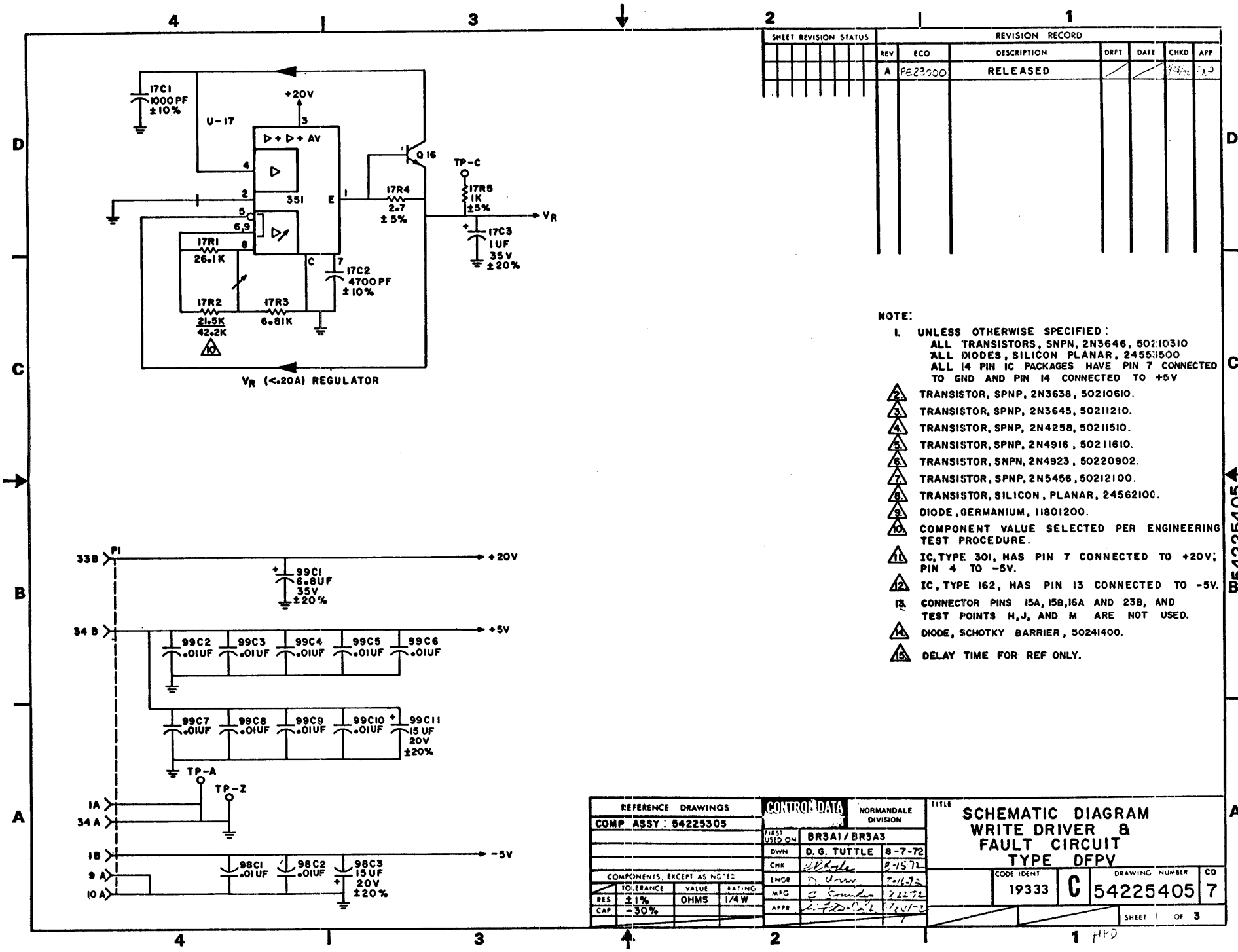
HOD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHNG	APP
		SEE SHEET 1 FOR REV				



CONTROL NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 2FNV		CODE IDENT 19333	DWG NO C 54225001	CD 4
				SHEET 2	

W54225001



SHEET REVISION STATUS					REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	PE23000	RELEASED						

- NOTE:
1. UNLESS OTHERWISE SPECIFIED:
 - ALL TRANSISTORS, SNPN, 2N3646, 50210310
 - ALL DIODES, SILICON PLANAR, 24553500
 - ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 2. TRANSISTOR, SPNP, 2N3638, 50210610.
 3. TRANSISTOR, SPNP, 2N3645, 50211210.
 4. TRANSISTOR, SPNP, 2N4258, 50211510.
 5. TRANSISTOR, SPNP, 2N4916, 50211610.
 6. TRANSISTOR, SNPN, 2N4923, 50220902.
 7. TRANSISTOR, SPNP, 2N5456, 50212100.
 8. TRANSISTOR, SILICON, PLANAR, 24562100.
 9. DIODE, GERMANIUM, 11801200.
 10. COMPONENT VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
 11. IC, TYPE 301, HAS PIN 7 CONNECTED TO +20V; PIN 4 TO -5V.
 12. IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.
 13. CONNECTOR PINS 15A, 15B, 16A AND 23B, AND TEST POINTS H, J, AND M ARE NOT USED.
 14. DIODE, SCHOTKY BARRIER, 50241400.
 15. DELAY TIME FOR REF ONLY.

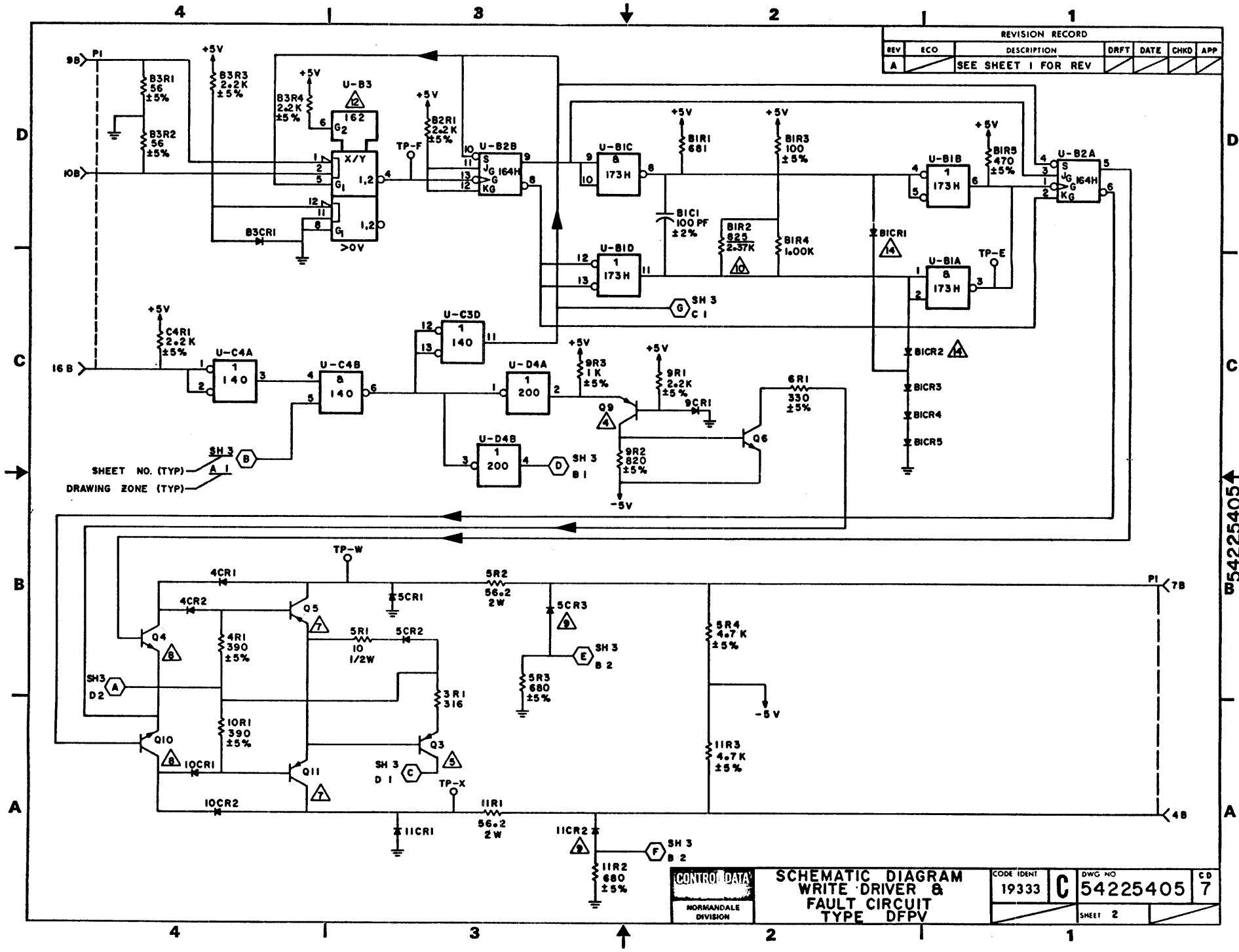
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54225305		FIRST USED ON	BR3A1/BR3A3		SCHEMATIC DIAGRAM		
		DWN	D. G. TUTTLE 8-7-72		WRITE DRIVER & FAULT CIRCUIT		
		CHK	D. Tuttle 8-15-72		TYPE DFV		
		ENGR	D. Tuttle 8-16-72		CODE IDENT	DRAWING NUMBER	CD
		MFG	C. Tuttle 7-22-72		19333	C 54225405	7
		APPR	D. Tuttle 8-15-72				
COMPONENTS, EXCEPT AS NOTED:							
RES	TOLERANCE	VALUE	RATING				
	±1%	OHMS	1/4 W				
CAP	-30%						

B54225405↑

1 HFD

SHEET 1 OF 3

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



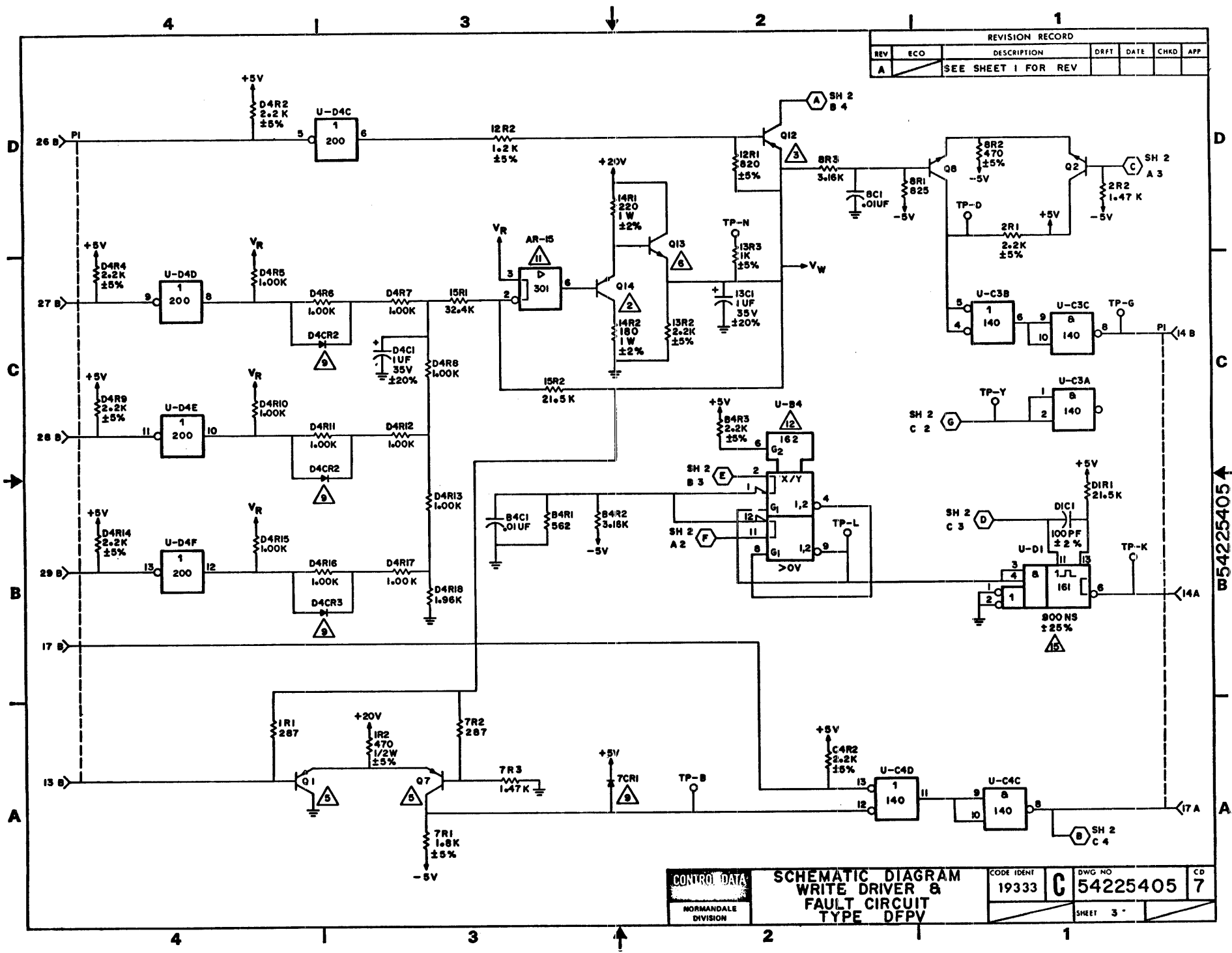
SHEET NO. (TYP) A 1
DRAWING ZONE (TYP)

CONTROL DATA
NORMANDALE
DIVISION

SCHEMATIC DIAGRAM
WRITE DRIVER &
FAULT CIRCUIT
TYPE DFPV

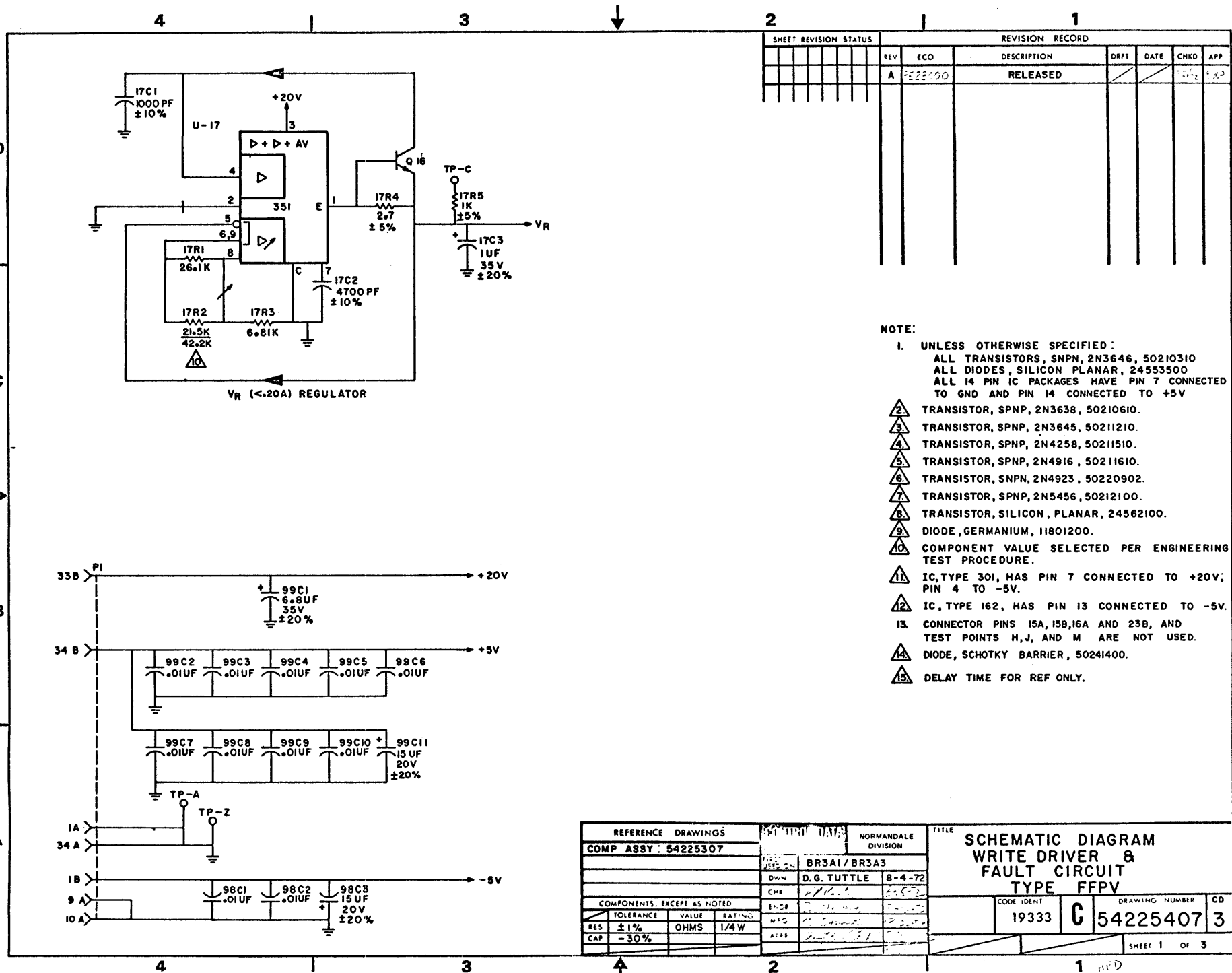
CODE IDENT 19333	DWG NO 54225405	CD 7
SHEET 2		

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE DFPV		CODE IDENT 19333	DWG NO 54225405	CD 7
			SHEET 3	C 4	

W54225405



SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	1933100	RELEASED							

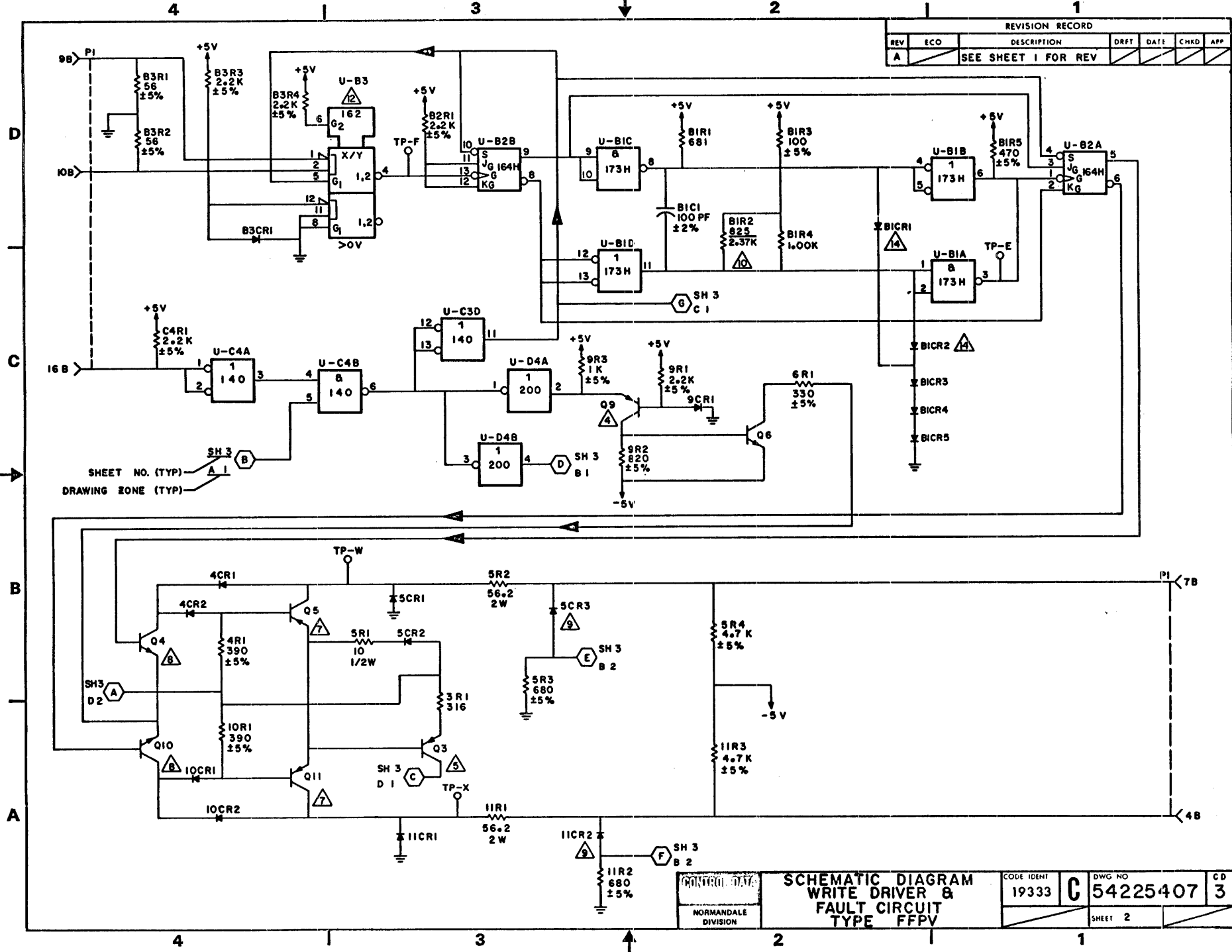
- NOTE:
- UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N3646, 50210310
 ALL DIODES, SILICON PLANAR, 24553500
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 - TRANSISTOR, SNPN, 2N3638, 50210610.
 - TRANSISTOR, SNPN, 2N3645, 50211210.
 - TRANSISTOR, SNPN, 2N4258, 50211510.
 - TRANSISTOR, SNPN, 2N4916, 50211610.
 - TRANSISTOR, SNPN, 2N4923, 50220902.
 - TRANSISTOR, SNPN, 2N5456, 50212100.
 - TRANSISTOR, SILICON, PLANAR, 24562100.
 - DIODE, GERMANIUM, 11801200.
 - COMPONENT VALUE SELECTED PER ENGINEERING TEST PROCEDURE.
 - IC, TYPE 301, HAS PIN 7 CONNECTED TO +20V; PIN 4 TO -5V.
 - IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.
 - CONNECTOR PINS 15A, 15B, 16A AND 23B, AND TEST POINTS H, J, AND M ARE NOT USED.
 - DIODE, SCHOTKY BARRIER, 50241400.
 - DELAY TIME FOR REF ONLY.

REFERENCE DRAWINGS		NORMANDALE DIVISION		TITLE	
COMP ASSY : 54225307		BR3A1 / BR3A3		SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE FFPV	
COMPONENTS, EXCEPT AS NOTED		DWN D.G. TUTTLE 8-4-72		CODE IDENT DRAWING NUMBER CD	
TOLERANCE VALUE RATING		MFG		19333 C 54225407 3	
RES	± 1%	OHMS	1/4W		
CAP	-30%			SHEET 1 OF 3	

70629100 E

4-91

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

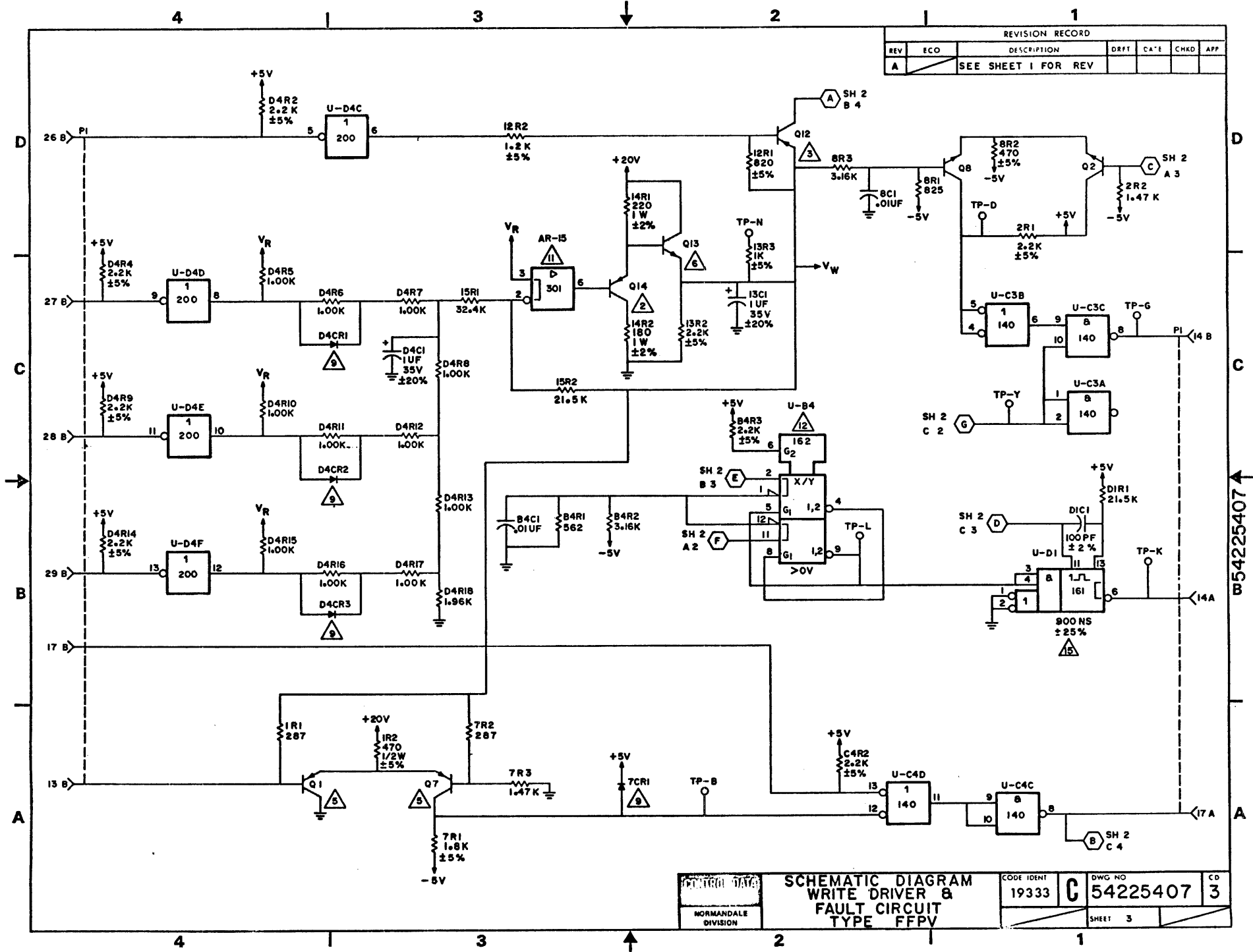


SHEET NO. (TYP) A 1
DRAWING ZONE (TYP) A 1

NORMANDEALE DIVISION	SCHEMATIC DIAGRAM WRITE DRIVER & FAULT CIRCUIT TYPE FFPV		CODE IDENT 19333	DWG NO 54225407	CD 3
			SHEET 2		

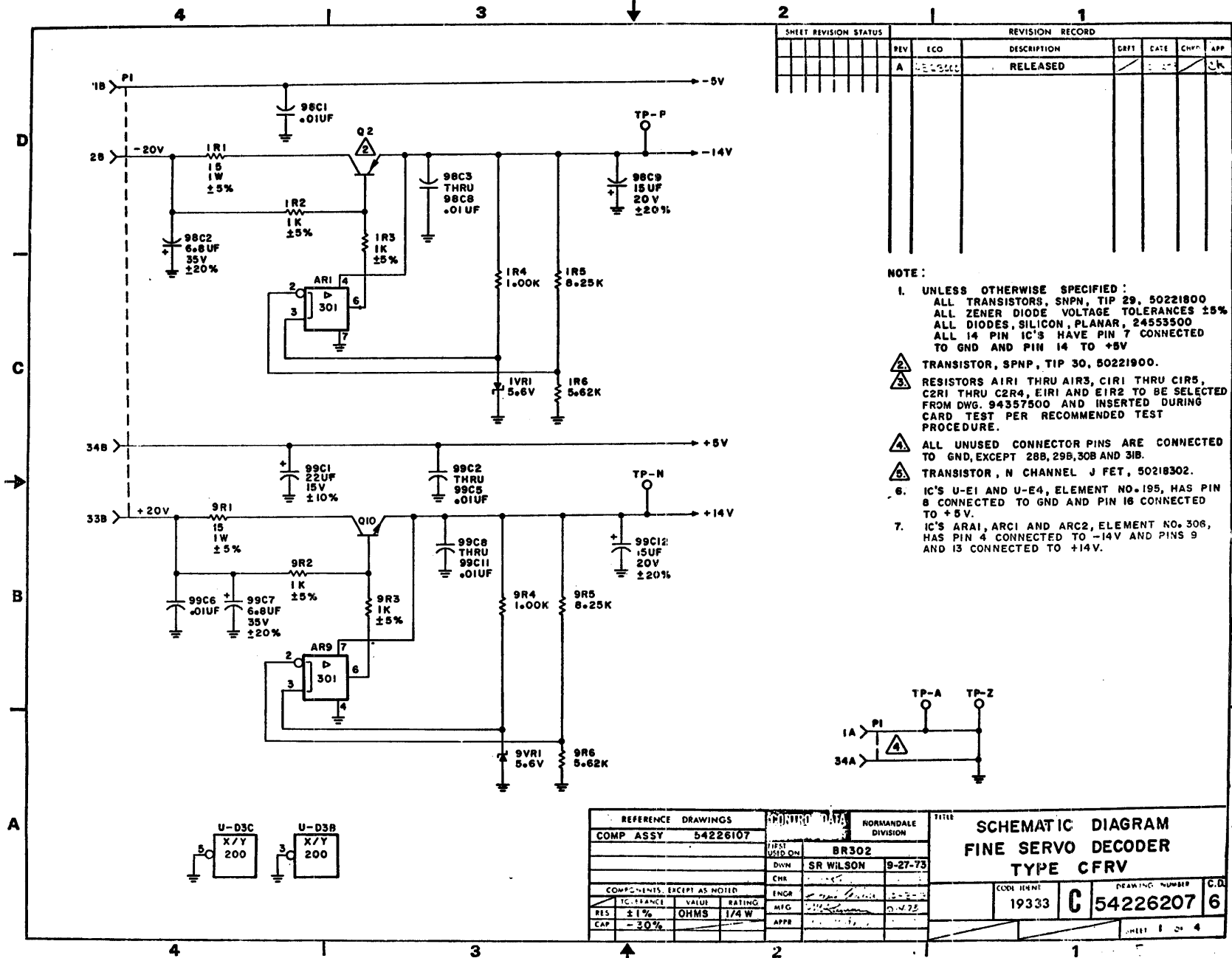
54225407

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	CA'E	CHKD	APP
A		SEE SHEET 1 FOR REV				



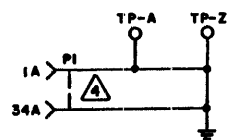
CONTROL DATA	Schematic Diagram				CODE IDENT	CD
	WRITE DRIVER & FAULT CIRCUIT TYPE FFPV				19333	3
NORMANDALE DIVISION					DWG NO	
					54225407	
					SHEET 3	

B54225407



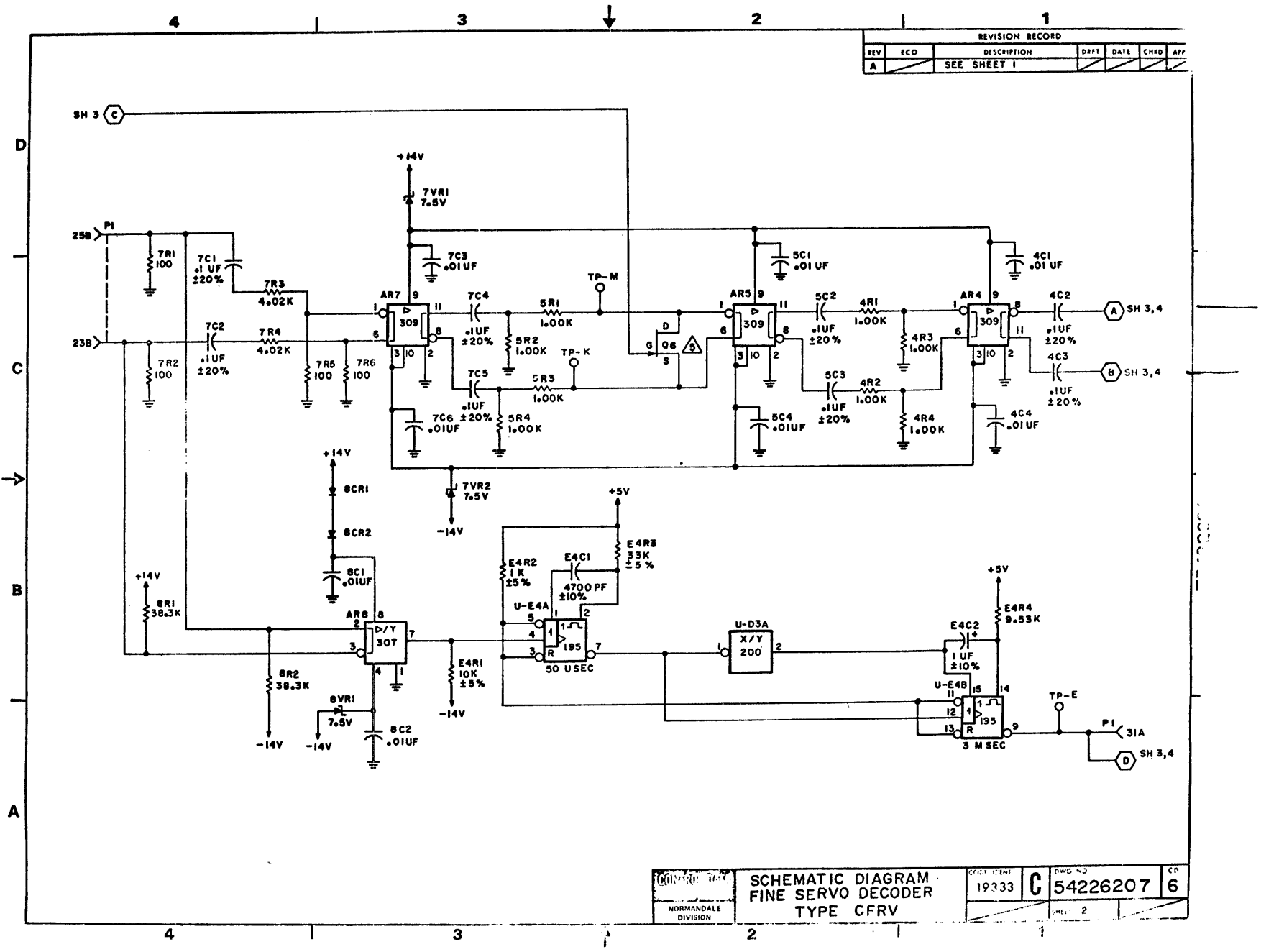
SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	02/03/00	RELEASED				CK	

- NOTE:
- UNLESS OTHERWISE SPECIFIED :
 ALL TRANSISTORS, SiPNP, TIP 29, 50221800
 ALL ZENER DIODE VOLTAGE TOLERANCES 15%
 ALL DIODES, SILICON, PLANAR, 24553500
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V
 - TRANSISTOR, SiPNP, TIP 30, 50221900.
 - RESISTORS AIR1 THRU AIR3, CIR1 THRU CIR5, C2R1 THRU C2R4, EIR1 AND EIR2 TO BE SELECTED FROM DWG 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
 - ALL UNUSED CONNECTOR PINS ARE CONNECTED TO GND, EXCEPT 28B, 29B, 30B AND 31B.
 - TRANSISTOR, N CHANNEL J FET, 50218302.
 - IC'S U-E1 AND U-E4, ELEMENT NO. 195, HAS PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 - IC'S AR1, ARCI AND ARC2, ELEMENT NO. 306, HAS PIN 4 CONNECTED TO -14V AND PINS 9 AND 13 CONNECTED TO +14V.



REFERENCE DRAWINGS	54226107	NORMANDEALE DIVISION	TITLE	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE CFRV		
COMP ASSY	54226107	BR302	19333	C	54226207	6
COMPONENTS, EXCEPT AS NOTED		9-27-73				
TC TOLERANCE	±1%	OHMS	174 W			
RES	±1%					
CAP	-30%					

054226207 A

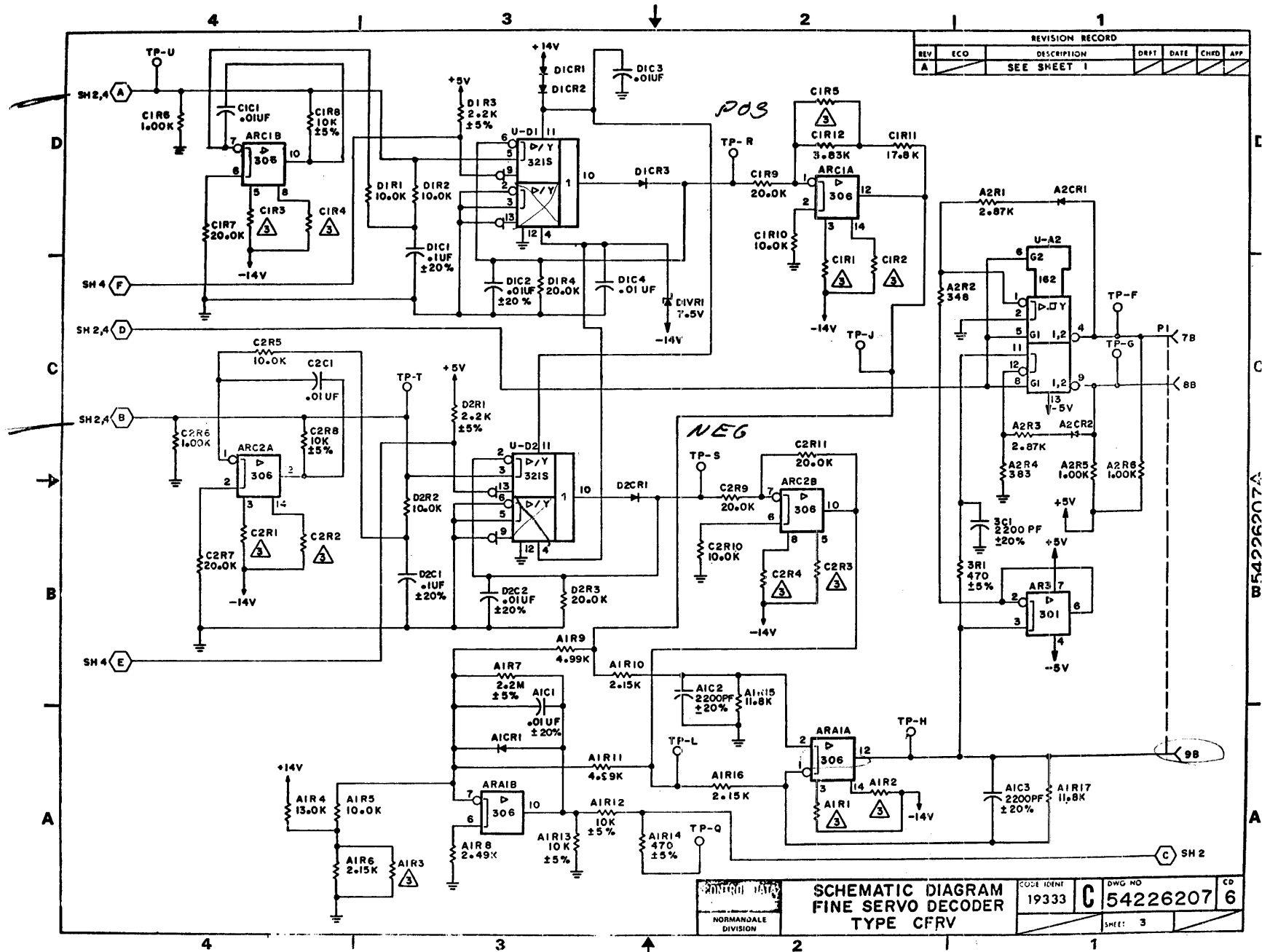


REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				

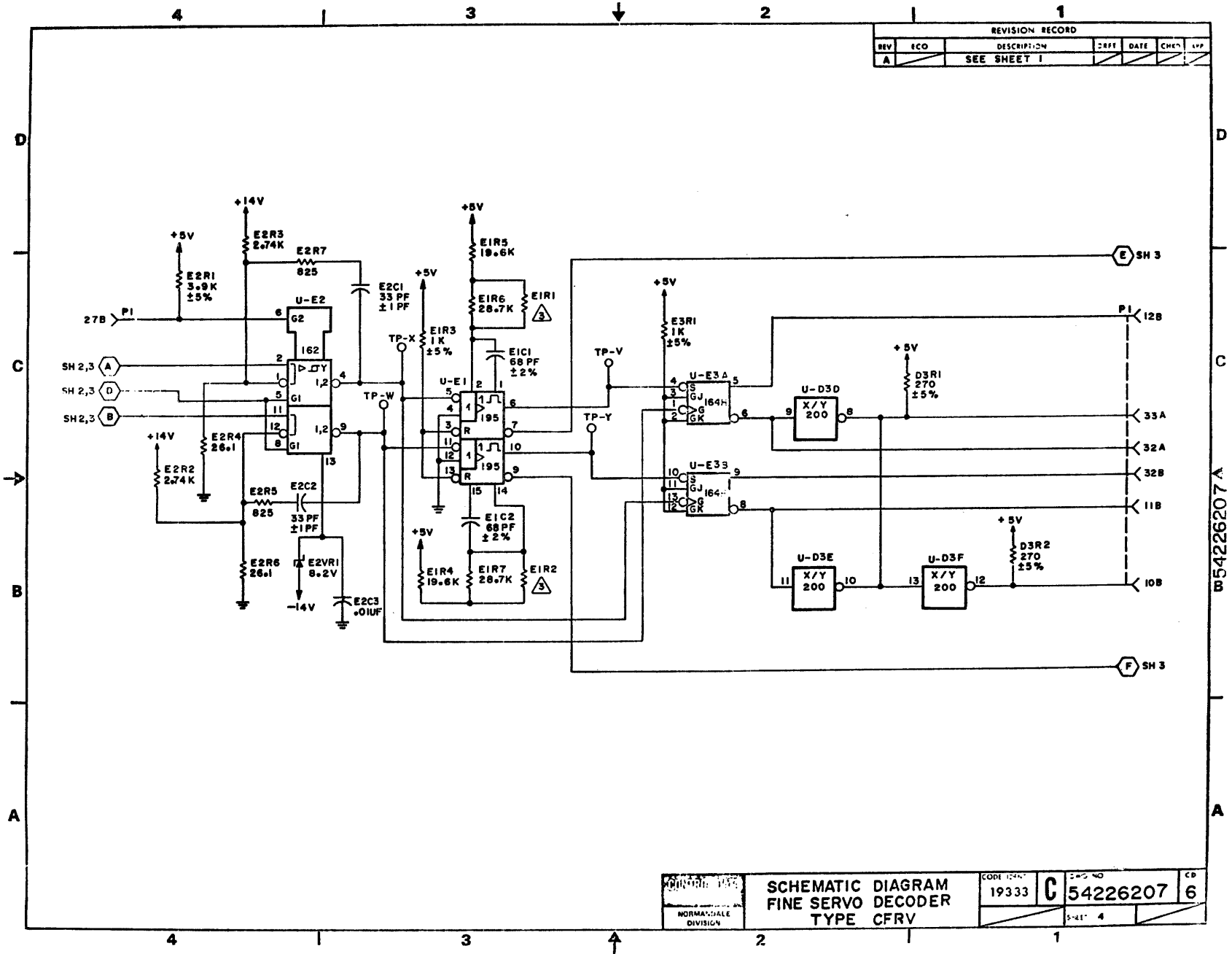
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE GFRV	CONT. IDENT.	DWG. NO.	CP.
		19333	C 54226207	6
		SHEET 2		

70629100 F

4-92.3



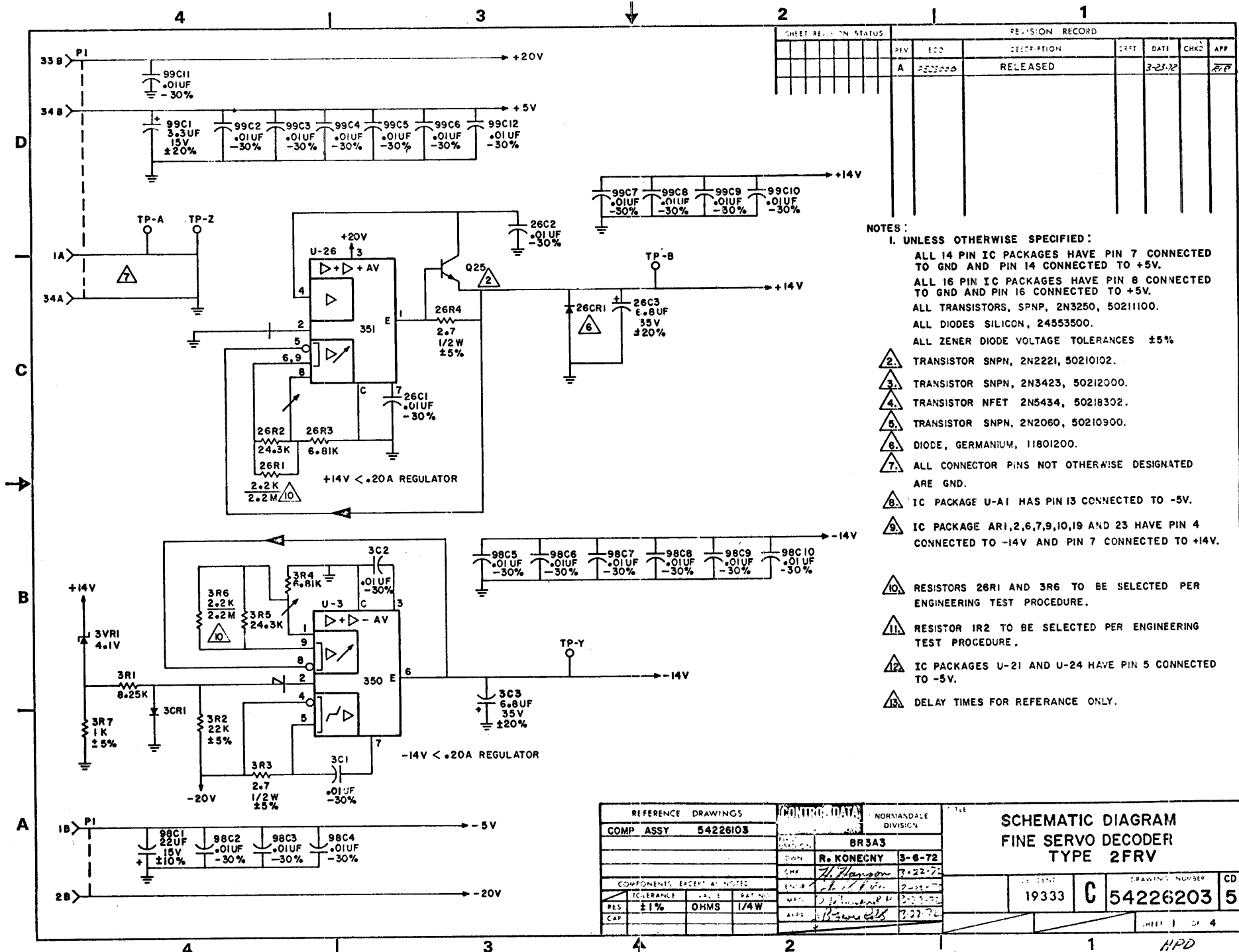
B54226207A



REVISION RECORD						
REV	ECO	DESCRIPTION	DIFF	DATE	CHKD	APP
A		SEE SHEET 1				

NORMAL DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE CFRV		CODE 19333	C	DRAWING NO 54226207	CD 6
				19333	4	

B54226207A



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DATE	CHKD	APP		
A	2023-0-0	RELEASED	3-23-72				

- NOTES:
1. UNLESS OTHERWISE SPECIFIED:
 - ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 - ALL TRANSISTORS, SPNP, 2N3250, 50211100.
 - ALL DIODES SILICON, 24553500.
 - ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$.
 2. TRANSISTOR SNPN, 2N2221, 50210102.
 3. TRANSISTOR SNPN, 2N3423, 50212000.
 4. TRANSISTOR NFET 2N5434, 50218302.
 5. TRANSISTOR SNPN, 2N2060, 50210900.
 6. DIODE, GERMANIUM, 1180200.
 7. ALL CONNECTOR PINS NOT OTHERWISE DESIGNATED ARE GND.
 8. IC PACKAGE U-A1 HAS PIN 13 CONNECTED TO -5V.
 9. IC PACKAGE ARI, 2, 6, 7, 9, 10, 19 AND 23 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
 10. RESISTORS 26R1 AND 3R6 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 11. RESISTOR 1R2 TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 12. IC PACKAGES U-21 AND U-24 HAVE PIN 5 CONNECTED TO -5V.
 13. DELAY TIMES FOR REFERENCE ONLY.

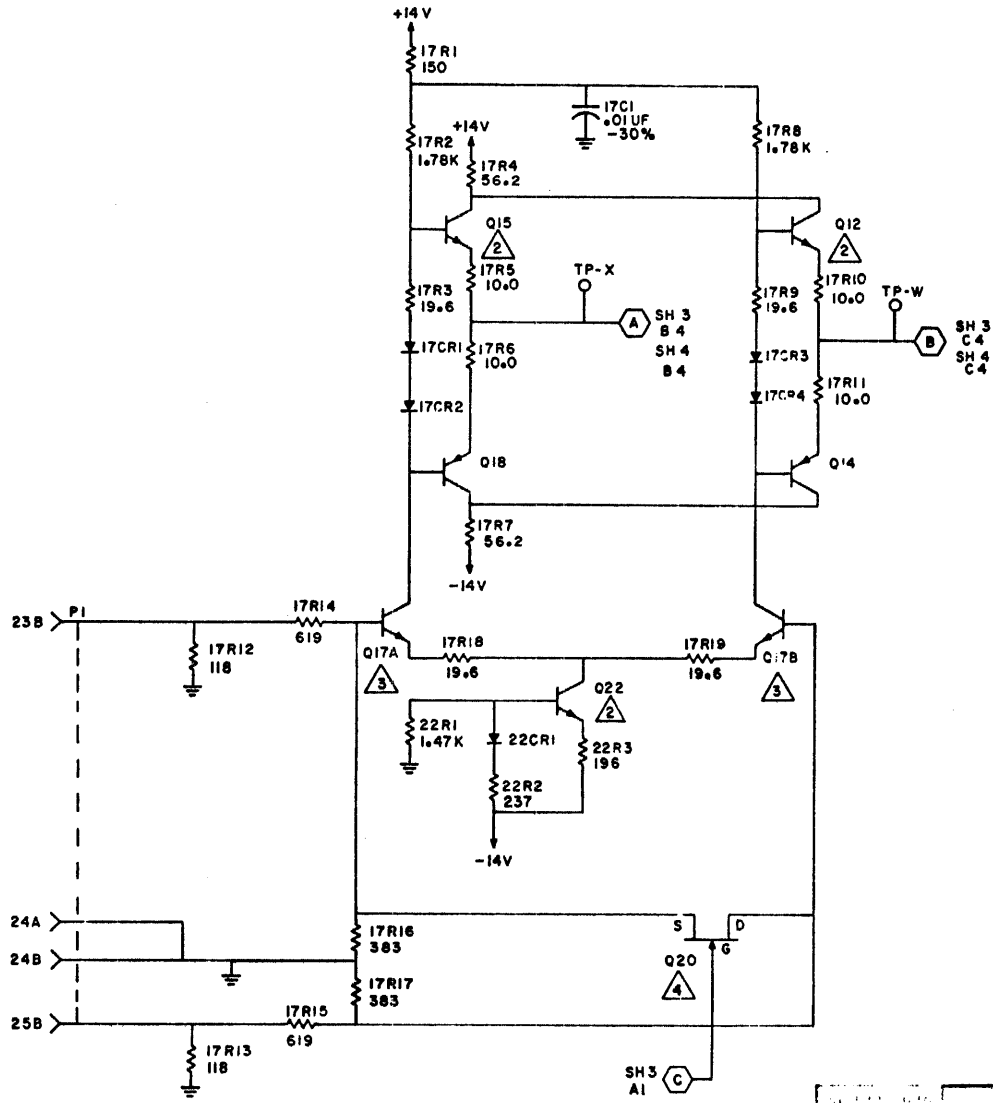
REFERENCE DRAWINGS		NORMAN DALE DIVISION		SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 2FRV	
COMP ASSY	54226103	BR 3A3			
COMPONENTS EXCEPT AS NOTED		OWN	R. KONECNY	3-6-72	DRAWING NUMBER 54226203
TOLERANCE	RES	CHK	J. Thompson	7-22-72	
RES	$\pm 1\%$	DATE	3-23-72	2-23-72	CD 5
CAP	OHMS	DATE	3-23-72	2-23-72	

W 54226203A

4-94

70629100 E

REVISION RECORD					
REV.	DATE	BY	CHKD.	APP.	REASON
					SEE SHT 1 FOR REV



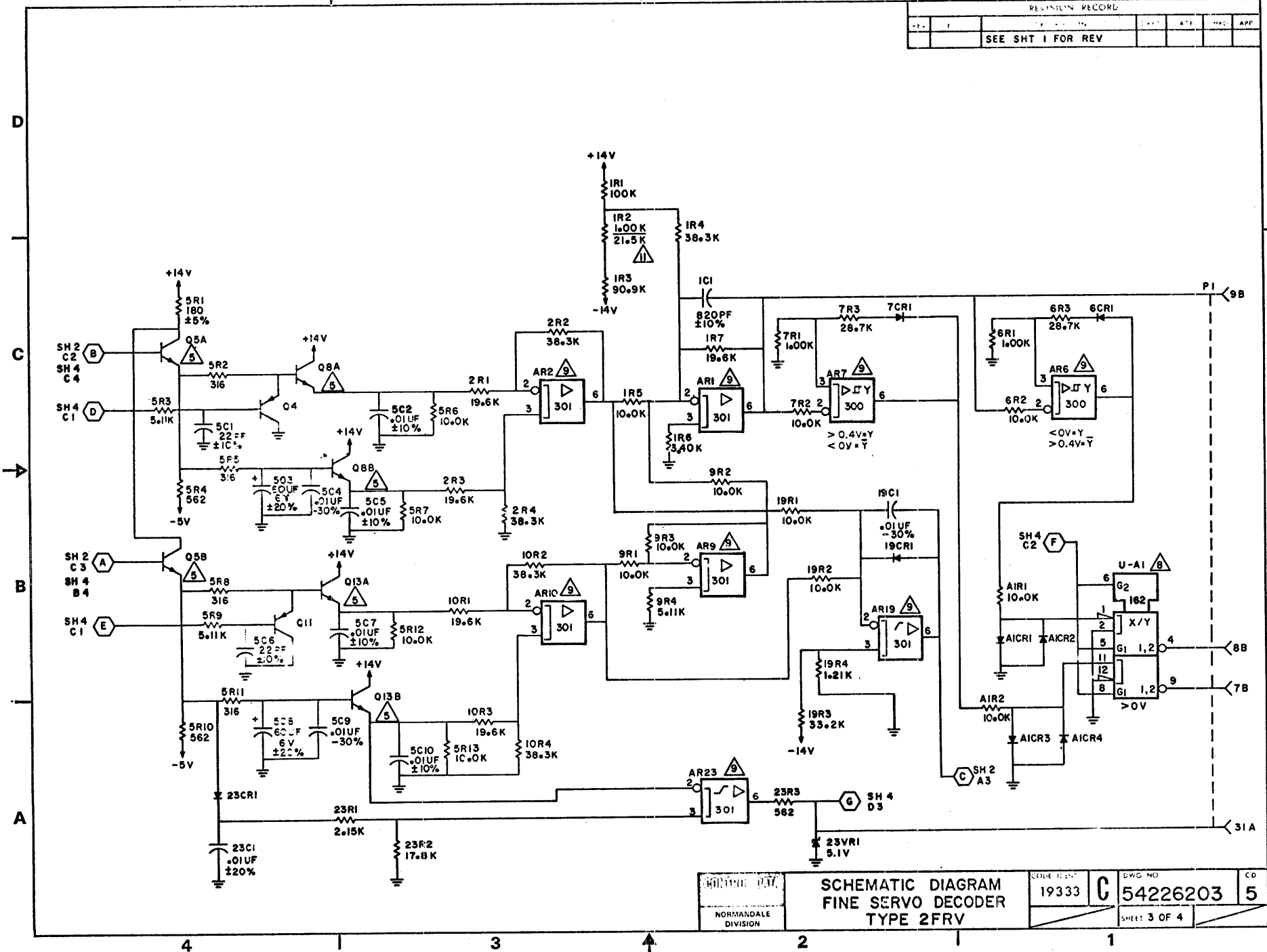
APPROVAL DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 2FRV		DATE 19333	REV. C	DWG. NO. 54226203	SHEET 2 OF 4	CD 5

W54226203A

70629100 E

4-95

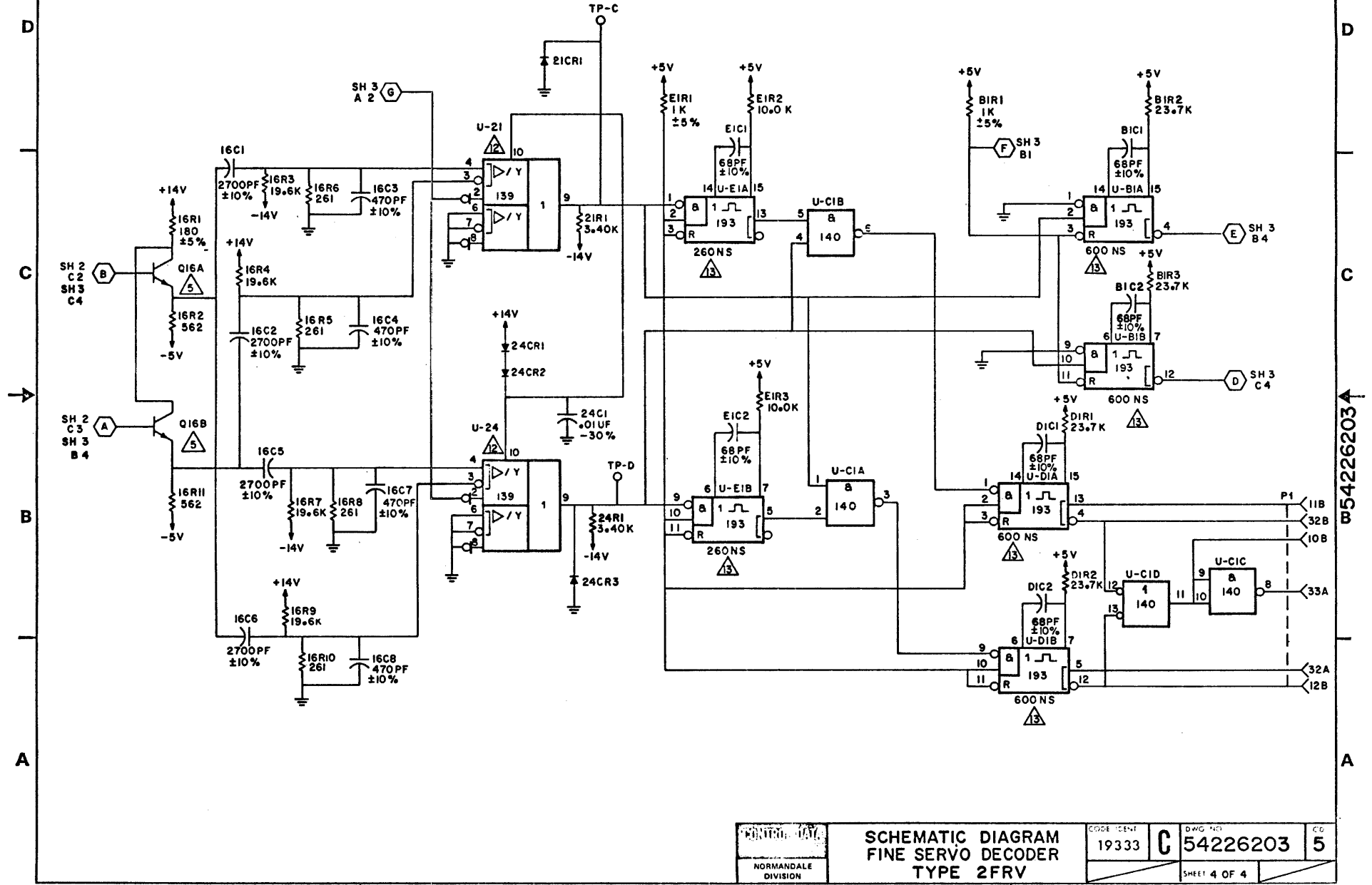
REVISION RECORD				
NO.	DATE	BY	APP.	APP.
SEE SH1 FOR REV				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 2FRV		SCALE 1:1	C	DWG NO	5
			19333		54226203	

B54226203A

REVISION RECORD						
REV	ECO	DESCRIPTION	ENT	DATE	CHKD	APP
		SEE SHT 1 FOR REV				



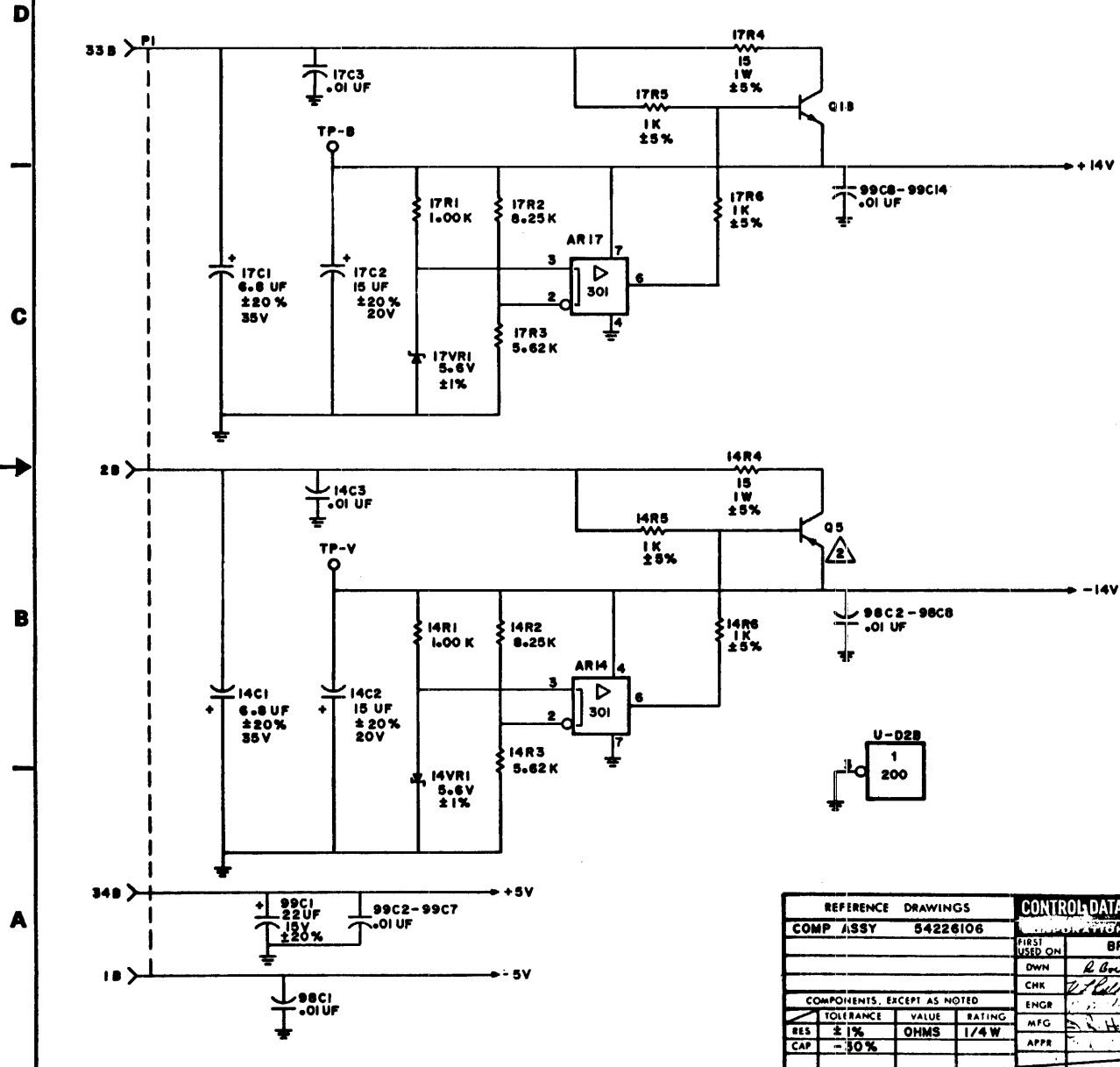
19333
NORMANDE
DIVISION

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 2FRV

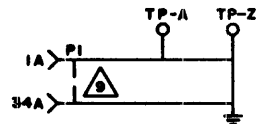
CODE IDENT 19333	DWG NO 54226203	C/D 5
SHEET 4 OF 4		

54226203

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED			11/73	ELP	



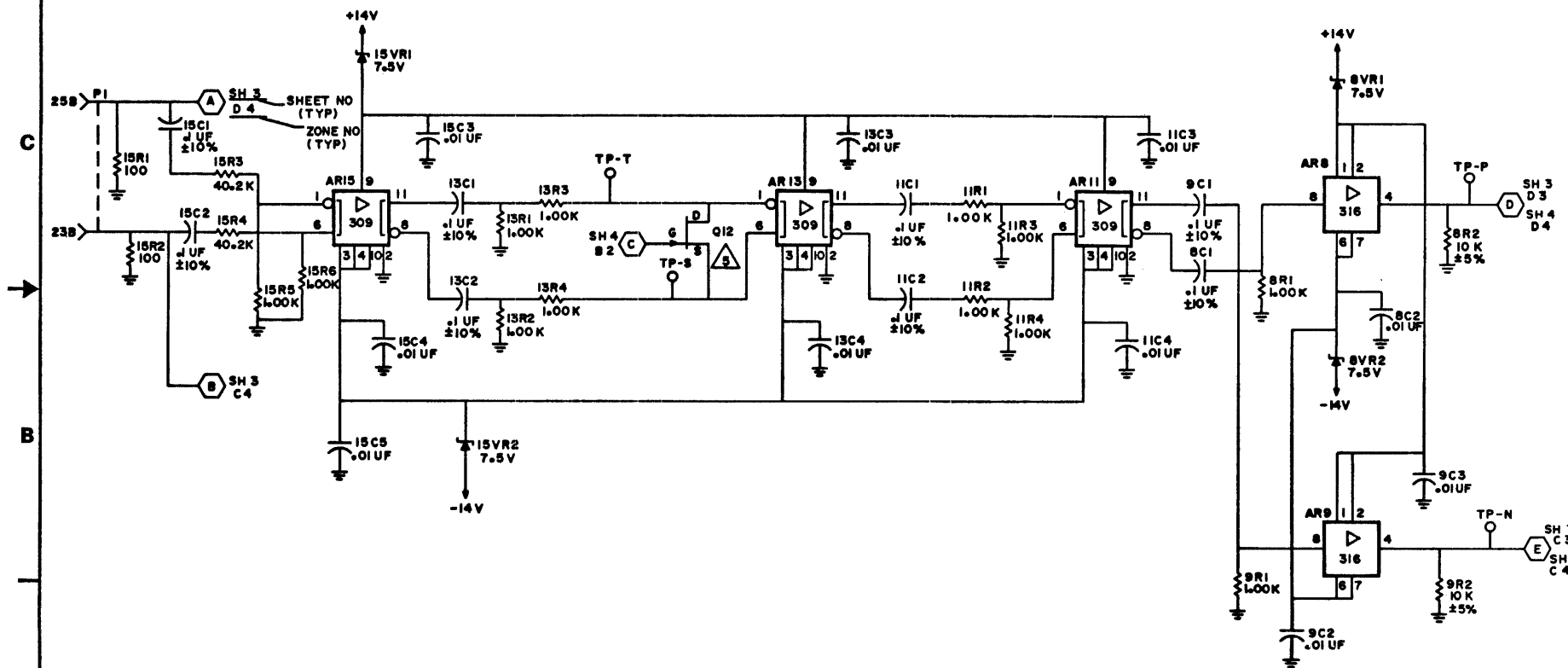
- NOTE:
1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, TIP 29, 50221800.
 ALL DIODES SILICON PLANAR, 24553500.
 ALL ZENER DIODE VOLTAGE TOLERANCES $\pm 5\%$
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V
 - 2 TRANSISTOR, SNPN, TIP 30, 50221900.
 - 3 DELAY TIME FOR REF ONLY
 - 4 IC, TYPE 139, HAS PIN 1 CONNECTED TO GND.
 - 5 TRANSISTOR, N CHANNEL J FET, 2N5434, 50218302.
 - 6 IC, TYPE 162 HAS PIN 13 CONNECTED TO -5V.
 - 7 IC, TYPE 3218 HAS PIN 12 CONNECTED TO GND.
 - 8 IC'S, AR1, AR2, AR3, AR4, AR6, AR7 AND AR10
 HAVE PIN 7 CONNECTED TO +14V AND PIN 4
 CONNECTED TO -14V.
 - 9 ALL UNUSED CONNECTOR PINS ARE GROUNDED.
 - 10 TEST SELECT RESISTOR TO BE SELECTED FROM
 DRAWING 94357500 AND INSERTED DURING CARD
 TEST PER RECOMMENDED TEST PROCEDURE.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY	54226106	FIRST USED ON	BR3A6			SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 3FRV	
COMPONENTS, EXCEPT AS NOTED		DWN	R. G. B.	5-3-73			
TOLERANCE		CHK	D. P. R.	5-9-73			
RES	$\pm 1\%$	ENGR		5-9-73			
CAP	-50%	MFG		5-9-73			
		APPR					
				CODE IDENT	DRAWING NUMBER	CD	
				19333	C 54226206	8	
				SHEET 1 OF 4			

B54226206

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



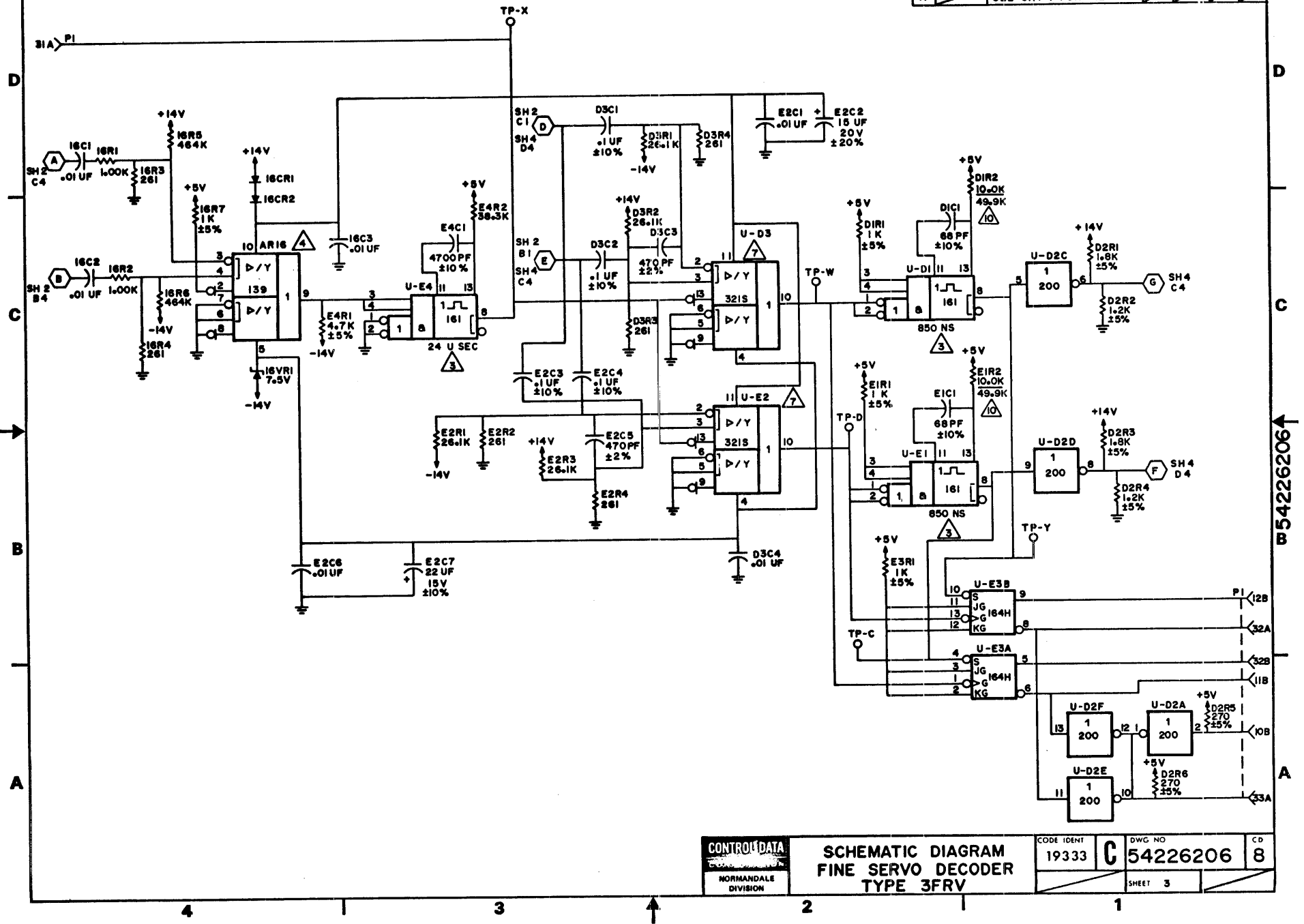
CONTROL DATA <small>Electronic Division</small> NORMANDALE DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 3FRV		CODE IDENT 19333	DWG NO 54226206	CD 8
				SHEET 2	

W54226206

70629100 E

4-99

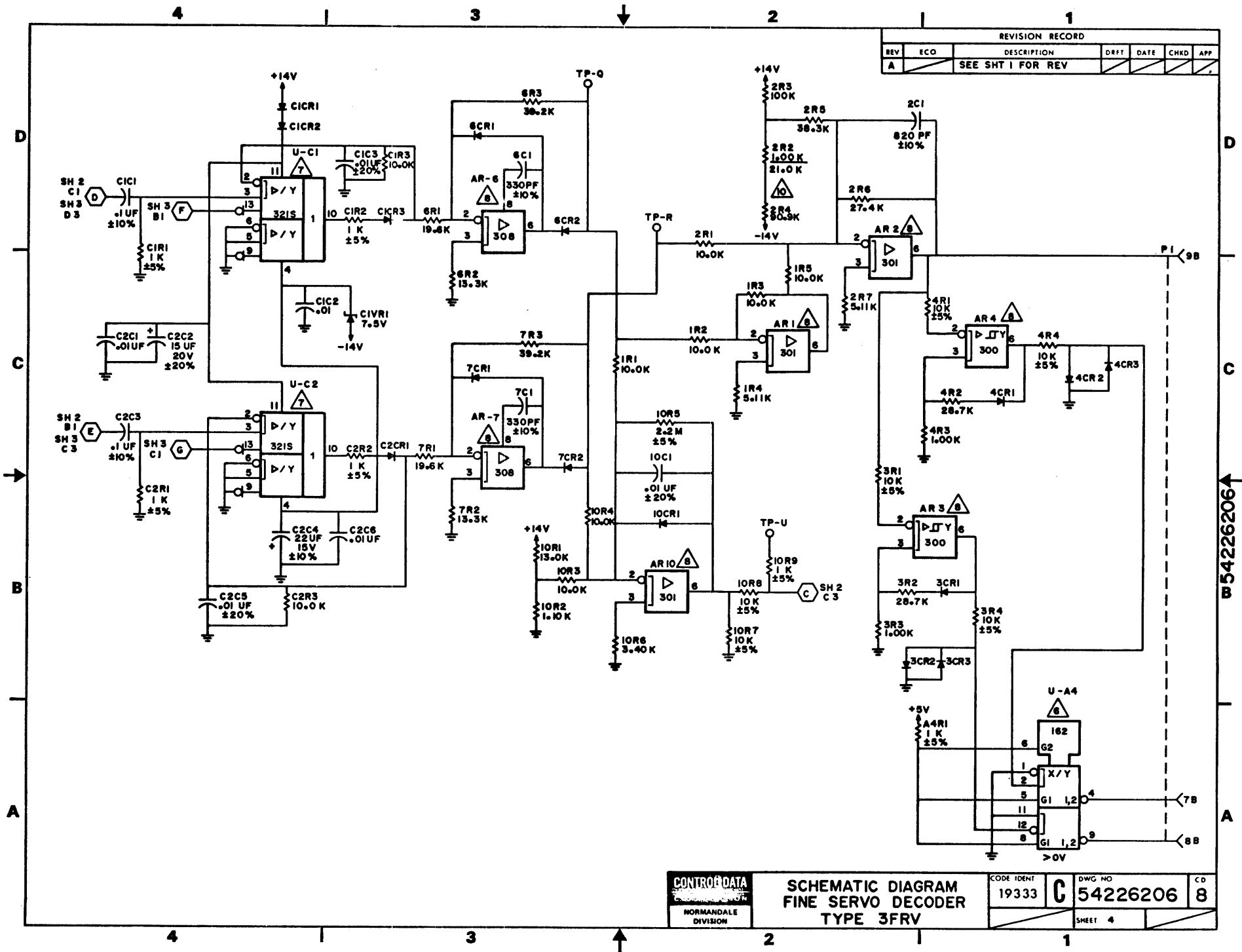
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM FINE SERVO DECODER TYPE 3FRV		CODE IDENT	DWG NO	CD
			19333	54226206	8
			SHEET 3		

W54226206

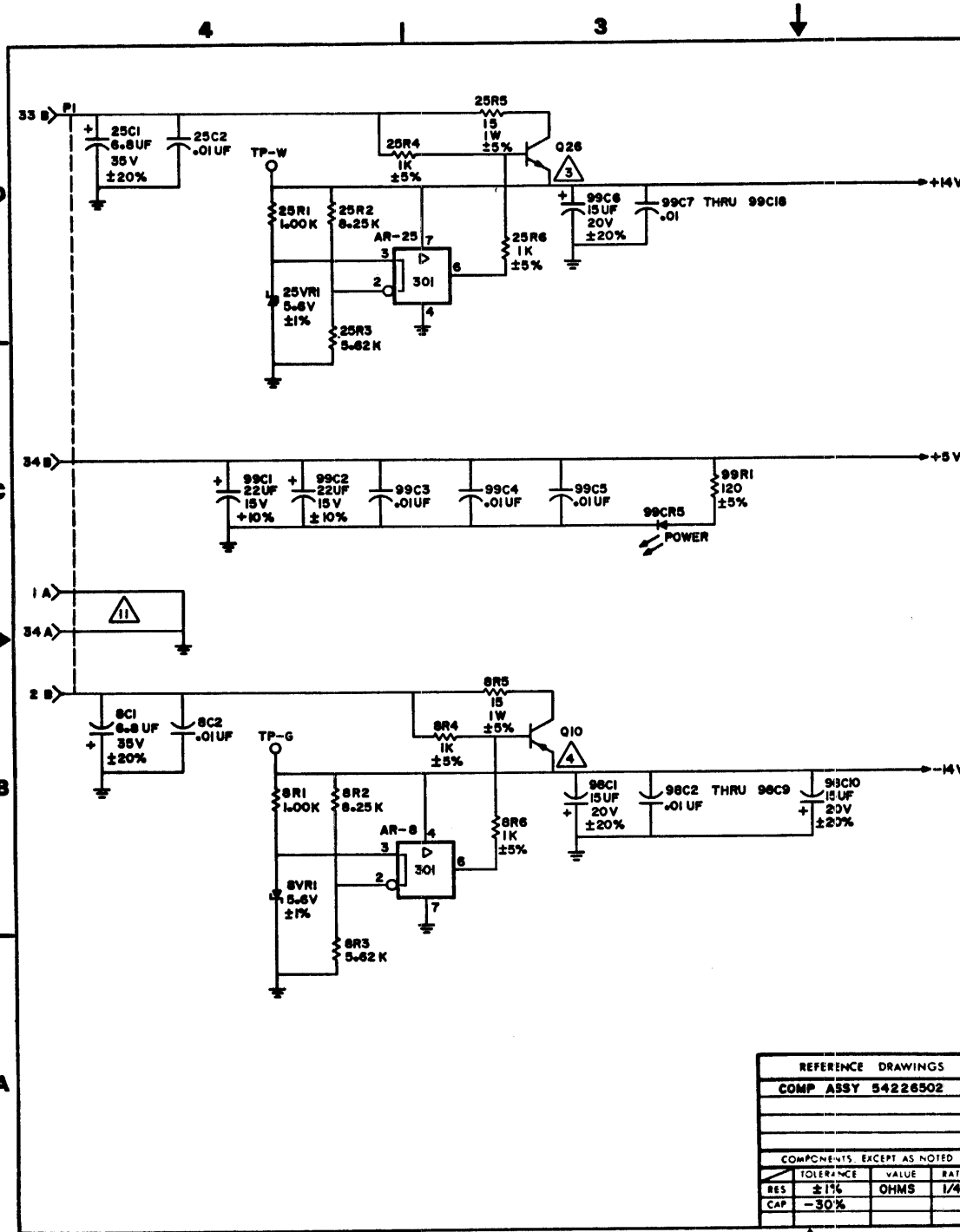
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
FINE SERVO DECODER
TYPE 3FRV

CODE IDENT	DWG NO	CD
19333	54226206	8
SHEET 4		



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23-00	RELEASED					

- NOTE:
- 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ALL TRANSISTORS, NFET, 2N5434, 50218302.
 ALL DIODES SILICON, 24553500.
 - 2. TRANSISTOR, SNPN, 2N2221, 50210102.
 - 3. TRANSISTOR, SNPN, POWER, 50221800.
 - 4. TRANSISTOR, SPNP, POWER, 50221900.
 - 5. DELAY TIMES FOR REFERENCE ONLY.
 - 6. IC PACKAGE AR 3, 4, 5, 6, 16, 17, AND 18 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +4V.
 - 7. TERMINAL NUMBERING FOR RELAY K11 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.
 - 8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
 - 9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 1.00K TO 1.00M.
 - 10. SPDT SWITCH.
 - 11. CONNECTOR PINS 7B, 10B, 21B, 23B, 25B, AND 27B SHALL NOT BE USED. ALL OTHER PINS NOT OTHERWISE DESIGNATED ARE GND.

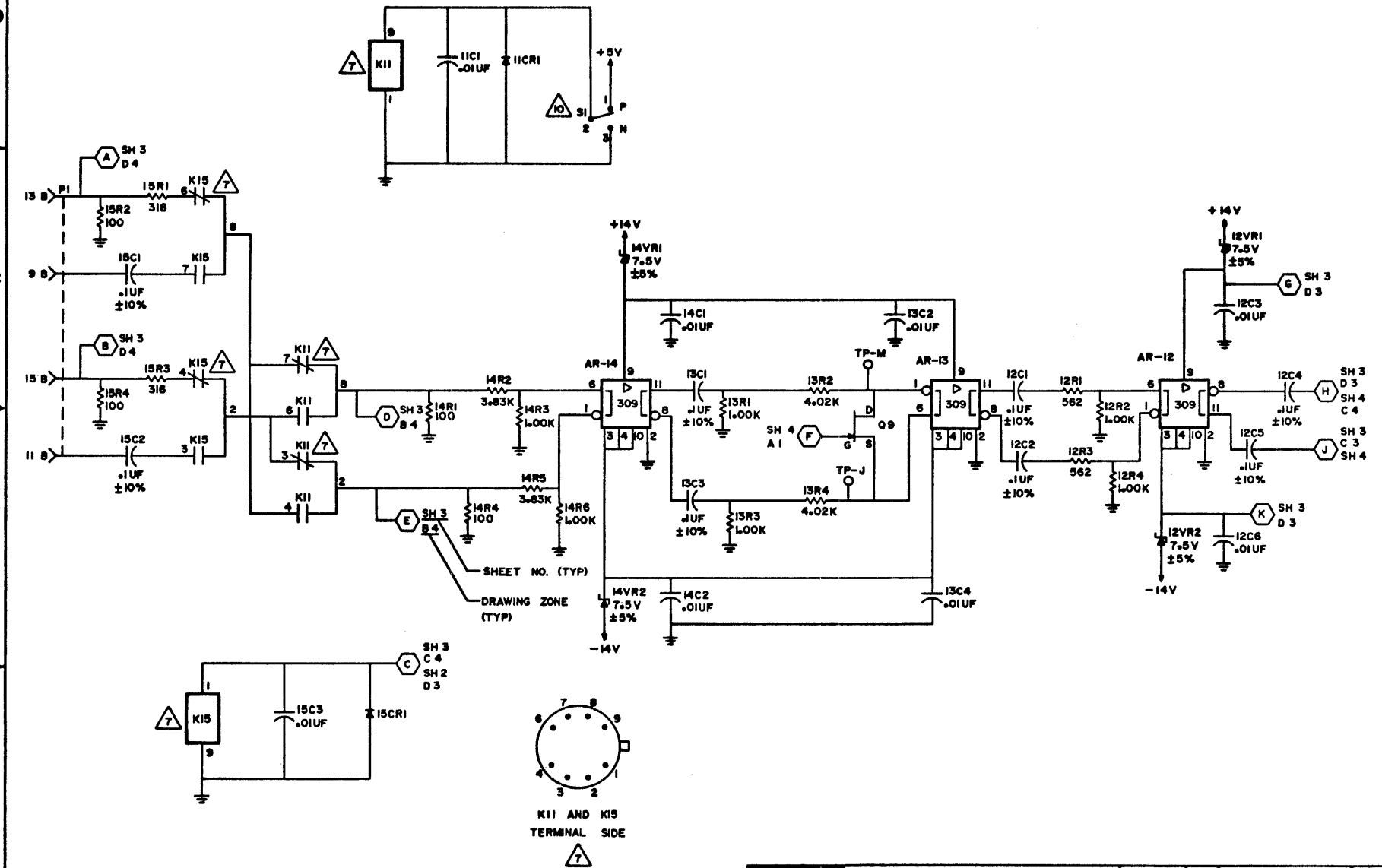
REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54226502			BR3AS				SCHEMATIC DIAGRAM	
			D.G. TUTTLE 9-9-72				HEAD ALIGNMENT CARD	
			9-27-72				TYPE BFSV	
COMPONENTS, EXCEPT AS NOTED			MFG		APPR		CODE IDENT	DRAWING NUMBER
RES	±1%	OHMS	1/4W				19333	C 54226602
CAP	-30%							8
							SHEET 1 OF 4	

B 54226602 ↑

4-100.2

70629100 E

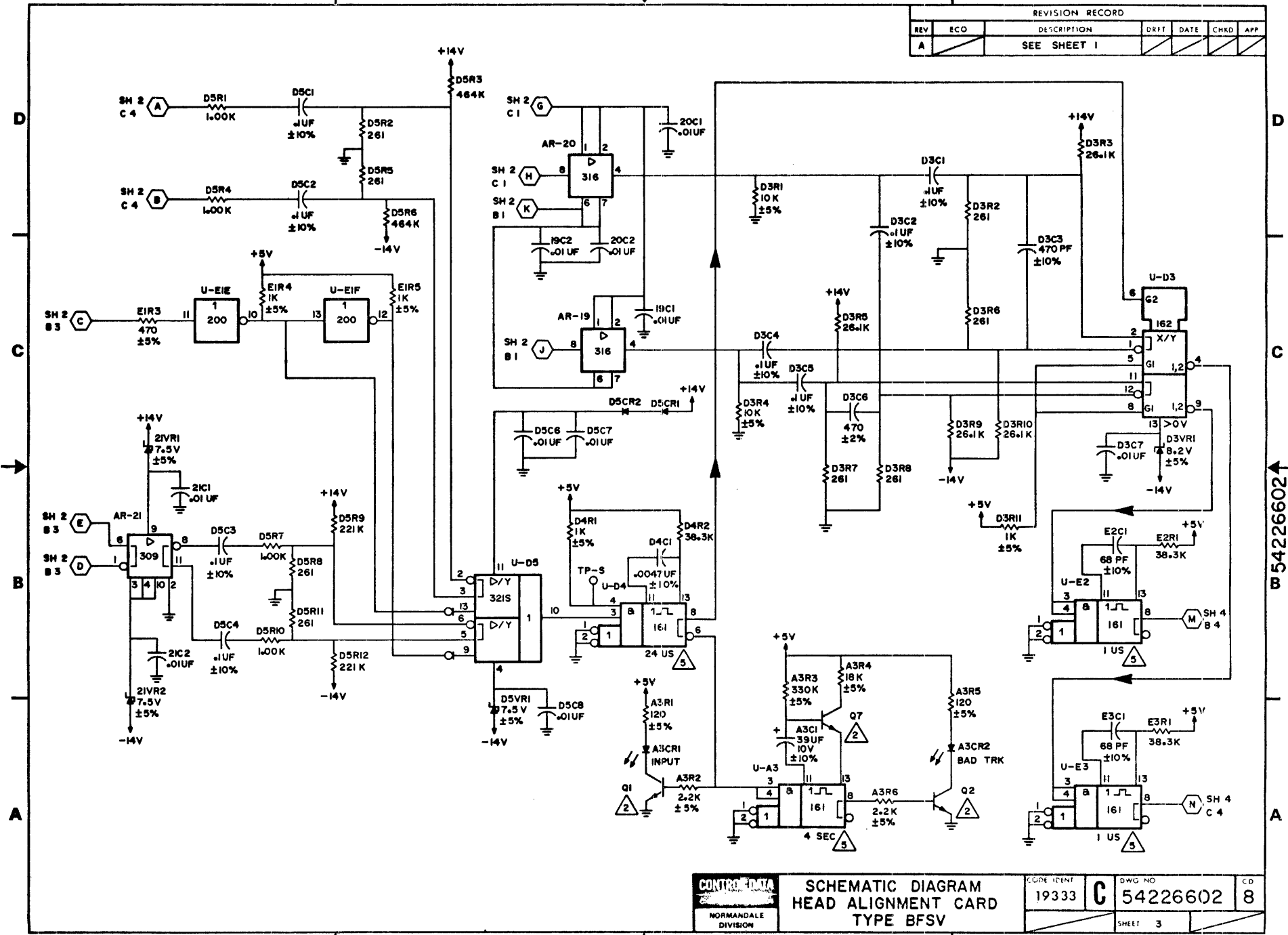
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE BFSV		CODE IDENT 19333	DWG NO 54226602	CD 8
			SHEET 2		

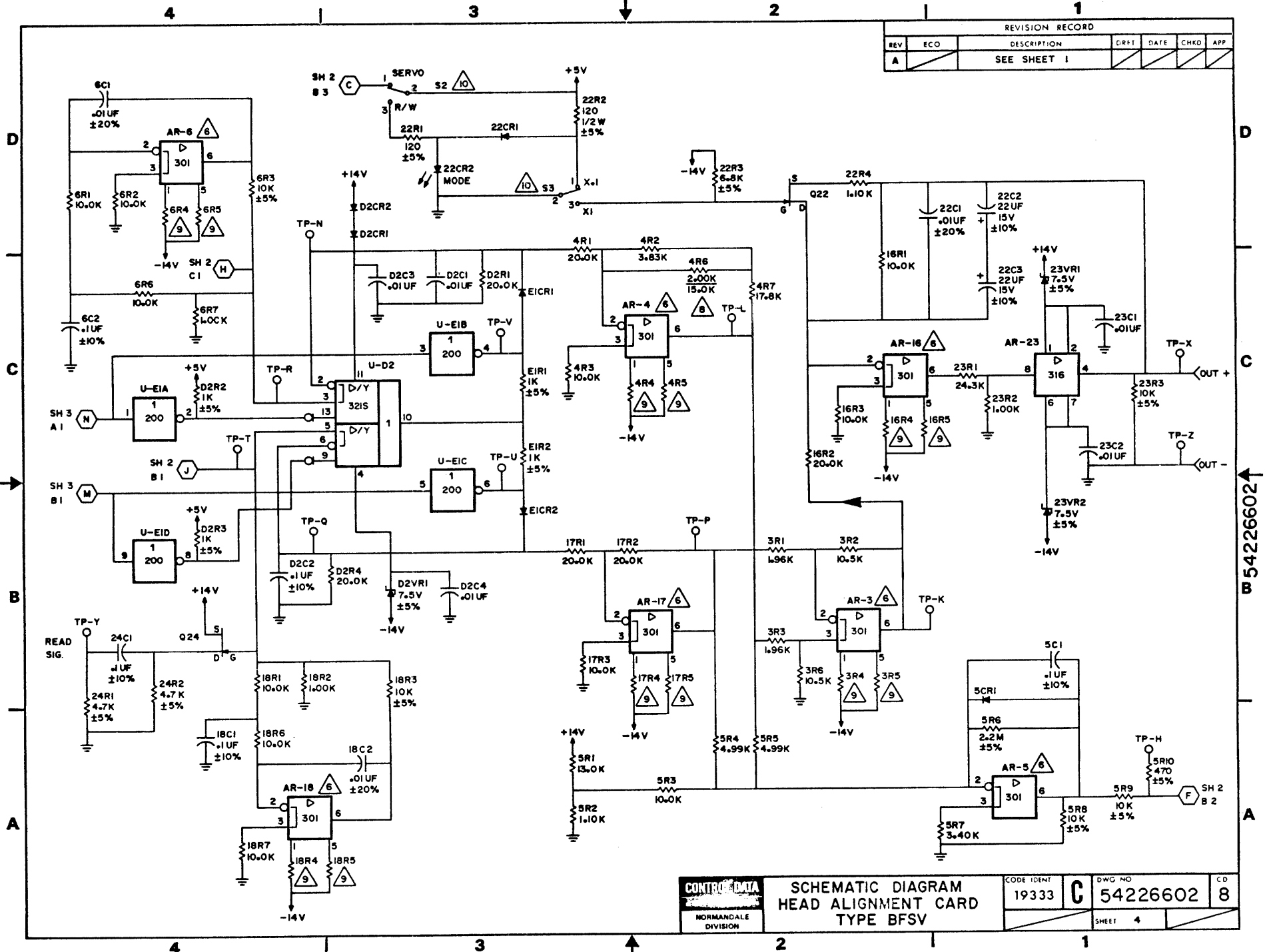
54226602

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



 NORMANDELE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE BFSV		CORE IDENT 19333	DWG NO C 54226602	CD 8
				SHEET 3	

REVISION RECORD						
REV	ECO	DESCRIPTION	CRFT	DATE	CHKD	APP
A		SEE SHEET 1				



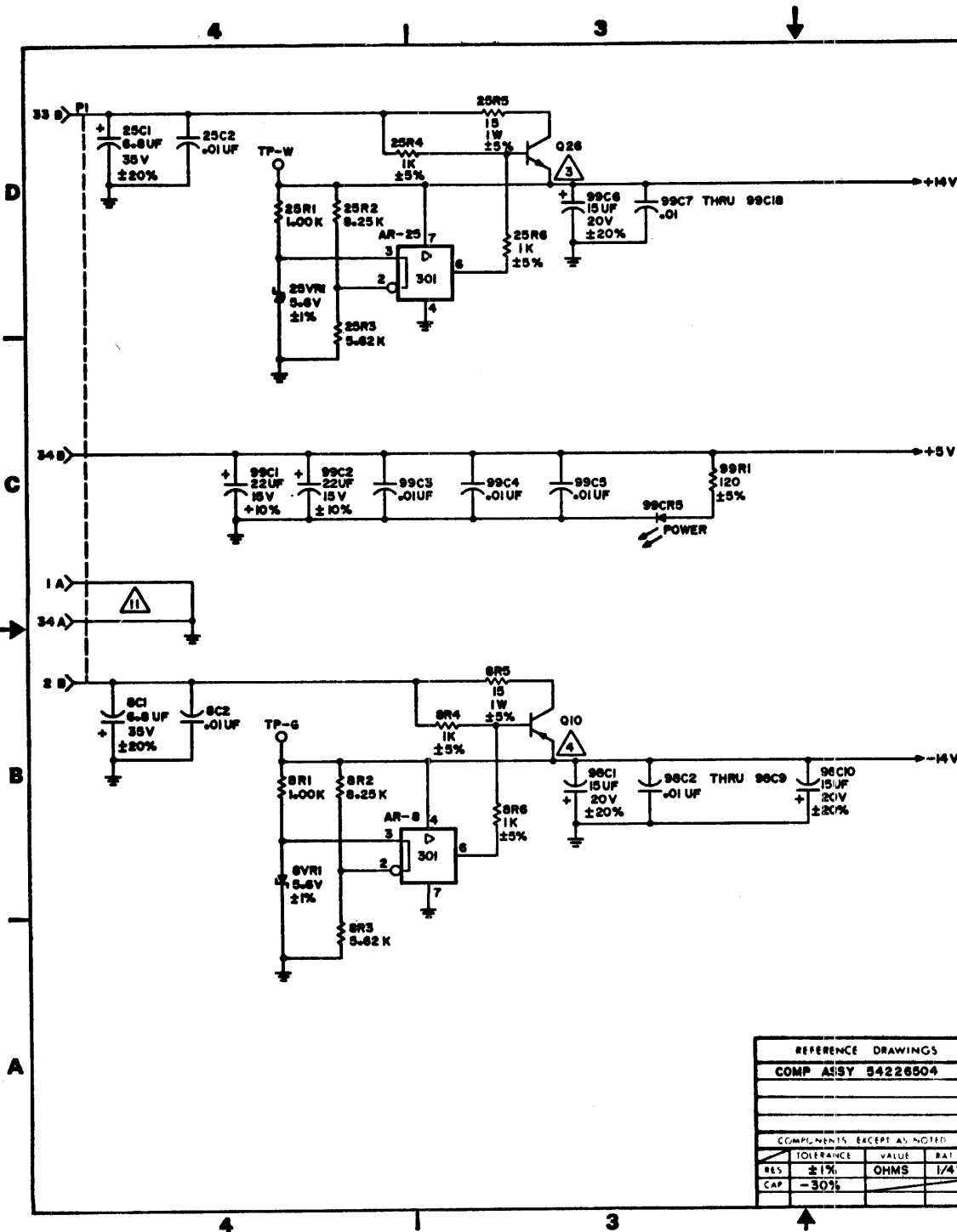
CONTROL DATA
NORMANDALE
DIVISION

SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE BFSV

CODE IDENT	DWG NO	CD
19333	54226602	8
SHEET 4		

70629100 E

4-100.5



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23000	RELEASED		7-19-73			

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ALL TRANSISTORS, NFET, 2N5434, 50218302.
 ALL DIODES SILICON, 24553500.

- 2. TRANSISTOR, SNPN, 2N2221, 50210102.
- 3. TRANSISTOR, SNPN, POWER, 50221800.
- 4. TRANSISTOR, SNPN, POWER, 50221900.
- 5. DELAY TIMES FOR REFERENCE ONLY.
- 6. IC PACKAGE AR 3, 4, 5, 6, 16, 17, AND 18 HAVE PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +4V.
- 7. TERMINAL NUMBERING FOR RELAY K11 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.
- 8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
- 9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 1.00K TO 1.00M.
- 10. SPDT SWITCH.
- 11. CONNECTOR PINS 7B, 10B, 21B, 23B, 25B, AND 27B SHALL NOT BE USED. ALL OTHER PINS NOT OTHERWISE DESIGNATED ARE GND.
- 12. NO CONNECTIONS.

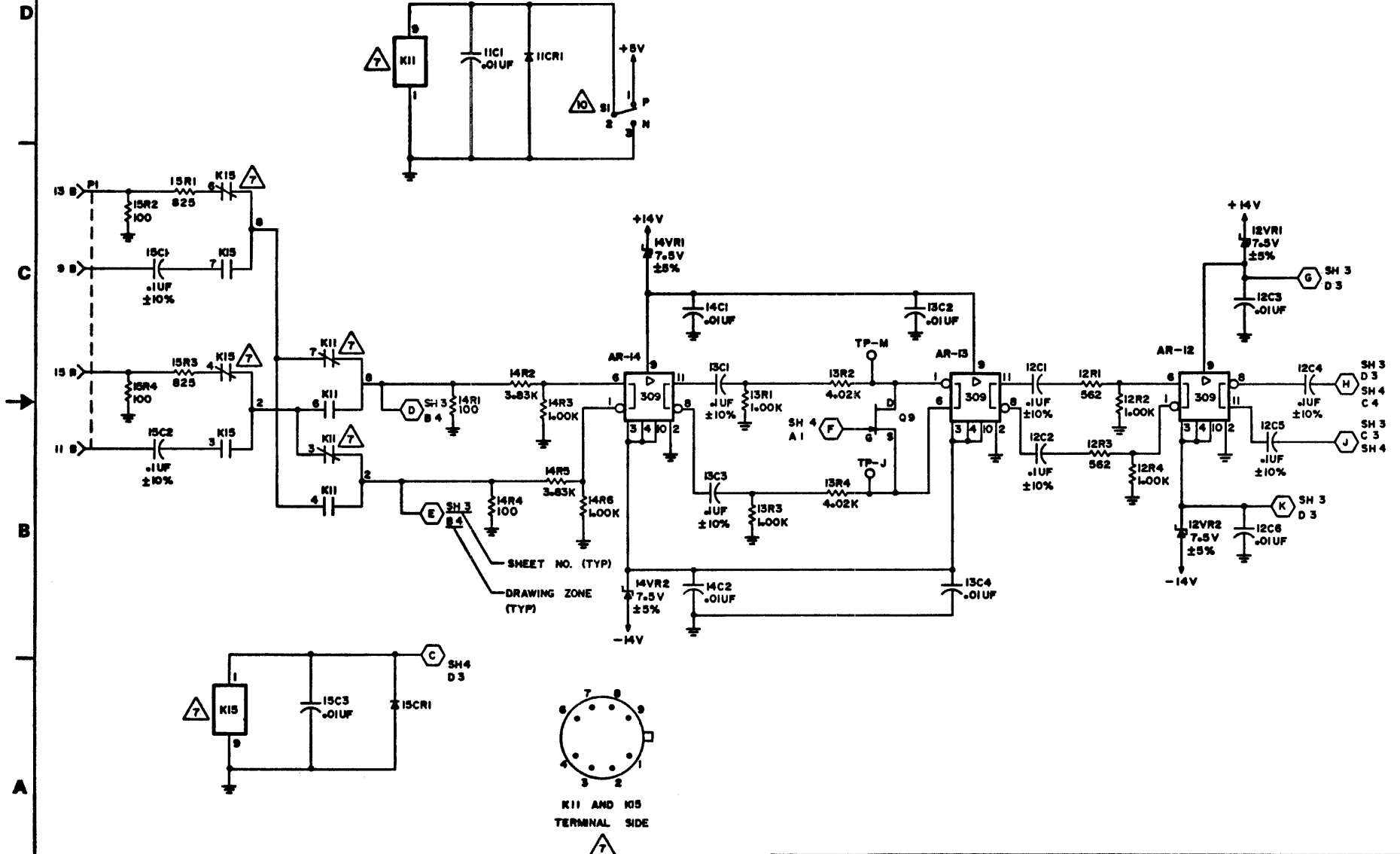
REFERENCE DRAWINGS COMP ASSY 54226604	CONTROL DATA BR3AS	NORMANDALE DIVISION	TITLE SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE CFSV
COMPONENTS EXCEPT AS NOTED:			CODE IDENT 19333
TOLERANCE	VALUE	RAT NO	DRAWING NUMBER 54226604
RES ±1%	OHMS	1/4W	C.D. 4
CAP -30%			

W54226604

4-100.6

70629100 F

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA
NORMANDEALE
DIVISION

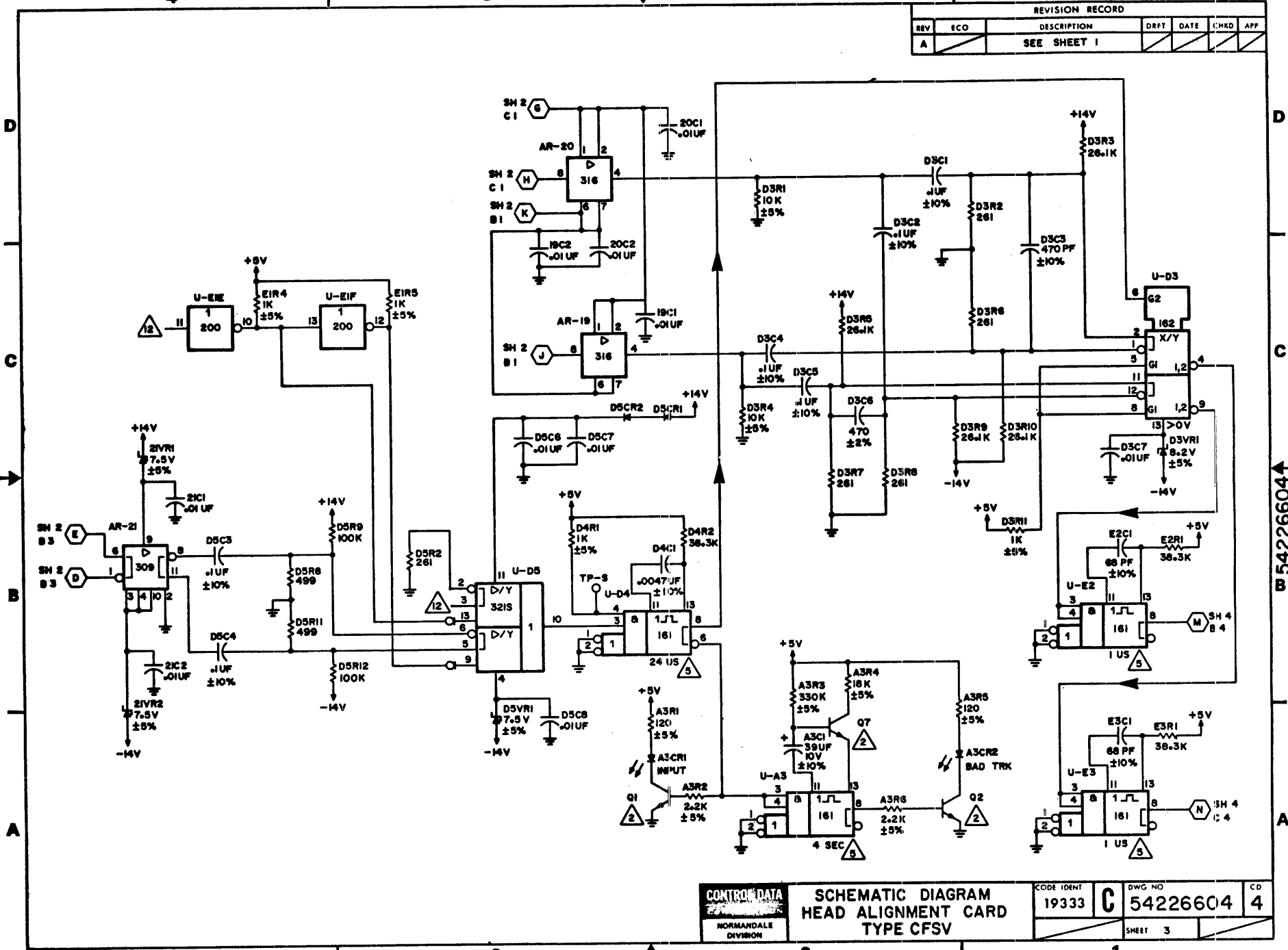
SCHEMATIC DIAGRAM
HEAD ALIGNMENT CARD
TYPE CFSV

CODE IDENT 19333	DWG NO C 54226604	CD 4
SHEET 2		

70629100 E

4-100,7

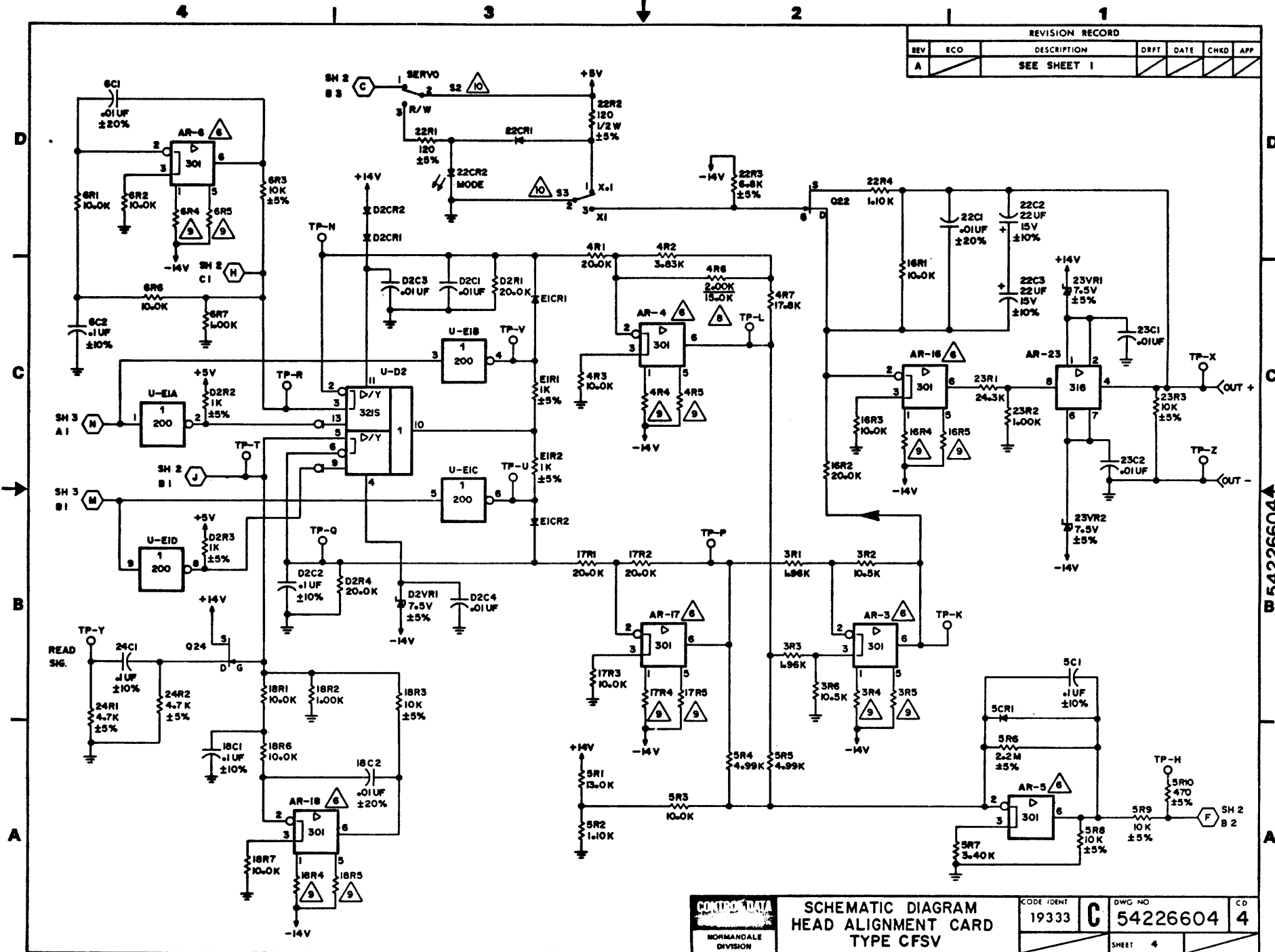
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



 NORMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE CFSV		CODE IDENT 19333	DWG NO C 54226604	CD 4
				SHEET 3	

B 54226604

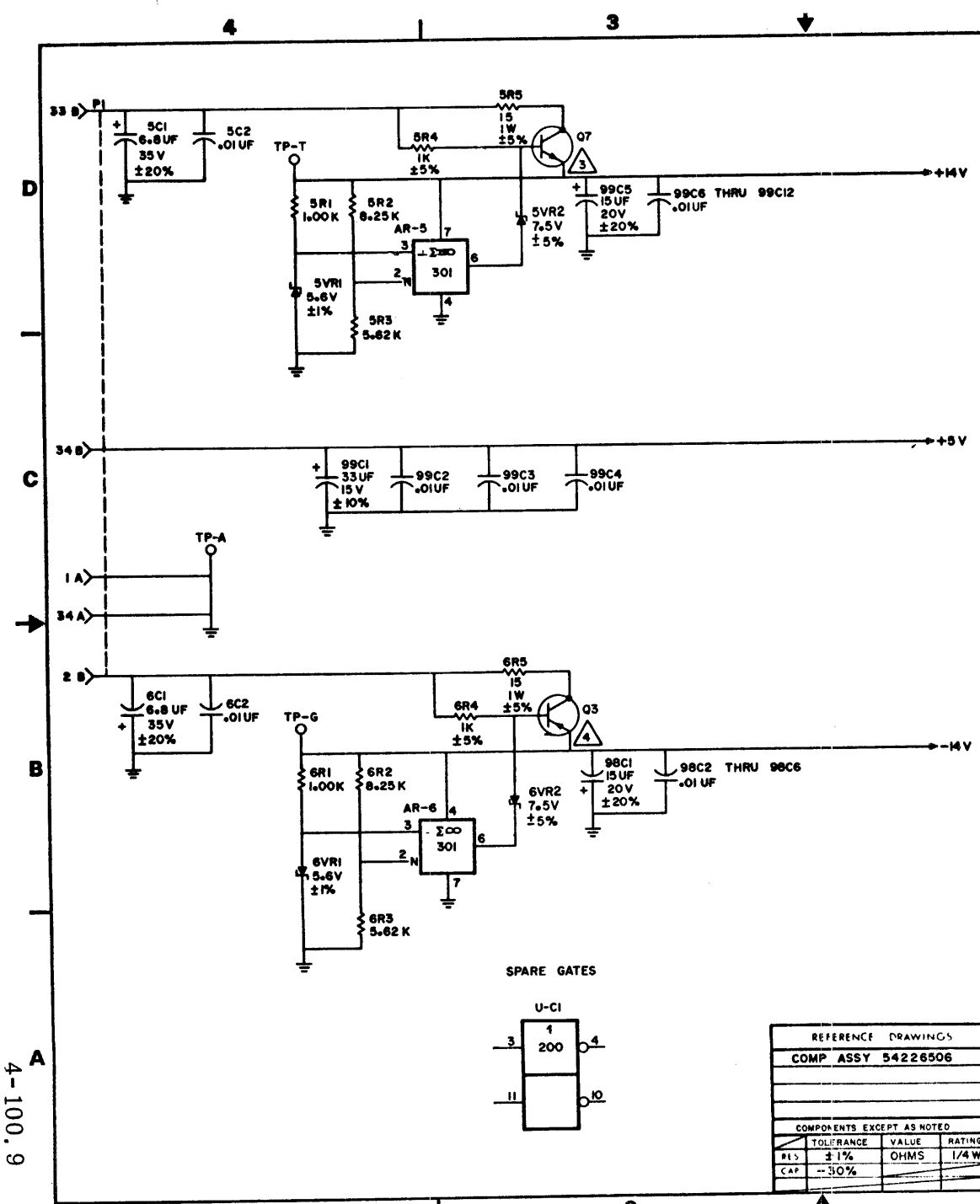
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



 CONTROL DATA NORMANDELL DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE CFSV		CODE IDENT 19333	DWG NO 54226604	CD 4
			SHEET 4		

54226604

70629100 G



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V EXCEPT U-B1.
 ALL TRANSISTORS, JFET, 50218302.
 ALL DIODES SILICON, 24553500.

- 2. TRANSISTOR, JFET, 50218100.
- 3. TRANSISTOR, SNPN, POWER, 50221800.
- 4. TRANSISTOR, SNPN, POWER, 50221900.
- 5. DELAY TIMES FOR REFERENCE ONLY.
- 6. IC PACKAGE U-A1, U-A3, AND U-A5 HAVE PIN 4 CONNECTED TO -14V AND PINS 9 AND 13 CONNECTED TO +14V.
- 7. TERMINAL NUMBERING FOR RELAY K14 AND K15 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM.
- 8. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.
- 9. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE, FROM THE FOLLOWING RANGE 2.00K TO 100K.
- 10. TOGGLE SWITCH, 94263907.
- 11. TRANSISTOR, SPNP, 2N4916, 50211610.
- 12. IC PACKAGE AR-1 HAS PIN 4 CONNECTED TO -14V AND PIN 7 CONNECTED TO +14V.
- 13. IC PACKAGE U-C3 HAS PIN 6 CONNECTED TO -14V AND PIN 11 CONNECTED TO +14V.
- 14. TRANSISTOR, SNPN, 2N3569, 50210811.

REFERENCE DRAWINGS	CONTROL DATA	NORMANDEALE DIVISION	TITLE	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV		
COMP ASSY 54226506	FIRST USED ON	BR389A/B	CODE IDENT	19333	DRAWING NUMBER	54226606
COMPONENTS EXCEPT AS NOTED			APPR			
TOLERANCE	VALUE	RATING				
RES	±1%	OHMS				
CAP	±30%					
			SHEET	1	OF	4

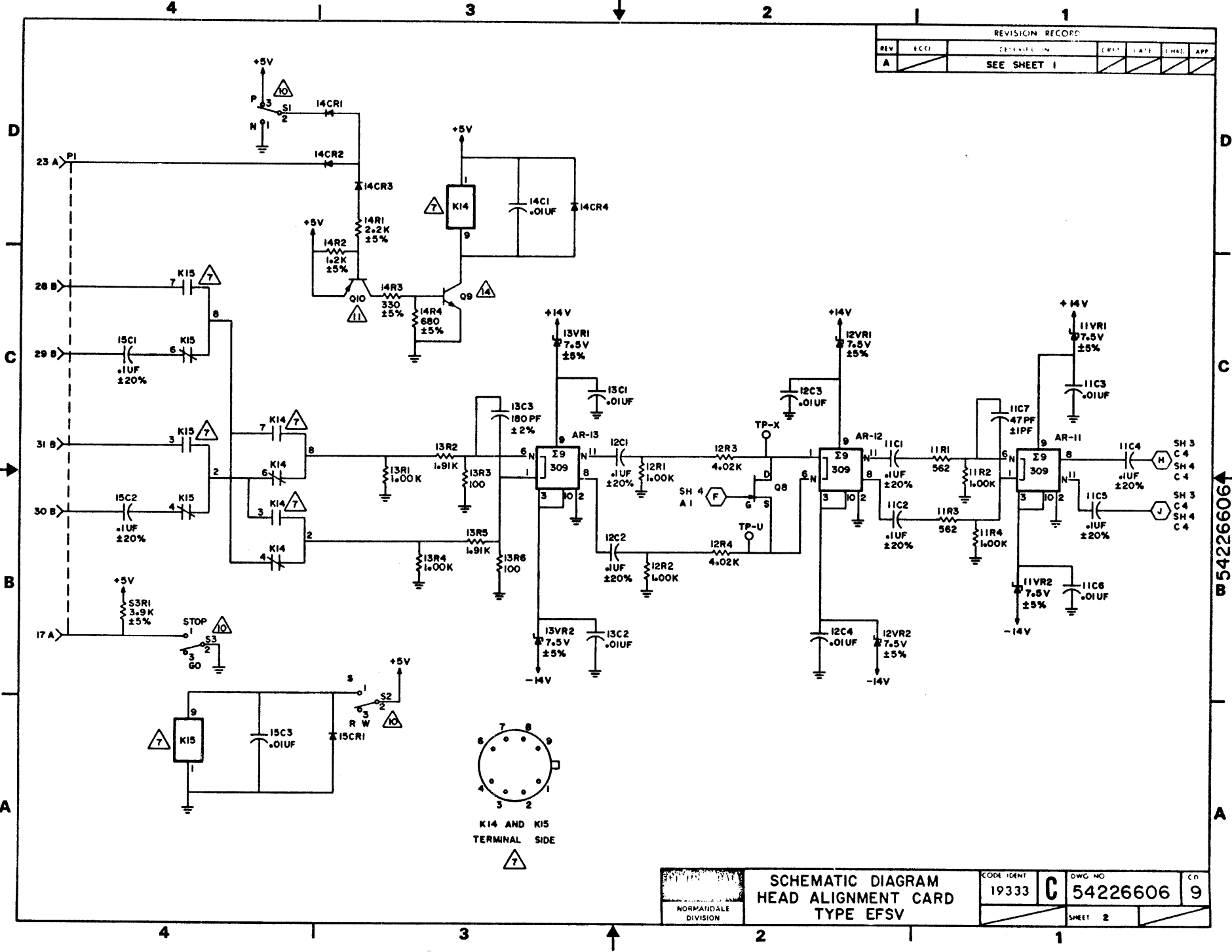
4-100.9

W54226606↑

4-100.10

70629100 G

REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHEET 1				



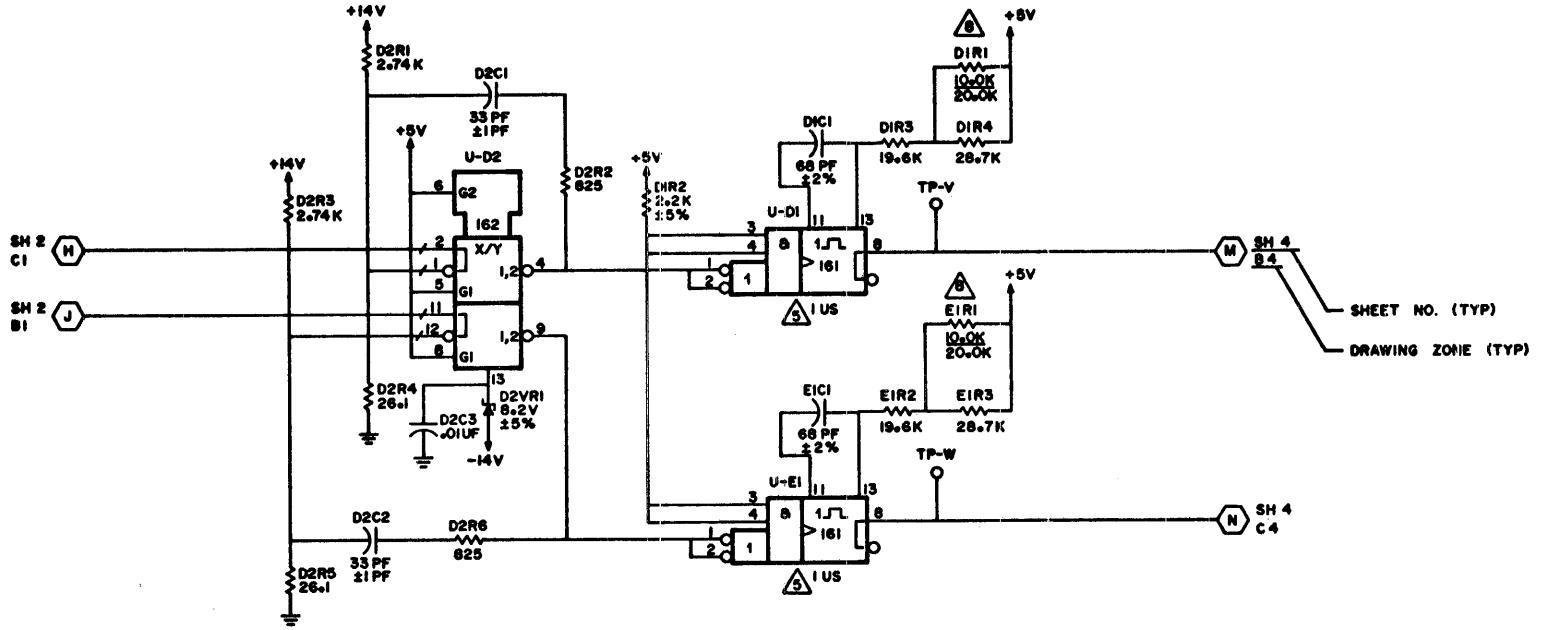
NORMAN DALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV		CODE IDENT 19333	C	DWG NO 54226606	CR 9
			SHEET 2			

54226606

70629100 G

4-100.11

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



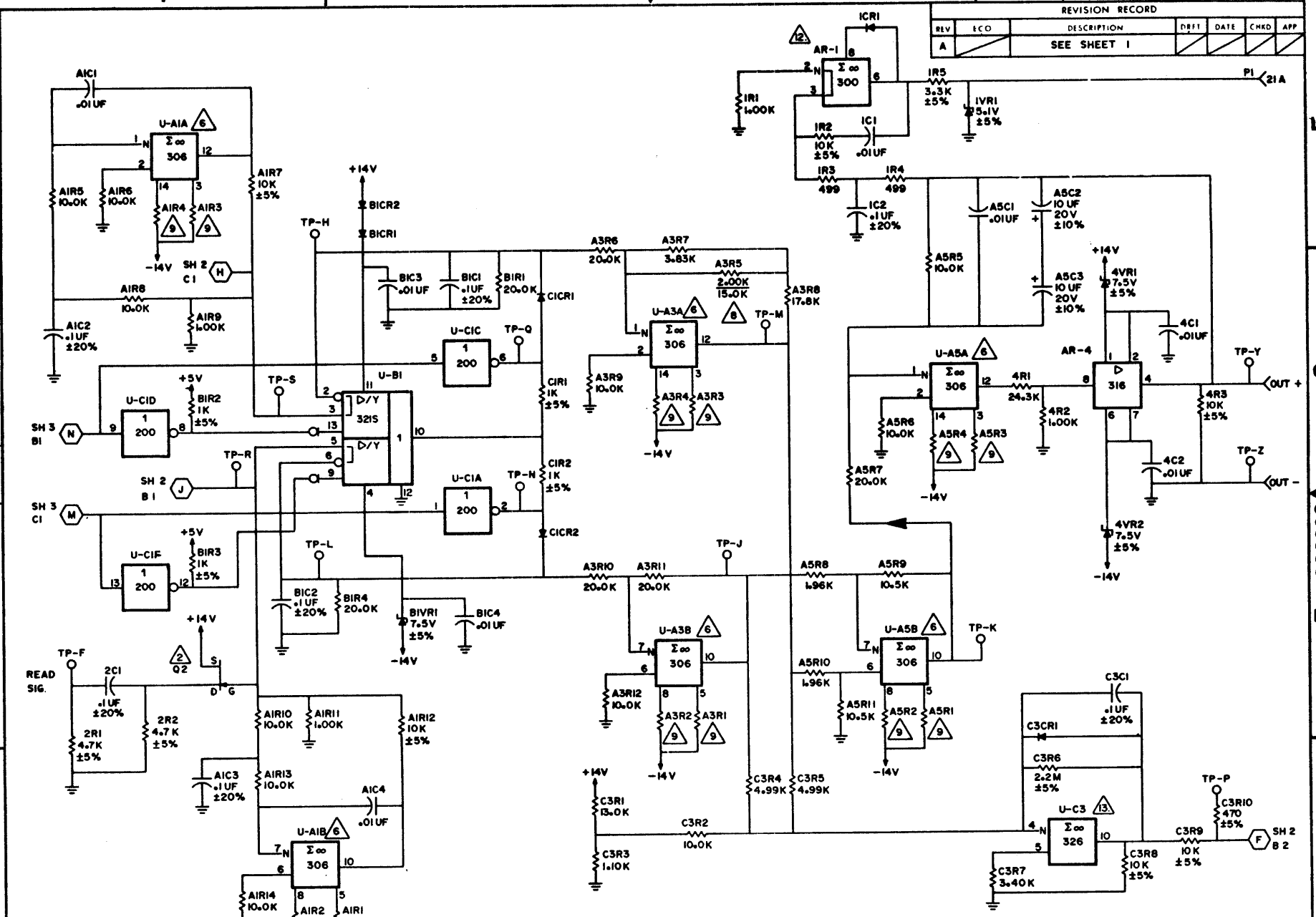
SHEET NO. (TYP)
DRAWING ZONE (TYP)

 NORMANDALE DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV		CODE IDENT 19333	DWG NO 54226606	CD 9
				SHEET 3	

4-100.12

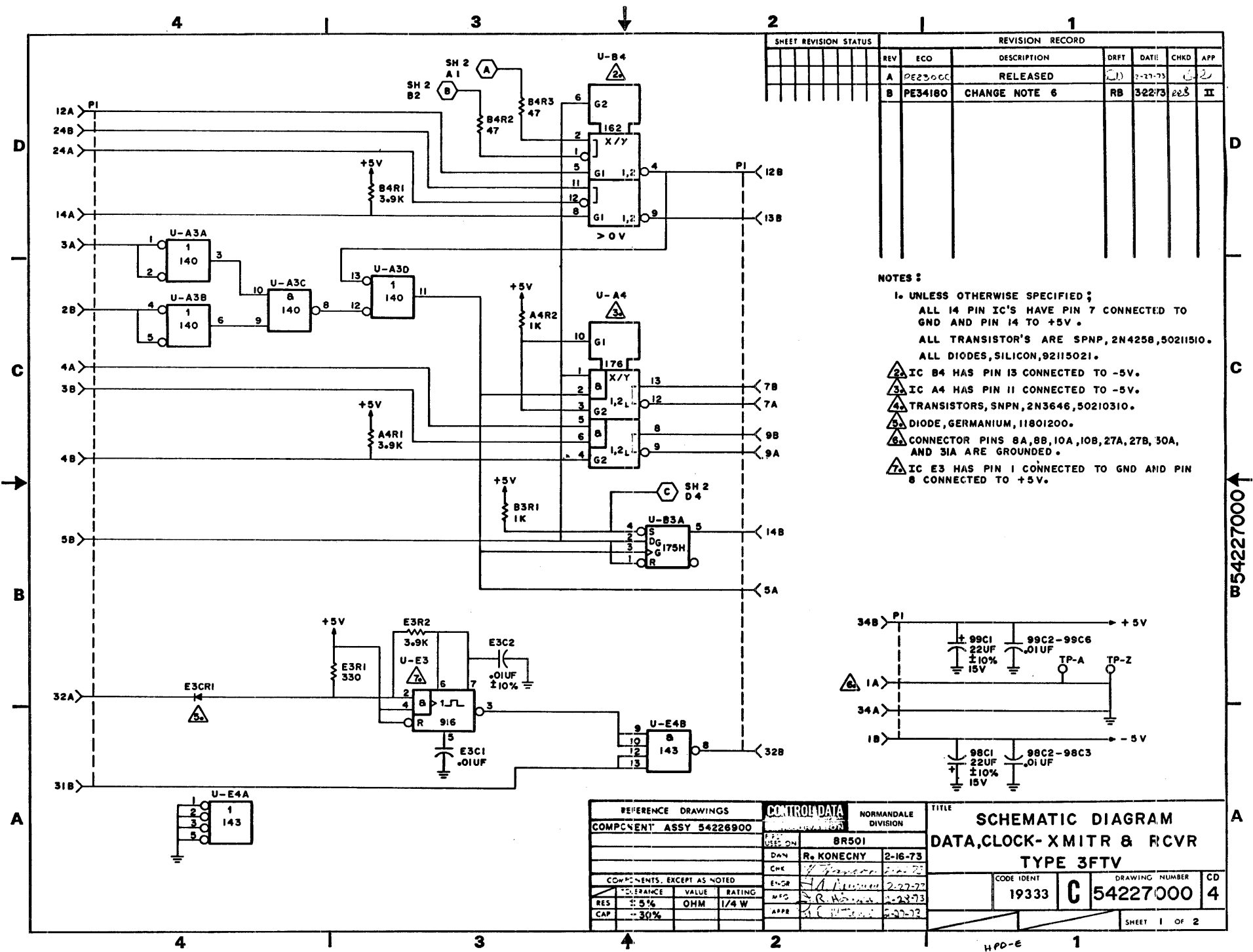
70629100 G

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



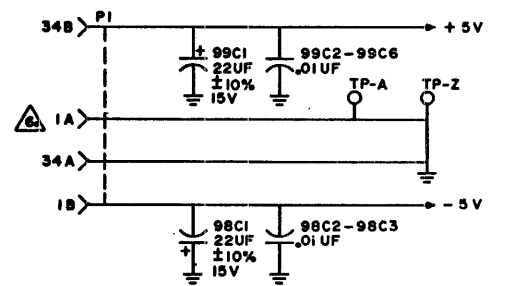
NORWANDA DIVISION	SCHEMATIC DIAGRAM HEAD ALIGNMENT CARD TYPE EFSV		CODE IDENT 19333	C	DWG NO 54226606	CO 9
					SHEET 4	

54226606



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE2300C	RELEASED	JD	2-27-73		
B	PE34180	CHANGE NOTE 6	RB	3/22/73	RLS	II

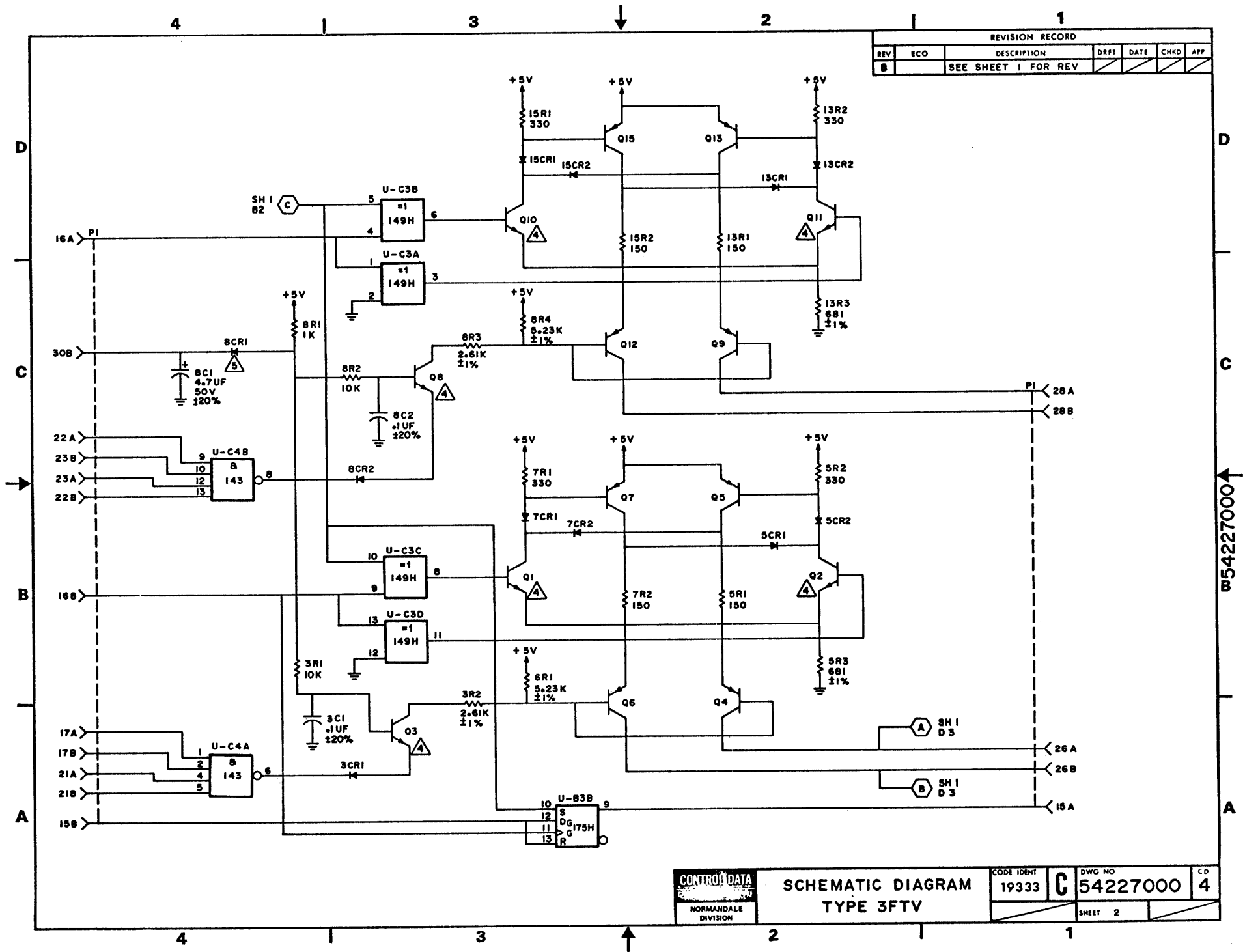
- NOTES:
- 1. UNLESS OTHERWISE SPECIFIED; ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
 - ALL TRANSISTOR'S ARE SPNP, 2N4258, 50211510.
 - ALL DIODES, SILICON, 92115021.
 - △2 IC B4 HAS PIN 13 CONNECTED TO -5V.
 - △3 IC A4 HAS PIN 11 CONNECTED TO -5V.
 - △4 TRANSISTORS, SNPN, 2N3646, 50210310.
 - △5 DIODE, GERMANIUM, 11801200.
 - △6 CONNECTOR PINS 8A, 8B, 10A, 10B, 27A, 27B, 30A, AND 31A ARE GROUNDED.
 - △7 IC E3 HAS PIN 1 CONNECTED TO GND AND PIN 8 CONNECTED TO +5V.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54226900		BR501		DAN R. KONECNY 2-16-73		SCHEMATIC DIAGRAM DATA, CLOCK-XMITR & RCVR TYPE 3FTV	
COMPONENTS, EXCEPT AS NOTED		CHK		ENGR		CODE IDENT 19333	
TOLERANCE VALUE RATING		MFG		APP		DRAWING NUMBER 54227000	
RES ± 5%	OHM 1/4 W					CD 4	
CAP ± 30%						SHEET 1 OF 2	

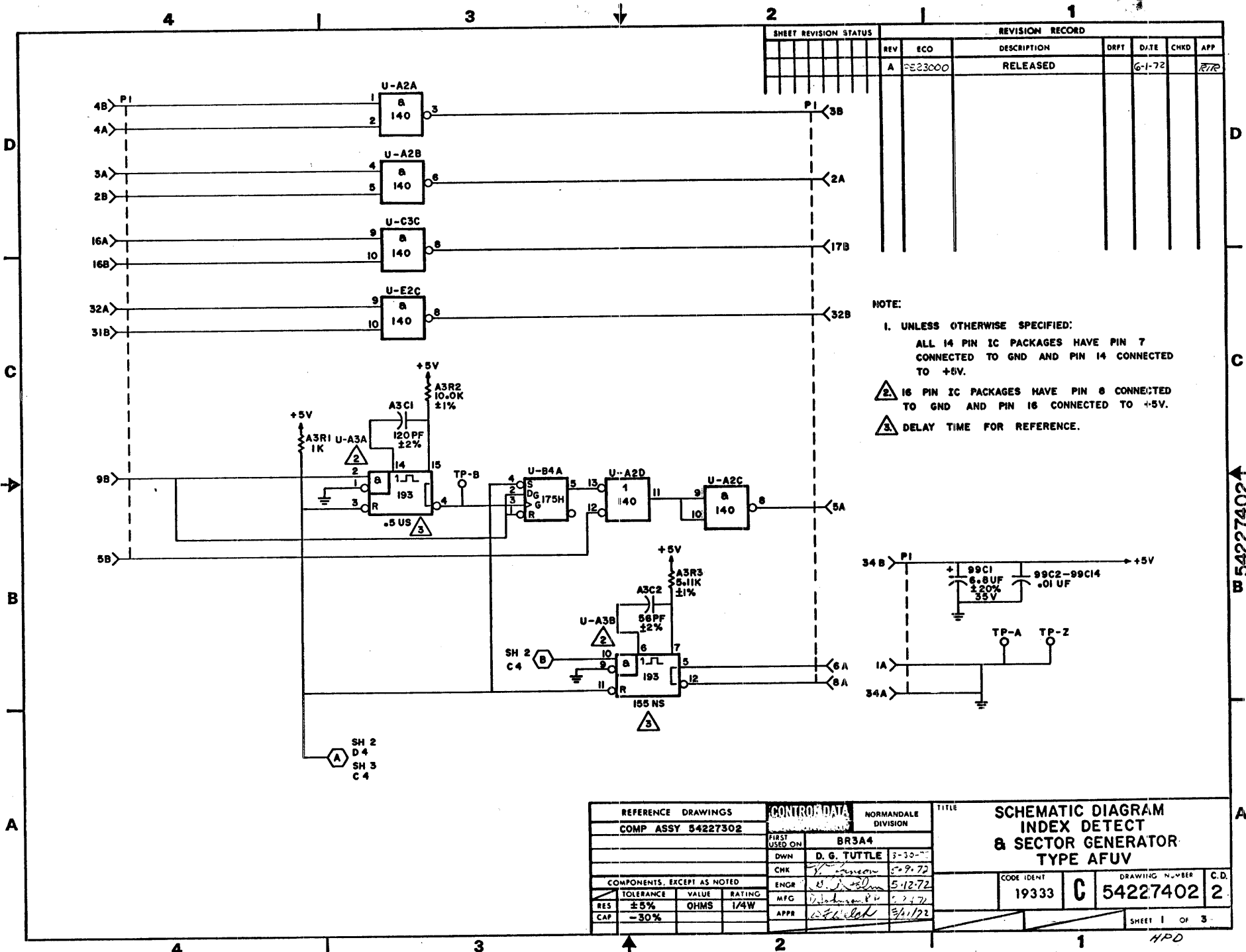
W54227000

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1 FOR REV				



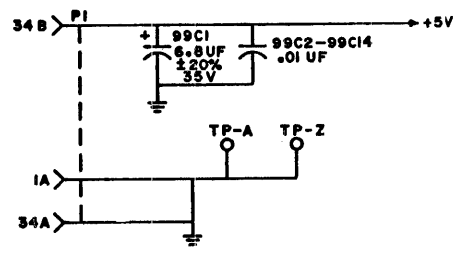
SCHEMATIC DIAGRAM
TYPE 3FTV

CODE IDENT 19333	C	DWG NO 54227000	CD 4
SHEET 2			



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE23000	RELEASED		6-1-72		RTR	

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7
 CONNECTED TO GND AND PIN 14 CONNECTED
 TO +5V.
 2. 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED
 TO GND AND PIN 16 CONNECTED TO +5V.
 3. DELAY TIME FOR REFERENCE.



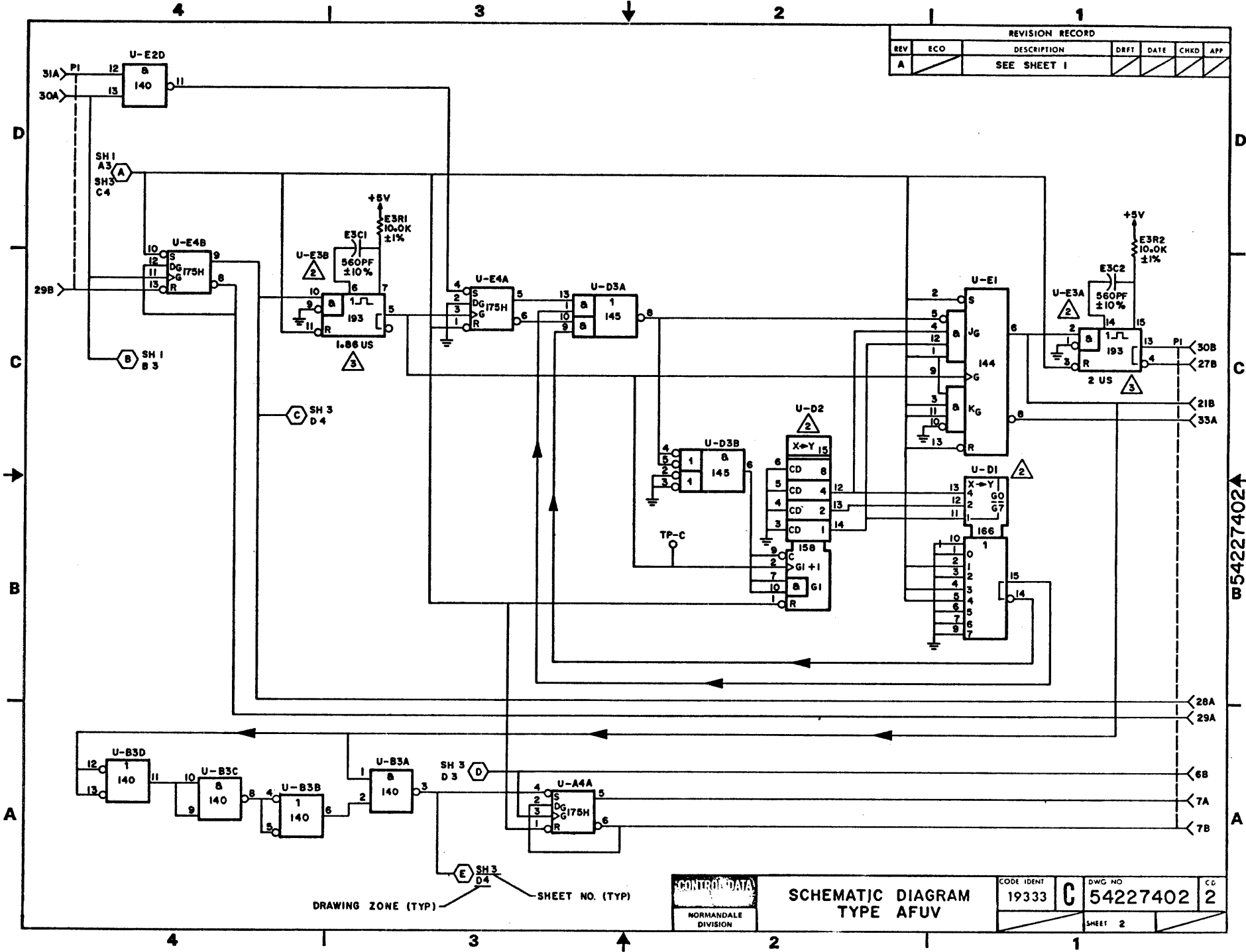
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54227302		FIRST USED ON		BR344		SCHEMATIC DIAGRAM INDEX DETECT & SECTOR GENERATOR TYPE AFUV	
COMPONENTS, EXCEPT AS NOTED		DWN	D. G. TUTTLE	3-30-72	CODE IDENT	DRAWING NUMBER	C.D.
TOLERANCE	VALUE	RATING	ENGR	5-9-72	19333	54227402	2
RES	±5%	OHMS	MFG	5-12-72			
CAP	-30%		APPR	3/1/72			
				SHEET 1 OF 3			

B 54227402

A

HPD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



DRAWING ZONE (TYP)

SHEET NO. (TYP)

CONTROL DATA
NORMANDALE
DIVISION

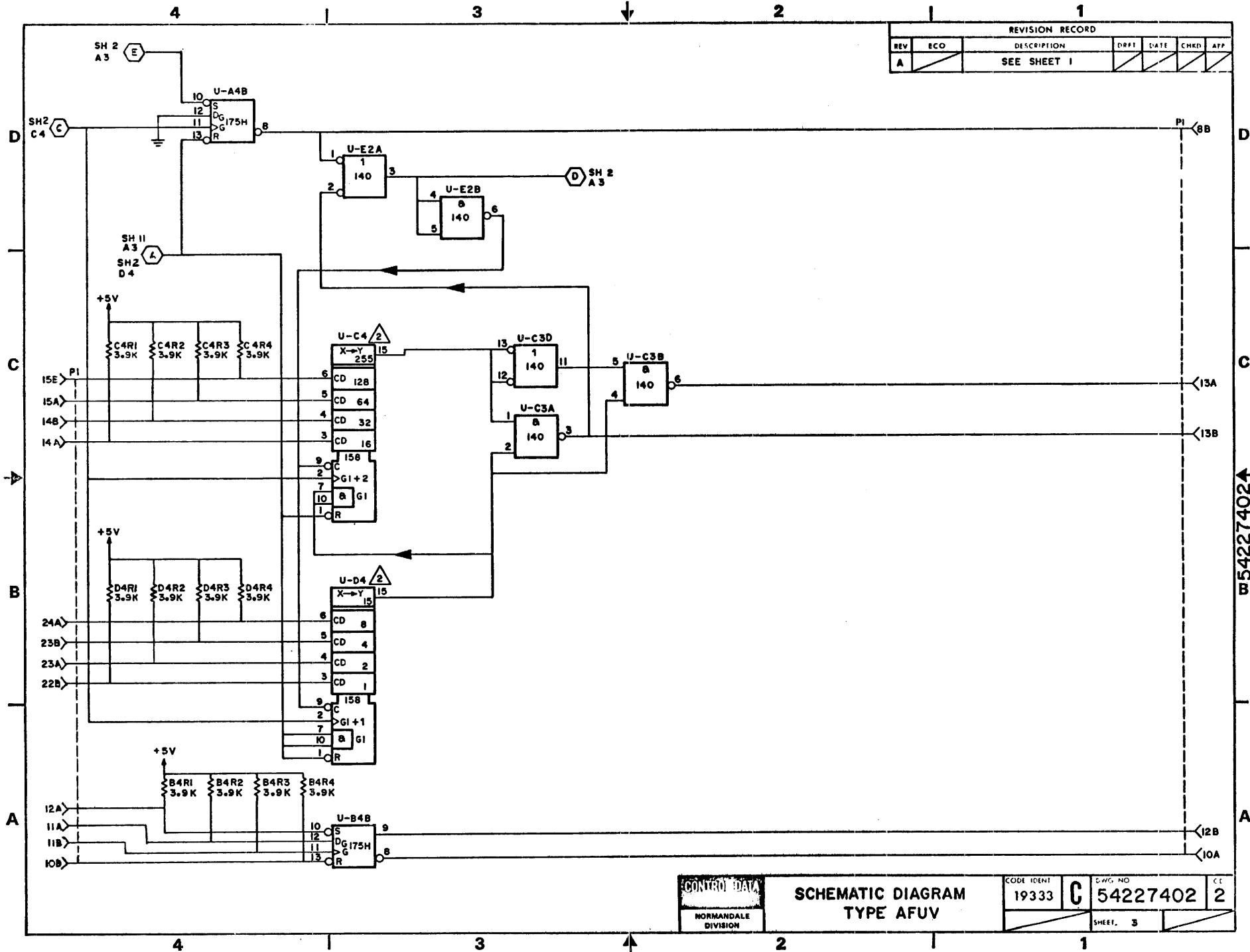
SCHEMATIC DIAGRAM
TYPE AFUV

CODE IDENT 19333	DWG NO C 54227402	CG 2
SHEET 2		

W54227402

70629100 E

4-105



REVISION RECORD						
REV	ECO	DESCRIPTION	DRAW	DATE	CHKD	APP
A		SEE SHEET 1				

CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
TYPE AFU

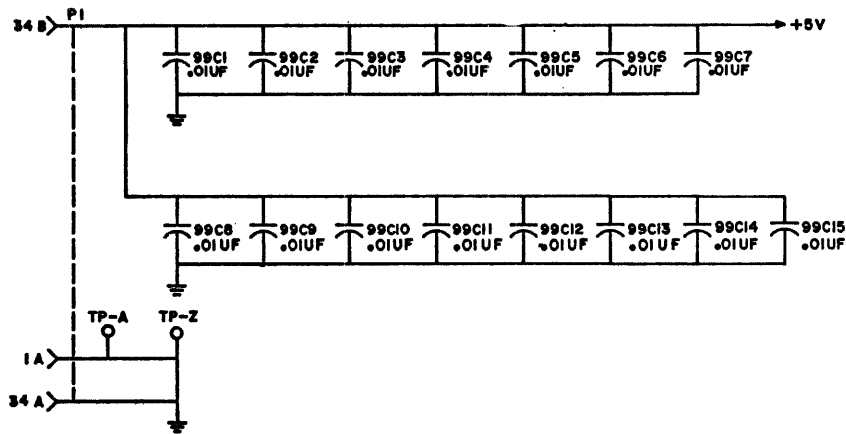
CODE IDENT 19333	DWG NO C 54227402	CC 2
SHEET 3		

54227402

4-106

70629100 E

SHEET REVISION STATUS							REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP					
A	Pe23000	RELEASED									



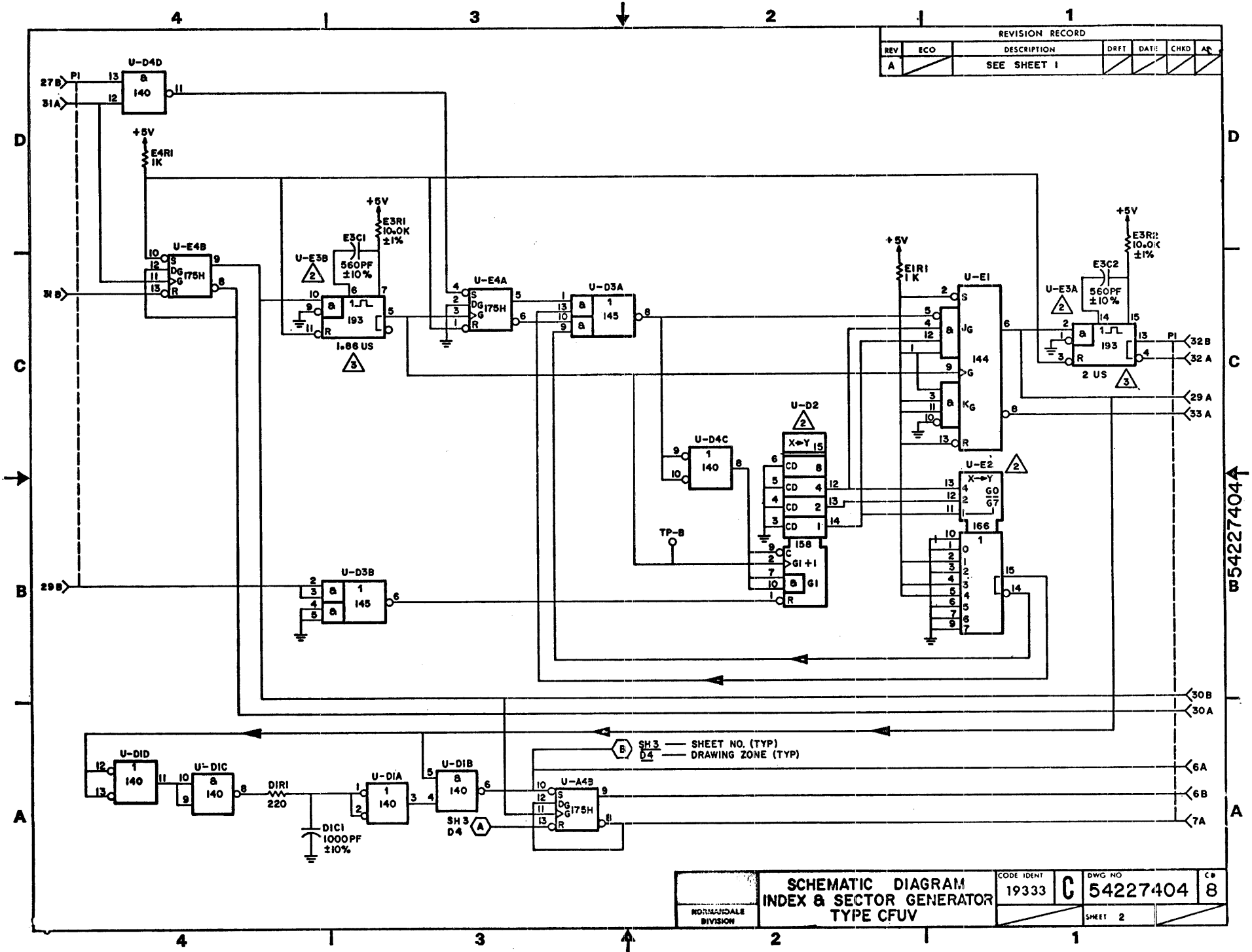
NOTE:

- 1. UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC PACKAGES HAVE PIN 7
CONNECTED TO GND AND PIN 14 CONNECTED
TO +5V.
- ⚠ 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED
TO GND AND PIN 16 CONNECTED TO +5V.
- ⚠ DELAY TIME FOR REFERENCE.

REFERENCE DRAWINGS			NORMANDALE DIVISION		TITLE		
COMP ASSY 54227304			BR3A6		SCHEMATIC DIAGRAM INDEX & SECTOR GENERATOR TYPE CFUV		
COMPONENTS, EXCEPT AS NOTED			FIRST USED ON	DWN	CHK	ENGR	MFG
TOLERANCE	VALUE	RATING					
RES	±5%	OHMS	1/4W				
CAP	-30%						
CODE IDENT					DRAWING NUMBER		C.D.
19333					C 54227404		8
SHEET 1 OF 3							

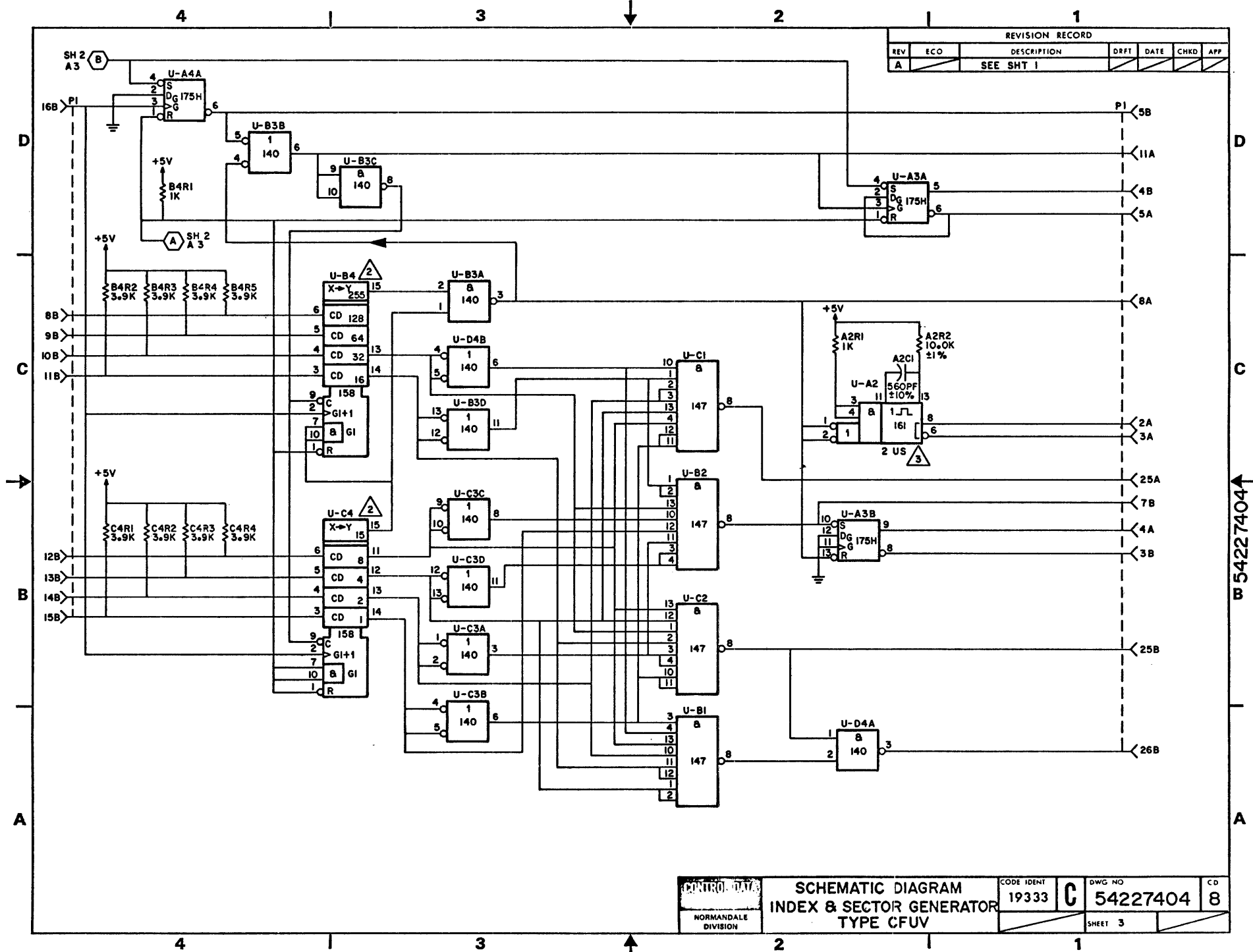
B 54227404

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	AP
A		SEE SHEET 1				



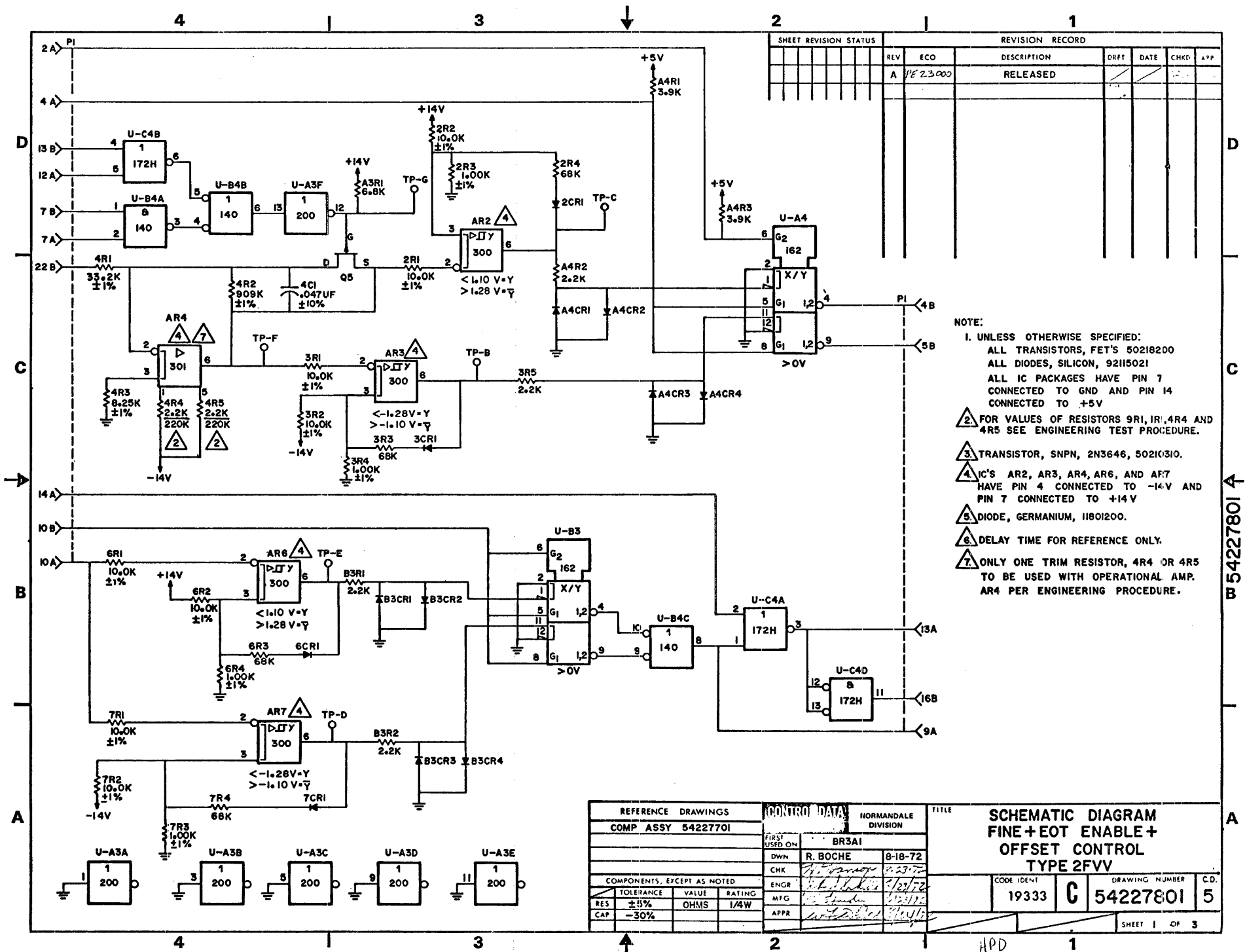
NORMANVILLE DIVISION	SCHEMATIC DIAGRAM INDEX & SECTOR GENERATOR TYPE CFUV		CODE IDENT 19333	DWG NO 54227404	C# 8
				SHEET 2	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1				



CONTROL DIVISION NORMANDALE DIVISION	SCHEMATIC DIAGRAM INDEX & SECTOR GENERATOR TYPE CFUV		CODE IDENT 19333	DWG NO 54227404	CD 8
			SHEET 3		

W 54227404

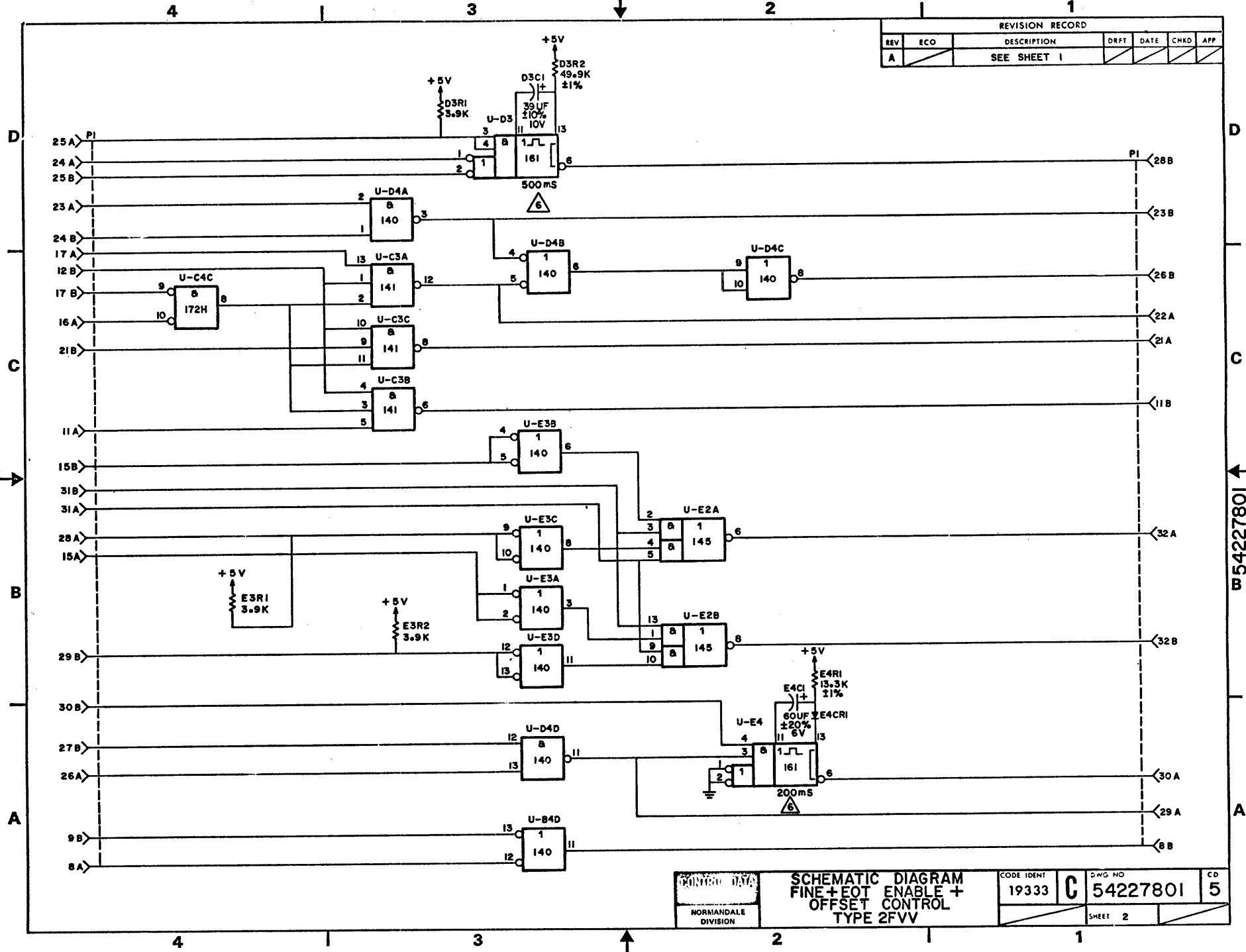


SHEET REVISION STATUS			REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	VE 2.3.000	RELEASED					

- NOTE:
1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, FET'S 50218200
 ALL DIODES, SILICON, 92115021
 ALL IC PACKAGES HAVE PIN 7
 CONNECTED TO GND AND PIN 14
 CONNECTED TO +5V
 2. FOR VALUES OF RESISTORS 9R1, 1R1, 4R4 AND
 4R5 SEE ENGINEERING TEST PROCEDURE.
 3. TRANSISTOR, SNPN, 2N3646, 5021K1310.
 4. IC'S AR2, AR3, AR4, AR6, AND AF7
 HAVE PIN 4 CONNECTED TO -14V AND
 PIN 7 CONNECTED TO +14V
 5. DIODE, GERMANIUM, 11801200.
 6. DELAY TIME FOR REFERENCE ONLY.
 7. ONLY ONE TRIM RESISTOR, 4R4 OR 4R5
 TO BE USED WITH OPERATIONAL AMP.
 AR4 PER ENGINEERING PROCEDURE.

REFERENCE DRAWINGS		NORMANDELE DIVISION		TITLE	
COMP ASSY 5422701		BR3A1		SCHEMATIC DIAGRAM FINE + EOT ENABLE + OFFSET CONTROL TYPE 2FVV	
FIRST USED ON		DWN R. BOCHE		8-18-72	
CHK		ENGR		CODE IDENT	
COMPONENTS, EXCEPT AS NOTED		MFG		DRAWING NUMBER	
TOLEANCE	VALUE	RATING	APPR	19333	54227801
RES ±5%		OHMS			
CAP -30%		1/4W			

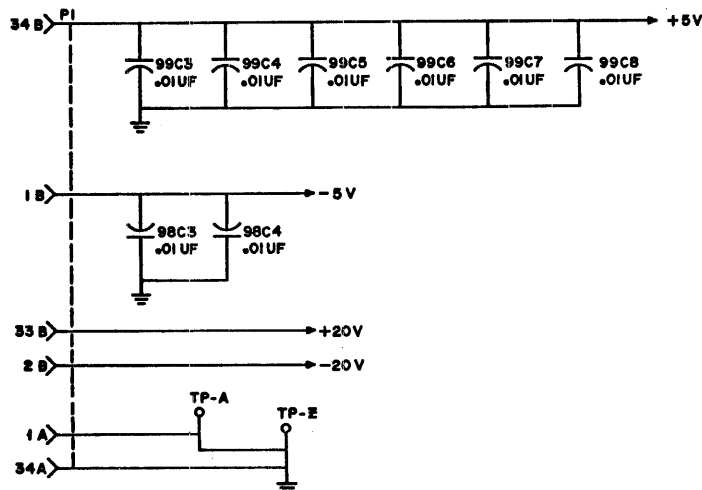
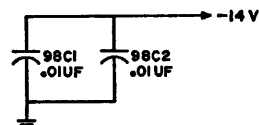
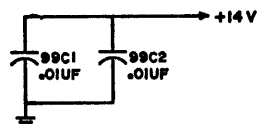
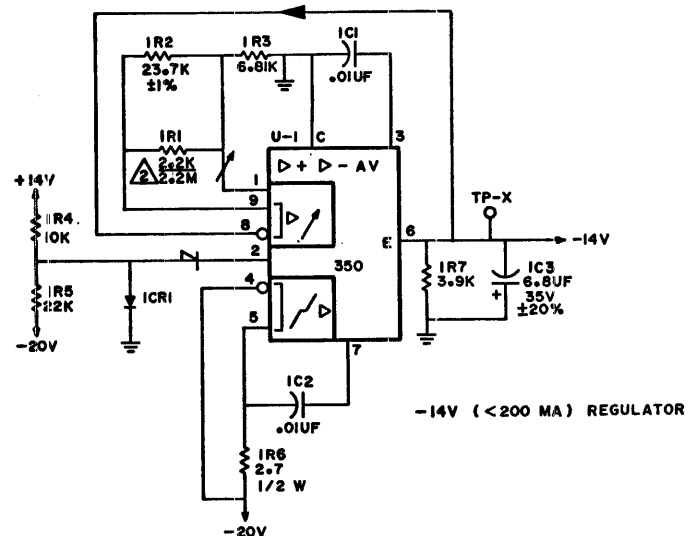
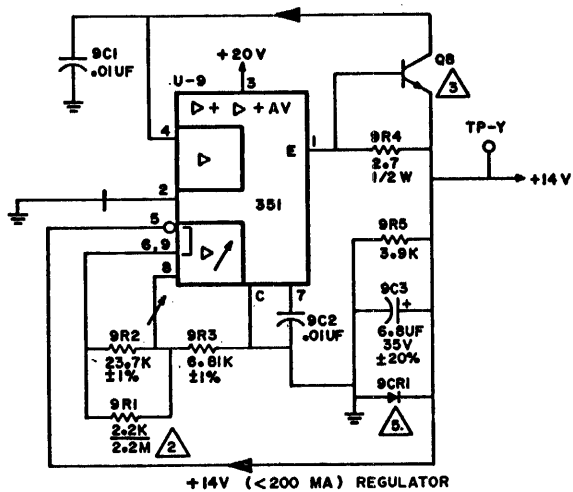
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET I				



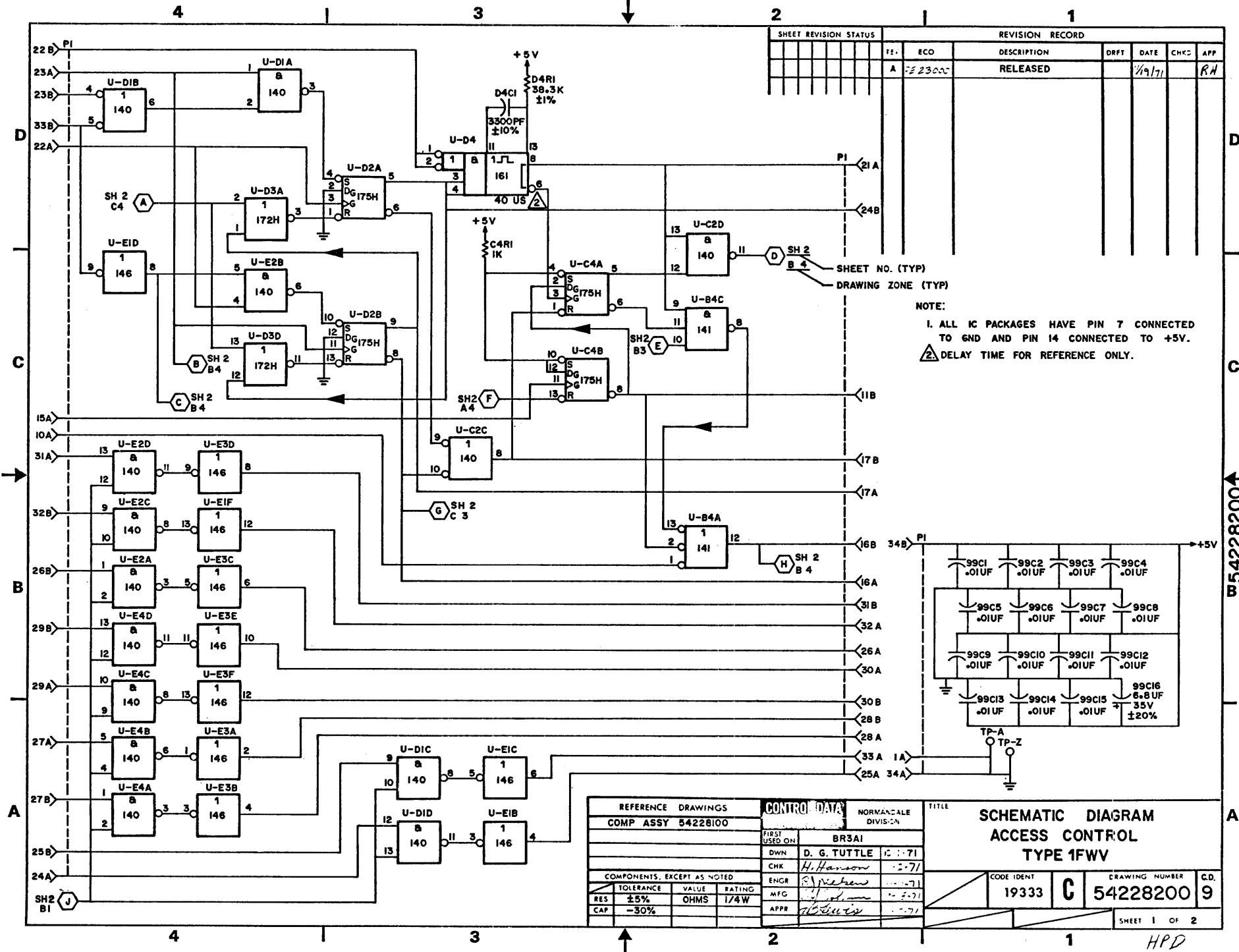
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM FINE+EOT ENABLE + OFFSET CONTROL TYPE 2FVV		CODE IDENT 19333	DWG NO C 54227801	CD 5
			SHEET 2		

108227801

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



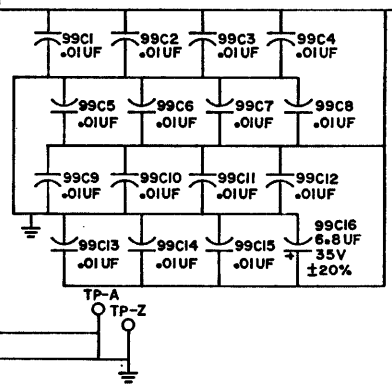
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM FINE + EOT ENABLE + OFFSET CONTROL TYPE 2FVV		CODE IDENT 19333	DWG NO 54227801	CD 5
			SHEET 3		



SHEET REVISION STATUS		REVISION RECORD					
REV.	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23000	RELEASED		7/17		RH	

SHEET NO. (TYP)
DRAWING ZONE (TYP)

NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
△ DELAY TIME FOR REFERENCE ONLY.

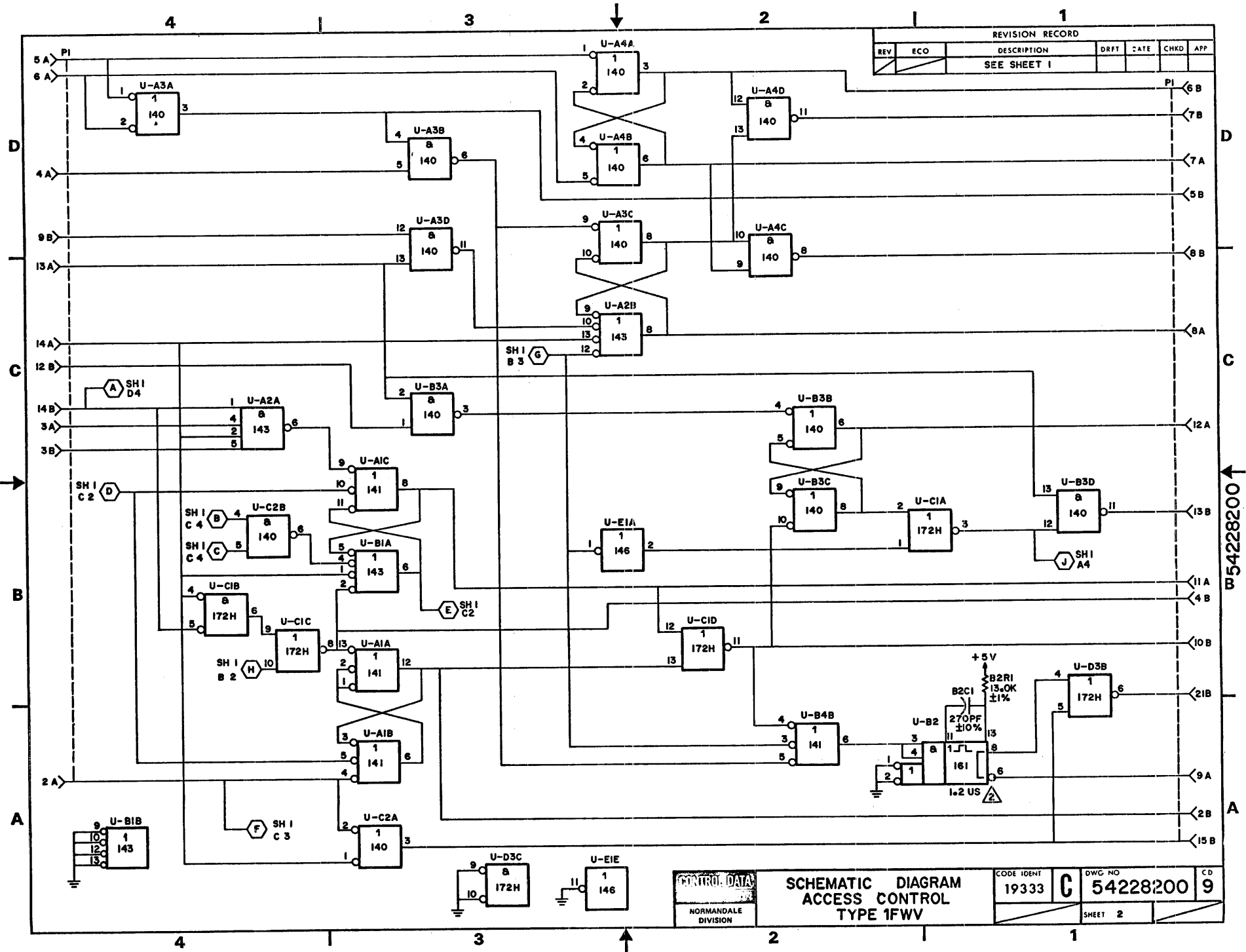


REFERENCE DRAWINGS		CONTROL DATA		NORMAN CALE DIVISION	
COMP ASSY 54228100		FIRST USED ON	BR3A1		
		DWN	D. G. TUTTLE 10-71		
		CHK	H. Hanson 11-71		
		ENGR	R. Nelson 11-71		
		MFG	1-5-71		
		APPR	11-71		

TITLE			
SCHEMATIC DIAGRAM ACCESS CONTROL TYPE 1FWV			
CODE IDENT	DRAWING NUMBER	G.D.	
19333	C 54228200	9	
SHEET 1 OF 2			

HPD

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1				



CONTROL DATA
NORMANDEALE
DIVISION

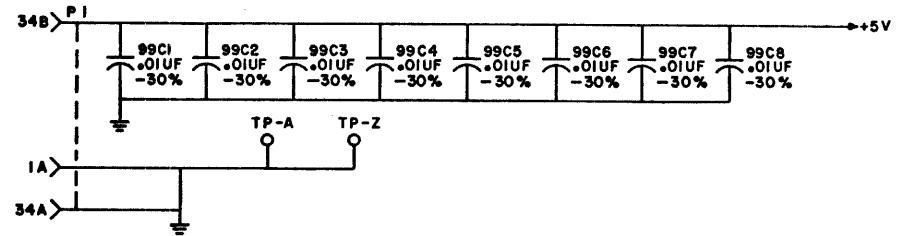
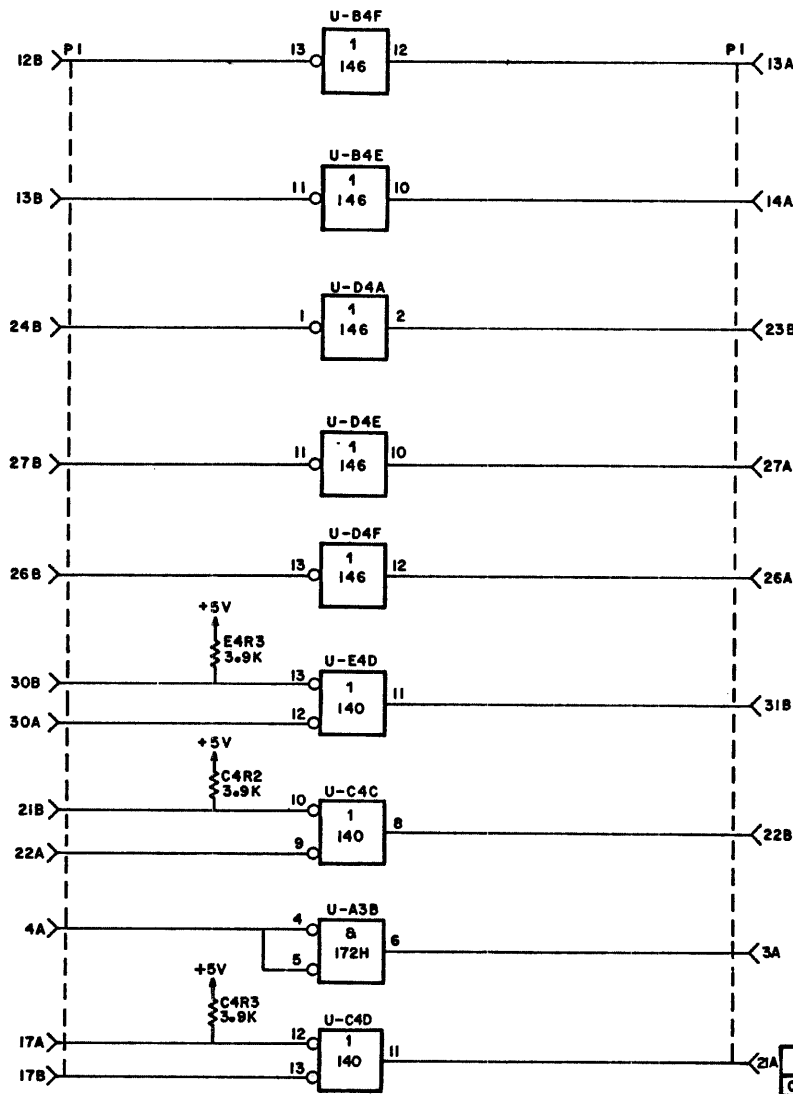
SCHEMATIC DIAGRAM
ACCESS CONTROL
TYPE 1FVW

CODE IDENT 19333	DWC NO 54228200	CD 9
SHEET 2		

W54228200

SHEET REVISION STATUS										REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP							
A	FE23000	RELEASED		3-22-72		TR							

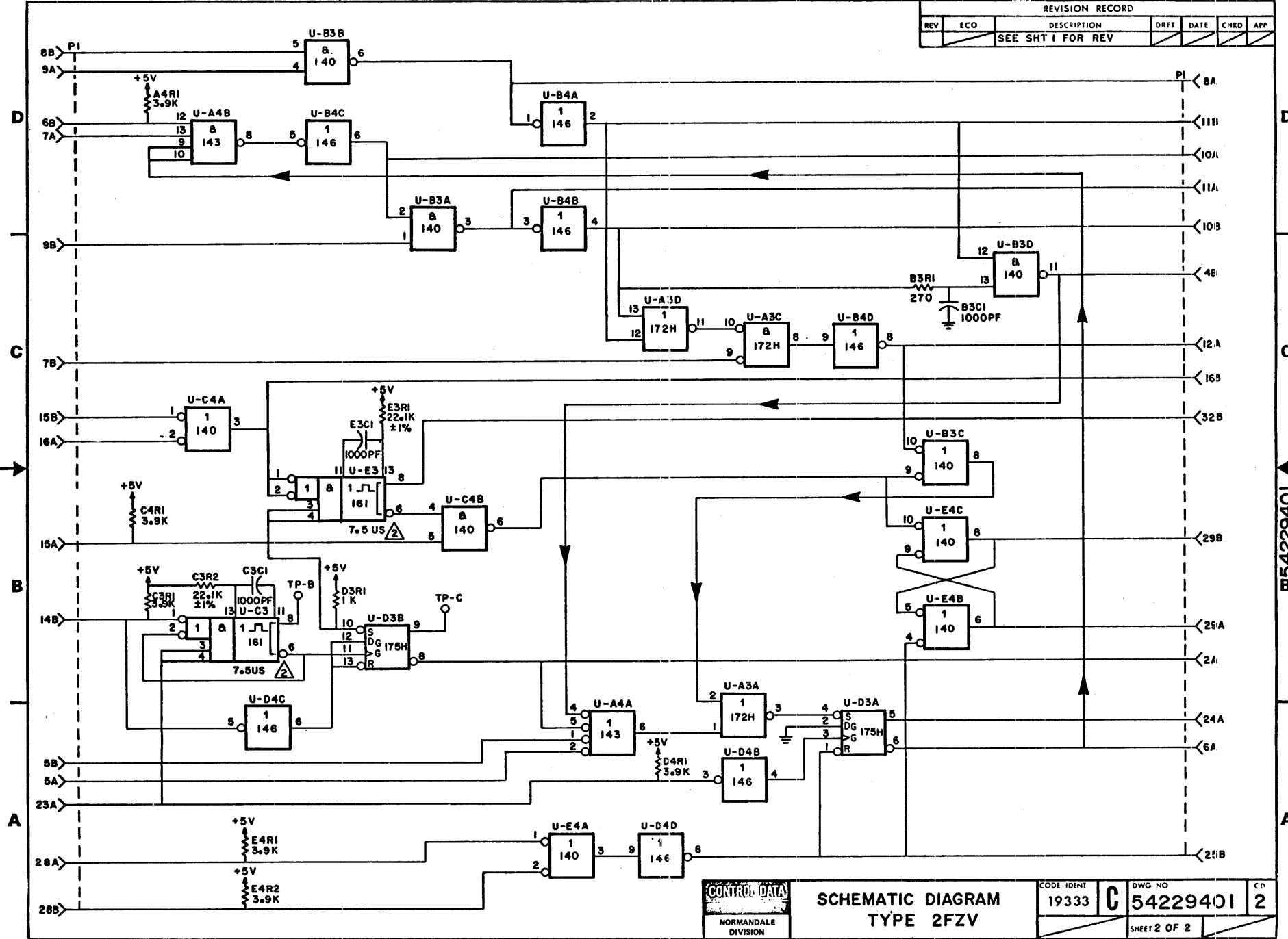
NOTE:
 1 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2 DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY	54229501	FIRST USED ON	BR 3AIG			SCHEMATIC DIAGRAM R/W/E ENABLE AND FAULT DETECTION TYPE 2FZV	
COMPONENTS, EXCEPT AS NOTED		DWN	<i>Diagrams</i>	2-11-72			
TOLERANCE		CHK	<i>2/28-72</i>	3-10-72			
RES ±5%	VAR. ±	ENGR	<i>RR W/GSP</i>	3-10-72			
CAP ±10%	OHMS	MFG	<i>Norman RD</i>	3-22-72			
	RATING	APPR	<i>J. J. [Signature]</i>	3-20-72			
	174 W	CODE IDENT		19333	DRAWING NUMBER	54229401	CD
		SHEET 1 OF 2				2	

HPD

REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD APP
		SEE SHT 1 FOR REV			



CONTROL DATA
NORMANDALE DIVISION

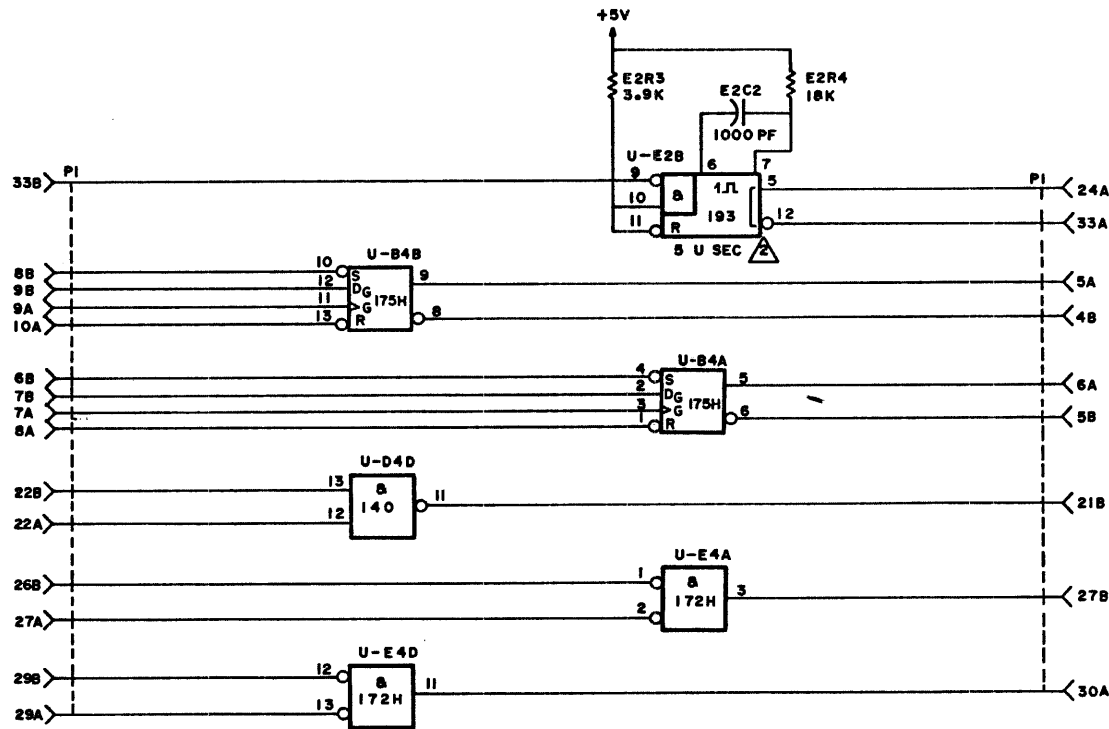
SCHEMATIC DIAGRAM
TYPE 2FZV

CODE IDENT 19333	DWG NO C 54229401	CP 2
SHEET 2 OF 2		

4-116

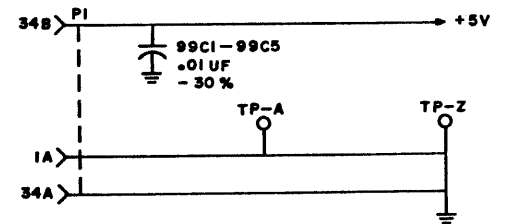
70629100 E

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE2300	RELEASED			2-20-73	3/77	



NOTES:

- UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S MUST HAVE PIN 7
CONNECTED TO GROUND AND PIN 14 TO +5V.
- △ DELAY TIME FOR REFERENCE ONLY.

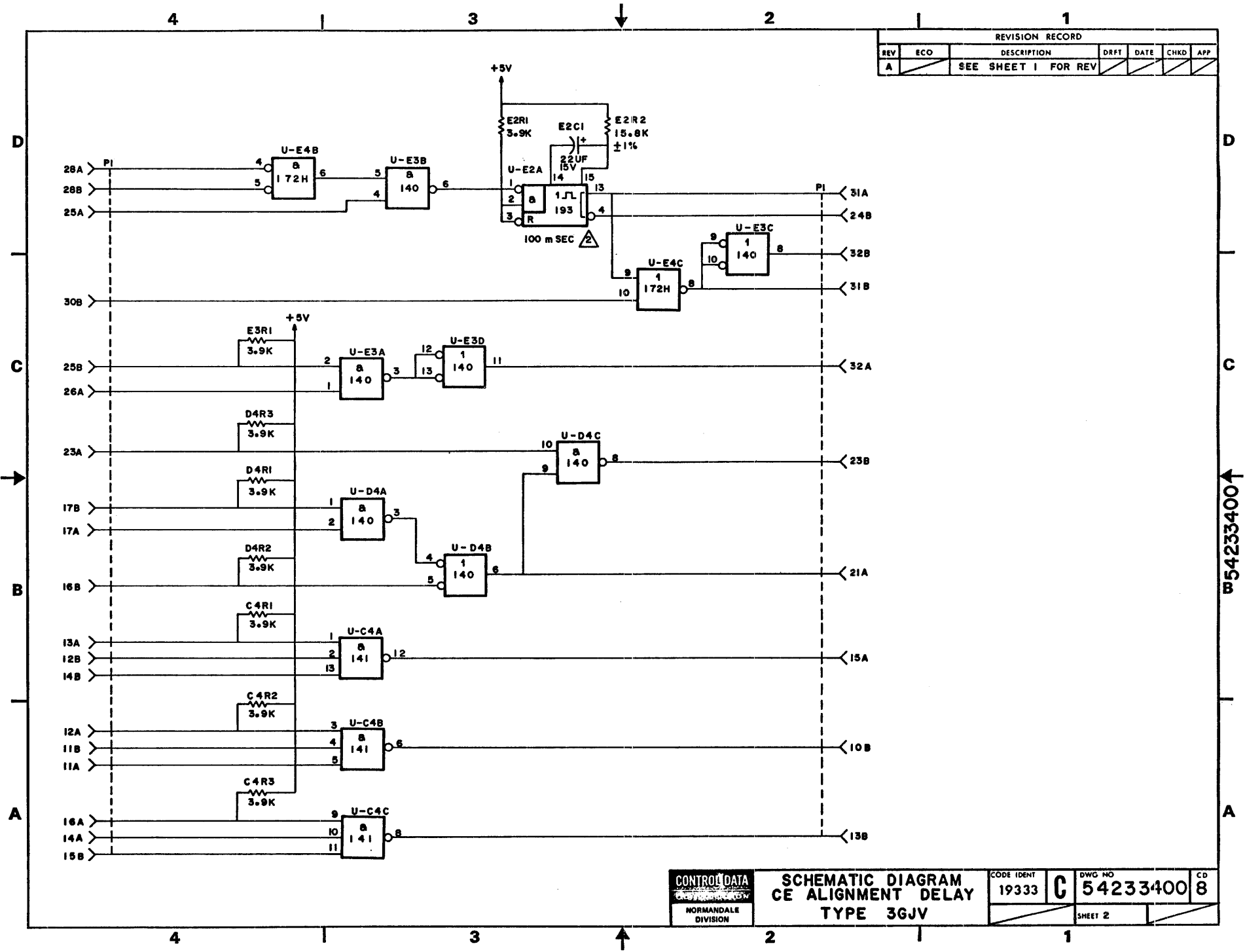


REFERENCE DRAWINGS		CONTROLDATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54233300		FIRST USED ON BR3AG				SCHEMATIC DIAGRAM CE ALIGNMENT DELAY TYPE 3GJV	
		DWN R. RICHTER 1-18-73				CODE IDENT 19333 C	
		CHK <i>Z. Hansen</i> 1-31-73				DRAWING NUMBER 54233400 8	
		ENGR <i>Z. Hansen</i> 1-31-73				SHEET 1 OF 2	
		MFG <i>Z. Hansen</i> 2-5-73				-HPD-	
		APPR <i>S. S. Williams</i> 2-9-73					
COMPONENTS, EXCEPT AS NOTED							
TOLERANCE	VALUE	RATING					
RES ± 5%	OHMS	1/4 W					
CAP ± 10%							

70629100 E

4-117

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
CE ALIGNMENT DELAY
TYPE 3GJV

CODE IDENT 19333	C	DWG NO 54233400	CD 8
		SHEET 2	

4-118

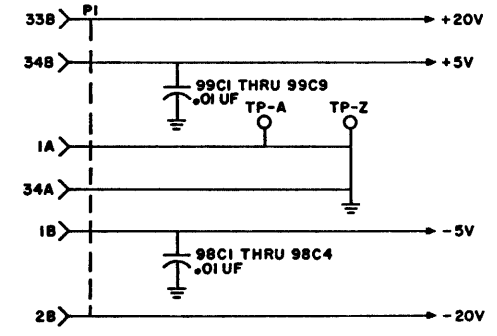
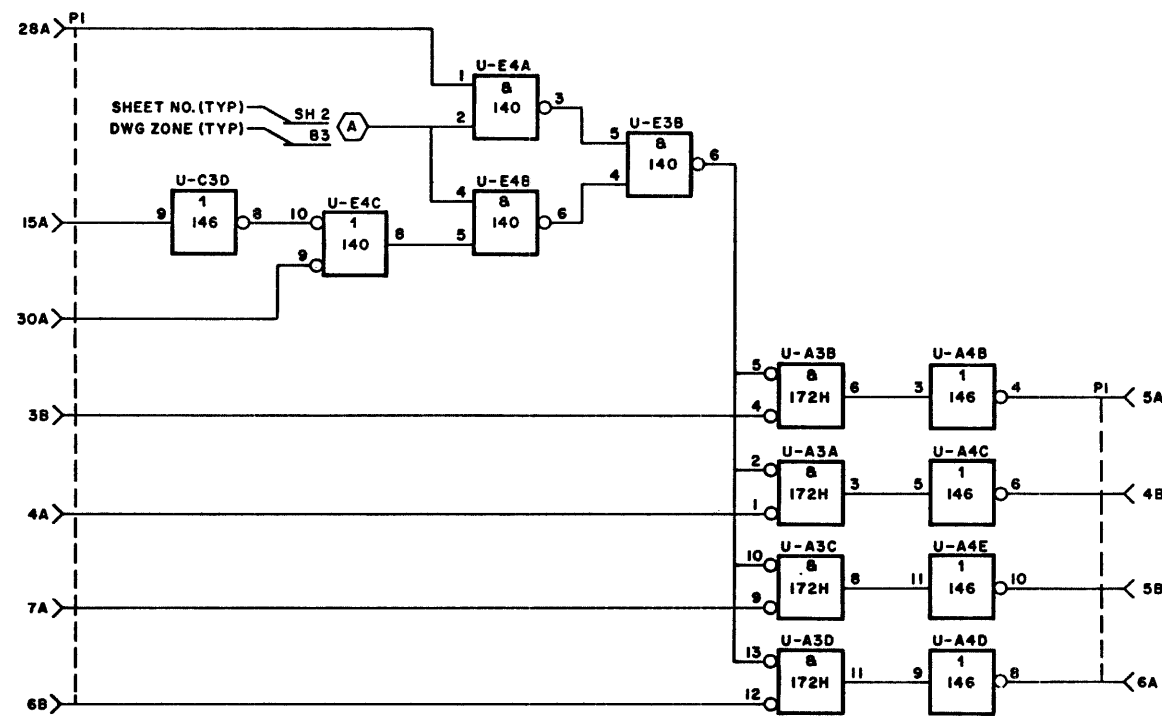
70629100 E

SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE30914	RELEASED							
B	PE30914	CONNECTOR PIN CHANGED FROM 6B TO 6A.	RKR	1-16	ell	II			
C	PE34116	CHANGED INDUCTOR VALUE TO 47 mH	R.K.	1-19-73	ell	I			

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL 14 PIN I-C'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V. ALL 16 PIN I-C'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V. ALL TRANSISTORS, SNPN, PLANAR, 24562100. ALL DIODES, SILICON, 24553500.

- Ⓐ TRANSISTOR, SNPN, 2N3642, 50210510.
- Ⓑ TRANSISTOR, SNPN, 2N3645, 50211210.
- Ⓒ DIODE, SILICON, 92115023.
- Ⓓ DIODE, SILICON, 92115021.
- Ⓔ I-C A2, B2, C2, D2, AND E2 HAVE PIN 13 CONNECTED TO -5V.
- Ⓕ I-C U-EI HAS PIN 4 CONNECTED TO -5V AND PINS 9 AND 13 CONNECTED TO +5V.
- Ⓖ DIODE, GERMANIUM, 11801200.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASS'Y 54233700		BR3A6				SCHEMATIC DIAGRAM STATIC DIAGNOSTIC TYPE 2GKV	
		DWN S. ZAK 10-2-72				CODE IDENT 19333 C	
		CHK [Signature] 10-10-72				DRAWING NUMBER 54233800 9	
COMPONENTS, EXCEPT AS NOTED		ENGR: [Signature] 10-10-72				C.D.	
TOLERANCE	VALUE	RATING	MFG				
RES +5%	OHMS	1/4W	[Signature]				
CAP -30%			[Signature]				
		APPR [Signature] 10-2-72				SHEET 1 OF 4	

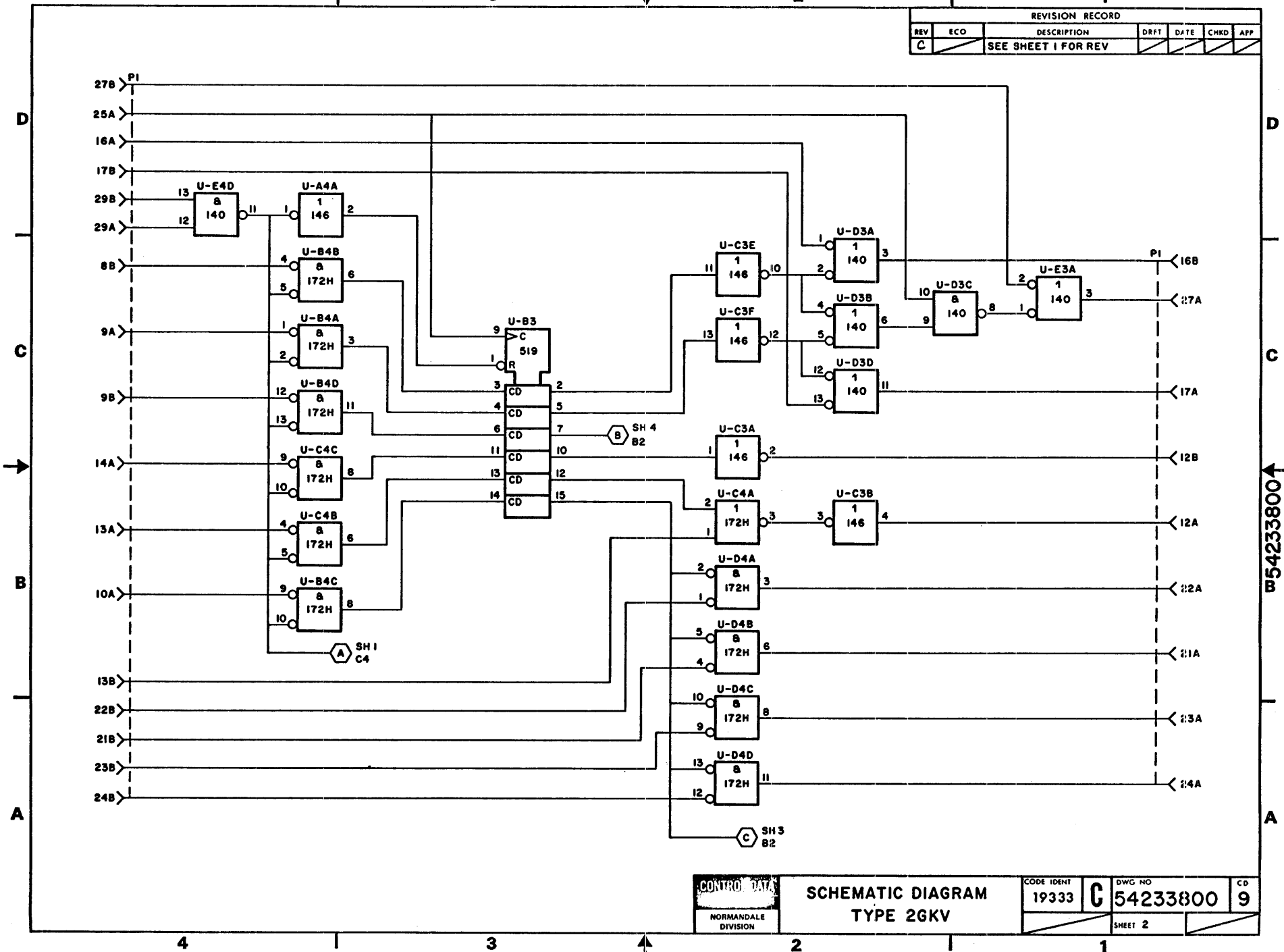
HPD 1

54233800

70629100 E

4-119

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
C		SEE SHEET I FOR REV				

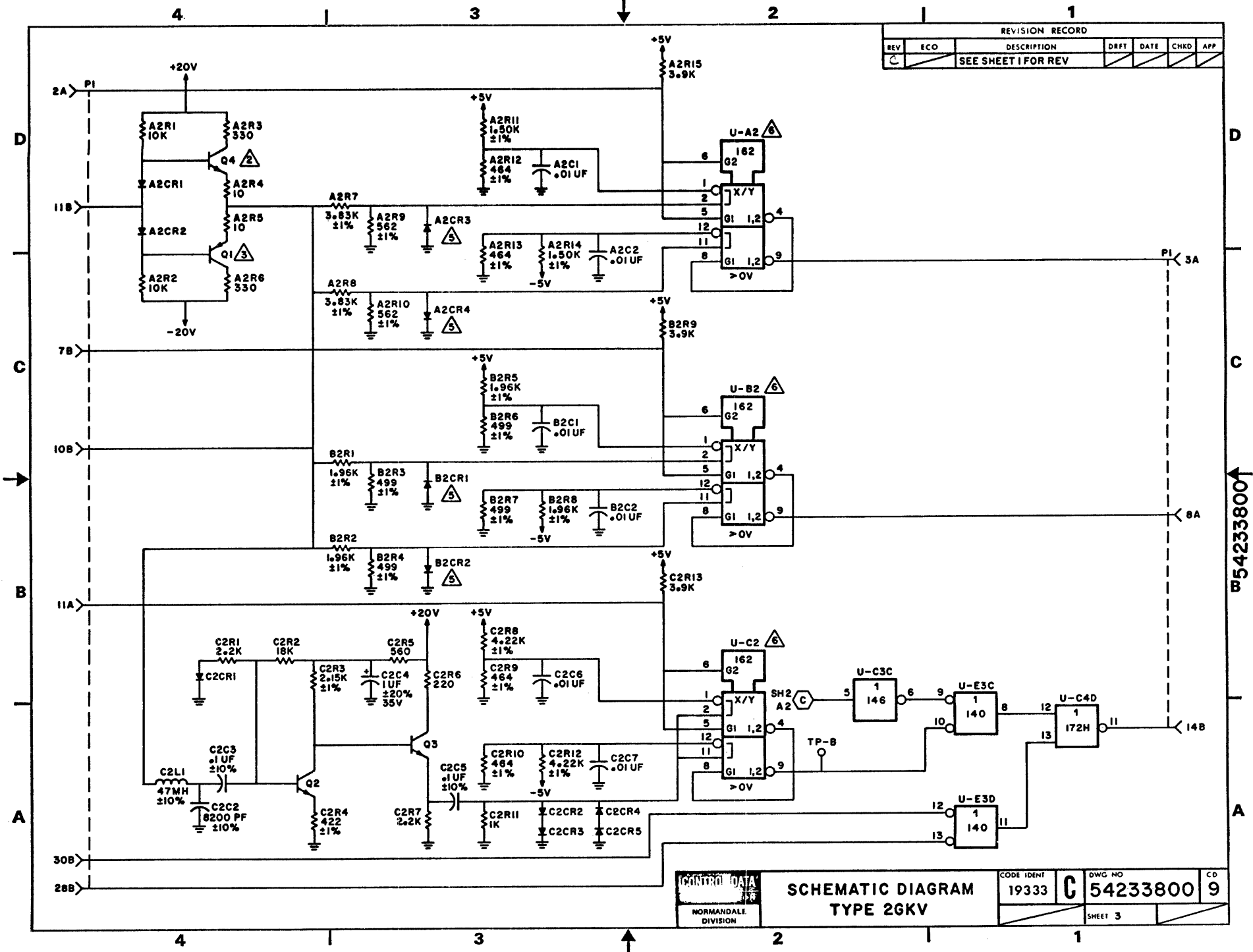


CONTROL DATA
NORMANDE
DIVISION

SCHEMATIC DIAGRAM
TYPE 2GKV

CODE IDENT 19333	DWG NO 54233800	CD 9
SHEET 2		

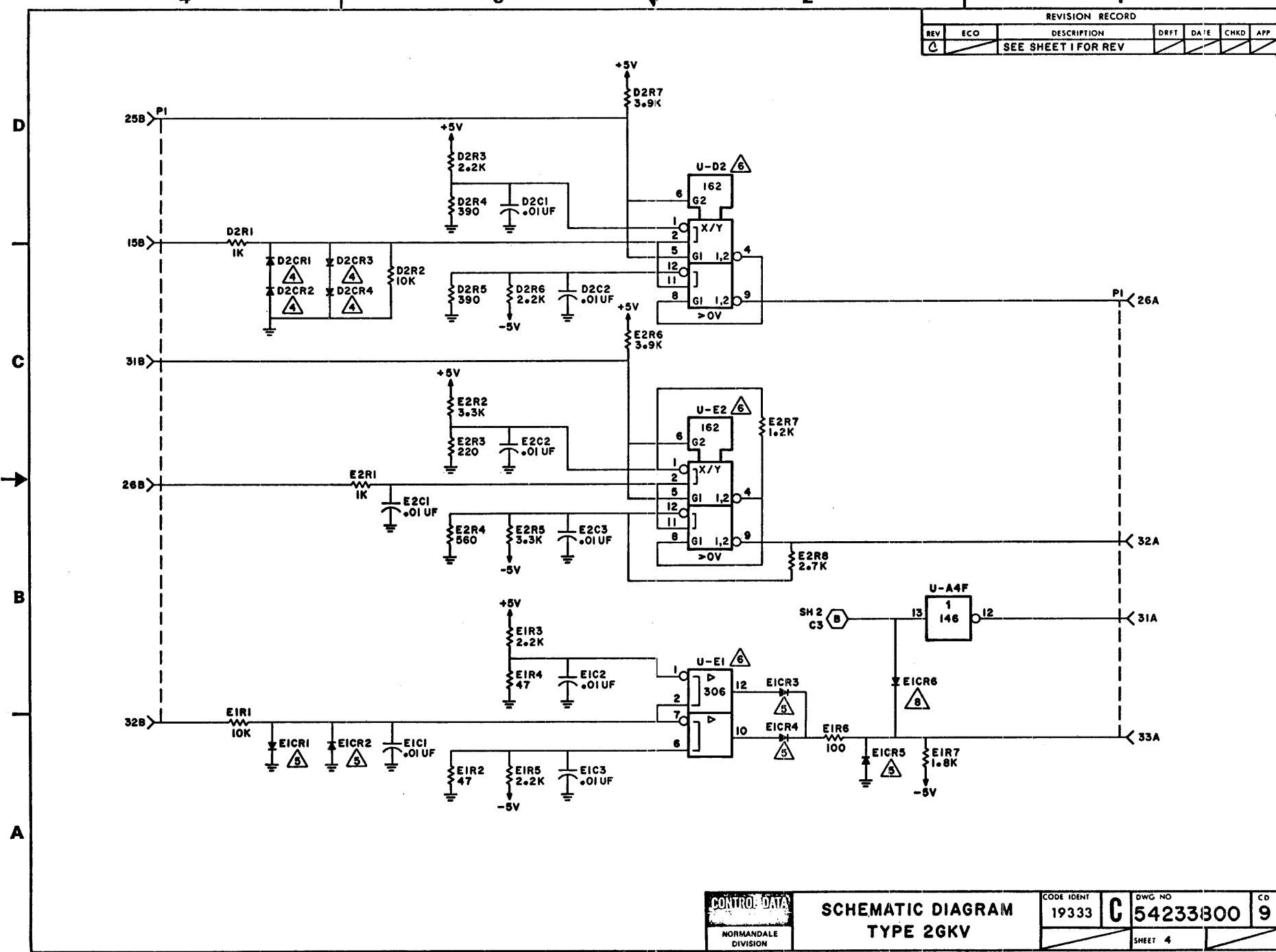
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
C		SEE SHEET I FOR REV				



CONTROL DATA NORMANDALL DIVISION	SCHEMATIC DIAGRAM TYPE 2GKV		CODE IDENT 19333	DWG NO C 54233800	CD 9
			SHEET 3		

54233800

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
1		SEE SHEET 1 FOR REV				



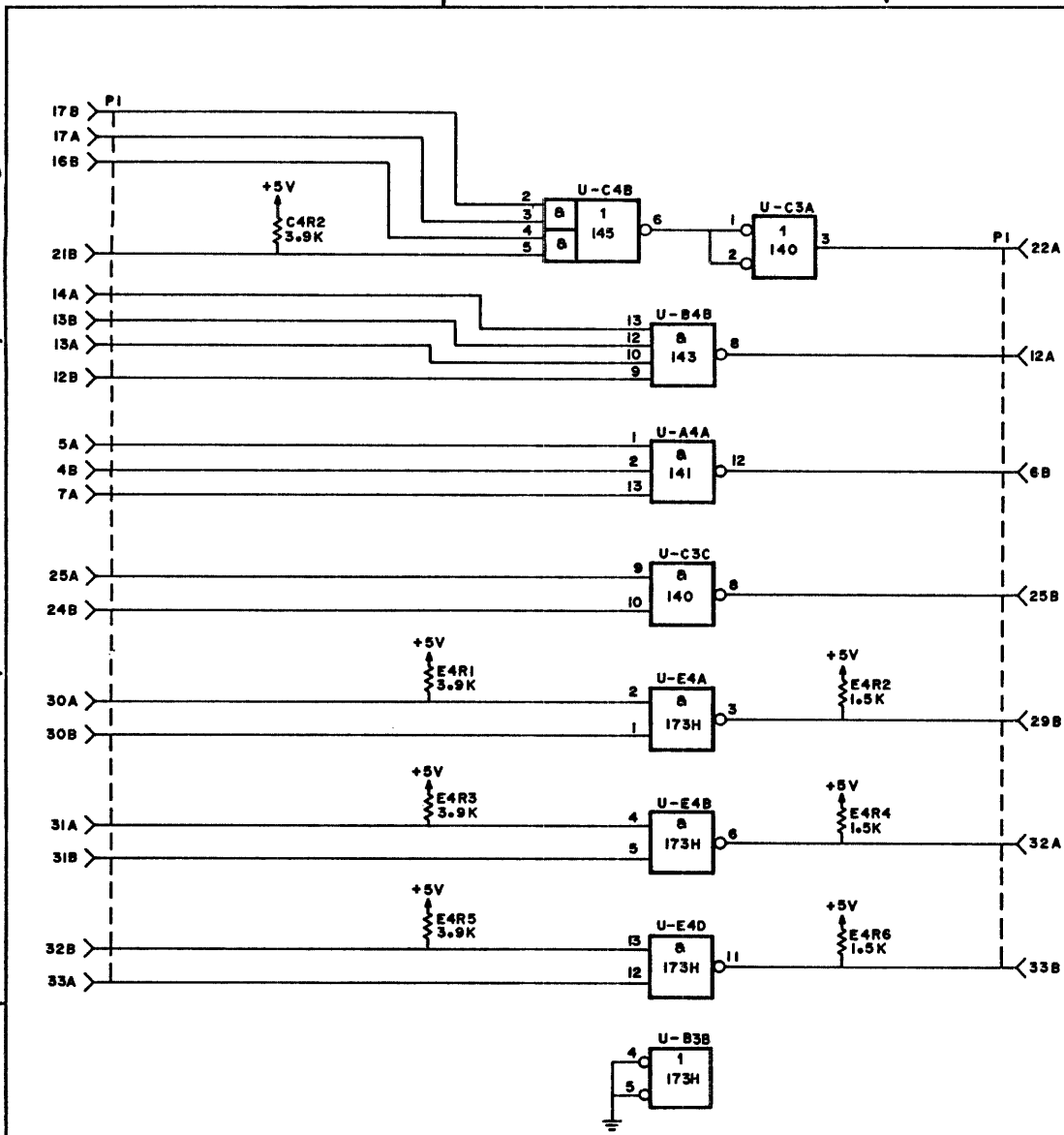
CONTROL DATA
NORMANDEALE
DIVISION

**SCHEMATIC DIAGRAM
TYPE 2GKV**

CODE IDENT 19333	DWG NO C 54233800	CD 9
SHEET 4		

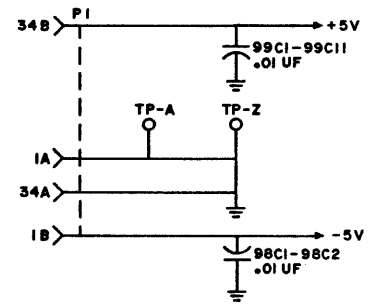
4-122

70629100 E



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					
B	PE30970	CHANGE GND TO -5V	RB	12-8-72	EEB	III	

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SNPN, 2N3646, 50210310.
ALL DIODES, SILICON, 92115021.
 - TRANSISTOR, SNPN, 2N4916, 50211610.
 - TRANSISTOR, SNPN, 2N3568, 50210810.
 - DIODE, ZENER, 50240108.
 - ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - VALUE OF D4R1 TO BE SELECTED IN PRODUCTION TO GIVE A PULSE OF 55 US ± 7 US AT TEST POINT G.
 - VALUE OF 2R1 TO BE SELECTED IN PRODUCTION TO DETECT A SPEED OF 3000 R. P. M. ± 300 R.P.M.
 - DELAY TIME FOR REFERENCE ONLY
 - ARIO HAS PIN 7 CONNECTED TO +5V AND PIN 4 CONNECTED TO -5V.

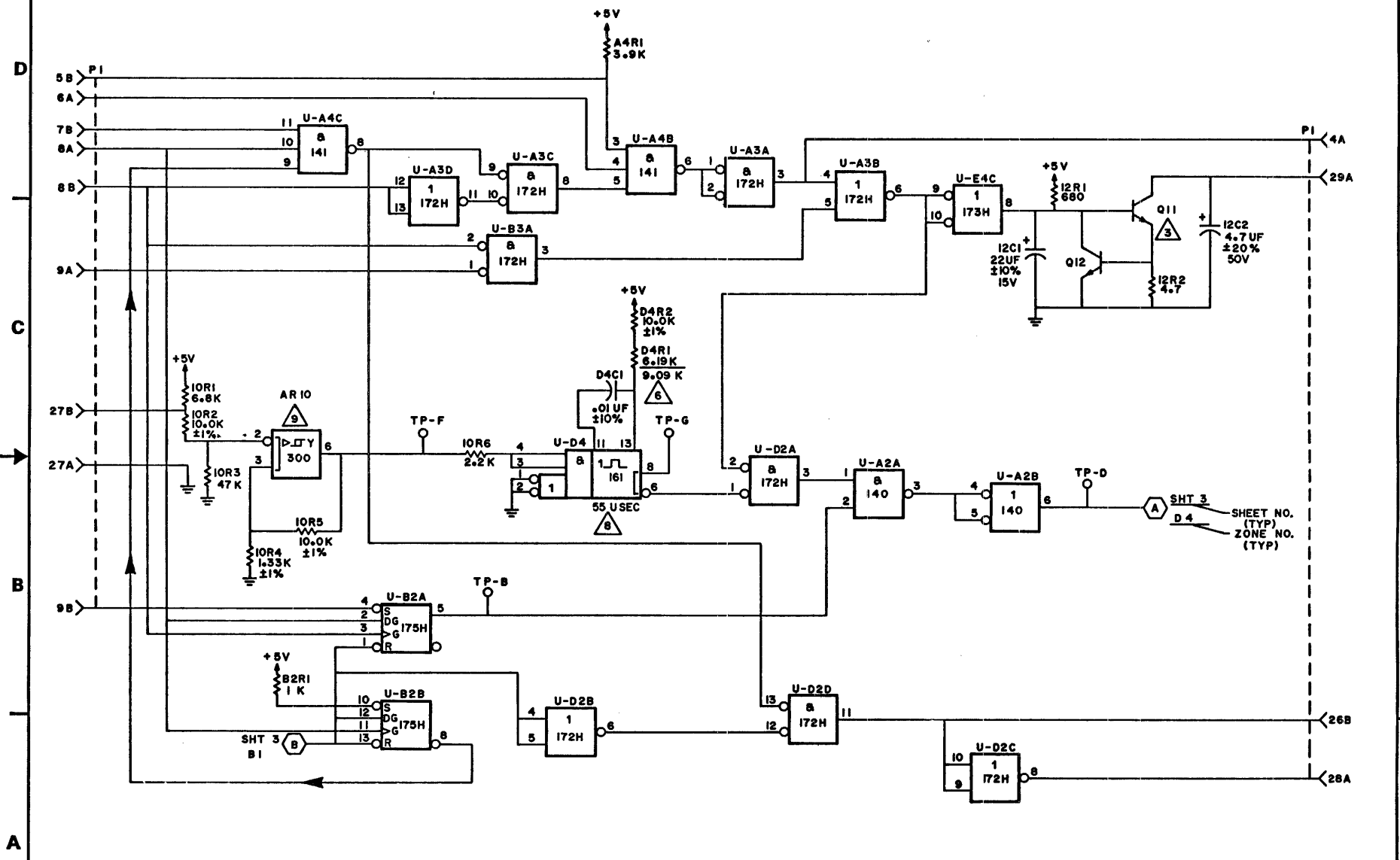


REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMP ASSY	54234100	FIRST USED ON	BR3A6			SCHEMATIC DIAGRAM	
		DWN	V. STEETEL	3-2-72		MOTOR CONTROL & SPEED DETECTOR	
		ENGR				TYPE 2GLV	
COMPONENTS, EXCEPT AS NOTED		MFG		3-7-72		CODE IDENT	DRAWING NUMBER
RES	TOLERANCE	VALUE	RATING			19333	54234200
	± 5%	OHMS	1/4 W			C	1
CAP	-30%						
		APPR				SHEET 1 OF 3	

HPD

W54234200

REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD APP
B		SEE SHT 1 FOR REV			



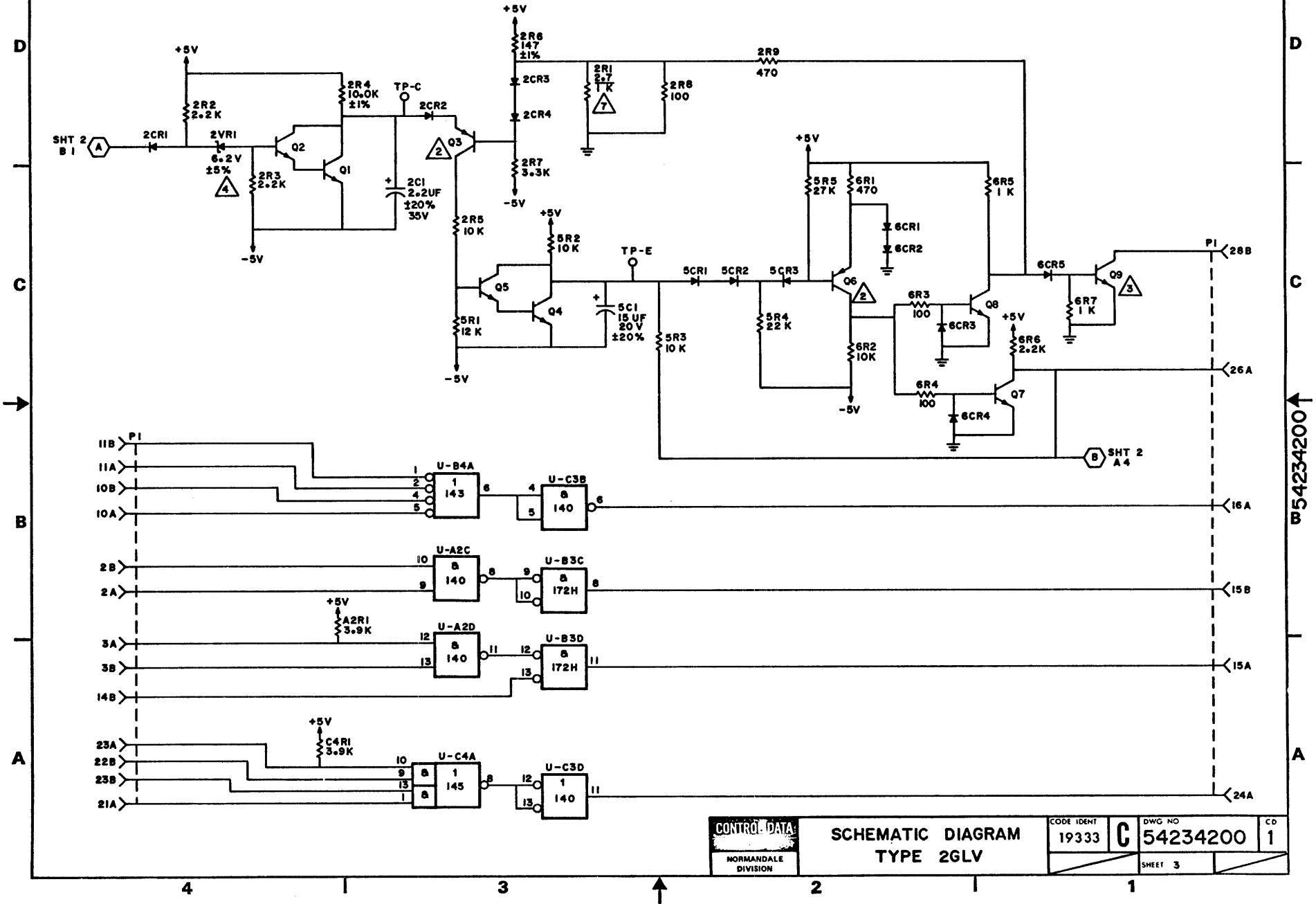
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 2GLV		CODE IDENT 19333	DWG NO 54234200	CD 1
			SHEET 2		

B54234200

4-124

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHT 1 FOR REV				

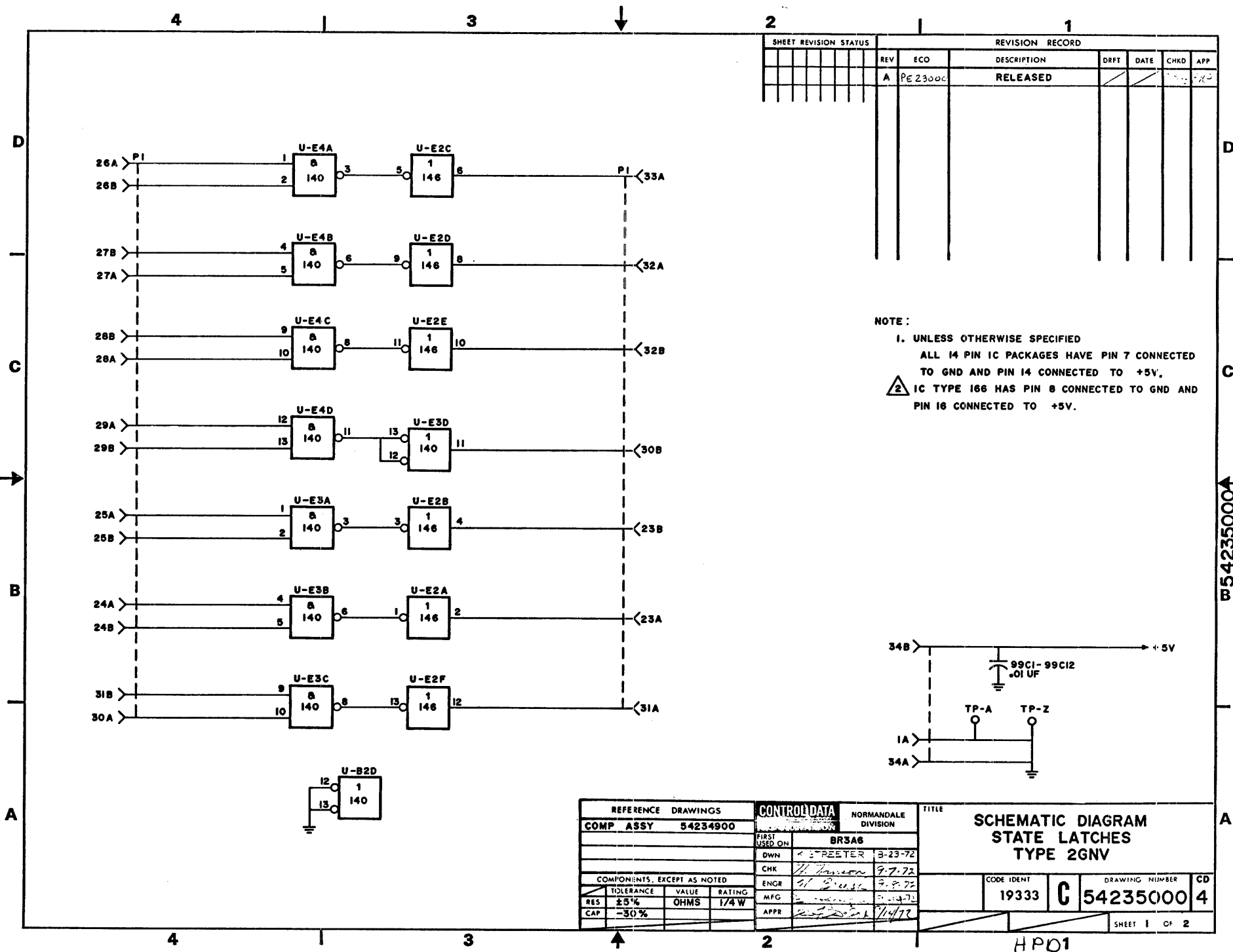


CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
TYPE 2GLV

CODE IDENT 19333	DWG NO 54234200	CD 1
SHEET 3		

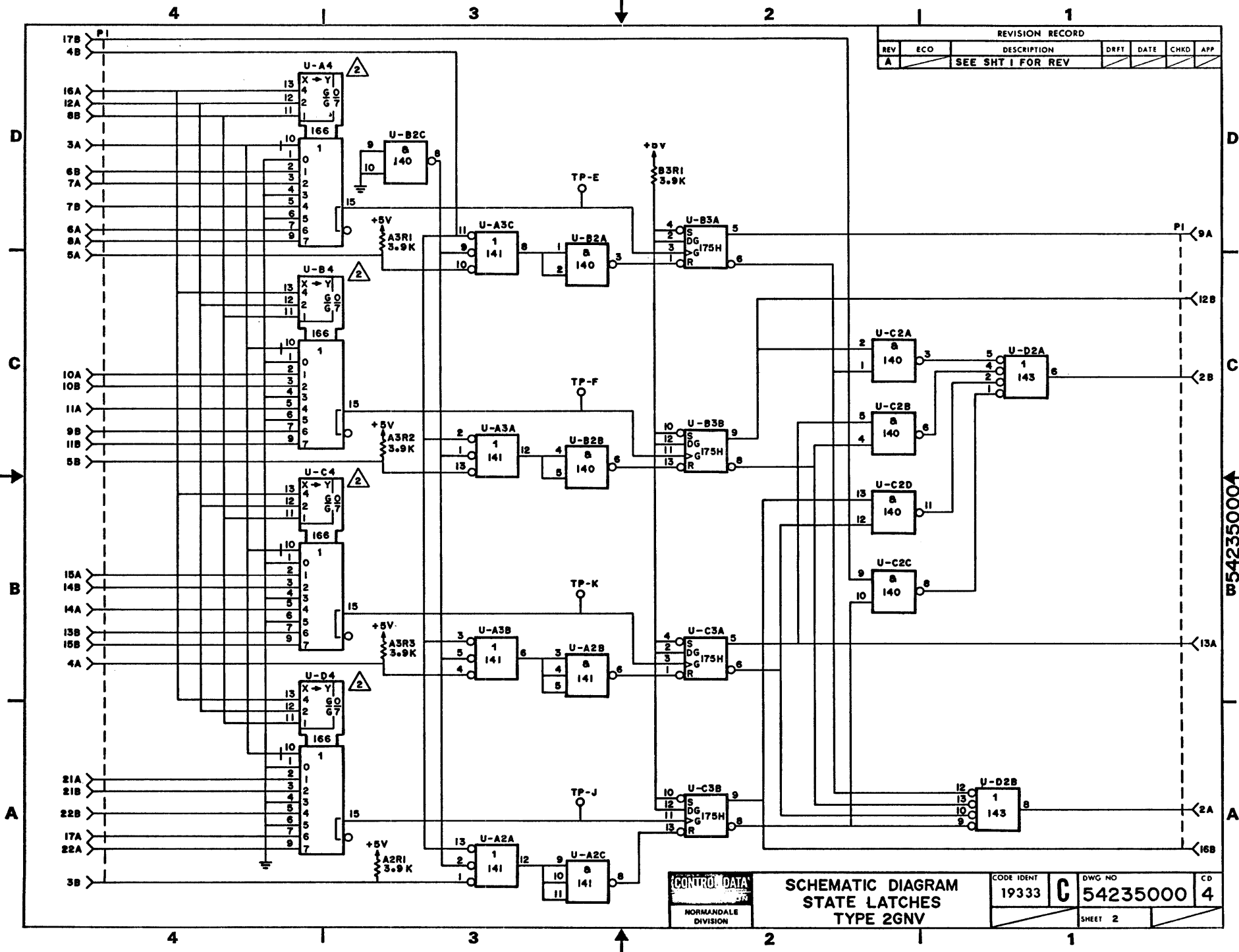
54234200



4-126

70629100 E

REVISION RECORD							
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		SEE SHT 1 FOR REV					



CONTROL DATA
NORMANDALE
DIVISION

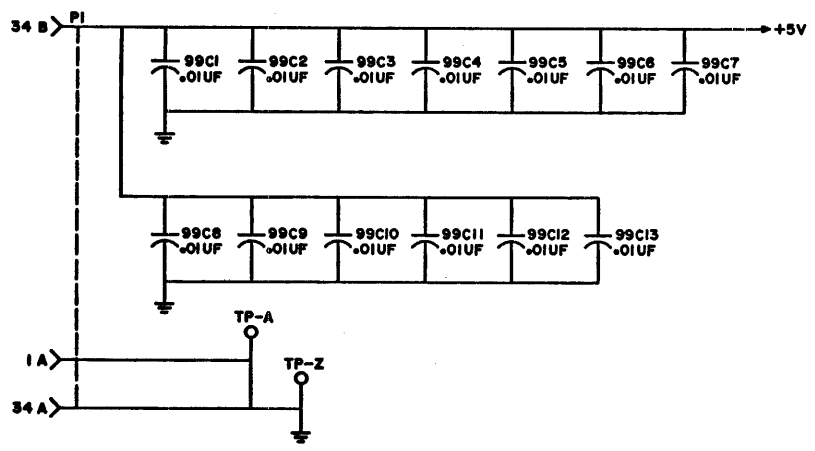
SCHEMATIC DIAGRAM
STATE LATCHES
TYPE 2GNV

CODE IDENT	19333	DWG NO	54235000	CD	4
		SHEET	2		

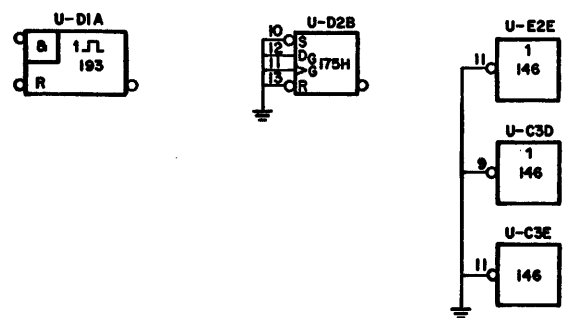
70629100 E

4-127

SHEET REVISION STATUS				REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE23000	RELEASED							
B	PE30859	VALUE & DELAY TIME CHG	SZ	9-30-72	DMS	II			



NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 2. ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 3. DELAY TIME FOR REFERENCE ONLY.

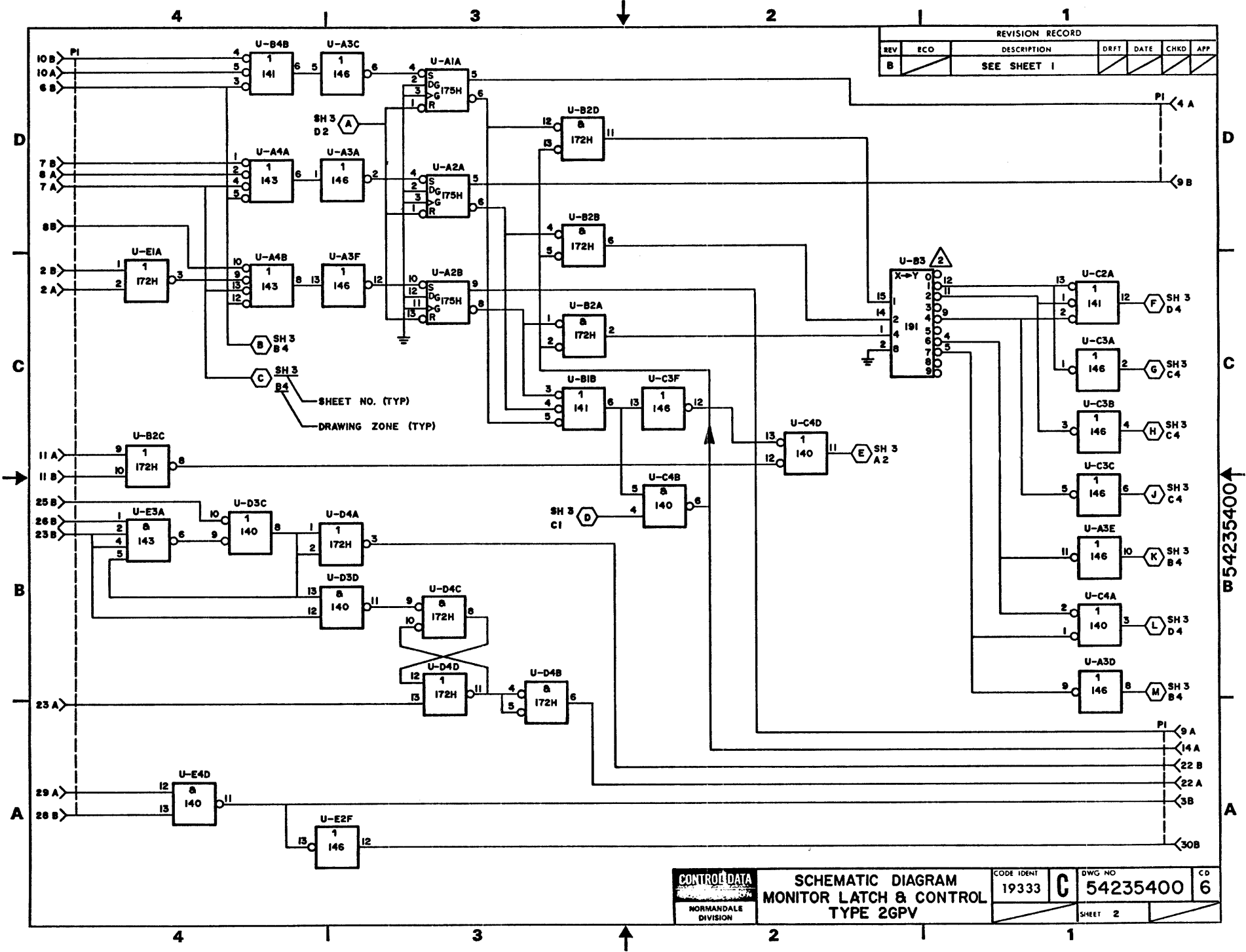


REFERENCE DRAWINGS	CONTROL DATA	NORMANDALE DIVISION	TITLE		
COMP ASSY 54235300	BR3A6		SCHEMATIC DIAGRAM		
	DWN D.G. TUTTLE	8-24-72	MONITOR LATCH & CONTROL		
	ENGR	8-8-72	TYPE 26PV		
COMPONENTS, EXCEPT AS NOTED	MFG	8-14-72	CODE IDENT	DRAWING NUMBER	C.D.
TOLERANCE VALUE RATING	APPR	9/14/72	19333	C 54235400	6
RES ±5% OHMS 1/4W					
CAP -30%					
SHEET 1 OF 3					

HPD 1

54235400

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				



CONTROL DATA
NORMANDALE DIVISION

SCHMATIC DIAGRAM
MONITOR LATCH & CONTROL
TYPE 26PV

CODE IDENT
19333

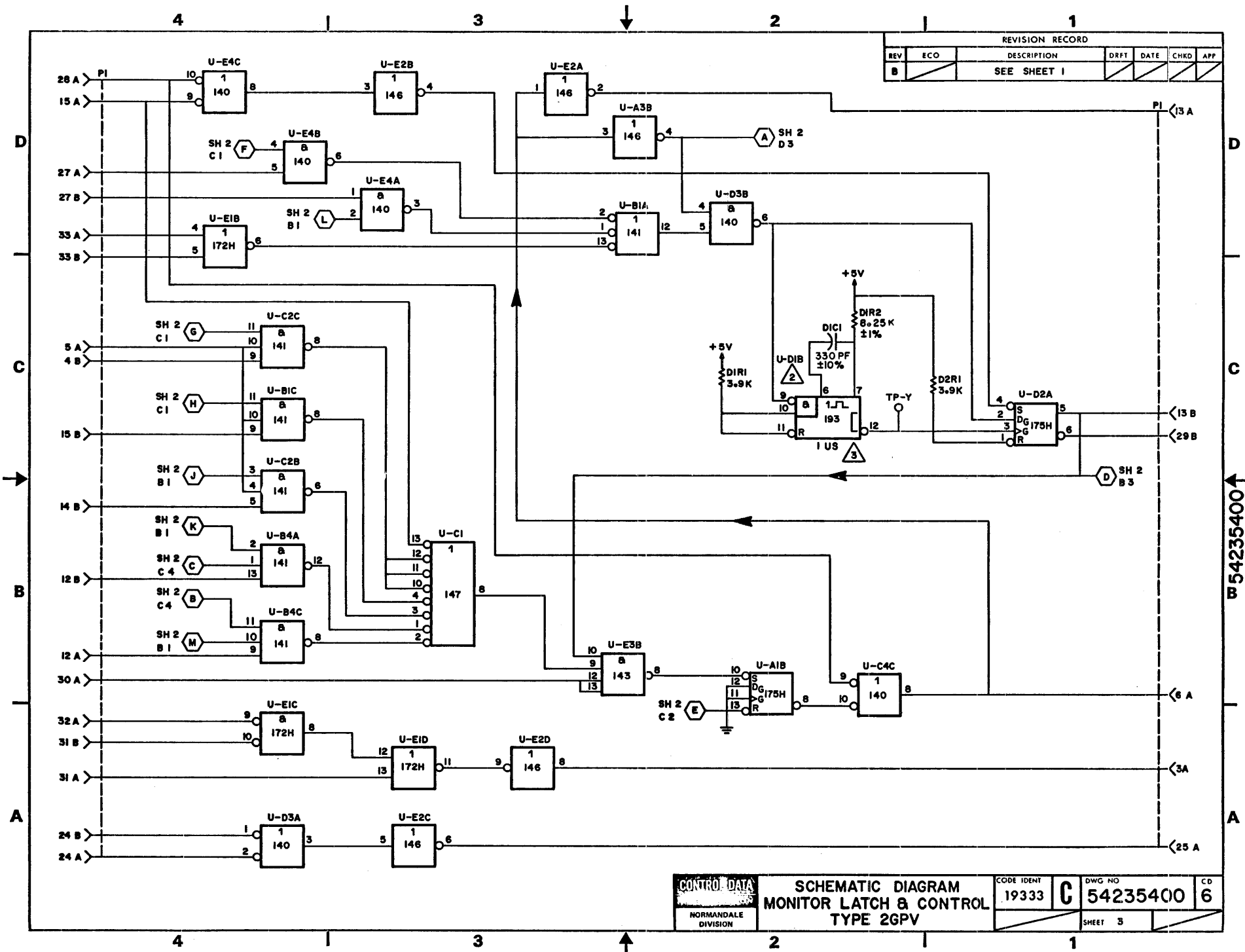
DWG NO
C 54235400
SHEET 2

CD
6

70629100 E

4-129

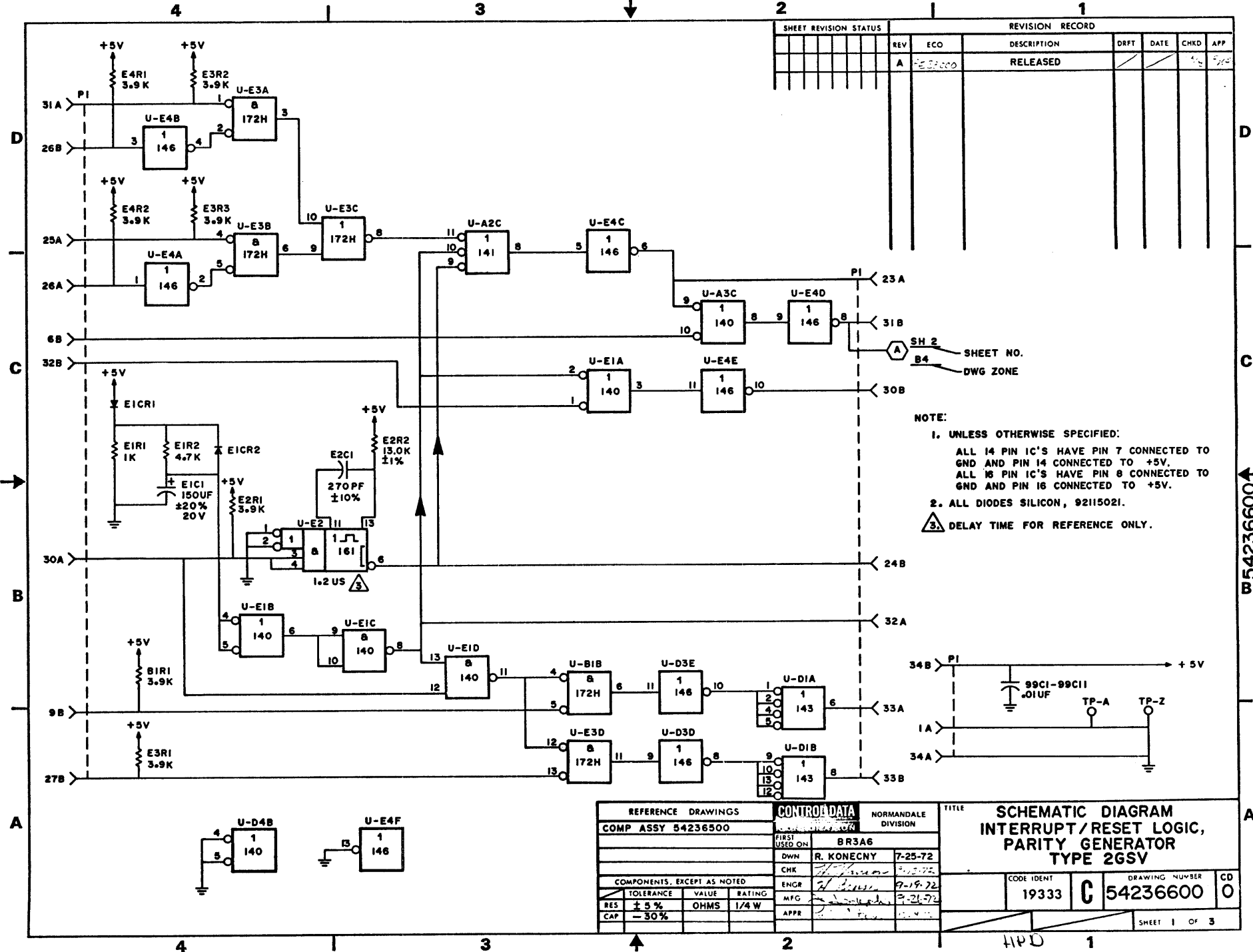
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				



CONTROL DATA NORMANDALE DIVISION	SCHMATIC DIAGRAM MONITOR LATCH & CONTROL TYPE 26PV		CODE IDENT 19333	DWG NO C 54235400	CD 6
				SHEET 3	

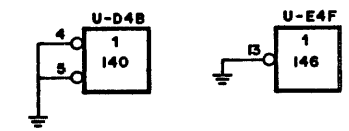
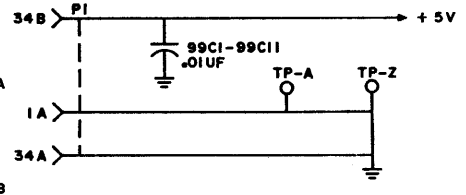
W 54235400

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE 3/20/72	RELEASED					



SH 2 SHEET NO.
B4 DWG ZONE

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 - ALL DIODES SILICON, 92115021.
- △. DELAY TIME FOR REFERENCE ONLY.

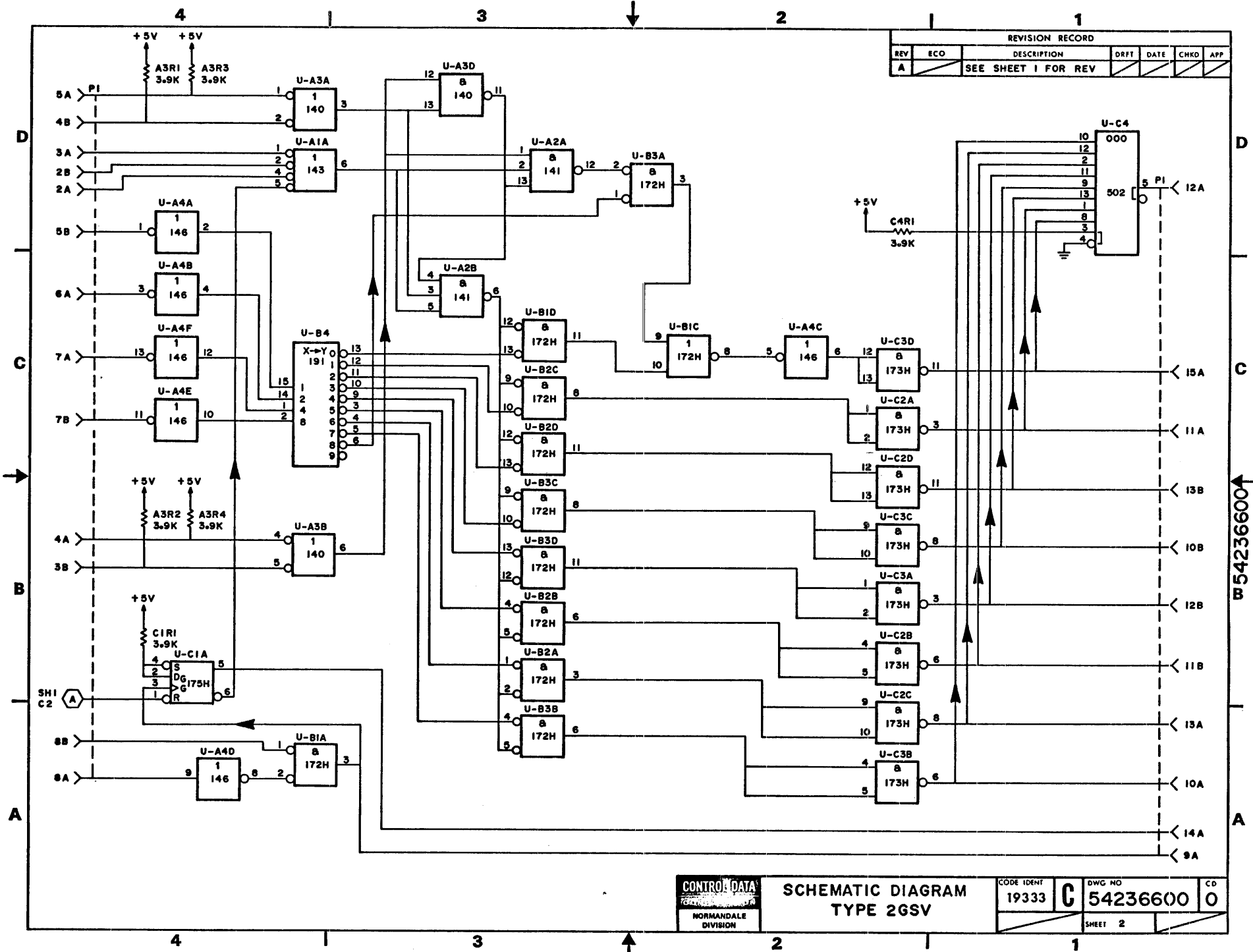


REFERENCE DRAWINGS			CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMP ASSY 54236500			FIRST USED ON		BR3A6		SCHEMATIC DIAGRAM	
			DWN		R. KONECNY		INTERRUPT / RESET LOGIC,	
			CHK		7-25-72		PARITY GENERATOR	
			ENGR		7-19-72		TYPE 2GSV	
			MFG		7-21-72		CODE IDENT	
			APPR				DRAWING NUMBER	
COMPONENTS, EXCEPT AS NOTED			TOLERANCE		VALUE		RATING	
			RES		± 5%		OHMS	
			CAP		- 30%		1/4 W	
							CD	
							19333	
							C	
							54236600	
							0	
							SHEET 1 OF 3	

HPD 1

B 54236600

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



**SCHEMATIC DIAGRAM
TYPE 2GSV**

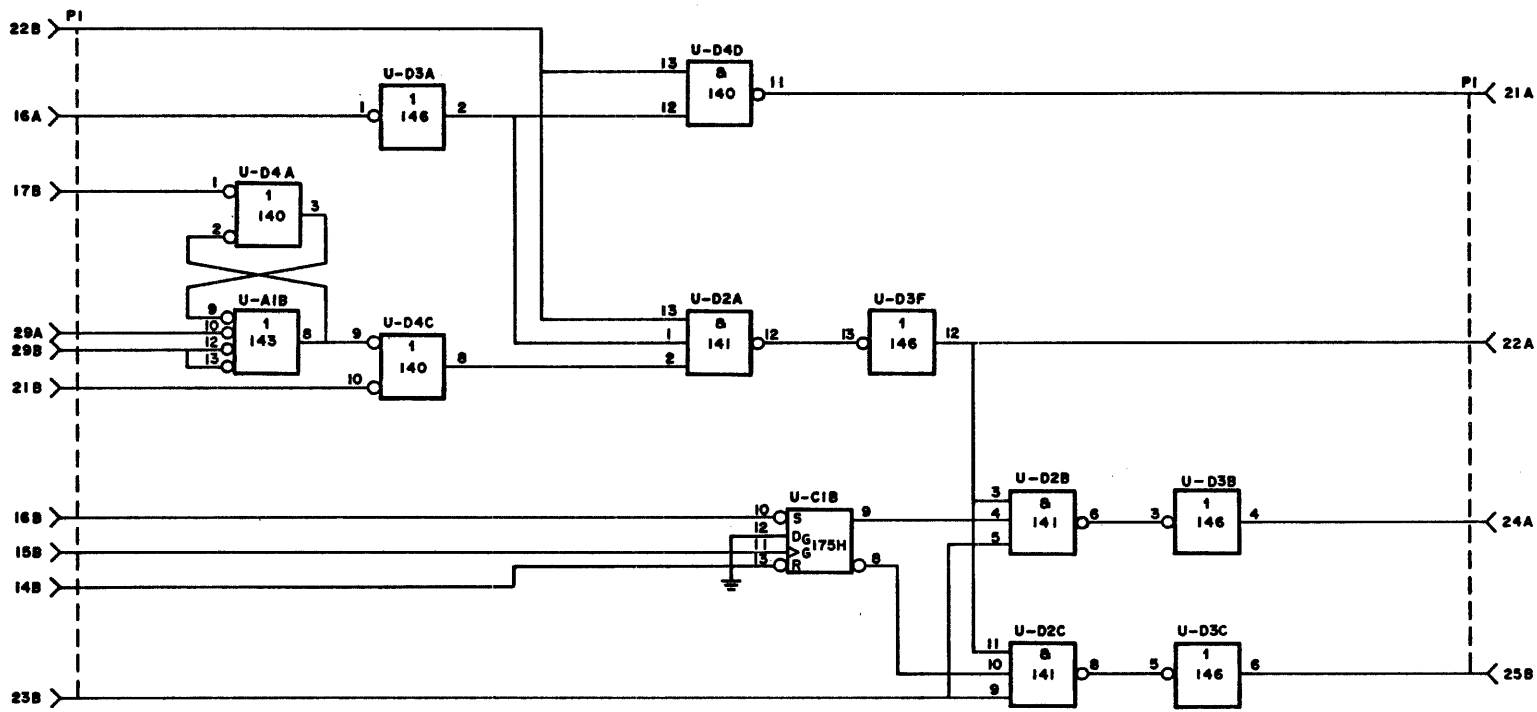
CODE IDENT 19333	DWG NO 54236600	CD 0
SHEET 2		

B 54236600

4-132

70629100 F

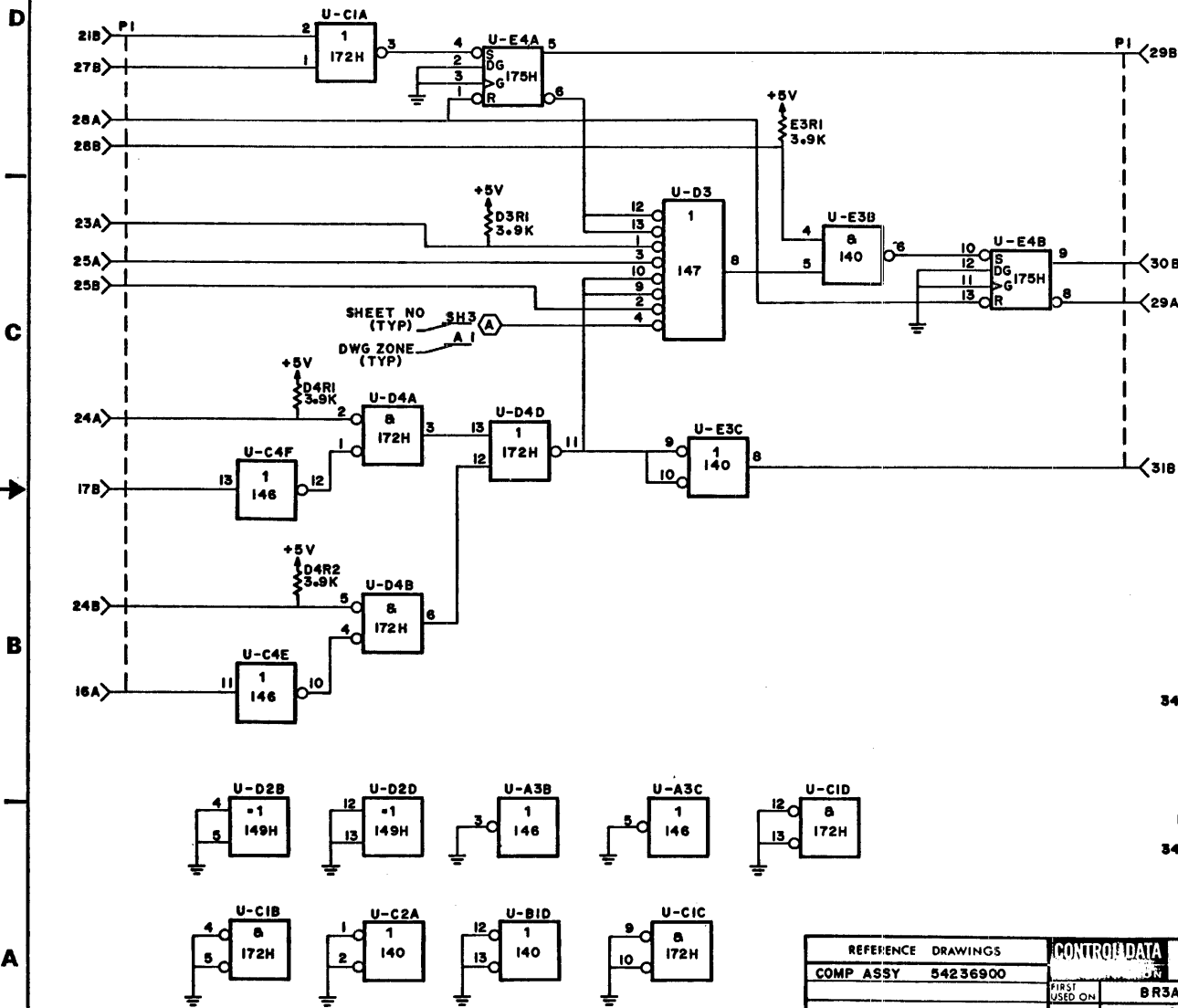
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



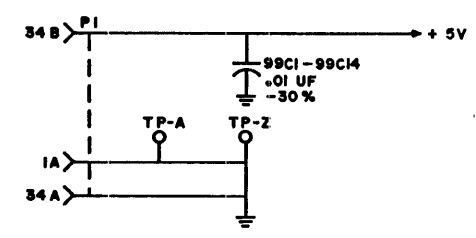
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 2GSV		CODE IDENT 19333	DWG NO C 54236600	CO 0
				SHEET 3	

54236600

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRAFT	DATE	CHKD	APP	
A	PE23000	RELEASED					



NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIME FOR REFERENCE ONLY.

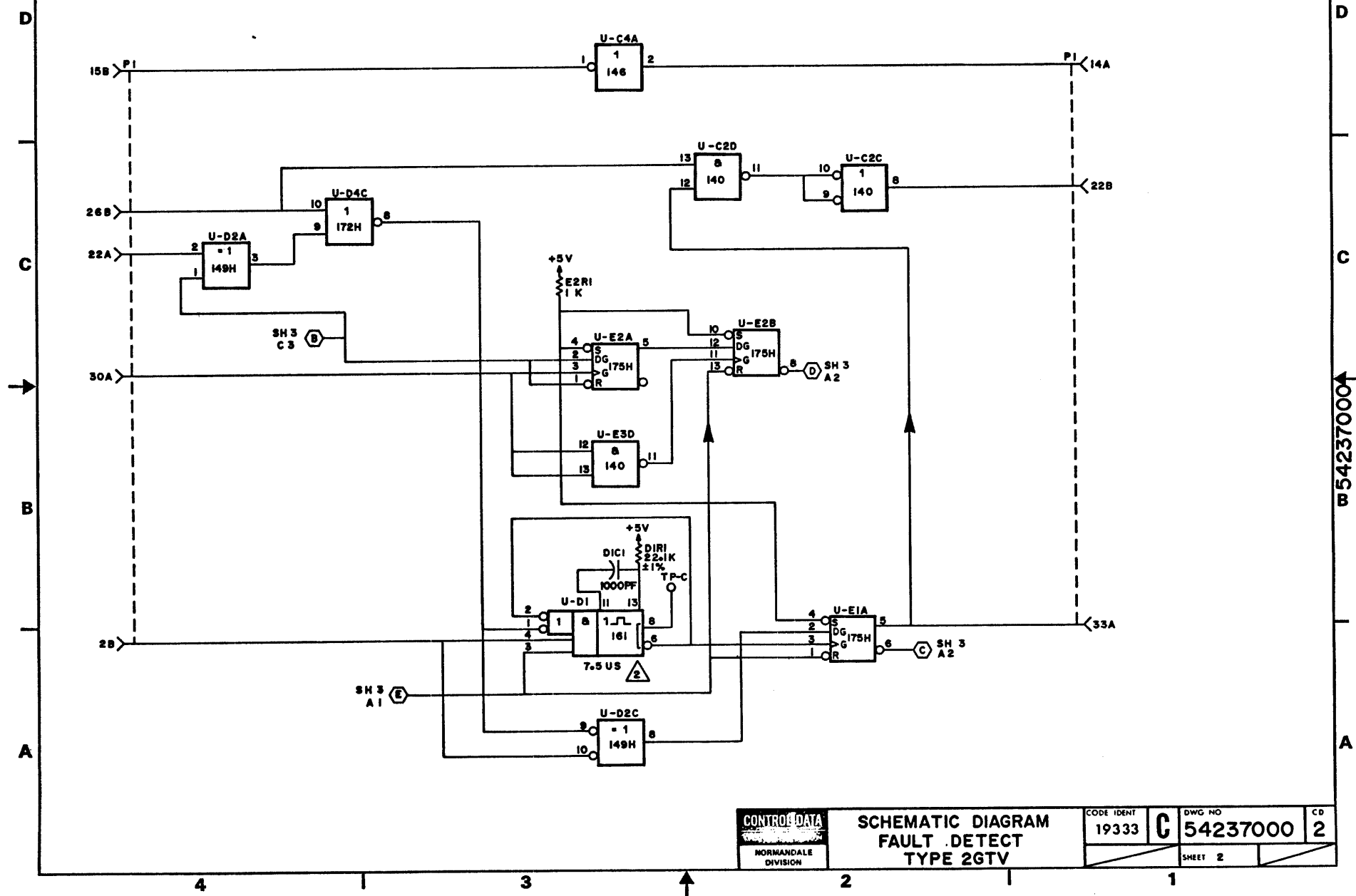


REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY	54236900	FIRST USED ON	BR3A6			SCHEMATIC DIAGRAM FAULT DETECT TYPE 2GTV	
COMPONENTS, EXCEPT AS NOTED		DWN	7-24-72	CHK	8-2-72	CODE IDENT	19333
TOLERANCE	VALUE	RATING		ENGR	8-7-72	DRAWING NUMBER	C 54237000
RES	±5%	OHMS	1/4 W	MFG	8-7-72	CD	2
CAP	±10%			APPR	1/5/72	SHEET 1 OF 3	

D
C
B
A

W54237000

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



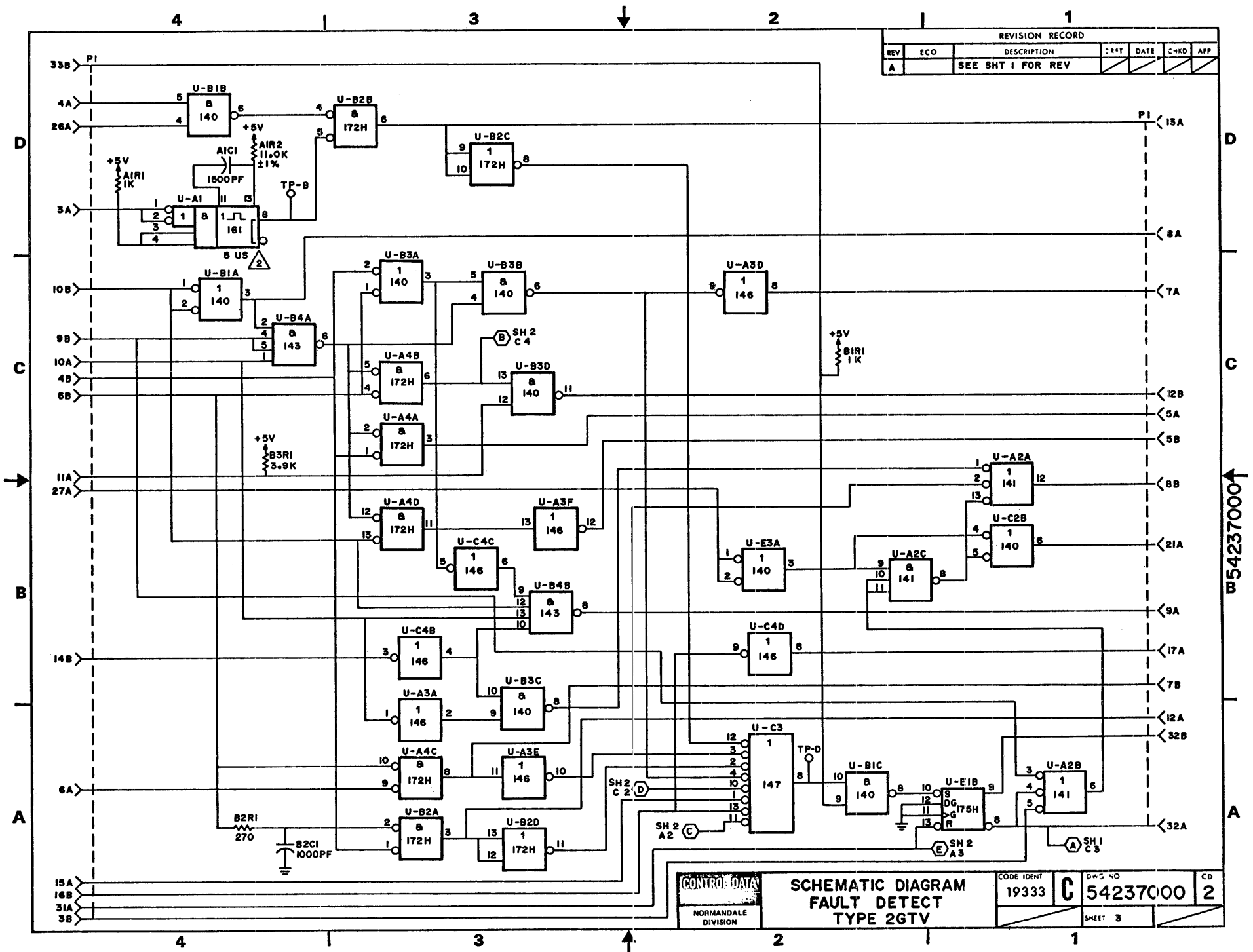
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM FAULT DETECT TYPE 2GTV		CODE IDENT 19333	DWG NO C 54237000	CD 2
				SHEET 2	

W 54237000

70629100 E

4-135

REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	DATE	C-KD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDEALE
DIVISION

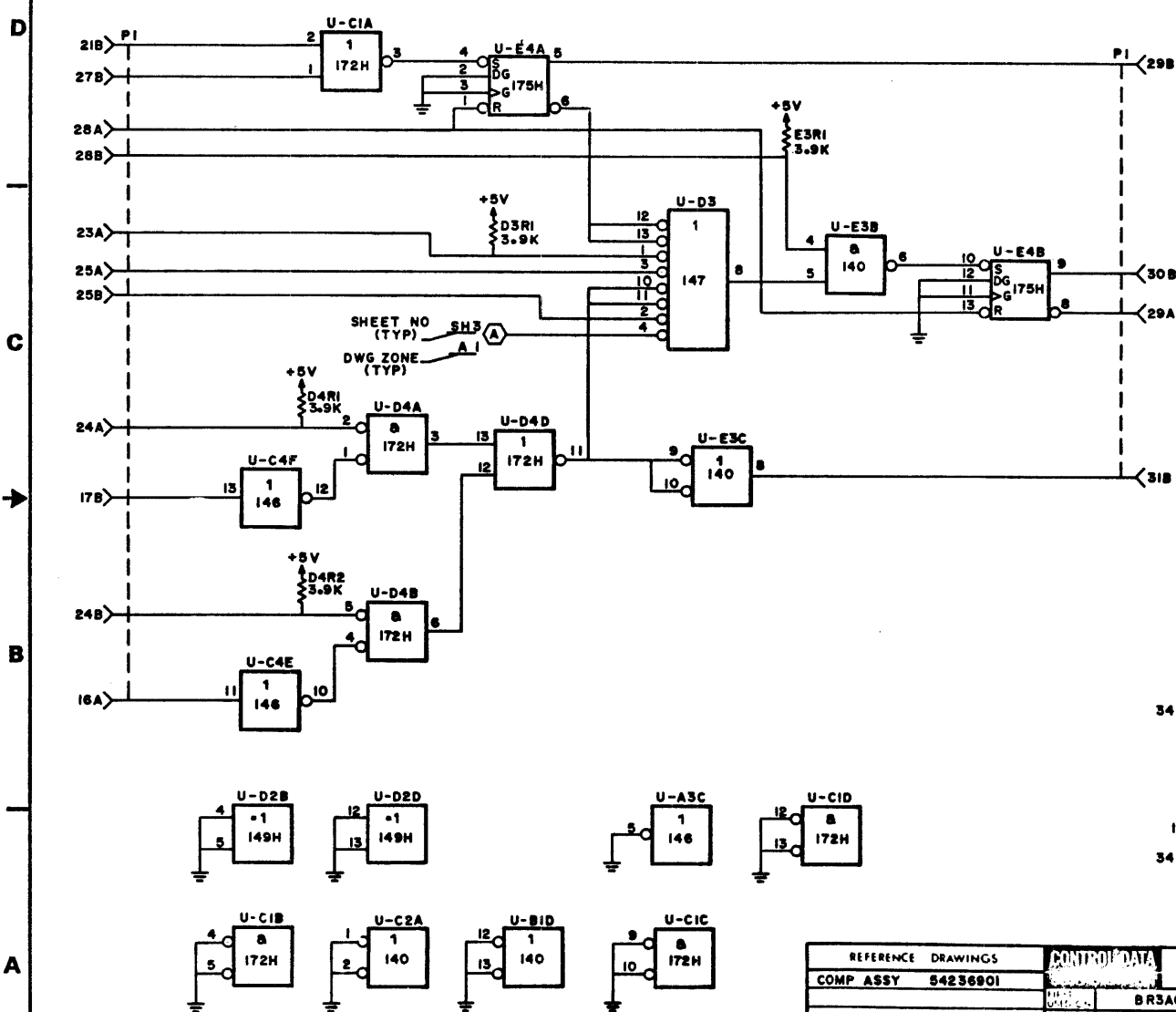
SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 2GTV

CODE IDENT	19333	DWG NO	C 54237000	CD	2
SHEET	3				

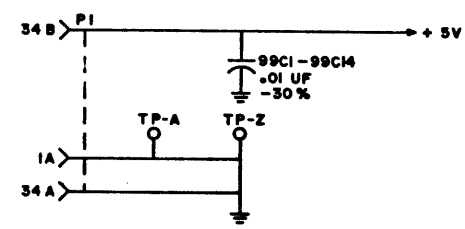
4-136

70629100 E

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE2E000	RELEASED	U	2-2-73			58



NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIME FOR REFERENCE ONLY.



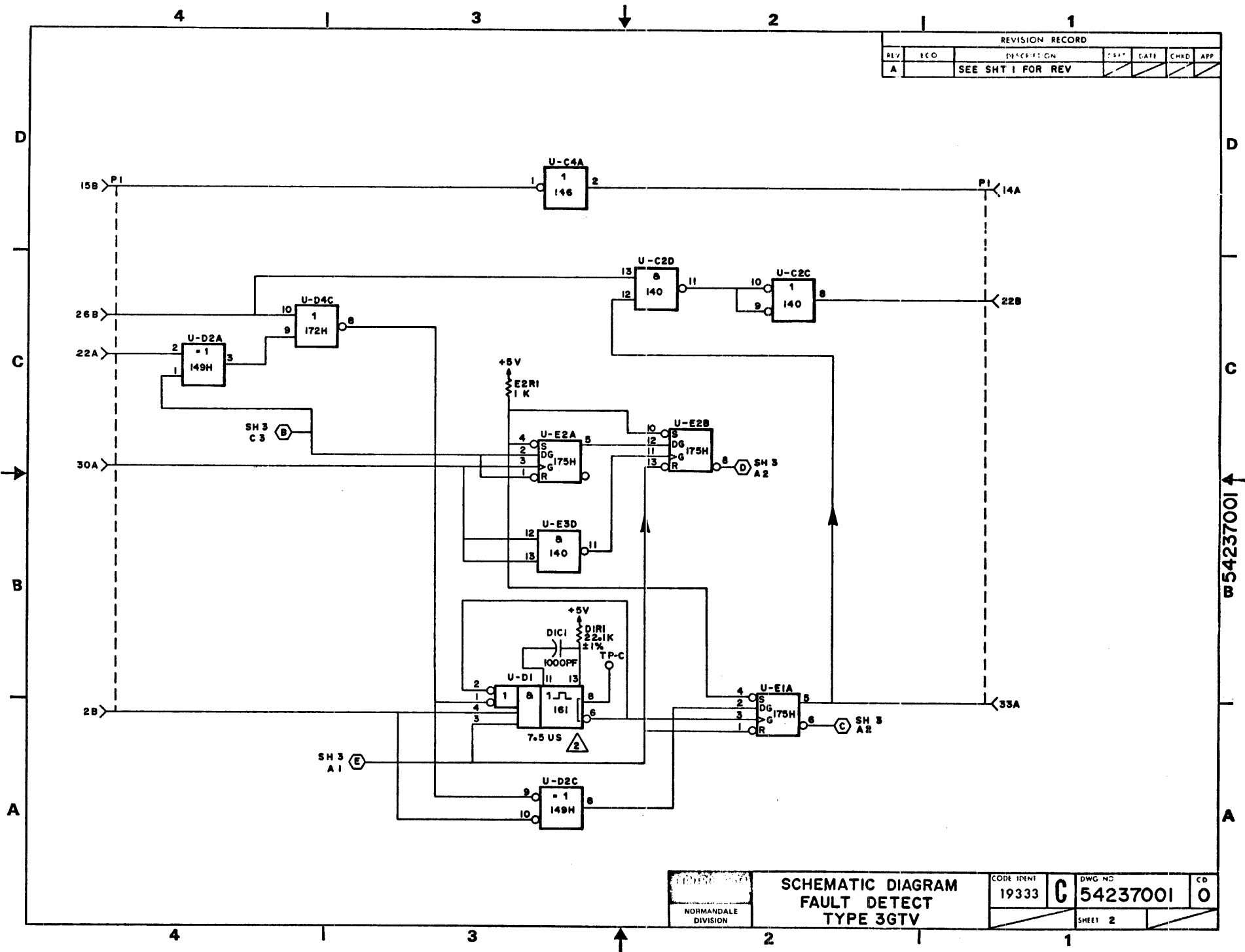
REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY	54236901	REV	BR3A6	DRWN	R. RICHTER	1-15-73	SCHEMATIC DIAGRAM FAULT DETECT TYPE 3GTV
		CHKR		ENGR			
COMPONENTS EXCEPT AS NOTED		REL	±5%	OHMS	1/4 W		CODE IDENT
RES		TOLERANCE	VALUE	RATING			19333
CAP		TOLERANCE	VALUE	RATING			DRAWING NUMBER
							54237001
							CD
							0
							SHEET 1 OF 3

400

70629100 E

4-137

REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHT 1 FOR REV				



NORMANDEALE DIVISION

SCHEMATIC DIAGRAM
FAULT DETECT
TYPE 3GTV

CODE IRM1
19333

DWG NO
54237001

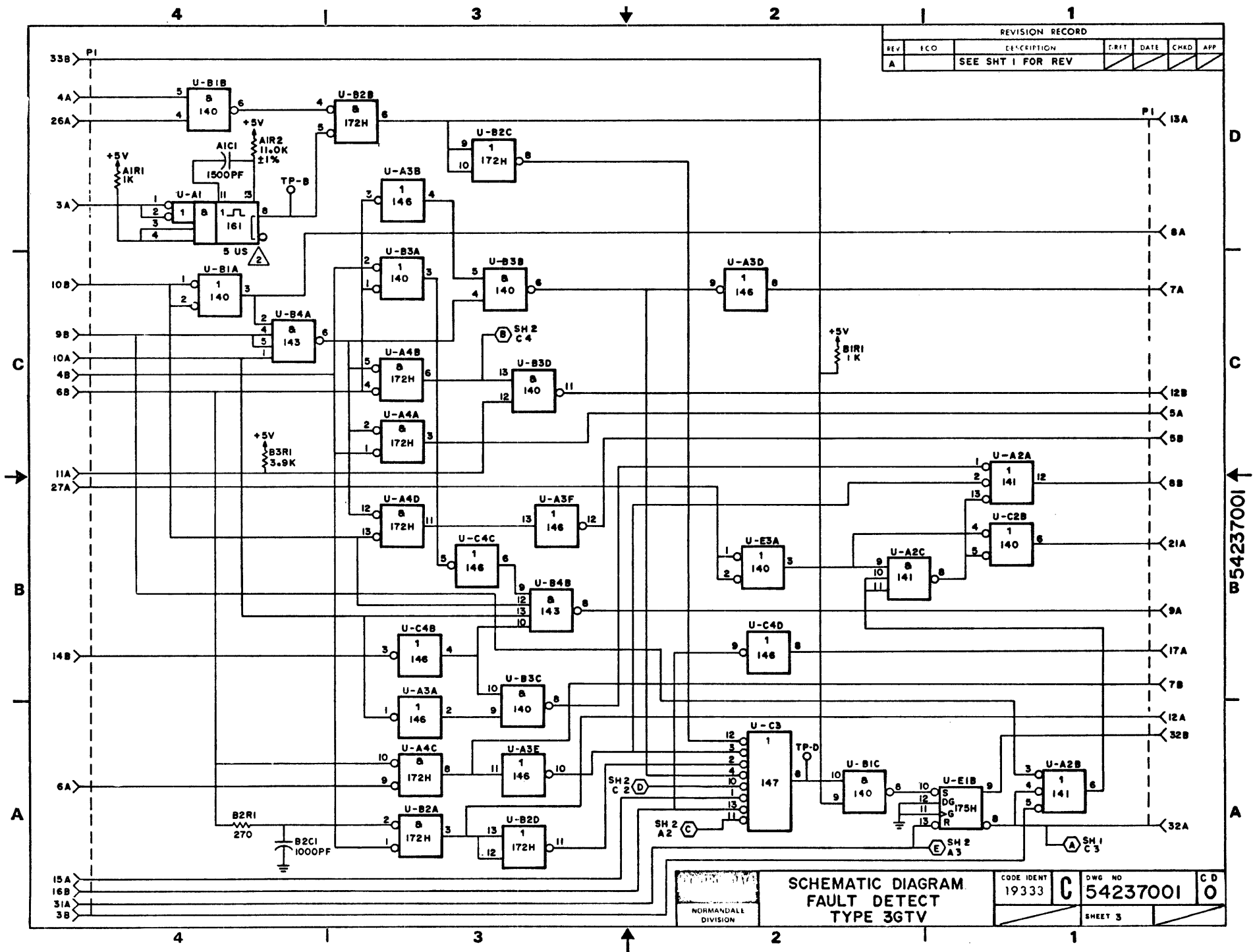
CD
0

SHEET 2

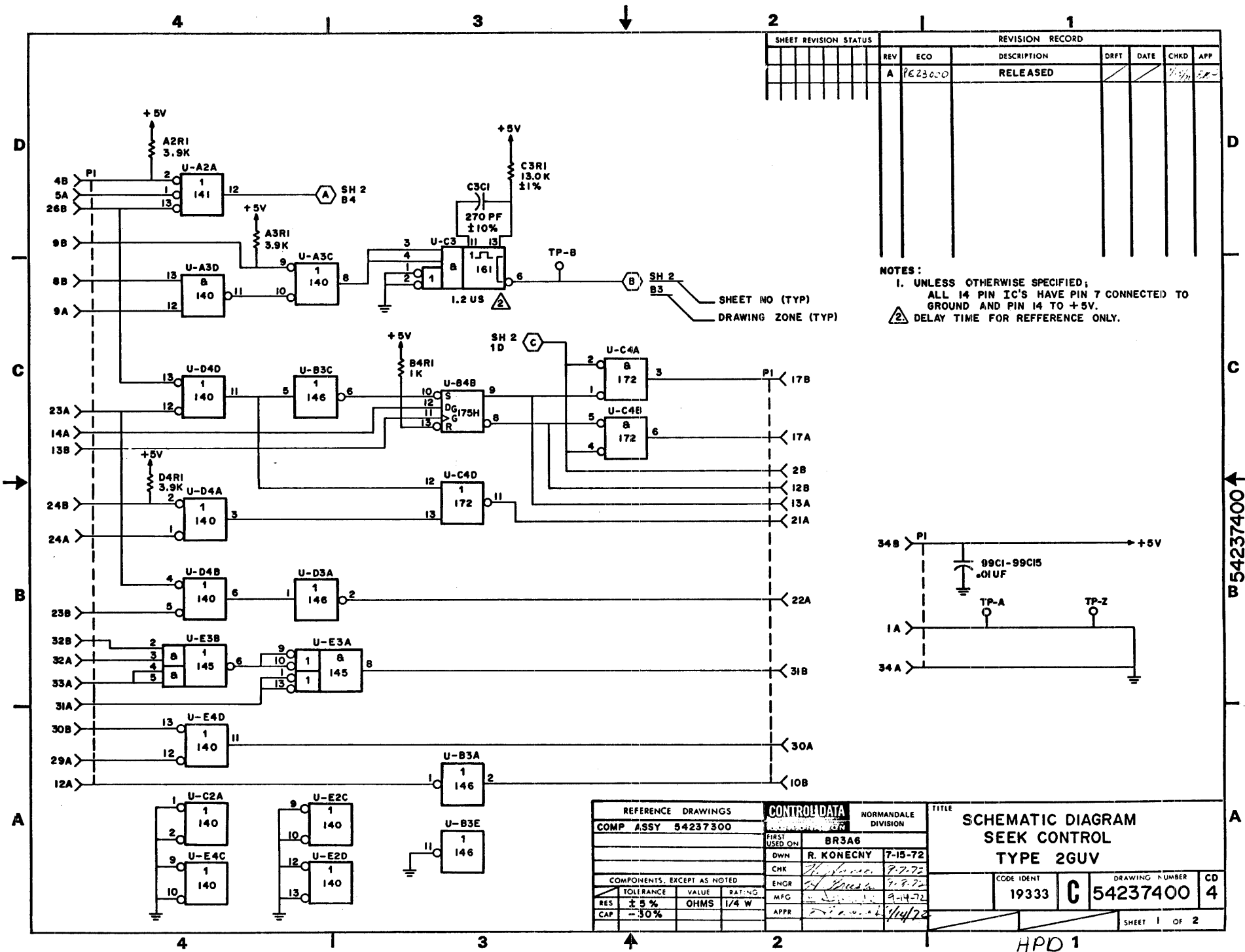
4-138

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM FAULT DETECT TYPE 3GTV		CODE IDENT 19333	DWG NO 54237001	C D 0
				SHEET 3	



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	7E23000	RELEASED					

NOTES:
 1. UNLESS OTHERWISE SPECIFIED;
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO
 GROUND AND PIN 14 TO +5V.
 ⚠ DELAY TIME FOR REFERENCE ONLY.

SH 2 (A) SHEET NO (TYP)
 SH 2 (B) DRAWING ZONE (TYP)

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54237300		FIRST USED ON BR3A6		DWN R. KONECNY 7-15-72		SCHEMATIC DIAGRAM	
COMPONENTS, EXCEPT AS NOTED		CHK [Signature] 7-7-72		ENGR [Signature] 7-8-72		SEEK CONTROL	
TOLERANCE VALUE RATING		MFG [Signature] 7-14-72		APPR [Signature] 7/14/72		TYPE 2GUV	
RES ± 5%	OHMS 1/4 W	CODE IDENT 19333		DRAWING NUMBER C 54237400		CD 4	
CAP -50%		SHEET 1 OF 2					

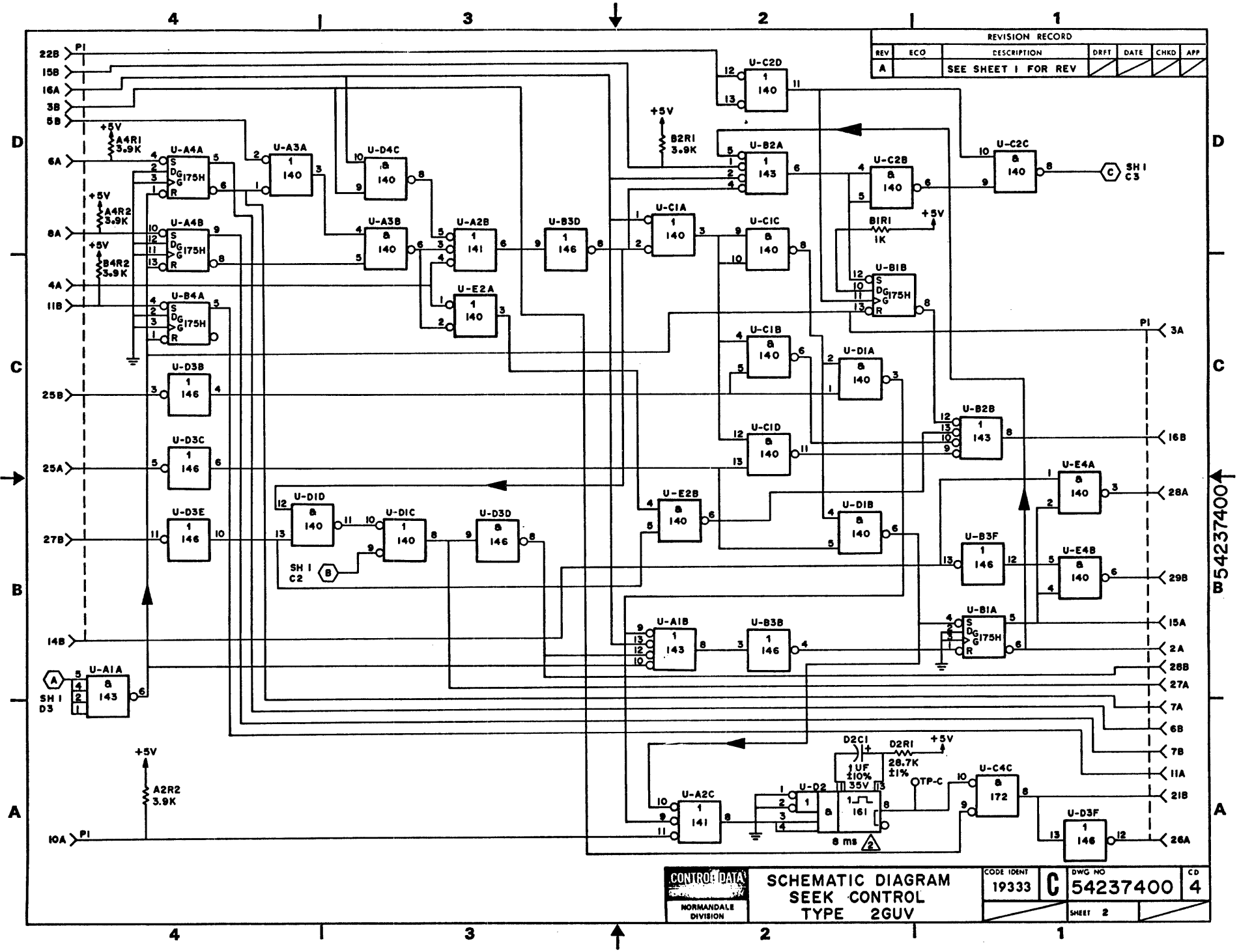
HPD 1

W 54237400 ↑

4-140

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



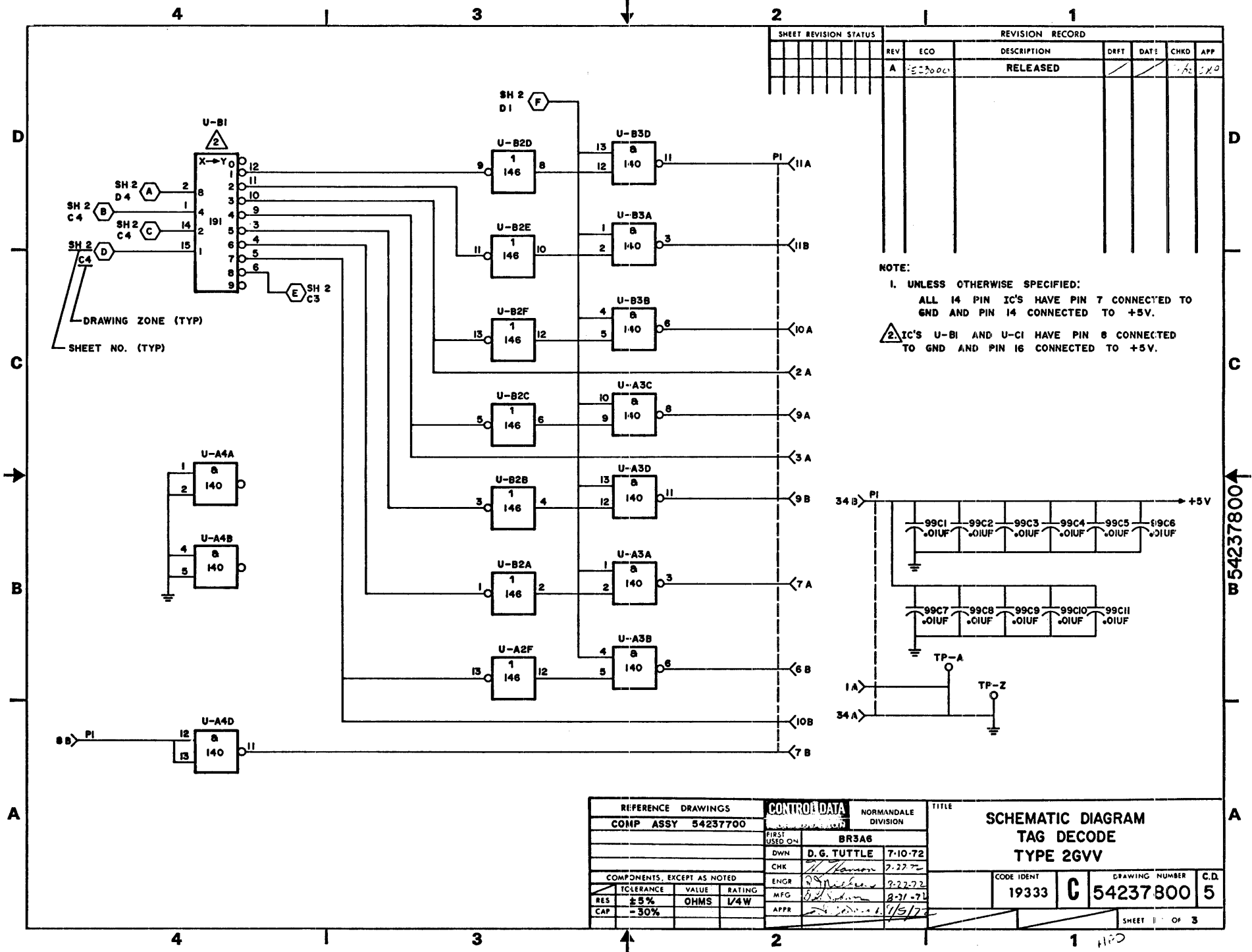
CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM SEEK CONTROL TYPE 2GUV		CODE IDENT 19333	DWG NO C 54237400	CD 4
			SHEET 2		

70629100 E

4-141

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. IC'S U-B1 AND U-C1 HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.

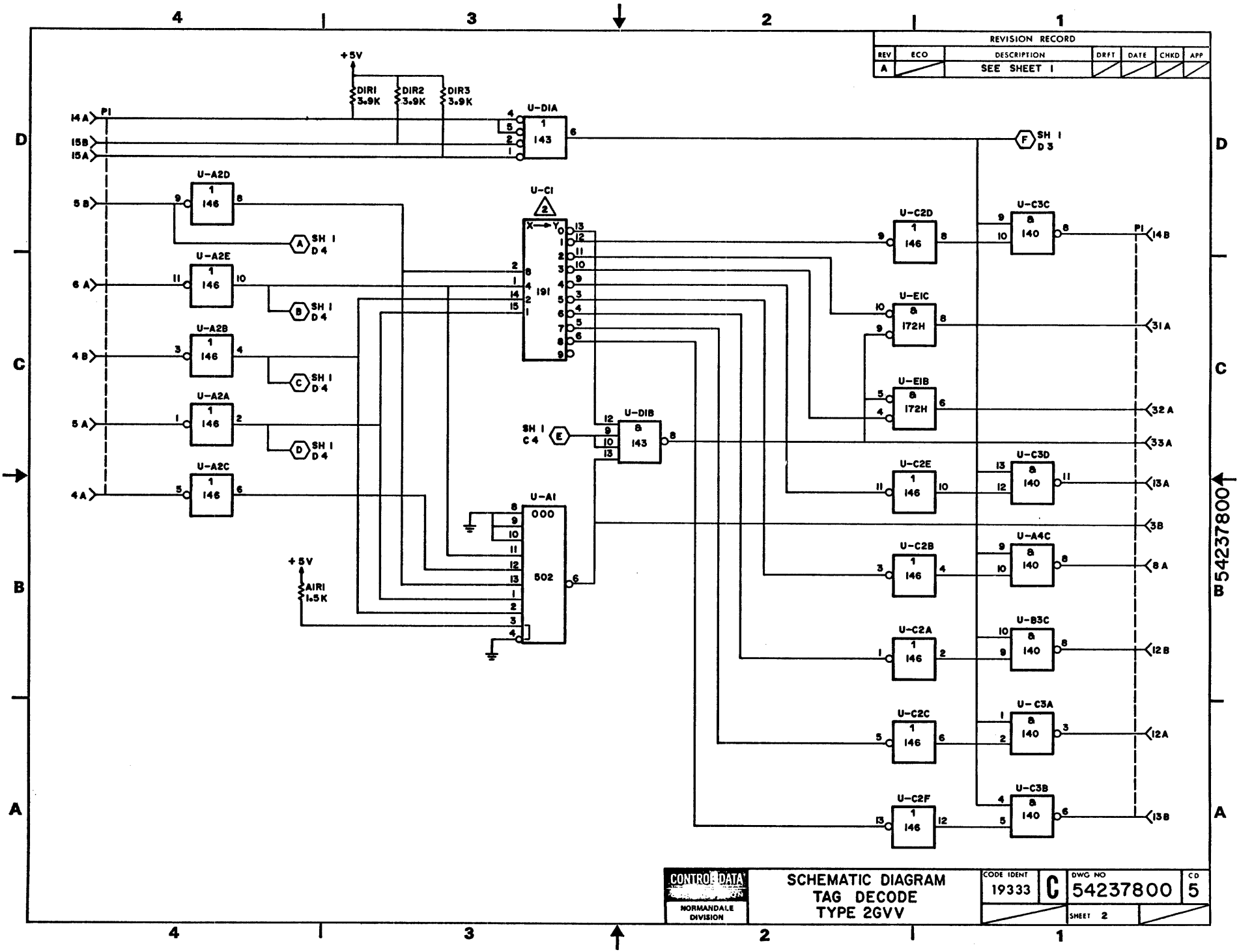


REFERENCE DRAWINGS		CONTROL DATA		NORMANDE DIVISION		TITLE	
COMP ASSY 54237700		FIRST USED ON		BR3A6		SCHEMATIC DIAGRAM	
		DWN		D. G. TUTTLE		TAG DECODE	
		CHK		7-10-72		TYPE 2GVV	
		ENGR		2-22-72		CODE IDENT	
		MFG		2-21-72		DRAWING NUMBER	
		APPR		1/13/72		C.D.	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES		± 5%		OHMS		1/4W	
CAP		- 30%					
		19333		C		54237800	
		SHEET 11		OF 3			

4-142

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA
NORMANDE
DIVISION

**SCHEMATIC DIAGRAM
TAG DECODE
TYPE 2GVV**

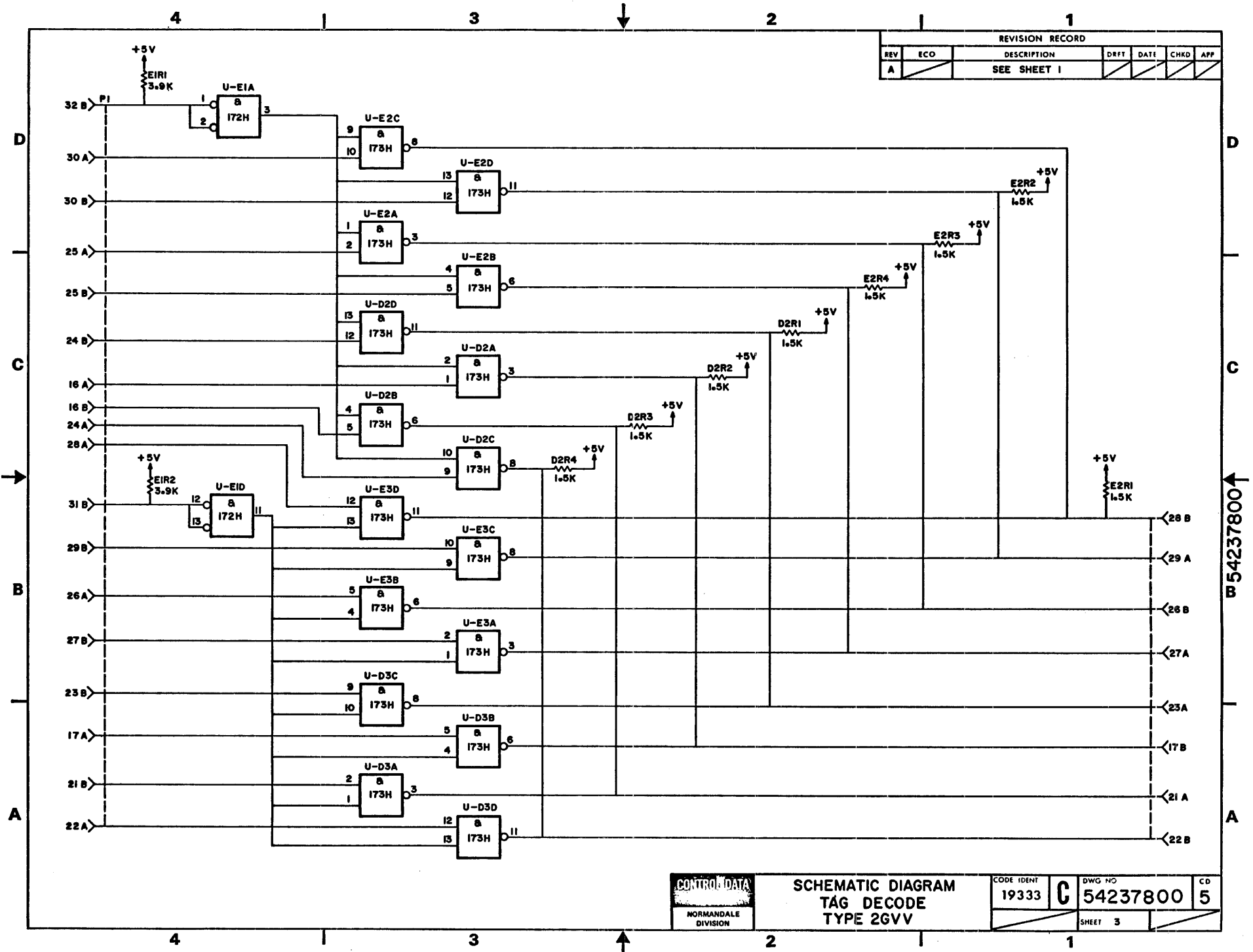
CODE IDENT 19333	C	DWG NO 54237800	CD 5
SHEET 2			

W 54237800

70629100 E

4-143

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA
NORMANDEALE
DIVISION

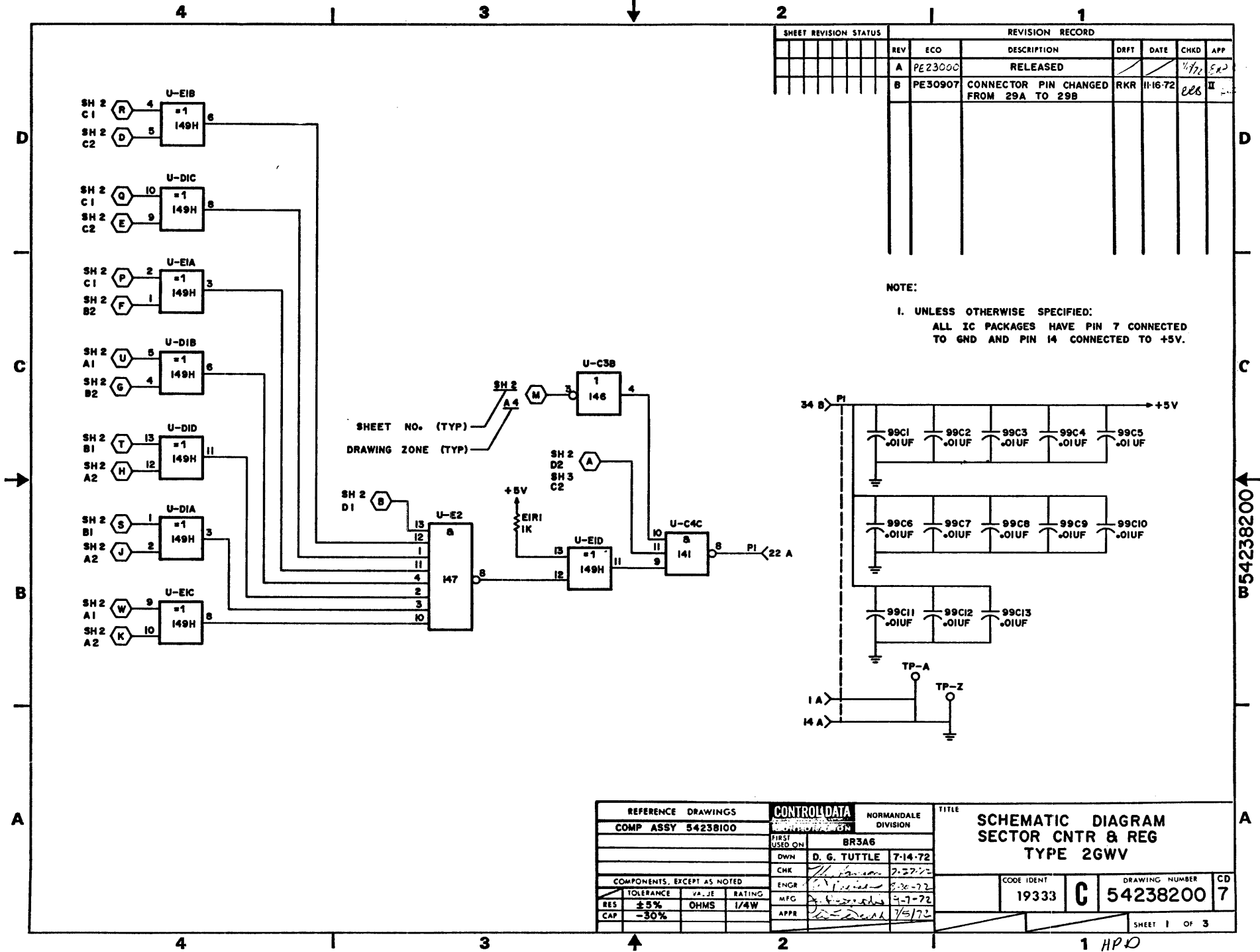
SCHEMATIC DIAGRAM
TAG DECODE
TYPE 26GV

CODE IDENT	19333	DWG NO	54237800	CD	5
		SHEET	3		

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					
B	PE30907	CONNECTOR PIN CHANGED FROM 29A TO 29B	RKR	11-16-72	ell		

NOTE:

I. UNLESS OTHERWISE SPECIFIED:
ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

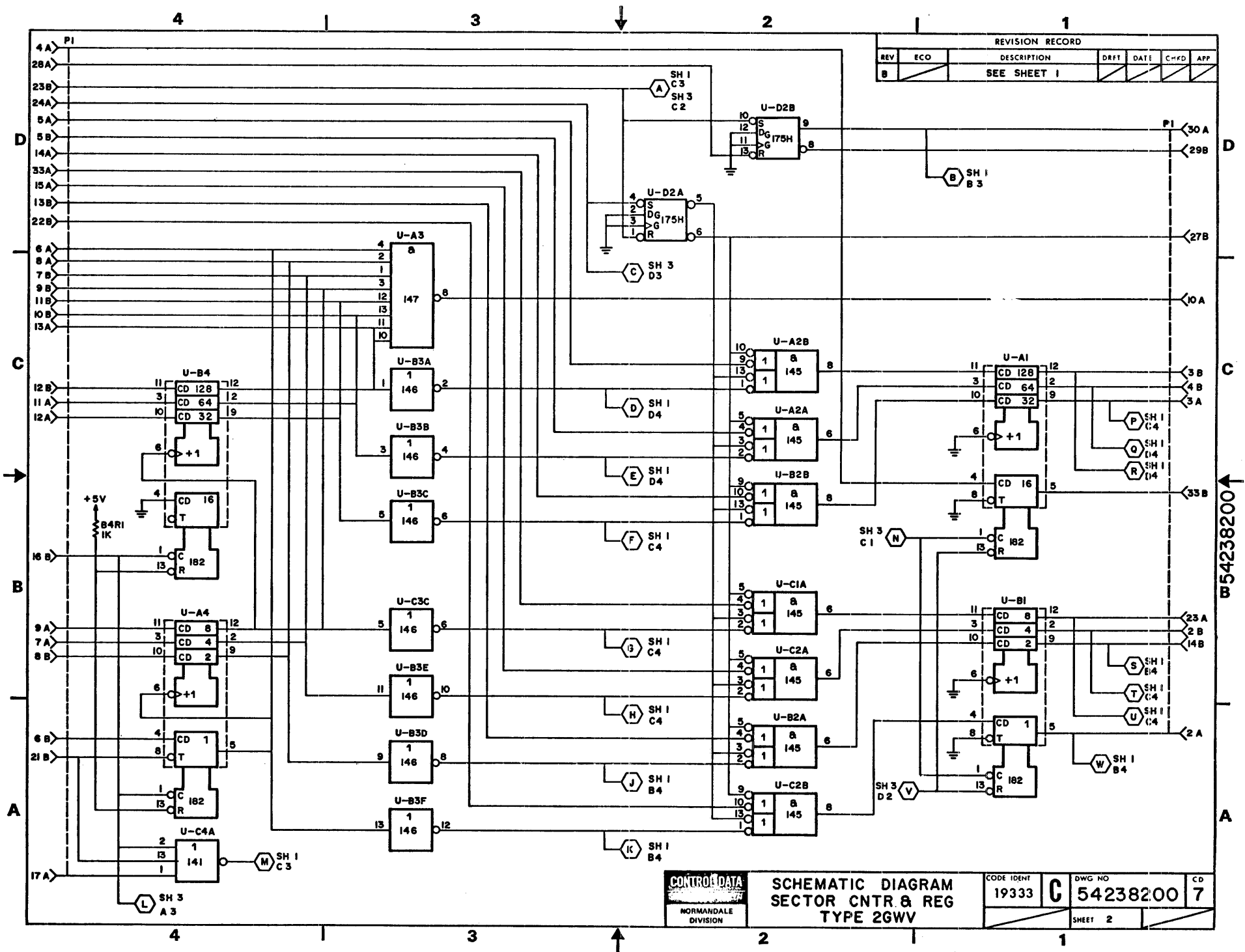


REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54238100		FIRST USED ON BR3A6		DWN D. G. TUTTLE 7-14-72		SCHEMATIC DIAGRAM	
		CHK [Signature] 7-27-72		ENGR [Signature] 8-30-72		SECTOR CNTR & REG	
		MFG [Signature] 9-7-72		APPR [Signature] 7/5/72		TYPE 2GWV	
COMPONENTS, EXCEPT AS NOTED		CODE IDENT 19333		DRAWING NUMBER C 54238200		CD 7	
TOLERANCE	VA-JE	RATING					
RES ±5%	OHMS	1/4W					
CAP -30%							SHEET 1 OF 3

1 HPD

70629100 F

4-145

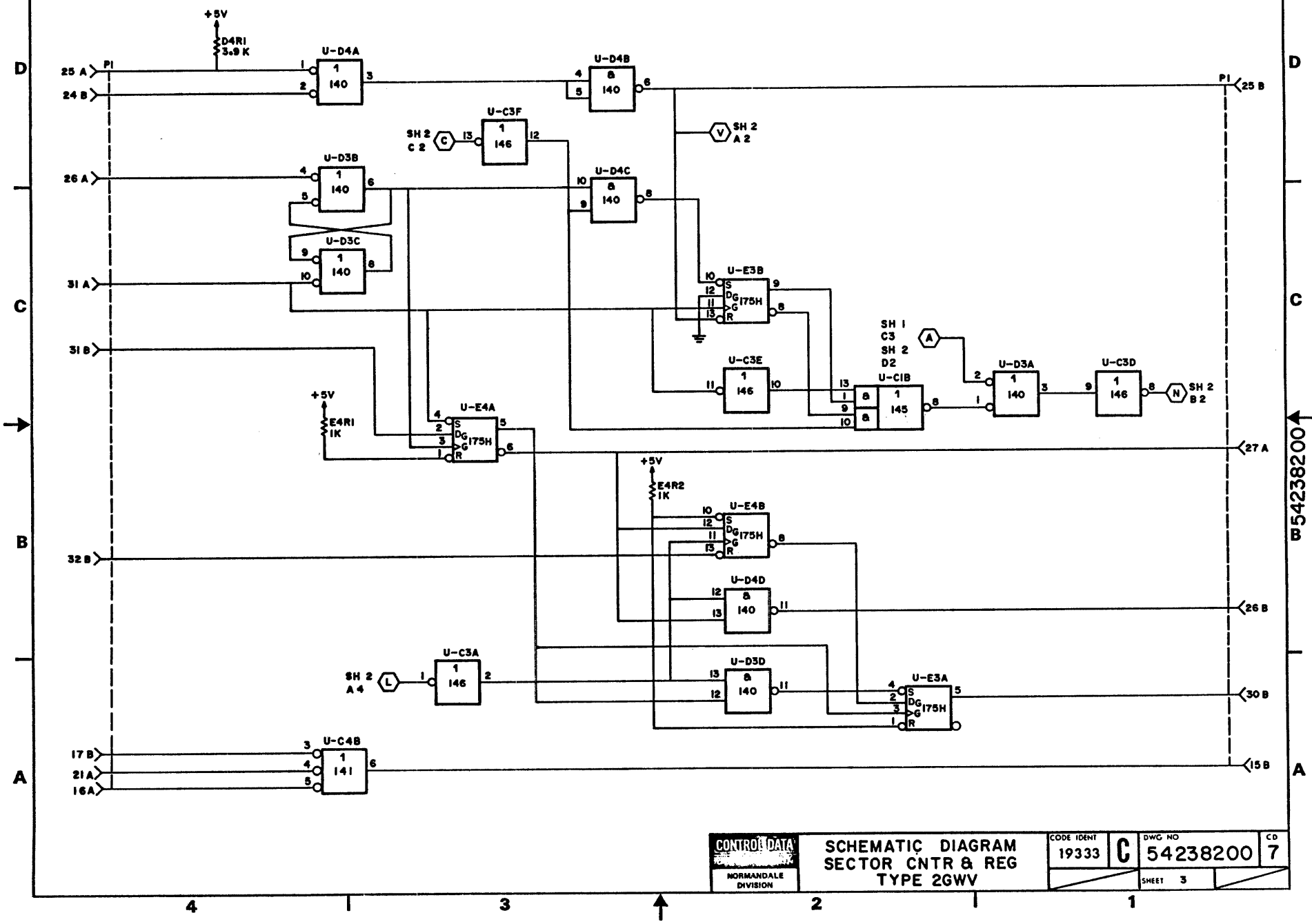


CONTROL DATA NORMANDALE DIVISION	SCHEMATIC DIAGRAM SECTOR CNTR & REG TYPE 2GWV		CODE IDENT 19333	DWG NO 54238200	CD 7
				SHEET 2	

4-146

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHEET 1				



CONTROL DATA
NORMANDALE DIVISION

SCHEMATIC DIAGRAM
SECTOR CNTR & REG
TYPE 2GWV

CODE IDENT
19333

DWG NO
54238200

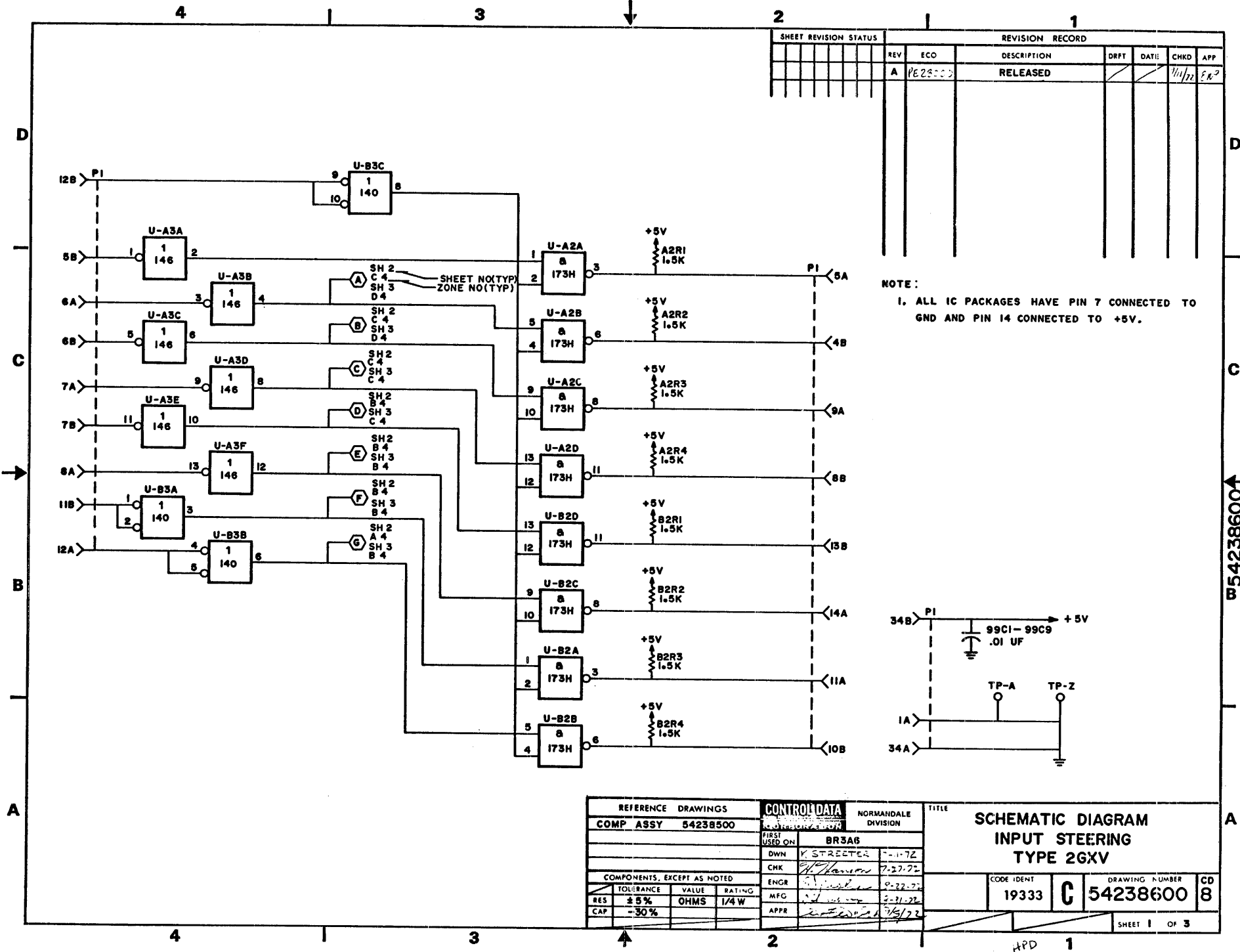
CD
7

SHEET 3

54238200

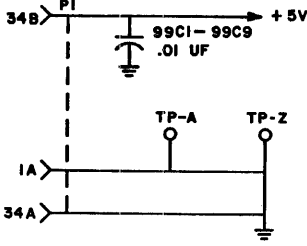
70629100 E

4-147



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED			1/1/72	EA?	

NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS		CONTROL DATA		NORMAN DALE DIVISION		TITLE	
COMP ASSY	54238500	FIRST USED ON	BR3A6			SCHEMATIC DIAGRAM INPUT STEERING TYPE 26XV	
COMPONENTS, EXCEPT AS NOTED		DWN	V. STREETER	7-1-72		CODE IDENT	DRAWING NUMBER
RES	± 5%	VALVE	H. Hanson	7-27-72		19333	54238600
CAP	-30%	RATING	ENG	9-22-72		C	8
			MFG	3-31-72			
			APPR	1/9/72			

SHEET 1 OF 3

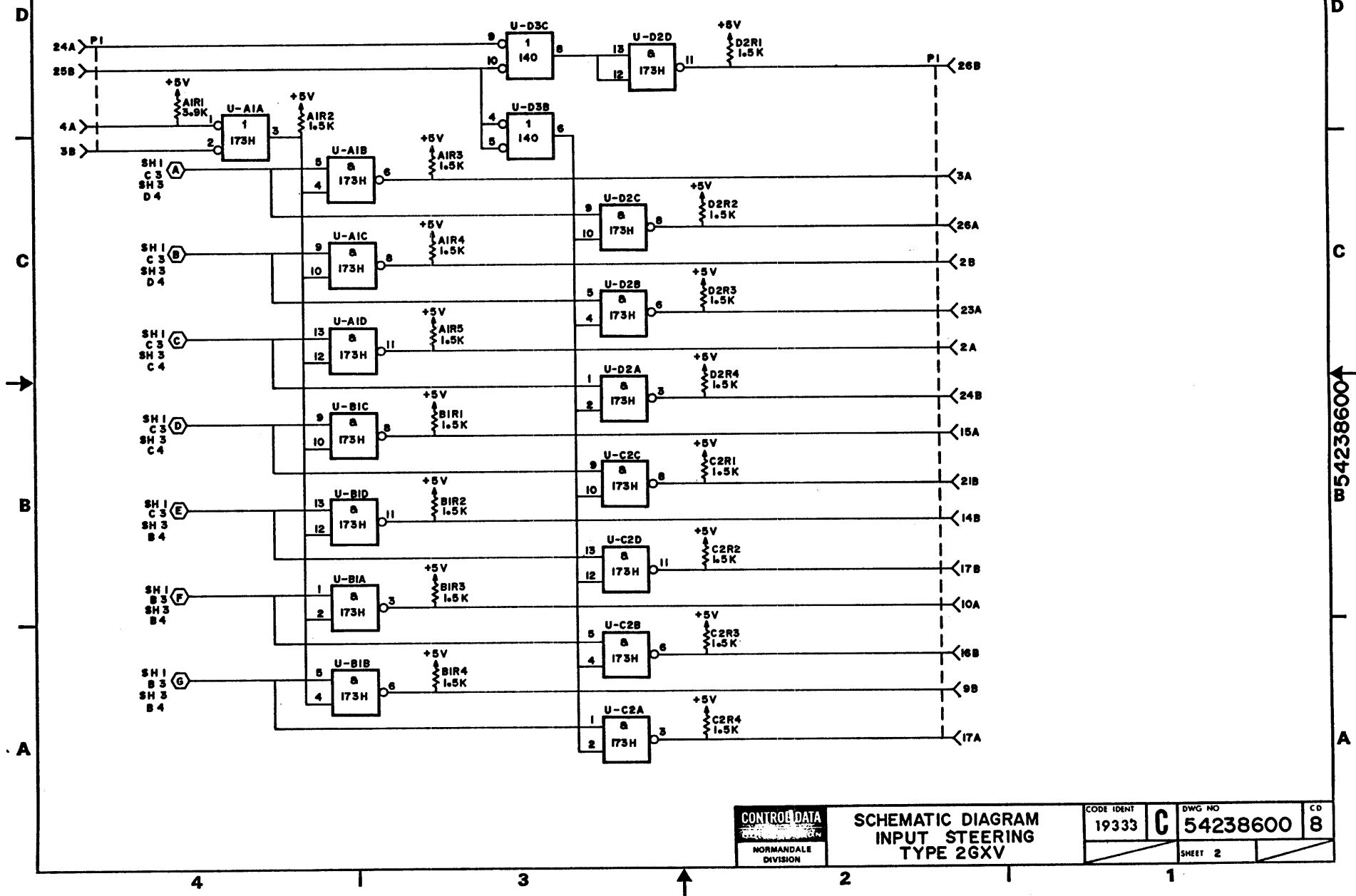
HPD 1

W54238600

4-148

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

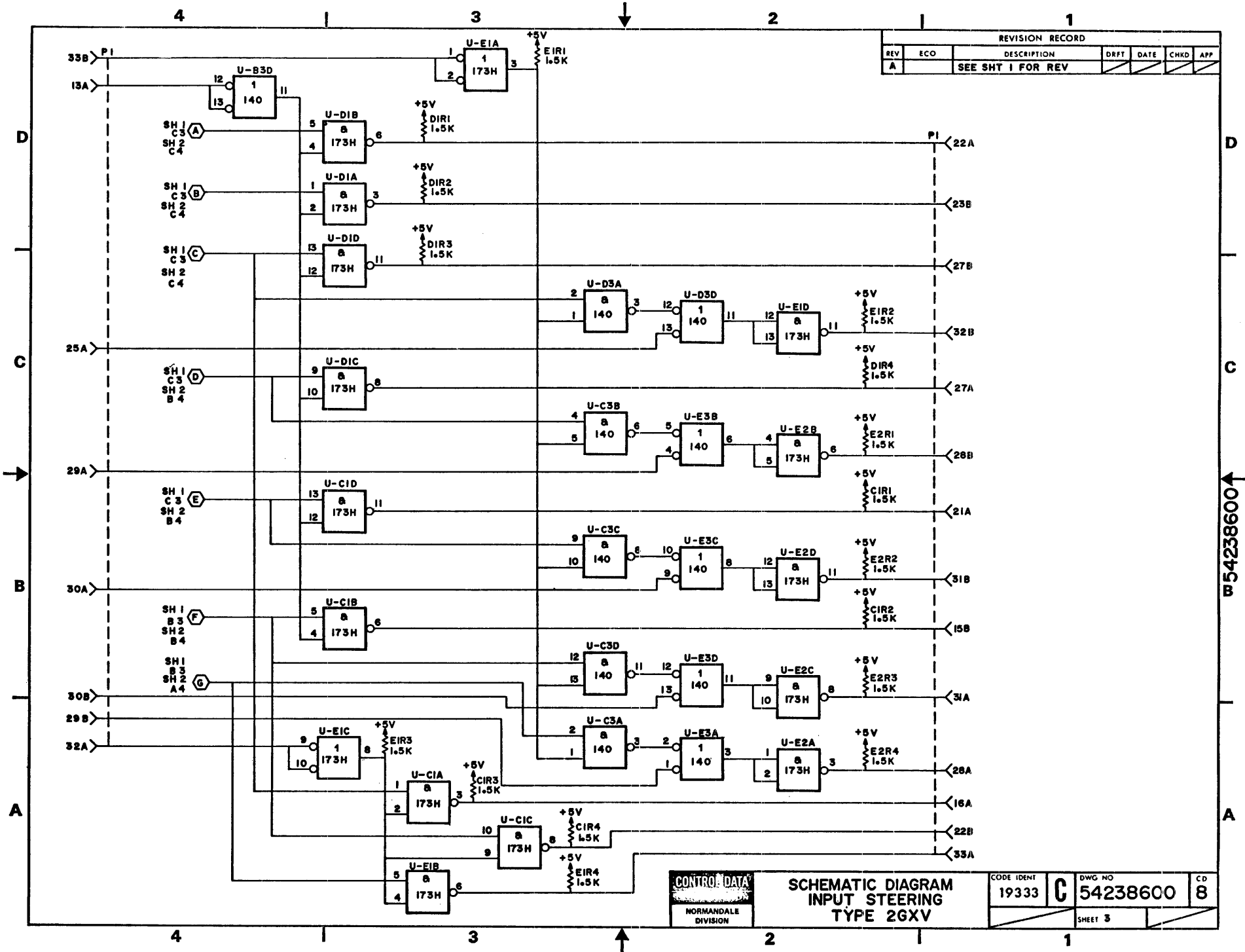


CONTROL DATA
NORMANDEALE
DIVISION

**SCHEMATIC DIAGRAM
INPUT STEERING
TYPE 2GXV**

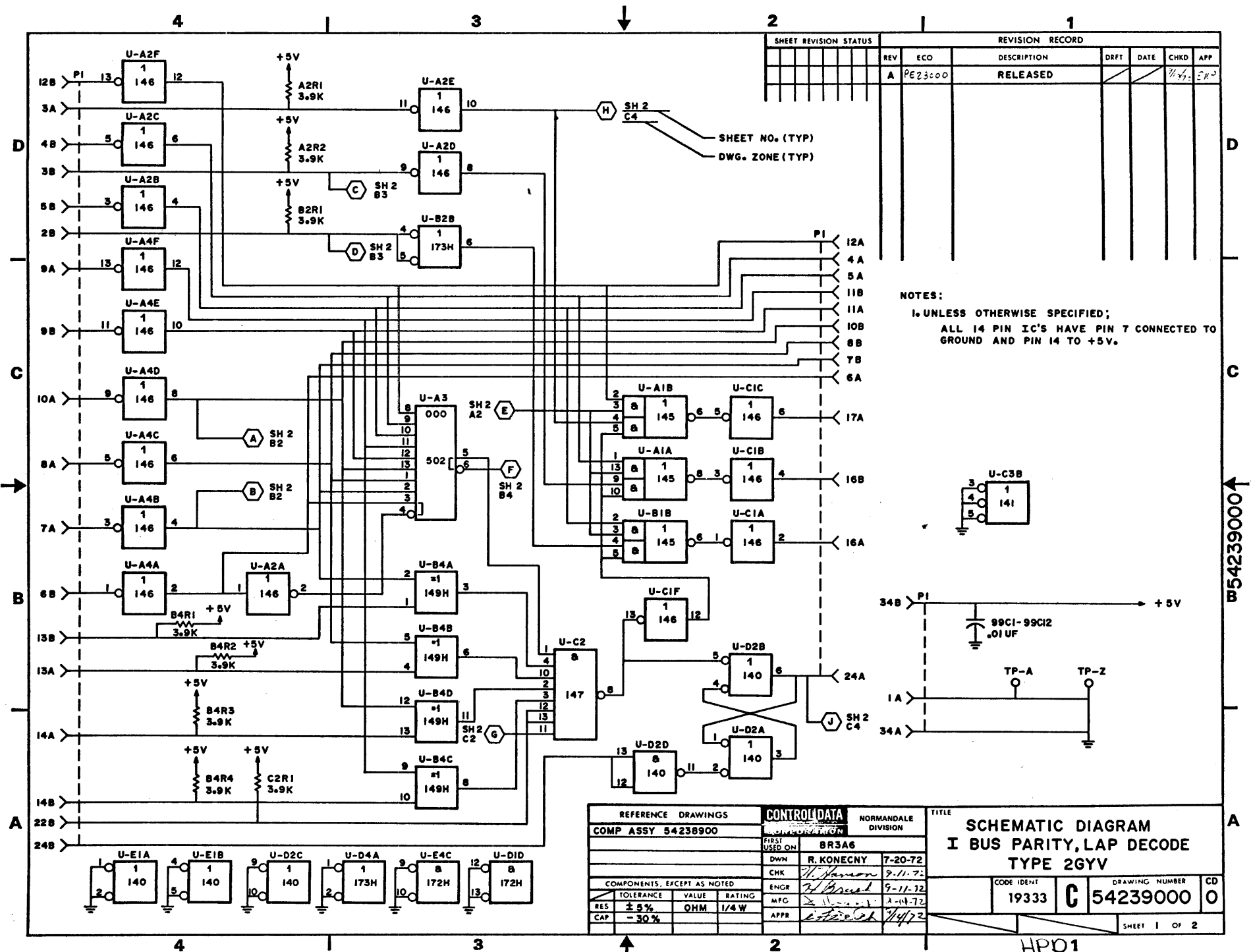
CODE IDENT 19333	DWG NO 54238600	CD 8
SHEET 2		

54238600



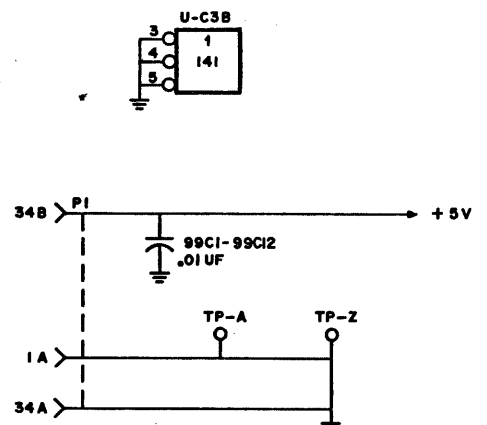
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

 NORMANDALE DIVISION	SCHMATIC DIAGRAM INPUT STEERING TYPE 2GXV		CODE IDENT 19333	DWG NO 54238600	CD 8
				SHEET 3	



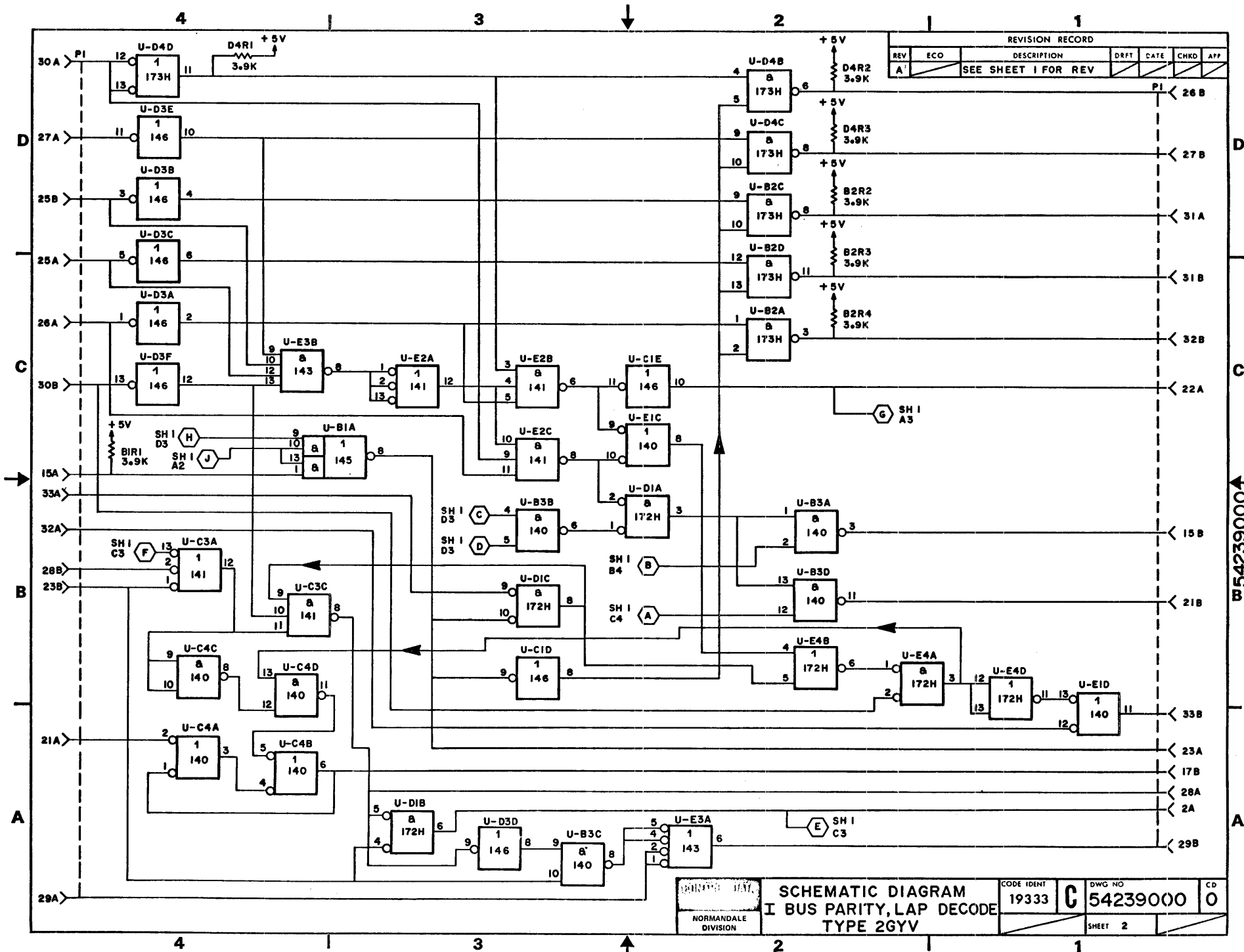
SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					

NOTES:
 1. UNLESS OTHERWISE SPECIFIED;
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 TO +5V.



REFERENCE DRAWINGS COMP ASSY 54238900	CONTROL DATA NORMANDALE DIVISION	TITLE SCHMATIC DIAGRAM I BUS PARITY, LAP DECODE TYPE 2GYV
FIRST USED ON	BR3A6	
DWN	R. KONECNY	7-20-72
CHK	<i>W. Hanson</i>	9-11-72
ENGR	<i>W. Hanson</i>	9-11-72
MFG	<i>W. Hanson</i>	2-14-72
APPR	<i>W. Hanson</i>	11/72
COMPONENTS, EXCEPT AS NOTED		CODE IDENT
TOLERANCE	VALUE	RATING
RES	± 5%	OHM 1/4 W
CAP	- 30%	
DRAWING NUMBER		CD
19333 C 54239000		0
SHEET 1 OF 2		

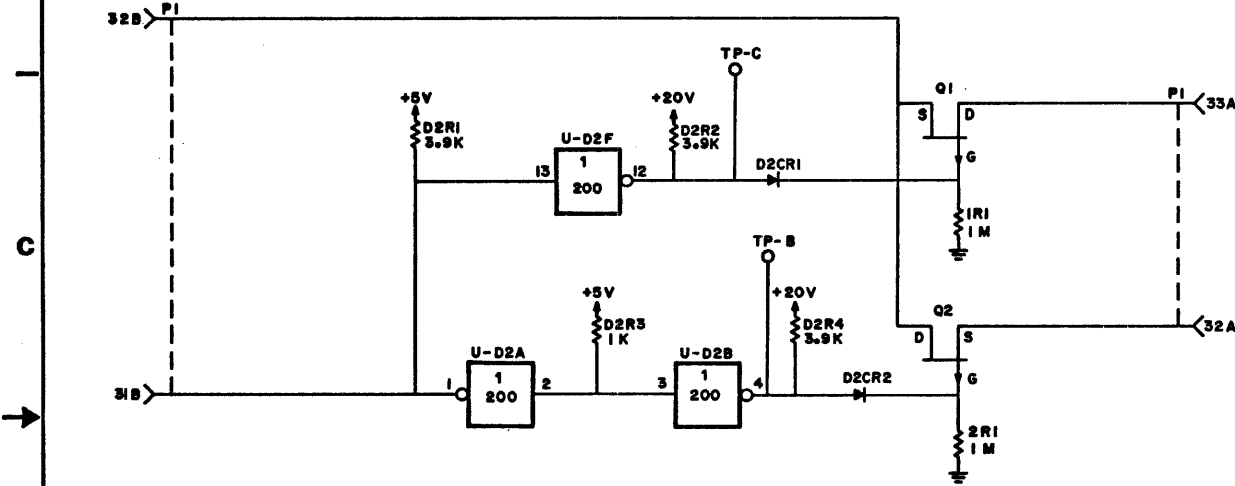
HPD1



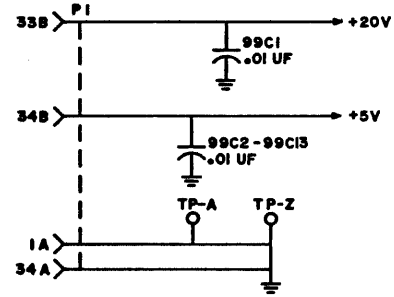
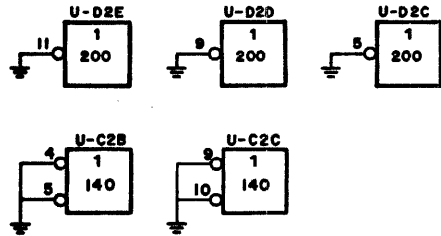
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

NORMANDE DIVISION	SCHEMATIC DIAGRAM I BUS PARITY, LAP DECODE TYPE 2GYV	CODE IDENT 19333	DWG NO C 54239000	CD 0
			SHEET 2	

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					



NOTE:
 1. UNLESS OTHERWISE SPECIFIED.
 ALL DIODES SILICON, 24553500.
 ALL TRANSISTORS FET, 2N5019, 50218200,
 2. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



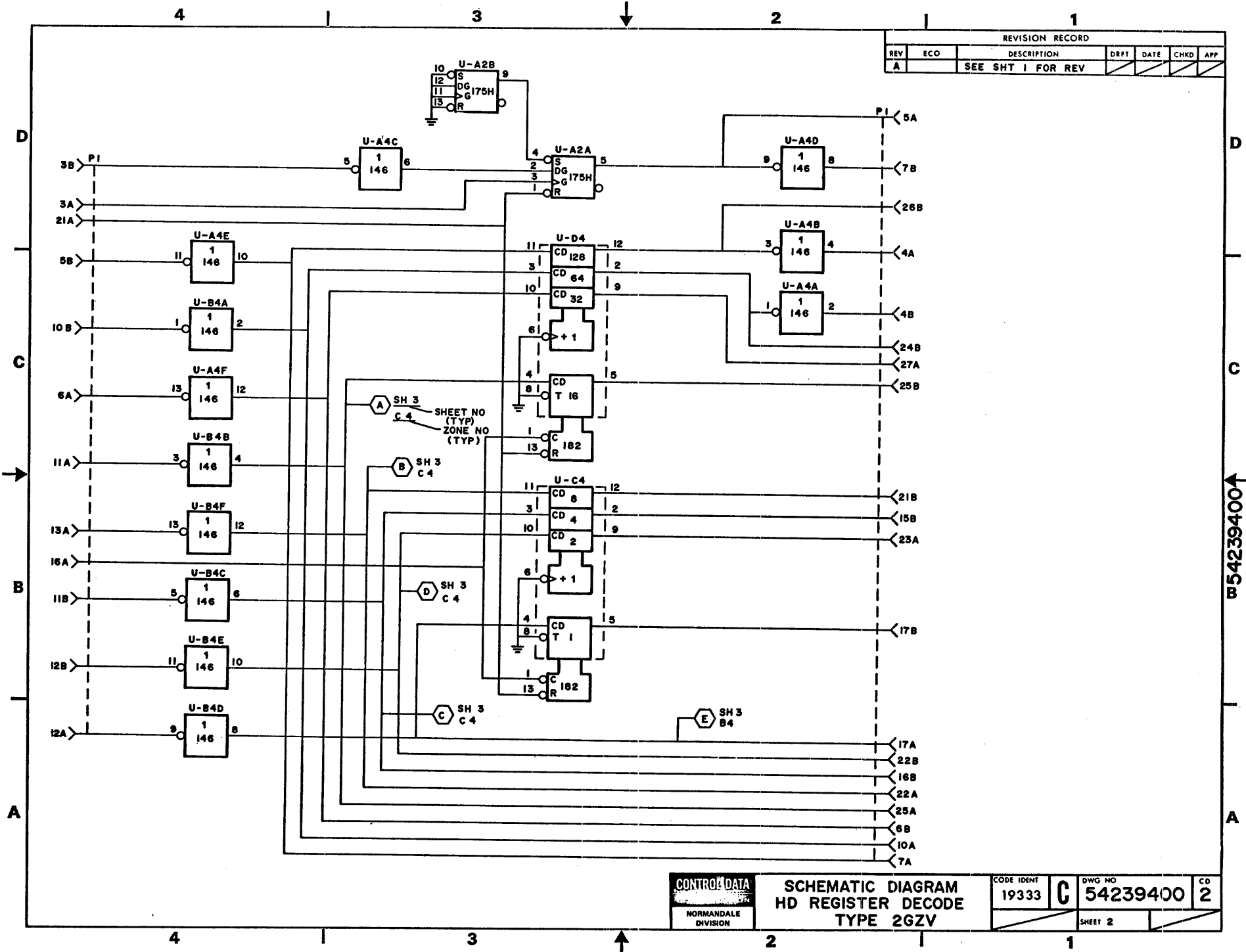
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY	54239300	FIRST USED ON	BR3A6	DWN	K. STREETER	7-13-72	SCHEMATIC DIAGRAM HD REGISTER DECODE TYPE 2GZV
		CHK		ENGR			
		MFG		APPR			
COMPONENTS, EXCEPT AS NOTED							
TOLERANCE	VALUE	RATING					
RES ±5%	OHMS	1/4 W					
CAP -30%							
				CODE IDENT	DRAWING NUMBER	CD	
				19333	C 54239400	2	
SHEET 1 OF 3							

54239400

70629100 E

4-153

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDALE
DIVISION

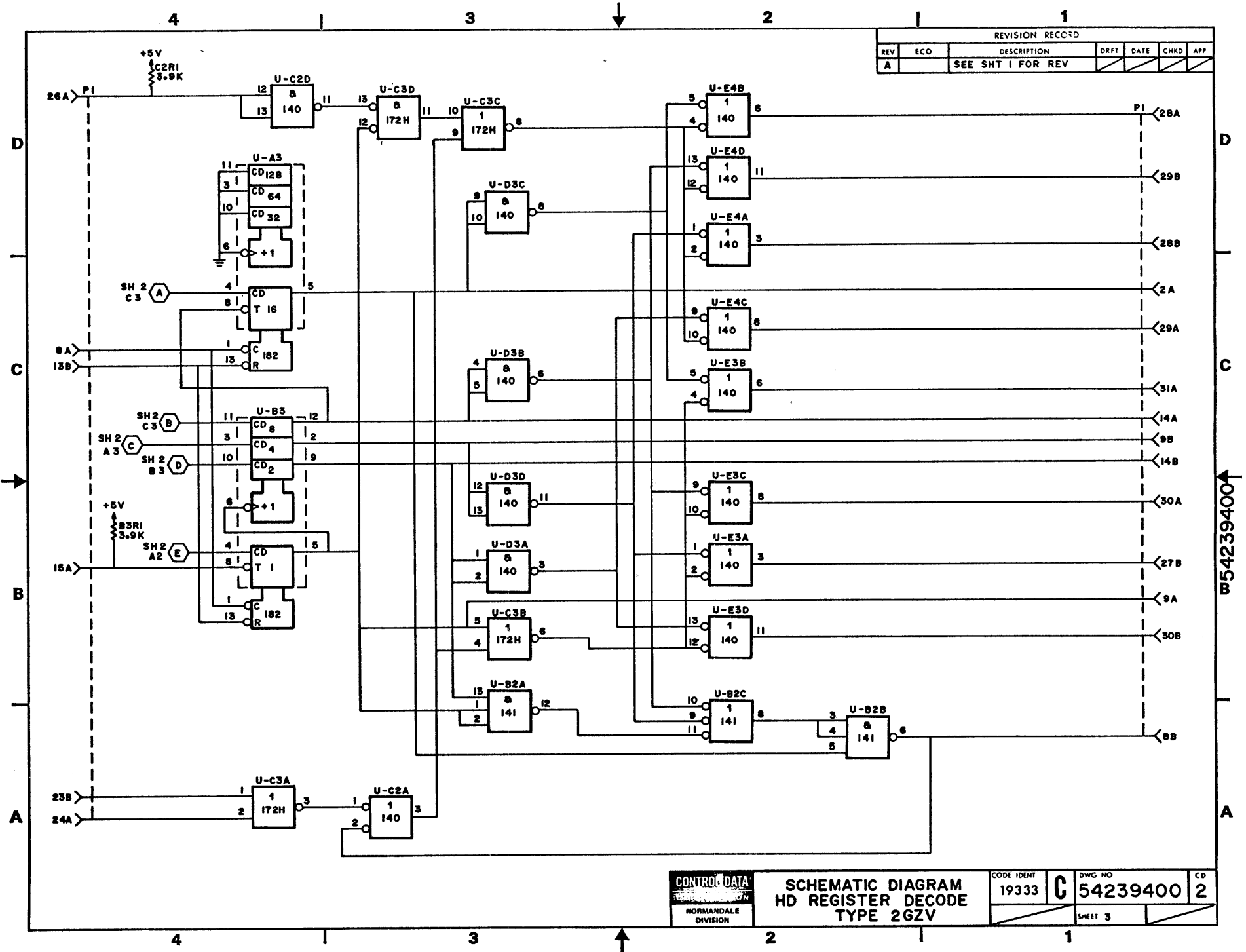
SCHMATIC DIAGRAM
HD REGISTER DECODE
TYPE 2GZV

CODE IDENT 19333	DWG NO 54239400	CD 2
SHEET 2		

4-154

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

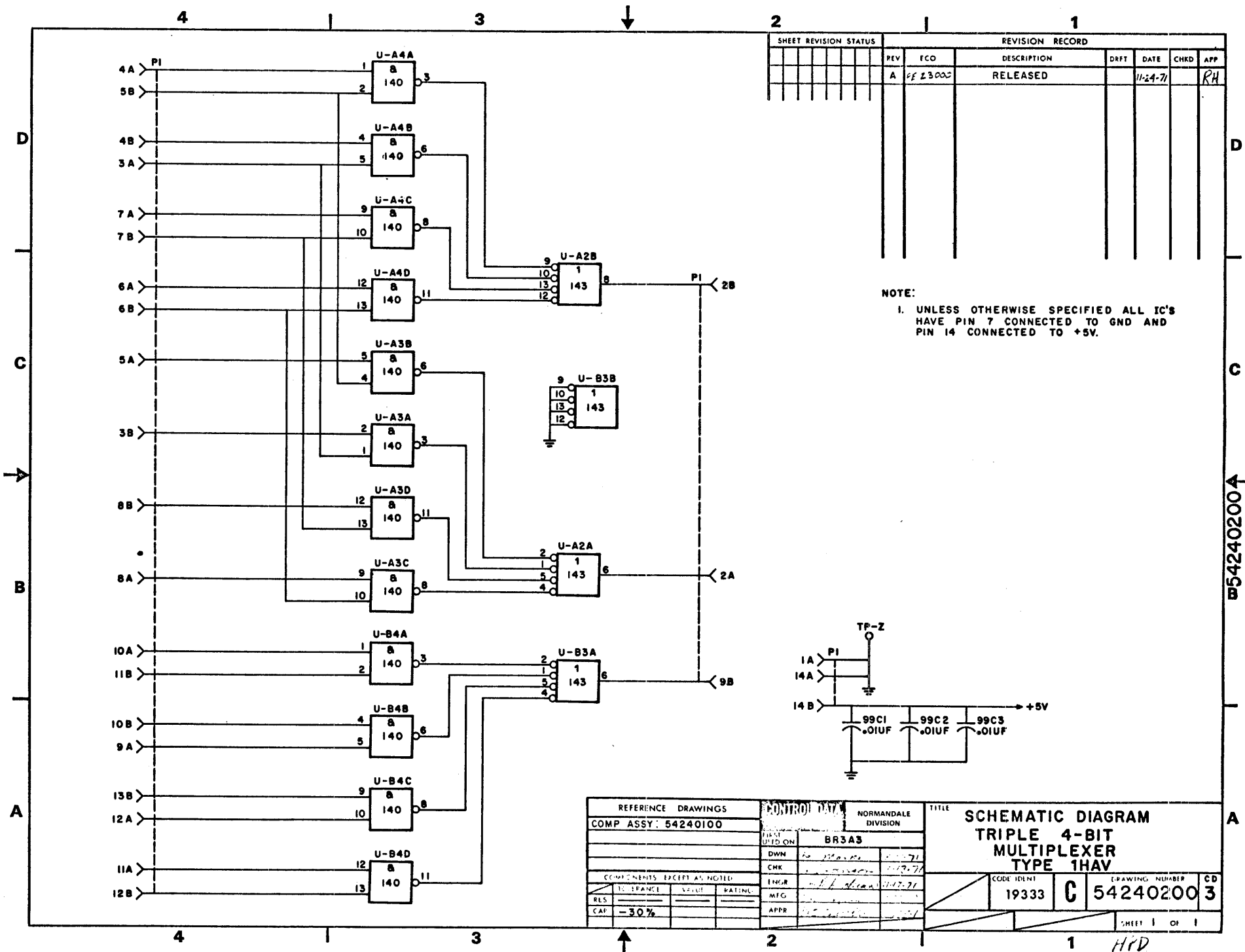


 NORMANDEALE DIVISION	SCHEMATIC DIAGRAM HD REGISTER DECODE TYPE 2GZV		CODE IDENT 19333	DWG NO C 54239400	CD 2
				SHEET 3	

W54239400

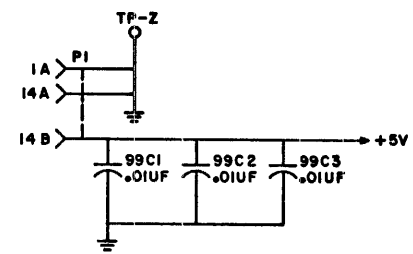
70629100 E

4-155



SHEET REVISION STATUS				REVISION RECORD					
REV	ECO	DESCRIPTION	DRAFT	DATE	CHKD	APP			
A	2300C	RELEASED		11-24-71		RH			

NOTE:
 1. UNLESS OTHERWISE SPECIFIED ALL IC'S
 HAVE PIN 7 CONNECTED TO GND AND
 PIN 14 CONNECTED TO +5V.



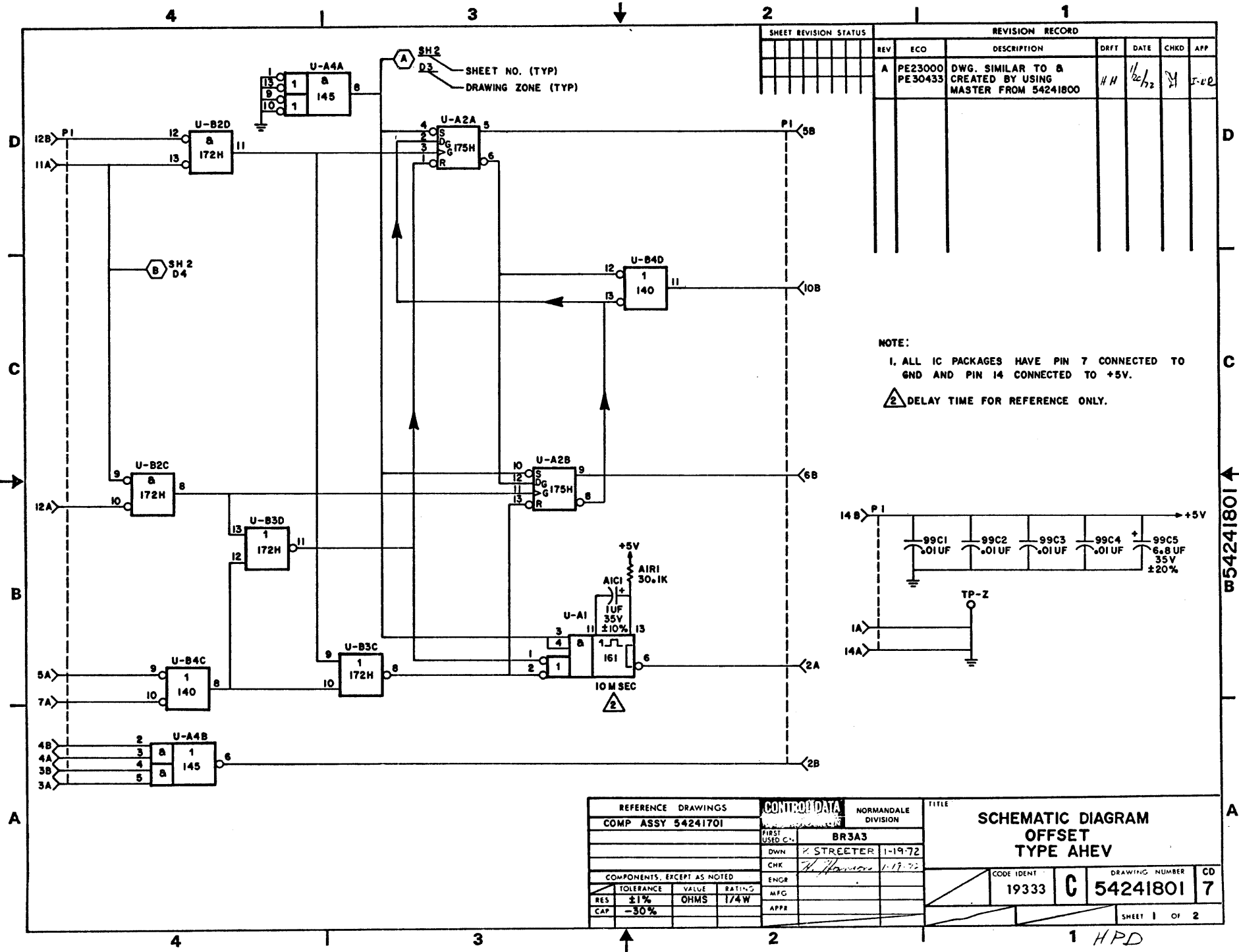
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54240100		BR3A3				SCHEMATIC DIAGRAM	
						TRIPLE 4-BIT	
						MULTIPLEXER	
						TYPE 1H4V	
COMPONENTS EXCEPT AS NOTED		ENGR		DATE		CODE IDENT	
DES	TO: FRANCE	DATE	WFG			19333	DRAWING NUMBER
CAT	-30%		APPR			C 54240200	CD
						SHEET 1 OF 1	

HPD

54240200

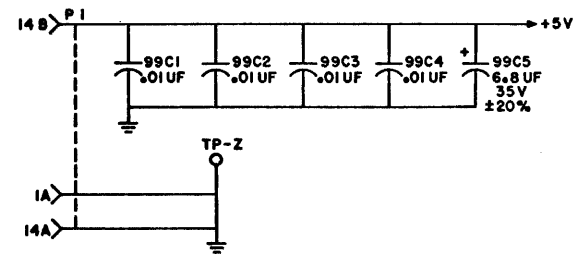
4-156

70629100 E



SHEET REVISION STATUS				REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE23000 PE30433	DWG. SIMILAR TO B CREATED BY USING MASTER FROM 54241800	H H	1/22/72		I-22			

NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54241701		BR3A3		DWN K. STREETER 1-19-72		SCHEMATIC DIAGRAM OFFSET TYPE AHEV	
COMPONENTS, EXCEPT AS NOTED		ENGR		CHK H. HANSEN 1-19-72		CODE IDENT	
RES	±1%	VALUE	RATING	APPR	19333	DRAWING NUMBER	CD
CAP	-30%	OHMS	1/4W		C	54241801	7
						SHEET 1 OF 2	

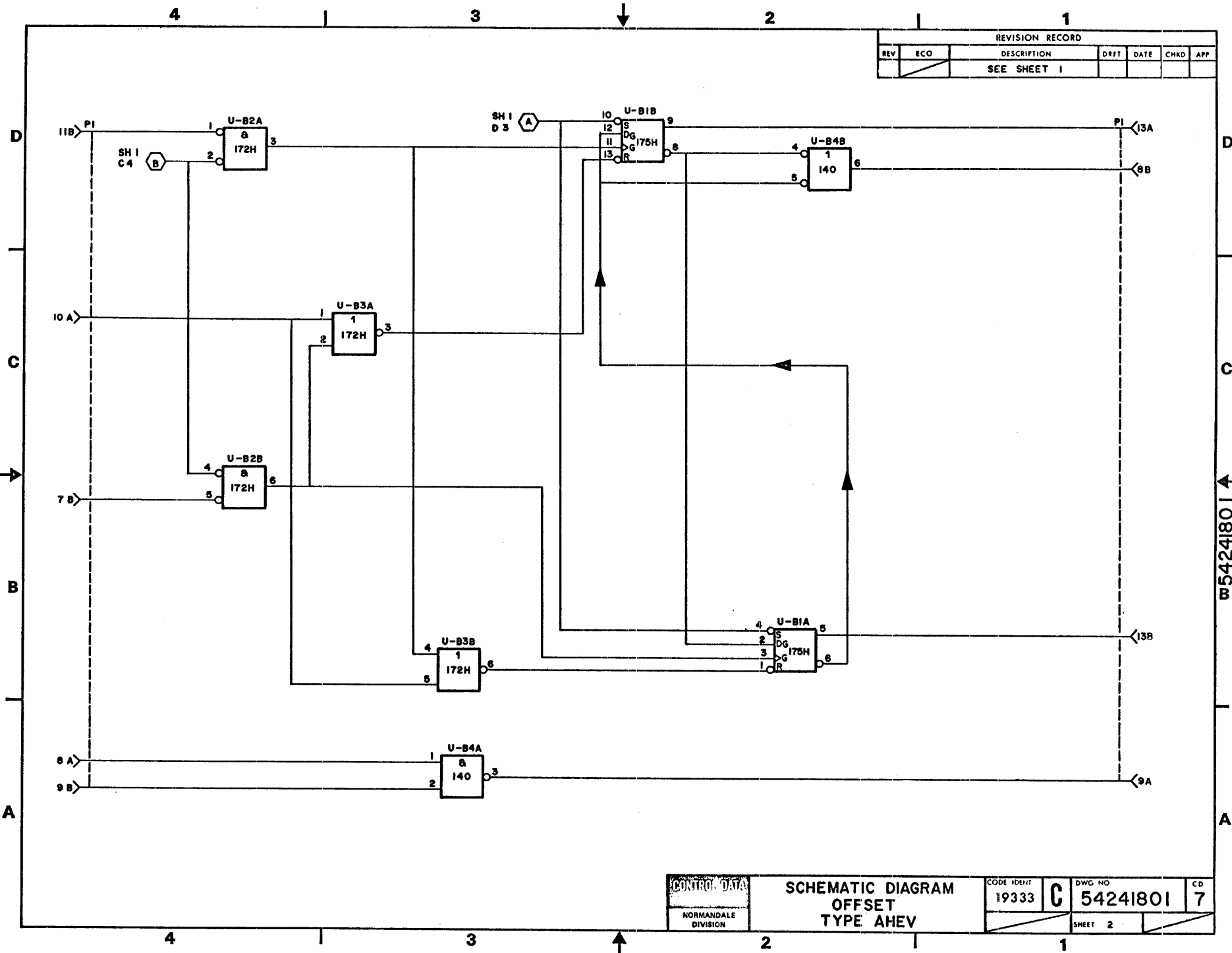
1 HPD

54241801

70629100 E

4-157

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
		SEE SHEET 1				



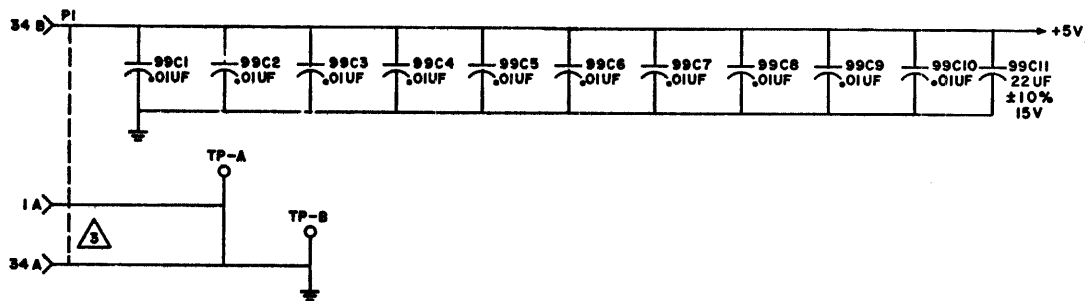
CONTROL DATA NORMANVILLE DIVISION	SCHEMATIC DIAGRAM OFFSET TYPE AHEV		CODE IDENT 19333	DWG NO C 54241801	CD 7
				SHEET 2	

W54241801

4-158

70629100 E

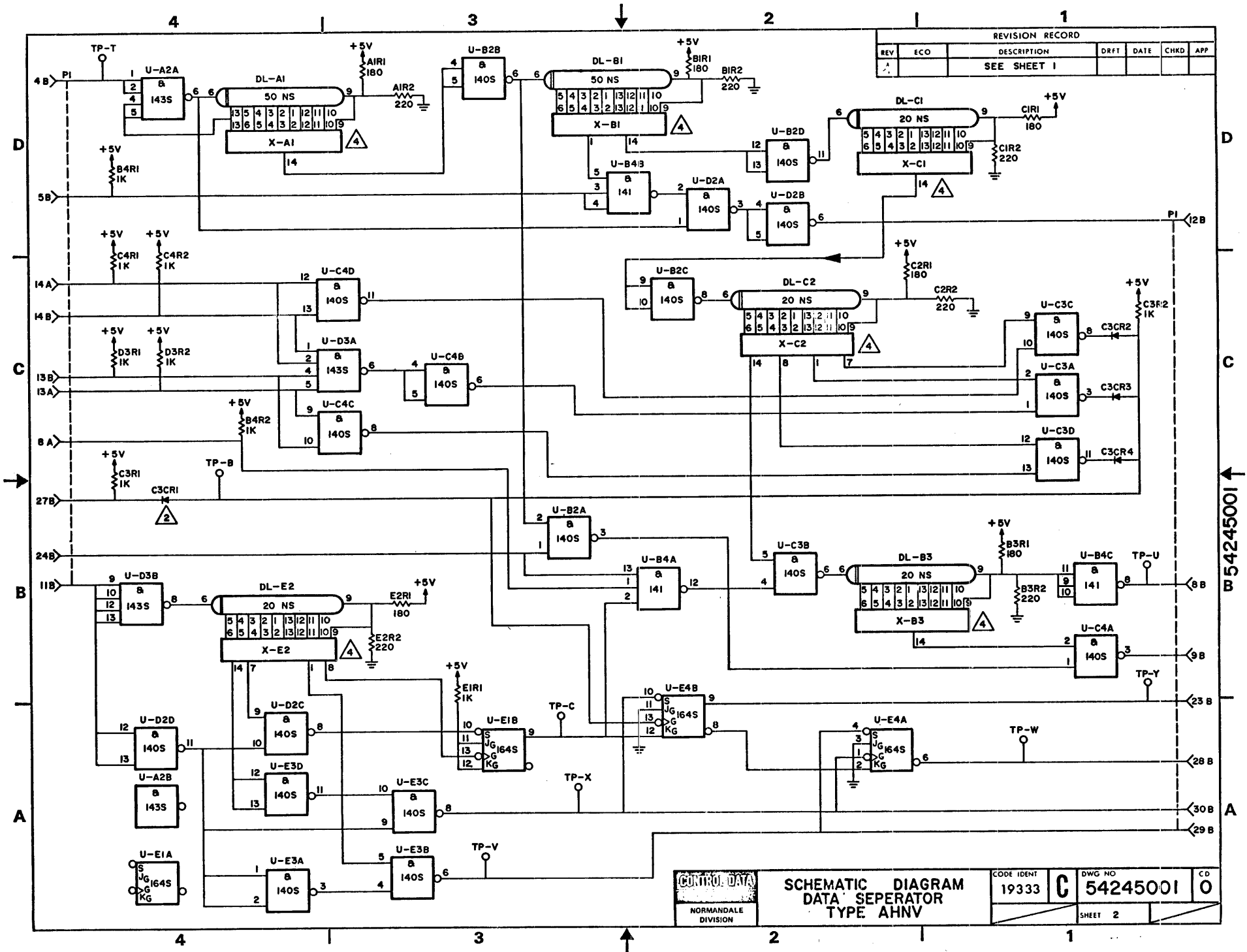
SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE230-0	RELEASED		2-8-72					



- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
ALL DIODES, SHOTTKY BARRIER, 50241400.
 - DIODE, SILICON, 92115023.
 - CONNECTOR PINS 2A THRU 7A ARE CONNECTED TO GND.
 - JUMPER PLUG-DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 - MATCHED WITH AHPV PER ENGINEERING TEST PROCEDURE.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMP ASSY 54244901		FIRST USED ON		BR3A3		SCHEMATIC DIAGRAM DATA SEPARATOR TYPE AHPV	
		DWN	K STREETER	1-13-72			
		CHK	<i>[Signature]</i>	1-21-72			
		ENGR	<i>[Signature]</i>	1-21-72			
		MFG	<i>[Signature]</i>	2-11-72			
		APPR	<i>[Signature]</i>	2-3-72			
COMPONENTS, EXCEPT AS NOTED				CODE IDENT	19333	DRAWING NUMBER	54245001
TOLERANCE	VALUE	RATING					C.D.
RES	+5%	OHMS	1/4 W				0
CAP	-30%						
						SHEET 1 OF 2	

54245001



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
1		SEE SHEET 1				

CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM DATA SEPARATOR TYPE AHNV		CODE IDENT 19333	DWG NO 54245001	CD 0
				SHEET 2	

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	23000	RELEASED		3-8-72			

D

C

B

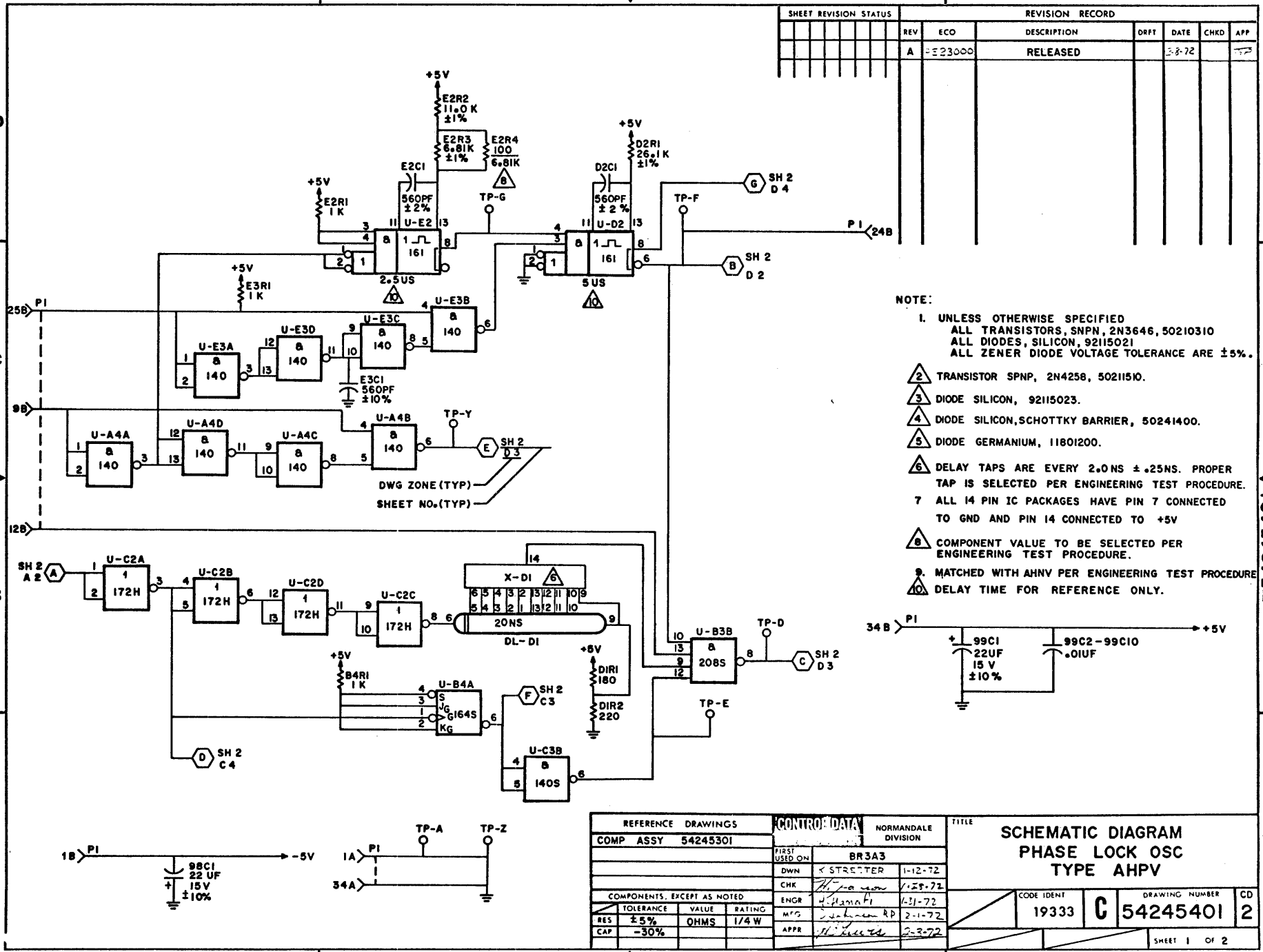
A

D

C

B54245401 ↑

A



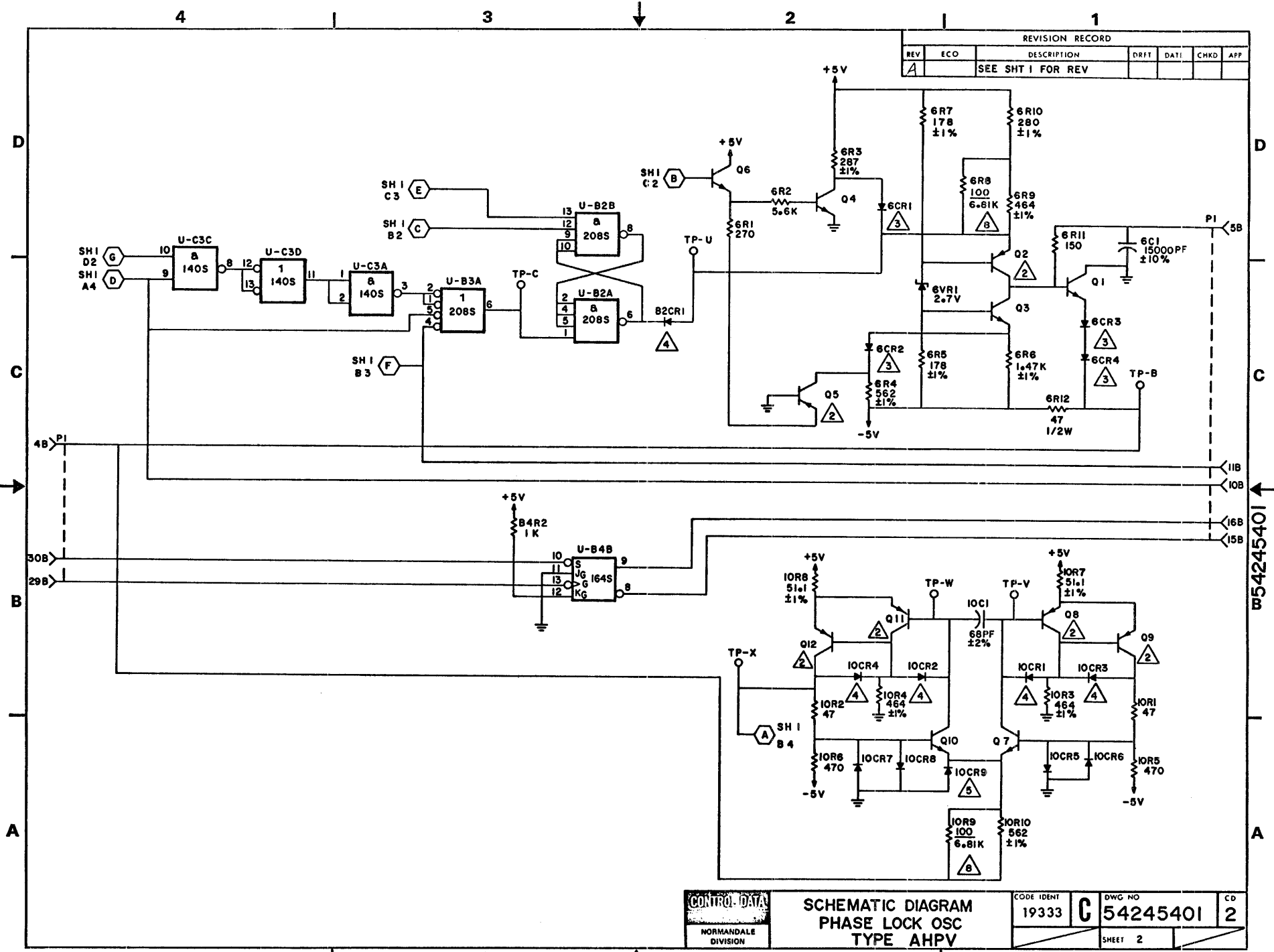
- NOTE:
- UNLESS OTHERWISE SPECIFIED
ALL TRANSISTORS, SNPN, 2N3646, 50210310
ALL DIODES, SILICON, 92115021
ALL ZENER DIODE VOLTAGE TOLERANCE ARE ±5%.
 - TRANSISTOR SPNP, 2N4258, 50211510.
 - DIODE SILICON, 92115023.
 - DIODE SILICON, SCHOTTKY BARRIER, 50241400.
 - DIODE GERMANIUM, 11801200.
 - DELAY TAPS ARE EVERY 2.0NS ±.25NS. PROPER TAP IS SELECTED PER ENGINEERING TEST PROCEDURE.
 - ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 - COMPONENT VALUE TO BE SELECTED PER ENGINEERING TEST PROCEDURE.
 - MATCHED WITH AHPV PER ENGINEERING TEST PROCEDURE
DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION	
COMP	ASSY	FIRST USED ON	BR3A3		
	54245301	DWN	X STRETTER	1-12-72	
COMPONENTS, EXCEPT AS NOTED		CHK	<i>[Signature]</i>	1-15-72	
TOLERANCE	VALUE	RATING	ENGR	4/11-72	
RES	±5%	OHMS	M/S	2-1-72	
CAP	-30%		APPR	2-2-72	

TITLE			
SCHEMATIC DIAGRAM PHASE LOCK OSC TYPE AHPV			
CODE IDENT	DRAWING NUMBER	CD	
19333	C 54245401	2	
SHEET 1 OF 2			

HPD

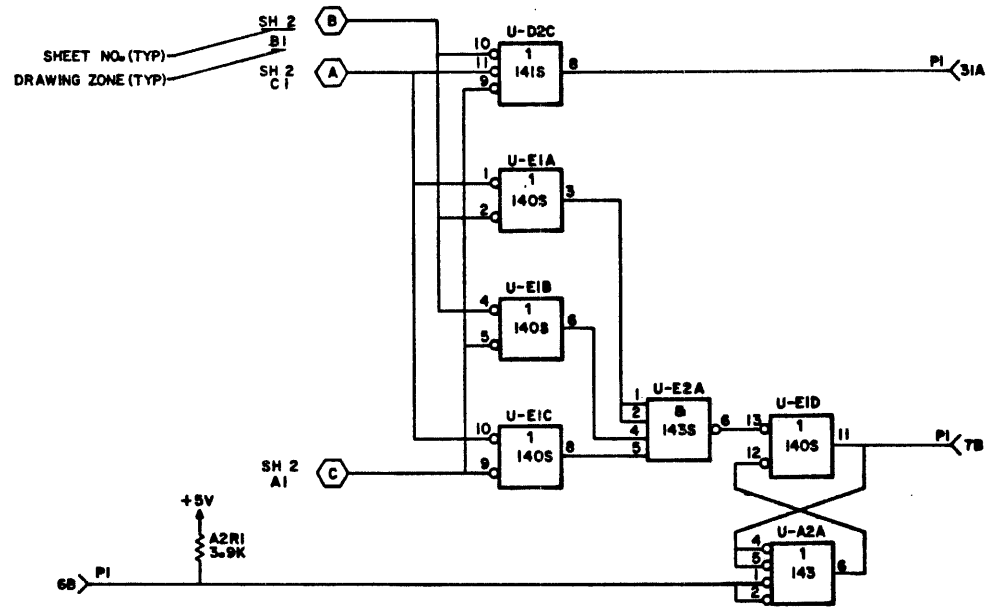
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



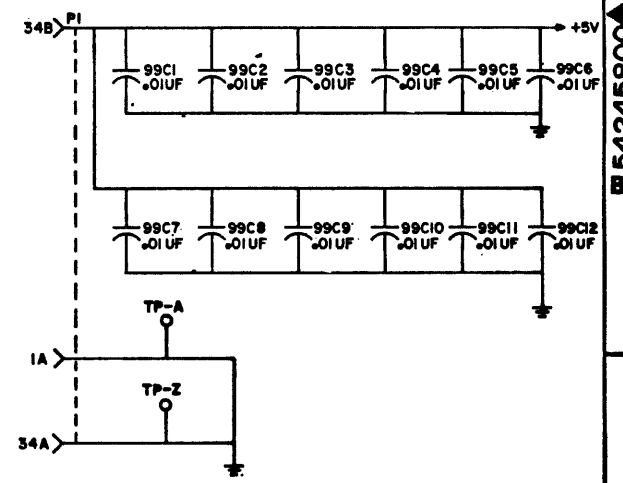
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM PHASE LOCK OSC TYPE AHPV		CODE IDENT 19333	DWG NO C 54245401	CD 2
			SHEET 2		

HPD

SHEET REVISION STATUS		REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	D.	
A	FE 23-000	RELEASED			12-71



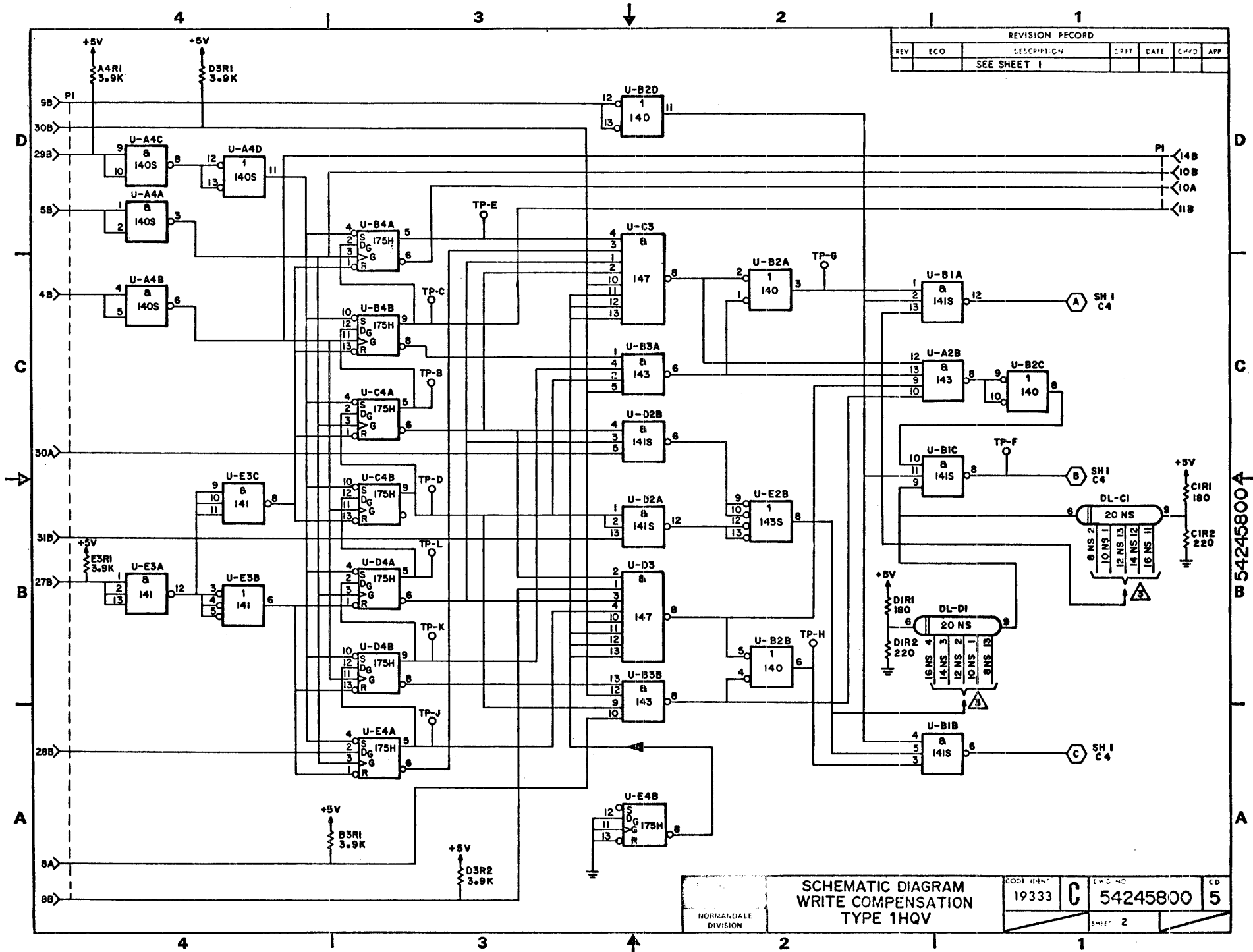
- NOTES:
- ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - DELAY LINES C1 AND D1 HAVE PINS 7 AND 8 CONNECTED TO GND.
 - DELAY TAPS ARE EVERY 2.00 ± 0.25 NS. DELAY TIME TO BE SELECTED PER ENGINEERING TEST PROCEDURE.



REFERENCE DRAWINGS		NORMANDEALE DIVISION		TITLE	
COMP ASSY 54245700		BR3A3		SCHEMATIC DIAGRAM	
		R. BOCHE 11-9-71		WRITE COMPENSATION	
		2/6/71		TYPE 1HQV	
COMPONENTS EXCEPT AS NOTED		2/6/71		CODE IDENT	
RES	± 5%	CHMS	1/4 W	19333	C
CAP	-30%			DRAWING NUMBER	
		2/9-71		54245800	
				CD	
				5	
				SHEET 1 OF 2	

HPD

REVISION RECORD						
REV	ECO	DESCRPT. CH	EFF	DATE	CHKD	APP
		SEE SHEET 1				



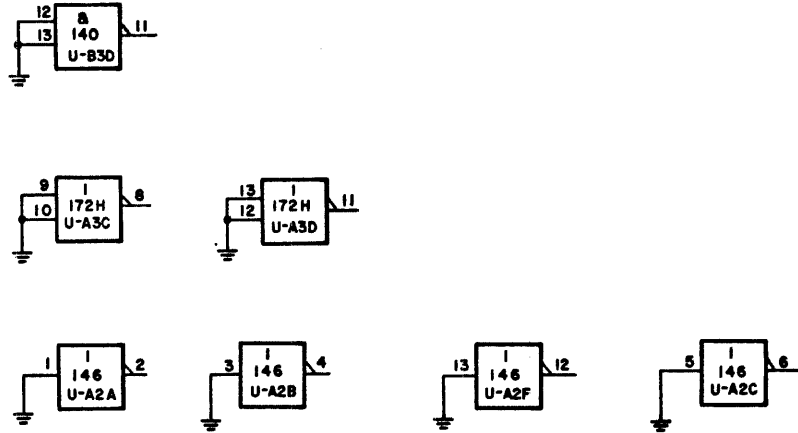
NORMAL-DALE DIVISION	SCHEMATIC DIAGRAM WRITE COMPENSATION TYPE 1HQV		CODE 11-44 19333	CD NO C 54245800	CD 5
				SHEET 2	

4-164

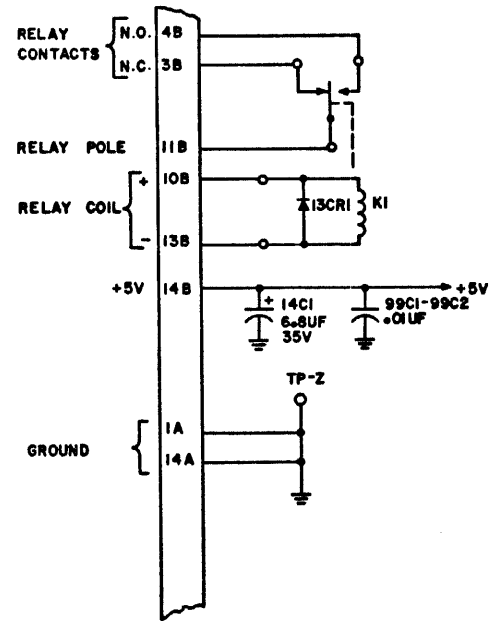
70629100 E

SHEET REVISION STATUS					REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	230000	RELEASED		11-29-73	WPK			

SPARE GATES



NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7
 CONNECTED TO GND AND PIN 14 CONNECTED
 TO +5V.
 DIODE, SILICON 92115023
 RELAY, FIND NO. 7, PN.94366100.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY. 54250900		BR 388		DWN V. WILSON		SCHEMATIC DIAGRAM	
				7/27/73		POWER INTERRUPT	
				7-21-73		TYPE 3JCV	
COMPONENTS, EXCEPT AS NOTED				ENGR		CODE IDENT	
TOLERANCE		VALU		MFG		DRAWING NUMBER	
RES		CAP		APPR		19333	
-30%						54251000	
						CD 3	
				SCALE 2/1		SHEET 1 OF 2	

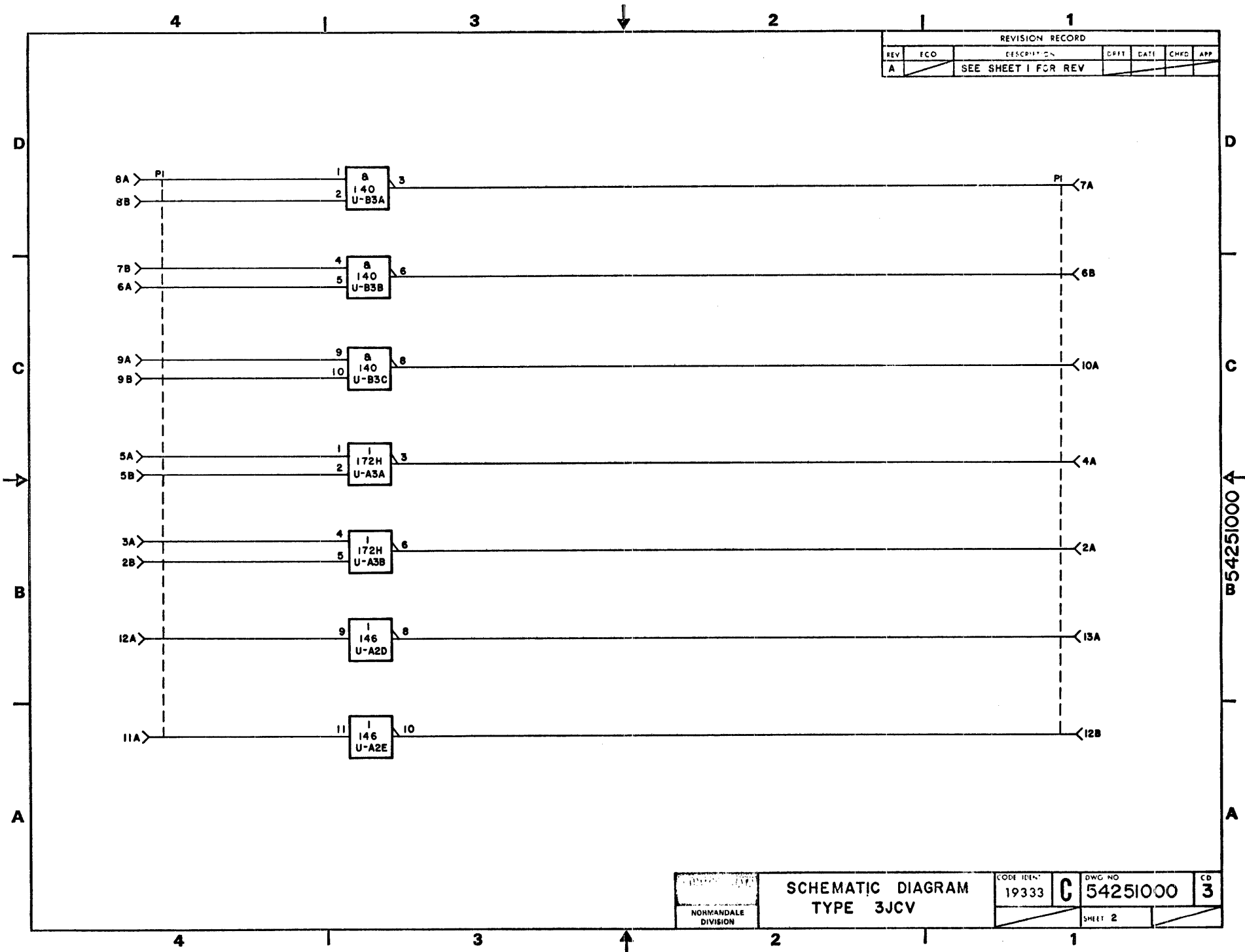
W 54251000

HPD-C

70629100 E

4-165

REVISION RECORD						
REV	FCO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



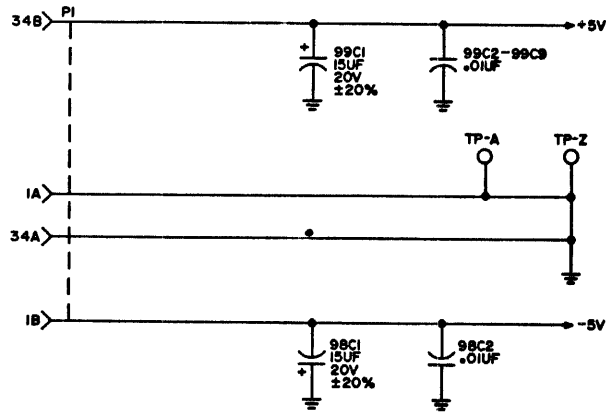
54251000 ↑

4-166

70629100 E

SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE 2311	RELEASED		9-10-73		ck			

NOTE:
 1 UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V.
 2 DELAY TIME FOR REFERENCE ONLY.



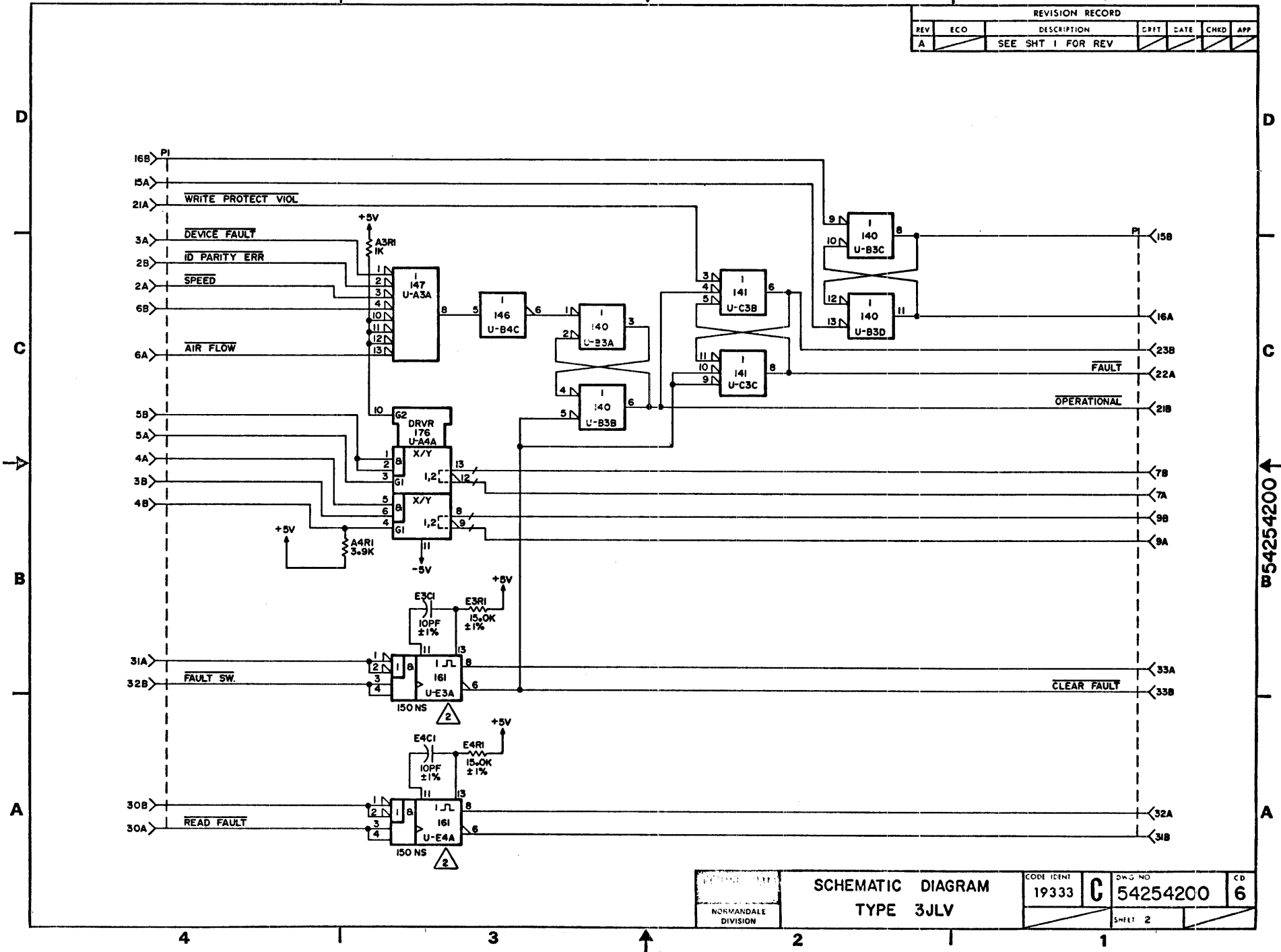
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 5425400		PART USED ON		BR3BB		SCHEMATIC DIAGRAM	
		DWN		MON BAKER		8-10-73	
		ENGR		D. J. K... ..		8-16-73	
		MFG		M. J.		8-20-73	
		APPR		...		8-24-73	
COMPONENTS EXCEPT AS NOTED				CODE IDENT		DRAWING NUMBER	
TOLERANCE		VALUE		RATING		19333 C 54254200	
RES ±5%		OHMS		1/4 W		CD 6	
CAP -30%							
						SHEET 1 OF 3	
						HP D-E	

54254200

70629100 E

4-167

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				

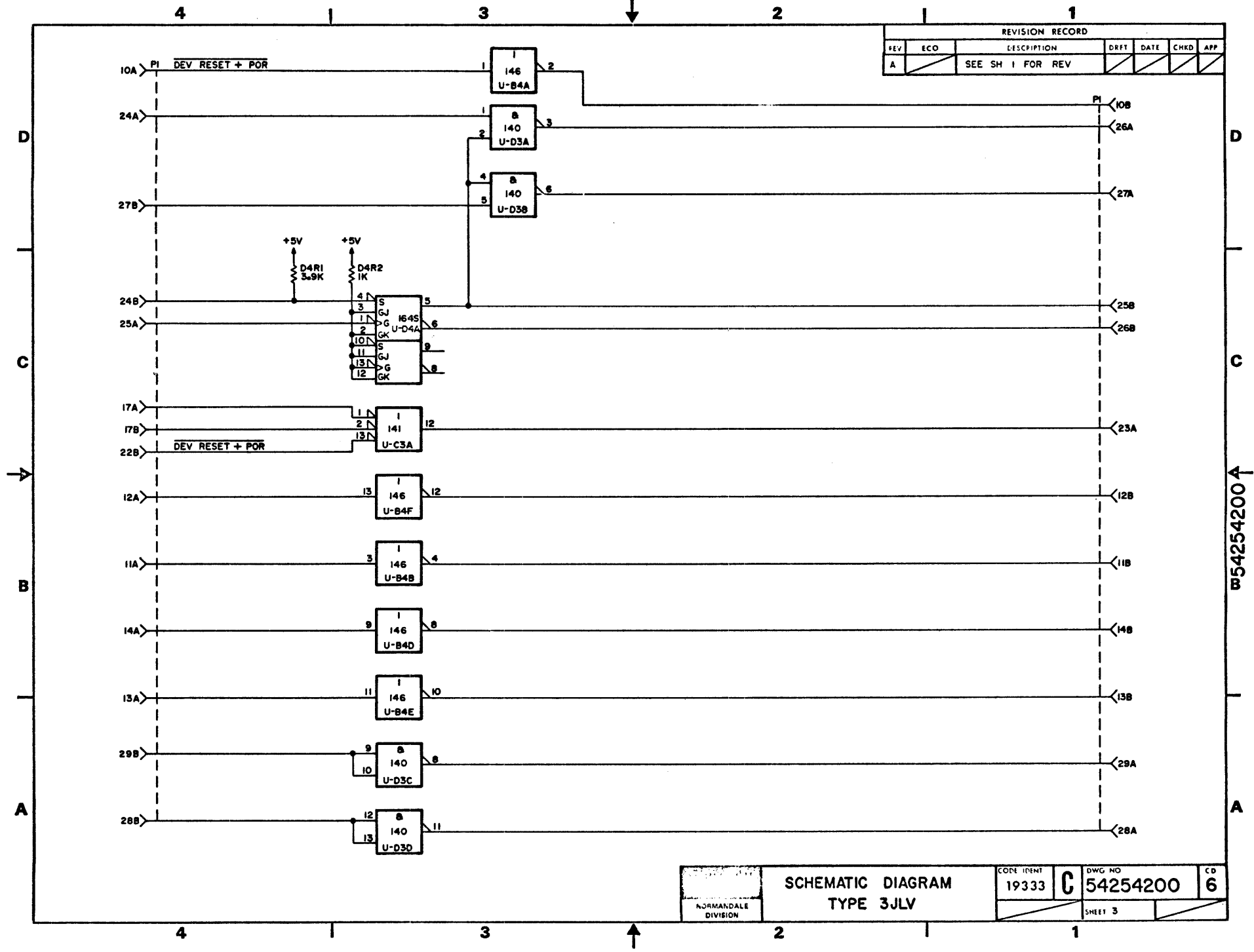


NORMANDE DIVISION	SCHEMATIC DIAGRAM TYPE 3JLV	CODE IDENT	19333	DWG NO 54254200	CD 6
		SHEET	2		

4-168

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				



NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JLV		CODE IDENT 19333	DWG NO C 54254200	CD 6
				SHEET 3	

W54254200

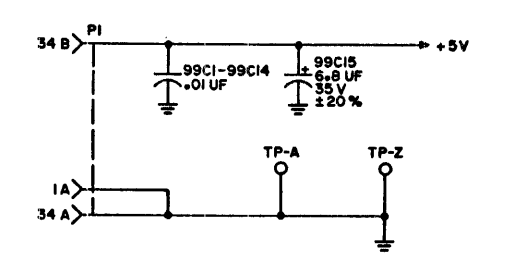
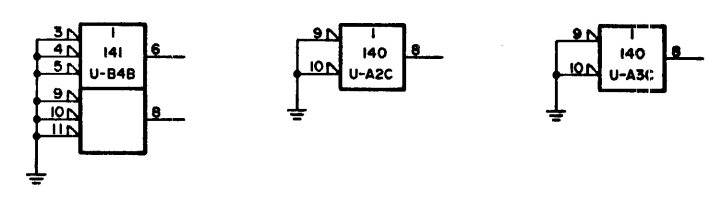
70629100 E

4-169

SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	E-3000	RELEASED		9-12-73		OK	

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V.
 ALL DIODES, GERMANIUM, 11801200.
 ⚠ DELAY TIME FOR REF ONLY.

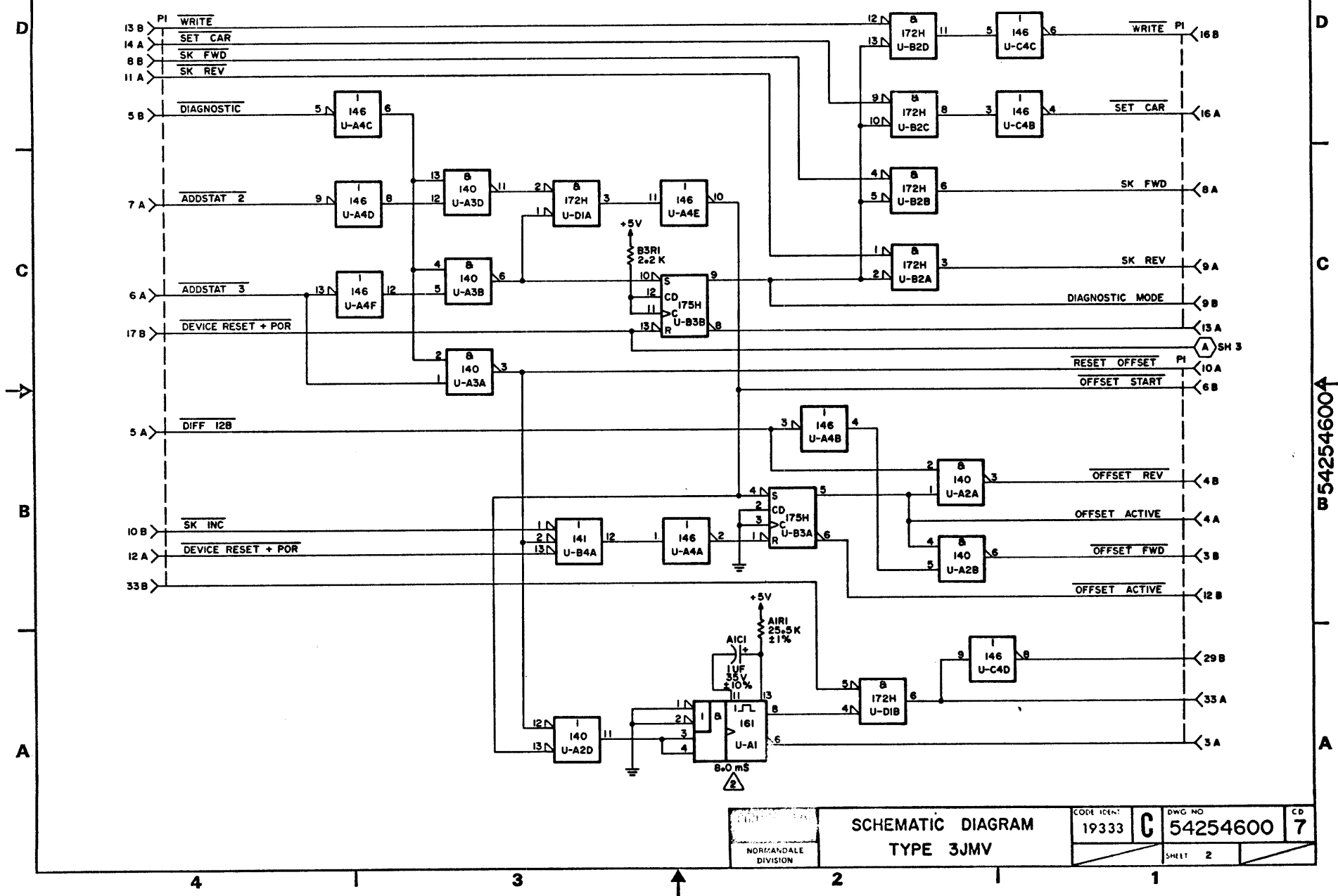
SPARE GATES



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54254500		FIRST USED ON BR3B8		DWN 8-9-73		SCHEMATIC DIAGRAM DIAGNOSTIC AND OFFSET TYPE 3JMV	
COMPONENTS, EXCEPT AS NOTED		CHK H. S. [Signature]		ENGR H. S. [Signature]		CODE IDENT 19333 C	
TOLERANCE VALUE RATING		MET [Signature]		APPR [Signature]		DRAWING NUMBER 54254600	
RES ± 5%						CD 7	
CAP - 30%						SHEET 1 OF 3	

W54254600A

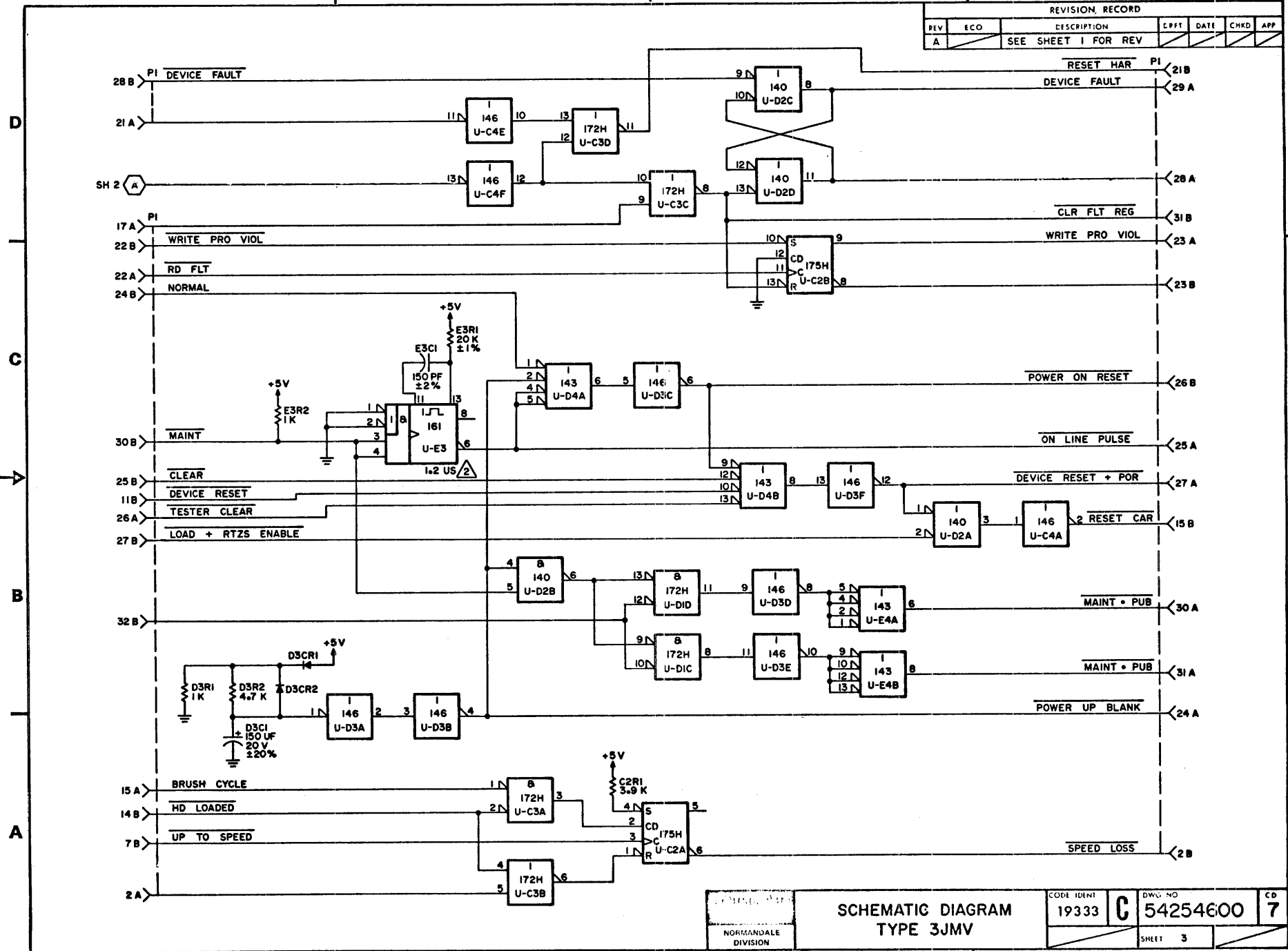
REVISION RECORD						
REV	ECO	DESCRIPTION	CHFT	DATE	CHKC	APP
A		SEE SHEET 1 FOR REV				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM		CODE IDENT: 19333	DWG NO: 54254600	CD: 7
	TYPE 3JMV		SHEET: 2		

54254600

REVISION RECORD						
REV	ECO	DESCRIPTION	LPFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



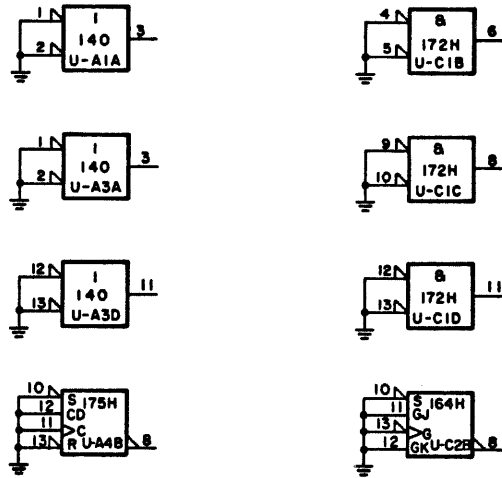
NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JMV		CODE IDENT 19333	C	DWG. NO 54254600	CD 7
					SHEET 3	

W54254600

4-172

70629100 E

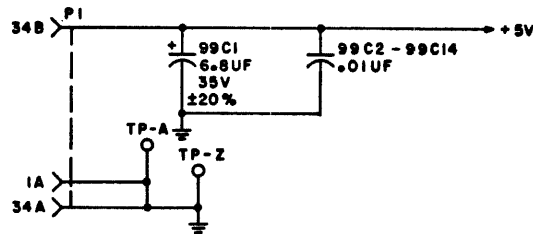
SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	RELEASED	RELEASED		4-10-73		CR	



NOTE:

- 1. UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V
ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GND AND PIN 16 TO +5V.

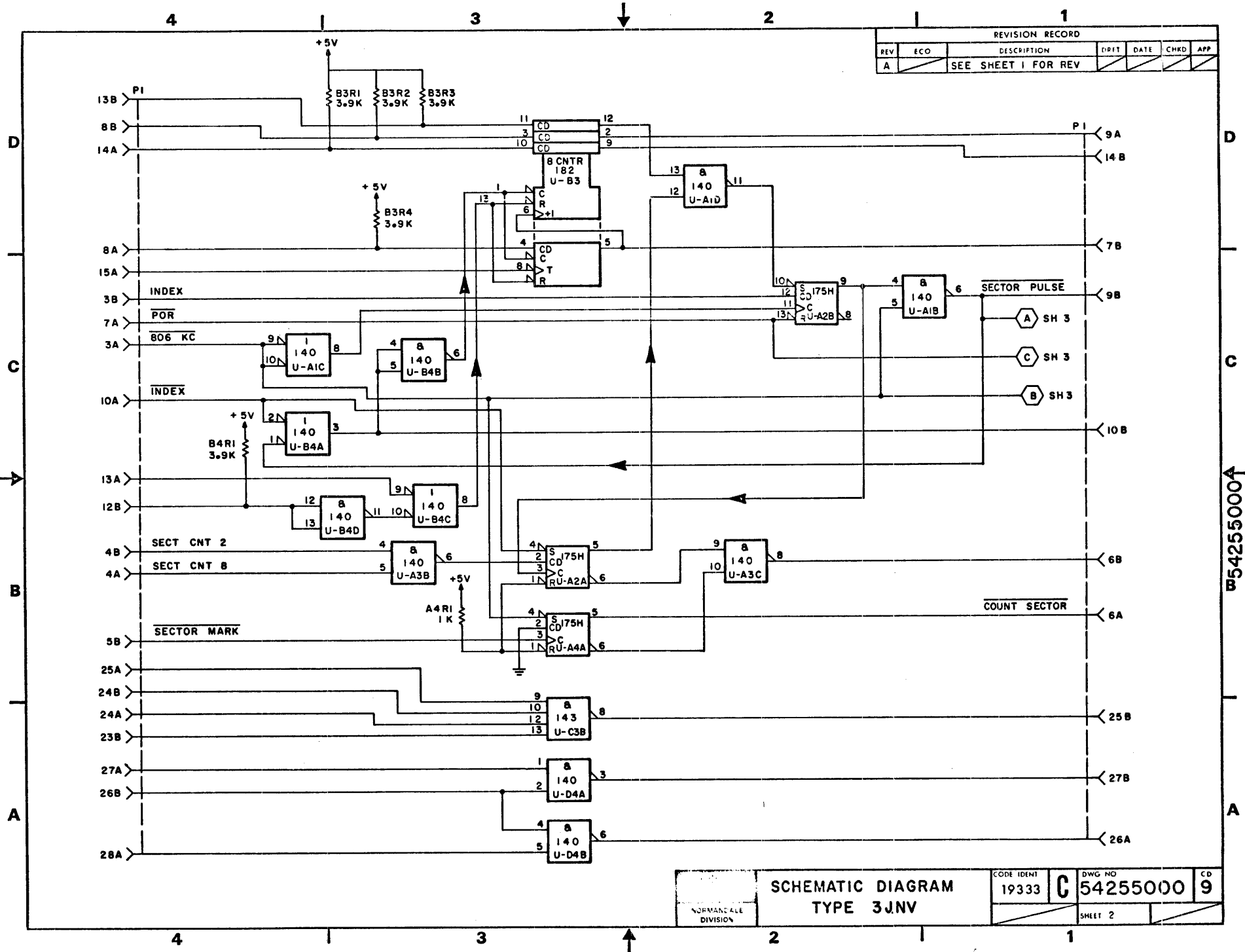
2. DELAY TIME FOR REFERENCE ONLY.



REFERENCE DRAWINGS			CONTROL DATA		NORMANDEALE DIVISION		TITLE		
COMP ASSY : 54254900			BR3B8				SCHEMATIC DIAGRAM		
			DWN		ENG		INDEX / SECTOR		
			CHK		APP		TYPE 3JNV		
COMPONENTS, EXCEPT AS NOTED			MTG		APP		DRAWING NUMBER		CD
RES	±5%	OHMS	1/4 W			19333 C		54255000	9
CAP	-30%								

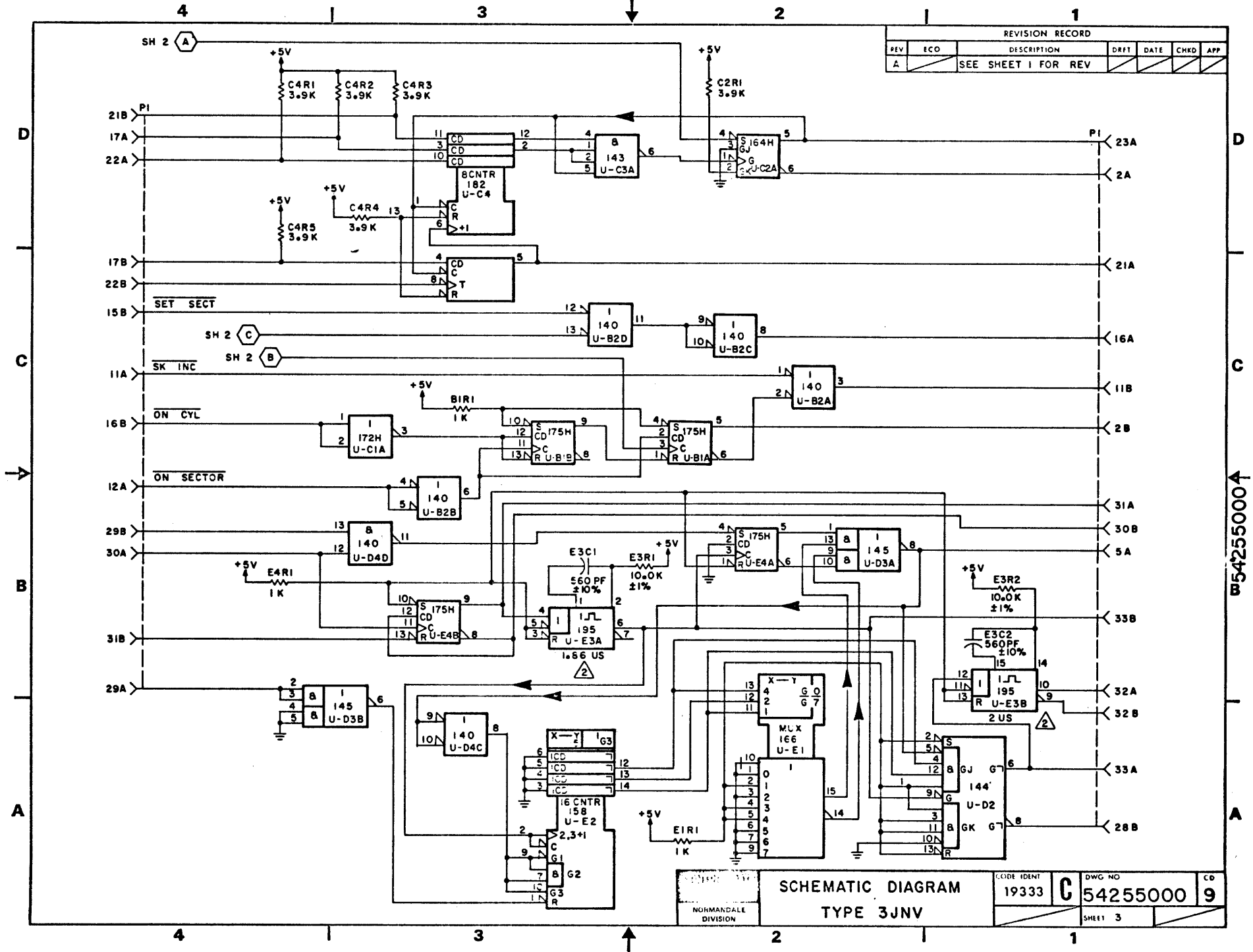
SHEET 1 OF 3
APD-E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRIT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



NORMANVILLE DIVISION	SCHEMATIC DIAGRAM TYPE 3JNV		CODE IDENT 19333	DWG NO 54255000	CD 9
			SHEET 2		

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

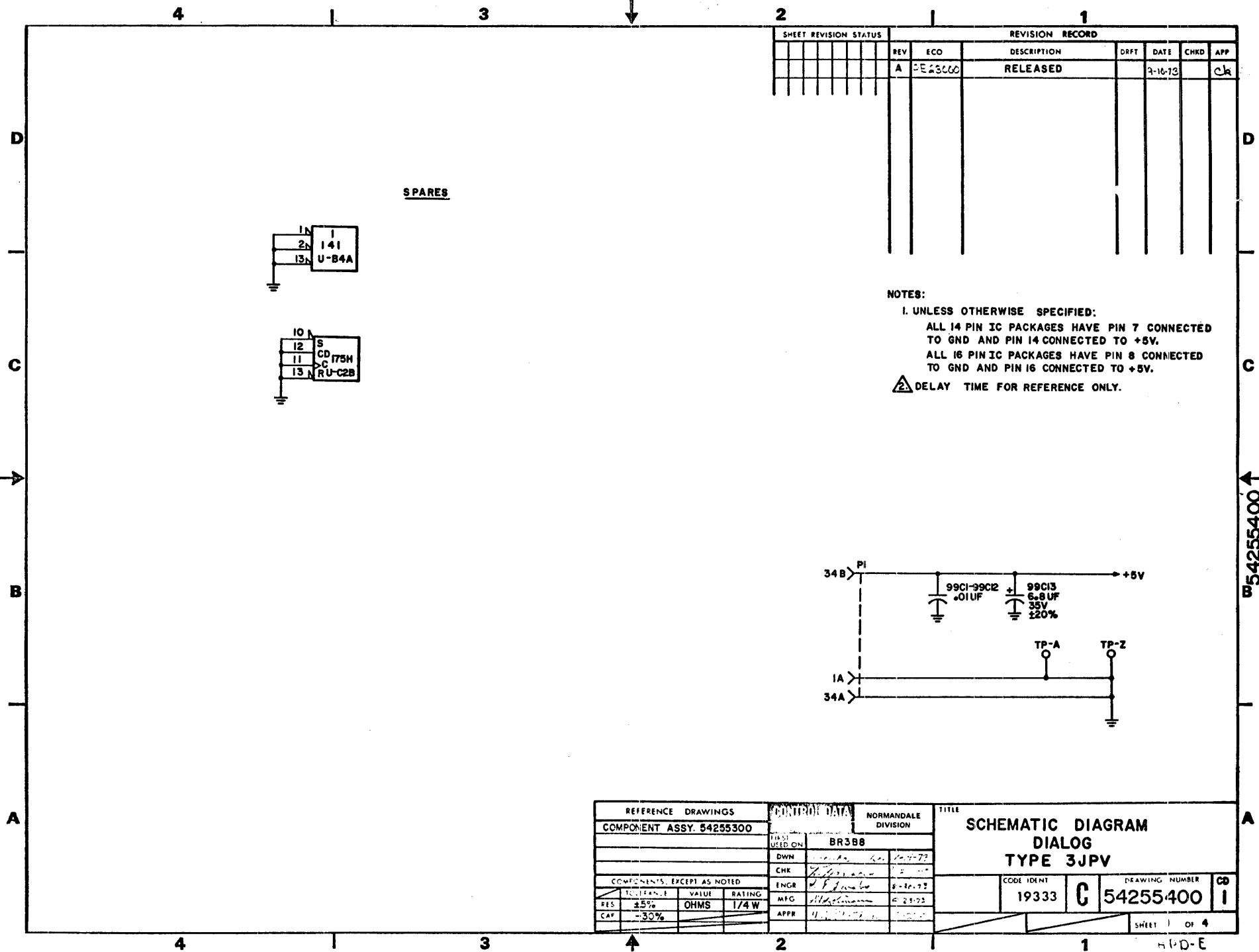


NORMANDE DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
	TYPE 3JNV		19333	C 54255000	9
			SHEET 3		

54255000

70629100 E

4-175



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	DE 23000	RELEASED		2-16-73		Clk	

NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 ALL 16 PIN IC PACKAGES HAVE PIN 8 CONNECTED TO GND AND PIN 16 CONNECTED TO +5V.
 ⚠ DELAY TIME FOR REFERENCE ONLY.

REFERENCE DRAWINGS		NORMANDEALE DIVISION		TITLE	
COMPONENT ASSY. 54255300		BR388		SCHEMATIC DIAGRAM DIALOG TYPE 3JPV	
COMPONENTS, EXCEPT AS NOTED		MFG		CODE IDENT	DRAWING NUMBER
RES	±5%	OHMS	1/4 W	19333	54255400
CAP	-30%			C	CD I
				SHEET	OF 4

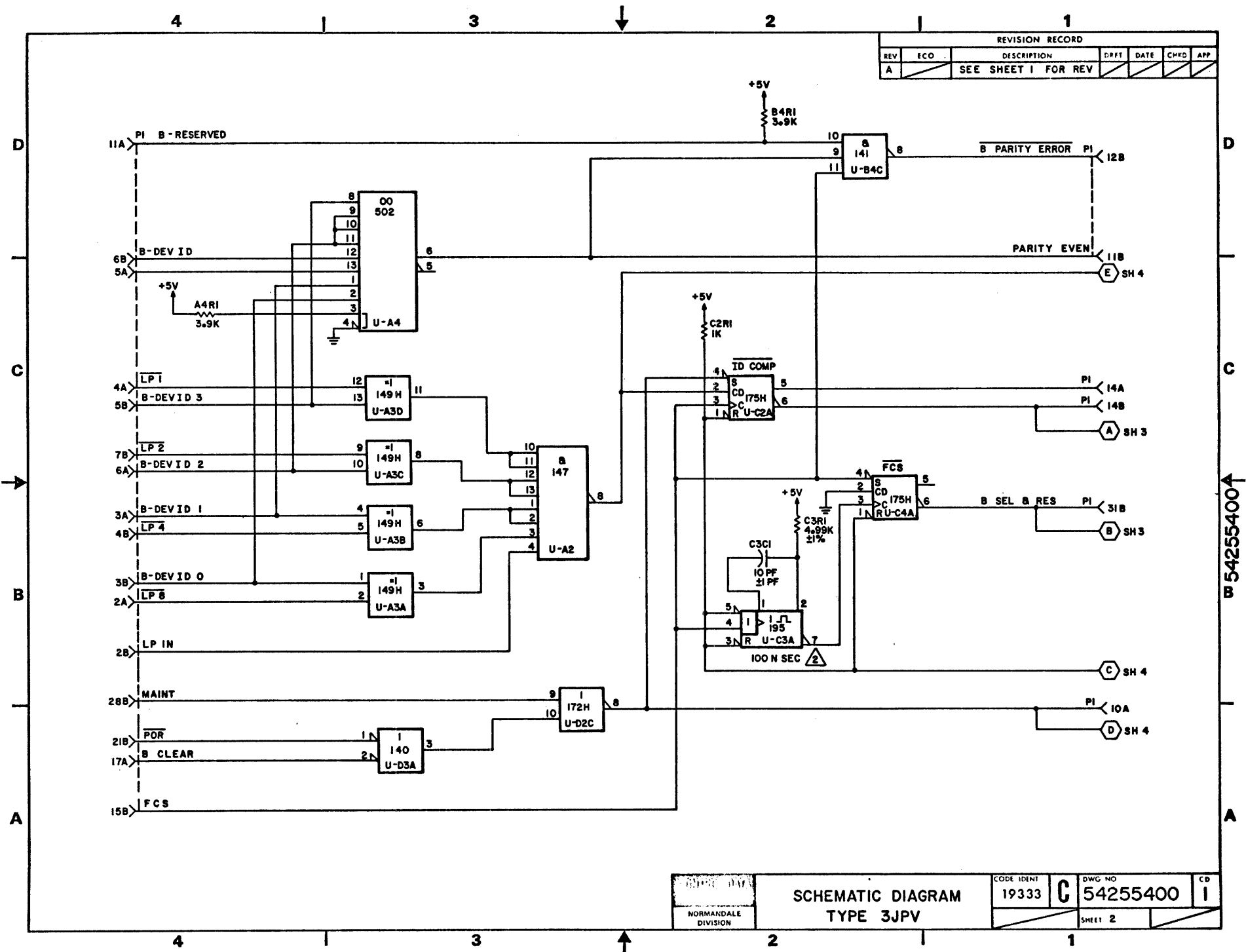
54255400 ↑

HPD-E

4-176

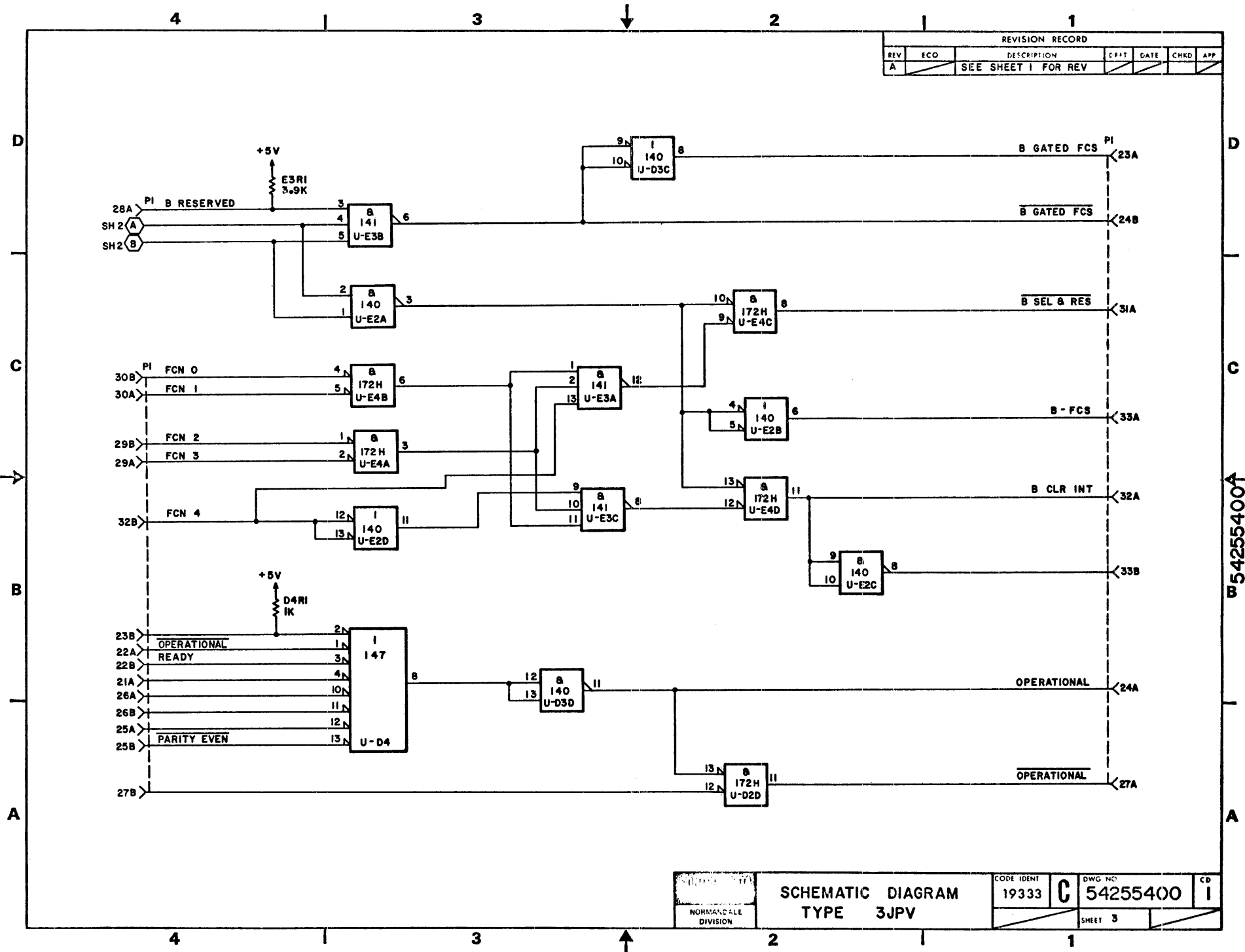
70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DFPT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JPV		CODE IDENT 19333	C	DWG NO 54255400	CD 1
					SHEET 2	

REVISION RECORD						
REV	ECO	DESCRIPTION	CPMT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

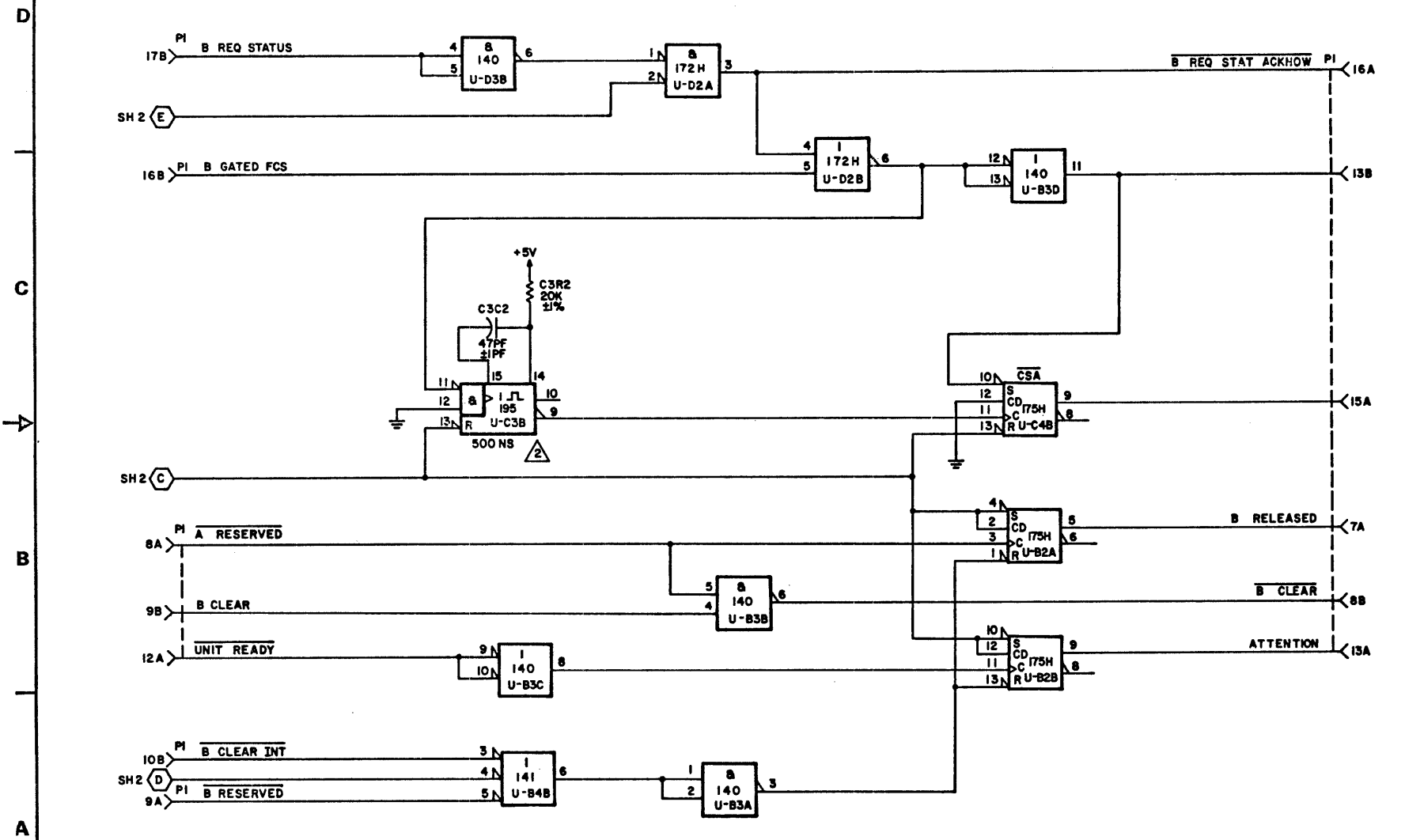


NORMANDELL DIVISION	SCHEMATIC DIAGRAM TYPE 3JPV	CODE IDENT	DWG NO	CD
		19333	C 54255400	1
		SHEET 3		

4-178

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHEET 1 FOR REV				



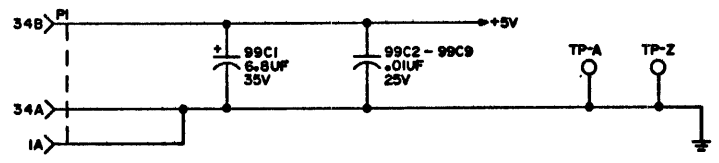
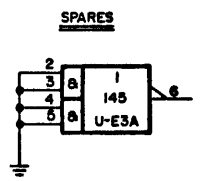
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JPV		CODE IDENT 19333	DWG NO 54255400	CD 1
				SHEET 4 OF 4	

54255400

70629100 E

SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	FE13200	RELEASED		11-1-73		ck			

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V.



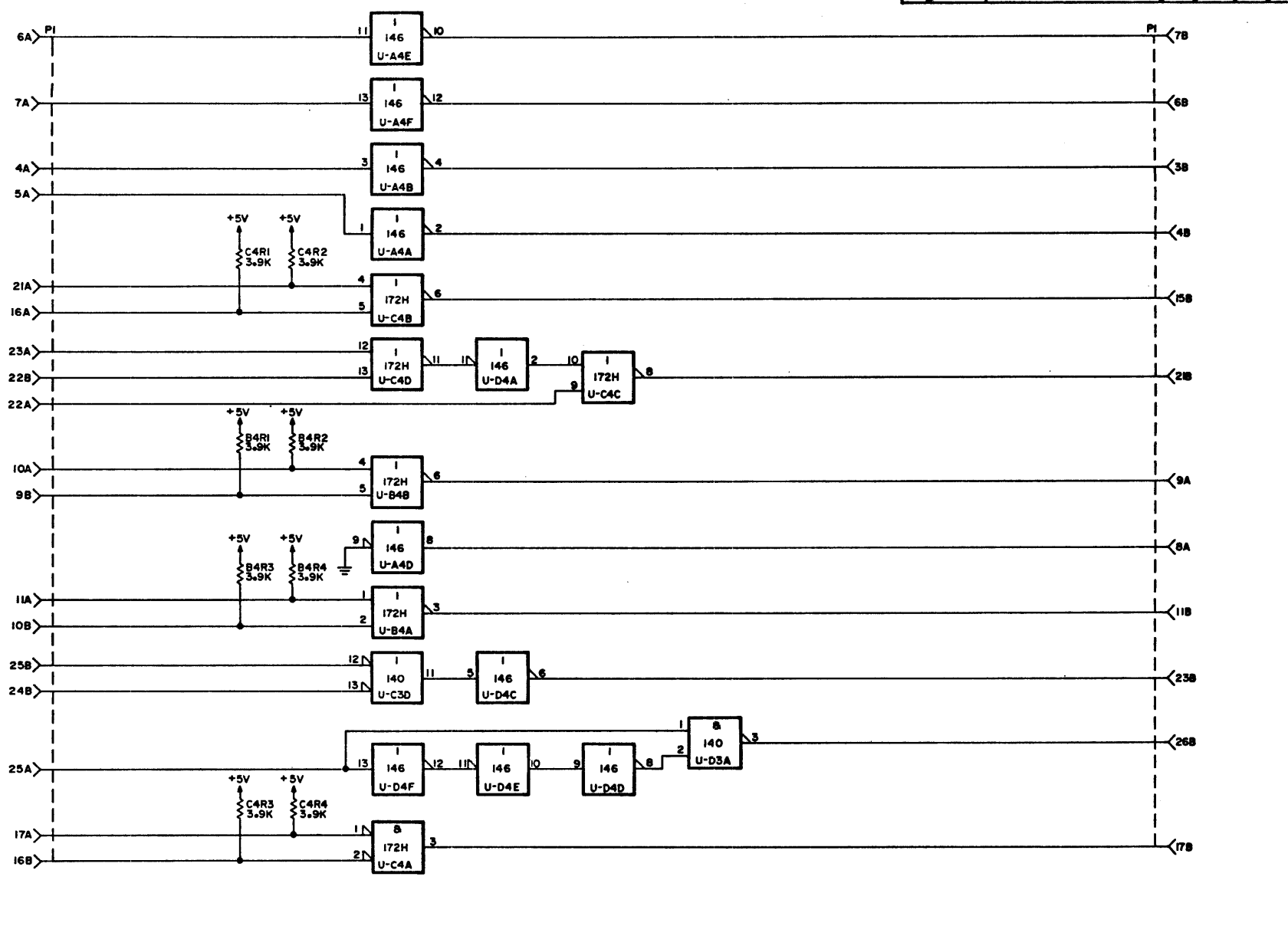
REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54255700			FIRST USED ON		BR3BB		SCHEMATIC DIAGRAM	
			DWN		MON BAKER		8-8-73	
			CHR		J. P. Baker		7-16-73	
			ENGR		R. F. Baker		8-28-73	
			MFG		M. L. Baker		9-24-73	
			APPR					
COMPONENTS EXCEPT AS NOTED			TOLERANCE		VALUE		RATING	
			RES		±5%		OHMS 1/4 W	
			CAP		-30%			
			CODE IDENT		19333		DRAWING NUMBER	
					C		54255800	
							SHEET 1 OF 3	

4-179

54255800

HPD-E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				



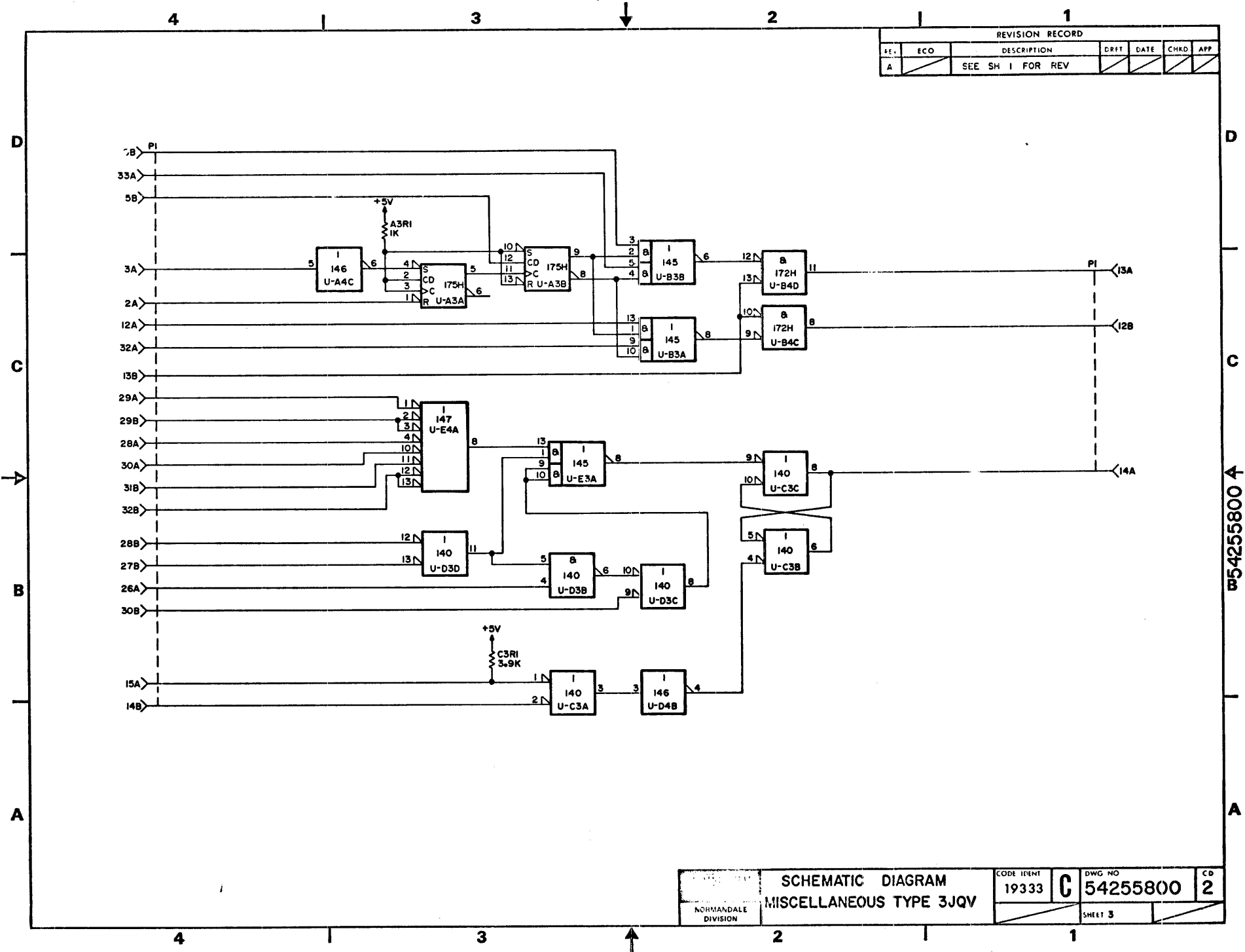
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	C	DWG NO	2
	MISCELLANEOUS TYPE 3JQV		19333		54255800	
			SHEET 2			

54255800

70629100 E

4-181

REVISION RECORD						
REV.	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SH 1 FOR REV				



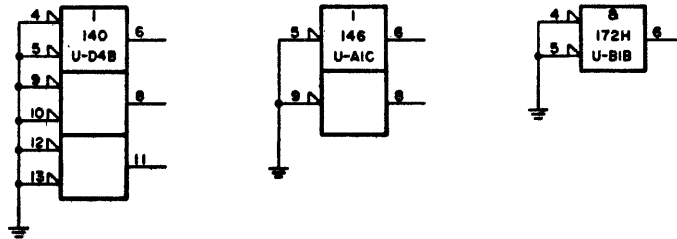
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
	MISCELLANEOUS TYPE 3JQV		19333	C 54255800	2
			SHEET 3		

4-182

70629100 E

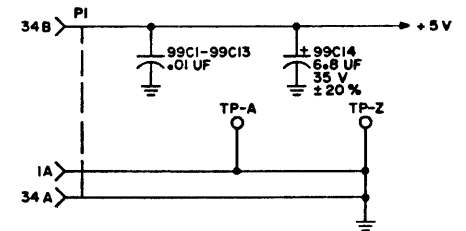
SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	1	RELEASED		1-1-73			

SPARE GATES



NOTE:

- UNLESS OTHERWISE SPECIFIED:
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
AND PIN 14 CONNECTED TO +5V.
- △ DELAY TIME FOR REF ONLY.



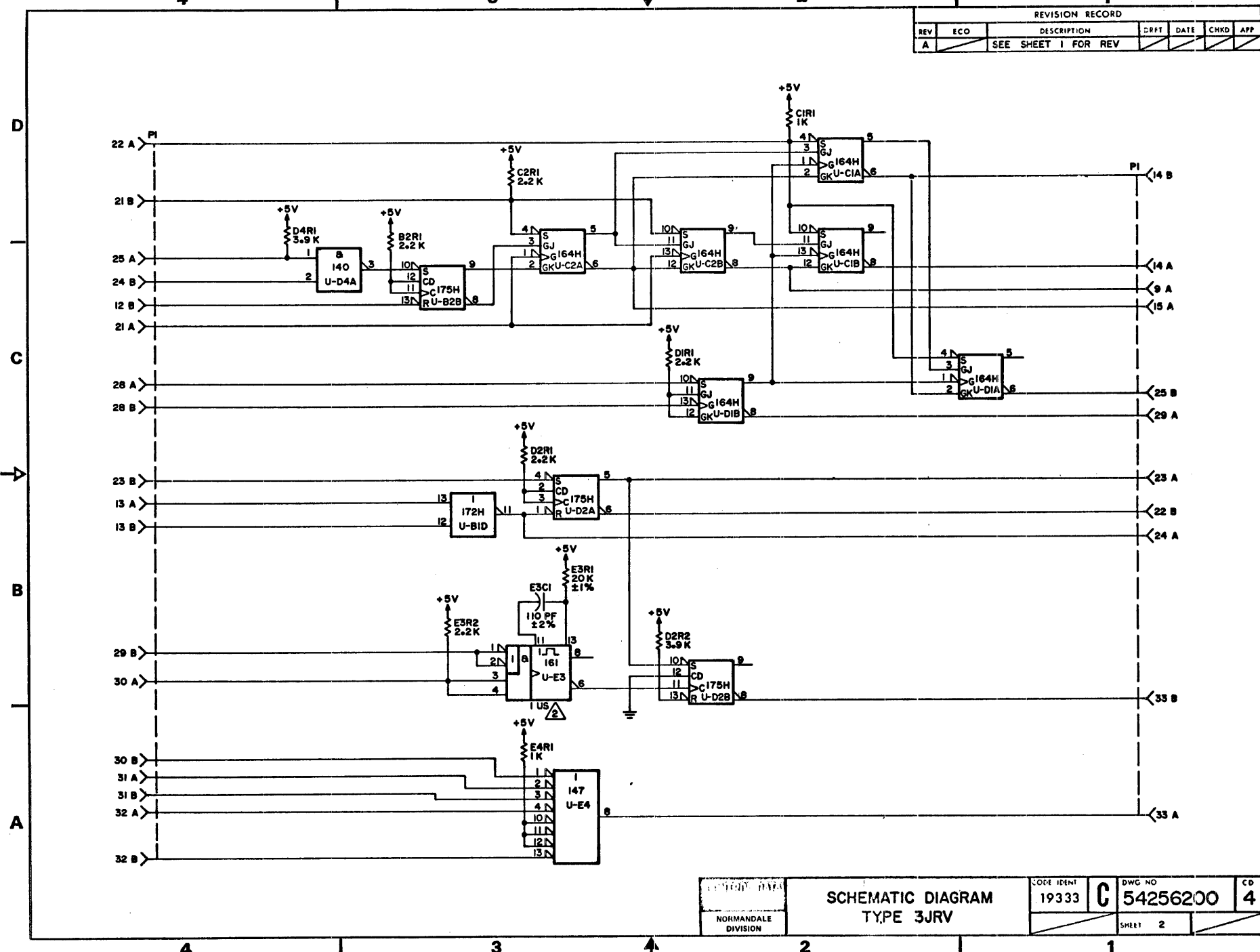
REFERENCE DRAWINGS			CONTROL DATA		NORMANDEALE DIVISION		TITLE		
COMP ASSY 54256100			BR3B8				SCHEMATIC DIAGRAM SERIALIZER / DESERIALIZER TYPE 3JR V		
COMPONENTS, EXCEPT AS NOTED			ENGR	8-17-73			CODE IDENT	DRAWING NUMBER	CD
TOLERANCE	VALUE	RATING	MFG	8-17-73			19333	C 54256200	4
RES	± 5 %	OHMS	1/4 W				SHEET 1 OF 3		
CAP	-30 %						HFD-E		

54256200

70629100 E

4-183

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



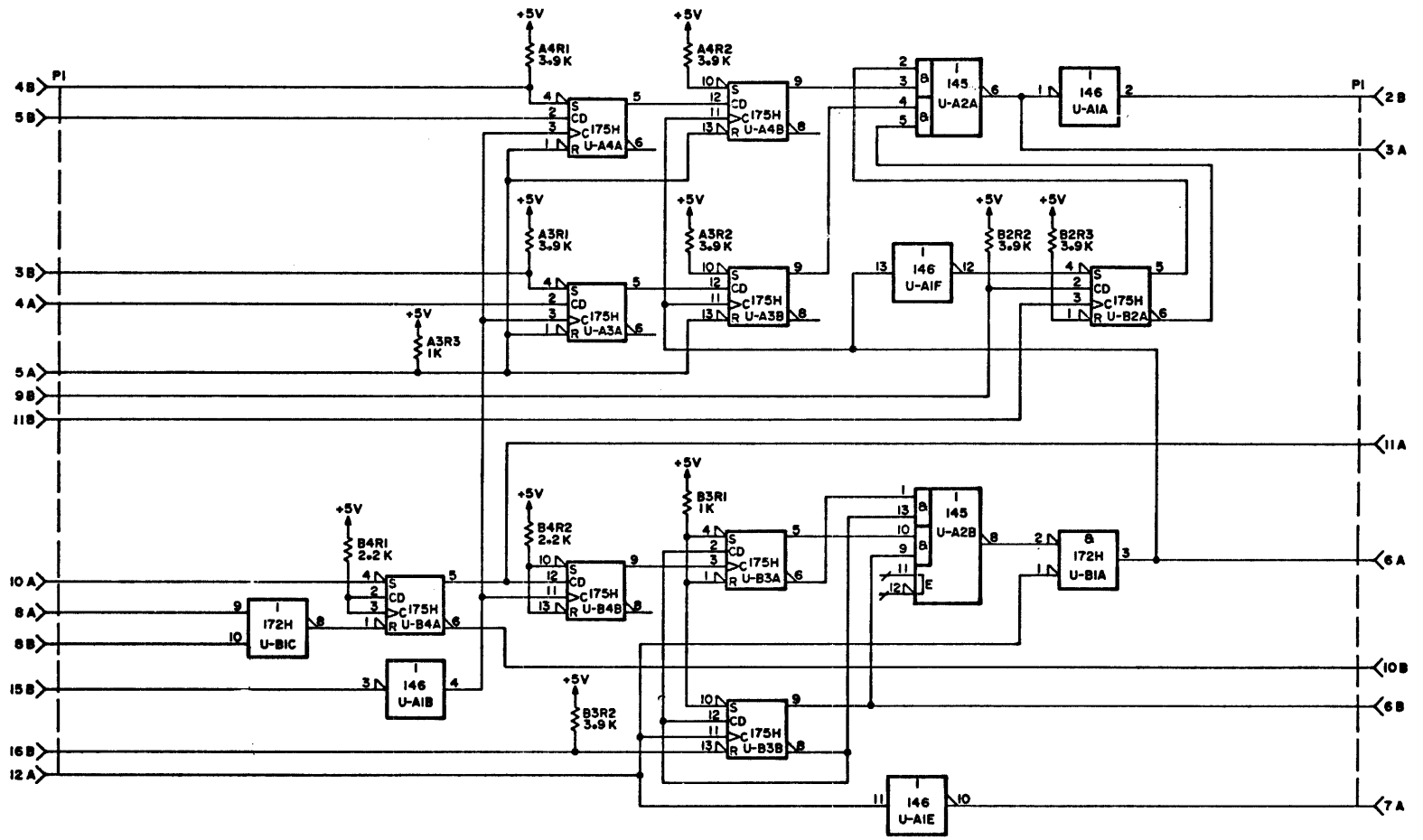
NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JRV		CODE IDENT 19333	DWG NO 54256200	CD 4
			SHEET 2		

54256200

4-184

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

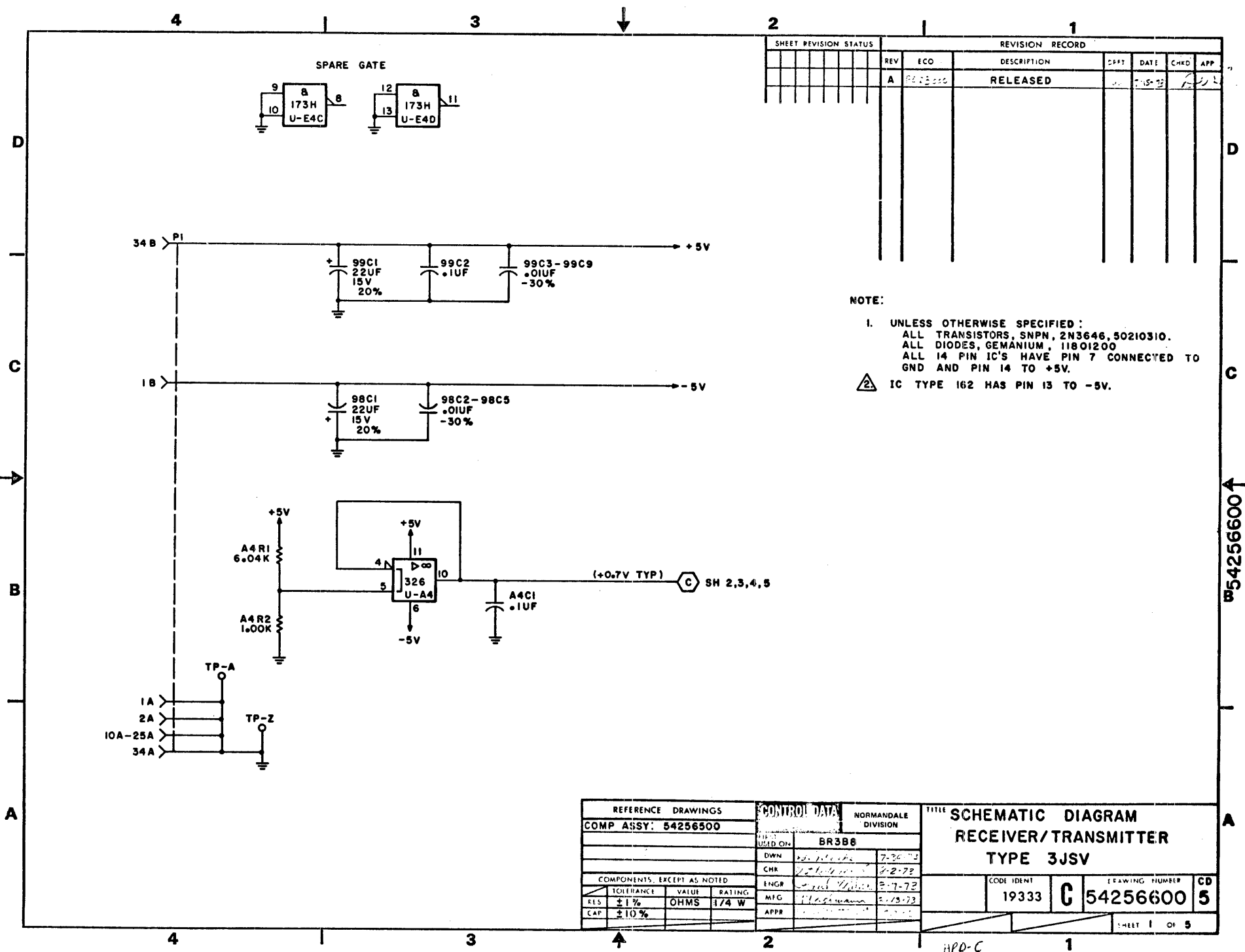


NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JRV		CODE IDENT 19333	C	DWG NO 54256200	CD 4
					SHEET 3	

B 54256200

70629100 E

4-185



SHEET REVISION STATUS			REVISION RECORD				
REV	ECO		DESCRIPTION	CHFT	DATE	CHKD	APP
A	REL	23-01-73	RELEASED		7-15-73		

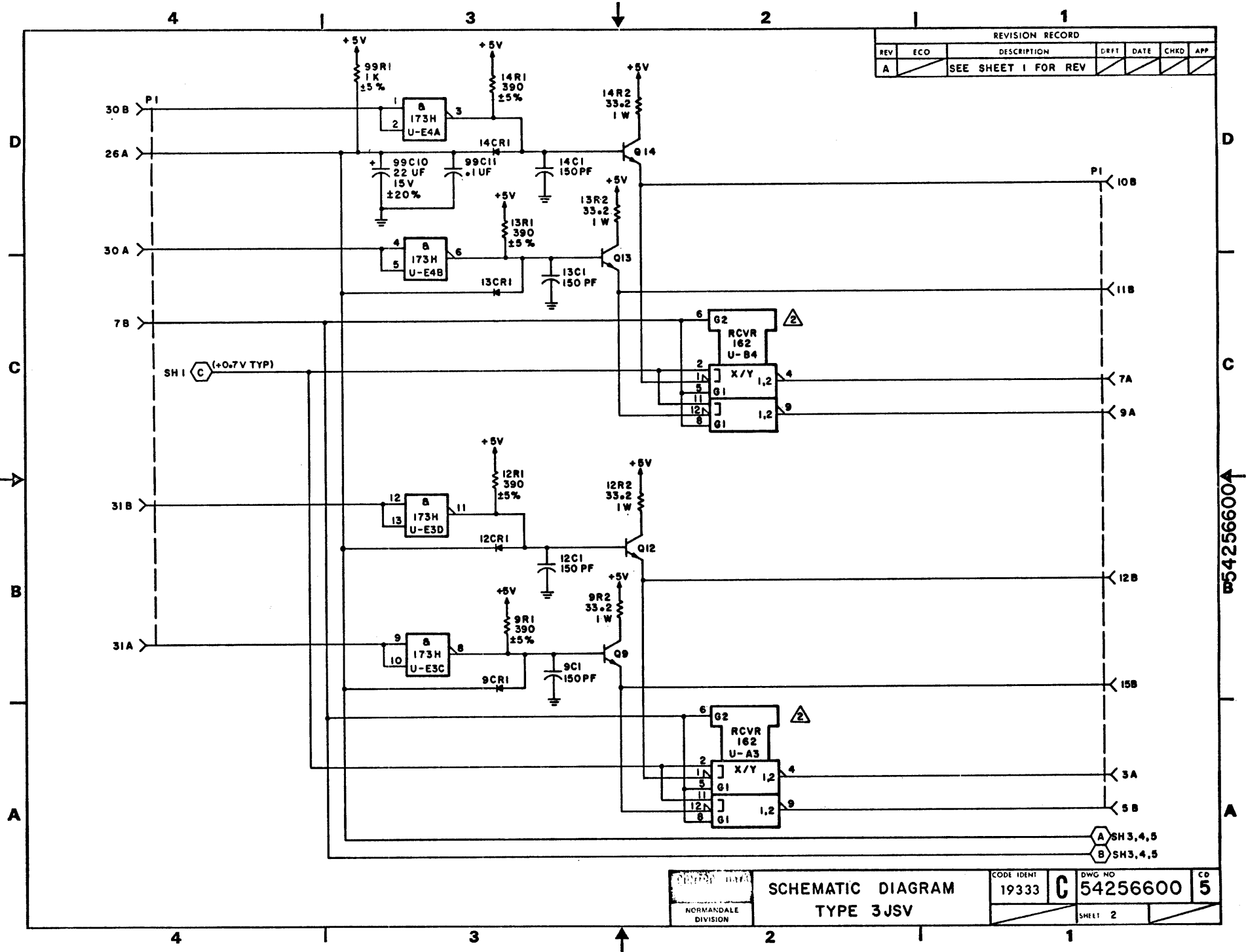
NOTE:
 1. UNLESS OTHERWISE SPECIFIED :
 ALL TRANSISTORS, SNPN, 2N3646, 50210310.
 ALL DIODES, GEMANIUM, 11801200
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND AND PIN 14 TO +5V.
 2. IC TYPE 162 HAS PIN 13 TO -5V.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54256500		BR3B8				SCHEMATIC DIAGRAM	
		DWN		7-20-73		RECEIVER/TRANSMITTER	
		CHK		2-2-72		TYPE 3JSV	
		ENGR		2-7-72		CODE IDENT	
		MFG		2-23-73		DRAWING NUMBER	
		APPR				CD	
COMPONENTS, EXCEPT AS NOTED				19333		54256600	
FES	±1%	OHMS	1/4 W			SHEET 1 OF 5	
CAP	±10%						

54256600

HPD-C 1

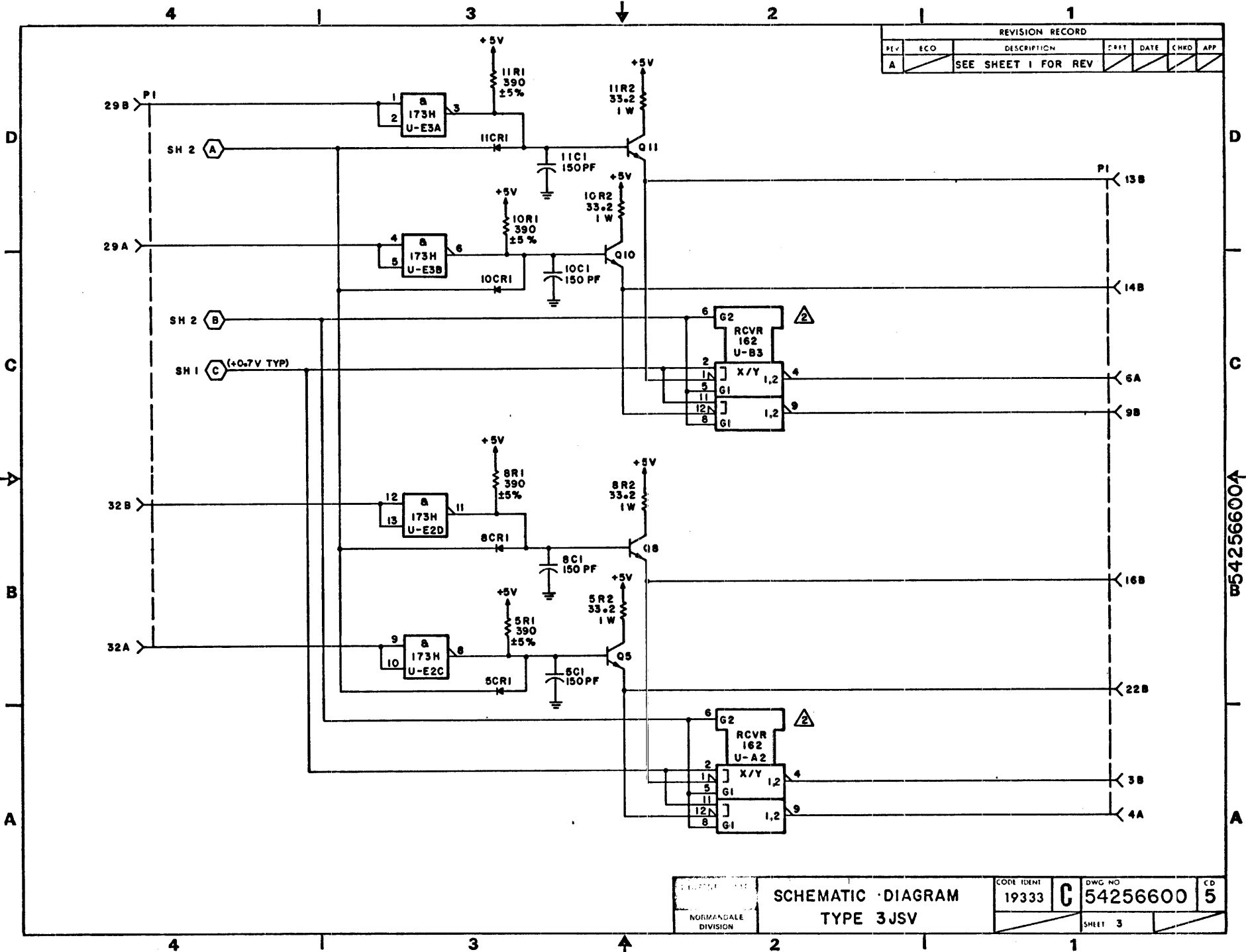
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 3JSV		CODE IDENT 19333	DWG NO C 54256600	CD 5
			SHEET 2		

54256600A

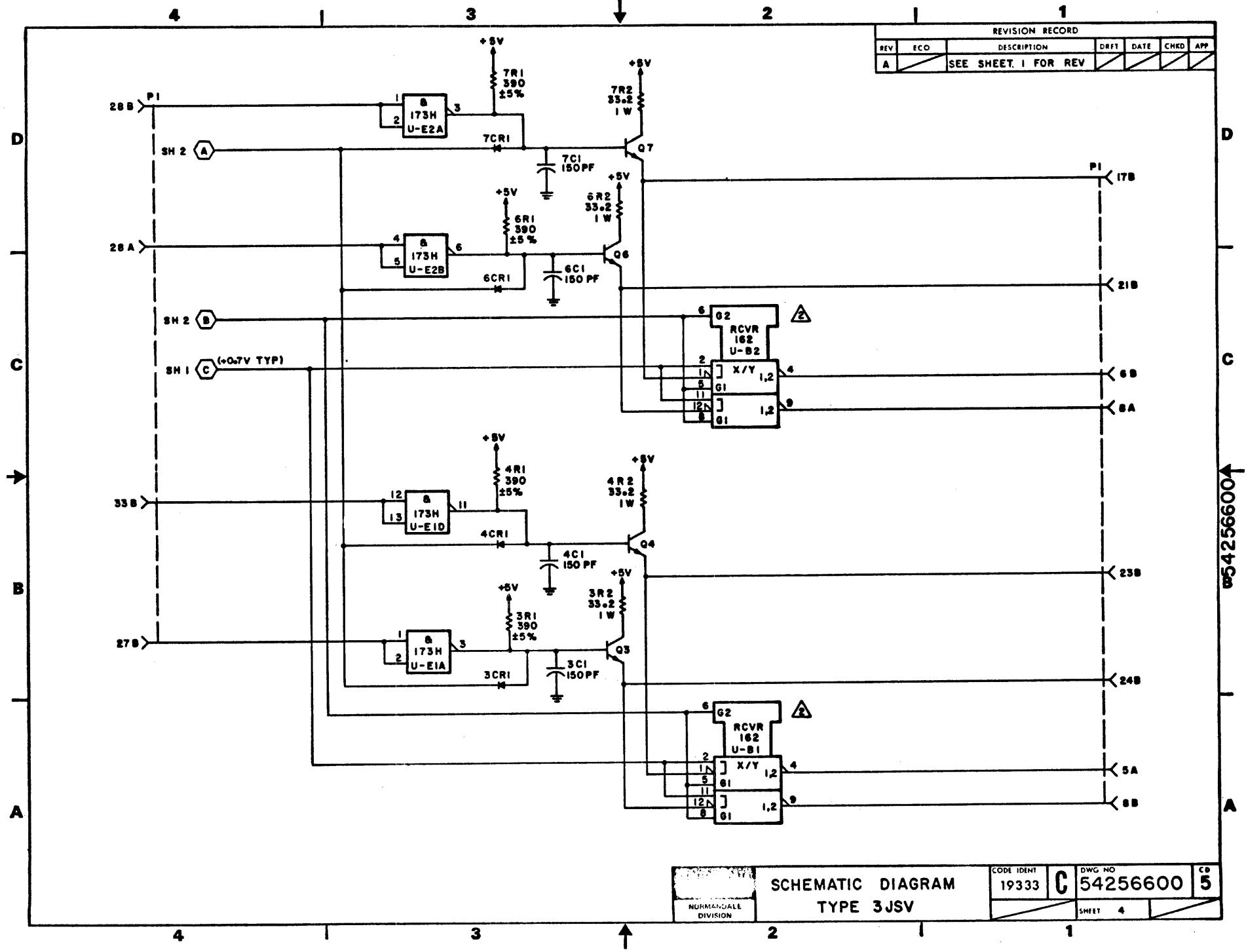
REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHEET 1 FOR REV				



NORMANDE DIVISION	SCHEMATIC DIAGRAM TYPE 3JSV		CODE IDENT 19333	DWG NO 54256600	CD 5
				SHEET 3	

W54256600A

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



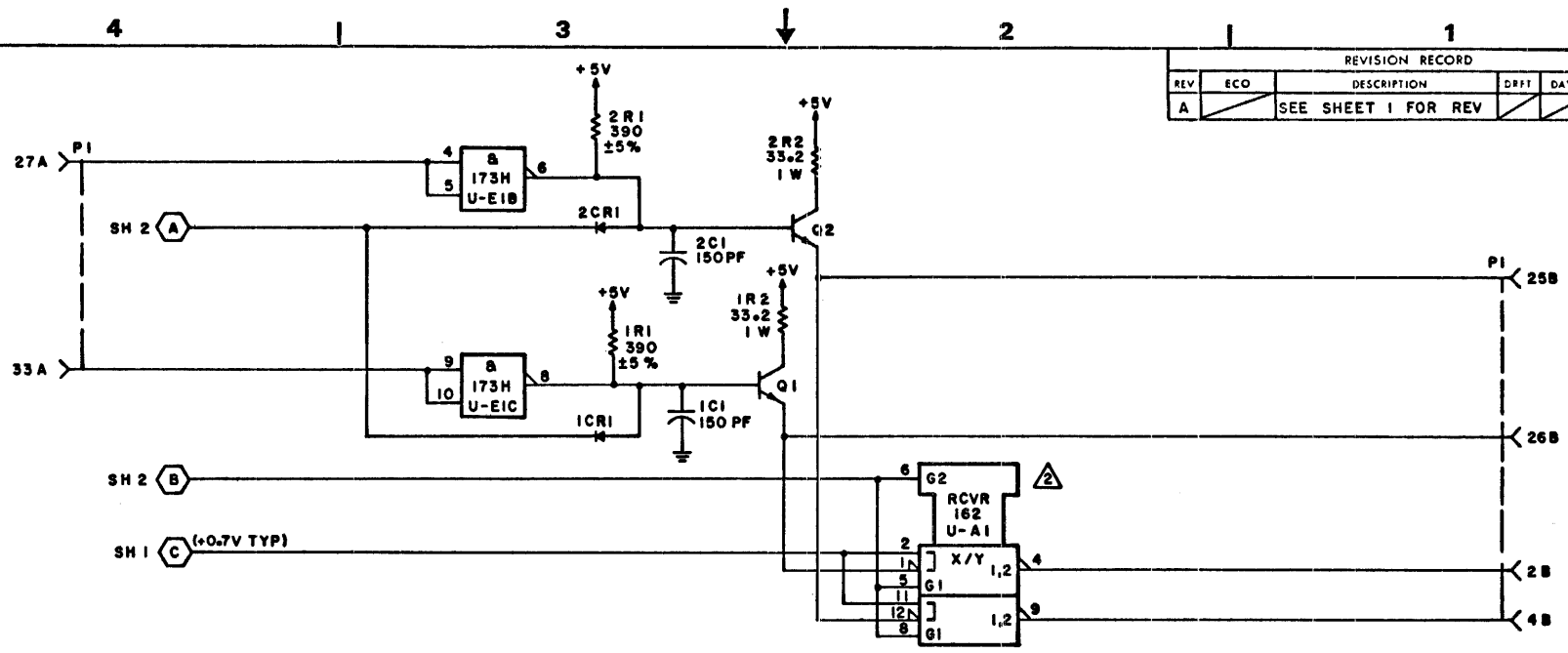
NORMAN-DALL DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
	TYPE 3JSV		19333	C 54256600	5
			SHEET	4	

54256600

70629100 F

4-189

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



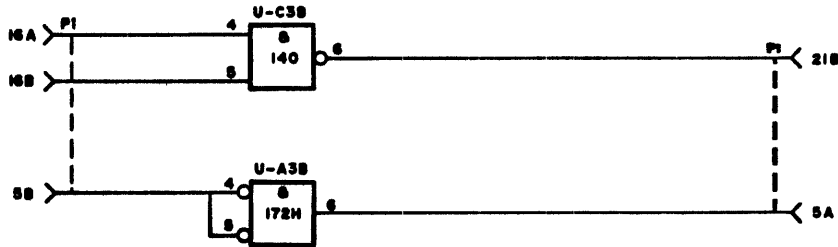
NON-MANDALÉ DIVISION	SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
	TYPE 3JSV		19333	54256600	5
			SHEET 5		

542566004

4-190

70629100 E

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23030	RELEASED					



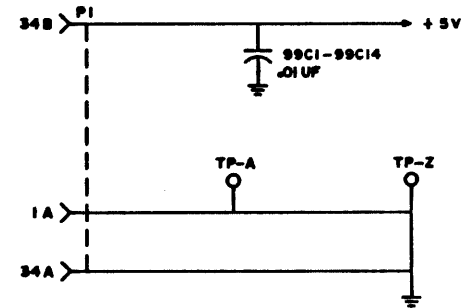
NOTES:

1. UNLESS OTHERWISE SPECIFIED;

ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.

ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.

2. IC'S U-C1, U-D1 AND U-E1 HAVE PIN 5 CONNECTED TO +5V AND PIN 12 CONNECTED TO GROUND.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE		
COMPONENT ASSY 54258900		CORPORATION		DIVISION		SCHEMATIC DIAGRAM DIFFERENCE ADDER TYPE 2JYV		
COMPONENTS EXCEPT AS NOTED		FIRST USED ON	8R3A8B		CODE IDENT	DRAWING NUMBER	CD	
TO TOLERANCE	VALUE	RATING	DWN	R. KONECNY	9-22-72	19333	C 54259000	5
RES	+5%	OHMS	1/4W	CHK	J. Konecny	12-6-72		
CAP	-35%			ENGR	J. Konecny	10/10/72		
				MFG	J. Konecny	10-12-72		
				APPR	J. Konecny	10-12-72		

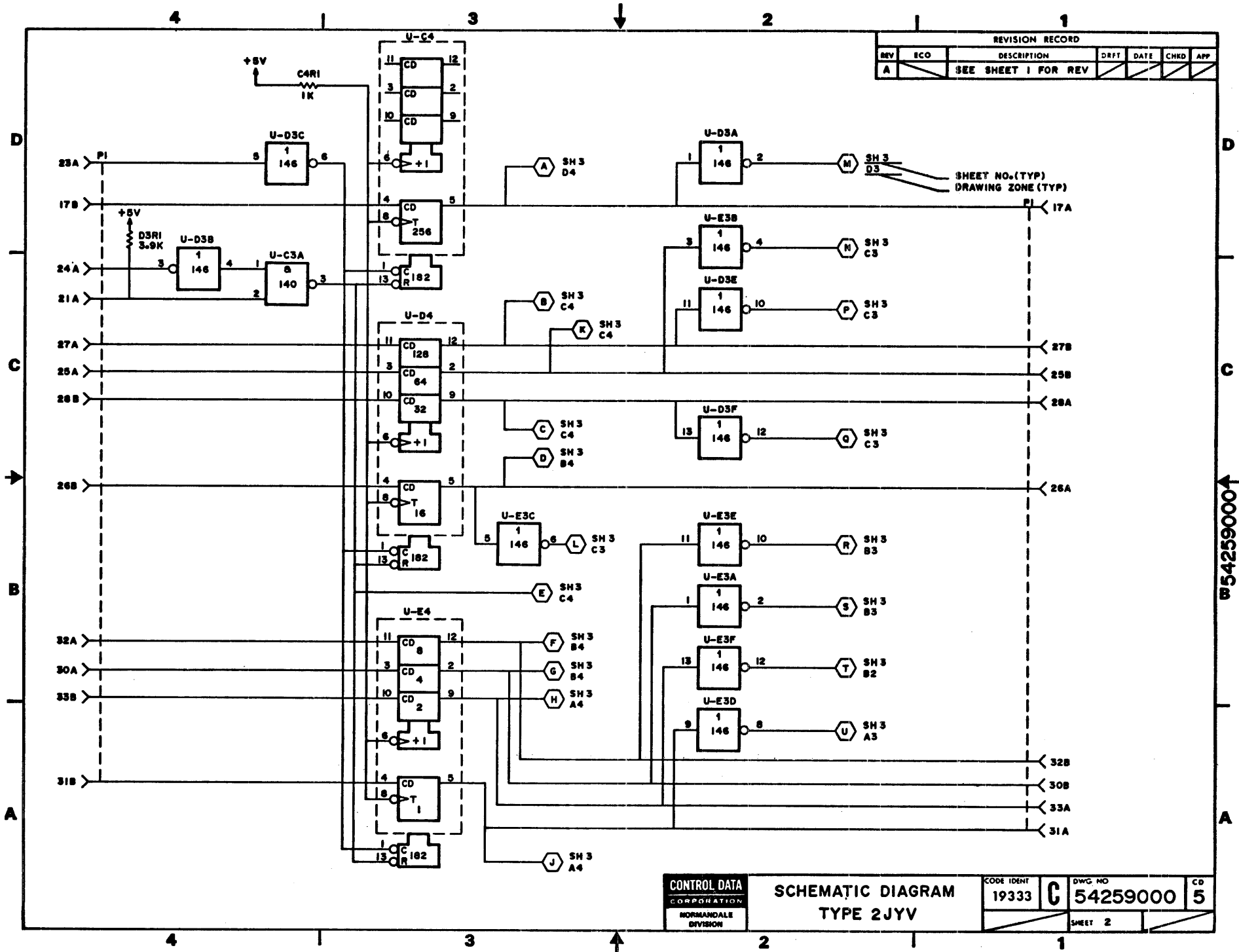
HPO

1

SHEET 1 OF 4

54259000

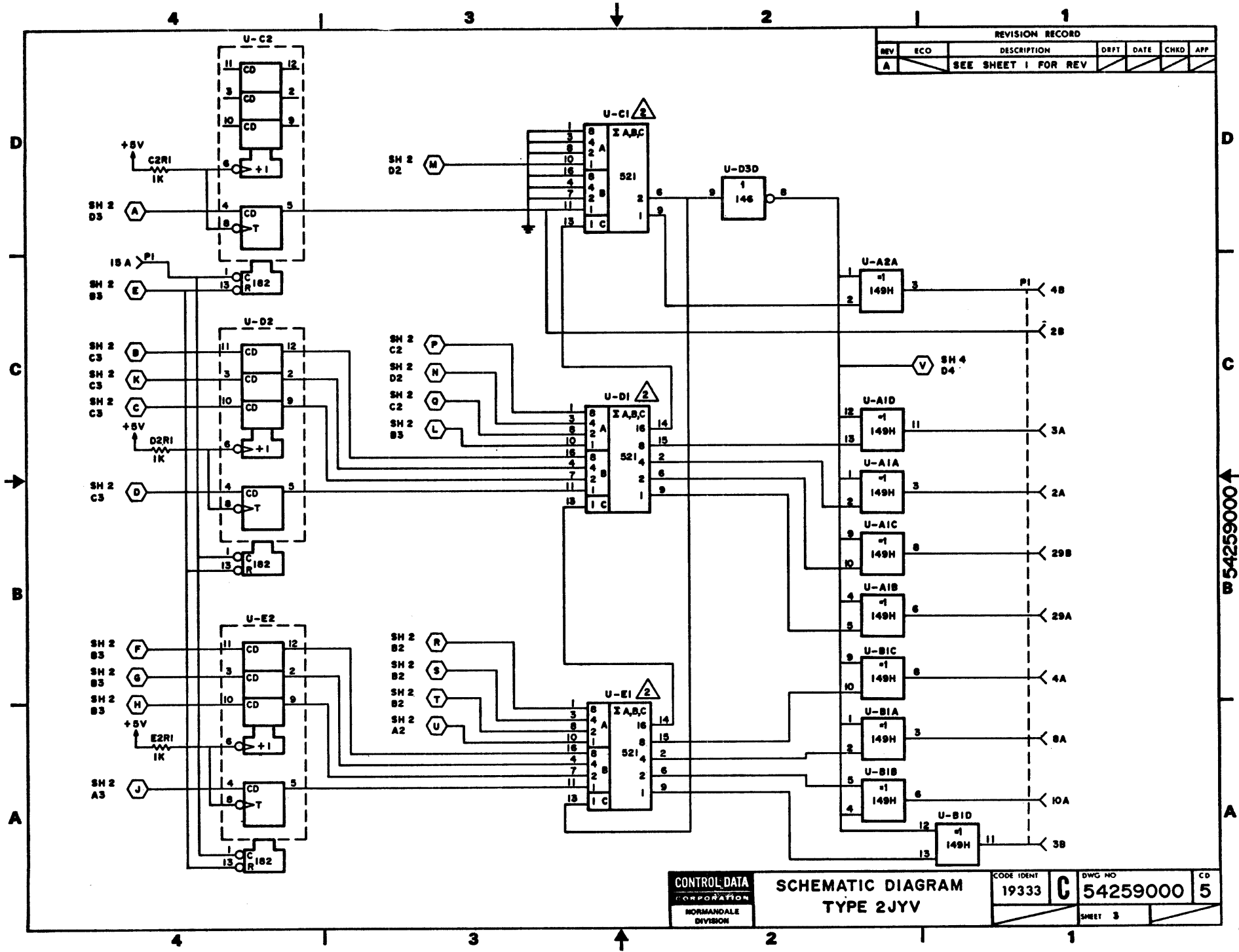
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA CORPORATION NORMANDALE DIVISION	SCHEMATIC DIAGRAM TYPE 2JYV		CODE IDENT 19333	DWG NO 54259000	CD 5
			SHEET 2		

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



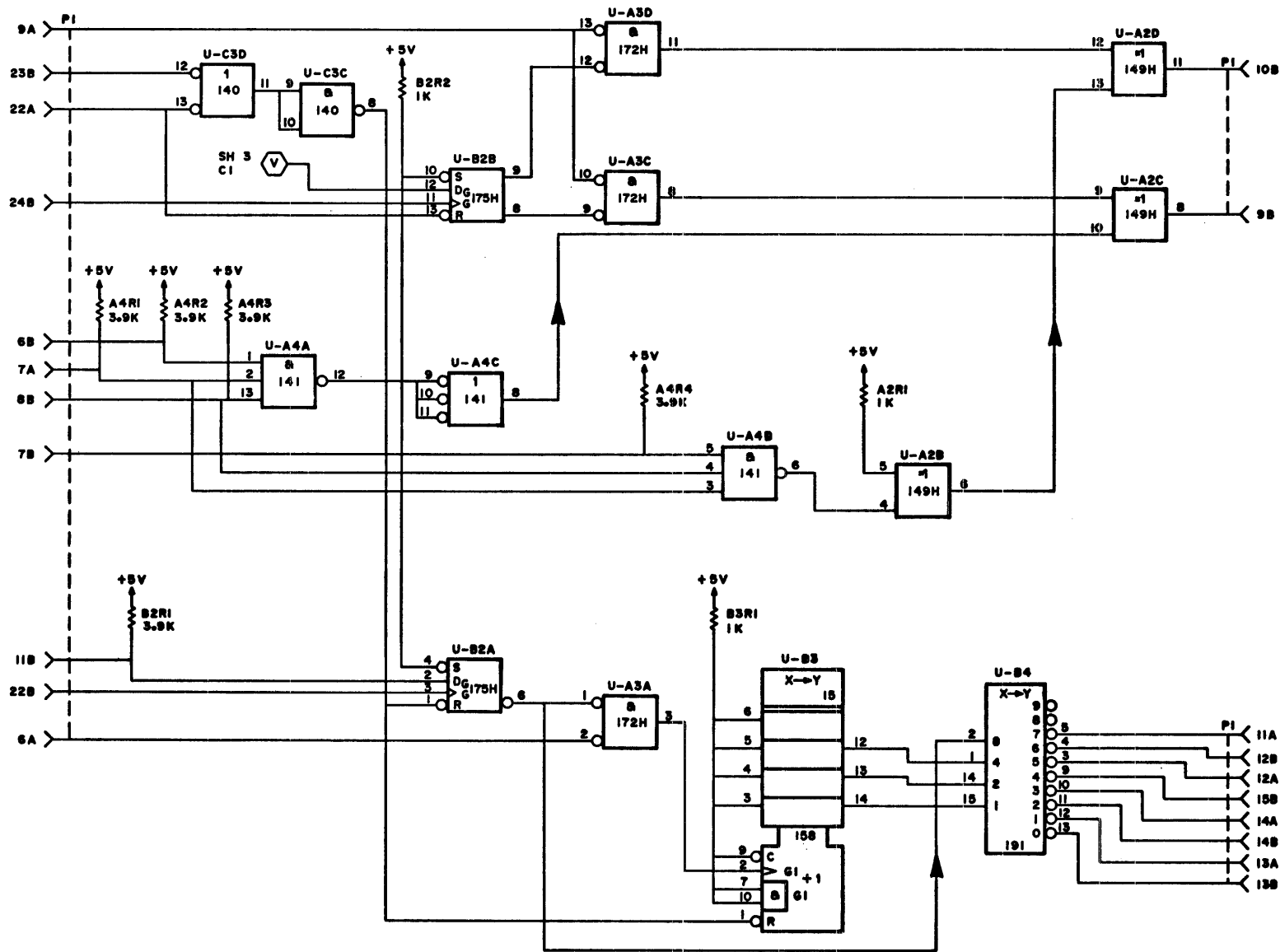
CONTROL DATA CORPORATION NORMANVILLE DIVISION	SCHEMATIC DIAGRAM TYPE 2JYV		CODE IDENT 19333	DWG NO 54259000	CD 5
				SHEET 3	

W 542590004

70629100 E

4-193

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA
 330
 NORMANDE
 DIVISION

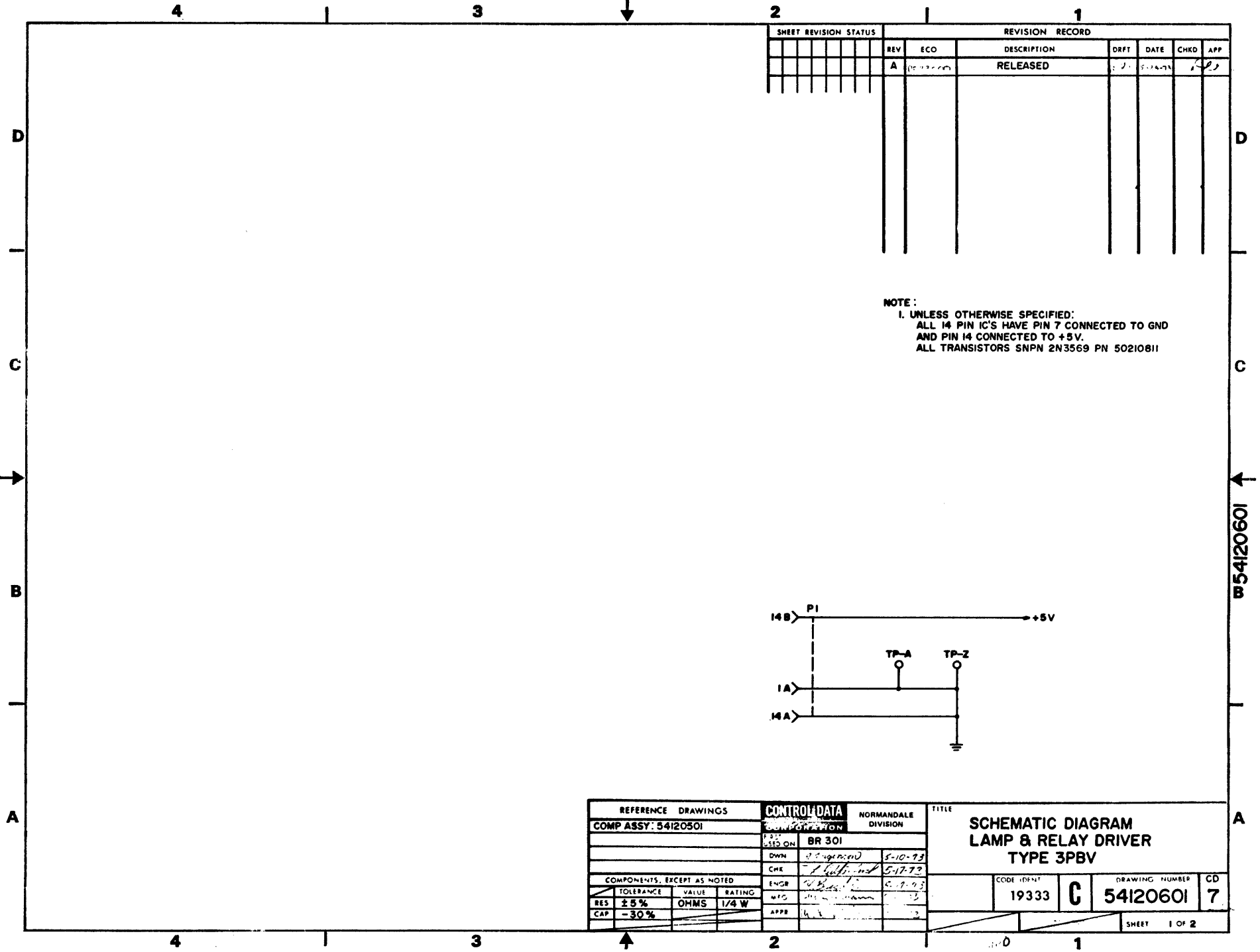
SCHMATIC DIAGRAM
 TYPE 2JYV

CODE IDENT 19333	DWG NO C 54259000	CD 5
SHEET 4		

W542590004

4-194

70629100 F



NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND
 AND PIN 14 CONNECTED TO +5V.
 ALL TRANSISTORS SNPN 2N3569 PN 50210811

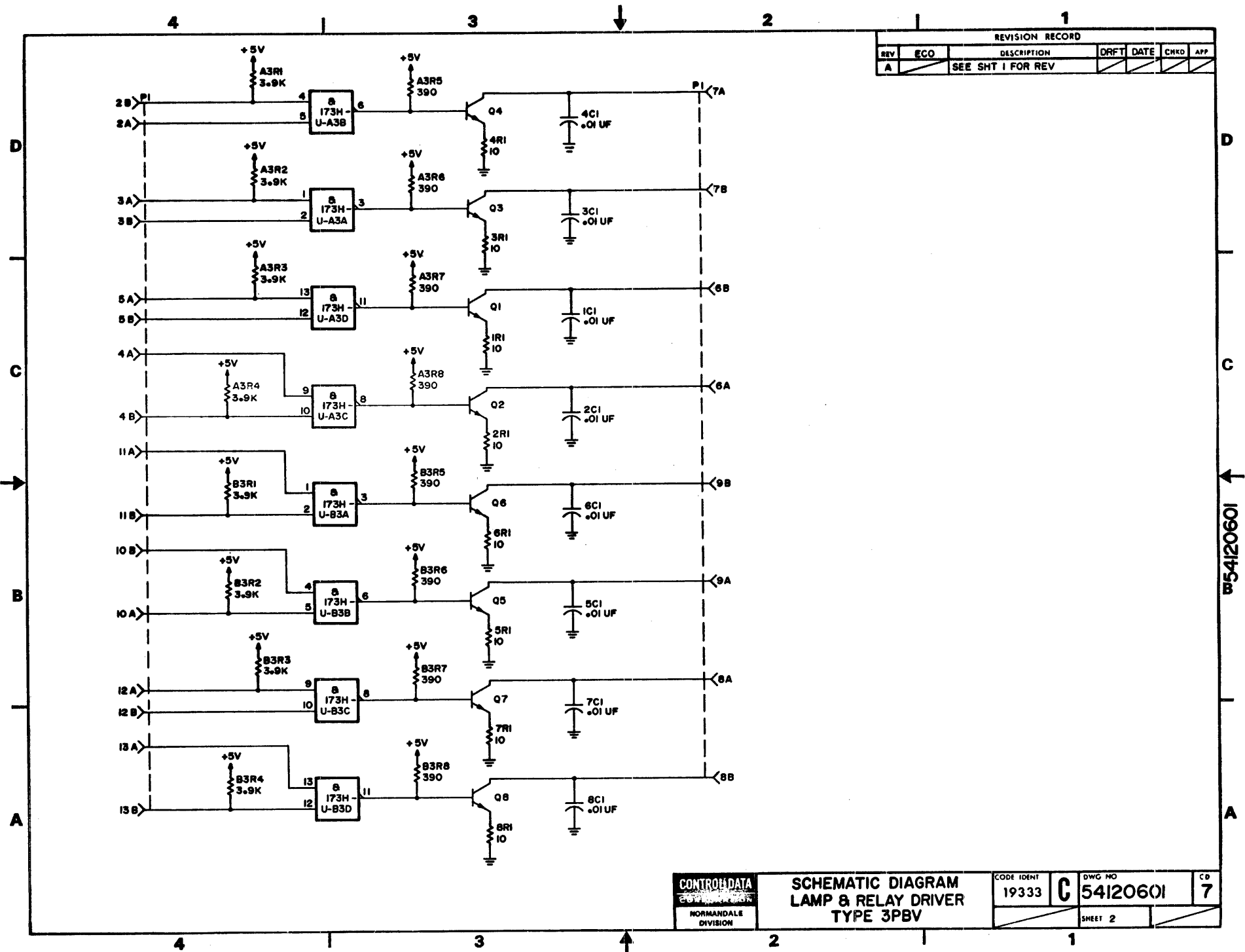
SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A		RELEASED		5-10-73					

REFERENCE DRAWINGS			CONTROL DATA		NORMANDELE DIVISION		TITLE		
COMP ASSY: 54120501			BR 301				SCHEMATIC DIAGRAM LAMP & RELAY DRIVER TYPE 3PBV		
COMPONENTS, EXCEPT AS NOTED			USED ON	DATE			CODE IDENT	DRAWING NUMBER	CD
RES	± 5 %	OHMS 1/4 W	CHKD	5-10-73			19333	C 54120601	7
CAP	- 30 %		ENGR	5-17-73					
			WFO						
			APPR						
							SHEET 1 OF 2		

70629100 F

4-195

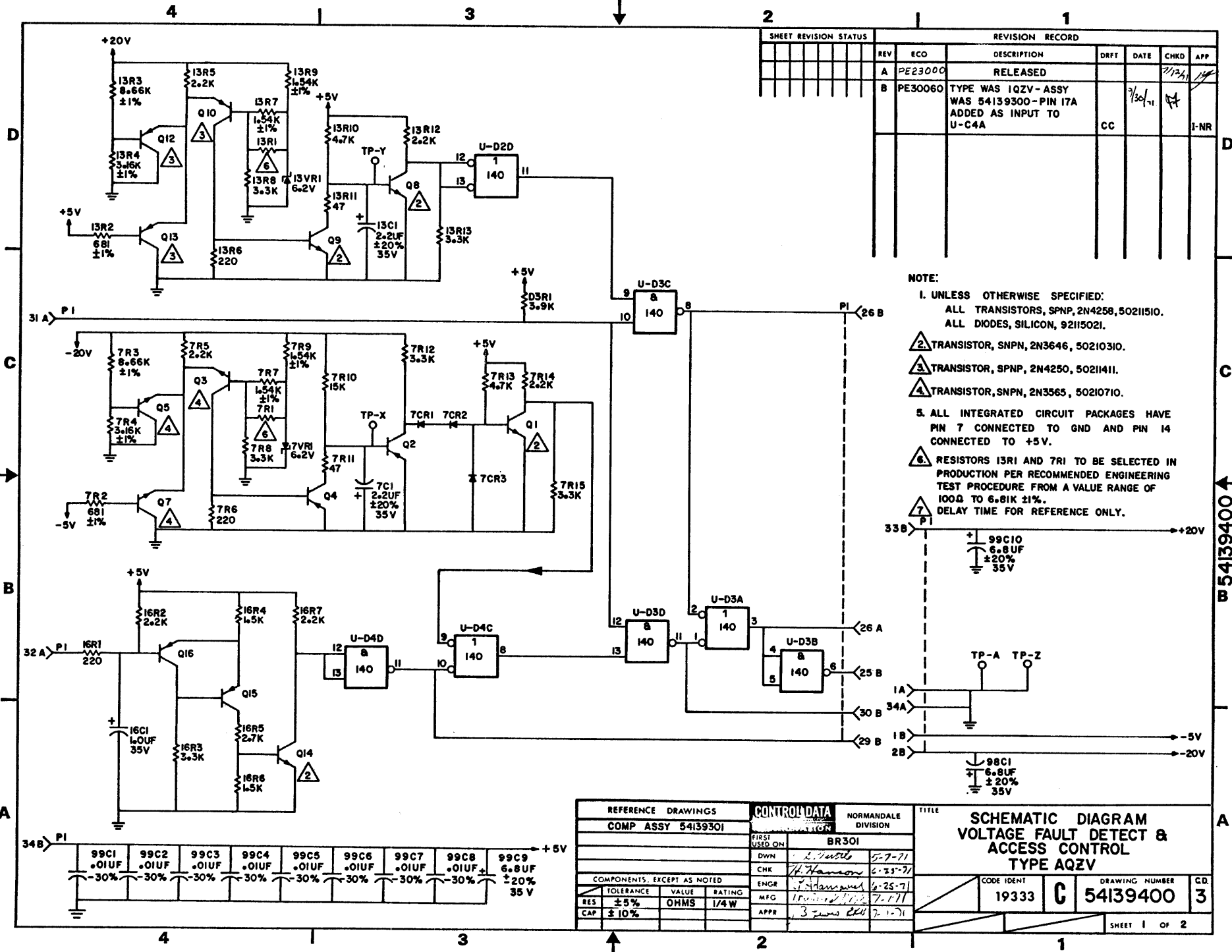
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHT 1 FOR REV				



CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
LAMP & RELAY DRIVER
TYPE 3PBV

CODE IDENT	19333	DWG NO	54120601	CD	7
			SHEET 2		



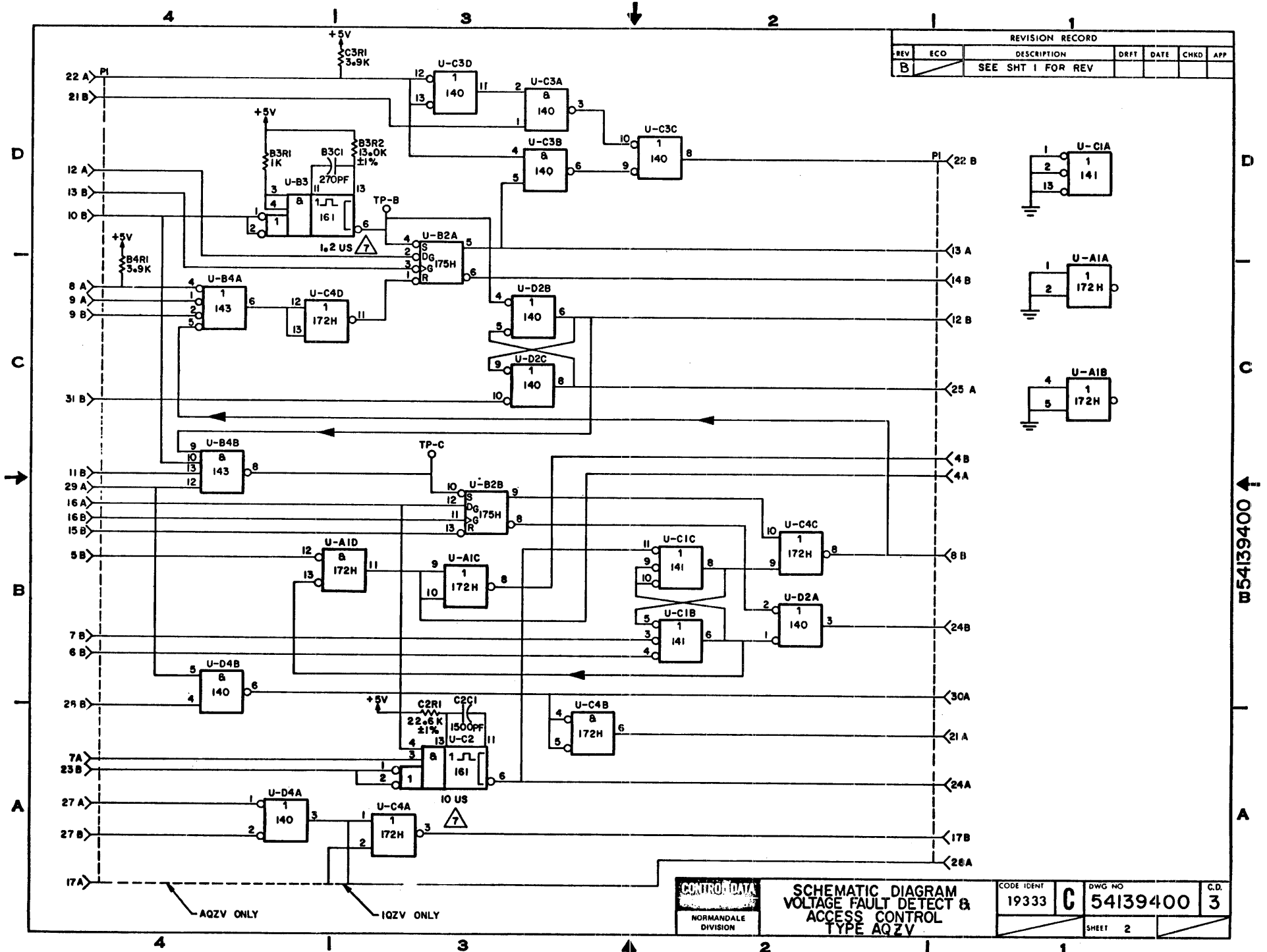
SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE23000	RELEASED			7/13/71	
B	PE30060	TYPE WAS 1QZV - ASSY WAS 54139300 - PIN 17A ADDED AS INPUT TO U-C4A	CC		7/30/71	

- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SPNP, 2N4258, 50211510.
ALL DIODES, SILICON, 92115021.
 - TRANSISTOR, SPNP, 2N3646, 50210310.
 - TRANSISTOR, SPNP, 2N4250, 50211411.
 - TRANSISTOR, SPNP, 2N3655, 50210710.
 - ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 - RESISTORS 13R1 AND 7R1 TO BE SELECTED IN PRODUCTION PER RECOMMENDED ENGINEERING TEST PROCEDURE FROM A VALUE RANGE OF 100Ω TO 6.81K ±1%.
DELAY TIME FOR REFERENCE ONLY.

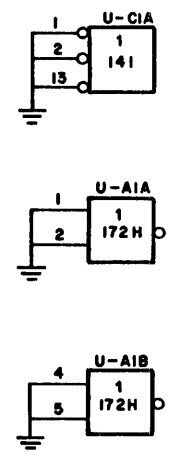
REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMP ASSY 54139301		BR301				SCHEMATIC DIAGRAM VOLTAGE FAULT DETECT & ACCESS CONTROL TYPE AQZV	
		FIRST USED ON					
		DWN		L. J. Wille		5-7-71	
		CHK		H. Hanson		6-23-71	
		ENGR		J. Hanson		6-25-71	
		MFG		10/10/71		7-17-71	
		APPR		3 times OK		7-1-71	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES ±5%		OHMS		1/4 W			
CAP ±10%							
		CODE IDENT		DRAWING NUMBER		CD.	
		19333		C 54139400		3	
		SHEET 1 OF 2					

70629100 E

4-197



REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
B		SEE SHT 1 FOR REV				

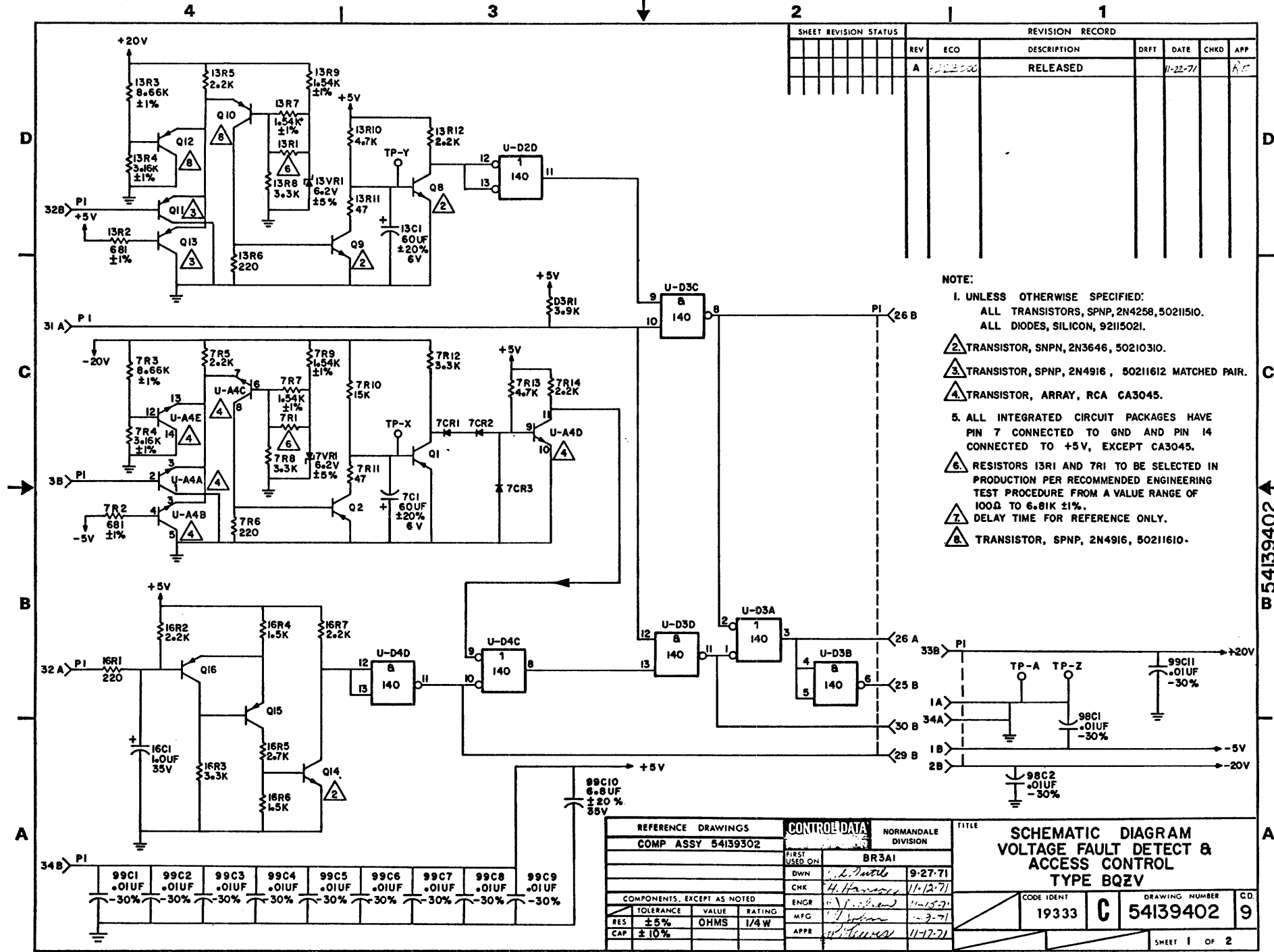


CONTROL DATA
NORMANDE
DIVISION

SCHEMATIC DIAGRAM
VOLTAGE FAULT DETECT &
ACCESS CONTROL
TYPE AQZV

CODE IDENT 19333	DWG NO C 54139400	C.D. 3
SHEET 2		

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	2	RELEASED		11-22-71		A.C.	



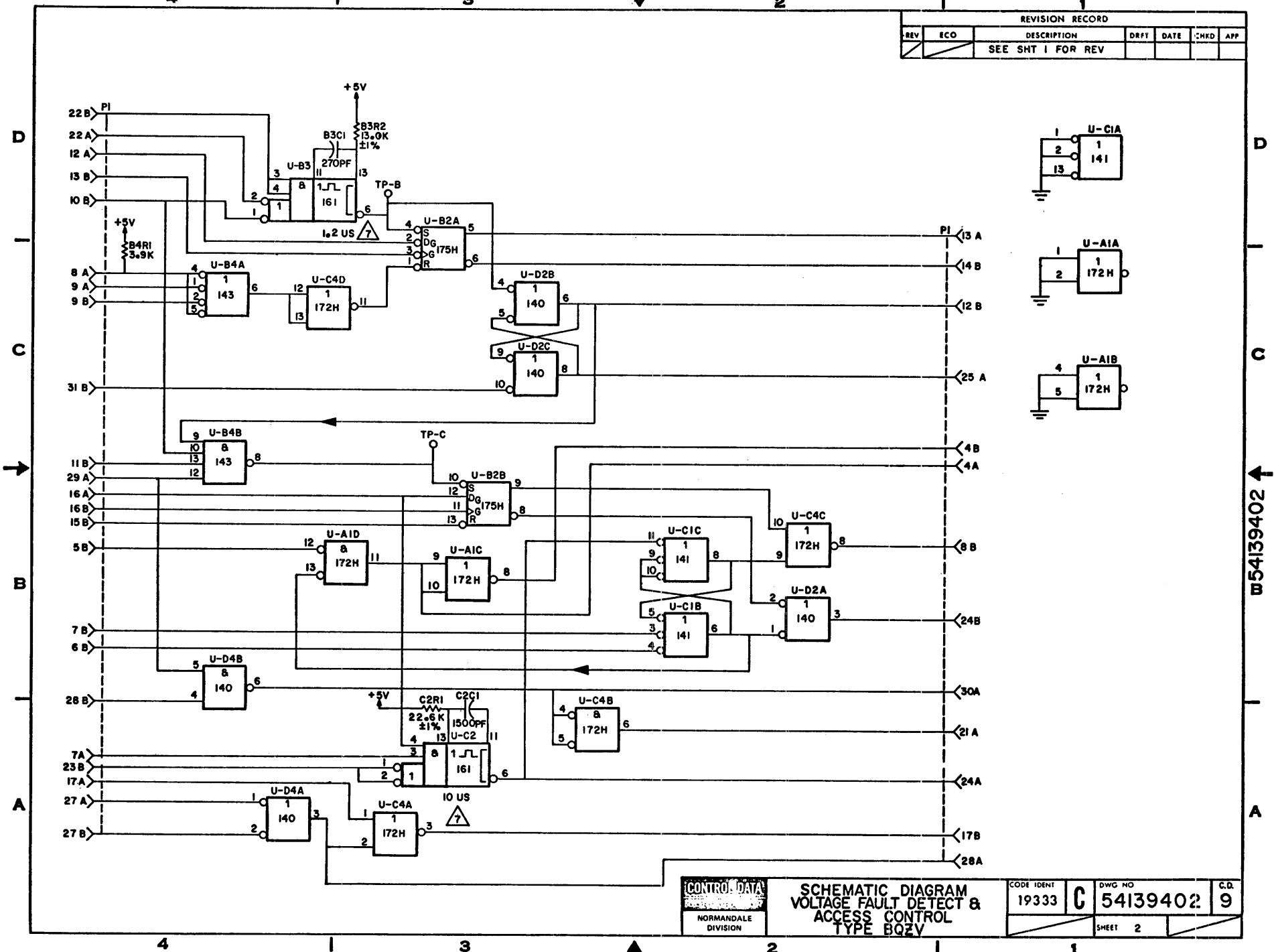
- NOTE:
- UNLESS OTHERWISE SPECIFIED:
ALL TRANSISTORS, SPNP, 2N4258, 50211510.
ALL DIODES, SILICON, 92115021.
 - TRANSISTOR, SPNP, 2N3646, 50210310.
 - TRANSISTOR, SPNP, 2N4916, 50211612 MATCHED PAIR.
 - TRANSISTOR, ARRAY, RCA CA3045.
 - ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V, EXCEPT CA3045.
 - RESISTORS 13R1 AND 7R1 TO BE SELECTED IN PRODUCTION PER RECOMMENDED ENGINEERING TEST PROCEDURE FROM A VALUE RANGE OF 100Ω TO 6.81K ±1%.
 - DELAY TIME FOR REFERENCE ONLY.
 - TRANSISTOR, SPNP, 2N4916, 50211610.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54139302		FIRST USED ON		BR3A1		SCHEMATIC DIAGRAM	
		DWN		L. Antle		VOLTAGE FAULT DETECT &	
		CHK		H. Hanson		ACCESS CONTROL	
		ENGR		11-15-71		TYPE BQZV	
		MFG		11-2-71		CODE IDENT	
		APPR		11-17-71		19333	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		DRAWING NUMBER	
RES		± 5%		OHMS		54139402	
CAP		± 10%		RATING		C.D.	
				1/4 W		9	
						SHEET 1 OF 2	

HPD

54139402

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFY	DATE	CHKD	APP
		SEE SHT 1 FOR REV				



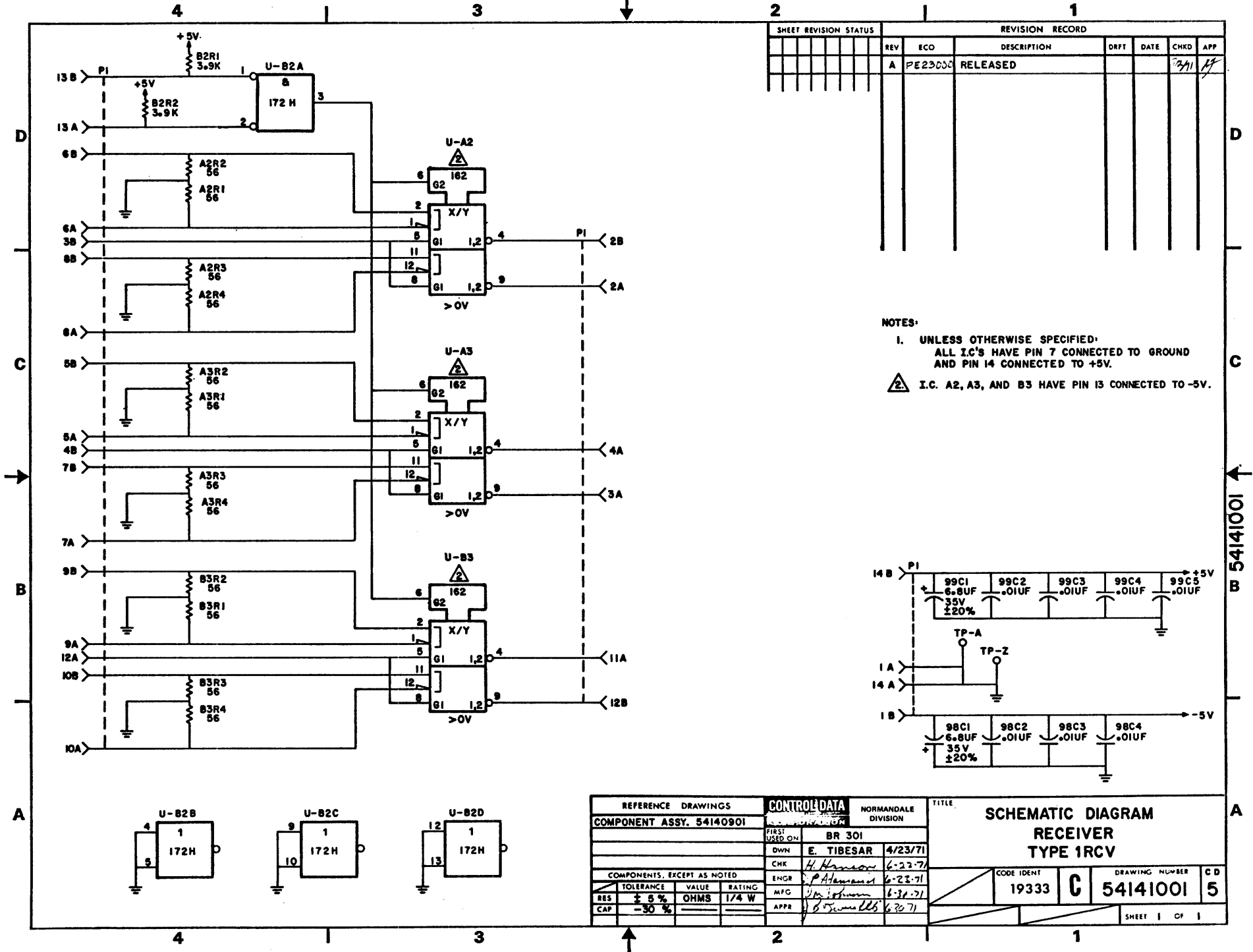
CONTROL DATA NORMANDEALE DIVISION	SCHEMATIC DIAGRAM VOLTAGE FAULT DETECT & ACCESS CONTROL TYPE BQZY			CODE IDENT 19333	DWG NO C 54139402	C.D. 9
			SHEET 2			

W54139402

4-200

70629100 E

SHEET REVISION STATUS		REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	PE2303C	RELEASED						

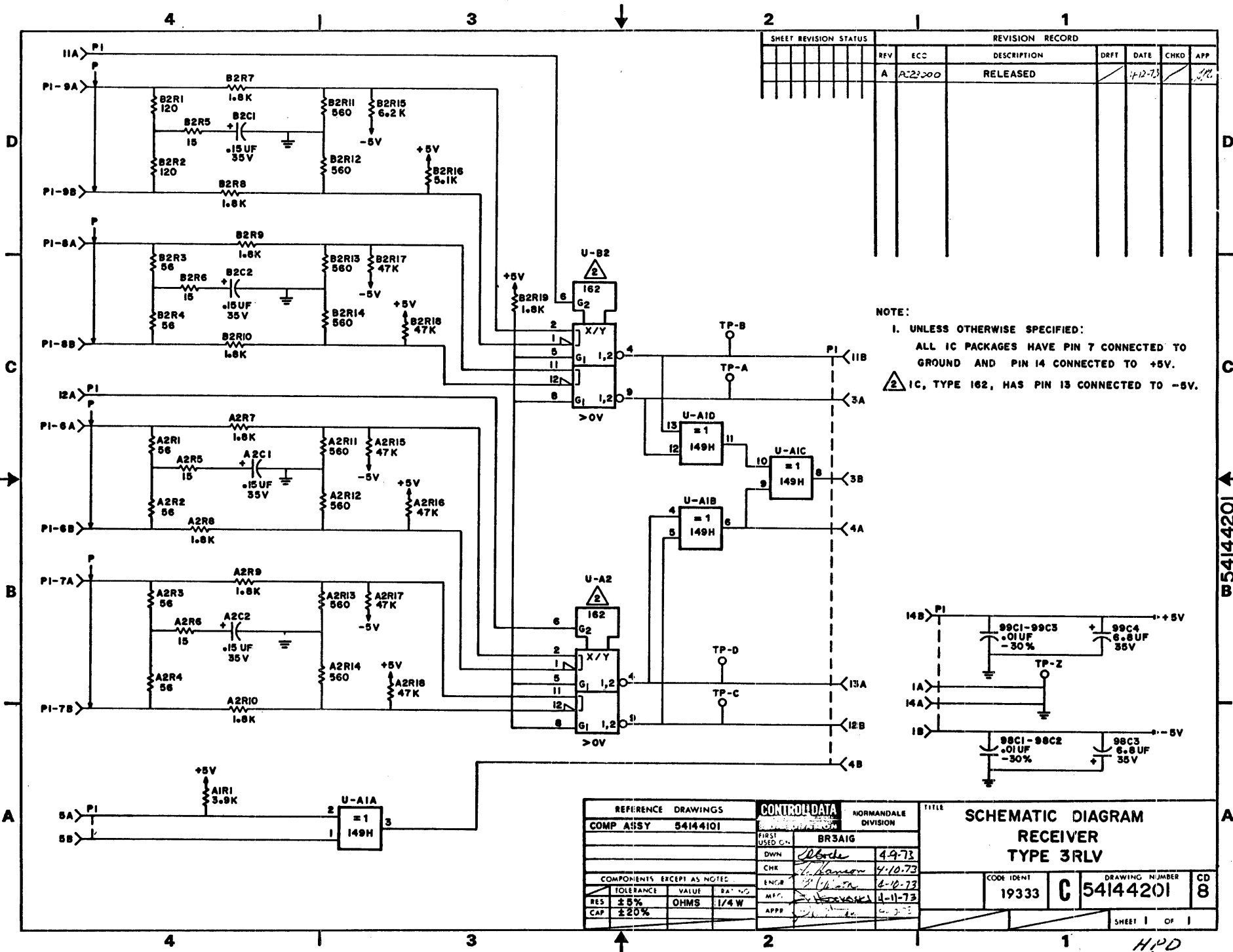


NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL I.C.'S HAVE PIN 7 CONNECTED TO GROUND
 AND PIN 14 CONNECTED TO +5V.
 △ I.C. A2, A3, AND B3 HAVE PIN 13 CONNECTED TO -5V.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY. 54140901		FIRST USED ON BR 301		DWN E. TIBESAR 4/23/71		SCHEMATIC DIAGRAM RECEIVER TYPE 1RCV	
COMPONENTS, EXCEPT AS NOTED		CHK H. Hanson 6-22-71		ENGR P. Adams 6-23-71		CODE IDENT 19333 C	
TOLERANCE VALUE RATING		MFG P. Adams 6-23-71		DRAWING NUMBER 54141001		CD 5	
RES ± 5 %	OHMS	APPR B. Swindle 6-30-71		SHEET 1 OF 1			
CAP -30 %							

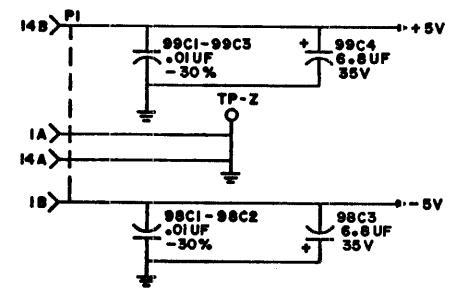
70629100 E

4-201



SHEET REVISION STATUS				REVISION RECORD			
REV	ECC	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	A-23-000	RELEASED		4-12-73			

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
 ⚠ IC, TYPE 162, HAS PIN 13 CONNECTED TO -5V.



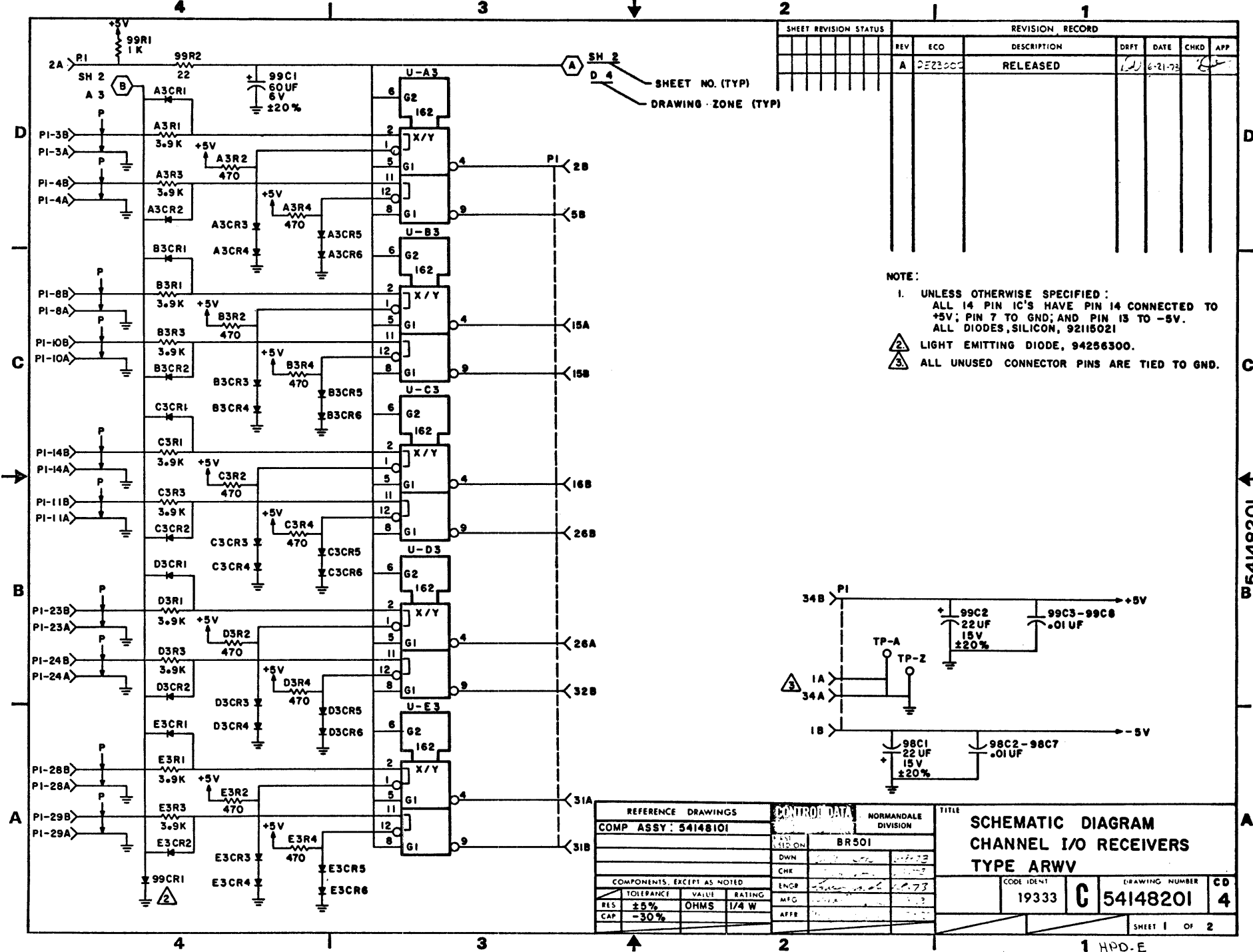
REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY	54144101	FIRST USED ON	BR3AIG	DWN	<i>[Signature]</i>	4-9-73	SCHEMATIC DIAGRAM RECEIVER TYPE 3RLV
		CHK	<i>[Signature]</i>	ENGR	<i>[Signature]</i>	4-10-73	
		RES	± 5%	MFG	<i>[Signature]</i>	4-11-73	
		CAP	± 20%	APP	<i>[Signature]</i>	4-11-73	
		COMPONENTS EXCEPT AS NOTED		CODE IDENT		DRAWING NUMBER	
				19333		C 54144201	
						CD 8	
						SHEET 1 OF 1	

W54144201

HPD

4-202

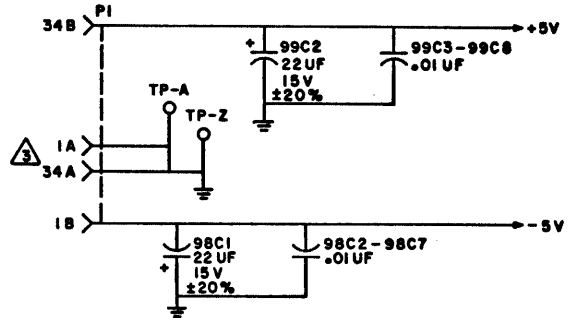
70629100 E



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	DEZ3000	RELEASED		6-21-73			

SHEET NO. (TYP)
DRAWING ZONE (TYP)

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL 14 PIN IC'S HAVE PIN 14 CONNECTED TO +5V; PIN 7 TO GND; AND PIN 13 TO -5V.
 ALL DIODES, SILICON, 92115021
 ⚠ LIGHT EMITTING DIODE, 94256300.
 ⚡ ALL UNUSED CONNECTOR PINS ARE TIED TO GND.



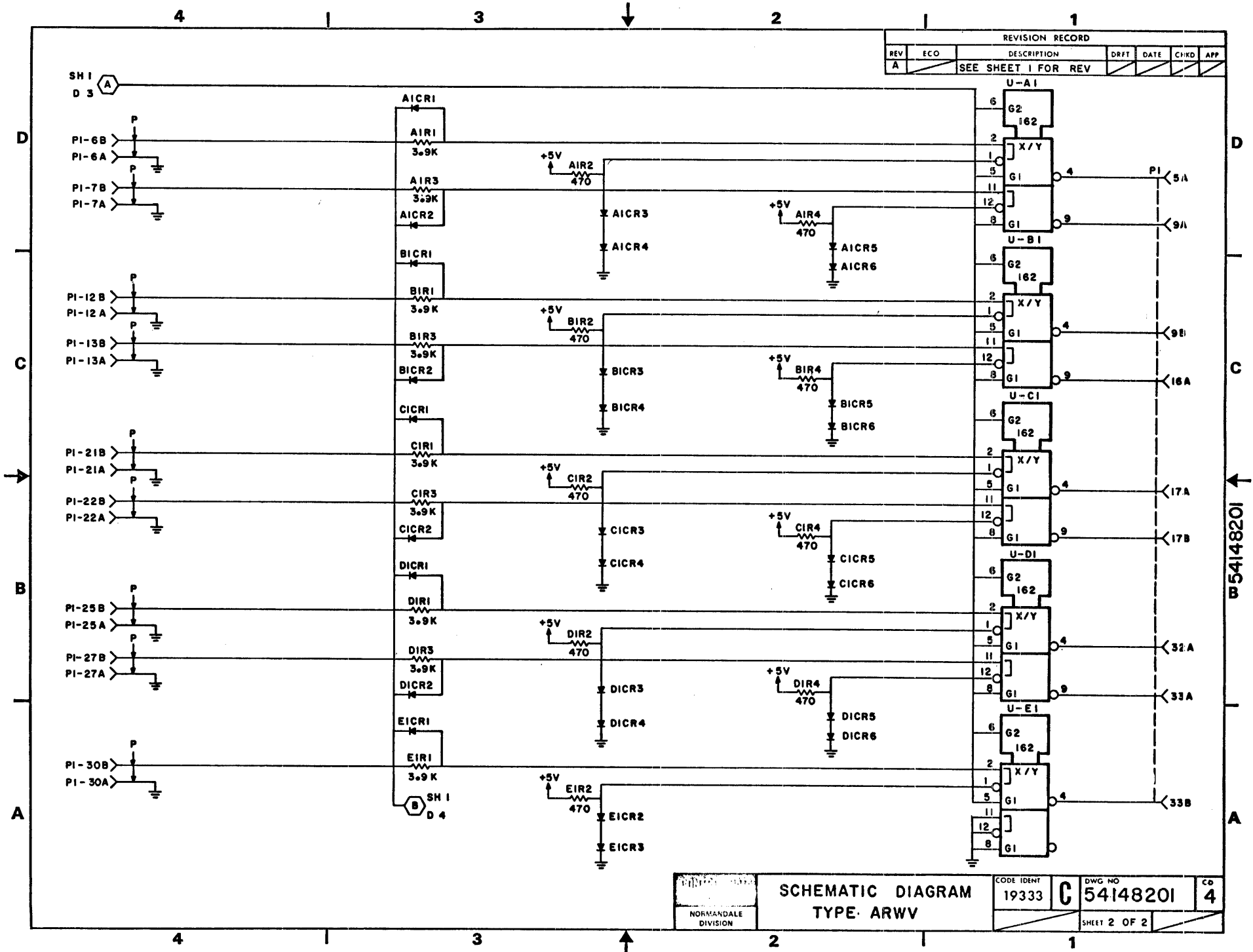
REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY: 54148101		BR 501				SCHEMATIC DIAGRAM CHANNEL I/O RECEIVERS TYPE ARWV	
COMPONENTS, EXCEPT AS NOTED		ENGR		DRAWING NUMBER		CD	
TOLERANCE	VALUE	RATING		19333	C	54148201	4
RES	±5%	OHMS	1/4 W				
CAP	-30%						

SHEET 1 OF 2

1 HPD-E

70629100 E

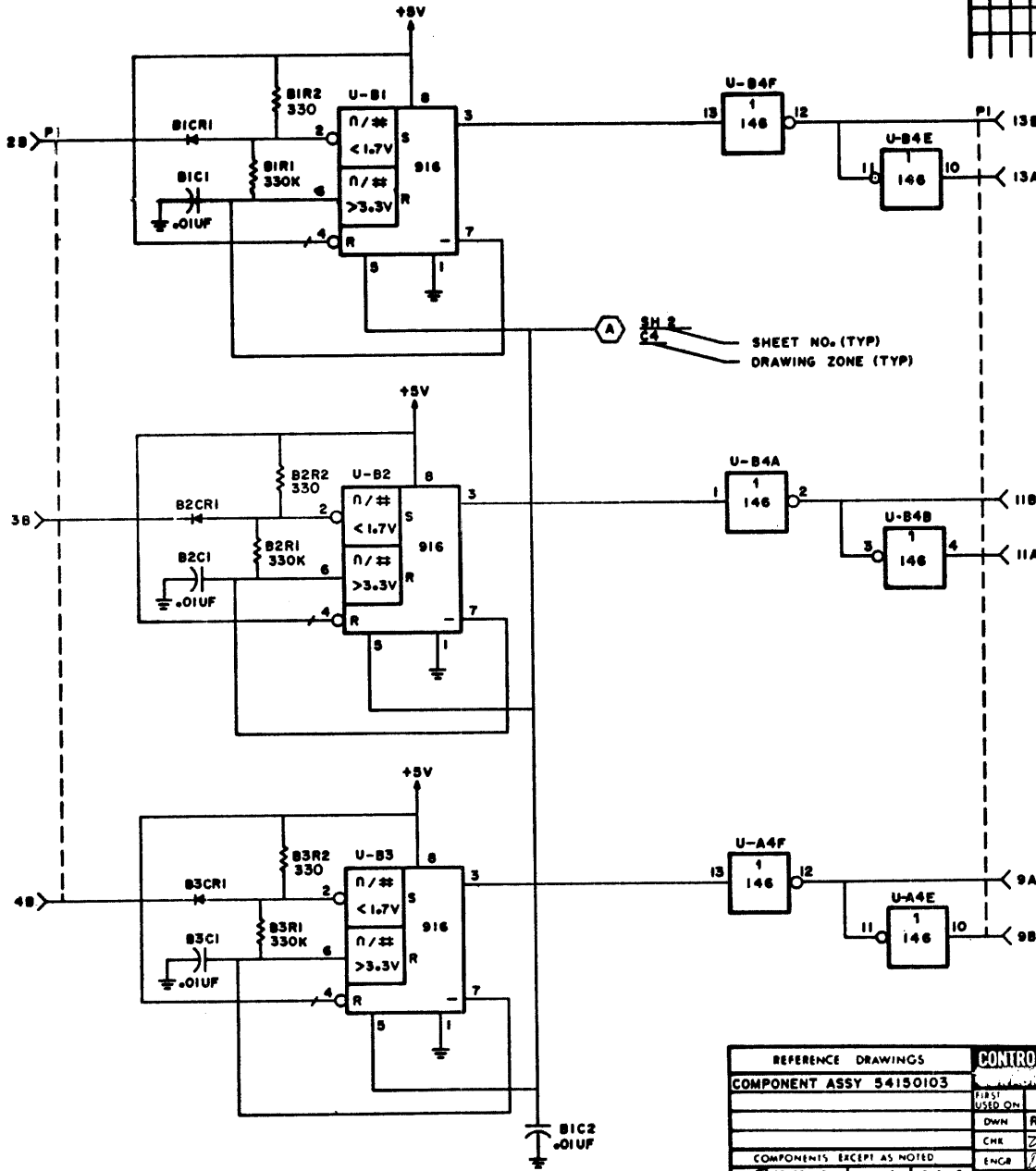
4-203



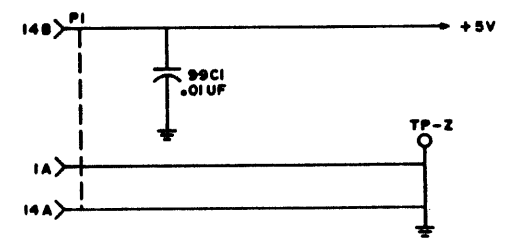
REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				

NORMANDEALE DIVISION	SCHEMATIC DIAGRAM TYPE ARWV		CODE IDENT 19333	DWG NO C 54148201	CD 4
				SHEET 2 OF 2	

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PER3000	RELEASED					



NOTE:
 1. UNLESS OTHERWISE SPECIFIED ;
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.
 ALL DIODES, GERMANIUM, 11801200.



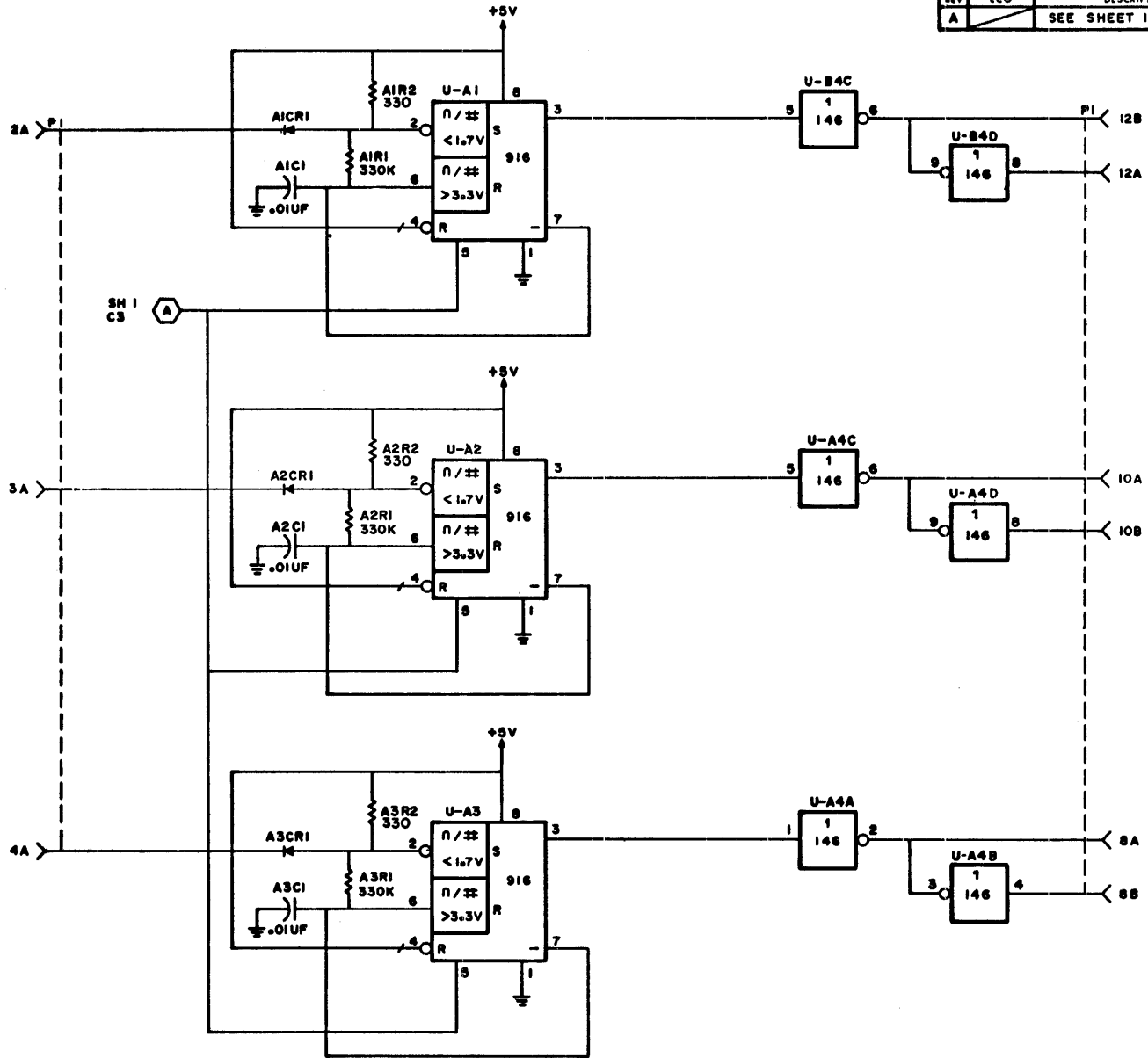
REFERENCE DRAWINGS	CONTROL DATA	NORMANDELE DIVISION	TITLE
COMPONENT ASSY 54150103	BR 302		SCHMATIC DIAGRAM SWITCH RECEIVER TYPE BSAV
	FIRST USED ON		
	DWN	R. KONECNY	2-11-74
	CHK	<i>V. J. Rittenberg</i>	2-11-74
	ENGR	<i>W. J. Rittenberg</i>	2-11-74
	MFG		2-12-74
	APP		
COMPONENTS EXCEPT AS NOTED		1701 146	1701 148
RES	± 5%	OHMS	1/4 W
CAP	-30%		
		19333	C 54150203
			5
		SHEET 1 OF 2	

W54150203

70629100 F

4-205

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA
NORMANDEALE
DIVISION

SCHEMATIC DIAGRAM
TYPE BSAV

CODE IDENT	19333	DWG NO	54150203	CR.	5
			SHEET 2		

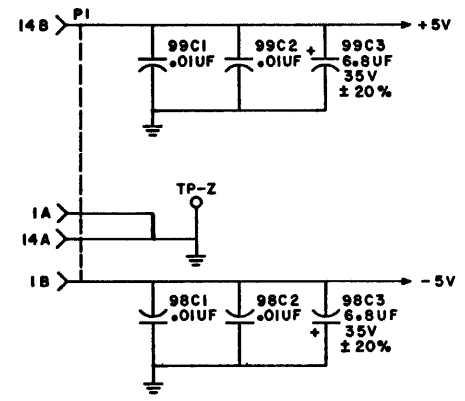
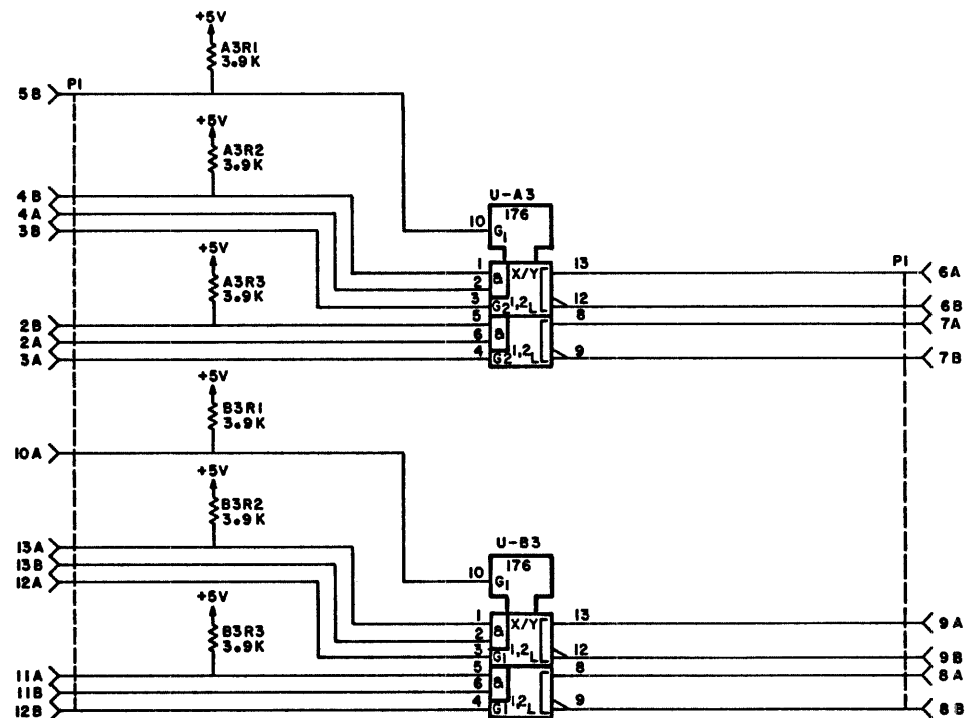
W54150203

4-206

70629100 E

SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP			
A	PE23CC	RELEASED							

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL IC'S HAVE PIN 7 CONNECTED TO GND; PIN 11 CONNECTED TO -5V; AND PIN 14 CONNECTED TO +5V.

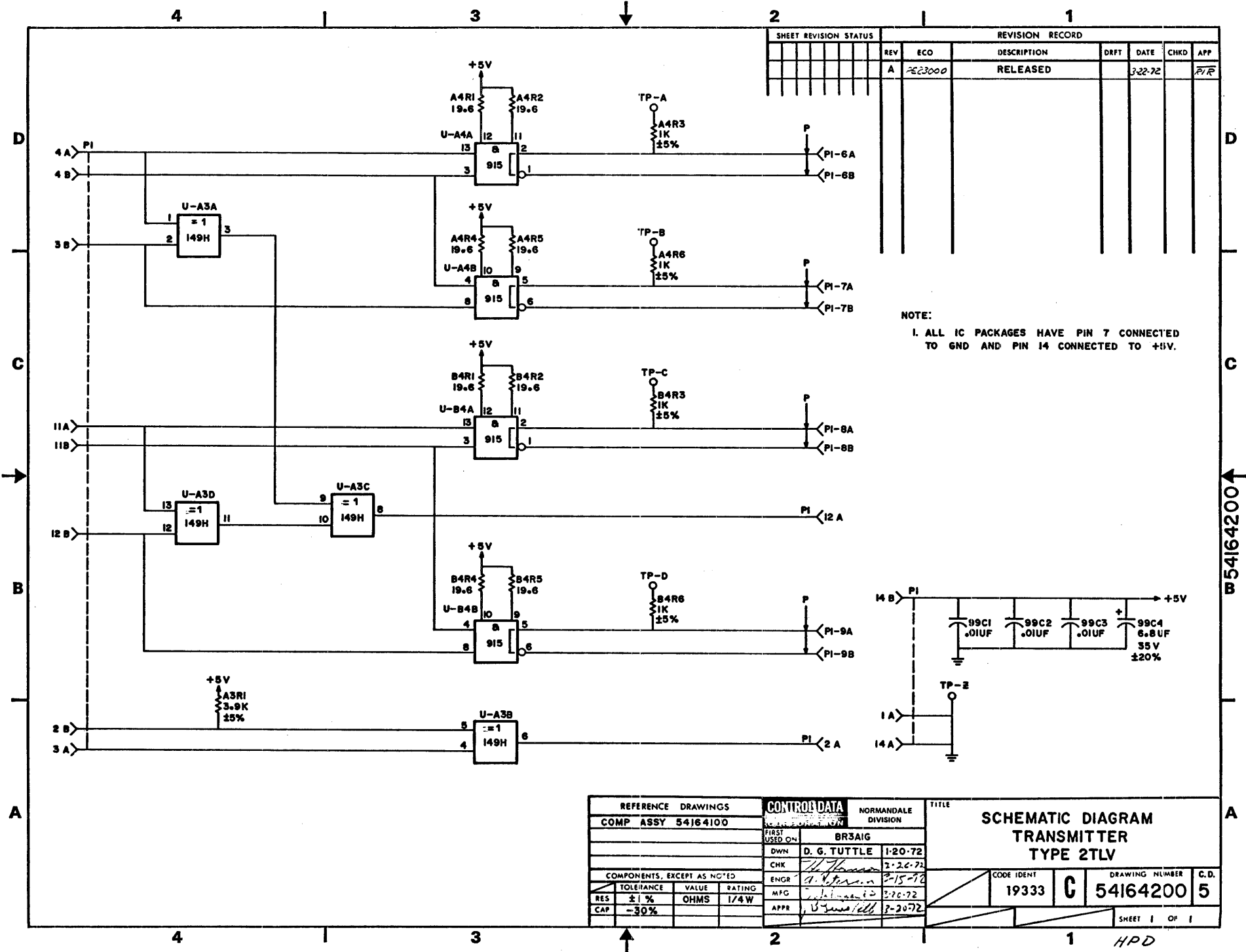


REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE			
COMP ASSY: 54160901		FIRST USED ON		BR301		SCHEMATIC DIAGRAM			
		DWN		7-14-71		TRANSMITTER			
		CHK		7-28-71		TYPE 1TCV			
COMPONENTS, EXCEPT AS NOTED		ENGR		7-28-71		CODE IDENT			
		MFG		8-9-71		DRAWING NUMBER			
		APPR		8-9-71		CD			
TOLERANCE	VALUE	RATING							
RES ± 5%	OHMS	1/4 W							
CAP - 30%									
						19333	C	54161001	O
								SHEET 1 OF 1	

HDP

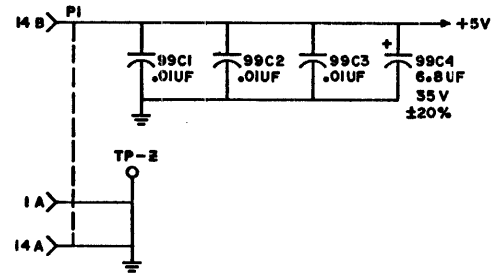
70629100 F

4-207



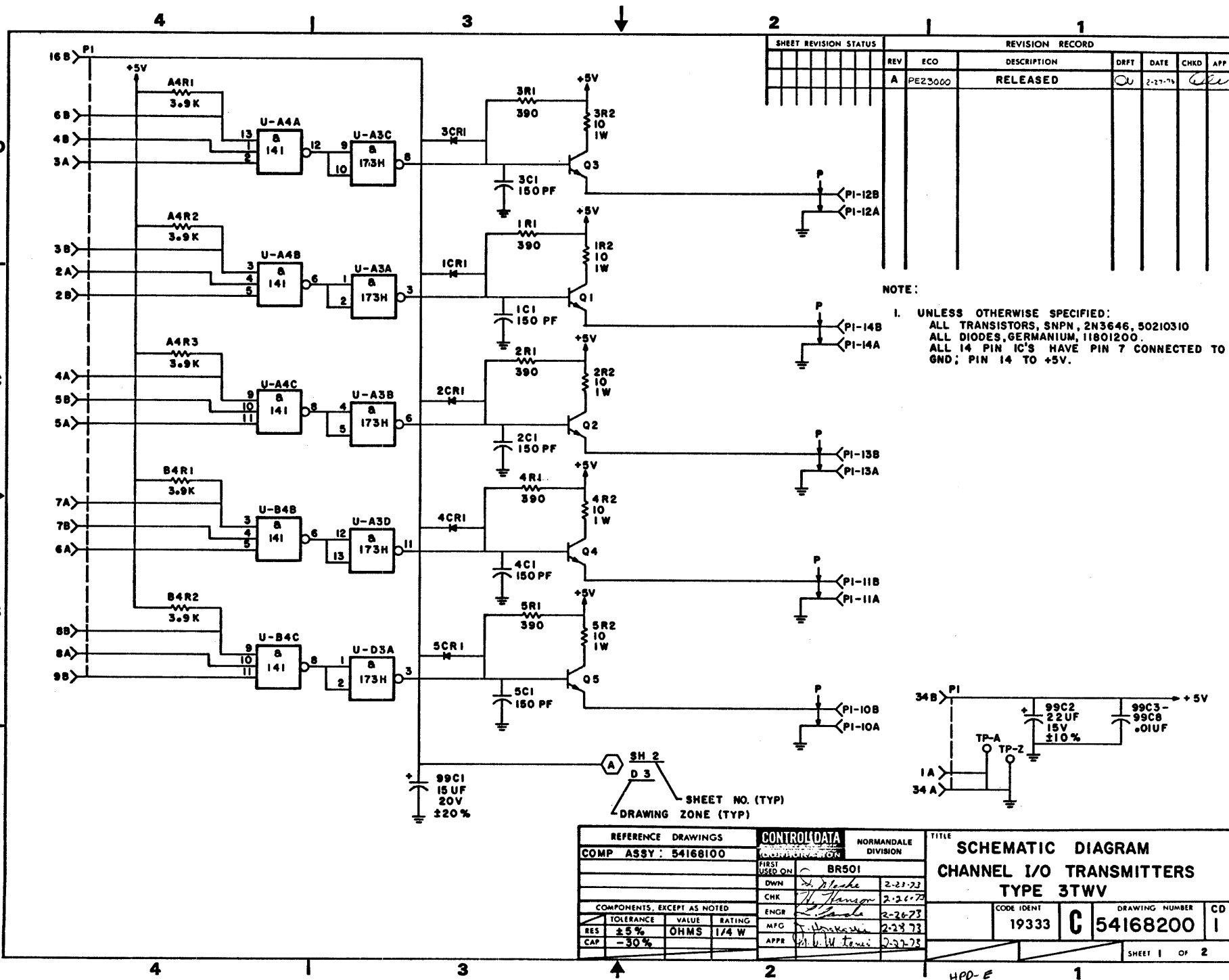
SHEET REVISION STATUS				REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A	FE23000	RELEASED		3-22-72		PTP		

NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54164100		FIRST USED ON BR3AIG		DWN D. G. TUTTLE 1-20-72		SCHEMATIC DIAGRAM TRANSMITTER TYPE 2TLV	
COMPONENTS, EXCEPT AS NOTED		CHK [Signature] 7-26-72		ENGR [Signature] 3-15-72		CODE IDENT 19333 C	
RES	± 1 %	OHMS	1/4 W	MFG [Signature] 3-26-72		DRAWING NUMBER	C.D.
CAP	-30 %			APPR [Signature] 3-20-72		54164200	5
						SHEET 1 OF 1	

HPD



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED		2-27-73			

NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N3646, 50210310
 ALL DIODES, GERMANIUM, 11801200.
 ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GND; PIN 14 TO +5V.

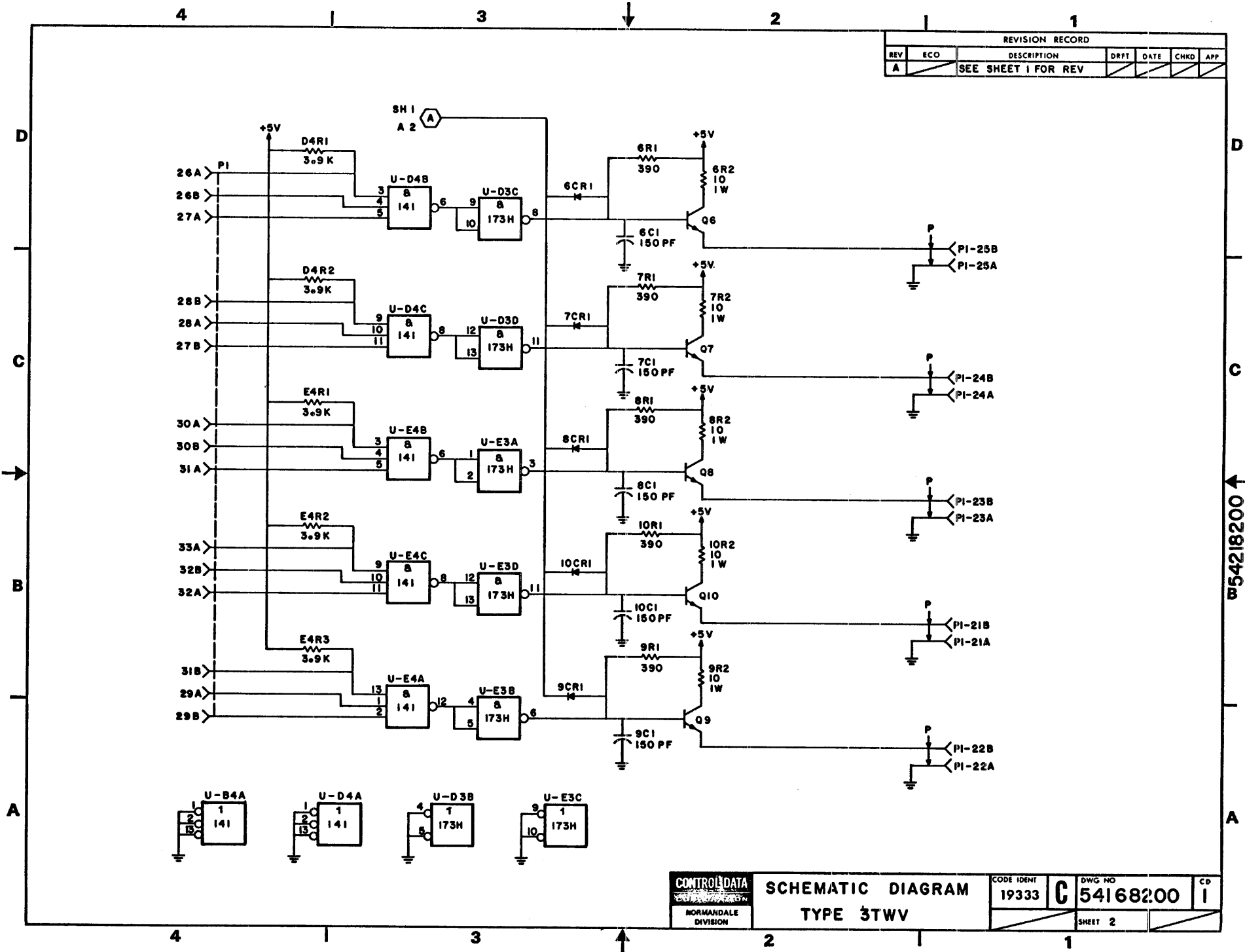
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54168100		FIRST USED ON: BR501				SCHEMATIC DIAGRAM	
		DWN: <i>S. H. Hinkle</i> 2-23-73				CHANNEL I/O TRANSMITTERS	
		CHK: <i>H. Hanson</i> 2-26-73				TYPE 3TW	
COMPONENTS, EXCEPT AS NOTED		ENGR: <i>S. H. Hinkle</i> 2-26-73		CODE IDENT: 19333		DRAWING NUMBER: 54168200	
TOLERANCE VALUE RATING		MFG: <i>S. H. Hinkle</i> 2-23-73		CD: 1		SHEET 1 OF 2	
RES ±5%	OHMS 1/4 W	APPR: <i>S. H. Hinkle</i> 2-23-73					
CAP -30%							

54168200

70629100 E

4-209

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1 FOR REV				



CONTROL DATA NORMANVILLE DIVISION	SCHEMATIC DIAGRAM TYPE 3TWV		CODE IDENT 19333	DWG NO C 54168200	CD 1
				SHEET 2	

4-210

70629100 E

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED					

NOTE:

1. UNLESS OTHERWISE SPECIFIED:
 ALL TRANSISTORS, SNPN, 2N3646, 50210310
 ALL DIODES, SILICON, 92115021

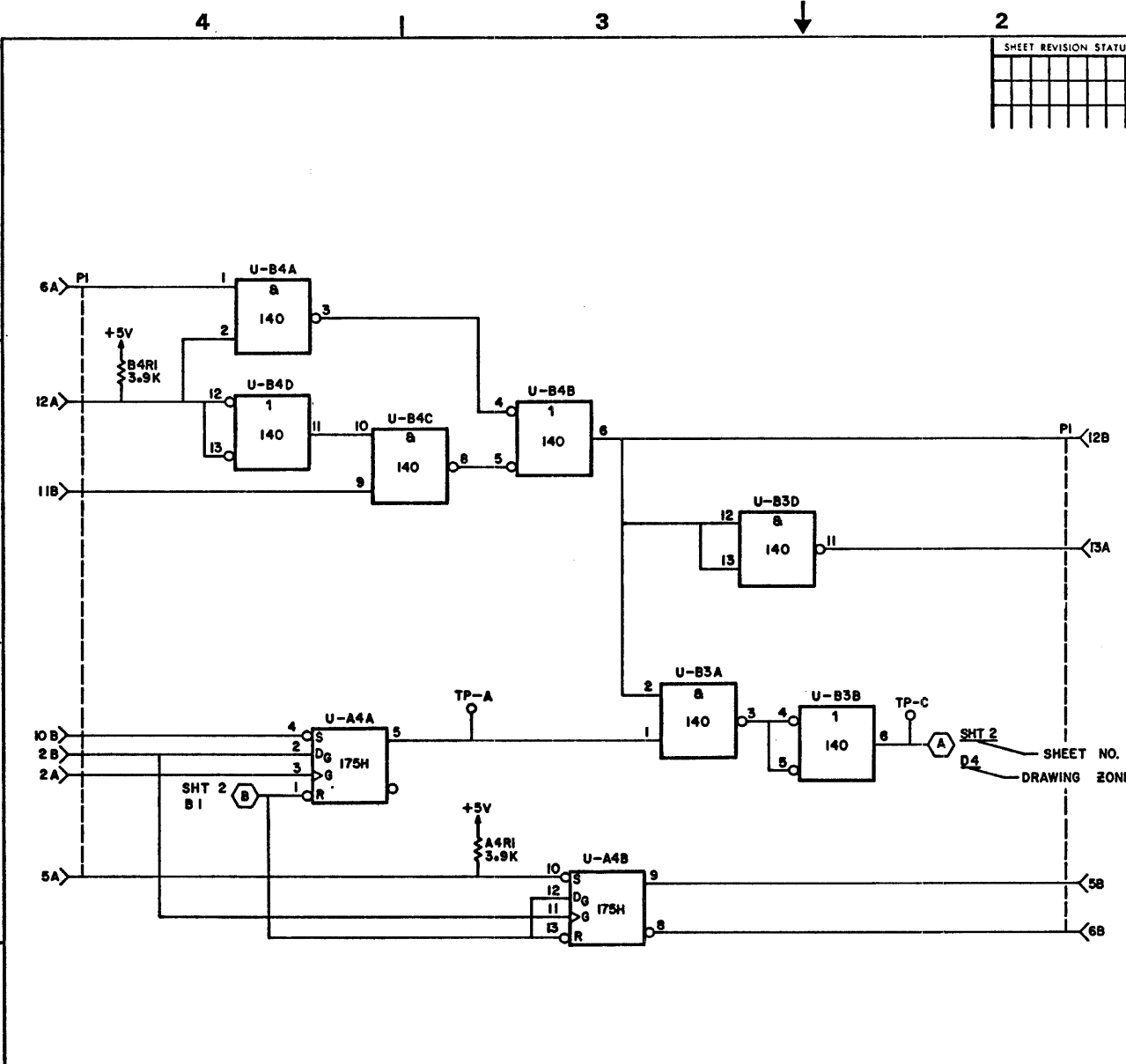
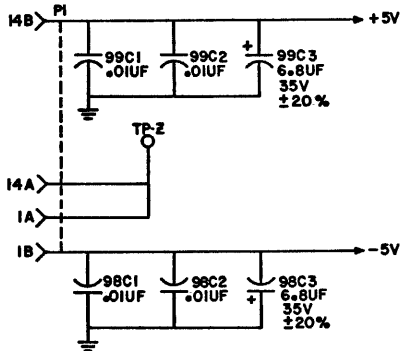
2. TRANSISTOR, SPNP, 2N4916, 50211610.
 3. TRANSISTOR, SNPN, 2N3568, 50210810.
 4. DIODE, ZENER, 50240108.

5. ALL IC. HAVE PIN 7 CONNECTED TO +5V, PIN 14 CONNECTED TO GRD.

6. VALUE OF A3R1 TO BE SELECTED IN PRODUCTION TO GIVE A PULSE OF 55US ± 7US AT OUTPUT PIN 3B.

7. VALUE OF IOR1 TO BE SELECTED IN PRODUCTION TO DETECT A SPEED OF 3000 R.P.M. ± 300 RPM WHEN PIN 9A IS GROUNDED.

8. DELAY TIME FOR REFERENCE ONLY.

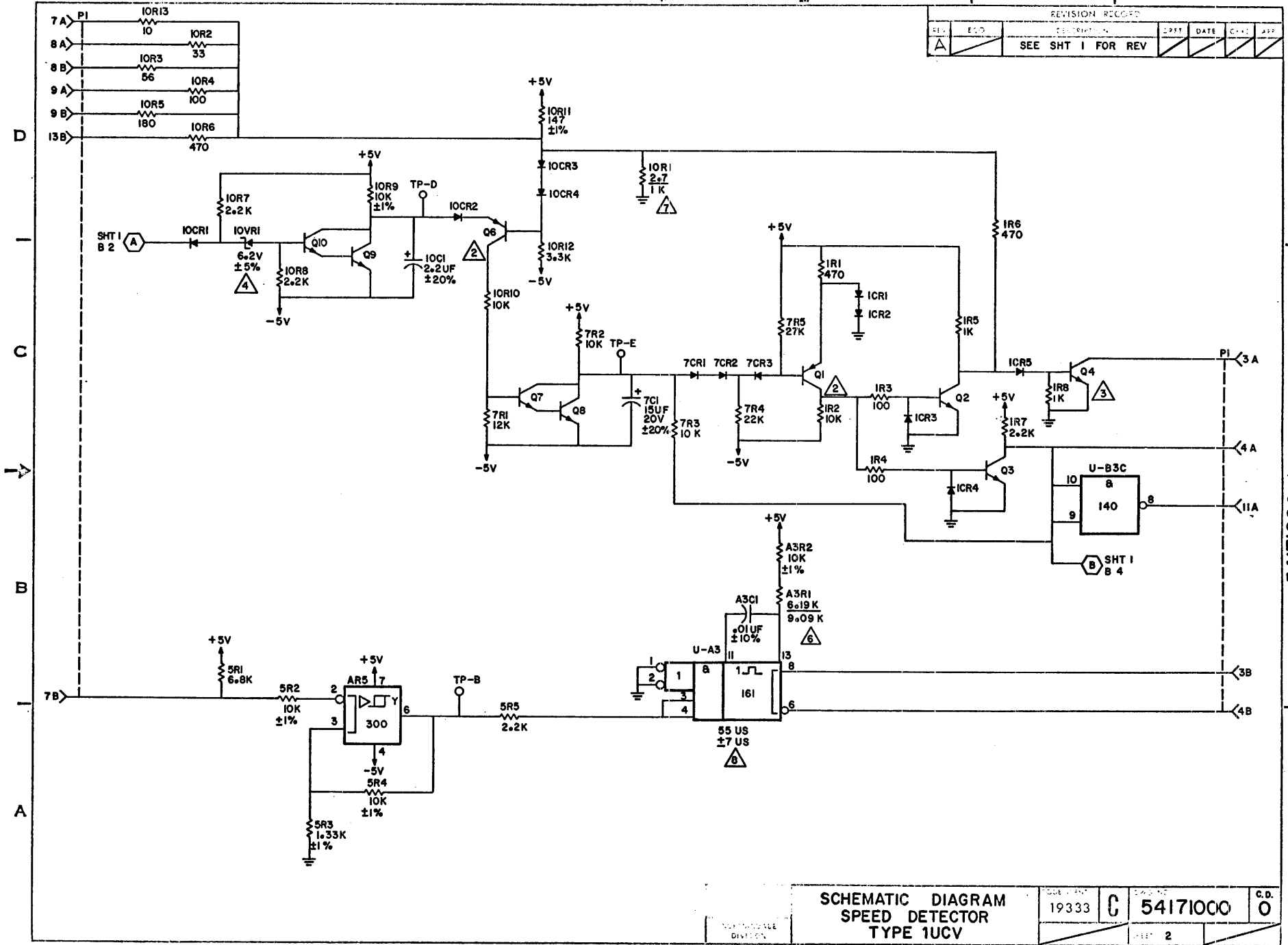


REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE		
COMP ASSY 54170900			BR301				SCHEMATIC DIAGRAM SPEED DETECTOR TYPE 1UCV		
COMPONENTS, EXCEPT AS NOTED			FIRST USED ON	DWN	CHK	ENGR	MFG	APPR	
			DWN	D. G. TUTTLE	4-22-71	CHK	H. Hanson	5-11-71	
			ENGR	D. G. Tuttle	4-22-71	MFG	W. J. ...	5-11-71	
			APPR	R. ...	5-11-71				
RES	± 5%	1/4 W	OHMS						
CAP	- 30V								
							CODE IDENT	DRAWING NUMBER	C.D.
							19333	54171000	0
							SHEET 1 OF 2		

70629100 E

4-211

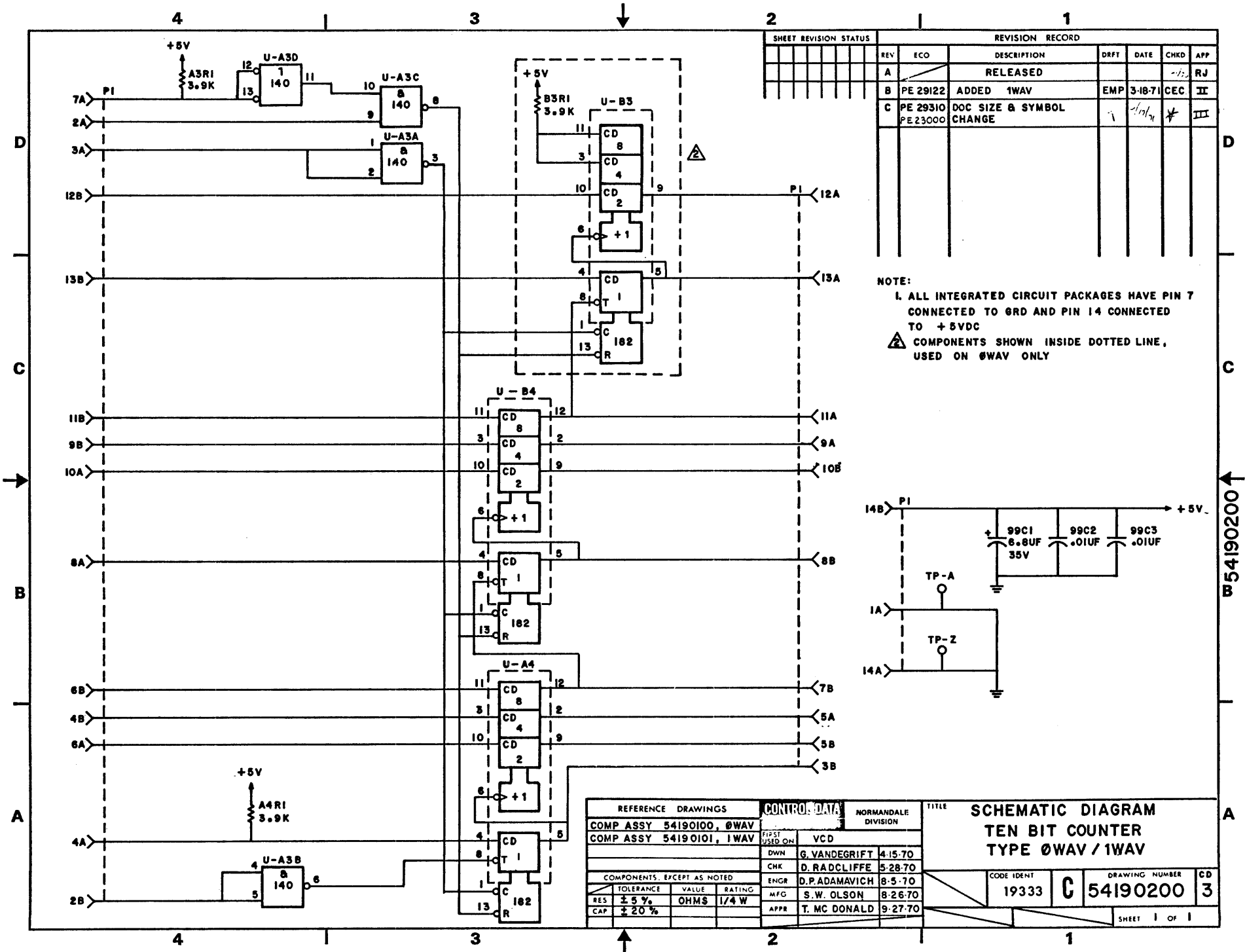
REVISION RECORD						
REV	ECO	DESCRIPTION	DATE	CHKD	APP	
A		SEE SHT 1 FOR REV				



SCHMATIC DIAGRAM
SPEED DETECTOR
TYPE 1UCV

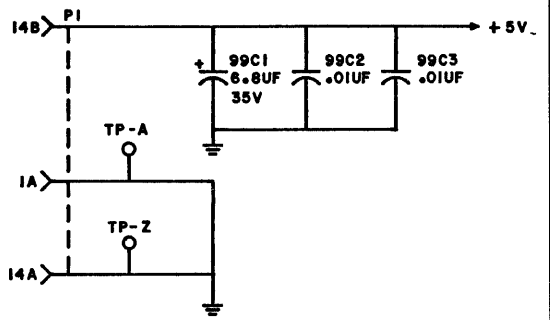
DATE	19333	REV	C	54171000	C.D.	0
			2			

54171000



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					RJ
B	PE 29122	ADDED 1WAV	EMP	3-18-71	CEC		II
C	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE					

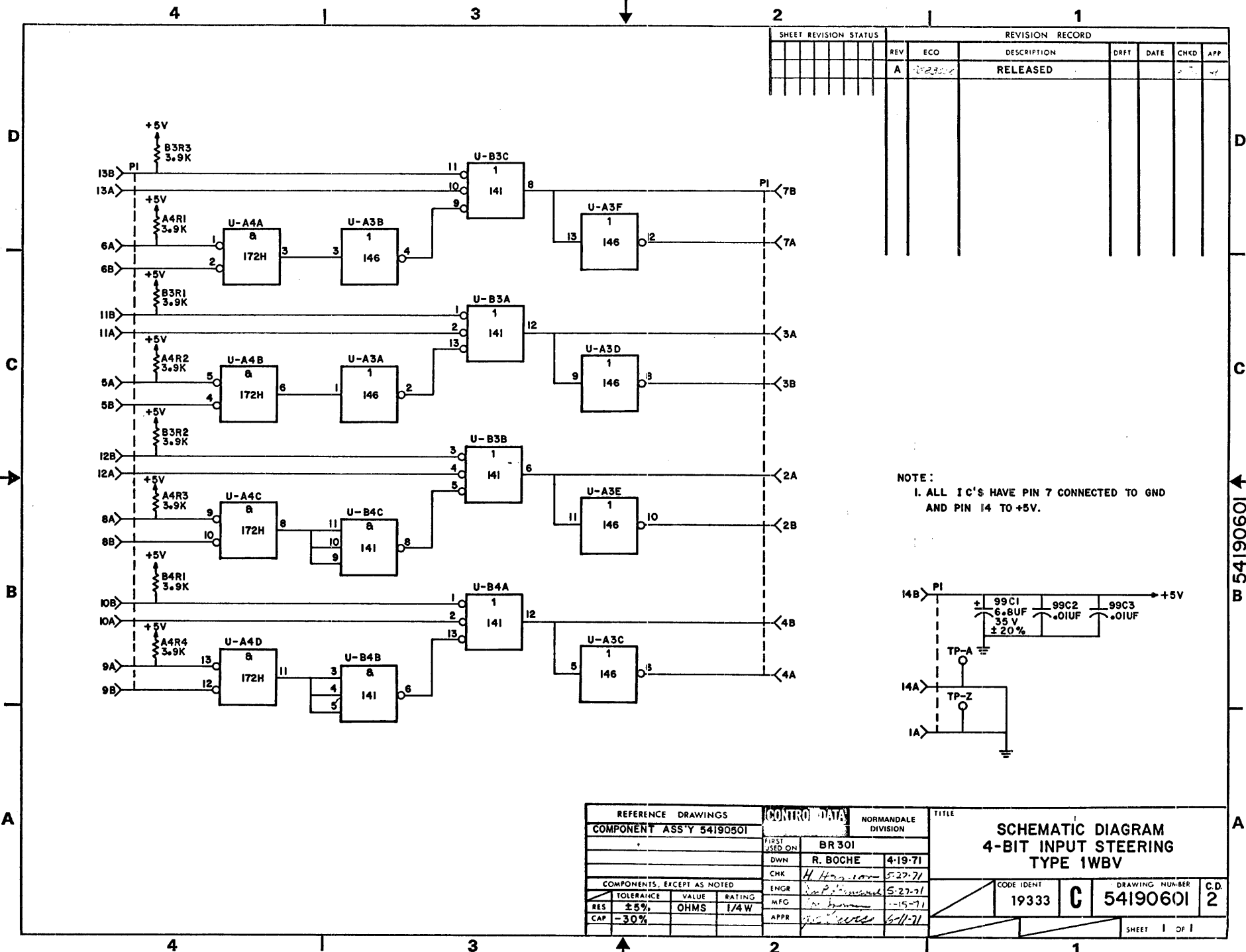
NOTE:
 1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO 0RD AND PIN 14 CONNECTED TO +5VDC
 ⚠ COMPONENTS SHOWN INSIDE DOTTED LINE, USED ON 0WAV ONLY



REFERENCE DRAWINGS			CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY 54190100, 0WAV			FIRST USED ON		VCD		SCHEMATIC DIAGRAM	
COMP ASSY 54190101, 1WAV			DWN		G. VANDEGRIFT		4-15-70	
			CHK		D. RADCLIFFE		5-28-70	
COMPONENTS, EXCEPT AS NOTED			ENGR		D.P. ADAMAVICH		8-5-70	
TOLERANCE			VALUE		RATING		MFG	
RES ± 5%			OHMS		1/4 W		S.W. OLSON	
CAP ± 20%							APPR	
							T. MC DONALD	
							9-27-70	
							CODE IDENT	
							19333	
							DRAWING NUMBER	
							C 54190200	
							CD	
							3	
							SHEET 1 OF 1	

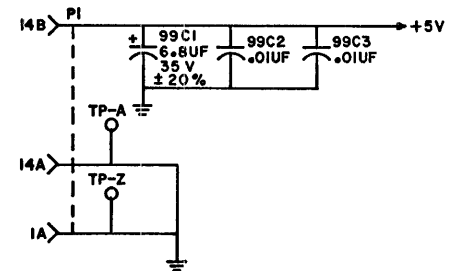
70629100 E

4-213



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					

NOTE:
1. ALL IC'S HAVE PIN 7 CONNECTED TO GND
AND PIN 14 TO +5V.



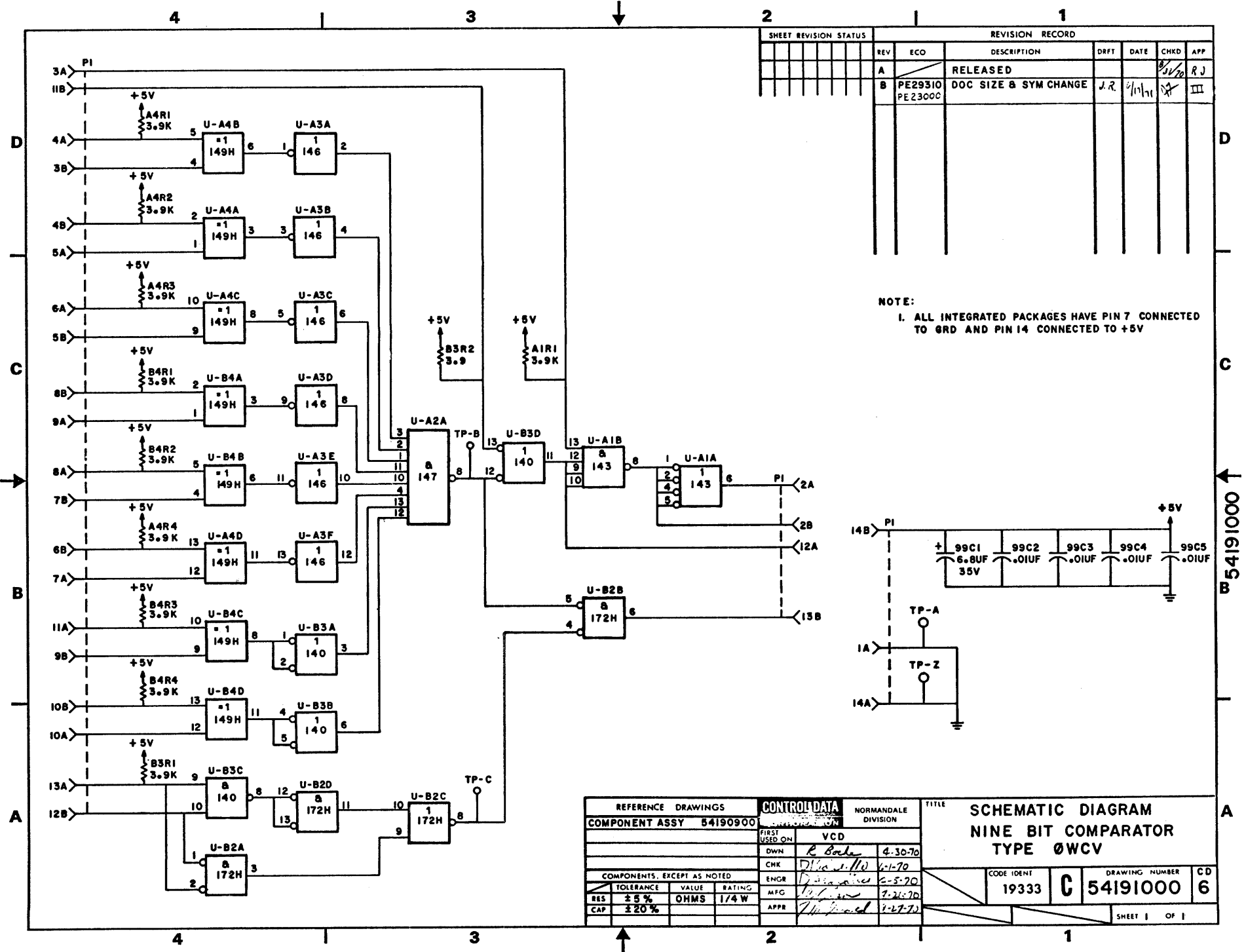
REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIVISION		TITLE	
COMPONENT ASS'Y 54190501		BR 301		4-19-71		SCHEMATIC DIAGRAM 4-BIT INPUT STEERING TYPE 1WBV	
COMPONENTS, EXCEPT AS NOTED		FIRST USED ON		DWN		CODE IDENT	
TOLERANCE		VALUE		RATING		DRAWING NUMBER	
RES	±5%	OHMS	1/4W	ENGR	H. H. ...	19333	C 54190601
CAP	-30%			MFG	...		C.D. 2
				APPR		SHEET 1 OF 1	

4-214

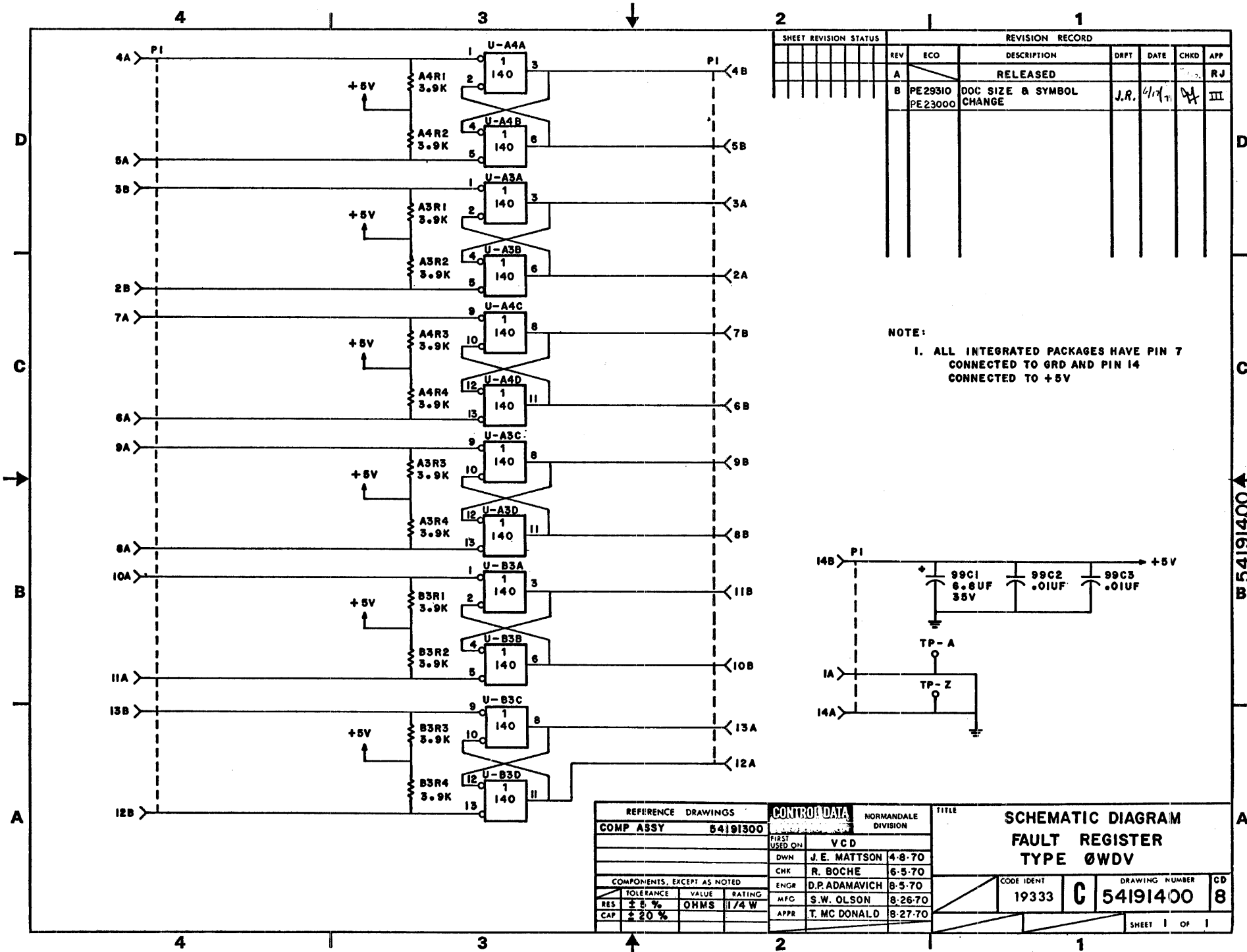
70629100 E

SHEET REVISION STATUS				REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP		
A		RELEASED				RJ		
B	PE29310 PE2300C	DOC SIZE & SYM CHANGE	J.R.	1/11/71		III		

NOTE:
I. ALL INTEGRATED PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V

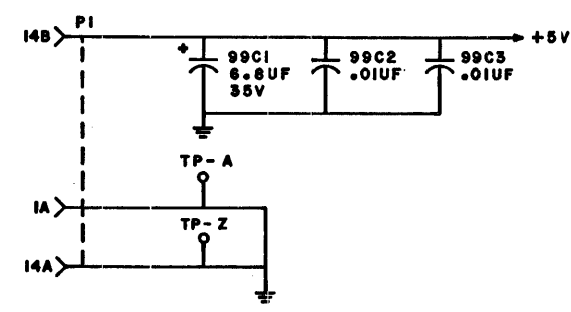


REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54190900		FIRST USED ON VCD		DWN R. Becker 4-30-70		SCHEMATIC DIAGRAM	
COMPONENTS, EXCEPT AS NOTED		ENGR D. J. ... 6-1-70		MFG ... 6-5-70		NINE BIT COMPARATOR	
TOLERANCE VALUE RATING		APPR ... 7-26-70		CODE IDENT 19333		DRAWING NUMBER 54191000	
RES ± 5 %	OHMS 1/4 W			CD 6		SHEET 1 OF 1	
CAP ± 20 %							



SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRPT	DATE	CHKD	APP	
A		RELEASED				RJ	
B	PE29310 PE23000	DOC SIZE & SYMBOL CHANGE	J.R.	6/17/71		III	

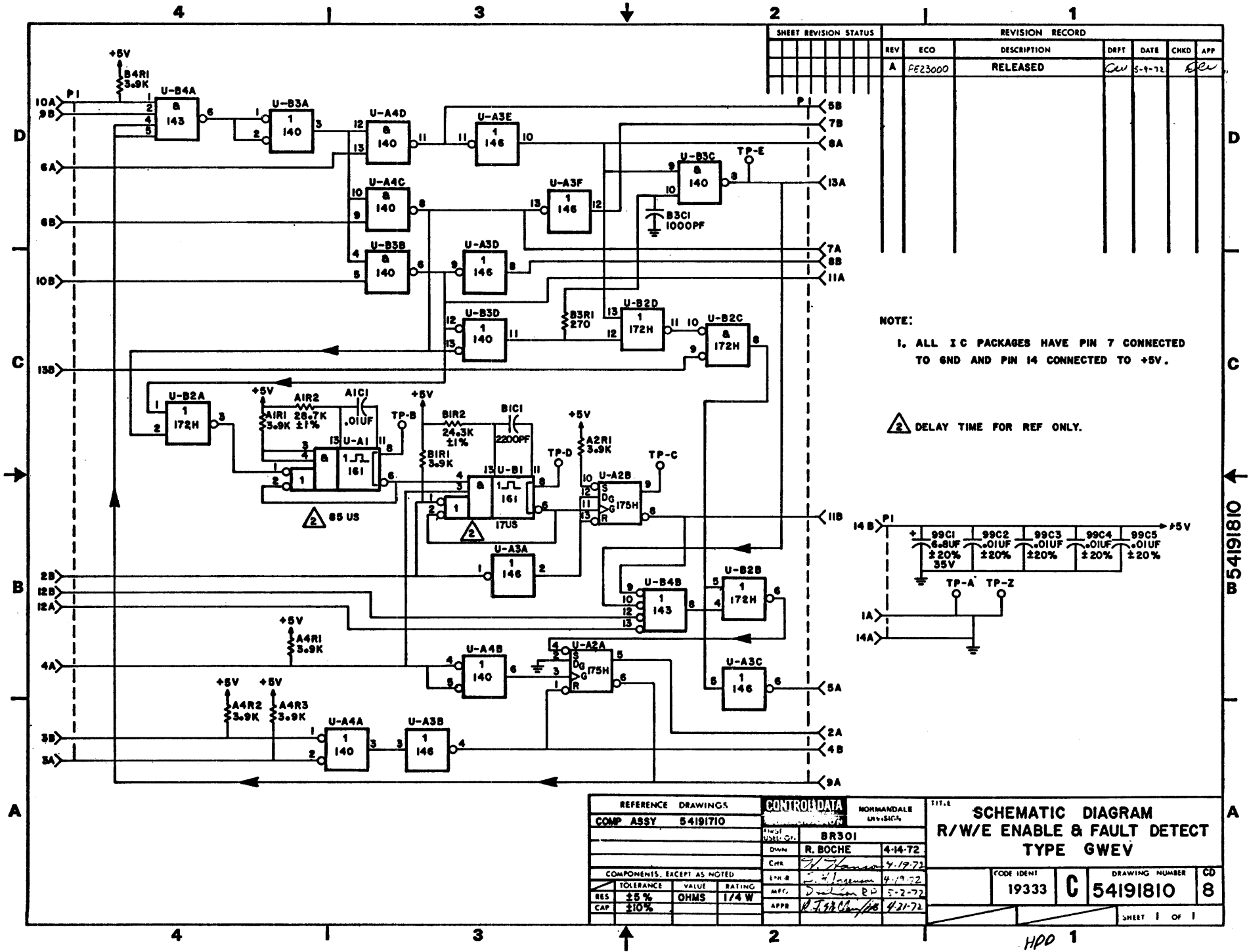
NOTE:
1. ALL INTEGRATED PACKAGES HAVE PIN 7
CONNECTED TO GRD AND PIN 14
CONNECTED TO +5V



REFERENCE DRAWINGS		CONTROL DATA		NORMANDELE DIVISION		TITLE	
COMP ASSY	54191300	FIRST USED ON:	VCD	SCHEMATIC DIAGRAM FAULT REGISTER TYPE ØWDV			
COMPONENTS, EXCEPT AS NOTED		DWN	J. E. MATTSON	4-8-70	CODE IDENT		
TOLERANCE		CHK	R. BOCHE	6-5-70	DRAWING NUMBER		
RES	± 5 %	ENGR	D.P. ADAMAVICH	8-5-70	CD		
MFC	OHMS	MFG	S.W. OLSON	8-26-70	19333 C 54191400 8		
CAP	± 20 %	RATING	1/4 W	8-27-70	SHEET 1 OF 1		

4-216

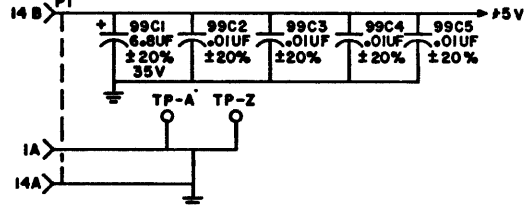
70629100 E



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	FE23000	RELEASED		5-9-72			

NOTE:
1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.

2 DELAY TIME FOR REF ONLY.



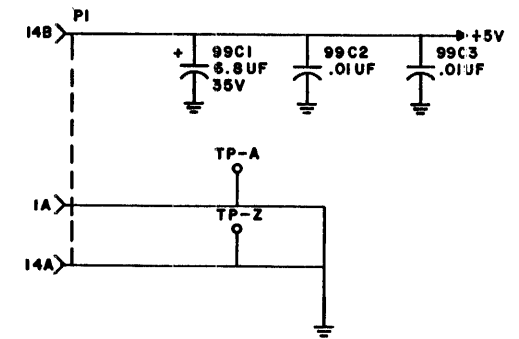
REFERENCE DRAWINGS		CONTROL DATA		NORMANDEALE DIV. SIGA		TITLE	
COMP ASSY	54191710	PART NUMBER	BR301	DATE	4-14-72	SCHEMATIC DIAGRAM R/W/E ENABLE & FAULT DETECT TYPE GWEV	
COMPONENTS, EXCEPT AS NOTED		DRWN	R. BOCHE	CHKD	4-17-72	CODE IDENT	19333
TOLERANCE	VALUE	RATING		DATE	5-2-72	DRAWING NUMBER	54191810
RES	±5%	OHMS	1/4 W	APPR	4-21-72	CD	8
CAP	±10%					SHEET	1 OF 1

HPD 1

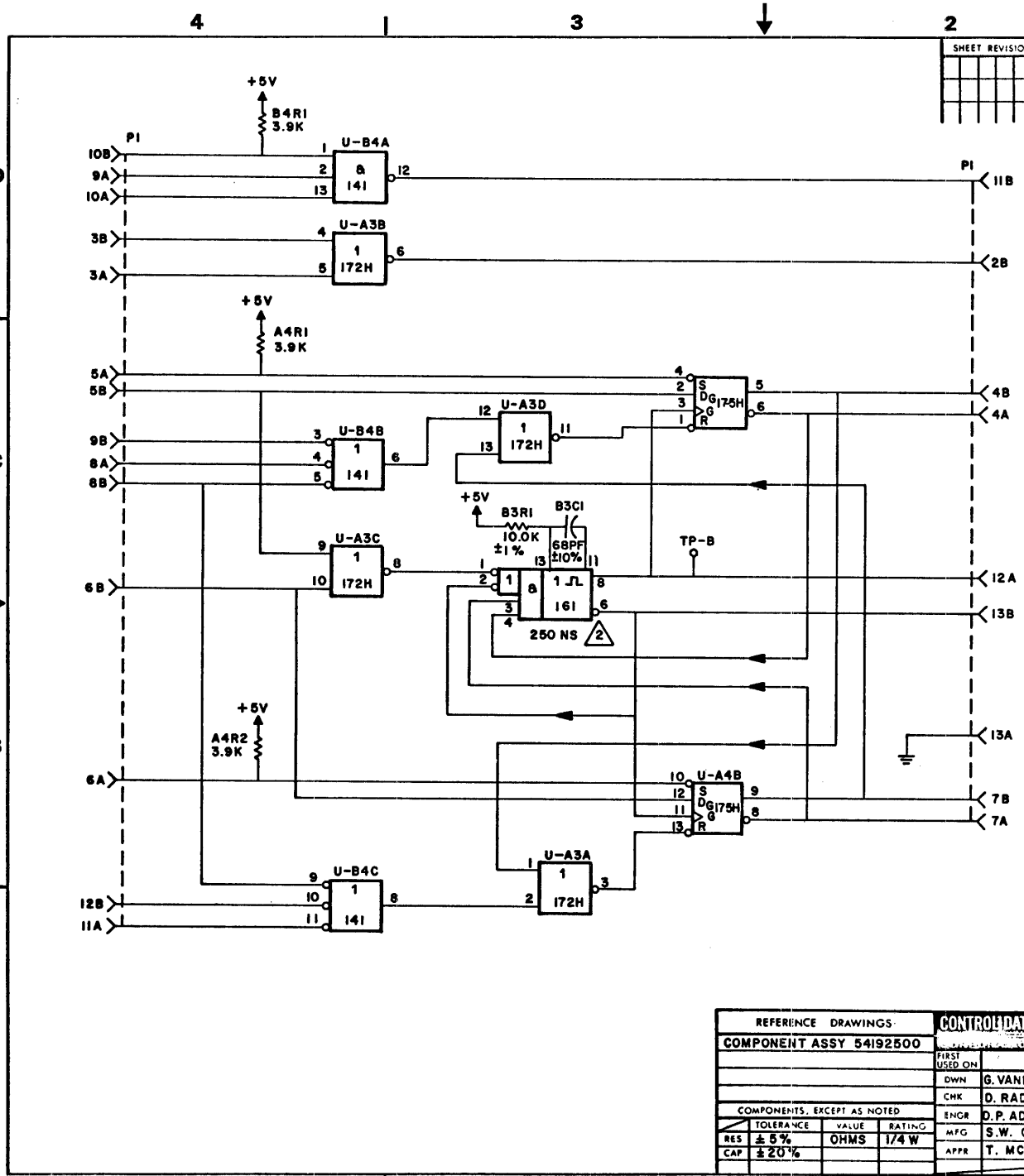
SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP.
A		RELEASED				RJ
B	PE 29310 PE 23000	DOC SIZE & SYMBOL CHANGE	JR	4/11/71		III

NOTE:

- ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5V
- DELAY TIME FOR REFERENCE ONLY.



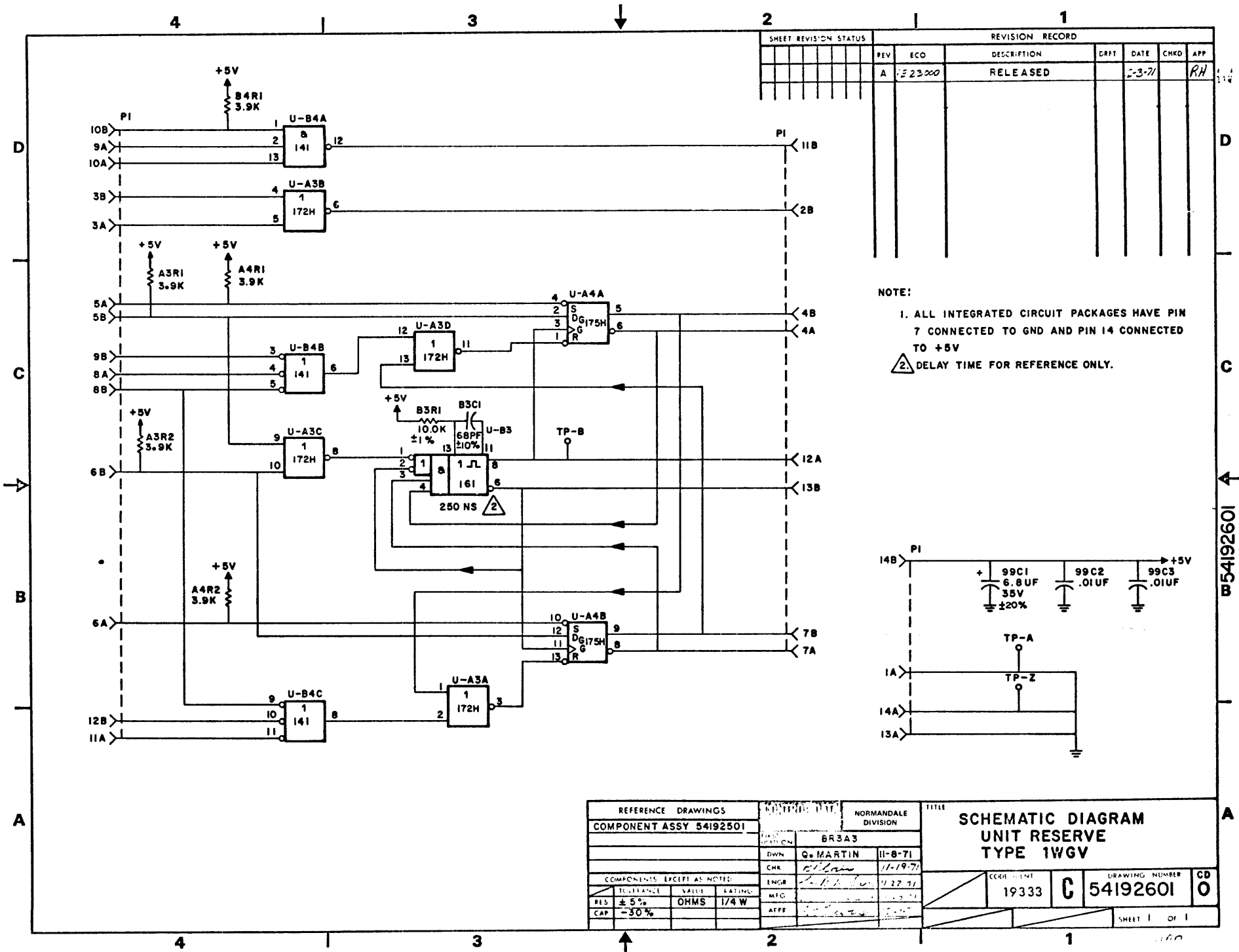
REFERENCE DRAWINGS		CONTROL DATA		NORMANDE DIVISION		TITLE	
COMPONENT ASSY 54192600		FIRST USED ON		VCD		SCHEMATIC DIAGRAM UNIT RESERVE TYPE ØWGV	
		DWN		G. VANDEGRIFT		4-14-70	
		CHK		D. RADCLIFFE		5-27-70	
		ENGR		D.P. ADAMAVICH		8-21-70	
		MFG		S.W. OLSON		9-3-70	
		APPR		T. McDONALD		9-27-70	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES		± 5%		OHMS		1/4 W	
CAP		± 20%					
		CODE IDENT		DRAWING NUMBER		CD	
		19333		C 54192600		2	
		SHEET		1 OF 1			



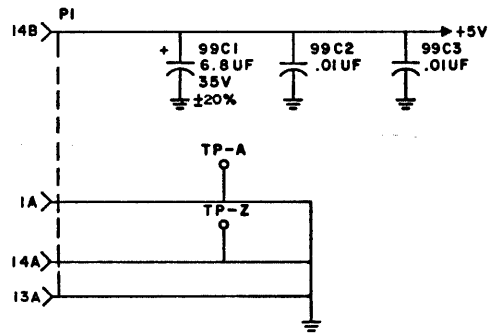
4-218

70629100 E

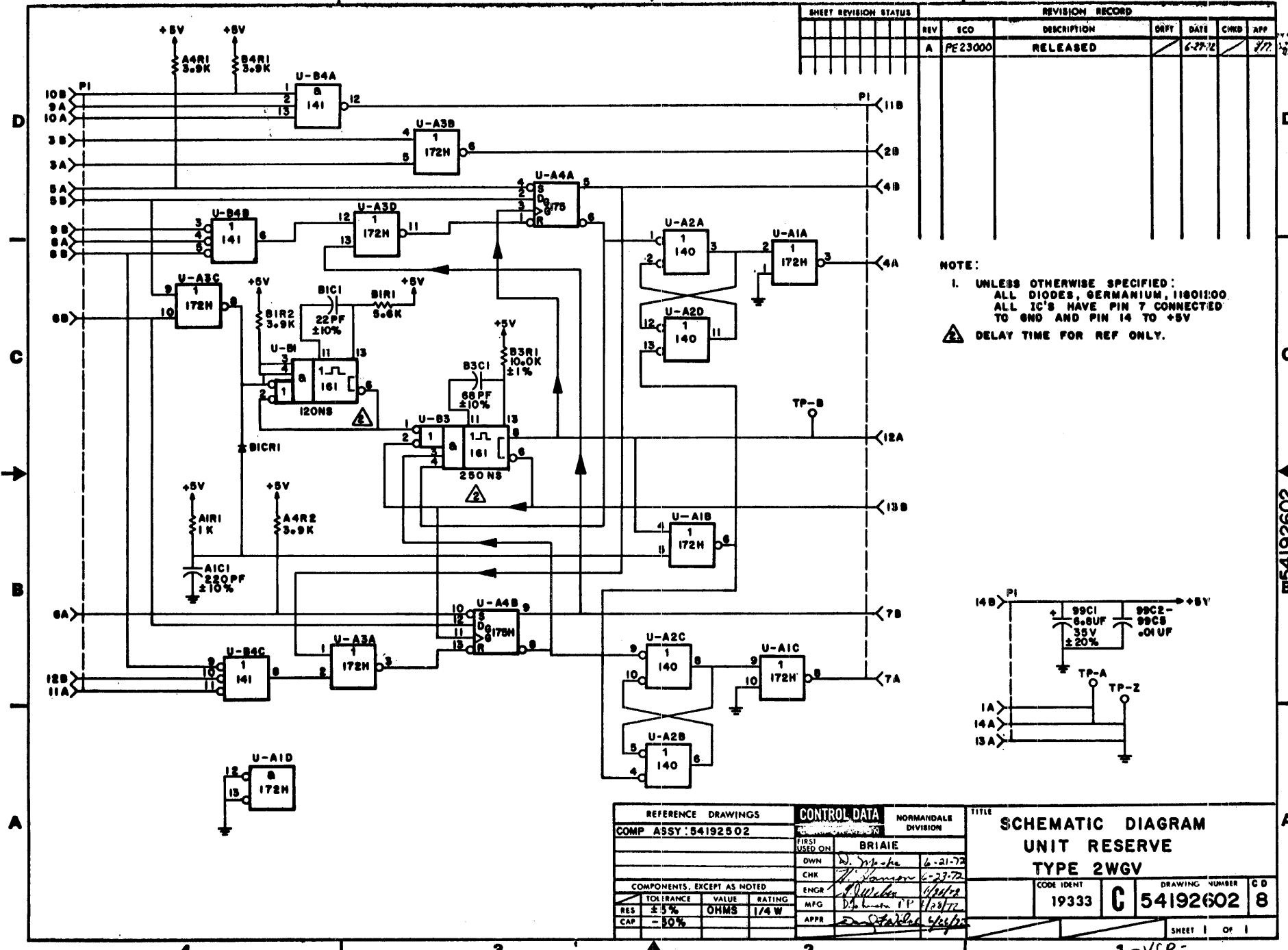
SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	122300	RELEASED		2-3-71		RH	



NOTE:
 1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 2. DELAY TIME FOR REFERENCE ONLY.

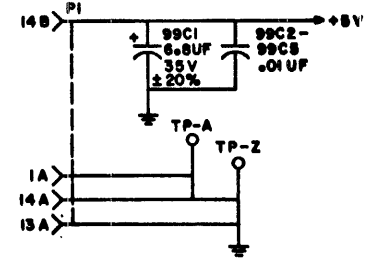


REFERENCE DRAWINGS	COMPONENT ASSY 54192501	6R3A3	NORMANDEALE DIVISION	TITLE	SCHEMATIC DIAGRAM UNIT RESERVE TYPE 1WGv
CHK	G. MARTIN	11-19-71			
ENGR		11-22-71			
MFG					
APP					
COMPONENTS EXCEPT AS NOTED:				CDR. NO.	19333
RES	± 5%	OHMS	1/4 W	CD	54192601
CAP	-30%				0
				SHEET	1 OF 1



SHEET REVISION STATUS				REVISION RECORD			
REV	SCO	DESCRIPTION	DRFT	DATE	CHKD	APP	VS
A	PE23000	RELEASED		6-27-72			1374

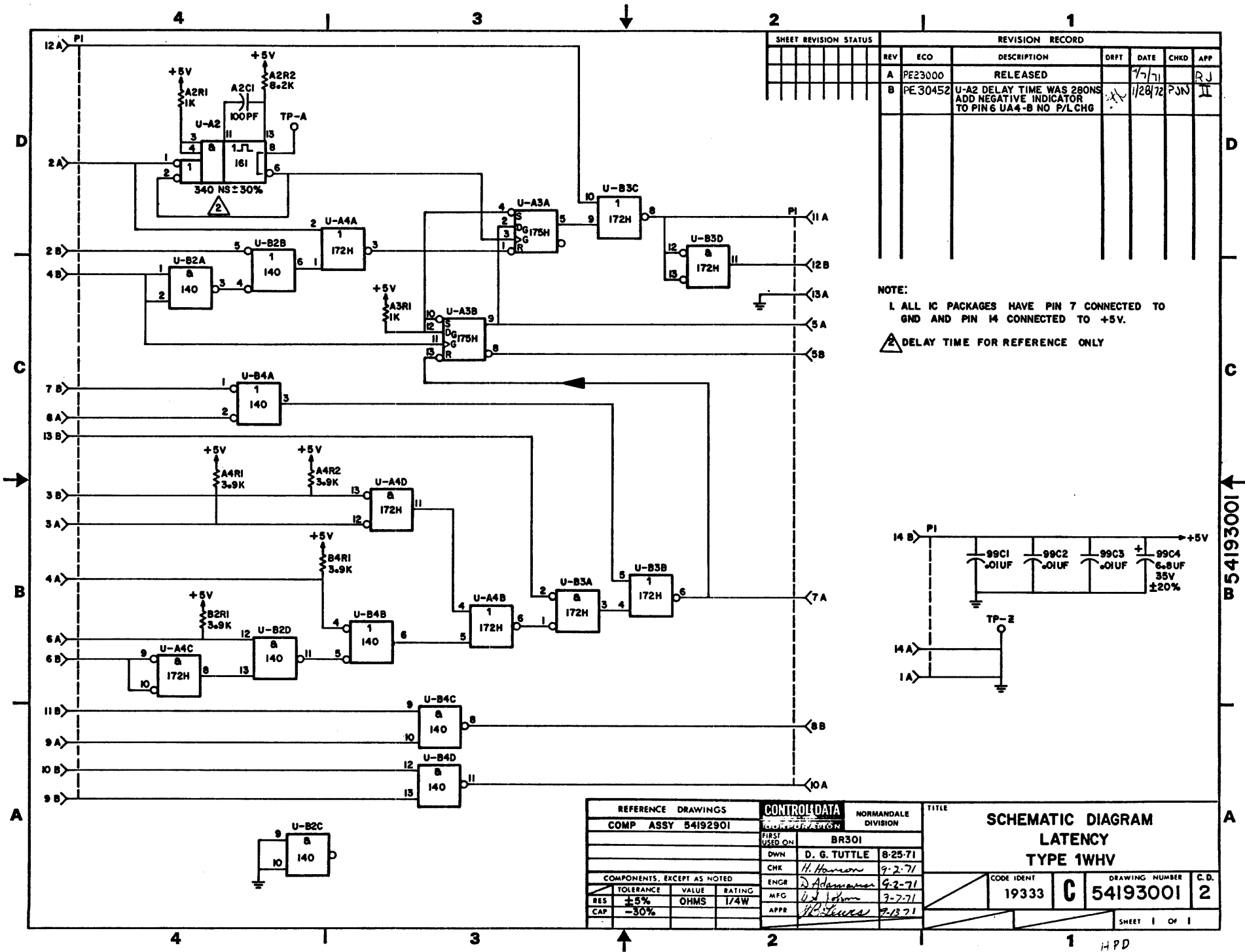
NOTE:
 1. UNLESS OTHERWISE SPECIFIED:
 ALL DIODES, GERMANIUM, 11801100
 ALL IC'S HAVE PIN 7 CONNECTED
 TO GND AND PIN 14 TO +5V
 ⚠ DELAY TIME FOR REF ONLY.



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY: 54192502		FIRST USED ON		BRIAIE		SCHEMATIC DIAGRAM	
		DWN		6-21-72		UNIT RESERVE	
		ENGR		6-23-72		TYPE 2WGV	
COMPONENTS, EXCEPT AS NOTED		MFG		1/23/72		CODE IDENT	
TOLERANCE		VALUE		RATING		DRAWING NUMBER	
RES ±5%	OHMS	1/4 W		APPR		19333 C 54192602 8	
CAP -50%						SHEET 1 OF 1	

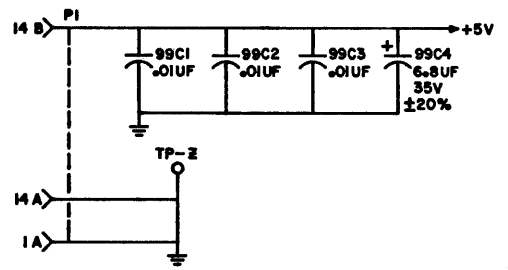
4-220

70629100 E



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PE23000	RELEASED		7-7-71		RJ	
B	PE30452	U-A2 DELAY TIME WAS 280NS ADD NEGATIVE INDICATOR TO PIN 6 UA4-B NO P/LCHG		1/28/72	PJN	II	

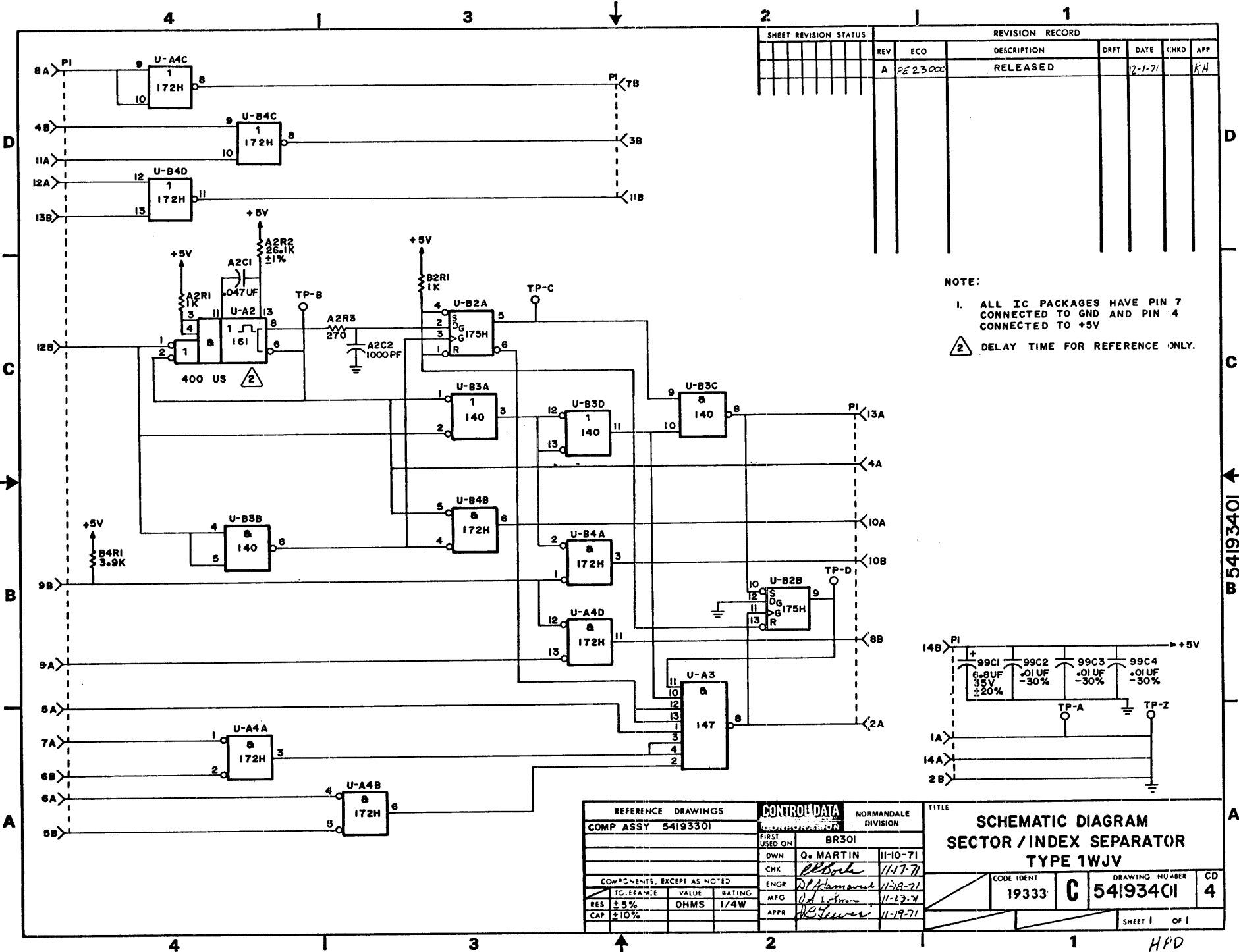
NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIME FOR REFERENCE ONLY



REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54192901		FIRST USED ON		BR301		SCHEMATIC DIAGRAM	
		DWN		D. G. TUTTLE		LATENCY	
		CHK		H. Hansen		TYPE 1WHV	
		ENGR		D. Adelman		CODE IDENT	
		MFG		J. J. Johnson		DRAWING NUMBER	
		APPR		W. Steiner		C. D.	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES		±5%		OHMS		1/4W	
CAP		-30%					
		CODE IDENT		DRAWING NUMBER		C. D.	
		19333		C 54193001		2	
		SHEET 1 OF 1		HPD			

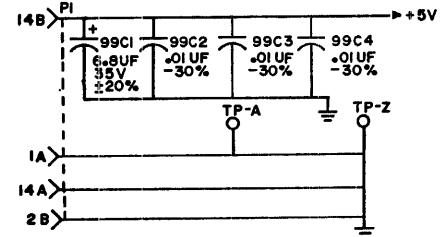
70629100 E

4-221



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	ORFT	DATE	CHKD	APP	
A	PE 23000	RELEASED		12-1-71		KH	

NOTE:
 1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V
 2. DELAY TIME FOR REFERENCE ONLY.



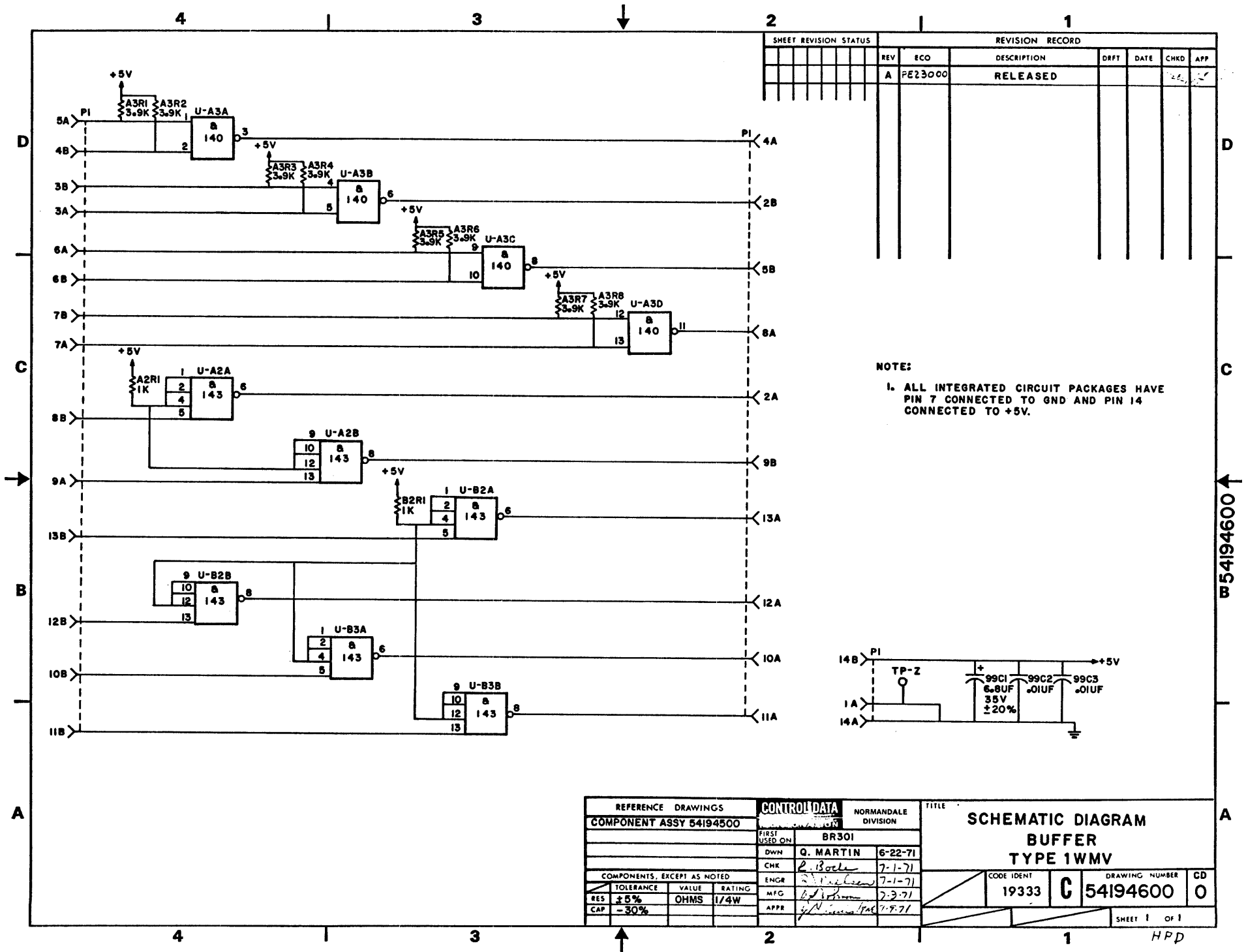
REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION	
COMP ASSY 54193301			FIRST USED ON	BR301		
			OWN	Q. MARTIN 11-10-71		
			CHK	<i>[Signature]</i> 11-17-71		
			ENGR	<i>[Signature]</i> 11-18-71		
			MFG	<i>[Signature]</i> 11-19-71		
			APPR	<i>[Signature]</i> 11-19-71		
COMPONENTS, EXCEPT AS NOTED						
TC. TOLERANCE	VALUE	RATING				
RES ±5%		OHMS 1/4W				
CAP ±10%						

TITLE			
SCHEMATIC DIAGRAM			
SECTOR / INDEX SEPARATOR			
TYPE 1WJV			
CODE IDENT	DRAWING NUMBER	CD	
19333	C 54193401	4	
SHEET 1 OF 1			

HPD

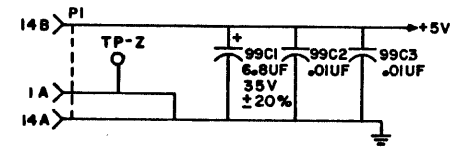
4-222

70629100 F



SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	REV	ECO	DESCRIPTION
A	FE23000	RELEASED							

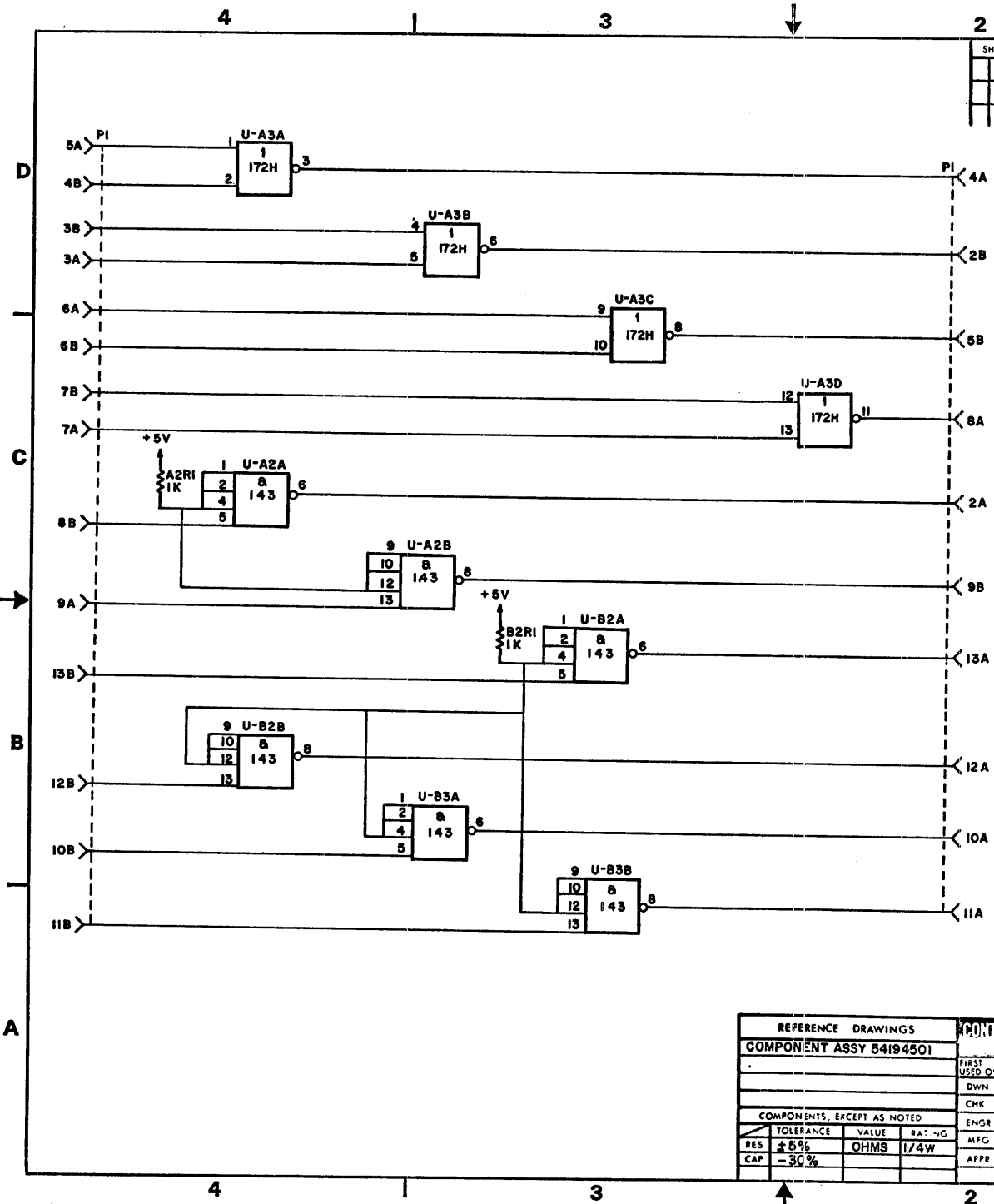
NOTE:
 1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



REFERENCE DRAWINGS				CONTROL DATA		NORMANDEALE DIVISION		TITLE		
COMPONENT ASSY 54194500				BR301				SCHEMATIC DIAGRAM		
FIRST USED ON				DWN		Q. MARTIN		6-22-71		
COMPONENTS, EXCEPT AS NOTED				CHK		P. BOEL		7-1-71		
ENGR				MFG		MFG		7-2-71		
APPR				APPR		M. J. ...		7-9-71		
RES	TOLERANCE	VALUE	RATING					CODE IDENT	DRAWING NUMBER	CD
	±5%	OHMS	1/4W					19333	C 54194600	0
CAP	-30%							SHEET 1 OF 1		
								HPD		

70629100 E

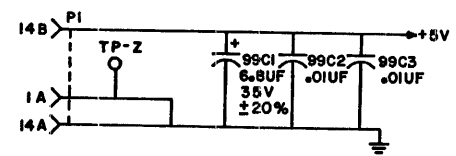
4-223



SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A	PR 23.000	RELEASED		11/1/71		RH	

NOTE:

1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.



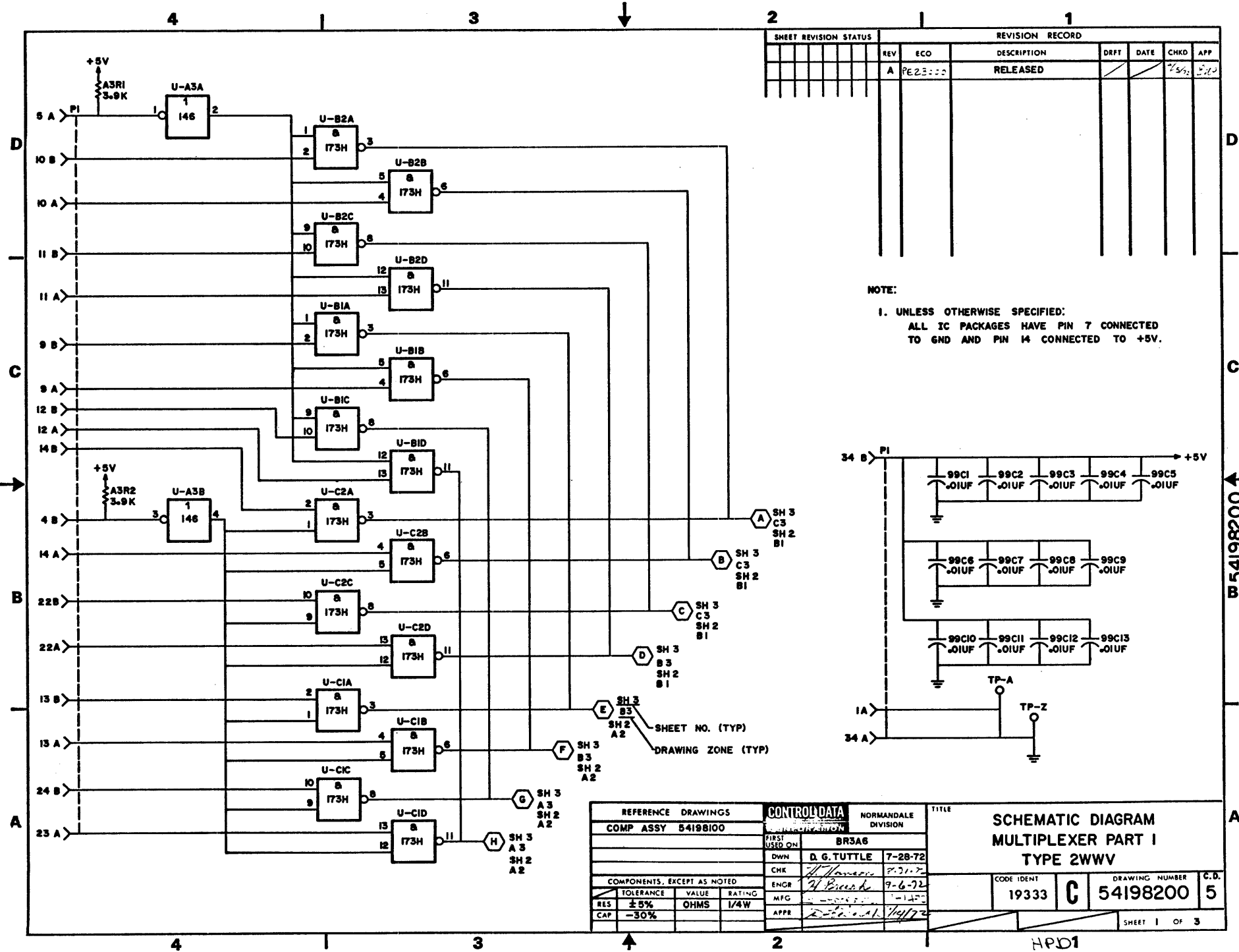
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54194501		BR 301				SCHEMATIC DIAGRAM	
		FIRST USED ON		11-1-71		BUFFER	
		DWN		R. BOCHE		TYPE AWMW	
		CHK		H. Hanson 11-2-71		DRAWING NUMBER	
COMPONENTS, EXCEPT AS NOTED		ENGR		J. J. J. 11-3-71		CD	
TOLERANCE	VALUE	RAT. %			CODE IDENT		
RES ±5%	OHMS	1/4W	MFG		19333		
CAP -30%			APPR		C		
				MFG		54194601	
				11-12-71		8	
				11-4-71		SHEET 1 OF 1	

HPD

W 54194601

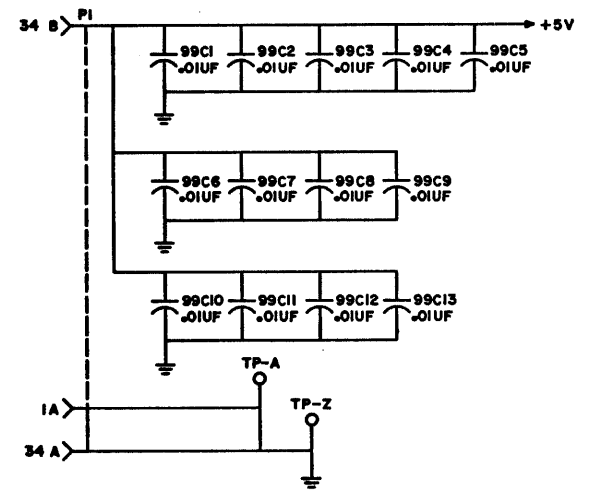
4-224

70629100 E



SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	REV	ECO	DESCRIPTION
A	PE23000	RELEASED							

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
ALL IC PACKAGES HAVE PIN 7 CONNECTED
TO GND AND PIN 14 CONNECTED TO +5V.



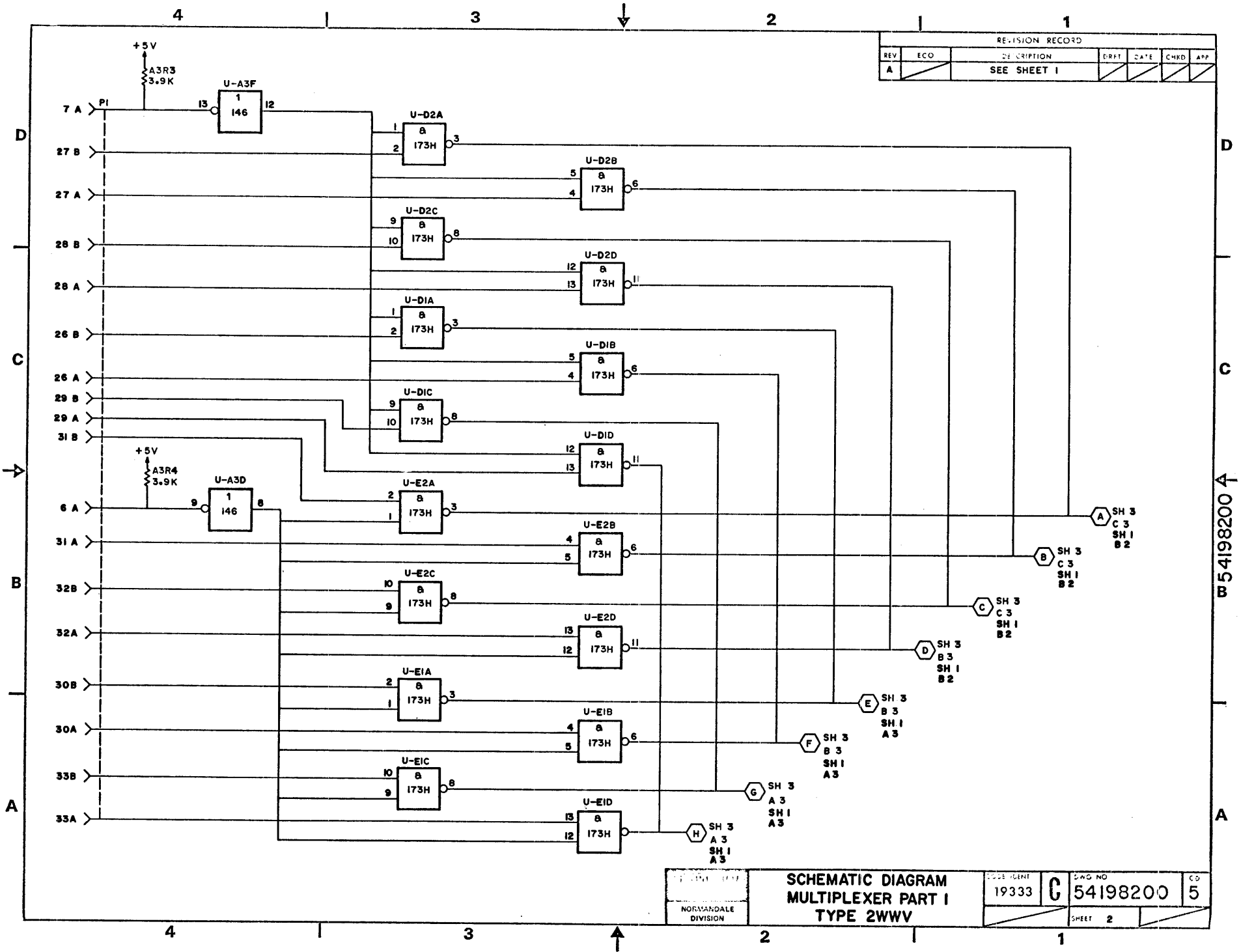
REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54198100			BR3A6				SCHEMATIC DIAGRAM MULTIPLEXER PART I TYPE 2WWV	
COMPONENTS, EXCEPT AS NOTED			FIRST USED ON		DWN		D. G. TUTTLE 7-28-72	
TOLERANCE			VALUE		RATING		ENGR	
RES ±5%			OHMS		1/4W		7-6-72	
CAP -30%							MFG	
							APPR	
							C.D.	
							DRAWING NUMBER	
							19333 C 54198200 5	
							SHEET 1 OF 3	

HPD1

70629100 F

4-225

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



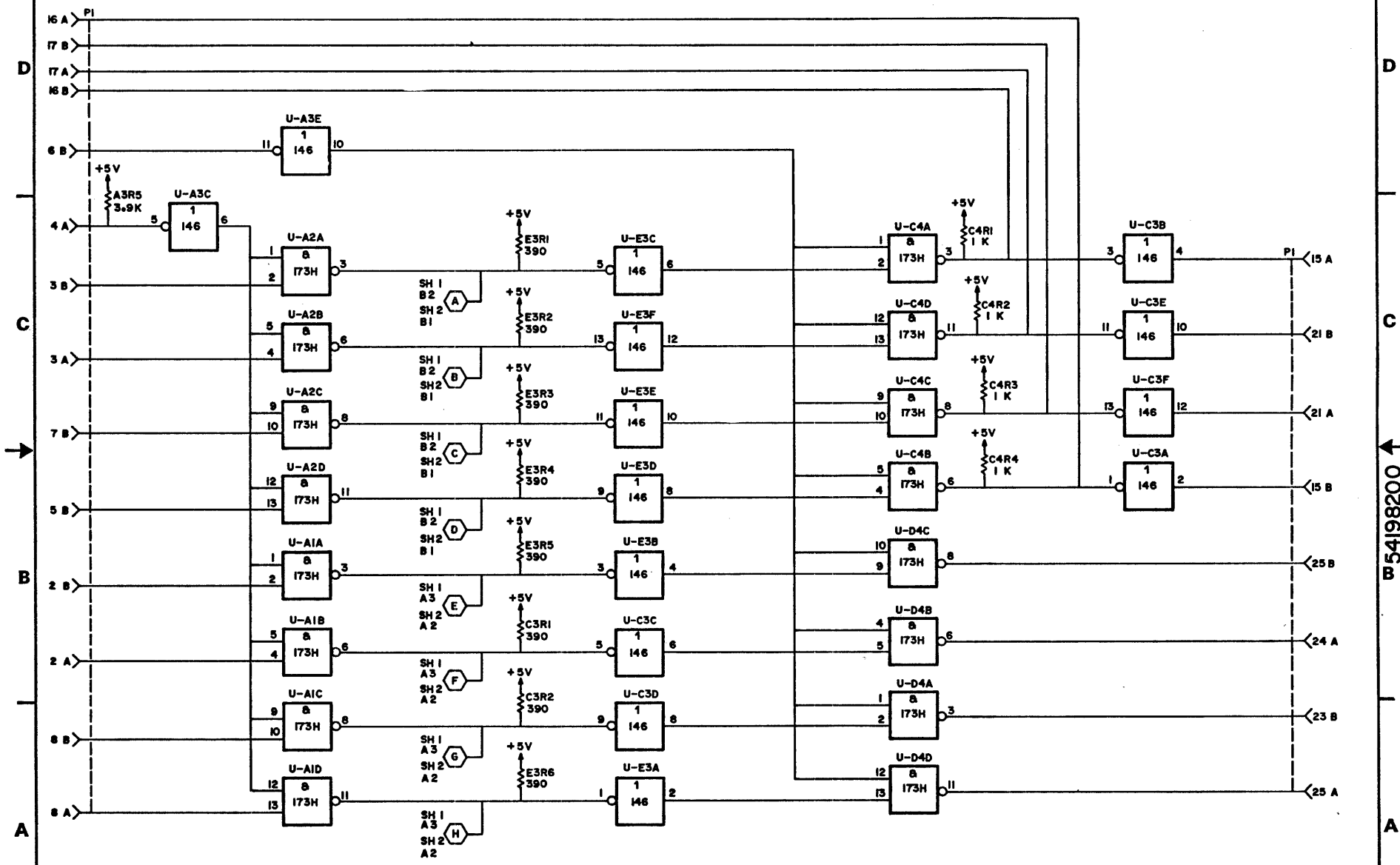
NORMANDEALE DIVISION	SCHEMATIC DIAGRAM MULTIPLEXER PART 1 TYPE 2WV		DATE 19333	REV C	DWG NO 54198200	CD 5
			SHEET 2			

W 54198200 A

4-226

70629100 E

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		SEE SHEET 1				



CONTROL DATA
NORMANDEALE
DIVISION

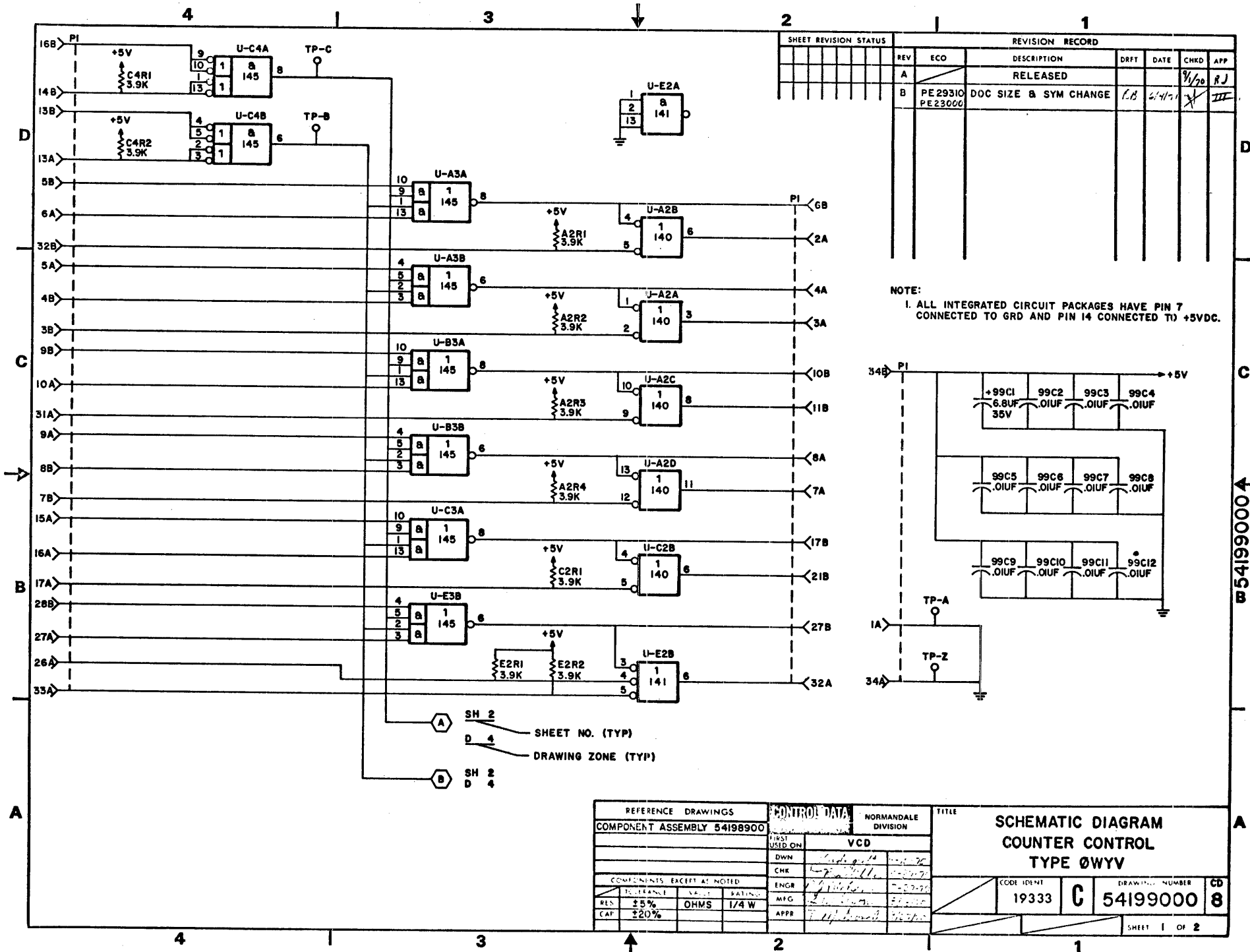
SCHEMATIC DIAGRAM
MULTIPLEXER PART I
TYPE 2WWV

CODE IDENT 19333	DWG NO 54198200	CD 5
SHEET 3		

54198200

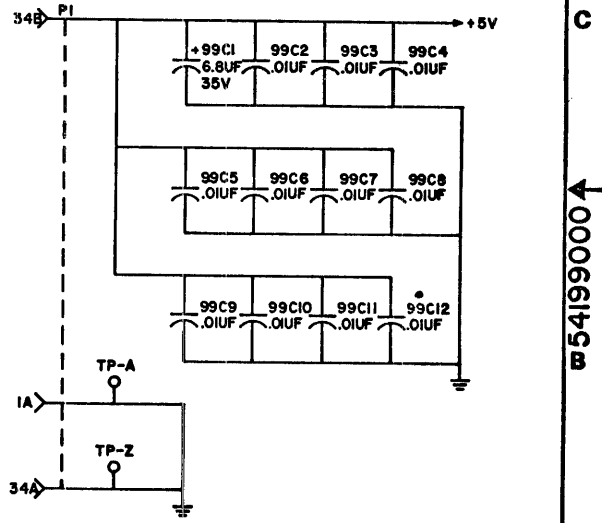
70629100 E

4-227



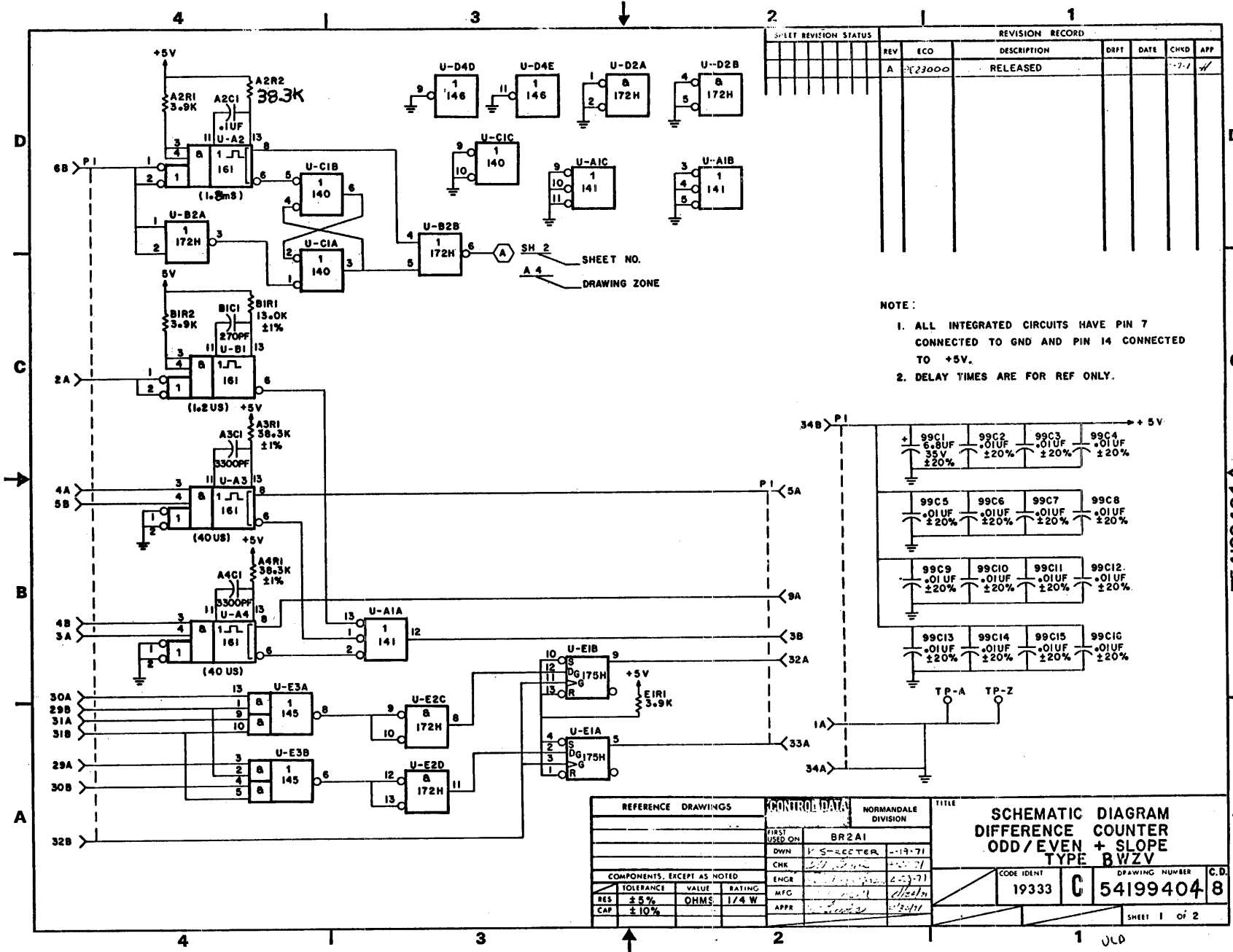
SHEET REVISION STATUS		REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
A		RELEASED					
B	PE 29310 PE 23000	DOC SIZE & SYM CHANGE	L.B	2/11/71		RJ III	

NOTE:
1. ALL INTEGRATED CIRCUIT PACKAGES HAVE PIN 7 CONNECTED TO GRD AND PIN 14 CONNECTED TO +5VDC.



A SH 2 SHEET NO. (TYP)
 D 4 DRAWING ZONE (TYP)
 B SH 2
 D 4

REFERENCE DRAWINGS				CONTROL DATA		NORMANDELE DIVISION		TITLE			
COMPONENT ASSEMBLY 54198900				VCD				SCHEMATIC DIAGRAM COUNTER CONTROL TYPE 0WV			
COMPONENTS EXCEPT AS NOTED				FIRST USED ON		DWN		CHK		ENGR	
RES	TOLERANCE	VAL	RATING	MFG	APPR	CODE IDENT	DRAWING NUMBER	CD			
RES	±5%	OHMS	1/4 W			19333	C 54199000	8			
CAP	±20%								SHEET 1 OF 2		



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DFT	DATE	CHKD	APP
A	23000	RELEASED				

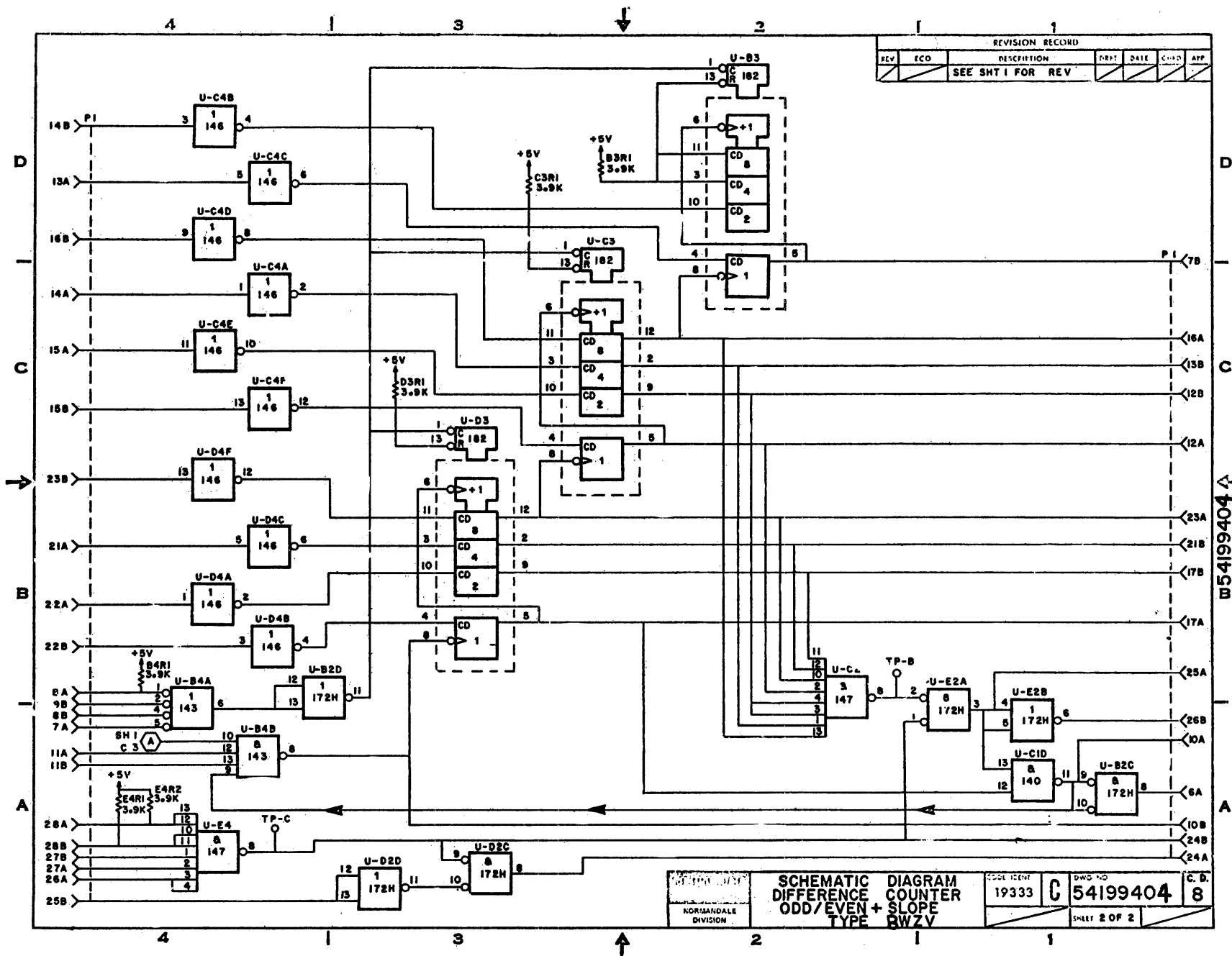
NOTE:
 1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIMES ARE FOR REF ONLY.

REFERENCE DRAWINGS			CONTROL DATA		NORMANDALE DIVISION		TITLE			
			FIRST USED ON	BR 2 A1		SCHEMATIC DIAGRAM DIFFERENCE COUNTER ODD/EVEN + SLOPE TYPE BWZV			C.D.	
			DWN	V S-SECTER --19-71						
			CHK	2/2/71						
COMPONENTS, EXCEPT AS NOTED			ENGR	2-23-71		CODE IDENT	DRAWING NUMBER	C.D.		
TOLERANCE	VALUE	RATING	MFG	2/2/71		19333	C	54199404	8	
RES ± 5%	OHMS	1/4 W	APPR	2/2/71						
CAP ± 10%							SHEET 1 OF 2			

54199404

4-230

70629100 E



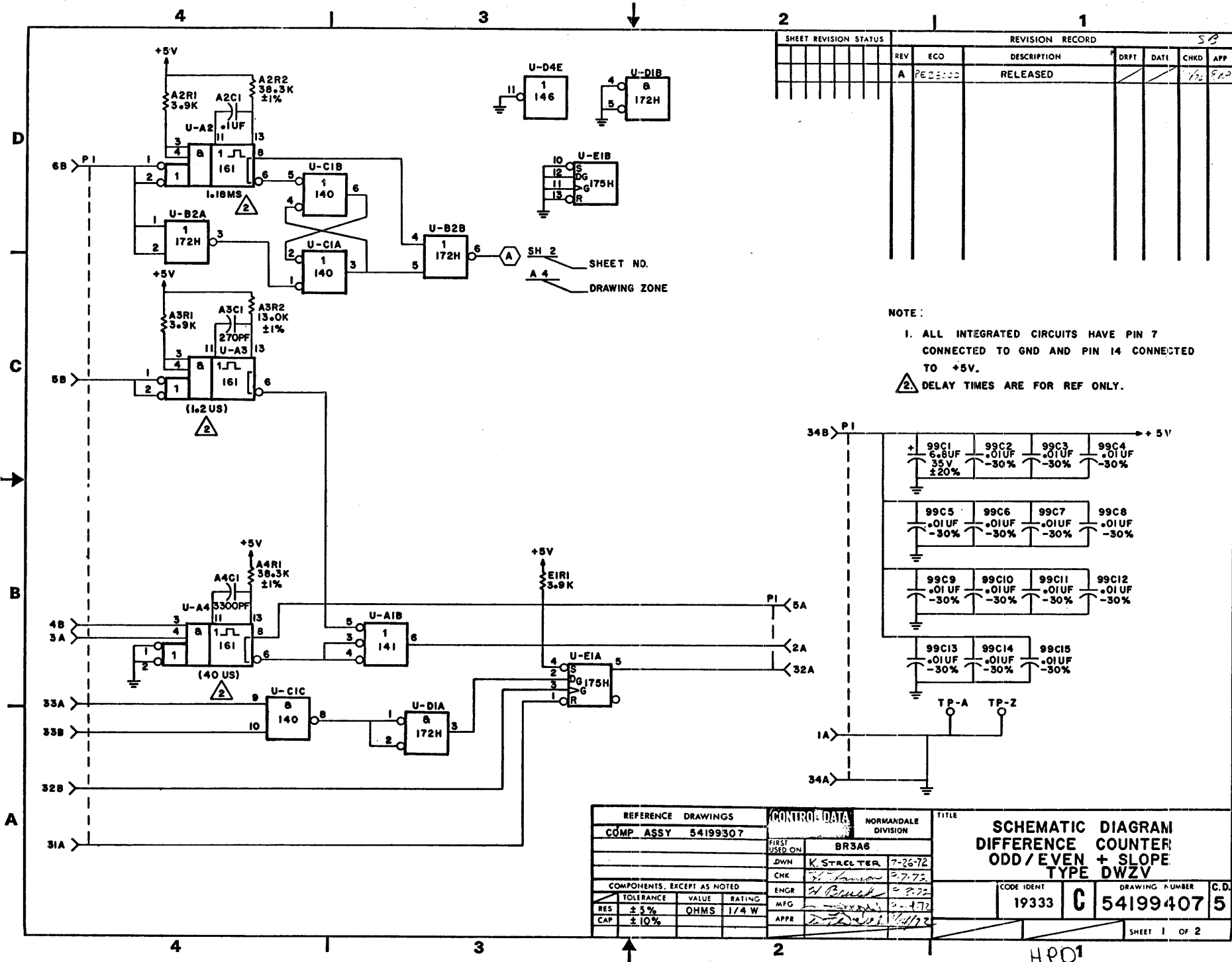
REVISION RECORD						
REV	ECO	DESCRIPTION	DRS	DATE	CHKD	APP
		SEE SHT 1 FOR REV				

NORMANDE DIVISION	SCHEMATIC DIAGRAM DIFFERENCE COUNTER ODD/EVEN + SLOPE TYPE RWZV	19333	C	54199404	C. B. 8

W54199404

70629100 E

4-231



SHEET REVISION STATUS		REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	PE25000	RELEASED			1/2	SPD

NOTE:
 1. ALL INTEGRATED CIRCUITS HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
 2. DELAY TIMES ARE FOR REF ONLY.

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMP ASSY 54199307		FIRST USED ON		BR3A6		SCHEMATIC DIAGRAM	
		DWN		K. STREETER		7-26-72	
		CHK		S. J. ...		2-7-73	
		ENGR		H. ...		2-7-73	
		MFG		...		2-1-72	
		APPR		...		4/1/72	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		RATING	
RES	± 5%	OHMS	1/4 W				
CAP	± 10%						
CODE IDENT		DRAWING NUMBER		C.D.			
19333		G 54199407		5			
SHEET 1 OF 2							

HPD1

W54199407

COMMENT SHEET

PLEASE COMPLETE ITEMS 1 THRU 11

From

(1) NAME
(2) DEPARTMENT OR ATTENTION OF
(3) STREET ADDRESS
(4) CITY AND STATE

Manual Information

(From Revision Record)

(5) MANUAL TITLE	
(6) PUBLICATION NO.	(7) REVISION
(8) FCO'S INCORPORATED INTO MANUAL	

Equipment Information

(From Equipment Nameplate & FCO Log)

(9) EQUIPMENT NO. AND DESCRIPTION
(10) SERIES CODE
(11) FCO'S INCORPORATED INTO EQUIPMENT

Comments

Large empty box for handwritten comments.

This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made above. Please include references to figure number, assembly number and design configuration level.

CUT ALONG LINE

MR 0902 PRINTED IN U.S.A.

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE

STAPLE

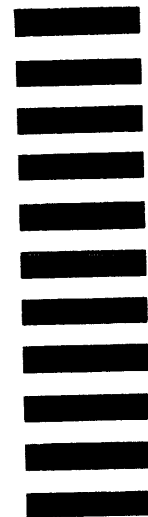
FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241
MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY
CONTROL DATA CORPORATION
Technical Publications Department
7801 Computer Avenue
Minneapolis MN 55435



CUT ALONG LINE

FOLD

FOLD

CONTROL DATA
CORPORATION

CORPORATE HEADQUARTERS, 8100 34th AVE. SO., MINNEAPOLIS, MINN. 55440
SALES OFFICES AND SERVICE CENTERS IN MAJOR CITIES THROUGHOUT THE WORLD

PRINTED IN U.S.A.