CONTROL DATA CORPORATION

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INTERFACE SPECIFICATION
FOR
LARK MODULE DRIVE
MODEL 9455

MAGNETIC PERIPHERALS INC.
a subsidiary of CONTROL DATA CORPORATION

INTERFACE SPECIFICATION FOR LMD (LARK) DRIVE

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INTERFACE SPECIFICATION FOR LMD (LARK) DRIVE

1.0 SCOPE

This document is an Engineering Specification which describes the interface requirements of the Magnetic Peripherals, Inc. LMD disk drive. For specific product characteristics see Table 1-1; for additional product detail reference LMD product specifications.

2.0 APPLICABLE DOCUMENTS

77641922 - Product Specification Lark Module Drive (LMD)
DR #9455 - Lark Module Drive Design Requirements
STD 1.41.104 - Engineering Standard

3.0 GENERAL DESCRIPTION

The LMD interface consists of a two cable arrangement composed of an "A" and a "B" cable. Figure 4.0-1 illustrates the system cabling configurations which are allowed.

The Interface for the LMD uses compatible SMD, CMD line drivers and receivers. All Interface lines carry the same definition and timing conditions where commonality can be achieved. Some Interface lines have different timing requirements because of the basic product characteristics.

See Engineering Standard STD 1.41.104 for definitions of logic terms and schematic drawing symbols used in this specification.

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TABLE 1-1. PRODUCT CHARACTERISTICS

MODEL TYPE	PRODUCT TYPE	NUMBER HEADS	TRANSFER RATE	BYTES/ TRACK	BYTES/ CYLINDER	BYTES/ SPINDLE	CYLINDER/ DEVICE	FIXED HEAD CAPACITY	FIXED MEDIA CAPACITY	REMOV-ABLE MEDIA	ROTATIONAL SPEED (RPM)
9760/62	SMD	5 DATA 1 SERVO	9.677 MHz	20 160	100 800	41 428 800/ 82 958 400	411/823	NONE	NONE	ALL	3600
9764/66	SMD	19 DATA 1 SERVO	9.677 MHz	20 160	383 040	157 429 440/ 315 241 920	411/823	NONE	NONE	ALL	3600
9730-12/ 9730-24	MMD	2/4 DATA 1 SERVO	9.677 MHz	20 160	40 320/ 80 640	12 902 400/ 25 804 800	320	NONE	ALL	NONE	3600
9730-12F/ 9730-24F	MMD	2/4 DATA 48 FIXED 1 SERVO	9.677 MHz	20 160	40 320/ 80 640+ FIXED HDS	12 902 400/ 25 804 800 PLUS 48 FIXED HEADS	320 + 12 FIXED HD	967 680	ALL	NONE	3600
9730-80	MMD	10 DATA 1 SERVO	9.677 MHz	20 160	100 800	82 958 400	823	NONE	ALL	NONE	3600
9730-80F	MMD	10 DATA 1 SERVO 48 OR 96 FIXED	9.677 MHz	20 160	100 800 + FIXED HEADS	82 958 400 PLUS 48 OR 96 FIXED HEADS	823 + (1) 10/20 (2) FIXED HDS	967 680/ 1 935 360	ALL	NONE	3600
9448-32	CMD	2 DATA 2 SERVO	9.677 MHz	20 160	40 320	32 578 560	823	NONE	16MB	16MB	3600
9448-64	CMD	4 DATA 2 SERVO	9.677 MHz	20 160	80 640	65 157 120	823	NONE	48MB	16MB	3600
9448-96	CMD	6 DATA 2 SERVO	9.677 MHz	20 160	120 960	97 735 680	823	NONE	80MB	16MB	3600
9455	LMD	4 DATA	9.677 MHz	20 672	82 688	17 033 728	206	NONE	8.5MB	8.5MB	3510

(1) 0.96 MB FHT OPTION HAS 3 HEADS IN LAST CYLINDER

(2) 1.92 MB FHT OPTION HAS 1 HEAD IN LAST CYLINDER

THE DATA CAPACITY SPECIFIED IS BASED ON THE NUMBER OF EIGHT-BIT BYTES THAT ARE RECORDED ON A TRACK. THE UNSECTORED AND UNFORMATTED CAPACITY DOES NOT INCLUDE AN ALLOWANCE FOR INTERFIELD GAPS.

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4.0 ACCESSORIES

Accessory items required, but not furnished with the device, are shown in Tables 4-1 and 4-2.

TABLE 4-1. CABLES* AND TERMINATORS

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO.
"A" Cable (Controller to Device)	One per Device in star, one per multi-spindle installation in Daisy Chain.	2	775642XX
"A" Cable (Device to Device)	One less than total devices in the Daisy Chain.	1,2	775642XX
"B" Cable (Controller to Device)	One per Device		775643XX
Terminator	One per Device in star, one per multi-spindle installation in Daisy Chain.		75886100-9

1. The number of cables required depends on number of units in daisy chain. (Refer to Figure 4.0-1)
2. Last two digits denote length. (For cable length see Table 4-2)

The above accessories are required but not included with the units; they must be purchased separately.

TABLE 4-2. I/O CABLE LENGTH AND TABS

	PART NUMBER TAB									
CABLE LENGTH IN FEET	5	6	8	10	15	20	25	30	40	50
"A" CABLE 775642XX	00	01	02	03	04	05	06	07	08	09
"B" CABLE 775643XX	00	01	02	03	04	05	06	07	08	09

NOTE*

A Lark drive consists of a Power and Input/Output Module (PIO) plus a micromodule Drive (μmD) which contains the drive mechanisms. Refer to the Lark product specification for cabling requirements for these internal units.

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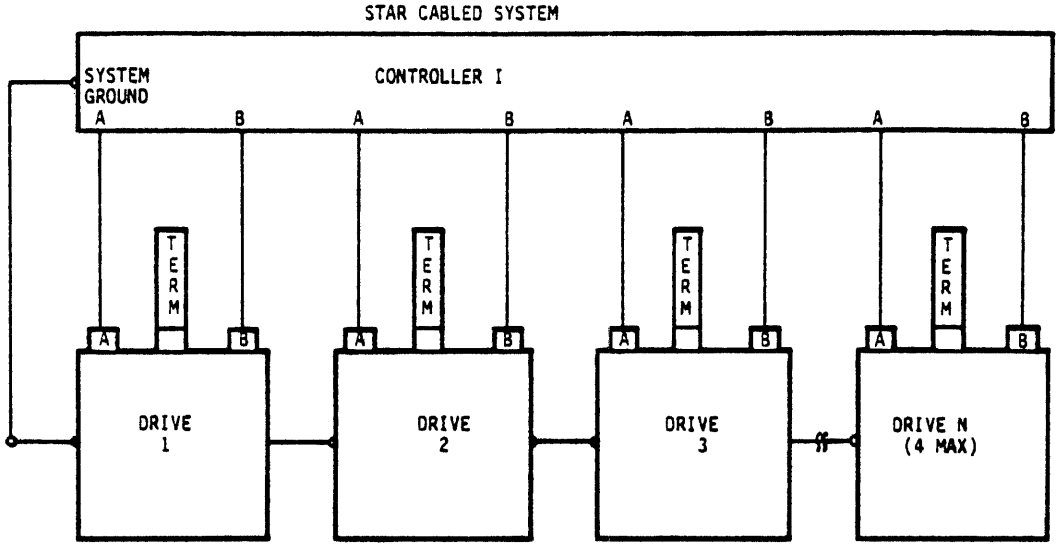
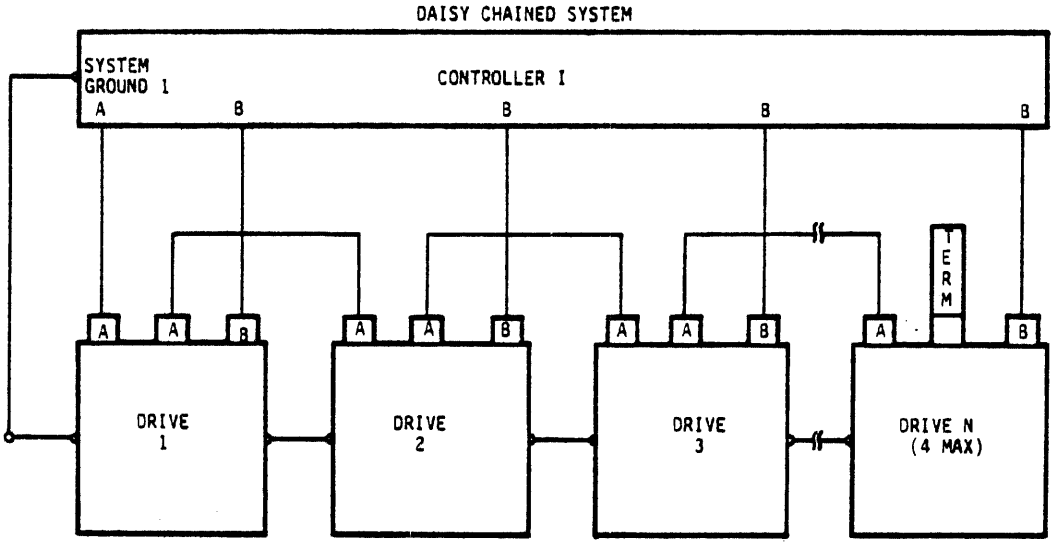


NOTES

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET



NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR.
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER CARDS.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET. MAXIMUM INIDIVIUAL B CABLE LENGTH = 50 FEET.

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Figure 4.0-1. Unit Cabling

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5.0 INTERFACE

5.1 INTERFACE DEFINITION

The Standard "A" cable I/O is a 60-conductor flat cable. The Standard "B" cable has 26 conductors.

All input and output signals are digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noise electrical environment.

The "A" cable is a twisted-pair, flat cable. The "B" cable is a ribbon flat-cable with ground plane and drain wire. Twisted-pair and/or ground plane shielding is utilized to minimize cross-talk and reduce inductive coupling due to discharges, as well as control impedance variations regardless of cable lay.

5.1.1 Terminated, Balanced Transmissions System

Transmitters and receivers of the industry standard types 75110A and 75108 or equivalent are used to provide a terminated, balanced transmission system (see Figures 5.1-1, 5.1-2 and 5.1-3).

5.1.2 Line Transmitter Characteristics

The device controller line transmitters (Figure 5.1-2) are compatible with the line receiver described in 5.1.3.

1. Output Signal Levels

   Control Signals - See Figure 5.1-2
   Data Signals - See Figure 5.1-1

2. Output Line Polarity

   The transmitters (Figure 5.1-2) are connected to the I/O lines such that the output, labeled "-", correspond with the low order pin number of the pin assignments and the output labeled "+", connects to the higher order pin number on the pin assignments (Figures 5.1-4 and 5.1-5), except for the Unit Selected line which is connected in the opposite manner. A logic 1 on the interface is defined when the "+" output is more positive than the "-" output (Figures 5.1-1 and 5.1-2).

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5.1.3 Input Amplifier (Receiver) Characteristics

The Device Controller input amplifier (Figure 5.1-3) is compatible with the transmitter described in 5.1.2.

1. Receiver Propagation Delay

   The receiver propagation delay is typically 17 ns in the direction of the logical 1, and 17 ns in the direction of the logical 0.

2. Receiver Input Polarity

   All receivers within the LMD are wired to interpret interface logic 1 (in True or active state) when the "+" line (wired to the higher numerical connector pin number) is more positive than the "-" line (wired to the lower numerical connector pin number). Refer to Figures 5.1-1 and 5.1-3 for voltage levels and Figures 5.1-4 and 5.1-5 for connector assignments.

5.1.4 Terminator

1. "A" Cable

   A terminator resistance as shown in Figures 5.1-2 and 5.1-3 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly which must be ordered separately.

   A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect line. See Paragraph 5.2.2-7. No termination resistance is used on the Power Sequence lines in the "A" cable.

2. "B" Cable

   A termination resistance as shown in Figure 5.1-1 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card for the receivers located within the drive.

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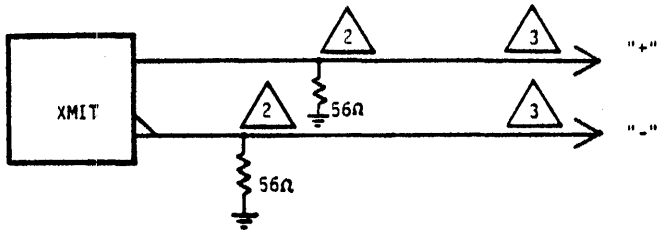


1. VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF 11 ± 3 mA, AND A 5% TERMINATING RESISTOR OF 56 OHMS.

2. TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS EXCEPT FOR THE OPEN CABLE DETECT DRIVER. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY.

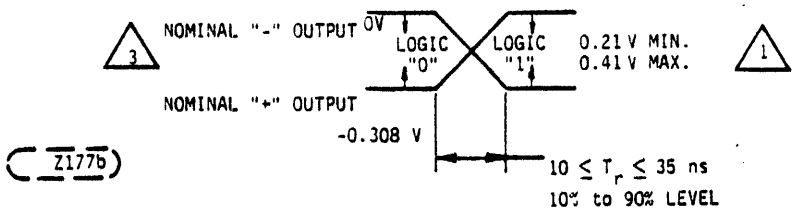
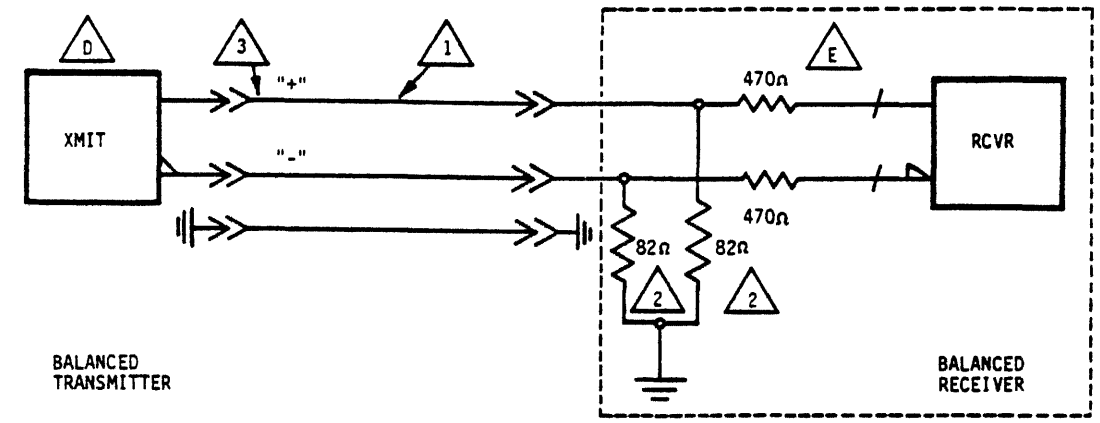


Figure 5.1-2. Control Line Transmitter



1. CABLE SHALL BE FLAT CABLE PER SECTION 5.1.5.3

2. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

3. NOMINAL "-" LINE 0V
   NOMINAL "+" LINE -0.175 V
   LOGIC 0 / LOGIC 1 { 1.21 V (MAX) / 0.623 V (MIN)
   $10 \leq T_r \leq 35$ ns, 10% to 90% LEVEL

D. DRIVER TYPE (REFER TO PARAGRAPH 5.1.1)

E. RECEIVER TYPE AND TERMINATION (REFER TO PARAGRAPH 5.1.1)

Figure 5.1-1. Typical Read/Write Data and Clock Transmitter and Receiver

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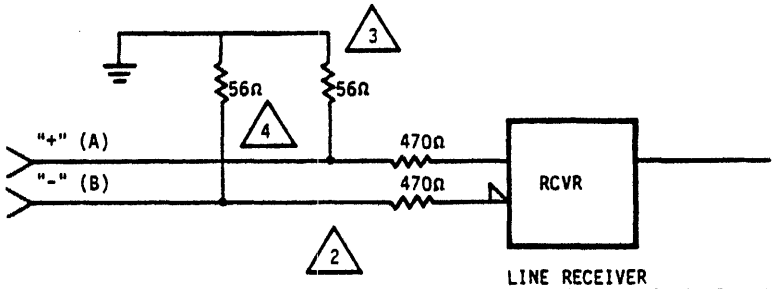
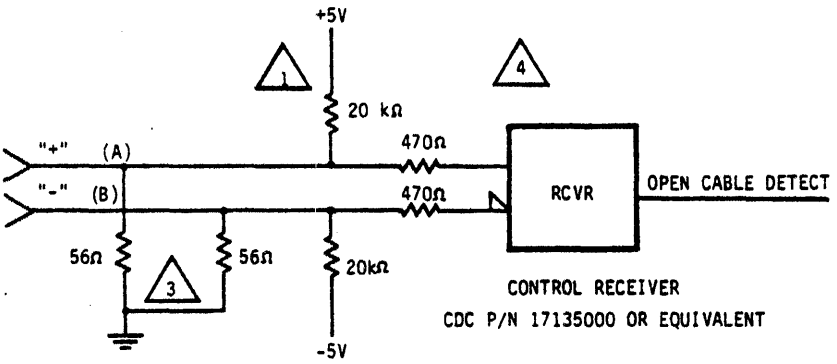


a) CONTROL LINE RECEIVER

LINE RECEIVER
CDC P/N 17185000 OR EQUIVALENT



CONTROL RECEIVER
CDC P/N 17135000 OR EQUIVALENT

b) OPEN CABLE DETECT RECEIVER

1. 20k OHM RESISTORS ARE TYPICAL VALUES
2. A BIAS NETWORK SHOULD BE USED TO PREVENT FALSE STATUS OR INTERRUPT CONDITIONS WHEN DRIVE POWER IS OFF AT CONTROLLER END OF UNIT SELECTED AND SEEK END SIGNALS.
3. TERMINATING RESISTORS ARE LOCATED:
   A. ON LOGIC CARD FOR "B" CABLE LINES.
   B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
4. SEE SECTION 5.2.2 FOR A DESCRIPTION OF THE OPEN CABLE DETECT SIGNAL

DIFFERENTIAL INPUTS	LOGIC OUTPUT
$V_A - V_B \geq 25mV$	"0"
$\lvert V_A - V_B \rvert < 25mV$	IND
$V_B - V_A \geq 25mV$	"1"

LINE RECEIVER TRUTH TABLE

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Figure 5.1-3. Control Line Receiver

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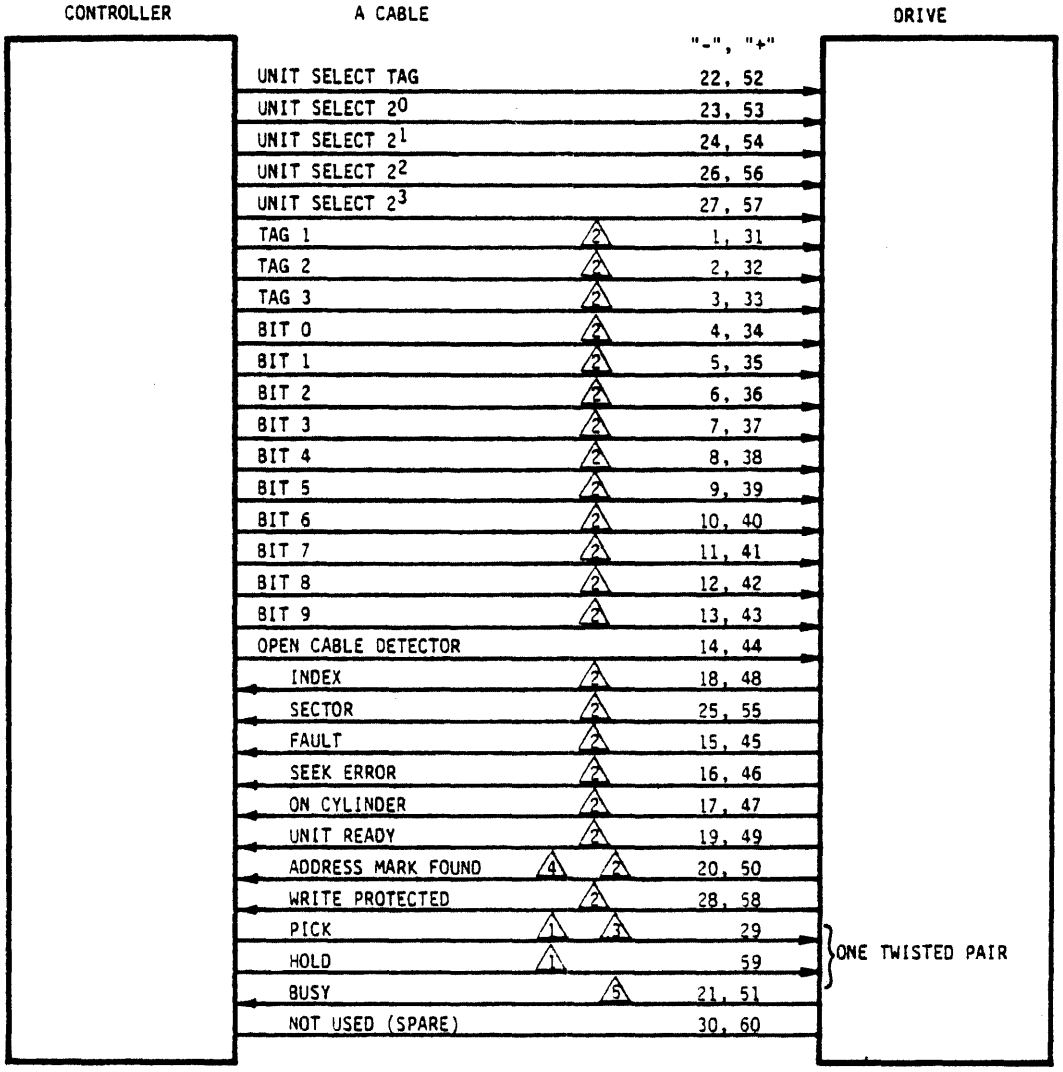

NOTE: 60 POSITION
30 TWISTED PAIR - STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT

1. SPECIAL SIGNAL, NOT A BALANCED TRANSMISSION SIGNAL
2. GATED BY UNIT SELECTED
3. NOT INTERPRETED, IS DAISY CHAINED, NO DRIVER CONNECTION WITHIN THE LMD.
4. NOT ACTIVATED, IS DAISY CHAINED, ALWAYS A LOGIC ZERO OUTPUT IF UNIT IS SELECTED
5. NOT GENERATED, IS DAISY CHAINED, NO DRIVER CONNECTION WITHIN THE LMD

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Figure 5.1-4. Tag Bus I/O Interface

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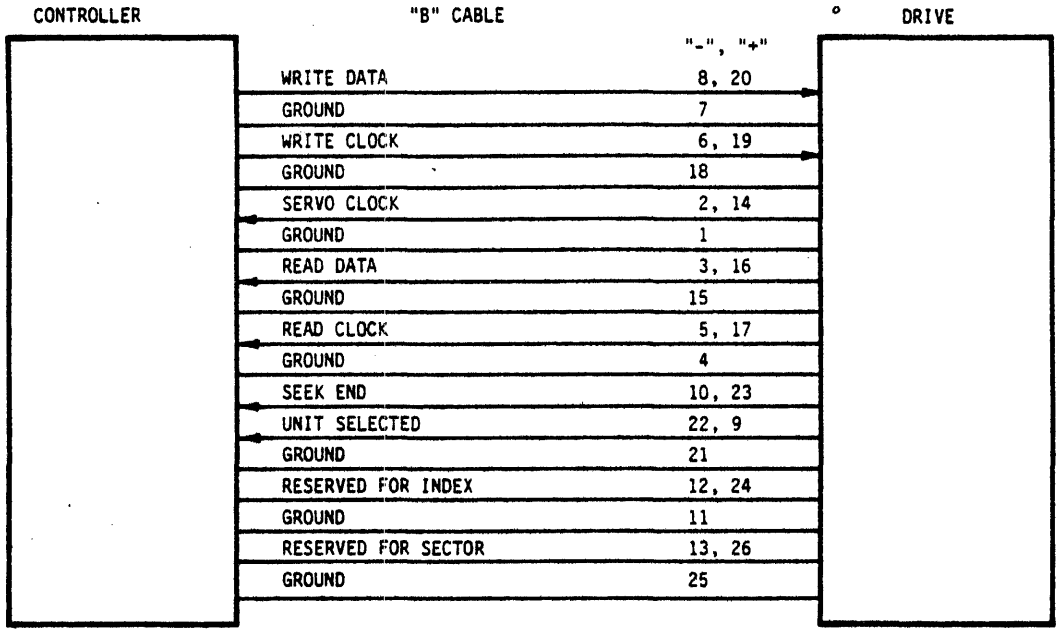

NOTES: 1. 26 CONDUCTOR FLAT CABLE.
MAXIMUM LENGTH - 50 FT.

2. NO SIGNALS GATED BY "A" CABLE UNIT SELECT.

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Figure 5.1-5. "B" Cable Interface

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5.1.5 I/O Cables (See Figure 5.1-6)

5.1.5.1 "A" Cable

DESCRIPTION	MPI P/N	BERG P/N	SPECTRA-STRIP P/N	ITEM*
Connector (60 Pos)	94361115	65043-007		1
Contact, Insert	94245603	48048	----------	3
Flat Cable (twisted-pair), 30 pair, 28 AWG	95043902		3CT-6028-7B-05-100	2

5.1.5.2 "A" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI P/N	3M P/N	ITEM*
60 pin, vertical header	91904653	3372-2302	4

5.1.5.3 "B" Cable

DESCRIPTION	MPI P/N	3M P/N	ITEM*
Connector (26 pos.)	65853402	3399-3000	5
Connector Pull Tab	92004801	3490-2	6
Flat Cable (26 pos.) with ground plane and drain wire.	95028509	3476-26	7

5.1.5.4 "B" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI P/N	BERG P/N	ITEM*
26 pin, vertical header	96752044	65610-126	8

5.1.6 I/O Cable Characteristics

"A" Cable

Type: 30 twisted pair, flat-cable
Twists per inch : 2
Impedance: 100 ± 10 ohms
Wire Size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft
Maximum cable length: 100 ft cumulative
Voltage Rating: 300 V rms

*REFER To Figure 5.1-6

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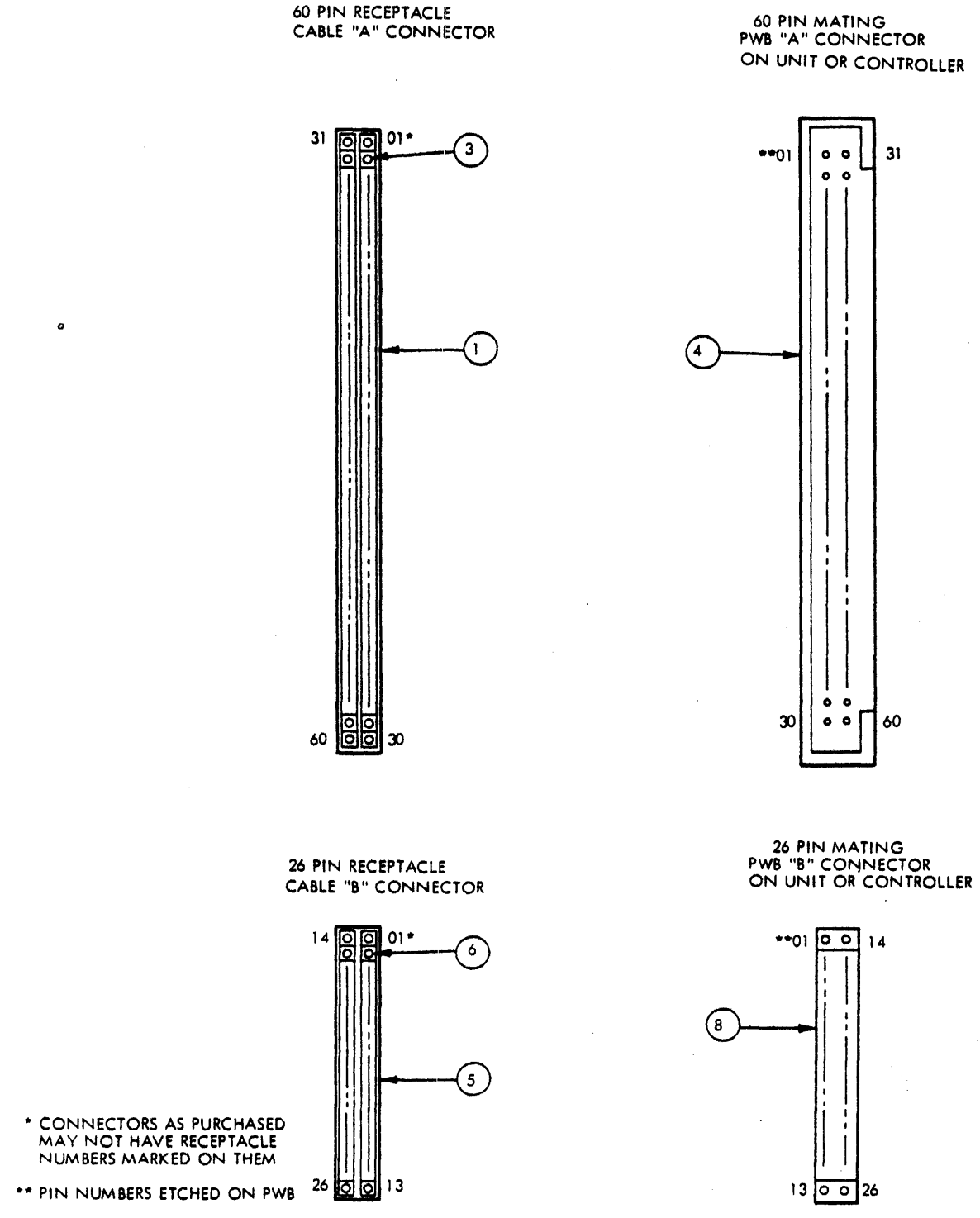

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Figure 5.1-6. I/O Connectors

5.1.6 I/O Cable Characteristics (cont'd)

"B" Cable (with ground plane)

Type: 26 conductor, flat cable with ground plane and drain wire
Impedance: 65 ohms (3M P/N 3476-26)
Wire size: No. 28 AWG, 7 strands
Propagation time: 1.5 to 1.8 ns/ft
Maximum cable length: 50 ft
Voltage Rating: 300 V rms

5.2 SIGNAL LINES

5.2.1 Address and Control Tag Functions (received by the unit)

Address and control functions are transferred on 10 bus lines (Bit 0 - Bit 9). The significance of the information on these lines is indicated by one of three tag lines (see Figures 5.1-4 and 5.2-1).

5.2.1.1 Cylinder Address (Tag 1)

Ten bus lines (Bit 0-Bit 9) are used to carry the cylinder address to the device. Since direct addressing is used, the controller need only place the new address on the Bus lines and strobe the Tag 1 line (see Figure 5.2-2). The seek operation will be initiated after the trailing edge of Tag 1 is received. On cylinder must be true, Seek Error must be false, and Fault must be false when Tag 1 is sent, otherwise the seek function will not be initiated.

With the LMD, if the Seek-On-Head-Change option is not selected, Tag 2 must precede Tag 1 when a head change is made. The correct head will be enabled during the seek operation after the trailing edge of Tag 1 (see Figure 5.2-2).

5.2.1.2 Head Select (Tag 2)

In the LMD, this tag signifies that head and volume address bits are on the Bus lines to the device (Figure 5.2-1). This command must be followed by a valid seek command since a head change is not executed until the next valid cylinder address code is received via a Tag 1 function. Read or write commands will result in a Fault status until after the seek has been executed.

BUS	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD/VOLUME SELECT	TAG 3 CONTROL SELECT
BIT 0	2^0	2^0 (1)	WRITE GATE
BIT 1	2^1	2^1 (1)	READ GATE
BIT 2	2^2	(2)	SERVO OFFSET PLUS
BIT 3	2^3	(2)	SERVO OFFSET MINUS
BIT 4	2^4	(2)	FAULT CLEAR
BIT 5	2^5	(2)	(2)
BIT 6	2^6	(2)	RTZ
BIT 7	2^7	(2)	DATA STROBE EARLY
BIT 8	2^8	(2)	DATA STROBE LATE
BIT 9	2^9	(2)	(2)

(1) HEAD CHANGES ARE NOT INITIATED UNTIL A VALID SEEK IS RECEIVED FOLLOWING A HEAD CHANGE COMMAND IF THE SEEK-ON-HEAD-CHANGE OPTION IS NOT SELECTED. IF THE SEEK-ON-HEAD-CHANGE OPTION IS SELECTED, THE HEAD CHANGES AND A ZERO DISTANCE SEEK WILL BE INITIATED AS A RESULT OF THE HEAD CHANGE.

(2) NOT INTERPRETED BY THE LMD.

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Figure 5.2-1. Tag Bus Decode

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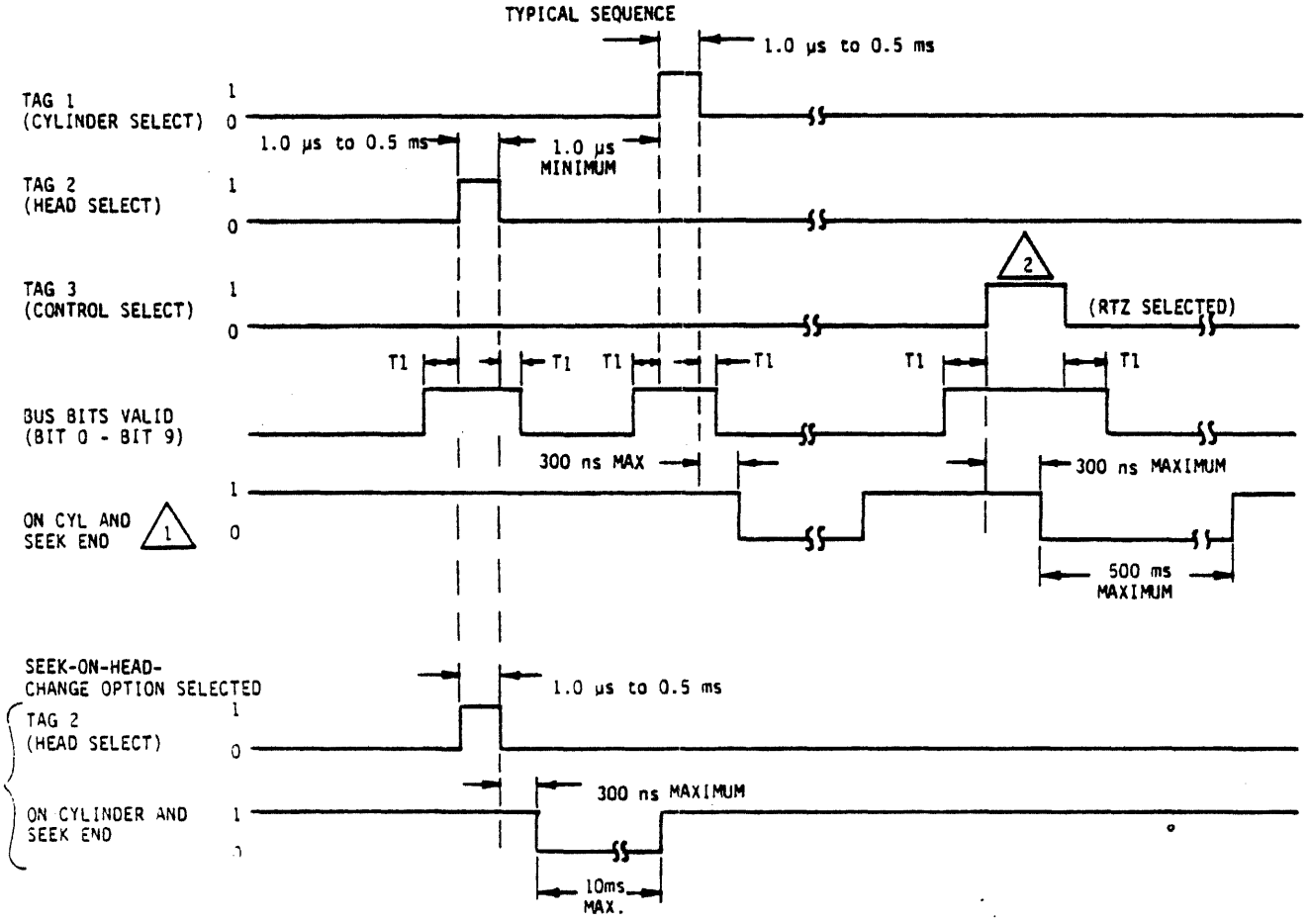

NOTES: T1 = 200 ns MINIMUM

1 SEEK-ON-HEAD-CHANGE OPTION NOT SELECTED.

2 RTZ MAY ALSO BE GENERATED WITH TAG 3 STABLE (TRUE) AND BY STROBING THE APPROPRIATE BUS BIT.

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Figure 5.2-2. Tag and Bus Timing

5.2.1.2 Head Select (Tag 2) (cont'd)

Note 1. Tag 2 must always be followed by Tag 1 (whether the head is different or the same).

Note 2. On Cylinder will not become False as a result of a head change command alone.

Note 3. Via a switch selectable Seek-On-Head-Change option within the LMD, a head select command will automatically initiate a head change and zero distance seek. "ON Cylinder" will go false for a maximum of 10 milliseconds. (Figure 5.2-2)

TABLE 5.2-1. TAG 2 BUS DECODE FOR LMD

HEAD NUMBER		SURFACE IDENTIFICATION
2^1	2^0	BUS BITS
0	0	Top - Cartridge Disk
0	1	Bottom - Cartridge Disk
1	0	Top - Fixed Disk
1	1	Bottom - Fixed Disk

5.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation with the Bus lines interpreted in the following manner:

1. Write Gate (Bit 0)

   The Write Gate line (Figures 5.1-4 and 5.2-1) enables the write driver. For typical Write Gate timing refer to Section 5.3.

2. Read Gate (Bit 1)

   Enabling of the Read Gate (Figure 5.2-1) enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on a PLO sync field. For typical Read Gate timing requirements refer to Section 5.3.

5.2.1.3 Control Select (Tag 3) (cont'd)

3. Servo Offset Plus

   This function is not executed by the LMD; however, On Cylinder will be deactivated for 2000* µs maximum from a logic change (i.e., 0 to 1 or 1 to 0) in this bit for Flat Cable Interface compatibility.

4. Servo Offset Minus

   This function is not executed by the LMD; however, On Cylinder will be deactivated for 2000* µs maximum from a logic change (i.e., 0 to 1 or 1 to 0) in this bit for Flat Cable Interface compatibility.

5. Fault Clear (Bit 4)

   A pulse, 300 ns minimum, sent to the device will deactivate to logic 0 the fault condition within 2000* µs measured from the leading edge of the Fault Clear pulse if the fault condition no longer exists.

6. (Bit 5)

   This bit not interpreted by the LMD.

7. RTZ (Bit 6)

   A pulse, 300 ns minimum, 1.0 ms maximum, sent to the device will cause the actuator to seek track 0, select head zero, select the cartridge volume and deactivate to logic 0 the Seek Error status.

   The RTZ function will be completed in 500 ms maximum. On Cylinder will be false during the RTZ function. (Figure 5.2-2)

8. Data Strobe Early (Bit 7)

   When this line is true, the Device PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

9. Data Strobe Late (Bit 8)

   When this line is true, the Device PLO Data Separtor will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line if false.

NOTE

The Data Strobe signals are intended to be an aid in recovering marginal data. The data strobe position returns to nominal when the respective signals go false. The Data Strobe signals are only applicable while reading data from the disk.

* This value subject to change at a later date.

5.2.1.3 Control Select (Tag 3) (cont'd)

10. (Bit 9)

This bit not interpreted by the LMD.

5.2.2 Individual Lines

The following individual lines are contained in the "A" cable (Figure 5.1-4).

1. Index

This signal occurs once per revolution and its leading edge is considered the sector pulse for sector zero; it is typically 1.25 μs (see Figure 5.2-3). Index pulses may be missed when the seek command for a head change is performed. The index timing will become valid when On Cylinder becomes true following the seek function. (Refer to Figure 5.2-4).

If a head switch occurs during an Index pulse, the pulse width is not affected.

2. Sector Mark

The Sector pulse (1.25 ±0.2 μs) is derived from the embedded servo information (see Figure 5.2-3). Sector pulse integrity is maintained throughout all seek operations in which no head change is effected. There are 63 sector pulses available per revolution. When combined with Index in the controller, this divides the tracks into 64 equal length sectors. An alternate sector count of 32 equal length sectors is available via a different device configuration (i.e., a different assembly number).

NOTE 1

All sector pulses will be generated during a seek which requires no head change.

NOTE 2

Some sector pulses will be omitted when a head change occurs (refer to Figure 5.2-4). If the controller counts Sector pulses to determine sector location, the controller should wait until the next Index pulse following the completion of a seek with head change to determine the rotational position of the disk. Sector pulse timing integrity is not guaranteed while ON Cylinder is false during a seek after a head change.

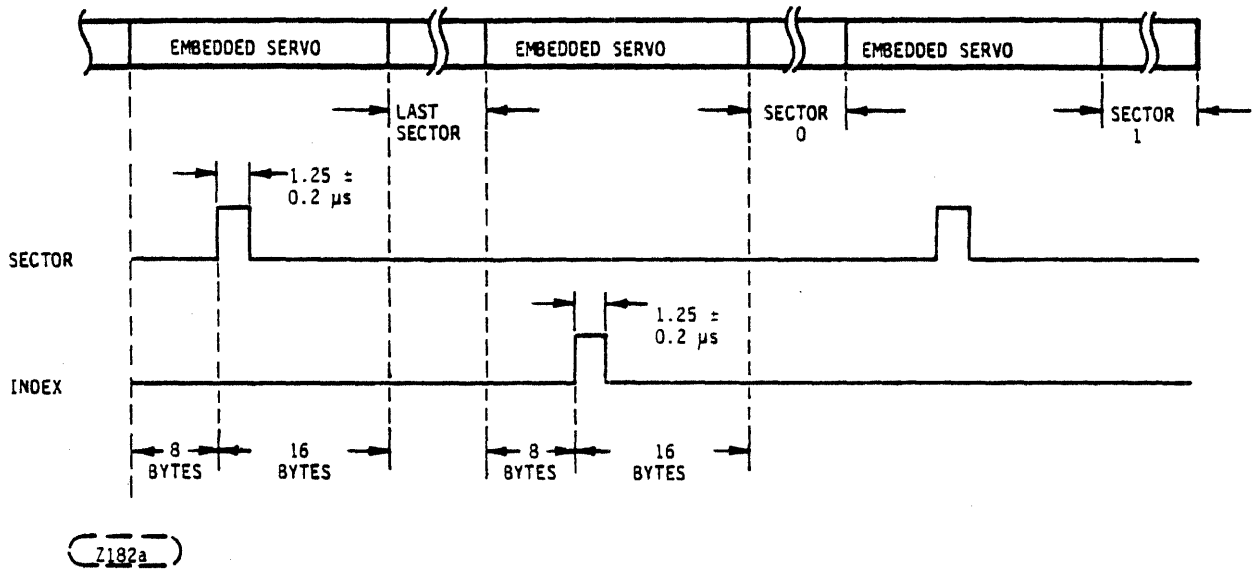

Figure 5.2-3. Relative Index and Sector Relationship

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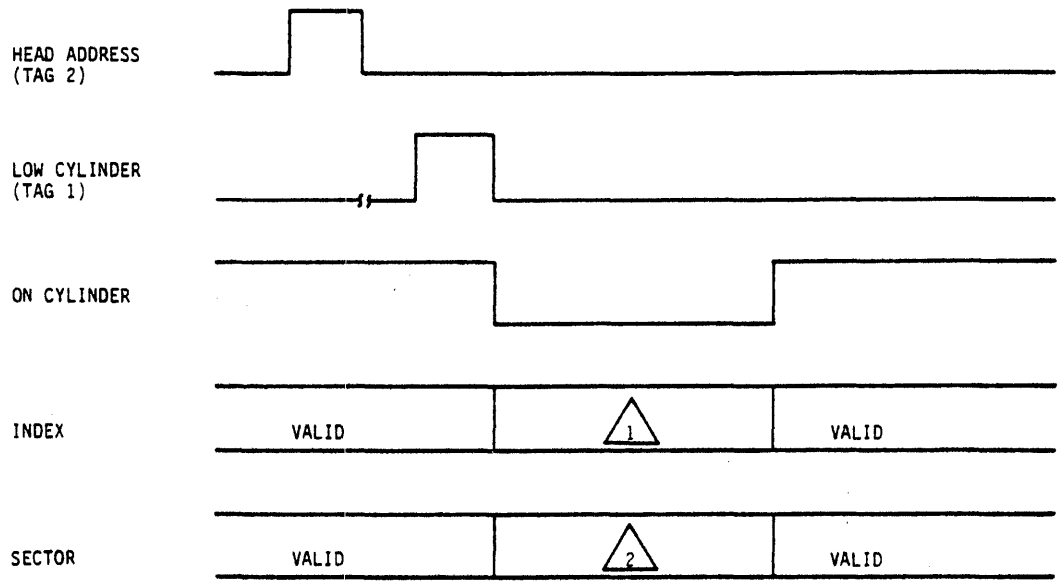

1 DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN INDEX PULSES ARE POSSIBLE.

2 DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN SECTOR PULSES ARE POSSIBLE.

NOTE: THE SERVO CLOCK TIMING INTEGRITY IS MAINTAINED DURING THE SEEK FUNCTION.

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Figure 5.2-4. Index and Sector Pulses During Seek

5.2.2 Individual Lines (cont'd)

3. Fault

When this line is true, a fault condition exists in the device. A fault condition will inhibit writing to prevent data destruction. This line will be deactivated within 2000* µs after activation of Fault Clear or by power sequencing the DC power to the unit (providing the fault no longer exists).

The fault conditions detected by the LMD may be grouped into the following four categoies:

A. Interface signal related faults

These types of faults indicate an attempted illegal operation by the interface controller. This type of fault may be generated by the detection of the interface Write Gate during a read operation, Write Gate or Read Gate while off cylinder, Write Gate and a write protected volume selected, Write or Read Gate after a head select and before a seek command, or Write Gate during the controller accessible section of a sector containing an unrecoverable embedded servo field.

NOTE

An LMD sector contains a drive interpreted embedded servo field followed by a controller accessible disk space for interface data storage/retrieval. The embedded servo field may not be read or written via the interface; however, a fault is not generated if the interface controller activates Read Gate or Write Gate during the embedded servo area. If the drive electronics is unable to properly recover an embedded servo area, any attempt to write in the succeeding sector area will generate a Write Fault.

B. Hardware Unsafe Faults Which Cause Head Retract

These types of faults indicate a detected drive hardware failure associated with the data read/write chain or the embedded servo internal protection electronics. These faults may be generated by a head failure (i.e., open or shorted head), the loss of write current, the loss of Write Data during the Write Gate time, internal write enable during an embedded servo field, or absence of one of two required signals to the read/write electronics signifying the presence of an embedded servo field (i.e., a redundancy check type feature).

*This value subject to change at a later date.

5.2.2 -contd.

C. Hardware Detected Faults Which Cause Head Retract

This type of fault, which indicates the loss of internal spindle motor speed control or improper servo positioning operation, will force a retract of the read/write heads. This type of fault may be created by the absence of embedded servo fields, an unsafe DC power voltage used by the head positioning electronics (i.e., +5 volts or ±16.5 volts), or a below normal voltage on the emergency retract capacitor.

D. Microcomputer Detected Faults

A microcomputer within the LMD continuously monitors the drive performance to determine safe and reliable operation of the LMD servo and spindle motor electronics. A microcomputer detected fault may be created by the inability of the servo phase locked oscillator to maintain frequency synchronization for servo positioning control or data field write control, out of tolerance spindle motor RPM, detection of the read/write heads positioned outside the valid data zones of the disk, or a failure of the drive to pass the power turn-on self test functions.

Certain microcomputer detected faults may lead to an emergency retract if the fault condition persists. Some faults indicate a Seek Error, and others indicate a need for maintenance though the LMD is still usable.

5.2.2 Individual Lines (cont'd)

4. Seek Error

When this line is true, a seek error has occurred. The error may only be deactivated by performing an RTZ. This signal indicates that the unit was unable to complete a move within 500 ms, or that the carriage has moved to a position outside the recording field or received an illegal track address. A Return-to-Zero Seek Command will deactivate Seek Error signal, return the heads to cylinder zero, select head zero, and enable the On Cylinder signal to the controller.

If an address greater than 205 is attempted, the Seek Error signal will go true within 1500* µs maximum of the cylinder address Tag 1. Carriage movement is not attempted until a RTZ command is received to deactivate the Seek Error signal.

5. On Cylinder

This status indicates the servo has positioned the heads over a track. The status is deactivated with any seek instruction.

For a zero distance seek without a head change command, On Cylinder is deactivated for 1500* µs maximum. For a zero distance seek with a head change, On Cylinder is deactivated for 10 ms maximum (see Figure 5.2-2 for Timing). For logic changes (i.e., either 0 to 1 or 1 to 0) in the Servo offset plus and minus commands, On Cylinder is deactivated within 300 ns and activated within 2000* µs max. for Flat Cable Interface compatibility.

6. Unit Ready

When true, and the device is selected, this line indicates that the device is up to speed, and the heads are positioned over the recording tracks.

*This value subject to change at a later date.

5.2.2 Individual Lines (cont'd)

7. Open Cable Detector

The open cable detect circuit (see Figure 5.1-3) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost. ("B" interface is not disabled by the open cable detect circuits).

NOTE

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation of the drive before the controller is ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 ohm termination resistance to ground should be used at the controller end.

8. Unit Select Tag

The rising edge of this signal signifies that the Unit Select (2^0, 2^1, 2^2, 2^3) lines are valid. The unit will be selected 600 ns (maximum) after the leading edge of this signal. For timing see Figure 5.2-5.

9. Unit Select (2^0, 2^1, 2^2, 2^3)

These four lines are binary coded to select the logical number of 1 of 4 LMD devices. The unit number (0 through 15) is selectable by means of switches located on a card within the PIO. A maximum of 4 Lark drives per system is allowed (Figure 4.0-1).

10. Address Mark Found

This signal is not activated by the LMD but is daisy chained at the connector. This signal output will always be a logic zero.

11. Write Protected

When this line is true, it indicates that the LMD is write protected. This signal will occur when write protection is desired by setting the PROTECT switch for the fixed volume or a tab setting on the removable volume. If Write Gate becomes true when the drive is write protected on the selected volume, then the Fault Line will become true. The write protected condition can be eliminated by resetting the PROTECT switch for the fixed volume or by changing the tab setting for the removable volume.

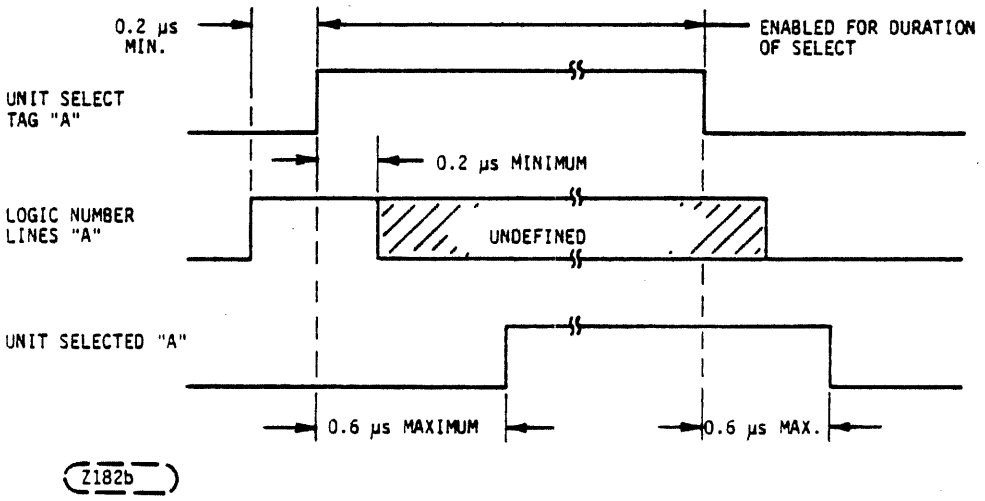


Figure 5.2-5. Logic Number Select and Timing Diagram

5.2.2 Individual Lines (cont'd)

12. Busy (Dual Channel Only)

The LMD has no Dual Channel option, but this signal is daisy chained, at the connector. This signal output is electrically undefined for a LMD with no electrical connections made within the LMD except a daisy chain connection at the connectors.

13. Spindle Motor Control (Hold and Pick) (Figure 5.2-6).

The Hold line enables the interface to start or stop the spindle motor provided the LMD DC power is on, the LMD AC power is on, and the control panel Start/Stop switch is in the Start position. Activation of the Hold input (i.e., a logic 1 or low level) will initiate rotation of the spindle motor. The spindle motor will be up to speed within 120 seconds maximum after application of the hold signal. The spindle motor up to speed condition will be reflected in the interface "Ready" line. The spindle motor may be stopped by deactivation of the Hold line (refer to Figure 5.2-6). The spindle motor will be stopped within 60 seconds maximum after the Hold input is deactivated. Note the "Ready" status will go false when the Hold input is deactivated.

NOTE

The LMD will provide a 10 ms minimum noise filter to the Hold line to guard against false detection of the Hold line, due to noise.

Individual devices may be started and stopped via the control panel Start/Stop switch if the interface Hold signal is activated (Low Level or logic 1).

NOTE

An internal switch is available for maintenance purposes which allows the spindle motor to be started or stopped by the control panel switch regardless of the state of the Hold input.

The LMD will directly pass the Pick signal for daisy chained operation but will not functionally interpret this signal.

INTERFACE SPECIFICATION FOR LMD (LARK) DRIVE

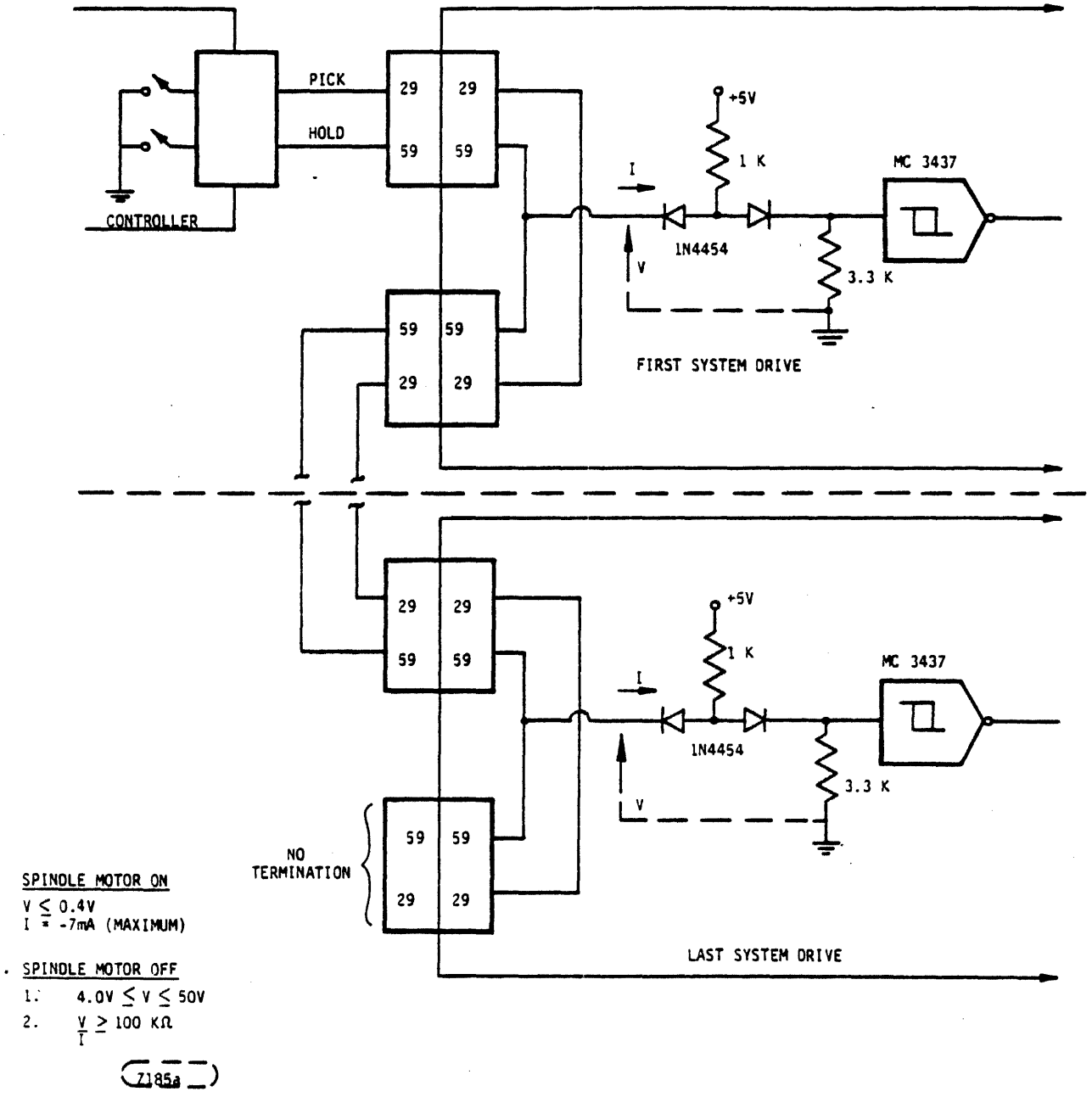


Figure 5.2-6. Spindle Motor Power Sequencing Control

5.2.2 Individual Lines (cont'd)

The following individual lines are contained in the interface "B" cable (Figure 5.1-5).

1. Unit Selected

   When the four Unit Select bit lines compare with settings of the unit select switches within the PIO, and when the leading edge of Unit Select Tag is received, the Unit Selected line goes to logic 1 and is transmitted to the controller on the "B" cable (see Figures 5.1-5 and 5.2-5).

2. Seek End

   Seek End is the combination of On Cylinder or Seek Error indicating that a seek operation has terminated.

   For a zero distance seek on the same head, Seek End goes to logic 0 for 2 ms maximum. For a zero distance seek with a head change, Seek End goes to logic 0 for 10 ms maximum (see Figure 5.2-2 for Timing).

   If a cylinder address greater than 205 has been selected (illegal cylinder address), Seek End will go false for 3 ms maximum.

5.2.3 Data and Clock Lines (Figures 5.1-5 and 5.2-7)

These lines are contained in the interface "B" cable.

1. Write Data

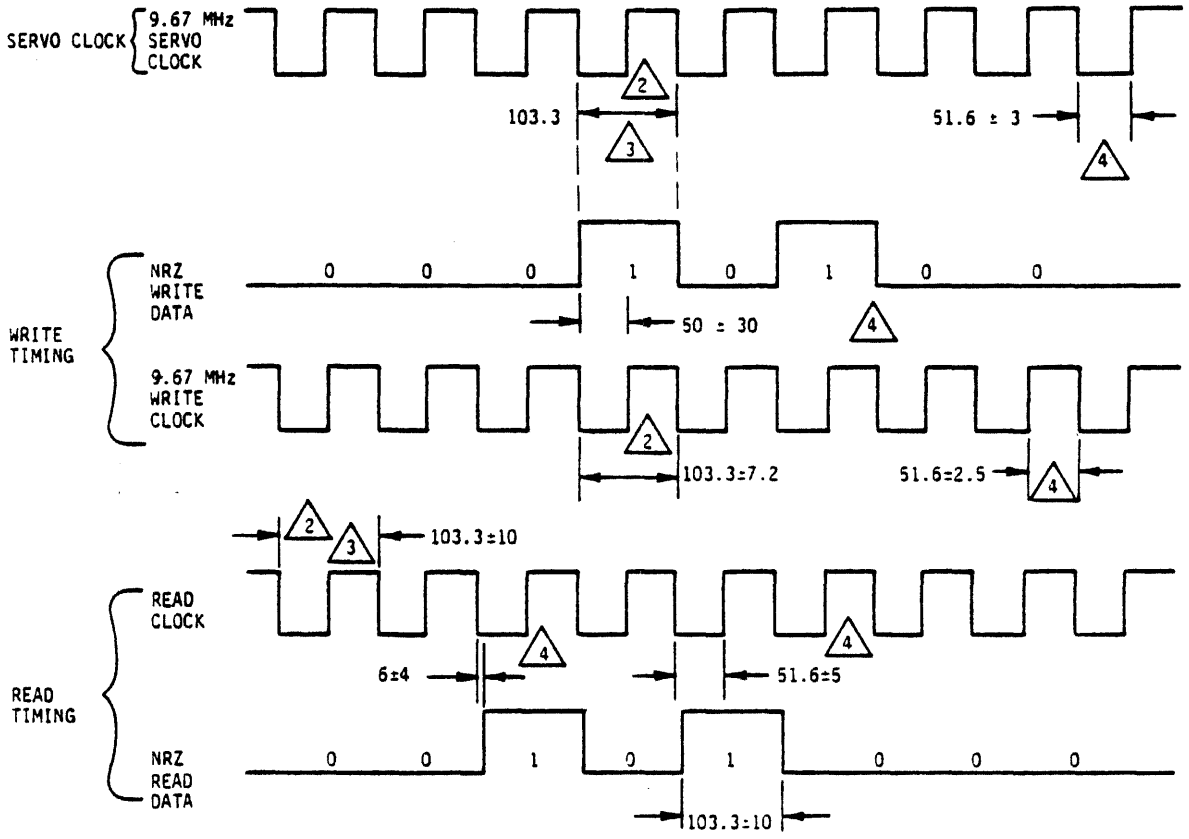
   This line carries NRZ data which is to be recorded on the disk pack.

2. Servo Clock

   The Servo Clock (Figure 5.2-7) is a continuously transmitted phase-locked 9.677 MHz (nominal) clock used to generate write data. Servo Clock is not gated with Unit Selected. This clock is frequency locked to the disk rotational speed by sampling a field within the embedded servo. Since the Servo Clock is derived via a sampled PLO system, the exact number of servo clocks between sector pulses may vary by ±4 clock cycles.

3. Read Data

   This line transmits the recovered data in the NRZ form (see Figure 5.2-7).



NOTES

1. ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE.
2. SIMILAR PERIOD SYMMETRY SHALL BE ±2 ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% to +4%.
4. TIMING APPLICABLE DURING READING OR WRITING.

Z187a

Figure 5.2-7 . NRZ Data and Clock Timing

5.2.3 Data and Clock Lines (cont'd)

4. Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 5.2-7. This signal is transmitted continuously, and is in phase sync within 88 servo clock periods from the concurrence of Read Gate and a PLO sync field.

5. Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ Write Data as illustrated in Figure 5.2-7. The Write Clock is the Servo Clock retransmitted to the device during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Gate.

5.3 DATA FORMAT AND DATA CONTROL TIMING

5.3.1 Format Definition

The Record Format on the disk is under limited control of the Controller; i.e., the embedded servo field may not be modified by the Controller. The Index and Sector pulses are available for use by the controller to indicate the beginning of a track or sector. A suggested format for fixed data records is shown in Figure 5.3-1.

The Format presented in Figure 5.3-1 consists of three functional areas: Embedded Servo, Address, and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the Disk where the Data areas are to be recorded.

5.3.1.1 Embedded Servo Area

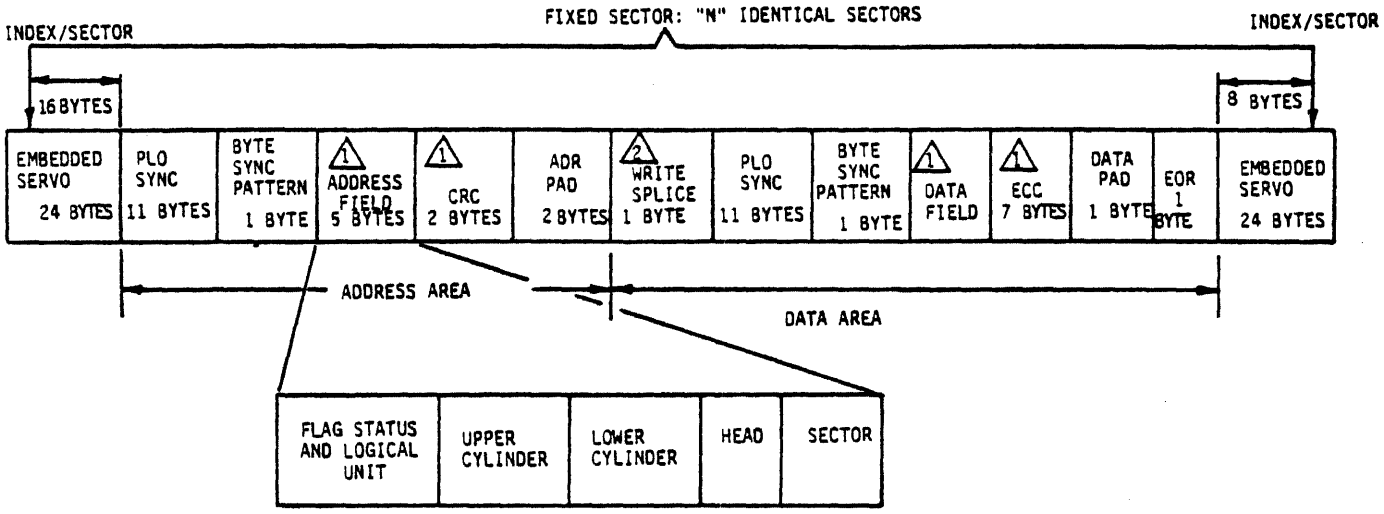
This area is 24 bytes long and is permanently preformatted on each track, it contains information for the drive's positional servo logic. This area is used solely by the drive and is not accessible by the controller, although the controller must allow for its existence.

NOTE

The LMD will internally ignore Read or Write Gate during the Embedded Servo Area.

This gap also serves as an interrecord gap between sectors to allow Controller decision making time.

INTERFACE SPECIFICATION FOR LMD (LARK) DRIVE



EXAMPLE NO. 1: DATA FIELD LENGTH USING 64 SECTORS

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

$$\text{DATA FIELD} = \frac{20{,}672}{64} - 67$$

$$\text{DATA} = 256 \text{ BYTES/SECTOR}$$

$$\% \text{ EFFICIENCY} = \frac{256 \times 64}{20{,}672} = 79\%$$

1 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

2 THIS WRITE SPLICE BYTE IS IN THIS LOCATION AS A RESULT OF A RECORD UPDATE, FOR FORMATTING CONSIDERATIONS THIS BYTE MAY BE ALLOWED FOR AT THE END OF THE DATA SECTOR BY INCREASING THE NUMBER OF EOR (END OF RECORD) BYTES FROM 1 TO 3. (REFER TO SECTIONS 4.1 AND 4.2)

Z271a

Figure 5.3-1. Sector Format

5.3.1.2 Address Area (Figure 5.3-1)

The address area is used to provide a positive indication of the track and sector locations. The address area is normally read by the Controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the Controller during a format function (Section 5.3.1) and thereafter only read to provide a positive indication of the sector location and establish the boundaries of data area. The address area consists of the following bytes.

a. PLO Sync (11 bytes minimum)

These 11 bytes of zeros are required by the drive to allow the drive's read data phase locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

b. Byte Sync Pattern (1 byte)

This byte is user-defined; it indicates to the user's Controller the beginning of the address field information, and it establishes byte synchronization (ie., the ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes).

c. Address Field

These bytes are user-defined and interpreted by the user's Controller. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address and one byte to define the sector address. (Although one byte of cylinder address encompasses the current LMD cylinder address space, two bytes are suggested for future enhancements and/or "module drive" family compatibility).

d. CRC (2 bytes recommended) -(Address Field Check Codes)

Selection of an appropriate error detection mechanism, such as a cyclic redundancy check code, is made by the user and applied to the address for file integrity purposes. These codes are generated by the user's Controller and written on the media when the address field is written. Data integrity is maintained, by the user's controller recalculating and verifying the address field check codes when the address field is read.

5.3.1.2 Address Area (cont'd)

e. ADR Pad (2 bytes) - (Address field pad)

The Address Field Pad bytes must be written by the Controller and is required by the drive to ensure proper recording and recovery of the last bits of the address field check codes.

5.3.1.3 Data Area (Figure 5.3-1)

The data area is used to record the user's data fields. The contents of the data fields within the data area are usually specified by the Host Computer system. The remaining parts of the data area are usually specified and interpreted by the user's disk controller to recover the data fields and ensure their integrity. The data area consists of:

a. Write Splice (1 byte)

This byte area is required by the drive to allow time for the write drivers to turn on and reach a recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format and is described in greater detail in Section 5.3.2.

b. PLO Sync (11 bytes)

These 11 bytes of zeros are required when reading to allow the drive's phase locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

c. Byte Sync Pattern (1 byte)

This byte is user defined and indicates to the user's controller the beginning of the data field bytes plus establishes byte synchronization for the data field.

d. Data Field (256 bytes with 64 sectors per track, or 512 bytes with 32 sectors per track)

The data field contains the Host System's data files.

e. ECC (7 bytes maximum) -(Data Field Check Codes)

Error correction codes are user defined and provide error detection and correction capability on the data field. The use of ECC is recommended for the LMD but is not mandatory.

5.3.1.3 Data Area (cont'd)

f. Data Pad (1 Byte) - (Data Field Pad)

The Data Field Pad byte must be written by the Controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes.

g. End of Range (1 byte)

This byte is required by the drive to account for electro-mechanical tolerances. They are not necessarily read or written, but they must be allocated in the sector format design.

The sector format in Figure 5.3-1 has been defined to account for restrictions placed on the format by the drive as well as functionality required by a disk controller. The following two sections recommend a procedure to be followed by the controller in order to format media per this format (Section 5.3.2) and discuss the control timing required to perform a data field read function and a data field write function per this format (Section 5.3.3).

5.3.2 Write Format Procedure

Provisions must be made within the Controller to format the disk. The following procedure is recommended for fixed sector formats with separate address and data fields.

PROCEDURE (Refer to Figure 5.3-2)

1. Select desired unit, cylinder, volume and head.

2. The Controller must wait for "On Cylinder" to begin a search for the leading edge of Index. This wait period will insure that the unit will be ready to write when the leading edge of Index is detected plus insure rotational position integrity as defined by the Index and Sector pulses.

3. Search for the leading edge of desired Sector pulse.

   NOTE

   The Index pulse provides a common rotational reference for each track and is considered a sector pulse.

4. Detect the leading edge of the selected Sector pulse and activate Write Gate and start transmitting zeros.

   NOTE

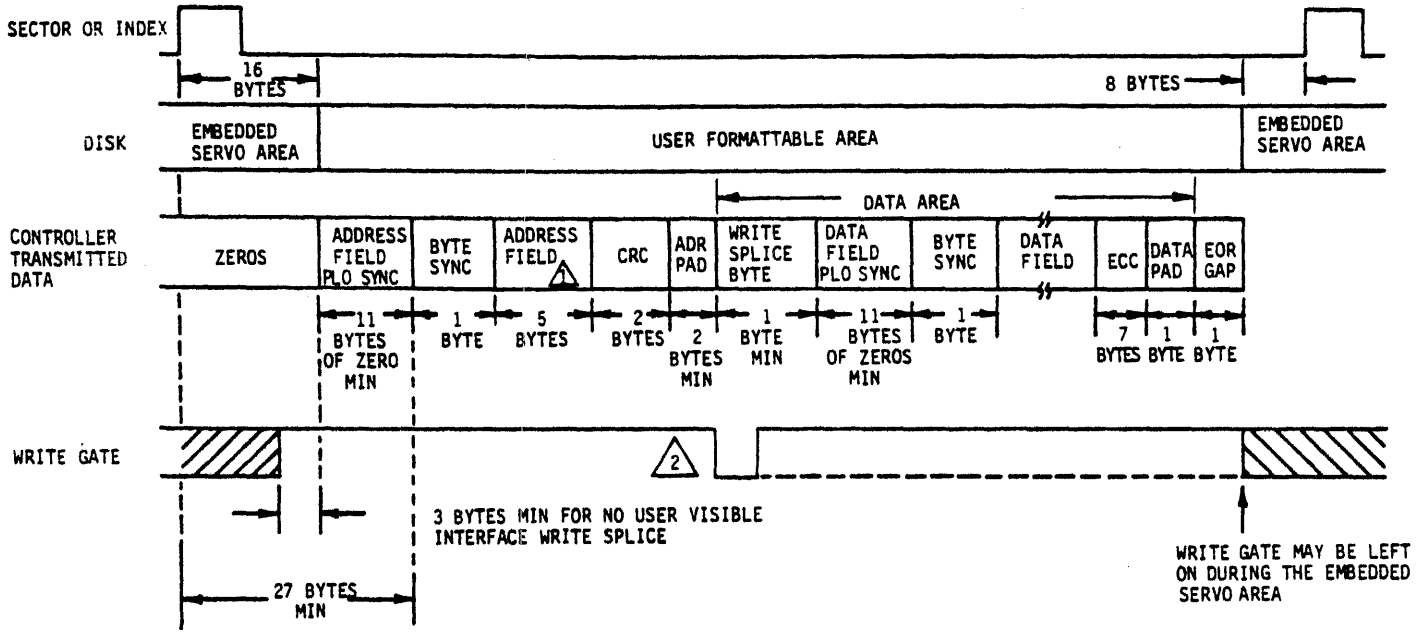
   The embedded servo is a write protected area (by the drive) and data transmitted to the drive by the Controller during the embedded servo time will not be written on the disk; however, to control write splice timing between the embedded servo area and the address PLO Sync field it is recommended that the controller activate Write Gate and begin transmitting all zeros no later than 13 byte times after the leading edge of the Sector pulse.

5. Transmit all zeros during the embedded servo area (beginning at least three byte times before the end of the embedded servo area) and for the address PLO sync field (11 bytes minimum). This is equivalent to transmitting a minimum of 27 bytes of zeros from the leading edge of the Sector pulse.

6. Transmit a byte sync pattern, the address field, and the address field check codes (CRC).

7. Transmit all zeros for the address field pad bytes, and terminate the Write Gate.

8. If a data field is to be written, proceed to Step 9, if no data field is to be written, proceed to Step 11.



1. THE ADDRESS FIELD INCLUDES THE CYLINDER HEAD AND SECTOR LOCATION.

2. WRITING THE DATA AREAS ARE OPTIONAL. THESE AREAS ARE USEFUL TO VERIFY THE INTERGRITY OF THE SECTOR IF THE FORMATTER READ VERIFIES THESE AREAS AFTER A FORMAT OPERATION WHICH ALSO WRITES THE DATA AREAS. IF DATA FIELDS ARE TO BE WRITTEN, WRITE GATE MUST BE DEACTIVATED FOR A MINIMUM OF ONE BIT TIME AFTER THE ADDRESS PAD AND REACTIVATED 6 BITS PRIOR TO THE DATA FIELD PLO SYNC AREA.

Z27Ib

Figure 5.3-2. Format Timing

5.3.2 Write Format Procedure (cont'd)

9. Reinitiate Write Gate during the write splice byte. Transmit all zeros for a data field PLO sync area (11 bytes minimum), transmit a data field byte sync pattern, the desired data, and the data field check codes (ECC).

10. Transmit all zeros for the data field pad (1 byte minimum).

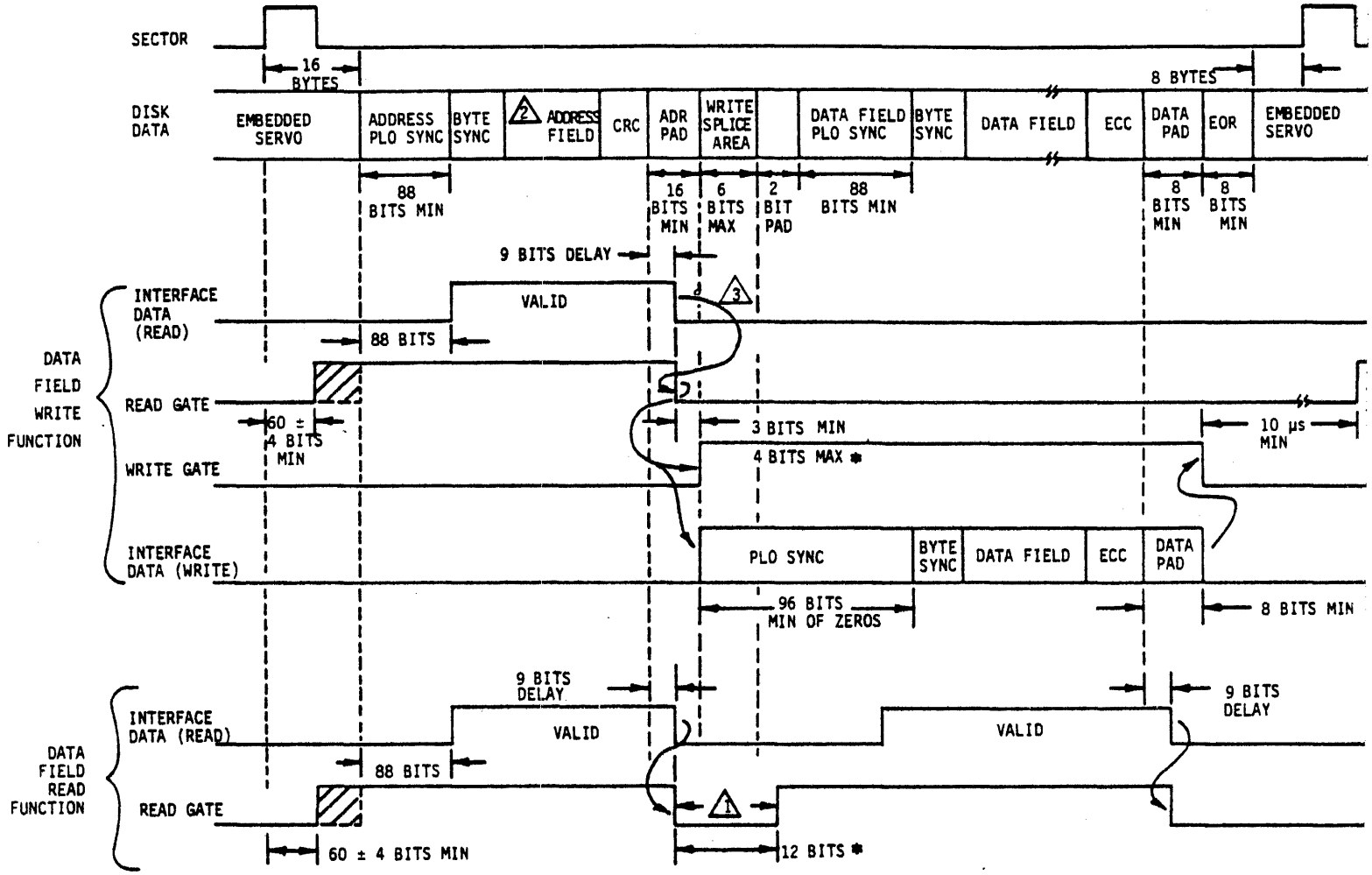
11. The controller may now terminate the write function and proceed to Step 1 if the entire track has been formatted or proceed to Step 3 if additional sectors on this track to be formatted. If additional sectors on the track are to be formatted, the Controller may leave Write Gate on until the next Sector pulse is detected and then proceed to Step 4. (If sequential sectors are to be formatted, Write Gate may be continuously left on, but the controller timing must be reinitialized with the next Sector pulse.)

This format procedure has allowed three bytes between the last bit of the address field check code and the first bit of the data field PLO sync field (i.e., the Address Field Pad and the Write splice bytes). However, if during formatting, Write Gate is enabled relative to the Sector pulses and the address and data areas are written consecutively (i.e., no physical write splice is created between the address and data areas), then only the Address Field Pad byte is required if three End of Range (EOR) bytes are allowed for at the end of the data area. (This allows CMD family format routines to be used for the LMD with a different number of format bytes only required between the end of the data field and the next sector pulse). Note that this format variation is still compatible with the normal read/write routines since a splice will be created per Figure 5.3-1 when a record update function is performed, redistributing the 3 byte EOR to a 1 byte EOR field and a write splice byte.

5.3.3 Read/Write Control Timing (See Figure 5.3-3)

The objective of this section is to specify the interrelationship of the drive interface control leads necessary to recover or record data fields on a formatted disk media. The format of Section 5.3.1 will be assumed; however, critical drive dependent parameters will be summarized to enable controller variations in the read/write timing.

To perform a data field read function, the address field is read and verified, then its data field is read. To perform a data field write function, the address field is read and verified, then the data area is written. The following sections will expand on these concepts.



1 READ GATE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD. THE 12 BYTE EXAMPLE CONSISTS OF ONE BYTE OF WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

2 THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

3 CABLE/CONTROLLER DELAY NOT SHOWN. MUST BE ≤ 4 BIT TIMES FOR THIS EXAMPLE. ALL TIMING SPECIFIED AT THE DRIVE CONNECTOR.

* VALUES ARE FOR THIS EXAMPLE.

Z272a

Figure 5.3-3. Typical Read/Write Timing

5.3.3.1 Read Function

The read function consists of reading the address fields and then the data fields. The critical interface lines associated with a read function are the Sector (Index) pulses, Read Gate, Read Clock, Read Data, and Servo Clock lines.

- Address Field Read (See Figure 5.3-3)

  The location of the address field is defined relative to the Sector (Index) pulse. To recover the address field the Controller waits for the leading edge of a Sector (Index) pulse. 60 ±4 Servo clock periods after the leading edge of a Sector (or Index) pulse Read Gate may be activated. The leading edge of Read Gate forces the phase locked oscillator to synchronize on the PLO sync field. Read Gate also enables the read data ouptut of the data separator after frequency and phase synchronization is established. Synchronization to the PLO sync pattern will not begin until the end of the embedded servo area. Read gate may be activated during the embedded servo area with internal drive logic accounting for the write splice between the embedded servo and the address field PLO sync if the formatter initiated a sector format function at least 3 bytes prior to the end of the embedded servo area.

  Read Data will be valid within 88 Servo Clock periods after the concurrence of Read Gate and the PLO Sync field. Read Clocks are transmitted continuously and will be in phase and frequency synchronization with the Read Data within 88 Servo Clock periods after the concurrence of Read Gate and the PLO Sync field. The Read Data lines will be a logic zero until the first one bit of the byte sync pattern is detected. It is then the controllers responsibility to establish byte synchronization, perform the address field verification and interpret the address field check codes (CRC). Read Gate may be deactivated after the last bit of the address field check code is received by the Controller and must be deactivated at least one bit prior to a Write Splice area.

  For example, consider the format of Figure 5.3-3. This example has a Write Splice area located on the disk two bytes after the address field check codes (the creation of this Write Splice area will be explained in Section 5.3.3.2). An examination of the Interface Data (Read) timing signal of Figure 5.3-3 reveals that the Interface Read Data is delayed by 9 bit times from data recorded on the media. Thus, to meet the requirement that Read Gate must be deactivated at least one bit prior to a Write Splice area requires that, for the format of Figure 5.3-3, Read Gate must be deactivated within six bit times after the reception of the last bit of the address field check code by the controller.

5.3.3.1 Read Function (cont'd)

The Controller may compare the contents of the disk media recorded address field to the desired sector location as they are received from the drive. However, a valid comparison should not be assumed until the disk media recorded CRC check code verifies its correctness. If the recorded and desired address fields compare and no check code error is detected, then the desired Data Area for either a data field update or data field read function has been found.

- Data Field Read (See Figure 5.3-3)

After the desired sector location has been found by comparison to the address field, the data field may be read. When a data field is updated a 6 bit wide Write Splice area is created on the media (see Section 5.3.3.2 Read Gate must be deactivated a minimum of one bit time preceding a Write Splice area and may be activated a minimum of one bit after a Write Splice area. For example consider the format of Figure 5.3-3. To satisfy the Read Gate/Write Splice timing requirements, Read Gate could be deactivated as soon as the last bit of the Address Field check code was received by the controller and activated 12 bit times following the Write Splice area. The example chose to deactivate Read Gate as soon as the last bit of the address field check code was received (versus deactivating Read Gate 6 bit times after the last bit of the address field check code) for timing compatibility with the data field update function (Section 5.3.3.2) which assumed this timing relationship to enable Write Gate and create the Write Splice area in the location shown in Figure 5.3-3.

Per Figure 5.3-3 if the Read Gate is activated after the Write Splice and at the beginning of the Data Field PLO Sync area, the interface Read Data lines will be valid within 88 servo clock periods. (The two bit pad following the Write Splice area allows Read Gate to be activated a minimum of 1 bit time after the Write Splice and still insures 11 bytes of Data Field PLO Sync Characters). The Controller may then search for the Data field byte sync pattern, establish byte synchronization, and read the Data field plus read and intrepret the Data field check codes. Read Gate may be deactivated after the last bit of the data field check code (ECC) is received (i.e., after the required number of Read Clocks is received after byte synchronization is established.

5.3.3.1 Read Function (cont'd)

- Summary of Critical Read Function Timing Parameters

  Controller variations of the read timing are allowed if the following drive-dependent parameters are met;

  a. Read Initialization Time

     Any head command requires a seek, and a read or write may not be initiated until On Cylinder is true following the seek command for the head change.

  b. Read Gate Timing

     Requesting the drive to establish bit synchronization (i.e., enabling Read Gate) for the address area should be done no earlier than 60 ±4 bits from the leading edge of a Sector (Index) pulse and at least 11 bytes prior to the address field byte sync pattern.

     Read Gate may not be enabled or True during a Write Splice area (Read Gate must be deactivated one bit time minimum before a Write Splice area and may be enabled one bit time minimum after a Write Splice area).

     NOTE

     Data (READ) at the interface is delayed by 9 bit times from the data recorded on the disk media.

5.3.3.2 Write Function (Figure 5.3-3)

The Write function consists of reading the address field to verify the sector location, and then writing the Data Area PLO Sync characters, the Byte Sync pattern, the Data Field, the Data Field Check Codes (ECC) and a Data Field Pad byte. The critical interface lines associated with the write function are the Write Gate, Write Data, and Servo Clock lines.

- Read Address Field Prior To Write

  The address field and address field check codes should be read and verified prior to writing the data area, except while formatting.

5.3.3.2 Write Function (cont'd)

- Write Splice Creation

  The last interface Read Data bit of the address field check codes will be delayed by 9 bit times from the recorded disk location. Thus if the Controller deactivates Read Gate when the last bit of the address field check code is detected, the disk R/W head will be located 9 bit times into the address pad byte. When the Read gate is deactivated the Write clocks to the drive should be enabled. (The Drive requires Write clocks to precede Write Gate by a minimum of 250 ns).

  The Controller must provide three-servo clock periods, minimum, of delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal. This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit. Thus from Figure 5.3-3, if the Read Gate was deactivated when the last interface data bit of the address field check code was received by the Controller and the Write Gate was activated 4 Servo Clock periods after Read Gate was deactivated a Write Splice area would be created at the location shown in Figure 5.3-3 (i.e., the Write Splice area on the media would start 16 bit times from the last bit of the recorded address field check code). In addition, if Write Clocks were enabled when Read Gate was deactivated the drive requirement for Write Clocks to precede Write Gate by 250 ns would also be met.

  Since the write driver turn on delay plus data encoder turn on delay is 6 Servo Clock periods maximum from the leading edge of Write Gate, the width of the Write Splice area recorded on the disk media will be 6 Servo Clock periods maximum.

- PLO Sync Field Write

  The PLO Sync field must consist of 11 valid and recoverable bytes of interface data zeros. From Figure 5.3-3 a 2-bit pad area is shown between the 6-bit splice area and the start of the data field PLO sync. This 2-bit pad area allows the Read Gate to be enabled one bit minimum after a Write Splice and be valid at the Drive Interface prior to the Data Field PLO sync bytes. Thus, to guarantee writing 11 valid bytes of PLO Sync characters, allow for the Write Splice area, and allow Read Gate to be enabled one bit time after a Write Splice but prior to an 11-byte PLO Sync field, it is recommended that the Controller transmit 12 bytes of zeros after Write Gate is enabled for the Data field PLO Sync field.

5.3.3.2 Write Function (cont'd)

- Byte Sync, Data Field, ECC and Data Pad Write

  After the Data Field PLO sync field is written a Byte Sync character should be written to enable the Controller to establish byte synchronization for the data field.

  After the data field is written, the data field check codes should be written followed by one data pad byte at the end of the check field to ensure proper recording and recovery of the check field codes.

  NOTE

  In addition to these requirements an additional 1 byte end of record (EOR) field should be allowed for in the format design to account for tolerances between embedded servo areas.

  After the data pad byte is written the Write Gate should be deactivated and Read Gate should not be activated to read the address Area of the next sector until 60 ±4 Servo Clock periods after the next Sector pulse is detected. This will allow ample time for the write-to-read recovery time (i.e., the 10 µs minimum between the trailing edge of Write Gate and the leading edge of Read Gate).

- Summary of Critical Write Function Parameters

  Controller timing variations in the record update function are allowed if the following drive dependent write (and interrelated read) timing parameters are met:

  1. Read-To-Write Time

     Assuming head selection is stabilized, the time lapse from disabling Read Gate to enabling Write Gate shall be 3 Servo Clock periods minimum.

  2. Write Clock-To-Write Gate Timing

     Write Clocks must precede Write Gate by a minimum of 250 ns.

  3. Write Driver plus Data Encoder Turn On From Write Gate

     The write driver plus data encoder turn on time (write splice width) is 6 servo clock periods maximum.

5.3.3.2 Write Function (cont'd)

4. Write Driver Turn Off From Write Gate

   To account for data encoding delays, Write Gate must be held on for at least one byte time after the last bit of the information to be recorded. (Refer to "Pad" in Figure 5.3-3.)

5. Write-To-Read Recovery Time

   The time lapse before Read Gate can be enabled after disabling the Write Gate is 10 µs minimum.