80286-BASED PRODUCTS TECHNICAL REFERENCE GUIDE Volume I

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80286-Based Products Technical Reference Guide

Fourth Edition	(December, 1987)
Third Edition	(May, 1987)
Second Edition	(October, 1986)
First Edition	(November, 1985)
Option Kit	#102789-001
Assembly	#106848-004
Text	#106485-004
Binder	#106486-004
Text Addendum	#114271-001

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NOTATIONAL CONVENTIONS

Values

I/O addresses and other values are in hexadecimal notation when shown with the letter h after them. Memory addresses are always in hexadecimal and are expressed as SSSS:0000, where SSSS is a 16-bit segment and 0000 is a 16-bit offset. All other numbers are in decimal notation.

Ranges

Ranges or limits for a parameter are shown as a pair of values separated by two dots (..). For example, 4..0 includes numbers 4, 0, and every number in between (3, 2, and 1).

Signal Labels

Signal values are labelled A0, A1, A15, etc. Signal names are in upper case. Signal names with a dash (-) as a suffix indicate that that signal is negative when true, or active when low.

Bit values are labelled bit 7, bit 6, bit 0, etc.

Labels with the smallest suffixes (A0, bit 0) have the least significance or value.

Register Notation and Usage

The standard Intel naming conventions are used for the 80286 registers. AX, BX, CX, and DX are the names of the general registers when used as word-length registers (16-bit). AH, AL, BH, BL, CH, CL, DH, and DL are the names for the general registers when they are used as byte-length registers (8-bit). When addresses are handled, BX usually contains the offset. However, SI (source index) or BP (base pointer) may also be used with the ES register.

The ES register denotes the extra segment and is used exclusively for address-segment parameter passing; FL is the flag register used to return the status of some operations. Status is given as the state of one of the flags within the register: CF for carry flag, IF for interrupt flag, etc.

The shaded register-set boxes are ignored on input and are unchanged for output. An exception is that the contents of AX are not guaranteed to be preserved across all calls. Always reload the function code in AH and the parameter in AL (if any) to repeat a call. Register contents are always preserved across BIOS calls, unless the register is used to return a value.

Bit Notation

Bit fields within a byte or word are shown as a range of decimal numbers separated by two dots <..> and enclosed in angle brackets. For example, reference to the four most-significant bits in a word is made with <15..12>. The higher number, representing the most-significant bit, is on the left.

Common Abbreviations

The following abbreviations are used throughout this guide:

Abbr.	Meaning	Comment
CNTLR	Controller	
DMA	Direct Memory Access	
FRI	Flux Reversals per Inch	
INT	Interrupt	
KB	Kilobyte	1024 Bytes
MB	Megabyte	1,024,000 Bytes
ms	Millisecond	Always preceded by a number
ns	Nanosecond	Always preceded by a number
RAM	Random-Access Memory	
ROM	Read-Only Memory	
RTC	Real-Time Clock	
TPI	Tracks Per Inch	
us	Microsecond	Always preceded by a number

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SYSTEM OVERVIEW

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SYSTEM OVERVIEW

1.1 INTRODUCTION

Chapter 1 introduces the COMPAQ PORTABLE 286® and COMPAQ DESKPRO 286® Personal Computers. It also includes information relating to their entire systems, such as:

- System characteristics
- System components
- System specifications
- System interconnection
- Introduction to the Intel 80286 Microprocessor, including the system memory map and I/O map
- System features
- Connectors

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computer systems are advanced general-purpose computers. Both have the same high performance capabilities. The main difference between them is that the COMPAQ PORTABLE 286 is portable.

The COMPAQ DESKPRO 286 has greater memory expansion capacity, more board slots, and larger fixed disk drive storage capability; requires an external monitor; and can operate at 6, 8, or 12 MHz, depending on the version of the system board installed.

Figures 1-1 and 1-2 show the two systems.

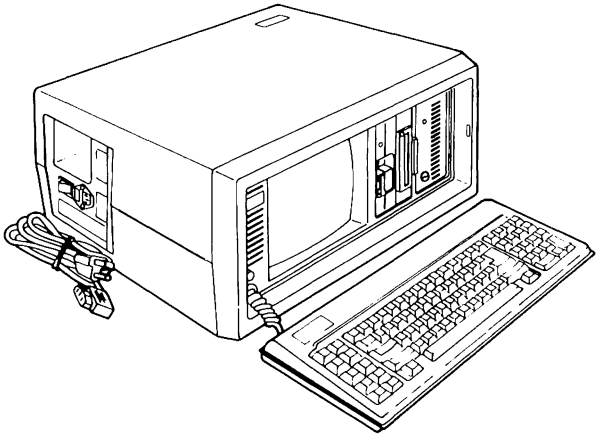

Figure 1-1. COMPAQ PORTABLE 286

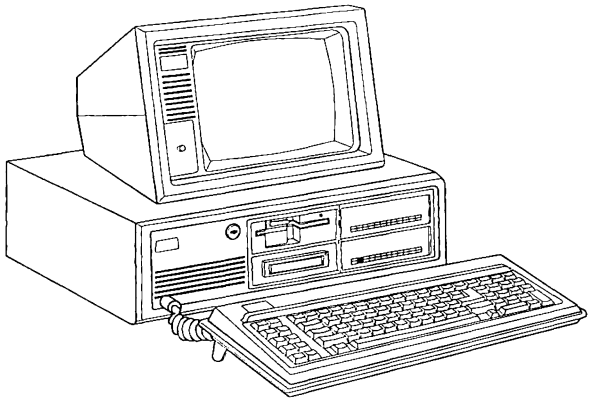

Figure 1-2. COMPAQ DESKPRO 286

1.2 SYSTEM CHARACTERISTICS

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers share the following characteristics:

- An 80286 microprocessor with an 8-MHz variable processing speed.

NOTE: The COMPAQ PORTABLE 286 and the 8-MHz COMPAQ DESKPRO 286 have data processing speeds which are switchable between 8 MHz and 6 MHz. The 12-MHz COMPAQ DESKPRO 286 has a switchable processing speed of 12 MHz and 8 MHz.

- Up to 2.7 Megabytes (COMPAQ PORTABLE 286) or 8.1 Megabytes (COMPAQ DESKPRO 286) of physical memory (using COMPAQ memory option boards).
- Numerous mass data storage options, including:
  - Diskette drives (5.25-inch 360-Kbyte or 1.2-Megabyte or 3.5" 1.44-Megabyte)
  - Fixed disk drives (20-, 30-, 40-, 70- or 130-Megabyte). (20-Megabyte fixed disk drive is the only size available for the COMPAQ PORTABLE 286.);
  - Choice of fixed disk drive backup (tape), including:
  - 10-Megabyte (COMPAQ PORTABLE 286 and 8-MHz COMPAQ DEKSPRO 286)
  - 40-Megabyte (8- and 12-MHz COMPAQ DESKPRO 286).
  - 135-Megabyte (12-MHz COMPAQ DESKPRO 286).
- Software compatibility with most popular programs written for the IBM PC-AT.
- For the COMPAQ DESKPRO 286, there has been a choice of two keyboards: the 101-key (U.S.)/102-key (international) COMPAQ Enhanced Keyboard or the 84-key keyboard. The COMPAQ PORTABLE 286 uses the 84-key keyboard.

NOTE: If your COMPAQ DESKPRO 286 Personal Computer is equipped to operate at 12 MHz, the COMPAQ Enhanced Keyboard is the only available keyboard.

- Asynchronous communications (serial) and printer (parallel) interfaces.
- Choice of three video display controller boards: the COMPAQ Video Graphics Controller Board (12-MHz COMPAQ DESKPRO 286 only); the COMPAQ Video Display Controller Board for graphics and high-resolution text; or the Color Graphics board for high-resolution graphics.
- Real-time clock with battery backup.
- Security lock.
- Multipurpose controller board.
- Multipurpose fixed disk drive controller board (COMPAQ DESKPRO 286, 12 Mhz only).

Table 1-1 lists features of the standard models of the COMPAQ PORTABLE 286 Personal Computers that operate at 8 and 6 MHz.

Table 1-2 lists features of the 8-MHz and 12-Mhz COMPAQ DESKPRO 286 personal computers.

Table 1-1. Features of the COMPAQ PORTABLE 286 Personal Computers

Features	COMPAQ PORTABLE 286 Model 1	COMPAQ PORTABLE 286 Model 2
80287 Coprocessor	Socket	Socket
Base memory size	256 KB	640 KB
Memory expansion without adding board	640 KB	640 KB
Maximum memory with (#) expansion boards	2.7 MB(1)	2.7 MB(1)
360-KB diskette drive	Option	Option
1.2-megabyte diskette drive	Standard	Standard
10-megabyte fixed disk drive backup (tape)	Option	Option
40-megabyte fixed disk drive backup (tape)	Option	Option
20-megabyte fixed disk drive (3.5 inch)	Option	Standard
Asynchronous interface (9 pin)	Standard	Standard
(Printer) interface	Standard	Standard
Security lock	Standard	Standard
Available expansion slots	3	2
Total expansion slots	5	5

Table 1-2. Features of the Various Models of 8 MHz and 12 MHz COMPAQ DESKPRO 286 Personal Computers

	COMPAQ DESKPRO 286	
Features	8 MHz	12 MHz
80287 Coprocessor Socket	Socket (6-MHz)	Socket (8-MHz)
Maximum Base memory size	640 KB	640 KB
Memory expansion without adding board	2.1 MB	2.1 MB
Maximum memory with (#) expansion boards	8.1 MB (3)	8.1 MB (3)
5.25-inch 360-KB diskette drive	Supported	Supported
5.25-inch 1.2-megabyte diskette drive	Standard	Standard
3.5 in. 1.44-megabyte diskette drive		Supported
10-megabyte fixed disk drive backup (tape)	Supported	
40-megabyte fixed disk drive backup (tape)	Supported	Supported
135-megabyte fixed disk drive backup (tape)		Supported
30-megabyte fixed disk drive	Supported	
70-megabyte fixed disk drive (Note 1)	Supported	Supported
130-megabyte diskette drive (Note 2)		Supported
20-megabyte intergrated fixed disk drive	Supported	Supported
40-megabyte intergrated fixed disk drive	Supported	Supported
Asynchronous interface (9 pin)	Standard	Standard
Printer interface	Standard	Standard
Security lock	Standard	Standard
Expansion slots	8	8

Notes: 1. Requires a multipurpose fixed disk drive controller board.
2. Requires ESDI controller board.

1.3 SYSTEM COMPONENTS FOR 8-MHZ 80286-BASED COMPAQ PERSONAL COMPUTERS

The 8-MHz COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Personal Computers are general-purpose computers with the following major components:

- System boards with:
  - An Intel 80286 microprocessor
  - A socket for an 80287 coprocessor
  - Expansion slots for mass data storage devices, video display controller boards, communication ports, and other hardware options
  - Programmable devices, such as DMA circuits, a keyboard controller, an interval timer, and an interrupt controller

The functions of the system boards for the two computers are similar, but the ROM and RAM for the COMPAQ DESKPRO 286 System Board Version 1 are on a separate memory board.

- A multipurpose controller board that supports two internal diskette drives and one fixed disk drive backup. The asynchronous communications and printer interfaces provide for communications with parallel or serial printers, modems, and other devices.
- A dual-mode video display controller board that supports the COMPAQ Dual-Mode Monitor and compatible monochrome and color (RGBI) monitors (optional with the COMPAQ DESKPRO 286). Internal color monitors are not available for the COMPAQ PORTABLE 286.
- An optional COMPAQ Enhanced Color Graphics Board and COMPAQ Color Monitor. (See the COMPAQ Enhanced Color Graphics Board Guide for details.)
- Mass data storage devices, such as diskette drives, fixed disk drives, and fixed disk drive backup systems, depending on the model.
- A power supply that provides the required voltages and current for the system board, keyboard, and typical expansion boards, such as video controllers and memory expansion boards.
- A fixed disk drive controller board that supports selected fixed disk drive options.

Figure 1-3 shows the system functional block diagram, which is the same for both systems, operating at 8 MHz.

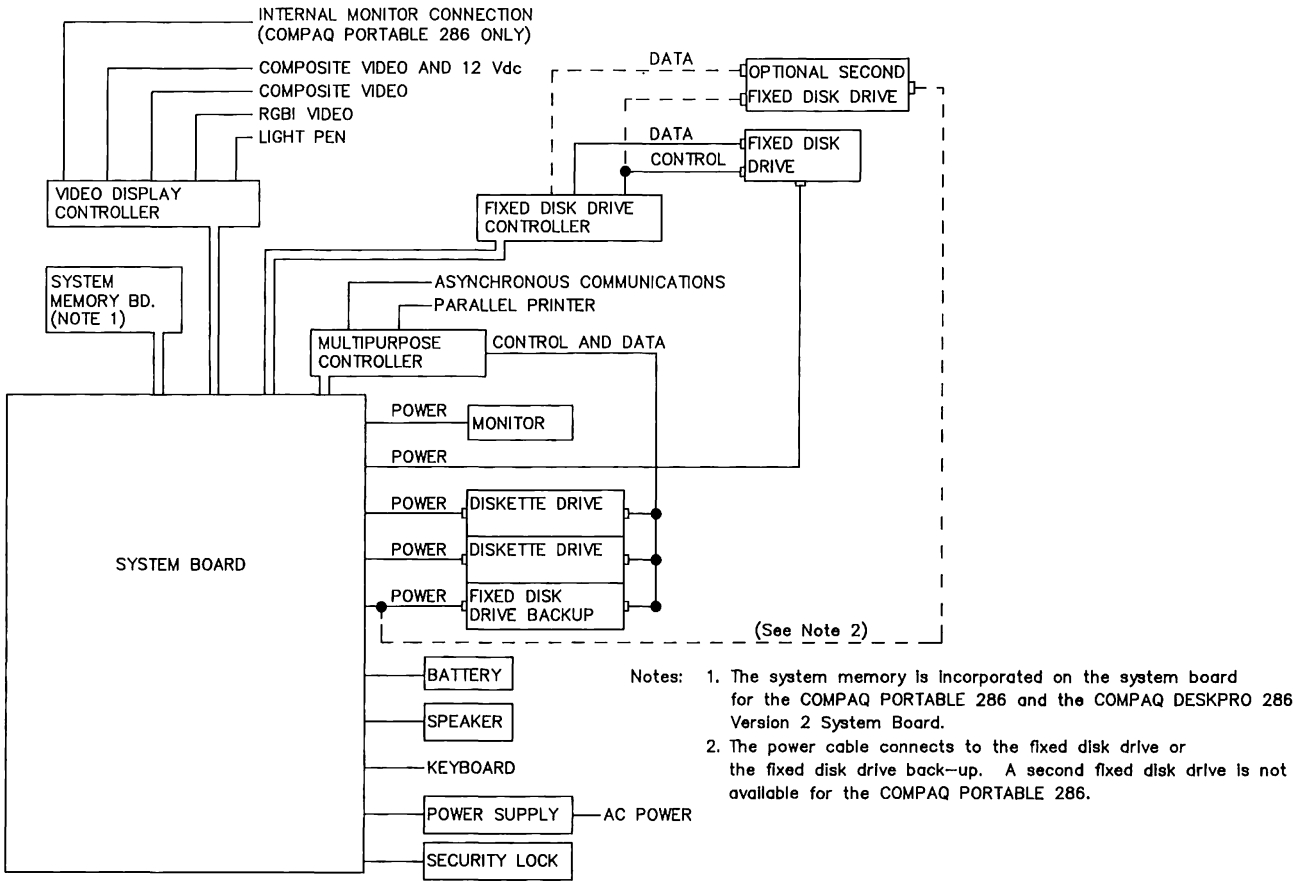

Figure 1-3. System Block Diagram for Both Systems (COMPAQ Portable 286 and COMPAQ DESKPRO 286) Operating at 8 MHz

1.4 SYSTEM COMPONENTS FOR 12-MHZ 80286-BASED COMPAQ PERSONAL COMPUTERS

The COMPAQ DESKPRO 286 Personal Computer, equipped to operate at 12 MHz, has the following major components:

- System board with:
  - A 12-MHz 80286 microprocessor
  - A socket for an 8-MHz 80287 coprocessor
  - Expansion slots for mass data storage devices, video display controller boards, communications ports, and other hardware options.
  - Programmable devices, such as direct memory access (DMA) circuits, a keyboard controller, an interval timer, and an interrupt controller.
- A multipurpose fixed disk drive controller board that supports two internal diskette drives, a maximum of two fixed disk drives with integrated controllers, and one fixed disk drive backup. The asynchronous communications and printer interfaces allow communications with parallel or serial printers, modems, and other devices.
- An optional dual-mode video display controller board that supports COMPAQ Dual-Mode Monitor, COMPAQ Color Monitor, and compatible monochrome and color (RGBI) monitors.
- An optional COMPAQ Enhanced Color Graphics Board and COMPAQ Color Monitor are available. (See the COMPAQ Enhanced Color Graphics Board Guide for details.)
- An optional COMPAQ Video Graphics Controller Board and optional COMPAQ Video Graphics Color Monitor or Video Graphics Monochrome Monitor.
- Mass data storage devices, such as diskette drives, fixed disk drives, and fixed disk drive backup systems, depending on the model.
- A power supply that provides the required voltages and current for the system board, keyboard, and typical expansion boards.
- A fixed disk drive controller board that supports selected fixed disk drive options.

Figure 1-4 shows the system functional block diagram for the 12-MHz COMPAQ DESKPRO 286 Personal Computer.

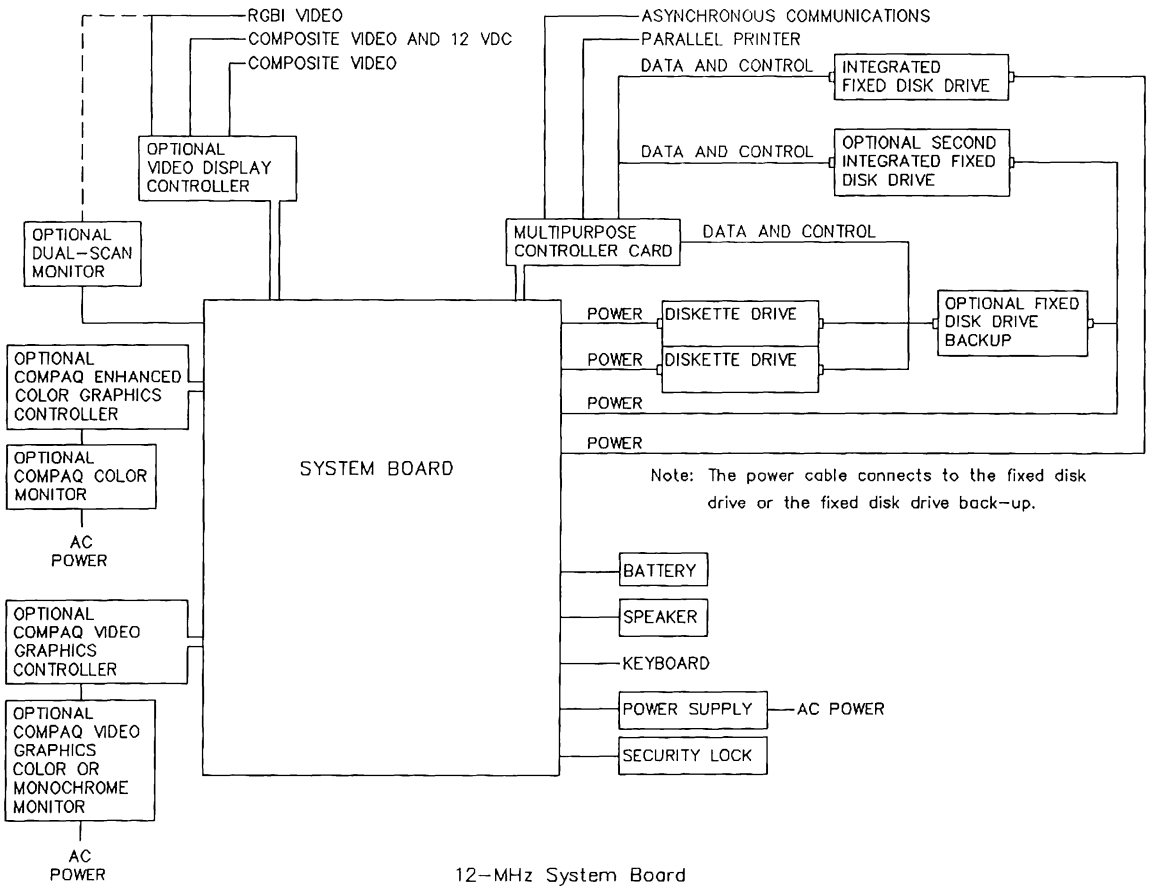

Figure 1-4. System Block Diagram for the 12-MHz COMPAQ DESKPRO 286 Personal Computer

1.5 SYSTEM SPECIFICATIONS

Tables 1-3 and 1-4 list the system specifications for the COMPAQ PORTABLE 286 and the COMPAQ DESKPRO 286 Personal Computers.

Table 1-3. COMPAQ PORTABLE 286 System Specifications

System size:	Width 20.0 in (508 mm) Height 8.5 in (216 mm) Depth 16.0 in (406 mm)
Weight:	Model 1: 30.3 lb (13.7 kg); Model 2: 33 lb (15.0 kg)
Air temperature:	Operating 50° to 104°F (10 to 40°C) Nonoperating 50° to 140°F (10 to 60°C) Shipping -22° to 140°F (-30 to 60°C)
Relative humidity (noncondensing):	Nonoperating 5% to 90% Operating 20% to 80%
Heat output:	Varies according to options installed; 1024 BTU/hr (maximum)
Noise level (acoustical):	Varies according to options installed. Nominal sound power levels (A Scale) in decibles per ANSI S1.29-1979 are: 54 (without Fixed Disk Drive Backup) 59 (with Fixed Disk Drive Backup)
Shock (Ref. Mil-Std-810C):	The values, in G's for 11 ms half-sine, of the levels of shock that the system can withstand with no damage are: Operating: 5 Nonoperating: 30
Vibration:	Values, in G's, 0 to peak, sinusoidal, 5 to 500 Hz, 1/2 octave per minute, of the levels of vibration that the system can withstand with no damage are: Operating: 0.25 Nonoperating: 0.50
AC power required (47 to 62 Hz):	120 VAC, nominal, with range of 102 to 132 VAC RMS, 3 A maximum, or 230 VAC, nominal, with range of 204 to 264 VAC RMS, 2.5 A maximum
Maximum altitude:	Operating 10,000 ft (3 000 m) Shipping 30,000 ft (9 000 m)
Agency compliances:	See Chapter 13 for additional monitor specifications. 120 VAC: UL478; CSA22.2; FCC Part 15, Class B 220-240 VAC: IEC380; DIN IEC 380/VDE 806; VDE 871, Class B

Table 1-4. COMPAQ DESKPRO 286 System Specifications

System size:	Width 19.8 in (503 mm) Height 6.4 in (162 mm) Depth 16.5 in (419 mm)
Weight:	Model 1: 37 lb (16.8 kg); Model 20: 42.4 lb (19.1 kg); Model 40: 44 lb (20.0 kg)
Air temperature:	Operating 50° to 104°F (10° to 40°C) Nonoperating 50° to 140°F (10° to 60°C) Shipping -22° to 140°F (-30° to 60°C)
Relative humidity (noncondensing):	Nonoperating 5%to 90% Operating 20%to 80%
Heat output:	Varies according to options installed 1229 BTU/hr (maximum)
Noise level (acoustical):	Varies according to options installed. Nominal sound power levels (A Scale) in decibles per ANSI S1.29-1979 are: 53 (without Fixed Disk Drive Backup) 62 (with Fixed Disk Drive Backup)
Shock (Ref. Mil-Std-810C):	The values, in G's for 11 ms half-sine, of the levels of shock that the system can withstand with no damage are: Operating: 5 Nonoperating: 20
Vibration:	Values, in G's, 0 to peak, sinusoidal, 5 to 500 Hz, 1/2 octave per minute, of the levels of vibration that the system can withstand with no damage are: Operating: 0.5 Nonoperating: 0.75
AC power required (47 to 62 Hz):	120 VAC, nominal, with range of 102 to 132 VAC RMS, 4 A max. (5 A max., 12 MHz Deskpro 286) or 230 VAC, nominal, with range of 204 to 264 VAC RMS, 2.5 A max. (4 A max., 12 MHz Deskpro 286)
Maximum altitude:	Operating 10,000 ft (3 000 m) Shipping 30,000 ft (9 000 m)
Agency compliances:	See Chapter 13 for additional monitor specifications. 120 VAC: UL478; CSA22.2; FCC Part 15, Class B 220-240 VAC: IEC380; DIN IEC 380/VDE 806; VDE 871, Class B

1.6 SYSTEM INTERCONNECTIONS

This section shows interconnections diagrams for the following COMPAQ personal computers:

- COMPAQ PORTABLE 286 Personal Computer - Figure 1-5
- COMPAQ DESKPRO 286 Personal Computer (8-MHz) - Figure 1-6
- COMPAQ DESKPRO 286 Personal Computer (12-MHz) - Figure 1-7

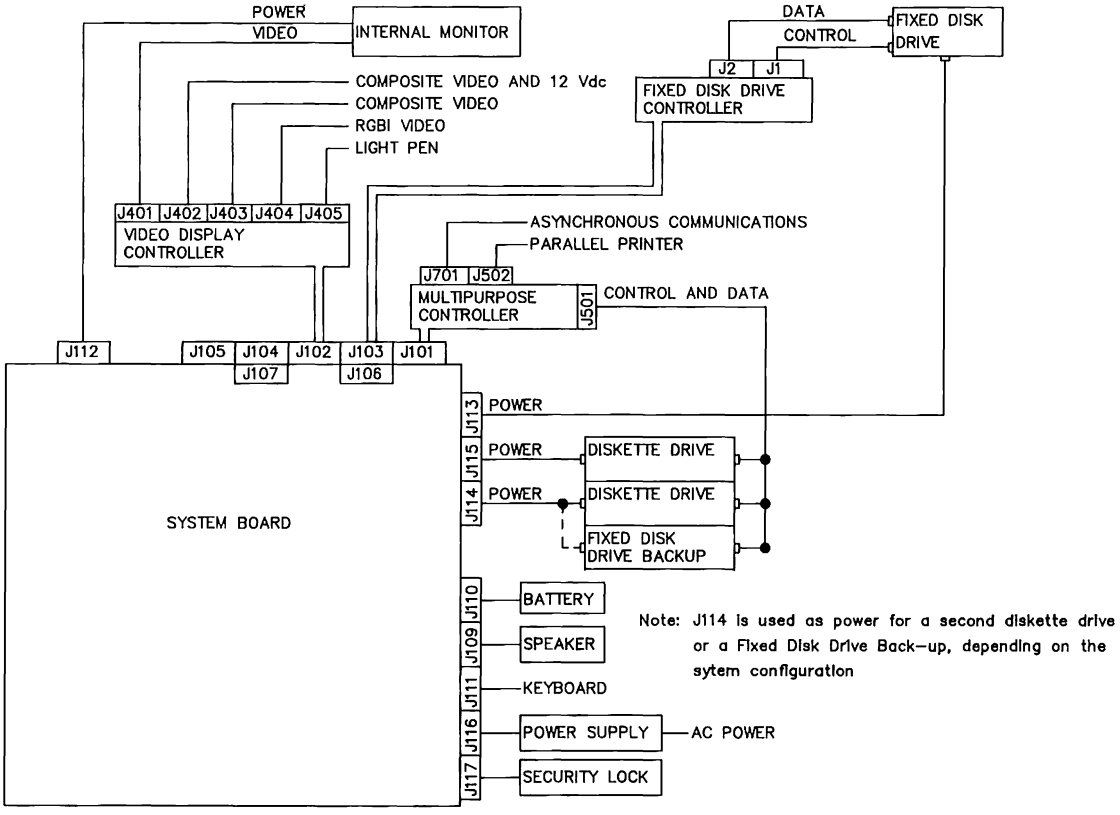

Figure 1-5. COMPAQ PORTABLE 286 Interconnection Diagram

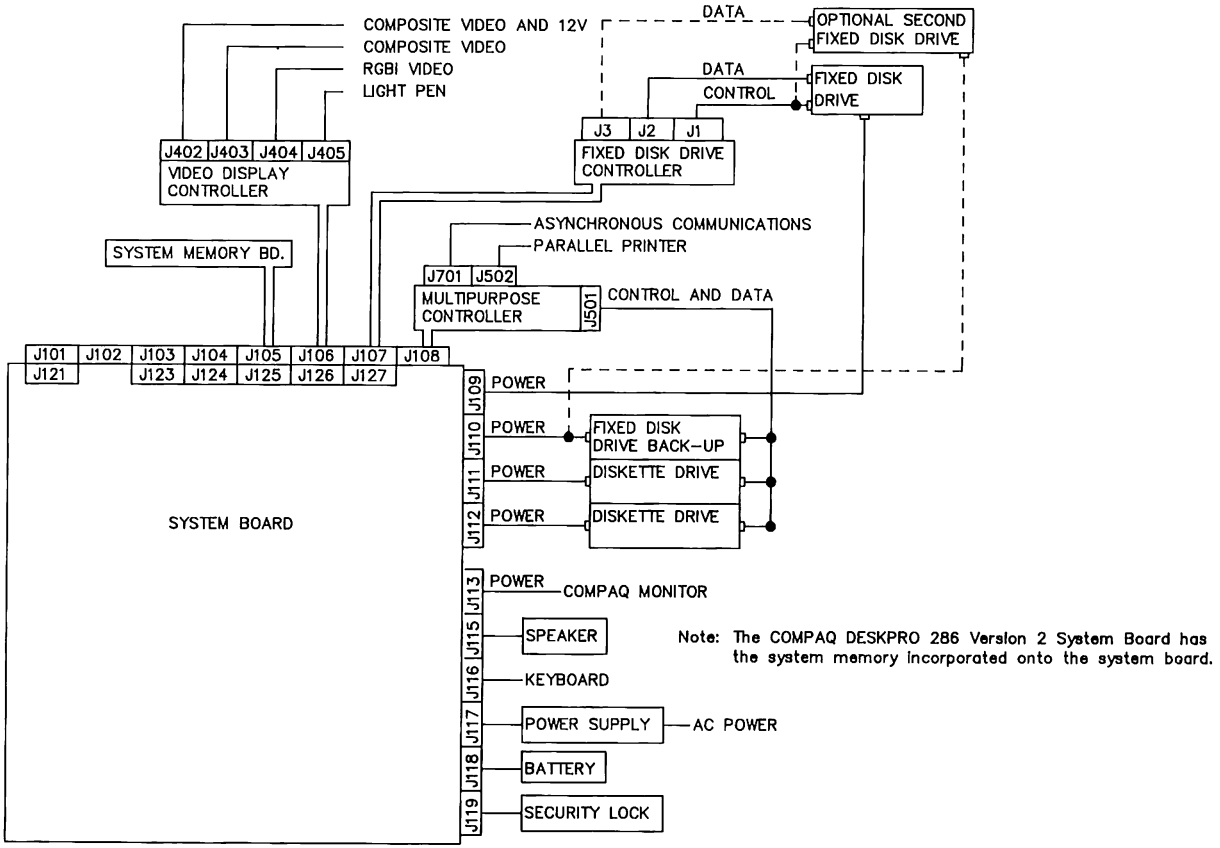

Figure 1-6. COMPAQ DESKPRO 286 (8-MHz) Interconnection Diagram

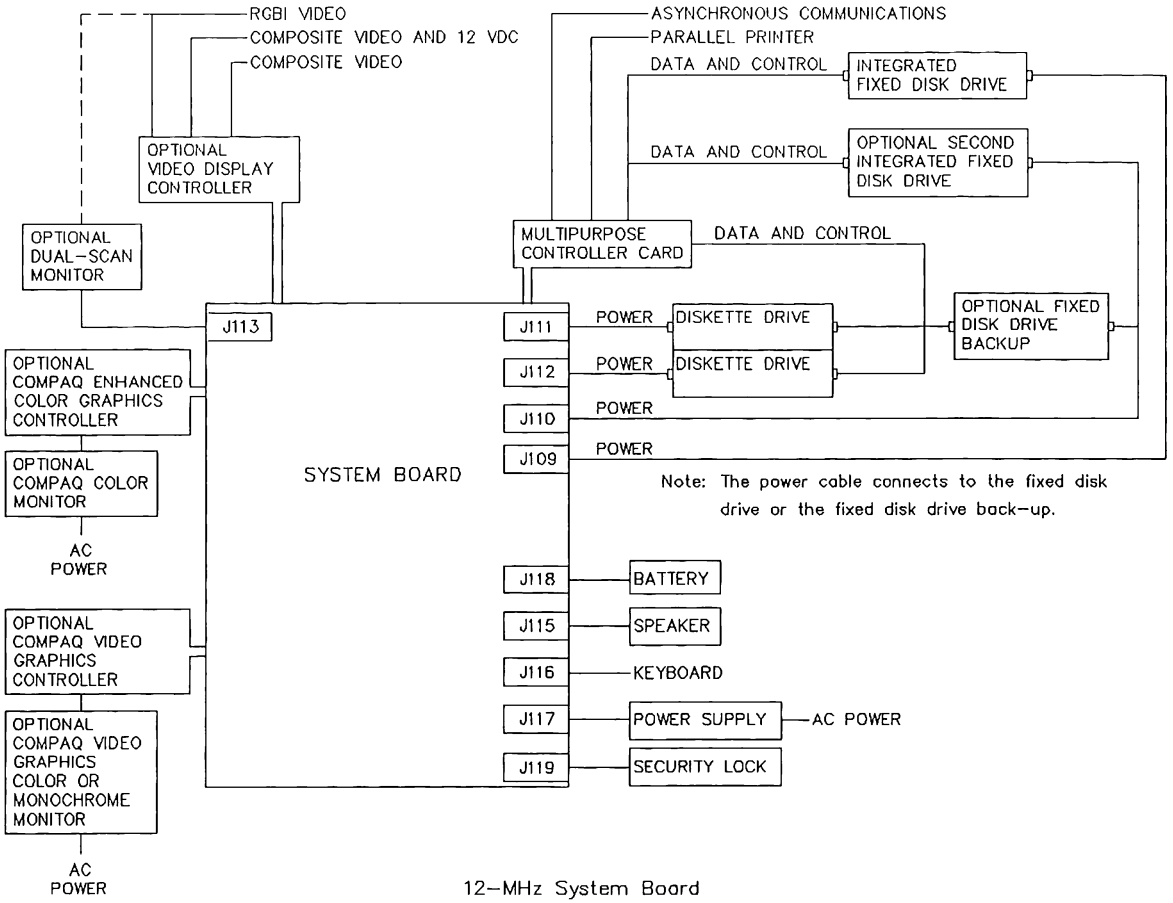

Figure 1-7. 12-MHz COMPAQ DESKPRO 286 Interconnection Diagram

1.7 INTRODUCTION TO THE INTEL 80286 MICROPROCESSOR

The Intel 80286 is is a 16-bit microprocessor compatible with the Intel 8088 and 8086 processors. The enhancements include greater speed, multitasking and multiuser capabilities, and an on-chip virtual-memory management unit.

80286 Software Concepts

The 80286 has two modes of operation: the Real mode and the Protected mode.

Real Mode

In the Real mode, the 80286 operates with the same memory limitations as the 8086 processor. That is, the 80286 addresses 1 Megabyte of memory using only the 20 least-significant bits of the 24-bit address bus.

Protected Mode

In Protected mode, the 80286 operates in a virtual-memory environment. It uses the full 24-bit address bus to directly address as many as 16 megabytes of real memory. In the virtual-memory environment, programs can specify 1 billion memory locations (1 gigabyte).

A disk operating system capable of virtual-memory operation transfers data in blocks so that a specified 30-bit virtual-memory location is addressed within the 24-bit real memory space. To use this mode, an operating system capable of managing the Protected mode must be loaded into the system.

80286 Hardware Concepts

The 80286 is a 68-pin very-large-scale integrated (VLSI) circuit that serves as the central processor.

The 80286 uses three buses: a 24-bit address bus, a 16-bit data bus, and a control bus to communicate with and control the rest of the system.

All devices outside the 80286 are addressed as either memory-mapped devices or I/O-mapped devices. The M/IO- signal specifies whether a memory-mapped or I/O-mapped device or location is being addressed. Tables 1-5 and 1-6 list the system memory map and I/O map, respectively.

Table 1-5. System Memory Map

Address Range(h)	Allocated Space	Assigned Use (If Any)
000000-09FFFF	640 KB	System Board Memory (See Note 1)
0A0000-0BFFFF	128-KB Video Memory	Reserved Graphics Buffer Area
0C0000-0DFFFF	128-KB ROM	I/O Expansion ROM
0E0000-0EFFFF	64-KB ROM	System ROM Set 2 (Optional)
0F0000-0FFFFF	64-KB ROM	System ROM Set 1
100000-FDFFFF	15-MB RAM	Expansion Memory
FE0000-FFFFFF	128-KB ROM	Contents are the same as 0E0000-0FFFFF (See Note 2)

Notes:
1. The COMPAQ DESKPRO 286 System Board Version 1 base memory is located on the COMPAQ DESKPRO 286 System Memory Board. The memory for the PORTABLE 286; the COMPAQ DESKPRO 286 with System Board Version 2, and the 12-MHz system board reside on the system memory board.
2. The system ROM can be addressed within either memory space. Memory decoding selects the ROM when these addresses are used. This arrangement is for software compatibility purposes.

Table 1-6. System I/O Map

	Range(h)	Function Addressed
SYSTEM BOARD	000-01F	DMA Controller 1
	020-03F	Interrupt Controller 1
	040-05F	Interval Timer (8254-2)
	060-06F	Keyboard Controller
	070-07F	Real-Time Clock, NMI
	080-08F	DMA Memory Page Register
	0A0-0BF	Interrupt Controller 2
	0C0-0DF	DMA Controller 2
	0F0	Clear 80287 Coprocessor
	0F1	Reset 80287 Coprocessor
	0F8-0FF	80287 Command Ports
CONTROLLER BOARDS	170-177	Fixed Disk Drive Controller 2
	1F0-1F7	Fixed Disk Drive Controller 1
	200-207	Game I/O
	278-27F	Parallel Port 3
	2F8-2FF	Serial Port 2 (COM2)
	300-31F	Not Used
	370-377	Multipurpose Drive or Multipurpose Fixed Disk Controller 2
	378-37F	Parallel Port 2
	380-38F	Not Used
	3A0-3AF	Not Used
	3B0-3DF	Video Display Controller
	3BC-3BF	LPT1
	3F0-3F7	Multipurpose Drive or Multipurpose Fixed Disk Controller 1
	3F8-3FF	Serial Port 1 (COM1)

Note: I/O address bits A<15..10> are not decoded.

1.8 SYSTEM FEATURES

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 have the following external features:

- Indicators
- Switches
- Security Lock
- Fuses
- Connectors

LED Indicators

Light-emitting diodes (LED) indicators show the activity or the state of the system. LED indicators are associated with the following devices:

- 5.25-inch 1.2-Megabyte diskette drives: two-color LED indicator. The light is red during read or write operations in the low-density mode (360-KB diskettes). The light is green during read or write operations in the high-density mode (1.2-Megabyte diskettes). The LED is white when no access is in progress.
- 3.5-inch 360-Kbyte diskette drives and fixed disk drive backup system: LED indicator that lights when the drive is accessed.
- 3.5-inch 1.44-Megabyte diskette drives: two-color LED indicators. The light is orange during read or write operation in a low-density mode (720 Kbyte diskettes) or in a high-density mode (1.44-Megabtye diskette).
- Fixed disk drive: LED indicator that lights when the fixed disk drive is in use. The LED color depends on the fixed disk drive type.
- The keyboard: three LED indicators that show the current state of the CAPS LOCK, NUM LOCK, and SCROLL LOCK key functions.

Security Lock

Each system has a security lock on the front to prevent unauthorized use of the computer (also shown in Figures 1-7 and 1-8). When the security lock is engaged, the computer ignores any input from the keyboard. The security lock on the COMPAQ DESKPRO 286 also locks in place the system unit cover.

Switches

Each system has a single AC power switch that turns all system power on or off. The COMPAQ PORTABLE 286 power switch is located on the left side of the system near the fan, as shown in Figure 1-9. The COMPAQ DESKPRO 286 power switch is located on the rear right corner of the system, as shown in Figure 1-11.

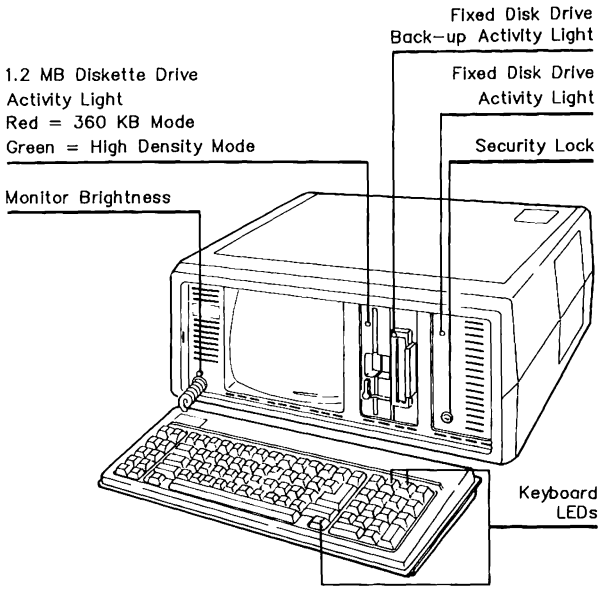

Figure 1-8. COMPAQ PORTABLE 286 Front View

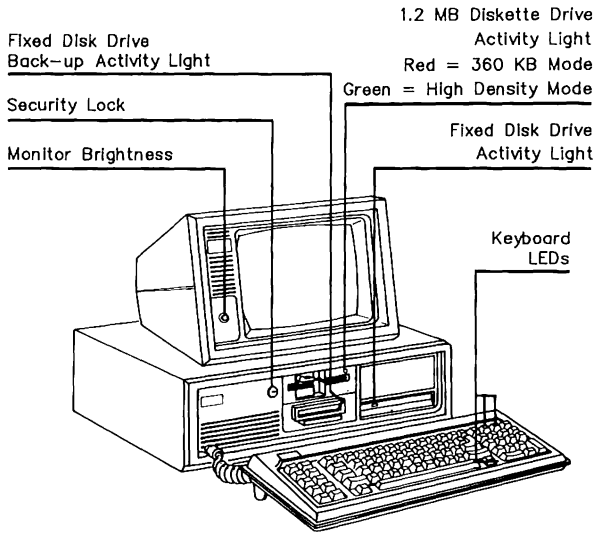

Figure 1-9. COMPAQ DESKPRO 286 Front View

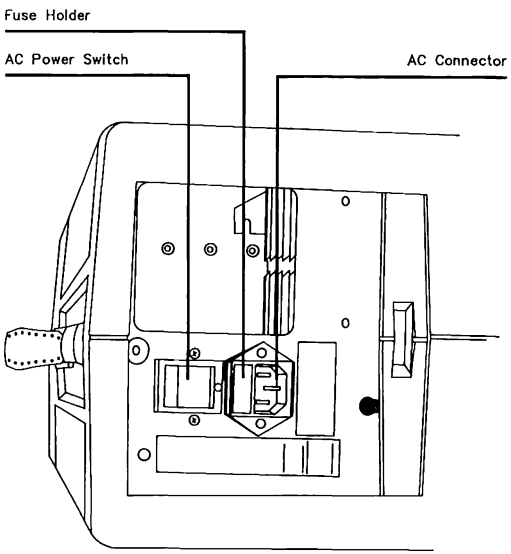

Figure 1-10. COMPAQ PORTABLE 286 Left Side View

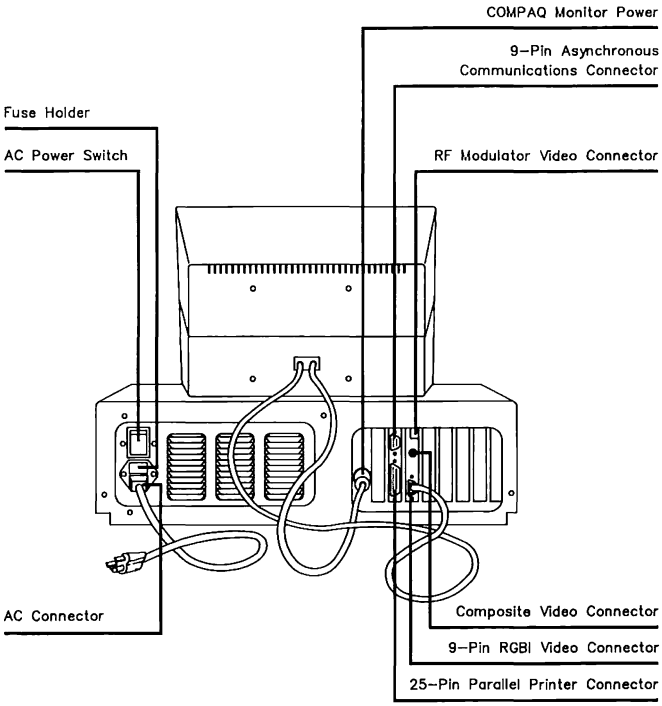

Figure 1-11. COMPAQ DESKPRO 286 Rear View

Fuses

Each system has a fuse on its AC power input for system protection. This fuse is in a removable housing that also contains a spare fuse, as shown in Figures 1-12 and 1-13.

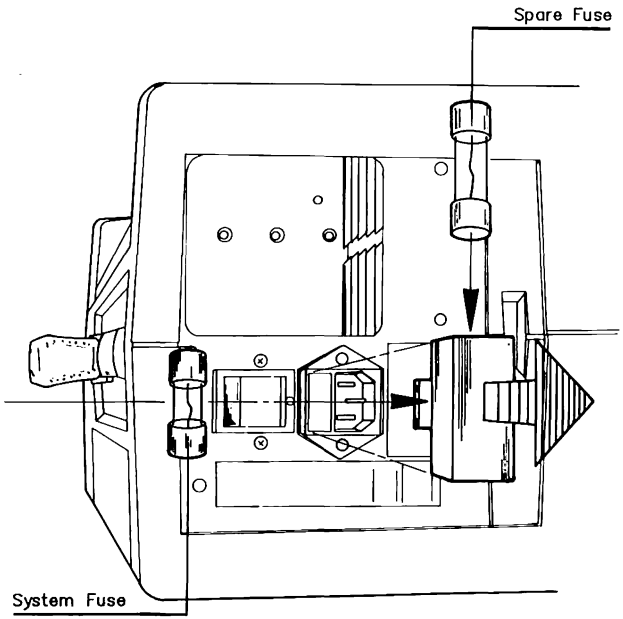

Figure 1-12. COMPAQ PORTABLE 286 Fuse Holder with Spare

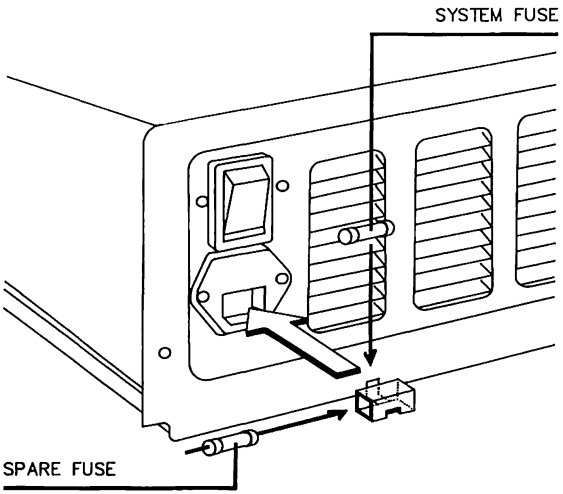

Figure 1-13. COMPAQ DESKPRO 286 Fuse Holder with Spare

Table 1-7 lists the fuse type required by each system.

Table 1-7. COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Fuse Types

	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286	COMPAQ DESKPRO 286 (12 MHz)
U.S.	3 A, 125 VAC	4 A, 125 VAC	5 A, 125 VAC
International	2.5 A, 250 VAC	2.5 A, 250 VAC	4 A, 250 VAC

1.9 CONNECTIONS

Each system has several connectors for peripheral devices, such as printers, modems, and monitors. Refer to Figure 1-11 for the locations of the COMPAQ PORTABLE 286 connectors. Refer to Figure 1-14 for the locations of the COMPAQ DESKPRO 286 connectors

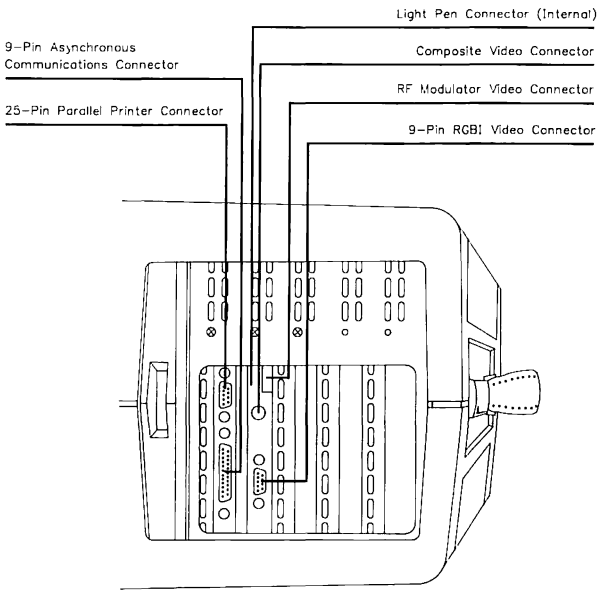

Figure 1-14. COMPAQ PORTABLE 286 Right Side View

Chapter 2

SYSTEM BOARDS

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Chapter 2, Part 1

SYSTEM BOARDS (8 AND 6 MHz ONLY)

Chapter 2
SYSTEM BOARDS

2.1 INTRODUCTION

This chapter contains a block diagram discussion of the theory of operation for COMPAQ® personal computers with an 80286 Central Processing Unit (CPU) operating at 8- and 12-MHz. This chapter is divided into two parts to differentiate between the systems. The two parts are:

- PART 1: SYSTEM BOARDS (8- and 6- MHz Only)
- PART 2: SYSTEM BOARD (12-MHz Only)

Both parts of this chapter discuss CPU and CPU support circuitry, memory system, programmable devices, and expansion bus and bus functions as well as subsections discussing miscellaneous board information, jumpers, and connectors.

Chapter 2, PART 1
SYSTEM BOARDS (8 AND 6 MHZ ONLY)

2.2 CPU AND CPU SUPPORT

The CPU and CPU support circuitry control and monitor the system.

The memory system controls access to and from the system Random Access Memory (RAM) and access from the system Read-Only Memory (ROM).

Programmable devices are hardware devices integrated on the system board that can be controlled or monitored by software.

The expansion bus and bus functions allow system access to hardware options that may be installed in the system. Hardware options may include display controllers, communications devices, and additional memory.

Also included in this chapter are discussions of:

- Miscellaneous System Board Information, such as fuses and indicators
- Jumpers
- Connectors
- Schematics

The 80286 microprocessor uses three busses, the 24-bit address bus, the 16-bit data bus, and the control bus to communicate with and control the system.

All devices outside the 80286 Central Processing Unit (CPU) are addressed either as memory-mapped devices or I/O-mapped devices.

The 80286 is reset when power is applied to the system board or after pressing the CTRL, ALT, and DEL keys simultaneously. After the CPU is reset, it addresses the ROM for instructions. The initial boot instructions in ROM check the system RAM and ROM for errors (checksums), and then initialize the system.

System initialization, or restart of the system, includes loading the programmable devices, such as the keyboard controller, the video controller, the RAM, and the with the desired starting values.

After initializing the system, the CPU loads the Disk Operating System (DOS) into memory from the diskette or fixed disk drive. The DOS is a program that manages and provides a consistent programming interface to the hardware.

Figure 2-1 is a functional block diagram of the 8- and 6-MHz system boards.

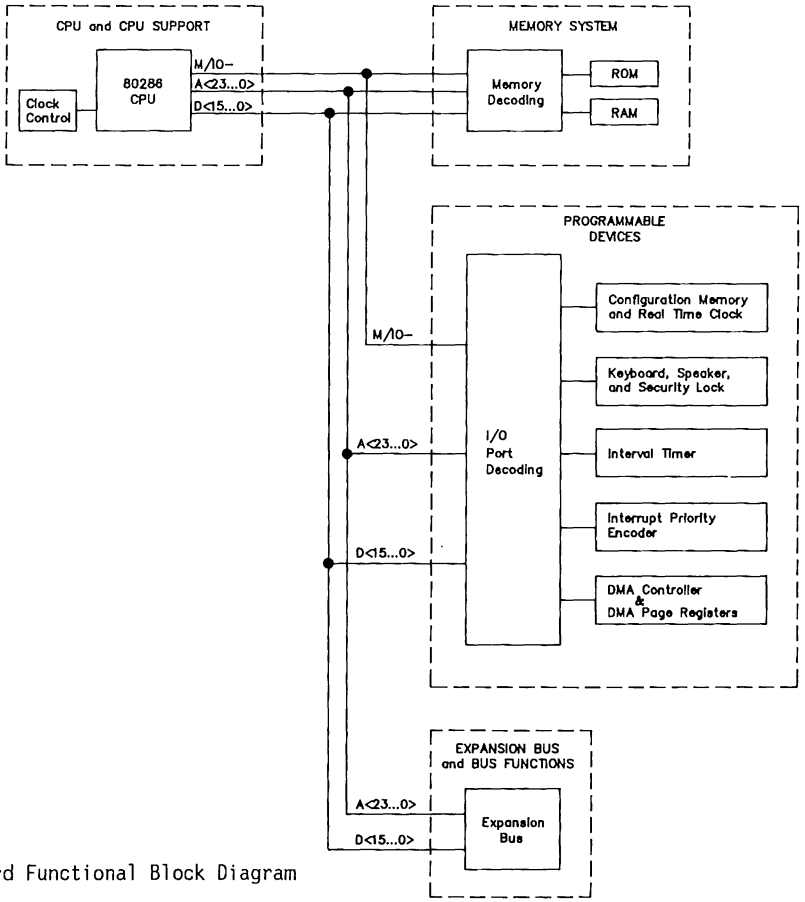


Figure 2-1. System Board Functional Block Diagram

Figure 2-2 shows a functional block diagram of the CPU and CPU support circuitry.

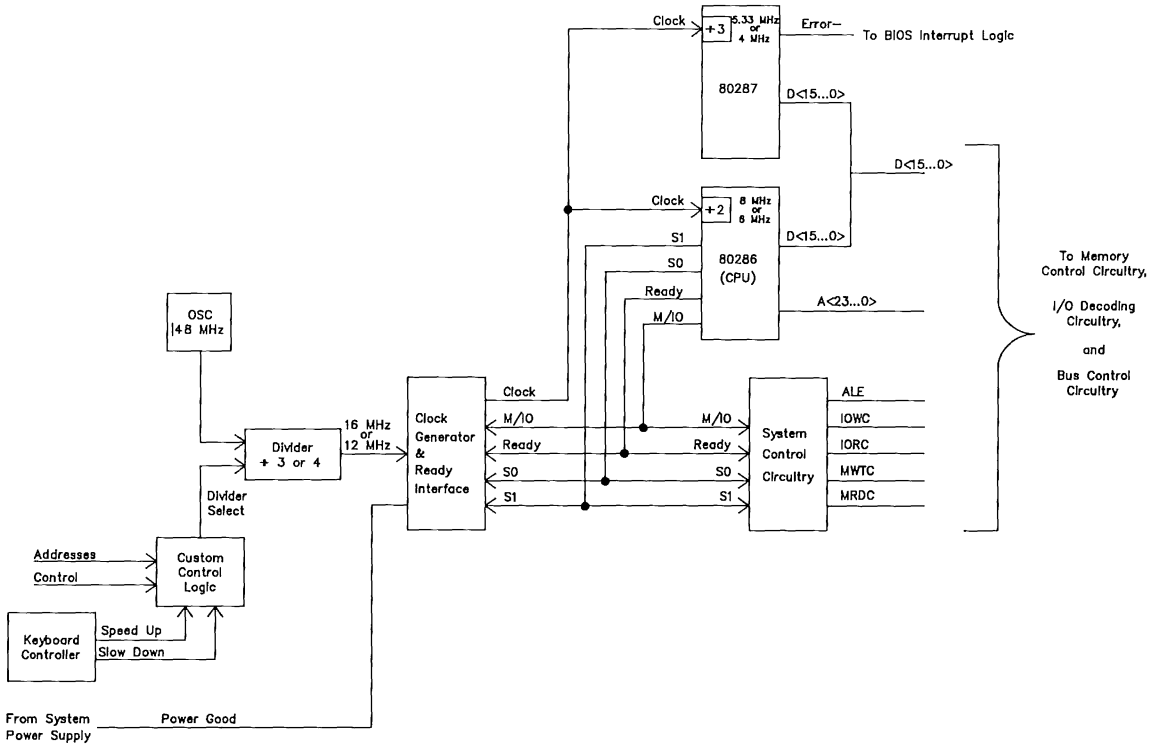


Figure 2-2. CPU and CPU Support Circuitry Block Diagram

Clock Generator and Ready Interface

The Clock Generator and READY Interface receives an input clock signal from an oscillator circuit and generates the clock signal for the 80286 CPU, the 80287 coprocessor, and the system control circuitry. The Clock Generator and READY Interface also monitors the power good (PWRGOOD) signal from the system power supply to control the system reset functions.

System Control Circuitry

The system control circuitry decodes the status signals S0, S1, and M/IO- (and other inputs such as CEN/AEN, READY-, et. al.) to control the system bus.

Table 2-1 shows the bus cycle status definition for the status signals.

Table 2-1. Bus Cycle Status Definition

M/IO-	S1	S2	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read (Ports)
0	1	0	I/O Write (Ports)
0	1	1	None: Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

80287 Math Coprocessor (Optional)

The 80287 Math Coprocessor is a high-performance numeric processor extension of the 80286, adding floating point, extended integer, and BCD data-type support.

The 80287 automatically executes all numeric instructions as they are encountered. The 80287 responds to particular I/O addresses (00F8h, 00FAh, and 00FCh) that are automatically generated by the 80286.

The ERROR- signal of the 80287 is connected to IRQ13 (INT 75h). The BIOS interrupt handler for INT 75h routes this interrupt to INT 02h, which is the actual routine for coprocessor exceptions. This method is used to provide compatibility with 8088/8086 coprocessor exceptions and to prevent interference with the video I/O interrupt, INT 10h.

A socket is provided on the system boards for the 80287. A unique feature of the coprocessor is the ability to run at 4.0 or 5.33 MHz.

Clock Function

The COMPAQ 80286-Based Personal Computer products offer the choice of an 8MHz system clock for superior processing speed, or a 6MHz system clock to maintain compatibility with slower systems.

General Timing Information

The CPU status signals (S0, S1, and M/IO) are decoded by the CPU support circuitry to produce the command strobes used by the rest of the system (ALE, IOWC, IORC, MWTC, and MRDC).

2.3 MEMORY SYSTEM

Memory Address Decoding

The 80286 uses addresses <A23...A0> and control line M/IO- to specify memory locations. The address and control lines are decoded to specify memory areas for the system RAM and ROM.

Expansion boards such as memory, disk, or video must have their own devices to decode the I/O or memory space for that board.

Figure 2-3 shows a simplified block diagram of memory address decoding for the system board.

The memory decoder uses the REFRESH-, MRDC-, MWTC-, BALE, and LA23 to LA17 address lines to generate the MEM16-, RAM-, ROM-, RAS-, and CAS- signals.

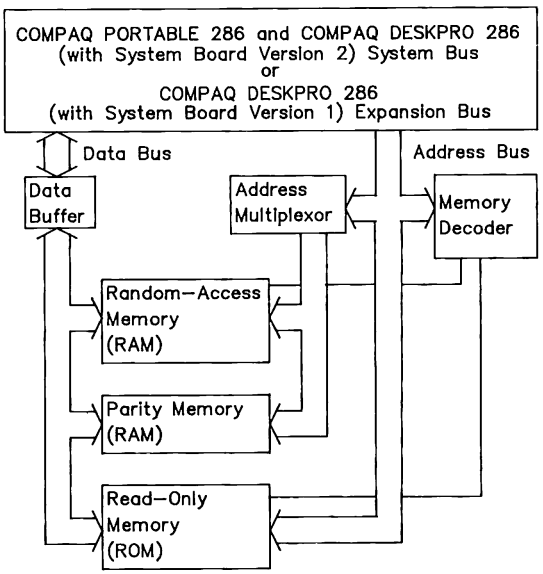


Figure 2-3. Memory Address Decoding Simplified Block Diagram

The 16-bit 80286 microprocessor (CPU) can read data from memory as bytes (8 bits), or words (16 bits). When a word on an an even boundary is read, an even numbered address is given by the CPU, and that address and the one above it are simultaneously read (Figure 2-4).

Two CPU cycles are required to read a word on an odd boundary. The next-lower even-numbered address is first given by the CPU, and the high-order byte of that location becomes the low-order 8 bits of the word. Then, the next-higher even-numbered address is given by the CPU, and the low-order byte of that location becomes the high-order 8 bits of the word.

Odd—numbered, High—order Byte	Even—numbered, Low—order Byte
Byte FFFFh (64K)	Byte FFFEh (64K—1)
.	.
.	.
.	.
Byte 0003h	Byte 0002h
Byte 0001h	Byte 0000h

Figure 2-4. A 16-Bit Word Divided into Two Bytes

Memory Support

Dynamic memory chips (RAM) require support circuitry to:

- Control the chips, using the CAS-, RAS-, and WR- signals
- Multiplex the address lines into the RAM
- Buffer the data lines
- Refresh the memory cells

The delay line generates the ENDRAS and STARTCAS signals and the signals that control the address multiplexing.

Two AM2966 chips buffer the address lines, and sequentially present the high- and low-order address lines to the RAM. The delay line controls the timing for this multiplexing operation.

Two 74LS245 chips buffer the data between the RAM and the data bus.

Memory refresh is accomplished by discrete circuitry. During memory refresh, every cell of every memory location is recharged.

COMPAQ PORTABLE 286 Memory System

The COMPAQ PORTABLE 286 system board has two banks for RAM (Bank 0 and Bank 1), two 16K x 8bit system ROMs, and two sockets for additional ROM. A bank of memory consists of 18 RAM devices located in two rows of 9.

COMPAQ PORTABLE 286 RAM

The COMPAQ PORTABLE 286 system board comes with 128 KB of RAM soldered in the first bank (Bank 0). The second bank (Bank 1) is socketed so that either 64K x 1-bit or 256K x 1-bit RAMs can be used.

Installing eighteen 64K x 1-bit RAMs in Bank 1 increases the total system board memory to 256 KB. Installing eighteen 256K x 1-bit RAMs in Bank 1 increases the memory to the maximum size of 640 KB.

If the COMPAQ PORTABLE 286 is purchased with 64K x 1-bit RAMs in Bank 1, then the jumper 'MS' is installed between pins 1 and 2 (Total RAM = 256KB). If 256K x 1-bit chips are used to replace the 64K x 1-bit chips in Bank 1, then move the jumper 'MS' to pins 2 and 3 (Total RAM = 640 KB).

If the COMPAQ PORTABLE 286 is purchased with 256K x 1bit RAMs in Bank 1, then the jumper 'MS' is installed between pins 2 and 3 (Total RAM = 640 KB).

In this model, a different decoding device (MEMPAL) is used, and when the jumper 'MS' is set between pins 1 and 2 the system disables the upper 128 KB of memory, reducing the total addressable RAM to 512 KB. This option is for use with certain software packages that will not run with more than 512 KB of system RAM.

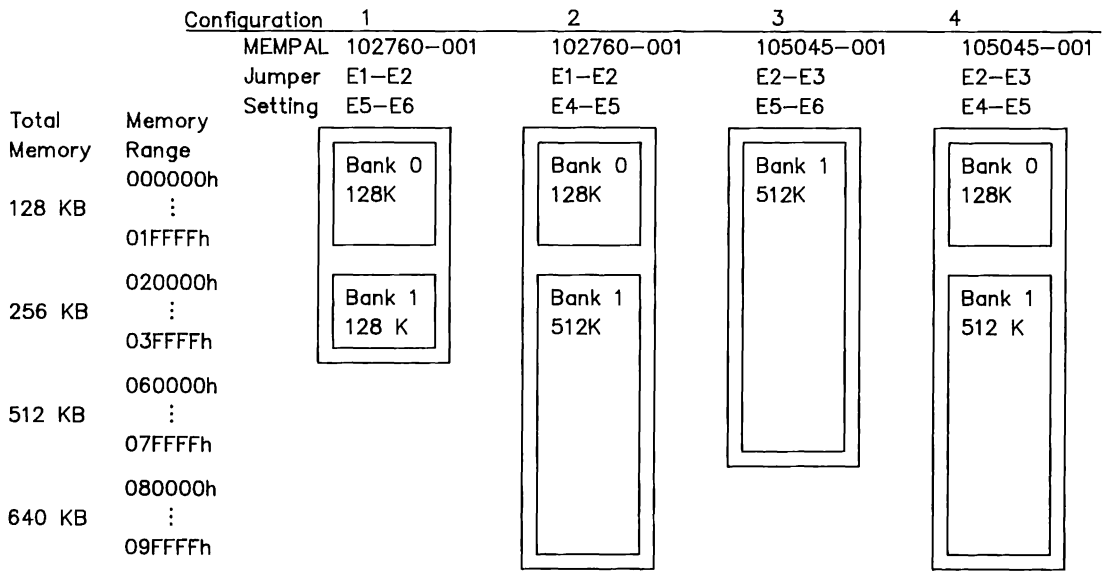
The system board uses approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

There are four possible memory configurations for the memory on the COMPAQ PORTABLE 286 system board:

1. 0-256 Kbytes using 64K x 1-bit dynamic RAMS (STANDARD Model 1).
2. 0-640 Kbytes by adding 256K x 1-bit dynamic RAMs to the Model 1.
3. 0-512 Kbytes using 256K x 1-bit dynamic RAMs, with Bank 0 disabled.
4. 0-640 Kbytes using 256K x 1-bit dynamic RAMs with all the memory enabled (STANDARD Model 2).

In every configuration, the lowest 128 KB of RAM is permanently installed (soldered in) as Bank 0.

Figure 2-5 shows the relationship between the memory map and the installed RAM.



Notes: 1. Configurations 2 and 4 are identical except for the MEMPAL type used.
2. For configuration 3, Bank 0 remains physically installed, but disabled. For this configuration only, address 000000h begins in Bank 1.

Figure 2-5. COMPAQ PORTABLE 286 Memory Configurations

COMPAQ PORTABLE 286 ROM

The COMPAQ PORTABLE 286 system board has four 28-pin sockets for ROM (or EPROM). The ROM sockets are addressed as two pairs, each 16 bits wide. The ROM pairs are designated ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and ROM Set 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 contains the BIOS that initializes and controls the system. Installed in the ROM Set 1 sockets are 16K x 8-bit devices, one containing all even bytes and the other containing all odd bytes. The ROM Set 2 sockets are empty and provide for future enhancement.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8-bit in size and may be either static and dynamic. Table 2-2 lists the jumper settings and resulting configuration for each type of ROM device.

Table 2-2. Jumper Settings for System ROMs

ROM Set 1 Jumper Settings			ROM Type
E13-E14	E10-E11	E16-E17	8Kx8, Static ROM, 250 ns
E14-E15	E10-E11	E16-E17	16Kx8, Static ROM, 250 ns
E13-E14	E11-E12	E16-E17	Invalid
E14-E15	E11-E12	E16-E17	32Kx8, Static ROM, 250 ns
E13-E14	E10-E11	E17-E18	8Kx8, Dynamic ROM, 150 ns
E14-E15	E10-E11	E17-E18	16Kx8, Dynamic ROM, 150 ns
E13-E14	E11-E12	E17-E18	Invalid
E14-E15	E11-E12	E17-E18	32Kx8, Dynamic ROM, 150 ns

ROM Set 2 Jumper Settings			ROM Type
E7-E8	E4-E5	E19-E20	8Kx8, Static ROM, 250 ns
E8-E9	E4-E5	E19-E20	16Kx8, Static ROM, 250 ns
E7-E8	E5-E6	E19-E20	Invalid
E8-E9	E5-E6	E19-E20	32Kx8, Static ROM, 250 ns
E7-E8	E4-E5	E20-E21	8Kx8, Dynamic ROM, 150 ns
E8-E9	E4-E5	E20-E21	16Kx8, Dynamic ROM, 150 ns
E7-E8	E5-E6	E20-E21	Invalid
E8-E9	E5-E6	E20-E21	32Kx8, Dynamic ROM, 150 ns

There are no jumper headers or plugs; the jumpers are etched on the solder side of the board in the following configurations:

ROM Set 1: 16K x 8-bit Static ROM (E14-E15, E10-E11, E16-E17)

ROM Set 2: 32K x 8-bit Dynamic ROM (E8-E9, E5-E6, E20-E21)

Changing the jumper settings requires cutting the conductors on the bottom side of the board to disconnect any unwanted jumpers, and soldering wire(s) to connect the jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

SYSTEM ROM Set 1 occupies the 64 KB space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. SYSTEM ROM Set 2 occupies the 64 KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K x 8-bit devices are used, the pair of ROMs fill the entire 64KB address space. When 16K x 8-bit devices are used, the most significant address bit is not decoded, so the ROMs are double mapped into two identical 32 KB sections of the 64 KB address space.

Similarly, when 8K x 8-bit devices are used, the two most significant address bits are not decoded, so the ROMs are mapped into four identical 16 KB sections of the 64 KB address space.

The system tests for the memory size as part of the Power-On Self-Test and compares this value with configuration memory. Errors detected cause the system to enter the SETUP program, if the diagnostic diskette or another diskette containing SETUP is installed.

COMPAQ DESKPRO 286 Memory System

The COMPAQ DESKPRO 286 Version 1 memory ROM and RAM are provided on a separate adapter board. See Chapter 3, "COMPAQ DESKPRO 286 System Memory Board" for more information.

The COMPAQ Deskpro 286 Version 2 system board has five banks for RAM, two 16K x 8-bit system ROMS, and two sockets for additional ROM.

COMPAQ DESKPRO 286 RAM

The COMPAQ DESKPRO 286 Version 2 System Board has 128 KB of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAMS may be used. Memory must be expanded in full-bank increments (18 RAM chips) in contiguous and ascending order, using the same RAM type (64K or 256K).

SW1 position 1 indicates the type of RAM in banks 1 through 4. When banks 1 through 4 are filled with 64K x 1-bit RAMS, SW1 position 1 must be CLOSED. When banks 1 through 4 are filled with 256K x 1-bit RAMS, SW1 position 1 must be OPEN.

NOTE: When SW1 position 1 is closed, positions 4 and 5 must both be open.

SW1 positions 2 and 3 limit the amount of base memory on the system board so that conflicts with expansion memory boards can be avoided. These two switches limit memory as shown in Table 2-3 regardless of the type of RAM in banks 1 through 4.

Table 2-3. Base Memory Size Switch Settings

SW1 Position 2	SW1 Position 3	(1) Total Base Memory	Address Range
CLOSED	CLOSED	Disabled RAM and ROM on System Board	
CLOSED	OPEN	256k	0-256 KB
OPEN	CLOSED	512k	0-512 KB
OPEN	OPEN	640k	0-640 KB

Notes: 1. Total Base Memory indicates maximum addressable base memory on the system board regardless of amount of RAM installed.
2. CLOSED = ON
OPEN = OFF

SW1 positions 4 and 5 enable/disable banks 2 through 4. These switches should be used to limit the amount of expansion memory on the system board when 256K x 1-bit RAMS are used to fill banks 1 through 4. (See Table 2-4).

Table 2-4. Expansion Memory Size Switch Settings

SW1 Pos 4	SW1 Pos 5	Banks Enabled	(1) Total Expansion Memory	Address Range
CLOSED	CLOSED	none	none	
CLOSED	OPEN	2	512K	1.0-1.5 MB
OPEN	CLOSED	2&3	1024K	1.0-2.0 MB
OPEN	OPEN	2,3,&4	1536K	1.0-2.5 MB

Notes: 1. Total Expansion Memory indicates maximum addressable expansion memory on the system board regardless of amount of RAM installed.
2. SW1 positions 4 and 5 should both be OPEN when 64K x 1-bit RAMS are used to fill banks 1 through 4 to ensure that SW1 positions 2 and 3 operate correctly.
3. CLOSED = ON
OPEN = OFF

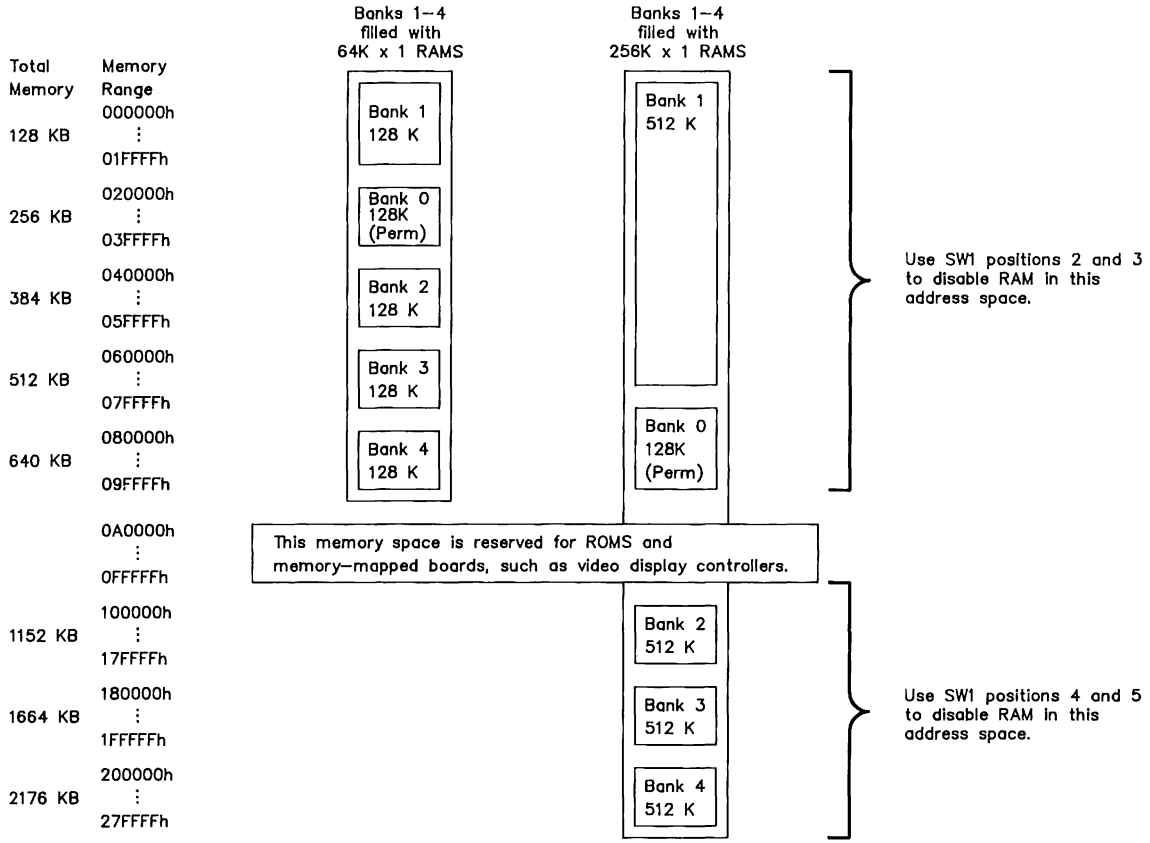


Figure 2-6. COMPAQ DESKPRO 286 Version 2 System Board Memory Configurations

The system board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

COMPAQ DESKPRO 286 Version 2 System Board ROM

The COMPAQ DESKPRO Version 2 System Board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (Basic Input Output System). Installed in the two ROM Set 1 sockets are 16K x 8-Bit devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and are provided for future expansion.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64KB space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64 KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K X 8-bit ROMs are used, the pair of ROMs fill the entire 64 KB address space. When 16K x 8-bit ROMs are used, the most-significant address bit is not decoded, so the ROMs are double-mapped into two identical 32 KB sections of the 64 KB address space.

Similarly, when 8K x 8-bit ROMs are used, the two most- significant address bits are not decoded, so the ROMs are quadruple-mapped into four identical 16 KB sections of the 64 KB address space.

Jumpers

Two jumpers (E1 and E2) are provided to enable use of a variety of types of ROM for special applications.

Table 2-5 shows the jumper settings and resulting configuration for each type of ROM.

Table 2-5. Jumper Settings for ROM Sets 1 and 2

ROM Set 1 = E1
ROM Set 2 = E2

Jumper Settings			ROM Type
1-2	4-5	7-8	8K x 8, Static ROM, 250 ns
2-3	4-5	7-8	16k x 8, Static ROM, 250 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32k x 8, Static ROM, 250 ns
1-2	4-5	8-9	8k x 8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16k x 8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32k x 8, Dynamic ROM, 150 ns

There are no jumper headers installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

ROM Set 1:16K x 8-bit Static ROM (E1: 2-3, 4-5, 7-8)

ROM Set 2:32K x 8-bit Dynamic ROM (E2: 2-3, 5-6, 8-9)

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering wire(s) to jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

2.4 PROGRAMMABLE DEVICES

The system BIOS controls the following system board programmable devices:

- Direct Memory Access (DMA) Controllers
- DMA Memory Page Register
- Real-Time Clock and Configuration Memory
- Keyboard Controller
- Interval Timer
- Interrupt Priority Encoder

These devices are all I/O mapped. Commands and opcodes are directed to the appropriate device by the I/O Port Decoding circuitry. Table 2-6 summarizes the port addresses used by the devices on the system board.

Table 2-6. System Board I/O Map

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
00h..0Fh	0 0	0 0 0 x	Y Y Y Y	8237A-5 Byte DMA Controller
20h..21h	0 0	0 0 1 x	x x x Y	8259A Interrupt Controller 1
40h	0 0	0 1 0 x	x x 0 0	8254-2 System Clock (Timer 0)
41h	0 0	0 1 0 x	x x 0 1	8254-2 Refresh Request (Timer 1)
42h	0 0	0 1 0 x	x x 1 0	8254-2 Speaker Tone (Timer 2)
43h	0 0	0 1 0 x	x x 1 1	8254-2 Command Mode Register
60h	0 0	0 1 1 0	x 0 x 0	8042 Date I/O Register
61h	0 0	0 1 1 0	x x x 1	Port B/C Input/Outputs
64h	0 0	0 1 1 0	x 1 x 0	8042 Status/Command Register
70h	0 0	0 1 1 1	x x x 0	RTC Address Register (bits <5..0>)
70h	0 0	0 1 1 1	x x x 0	NMI Enable Register (bit <7>)
71h	0 0	0 1 1 1	x x x 1	RTC Data I/O Register
80h	0 0	1 0 0 x	0 0 0 0	DMA Page Register Spare
81h	0 0	1 0 0 x	0 0 0 1	DMA Page Register CH 2 Page
82h	0 0	1 0 0 x	0 0 1 0	DMA Page Register CH 3 Page
83h	0 0	1 0 0 x	0 0 1 1	DMA Page Register CH 1 Page
84h	0 0	1 0 0 x	0 1 0 0	DMA Page Register Spare
85h	0 0	1 0 0 x	0 1 0 1	DMA Page Register Spare
86h	0 0	1 0 0 x	0 1 1 0	DMA Page Register Spare
87h	0 0	1 0 0 x	0 1 1 1	DMA Page Register CH 0 Page
88h	0 0	1 0 0 x	1 0 0 0	DMA Page Register Spare

(Continued)

Table 2-6. (Continued)

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
89h	0 0	1 0 0 x	1 0 0 1	DMA Page Register CH 6 Page
8Ah	0 0	1 0 0 x	1 0 1 0	DMA Page Register CH 7 Page
8Bh	0 0	1 0 0 x	1 0 1 1	DMA Page Register CH 5 Page
8Ch	0 0	1 0 0 x	1 1 0 0	DMA Page Register Spare
8Dh	0 0	1 0 0 x	1 1 0 1	DMA Page Register Spare
8Eh	0 0	1 0 0 x	1 1 1 0	DMA Page Register Spare
8Fh	0 0	1 0 0 x	1 1 1 1	DMA Page Register Refresh Page
A0h..A1h	0 0	1 0 1 x	x x x Y	8259A Interrupt Controller 2
C0h..CFh	0 0	1 1 0 Y	Y Y Y x	8237A-5 Word DMA Controller
F0h	0 0	1 1 1 x	0 x x 0	Clear Math Processor Busy
F1h	0 0	1 1 1 x	0 x x 1	Reset Math Processor
F8h..FFh	0 0	1 1 1 1	1 Y Y x	80287 Command Ports

Notes: 1. x = Don't care. The value of these bits does not affect the I/O address decoding.
2. Y = Register dependent.

I/O Port Decoding

The 80286 uses address (A<15...0>) and control lines (M/IO-) to specify I/O operations. Although the 80286 uses 16 bits for an I/O address, the system board and expansion boards use only 10 bits (A<9...0>), therefore I/O space is limited to 3FFh. The address and control lines are decoded to specify I/O and addresses for the system board I/O-mapped devices (DMA controllers, real-time clock, interval timer, etc.).

Expansion boards such as memory, disk, and video must have their own devices to decode the I/O-mapped devices for that board. Figure 2-7 shows a simplified block diagram of I/O port decoding for the system board.

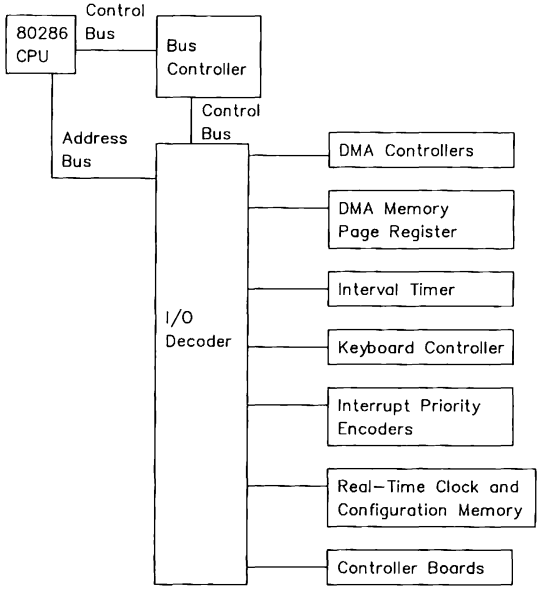


Figure 2-7. I/O Address Decoding Simplified Block Diagram

Direct Memory Access Controller

Direct Memory Access (DMA) is a method of directly accessing memory without involving the CPU. DMA is normally used to transfer blocks of data to or from an I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

The system board uses two Intel 8237 DMA controllers, with four bidirectional data channels each. The DMA controllers operate at half the system clock rate (8 MHz/2 or 4 MHz/2). Table 2-7 lists the function assigned to each DMA channel.

Table 2-7. DMA Channels Assigned to the Controllers

Controller 1 (Byte Transfers)	
Channel	Function
0	Spare
1	SDLC (Communications)
2	Diskette Data Transfers
3	Spare
Controller 2 (Word Transfers)	
Channel	Function
4	Cascade for Controller 1
5	Spare
6	Spare
7	Spare

The DMA controllers hold (or define) only 16 bits of the 24-bit address. The other 8 address bits are contained in the DMA Memory Page Register (74LS612) or MAP Gate Array. See the "DMA Memory Page Register" section for more information.

DMA Controller 1 is used for byte (8-bit) data transfers (Figure 2-8). DMA Controller 2 is used for word (16-bit) data transfers. Unlike the CPU, DMA Controller 2 can only transfer words on an even boundary.

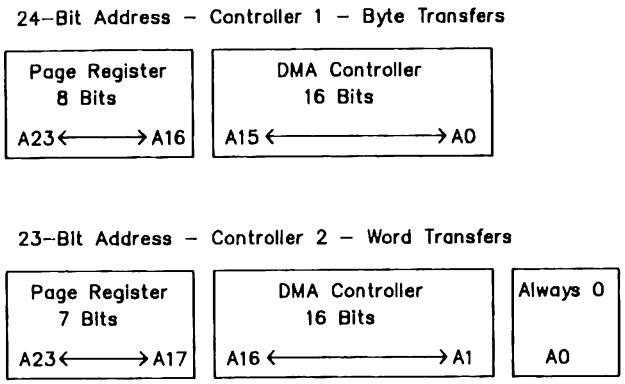


Figure 2-8. Memory Address Derived from Page Register and DMA Register Contents

A16 from the DMA memory page register is disabled when DMA Controller 2 is selected. A0 is not connected to DMA Controller 2. A0 is always 0 when word-length transfers are selected. This arrangement (not connecting A0) means that the size of the block of data that can be moved or addressed is measured in 16-bit words, rather than 8-bit bytes.

Since the DMA controllers only contain 16 bits of the 24-bit address, they can only move blocks of data within their ability to address that data. DMA Controller 1 can move up to 64K bytes of data. DMA Controller 2 can move up to 64K words, or 128K bytes of data.

The DMA controllers are complex devices with several registers for commands and status. Table 2-8 shows the I/O-map and the commands and formats of the registers.

Transferring Data from I/O Devices to Memory

DMA controllers and I/O devices use the DRQx and DAKx signals as "handshaking". When an I/O device has a byte or word of data to send, the I/O device makes its DRQx line active. When the DAKx line from the DMA controller goes active, the device puts its data on the data bus.

Transferring Data from Memory to Memory

The hardware does not support memory-to-memory block transfers.

NOTE: After power-on, it is recommended that all command, mode, and mask registers be loaded with valid values to ensure proper operation of the device.

Table 2-8. DMA Controller Registers

Register Function	Bits	Port Addresses Cntlr 1	Cntlr 2	Read/Write
Status	8	08h	D0h	Read
Command	8	08h	D0h	Write
Mode	6	0Bh	D6h	Write
Write Single Mask Bit	4	0Ah	D4h	Write
Write All Mask Bits	4	0Fh	DEh	Write
Software DRQx Request	4	09h	D2h	Write
Base And Current Address - CH 0	16	00h	C0h	Write
Current Address - CH 0	16	00h	C0h	Read
Base & Current Word Count - CH 0	16	01h	C2h	Write
Current Word Count - CH 0	16	01h	C2h	Read
Base And Current Address - CH 1	16	02h	C4h	Write
Current Address - CH 1	16	02h	C4h	Read
Base & Current Word Count - CH 1	16	03h	C6h	Write
Current Word Count - CH 1	16	03h	C6h	Read
Base And Current Address - CH 2	16	04h	C8h	Write
Current Address - CH 2	16	04h	C8h	Read
Base & Current Word Count - CH 2	16	05h	CAh	Write
Current Word Count - CH 2	16	05h	CAh	Read
Base And Current Address - CH 3	16	06h	CCh	Write
Current Address - CH 3	16	06h	CCh	Read
Base & Current Word Count - CH 3	16	07h	CEh	Write

Note: See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.

(Continued)

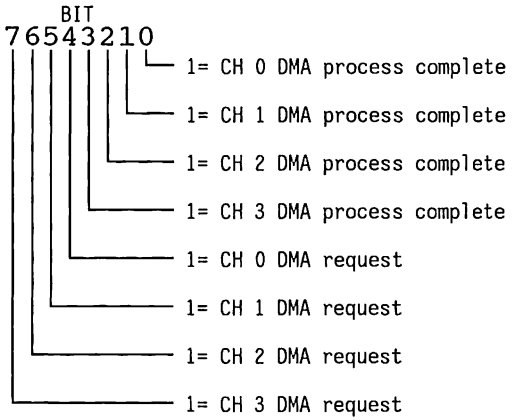
Table 2-8. (Continued)

Register Function	Bits	Port Addresses Cntrl 1	Cntrl 2	Read/Write
Current Word Count - CH 3	16	07h	CEh	Read
Temporary	16	0Dh	DAh	Read
Reset Pointer Flip-flop	(Note 1)	0Ch	D8h	Write
Master Reset	(Note 1)	0Dh	DAh	Write
Reset Mask Register	(Note 1)	0Eh	DCh	Write

Notes: 1. This is not a register, but a direct command to the DMA Controller.
2. See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.

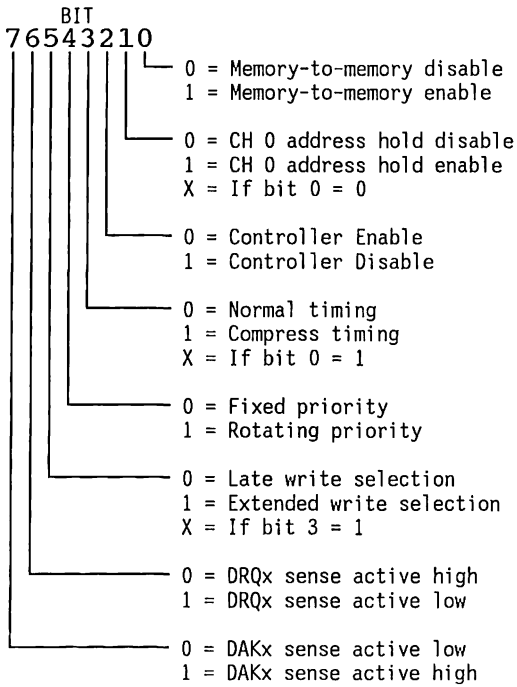
STATUS

The Status register bits are set (= 1) to indicate that a channel has requested DMA access or that a DMA process is complete.



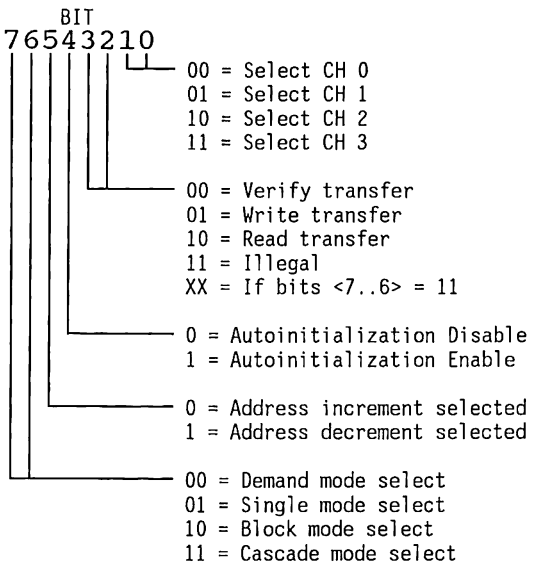
COMMAND

The command register bits control the DMA operation. All bits are reset (=0) by the master clear instruction or a system reset. This register must be programmed to 00 for proper system operation.



MODE

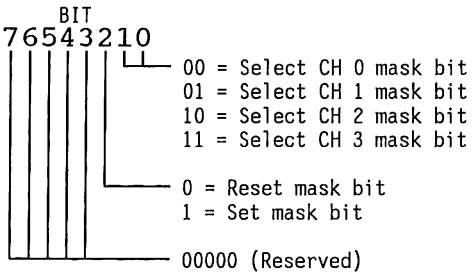
Each channel has a 6-bit register associated with it. The first two bits of the byte written to this register specify which channel is being selected. These registers specify the operating mode for each channel.



If the BLOCK or DEMAND mode is selected for a channel, the total transfer time must not exceed 15 us or RAM will not be properly refreshed.

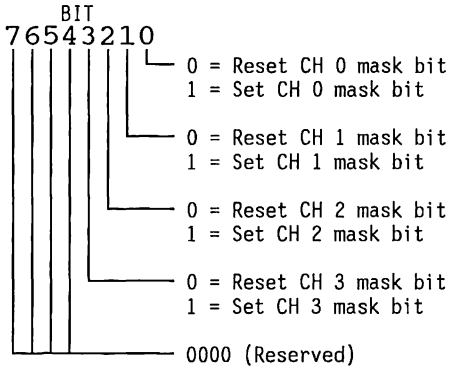
WRITE SINGLE MASK BIT

This command sets (=1) or resets (=0) a single mask bit. When a mask bit is set, that channel's DRQx is disabled. The "WRITE ALL MASK BITS" command can set or reset all the mask bits.



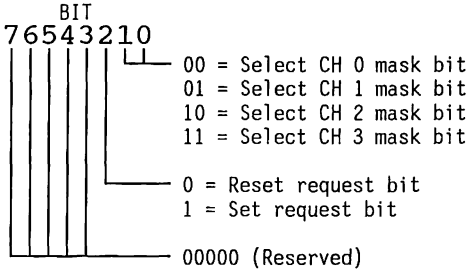
WRITE ALL MASK BITS

This command sets (=1) or resets (=0) all the mask bits. When a bit is set, that channel's DRQx is disabled. The "WRITE SINGLE MASK BIT" command can set or reset a single mask bit.



SOFTWARE DRQx REQUEST

The DMA controller can respond to software requests for DMA as well as hardware requests from DRQx lines. The channel must be in the block mode, and the appropriate registers (base addresses and so forth) must be set before initiating this request.



BASE AND CURRENT ADDRESS - CHANNELS 0-3

These 16-bit registers specify the starting destination address for the memory transfer. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation. The first write to this register loads the eight least-significant bits. The second consecutive write loads the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

CURRENT ADDRESS CHANNELS 0-3

These 16-bit registers specify either the current address, or the destination address for the next data transfer. This address is the same as the base address, plus address increments or decrements made after each data transfer. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the eight least-significant bits. The second consecutive read returns the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

BASE AND CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words to be transferred. This is a write-only register. The 16-bit contents are loaded into these registers as a two-part operation.

The first write to this register loads the eight least-significant bits. The second consecutive write loads the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit registers specify the number of words already moved as part of a data block. These are read-only registers. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the eight least- significant bits. The second consecutive read returns the eight most-significant bits. See the "RESET POINTER FLIP-FLOP" command.

TEMPORARY

This register is not used in this hardware configuration.

RESET POINTER FLIP-FLOP

This is a direct command to the DMA controller to reset the pointer flip-flop that keeps track of 16-bit data transfers. This command is given to reset the pointer to a known state so that the DMA controller will load the high- and low-order bytes in the proper sequence. Use this command before writing a 16-bit base address or other 16-bit command or data to the DMA controller.

MASTER RESET

This is a direct command to the DMA controller to reset the DMA controller It has the same effect as a hardware reset; the command, status, request, temporary, and pointer flip-flop registers are reset (=0), and the mask register bits are set (=1).

RESET MASK REGISTER

This is a direct command to the DMA controller to reset the mask register, enabling all four channels to receive DRQs (data requests).

DMA Memory Page Register

The DMA memory page register contains the eight most significant bits of the 24-bit address. It works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 2-9 shows the port address assigned to each page register. See the section on the DMA controllers for more information.

Table 2-9. Port Address For DMA Channels

DMA Channel	Page Register I/O Port Address
0	087h
1	083h
2	081h
3	082h
4	None
5	08Bh
6	089h
7	08Ah
Refresh	08Fh (See Note)

Note: The DMA memory page register for the refresh channel must be programmed with 00h for proper system operation.

Real-Time Clock and Configuration Memory

The COMPAQ 286 family computer system boards use the Motorola MC146818 device as their Real-Time Clock (RTC) and Configuration Memory. This device has a total of 64 bytes of memory. The first fourteen memory locations are used for the RTC. The remaining 50 memory locations are used for the system configuration.

A value can be written to or read from all 64 registers except:

- Status Registers C and D, which are read-only
- Bit 7 of Status Register A, which is read-only
- The high-order bit of the seconds byte, which is read-only

Figure 2-9 shows the memory map for the MC146818.

To prevent a loss of time or system configuration, the MC146818 uses power obtained from a battery mounted on the inside of the computer. The battery maintains the time and system configuration during power loss for up to three years. The system does NOT charge the battery.

NOTE: If the battery is disconnected or fails for any reason, the time and system configuration must be reprogrammed into the MC146818.

To reset the time or system configuration, run the SETUP procedure found on the USER'S PROGRAM diskette or on the Advanced Diagnostics Diskette. To reset the time, use either the SETCLOCK (DOS) command, or the appropriate INT 1Ah (BIOS) command.

The MC146818 is an I/O mapped device. Use the 80286 OUT and IN instructions to read or write to the memory in this device. Note that the port 70h is shared between the NMI mask register and the configuration memory address register. To leave the NMI mask enabled, make sure that bit 7 is set to 0 when writing a RTC address to port 70h.

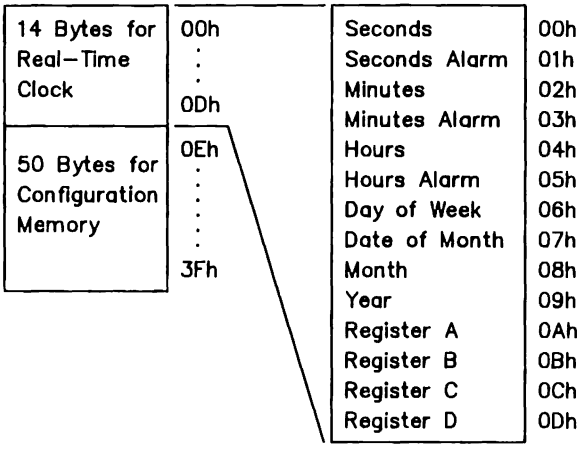


Figure 2-9. MC146818 Memory Map

To write a value into memory:

1. Use OUT 70h, AL to specify the memory location to change. 70h is the port number; AL is the memory location.
2. Use OUT 71h, AL to specify the data for the memory location. 71h is the port number; AL is the data.

To read the contents of a memory location:

1. Use OUT 70h, AL to specify the memory location to read. 70h is the port number; AL is the memory location.
2. Use IN AL, 71h to read data stored in that location. The returned data is placed in the AL register of the 80286.

Table 2-10 summarizes the types of information stored in the MC146818's memory locations.

Table 2-10. MC146818 Real-Time Clock Memory Locations

Register	Function
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hour
05h	Hour Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Status Register A
0Bh	Status Register B
0Ch	Status Register C
0Dh	Status Register D
0Eh	Diagnostic Register
0Fh	Reset Code Byte
10h	Diskette Drive Type
11h	Reserved
12h	Fixed Disk Drive Type
13h	Reserved
14h	Equipment Installed
15h,16h	System Board Memory Size
17h,18h	Extended Memory Installed

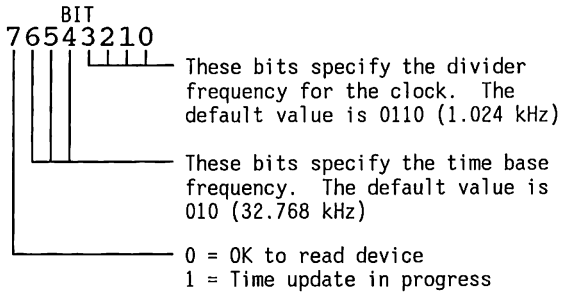
(Continued)

Table 2-10. (Continued)

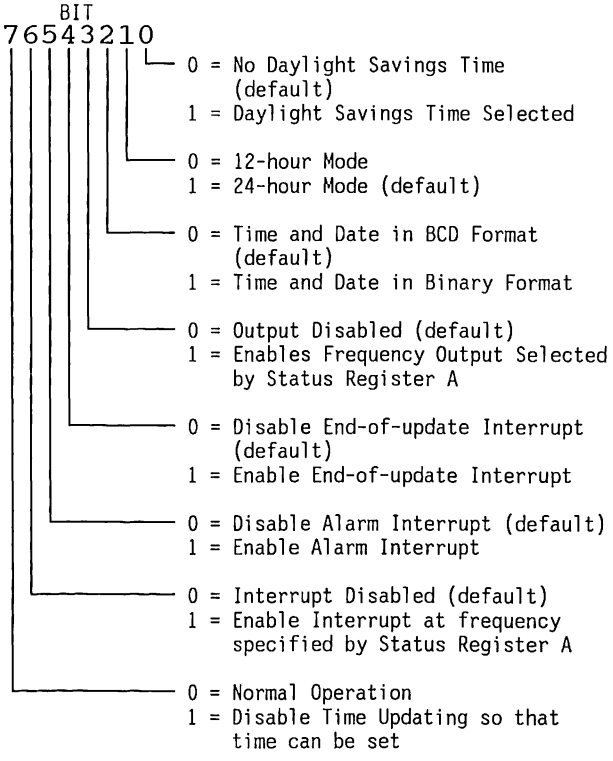
Register	Function
19h-2Ch	Reserved
2Dh	Additional Flags
2Eh,2Fh	Checksum Value
30h,31h	Memory More than 1 MB
32h	Century, part of time and date function
33h	System Information
34h-3Fh	Reserved

Information about registers 0Ah through 33h follows.

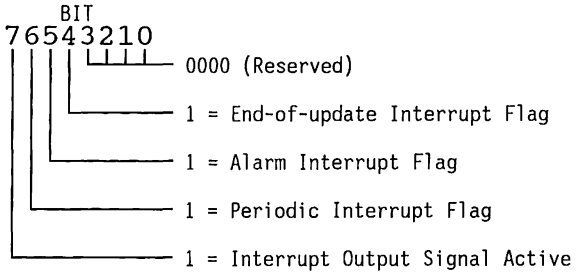
STATUS REGISTER BYTE 0Ah



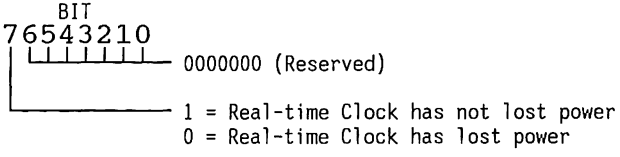
STATUS REGISTER BYTE 0Bh



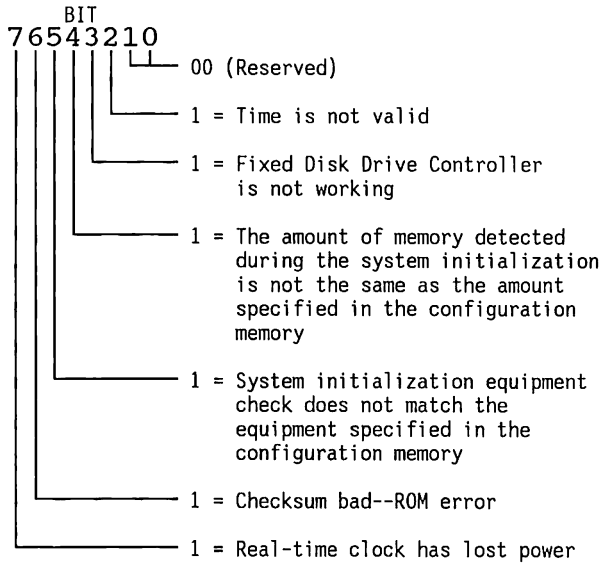
STATUS REGISTER BYTE 0Ch--READ-ONLY



STATUS REGISTER BYTE 0Dh

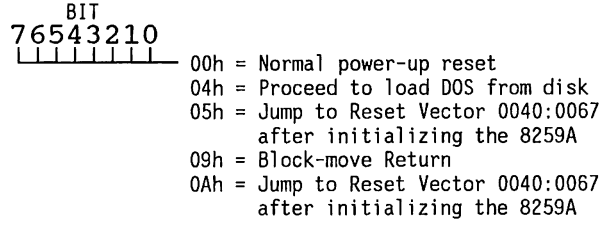


CONFIGURATION BYTE 0Eh--DIAGNOSTIC STATUS BYTE

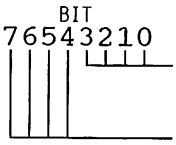


CONFIGURATION BYTE 0Fh--RESET CODE BYTE

The reset code tells the system what to do after the CPU is reset. The reset code identifies the type of, or reason for, reset. The reset code also provides a method of resetting the system without losing previously-stored data or to return the system to the Real Mode from the Protected Virtual Memory Mode.



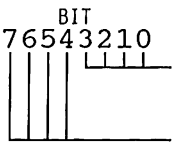
CONFIGURATION BYTE 10h--DISKETTE DRIVE TYPE



Secondary Diskette Drive Type
(use values given below)

Primary Diskette Drive Type:
0000 = No diskette drive
0001 = 360-Kbyte Diskette Drive
0010 = 1.2-Megabyte Diskette Drive
0011 = Reserved
:
1111 = Reserved

CONFIGURATION BYTE 12h--FIXED DISK DRIVE TYPE



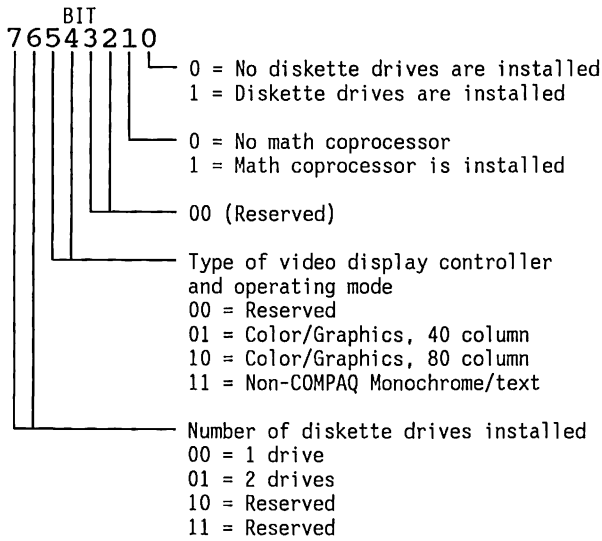
Value defines second fixed disk dirve type
(use table below)

Values defines fixed disk drive type:

Value	Size	System
0000	None	
0010	20-MB	COMPAQ PORTABLE 286
0010	20-MB	COMPAQ DESKPRO 286
0110	30-MB	COMPAQ DESKPRO 286
1100	70-MB	COMPAQ DESKPRO 286

NOTE: This byte identifies the type of fixed disk drive used, not the capacity.

CONFIGURATION BYTE 14h--EQUIPMENT INSTALLED



CONFIGURATION BYTES 15h AND 16h--BASE MEMORY SIZE

Value indicates valid memory sizes for the base memory size:

Byte 16h	Byte 15h	Memory Size
00h	80h	128 KB
01h	00h	256 KB
02h	00h	512 KB
02h	80h	640 KB

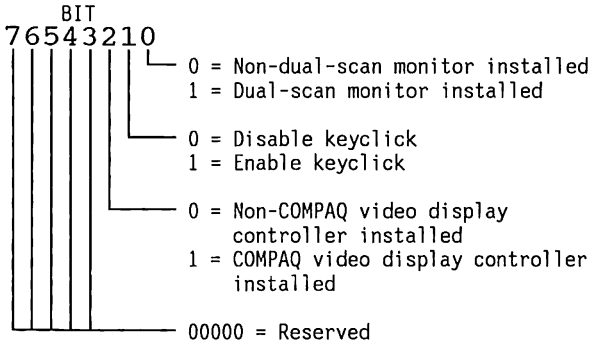
CONFIGURATION BYTES 17h AND 18h--MEMORY AMOUNT

Value indicates valid memory sizes for memory on all memory option boards:

Byte 18h	Byte 17h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
.	.	
.	.	
3Bh	80h	15232 KB

CONFIGURATION BYTE 2Dh--ADDITIONAL FLAGS

This byte allows the configuration of special features.



CONFIGURATION BYTES 2Eh AND 2Fh--MEMORY CHECKSUM

Value stored is the checksum for memory addresses 10h..2Dh.

Byte 2Eh = High byte of checksum

Byte 2Fh = Low byte of checksum

CONFIGURATION BYTES 30h AND 31h--MEMORY OVER 1 MB

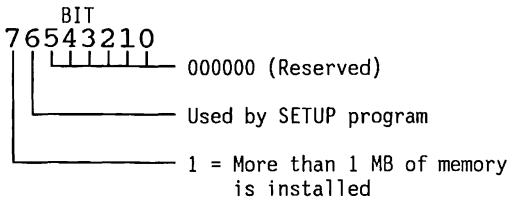
Value indicates amount of system memory in excess of 1 MB. These bytes are updated by the BIOS at power-on.

Byte 31h	Byte 30h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
08h	00h	2048 KB
0Ah	00h	2560 KB
0Ch	00h	3072 KB
0Eh	00h	3584 KB
10h	00h	4096 KB
12h	00h	4608 KB
14h	00h	5120 KB
16h	00h	5632 KB
18h	00h	6144 KB
1Ah	00h	6656 KB
1Ch	00h	7168 KB
1Eh	00h	7680 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 32h--DATE, CENTURY

This is the century part of the current time and date encoded in BCD (binary coded decimal). The BIOS sets and reads this value.

CONFIGURATION BYTE 33h--SYSTEM INFORMATION



Keyboard Controller

An INTEL 8042 single-chip microcomputer provides:

- An output port for system function control and keyboard communication
- An input port to read system function status
- A test port to read the status of the keyboard clock and data lines

The 8042 has internal ROM that is custom-programmed with keyboard scan codes and operating instructions. Figure 2-10 shows a simplified block diagram of the keyboard controller.

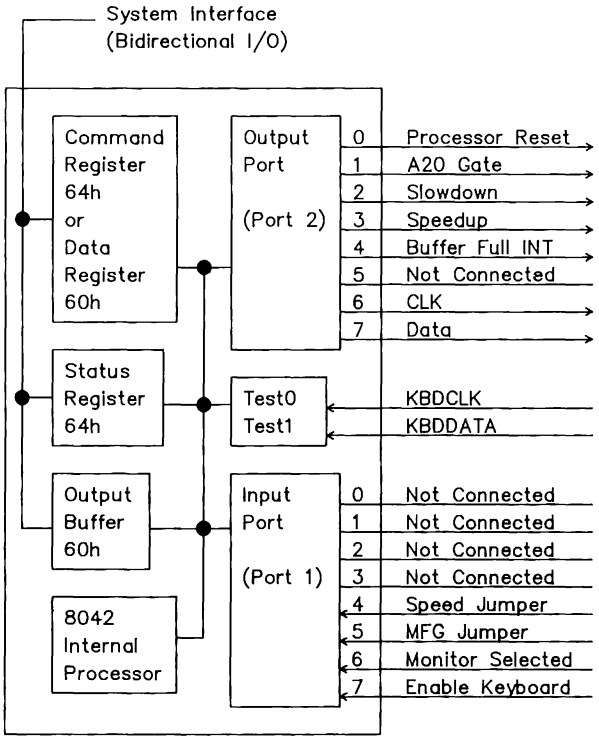


Figure 2-10. Keyboard Controller Functional Block Diagram

The 8042 communicates with the keyboard in a bidirectional, serial format with a synchronizing clock. The 8042 receives serial data, checks its parity, translates the 11- or 9-bit scan codes from the keyboard into system codes, and interrupts the 80286 to transfer data into the system.

Command codes between the 8042 and the keyboard are described in Chapter 8.

The 8042-to-Keyboard Interface

The 8042 and the keyboard are connected by a four conductor, shielded cable that carries a power line, a ground line, a data signal, and a clock signal.

The 8042 and the keyboard communicate in a handshaking fashion, using the data and clock lines for synchronous serial communication. The data and clock lines are driven by open-collector drivers at both ends of the cable in a wired-OR fashion.

The keyboard supplies the synchronizing clock for data transmissions in either direction.

Figure 2-11 shows a simplified schematic of the data and clock circuits.

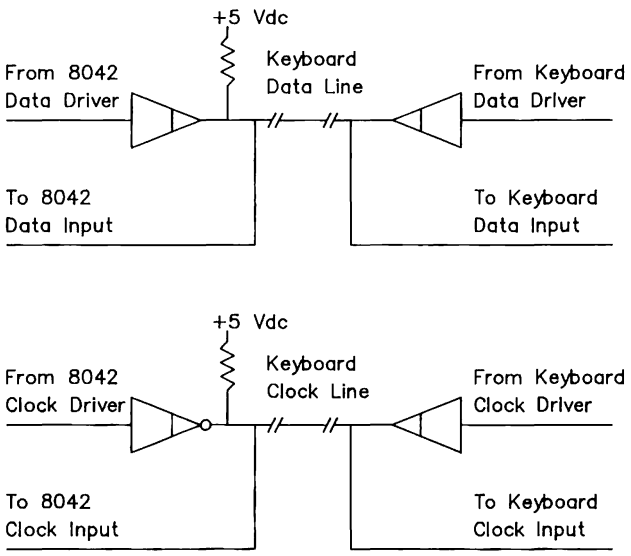
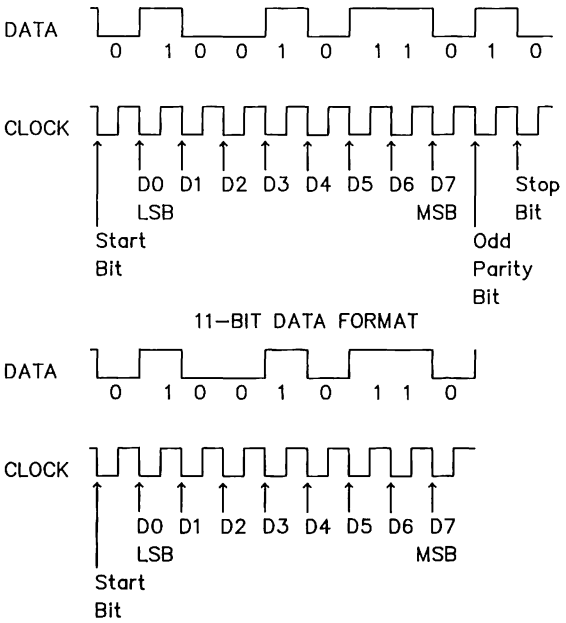


Figure 2-11. Simplified Schematic of the Data and Clock Circuits

11- or 9-Bit Data Transmission Format

The 8042 adds versatility to the system by allowing 11- or 9- bit keyboards to be used interchangeably at any time. The system sends commands to the 8042 to specify the type of scan code it expects, and the 8042 sends that type of scan code, regardless of the type of keyboard connected.

The 8042 automatically tests for keyboard type by monitoring the data format. Figure 2-12 shows 11- and 9- bit data formats with sample data transfers.



Note: The keyboard drives the data line low for the Stop Bit at the end of a transmission to acknowledge the transmission.

Figure 2-12. 11- and 9-Bit Data Formats

Table 2-11 lists the 11- and 9-bit data transfer timing parameters.

Table 2-11. Keyboard Data Timing Parameters

Parameter	11-Bit	9-Bit
Clock timing (min.), Falling edge to falling edge	60 us	25 us
Clock timing (min.), Falling edge to rising edge	5 us	5 us
Transmission Time (max.) First edge to completion	2 us	2 us
Time data must be valid before falling clock edge	0 us	0 us
Time data must be valid after falling clock edge	5 us	12 us

8042 Port Functions

The 8042 has three ports:

- An 8-bit output port for system function control and keyboard communication
- An 8-bit input port to read system function status
- A 2-bit test port to read the status of the keyboard clock and data lines.

To write to the output port:

1. Write command D1h (next byte is a value byte) to I/O address 64h.
2. Write the desired value for the output port to port address 60h.

To read the 8042 output port value:

1. Write command D0h (transfer the current output port values to the 8042 output buffer) to port address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-13 shows the bit values for the output port of the 8042.

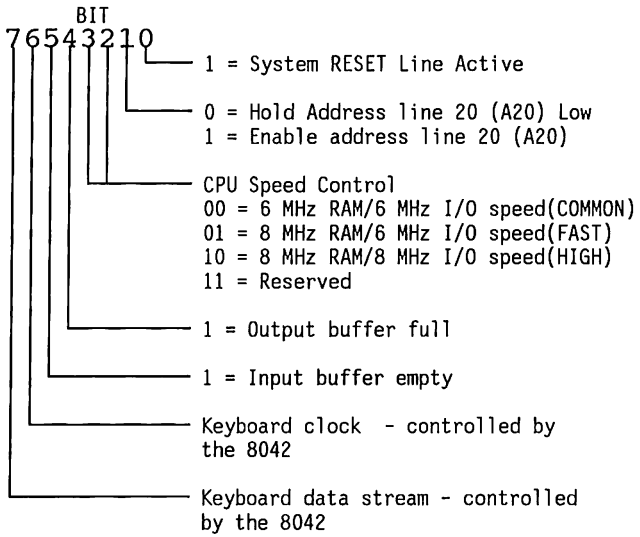


Figure 2-13. 8042 Output Port - Bit Definition

To read the 8042 input port value:

1. Write command C0h (transfer the current input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h) with the special read command A5h.

Figure 2-14 shows the format of the byte returned from the 8042 input port.

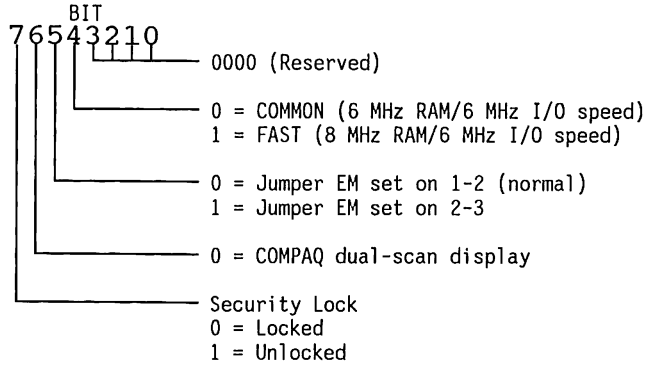


Figure 2-14. 8042 Input Port - Bit Definition

To read the 8042 TEST input port value:

1. Write the command E0h (transfer the current TEST input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-15 shows the format of the byte returned by the 8042 TEST input port.

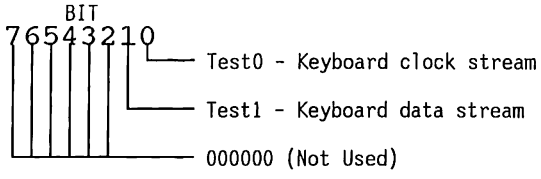


Figure 2-15. 8042 Test Input Port - Bit Definition

Programming the 8042

The 8042 is I/O-mapped at port addresses 60h and 64h.

Prior to writing a command or data to ports 60h or 64h, the 8042 Status register must indicate "Input Buffer Empty". Also, prior to reading data from port 60h, test the 8042 Status register to ensure a "Data in Buffer" condition.

Port 60h, Data I/O Register. Use the 80286's IN instruction to read data from the 8042's output buffer. Data in the Data I/O register is from the keyboard, unless the 8042 has been given a command such as 20h, Read Command byte.

Use the 80286's OUT instruction to send data to the keyboard, unless the 8042 has been given a multibyte command such as 60h, Write Command Byte. To give a multibyte command to the keyboard, write the first command byte to port 64h and the second command byte to 60h.

Port 64h, Command/Status Register. The following pages describe the format for Command/Status register (port 64h) I/O interactions with the 8042.

Use the 80286's IN instruction to read the status of the 8042 and the keyboard (input from port 64h).

Use the 80286's OUT instruction to give a command to the 8042 (output to port 64h). Writing to this address automatically sets the COMMAND/DATA flag to 1.

Most commands involve a single write step. However, some commands do require a second step, such as a subsequent 8042 register read or write.

Figure 2-16 shows the 8042 Status register. Figure 2-17 shows the 8042 command byte. Table 2-12 lists the 8042 command codes.

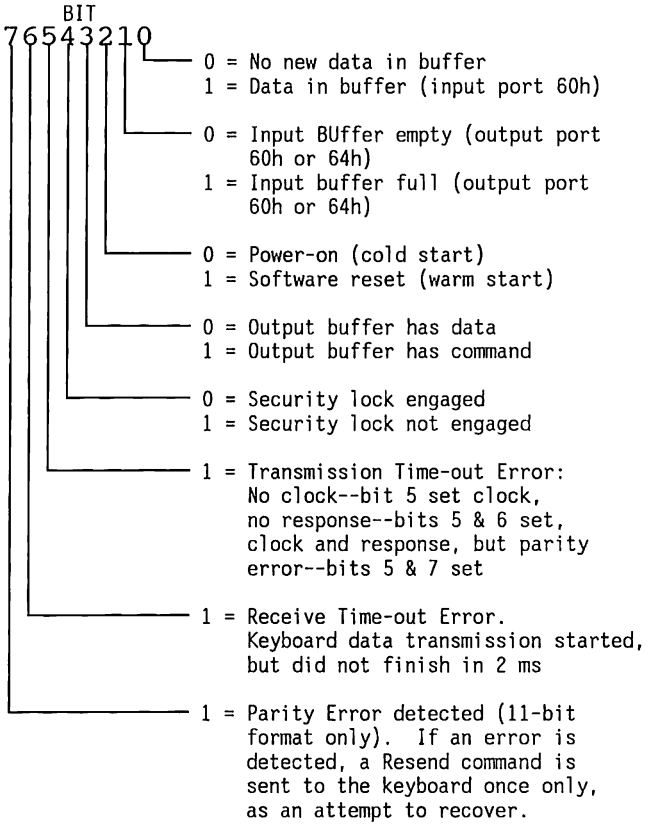


Figure 2-16. 8042 Status Register (Input Port 64h)

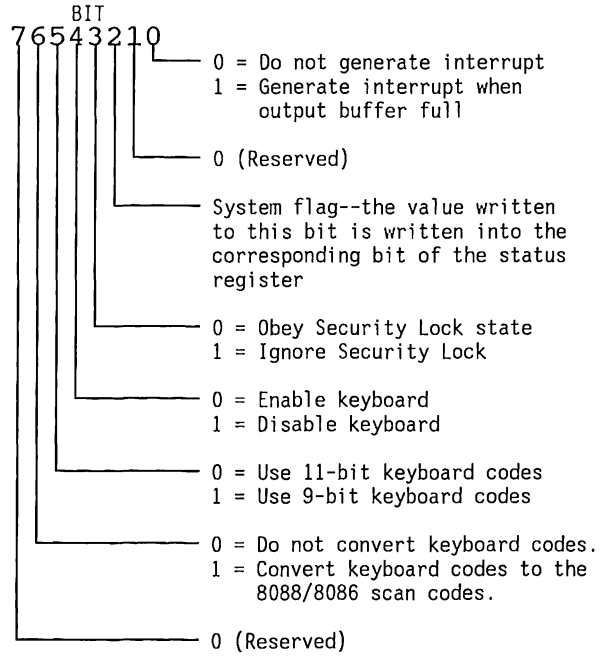


Figure 2-17. 8042 Command Byte (Output Port 64h).

Table 2-12. 8042 Command Codes (Output Port 64)

Code	Function
20h	Put the current command byte on the 8042's output port
60h	Load the next byte put into the 8042's input port as the command byte
A1h	COMMON Speed--the 8042 output port selects the 6-MHz RAM/6-MHz I/O speed (SLOWDOWN bit = 0 , SPEEDUP bit = 1.)
A2h	FAST Speed--the 8042 output port selects an address-dependent speed (SLOWDOWN bit and SPEEDUP bit = 1.)
A3h	HIGH Speed--the 8042 output port selects the 8-MHz RAM/8-MHz I/O speed (SLOWDOWN bit = 1 , SPEEDUP bit = 0.)
A4h	Toggle--the 8042 changes its speed-control output port bits between the COMMON mode speed and the speed defined with the HIGHSP command (A6h).
A5h	Special Read--the 8042 places the real value of port 2 except for bits 4 and 5 which are given a new definition in the output buffer. No output-buffer full is generated. If bit 5 = 0 then a 9-bit keyboard is in use If bit 5 = 1, then an 11-bit keyboard is in use If bit 4 = 0, the interrupt is disabled If bit 4 = 1, when the output buffer full interrupt is enabled
A6h	HIGHSP--the 8042 interprets the next byte written to port 60h as the maximum speed for the system when the Toggle command (A4h) is used. Value — Highest Speed 00h — COMMON (6 MHz RAM/6 MHz I/O speed) 01h — FAST (address-dependent 8 MHz RAM/6 MHz I/O speed) 02h — HIGH (8 MHz RAM/8 MHz I/O speed) Note: Only the two least-significant bits are used. The other bits should be set to 0.

(Continued)

Table 2-12. (Continued)

Code	Function
AAh	Initialization--the 8042 initializes ports 1 and 2 to their setup value, sets HIGHSP (CPU speed) to the value set by the jumper, disables the keyboard and clears the buffer pointers. It then places 55h in the output buffer.
ABh	Interface Test--directs the 8042 to test the data and clock lines of the keyboard interface. The output buffer (input port 60h) receives the test results, according to: 00h - No error detected 01h - The keyboard clock line is stuck low 02h - The keyboard clock line is stuck high 03h - The keyboard data line is stuck low 04h - The keyboard data line is stuck high 05h - COMPAQ diagnostic feature Note: The keyboard data line test does not check for line stuck low for 9-bit keyboards.
ACh	Diagnostic Dump--Reserved for diagnostic purposes.
ADh	Disable Keyboard--sets bit 4 of the 8042's command byte, which disables the keyboard interface. Data is not sent or received until the keyboard is enabled.
AEh	Enable Keyboard--resets bit 4 of the 8042's command byte, which enables the keyboard interface.
C0h	Read Input Port--directs the 8042 to transfer the status of the input port and place it in the output buffer (input port 60h). Use this command only when the output buffer is empty.
D0h	Read Output Port--directs the 8042 to transfer the current byte in the output port to the output buffer (input port 60h). The values for the SPEEDUP and SLOWDOWN bits (D6 & D7) will not be accurate. Use the Special Read command (A5h) to read the correct values. Use the Read Output Port command only when the output buffer is empty.

(Continued)

Table 2-12. (Continued)

Code	Function
D1h	Write Output Port--place the next byte written to the 8042 data register (output port 60h) on the 8042's output port. The system speed bits are not set by this command--use commands A1h to A6h for speed functions.
	CAUTION Setting bit 0 of the 8042's Output Port 0 puts the system in a reset state until the power is turned off.
E0h	Read Test0 and Test1 Inputs--directs the 8042 to put the current state of Test0 and Test1 into the output buffer (output port 60h). Test0 is bit 0 and Test1 is bit 1.
F0h-FFh	Pulse Output Port--the 8042's output port, bits <3..0>, can be pulsed (strobed low) for approximately 2 us. Bits <3..0> of this command byte each represent one bit, or signal of the output port to be pulsed. Note: Bit 0 of the 8042's Output Port 0 is connected to the system reset. Pulsing bit 0 will reset the system.

System Scan Codes

Table 2-13 shows the codes sent by the keyboard to the 8042 for each key, and the final code sent to the system by the 8042.

Table 2-13. Keyboard Scan Codes

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
	00h	FFh (Note 1)	
ESC	76h	01h	01h
1,!	16h	02h	02h
2,@	1Eh	03h	03h
3,#	26h	04h	04h
4,$	25h	05h	05h
5,%	2Eh	06h	06h
6,^	36h	07h	07h
7,&	3Dh	08h	08h
8,*	3Eh	09h	09h
9,(	46h	0Ah	0Ah
0,)	45h	0Bh	0Bh
-,_	4Eh	0Ch	0Ch
=,+	55h	0Dh	0Dh
<--	66h	0Eh	0Eh

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Tab	0Dh	0Fh	0Fh
Q	15h	10h	10h
W	1Dh	11h	11h
E	24h	12h	12h
R	2Dh	13h	13h
T	2Ch	14h	14h
Y	35h	15h	15h
U	3Ch	16h	16h
I	43h	17h	17h
O	44h	18h	18h
P	4Dh	19h	19h
[,{	54h	1Ah	1Ah
],}	5Bh	1Bh	1Bh
RET	5Ah	1Ch	1Ch
Ctrl	14h	1Dh	1Dh
A	1Ch	1Eh	1Eh
S	1Bh	1Fh	1Fh
D	23h	20h	20h
F	2Bh	21h	21h
G	34h	22h	22h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
H	33h	23h	23h
J	3Bh	24h	24h
K	42h	25h	25h
L	4Bh	26h	26h
;,:	4Ch	27h	27h
','	52h	28h	28h
`,~	0Eh	29h	29h
Lshift	12h	2Ah	2Ah
\,|	5Dh	2Bh	2Bh
Z	1Ah	2Ch	2Ch
X	22h	2Dh	2Dh
C	21h	2Eh	2Eh
V	2Ah	2Fh	2Fh
B	32h	30h	30h
N	31h	31h	31h
M	3Ah	32h	32h
,,<	41h	33h	33h
.,>	49h	34h	34h
/,?	4Ah	35h	35h
Rshift	59h	36h	36h
*,PrtSc	7Ch	37h	37h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Alt	11h	38h	38h
Space	29h	39h	39h
Caps Lock	58h	3Ah	3Ah
F1	05h	3Bh	3Bh
F2	06h	3Ch	3Ch
F3	04h	3Dh	3Dh
F4	0Ch	3Eh	3Eh
F5	03h	3Fh	3Fh
F6	0Bh	40h	40h
F7	02h,83h (Note 2)	41h	41h
F8	0Ah	42h	42h
F9	01h	43h	43h
F10	09h	44h	44h
Num Lock	77h	45h	45h
Scroll Lock	7Eh	46h	46h
Home,7	6Ch	47h	47h
Up,8	75h	48h	48h
PgUp,9	7Dh	49h	49h

(Continued)

Table 2-13. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
-	7Bh	4Ah	4Ah
Left,4	6Bh	4Bh	4Bh
5	73h	4Ch	4Ch
Right,6	74h	4Dh	4Dh
+	79h	4Eh	4Eh
End,1	69h	4Fh	4Fh
Down,2	72h	50h	50h
PgDn,3	7Ah	51h	51h
Ins,0	70h	52h	52h
Del,.	71h	53h	53h
Sys Req	7Fh,84h (Note 2)	54h	

(Continued)

Table 2-13. (Continued)

US Character	11-Bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
R (Note 3)	60h	55h	
R (Note 3)	61h	56h	
F11 (Note 4)	78h	57h	
F12 (Note 4)	07h	58h	
R (Note 3)		59h through 7Fh	

Notes: 1. When the 8042 cannot read data from the keyboard, the 8042 sends FFh to the system, and sets the parity error bit of the Status register.
2. The second value is generated when the 8042 translates a 9-bit code to an 11-bit code.
3. R = Reserved
4. The F11 and F12 keys (System Scan Codes 57H and 58h respectively) are only available on the COMPAQ Enhanced Keyboard.

8042/Keyboard Communications Time Restraints

If a code transmission from the keyboard exceeds 2 ms, a time-out error results and the 8042 sends FFh to the system. No retries are attempted from a time-out error.

A keyboard clock signal strobes the 8042 during a data transmission to cycle data bits from the 8042 to the keyboard.

If the keyboard clock does not begin strobing within 15 ms after a byte is ready to transmit, or if the byte is not completely transmitted within 2 ms, the 8042 sends FEh to the system and sets the transmit time-out error bit in the status register.

The keyboard must respond to all transmissions from the 8042 within 25 ms, or the parity and time-out error bits are set in the status register of the 8042 and FEh is sent to the system. No retries are attempted by the 8042 after any data transmission error.

Security Key Lock

The security key lock is connected to the P17 line of the 8042 keyboard processor. When the security lock is unlocked, the keyboard is disabled. This feature allows a program to continue without accidental interference.

Interval Timer

The purpose of a programmable interval timer is to generate pulses at software-controllable intervals.

An Intel 8254 Programmable Interval Counter on the system boards provide three frequencies, or timed pulses for the system. The three counters count down a 16-bit value at a rate of 1.193 million counts-per-second and give an output pulse on the OUT pins. Table 2-14 lists the interval timer functions.

Two channels (interrupt and refresh) are on at all times; only the speaker tone can be disabled and enabled.

Table 2-14. Interval Timer Functions

Function	Counter 0 System Timer
Gate	Always On
Clock In	1.193 MHz
Clock Out	8259A IRQ0
Function	Counter 1 Refresh Request
Gate	Always On
Clock In	1.193 MHz
Clock Out	Request Refresh
Function	Counter 2 Speaker Tone
Gate	Programmable
Clock In	1.193 MHz
Clock Out	Speaker Input

Interval Timer Architecture

The interval timer contains three identical counters. Figure 2-18 shows the architecture of the interval timer. CRm and CRl contain the most- and least-significant bytes of the 16-bit initial count value. These registers are cleared when they are both transferred into CE.

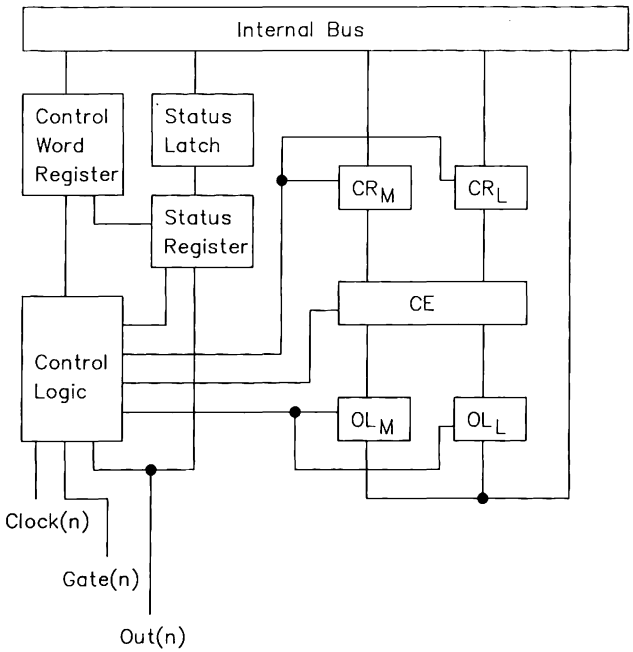


Figure 2-18. Counter Architecture

CE is the actual "Counting Element" latch that contains the value being counted down.

OLm and OLl contain the most- and least-significant bytes of the CE value, unless a latch command is given. In this case, the OLm and OLl registers hold the count until read.

Programming the Interval Timer

The timer is an I/O-mapped device. Table 2-15 lists the ports used. Several commands are available:

- The Control Word specifies:
  - which counter to read or write
  - the operating mode
  - the count format
- The Counter-Latch command latches the current count so that it can be read by the system. The count-down process continues.
- The Read-Back command reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 2-15. Interval Timer Port Assignments

Port	Function
40h	Read or Write Count for Counter 0 (System Clock)
41h	Read or Write Count for Counter 1 (Refresh Request)
42h	Read or Write Count for Counter 2 (Speaker Tone)
43h	Input for Control Word, Counter Latch, or Read-Back commands (Command Mode Register)

Interval Timer Operating Modes and Initial Values

Six operating modes are available (See Table 2-16).

Table 2-16. Interval Timer Operating Modes

Mode	Function
0	Out signal on end-of-count (=0)
1	Hardware retriggerable one-shot
2	Rate generator (divide-by-n counter)
3	Square-wave output
4	Software-triggered strobe
5	Hardware-triggered strobe

The three counters are initialized with the values shown in Table 2-17.

Table 2-17. Interval Timer Initial Values

Counter	Mode	Control Word	Count	Frequency
0	3	36h	65535	18.207 Hz
1	2	54h (See Note)	19	62.799 KHz
2	3	B6h	1336	893.10 Hz

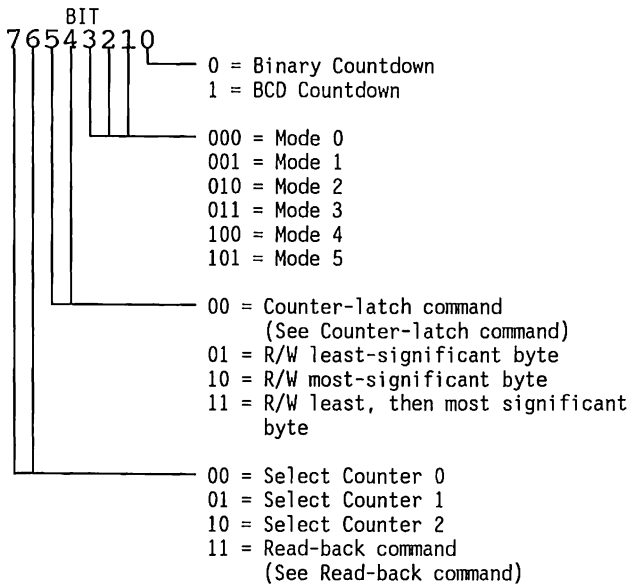
Note: Only the least-significant byte of the divisor is loaded.

Programming the interval timer is a simple process:

1. Write a control word.
2. Write an initial count for each counter.
3. Load the least- and most-significant bytes of the 16-bit counter in two steps (writes).

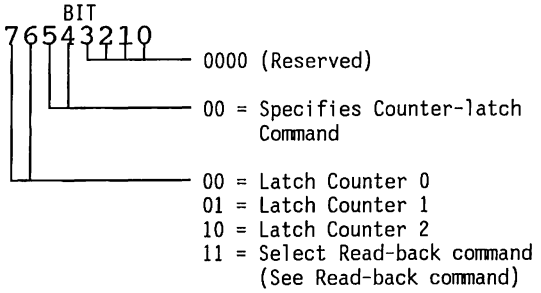
Interval Timer Control Word Format

The Control Word specifies the counter, whether it is to be written to or read from, the operating mode, and whether it counts down in a 16-bit or binary-coded decimal (BCD) format.



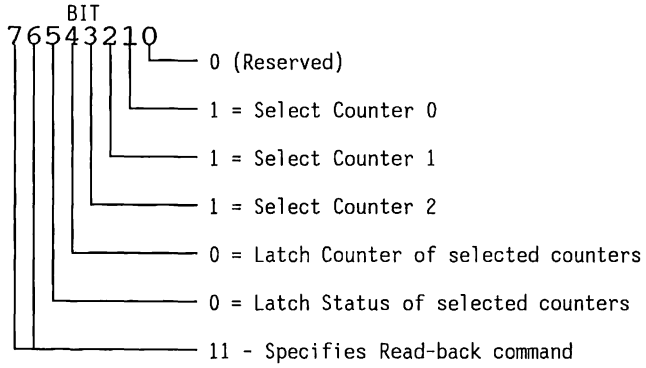
Interval Timer Counter-latch Command

The Counter-latch command latches the count at the time the command is received. The count is held in the OL registers until read.

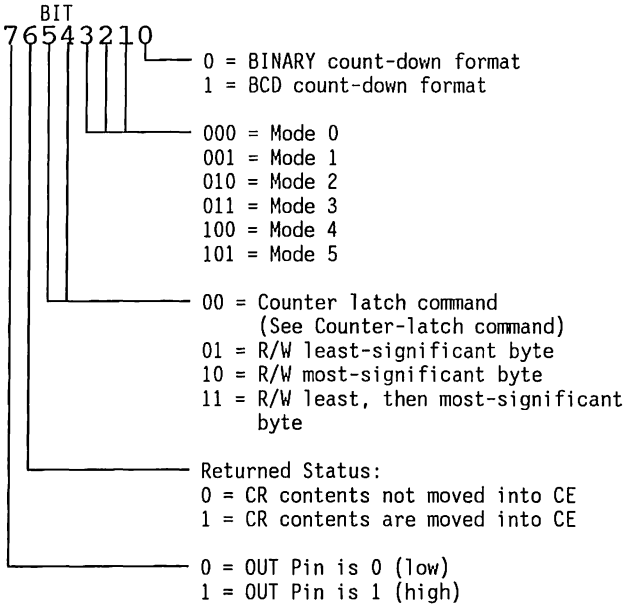


Interval Timer Read-back Command

The Read-back command causes the count or status of the counters to be latched in the OL registers until read. A single read-back can latch the count or status of all three counters.



The status byte latched into OL has the format:



Interrupt Priority Encoders

The 80286 processor has two signals for interrupts, labelled NMI (nonmaskable interrupt) and INTR (maskable interrupts). A maskable interrupt is an interrupt that can be enabled or disabled by the processor STI/CLI instructions. A nonmaskable interrupt is not masked off by the CLI instruction but can be disabled under software control by the system board logic.

NMI Interrupt Facts

NMI interrupts are caused by parity errors on the system board, memory boards, or any expansion boards which pull the IOCHK- line low.

System software can also generate a software interrupt to the NMI routine. When the IOCHK- line is pulled low, it sets the IOCHK- latch, which holds the error condition until software can examine it.

The source of the NMI can be determined by examining input port 61h, bit 6. If this bit is set, the interrupt came from the hardware IOCHK- line. To clear the hardware IOCHK- latch, pulse bit 3 of port 61h high.

The mask register for the NMI interrupt is at I/O-address 70h. The format for this byte is 10000000, that is, only the most significant bit is decoded. Write an 80h to port 70h to mask the NMI signal. This port is shared with the Real-Time Clock and Configuration Memory Device (the lower 6 bits). Do not modify the contents of this register without considering the effects on the state of the other bits.

INTR Interrupt Facts

All INTR-type interrupts to the CPU are channeled through the interrupt controllers (8259A). These devices generate interrupts on the 80286's interrupt line, which can be masked in the 80286 by software.

The interrupt controllers are 8-input devices that can accept interrupt signals from several devices, then prioritize them and interrupt the processor. The processor then automatically reads the interrupt controller to determine the source of the highest-priority interrupt and calls the appropriate interrupt routine.

Two interrupt controllers (a master and a slave) are used so that more than eight levels of interrupt are possible. The slave (Interrupt Controller 2) interrupts the master (Interrupt Controller 1) to show an interrupt. When Interrupt Controller 1 is properly programmed (in the special fully nested mode) Interrupt Controller 2 sends the correct interrupt vector to the CPU for the source of the interrupt. Figure 2-19 shows a diagram of the interrupt controller circuit.

All interrupts can be masked off, using the CLI instruction of the 80286. The base I/O address for Interrupt Controller 1 is 20h; for Interrupt Controller 2 it is A0h. Table 2-18 lists the initial interrupt controller values.

Table 2-18. Initial Interrupt Controller Values

Port	Value	Description of Contents
20h	11h	Cntlr 1, ICW1
21h	08h	Cntlr 1, ICW2 vector address for 000020h
21h	04h	Cntlr 1, ICW3 indicates slave connection
21h	01h	Cntlr 1, ICW4 8086 mode
A0h	11h	Cntlr 2, ICW1
A1h	70h	Cntlr 2, ICW2 vector address for 0001C0h
A1h	02h	Cntlr 2, ICW3 indicates slave ID
A1h	01h	Cntlr 2, ICW4 8086 mode
A21h	B8h	Cntlr 1, Interrupt mask (may vary with option)
A1h	9Dh	Cntlr 2, Interrupt mask (may vary with option)

Table 2-19 shows the 16 possible sources for an interrupt and their priorities. The highest-priority interrupt is processed first.

Table 2-19. Interrupts And Their Priorities

Priority	Label	Controller	Typical Interrupt Source
1	NMI	(Note)	Parity Error Detected
2	IRQ0	1	Interval Timer Output 0
3	IRQ1	1	Keyboard
	IRQ2	1	Interrupt from Controller 2
4	IRQ8	2	Real-Time Clock
5	IRQ9	2	Expansion Bus Pin B04
6	IRQ10	2	Expansion Bus Pin D03
7	IRQ11	2	Expansion Bus Pin D04
8	IRQ12	2	Expansion Bus Pin D05
9	IRQ13	2	Math Coprocessor
10	IRQ14	2	Fixed Disk Drive Controller --Expansion Bus Pin D07
11	IRQ15	2	Expansion Bus Pin D06
12	IRQ3	1	Serial Port 2 --Expansion Bus Pin B25
13	IRQ4	1	Serial Port 1 --Expansion Bus Pin B24
14	IRQ5	1	Parallel Port 2 --Expansion Bus Pin B23
15	IRQ6	1	Diskette Drive Controller --Expansion Bus Pin B22
16	IRQ7	1	Parallel Port 1 --Expansion Bus Pin B21

Note: The NMI signal is controlled through I/O port 70h, bit 7.

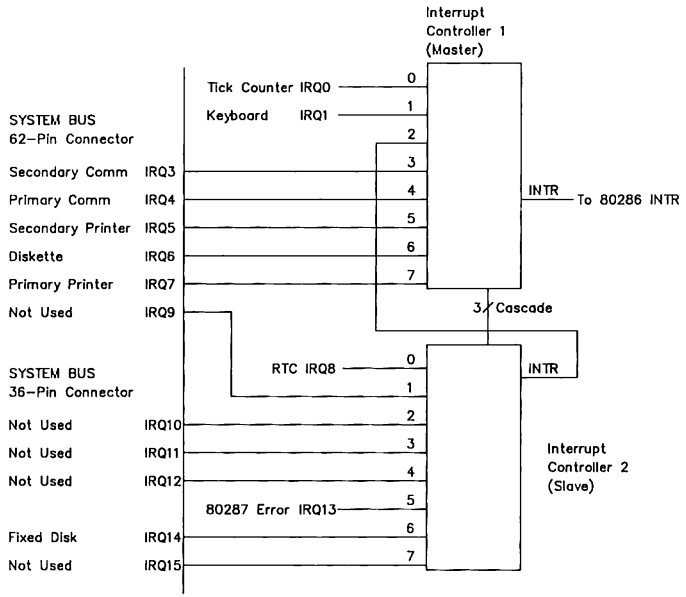


Figure 2-19. Interrupt Controller Circuit Diagram

2.5 EXPANSION BUS

The system board uses expansion slots to support additional circuit boards.

Expansion slots either have two connectors (62-pin and 36-pin) or one connector (62-pin). Slots with both connectors support a 16-bit data bus and the high-order address lines, LA<23..17> as well as additional interrupt and DMA lines. Slots with only one connector support only an 8-bit data bus with address lines SA<19..0>.

This section presents the expansion bus and the system timing requirements and includes:

- Detailed explanations of the expansion bus signals
- Major functions supplied to the expansion bus, such as:
  - Address Handling
  - Data Handling
  - Non-CPU Operations
  - DMA Operations
  - Dynamic RAM Refresh
  - Other Bus Master Operations
- Timing Considerations

Address Handling

When the CPU begins a bus cycle, it places an address on the address bus. This address may be placed on the bus even while the previous cycle is still in progress. Since most devices expect to see a valid address for the duration of a bus cycle, the system board latches the address onto the system bus.

System bus lines that contain the latched address are SA<19..0>. These latches are of the fall-through type so that when the address latch enable signal (ALE) goes active, the address appears at the output. When ALE goes inactive, the addresses will stay on the outputs until the next bus cycle begins.

Some high speed devices overlap some operations (such as address decoding). To allow this, the system bus provides a set of address lines (LA<23..17>) that are not latched but which provide a greater setup time to do decoding. When the address changes, expansion bus devices may decode the high-order address lines and then latch them using BALE. This allows expansion bus devices to take advantage of addresses for the next bus cycle that may be placed on the bus before the current bus cycle is complete.

When other devices (such as DMA or other bus masters) take control of the system bus, the BALE line is held active for the entire duration of the operation. As a result, expansion bus devices annot use BALE to latch the high-order address lines. Therefore, LA<23...17> should be held stable for the entire duration of each bus cycle.

Data Handling

Data handling for these products is accomplished with two data buses. The first is the 8-bit bus which is compatible with previous products. It is provided by the SD<7..0> lines. External devices and memory that are limited to 8-bit transfers will use this bus and the control lines SMRDC-, SMWTC-, IORC-, and IOWC- to enable or latch data on the bus.

Devices that can transfer data 16 bits at a time must also use the SD<15..8> lines for data transfer. The lines SBHE- and SA0 are used to determine which byte(s) are desired. These devices tell the system board that they are 16-bit devices by setting the M16- or IO16- (as appropriate) when they are addressed. Table 2-105 shows the relationship between the three lines.

Table 2-20. M16-, IO16-, SA0, and SBHE- Signal Relationship

M16- or IO16-	SA0	SBHE-	Cycle Type
High	High	----	Odd byte transfer on lines SD<7..0>
High	Low	----	Even byte transfer on lines SD<7..0>
Low	High	High	Reserved
Low	High	Low	Odd byte transfer on lines SD<15..8>
Low	Low	High	Even byte transfer on lines SD<7..0>
Low	Low	Low	Even word transfer on lines SD<15..0>

Non-CPU Operations

The system board supports several operations that are not related to the processor chip itself. They are refresh, traditional direct memory access, and expansion bus master access. Refresh is provided to prevent loss of data in dynamic RAMs (DRAMs). The other operations are used by expansion bus devices that require access to memory or I/O without processor intervention.

The system board prioritizes the requests for each type of service according to the following rules:

- If the CPU is the bus master, it completes the current processor cycle. (This includes word operations to 8-bit memory, which execute as two single-byte operations).
- If the CPU has an instruction LOCKed, it will complete the instruction.
- There is an automatic LOCK between an interrupt acknowledge and the first bus write in the acknowledge sequence.
- In the 80286 protected-virtual mode, segment-descriptor operations are automatically LOCKed (six words are loaded at one time).
- Refresh and other DMA cycles are started on a first-come, first-served basis after the CPU releases the bus.
- If a refresh is in progress when a DMA cycle is requested, the DMA cycle will be run without allowing the CPU to regain control of the bus.
- If a direct memory cycle is in progress when a refresh is requested, the refresh cycle will be run without allowing the CPU to regain control of the bus.
- The DMA controller will hold the bus until all outstanding DMA requests are handled.
- If a DMA channel is programmed for demand or block transfer modes, the DMA controller will keep the bus for the entire time to complete the programmed operation.
- Wait states or 8-bit memory anywhere in the system can delay the time required to acknowledge a DMA request.

Because of the above conditions, peripheral designers must assume that the latency on any DMA request can be as high as 10-12 us in a typical system using only diskette operations. If more than one DMA device is operating at one time, the latency can be even greater. If a program uses a LOCK prefix before string instructions or uses block- or demand-mode DMA, then the latency could reach the millisecond range.

DMA Operations

The DMA controllers in the system operate as a separate subsystem from the main bus controller. They handle requests from the DMA peripherals, arbitrate between them, and then request access to the system address and control lines from the CPU.

There are two types of DMA: byte and word. One of the DMA controllers is connected to handle byte-DMA operations, the other, word-DMA operations. To simplify the arbitration between sources, the request line from the byte controller is connected to a DMA request line (DRQ4) on the word controller. The word DMA controller is programmed for cascade mode on channel 0 (to which DRQ4 is connected) so that it will not actually place an address on the bus when it acknowledges the byte controller's request.

Byte-DMA Operations

The DMA byte cycle begins when a peripheral sets a DRQ<3..0> line active. The DMA controller then arbitrates among any other pending requests and sets the hold request output active. This line (DRQ4) is connected to the word controller as discussed above which does its arbitration. The word controller then sets its hold request line active which is in turn synchronized and arbitrated by the hold arbitration logic discussed above.

When the system responds to the request with an acknowledge, the word DMA controller will respond with a DAK4, which acts as a hold acknowledge to the byte controller. The byte controller will, after synchronizing the acknowledge, place an address on the bus lines.

Logic drives the SBHE- line in the opposite sense of SA0 in order to satisfy 16 bit devices on the bus. When this is complete, the DMA controller drives the lines IORC-, IOWC-, MWTC-, and MRDC- according to the type of cycle being run. If SA0 is high and the addressed memory is 16-bit, logic routes the data between the low half and high half of the data bus. The data is moved from high to low on memory reads, and from low to high on memory writes.

Word-DMA Operations

Word-DMA operations are only possible between word memory (16 bit) and word peripherals. Also, the DMA cannot operate on an odd-address boundary, on either memory or I/O. The system latches the SA0 and SBHE- lines to enable 16-bit devices on the bus.

The DMA-word cycle begins when a peripheral sets a DRQ5-DRQ7 line active. The DMA controllers then arbitrate among any other pending requests and set the hold request output active.

When the system responds to the request, the word DMA controller will, after synchronizing the acknowledge, respond with a DAKx acknowledge to the peripheral. The DMA controller will place the address on the bus and then drive the control lines.

Dynamic RAM Refresh

The dynamic RAM refresh subsystem is designed to do a memory read cycle on each of 256 addresses in the memory space as addressed by SA<7..0>. The other address lines are in an undefined state during the RAM refresh time. The system can also be driven by an external source if another bus master has control.

The system consists of a timer (part of the 8254) that generates the refresh requests every 15.924 us, arbitration logic that arbitrates whether the refresh controller or the DMA subsystem gets control of the bus, a timing generator, and a refresh address counter. The refresh request rate of 62.799 kHz provides 128 refresh cycles in 2.038 ms or 256 cycles in 4.0765 ms.

If an external bus master wishes to take the bus for long periods of time, it must perform refresh or risk losing the contents of dynamic memory. The external bus master can do this by developing its own refresh request timer and internal arbitration.

When it is not otherwise driving the bus, but still has bus control, the bus master can generate a refresh cycle by pulling the REFRESH- line low with an open collector gate. When the MRDC- line goes inactive from the refresh cycle, the REFRESH- line should be released. The external bus master can then take full control.

Other Bus-Master Operations

This system allows other bus masters to take over the system buses and use the I/O peripherals and memory. This is accomplished by the bus master software programming an unused DMA channel for cascade operation. When this is complete, the bus master can request the bus by setting the appropriate DRQx (<7..5>, <3..0>) line active and waiting for a response.

When the system responds with DAKx, the bus master can pull the GRAB- line active (low), disabling the address, data, and control lines. The bus master should then wait one BCLK period before enabling its own buffers with valid address information and wait one more BCLK period before driving the control lines.

When the bus master is finished, it should release the GRAB- and DRQx lines to allow the CPU to continue operations. If the bus master keeps control of the bus for more than 15 us, then it must provide its own refresh timing and request logic to prevent loss of dynamic memory contents.

Bus Driving/Loading Information

The following information is provided to improve the probability that third-party controller boards will work with the standard COMPAQ boards and options.

On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 mA and source 10 mA at 0.5 Vdc and 2.4 Vdc respectively.

On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 mA at 0.5 Vdc.

The load on any logic line from a single bus slot should not exceed -2.0 mA in the low state (at 0.5 Vdc) or 0.1 mA in the high state (at 2.7 Vdc).

The logic-high voltage at the expansion bus ranges from 2.0 Vdc to 5.5 Vdc. The logic low voltage at the expansion bus ranges from -1.2 Vdc to 0.8 Vdc.

Bus Timing Information

In the FAST mode, the system clock toggles between two frequencies (8 MHz or 6 MHz):

- According to address, in which case the new speed will occur during the BALE time
- According to bus size (when M16- changes state), in which case the new speed will occur in the first clock after BALE.

During these changes, the bus timings for the affected cycles will be somewhere between the actual 8 MHz and 6 MHz timings. Table 2-21 lists the important timing parameters for the expansion slots. This information assumes that the system clock is at a constant speed of either 8 MHz or 6 MHz.

NOTE: The expansion bus timing information is provided to aid in a general understanding of the system and is subject to change.

Table 2-21. Expansion Slot Timing Parameters

Address access time from SA<19..0> address lines, 16 bit bus read cycle.	
Access time 8 MHz	228 ns
Access time 6 MHz	332 ns
Address access time from SA<19..1> address lines, 8 bit bus read cycle.	
Access time 8 MHz	603 ns
Access time 6 MHz	832 ns
Address access time from SA0 address line, 8 bit bus read cycle.	
Access time 8 MHz	589 ns
Access time 6 MHz	818 ns
Access time from BALE active, 16 bit bus read cycle.	
Access time 8 MHz	232 ns
Access time 6 MHz	336 ns
MRDC- Access time, 16-bit bus read cycle.	
Access time 8 MHz	190 ns
Access time 6 MHz	273 ns
IORC- access time, 16-bit bus read cycle.	
Access time 8 MHz	127 ns
Access time 6 MHz	190 ns
MRDC-, IORC-, access time, 8-bit bus read cycle.	
Access time 8 MHz	502 ns
Access time 6 MHz	690 ns

(Continued)

Table 2-21. (Continued)

SMRDC- access time, 8-bit bus read cycle.	
Access time 8 MHz	484 ns
Access time 6 MHz	672 ns
CPU read data hold from MRDC-, IROC-, inactive, 8-bit bus cycle.	
Hold	1 ns
LAx address valid to 16-bit memory command setup.	
Setup 8 MHz	106 ns
Setup 6 MHz	169 ns
16-bit bus memory cycle M16- low delay from LAx address valid.	
Maximum allowed delay 8 MHz	108 ns
Maximum allowed delay 6 MHz	171 ns
BALE valid to 16-bit memory command setup.	
Setup 8 MHz	20 ns
Setup 6 MHz	41 ns
BALE valid to M16- setup.	
Setup 8 MHz	7 ns
Setup 6 MHz	28 ns
SA<19..0> address valid to 16-bit memory command setup.	
Setup 8 MHz	22 ns
Setup 6 MHz	42 ns

(Continued)

Table 2-21. (Continued)

SA<19..0> address valid to I/O, 8-bit command setup.	
Setup 8 MHz	84 ns
Setup 6 MHz	126 ns
SA0 address hold from command.	
HOLD 8 MHz	96 ns
HOLD 6 MHz	137 ns
SA<19..1> address hold from command.	
HOLD 8 MHz	110 ns
HOLD 6 MHz	151 ns
CPU write data setup to MWTC- active, 16-bit bus memory cycle.	
Setup 8 MHz	-5 ns
Setup 6 MHz	+16 ns
CPU write data setup to IOWC- (16/8-bit), MWTC- (8-bit), active.	
Setup 8 MHz	58 ns
Setup 6 MHz	100 ns
CPU write data setup to MWTC-, IOWC-, inactive, 16-bit bus cycle.	
Setup 8 MHz	245 ns
Setup 6 MHz	350 ns

(Continued)

Table 2-21. (Continued)

CPU write data setup to MWTC-, IOWC-, inactive, 8-bit bus cycle.	
Setup 8 MHz	620 ns
Setup 6 MHz	850 ns
Refresh address setup to MRDC- active	
Setup 8 MHz	76 ns
Setup 6 MHz	118 ns
Refresh address hold from MRDC- inactive	
HOLD	-5 ns
Refresh wait state BUSRDY low delay from MRDC- active	
Maximum allowed delay 8 MHz	90 ns
Maximum allowed delay 6 MHz	132 ns
Refresh wait state BUSRDY high setup to BCLK rising	
Setup	5 ns
CPU memory or I/O command wait state BUSRDY high setup to BCLK rising	
Setup 8 MHz	51 ns
CPU 16-bit memory command wait state BUSRDY low delay from command active	
Maximum allowed delay 8 MHz	75 ns
Maximum allowed delay 6 MHz	117 ns

(Continued)

Table 2-21. (Continued)

CPU 16-bit I/O command wait state BUSRDY low delay from command active	
Maximum allowed delay 8 MHz	12 ns
Maximum allowed delay 6 MHz	32 ns
CPU 8-bit command wait state BUSRDY low delay from command active	
Maximum allowed delay 8 MHz	387 ns
Maximum allowed delay 6 MHz	532 ns
CPU minimum command active from BUSRDY high after added wait state.	
Command active 8 MHz	135 ns
Command active 6 MHz	177 ns
CPU maximum command active from BUSRDY high after added wait state.	
Command active 8 MHz	300 ns
Command active 6 MHz	382 ns
CPU 16-bit memory command no wait state NOWS- low delay from command active.	
Maximum allowed delay 8 MHz	20 ns
Maximum allowed delay 6 MHz	41 ns
CPU 8-bit memory command no wait state NOWS- low setup to BLCK falling required.	
Setup required	16 ns

(Continued)

Table 2-21. (Continued)

DMA memory read, I/O write command additional wait state. BUSRDY low delay from memory read command active.	
Maximum allowed delay 8 MHz	182 ns
Maximum allowed delay 6 MHz	265 ns
DMA I/O read, memory write command additional wait state. BUSRDY low delay from I/O read command active.	
Maximum allowed delay 8 MHz	273 ns
Maximum allowed delay 6 MHz	440 ns
Required I/O data access time from IORC- for DMA write to RAM.	
DMA I/O read access time 8 MHz	264 ns
DMA I/O read access time 6 MHz	347 ns
DATA valid after IOWC- low during DMA read from RAM.	
DMA data valid from IOWC- low	163 ns
DATA setup to IOWC- high during DMA read from RAM.	
Data setup to IOWC- high 8 MHz	217 ns
Data setup to IOWC- high 6 MHz	383 ns

2.6 MISCELLANEOUS SYSTEM BOARD INFORMATION

This section contains miscellaneous information that does not relate to any of the other sections, such as:

- Speed control
- Real-Time Clock and Configuration-Memory Battery
- Indicators
- Fuses
- Speaker Interface
- Clock Circuits
- System Board Power Requirements

Speed Control

The system boards have three speed modes:

- COMMON - I/O speed = 6 MHz, RAM speed = 6 MHz
- FAST - I/O speed = 6 MHz, RAM speed = 8 MHz
- HIGH - I/O speed = 8 MHz, RAM speed = 8 MHz

In the COMMON mode, all memory addresses or bus cycle types operate at 6 MHz except:

- DMA transfers (3 MHz (6 MHz/2)), and
- 80287 processes (4 MHz (12 MHz/3))

The FAST mode operates the system at a faster (8 MHz) speed except when this might cause a problem with operation of hardware options. In the FAST mode, the following memory addresses or bus cycle types continue to operate at 6 MHz:

- Memory with addresses 0A0000h to 0EFFFFh
- Memory with addresses FE0000h to FFFFFFh
- All I/O devices (except DMA transfers and 80287 processes)
- Any 8-bit memory device

In the FAST mode, the following memory addresses or bus cycle types operate at 8 MHz:

- RAM in base memory (000000h to 09FFFFh) unless it is 8-bit
- RAM in extended memory (100000h to FDFFFFh) unless it is 8-bit
- Standard ROM (0F0000h to 0FFFFFh)
- DMA transfers (half-speed (8 MHz/2))
- 80287 processes (5.33 MHz (16 MHz/3))

In the HIGH mode, all memory addresses or bus cycle types operate at 8 MHz except:

- 8 bit I/O or memory devices
- DMA transfers (half-speed (8 MHz/2)), and
- 80287 processes (5.33 MHz)

The speed is controlled by system software through the keyboard controller (8042).

The ES jumper located on the system board (switch 6 on the DESKPRO 286 with Version 2 System Board) sets the speed of the CPU when the system is powered up. When ES is in position 1-2, the CPU speed can be toggled between COMMON and FAST mode using the multiple key combination of Ctrl, Alt,\. When ES is in position 2-3, the CPU speed is limited to the COMMON mode and use of the multiple key combination Ctrl, Alt, \ will not affect the CPU speed.

The MODE SPE[ED] command overrides the ES setting in all cases.

NOTE: It is possible to restrict the CPU to the COMMON 6 MHz speed using the ES jumper.

Real-Time Clock and Configuration-Memory Battery

Table 2-22 lists the battery voltage range at the battery connector under load condition.

Table 2-22. Battery Connector Pinout

Pin	Function	Battery Voltage Min.	Max.
1	+5 Vdc Power	5.0	5.4
2	Keyed		
3	Not Used		
4	Ground	0.0	0.0

The voltage for a new battery must not exceed 6.2 V open circuit. The current drain on the battery varies with the voltage and the clock operating mode, but is between 50 to 90 ua after running SETUP. The maximum current is less than 150 uA.

CAUTION

Only COMPAQ Authorized Dealers should replace the system battery. Extreme caution must be observed to replace the battery with an identical battery type and on the correct connector pins.

Indicators (LEDs)

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 system boards have a light-emitting diode (LED) that lights when the +5 Vdc power is ON.

Fuses

The COMPAQ PORTABLE 286 system board and the COMPAQ DESKPRO 286 Version 2 system board have no user-replaceable fuses. The COMPAQ DESKPRO 286 Version 1 system board has two (Table 2-23).

Table 2-23. COMPAQ DESKPRO 286 Version 1 Fuses

F1, Keyboard Power Fuse, 2.5A
F2, Monitor Power Fuse, 2.5A

Speaker Interface

The speaker interface allows the speaker to be driven from two sources: the 8254-2 interval timer 2, or the processor through port 61h bit 1. In addition, the 8354 interval timer can be enabled and disabled from port 61h bit 0.

To use the 8254 interval timer to generate a tone, program Timer 2 to the desired frequency (the input clock rate is 1.193 MHz), and set port 61h bits 0 and 1 to 1. If the speaker is to be toggled directly by the CPU, port 61h bit 0 should be set to 0 and bit 1 should be toggled.

Clock Circuits

The two crystal oscillators on the system board provide:

- Clock frequencies for the 80286 processor and the entire system
- A clock source for video color burst signal and general timing

A crystal oscillator provides a 48-MHz frequency that is divided by 3 or 4 (software-selected) to provide the master clock for the clock-generator interface.

The clock generator interface further buffers the 12- or 16-MHz clock to supply the clocks used by the 80286, 80287, and other clocked devices. This interface also controls the reset signal. System reset does not occur until power levels are stable (PWRGOOD signal from power supply becomes active).

A second crystal oscillator on the system board provides a 14.31818-MHz (4 times 3.579545 MHz) clock signal for color-burst timing. This clock signal connects to pin B30 of the board slots for use by video controller and other boards.

System Board Power Requirements

Both system boards use +5 Vdc, and +12 Vdc power. They distribute power for other components of the system from the -5 Vdc, -12 Vdc and auxiliary +12 Vdc provided by the power supply.

2.7 GATE ARRAY DEVICES

The Version 2 system board of the COMPAQ DESKPRO 286 has three gate array devices:

- Memory and Speed Control (MSC) Gate Array
- Clock and Buffer Control (CBC) Gate Array
- Memory Map (MAP) Gate Array

The Gate Array Devices allow the size and cost of the system board to be reduced by consolidating the functions of several devices on the Type 1 system board. Both system boards are compatible, and are designed to the same programming standards.

This section describes the Gate Array Devices and provides a functional overview of each device.

MSC Gate Array

The MSC Gate Array includes the memory decoding and speed control functions resident on a Type 1 system board in (PALs) MEMCNT1, MEMCNT2, and SPEEDPAL.

The speed control function allows the selection of either an 8 MHz clock speed or a 6 MHz clock speed. The memory decoding functions include the generation of RAS-, CAS-, RAM-, MEM16, and ROM Enable- with multiple RAS and CAS lines for memory bank and hi/lo byte selection. In addition, the MSC Gate Array serves as a stand-alone memory controller for memory expansion boards.

CBC Gate Array

The CBC Gate Array incorporated the function of the 82284, 82288, and the CTRLPAL on the Version 1 system board. In addition, the CBC includes the clock switching/generation logic, generation of automatic and requested wait-states, shutdown logic, 8/16 bit bus conversion, and bus arbitration.

MAP Gate Array

The MAP Gate Array incorporates the functions of the Memory Page Register (74LS612), and PALs NCPPAL and PPIPAL on the Type 1 system board. In addition, the MAP Gate Array provides the circuitry for PORT B, SPEAKER and GATE control, REFRESH DETECT, and NMI control.

2.8 JUMPERS AND SWITCHES

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Version 1 system boards have three jumpers in common. The ES jumper determines the CPU speed when power is applied and allows toggling of CPU through keyboard commands. The ED jumper indicates the primary display controller used when power is applied. EM is reserved for manufacturing test purposes. Table 2-24 defines the jumper settings.

Table 2-24. COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 Type 1 Common Jumpers

Label	Setting	Description
ES	2-3	CPU speed initial setting - 6MHz (COMMON)
	1-2	CPU speed toggle active (COMMON/FAST)
ED	2-3	COMPAQ Graphics or RGB video controller
	1-2	Non-COMPAQ monochrome/text video controller
EM	1-2	Reserved

The functions of the ES, ED, and EM jumpers are implemented with a switch on the COMPAQ DESKPRO 286 with Version 2 system board. Table 2-25 defines the switch settings.

Table 2-25. COMPAQ DESKPRO 286 (with Version 2 system board) Switch SW1 Settings

SW1 Position	Setting	Description
6	CLOSED	CPU speed initial setting - 6 MHz (COMMON)
	OPEN	CPU speed toggle active (COMMON/FAST)
8	CLOSED	COMPAQ Graphics or RGBI Video Controller
	OPEN	non-COMPAQ monochrome/text video controller
7	CLOSED	Reserved

Note: CLOSED = ON, OPEN = OFF

The COMPAQ PORTABLE 286 system board has several other jumpers which select the RAM and ROM configurations. These jumpers are explained in "The COMPAQ PORTABLE 286 Memory" section in this chapter. (See Chapter 4 for information on jumper settings when using a 512/2048 Kbyte Memory Expansion Board.).

The COMPAQ DESKPRO 286 (with Version 1 system board) RAM and ROM configuration jumpers are explained in Chapter 3, System Memory Board.

The COMPAQ DESKPRO 286 (with Version 2 system board) has jumpers which select the ROM type. The RAM configurations are controlled by switch settings (SW1, positions 1 through 5 on system board). These jumpers and switch settings are explained in "The COMPAQ DESKPRO 286 RAM" section in this chapter.

2.9 CONNECTORS

Tables 2-26 through 2-28 list the system board connectors. Table 2-29 describes the expansion slot signals. Figures 2-20 through 2-39 show the connectors on the system boards.

Table 2-26. System Board Connections

Function	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286
DC power(In)	J116	J117
Drive power(Out)	J114-J115	J111-J112
Fixed disk drive power	J113	J109 or J110 (See Note)
Battery	J110	J118
Keyboard	J111	J116
Monitor power	J112	J113
Security lock	J117	J119
Speaker	J109	J115

Note: J110 is for an optional fixed disk drive back-up or second fixed disk drive.

Table 2-27. COMPAQ PORTABLE 286 System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	N/A	Diskette/Tape Controller
2	J102	N/A	Video Display Controller
3	J103	J106	Fixed Disk Drive Controller
4	J104	J107	Expansion (available)
5	J105	See Note	Expansion (available)

Note: Connector J108 is not installed.

Table 2-28. COMPAQ DESKPRO 286 System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	J121	Expansion (available)
2	J102	N/A	Expansion (available)
3	J103	J123	Expansion (available)
4	J104	J124	Expansion (available)
5	J105	J125	See Note
6	J106	J126	Fixed Disk Drive Controller
7	J107	J127	Video Display Controller
8	J108	N/A	Diskette/Tape Controller

Note: In the COMPAQ DESKPRO 286 with Version 1 system board, slot 5 contains the System Memory Board. In the COMPAQ DESKPRO 286 with Version 2 system board, slot 5 is available for expansion.

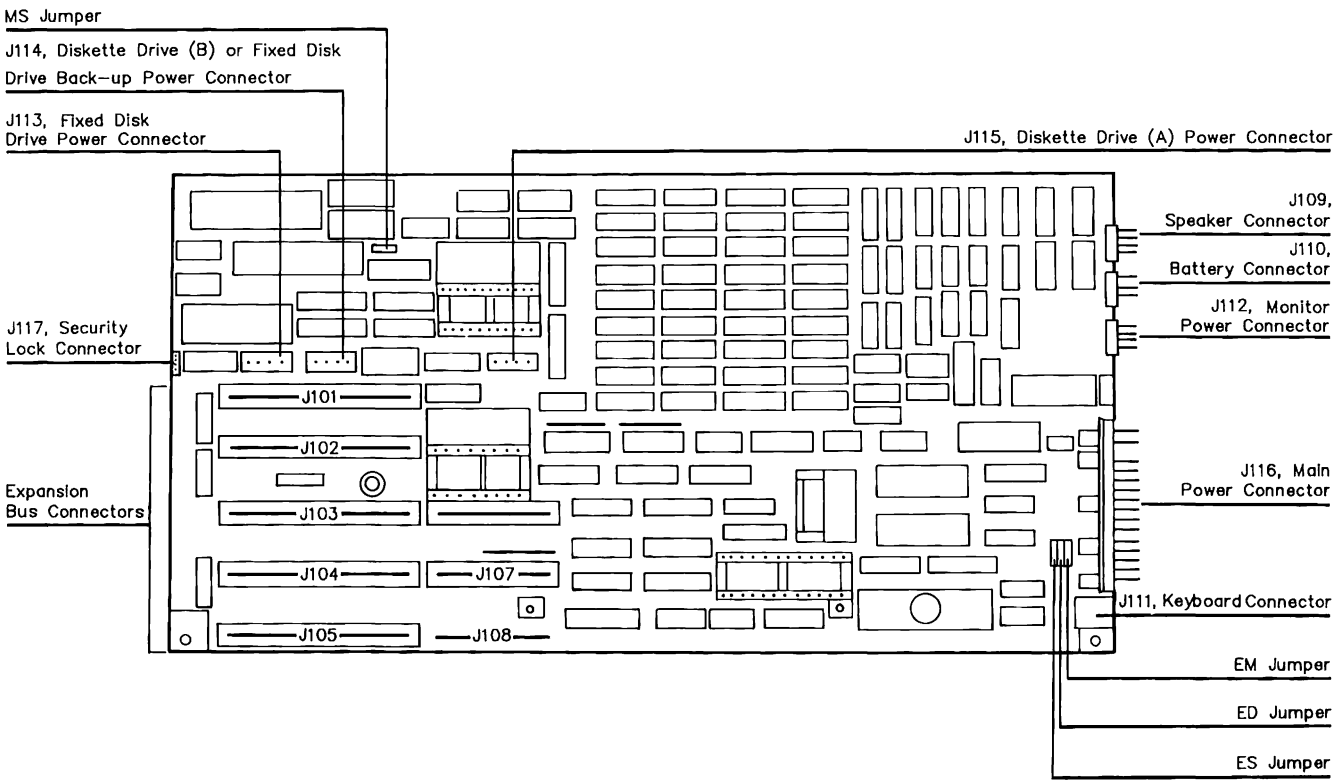


Figure 2-20. COMPAQ PORTABLE 286 System Board Connectors and Jumpers

Table 2-29. Expansion Slot Signals

Signal Name	Slot Pin	Type	Description
AEN	A11	O	This output signal when inactive (low) indicates that the CPU or controller board bus master has control of the bus. When active, the DMA controller has control of the bus. It is often used to disable devices which must not respond during a DMA cycle.
BALE	B28	O	This output signal (when high) indicates that a valid address is present on the LA<23..17> address lines. The LA<23..17> address lines or any decodes developed from them should be latched at the falling edge of BALE. This line is high when a DMA or bus master operation is occurring.
BCLK	B20	O	This output signal is provided to allow synchronization to the main processor clock. Its frequency will be either 6 MHz or 8 MHz with a duty cycle of 50%.
BUSRDY	A10	I	This input signal is used to lengthen a bus cycle from its standard time if a controller board cannot respond quickly enough. It should be pulled low by an open collector type device as soon as a slow addressed device is selected and held low until the device has responded. Bus cycles are lengthened by an integral number of (BCLK) cycles. This line should not be held low for more than 2.5 us. This line should be driven by an open-collector device capable of sinking 20 mA.
DAK0- DAK1- DAK2- DAK3- DAK5- DAK6- DAK7-	D08 B17 B26 B15 D10 D12 D14	O O O O O O O	These output lines (DMA Acknowledge) indicate that a request for a DMA service from the DMA subsystem has been recognized. The acknowledge is indicated by a LOW on this line. Use this line with the IORC- or IOWC- line to decode the desired DMA device. If used to signal acceptance of a bus-master request, this signal indicates when it is legal to pull GRAB- low.
DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	D09 B18 B06 B16 D11 D13 D15	I I I I I I I	These input lines are used to request a DMA service from the DMA subsystem or to gain control of the system bus from the main CPU (DMA request). The request is made when the line goes from a low to a high and must remain high until the appropriate DAK<7..5>, <3..0> line goes active.

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
GRAB-	D17	I	This input signal is used to indicate that a controller board bus master is controlling the bus. A controller board can pull this line low when the appropriate DAK line is made active, signalling that a master request is granted. The system address, data and control lines will be floated, allowing the controller board to begin controlling them one full BCLK period after GRAB is made active. At least one more full BCLK period should be allowed after putting a valid address on the bus before activating any of the control lines. This line should be driven by an open-collector device capable of sinking 20 mA.
GROUND	B01	--	These lines are connected to the system ac and dc ground. The maximum current allowed on any single contact is 1.5 A.
	B10	--	
	B31	--	
	D18	--	
IOCHK-	A01	I	This input signal is used to signal the CPU about parity or other serious errors on controller boards. This signal should be driven low by an open collector type output capable of sinking 20 mA when an uncorrectable system error occurs.
IORC-	B14	I/O	This output line (I/O read) indicates (when low) when an I/O device is to send data to the data bus. It can be driven by a controller board acting as a bus master.
IOWC-	B13	I/O	This output line (I/O write) indicates (when low) when an I/O device is to accept the data from the data bus. It can be driven by a controller board acting as a bus master.
IO16-	D02	I	This input line (I/O is 16 bits) signals the system that the addressed I/O device is capable of transferring 16 bits of data at once. When this line is made active, during an I/O read or write, the standard one wait state I/O cycle will be run. This line should be driven low by an open-collector device capable of sinking 20 mA.
IRQ3	B25	I	These input lines are used to interrupt the CPU to request some service. The interrupt is recognized when the line goes from a low to a high and remains there until the appropriate interrupt service routine is executed.
IRQ4	B24	I	
IRQ5	B23	I	
IRQ6	B22	I	
IRQ7	B21	I	
IRQ9	B04	I	
IRQ10	D03	I	
IRQ11	D04	I	
IRQ12	D05	I	
IRQ14	D07	I	
IRQ15	D06	I	

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
LA17 LA18 LA19 LA20 LA21 LA22 LA23	C08 C07 C06 C05 C04 C03 C02	I/O I/O I/O I/O I/O I/O I/O	These output signals (Latchable Address) are used to decode memory which must respond with zero or one wait state. They are only guaranteed to be valid when BALE is high. These can be driven by a controller board acting as a bus master.
MRDC-	C09	I/O	This output line (Memory Read) indicates (when low) when a memory device is to send data to the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
MWTC-	C10	I/O	This output line (Memory Write) indicates (when low) when a memory device is to accept the data from the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
M16-	D01	I	This input line (memory is 16 bits) signals the system that the addressed memory is capable of transferring 16 bits of data at once. When this line is made active, during a memory read or write, the standard one wait state memory cycle will be run. This line should be derived from the LA<23..17> address lines. This line should be driven low by an open collector device capable of sinking 20 mA.
NOWS-	B08	I	This input line (No Wait State) is used to inform the system that standard wait states can be deleted for cycles when this line is made active. The line must be pulled low 45 ns before the falling edge of BCLK in order to be recognized. This line should be driven by an open-collector device capable of sinking 20 mA.
OSC	B30	O	This output signal is a clock for use in video color burst and other general timing applications. Its frequency is 14.31818 MHz and duty cycle is approximately 50%.
REFRESH-	B19	I/O	This output signal is used to indicate (when low) a refresh cycle in progress. It should be used to enable the SA<7..0> address lines to the row address inputs of all banks of dynamic memory so that when the MRDC- goes active, the entire system memory is refreshed at one time. It can be driven by a controller board acting as a bus master.
RESDRV	B02	O	This output signal is used to reset the hardware during powerup or power failure.

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
SA0	A31	I/O	These bidirectional signals address memory or I/O devices within the system. They form the low order 20 bits of the 24 bit address bits that the system offers. These lines are enabled onto the bus while BALE is high and are latched when BALE goes from a high to a low state. These can be driven by a controller board acting as a bus master.
SA1	A30	I/O	
SA2	A29	I/O	
SA3	A28	I/O	
SA4	A27	I/O	
SA5	A26	I/O	
SA6	A25	I/O	
SA7	A24	I/O	
SA8	A23	I/O	
SA9	A22	I/O	
SA10	A21	I/O	
SA11	A20	I/O	
SA12	A19	I/O	
SA13	A18	I/O	
SA14	A17	I/O	
SA15	A16	I/O	
SA16	A15	I/O	
SA17	A14	I/O	
SA18	A13	I/O	
SA19	A12	I/O	
SBHE-	C01	I/O	This output signal (System Bus High Enable) indicates (when low) that the high half of the SD data bus should transfer the data on boards which support the full 16-bit data bus. It can be driven by a controller board acting as a bus master.
SD0	A09	I/O	These bidirectional signals are the low 8 bits of the system data bus. They should be used exclusively by all eight bit devices to transfer data. Sixteen-bit devices should use these lines to transfer only the low half of a data word when the address line A0 is low. These can be driven by a controller board acting as a bus master.
SD1	A08	I/O	
SD2	A07	I/O	
SD3	A06	I/O	
SD4	A05	I/O	
SD5	A04	I/O	
SD6	A03	I/O	
SD7	A02	I/O	

(Continued)

Table 2-29. (Continued)

Signal Name	Slot Pin	Type	Description
SD08	C11	I/O	These bidirectional signals are the high 8 bits of the system data bus. Sixteen bit devices should use these lines to transfer the high half of a data word when the line SBHE- is low. These can be driven by a controller board acting as a bus master.
SD09	C12	I/O	
SD10	C13	I/O	
SD11	C14	I/O	
SD12	C15	I/O	
SD13	C16	I/O	
SD14	C17	I/O	
SD15	C18	I/O	
SMRDC-	B12	O	This output line (Standard Memory Read) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MRDC-.
SMWTC-	B11	O	This output line (Standard Memory Write) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MWTC-.
T/C	B27	O	This output signal (when high) indicates that the Terminal Count of a DMA operation has been reached. It should be decoded with the appropriate DAKx line for proper operation.
+5 Vdc	B03	--	These lines are connected to the system power supply for 5 volts. In addition to the maximum current available from the supply, the maximum current allowed on any single contact is 1.5 A.
	B29	--	
	D16	--	
-5 Vdc	B05	--	This line is connected to the system power supply for minus 5 volts. This supply is intended for low-current usage only (500 mA).
-12 Vdc	B07	--	This line is connected to the system power supply for minus 12 volts. This supply is intended for low-current usage only (1.0 A).
+12 Vdc	B09	--	This line is connected to the system power supply for 12 volts. In addition to the maximum current available from the supply, the maximum current allowed on this contact is 1.5 A.

The 36-pin connector conducts the high-order byte of the 16-bit data bus, the memory address lines for bits DAK<7..5>, LA<23..17>, signals, and more. These signals generally relate to 16-bit or high-address memory transfers.

The 62-pin connector conducts the signals needed by adapters that do not need word-length data transfers or access to more than the base 1 MB of memory.

Figure 2-21 shows the 36-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
M16–	D01	C01	SBHE–
IO16–	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0–	D08	C08	LA17
DRQ0	D09	C09	MRDC–
DACK5–	D10	C10	MWTC–
DRQ5	D11	C11	SD8
DACK6–	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7–	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V	D16	C16	SD13
GRAB–	D17	C17	SD14
SIGNAL GROUND	D18	C18	SD15

Figure 2-21. Expansion Slot - 36-Pin Connector

Figure 2-22 shows the 62-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
GROUND	B01	A01	IOCHK–
RESDRV	B02	A02	SD7
+5 Vdc	B03	A03	SD6
IRQ9	B04	A04	SD5
–5 Vdc	B05	A05	SD4
DRQ2	B06	A06	SD3
–12 Vdc	B07	A07	SD2
NOWS–	B08	A08	SD1
+12 Vdc	B09	A09	SD0
GROUND	B10	A10	BUSRDY
SMWTC–	B11	A11	AEN
SMRDC–	B12	A12	SA19
IOWC–	B13	A13	SA18
IORC–	B14	A14	SA17
DAK3–	B15	A15	SA16
DRQ3	B16	A16	SA15
DAK1–	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH–	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DAK2–	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5 Vdc	B29	A29	SA2
OSC	B30	A30	SA1
SIGNAL GROUND	B31	A31	SA0

Figure 2-22. Expansion Slot - 62-Pin Connector

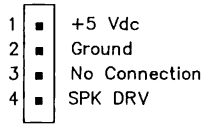


Figure 2-23. J109, COMPAQ PORTABLE 286 Speaker Connector

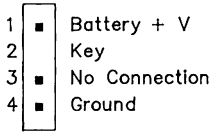


Figure 2-24. J110, COMPAQ PORTABLE 286 Battery Connector

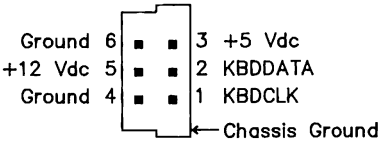


Figure 2-25. J111, COMPAQ PORTABLE 286 Keyboard Connector

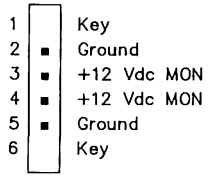


Figure 2-26. J112, COMPAQ PORTABLE 286 Monitor Connector

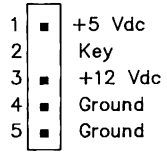
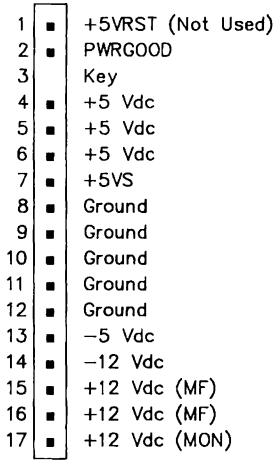


Figure 2-27. J113, J114, and J115, COMPAQ PORTABLE 286 Drive Power Connectors



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 2-28. J116, COMPAQ PORTABLE 286 Main Power Connector

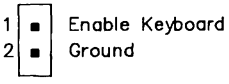


Figure 2-29. J117, COMPAQ PORTABLE 286 Security Lock Connector

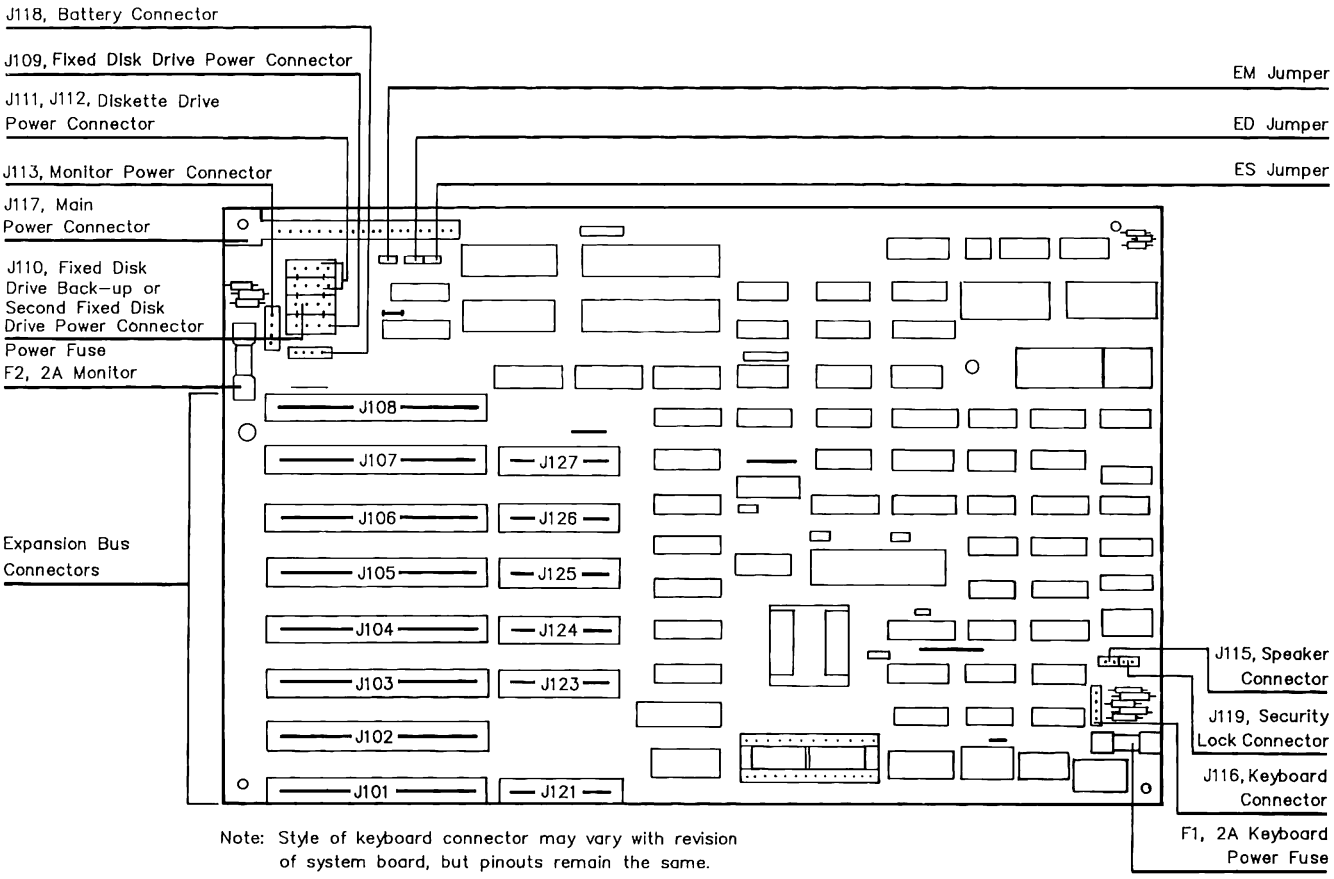


Figure 2-30. COMPAQ DESKPRO 286 Version 1 System Board Connectors and Jumpers

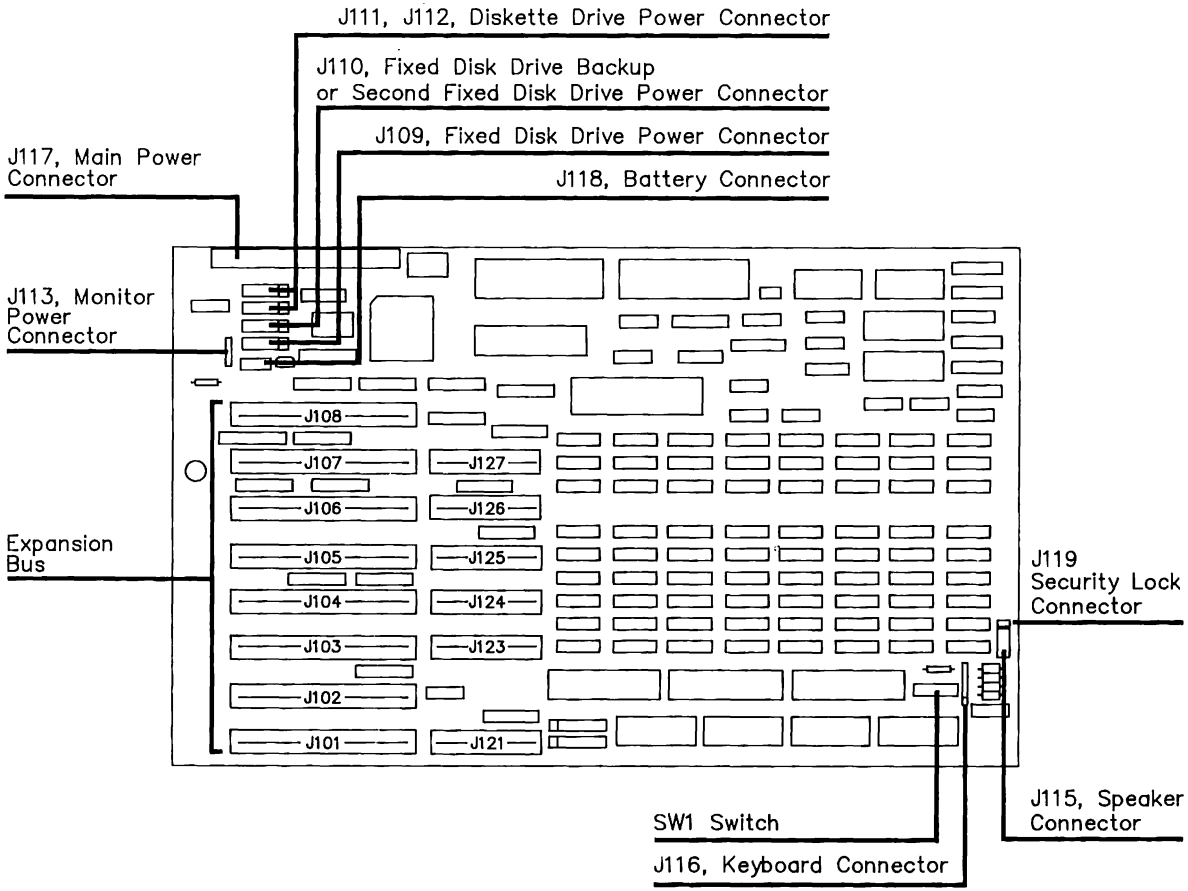


Figure 2-31. COMPAQ DESKPRO 286 Version 2 System Board Connectors and SW1 Location

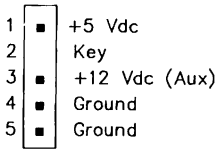


Figure 2-32. J109 and J110, COMPAQ DESKPRO 286 Fixed Disk Drive or Fixed Disk Drive Back-up Power Connector

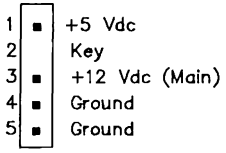


Figure 2-33. J111 and J112, COMPAQ DESKPRO 286 Diskette Drive Power Connectors

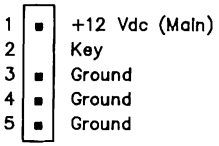


Figure 2-34. J113, COMPAQ DESKPRO 286 Monitor Power Connector

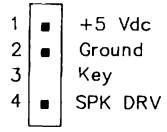


Figure 2-35. J115, COMPAQ DESKPRO 286 Speaker Connector

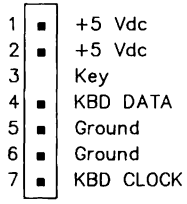
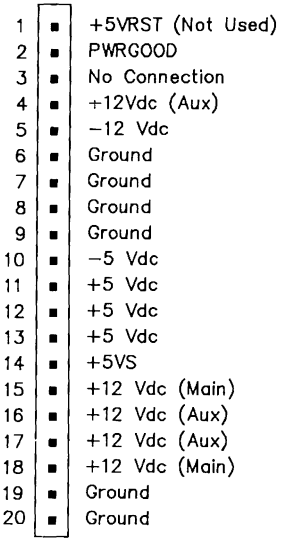


Figure 2-36. J116, COMPAQ DESKPRO 286 Keyboard Connector



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 2-37. J117, COMPAQ DESKPRO 286 Main Power Connector

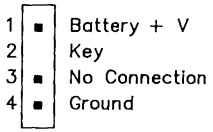


Figure 2-38. J118, COMPAQ DESKPRO 286 Battery Connector

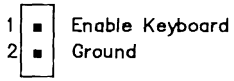


Figure 2-39. J119, COMPAQ DESKPRO 286 Security Lock Connector

2.10 COMPONENT LAYOUTS AND SCHEMATICS

Figure 2-40 shows the component layout for the COMPAQ PORTABLE 286 system board. Figure 2-41 shows the schematics for the COMPAQ PORTABLE 286 system board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

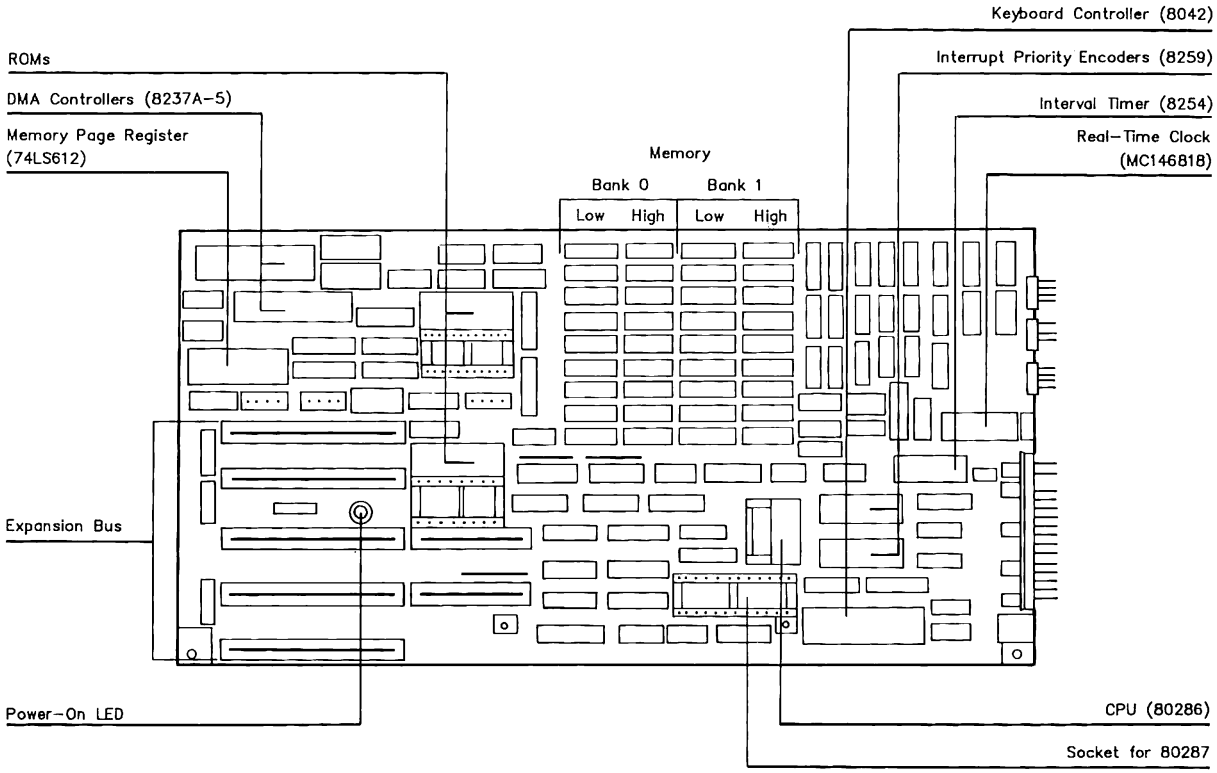


Figure 2-40. COMPAQ PORTABLE 286 System Board Component Layout (Page 1 of 1)

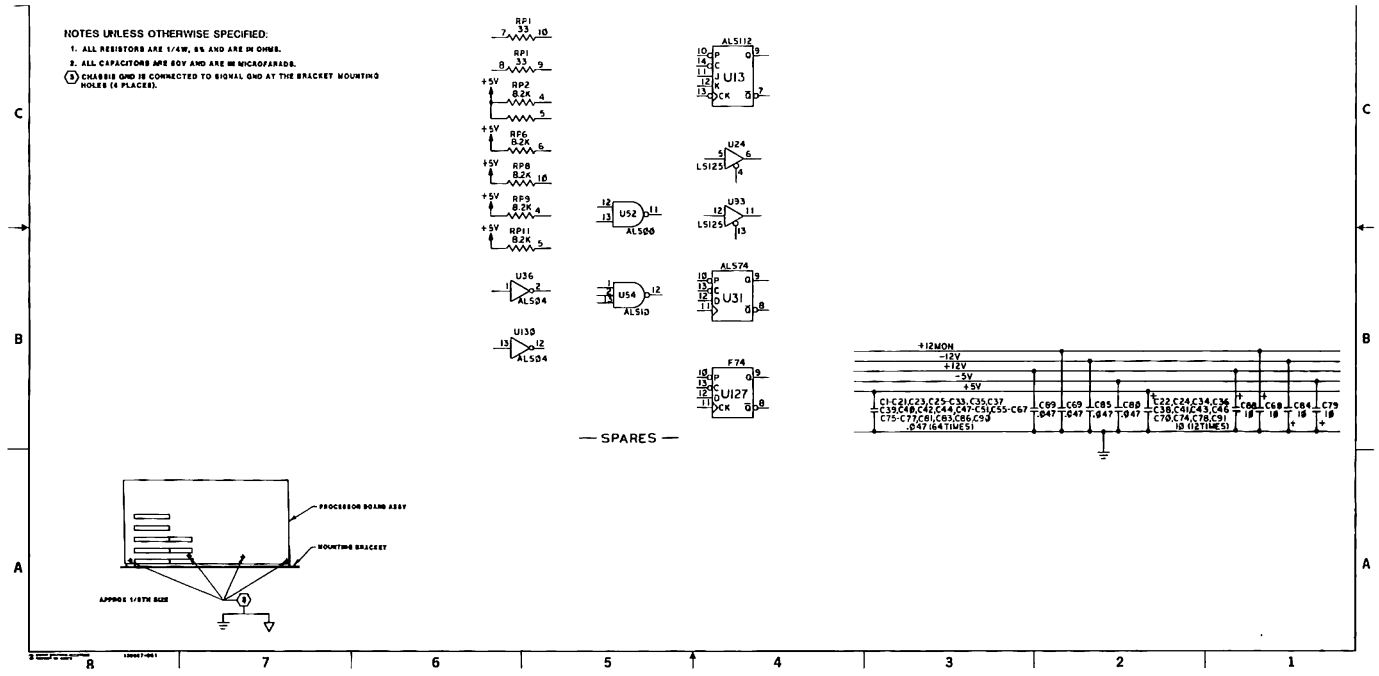


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 1 of 7)

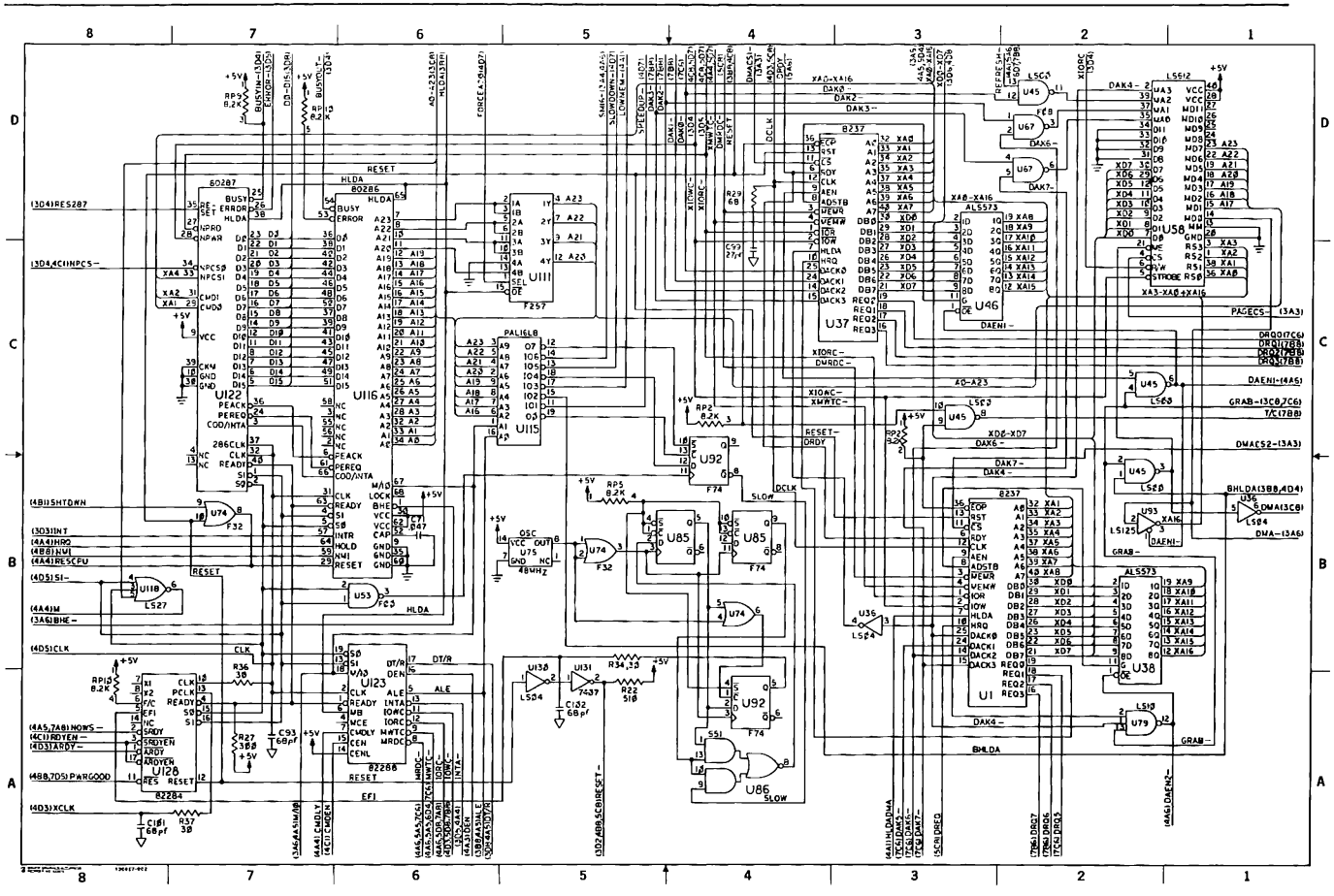


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 2 of 7)

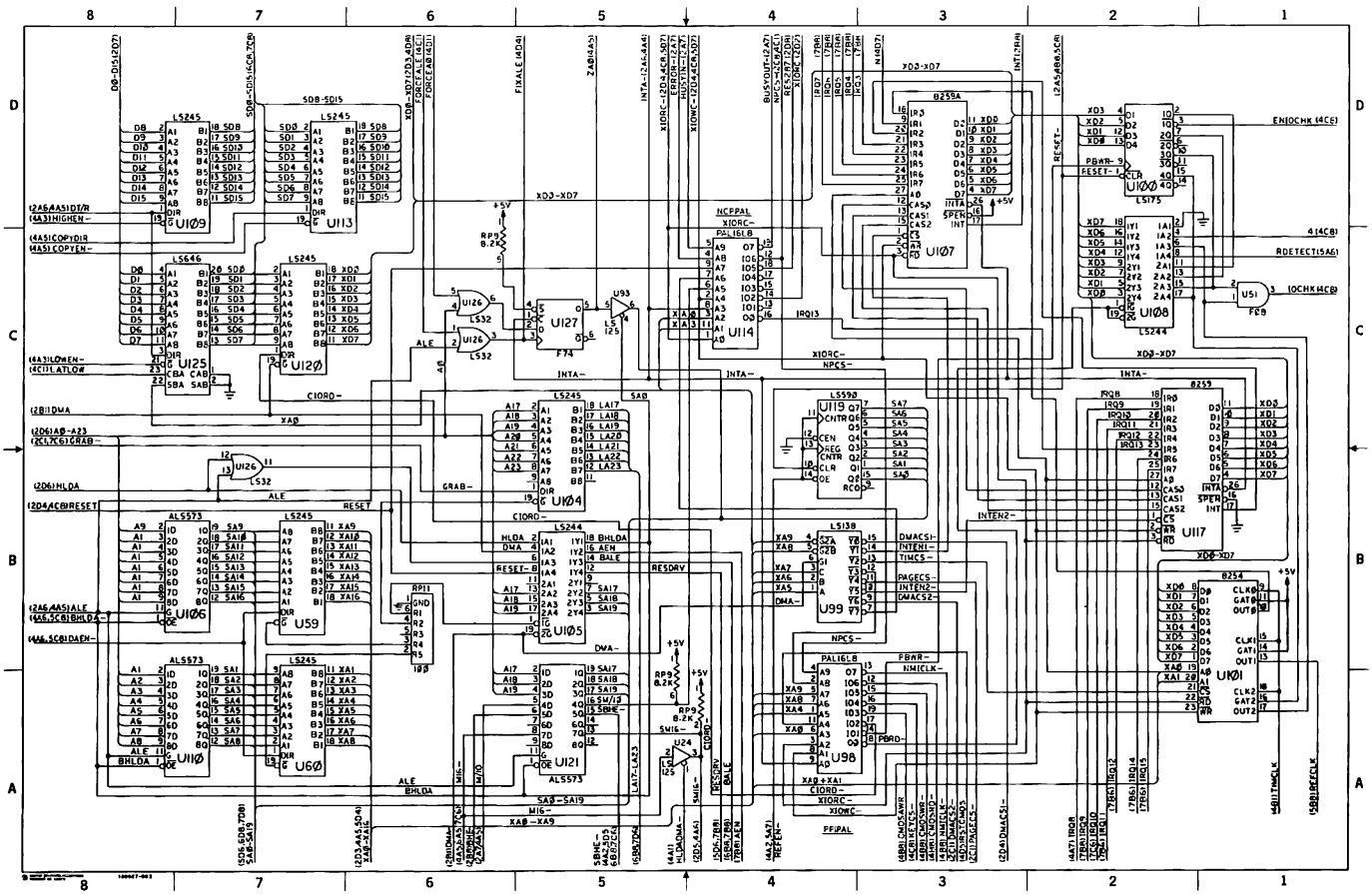


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 3 of 7)

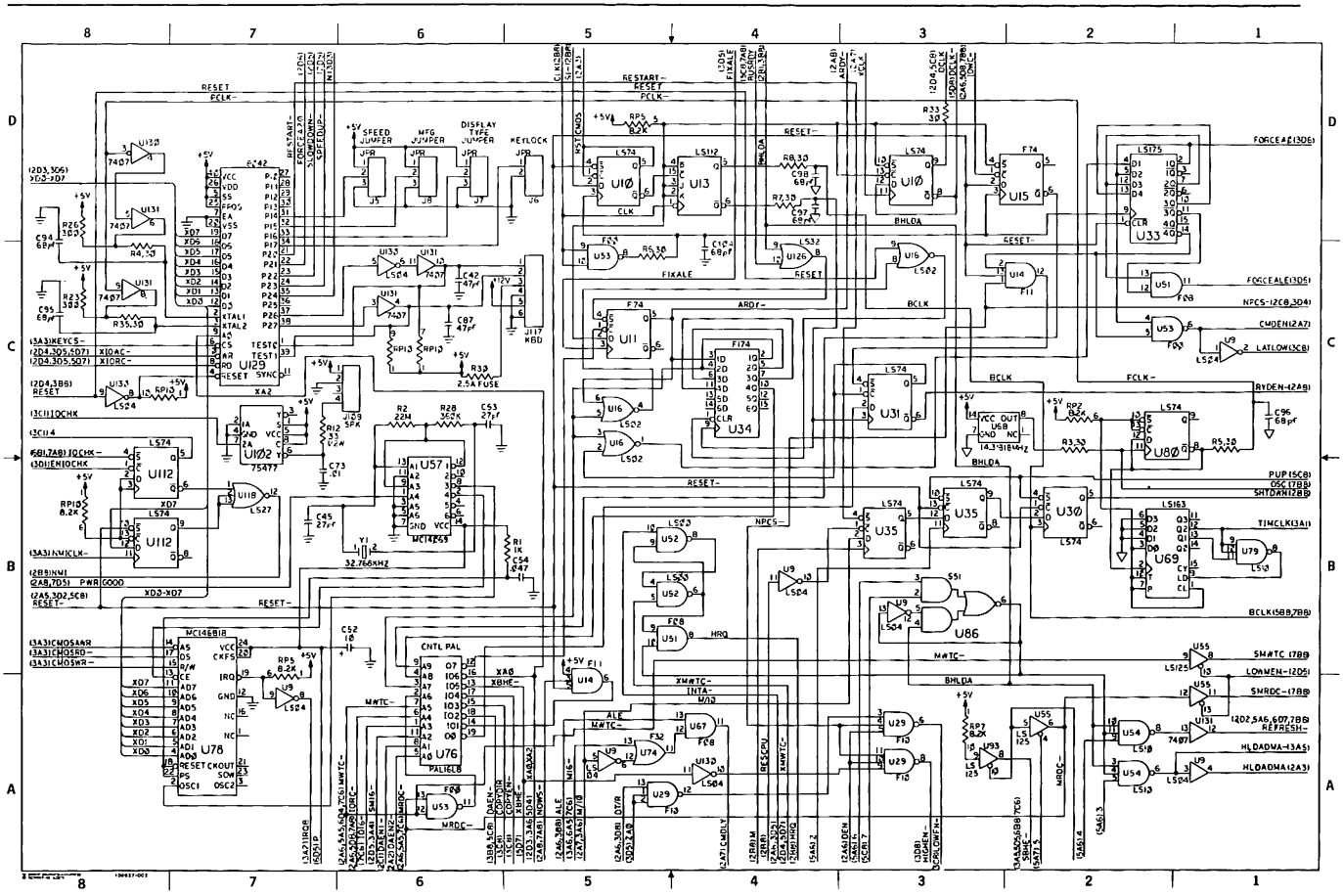


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 4 of 7)

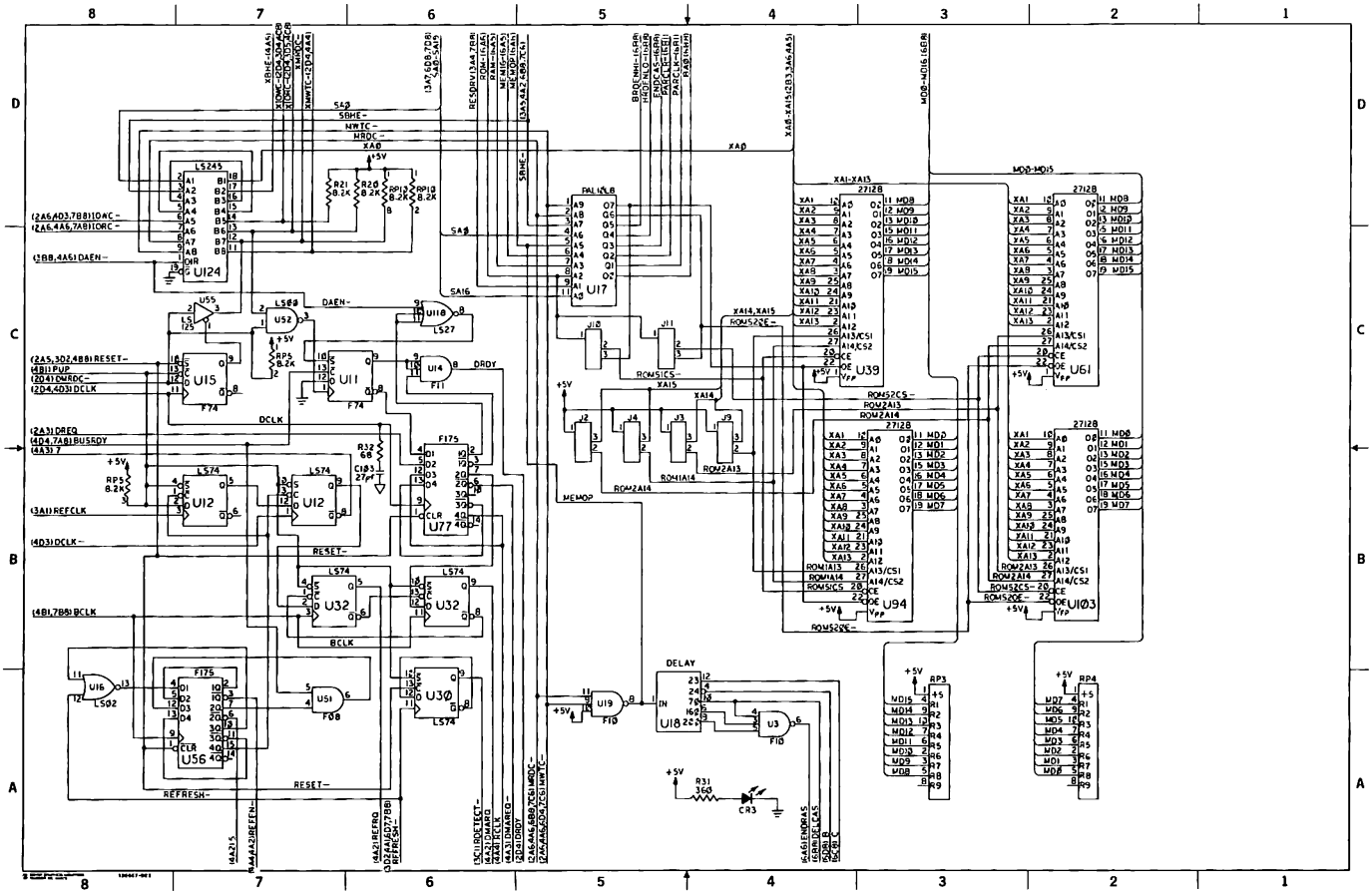


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 5 of 7)

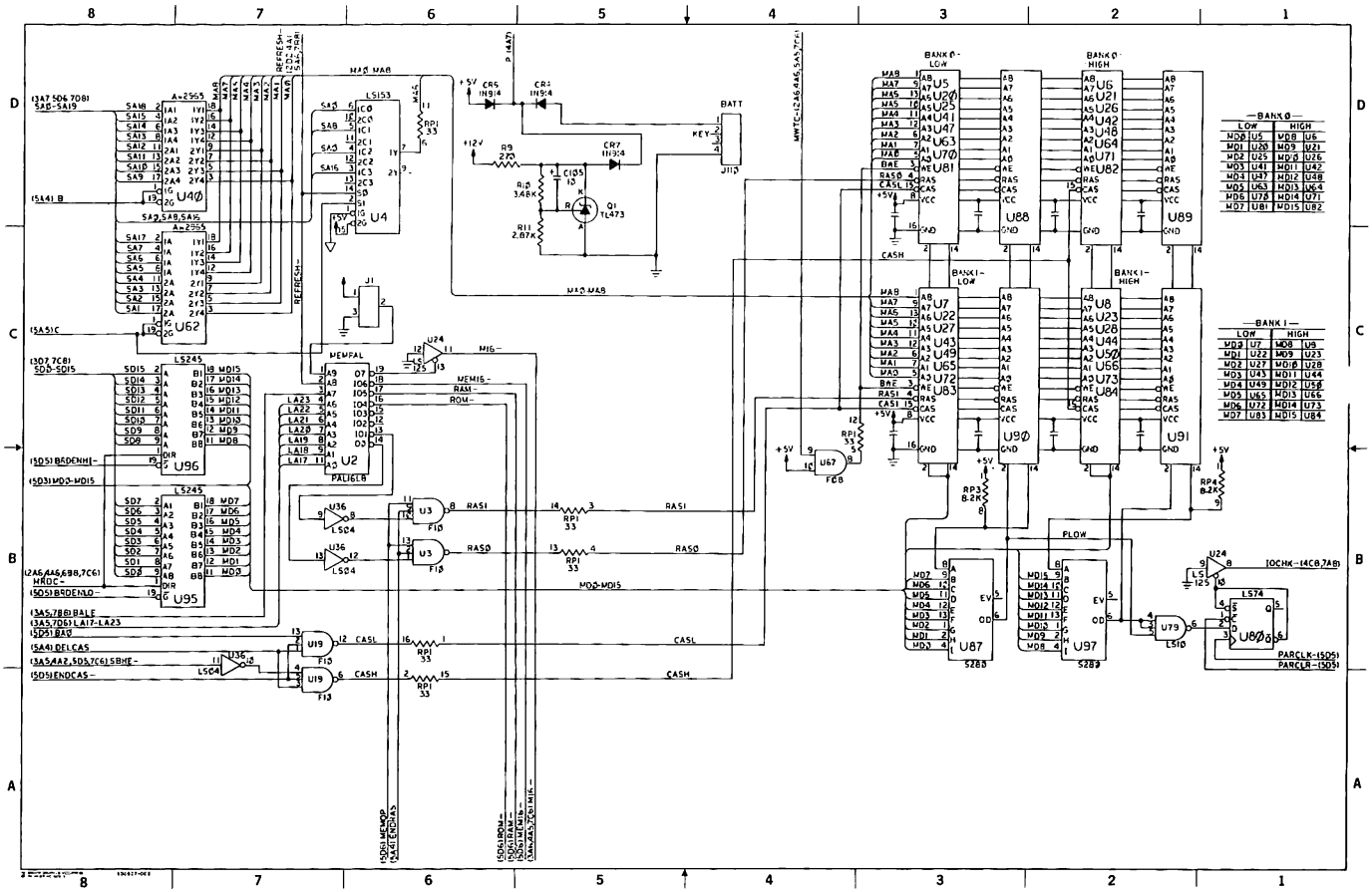


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 6 of 7)

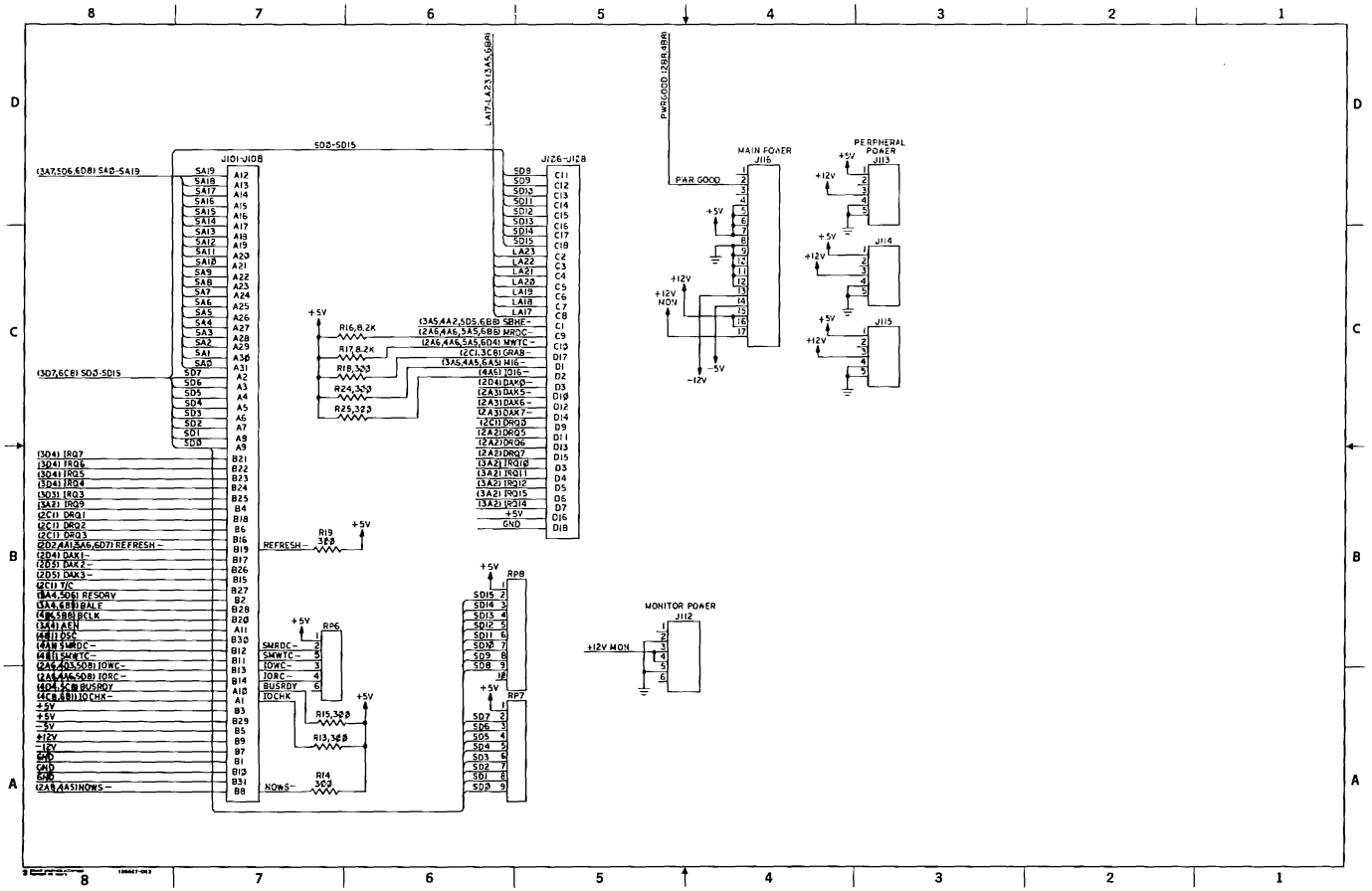


Figure 2-41. COMPAQ PORTABLE 286 System Board Schematics (Page 7 of 7)

Figure 2-42 shows the component layout for the COMPAQ DESKPRO 286 Version 1 System Board. Figure 2-43 shows the schematics for the COMPAQ DESKPRO 286 Version 1 System Board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

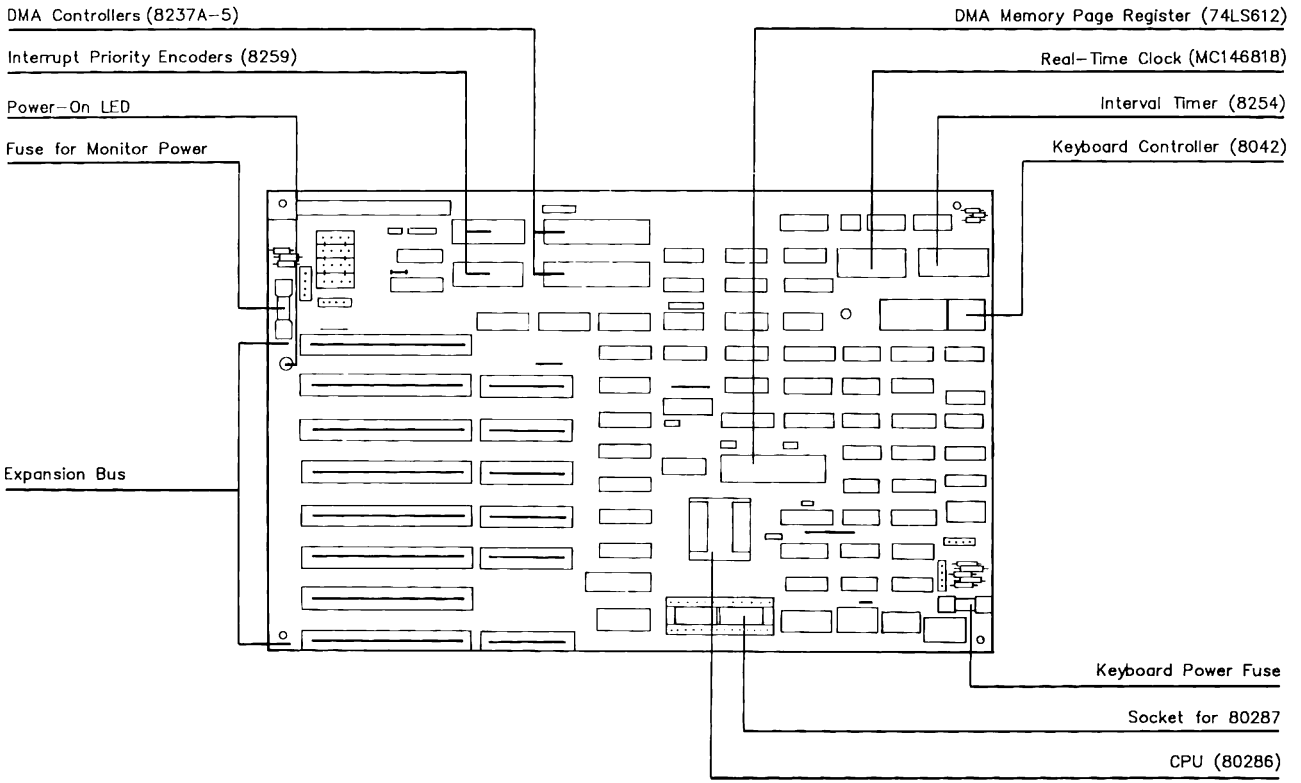


Figure 2-42. COMPAQ DESKPRO 286 Version 1 System Board Component Layout (Page 1 of 1)

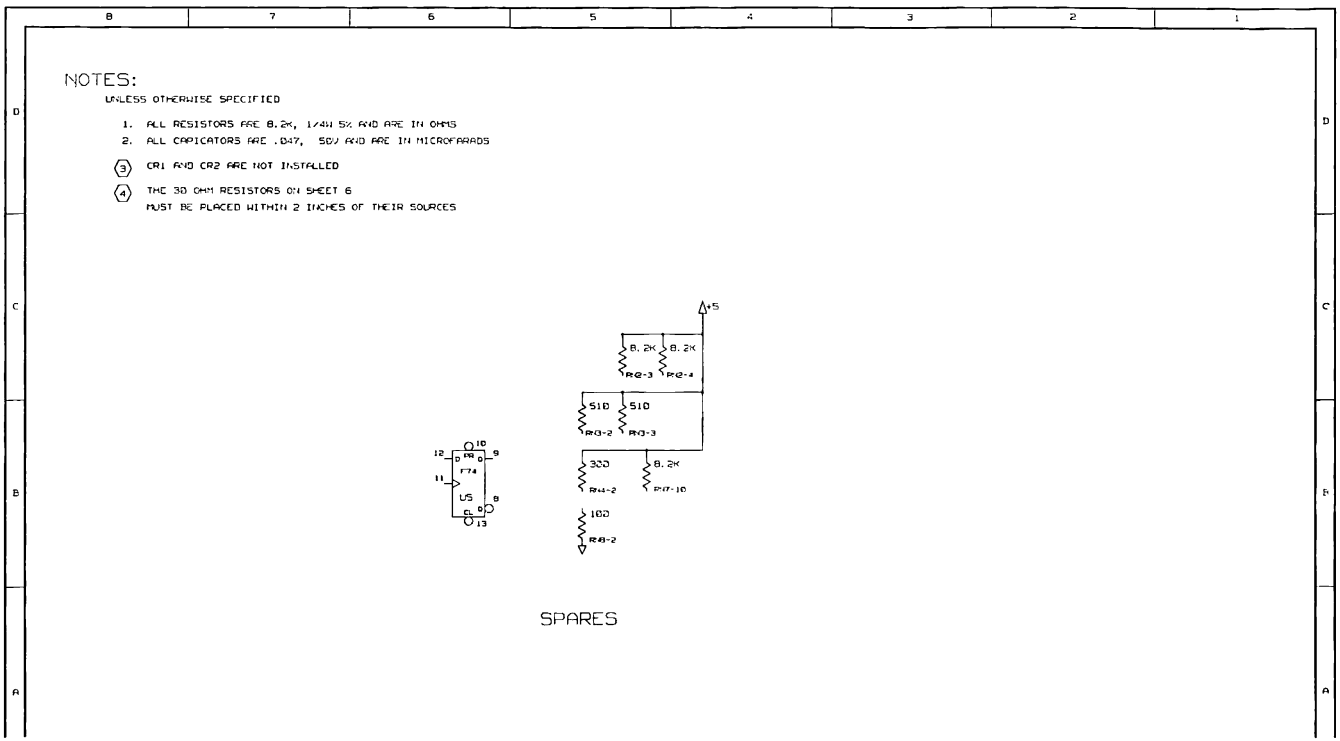


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 1 of 8)

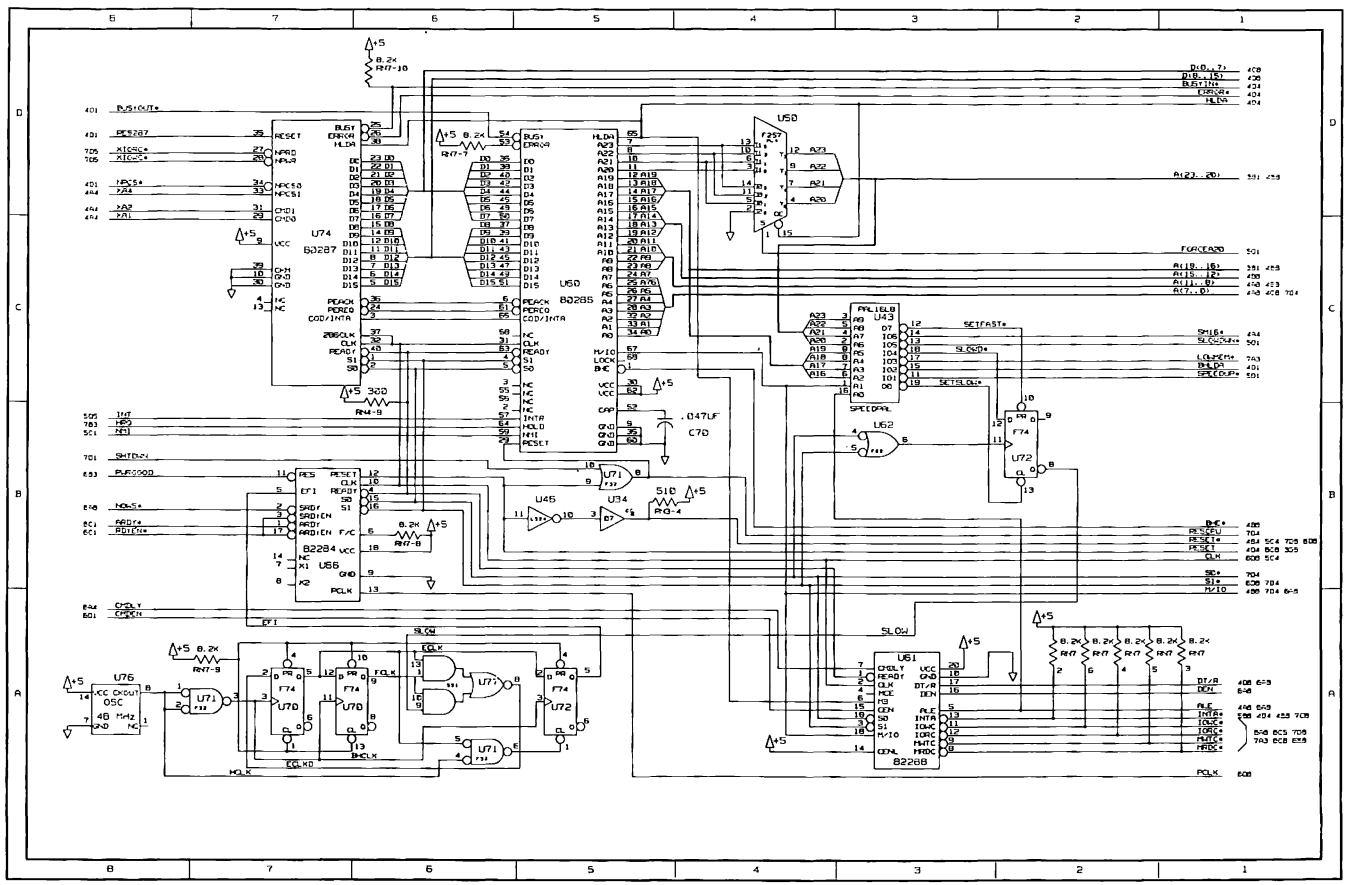


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 2 of 8)

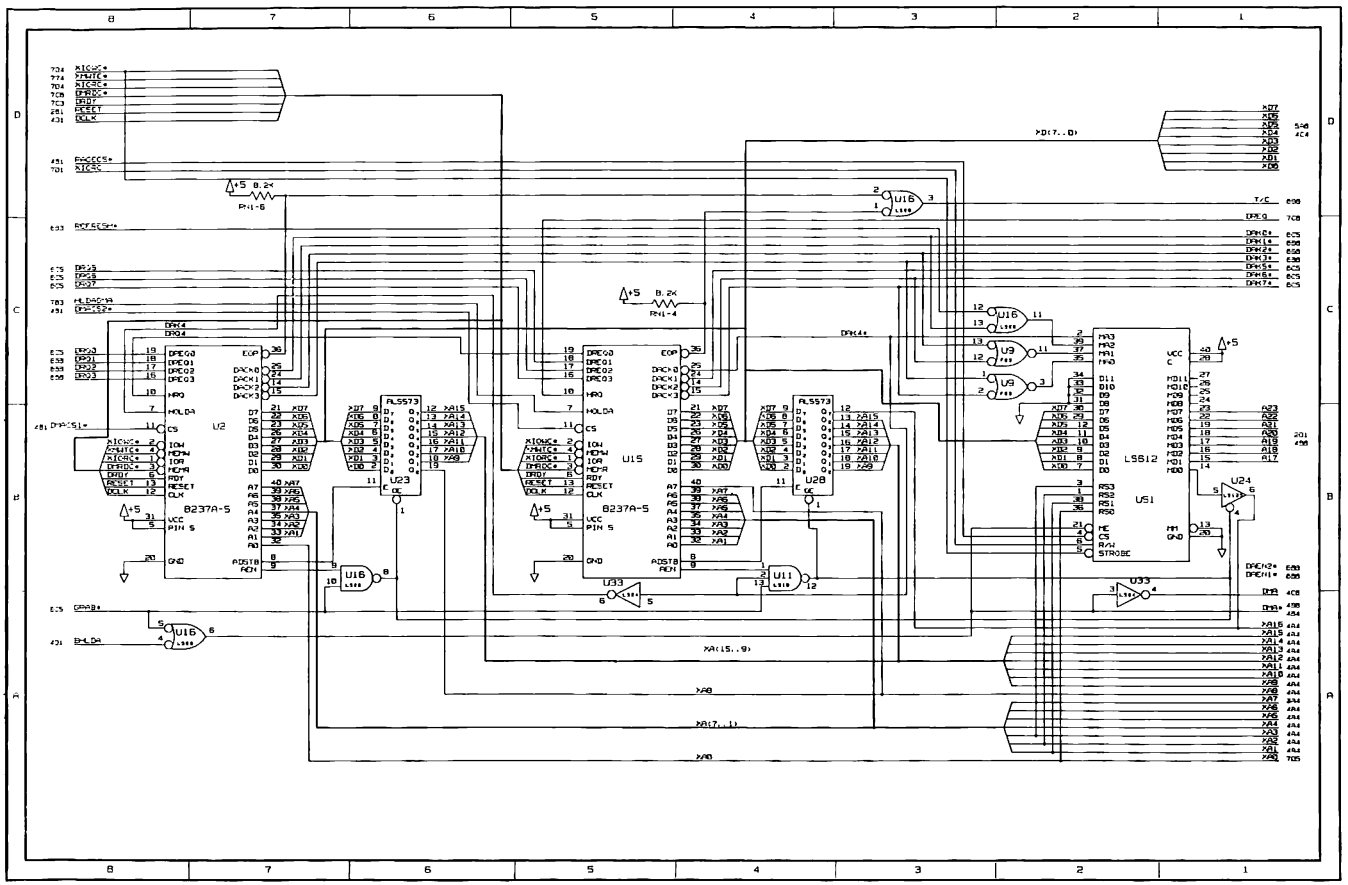


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 3 of 8)

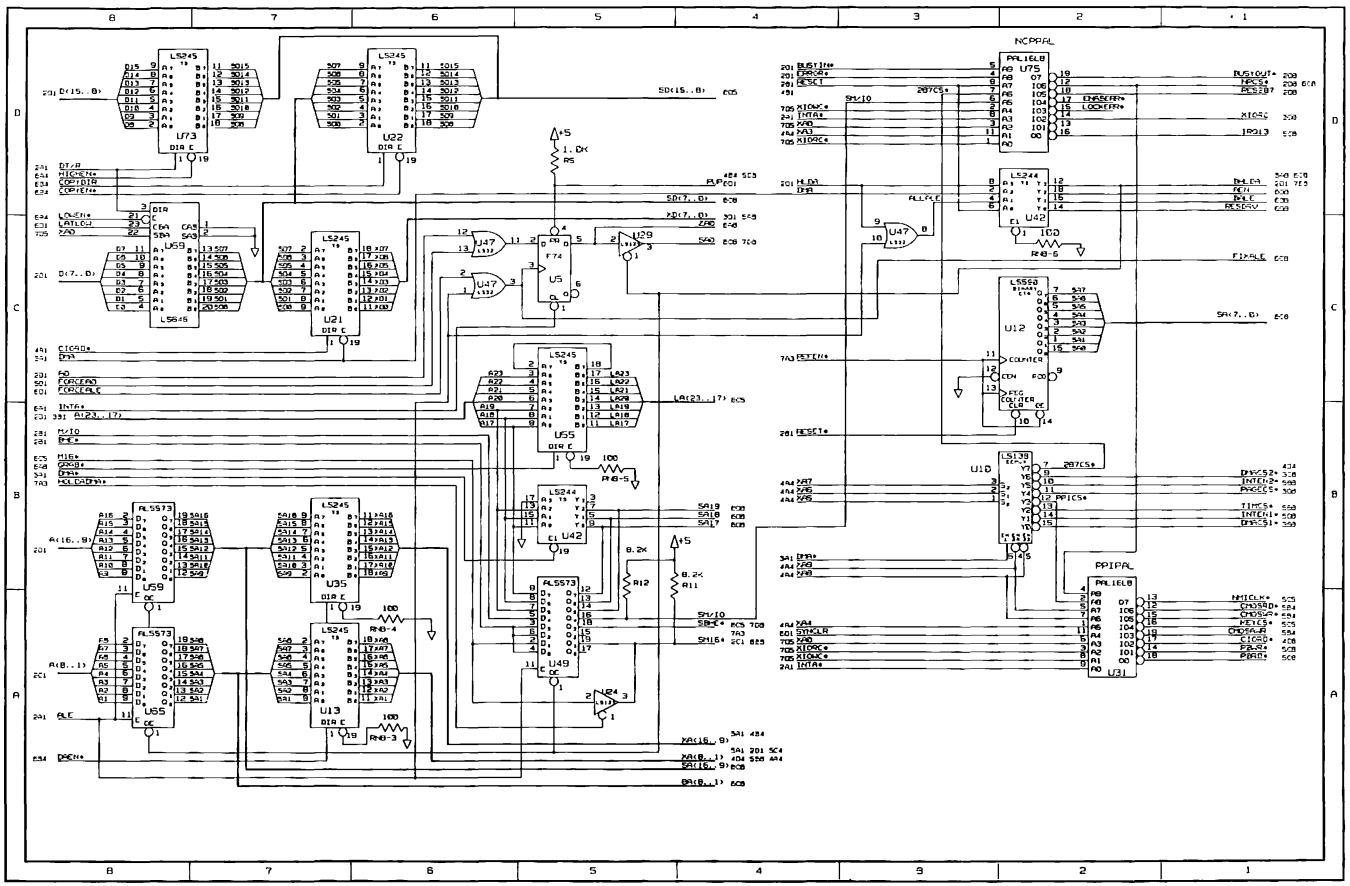


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 4 of 8)

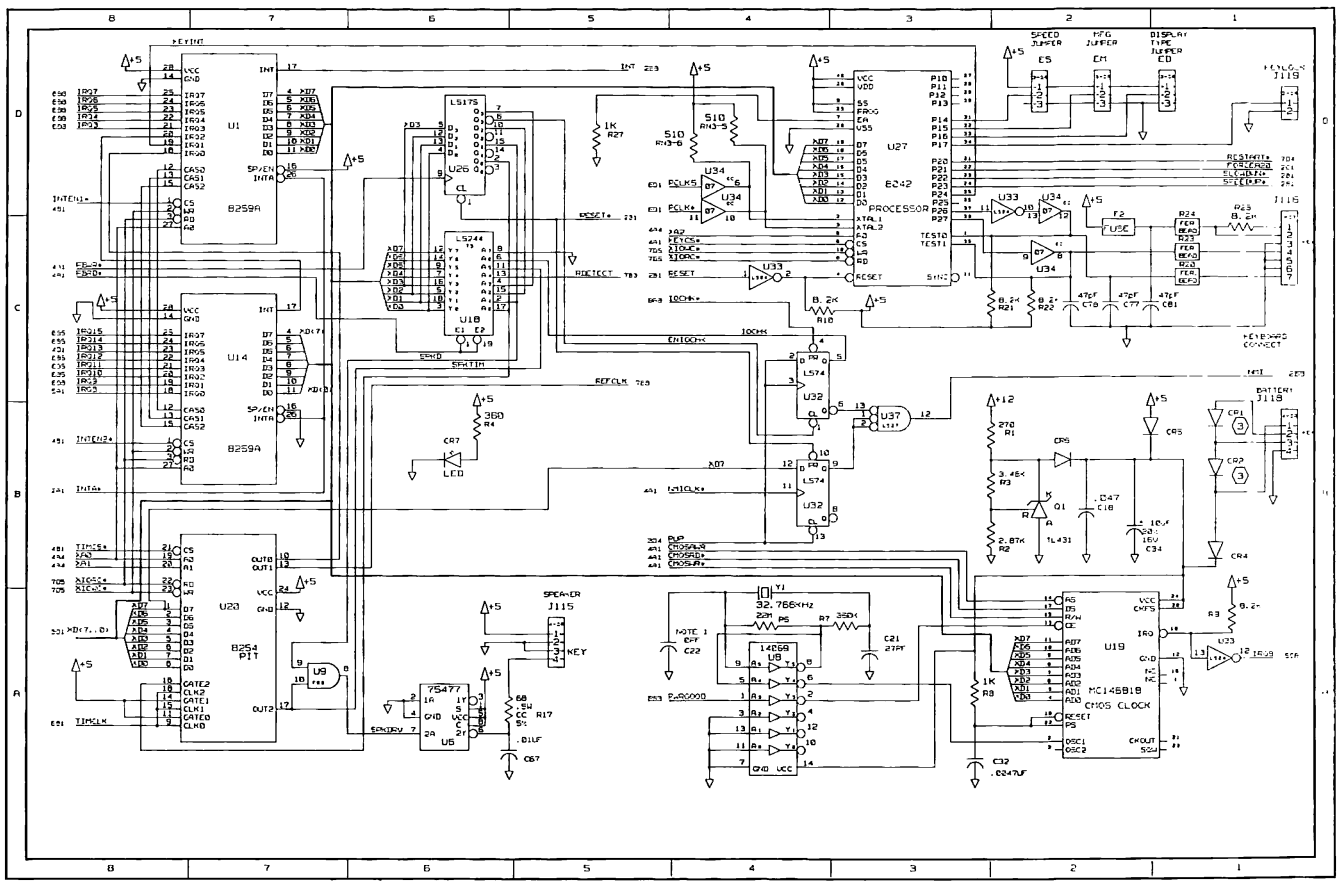


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 5 of 8)

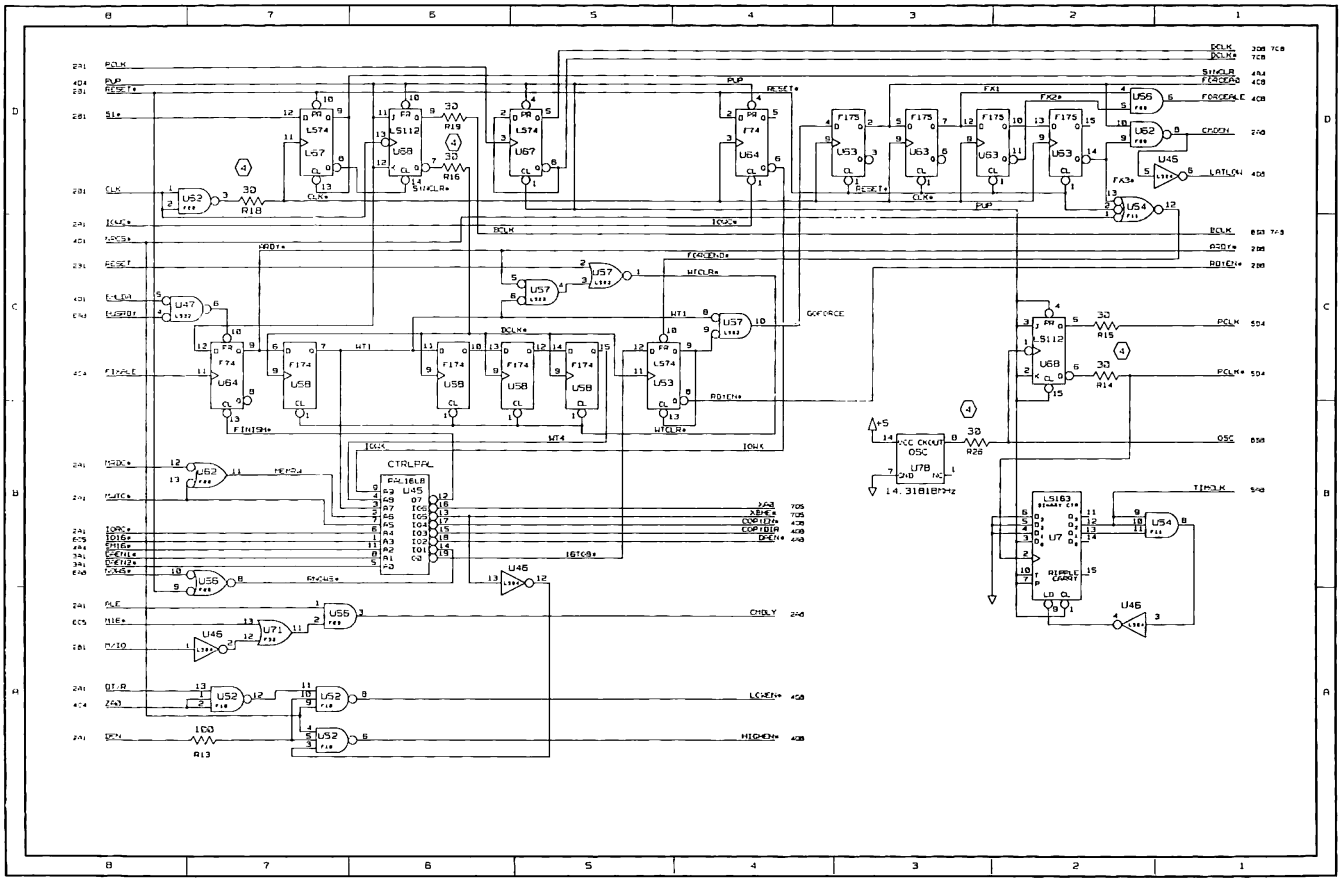


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 6 of 8)

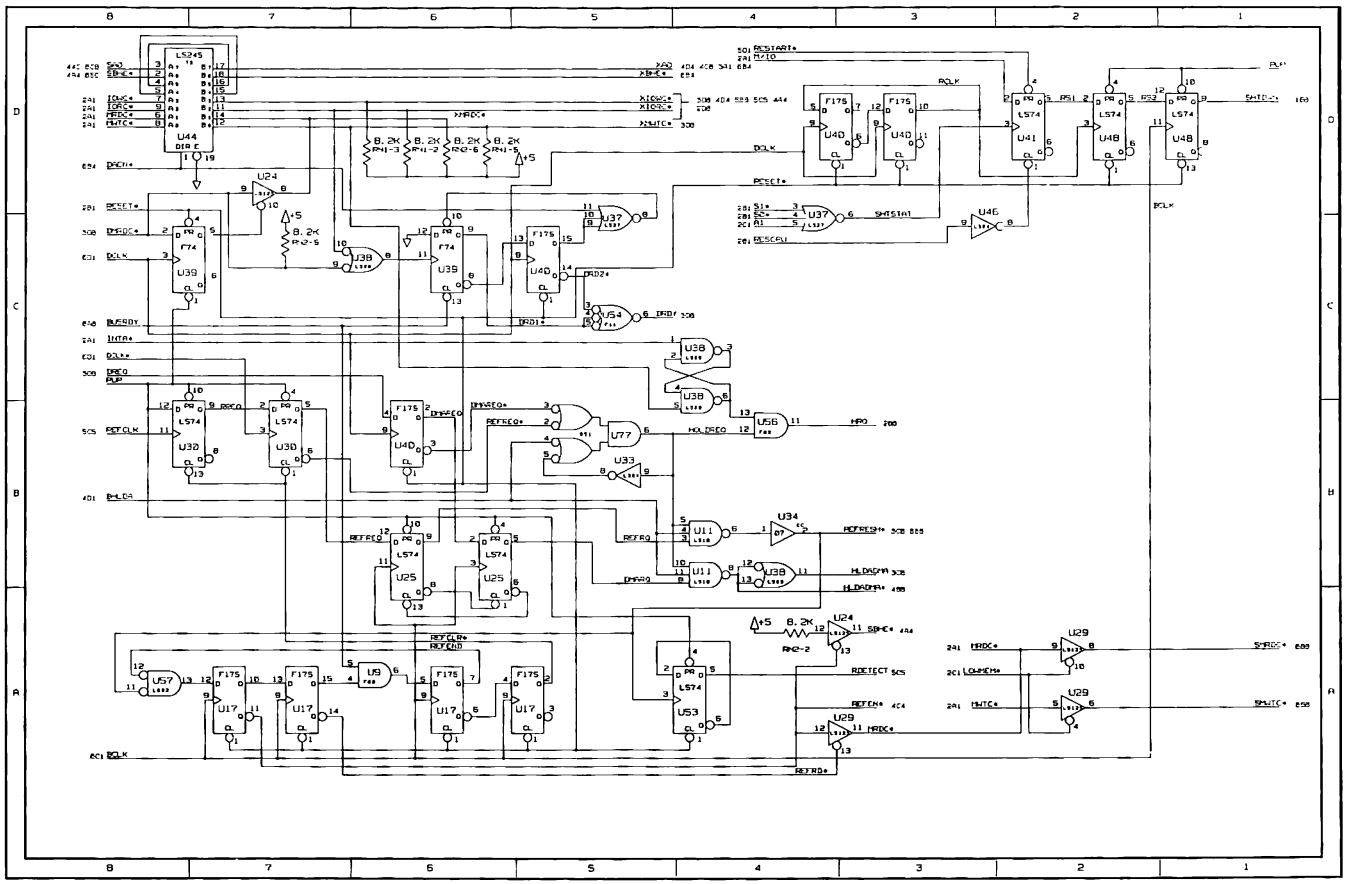


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 7 of 8)

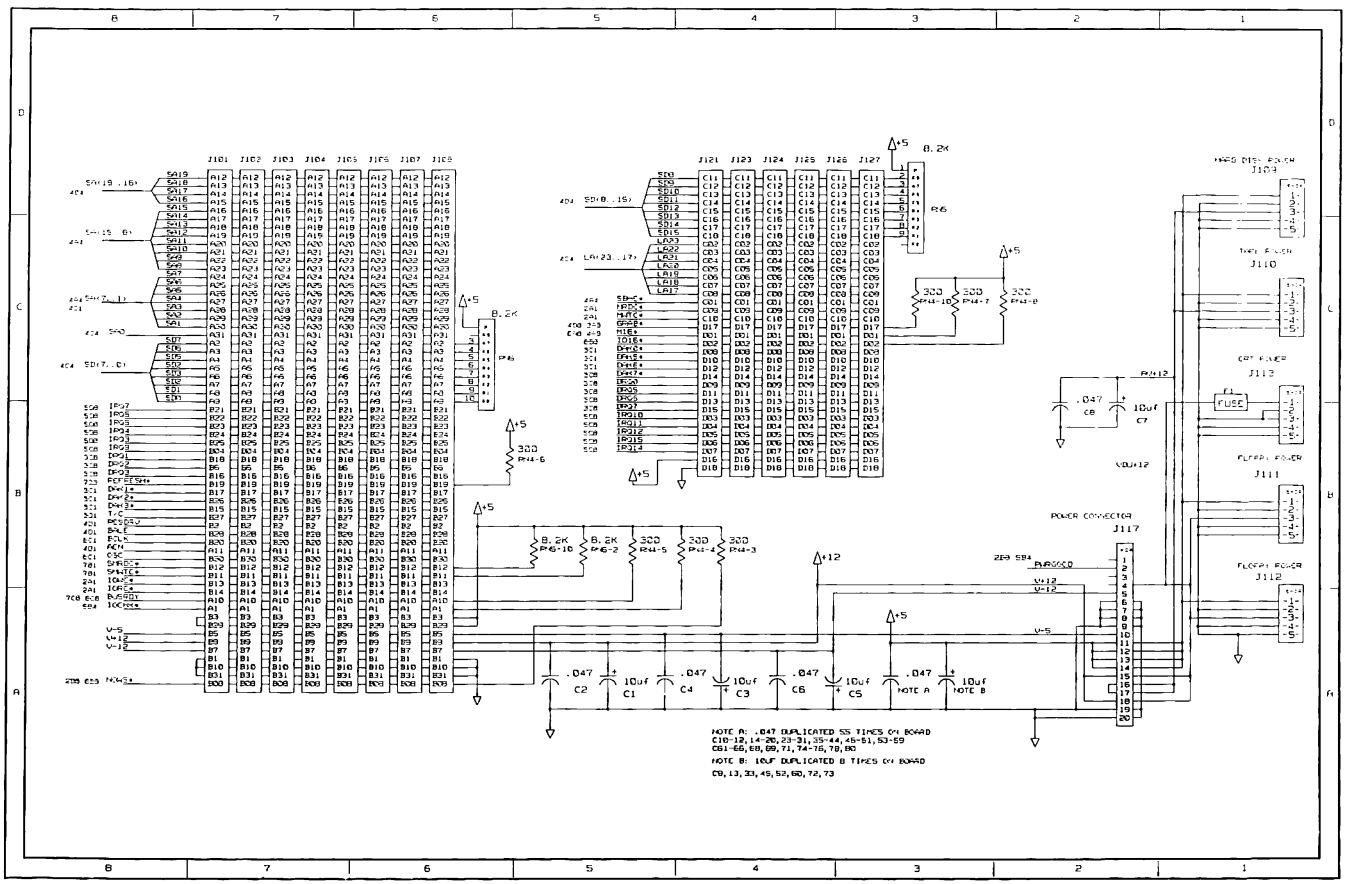


Figure 2-43. COMPAQ DESKPRO 286 Version 1 System Board Schematics (Page 8 of 8)

Figure 2-44 shows the component layout for the COMPAQ DESKPRO 286 Version 2 System Board. Figure 2-45 shows the schematics for the COMPAQ DESKPRO 286 Version 2 System Board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

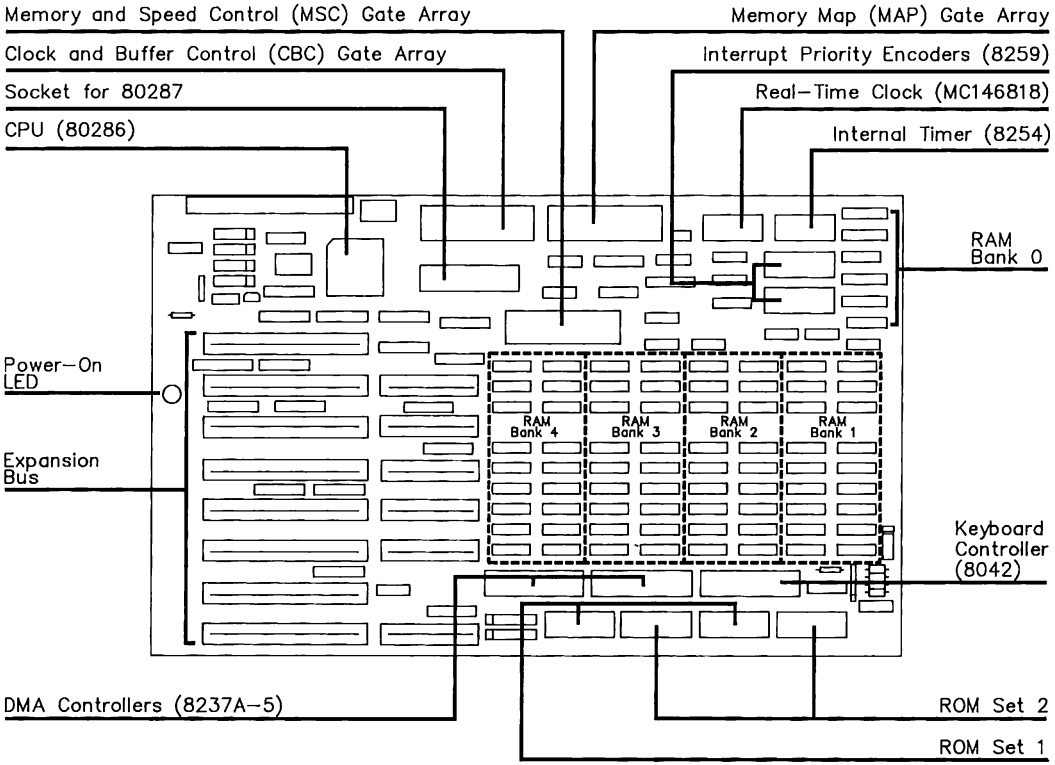


Figure 2-44. COMPAQ DESKPRO 286 Version 2 System Board Component Layout (Page 1 of 1)

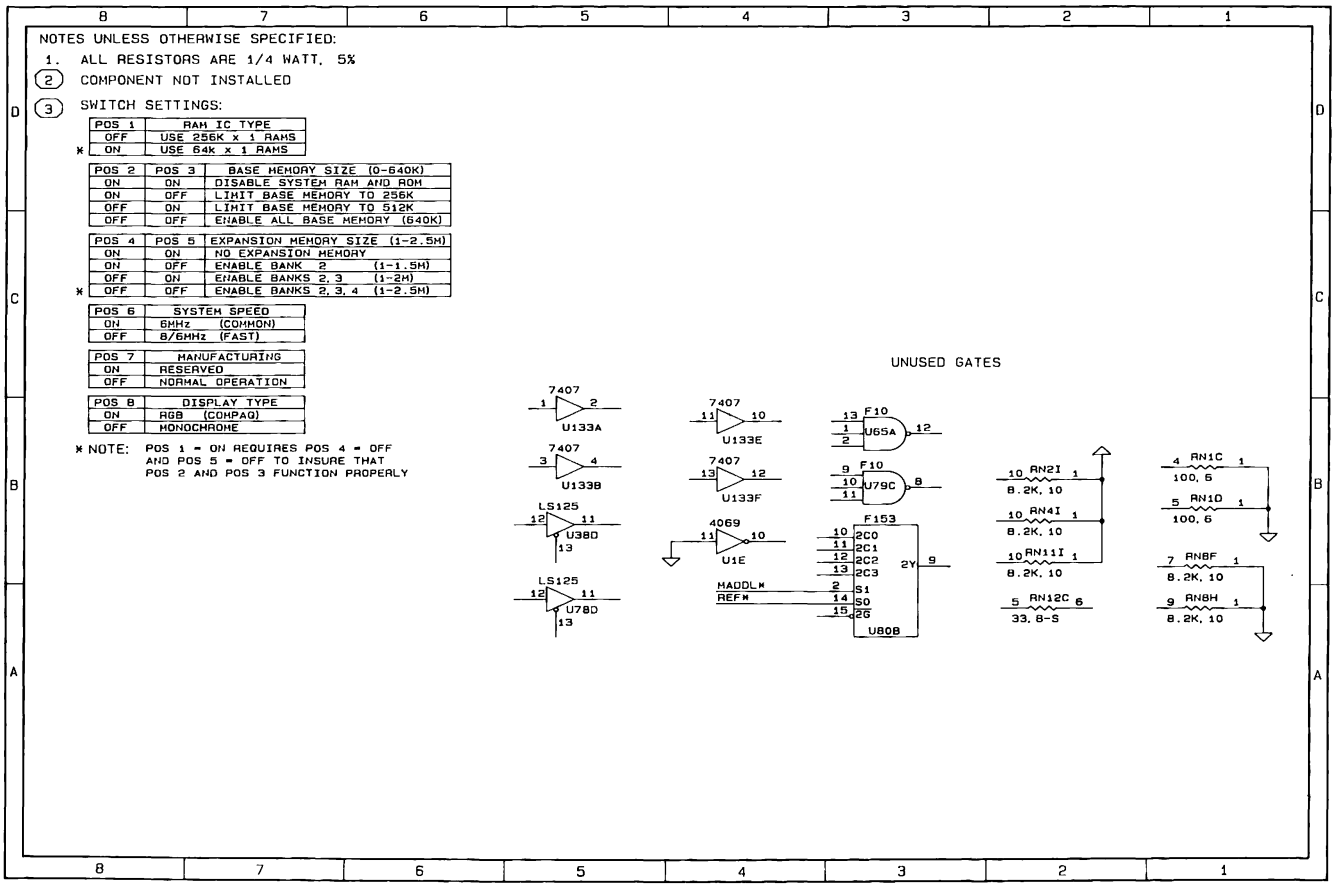


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 1 of 18)

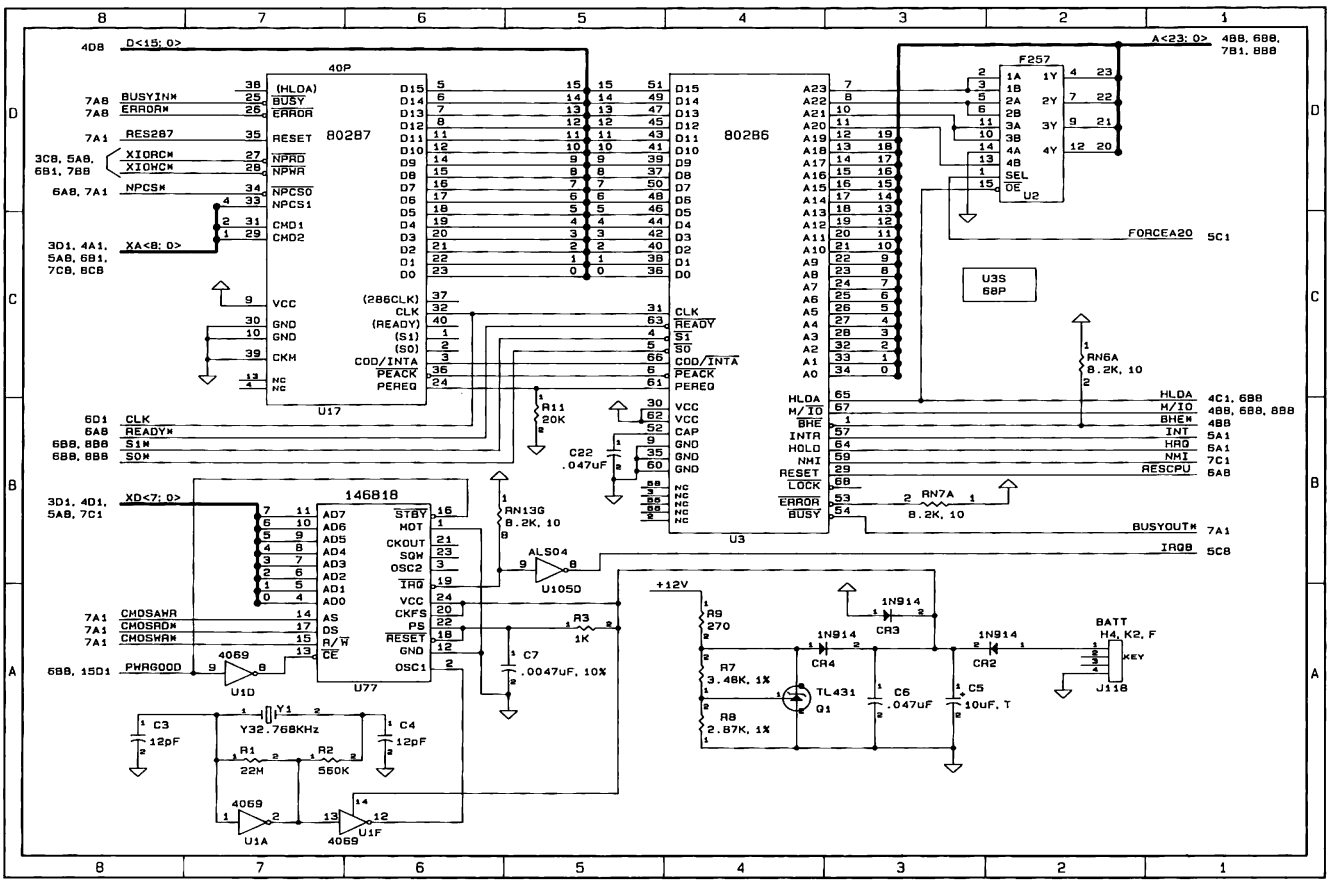


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 2 of 18)

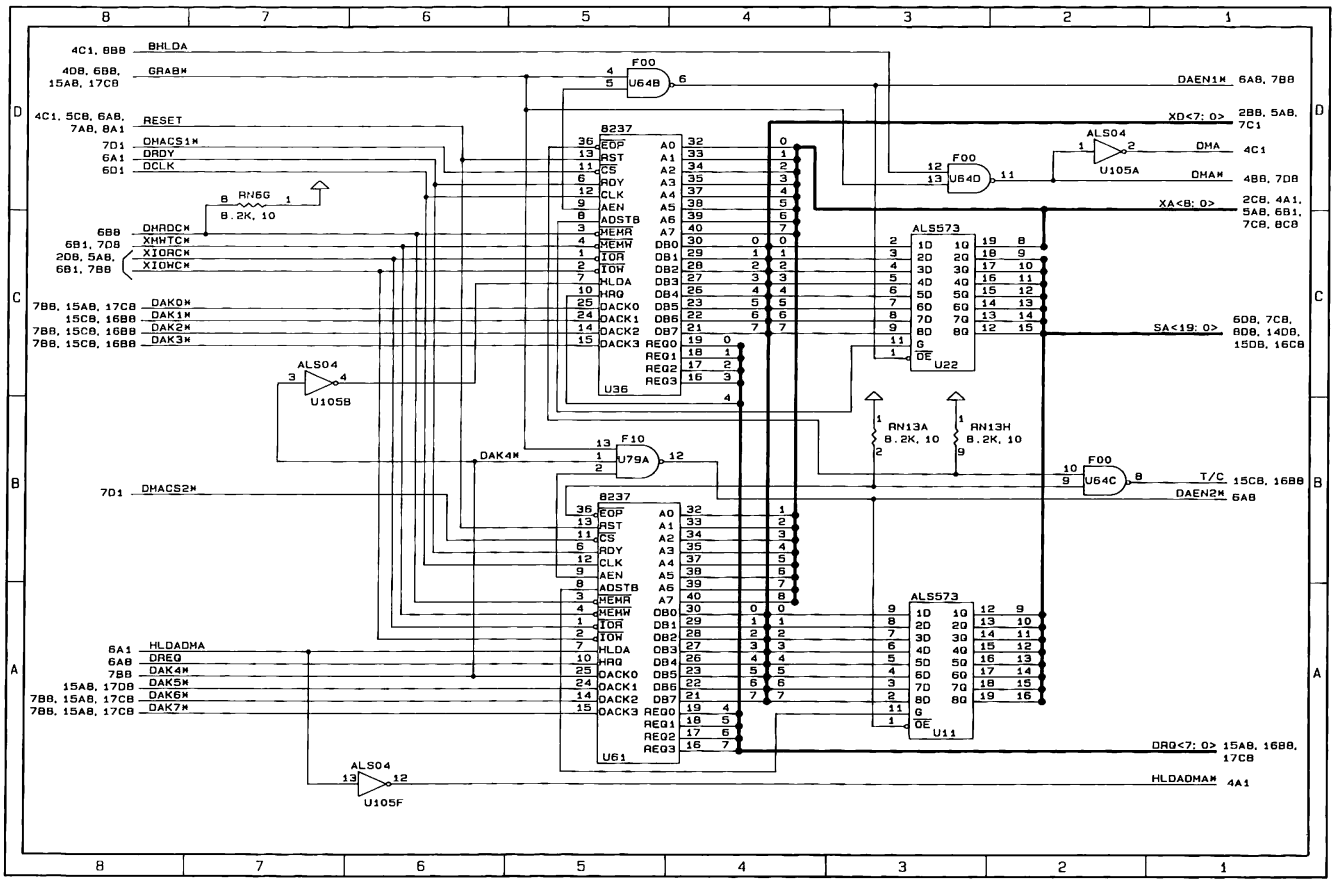


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 3 of 18)

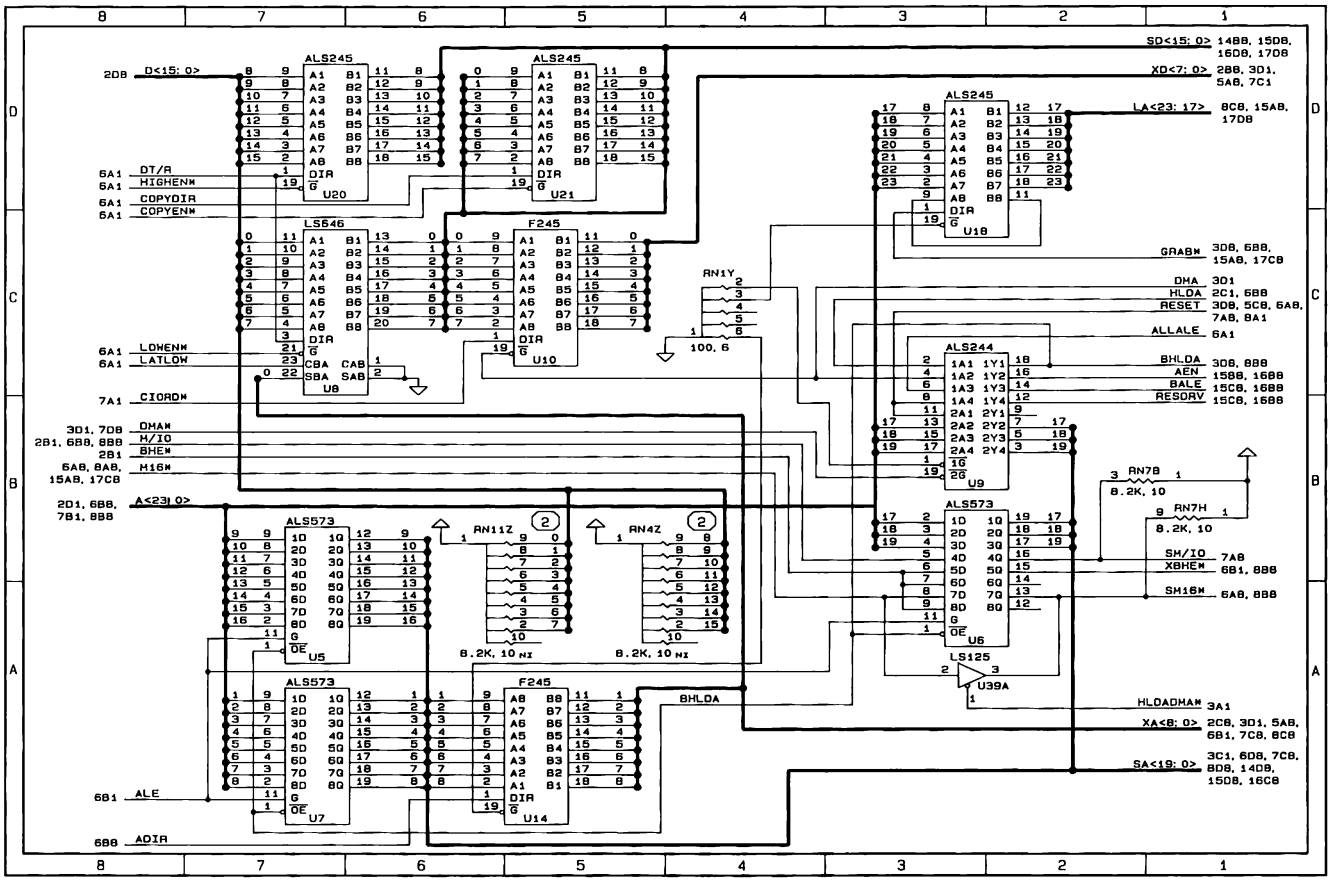


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 4 of 18)

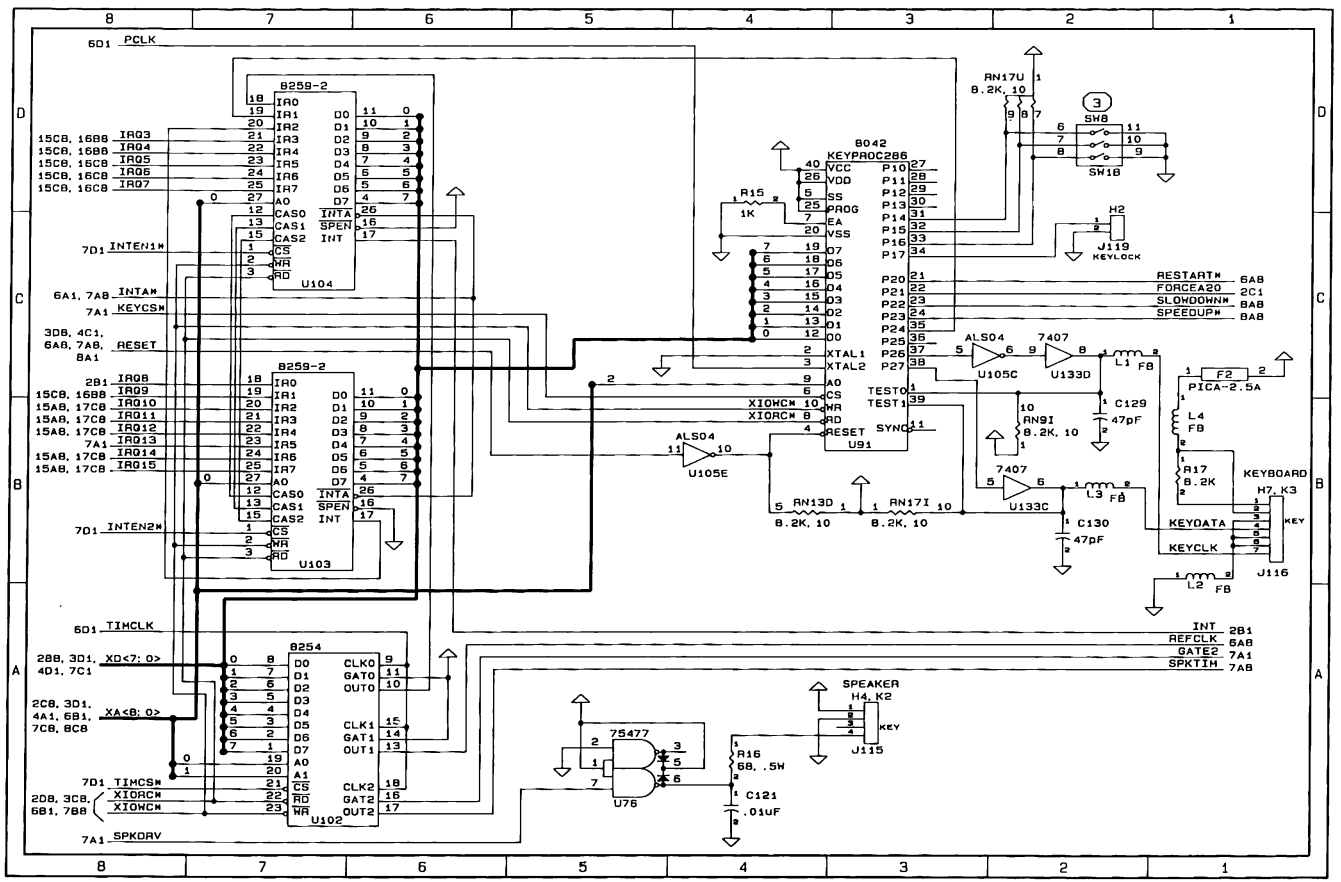


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 5 of 18)

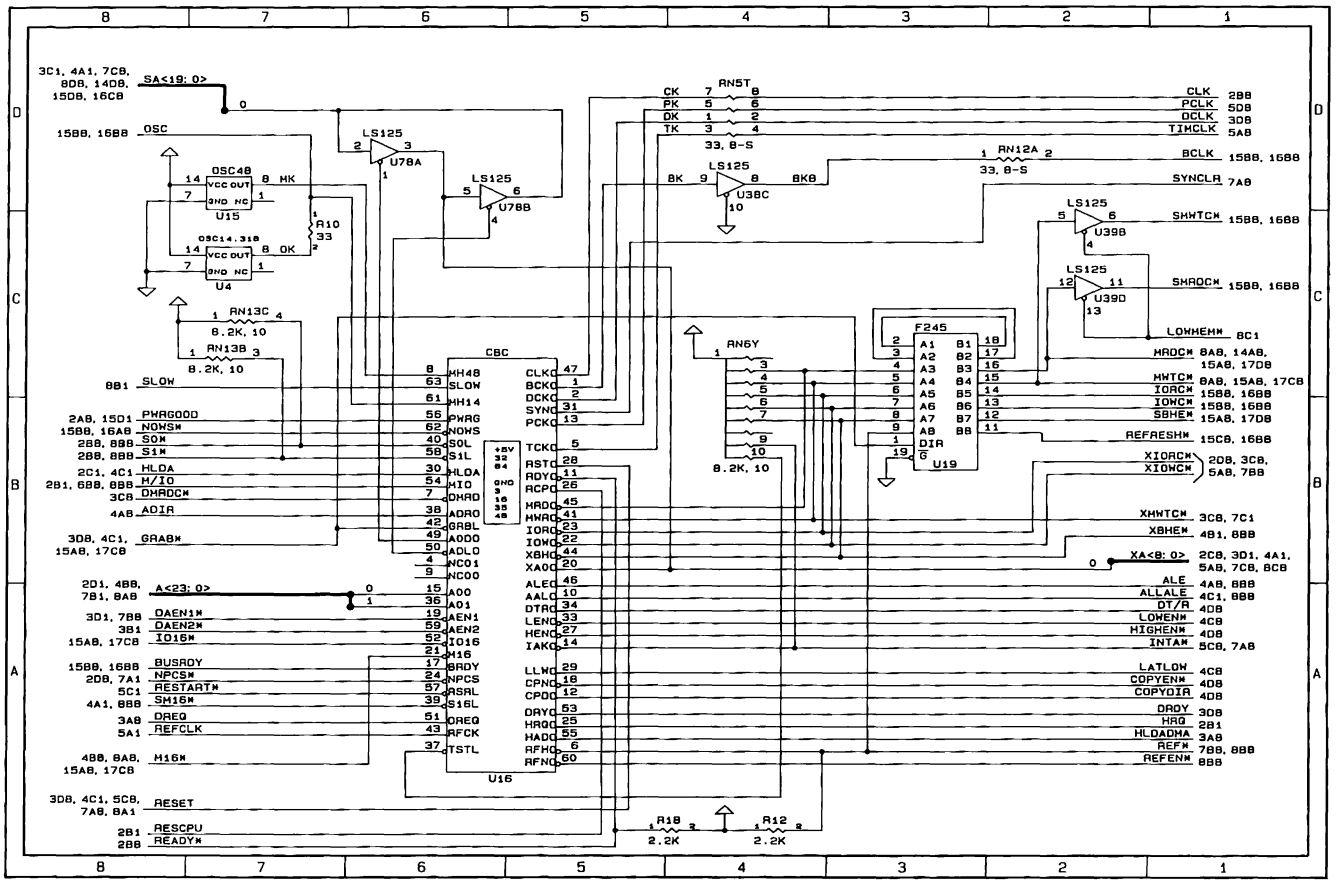


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 6 of 18)

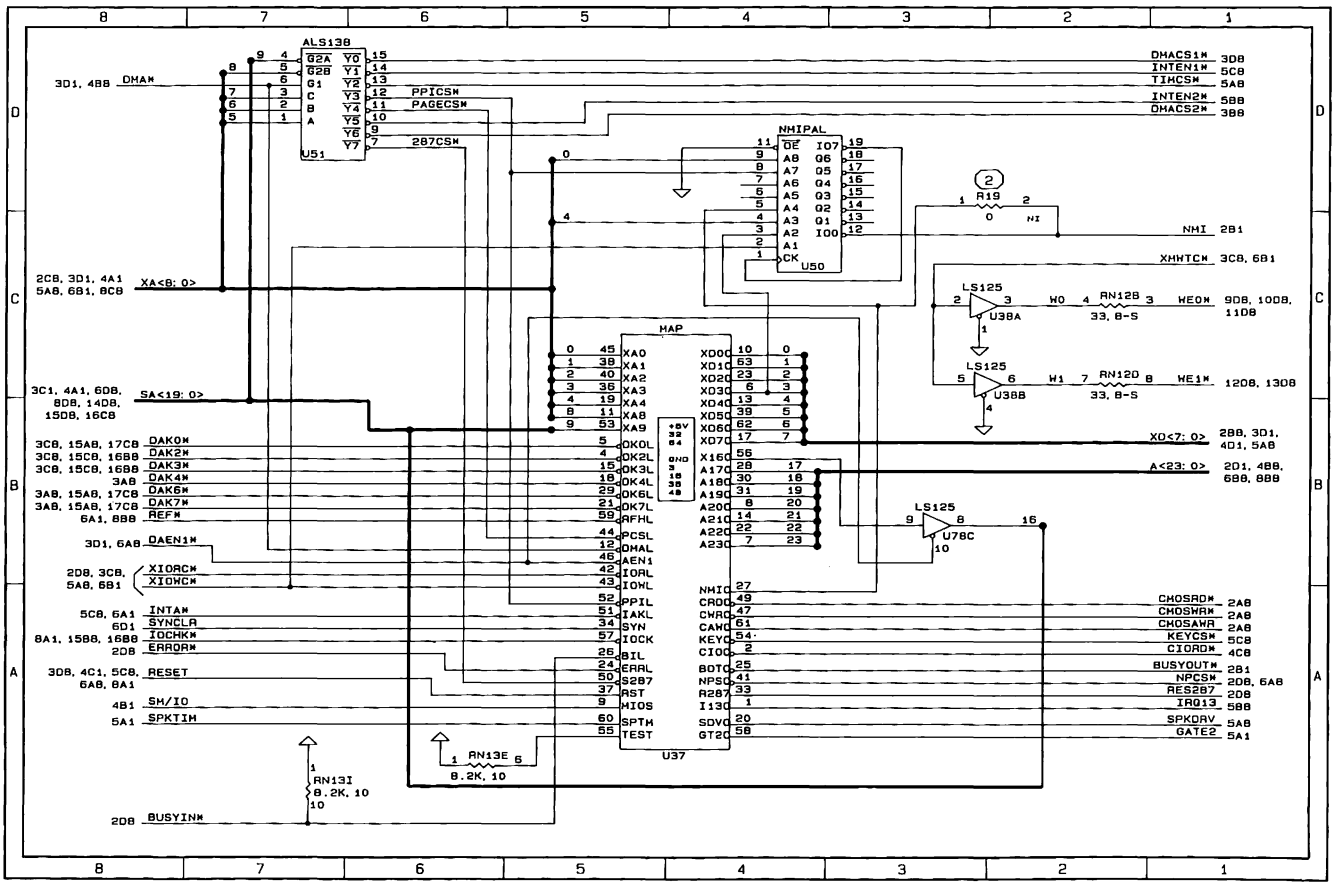


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 7 of 18)

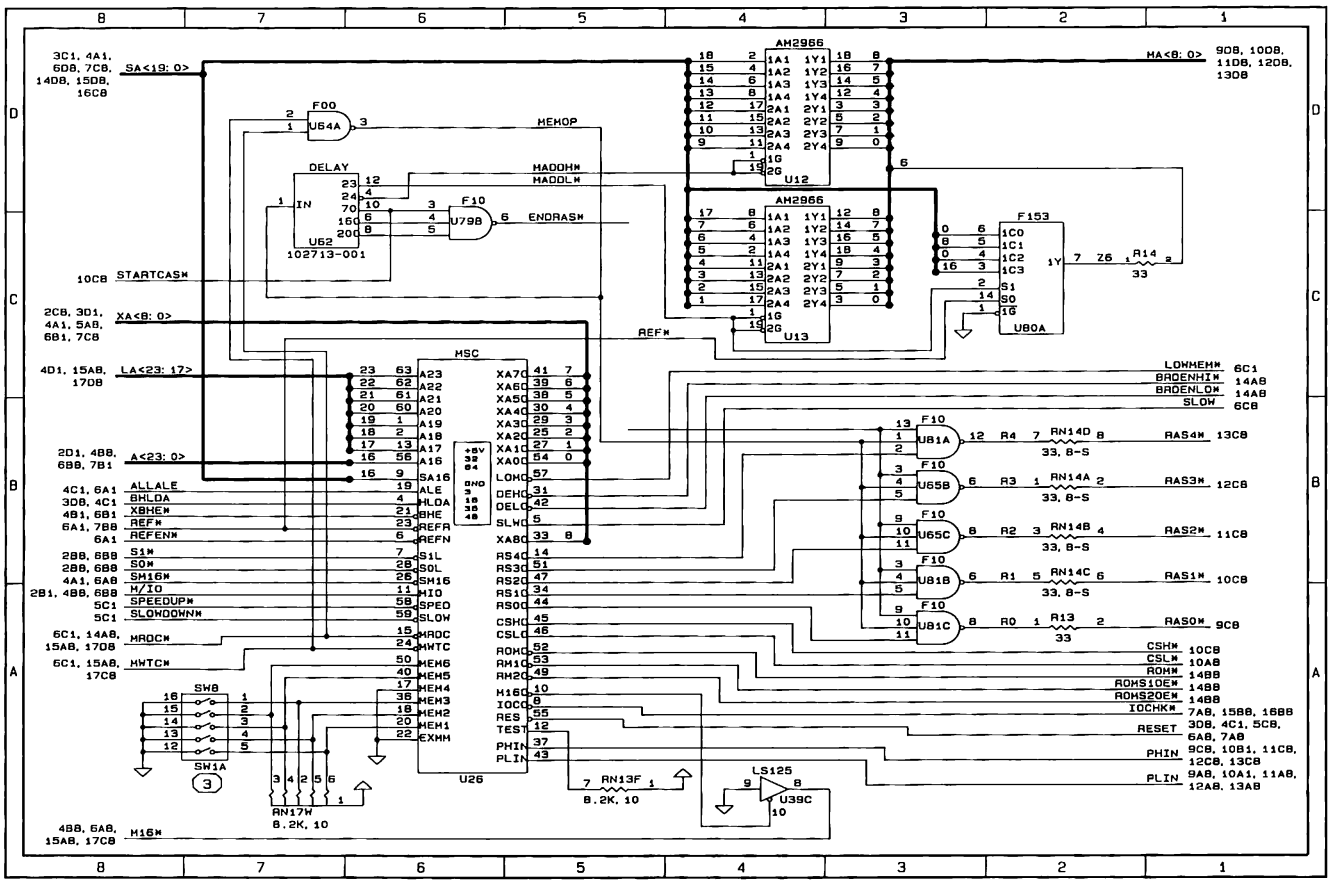


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 8 of 18)

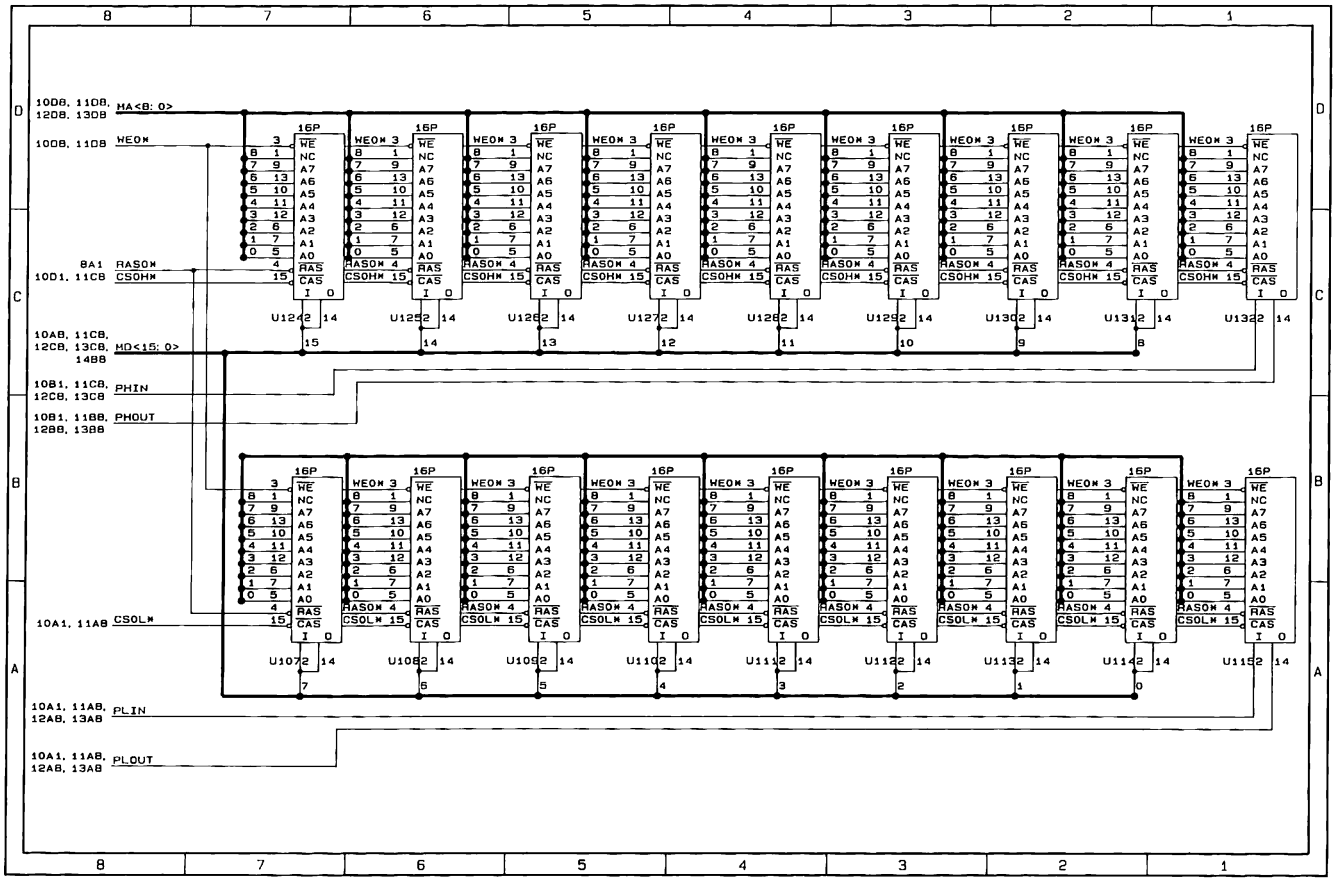


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 9 of 18)

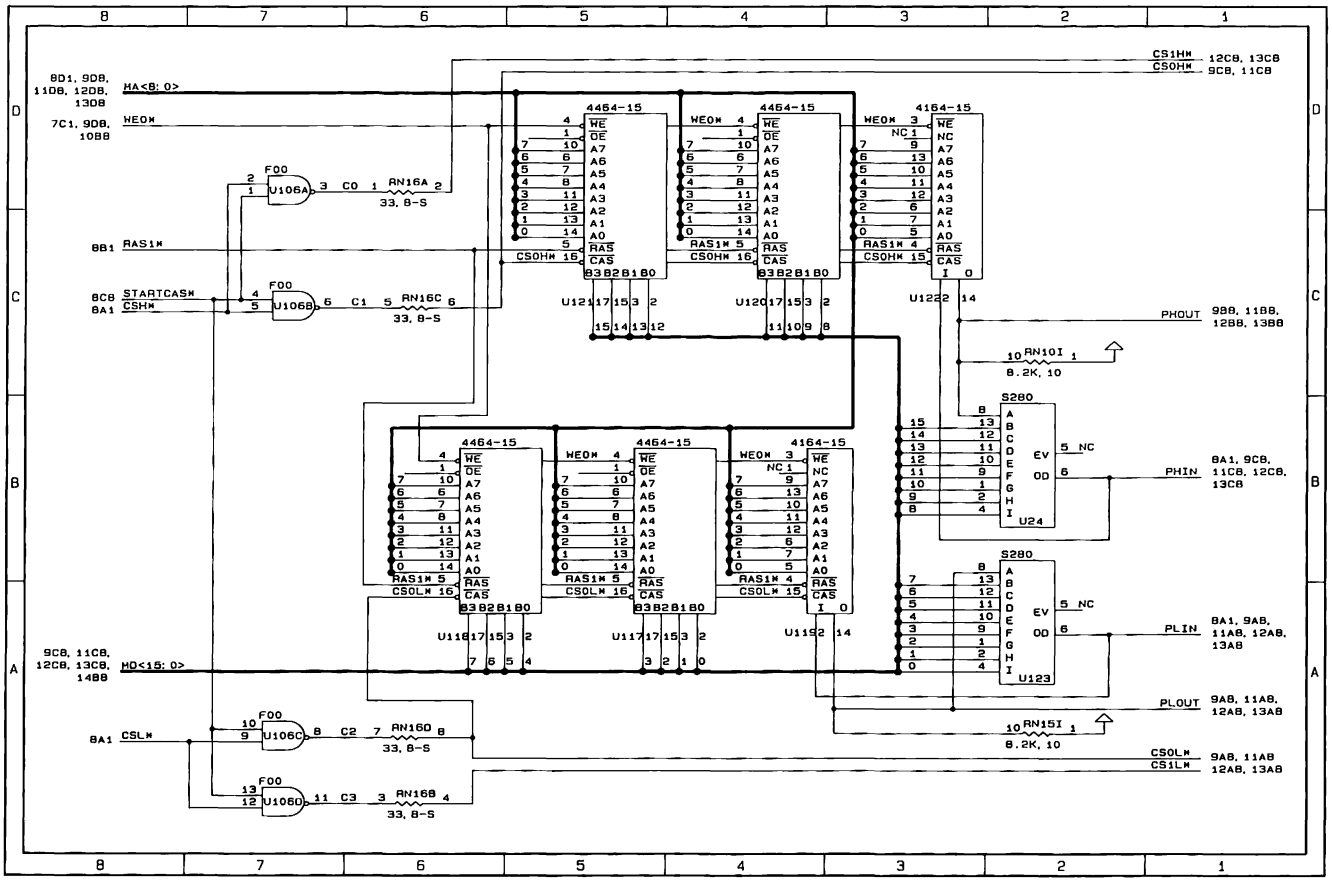


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 10 of 18)

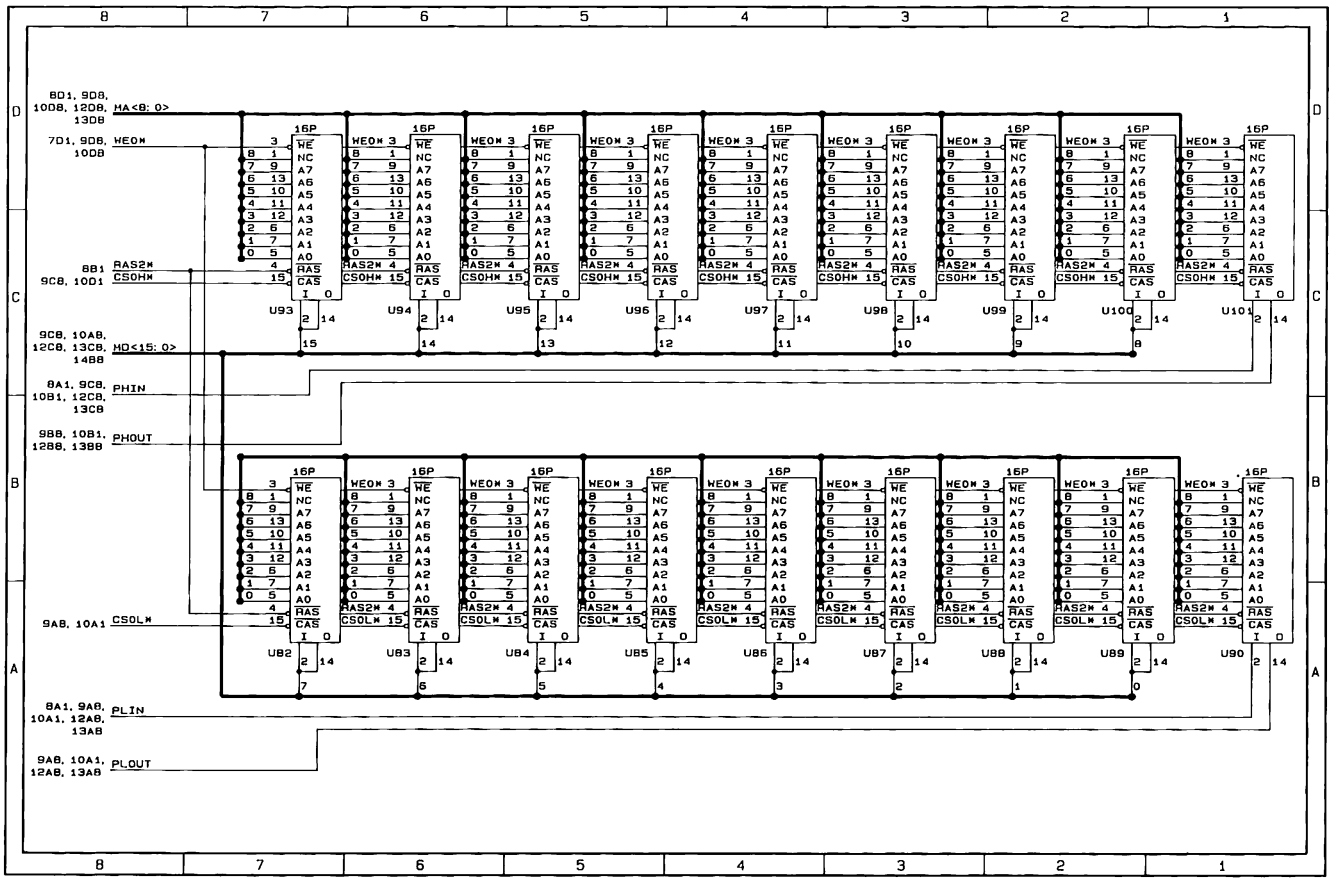


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 11 of 18)

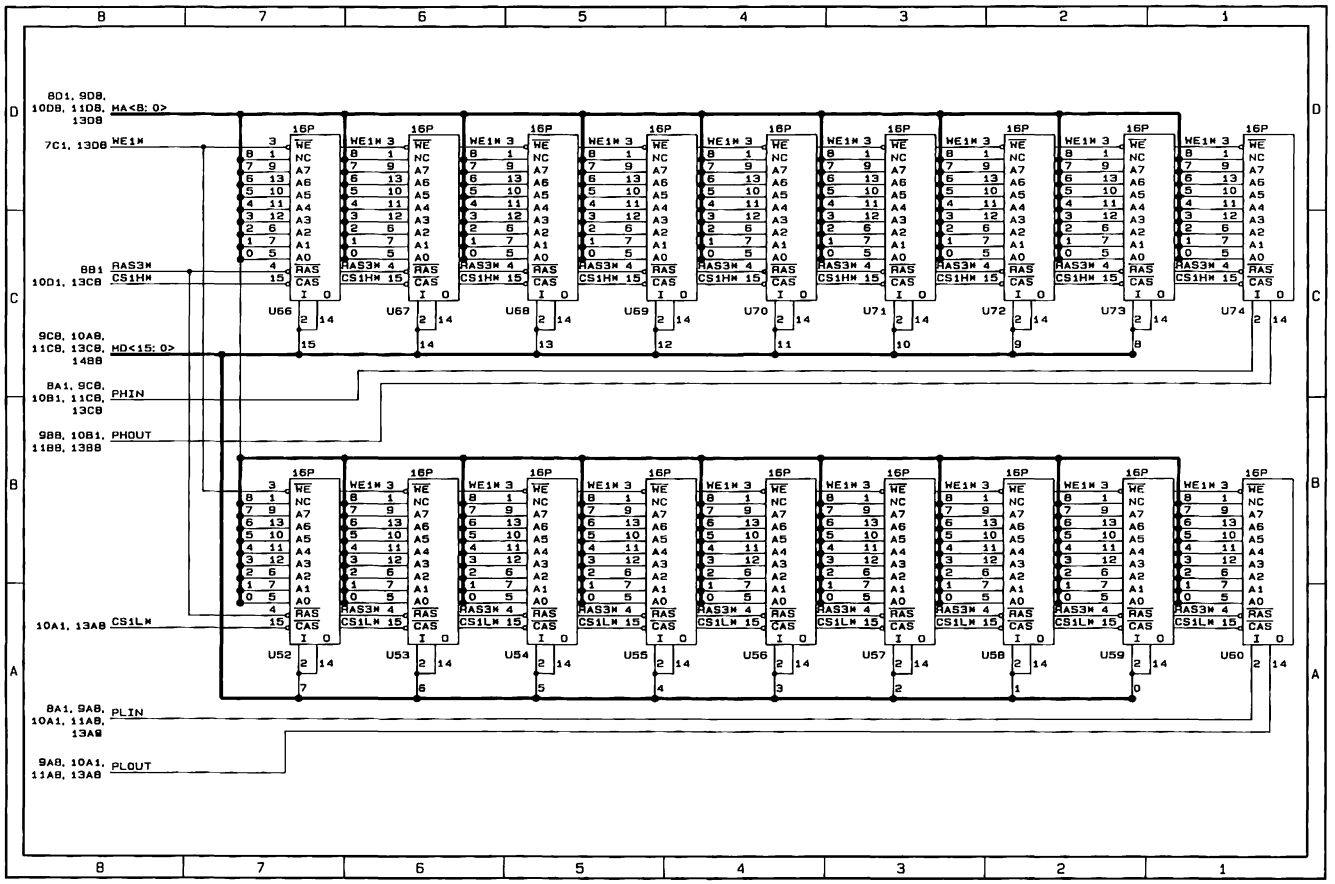


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 12 of 18)

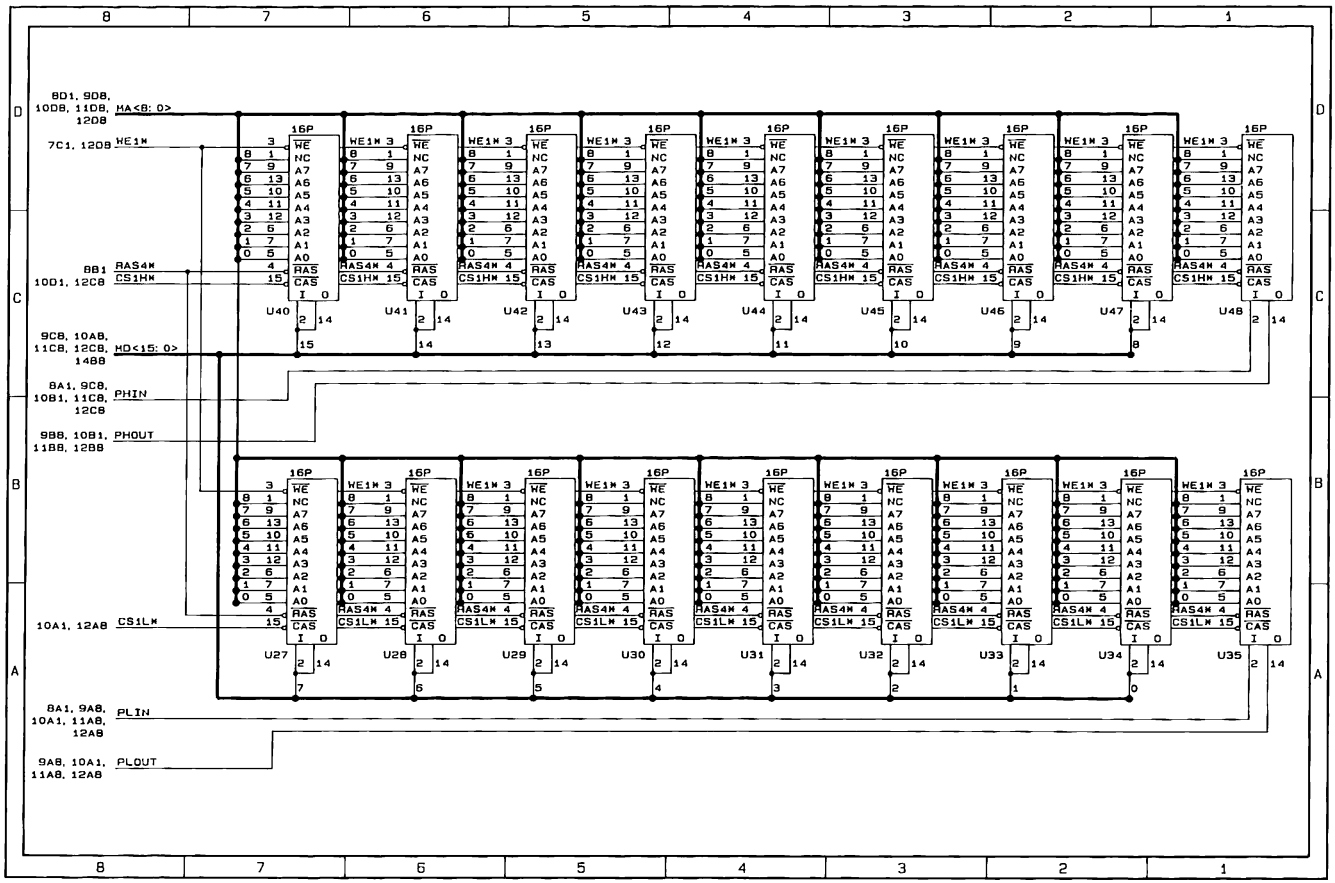


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 13 of 18)

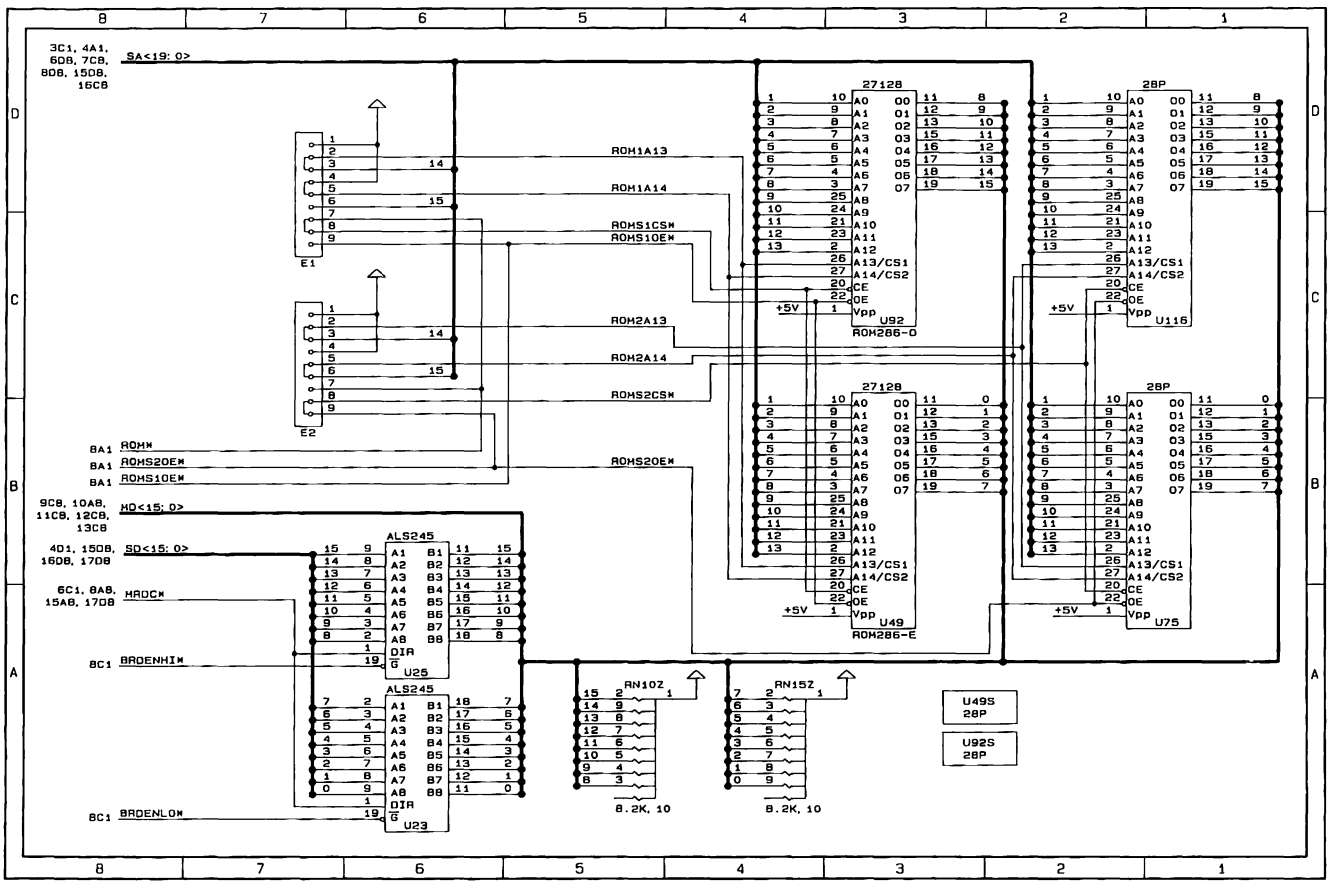


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 14 of 18)

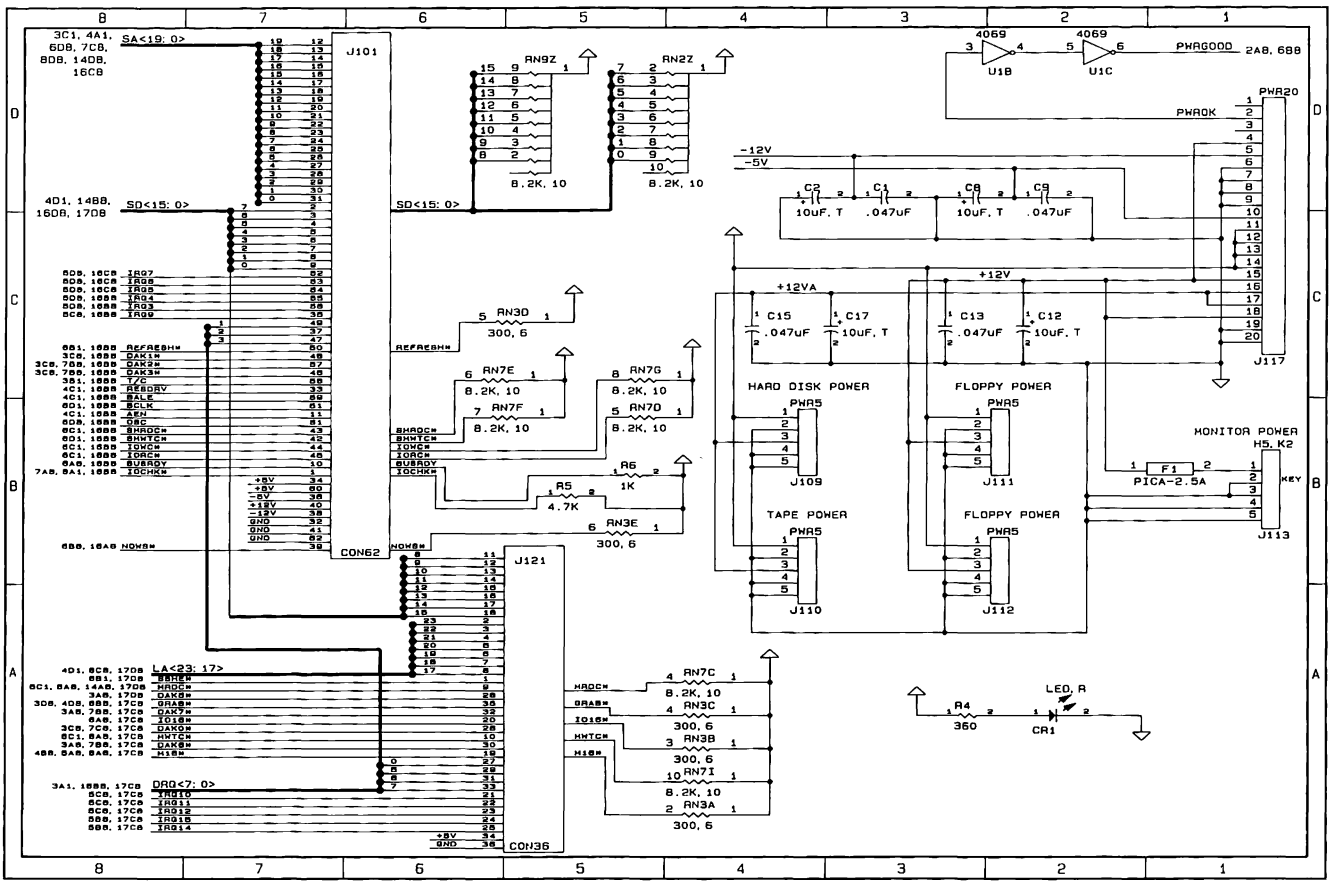


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 15 of 18)

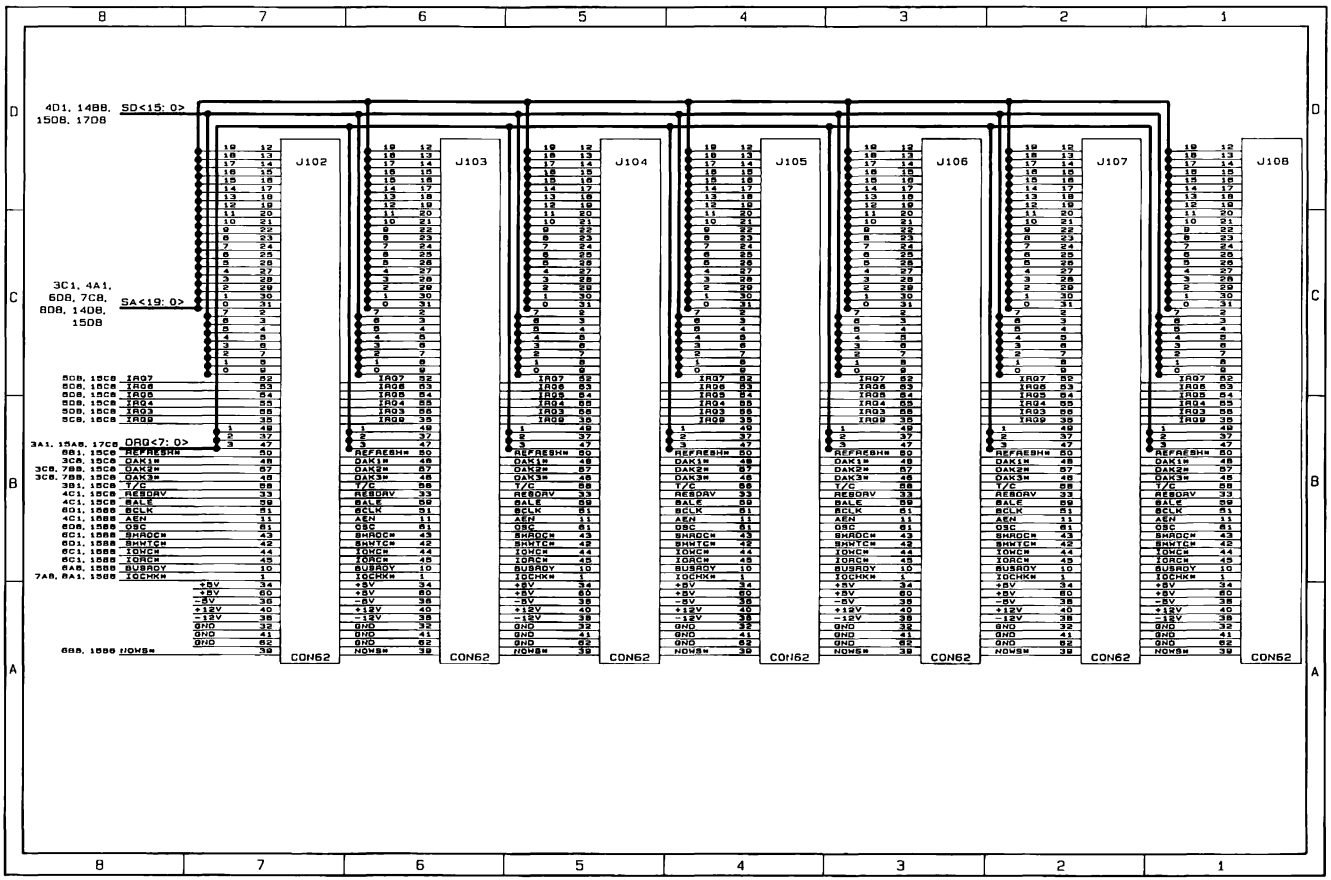


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 16 of 18)

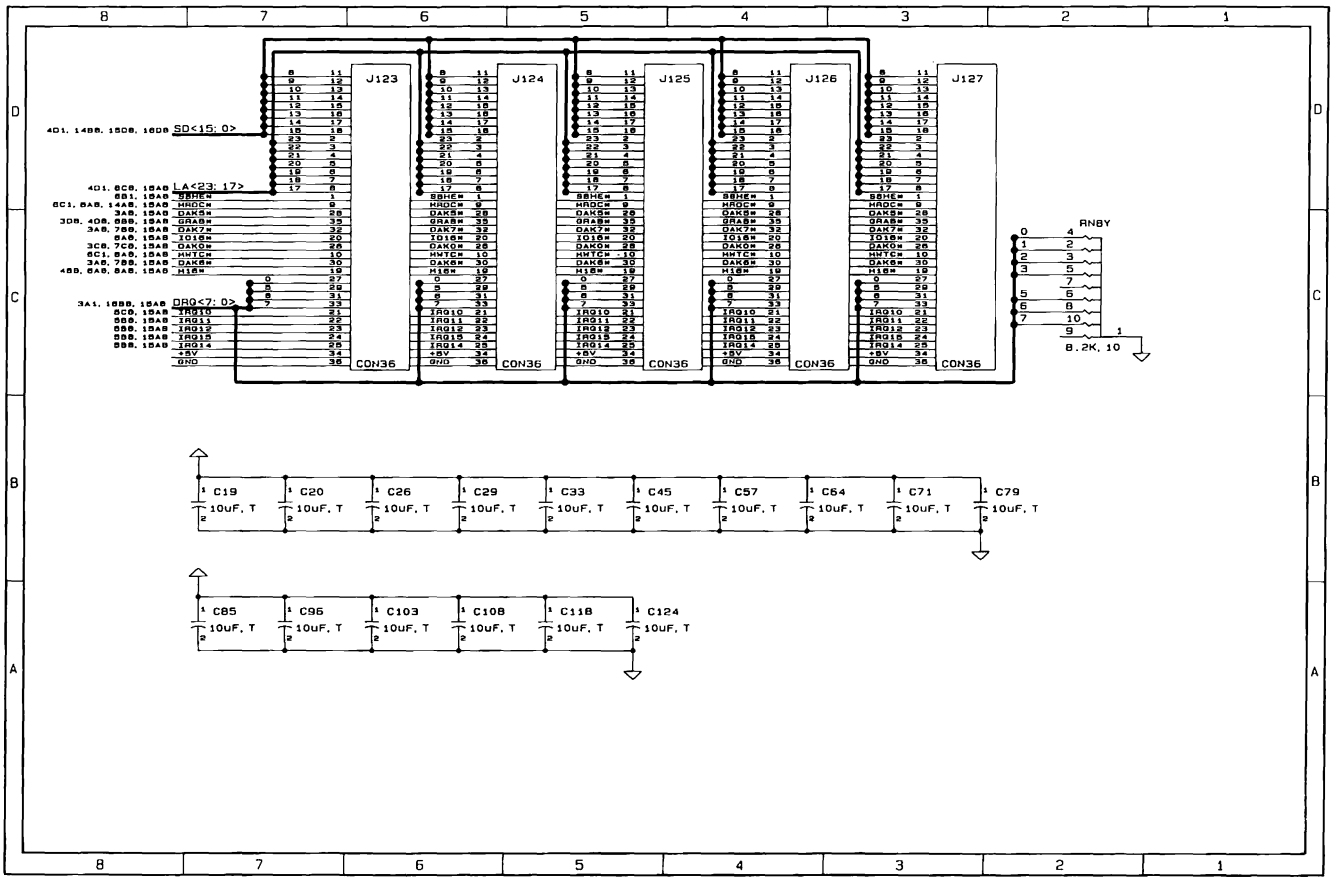


Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 17 of 18)

Figure 2-45. COMPAQ DESKPRO 286 Version 2 System Board Schematics (Page 18 of 18)

Chapter 2, Part 2

SYSTEM BOARD (12 MHz ONLY)

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CHAPTER 2, PART 2
SYSTEM BOARD (12-MHz ONLY)

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2.14 PROGRAMMABLE DEVICES (Continued)

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2.14 PROGRAMMABLE DEVICES (Continued)

TABLE OF CONTENTS (Continued)

2.11 THE 12-MHz COMPAQ DESKPRO 286 PERSONAL COMPUTER

This chapter describes the theory of operation for the COMPAQ DESKPRO 286 Personal Computers with a 12-MHz 80286 Central Processing Unit (CPU).

Included in the description are:

- CPU and CPU support circuitry, which control and monitor the system.
- Memory system, which controls access to and from the system random-access memory (RAM) and access from the system read-only memory (ROM).
- Programmable devices are hardware devices that are on the system board and that can be controlled or monitored by software.
- The expansion bus and bus functions allow system access to hardware options that may be installed in the system. Hardware options may include display controllers, communications devices, and additional memory.

Information also included in this chapter:

- Miscellaneous system board information, such as fuses and indicators
- Jumpers
- Connectors
- Schematics

Figure 2-46 is a functional block diagram of the system board.

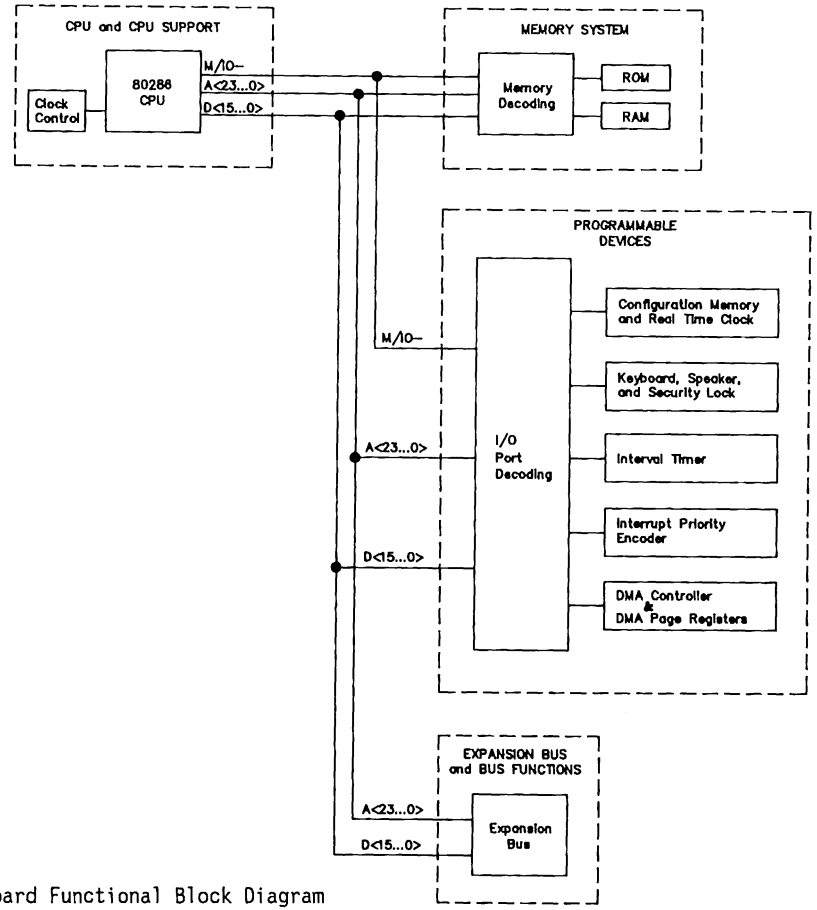


Figure 2-46. System Board Functional Block Diagram

2.12 CPU AND CPU SUPPORT

The 80286 microprocessor uses three buses, the 24-bit address bus, the 16-bit data bus, and the control bus to communicate with and control the system.

All devices outside the 80286 microprocessor are addressed as either memory-mapped devices or I/O-mapped devices.

To reset the 80286, apply power to the system board or simultaneously press the CTRL+ ALT+ DEL keys. Once the CPU is reset, it addresses the ROM for instructions. The initial boot instructions in ROM check the system RAM and ROM for errors (checksums), then initialize the system.

System initialization, or restart of the system, includes loading the desired starting values into the programmable devices, such as the keyboard controller, the video controller, the RAM, and the CPU.

After system initialization, the CPU loads the disk operating system (DOS) into memory from the diskette or fixed disk drive. The DOS is a program that manages and provides a consistent programming interface to the hardware.

Included in this category are the:

- Clock generator and READY interface
- System control circuitry
- 80287 numeric coprocessor
- Clock function

Figure 2-47 shows a functional block diagram of the CPU and CPU support circuitry.

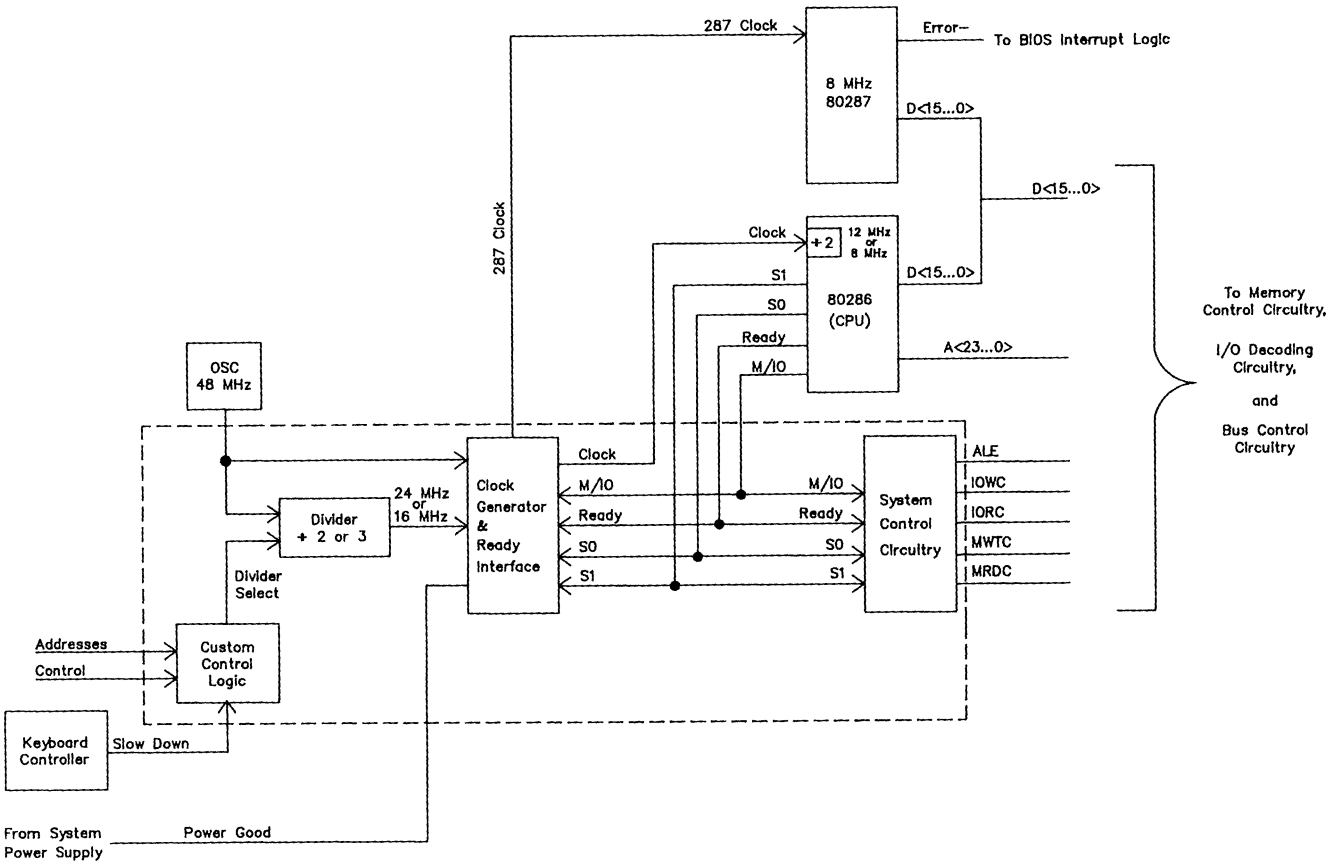


Figure 2-47. CPU and CPU Support Circuitry Block Diagram

Clock Generator and Ready Interface

The clock generator and READY interface receives an input clock signals from an oscillator circuit and generates the clock signal for the 80286 CPU, the 80287 coprocessor, and the system control circuitry. The clock generator and READY interface also monitors the power good (PWRGOOD) signal from the system power supply to control the system reset functions.

System Control Circuitry

The system control circuitry decodes the status signals S0, S1, and M/IO-, and other inputs, such as CEN/AEN, and READY-, to control the system bus.

Table 2-30 shows the bus cycle status definition for the status signals.

Table 2-30. Bus Cycle Status Definition

M/IO-	S0	S1+	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read (Ports)
0	1	0	I/O Write (Ports)
0	1	1	None: Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

80287 Numeric Coprocessor (Optional)

The 80287 Numeric Coprocessor is a high-performance numeric processor extension of the 80286, adding floating-point, extended integer, and BCD data-type support.

The 80287 automatically executes all numeric instructions as they are received. The 80287 responds to particular I/O addresses (00F8h, 00FAh, and 00FCh) automatically generated by the 80286.

The 80287's ERROR- signal is connected to IRQ13 (INT 75h). The BIOS interrupt handler for INT 75h routes this interrupt to INT 02h, which is the actual routine for coprocessor exceptions. This method provides compatibility with 8088/8086-coprocessor exceptions and prevents interference with the video I/O interrupt, INT 10h.

A socket on the system board holds the 80287 coprocessor. The 80287 coprocessor operates at 8 MHz.

Clock Function

The COMPAQ DESKPRO 286 Personal Computer with a 12 MHz 80286 offers the choice of a 12-MHz/8-MHz switching system clock for improved processing speed or a fixed 8-MHz system clock to maintain compatibility with slower systems.

2.13 MEMORY SYSTEM

Memory Address Decoding

The 80286 uses addresses <A23..A0> and control line M/IO- to specify memory locations. The address and control lines are decoded to specify memory areas for the system RAM and ROM

The memory system includes:

- Memory address decoding
- Memory support
- Memory system (RAM & ROM)

Expansion boards such as memory, disk, or video must have their own devices to decode the I/O or memory space for that board.

Figure 2-48 shows a simplified block diagram of memory address decoding for the system board.

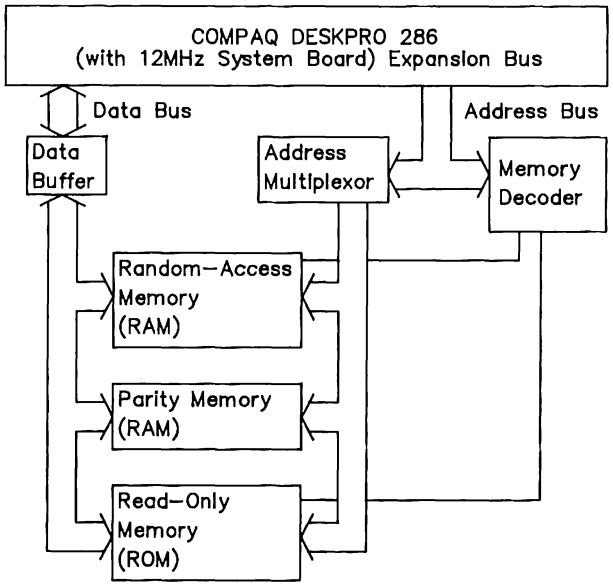


Figure 2-48. Memory Address Decoding Simplified Block Diagram

The memory decoder uses the REFRESH-, MRDC-, MWTC-, BALE, and address lines LA23 through LA17 to generate the MEM16-, RAM-, ROM-, RAS-, and CAS- signals.

The 16-bit 80286 microprocessor can read data from memory as bytes (8 bits) or words (16 bits). When it reads a word on an an even boundary, an even-numbered address is generated, and the CPU simultaneously reads that address and the one above it (Figure 2-49).

Odd-numbered, High-order Byte	Even-numbered, Low-order Byte
Byte FFFFh (64K)	Byte FFFEh (64K-1)
.	.
.	.
.	.
Byte 0003h	Byte 0002h
Byte 0001h	Byte 0000h

Figure 2-49. A 16-Bit Word Divided into Two Bytes

Two CPU cycles are required to read a word on an odd boundary. The next lower even-numbered address is given first by the CPU, and the high-order byte of that location becomes the low-order 8 bits of the word. The next higher even-numbered address is then given by the CPU, and the low-order byte of that location becomes the high-order 8 bits of the word.

Memory Support

Dynamic memory devices (RAM) require support circuitry to:

- Control the devices, using the CAS-, RAS-, and WR- signals
- Multiplex the address lines into the RAM
- Buffer the data lines
- Refresh the memory cells

The delay line generates the ENDRAS and STARTCAS signals and the signals that control the address multiplexing.

Three AM2966 devices buffer the address lines and sequentially present the high- and low-order address lines to the RAM. The delay line controls the timing for this multiplexing operation.

Two 74F245 chips buffer the data between the RAM and the data bus.

Memory refresh is controlled by the CBC and MSC gate arrays. During memory refresh, every cell of every memory location is recharged.

Memory System

The 12-MHz COMPAQ DESKPRO 286 has five banks for RAM, two 16K x 8-bit system ROMS, and two sockets for additional ROM.

Random Access Memory (RAM)

The 12-MHz COMPAQ DESKPRO 286 has 128 Kbytes of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAMS may be used. Memory must be expanded in full-bank increments (18 RAM devices) in contiguous and ascending order, using the same RAM type (64K or 256K).

SW1 position 1 indicates the type of RAM in banks 1 through 4. When banks 1 through 4 are filled with 64K x 1-bit RAMs, SW1 position 1 must be CLOSED. When banks 1 through 4 are filled with 256K x 1-bit RAMS, SW1 position 1 must be OPEN.

NOTE: When SW1 position 1 is closed, positions 4 and 5 must both be open.

SW1 positions 2 and 3 limit the amount of base memory on the system board so that conflicts with expansion memory boards can be avoided. These two switches limit memory, as shown in Table 2-31, regardless of the type of RAM in banks 1 through 4.

Table 2-31. Base Memory Size Switch (SW1) Settings

SW1		Total	Address
Position 2	Position 3	Base Memory (Note)	Ranges
CLOSED	CLOSED	Disabled RAM and ROM on System Board	
CLOSED	OPEN	256k	0-256 KB
OPEN	CLOSED	512k	0-512 KB
OPEN	OPEN	640k	0-640 KB

Legend: Closed = ON
Open = OFF

Note: Total base memory indicates maximum addressable base memory on the system board regardless of amount of RAM installed.

SW1 positions 4 and 5 enable/disable banks 2 through 4. These switches should be used to limit the amount of expansion memory on the system board when 256K x 1-bit RAMS are used to fill banks 1 through 4. Table 2-32 gives the switch settings for expansion memory.

Table 2-32. Expansion Memory Size Switch (SW1) Settings

SWI		Banks	Total Expansion Memory	Address
Position 4	Position 5	Enabled	(Note 1)	Range
CLOSED	CLOSED	None	None	-
CLOSED	OPEN	2	512K	1.0-1.5 MB
OPEN	CLOSED	2,3	1024K	1.0-2.0 MB
OPEN	OPEN	2,3,4	1536K	1.0-2.5 MB

Legend: CLOSED = ON
OPEN = OFF

Notes: 1. Total expansion memory indicates maximum addressable expansion memory on the system board regardless of amount of RAM installed.

2. SW1 positions 4 and 5 should both be OPEN when 64K x 1-bit RAMS fill banks 1 through 4 to ensure that SW1 positions 2 and 3 operate correctly.

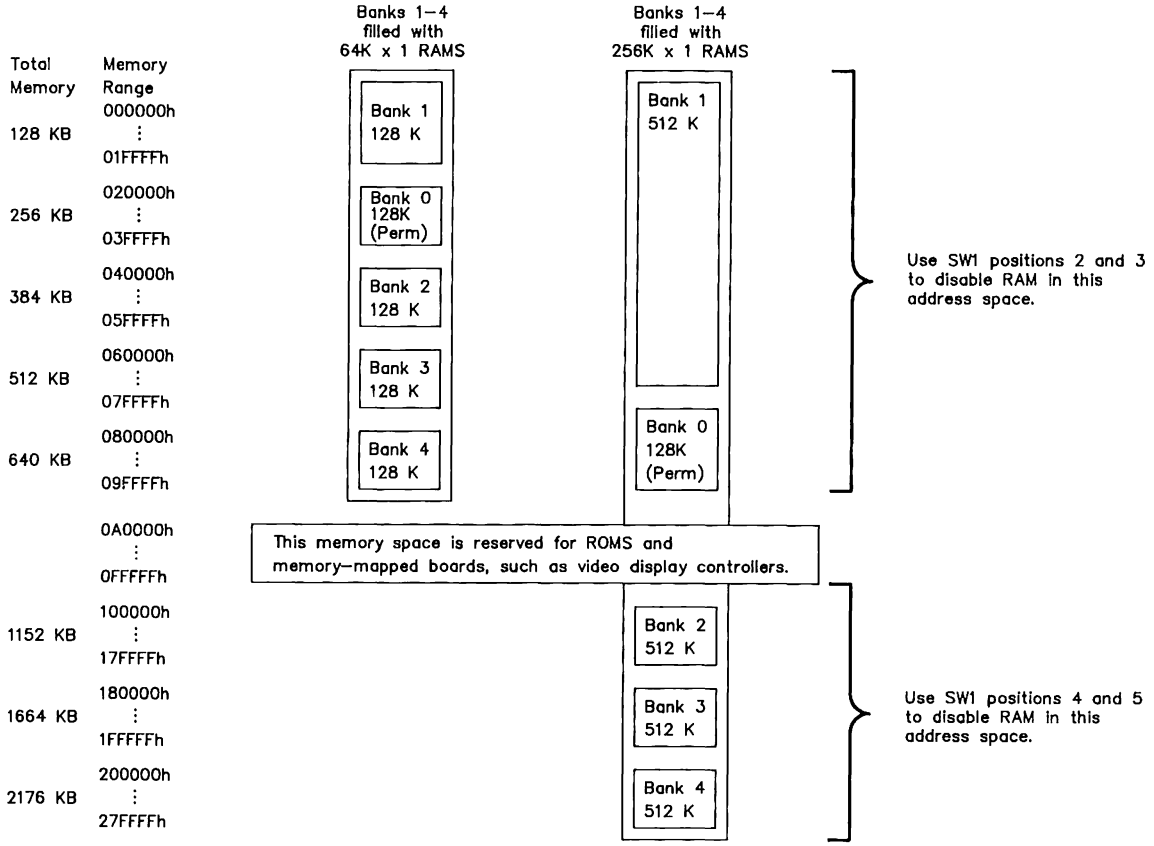


Figure 2-50. System Board Memory Configurations

The system board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit dynamic RAM devices with a response time of 100 ns or faster. (CAS access time must be 50 ns or faster.)

Read Only Memory (ROM)

The system board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 KB below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (basic input output system). Installed in the two ROM Set 1 sockets are 16K x 8-bit devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and permit future expansion.

ROMs can be, by pairs, either 8K, 16K, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64-Kbyte space at address 0F0000h through 0FFFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64-Kbyte space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K x 8-bit ROMs are used, the pair of ROMs fill the entire 64-Kbyte address space. When 16K x 8-bit ROMs are used, the most-significant address bit is not decoded, so the ROMs are double-mapped into two identical 32-Kbyte sections of the 64-Kbyte address space.

Similarly, when 8K x 8-bit ROMs are used, the two most-significant address bits are not decoded, so the ROMs are quadruple-mapped into four identical 16-Kbyte sections of the 64 KB address space.

Jumpers

Two jumpers (E1 and E2) are provided to enable use of a variety of types of ROM for special applications.

Table 2-33 gives the jumper settings and resulting configuration for each type of ROM.

Table 2-33. Jumper Settings for ROM Sets 1 and 2

ROM Set 1 = E1
ROM Set 2 = E2

Jumper Settings			ROM Type
1-2	4-5	7-8	8K x 8, Static ROM, 150 ns
2-3	4-5	7-8	16K x 8, Static ROM, 150 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32K x 8, Static ROM, 150 ns
1-2	4-5	8-9	8K x 8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16K x 8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32K x 8, Dynamic ROM, 150 ns

No jumper headers are installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

ROM Set 1:16K x 8-bit Static ROM (E1: 2-3, 4-5, 7-8)

ROM Set 2:32K x 8-bit Dynamic ROM (E2: 2-3, 5-6, 8-9)

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering wire(s) to jumpers as desired.

2.14 PROGRAMMABLE DEVICES

The system BIOS controls the following system board programmable devices:

- Direct memory access (DMA) controllers
- DMA memory page register
- Real-time clock and configuration memory
- Keyboard controller
- Interval timer
- Interrupt priority encoder

These devices are all I/O mapped. Commands and opcodes are directed to the appropriate device by the I/O port decoding circuitry. Table 2-34 summarizes the port addresses used by the devices on the system board.

Table 2-34. System Board I/O Map

	Address Bits										
Port	9	8	7	6	5	4	3	2	1	0	Device
00h..0Fh	0	0	0	0	0	X	Y	Y	Y	Y	8237A-5 Byte DMA Controller
20h..21h	0	0	0	0	1	X	X	X	X	Y	8259A Interrupt Controller 1
40h	0	0	0	1	0	X	X	X	0	0	8254-2 System Clock (Timer 0)
41h	0	0	0	1	0	X	X	X	0	1	8254-2 Refresh Request (Timer 1)
42h	0	0	0	1	0	X	X	X	1	0	8254-2 Speaker Tone (Timer 2)
43h	0	0	0	1	0	X	X	X	1	1	8254-2 Command Mode Register
60h	0	0	0	1	1	0	X	0	X	0	8042 Date I/O Register
61h	0	0	0	1	1	0	X	X	X	1	Port B/C Input/Outputs
64h	0	0	0	1	1	0	X	1	X	0	8042 Status/Command Register
70h	0	0	0	1	1	1	X	X	X	0	RTC Address Register (Bits <5..0>)
70h	0	0	0	1	1	1	X	X	X	0	NMI Enable Register (Bit <7>)
71h	0	0	0	1	1	1	X	X	X	1	RTC Data I/O Register
80h	0	0	1	0	0	X	0	0	0	0	DMA Page Register Spare
81h	0	0	1	0	0	X	0	0	0	1	DMA Page Register CH 2 Page
82h	0	0	1	0	0	X	0	0	1	0	DMA Page Register CH 3 Page
83h	0	0	1	0	0	X	0	0	1	1	DMA Page Register CH 1 Page
84h	0	0	1	0	0	X	0	1	0	0	DMA Page Register Spare
85h	0	0	1	0	0	X	0	1	0	1	DMA Page Register Spare
86h	0	0	1	0	0	X	0	1	1	0	DMA Page Register Spare
87h	0	0	1	0	0	X	0	1	1	1	DMA Page Register CH 0 Page
88h	0	0	1	0	0	X	1	0	0	0	DMA Page Register Spare

(Continued)

Table 2-34. (Continued)

Port	Address Bits 9 8	7 6 5 4	3 2 1 0	Device
89h	0 0	1 0 0 X	1 0 0 1	DMA Page Register CH 6 Page
8Ah	0 0	1 0 0 X	1 0 1 0	DMA Page Register CH 7 Page
8Bh	0 0	1 0 0 X	1 0 1 1	DMA Page Register CH 5 Page
8Ch	0 0	1 0 0 X	1 1 0 0	DMA Page Register Spare
8Dh	0 0	1 0 0 X	1 1 0 1	DMA Page Register Spare
8Eh	0 0	1 0 0 X	1 1 1 0	DMA Page Register Spare
8Fh	0 0	1 0 0 X	1 1 1 1	DMA Page Register Refresh Page
A0h..A1h	0 0	1 0 1 X	X X X Y	8259A Interrupt Controller 2
C0h..CFh	0 0	1 1 0 Y	Y Y Y X	8237A-5 Word DMA Controller
F0h	0 0	1 1 1 X	0 X X 0	Clear Numeric Processor Busy
F1h	0 0	1 1 1 x	0 X X 1	Reset Numeric Processor
F8h..FFh	0 0	1 1 1 1	1 Y Y X	80287 Command Ports

Legend: X = Don't care. The value of these bits does not affect the I/O address decoding.
Y = Register dependent.

I/O Port Decoding

The 80286 uses address (A<15...0>) and control lines (M/IO-) to specify I/O operations. Although the 80286 uses 16 bits for an I/O address, the system board and expansion boards use only 10 bits; (A<9...0>), therefore I/O space is limited to 3FFh. The address and control lines are decoded to provide chip selects and addresses for the system board I/O-mapped devices (DMA controllers, real-time clock, and interval timer).

Each expansion board such as memory, disk, and video, must have its own device to decode the I/O-mapped devices for that board. Figure 2-51 shows a simplified block diagram of I/O port decoding for the system board.

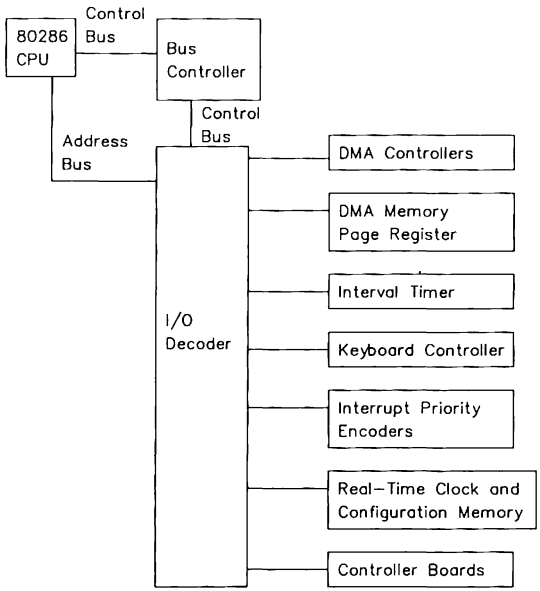


Figure 2-51. I/O Address Decoding Simplified Block Diagram

Direct Memory Access Controllers

Direct memory access (DMA) is a method of directly accessing memory without involving the CPU. DMA is normally used to transfer blocks of data to or from an I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

The system board uses two Intel 8237 DMA controllers; each with four bidirectional data channels. The DMA controllers operate at 4 MHz. DMA Controller 1 is used for byte (8-bit) data transfers. DMA Controller 2 is used for word (16-bit) data transfers. Unlike the CPU, DMA Controller 2 can only transfer words on an even boundary. Table 2-35 lists the function assigned to each DMA channel.

Table 2-35. DMA Channels Assigned to the Controllers

Channel	Function
Controller 1 (Byte Transfers)	
0	Spare
1	SDLC (Communications)
2	Diskette Data Transfers
3	Spare
Controller 2 (Word Transfers)	
4	Cascade for Controller 1
5	Spare
6	Spare
7	Spare

The DMA controllers hold (or define) only 16 bits of the 24-bit address. The other 8 address bits are generated by the MAP gate array. See the "DMA Memory Page Register" section for more information. Figure 2-52 shows memory address derived from page register and DMA register contents.

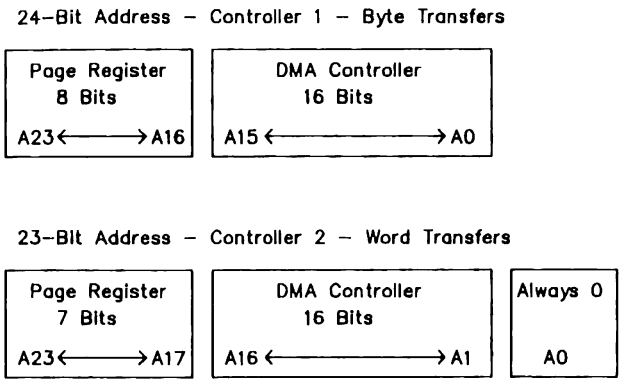


Figure 2-52. Memory Address Derived from Page Register and DMA Register Contents

A16 from the DMA memory page register is disabled when DMA Controller 2 is selected. A0 is not connected to DMA Controller 2. A0 is always 0 when word-length transfers are selected. This arrangement means that the size of the block of data that can be moved or addressed is measured in 16-bit words rather than in 8-bit bytes.

Since the DMA controllers only contain 16 bits of the 24-bit address, they can move blocks of data only within their ability to address that data.
DMA Controller 1 can move up to 64 Kbytes of data.
DMA Controller 2 can move up to 64K words, or 128 Kbytes of data.

The DMA controllers are complex devices with several registers for commands and status. Table 2-36 lists the I/O map and the commands and formats of the registers.

Transferring Data from I/O Devices to Memory

DMA controllers and I/O devices use the DRQx and DAKx signals as "handshaking". When an I/O device has a byte or word of data to send, the I/O device makes its DRQx line active. When the DAKx line from the DMA controller becomes active, the device puts its data on the data bus.

Transferring Data from Memory to Memory

The hardware does not support memory-to-memory block transfers.

NOTE: After power-on, it is recommended that all Command, Mode, and Mask registers be loaded with valid values to ensure proper operation of the device.

Table 2-36. DMA Controller Registers

Register Function	Bits	Port Addresses Cntlr 1	Cntlr 2	Read/Write
Status	8	08h	D0h	Read
Command	8	08h	D0h	Write
Mode	6	0Bh	D6h	Write
Write Single Mask Bit	4	0Ah	D4h	Write
Write All Mask Bits	4	0Fh	DEh	Write
Software DRQx Request	4	09h	D2h	Write
Base and Current Address - CH 0	16	00h	C0h	Write
Current Address - CH 0	16	00h	C0h	Read
Base and Current Word Count - CH 0	16	01h	C2h	Write
Current Word Count - CH 0	16	01h	C2h	Read
Base and Current Address - CH 1	16	02h	C4h	Write
Current Address - CH 1	16	02h	C4h	Read
Base and Current Word Count - CH 1	16	03h	C6h	Write
Current Word Count - CH 1	16	03h	C6h	Read
Base and Current Address - CH 2	16	04h	C8h	Write
Current Address - CH 2	16	04h	C8h	Read
Base and Current Word Count - CH 2	16	05h	CAh	Write
Current Word Count - CH 2	16	05h	CAh	Read
Base and Current Address - CH 3	16	06h	CCh	Write
Current Address - CH 3	16	06h	CCh	Read
Base and Current Word Count - CH 3	16	07h	CEh	Write

(Continued)

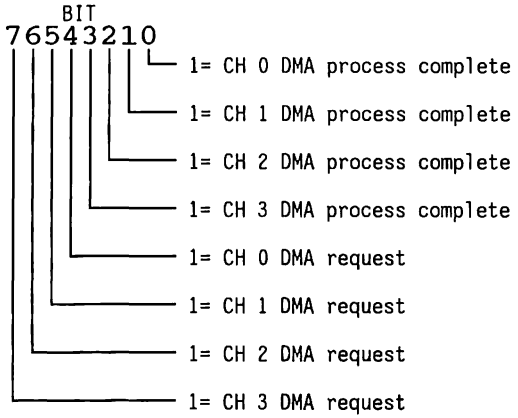
Table 2-36. (Continued)

Register Function	Bits	Port Addresses Cntrl 1	Cntrl 2	Read/Write
Current Word Count - CH 3	16	07h	CEh	Read
Temporary	16	0Dh	DAh	Read
Reset Pointer Flip-flop	(Notes 1,2)	0Ch	D8h	Write
Master Reset	(Note 2)	0Dh	DAh	Write
Reset Mask Register	(Note 2)	0Eh	DCh	Write

Notes: 1. See "RESET POINTER FLIP-FLOP" for an explanation of 16-bit data transfers to the DMA controllers.
2. This is not a register, but a direct command to the DMA Controller.

STATUS

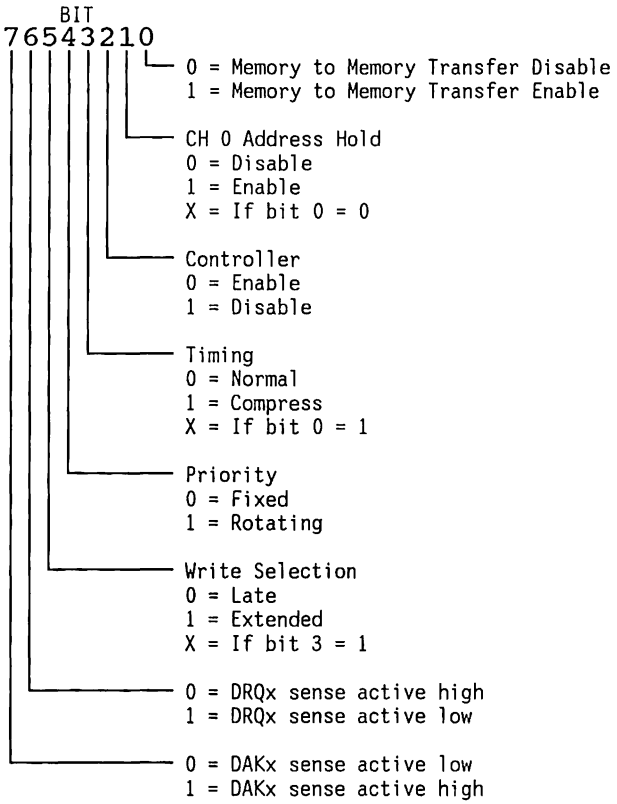
The STATUS register bits are set (= 1) to indicate that a channel has requested DMA access or that a DMA process is complete.



COMMAND

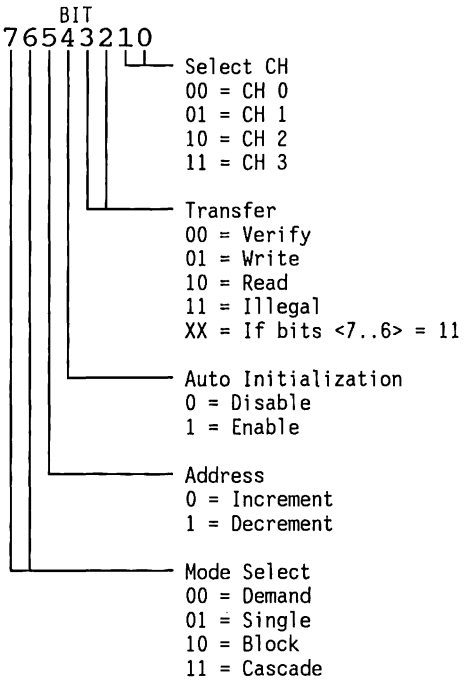
The COMMAND register bits control the DMA operation. All bits are reset (=0) by the master clear instruction or a system reset. This register must be programmed to 00 for proper system operation.

COMMAND (Continued)



MODE

Each channel has a 6-bit register associated with it. The first 2 bits of the byte written to this register specify which channel is being selected. These registers specify the operating mode for each channel.

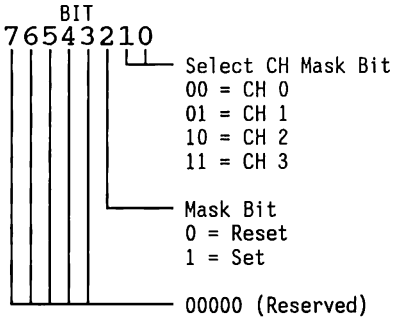


MODE (Continued)

If the Block or Demand mode is selected for a channel, the total transfer time must not exceed 15 us or RAM is not properly refreshed.

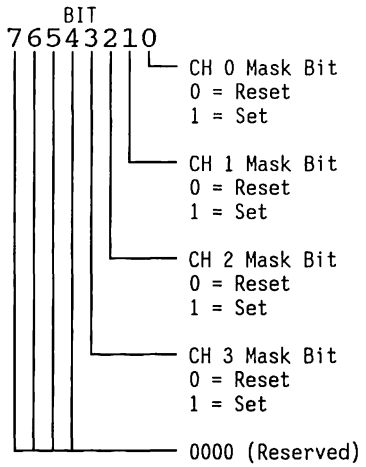
WRITE SINGLE MASK BIT

This command sets (=1) or resets (=0) a single mask bit. When a mask bit is set, that channel's DRQx is disabled. The WRITE ALL MASK BITS command can set or reset all the mask bits.



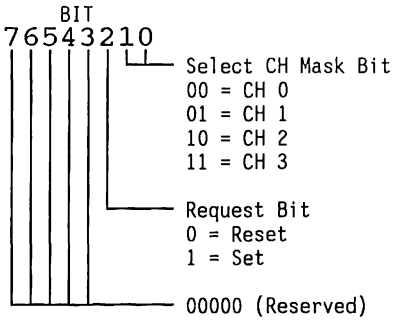
WRITE ALL MASK BITS

This command sets (=1) or resets (=0) all the Mask bits. When a bit is set, that channel's DRQx is disabled. The WRITE SINGLE MASK BIT command can set or reset a single mask bit.



SOFTWARE DRQx REQUEST

The DMA controller can respond to software requests for DMA as well as hardware requests from DRQx lines. The channel must be in the block mode, and the appropriate registers (base addresses and so forth) must be set before initiating this request.



BASE AND CURRENT ADDRESS - CHANNELS 0-3

These 16-bit write-only registers specify the starting destination address for the memory transfer. The 16-bit contents are loaded into these registers as a two-part operation. The first write to this register loads the 8 least-significant bits. The second consecutive write loads the 8 most-significant bits. See the RESET POINTER FLIP-FLOP command.

CURRENT ADDRESS - CHANNELS 0-3

These 16-bit read-only registers specify either the current address or the destination address for the next data transfer. This address is the same as the base address, plus address increments or decrements made after each data transfer. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the 8 least-significant bits. The second consecutive read returns the 8 most-significant bits. See the RESET POINTER FLIP-FLOP command.

BASE AND CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit write-only registers specify the number of words to be transferred. The 16-bit contents are loaded into these registers as a two-part operation. The first write to this register loads the 8 least-significant bits. The second consecutive write loads the 8 most-significant bits. See the RESET POINTER FLIP-FLOP command, (QF12).

CURRENT WORD COUNT - CHANNELS 0-3

These 16-bit read-only registers specify the number of words already moved as part of a data block. The 16-bit contents are read from these registers as a two-part operation. The first read from this register returns the 8 least- significant bits. The second consecutive read returns the 8 most-significant bits. See the RESET POINTER FLIP-FLOP command.

TEMPORARY

This register is not used in this hardware configuration.

RESET POINTER FLIP-FLOP

This is a direct command to the DMA controller to reset the pointer flip-flop that keeps track of 16-bit data transfers. This command resets the pointer to a known state so that the DMA controller can load the high- and low-order bytes in the proper sequence. Use this command before writing a 16-bit base address or other 16-bit command or data to the DMA controller.

MASTER RESET

This is a direct command to the DMA controller to reset the DMA controller. It has the same effect as a hardware reset; the Command, Status, Request, Temporary, and Pointer Flip-Flop registers are reset (=0), and the Mask register bits are set (=1).

RESET MASK

This is a direct command to the DMA controller to reset the Mask register, enabling all four channels to receive DRQs (data requests).

DMA Memory Page Register

The DMA Memory Page register contains the 8 most-significant bits of the 24-bit address. It works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 2-37 lists the port address assigned to each page register. For more information on the DMA controllers, see Section 2.14.

Table 2-37. Port Address For DMA Channels

DMA Channel	Page Register I/O Port Address
0	087h
1	083h
2	081h
3	082h
4	None
5	08Bh
6	089h
7	08Ah
Refresh	08Fh (See Note)

Note: The DMA Memory Page register for the refresh channel must be programmed with 00h for proper system operation.

Real-Time Clock and Configuration Memory

The COMPAQ 286 family computer system boards use the Motorola MC146818 device as their real-time clock (RTC) and configuration memory. This device has a total of 64 bytes of memory. The first 14 memory locations are used for the RTC. The remaining 50 memory locations are used for the system configuration.

A value can be written to or read from all 64 registers except:

- Status registers C and D, which are read-only
- Bit <7> of Status register A, which is read only
- The high-order bit of the seconds byte, which is read-only

Figure 2-53 shows the memory map for the MC146818.

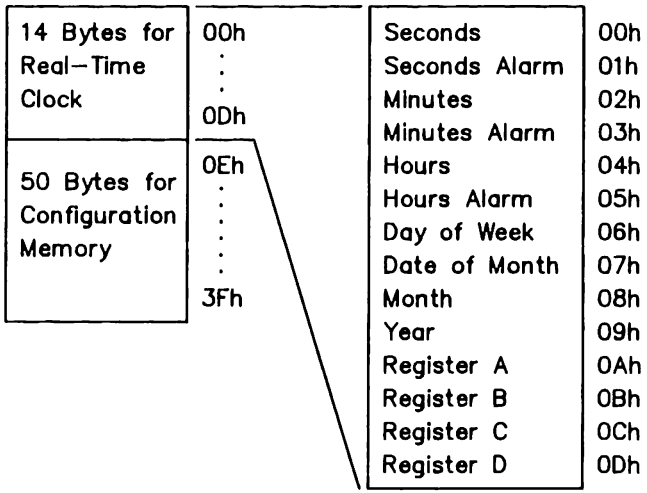


Figure 2-53. MC146818 Memory Map

To prevent a loss of time or system configuration, the MC146818 uses power obtained from a battery mounted on the inside of the computer. The battery maintains the time and system configuration during power loss for as long as three years. The system does NOT charge the battery.

NOTE: If the battery is disconnected or fails for any reason, the time and system configuration must be reprogrammed into the MC146818.

To reset the time or system configuration, run the SETUP procedure found on the USER PROGRAMS diskette or on the Advanced Diagnostics Diskette. To reset the time, use either the SETCLOCK (DOS) command, or the appropriate INT 1Ah (BIOS) command.

The MC146818 is an I/O mapped device. Use the 80286 OUT and IN instructions to read or write to the memory in this device. Note that the port 70h is shared between the NMI Mask register and the Configuration Memory Address register. To leave the NMI Mask enabled, make sure when writing a RTC address to port 70h that bit <7> is set to 0 .

To write a value into memory:

1. Use OUT 70h, AL to specify the memory location to change. 70h is the port number; AL is the memory location.
2. Use OUT 71h, AL to specify the data for the memory location. 71h is the port number; AL is the data.

To read the contents of a memory location:

1. Use OUT 70h, AL to specify the memory location to read. 70h is the port number; AL is the memory location.
2. Use IN AL, 71h to read data stored in that location. The returned data is placed in the AL register of the 80286.

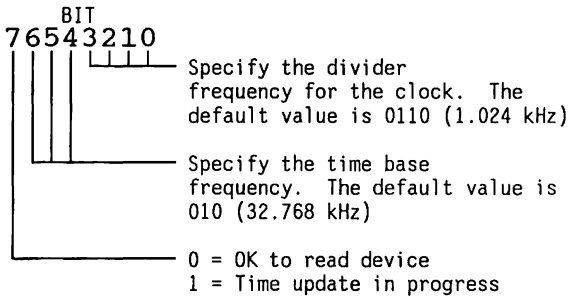
Table 2-38 summarizes the types of information stored in the MC146818's memory locations.

Table 2-38. MC146818 Real-Time Clock Memory Locations

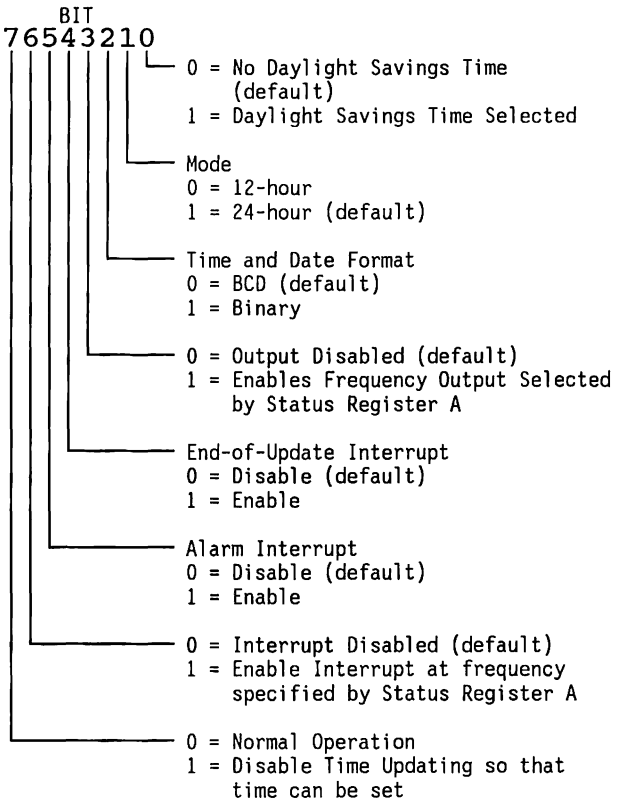
Register	Function
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hour
05h	Hour Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Status Register A
0Bh	Status Register B
0Ch	Status Register C
0Dh	Status Register D
0Eh	Diagnostic Register
0Fh	Reset Code Byte
10h	Diskette Drive Type
11h	Reserved
12h	Fixed Disk Drive Type
13h	Reserved
14h	Equipment Installed
15h,16h	System Board Memory Size
17h,18h	Extended Memory Installed
19h-2Ch	Reserved
2Dh	Additional Flags
2Eh,2Fh	Checksum Value
30h,31h	Memory More than 1 MB
32h	Century (part of time and date function)
33h	System Information
34h-3Fh	Reserved

Information about registers 0Ah through 33h follows.

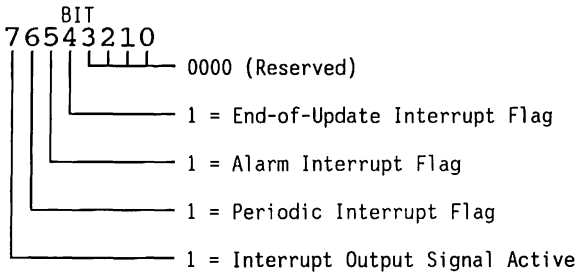
STATUS - BYTE 0Ah



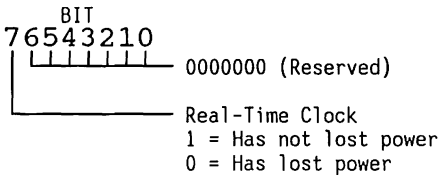
STATUS - BYTE 0Bh



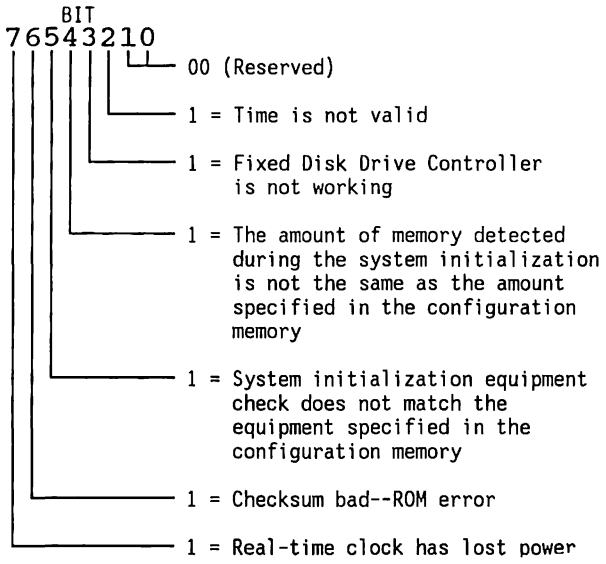
STATUS - BYTE 0Ch--READ-ONLY



STATUS - BYTE 0Dh

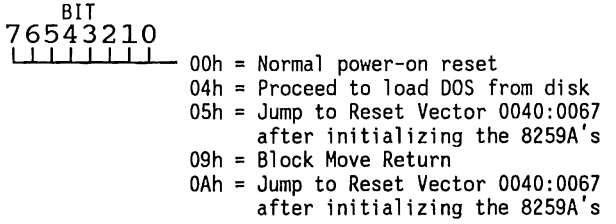


CONFIGURATION BYTE 0Eh--DIAGNOSTIC STATUS BYTE

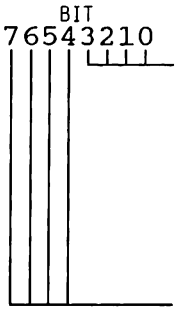


CONFIGURATION BYTE 0Fh--RESET CODE BYTE

The reset code tells the system what to do after the CPU is reset. The reset code identifies the type of, or reason for, reset. The reset code also provides a method of resetting the system without losing previously stored data or to return the system to the Real mode from the Protected Virtual Memory mode.



CONFIGURATION BYTE 10h--DISKETTE DRIVE TYPE



Secondary (drive 2) Diskette Drive Type:
0000 = No diskette drive
0001 = 360-KB Diskette Drive
0010 = 1.2-MB Diskette Drive
0011 = Reserved
0100 = 1.44-MB Diskette Drive
0101 = Reserved
:
1111 = Reserved

Primary (drive 1) Diskette Drive Type:
0000 = No diskette drive
0001 = 360-KB Diskette Drive
0010 = 1.2-MB Diskette Drive
0011 = Reserved
:
1111 = Reserved

CONFIGURATION BYTE 12h--FIXED DISK DRIVE TYPE

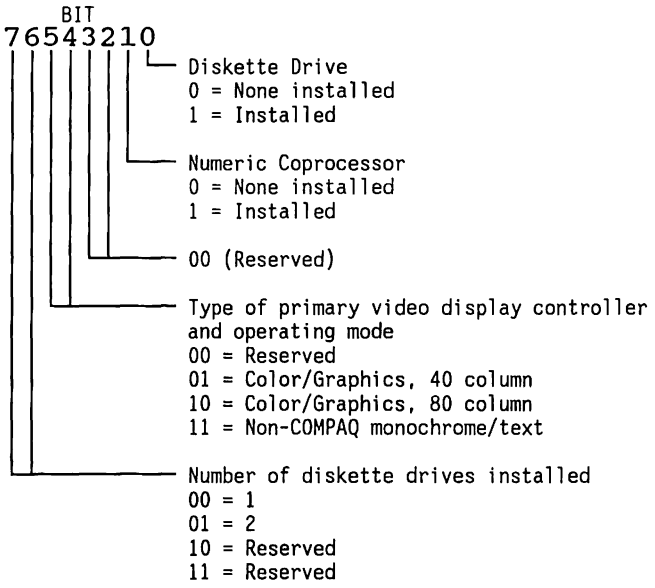
Bits	Function
<7..4>	Value defines first fixed disk drive type:

Value	Type
0000	None
0001..1110	1..14
1111	Other--see byte 19h

Bits	Function
<3..0>	Value defines second fixed disk drive type (use table above) and byte 1Ah.

NOTE: This byte identifies the type of fixed disk drive used, not the capacity.

CONFIGURATION BYTE 14h--EQUIPMENT INSTALLED



CONFIGURATION BYTES 15h AND 16h--BASE MEMORY SIZE

Value indicates valid memory sizes for the base memory size:

Byte 16h	Byte 15h	Memory Size
00h	80h	128 KB
01h	00h	256 KB
02h	00h	512 KB
02h	80h	640 KB

CONFIGURATION BYTES 17h AND 18h--EXPANSION MEMORY SIZE

Value indicates valid memory sizes for all expansion memory:

Byte 18h	Byte 17h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 19h --DRIVE C TYPE

If the disk drive is an extended drive type (type 15 or greater) bits <7..4> of byte 12h contain 1111 (binary).

The type of drive in Drive C appears in byte 19H.

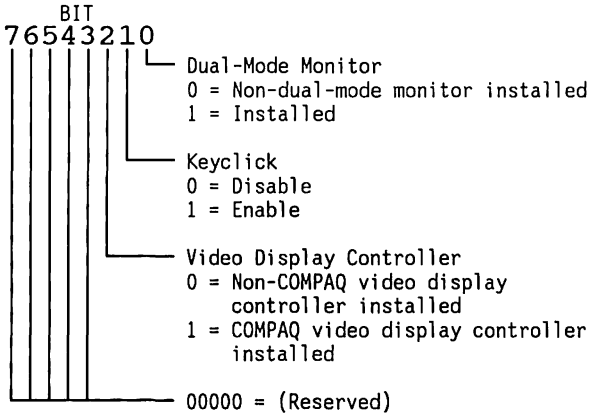
CONFIGURATION BYTE 1Ah--DRIVE D TYPE

If the disk drive is an extended drive type (type 15 or greater) bits <3..0> of byte 12h contain 1111 (binary).

The type of drive in drive D appears in byte 1Ah.

CONFIGURATION BYTE 2Dh--ADDITIONAL FLAGS

This byte allows the configuration of special features.



CONFIGURATION BYTES 2Eh AND 2Fh--MEMORY CHECKSUM

Value stored is the checksum for memory addresses 10h..2Dh.

Byte 2Eh = High byte of checksum

Byte 2Fh = Low byte of checksum

CONFIGURATION BYTES 30h AND 31h--MEMORY OVER 1 MB

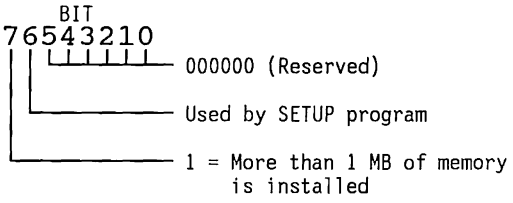
Value indicates amount of system memory in excess of 1 MB. These bytes are updated by the BIOS at power-on.

Byte 31h	Byte 30h	Memory Size
02h	00h	512 KB
04h	00h	1024 KB
06h	00h	1536 KB
08h	00h	2048 KB
0Ah	00h	2560 KB
0Ch	00h	3072 KB
0Eh	00h	3584 KB
10h	00h	4096 KB
12h	00h	4608 KB
14h	00h	5120 KB
16h	00h	5632 KB
18h	00h	6144 KB
1Ah	00h	6656 KB
1Ch	00h	7168 KB
1Eh	00h	7680 KB
.	.	.
.	.	.
3Bh	80h	15232 KB

CONFIGURATION BYTE 32h--DATE, CENTURY

This is the century part of the current time and date encoded in BCD (binary coded decimal). The BIOS sets and reads this value.

CONFIGURATION BYTE 33h--SYSTEM INFORMATION



Keyboard Controller

An INTEL 8042 single-device microcomputer provides:

- An output port for system function control and keyboard communication
- An input port to read system function status
- A test port to read the status of the keyboard clock and data lines

The 8042 has internal ROM that is custom-programmed with keyboard scan codes and operating instructions. Figure 2-54 shows a simplified block diagram of the keyboard controller.

SMAP Device

The SMAP (a Compaq designed Application Specific IC) device monitors the Intel 8042 controller for commands to "force A20 low" or "restart CPU". If either command is received, the SMAP drives the appropriate signal and prevents its use by the 8042. The SMAP does this by disabling writes to the 8042. This SMAP generated response occurs within a few us and happens much faster than if generated by the 8042. The effects of these commands being intercepted are, except for speed, invisible to the application programmer. Since these commands are often used to switch between Real and Protected modes of the CPU, performance of applications using the mode switch is increased. Programming of these commands is described below under "Programming the 8042".

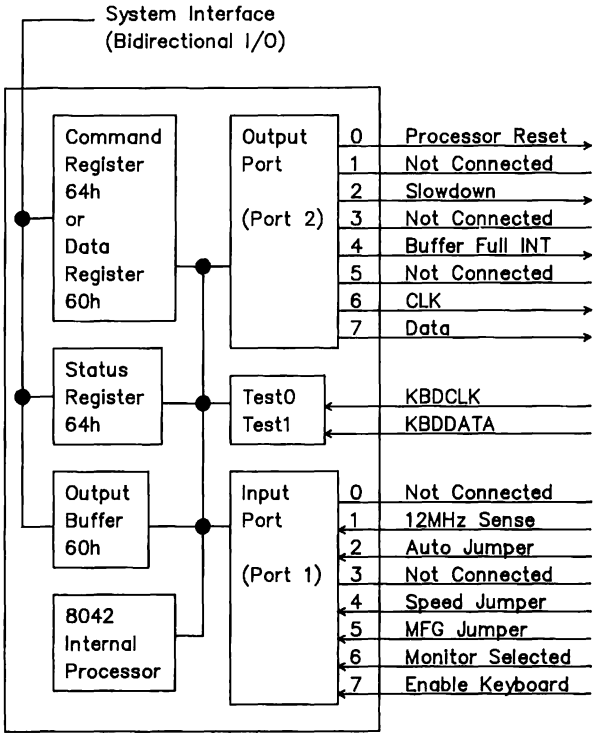


Figure 2-54. Keyboard Controller Functional Block Diagram

The 8042 communicates with the keyboard in a bidirectional, serial format with a synchronizing clock. The 8042 receives serial data, checks its parity, translates the 11- or 9-bit scan codes from the keyboard into system codes, and interrupts the 80286 to transfer data into the system.

(Command codes between the 8042 and the keyboard are described in Chapter 8.)

8042-to-Keyboard Interface

The 8042 and the keyboard are connected by a four conductor, shielded cable that carries a power line, a ground line, a Data signal, and a Clock signal.

The 8042 and the keyboard communicate in a handshaking fashion, using the Data and Clock lines for synchronous serial communication. The Data and Clock lines are driven by open-collector-type drivers at both ends of the cable in a wired-OR fashion.

The keyboard supplies the synchronizing clock for data transmissions in either direction.

Figure 2-55 shows a simplified schematic of the data and clock circuits.

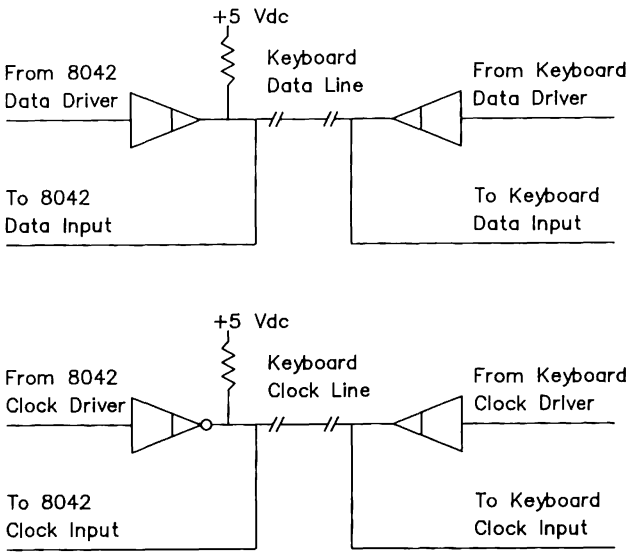
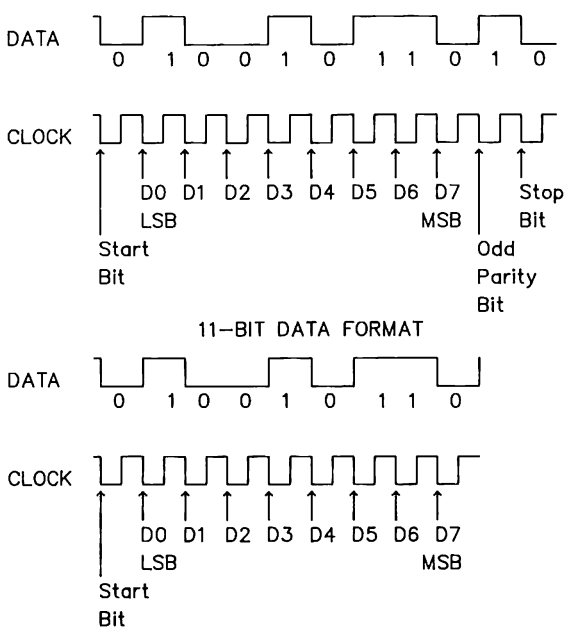


Figure 2-55. Simplified Schematic of the Data and Clock Circuits

11- or 9-Bit Data Transmission Format

The 8042 adds versatility to the system by allowing 11- or 9- bit keyboards to be used interchangeably at any time. The system sends commands to the 8042 to specify the type of scan code it expects, and the 8042 sends that type of scan code, regardless of the type of keyboard connected.

The 8042 automatically tests for keyboard type by monitoring the data format. Figure 2-56 shows 11- and 9- bit data formats with sample data transfers.



Note: The keyboard drives the data line low for the Stop Bit at the end of a transmission to acknowledge the transmission.

Figure 2-56. 11- and 9-Bit Data Formats

Table 2-39 lists the 11- and 9-bit data transfer timing parameters.

Table 2-39. Keyboard Data Timing Parameters

Parameter	11-Bit	9-Bit
Clock timing (min.), Falling edge to falling edge	60 us	25 us
Clock timing (min.), Falling edge to rising edge	5 us	5 us
Transmission Time (max.) First edge to completion	2 us	2 us
Time data must be valid before falling clock edge	0 us	0 us
Time data must be valid after falling clock edge	5 us	12 us

8042 Port Functions

The 8042 has three ports:

- An 8-bit output port for system function control and keyboard communication
- An 8-bit input port to read system function status
- A 2-bit test port to read the status of the keyboard Clock and Data lines.

To write to the output port:

1. Write command D1h (next byte is a value byte) to I/O address 64h.
2. Write the desired value for the output port to port address 60h.

To read the 8042 output port value:

1. Write command D0h (transfer the current output port values to the 8042 output buffer) to port address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-57 shows the bit values for the output port of the 8042.

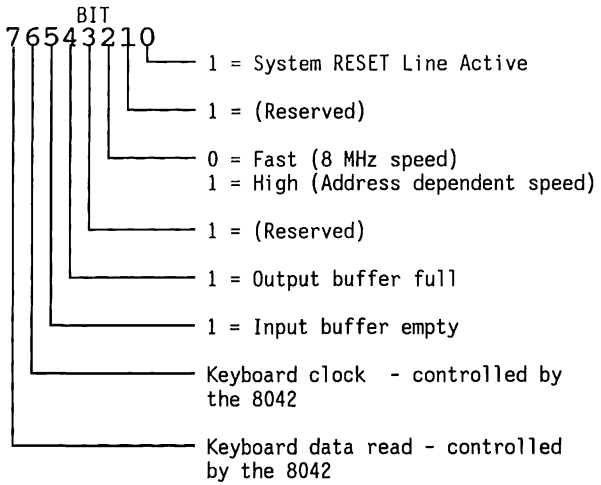


Figure 2-57. 8042 Output Port - Bit Definition

To read the 8042 input port value:

1. Write command C0h (transfer the current input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h) with the special read command A5h.

Figure 2-58 shows the format of the byte returned from the 8042 input port.

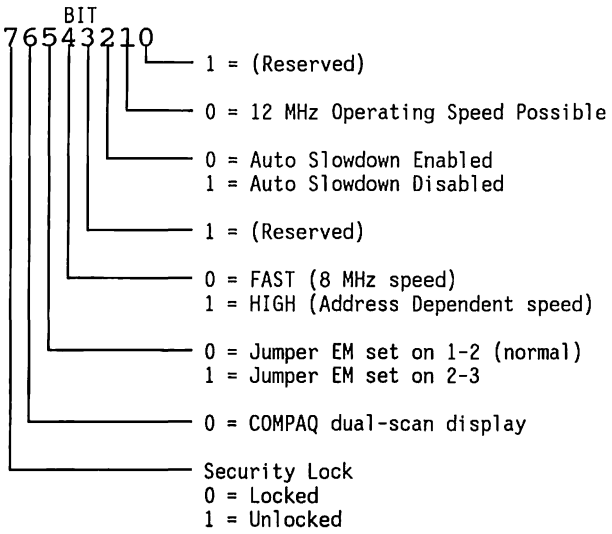


Figure 2-58. 8042 Input Port - Bit Definition

To read the 8042 TEST input port value:

1. Write the command E0h (transfer the current TEST input port values to the 8042 output buffer) to I/O address 64h.
2. Read the 8042 output buffer (port address 60h).

Figure 2-59 shows the format of the byte returned by the 8042 TEST input port.

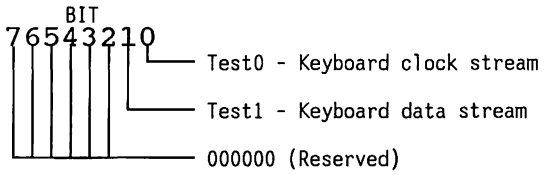


Figure 2-59. 8042 Test Input Port - Bit Definition

Programming the 8042

The 8042 is I/O-mapped at port addresses 60h and 64h.

Prior to writing a command or data to ports 60h or 64h, the 8042 STATUS register must indicate "Input Buffer Empty". Also, prior to reading data from port 60h, test the 8042 STATUS register to ensure a "Data in Buffer" condition.

Port 60h, Data I/O Register. Use the 80286's IN instruction to read data from the 8042's output buffer. Data in the DATA I/O register is from the keyboard, unless the 8042 has been given a command such as 20h, READ COMMAND byte.

Use the 80286's OUT instruction to send data to the keyboard, unless the 8042 has been given a multibyte command such as 60h, Write Command Byte. To give a multibyte command to the keyboard, write the first command byte to port 64h and the second command byte to 60h.

Port 64h, COMMAND/STATUS register. The following pages describe the format for COMMAND/STATUS register (port 64h) I/O interactions with the 8042.

Use the 80286's IN instruction to read the status of the 8042 and the keyboard (input from port 64h). Use the 80286's OUT instruction to give a command to the 8042 (output to port 64h). Writing to this address automatically sets the COMMAND/DATA flag to 1.

Most commands involve a single write step. However, some commands do require a second step, such as a subsequent 8042 register read or write.

Figure 2-60 shows the 8042 Status register. Figure 2-61 shows the 8042 command byte. Table 2-40 lists the 8042 command codes.

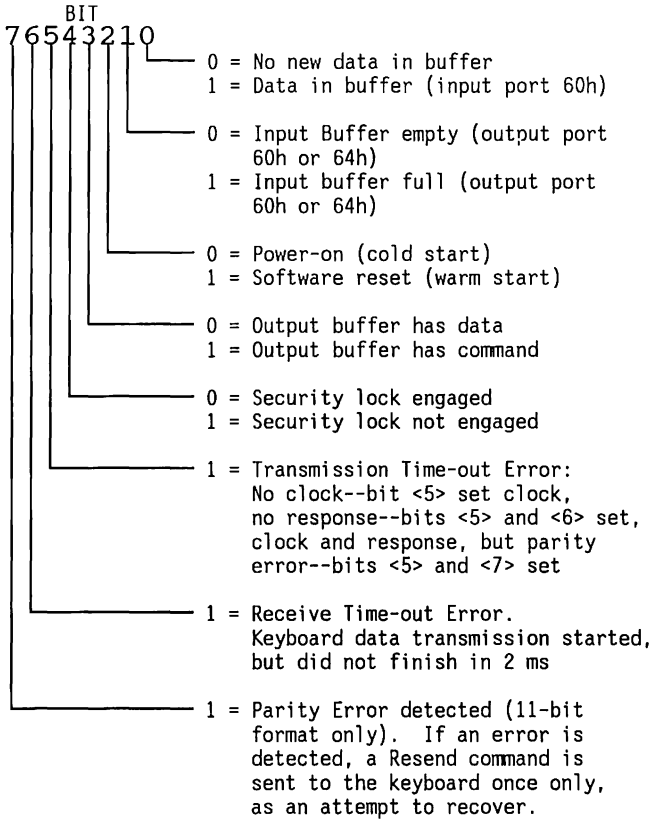


Figure 2-60. 8042 Status Register (Input Port 64h)

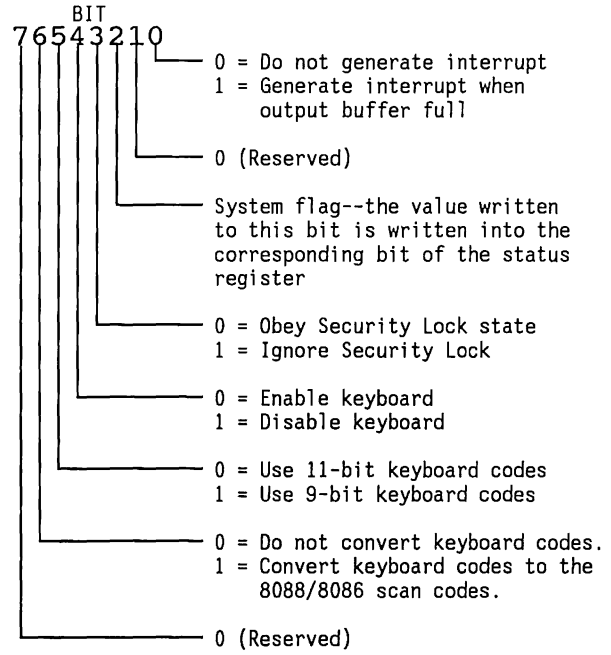


Figure 2-61. 8042 Command Byte (Output Port 64h).

Table 2-40. 8042 Command Codes (Output Port 64)

Code	Function
20h	Put the current command byte on the 8042's output port
60h	Load the next byte put into the 8042's input port as the command byte
A1h	FAST Speed--the 8042 output port selects the 8-MHz speed (SLOWDOWN bit = 0)
A2h	HIGH Speed--the 8042 output port selects an address-dependent speed (SLOWDOWN bit = 1.)
A4h	Toggle--the 8042 changes its speed-control output port bit between the FAST mode speed and the speed defined with the HIGHSP command (A6h).
A5h	Special Read--the 8042 places the real value of port 2 except for bits <4> and <5> which are given a new definition in the output buffer. No output-buffer full is generated. If bit <5> = 0 then a 9-bit keyboard is in use If bit <5> = 1, then an 11-bit keyboard is in use If bit <4> = 0, the interrupt is disabled If bit <4> = 1, interrupt is enabled when the output buffer full
A6h	HIGHSP--the 8042 interprets the next byte written to port 60h as the maximum speed for the system when the Toggle command (A4h) is used. Value Highest Speed 00h FAST (8 MHz) 01h HIGH (address-dependent speed) Note: Only the least-significant bit is used. The other bits should be set to 0.

(Continued)

Table 2-40. (Continued)

Code	Function
AAh	Initialization--the 8042 initializes ports 1 and 2 to their setup value, sets HIGHSP (CPU speed) to the value set by the jumper, disables the keyboard and clears the buffer pointers. It then places 55h in the output buffer.
ABh	Interface Test--directs the 8042 to test the data and clock lines of the keyboard interface. The output buffer (input port 60h) receives the test results, according to: 00h - No error detected 01h - The keyboard Clock line is stuck low 02h - The keyboard Clock line is stuck high 03h - The keyboard Data line is stuck low 04h - The keyboard Data line is stuck high 05h - COMPAQ diagnostic feature Note: The keyboard Data line test does not check for line stuck low for 9-bit keyboards.
ACh	Diagnostic Dump--Reserved for diagnostic purposes.
ADh	Disable Keyboard--sets bit <4> of the 8042's command byte, which disables the keyboard interface. Data are not sent or received until the keyboard is enabled.
AEh	Enable Keyboard--resets bit <4> of the 8042's command byte, which enables the keyboard interface.
C0h	Read Input Port--directs the 8042 to transfer the status of the input port and place it in the output buffer (input port 60h). Use this command only when the output buffer is empty.
D0h	Read Output Port--directs the 8042 to transfer the current byte in the output port to the output buffer (input port 60h). The values for the SPEEDUP and SLOWDOWN bits (D6 and D7) will not be accurate. Use the Special Read command (A5h) to read the correct values. Use the Read Output Port command only when the output buffer is empty.

(Continued)

Table 2-40. (Continued)

Code	Function
D1h	Write Output Port--place the next byte written to the 8042 data register (output port 60h) on the 8042's output port. The system speed bits are not set by this command--use commands A1h to A6h for speed functions. **CAUTION** Setting bit <0> of the 8042's Output Port 0 puts the system in a reset state until the power is turned off.
E0h	Read Test0 and Test1 Inputs--directs the 8042 to put the current state of Test0 and Test1 into the output buffer (output port 60h). Test0 is bit <0> and Test1 is bit<1>.
F0h-FFh	Pulse Output Port--the 8042's output port, bits <3..0>, can be pulsed (strobed low) for approximately 2 us. Bits <3..0> of this command byte each represent one bit, or signal of the output port to be pulsed. Note: Bit <0> of the 8042's Output Port 0 is connected to the system reset. Pulsing bit <0> resets the system.

System Scan Codes

Table 2-41 shows the codes sent by the keyboard to the 8042 for each key and the final code sent to the system by the 8042.

Table 2-41. Keyboard Scan Codes

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
	00h	FFh (Note 1)	
ESC	76h	01h	01h
1,!	16h	02h	02h
2,@	1Eh	03h	03h
3,#	26h	04h	04h
4,$	25h	05h	05h
5,%	2Eh	06h	06h
6,^	36h	07h	07h
7,&	3Dh	08h	08h
8,*	3Eh	09h	09h
9,(	46h	0Ah	0Ah
0,)	45h	0Bh	0Bh
-,_	4Eh	0Ch	0Ch
=,+	55h	0Dh	0Dh
<--	66h	0Eh	0Eh

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Tab	0Dh	0Fh	0Fh
Q	15h	10h	10h
W	1Dh	11h	11h
E	24h	12h	12h
R	2Dh	13h	13h
T	2Ch	14h	14h
Y	35h	15h	15h
U	3Ch	16h	16h
I	43h	17h	17h
O	44h	18h	18h
P	4Dh	19h	19h
[,{	54h	1Ah	1Ah
],}	5Bh	1Bh	1Bh
RET	5Ah	1Ch	1Ch
Ctrl	14h	1Dh	1Dh
A	1Ch	1Eh	1Eh
S	1Bh	1Fh	1Fh
D	23h	20h	20h
F	2Bh	21h	21h
G	34h	22h	22h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
H	33h	23h	23h
J	3Bh	24h	24h
K	42h	25h	25h
L	4Bh	26h	26h
;,:	4Ch	27h	27h
',"	52h	28h	28h
`,~	0Eh	29h	29h
Lshift	12h	2Ah	2Ah
\,|	5Dh	2Bh	2Bh
Z	1Ah	2Ch	2Ch
X	22h	2Dh	2Dh
C	21h	2Eh	2Eh
V	2Ah	2Fh	2Fh
B	32h	30h	30h
N	31h	31h	31h
M	3Ah	32h	32h
,,<	41h	33h	33h
.,>	49h	34h	34h
/,?	4Ah	35h	35h
Rshift	59h	36h	36h
*,PrtSc	7Ch	37h	37h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
Alt	11h	38h	38h
Space	29h	39h	39h
Caps Lock	58h	3Ah	3Ah
F1	05h	3Bh	3Bh
F2	06h	3Ch	3Ch
F3	04h	3Dh	3Dh
F4	0Ch	3Eh	3Eh
F5	03h	3Fh	3Fh
F6	0Bh	40h	40h
F7	02h,83h (Note 2)	41h	41h
F8	0Ah	42h	42h
F9	01h	43h	43h
F10	09h	44h	44h
Num Lock	77h	45h	45h
Scroll Lock	7Eh	46h	46h
Home,7	6Ch	47h	47h
Up,8	75h	48h	48h
PgUp,9	7Dh	49h	49h

(Continued)

Table 2-41. (Continued)

U.S. Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
-	7Bh	4Ah	4Ah
Left,4	6Bh	4Bh	4Bh
5	73h	4Ch	4Ch
Right,6	74h	4Dh	4Dh
+	79h	4Eh	4Eh
End,1	69h	4Fh	4Fh
Down,2	72h	50h	50h
PgDn,3	7Ah	51h	51h
Ins,0	70h	52h	52h
Del,.	71h	53h	53h
Sys Req	7Fh,84h (Note 2)	54h	

(Continued)

Table 2-41. (Continued)

US Character	11-bit Keyboard Scan Code	System Scan Code	9-Bit Keyboard Scan Code
R (Note 3)	60h	55h	
R (Note 3)	61h	56h	
F11 (Note 4)	78h	57h	
F12 (Note 4)	07h	58h	
R (Note 3)		59h through 7Fh	

Notes: 1. When the 8042 cannot read data from the keyboard, the 8042 sends FFh to the system, and sets the parity error bit of the Status register.

2. The second value is generated when the 8042 translates a 9-bit code to an 11-bit code.

3. R = Reserved

4. The F11 and F12 keys (System Scan Codes 57H and 58h respectively) are only available on the COMPAQ Enhanced Keyboard.

8042/Keyboard Communications Time Restraints

If a code transmission from the keyboard exceeds 2 ms, a time-out error results and the 8042 sends FFh to the system. No retries are attempted from a time-out error.

A keyboard Clock signal strobes the 8042 during a data transmission to cycle data bits from the 8042 to the keyboard.

If the keyboard clock does not begin strobing within 15 ms after a byte is ready to transmit, or if the byte is not completely transmitted within 2 ms, the 8042 sends FEh to the system and sets the transmit time-out error bit in the Status register.

The keyboard must respond to all transmissions from the 8042 within 25 ms, or the parity and time-out error bits are set in the Status register of the 8042 and FEh is sent to the system. No retries are attempted by the 8042 after any data transmission error.

Security Key Lock

The security key lock is connected to the P17 line of the 8042 keyboard processor. When the security lock is locked, the keyboard is disabled. This feature allows a program to continue without accidental interference.

Interval Timer

The purpose of a programmable interval timer is to generate pulses at software-controllable intervals.

An Intel 8254 Programmable Interval Counter on the system boards provide three frequencies, or timed pulses, for the system. The three counters count down a 16-bit value at a rate of 1.193 million counts-per-second and give an output pulse on the OUT pins. Table 2-42 lists the interval timer functions.

Two channels (interrupt and refresh) are on at all times; only the speaker tone can be disabled and enabled.

Table 2-42. Interval Timer Functions

Function	System Timer
Counter 0:	
Gate	Always On
Clock In	1.193 MHz
Clock Out	8259A IRQ0
Counter 1:	
Gate	Always On
Clock In	1.193 MHz
Clock Out	Request Refresh
Counter 2:	
Gate	Programmable
Clock In	1.193 MHz
Clock Out	Speaker Input

Interval Timer Architecture

The interval timer contains three identical counters. Figure 2-62 shows the architecture of the interval timer. CRm and CRl contain the most- and least-significant bytes of the 16-bit initial count value. These registers are cleared when they are both transferred into CE.

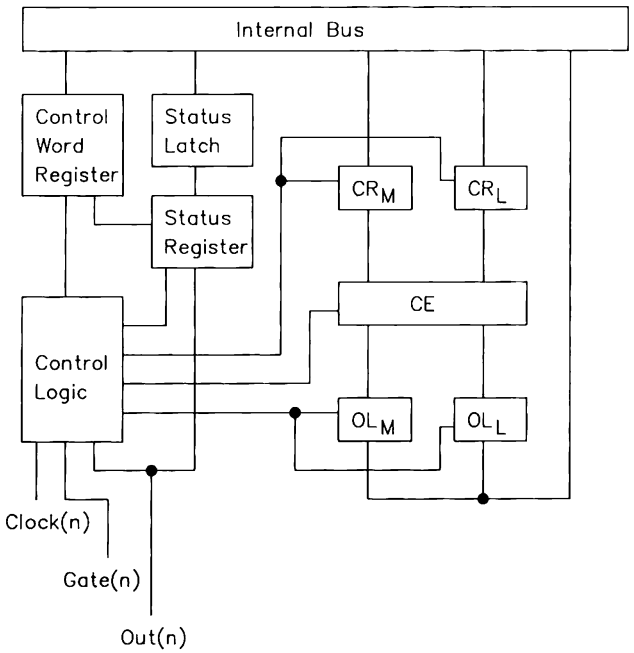


Figure 2-62. Counter Architecture

CE is the actual "Counting Element" latch that contains the value being counted down.

OLm and OLl contain the most- and least-significant bytes of the CE value, unless a latch command is given. In this case, the OLm and OLl registers hold the count until read.

Programming the Interval Timer

The timer is an I/O-mapped device. Table 2-43 lists the ports used. Several commands are available:

- The Control Word specifies:
  - which counter to read or write
  - the operating mode
  - the count format
- The Counter Latch command latches the current count so that it can be read by the system. The count-down process continues.
- The Read Back command reads the count value, programmed mode, the current state of the OUT pins, and the state of the null count flag of the selected counter.

Table 2-43. Interval Timer Port Assignments

Port	Function
40h	Read or Write Count for Counter 0 (System Clock)
41h	Read or Write Count for Counter 1 (Refresh Request)
42h	Read or Write Count for Counter 2 (Speaker Tone)
43h	Input for Control Word, Counter Latch, or Read Back commands (Command Mode Register)

Interval Timer Operating Modes and Initial Values

Six operating modes are available and are listed in Table 2-44.

Table 2-44. Interval Timer Operating Modes

Mode	Function
0	Out signal on end-of-count (=0)
1	Hardware retriggerable one-shot
2	Rate generator (divide-by-n counter)
3	Square-wave output
4	Software-triggered strobe
5	Hardware-triggered strobe

The three counters are initialized with the values given in Table 2-45.

Table 2-45. Interval Timer Initial Values

Counter	Mode	Control Word	Count	Frequency
0	3	36h	65535	18.207 Hz
1	2	54h (See Note)	19	62.799 KHz
2	3	B6h	1336	893.10 Hz

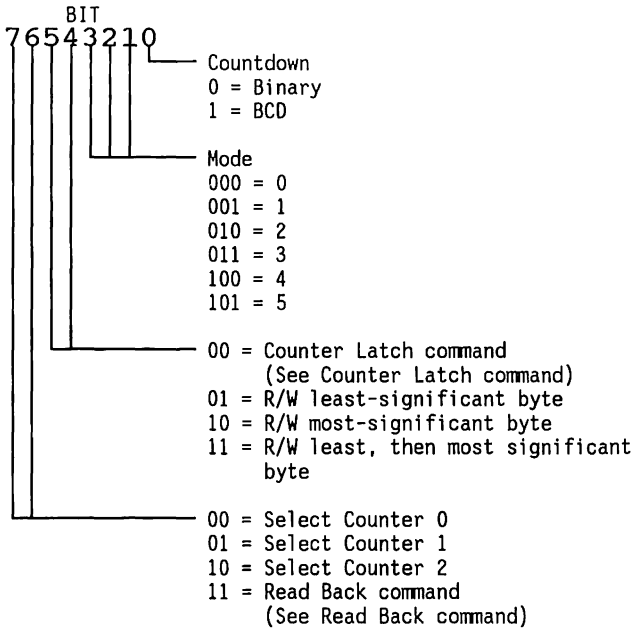
Note: Only the least-significant byte of the divisor is loaded.

Programming the interval timer is a simple process:

1. Write a control word.
2. Write an initial count for each counter.
3. Load the least- and most-significant bytes of the 16-bit counter in two steps (writes).

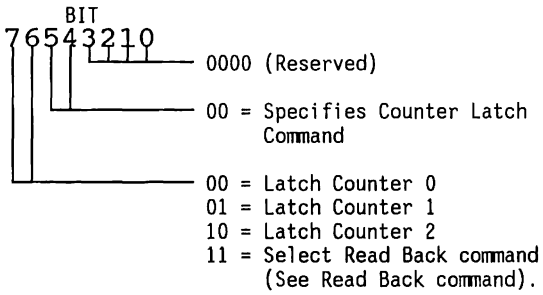
Interval Timer Control Word Format

The Control Word specifies the counter, whether it is to be written to or read from, the operating mode, and whether it counts down in a 16-bit or binary-coded decimal (BCD) format.



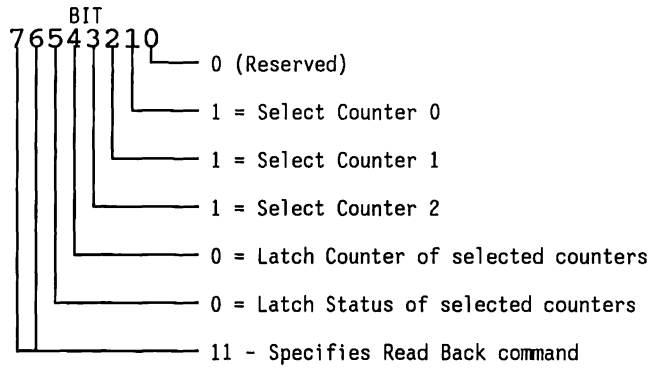
Interval Timer Counter-latch Command

The Counter Latch command latches the count at the time the command is received. The count is held in the OL registers until read.

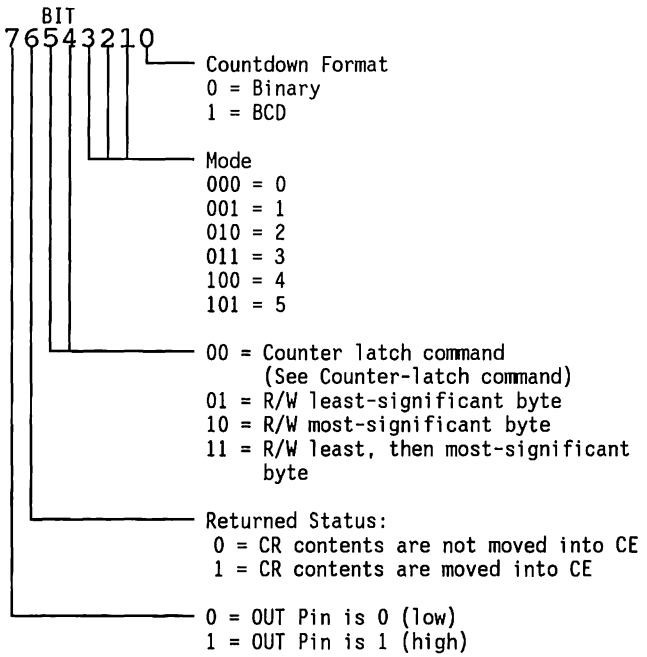


Interval Timer Read Back Command

The Read Back command causes the count or status of the counters to be latched in the OL registers until read. A single read-back can latch the count or status of all three counters.



The status byte latched into OL has the following format:



Interrupt Priority Encoders

The 80286 processor has two signals for interrupts, labelled NMI (nonmaskable interrupt) and INTR (maskable interrupts). A maskable interrupt is an interrupt that can be enabled or disabled by the processor STI/CLI instructions. A nonmaskable interrupt is not masked off by the CLI instruction but can be disabled under software control by the system board logic.

NMI Interrupts

NMI interrupts are caused by parity errors on the system board, memory boards, or any expansion boards that pull the IOCHK- line low.

System software can also generate a software interrupt to the NMI routine. When the IOCHK- line is pulled low, it sets the IOCHK- latch, which holds the error condition until software can examine it.

The source of the NMI can be determined by examining input port 61h, bit <6>. If this bit is set, the interrupt came from the hardware IOCHK- line. To clear the hardware IOCHK- latch, pulse bit <3> of port 61h high.

The mask register for the NMI interrupt is at I/O-address 70h. The format for this byte is 10000000, that is, only the most significant bit is decoded. Write an 80h to port 70h to mask the NMI signal. This port is shared with the real-time clock and configuration memory device (the lower 6 bits). Do not modify the contents of this register without considering the effects on the state of the other bits.

INTR Interrupts

All INTR-type interrupts to the CPU are channelled through the interrupt controllers (8259A). These devices generate interrupts on the 80286's interrupt line, which can be masked in the 80286 by software.

The interrupt controllers are 8-input devices that can accept interrupt signals from several devices, then prioritize them and interrupt the processor. The processor then automatically reads the interrupt controller to determine the source of the highest-priority interrupt and calls the appropriate interrupt routine.

Two interrupt controllers (a master and a slave) are used so that more than eight levels of interrupt are possible. The slave (Interrupt Controller 2) interrupts the master (Interrupt Controller 1) to show an interrupt. When Interrupt Controller 1 is properly programmed (in the special fully nested mode) Interrupt Controller 2 sends the correct interrupt vector to the CPU for the source of the interrupt. Figure 2-63 shows a diagram of the interrupt controller circuit.

All interrupts can be masked off, using the CLI instruction of the 80286. The base I/O address for Interrupt Controller 1 is 20h; for Interrupt Controller 2 it is A0h. Table 2-46 lists the initial interrupt controller values.

Table 2-46. Initial Interrupt Controller Values

Port	Value	Description of Contents
20h	11h	Cntlr 1, ICW1
21h	08h	Cntlr 1, ICW2 vector address for 000020h
21h	04h	Cntlr 1, ICW3 indicates slave connection
21h	01h	Cntlr 1, ICW4 8086 mode
A0h	11h	Cntlr 2, ICW1
A1h	70h	Cntlr 2, ICW2 vector address for 0001C0h
A1h	02h	Cntlr 2, ICW3 indicates slave ID
A1h	01h	Cntlr 2, ICW4 8086 mode
A21h	B8h	Cntlr 1, Interrupt mask (may vary with option)
A1h	9Dh	Cntlr 2, Interrupt mask (may vary with option)

Table 2-47 lists the 16 possible sources for an interrupt and their priorities. The highest-priority interrupt is processed first.

Table 2-47. Interrupts And Their Priorities

Priority	Label	Controller	Typical Interrupt Source
1	NMI	(Note)	Parity Error Detected
2	IRQ0	1	Interval Timer Output 0
3	IRQ1	1	Keyboard
	IRQ2	1	Interrupt from Controller 2
4	IRQ8	2	Real-Time Clock
5	IRQ9	2	Expansion Bus Pin B04
6	IRQ10	2	Expansion Bus Pin D03
7	IRQ11	2	Expansion Bus Pin D04
8	IRQ12	2	Expansion Bus Pin D05
9	IRQ13	2	Numeric Coprocessor
10	IRQ14	2	Fixed Disk Drive Controller --Expansion Bus Pin D07
11	IRQ15	2	Expansion Bus Pin D06
12	IRQ3	1	Serial Port 2 --Expansion Bus Pin B25
13	IRQ4	1	Serial Port 1 --Expansion Bus Pin B24
14	IRQ5	1	Parallel Port 2 --Expansion Bus Pin B23
15	IRQ6	1	Diskette Drive Controller --Expansion Bus Pin B22
16	IRQ7	1	Parallel Port 1 --Expansion Bus Pin B21

Note: The NMI signal is controlled through the I/O port 70h, bit <7>.

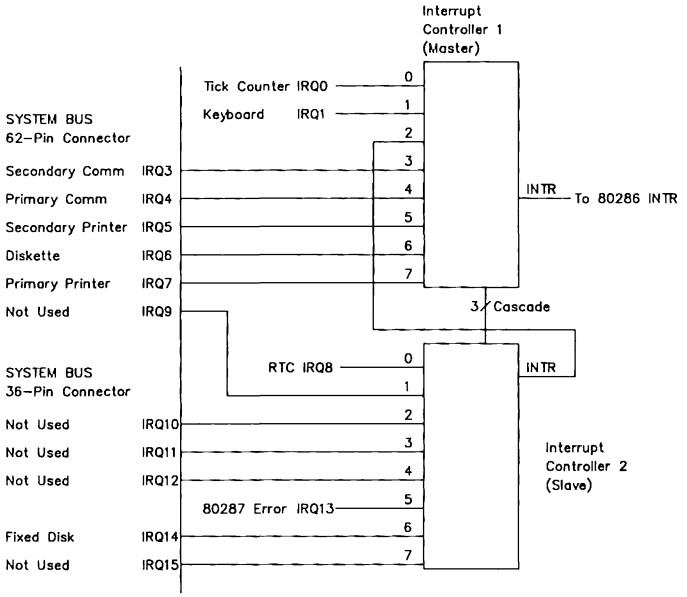


Figure 2-63. Interrupt Controller Circuit Diagram

2.15 EXPANSION BUS

The system board uses expansion slots to support additional circuit boards.

Expansion slots have either two connectors (62-pin and 36-pin) or one connector (62-pin). Slots with both connectors support a 16-bit data bus and the high-order address lines, LA<23..17> as well as additional interrupt and DMA lines. Slots with only one connector support only an 8-bit data bus with address lines SA<19..0>.

This section presents the expansion bus and the system timing requirements and includes:

- Detailed explanations of the expansion bus signals
- Major functions supplied to the expansion bus, such as:
  - Address Handling
  - Data Handling
  - Non-CPU Operations
  - DMA Operations
  - Dynamic RAM Refresh
  - Other Bus Master Operations
- Timing Considerations

Address Handling

When the CPU begins a bus cycle, it places an address on the address bus. This address may be placed on the bus while the previous cycle is still in progress. Since most devices expect to see a valid address for the duration of a bus cycle, the system board latches the address onto the system bus.

System bus lines that contain the latched address are SA<19..0>. These latches are of the fall-through type so that when the address latch enable signal (ALE) goes active, the address appears at the output. When ALE goes inactive, the addresses will stay on the outputs until the next bus cycle begins.

Some high speed devices overlap some operations ,such as address decoding. To allow this, the system bus provides a set of address lines (LA<23..17>) that are not latched but which provide a greater setup time to do decoding. When the address changes, expansion bus devices may decode the high-order address lines and then latch them using BALE. This allows expansion bus devices to take advantage of addresses for the next bus cycle that may be placed on the bus before the current bus cycle is complete.

When other devices (such as DMA or other bus masters) take control of the system bus, the BALE line is held active for the entire duration of the operation. As a result, expansion bus devices cannot use BALE to latch the high-order address lines. Therefore, LA<23..17> should be held stable for the entire duration of each bus cycle.

Data Handling

Data handling for these products is accomplished with two data buses. The first is the 8-bit bus that is compatible with previous products. It is provided by the SD<7..0> lines. External devices and memory that are limited to 8-bit transfers use this bus and the control lines SMRDC-, SMWTC-, IORC-, and IOWC- to enable or latch data on the bus.

Devices that can transfer data 16 bits at a time must also use the SD<15..8> lines for data transfer. The lines SBHE- and SA0 are used to determine which byte(s) are desired. These devices tell the system board that they are 16-bit devices by setting the M16- or IO16- (as appropriate) when they are addressed. Table 2-48 lists the signal relationships.

During 12-MHz local memory cycles, the MRDC-, MWTC-, SMRDC-, SMWTC-, IROC-, IOWC-, and SBHE- strobes are inhibited on the expansion bus. This allows maximum compatibility with the standard 8-MHz expansion bus.

Table 2-48. M16-, IO16-, SA0, and SBHE- Signal Relationship

M16- or IO16-	SA0	SBHE-	Cycle Type
High	High	----	Odd byte transfer on lines SD<7..0>
High	Low	----	Even-byte transfer on lines SD<7..0>
Low	High	High	Reserved
Low	High	Low	Odd-byte transfer on lines SD<15..8>
Low	Low	High	Even-byte transfer on lines SD<7..0>
Low	Low	Low	Even-word transfer on lines SD<15..0>

Non-CPU Operations

The system board supports several operations that are not related to the processor chip itself. These are refresh, traditional direct memory access, and expansion bus master access. Refresh is provided to prevent loss of data in dynamic RAMs (DRAMs). The other operations are used by expansion bus devices that require access to memory or I/O without processor intervention.

The system board prioritizes the requests for each type of service according to the following rules:

- If the CPU is the bus master, it completes the current processor cycle. This includes word operations to 8-bit memory, which execute as two single-byte operations.
- If the CPU has an instruction LOCKed, it will complete the instruction.
- There is an automatic LOCK between an interrupt acknowledge and the first bus write in the acknowledge sequence.
- In the 80286 Protected-Virtual mode, segment-description operations are automatically LOCKed; that is, six words are loaded at one time.
- Refresh and other DMA cycles are started on a first-come, first-served basis after the CPU releases the bus.
- If a refresh is in progress when a DMA cycle is requested, the DMA cycle will be run without allowing the CPU to regain control of the bus.
- If a direct memory cycle is in progress when a refresh is requested, the refresh cycle will be run without allowing the CPU to regain control of the bus.
- The DMA controller will hold the bus until all outstanding DMA requests are handled.
- If a DMA channel is programmed for demand or block transfer modes, the DMA controller will keep the bus for the entire time to complete the programmed operation.
- Wait states or 8-bit memory anywhere in the system can delay the time required to acknowledge a DMA request.

Because of the above conditions, peripheral designers must assume that the latency on any DMA request can be as high as 10-12 us in a typical system using only diskette operations. If more than one DMA device is operating at one time, the latency can be even greater. If a program uses a LOCK prefix before string instructions or uses block- or demand-mode DMA, then the latency could reach the millisecond range.

DMA Operations

The DMA controllers in the system operate as a separate subsystem from the main bus controller. They handle requests from the DMA peripherals, arbitrate between them, and then request access to the system address and control lines from the CPU.

There are two types of DMA: byte and word. One of the DMA controllers is connected to handle byte-DMA operations, the other, word-DMA operations. To simplify the arbitration between sources, the request line from the byte controller is connected to a DMA request line (DRQ4) on the word controller. The word DMA controller is programmed for cascade mode on channel 0 (to which DRQ4 is connected) so that it will not actually place an address on the bus when it acknowledges the byte controller's request.

Byte-DMA Operations

The DMA byte cycle begins when a peripheral sets a DRQ<3..0> line active. The DMA controller then arbitrates among any other pending requests and sets the hold request output active. This line (DRQ4) is connected to the word controller, as discussed above, which does its arbitration. The word controller then sets its hold request line active, which is in turn synchronized and arbitrated by the hold arbitration logic discussed above.

When the system responds to the request with an acknowledge, the word DMA controller will respond with a DAK4, which acts as a hold acknowledge to the byte controller. After synchronizing the acknowledge, the byte controller will place an address on the bus lines.

Logic drives the SBHE- line in the opposite sense of SA0 in order to satisfy 16 bit devices on the bus. When the 16-bit devices are stabilized, the DMA controller drives the lines IORC-, IOWC-, MWTC-, and MRDC- according to the type of cycle being run. If SA0 is high and the addressed memory is 16-bit, logic routes the data between the low half and high half of the data bus. The data is moved from high to low on memory reads and from low to high on memory writes.

Word-DMA Operations

Word-DMA operations are possible only between word memory (16 bit) and word peripherals. Also, the DMA cannot operate on an odd-address boundary, on either memory or I/O. The system latches the SA0 and SBHE- lines to enable 16-bit devices on the bus.

The word-DMA cycle begins when a peripheral sets a DRQ5-DRQ7 line active. The DMA controllers then arbitrate among any other pending requests and set the hold request output active.

When the system responds to the request, the word-DMA controller will, after synchronizing the acknowledge, respond with a DAKx acknowledge to the peripheral. The DMA controller will place the address on the bus and then drive the control lines.

Dynamic RAM Refresh

The dynamic RAM refresh subsystem is designed to do a memory read cycle on each of 512 addresses in the memory space as addressed by SA<8..0>. During the RAM refresh time the other address lines are in an undefined state. The system can also be driven by an external source if another bus master has control.

The system consists of a timer (part of the 8254) that generates the refresh requests every 15.924 us, arbitration logic that arbitrates whether the refresh controller or the DMA subsystem gets control of the bus, a timing generator, and a refresh address counter. The refresh request rate of 62.799 kHz provides 128 refresh cycles in 2.038 ms, or 256 cycles in 4.0765 ms, or 512 cycles in 8.153 ms.

If an external bus master wishes to take the bus for long periods of time, it must perform refresh or risk losing the contents of dynamic memory. The external bus master can do this by developing its own refresh request timer and internal arbitration.

When it is not otherwise driving the bus but still has bus control, the bus master can generate a refresh cycle by pulling the REFRESH- line low with an open collector gate. When the MRDC- line goes inactive from the refresh cycle, the REFRESH- line should be released. The external bus master can then take full control.

Other Operations by Bus Masters

This system allows other bus masters to take over the system buses and use the I/O peripherals and memory. This is accomplished by the bus master software programming an unused DMA channel for cascade operation. When this is complete, the bus master can request the bus by setting the appropriate DRQx (<7..5>, <3..0>) line active and waiting for a response.

When the system responds with DAKx, the bus master can pull the GRAB- line active (low), disabling the address, data, and control lines. The bus master should then wait one BCLK period before enabling its own buffers with valid address information and wait one more BCLK period before driving the control lines.

When the bus master is finished, it should release the GRAB- and DRQx lines to allow the CPU to continue operations. If the bus master keeps control of the bus for more than 15 us, then it must provide its own refresh timing and request logic to prevent loss of dynamic memory contents.

Bus Driving/Loading Information

The following information is provided to improve the probability that third-party controller boards will work with the standard COMPAQ boards and options.

On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 mA and source 10 mA at 0.5 Vdc and 2.4 Vdc respectively.

On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 mA at 0.5 Vdc.

The load on any logic line from a single bus slot should not exceed -2.0 mA in the low state (at 0.5 Vdc) or 0.1 mA in the high state (at 2.7 Vdc).

The logic-high voltage at the expansion bus ranges from 2.0 Vdc to 5.5 Vdc. The logic low voltage at the expansion bus ranges from -1.2 Vdc to 0.8 Vdc.

Bus Timing Information

In the HIGH mode, the system clock toggles between two frequencies (12 MHz or 8 MHz) according to address, in which case the new speed will occur during the BALE time.

During these changes, the bus timings for the affected cycles will be somewhere between the actual 12 MHz and 8 MHz timings. Table 2-49 lists the important timing parameters for the expansion slots. This information assumes that the system clock is at a constant speed of 8 MHz.

NOTE: The expansion bus timing information is provided to aid in a general understanding of the system and is subject to change.

Table 2-49. Expansion Slot Timing Parameters

Address access time from SA<19..0> address lines, 16 bit bus read cycle.	
Access time 8 MHz	228 ns
Address access time from SA<19..1> address lines, 8 bit bus read cycle.	
Access time 8 MHz	603 ns
Address access time from SA0 address line, 8 bit bus read cycle.	
Access time 8 MHz	589 ns
Access time from BALE active, 16 bit bus read cycle.	
Access time 8 MHz	232 ns
MRDC- Access time, 16-bit bus read cycle.	
Access time 8 MHz	190 ns
IORC- access time, 16-bit bus read cycle.	
Access time 8 MHz	127 ns
MRDC-, IORC-, access time, 8-bit bus read cycle.	
Access time 8 MHz	502 ns
SMRDC- access time, 8-bit bus read cycle.	
Access time 8 MHz	484 ns
CPU read data hold from MRDC-, IROC-, inactive, 8-bit bus cycle.	
Hold 8 MHz	1 ns

(Continued)

Table 2-49. (Continued)

LAx address valid to 16-bit memory command setup.	
Setup 8 MHz	106 ns
16-bit bus memory cycle M16- low delay from LAx address valid.	
Maximum allowed delay 8 MHz	108 ns
BALE valid to 16-bit memory command setup.	
Setup 8 MHz	20 ns
BALE valid to M16- setup.	
Setup 8 MHz	7 ns
SA<19..0> address valid to 16-bit memory command setup.	
Setup 8 MHz	22 ns
SA<19..0> address valid to I/O, 8-bit command setup.	
Setup 8 MHz	84 ns
SA0 address hold from command.	
Hold 8 MHz	96 ns
SA<19..1> address hold from command.	
Hold 8 MHz	110 ns
CPU write data setup to MWTC- active, 16-bit bus memory cycle.	
Setup 8 MHz	-5 ns

(Continued)

Table 2-49. (Continued)

CPU write data setup to IOWC- (16/8-bit), MWTC- (8-bit), active.	
Setup 8 MHz	58 ns
CPU write data setup to MWTC-, IOWC-, inactive, 16-bit bus cycle.	
Setup 8 MHz	245 ns
CPU write data setup to MWTC-, IOWC-, inactive, 8-bit bus cycle.	
Setup 8 MHz	620 ns
Refresh address setup to MRDC- active.	
Setup 8 MHz	76 ns
Refresh address hold from MRDC- inactive.	
Hold 8 Hz	-5 ns
Refresh wait state BUSRDY low delay from MRDC- active.	
Maximum allowed delay 8 MHz	90 ns
Refresh wait state BUSRDY high setup to BCLK rising.	
Setup 8 MHz	5 ns
CPU memory or I/O command wait state BUSRDY high setup to BCLK rising.	
Setup 8 MHz	51 ns
CPU 16-bit memory command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	75 ns

(Continued)

Table 2-49. (Continued)

CPU 16-bit I/O command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	12 ns
CPU 8-bit command wait state. BUSRDY low delay from command active.	
Maximum allowed delay 8 MHz	387 ns
CPU minimum command active from BUSRDY high after added wait state.	
Command active 8 MHz	135 ns
CPU maximum command active from BUSRDY high after added wait state.	
Command active 8 MHz	300 ns
CPU 16-bit memory command no wait state NOWS- low delay from command active.	
Maximum allowed delay 8 MHz	20 ns
CPU 8-bit memory command no wait state NOWS- low setup to BLCK falling required.	
Setup required 8 MHz	16 ns
DMA memory read, I/O write command additional wait state. BUSRDY low delay from memory read command active.	
Maximum allowed delay 8 MHz	182 ns
DMA I/O read, memory write command additional wait state. BUSRDY low delay from I/O read command active.	
Maximum allowed delay 8 MHz	273 ns

(Continued)

Table 2-49. (Continued)

Required I/O data access time from IORC- for DMA write to RAM.	
DMA I/O read access time 8 MHz	264 ns
DATA valid after IOWC- low during DMA read from RAM.	
DMA data valid from IOWC- low 8 MHz	163 ns
DATA setup to IOWC- high during DMA read from RAM.	
Data setup to IOWC- high 8 MHz	217 ns

2.16 MISCELLANEOUS SYSTEM BOARD INFORMATION

This section contains miscellaneous information that does not relate to any of the other sections, such as:

- Speed control
- Real-Time Clock and Configuration-Memory Battery
- Indicators
- Fuses
- Speaker Interface
- Clock Circuits
- System Board Power Requirements

Speed Control

- FAST - I/O speed = 8 MHz, memory speed = 8 MHz
- HIGH - I/O speed = 8 MHz
  Memory Speed (Expansion Bus) = 8 MHz
  Memory Speed (System Board) = 12 MHz
- AUTO - operates in HIGH, except to switch to 8 MHz during diskette operations

In the FAST mode, all memory addresses or bus cycle types operate at 8 MHz except:

- DMA transfers (4 MHz)

The HIGH mode operates the system board RAM and ROM at a faster (12 MHz) speed. In the HIGH mode, the following memory addresses or bus cycle types continue to operate at 8 MHz:

- Memory with addresses 000000h to 09FFFFh not physically located on the system board.
- Memory with addresses 0A0000h to 0DFFFFh
- Memory with addresses 100000h to FDFFFFh not physically located on the system board.
- All I/O devices, except DMA transfers (4 MHz)
- Any 8-bit memory device

In the HIGH mode, the following memory addresses or bus cycle types operate at 12 MHz:

- RAM in base memory (000000h to 09FFFFh) physically located on the system board.
- RAM in extended memory (100000h to FDFFFFh) physically located on the system board
- ROM (0E0000h to 0FFFFFh and FE0000h to FFFFFFh))

The speed is controlled by system software through the keyboard controller (8042).

The AUTO mode is a subset of the HIGH mode. In the AUTO mode, all cycles operate as in HIGH mode, except that the default system speed automatically switches to 8 MHz during diskette operations.

Switch SW1 position 6 together with the AUTO jumper sets the speed of the CPU when the system is powered-on. When the speed switch is OFF and AUTO is disabled, the system boots in the HIGH mode, and the CPU speed can be toggled between HIGH and FAST mode using the multiple key combination of Ctrl, Alt, \.

When the speed switch is OFF and AUTO is enabled, the system will boot in the AUTO mode, and the CPU speed can be toggled between AUTO and FAST mode using the multiple key combination of Ctrl, Alt, \.

When the speed switch is ON, the CPU speed is limited to the FAST mode and use of the multiple key combination Ctrl, Alt, \ will not affect the CPU speed.

The MODE SPE[ED] command overrides the speed switch and AUTO jumper settings in all cases.

Real-Time Clock and Configuration-Memory Battery

Table 2-50 lists the battery voltage range at the battery connector under load condition.

Table 2-50. Battery Connector Pinout

Pin	Function	Battery Voltage Min.	Max.
1	+5 VDC Power	5.0	5.4
2	Keyed		
3	Not Used		
4	Ground	0.0	0.0

The voltage for a new battery must not exceed 6.2 V open circuit. The current drain on the battery varies with the voltage and the clock operating mode, but is between 50 to 90 uA after running SETUP. The maximum current is less than 150 uA.

CAUTION

Only Authorized Dealers should replace the system battery. Extreme caution must be observed to replace the battery with an identical battery type and on the correct connector pins.

Indicators (LEDs)

The system board has a light-emitting diode (LED) that lights when the +5 Vdc power is ON.

Fuses

The 12-MHz system board has no user-replaceable fuses.

Speaker Interface

The speaker interface allows the speaker to be driven from two sources: the 8254-2 interval timer 2, or the processor through port 61h bit <1>. In addition, the 8254 interval timer 2 can be enabled and disabled from port 61h bit <0>.

To use the 8254 interval timer to generate a tone, program Timer 2 to the desired frequency (the input clock rate is 1.193 MHz) and set port 61h bits <0> and <1> to 1. If the speaker is to be toggled directly by the CPU, port 61h bit <0> should be set to 0 and bit <1> should be toggled.

Clock Circuits

The two crystal oscillators on the system board provide:

- Clock frequencies for the 80286 processor and the entire system
- A clock source for video color-burst signal and general timing

A crystal oscillator provides a 48-MHz frequency that is divided by 2 or 3 (software-selected) by the clock-generator interface to provide a master clock for the 80286.

The clock generator interface then divides both the 48-MHz and the master clock to supply the clocks used by the 80287 and other clocked devices. This interface also controls the reset signal. System reset does not occur until power levels are stable, that is,until PWRGOOD signal from power supply becomes active.

A second crystal oscillator on the system board provides a 14.31818-MHz (4 times 3.579545 MHz) clock signal for color-burst timing. This clock signal connects to pin B30 of the board slots for use by the video controller and other boards.

System Board Power Requirements

The system board uses +5 VDC and +12 VDC power and distributes power for other components of the system from the -5 VDC, -12 VDC and auxiliary +12 VDC provided by the power supply.

2.17 GATE ARRAY DEVICES

The 12-MHz system board has three gate array devices:

- Memory and Speed Control (MSC) Gate Array
- Clock and Buffer Control (CBC) Gate Array
- Memory Map (MAP) Gate Array

This section describes the Gate Array Devices and provides a functional overview of each device.

MSC Gate Array

The MSC Gate Array includes the memory decoding and speed change functions.

The speed change function indicates whether the system should run at 12 MHz or 8 MHz when operating in the HIGH mode. The memory decoding functions include the generation of chip select and output enable signals, as well as multiple RAS and CAS lines for memory bank and hi/lo byte selection. In addition, the MSC Gate Array provides the address during REFRESH cycles.

CBC Gate Array

The CBC Gate Array provides buffer and clock control. It includes the clock switching/generation logic, generation of automatic and requested wait-states, shutdown logic, 8/16 bit bus conversion, and bus arbitration.

MAP Gate Array

The MAP Gate Array includes the DMA page register, as well as the circuitry for PORT B, SPEAKER and GATE control, REFRESH DETECT, and NMI control.

2.18 JUMPERS AND SWITCHES

The 12-MHz system board has three switch positions not used for memory selection (Figure 2-64). These switch positions are described in Table 2-51.

Table 2-51. System Board Switch SW1 Settings

SW1 Position	Setting	Description
6	CLOSED	CPU speed limit setting - 8 MHz (FAST)
	OPEN	CPU speed toggle active (HIGH/FAST or AUTO/FAST)
8	CLOSED	COMPAQ Graphics or RGBI Video Controller
	OPEN	non-COMPAQ monochrome/text video controller
7	CLOSED	Reserved

Legend: CLOSED = ON, OPEN = OFF

The AUTO jumper (labeled E5 on the system board) settings enables or disables an additional speed option. When AUTO is enabled, the default system speed automatically switches to 8 MHz during diskette drive operations. This allows time-dependent copy-protection schemes to work properly. Table 2-52 lists the AUTO jumper settings.

Table 2-52. AUTO Jumper (E5) Settings

Setting	Description
1-2	AUTO disabled (CPU toggle: HIGH/FAST)
1-2	AUTO enabled (CPU toggle: AUTO/FAST)

Note: The AUTO jumper has no effect if the speed switch is set to limit the CPU speed to FAST.

2.19 CONNECTORS AND EXPANSION SLOTS

Tables 2-53 and 2-54 list the system board connectors and expansion slots, respectively. Table 2-55 describes the expansion slot signals. Figures 2-64 through 2-74 show the connectors on the system board.

Table 2-53. System Board Connections

Function	COMPAQ DESKPRO 286 (12-MHz Only)
Fixed disk drive power	J109 or J110 (See Note)
Drive power(Out)	J111-J112
Monitor power	J113
Speaker	J115
Keyboard	J116
DC power(In)	J117
Battery	J118
Security lock	J119

Note: J110 is for a fixed disk drive back-up or second fixed disk drive.

Table 2-54. System Board Expansion Slots

Slot	62-Pin	36-Pin	Function
1	J101	J121	Expansion (available)
2	J102	N/A	Expansion (available)
3	J103	J123	Expansion (available)
4	J104	J124	Expansion (available)
5	J105	J125	Expansion (available)
6	J106	J126	Fixed Disk Drive Controller
7	J107	J127	Video Display Controller
8	J108	N/A	Diskette/Tape Controller

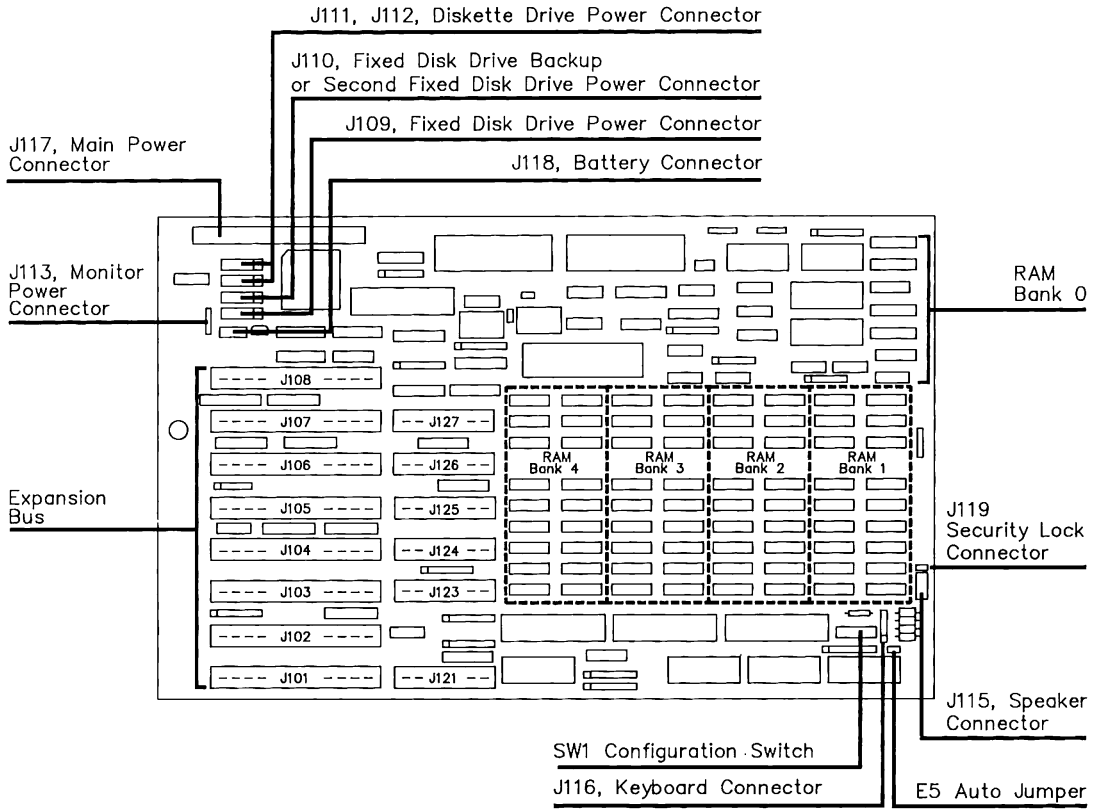


Figure 2-64. System Board Connectors, SW1 Switch, and AUTO Jumper Locations

Table 2-55. Expansion Slot Signals

Signal Name	Slot Pin	Type	Description
AEN	A11	O	This output signal when inactive (low) indicates that the CPU or controller board bus master has control of the bus. When active, the DMA controller has control of the bus. It is often used to disable devices which must not respond during a DMA cycle.
BALE	B28	O	This output signal (when high) indicates that a valid address is present on the LA<23..17> address lines. The LA<23..17> address lines or any decodes developed from them should be latched at the falling edge of BALE. This line is high when a DMA or bus master operation is occurring.
BCLK	B20	O	This output signal is provided to allow synchronization to the main processor clock. Its frequency will be either 8 MHz or 12 MHz.
BUSRDY	A10	I	This input signal is used to lengthen a bus cycle from its standard time if a controller board cannot respond quickly enough. It should be pulled low by an open collector type device as soon as a slow addressed device is selected and held low until the device has responded. Bus cycles are lengthened by an integral number of (BCLK) cycles. This line should not be held low for more than 2.5 us. This line should be driven by an open-collector device capable of sinking 20 mA.
DAK0- DAK1- DAK2- DAK3- DAK5- DAK6- DAK7-	D08 B17 B26 B15 D10 D12 D14	O O O O O O O	These output lines (DMA Acknowledge) indicate that a request for a DMA service from the DMA subsystem has been recognized. The acknowledge is indicated by a LOW on this line. Use this line with the IORC- or IOWC- line to decode the desired DMA device. If used to signal acceptance of a bus-master request, this signal indicates when it is legal to pull GRAB- low.
DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	D09 B18 B06 B16 D11 D13 D15	I I I I I I I	These input lines are used to request a DMA service from the DMA subsystem or to gain control of the system bus from the main CPU (DMA request). The request is made when the line goes from allow to a high and must remain high until the appropriate DAK<7..5>, <3..0> line goes active.

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
GRAB-	D17	I	This input signal is used to indicate that a controller board bus master is controlling the bus. A controller board can pull this line low when the appropriate DAK line is made active, signaling that a master request is granted. The system address, data and control lines will be floated, allowing the controller board to begin controlling them one full BCLK period after GRAB is made active. At least one more full BCLK period should be allowed after putting a valid address on the bus before activating any of the control lines. This line should be driven by an open-collector device capable of sinking 20 mA.
GROUND	B01	--	These lines are connected to the system ac and dc ground. The maximum current allowed on any single contact is 1.5 A.
	B10	--	
	B31	--	
	D18	--	
IOCHK-	A01	I	This input signal is used to signal the CPU about parity or other serious errors on controller boards. This signal should be driven low by an open collector type output capable of sinking 20 mA when an uncorrectable system error occurs.
IORC-	B14	I/O	This output line (I/O read) indicates (when low) when an I/O device is to send data to the data bus. It can be driven by a controller board acting as a bus master.
IOWC-	B13	I/O	This output line (I/O write) indicates (when low) when an I/O device is to accept the data from the data bus. It can be driven by a controller board acting as a bus master.
IO16-	D02	I	This input line (I/O is 16 bits) signals the system that the addressed I/O device is capable of transferring 16 bits of data at once. When this line is made active, during an I/O read or write, the standard one wait state I/O cycle will be run. This line should be driven low by an open-collector device capable of sinking 20 mA.
IRQ3	B25	I	These input lines are used to interrupt the CPU to request some service. The interrupt is recognized when the line goes from a low to a high and remains there until the appropriate interrupt service routine is executed.
IRQ4	B24	I	
IRQ5	B23	I	
IRQ6	B22	I	
IRQ7	B21	I	
IRQ9	B04	I	
IRQ10	D03	I	
IRQ11	D04	I	
IRQ12	D05	I	
IRQ14	D07	I	
IRQ15	D06	I	

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
LA17 LA18 LA19 LA20 LA21 LA22 LA23	C08 C07 C06 C05 C04 C03 C02	I/O I/O I/O I/O I/O I/O I/O	These output signals (Latchable Address) are used to decode memory which must respond with zero or one wait state. They are only guaranteed to be valid when BALE is high. These can be driven by a controller board acting as a bus master.
MRDC-	C09	I/O	This output line (Memory Read) indicates (when low) when a memory device is to send data to the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
MWTC-	C10	I/O	This output line (Memory Write) indicates (when low) when a memory device is to accept the data from the data bus. This signal is active over the entire address space of the system. It can be driven by a controller board acting as a bus master.
M16-	D01	I	This input line (memory is 16 bits) signals the system that the addressed memory is capable of transferring 16 bits of data at once. When this line is made active, during a memory read or write, the standard one wait state memory cycle will be run. This line should be derived from the LA<23..17> address lines. This line should be driven low by an open collector device capable of sinking 20 mA.
NOWS-	B08	I	This input line (No Wait State) is used to inform the system that standard wait states can be deleted for cycles when this line is made active. The line must be pulled low 45 ns before the falling edge of BCLK in order to be recognized. This line should be driven by an open collector device capable of sinking 20 mA.
OSC	B30	O	This output signal is a clock for use in video color burst and other general timing applications. Its frequency is 14.31818 MHz and duty cycle is approximately 50%.
REFRESH-	B19	I/O	This output signal is used to indicate (when low) a refresh cycle in progress. It should be used to enable the SA<8..0> address lines to the row address inputs of all banks of dynamic memory so that when the MRDC- goes active, the entire system memory is refreshed at one time. It can be driven by a controller board acting as a bus master.
RESDRV	B02	O	This output signal is used to reset the hardware during power-on or power failure.

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
SA0	A31	I/O	These bidirectional signals address memory or I/O devices within the system. They form the low order 20 bits of the 24 bit address bits that the system offers. These lines are enabled onto the bus while BALE is high and are latched when BALE goes from a high to a low state. These can be driven by a controller board acting as a bus master.
SA1	A30	I/O	
SA2	A29	I/O	
SA3	A28	I/O	
SA4	A27	I/O	
SA5	A26	I/O	
SA6	A25	I/O	
SA7	A24	I/O	
SA8	A23	I/O	
SA9	A22	I/O	
SA10	A21	I/O	
SA11	A20	I/O	
SA12	A19	I/O	
SA13	A18	I/O	
SA14	A17	I/O	
SA15	A16	I/O	
SA16	A15	I/O	
SA17	A14	I/O	
SA18	A13	I/O	
SA19	A12	I/O	
SBHE-	C01	I/O	This output signal (System Bus High Enable) indicates (when low) that the high half of the SD data bus should transfer the data on boards which support the full 16-bit data bus. It can be driven by a controller board acting as a bus master.
SD0	A09	I/O	These bidirectional signals are the low 8 bits of the system data bus. They should be used exclusively by all eight bit devices to transfer data. Sixteen-bit devices should use these lines to transfer only the low half of a data word when the address line A0 is low. These can be driven by a controller board acting as a bus master.
SD1	A08	I/O	
SD2	A07	I/O	
SD3	A06	I/O	
SD4	A05	I/O	
SD5	A04	I/O	
SD6	A03	I/O	
SD7	A02	I/O	

(Continued)

Table 2-55. (Continued)

Signal Name	Slot Pin	Type	Description
SD08 SD09 SD10 SD11 SD12 SD13 SD14 SD15	C11 C12 C13 C14 C15 C16 C17 C18	I/O I/O I/O I/O I/O I/O I/O I/O	These bidirectional signals are the high 8 bits of the system data bus. Sixteen bit devices should use these lines to transfer the high half of a data word when the line SBHE- is low. These can be driven by a controller board acting as a bus master.
SMRDC-	B12	O	This output line (Standard Memory Read) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MRDC-.
SMWTC-	B11	O	This output line (Standard Memory Write) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MWTC-.
T/C	B27	O	This output signal (when high) indicates that the Terminal Count of a DMA operation has been reached. It should be decoded with the appropriate DAKx line for proper operation.
+5 Vdc	B03 B29 D16	-- -- --	These lines are connected to the system power supply for 5 volts. In addition to the maximum current available from the supply, the maximum current allowed on any single contact is 1.5 A.
-5 Vdc	B05	--	This line is connected to the system power supply for minus 5 volts. This supply is intended for low-current usage only (500 mA).
-12 Vdc	B07	--	This line is connected to the system power supply for minus 12 volts. This supply is intended for low-current usage only (1.0 A).
+12 Vdc	B09	--	This line is connected to the system power supply for 12 volts. In addition to the maximum current available from the supply, the maximum current allowed on this contact is 1.5 A.

The 36-pin connector conducts the high-order byte of the 16-bit data bus, the memory address lines for bits DAK<7..5>, LA<23..17>, signals, and more. These signals generally relate to 16-bit or high-address memory transfers.

The 62-pin connector conducts the signals needed by adapters that do not need word-length data transfers or access to more than the base 1 MB of memory.

Figure 2-65 shows the 36-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
M16–	D01	C01	SBHE–
IO16–	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0–	D08	C08	LA17
DRQ0	D09	C09	MRDC–
DACK5–	D10	C10	MWTC–
DRQ5	D11	C11	SD8
DACK6–	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7–	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V	D16	C16	SD13
GRAB–	D17	C17	SD14
SIGNAL GROUND	D18	C18	SD15

Figure 2-66 shows the 62-pin connector and the signals that it provides.

Signal	Pin	Pin	Signal
GROUND	B01	A01	IOCHK–
RESDRV	B02	A02	SD7
+5 Vdc	B03	A03	SD6
IRQ9	B04	A04	SD5
–5 Vdc	B05	A05	SD4
DRQ2	B06	A06	SD3
–12 Vdc	B07	A07	SD2
NOWS–	B08	A08	SD1
+12 Vdc	B09	A09	SD0
GROUND	B10	A10	BUSRDY
SMWTC–	B11	A11	AEN
SMRDC–	B12	A12	SA19
IOWC–	B13	A13	SA18
IORC–	B14	A14	SA17
DAK3–	B15	A15	SA16
DRQ3	B16	A16	SA15
DAK1–	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH–	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DAK2–	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5 Vdc	B29	A29	SA2
OSC	B30	A30	SA1
SIGNAL GROUND	B31	A31	SA0

Figure 2-66. Expansion Slot - 62-Pin Connector

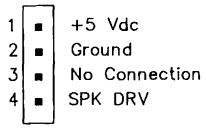


Figure 2-67. J109 and J110, Fixed Disk Drive or Fixed Disk Drive Back-up Power Connector

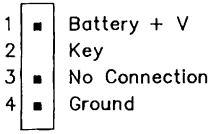


Figure 2-68. J111 and J112, Diskette Drive Power Connectors

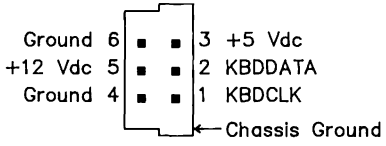


Figure 2-69. J113, Monitor Power Connector

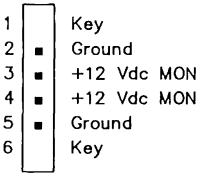


Figure 2-70. J115, Speaker Connector

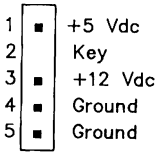


Figure 2-71. J116, Keyboard Connector

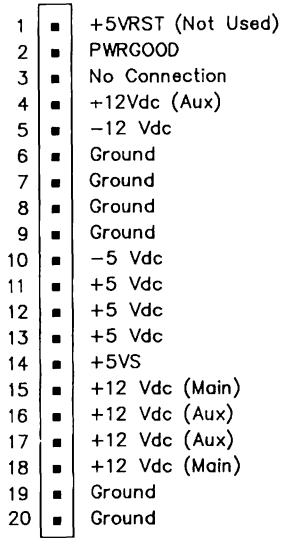


Figure 2-72. J117, Main Power Connector

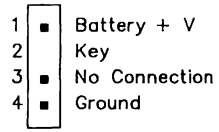


Figure 2-73. J118, Battery Connector

Figure 2-74. J119, Security Lock Connector

2.20 COMPONENT LAYOUTS AND SCHEMATICS

Figure 2-75 shows the component layout for the 12-MHz COMPAQ DESKPRO 286 system board. Figure 2-76 shows the schematics for this system board. Compaq Computer Corporation does not guarantee the accuracy of the component layout or the schematics. They are provided to aid in a general understanding of the system operation.

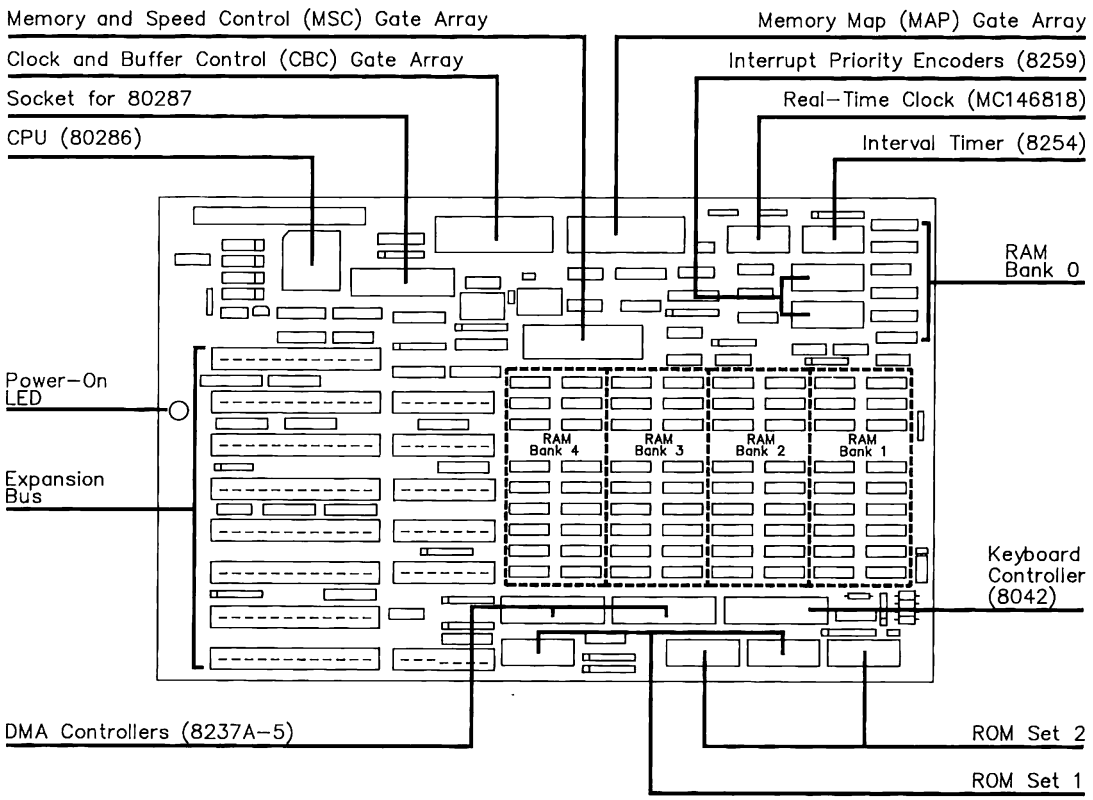


Figure 2-75. The 12-MHz COMPAQ DESKPRO 286 System Board Component Layout

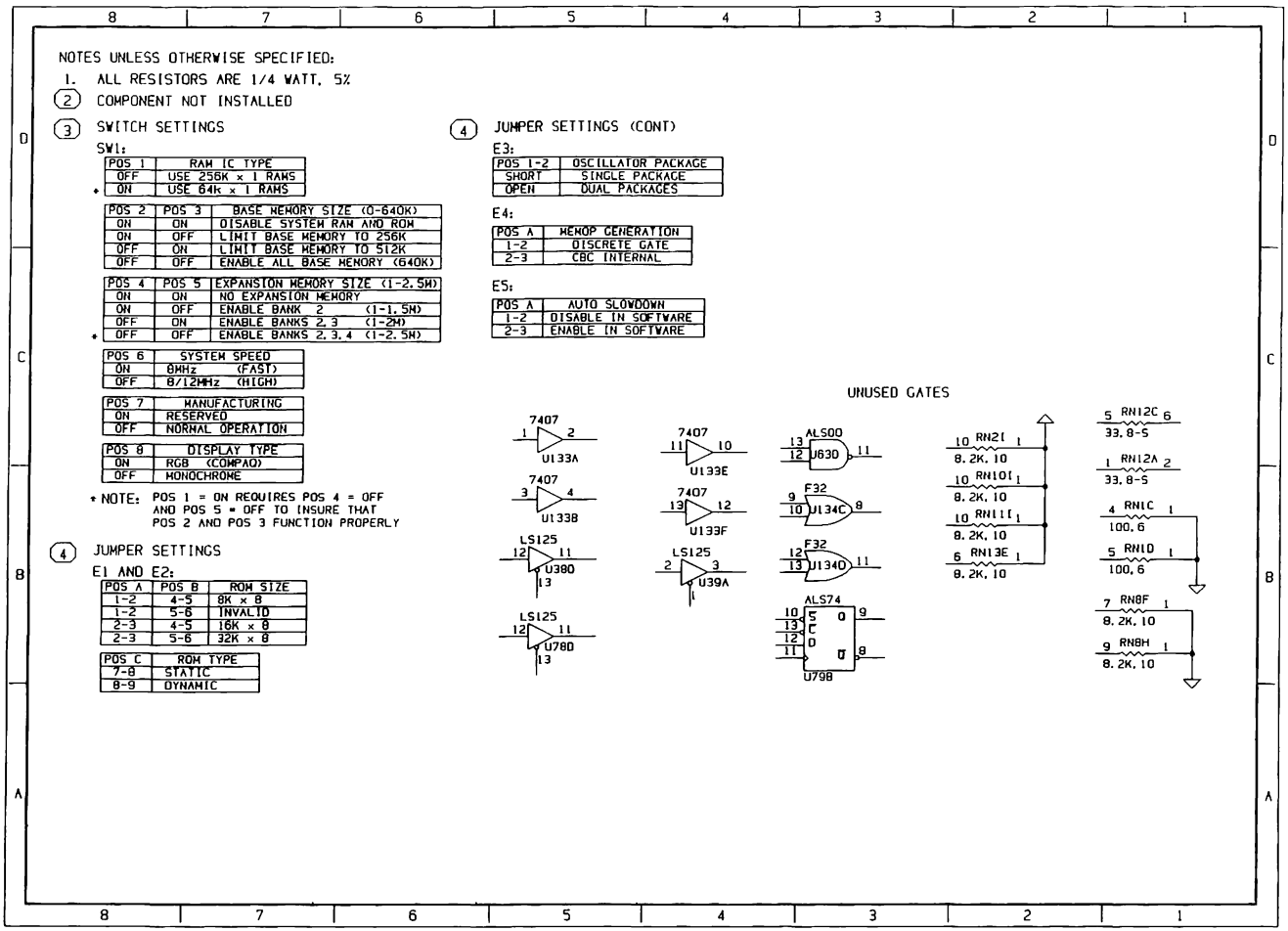


Figure 2-76. The 12 MHz COMPAQ DESKPRO 286 System Board Schematics (Page 1 of 19)

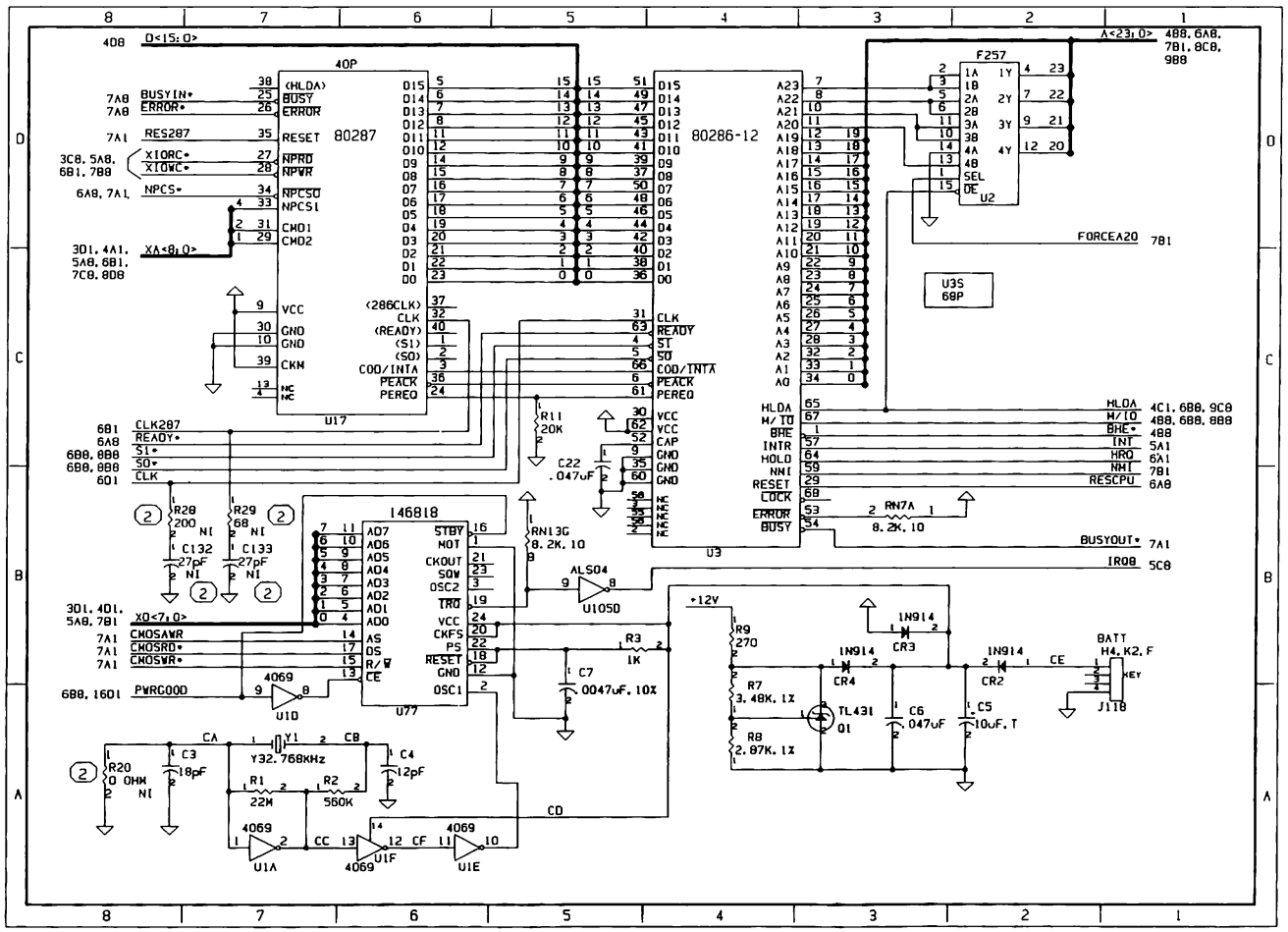


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 2 of 19)

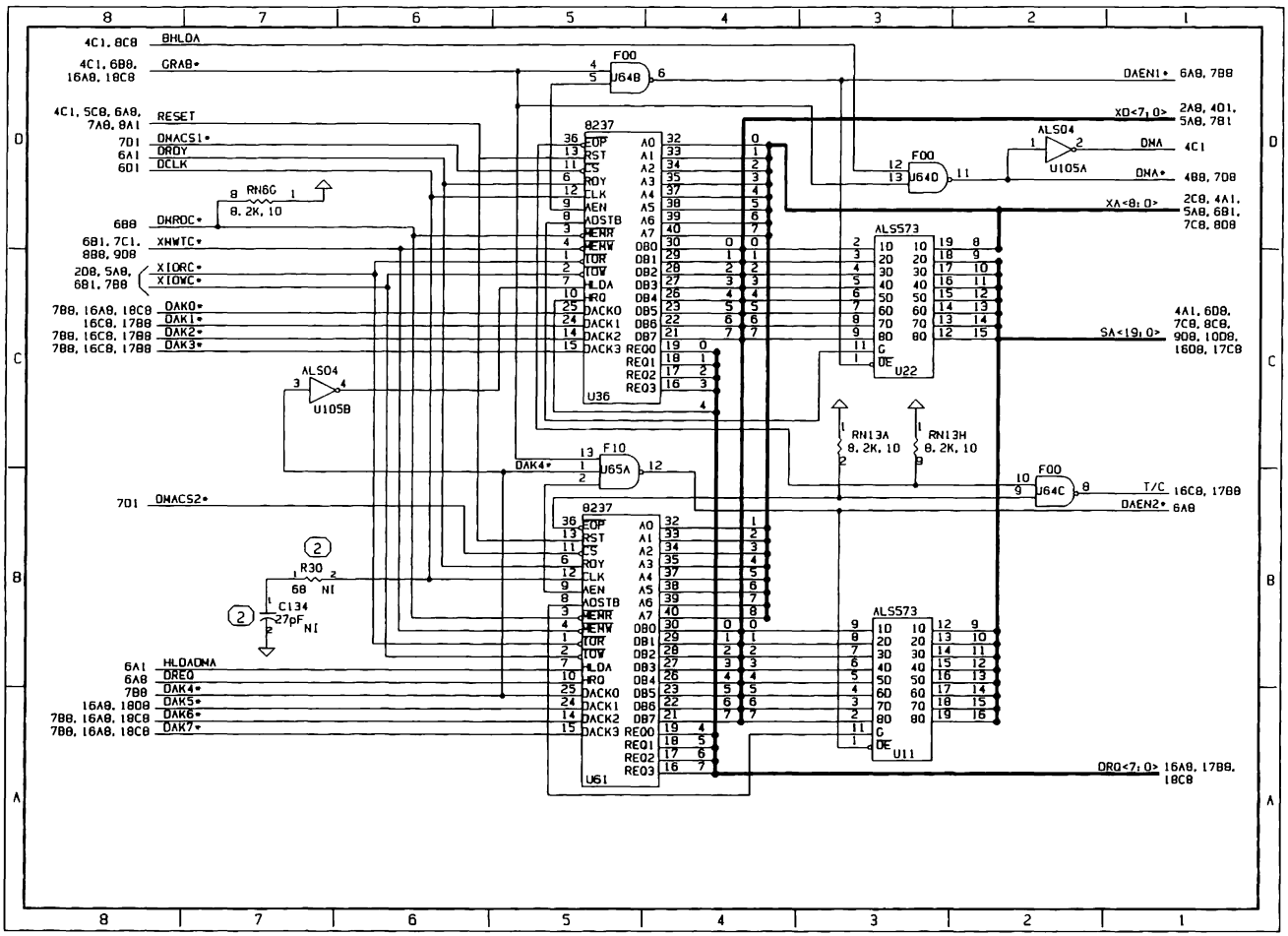


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 3 of 19)

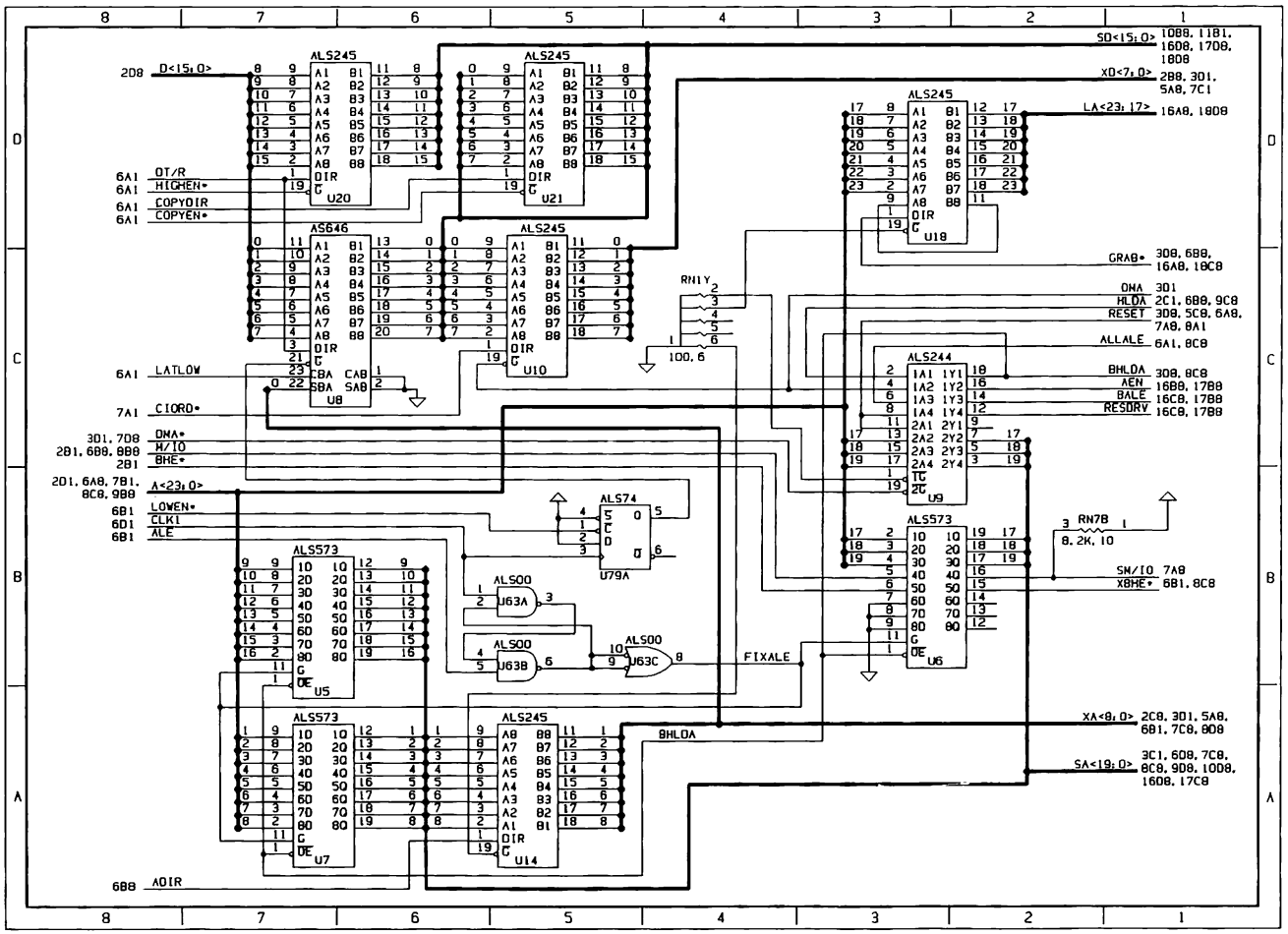


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 4 of 19)

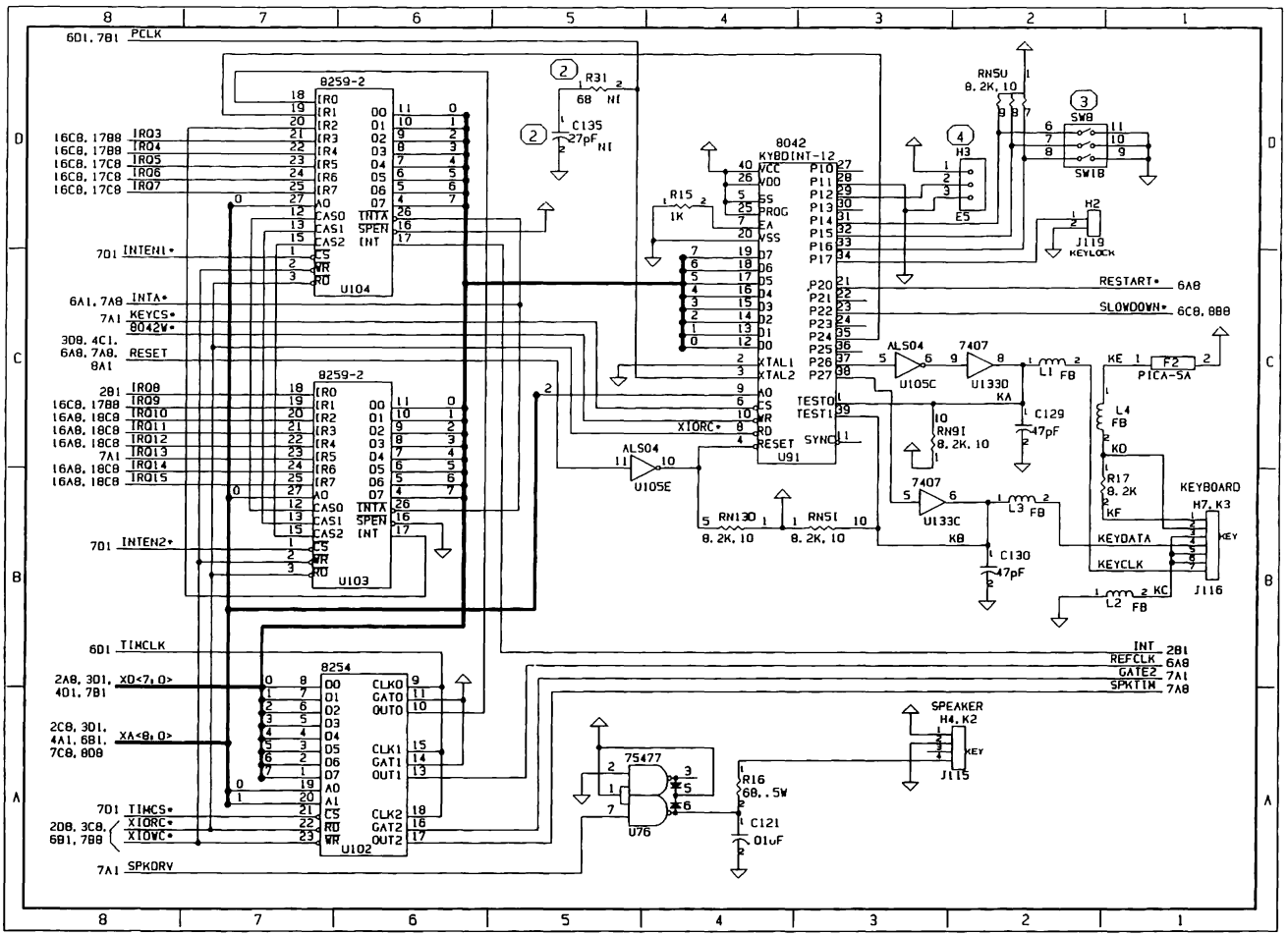


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 5 of 19)

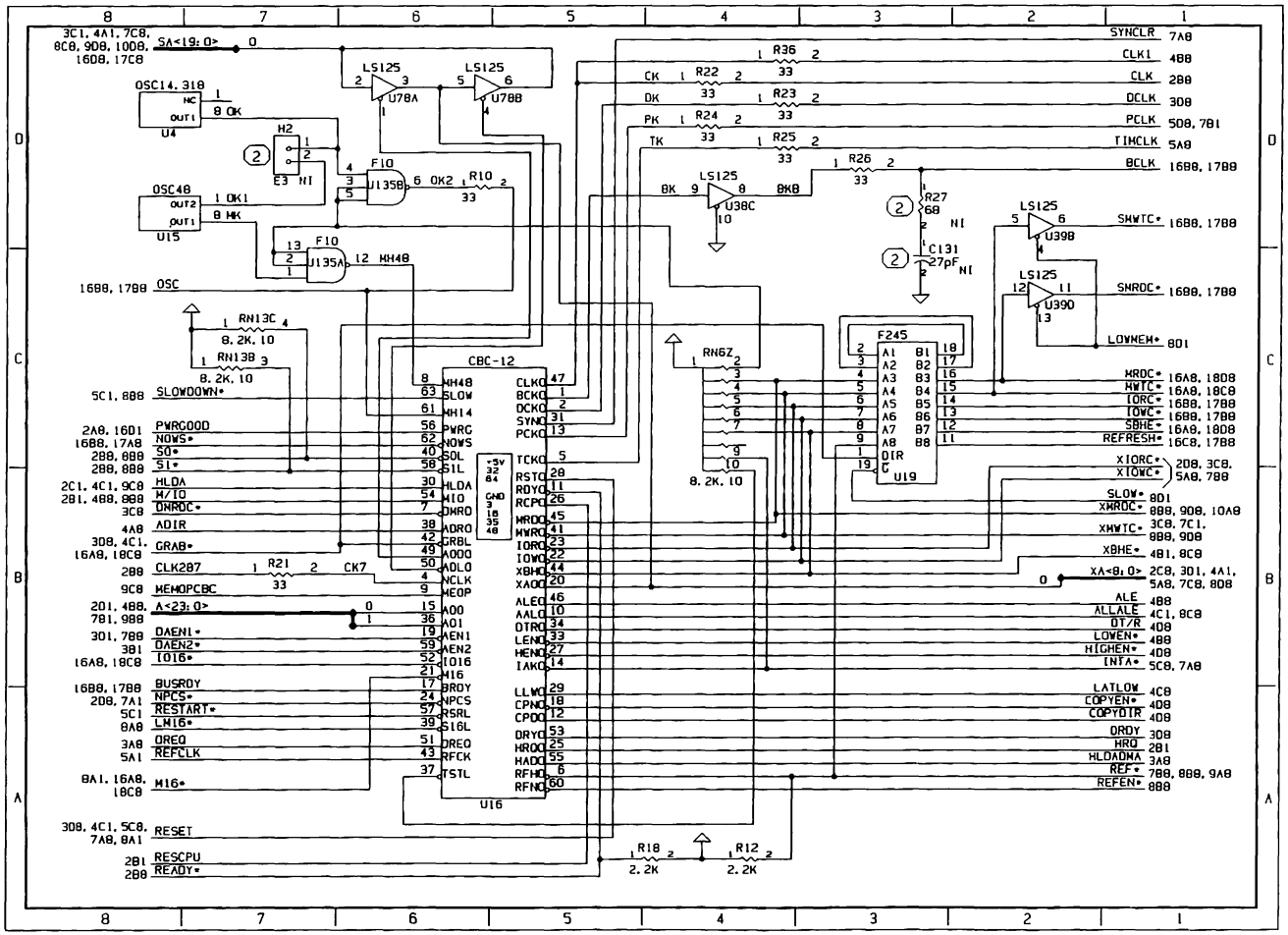


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 6 of 19)

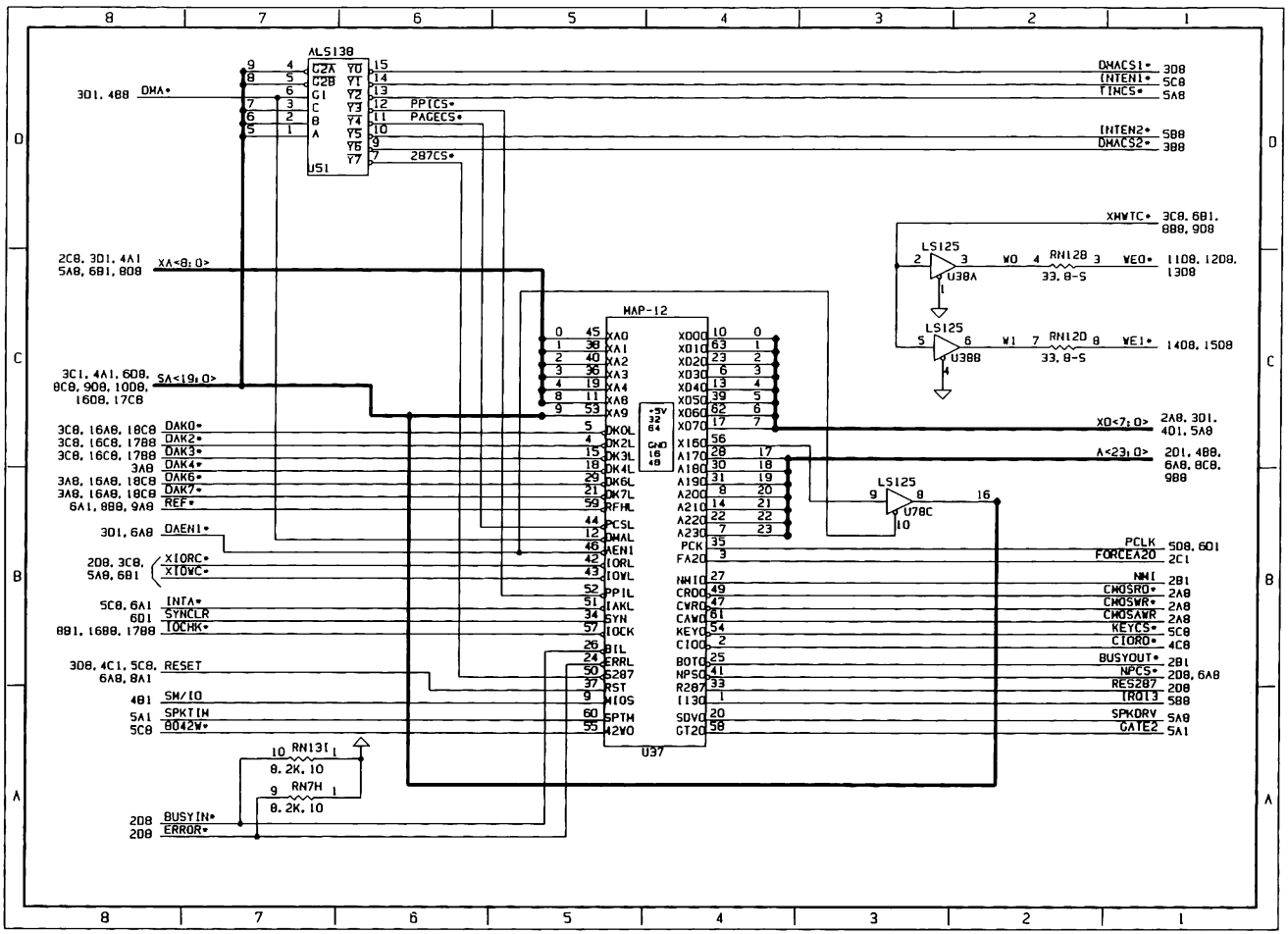


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 7 of 19)

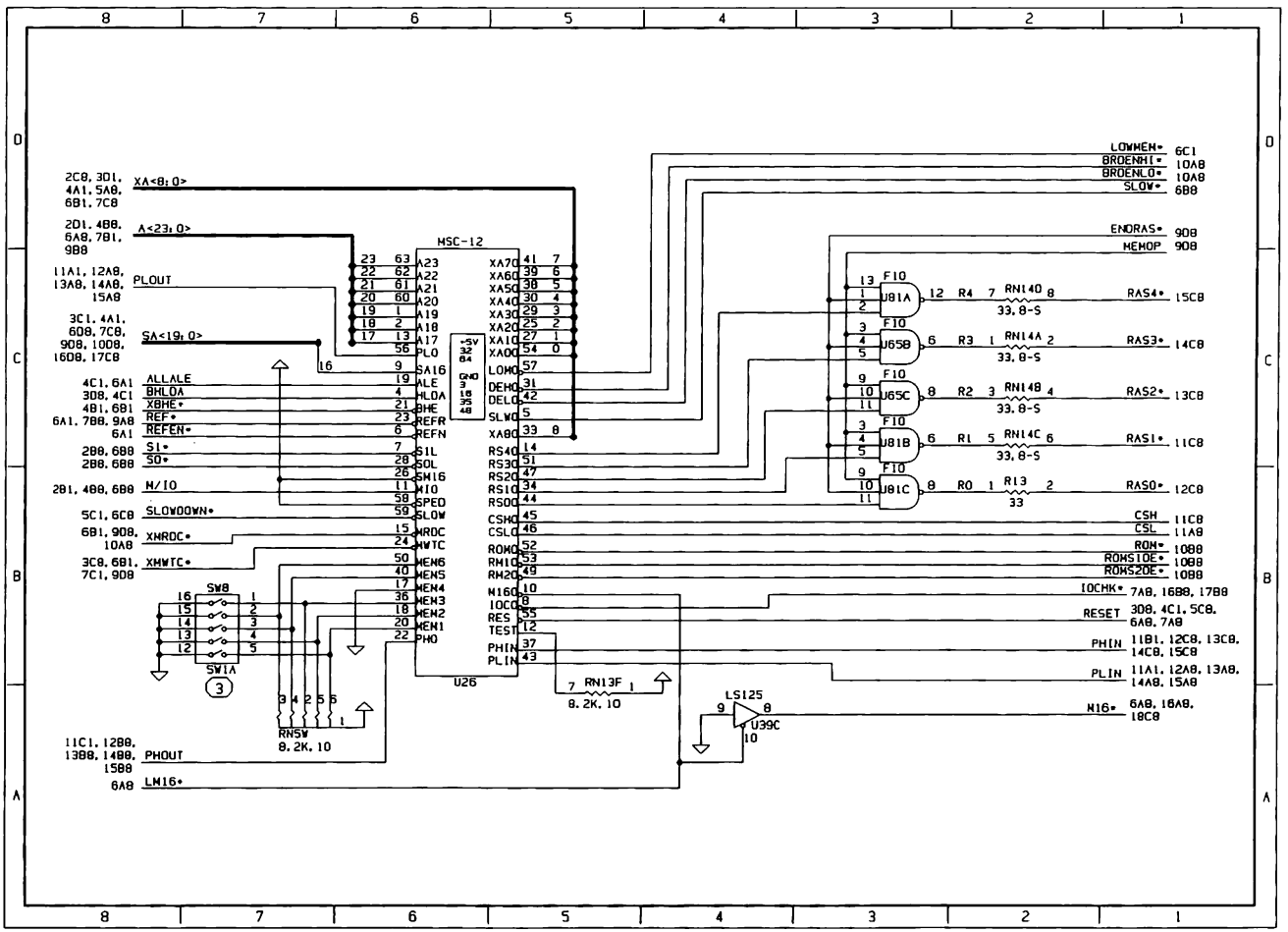


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 8 of 19)

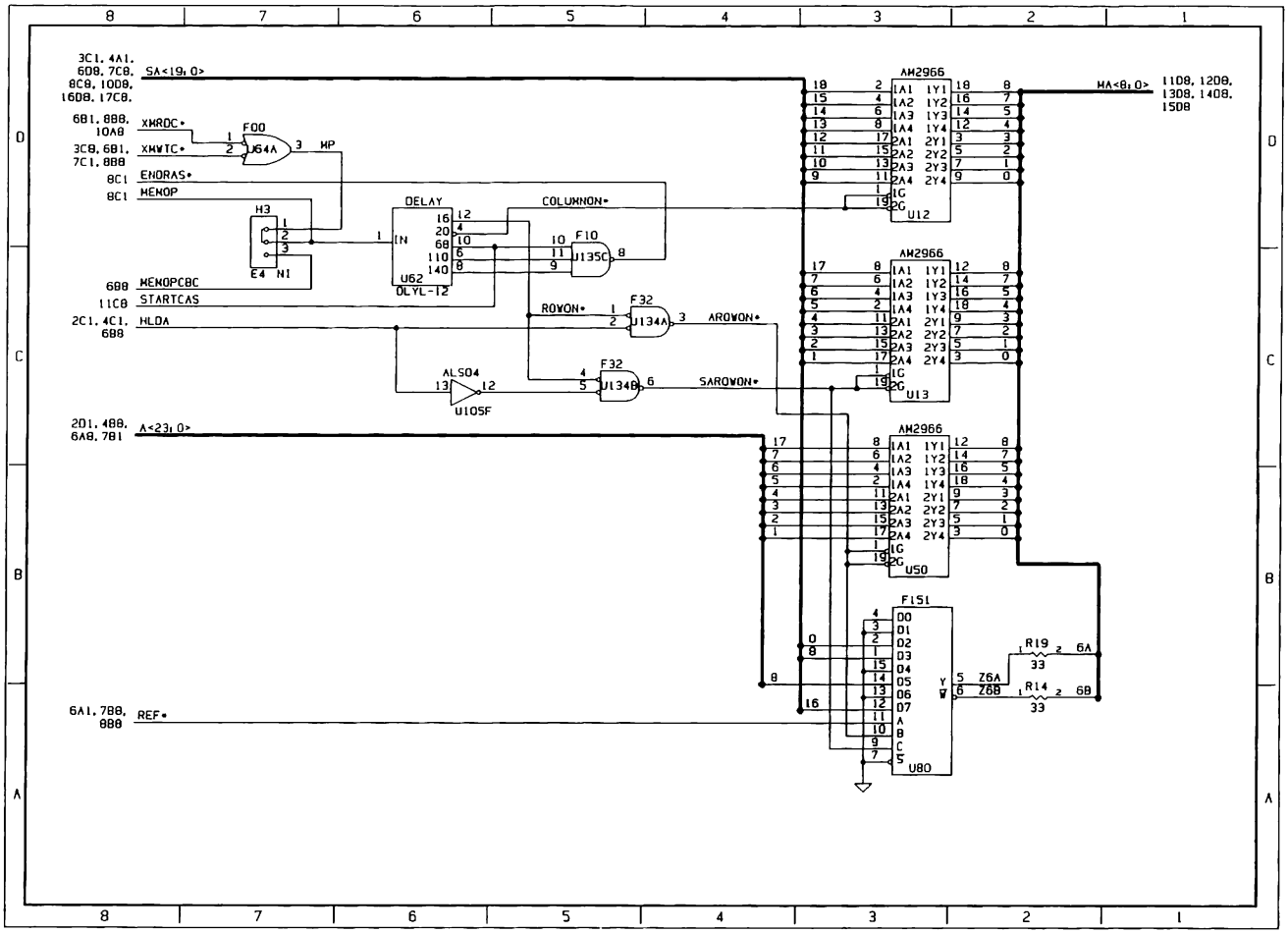


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 9 of 19)

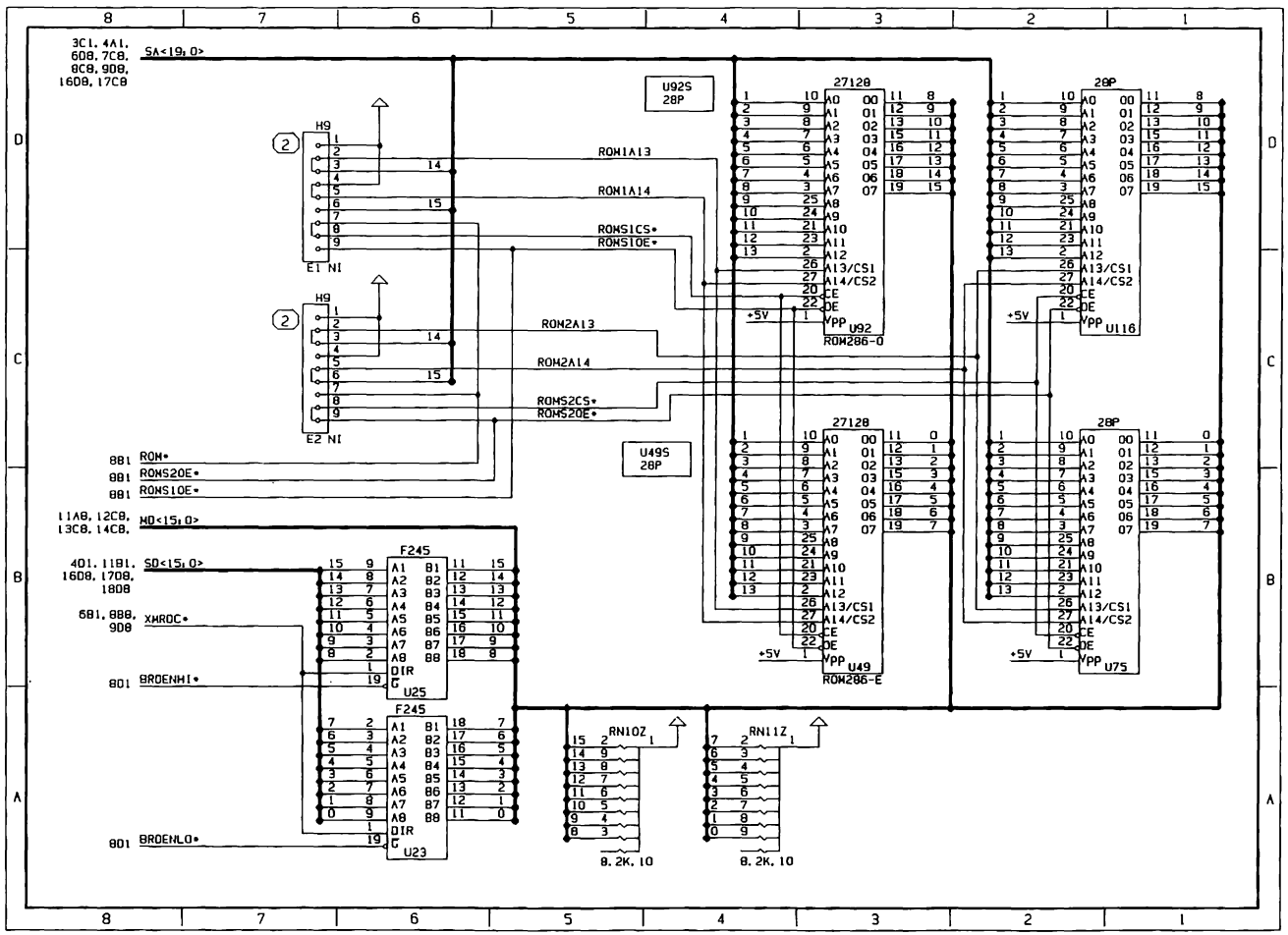


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 10 of 19)

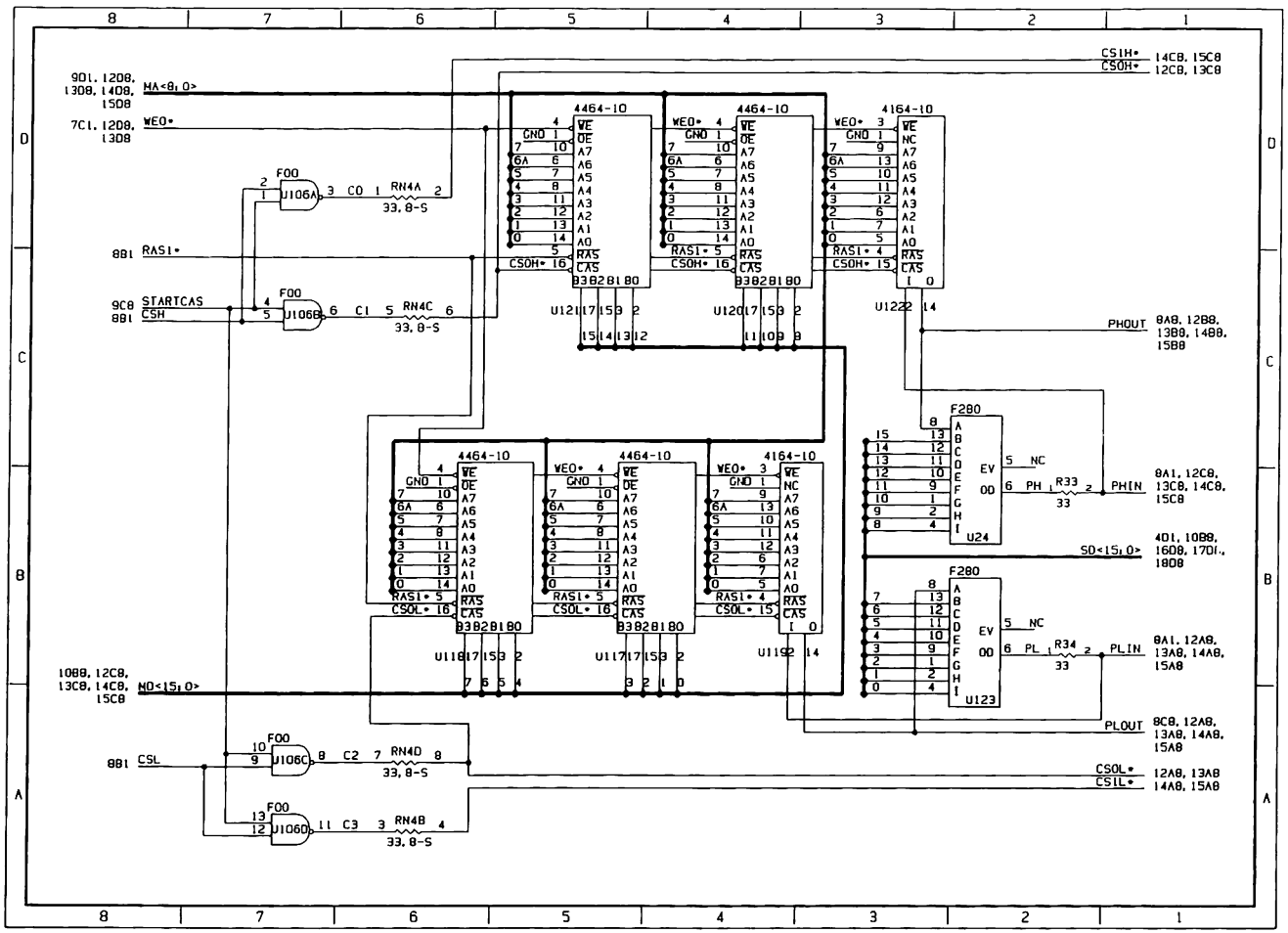


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 11 of 19)

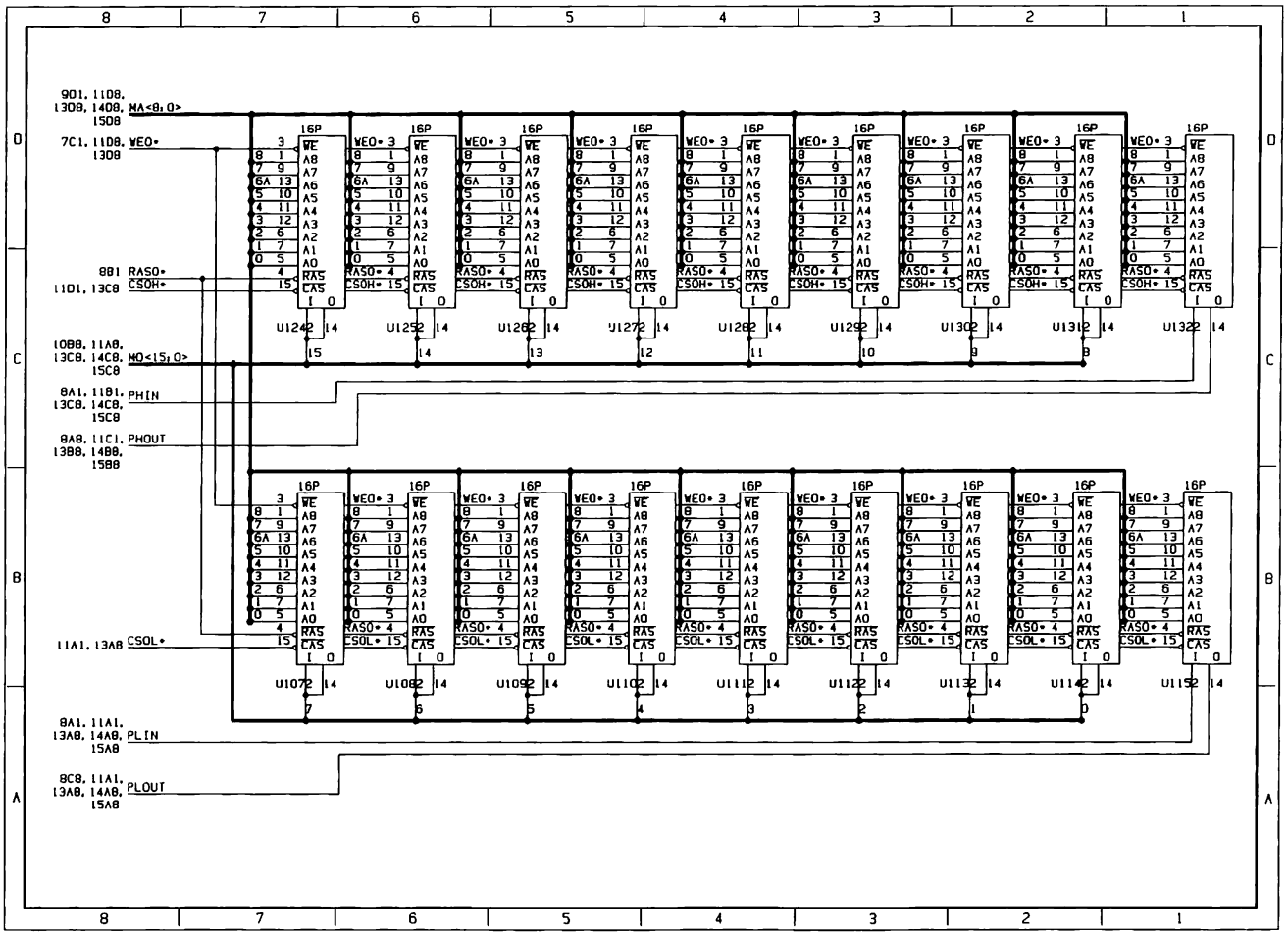


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 12 of 19)

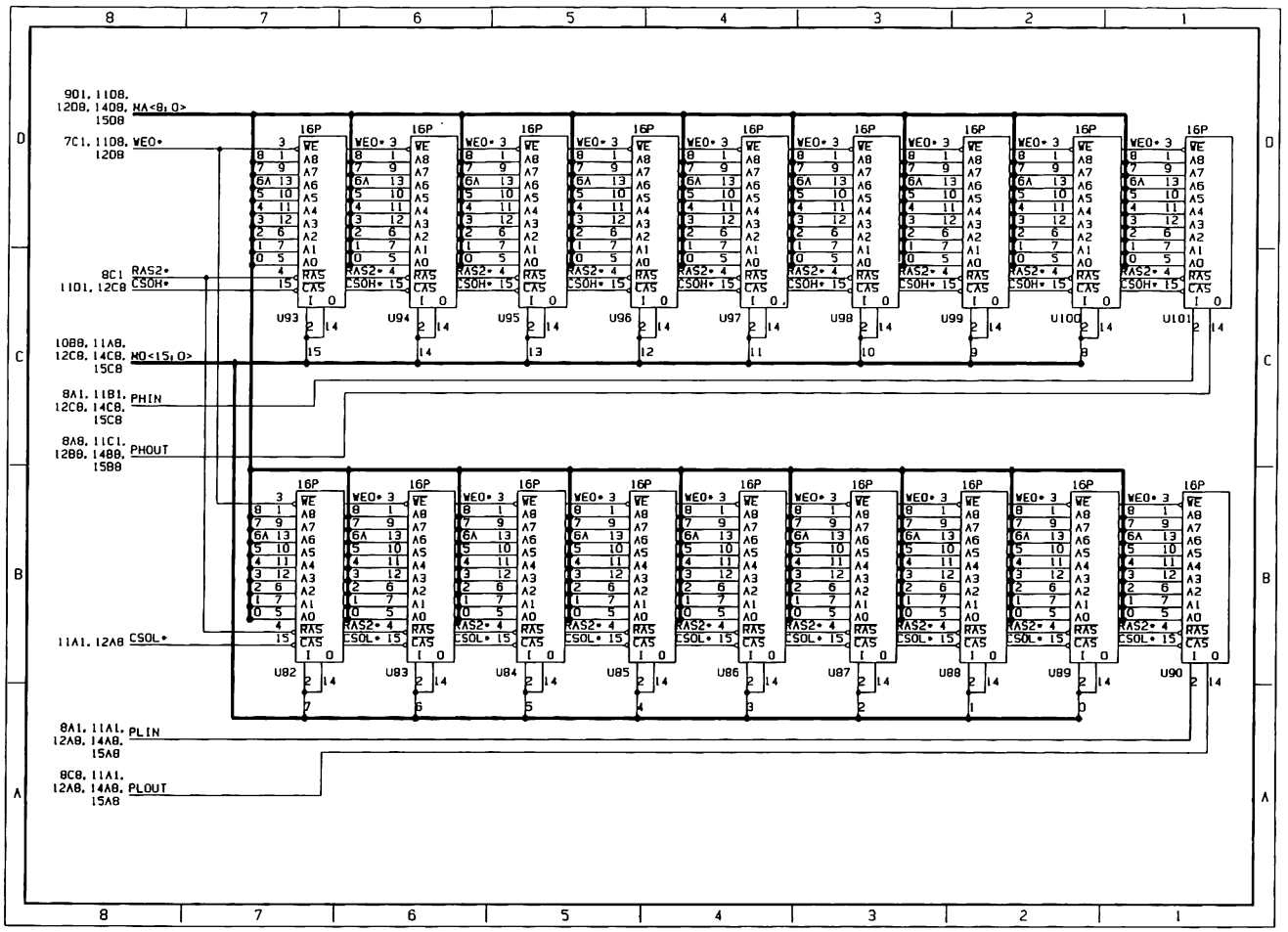


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 13 of 19)

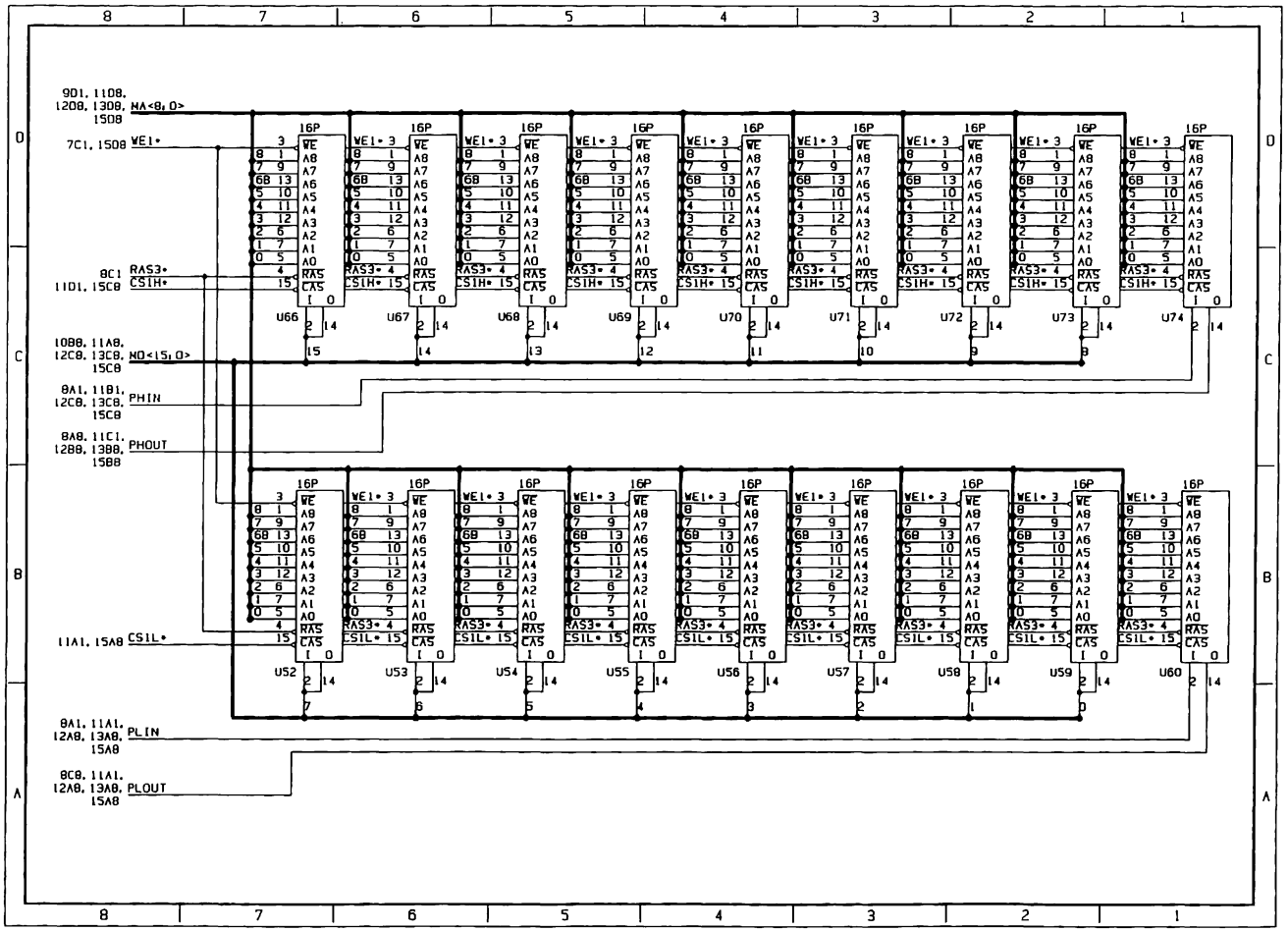


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 14 of 19)

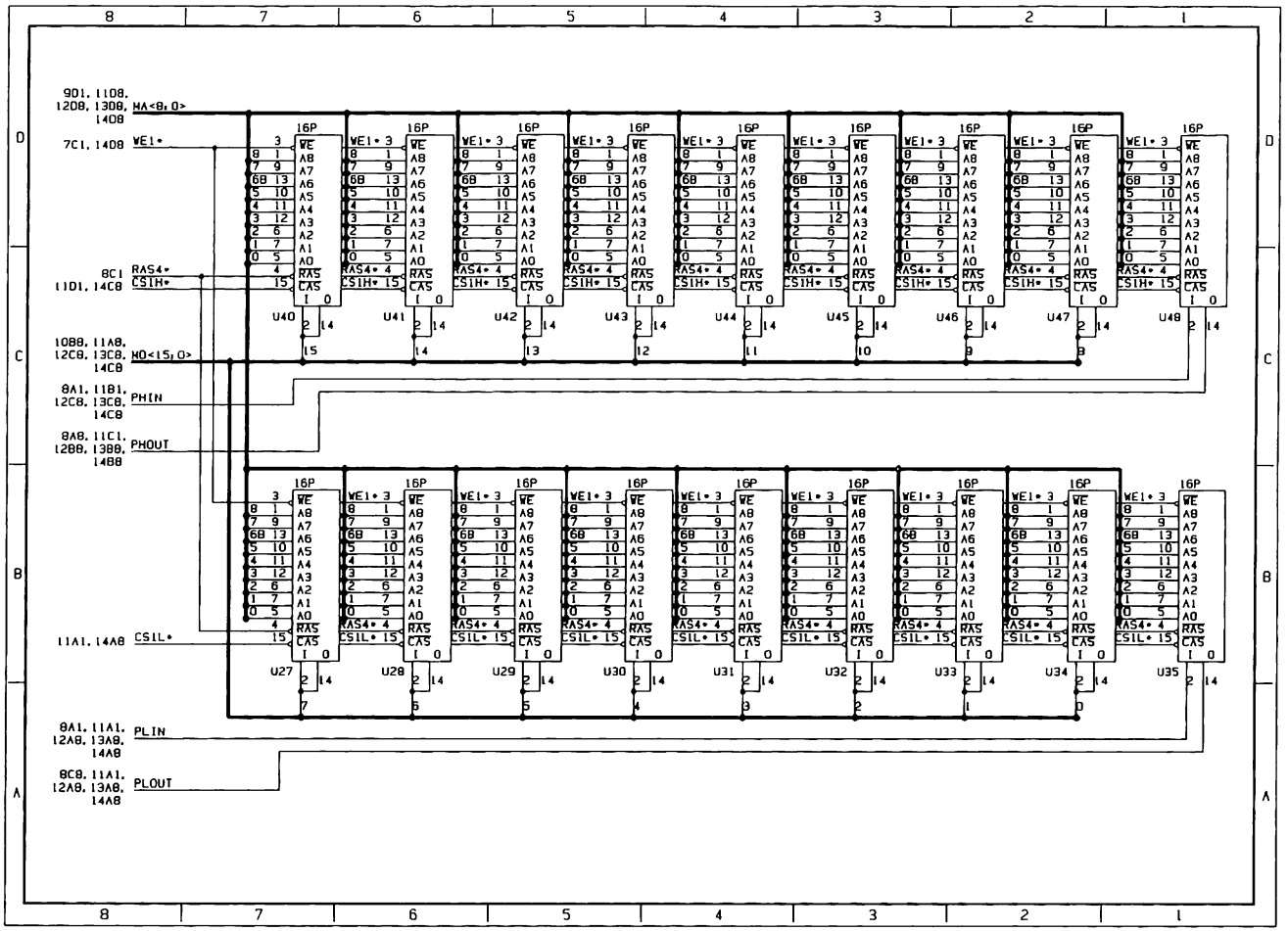


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 15 of 19)

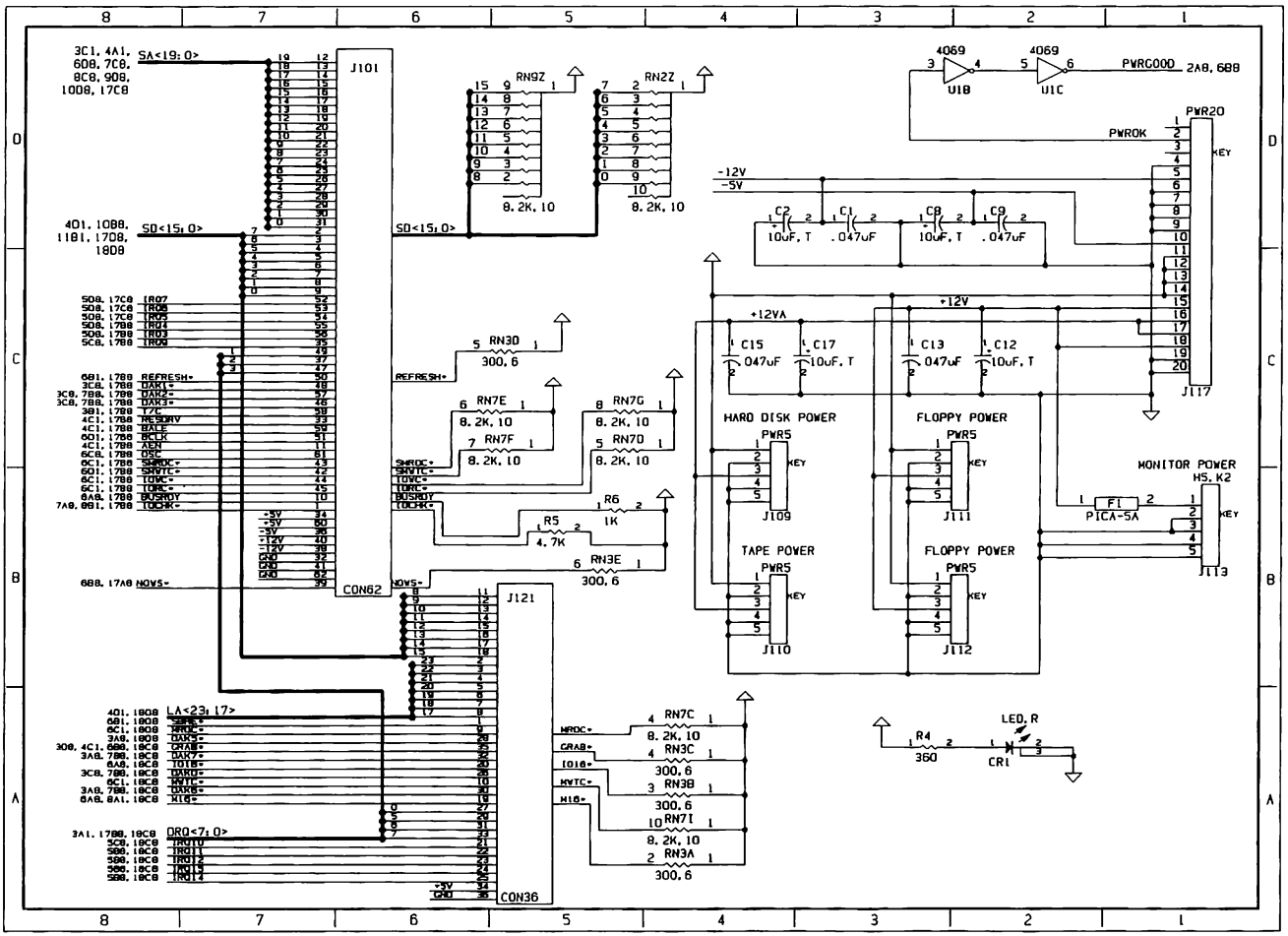


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 16 of 19)

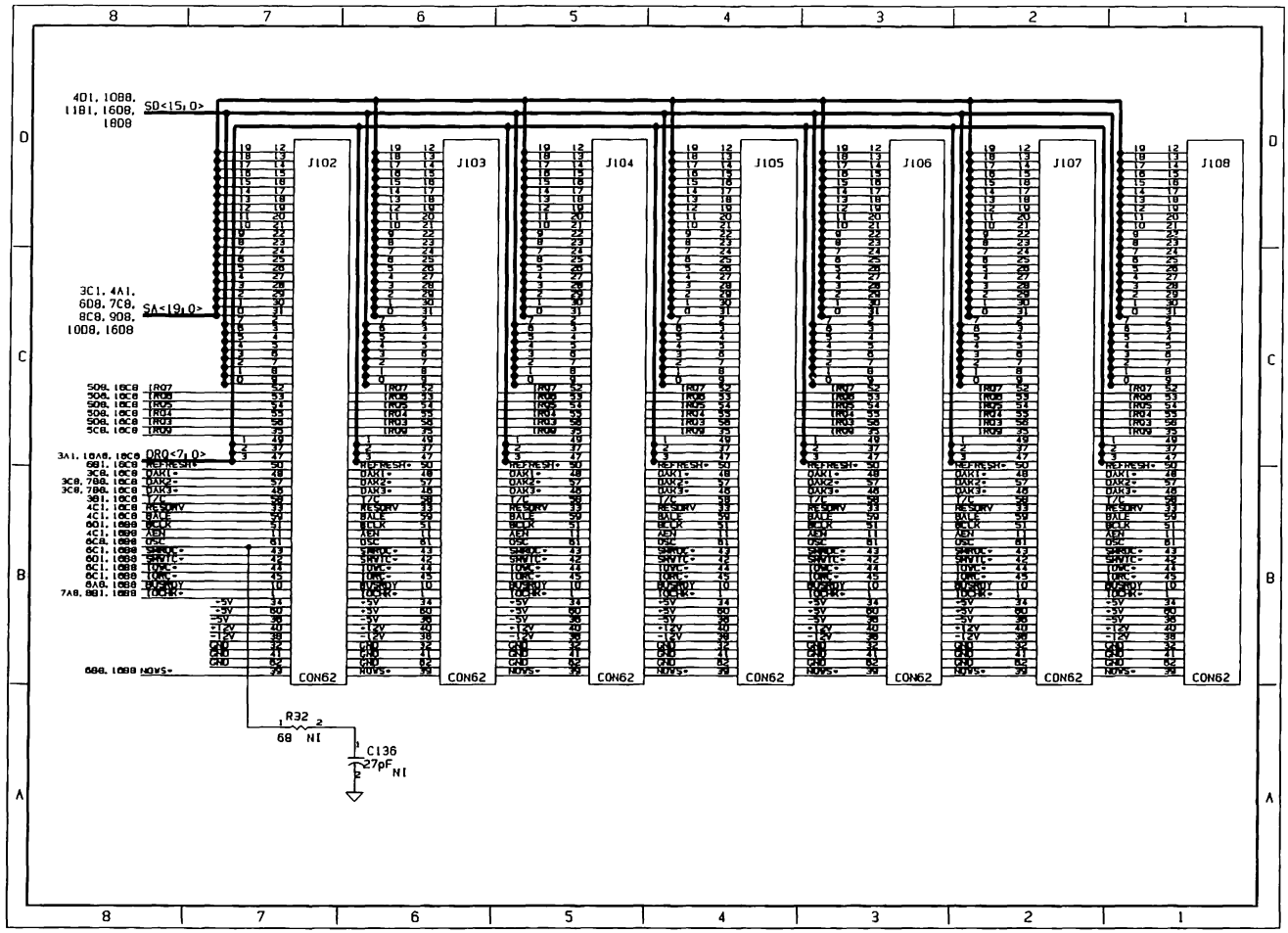


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 17 of 19)

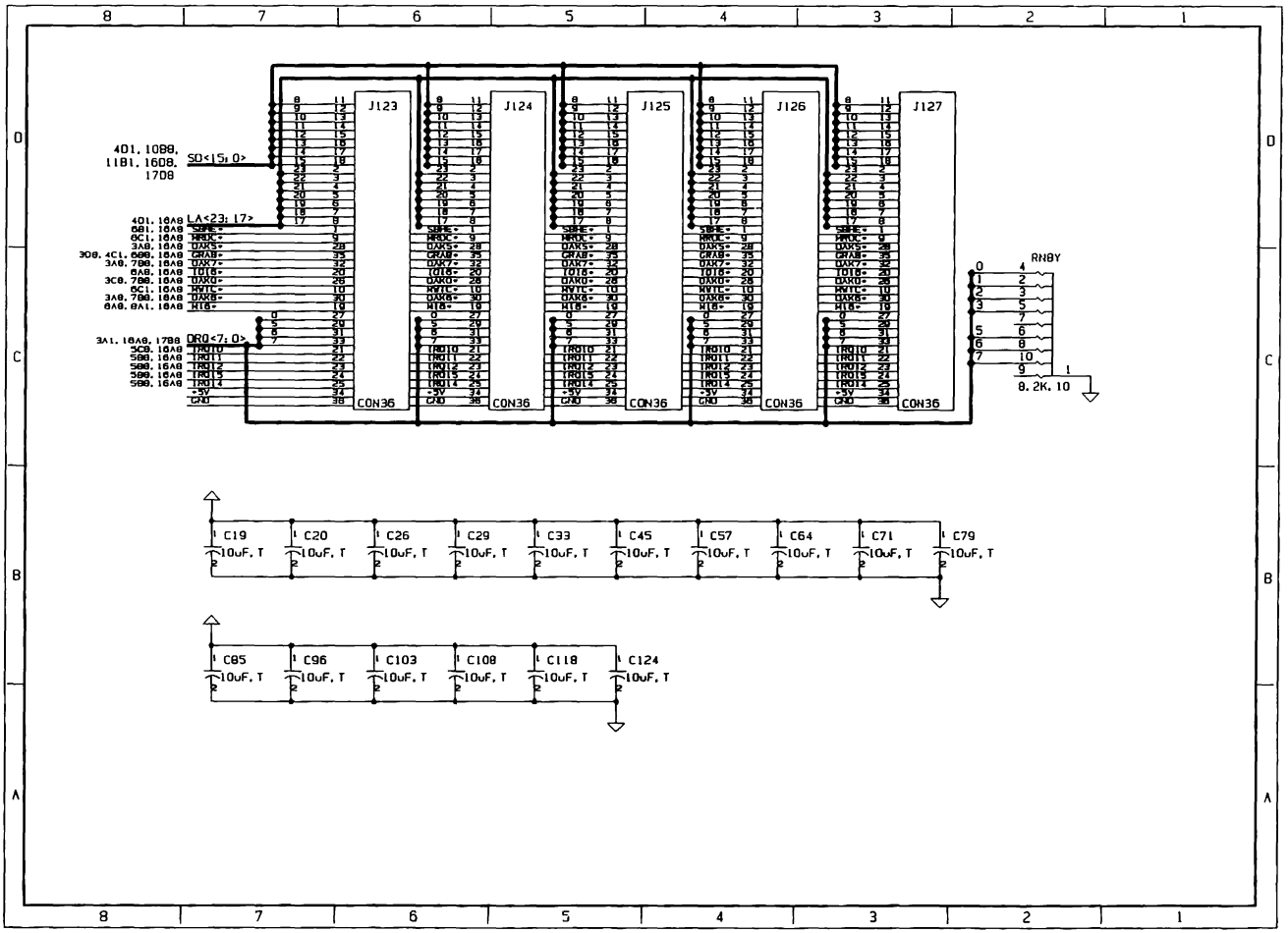


Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 18 of 19)

Figure 2-76. The 12 MHz DESKPRO 286 System Board Schematics (Page 19 of 19)

Chapter 3

COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD

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3.1 INTRODUCTION

The COMPAQ DESKPRO 286® Version 1 System Memory Board is required for use with the COMPAQ DESKPRO 286 Version 1 System Board. The System Memory Board provides system memory, ROM and RAM. Memory address decoding and memory support functions are described in Chapter 2, SYSTEM BOARD.

There are three versions of the COMPAQ DESKPRO 286 System Memory Board. All three boards are functionally equivalent. Version 1 can be distinguished from Versions 2 and 3 by component layout (see Figures 3-1 and 3-2). Versions 2 and 3 have the same component layout, but they have different assembly numbers. (See Figure 3-2 for location of assembly number). Version 2 has assembly number 000178-XXX and Version 3 has assembly number 000382-XXX.

Figures 3-1 and 3-2 show the component layout of the COMPAQ DESKPRO 286 System Memory Boards. Figure 3-3 shows the functional block diagram.

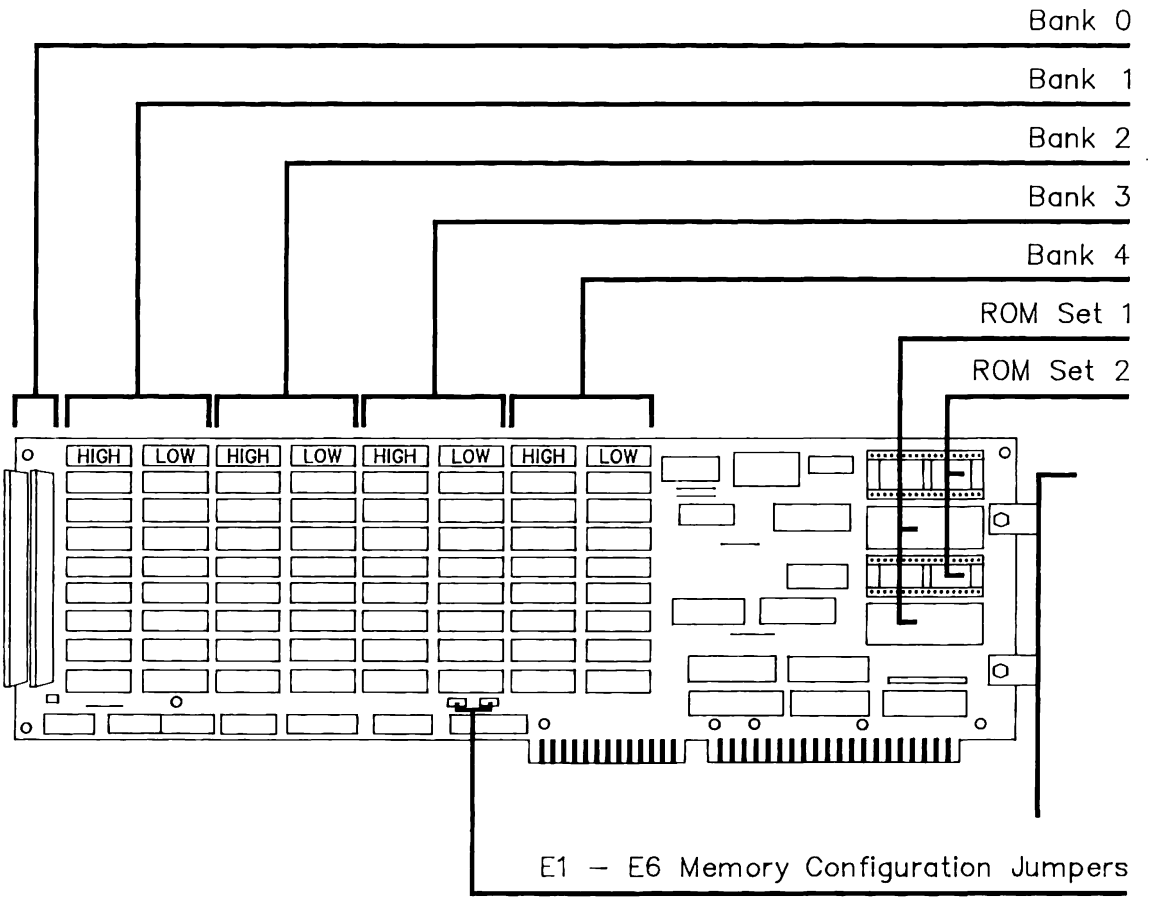


Figure 3-1. COMPAQ DESKPRO 286 System Memory Board Version 1 Component Layout

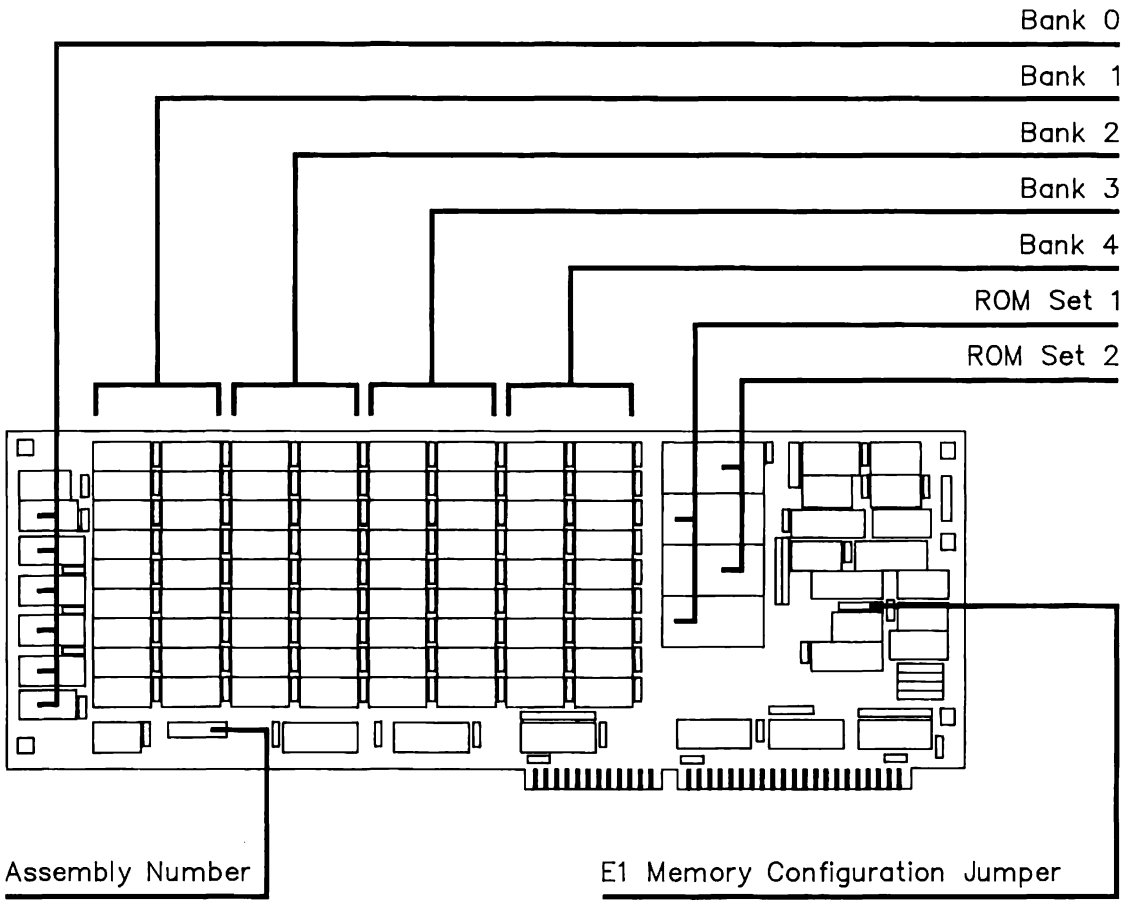


Figure 3-2. COMPAQ DESKPRO 286 System Memory Board Version 2 and Version 3 Component Layout

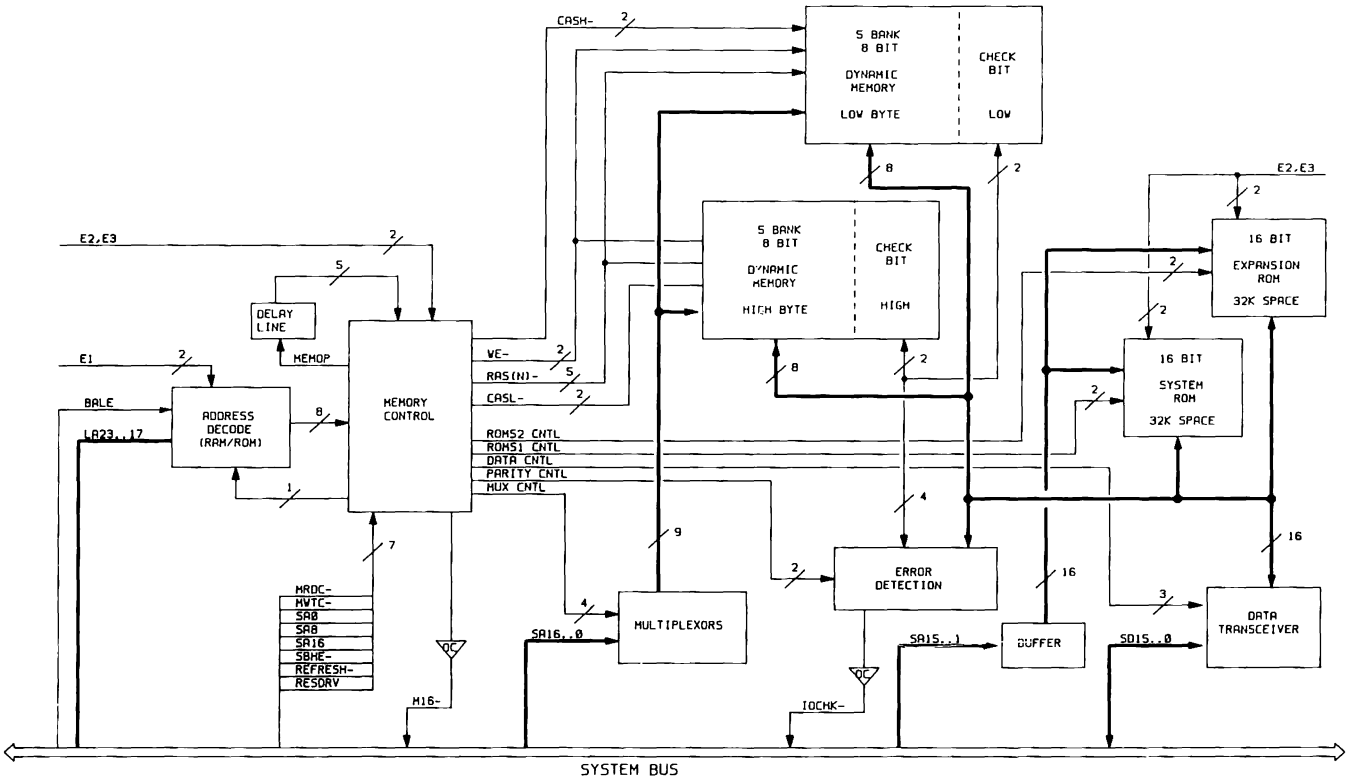


Figure 3-3. COMPAQ DESKPRO 286 System Memory Board Functional Block Diagram

3.2 COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD RAM

NOTE: Memory address decoding and memory support are explained in Chapter 2.

The COMPAQ DESKPRO 286 System Memory Board has 128 Kbyte of RAM soldered in the first bank (Bank 0). The four remaining banks (Banks 1 through 4) are socketed so that either 64K x 1-bit or 256K x 1-bit RAM chips may be used. Memory must be expanded in full-bank increments (18 RAM chips) in contiguous and ascending order, using the same type of dynamic RAM (DRAM) devices.

Tables 3-1, 3-2, and 3-3 show the possible memory configurations and the corresponding jumper settings and address ranges for Versions 1, 2, and 3 of the System Memory Board respectively.

Table 3-1. Memory Configurations and Corresponding Jumper Settings Version 1

Jumper	Setting	Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
E1-E2	E5-E6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
E1-E2	E4-E5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
E2-E3	E5-E6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
E2-E3	E4-E5	0-640 KB	256 KB	128 KB	512 KB	(512 KB)	(512 KB)	(512 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

Table 3-2. Memory Configurations and Corresponding Jumper Settings Version 2

E1 Jumper Setting		Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
1-2	5-6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
1-2	4-5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
2-3	5-6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
2-3	4-5	0-640 KB	256 KB	128 KB	512 KB	(512 KB)	(512 KB)	(512 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

Table 3-3. Memory Configurations and Corresponding Jumper Settings Version 3

E1 Jumper Setting		Address Range	RAM Size	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4
1-2	5-6	0-640 KB	64 KB	128 KB	128 KB	128 KB	128 KB	128 KB
1-2	4-5	0-512 KB	64 KB	128 KB	128 KB	128 KB	128 KB	(128 KB)
2-3	5-6	0-640 KB; 1-2.5MB	256 KB	128 KB	512 KB	512 KB	512 KB	512 KB
2-3	4-5	0-256 KB		128 KB	128 KB	(128 KB)	(128 KB)	(128 KB)

Notes: 1. All memory sizes are in Kbytes unless otherwise noted.
2. Use the instructions that come with the COMPAQ memory option kit to properly configure your memory board.
3. Memory banks shown in parentheses ( ) are not enabled when the jumpers are set as shown, regardless of whether or not RAM is installed in these banks.

There are five possible memory configurations for the COMPAQ DESKPRO 286 System Memory Board. Configurations 1 through 5 are supported by Versions 1 and 2. Configurations 1, 2, 3, and 5 are supported by Version 3.

1. 0-640 KB using 64K x 1-bit DRAM chips
2. 0-512 KB using 64K x 1-bit DRAM chips
3. 0-2.176 MB using 256K x 1-bit DRAM chips (0-640 KB plus 512 KB-1536 KB)
4. 0-640 KB using 256K x 1-bit DRAM chips
5. 0-256 KB using 64K x 1-bit DRAM chips

In every configuration, the lowest 128 Kbytes of RAM is permanently installed as Bank 0. Figure 3-4 and 3-5 shows the relationship between the memory map and the installed RAM banks for each configuration.

Configurations 2 and 5 are for use with certain hardware and software packages that require system memory to be limited. These configurations disable the specified address ranges without requiring removal of the unused RAM.

The system memory board uses COMPAQ-approved 64K x 1-bit or 256K x 1-bit DRAMs with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.)

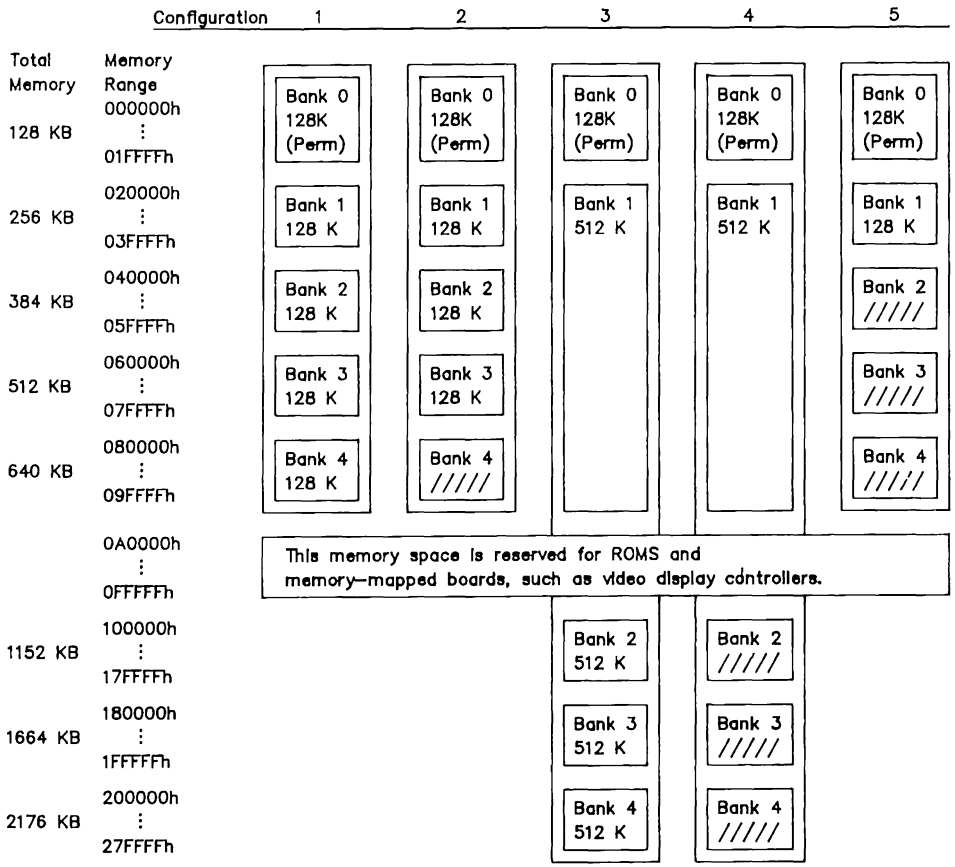


Figure 3-4. COMPAQ DESKPRO 286 (with Version 1 System Board) Memory Configurations

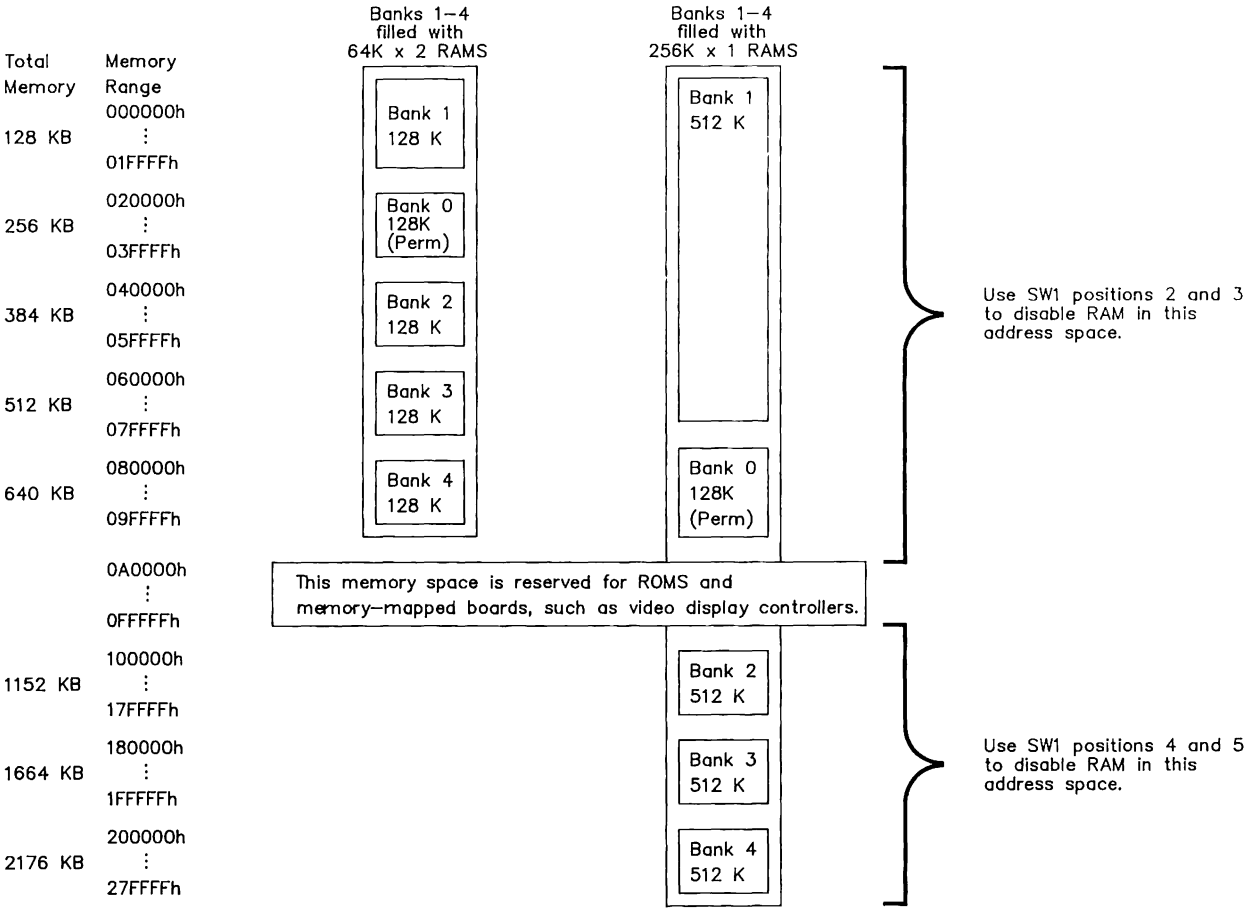


Figure 3-5. COMPAQ DESKPRO 286 (with Version 2 System Board) Memory Configurations

3.3 COMPAQ DESKPRO 286 SYSTEM MEMORY BOARD ROM

The COMPAQ DESKPRO System Memory Board has four 28-pin sockets for ROM or EPROM. The ROM sockets are addressed as two pairs, each 16 bits wide and designated as ROM Set 1 (always present and including address 0FFFF0h or FFFFF0h) and system ROM SET 2 (located in the address space 64 Kbytes below ROM Set 1).

ROM Set 1 controls the initial system operation (resetting and initializing the system). This code is known as the BIOS (Basic Input Output System). Installed in the two ROM Set 1 sockets are 16K x 8 devices, one containing all even bytes and the other containing all odd bytes. The two ROM Set 2 sockets are empty and are provided for future expansion.

ROMs can be, by pairs, either 8K x 8, 16K x 8, or 32K x 8 bits in size and can be either static or dynamic. ROM Set 1 occupies the 64-KB space at address 0F0000h through 0FEFFFh and identically at address FF0000h through FFFFFFh. ROM Set 2 occupies the 64-KB space at address 0E0000h through 0EFFFFh and identically at address FE0000h through FEFFFFh.

When 32K X 8 ROM chips are used, the pair of ROM chips fill the entire 64-Kbyte address space. When 16K x 8 ROM chips are used, the most-significant address bit is not decoded, so the ROM chips are double-mapped into two identical 32-Kbyte sections of the 64-Kbyte address space.

Similarly, when 8K x 8 ROMs are used, the two most-significant address bits are not decoded, so the ROM chips are quadruple-mapped into four identical 16-Kbyte sections of the 64-Kbyte address space.

3.4 JUMPERS

Several jumpers are provided to enable use of a variety of types of ROM for special applications.

Tables 3-4 and 3-5 lists the jumper settings and resulting configuration for each type of ROM.

Table 3-4. Jumper Settings for ROM Sets 1 and 2 - Version 1 System Memory Board

ROM Set 1 Jumper Settings			ROM Type
E7-E8	E10-E11	E13-E14	8Kx8, Static ROM, 250 ns
E8-E9	E10-E11	E13-E14	16Kx8, Static ROM, 250 ns
E7-E8	E11-E12	E13-E14	Invalid
E8-E9	E11-E12	E13-E14	32Kx8, Static ROM, 250 ns
E7-E8	E10-E11	E14-E15	8Kx8, Dynamic ROM, 150 ns
E8-E9	E10-E11	E14-E15	16Kx8, Dynamic ROM, 150 ns
E7-E8	E11-E12	E14-E15	Invalid
E8-E9	E11-E12	E14-E15	32Kx8, Dynamic ROM, 150 ns
ROM Set 2 Jumper Settings			ROM Type
E16-E17	E19-E20	E22-E23	8Kx8, Static ROM, 250 ns
E17-E18	E19-E20	E22-E23	16Kx8, Static ROM, 250 ns
E16-E17	E20-E21	E22-E23	Invalid
E17-E18	E20-E21	E22-E23	32Kx8, Static ROM, 250 ns
E16-E17	E19-E20	E23-E24	8Kx8, Dynamic ROM, 150 ns
E17-E18	E19-E20	E23-E24	16Kx8, Dynamic ROM, 150 ns
E16-E17	E20-E21	E23-E24	Invalid
E17-E18	E20-E21	E23-E24	32Kx8, Dynamic ROM, 150 ns

Table 3-5. Jumper Settings for ROM Sets 1 and 2 - Version 2 and 3 System Memory Board

ROM Set 1 - E2 ROM Set 2 - E3 Jumper Settings			ROM Type
1-2	4-5	7-8	8Kx8, Static ROM, 250 ns
2-3	4-5	7-8	16Kx8, Static ROM, 250 ns
1-2	5-6	7-8	Invalid
2-3	5-6	7-8	32Kx8, Static ROM, 250 ns
1-2	4-5	8-9	8Kx8, Dynamic ROM, 150 ns
2-3	4-5	8-9	16Kx8, Dynamic ROM, 150 ns
1-2	5-6	8-9	Invalid
2-3	5-6	8-9	32Kx8, Dynamic ROM, 150 ns

There are no jumper headers installed. The jumpers are etched on the solder side (bottom) of the board in the following configurations:

Version 1
ROM Set 1: 16K x 8 Static ROM (E8-E9, E10-E11, E13-E14)
ROM Set 2: 32K x 8 Dynamic ROM (E17-E18,E20-E21, E23-E24)

Version 2
ROM Set 1: 16K x 8 Static ROM (E1: 2-3, 4-5, 7-8)
ROM Set 2: 32K x 8 Dynamic ROM (E2: 2-3, 5-6, 8-9)

Changing the jumper settings requires cutting the conductor on the solder side (bottom) of the board to disconnect any unwanted jumpers, then soldering the wire(s) to jumpers as desired.

NOTE: Modifying these jumpers invalidates the COMPAQ warranty for this board.

3.5 SCHEMATICS

Figure 3-6 shows the schematics for the COMPAQ DESKPRO 286 System Memory Board Version 1. Figure 3-7 shows the schematics for the COMPAQ DESKPRO 286 System Memory Board Versions 2 and 3. Versions 2 and 3 have the same schematics, only the PALS are different. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

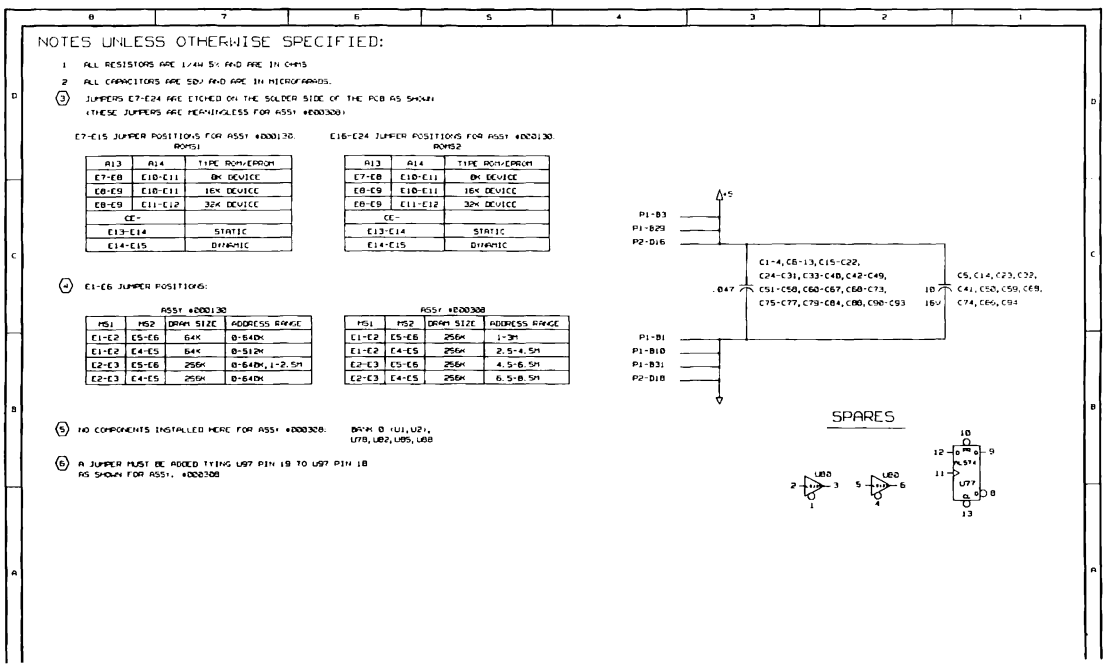


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Version 1 Schematics (Page 1 of 5)

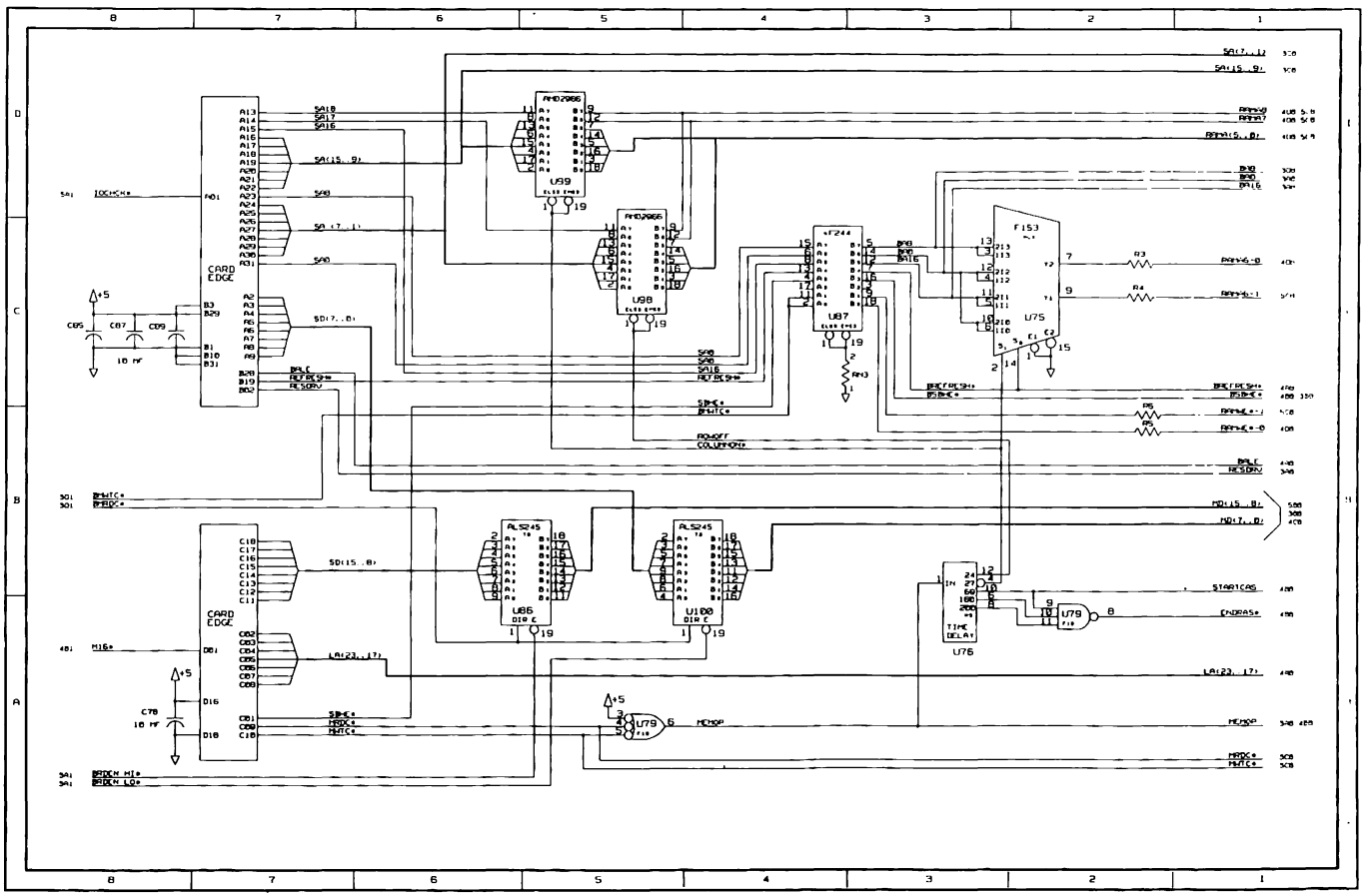


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 2 of 5)

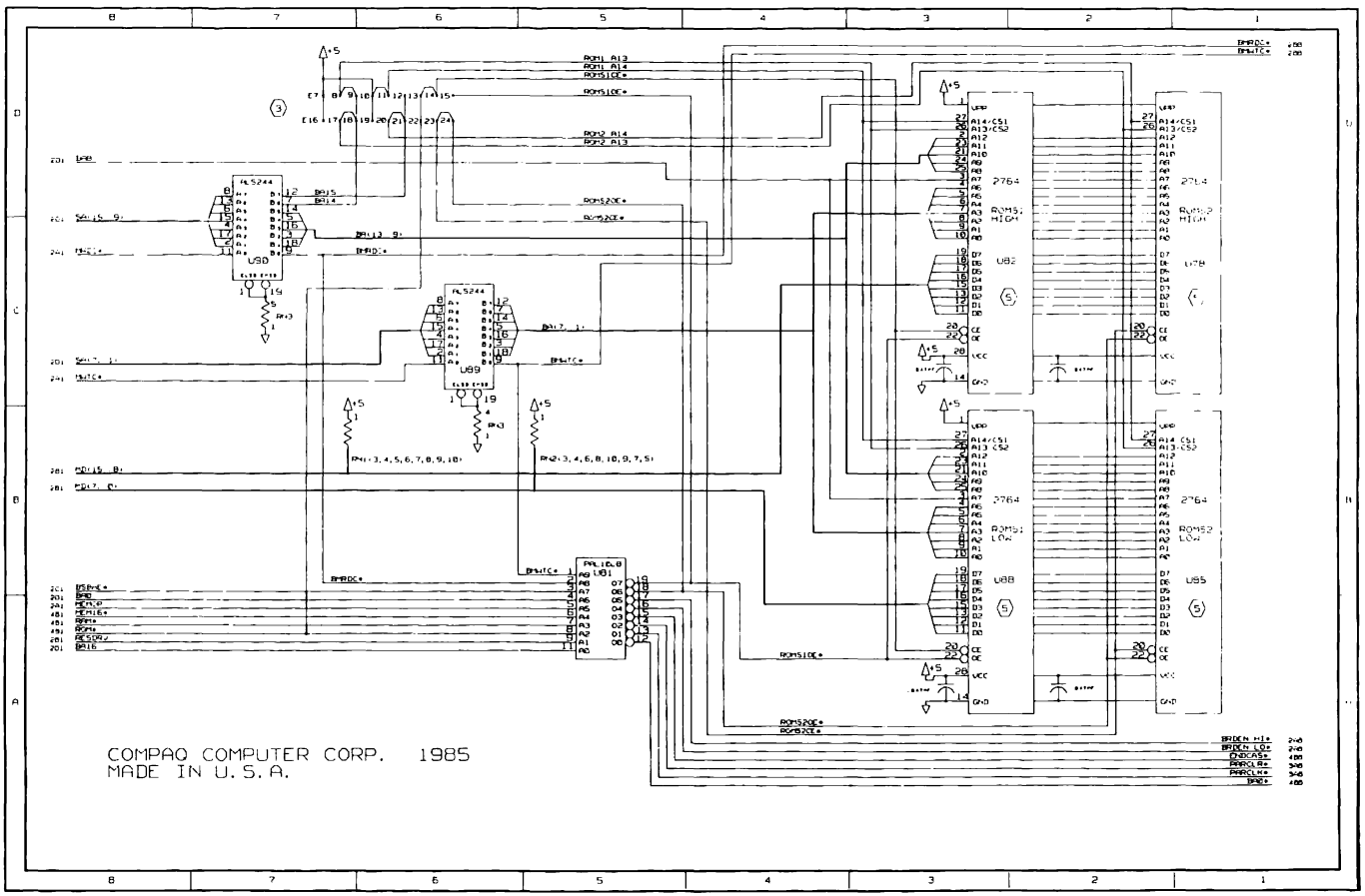


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 3 of 5)

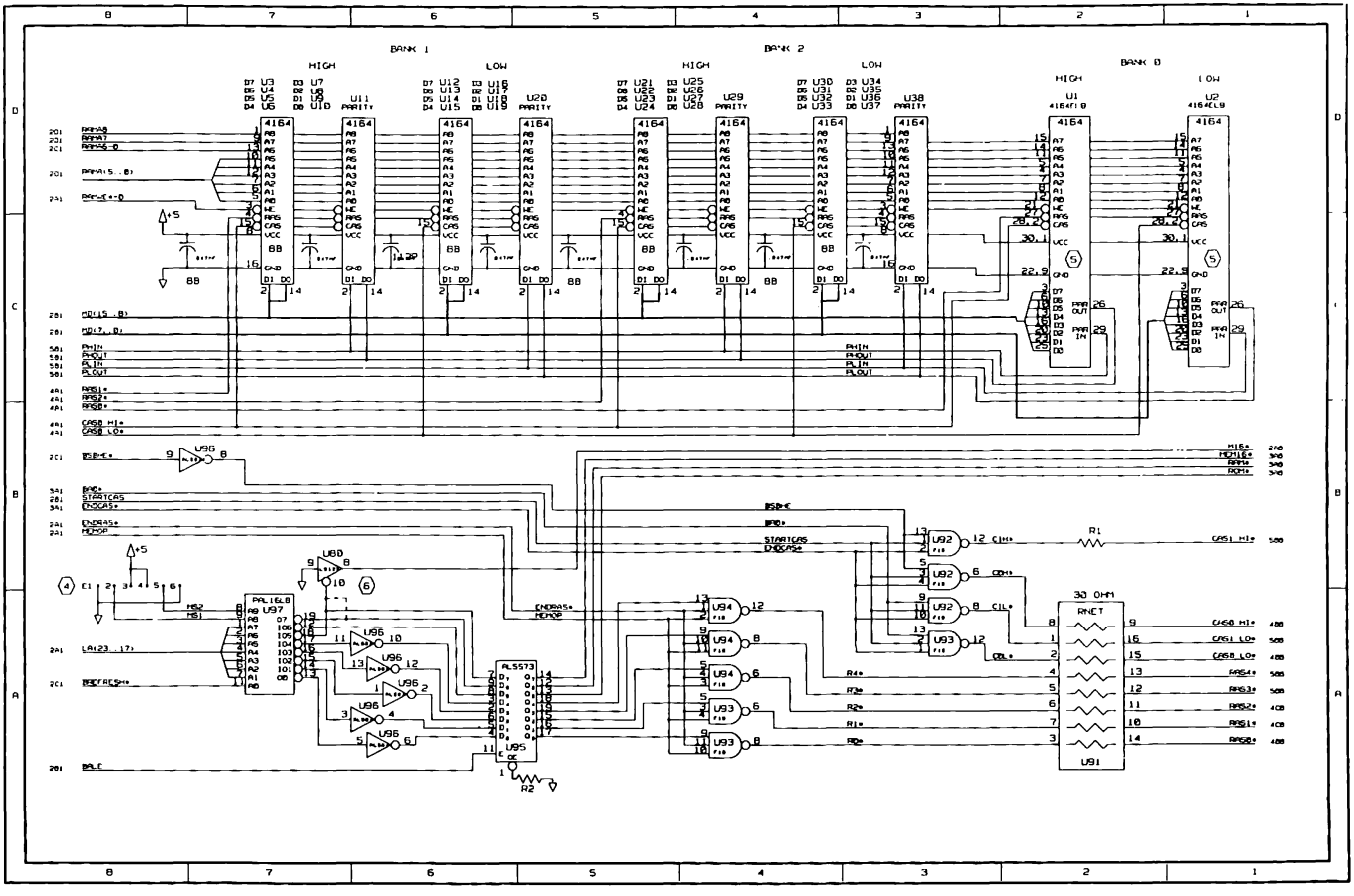


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 4 of 5)

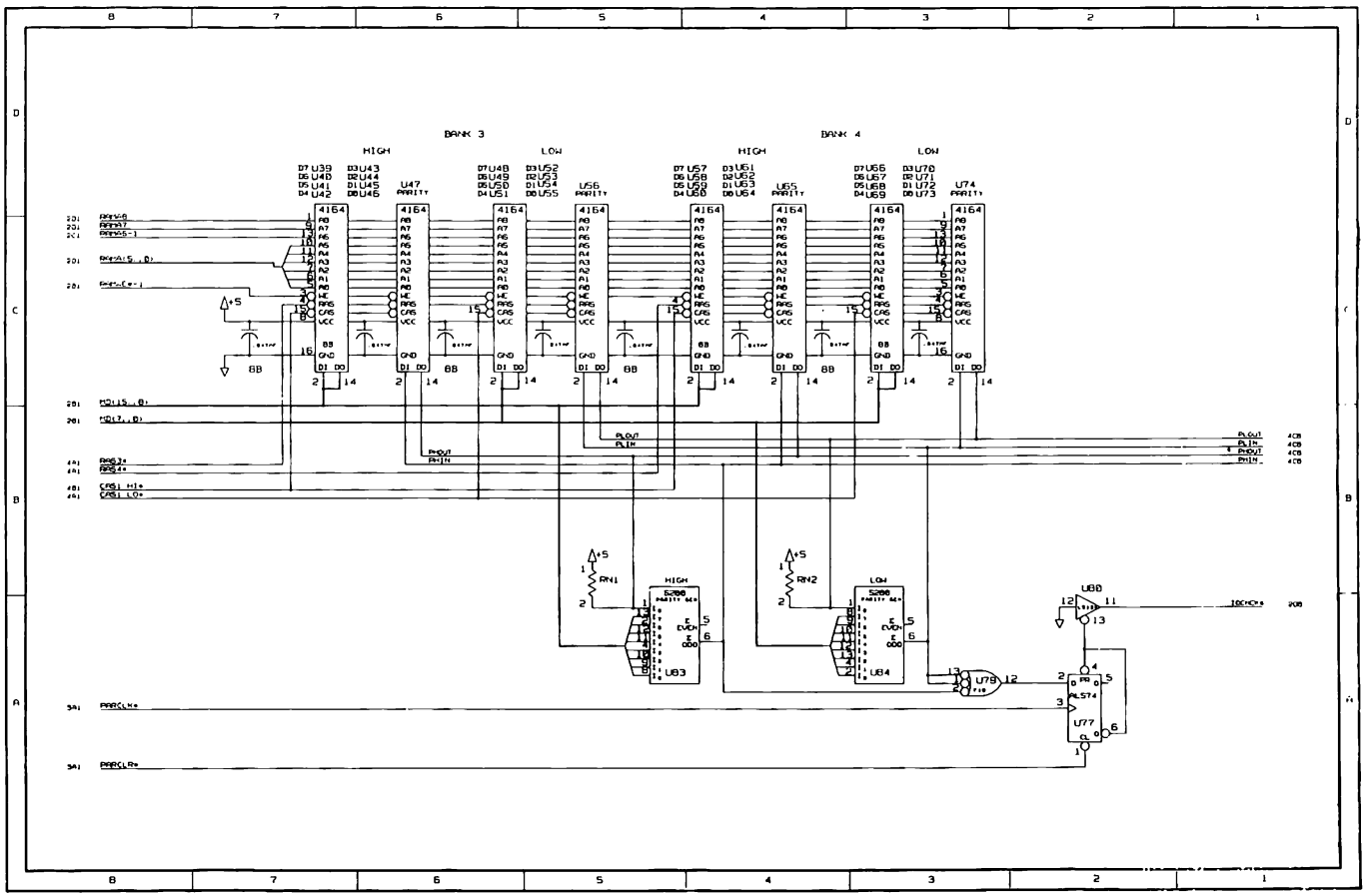


Figure 3-6. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 5 of 5)

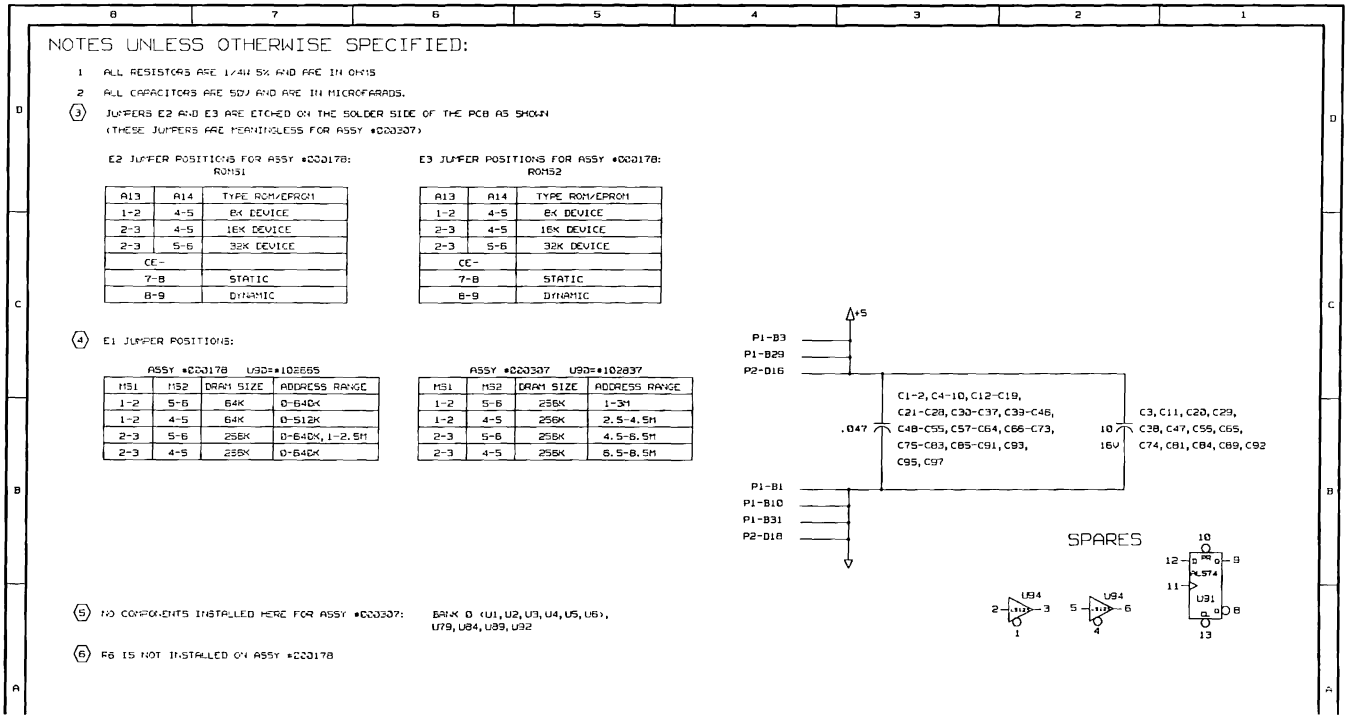


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Versions 2 and 3 Schematics (Page 1 of 5)

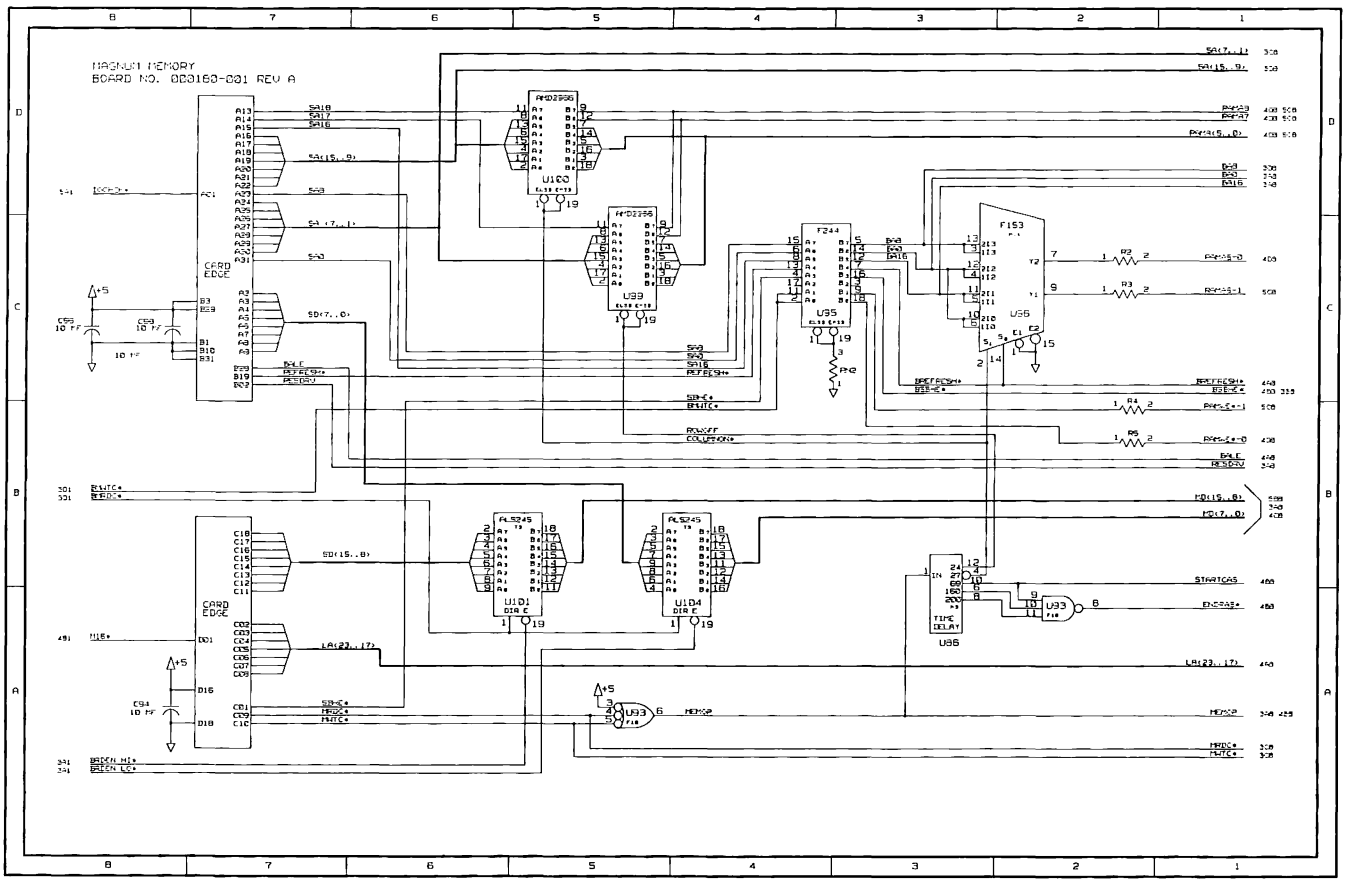


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 2 of 5)

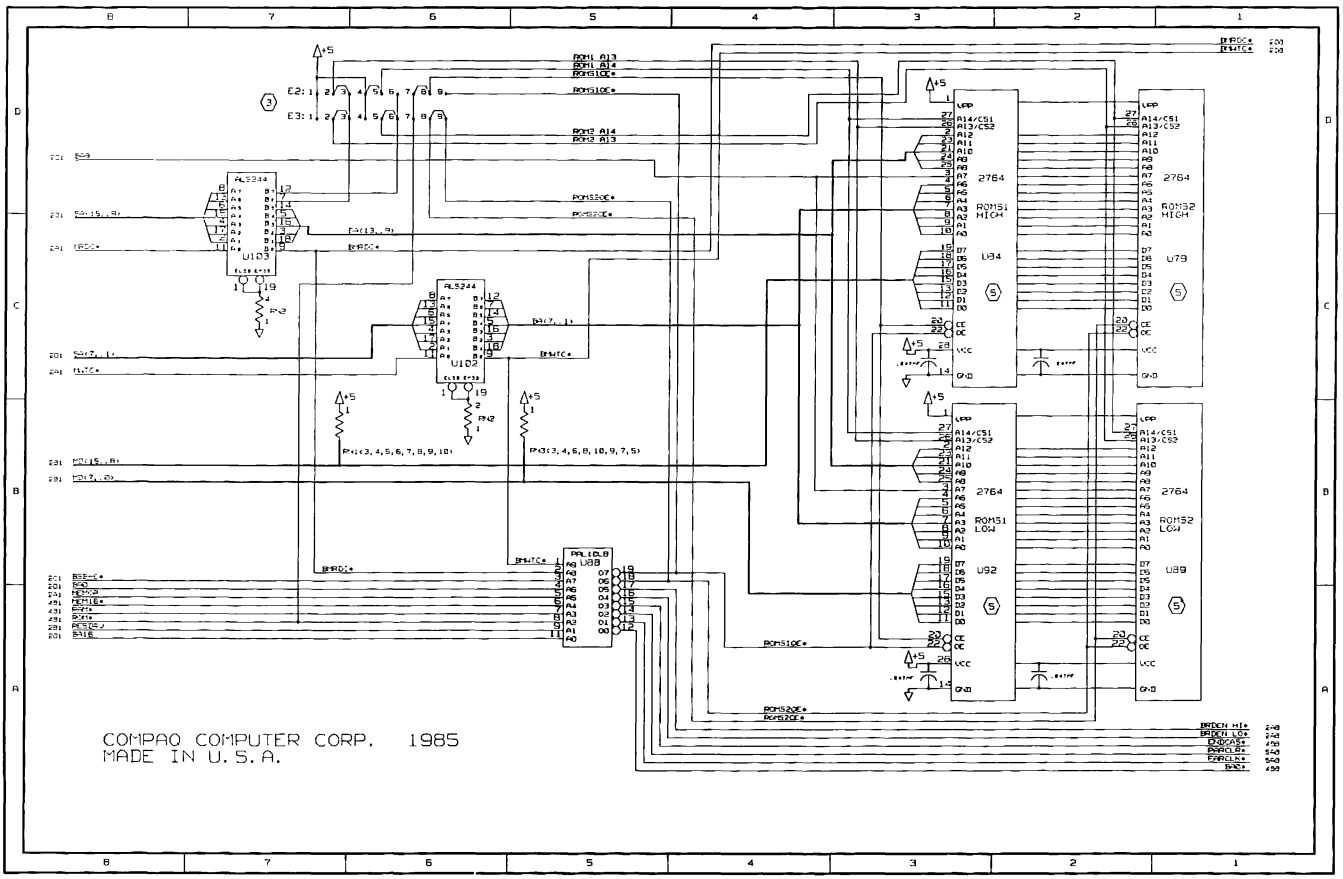


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 3 of 5)

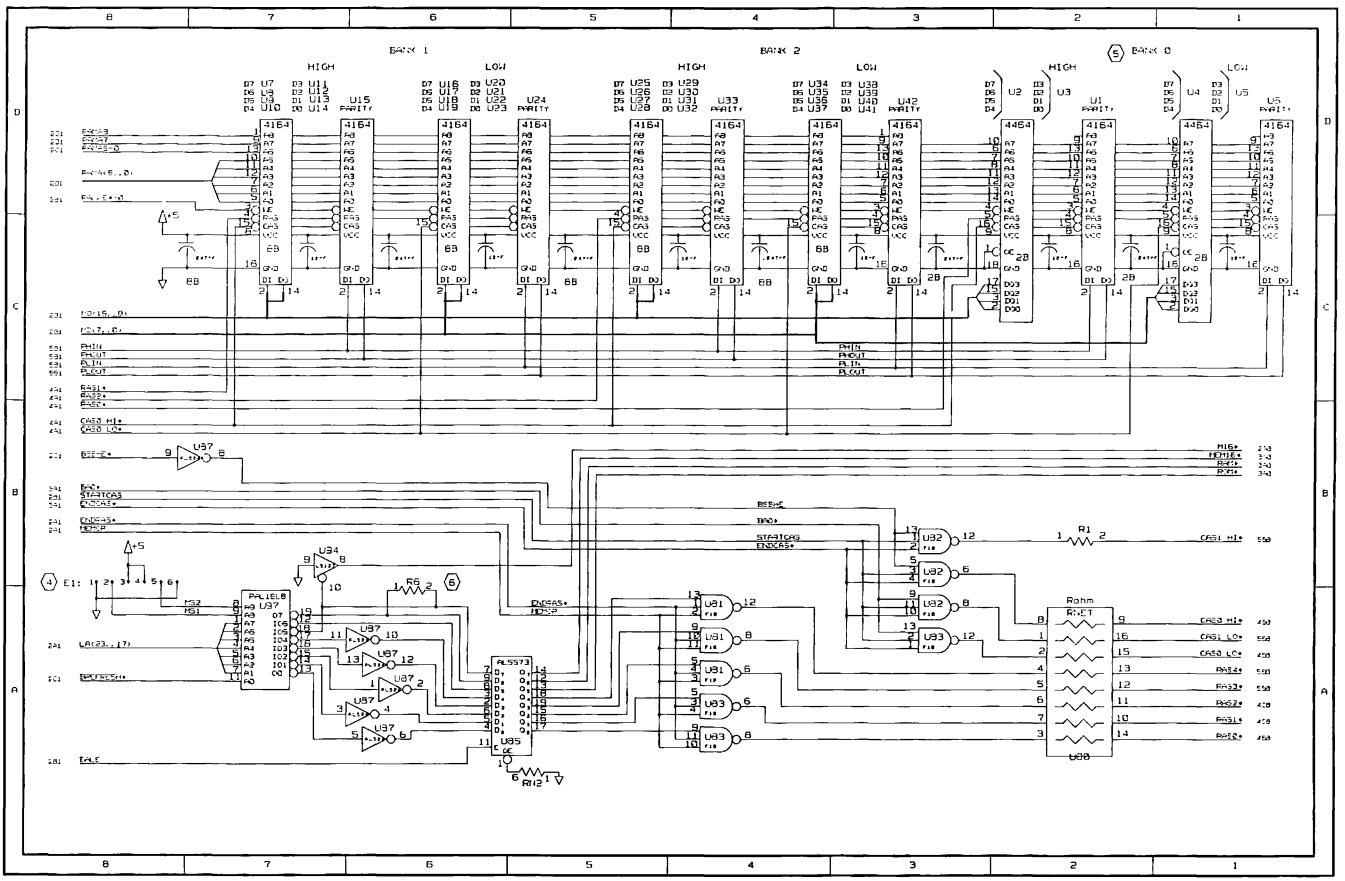
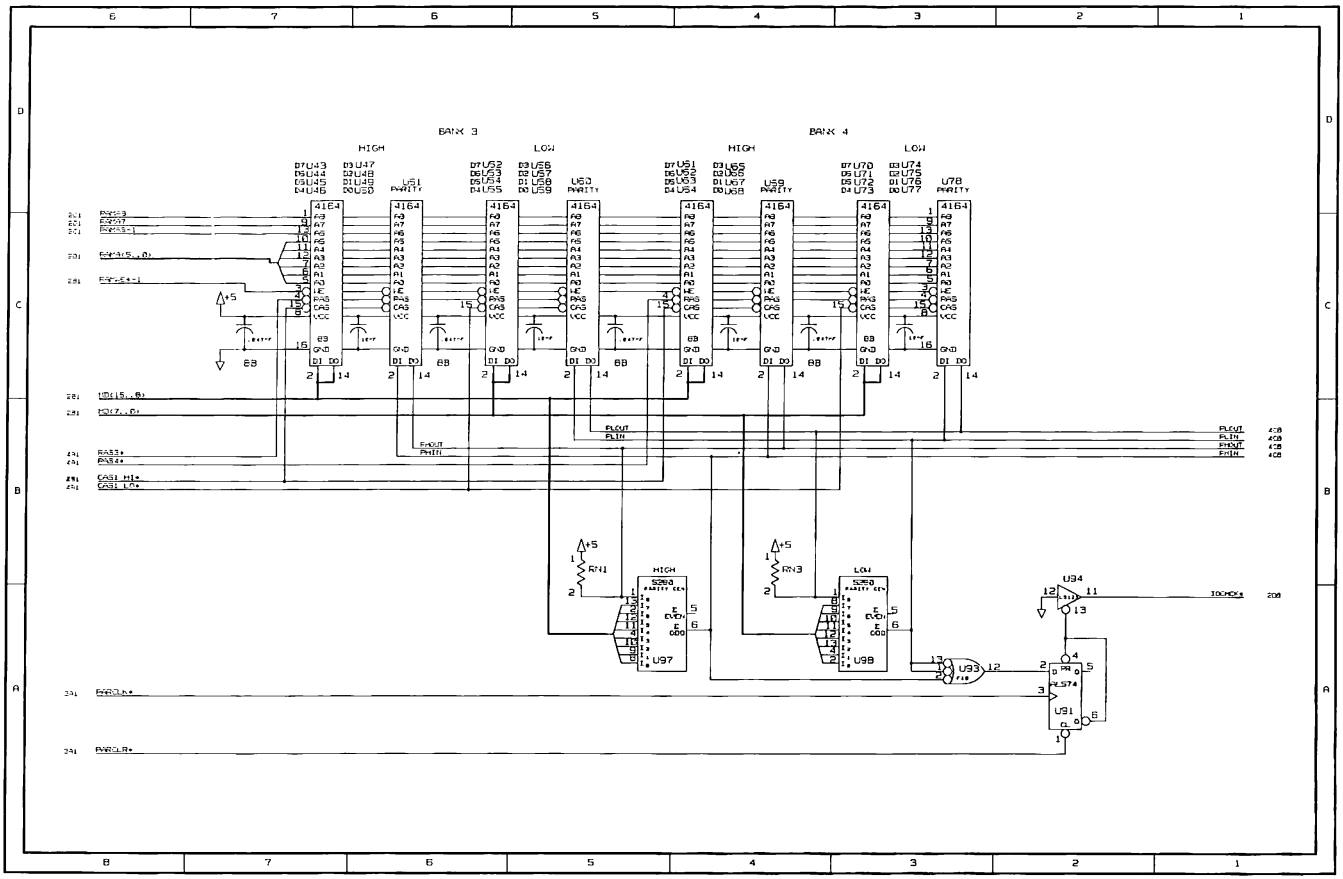


Figure 3-7. COMPAQ DESKPRO 286 System Memory Board Schematics (Page 4 of 5)



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Chapter 4

512/2048-KBYTE MEMORY EXPANSION BOARD

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4.1 INTRODUCTION

The 512/2048-Kbyte Memory Expansion Board provides for memory expansion of the COMPAQ DESKPRO 286® and the COMPAQ PORTABLE 286® Figures 4-1 and 4-2 show the component layouts for the two versions of the 512/2048-Kbyte Memory Expansion Board. Figure 4-3 shows the functional block diagram.

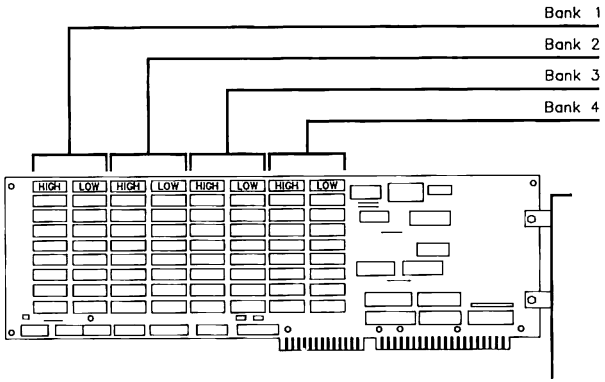

Figure 4-1. 512/2048-Kbyte Memory Expansion Board Version 1 Component Layout

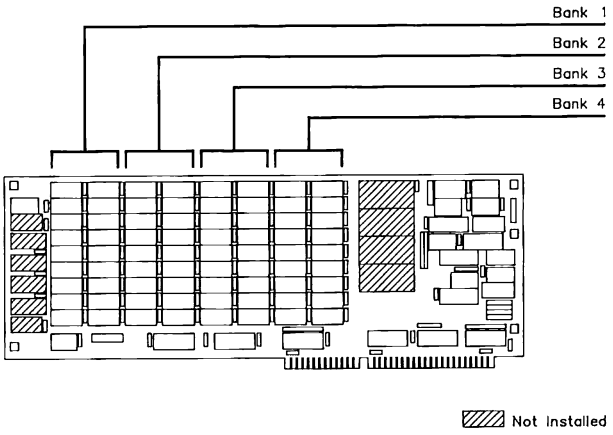

Figure 4-2. 512/2048-Kbyte Memory Expansion Board Version 2 Component Layout

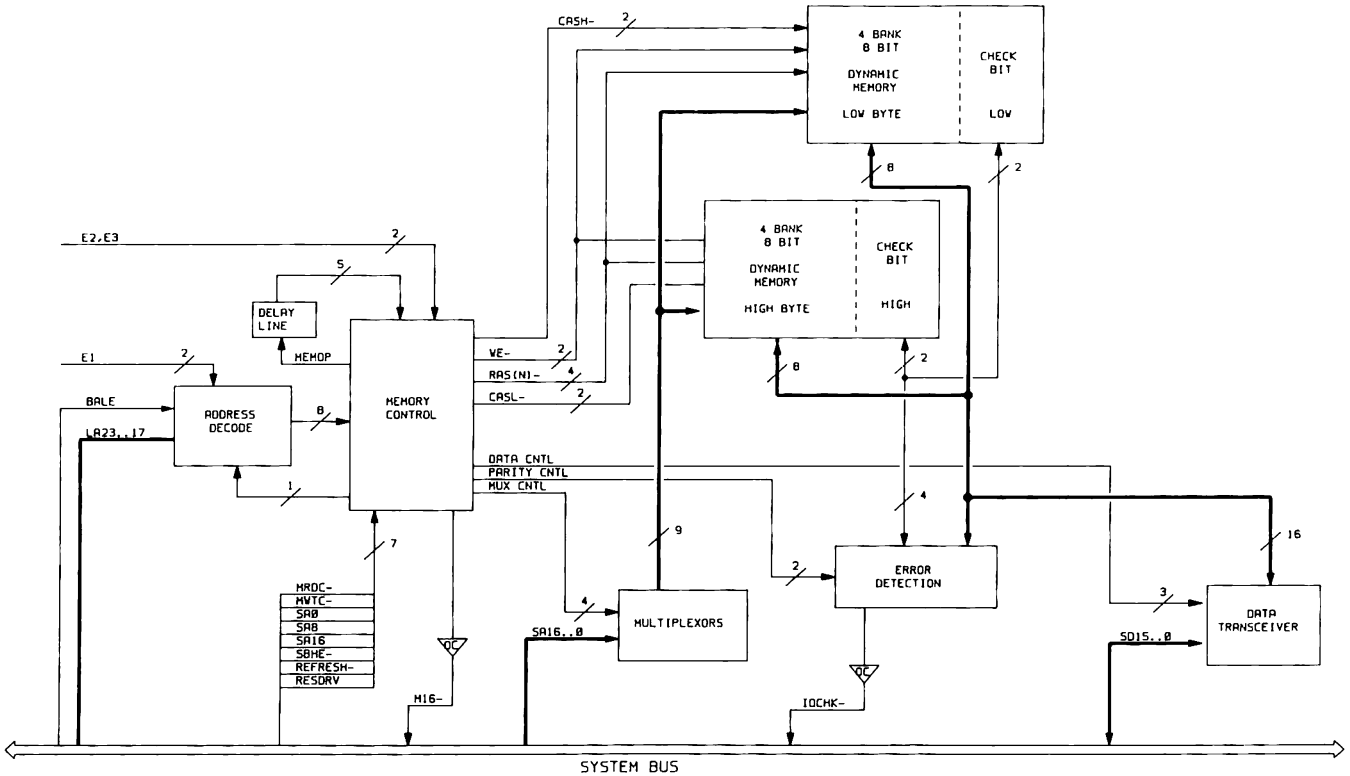

Figure 4-3. 512/2048-Kbyte Memory Expansion Board Functional Block Diagram

4.2 512/2048-KBYTE MEMORY EXPANSION BOARD RAM

The 512/2048-Kbyte Memory Expansion Board has four banks of sockets (Banks 1...4) that provide for system memory expansion using 256K x 1 dynamic RAM (DRAM) chips.

Memory must be installed in full-bank increments (18 DRAMs) in contiguous and ascending order.

There are four possible configurations (address ranges) for the 512/2048-Kbyte Memory Expansion Board:

- 1-3 Megabyte for the COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 with 640 Kbytes of base memory.
- 5-4.5 Megabyte for the COMPAQ DESKPRO 286 with 2176 Kbytes or the System Memory Board or on the COMPAQ DESKPRO 286 Version 2 System Board. (See Note).
- 5-6.5 Megabytes for the COMPAQ DESKPRO 286 with a 2.5-4.5-megabyte Memory Expansion Board installed.
- 5-8.5 Megabytes for the COMPAQ DESKPRO 286 with a 4.5-6.5-megabyte Memory Expansion Board installed.

NOTE: COMPAQ DESKPRO 286 Version 1 System Board requires the System Memory Board. The Version 2 System Board has the system ROM and RAM on the system board and does not use the System Memory Board.

Tables 4-1 and 4-2 show the possible memory configurations and their corresponding jumper settings.

Table 4-1. Memory Configuration and Corresponding Jumper Settings - Version 1 Memory Expansion Board

Jumper Setting	Address Range	Bank 1	Bank 2	Bank 3	Bank 4
E1-E2, E5-E6	1-3 MB	512 KB	512 KB	512 KB	512 KB
E1-E2, E4-E5	2.5-4.5 MB	512 KB	512 KB	512 KB	512 KB
E2-E3 E5-E6	4.5-6.5 MB	512 KB	512 KB	512 KB	512 KB
E2-E3 E4-E5	6.5-8.5 MB	512 KB	512 KB	512 KB	512 KB

Note: Use the instructions that come with the COMPAQ memory option kit to properly configure your memory expansion board.

Table 4-2. Memory Configuration and Corresponding Jumper Settings - Version 2 Memory Expansion Board

E1 Jumper Setting	Address Range	Bank 1	Bank 2	Bank 3	Bank 4
1-2,5-6	1-3 MB	512 KB	512 KB	512 KB	512 KB
1-2,4-5	2.5-4.5-MB	512 KB	512 KB	512 KB	512 KB
2-3,5-6	4.5-6.5 MB	512 KB	512 KB	512 KB	512 KB
2-3,4-5	6.5-8.5 MB	512 KB	512 KB	512 KB	512 KB

Note: Use the instructions that come with the COMPAQ memory option kit to properly configure your memory expansion board.

The 512/2048-Kbyte Memory Expansion Board uses approved 256K x 1 DRAM chips with a response time of 150 ns or faster. (CAS access time must be 75 ns or faster.) Use Only 256K x 1 DRAM in the 512/2048-Kbyte Memory Expansion Board.

Never add a memory expansion board with an address range that will overlap with any existing memory boards. Be sure to install memory expansion boards so that memory is contiguous through the specified address range for a particular memory expansion board, all four banks of RAM must be installed.

NOTE: Use the instructions that come with the COMPAQ Memory Expansion Board Option Kit to properly configure your memory board.

The schematics supplied in Chapter 3, COMPAQ DESKPRO System Memory Board are generally accurate for the board except that memory bank 0 and ROMs are not installed.

Figure 4-4 shows the relationship between the memory map and the installed RAM banks for each configuration.

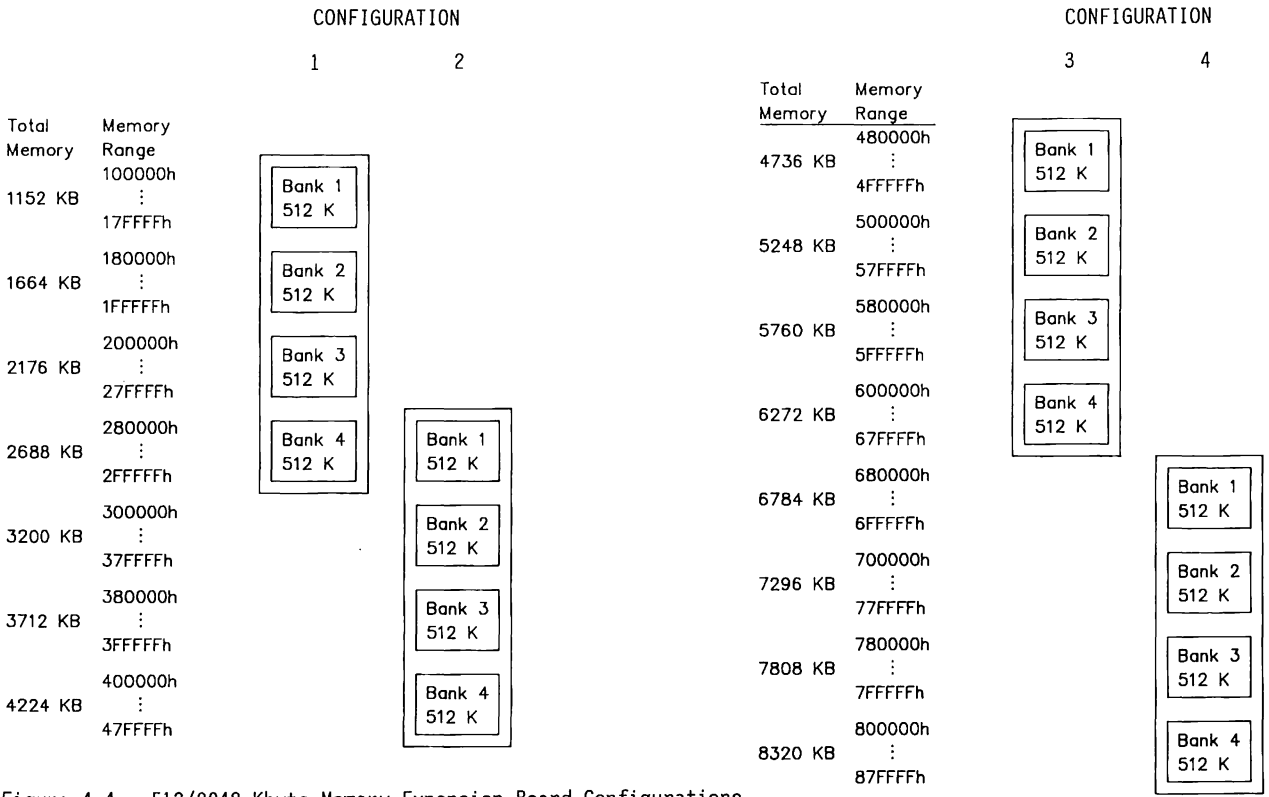

Figure 4-4. 512/2048-Kbyte Memory Expansion Board Configurations

Chapter 5

MULTIPURPOSE CONTROLLER BOARDS

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MULTIPURPOSE CONTROLLER BOARDS

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MULTIPURPOSE CONTROLLER BOARDS

5.1 INTRODUCTION

The multipurpose controller and multipurpose fixed disk drive controller boards are described in this chapter. The multipurpose controller board is used in the 8-MHz COMPAQ DESKPRO 286® and COMPAQ PORTABLE 286® Personal Computers

The multipurpose fixed disk drive controller board is used in the 12-MHz COMPAQ DESKPRO 286 Personal Computer.

Both controller boards supply the diskette drive and fixed disk drive drive backup controller board functions, as well as asynchronous and parallel printer communications functions. In addition to the above functions, the multipurpose fixed disk drive controller board also interfaces with a 40-megabyte fixed disk drive.

To interface with the multipurpose fixed disk drive controller board, the 40-megabyte fixed disk drive has an integrated controller on a logic board attached to the drive. The multipurpose fixed disk drive controller circuitry provides address decoding, buffers, and a control and data connector for the fixed disk drive controller.

NOTE: If a second 40-megabyte fixed disk drive is added to a COMPAQ DESKPRO 286, a 40-megabyte fixed disk drive back-up cannot be added to the system's configuration.

Figure 5-1 shows the component layout for the multipurpose controller board. Figure 5-2 shows the component layout for the multipurpose fixed disk drive controller board.

Figure 5-3 shows the functional block diagram for both multipurpose controller boards.

Three functions of both controller boards are controlled by programmable devices:

- Diskette and fixed disk drive backup controller functions are handled by an NEC 765A floppy disk controller device.
- Asynchronous communications are handled by a National Semiconductor NS16450.
- Parallel printer output and status are handled by a custom large-scale-integrated (LSI) device. This device also controls some drive control functions.

The following sections describe these programmable devices and other functions of the multipurpose controller boards.

Table 5-1 lists the I/O ports used on the multipurpose controller boards.

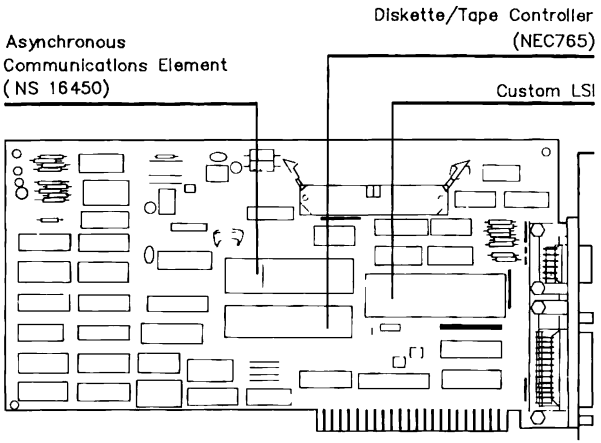


Figure 5-1. Multipurpose Controller Board Component Layout

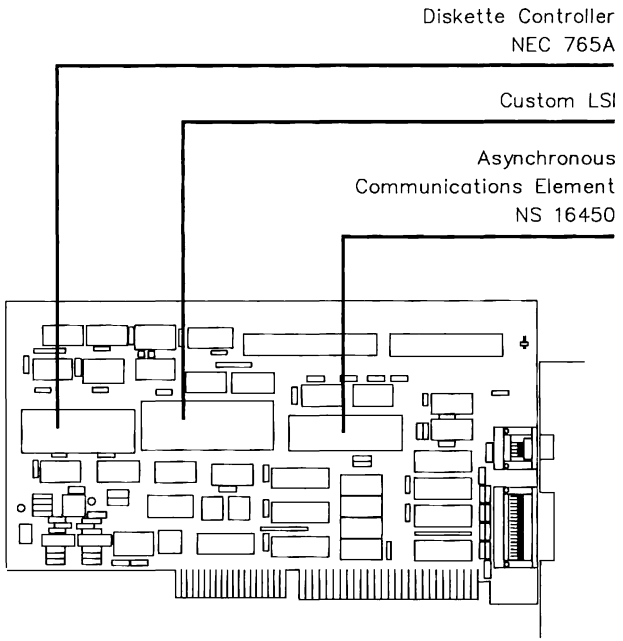


Figure 5-2. Multipurpose Fixed Disk Drive Controller Board Component Layout

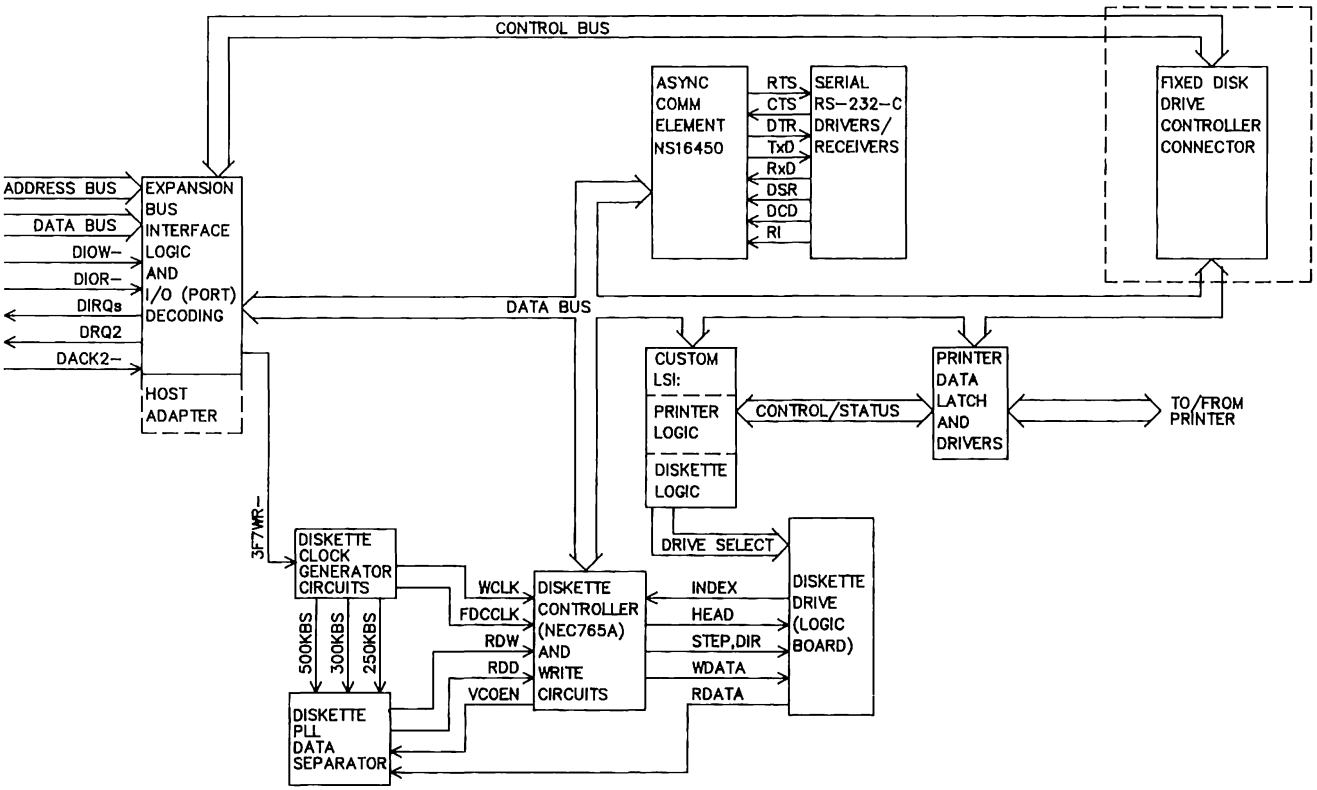


Figure 5-3. Functional Block Diagram for Both Multipurpose Controller Boards.

Table 5-1. Controller Board I/O Ports

Port	R/W	Register Functions	Multipurpose Controller Board	Multipurpose Fixed Disk Drive Controller Board
2F8h	R/W	COM2 Divisor Latch LSB (with DLA bit = 1 [Note 1])	(J2,2-3),(J4,2-3)	(J1, Pos. 2)
2F8h	R	COM2 Received Data (with DLA bit = 0 [Note 1])	"	"
2F8h	W	COM2 Transmit Data (with DLA bit = 0 [Note 1])	"	"
2F9h	R/W	COM2 Divisor Latch MSB (with DLA bit = 1 [Note 1])	"	"
2F9h	R/W	COM2 Interrupt Enable (with DLA bit = 0 [Note 1])	"	"
2FAh	R	COM2 Interrupt ID	"	"
2FAh	W	COM2 Reserved	"	"
2FBh	R/W	COM2 Line Control	"	"
2FCh	R/W	COM2 Modem Control	"	"
2FDh	R	COM2 Line Status	"	"
2FEh	R	COM2 Modem Status	"	"
2FFh	R/W	COM2 Reserved	"	"
370h	R/W	Diskette2 Reserved (Note 2)	(J1,1-2)	(J2, Pos. 2)
371h	R/W	Diskette2 Reserved (Note 2)	"	"
372h	W	Diskette2 Drive Control (Note 2)	"	"
372h	R	Diskette2 Reserved (Note 2)	"	"
373h	R/W	Diskette2 Reserved (Note 2)	"	"
374h	R	Diskette2 Main Status (Note 2)	"	"
374h	W	Diskette2 Reserved (Note 2)	"	"
375h	R/W	Diskette2 Data (Note 2)	"	(J1, Pos. 2)
377h	R	Diskette2 and Fixed Disk 2 Status (Note 2)	"	"
377h	W	Diskette2 Data Rate (Note 2)	"	"
3BCh	R/W	Printer1 Data	(J3,2-3)	SW2 ON
3BDh	R	Printer1 Status	"	"
3BDh	W	Printer1 Reserved	"	"

Notes: 1. The DLA bit is in the Line Control register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.
2. Diskette1 and Diskette2 are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

(Continued)

Table 5-1. (Continued)

Port	R/W	Register Functions	Multipurpose Controller Board	Multipurpose Fixed Disk Drive Controller Board
3BEh	R/W	Printer1 Control	(J2,2-3)	SW2 ON
3BFh	R/W	Printer1 Reserved	"	"
3F0h	R/W	Diskette1 Reserved	(J1,2-3)	(J2, Pos. 1)
3F1h	R/W	Diskette1 Reserved	"	"
3F2h	W	Diskette1 Drive Control	"	"
3F2h	R	Diskette1 Reserved	"	"
3F3h	R/W	Diskette1 Reserved	"	"
3F4h	R	Diskette1 Main Status	"	"
3F4h	W	Diskette1 Reserved	"	"
3F5h	R/W	Diskette1 Data	"	"
3F7h	R	Diskette1 and Fixed Disk 1 Status (Note 1)	"	"
3F7h	W	Diskette1 Data Rate	"	"
3F8h	R/W	Divisor Latch LSB (with DLA bit = 1 (Note 2))	(J2,1-2),(J4,1-2)	(J1 Pos. 1)
3F8h	R	COM1 Received Data (with DLA bit = 0 [Note 2])	"	"
3F8h	W	COM1 Transmit Data (with DLA bit = 0 (Note 2))	"	"
3F9h	R/W	COM1 Divisor Latch MSB (with DLA bit = 1 [Note 2])	"	"
3F9h	R/W	COM1 Interrupt Enable (with DLA bit = 0 [Note 2])	"	"
3FAh	R	COM1 Interrupt ID	"	"
3FAh	W	COM1 Reserved	"	"
3FBh	R/W	COM1 Line Control	"	"
3FCh	R/W	COM1 Modem Control	"	"
3FDh	R	COM1 Line Status	"	"
3FEh	R	COM1 Modem Status	"	"
3FFh	R/W	COM1 Reserved	"	"

Notes:
1. Only bit D7 of this port address is resident on the multipurpose controller board. Bits D<6..0> are resident on the fixed disk drive controller board.
2. The DLA bit is in the Line Control Register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.

5.2 DRIVE CONTROLLER CIRCUITS

The drive controller board circuits control one or two 1.2-MB or 360-KB or 1.44-MB diskette drives and one fixed disk drive backup (10- or 40-MB).

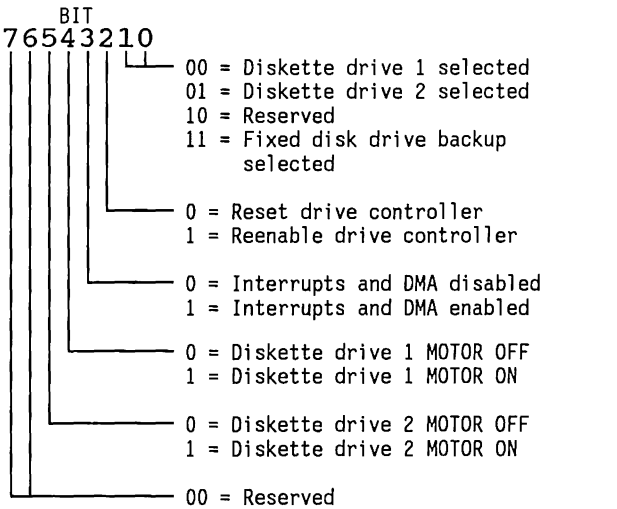
The drive controller uses four I/O port addresses to transmit data to and from a diskette drive or fixed disk drive backup, to control the drive functions, and to read the current drive status. Table 5-2 lists the port addresses for the drive controller.

Table 5-2. Drive Controller Port Addresses

Port 1	Port 2	R/W	Register Function
3F2h	372h	W	Drive Control
3F4h	374h	R	Drive Status
3F5h	375h	R/W	Data
3F7h	377h	W	Data Transfer Rate Control
3F7h	377h	R	Diskette and Fixed Disk Status

DRIVE CONTROL (3F2h, WRITE ONLY)

The Drive Control register is part of the Custom LSI device. It controls functions such as Interrupt and DMA Enable, Drive MOTOR ON, DRIVE SELECT, and Controller Reset. The format for this register is as follows:



MAIN STATUS (3F4h, READ-ONLY)

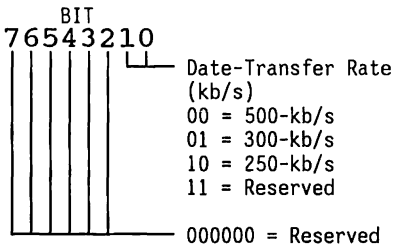
The Main Status register is part of the NEC 765A drive controller. It is used as the Diskette Status register.

DATA (3F5h)

The Data register is part of the NEC 765A drive controller. Data and NEC 765A controller commands are written, and data and status bytes are read from the controller through this port.

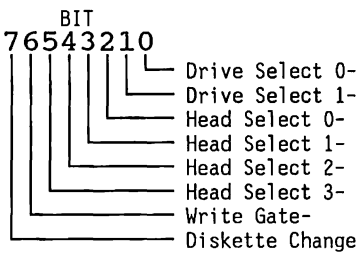
DATA TRANSFER RATE CONTROL (3F7h, WRITE-ONLY)

The Data-Transfer Rate Control register shares port 3F7h with the Diskette1 and Fixed Disk1 Status register. This register contains the current data-transfer rate in kilobits per second (kb/s). The format for this register is:



DISKETTE1 AND FIXED DISK1 STATUS (3F7h, READ ONLY)

This register provides both diskette1 status information (bit <7>) and fixed disk1 status information (bits <6...0>). The format for this register is as follows:



Drive Controller (NEC 765A)

The NEC 765A Floppy Disk Controller is the heart of the multipurpose controller board. It accepts commands from the system and controls most drive functions and the transfer of data to and from the drives.

The NEC 765A operates in the DMA mode for data transfers to the system. It issues a DMA request signal (DRQ2) and receives a DMA Acknowledge signal (DACK2-) for each byte transferred.

The NEC 765A has two registers, a Data register and the Main Status register (See Table 5-3). The Data register is used to program the device or to transmit or receive blocks of data.

Table 5-3. NEC 765A Registers

Port		
1	2	Function
3F4h	374h	Main Status Register
3F5h	375h	Data Register

All NEC 765A commands have three operating phases:

- The command phase, where the NEC 765A receives the command from the system.
- The execution phase, where the NEC 765A carries out the command.
- The results phase, where the status and results are read back from the NEC 765A to the system.

For detailed command information, refer to the NEC 765A or Intel 8272A component data sheets.

The Custom LSI Device

The Custom LSI device is a circuit for address decoding and control signal timing. It is addressed as a port device to control the diskette drive motors and for drive selection.

Programmable Data Transfer Rate

The system can transfer data with the diskette drives at 250-, 300-, or 500-kb/s. Table 5-4 lists the data transfer rates used by various drives. The Data-Transfer Rate Control register format describes the byte that specifies the present transfer rate.

Table 5-4. Programmable Data Transfer Rate

Transfer Rate	When Used
500 kb/s	1.2-Megabyte Diskette Drive with 1.2-Megabyte media or 1.44-Megabyte Diskette Drive with 1.44-Megabyte media.
500 kb/s	40-Megabyte Fixed Disk Drive Backup with 40-Megabyte media
300 kb/s	1.2-Megabyte Diskette Drive with 360-Kbyte media
250 kb/s	Double-density diskette drive, Fixed Disk Drive Backup with 10-megabyte media; or 1.44-Megabyte Diskette Drive with 720-Kbyte media

Data Separator

Data separation separates the Data and Clock signal from the drives into separate Clock and Data lines. Several devices form a voltage-controlled oscillator/phase-locked loop circuit to perform the data separation.

Write Precompensation and Write Control

Write precompensation is a process of time shifting write data bits to help negate an opposite shift induced during magnetic recording. This process increases the data integrity at high data densities. The data density increases as the diskette drive head approaches the center tracks (track 40 or 80).

Write precompensation is always on. The amount of precompensation varies with the data transfer rate (See Table 5-5).

Table 5-5. Write Precompensation Amounts

Transfer Rate	Precompensation
500-kilobytes per second	125 ns
300-kilobytes per second	208 ns
250-kilobytes per second	250 ns

5.3 ASYNCHRONOUS COMMUNICATIONS CIRCUITS

The asynchronous serial port is always enabled except on revision level G (or later) multipurpose controller boards or on multipurpose fixed disk drive controller board, which can disable the port by setting Switch 3 in switch bank SW1 to the OFF position.

The heart of the asynchronous communication circuit is a National Semiconductor NS16450 Asynchronous Communications Element (ACE). This device converts data received in a parallel format from the system to data in a serial format for a serial printer or other serial device. It also converts the serial data to parallel.

This device is I/O-mapped at ports 3F8h..3FFh or 2F8h..2FFh, depending on whether COM1 or COM2 is selected (see Table 5-6).

Table 5-6. I/O Ports for Asynchronous Communications

Port 1	Port 2	Function
3F8h	2F8h	Receiver Buffer (when read by system), Transmitter Holding Register (when written to by system) or
See Note		Baud Rate Divisor Latch
3F9h	2F9h	Interrupt Enable or
See Note		Baud Rate Divisor Latch
3FAh	2FAh	Interrupt ID (read only)
3FBh	2FBh	Line Control
3FCh	2FCh	Modem Control
3FDh	2FDh	Line Status
3FEh	2FEh	Modem Status
3FFh	2FFh	Scratch

Note: When bit 7 of the Line Control Register (LCR) is set (=1), writing to the first two ports programs the divisor rate for the Baud Rate Generator.

ACE RECEIVER BUFFER OR TRANSMITTER HOLDING REGISTER (3F8h)

This register contains the byte just received or the next byte to be transmitted by the ACE.

ACE BAUD RATE DIVISOR LATCH (3F8h, 3F9h)

The NS16450 contains a built-in baud rate generator that divides the input clock (1.8432 MHz) by a divisor to create a desired baud rate or serial transmission frequency.

The divisor is found according to the formula:

Divisor = 1843200 / (Desired Baud Rate x 16)

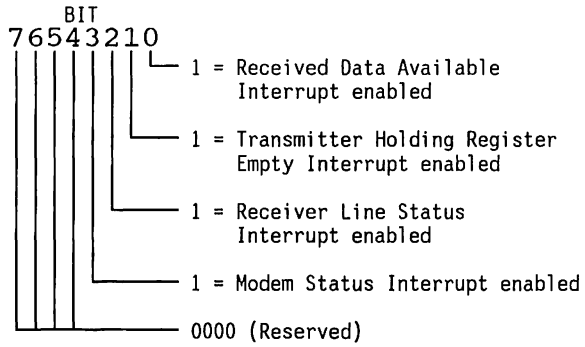
The following tabulation gives the divisors calculated for specific baud rates:

Baud Rate	Divisor
110	1047
150	768
300	384
600	192
1200	96
2400	48
4800	24
9600	12

Setting bit <7> (=1) enables the first two I/O addresses of the Line Control register as the addresses for the least- and most-significant bytes of the 16-bit baud rate divisor.

ACE INTERRUPT ENABLE REGISTER (3F9h)

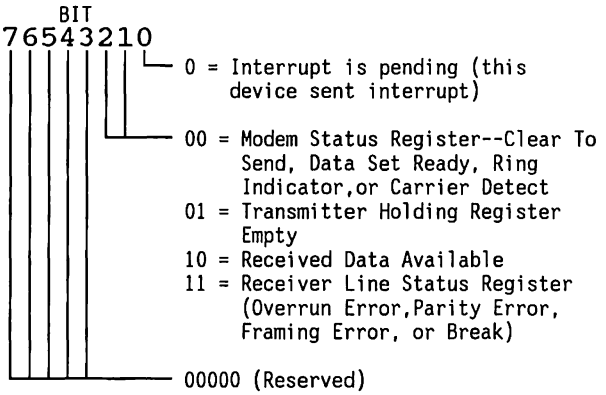
The bits of this register enable up to four interrupt sources.



ACE INTERRUPT ID REGISTER (3FAh, READ-ONLY)

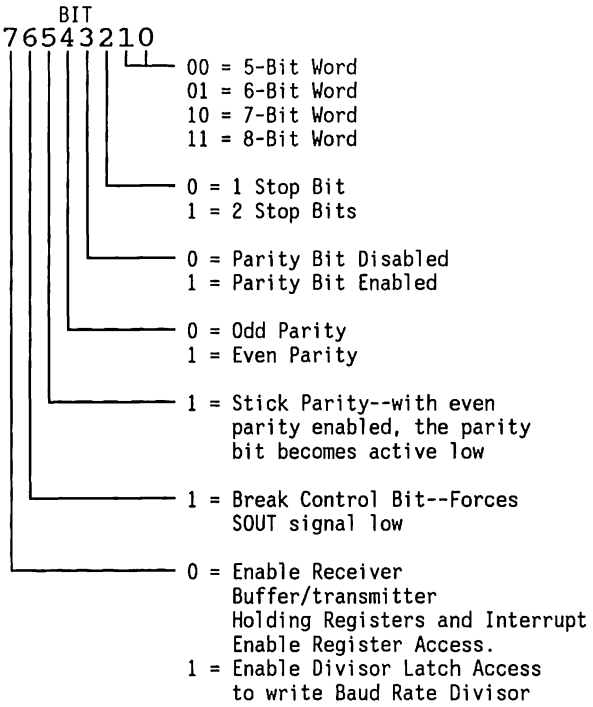
When a hardware interrupt occurs, the system searches for the device sending the interrupt and the reason for that interrupt.

This register contains a bit that flags the ACE as the source of the interrupt and two bits that specify the reason for the interrupt. The ACE interrupts are prioritized, and listed below with the lowest-priority interrupt first. To clear the interrupt, read the contents of the register shown.



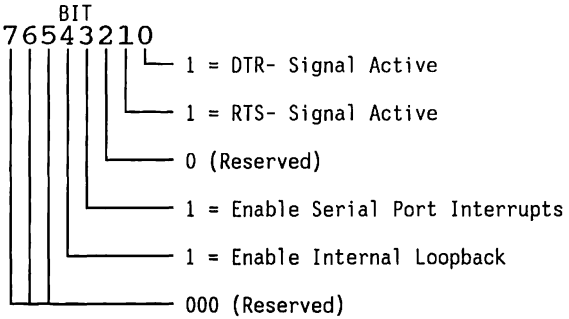
ACE LINE CONTROL REGISTER (3FBh)

This register specifies the serial data transmission format.



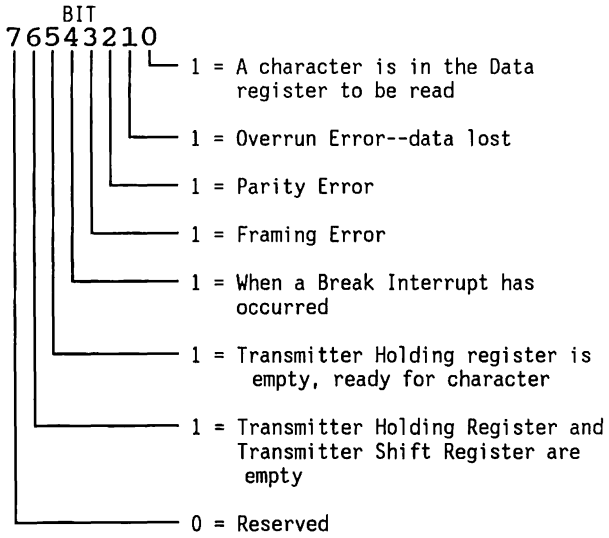
ACE MODEM CONTROL REGISTER (3FCh)

This register controls the modem interface lines.



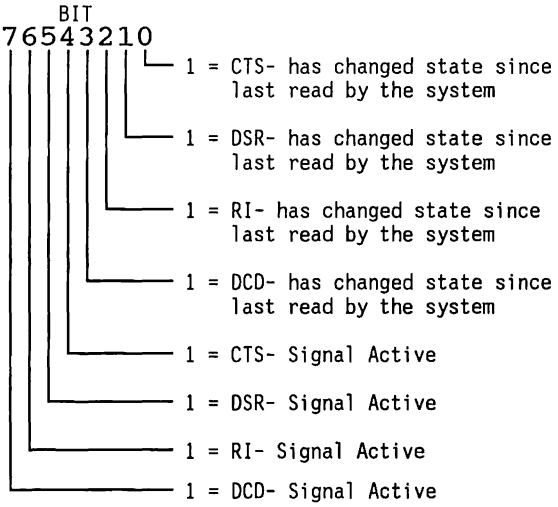
ACE LINE STATUS REGISTER (3FDh, READ-ONLY)

This register contains the status of the current data transfer.



ACE MODEM STATUS REGISTER (3FEh, READ-ONLY)

This register contains the status of the modem interface lines.



ACE RESERVED (3FFh)

This is not currently used.

5.4 PRINTER CIRCUITS

The printer port is enabled either by setting Jumper J3, Pins 2-3, on the multipurpose controller board or by setting Switch 2 in switch bank SW1, on the multipurpose fixed disk drive controller board. When the printer is disabled, the printer port of a different controller can be used instead of the multipurpose controller board or multipurpose fixed disk drive controller board port.

The printer circuits are addressed as ports. Data is sent in parallel to the printer, and printer status is received from the printer through these ports.

Before printing, the system must select the printer for output (through the Printer Control register). For each byte sent to the printer, the system:

1. Checks the Printer Status register.
   If the busy, paper out, or printer fault signals are active, the system either waits until the status changes or it shows an error message.
2. Sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control Register) for 500 ns (or longer).
3. Monitors the Printer Status register for acknowledgement of the data byte before sending the next byte.

In addition to data lines to the printer, the system also has several control lines that control printer functions.

Printer functions are controlled by writing to or reading from I/O ports. Table 5-7 provides I/O Ports for Printer Access.

Table 5-7. I/O Ports For Printer Access

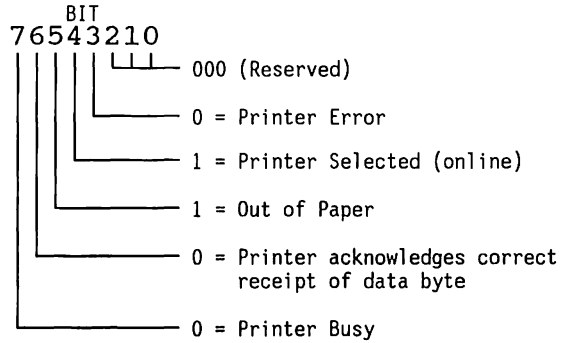
Port	R/W	Function
3BCh	R/W	Printer Data register
3BDh	R	Printer Status register
3BEh	R/W	Printer Control register

PRINTER DATA REGISTER (3BCh)

Each byte written to the Printer Data register (read or write) is latched into a loopback register and is sent to the printer. The register contents can be read back (for test purposes).

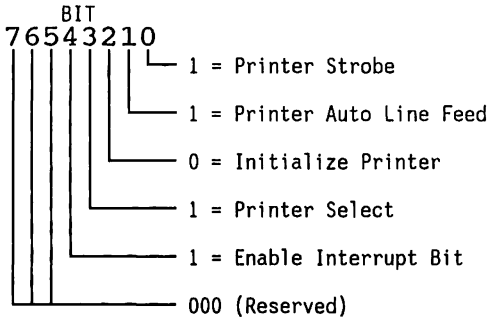
PRINTER STATUS REGISTER (3BDh, READ-ONLY)

This register contains the current printer status.



PRINTER CONTROL REGISTER (3BEh)

This register selects the printer for output, strobes the data into the printer, and performs other printer control functions.



5.5 JUMPERS

Jumpers for both the multipurpose controller board and the multipurpose fixed disk drive controller board are given in this section.

Multipurpose Controller Board Jumpers

The multipurpose controller board has four jumpers which are described in Table 5-8. The jumper locations are shown in Figure 5-4.

Table 5-8. Multipurpose Controller Board Jumpers

Jumper	Function
J1	Diskette Controller Board Base-Address Select. This address-selection option is available for special applications and under normal circumstances should not be changed. (J1,1-2) Secondary (Diskette2) Address Select (370h) (J1,2-3) Primary (Diskette1) Address Select (3F0h, standard) "Diskette1 and Diskette2" are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.
J2	Asynchronous Communications Port Base-Address Select. This address-selection option allows two asynchronous communication ports to operate at the same time, using two I/O port ranges. Jumpers J2 and J4 are generally set together (see jumper J4). (J2,1-2) Asynchronous communications Port 1 (COM1) selected (3F8h, standard) (J2,2-3) Asynchronous communications Port 2 (COM2) selected (2F8h)

(Continued)

Table 5-8. (Continued)

Jumper	Function
J3	Printer Enable. This jumper allows the printer port decoding to be disabled. This option prevents conflicts with I/O addresses 3BCh-3BFh when a multifunction board is installed that has Printer1 I/O port decoding. (J3,1-2) Parallel Printer Port disabled (J3,2-3) Parallel Printer Port enabled (standard)
J4	Asynchronous Communications Port Interrupt Select. This jumper option allows the interrupt request line associated with the asynchronous communications port to be changed when the selected asynchronous communications port is changed. COM1 and IRQ4 are used together, as are COM2 and IRQ3. (J4,1-2) Asynchronous Communications Port IRQ4 (COM1) selected (standard) (J4,2-3) Asynchronous Communications Port IRQ3 (COM2) selected

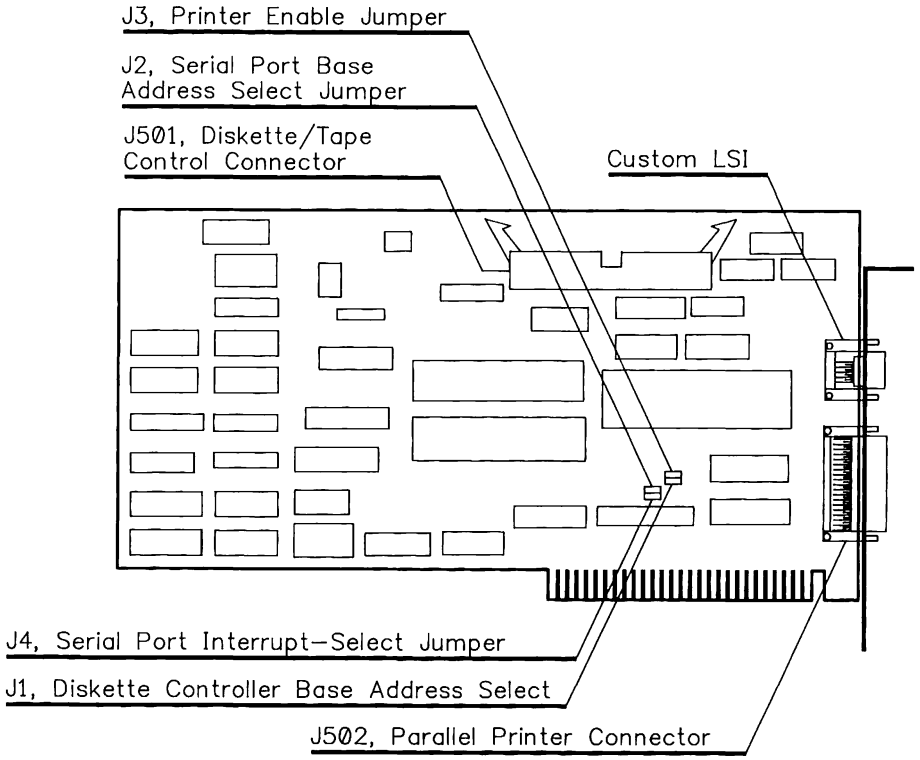


Figure 5-4. Multipurpose Controller Board Jumper Locations

Multipurpose Fixed Disk Drive Controller Board Jumpers

The multipurpose fixed disk drive controller board jumpers are described in Table 5-9 and are shown in Figure 5-5.

Table 5-9. Multipurpose Fixed Disk Drive Controller Board Jumpers

Jumper	Function
J1	Asynchronous Communications Port Base-Address and Interrupt Request Select. This address-selection option allows two asynchronous communications ports to operate at the same time, using two I/O port ranges. Position 1, Com1-Asynchronous Communications Port 1 selected (3F8H and IRQ4 standard). Position 2, Com2-Asynchronous Communications Port 2 selected (2F8h and IRQ3).
J2	Diskette and Fixed Disk Drive Base-Address Select. This address selection option is available for special applications and under normal circumstances should not be changed. Position 1, Primary (Diskette1) Address Select (3F0h standard). Position 2, Secondary (Diskette2) Address Select (370h). "Diskette1 and Diskette2" are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.
Note:	To change the setting, remove the shunt jumper room the socket, rotate it 180 degrees, and reinstall the jumper in the socket.

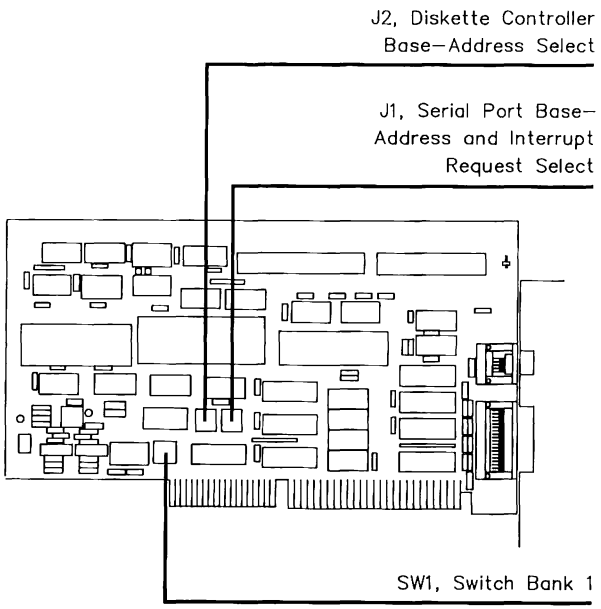


Figure 5-5. Multipurpose Fixed Disk Drive Controller Board Jumper Locations

5.6 SWITCHES

The multipurpose fixed disk drive controller board and multipurpose controller board version 2 have four switches in one switch bank (SW1). These switches are described in Table 5-10.

Table 5-10. Multipurpose Fixed Disk Drive Controller Board Switch Positions (SW1)

Number	Function
1	Fixed Disk Drive Enable. This switch allows the fixed disk drive port to be disabled. S1 = On, fixed disk drive port enabled (standard) S1 = Off, fixed disk drive port disabled.
2	Printer Enable. This switch allows the printer port to be disabled. This option prevents conflicts with I/O addresses 38Ch-38Fh when a multifunction board is installed that has a printer I/O port at these addresses. S2 = On, Parallel Printer Port enabled (standard) S2 = Off, Parallel Printer Port disabled.
3 (See Note)	Serial Port disable. Allows the serial port to be disabled. S3 = On, Serial Port Enabled (Standard) S3 = Off, Serial Port Disabled
4	Reserved Always Off.

Note: This function is available only on revision level G (or later) multipurpose fixed disk controller boards.

5.7 CONNECTORS

The connector descriptions for both the multipurpose controller board and multipurpose fixed disk drive controller boards are described in this section.

Table 5-11 lists the connectors and the number of table that contains the signal description for each connector. Tables 5-12 through 5-16 contain the signal descriptions for each controller board connector.

Figure 5-6 shows the multipurpose controller board connectors and jumpers. Figure 5-7 shows the multipurpose fixed disk drive controller board connectors and jumpers.

The multipurpose controller board signals used by diskette drives and fixed disk drive backup are listed in Table 5-17.

NOTE: Pin 34 of the 34-conductor control cable is implemented as the DISKETTE CHANGE- signal. Diskette drives that use this pin for DRIVE READY- do not work.

Table 5-11. Controller Connectors

Connector	Description	Location of Signal Description
J701	Asynchronous Communication Connector	Table 5-12
J502	Parallel Printer Connector	Table 5-13
J902	Fixed Disk Drive LED	Table 5-14
J901	Fixed Disk Drive Controller Host Adapter Connector	Table 5-15
J501	Diskette Drive Connector	Table 5-16

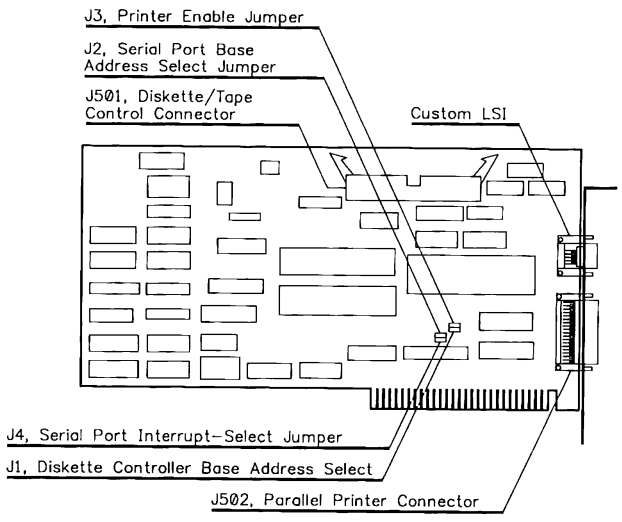


Figure 5-6. Multipurpose Controller Board Connector Locations

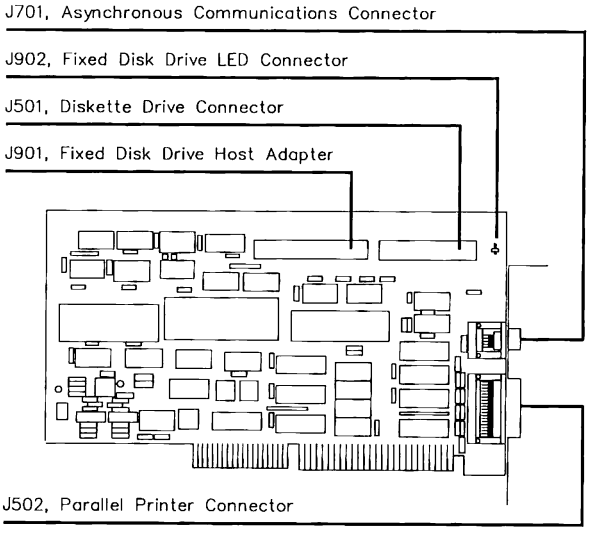


Figure 5-7. Multipurpose Fixed Disk Drive Controller Board Connector Locations

Table 5-12. J701, 9-Pin Serial Connector Signals

Signal	Pin	I/O	Description
CARRIER DETECT (CD)	1	I	Modem signal indicating that a connection is established with another modem
CLEAR TO SEND SEND (CTS)	8	I	Modem signal indicating readiness to accept data
DATA SET READY (DSR)	6	I	Modem signal--it is online and can receive data
DATA TERMINAL READY (DTR)	4	O	Signal to a modem indicating that the computer is ready
RECEIVE DATA (RX)	2	I	Serial data receive line
REQUEST TO SEND (RTS)	7	O	Signal to a modem to request a transmission
RING INDICATOR (RI)	9	I	Modem signal indicating that it is receiving a ringing signal from the phone line
SIGNAL GROUND	5	- -	- -
TRANSMIT DATA (TX)	3	O	Serial data sent to modem

Note: All signal levels are RS-232-C compatible.

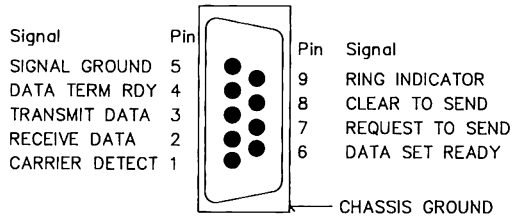


Figure 5-8. J701, 9-Pin Asynchronous Communications Connector

Table 5-13. J502, 25-Pin Parallel Printer Connector Signals

Signal	Pin	I/O	Description
ACKNOWLEDGE-	10	I	Data sent to printer has been received.
AUTO LINEFEED-	14	O	Instructs printer to automatically feed one line of paper after receiving a carriage return.
BUSY	11	I	Active-high signal indicating that the printer cannot receive data due to printing, offline, or error conditions.
DATA BIT 0	2	O	Signals transmit data to printer in 8-bit parallel format.
DATA BIT 1	3	O	
DATA BIT 2	4	O	
DATA BIT 3	5	O	
DATA BIT 4	6	O	
DATA BIT 5	7	O	
DATA BIT 6	8	O	
DATA BIT 7	9	O	
ERROR-	15	I	Indicates a printer error condition such as out-of-paper.
SIGNAL GROUND	18	-	Return conductors for all signals.
	19	-	
	20	-	
	21	-	
	22	-	
	23	-	
	24	-	
	25	-	

(Continued)

Table 5-13. (Continued)

Signal	Pin	I/O	Description
INITIALIZE PRINTER-	16	O	Initializes the printer and clears the print buffer. This signal should remain active for at least 500 us.
PAPER END	12	I	Indicates that the printer is out of paper.
SELECT	13	I	Indicates that the printer is selected and online.
SELECT IN-	17	O	Selects the printer and enables it to accept data.
STROBE-	1	O	On high-to-low transition, causes data present on DATA BIT lines to be loaded into printer. STROBE- pulse width must be a minimum of 500 ns. Data must be setup a minimum of 500 ns before the high-to low transition and held a minimum of 500 ns after the low-to-high transition.

Note: All signals are TTL-level.

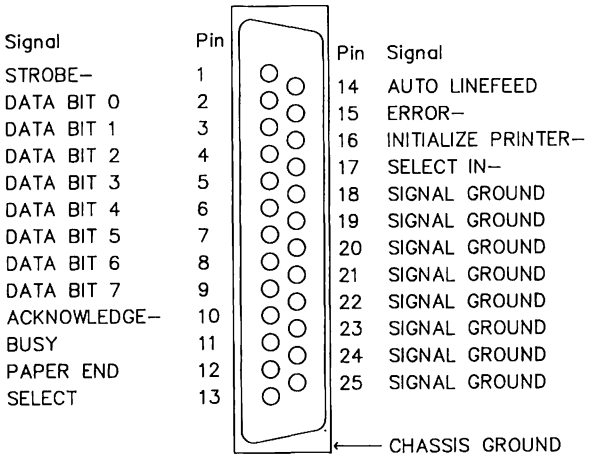


Figure 5-9. J502, 25-Pin Parallel Printer Connector

Table 5-14. J902, Fixed Disk Drive Controller LED Indicators

Signal	Pin	I/O	Description
LEDANODE	1		+5 VDC source for the fixed disk drive LED indicator.
- -	2		Reserved
ACTIVE-	3	O	Indicates that the fixed disk drive is being accessed. This line is used to drive an activity LED indicator that lights when the drive is activated.
- -	4		Reserved

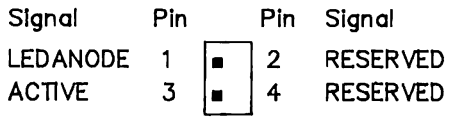


Figure 5-10. J902, Fixed Disk Drive Controller LED Indicators Connector

Table 5-15. J901, Fixed Disk Drive Controller Host Adapter Connector Signal Descriptions

Signal	Pin	I/O	Description
ACTIVE-	39	I	Active-low signal indicating that the fixed disk drive LED indicator is on and the fixed disk drive is being accessed.
CS1FX-	37	O	Chip Select 1Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 1F0h and 1F7h.
CS3FX-	38	O	Chip Select 3Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 3F6h through 3F7h.
DA0 DA1 DA2	35 33 36	O O O	Address A0-A2. Buffered address lines from the address bus to the fixed disk drive controller.
DALE	28	O	Address latch enable. Signals that address bus signals are stable and valid.
DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0	3 5 7 9 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O	Data bit 0-7. Least-significant eight bits of the 16-bit data bus for data and status communication between the controller and the host. D7 is the most-significant bit of this byte.

(Continued)

Table 5-15. (Continued)

Signal	Pin	I/O	Description
DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15	4 6 8 10 12 14 16 18	I/O I/O I/O I/O I/O I/O I/O I/O	Data bit 8-15. Most-significant eight bits for data and status communication between the controller and the host. DD15 is the most-significant bit of this byte.
DIOW-	23	O	I/O write. Active when the host writes a control byte or data word to the controller.
DIOR-	25	O	I/O read. Active when the host reads a status byte or data word from the controller.
I/O16CS-	32	I	Chip Select 16. Chip select used to signal the processor that the current I/O cycle is a 16-bit, single wait-state cycle.
IRQ14	31	I	Interrupt Request 14. Asserted by the controller to interrupt the processor upon completion of a fixed disk drive operation.
RST-	1	O	Reset. This signal resets the controller to the initial power-on condition.
SIGNAL GROUND	2,19, 22,24, 26,30,40	-	Return conductor.

Note: Pins 20, 21, 27, 29, and 34 are not connected.

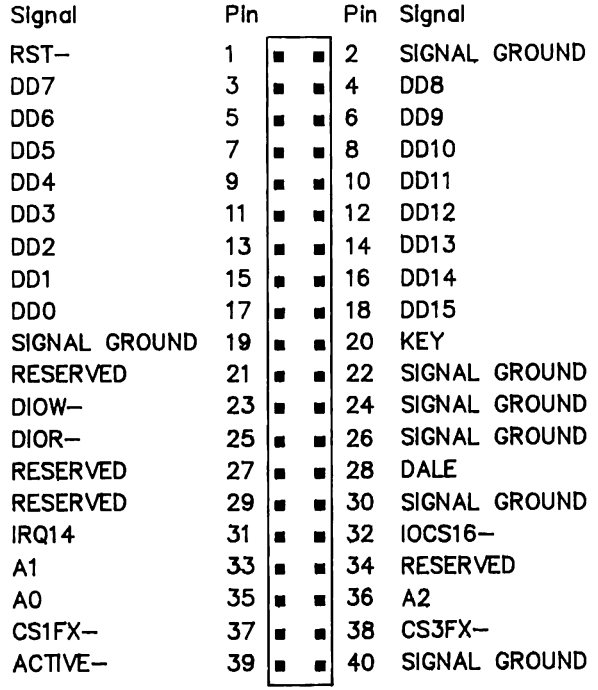


Figure 5-11. J901, Fixed Disk Drive Controller Host Adapter Connector

Table 5-16. J501, Diskette Drive Controller Signal Connector Descriptions

Signal	Pin	I/O	Description
LOW DENSITY-	2	O	Selects HIGH or LOW density for 1.2-MB diskette drives. Not used on 360-KB diskette drives.
DIRECTION-	18	O	Selects the direction to step the head when a step pulse is issued.
DISKETTE CHANGE-	34	I	Indicates that the drive door has been opened.
DRIVE 1 SELECT- DRIVE 2 SELECT- DRIVE 4(TAPE)SELECT-	14 12 6	O O O	Allows the selection of a drive so that it can respond to the interface signals.
INDEX-	8	I	(Diskette) Indicates to the drive controller that the media index opening is under the index sensor.
MOTOR1 ON-	10	O	Activates the drive motor.
MOTOR2 ON-	16	O	Activates the drive motor.
READ DATA-	30	I	This is the data-stream read from the drives and contains clock and data signals.
SIDE SELECT-	32	O	Selects Side 0 (Head 0) or Side 1 (Head 1).
STEP-	20	O	(Diskette) Tells the drive to step the heads one track.
TRACK 00-/BUSY-	26	I	(Diskette) Indicat- to the controller that the heads are at Track 0.
WRITE DATA-	22	O	This stream of data is written to the drive when WRITE GATE- signal is enabled.
WRITE GATE-	24	O	Enables the drive's write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	28	I	Indicates to the drive controller that the media is write protected.

(Continued)

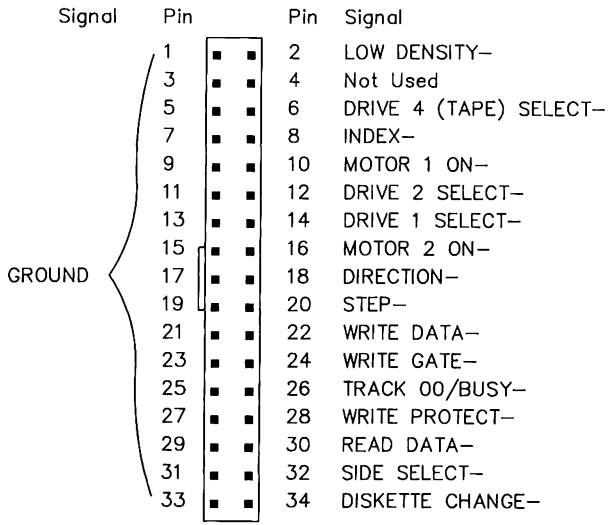


Figure 5-12. J501, Diskette Drive Controller Connector

Table 5-17. Multipurpose Fixed Disk Drive Controller Signals Used by the Diskette Drives

Controller Pin	Function	Diskette Drive 1 Pin	Function (Note 1)	Diskette Drive 2 Pin	Function	Fixed Disk Drive Back-up Pin	Function
2	DENSITY-	2	DENSITY- (Note 2)	2	DENSITY-	2	DENSITY-
4	Not used	4	Not used	4	Not used	4	Not used
6	DRIVE 4 (TAPE) SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-
8	INDEX-	8	INDEX-	8	INDEX-	8	INDEX-
10	MOTOR 1 (A) ON-	10	MOTOR 2 ON-(Note 3)	10	MOTOR 1 ON-	10	MOTOR 2 ON-
12	DRIVE 2 (B) SELECT-	12	DRIVE 1 SELECT-(Note 3)	12	DRIVE 2 SELECT-	12	DRIVE 1 SELECT-
14	DRIVE 1 (A) SELECT-	14	DRIVE 2 SELECT-(Note 3)	14	DRIVE 1 SELECT-	14	DRIVE 2 SELECT-
16	MOTOR 2 (B) ON-	16	MOTOR 1 ON-(Note 3)	16	MOTOR 2 ON-	16	MOTOR 1 ON-
18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-
20	STEP-	20	STEP-	20	STEP-	20	STEP-
22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-
24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-
26	TRACK 00-/BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-
28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-
30	READ DATA-	30	READ DATA-	30	READ DATA-	30	READ DATA-
32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-
34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-

Notes: 1. The order of the columns does not reflect the order of the connectors on the diskette disk drive cable.
2. Shaded areas denote functions unused on that drive.
3. The diskette drive cable interchanges pin 10 with pin 16 and pin 12 with pin 14 for Diskette Drive 1.

5.8 SCHEMATICS

Schematics for the multipurpose controller board are shown in Figure 5-13. Schematics for the multipurpose fixed disk drive controller board are shown in Figure 5-14. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the operation of the controller.

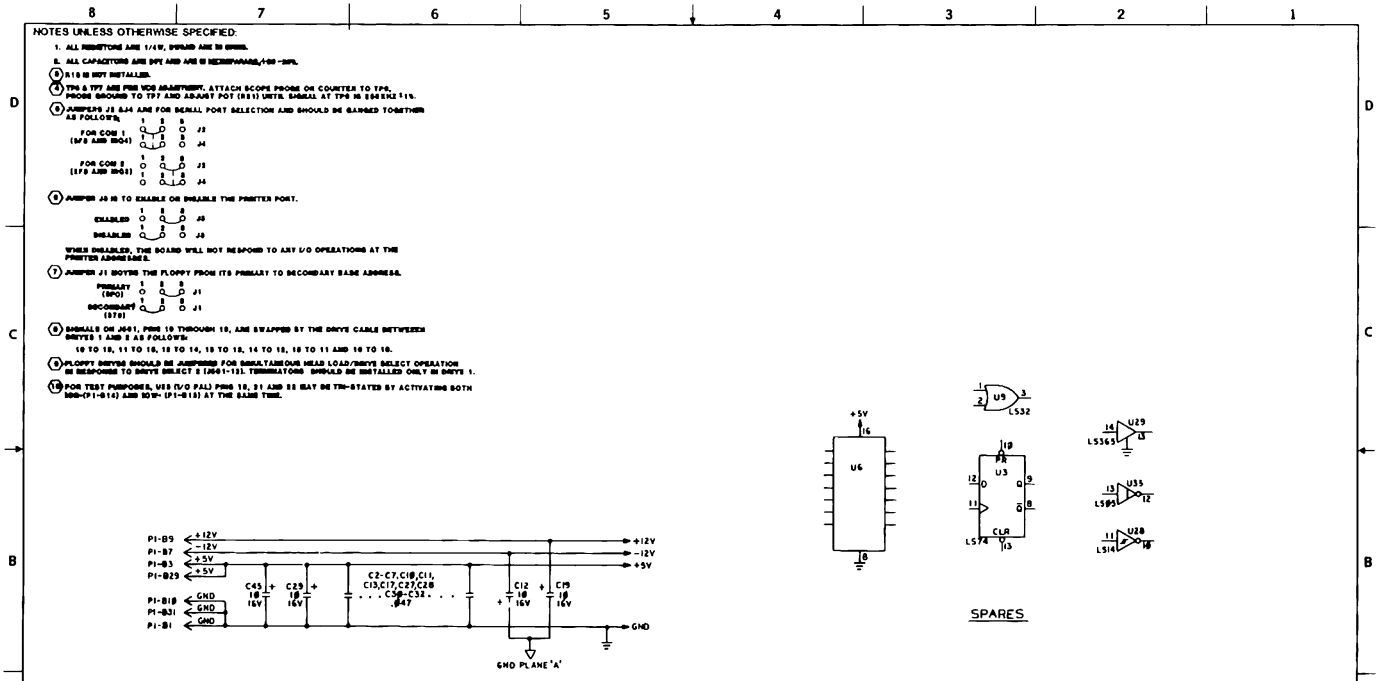


Figure 5-13. Multipurpose Controller Board Schematics (Page 1 of 4)

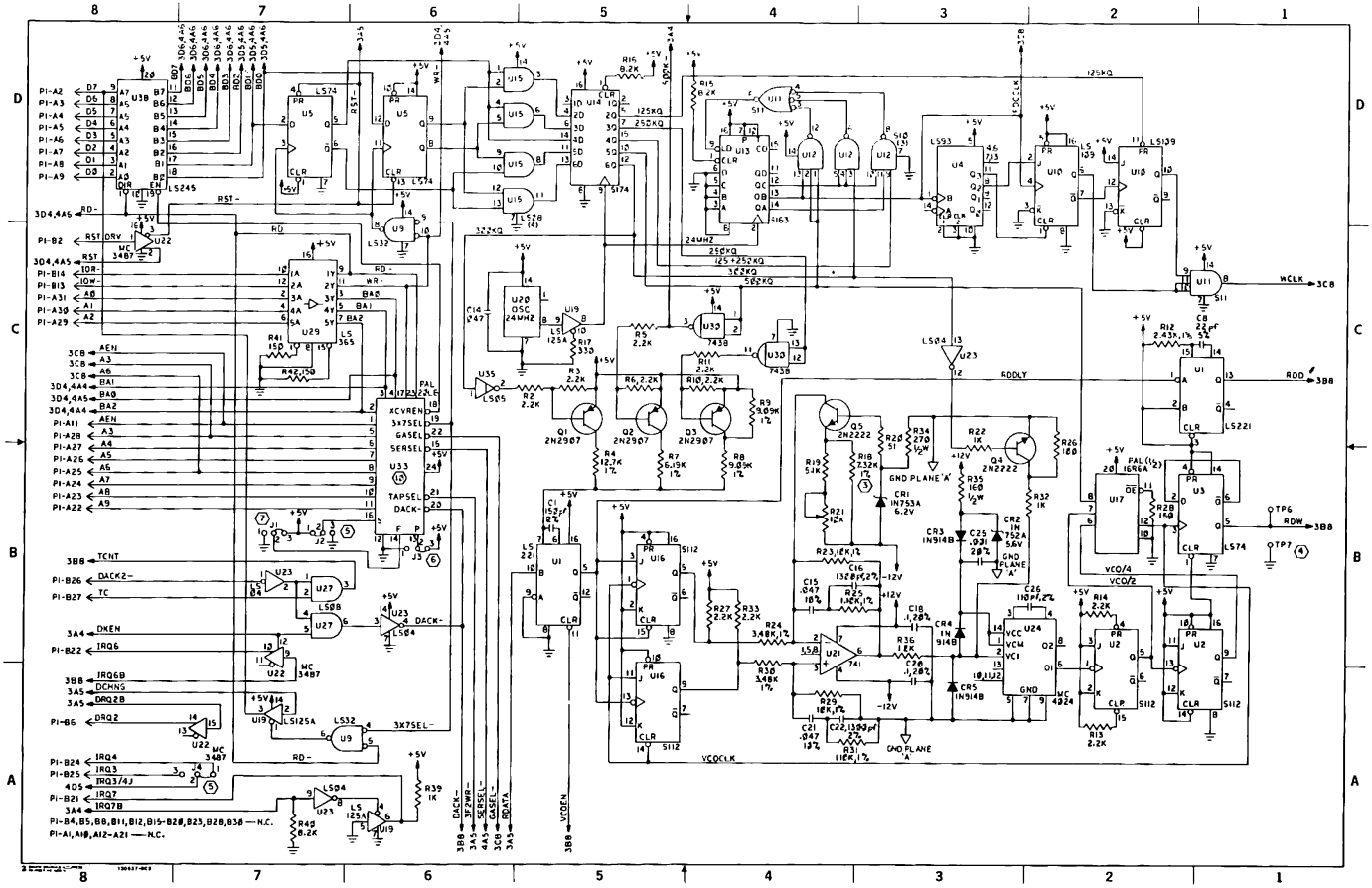


Figure 5-13. Multipurpose Controller Board Schematics (Page 2 of 4)

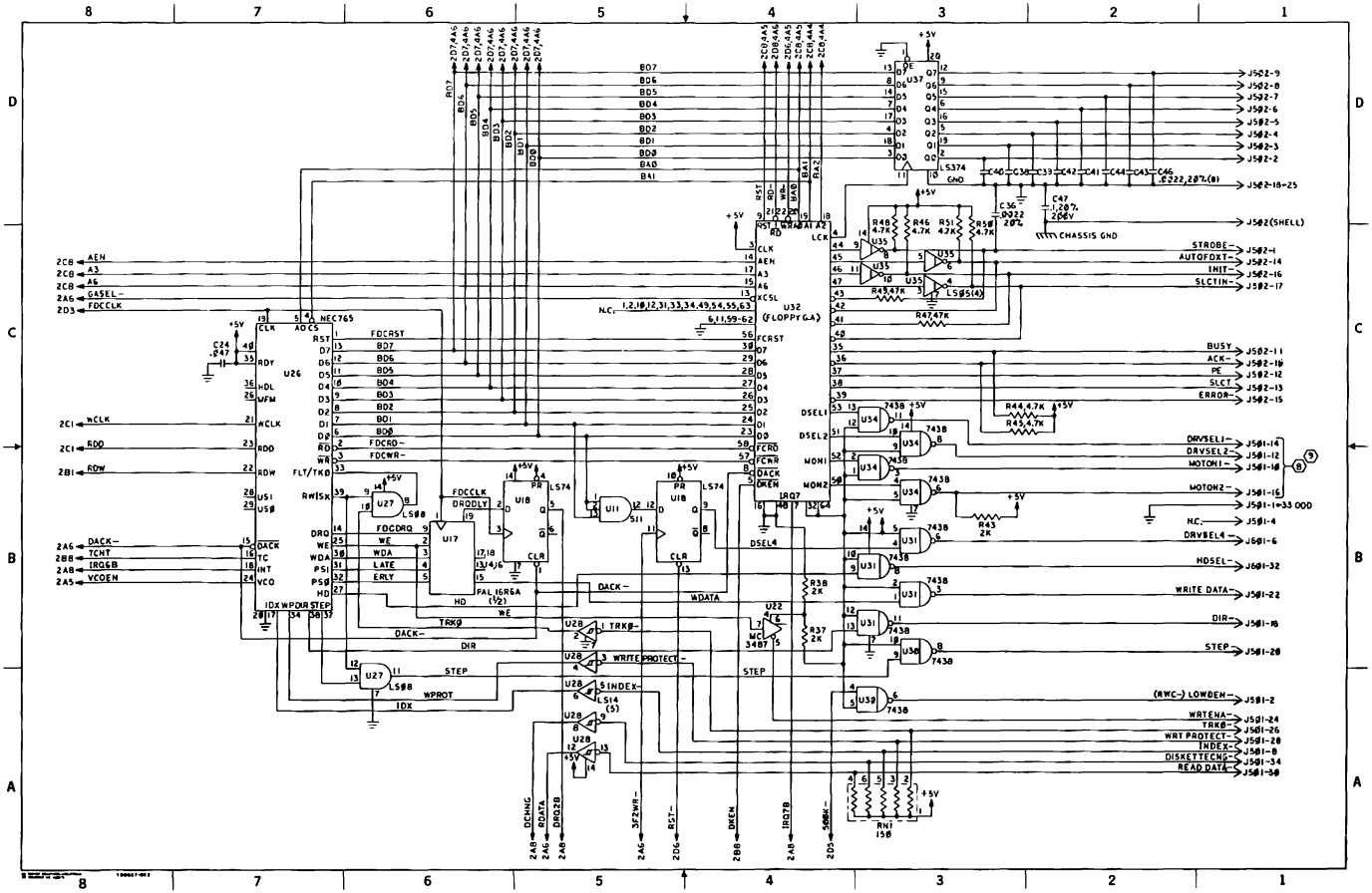


Figure 5-13. Multipurpose Controller Board Schematics (Page 3 of 4)

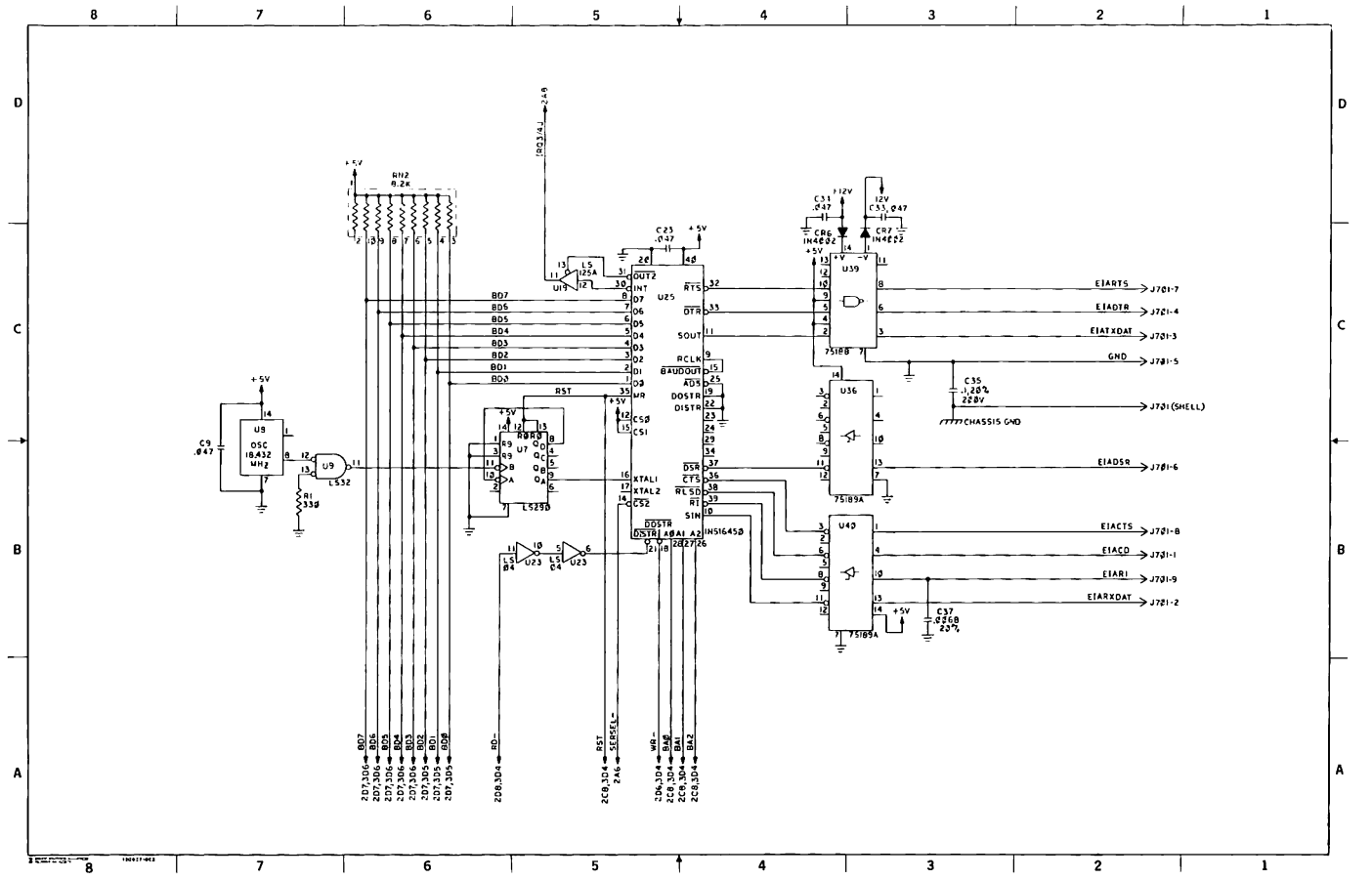


Figure 5-13. Multipurpose Controller Board Schematics (Page 4 of 4)

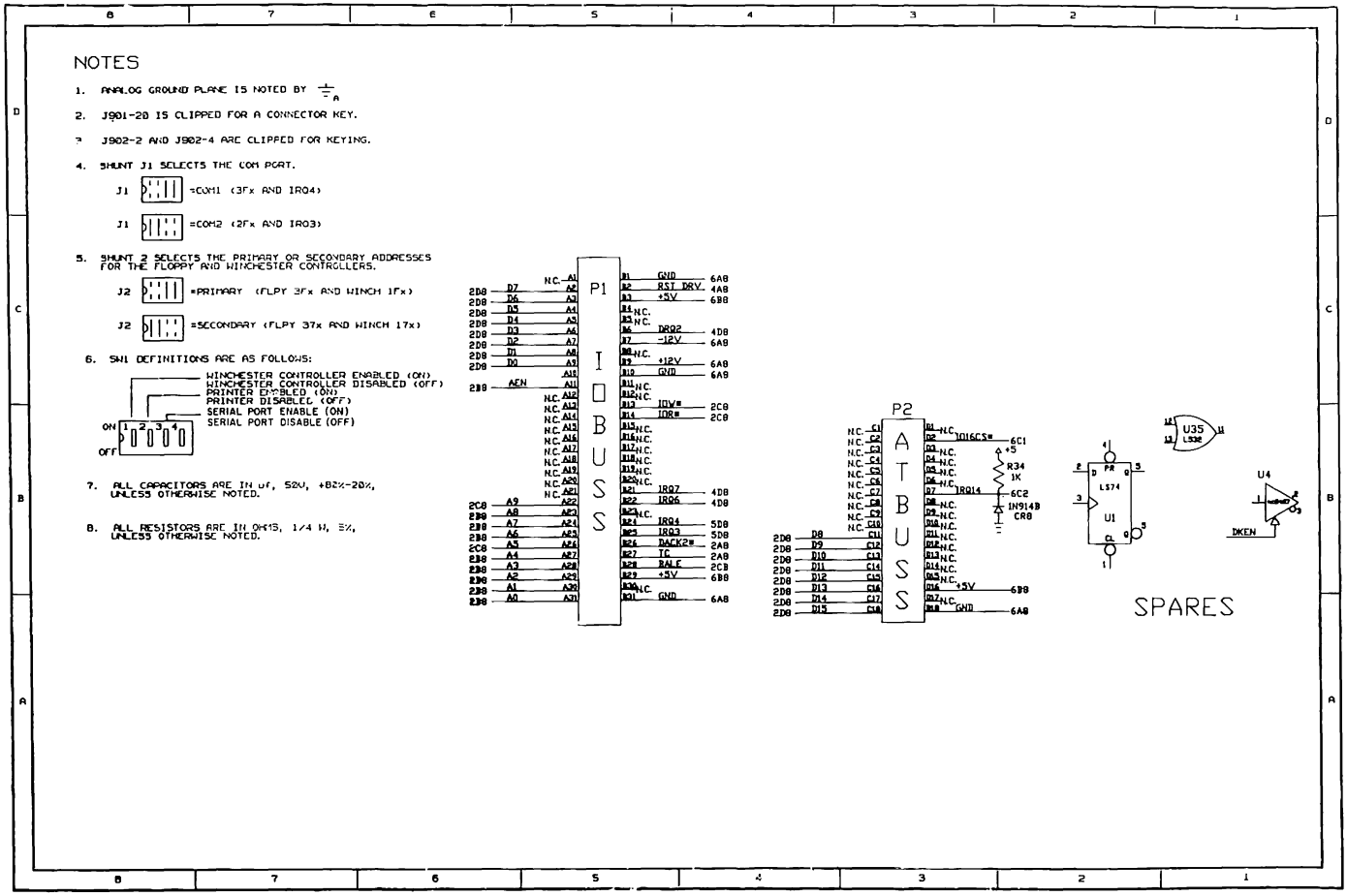


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 1 of 6)

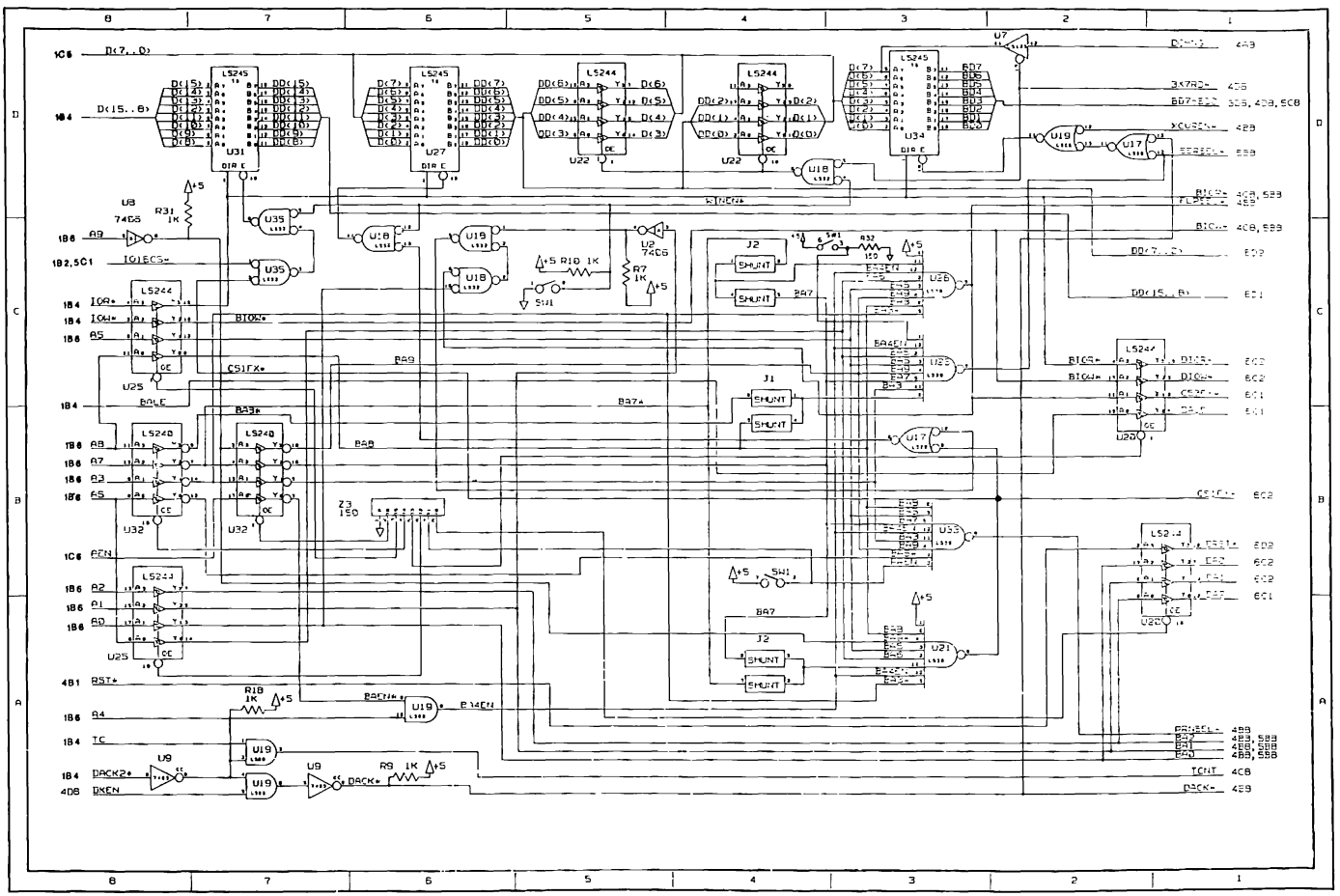


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 2 of 6)

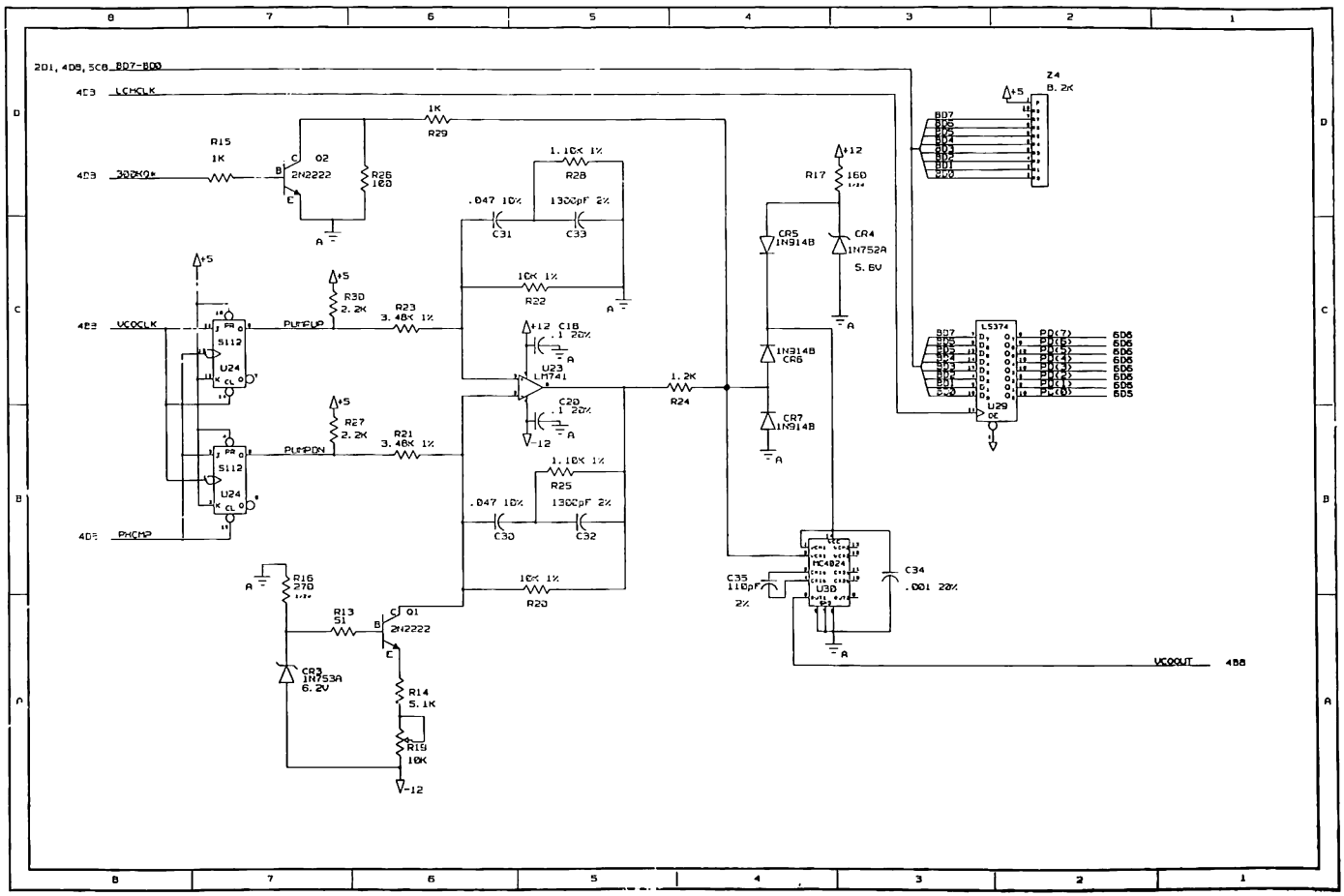


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 3 of 6)

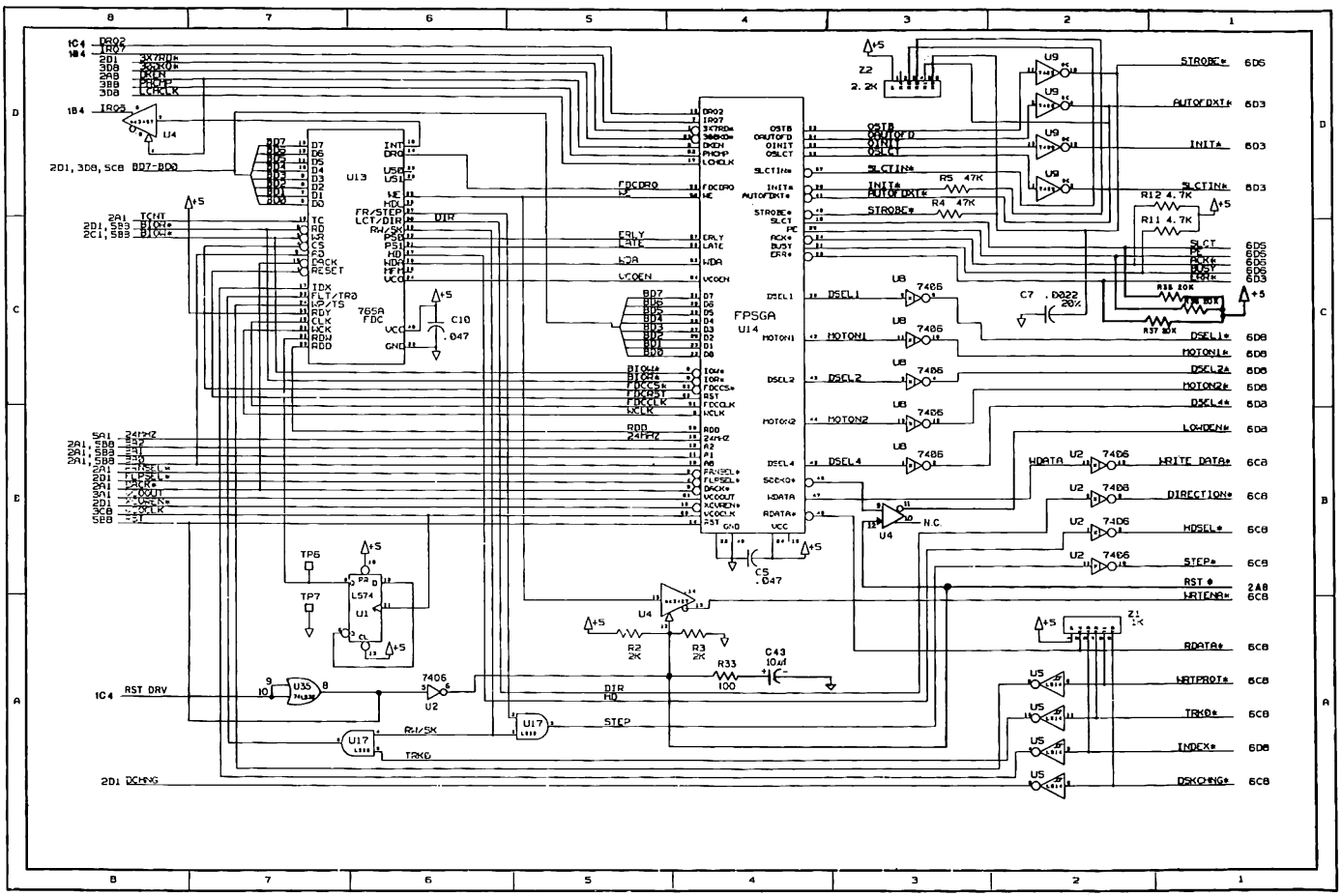


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 4 of 6)

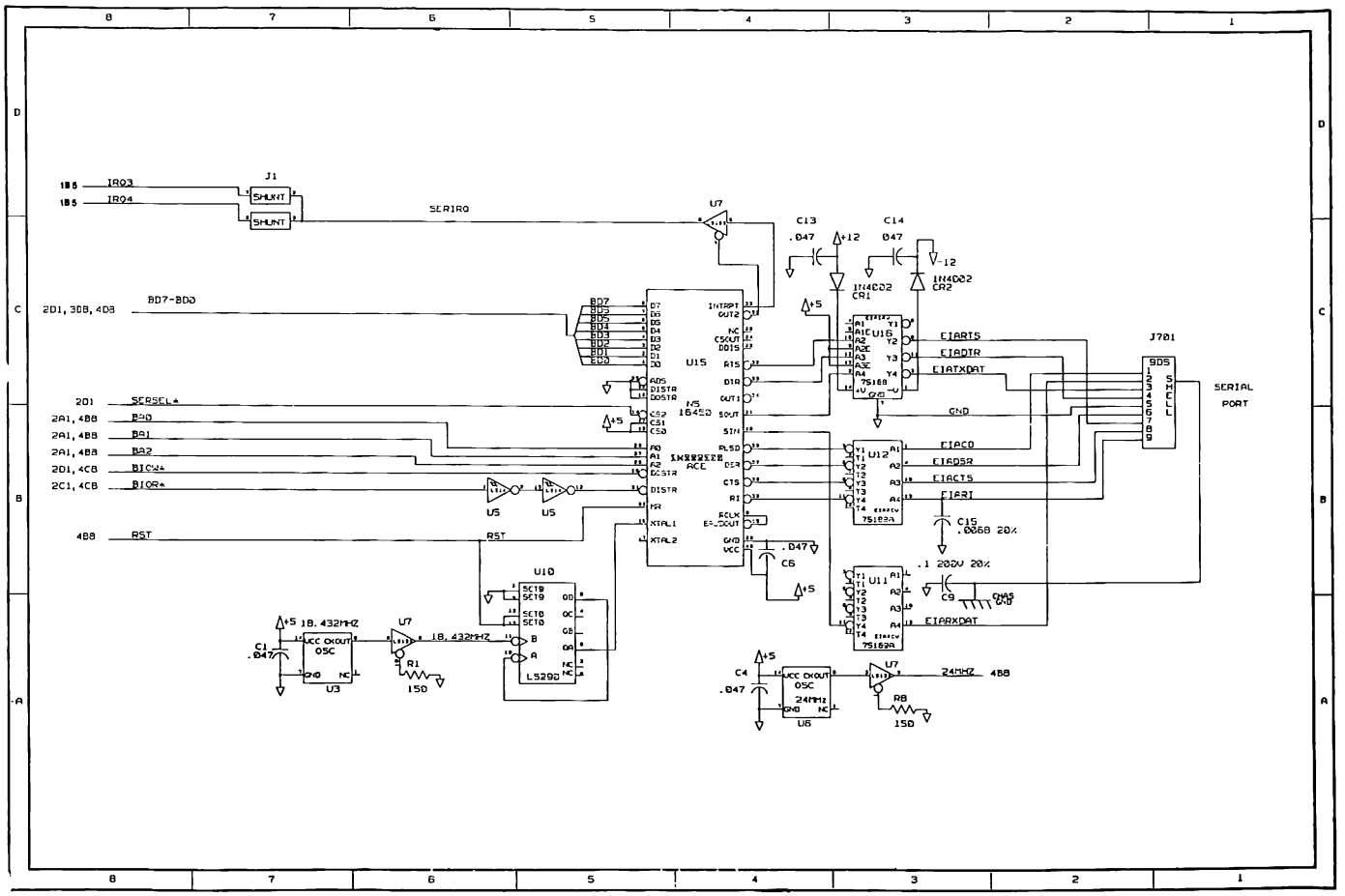


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 5 of 6)

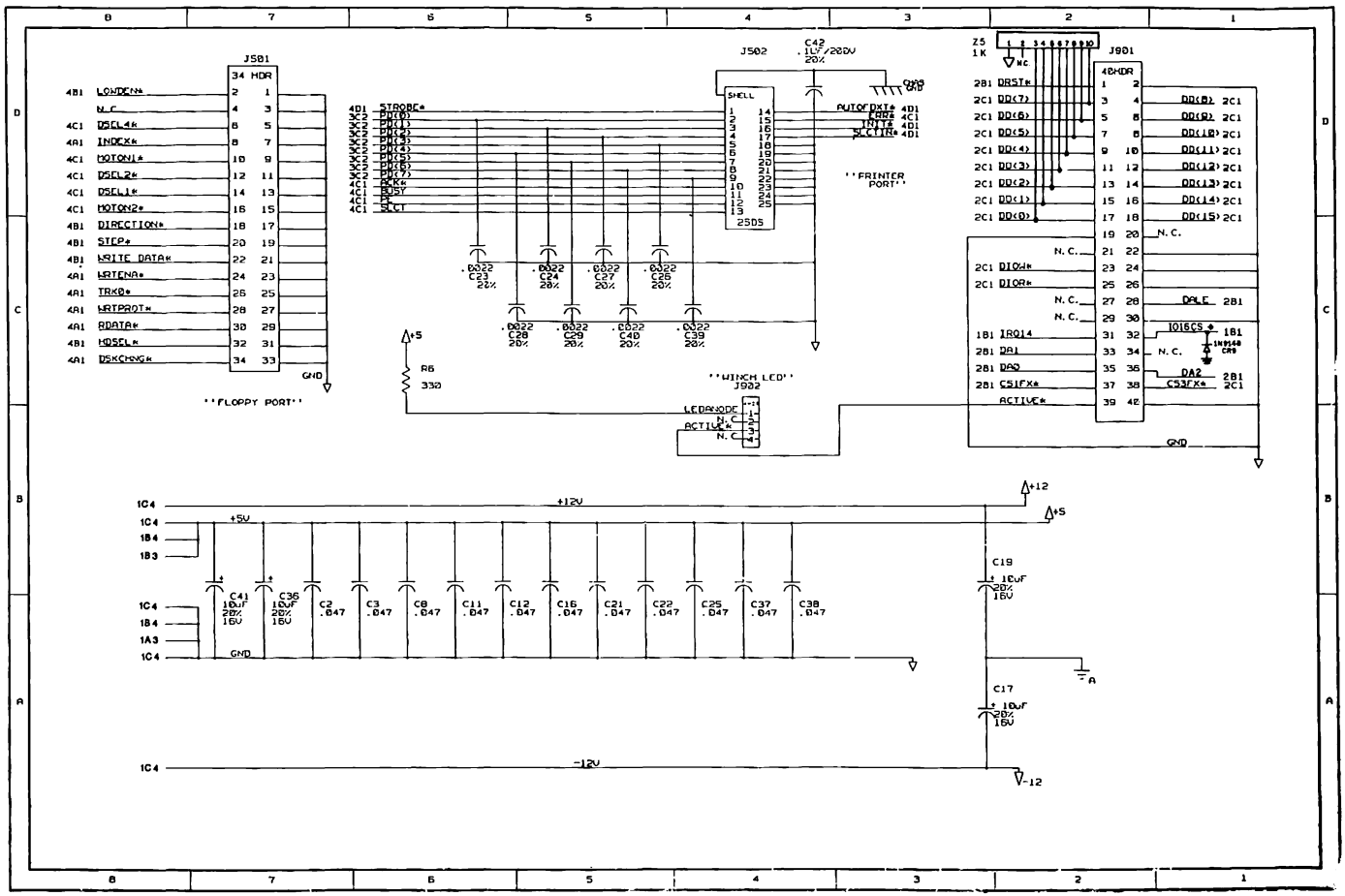


Figure 5-14. Multipurpose Fixed Disk Drive Controller Board Schematics (Page 6 of 6)

Chapter 6

FIXED DISK DRIVE CONTROLLER BOARD

Chapter 7

VIDEO DISPLAY CONTROLLER BOARDS

TABLE OF CONTENTS

CHAPTER 7
VIDEO DISPLAY CONTROLLER BOARDS

Chapter 7
VIDEO DISPLAY CONTROLLER BOARDS

7.1 INTRODUCTION

The video display controller board (Figure 7-1) provides a way to display information on one of several types of CRT displays. The video display controller board is functionally identical in both the COMPAQ PORTABLE 286® and the COMPAQ DESKPRO 286® Personal Computers.

The video display controller board has the following features:

- Dual-mode displays
- Updatable Display without blanking
- Socketed character-generator ROM
- Color-graphics capabilities
- Lightpen capability
- Composite-video capability

There are three versions of the video display controller board. All three versions are functionally identical. The Video Display Controllers are shown in Figures 7-1, 7-2 and 7-3.

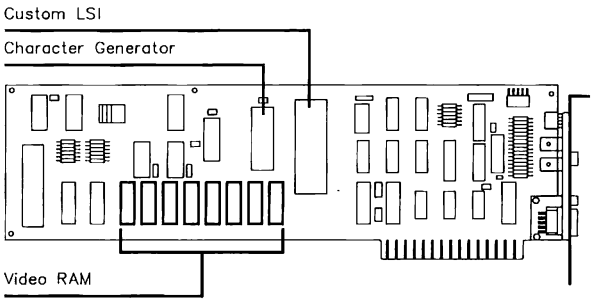


Figure 7-1. Version 1 of the Video Display Controller Board

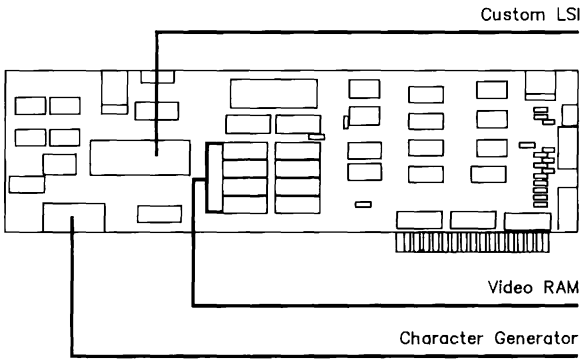


Figure 7-2. Version 2 of the Video Display Controller Board

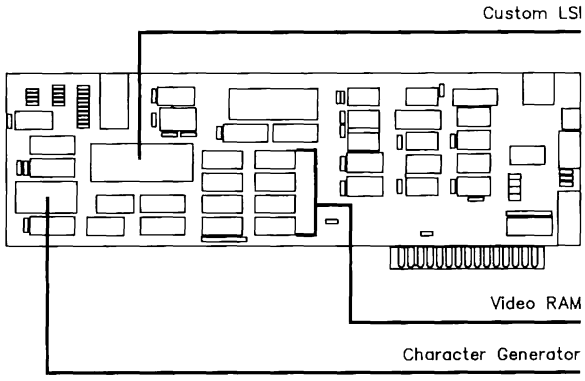


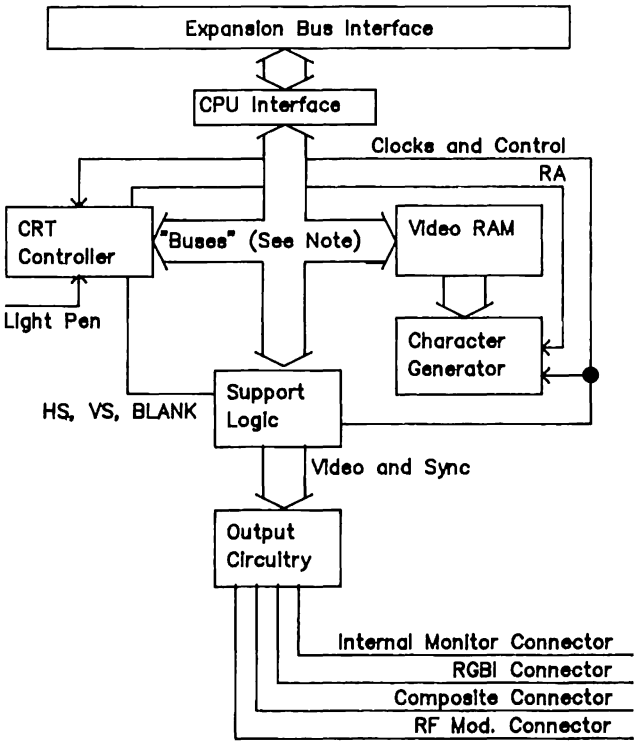
Figure 7-3. Version 3 of the Video Display Controller Board

7.2 FUNCTIONAL DESCRIPTION

The video display controller board consists of 6 major functional blocks:

- The CPU Interface
- CRT Controller
- Support Logic
- Video Memory
- Character Generator
- Output Circuitry

Figure 7-4 shows the functional block diagram of the Video Display Controller Board.



Note: "Buses" includes the address, data, control, and decode buses.

Figure 7-4. Video Display Controller Board Functional Block Diagram

The following sections briefly describe each functional block.

CPU Interface

The CPU interface consists of address decoding logic, address bus buffers, and data bus transceivers. The video display controller board uses the 8-bit bus to interface with the CPU. It does not require the full 16-bit bus expansion slot.

Address lines, together with the bus control signals, are used to decode valid I/O devices. The output lines of the decoders select the 6845, video memory, and other functions. The decoders also provide control of the data bus transceiver.

The interface circuitry allows shared access of video memory between the CPU and the 6845 by multiplexing address lines to the video memory. The CPU can access the video memory at any time without interfering with the display.

The interface circuitry also provides buffering for the reset signal and the 14.318 MHz clock.

Optional jumpers J7 and J8 select a base I/O port address of 3DXh (standard) or a base I/O port address of 3BXh. Optional jumper J9 selects a base memory address for the video memory of B8000h (standard) or B0000h.

CRT Controller

The CRT controller (6845) is an LSI device that generates the addresses and other signals that refresh the video memory. It also supplies the synchronization and blanking signals for the output circuitry.

The 6845 device contains 19 internal registers, all of which are I/O-mapped. The system BIOS programs the internal registers that control the display timing.

The 6845's lightpen register allows lightpen interactions for systems with monitors that are optically compatible (dual-mode monitors are not compatible due to their medium-persistence phosphor).

Support Logic

The support logic consists primarily of a custom LSI circuit that provides several video functions, including:

- Converting data bytes from the video memory or the character generator into the individual dots on the display (shift register or serialization).
- Controlling the application of the associated video attributes and conditions. The Mode and Color registers, and part of the Status register are part of this device.
- Generating the memory timing and other clock signals for the 6845.

The support logic selects the high- or low-scan mode according to the character-height parameter written to the 6845's internal register 09h. A value of 0Dh in register 09h selects the high-scan mode.

Video Memory

The video memory on the video display controller board consists of 16 Kbytes of dynamic RAM beginning at address B8000h and extending to BBFFFh (Figure 7-5). The video memory is dual-ported so that the CPU can access it at any time without causing visual anomalies on the CRT display.

One wait state is automatically inserted on all video memory cycles by asserting the I/O READY- line on the expansion bus. The wait state is required for synchronization purposes. The base address of video memory can be changed from B8000 (standard) to B0000 (optional Jumper J9).

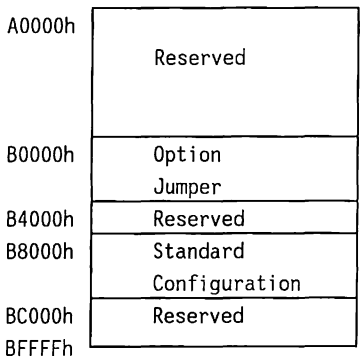


Figure 7-5. Video Memory Address Space

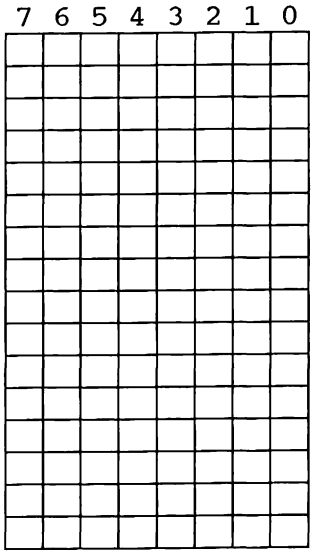
Character Generator

The character generator is an 8 Kbyte x 8 static ROM chip. Special character sets may be supported by replacing the standard ROM (socketed) with a 250 ns, 2764-type EPROM. The CPU cannot read the ROM's contents--it is accessed only by the 6845, together with video RAM.

The 8 Kbyte x 8 character generator ROM contains three character sets of 256 characters each. The first set is used for the 9 x 14 dot cell character set and takes up 4 Kbytes. From each group of 16 bytes, 14 are used to form the cell, with bytes +00h through +05h for the lower six displayed lines, and bytes +08h through +0Fh for the top eight scan lines. Scan line 0 is adjacent on the screen to scan line 13 of the character above.

The video display controller board generates a 9th horizontal dot from an 8-bit-wide ROM for 9 x 14 dot cells. It replicates bit 0 (the 8th dot) for graphics characters C0h through DFh. It places a blank dot in the 9th position for other characters. This scheme allows continuous horizontal lines and solid figures needed by certain graphics symbols.

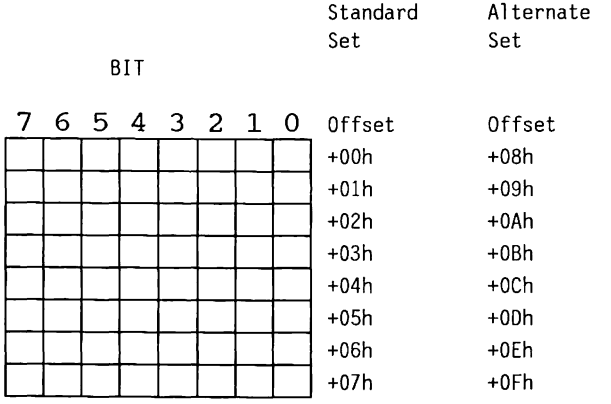
The layout of the 9 x 14 dot cell is as follows:



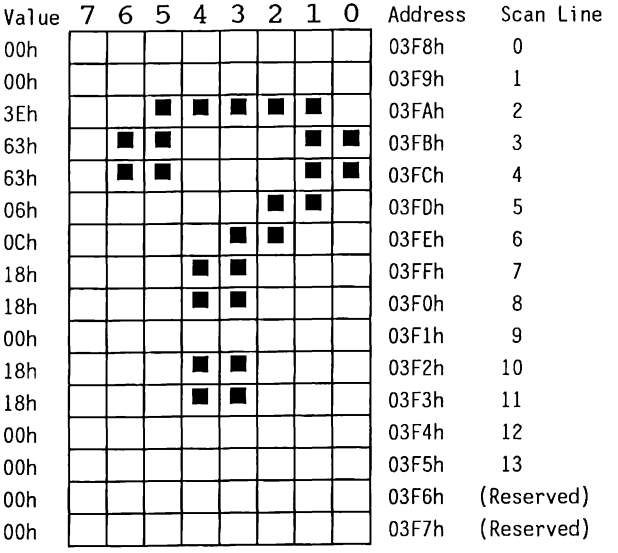
The second and third sets are interleaved and occupy the remaining 4 Kbytes. They provide standard and alternate 8 x 8 dot versions (selectable by Jumper J1) of an 8 x 8 dot cell character font used by both 40- and 80-column low-scan text modes. Scan line 0 is adjacent on the screen to scan line 7 of the character above.

NOTE: A separate character font contained in the system ROM duplicates the first 128 standard 8 x 8 dot cells and is used by ROM BIOS routines to display text in one of the graphics display modes.

The second and third character sets in the character generator ROM have 8 x 8 dot cells and are interleaved every eight bytes. That is, the standard set begins at offset 1000h, and the alternate set begins at 1008h. The layouts are as follows:



Example: Question mark (ASCII 3Fh) in the 9 x 14 dot cell.



NOTE: The bytes at addresses 03FBh and 03FCh have the least-significant bit = 1, but this bit is not right-extended into the 9th column because '?' lies outside of the special range C0h through DFh.

Example: Question mark (ASCII 3Fh) in the standard 8 x 8 dot cell.

Value	7	6	5	4	3	2	1	0	Address	Scan Line
78h		■	■	■	■				13F0h	0
CCh	■	■			■	■			13F1h	1
0Ch					■	■			13F2h	2
18h				■	■				13F3h	3
30h			■	■					13F4h	4
00h									13F5h	5
30h			■	■					13F6h	6
00h									13F7h	7

Example: Question mark (ASCII 3Fh) in the alternate 8 x 8 dot cell.

Value	7	6	5	4	3	2	1	0	Address	Scan Line
3Ch			■	■	■	■			13F8h	0
42h		■					■		13F9h	1
02h							■		13FAh	2
04h						■			13FBh	3
08h					■				13FCh	4
00h									13FDh	5
08h					■				13FEh	6
00h									13FFh	7

Output Circuitry

The output circuitry contains the logic and buffers required to interface the video display controller board with a video display. The output circuitry can directly drive a composite video monitor, an internal monitor (COMPAQ PORTABLE 286 only), an RGBI TTL input monitor, or a television, using an external RF modulator (not supplied).

The RGBI, composite, and RF modulator outputs are normally only active in the low-scan mode. The internal monitor interface is always enabled. When COMPAQ Dual-Mode Monitors are used with the COMPAQ DESKPRO 286, Jumpers J3 and J5 are set to enable all video outputs for both modes.

7.3 PROGRAMMING THE VIDEO DISPLAY CONTROLLER BOARD

The video display controller board is an I/O-mapped and memory-mapped (video memory) board. Table 7-1 lists the I/O addresses.

Table 7-1. Video Display Controller Board I/O Addresses

I/O Addr.	Read or Write	Register Description
3D4h	W	6845 Index
3D5h	R/W	6845 Data
3D8h	W	Mode
3D9h	W	Color
3DAh	R	Status
3DBh	W	Reset Lightpen
3DCh	W	Set Lightpen

6845 INDEX AND DATA REGISTERS (3D4h AND 3D5h)

The 6845 CRT controller is addressed as two port addresses. One port (3D4h) accesses the Index register. The other port (3D5h) accesses the Data register.

The CRT controller has 19 internal registers. The Index register counts as one of these, although it serves as a pointer to the other registers.

To write to or read from, a 6845 register:

1. Load the 6845's register number into the Index register (3D4h).

2. Write or read the byte to/from the Data register (3D5h).

The registers pointed to with Index register values of 00h to 0Bh directly control the timing of the CRT controller and the associated waveform profiles which drive the display monitors. Before changing any of the default parameters in these registers, be sure that the environment is understood (i.e., which monitors are connected to the video display controller and the timing that each display requires) for proper operation.

The initial register values are listed in Table 7-2.

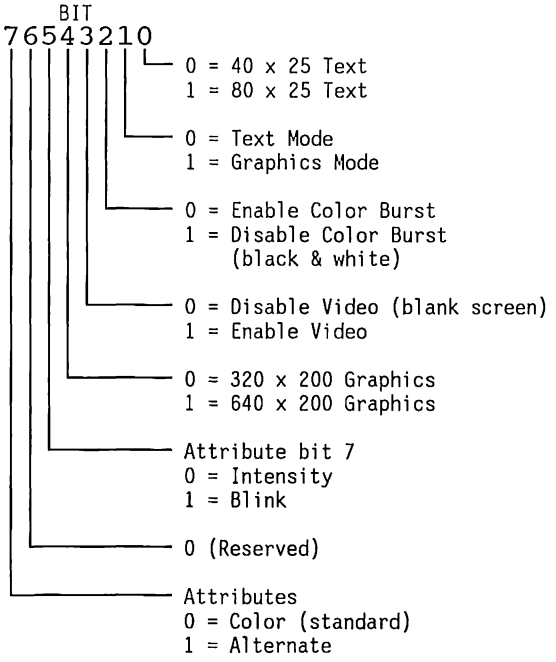
Table 7-2. Initial Values for 6845 Internal Registers

Index Reg.	Register Description	Read or Write	Recommended Values (Default) 40x25 Low-Scan	80x25 High-Scan	80x25 Low-Scan	Graphics Low-Scan
00h	Horizontal Total (characters)	W	38h	71h	71h	38h
01h	Horizontal Displayed (characters)	W	28h	50h	50h	28h
02h	Horizontal Sync Position (characters)	W	2Dh	5Ah	5Ah	2Dh
03h	Horizontal Sync Width (characters)	W	0Ah	0Ah	0Ah	0Ah
04h	Vertical Total (rows)	W	1Fh	19h	1Fh	7Fh
05h	Vertical Total Adjust (lines)	W	06h	06h	06h	06h
06h	Vertical Displayed (rows)	W	19h	19h	19h	64h
07h	Vertical Sync Position (rows)	W	1Ch	19h	1Ch	70h
08h	Interlace Mode & Skew	W	02h	02h	02h	02h
09h	Character Height (lines)	W	07h	0Dh	07h	01h
0Ah	Cursor Start (line)	W	06h	0Bh	06h	06h
0Bh	Cursor End (line)	W	07h	0Ch	07h	07h
0Ch	Display Start Address (high)	R/W	00h	00h	00h	00h
0Dh	Display Start Address (low)	R/W	00h	00h	00h	00h
0Eh	Cursor Address (high)	R/W	00h	00h	00h	00h
0Fh	Cursor Address (low)	R/W	00h	00h	00h	00h
10h	Lightpen Address (high)	R	XXh	XXh	XXh	XXh
11h	Lightpen Address (low)	R	XXh	XXh	XXh	XXh

Note: Recommended values apply to COMPAQ Monitors.
chrs = characters (i.e., character count)
lines = horizontal scan lines elements which make up a character row
row = vertical character units (i.e., row = 8 or 14 lines)
X = undefined

MODE REGISTER (3D8h, WRITE-ONLY)

This register selects the current video-display mode in conjunction with other 6845 registers.



Bit 0. If bit 0 = 0, text is displayed in a 40-column mode. In the 40-column modes, the clock for the video and timing logic is divided by two.

If bit 0 = 1, text is displayed in an 80-column mode.

Bit 1. If bit 1 = 0 , the text mode is selected.

If bit 1 = 1, the bit-mapped graphics mode is selected.

Bit 2. If bit 2 = 0, color encoding on the composite video output is enabled. This bit only affects the composite video outputs; the other video outputs are unaffected.

If bit 2 = 1, the reference color burst signal for the composite video output is disabled (black and white display).

Bit 3. If bit 3 = 0, the entire display is blanked, but the sync signals are still active.

If bit 3 = 1, the screen is displayed normally.

Bit 4. If bit 4 = 0, the display format is 320 x 200 in the graphics modes.

If bit 4 = 1, the display format is 640 x 200 in the graphics modes (Mode register bit 1 = 1).

The 640 x 200 mode is a 1 bit-per-pixel format, while the 320 x 200 mode is 2 bits per pixel.

Bit 5. This bit has meaning in the text modes only.

If bit 5 = 0, then bit 7 of the text-attribute byte controls the background intensity function.

If bit 5 = 1, then bit 7 of the text-attribute byte controls the blinking function.

Bit 6. Reserved (always 0).

Bit 7. This bit has meaning in the text modes only.

If bit 7 = 0 (standard), the text is displayed with the color attributes (color foreground and background). See the section on video display modes.

If bit 7 = 1, the text is displayed with the alternate attributes that defines a white or black foreground or background and text underlining capability. This mode is only available when in the high-scan mode. The low-scan mode uses the color attributes regardless of the state of this bit.

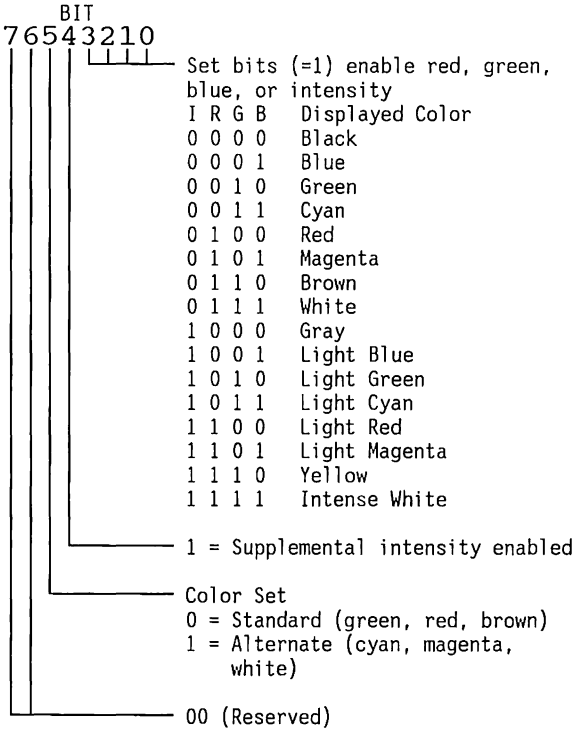
COLOR REGISTER (3D9h, WRITE-ONLY)

The Color register specifies:

- A mode-dependent color for the background, foreground, or border
- Supplemental video intensity
- Standard or alternate color set for the 320 x 200 graphics mode

The color displayed on the screen is a result of the Color register values and the colors specified in video memory for each display location.

In the two graphics modes, either 1 or 4 colors may be displayed at once. In the text modes, 16 foreground and 8 background colors can be displayed simultaneously.



Bits 3..0. These four bits select a mode-dependent color.

In the 640 x 200 graphics mode, they select the color of an active pixel.

In the 320 x 200 graphics mode, they select the color of an inactive pixel, or background.

In the 40 x 25 text mode, they select the color of the overscanned border.

Bit 4. If bit 4 = 0, unintensified colors are selected for both the 320 x 200 graphics mode and the background colors in the text modes.

If bit 4 = 1, intensified colors are selected for both the 320 x 200 graphics mode, and background colors in the text modes.

Bit 5. Selects the color set used in the 320 x 200 graphics mode.

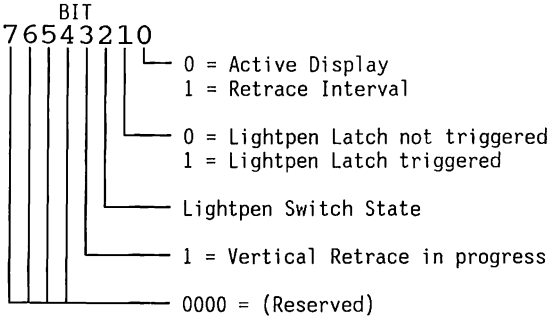
If bit 5 = 0, the standard color set is selected. The standard set consists of green, red, and brown.

If bit 5 = 1, the alternate color set is selected. The alternate set consists of cyan, magenta, and white.

Bits 7..6. Bits 7 and 6 are always 0 (reserved).

STATUS REGISTER (3DAh, READ-ONLY)

The Status register contains real-time event status information.



Bit 0. If bit 0 = 0, the video raster is on the active (displayed) area of the screen

If bit 0 = 1, the video raster is in a horizontal or vertical retrace period

Bit 1. This bit reflects the state of the lightpen latch.

If bit 1 = 1, the lightpen has triggered--the 6845 lightpen address registers may contain a valid address. The state of the lightpen latch can be cleared by writing to port 3DBh and set by writing to 3DCh.

Bit 2. This bit reflects the state of the lightpen switch signal of the lightpen interface connector. This signal is not latched or debounced.

Bit 3. This bit reflects the state of the vertical sync signal.

If bit 3 = 1, the vertical retrace signal is active.

CLEAR OR SET LIGHTPEN LATCH (3DBh AND 3DCh, WRITE-ONLY)

By writing any value to port 3DBh, the lightpen latch bit of the Status register will be reset to 0.

By writing any value to port 3DCh, the lightpen latch bit of the Status register will be set to 1.

Bit 1 of the Status register (3DAh) defines the lightpen latch status.

7.4 VIDEO DISPLAY MODES

The video display controller board displays either graphics or text.

Text displays are character-oriented. The dot patterns for the display is stored in a character-generator ROM. Text on COMPAQ Monitors is normally displayed in the high-scan mode (see COMPAQ Dual-Mode Monitors).

Graphics displays are pixel-oriented. The color of each pixel is specified in video memory. A pixel is the smallest controllable display element--a single dot on the screen. Graphics on COMPAQ Monitors are displayed in the low-scan mode.

Figure 7-6 compares the pixel patterns for the 9 x 14 and 8 x 8-pixel text characters.

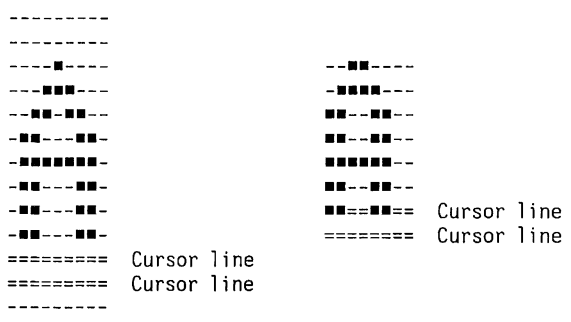


Figure 7-6. Comparison of Text Character Formats

Text Displays

For text displays, the video display controller board uses two bytes of video memory to define each character: the character byte and the attribute byte.

The character byte (even address) is sent to the character generator. The character generator provides the patterns for that character code.

The attribute byte (odd address) specifies the foreground and background color to use for the character and whether the character should be intensified or blinking (See the Mode register)

Table 7-3 lists the character codes and the resulting characters defined in the character generator. The table displays the characters in a hexadecimal format. For example, 20h is the value for the space character.

Table 7-3. Character Codes

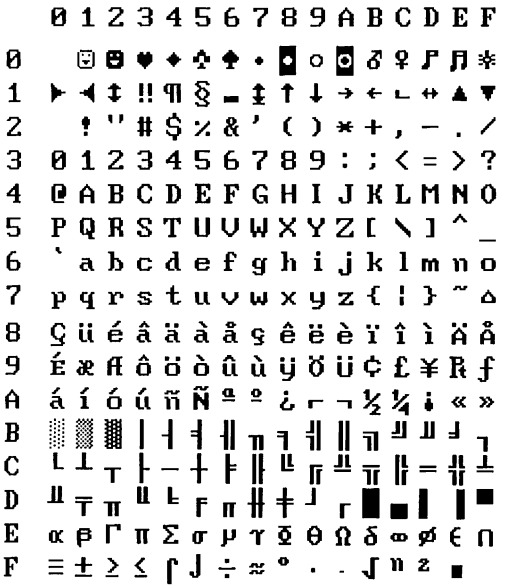


Figure 7-7 shows the text attribute byte values (with mode register bit 7 = 0).

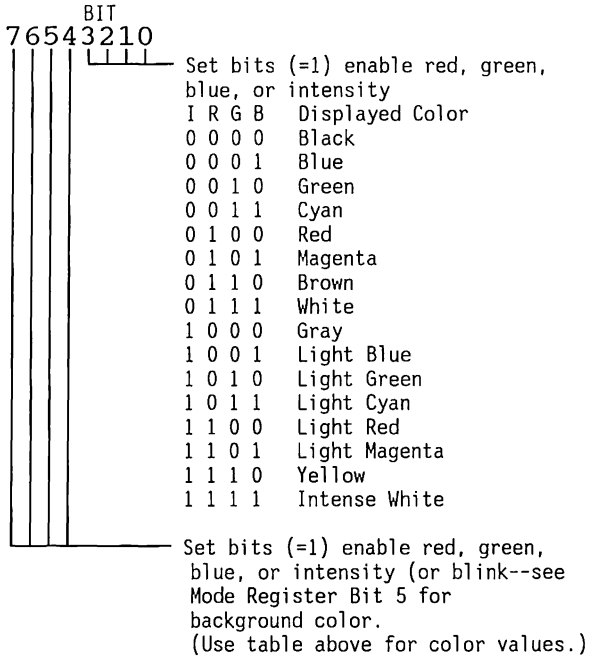


Figure 7-7. Attribute Byte for Color Text

Figure 7-8 shows the alternate text-attribute byte values (with Mode register bit 7 = 1)

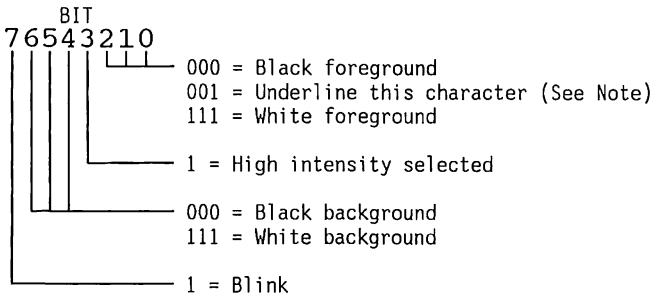


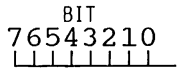
Figure 7-8. Alternate Attribute Byte (80 x 25, High-Scan Text Only)

NOTE: Hardware draws the underline by turning on all 9 pixels of scan line 13 (lowest) of the character cell.

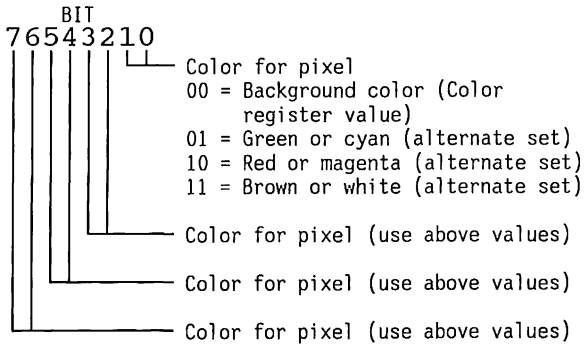
Graphics Displays

For pixel-oriented displays, the video display controller board uses video memory as the source of the patterns to display.

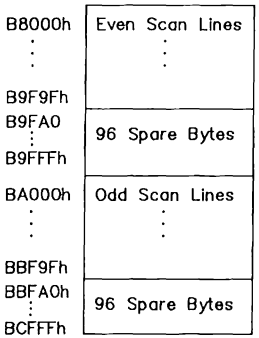
In the 640 x 200-pixel graphics mode, a single byte of video memory defines the state of eight pixels. Bit 7 is the left-most pixel on the display. The color used for active pixels is specified in the color register.



In the 320 x 200-pixel graphics mode, a single byte defines the state of four pixels (two bits per pixel). The two bits that define a pixel specify one of three colors from the standard or alternate color set or the background color. Bits 7 and 6 control the left-most pixel.



For the graphics modes, the video memory is divided into separate blocks for the even and odd scan lines. Figure 7-9 shows the format of video memory for the graphic modes.



Addresses for Graphics

Row	First Column	Last Column
1	B8000h	B804Fh
2	BA000h	BA04Fh
3	B8050h	B809Fh
4	BA050h	BA09Fh
⋮	⋮	⋮
197	B9F00h	B9F4Fh
198	BBF00h	BBF4Fh
199	B9F50h	B9F9Fh
200	BBF50h	BBF9Fh

Figure 7-9. Format of Video Memory for the Graphic Modes

7.5 MONITORS SUPPORTED

The video display controller board supports four types of monitors:

- COMPAQ Dual-Mode Monitors.
- Red-Green-Blue (RGB) color monitors that connect to the standard DB-9 (9-pin) connector, including the COMPAQ Color Monitor in 200-line Mode.
- Monochrome or color monitors that require composite-video signals may use an RCA-type connector or a recessed Berg connector.

COMPAQ Dual-Mode Monitors

The standard COMPAQ monitor is dual-mode. Dual-mode means that there are two different display modes, with different scanning frequencies for each mode.

The high-scan mode has a horizontal scan frequency of 18.5 kHz and a vertical scan frequency of 50 Hz, non-interlaced. High scan supports the text modes, using a 9 x 14-pixel character block. This mode has 350 active vertical lines for 25 rows of 14-pixel high characters, and 720 horizontal pixels for 80 columns of 9-pixel wide characters.

When the high-scan mode is selected, the monitor mode line switches to select the 9 x 14 character set in the character generator.

The low-scan mode has a horizontal frequency of 15.7 kHz, and a vertical frequency of 60 Hz, non-interlaced. This mode is compatible with most television and RGB displays that use 200 active scan lines. The low-scan mode uses an 8 x 8 character block for text, and is the only mode used for graphics.

To select the high-scan mode, program the 6845 according to the "80 x 25 High Scan" column in Table 7-6.

Characters are displayed in the 80 x 25-character format, with a 9 x 14-dot matrix on COMPAQ Dual-Mode Monitors, or an 8 x 8-dot matrix using other monitors.

COMPAQ Dual-Mode Monitors can accept two scan (sync) frequencies from the video display controller board. One scan mode displays high-quality text (9 x 14-pixel characters). The other mode displays graphics.

The high- and low-scan modes can also be easily accessed using either of the following methods:

- Keyboard selection (using COMPAQ MS-DOS and XENIX) Simultaneously pressing the multiple key combination of CTRL, ALT, and < (LESS THAN) keys will switch into low-scan mode. Simultaneously pressing the multiple key combination of CTRL, ALT, and > (GREATER THAN) keys will switch into high-scan mode.
- COMPAQ MS-DOS, Version 3 MODE Command. Refer to MS-DOS Version 3 Reference Guide for more information on the MODE command.

RGBI Monitors

RGBI monitors receive their video signals in the form of separate lines for the red, green, and blue colors, intensity, horizontal sync, and vertical sync. These are all TTL-level signals. With four signals (red, green, blue, and intensity) to specify color, 16 colors or shades of gray are available. Monitors that do not support the intensity signal are limited to eight colors.

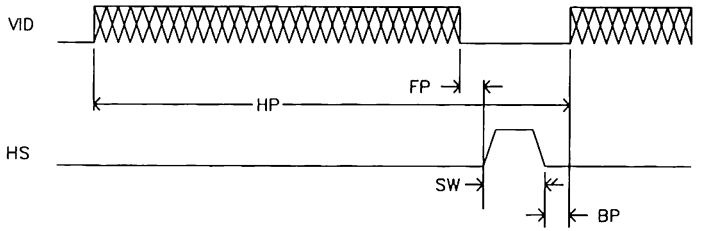
The COMPAQ Color Monitor is compatible with this video display controller board. However, it is restricted to only the 200-scan line, 16 color operation.

Composite Video Monitors

Composite video monitors, or other video equipment with composite video inputs, connect to the RCA-type jack provided on the mounting bracket. If a monochrome display is used, disable the color burst signal to reduce interference.

An external RF modulator can be connected to either the RCA-type connector or the recessed Berg connector for use with television receivers. The Berg connector provides the same video signal as the RCA-type connector plus a +12 volt power connection. Due to television bandwidth limitations, 80-column television displays are not recommended.

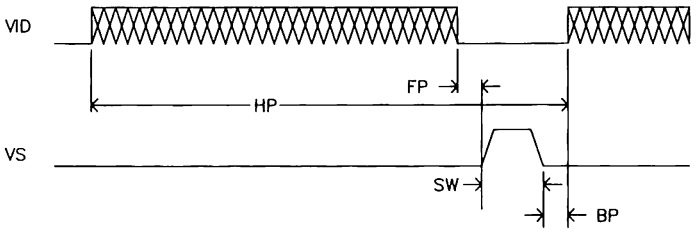
Figure 7-10 shows the timing characteristics for the horizontal sync signals.



Symbol	Parameter	High Scan (Hi Res)	Low Scan (Graphics)
HP	Horizontal Period	54.1 µs	63.7 µs
FP	Front Porch	5.7 µs	6.7 µs
SW	Sync Width	3.8 µs	4.5 µs
BP	Back Porch	6.6 µs	7.8 µs

Figure 7-10. Horizontal Timing

Figure 7-11 shows the timing characteristics for the vertical sync signals.



Symbol	Parameter	High Scan (Hi Res)	Low Scan (Graphics)
VP	Vertical Period	20.00 ms	16.68 ms
FP	Front Porch	0.00 ms	1.53 ms
SW	Sync Width	0.16 ms	0.19 ms
BP	Back Porch	0.92 ms	2.23 ms

Figure 7-11. Vertical Timing

Figure 7-12 shows the characteristics for the video connectors.

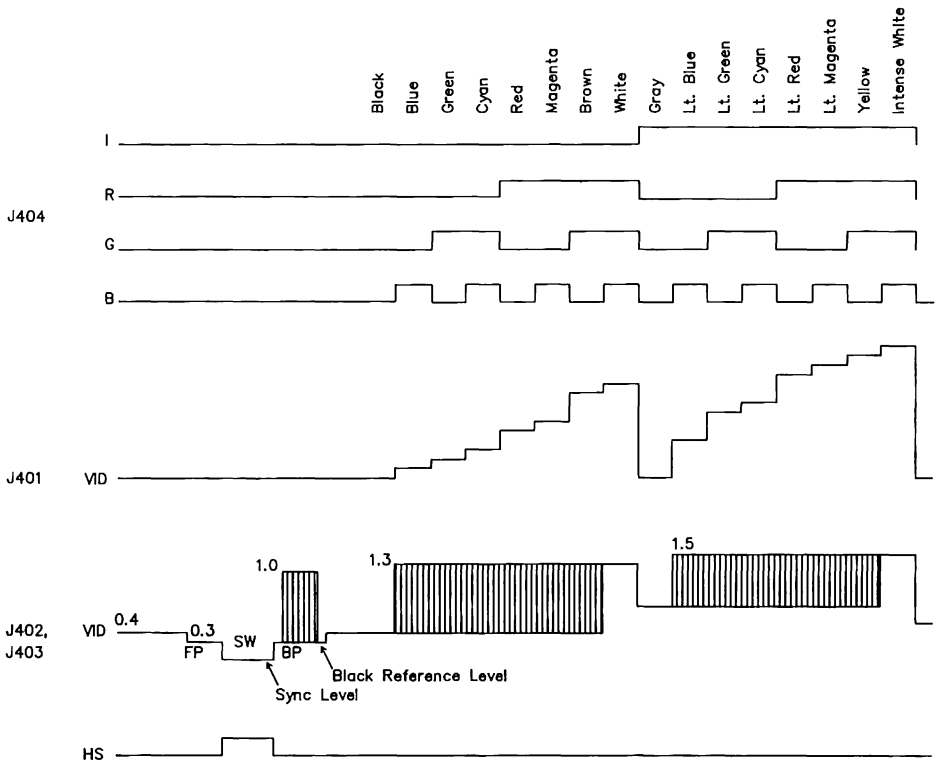


Figure 7-12. Video Display Controller Board Output Signal Waveforms

7.6 JUMPERS

Jumpers J1 through J9 are identical on all three video display controller boards. Two additional Jumpers, J10 and J11 have been added to the Version 3 video display controller board to enable the additional 16 Kbytes of RAM provided by the dynamic RAM devices on the controller

Jumpers J1 through J9 change the configuration of the video display controller board. Only J3 and J5 have pins and shorting blocks installed. The remaining jumpers are etched on the controller board.

Table 7-4 lists the jumpers for all three video display controller boards. The jumper arrangement is shown in Figures 7-13 through 7-15.

CAUTION

Modifying etched jumpers invalidates the COMPAQ warranty of the board.

Table 7-4. Jumpers on the Video Display Controller Board

J1 - 8 x 8 Character Set Jumper

The character generator ROM contains two complete sets of 8 x 8 dot lookup tables. The standard table is suitable for all types of monitors. The alternate table provides sharper character sets for 40-column displays on televisions. This jumper is etched on the board.

J1	Configuration
2-3	Standard 8 x 8 cell
1-2	Alternate 8 x 8 cell

(Continued)

Table 7-4. (Continued)

J2 - Vertical Sync Polarity

The vertical sync signals can have positive (standard) or negative polarity. This jumper is etched on the board.

J2	Configuration
1-2	Positive vertical sync (standard)
2-3	Negative vertical sync

J4 - Horizontal Sync Polarity

The horizontal sync signals can have positive (standard) or negative polarity. This jumper is etched on the board.

J4	Configuration
2-3	Positive horizontal sync (standard)
1-2	Negative horizontal sync

J3, J5 - External High-Scan Video

These jumpers control all but the internal monitor. Video outputs will be active in high-scan. They are changed as a set (both to 2-3 or both to 1-2).

J3	J5	Configuration
2-3	2-3	Enable high-scan video on external outputs (standard setting for COMPAQ DESKPRO Computers)
1-2	1-2	Disable high-scan video on external outputs (standard setting for COMPAQ PORTABLE Computers)

(Continued)

Table 7-4. (Continued)

J6 - Enable Mode Signal

This 2-pin jumper connects the MODE signal to pin 7 of the 9-pin connector. The MODE signal is low for high-scan (18.5 kHz) and high for low-scan (15.7 kHz). Cutting this jumper's etch makes pin 7 not connect.

J6	Configuration
1-2	Connect MODE signal to pin 7
n.c.	Disconnect MODE signal from pin 7

J7, J8, J9 - Standard/Alternate Video Display Controller Board Addresses

These jumpers change the video memory base address from B8000h to B0000h. They also change the Video Display Controller Board's I/O address from 3DXh to 3BXh (X = value from 0 to F(h)). These jumpers are etched on the board.

Boards with standard or alternate base addresses are functionally identical.

J7	J8	J9	Configuration
1-2	1-2	1-2	Standard
2-3	2-3	2-3	Alternate

(Continued)

Table 7-4. (Continued)

J10, J11 - Extended Memory (Version 3 Video Display Controller Board only)

These jumpers enable additional video memory. Standard video buffer size is 16K bytes of Dynamic RAM beginning at address B8000h and extending to address BBFFFh. Extended video buffer size is 32K bytes beginning at address B8000h and extending to BFFFFh.

Jumpers J10 and J11 are etched on the board to 16K bytes (standard buffer size), and are changed as a set (both to 2-3 or both to 1-2).

J10	J11	Configuration
2-3	2-3	Standard video memory (16K bytes)
1-2	1-2	Extended video memory (32K bytes)

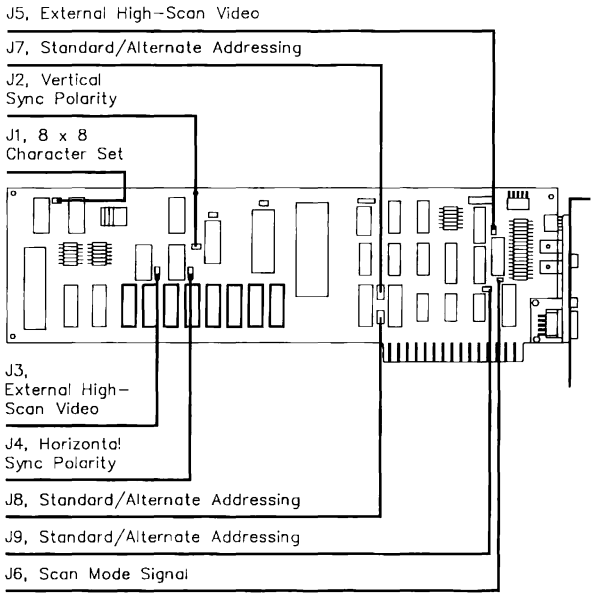


Figure 7-13. Version 1 Video Display Controller Board Jumper Arrangement

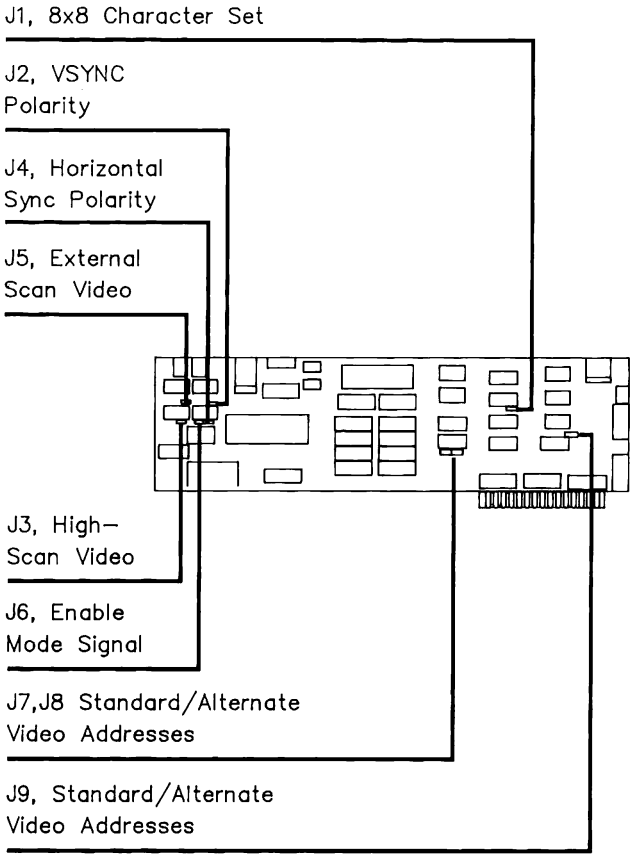


Figure 7-14. Version 2 Video Display Controller Board Jumper Arrangement

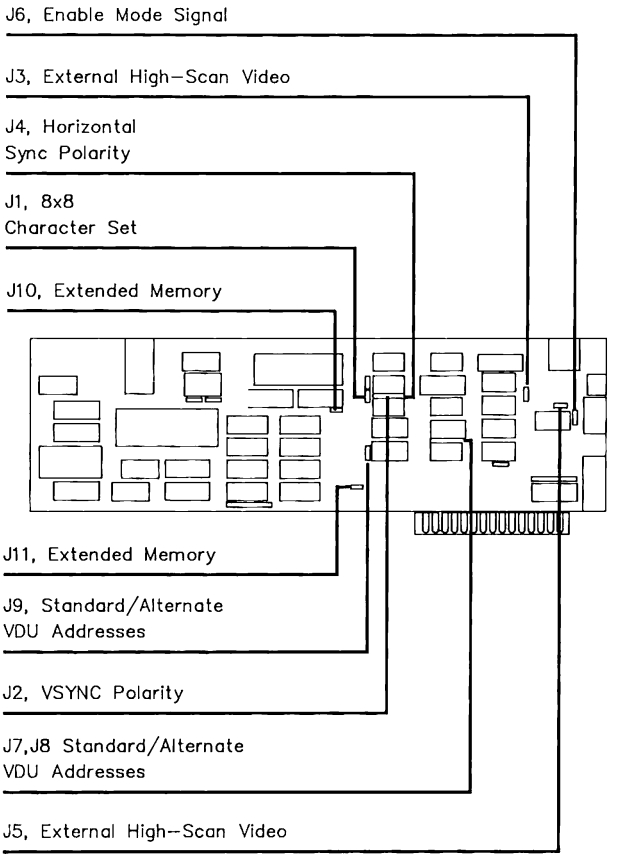


Figure 7-15. Version 3 Video Display Controller Board Jumper Arrangement

7.7 CONNECTORS

Table 7-5 through 7-9 show the video display controller board connector signals.

Figure 7-16 shows the location of the connectors on a Version 1 video display controller board. The connectors are located in the same positions on all three versions of the video display controller board.

Figure 7-17 through 7-19 show the video display controller board connectors.

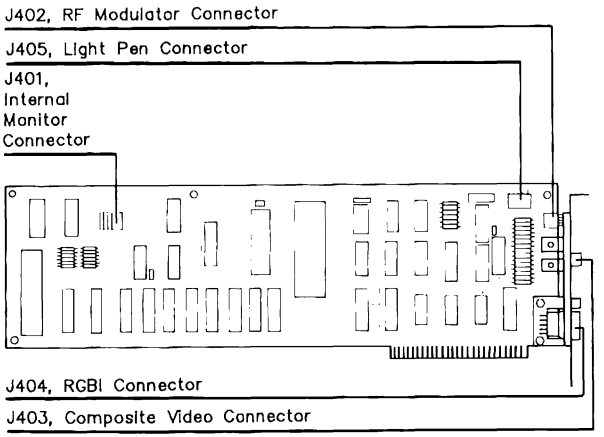


Figure 7-16. Connectors on the Video Display Controller Board

Table 7-5. J401, Internal Monitor Connector Signals

Signal	Pin	I/O	Description
Chassis Ground	11,12	-	Cable Shield
HS	7	O	Horizontal sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is always fixed at 8 characters regardless of the duration programmed in the 6845. Refer to Section 8.5 for the timing characteristics.
MODE	3	O	This TTL signal controls the monitor mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The MODE signal is high (= 1) for the low-scan mode, and low (= 0) for the high-scan mode.
Signal Ground	2,4,8	-	This is the ground reference for the TTL signals.
VID	5	O	This analog video output signal ranges from 1.0 Vdc (black) to 2.5 Vdc (white) into 470 to 6800 ohms (impedance). Its ground reference is the video ground signal (pin 6).
Video Ground	6	-	This is the ground reference for the VID signal (pin 5).
VS-	1	O	Vertical sync is an active-low TTL signal in both level and drive characteristics. The pulse duration is always fixed to three scan lines regardless of the duration that is programmed in the 6845's internal registers. Refer to the section 8.5 for the timing characteristics for the vertical sync signals.

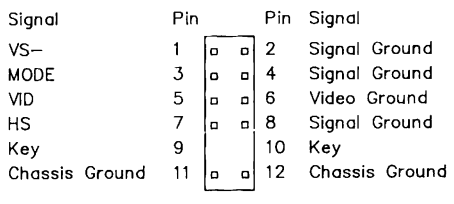


Figure 7-17. J401, Internal Monitor Connector

Table 7-6. J402, RF Modulator Connector Signals

Signal	Pin	I/O	Description
+12 Vdc	1	O	Power
COMPOSITE VIDEO	3	O	This analog signal is the composite video output
Signal Ground	4	-	Reference for composite video

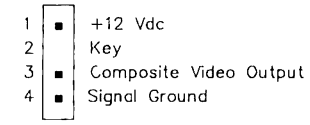


Figure 7-18. J402, RF Modulator Connector

Table 7-7. J403, Composite Video Connector Signals

Signal	Pin	I/O	Description
Chassis Ground	2	-	Reference for composite video
COMPOSITE VIDEO	1	O	This analog signal is the composite video output

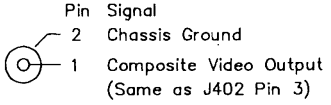


Figure 7-19. J403, Composite Video Connector

Table 7-8. J404, RGBI Video Connector Signals

Signal	Pin	I/O	Description
B	5	O	Blue. Active-high TTL signal.
G	4	O	Green. Active-high TTL signal.
HS	8	O	Horizontal sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is fixed at eight characters regardless of the duration programmed in the 6845. Refer to the "Monitors Supported" section for the timing characteristics.
I	6	O	Intensity. Active-high TTL signal.
MODE	7	O	This signal controls the monitor high- or low-scan mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The MODE signal is high for the low-scan mode and low for the high-scan mode.
R	3	O	Red. Active-high TTL signal.
Signal Ground	1,2	-	TTL signal reference.
VS	9	O	Vertical sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is fixed to 3 scan lines regardless of the pulse duration programmed in the 6845. Refer to the "Monitors Supported" section for the timing characteristics.

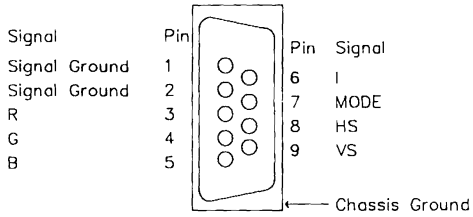


Figure 7-20. J404, RGBI Connector

Table 7-9. J405, Lightpen Connector Signals

Signal	Pin	I/O	Description
+5 Vdc	5	O	+5 Vdc lightpen power source
+12 Vdc	6	O	+12 Vdc lightpen power source
LIGHTPEN SWITCH-	3	I	Active-low signal indicates lightpen switch contact closed
LIGHTPEN TRIGGER-	1	I	Active-low signal indicates lightpen triggered
Signal Ground	4	-	Reference for TTL signals

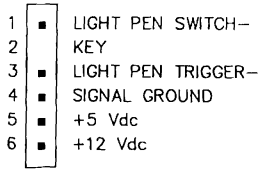


Figure 7-21. J405, Lightpen Connector

7.8 SCHEMATICS

Figure 7-22 shows the schematics for the Video Display Controller Board Version 1. COMPAQ Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

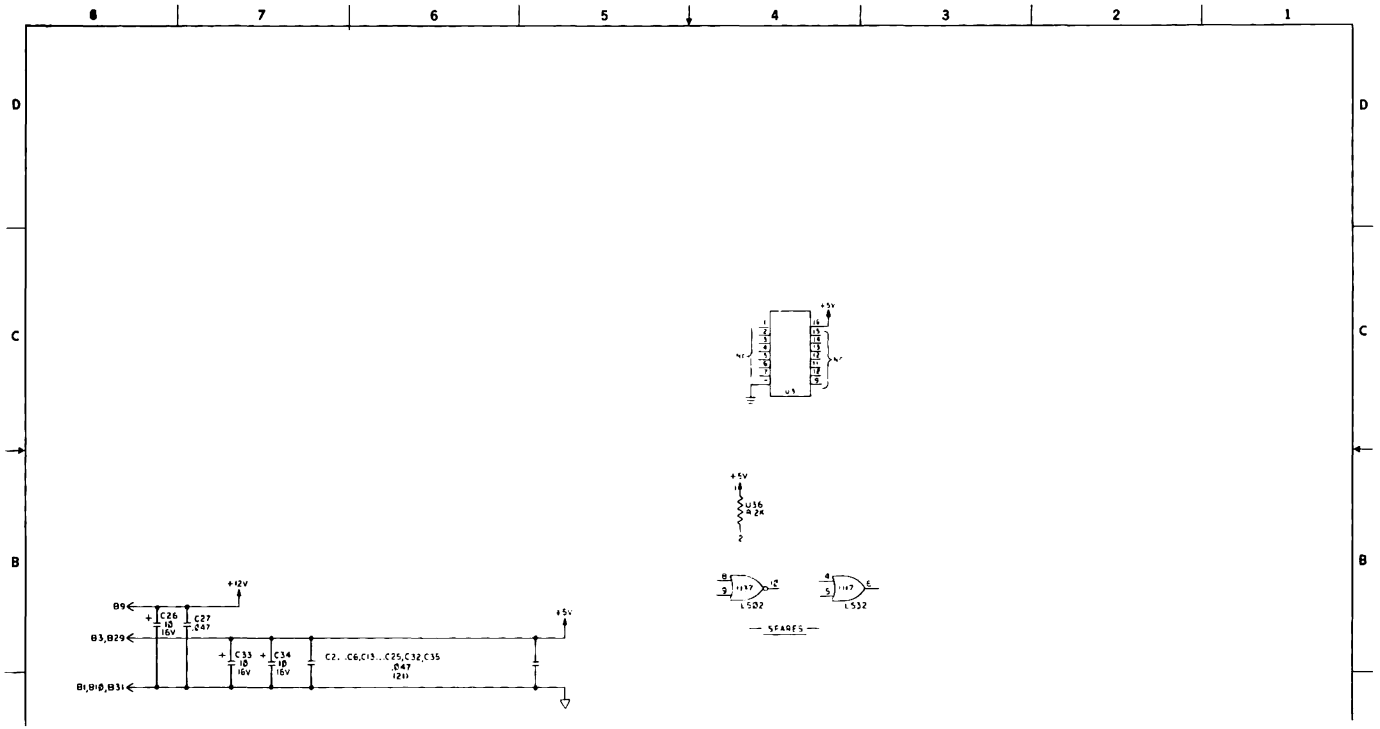


Figure 7-22. Video Display Controller Board Version 1 Schematics (Page 1 of 5)

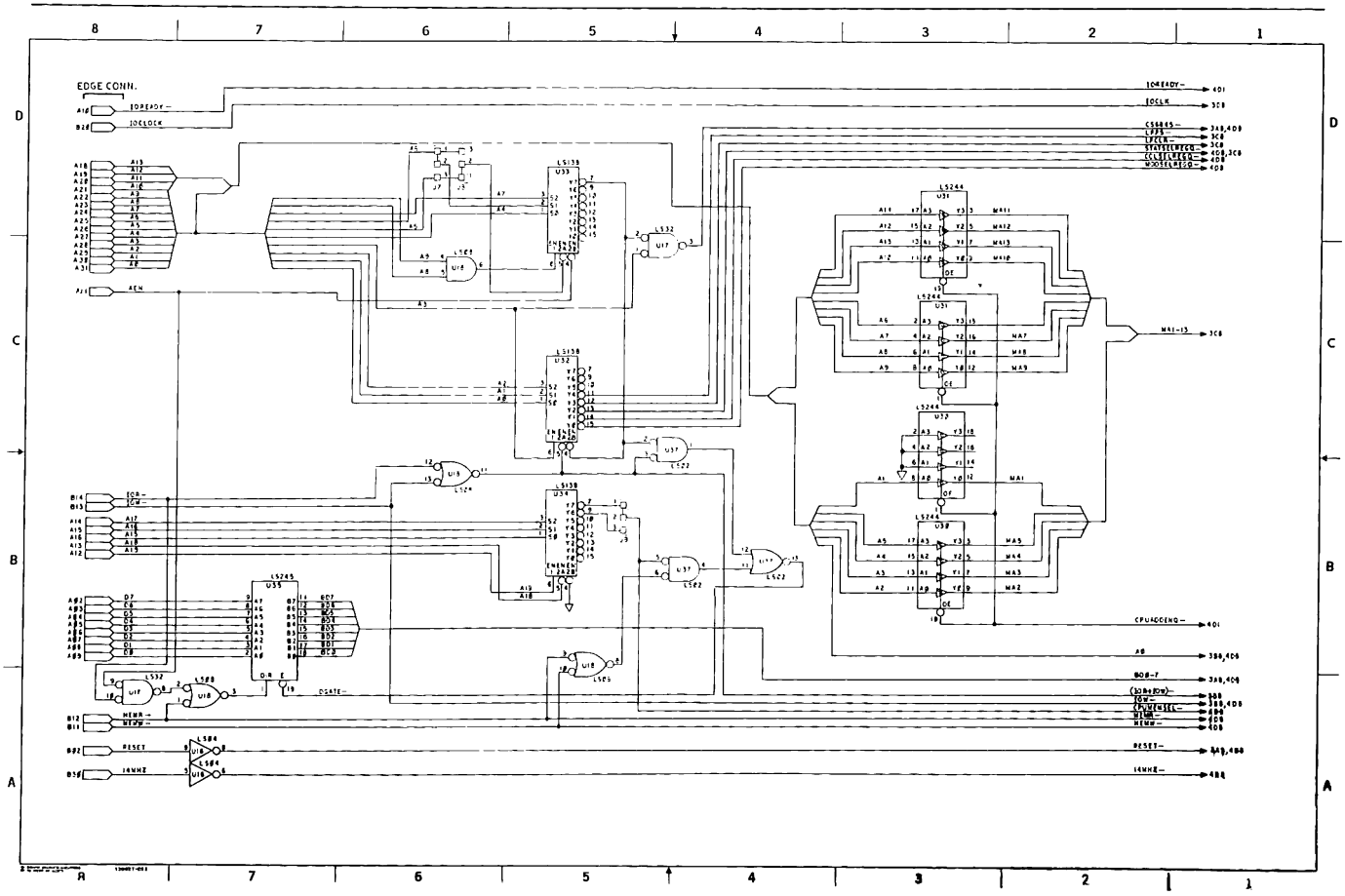


Figure 7-22. Video Display Controller Board Version 1 Schematics (Page 2 of 5)

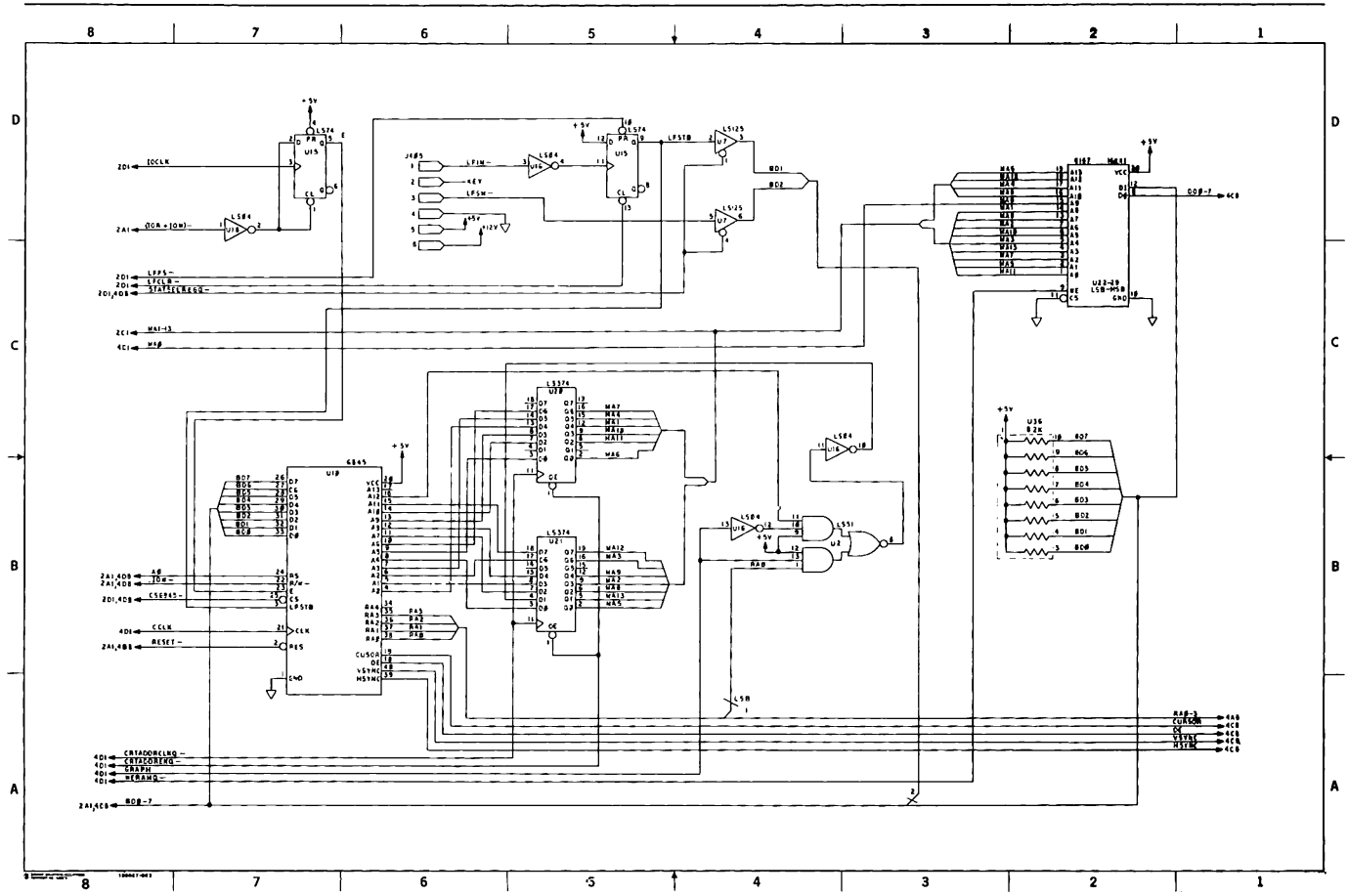


Figure 7-22. Video Display Controller Board Version 1 Schematics (Page 3 of 5)

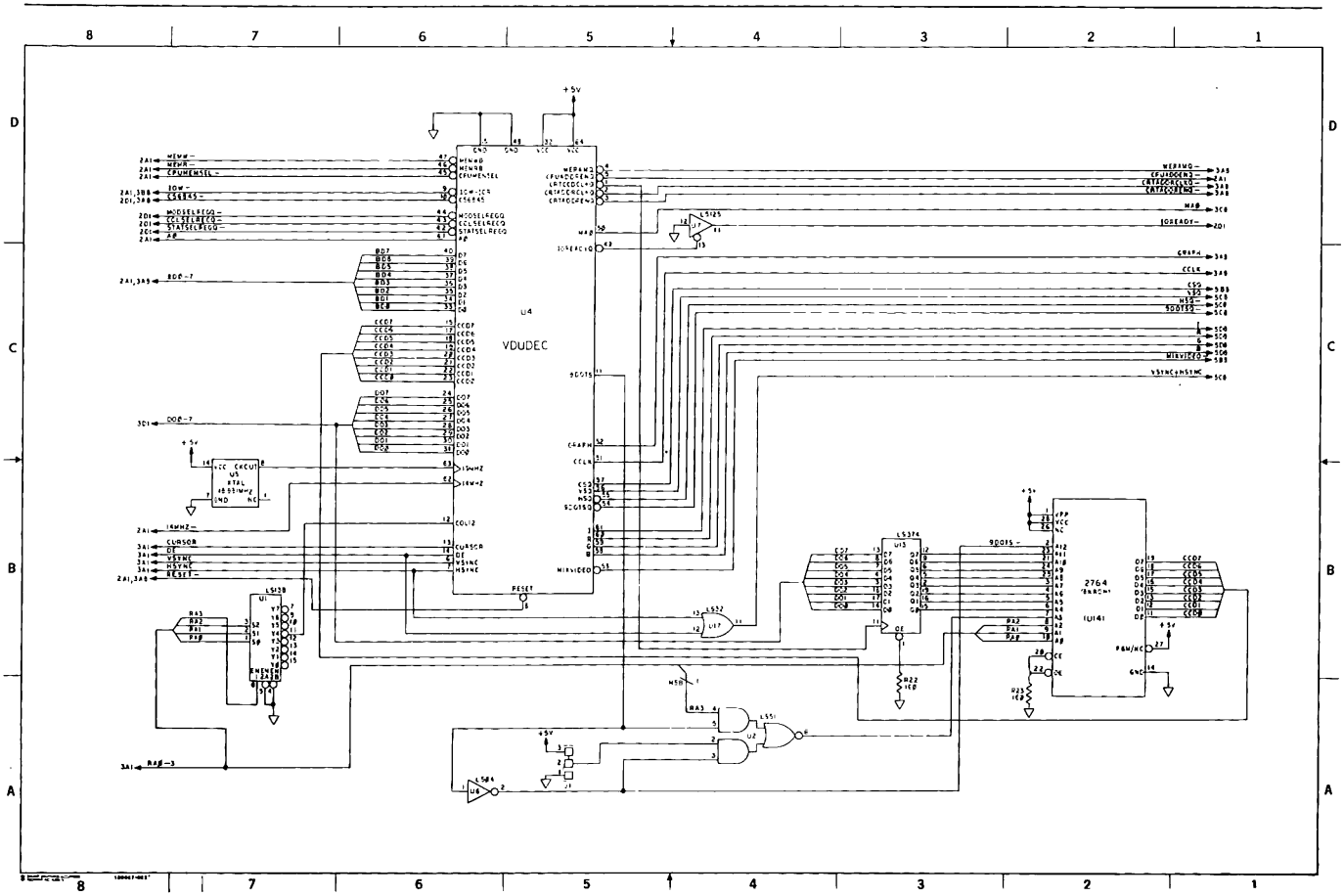


Figure 7-22. Video Display Controller Board Version 1 Schematics (Page 4 of 5)

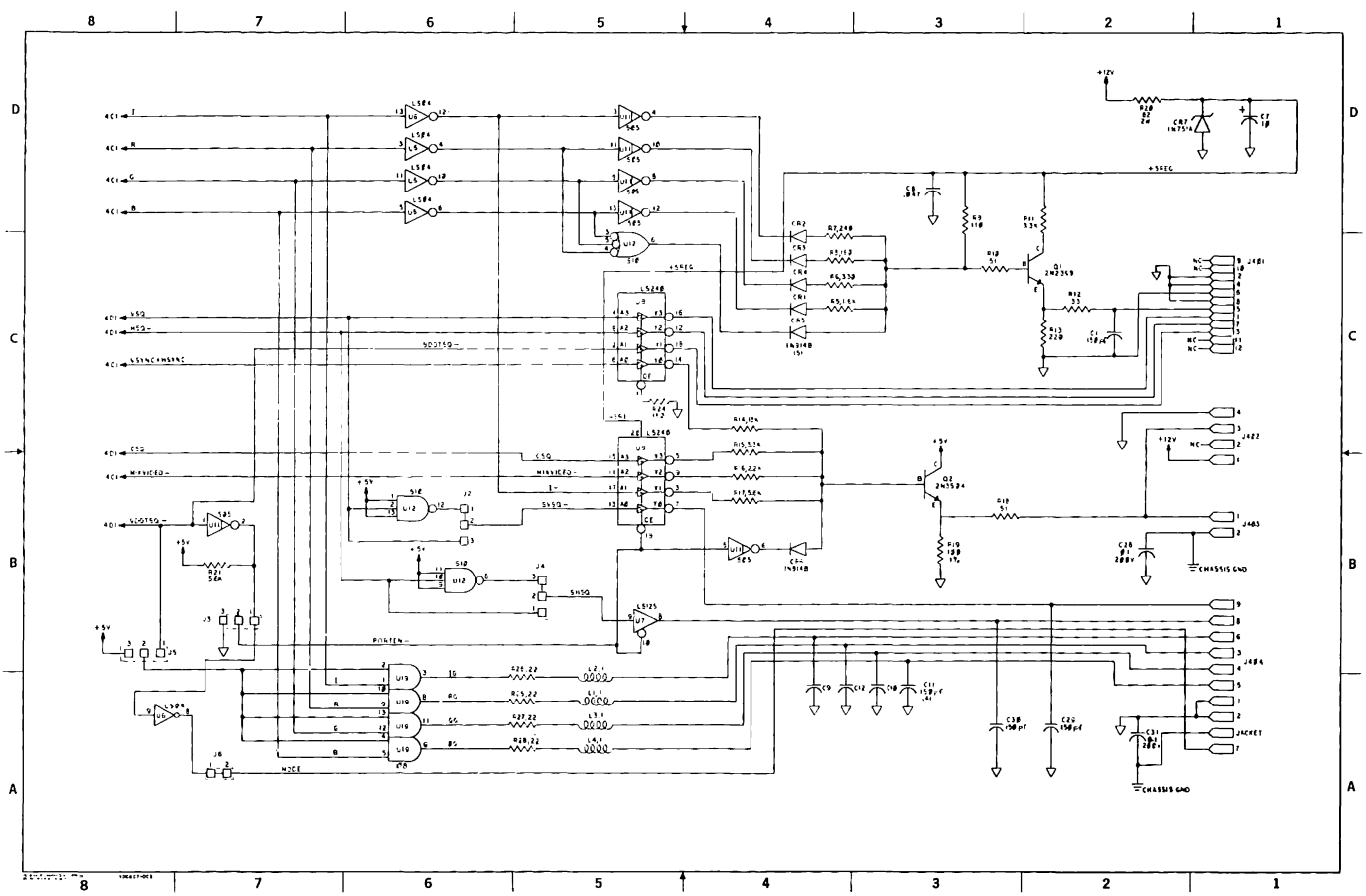


Figure 7-22. Video Display Controller Board Version 1 Schematics (Page 5 of 5)

Figure 7-23 shows the schematics for the Video Display Controller Board Version 2. COMPAQ Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

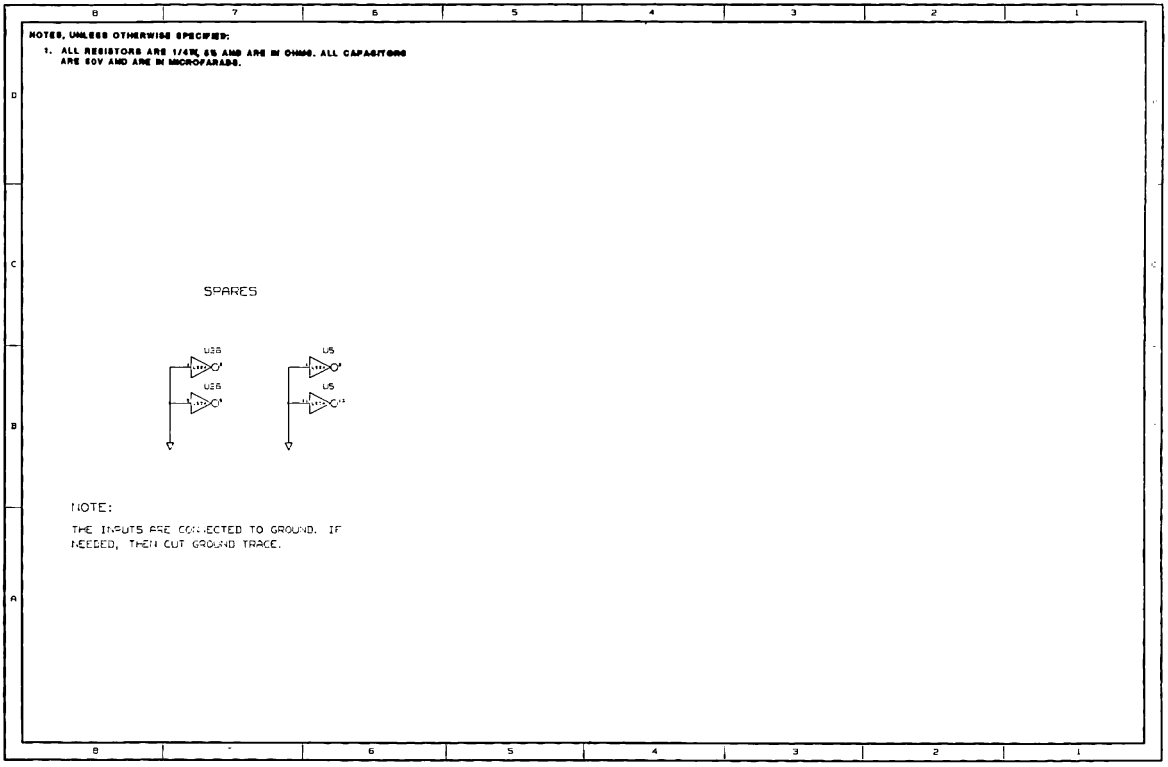


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 1 of 7)

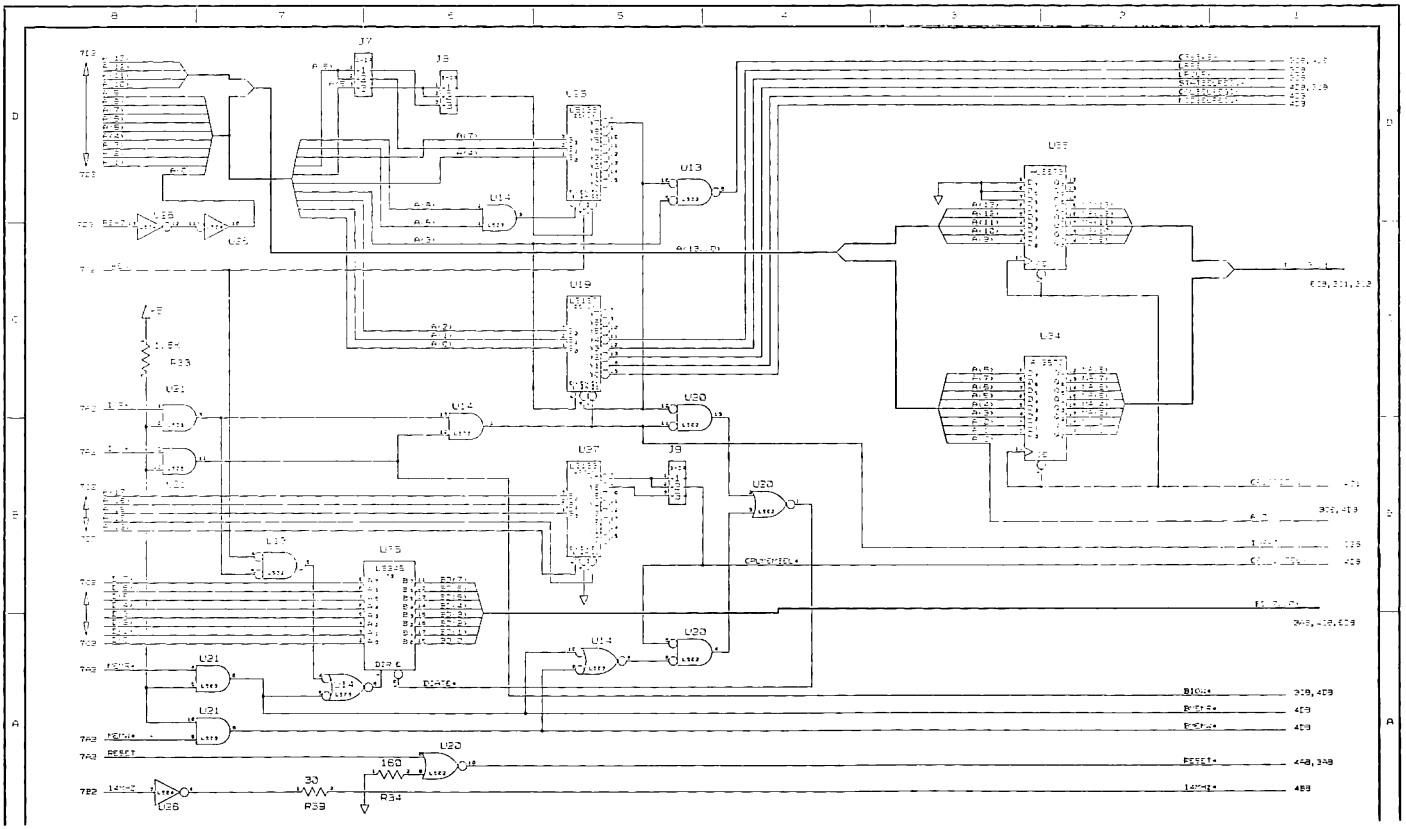


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 2 of 7)

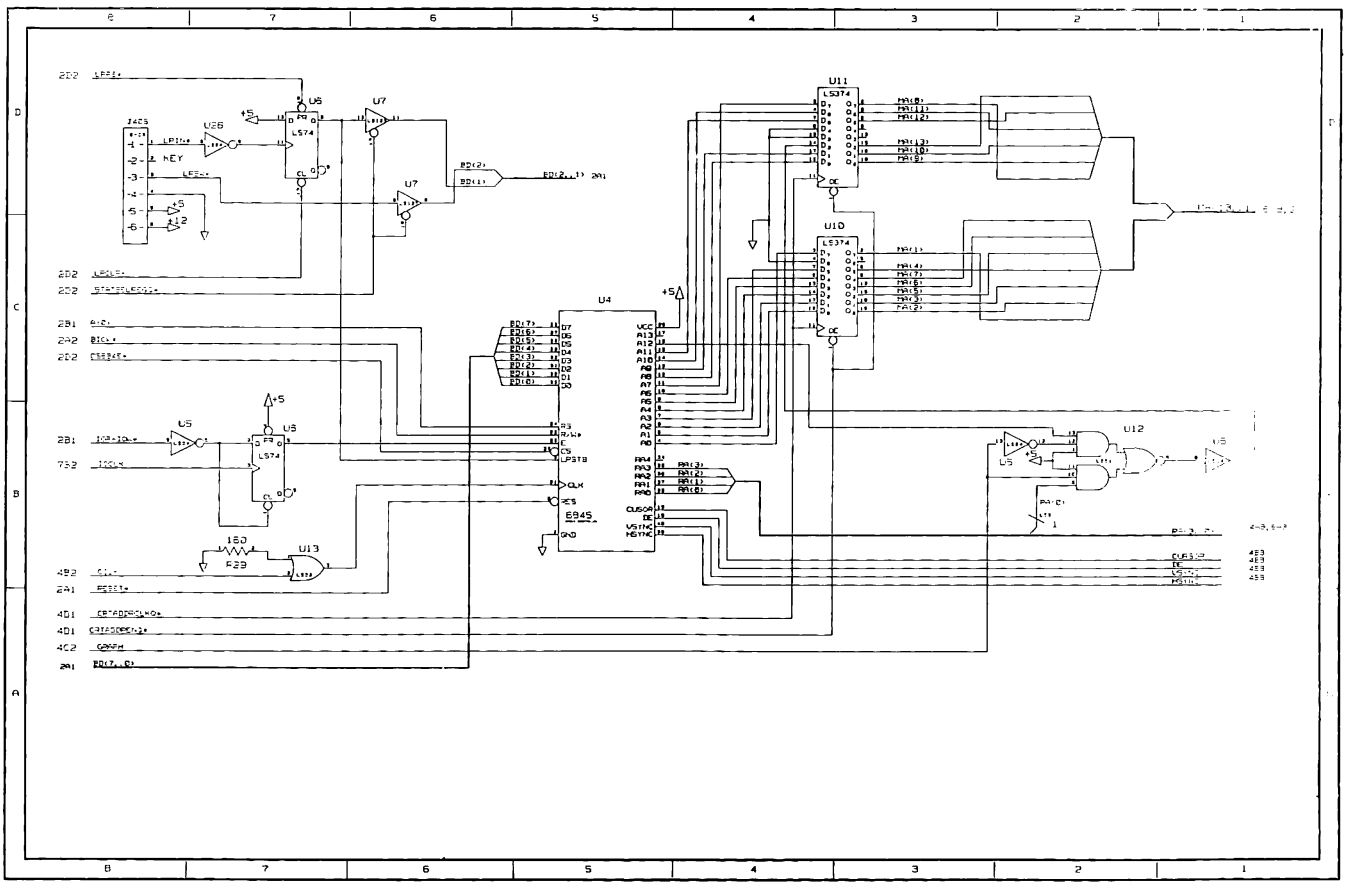


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 3 of 7)

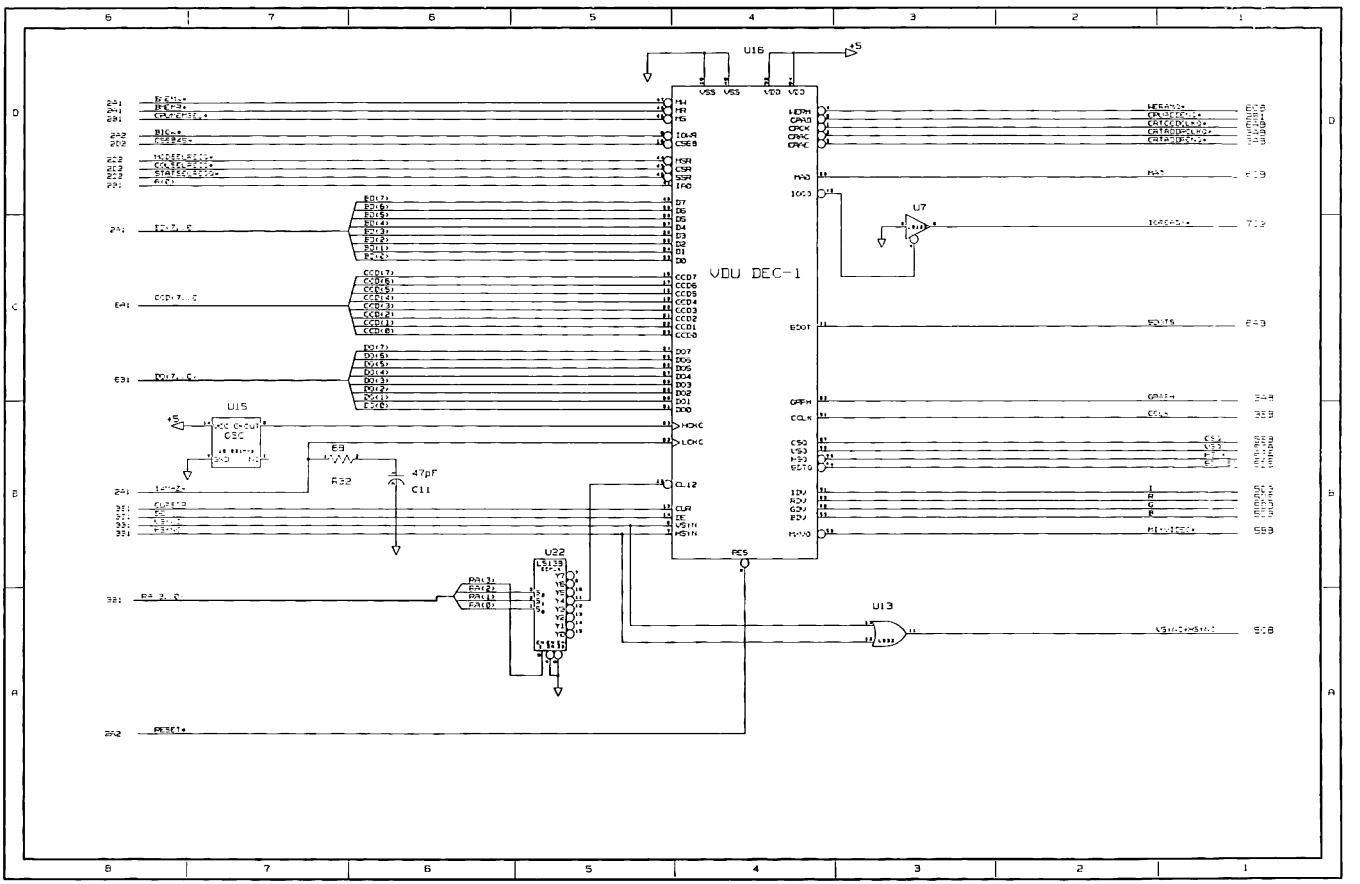


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 4 of 7)

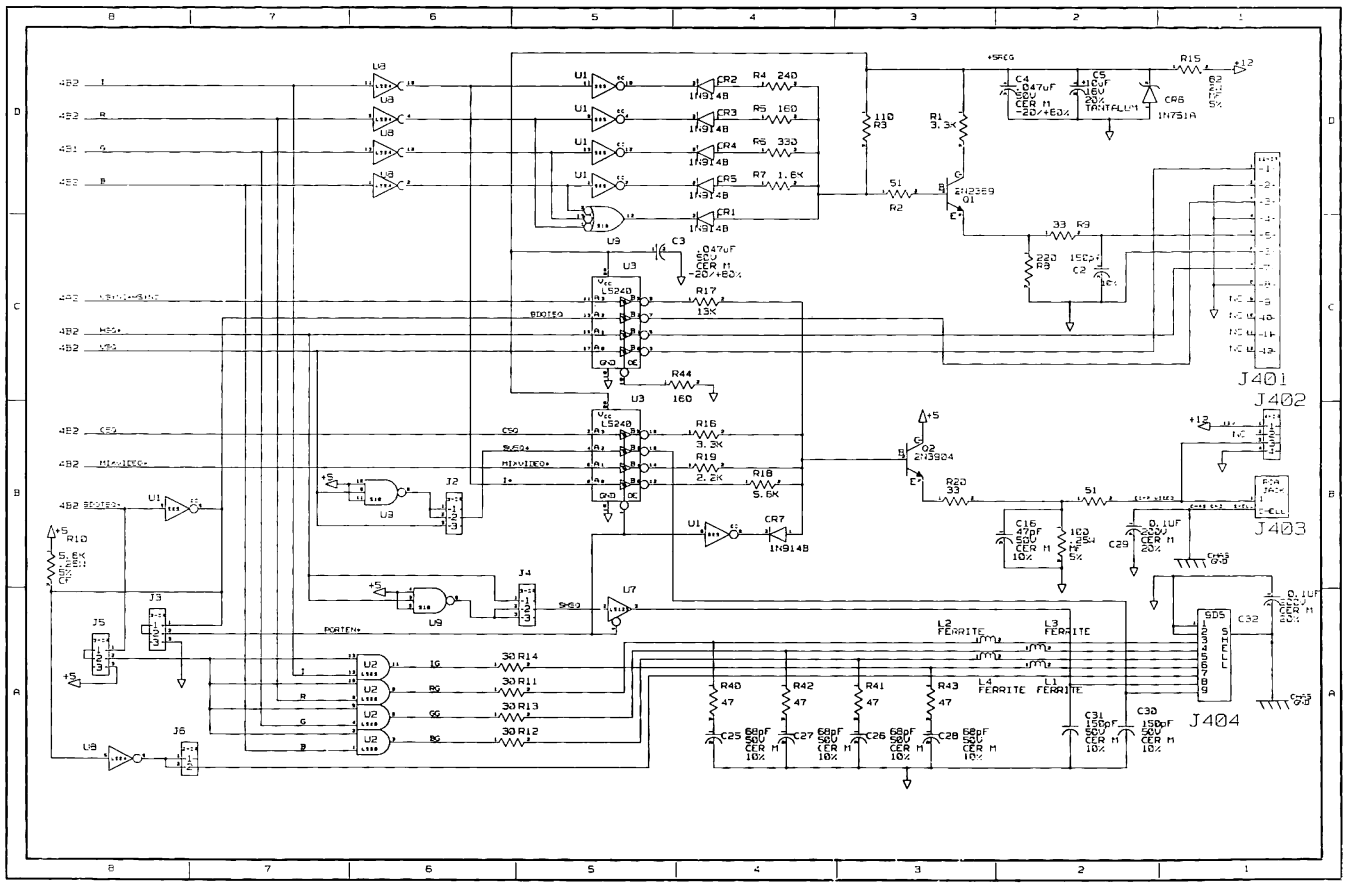


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 5 of 7)

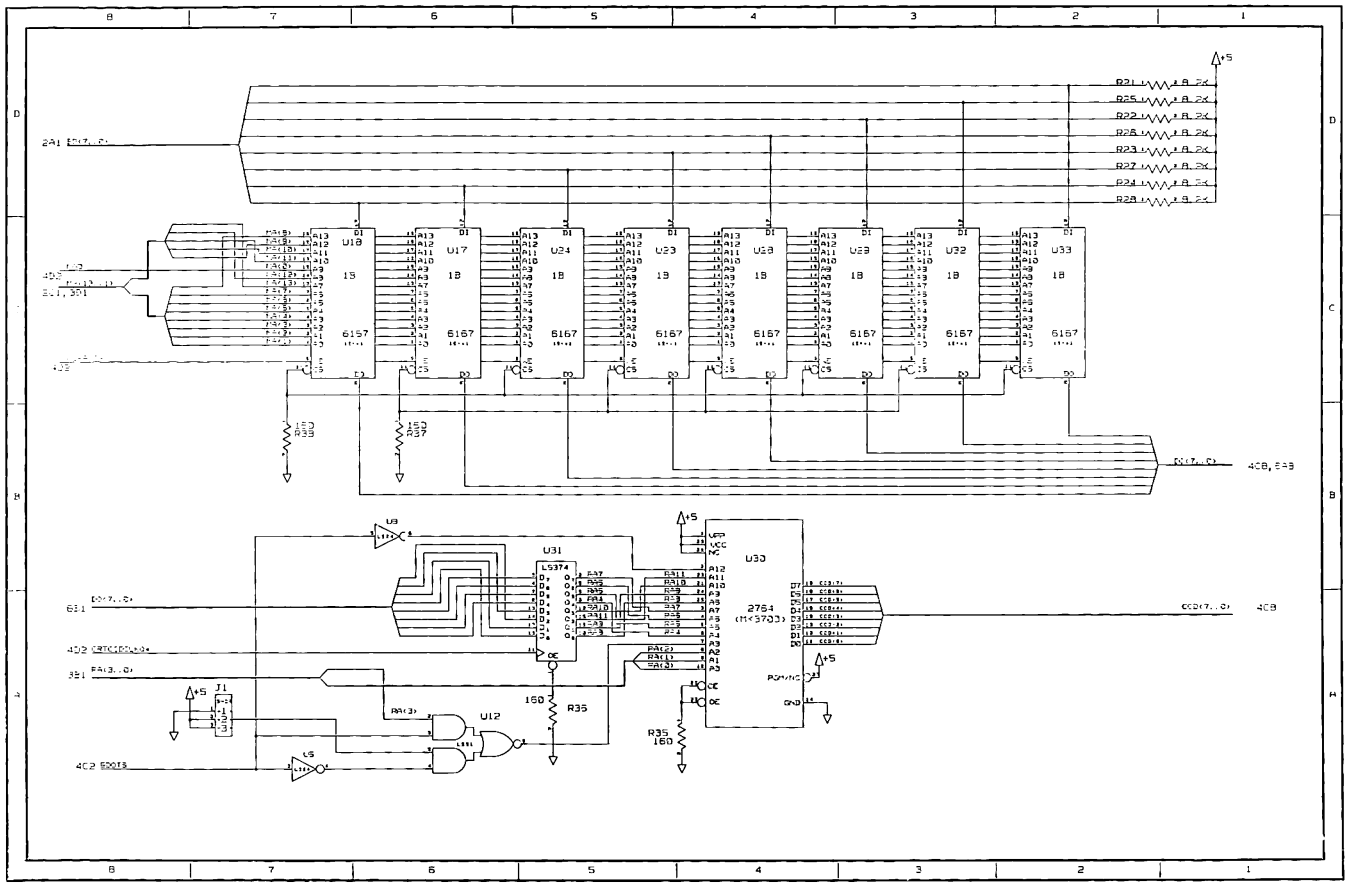


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 6 of 7)

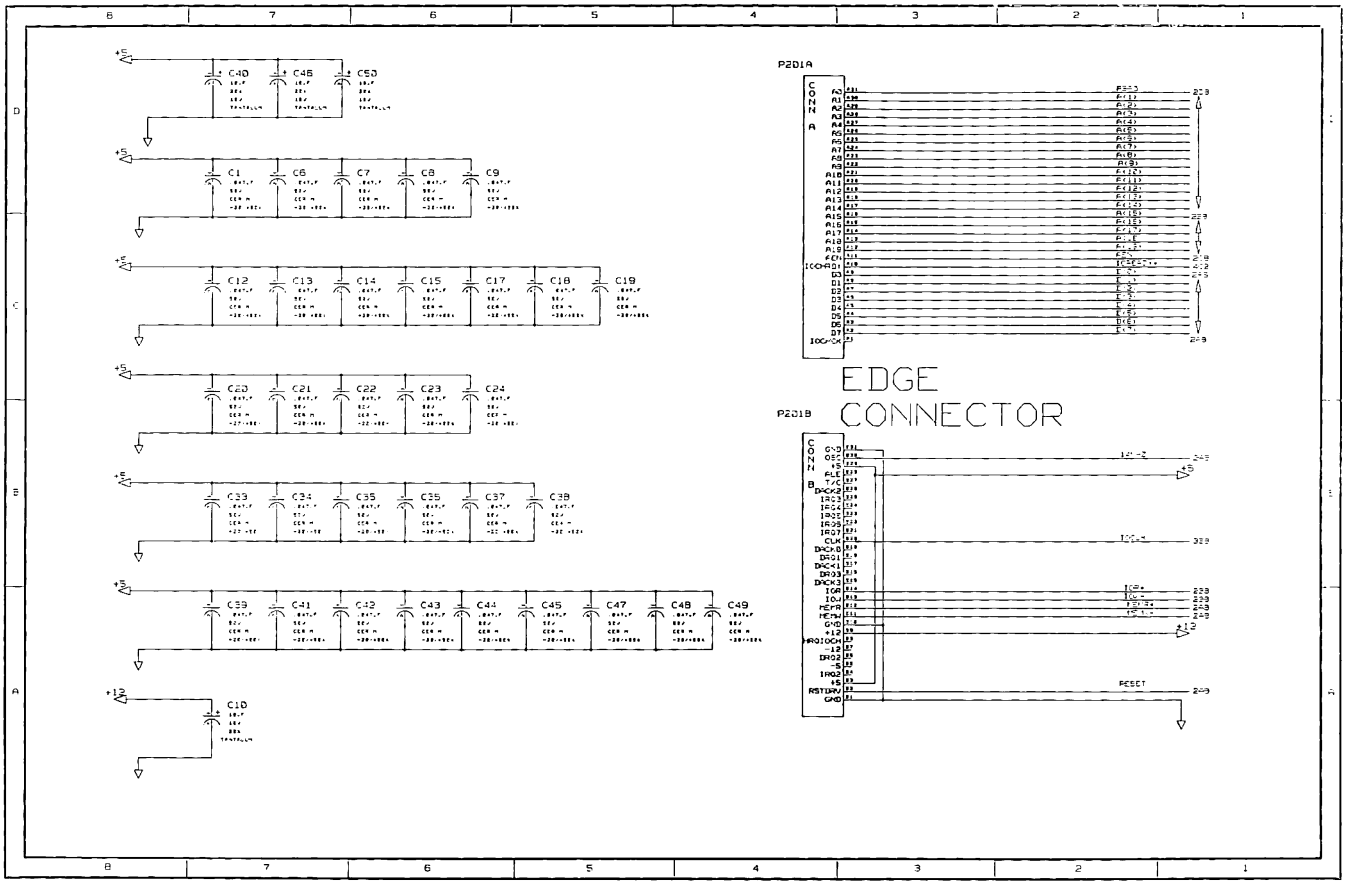


Figure 7-23. Video Display Controller Board Version 2 Schematics (Page 7 of 7)

Figure 7-24 shows the schematics for the Video Display Controller Board Version 3. COMPAQ Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.

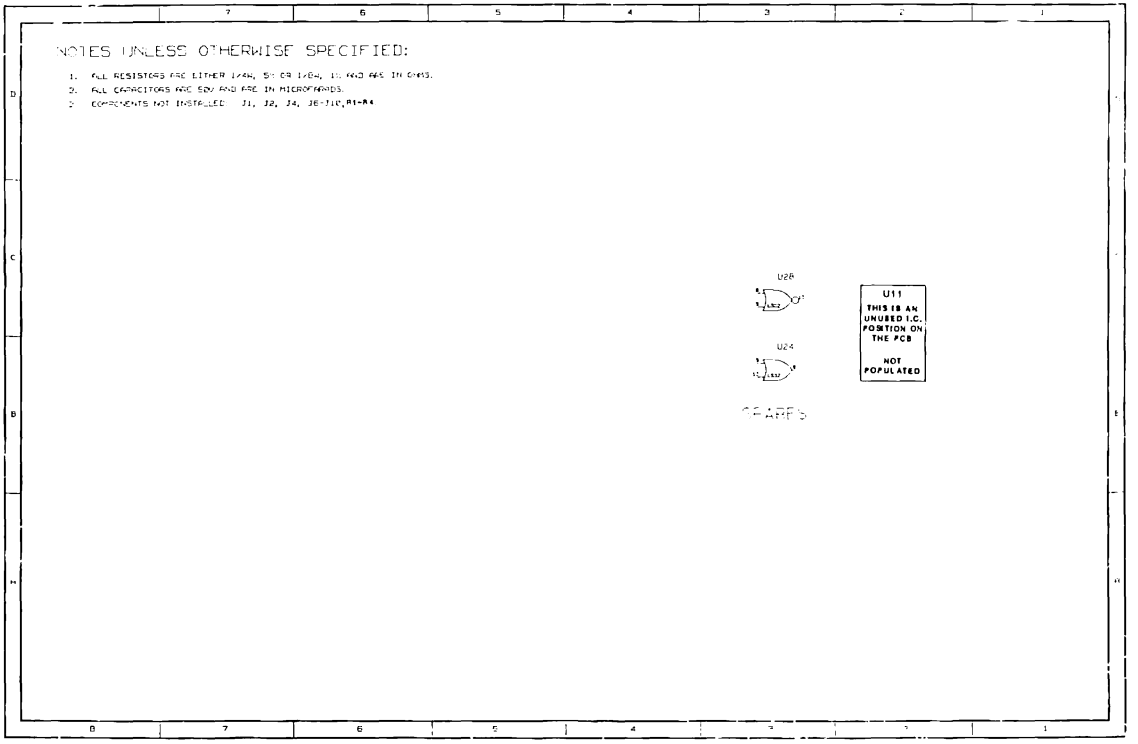


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 1 of 7)

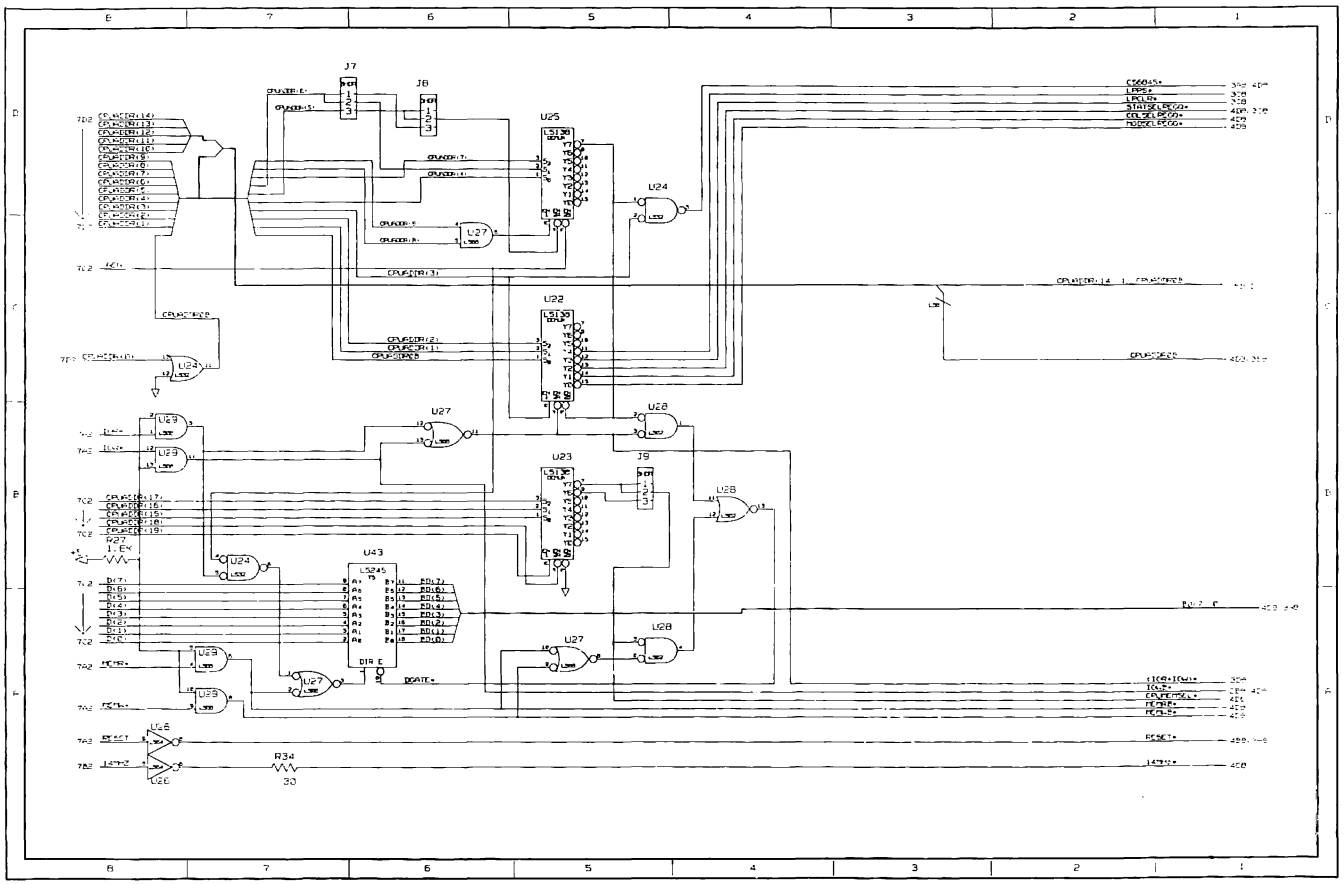


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 2 of 7)

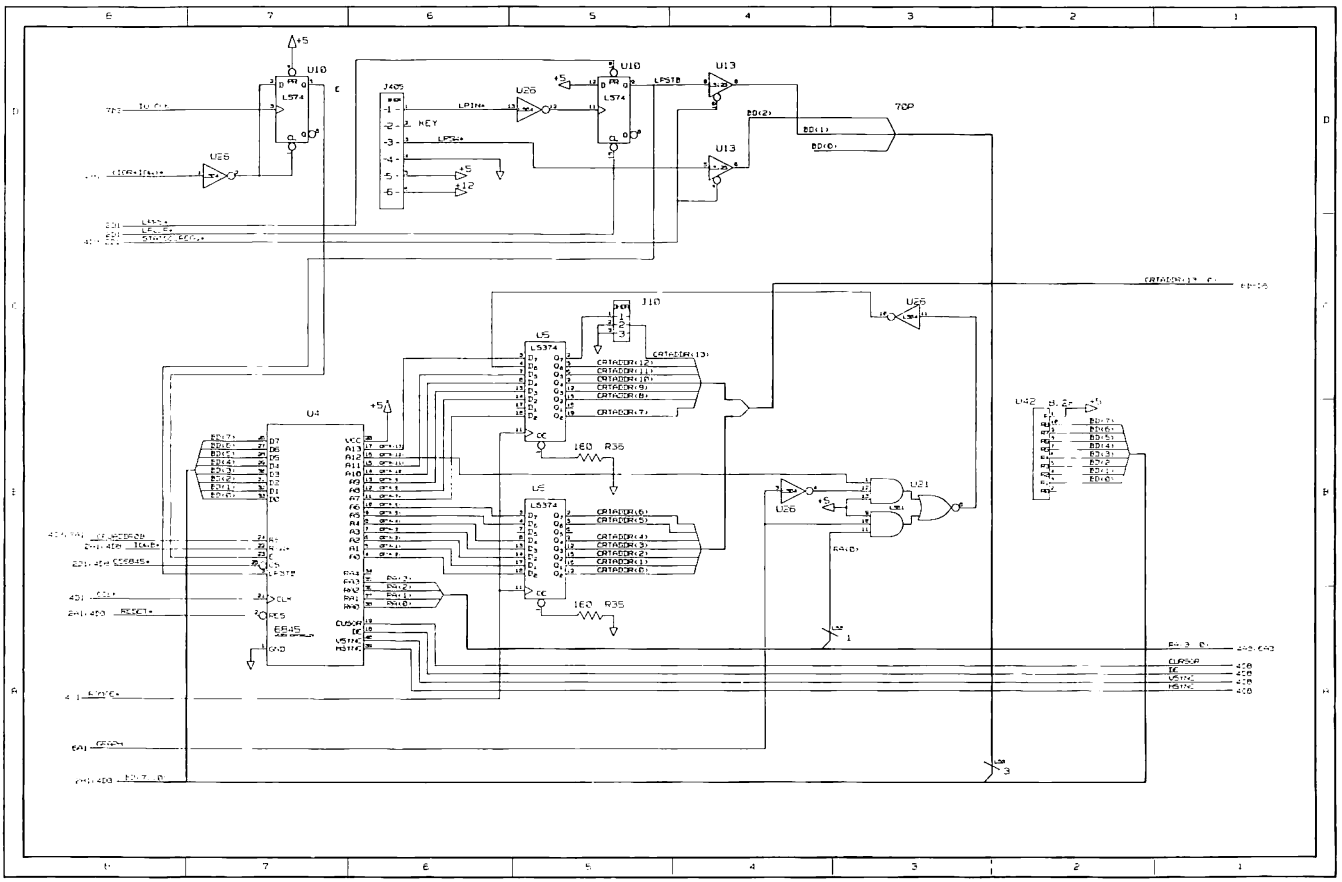


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 3 of 7)

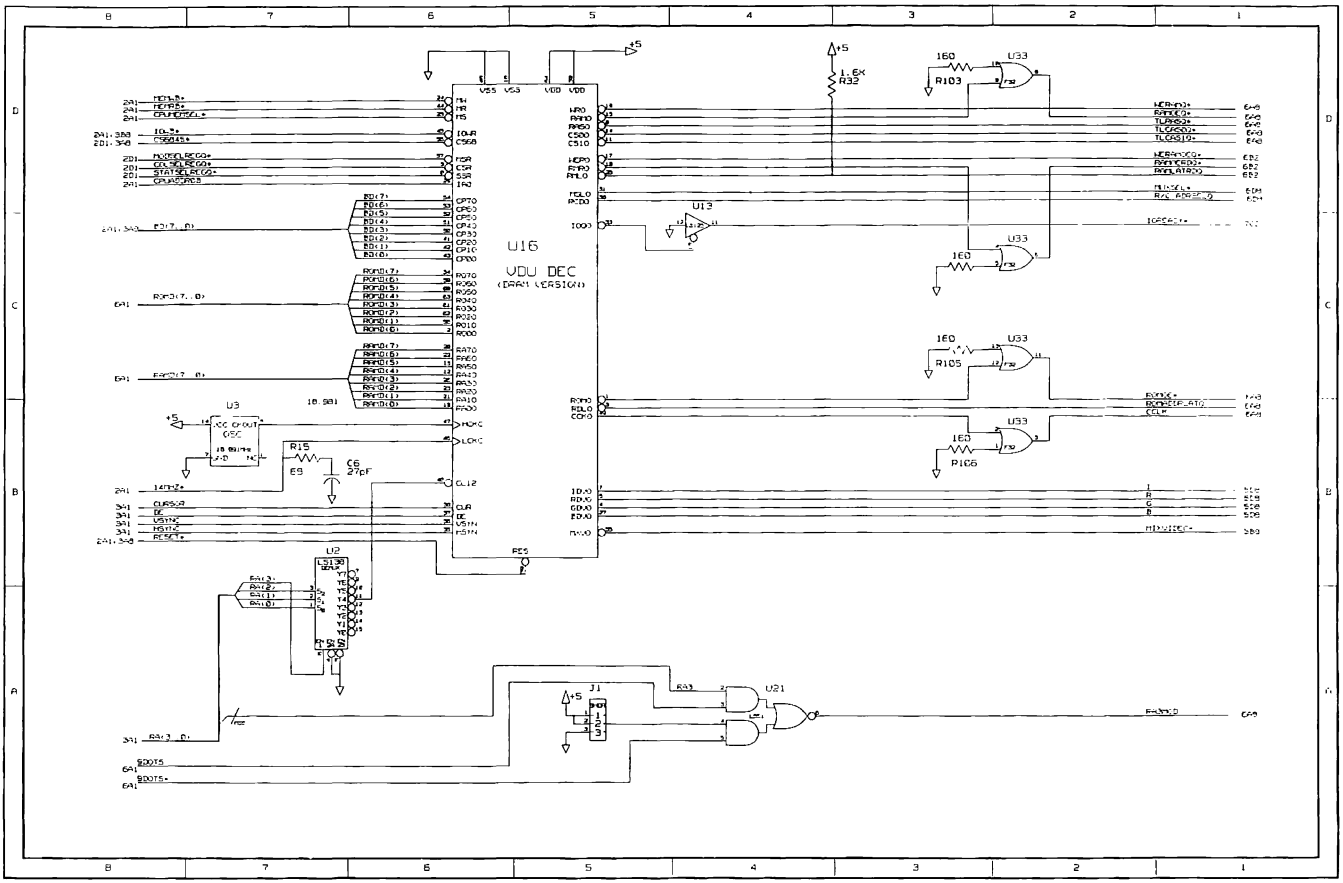


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 4 of 7)

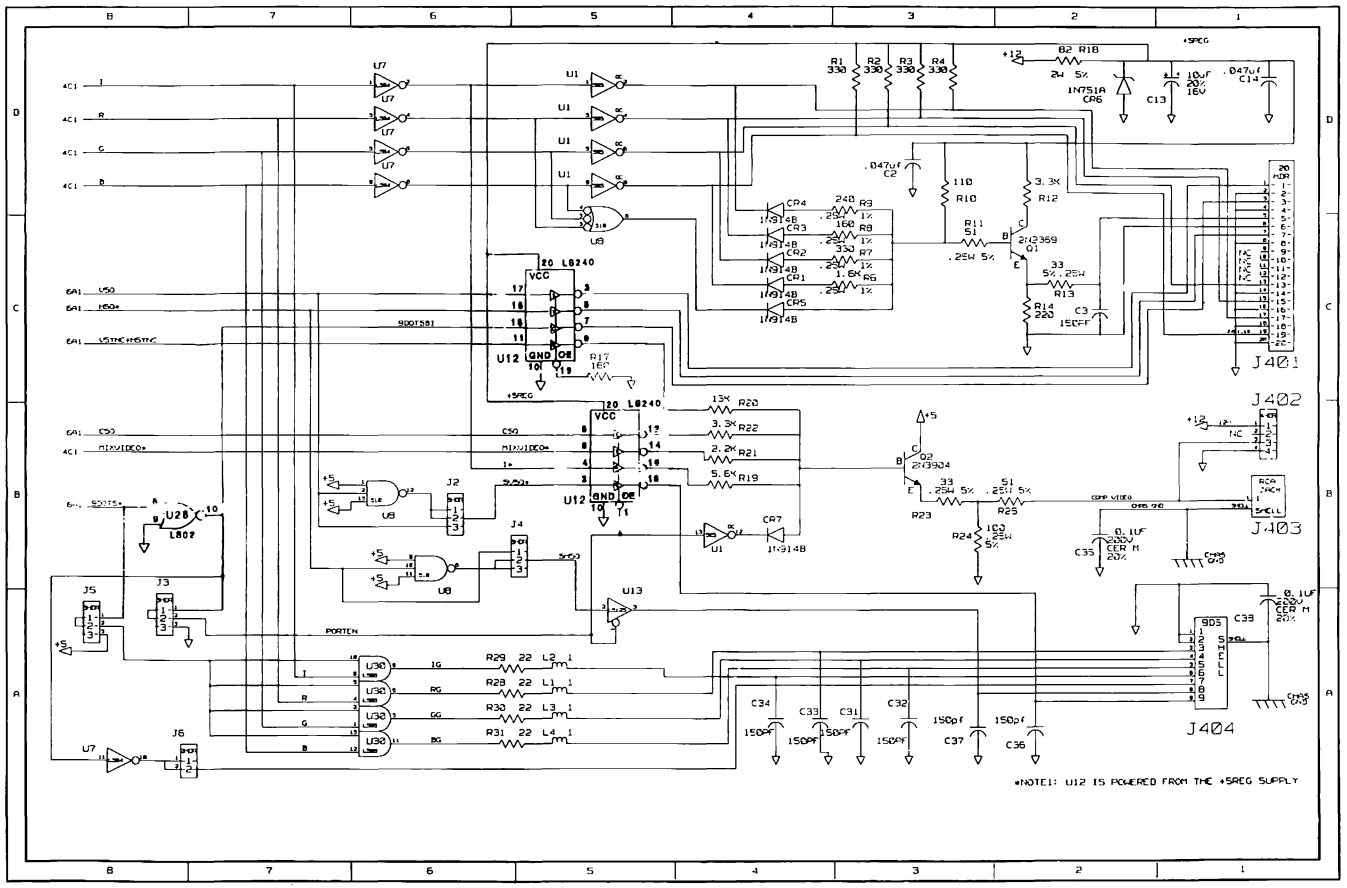


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 5 of 7)

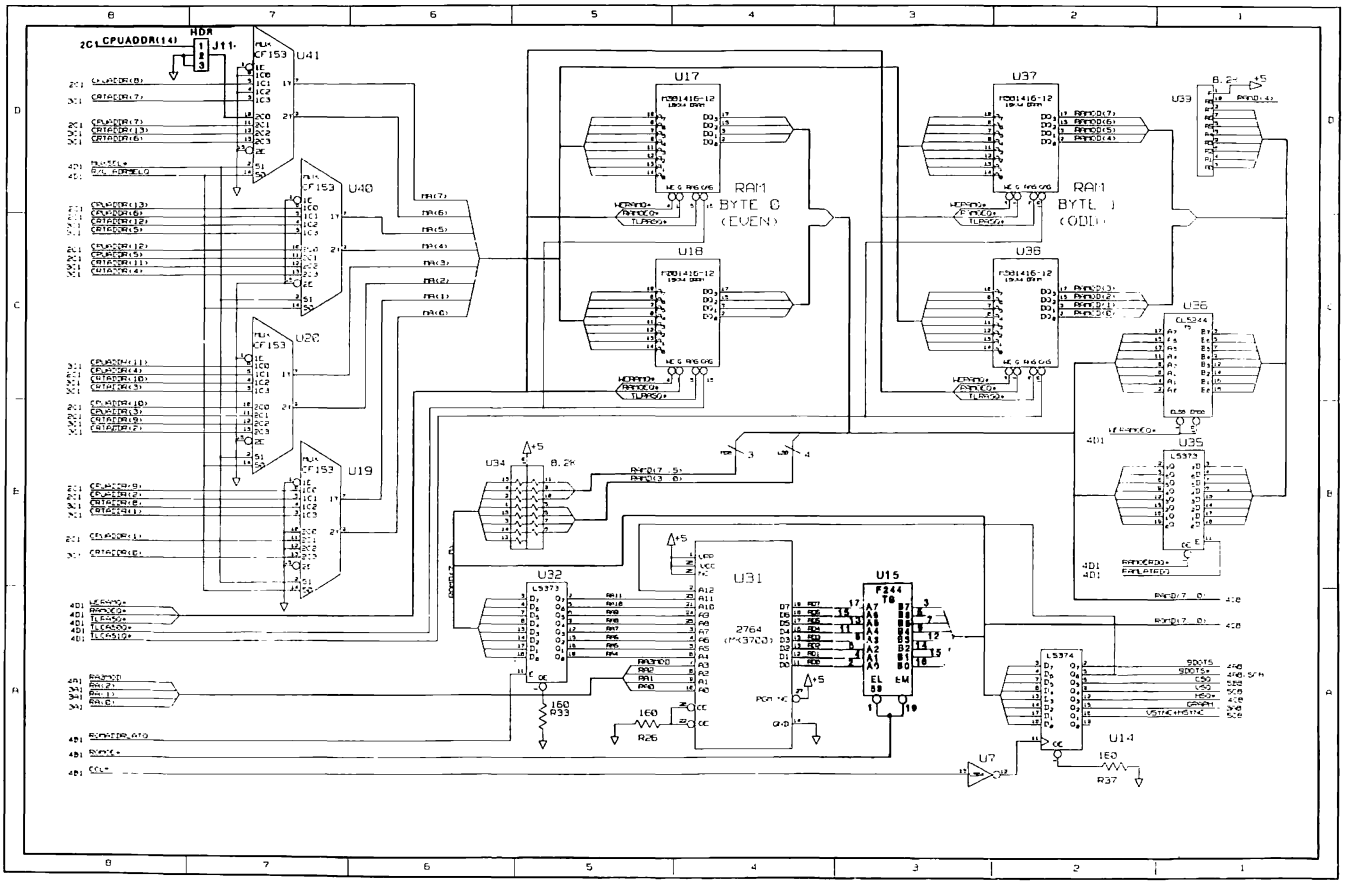


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 6 of 7)

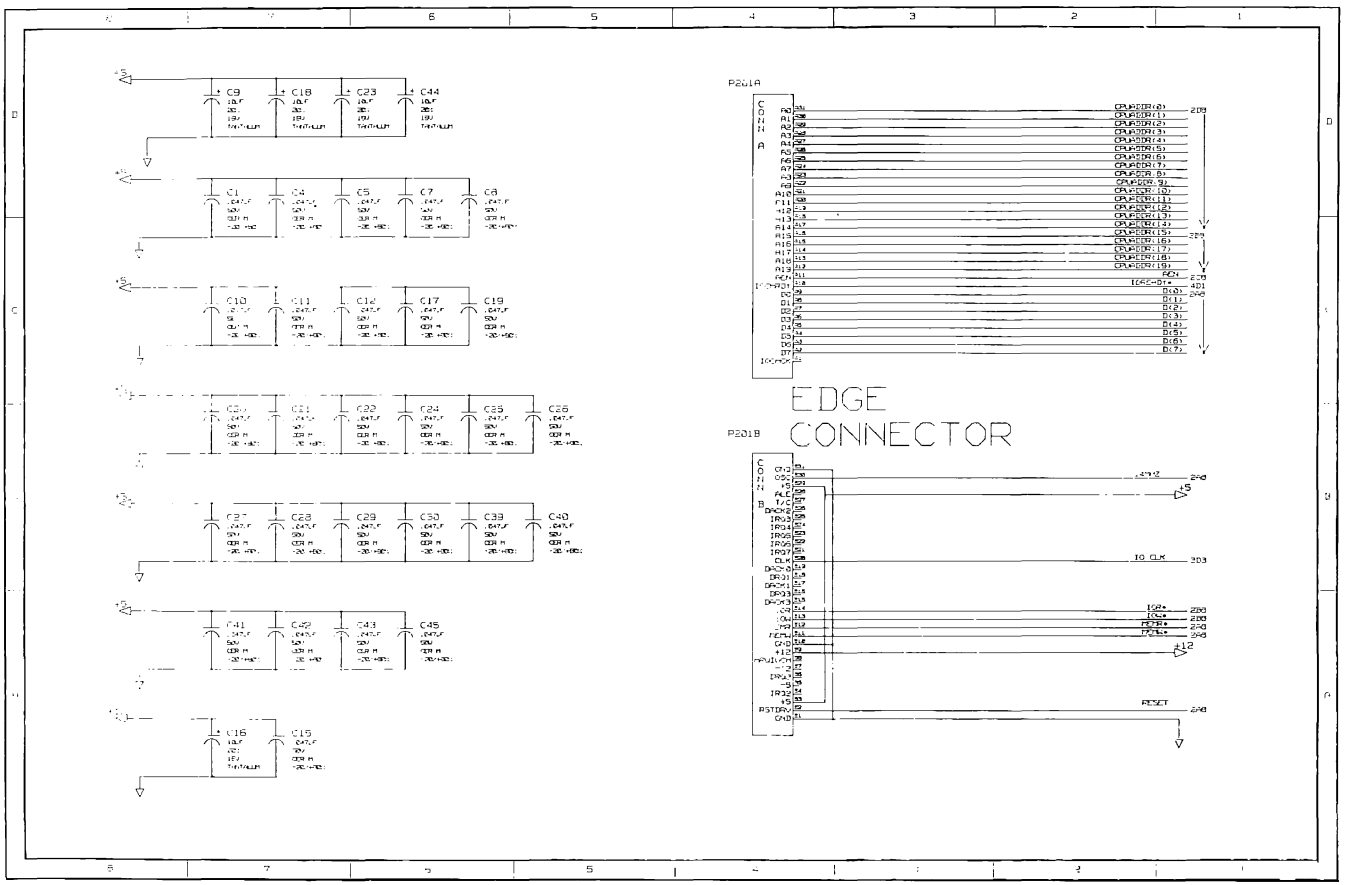


Figure 7-24. Video Display Controller Board Version 3 Schematics (Page 7 of 7)

Chapter 8

KEYBOARDS

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KEYBOARDS

Chapter 8
KEYBOARDS

8.1 INTRODUCTION

The keyboard is the primary means by which the user communicates with the system. Two keyboards operate with the COMPAQ DESKPRO 286® : the 84-key keyboard and the COMPAQ Enhanced Keyboard. The COMPAQ® PORTABLE 286® uses only the 84-key keyboard. The COMPAQ Enhanced Keyboard is a 101-key keyboard (102 keys international) that offers additional features, such as a separate cursor control key cluster, additional function keys (F11 and F12), and enhanced programmability for make/break and repeating key functions.

Each of the two keyboards that operate with the COMPAQ DESKPRO 286 contains a microprocessor that scans the keyboard for pressed keys. The microprocessor also monitors its communication line with the system. The communication line carries keyboard control commands from the system and keyboard scan and acknowledgment codes to the system. Keyboard scan codes are generated by the keyboard when a key is pressed or released. Typically, a Make code is generated when a key is pressed. A Break code is generated when the key is released.

Within this chapter, the term "system" refers to the keyboard controller (8042) on the system board.

Figure 8-1 is a functional block diagram of the keyboard, which is the same for both keyboards.

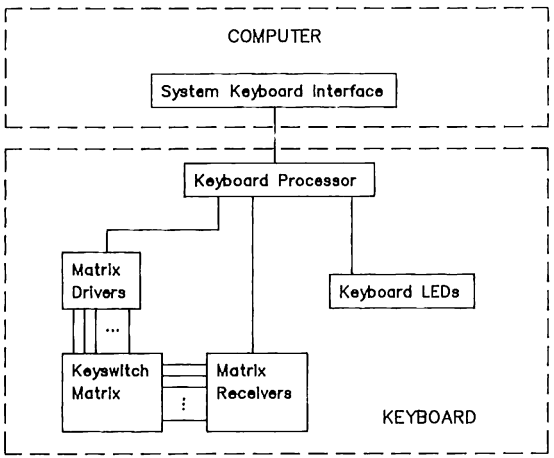


Figure 8-1. Keyboard Functional Block Diagram

8.2 KEYBOARD FEATURES

Both the 84-key and COMPAQ Enhanced keyboards contain a first-in, first-out (FIFO) buffer and a repeating key function. The 84-key keyboard can store as many as sixteen hex codes in its FIFO buffer. The COMPAQ Enhanced Keyboard is capable of storing sixteen 11-bit or twenty 9-bit hex codes in its FIFO buffer. Keycodes are placed in the FIFO buffer when keys are pressed or released, if the system is not ready to accept the keycode from the keyboard. When the system is ready to accept the keycode, the keyboard sends the keycodes stored in the FIFO buffer to the system in the order in which the keys were pressed.

When two keys are pressed simultaneously, the keyboard processes the first keycode detected and stores the second in the FIFO buffer. If any key is pressed while the FIFO buffer is full, the corresponding keycode is not generated and an overrun code (00h) is stored in the buffer. A location in the FIFO buffer is reserved for overrun conditions.

Another important feature of the keyboards is the repeating key function. This feature allows the keyboards to repeatedly generate and send the Make code to the system as long as the key is held down. The rate at which Make codes are generated can be programmed on both keyboards. The 84-key keyboard has a fixed set of keys (except for a few special function keys) that are capable of the repeat operation. The COMPAQ Enhanced Keyboard allows the user to designate a particular set of keys to perform the repeat operations. The set of keys that can perform the repeat operation is programmable by the system via commands.

Figure 8-2 shows the 84-key keyboard. Figure 8-3 shows the COMPAQ Enhanced Keyboard.

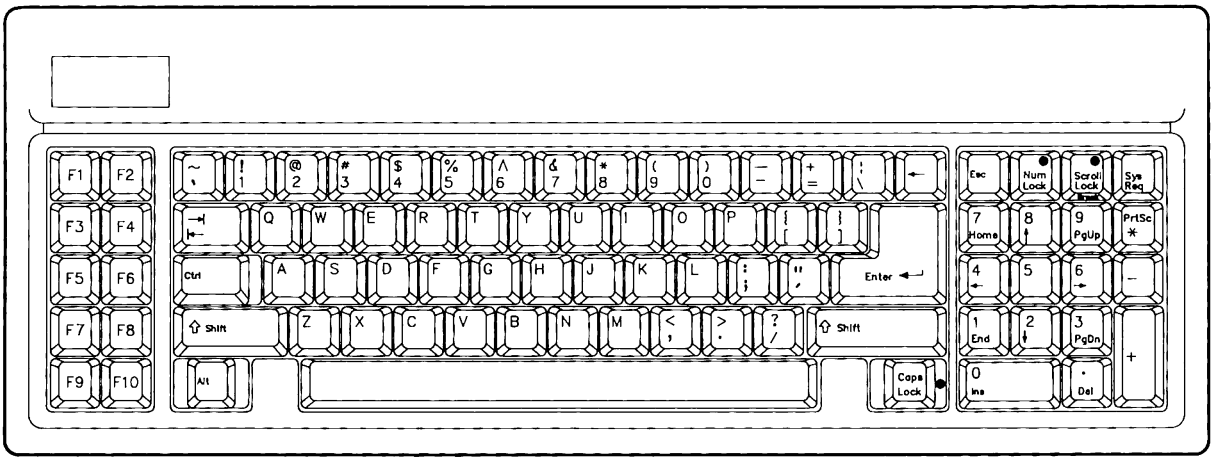


Figure 8-2. 84-Key Keyboard (U.S. English)

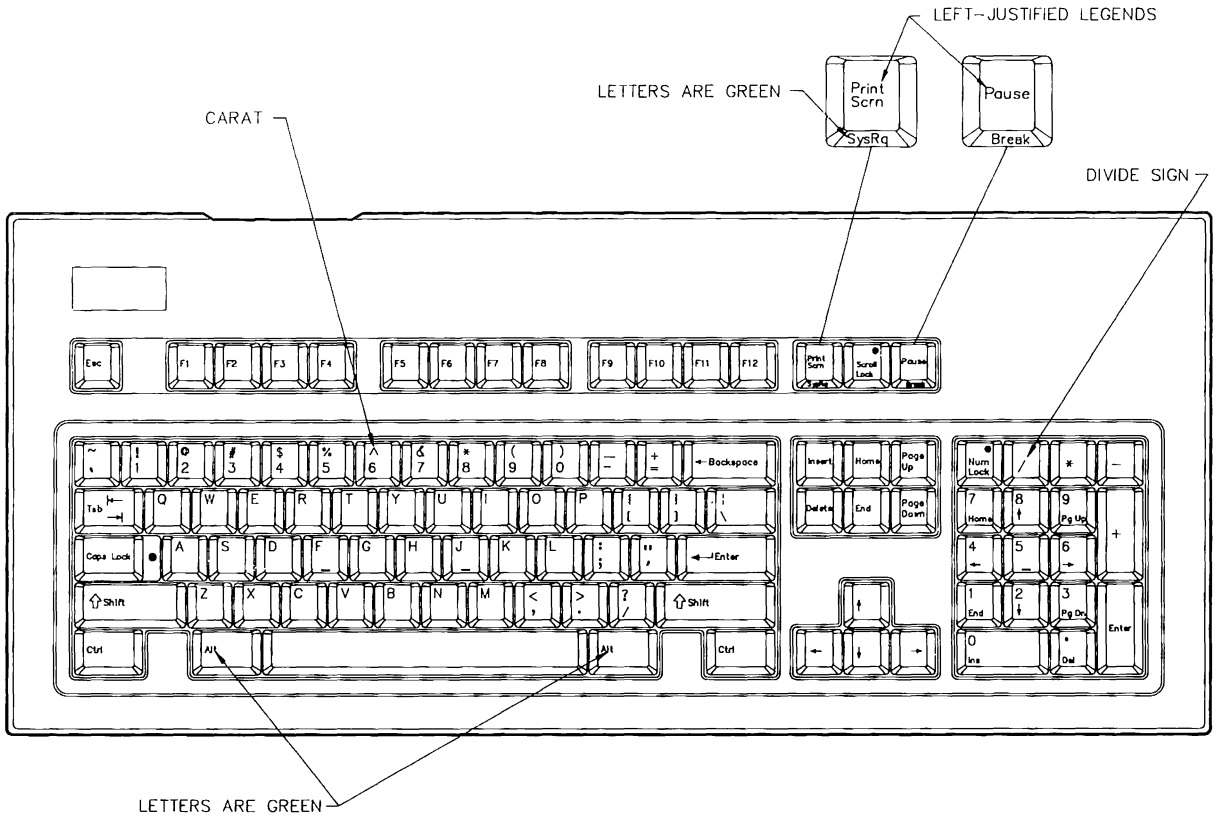


Figure 8-3. COMPAQ Enhanced Keyboard (U.S. English)

8.3 KEYBOARD COMMUNICATIONS INTERFACE

Both keyboards use a bidirectional, asynchronous interface for communications with the system. The keyboard cable is a 4-conductor, shielded cable.

The keyboard data (KBDDATA) and keyboard clock (KBDCLK) signals use TTL-compatible voltage levels, with open-collector drivers.

Communication between the system and the keyboards is implemented with a protocol method, shown in Figure 8-4.

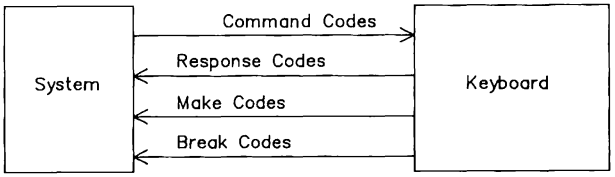


Figure 8-4. Keyboard Communication Protocol

Table 8-1. Keyboard Specifications for all Keyboards

	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286
Voltage	+ 12 VDC	+ 5 VDC
Tolerance	± 15%	± 10%
Current	250 mA (maximum)	250 mA (maximum)
Cable Length:		
Coiled	20 in. (51 cm)	38 in. (97 cm)
Extended	57 in. (145 cm)	75 in. (190 cm)

Communication Protocol

The communications link between the system and keyboard is bidirectional. For status information, the system controls the communications link. For data communication, either the system or the keyboard can put data on the data line, but not at the same time. Clock pulses are always required to transfer data generated by the keyboard in either direction.

Commands from the System

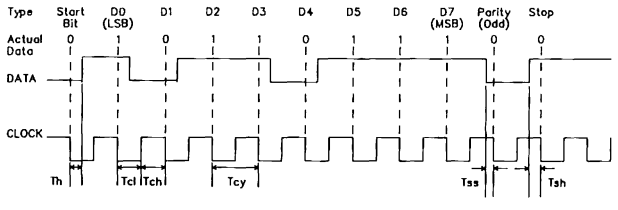
The system can send various commands to the keyboard. When the keyboard is transmitting data to the system, the system first clamps the CLOCK signal line to request a keyboard transmission halt. To ensure that the keyboard recognizes the system's request, the CLOCK line must remain low (0) for at least 60 us. If the keyboard's transmission is past the rising edge of the parity bit's CLOCK pulse, the keyboard completes its transmission before clocking in the system command. If the CLOCK line was clamped low prior to the rising edge of the parity bit clock pulse, the aborted transmission is loaded into the keyboard FIFO buffer.

When the system is ready to transmit a command to the keyboard, it sets the DATA line low (0). This action serves as both a Request-to-Send and a start bit. On detecting the DATA line low, the keyboard sets the CLOCK line low, causing the start bit to be clocked out of the system. The system then places the least-significant bit (LSB, data bit <0>) on the DATA line and the keyboard clocks this bit out of the system as shown in Figure 9-5. This process continues until all 8 data bits are clocked out of the system.

After all data bits are clocked out of the system, the system places an odd parity bit on the DATA line. The keyboard repeats its clocking of the parity bit as before. The keyboard then sets the DATA line low and clocks this line to the system for a stop bit. When the keyboard receives the stop bit, the system clamps the CLOCK line low to inhibit the keyboard while it is processing the received data.

After the keyboard receives a system command, the keyboard returns an ACK code to the system. If a parity error invalid code or time out occurs, a RESEND command is sent to the system. (For more information on the ACK code and RESEND, see the section titled "84-Key Keyboard Responses to the System" in this chapter.)

Figure 8-5 shows the timing of system-to-keyboard transmissions.



Code = EDh

Symbol	Parameter	Minimum	Maximum
Tcy	Cycle Time	60 us	80 us
Tcl	Clock Low	25 us	35 us
Tch	Clock High	25 us	45 us
Th	Data Hold	0 us	25 us
Tss	Stop Bit Setup	8 us	20 us
Tsh	Stop Bit Hold	15 us	25 us

Notes: 1. DATA signal clamped low by system, used as RTC signal.
2. DATA signal clamped low by keyboard as Stop Bit.
3. CLOCK signal clamped low by system to inhibit keyboard.

Figure 8-5. System-to-Keyboard Timing Transmissions

8.4 KEYBOARD FUNCTIONS

This section describes the unique functions of each keyboard. These descriptions refer to the U.S. keyboards only, because key numbers differ for the various international keyboards. The layouts of the international keyboards are illustrated in Section 8.6, International Keyboards.

84-Key Keyboard

The keyboard generates a fixed set of Make and Break codes for each of the keys on the 84-key keyboard. When a key is pressed, the keyboard sends that key's Make code to the system.

When a key is released, the keyboard sends two keycodes forming the Break Code: F0h, followed by that key's Make code to the system.

Figure 8-6 shows a layout of the 84-key keyboard and the position number assigned to each key. Table 8-2 lists the Make codes for each key on the 84-key

keyboard.

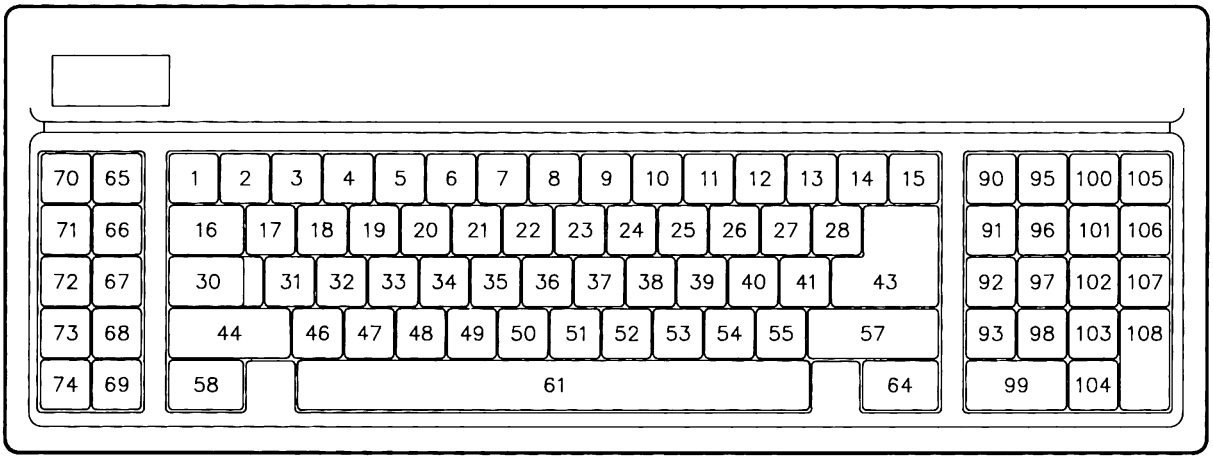


Figure 8-6. Assigned Position Number for Each Key on the 84-Key Keyboard

Table 8-2. Legend and Keycode Data for the U.S. 84-Key Keyboard

Location	Legend (Top of Cap)		Make Code
1	~	`	0E
2	!	1	16
3	@	2	1E
4	#	3	26
5	$	4	25
6	%	5	2E
7	^	6	36
8	&	7	3D
9	*	8	3E
10	(	9	46
11	)	0	45
12	_	-	4E
13	+	=	55
14	|	\	5D
15	(BackSpace)		66
16	(Back Tab) (Tab)		0D
17	Q		15
18	W		1D
19	E		24
20	R		2D
21	T		2C
22	Y		35
23	U		3C
24	I		43
25	O		44

(Continued)

Table 8-2. (Continued)

Location	Legend (Top of Cap)		Make Code
26	P		4D
27	{	[	54
28	}	]	5B
30	CTRL		14
31	A		1C
32	S		1B
33	D		23
34	F		2B
35	G		34
36	H		33
37	J		3B
38	K		42
39	L		4B
40	:	;	4C
41	"	'	52
43	ENTER		5A
44	LEFT SHIFT		12
46	Z		1A
47	X		22
48	C		21
49	V		2A
50	B		32
51	N		31
52	M		3A
53	<	,	41

(Continued)

Table 8-2. (Continued)

Location	Legend (Top of Cap)	Make Code
54	> .	49
55	? /	4A
57	(Right) SHIFT	59
58	ALT	11
61	(Space Bar)	29
64	CAPS LOCK	58
65	F2	05
66	F4	06
67	F6	04
68	F8	0C
69	F10	03
70	F1	05
71	F3	04
72	F5	03
73	F7	83
74	F9	01
90	ESC	76
91	7 HOME	6C
92	4 (Left Arrow)	6B
93	1 END	69
95	NUM LOCK	77
96	8 (Up Arrow)	75
97	5	73
98	2 (Down Arrow)	72
99	0 INS	70

(Continued)

Table 8-2. (Continued)

Location	Legend (Top of Cap)	Make Code
100	SCROLL LOCK	7E
101	9 PGUP	7D
102	6 (Right Arrow)	74
103	3 PGDN	7A
104	. DEL	71
105	SYS REQ	84
106	PRINT SCREEN *	7C
107	-	7B
108	+	79

System/Keyboard Commands and Acknowledgments

The commands sent by the system are listed in Table 8-3.

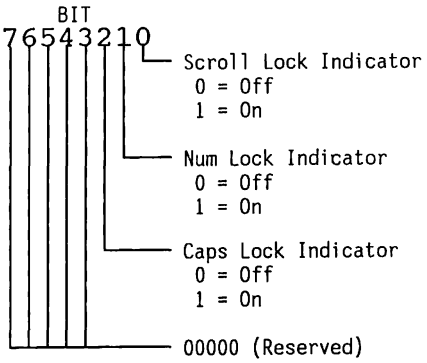
Table 8-3. System Commands to the Keyboard

Code	Function
EDh	Set Status Indicators
EEh	Echo Command (Diagnostic Aid)
EFh..F2h	Reserved--No operation
F3h	Set Key Repeat Rate
F4h	Enable the Keyboard
F5h	Disable Keyboard Scanning
F6h	Set Default Conditions
F7h..FDh	Reserved--No operation
FEh	Resend Command
FFh	Reset Command

SET STATUS INDICATORS (EDh)

The Set Status Indicators (EDh) command is a 2-byte command that changes the state of the keyboard LED indicators. After receiving this command, the keyboard halts scanning, returns an ACK (acknowledgment) code to the system, and waits for the system to send the option byte. The option byte indicates which LED indicators are to be affected.

When the option byte is received, the keyboard sets the status indicator, returns an ACK code, and resumes scanning if previously enabled. If another command is received while the keyboard is waiting for the option byte, the Set Status Indicators command is aborted and the new command is executed. No change to the LED indicators occurs. The status byte is formatted as follows:



Bit <7> is the most-significant bit (MSB), and bit <0> is the least-significant bit (LSB).

ECHO (EEh)

The Echo (EEh) command is used for diagnostics. After receiving this command, the keyboard returns an Echo (EEh) response.

NOP (EFh..F2h)

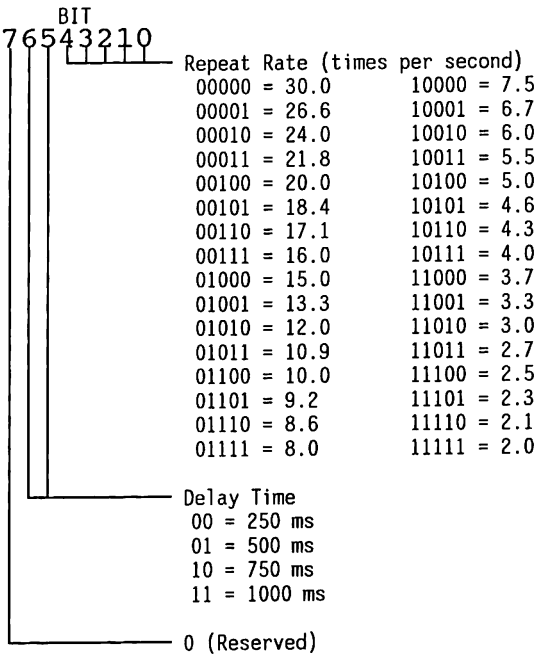
The keyboard responds to the NOP command with an ACK code. No other action is taken.

SET KEY REPEAT RATE (F3h)

The Set Key Repeat Rate (F3h) command is a 2-byte command that changes the key-repeat delay and rate values.

Once the keyboard receives the Set Key Repeat Rate command, it stops scanning and returns an ACK code. The system then sends a byte that contains the repeat rate and delay time values. The repeat rate is the number of times the key is repeated every second. The delay time is the length of time a key must be held down before the key repeat function begins. The keyboard then returns an ACK code and remains in the disabled state until it receives the Enable command.

The format for the Set Key Repeat Rate/Delay Time byte is as follows:



ENABLE (F4h)

The Enable (F4h) command causes the keyboard to start its scanning function. After receiving this command, the keyboard returns an ACK code, clears the output buffer, and starts scanning.

DISABLE (F5h)

The Disable (F5h) command halts keyboard scanning. After receiving this command, the keyboard returns an ACK (acknowledge) code to the system.

SET DEFAULT CONDITIONS (F6h)

The Set Default Conditions (F6h) command causes the keyboard to send an ACK code and its default conditions to the system. If the keyboard was enabled prior to receiving the Set Default Conditions command, the keyboard continues scanning.

NOP (F7h..FDh)

The keyboard responds to the NOP command with an ACK code. No other action is taken.

RESEND (FEh)

The Resend (FEh) command is issued to the keyboard only after a keyboard transmission. The keyboard responds by retransmitting the most recent byte transmitted to the system. If the most recent byte was Resend, the keyboard transmits the byte sent before the Resend command.

RESET (FFh)

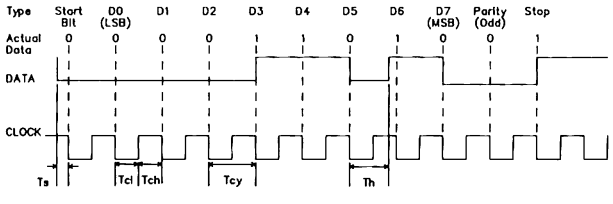
The Reset (FFh) command is accepted by the keyboard by returning an ACK code to the system. For the system to accept the ACK code, the system must raise the CLOCK and DATA lines for at least 500 us. After receiving the Reset command, the keyboard is disabled until either the ACK code is accepted by the system or another command is issued to the keyboard.

If the Reset ACK code is accepted by the system as described above, the keyboard clears its character output buffer, sets the default repeat-key rate, and turns all LED indicators ON, then OFF. Once this process is completed, an ACK code is sent to the system followed by a Power-on Complete response (an AAh code). At this point, the keyboard returns to normal operation.

84-Key Keyboard Responses to the System

Before the keyboard responses are sent to the system, the keyboard verifies the status of two signals, CLOCK and DATA. Should the CLOCK signal be low (=0), the keyboard recognizes an inhibited state and loads the keystrokes into its buffer as previously described. Once the inhibited state is removed, the keystrokes are sent to the system. If the data signal is low, the keyboard recognizes a Request-To-Send condition from the system. Keystrokes are also loaded into the keyboard buffer for this state and the keyboard prepares to receive the system commands. Once this state is cleared, the stored keystrokes are sent to the system.

The keyboard initiates the transmission of keystrokes and responses to system commands to the system only when both the CLOCK and DATA signals are high (=1). Data transmitted to the system consists of 11 bits: a start bit, 8 data bits, an odd parity bit, and a stop bit. Figure 8-7 shows the timing transmission for keyboard responses sent to the system.



Code = 58h

Symbol	Parameter	Minimum	Maximum
Tcy	Cycle Time	60 us	80 us
Tcl	Clock Low	30 us	35 us
Tch	Clock High	30 us	45 us
Ts	Data Setup	8 us	14 us
Th	Data Hold	45 us	62 us

Note: CLOCK signal clamped low by system to inhibit keyboard.

Figure 8-7. Timing Diagram Standard for Keyboard-to-System Transmissions

The system can halt a keyboard transmission by setting the CLOCK signal low. The keyboard checks the CLOCK signal every 60 us to verify the signal's state. If the CLOCK signal is detected as low, the keyboard finishes this transmission only if the rising edge of the CLOCK pulse for the parity bit has not occurred.

Responses sent from the keyboard to the system are listed in Table 8-4.

Table 8-4. Keyboard Responses to the System

Code	Function
00h	Overrun
AAh	Power-On Completed
EEh	Echo
F0h	Break
FAh	ACK
FEh	Resend
FDh	Failure

OVERRUN (00h)

The keyboard places 00h as the last character in the keyboard character buffer to indicate a buffer overrun.

POWER-ON COMPLETED (AAh)

The keyboard transmits the Power-On Completed (AAh) response to the system upon completion of power on and removal of the keyboard inhibit state, or on successful completion of a Reset command from the system.

ECHO (EEh)

The keyboard transmits an Echo response to the system in response to the system's Echo command. This response is substituted for the ACK code.

BREAK (F0h)

When a key is released, the keyboard transmits a Break prefix (F0h), followed by the Make code for that particular key.

ACK (FAh)

The keyboard transmits an ACK (FAh) code in response to valid system commands, except for an Echo or Resend command. If the command is not valid or had a parity error, the keyboard sends a Resend command to the system instead of an ACK. If the system begins a transmission during an ACK code response, the keyboard discards this ACK code and the new system command is accepted and processed.

RESEND (FEh)

The keyboard transmits a Resend (FEh) response to the system in response to an invalid system command. The Resend response instructs the system to retransmit its last command.

COMPAQ Enhanced Keyboard

The COMPAQ Enhanced Keyboard is capable of performing all the functions of the 84-key keyboard. It also supports a number of additional modes and functions. The most outstanding features are a separate cursor control key cluster and the addition of keys F11 and F12. Figure 8-8 shows a layout of the keyboard and the position number assigned to each key.

NOTE: Position numbers apply only to the U.S. English keyboard; position numbers are different for the international keyboard.

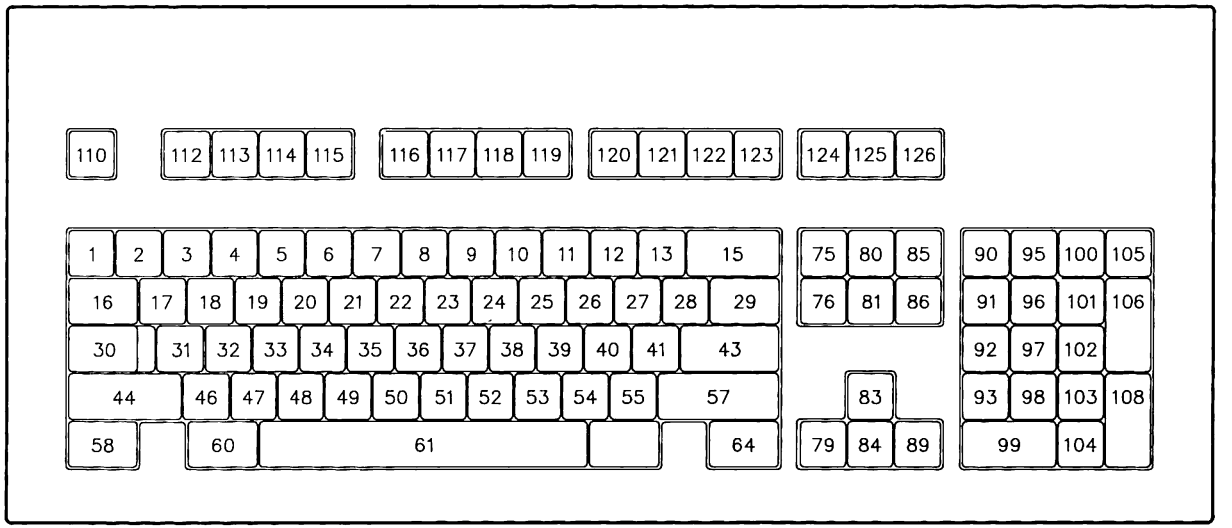


Figure 8-8. Assigned Position Number for Each Key on the COMPAQ Enhanced Keyboard

The COMPAQ Enhanced Keyboard has three operating modes. Each can be selected by using keyboard commands, which are discussed in more detail later in this section. These modes offer a range of functionality and compatibility features to software applications.

Mode 1

In Mode 1, the scan codes generated by the enhanced keyboard are compatible with keyboards used in 8088- and 8086-based systems. To access Mode 1 scan codes, send the F0h keyboard command to the keyboard and disable the 8042 scan code translation mapping. The scan codes generated by Mode 1 of the keyboard are identical to system codes required for input to the BIOS. To obtain system codes and status information, BIOS INT 16h functions AH = 00h, 01h, and 02h should be used by applications operating the keyboard in Mode 1.

Mode 2

In Mode 2, the COMPAQ Enhanced Keyboard generates scan codes compatible with the 84-key keyboard.

Mode 2 is the default mode of the COMPAQ Enhanced Keyboard that is selected by the COMPAQ DESKPRO 286 during power-on initialization. In this mode, the 8042 keyboard controller scan code translation is enabled so that the scan codes generated by the keyboard can be translated to the system codes required by the BIOS. Except for the system codes associated with the new keys of the COMPAQ Enhanced Keyboard, the system codes (after translation) resemble the scan codes generated by the keyboard in Mode 1. To properly access the system codes generated by the new keys of the COMPAQ Enhanced Keyboard, applications should use BIOS functions INT 16h AH = 10h, 11h, and 12h instead of the traditional functions INT 16h AH = 00h, 01h, and 02h. During power-on, NUM LOCK is set active to enable the numeric keypad.

Mode 3

Mode 3 generates a scan code set different from those of Modes 1 or 2. In this mode, the 8042 keyboard controller translation must be disabled, because the 8042 is not capable of translating the scan code set generated. Applications that want to use the COMPAQ Enhanced Keyboard in Mode 3 should explicitly select this mode by using the F0h keyboard command. These applications must assume responsibility for directly handling the scan codes generated by the keyboard since the 8042 and BIOS are not capable of handling the scan code set generated in Mode 3.

Tables 8-5 through 8-9 lists the scan code sets generated by the COMPAQ Enhanced Keyboard Modes 1, 2, and 3. For Mode 1, a Break code consists of a Make code with the high bit (bit <7>) set to 1. For example, 9Ch is the Break code for 1Ch, and A0h is the Break code for 20h. For Modes 2 and 3, a Break code is a 2-byte sequence consisting of the Make code immediately preceded by the F0h. For example, F0h 0Eh is the Break code for 0Eh.

In Modes 2 and 3, the COMPAQ Enhanced Keyboard generates the Break codes, F0h precedes the Make code to signify a Break code sequence. In Mode 1, the keyboard generates the Break codes by setting the most-significant bit of the Make code to a 1.

Table 8-5. COMPAQ Enhanced Keyboard Scan Codes for Mode 1

Key Location	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
1	`	29	
2	1	02	
3	2	03	
4	3	04	
5	4	05	
6	5	06	
7	6	07	
8	7	08	
9	8	09	
10	9	0A	
11	0	0B	
12	-	0C	
13	+	0D	
15	BACKSPACE	0E	
16	TAB	0F	
17	Q	10	
18	W	11	
19	E	12	

Notes: 1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller board.

2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.

(Continued)

Table 8-5. (Continued)

Key Location	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
20	R	13	
21	T	14	
22	Y	15	
23	U	16	
24	I	17	
25	O	18	
26	P	19	
27	[	1A	
28	]	1B	
29	\	2B	
30	CAPS LOCK	3A	
31	A	1E	
32	S	1F	
33	D	20	
34	F	21	
35	G	22	
36	H	23	
37	J	24	
38	K	25	
39	L	26	
40	;	27	
41	"	28	
42		2B	(International only)
43	ENTER	1C	
44	(Left) SHIFT	2A	
45		56	(International only)

(Continued)

Table 8-5. (Continued)

Key Location	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
46	Z	2C	
47	X	2D	
48	C	2E	
49	V	2F	
50	B	30	
51	N	31	
52	M	32	
53	,	33	
54	.	34	
55	/	35	
57	(Right) SHIFT	36	
58	CTRL	1D	
60	(Left) ALT	38	
61	(Space Bar)	39	
62	(Right) ALT	E0 38	
64	(Right) CTRL	E0 1D	

Notes: 1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.

2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.

(Continued)

Table 8-5. (Continued)

Key Location	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
75	INS	E0 52	3
76	DEL	E0 53	3
79	(Left Arrow)	E0 4B	3
80	HOME	E0 47	3
81	END	E0 4F	3
83	(Up Arrow)	E0 48	3
84	(Down Arrow)	E0 50	3
85	PGUP	E0 49	3
86	PGDN	E0 51	3
89	(Right Arrow)	E0 4D	3
90	NUM LOCK	45	4
91	7	47	4
92	4	4B	4
93	1	4F	4
95	/	E0 35	4
96	8	48	4
97	5	4C	4
98	2	50	4
99	0	52	4
100	*	37	4
101	9	49	4
102	6	4D	4
103	3	51	4
104	.	53	4
105	-	4A	4
106	+	4E	4
108	ENTER	E0 1C	4

(Continued)

Table 8-5. (Continued)

Key Location	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
110	ESC	01	
112	F1	3B	
113	F2	3C	
114	F3	3D	
115	F4	3E	
116	F5	3F	
117	F6	40	
118	F7	41	
119	F8	42	
120	F9	43	
121	F10	44	
122	F11	57	
123	F12	58	
124	PRINT SCREEN	E0 2A E0 37	
125	SCROLL LOCK	46	
126	PAUSE	E1 1D 45 E1 9D C5	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.
3. Scan codes listed are for NUM LOCK inactive.
4. This is a numeric cluster key.

The following keys have special codes during Mode 1 operation depending on the state of the SHIFT, NUM LOCK, ALT, and CTRL keys. Table 8-6 lists the scan codes generated by these keys.

Table 8-6. Combination Scan Codes for Mode 1

Key Location	U.S. Key Legend	Scan Code Make/Break
Shift Active with NUM LOCK OFF:		
75	INS	E0 AA E0 52
76	DEL	E0 AA E0 53
79	(Left Arrow)	E0 AA E0 4B
80	HOME	E0 AA E0 47
81	END	E0 AA E0 4F
83	(Up Arrow)	E0 AA E0 48
84	(Down Arrow)	E0 AA E0 50
85	PGUP	E0 AA E0 49
86	PGDN	E0 AA E0 51
89	(Right Arrow)	E0 AA E0 4D
Shift Active with NUM LOCK ON:		
75	INS	E0 52
76	DEL	E0 53
79	(Left Arrow)	E0 4B
80	HOME	E0 47
81	END	E0 4F
83	(Up Arrow)	E0 48
84	(Down Arrow)	E0 50
85	PGUP	E0 49
86	PGDN	E0 51
89	(Right Arrow)	E0 4D
Shift Active with NUM LOCK OFF:		
95	KEYPAD /	E0 AA E0 35/E0 B5 E0 2A
Shift Active or CTRL Active:		
124	PRINT SCREEN	E0 37 / E0 B7
ALT Active:		
124	PRINT SCREEN	54 / D4
CTRL Active:		
126	PAUSE	E0 46 E0 C6

Note: Key 126 is not typematic and generates a scan code only on the Make condition.

Table 8-7. COMPAQ Enhanced Keyboard Scan Codes for Mode 2

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
1	`	0E	29	
2	1	16	02	
3	2	1E	03	
4	3	26	04	
5	4	25	05	
6	5	2E	06	
7	6	36	07	
8	7	3D	08	
9	8	3E	09	
10	9	46	0A	
11	0	45	0B	
12	-	4E	0C	
13	+	55	0D	
15	BACKSPACE	66	0E	
16	TAB	0D	0F	
17	Q	15	10	
18	W	1D	11	
19	E	24	12	
20	R	2D	13	
21	T	2C	14	
22	Y	35	15	
23	U	3C	16	
24	I	43	17	
25	O	44	18	
26	P	4D	19	
27	[	54	1A	
28	]	5B	1B	

(Continued)

Table 8-7. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
29	\	5D	2B	
30	CAPS LOCK	58	3A	
31	A	1C	1E	
32	S	1B	1F	
33	D	23	20	
34	F	2B	21	
35	G	34	22	
36	H	33	23	
37	J	3B	24	
38	K	42	25	
39	L	4B	26	
40	;	4C	27	
41	"	52	28	
42		5D	(International only)	
43	ENTER	5A	1C	
44	(Left) SHIFT	12	2A	
45		61	(International only)	

Notes: 1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.

2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.

(Continued)

Table 8-7. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
46	Z	1A	2C	
47	X	22	2D	
48	C	21	2E	
49	V	2A	2F	
50	B	32	30	
51	N	31	31	
52	M	3A	32	
53	,	41	33	
54	.	49	34	
55	/	4A	35	
57	(Right) SHIFT	59	36	
58	(Left) CTRL	14	1D	
60	(Left) ALT	11	38	
61	(Space)	29	39	
62	(Right) ALT	E0 11	E0 38	
64	(Right) CTRL	E0 14	E0 1D	
75	INS	E0 70	E0 52	3
76	DEL	E0 71	E0 53	3
79	(Left Arrow)	E0 6B	E0 4B	3
80	HOME	E0 6C	E0 47	3
81	END	E0 69	E0 4F	3
83	(Up Arrow)	E0 75	E0 48	3
84	(Down Arrow)	E0 72	E0 50	3
85	PGUP	E0 7D	E0 49	3
86	PGDN	E0 7A	E0 51	3
89	(Right Arrow)	E0 74	E0 4D	3
90	NUM LOCK	77	45	4
91	7	6C	47	4

(Continued)

Table 8-7. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
92	4	6B	4B	4
93	1	69	4F	4
95	/	E0 4A	E0 35	4
96	8	75	48	4
97	5	73	4C	4
98	2	72	50	4
99	0	70	52	4
100	*	7C	37	4
101	9	7D	49	4
102	6	74	4D	4
103	3	7A	51	4
104	.	71	53	4
105	-	7B	4A	4
106	+	79	4E	4
108	ENTER	E0 5A	E0 1C	4
110	ESC	76	01	
112	F1	05	3B	
113	F2	06	3C	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.
3. Scan codes listed are for NUM LOCK inactive.
4. This is a numeric cluster key.

(Continued)

Table 8-7. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
114	F3	04	3D	
115	F4	0C	3E	
116	F5	03	3F	
117	F6	0B	40	
118	F7	83	41	
119	F8	0A	42	
120	F9	01	43	
121	F10	09	44	
122	F11	78	57	
123	F12	07	58	
124	PRINT SCREEN	E0 12 E0 7C	E0 2A E0 37	
125	SCROLL LOCK	7E	46	
126	PAUSE	E1 14 77 E1 F0 14 F0 77	E1 1D 45 E1 9D C5	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.
3. Scan codes listed are for NUM LOCK inactive.
4. This is a numeric cluster key.

Combination scan codes for Mode 2 are the same as for Mode 1. Refer to Table 8-6 for the combination scan codes.

The following keys have special codes during Mode 2 operation depending on the state of the SHIFT, NUM LOCK, ALT, and CTRL keys. Table 8-8 lists the scan codes generated by these keys.

Table 8-8. Combination Scan Codes for Mode 2

Key Location	U.S. Key Legend	Scan Code
Shift Active with NUM LOCK OFF:		
75	INS	E0 F0 12 E0 70
76	DEL	E0 F0 12 E0 71
79	(Left Arrow)	E0 F0 12 E0 6B
80	HOME	E0 F0 12 E0 6C
81	END	E0 F0 12 E0 69
83	(Up Arrow)	E0 F0 12 E0 75
84	(Down Arrow)	E0 F0 12 E0 72
85	PGUP	E0 F0 12 E0 7D
86	PGDN	E0 F0 12 E0 7A
89	(Right Arrow)	E0 F0 12 E0 74
Shift Inactive with NUM LOCK ON:		
75	INS	E0 12 E0 70
76	DEL	E0 12 E0 71
79	(Left Arrow)	E0 12 E0 6B
80	HOME	E0 12 E0 6C
81	END	E0 12 E0 69
83	(Up Arrow)	E0 12 E0 75
84	(Down Arrow)	E0 12 E0 72
85	PGUP	E0 12 E0 7D
86	PGDN	E0 12 E0 7A
89	(Right Arrow)	E0 12 E0 74
Shift Active with NUM LOCK OFF:		
95	Keypad /	E0 F0 12 4A

(Continued)

Table 8-8. (Continued)

Key Location	U.S. Key Legend	Scan Code
Shift Active or CTRL Active:		
124	PRINT SCREEN	E0 7C
ALT Active:		
124	PRINT SCREEN	84
CTRL Active:		
126	PAUSE	E0 7E E0 F0 7E

Note: Key 126 is not a repeat key and generates a scan code only on the Make condition.

Table 8-9. COMPAQ Enhanced Keyboard Scan Codes for Mode 3

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2) Note
1		0E
2	1	16
3	2	1E
4	3	26
5	4	25
6	5	2E
7	6	36
8	7	3D
9	8	3E
10	9	46
11	0	45
12	-	4E
13	+	55
15	BACKSPACE	66
16	TAB	0D
17	Q	15
18	W	1D

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.

(Continued)

Table 8-9. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Note
19	E	24	
20	R	2D	
21	T	2C	
22	Y	35	
23	U	3C	
24	I	43	
25	O	44	
26	P	4D	
27	[	54	
28	]	5B	
29	\	5C	
30	CAPS LOCK	14	
31	A	1C	
32	S	1B	
33	D	23	
34	F	2B	
35	G	34	
36	H	33	
37	J	3B	
38	K	42	
39	L	4B	
40	;	4C	
41	"	52	
42		53	(International only)
43	ENTER	5A	
44	(Left) SHIFT	12	
45		13	(International only)

(Continued)

Table 8-9. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Note
46	Z	1A	
47	X	22	
48	C	21	
49	V	2A	
50	B	32	
51	N	31	
52	M	3A	
53	,	41	
54	.	49	
55	/	4A	
57	(Right) SHIFT	59	
58	(Left) CTRL	11	
60	(Left) ALT	19	
61	(Space Bar)	29	
62	(Right) ALT	39	
64	(Right) CTRL	58	
75	INS	67	
76	DEL	64	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.

(Continued)

Table 8-9. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
79	(Left Arrow)	61	
80	HOME	6E	
81	END	65	
83	(Up Arrow)	63	
84	(Down Arrow)	60	
85	PGUP	6F	
86	PGDN	6D	
89	(Right Arrow)	6A	
90	NUM LOCK	76	3
91	7	6C	3
92	4	6B	3
93	1	69	3
95	/	77	3
96	8	75	3
97	5	73	3
98	2	72	3
99	0	70	3
100	*	7E	3
101	9	7D	3
102	6	74	3
103	3	7A	3
104	.	71	3
105	-	84	3
106	+	7C	3

(Continued)

Table 8-9. (Continued)

Key Code	U.S. Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
108	ENTER	79	3
110	ESC	08	
112	F1	07	
113	F2	0F	
114	F3	17	
115	F4	1F	
116	F5	27	
117	F6	2F	
118	F7	37	
119	F8	3F	
120	F9	47	
121	F10	4F	
122	F11	56	
123	F12	5E	
124	PRINT SCREEN	57	
125	SCROLL LOCK	5F	
126	PAUSE	62	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for SHIFT, ALT, and CTRL inactive.
3. This is a numeric cluster key.

In addition to the commands supported by the 84-key keyboard, the COMPAQ Enhanced Keyboard supports a number of commands related to its enhanced programmable functions. Table 8-10 lists the additional commands supported by the COMPAQ Enhanced Keyboard.

Table 8-10. Additional Commands Supported by the COMPAQ Enhanced Keyboard

Command Code	Function
F2h	Requests the identification sequence from the keyboard. The keyboard should respond with an ACK and the 2-byte identification code. The enhanced keyboard identification sequence is ABh followed by 83h. The keyboard scanning is then enabled.
EFh, F1h	Keyboard does not acknowledge these commands. The keyboard transmits a Resend response and continues scanning for keys.
F0h	Selects one of three modes of operation for the COMPAQ Enhanced Keyboard. This is a 2-byte command sequence. The second byte specifies the mode of the COMPAQ Enhanced Keyboard. The second byte is as follows: 01 - Selects Mode 1 of the keyboard. 02 - Selects Mode 2 of the keyboard. 03 - Selects Mode 3 of the keyboard. Once the option byte is acknowledged, the keyboard establishes the new mode of operation and resumes scanning.

(Continued)

Table 8-10. (Continued)

Command Code	Function
F7h	Programs all keys to be able to perform the repeat function. Once the keyboard acknowledges the command, it resumes scanning if previously enabled. This command is enabled only during the Mode 3 keyboard operation.
F8h	Programs all keys to generate Make/Break codes. Once the keyboard acknowledges the command, it resumes scanning if previously enabled. This command is enabled only during Mode 3 keyboard operation.
F9h	Programs all keys to generate only Make codes. Once the keyboard acknowledges the command, it resumes scanning if previously enabled. This command is enabled only during Mode 3 keyboard operation.
FAh	Programs all keys for Make/Break and repeat operations. Once the keyboard acknowledges the command, it resumes scanning if previously enabled. This command is enabled only during Mode 3 keyboard operation.
FBh	Enables the repeat function of an individual key. A 2-byte command, of which the second byte is the Make code, it identifies the key to be affected by the command. This command is enabled only during Mode 3 keyboard operation. Keyboard scanning is disabled after this command. An Enable (F4h) command allows the keyboard to resume scanning.

(Continued)

Table 8-10. (Continued)

Command Code	Function
FCh	Programs an individual key to generate Make and Break codes. A 2-byte command, of which the second byte is the Make code, it identifies the key to be affected by the command. This command is enabled only during Mode 3 keyboard operation. Keyboard scanning is disabled after this command. An Enable (F4h) command allows the keyboard to resume scanning.
FDh	Programs an individual key to generate only Make codes. A 2-byte command, of which the second byte is the Make code, it identifies the key to be affected by the command. This command is enabled only during Mode 3 keyboard operation. Keyboard scanning is disabled after this command. An Enable (F4h) command allows the keyboard to resume scanning.
F5h	Disables the keyboard from the system. The keyboard acknowledges the command and resets to the following conditions: ■ Resets typematic rate to 10 characters per second ■ Sets typematic delay to 500 ms ■ Halts scanning ■ Clears keyboard buffer ■ Sets default key types (Mode 3 only) ■ Clears last typematic key ■ Awaits further system instructions

(Continued)

Table 8-10. (Continued)

Command Code	Function
F6h	The keyboard resets to the following conditions: ■ Resets typematic rate to 10 characters per second ■ Sets typematic delay to 500 ms ■ Clears keyboard buffer ■ Sets default key types (Mode 3 only) ■ Clears last typematic key ■ Continues to scan

Figure 8-9 shows the key legends associated with key 42 for the international COMPAQ Enhanced Keyboards. Figure 8-10 shows the legends for key 45. Table 8-11 lists the scan codes for these keys.

Table 8-11. International Scan Codes

Key	Mode 1 Scan Code (h)	Mode 2 Scan Code (h)	Mode 3 Scan Code (h)
42	2B	5D	53
45	56	61	13

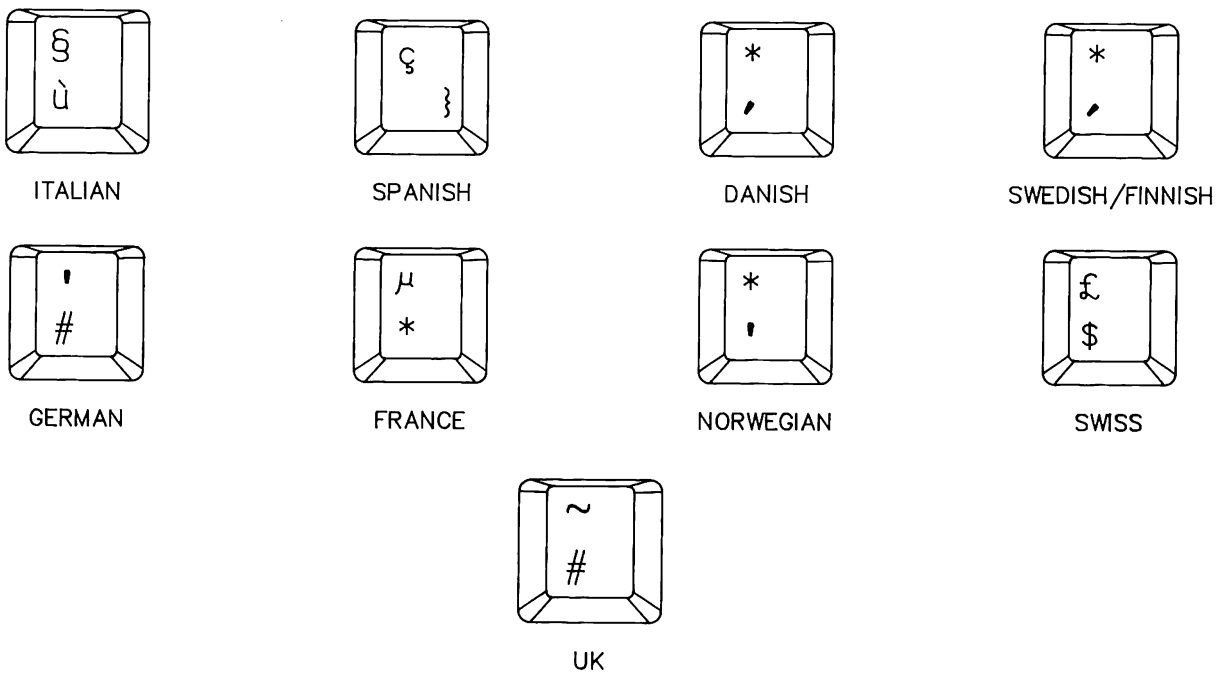


Figure 8-9. Key 42

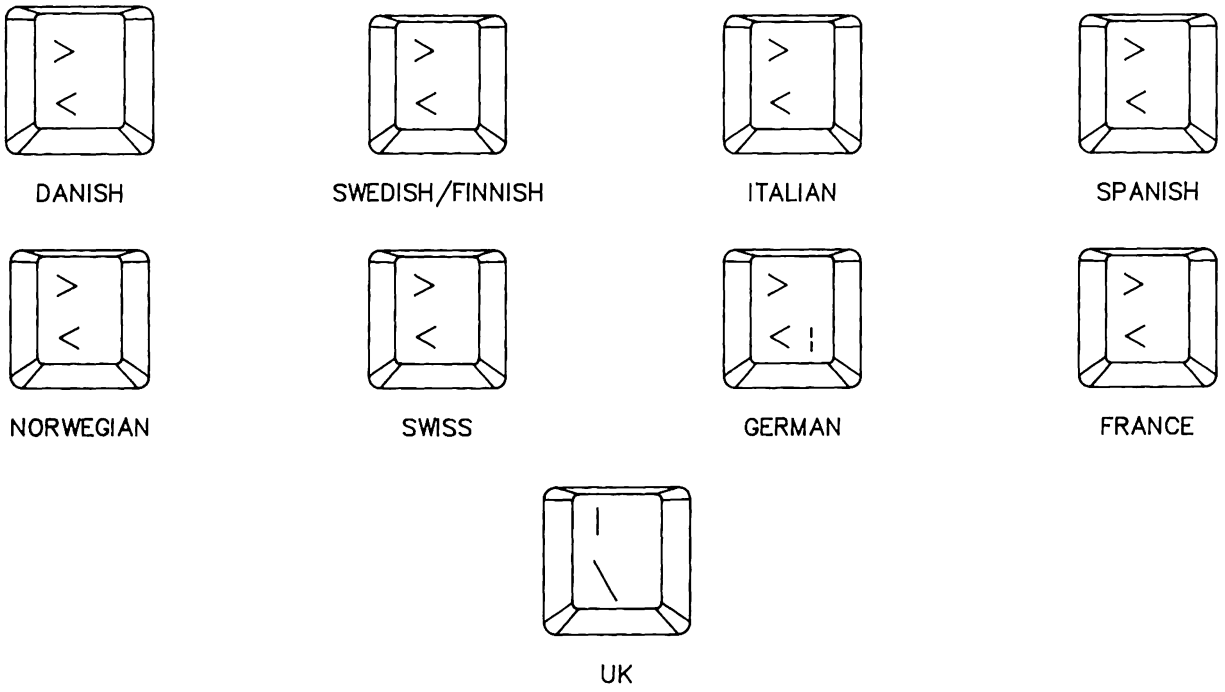


Figure 8-10. Key 45

8.5 CONNECTORS

The keyboard for the COMPAQ PORTABLE 286 uses a 6-pin modular-type connector, which is shown in Figure 8-11.

Both keyboards for the COMPAQ DESKPRO 286 use a 5-pin molded connector, which is shown in Figure 8-12.

Table 8-12 lists the keyboard connector signals.

Table 8-12. Keyboard Cable Connector Signals

COMPAQ DESKPRO 286 Pin	Signal
1	KBDCLK (Keyboard Clock Signal)
2	KBDDATA (Keyboard Data Signal)
3	Reserved (Note 1)
4	Signal Ground
5	Power (Note 2)
Shield	Chassis Ground

Notes:
1. Pin 3 on the COMPAQ PORTABLE 286 keyboard connector is +5 VDC.
2. Power for the COMPAQ PORTABLE 286 is +12 VDC. Power for the COMPAQ DESKPRO 286 is +5 VDC.

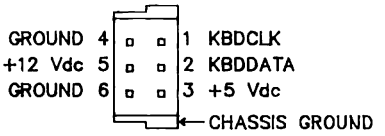


Figure 8-11. COMPAQ PORTABLE 286 Keyboard Connector

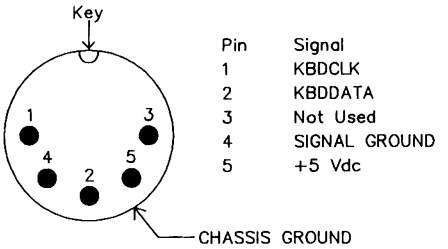


Figure 8-12. COMPAQ DESKPRO 286 Keyboard Connector

8.6 INTERNATIONAL KEYBOARDS

This section shows the international versions of the COMPAQ Enhanced Keyboard and the 84-key keyboard. Figures 8-13 through 8-22 show the version by country in alphabetic order.

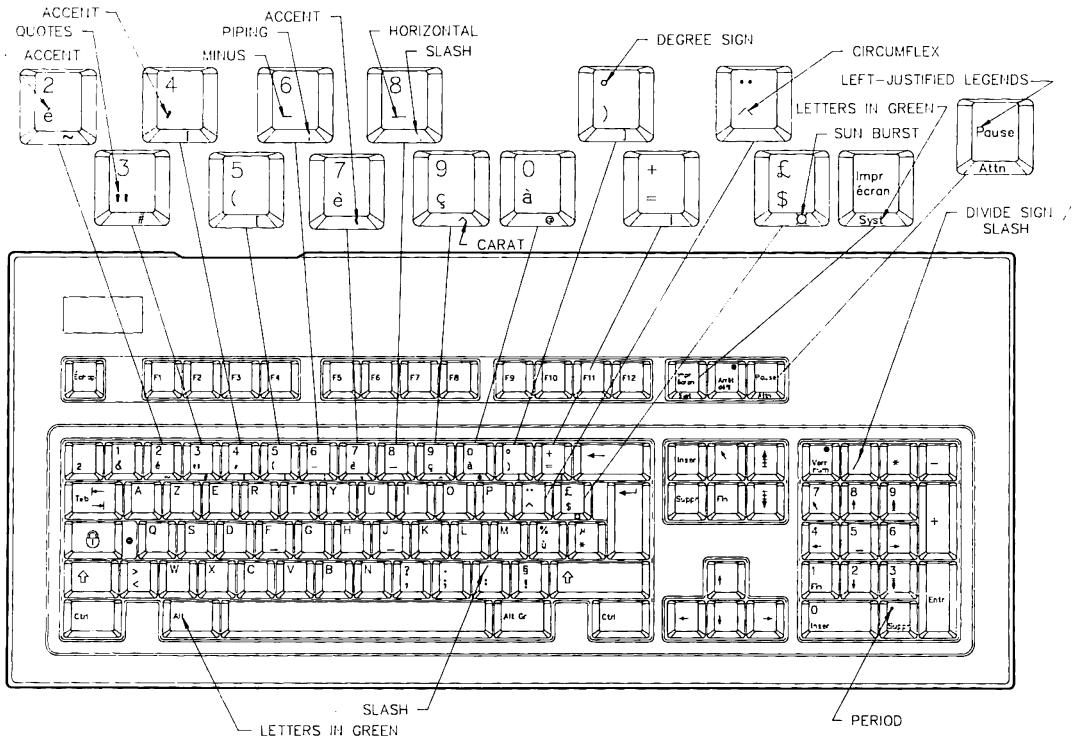


Figure 8-13. French Enhanced Keyboard

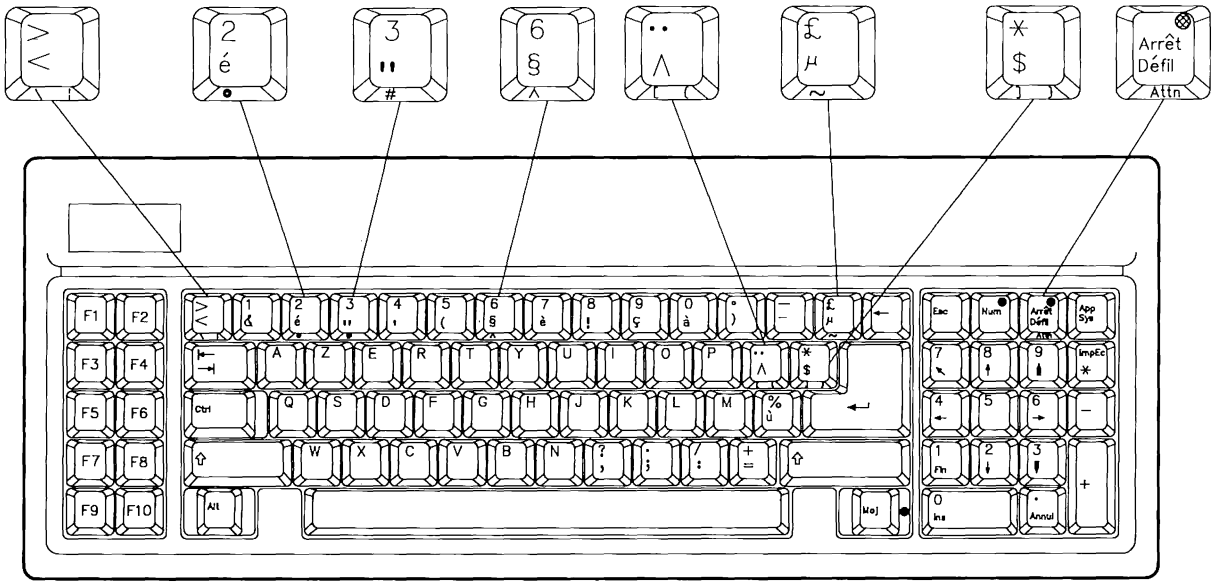


Figure 8-14. French 84-Key Keyboard

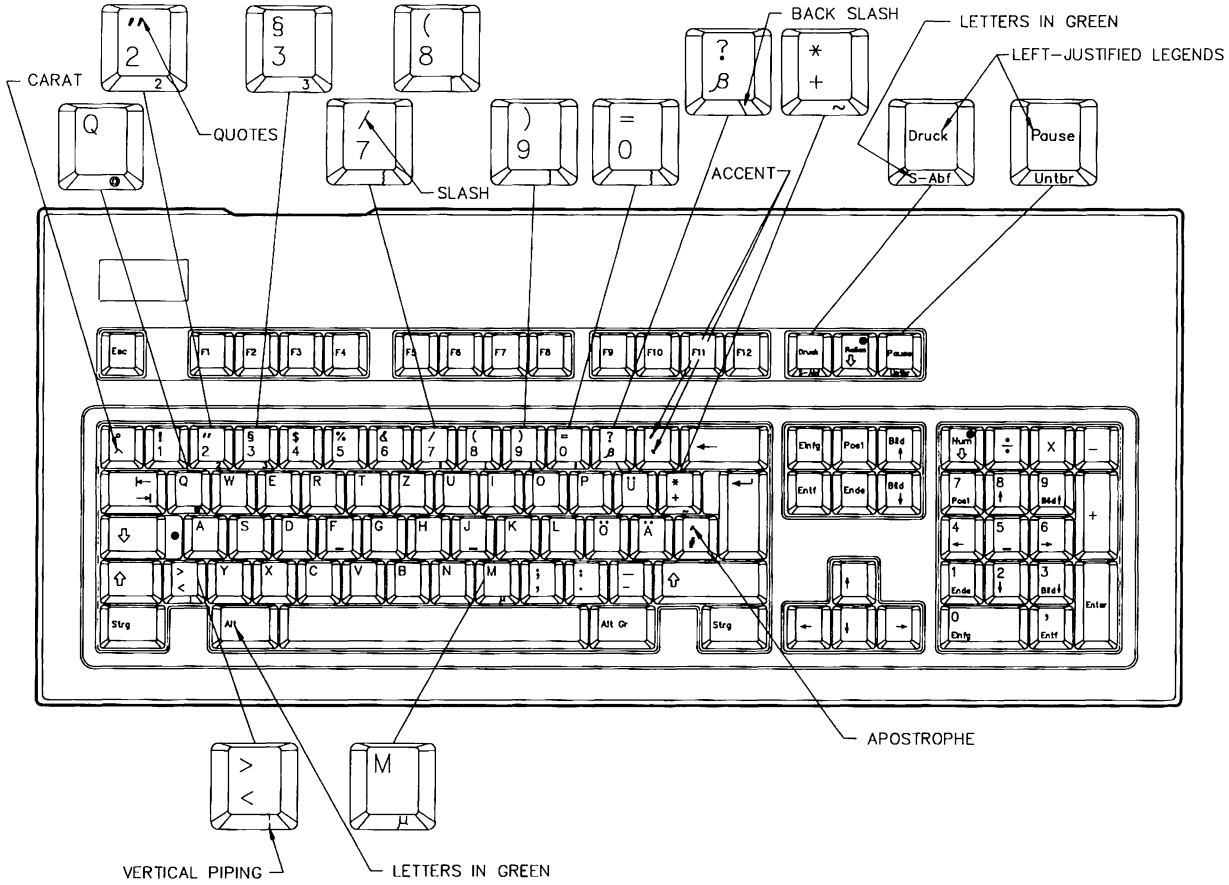


Figure 8-15. German Enhanced Keyboard

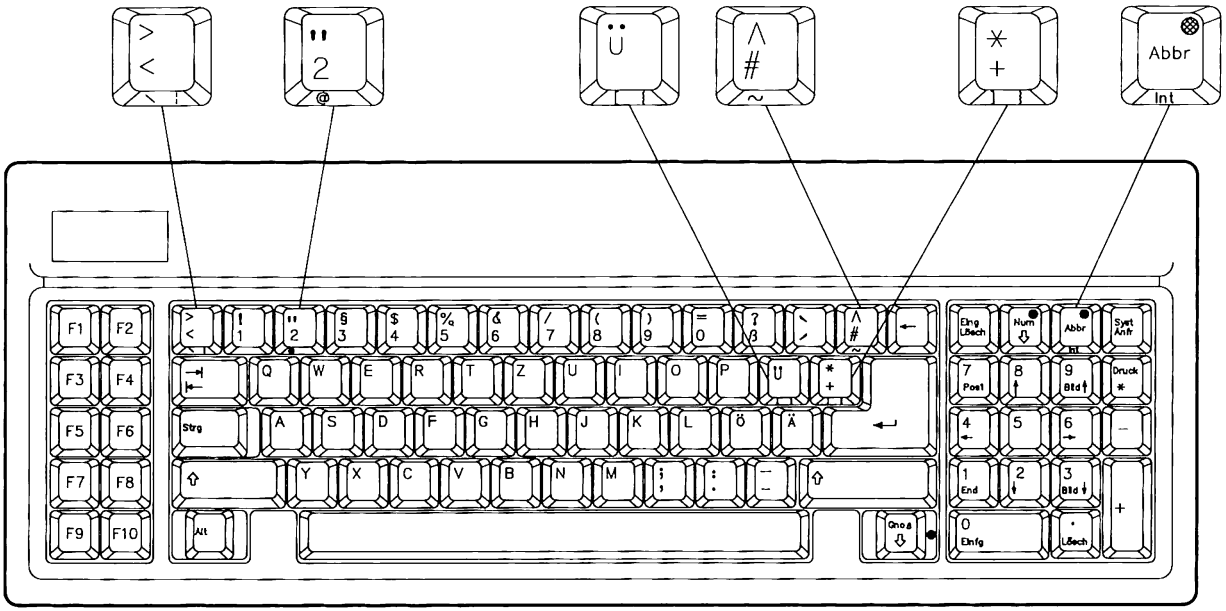


Figure 8-16. German 84-Key Keyboard

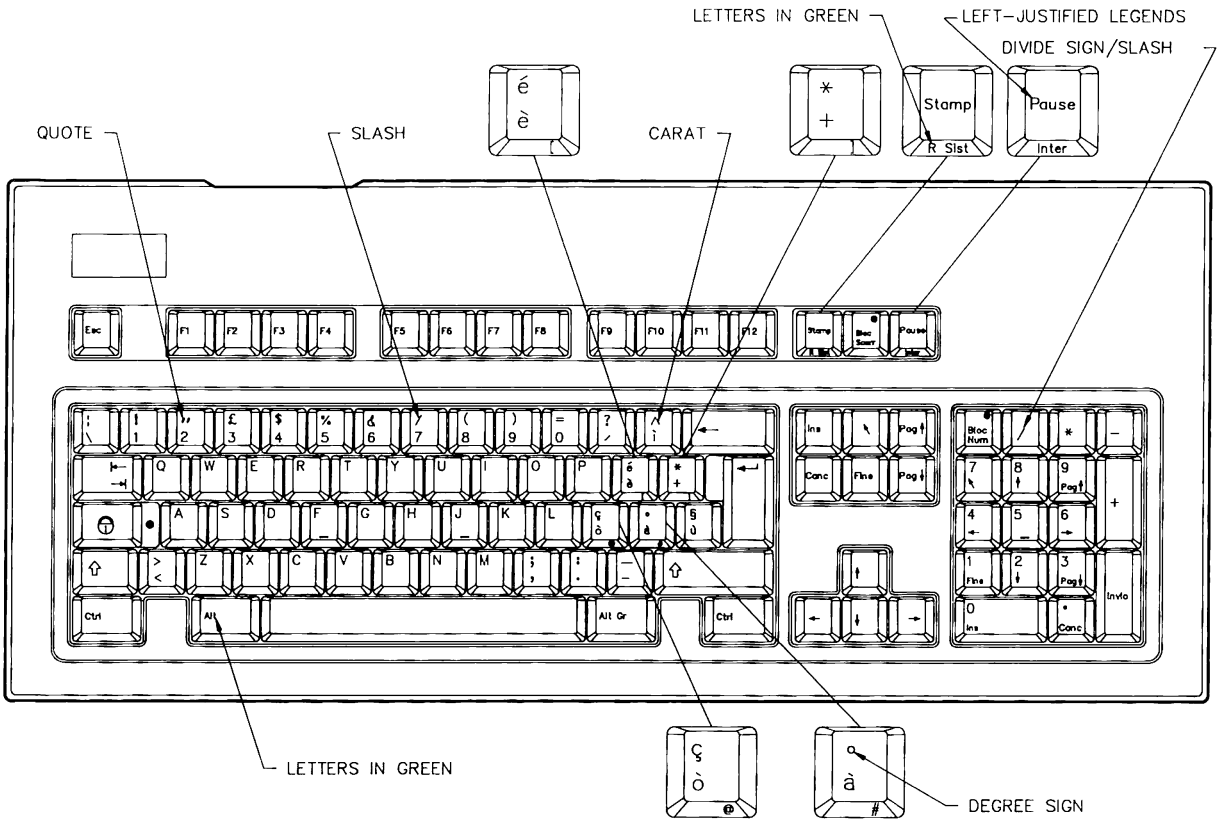


Figure 8-17. Italian Enhanced Keyboard

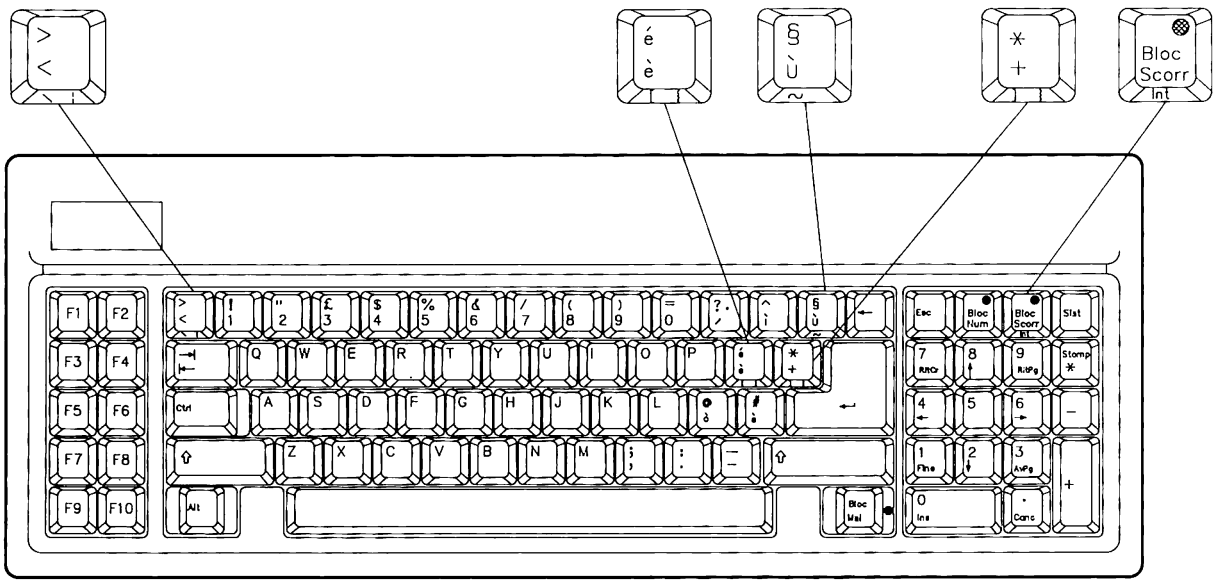


Figure 8-18. Italian 84-Key Keyboard

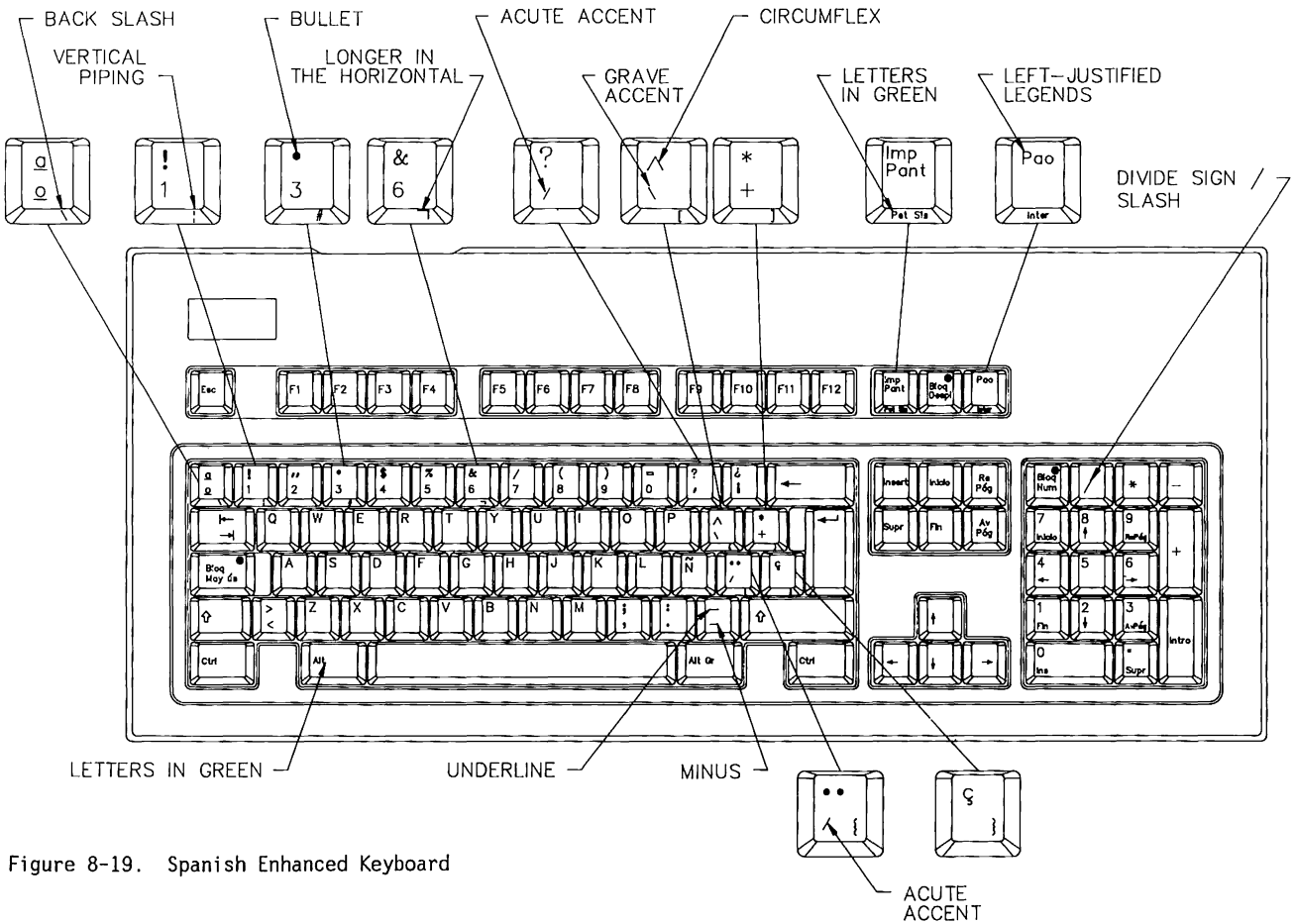


Figure 8-19. Spanish Enhanced Keyboard

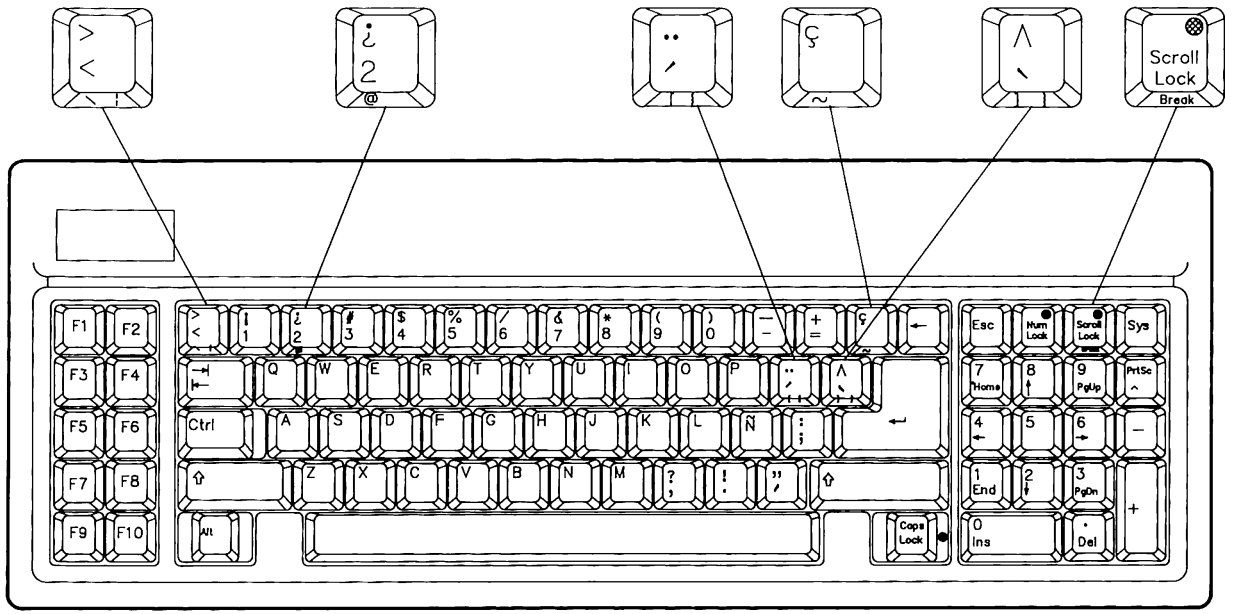


Figure 8-20. Spanish 84-Key Keyboard

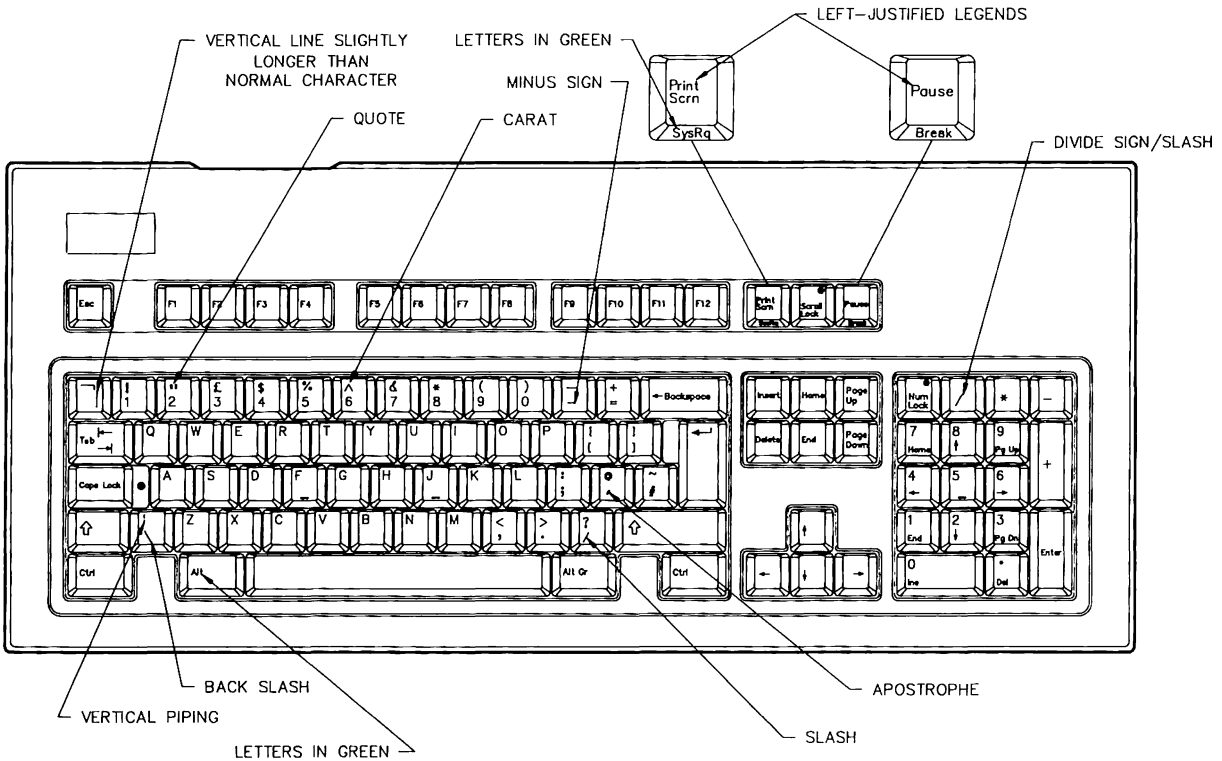


Figure 8-21. United Kingdom Enhanced Keyboard

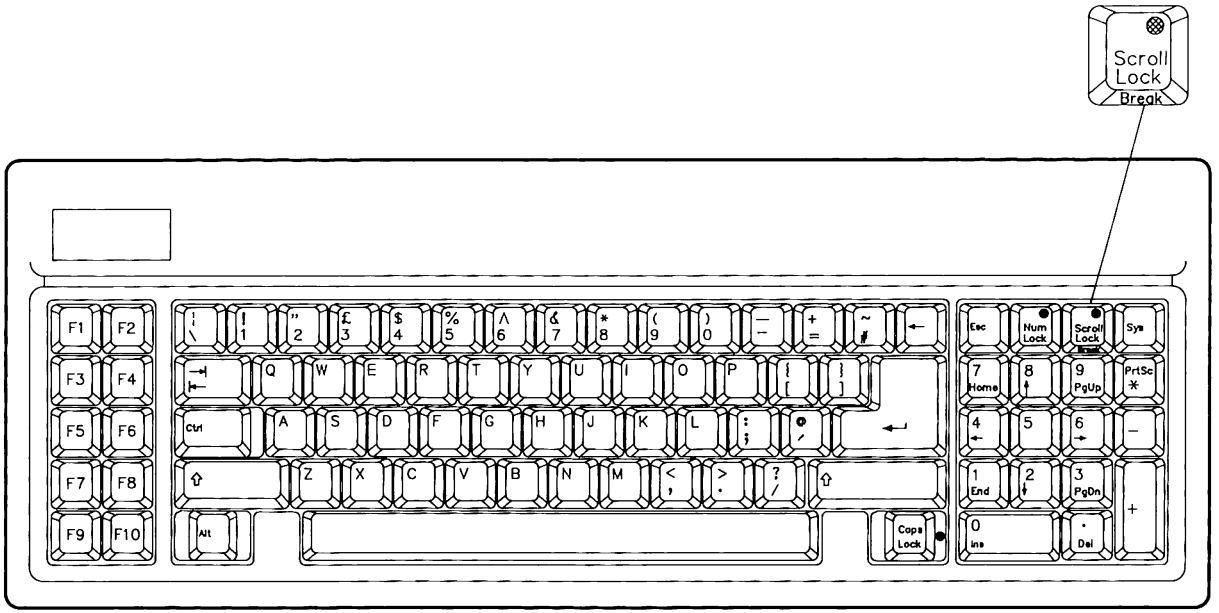


Figure 8-22. United Kingdom 84-Key Keyboard

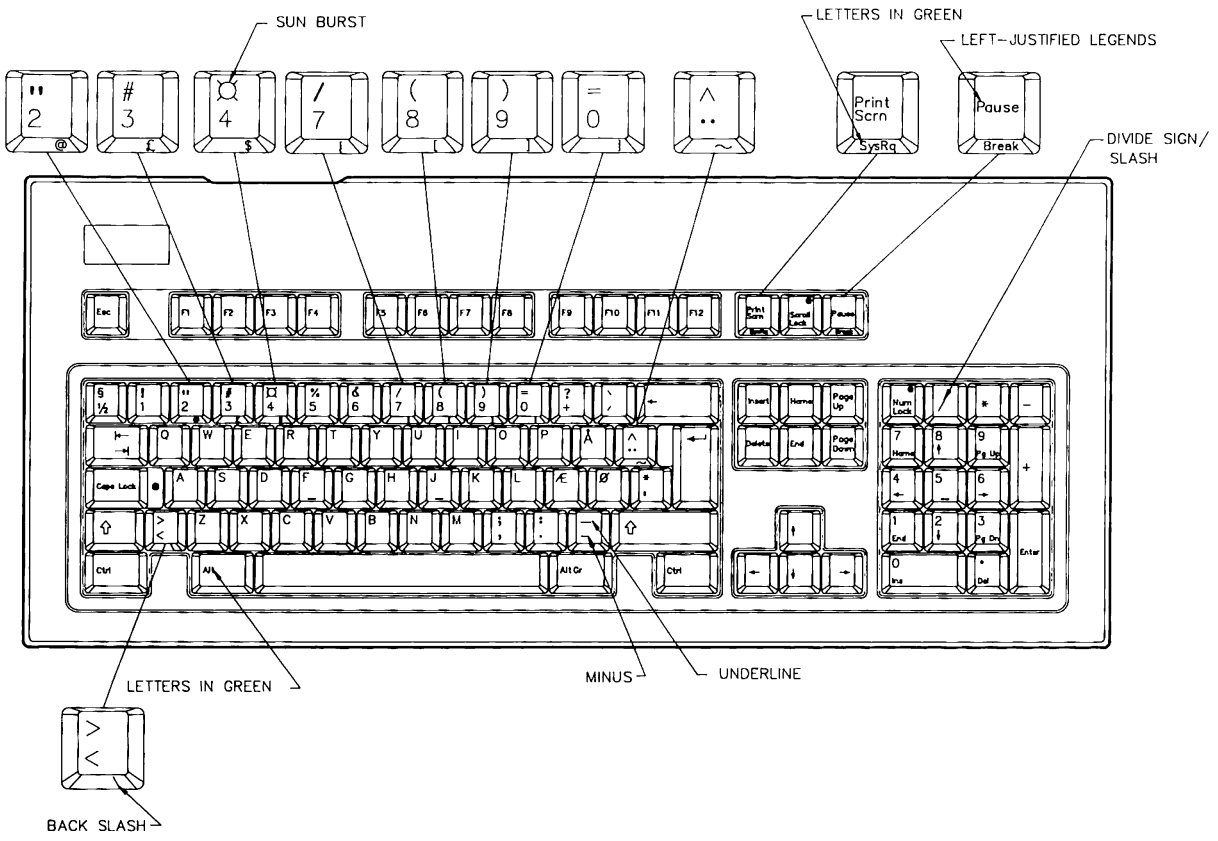


Figure 8-23. Danish Enhanced Keyboard

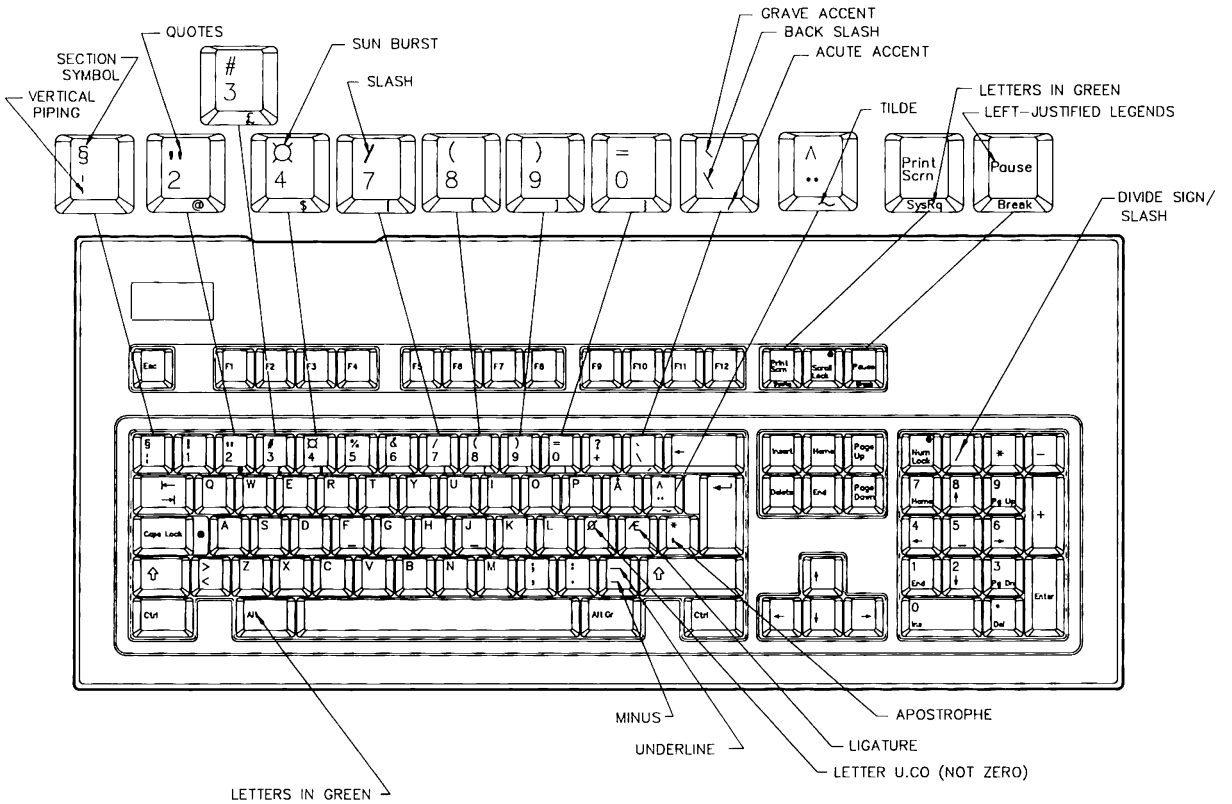


Figure 8-24. Norwegian Enhanced Keyboard

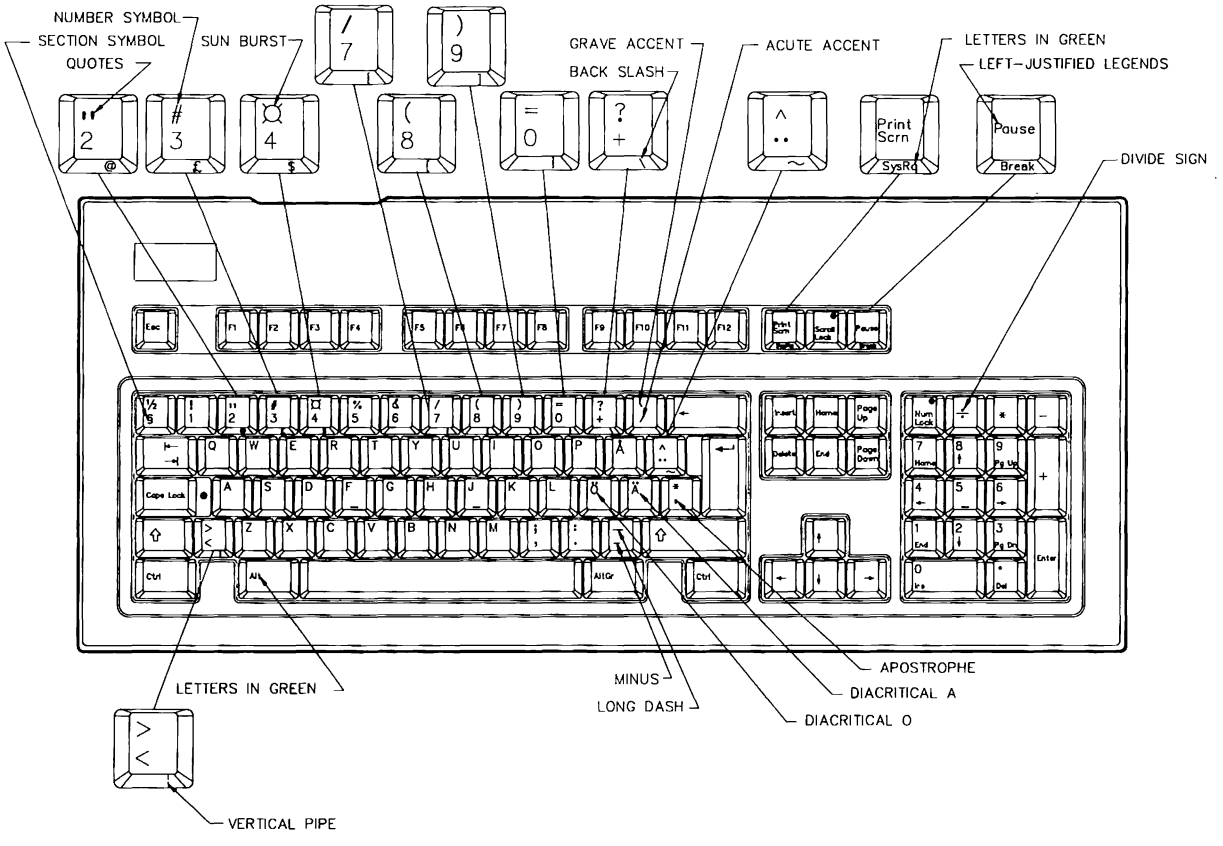


Figure 8-25. Swedish/Finnish Enhanced Keyboard

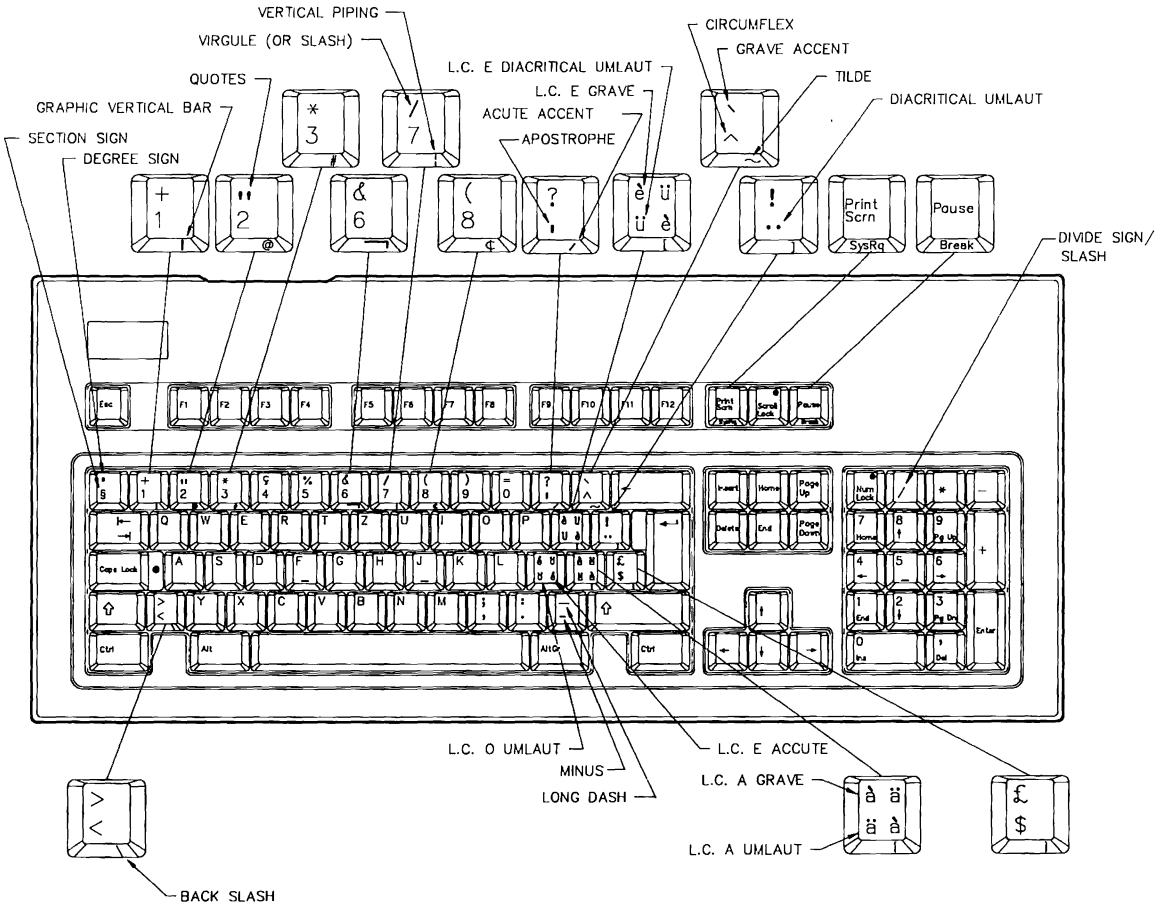


Figure 8-26. Swiss Enhanced Keyboard

Chapter 9

POWER SUPPLY

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9.1 INTRODUCTION

The COMPAQ PORTABLE 286® and COMPAQ DESKPRO 286® Personal Computers use a switching-type power supply to provide high-amperage, low-noise, DC power for the system.

Figure 9-1 shows the power supply for the COMPAQ PORTABLE 286. Figure 9-2 shows the power supply for the COMPAQ DESKPRO 286.

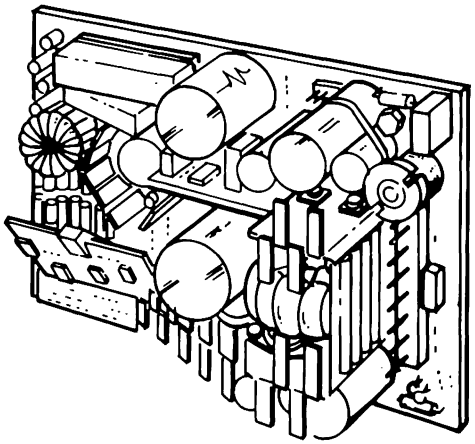


Figure 9-1. COMPAQ PORTABLE 286 Power Supply

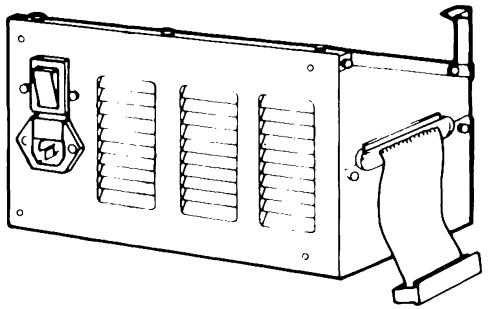
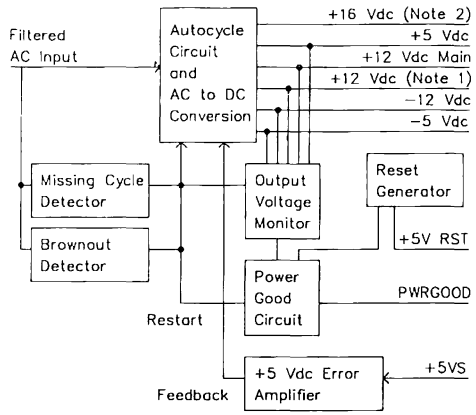


Figure 9-2. COMPAQ DESKPRO 286 Power Supply

9.2 FUNCTIONAL DESCRIPTION

The power supply provides four voltage levels for the system (+5 Vdc, -5 Vdc, +12 Vdc, and -12 Vdc). The +12 Vdc is provided as two separate outputs, main and auxiliary, to provide better power regulation. The COMPAQ PORTABLE 286 also provides +16 Vdc (unregulated) for the cooling fan.

Figure 9-3 shows the functional block diagram for both systems.



Notes: 1. This signal is +12 Vdc MON for the COMPAQ PORTABLE 286. It is 12 Vdc AUX for the COMPAQ DESKPRO 286.
2. COMPAQ PORTABLE 286 only.

Figure 9-3. Power Supply Functional Block Diagram

AC Input

The COMPAQ PORTABLE 286 and COMPAQ DESKPRO 286 have power supplies with jumper-selectable inputs to select 120 volt (North American) or 220-240 volt (international) AC power input. The COMPAQ DESKPRO 286 has different cooling fans and AC power fuses for the North American and international versions. The COMPAQ PORTABLE 286 only requires a different AC power fuse.

NOTE: Only Authorized COMPAQ Computer Service Representatives should change the AC input configuration. Changing the AC input configuration invalidates the COMPAQ warranty. The label near the AC power switch states the AC input power requirements for your system.

Power-On Sequence

The power-on sequence guarantees that all outputs are above the specified low voltage limits within 100 ms of power-on. The output load determines the order and the amount of time after the PWRGOOD signal is active (high) in which the outputs reach their regulated voltage level. Signal +5VRST is also set high at or prior to PWRGOOD becoming active (high).

Power-Down Sequence

The power-down sequence is dependent on the same variables as the power-on sequence. The output load determines both the order in which the output voltages drop out of regulation and the time remaining after the PWRGOOD signal becomes inactive (low). The PWRGOOD signal goes low within 8 ms after the power switch is turned off.

Autocycle Circuitry

The Autocycle Circuitry is the heart of the fault-detection functions for the power supplies. When a fault is detected, the power supply shuts down for approximately two seconds, then tries to restart. If the fault still exists, the power supply stays off for another two seconds, then tries to restart again.

The following paragraphs describe the additional protection of fault-detection circuits that trigger the autocycle circuitry.

The overvoltage protection circuit provides two types of protection. First, all outputs have a zener diode that will short to ground any supply voltage that exceeds specifications. Second, the +5 Vdc output has an overvoltage crowbar circuit that triggers the autocycle function when the output exceeds 6.2 Vdc for the COMPAQ PORTABLE 286 or 5.6 Vdc for the COMPAQ DESKPRO 286.

The low voltage protection circuit monitors the DC outputs. When one of the outputs drops below the specified limit, it triggers the autocycle circuit.

The AC input overcurrent protection circuit is a fuse on the outside of the unit. The fuse rating varies with the model (see Table 9-1).

NOTE: The power supply for the 12-MHz COMPAQ DESKPRO 286 does not contain a missing power detector circuit.

The missing cycle detector monitors the AC power input. If the AC power input is interrupted for more than one-half cycle, it pulls the PWRGOOD signal low, thereby triggering the autocycle circuit.

The brownout protection circuit and the autocycle circuit are triggered if the AC input voltage drops to 65-100 Vac (North American) or 130-200 Vac (international) under nominal to heavy loads.

CAUTION

Do not attempt to disassemble or repair the power supply. There are no user-serviceable components. Never operate the power supply without a load.

9.3 SPECIFICATIONS

Tables 9-1 through 9-3 provide the power supply specifications.

Table 9-1. Power Supply Specifications

	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286 (6 and 8 MHz)	COMPAQ DESKPRO 286 (12MHz Only)
Input AC voltage RMS:			
Domestic	102 to 132 VAC	102 to 132 VAC	102 to 132 VAC
International	204 to 264 VAC	204 to 264 VAC	204 to 264 VAC
Line frequency:	47 to 62 Hz	47 to 62 Hz	47 to 62 Hz
Input fuse rating:			
120 VAC RMS	3 A	4 A	5 A
220-240 VAC RMS	2.5 A	2.5 A	4 A
In-rush current (peak, over one line cycle interval):			
120 VAC	40 A	40 A	40 A
220-240 VAC	80 A	80 A	80 A
Environment:			
Temperature	41°F to 113°F (5°C to 45°C)	41°F to 113°F (5°C to 45°C)	41°F to 113°F (5°C to 45°C)
Altitude	0 to 10,000 ft (0 to 3 000 m)	0 to 10,000 ft (0 to 3 000 m)	0 to 10,000 ft (0 to 3 000 m)
Relative humidity	5% to 95%	5% to 95%	5% to 95%
Power dissipation (Note 1):			
Starting (Note 2)	200 W	200 W	220 W
Steady state	160 W	160 W	192 W

Notes: 1. These limits were established under the following conditions: 120 V, 60 Hz, 25°C, sea level, and 50% relative humidity.
2. Peak output power may be used on a 5-percent duty cycle, not to exceed 30-seconds continuous operation.

(Continued)

Table 9-1. (Continued)

	COMPAQ PORTABLE 286					COMPAQ DESKPRO 286				
	Current (A)					Current (A)				
Voltage:	Nominal	Min.	Max.	Abs. Max. (Note 3)	Regulation	Nominal	Min.	Max.	Abs. Max. (Note 3)	Regulation
+5 VDC	+5.0	1.5	15.0		(± 2%)	+5.0	1.5	15.0	(Note 4)	(± 2%)
+12 VDC	+12.25	1.0	5.0	7.0	(± 2%)	+12.25	1.0	5.0	7.0	(± 2%)
+12 VDC(Aux)	N/A					+12.25	0.0	5.0	7.0	(± 2%)
+12 VDC(MON)	+12.25	0.0	1.5	3.0	(± 2%)	N/A				
-5 VDC	-5.0	0.0	0.5		(± 5%)	-5.0	0.0	0.5		(± 5%)
-12 VDC	-12.0	0.0	1.0		(± 5%)	-12.0	0.0	0.5		(± 5%)
Over-Voltage Limits:										
+5 VDC	6.2 VDC					5.6 VDC				
+12 VDC	13.0 VDC					13.0 VDC				
-5 VDC	-5.6 VDC					-5.6 VDC				
-12 VDC	-13.0 VDC					-13.0 VDC				
Maximum Ripple/Output	50 mV RMS					50 mV RMS				

Notes: 3. Abs. Max = Absolute maximum current. The peak output power may be used on a 5-percent duty cycle, not to exceed 30-seconds continuous operation.

4. The maximum +5-VDC current is 20 amperes for the 12-MHz COMPAQ DESKPRO 286 Personal Computer.

Table 9-2. COMPAQ PORTABLE 286 Expansion Bus Slot Power Allocation

	Per Slot				Total (All Slots)			
	+5 Vdc	+12 Vdc	-12 Vdc	-5 Vdc	+5 Vdc	+12 Vdc	-12 Vdc	-5 Vdc
Configuration 1	3 A	1 A	0.3 A	0.2 A	7 A	2 A	0.3 A	0.2 A
Configuration 2	3 A	1 A	0.3 A	0.2 A	6 A	1 A	0.3 A	0.2 A
Configuration 3	3 A	1 A	0.3 A	0.2 A	6 A	1 A	0.3 A	0.2 A

Notes: 1. The amperage values given are the absolute maximum values.
2. Configuration 1 = unit with 1.2-megabyte diskette drive and 256 Kbytes RAM
Configuration 2 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, and 20-megabyte fixed disk drive
Configuration 3 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, 20-megabyte fixed disk drive, and fixed disk drive backup.

Table 9-3. 8-MHz COMPAQ DESKPRO 286 Expansion Bus Slot Power Allocation

	Per Slot				Total (All Slots)			
	+5 Vdc	+12 Vdc	-12 Vdc	-5 Vdc	+5 Vdc	+12 Vdc(main)	-12 Vdc	-5 Vdc
Configuration 1	3 A	1 A	0.3 A	0.2 A	8 A	2 A	0.3 A	0.2 A
Configuration 2	3 A	1 A	0.3 A	0.2 A	7 A	2 A	0.3 A	0.2 A
Configuration 3	3 A	1 A	0.3 A	0.2 A	7 A	1 A	0.3 A	0.2 A

Notes: 1. The amperage values given are the absolute maximum values.
2. Configuration 1 = unit with 1.2-megabyte diskette drive and 256 Kbytes RAM
Configuration 2 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, and 20-megabyte fixed disk drive
Configuration 3 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, 40-megabyte fixed disk drive, and fixed disk drive backup.
3. All Configurations are assumed to be using the COMPAQ keyboard and COMPAQ Dual-Mode Monitor.
4. +12 Vdc (Aux) is available only on system board connectors J109 and J110, supplies a maximum of 4 A, and is reserved for fixed disk drives or a fixed disk drive backup only.

Table 9-4. 12-MHz COMPAQ DESKPRO 286 Expansion Bus Slot Power Allocation

	Per Slot				Total (All Slots)			
	+5 Vdc	+12 Vdc	-12 Vdc	-5 Vdc	+5 Vdc	+12 Vdc(main)	-12 Vdc	-5 Vdc
Configuration 1	3 A	1 A	0.3 A	0.2 A	8 A	2 A	0.3 A	0.2 A
Configuration 2	3 A	1 A	0.3 A	0.2 A	7 A	2 A	0.3 A	0.2 A
Configuration 3	3 A	1 A	0.3 A	0.2 A	7 A	1 A	0.3 A	0.2 A

Notes: 1. The amperage values given are the absolute maximum values.

2. Configuration 1 = unit with 1.2-megabyte diskette drive and 256 Kbytes RAM
   Configuration 2 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, and 20-megabyte fixed disk drive
   Configuration 3 = unit with 1.2-megabyte diskette drive, 640 Kbytes RAM, 40-megabyte fixed disk drive, and fixed disk drive backup.

3. All Configurations are assumed to be using the COMPAQ keyboard and COMPAQ Dual-Mode Monitor.

4. +12 Vdc (Aux) is available only on system board connectors J109 and J110, supplies a maximum of 4 A, and is reserved for fixed disk drives or a fixed disk drive backup only.

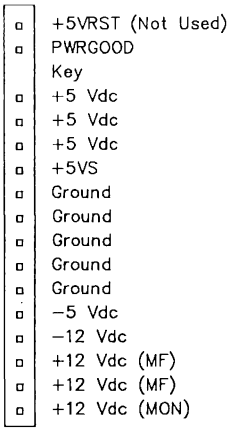
9.4 CONNECTORS

Table 9-5 describes the power supply signals. Figures 9-4 and 9-5 show the voltages or signals provided by the power supply to the system board.

Table 9-5. Power Supply Connector to the System Boards

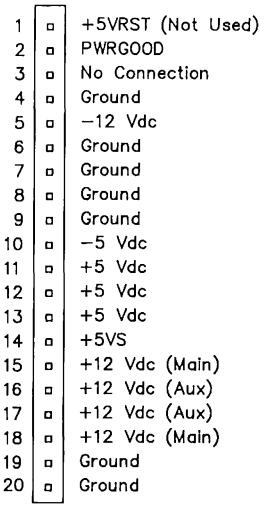
Signal	COMPAQ PORTABLE 286 Pin	COMPAQ DESKPRO 286 Pin	I/O	Description
+5VRST (Note 1)	1	1	O	The +5VRST signal is regulated from the +15 Vdc line. This signal ranges from +4.8 Vdc to +5.2 Vdc
PWRGOOD	2	2	O	The PWRGOOD signal is controlled by the low voltage monitor and the missing cycle detector circuits. When all outputs are above the minimum values (see specifications), and there is no fault, the PWRGOOD signal is TTL high (+3.5 to +5.25 Vdc). If a low voltage condition is detected, the PWRGOOD signal is pulled low (less than 0.4 Vdc)
+5 Vdc	4,5,6	11,12,13	O	+5.0 Vdc
+5VS	7	14	I	The +5VS signal provides feedback from the system board. The power supply shuts down if the +5VS signal is interrupted or disconnected
Ground	8,9,10,11,12	6,7,8,9,19,20		Signal Ground
-5 Vdc	13	10	O	-5 Vdc
-12 Vdc	14	5	O	-12 Vdc
+12MF	15,16	N/A	O	+12 Vdc for everything except monitor
+12MON	17	N/A	O	+12 Vdc for internal monitor
+12VMAIN	N/A	15,18	O	+12 Vdc for J111 and J112 (Diskette drives A and B), J113 (COMPAQ Dual-Mode Monitor power), and expansion bus slots
+12VAUX	N/A	16,17	O	+12 Vdc for J109 and J110 (Fixed Disk Drive C and Fixed Disk Drive Backup)
No Connection	-	3,4	-	-

Note: There is no connection to this pin on the COMPAQ DESKPRO 286 with the 12-MHz system board.



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 9-4. COMPAQ PORTABLE 286 Power Supply Cable Signals



Note: The maximum current for a single conductor (pin) must not exceed 5.0 A per line for +5 Vdc or 4.0 A for other lines.

Figure 9-5. COMPAQ DESKPRO 286 Power Supply Cable Signals

Chapter 10

DISKETTE DRIVES

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10.1 INTRODUCTION

The COMPAQ PORTABLE 286® and the COMPAQ DESKPRO 286® Personal Computer use 5.25-inch diskette drives, capable of storing either 1.2 megabytes or 360 kilobytes (Kbytes) of data.

The 12-MHz DESKPRO 286 also supports the 3.5-inch 1.44-Mbyte Diskette Drive; this device requires MS-DOS Version 3.3, as published by Compaq Computer Corporation, as an operating system.

A diskette drive has a diskette drive logic board that controls the diskette drive motor speed, read and write circuits, and other electronic circuits. The diskette drive logic board is mounted on the diskette drive. It connects to the:

- Ceramic heads, which read and write data to the diskettes
- Index sensor
- Door-closed sensor
- Write-protect sensor
- Stepper motor, which steps the heads back and forth
- Track-zero sensor
- Diskette controller (multipurpose controller board or multipurpose fixed disk controller board [12-MHz COMPAQ DESKPRO 286 only])

Various diskette drive logic boards use different connectors and pin arrangements foer the internal drive functions. The connections to the multipurpose controller board or multipurpose fixed disk drive controller board and the DC power source remain the same.

A diskette drive has a main chassis, on which are mounted the diskette drive motor, stepper motor, head-carriage assembly, spindle, and diskette drive logic board. The left and right diskette guides, the front bezel, and the front-door mechanism are also mounted on the chassis.

Figure 10-1 shows a typical diskette drive chassis.

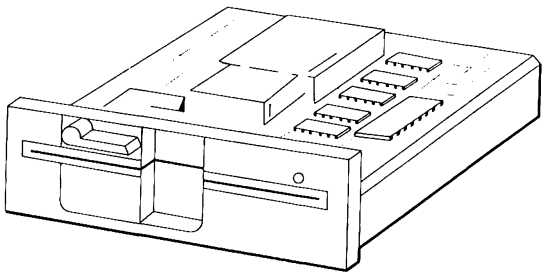


Figure 10-1. Typical Diskette Drive Chassis

Figure 10-2 is a functional block diagram for a diskette drive.

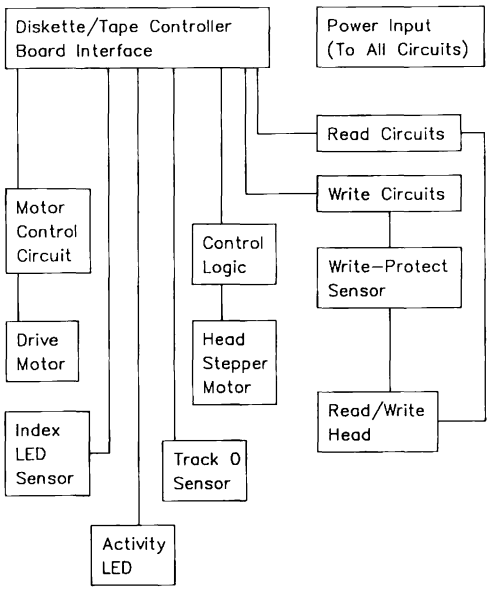


Figure 10-2. Diskette Drive Functional Block Diagram

10.2 FUNCTIONAL DESCRIPTION

The DESKPRO 286 allows the use of multiple diskette drives, which are connected in a daisy-chained manner (one after another on the same cable) from a single controller. The drives have four jumpers, only one of which is installed, corresponding to the individual drive select signals in the cable.

The 1.44-MB, the 1.2-MB, and the 360-KB capacity diskette drives are configured identically; that is, they are jumpered for the second physical diskette drive position and respond to the DRIVE 2 SELECT- signal. The drive is put in this configuration by installing jumper DS1 and removing jumpers DS0, DS2, and DS3.

However, it is the drive placement on the cable that determines which one becomes drive A. The controller cable has two diskette drive connectors, one for drive A, the other for drive B. A third connector is for the fixed disk drive backup (tape) device. Any diskette drive configured as described above and plugged into the drive A connector becomes drive A; likewise, a drive plugged into the drive B connector becomes drive B. The drive A connector is positioned between a pair of cable conductor twists. This pair of cable twists allows two drives that are configured identically to be accessed independently. The drive B connector and 40 megabyte tape backup connector is on the untwisted portion of the cable.

The 1.44-MB drive is only supported as drive B.

The cable termination resistor pack should be installed in drive A, regardless of drive capacity. There should be no termination on drive B for 1.2-MB and 360-KB diskette drives.

1.2-MB Diskette Drive

The 1.2-MB diskette drive is a high-capacity diskette drive with the following features:

- Half-height, 5.25-inch diskette drive
- Two transfer rates--300 kb/s (low density) or 500 kb/s (high density)
- Data storage on 80 tracks (96 TPI)

To read or write to 48-TPI media, the software must step the 96-TPI drive head twice between each 48-TPI track. Because the track width of the 96-TPI diskette drive is approximately half the track width of the 48-TPI diskette drive, standard 48-TPI diskette drives may not be able to read diskettes written by the 96-TPI drive in the 48-TPI format.

360-KB Diskette Drive (Optional)

The 360-KB diskette drive has the following features:

- Half-height, 5.25-inch diskette drive
- Double-sided, double-density (DSDD) 40 tracks (48 TPI)
- Single transfer rate of 250 kb/s

1.44-MB Diskette Drive (Optional)

The 1.44-MB diskette drive is a high-capacity diskette drive with the following features:

- Half-height, 3.5-inch diskette drive
- Two transfer rates--250 kb/s (low density) or 500 kb/s (high density)
- Data storage on 80 tracks (135 TPI)
- Write and read compatible with low density (720 KB) 3.5-inch media.

The 3.5-inch drive is configured in a 5.25-inch, half-height adapter frame for ease of mounting in the system.

10.3 SPECIFICATIONS

Table 10-1 lists the physical and electrical specifications for the 1.2-MB, 360-KB, and the 1.44-MB diskette drives.

Table 10-1. 1.2-MB, 360-KB, and 1.44-MB Diskette Drive Physical and Electrical Specifications

	1.2-MB Diskette Drive	360-KB Diskette Drive	1.44-MB Diskette Drive (Excluding 5.25 Adapters)
Drive Type	2	1	4
Size:			
Width	5.8 in. (146 mm)	5.8 in. (146 mm)	4.0 in. (102 mm)
Height	1.6 in. (41 mm)	1.6 in. (41 mm)	1.0 in. (25 mm)
Depth	8.0 in. (203 mm)	8.0 in. (203 mm)	6.056 in. (154 mm)
Capacity:			
Unformatted	1,600,000 bytes	500,000 bytes	2,000,000 bytes
Formatted	1,228,800 bytes	368,640 bytes	1,474,560 bytes
Flux reversal density	9875 FRPI (Track 79)	5876 FRPI (Track 39)	17,434 FRPI (Track 79)
Data-transfer rate high/low density	500/300 kb/s	250 kb/s	500/250 kb/s
Sectors/track high/low density	15/9	9	18/9
Bytes/sector	512	512	512
Seek time:			
Track-to-track	3 ms	6 ms	3 ms
Average	79 ms	80 ms	80 ms
Settling time	15 ms	15 ms	15 ms
Rotational Speed	360 RPM ±1.0%	300 RPM ±1.5%	300 RPM ±1.0%
Motor Start Time	500 ms	500 ms	700 ms

10.4 CONNECTORS

A diskette drive has two connectors: control and power. Table 10-2 lists the diskette drive control signals.

Table 10-2. Diskette Drive Control Signals

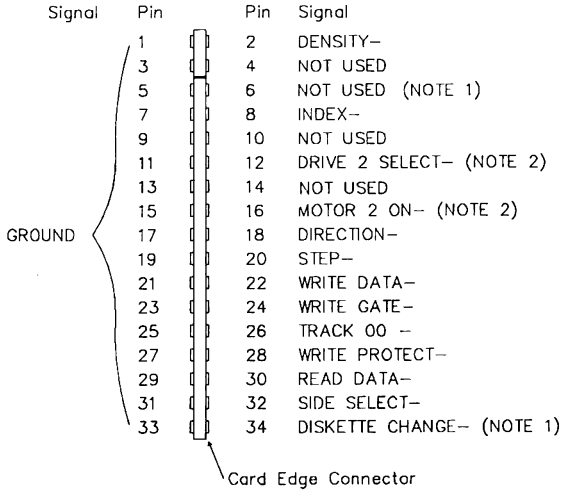
Signal	Pin	I/O	Description
LOW DENSITY-	2	I	When using high-capacity drives, this signal selects High or Low mode (See Note)
DIRECTION-	18	I	Selects the direction in which to move the head when a step pulse is issued
DISKETTE CHANGE-	34	O	Indicates to diskette drive controller that the drive door has been opened (and possibly different media installed) (See Note)
DRIVE 2 SELECT-	12	I	Allows the selection of a diskette drive so that it can respond to the interface signals
Notes: 1. The LOW DENSITY- and DISKETTE CHANGE- signals are not used on a 360-KB (48-TPI) diskette drive. 2. All odd pin numbers are ground.			

(Continued)

Table 10-2. (Continued)

Signal	Pin	I/O	Description
INDEX-	8	O	Indicates to the diskette drive controller that the media index hole is under the index sensor
MOTOR 2 ON-	16	I	Activates the drive motor
READ DATA-	30	O	The data-stream read from the diskette containing CLOCK and DATA signals
SIDE SELECT-	32	I	Selects side 0 (Head 0) or side 1 (Head 1)
STEP-	20	I	Tells the diskette drive to step the heads one track
TRACK 00-	26	O	Indicates to the diskette drive controller that the heads are at Track 0
WRITE DATA-	22	I	This stream of data is written to the diskette when WRITE GATE- is enabled
WRITE GATE-	24	I	Enables the diskette drive write circuits so data from the WRITE DATA- signal are written
WRITE PROTECT-	28	O	Indicates to the diskette drive controller that the media is write protected
Notes: 1. The LOW DENSITY- and DISKETTE CHANGE- signals are not used on a 360-KB (48-TPI) diskette drive. 2. All odd pin numbers are ground.			

Figures 10-3 and 10-4, respectively, show the pinouts of the diskette drive control and power connectors.



Notes: 1. Not applicable on 360-KB diskette drives.
2. DRIVE 2 SELECT- and MOTOR 2 ON- are the signals supplied by the multipurpose fixed disk drive controller (MFDDC) board for Diskette Drive 1 (A), the signals from the MFDDC are DRIVE 1 SELECT- and MOTOR 1 ON-.

Figure 10-3. Diskette Drive Control Connector

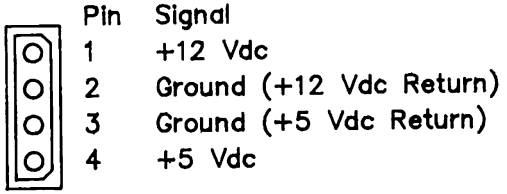


Figure 10-4. Diskette Drive Power Connector

Chapter 11

FIXED DISK DRIVES

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11.1 INTRODUCTION

COMPAQ® 80286-based computer products use fixed disk drives that are compatible with either the ST506 or ESDI standard interface or the COMPAQ 16-bit custom interface. These interfaces specify connector pinouts, signal definitions, and signal types for fixed disk drives.

Fixed disk drives available for these systems include 20- and 40-megabyte versions with the COMPAQ 16-Bit custom interface and 20-, 30-, and 70-megabyte versions with the ST506 standard interface. The 130-megabyte fixed disk drive comes with its own ESDI controller board. This drive is supported only on the 12-MHz DESKPRO 286 among the 80286-based products.

Fixed disk drives:

- Are sealed units. The media (disk surfaces) are not removable.
- Rotate the media at 3600 RPM
- Have a much higher data-transfer rate and faster access time than diskette drives.

All fixed disk drives have the same general components:

- A sealed head-disk assembly containing the disk platters, heads, and drive motor
- A drive-logic circuit board that controls the fixed disk drive's motors and the read and write electronics

Some fixed disk drives have the controller electronics integrated with the drive electronics (COMPAQ 16-bit interface). These drives require only a host adapter to the system bus as opposed to the separate controller required by the ST506 or ESDI interfaces.

Figure 11-1 shows the functional block diagram for a fixed disk drive.

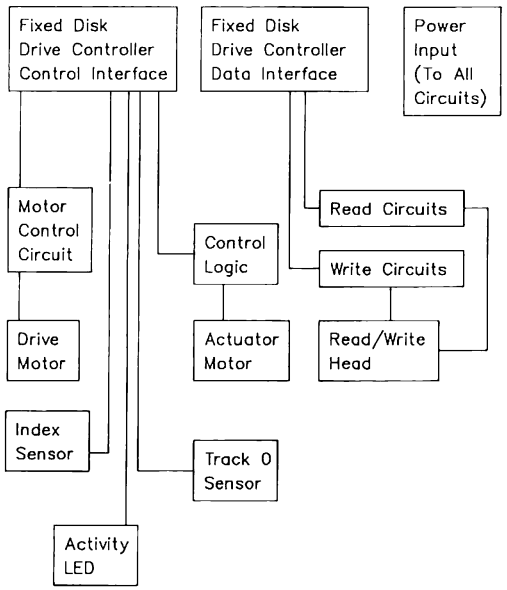


Figure 11-1. Fixed Disk Drive Functional Block Diagram

11.2 CONFIGURATION

A fixed disk drive controller is I/O mapped into specific I/O addresses. Generally, a jumper on the fixed disk drive controller specifies the base I/O address for that controller.

The fixed disk drive controller responds to commands given to it, and takes control of the system as needed to transfer information.

Two fixed disk drive controllers cannot occupy the same I/O address without causing bus contention and possibly damaging the system.

The COMPAQ 80286-based computer products may have 10 different fixed disk drive configurations. The nine possible configurations are:

- One or two 5.25" 40-megabyte, COMPAQ Interface
- One or two 3.50" 40-megabyte, COMPAQ Interface
- One or two 3.50" 20-megabyte, COMPAQ Interface
- One 5.25" 70-megabyte, ST506 Interface
- One 5.25" 30-megabyte, ST506 Interface
- One 5.25" 20-megabyte, ST506 Interface
- One 5.25" 130-megabyte, ESDI

Addendum 114271-001 (12-88)
To Manual No. 102789-001

ST506 fixed disk drives should have their drive select jumpers set to DS1. The COMPAQ Dual Fixed Disk Drive Control Cable automatically selects the second fixed disk drive. Refer to Chapter 5 in this guide for information on setting the correct jumper settings required for a particular fixed disk drive configuration.

ST506 fixed disk drives require that a terminating resistor pack be installed only on the last fixed disk drive on the control cable. Fixed disk drives with the COMPAQ 16-Bit interface do not require a terminating resistor pack at the drive.

COMPAQ 16-bit fixed disk drives are configured for single or dual-mode according to the jumper settings in Table 11-1.

Table 11-1. Fixed Disk Drive Jumper Settings

Jumper		Function
Drive 1	Drive 2	
E7,E5	N/A	One 3.5-inch 20- or 40-megabyte drive
E7,E6	E6	Two 3.5-inch 20- or 40-megabyte drives
J3 IN:C installed	N/A	One 5.25-inch 40-megabyte drive
J3 IN:C installed	J1 IN:C removed	Two 5.25-inch 40-megabyte drives

Addendum 114271-001 (12-88)
To Manual No. 102789-001

11.3 SPECIFICATIONS

Table 11-2. Fixed Disk Drive Physical and Electrical Specifications

	3.5-inch Drives		5.25-inch Drives				
	20MB	40MB	20MB	30MB	70MB	40MB	130MB
Capacity (megabyte):							
Unformatted	26.69	53.66	25.62	36.32	86.78	51.08	161.8
Formatted	21.41	42.65	21.41	30.33	72.46	42.65	134.5
Drive type*	2	17/43**	2	6	12	17	25/35
Data transfer rate (mb/s)	8.0	8.0	5.0	5.0	5.0	5.0	10.0
Rotational speed (RPM)	3600	3600	3600	3600	3600	3600	3600
Number of heads (logical)	4	5/4	4	5	9	5	16
Number of heads (physical)	2	4	4	5	9	5	8
Average Access Time (ms)	29	29	105	40	29	29	20
Number of cylinders (logical)	615	980/805	615	697	925	980	966
Physical sectors/track	26	26	17	17	17	17	34 + 1 (spare)
Logical sectors/track	17	17/26	17	17	17	17	17/34
Write precompensation cylinder	128	128	128	128	128	128	Not Used
Landing zone cylinder	638	980/805	638	696	924	980	966
Size:							
Width (in. (mm))	4.1 (104)	4.1 (104)	5.8 (146)	5.8 (146)	5.8 (146)	5.8 (146)	5.75 (146)
Height (in. (mm))	1.7 (43)	1.7 (43)	1.7 (43)	3.4 (43)	3.4 (86)	1.7 (43)	3.25 (83)
Depth (in. (mm))	5.8 (146)	5.8 (146)	8.0 (203)	8.0 (203)	8.0 (203)	8.8 (223)	8.0 (203)
Weight (lb (kg))	1.8 (0.8)	1.8 (0.8)	3.5 (1.6)	7.5 (3.4)	8.0 (3.6)	4.2 (1.9)	8.0 (3.6)
Number of ECC bytes	4	4	4	4	4	4	7
Interface	COMPAQ 16	COMPAQ 16	ST506	ST506	ST506	COMPAQ 16	ESDI

* Used in SETUP program.
** Requires system ROM revision F.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

11.4 ST506 INTERFACE CONNECTORS

The fixed disk drive controller board with ST506 standard interface connects to the fixed disk drive via two cables: the control cable and the data cable. The control cable connects in a daisy-chain manner to all the fixed disk drives in the system. A separate data cable connects the fixed disk drive controller to each fixed disk drive.

Tables 11-3 and 11-4 list the fixed disk drive connector signals. Figures 11-2 through 11-4 show the connectors.

See Section 11.6 for information on the 130-MB Fixed Disk Drive and its ESDI controller board.

Table 11-3. Fixed Disk Drive Control Cable Signals

Signal	Pin	I/O	Description
DIRECTION IN-	34	I	Defines the direction of motion of the heads when the fixed disk drive is executing a seek.
DRIVE SELECT 1-	26	I	Indicates that Fixed Disk Drive 1 is to respond to the control signals on the fixed disk drive control bus.
DRIVE SELECT 2-	28	I	Indicates that Fixed Disk Drive 2 is to respond to the control signals on the fixed disk drive control bus.
GROUND	All Odd No. Pins		Signal ground
HEAD SELECT 2^0-	14	I	First and least-significant bit of the binary-coded head-select address.
HEAD SELECT 2^1-	18	I	Second bit of the binary-coded head-select address.
HEAD SELECT 2^2-	4	I	Third bit of the binary-coded head-select address.
INDEX-	20	O	Indicates the beginning of a track.

(Continued)

Table 11-3. (Continued)

Signal	Pin	I/O	Description
REDUCED WRITE CURRENT-/ HEAD SELECT 2^3-	2	I	Functions as the reduced write current signal or a head-select 2^3 bit. The control bit for this selection is in the fixed disk drive control register. In the reduced write current mode, this line, in conjunction with the WRITE GATE- signal, reduces the magnitude of the write current for writing on inner-disk cylinders. In the head-select mode, this pin is the fourth and most-significant bit of the head-select binary code.
READY-	22	O	When active with SEEK COMPLETE-, READY- indicates that the fixed disk drive is ready to perform a read, write, or seek command.

(Continued)

Table 11-3. (Continued)

Signal Name	Pin	I/O	Signal Description
Reserved	16,30, 32	-- --	
SEEK COMPLETE-	8	O	Indicates that the heads have settled on the specified track at the end of a track seek operation.
STEP-	24	I	This signal causes the heads to move one track in the direction defined by the DIRECTION IN- signal.
TRACK 000-	10	O	Indicates that the heads are on track zero (000).
WRITE FAULT-	12	O	Indicates that a condition exists that may cause improper writing on the fixed disk and that writing is, therefore, inhibited.
WRITE GATE-	6	I	When active, allows data on the data cable +MFM WRITE DATA signal to be written on the fixed disk.

Note: All odd-numbered pins are Signal Ground.

Table 11-4. Fixed Disk Drive Data Cable Signals

Signal Name	Pin	I/O	Signal Description
DRIVE SELECTED-	1	O	When active, the fixed drive is selected and is responding to the control bus.
GROUND	2,4, 6,8, 11,12, 15,16, 19,20,	--	Signal Ground
+MFM WRITE DATA	13	I	MFM-encoded write data to be written to the fixed disk.
-MFM WRITE DATA	14	I	MFM-encoded write data to be written to the fixed disk.
+MFM READ DATA	17	O	MFM-encoded read data from the fixed disk.
-MFM READ DATA	18	O	MFM-encoded read data from the fixed disk.
Reserved	3,5,7	--	
Spare	9,10	--	

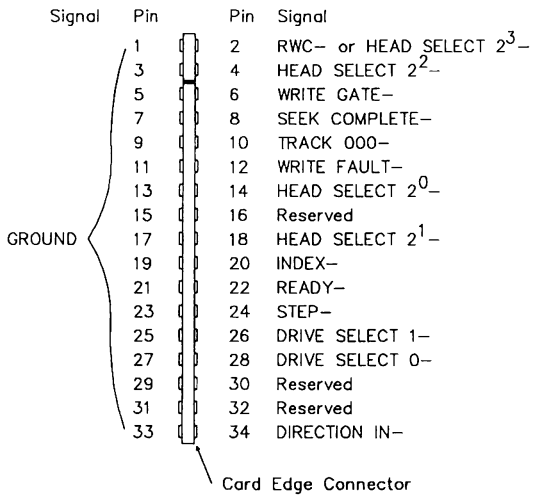


Figure 11-2. Fixed Disk Drive Control Cable Connector (ST506)

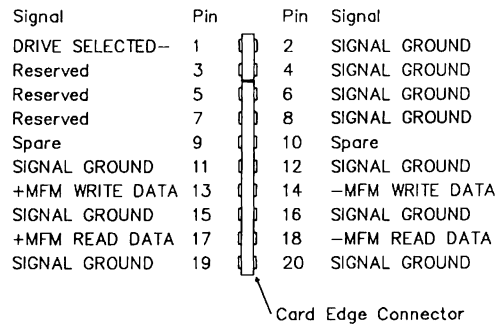


Figure 11-3. Fixed Disk Drive Data Cable Connector (ST506)

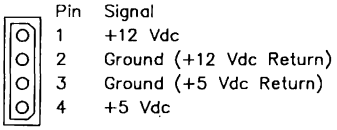


Figure 11-4. Fixed Disk Drive Power Cable Connector

11.5 COMPAQ 16-BIT INTERFACE CONNECTORS

The fixed disk drives with the COMPAQ 16-bit interface connector use a single 40-pin connector, which is defined in Table 11-5. The interface cable is capable of being connected in a daisy-chain configuration to control up to two fixed disk drives. See Section 11.6 for information on the 130-MB Fixed Disk Drive.

Table 11-5. COMPAQ 16-Bit Interface Connector

Pin Name	Pin Number	I/O	Signal Name	Signal Description
HRST-	1	I	Host reset	Reset signal from the host system that is active during power-on and inactive thereafter.
HD0	17	I/O	Host data bus	16-bit bidirectional data bus between the host and the fixed disk drives used for register and ECC byte access. All bits are used for data word transfers.
HD1	15			
HD2	13			
HD3	11			
HD4	9			
HD5	7			
HD6	5			
HD7	3			
HD8	4			
HD9	6			
HD10	8			
HD11	10			
HD12	12			
HD13	14			
HD14	16			
HD15	18			
HIOW-	23	I	Host I/O write	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data port of the drive.

(Continued)

Table 11-5. (Continued)

Pin Name	Pin Number	I/O	Signal Name	Signal Description
HIOR-	25	I	Host I/O read	Read strobe, the falling edge of which enables data from a register or the data port of the drive onto the host data bus, HD0 through HD15. The rising edge of HIOR- latches data at the host.
HALE	28	I	Host address latch enable	Address valid indication from the host system. The host address and chip selects, HA0 through HA2, HCS0-, and HCS1-, are guaranteed valid on the falling edge of this signal. The address and chip select signals are held valid after the HALE falling edge by the host system; therefore, the drive need not latch these signals with HALE.
HIRQ	31	0	Host interrupt request	Interrupt to the host system, activated only when the drive CPU has a pending interrupt, the drive is selected, and the host activates the IEN- bit in the digital output register. When the IEN- bit is inactive, or the drive is not selected, this output is in a high-impedance state, regardless of the presence or absence of a pending interrupt.
HI016	32	0	Host 16-bit I/O	Indication to the host system that the 16-bit data port has been addressed and that the drive is prepared to send or receive a 16-bit data word. This must be an open-collector output.
HA0	35	I	Host address bus	3-bit binary-coded address supplied by the host when accessing a register or the data base port in the drive.
PDIAG-	34	I/O	Passed diagnostic	Output by the drive if it is jumpered in the slave mode, and input to the drive if jumpered in the master mode. The signal indicates to a master that the slave has passed its internal diagnostic command. The master drive determines the state of this pin and returns the slave diagnostic status to the host with its own.

(Continued)

Table 11-5. (Continued)

Pin Name	Pin Number	I/O	Signal Name	Signal Description
HCS0-	37	I	Host chip select 0	Chip select decoded from the host address bus. Used to select some of the host accessible registers.
HCS1-	38	I	Host chip select 1	Chip select decoded from the host address bus. Used to select some of the host-accessible registers.
DASP-	39	I/O	Drive active/ slave present	Time-multiplexed signal that indicates drive active or slave present. When the drive is executing a diagnostic command, this line is an output from a slave drive, and and input to a master drive indicating that a slave drive is present. At all times other than during diagnostics, this line is an output from both master and slave drives which is active when the drive is selected and being accessed (BSY is active), and is used to drive an activity LED indicator. This signal must be an open-collector output.
GND	2 19 22 24 26 30 40	-	Ground	Signal ground returns for the interface lines.
RSVD	21 27 29	-		Reserved pins.
KEY	20	-		Pin used for keying the interface connector.

11.6 130-MB FIXED DISK DRIVE SYSTEM

The 130-MB fixed disk drive system provides 130 MB of data storage on a full-height, fixed disk drive. This system:

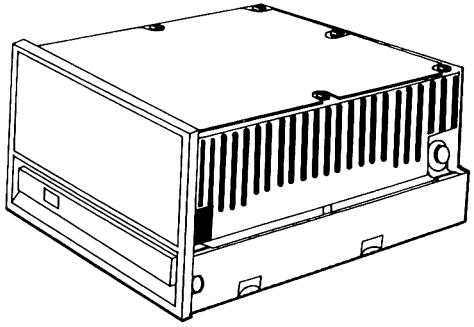
- Uses an ESDI-type fixed disk drive controller in a 16-bit expansion slot on the system board (typically slot 6).
- Provides a data-transfer rate of 10 Mb/s.

130-MB Fixed Disk Drive

The 130-MB fixed disk drive is a high-capacity, high-speed, full-height, ESDI-compatible fixed disk drive.

It is supported on the 12-MHz DESKPRO 286.

Figure 11-5 shows the 130-MB fixed disk drive:



130—MB Fixed Disk Drive

Figure 11-5. 130-MB Fixed Disk Drive

Figure 11-6 shows the functional block diagram for the 130-MB fixed disk drive.

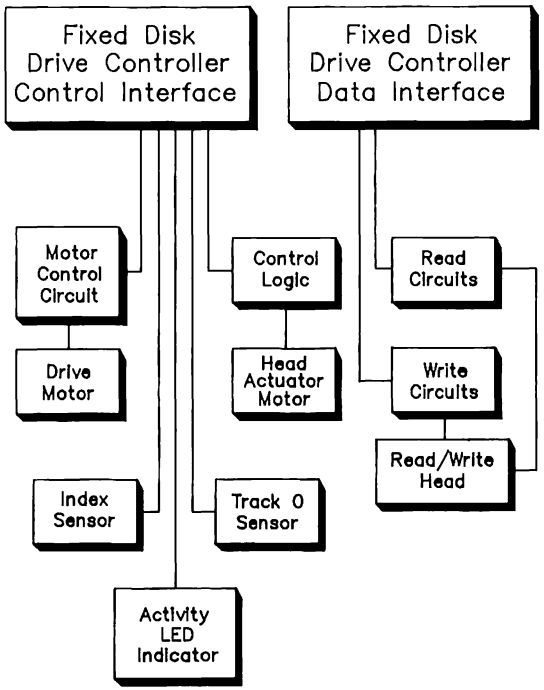


Figure 11-6. 130-MB Fixed Disk Drive Functional Block Diagram

Logical Configuration

The 130-MB fixed disk drive has an ESDI interface and contains circuitry normally found on a fixed disk drive controller.

Most fixed disk drives contain 17 sectors of data per track. The 130-MB fixed disk drive has 35 sectors per track. One of these sectors is reserved for error management--when a sector is detected as bad, the diagnostic software reassigns the reserved sector to replace the bad sector.

Because some operating systems are not adapted to a 34-sector arrangement, the 130-MB fixed disk drive system has a Translate mode to rearrange the logical configuration of the drive. In the Translate mode, as drive type 25, the drive appears to have 17 sectors per track instead of 34 and 16 heads instead of 8.

The 130-MB fixed disk drive can be used as drive type 35, which operates in the non-Translate mode. Using the drive in this mode may allow improved performance in some applications. For DOS systems to use drive type 35, the DOS must be Version 3.2 or later.

Configuring the 130-MB Fixed Disk Drive System

The fixed disk drive should have its drive-select jumpers set to DS1. A terminating resistor pack is installed on the fixed disk drive of a single fixed disk drive system, which is all that is allowed.

Figure 11-7 shows an interconnection diagram for the 130-MB fixed disk drive system.

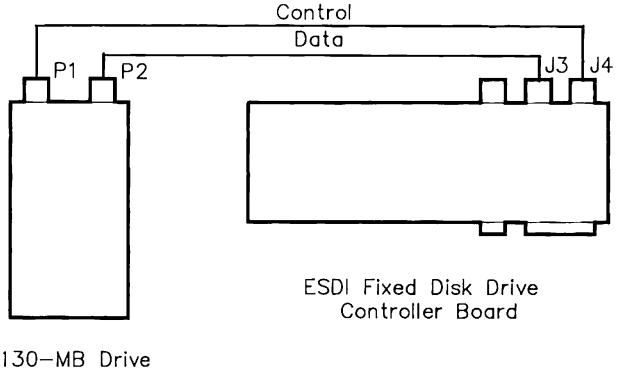


Figure 11-7. 130-MB Fixed Disk Drive System Interconnection Diagram

Jumpers

Table 11-6 describes the fixed disk drive controller jumpers.

Table 11-6. Fixed Disk Drive Controller Jumpers

Jumper	Function
W3	Fixed Disk Drive Base Address Select. This address selection is available only for special circumstances and under normal circumstances should never be changed. W3,2-3 Standard Address Select (1F0h, standard setting) W3,1-2 Alternate Address Select (170h)
W2	Translate or non-Translate Mode Select. The absence of this jumper allows the mode to be software programmable. The presence of this jumper forces the controller into non-Translate mode.

In the Translate mode, the fixed disk drive controller changes the logical arrangement of data on the fixed disk drive, so that the fixed disk drive appears to have 17 sectors per track and 16 heads.

The controller jumpers are shown in Figure 11-8.

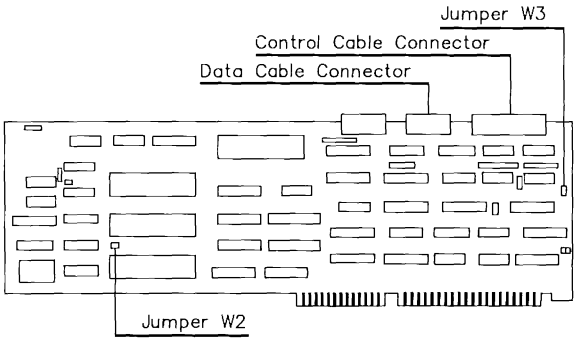


Figure 11-8. ESDI Fixed Disk Drive Controller Board

ESDI Fixed Disk Drive Controller

The ESDI fixed disk drive controller is compatible with the ESDI standard that specifies signal, connectors, and command protocols.

The ESDI controller:

- Provides for the control of the 130-MB fixed disk drive
- Plugs directly into a 16-bit expansion slot
- Incorporates a 56-bit error correction code (ECC) polynomial for error detection and correction
- Has on-board diagnostics

Figure 11-9 shows the functional block diagram for the ESDI controller.

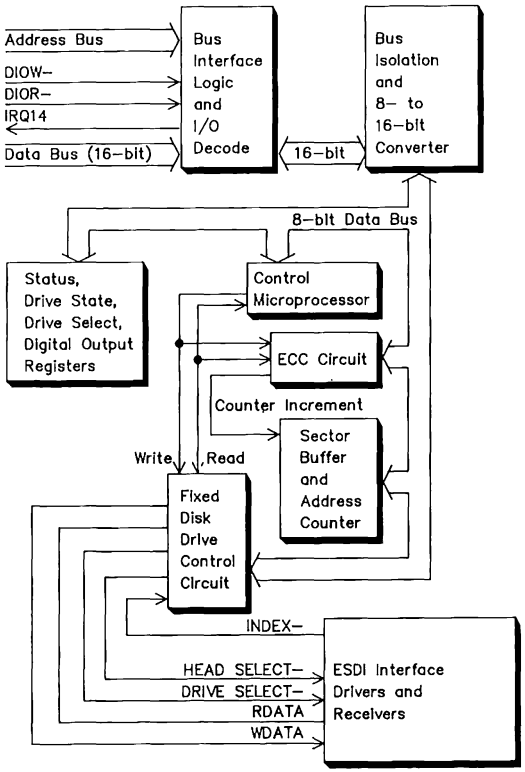


Figure 11-9. ESDI Fixed Disk Drive Controller Functional Block Diagram

ESDI Controller Commands

The ESDI controller is compatible with all software written for the ST506-compatible fixed disk drive controller.

The ESDI controller supports all the commands listed in Chapter 6, Fixed Disk Drive Controller Board

For the ESDI controller, the Write Precompensation Cylinder register (I/O address 1F1h) is reserved. Write precompensation is not programmable on ESDI drives.

For the Seek and Recalibrate commands, the step rate codes are ignored on the 130-MB controller.

Connectors

Table 11-7 describes the 34-pin control cable connector pinouts and signal descriptions. All I/O designations are with respect to the drive.

Table 11-7. 34-Pin Control Cable Connector Signal Descriptions

Signal	Pin (See Note)	I/O	Description
HEAD SELECT 2^3-	2	I	Lines that allow selecting individual read/write heads in a binary code sequence.
2^2-	4		
2^0-	14		
2^1-	18		
WRITE GATE-	6	I	Allows data to be written on the disk.
CONFIG/STATUS DATA-	8	O	Drive presents serial data on this line upon request from the controller.
TRANSFER ACK-	10	O	Line from the drive indicating that a transfer request has been acknowledged and valid data transferred. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-.
ATTENTION-	12	O	Signal from the drive indicating the drive wants the controller to request its status.
SECTOR-	16	O	Indicates the beginning of a sector.
INDEX-	20	O	Indicates the beginning of a track
READY-	22	O	Signal indicates only that the spindle is up to speed.
TRANSFER REQ-	24	I	Line from the controller requesting that one bit of data be sent between the drive and the controller. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-.
DRIVE SELECT 1-	26	I	These bits provide the binary-coded drive select address.
DRIVE SELECT 2-	28	I	
READ GATE-	32	I	Signal allows data to be read from the disk.
COMMAND DATA	34	I	When a command is issued, 16 information bits of serial data, plus parity, are sent to the drive on this line.
RESERVED	30		

Note: All odd numbered pins are ground.

Table 11-8 describes the 20-pin data cable connector pinouts and signal descriptions. All I/O designations are with respect to the drive.

Table 11-8. 20-Pin Data Cable Connector Description

Signal	Pin	I/O	Description
DRIVE SELECTED-	1	O	A status line provided to inform the controller system of the selection status of the drive.
SECTOR-	2	O	Indicates the beginning of a sector.
COMMAND COMPLETE-	3	O	A status line that indicates command completion to the controller.
ADDRESS MARK ENABLE-	4	O	The trailing edge of this signal with the WRITE GATE- asserted initiates writing the sync field on the drive.
+READ/REFERENCE CLOCK	10	O	Differential clock signal used for reading data bits from the drive.
-READ/REFERENCE CLOCK	11	O	
+NRZ WRITE DATA	13	I	A differential pair
-NRZ WRITE DATA	14	I	that defines the data to be written on the track.

(Continued)

Table 11-8. (Continued)

Signal	Pin	I/O	Description
+NRZ READ DATA	17	O	Data recovered by
-NRZ READ DATA	18	O	reading previously written information is transmitted to the controller via this differential pair.
+WRITE CLOCK	7	I	A differential pair of
-WRITE CLOCK	8	I	clocks used for writing data bits to the drive.
INDEX	20	O	Indicates the beginning of a track.
GROUND	5, 6, 7 12, 15, 16 19		

Figure 11-10 shows the pinout of J3, the data cable connector.

Signal	Pin		Pin	Signal
−DRIVE SELECTED	1	2		−SECTOR
−COMMAND COMPLETE	3	4		−ADDRESS MARK ENABLE
SIGNAL GROUND	5	6		SIGNAL GROUND
+WRITE CLOCK	7	8		−WRITE CLOCK
SIGNAL GROUND	9	10		+READ/REFERENCE CLOCK
−READ/REFERENCE CLOCK	11	12		SIGNAL GROUND
+NRZ WRITE DATA	13	14		−NRZ WRITE DATA
SIGNAL GROUND	15	16		SIGNAL GROUND
+NRZ READ DATA	17	18		−NRZ READ DATA
SIGNAL GROUND	19	20		−INDEX

Figure 11-10. J3, Data Cable Connector

Figure 11-11 shows J4, the control cable connector.

Signal	Pin		Pin	Signal
GROUND	1	2		HEAD SELECT 2^3−
GROUND	3	4		HEAD SELECT 2^2−
GROUND	5	6		WRITE GATE−
GROUND	7	8		CONFIG/STATUS DATA−
GROUND	9	10		TRANSFER ACK−
GROUND	11	12		ATTENTION−
GROUND	13	14		HEAD SELECT 2^0−
Key	15	16		SECTOR−
GROUND	17	18		HEAD SELECT 2^1−
GROUND	19	20		INDEX−
GROUND	21	22		READY−
GROUND	23	24		TRANSFER REQ−
GROUND	25	26		DRIVE SELECT 1−
GROUND	27	28		DRIVE SELECT 2−
GROUND	29	30		Reserved
GROUND	31	32		READ GATE−
GROUND	33	34		COMMAND DATA−

Figure 11-11. J4, Control Cable Connector

Chapter 12

FIXED DISK DRIVE BACKUPS

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FIXED DISK DRIVE BACKUP SYSTEMS

12.1 INTRODUCTION

Three sizes of fixed disk drive backup (tape) are avaiable:

- 10-Megabyte Tape Backup
- 40-Megabyte Tape Backup
- 135-Megabyte Tape Backup (among the 80286-based products, supported only on the 12-MHz COMPAQ DESKPRO 286®).

12.2 10- AND 40-MEGABYTE FIXED DISK DRIVE BACKUP (TAPE)

The 10-megabyte fixed disk drive backup uses a 3M DC 1000 tape cartridge or equivalent and the COMPAQ TAPE Utility Version 1 to provide a data backup for fixed disk drives. The fixed disk drive backup stores up to 10 megabytes of data on a single tape cartridge.

The 40-megabyte fixed disk drive backup (tape) uses a 3M DC 2000 tape cartridge or equivalent and the COMPAQ® TAPE Utility Version 2.0 (or later) or other Tape Utilities to provide a data backup for fixed disk drives. The 40-megabyte fixed disk drive backup stores a maximum of 40 megabytes of data on a single tape cartridge. 3M DC 1000 tape cartridges which were created on a 10-megabyte fixed disk drive backup can be read on a 40-megabyte fixed disk drive backup but cannot be written.

The fixed disk drive backup is connected in a daisy-chain manner with the diskette drives. An NEC 765A diskette controller controls all fixed disk drive backup functions and data formats.

Figure 12-1 shows the fixed disk drive backup systems.

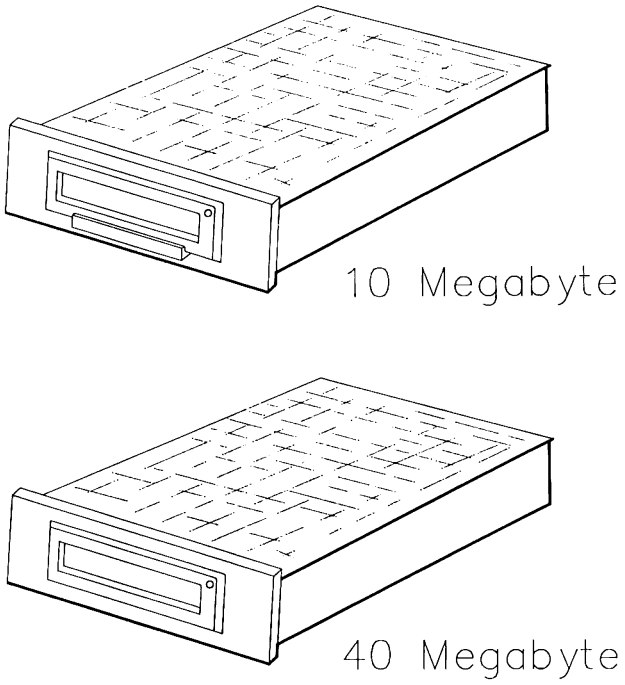


Figure 12-1. Fixed Disk Drive Backup Systems (Tape Drive)

The fixed disk drive backup consists of a microprocessor, firmware, stepper motor, drive motor, read/write head, and a control logic board.

The 40-megabyte and 10-megabyte fixed disk drive backup logic board uses a Z8 microprocessor with 8 kbytes of ROM to control the drive. The logic board connects to the:

- Movable head, which reads and writes data
- Cartridge-installed sensor
- Write-protect sensor
- End-of-tape/beginning-of-tape (EOT/BOT) sensor
- Stepper motor, which positions the head
- DC power supply
- Drive motor, which advances and rewinds the tape
- Diskette/Tape Controller Board

Figure 12-2 is a functional block diagram of the fixed disk drive backup systems.

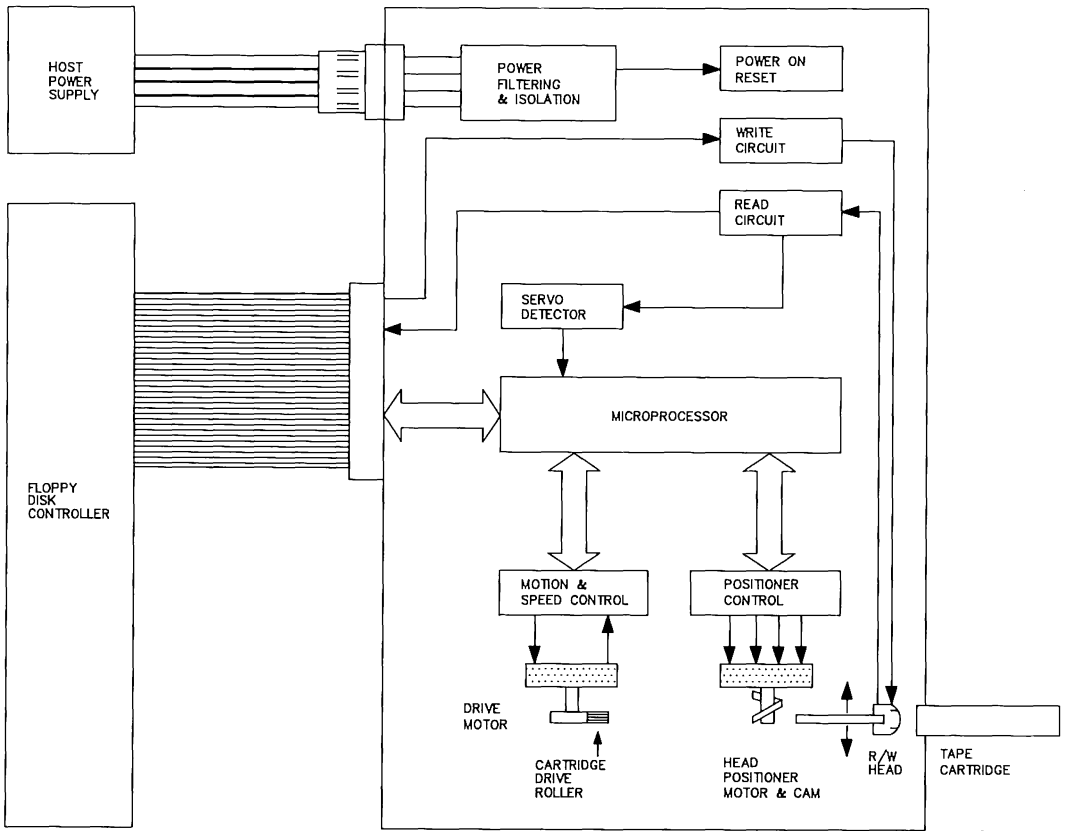


Figure 12-2. Fixed Disk Backup Tape Drive Functional Block Diagram (10- and 40-Megabyte)

Specifications

Table 12-1 lists the physical and electrical specifications of the fixed disk drive backup systems.

Table 12-1. 40-Megabyte and 10-Megabyte Fixed Disk Drive Backup Systems Physical and Electrical Specifications

	40-Megabyte Fixed Disk Drive Backup		10-Megabyte Fixed Disk Drive Backup
Size:			
Width	5.65 in. (144 mm)		Same
Height	1.65 in. (41 mm)		Same
Depth	8.00 in. (203 mm)		Same
Weight	1.7 lb (0.77 kg)		Same
Formatted capacity (with ECC)	40.63 megabyte		10.35 megabyte
Flux reversal density	10000 FRI		6400 FRI
Data-transfer rate	500 kb/s		250 kb/s
Head positioning time:			
Adjacent tracks	250 ms		Same
Move (worst case)	1 sec		Same
Tape speed:			
Read/write	50 in./s		39 in./sec
Rewind/fast forward	70 in./s		70 in./sec
Tape end-to-end positioning time:	DC 1000 (see Note 1)	DC 2000	DC 1000 (see Note 2)
Read/write	44 sec	49 sec	57 sec
Forward/reverse	31 sec	35 sec	31 sec
Track density	83 TPI		59 TPI
Number of tracks	20		8
Blocks/track	124		158
Sectors/block	18 (2 for ECC)		8
Bytes/sector	1024		1024

Notes: 1. The 10-megabyte fixed disk drive backup uses DC 1000 tape cartridges (supported on other COMPAQ products) which can be read by the 40-megabyte fixed disk drive backup. The 40-megabyte fixed disk drive backup cannot write to a DC 1000 tape cartridge, but can erase a DC 1000 tape cartridge.

2. DC 2000 tape cartridge does not physically fit into a 10-megabyte fixed disk drive backup.

Fixed Disk Drive Backup Commands

All fixed disk drive backup operations are one of five processes:

1. Servo-Write, which initializes the tape media by writing indexing information.
2. Tape Format, which writes block, sector, and track information onto the tape. This information joins the indexing information previously written by Servo-Write. This process prepares data areas consistent with the NEC 765A diskette drive controller data format.
3. Write-Data, which writes information in the same layout as standard diskette tracks.
4. Read-Data, which reads information in the same layout as diskette tracks.
5. Erase, which erases all information on tape, including servo and data information. (Supported only on the 40-megabyte fixed disk drive backup.)

The Servo-Write operation is initiated by executing an Enter Format Mode command followed by the Servo-Write command. This action moves the tape to the beginning, at block 0 and head 0, and then writes encoding index pulses on the tape in a streaming-write mode. These pulses are used solely by the fixed disk drive backup and are not available to the programmer.

NOTE: If the Servo-Write operation is interrupted, the tape cartridge must be fully erased before it can be used again.

The format operation for tape is similar to the format process for diskette drives. To format the tape, the multipurpose controller board takes control of the interface and supplies the track and sector data for every block on the track. The data format on the tape has the characteristics of a diskette.

The fixed disk drive backup systems accept commands from the multipurpose controller board as pulses on the step line. The number of pulses determines the desired command. Any number of pulses not recognized as commands are ignored. The fixed disk drive backup does not recognize the step pulses unless the NEC 765A is programmed for a 3- or 6-ms gap between pulses. Table 12-2 lists the fixed disk drive backup commands.

Table 12-2. Fixed Disk Drive Backup Command Summary

Step Pulses	Command	Action
2	STOP MOTION	Stops tape - deactivates BUSY- signal.
3	PAUSE	Moves tape back two blocks - stops tape.
4	SEEK LOAD POINT	Rewinds tape at 50 IPS and goes to track 0.
5	MOVE TAPE FORWARD	Moves tape forward at 70 IPS (fast forward).
6	MOVE TAPE BACK	Moves tape backward at 70 IPS (rewind).
7	REPORT NORMAL COMPLETION	Latches BUSY- line if latest command has successfully completed.
8	REPORT DRIVE PRESENT	Latches BUSY- line if selected.
9	REPORT END	Latches BUSY- line if at end of tape.
10	REPORT BEGIN	Latches BUSY- line if at tape beginning.
11	REPORT CART	Latches BUSY- line if cartridge is present.
12	REPORT TRACK FOUND	Latches BUSY- line if track seek has completed.
13	REPORT NEW CARTRIDGE	Latches BUSY- line if cartridge has been replaced.
14	MOVE TAPE AGAINST DATA	Moves tape at 50 IPS (or 39 IPS if in low-density mode) toward file beginning.
15	MOVE TAPE WITH DATA	Moves tape at 50 IPS (or 39 IPS if in low-density mode) toward file end.
16	ENTER FORMAT MODE	Produces index pulses at end and beginning of data area to allow formatting by the 765. The drive must be in the Format mode to enable subsequent execution of the Servo Write command.
17	ENTER NORMAL MODE	Produces index pulses at beginning of data area.
18 *	REPORT EXPANDED INSTRUCTION SET	Pulses the BUSY- line if it supports the Expanded command set (commands 19, 28, and 29.)
19 *	REPORT DRIVE/CARTRIDGE TYPE	Pulses the BUSY- line. The controller responds with "N" step pulses to inquire about a specific status condition.
20	SEEK TRACK 0	Initiates tape motion and seeks track 0.
21	SEEK TRACK 1	Initiates tape motion and seeks track 1.
22	SEEK TRACK 2	Initiates tape motion and seeks track 2.
23	SEEK TRACK 3	Initiates tape motion and seeks track 3.
24	SEEK TRACK 4	Initiates tape motion and seeks track 4.

* These commands are not available with the 10-megabyte fixed disk drive backup.

(Continued)

Table 12-2. (Continued)

Step Pulses	Command	Action
25	SEEK TRACK 5	Initiates tape motion and seeks track 5.
26	SEEK TRACK 6	Initiates tape motion and seeks track 6.
27	SEEK TRACK 7	Initiates tape motion and seeks track 7.
28 *	SEEK TRACK "N"	Pulses BUSY- line. The controller responds with "N" step pulses.
29 *	ERASE TAPE	Erases entire tape.
31	SERVO WRITE	Writes servo pattern on blank cartridge. The drive must be in Format mode.
32	RECALIBRATE	Sends simulated "at track 0" status to multipurpose controller board for diskette drive compatibility.

* These commands are not available with the 10-megabyte fixed disk drive backup.

Command 19 causes the drive to pulse the BUSY- line. The controller responds with "N" pulses to inquire for a specific status condition. Table 12-3 gives the pulses used for the various status conditions. Command 19 is not available with the 10-megabyte fixed disk drive backup.

Table 12-3. BUSY- Line Pulses for Status

"N" Step Pulses	Status Condition	Drive BUSY- Response	Status
4	Cartridge Type	Low	DC 2000 cartridge in drive.
		High	DC 1000 cartridge in drive.
5	Servo Density	Low	High-density, servo written, transfer rate at 500 kHz, R/W speed at 50 IPS.
		High	Low-density, servo written or blank cartridge. Transfer rate at 500 kHz, R/W speed at 39 IPS.
6	Drive Type	Low	40-Megabyte fixed disk drive backup.
		High	10-Megabyte fixed disk drive backup.

Connectors

The fixed disk drive backup systems use the same cable, connectors, and pin arrangements as the diskette drives for the connections to the multipurpose controller board or multipurpose fixed disk controller board and the DC power supply.

The signal functions are different, however, and special software drivers are used to control the fixed disk drive backup systems. Table 12-4 shows the signal functions.

Table 12-4. Drive Logic Board to Drive Controller Signal Descriptions

Signal Name	Function
DRIVE 4 (TAPE) SELECT-	Drive select 4 is used to select 40-megabyte fixed disk drive backup.
INDEX-	Indicates to the multipurpose controller board that one block has passed.
READ DATA-	This is the data stream of data and clock pulses from the 40-megabyte fixed disk drive backup.
STEP-	Pulses give commands to the fixed disk drive backup.
BUSY-	Indicates to the multipurpose controller board that the fixed disk drive backup is still executing a command.
WRITE DATA-	This stream of data is written to the tape when WRITE GATE- is enabled.
WRITE GATE-	Enables the drive-logic disk-write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	Indicates to the multipurpose controller board that the cartridge in the drive is write-protected.

Figures 12-3 and 12-4 show the fixed disk drive backup system connectors.

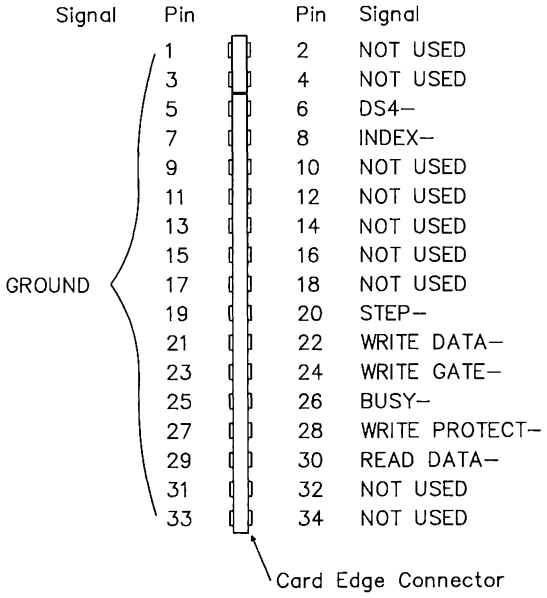


Figure 12-3. Fixed Disk Drive Backup Connector Pinout

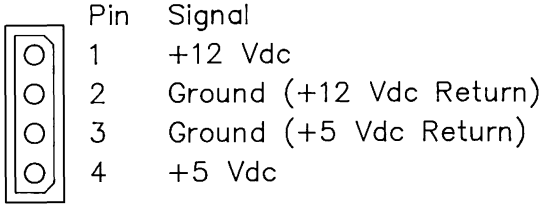


Figure 12-4. Fixed Disk Drive Backup Power Connector Pinout

Tape Format

The tape utility begins formatting with a SERVO-WRITE process. The SERVO-WRITE process divides the tape into sections called servo-blocks. Table 12-5 lists the track and sector sizes for the DC 1000 and DC 2000 tape cartridges.

Table 12-5. Tape Track/Sector Sizes

Tape Cartridge	DC 1000	DC 2000
Number of tracks	8	20
Number of blocks/track	158	124
Number of sectors/block	8 (Note 1)	18 (Note 2)
Number of bytes/sector	1024	1024

Notes: 1. Xenix uses two sectors for ECC, leaving 6 data sectors.
2. Two sectors are ECC, leaving 16 data sectors available.

The tape utility then writes format data into the servo-blocks. Each of the tape tracks is formatted by the NEC765A diskette controller to yield a specific number of 1024-byte sectors per block. The data is written in double-density or modified frequency modulation (MFM) with the same layout as a standard diskette track. Table 12-6 gives the data format for the tape.

Table 12-6. Tape Data Format

	Nominal Value(hex)	Number of Bytes
(Index pulse) Pre-index Gap	4E	80
Pre-index Address Mark Sync	00	12
Index Address Mark	FC(Note 1)	4
Gap 1	4E	50
Pre-ID AM Sync	00 (Note 2)	12
ID Address Mark	FE (Note 2)	4
Sector ID	xx (Note 3)	4
Sector ID CRC	xx (Note 3)	2
Gap 2	4E	22
Pre-Data AM Sync	00	12
Data Address Mark	FB (Note 2)	4
Data	xx (Note 3)	1024
Data CRC	xx	2
Gap 3	4E	54
Gap 4	4E	(until second index pulse)

Notes: 1. First 3 bytes are C2 with missing clock transition between bits 3 and 4.
2. First 3 bytes are A1 with missing clock transition between bits 4 and 5.
3. xx = data dependent.

The Gap 3 value (54 bytes) shows the gap size when the tape is formatted. The Gap 3 size specified in the read/write commands is smaller (23 bytes). The size of Gap 4 depends on the tape speed. The NEC765A keeps writing until the second index pulse occurs.

The boxed field of Table 12-5 is written once for each sector in the block, with appropriate sector ID values for each sector written. The sector ID consists of four 1-byte fields that are used to identify each sector (using diskette mnemonics):

CYL	HEAD	SECT	SIZE	(CRC)	(CRC)

40-megabyte fixed disk drive backup:

```
Cylinder = 0..123  Tape block number
Head     = 0       (Not used)
Sector   = 1..18*  Sector number (within tape block)
Size     = 3       Sector size (3 denotes 1024 bytes)
```

*Two sectors are for ECC, 16 data sectors are available.

10-megabyte fixed disk drive backup

```
Cylinder = 0..157  Tape block number
Head     = 0       (Not used)
Sector   = 1..8    Sector number (within tape block)
Size     = 3       Sector size (3 denotes 1024 bytes)
```

Tape Utilities

Compaq provides TAPE Utilities to use with the fixed disk drive backup systems. These utilities make the 10-megabyte and the 40-megabyte fixed disk drive backup systems available to MS-DOS users.

This section provides information on the data format used by the COMPAQ TAPE Utilities. This description includes the tape header information, tape identification area, save set descriptions, file allocation table, and directory and file information.

The 10-megabyte fixed disk drive backup uses only a DC 1000 tape cartridge. The 40-megabyte fixed disk drive backup can accept either a DC 1000 or DC 2000 tape cartridge. Some differences in the support between the two drives reflects this difference in tape cartridges.

MS-DOS File Storage (Tape)

The format of the data depends on the Tape Utility used to write the data to the tape. This section discusses the format of data written to the tape, DC 1000 and DC 2000, using COMPAQ TAPE Utilities. Two versions of COMPAQ TAPE Utility exist. Tape Utility Version 1 supports only the 10-megabyte fixed disk drive backup. Tape Utility Version 2 supports both the 10-megabyte and the 40-megabyte fixed disk drive backup, and can read data from a 10-megabyte tape backed up with Tape Utility Version 1. It can also erase a 10-megabyte tape.

The COMPAQ TAPE Utilities place a tape header (HDR) and a file allocation table (FAT) at the beginning of the tape (Track 0, Block 0).

When a set of files is written to the tape, the HDR and the FAT are modified to reflect the new tape status. A redundant copy of the HDR and FAT is stored in Track 0, Block 1. If the first block becomes unreadable, the information in the second block is used to retrieve the data on the tape. All remaining blocks contain directory and file information.

COMPAQ TAPE Utility, Version 2 generates an error correction code (ECC) when writing to a DC 2000 tape. The ECC is stored in the last two sectors of each block. Figure 12-5 shows the format of the blocks.

Block	Sector 1	2	3	...	15	16	17	18
0	HDR	FAT	FAT	...	FAT	FAT	ECC	ECC
1	HDR	FAT	FAT	...	FAT	FAT	ECC	ECC
2	FILES	...	...	...	...	...	ECC	ECC
.								
.								
.								

Figure 12-5. MS-DOS Track 0 Format (DC 2000 tape)

Figure 12-6 shows the format for Track 0 data without ECC. No ECC is generated by Tape Utility Version 2 when used with a 10-megabyte fixed disk drive backup.

Block	Sector 1	2	3	4	5	6	7	8
0	HDR	FAT	FAT	FAT	(FAT)	(FAT)	(FAT)	(FAT)
1	HDR	FAT	FAT	FAT	(FAT)	(FAT)	(FAT)	(FAT)
2	FILE	...						
.								
.								
.								

Figure 12-6. MS-DOS Tape Track 0 Data (DC 1000 tape)

Tape Header

The tape header (HDR) occupies the first 1024-byte sector on the tape. The tape header is divided into several sections, the Tape Identification area (TID), the Save Set Description area, and a reserved area. Figure 12-7 provides a summary of the tape header format.

COMPAQ TAPE Utility	TID	Save Set Description	Reserved
Version 1	64 Bytes	N/A	960 bytes
Version 2	64 Bytes	768 bytes	192 bytes

Figure 12-7. MS-DOS Tape Header

Tape Identification Area

Table 12-7 lists the contents of the Tape Identification area. Table 12-8 further explains the contents of the Tape Identification area.

Table 12-7. Tape Identification Area

Address	Function	COMPAQ TAPE Utilities Bytes
0	Reserved (must be zero)	2
2	Volume name	32
34	Create (format) time	2
36	Create (format) date	2
38	Tracks per tape	2
40	Blocks per track	2
42	Sectors per block	2
44	Bytes per sector	2
46	Tape number	2
48	More flag (for multiple-tape backup)	2
50	Backup time	2
52	Backup date	2
54	Program version (in BCD)	2
56	Format type	2
58	Reserved	6

Table 12-8. Tape Identification Area Parameters

Parameter Name	Description
Volume name	Up to 31 characters in length, padded with zeros to 32 bytes, resulting in a 'standard' null-terminated string
Date/time the tape was initialized	Set only when the tape is formatted (by TAPE FORMAT or TAPE BACKUP), and is not updated by a normal BACKUP operation. (See Figure 12-8)
Number of tracks per tape	20 for 40-megabyte tape, numbered 0..19, 8 for 10-megabyte tape, numbered 0..7
Number of intra-servo blocks per tape track	124 for 40-megabyte tape, numbered 0..123, 158 for 10-megabyte tape, numbered 0..157
Number of sectors per block	18 for 40-megabyte tape, numbered 1..18, 8 for 10-megabyte tape, numbered 1..8
Number of bytes per sector	1024
Tape number	The number of this tape in a multiple-tape backup set. For a single-tape backup, this entry is 1
More flag	This word is set to 1 to indicate that there are additional tapes in the backup set, or 0 to indicate that this is the last tape in the set. For a single tape backup, this entry is 0
Date/time	The Date/time is written by BACKUP when the tape was backed-up and updated. (See Figure 12-8)
Tape utility version (in BCD)	The version of the COMPAQ TAPE Utility that wrote the tape 0000h = Tape Utility before Version 1.10 0110h = TAPE Utility Version 1.1 02xxh = TAPE Utility Version 2.xx
Format Descriptor	The low byte of this word appears at offset +56 in the first sector of the tape. The format descriptor is used by the software to determine the tape format by recognizing the following codes: 0 - Tape is unused 1 - Reserved 2 - Reserved 3 - Tape used by COMPAQ TAPE Utility prior to version V1.10 4 - Tape used by COMPAQ TAPE Utility version V1.10 and later

Figure 12-8 shows the format of the time and date parameters of the Tape Identification area.

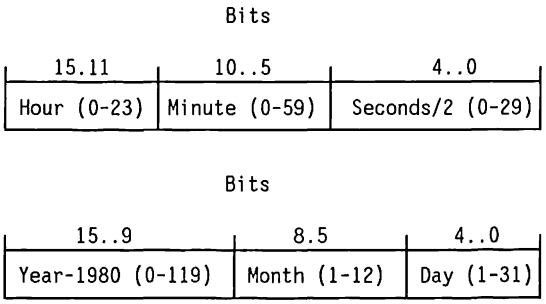


Figure 12-8. Date and Time Format

Save Set Descriptions

The COMPAQ TAPE Utility Version 2 supports multiple backups per tape. (This feature does not apply to COMPAQ TAPE Utility Version 1.) Each time a set of files is backed up to the tape, a save set description containing 24 bytes is written to the tape header. Up to 32 save set descriptions can be stored in the 768-byte save set description area of the tape header. Table 12-9 lists the 24-byte save set parameters.

Table 12-9. Save Set Description

Function	Bytes
Backup time	2
Backup date	2
Version	2
Save Set label	12
Start block	2
Source drive	1
Reserved	3

Table 12-10 further explains the contents of the save set description.

Table 12-10. Save Set Description Parameters

Parameter Name	Description
Backup time/date	Time/date the save set was backed up. This entry in the last nonblank save set matches the backup time and data located in the TID area.
Tape Utility Version (in BCD)	The version of the COMPAQ TAPE Utility that wrote the save set.
Starting block of Save Set	Tape block number where the save set begins.
Backup source	Disk drive from drive which the save set was backed up.
Save Set label	Save set label, up to 11 characters in length. padded with zeros to 12 bytes, resulting in a standard null-terminated string.

File Allocation Table

The file allocation table (FAT) controls the assignment of sectors on the tape. For every sector on the tape, except for sectors containing ECC information, 2 bits are maintained in the FAT that describe the current state of that sector:

FAT Entry	Sector Status
0 0	Not allocated
0 1	Start of a file (header)
1 0	Allocated
1 1	Bad sector

NOTE: Any empty sectors in the last block of a save set are marked as allocated in the FAT.

Each FAT byte contains four 2-bit fields, with the least-significant bits describing the first sector. The FAT has allocation entries for the entire tape, including the tape HDR and FAT sectors. The entries for these sectors are "allocated."

Not all 16 available sectors on a DC 2000 tape cartridge are used for the FAT (not all are necessary).

The size (in bytes) of the FAT for a tape can be determined by the following formula:

> (Tracks x blocks per track x sectors per block x bits per sector)/8 bits per byte

The size (in bytes) of the FAT for a DC 1000 tape can be determined by the following formula:

> (8 tracks x 158 blocks per track x 8 sectors per block x 2 bits per sector)/8 bits per byte = 2528 bytes/FAT

Example: A DC 1000 tape with no bad blocks contains two files, one which occupies one sector, and one which occupies three sectors. The first 6 bytes of the FAT would appear as follows:

FAT entries for first block on tape:

```
10101010|10101010|
   AA   |   AA   |
```

FAT entries for second block on tape:

```
10101010|10101010
   AA   |   AA
```

FAT entries for files:

```
|10100101|00000000
|   A5   |   00
```

For a DC 2000 tape, the FAT table is:

(20 tracks x 124 blocks per track x 16 sectors per block x 2 bits per sector)/8 bits per byte = 39680/4 or 9920 bytes/FAT

Example: A DC 2000 tape with no bad blocks contains two files, one which occupies 1 sector, and one which occupies 3 sectors. The first 10 bytes of the FAT would appear as follows:

FAT entries for first block on tape:

10101010	10101010	10101010	10101010
AA	AA	AA	AA

FAT entries for second block on tape:

10101010	10101010	10101010	10101010
AA	AA	AA	AA

FAT entries for files:

10100101	00000000
A5	00

Directory Information

When writing data to a tape using COMPAQ TAPE Utility Version 2, all blocks after 0 and 1 on track 0 contain directory and file information. This section on directory information does not apply with COMPAQ TAPE Utility Version 1. If the backup spanned multiple directories, the first sector(s) of the save set contain directory information. This information tells the COMPAQ TAPE Utility which directories to create on the destination disk during the tape restore process. These sectors are marked as allocated in the FAT.

Table 12-11 lists the format of the directory information.

Table 12-11. Directory Information

Function	Bytes
Directory name 1	78
Last entry flag	2
Reserved for future use	2
.	
.	
.	
Directory name x	78
Last entry flag	2
Reserved for future use	2

Table 12-12 lists the directory information parameters.

Table 12-12. Directory Information Parameters

Parameter Name	Description
Directory name	Directory pathname, padded with zeros to 78 bytes, resulting in a standard null-terminated string
Last entry flag	End of the directory name list. This word is set to 1 if this is the last entry in the directory. If this is not the last entry, this word is 0.
Reserved	

Only the pathnames of the lowest level subdirectories are saved. All intermediate subdirectories can be recreated from these.

Example: The following directory names are generated for the directory shown in Figure 12-9:

```
\DOS
\TOOLS\EDITOR
\MISC\REPORTS\TEMP
\MISC\MEMOS
\MISC\EXPENSE
```

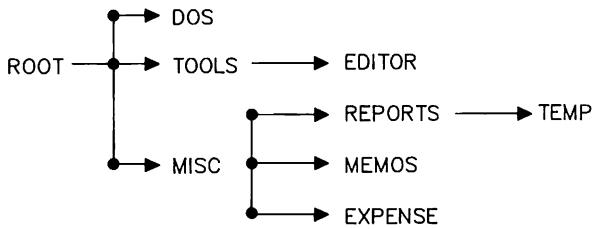


Figure 12-9. Sample Directory

File Information

Following the directory information (if any) are the sectors containing the file information.

The first sector of each file contains a header, which contains various information about the file.

Table 12-13 describes the file information.

Table 12-13. File Information

Function	Bytes
Header Signature (55h, AAh)	2
Filename	108
File Attribute	2
Original File Time	2
Original File Date	2
File Size (in bytes)	4
Backup Time	2
Backup Date	2
Aux File Attribute #1	2
Aux File Attribute #2	2

The file information parameters are given in Table 12-14.

Table 12-14. File Information Parameters

Parameter Name	Description
Header Signature	The 2-byte header signature is 55h, AAh. This signature is used to identify the header or separate it from the rest of the tape information.
Filename	The filename may be up to 107 characters in length, padded with zeros to 108 bytes, resulting in a standard null-terminated string. There is no structure imposed on the filename other than maximum length, but the COMPAQ TAPE Utility expects a DOS-style pathname (without a drive letter).
File Attribute	This word value is used by the COMPAQ TAPE Utility to retain the original attributes of the file as specified by the operating system. For MS-DOS, only the low-order byte is used.
Original Date/time	Original date/time of the file. (See Figure 12-3 for format)
File Size	32-bit file size (in bytes)
Backup Time and Date	The date and time the file was backed up. This value is the same as the corresponding value in the headers of all the other files that were part of the same backup .
Aux File Attribute #1	Not used in COMPAQ TAPE Utility prior to version 1.10. In version 1.10 and later: Bit 0, if set (=1), means that this file is continued on the next tape. In this case, the file size indicates only the portion of the file that is on this tape. Bit 1, if set (=1), means that this file is continued from the previous tape. In this case, the file size indicates only the portion of the file that is on this tape. If bit 1 is set (=1), with bit 0 reset (=0), this is the last portion of the file.
Aux File Attribute #2	Reserved, must be 0.

12.3 135-MB FIXED DISK DRIVE BACKUP (TAPE)

This section provides a detailed discussion of the 135-MB tape backup, supported on the 12-MHz COMPAQ DESKPRO 286.

It also provides information about the SY-TOS Operating System as well as the COMPAQ Tape Host Adapter.

The 135-MB tape backup includes the following features:

- No preformatting required
- Direct read after write
- Data verification
- Erase Bar
- Read QIC24 and QIC120 formatted cartridges

Figure 12-10 shows the 135-MB tape backup system. Figure 12-11 shows a functional block diagram of the 135-MB tape backup.

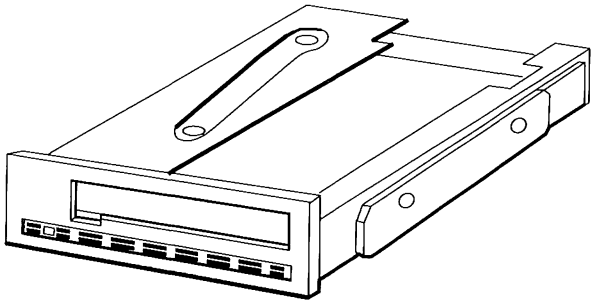


Figure 12-10. 135-MB Tape Backup

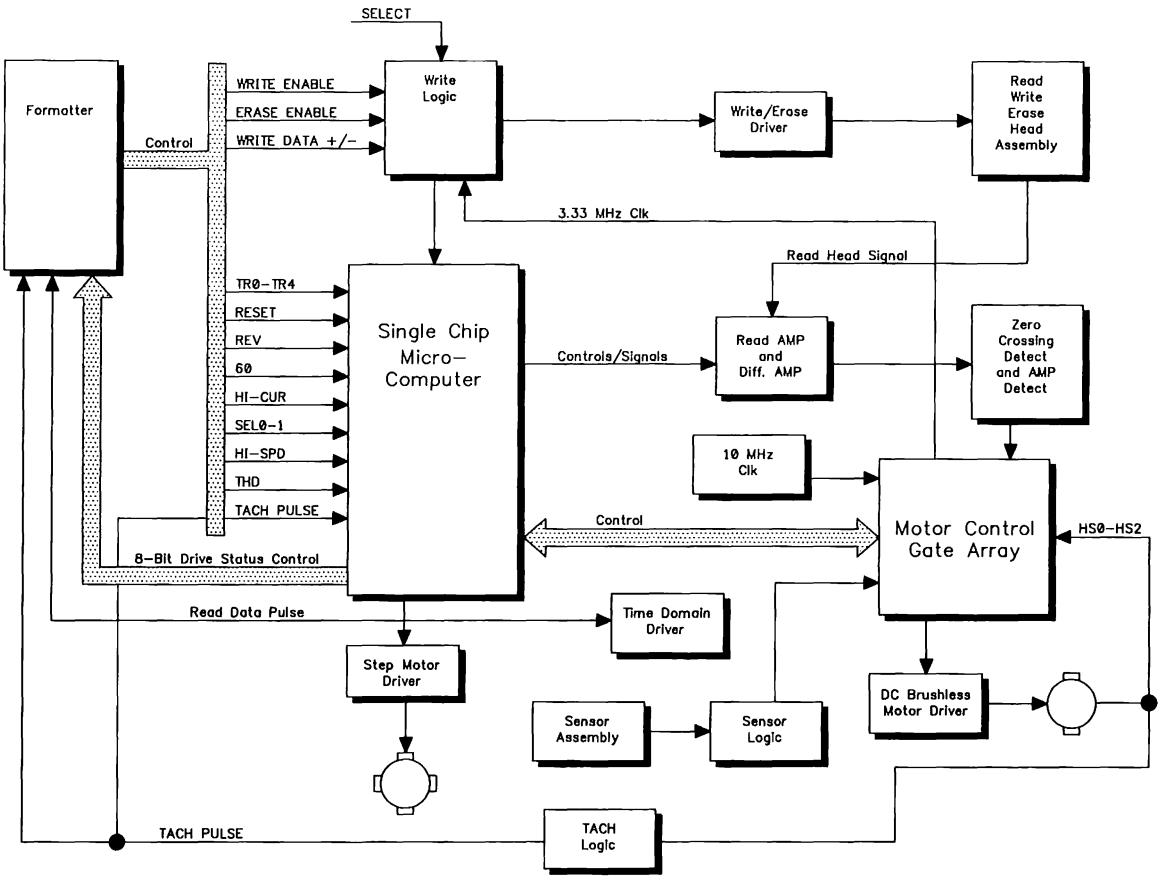


Figure 12-11. 135-MB Tape Backup Functional Block Diagram

135-MB Tape Backup Specifications

Table 12-15. 135-MB Tape Backup Physical and Electrical Specifications

Size:	
Width	5.8 inch (147 mm)
Height	1.7 inch (43 mm)
Depth	8.3 inch (211 mm)
Weight	2.4 lb (1.1 kg)
Formatted capacity (with ECC)	135 MB
Flux reversal density	12500 FRPI
Bit density	10000 BPI
Data-transfer rate	720 Kb/s
Tape speed:	
Read/write	72 in./second
Rewind/fast forward	90 in./second
Tape end-to-end positioning time:	DC 600XTD
Read/write	100 seconds
Forward/reverse	80 seconds
Track density	76 TPI
Number of tracks	18
Blocks/track	16,900
Bytes/block	512

135-MB Tape Backup Connector

The 135-MB tape backup interfaces the COMPAQ Tape Host Adapter via a 50-pin interface signal connector. Table 12-16 shows the signal functions of this connector.

Table 12-16. Tape Backup Logic Board to Tape Host Signal Descriptions

Pin Number	Signal	Function
02-10		Reserved.
12	DDATA7-	Tape Host Adapter Bus Bit 7, MSB
14	DDATA6-	Tape Host Adapter Bus Bit 6
16	DDATA5-	Tape Host Adapter Bus Bit 5
18	DDATA4-	Tape Host Adapter Bus Bit 4
20	DDATA3-	Tape Host Adapter Bus Bit 3
22	DDATA2-	Tape Host Adapter Bus Bit 2
24	DDATA1-	Tape Host Adapter Bus Bit 1
26	DDATA0-	Tape Host Adapter Bus Bit 0, LSB
28	ONL-	Online
30	REQ-	Request
32	RST-	Reset Controller
34	XFER-	Transfer
36	ACK-	Acknowledge
38	RDY-	Ready
40	EXC-	Exception
42	DIRTOHOST-	Direction to Host

Note: See Table 12-18 for signal descriptions

Figures 12-12 and 12-13, respectively, show the 135-MB tape backup control and power connectors.

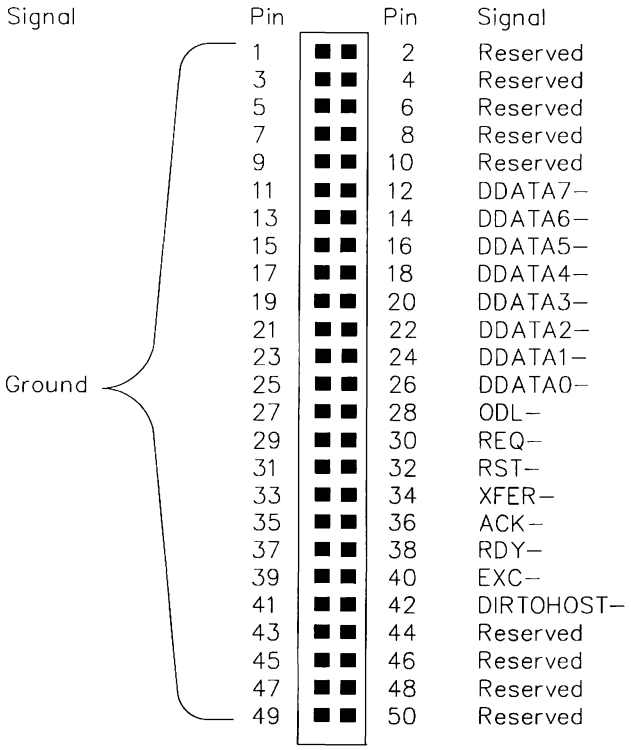


Figure 12-12. 135-MB Tape Backup Control Connector

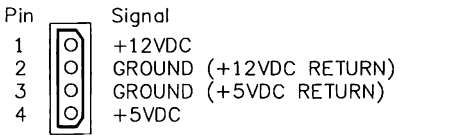


Figure 12-13. 135-MB Tape Backup Power Connector

135-MB Tape Backup Commands

Because the 135-MB tape backup uses the SY-TOS Tape Operating System for typical tape drive functions, this section only lists and briefly describes the 135-MB commands (Table 12-17).

Table 12-17. 135-MB Tape Backup Command Summary

Command	Command Code	Action
Select QIC-24	27h	Instructs the tape drive to read a 9-track QIC-24 format tape.
Select QIC-120	28h	Instructs the tape drive to write in the 15-track QIC-120 format.
Select QIC-150	29h	Instructs the tape drive to write in the 18-track QIC-150 format.
Write Data	40h	Causes data to be written on the tape.
Write without Underruns	41h	Instructs the tape drive to perform all functions of a WRITE command. Causes continuous tape movement.
Write File Mark	60h	Causes a FILE MARK to be written on the tape.
Write File Mark/Write	62h	Instructs the tape drive to combine the Write File command with a Write command to achieve streaming tape operation when writing file marks. Stops if underrun occurs.
Write File Mark/Write without Underruns	63h	Instructs the tape drive to combine the Write File Mark and a Write command to a achieve streaming tape operation whe writing file marks. Does not stop if underrunn occurs.
Read Data	80h	Causes data to be read from the tape to the tape drive.
Read Continuous	82h	Instructs tape drive to begin or continue a read operation, without stopping at File Marks.
Read Block (n)	8Ah	Allows the host to read to read any given block by addressing the block via its block number (n).
Space Forward	81h	Instructs the tape drive to logically move the tape forward over the subsequent data block or file mark.
Space Reverse	89h	Instructs the device to logically move the tape in a reverse direction over the previous data block or file mark.
Search to End of Recorded Media	A3h	Instructs the device to search for the end of the recorded media.

(Continued)

Table 12-17. (Continued)

Command	Command Code	Action
Read File Mark	A0h	Causes the tape in the tape drive to move to the EOM side of the next file mark.
Read File Marks	B1h..BFh	Identical in function to Read File Mark command except that the number of file marks read are equal to the binary value of nnnn. For example, 1011 0001 causes one file mark to be read and 1011 0010 causes to files marks to be read. In the case where nnnn is zero (0011 0000), the tape drive returns a illegal command status.
Read Status Command	C0h	Causes the tape drive to transfer to the host information about itself.
Erase Tape	22h	Completely erases the tape in the tape drive.
Rewind to BOT	C2h	Positions the tape in its tape drive.
Initialization (Retension)	24h	Conditions the tape as per specifications of media manufacturer.
Rewind to BOT	C2h	Positions the tape in its tape drive.
Rewind to BOT	C2h	Positions the tape in its tape drive.
Run Self-Test	C2h	Instructs the tape drive to perform self-test operations.
Run Self-Test 2	CAh	Instructs the tape drive to perform unique self-test operations.
Run Self-Test 3	CBh	Instructs the tape drive to perform self-test operations.
Read Firmware Identification	CFh	Instructs the tape drive to transfer to the host adapter six-bytes of identification data.
Select Drive	01h	Selects the tape drive for on-line operation.

SY-TOS Tape Operating System

The 135-MB tape backup uses the SY-TOS Tape Operating System for all tape backup functions.

For detailed information on the SY-TOS Tape Operating System, refer to the SY-TOS User's Guide provided with the 135-MB tape backup.

COMPAQ Tape Host Adapter

The COMPAQ Tape Host Adapter provides the interface for the 135-MB tape backup to the 12-MHz DESKPRO 286.

The tape host adapter:

- Interfaces the 135-MB tape backup to the DESKPRO 286
- Plugs directly into the 8-bit expansion slot (J108)
- Provides an 8-position switch for setting options and configuration settings.

Figure 12-14 shows the COMPAQ Tape Host Adapter. Figure 12-15 shows the COMPAQ Tape Host Adapter functional block diagram.

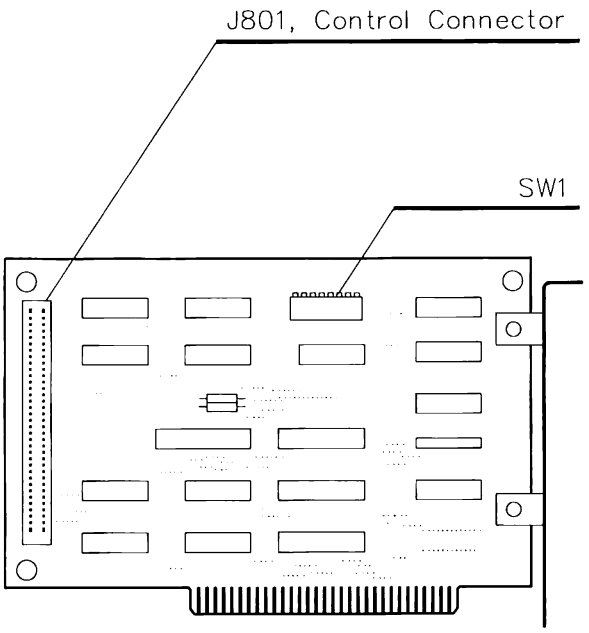


Figure 12-14. COMPAQ Tape Host Adapter

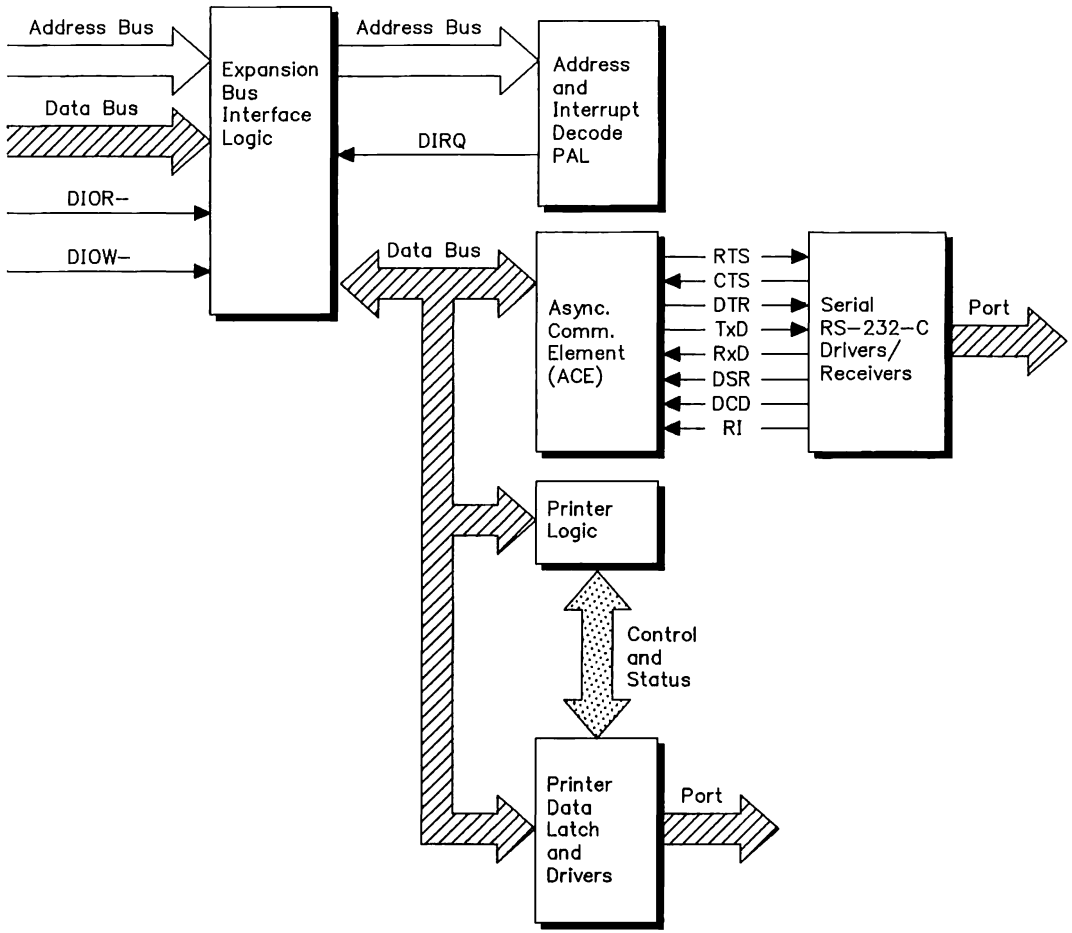


Figure 12-15. COMPAQ Tape Host Adapter Functional Block Diagram

Tape Host Adapter I/O Port Description

The tape host adapter interface is configured as two I/O addresses, beginning at one of two possible jp25

selectable base addresses. Table 12-18 defines the port addresses and their functions.

A more detailed description of the I/O port addresses follows Table 12-18.

Table 12-18. COMPAQ Tape Host Adapter I/O Port Description

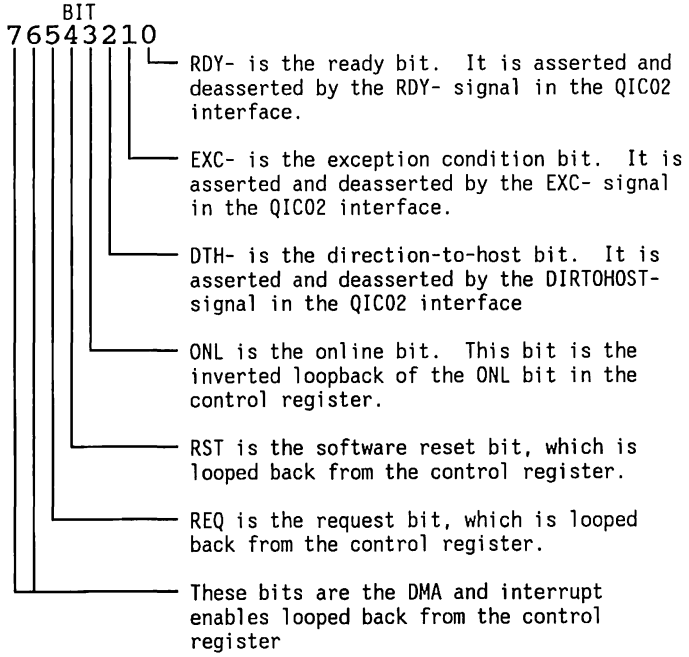
Address (Hex) Primary/Secondary	Read Function	Write Function
300/200	Status register	Control register
301/201	Data register	Data register

Data Register (Read/Write) (301/201)

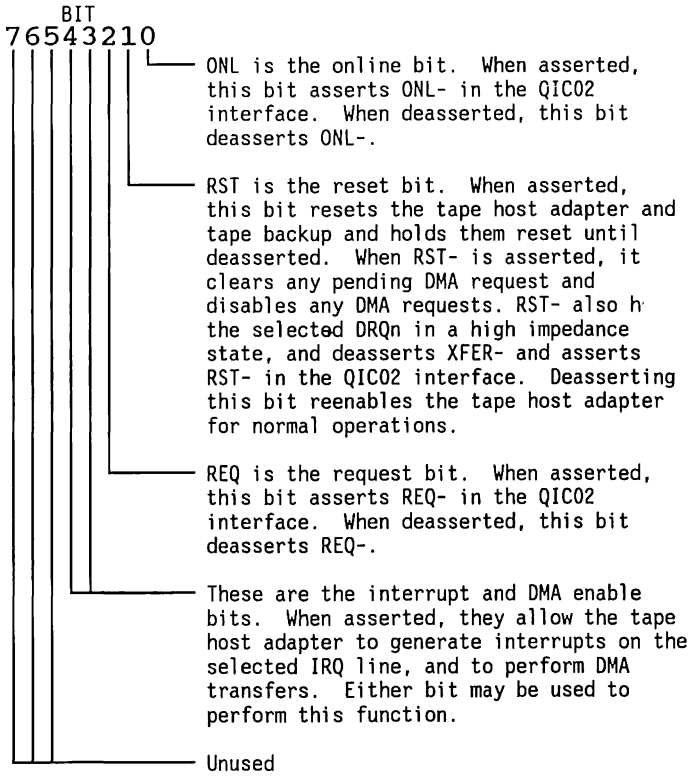
The data register is the port through which all command, status, and data bytes are transferred between the 12-MHz DESKPRO 286 and the tape host adapter. Command and status bytes are transferred by programmed I/O. Data bytes are transferred using DMA operations.

Status Register (Read Only) (300h/200h)

This register contains the status from the tape host adapter and the tape backup.



Control Register (Write Only)



Command Protocol

Commands for the COMPAQ Tape Host Adapter consists of the following general types:

- Status Transfer
- Data Transfer
- Drive Stand-alone

A command may be issued any time the tape backup is ready (RDY- active), and not online (ONL- is inactive), or when EXC- is asserted. Commands are issued by writing the command code to the data register of the tape host adapter,. asserting ONL for data transfer commands, asserting the control register REQ bit, and waiting until the tape backup transition from not-ready to ready. When this transition has occurred, deassert REQ and wait for another not-ready-to-ready transition.

On Drive Stand-alone commands, this second transition indicates the completion of the command.

For a Status Transfer command, this second transition and subsequent not-ready to ready transitions indicate that one of the bytes of status information is ready for reading by the host in the data register. After each status byte is read from the data register, REQ is asserted, not-ready is verified, and REQ is deasserted to complete the handshake protocol. When all status bytes have been transferred, the next not-ready to ready transition signals the completion of the command.

During Data Transfer commands, the second and all subsequent not-ready to ready transitions signal the first byte of each new block of data. On the first block of data, the tape host adapter DMA should not be enabled until after the Data Transfer command has been issued and accepted. The tape backup DIRTOHOST- signal must also be in the correct state and the DESKPRO 286 DMA controller has been programmed for the transfer.

The DESKPRO 286 DMA channel should then be unmasked, allowing the DMA transfer to take place. When the transfer is complete, which may be polled, or is signaled by an interrupt, the process starts over again at the next not-ready to ready transition. To begin the next transfer for each following block of data, take the following actions:

- Program the DESKPRO 286 DMA controller
- Unmask the DESKPRO 286 DMA channel

A Data Transfer command is terminated by reaching the end of tape, reading a file mask, or by deasserting the ONL bit in the control register.

When EXC- is asserted by the tape backup, the status of the tape backup must be transferred to the host before any other operation can begin. Typical times for EXC- to be asserted are:

- At power up
- After a software reset
- When the drive does not recognize an issued command code as a valid command
- When a command other than Read Status is issued when EXC- is active

This condition will be signaled by an interrupt, if interrupts are enabled, and will be available in the status register for polling. In response to seeing the EXC- bit asserted, the host must issue a Read Status command, any other command will be rejected.

Tape Host Adapter Connector

The 135-MB tape backup interfaces the COMPAQ tape host adapter through J801, the interface connector. The COMPAQ tape host adapter interfaces the 8-/16-bit expansion bus of the DESKPRO 286 through P1. Table 12-19 shows the signal functions for the tape host adapter interface connector, J801.

Table 12-19. Tape Host Adapter, J801 Connector Signal Descriptions

Pin	I/O	Signal	Signal Description
12	I/O	DDATA7-	Negative true
14	I/O	DDATA6-	bidirectional data bus between the
16	I/O	DDATA5-	tape host adapter and the tape
18	I/O	DDATA4-	backup. Bit <7> is the most
20	I/O	DDATA3-	significant.
22	I/O	DDATA2-	
24	I/O	DDATA1-	
26	I/O	DDATA0-	
28	O	ONL-	Online. Asserted before beginning a Read or Write command. Deasserted to terminate command.
30	O	REQ-	Request. Handshake signal for command or status byte transfers between the tape host adapter and system. It is asserted to indicate that the command byte has been placed on the data bus (DDATA) or that a status byte has been taken from the bus.
32	O	RST-	Reset. When asserted, RST- resets and holds the tape backup reset. Reenables tape backup when deasserted.

(Continued)

Table 12-19. (Continued)

Pin	I/O	Signal	Signal Description
34	O	XFER-	Transfer. Handshake signal for data byte transfers between the tape host adapter and the tape drive backup. It is asserted to indicate that a byte has been placed on the data bus (DDATA) during a write command, or that a byte has been taken from the data bus during a read command.
36	I	ACK-	Acknowledge. Handshake signal for data byte transfers between tape host adapter the tape backup. It is asserted to indicate that a byte has been taken from the data bus (DDATA) during a write command, or that a byte has been placed on the data bus during a read command.
38	I	RDY-	Drive Ready. This signal has three functions. First, it is an indication that a non-data transfer command has completed. Second, it is a handshake signal for command or status byte transfers between the tape host adapter and the tape backup. And third, it is an indication that the next block of data is ready for transfer during a Data Transfer command.

(Continued)

Table 12-19. (Continued)

Pin	I/O	Signal	Signal Description
40	I	EXC-	Exception condition. Indication from tape backup that a condition exists which requires the tape host adapter to perform a Get Status command before any other operation is begun
42	I	DIRTOHOST-	Direction to host. Indicates direction in which the tape backup is prepared to transfer data. When asserted, the transfer direction is to the tape host adapter. When deasserted, the direction is to the tape backup.
2, 4 6, 8, 10 44, 46 48, 50		Reserved	Reserved. These pins are not driven or received.
All Odd Pins		Ground	Signal Ground.

Switch Settings

Table 12-20 lists the switch settings for the COMPAQ Tape Host Adapter.

Table 12-20. Switch Settings for the COMPAQ Tape Host Adapter

Reference Designator	Function	Description and Default
SW1-1 SW1-2	Tape host interrupt select switches	SW1-1 = ON SW1-2 = OFF* Interrupt 5 (IRQ5) selected. SW1-1 = OFF SW1-2= ON: Interrupt 3 (IRQ3) selected.
SW1-3 SW1-4 SW1-5 SW1-6	Tape host adapter DMA channel select switches	SW1-3 and SW1-5 = ON* SW1-4 and SW1-6 = OFF:* DMA channel 3 selected. SW1-3 and SW1-5 = OFF SW1-4 and SW1-6 = ON: DMA channel 1 selected
SW1-7 SW1-8	Tape host adapter base address select switch	SW1-7 = ON * SW1-8 = OFF:* Primary base address (300h) selected. SW1-7 = OFF SW1-8 = ON: Secondary address (200h) selected.

* Default setting

Schematics

The schematics for the COMPAQ Tape Host Adapter are shown in Figure 12-16. Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided as an aid to understanding the operation of the tape host adapter.

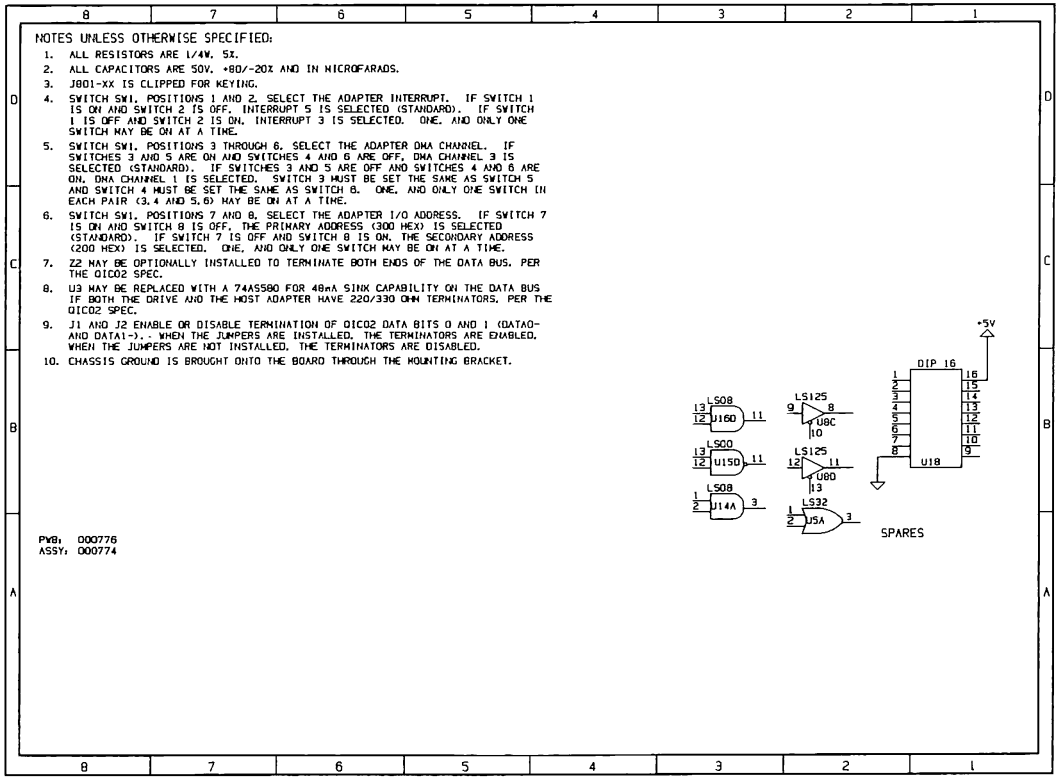


Figure 12-16. COMPAQ Tape Host Adapter Schematics (Page 1 of 4)

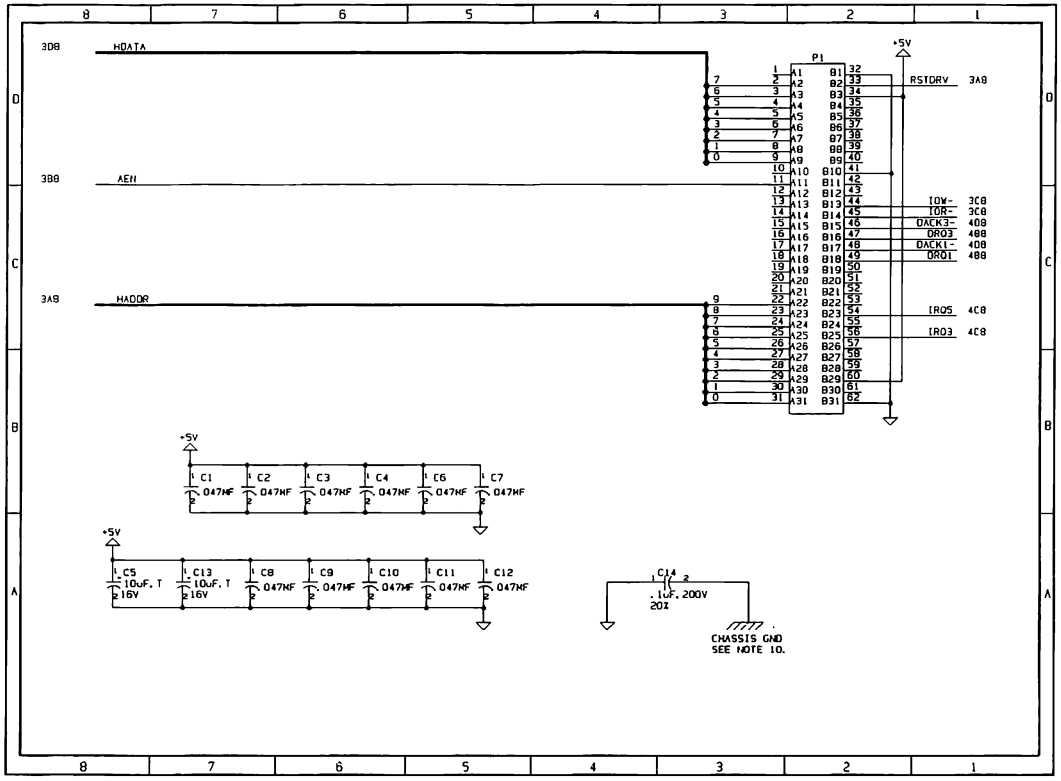


Figure 12-16. COMPAQ Tape Host Adapter Schematics (Page 2 of 4)

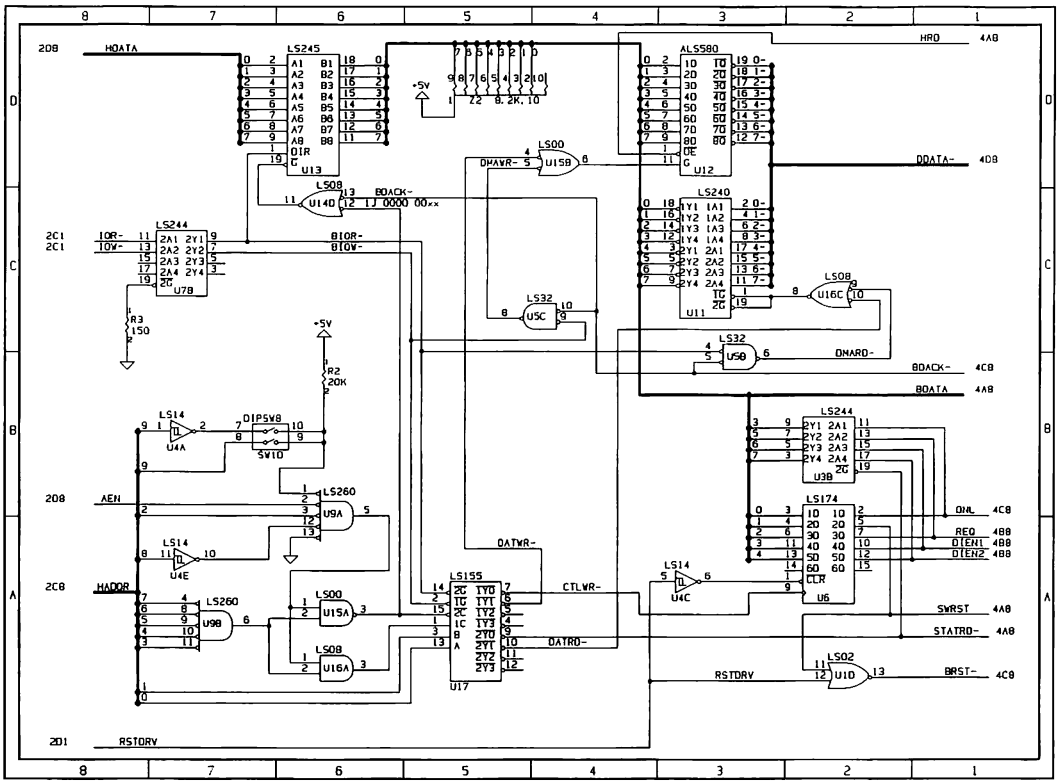


Figure 12-16. COMPAQ Tape Host Adapter Schematics (Page 3 of 4)

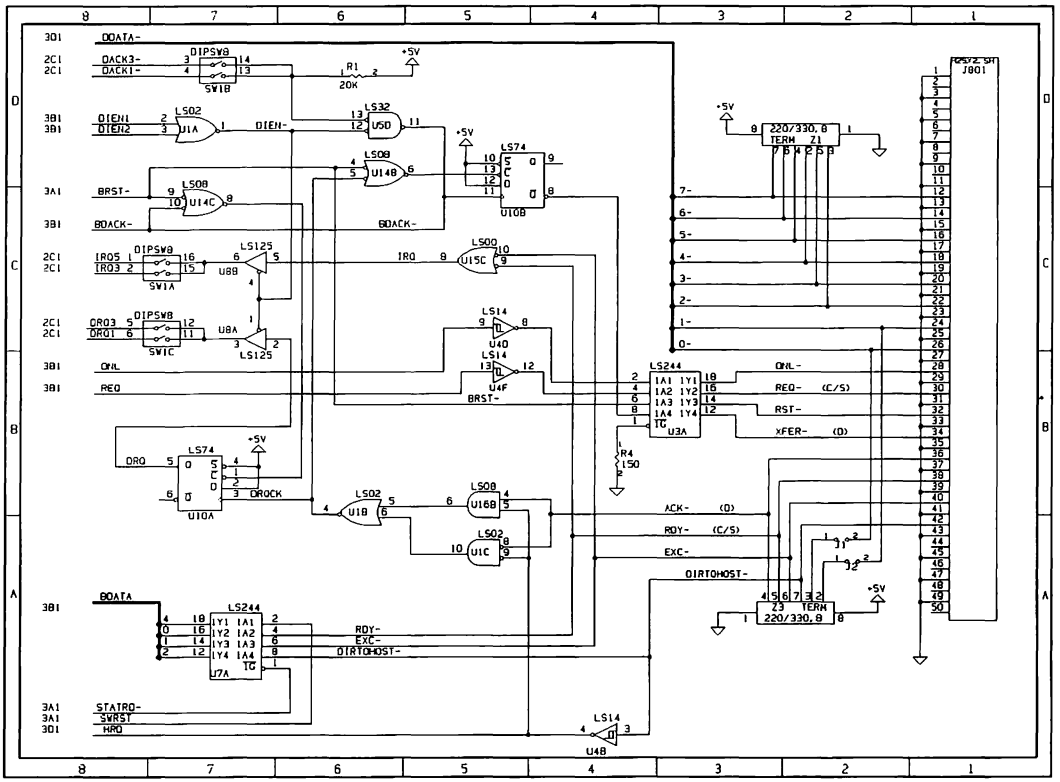


Figure 12-16. COMPAQ Tape Host Adapter Schematics (Page 4 of 4)

Chapter 13
MONITORS

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MONITORS

13.1 COMPAQ® DUAL-MODE MONITOR

COMPAQ monitors have the following features:

- Dual-mode capability
- Amber and green screen available (external monitors only)
- 12-volt DC operation

The COMPAQ Dual-Mode monitors are capable of displaying in either the high-resolution text mode or the graphics mode with the same monitor. Mode selection is accomplished via the COMPAQ Video Display Controller Board by changing the monitor scan rates. The COMPAQ Video Display Controller Board changes the scan rates in response to software interrupts (See Chapter 7) or to multiple-key commands from the keyboard (See Chapter 8).

The COMPAQ PORTABLE 286® has an internal dual-mode monitor that is internally connected to the COMPAQ Video Display Controller Board. The COMPAQ Dual-Mode Monitor is an external monitor which may be used with the COMPAQ DESKPRO 286® or, optionally, with the COMPAQ PORTABLE 286.

Figures 13-1 and 13-2 show the COMPAQ Dual-Mode Monitors.

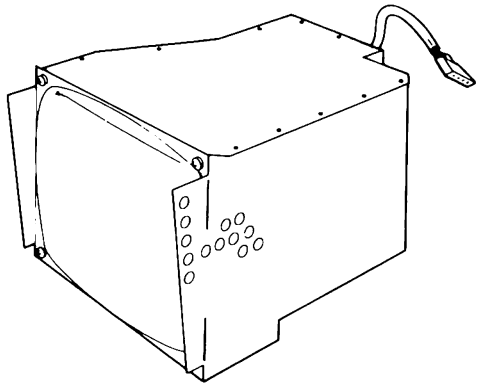

Figure 13-1. COMPAQ PORTABLE 286 Dual-Mode Monitor

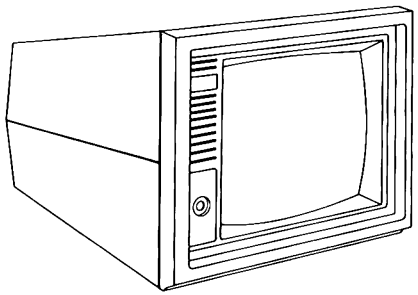

Figure 13-2. COMPAQ Dual-Mode Monitor

Figures 13-3 and 13-4 show the monitors' functional block diagrams.

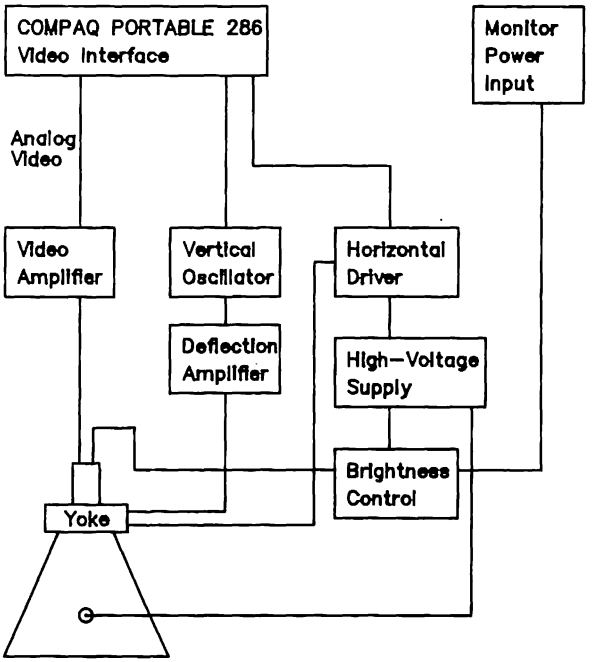

Figure 13-3. Functional Block Diagram for COMPAQ PORTABLE 286 Monitor

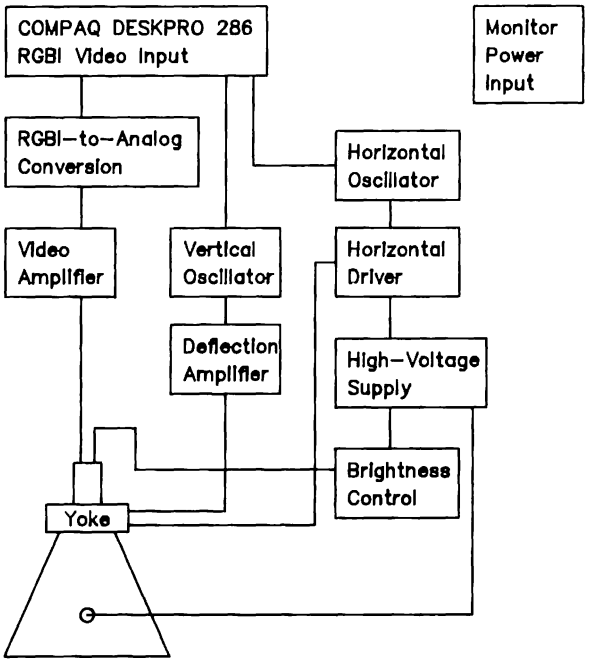

Figure 13-4. Functional Block Diagram for COMPAQ DESKPRO 286 Monitor

COMPAQ Dual-Mode Monitor Specifications

Table 13-1 lists the monitor specifications.

Table 13-1. COMPAQ Dual-Mode Monitor Specifications

	COMPAQ PORTABLE 286	COMPAQ DESKPRO 286
Screen:		
CRT size	9 in. diagonal	12 in. diagonal
Phosphor	Green, medium persistence	Green, medium persistence or Amber, medium persistence
Active area (see Figure 13-5)		
Horizontal	6.3 in. (16.0 cm)	8.1 in. (20.6 cm)
Vertical	4.6 in. (11.7 cm)	6.0 in. (15.2 cm)
Power Requirements:		
Voltage	12.3 Vdc, ±4%	12.4 Vdc, ±4%
Current	1.5 A max, 2.0 A surge (5 ms)	1.8 A max, 2.5 A surge (10 ms)
Signals:		
Video	Analog, 1.0 to 2.5 V into 470 ohms min.	Digital, TTL-level RGBI yielding a 15-level gray scale
Horizontal Sync	Positive, TTL-level	Positive, TTL-level
Vertical Sync	Negative, TTL-level	Positive, TTL-level
Connectors:		
Power	6-pin single row, AMP 102409-5, or equiv.	3-pin male circular DIN AMP 211502-5, or equiv.
Signal	12-pin double row, AMP 87227-6, or equiv.	9-pin male subminiature D

Figure 13-5 shows the active area on the screen.

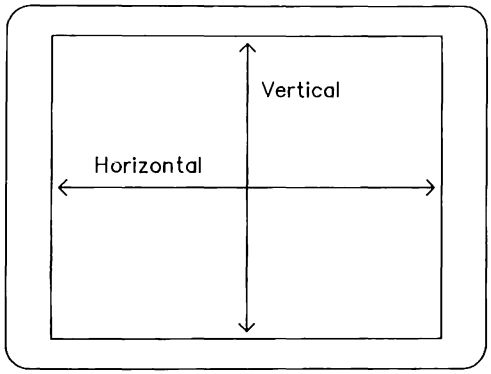

Figure 13-5. Screen Active Area

Table 13-2 lists the monitor resolution (pixel density) and frequency for the high-scan and low-scan modes.

Table 13-2. Monitor Resolution and Frequencies

Scan Mode	Mode Signal	Resolution (in pixels)	Horiz. Freq.	Vert. Freq.
High-Scan	LOW	720 x 350	18.5 KHz	50 Hz
Low-Scan	HIGH	640 x 200	15.7 KHz	60 Hz

Table 13-3 lists the Safety Compliances for the monitors.

Table 13-3. COMPAQ Dual-Mode Monitor Safety Compliances

Safety	UL 1418 UL 478 DHHS 21 CFR Subchapter J CSA 22.2 #154 VDE or TUV in accordance with DIN IEC 380/VDE 806
RFI	
U S	FCC Class B
International	VDE 0871 Level B (See Note)

Note: Units shipped internationally comply with this regulation and include COMPAQ part numbers 102508-3, green phosphor, international and 102508-4, amber phosphor, international.

COMPAQ Dual-Mode Monitor Waveforms

References to the red, green, blue, and intensity signals in the COMPAQ Video Display Controller Board translate to variations in intensity on COMPAQ monochrome monitors by assigning a weighted value to each signal. Figures 13-6 through 13-8 show the timing parameters for the monitors.

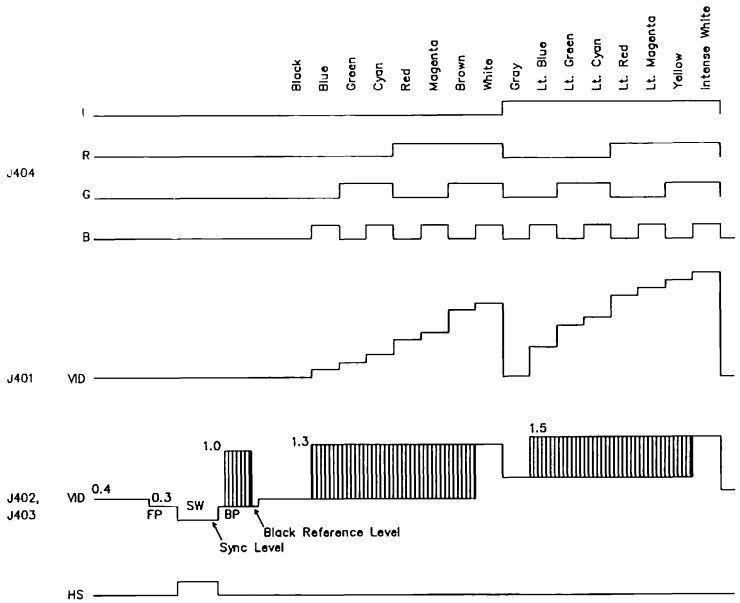

Figure 13-6. COMPAQ Dual-Mode Monitor Video Timing Waveforms

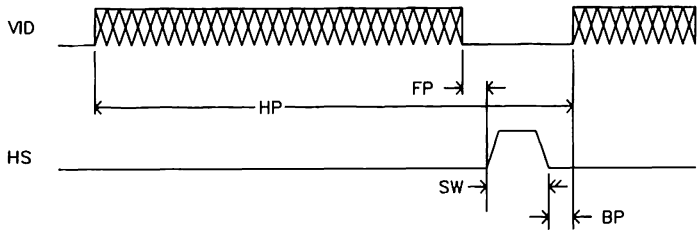

Figure 13-7. COMPAQ Dual-Mode Monitor Horizontal Timing

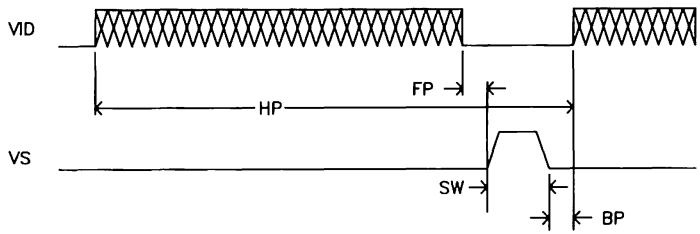

Figure 13-8. COMPAQ Dual-Mode Monitor Vertical Timing

COMPAQ Dual-Mode Monitor Connectors

The COMPAQ PORTABLE 286 Dual-Mode Monitor signal cable connects to the COMPAQ Video Display Controller Board connector J401 (connector J401 is an internal connector). The COMPAQ PORTABLE 286 monitor-power cable connects to the system board connector J112. Figure 13-9 and Table 13-4 describe the monitor signal connector. Figure 13-10 shows the monitor power connector.

The COMPAQ Dual-Mode Monitor signal cable connects to the COMPAQ Video Display Controller Board RGBI connector (J404). The COMPAQ Dual-Mode Monitor power cable connects to the monitor power receptacle. These connectors are on the back of the system unit. Figure 13-11 and Table 13-5 describe the monitor signal connector. Figure 13-12 shows the monitor power connector.

Table 13-4. COMPAQ PORTABLE 286 Monitor Signal Connector

Signal	Pin	I/O	Description
Chassis ground	11,12	-	Cable Shield.
HS	7	I	Horizontal sync is an active-high TTL signal in both level and drive characteristics. Refer to the Waveforms section for the horizontal sync signal timing characteristics.
MODE	3	I	The mode signal (TTL) indicates whether the monitor should be in the high- or low-scan mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The mode signal is high (logic 1), for the low-scan mode, and low (logic 0) for the high-scan mode.
Signal ground	2,4,8	-	This is the ground reference for the TTL signals.
VID	5	I	This is the analog video output signal. The signal voltage ranges from 1.0 volts (black) to 2.5 volts (white) into 470 to 6800 ohms (impedance). This signal is referenced to the video signal ground (pin 6).
Video ground	6	-	This is the ground reference for the VID signal (pin 5).
VS-	1	I	Vertical sync is an active-low TTL signal in both level and drive characteristics. Refer to the Waveforms section for the vertical sync signal timing characteristics.

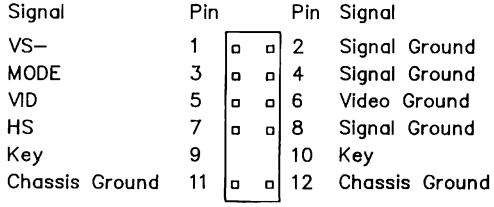

Figure 13-9. COMPAQ PORTABLE 286 Dual-Mode Monitor Signal Connector

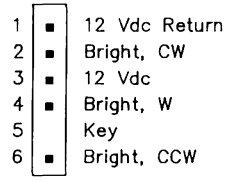

Figure 13-10. COMPAQ PORTABLE 286 Dual-Mode Monitor Power Connector

Table 13-5. COMPAQ Dual-Mode Monitor Signal Connector

Signal	Pin	I/O	Description
B	5	I	Blue, active-high TTL video signal.
G	4	I	Green, active-high TTL video signal.
HS	8	I	Horizontal sync is an active-high TTL signal in both level and drive characteristics. Refer to the waveform section for the timing characteristics.
I	6	I	Intensity, active-high TTL video signal
MODE	7	I	The mode signal controls the monitor high- or low-scan mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The mode signal is high for the low-scan mode and low for the high-scan mode.
R	3	I	Red, active-high TTL video signal.
Signal Ground	1,2	-	TTL signal reference.
VS	9	I	Vertical sync is an active high TTL signal in both level and drive characteristics. Refer to the waveform section for the timing characteristics.

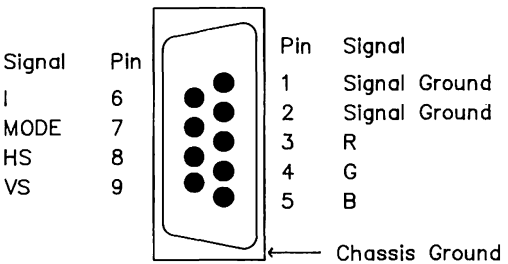

Figure 13-11. COMPAQ Dual-Mode Monitor Signal Connector

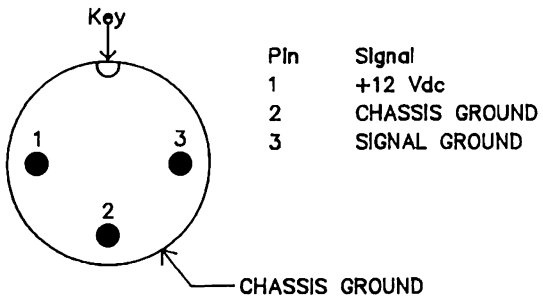

Figure 13-12. COMPAQ Dual-Mode Monitor Power Connector

13.2 OTHER COMPAQ MONITORS

COMPAQ monitors other than the COMPAQ Dual-Mode Monitor each have individual technical reference guides. To obtain these manuals, contact your Authorized COMPAQ Computer Dealer.

Chapter 14

BIOS PROGRAMMING GUIDE

Chapter 15

300-/600-MEGABYTE FIXED DISK DRIVE EXPANSION UNIT

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CHAPTER 15
COMPAQ 300-/600-MEGABYTE FIXED DISK DRIVE EXPANSION UNIT

Addendum 114271-001 (12-88)
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15.4 SOFTWARE CONSIDERATIONS (CONTINUED)

Chapter 15
COMPAQ 300-/600-MEGABYTE FIXED DISK DRIVE EXPANSION UNIT

Addendum 114271-001 (12-88)
To Manual No. 102789-001

15.1 INTRODUCTION

The COMPAQ 300-/600-Megabyte Fixed Disk Drive Expansion Unit is an option available for the 12-MHz DESKPRO 286 Personal Computer. This option provides greatly expanded mass storage to meet the needs of advanced applications, mainframe communications, multi-user systems, and networking activities.

Figure 15-1 shows the fixed disk drive expansion unit and Figure 15-2 shows a block diagram of this expansion system.

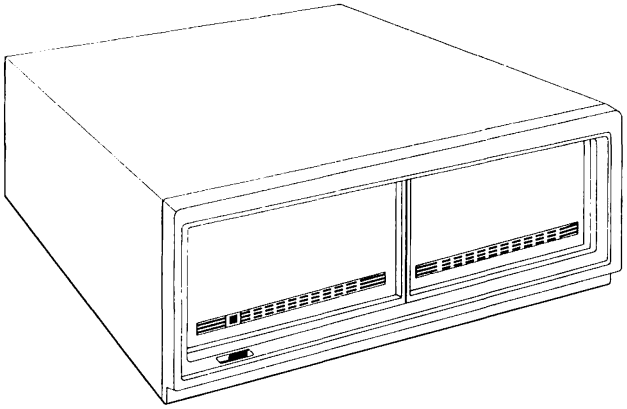

Figure 15-1. COMPAQ 300-/600-Megabyte Fixed Disk Drive Expansion Unit

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As shown below the expansion unit comes with an external ESDI interface adapter board and an external ESDI controller board.

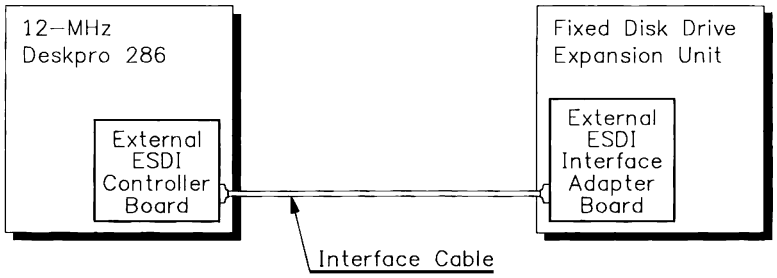

Figure 15-2. COMPAQ Fixed Disk Drive Expansion Unit System Block Diagram

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15.2 FEATURES

The expansion unit holds one standard and one optional COMPAQ 300-Megabyte Fixed Disk Drive. A total of two expansion units may be used with the 80286-Based Personal Computer.

The 300-megabyte fixed disk drives are controlled by the COMPAQ 1:1 interleave buffered ESDI External Fixed Disk Drive Controller. Data retrieval time is reduced by a forward reading buffer and 1:1 interleave. Data-transfer rate is 10 Mb/s.

Performance is also enhanced with MS DOS Version 3.3, as published by Compaq Computer Corporation. It enables each 300-megabyte fixed disk drive to be formatted as a single logical drive, providing the capability to create or download files up to the total capacity of the fixed disk drive.

1.2 Gigabytes Maximum Storage Capacity

Two expansion units, each holding two 300-megabyte fixed disk drives, may be combined to offer a total of 1.2 gigabytes of mass storage.

LAN Fault Tolerant Configuration

The expansion unit offers an ideal platform for specialized software design to address the high fault tolerance requirements of LAN (Local Area Network) operation. Two configurations that address those requirements are referred to as disk mirroring and disk duplexing. Disk mirroring and disk duplexing provide integrity of data on two fixed disk drives with duplicate read and write actions. These configurations also provide quicker read response time, since the first drive to access the data provides the read.

Disk Mirroring

In disk mirroring, two identical fixed disk drives use the same ESDI controller. Mirroring ensures that data integrity is maintained; should a data fault occur on the primary fixed disk drive, the system can continue to function using the secondary fixed disk drive and the data duplicated there.

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Disk Duplexing

Disk duplexing, therefore, provides the highest degree of fault tolerance and system reliability, as well as increased performance in write operations. Disk duplexing requires two fixed disk drive controllers and two identical fixed disk drives.

15.3 HARDWARE CONSIDERATIONS

The COMPAQ 300-/600-Megabyte Fixed Disk Drive Expansion Unit comes with an external ESDI controller board and an external ESDI interface adapter board.

External ESDI Controller Board

The ESDI controller board, which fits in an expansion slot of the personal computer, is required when using one or two 300-megabyte fixed disk drives mounted in an expansion unit. Figure 15-3 shows a block diagram of the ESDI controller board.

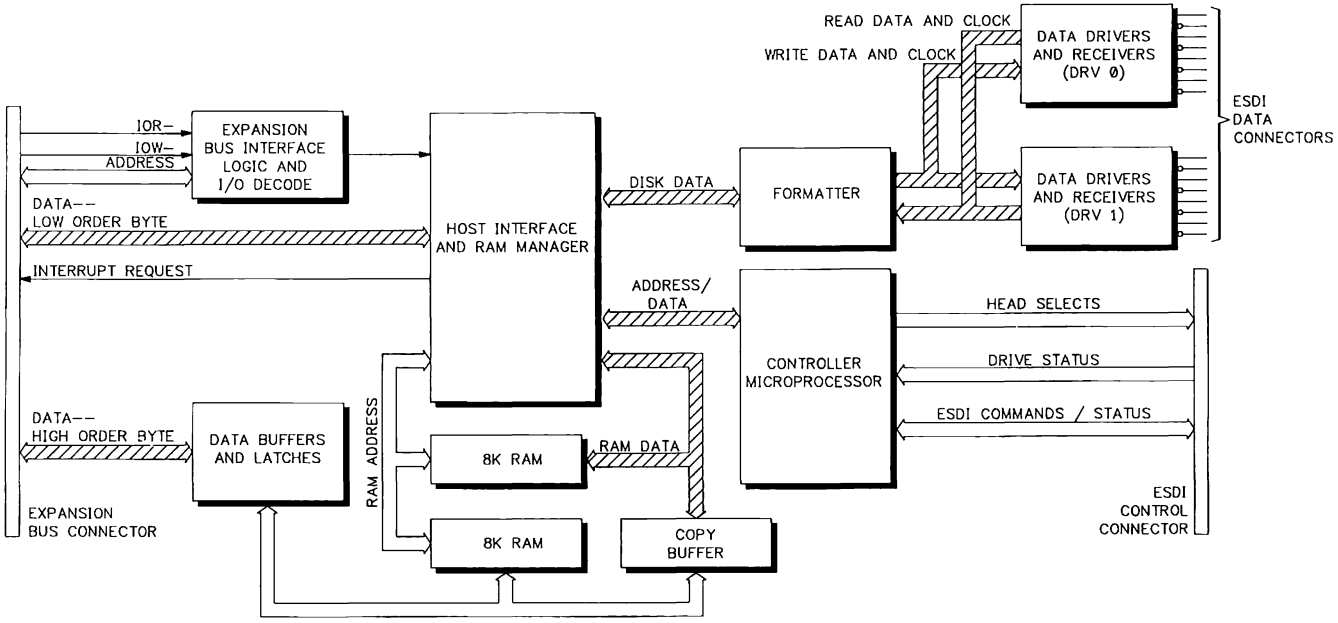

Figure 15-3. External ESDI Controller Board Functional Block Diagram

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The external ESDI controller board conforms to the ESDI standard of signal, connector, and command protocols, and includes the following features:

- 1:1 interleave with 16-Kbyte buffer
- 56-bit Error Correction Code (ECC) polynomial for error detection and correction
- On-board diagnostics

The external ESDI controller board supports all commands and uses the same registers discussed in Chapter 6. The Write Precompensation Cylinder register (I/O address 1F1h) is reserved, however, since write precompensation is not programmable on the ESDI controller. An additional register unique to the external ESDI board is described in Section 15.4.

The external ESDI controller board uses one of two addresses (primary or secondary) available to the DESKPRO 286 CPU for fixed disk drive operation. The external ESDI controller board can be configured for either address (refer to Section 15.6).

Table 15-1 shows the possible configurations and fixed disk drive board requirements for 286-based products.

Table 15-1. Fixed Disk Drive Controller Board Requirements For 300-Megabyte Fixed Disk Drives

Configuration	Fixed Disk Drive Controller Board Required
External 300 MB	1 ESDI board
External 600 MB	1 ESDI board
External 900 MB or 1200 MB (two expansion units)	2 ESDI boards

NOTES 1. Expansion unit not used.
2. With two external ESDI controller boards installed, Winchester Controller on FSPW board must be disabled (FSPW switch SW500-3 in ON position).

Since only two I/O addresses are available to the CPU for fixed disk drive operation, no more than two fixed disk drive controllers can be active in the personal computer, with each controller configured for a different address (refer to note 2 in Table 15-1).

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External ESDI Interface Adapter Board

The 300-/600-Megabyte Fixed Disk Drive Expansion Unit comes with the expansion interface adapter board installed. This board provides an interface between the one or two 300-megabyte fixed disk drive(s) in the expansion unit and the external ESDI controller board mounted in the PC. Figure 15-4 shows a functional block diagram of the expansion interface adapter circuitry.

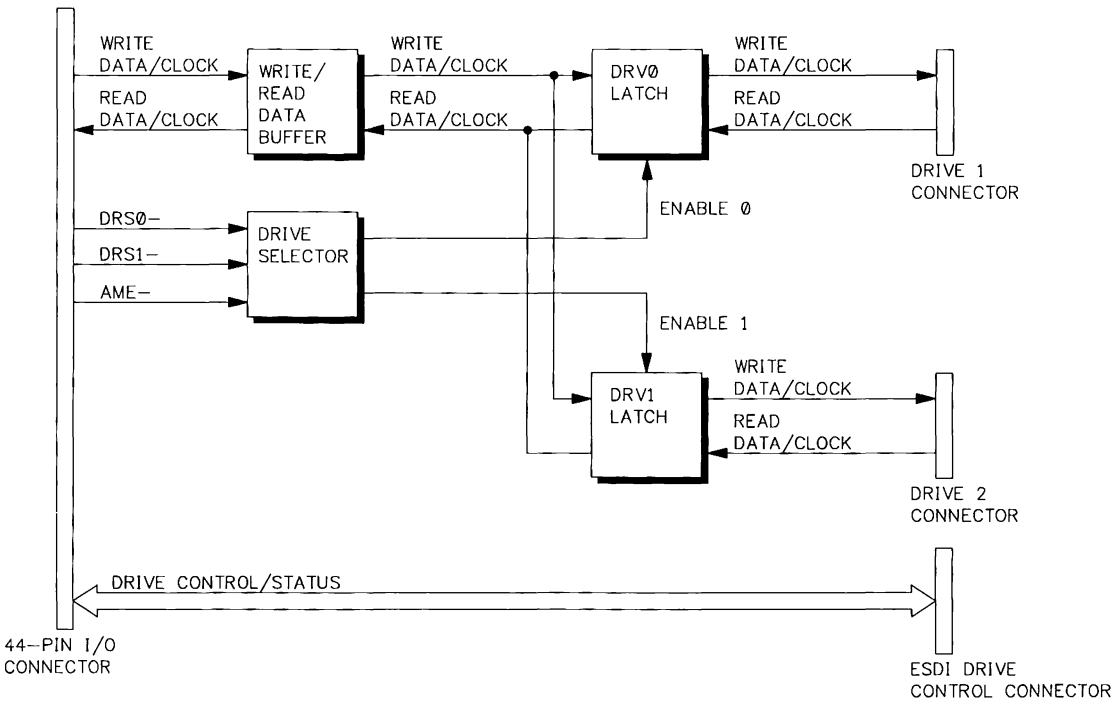

Figure 15-4. External ESDI Interface Adapter Board Functional Block Diagram

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15.4 SOFTWARE CONSIDERATIONS

NOTE: The 300-/600-megabyte fixed disk drive expansion unit requires that the 12-MHz DESKPRO 286 either have system ROM revision P.1G (or later) installed, or uses the MS-DOS driver EXTDISK.SYS. The system ROM revision level can be determined by using the ROMREV program on the DIAGNOSTICS diskette.

The expansion unit requires that the current system ROM INT 13h Fixed Disk Drive I/O interface allow support of a fixed disk drive controller set to alternate address (170h-177h). The MS-DOS driver EXTDISK.SYS provides this support for older system ROM revisions.

To determine if INT 13h support for the alternate fixed disk drive adapter is present, execute an INT 13h with AH = 08h (Get Drive Parameters) and DL = 82h. If support is present, then the carry flag is not set on return (CF = NC), otherwise the carry flag is set (CF = CY).

To determine the number of fixed disk drives supported by INT 13h, calling INT 13h with AH = 08h and DL = 80h will return the number of drives on the primary fixed disk drive adapter in DL (0...2). In addition, calling INT 13h with AH = 08h and DL = 82h will return the number of drives on the alternate fixed disk drive adapter in DL (0...2). Drives on the primary adapter are accessed as 80h and 81h. Drives on the secondary are accessed as 82h and 83h. If one fixed disk drive is on the primary adapter and one fixed disk drive on the alternate adapter, then drives 80h and 82h are present.

Functions AH = 88h, Get Pointer to Fixed Disk Drive Parameter Table, and AH = 89h, Set Pointer to Fixed Disk Drive Parameter Table, provide access to the Fixed Disk Drive Parameter Tables for drives 82h and 83h much like INT 41h and INT 46h provide pointers to the Fixed Disk Drive Parameter Tables for drives 80h and 81h.

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INT 13h Fixed Disk Drive I/O Changes

For all INT 13h I/O, drives 82h and 83h will access drives 0 and 1 of the alternate fixed disk drive adapter. If the requested drive is not 82h or 83h, control is passed to the old INT 13h handler.

INT 13h, AH = 00h - Reset

If DL is 82h or 83h on entry, the alternate and the primary fixed disk drive controllers are reset. If DL is 80h or 81h, the primary fixed disk drive controller is reset, but the alternate fixed disk drive controller is not.

INT 13h, AH = 02h, 03h, 04h, 05h - Read Sectors/Write Sectors/Verify Sectors/Format Track

There is no change except that drives 82h and 83h access the fixed disk drives on the alternate fixed disk drive controller.

INT 13h, AH = 08h - Get Drive Parameters

If DL is 80h or 81h on entry, Get Drive Parameters will return in DL, the number of drives on the primary fixed disk drive controller. The number of fixed disk drives on the alternate fixed disk drive controller will be returned if DL is 82h or 83h on entry.

INT 13h, AH = 09h - Set Drive Parameters

There is no change except that drives 82h and 83h set the drive parameters for the fixed disk drives on the alternate fixed disk drive controller.

INT 13h, AH = 0Ah, 0Bh - Read Long/Write Long

There is no change except that drives 82h and 83h access the fixed disk drives on the alternate fixed disk drive controller.

INT 13h, AH = 0Ch - Seek Cylinder

There is no change except that drives 82h and 83h access the fixed disk drives on the alternate fixed disk drive controller.

INT 13h, AH = 0Dh - Alternate Disk Reset

There is no change except that drives 82h and 83h cause the alternate fixed disk drive controller to be reset.

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INT 13h, AH = 0Eh, 0Fh - Reserved

INT 13h, AH = 10h, 11h - Test Drive Ready/Recalibrate Drive

There is no change except that drives 82h and 83h access the fixed disk drives on the alternate fixed disk drive controller.

INT 13h, AH = 12h, 13h - Reserved

INT 13h, AH = 14h - Controller Diagnostic

There is no change except that drives 82h and 83h will cause the controller diagnostic to be performed on the alternate fixed disk drive controller.

INT 13h, AH = 15h - Get Type of Drive

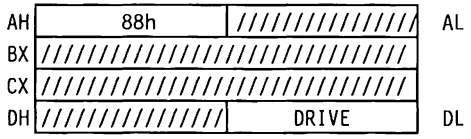
There is no change except that drives 82h and 83h return the drive type and capacity (in sectors) for the fixed disk drives on the alternate controller.

New INT 13h Fixed Disk Drive I/O Calls

INT 13h, AH = 88h - Get Pointer to Fixed Disk Drive Parameter Table and Drive Count

Returns a pointer to ES:BX to the fixed disk drive parameter table for drive 82h or 83h, the number of fixed disk drives on the alternate fixed disk drive adapter in AL, and the hardware interrupt number (11, 12, 14, or 15) in CL.

INPUT:



Where DL = 82h or 83h

OUTPUT: CL = IRQ (11, 12, 14, or 15)

AH	88h	# DRIVES	AL
BX	OFFSET OF POINTER		
CH	////////////////	CNTLR INT	CL
DX	////////////////	DRIVE	

ES	SEGMENT OF POINTER

All other registers are preserved.

If INT 13h support is not present for drives 82h and 83h, then AH is set to 01h (bad command) and the carry flag is set to CY on return. The drive count returned in AL is the number of drives sensed during the power-on self-test routines.

INT 13h AH = 89h - Set Pointer To Fixed Disk Drive Parameter Table and Drive Count

Sets the pointer from ES:BX to the Fixed Disk Drive Parameter Table for drive 82h or 83h and the number of fixed disk drives on the alternate fixed disk drive adapter.

INPUT:

AH	89h	# DRIVES	AL
BX	OFFSET OF POINTER		
CX	////////////////////////////////		
DX	////////////////	DRIVE	DL

ES	SEGMENT OF POINTER

Where DL = 82h or 83h

OUTPUT:

AH	89h	# DRIVES	AL
BX	OFFSET OF POINTER		
CX	////////////////////////////////		
DX	////////////////	DRIVE	DL

ES	SEGMENT OF POINTER

All registers are preserved. The drive count being set by AL is analogous to setting the primary fixed disk drive adapter count at 40:75.

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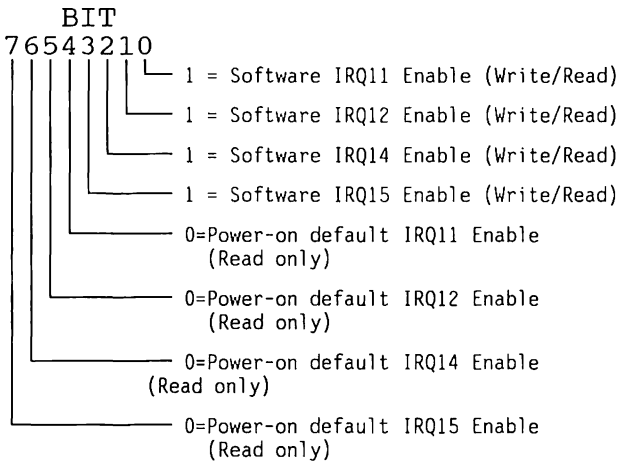
Interrupt Support

The interrupt for the fixed disk drive controller shipped with an expansion unit can be selected with a switch located on the external ESDI controller board. In addition, the interrupt can be changed via software. The INT 13h of EXTDISK.SYS will use the interrupt selected by the ESDI switch settings (refer to Section 15.6). If IRQ14 is selected, additional overhead in INT 13h will be incurred because the primary fixed disk drive controller must be disabled before an interrupt from the alternate fixed disk drive adapter can occur.

The ESDI Interrupt configuration register (address 11F1h) determines interrupt control of the ESDI fixed disk drive controller. This register enables one of four interrupts that are hardware/software selectable.

The bits in this register are as follows:



At power-on, the settings of switch SW500 (Table 15-5) are used by register bits four through seven to select the interrupt enable. The first write to the register, however, overrides the switch SW500 settings, and the value written into bits zero through three is then used to select the interrupt enable.

A read to this register will yield either the power-on default setting if a write has not yet occured, or the software setting if a write has occured.

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CMOS RAM Bytes 1Bh and 1Ch

CMOS RAM bytes 1Bh and 1Ch are used to contain the fixed disk drive types for drives 82h and 83h respectively. If CMOS RAM byte 1Bh is 00h, drive 82h is assumed to be not present; if CMOS RAM byte 1Ch is 00h, drive 83h is assumed to be not present.

15.5 CONNECTORS

Connectors for the expansion unit are located on two separate boards, the external ESDI interface adapter board and the external ESDI controller board. The external ESDI interface adapter board is mounted in the expansion unit. The external ESDI controller board is mounted inside the 12-MHz DESKPRO 286 Personal Computer. (See Figures 15-5, 15-6, and 15-7.)

The connectors mounted on the external ESDI interface adapter board are identical to those found on the ESDI portion of the FPSE controller board used to control internally mounted 300-megabyte fixed disk drives.

The external ESDI controller is connected to the expansion unit by means of a multiconductor cable via the 44-pin expansion interface connector.

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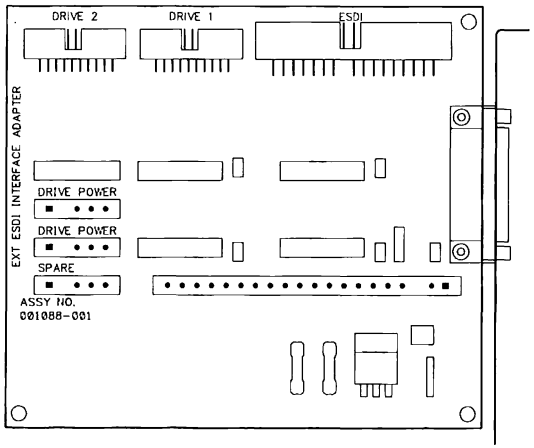

Figure 15-5. External ESDI Interface Adapter Board

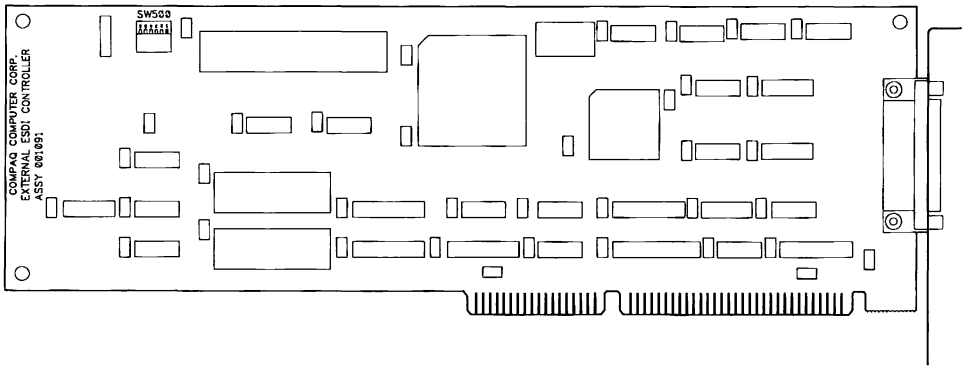

Figure 15-6. External ESDI Controller Board

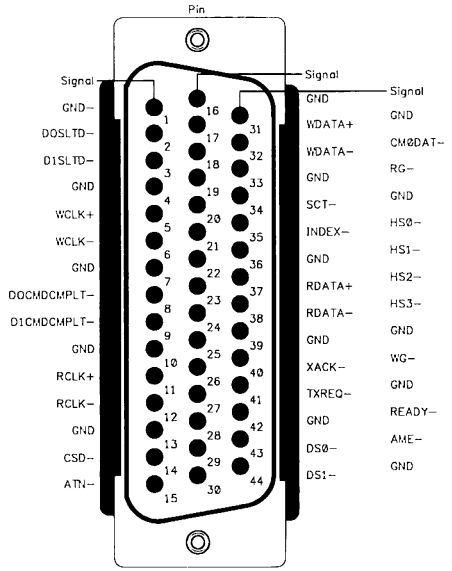

Figure 15-7. 44-Pin Expansion Unit Interface Cable Connector

Table 15-2 contains the pin descriptions and signal functions for this connector.

Table 15-2. 44-Pin Expansion Cable Signal Description

Signal	Pin	I/O	Description
DOSLTD-	2	I	Lines that indicate the drive currently selected
D1SLTD-	3	I	
WCLK+	5	O	A differential clock pair used for writing
WCLK-	6	O	data bits to the drive
DOCMDCMPLT-	8	I	Status lines that indicate command completion from
D1CMDCMPLT-	9	I	a drive to the controller
RCLK+	11	I	A differential clock signal used for reading
RCLK-	12	I	data bits from a drive
CSD-	14	I	Configuration/Status Data (serial) present on this line from a drive, at the request of the controller
ATN-	15	I	A signal from a drive indicating the drive wishes the controller to request its status
WDATA+	17	O	A differential pair that defines the data to be written
WDATA-	18	O	to the drive

NOTE: I/O direction is defined using the controller as the signal source; therefore, INPUT or OUTPUT is to or from the controller respectively.

(Continued)

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Table 15-2. (Continued)

Signal	Pin	I/O	Description
SCT-	20	I	Signal that indicates the beginning of a sector
INDEX-	21	I	Signal that indicates the beginning of a track
RDATA+	23	I	Data recovered by reading previous written information is transmitted to the controller via this differential pair
RDATA-	24	I	
XACK-	26	I	Line from a drive indicating that a TXREQ- has been acknowledged and valid data transferred. All transfers handshake with TXREQ- and XACK-
TXREQ-	27	O	Line from the controller requesting that one bit of data be transferred from the drive to the controller. All transfers handshake with TXREQ- and XACK-
DS0-	29	O	These bits provide the binary coded drive select address
DS1-	30	O	

NOTE: I/O direction is defined using the controller as the signal source; therefore, INPUT or OUTPUT is to or from the controller respectively.

(Continued)

Table 15-2. (Continued)

Signal	Pin	I/O	Description
CMDDAT-	32	O	When a command is issued to the drive, 16 information bits of serial data, plus parity, are sent to the drive via this line
RG-	33	O	Signal that allows data to be read from the disk (READ GATE)
HS0-	35	O	Lines that allow selecting individual read/write heads in a binary code sequence
HS1-	36	O	
HS2-	37	O	
HS3-	38	O	
WG-	40	O	Signal that allows data to be written to a disk (WRITE GATE)
READY-	42	I	Signal from a drive that the spindle is up to speed
AME-	43	O	The trailing edge of this signal, with the WRITE GATE- asserted, initiates writing the sync field on the drive
GND-	1, 4, 7, 10, 13,16, 19, 22, 25,28, 31, 34, 39,41, 44.		Signal Return

NOTE: I/O direction is defined using the controller as the signal source; therefore, INPUT or OUTPUT is to or from the controller respectively.

Figure 15-8 shows the ESDI connector on the External Interface Adapter board.

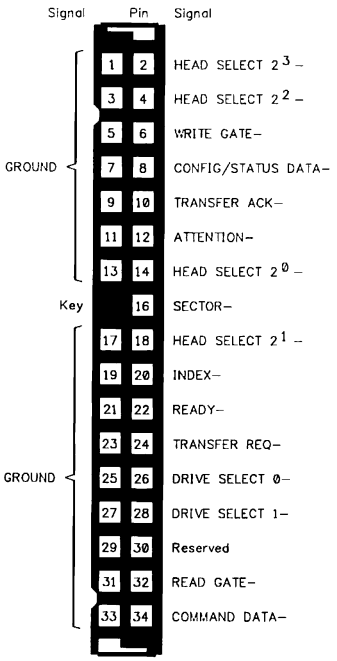

Figure 15-8. ESDI (Drive Control) Cable Connector

Table 15-3 shows the pin/signal descriptions for this connector. All I/O designations are with respect to the drive.

Table 15-3. 34-Pin ESDI Connector Signal Description

Signal	Pin (note)	I/O	Description
HEAD SELECT 23-	2	I	Lines that allow selecting individual read/write heads in a binary code sequence
22-	4	I	
20-	14	I	
21-	18	I	
WRITE CATE-	6	I	Allows data to be written on the disk
CONFIG/ STATUS DATA-	8	O	Serial data received in a 16-bit plus parity format from controller.
TRANSFER ACK-	10	O	Line from the drive indicating that a transfer request has been acknowledged and valid data transferred. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-
ATTENTION-	12	O	Signal from the drive indicating the drive wants the controller to request its stauts
SECTOR-	16	O	Indicates the beginning of a sector
INDEX-	20	O	Indicates the beginning of a track

NOTE: All odd numbered pins are ground.

(Continued)

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Table 15-3. (Continued)

Signal	Pin (note)	I/O	Description
READY-	22	O	Signal indicates only that the spindle is up to speed
TRANSFER REQ-	24	I	Line from the controller requesting that one bit of data be sent between the drive and the controller. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-.
DRIVE SELECT 1- DRIVE SELECT 2-	26 28	I I	These bits provide the binary-coded drive select address.
READ GATE-	32	I	Signal allows data to be read from the disk
COMMAND DATA	34	I	A command issued in a serial 16-bit plus parity format.
RESERVED	30		

NOTE: All odd numbered pins are ground.

Figure 15-9 shows the drive (1 or 2) connector on the External Interface Adapter board.

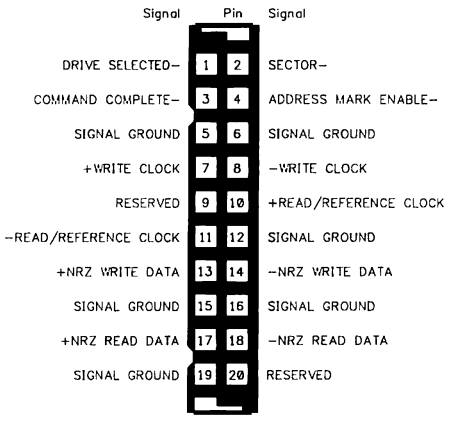

Figure 15-9. DRIVE 1/DRIVE 2 Data Cable Connector

Table 15-4 shows the pin/signal descriptions for this connector. All I/O designations are with respect to the drive.

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Table 15-4. DRIVE 1/DRIVE 2 Data Cable Connector Signal Descriptions

Signal	Pin	I/O	Description
DRIVE SELECTED-	1	O	A status line provided to inform the controller system of the selection status of the drive
SECTOR-	2	O	Indicates the beginning of sector
COMMAND COMPLETE-	3	O	A status line that indicates command completion to the controller
ADDRESS MARK ENABLE-	4	O	The trailing edge of this signal with the WRITE GATE- asserted initiates writing the sync field on the drive.
+READ/ REFERENCE CLOCK	10	O	Differential clock signal used for reading data bits from the drive.
-READ/ REFERENCE CLOCK	11	O	
+NRZ WRITE DATA	13	I	A differential pair that defines the data to be written on the track
-NRZ WRITE DATA	14	I	
+NRZ READ DATA	17	O	Data recovered by reading previously written information is transmitted to the controller via this this differential pair.
-NRZ READ DATA	18	O	
+WRITE CLOCK	7	I	A differential pair of clocks used for writing data bits to the drive.
-WRITE CLOCK	8	I	
GROUND	5, 6, 12, 15, 16, 19		Signal returns

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15.6 SWITCHES

The external ESDI controller board and the FPSE controller board located in the 12-MHz DESKPRO 286 Personal Computer have switches which allow configuring the expansion unit. Switch positions and functions for switch SW500 of the FPSE controller board are shown in Chapter 6, Table 6-8.

The location of switch SW500 on the external ESDI controller board is shown in Figure 15-6.

Switch settings for the external ESDI controller are listed in Table 15-5. There are no switches or jumpers on the expansion interface board.

Table 15-5. External ESDI Controller Board Switch SW500 Description

Switch Number	Function
1 (note 1)	Controller Address SW500-1 = OFF, Primary Address SW500-1 = ON, Secondary Address
2 & 3 (note 2)	Power-On Default Interrupt SW500-2 = ON, -3 = ON, IRQ11 SW500-2 = OFF, -3 = ON, IRQ12 SW500-2 = ON, -3 = OFF, IRQ14 SW500-2 = OFF, -3 = OFF, IRQ15

NOTES: 1. When using two fixed disk drive controller boards, each board should be configured to a different address.
2. The interrupt determined by these switch settings can be overridden by writing to the ESDI Interrupt Configuration register on the controller board.

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15.7 SCHEMATICS

The schematics for the external ESDI interface adapter board are shown in Figure 15-10 and the schematics for the external ESDI controller board are shown in Figure 15-11.

Compaq Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the operation of the controller boards.

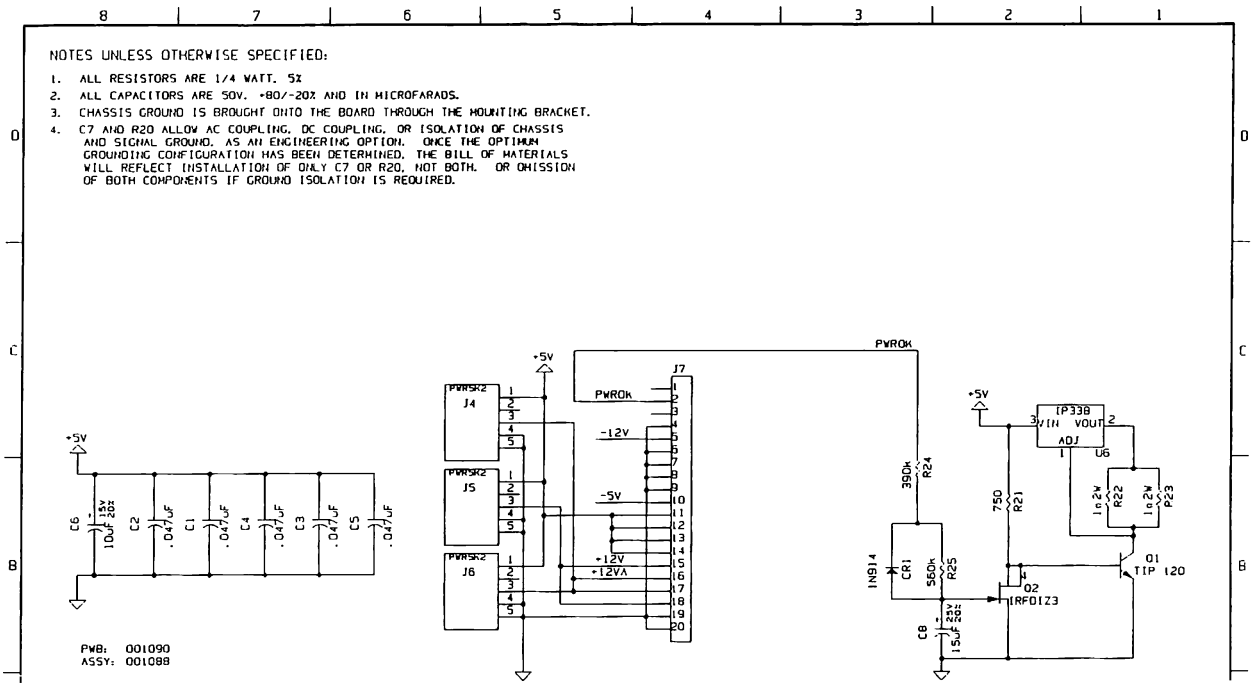

Figure 15-10. Schematic of the External ESDI Interface Adapter Board (Page 1 of 2)

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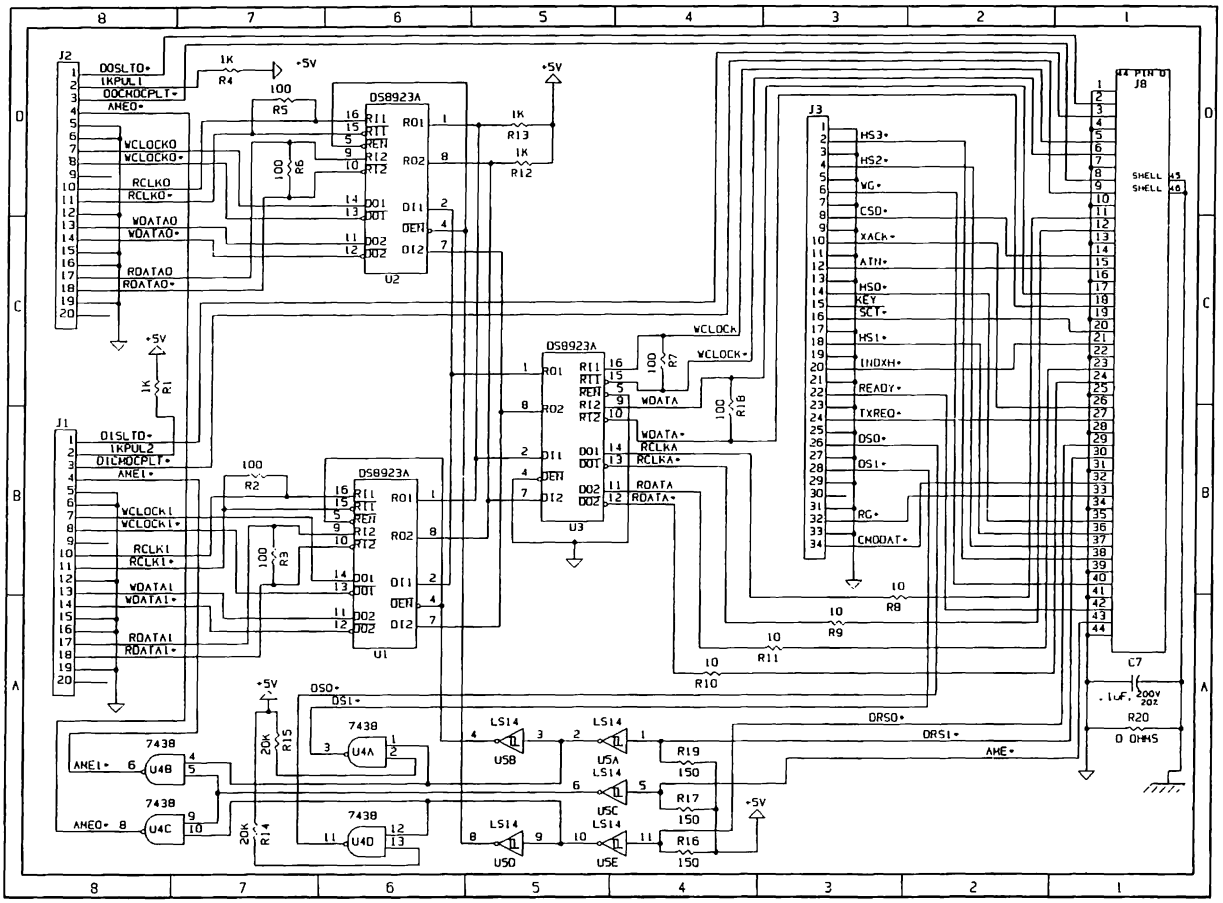

Figure 15-10. Schematic of the External ESDI Interface Adapter Board (Page 2 of 2)

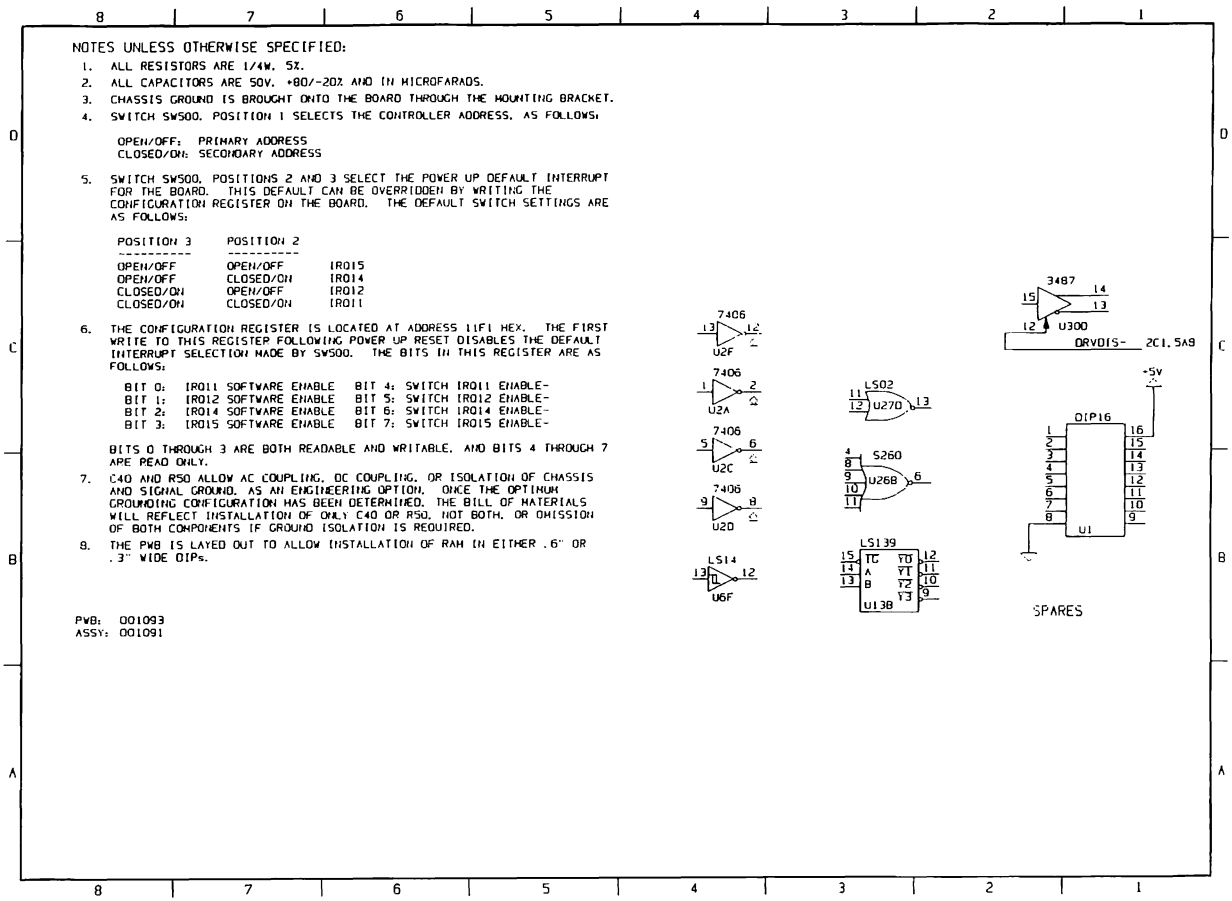

Figure 15-11. Schematic of the External ESDI Controller Board (Page 1 of 5)

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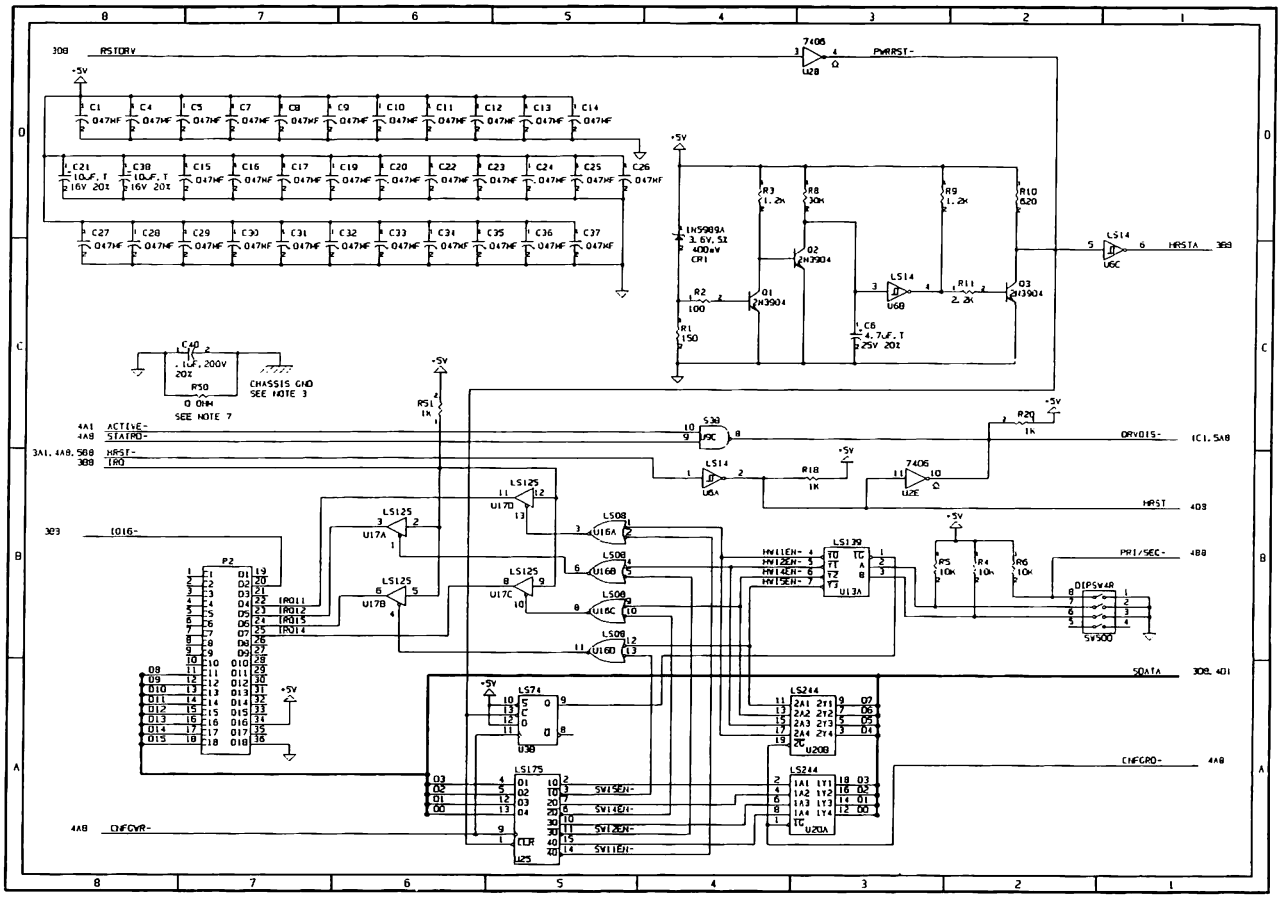

Figure 15-11. Schematic of the External ESDI Controller Board (Page 2 of 5)

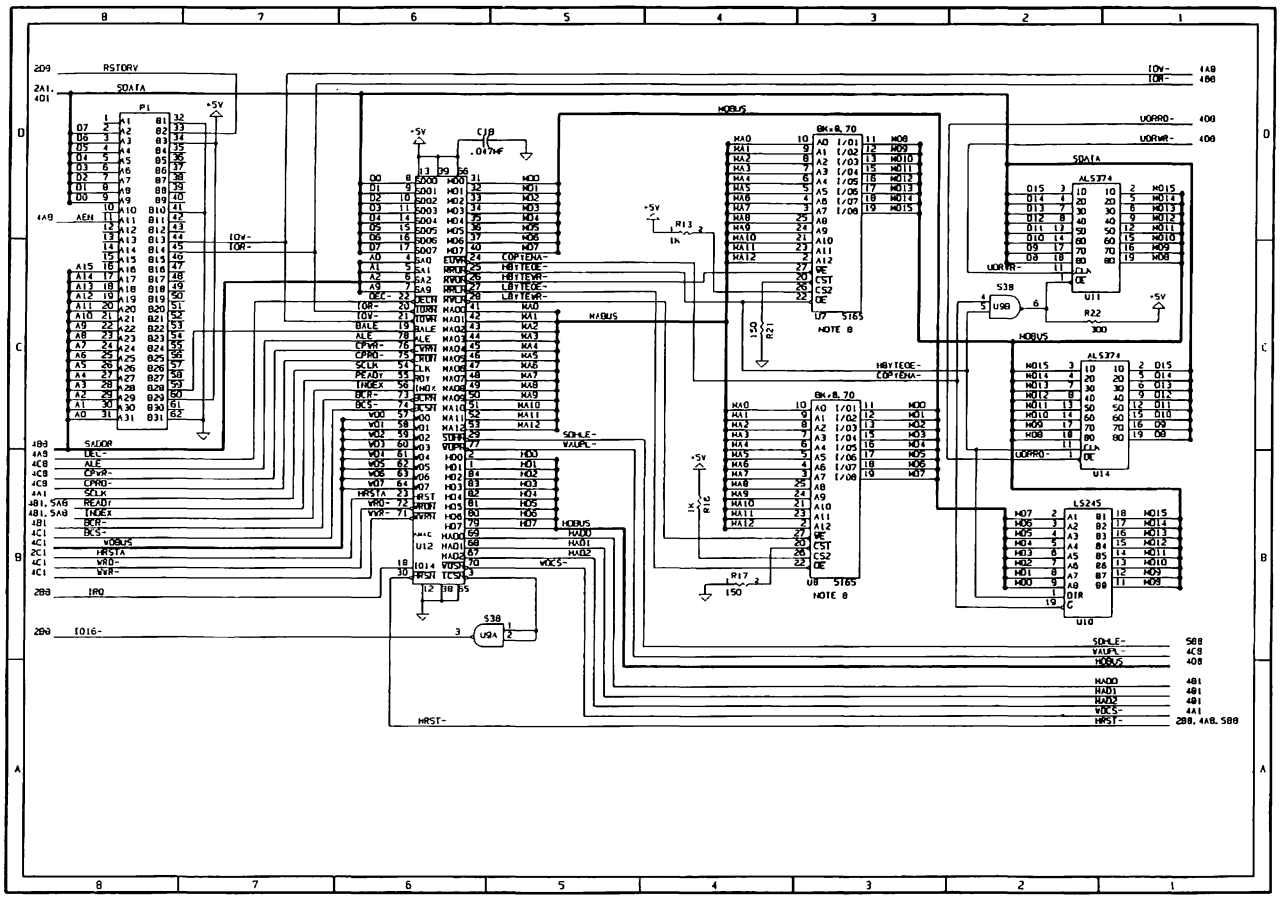

Figure 15-11. Schematic of the External ESDI Controller Board (Page 3 of 5)

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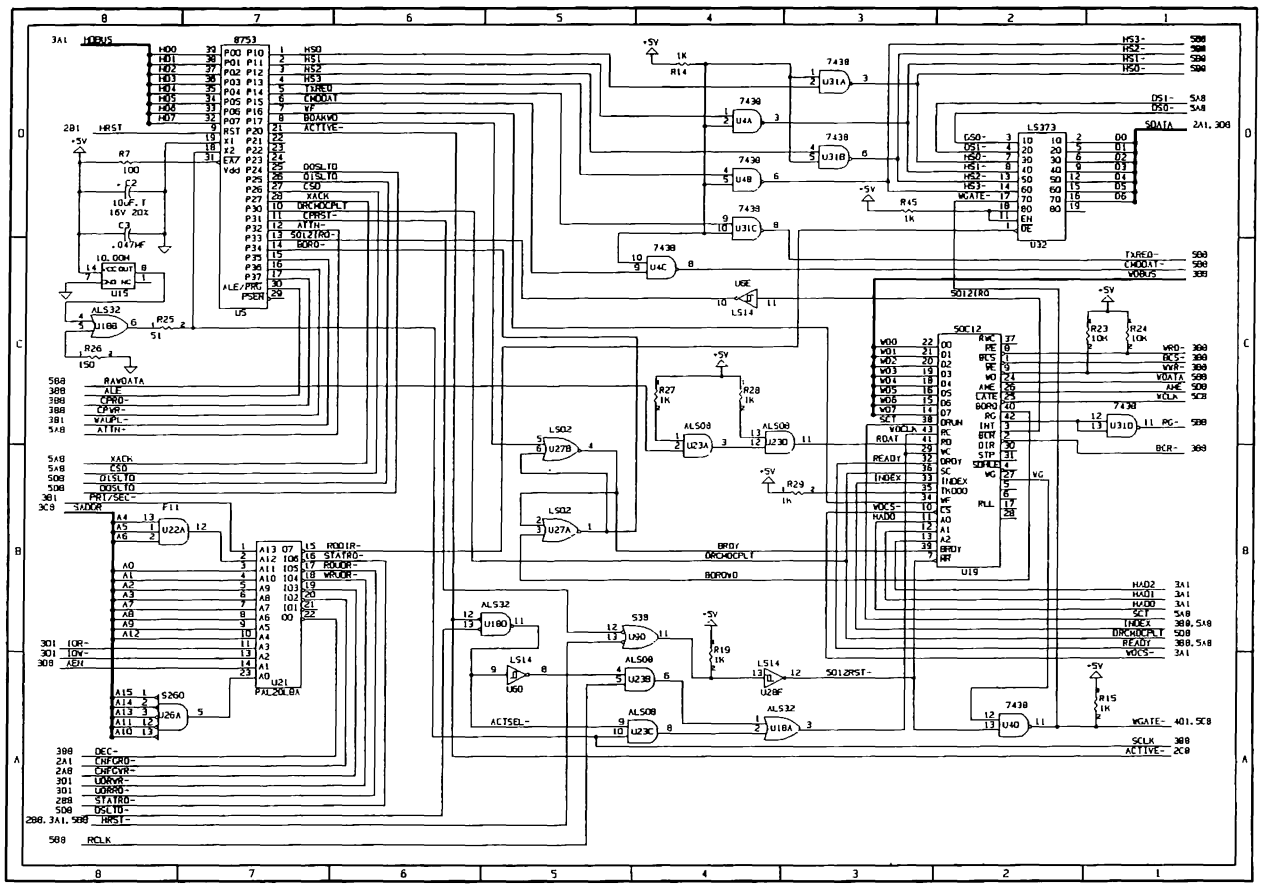

Figure 15-11. Schematic of the External ESDI Controller Board (Page 4 of 5)

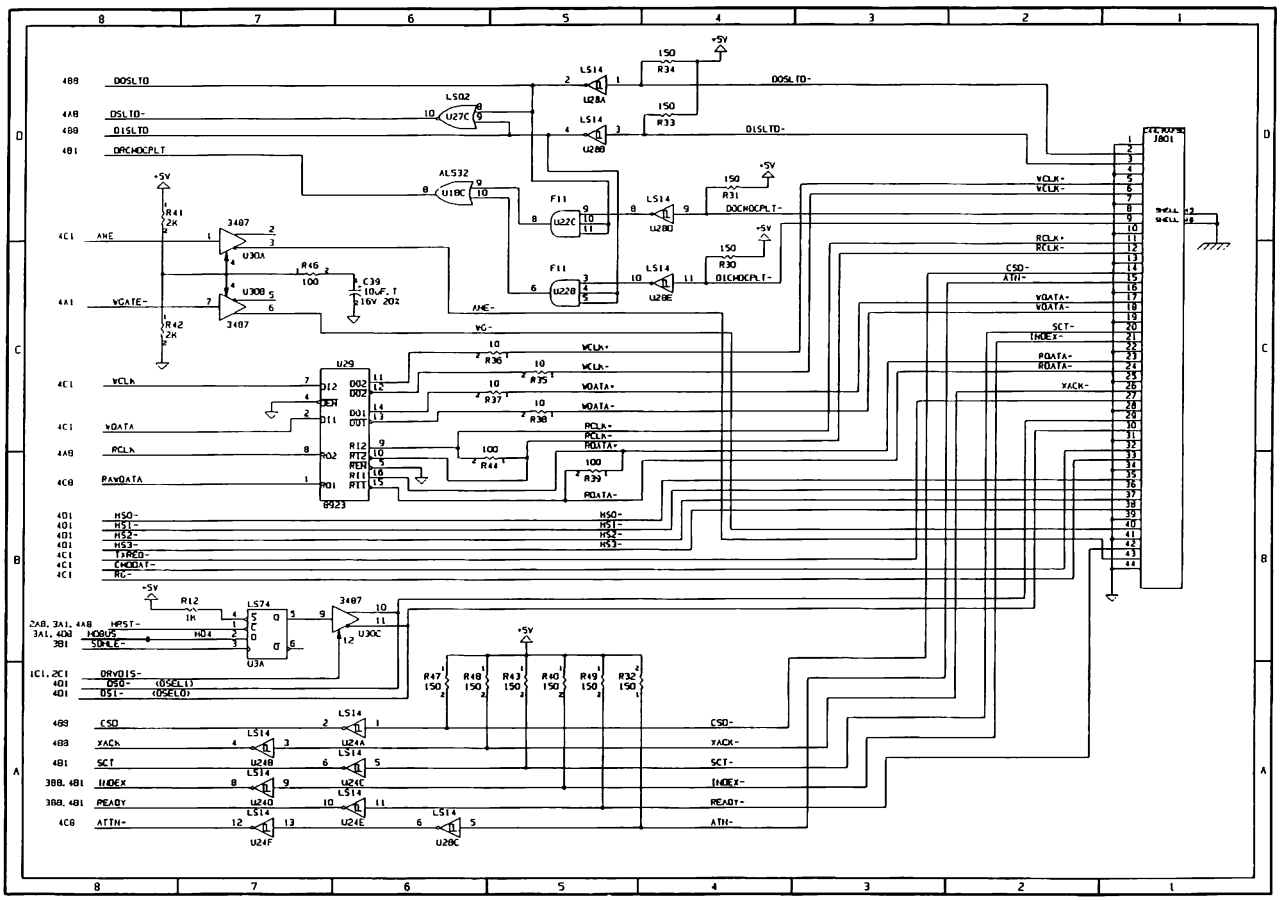

Figure 15-11. Schematic of the External ESDI Controller Board (Page 5 of 5)

Chapter 16

2400 BAUD INTERNAL MODEM

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Chapter 16
2400-BAUD INTERNAL MODEM

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16.1 INTRODUCTION

The 2400-Baud Internal Modem is a Hayes compatible modem that uses standard Bell and CCITT protocols and speeds. Information contained in this chapter can be used as a programming reference in developing software to allow communication between the COMPAQ 80286-Based Personal Computer and other computer services. The information can also be used to help determine the appropriate configurations and settings when using the 2400-Baud Internal Modem existing communications software.

The 2400-Baud Internal Modem is compatible with the following standard protocols and speeds:

- Bell 103 at 300 bps
- CCITT V.21 at 300 bps
- Bell 212A at 1200 bps
- CCITT V.22 1200 bps (asynchronous)
- CCITT V.22 bis at 2400 bps (asynchronous)

This chapter contains the following information about the 2400-Baud Internal Modem option; numbers indicate the number of the section which the indicated topic is discussed:

- Modem functional description and block diagram; COM1/COM2 selection
- Modem commands and result codes [16.2]
- Modem operation registers [16.3]
- Modem programming information [16.4]
- Universal asynchronous receiver/transmitter (UART) registers [16.5]
- Modem connector [16.6]

Functional Description

The modem connects to the system board via a 62 pin industry standard board edge connector. This connection provides signals to and from the system board as well as power to the modem. All signals are CMOS level.

The modem is functionally equivalent to a Hayes internal modem. The UART of the internal modem is compatible with the National Semiconductor NS16C450 UART used on COM adapters.

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Once the modem is installed in the computer and connected to a telephone line, turning on the system unit power switch resets and automatically configures the modem for operation. For proper modem communications to occur, purchased communications software must first write a valid setup sequence to the modem UART. This sequence must include selection of the following parameters:

- Baud Rate: 300, 1200, or 2400
- Format: 7 or 8 data bits; start bits; stop bits; odd, even, or no parity

The 2400 Baud Internal Modem utilizes the Hayes AT command set for computer/modem communications. This command set allows the 2400 Baud Internal Modem to be configured through software and thus eliminates setting switches.

At power-on or modem reset, the modem goes into the command state and interprets the AT commands sent to it from the UART. These commands are used to configure, establish, and control a connection with a remote modem.

When a connection is successfully made, the modem goes into the online state. In this state, data rather than AT commands are passed to the remote computer. The modem remains in the online state until an escape code is received; receipt of this code causes the modem to revert to the command state. The modem also reverts to the command state when the connection is broken by either the internal modem or the remote modem.

Included as part of the AT command set are twenty eight 8-bit registers (0 through 27). The registers store operating instructions for the modem, such as timing parameters, counters, and ASCII values for frequently-used characters.

Figure 16-1 shows a block diagram of the 2400 baud modem.

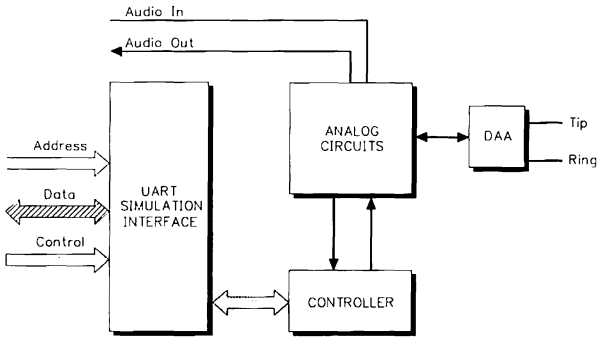

Figure 16-1. Block Diagram of 2400 Baud Internal Modem

COM1/COM2 Selection

The modem (or another serial device) can be configured for either of two I/O ports, COM1 or COM2, for asynchronous (serial) communications devices, although only one device at a time can use COM1 or COM2. COM1 and COM2 interrupt requests (IRQ) can also be addressed for either the internal modem or another serial device. COM2 is the default I/O port for the 2400-Baud Internal Modem.

COM1 or COM2 is hardware-selected by a switch on the modem labeled COM 1/2.

COM1 uses the hex addresses 3F8h through 3FFh and generates an interrupt request on line IRQ4. COM2 uses hex addresses 2F8h through 2FFh and generates an interrupt request on line IRQ3. If you change the I/O port for the modem, be sure that you do not set the modem to occupy a COM port address that is already being used.

16.2 MODEM COMMANDS AND RESULT CODES

Hayes-compatible commands and result codes are defined in Table 16-1 and Table 16-2 respectively.

Table 16-1. Modem Commands

Command	Description
Escape Commands:	
Prefix, Repeat, Escape	
AT	Attention prefix: precedes all command lines except A/ (repeat) and +++ (escape) commands. For command to function, both letters of prefix must be in either uppercase or lowercase.
A/	Repeats last command line. A/ is not preceded by AT or followed by pressing the ENTER key.
+++	Escape code: Allows you to go from online state to command state (1-second pause before and after escape code entry. +++ is not preceded by AT or followed by pressing the ENTER key.)
Selection of Mode of Operation Commands:	
B0	CCITT V.22 bis (2400 bps) CCITT V.22 (1200 bps) CCITT V.21 (300 bps)
*B1	Bell 212A (1200 bps) Bell 103 (300 bps)
Dialing Commands:	
Dn	Dial [n = any digits to dial]. 0 - 9 are valid characters for pulse (rotary) or tone dialing; A,B,C,D, #, or * are valid characters for tone dialing only.
NOTE: * denotes factory setting ** NVRAM default	

(Continued)

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Table 16-1. (Continued)

Command	Description
*P	Pulse (rotary dial)
T	Touch-tone
,	Pause (causes modem to pause for 2 seconds before dialing)
!	Flash (used for PABX special features, such as call forwarding or call transfer)
@	Wait for silence
W	Wait for second dial tone (often used when dialing through a PABX or when using a long distance telephone service)
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)
S	Dial stored number
Other Commands:	
A	Answer call manually without waiting for ring
E0	Disable command echo; characters not echoed
*E1	Enable command echo; characters echoed
F0	Responds ERROR
*F1	Full duplex
*H0	On-hook (hang up)
H1	Off-hook, (request off-hook)
I0	Request product ID code
I1	Request checksum
I2	Verify checksum (OK or ERROR)
I3	Request ROM revision code
L0, L1	Low speaker volume
*L2	Medium speaker volume
L3	High speaker volume
M0	Speaker always off
*M1	Speaker on until carrier detected
M2	Speaker always on
M3	Speaker on until carrier detected except during dialing
O0	Go to online state
O1	Go online and request retrain
*O2	Enable automatic request for retrain
O3	Disable automatic request for retrain
*Q0	Result codes displayed
Q1	Result codes not displayed
r?	Requests current value of register r and reports to host; r = 0-27 (number of registers)
r=n	Assigns a value n to register r
V0	Numerical result codes
*V1	Word result codes
Xn	Result code selection
X0	Basic result code set (0-4)
X1	Extended result code set (0-5,10)
X2	Add dial tone detection (0-6,10)
X3	Add busy signal detection (0-5,7,10)
*X4	Add dial tone and busy signal detection (0-7,10)
*Y0	Long space disconnect disabled
Y1	Long space disconnect enabled
Z	Software reset: restores all NVRAM default settings

NOTE: * denotes factory setting
** NVRAM default

(Continued)

Table 16-1. (Continued)

NOTE: * denotes factory setting
** NVRAM default

(Continued)

Table 16-1. (Continued)

Command	Description
*&C0	Data carrier detect (DCD) always on
**&C1	DCD ON only when data carrier is present
*&D0	The modem ignores the data terminal ready (DTR)
&D1	The modem assumes the asynchronous command state if an ON-to-OFF transition of DTR is detected
**&D2	The modem hangs up, assumes the asynchronous command state, and disables auto-answer when an ON-to-OFF transition of DTR is detected
&D3	A modem reset occurs when an ON-to-OFF transition of DTR is detected
&F	Modem loads default configuration from modem ROM firmware
&G = Guard tone selection (CCITT) (used for a call from the United States to a European country)	
*&G0	No guard tone
&G1	550-Hz guard tone
&G2	1800-Hz guard tone
&J = Means of connection to telephone network	
*&J0	Typical USOC RJ11C telephone jack
&J1	A/A1 lead control; USOC RJ12/RJ13 jack. A/A1 lead control not supported in hardware; however, the AT commands and S register status bit responds as if it were supported.
&P = Make/break dial pulse ratio selection	
&P0	United States/Canada ratio of 39/61
&P1	UK/Hong Kong ratio of 33/67

NOTE: * denotes factory setting
** NVRAM default

(Continued)

Table 16-1. (Continued)

Command	Description
&R = Request-to-send (RTS) and clear-to-send selection (CTS)	
*&R0	CTS follows RTS; responds with ERROR
&R1	CTS is always on (modem ignores RTS); responds with ERROR
&S = Data Set Ready (DSR) command	
*&S0	DSR always ON
&S1	DSR complies with RS232C specifications; responds with ERROR
&T = Test command	
*&T0	Terminates any test in progress
&T1	Starts local analog loopback test
&T3	Starts local digital loopback test
&T4	The modem grants a request from a remote modem for remote digital loopback (RDL)
&T5	The modem denies a request from a remote modem for RDL
&T6	Starts remote digital loopback test
&T7	Starts RDL with self-test
&T8	Starts local analog loopback test with self-test
&W	Write (save) active (current) configuration to NVRAM
&Zn	Write (save) telephone number n to NVRAM

NOTE: * denotes factory setting
** NVRAM default

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Table 16-2. Modem Result Codes

Code	Command	Description
0	OK	Command line executed without error
1	CONNECT	Connected at 300 bps (X1, X2, X3, X4 commands) Connected at 300, 1200, or 2400 bps (X0 command)
2	RING	Ringing signal detected
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command; error in command line; command line exceeds buffer (40 characters, including punctuation); cannot operate at 300 bps in CCITT V.22 mode; invalid character format at 1200 bps; invalid checksum
5	CONNECT	Connected at 1200 bps; (X1, X2, X3, X4 commands) 1200
6	NO DIALTONE	Dial tone not detected and subsequent commands not processed (X2, X4 commands)
7	BUSY	Busy signal detected and subsequent commands not processed (X3, X4 commands)
8	NO ANSWER	Silence not detected and subsequent commands not processed (@ dial modifier only)
10	CONNECT	Connected at 2400 bps (X1, X2, X3, X4 commands) 2400

16.3 MODEM OPERATION REGISTERS

Included as part of the AT command set are twenty-eight 8-bit registers (0-27) referred to as operation registers. Eight of these registers can be saved into NVRAM, so that during power-on or reset the configuration which the user defines is automatically loaded by the modem. Three modem configuration profiles can exist:

- Factory Configuration: This configuration, saved in ROM, sets the modem into a state which most communications software can recognize. This configuration can become the active configuration by execution of the AT&F command. It can become The user configuration by execution of the AT&F&W command.
- User Configuration: This configuration is the configuration saved in NVRAM. The user or the communications software package creates this configuration by changing the active configuration and then executing the AT&W command.
- Active Configuration: This configuration consists of the current modem settings during a communication session. It can become the factory configuration if an AT&F command is executed, or it can be the user configuration if the settings have not been changed after a reset.

This section provides general information about viewing the current value of a register, changing the current value of one or more registers, and returning all registers to their original default settings. This information is followed by detailed discussions of the 28 operation registers.

Each register is assigned a default value at power-on and at modem reset.

The value of a register is expressed as a string of ASCII characters. However, some communication software may have to convert the ASCII values into hexadecimal or other common notation when using the internal registers (and UART registers).

NOTE: All register commands are preceded by typing the letters AT. All register commands are terminated by pressing the ENTER key.

Viewing the Current Value of a Register

To see the current value of a register, follow these instructions:

1. Type ATr? (r = the number of the register)
2. Press the ENTER key

The current decimal value of the specified register is displayed in ASCII.

Viewing the Current Values of More Than One Register

The values of several registers can be shown with one command. For example, to view the current decimal values in registers 0 and 7, follow these instructions:

1. Type AT0?7?
2. Press the ENTER key

The ASCII value stored in each register specified is displayed in order. For example, the display shown in response to the command issued in Step 1 might be:

001
030

This display indicates that 001 is stored in register 0 and 030 is stored in register 7.

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Changing the Value of a Register

To change the current value of a register, follow these instructions:

1. Type ATr=n r = the number of the register; n = the new decimal value to be entered in the register. The valid values for n vary with the individual register.
2. Press the ENTER key

For example, to enter 030 in register 7, type AT7=030, then press the ENTER key.

The value of n specified is entered in the named register.

Returning to User NVRAM Configuration

To return to the user NVRAM configuration, follow these instructions:

1. Type ATZ
2. Press the ENTER key

All registers are returned to the user configuration values.

NOTE: This command also breaks the connection when the command is issued in conjunction with the escape code command (+++) while online.

To store a programmed value to the user NVRAM configuration, follow these instructions:

1. Type AT&W
2. Press the ENTER key

Returning to Original Factory Configuration

To return to the original factory configuration, follow these instructions.

1. Type AT&F
2. Press the ENTER key

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Register Descriptions

This section provides complete information on all 28 operation registers. Registers 0 through 12 and 18, 25, and 26 can be set by the user. Registers 14, 16, 21 through 23, and 27 are bit-mapped and merely reflect parameters that have been set for the modem.

The registers described in this section are:

- 0 - Ring to answer on
- 1 - Ring count
- 2 - Escape code character
- 3 - Carriage return
- 4 - Line-feed character
- 5 - Backspace character
- 6 - Wait for dial tone
- 7 - Wait for carrier after dialing
- 8 - Pause time for comma
- 9 - Carrier detect response time
- 10 - Delay between carrier loss and hang up
- 11 - Dual-tone multifrequency (DTMF) dialing speed (DTR)
- 12 - Escape code guard time
- 13 - Reserved
- 14 - Bit mapped
- 15 - Reserved
- 16 - Bit mapped
- 17 - Reserved
- 18 - Test timer
- 19 - Reserved
- 20 - Reserved
- 21 - Bit mapped
- 22 - Bit mapped
- 23 - Bit mapped
- 24 - Reserved
- 25 - Delay to data terminal ready
- 26 - RTS to CTS delay
- 27 - Bit mapped

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0 - Ring to Answer On

Register 0 determines the number of times the telephone rings before the internal modem automatically answers the call.

Value Range: 0 through 255 (number of rings)

Default: 00 (the modem does not answer at all)

If register 0 is set at the default (0), the internal modem does NOT automatically answer the telephone.

When register 0 is set to a number greater than 0, the internal modem answers the telephone automatically (auto-answer) on the ring specified.

1 - Ring Count

Register 1 is a read-only register which works with register 0 to track the number of times the telephone rings.

Value Range: 0 through 8 (number of rings)

Default: 00

When register 1 is a value greater than 0, and no ring occurs for 8 seconds, the register reverts to the default of 0 rings.

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2 - Escape Code Character

Register 2 holds the ASCII value of the escape command.

Value Range: 0 through 127 (ASCII)

Default: 43

If you are echoing remote modem commands, it is possible that your modem can be put into the command state accidentally while receiving a signal. This situation can be avoided by changing the value of your escape code.

NOTE: Do not enter a value greater than 127. A value greater than 127 completely disables the escape command; that is, the modem does not recognize any commands, including the hang-up (H0) command. This situation would prevent you from breaking the connection, and you would be forced to wait for the other modem to disconnect.

3 - Carriage Return

Register 3 holds the ASCII value that is transmitted to signify the end of line when you press the ENTER key.

Value Range: 0 through 127 (ASCII)

Default: 13

The end-of-line character terminates both the command line and the result code.

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4 - Line-Feed Character

Register 4 holds the ASCII value that is transmitted to signify a line feed when you press the ENTER key.

Range Value: 0 through 127 (ASCII)

Default: 10

If you do not want a line-feed character, set the value at 0. When result codes are displayed as words, the line-feed character is output after you press the ENTER key.

5 - Backspace Character

Register 5 holds the ASCII value of the backspace character.

Value Range: 0 through 127

Default 08

The backspace character acts as both the BACKSPACE key and the character to move the cursor back one space. The BACKSPACE key is echoed back to the computer and is followed by an ASCII space character and a second backspace character (three characters in all). Because the time required to process a backspace character is the same as the time required by the modem to transmit three characters, a repeat-key function may not work properly on backspaces.

6 - Wait For Dial Tone

Register 6 controls the amount of time (delay) the modem waits to dial after the phone is picked up.

Value Range: 2 through 255 (seconds)

Default: 02

This delay allows the telephone system time to detect the off-hook condition and for the dial tone to come on. This feature allows you to increase the delay if a dial tone does not occur within 2 seconds. If you set register 6 for less than 2 seconds, the modem still waits 2 seconds before dialing.

Register 6 is used only if X-codes X0, X1, or X3 are selected. Do not set register 6 if you have selected codes X2 or X4, which enable dial tone detection and disable blind dialing, as these X-codes override the register 6 setting.

Register 6 does not control the W (Wait for Dial Tone) command.

7 - Wait For Carrier After Dialing

Register 7 controls the number of seconds the internal modem waits for an answering modem's carrier signal after dialing.

Value Range: 1 through 255 (seconds)

Default: 30

If the internal modem does not detect a carrier within 30 seconds (default), it hangs up and sends the NO CARRIER result code.

Register 7 also controls the number of seconds the internal modem waits for a dial tone after the W (Wait for Dial Tone) command is issued before hanging up and sending the NO DIALTONE (issued as two words) result code.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

8 - Pause Time for Comma

Register 8 determines the number of seconds the pause (generated by the "," comma dial modifier) lasts.

Value Range: 0 through 255 (seconds)

Default: 02

9 - Carrier Detect Response Time

Register 9 determines the length of time that a carrier signal must be present for the internal modem to recognize the signal and to send a carrier detect tone.

Value Range: 1 through 255 (0.1 through 25.5 seconds)

Default: 06 (0.6 second)

This feature safeguards against the modem mistaking a busy signal or a ring for a carrier signal.

The value range and default for register 9 represent 0.1 (1/10) second increments. The higher the value, the easier the internal modem detects a carrier signal without error.

10 - Delay Between Carrier Loss and Hang-Up

Register 10 allows you to set the amount of time that elapses after a remote modem carrier signal is lost before the internal modem disconnects.

Value Range: 1 through 255 (0.1 through 25.5 seconds)

Default: 14 (1.4 seconds)

Setting the delay time allows the carrier to disappear momentarily without causing the internal modem to disconnect.

The value range and default for register 10 represents 0.1 (1/10) second increments. If your line has a lot of static, set register 10 for a value greater than 1.4. Setting register 10 to 255 causes the modem to ignore actual carrier status and to function as though a carrier were constantly present.

NOTE: If the value in register 10 is set for less than the value of register 9, even a momentary loss of carrier signal causes the internal modem to disconnect. This occurs because the end of the delay period (before the modem disconnects) is reached before the carrier signal is detected.

11 - Dual-Tone Multi-frequency (DTMF) Dialing Speed

Register 11 sets the duration and spacing of touch tones in DTMF dialing.

Value Range: 50 through 255 (.05 through .255 seconds)

Default: 95 milliseconds

The value range and default for register 11 represent 0.001 (1/1000) second increments. The default dialing speed settings give the equivalent of 7.14 digits per second. The minimum length of time for reliable dialing is 50 milliseconds, or 10 digits per second. A maximum of 255 milliseconds slows dialing speed to 1.9 digits per second.

NOTE: Setting register 11 has no effect on pulse dialing speed, which is 10.5 pulses per second in the United States and 10.3 pulses per second outside the United States.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

12 - Escape Code Guard Time

Register 12 controls the escape code guard time. The escape code guard time is the time delay required before and after entering escape code characters.

Value Range: 0, 20 through 255 (0, 0.4 through 5.1 seconds)

Default: 50 (1 second)

The guard time also determines how quickly you must enter the escape code characters. The interval between each of the (three) escape code characters must be less than the guard time; otherwise, the escape code is not recognized.

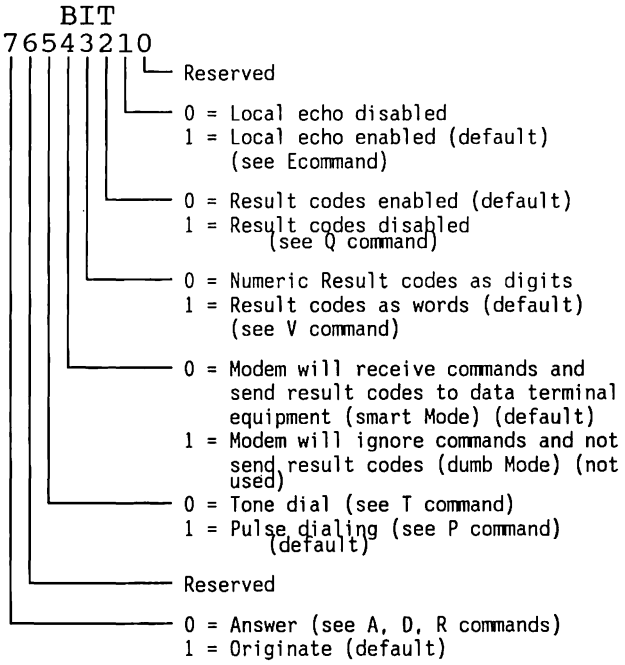
The value range and default for register 12 represent 0.02 (1/50) second increments. To instruct the modem to disregard guard time entirely when recognizing the escape code, set the guard time to 0.

13 - Reserved

This register is reserved.

14 - Bit Mappped

Register 14 for the 2400-Baud Internal Modem is defined as follows:



CAUTION

Writing to register 14 may cause unpredictable results.

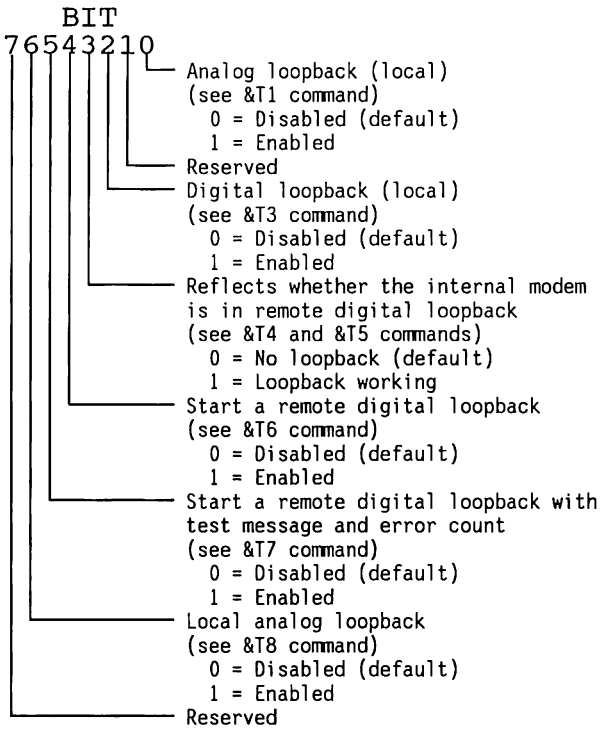
Addendum 114271-001 (12-88)
To Manual No. 102789-001

15 - Reserved

This register is reserved.

16 - Bit Mapped

This register controls the modem testing features for the 2400-baud modem:



CAUTION

Writing to register 16 may cause unpredictable results.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

17 - Reserved

This register is reserved.

18 - Test Timer

This register is used to determine the length of time allowed for a modem diagnostic test.

Value Range: 0 through 255 (seconds)

Default: 0 (disables the register)

The modem automatically cancels any diagnostic test when the duration of the test equals the value selected.

19 - Reserved

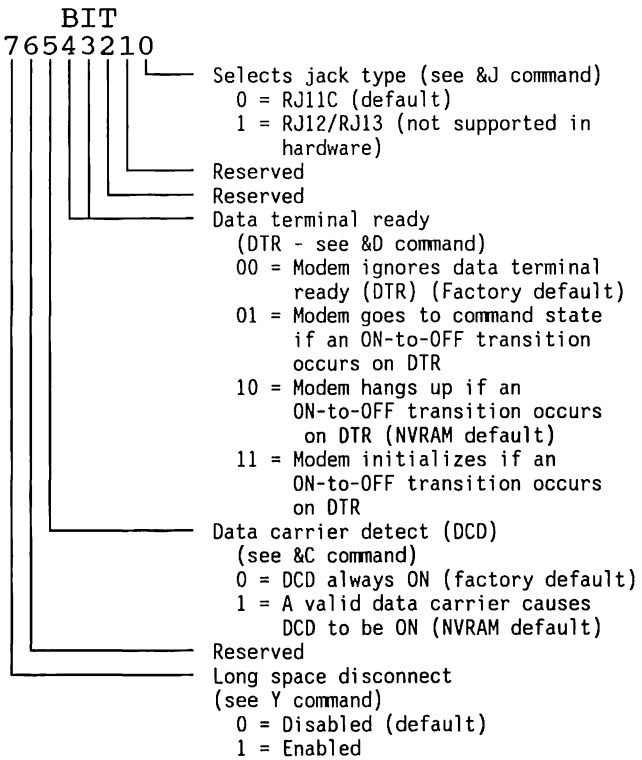
This register is reserved.

20 - Reserved

This register is reserved.

21 - Bit Mapped

This register determines several bit-mapped options, as described in the following bit map:

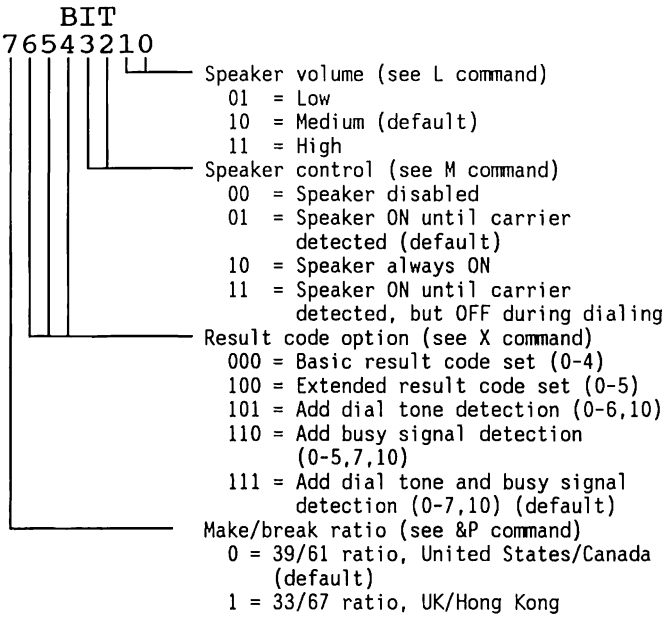


CAUTION

Writing to register 21 may cause unpredictable results.

22 - Bit Mapped

This register determines several bit-mapped options as described in the following bit map:

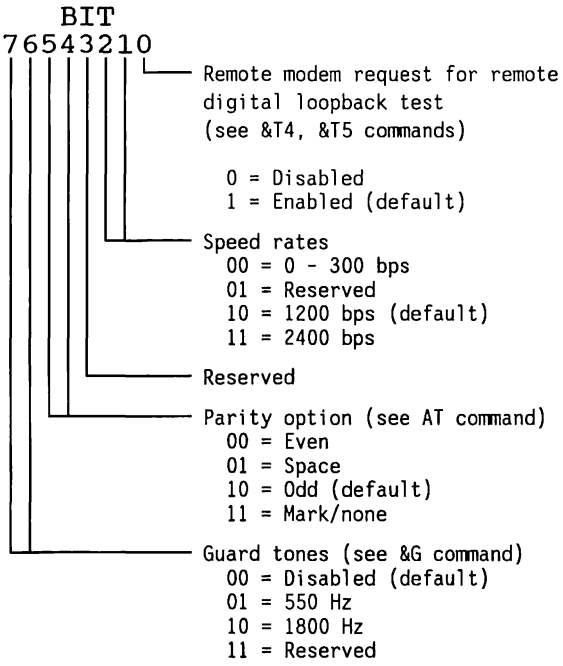


CAUTION

Writing to register 22 may cause unpredictable results.

23 - Bit Mapped

This register determines several bit-mapped options as described in the following bit map:



CAUTION

Writing to register 23 may cause unpredictable results.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

24 - Reserved

This register is reserved.

25 - Delay To Data Terminal Ready

This register detects a change in the data terminal ready (DTR) signal.

Value Range: 0 through 255 (.05 through 2.55 seconds)

Default: 5 (.05 seconds)

The value range and default for register 9 represent 0.01 (1/100) second increments. When the internal modem is in the asynchronous mode, a change in DTR (to ON or to OFF) lasting for less than the value of the register is ignored.

26 - RTS to CTS Delay

This register sets the delay from request-to-send (RTS) to clear-to-send (CTS).

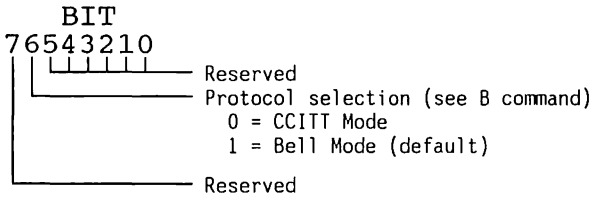
Value Range: 0 through 255 (0 through 2.55 seconds)

Default: 00

The value range and default for register 26 represent 0.01 (1/100) second increments.

27 - Bit Mapped

This register determines protocol selection.



CAUTION

Writing to register 27 may cause unpredictable results.

16.4 PROGRAMMING INFORMATION

The following information is provided for the computer programmer who has some training or experience writing asynchronous communications software. This section includes technical details on the local and remote interface parameters, sequences of events that occur during calling and answering, and some special programming considerations.

Programming Guidelines

The foundation of communications software is a program capable of sending ASCII characters to a modem through a communication port.

To ensure compatibility with remote modems and various telephone systems, the program should implement all commands and functions available in the communications software package. This also gives the user complete access to all features.

The internal modem command buffer can hold a maximum of 40 characters. A longer command string will not be executed and will return an error message.

NOTE: Routines that write to bit-mapped operation registers are not advisable, since writing to these registers can have unpredictable results.

Software should be able to address the internal modem's UART registers to help the modem adapt automatically to incoming calls with various speeds and communication protocols.

Pascal, C, Basic, or assembly language can be used to develop communications software. All of these languages have adequate support for COM1 or COM2 devices.

Addendum 114271-001 (12-88)
To Manual No. 102789-001

Selecting Interface Parameters

You must establish the parameters that define how the modem communicates with the remote computer and the COMPAQ 80286-Based Personal Computer. These parameters define the remote and local interfaces.

Local

Local interface parameters influence communication between the internal modem and the COMPAQ 80286-Based Personal computer. Before any processing, set the local interface parameters to ensure that the modem accurately processes commands and result codes.

Table 16-3 defines the recommended local interface parameters.

Table 16-3. Local Interface Parameters

Parameter	Description
E0	Disables character echo in command mode, making it easier to read result codes and recognize mistakes
Q0	Enables result codes
V1	Displays result codes as words rather than numbers
X3	Selects extended result code set and informs user of connection speed (blind dialing)
S0=0	Disables auto-answer; setting S0 greater than or equal to 1 causes the modem to answer automatically on that number of rings
S2=29	Sets escape code character to ASCII 29 (CTRL]) when originating a call
S2=28	Sets escape code character to ASCII 28 (CTRL \) when answering a call; If the two communicating modems do not use different escape codes, the software must be designed to handle sudden and unpredictable transitions into the command mode
S3=30	Sets the carriage return character to ASCII 30 (CTRL ^)

(Continued)

Table 16-3. (Continued)

Parameter	Description
S4=31	Sets the line feed character to ASCII 31 (CTRL _); Word result codes are preceded and followed by a carriage return/line feed, whereas commands and numeric result codes are simply followed by pressing the ENTER key; setting the carriage return and line feed to infrequently-used characters better offsets the result codes and commands from data on the display
S12=20	Establishes an escape code guard time at least two to three times greater than the time required to transmit a character at 300 bps, the lowest transmission speed

Remote

Remote interface parameters affect communication between the internal modem and the remote computer. Parameters include characteristics of the phone equipment, the remote modem, and the remote computer.

Three sequences of commands are described to illustrate remote interface parameters. Software should set these parameters and send them to the modem immediately before originating or answering a call.

Sequence 1 - Preparing to Dial

Command	Description
ATS6=2	Sets time delay before blind dialing
ATS8=2 (optional)	Sets length of pause generated by the comma (,) dial modifier
ATS11=70	Sets the speed of touch-tone dialing
ATM1	Selects speaker mode
ATD; (required)	Causes the modem to go off-hook, wait the time set by register 6, and return to the command mode

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If a dial tone is detected within the time specified by register 6, the program should proceed with sequence 2 and request a number to dial. Sequence 2 is unnecessary if a number to dial is entered after the ATD command instead of the semicolon. If so, the number is dialed as soon as the command is entered. The program should inform the user when the modem goes off-hook.

In sequence 1, the ATD command is the only required command, since the modem defaults can be used for the first four parameters.

Sequence 2 - Dialing

Command	Description
ATS6=2 (optional)	Resets time delay before blind dialing
ATD (required)	Dial command followed by the phone number (up to 36 digits)

In sequence 2, resetting 6 to 2 seconds causes immediate dialing, since the modem subtracts an automatic 2-second wait for dial tone from the value you specify for Register 6. The modem should dial the number specified by the user, and the program should inform the user when the dialing is taking place.

Sequence 3 - Going Online (Originate or Answer)

Command	Description
ATM1	Sets the speaker mode
ATS7=30 (optional	Sets the wait time for the carrier
ATS9=6	Sets carrier detect time
ATS10=7	Sets the maximum loss of carrier that can be tolerated without hanging up
Originating ATS2=290 (required)	Sets escape command character to ASCII 29 and issues the O command to complete the connection
Answering ATS2=28A (required)	Sets escape command character to ASCII 28 and issues the A command to provide a carrier signal to the originating modem

The software should wait for "CONNECT nnnn" and adjust the baud rate of the UART accordingly, or inform the user if "NO CARRIER" is received.

Programming Example

The following simple BASIC program shows how to cause the internal modem to dial a number:

```
10 OPEN "COM2:1200,E,7" AS #1
20 INPUT "Number to dial";A$
30 PRINT #1,"ATDT"A$
40 GOTO 20
```

Selecting Valid Character Formats

When developing any communications program for the internal modem, a subroutine must be included to indicate to the UART the standard character format you select for transmitting commands, result codes, and data. This subroutine should consider the rate of data transmission and the maximum word length that can be generated by the UART device. The character format shown in Figure 16-2 illustrates how asynchronous data transmission is performed by the UART.

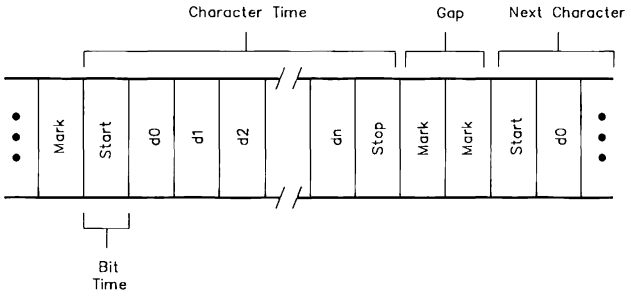

Figure 16-2. Asynchronous Data Transmission

The combination of bits (start, stop, data, and parity) comprising each character determines the format of the commands, result codes, and data transferred by the modem.

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To Manual No. 102789-001

Character Format and Transmission Rate

Although the maximum character length generated by the UART is 12 bits, the bit combinations processed by the modem are restricted by the transmission speed.

Valid Formats at 300, 1200, and 2400 bps

If communications at 300, 1200, and 2400 bps are supported, character length is 10 bits. The following combinations are valid:

Start Bits	Data Bits	Parity	Stop Bits
1	7	mark or space	1
1	7	even or odd	1
1	7	none	2
1	8	none	1

Additional stop bits can be added, but are read as a delay between characters.

Valid Formats at 300 bps Only

If your software is designed for 300 bps communications only, character length can be 10 or 11 bits. The following additional combinations are valid:

Start Bits	Data Bits	Parity	Stop Bits
1	8	even	1
1	8	odd	1

Any additional stop bits are read as a delay between characters.

Detecting Transmission Rate

The settings of the answering modem determine the transmission rate. The AT prefix alerts the modem to the communications rate and parity setting of the local data terminal equipment.

When originating a call, the internal modem automatically adopts these parameters until another AT is received, or until the power is turned off. When answering a call, the modem determines the transmission speed from the carrier signal of the originating modem.

Changes in Speed and Format

Software must monitor changes in the transmission rate of commands and result codes from connection to connection. This may cause command and result code rates to be different before and after the online connection is made.

The modem accepts commands and generates result codes at a default rate of 2400 bps (when first turned on), or at the speed of the previous command, until either the internal modem rate is changed or the modem answers a call at a different speed.

The modem then adjusts to the new transmission rate and subsequent commands and result codes are generated at the new rate. The initial result code of the answer-call sequence is generated either at the default rate or at the rate of the previous AT command.

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16.5 UART REGISTERS

UART register values are used by communications software to control the internal modem.

The UART registers can be addressed either through I/O port COM1 or COM2 (default) on the COMPAQ 80286-Based Personal Computer for asynchronous communication.

Each addressable UART register is described in a separate subsection. The name of each subsection gives:

- The name of the UART register
- The register base address (in hexadecimal)
- The register designation, either:

  Read/Write
  Read Only
  Write Only

Each register is defined. The registers do not have to be initialized in a particular sequence, except that bit <7> of the Line Control register must be set to access certain registers. Certain bits and registers function together to transfer information.

The UART registers are:

- Divisor Latch (least-significant byte)
- Line Control
- Receiver Buffer
- Modem Control
- Transmitter Holding
- Line Status
- Divisor Latch (most-significant byte)
- Modem Status
- Interrupt Enable
- Scratch Pad
- Interrupt Identification

Divisor Latch - Least-Significant Byte 2F8h [COM2], 3F8h [COM1], (Read/Write)

This register contains the low 8 bits of the baud rate divisor (a formula used to set the baud rate).

This register is used with the Divisor Latch - most-significant byte, which is the next address - 2F9h [COM2] or 3F9h [COM1]. Together both addresses, 2F8h [COM2] or 3F8h [COM1] and 2F9h [COM2] or 3F9h [COM1], must contain the hexadecimal equivalent value of the baud rate divisor to set the desired baud rate.

Use the following hex values for the appropriate baud rate:

Value	Baud Rate
180h	300
60h	1200
30h	2400

The formula for the divisor is:

divisor = 115200/baud

NOTE: To access this register, bit <7> (Divisor Latch) of the Line Control register must be logical 1.

Receiver Buffer 2F8h [COM2], 3F8h [COM1], (Read Only)

This register contains the character that has just been received. The character is received serially. The least-significant bit (bit <0>) is received first. To access this register, bit <7> (Divisor Latch) of the Line Control register must be 0. Data are valid when bit <0> (Data Ready) of the Line Status register is 1.

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Transmitter Holding 2F8h [COM2], 3F8h [COM1], (Write Only)

This register is used to load a character that is about to be transmitted. Bit <5> (Transmitter Holding Register Empty) of the Line Status register must be 1 before loading the next character (see the Line Status register). The least-significant bit (bit <0>) is loaded first. To access this register, bit <7> (Divisor Latch) of the Line Control register must be 0.

Divisor Latch - Most-Significant Byte 2F9h [COM2], 3F9h [COM1], (Read/Write)

This register contains the high 8 bits of the baud rate divisor (a formula used to set the baud rate).

This register is used with the Divisor Latch - least-significant byte, which is at the previous address - 2F8h [COM2], 3F8h [COM1]. Together both addresses, 2F8h [COM2] or 3F8h [COM1] and 2F9h [COM2] or 3F9h [COM1], must contain the hexadecimal equivalent value of the baud rate divisor to set the desired baud rate.

Use the following hexadecimal values for the appropriate baud rate:

Value	Baud Rate
180h	300
60h	1200
30h	2400

The formula for the divisor is:

divisor = 115200/baud

NOTE: To access this register, bit <7> (Divisor Latch) of the Line Control register must be logical 1.

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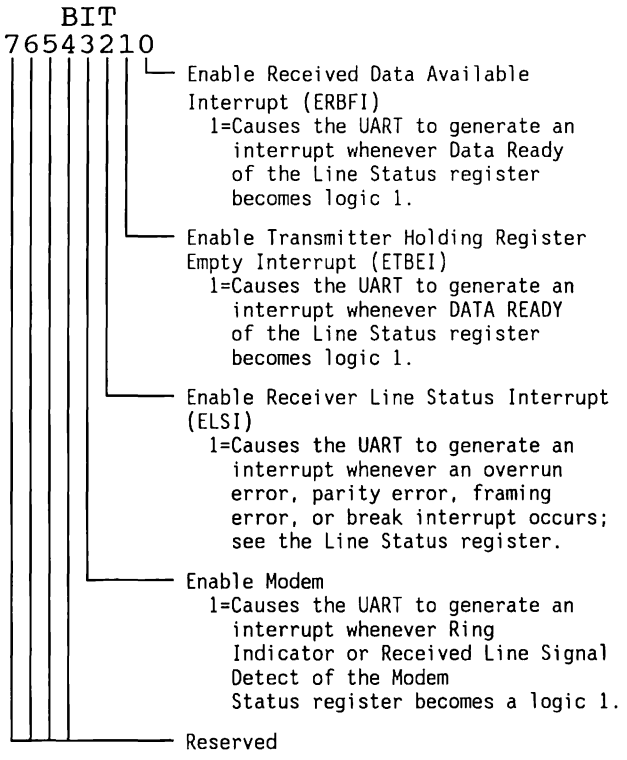
To Manual No. 102789-001

Interrupt Enable 2F9h [COM2], 3F9h [COM1], (Read/Write)

This register enables the interrupts to activate the interrupt output signal.



NOTE: To access this register, bit <7> (Divisor Latch) of the Line Control register must be logical 0.

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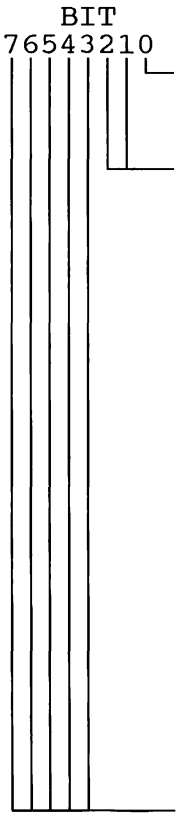
To Manual No. 102789-001

Interrupt Identification 2FAh [COM2], 3FAh [COM1], (Read Only)

This register stores information that indicates a pending interrupt and its priority.

The information contained in bits <0>, <1>, and <2> is always available even if the interrupt capability has not been enabled by the Interrupt Enable register.

NOTE: When COM1 or COM2 is selected, the modem automatically adjusts for either line. However, for an interrupt to reach the processor, OUT 2 (bit <3> of the Modem Control register) must be a logic 1, thereby enabling the interrupt line. The bits of the Interrupt Enable register must be set high (1) to enable the desired interrupt signal, although the interrupt sources can be individually activated.



BIT 2	BIT 1	PRIORITY	INTERRUPT SOURCE
1	1	1 (highest)	Overrun error or parity error or framing error or Break Interrupt (see Line Status register)
1	0	2	Data Ready (see Line Status register)
0	1	3	Transmit Holding register empty (see Line Status register)
0	0	4 (lowest)	Ring indicator or received line signal detect (see Modem Status register)

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To Manual No. 102789-001

Line Control 2FBh [COM2], 3FBh [COM1], (Read/Write)

The Line Control register specifies character and word formats and controls access to other UART registers.

BIT
76543210

Select word length as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Number of Stop Bits (STB)
1 = 2 per character (1-1/2 for 5-bit words only)
0 = 1 per character

Parity Enable (PEN)
1 = Enable parity generation or checking
0 = Disable parity generation or checking

Parity Select (EPS)
1 = Even parity
0 = Odd parity
If even parity is set, bit <3> (Parity Enable) must be a logic 1

Stick Parity
1 = Set
0 = Not set (Bit <3> must be a logic 1 to enable Stick Parity)

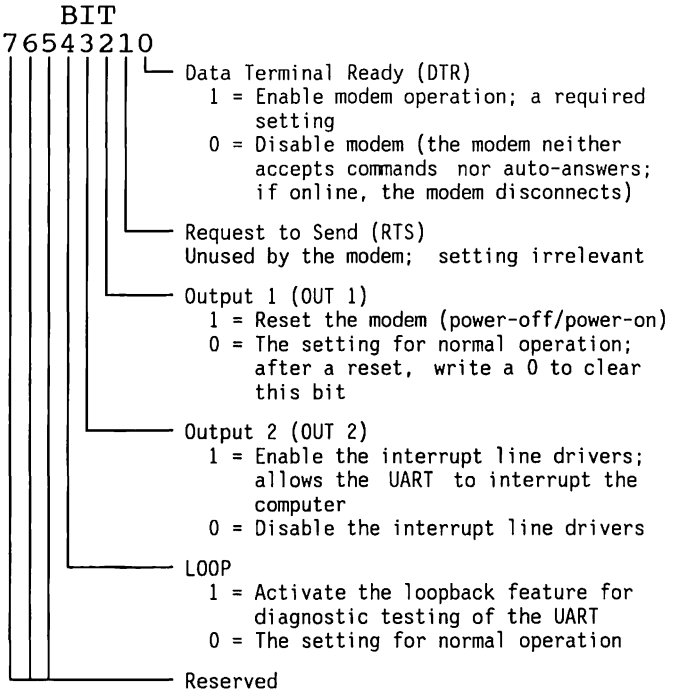
Set Break
1 = Cause modem to transmit a continuous break signal
0 = Stop break signal

Divisor Latch (DLAB)
1 = Enable access to divisor latches of the baud rate generator during a read/write operation
0 = Enable access to the Transmit Holding register, receiver buffer, and Interrupt Enable register

Addendum 114271-001 (12-88)
To Manual No. 102789-001

Modem Control 2FCh [COM2], 3FCh [COM1], (Read/Write)

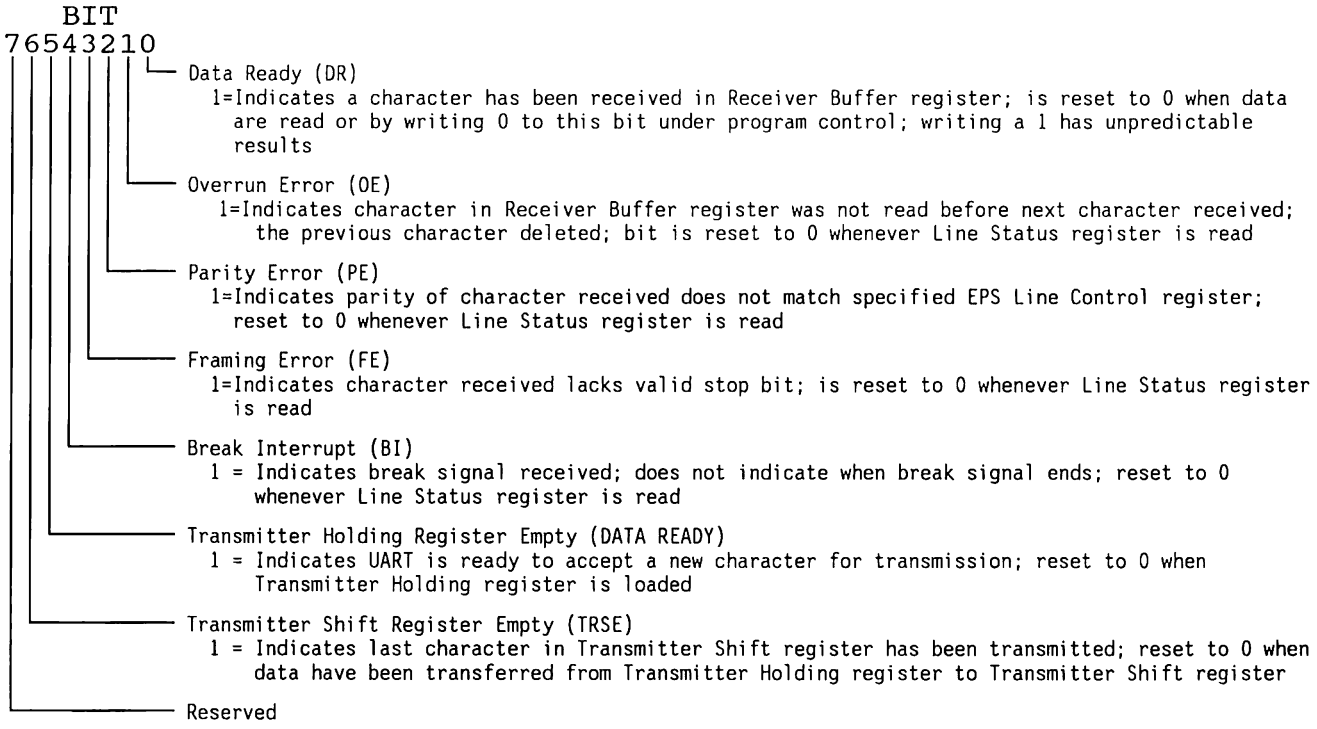
This register manages the interface between the internal modem and the COMPAQ 80286-Based Personal Computer.



Addendum 114271-001 (12-88)
To Manual No. 102789-001

Line Status 2FDh [COM2], 3FDh [COM1], (Read Only) (Bit <0>, Read/Write)

This register provides status information about data transfer and associated error conditions.



Addendum 114271-001 (12-88)
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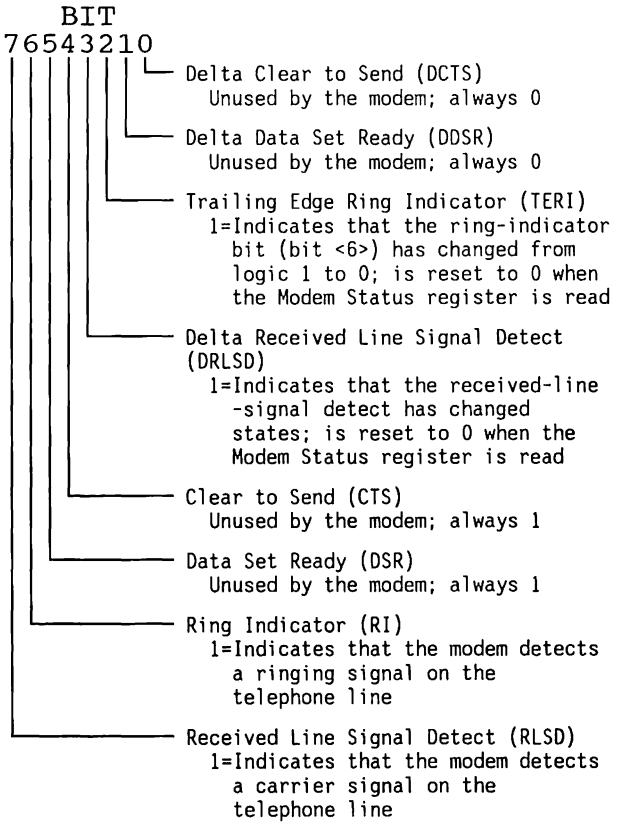
Modem Status 2FEh [COM2], 3FEh [COM1],(Read Only)

The register provides the current status of control signals from the modem. When either bit <2> or bit <3> is a logic 1, a modem status interrupt is generated, if the interrupt is enabled.



Scratch Pad 2FFh [COM2], 3FFh [COM1], (Read/Write)

The Scratch Pad register is an additional modem register that can store 1 byte in bits <7..0>. The byte has no effect on the UART or the internal modem, but can be used as a scratch pad for software.

16.6 MODEM CONNECTOR

The internal modem interfaces with the COMPAQ 80286-Based Personal Computer via a ISA 62-pin edge connector.

Appendix A

ERROR MESSAGES

Appendix A
ERROR MESSAGES

ERROR MESSAGES

The following pages list the error codes and a brief description of the probable source of the error.

Common Power-On Messages

Table A-1 lists the messages that could occur when the system is turned on or reset.

Table A-1. Power-On Messages

Message	Beeps	Probable Cause
163-Time & Date Not Set	2S	Invalid Time or Date
(One very short beep)	1VS	Power-up Successful; FAST (8 MHz) Speed
(Two very short beeps)	2VS	Power-up Successful; System-board DIP Switch Selected Speed (HIGH or AUTO)
RESUME = "F1" KEY	None	Any Failure

Initialization Diagnostic Messages

Table A-2 lists error messages that may occur as part of the Power-On Self-Test (POST).

Table A-2. Power-On Self-Test (Post) Messages

Message	Beeps	Probable Cause
101-I/O ROM Error	1L, 1S	Option ROM checksum
101-ROM Error	1L, 1S	System ROM checksum
102-System Board Failure	None	DMA, timers, etc.
102-System or Memory Board Failure	None	High-order addresses
162-System Options Error	2S	No diskette drives or mismatch in drive types
162-System Options Not Set-(Run Setup)	2S	System configuration
164-Memory Size Error	2S	Memory size discrepancy
XX000Y ZZ 201-Memory Error	None	RAM failure
XX000Y ZZ 203-Memory Address Error	2S	Memory high address error
301-Keyboard Error	None	Keyboard failure
301-Keyboard Error or Test Fixture Installed	None	Keyboard test fixture
302-System Unit Security Lock is Locked - Unlock System Unit Security Lock	2S	System locked
303-Keyboard Controller Error	None	Keyboard controller
304-Keyboard or System Unit Error	None	Keyboard interface
402-Monochrome Adapter Failure	1L, 2S	Mono display controller
501-Display Adapter Failure	1L, 2S	Graphics display controller
601-Diskette Controller Error	None	Diskette controller

(Continued)

Table A-2. (Continued)

Message	Beeps	Probable Cause
602-Diskette Boot Record Error	None	Diskette does not have a valid boot record
702-Coprocessor Detection Error	None	Switch setting does not agree with 80287 detection
1780-Disk 0 Failure	None	Fixed disk drive 0 not ready
1781-Disk 1 Failure	None	Fixed disk drive 1 not ready
1782-Disk Controller Failure	None	Fixed disk drive controller
1790-Disk 0 Error	None	Fixed disk drive 0 access error
1791-Disk 1 Error	None	Fixed disk drive 1 access error
Parity Check 2 XXOOOY ZZ	None	Parity RAM failure

Notes: 1. Tables A-13, A-14, and A-15 define XX, Y, and ZZ.
2. L means a long beep, and S means a short beep.

Advanced Diagnostics Error Messages

The following tables list error messages that may occur during testing by the advanced diagnostics.

Processor

Table A-3 lists error messages that relate to the 80386 microprocessor or to other system board devices.

Table A-3. Processor Error Message

Message	Problem Failure
101-01	CPU test failed
102-01	Numeric co-processor initial status word incorrect
102-02	Numeric co-processor initial control word incorrect
102-03	Numeric co-processor tag word not all ones
102-04	Numeric co-processor tag word not all zeros
102-05	Numeric co-processor exchange command failed
102-06	Numeric co-processor masked exception incorrectly handled
102-07	Numeric co-processor unmasked exception incorrectly handled
102-08	Numeric co-processor wrong mask bit set in status register
102-09	Numeric coprocessor unable to store real number
102-10	Numeric coprocessor real number calculation test failed
102-11	Numeric coprocessor speed test failed
102-12	Numeric coprocessor pattern test failed
102-14	Switch indicates no numeric co-processor present
102-15	Numeric co-processor is inoperative or socket is unoccupied
103-01	DMA page registers test failed
103-02	DMA byte controller test failed
103-03	DMA word controller test failed
104-01	Interrupt controller master test failed
104-02	Interrupt controller slave test failed
104-03	Interrupt controller software RTC is inoperative
105-01	Port 61 bit 6 not at zero
105-02	Port 61 bit 5 not at zero
105-03	Port 61 bit 3 not at zero
105-04	Port 61 bit 1 not at zero
105-05	Port 61 bit 0 not at zero
105-06	Port 61 bit 5 not at one
105-07	Port 61 bit 3 not at one
105-08	Port 61 bit 1 not at one
105-09	Port 61 bit 0 not at one
105-10	Port 61 I/O test failed
105-11	Port 61 bit 7 not at zero
105-12	Port 61 bit 2 not at zero
105-13	No interrupt generated by failsafe timer
105-14	NMI not triggered by failsafe timer
106-01	Keyboard controller self-test failed

(Continued)

Table A-3. (Continued)

Message	Problem Failure
107-01	CMOS RAM test failed
108-02	CMOS interrupt test failed
108-03	CMOS interrupt test, CMOS not properly initialized
109-01	CMOS clock load data test failed
109-02	CMOS clock rollover test failed
109-03	CMOS clock test, CMOS not properly initialized
110-01	Programmable timer load data test failed
110-02	Programmable timer dynamic test failed
111-01	Refresh detect test failed
112-01	Speed test slow mode out of range
112-02	Speed test mixed mode out of range
112-03	Speed test fast mode out of range
112-04	Unable to enter slow mode in speed test
112-05	Unable to enter mixed mode in speed test
112-06	Unable to enter fast mode in speed test
112-07	Speed test system error
113-01	Protected mode test failed
114-01	Speaker test failed

Memory

Table A-4 lists error messages for memory-related errors.

Table A-4. Memory Error Messages

Message	Probable Failure
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
203-01	Memory write/read test failed
203-02	Error during saving program memory in write/read test
203-03	Error during restore of program memory in write/read test
204-01	Memory address test failed
204-02	Error during saving program memory in address test
204-03	Error during restore of program memory in address test
205-01	Walking I/O test failed
205-02	Error during saving program memory in walking I/O test
205-03	Error during restore of program memory in walking I/O test
205-04	Insufficient memory to perform test

Keyboard

Table A-5 lists error messages for keyboard-related errors.

Table A-5. Keyboard Error Messages

Message	Probable Failure
301-01	Keyboard short test, 8042 self-test failed
301-02	Keyboard short test, interface test failed
301-03	Keyboard short test, echo test failed
301-04	Keyboard short test, keyboard reset failed (286/386 only)
301-05	Keyboard short test, keyboard reset failed (88/86 only)
302-01	Keyboard long test, failed
302-02	Remaining unstruck keys
303-01	Keyboard LED test, 8042 self-test failed
303-02	Keyboard LED test, reset test failed
303-03	Keyboard LED test, reset failed
303-04	Keyboard LED test, LED command test failed
303-05	Keyboard LED test, LED command test failed
303-06	Keyboard LED test, LED command test failed
303-07	Keyboard LED test, LED command test failed
303-08	Keyboard LED test, command byte restore test failed
303-09	Keyboard LED test, LEDs failed to light
304-01	Keyboard typematic test failed
304-02	Unable to enter mode 3
304-03	Incorrect scan code from keyboard
304-04	No make code observed
304-05	Unable to disable repeat key feature
315-01	Security lock inoperative
315-02	Security lock stuck in locked position

Printer

Table A-6 lists error messages for printer-related errors.

Table A-6. Printer Error Messages

Message	Probable Failure
401-01	Printer connected test failed
402-01	Printer Data register failed
402-02	Printer Control register failed
402-03	Printer Data and control registers failed
402-04	Printer Loopback failed
402-05	Printer Loopback and data registers failed
402-06	Printer Loopback and control registers failed
402-07	Printer Loopback, data and control registers failed
402-08	Printer Interrupt test failed
402-09	Printer Interrupt and data registers failed
402-10	Printer Interrupt and control registers failed
402-11	Printer Interrupt, control and data registers failed
402-12	Printer Interrupt and loopback failed
402-13	Printer Interrupt, loopback, data registers failed
402-14	Printer Interrupt, loopback, control registers failed
402-15	Printer Interrupt, loopback, control and data registers failed
402-16	Printer unexpected interrupt received
403-01	Printer pattern test failed
498-00	Printer failed or not connected

Video

Table A-7 lists error messages for video-related errors.

Table A-7. Video Error Messages

Message	Probable Failure
501-01	VDU controller test failed
502-01	VDU memory test failed
503-01	VDU attribute test failed
504-01	VDU character set test failed
505-01	VDU 80x25 mode 9x14 char cell test failed
506-01	VDU 80x25 mode 8x8 char cell test failed
507-01	VDU 40x25 mode test failed
508-01	VDU 320x200 mode color set 0 test failed
509-01	VDU 320x200 mode color set 1 test failed
510-01	VDU 640x200 mode test failed
511-01	VDU Screen memory page test failed
512-01	VDU Gray scale test failed
514-01	VDU White screen test failed
516-01	VDU Noise pattern test failed
517-01	Light pen text mode test failed - no response
517-02	Light pen text mode test failed - invalid response
517-03	Light pen medium resolution mode test failed - no response
517-04	Light pen medium resolution mode test failed - invalid response

Table A-8 lists error messages for monochrome video-related errors.

Table A-8. Monochrome Video Error Messages

Message	Probable Failure
802-01	Monochrome video memory test failed
824-01	Monochrome text mode test failed

Diskette Drive

Table A-9 lists error messages for diskette-related errors.

Table A-9. Diskette Drive Error Messages

Message	Probable Failure
600-xx	Floppy ID test
05	Failed to reset controller
20	Failed to get drive type
601-xx	Floppy format
05	Failed to reset controller
09	Failed to format a track
23	Failed to set drive type in ID media
602-xx	Floppy read test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit

(Continued)

Table A-9. (Continued)

Message	Problem Failure
05	Failed to reset controller
06	Fatal error while reading
603-xx	Floppy write read compare test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read buffers
604-xx	Floppy random seek test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
605-xx	Floppy ID media test
20	Failed to get drive type
24	Failed to read floppy media
25	Failed to verify floppy media
606-xx	Floppy speed test
26	Failed to read media in speed test
27	Failed speed limits
607-xx	Floppy wrap test
10	Failed sector wrap test
608-xx	Floppy write protect test
28	Failed write protect test
609-xx	Floppy reset controller test
05	Failed to reset controller

(Continued)

Table A-9. (Continued)

Message	Problem Failure
610-xx	Floppy change line test
21	Failed to get change line status
22	Failed to clear change line status
694-00	Pin 34 not cut on 360-Kbyte diskette drive
697-00	Diskette type error
698-00	Diskette drive speed not within limits
699-00	Drive/media ID error - Rerun SETUP

Serial Communications

Table A-10 lists error messages for serial communications-related errors.

Table A-10. Serial Communications Error Messages

Message	Probable Failure
11xx-yy	Serial port test failed
01-01	UART DLAB bit failure
01-02	Line input or UART fault
01-03	Address line fault
01-04	Data line fault
01-05	UART control signal failure
01-06	UART THRE bit failure
01-07	UART DATA READY bit failure
01-08	UART TX/RX buffer failure
01-09	INTERRUPT circuit failure
01-10	COM 1 set to invalid interrupt
01-11	COM 2 set to invalid interrupt
01-12	DRIVE/RECEIVER control signal failure
01-13	UART control signal interrupt failure
01-14	DRIVER/RECEIVER data failure

(Continued)

Table A-10. (Continued)

Message	Probable Failure
09-01	Clock register initialization failure
09-02	Clock register rollover failure
09-03	Clock reset failure
09-04	Input line or clock failure
09-05	Address line fault
09-06	Data line fault

Modem

Table A-11 lists error messages for serial communications-related errors.

Table A-11. Modem Error Messages

Message	Probable Failure
1201-xx	Modem Internal Loopback Test
01	UART DLAB bit failure
02	Line input or UART fault
03	Address line fault
04	Data line fault
05	UART control signal failure
06	UART THRE bit failure
07	UART DATA READY bit failure
08	UART TX/RX buffer failure
09	INTERRUPT circuit failure
10	COM 1 set to wrong interrupt
11	COM 2 set to wrong interrupt
12	DRIVER/RECEIVER control signal failure
13	UART control signal interrupt failure
14	DRIVE/RECEIVER data failure
15	Modem detection failure
16	Modem ROM checksum failure
17	Tone detection failure
1202-xx	Modem Time-out
1202-01	Modem Timed out waiting for SYNC
02	Modem Timed out waiting for modem response
03	Modem Exceeded data block retry limit
1203-xx	Modem External Termination Test
01	Modem external TIP/RING failure
02	Modem external DATA TIP/RING failure
03	Modem line termination failure
1204-xx	Modem Auto Originate Test
01	Modem Timed out waiting for SYNC
02	Modem Timed out waiting for modem response
03	Modem exceeded data block retry limit
04	RCV exceeded carrier lost limit
05	XMIT exceeded carrier lost limit
06	Timed out waiting for Dial Tone
07	Dial number string too long
08	Modem timed out waiting for remote response
09	Modem exceeded maximum re-dial limit
10	Line Quality prevented remote connection
11	Modem timed out waiting for remote connection
1205-xx	Modem Auto Answer Test
01	Modem Timed out waiting for SYNC
02	Modem Timed out waiting for modem response
03	Modem exceeded data block retry limit
04	RCV exceeded carrier lost limit
05	XMIT exceeded carrier lost limit
06	Timed out waiting for Dial Tone
07	Dial number string too long

(Continued)

Table A-11. (Continued)

Message	Probable Failure
08	Modem timed out waiting for remote response
09	Modem exceeded maximum re-dial limit
10	Line Quality prevented remote connection
11	Modem timed out waiting for remote connection
1210-xx	Modem Direct Connect Test
01	Modem Timed out waiting for SYNC
02	Modem Timed out waiting for modem response
03	Modem exceeded data block retry limit
04	RCV exceeded carrier lost limit
05	XMIT exceeded carrier lost limit
06	Timed out waiting for Dial Tone
07	Dial number string too long
08	Modem timed out waiting for remote response
09	Modem exceeded maximum re-dial limit
10	Line Quality prevented remote connection
11	Modem timed out waiting for remote connection

Fixed Disk Drive

Table A-12 lists error messages for fixed disk drive-related errors.

Table A-12. Fixed Disk Drive Error Messages

Message	Probable Failure
1700-xx	Hard disk ID test
05	Failed to reset controller
09	Failed to format a track
41	Failed to ID hard disk (drive not ready)
42	Recalibrate drive failed
45	Failed to get drive parameters from ROM
46	Invalid drive parameters found in ROM
64	Not a COMPAQ HD Controller ROM
66	Failed init drive parameter
69	Failed to read drive size from controller
70	Failed translate mode
71	Failed non-translated mode
1701-xx	Hard disk format test
05	Failed to reset controller
09	Failed to format a cylinder
42	Recalibrate drive failed
58	Failed to write sector buffer
59	Failed to read sector buffer
66	Failed init drive parameter

(Continued)

Table A-12. (Continued)

Message	Problem Failure
1702-xx	Hard disk read test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
40	Failed cylinder 0
65	Exceeded max bad sector per track
68	Failed to read long
70	Failed translate mode
71	Failed non-translated mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1703-xx	Hard disk write read compare test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read buffers
40	Cylinder 0 error
55	Cylinder 1 error
63	Failed soft error rate
65	Exceeded max bad sector per track
67	Failed to write long

(Continued)

Table A-12. (Continued)

Message	Problem Failure
1703-xx	Hard disk write read compare test
68	Failed to read long
70	Failed translate mode
71	Failed non-translate mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1704-xx	Hard disk random seek test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
40	Cylinder 0 error
55	Cylinder 1 error
65	Exceeded max bad sector per track
70	Failed translate mode
71	Failed non-translate mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1705-xx	Hard disk controller test
05	Failed to reset controller
44	Failed hard disk controller diagnostics
56	Failed controller RAM diagnostics
57	Failed controller to drive diagnostics
1706-xx	Hard disk drive ready test
41	Drive not ready
1707-xx	Hard disk recalibrate test
42	Failed to recalibrate drive

(Continued)

Table A-12. (Continued)

Message	Problem Failure
1708-xx	Hard disk format bad track test
02	Exceeded max hard error limit
05	Failed to reset controller
09	Format track bad failed
42	Recalibrate drive failed
43	Failed to format a cylinder bad
58	Failed to write sector buffer
59	Failed to read sector buffer
1709-xx	Hard disk reset controller test
05	Failed to reset controller
1710-xx	Hard disk park head test
45	Failed to get drive parameters from ROM
47	Failed to park heads
1714-xx	Hard disk file write test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read buffers
10	Failed floppy sector wrap during read
20	Failed to get floppy drive type
24	Failed to read floppy media
25	Failed to verify floppy media

(Continued)

Table A-12. (Continued)

Message	Problem Failure
1714-xx	Hard disk file write test
48	Failed to move disk table to RAM
49	Failed to read floppy media in file write test
50	Failed File I/O write test
51	Failed File I/O read test
52	Failed File I/O compare test
55	Failed cylinder 1
65	Exceeded max bad sector per track
70	Failed translate mode
71	Failed non-translate mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1715-xx	Hard disk head select test
45	Failed to get drive parameters from ROM
53	Failed Drive/Head register test
54	Failed Digital Input register test
1716-xx	Hard disk conditional format test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read buffers
09	Failed to format a cylinder
40	Cylinder 0 error
42	Failed recalibrate
55	Cylinder 1 error

(Continued)

Table A-12. (Continued)

Message	Problem Failure
1716-xx	Hard disk conditional format test
58	Failed to write sector buffer
59	Failed to read sector buffer
60	Failed to compare sector buffer
65	Exceeded max bad sector per track
66	Failed init drive parameter
70	Failed translate mode
71	Failed non-translate mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1717-xx	Hard disk ECC test
01	Exceeded max soft error limit
02	Exceeded max hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Reset controller failed
06	Fatal error while reading (BIOS st. >= 0x20)
07	Fatal error while writing
08	Failed compare of write/read buffers
40	Cylinder 0 failed
55	Cylinder 1 failed
61	Failed uncorrectable error
62	Failed correctable error
65	Exceeded max bad sector per track
67	Failed to write long
68	Failed to read long
70	Failed translate mode
71	Failed non-translate mode
72	Bad track limit exceeded
73	Previously exceeded bad track limit
1799-00	Invalid fixed disk drive type

Fixed Disk Drive Backup (Tape)

Table A-13 lists fixed disk drive backup-related errors.

Table A-13. Fixed Disk Drive Backup (Tape) Error Messages

Message	Probable Cause
1900-xx	Tape ID
01	Drive not installed
02	Cartridge not installed
26	Can not identify drive
27	Drive not compatible with controller
37	Drive installed in other than drive 3
1901-xx	Tape servo write
01	Drive not installed
02	Cartridge not installed
03	Tape motion error
04	Drive busy error
05	Track seek error
06	Tape write protected error
07	Tape already servo written
08	Unable to servo write
11	Drive recalibration error
21	Got servo pulses 2'nd time but not 1'st
22	Never got to EOT after servo check
25	Unable to erase cartridge
27	Drive not compatible with controller
91	Power loss during test - replace cartridge or bulk erase it
1902-xx	Tape format
01	Drive not installed
02	Cartridge not installed

(Continued)

Table A-13. (Continued)

Message	Problem Failure
1902-xx	Tape format
03	Tape motion error
04	Drive busy error
05	Track seek error
06	Tape write protected error
09	Unable to format
10	Format mode error
11	Drive recalibration error
12	Tape not servo written
13	Tape not formatted
21	Got servo pulses 2'nd time but not 1'st
22	Never got to EOT after servo check
27	Drive not compatible with controller
28	Format gap error
1903-xx	Tape drive sensor test
01	Drive not installed
23	Change line unset
27	Drive not compatible with controller
1904-xx	Tape BOT EOT test
01	Drive not installed
02	Cartridge not installed
03	Tape motion error
04	Drive busy error
05	Track seek error
15	Sensor error flag
27	Drive not compatible with controller
30	Exception bit not set
31	Unexpected drive status
32	Device fault
33	Illegal command

(Continued)

Table A-13. (Continued)

Message	Problem Failure
34	No data detected
35	Power-on reset occured
1905-xx	Tape read test
01	Drive not installed
02	Cartridge not installed
03	Tape motion error
04	Drive busy error
05	Track seek error
14	Drive timeout error
16	Block locate (block ID) error
17	Soft error limit exceeded
18	Hard error limit exceeded
19	Write error (probably ID error)
27	Drive not compatible with controller
30	Exception bit not set
31	Unexpected drive status
32	Device fault
33	Illegal command
34	No data detected
35	Power-on reset occured
1906-xx	Tape write/read/compare test
01	Drive not installed
02	Cartridge not installed
03	Tape motion error
04	Drive busy error
05	Track seek error
06	Tape write protected error
14	Drive timeout error
16	Block locate (block ID) error
17	Soft error limit exceeded

(Continued)

Table A-13. (Continued)

Message	Problem Failure
18	Hard error limit exceeded
19	Write (probably ID error)
27	Drive not compatible with controller
30	Exception bit not set
31	Unexpected drive status
32	Device fault
33	Illegal command
34	No data detected
35	Power-on reset occured
1907-xx	Tape Write-Protected Test
24	Failed write-protected test
30	Exception bit not set
31	Unexpected drive status
32	Device fault
33	Illegal command
34	No data detected
35	Power-on reset occured

Enhanced Color Graphics and Video Graphics Controller Boards

Table A-14 lists the Enhanced Color Graphics and Video Graphics Controller Boards-related errors.

Table A-14. Enhanced Color Graphics and Video Graphics Controller Boards-Related Error Messages

Message	Probable Failure
2402-01	VDU memory test failed
2403-01	VDU attribute test failed
2404-01	VDU character set test failed
2405-01	VDU 80x25 mode 9x14 char cell test failed
2406-01	VDU 80x25 mode 8x8 char cell test failed
2407-01	VDU 40x25 mode test failed
2408-01	VDU 320x200 mode color set 0 test failed
2409-01	VDU 320x200 mode color set 1 test failed
2410-01	VDU 640x200 mode test failed
2411-01	VDU Screen memory page test failed
2412-01	VDU Gray scale test failed
2414-01	VDU White screen test failed
2416-01	VDU Noise pattern test failed
2417-01	Lightpen text mode test failed - no response
2417-02	Lightpen text mode test failed - invalid response
2417-03	Lightpen medium res. mode test failed - no response

Table A-14 (Continued)

Message	Probable Failure
2417-04	Lightpen medium res. mode failed - invalid response
2418-01	ECG or VG memory test failed
2418-02	ECG or VG shadow RAM test failed
2419-01	ECG or VG ROM checksum test failed
2420-01	ECG or VG attribute test failed
2421-01	ECG or VG 640x200 graphics mode test failed
2422-01	ECG or VG 640x350 16 color set test failed
2423-01	ECG or VG 640x350 64 color set test failed
2424-01	ECG or VG monochrome text mode test failed
2425-01	ECG or VG monochrome graphics mode test failed
2431-01	Failed 640 x 480 graphics
2432-01	Failed 256-color mode test

Memory-Error Codes

Memory-error codes result when the system detects a memory fault during the power-on self-test or as a result of a diagnostic test. The test programs attempt to isolate the memory fault to a specific chip, then generate a memory-error code that specifies which memory chip to replace.

In some cases, replacing the memory chip will not solve the problem because: 1) the system may not be able to accurately determine which chip or chips are at fault, and 2) the problem may be due to a failure in the memory-support circuitry, not the memory device.

If replacing the indicated memory devices does not solve the problem, return your system to an Authorized COMPAQ Dealer for service. Memory boards with soldered memory devices should also be returned to an Authorized COMPAQ Dealer for service.

The memory-error code points to a specific memory address. The physical location of the memory address depends on the type of system, the number and type of memory boards installed, and type of memory device used (64K RAMs or 256K RAMs).

This section provides 10 tables to help you identify which memory device to replace when the system shows a memory error. Use the following chart to determine which of the 10 tables to use to find the suspected defective chip.

COMPAQ PORTABLE 286 Memory Configurations

System Board RAM Type	Error Code XX Value	Memory Device Location	Lookup Table
64K	00 to 02 (0-256 KB)	System Board	1
	10 to 2E (1-3 MB)	Memory Expansion Board	3
256K	00 to 08 (0-640 KB)	System Board	2
	10 to 2E (1-3 KB)	Memory Expansion Board	3
64K	00 to 08 (0-640 KB)	System Memory Board	4
	00 to 08 (0-640 KB)	Version 2 System Board	6
	10 to 2E (1-3 MB)	Memory Expansion Board	3
256K	00 to 08, 10 to 26 (0-640 KB, 1-2.5 MB)	System Memory Board	5
	00 to 08, 10 to 26 (0-640 KB, 1-2.5 MB)	Version 2 System Board	9
	28 to 46 (2.5-4.5 MB)	Memory Expansion Board	6
	48 to 66 (4.5-6.5 MB)	Memory Expansion Board	7
	68 to 86 (6.5-8.5 MB)	Memory Expansion Board	10

Note: XX codes 0A to 0F represent the memory space for the video memory and system ROMs. Errors in the video memory or system ROM space are not reported in the XX000B YYZZ error message format.

Table 1. Defective Memory Chip Isolation Map for the COMPAQ PORTABLE 286 System Board using 64K RAMs (0-256 KB)

Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "020001 0010" specifies chip U50.

Use the following chart to locate a defective memory chip:

	XX = 00 Bank 0		XX = 02 Bank 1	
Data Bit	B = 0	B = 1	B = 0	B = 1
YY or ZZ	Low	High	Low	High
01	U5	U6	U7	U8
02	U20	U21	U22	U23
04	U25	U26	U27	U28
08	U41	U42	U43	U44
10	U47	U48	U49	U50
20	U63	U64	U65	U66
40	U70	U71	U72	U73
80	U81	U82	U83	U84
00	U88	U89	U90	U91

Table 2. Defective Memory Chip Isolation Map for the COMPAQ PORTABLE 286 System Board using 256K RAMs (0-640 KB)

Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "020000 0100" specifies chip U7.

Use the following chart to locate a defective memory chip:

	XX = 00		XX = 02, 04, 06, 08	
	Bank 0		Bank 1	
Data Bit	B = 0	B = 1	B = 0	B = 1
YY or ZZ	Low	High	Low	High
01	U5	U6	U7	U8
02	U20	U21	U22	U23
04	U25	U26	U27	U28
08	U41	U42	U43	U44
10	U47	U48	U49	U50
20	U63	U64	U65	U66
40	U70	U71	U72	U73
80	U81	U82	U83	U84
00	U88	U89	U90	U91

Table 3. Defective Memory Chip Isolation Map for a Memory Expansion Board Mapped into the 1-3 MB Memory Space (256 KB RAMs)

This isolation map is valid for a system memory board that uses 64K RAMs.
Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "240000 0100" specifies chip U55.

Use the following chart to locate a defective memory chip:

	XX = 10, 12, 14, 16, Bank 1		XX = 18, 1A, 1C, 1E, Bank 2		XX = 20, 22, 24, 26, Bank 3		XX = 28, 2A 2C, 2E Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low
80	U3	U12	U21	U30	U39	U48	U57	U66
40	U4	U13	U22	U31	U40	U49	U58	U67
20	U5	U14	U23	U32	U41	U50	U59	U68
10	U6	U15	U24	U33	U42	U51	U60	U69
08	U7	U16	U25	U34	U43	U52	U61	U70
04	U8	U17	U26	U35	U44	U53	U62	U71
02	U9	U18	U27	U36	U45	U54	U63	U72
01	U10	U19	U28	U37	U46	U55	U64	U73
00	U11	U20	U29	U38	U47	U56	U65	U74

Table 4. Defective Memory Chip Isolation Map for the COMPAQ DESKPRO 286 System Memory Board using 64K RAMs (0-640 KB)

The memory-error code is in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "040001 0010" specifies chip U24.

Use the following chart to locate a defective memory chip:

	XX = 00 Bank 0		XX = 02 Bank 1		XX = 04 Bank 2		XX = 06 Bank 3		XX = 08 Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low	High	Low
80	U1	U2	U3	U12	U21	U30	U39	U48	U57	U66
40			U4	U13	U22	U31	U40	U49	U58	U67
20			U5	U14	U23	U32	U41	U50	U59	U68
10			U6	U15	U24	U33	U42	U51	U60	U69
08			U7	U16	U25	U34	U43	U52	U61	U70
04			U8	U17	U26	U35	U44	U53	U62	U71
02			U9	U18	U27	U36	U45	U54	U63	U72
01			U10	U19	U28	U37	U46	U55	U64	U73
00			U11	U20	U29	U38	U47	U56	U65	U74

Table 5. Defective Memory Chip Isolation Map for the COMPAQ DESKPRO 286 System Memory Board using 256K RAMs (0-640 KB, 1-2.5 MB)

Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "040001 0010" specifies chip U6.

Use the following chart to locate a defective memory chip:

	XX = 00		XX = 02, 04, 06, 08		XX = 10, 12, 14, 16		XX = 18, 1A, 1C, 1E		XX = 20, 22, 24, 26	
	Bank 0		Bank 1		Bank 2		Bank 3		Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low	High	Low
80	U1	U2	U3	U12	U21	U30	U39	U48	U57	U66
40			U4	U13	U22	U31	U40	U49	U58	U67
20			U5	U14	U23	U32	U41	U50	U59	U68
10			U6	U15	U24	U33	U42	U51	U60	U69
08			U7	U16	U25	U34	U43	U52	U61	U70
04			U8	U17	U26	U35	U44	U53	U62	U71
02			U9	U18	U27	U36	U45	U54	U63	U72
01			U10	U19	U28	U37	U46	U55	U64	U73
00			U11	U20	U29	U38	U47	U56	U65	U74

Table 6. Defective Memory Chip Isolation Map for the COMPAQ DESKPRO 286 Version 2 System Board using 64K RAMs (0-640 KB)

The memory-error code is in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "040001 0010" specifies chip U96.

Use the following chart to locate a defective memory chip:

	XX = 00 Bank 0		XX = 02 Bank 1		XX = 04 Bank 2		XX = 06 Bank 3		XX = 08 Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low	High	Low
80	U124	U107	U121	U118	U93	U82	U66	U52	U40	U27
40	U125	U108			U94	U83	U67	U53	U41	U28
20	U126	U109			U95	U84	U68	U54	U42	U29
10	U127	U110			U96	U85	U69	U55	U43	U30
08	U128	U111	U120	U117	U97	U86	U70	U56	U44	U31
04	U129	U112			U98	U87	U71	U57	U45	U32
02	U130	U113			U99	U88	U72	U58	U46	U33
01	U131	U114			U100	U89	U73	U59	U47	U34
00	U132	U115	U122	U119	U101	U90	U74	U60	U48	U35

Table 7. Defective Memory Chip Isolation Map for the COMPAQ DESKPRO 286 Version 2 System Board using 256K RAMs (0-640 KB, 1-2.5 MB)

The memory-error code is in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "040001 0010" specifies chip U121.

Use the following chart to locate a defective memory chip:

	XX = 00		XX = 02, 04, 06, 08		XX = 10, 12, 14, 16		XX = 18, 1A, 1C, 1E		XX = 20, 22, 24, 26	
	Bank 0		Bank 1		Bank 2		Bank 3		Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low	High	Low
80	U124	U107	U121	U118	U93	U82	U66	U52	U40	U27
40	U125	U108			U94	U83	U67	U53	U41	U28
20	U126	U109			U95	U84	U68	U54	U42	U29
10	U127	U110			U96	U85	U69	U55	U43	U30
08	U128	U111	U120	U117	U97	U86	U70	U56	U44	U31
04	U129	U112			U98	U87	U71	U57	U45	U32
02	U130	U113			U99	U88	U72	U58	U46	U33
01	U131	U114			U100	U89	U73	U59	U47	U34
00	U132	U115	U122	U119	U101	U90	U74	U60	U48	U35

Table 8. Defective Memory Chip Isolation Map for a Memory Expansion Board Mapped into the 2.5-4.5 MB Memory Space (256 KB RAMs)

This isolation map is valid for a system memory board that uses 256K RAMs.
Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "2A0001 0080" specifies chip U3.

Use the following chart to locate a defective memory chip:

	XX = 28, 2A, 2C, 2E Bank 1		XX = 30, 32, 34, 36 Bank 2		XX = 38, 3A, 3C, 3E Bank 3		XX = 40, 42, 44, 46 Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low
80	U3	U12	U21	U30	U39	U48	U57	U66
40	U4	U13	U22	U31	U40	U49	U58	U67
20	U5	U14	U23	U32	U41	U50	U59	U68
10	U6	U15	U24	U33	U42	U51	U60	U69
08	U7	U16	U25	U34	U43	U52	U61	U70
04	U8	U17	U26	U35	U44	U53	U62	U71
02	U9	U18	U27	U36	U45	U54	U63	U72
01	U10	U19	U28	U37	U46	U55	U64	U73
00	U11	U20	U29	U38	U47	U56	U65	U74

Table 9. Defective Memory Chip Isolation Map for a Memory Expansion Board Mapped into the 4.5-6.5 MB Memory Space (256 KB RAMs)

Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "520000 0400" specifies chip U35.

Use the following chart to locate a defective memory chip:

	XX = 48, 4A, 4C, 4E Bank 1		XX = 50, 52, 54, 56 Bank 2		XX = 58, 5A, 5C, 5E Bank 3		XX = 60, 62, 64, 66 Bank 4	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low
80	U3	U12	U21	U30	U39	U48	U57	U66
40	U4	U13	U22	U31	U40	U49	U58	U67
20	U5	U14	U23	U32	U41	U50	U59	U68
10	U6	U15	U24	U33	U42	U51	U60	U69
08	U7	U16	U25	U34	U43	U52	U61	U70
04	U8	U17	U26	U35	U44	U53	U62	U71
02	U9	U18	U27	U36	U45	U54	U63	U72
01	U10	U19	U28	U37	U46	U55	U64	U73
00	U11	U20	U29	U38	U47	U56	U65	U74

Table 10. Defective Memory Chip Isolation Map for a Memory Expansion Board Mapped into the 6.5-8.5 MB memory space (256K RAMs)

Memory-error codes are in the format XX000B YYZZ.
XX equals the 128-KB memory segment in which an error is detected.
000 is always equal to 000 (not used)
B identifies whether the defective memory chip is in the high byte or the low byte of the memory bank.
When B = 0, YY defines the defective-chip row location within the low byte of the memory bank.
When B = 1, ZZ defines the defective-chip row location within the high byte of the memory bank.
For example, the memory-error message "860000 0200" specifies chip U72.

Use the following chart to locate a defective memory chip:

	XX = 68, 6A, 6C, 6E (Bank 1)		XX = 70, 72, 74, 76 (Bank 2)		XX = 78, 7A, 7C, 7E (Bank 3)		XX = 80, 82, 84, 86 (Bank 4)	
Data Bit	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0	B = 1	B = 0
YY or ZZ	High	Low	High	Low	High	Low	High	Low
80	U3	U12	U21	U30	U39	U48	U57	U66
40	U4	U13	U22	U31	U40	U49	U58	U67
20	U5	U14	U23	U32	U41	U50	U59	U68
10	U6	U15	U24	U33	U42	U51	U60	U69
08	U7	U16	U25	U34	U43	U52	U61	U70
04	U8	U17	U26	U35	U44	U53	U62	U71
02	U9	U18	U27	U36	U45	U54	U63	U72
01	U10	U19	U28	U37	U46	U55	U64	U73
00	U11	U20	U29	U38	U47	U56	U65	U74

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