QUARTER-INCH CARTRIDGE TAPE HARDWARE MANUAL

NOTE

This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the installation instructions, it may interfere with radio communications. The equipment has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, which users may be required to correct at their own expense.

Specifications Subject to Change.

First Edition (December 1985) A-Ø9-ØØ929-Ø1

CAUTION

You must follow the guidelines outlined below to ensure satisfactory performance and full service life of your quarter-inch cartridge (QIC) drive and tapes. **Be sure the write-protect cam is in the correct position.** You should attain a soft (correctable) error rate of 1 in $1x10^8$ bit transfers, a cartridge life of 2000 passes (one pass is equivalent to winding the tape its full length from one end to the other), and a drive life of 5 years.

Failure to follow these guidelines can result in poor performance (excessive errors); damage to the tape cartridges, tape drive, or both; loss of interchangeability; or a combination of these conditions.

Drive and Cartridge Care. Treat cartridges with care and use them in an environment with the following conditions:

Maximum wet bulb temperature:	79°F (26°C)
Operating temperature:	41°F to 113°F (5°C to 45°C)
Relative humidity:	20% to 80% noncondensing
Altitude:	-1000 feet to 15,000 feet

Be sure to retension the cartridge before its initial pass (see below). Protect the drive and cartridges from excessive shocks, which can impair the drive alignment and cartridge tension. Do not expose the tape cartridge to magnetic fields, such as from CRT screens or power sources.

Approved Cartridge Use. Use only approved tape cartridges to attain the specified error rate standard. Other cartridges may initially meet this standard, yet degrade in reliability over the specified cartridge life. The following cartridge tapes are approved: the DC-600A and DC-615A (3M Corp.), and the 10000FTPI (Data Electronics, Inc.).

Cartridge Retensioning. Keep the cartridge properly tensioned to ensure full life service and data reliability. **Failure to adequately tension the cartridge will damage the cartridge and destroy data on the tape.** To retension the cartridge, use the tape unit retension command. (See Section 4 of the Quarter-Inch Cartridge Tape for NGEN Manual for details.)

With normal use, retension the cartridge every eight hours. When using the tape drive extensively in start/stop mode, retension the cartridge once every two hours.

Tape Head Cleaning. Clean the tape drive read/write head assembly after any initial pass of a new cartridge; once after two hours (of actual tape movement) when using a new cartridge; and at least once every eight hours thereafter for the life of the tape. In addition, if the tape drive has not been used for a week or longer (or if you are not sure how long the tape drive has been unused), clean the tape head before use.

Failure to clean the heads will result in excessive data errors and may decrease the life of the drive. (See Appendix B of the Quarter-Inch Cartridge Tape for NGEN Manual for details.)

CONTENTS

LIST OF FIGURES

LIST OF TABLES

RELATED DOCUMENTATION

The documents described below provide additional information related to the contents of this manual. For a complete list of Convergent Technologies® documentation, see the "Guide to Technical Documentation" in the Executive Manual or similar command-line interpreter manual for your operating system.

CONVERGENT TECHNOLOGIES DOCUMENTATION

Introductory
- Installation Guide (NGEN)
- Operator's Guide (NGEN)

Hardware
- Diagnostics Manual
- Floppy/Hard Disk Manual
- Processor Manuals
- Software Debugger

The NGEN Installation Guide describes the procedure for unpacking, assembling, cabling, and powering up an NGEN workstation.

The NGEN Operator's Guide is a link between the user and the workstation. It describes the operator controls, use of the floppy disk drives, how to verify workstation operations, and how to use software release notices.

The NGEN Diagnostics Manual outlines the tests used to verify proper operation of the modules of a workstation. The manual describes tests for individual modules, along with bootstrap procedures and customization programs.

The Floppy/Hard Disk Manual describes the architecture and theory of operation for the Floppy/Hard Disk Module. It discusses the applicable disk drives and controllers, and contains the applicable OEM disk drive manuals.

The Processor Manuals describe the respective Processor Modules. Each manual (a two-volume set) covers one processor module and details the architecture and theory of operation of the printed circuit boards, external interfaces, and memory expansion, as well as the X-Bus specifications.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. It can be used in debugging C, FORTRAN, Pascal, and assembly language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

VENDOR DOCUMENTATION

The boards that make up the Quarter-Inch Cartridge Tape Module are dependent upon programmable large-scale integration (LSI) circuitry to perform their functions. Since only hardware functions and software interfaces of the LSI circuitry are summarized in this manual, see the following for additional information:

- Intel Component Data Catalog. Santa Clara, CA: Intel Corporation, 1980.
- Intel Microprocessor and Peripheral Handbook. Santa Clara, CA: Intel Corporation, 1980.

NUMBERS

Numbers used in this manual are written in decimal unless suffixed with "h" for hexadecimal. For example, 1Øh = 16 and ØFFh = 255.

SIGNAL NAMES

Signal names used in this manual are suffixed with plus (+) and minus (-) to distinguish active-high from active-low signals, respectively. An example of a RD (Read) signal is as follows:

Signal Name	Logical State	Voltage Level
RD-	Ø (active)	Low
	1 (inactive)	High
RD+	Ø (inactive)	Low
	1 (active)	High

1 OVERVIEW

INTRODUCTION TO THE MANUAL

This manual is written for the engineer who tests or services the Quarter-Inch Cartridge (QIC) Tape Module electronics, or writes or modifies system software for use with the workstation. This manual does not, however, support modifications to existing hardware. The manual is divided into the following chapters:

- o Overview
- o Architecture
- o Theory of Operation
- o Drive Specifications

Chapter 1, "Overview," describes the capabilities of the QIC Tape Module and its major components.

Chapter 2, "Architecture," covers the tape control circuitry in terms of its applicable software interface to hardware components. Applicable command and status registers for the control circuitry are defined. In addition, the X-Bus identification scheme is summarized.

Chapter 3, "Theory of Operation," details the component-level circuit description of the QIC Tape Module. In addition, an interconnect wire list is provided.

Chapter 4, "Drive Specifications," contains the manufacturer's manual for the tape drive.

In addition, Appendix A contains QIC Tape Module specifications, Appendix B contains the schematic diagrams for the QIC Tape Module, and Appendix C contains the cleaning instructions for the drive heads.

GENERAL DESCRIPTION

The QIC Tape Module, shown in Figure 1-1, consists of a single modular assembly and contains the circuitry necessary to provide 55M bytes of storage on one DC-600A, quarter-inch cartridge tape.

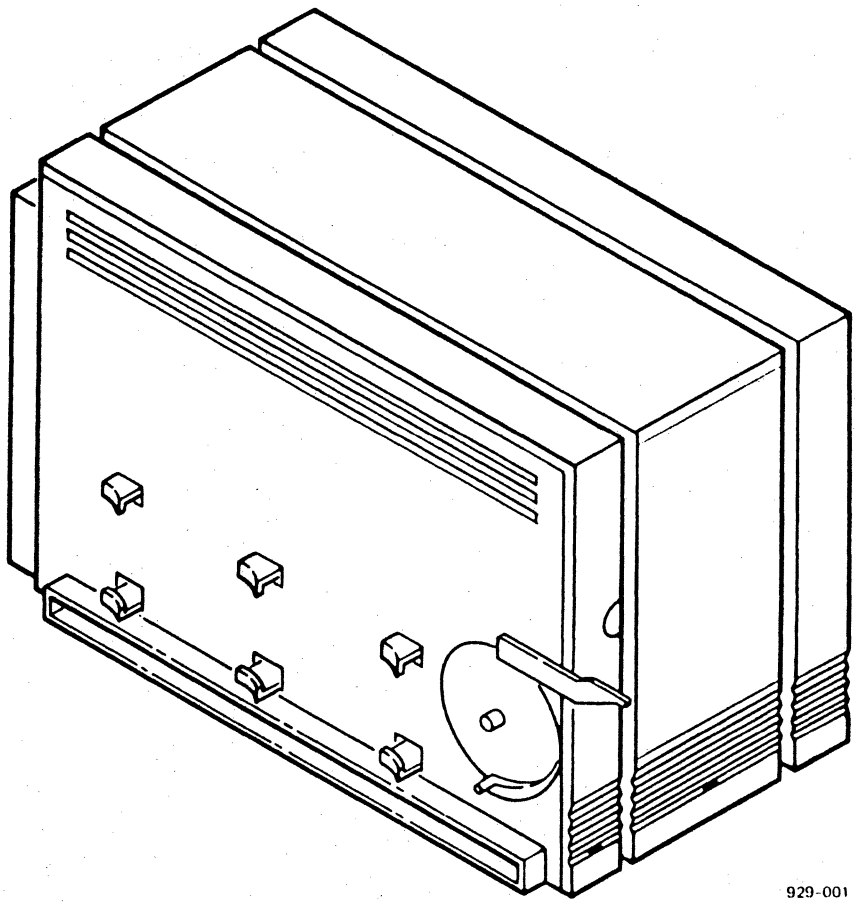


Figure 1-1. Quarter-Inch Cartridge Tape Module

MAJOR COMPONENTS

The major components of the QIC Tape Module include the following:

- o the enclosure, which houses the drive and the Tape Drive Control board
- o the Tape Drive Control board, mounted vertically on the left side of the enclosure (with module facing front)
- o one tape drive, mounted vertically in the enclosure
- o the motherboard, which lies on the bottom of the enclosure
- o two dc/dc power converters that plug into the motherboard, one supplying +12 Vdc and one supplying +5 Vdc

The major components used for tape drive control logic are on the Tape Drive Control board, and include

- o tape drive control circuitry
- o one X-Bus Gate Array, for the X-Bus interface
- o one 8253 programmable interval timer

2 ARCHITECTURE

INTRODUCTION

This chapter provides information for the systems programmer, engineer, or technician, who needs to understand the Quarter-Inch Cartridge (QIC) Tape Module hardware at a functional block level, and who must program the devices within the QIC Tape Module.

A functional block diagram is shown in Figure 2-1. Each block is described in this chapter in relation to the programmable device or devices performing the applicable function in the workstation. The nature of the function and how it is implemented is described. In addition, specific status and command registers are examined.

The following subjects are discussed:

- o X-Bus interface
- o tape control/status registers
- o tape drive read/write operation
- o tape drive command and status registers
- o tape drive control to tape drive interface
- o DMA transfer mode 3
- o ROM addressing
- o Module I/O address summary

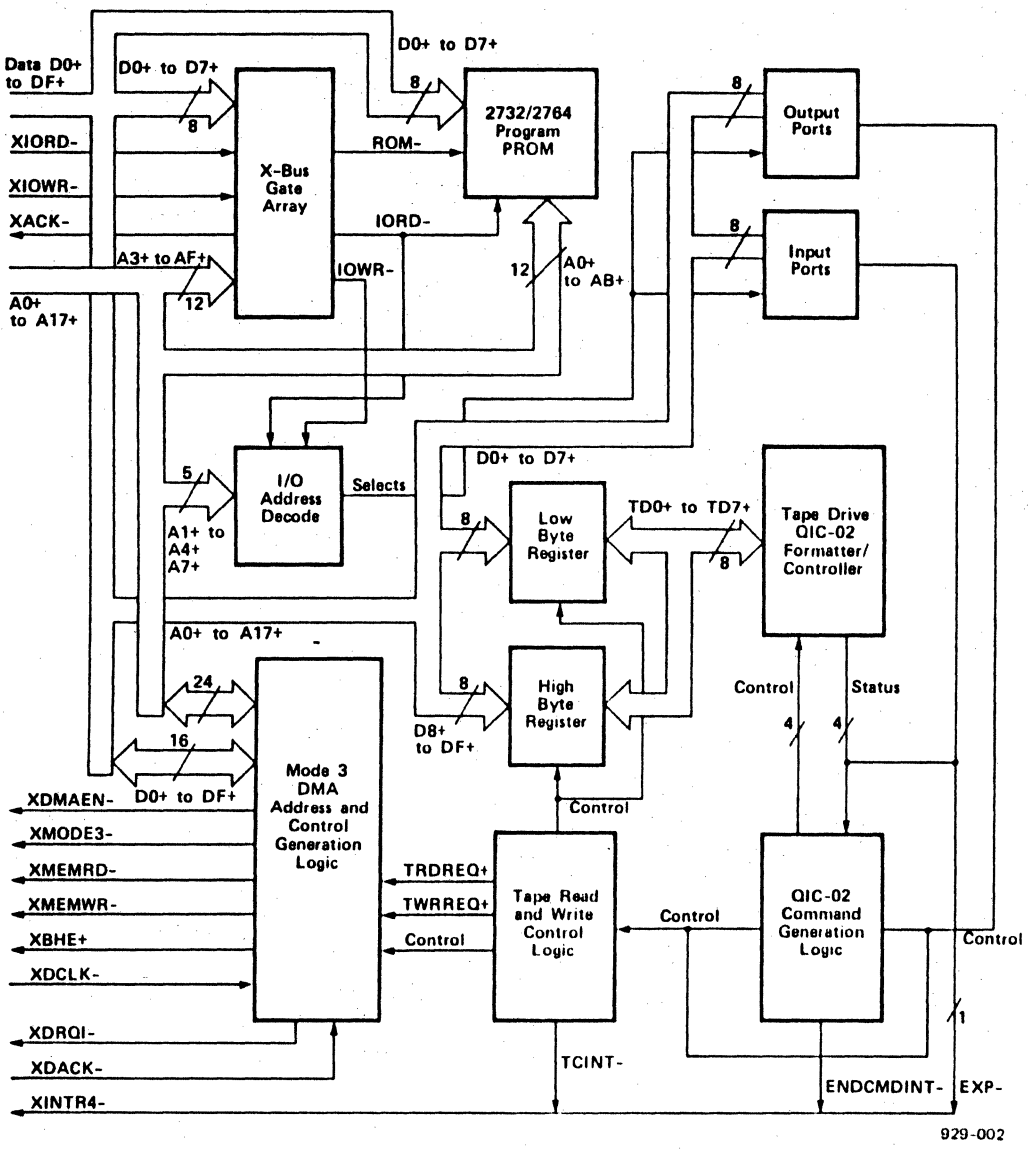


Figure 2-1. Quarter-Inch Cartridge Tape Module Functional Block Diagram

X-BUS INTERFACE

The I/O ports on the QIC Tape Module are partially defined by the module base I/O address issued by the Processor Module. For example, the Status register resides at port XX80h, where XX is the module address and 80h is the register address. Upon either a power-up or a manual reset, the bootstrap ROM program in the Processor Module assigns a unique I/O base address to each module that is physically attached to the X-Bus.

MODULE IDENTIFICATION

A power-up reset, manual (push-button) reset, or any I/O operation to specific ports in your Processor Module, resets all X-Bus modules except the Processor Module. Only the module immediately to the right of the Processor Module is enabled. This module identifies itself by placing a type/state word on the data bus when port Ø is read by the Processor Module.

The Processor Module writes to port Ø, a base I/O address that corresponds to a register in the module and defines the range of I/O addresses reserved for the module's use. Writing to port Ø also causes the module to reenable the X-Bus connection to the next module, and to ignore subsequent reads and writes to and from port Ø. This allows the Processor Module, to repeat the process for each module, beginning at the module adjacent to the Processor Module and repeating the process for each module to the right.

A ready timeout, signaled by a nonmaskable interrupt (NMI) when accessing port Ø, indicates that no additional modules are available.

IMPLEMENTATION

The module identification scheme is implemented by hardware as follows:

- All modules on the X-Bus are assigned an input signal line (XPIN) and are required to generate an output signal line (XPOUT). The input signal always enters a module on the module's left side, and the output signal always exits the module on the module's right side.

- During power-up, all modules reset an internal flip-flop to drive XPOUT low.

- The XPIN line of the module closest to the Processor Module is controlled by the Processor Module. When XPIN is low, the I/O register clears.

- When a module's XPIN is high and its XPOUT is low, the base I/O address is zero.

- The Processor Module reads port Ø to identify the module (in this case, the QIC Tape Module) and then writes a byte to the low-order eight bits of the data bus, which become the high-order eight bits of the module's I/O address range (256 byte-ports or 128 word-ports). This write also enables the XPOUT line in the module, which allows the next module on the right to undergo the same operation.

Eight-bit devices are not required to scan the high-order byte of a port. Therefore, the base I/O address is written to the low-order byte of port Ø. This corresponds to the high-order byte of the 16-bit base address, and defines a range of up to 256 port addresses reserved for the QIC Tape Module's use.

The Processor Module is always referred to as module Ø, the first module to the right of the Processor Module is referred to as module 1, and so on. The bootstrap ROM always writes this module number to the low byte of port Ø when it performs the identification polling sequence. Therefore, the module to the right of the Processor Module uses I/O ports Ø1ØØh through Ø1FFh, the next module to the right uses ports Ø2ØØh through Ø2FFh, and so on, depending on how many modules are used. The bootstrap ROM also builds an array of the module type/state words returned by each module, and stores this table in memory for the system.

TAPE CONTROL/STATUS REGISTERS

The following registers are described in detail:

- Read Tape Control registers
- Write Tape Control registers
- Read Tape Line Status registers

READ TAPE CONTROL REGISTER (XX82h)

Data Bit	Function
Ø	Tape Reset (TRESET+). Resets the tape drive when asserted for at least 2Ø microseconds. This signal is the inverted RESET- of the drive.
1	Tape On Line (TONLINE+). This signal is the inverted ONLINE- signal of the drive.
2 to 4	Reserved.

Data Bit	Function
5	Tape Write Operation (TPWROP+). When high, it enables the tape write operation.
6	Tape Read Operation (TPRDOP+). When high, it enables the tape read operation.
7	Tape Select (TSEL+). Tape selected light on the motherboard and interrupt enabled.

WRITE TAPE CONTROL REGISTER (XX82h)

Data Bit	Function
Ø	Tape Reset (TRESET+). Resets the tape drive when asserted for at least 2Ø microseconds. This signal is the inverted RESET- of the drive.
1	Tape On Line (TONLINE+). This signal is the inverted ONLINE- signal of the drive.
2 to 4	Reserved.
5	Tape Write Operation (TPWROP+). When high, it enables the tape write operation.
6	Tape Read Operation (TPRDOP+). When high, it enables the tape read operation.
7	Tape Select (TSEL+). Tape selected light on the motherboard and interrupt enabled.

READ TAPE LINE STATUS REGISTER (XX84h)

Data Bit	Function
Ø	Tape Acknowledge (TACK+). Reflects the inverted ACKNOWLEDGE- signal of the tape drive.
1	Tape Ready (TREADY+). Reflects the inverted READY- signal of the drive.
2	Tape Exception (TEXP+). Reflects the inverted EXCEPTION- signal of the drive.
3	Tape Direction (TDIRC+). Reflects the DIRECTION- signal of the drive.
4	Terminal Count Interrupt (TCINT+). When set, TCINT+ signals that terminal count is reached in the read/write operation.
5	End of Command Interrupt (ENDCMDINT+). When set, ENDCMDINT+ signals the completion of a command.
6	Reserved.
7	Reserved.

INTERRUPT CLEAR REGISTER (PORT XX88h)

A write to this register with any value clears the interrupt condition bits TCINT+ (bit 4) and ENDCMDINT+ (bit 5) in the Read Tape Line Status register (XX84h).

TAPE DRIVE READ/WRITE

READING DATA FROM TAPE TO PROCESSOR MODULE

The sequence to issue the read command is as follows:

1. The Processor Module sets up the DMA word address by writing the 23-bit word address to the DMA Address registers (ports XX8Ah, XX8Ch, and XX8Eh).

2. Timer counter Ø (port XX90h) is set by the Time Mode Control register (port XX96h) to mode Ø (interrupt on terminal count) and loaded with the value of the number of bytes in a multiple of 512 bytes to be transferred, minus one byte.

3. TSET+, TONLINE+, TSEL+, and TPRDOP+ bits are set in the Tape Control register (port XX82h).

4. Assertion of TREADY+ is checked in the Tape Line Status register (port XX84h).

5. Command byte 80h is issued to the Tape Command Byte register (port XX80h).

6. The Processor Module waits for an interrupt for completion of the read operation.

8. Upon interrupt, the Tape Line Status register (port XX84h) is read for the interrupt condition.

9. The TSEL+ bit in the Tape Control register (port XX82h) is reset to free the X-Bus interrupt line.

10. A write is performed to the Clear Pending Interrupt register (port XX88h) to clear the interrupt.

11. The TPRDOP+ bit in the Tape Control register (port XX82h) is reset to inhibit erroneous read on tape.

12. If the TEXP+ interrupt in the Tape Line Status register (port XX84h) is asserted, a file mark is encountered. Operation is terminated by issuing a read status command.

13. If TCINT+ interrupt in the Tape Line Status register (port XX84h) is not asserted, an error exit routine is performed.

14. If not the last buffer block, then go to step 16.

15. The Processor Module may deassert TONLINE+ in the Tape Control register (port XX82h). Either a Read File Mark or another Read Data command is issued. End.

16. The Processor Module waits for TREADY+, which signals that the drive is ready for the next data block.

17. The address counters and timer counter 0 are reloaded with the value of bytes in a multiple of 512 bytes to be transferred, minus two bytes.

18. TPRDOP+ is set to continue the read operation. TSEL+ is set to enable the interrupt and light the LED.

19. Go to 6.

WRITING DATA FROM THE PROCESSOR MODULE TO TAPE

The sequence to issue the write command is as follows:

1. The Processor Module sets up the DMA word address by writing the 23-bit addresses to the DMA Address registers (ports XX8Ah, XX8Ch, XX8Eh).

2. Timer counter Ø (port XX9Øh) is set by the Timer Mode Control register (port XX96h) to mode Ø (interrupt on terminal count) and loaded with the value of the number of bytes to be transferred in a multiple of 512 bytes, minus one byte.

3. Timer counter 1 (port XX92h) is set by the Timer Mode Control register (port XX96h) to a programmable one-shot mode 1, and loaded with 51Ø bytes (512 bytes minus two).

4. TSET+, TONLINE+, TSEL+, and TPWROP+ bits are set in the Tape Control register (port XX82h).

5. TREADY+ for drive ready is checked in the Tape Line Status register (port XX84h).

6. Command byte 4Øh is issued to the Tape Command Byte register (port XX8Øh).

7. The Processor Module waits for an interrupt for completion of the write operation.

8. Upon interrupt, the Tape Line Status register (port XX84h) is read to verify the existence of TCINT+.

9. The TSEL+ bit in the Tape Control register (port XX82h) is reset.

10. A write to the Clear Pending Interrupt register (port XX88h) is performed to clear the interrupt condition.

11. The TPWROP+ bit in the Tape Control register (port XX82h) is set to inhibit an erroneous write to tape.

12. If not the last buffer block, then go to step 16.

13. The Tape Line Status register (port XX84h) is read, and there is a wait for TREADY+.

14. The Processor Module may either issue a Write File Mark command or reset TONLINE+ to terminate the Write Data to Tape operation.

15. End.

16. To continue writing from the buffer, the address counters and the timer counter Ø are loaded with the number of bytes to be transferred, minus one byte.

17. TPWROP+ is set to restart the tape write operation. TSEL+ is set to enable the interrupt and LED.

18. Go to 7.

COMMAND AND STATUS REGISTERS

READ TAPE STATUS BYTE REGISTER (PORT XX80h)

Six bytes are read from this register; bytes Ø through 5.

BYTE Ø

Data bit functions of this register are as follows:

Data Bit	Function
Ø	File Mark Detected. Tape control circuitry sets this bit when it detects a file mark during a Read Data or Read File Mark operation. A Read Tape Status sequence resets the bit.
1	Block-in-Error Not Located. The tape control circuitry sets this bit when an unrecoverable read error occurs and the control circuitry cannot confirm that the last block transmitted was the block in error. A Read Tape Status sequence resets the bit.
2	Unrecoverable Data Bit Error. The tape control circuitry sets this bit when a hard error occurs during a read or write operation. A Read Tape Status sequence resets the bit.
3	End of Media. The tape control circuitry sets this bit when it detects the logical early warning hole of the last track during a write operation. A Read Tape Status sequence resets the bit.

Data Bit	Function
4	Write Protect. The tape control circuitry sets this bit if the cartridge write protect plug is set in the file's protect position. Changing the plug position resets the bit.
5	Drive Not Online. The tape control circuitry sets this bit if the drive is not physically connected or is not receiving power.
6	Cartridge Not in Place. The tape control circuitry sets this bit if a cartridge is not fully inserted into the drive.
7	Exception Byte Ø. This bit is set if any of the other bits in status byte Ø are set.

BYTE 1

Data bit functions of this register are as follows:

Data Bit	Function
Ø	Reset/Power-Up Occurred. The tape control circuitry sets this bit after the Processor Module issues a reset, or when the QIC Tape Module is powered up. A Read Tape Status sequence resets the bit.
1	End of recorded data.
2	Parity error on data bus.

Data Bit	Function
3	Beginning of Media. The tape control circuitry sets this bit when the cartridge is at the beginning of tape. This bit is reset when the drive leaves the beginning of the tape.
4	Eight or more retries.
5	No Data Detected. The tape control circuitry sets this bit when an unrecoverable data error occurs due to lack of recorded data. This occurs when the QIC Tape Module does not detect a data block within a tape control circuitry timeout. A Read Tape Status sequence resets the bit.
6	Illegal Command. The tape control circuitry sets this bit if any of the following conditions occur: o the Processor Module asserts ONLINE- when a data transfer command is received o the Processor Module sends a command other than Write or Write File Mark during a write operation o the Processor Module sends a command other than Read or Read File Mark during a read operation o the Processor Module sends a Select command when the cartridge in the drive is not at the beginning of the tape
7	Exception byte 1.

BYTE 2

Tape status byte 2 is the most significant byte, with a soft-error count.

BYTE 3

Tape status byte 3 is the least significant byte, with a soft-error count.

BYTE 4

Tape status byte 4 is the most significant byte, with a buffer-underrun count.

BYTE 5

Tape status byte 5 is the least significant byte, with a buffer-underrun count.

WRITE TAPE COMMAND BYTE REGISTER (XX80h)

Bytes of this Write register can be configured for one of the following:

Command	Data Bits 7	6	5	4	3	2	1	Ø
Select Drive	Ø	Ø	Ø	1	Ø	Ø	Ø	1
Beginning of Tape	Ø	Ø	1	Ø	Ø	Ø	Ø	1
Erase Tape	Ø	Ø	1	Ø	Ø	Ø	1	Ø
Retension	Ø	Ø	1	Ø	Ø	1	Ø	Ø
Read Data	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Read File Mark	1	Ø	1	Ø	Ø	Ø	Ø	Ø
Write Data	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø
Write File Mark	Ø	1	1	Ø	Ø	Ø	Ø	Ø
Read Tape Status	1	1	Ø	Ø	Ø	Ø	Ø	Ø

CONTROL CIRCUITRY TO TAPE DRIVE INTERFACE

Communication between the Tape Drive Control board and the tape drive takes place through the tape drive interface, which consists of the following:

- four control lines from the Processor Module
- four control lines from the tape drive
- the 8-bit bidirectional data bus

For detailed information on the tape drive interface, see the manufacturer's tape drive manual in Chapter 4, "Drive Specifications."

DMA TRANSFER MODE 3

DIRECT MEMORY ACCESS

Direct memory access (DMA) transfer operations are bus operations that access data differently than the conventional master/slave I/O or memory operations. DMA transfer operations allow other bus masters besides the Processor Module to independently access the buses and support data transfers without direct program control. Bus masters can retain the bus for more than one cycle at a time. The X-Bus has four DMA transfer modes, mode Ø through mode 3. Since the QIC Tape Module uses only mode 3, only mode 3 is described here. For information about modes Ø through 2, see the Processor Manual for your system.

MODE 3

During a mode 3 transfer, the Processor Module only provides the arbitration for bus acquisition signals. The requesting module, which must be a master, generates the control and addresses. Mode 3 is only valid on DMA channels 1 through 3 of the Processor Module; however, more than one mode 3 master may share the same data transfer channel. The QIC Tape Module uses DMA channel 1.

The data requests and acknowledges are daisy-chained through priority arbitration logic. When the Processor Module asserts XDACK- (X-Bus DMA Acknowledge), each mode 3 module determines if it has a valid request. If the applicable mode 3 module has asserted X-Bus DMA Request (XDRQ-), then it controls the channel and inhibits X-Bus DMA Acknowledge (XDACK-) for the next X-Bus mode 3 master module downstream. If no request is pending for the applicable module, the mode 3 master module asserts XDACK- for the next module on the X-Bus.

ROM ADDRESSING

The ROM address is mapped in the module memory address by writing I/O address XX1Øh with bit 2 of the data bus set. Input/output address XX2Øh is the memory select register, which is loaded with ØØh through ØFh, specifying a 1M-byte X-Bus window that can be used for ROM.

The following is an example of how to read the bootstrap ROM when connected to a Processor Module with an 8Ø186 CPU:

- Write a value of ØC038h to the 8Ø186 CPU upper memory chip select (UMCS) address ØFFAØh to specify a 256K-byte memory block size.

- Write a value of 2880h to port ØFAØØh, the Extended Address register (EAR) of the Processor Module, to set to the fifth 1M-byte boundary with a window size of 224K.

- Output byte value 5 to port XX2Øh, and set the EAR of the X-Bus Gate Array to respond to the fifth 1M-byte boundary.

- Output byte value 4 to port XXØAh for boot enable.

- Read the bootstrap ROM contents starting from address ØCØØØØh.

MODULE I/O ADDRESS SUMMARY

A summary of the I/O ports defined for the QIC Tape Module is provided in Table 2-1. Port number, input information, and output information are listed.

Table 2-1. I/O Address Summary (Page 1 of 2)

Port No. (h)	Read	Write
XX8Ø	Tape Status Byte register	Tape Command Byte register
XX82	Tape Control register	Tape Control register
XX84	Tape Line Status register	---
XX86	---	---
XX88	---	Clear Pending Interrupt register
XX8A	---	DMA Low 8 Address Bits register
XX8C	---	DMA Middle 8 Address Bits register
XX8E	---	DMA High 8 Address Bits register

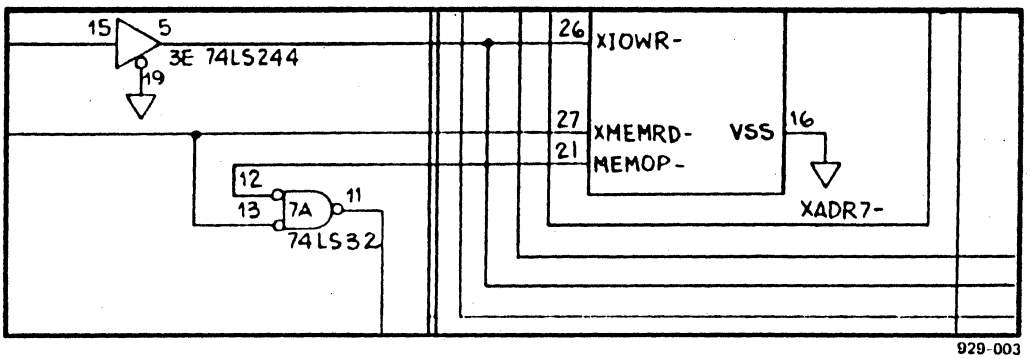
Table 2-1. I/O Address Summary (Page 2 of 2)

Port No. (h)	Read	Write
XX90	Timer Counter 0 register	Timer Counter 0 register
XX92	Timer Counter 1 register	Timer Counter 1 register
XX94	Timer Counter 2 register	Timer Counter 2 register
XX96	---	Timer Mode Control register

3 THEORY OF OPERATION

This chapter, which provides detailed component-level descriptions of the hardware incorporated in the Quarter-Inch Cartridge (QIC) Tape Module, is directed to the engineer who needs to understand the QIC Tape Module at the component level. Each functional block is described in relation to the logic that performs the function. Schematic windows are provided on each applicable page to supplement the text. In addition, a complete set of schematic drawings is provided in Appendix B.

Each schematic window represents an applicable portion of the schematic diagram. The page of the schematic diagram and location (coordinate) within that page is provided below each window, as shown in the following example:



(From Figure B-1, Page 2, Coordinate 8B.)

This window comes from the second page of the schematic drawing in Figure B-1 (Appendix B). The exact location, taken from the top left corner of the window, is at coordinate 8B.

CIRCUIT DESCRIPTIONS

Detailed component-level circuit descriptions are given for the following:

- o X-Bus Gate Array
- o tape drive operation
- o mode 3 DMA
- o tape drive interface logic
- o 8253 programmable interval timer
- o power supplies

X-BUS GATE ARRAY

The X-Bus Gate Array at 5E is used for the following:

- o module identification
- o I/O read and I/O write
- o Bootstrap requests from the CPU

The pin assignments and functions of the X-Bus Gate Array are listed in Table 3-1.

Table 3-1. X-Bus Gate Array Pin Assignments and Functions (Page 1 of 5)

Pin	Function
1	**Reset (RESET-).** Low true input initializes the device and suspends all operations.
2 to 5	**X-Bus Address Bus (XADR14- through XADR17-).** Low true input reflects the module memory base address.
6 to 9	**Data Bus (DAT7+ through DAT4+).** High true input reflects data to be written into the X-Bus Gate Array when the proper control signals are valid.
10 to 12	**Data Bus (DAT3+ through DAT0+).** Bidirectional, high true data bits reflect data to be written into or read from the X-Bus Gate Array when the proper control signals are valid.
14	**Oscillator Resistor (OSCRES+).** High true output pin is used for connection of a timing resistor for the on-chip oscillator.
15	**Oscillator Return (OSCRET+).** High true input pin is used for connection of the oscillator RC network through a protection resistor.

Table 3-1. X-Bus Gate Array Pin Assignments and Functions (Page 2 of 5)

Pin	Function
16	**Power (VSS-).** This input is a power connection required by the X-Bus Gate Array.
17	**Oscillator Capacitor (OSCCAP+).** High true output pin is used for connection of a timing capacitor for the on-chip oscillator.
18	**Acknowledge (ACK+).** High true output indicates to the X-Bus that the data has been transferred and the bus cycle can be terminated. ACK+ is generated only for I/O operations and ROM reading.
19	**I/O Read (IORD-).** Low true output read strobe is generated by the X-Bus Gate Array only if the module is selected for an I/O read operation.
20	**I/O Write (IOWR-).** Low true output write strobe is generated by the X-Bus Gate Array only if the module is selected for an I/O write operation.
21	**Memory Operation (MEMOP-).** Low true output indicates the module is selected for a memory operation.

Table 3-1. X-Bus Gate Array Pin Assignments and Functions (Page 3 of 5)

Pin	Function
22	**ROM Enable (ROM-).** Low true output enables the ROM device.
23	**X-Bus Priority Out (XPOUT+).** Positive true output is a daisy-chained signal that allows the next module to initialize.
24	**Identification Enable (IDEN-).** Low true output signifies that DMA is active on the X-Bus.
25	**X-Bus I/O Read (XIORD-).** Low true input indicates that an I/O read operation is to be performed on the X-Bus. This signal is used in conjunction with the XADR8- through XADRF- lines to determine if the I/O operation is for the module.
26	**X-Bus I/O Write (XIOWR-).** Low true input indicates that an I/O write operation is to be performed on the X-Bus. This signal is used in conjunction with the XADR8- through XADRF- lines to determine if the I/O operation is for the module.

Table 3-1. X-Bus Gate Array Pin Assignments and Functions (Page 4 of 5)

Pin	Function
27	**X-Bus Memory Read (XMEMRD-).** Low true signal indicates that a memory read operation is to be performed on the X-Bus. This signal is used only to enable the CPU to read the module ROM.
28	**Load Address Enable (LOADEN+).** High true input allows access to the on-chip locations (memory select registers and ROM shadow bit). When this input is high, these two functions are not decoded and the I/O operation is intended for external devices. When LOADEN- is low, XADR3- and XADR5- decode the I/O operation as follows:

XADR3-	XADR5-	I/O Operation
Ø	Ø	External
1	Ø	ROM shadow bit
Ø	1	Memory Select register
1	1	External

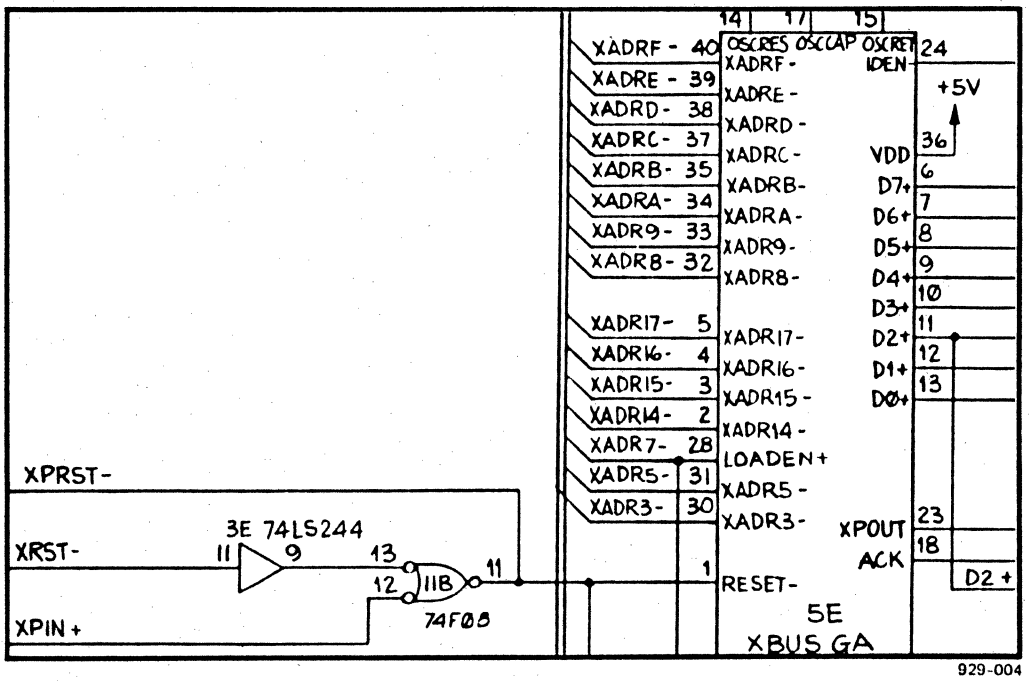
Table 3-1. X-Bus Gate Array Pin Assignments and Functions (Page 5 of 5)

Pin	Function
29	**X-Bus DMA Enable (XDMEN-).** Low true input indicates that the DMA is active on the X-Bus.
30 to 31	**X-Bus Address Bus (XADR3- and XADR5-).** Low true inputs. (See pin 28 above.)
32 to 35	**X-Bus Address Bus (XADR8- through XADRB-).** Low true inputs. XADR8- through XADRF- reflect module I/O base address, except during initialization.
36	**Power (VDD+).** This input is a power connection required by the X-Bus Gate Array.
37 to 40	**X-Bus Address Bus (XADRC- through XADRF-).** Low true inputs. (See pins 32 to 35 above.)

MODULE IDENTIFICATION

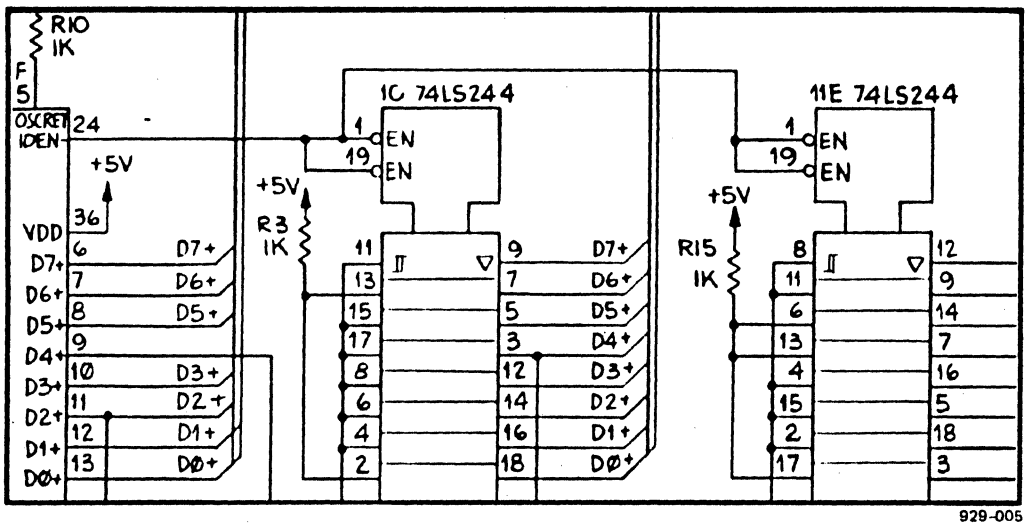
Base addresses for the various I/O ports and registers are assigned by the Processor Module when a power-up or manual reset occurs on the X-Bus as XRST- (X-Bus Reset), or when XPIN+ (X-Bus Priority In) is reset low, signifying that activity on the X-Bus for the QIC Tape Module is suspended.

As shown in the following window, XRST-, connecting from J1, pin 88, is buffered at 3E (pin 9) and driven through gate 11B to the X-Bus Gate Array (5E). Resetting 5E clears all the internal registers. After reset, the Processor Module performs a read, and since the X-Bus Gate Array is clear, it responds to I/O port address, location Ø.



(From Figure B-1, Page 2, Coordinate 8D.)

When XIORD- (X-Bus I/O Read) is low, 5E generates a low at pin 24 (IDEN-), enabling 1C and 11E. The data from the input of 1C and 11E is transferred to the data bus DØ+ through D7+, and D8+ through DF+.



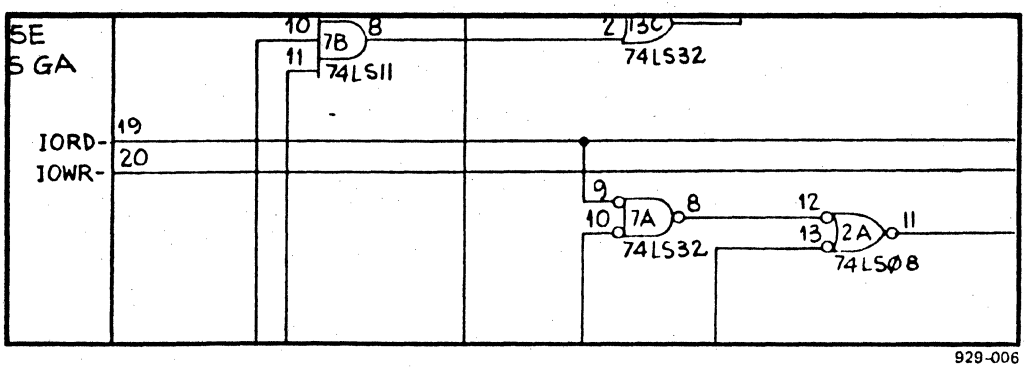
(From Figure B-1, Page 2, Coordinate 6D.)

The identification codes are as follows:

- high byte 31 (which is the QIC Tape Module identification type)
- low byte 41 (which means this is a bootable device, the boot ROM can be read through DMA channel Ø, and can support a non-8Ø186 CPU)

Module Identification Read

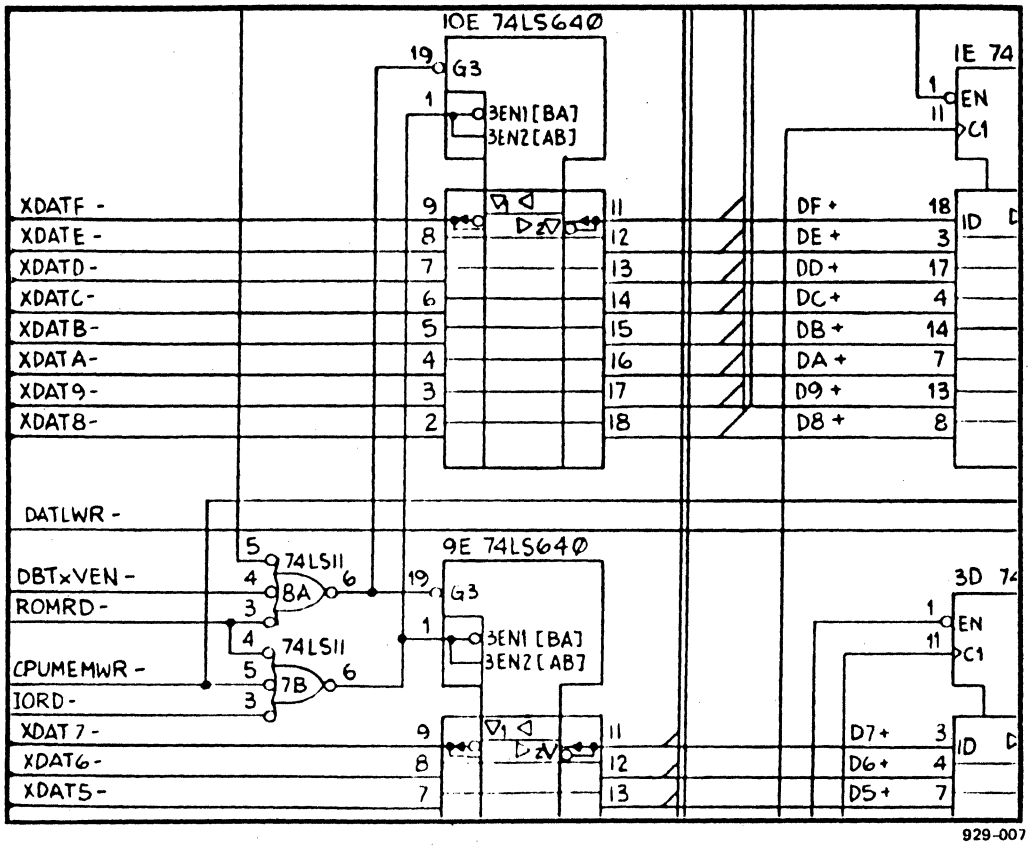
Pin 19 of 5E (IORD-) is a modifier signal that is enabled and goes to pin 9 of 7A.



(From Figure B-1, Page 2, Coordinate 6C.)

When pin 8 of 7A is low, the output of 2A (pin 11) is low. The signal coming from pin 11 is DBTXVEN- (Data Bus Transceiver Enable), which enables data bus transceivers, 9E and 1ØE.

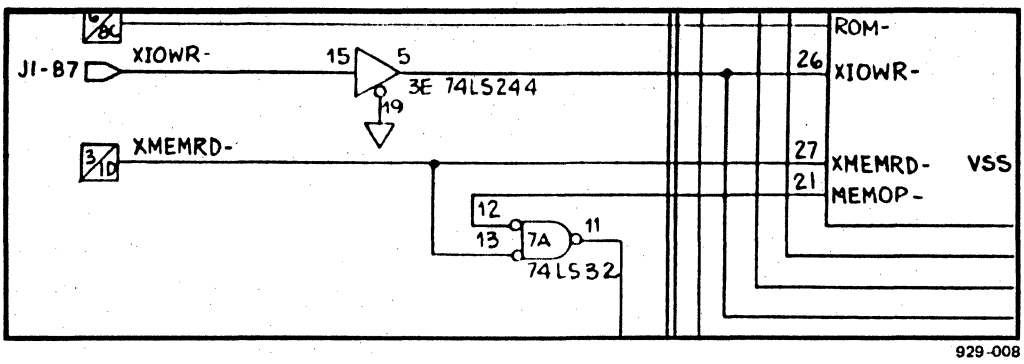
Since pin 4 of 8A is low, pin 19 of both 9E and 1ØE are low. The direction is controlled by pin 1 of 9E and 1ØE, which are tied to pin 6 of 7B. IORD- (from pin 19 of 5E) is low and goes to AND gate 7B, forcing pin 6 of 7B low, and thus pin 1 of 9E and 1ØE are also low, enabling the direction of the data to flow to the CPU.



(From Figure B-1, Page 4, Coordinate 8D.)

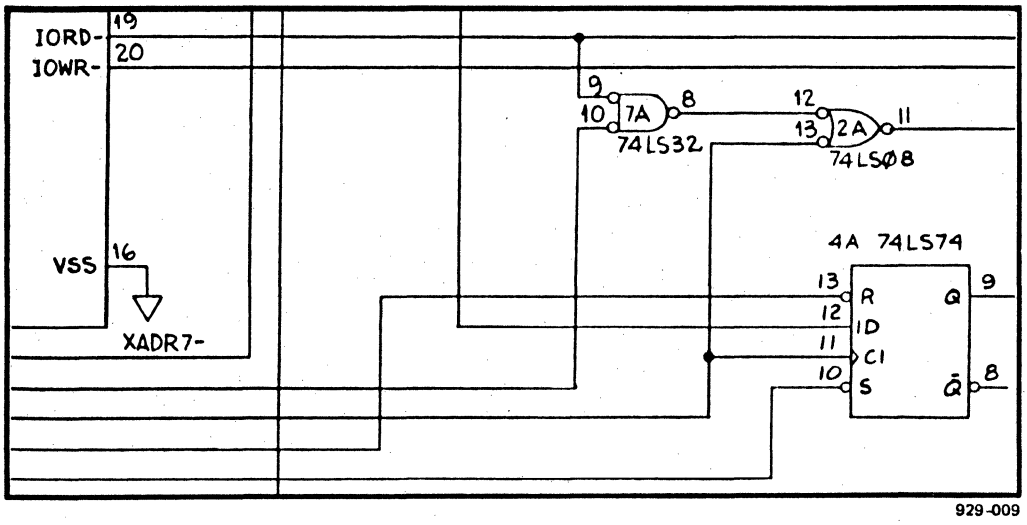
Module Identification Write

After the Processor Module reads the identification code of 31 and 41, it writes to port 0, an internal register of the X-Bus Gate Array (the value of the base address of the module it selected).



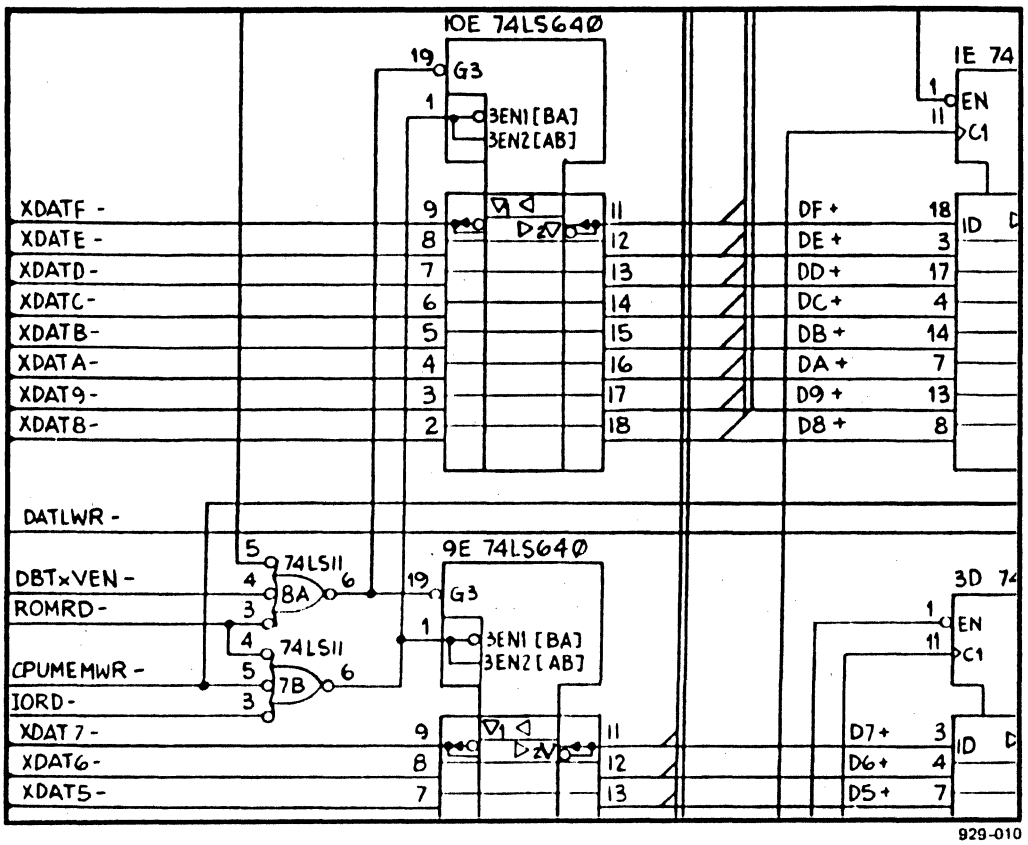
(From Figure B-1, Page 2, Coordinate 8C.)

As shown above, XIOWR- from J1-87 is asserted and buffered through pin 5 of 3E to pin 13 of AND gate 2A (pin 13). Pin 11 of 2A (DBTXVEN-) goes low and enables transceivers 9E and 10E.



(From Figure B-1, Page 2, Coordinate 6C.)

Since this is not a read operation, pin 6 of 7B remains high. As shown in the following window, pin 1 of 9E, and pin 1 of 10E are high, enabling data to be transferred from the X-Bus data bus to the X-Bus Gate Array.

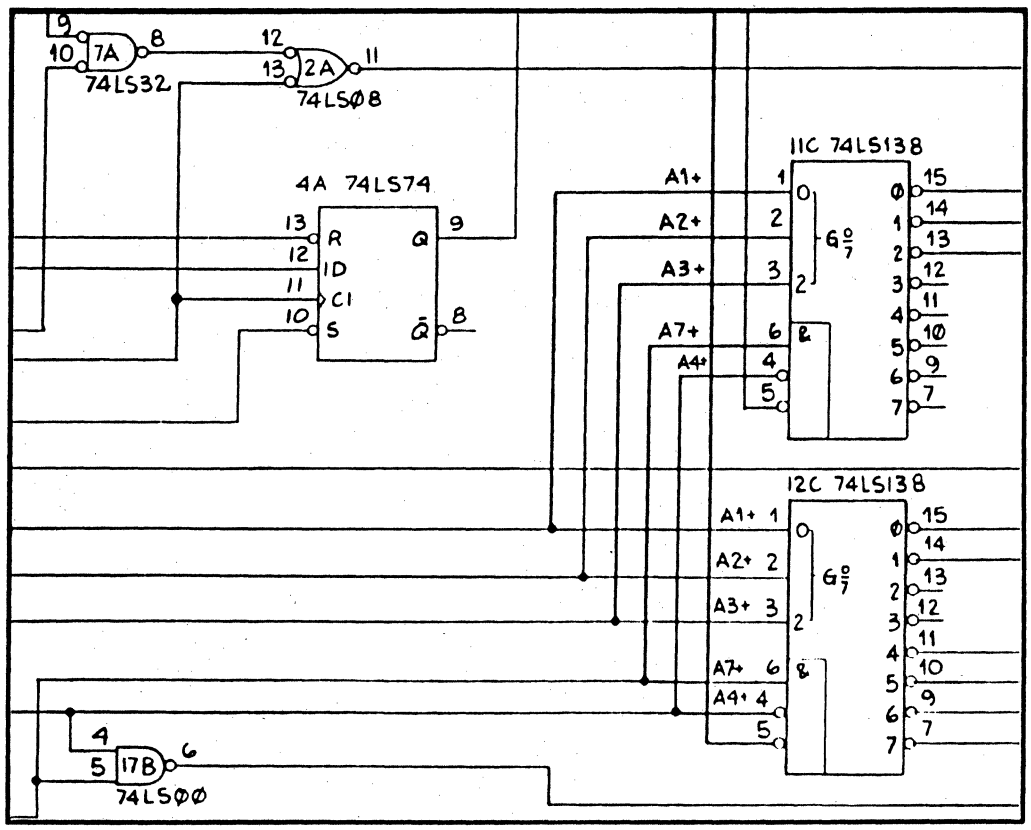


(From Figure B-1, Page 4, Coordinate 8D.)

I/O READ AND WRITE

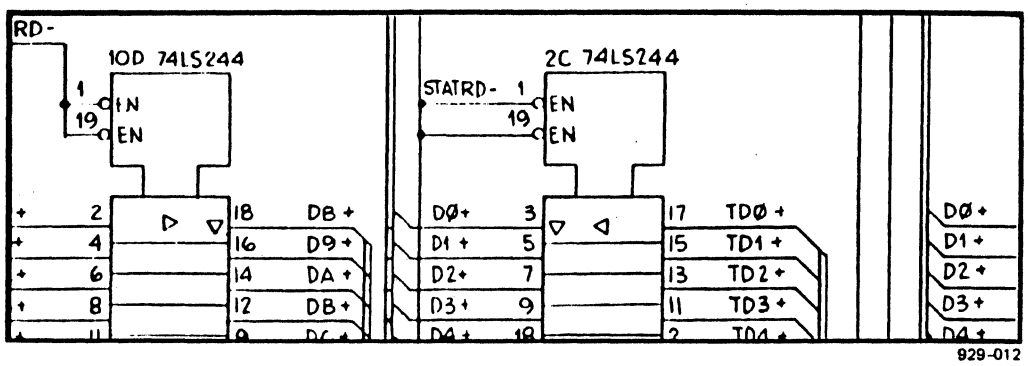
Decoders 11C and 12C decode the proper I/O addresses for various I/O ports. Decoder 11C is used for input read, and decoder 12C is used for output write. The select and enable lines of the decoders are connected to the address lines A1+

through A4+, and A7+. The range of the output-decoded address is from XX8Ø through XX8E. The timer chip select enable is connected to pin 6 of 17B, which is enabled when A4+ and A7+ are high. Thus, the timer responds to address space XX9Ø.



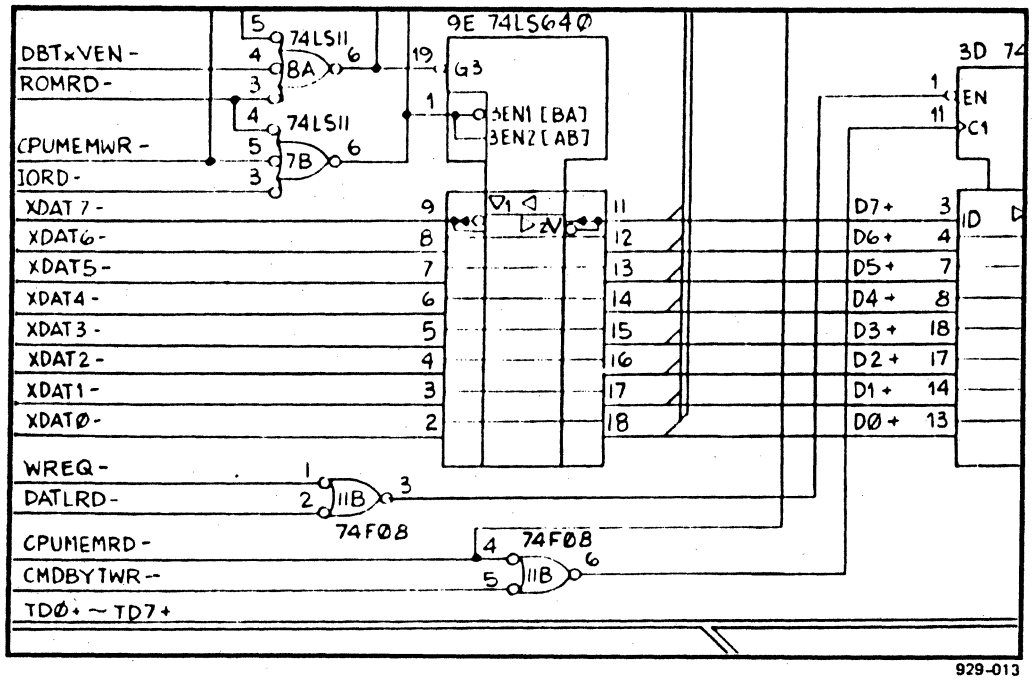
(From Figure B-1, Page 2, Coordinate 5C.)

The X-Bus Gate Array compares the module base address and generates a low signal at pin 19 of 5E (IORD-), enabling pin 5 of 11C. At the same time, a low enable signal is generated at pin 15 of 11C. Since pin 15 is connected to pins 1 and 19 of 2C, the 8-bit data on the TDØ+ through TD7+ bus is sent to the CPU through transceiver 9E.



(From Figure B-1, Page 6, Coordinate 6D.)

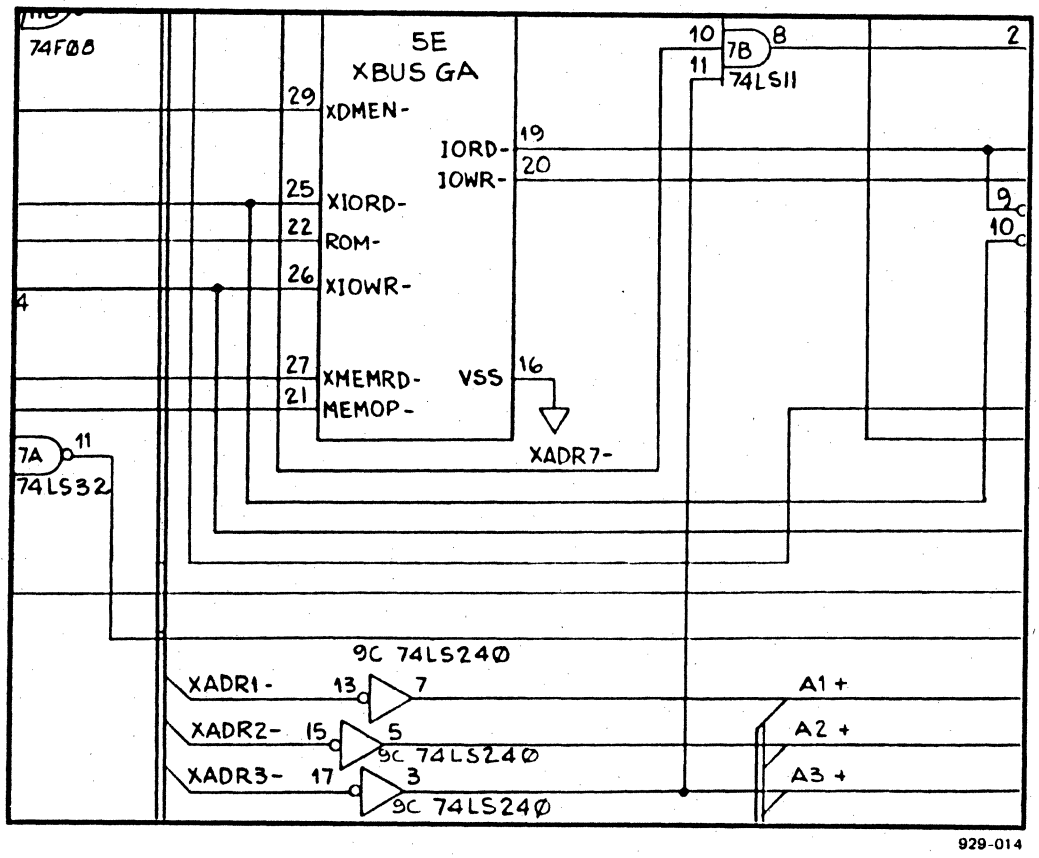
In a write operation, pin 2Ø of 5E is enabled, which means that pin 5 of 12C is also enabled. A low signal is generated at pin 15 of 12C. The data is latched to register 3D at the trailing edge of the IOWR-. IOWR- is modified from XIOWR- to provide the proper address setup time and data hold time.



(From Figure B-1, Page 4, Coordinate 8C.)

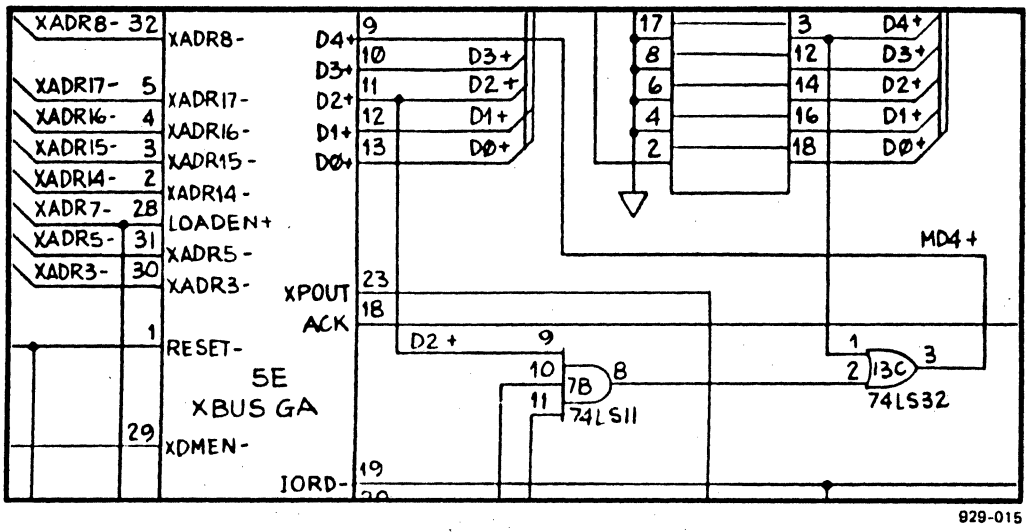
BOOTSTRAP REQUESTS FROM THE CPU

When the CPU boots from the tape, it asserts boot bit D2 (pin 11 of 5E) to port XXØAh. XX is the base address assignment the CPU gives to a particular module. When bit D2 is enabled, pin 9 of 7B is high. Since the CPU is writing to the X-Bus Gate Array at XXØAh, XADR7- is not asserted at pin 28 of the X-Bus Gate Array, and thus it is high. Pin 17 of 9C (XADR3-) is asserted and inverted at pin 3 of 9C. Pin 11 of 7B (A3+) is set to 1 and enabled.



(From Figure B-1, Page 2, Coordinate 7C.)

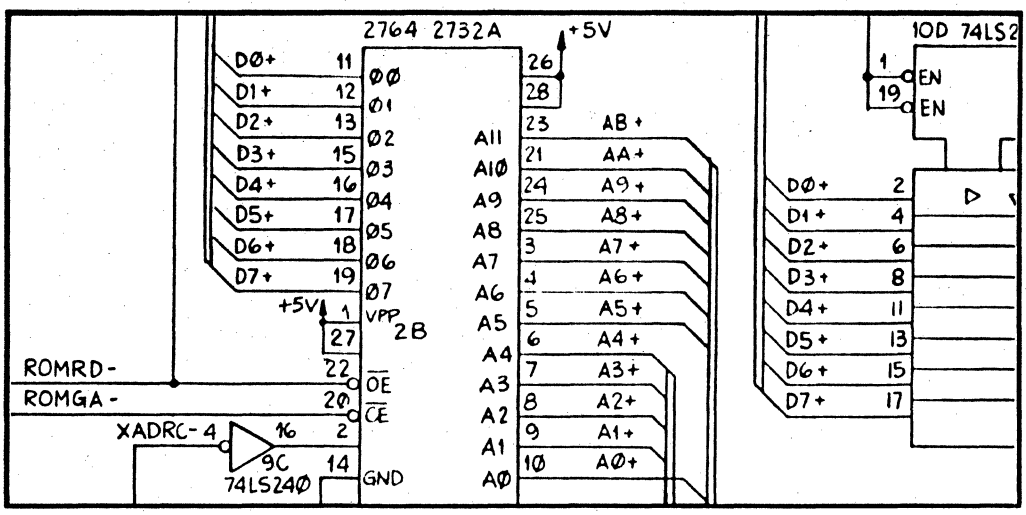
When D2+ is set to 1, pin 8 of 7B and pin 3 of 13C are also set to 1, indicating at pin 9 of 5E that there is a boot enable. When there is no boot enable, data bit D4+ goes through pin 1 of 13C to pin 3 of 13C, and then back to pin 9 of the X-Bus Gate Array.



(From Figure B-1, Page 2, Coordinate 6C.)

CPU ROM Read

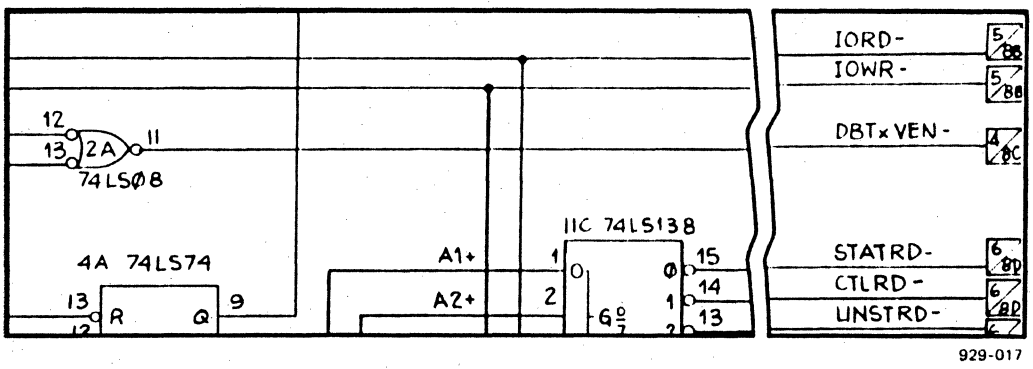
The CPU bootstrap ROM in the Processor Module does not have the code to boot from the tape. The program in the 2732A EPROM (2B) contains instructions for the CPU to boot from the tape. The CPU reads the bootstrap program into its memory and then executes the program.



929-016

(From Figure B-1, Page 6, Coordinate 8D.)

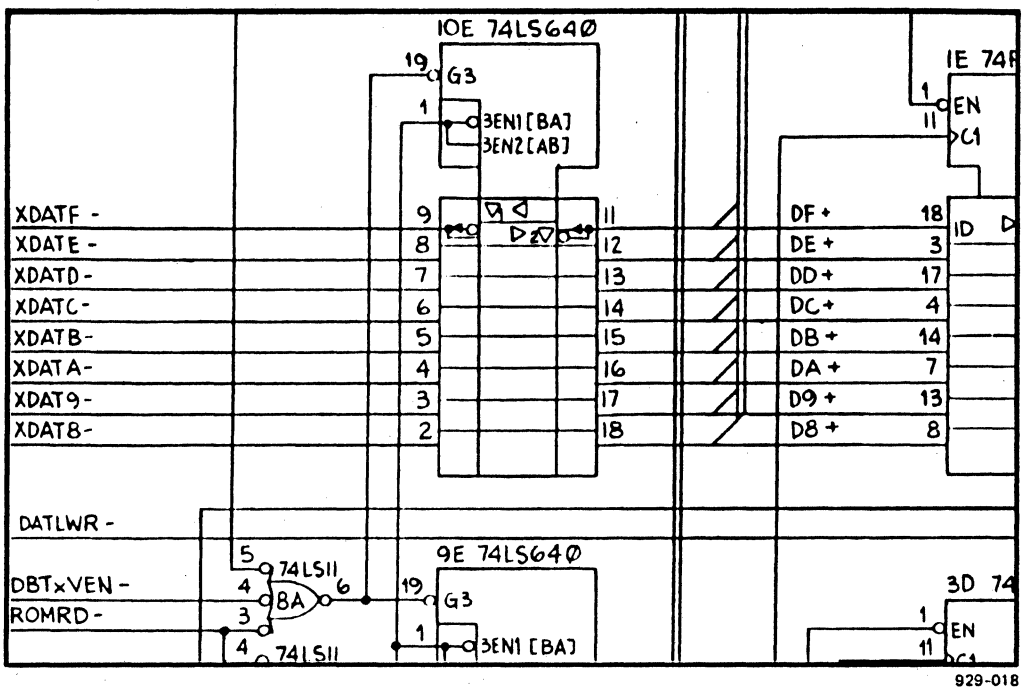
After setting the proper X-Bus window, the CPU performs an I/O read to the ROM. IORD- is asserted, which enables transceivers 9E and 10E. 2A (pin 11) enables DBTXVEN- (data bus transceiver enable).



929-017

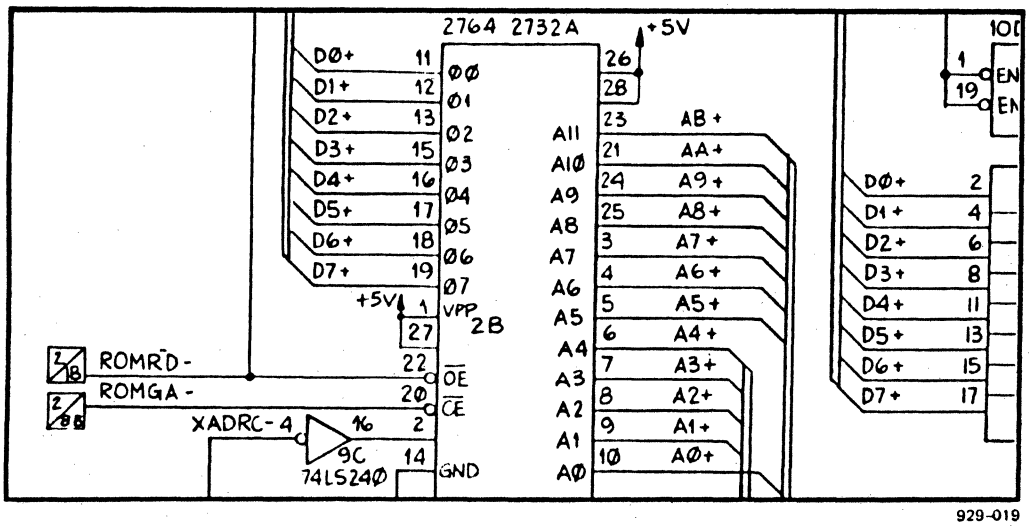
(From Figure B-1, Page 2, Coordinate 4C.)

DBTXVEN- is now low, enabling transceivers 9E and 10E, which provide the data for an I/O operation.



(From Figure B-1, Page 2, Coordinate 4C.)

The X-Bus Gate Array (5E) asserts the ROM at pin 20 of 2B, which is the CS- (Chip Select) pin. During the I/O read cycle, 5E also enables MEMOP- (Memory Operation) at pin 21 to read data from the ROM. Once the content of the ROM is loaded into the CPU, the CPU can execute the code read from the 2732A.

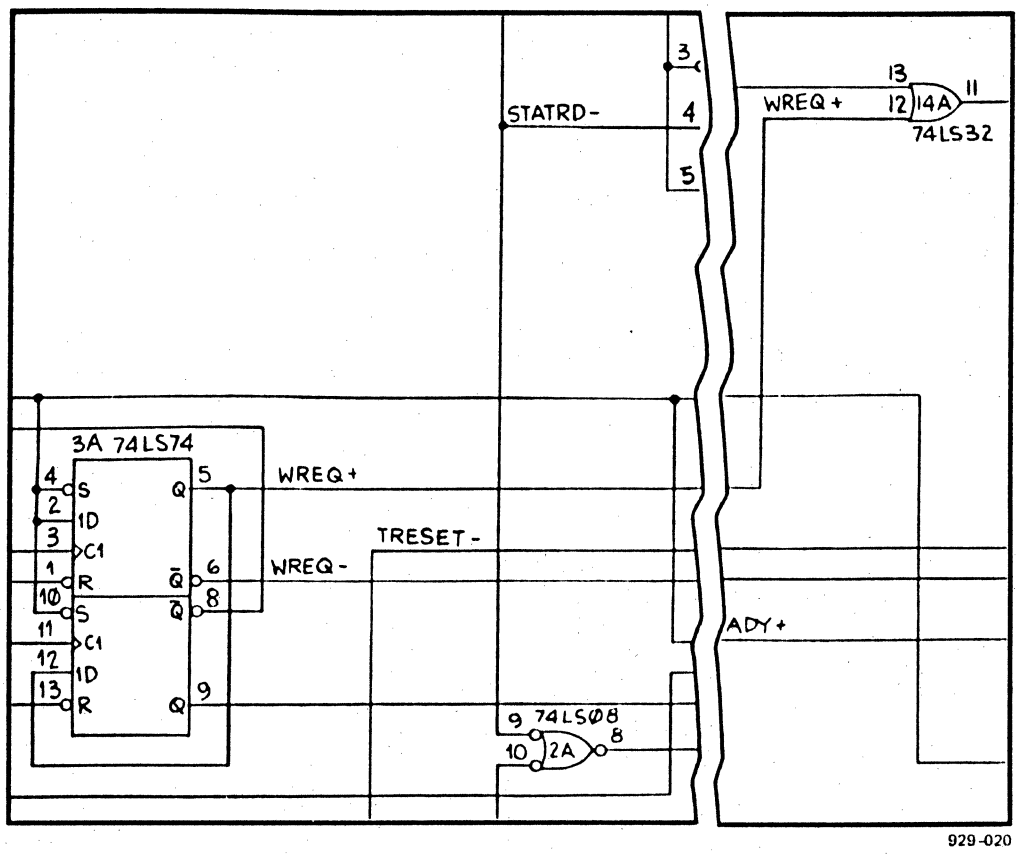


(From Figure B-1, Page 6, Coordinate 8D.)

TAPE DRIVE OPERATION

READ STATUS COMMAND

The CPU issues a read status command (ØCØh to port XX8Øh). At the trailing edge of the command byte write, pin 5 of flip-flop 3A is clocked high (since the input of 3A is high). When pin 5 of 3A goes high, WREQ+ (Write Request) at pins 11 and 12 of 14A are also high. A timing diagram for the read status command is shown in Figure 3-1.



(From Figure B-1, Page 6, Coordinate 3C.)

Pin 11 goes to pin 13 of 4E, which is output at pin 7 of 4E as REQUEST-. Some time after REQUEST- is set, the tape drive will set READY-. READY- (coming in from J1-9 at pin 6 of buffer 3E) is output at pin 14 as TREADY-.

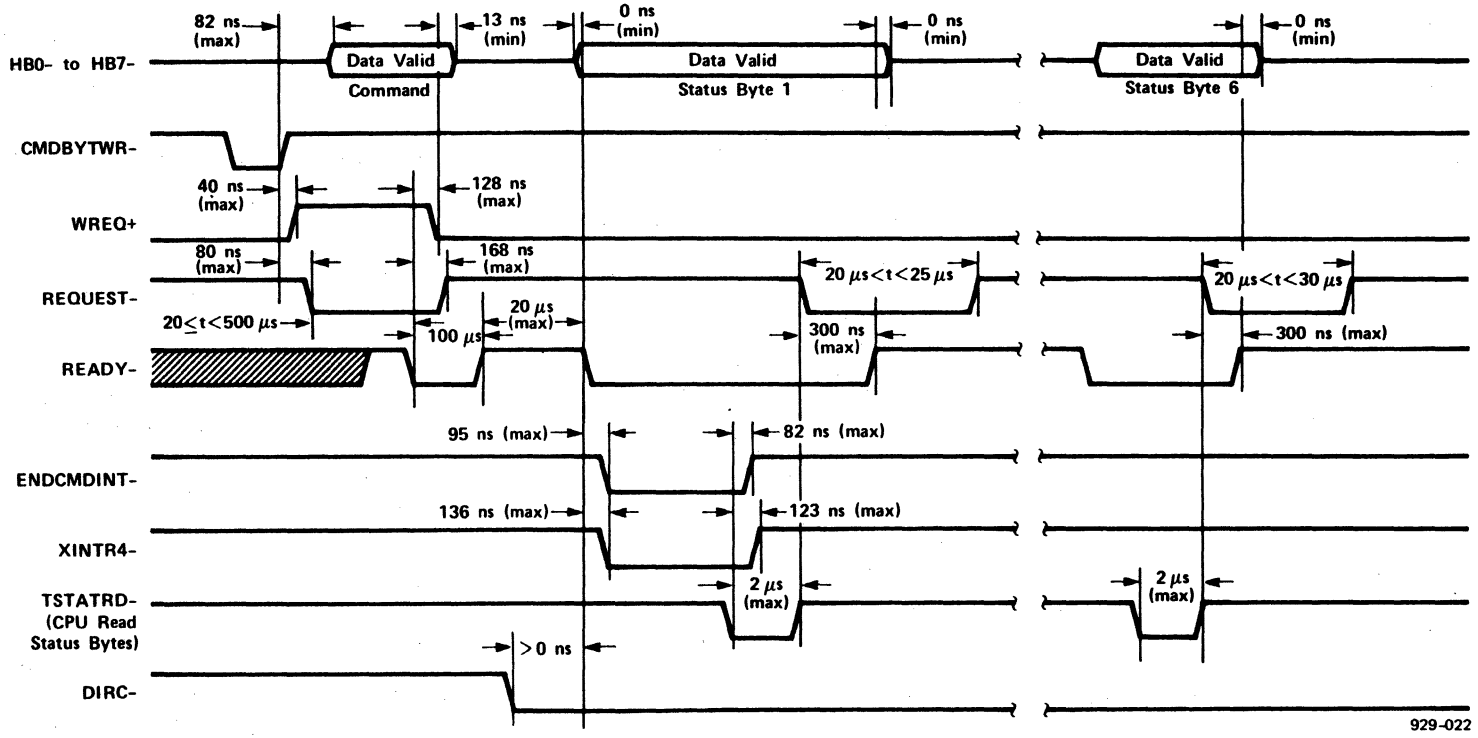
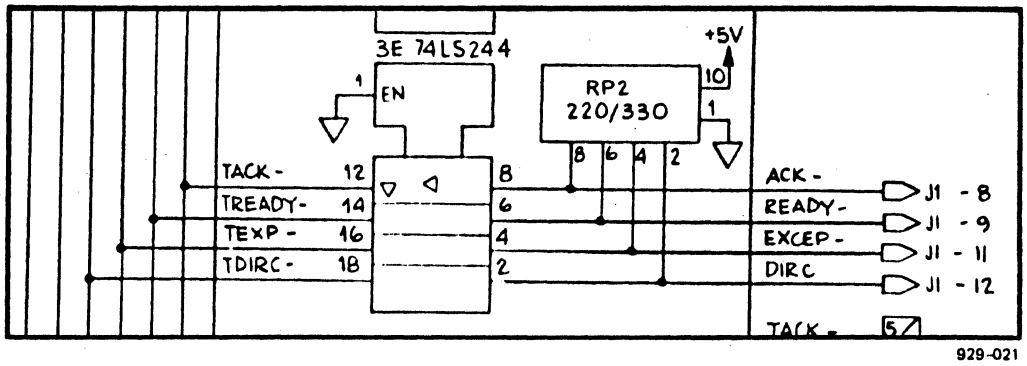
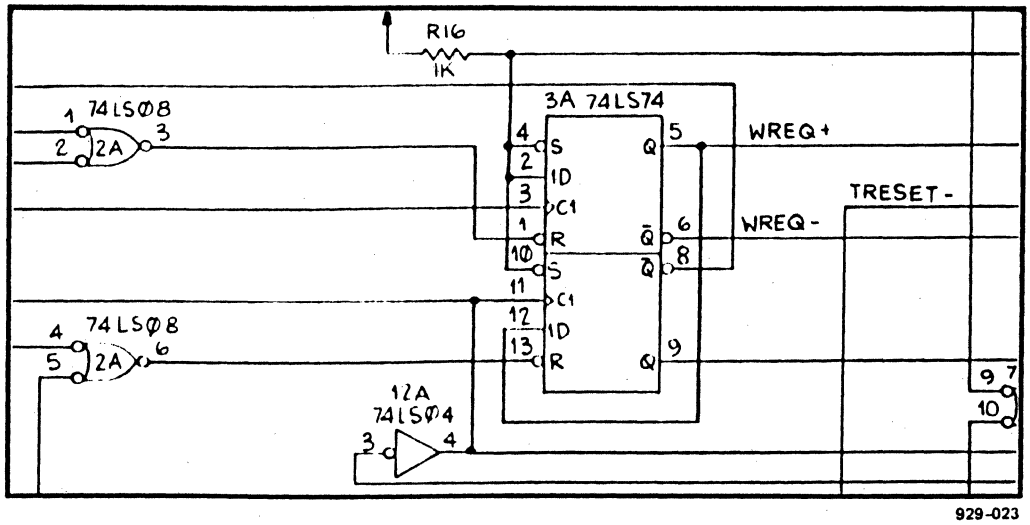


Figure 3-1. Read Status Command Timing Diagram



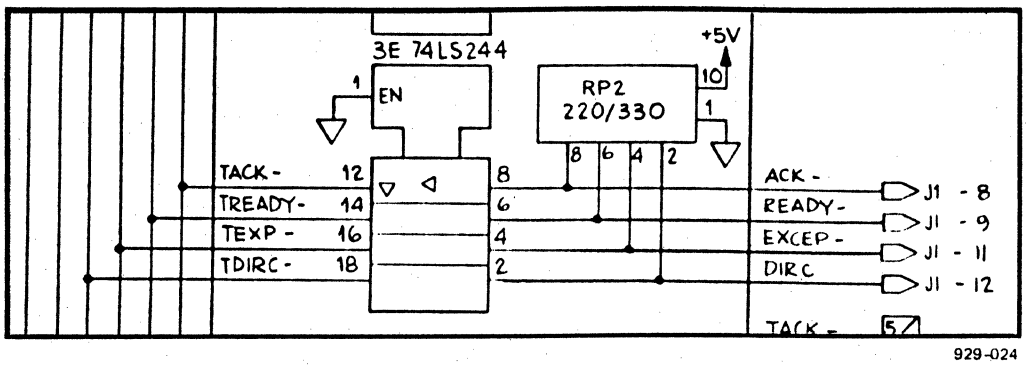
(From Figure B-1, Page 6, Coordinate 3B.)

When TREADY- is low, it goes to 12A, pin 3. Pin 4 of 12A is high and latches the data into pin 11 of flip-flop 3A. Pin 8 of 3A goes low, thus the output of AND gate 2A (pin 3) goes low, clearing 3A (pin 5) and removing the WREQ+.



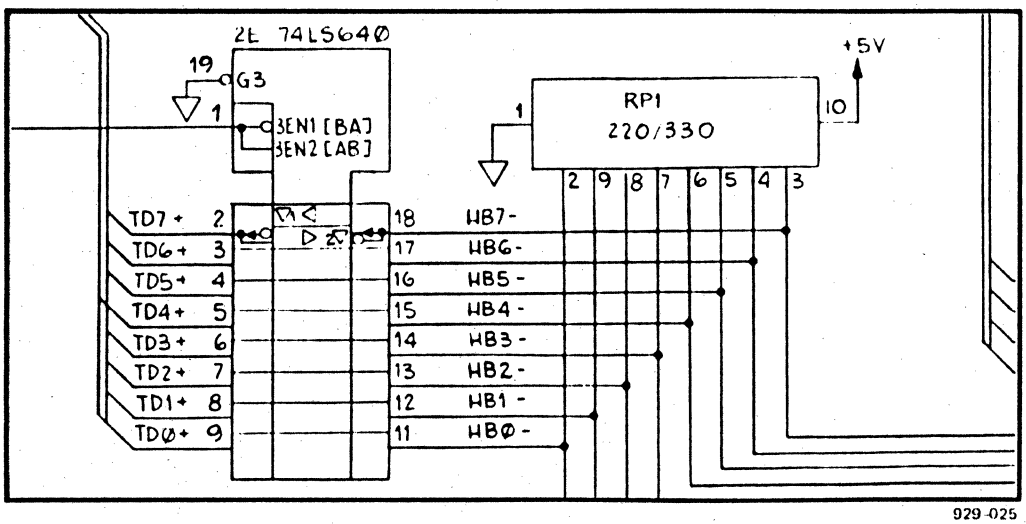
(From Figure B-1, Page 6, Coordinate 7B.)

The tape drive deasserts READY- some time after REQUEST- goes false. The tape drive asserts READY- again when the status byte is available to be read, and asserts DIRC- in preparation for sending the first status byte. DIRC-, coming from J1, pin 12, goes to pin 2 of 3E.



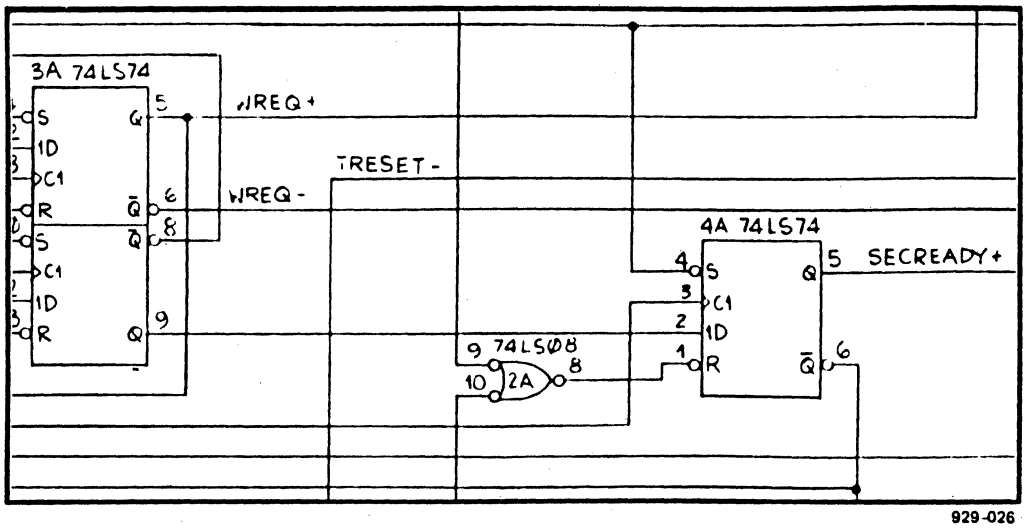
(From Figure B-1, Page 6, Coordinate 3B.)

The buffered output at pin 18 (TDIRC-) goes to pin 1 of 2E. When pin 1 is asserted, the transceiver data path direction is from the HBØ- through HB7- bus, to the TDØ+ through TD7+ bus.



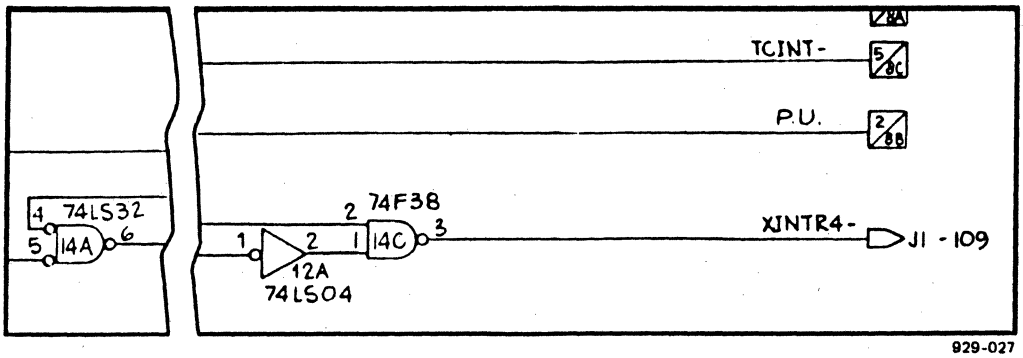
(From Figure B-1, Page 4, Coordinate 8B.)

Since pin 9 of 3A is high, the assertion of READY- forces pin 5 of 4A, SECREADY+ (Second Ready), high.



(From Figure B-1, Page 6, Coordinate 6B.)

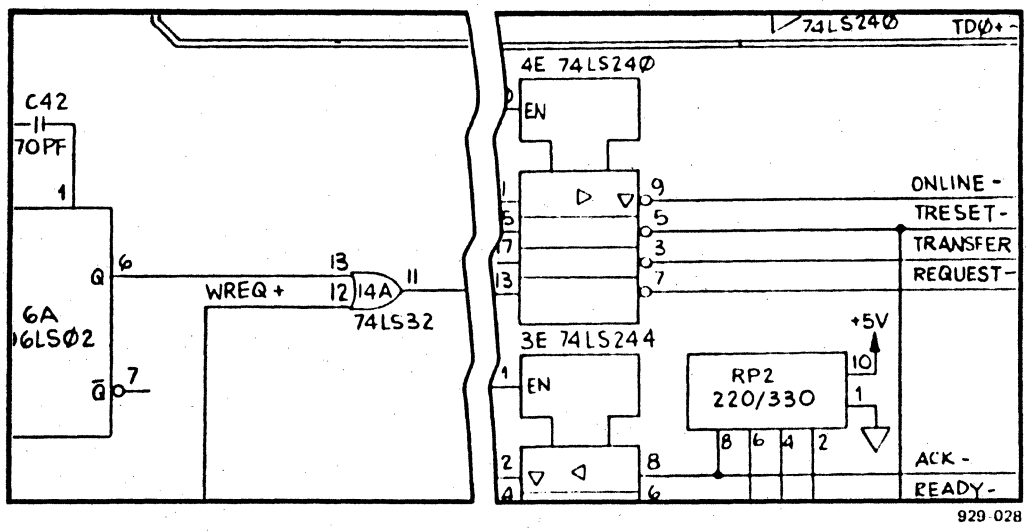
Because pin 4 of 14A is performing a read status only, it is low. So pin 6 of 14A is also low, and pin 2 of 12A is high. When the drive is selected at pin 2 of 14C, an interrupt is generated at J1-109 to inform the CPU that the status byte is available.



(From Figure B-1, Page 6, Coordinate 4A.)

After receiving the interrupt, the Processor Module reads port XX84h (LINSTRD-) to verify that ENDCMDINT+ is set. The Processor Module then performs six reads on port XX80h (STATRD-) to fetch the six status bytes.

When the tape does a read from port XX80h (STATRD-), the output of 2A goes low to clear SECREADY+. When SECREADY+ is clear, pin 6 of 4A goes high, which removes the interrupt. Every time the CPU reads the status, it triggers one-shot flip-flop 6A, and 6A goes high for 20 microseconds. Pin 6 of 6A and pins 13 and 11 of 14A go high. Thereafter, REQUEST-, coming from pin 7 of 4E, remains low for 20 microseconds.



(From Figure B-1, Page 6, Coordinate 5C.)

READ TAPE DATA COMMAND

As shown in the following two windows, the CPU sets the DMA word address by writing the 23-bit address to address registers 8D, 9D, 4C, 5C, 6C, and 7C. A timing diagram of the Read Tape Data command is shown in Figure 3-2.

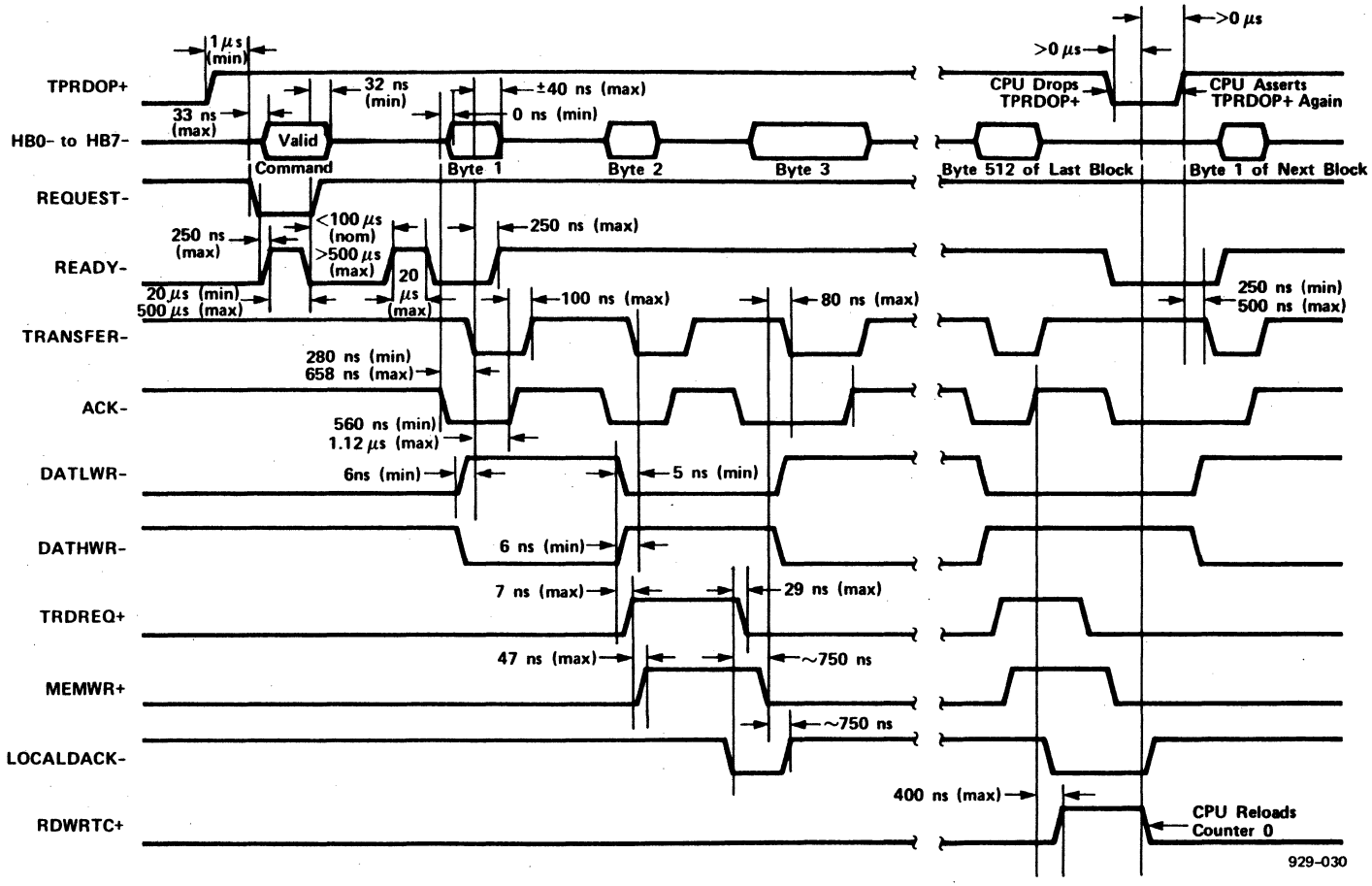
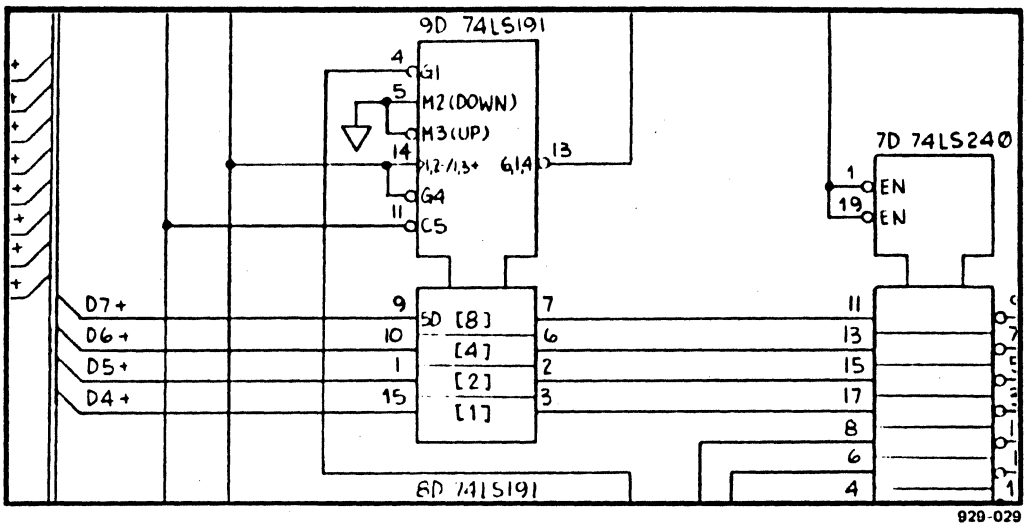
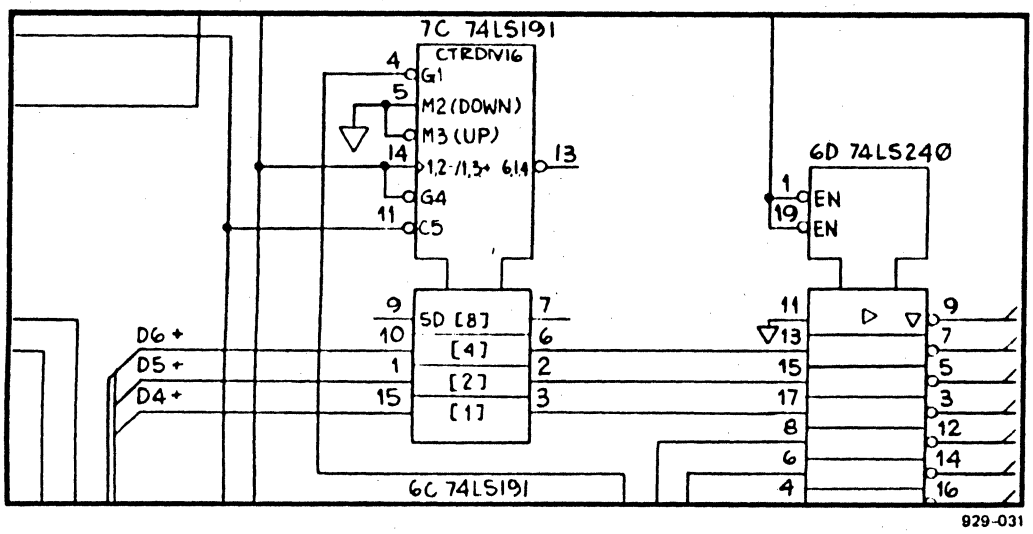


Figure 3-2. Read Tape Data Command Timing Diagram



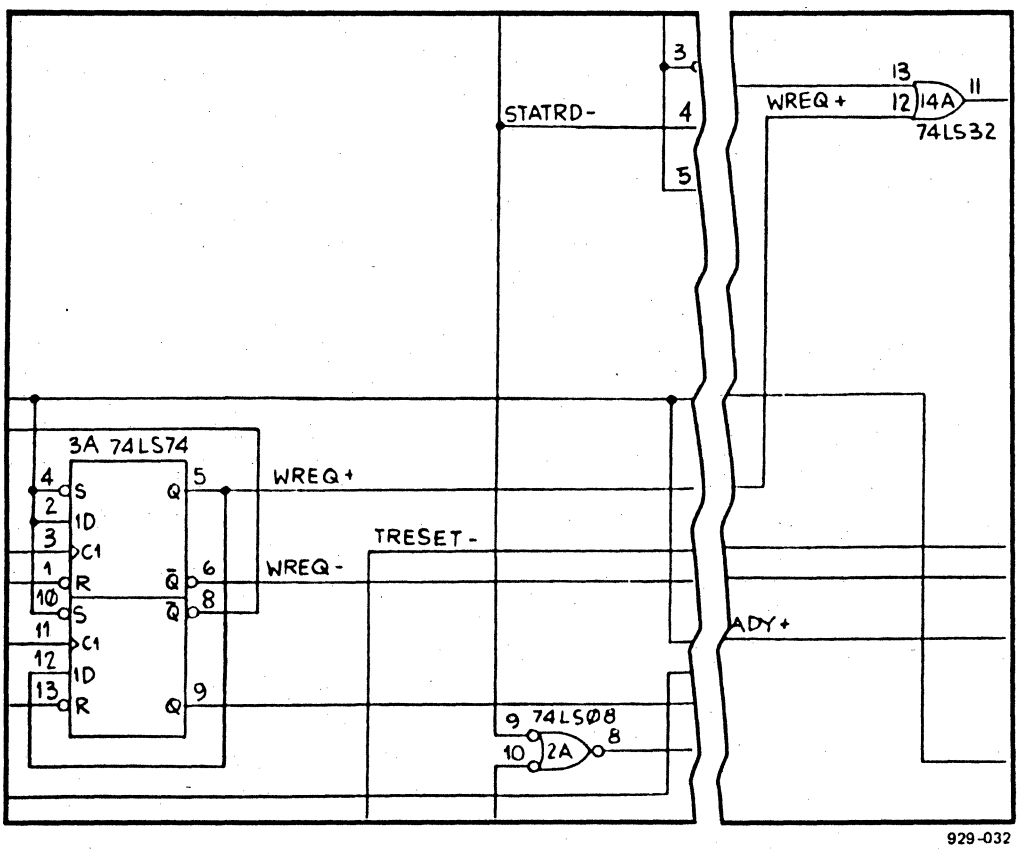
(From Figure B-1, Page 4, Coordinate 4C.)



(From Figure B-1, Page 5, Coordinate 4C.)

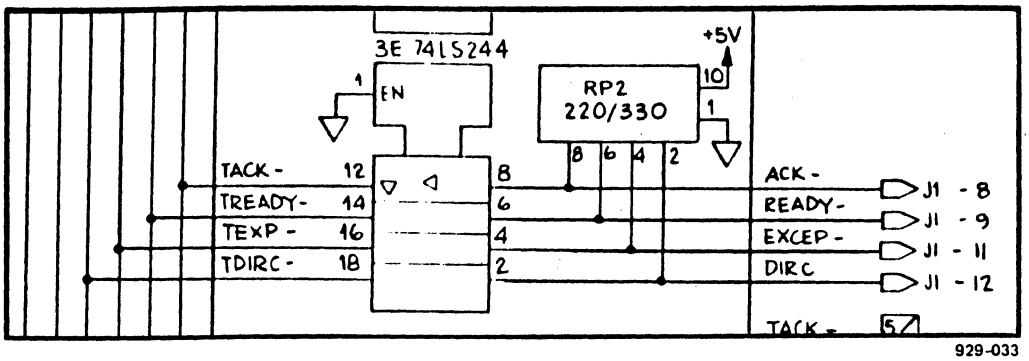
The CPU is reading data from the tape and writing to the memory, so it needs to know the address of the memory to be written. The 23-bit word address (A1+ through A17+), is loaded into the address counter by writing to ports XX8Ah, XX8Ch, and XX8Eh. Each write loads 8 bits of address into the counter. Address Ø is asserted automatically during DMA.

The CPU also sets up the 8253 programmable interval timer, telling it how many bytes need to be transferred from the tape. The CPU then issues the command byte 40h to the CMDBTWR- (Command Byte Write) port. At the trailing edge of CMDBTWR-, flip-flop 3A is clocked at pin 3, then at pin 5, which goes high. The output of pin 5, WREQ+ (Write Request), goes through 14A (pin 12), indicating to the drive that there is a write request.



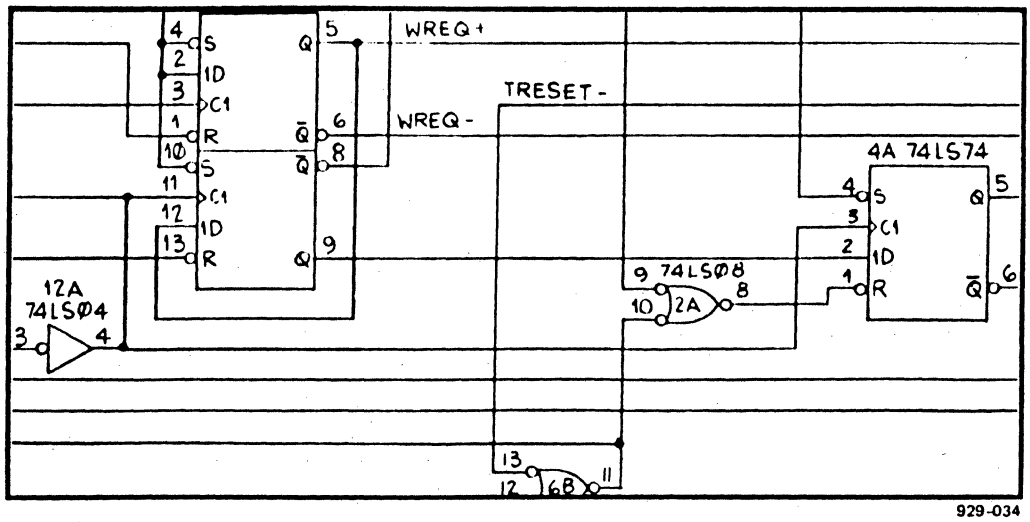
(From Figure B-1, Page 6, Coordinate 3C.)

The tape drive asserts a ready through J1, pin 9, which is then buffered through pin 6 of 3E as TREADY- (Tape Ready).



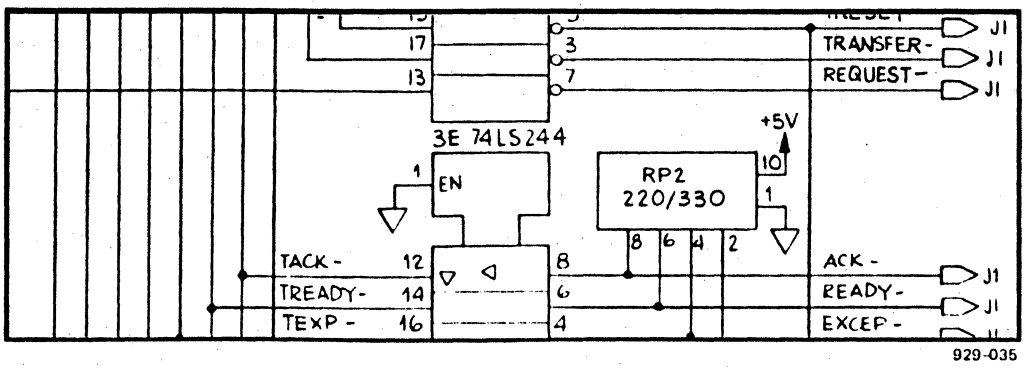
(From Figure B-1, Page 6, Coordinate 3B.)

TREADY- is inverted at pin 3 of 12A and clocks pin 11 of 3A. Since pin 5 of 3A is set to 1, pin 9 goes high, and pin 8 goes low, clearing the request. The tape drive deasserts and asserts READY- again. The second time that READY- is asserted, SECREADY+ (Second Ready) at pin 5 of 4A is asserted, indicating that the data is ready to be read.



(From Figure B-1, Page 6, Coordinate 7B.)

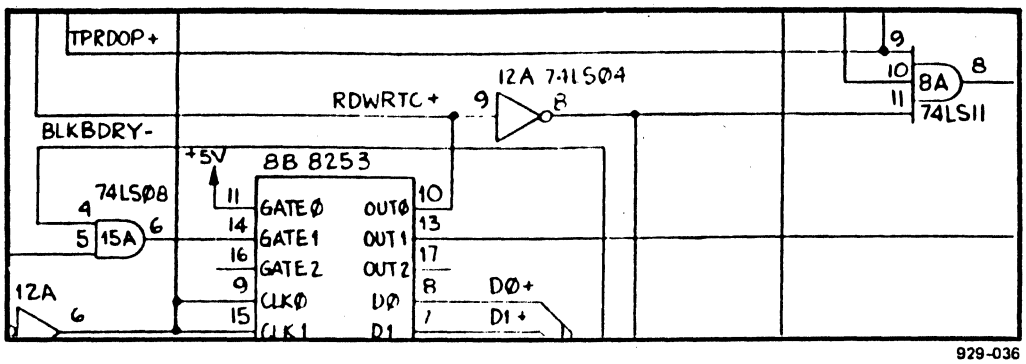
The handshake between the Tape Drive Control board and the QIC-Ø2 interface is through ACK- (Acknowledge) and TRANSFER- (Transfer), via J1, pins 8 and 7, respectively.



(From Figure B-1, Page 6, Coordinate 3B.)

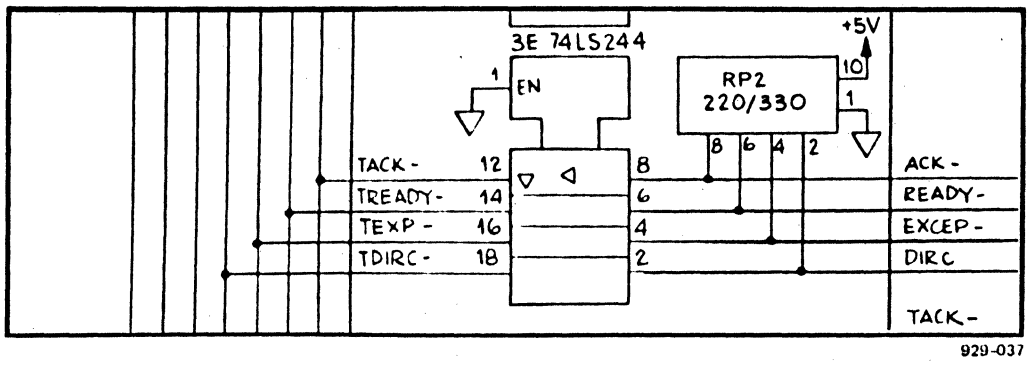
During a read operation, the tape asserts ACK-. When the tape control circuitry on the Tape Drive Control board receives the data, it asserts TRANSFER-, notifying the tape drive that the data has been received. The tape drive monitors the transfer. When the transfer has been asserted, the tape drive drops the acknowledge and asserts an acknowledge for the second byte.

Since counter Ø of the 8253 programmable interval timer (8B) is set in the interrupt on terminal count mode, pin 1Ø is low, and pin 8 of 12A and pin 11 of 8A are high, set in the initial condition.



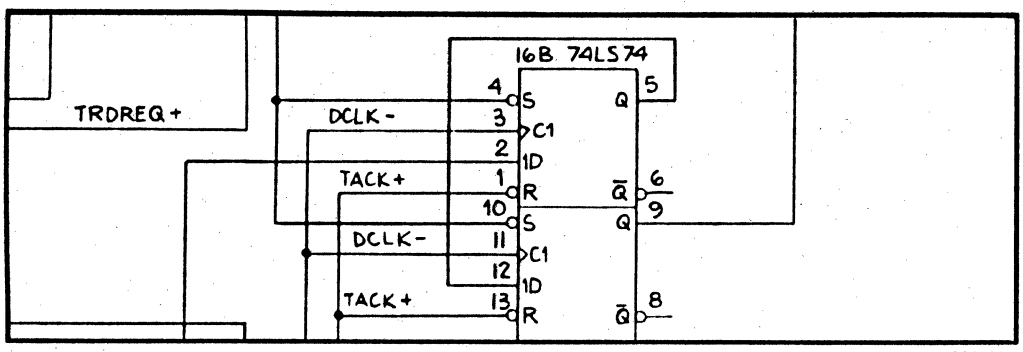
(From Figure B-1, Page 5, Coordinate 7B.)

Pin 9 of 8A is tied to TPRDOP+ (Tape Read Operation), and is high because it is reading. Pin 10 of 8A is tied to TACK+ (Tape Acknowledge), originating from pin 6 of 12A through pin 12 of buffer 3E.



(From Figure B-1, Page 6, Coordinate 3B.)

When the tape drive has data available, TACK- is low, and pin 6 of 12A is high. Pin 10 of 8A goes high, indicating that a byte is available. Pin 3 of 16B is tied to DCLK- (Data Clock), which is running at 250 nanoseconds. When a byte is available, pin 2 of 16B is high.

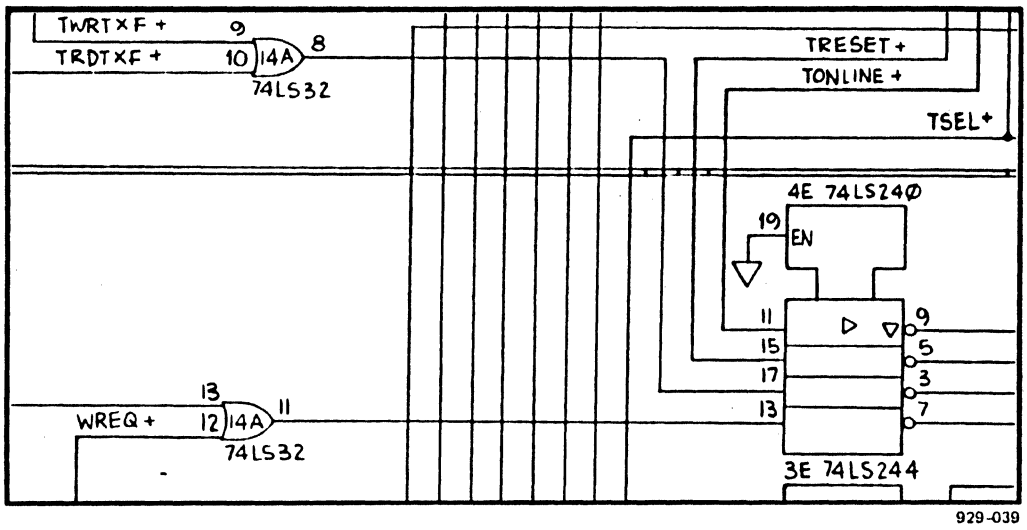


(From Figure B-1, Page 5, Coordinate 4C.)

At the next clock (250 nanoseconds later), DCLK- is asserted again, and pin 9 of 16B goes high. Because this clock is asynchronous, 16B prevents metastable conditions. Data from the tape drive may be valid as late as 40 nanoseconds after ACK- is asserted.

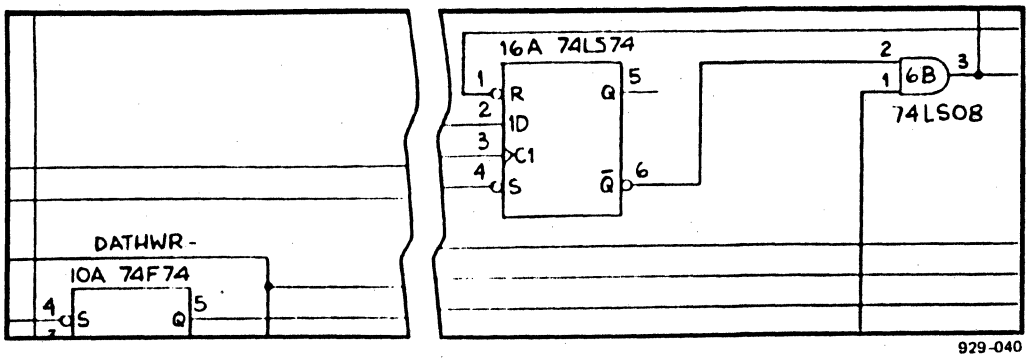
Pin 9 of 16B goes to pin 1 of 6B. There is as yet no write to CPU memory, and no DMA operation occurring at this time. (At this point, pin 2 of 6B is high, because MEMWR+ (Memory Write) is low.) TRDTXF+ (Tape Read Transfer) comes from pin 3 of 6B, indicating that the tape is available.

TRDTXF+ now goes to pin 10 of 14A, while pin 8 of 14A goes into pin 17 of 4E, indicating that the data has been received.



(From Figure B-1, Page 6, Coordinate 4C.)

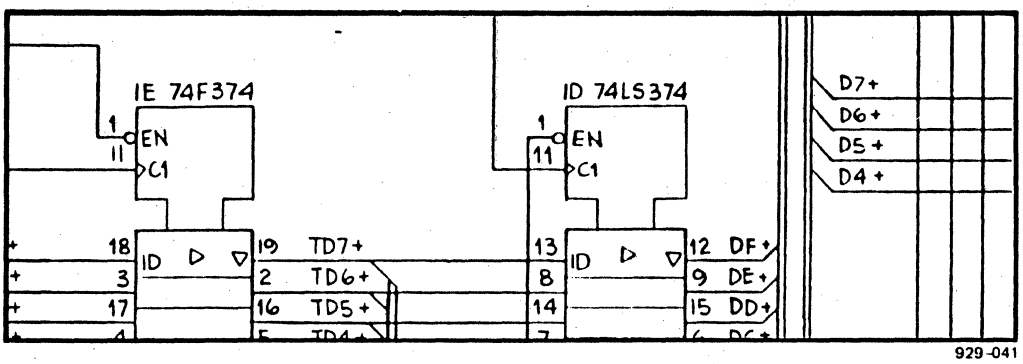
Pin 3 of 6B clocks pin 3 of 10A. This causes pin 5 of 10A to go high, deasserting DATLWR- (Data Low Write).



(From Figure B-1, Page 5, Coordinate 4D.)

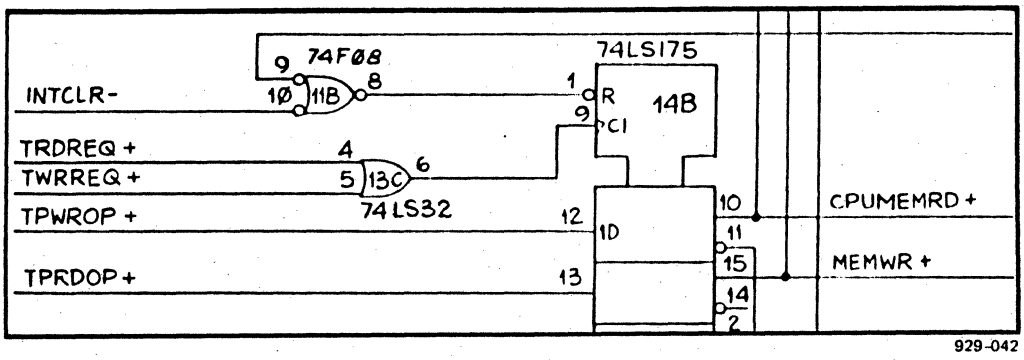
DATLWR- clocks into pin 11 of 2D, and the tape data lines (HB0- through HB7-), coming through 2E, are latched into 2D. When the second byte is available, the tape drive asserts TACK- once again.

Pin 3 of 6B goes high, notifying the tape drive that it has received the data. 1ØA now clocks the flip-flop (pin 6 of 1ØA goes high and clocks pin 11). DATHWR- at pin 6 of 1ØA goes high and latches the data into register 1D.



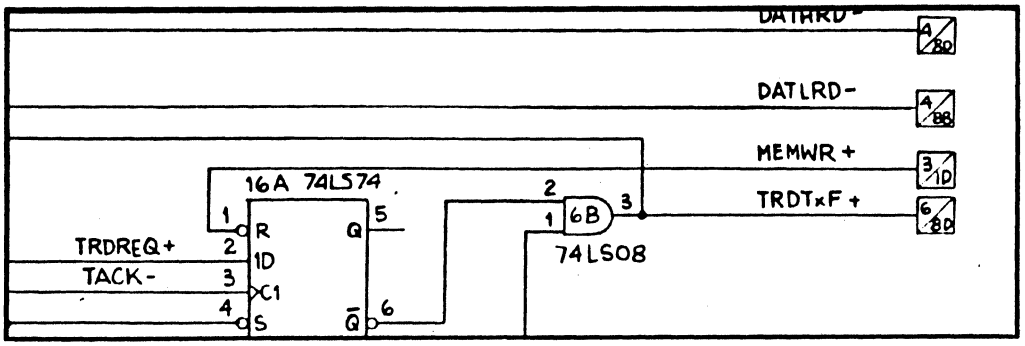
(From Figure B-1, Page 4, Coordinate 6D.)

Pin 9 of 1ØA also goes high, issuing TRDREQ+. Two bytes have already been received at this point, and are ready to do a DMA transfer to the CPU memory. TRDREQ+ goes to pin 4 of 13C and clocks pin 9 of 14B, generating a DMA request.



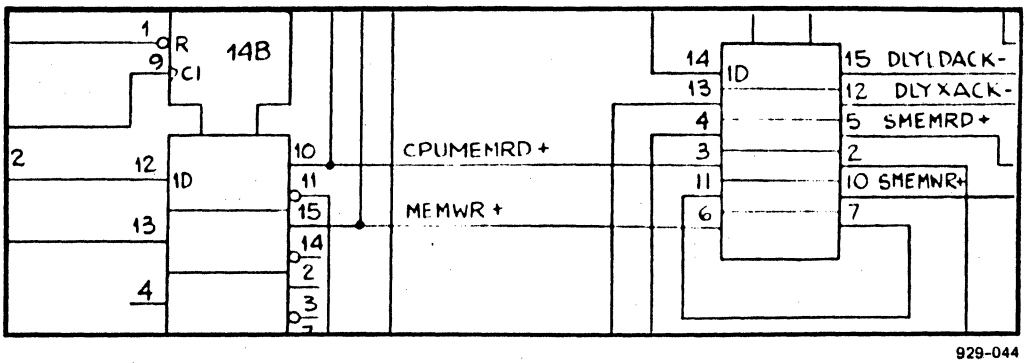
(From Figure B-1, Page 3, Coordinate 8D.)

At the same time, TRDREQ+ also goes to pin 2 of 16A to inhibit further returning of a TRANSFER- signal to the tape drive until DMA is complete.



(From Figure B-1, Page 5, Coordinate 3D.)

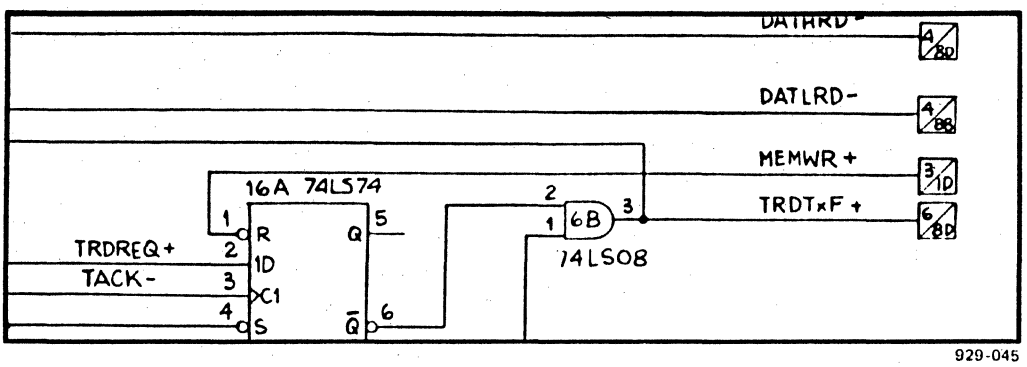
MEMWR+ (pin 15 of 14B) is asserted, and one clock later, SMEMWR+ (Synchronous Memory Write) goes high, indicating a local request with LOCAL RQ+.



(From Figure B-1, Page 3, Coordinate 7D.)

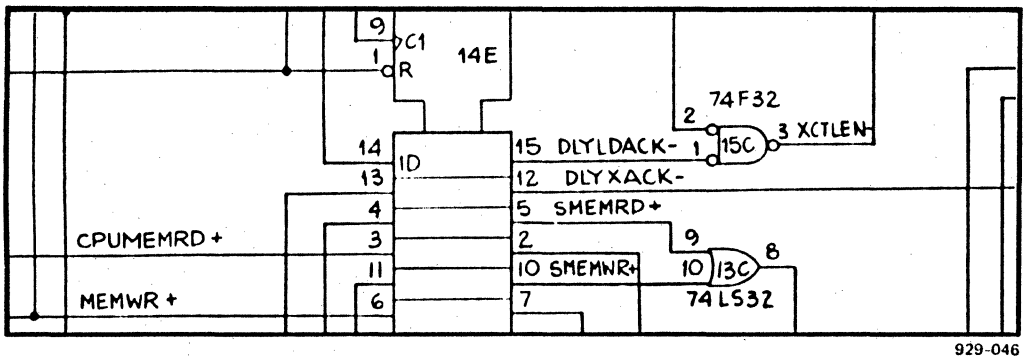
If the third byte is available before the DMA is complete, TACK- clocks pin 3 of 16A, and pin 6 of 16A has a Ø.

When the Processor Module is signaled that the DMA is finished, it clears 11B and 14B, thus clearing MEMWR+ at pin 15. MEMWR+ then goes low, forcing pin 1 of 16A low, and forcing pin 6 of 16A high. At this point, pin 3 of 16A gives a transfer acknowledge back to the tape drive.



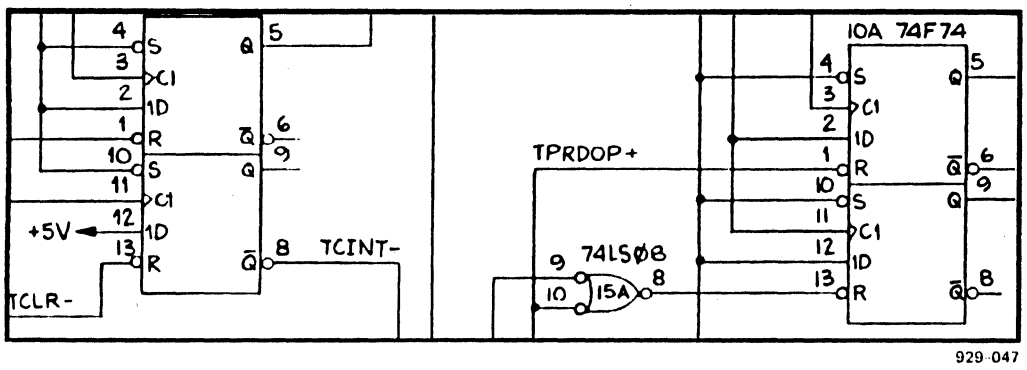
From Figure B-1, Page 5, Coordinate 3D.)

If the DMA is completed before the third byte count, the MEMWR+ still clears pin 6 of flip-flop 14E, which goes high and is enabled.



(From Figure B-1, Page 3, Coordinate 6D.)

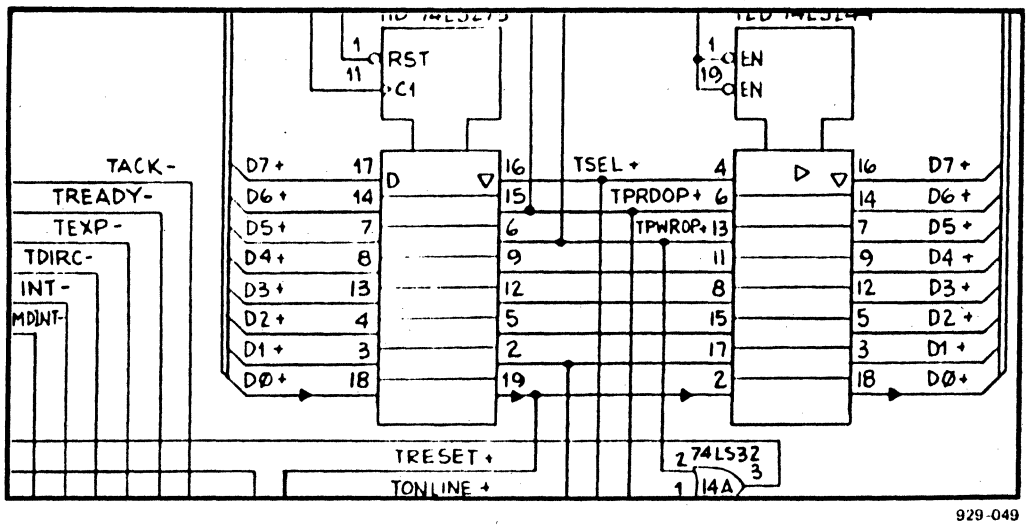
The flip-flop is cleared when LOCAL DACK- is low and goes through 15A (pin 9), indicating that the request is not finished.



(From Figure B-1, Page 5, Coordinate 6C.)

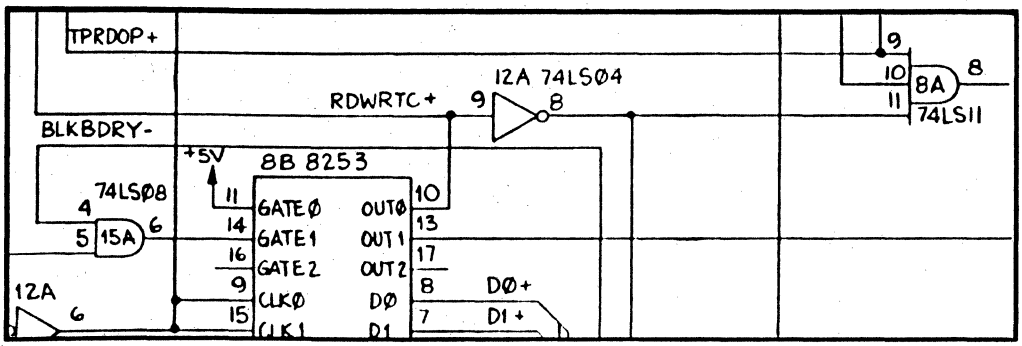
WRITE TAPE DATA COMMAND

When writing data to the tape, the CPU enables TSEL+ (T-Select) and TONLINE+ (T-On Line) at 11D, and enables the bit write operation. A timing diagram of the write tape data command is shown in Figure 3-3.



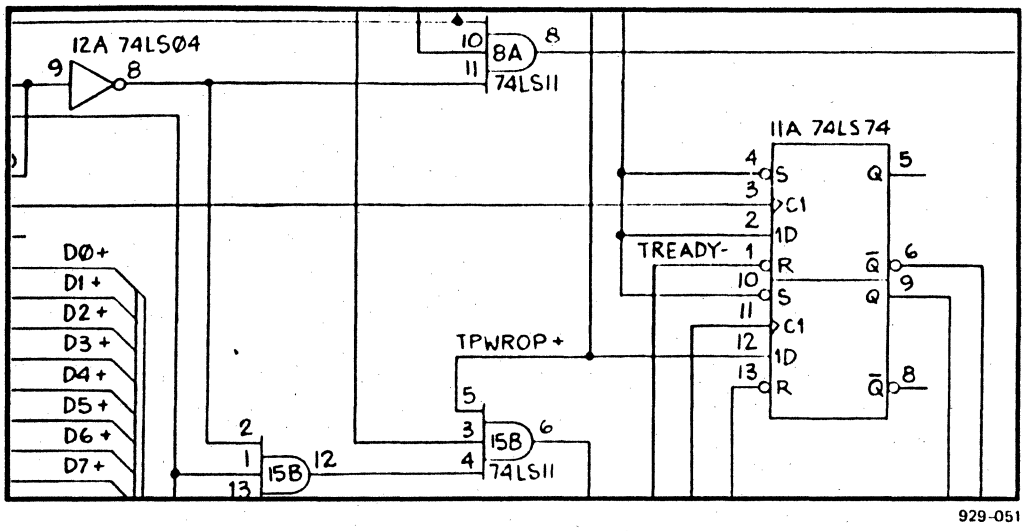
(From Figure B-1, Page 6, Coordinate 3D.)

7A writes to the tape. The 8253 programmable interval timer at 8B enables OUTØ (the internal counter) at pin 1Ø, generating RDWRTC+ (Read Write Terminal Count).



(From Figure B-1, Page 5, Coordinate 7B.)

When SECREADY+ goes high, TREADY- clears flip-flop 11A. At this time, pin 6 of 11A and pin 1 of 15B are high, and pin 2 of 15B is high.



(From Figure B-1, Page 5, Coordinate 6B.)

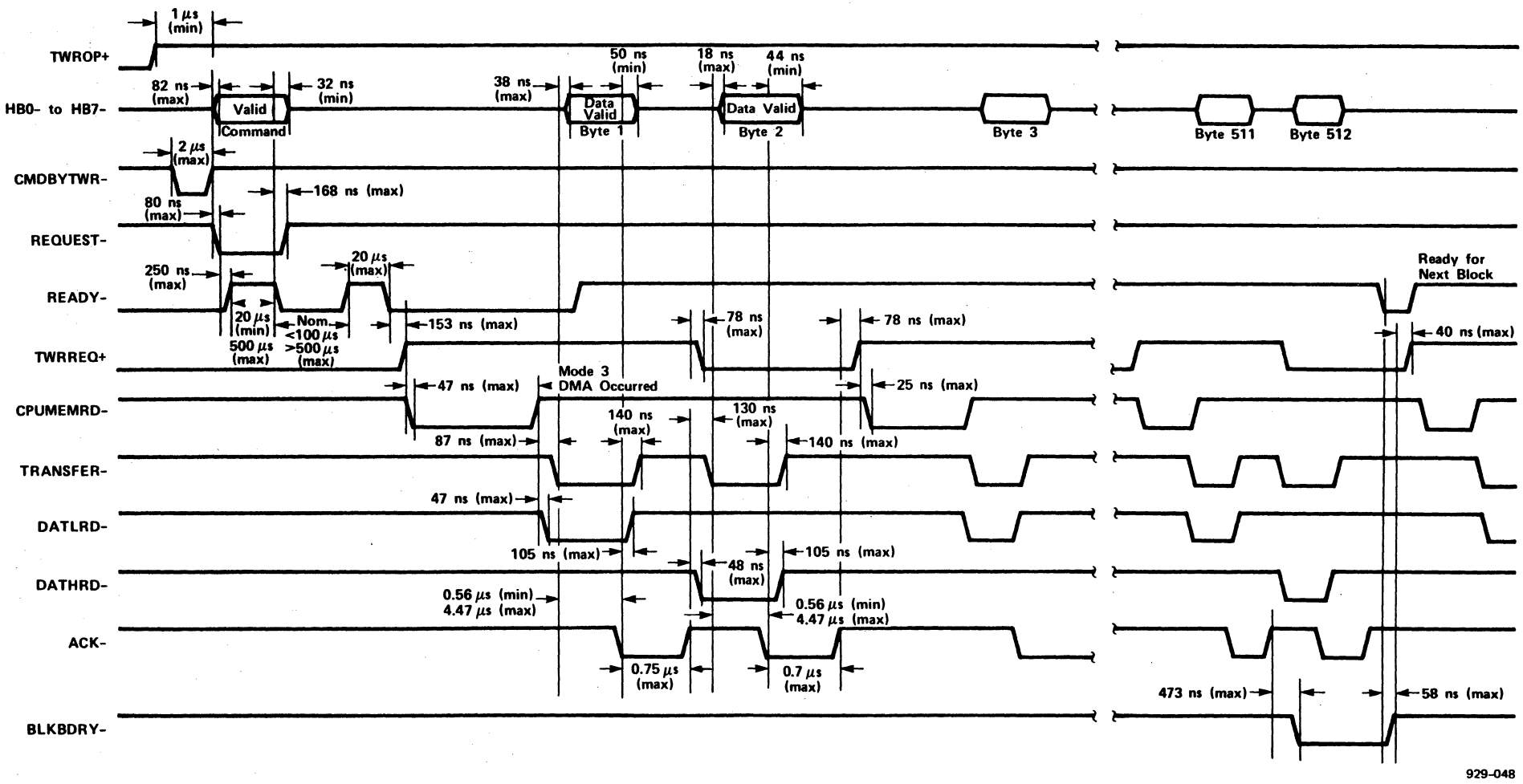
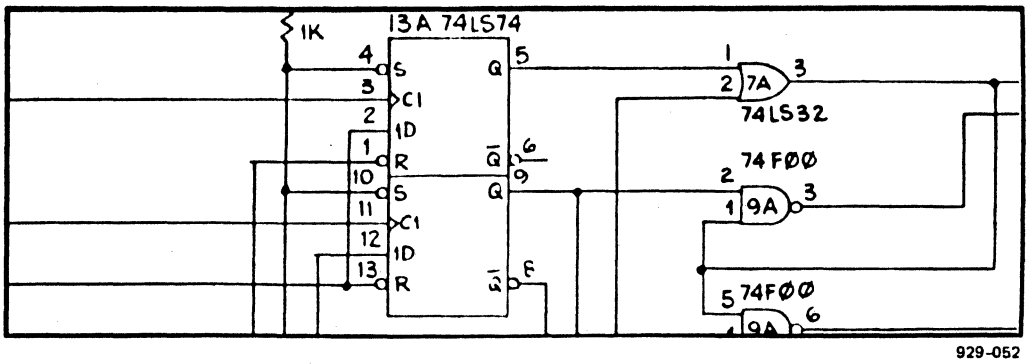


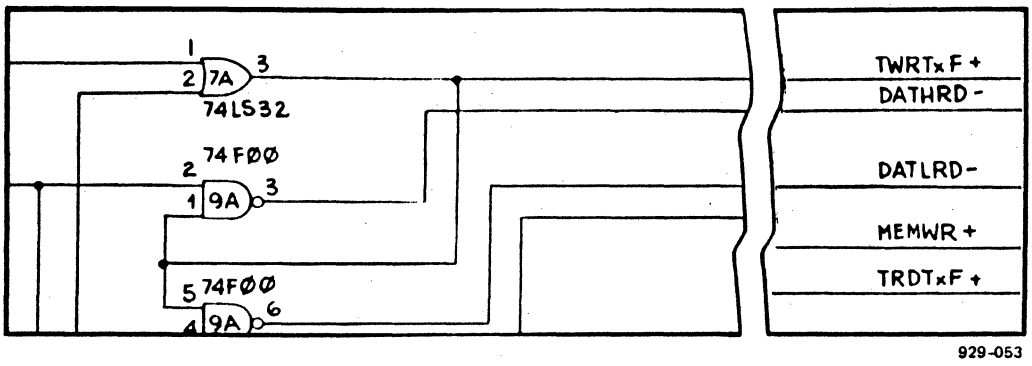
Figure 3-3. Write Tape Data Command Timing Diagram

Pin 6 of 11B causes pin 1 of 15B to go high. Pin 1Ø of 8B goes low, then gets inverted to high at 12A, generating a SECREADY+. At this time, the outputs of pin 12 (11A and 15B) are high. When pins 3, 4, and 5 of 15B go high, their outputs go to pin 8 of 13A, which is a divide-by-two flip-flop that controls the high-low byte. Then, pins 2 and 13 of 13A issue TPWROP+ (Tape Write Operation), giving a DMA request.



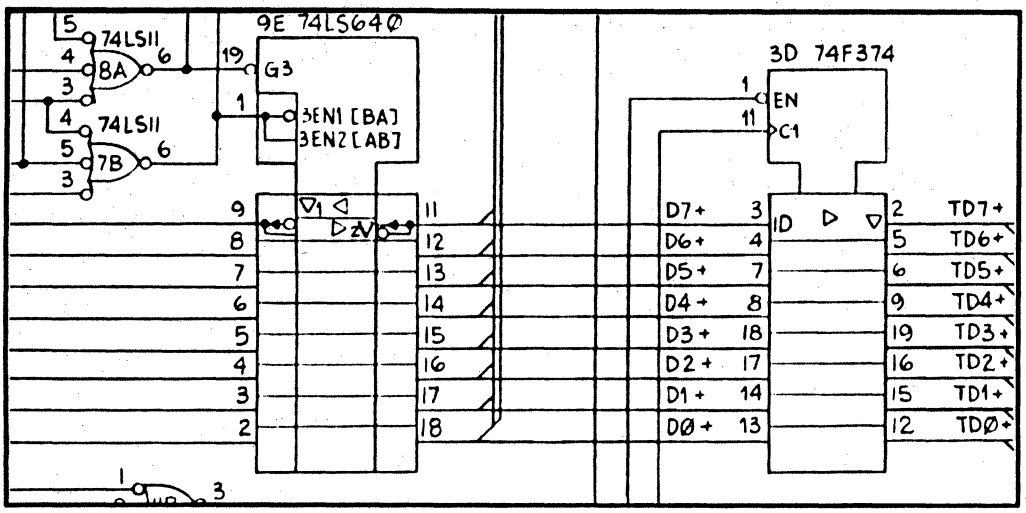
(From Figure B-1, Page 5, Coordinate 7D.)

Pin 6 of gate 9A goes low, issuing a DATLRD- (Data Low Read). DATLRD- is driven through gate 11B



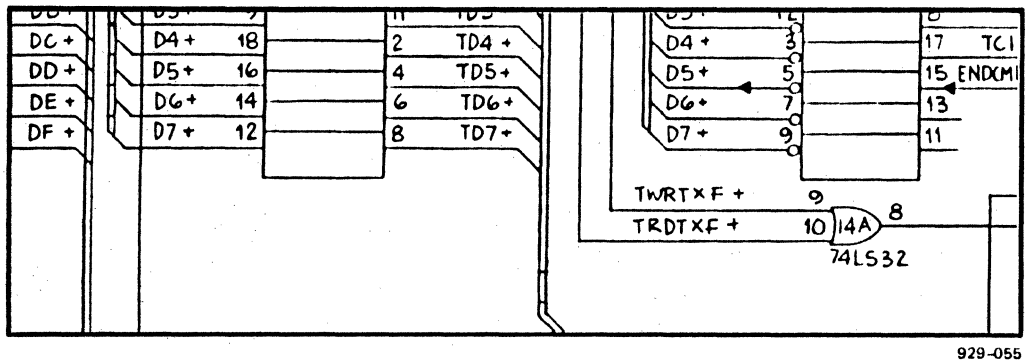
(From Figure B-1, Page 5, Coordinate 5D.)

(pin 2), and the output of 11B (pin 3) enables 3D at pin 1.



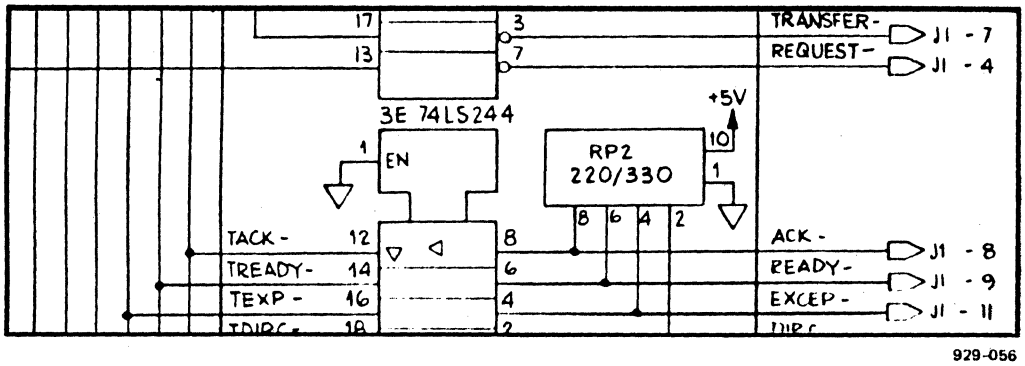
(From Figure B-1, Page 4, Coordinate 7C.)

The control circuitry asserts TRANSFER- to inform the tape drive that data is available. The tape drive receives the data, asserts acknowledge, and the control circuity removes the transfer. This is called a handshake operation. When pin 1 or pin 3 of 7A is high, the tape generates a transfer to pin 9 of 14A.



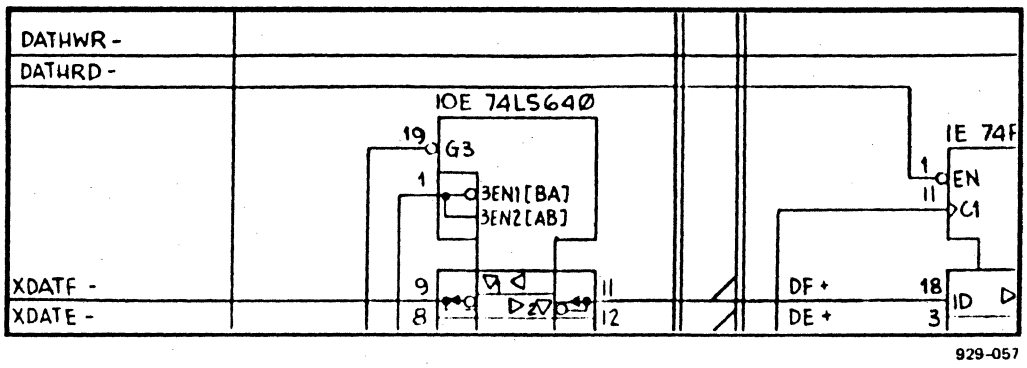
(From Figure B-1, Page 6, Coordinate 5C.)

The high output (pin 8) then goes to pin 17 of 4E, and lowers the transfer, indicating to the tape drive that there is data available. The tape drive then issues an ACK- from connector J1, pin 8, to pin 8 of buffer 3E. ACK- is buffered, bringing pin 12 of 3E low and issuing a TACK- (Tape Acknowledge). When TACK- is low, there is a transfer pending, and the acknowledge is coming back from the tape drive.



(From Figure B-1, Page 6, Coordinate 3B.)

When TACK- is high, it clocks pin 11 of flip-flop 13A. Pin 9 of 13A is then driven high through gate 9A, where the output (pin 3) enables pin 1 of 1E.



(From Figure B-1, Page 4, Coordinate 8D.)

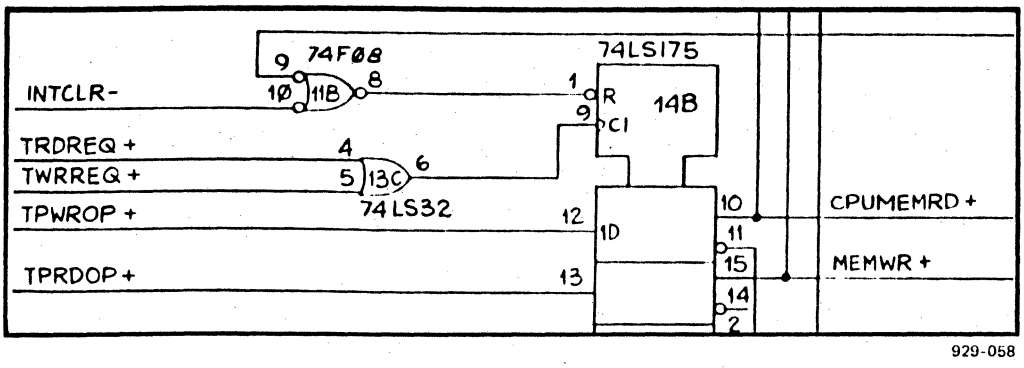
MODE 3 DMA

CONTROL ARBITRATION

The tape control circuitry operates asynchronously to the CPU and performs reads and writes at any time. The CPU responds to the tape control circuitry with an XACK- after each transfer.

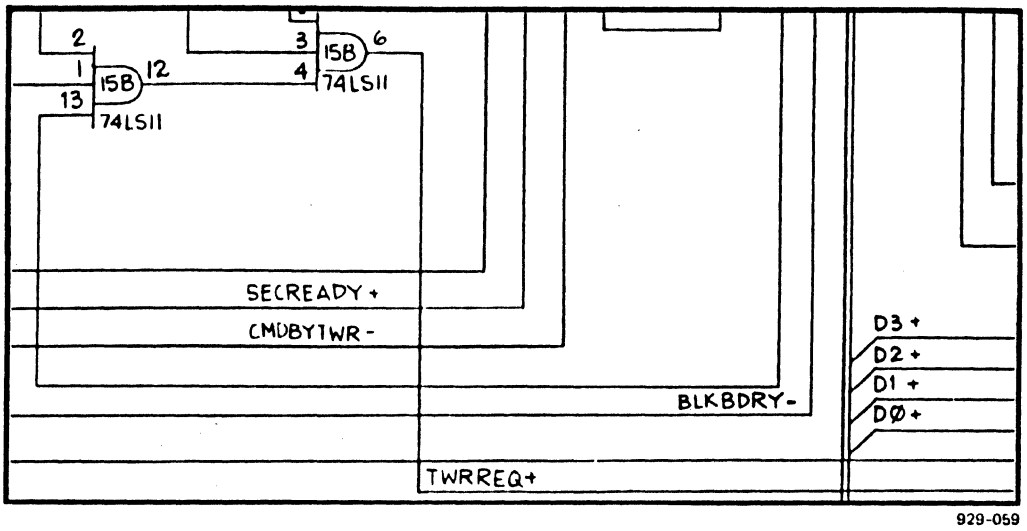
DMA MEMORY READ

When the tape control circuitry performs a tape write operation, TPWROP+ (at pin 12 of control register 14B) is set.



(From Figure B-1, Page 3, Coordinate 8D.)

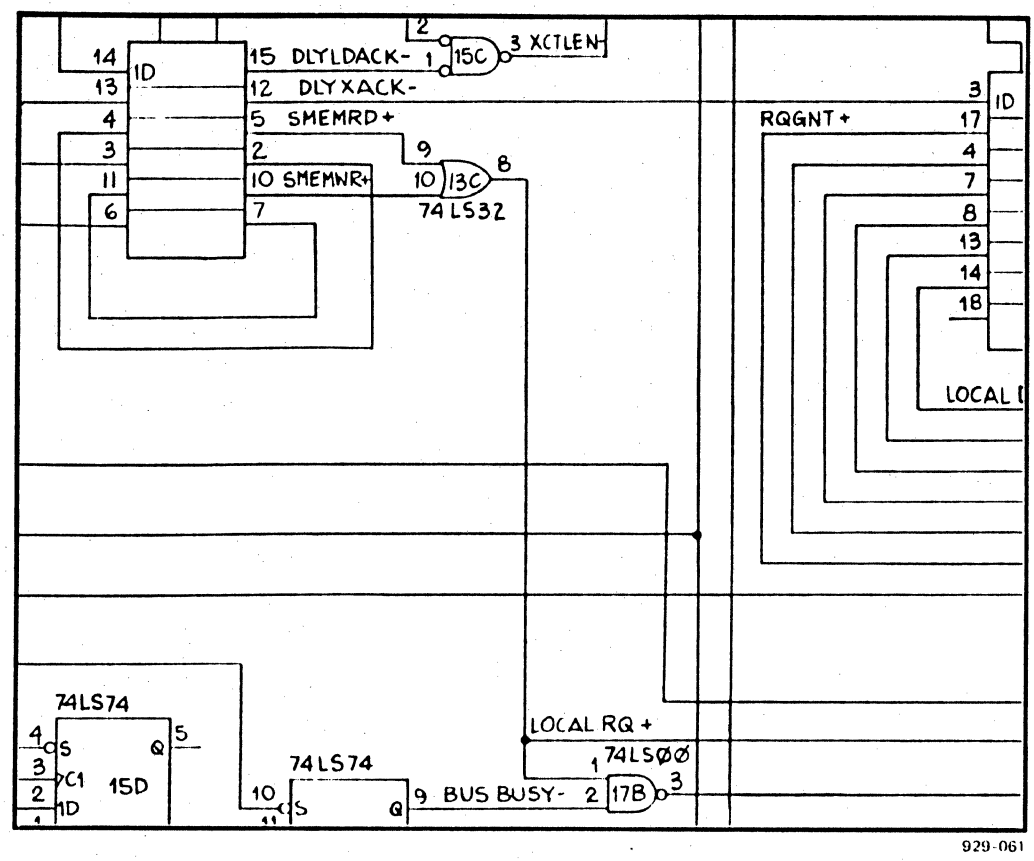
TWRREQ+, from pin 6 of 15B, is asserted to request a word of data to be read from CPU memory, through mode 3 DMA.



(From Figure B-1, Page 5, Coordinate 5B.)

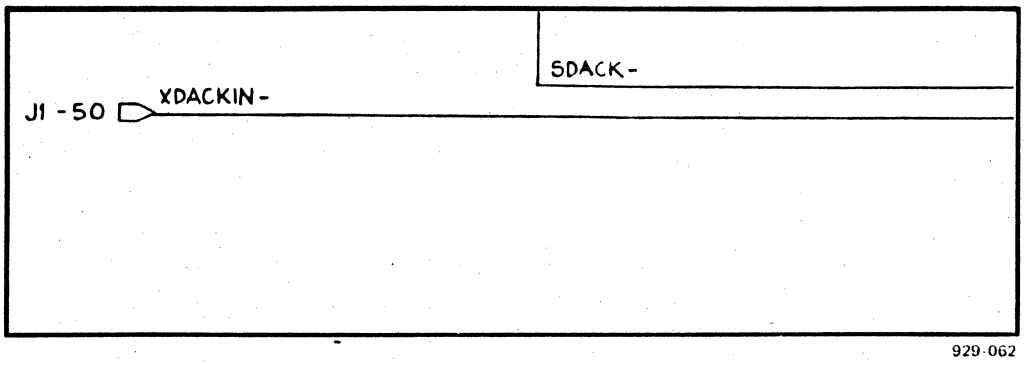
This causes pin 5 of 13C to go high. At the same time, pin 6 of 13C goes high and is driven to the clock of 14B (pin 9). The output of pin 1Ø, CPUMEMRD+ (CPU Memory Read), is high. This means that data is read from the memory, and then written to the tape. CPUMEMRD+ is high, so pin 3 of 14E is also high. (See Figure 3-4.)

One clock later, pin 2 of 14E goes high, and then the output of pin 5 goes high, which is SMEMRD+ (Synchronous Memory Read). Pin 8 of 13C generates LOCAL RQ+ (Local Request), which is high and goes to pin 1 of 17B. Pin 3 of 17B then goes low and drives pin 11 of 15A (XDRQ1OUT-) low, which indicates that there is a DMA request pending.



(From Figure B-1, Page 3, Coordinate 6C.)

The CPU acknowledges the request by lowering XDACKIN- (DMA Acknowledge In) via connector J1, pin 5Ø.



(From Figure B-1, Page 3, Coordinate 8B.)

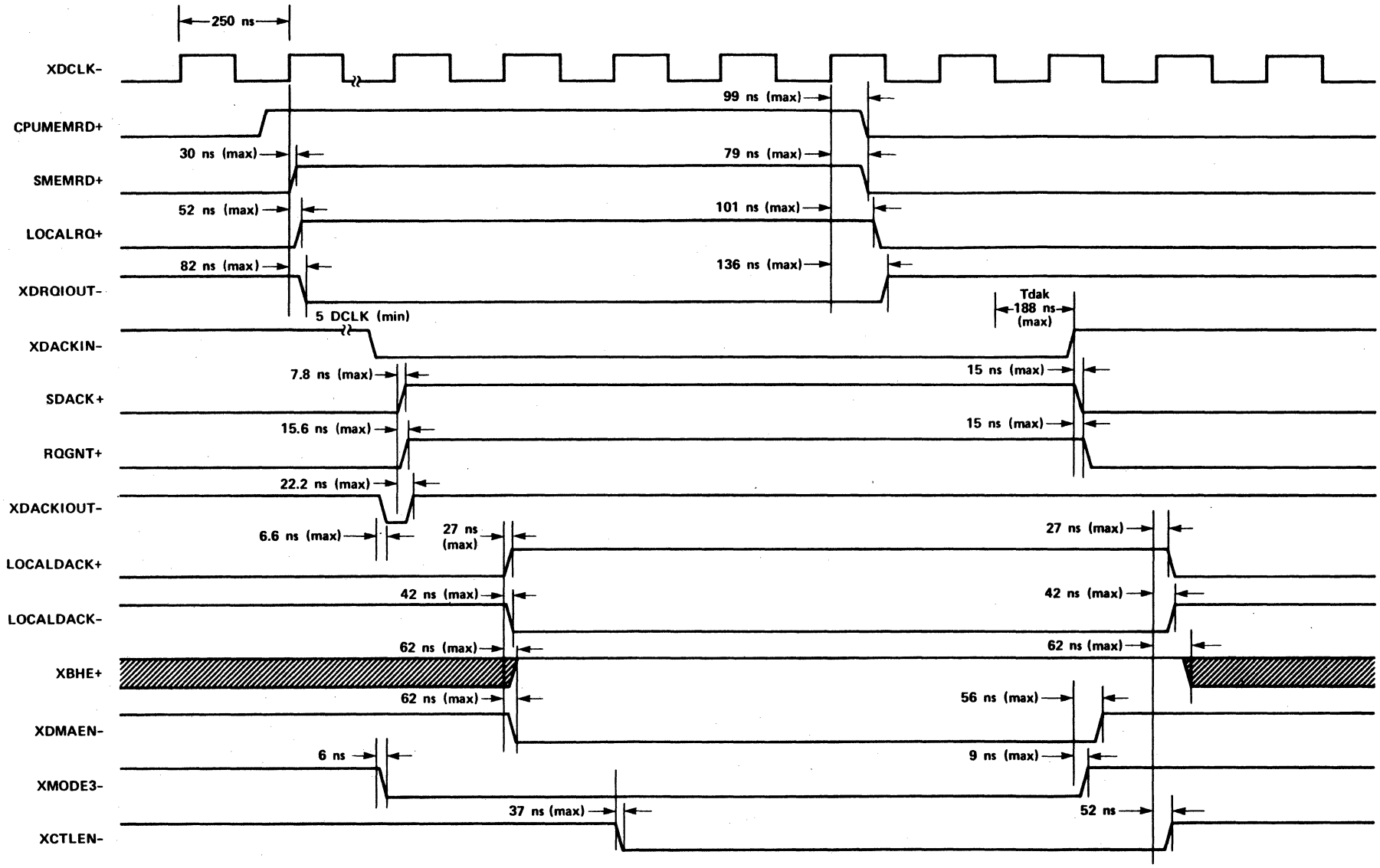


Figure 3-4. Mode 3 DMA Memory Read Timing Diagram (Page 1 of 2)

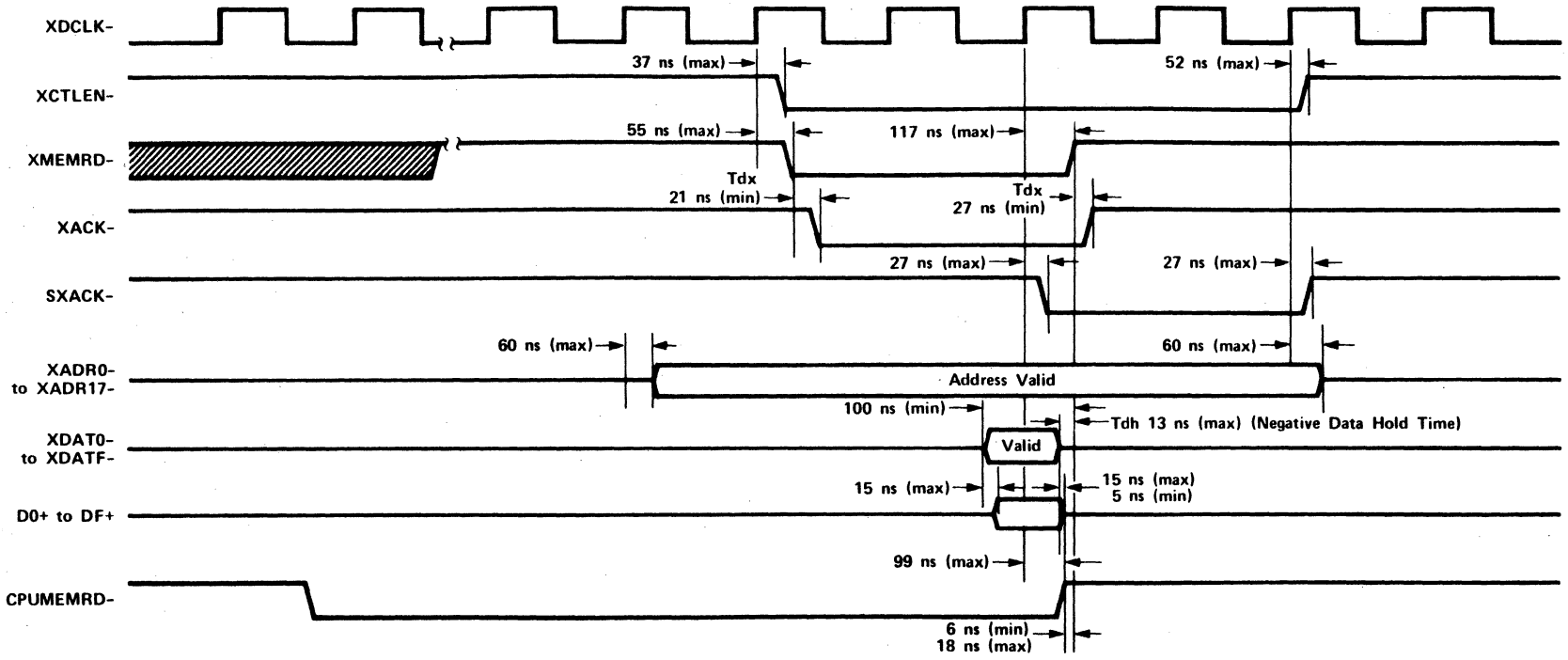
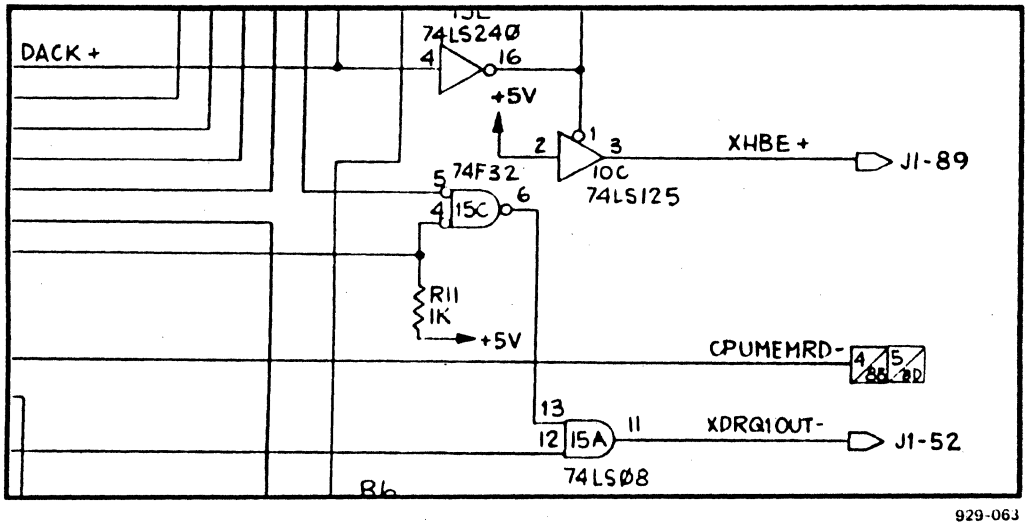


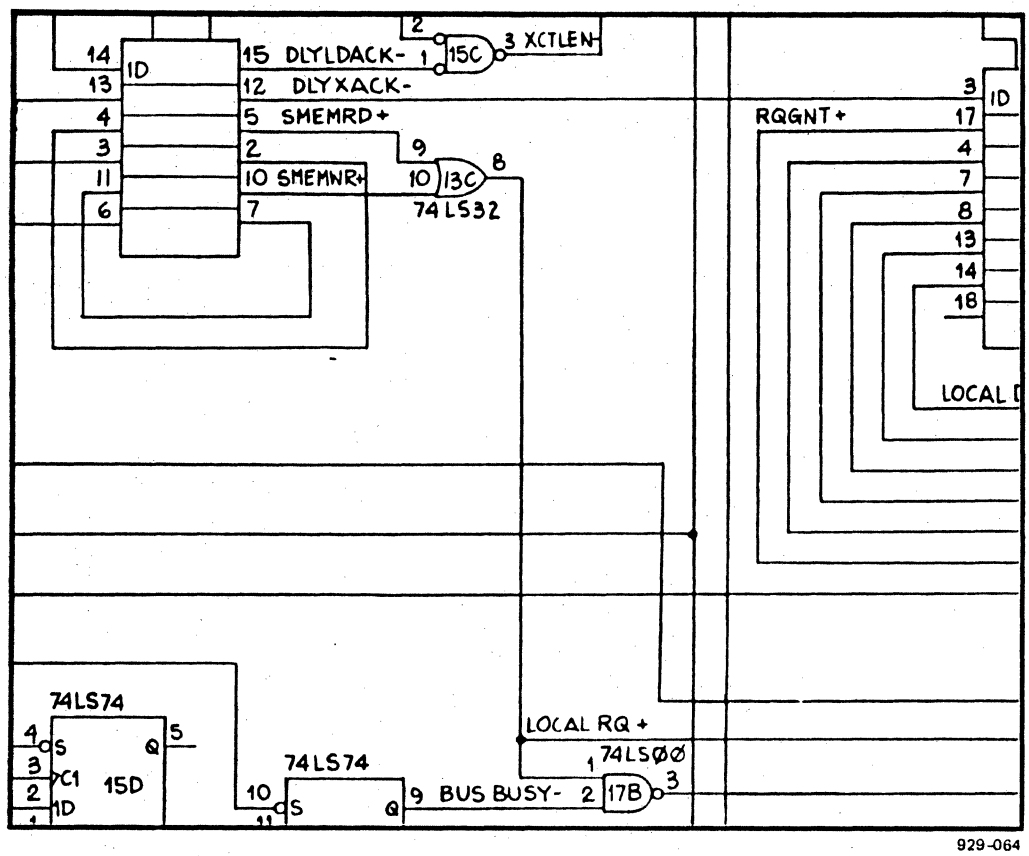
Figure 3-4. Mode 3 DMA Memory Read Timing Diagram (Page 2 of 2)

XDACKIN- goes low, pin 6 of 14C goes high, and DCLK- (Data Clock) clocks pin 5 of 14D, which also goes high. SDACK+ (Synchronous DMA Acknowledge) clocks pin 11 of 14D. Since pin 8 of 13C is high, there is a request pending. Pin 8 is tied to pin 12 of 14D. This means that pin 9 of 14D will be high, indicating that there is a bus available and the request has been granted. One clock later, LOCAL DACK- goes high, and LOCAL DACK- at pin 16 of 13E goes low, which enables the DMA.



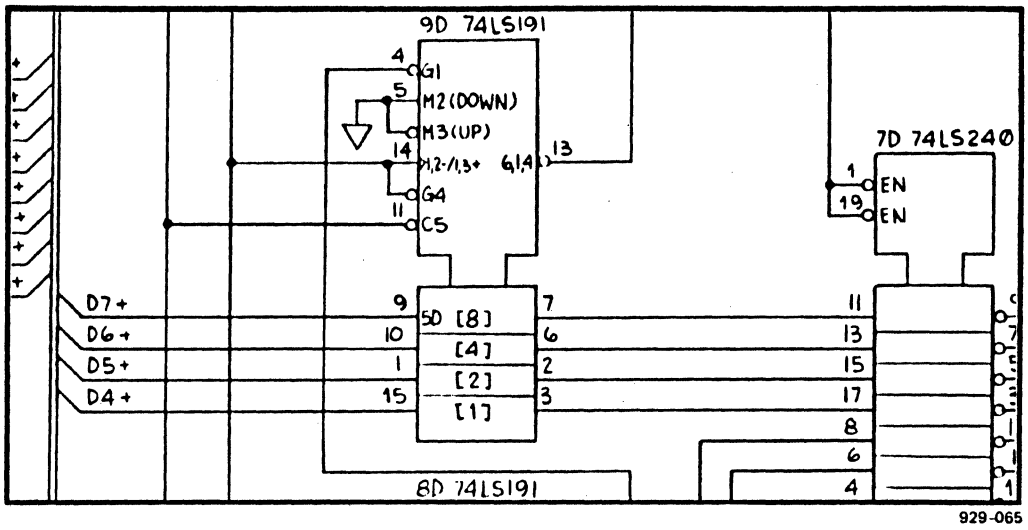
(From Figure B-1, Page 3, Coordinate 3C.)

When XACKIN+ is high, pin 11 of 14C generates XMODE3-, which is low-asserted. This means that the address line is asserted, so a read is being performed from the CPU. When pin 3 of 15C is low, XCTLEN- enables transceiver 13E, generates XMEMRD- at pin 3, and sends it to the CPU.

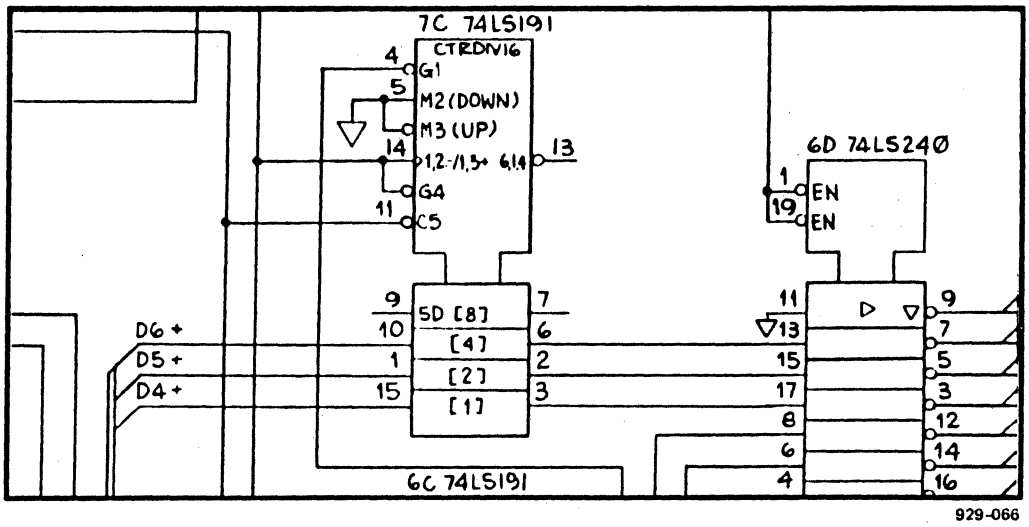


(From Figure B-1, Page 3, Coordinate 6C.)

When LOCAL DACK- is asserted, the address is driven on the X-Bus address lines through inverted buffers 7D, 5D, and 6D. As shown in the following two windows, the address counters (8D, 9D, 4C, 5C, 6C, and 7C) are incremented at the trailing edge of LOCAL DACK-.

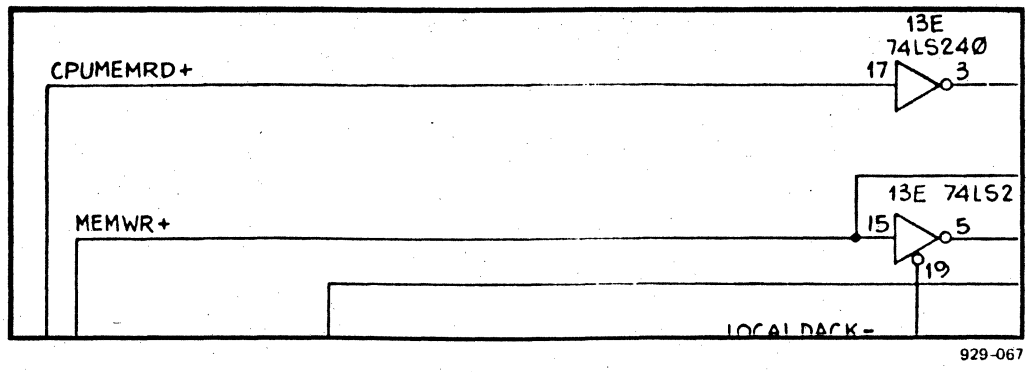


(From Figure B-1, Page 4, Coordinate 4C.)



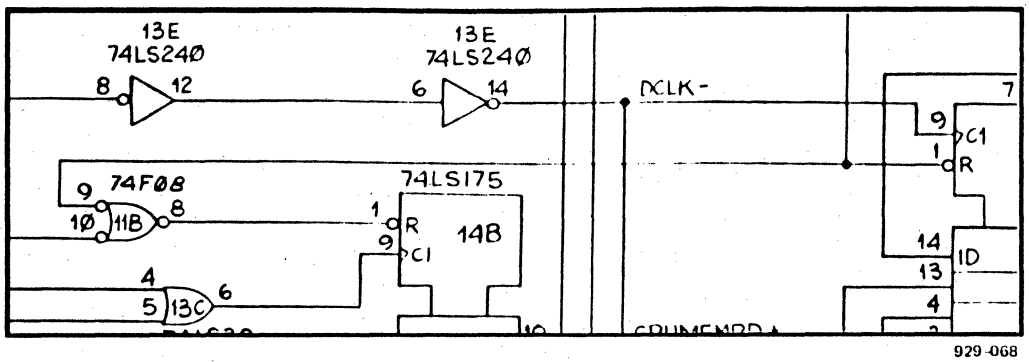
(From Figure B-1, Page 5, Coordinate 4C.)

The mode 3 master DMA supplies the address and control lines during the DMA cycle. When the CPU receives a DMA, and when an XMEMRD- from pin 3 of 13E is asserted, the CPU issues XACK-, indicating that the data has been supplied.



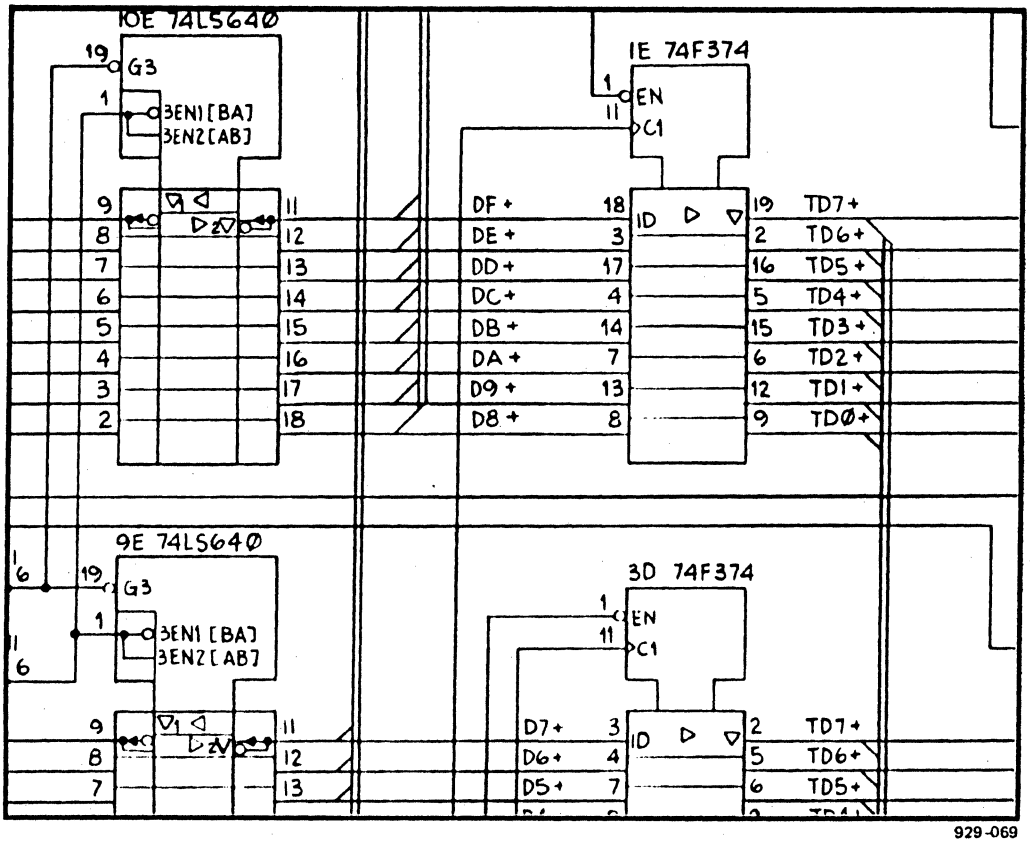
(From Figure B-1, Page 3, Coordinate 6D.)

Two clocks later, the CPU issues a XACK-. The delay on XACK- at pin 3 of 13D goes low, pin 2 of 13D goes low, and pin 11 of 13C goes low, clearing the request. When the CPU returns with XACK- (indicating that the CPU has supplied the data and cleared the request), pin 8 of 13C goes low. One clock later, pin 2 of 13D goes low, forcing XACK- low. Since LOCAL DACK- is already low, pin 11 of 13C and pin 8 of 11B are low, clearing pin 1 of 14E and 14B.



(From Figure B-1, Page 3, Coordinate 7D.)

This sequence clears the CPU memory, inverting it from high to low, bringing XMEMRD- high. Since pin 17 of 13E is low, the output of pin 3 (XMEMRD-) is high and completes the memory read cycle. At the same time, CPUMEMRD- at pin 11 of 14B goes high and clock the data on the data bus at pin 11 of 1E and 3D.



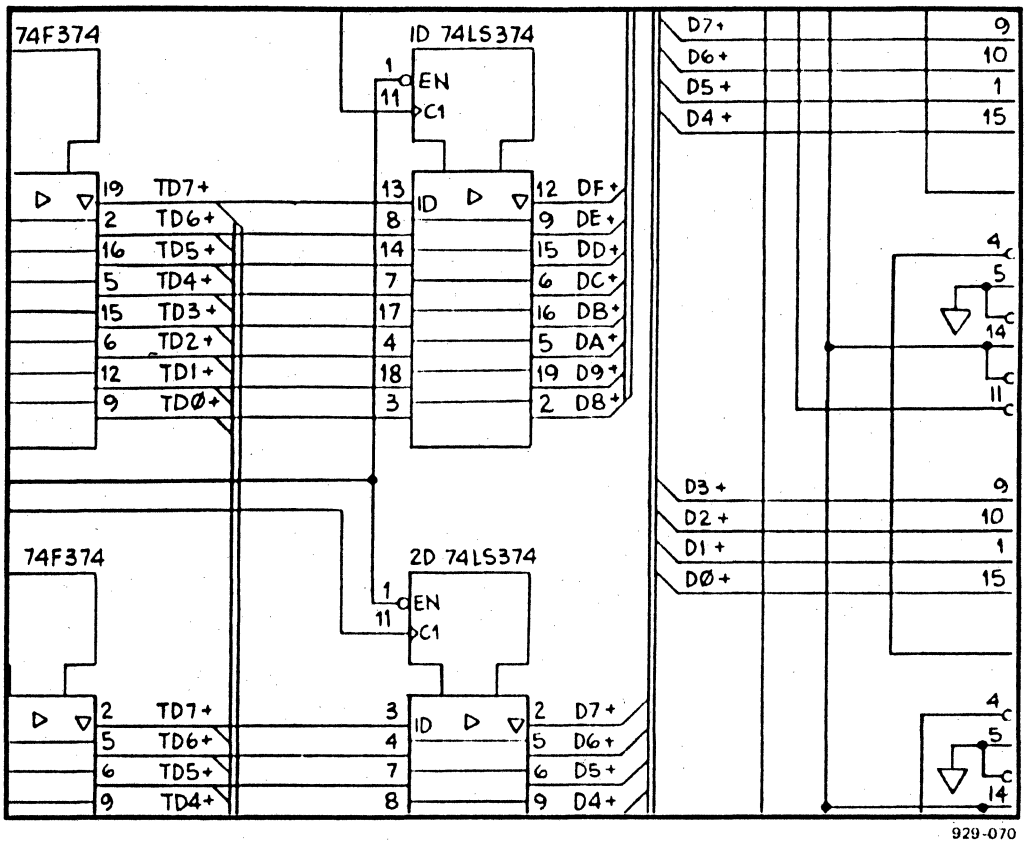
(From Figure B-1, Page 4, Coordinate 7D.)

Upon completion of DMA, pin 11 of 14B goes high, and CPUMEMRD- clocks flip-flop 13A at pin 3. It then clocks the data on the X-Bus data bus to register 1E and 3D. Pin 5 of 3A is driven high by gate 7A, requesting that a byte be written to the tape drive.

DMA MEMORY WRITE

The DMA memory write operation is identical to the DMA memory read operation, except for the following:

- o TPRDOP+ is enabled
- o MEMWR+ is asserted to write the content from registers 1D and 2D to memory



(From Figure B-1, Page 4, Coordinate 5D.)

A timing diagram for the DMA Memory Write operation is shown in Figure 3-5.

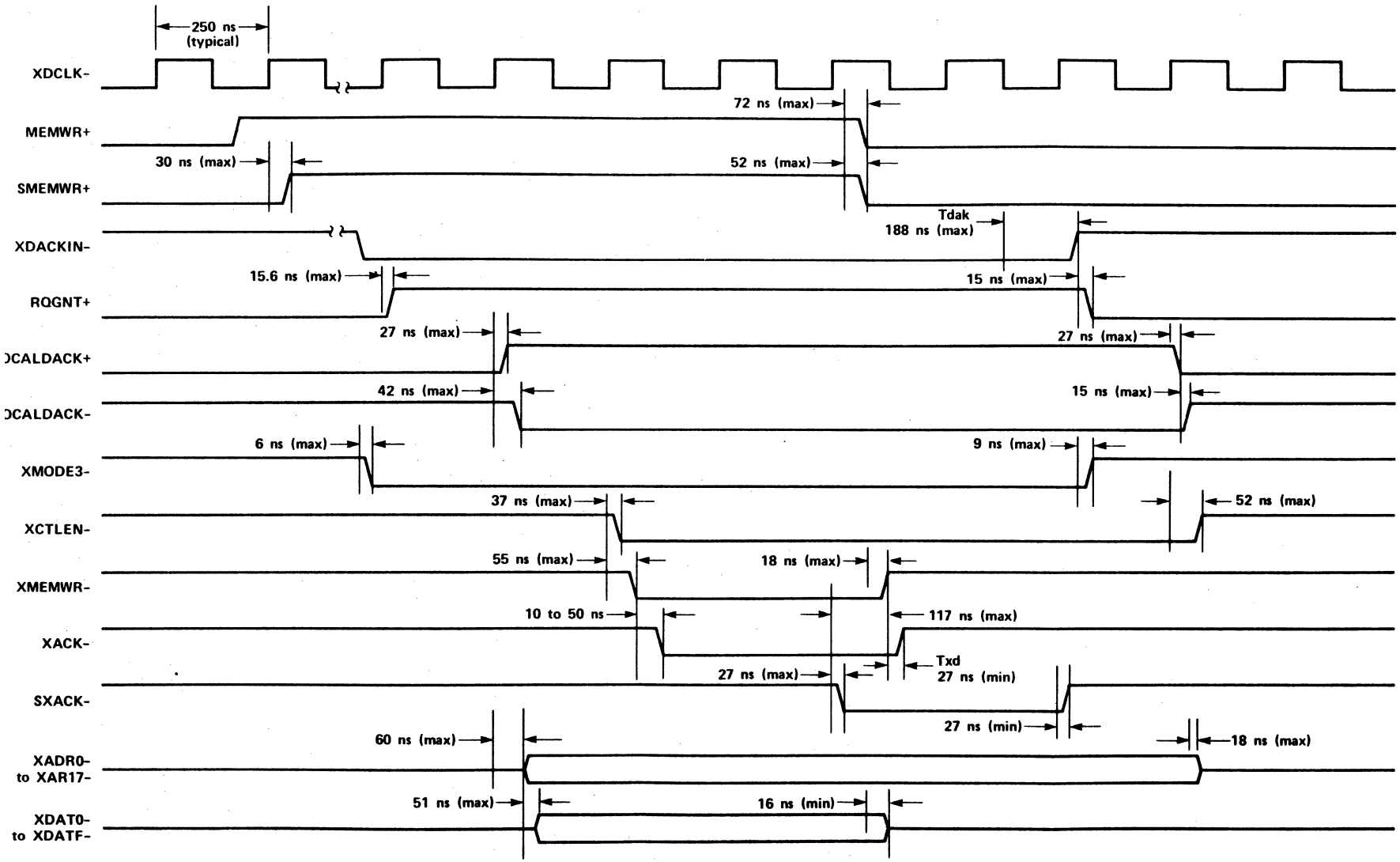


Figure 3-5. Mode 3 DMA Memory Write Timing Diagram

TAPE DRIVE INTERFACE LOGIC

The tape drive control circuitry communicates with the tape drive through a QIC-Ø2 interface, which contains

- four control lines from the tape drive control circuitry
- four control lines from the tape drive
- one 8-bit bidirectional bus (TBUS)

The control lines for the tape drive control circuitry and the tape drive are shown in Table 3-2 and Table 3-3, respectively.

For detailed information on the tape drive interface, see the manufacturer's drive manual in Chapter 4, "Drive Specifications," which includes the following:

- control lines
- bidirectional bus lines
- pin assignments
- interface signal timing
- signal terminations
- signal loading
- power interface

Table 3-2. Tape Drive Control Circuitry Control Lines

Signal	Function
REQUEST-	Driven by the control circuitry to signal the tape drive that a command is present on the TBUS
ON LINE-	Host-generated control signal asserted prior to initiating a read or write operation and reset to terminate a read or write operation
TRANSFER-	Data handshake signal from the Processor Module, used with ACKNOWLEDGE- from the tape drive to transfer data asynchronously across the interface
RESET-	Causes the tape drive to perform power-on/reset sequence

Table 3-3. Tape Drive Control Lines (Page 1 of 2)

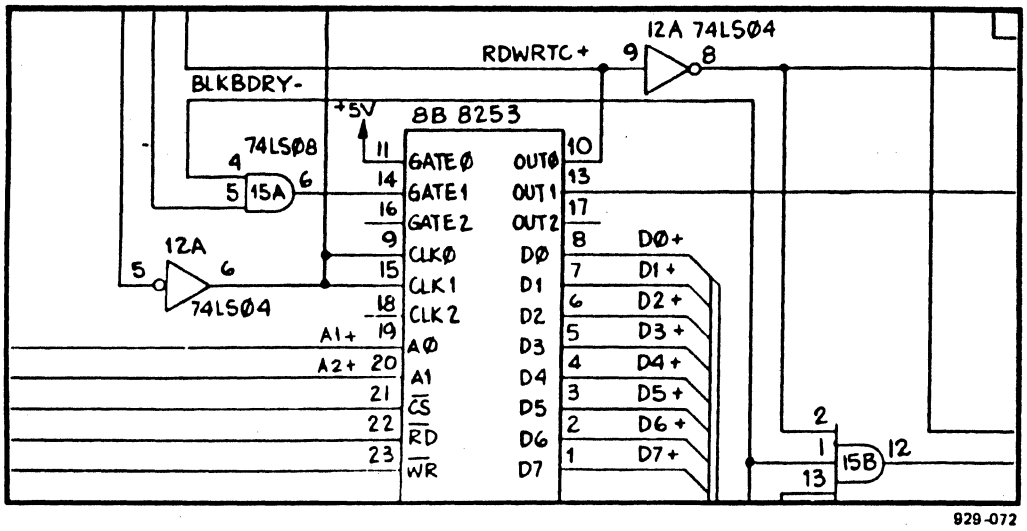
Signal	Function
READY-	Tape drive generated signal which indicates one of the following: o a command has been taken from the TBUS o data has been placed on the TBUS during a read-status sequence o a beginning-of-tape, retention, or erase sequence has been completed o a buffer is ready to be filled by the host, or a Write File Mark command can be issued, or ONLINE- deasserted during a write-data sequence o a Write File Mark command has been completed during a write-file-mark sequence o a buffer is ready to be emptied in the read mode o the tape drive is ready to receive a new command

Table 3-3. Tape Drive Control Lines (Page 2 of 2)

Signal	Function
EXCEPTION-	Signals the termination of an operation. The termination referred to may be a normal completion or an interruption due to a fault. The host must initiate a sense interrupt status.
ACKNOWLEDGE-	Handshake signal from the tape drive, used with TRANSFER- to transfer data across the TBUS asynchronously.
DIRECTION-	When true, data flows to the control circuitry. When false, data flows to the tape drive.

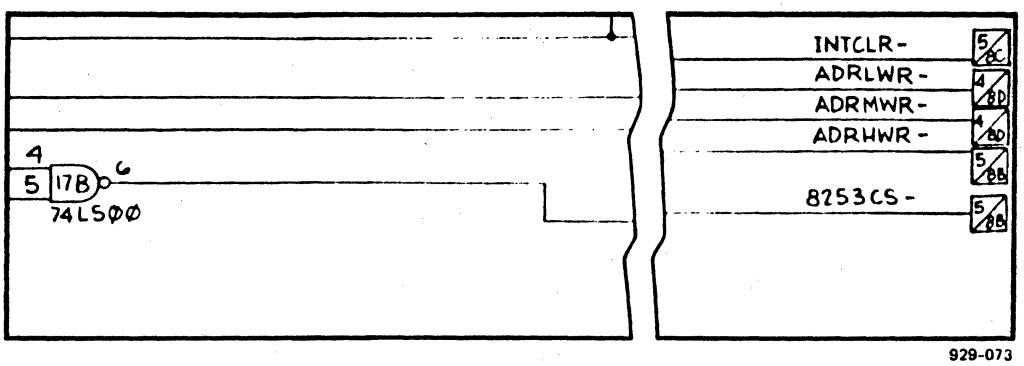
8253 PROGRAMMABLE INTERVAL TIMER

The tape control circuitry uses an 8253 programmable interval timer (8B) resident on the Tape Drive Control board. Counter Ø is used to count the number of bytes to be transferred to the tape drive. Counter 1 is used to detect the 512-byte block boundary. Counter 2 is not used. The pin assignments and functions of timer 8B are provided in Table 3-4.



(From Figure B-1, Page 5, Coordinate 7B.)

8B is selected when 17B issues 8253 CS- from pin 6. When selected, the CPU writes to several registers in 8B (using the XIOWR- strobe) to set the timing mode.



(From Figure B-1, Page 2, Coordinate 5A.)

Table 3-4. 8253 Programmable Interval Timer 8B Pin Assignments and Functions (Page 1 of 2)

Pin	Function
1 to 8	**Data Bus Lines (DØ+ through D7+).** Bidirectional buffered data bus, which interfaces to system bus.
9	**Clock Ø (CLKØ+).** Clock input of counter Ø.
10	**Output Ø (OUTØ+).** Used for counting the number of bytes to be transferred to the tape drive.
11	**Gate Ø (GATEØ+).** Gate input of counter Ø; strapped to +5 V.
12	**Ground.**
13	**Output 1 (OUT1+).** Used for the 512-byte block boundary counter.
14	**Gate 1 (GATE1+).** Gate input of counter 1.
15	**Clock 1 (CLK1+).** 1-MHz clock input of counter 1.
16	**Gate 2 (GATE2+).** Not used.
17	**Output 2 (OUT2+).** Not used.

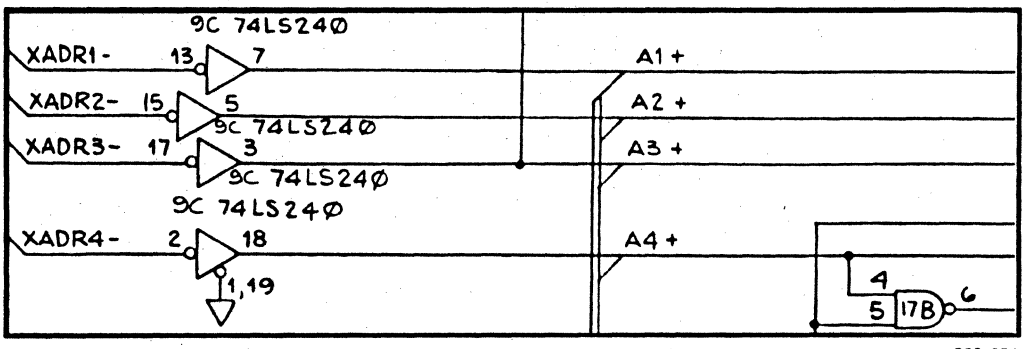
Table 3-4. 8253 Programmable Interval Timer 8B Pin Assignments and Functions (Page 2 of 2)

Pin	Function
18	**Clock 2 (CLK2+).** Not used.
19, 20	**Address Lines (A0+ and A1+).** Used to select one of the three counters or the Mode Control word for read or write operations; connected to X-Bus address lines XADR1- and XADR2-.
21	**Chip Select (CS-).** Enables the 8253 when 17B issues 8253CS- from pin 6.
22	**Read (RD-).** Signifies I/O read operation.
23	**Write (WR-).** Signifies I/O write operation.
24	**Power (+5 V).**

Internal registers of 8B are listed below with their addresses in the module relative to the module base I/O address (XXh):

A2+	A1+	Read Register (RD-)	Write Register (WR-)
Ø	Ø	Read counter Ø (XX9Ø)	Load counter Ø (XX9Øh)
Ø	1	Read counter 1 (XX92h)	Load counter 1 (XX92h)
1	Ø	Read counter 2 (XX94h)	Load counter 2 (XX94h)
1	1	-----	Mode Control word (XX96h)

The CPU can select one of several registers by using XADR1- and XADR2-, and can read from or write to the selected registers. XADR1- is inverted at 9C before generating to 8B as AØ+.



(From Figure B-1, Page 2, Coordinate 7B.)

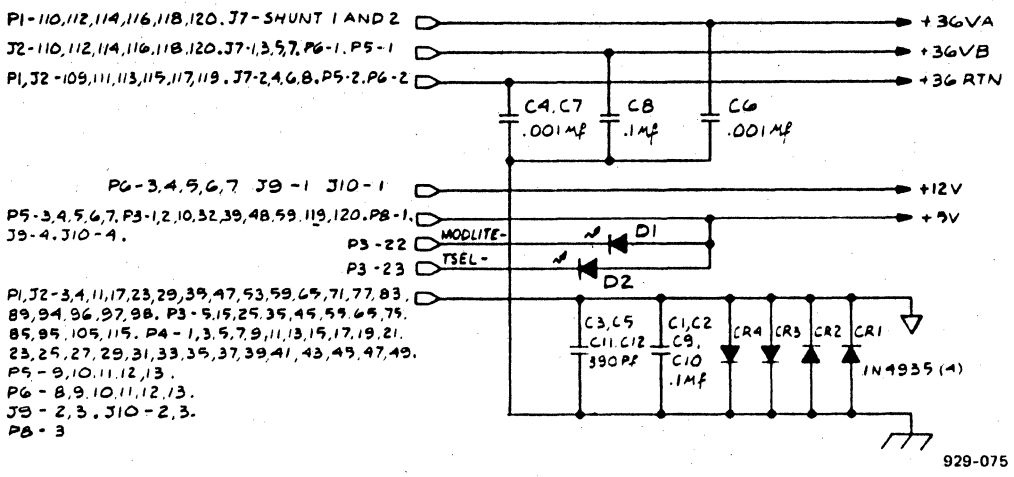
A1+ connects to the AØ+ input of 8B (pin 19), and A2+ connects to the A1+ input of 8B (pin 2Ø).

During I/O cycles, read operations are indicated when IORD- is generated from pin 19 of 5E to the RD- input of 8B, pin 22. Write operations are indicated when IOWR- is generated from pin 2Ø of 5E to the WR- input of 8B at pin 23.

POWER SUPPLIES

Two standard dc/dc power converters are used in the QIC Tape Module. One supplies +12 Vdc for the drive and the other supplies +5 Vdc for the drive and controller circuitry. For more information, refer to the Power System Manual.

QIC TAPE MODULE INTERCONNECT WIRE LIST



Signal	X-BUS IN P1	X-BUS OUT J2	CNT-RLR P3	TAPE P4	BRK P5	BRK P6	SDL J7	FAN P8	PWR J9	PWR J10
XPWREN-	5	5			15	15				
XDACK3-	6	6								
XDRQ3-	7	7								
XDACK2-	8	8								
XDRQ2-	9	9								
XDACK1 IN-	10		50							
XDRQ1 OUT-	12		52							
XDRQ4-	13	13								
XADRF-	14	14	60							
XADRE-	15	15	61							
XADRD-	16	16	62							
XADRC	18	18	63							
XADRB-	19	19	64							
XADRA-	20	20	66							

Signal	X-BUS IN P1	X-BUS OUT J2	CNT-RLR P3	TAPE P4	BRK P5	BRK P6	SDL J7	FAN P8	PWR J9	PWR J10
XADR17-	21	21	67							
XADR16-	22	22	68							
XADR15-	24	24	69							
XADR14-	25	25	70							
XADR13-	26	26	71							
XADR12-	27	27	72							
XADR11-	28	28	73							
XADR10-	30	30	74							
XADR9-	31	31	76							
XADR8-	32	32	77							
XADR7-	33	33	78							
XADR6-	34	34	79							
XADR5-	36	36	80							
XADR4-	37	37	81							
XADR3-	38	38	82							
XADR2-	39	39	83							
XADR1-	40	40	84							
XADR0-	42	42	111							
XPIN+	44		116							
XPOUT+		44	117							
X33KHZ SYNC+	46	46			14	14				
XINTR5-	48	48								
XINTR3-	49	49								
XINTR4-	50	50	109							
XINTR2-	51	51								
XINTR1-	52	52								

Signal	X-BUS IN P1	X-BUS OUT J2	CNT-RLR P3	TAPE P4	BRK P5	BRK P6	SDL J7	FAN P8	PWR J9	PWR J10
XINTRØ-	54	54								
XMODE3-	55	55	54							
XMEMRD-	57	57	112							
XMEMWR-	58	58	56							
XDMAEN-	6Ø	6Ø	11Ø							
XMODE2-	61	61								
XDATF-	62	62	1Ø8							
XDATE-	63	63	1Ø7							
XDATD-	64	64	1Ø6							
XDATC-	66	66	1Ø4							
XDATB-	67	67	1Ø3							
XDATA-	68	68	1Ø2							
XDAT9-	69	69	1Ø1							
XDAT8-	7Ø	7Ø	1ØØ							
XDAT7-	72	72	99							
XDAT6-	73	73	98							
XDAT5-	74	74	97							
XDAT4-	75	75	96							
XDAT3-	76	76	94							
XDAT2-	78	78	93							
XDAT1-	79	79	92							
XDATØ-	8Ø	8Ø	91							
XSPKR-	81	81								
XACK-	82	82	9Ø							
XLOCK-	84	84								
XBHE+	85	85	89							

Signal	X-BUS IN P1	X-BUS OUT J2	CNTRLR P3	TAPE P4	BRK P5	BRK P6	SDL J7	FAN P8	PWR J9	PWR J10
XRESET-	86	86	88							
XIOWR-	91	91	87							
XIORD-	92	92	86							
XPCLK+	93	93								
XDCLK-	95	95	118							
ONLINE-			3	28						
REQ-			4	30						
RST-			6	32						
XFER-			7	34						
ACK-			8	36						
READY-			9	38						
EXCEP-			11	40						
DIRC-			12	42						
TD7-			13	12						
TD6-			14	14						
TD5-			16	16						
TD4-			17	18						
TD3-			18	20						
TD2-			19	22						
TD1-			20	24						
TD0-			21	26						
MODLITE-			22							
TSEL-			23							
XDACK1 OUT-		10	51							
XDRQ1 IN-		12	53							

4 DRIVE SPECIFICATIONS

ARCHIVE
CORPORATION

SCORPION™

1/4" Streaming Tape Drive
PRODUCT DESCRIPTION

Part Number 20271-001

March 1984

APPENDIX A: QUARTER-INCH CARTRIDGE TAPE MODULE SPECIFICATIONS

GENERAL

TAPE PERFORMANCE

Number of tracks:	9
Number of channels:	2 (read-after-write)
Tape capacity:	55M bytes
Tape backup time:	Typically one minute per each megabyte file. Actual time required for backup depends on system activity and file fragmentation.
Recording mode:	NRZI
Recording data density:	8,000 bpi
Encoding method:	4 to 5 RLL
Flux density:	10,000 ftpi
Track capacity:	6.6M bytes
Data transfer rate:	90K bytes per second
Maximum burst:	200K bytes per second
Tape speed:	90 ips
Start/stop time:	300 milliseconds

INTERFACE

ELECTRICAL

QIC-02, Revision D with command and interface timing as specified in the Archive Corporation 1/4" Streaming Tape Drive Product Description

DATA FORMAT

QIC-24, Revision D

RELIABILITY

MAXIMUM ERROR RATE

Soft write:	less than 1220 blocks (rewritten with a DC-600A tape)
Soft read:	1 in 10^8 bits read
Hard read:	1 in 10^{10} bits read

MTBF

5,000 POH, 30% duty cycle

MTTR

30 minutes

SERVICE LIFE

5 years

POWER REQUIREMENTS

INTELLIGENT TAPE DRIVE

Tolerance

+12 Vdc:	+/- Ø.8 A
+12 Vdc:	+/- 1Ø%
+5 Vdc:	+/- 5%

Ripple

+12 Vdc:	1ØØ mV p-p
+5 Vdc:	5Ø mV p-p

Operational Current

+12 Vdc:	1.75 A
+5 Vdc:	2.4 A

Tape Start or Stop Current

+12 Vdc:	+4.15 A up to 1 second
+5 Vdc:	Ø A

Power Dissipation (Streaming Mode)

+12 Vdc:	21 W
+5 Vdc:	12 W

Power Dissipation (Start, Stop, or Surge)

+12 Vdc:	5Ø W
+5 Vdc:	12 W

TAPE CONTROL CIRCUITRY

DC voltage

+5 V

Tolerance

+/- 5%

Current

1.2 A

Power Dissipation

6 W

SAFETY

ESD

5,000 V:	No observable effect
12,500 V:	Errors corrected via software intervention
17,500 V:	Error corrected via operator intervention
25,000 V:	No permanent damage

ENVIRONMENTAL

ALTITUDE

Operating:	-200 ft to +15,000 ft
Nonoperating:	-1,000 ft to +30,000 ft

TEMPERATURE

Operating:	+5°C to +45°C (+41°F to +113°F)
Nonoperating:	-30°C to +60°C (-22°F to +140°F)

HUMIDITY

Operating:	20% to 80%
Nonoperating:	85% at 60°C for 12 hours

THERMAL GRADIENT

Operating:	1°C per minute (33.7 F per minute)

SHOCK

Operating:	2.5g maximum (1.2 sine wave of 11 milliseconds duration on three orthagonal axes)
Nonoperating:	25g maximum (0.5 sine wave of 11 milliseconds duration on three orthagonal axes)

VIBRATION

5 Hz to 55 Hz

Sweep

15-minute cycle at Ø.Ø15 inches amplitude

Dwell

1Ø minutes each 4 major resonances:

5 to 1Ø Hz:	A = Ø.124 inches (3.2 mm)
1Ø to 25 Hz:	A = Ø.Ø4Ø inches (1.Ø mm)
25 to 55 Hz:	A = Ø.Ø15 inches (Ø.4 mm)

PHYSICAL

Height:	3.25 inches
Width:	5.75 inches
Depth:	8.45 inches
Weight:	3.75 lb

APPENDIX B: TAPE CONTROL BOARD SCHEMATIC DIAGRAMS

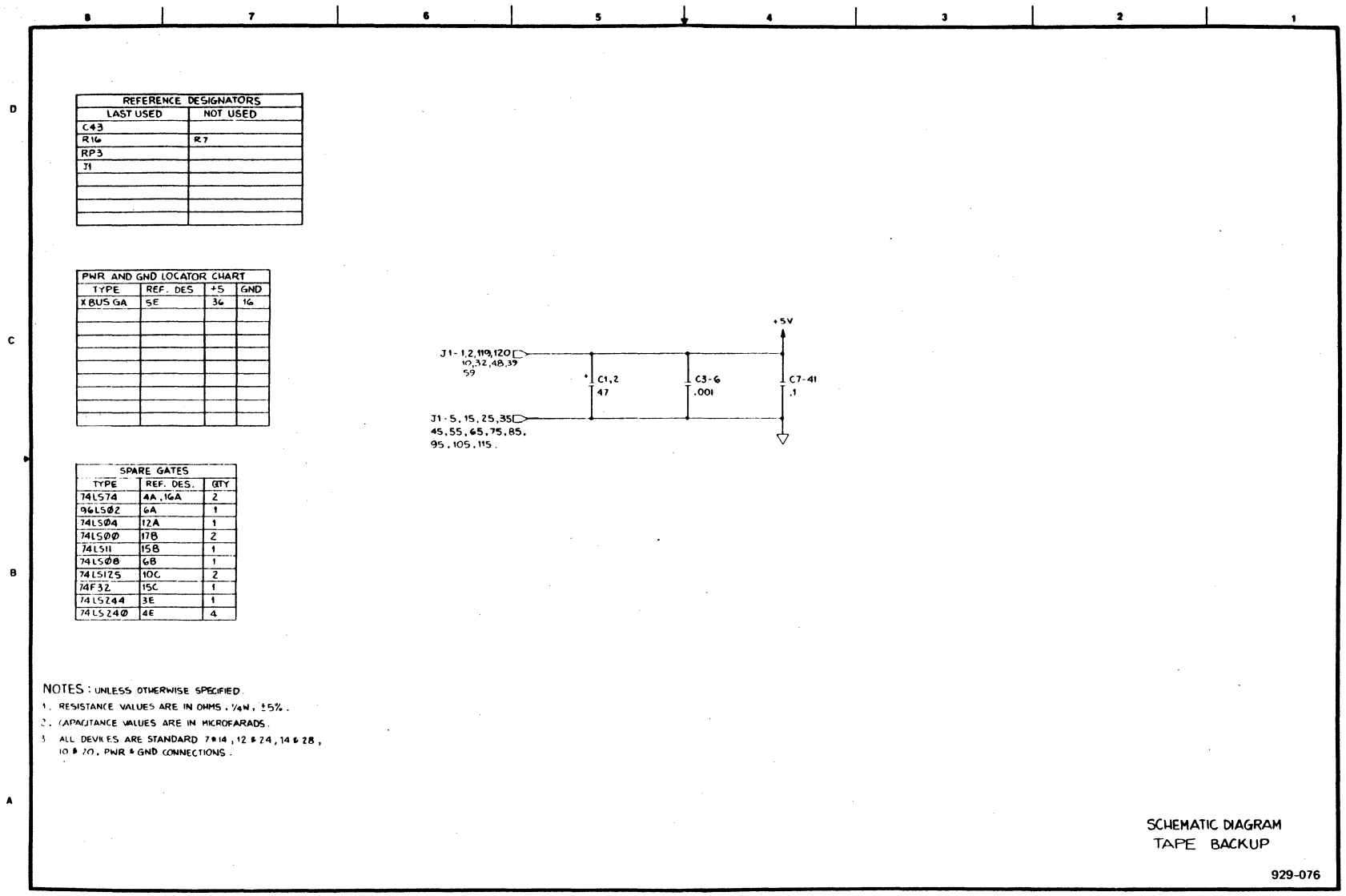


Figure B-1. Tape Control Board Schematic Diagram (Page 1 of 6)

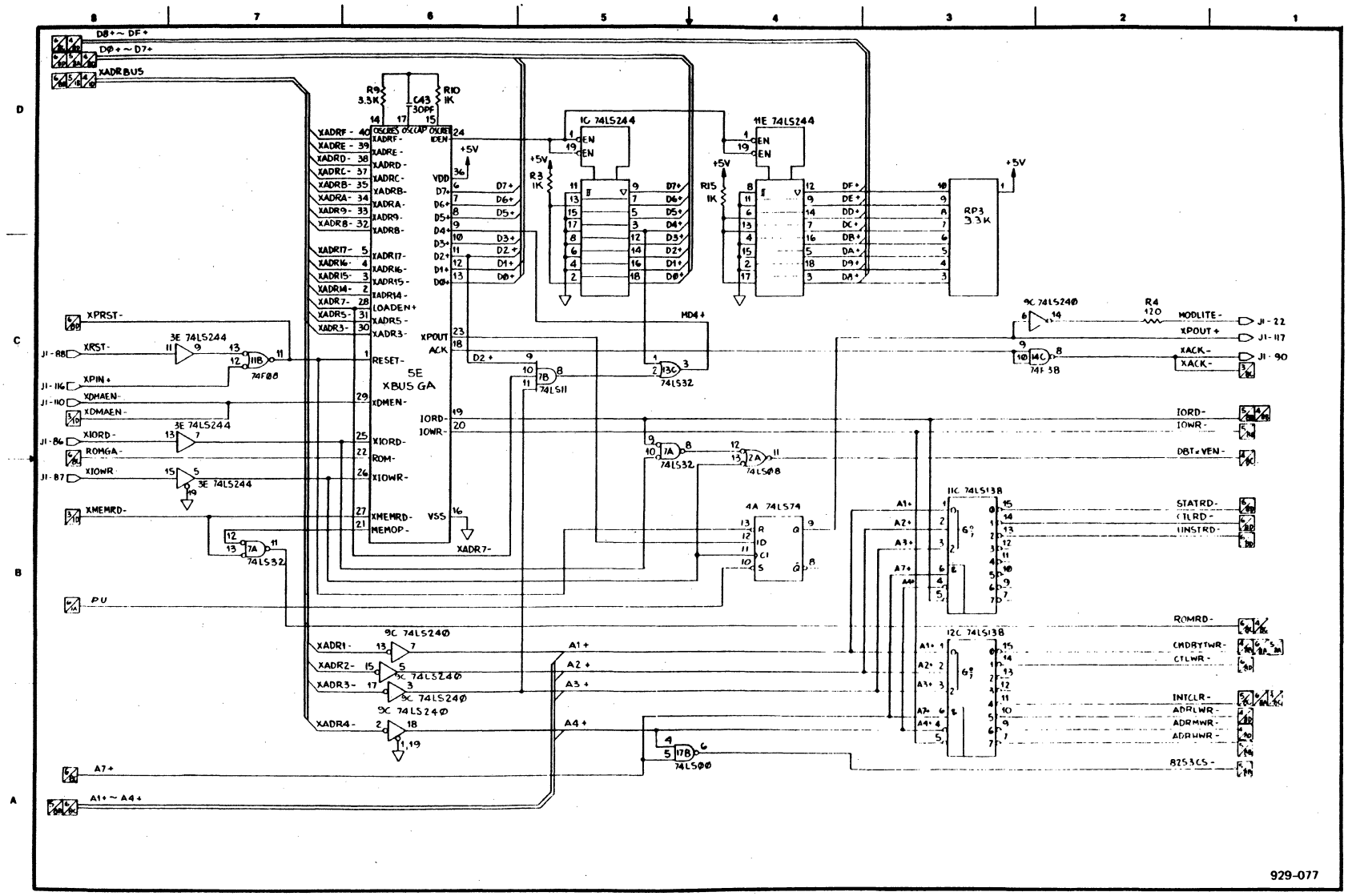


Figure B-1. Tape Control Board Schematic Diagram (Page 2 of 6)

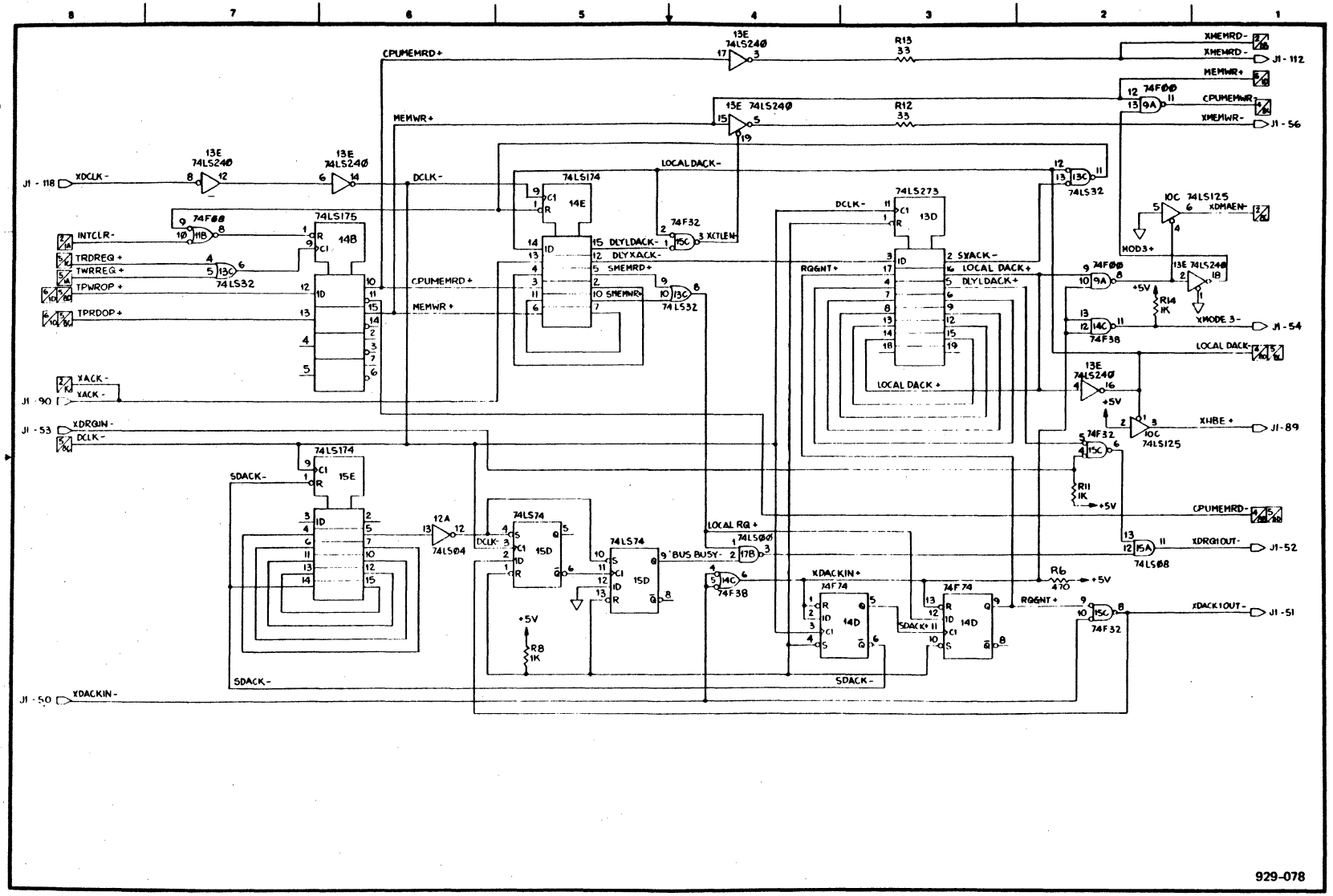


Figure B-1. Tape Control Board Schematic Diagram (Page 3 of 6)

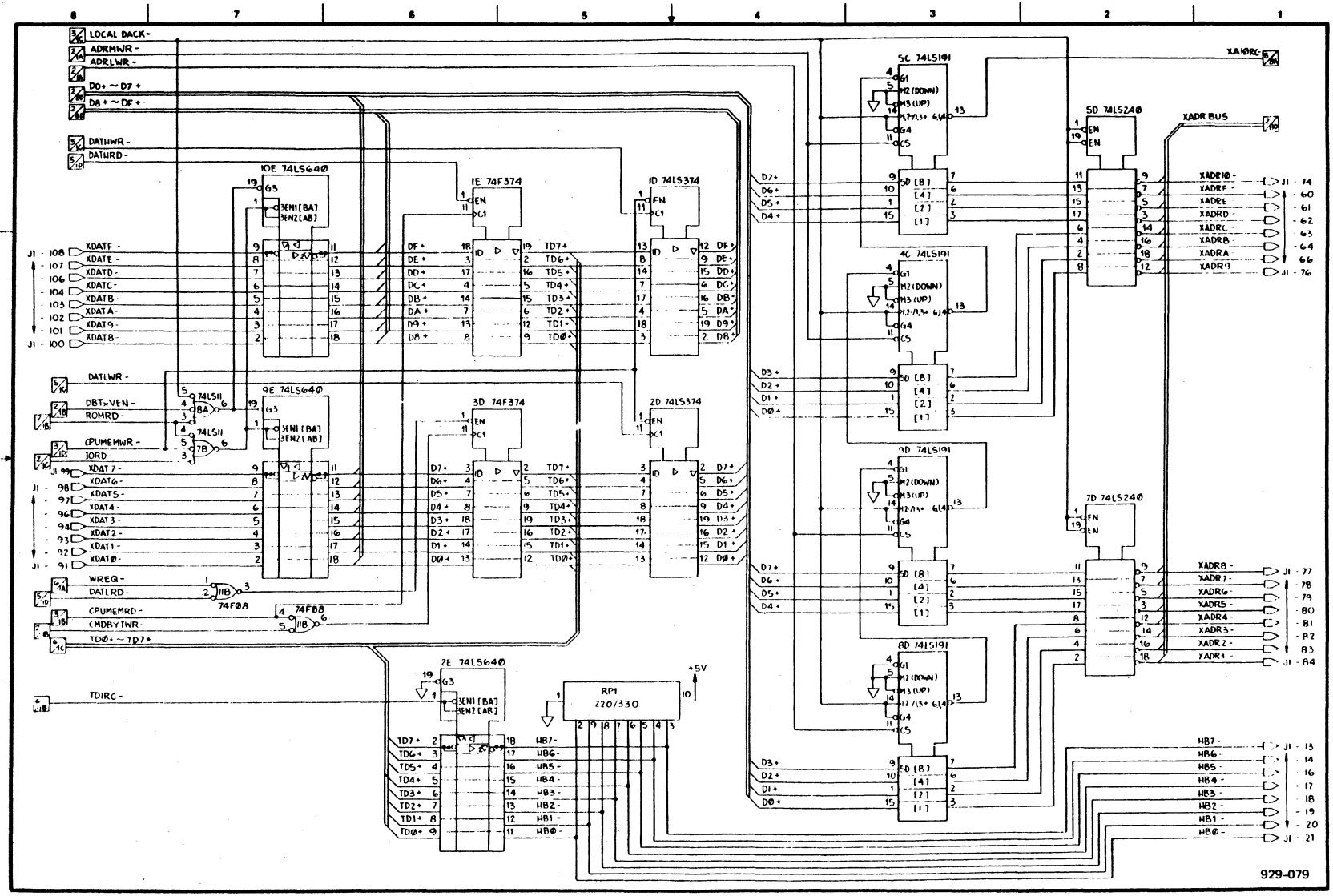


Figure B-1. Tape Control Board Schematic Diagram (Page 4 of 6)

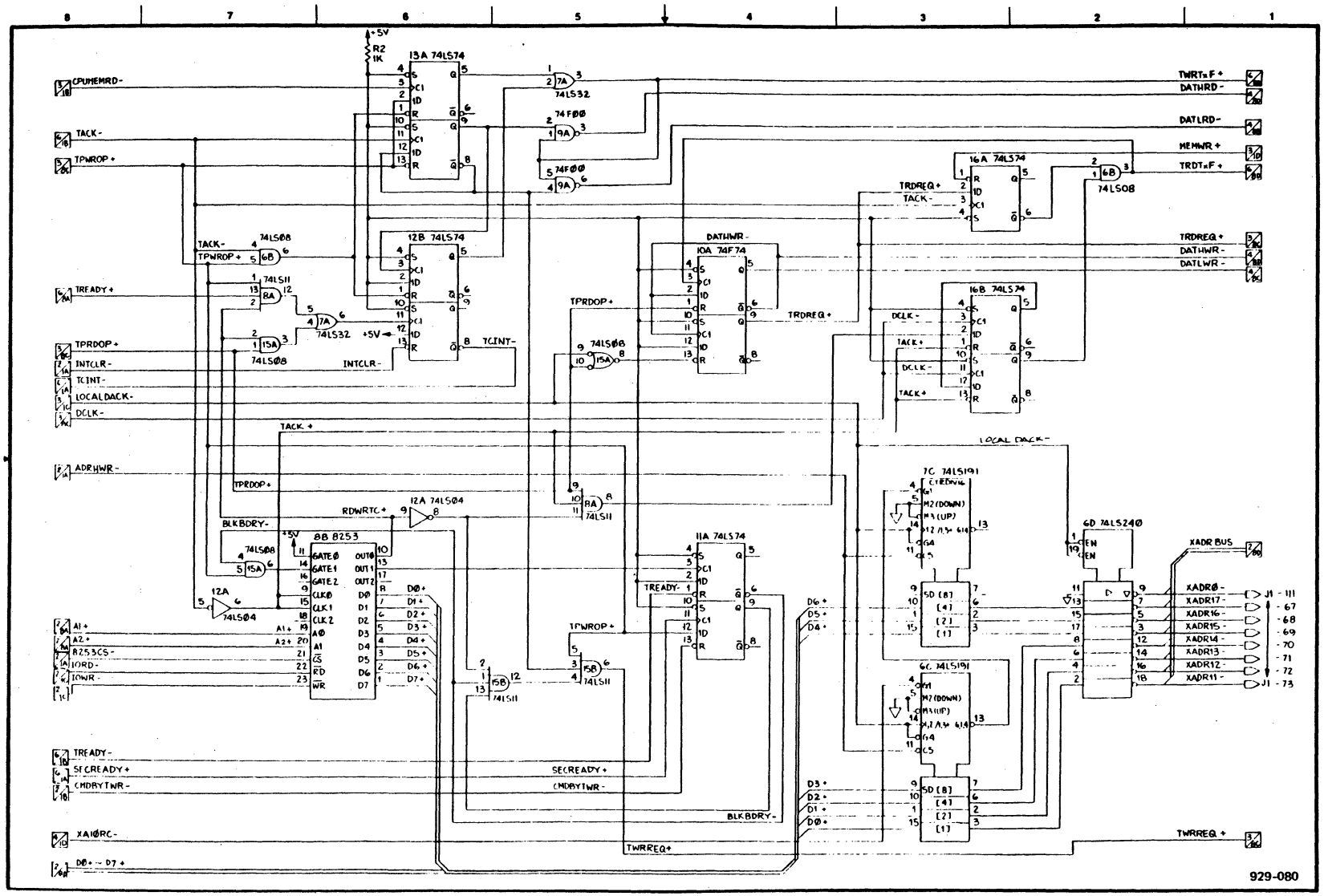


Figure B-1. Tape Control Board Schematic Diagram (Page 5 of 6)

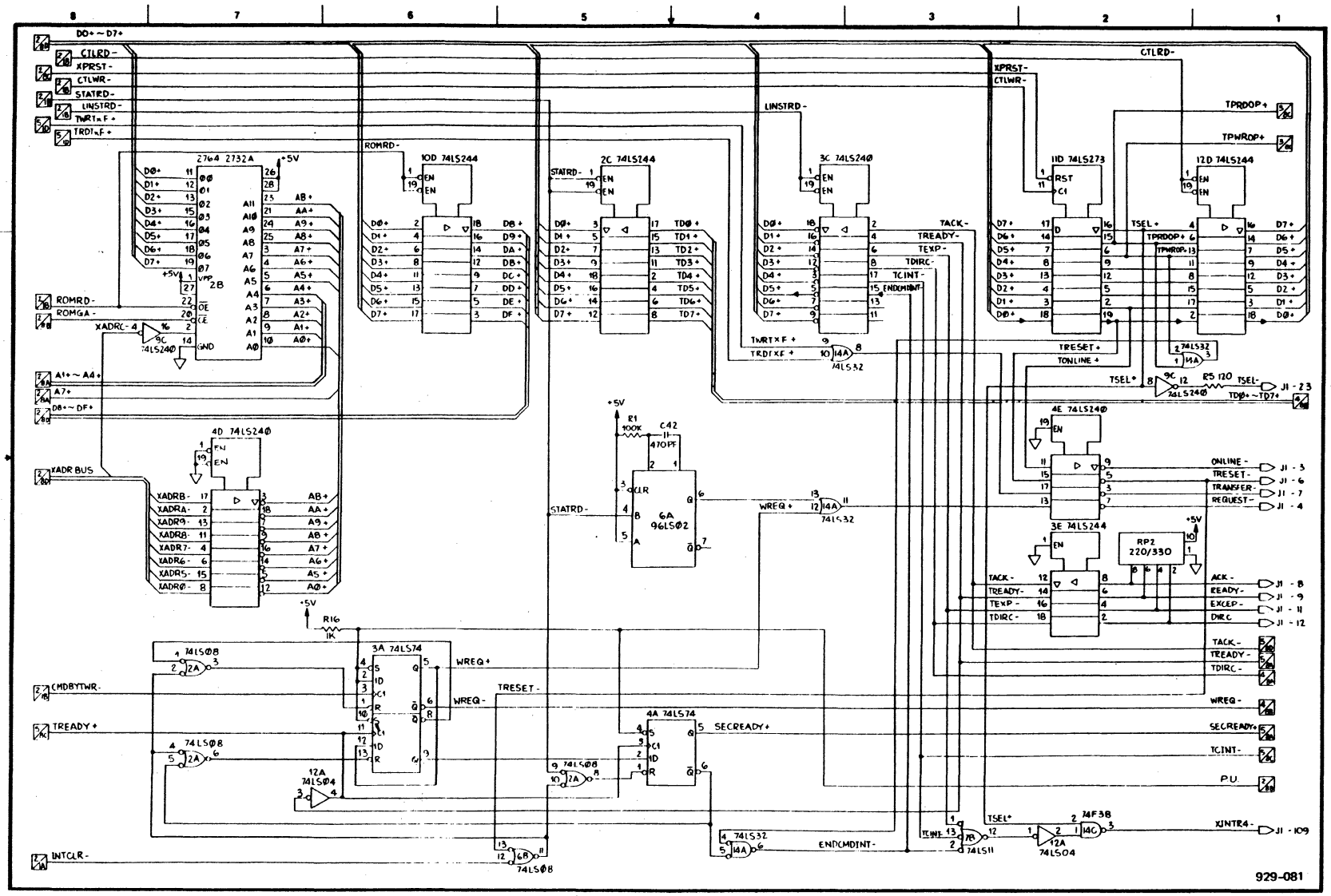


Figure B-1. Tape Control Board Schematic Diagram (Page 6 of 6)

QUARTER-INCH CARTRIDGE TAPE

The tape drive uses a quarter-inch cartridge (QIC) tape with a tape length of 600 feet. It is recommended that you use 3M DC-600A tape cartridges. Figure C-1 shows the internal components of the DC-600A, and how the components interact with the tape drive. Figure C-2 shows the safe and unprotected positions of the write protect plug.

The QIC tape drive has an MTBF of 5000 power-hours and a MTTR of one-half hour. Recommended full service life is five years.

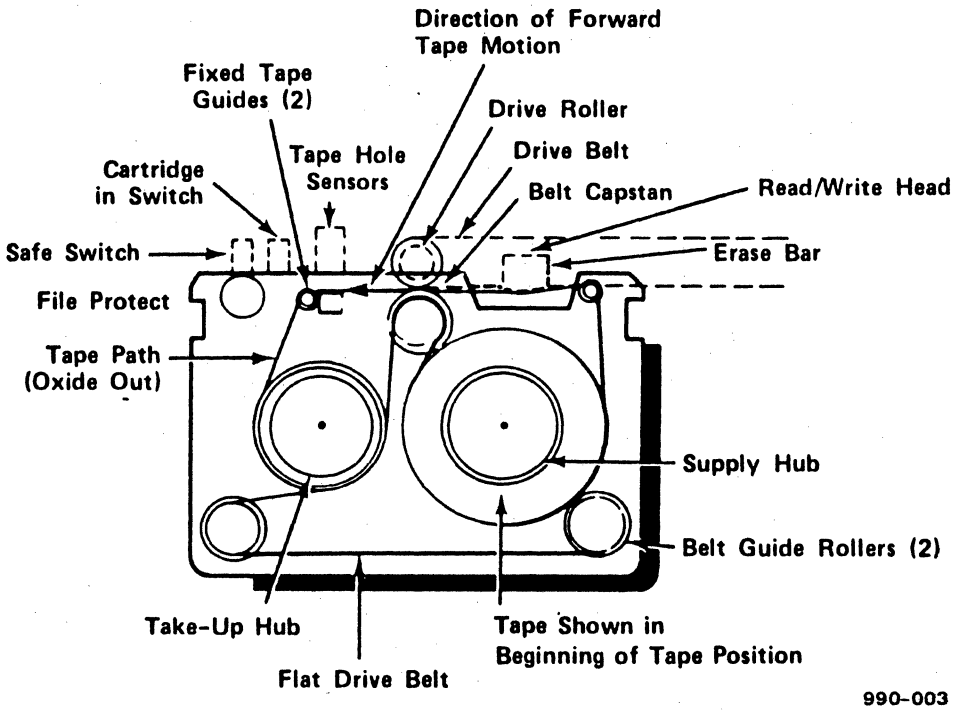


Figure C-1. Internal Components of the DC-600A Quarter-Inch Cartridge Tape

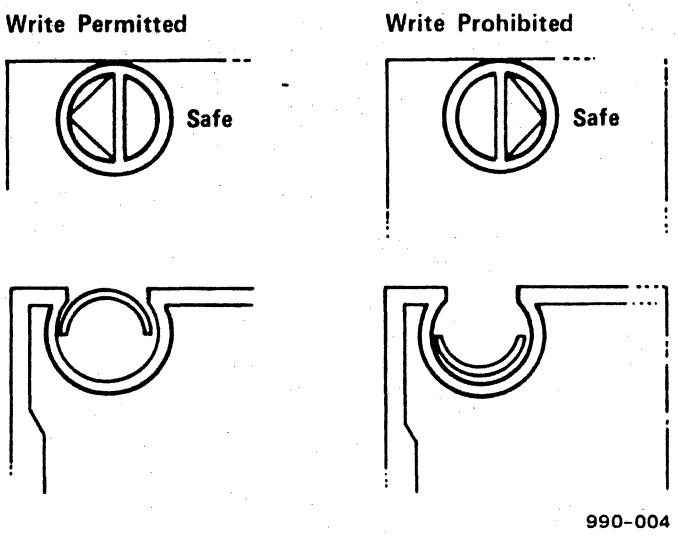


Figure C-2. Tape Write Protect Plug Positions

TAPE DRIVE HEAD MAINTENANCE PROCEDURE

This chapter covers the cleaning of the tape drive heads, to ensure maximum performance of the tape drive. If you are using new tape cartridges, the heads must be cleaned after every two hours of actual use. For other cartridge conditions, cleaning should be performed at eight-hour intervals during normal use. Normal use is defined by the specification of the unit. For hostile environments, such as high humidity or high temperatures, it may be necessary to increase the frequency of head cleaning to once every four to six hours.

The following troubleshooting procedure suggests some of the more common sources of poor performance. If the drive is reading erroneous data, follow these steps to discover the source:

- o do the first step of the troubleshooting procedure, then attempt to read the drive

- o if the error persists, do the second step, then attempt to read the drive

- o if the error still persists, do the third step, and so on

TROUBLESHOOTING PROCEDURE

1. Retension the cartridge by sending a Retension command request to the drive.

2. Clean the tape heads, as detailed in the following cleaning procedure.

3. Retension the cartridge by sending a Retension command request to the drive.

4. Replace the cartridge with a known good cartridge. The original cartridge may be worn.

5. Retension the cartridge by sending a Retension command request to the drive.

6. Change the tape drive.

7. Change the Quarter-Inch Cartridge Interface (QIC-Ø2) board.

8. Change the QIC-Ø2 flex cable.

CLEANING EQUIPMENT

To clean the tape drive heads, you will need the Inmac Tape Drive Head Cleaning Kit (part number 7150), which contains the following:

- swabs (noncotton)
- cleaning solution
- aerosol can containing compressed air

CLEANING PROCEDURE

To clean the tape drive heads, perform the following steps:

1. Remove the cartridge from inside the drive by firmly moving the slide lever away from the cartridge until the lever stop is reached. The lever action causes the head assembly to retract from the cartridge. The same action triggers an ejector which lifts the cartridge clear of the retaining lip, and pushes it out of the aperture.

2. Move the head assembly into the tape contact position by moving the upper slide lever to the right-hand stop. Power down the tape drive.

3. Dampen a swab by dripping cleaning solution onto the dual-colored spade end of the swab.

CAUTION

Do not dip the swab into the cleaning solution.

4. Insert the swab, spade end first, through the cartridge access slot until you touch the head.

5. Using the coarse, green side of the swab, clean the head with an up-and-down motion (toothbrush style).

6. Remove the swab and redampen it with another application of cleaning solution. Again, do not dip the swab into the cleaning solution.

7. Reinsert the swab and clean the head again with the fine, white side of the swab by using the same up-and-down motion you used for the coarse, green side.

8. Remove the swab. Now, insert a clean, dry swab and remove any residue of cleaning fluid.

9. Discard both swabs. Store unused swabs so that they do not collect dust or debris.

10. Inspect the sensor holes which are located on the inside near the head spring assembly. Clean the tape hole sensor openings as needed by using the compressed air from the aerosol container that comes with the kit.

11. Move the head assembly back into the retract position by moving the upper slide lever to the left-hand stop. The tape drive is now ready for use.

GLOSSARY

2732 EPROM (erasable programmable read-only memory). The 2732 EPROM contains the necessary information for the X-Bus master to bootstrap from the tape drive.

8253 programmable interval timer. The 8253 is a three-channel programmable counter/timer chip manufactured by Intel. It is used in the Quarter-Inch Cartridge Tape Module for interrupt control and DMA transfers. See the Intel Microprocessor and Peripheral Handbook.

buffer. A buffer is an amplifying signal driver, not necessarily with memory capability. Buffers that provide temporary storage for data are called storage buffers.

bus. A bus is a signal line or a set of lines used by an interface system to connect a number of devices and to transfer information. In general, three types of buses make up a bus set (which is also referred to as a bus): the address bus, the data bus, and the control bus. See also **X-Bus.**

bus cycle. A bus cycle is the transfer of data bytes or words across an interface by means of an interlocked sequence of control signals. Interlocked denotes a fixed sequence of events in which one event must occur before the next event can occur.

byte. A byte is a group of eight adjacent bits operated on as a unit. See also **high-order byte** and **low-order byte.**

clock cycle. A clock cycle is a signal waveform used to synchronize the timing of switching circuits and memory.

compatibility. Compatibility is the degree to which modules can be interconnected and used without modification.

daisy chain. A daisy chain is a specific method of propagating signals along a bus. The daisy chain method permits assignment of device priorities based on the electrical position of the device along the bus.

decoder. A decoder is a device that determines the meaning of a set of signals and then initiates a system operation based on those signals.

direct memory access logic. See **DMA.**

DMA (direct memory access). DMA allows a peripheral device to transfer data to or from memory without using the CPU, via a DMA controller in the Processor Module.

DMA address. When the DMA channel is initialized for a transfer, the DMA address is the initial memory address of the transfer. If the DMA address is read for status at any time, it is the current memory address of the transfer.

driver. See **buffer.**

flip-flop. A flip-flop is a digital circuit that can be in either of two states, depending on the input received, and which state it was in when the input was received.

handshake. A handshake is the exchange of control signals between the CPU and a device, or devices.

high-order byte. A high-order byte is the most significant byte in a word (bits 8h to Fh). The high-order byte is also called the odd byte, since it always has an odd address in memory. See also **byte.**

identification polling sequence. The identification polling sequence is a routine in the bootstrap ROM of the Processor Module. The sequence is used to identify modules connected to the X-Bus.

interface. An interface is a shared boundary between two systems, or between parts of two systems, through which information is conveyed.

interrupt logic. Interrupt logic interrupts the CPU so that it can service an I/O or peripheral device.

I/O pins. Input/output (I/O) pins are the pins of a chip through which signals are input or output.

low-order byte. A low-order byte is the least significant byte in a word (bits Øh to 7h). The low-order byte is also called the even byte, since it always has an even address in memory. See also **byte.**

manual reset. A manual reset is a system reset brought about when the user presses the reset button on the back of the Processor Module. See also **reset.**

mode 3 DMA. Mode 3 DMA performs transfer operations that allow other bus masters besides the Processor Module CPU to independently access the buses and to support data transfers without direct program control.

motherboard. The motherboard interfaces to all boards and power supplies.

NMI. See **nonmaskable interrupt.**

nonmaskable interrupt (NMI). During the X-Bus module identification polling sequence, a nonmaskable interrupt signals a ready timeout to signify that no additional modules are connected to the X-Bus.

port. A port is an I/O address, usually containing (if a status port) or requiring (if a command port) specific data. A port can allow access to several registers. See also **register.**

power-up reset. A power-up reset is an automatic system reset that occurs when the power is turned on. See also **reset.**

QIC-Ø2 interface. The QIC-Ø2 interface is used to transmit data, commands, and status information to and from the tape drive. (See the Archive Corporation 1/4" Streaming Tape Drive Product Description in Chapter 4, "Drive Specifications.")

register. A register is a temporary memory location for data.

reset. A reset can be either a system reset, as defined by the reset pin functions of the various chips connected to the system reset function, or a software register reset, equivalent to a clear. See also **power-up reset** and **manual reset.**

set. To set is to write a logical 1 or series of 1s to a register.

signal. A signal is the physical representation of logic.

signal line. A signal line is one of a set of signal conductors in an interface system used to transfer messages among interconnected modules.

system. A system is a set of interconnected elements that achieve a given objective through the performance of a specified function.

word. A word is 16 bits or 2 bytes.

workstation master. A workstation master is a master module within a workstation.

X-Bus. X-Bus is a standard asynchronous system bus that allows total configurability and interconnection of the workstation modules. The X-Bus supports two independent address spaces: memory and I/O. The X-Bus structure is built upon the master-slave concept, allowing modules of different speeds to interface.

X-Bus Gate Array. The X-Bus Gate Array, located on the Tape Drive Control board in the Quarter-Inch Cartridge Tape Module, is used for module identification, I/O read and I/O write, and bootstrap requests from the CPU.

X-Bus master. An X-Bus master is the module that controls the X-Bus.