PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AR

BTC UDA50-0-1

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER 075AR

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FIELD MAINTENANCE PRINT SET

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TABLE OF CONTENTS

DWG. NUMBER	DESCRIPTION
*D-UA-UDA50-0-0	ADAPTER ,UNIBUS DISK
*K-PL-UDA50-0-DBP	ADAPTER, UNIBUS DISK
*B-DD-M7161-0	UDA #1
*D-UA-M7161-0-0	UDA #1
*K-PL-M7161-0-DBP	UDA #1
:D-CS-M7161-0-UDA1	UDA #1
* B-DD-M7162-0	UDA #2
* D-UA-M7162-0-0	UDA #2
* K-PL-M7162-0-DBP	UDA #2
* D-CS-M7162-0-UDA2	UDA#2
B-DD-M7485-0	UDA PR
D-UA-M7485-0-0	UDA PR
K-PL-M7485-0-DBP	UDA PR
K-CS-M7485-0-1	UDA PR
B-DD-M7486-0	UDA SI
D-UA-M7486-0-0	UDA SI
K-PL-M7486-0-DBP	UDA SI
K-CS-M7486-0-1	UDA SI

*NOTE: THESE DRAWINGS AND PARTS ARE INACTIVE.

UNIT VARIATIONS COVERED BY THIS PRINT SET
UDA50-00 *
UDA50-A

UDA5Ø

Field Maintenance Print Set

Digital Equipment Corporation

Print Set Part Number MP-Ø1331

REVISION HISTORY			
REV.	A	B	
ECO NUMBER	RELEASED TO ECO CONTROL AT REV A	UDA5Ø-CXØØ6 AP17FEB84 B. BLACKLEDGE	
DATE		3043 RPM 29 FEB 84	

DRN. K. Davis	DATE 23 FEB 82	TITLE digital
CHK'D. W. Main	DATE 23 FEB 82	ADAPTER, UNIBUS DISK
DES. ENG. M. A. Richeson	DATE 23 JUN 82	
RESP. ENG. M.A. Richeson	DATE 23 JUN 82	DOCUMENT NUMBER
FIELD SERVICE R. W. Scanlin	DATE 23 JUN 82	SIZE B · CODE TC · NUMBER UDA5Ø-Ø-1 · REV. B
NEXT HIGHER DOC.		SHEET 1 OF 1

SIZE B · CODE TC · NUMBER UDA5Ø-Ø-1 · REV. B

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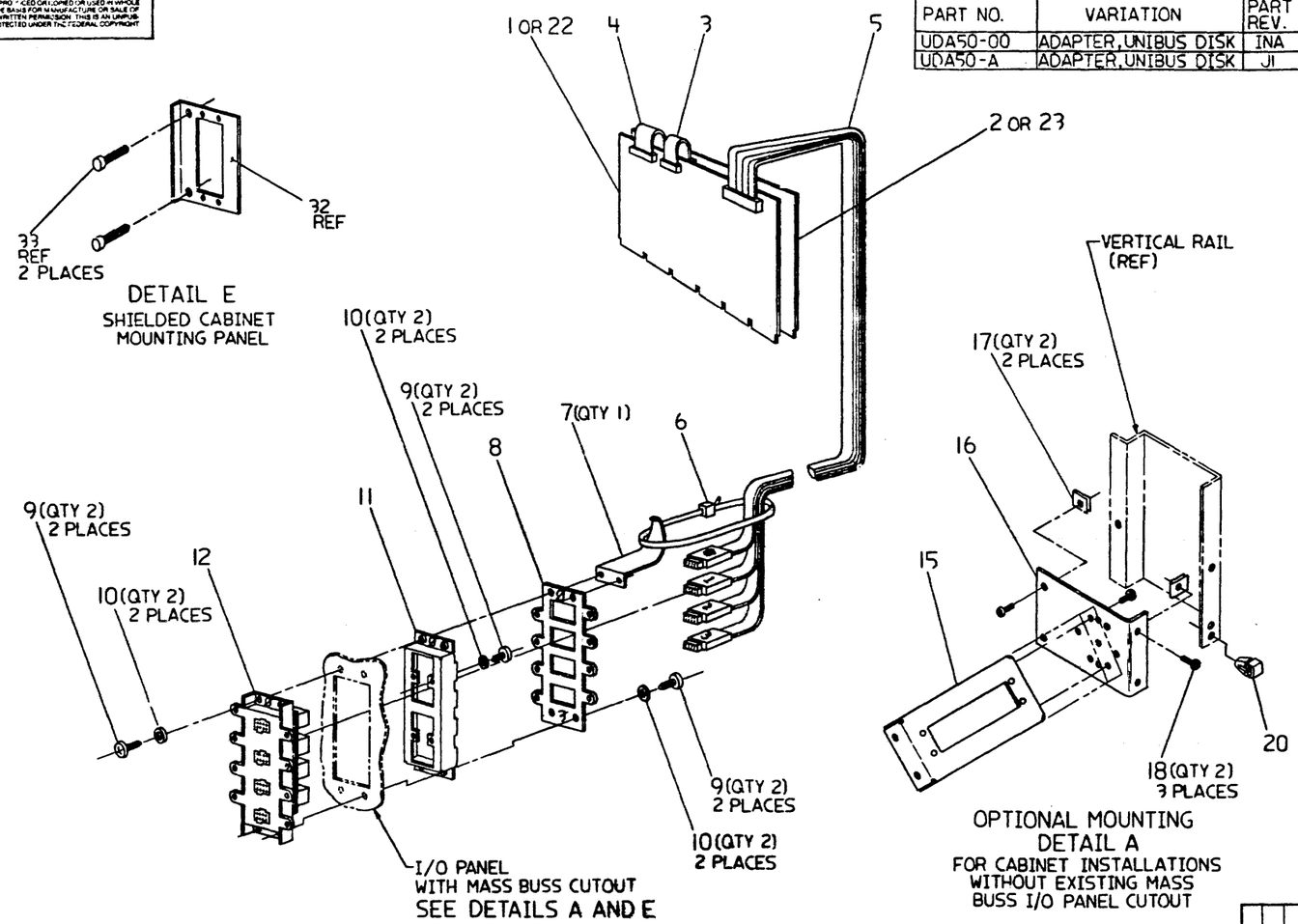

LEGEND		
PART NO.	VARIATION	PART REV.
UDA50-00	ADAPTER, UNIBUS DISK	INA
UDA50-A	ADAPTER, UNIBUS DISK	J1

NOTES:

1. DO NOT ASSEMBLE ITEMS 6 THRU 12. THIS WILL BE FIELD INSTALLED IN AN EXISTING I/O BULKHEAD WITH AVAILABLE MASS BUSS CUTOUT.
2. PROPERLY BAG AND TAG ITEMS FOR SHIPMENT.
3. FOR SPECIFICATIONS, INSTALLATION AND/OR PROCEDURE, REFER TO THE UDA50 DISK CONTROLLER USERS GUIDE, P/N EK-UDA50-UG.
4. ITEM 14 (BOOTSTRAP ROM) IS FOR USE IN M9312 MODULE WHEN APPLICABLE, IN PDP/11 CPU'S.
5. ITEM 19 (BOOTSTRAP ROM) IS FOR USE IN CPU MEMORY CONTROLLER MODULE WHEN APPLICABLE IN THE 11/750 CPU'S.
6. DELETED PER ECO UDA50-CX005.

CAUTION: OFF SHEET PARTS LIST EXISTS. SEE K-PL-UDA50-0-DBP(Z2142).

TOP DOC: K-DD-UDA50-0-DBU

REVISION HISTORY			DOC REV	PART REV
DATE	ECO NUMBER			
3098	REVISED & REDRAWN PER ECO UDA50-CX007 RAC 10 APR 85 M. LEWIS		H	H
3101	UDA50-CX008 BC 16 OCT 85 M. LEWIS		J	00 INA A/J
3180	UDA50-CX009 MCH 28 APR 86 R. FULLER		K	00 INA A/J1

DESCRIPTION	DRAWING NO.	PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)

INCHES TOLERANCES	ANGLES ±0°30'	APPLICABLE DIMENSION RANGE (CHECK ONE)	DIMENSION RANGE IN INCHES: OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
X = ±.1	SURFACE QUALITY	☐	±.02		±.03	±.05	±.10	
XX = ±.02		☐	±.004	±.008	±.012	±.016	±.024	±.04
XXX = ±.005	MICROINCHES	☐						

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: SEE PARTS LIST

FINISH

		DATE
DRN	R.A. Corradis	10 APR 85
CHK'D	R. MICHAUD	10 APR 85
DES. ENG.	M. LEWIS	10 APR 85
RESP. ENG.	R. JOHNSON	10 APR 85
MFG. ENG.	D. WILEY	10 APR 85

NEXT HIGHER DOC: K-DD-UDA50-0-DBU

TITLE: ADAPTER, UNIBUS DISK

digital

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV
D	UA	UDA50-0-0	K

SCALE NONE SHEET 1 OF 1

DRAWING NUMBER: DUA UDA50-0-0

DRAWING NUMBER: 1 OF 1

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QUANTITY PER VARIATION/REVISION 00 INA	A J1
1	1	D-UA-M7162-0-0	M7162-00		UDA#2 (UNIBUS DISK ADAPTER BOARD#2	1	-
2	2	D-UA-M7161-0-0	M7161-YA		M7161 W BLASTED ROM'S,4-LAYER HEX	1	-
3	3	C-IA-7018447-0-0	70-18447-00	B	40 PIN FLAT CABLE ASSEMBLY	1	1
4	4	C-IA-7018448-0-0	70-18448-00		50 PIN FLAT CABLE ASSEMBLY	1	1
5	5		17-00463-01	A	CABLE,COAX,ASSY,SI SHIELDED RIBBON	1	1
6	6		90-07032-00		TIE,CABLE BUNDL.DIA 0-1-3/4"=101	1	1
7	7	C-MD-7426095-0-0	74-26095-01		BRACKET,CABLE RETAINER	1	1
8	8	C-MD-7426090-0-0	74-26090-01		MOUNT,REAR CONN.	1	1
9	9		90-06011-01		SCREW,MACH PAN PHIL 4-40	12	12
10	10		90-06688-00		WASHER,HELICAL SPLIT SST .	12	12
11	11	D-IA-7426094-0-0	74-26094-01		HOUSING,REAR SHIELD	1	1
12	12	C-AD-7018454-0-0	70-18454-01		UDA BULKHEAD SUB-ASSEMBLY	1	1
13	13		37-00652-01		PKG KIT OPTION UDA50 CUSTOMER	1	1
14	14	SEE NOTE # 14	23-767A9-00	A	A9-01	1	1
15	15	D-IA-7425425-0-0	74-25425-01		BULKHEAD,I/O UDA,RETMA MNT	1	1
16	16	C-MD-7425426-0-0	74-25426-01		BRACKET,VERTICAL RAIL	1	1
17	17		90-07786-00		RETAINER,U-NUT 10-32X .	4	4
18	18		90-09700-00		SCREW,SEMS TRUSS PHIL 10-32	6	6
19	19	SEE NOTE # 19	23-990A9-00	A	A9-01	1	1
20	20		90-07867-00		MOUNT, PUSH,CABLE TIE	3	3
21	21	SEE NOTE # 21	EK-UDA50-UG		UDA50 CONTROLLER USER GUIDE	1	1
22	22	D-UA-M7486-0-0	M7486-00		UDA SI	-	1
23	23	D-UA-M7485-0-0	M7485-YA		M7485 W/BLASTED ROMS,4-LAYER HEX	-	1
24	24	B-MD-7427791-0-0	74-27791-01	A	MOUNT,GROUNDING	2	-
25	25		90-06634-00		WASHER,LOCK INTERNAL STEEL .	2	-
26	26	B-IA-7427505-0-0	74-27505-01		BRACKET,CABLE MOUNTING	1	-
27	27	C-IA-7427503-0-0	74-27503-01		ANGLE,GROUNDING	1	-
28	28	C-IA-7427504-0-0	74-27504-01		BRACKET,GROUNDING	1	-
29	29		90-06024-01		SCREW,MACH PAN PHIL 6-32	2	-
30	30		90-06558-00		NUT,HEX 6-32X .307AF CS/CAD	2	-
31	31		90-06633-00		WASHER,LOCK INTERNAL STEEL .	2	-
32	32		74-26407-05		PANEL,DOUBLE (MASS BUS)	-	1

REVISION HISTORY			KPL MATRIX FORMAT	SECTION A OF A	DRN: R. DUCHARME	
ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX		DATE: 03-NOV-85	D I G I T A L
RD	INITIAL	A	[A] 00,A		CHK'D: W.C.M.	TITLE PARTS LIST
BD	UDA50-CX001	B	[B]		DATE: 03-NOV-85	ADAPTER, UNIBUS DISK
RD	UDA50-CX002	C	[C]		DES.ENG: R. DUCHARME	
JW	UDA50-CX003	D	[D]		DATE: 03-NOV-85	DOCUMENT NUMBER
TK	UDA50-CX004	E	[E]			SIZE CODE NUMBER REV
TK	UDA50-CX005	F	[F]		RESP.ENG.: W. MATHRANI	K PL UDA50-0-DBP K
ML	UDA50-CX007	H	[H]		DATE: 03-NOV-85	
ML	UDA50-CX008	J	[J]			
RF	UDA50-CX009	K			MFG.ENG: K. SHAHEED	RELEASE DATE: 28-APR-86
					DATE: 03-NOV-85	RELEASE STATUS: RELEASED

BASIC PART NUMBER:	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:	EDIT #
UDA50	D-UA-UDA50-0-0	K-DD-UDA50-0-DBU	Z2142K.PLS	1

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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION		QUANTITY PER VARIATION/REVISION 00 J1	A J1
33	33		12-19534-01		SCREW, CAPTV SLOT	4-40	-	2

14 NOTE: SEE NOTE 4 ON ASSEMBLY DRAWING (D-UA-UDA50-0-0).
19 NOTE: SEE NOTE 5 ON ASSEMBLY DRAWING (D-UA-UDA50-0-0).
21 NOTE: SEE NOTE 3 ON ASSEMBLY DRAWING (D-UA-UDA50-0-0).

DIGITAL	TITLE	SIZE	CODE	DOCUMENT NUMBER	REV
	ADAPTER, UNIBUS DISK SECTION A OF A	K	PL	UDA50-0-DBP	K

SIZE	CODE	NUMBER	REV.
B	DD	M7161-0	D

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS			
B-DD-M7161-0	1		UDA #1	A	B	C	D
D-UA-M7161-0-0	2		UDA #1	A	B	B	C
K-CS-M7161-0-UDA1	15		UDA #1	B	C	D	E
K-PL-M7161-0-DBP	-		UDA #1	A	B	C	D
K-PC-M7161-0-DBC	-		P.C. DESIGN DATA BASE	B	B	B	B
		5014040-00	ETCH BOARD	B	B	B	B
D-EC-5014040-0-0	2		ETCH CUT DRAWING	A	B	B	C
D-MD-5014040-0-0	5		DRILL AND ETCH DRAWING	A	A	A	A

NOTES:

REVISIONS			
REV.	A	B	C	D
CHG NO.	INIT	M7161-CX001	M7161-CX02A	M7161-CX004
DATE	RPM 16 JUN 81	RPM 19 AUG 81	NL 26 Feb 82	SMB 7 Jul 82

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digital

USED ON OPTION/MODEL	
RA80	

DRN.	TAMARA J. [illegible]	26-Feb-82
CHK'D	W. Landry	1-MAR-82
ENG.	C. Ridgeway	2/1/82
PROD.	D. SWIFT N.L.	1-MAR-82

TITLE: UDA #1

SIZE	CODE	NUMBER	REV.
B	DD	M7161-0	D

SHEET 1 OF 1

DRB 128

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COMPONENT SIDE VIEW

17
81
1
15.688 REF.
1-1
1-7
SEE NOTE 3
SEE NOTE 2
MOUNT AS SHOWN
8.41 REF.
TH2
TH1
P5
P6
P2
D4 D3 D2 D1
E93 E82
E115 E105 E104 E92 E81 E73 E63 E59 E50 E40 E29 E18 E9 E7
E129
E123 E114 E102 E91 E80 E72 E58 E49 E39 F28 E17 E6
E122 E113 E90 E79 E71 E48 E38 E27
E121 E112 E100 E89 E78 E70 E57 E47 E37 E26 E16 E5
E128 E120 E111 E99 E88 E77 E69 E56 E46 E36 E25 E15 E4
E127 Y1 E110 E98 E87 E68 E45 E35 E24 E14 E3
E119 E109 E97 E86 E76 E67 E55 E44 E34 E23
E126 E118 E108 E85 E75 E66 E62 E54 E43 E33 E22 E13 E2
E125 E117 E107 E85 E84 E65 E61 E53 E32 E21
E124 E116 E106 E94 E83 E74 E64 E60 E52 E31 E20 E12 E1
C6 C5 C4 C3 C2 C1
4-4 4-7 4-3
4-8 4-31
4-14 4-37
4-9 4-32
4-15 4-38
4-10 4-33
4-16 4-39
4-11 4-34
4-17 4-40
4-12 4-35
4-18 4-41
4-13 4-36
4-19 4-42

WIRE ADDS FOR THIS AREA SHOWN ON SHT.2 (UA)

WIRE ADDS FOR THIS AREA SHOWN ON SHT.2 (UA)

NOTES:1.THE FOLLOWING ARE SPARES: R41, E39, E88, E97, E101, E103, E110, E118, E119, E121, E124, E127-E129.
2.MOUNT D1-D4 ON COMPONENT SIDE, LONGER LEG TO RIGHT. LEAVE LEADS APPROXIMATLY .18 LONG.
3.DO NOT INSTALL EYELET (ITEM 81) IN POSITION SHOWN.

STEP E	↑ Y AXIS NA	STEP	TIMES
REPEAT	→ X AXIS NA	STEP	TIMES

CHK	CHANGE NO	REV
	RELEASED TO ECO CONTROL AT REV A	A
	M7161- CX001 RA 18 AUG81 CRIDGEWAY	B
	M7161- CX004 SL 26 JUL 82 CRIDGEWAY	C

ETCH REV. B

SIGNATURES	DATE
DRN.	29 NOV 81
CHK'D.	23 DEC 81
MECH.ENG.	16 JUN 81
PROJ.ENG.	16 JUN 82
PROD.	16 JUN 82

digital

TITLE: UDA #1

SCALE 1.5/1 | SIZE D | CODE UA | NUMBER M7161-0-0 | REV C

SHT. 1 OF 4

NEXT HIGHER ASSY. B-DD-M7161-0

M7161-0-0 DUA 2

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E123 E114 E102 E91 E80 E72
E122 E113 E101 E90 E79 E71
E121 E112 E100 E89 E78 E70
E128 E120 E111 E99 E88 E77 E69
E127 Y1 E110 E98 E87 E68
E119 E109 E97 E86 E76 E67
E126 E118 E108 E96 E85 E75 E66
E125 E117 E107 E95 E84 E65
E124 E116 E106 E94 E83 E74 E64
C6 C5 C4

4-1 4-2 4-6 4-30 4-7 2-1 4-55 4-56 1-48 4-5
4-54 4-53 4-23 4-52 4-61 4-51 4-60 4-22 4-58 4-59 4-57 4-50 4-49 4-26 4-28 4-25 4-29 4-27 4-47 4-24
0-12 1-10 1-11 1-5 4-62 0-13
4-43 4-44 4-45 4-46 4-48 1-4 1-6 0-8 0-9

REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE: UDA#1

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
D	UA	M7161-0-0	C

SCALE 3/1 SHEET 2 OF 4

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LEGEND:
0-'XX' = PCO-UDA 001.
1-'XX' = PCO-UDA 004.
2-'XX' = PCO-UDA 011.

REWORK INSTRUCTIONS-INITIAL RELEASE

0-1.
0-2.
0-3.
0-4. } SEE D-EC-5014040-0-0
0-5.
0-6.
0-7.

WIRE ADDS-COMPONENT SIDE AS SHOWN:
0-8. FROM PTH ABOVE C68 TO PTH TO LEFT OF E86-1.
0-9. FROM E85-5 TO E76-11.
1-10. FROM E76-15 TO PTH ON LEFT OF E85.
1-11. FROM PTH BELOW E75-7&8 TO E87-10.
0-12. FROM E87-11 TO PTH BELOW E66 & E75.
0-13. FROM E66-7 TO E76-11.

COMPONENT DELETES:
1-14. DELETE CAPACITOR C70 (1012784).
1-15. " RESISTOR R42 (1300447).
1-16. " I.C. SOCKET XE55 (1215006-08).
1-17. " " XE56 " .
1-18. " " XE57 " .
1-19. " " XE58 " -08).
1-20. " " XE91 " -01).
1-21. " " XE100 " -06).
1-22. " " XE102 " -06).
1-23. DELETE I.C. SOCKET XE108 (1215006-01).

COMPONENT ADDS:
1-24. ADD RESISTOR R2 (1300229).
1-25. " " R12 (1300229).
1-26. " " R3 (1301972).
1-27. " RESISTOR R11 (1301972).
1-28. " I.C. (23013F4-01) E100.
1-29. ADD I.C. (23014F4-01) E102.
1-30. REMOVE RESISTOR R7-1300316 AND REPLACE WITH 1300365.
1-31. " " R24-1302379 " 1312929.
1-32. " " R25- " 1312929.
1-33. " " R33- " 1312929.
1-34. " " R14- " 1302377.
1-35. " " R17- " .
1-36. " " R27- " .
1-37. " " R29- " .
1-38. " " R30- " .
1-39. " " R31- " .
1-40. " RESISTOR R32-1302379 " 1302377.
1-41. " I.C. Y1-1811660-24 " 1811660-16.
1-42. " " E35-1912847 " 1910548.
1-43. " " E68- " .
1-44. " " E69- " .
1-45. " " E70- " .
1-46. " I.C. E71-1912847 " 1910548.
1-47. REMOVE CAPACITOR C43-1012784 AND REPLACE WITH 1013466-11. MOUNT IN PTH ABOVE E52-12 & PTH BELOW E53-5 AS SHOWN.
1-48. REMOVE RESISTOR R21-1300479 AND REPLACE WITH 1300417. MOUNT IN PTH BELOW E77-2 & PTH ABOVE E87-9 AS SHOWN.

WIRE ADDS-COMPONENT SIDE AS SHOWN:
2-1. FROM PTH ABOVE Y1-8 TO PTH ABOVE Y1-9.

ECO M7161-CX001

COMPONENT DELETES (SIDE 1)
1-1. DELETE E11, R NETWORK 8-1.39K, 5%, 10 PIN (1312114-00).

WIRE ADDS (SIDE 1) 30 AWG
1-4. FROM E86-1 TO E68-2.
1-5. FROM E86-3 TO E66-13.
1-6. FROM E86-2 TO PTH BELOW & TO LEFT OF E86-1.
(IF REWORK STEP 0 6 HAS BEEN DONE).

COMPONENT ADDS (SIDE 1)
1-7. ADD E11, R NETWORK, 9-1K, 2%, 10 PIN (1316395 02).

D-UA-M7161-0-0

REVISION HISTORY		
DATE	ECO NUMBER	REV.

DRD 130A

TITLE: UDA # 1

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV.
D	UA	M7161-0-0	C
SCALE		SHEET 3 OF 4	

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ECO M7161-CX004

COMPONENT DELETES

4-1.	DELETE	CAPACITOR	C94 (1012784-00).
4-2.		"	C95 (1012784-00).
4-3.		CAPACITOR	C43 (1013466-11).
4-4.		RESISTOR	R7 (1300365-00).
4-5.		RESISTOR	R21 (1300417-00).
4-6.		OSILLATOR	Y1 (1811660-16) SAVE PART.
4-7.		I.C. SOCKET	XY1 (1215006-01).
4-8.		CROM	E17 (23043F4-00).
4-9.		"	E16 (23044F4-00).
4-10.		"	E15 (23045F4-00).
4-11.		"	E14 (23046F4-00).
4-12.		"	E13 (23047F4-00).
4-13.		"	E12 (23048F4-00).
4-14.		"	E6 (23049F4-00).
4-15.		"	E5 (23050F4-00).
4-16.		"	E4 (23051F4-00).
4-17.		"	E3 (23052F4-00).
4-18.		"	E2 (23053F4-00).
4-19.	DELETE	CROM	E1 (23054F4-00).

COMPONENT ADDS

4-22.	ADD	COUNTER	E127 (1914451-00).
4-23.		COUNTER	E128 (1914451-00).
4-24.		74LS164	E124 (1912850-00).
4-25.		POST	TP21 (9009149-01).
4-26.		"	TP22 "
4-27.		"	TP23 "
4-28.		POST	TP24 (9009149-01).
4-29.		CLIP	W14 (1215899-00).
4-30.		OSCILLATOR	Y1 (1811660-16).
4-31.		CROM	E17 (23064F4-00).
4-32.		"	E16 (23065F4-00).
4-33.		"	E15 (23066F4-00).
4-34.		"	E14 (23067F4-00).
4-35.		"	E13 (23068F4-00).
4-36.		"	E12 (23069F4-00).
4-37.		"	E6 (23070F4-00).
4-38.		"	E5 (23071F4-00).
4-39.		"	E4 (23072F4-00).
4-40.		"	E3 (23073F4-00).
4-41.		"	E2 (23074F4-00).
4-42.	ADD	CROM	E1 (23075F4-00).

WIRE ADDS SIDE 1-30AWG-AS SHOWN

4-43.	ADD WIRE FROM	E124-1	TO E124-2.
4-44.		E124-1	E124-9.
4-45.		E124-9	E116-15.
4-46.		E116-15	TP21.
4-47.		E124-13	TP24.
4-48.		E85-3	TP23.
4-49.		E124-10	TP22.
4-50.		E124-8	E128-5.
4-51.		E128-2	E128-7.
4-52.		E128-7	PTH RIGHT OF E128-7.
4-53.		E128-12	PTH RIGHT OF E128-7.
4-54.		E128-6	E128-13.
4-55.		E128-1	E91-10.
4-56.		E127-8	E87-9.
4-57.		E127-1	E128-8.
4-58.		E127-7	PTH RIGHT OF E127-7.
4-59.		E127-7	E127-2.
4-60.		E127-6	E127-13.
4-61.		E127-12	PTH RIGHT OF E127-7.
4-62.	ADD WIRE FROM	E75-5	TO C58.

AFTER COMPLETING ABOVE REWORK STEPS MARK THE MODULE AS REV C.

REVISION HISTORY		
DATE	ECO NUMBER	REV.

TITLE: UDA#1

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV.
D	UA	M7161-0-0	C

SCALE: N/A SHEET 1 OF 2

AUTOMATED BY PRTLST.3P(44) P A R T S L I S T SHEET A1 OF A3

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	YA	REFERENCE DESIGNATOR
1	1	D-MD-5014040-0-0	5014040-00	UDA NO. 1	1	1	
2	2		1012784-00	.047 MFD 50V +80-20% CER	90	90	C10-C42,C44-C69,C71-C93,C96-C103
3	3		1013466-08	680.0 MMF 50V 10% X7R CER	1	1	C9
4	4		1013466-11	*** THIS ITEM IS NOT USED ***	-	-	
5	5		1016549-00	47 MFD 10V +50-10% AL EL	8	8	C1,C2,C3,C4,C5,C6,C7,C8
6	6		1112689-00	LED .8MCD@16MA VF=5V	4	4	D1,D2,D3,D4
7	7		1209838-00	SKT,IC 16PIN DIP GOLD	1	1	XE74
8	8		1210385-01	PIN 1POS WIRE WRAP	6	6	TP1,TP2,TP3,TP4,TP5,TP6
9	9		1211164-06	SW,DIP 10POS/1PST 5VDC100MA F	1	1	E96
10	10		1212965-04	PCB,HEADER 20PIN(2X05).100CC 90D	1	1	P3
11	11		1214314-00	CONN,P+S 02SKT(1X02).100CC JUM	2	2	W2,W4
12	12		1214993-00	PCB,HEADER 40POS(2X20).100CC 90D	1	1	P2
13	13		1215006-01	*** THIS ITEM IS NOT USED ***	-	-	
14	14		1215006-06	*** THIS ITEM IS NOT USED ***	-	-	
15	15		1216832-02	PCB,HEADER 40POS(2X20).100CC 90D	1	1	P6
16	16		1216832-03	PCB,HEADER 50POS(2X25).100CC 90D	1	1	P5
17	17		1216988-02	HANDLE,MODULE,HEX TWO EJECTORS	1	1	
18	18		1300229-00	100.0 .25 W 5.0 % CC	7	7	R4,R5,R6,R22,R34,R2,R12
19	19		1300316-00	470.0 .25 W 5.0 % CC	4	4	R8,R9,R13,R20
20	20		1300365-00	1.0 K .25 W 5.0 % CC	3	3	R1,R10,R19
21	21		1300417-00	*** THIS ITEM IS NOT USED ***	-	-	
22	22		1301972-00	270.0 .25 W 5.0 % CC	2	2	R3,R11
23	23		1302377-00	39.0 .25 W 5.0 % CC	7	7	R14,R17,R27,R29,R30,R31,R32
24	24		1302379-00	75.0 .25 W 5.0 % CC	6	6	R15,R16,R18,R23,R26,R28
25	25		1305125-00	383.0 .25 W 1.0 % RN55D-F10	2	2	R36,R40
26	26		1311422-00	178.0 .25 W 1.0 % RN55D-F10	4	4	R35,R37,R38,R39
27	27		1316395-02	R NETWORK 9-1.0K 2.0 % 10PIN	1	1	E11
28	28		1312929-00	62.0 .25 W 5.0 % CC	3	3	R24,R25,R33
29	29		1316395-00	R NETWORK 9-4.7K 2.0 % 10PIN	1	1	E42
30	30		1617533-00	DELAY= 250NS,5TAPS 14PIN DIP	1	1	E108

REVISION HISTORY			BASIC PART NO: M7161										
ENG	ECO NUMBER	REV	SECTION A OF A	DRN: R. MICHAUD	DATE: 11-NOV-80		D	I	G	I	T	A	L
	INITIAL	A	SECTION.VARIATION INDEX	CHK'D: C. RIDGEWAY	DATE: 11-NOV-80	TITLE PARTS LIST							
CR	M7161-CX001	B	[A] 00,YA			UDA #1							
CR	M7161-CX002	C	[B]										
CR	M7161-CX002	C	[C]	DES.ENG: C. RIDGEWAY	DATE: 11-NOV-80								
CR	M7161-CX002	C	[D]			DOCUMENT NUMBER							
CR	M7161-CX002	C	[E]										
CR	M7161-CX004	D	[F]	RESP.ENG.: B. MATHRANI	DATE: 11-NOV-80	SIZE	CODE	NUMBER		REV			
			[H]										
			[J]										
			[K]	MFG.ENG.: D. SWIFT	DATE: 11-NOV-80	K	PL	M7161-0-DBP		D			
			[L]										
			[M]	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:				EDIT #			
			[N]	D-UA-M7161-0-0	# B-DD-M7161-0	Z1748D.PLS				16			

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AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	YA	REFERENCE DESIGNATOR
31	31		1618344-00	DELAY= 58NS,5TAPS	1	1	E91
32	32		1811660-16	OSCILLATOR, XTAL 17.280 MHZ	1	1	Y1
33	33		1907705-00	DEC 8881 NAND GATE-QUAD 2IN O	1	1	E84
34	34		1910532-00	74S00 NAND GATE-QUAD 2IN	2	2	E33,E47
35	35		1910534-00	74S04 INVERTER GATE-HEX 1I	2	2	E80,E92
36	36		1910536-00	74S10 NAND GATE-TRIPLE 3IN	1	1	E90
37	37		1910537-00	74S11 AND GATE-TRIPLE 3INP	1	1	E46
38	38		1910542-00	74S64 A-O-I GATE 4-2-3-2	2	2	E44,E89
39	39		1910544-00	74S74 FF-D DUAL,EDGE TRIGG	1	1	E51
40	40		1910545-00	74S112 FF-JK DUAL,EDGE TRIG	1	1	E120
41	41		1910546-00	74S140 NAND GATE-DUAL 4INPU	1	1	E50
42	42		1910548-00	74S157 MUX 1 OF 2 (QUAD)	5	5	E35,E68,E69,E70,E71
43	43		1910550-00	74S174 FF-D HEX	6	6	E7,E8,E21,E22,E24,E25
44	44		1910552-00	74S194 SHIFT REG.,4BIT RIGH	2	2	E54,E62
45	45		1910950-00	74S74 FF-D DUAL (-45 VERSI	1	1	E40
46	46		1911116-00	DEC 8837 RECEIVER,BUS,HEX,UN	1	1	E64
47	47		1911579-00	8641 TRANSCEIVER,BUS,QUA	1	1	E83
48	48		1911675-00	74S138 DECODER/DEMUX 3-8 LIN	3	3	E73,E82,E93
49	49		1911676-00	74S139 DECODER-DUAL TWO-INP	2	2	E43,E81
50	50		1911712-00	74S51 AND-OR GATE-INVERT D	1	1	E49
51	51		1911983-00	74S133 NAND GATE-POSITIVE 1	1	1	E28
52	52		1912097-00	SN 74S182 LOOK AHD CARRY GEN	1	1	E45
53	53		1912388-00	74S02 NOR GATE-QUAD 2IN,PO	2	2	E67,E126
54	54		1912389-00	74S08 AND GATE-QUAD 2IN,PO	2	2	E48,E36
55	55		1912728-00	74S251 MUX 1 OF 8 TRI-STA	4	4	E72,E77,E78,E79
56	56		1912799-00	LS00 NAND-GATE-QUAD 2IN,P	1	1	E98
57	57		1912803-00	LS04 INVERTER GATE,HEX	2	2	E85,E109
58	58		1912808-00	LS11 AND GATE-TRIPLE 3IN	1	1	E65
59	59		1912820-00	LS51 A-O-I GATE 2-WIDE 2I	1	1	E99
60	60		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	1	1	E125
61	61		1912842-00	LS138 DECODER-THREE INPUT,	1	1	E75
62	62		1912860-00	LS259 LATCH 8BIT	1	1	E66
63	63		1912863-00	LS273 FF-D OCTAL W/CLEAR	3	3	E20,E41,E104
64	64		1912864-00	LS279 LATCH,QUAD-S-R	1	1	E76
65	65		1913040-00	DC 005 TRANSCEIVER 4BIT	4	4	E94,E95,E106,E107
66	66		1913245-02	2901A-1 MICROPRESCESSOR 4-	4	4	E55,E56,E57,E58
67	67		1913414-00	LS14 INVERTER GATE-HEX SC	1	1	E87
68	68		1913939-00	LS191 COUNTER,SYNCHR. UP/D	2	2	E112,E122
69	69		1914214-00	LS374 FF-D OCTAL EDGE TRIG	6	6	E23,E26,E27,E113,E114,E123
70	70		1914438-00	DC 013 UNIBUS INTERRRUPT-BIP	2	2	E116,E117
71	71		1914451-00	74LS393 COUNTER,BINARY,4BIT	3	3	E111,E127,E128
72	72		1915193-00	LS244 DRIVER,LINE,OCTAL,T	2	2	E59,E63
73	73		1915218-00	LS245 TRANSCEIVER,BUS,OCT	2	2	E105,E115
74	74		1915305-00	AM 2908 TRANSCEIVER,BUS,LATCH	4	4	E52,E53,E60,E61
75	75		1916680-01	2911A MICROPROGRAM SEQUENC	6	6	E9,E10,E18,E19,E29,E30
76	76		1917956-00	74LS280N PARITY GEN/CHK,9BIT	6	6	E31,E32,E34,E36,E37,E38
77	77		23301E2-00	E2-06	1	1	E100
78	78		23302E2-00	E2-06	1	1	E102

D	I	G	I	T	A	L	TITLE	SIZE	CODE	DOCUMENT NUMBER	REV
							UDA #1	K	PL	M7161-0-DBP	D
							SECTION A OF A				

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	QTY PER VARIATION YA	REFERENCE DESIGNATOR
79	79		4901259-00	ADHESIVE,ETHYL CYANOACRYLATE,KIT	A/R	A/R	
80	80		5408778-00	REPLACED BY 13-18784-01	1	1	E74
81	81		9000024-01	EYELET,ROLLED 0.1210DX0.192	11	11	
82	82		9009157-00	ADH,LIQ.RM.TEMP CURING COLORLESS	A/R	A/R	
83	83		9105740-55	WIRE(WRAP) 30AWG KYNAR UL14	A/R	A/R	
84	84		23064F4-00	F4-01	-	1	E17
85	85		23065F4-00	F4-01	-	1	E16
86	86		23066F4-00	F4-01	-	1	E15
87	87		23067F4-00	F4-01	-	1	E14
88	88		23068F4-00	F4-01	-	1	E13
89	89		23069F4-00	F4-01	-	1	E12
90	90		23070F4-00	F4-01	-	1	E6
91	91		23071F4-00	F4-01	-	1	E5
92	92		23072F4-00	F4-01	-	1	E4
93	93		23073F4-00	F4-01	-	1	E3
94	94		23074F4-00	F4-01	-	1	E2
95	95		23075F4-00	F4-01	-	1	E1
96	96		1912850-00	LS164 SHIFT REG. 8BIT SERI	1	1	E124
97	97		1215899-00	JUMPER 02POS CLIP TIN .02 -.	1	1	W14
98	98		9009149-01	PIN,STAKING 0.235 HX0.345LG SQUA	4	4	TP21-TP24

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							UDA #1	

SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7161-0-DBP	D

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W, 5%.
2. GATES MARKED WITH A STAR (*) MAY BE 'S' OR 'LS'.
3. 2901 RAM REGISTERS CONFIGURED FOR A 16 BIT ROTATE WHILE THE 'Q' REGISTER IS A 16 BIT SHIFT.
4. LITERAL BITS 0-7 CORRESPONDS TO BUS SRC 0-3, IOC SEL 0-3 AND SET IOC.

+5.0V
R9 470Ω
R8 470Ω
R13 470Ω

DEADBAND L
ALU TO BUS H
74S00 E33
2901 TO BUS L
F=ZERO H

DBUS 12 H
DBUS 13 H
DBUS 14 H
DBUS 15 H
DBUS 08 H
DBUS 09 H
DBUS 10 H
DBUS 11 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H

2901 FOUR BIT SLICE
E55 (Y0 Y1 Y2 Y3)
E56 (Y0 Y1 Y2 Y3)
E57 (Y0 Y1 Y2 Y3)
E58 (Y0 Y1 Y2 Y3)

OUT EN
GEN
PROP
F3
OVERFLOW
F=0
ALU MSB H
Q3 SHIFT 0
RAM3 RAM0
IN CARRY OUT
C16 H
Q7 H
RAM 7 H
RAM 15 H
C8 IN H
C4 IN H
C12 IN H
CARRY IN H

ALU DEST 2 H
ALU DEST 1 H
ALU DEST 0 H
I8
I7 DESTINATION
I6

ALU FUNC 2 H
ALU FUNC 1 H
ALU FUNC 0 H
I5
I4
I3
ALU FUNCTION

ALU SOURCE 2 H
ALU SOURCE 1 H
ALU SOURCE 0 H
I2
I1
I0
SOURCE

A REG 0 H
A REG 1 H
A REG 2 H
A REG 3 H
A0
A1
A2
A3
'A' ADDRESS READ

B REG 0 H
B REG 1 H
B REG 2 H
B REG 3 H
B0
B1
B2
B3
'B' ADDRESS READ/WRITE

PROCCLK L
CLOCK
D0 D1 D2 D3

2901:
+5V = 10
GND = 30

CARRY SKIPPER 74S182 E45
G OUT
P OUT
G0
P0
C4 OUT
G1
P1
C2 OUT
G2
P2
C1 OUT
C IN
RVCC1
G2 L
P2 L
C12 IN H
C8 IN H
C4 IN H

4X2 MUX 74S157 E68
4X2 MUX 74S157 E69
4X2 MUX 74S157 E70
4X2 MUX 74S157 E71
YA
YB
YC
YD
0-DA
1-DA
0-DB
1-DB
0-DC
1-DC
0-DD
1-DD
1 SEL
EN

SET IOC H
DBUS 15 H
IOC SEL 2 H
DBUS 14 H
IOC SEL 1 H
DBUS 13 H
IOC SEL 0 H
DBUS 12 H
SEL LITERAL L
ENA HI LTRL L
BUS SRC 3 H
DBUS 11 H
BUS SRC 2 H
DBUS 10 H
BUS SRC 1 H
DBUS 09 H
BUS SRC 0 H
DBUS 08 H
SET IOC H
DBUS 07 H
IOC SEL 2 H
DBUS 06 H
IOC SEL 1 H
DBUS 05 H
IOC SEL 0 H
DBUS 04 H
SEL LITERAL L
ENA LO LTRL L
BUS SRC 3 H
DBUS 03 H
BUS SRC 2 H
DBUS 02 H
BUS SRC 1 H
DBUS 01 H
BUS SRC 0 H
DBUS 00 H

74S64 E44
ENA HI LTRL L
74S02 S67
ENA LO LTRL L
ALU FUNC 2 H
ALU FUNC 1 H
ALU FUNC 0 H
RVCC1
CARRY IN H
SEL LITERAL L

ALU

UDA1 BASE LEVEL 3-DEC ETCH LEVEL B

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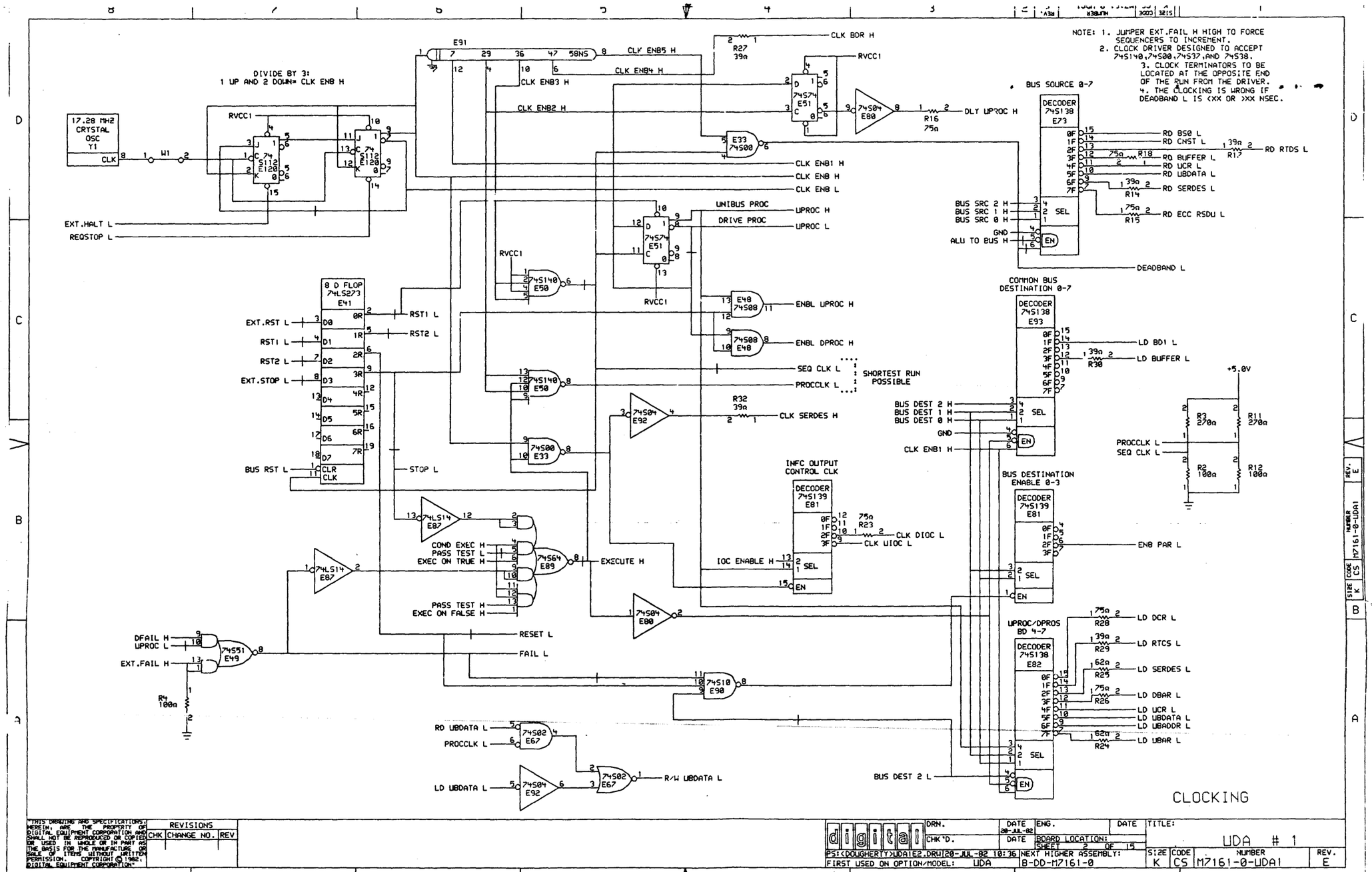
REVISIONS
CHK CHANGE NO. REV
S.L. 21 JAN 82 E
L.P.SOSKIN 22 JAN 82 F

DRW D. Pauritsky 20-JUL-82
CHK R. Wiebrand 7-21-82
ENG. C. Rose
BOARD LOCATION:
SHEET 1 OF 15
DATE
TITLE: UDA # 1
PS:<DOUGHERTY.UDA1.DRW|28-JUL-82 10:31| NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA B-DD-M7161-0
SIZE K | CODE CS | NUMBER M7161-0-UDA1 | REV. F



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REVISIONS		
CHK	CHANGE NO.	REV

digital

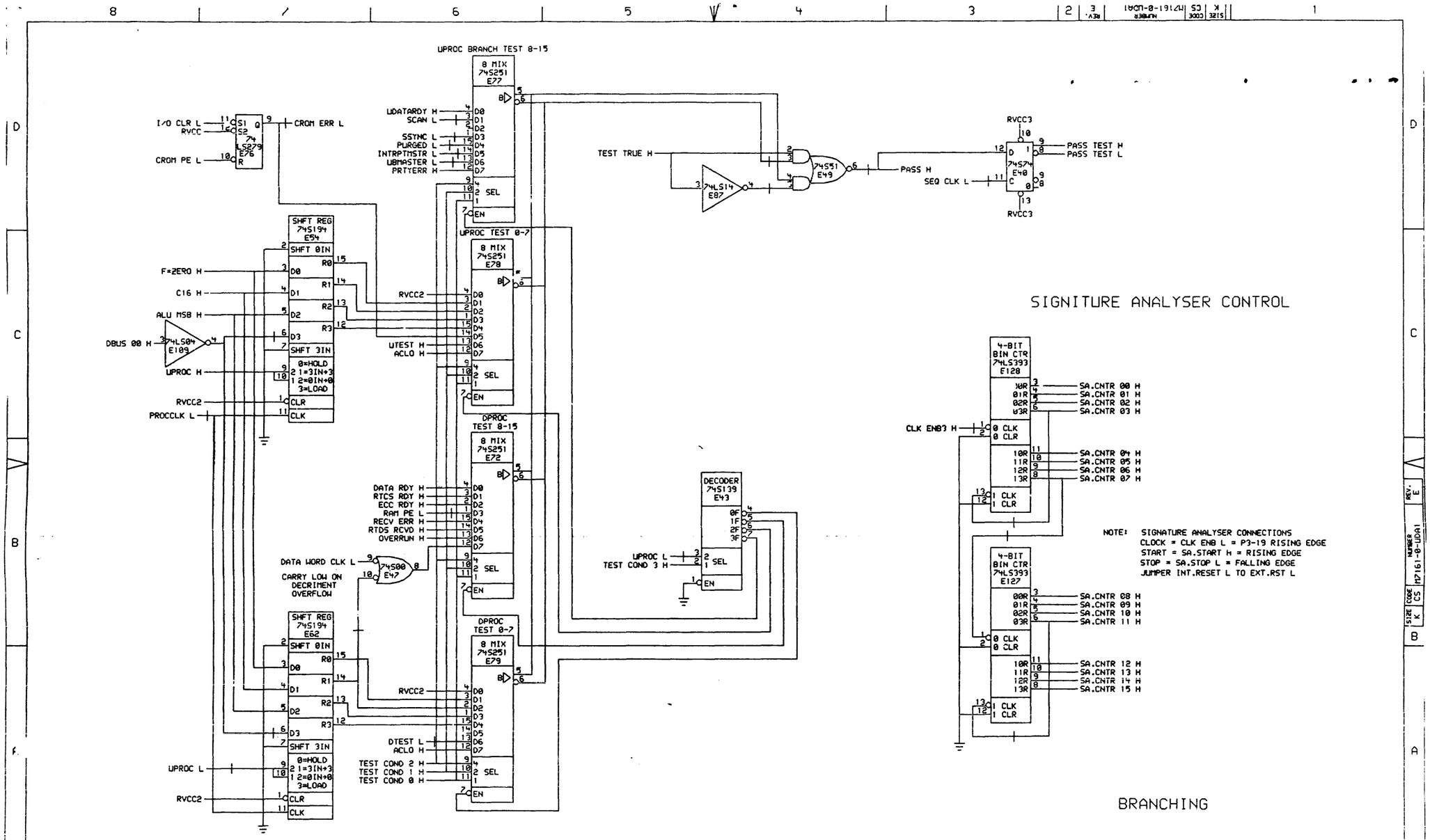
DRN. | DATE | ENG. | DATE | TITLE: UDA # 1

CHK'D. | DATE 28-JUL-82 | BOARD LOCATION: | SHEET 2 OF 15

PS:<DOUGHERTY>UDA1E2.DRW 28-JUL-82 10:36 | NEXT HIGHER ASSEMBLY: B-DD-M7161-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E



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REVISIONS		
CHK	CHANGE NO.	REV

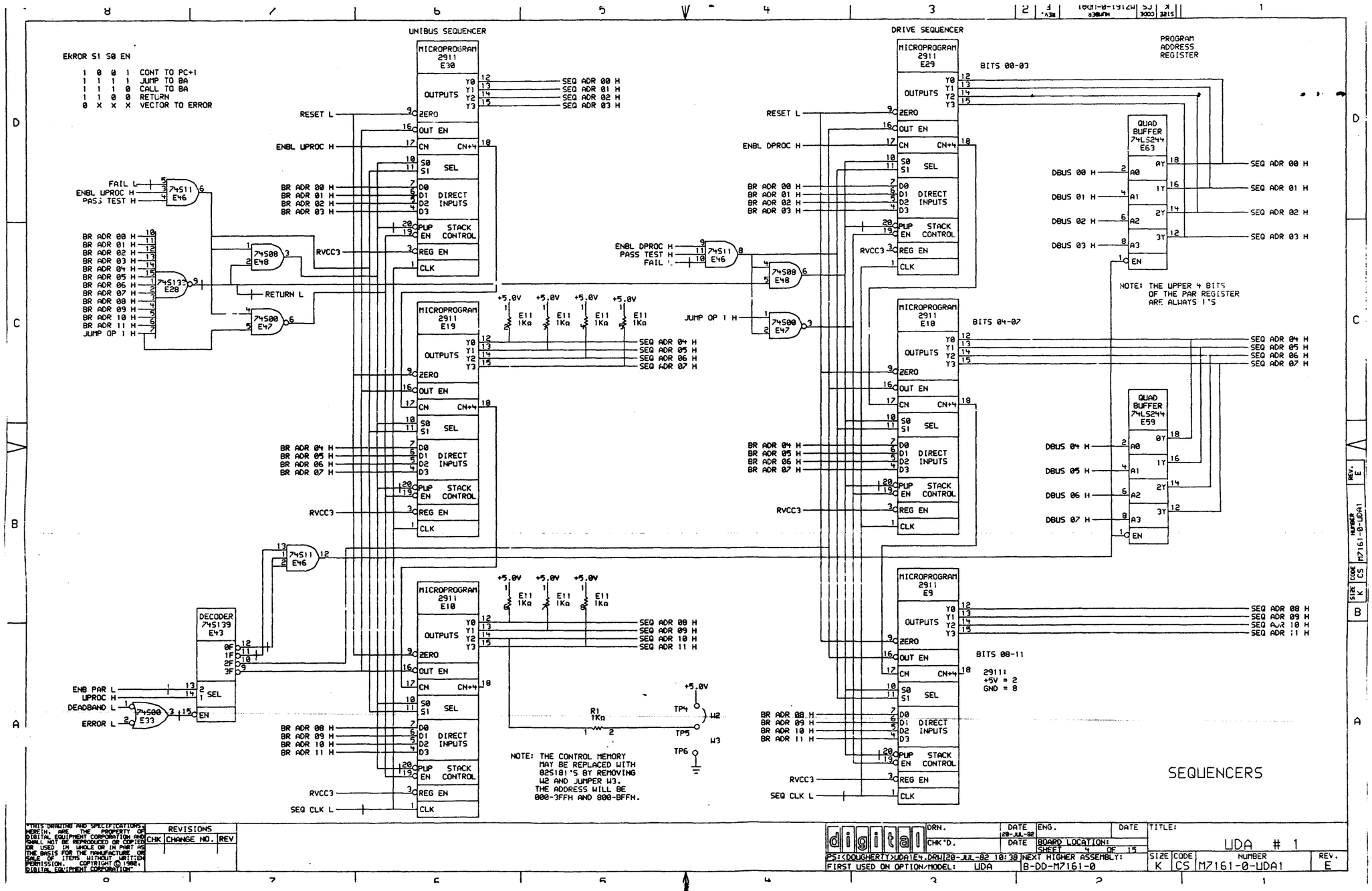
digital

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE:
CHK'D.	DATE	BOARD LOCATION: SHEET 3 OF 15		UDA # 1

PS:<DOUGHERTY>UDA1E3.DRW 19-JUL-82 15:28 NEXT HIGHER ASSEMBLY: B-DD-M7161-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. | DATE 20-JUL-82 | ENG. | DATE | TITLE: UDA # 1

CHK'D. | DATE | BOARD LOCATION: SHEET 4 OF 15

PS:<DOUGHERTY>UDA1E4.DRW|20-JUL-82 10:38 | NEXT HIGHER ASSEMBLY: B-DD-M7161-0

FIRST USED ON OPTION/MODEL: UDA

SIZE K | CODE CS | NUMBER M7161-0-UDA1 | REV. E

CROM PARITY CHECKING

BITS 00-08 — PARITY GEN 74LS280 E38
BR ADR 00 H
BR ADR 01 H
BR ADR 02 H
BR ADR 03 H
BR ADR 04 H
BR ADR 05 H
BR ADR 06 H
BR ADR 07 H
BR ADR 08 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD

BITS 09-17 — PARITY GEN 74LS280 E37
BR ADR 09 H
BR ADR 10 H
BR ADR 11 H
CROM PRTY H
JUMP OP 1 H
COND EXEC H
SENSE H
BUS SRC 0 H
BUS SRC 1 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD

BITS 18-26 — PARITY GEN 74LS280 E36
BUS SRC 2 H
BUS SRC 3 H
IOC SEL 0 H
IOC SEL 1 H
IOC SEL 2 H
SET IOC H
IOC ENABLE H
BUS DEST 0 H
BUS DEST 1 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD

BITS 27-35 — PARITY GEN 74LS280 E34
BUS DEST 2 H
PR 28 H
PR 29 H
PR 30 H
PR 31 H
B REG 0 H
B REG 1 H
B REG 2 H
B REG 3 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD

BITS 36-44 — PARITY GEN 74LS280 E32
EXEC ON TRUE H
ALU TO BUS H
ALU SOURCE 0 H
ALU SOURCE 1 H
ALU SOURCE 2 H
ALU FUNC 0 H
ALU FUNC 1 H
ALU FUNC 2 H
ALU DEST 0 H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD

BITS 45-47 — PARITY GEN 74LS280 E31
ALU DEST 1 H
ALU DEST 2 H
CARRY IN H
D0 D1 D2 D3 D4 D5 D6 D7 D8 → FEVEN, FODD → ODD PARITY → CROM PE1 L

QUAD BUFFER 74LS244 E63
RAM PE1 L
TIMEOUT L
CROM PE L
UPROC H
FAIL L
RESET L
1A0 1A1 1A2 1A3 1EN → 1Y SEQ ADR 00 H, 2Y SEQ ADR 01 H, 3Y SEQ ADR 02 H, 4Y SEQ ADR 03 H

74S10 E90 → 74S10 E90 → ERROR L

U TIMEOUT H
UPROC L
UPROC H
D TIMEOUT H
74LS51 E99 → TIME ERR L

EXT.HALT L
74LS00 E98 → 100Ω R34 → 60HZ H

4-BIT BIN CTR 74LS393 E111
00R 01R 02R 03R → U TIMEOUT H
0 CLK 0 CLR
10R 11R 12R 13R → D TIMEOUT H
1 CLK 1 CLR

UPROC L
CLK ENB H
PASS TEST L
74LS51 E99 → 74LS00 E98 → 74S04 E92 → 39Ω R31 → D FAILTEST H

STOP L
ERROR L
74LS00 E98 → RST TIMER H

PIPELINE ADDRESS REGISTER 00-05
6 D FF 74S174 E8
SEQ ADR 00 H
SEQ ADR 01 H
SEQ ADR 02 H
SEQ ADR 03 H
SEQ ADR 04 H
SEQ ADR 05 H
RVCC2
SEQ CLK L
D0 D1 D2 D3 D4 D5 CLR CLK
R0 R1 R2 R3 R4 R5 → PADR 0 H, PADR 1 H, PADR 2 H, PADR 3 H, PADR 4 H, PADR 5 H

PIPELINE ADDRESS REGISTER 06-11
6 D FF 74S174 E7
SEQ ADR 06 H
SEQ ADR 07 H
SEQ ADR 08 H
SEQ ADR 09 H
SEQ ADR 10 H
SEQ ADR 11 H
RVCC2
D0 D1 D2 D3 D4 D5 CLR CLK
R0 R1 R2 R3 R4 R5 → PADR 6 H, PADR 7 H, PADR 8 H, PADR 9 H, PADR 10 H, PADR 11 H

PIPELINE REGISTER BITS 36,44-46
8 D FLOP 74LS273 E20
RAM PE L
TIME ERR L
CROM PE2 L
CROM PE1 L
CROM 36 H
CROM 44 H
CROM 45 H
CROM 46 H
RVCC2
D0 D1 D2 D3 D4 D5 D6 D7 CLR CLK
0R 1R 2R 3R 4R 5R 6R 7R → RAM PE1 L, TIMEOUT L, CROM PE L, CROM PE2 L, EXEC ON TRUE H, ALU DEST 0 H, ALU DEST 1 H, ALU DEST 2 H
+5.0V → E42 4.7kΩ
74S04 E92 → EXEC ON FALSE H

ADDRESS 000-7FFH CROM 00-07
2K X 8 PROM 82S191 E17
PADR 0 H … PADR 10 H → ADR
PADR 11 H → EN
+5.0V → E42 4.7kΩ, E11 1kΩ
REQSTOP L
PROMENBL H
SEQ CLK L

PIPELINE REGISTER BITS 00-07
8 D FF 74LS374 E27
D0 D1 D2 D3 D4 D5 D6 D7 EN OUT CLK
0R 1R 2R 3R 4R 5R 6R 7R → BR ADR 00 H, BR ADR 01 H, BR ADR 02 H, BR ADR 03 H, BR ADR 04 H, BR ADR 05 H, BR ADR 06 H, BR ADR 07 H

ADDRESS 800-FFFH CROM 00-07
2K X 8 PROM 82S191 E6
PADR 0 H … PADR 10 H → ADR
PADR 11 H → EN
PROMENBL H

NOTE: AN ERROR WILL ALLOW THE INSTRUCTION WITH THE ERROR TO COMPLETE, THE NEXT ONE, THEN VECTOR TO THE ERROR ROUTINE.

CONTROL READ ONLY MEMORY BITS 00,07 PARITY AND PAR,PR 00-07,36,44-46

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REVISIONS		
CHK	CHANGE NO.	REV

digital

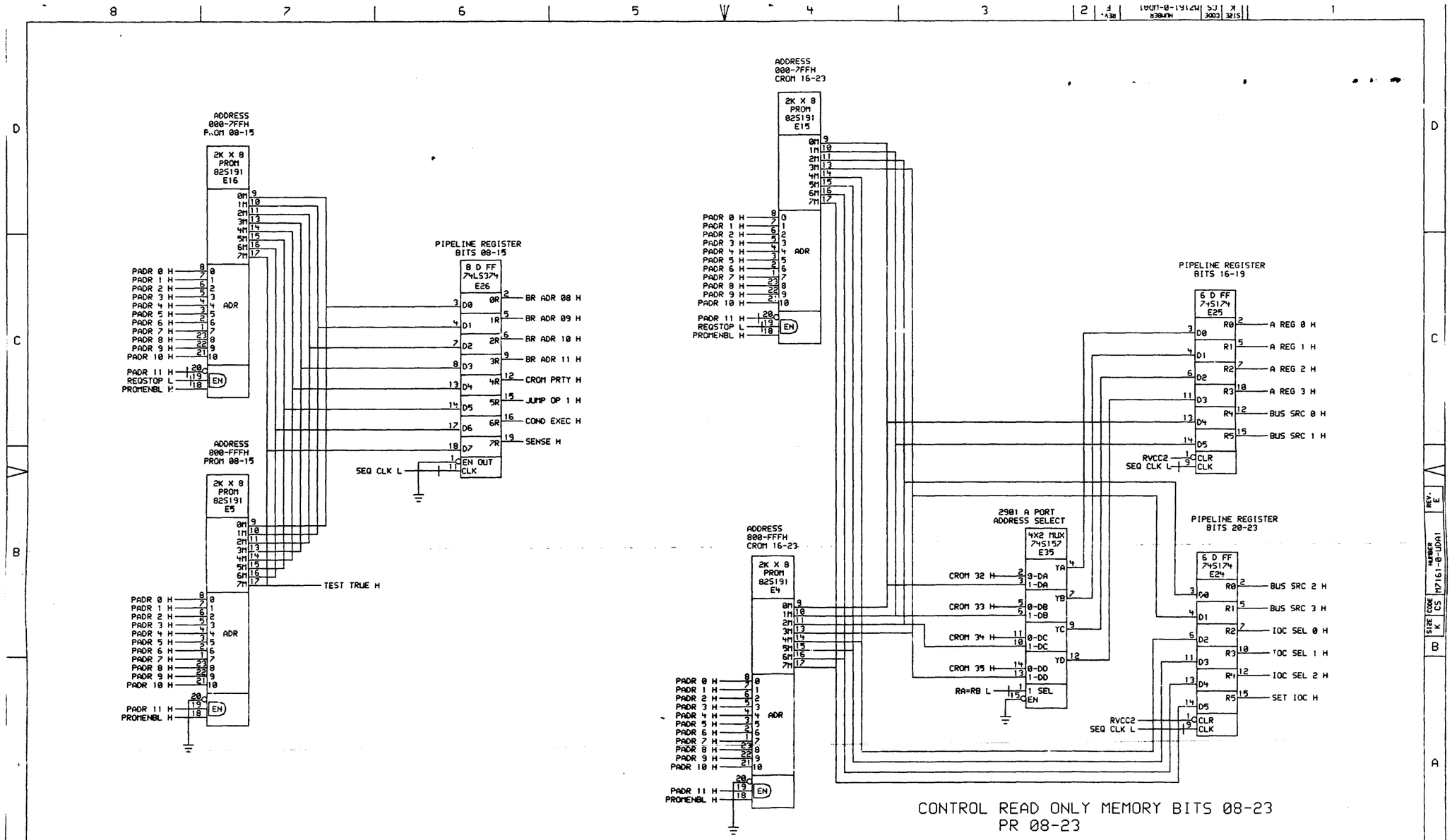
DRN.	DATE	ENG.	DATE	TITLE:
CHK'D.	20-JUL-82			UDA # 1

DATE | BOARD LOCATION: | SHEET 5 OF 15

P5:<DOLGHERTY>UDA1E5.DRW 20-JUL-82 10:49 | NEXT HIGHER ASSEMBLY: | A-DD-M7161-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E



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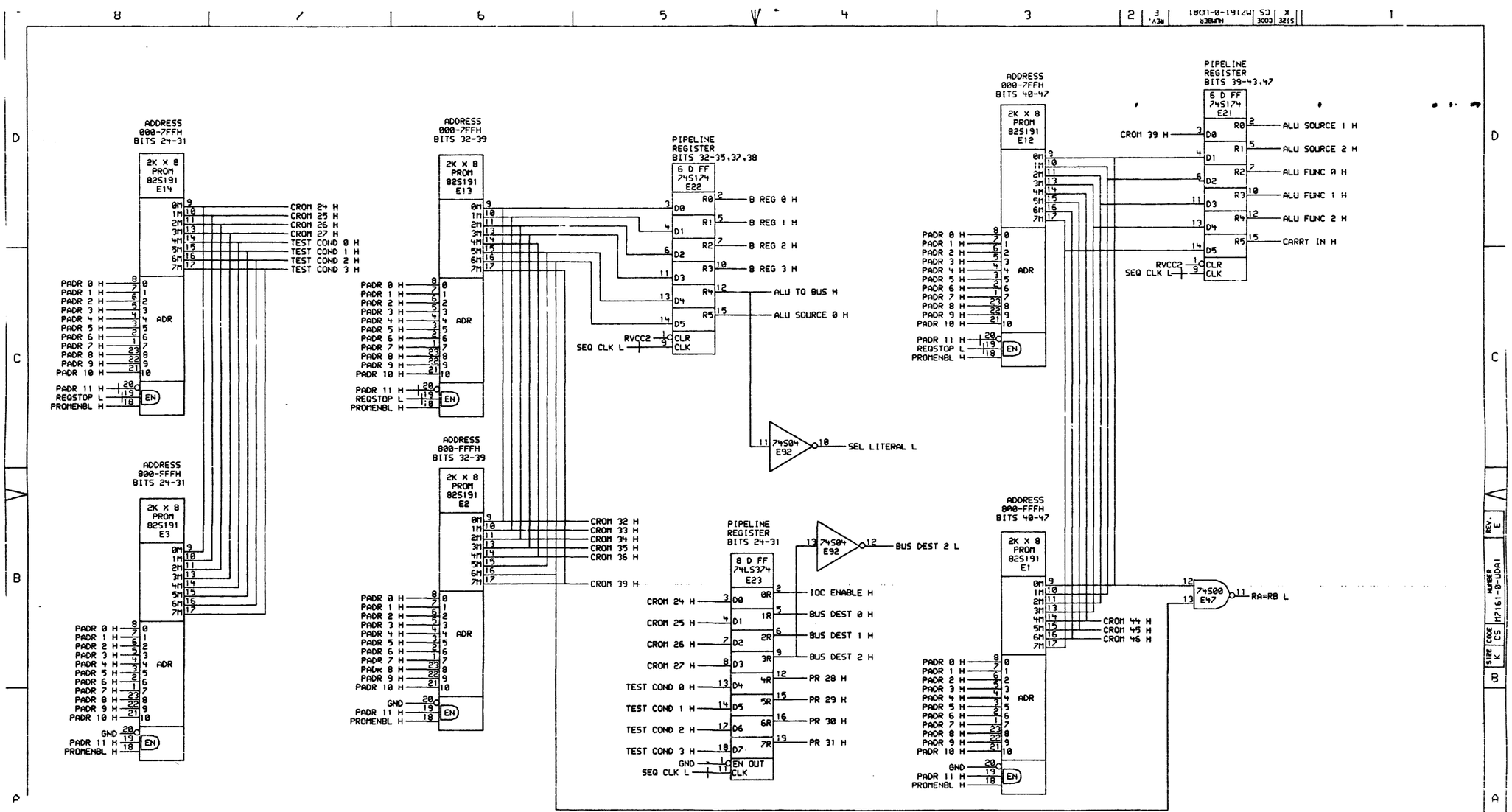
REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN.	DATE	ENG.	DATE	TITLE:
	CHK D.	28-JUL-82			LIDA # 1
PS:<DOUGHERTY>LIDA1E6.DRW 19-JUL-82 16:44		DATE	BOARD LOCATION:		
FIRST USED ON OPTION/MODEL: LIDA			SHEET 6 OF 15	NEXT HIGHER ASSEMBLY: B-DD-M7161-0	

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-LIDA1	E



CONTROL READ ONLY MEMORY BITS 24-47
PR 32-35,37-43,47

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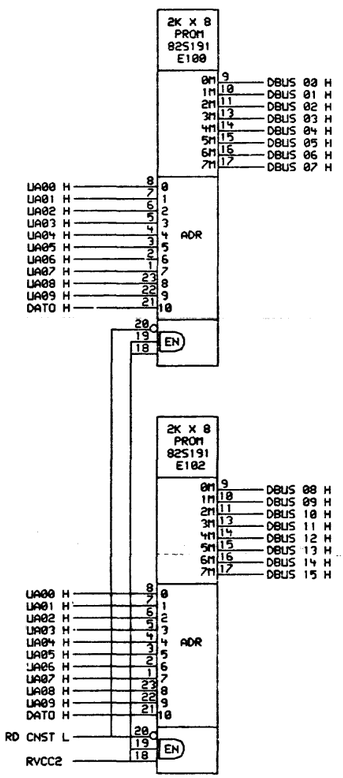
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE: UDA # 1
CHK'D.	DATE	BOARD LOCATION: SHEET 2 OF 15		
PS:<DOUGHERTY>UDA1E7.DRW 19-JUL-82 16:52		NEXT HIGHER ASSEMBLY: B-DD-M7161-0		
FIRST USED ON OPTION/MODEL: UDA				

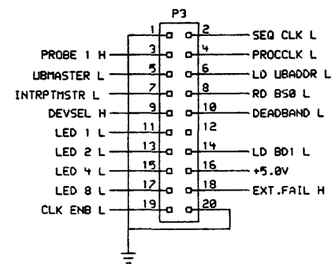
SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E

LOG/ANTILOG
CONSTANT PROM
2K X 12 BITS

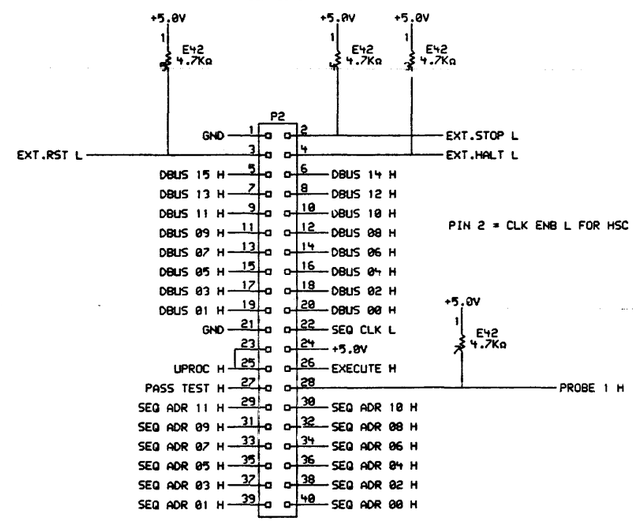


NOTE: BITS 12-15 OF THE PROM MUST BE ZERO FOR SOFTWARE EFFICIENCY.

TEST
CONNECTOR



LOGIC ANALYSER
CONNECTOR



PIN 2 = CLK ENB L FOR HSC

LOG/ALG PROM AND CONNECTORS

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE:
CHK'D.	DATE	BOARD LOCATION: SHEET 8 OF 15		LDA # 1

PS:<DOUGHERTY>LDA1E8.DRW 20-JUL-82 13:41 | NEXT HIGHER ASSEMBLY: | SIZE K | CODE CS | NUMBER M7161-0-LDA1 | REV. E

FIRST USED ON OPTION/MODEL: LDA | B-DD-M7161-0

NOTE: UNIBUS INTERFACE 5-14 PIN, 12-16 PIN, 10-30PIN.

UNIBUS/CONSTANT ADDRESS REGISTER

8 D FF 74LS374 E114

DBUS 00 H → D0 → 0R → UA00 H
DBUS 01 H → D1 → 1R → UA01 H
DBUS 02 H → D2 → 2R → UA02 H
DBUS 03 H → D3 → 3R → UA03 H
DBUS 04 H → D4 → 4R → UA04 H
DBUS 05 H → D5 → 5R → UA05 H
DBUS 06 H → D6 → 6R → UA06 H
DBUS 07 H → D7 → 7R → UA07 H
GND → EN OUT
CLK

UP/DOWN COUNTER 74LS191 E122

DBUS 08 H → D0 → R0 → UA08 H
DBUS 09 H → D1 → R1 → UA09 H
DBUS 10 H → D2 → R2 → UA10 H
DBUS 11 H → D3 → R3 → UA11 H
MAX/MIN
RIP CLK
CLK
UP/DRN
GND
EN
LOAD

UP/DOWN COUNTER 74LS191 E112

DBUS 04 H → D0 → R0 → UA04 H
DBUS 03 H → D1 → R1 → UA03 H
DBUS 02 H → D2 → R2 → UA02 H
DBUS 01 H → D3 → R3 → UA01 H
INCRIMENT WORD
ADVADDR H
GND
MAX/MIN
RIP CLK
CLK
UP/DRN
LD UBADDR L
EN
LOAD

AUTO-INCREMENT FOR 256 WORDS MAX.

+5.0V
R10 1KΩ
DEVSEL H

TP1
A02 H
W4
TP2
W5
A02 L
TP3
RVCC1
8881 E84

UNIBUS ADDRESS DRIVER/COMPARATOR

4 BIT TRANSCEIVER DC005 E95

IN/OUT D3 D2 D1 D0 → UA14 H UA13 H UA12 H UA15 H
MATCH H
BU3 BU2 BU1 BU0 MENB
BUS A14 L EK1
BUS A13 L EK2
BUS A12 L EC1
BUS A15 L ED2
JA3 JA2 JA1
JV3 JV2 JV1
XMIT REC
E96
GND

4 BIT TRANSCEIVER DC005 E106

IN/OUT D3 D2 D1 D0 → UA08 H UA07 H UA06 H UA16 H
MATCH H
BUS A08 L EN2
BUS A07 L EP2
BUS A06 L EL1
BUS A16 L EE2
E96
GND

4 BIT TRANSCEIVER DC005 E94

IN/OUT D3 D2 D1 D0 → UA11 H UA10 H UA09 H UA17 H
MATCH H
BUS A11 L EL1
BUS A10 L EP1
BUS A09 L ER1
BUS A17 L ED1
E96
GND
MSTR H

4 BIT TRANSCEIVER DC005 E107

IN/OUT D3 D2 D1 D0 → UA05 H UA04 H UA03 H TMSYN H
MATCH H
BUS A05 L EV1
BUS A04 L EU2
BUS A03 L EV2
BUS MSYN L EE1
E96
GND

UNIBUS ADDRESS SELECTOR SWITCH
W4=76X XX0,2Q
W5=76X XX4,6Q
RANGE:
760 000Q-
777 776Q

UNIBUS DATA REGISTER

UDASA

2908 BUS TRANCEIVER E61

DBUS 00 H → TX0 → RX0 → DBUS 00 H
DBUS 01 H → TX1 → RX1 → DBUS 01 H
DBUS 02 H → TX2 → RX2 → DBUS 02 H
DBUS 03 H → TX3 → RX3 → DBUS 03 H
BUS0 ↔ CS2 ↔ BUS D00 L
BUS1 ↔ CR2 ↔ BUS D01 L
BUS2 ↔ CU2 ↔ BUS D02 L
BUS3 ↔ CT2 ↔ BUS D03 L
TXCLK BUS ENO → PAR
RX/LCH/EN
RXEN

2908 BUS TRANCEIVER E60

DBUS 04 H → TX0 → RX0 → DBUS 04 H
DBUS 05 H → TX1 → RX1 → DBUS 05 H
DBUS 06 H → TX2 → RX2 → DBUS 06 H
DBUS 07 H → TX3 → RX3 → DBUS 07 H
BUS0 ↔ CN2 ↔ BUS D04 L
BUS1 ↔ CP2 ↔ BUS D05 L
BUS2 ↔ CV2 ↔ BUS D06 L
BUS3 ↔ CM2 ↔ BUS D07 L
TXCLK BUS ENO → PAR
RX/LCH/EN
RXEN

2908 BUS TRANCEIVER E53

DBUS 08 H → TX0 → RX0 → DBUS 08 H
DBUS 09 H → TX1 → RX1 → DBUS 09 H
DBUS 10 H → TX2 → RX2 → DBUS 10 H
DBUS 11 H → TX3 → RX3 → DBUS 11 H
BUS0 ↔ CL2 ↔ BUS D08 L
BUS1 ↔ CK2 ↔ BUS D09 L
BUS2 ↔ CJ2 ↔ BUS D10 L
BUS3 ↔ CH1 ↔ BUS D11 L
TXCLK BUS F.NO → PAR
RX/LCH/EN
RXEN

2908
+5V = PIN 20
GND = PINS 5,15
TXCLK IS AN EDGE TRIGGERED LATCH
RX/LCH/EN IS AN ENABLE FOR A TRANSPARENT LATCH

2908 BUS TRANCEIVER E52

DBUS 12 H → TX0 → RX0 → DBUS 12 H
DBUS 13 H → TX1 → RX1 → DBUS 13 H
DBUS 14 H → TX2 → RX2 → DBUS 14 H
DBUS 15 H → TX3 → RX3 → DBUS 15 H
BUS0 ↔ CH2 ↔ BUS D12 L
BUS1 ↔ CF2 ↔ BUS D13 L
BUS2 ↔ CE2 ↔ BUS D14 L
BUS3 ↔ CD2 ↔ BUS D15 L
TXCLK BUS ENO → PAR
RX/LCH/EN
RXEN

LD UBDATA L → BUS ENB L
BUS LTCH L → RD UBDATA L

UNIBUS DATA AND ADDRESS

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE: UDA # 1
CHK'D.	DATE	BOARD LOCATION: SHEET 9 OF 15		
PS:<DOUGHERTY>UDA1E9.DRW 20-JUL-82 12:53	NEXT HIGHER ASSEMBLY: B-DD-M7161-0			SIZE K / CODE CS / NUMBER M7161-0-UDA1 / REV. E
FIRST USED ON OPTION/MODEL: UDA				

NOTES:
1) BUS NPG IN TO OUT JUMPER MUST BE REMOVED (CB1 FROM CA1).
2) C0 IS UNDRIVEN AND PULLED INACTIVE
3) GATES MARKED WITH A STAR (*) MAY BE 74SXX OR 74LSXX.
4) INTR H CONNECTION TO 8641 IS TO GENERATE SSYNC FOR NON-EXISTANT MEMORY.

ENSLAVE H	INIT MODE =0	RUN MODE =1
UDAIP R	-	POLL
X0/4 W	INIT	INIT
UDASA R	STATUS	0
X2/6 W	ADDR/DATA	PURGE

UNIBUS I/O PAGE ADDRESS DECODER

DECODER 74LS138 E75

RDX0.RUN L
RDX2.RUN L
WRTX0.RUN L
WRTX2.RUN L
RDX0.INIT L
RDX2.INIT L
WRTX0.INIT L
WRTX2.INIT L

INTR L → 74LS279 E76 → PURGED L (VAX BUFFER PURGED)

ENSLAVE H → 74LS14 E87 → 74LS279 E76 → SCAN L (POLL OF COMMAND BUFFER REQUESTED)

NOTE: FOR INTERRUPT LEVEL 4 THE JUMPERS ARE: 2-5,3-4, 6-7,8-9,10-11,12-13.

+5.0V
R39 178Ω 1%
R38 178Ω 1%

BG4 OUT H (DT2) BUS BR7 L
BG4 IN H (DS2) BUS BR6 L
BG5 OUT H (DR2) BUS BR5 L
BG5 IN H (DP2) BUS BR4 L
BG6 OUT H (DN2)
XE74 PIN SOCK
(DK2) BG7 IN H
(DL2) BG7 OUT H
(CM2) BG6 IN H

R40 383Ω 1%

BUS AC LO L (CV1) → 8837 E64 → ACLO H
BUS DC LO L (CN1) → 8837 E64
BUS INIT L (DL1) → 8837 E64
BUS PA L (CC1) → 8837 E64
BUS PB L (CS1) → 8837 E64 → 74LS04 E109

SSYNC EN H, C1 H → 74S08 E86 → DEVSEL H

C1 H, A01 H → 74S158 E75 (SEL, EN)

74LS11 E65 → BUS RST L

DEVSEL H TO SSYNC EN H
145-521 NSEC DELAY HIGH
201-519 NSEC DELAY LOW

+5.0V R19 1KΩ
DEVSEL H → 8881 E84 → R20 470Ω → BUS LTCH L
C9 680 pf

74LS04 E85 → SSYNC EN H
8881 E84 → BUS SSYNC L
74LS04 E85 → SSYNC L

UNIBUS CONTROL DC013 E117
REQUEST MASTER
STL GRANT
BG OUT
BG IN
BUS REQ
BUS SSYN
BUS BBSY
BUS NPR
BUS SACK
SACK
CLR EN
MASTER CLR INIT
→ INTRPTMSTR L

INTERRUPT CONTROL

+5.0V R37 178Ω 1%
→ UBMASTER L

UNIBUS PARITY ERROR DETECTION

BUS LTCH L, I/O CLR L → 74S02 E126 → 74LS74 E125 → PRTYERR H

BUS PA/PB L
1 1 NO ERROR IN SLAVE DATI/P
1 0 SLAVE ERROR IN DATAI/P
1 X RESERVED

I/O CONTROL REGISTER

8 BIT LATCH 74LS259 E66

UTEST H
NPR REQ H
I/O CLR L
DATO H
ENSLAVE H
BUS REQ H

IOC SEL 2 H
IOC SEL 1 H
IOC SEL 0 H
→ DATA EN RESET
CLK UIOC L

SET IOC H, RST1 L → 74S08 E86

INTR H → 8881 E84 → FM1 BUS INTR L

74LS04 E85 → INTR L

BUS NPG IN H (CA1)
+5.0V R35 178Ω 1%
R36 383Ω 1%

UNIBUS CONTROL DC013 E116
REQUEST MASTER
STL GRANT
BG OUT
BG IN
BUS REQ
BUS SSYN
BUS BBSY
BUS NPR
BUS SACK
SACK
CLR EN
MASTER CLR INIT

R'CC1
→ (CB1) BUS NPG OUT H
→ (FJ1) BUS NPR L
→ (FD1) BUS BBSY L
→ (FT2) BUS SACK L

NPR CONTROL

SHIFT REG 74LS164 E124
DATA IN
0R 1R 2R 3R 4R 5R 6R 7R
NPR REQ H
TP21 W14 TP22 TP23 TP24
CLR
CLK
SA.CNTR 02 H

74LS04 E109 → MSTR H

74S08 E86 → MCLR H

74LS00 E98 → 74LS11 E65 → BUS ENB L
RDX2.INIT L

E108
MSTR H, SSYNC L → 74LS279 E76
60NS 120NS 160NS 190NS 250NS
ADVADDR H
XFER L
74S02 E126 → BUS LTCH L
BUS SSYNC L
TMSYN H

INTR H → (EJ1) BUS SSYNC L, SSYNC H
DATO H → (EF2) BUS C1 L, C1 H
UA02 H → (EF1) BUS A02 L, A02 H → 74LS04 E109 → A02 L
UA01 H → (EH1) BUS A01 L, A01 H
8641 E83 → 74LS04 E109 → SSYNC L

RVCC1
I/O CLR L
R/W UBDATA L
START L → 74LS74 E125 → 74LS11 E65 → UDATARDY H
INITIALIZATION BASE ADDRESS WRITTEN

WRTX2.INIT L → 74S08 E86

74LS04 E109 → UA01 H

BUS C1/C0 L
DATO 1 0 DATA XFER MASTER TO SLAVE
DATI 1 1 DATA XFER SLAVE TO MASTER

UNIBUS CONTROL

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REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN.	DATE 20-JUL-82	ENG. DATE
	CHK'D.	DATE	BOARD LOCATION: SHEET 10 OF 15
PS:<DOUGHERTY>UDA1EA.DRW;20-JUL-82 10:56			NEXT HIGHER ASSEMBLY: B-DD-M7161-0
FIRST USED ON OPTION/MODEL: UDA			

TITLE: UDA # 1

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E

DATA BUS CONNECTOR

P5

SET IOC H
IOC SEL 2 H
IOC SEL 1 H
IOC SEL 0 H
CLK DIOC L
LD DCR L
LD RTCS L
RD RTDS L
RST2 L

OCTAL BUS TRNVER 74LS245 E115

DBUS 15 H
DBUS 14 H
DBUS 13 H
DBUS 12 H
DBUS 11 H
DBUS 10 H
DBUS 09 H
DBUS 08 H

OCTAL BUS TRNVER 74LS245 E105

DBUS 07 H
DBUS 06 H
DBUS 05 H
DBUS 04 H
DBUS 03 H
DBUS 02 H
DBUS 01 H
DBUS 00 H

ALU TO BUS H
BUS SRC 3 H
74S02 E67
DEADBAND L
74S02 E126

+5.0V
E42 4.7KΩ
74LS14 E87
DTEST L

CONTROL CONNECTOR

HEADER 40POS WITH LATCHES

P6

LD BUFFER L
RD BUFFER L
LD SERDES L
RD SERDES L
LD DBAR L
RD ECC RSDU L
LD UBAR L
CLK SERDES H
CLK ENB1 H
R33 62Ω
CLK BDR H
D FAILTEST H
DLY UPROC H

DATA WORD CLK L
OVERRUN H
RECV ERR H
RTDS RCVD H
RAM PE L
ECC RDY H
RTCS RDY H
DATA RDY H

UNIBUS CONTROL REGISTER WRITE ONLY

8 D FLOP 74LS273 E104

DBUS 00 H
DBUS 01 H
DBUS 10 H
DBUS 11 H
DBUS 12 H
DBUS 13 H
DBUS 14 H
DBUS 15 H
RST1 L

UA16 H
UA17 H
DFAIL H
LED 1 L
LED 2 L
LED 4 L
LED 8 L

D4 D3 D2 D1

+5.0V

UNIBUS CONTROL REGISTER READ/WRITE

8 D FF 74LS374 E123

DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
EN OUT CLK

8 D FF 74LS374 E113

DBUS 08 H
DBUS 09 H
DBUS 10 H
DBUS 11 H
DBUS 12 H
DBUS 13 H
DBUS 14 H
DBUS 15 H
RD UCR L
LD UCR L
EN OUT CLK

NOTE: DBUS 00 H MUST BE PULLED UP
THE OTHER PULLUPS ARE OPTIONAL.

+5.0V
E42 4.7KΩ
DBUS 00 H

+5.0V AA2
+5.0V BA2
+5.0V CA2
+5.0V DA2
+5.0V EA2
+5.0V FA2

GND AC2
GND AT1
GND BC2
GND BT1
GND CC2
GND CT1
GND DC2
GND DT1
GND EC2
GND ET1
GND FC2
GND FT1

NOTE: C1 THRU C8
47μF
10V
+50%,-10%

C2 C1 C5 C4 C3 C6 C7 C8

R6 100Ω RVCC1
R22 100Ω RVCC2
R5 100Ω RVCC3
+5.0V

SA.CNTR 15 H
74LS14 E87
60H2 H

UDA2 CONNECTORS AND CR REG

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE: UDA # 1	
CHK'D.	DATE	BOARD LOCATION: SHEET 11 OF 15			
PS:<DOUGHERTY>UDA1E8.DRW 20-JUL-82 13:43		NEXT HIGHER ASSEMBLY:		SIZE K	CODE CS
FIRST USED ON OPTION/MODEL: UDA		B-DD-M7161-0		NUMBER M7161-0-UDA1	REV. E

+5.0V

C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29

+5.0V

C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C44 C45 C46 C47 C48 C49

+5.0V

C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69

+5.0V

C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89

+5.0V

C90 C91 C92 C93 C96 C97 C98 C99 C100 C101 C102 C103

NOTE:
ALL CAPACITORS ON THIS SHEET:
4.7nF
50V
+80%,-20%

SPARES

16 PIN SOCK E118

16 PIN SOCK E129

74S74 E48

74S04 E80

74S04 E80

74S04 E80

74S04 E80

20 PIN SOCK E97

20 PIN SOCK E110

20 PIN SOCK E119

20 PIN SOCK E121

QUAD BUFFER 74LS244 E59
A0 A1 A2 A3 EN
0Y 1Y 2Y 3Y

+5.0V E42 4.7KΩ

+5.0V E11 1KΩ

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 28-JUL-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION: SHEET 12 OF 15	

PS:<DOUGHERTY>UDA1EC.DRW|28-JUL-82 13:44| NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA | B-DD-M7161-0

TITLE: UDA # 1

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E

Vertical location (A-D) Direction of line (Left, Right, Up, Down)
or electrical (Input, Output, Both)
KEY: SS-VH,D or backplane pin (Pin)
Schematic Sheet Horizontal location (1-8)

+5.0V	1-D5,D	2-C1,D	4-A4,D	4-B5,D	4-B5,D	4-B6,D	
	4-C5,D	4-C5,D	4-C5,D	4-C6,D	5-B4,D	5-C3,D	5-C3,D	8-B3,D
	8-B3,L	8-C2,L	8-C3,D	8-C3,D	8-C4,D	9-D5,D	10-C1,D	10-C3,R
	10-D2,R	10-D4,D	11-A7,D	11-B1,L	11-C4,R	11-D2,D	12-A3,D	12-A4,D
	12-B7,D	12-C7,D	12-C7,D	12-D7,D	12-D7,D	11-B3,R <AA2>		
	11-B3,R <BA2>		11-B3,R <CA2>		11-B3,R <DA2>		11-B3,R <EA2>	
			11-B3,R <FA2>					
50H2 H	5-B7,R	11-A1,L						
A REG 0 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	6-C1,L			
A REG 1 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	6-C1,L			
A REG 2 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	6-C1,L			
A REG 3 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	6-C1,L			
A01 H	10-A2,L	10-D6,R						
A02 H	9-D6,R	10-A2,L						
A02 L	9-D6,R	10-A1,L						
ACLO H	7-A6,R	3-C6,R	10-D7,L					
ADVADDR H	9-A8,R	10-B4,L						
ALU DEST 0 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A4,L	5-A8,R		
ALU DEST 1 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A4,L	5-A7,R		
ALU DEST 2 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A4,L	5-A7,R		
ALU FUNC 0 H	1-B2,R	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R		
	7-D2,L							
ALU FUNC 1 H	1-B2,R	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R		
	7-D2,L							
ALU FUNC 2 H	1-B2,R	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R		
	7-D2,L							
ALU MSB H	1-D7,L	3-C7,R						
ALU SOURCE 0 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R	7-C4,L		
ALU SOURCE 1 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R	7-D2,L		
ALU SOURCE 2 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-A8,R	7-D2,L		
ALU TO BUS H	1-D8,R	2-C3,R	5-A8,R	7-C4,L	11-B7,R			
B REG 0 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-B8,R	7-D5,L		
B REG 1 H	1-B3,R	1-B6,R	1-C4,R	1-C8,R	5-B8,R	7-D5,L		
B REG 2 H	1-B3,R	1-B4,R	1-B6,R	1-B8,R	5-B8,R	7-D5,L		
B REG 3 H	1-B3,R	1-B4,R	1-B6,R	1-B8,R	5-B8,R	7-C5,L		
BG4 IN H	10-D2,R <DS2>							
BG4 OUT H	10-D2,R <DT2>							
BG5 IN H	10-D2,R <DP2>							
BG5 OUT H	10-D2,R <DR2>							
BG6 IN H	10-D1,L <DM2>							
BG6 OUT H	10-D2,R <DN2>							
BG7 IN H	10-D1,L <DK2>							
BG7 OUT H	10-D1,L <DL2>							
BR ADR 00 H	4-C8,R	4-D4,R	4-D7,R	5-D1,L	5-D8,R			
BR ADR 01 H	4-C8,R	4-D4,R	4-D7,R	5-D1,L	5-D8,R			
BR ADR 02 H	4-C8,R	4-D4,R	4-D7,R	5-D1,L	5-D8,R			
BR ADR 03 H	4-C8,R	4-D4,R	4-D7,R	5-D1,L	5-D8,R			
BR ADR 04 H	4-B4,R	4-B7,R	4-C8,R	5-D1,L	5-D8,R			
BR ADR 05 H	4-B4,R	4-B7,R	4-C8,R	5-D1,L	5-D8,R			
BR ADR 06 H	4-B4,R	4-B7,R	4-C8,R	5-C1,L	5-D8,R			
BR ADR 07 H	4-B4,R	4-B7,R	4-C8,R	5-C1,L	5-D8,R			
BR ADR 08 H	4-A4,R	4-A7,R	4-C8,R	5-D8,R	6-C6,L			
BR ADR 09 H	4-A4,R	4-A7,R	4-C8,R	5-C8,R	6-C6,L			
BR ADR 10 H	4-A4,R	4-A7,R	4-C8,R	5-C8,R	6-C6,L			
BR ADR 11 H	4-A4,R	4-A7,R	4-C8,R	5-C8,R	6-C6,L			

BUS A01 L	10-A2,L <EH1>
BUS A02 L	10-A2,L <EF1>
BUS A03 L	9-B5,R <EV2>
BUS A04 L	9-B5,R <EU2>
BUS A05 L	9-B5,R <EV1>
BUS A06 L	9-C5,R <EU1>
BUS A07 L	9-C5,R <EP2>
BUS A08 L	9-C5,R <EN2>
BUS A09 L	9-B6,R <ER1>
BUS A10 L	9-B6,R <EP1>
BUS A11 L	9-B6,R <EL1>
BUS A12 L	9-C6,R <EC1>
BUS A13 L	9-C6,R <EK2>
BUS A14 L	9-C6,R <EK1>
BUS A15 L	9-C6,R <ED2>
BUS A16 L	9-C5,R <EE2>
BUS A17 L	9-B6,R <ED1>
BUS AC LO L	10-D8,R <CV1>
BUS BBSY L	10-B1,L <FD1>
BUS BR4 L	10-D1,L <DH2>
BUS BR5 L	10-D1,L <DF2>
BUS BR6 L	10-D1,L <DE2>
BUS BR7 L	10-D1,L <DD2>
BUS C1 L	10-A2,L <EF2>
BUS D00 L	9-D2,L <CS2>
BUS D01 L	9-D2,L <CR2>
BUS D02 L	9-D2,L <CU2>
BUS D03 L	9-D2,L <CT2>
BUS D04 L	9-C1,L <CN2>
BUS D05 L	9-C1,L <CP2>
BUS D06 L	9-C1,L <CV2>
BUS D07 L	9-C1,L <CM2>
BUS D08 L	9-B2,L <CL2>
BUS D09 L	9-B2,L <CK2>
BUS D10 L	9-B2,L <CJ2>
BUS D11 L	9-B2,L <CH1>
BUS D12 L	9-A1,L <CH2>
BUS D13 L	9-A1,L <CF2>
BUS D14 L	9-A1,L <CE2>
BUS D15 L	9-A1,L <CD2>
BUS DC LO L	10-C8,R <CN1>
BUS DEST 0 H	2-C3,R 5-B8,R 7-B4,L
BUS DEST 1 H	2-C3,R 5-B8,R 7-B4,L
BUS DEST 2 H	2-C3,R 5-B8,R 7-B4,L
BUS DEST 2 L	2-A3,R 7-B4,L
BUS ENB L	9-A3,R 10-B1,L
BUS INIT L	10-C8,R <DL1>
BUS INTR L	10-C4,L <FM1>
BUS LTCH L	9-A3,R 10-B1,L 10-C3,R 10-C7,R
BUS MSYN L	9-B5,R <EE1>
BUS NPG IN H	10-C3,R <CA1>
BUS NPG OUT H	10-C1,L <CB1>
BUS NPR L	10-C1,L <FJ1>
BUS PA L	10-C8,R <CC1>
BUS PB L	10-C8,R <CS1>
BUS REQ H	10-C5,L
BUS RST L	2-B7,R 10-D5,L
BUS SACK L	10-B1,L <FT2>
BUS SRC 0 H	1-A4,R 1-A7,R 2-D3,R 5-C8,R 6-C1,L
BUS SRC 1 H	1-A4,R 1-A7,R 2-D3,R 5-C8,R 6-C1,L
BUS SRC 2 H	1-A4,R 1-A7,R 2-D3,R 5-C8,R 6-B1,L

BUS SRC 3 H	1-A4,R 1-A7,R 5-C8,R 6-B1,L 11-B7,R
BUS SSYNC L	10-B2,L 10-C3,L 10-A2,L <EJ1>
C1 H	10-A2,L 10-D6,R 10-D7,R
C12 IN H	1-C1,L 1-C8,R
C16 H	1-C7,L 3-C7,R
C4 IN H	1-C1,L 1-C4,R
C8 IN H	1-B6,R 1-C1,L
CARRY IN H	1-B2,R 1-B3,R 5-A7,R 7-D2,L
CLK BDR H	2-D4,L 11-A8,R
CLK DIOC L	2-B3,L 11-C8,L
CLK ENB H	2-D4,L 5-B7,R
CLK ENB L	2-D4,L 8-C3,R
CLK ENB1 H	2-B3,R 2-D4,L 11-A8,R
CLK ENB2 H	2-D6,L
CLK ENB3 H	2-D6,L 3-C3,R
CLK ENB4 H	2-D5,L
CLK SERDES H	2-C4,L 11-A8,R
CLK UIOC L	2-B3,L 10-C6,R
COND EXEC H	2-B6,R 5-C8,R 6-C6,L
CROM 24 H	7-B5,R 7-D7,L
CROM 25 H	7-B5,R 7-D7,L
CROM 26 H	7-B5,R 7-D7,L
CROM 27 H	7-B5,R 7-D7,L
CROM 32 H	6-B3,R 7-B5,L
CROM 33 H	6-B3,R 7-B5,L
CROM 34 H	6-B3,R 7-B5,L
CROM 35 H	6-A3,R 7-B5,L
CROM 36 H	5-A4,R 7-B5,L
CROM 39 H	7-B5,L 7-D2,R
CROM 44 H	5-A4,R 7-B3,L
CROM 45 H	5-A4,R 7-B3,L
CROM 46 H	5-A4,R 7-B3,L
CROM ERR L	3-D7,L
CROM PE L	3-D7,R 5-B4,L 5-D7,R
CROM PE1 L	5-A5,L 5-B4,R
CROM PE2 L	5-B4,L 5-B4,R
CROM PRTY H	5-C8,R 6-C6,L
D FAILTEST H	5-B5,L 11-A8,R
D TIMEOUT H	5-B5,L 5-C7,R
DATA RDY H	3-B6,R 11-A7,L
DATA WORD CLK L	3-B7,R 11-A7,L
DATO H	8-A6,R 8-C6,R 10-A3,R 10-C5,L
DBUS 00 H	1-A4,R 1-D2,L 3-C8,R 4-D2,R 8-B3,L 8-D6,L
	9-D2,L 9-D3,R 9-D7,R 11-B6,L 11-C4,L 11-C5,R 11-D3,R 11-D5,R
DBUS 01 H	1-A4,R 1-C2,L 4-D2,R 8-B4,R 8-D6,L 9-A7,R
	9-D2,L 9-D3,R 11-B6,L 11-C4,L 11-C5,R 11-D5,R
DBUS 02 H	1-A4,R 1-C2,L 4-D2,R 8-B3,L 8-C6,L 9-A7,R
	9-D2,L 9-D3,R 11-B4,L 11-B5,R 11-B6,L
DBUS 03 H	1-A4,R 1-C2,L 4-C2,R 8-B4,R 8-C6,L 9-A7,R
	9-D2,L 9-D3,R 11-B4,L 11-B5,R 11-B6,L
DBUS 04 H	1-A5,R 1-D4,L 4-B2,R 8-B3,L 8-C6,L 9-A7,R
	9-C1,L 9-C2,R 11-B4,L 11-B5,R 11-B6,L
DBUS 05 H	1-B5,R 1-D4,L 4-B2,R 8-B4,R 8-C6,L 9-B7,R
	9-C1,L 9-C2,R 11-B4,L 11-B5,R 11-C6,L
DBUS 06 H	1-B5,R 1-D4,L 4-B2,R 8-B3,L 8-C6,L 9-B7,R
	9-C1,L 9-C2,R 11-B4,L 11-B5,R 11-C6,L
DBUS 07 H	1-B5,R 1-D4,L 4-B2,R 8-B4,R 8-C6,L 9-B7,R
	9-C1,L 9-C2,R 11-B4,L 11-B5,R 11-C6,L
DBUS 08 H	1-A7,R 1-D6,L 8-B3,L 8-B6,L 9-B2,L 9-B3,R
	9-B7,R 11-A5,R 11-B4,L 11-C6,L
DBUS 09 H	1-A7,R 1-D6,L 8-B4,R 8-B6,L 9-B2,L 9-B3,R

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REVISIONS		
CHK	CHANGE NO.	REV.

DRN.	DATE 20-JUL-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION:	
		SHEET 13 OF 15	

DSK:UDAIE.T2P[4,50] 20-JUL-82 12:55 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA B-DD-M7161-0

TITLE: UDA # 1

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E

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                                  9-D7,R 11-A4,L 11-A5,R 11-C6,L
DBUS 10 H ....................... 1-A7,R  1-D6,L  8-B3,L  8-B6,L  9-B2,L  9-B3,R
                                  9-D7,R 11-A4,L 11-A5,R 11-D5,R 11-D6,L
DBUS 11 H ....................... 1-A7,R  1-D6,L  8-B4,R  8-B6,L  9-B2,L  9-B3,R
                                  9-C7,R 11-A4,L 11-A5,R 11-D5,R 11-D6,L
DBUS 12 H ....................... 1-A8,R  1-D7,L  8-B3,L  8-B6,L  9-A1,L  9-A2,R
                                  9-C7,R 11-A4,L 11-A5,R 11-D5,R 11-D6,L
DBUS 13 H ....................... 1-B8,R  1-D7,L  8-B4,R  8-B6,L  9-A1,L  9-A2,R
                                  9-C7,R 11-A4,L 11-A5,R 11-C5,R 11-D6,L
DBUS 14 H ....................... 1-B8,R  1-D7,L  8-B3,L  8-B6,L  9-A1,L  9-A2,R
                                  9-C7,R 11-A4,L 11-A5,R 11-C5,R 11-D6,L
DBUS 15 H ....................... 1-B8,R  1-D7,L  8-B4,R  8-B6,L  9-A1,L  9-A2,R
                                  9-C7,R 11-A4,L 11-A5,R 11-C5,R 11-D6,L
DEADBAND L ...................... 1-D8,R  2-C2,L  4-A8,R  8-D2,L 11-B7,R
DEVSEL H ........................ 8-D3,R  9-D4,L 10-C5,R 10-D6,R
DFAIL H ......................... 2-A8,R 11-D3,L
DLY UPROC H ..................... 2-D3,L 11-A8,R
DTEST L ......................... 3-A6,R 11-A6,L
ECC RDY H ....................... 3-B6,R 11-A7,L
ENA HI LTRL L ................... 1-A8,R  1-B1,L
ENA LO LTRL L ................... 1-A1,L  1-A5,R
ENB PAR L ....................... 2-B2,L  4-A8,R
ENBL DPROC H .................... 2-C4,L  4-C5,R  4-D4,R
ENBL UPROC H .................... 2-C4,L  4-D7,R  4-D8,R
ENSLAVE H ....................... 10-C5,L 10-D4,R
ERROR L ......................... 4-A8,R  5-B7,R  5-C5,L
EXEC ON FALSE H ................. 2-B6,R  5-A3,L
EXEC ON TRUE H .................. 2-B6,R  5-A4,L  5-A8,R
EXECUTE H ....................... 2-B5,L  8-B3,L
EXT.FAIL H ...................... 2-A8,R  8-C2,L
EXT.HALT L ...................... 2-C8,R  5-C7,R  8-B3,L
EXT.RST L ....................... 2-C7,R  8-B4,R
EXT.STOP L ...................... 2-C7,R  8-C3,L
F=ZERO H ........................ 1-D3,L  3-C7,R
FAIL L .......................... 2-A6,L  4-C5,R  4-D8,R  5-C7,R
G2 L ............................ 1-C2,R  1-C6,L
GND ............................. 2-B3,R  2-C3,R  7-A3,R  7-A5,R  7-A6,R  7-A8,R
                  8-B4,R  8-C4,R  9-A5,R  9-A6,R  9-A8,R  9-B8,R  9-C5,R  9-C6,R
                  9-C7,R 11-A3,R <AC2>   11-A3,R <AT1>   11-A3,R <BC2>
                 11-A3,R <BT1>   11-A3,R <CC2>   11-A3,R <CT1>   11-A3,R <DC2>
                 11-A3,R <DT1>   11-A3,R <EC2>   11-A3,R <ET1>   11-A3,R <FC2>
                                 11-A3,R <FT1>
I/O CLR L ....................... 3-D7,R 10-A7,R 10-C5,L 10-C7,R
INTR H .......................... 10-A3,R 10-C5,L
INTR L .......................... 10-C4,L 10-D4,R
INTRPTMSTR L .................... 3-D6,R  8-D3,R 10-C1,L
IOC ENABLE H .................... 2-B4,R  5-B8,R  7-B4,L
IOC SEL 0 H ..................... 1-B5,R  1-B8,R  5-C8,R  6-B1,L 10-C6,R 11-C8,L
IOC SEL 1 H ..................... 1-B5,R  1-B8,R  5-C8,R  6-B1,L 10-C6,R 11-C8,L
IOC SEL 2 H ..................... 1-B5,R  1-B8,R  5-B8,R  6-A1,L 10-C6,R 11-C8,L
JUMP OP 1 H ..................... 4-C4,R  4-C8,R  5-C8,R  6-C6,L
LD BD1 L ........................ 2-C2,L  8-D2,L
LD BUFFER L ..................... 2-C2,L 11-B8,R
LD DBAR L ....................... 2-A2,L 11-B8,R
LD DCR L ........................ 2-B2,L 11-C8,L
LD RTCS L ....................... 2-A2,L 11-C8,L
LD SERDES L ..................... 2-A2,L 11-B8,R
LD UBADDR L ..................... 2-A2,L  8-D2,L  9-A8,R
LD UBAR L ....................... 2-A2,L 11-B8,R
LD UBDATA L ..................... 2-A2,L  2-A6,R  9-A3,R
LD UCR L ........................ 2-A2,L 11-A5,R
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LED 1 L ......................... 8-D3,R 11-D3,L
LED 2 L ......................... 8-D3,R 11-D3,L
LED 4 L ......................... 8-C3,R 11-C3,L
LED 8 L ......................... 8-C3,R 11-C3,L
MSTR H .......................... 9-A6,R 10-B1,L 10-B7,R
NPR REQ H ....................... 10-B6,R 10-C5,L
OVERRUN H ....................... 3-B6,R 11-A7,L
P2 L ............................ 1-C2,R  1-C6,L
PADR 0 H ........................ 5-B3,R  5-D2,R  5-D4,L  6-A5,R  6-B8,R  6-C8,R
                  6-D4,R  7-B3,R  7-B6,R  7-B8,R  7-C6,R  7-C8,R  7-D3,R
PADR 1 H ........................ 5-B3,R  5-D2,R  5-D4,L  6-A5,R  6-B8,R  6-C8,R
                  6-D4,R  7-B3,R  7-B6,R  7-B8,R  7-C6,R  7-C8,R  7-D3,R
PADR 10 H ....................... 5-B3,R  5-C2,R  5-C4,L  6-A5,R  6-A8,R  6-C4,R
                  6-C8,R  7-A3,R  7-A8,R  7-B6,R  7-C3,R  7-C6,R  7-C8,R
PADR 11 H ....................... 5-B3,R  5-B4,L  5-C2,R  6-A5,R  6-A8,R  6-C4,R
                  6-C8,R  7-A3,R  7-A6,R  7-A8,R  7-C3,R  7-C6,R  7-C8,R
PADR 2 H ........................ 5-B3,R  5-D2,R  5-D4,L  6-A5,R  6-B8,R  6-C8,R
                  6-D4,R  7-B3,R  7-B6,R  7-B8,R  7-C6,R  7-C8,R  7-D3,R
PADR 3 H ........................ 5-B3,R  5-D2,R  5-D4,L  6-A5,R  6-B8,R  6-C4,R
                  6-C8,R  7-B3,R  7-B6,R  7-B8,R  7-C3,R  7-C6,R  7-C8,R
PADR 4 H ........................ 5-B3,R  5-C2,R  5-D4,L  6-A5,R  6-B8,R  6-C4,R
                  6-C8,R  7-A3,R  7-B6,R  7-B8,R  7-C3,R  7-C6,R  7-C8,R
PADR 5 H ........................ 5-B3,R  5-C2,R  5-D4,L  6-A5,R  6-B8,R  6-C4,R
                  6-C8,R  7-A3,R  7-B6,R  7-B8,R  7-C3,R  7-C6,R  7-C8,R
PADR 6 H ........................ 5-B3,R  5-C2,R  5-C4,L  6-A5,R  6-B8,R  6-C4,R
                  6-C8,R  7-A3,R  7-B6,R  7-B8,R  7-C3,R  7-C6,R  7-C8,R
PADR 7 H ........................ 5-B3,R  5-C2,R  5-C4,L  6-A5,R  6-B8,R  6-C4,R
                  6-C8,R  7-A3,R  7-B6,R  7-B8,R  7-C3,R  7-C6,R  7-C8,R
PADR 8 H ........................ 5-B3,R  5-C2,R  5-C4,L  6-A5,R  6-A8,R  6-C4,R
                  6-C8,R  7-A3,R  7-A8,R  7-B6,R  7-C3,R  7-C6,R  7-C8,R
PADR 9 H ........................ 5-B3,R  5-C2,R  5-C4,L  6-A5,R  6-A8,R  6-C4,R
                  6-C8,R  7-A3,R  7-A8,R  7-B6,R  7-C3,R  7-C6,R  7-C8,R
PASS H .......................... 3-D3,L
PASS TEST H ..................... 2-B6,R  3-D2,L  4-C5,R  4-D8,R  8-B4,R
PASS TEST L ..................... 2-B6,R  3-D2,L  5-B7,R
PR 28 H ......................... 5-B8,R  7-B4,L
PR 29 H ......................... 5-B8,R  7-A4,L
PR 30 H ......................... 5-B8,R  7-A4,L
PR 31 H ......................... 5-B8,R  7-A4,L
PROBE 1 H ....................... 8-B2,L  8-D3,R
PROCCLK L ....................... 1-B3,R  1-B4,R  1-B6,R  1-B8,R  2-A6,R  2-B2,R
                                 2-C4,L  3-C8,R  8-D2,L
PROMENBL H ...................... 5-B3,R  5-C3,R  6-A5,R  6-A8,R  6-C4,R  6-C8,R
                                 7-A3,R  7-A6,R  7-A8,R  7-C3,R  7-C6,R  7-C8,R
PRTYERR H ....................... 3-D6,R 10-C6,L
PURGED L ........................ 3-D6,R 10-D3,L
Q7 H ............................ 1-C4,R  1-C6,L
R/W UBDATA L .................... 2-A5,L 10-A7,R
RA=RB L ......................... 6-A3,R  7-B2,L
RAM 15 H ........................ 1-C1,L  1-C8,R
RAM 7 H ......................... 1-C4,R  1-C6,L
RAM PE L ........................ 3-B6,R  5-B5,R 11-A7,L
RAM PE1 L ....................... 5-B4,L  5-D7,R
RD BS0 L ........................ 2-D2,L  8-D2,L
RD BUFFER L ..................... 2-D2,L 11-B8,R
RD CNST L ....................... 2-D2,L  8-A6,R
RD ECC RSDU L ................... 2-D2,L 11-B8,R
RD RTDS L ....................... 2-D1,L 11-C8,L
RD SERDES L ..................... 2-D2,L 11-B8,R
RD UBDATA L ..................... 2-A6,R  2-D2,L  9-A3,R
RD UCR L ........................ 2-D2,L 11-A5,R
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```
RDX0.INIT L ..................... 10-D5,L
RDX2.INIT L ..................... 10-B2,R 10-D5,L
RDX2.RUN L ...................... 10-D5,L
RECV ERR H ...................... 3-B6,R 11-A7,L
REQSTOP L ....................... 2-C8,R  5-C3,R  6-C4,R  6-C8,R  7-C3,R  7-C6,R
                                 7-C8,R
RESET L ......................... 2-A6,L  4-D4,R  4-D7,R  5-C7,R
RETURN L ........................ 4-C7,L
RST TIMER H ..................... 5-B6,L
RST1 L .......................... 2-C6,L  2-C7,R 10-B7,R 11-C5,R
RST2 L .......................... 2-C6,L  2-C7,R 11-C8,L
RTCS RDY H ...................... 3-B6,R 11-A7,L
RTDS RCVD H ..................... 3-B6,R 11-A7,L
RVCC ............................ 3-D7,R
RVCC1 ........................... 1-B2,R  1-C2,R  2-C5,D  2-C6,D  2-D3,L  2-D7,R
                                 9-D6,R 10-A7,R 10-C3,R 11-B1,L
RVCC2 ........................... 3-A6,R  3-A7,R  3-C6,R  3-C7,R  5-A4,R  5-B4,R
                  5-C4,R  6-A2,R  6-B2,R  7-C2,R  7-C5,R  8-A6,R 11-B1,L
RVCC3 ........................... 3-D3,D  3-D3,D  4-A4,R  4-A7,R  4-B4,R  4-B7,R
                                 4-C3,R  4-C7,R 11-B1,L
SA.CNTR 00 H .................... 3-C2,L
SA.CNTR 01 H .................... 3-C2,L
SA.CNTR 02 H .................... 3-C2,L 10-B6,R
SA.CNTR 03 H .................... 3-C2,L
SA.CNTR 04 H .................... 3-B2,L
SA.CNTR 05 H .................... 3-B2,L
SA.CNTR 06 H .................... 3-92,L
SA.CNTR 07 H .................... 3-B2,L
SA.CNTR 08 H .................... 3-B2,L
SA.CNTR 09 H .................... 3-B2,L
SA.CNTR 10 H .................... 3-B2,L
SA.CNTR 11 H .................... 3-B2,L
SA.CNTR 12 H .................... 3-A2,L
SA.CNTR 13 H .................... 3-A2,L
SA.CNTR 14 H .................... 3-A2,L
SA.CNTR 15 H .................... 3-A2,L 11-A2,R
SCAN L .......................... 3-D6,R 10-D3,L
SEL LITERAL L ................... 1-A2,R  1-A5,R  1-A8,R  7-C4,L
SENSE H ......................... 5-C8,R  6-C6,L
SEQ ADR 00 H .................... 4-D1,L  4-D5,L  5-D4,R  5-D5,L  8-A3,L
SEQ ADR 01 H .................... 4-D1,L  4-D5,L  5-D4,R  5-D5,L  8-A4,R
SEQ ADR 02 H .................... 4-D1,L  4-D5,L  5-D4,R  5-D5,L  8-A3,L
SEQ ADR 03 H .................... 4-C1,L  4-D5,L  5-D4,R  5-D5,L  8-A4,R
SEQ ADR 04 H .................... 4-C1,L  4-C5,L  5-D4,R  8-A3,L
SEQ ADR 05 H .................... 4-C1,L  4-C5,L  5-C4,R  8-A4,R
SEQ ADR 06 H .................... 4-C1,L  4-C5,L  5-C4,R  8-B3,L
SEQ ADR 07 H .................... 4-C1,L  4-C5,L  5-C4,R  8-B4,R
SEQ ADR 08 H .................... 4-B1,L  4-B5,L  5-C4,R  9-B3,L
SEQ ADR 09 H .................... 4-A5,L  4-B1,L  5-C4,R  8-B4,R
SEQ ADR 10 H .................... 4-A1,L  4-A5,L  5-B4,R  8-B3,L
SEQ ADR 11 H .................... 4-A1,L  4-A5,L  5-B4,R  8-B4,R
SEQ CLK L ....................... 2-B2,R  2-C4,L  3-D3,R  4-A4,R  4-A7,R  5-C2,R
                  5-C4,R  6-A2,R  6-B2,R  6-B6,R  7-A5,R  7-C2,R  7-C5,R  8-B3,L
                                  8-D2,L
SET IOC H ....................... 1-B5,R  1-B8,R  5-B8,R  6-A1,L 10-B7,R 11-C8,L
SSYNC EN H ...................... 10-D3,L 10-D7,R
SSYNC H ......................... 10-A2,L
SSYNC L ......................... 3-D6,R 10-A1,L 10-B7,R 10-C2,R
STOP L .......................... 2-B6,L  5-B7,R
TEST COND 0 H ................... 3-A6,R  7-B5,R  7-D7,L
TEST COND 1 H ................... 3-A6,R  7-A5,R  7-D7,L
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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE	ENG.	DATE	TITLE:
	29-JUL-82			UDA # 1
CHK'D.	DATE	BOARD LOCATION:		
		SHEET 14 OF 15		

DSK:UDAITE.T2P[4,50] 29-JUL-82 12:56 NEXT HIGHER ASSEMBLY: B-DD-M7161-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7161-0-UDA1	E

TEST COND 2 H	3-A6,R	7-A5,R	7-C7,L			
TEST COND 3 H	3-B5,R	7-A5,R	7-C7,L			
TEST TRUE H	3-D5,R	6-B7,L				
TIME ERR L	5-B4,R	5-C5,L				
TIMEOUT L	5-B4,L	5-D7,R				
TMSYN H	9-B4,L	10-A4,L				
U TIMEOUT H	5-C5,L	5-C7,R				
UA00 H	8-B6,R	8-C6,R	9-D7,L			
UA01 H	8-B6,R	8-C6,R	9-A7,L	10-A3,R		
UA02 H	8-B6,R	8-C6,R	9-A7,L	10-A3,R		
UA03 H	8-B6,R	8-C6,R	9-A7,L	9-B4,L		
UA04 H	8-B6,R	8-C6,R	9-A7,L	9-B4,L		
UA05 H	8-B6,R	8-C6,R	9-B4,L	9-B7,L		
UA06 H	8-B6,R	8-C6,R	9-B7,L	9-C4,L		
UA07 H	8-B6,R	8-C6,R	9-B7,L	9-C4,L		
UA08 H	8-B6,R	8-C6,R	9-B7,L	9-C4,L		
UA09 H	8-A6,R	8-C6,R	9-B5,L	9-D7,L		
UA10 H	9-B5,L	9-D7,L				
UA11 H	9-B5,L	9-C7,L				
UA12 H	9-C5,L	9-C7,L				
UA13 H	9-C5,L	9-C7,L				
UA14 H	9-C5,L	9-C7,L				
UA15 H	9-C5,L	9-C7,L				
UA16 H	9-C4,L	11-D3,L				
UA17 H	9-B5,L	11-D3,L				
UBMASTER L	3-D6,R	8-D3,R	10-C1,L			
UDATARDY H	3-D6,R	10-A5,L				
UPROC H	2-D4,L	3-C7,R	4-A8,R	5-C7,R	5-D7,R	8-B4,R
UPROC L	2-A8,R	2-C4,L	3-A7,R	3-B5,R	5-B7,R	5-C7,R
UTEST H	3-C6,R	10-C5,L				
WRTX0.INIT L	10-D5,L					
WRTX0.RUN L	10-D5,L					
WRTX2.INIT L	10-A8,R	10-D5,L				
WRTX2.RUN L	10-D5,L					
XFER L	10-A6,R					

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 20-JUL-82	ENG.	DATE	TITLE: UDA # 1
CHK'D.	DATE	BOARD LOCATION: SHEET 15 OF 15		
DSK:UDA1E.T2P[4,50]	20-JUL-82 12:56	NEXT HIGHER ASSEMBLY:		SIZE K CODE CS NUMBER M7161-0-UDA1 REV. E
FIRST USED ON OPTION/MODEL: UDA		B-DD-M7161-0		

SIZE	CODE	NUMBER	REV.
B	DD	M7162-0	C

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
G-DD-M7162-0	-	M7162-00	DRAWING DIRECTORY	B C
K-PL-M7162-0-DBP	3		PARTSLIST DATA BASE	B C
D-UA-M7162-0-0	2		UNIT ASSEMBLY	B C
K-PC-M7162-0-DBC	-		P.C. DATA BASE	B C
K-CS-M7162-0-DBS	-		SUDS DATA BASE	B C
K-CS-M7162-0-UDA2	13		CIRCUIT SCHEMATIC	B C
		5014921-00	P.C. ETCH BOARD	B C
E-EC-5014921-0-0	3		ETCH CUT DRAWING	B C
D-MD-5014921-0-0	6		DRILL & ETCH DRAWING	B C

NOTES:

REVISIONS			
REV.	B	C	
CHG NO.	INIT	M7162-C001/A	
DATE	18 May 81	28 APR 82	

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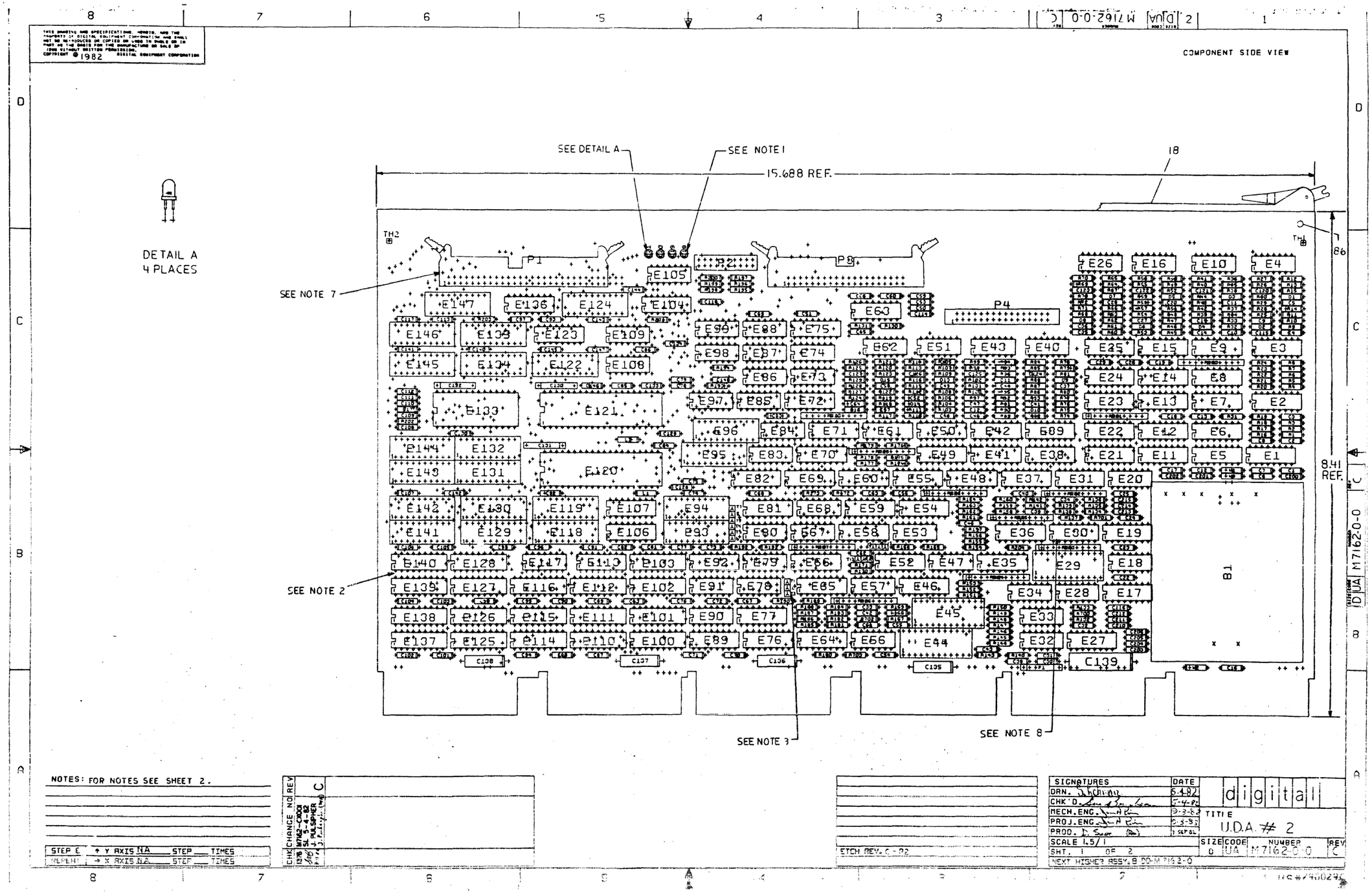
digital

USED ON OPTION/MODEL				
DRN. S. Lehman	4-14-82	TITLE UDA # 2		
CHK'D M Landy	20 APR 82			
ENG.	9-3-82	SIZE B	CODE DD	NUMBER M7162-0 REV. C
PROD D. SWIFT (RPM)	7 SEP 82	SHEET 1 OF 1		

DRB 126


COMPONENT SIDE VIEW
SEE DETAIL A
SEE NOTE 1
15.688 REF.
18
DETAIL A
4 PLACES
SEE NOTE 7
SEE NOTE 2
SEE NOTE 3
SEE NOTE 8
8.41 REF.
P1
P2
P3
P4
B1
NOTES: FOR NOTES SEE SHEET 2.
STEP E ↑ Y AXIS NA STEP ___ TIMES
REPEAT → X AXIS NA STEP ___ TIMES
CHK CHANGE NO REV
1376 M7162-C0001 SL 5-4-82 J. PULSIPHER
C
ETCH REV. C - P2
SIGNATURES DATE
DRN. 5-4-82
CHK'D. 5-4-82
MECH. ENG. 9-3-82
PROJ. ENG. 9-3-82
PROD. 1 SEP 82
SCALE 1.5/1
SHT. 1 OF 2
NEXT HIGHER ASSY. B DD-M7162-0
digital
TITLE
U.D.A. # 2
SIZE 0 CODE UA NUMBER M7162-0-0 REV C
M7162-0-0
DUA

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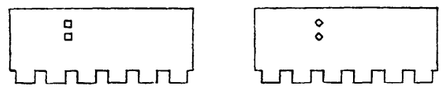
NOTES:

1. D18, D19, D20 & D21 TO BE MOUNTED ON COMPONENT SIDE, LONGER LEG TO LEFT. LEAVE LEADS APPROX. .18" LONG IN ORDER TO BEND OVER AS SHOWN.
2. PLEASE FOLLOW CMOS HANDLING PROCEDURES WHEN INSTALLING E100-E103, E110-E112, E114-E116, E125-E128, E137-E140. = VERY IMPORTANT=
3. PINS T1-T15 (1210385-01) MUST BE INSTALLED ON BOARD WITH SIDES PARALLEL TO EDGES OF BOARD.



THIS NOT THIS

JUMPERS W4—W8 (1214314-00) ARE INSTALLED AS FOLLOWS:

JUMPER W4—PINS T1 & T2
JUMPER W5—PINS T4 & T5
JUMPER W6—PINS T7 & T8
JUMPER W7—PINS T11 & T12
JUMPER W8—PINS T13 & T14

4. THE FOLLOWING ARE SPARES ON THE BOARD. THEY CAN BE USED FOR ADDING COMPONENTS TO THE CIRCUIT: E27, E24, E1, E5, E11, E17, E18, E19, E20, E21, E6, E12, E22, E63, E89, E124, E146, C50, C53, C59, C114, C200-C206, C210-C215. C21-NOT USED
5. THE FOLLOWING ARE EXTRA ECL DATA BUS TERMINATION RESISTORS WHICH CAN BE USED TO "TWEAK" THE ECL LINES IF NECESSARY: R172, R177, R178, R179, R142, R158, R159, R164, R163, R162, R160, R161, R22, R5, R23, R24.
6. RESISTORS R204, R700, R701, R702, R703 APPEAR ON SHEET 1 OF THIS DOCUMENT, BUT ARE NOT IN SEQUENTIAL ORDER.
7. CONNECTOR P1 (1216832-03) TO BE MOUNTED ON COMPONENT SIDE WITH PIN 1 TO THE FAR LEFT.
8. MOUNT ITEM 83 (E30, E37, E48, E52, E54, E64) FLUSH WITH BOARD.

REVISION HISTORY		
DATE	ECO NUMBER	REV.

TITLE U.D.A. NO. 2

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV.
D	UA	M7162-0-0	C
SCALE		SHEET 2 OF 2	

DRD 138A

AUTOMATED BY PRTLST.3P(44) P A R T S L I S T SHEET A1 OF A3

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5014921-0-0	5014921-00	DRILL AND ETCH BRD.	1	
2	2		1212385-00	*** THIS ITEM IS NOT USED ***	-	
3	3		1012784-00	.047 MFD 50V +80-20% CER	124	C1-C5,C7-C15,C17-C20,C22-C49,
						CONT C51,C52,C54-C58,C60-C113,
						CONT C115-C118,C128,C129,C133,C134,
						CONT C140-C148
4	4		1013466-09	1000.0 MMF 50V 10% X7R CER	2	C6,C16
5	5		1013466-11	.22 MFD 50V +80-20% Z5U CER	3	C130,C131,C132
6	6		1015878-00	.01 MFD 50V +80-20% CER	8	C120-C127
7	7		1016549-00	47 MFD 10V +50-10% AL EL	4	C135-C138
8	8		1104860-00	1N 746A VZ= 3.3 5%	8	D6,D2,D14,D10,D8,D4,D16,D12
9	9		1105275-00	D 672 TR= 15NS PIV= 60V SI	8	D5,D1,D13,D9,D7,D3,D15,D11
10	10		1110836-00	1N 759A VZ= 12.0 5% .40W	1	D17
11	11		1112689-00	LED .8MCD@16MA VF=5V	4	D18-D21
12	12		1205747-00	FUSE, SUB-MINI, 5.000A, 125V, A	1	F1
13	13		1210385-01	PIN 1POS WIRE WRAP	15	T1-T15
14	14		1212965-04	PCB,HEADER 20PIN(2X05).100CC 90D	1	P2
15	15		1214314-00	CONN,P+S 02SKT(1X02).100CC JUM	5	W4-W8
16	16		1216832-02	PCB,HEADER 40POS(2X20).100CC 90D	1	P3
17	17		1216832-03	PCB,HEADER 50POS(2X25).100CC 90D	1	P1
18	18		1216988-02	HANDLE,MODULE,HEX TWO EJECTORS	1	
19	19		1218348-00	PCB,HEADER 32PIN(2X16).100CC 90D	1	P4
20	20		1300202-00	47.0 .25 W 5.0 % CC	16	R16,R43,R29,R32,R45,R58,R61,R72,
						CONT R82,R87,R89,R101,R103,R111,R110,
						CONT R128
21	21		1300247-00	120.0 .25 W 5.0 % CC	16	R156,R141,R135,R187,R183,R185,
						CONT R153,R150,R182,R192,R155,R170,
						CONT R700,R701,R702,R703
22	22		1300271-00	220.0 .25 W 5.0 % CC	8	R52,R15,R109,R81,R67,R38,R123,
						CONT R96

REVISION HISTORY			BASIC PART NO: M7162	DRN: S. BOURBEAU	DATE: 20-JAN-81	D I G I T A L
ENG	ECO NUMBER	REV	SECTION A OF A			
	INITIAL	P	SECTION.VARIATION INDEX	CHK'D: R. MICHAUD	DATE: 20-JAN-81	TITLE PARTS LIST
AP	M7162-CX001	C	[A] 00			UDA # 2
			[B]			
			[C]	DES.ENG: J. PULSIPHER	DATE: 20-JAN-81	
			[D]			
			[E]			DOCUMENT NUMBER
			[F]	RESP.ENG.: B. MATHRANI	DATE: 20-JAN-81	
			[H]			SIZE CODE NUMBER REV
			[J]			
			[K]	MFG.ENG.: D. SWIFT	DATE: 20-JAN-81	K PL M7162-0-DBP C
			[L]			
			[M]	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME: EDIT #
			[N]	D-UA-M7162-0-0	#B-DD-M7162-0	Z1770C.PLS 21

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LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
23	23		1300316-00	470.0 .25 W 5.0 % CC	12	R201,R190,R189,R6,R21,R174,R173,
					CONT.	R1,R7,R8,R176,R175.
24	24		1300365-00	1.0 K .25 W 5.0 % CC	1	R194
25	25		1300432-00	3.0 K .25 W 5.0 % CC	1	R203
26	26		1300479-00	10.0 K .25 W 5.0 % CC	1	R193
27	27		1301477-00	82.0 .25 W 5.0 % CC	5	R202,R3,R20,R19,R18
28	28		1302379-00	75.0 .25 W 5.0 % CC	8	R131,R130,R198,R199,R200,R197,
					CONT	R196,R195
29	29		1302873-00	261.0 .25 W 1.0 % RN55D-F10	8	R132,R204,R147,R144,R148,R149,
					CONT.	R165,R140
30	30		1302887-00	130.0 .25 W 1.0 % RN55D-F10	4	R2,R4,R17,R31
31	31		1303036-00	56.20 .25 W 1.0 % RN55D-F10	32	R56,R50,R55,R49,R27,R13,R26,R12,
					CONT.	R114,R107,R113,R105,R85,R79,R84,
					CONT	R78,R70,R65,R69,R64,R41,R36,R40,
					CONT	R35,R126,R121,R125,R120,R99,R94,
					CONT	R98,R93
32	32		1304863-00	316.0 .25 W 1.0 % RN55D-F10	32	R57,R51,R54,R48,R28,R14,R25,R11,
					CONT	R115,R108,R112,R106,R86,R80,R83,
					CONT	R77,R71,R66,R68,R63,R42,R37,R39,
					CONT	R34,R127,R122,R124,R119,R100,
					CONT	R95,R97,R92
33	33		1311522-00	200.0 .25 W 5.0 % CC	16	R157,R136,R139,R188,R186,R184,
					CONT	R152,R131,R151,R154,R171,R191,
					CONT	R133,R137,R167,R180
34	34		1312114-01	R NETWORK 8-470 5.0 % 10PIN	11	R300-R310
35	35		1312929-00	62.0 .25 W 5.0 % CC	8	R47,R10,R104,R76,R62,R33,R118,
					CONT	R91.
36	36		1318341-01	162.0 .25 W 1.0 % RN55D-F10	8	R169,R168,R143,R166,R134,R138,
					CONT.	R146,R145
37	37		1318341-02	187.0 .25 W 1.0% RN55D-F100	16	R44,R46,R30,R9,R73,R60,R59,R53,
					CONT	R102,R90,R88,R74,R129,R117,R115,
					CONT	R75
38	38		1617533-00	DELAY= 250NS,5TAPS 14PIN DIP	1	E97
39	39		1618336-00	DELAY= 10NS	4	E28,E57,E34,E56
40	40		1618337-00	DELAY= 18NS	2	E53,E33
41	41		1618343-00	PULSE XFMR,RATIO 1:1:1, 80UH	8	E4,E16,E40,E51,E10,E26,E43,E62
42	42		1618345-00	DELAY= 14NS	2	E47,E32
43	43		1910534-00	74S04 INVERTER GATE-HEX 1I	2	E108,E84
44	44		1910544-00	74S74 FF-D DUAL,EDGE TRIGG	6	E99,E85,E98,E79,E90,E105
45	45		1910545-00	74S112 FF-JK DUAL,EDGE TRIG	1	E76
46	46		1910956-00	74S151 MUX 1 OF 8	1	E69
47	47		1910957-00	74S175 FF-D QUAD COMMON CLO	2	E81,E92
48	48		1911399-00	10102 NOR GATE,QUAD 2IN	4	E8,E23,E49,E70
49	49		1911401-00	10104 AND GATE,QUAD 2IN	1	E31
50	50		1911404-00	10107 XOR/NOR GATE,3-2IN	1	E35
51	51		1911414-00	10124 TTL TO ECL TRNSLTR	3	E60,E59,E65
52	52		1911415-01	10125 ECL TO TTL TRANSLATE	2	E66,E58
53	53		1911420-00	10174 DUAL 4 TO 1 MUX	2	E36,E46

TITLE	SECTION A OF A
UDA # 2	

SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7162-0-DBP	C

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER		DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
54	54		1911573-00		74S280 PARITY GEN/CHKR,9BIT	2	E91,E117
55	55		1911712-00		74S51 AND-OR GATE-INVERT D	2	E74,E73
56	56		1912096-00	DEC	74S86 XOR GATE,QUAD 2IN	1	E80
57	57		1912389-00		74S08 AND GATE-QUAD 2IN,PO	1	E83
58	58		1912746-00	DEC	74S37 NAND GATE-QUAD 2IN	1	E87
59	59		1912801-00		LS02 NOR-GATE-QUAD 2IN	1	E109
60	60		1912816-00		LS32 OR GATE-QUAD 2IN,POS	1	E88
61	61		1912820-00		LS51 A-O-I GATE 2-WIDE 2I	1	E86
62	62		1912833-00		LS109 FF-JK DUAL,POS EDGE	1	E75
63	63		1912847-00		LS157 MUX 1 OF 2(QUAD)	1	E113
64	64		1912848-00		LS158 MUX 1 OF 2 (QUAD)	1	E104
65	65		1912853-00		LS175 FF-D QUAD	1	E123
66	66		1912860-00		LS259 LATCH 8BIT	1	E136
67	67		1912863-00		LS273 FF-D OCTAL W/CLEAR	3	E147,E94,E95
68	68		1912864-00		LS279 LATCH,QUAD-S-R	1	E72
69	69		1913340-00		74S32 OR GATE-QUAD 2IN	2	E78,E67
70	70		1913493-01		74S241J OCTAL BUFFER,TRI-STA	4	E131,E132,E143,E144
71	71		1913671-00		74S374 FF-D OCTAL TRISTATE	4	E141,E129,E142,E130
72	72		1913939-00		LS191 COUNTER,SYNCHR. UP/D	2	E106,E107
73	73		1914082-01		74S163 COUNTER,SYNCH,UP/DOW	2	E77,E82
74	74		1914214-00		LS374 FF-D OCTAL EDGE TRIG	6	E135,E134,E145,E118,E119,E93
75	75		1915193-00		LS244 DRIVER,LINE,OCTAL,T	2	E96,E122
76	76		1916574-00		10114 RECEIVER,LINE,TRIPL	8	E15,E71,E3,E38,E25,E55,E9,E41
77	77		1917043-00	DC	018 SERIALIZER-DESERIALIZ	2	E120,E121
78	78		1917277-00		100131 FF-D TRIPLE	1	E44
79	79		1917289-00		100102 OR/NOR GATE,QUINT,2	2	E45,E29
80	80		1917839-00		10192 LINE DRIVER,QUAD DIF	8	E2,E14,E42,E61,E7,E13,E39,E50
81	81		1917956-00		74LS280N PARITY GEN/CHK,9BIT	1	E68
82	82		1918352-00	PS	4317 DC-DC CONVERTER	1	B1
83	83		1918353-00		10231 FF-D MASTER-SLAVE	6	E30,E52,E64,E37,E48,E54
84	84		2115102-00	DEC	DC309 NMOS CUSTOM LSI FOR	1	E133
85	85		2117498-02		6147P RAM,4KX1,STATIC,55NS	18	E101,E110,E114,E140,E139,E138,
						CONT	E137,E111,E115,E100,E128,E127,
						CONT.	E126,E125,E102,E103,E116,E112
86	86		9000024-01		EYELET,ROLLED 0.121DDX0.192	12	
87	87		9009185-00		JUMPER, WIRE, INSULATED, BLACK B	3	W1-W3
88	88		1611257-01		CHOKE(CERAMIC BEAD)AXIAL LEAD,ON	2	L1,L2
89	89		9105740-55		*** THIS ITEM IS NOT USED ***	-	
90	90		9009157-00		*** THIS ITEM IS NOT USED ***	-	
91	91		4901259-00		*** THIS ITEM IS NOT USED ***	-	
92	92		9107256-11		*** THIS ITEM IS NOT USED ***	-	
93	93		1001796-00		50 MFD 25V +75-10% AL EL	1	C139

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							UDA # 2	

SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7162-0-DBP	C

P1
DBUS 15 H
DBUS 14 H
DBUS 13 H
DBUS 12 H
DBUS 11 H
DBUS 10 H
DBUS 09 H
DBUS 08 H
DBUS 07 H
DBUS 06 H
DBUS 05 H
DBUS 04 H
DBUS 03 H
DBUS 02 H
DBUS 01 H
DBUS 00 H
SET IOC H
IOC SEL 2 H
IOC SEL 1 H
IOC SEL 0 H
CLK DIOC L
RESET L
LD DCR L
LD RTCS L
RD RTDS L

8 D FLOP 74LS273 E147
DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
RESET L
LD DCR L
DRV SEL 0 H
DRV SEL 1 H
DRV SEL 2 H
DRV SEL 3 H
EN RAM PE H

8 BIT LATCH 74LS259 E136
IOC SEL 2 H
IOC SEL 1 H
IOC SEL 0 H
SET IOC H
DTEST H
RSGEN EN L
CMD OUT L
DI/O CLR L
SERDES ENABLE H
RD MODE H
ECC ENABLE H
ECC TIME H

CLK DIOC L
74S08 E83
74LS32 E88
SERDES10 EN H

74S04 E108
74S04 E84
DIAG MODE L
DIAG MODE H

DRIVE CONTROL REGISTER
8 D FF 74LS374 E135
+5.0V
R194 1KΩ
ODD PRTY H
DIAG CLK H
DIAG DATA H
LED 1 L
LED 2 L
LED 4 L
LED 8 L
D20
D21
D19
D18

NOTE: UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 1/4W, 5%.

+15.0V
R202 82Ω
C109 47nF 50V
D17 1N759A 12V 5% .4W
+12.0V

+5.0V
RVCC1 R201 470Ω
RVCC2 R190 470Ω
RVCC3 R189 470Ω
C135 47μF 10V
C136 47μF 10V
C137 47μF 10V
C138 47μF 10V
GND

R198 75Ω
P3
LD SERDES L
LD BUFFER L
RD BUFFER L
RD SERDES L
LD DBAR L
RD ECC RSDU L
LD UBAR L
CLK SERDES H
CLK ENB H
CLK BDR H
R131 75Ω
RECV ERROR H
DLY UPROC H
DTEST H
R199 75Ω
74LS32 E88
DATA WORD CLK L
RTDS RCVD H
R130 75Ω
OVERRUN H
R200 75Ω
R197 75Ω
R196 75Ω
R195 75Ω
RAM PE L
ECC RDY H
RTCS RDY H
DATA RDY H

BUS BG7 IN H → BUS BG7 OUT H
BUS BG6 IN H → BUS BG6 OUT H
BUS BG5 IN H → BUS BG5 OUT H
BUS BG4 IN H → BUS BG4 OUT H
BUS NPG IN H → BUS NPG OUT H

CLK BDR H → 74S04 E108 → CLK BDR L
DLY UPROC H → 74S04 E108 → DLY UPROC L

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REVISIONS		
CHK	CHANGE NO.	REV
376	M7162-CX001	
WS	9-15-82	
JP	PUBSPHER	C

digital

DRN: QD Doherty
CHK: D.
DATE: 14-SEP-82
ENG.
DATE
BOARD LOCATION:
SHEET 1 OF 16
PS1:<DOUGHERTY>UDA2C1.DRW;14-SEP-82 17:39
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA
8-DD-M7162-0

TITLE: UDA # 2

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

REV. C
NUMBER M7162-0-UDA2
CODE CS
SIZE K
B

BUFFER MEMORY

HIPRTY OUT H — RAM 15 H — RAM 14 H — RAM 13 H — RAM 12 H — RAM 11 H — RAM 10 H — RAM 09 H — RAM 08 H

HIPRTY IN H

LOPRTY OUT H — RAM 07 H — RAM 06 H — RAM 05 H — RAM 04 H — RAM 03 H — RAM 02 H — RAM 01 H — RAM 00 H

LOPRTY IN H

4K X 1 RAM 6147 E101 / E110 / E114 / E140 / E139 / E138 / E137 / E111 / E115

4K X 1 RAM 6147 E100 / E128 / E127 / E126 / E125 / E102 / E103 / E116 / E112

BA00 H … BA11 H — A0 … A11 — DIN DOUT — WREN ENO

RVCC1

DLY UPROC L — CLK BDR L — UPROC L — LD BUFFER L — DLY UPROC H — CLK BDR L — UPROC H — LD BUFFER L

74LS32 E88 — 74LS109 E75 — INC UBAR H — INC DBAR H

UPROC L — UPROC H — 74S51 E74 — 74S04 E108 — READ L — READ H

CLK ENB H — READ L — READ H — RVCC1 — 74S37 E87 — 74S51 E74 — RAM WE L — RAM CS L

BUFFER SELECT

DLY UPROC L — CLK BDR L — 74S74 E98 — UPROC H — UPROC L

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. | DATE | ENG. | DATE | TITLE: UDA # 2

CHK'D. | DATE | BOARD LOCATION: | SHEET 4 OF 16

PS:<DOUGHERTY.UDA2C4.DRN] 14-SEP-82 17:39 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0

FIRST USED ON OPTION/MODEL: UDA

SIZE K | CODE CS | NUMBER M7162-0-UDA2

SERDES AND ECC

NRZ DATA IN H
NRZ CLK OUT H

SERDES DC018 E120
RD SERDES L
RD MODE H
LD SERDES L
CLK SERDES H
CMD OUT L
SERDES ENABLE H
SDO16/10 H
L1 36 Ω @ 1.0MHZ CERAMIC BEAD CHOKE
DATA WORD CLK L
DATA RDY H
OVERRUN H
RVCC1
74S74 E85
NR2 DATA OUT H

4-BUF DRIVERS 74S241 E131
4-BUF DRIVERS 74S241 E144
4-BUF DRIVERS 74S241 E143
4-BUF DRIVERS 74S241 E132
I/O 03 H
I/O 02 H
I/O 01 H
I/O 00 H
I/O 07 H
I/O 06 H
I/O 05 H
I/O 04 H
I/O 11 H
I/O 10 H
I/O 09 H
I/O 08 H
I/O 15 H
I/O 14 H
I/O 13 H
I/O 12 H
DBUS 12 H
DBUS 13 H
DBUS 14 H
DBUS 15 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
DBUS 08 H
DBUS 09 H
DBUS 10 H
DBUS 11 H
DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H
RD SERDES L

SERDES DC018 E121
RD ECC L
WRT ECC L
LD ECC L
STROBE ECC H
DATA OUT L
SERDES10 EN H
RVCC1
SDO16 H
SDO10 H
L2 36 Ω @ 1.0MHZ CERAMIC BEAD CHOKE
ECC SYMBOL CLK L
QUAD BUFFER 74LS244 E96
QUAD BUFFER 74LS244 E122
ECC OUT 8 H
ECC OUT 9 H
ECC OUT 0 H
ECC OUT 1 H
ECC OUT 2 H
ECC OUT 3 H
ECC OUT 4 H
ECC OUT 5 H
ECC OUT 6 H
ECC OUT 7 H
WRT ECC L
+5.0V
R203 3KΩ
ECC SYMBOL L
R193 10KΩ

R-S GEN DC389 E133
RSGEN CLK L
ECC FDBCK EN H
ECC INPUT EN H
ECC CLR L
ECC OUT 9 H
ECC OUT 8 H
ECC OUT 7 H
ECC OUT 6 H
ECC OUT 5 H
ECC OUT 4 H
ECC OUT 3 H
ECC OUT 2 H
ECC OUT 1 H
ECC OUT 0 H

8 D FF 74LS374 E134
8 D FF 74LS374 E145
DTEST H
SERDES ENABLE H
WRT ECC L
RD ECC RSDU L
STROBE ECC H

P2
GND
NR2 CLK OUT H
ECC FDBCK EN H
ECC INPUT EN H
RSGEN CLK L
DATA WORD CLK L
LED 1 L
LED 2 L
LED 4 L
LED 8 L
CLK BDR L
SDO16/10 H
SDO16 H
NR2 DATA IN H
DATA RDY H
GND

■ NOTE: PIN 20 IS ACTUALLY EFL GROUND.

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE	ENG.	DATE	TITLE:
CHK'D.	14-SEP-82			UDA # 2

PS:<DOUGHERTY.UDA2C5.DRW>14-SEP-82 17:40 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0 | BOARD LOCATION: | SHEET 5 OF 16

FIRST USED ON OPTION/MODEL: UDA | SIZE K | CODE CS | NUMBER M7162-0-UDA2 | REV. C

RTDS
(REAL TIME DRIVE STATUS)

RTCS
(REAL TIME CONTROLLER STATUS)

RVCC2
74S86 E80
RTDS PE H
RTDS CLK H
CLR PTY L
74S74 E90
4 D FF 74S175 E81
RTDS DATA H
RTDS DATA 1 L
RTDS DATA 2 L
RTDS DATA 3 L
4 D FF 74S175 E92
RTDS DATA 4 L
RTDS DATA 5 L
RTDS DATA 6 L
74S32 E78
QUAD BUFFER 74LS244 E96
DATA XMIT ERROR H
RTCS RDY H
RTDS RCVD H
RECV ERROR H
DBUS 07 H
DBUS 02 H
DBUS 03 H
DBUS 08 H
8 D FF 74LS374 E93
ATTENTION H
R/W RDY H
SECTOR PULSE H
RECEIVER RDY H
INDEX PULSE H
AVAILABLE
RD RTDS L
DBUS 01 H
DBUS 15 H
DBUS 04 H
DBUS 00 H
DBUS 05 H
DBUS 06 H
BIN CTR 74S163 E77
74S04 E84
SYNCH DET H
74S112 E76
CLR PTY L
74LS279 E72
RTDS RCVD H
BIN CTR 74S163 E82
74S32 E67
74S04 E84
RTCS CLK H
8 MUX 74S151 E69
RCVR RDY
WRT GATE
RD GATE
INIT
RESERVED
RESERVED
PARITY
SEL
EN
WRC L
RTCS DATA H
8 D FLOP 74LS273 E94
8 D FLOP 74LS273 E95
DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
RVCC2
LD RTCS L
74S08 E83
RTCS RDY H
PARITY GEN 74LS280 E68
FEVEN
FODD
EVEN PARITY H
DATA PULSE ERROR L
DATA XMIT ERROR H
REAL TIME PULSE ERROR L
RECV ERROR H
RTDS PE H
SYNCH DET H
DI/O CLR L

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 14-SEP-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION:	
		SHEET 5 OF 16	

TITLE: UDA # 2

PS:<DOUGHERTY>UDA2C6.DRW|14-SEP-82 17:48|NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA | B-DD-M7162-0

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

WCD ENCODER
(WRITE/COMMAND DATA)

DIAG CLK H
NR2 CLK OUT H
DIAG MODE L
NR2 DATA OUT H
DIAG DATA H
DIAG MODE H
10124 E59
10124 E60
10124 E59
10124 E59
R133 200Ω
R700 120Ω
R701 120Ω
R137 200Ω
-5.2V

DRV SEL 0 H
DRV SEL 1 H
DRV SEL 2 H
DRV SEL 3 H
RVCC3
10124 E65
DRV SEL0 T L
DRV SEL1 T L
DRV SEL2 T L
DRV SEL3 T L
R303 470Ω
-5.2V

00102 E29
E28 10nS
E34 10nS
WCDDL2
WCDDL1
R138 162Ω 1%
R134 162Ω 1%
R303 470Ω
R303 470Ω
R132 261Ω 1%
R204 261Ω 1%
-5.2V

10231 E30
10231 E30
R135 120Ω

WRAP H
WCD P1 H
WCD P2 L
WCD P2 H

R156 120Ω
R141 120Ω
2X4 MIX 10174 E36
D00 D01 D02 D03
D10 D11 D12 D13
B0 B1
SEL EN
R3 82Ω
R20 82Ω
R2 130Ω 1%
R4 130Ω 1%
HI WCD H
LO WCD H
-5.2V

WCD NEW DATA H
WCD DLY DATA H

R302 470Ω
R157 200Ω
R135 200Ω
R139 200Ω
R305 470Ω
R305 470Ω
-5.2V

NOTE: R302,R303, AND R305 ARE
10 PIN SIPS WITH PINS 1 AND 10
CONNECTED TO -5.2V.

RRD DECODER
(READ/RESPONSE DATA)

HIGH H
RRD H
100131 E44
10107 E35
E47 14nS
E53 18nS
R146 162Ω 1%
R147 261Ω 1%
-5.2V

10231 E52
R187 120Ω
R183 120Ω
R185 120Ω
R188 200Ω
R186 200Ω
R184 200Ω
R144 261Ω 1%
R145 162Ω 1%
-5.2V

10125 E66
T1 T2 W4
NR2 CLK OUT H
SWEEP FREQ H
T3 (USE ONLY WITH PULSED FUNCTION GENERATOR OR DIAG CLK H)
10125 E66
NR2 DATA IN H

NOTE: R302,R303, AND R305 ARE
10 PIN SIPS WITH PINS 1 AND 10
CONNECTED TO -5.2V.

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 14-SEP-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION: SHEET 2 OF 16	

PS:<DOUGHERTY>UDA2C2.DRW;14-SEP-82 12:41

FIRST USED ON OPTION/MODEL: UDA	B-DD-M7162-0	NEXT HIGHER ASSEMBLY:	SIZE K	CODE CS	NUMBER M7162-0-UDA2 REV. C

TITLE: UDA # 2

RTCS ENCODER
(REAL TIME CONTROLLER STATE)

HIGH H

NOTE 1. REFERENCE SDI TECHNICAL REPORT.

SWEEP FREQ H
RTCS CLK H
DIAG MODE L
RTCS DATA H
DIAG MODE H

10124 E59
10124 E60
10124 E60
10124 E59

R167 200Ω
R702 120Ω
R703 120Ω
R180 200Ω
-5.2V

00102 E45
00102 E45
00102 E45
00102 E45

E57 10ns
E56 10ns

R169 162Ω 1%
R168 162Ω 1%
R306 470Ω
R306 470Ω
R148 261Ω 1%
R149 261Ω 1%

NOTE: R304 AND R306 ARE 10 PIN SIPS WITH PINS 1 AND 10 CONNECTED TO -5.2V.

10231 E64
R182 120Ω

RTCS P2 H
RTCS P2 L
RTCS P1 H

2X4 MIX 10174 E46
D00 D01 D02 D03
D10 D11 D12 D13
1 SEL
EN

R150 120Ω
R153 120Ω

HI RTCS H
LO RTCS H

R19 82Ω
R18 82Ω
R31 130Ω 1%
R17 130Ω 1%

RTCS NEW DATA H
RTCS DLY DATA H

R152 200Ω
R181 200Ω
R151 200Ω
R304 470Ω
R304 470Ω

RTDS DECODER
(REAL TIME DRIVE STATE)

NOTE: ALL DELAY LINES ON THIS SHEET HAVE PINS 8 AND 14 CONNECTED TO -5.2V.

HIGH H
RTDS H

100131 E44 (MS SET MR CLR)
10107 E35
E32 14ns
E33 10ns

R140 261Ω 1%
R143 162Ω 1%
R192 120Ω
10231 E52

R155 120Ω
R170 120Ω
R154 200Ω
R171 200Ω
R191 200Ω
R165 261Ω 1%
R166 162Ω 1%

10125 E58
10125 E66
10125 E66

T4 T5 T6 T14 T13 T10 T12 T11 T7 T8 T9 T15
W5 W8 W7 W6

RTCS CLK H
DIAG CLK H
SWEEP FREQ H
RTCS CLK H
RTDS DATA H
RTCS DATA H

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REVISIONS		
CHK	CHANGE NO.	REV

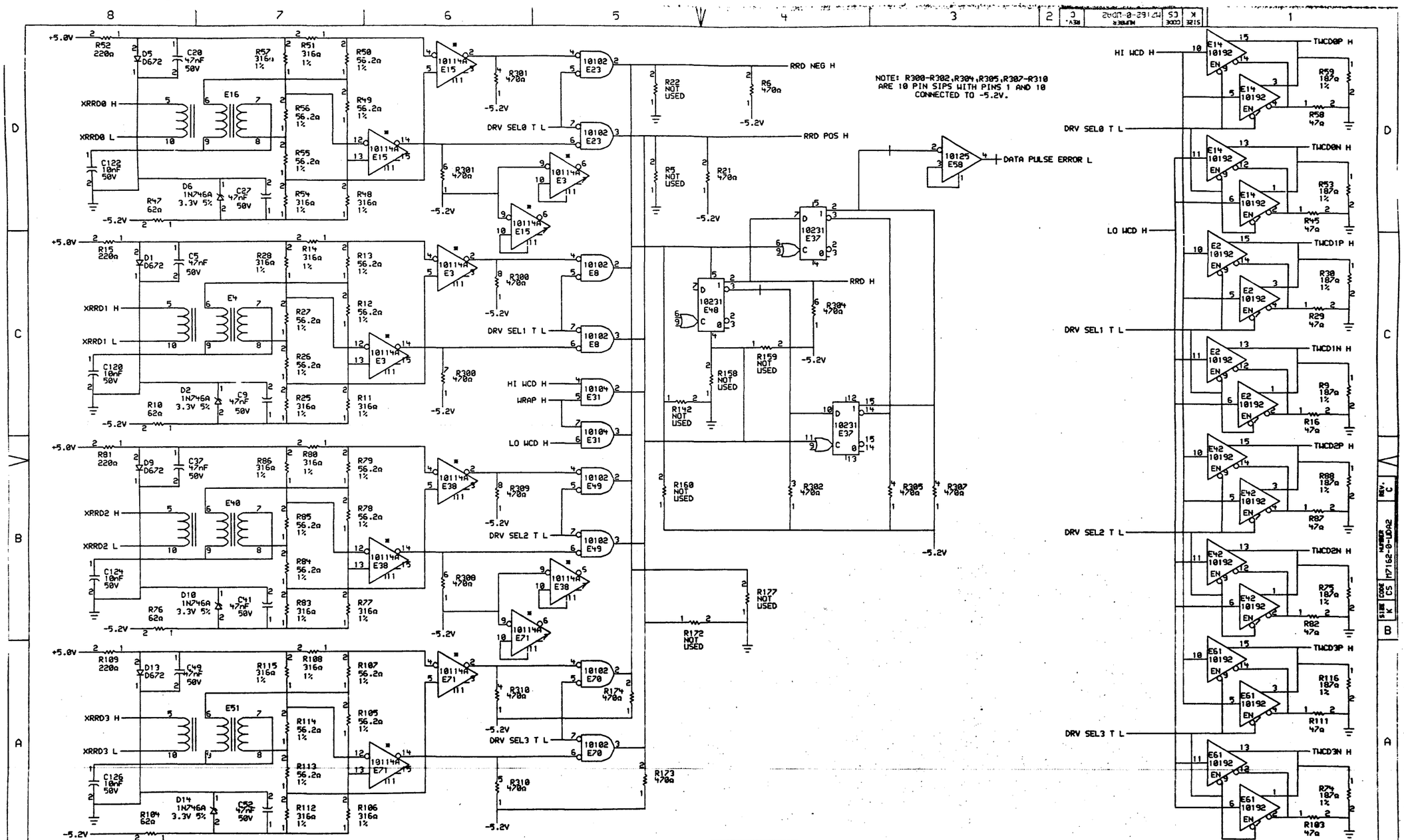
digital

DRN.	DATE	ENG.	DATE	TITLE:
CHK'D.	14-SEP-82 DATE		DATE	UDA # 2

BOARD LOCATION:
SHEET 8 OF 16

PS:<DOUGHERTY>UDA2C8.DRW;14-SEP-82 17:41 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0 | FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE	ENG.	DATE	TITLE: UDA # 2
CHK'D.	DATE	BOARD LOCATION: SHEET 9 OF 16		

PSI:<DOUGHERTY>UDA2C9.DRW;14-SEP-82 17:42 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

NOTE: R300,R301,R304,R305,R307-R310 ARE 10 PIN SIPS WITH PINS 1 AND 10 CONNECTED TO -5.2V.

REVISIONS		
CHK	CHANGE NO.	REV

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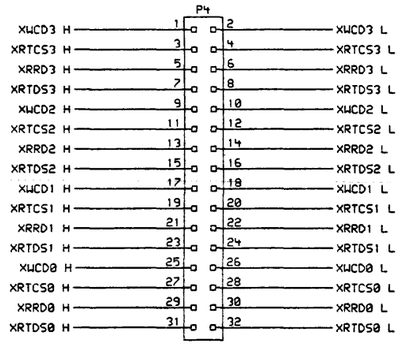
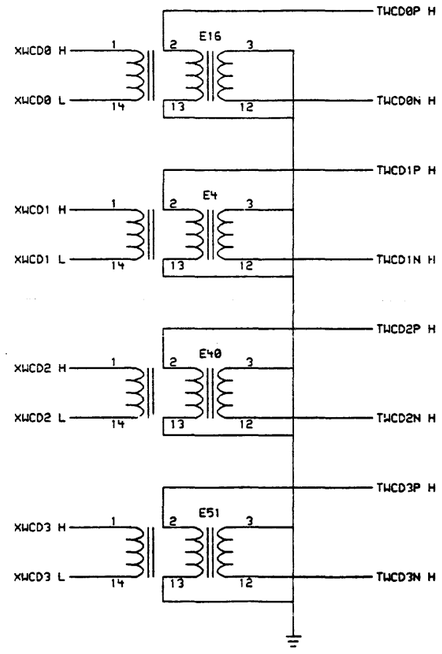
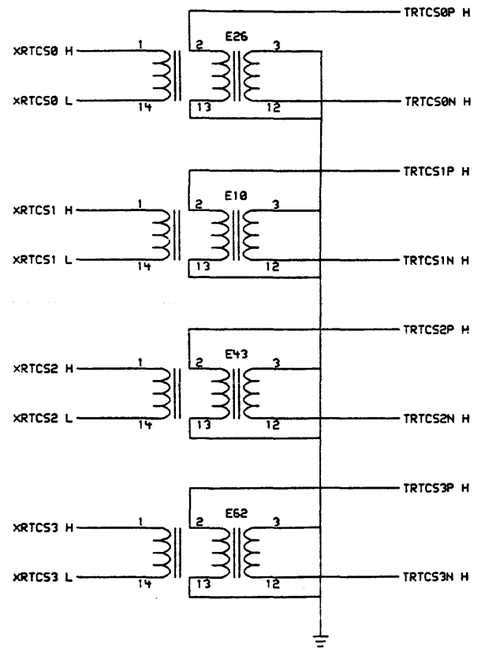
digital	DRN.	DATE 14-SEP-82	ENG. / DATE
	CHK'D.	DATE	BOARD LOCATION:
			SHEET 10 OF 16
PS:<DOUGHERTY>UDA2CA.DRW;14-SEP-82 12:42	NEXT HIGHER ASSEMBLY: B-DD-M7162-0		
FIRST USED ON OPTION/MODEL: UDA			

TITLE: UDA # 2

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C







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REVISIONS		
CHK	CHANGE NO.	REV

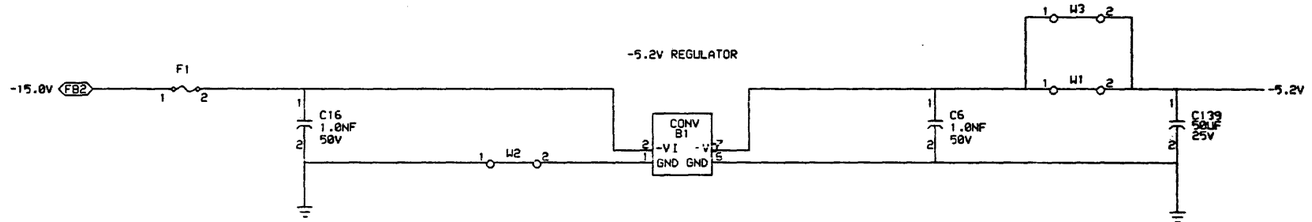
DRN.	DATE 14-SEP-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION: SHEET 11 OF 16	

TITLE: UDA # 2

PS:<DOUGHERTY>UDA2EC9.DRW 14-SEP-82 17:49
FIRST USED ON OPTION/MODEL: UDA
NEXT HIGHER ASSEMBLY: B-DD-M7162-0

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

REV. C
NUMBER M7162-0-UDA2
CODE CS
SIZE K
B



NOTE:
1nF CAPS MUST BE AS CLOSE
AS POSSIBLE TO THE REGULATOR.

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 14-SEP-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION:	
		SHEET 12 OF 16	

TITLE: UDA # 2

PS:<DOUGHERTY>UDA2CC.DRW 14-SEP-82 17:43 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0

FIRST USED ON OPTION/MODEL: UDA

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

+5.0V

C1 47nF 50V, C2 47nF 50V, C3 47nF 50V, C4 47nF 50V, C7 47nF 50V, C8 47nF 50V, C12 47nF 50V, C13 47nF 50V, C14 47nF 50V, C17 47nF 50V, C18 47nF 50V, C19 47nF 50V, C21 47nF 50V, C22 47nF 50V, C23 47nF 50V, C24 47nF 50V, C25 47nF 50V, C26 47nF 50V, C29 47nF 50V, C30 47nF 50V, C31 47nF 50V, C32 47nF 50V

+5.0V

C33 47nF 50V, C34 47nF 50V, C35 47nF 50V, C38 47nF 50V, C39 47nF 50V, C40 47nF 50V, C42 47nF 50V, C43 47nF 50V, C45 47nF 50V, C46 47nF 50V, C48 47nF 50V, C51 47nF 50V, C54 47nF 50V, C55 47nF 50V, C65 47nF 50V, C66 47nF 50V, C83 47nF 50V, C84 47nF 50V, C91 47nF 50V, C92 47nF 50V, C102 47nF 50V, C105 47nF 50V

+5.0V

C107 47nF 50V, C110 47nF 50V, C113 47nF 50V, C116 47nF 50V, C117 47nF 50V, C118 47nF 50V, C120 47nF 50V, C130 220nF 50V, C131 220nF 50V, C132 220nF 50V, C129 47nF 50V, C133 47nF 50V, C134 47nF 50V, C140 47nF 50V, C141 47nF 50V, C142 47nF 50V, C143 47nF 50V, C144 47nF 50V, C145 47nF 50V, C146 47nF 50V, C147 47nF 50V, C148 47nF 50V

-5.2V

C10 47nF 50V, C56 47nF 50V, C60 47nF 50V, C61 47nF 50V, C62 47nF 50V, C63 47nF 50V, C64 47nF 50V, C67 47nF 50V, C68 47nF 50V, C69 47nF 50V, C70 47nF 50V, C71 47nF 50V, C72 47nF 50V, C73 47nF 50V, C74 47nF 50V, C75 47nF 50V, C76 47nF 50V, C77 47nF 50V, C78 47nF 50V, C79 47nF 50V, C80 47nF 50V, C81 47nF 50V, C82 47nF 50V

-5.2V

C95 47nF 50V, C86 47nF 50V, C87 47nF 50V, C88 47nF 50V, C89 47nF 50V, C90 47nF 50V, C93 47nF 50V, C94 47nF 50V, C95 47nF 50V, C96 47nF 50V, C97 47nF 50V, C98 47nF 50V, C99 47nF 50V, C100 47nF 50V, C101 47nF 50V, C103 47nF 50V, C104 47nF 50V, C106 47nF 50V, C108 47nF 50V, C111 47nF 50V, C112 47nF 50V, C115 47nF 50V

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. DATE 14-SEP-82 ENG. DATE

CHK'D. DATE

PS:<DOUGHERTY>UDA2CD.DRW 14-SEP-82 17:43

FIRST USED ON OPTION/MODEL: UDA

NEXT HIGHER ASSEMBLY: B-DD-M7162-0

BOARD LOCATION:

SHEET 13 OF 16

TITLE: UDA # 2

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

REV. C

NUMBER M7162-0-UDA2

SIZE K CODE CS

P1

P2

P3

P4

TEST POINTS

7 8 9 4 5 6

15 14 13

12 11 10

1 2 3

-5.2V

REG

NOTE: JUMPER CONFIGURATIONS

NORMAL CONFIGURATIONS	TTL WRAPAROUND W/DIAG CLK	TTL WRAPAROUND W/PULSED EXT CLK
1 - 2	2 - 3	2 - 3
4 - 5	5 - 6	5 - 6
7 - 8	8 - 9	8 - 9
11 - 12	10 - 11	10 - 11
13 - 14	13 - 14	14 - EXT CLK
		15 - EXT CLK GND

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. | DATE 14-SEP-82 | ENG. | DATE

CHK'D. | DATE | BOARD LOCATION: SHEET 14 OF 16

PS:<DOUGHERTY>UDA2CE.DRW]14-SEP-82 17:43 | NEXT HIGHER ASSEMBLY: B-DD-M7162-0

FIRST USED ON OPTION/MODEL: UDA

TITLE: UDA # 2

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

M7162-0-UDA2 REV. C SIZE K CODE CS B

Vertical location (A-D) Direction of line (Left, Right, Up, Down)
or electrical (Input, Output, Both)
KEY: 5S-VH,D or backplane pin (Pin)
Schematic Sheet Horizontal location (1-8)

+12.0V 1-D1,L
+15.0V ..... 1-D2,R <CU1>
+5.0V 1-A4,R 1-C1,L 1-C4,D 5-B3,D 5-B4,D 9-A8,R
9-B8,R 9-C8,R 9-D8,R 10-A8,R 10-B8,R 10-C8,R 10-D8,R 13-C8,D
13-C8,D 13-D8,D 1-C2,R <AA2> 1-C2,R <BA2> 1-C2,R <CA2>
1-C2,R <DA2> 1-C2,R <EA2> 1-C2,R <FA2>
-15.0V ..... 12-C7,R <FB2>
-5.2V 7-A2,D 7-A5,D 7-B4,R 7-B7,D 7-C1,R 7-C6,R
7-C7,D 7-C7,D 8-A3,L 8-A5,D 8-B4,R 8-C2,R 8-C7,D 8-C7,D
8-C7,R 9-A6,D 9-A6,D 9-A8,R 9-B3,D 9-B6,D 9-B6,D 9-B8,R
9-C4,D 9-C6,D 9-C6,D 9-C8,R 9-D4,D 9-D4,D 9-D6,D 9-D6,D
9-D8,R 10-A2,D 10-A6,R 10-A6,R 10-A8,R 13-B2,D 10-B4,L 10-B6,D
10-B6,D 10-B8,R 10-C2,D 10-C4,D 10-C5,L 10-C6,D 10-C6,D 10-C8,R
10-D2,D 10-D5,D 10-D5,D 10-D6,D 10-D6,D 10-D8,R 12-C2,L 13-A8,D
13-B8,D
BA00 H 3-B1,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R 4-B5,R
4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R 4-D4,R
4-D5,R -D5,R 4-D6,R 4-D7,R 4-D8,R
BA01 H 3-B1,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R 4-B5,R
4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R 4-D4,R
4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA02 H 3-B1,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R 4-B5,R
4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R 4-D4,R
4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA03 H 3-B1,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R 4-B5,R
4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R 4-D4,R
4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA04 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA05 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA06 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA07 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA08 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA09 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-D2,R 4-D2,R 4-D3,R
4-D4,R 4-D5,R 4-D5,R 4-D6,R 4-D7,R 4-D8,R
BA10 H 3-D2,L 3-D3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-C2,R 4-C2,R 4-C3,R
4-C4,R 4-C5,R 4-C5,R 4-C6,R 4-C7,R 4-C8,R
BA11 H 3-C2,L 3-C3,L 4-B2,R 4-B2,R 4-B3,R 4-B4,R
4-B5,R 4-B5,R 4-B6,R 4-B7,R 4-B8,R 4-C2,R 4-C2,R 4-C3,R
4-C4,R 4-C5,R 4-C5,R 4-C6,R 4-C7,R 4-C8,R
BUS BG4 IN H ..... 1-A5,R <DS2>
BUS BG4 OUT H ..... 1-A5,L <DT2>
BUS BG5 IN H ..... 1-A5,R <DP2>
BUS BG5 OUT H ..... 1-A5,L <DR2>
BUS BG6 IN H ..... 1-A5,R <DM2>
BUS BG6 OUT H ..... 1-A5,L <DN2>
BUS BG7 IN H ..... 1-A5,R <DK2>
BUS BG7 OUT H ..... 1-A5,L <DL2>
BUS NPG IN H ..... 1-A5,R <CA1>
BUS NPG OUT H ..... 1-A5,L <CB1>
CLK BDR H 1-A2,R 1-B6,L
CLK BDR L 1-A1,L 3-B6,R 4-A3,R 4-A8,R 4-A8,R 5-A7,R
CLK DIOC L 1-C4,R 1-C7,R
CLK ENB H 1-B6,L 4-A5,R
CLK SERDES H 1-B6,L 2-A4,R 5-C8,R
CLR PTY L 6-A5,L 6-D7,R
CMD OUT L 1-D3,L 2-D7,R 5-C8,R
DATA OUT L 2-C3,L 5-C4,R
DATA PULSE ERROR L 6-B2,R 9-D3,L
DATA RDY H 1-A8,R 5-A7,L 5-C7,L
DATA WORD CLK L 1-A6,L 2-D7,R 5-A7,L 5-C7,L
DATA XMIT ERROR H 6-B1,L 6-D5,R
DBUS 00 H 1-C7,R 1-D5,R 3-C3,R 3-D5,L 3-D7,R 5-A1,L
5-B5,R 5-C5,L 6-C4,R 6-C5,L
DBUS 01 H 1-C7,R 1-D5,R 3-C3,R 3-D5,L 3-D7,R 5-A1,L
5-B5,L 5-B5,R 6-B4,R 6-C5,L
DBUS 02 H 1-D5,R 1-D7,R 3-C3,R 3-D5,L 3-D7,R 5-A1,L
5-B5,L 5-B5,R 6-B4,R 6-D5,L
DBUS 03 H 1-D5,R 1-D7,R 3-C3,R 3-D5,L 3-D7,R 5-A1,L
5-B5,L 5-B5,R 6-B4,R 6-D5,L
DBUS 04 H 1-D5,R 1-D7,R 3-D2,R 3-D4,R 3-D5,L 3-D7,R
5-A1,L 5-C5,R 5-D5,L 6-B4,R 6-C5,L
DBUS 05 H 1-D5,R 1-D7,R 3-D2,R 3-D4,R 3-D5,L 3-D7,R
5-A1,L 5-C5,R 5-D5,L 6-B4,R 6-B5,L
DBUS 06 H 1-D5,R 1-D7,R 3-C7,R 3-D2,R 3-D4,R 3-D5,L
5-A1,L 5-C5,R 5-D5,L 6-B4,R 6-B5,L
DBUS 07 H 1-D5,R 1-D7,R 3-C5,L 3-C7,R 3-D2,R 3-D4,R
5-A1,L 5-C5,R 5-D5,L 6-B4,R 6-D5,L
DBUS 08 H 1-B5,R 1-D7,R 3-C5,L 3-C7,R 3-D2,R 3-D4,R
5-B6,R 5-C1,L 5-C6,L 6-D5,L
DBUS 09 H 1-B5,R 1-D7,R 3-C5,L 3-C7,R 3-D2,R 3-D4,R
5-B1,L 5-B6,L 5-B6,R
DBUS 10 H 1-B5,R 1-D7,R 3-C5,L 3-C7,R 3-D2,R 3-D4,R
5-B1,L 5-B6,L 5-B6,R
DBUS 11 H 1-B5,R 1-D7,R 3-C2,R 3-C4,R 3-C5,L 3-C7,R
5-B1,L 5-B6,L 5-B6,R
DBUS 12 H 1-B5,R 1-D7,R 3-C5,L 3-C7,R 5-B1,L 5-C6,R
5-D6,L
DBUS 13 H 1-B5,R 1-D7,R 3-B5,L 3-B7,R 5-B1,L 5-C6,R
5-D6,L
DBUS 14 H 1-B5,R 1-D7,R 3-B5,L 3-B7,R 5-B1,L 5-C6,R
5-D6,L
DBUS 15 H 1-B5,R 1-D7,R 3-B5,L 3-B7,R 5-B1,L 5-C6,R
5-D6,L 6-C5,L
DI/O CLR L 1-D3,L 6-A2,R
DIAG CLK H 1-B4,L 7-D8,R 8-B1,L
DIAG DATA H 1-B4,L 7-C8,R
DIAG MODE H 1-C4,L 7-C8,R 8-C8,R
DIAG MODE L 1-C4,L 7-D8,R 8-C8,R
DLY UPROC H 1-A2,R 1-A7,R 4-A8,R
DLY UPROC L 1-A1,L 4-A3,R 4-A8,R
DRV SEL 0 H 1-D5,L 7-C8,R
DRV SEL 1 H 1-D5,L 7-B8,R
DRV SEL 2 H 1-D5,L 7-B8,R
DRV SEL 3 H 1-D5,L 7-B8,R
DRV SEL0 T L 7-C7,L 9-D2,R 9-D5,R 10-D2,R 10-D5,R
DRV SEL1 T L 7-B7,L 9-C2,R 9-C5,R 10-C2,R 10-C5,R
DRV SEL2 T L 7-B7,L 9-B2,R 9-B5,R 10-B2,R 10-B5,R
DRV SEL3 T L 7-B7,L 9-A2,R 9-A5,R 10-A2,R 10-A5,R
DTEST H 1-A7,R 1-D3,L 5-B2,R
ECC CLR L 2-D3,L 5-C2,R
ECC ENABLE H 1-D3,L 2-C7,R
ECC FDBCK EN H 2-B2,L 5-A7,L 5-C2,R
ECC INPUT EN H 2-D2,L 5-A7,L 5-C2,R
ECC OUT 0 H 5-A2,R 5-B3,R 5-C1,L
ECC OUT 1 H 5-A2,R 5-B3,R 5-C1,L
ECC OUT 2 H 5-A2,R 5-A3,R 5-C1,L
ECC OUT 3 H 5-A2,R 5-A3,R 5-C1,L
ECC OUT 4 H 5-A2,R 5-A3,R 5-C1,L
ECC OUT 5 H 5-A2,R 5-A3,R 5-C1,L
ECC OUT 6 H 5-A2,R 5-A3,R 5-D1,L
ECC OUT 7 H 5-A2,R 5-A3,R 5-D1,L
ECC OUT 8 H 5-B4,R 5-C2,R 5-D1,L
ECC OUT 9 H 5-B2,R 5-B4,R 5-D1,L
ECC RDY H 1-A8,R 2-B3,L
ECC START H 2-C5,L
ECC STOP H 2-B6,R 2-C5,R
ECC SYMBOL CLK L 2-C6,R 5-C3,L
ECC SYMBOL L 5-B3,L
ECC TIME H 1-D3,L 2-D7,R
ECC10+2 H 2-C6,L
ECCT16 L 2-D6,L
EN RAM PE H 1-D5,L 3-A6,R
EVEN PARITY H 6-B1,L
GND 3-A2,R 3-A3,R 3-B3,R 5-A7,L 5-A7,R 5-C4,R
5-C4,R 1-C2,R <AC2> 1-B2,R <AT1> 1-B2,R <BC2>
1-B2,R <BT1> 1-B2,R <CC2> 1-B2,R <CT1> 1-B2,R <DC2>
1-B2,R <DT1> 1-B2,R <EC2> 1-B2,R <ET1> 1-B2,R <FC2>
1-B2,R <FT1>
HI RTCS H 8-D1,L 10-C5,R 10-D2,R
HI WCD H 7-D1,L 9-C5,R 9-D2,R
HIGH H 7-B6,R 8-B7,R 8-D3,L
HIPRTY IN H 3-A5,L 4-C8,R
HIPRTY OUT H 3-A7,R 4-D7,L
I/O 00 H 5-C6,L 5-D6,R 5-D7,L
I/O 01 H 5-C6,L 5-D6,R 5-D7,L
I/O 02 H 5-C6,L 5-D6,R 5-D7,L
I/O 03 H 5-C6,L 5-D6,R 5-D7,L
I/O 04 H 5-B6,L 5-B6,R 5-D7,L
I/O 05 H 5-B6,L 5-B6,R 5-D7,L
I/O 06 H 5-B6,L 5-B6,R 5-C7,L
I/O 07 H 5-B6,L 5-C6,R 5-C7,L
I/O 08 H 5-C5,L 5-C7,L 5-D5,R
I/O 09 H 5-C5,L 5-C7,L 5-D5,R
I/O 10 H 5-C5,L 5-C7,L 5-D5,R
I/O 11 H 5-C5,L 5-C7,L 5-D5,R
I/O 12 H 5-B5,L 5-B5,R 5-C7,L
I/O 13 H 5-B5,L 5-B5,R 5-C7,L
I/O 14 H 5-B5,L 5-B5,R 5-C7,L
I/O 15 H 5-B5,L 5-C5,R 5-C7,L
INC DBAR H 3-A3,R 4-A7,L
INC UBAR H 3-B3,R 4-A7,L
IOC SEL 0 H 1-C3,R 1-C7,R
IOC SEL 1 H 1-C3,R 1-C7,R
IOC SEL 2 H 1-C3,R 1-C7,R
LD BUFFER L 1-B6,L 3-B7,R 4-A8,R 4-A8,R

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REVISIONS

CHK	CHANGE NO.	REV

DRN.	DATE	ENG.	DATE	TITLE:
	15-SEP-82			UDA # 2
CHK'D.	DATE	BOARD LOCATION:		
		SHEET 15 OF 16		

DSK:UDA2,T2P4,50) 15-SEP-82 07:24 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA B-DD-M7162-0

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

LD DBAR L	1-B6,L	3-A4,R		
LD DCR L	1-C5,R	1-C6,L		
LD ECC L	2-B6,L	5-C4,R		
LD RTCS L	1-C6,L	6-B4,R		
LD SERDES L	1-B6,L	5-C8,R		
LD UBAR L	1-B6,L	3-B3,R		
LED 1 L	1-B3,L	5-A7,R		
LED 2 L	1-B3,L	5-A7,R		
LED 4 L	1-B3,L	5-A7,R		
LED 8 L	1-B3,L	5-A7,R		
LO RTCS H	8-C1,L	10-B5,R	10-D2,R	
LO WCD H	7-D1,L	9-B5,R	9-D2,R	
LOPRTY IN H	3-B5,L	4-B8,R		
LOPRTY OUT H	3-B7,R	4-C7,L		
NRZ CLK OUT H	5-A7,L	5-D8,R	7-B1,L	7-D8,R
NRZ DATA IN H	5-A7,L	5-D8,R	7-A2,L	
NRZ DATA OUT H	5-B7,L	7-C8,R		
ODD PRTY H	1-B4,L	3-A7,R	3-B7,R	
OVERRUN H	1-A7,R	5-C7,L		
RAM 00 H	3-B7,R	3-D6,R	3-D7,L	4-C1,L
RAM 01 H	3-B7,R	3-D6,R	3-D7,L	4-C2,L
RAM 02 H	3-A7,R	3-D6,R	3-D7,L	4-C3,L
RAM 03 H	3-A7,R	3-D6,R	3-D7,L	4-C3,L
RAM 04 H	3-A7,R	3-D6,R	3-D7,L	4-C4,L
RAM 05 H	3-A7,R	3-D6,R	3-D7,L	4-C5,L
RAM 06 H	3-A7,R	3-C6,R	3-D7,L	4-C6,L
RAM 07 H	3-A7,R	3-C6,R	3-C7,L	4-C6,L
RAM 08 H	3-A7,R	3-C6,R	3-C7,L	4-D1,L
RAM 09 H	3-A7,R	3-C6,R	3-C7,L	4-D2,L
RAM 10 H	3-A7,R	3-C6,R	3-C7,L	4-D3,L
RAM 11 H	3-A7,R	3-C6,R	3-C7,L	4-D3,L
RAM 12 H	3-A7,R	3-C6,R	3-C7,L	4-D4,L
RAM 13 H	3-A7,R	3-B6,R	3-B7,L	4-D5,L
RAM 14 H	3-A7,R	3-B6,R	3-B7,L	4-D6,L
RAM 15 H	3-A7,R	3-B6,R	3-B7,L	4-D6,L
RAM CS L	4-A4,L			
RAM PE L	1-A8,R	3-A5,L		
RAM WE L	4-A4,L			
RD BUFFER L	1-B6,L	3-B6,R		
RD ECC L	2-C2,L	5-C4,R		
RD ECC RSDU L	1-B6,L	5-B2,R		
RD MODE H	1-D3,L	2-C3,R	5-C8,R	
RD RTDS L	1-C6,L	6-B5,R		
RD SERDES L	1-B6,L	5-B5,R	5-B6,R	5-C8,R
READ H	3-A6,R	3-A7,R	3-B7,R	3-B7,R 4-A5,L 4-A5,R
READ L	3-A7,R	3-B7,R	4-A5,L	4-A5,R
REAL TIME PULSE ERROR L	6-A2,R	10-D3,L		
RECV ERROR H	1-B8,R	6-A1,L	6-D5,R	
RESET L	1-C5,R	1-C7,R		
RRD H	7-A7,R	9-C4,L		
RRD NEG H	9-D4,L			
RRD POS H	9-D4,L			
RSGEN CLK L	2-A5,L	5-A7,L	5-C2,R	
RSGEN EN L	1-D3,L	2-B6,R		
RTCS CLK H	6-C4,R	8-B2,L	8-D8,R	
RTCS DATA H	6-C1,L	8-A2,L	8-C8,R	
RTCS DLY DATA H	8-C2,L			
RTCS NEW DATA H	8-C2,L			
RTCS P1 H	8-D3,L			
RTCS P2 H	8-D3,L			
RTCS P2 L	8-D3,L			

RTCS RDY H	1-A8,R	6-A3,L	6-D5,R			
RTDS CLK H	6-A6,R	6-A8,R	6-B8,R	6-D8,R	8-B2,L	
RTDS DATA 1 L	6-C8,R	6-D7,L				
RTDS DATA 2 L	6-C7,L	6-C8,R				
RTDS DATA 3 L	6-C7,L	6-C8,R				
RTDS DATA 4 L	6-B8,R	6-C7,L				
RTDS DATA 5 L	6-B7,L	6-B8,R				
RTDS DATA 6 L	6-B7,L	6-B8,R				
RTDS DATA H	6-D8,R	8-B2,L				
RTDS H	8-B8,R	10-C4,L				
RTDS NEG H	10-D4,L					
RTDS PE H	6-A3,R	6-B5,R	6-D7,L			
RTDS POS H	10-D4,L					
RTDS RCVD H	1-A8,R	6-A5,L	6-D5,R			
RVCC1	1-C2,L	2-B3,D	2-D7,D	4-A3,D	4-A3,D	4-A5,R
	4-A8,R	5-A7,D	5-B7,D	5-B8,R	5-C4,R	
RVCC2	1-C1,L	6-A5,R	6-A6,D	6-A8,R	6-B3,R	6-B4,D
	6-B4,R	6-C1,D	6-C4,R	6-C8,R	6-D2,R	6-D7,D
RVCC3	1-C1,L	7-B8,R				
SDO10 H	5-C3,L					
SDO16 H	5-A7,L	5-B4,R				
SDO16/10 H	5-A7,L	5-B8,R				
SERDES ENABLE H	1-D3,L	5-B2,R	5-B8,R			
SERDES10 EN H	1-C2,L	5-C4,R				
SET IOC H	1-C3,R	1-C7,R				
STROBE ECC H	2-B4,L	5-B2,R	5-C4,R			
SWEEP FREQ H	7-B1,L	8-B2,L	8-D8,R			
SYNCH DET H	6-A3,R	6-B5,L				
TRTCS0N H	10-D1,L	11-C2,L				
TRTCS0P H	10-D1,L	11-D2,L				
TRTCS1N H	10-C1,L	11-C2,L				
TRTCS1P H	10-C1,L	11-C2,L				
TRTCS2N H	10-B1,L	11-B2,L				
TRTCS2P H	10-B1,L	11-C2,L				
TRTCS3N H	10-A1,L	11-B2,L				
TRTCS3P H	10-A1,L	11-B2,L				
TWCD0N H	9-D1,L	11-C4,L				
TWCD0P H	9-D1,L	11-D4,L				
TWCD1N H	9-C1,L	11-C4,L				
TWCD1P H	9-C1,L	11-C4,L				
TWCD2N H	9-B1,L	11-B4,L				
TWCD2P H	9-B1,L	11-C4,L				
TWCD3N H	9-A1,L	11-B4,L				
TWCD3P H	9-A1,L	11-B4,L				
UPROC H	3-C2,R	4-A3,L	4-A6,R	4-A8,R		
UPROC L	2-A4,R	3-A4,R	4-A3,L	4-A6,R	4-A8,R	
WCD DLY DATA H	7-C2,L					
WCD NEW DATA H	7-C2,L					
WCD P1 H	7-D2,L					
WCD P2 H	7-D2,L					
WCD P2 L	7-D2,L					
WCDDL1	7-C4,L					
WCDDL2	7-D4,L					
WRAP H	7-D2,L	9-C5,R	10-C5,R			
WRC L	6-C2,L					
WRT ECC L	2-C3,L	5-A4,R	5-B2,R	5-C4,R		
XRRD0 H	9-D8,R	11-B7,R				
XRRD0 L	9-D8,R	11-B6,L				
XRRD1 H	9-C8,R	11-B7,R				
XRRD1 L	9-C8,R	11-B6,L				
XRRD2 H	9-B8,R	11-C7,R				

XRRD2 L	9-B8,R	11-C6,L
XRRD3 H	9-A8,R	11-C7,R
XRRD3 L	9-A8,R	11-C6,L
XRTCS0 H	11-B7,R	11-C3,R
XRTCS0 L	11-B6,L	11-C3,R
XRTCS1 H	11-C3,R	11-C7,R
XRTCS1 L	11-C3,R	11-C6,L
XRTCS2 H	11-B3,R	11-C7,R
XRTCS2 L	11-B3,R	11-C6,L
XRTCS3 H	11-B3,R	11-C7,R
XRTCS3 L	11-B3,R	11-C6,L
XRTDS0 H	10-D8,R	11-B7,R
XRTDS0 L	10-D8,R	11-B6,L
XRTDS1 H	10-C8,R	11-B7,R
XRTDS1 L	10-C8,R	11-B6,L
XRTDS2 H	10-B8,R	11-C7,R
XRTDS2 L	10-B8,R	11-C6,L
XRTDS3 H	10-A8,R	11-C7,R
XRTDS3 L	10-A8,R	11-C6,L
XWCD0 H	11-B7,R	11-C5,R
XWCD0 L	11-B6,L	11-C5,R
XWCD1 H	11-C5,R	11-C7,R
XWCD1 L	11-C5,R	11-C6,L
XWCD2 H	11-B5,R	11-C7,R
XWCD2 L	11-B5,R	11-C6,L
XWCD3 H	11-B5,R	11-C7,R
XWCD3 L	11-B5,R	11-C6,L

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 15-SEP-82	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION:	
		SHEET 16 OF 16	
DSK:UDA2.T2P[4,50]	15-SEP-82 07:24	NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL: UDA		B-DD-M7162-0	

TITLE: UDA # 2

SIZE	CODE	NUMBER	REV.
K	CS	M7162-0-UDA2	C

REV. C | NUMBER M7162-0-UDA2 | CODE CS | SIZE K

SOURCE BY NUMBER

DRW. NO. NUMBER

BDD M7485-0

SOURCE BY NUMBER

SIZE	CODE	NUMBER	REV
B	DD	M7485-0-0	J

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																
B-DD-M7485-0-0	2		Drawing Directory	A	B	C	D	E	F	H	J									
D-UA-M7485-0-0	1		Unit Assembly	A	A	A	B	C	D	E	F									
K-PL-M7485-0-DBP	3		Parts List (23715)	A	B	C	D	E	F	H	J									
K-CS-M7485-0-1	12		Circuit Schematic	A	B	C	D	E	F	F	F									
K-CS-M7485-0-02	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-03	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-04	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-05	—		Circuit Schematic	A	B	B	B	B	—	—	—									
K-CS-M7485-0-06	—		Circuit Schematic	A	B	B	B	B	—	—	—									
K-CS-M7485-0-07	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-08	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-09	—		Circuit Schematic	A	A	A	A	A	—	—	—									
K-CS-M7485-0-10	—		Circuit Schematic	A	A	A	A	A	—	—	-									
K-CS-M7485-0-11	—		Circuit Schematic	A	A	A	A	A	—	—	-									
K-CS-M7485-0-12	—		Circuit Schematic	A	A	A	A	A	—	—	—									
		M7485-00	UDA PR	A	A	B	C	C	D1	D1	D2									
		M7485-YA	UDA PR (WITH PROMS)	A	B	C	D	E1	F1	H1	H2									
	-	5015403-01	Etched Board	A	A	A	A	A	—	—	—									
K-PC-M7485-0-DBC	-		PC Data Base	A	A	A	A	A	B	B	B									

NOTES:

REVISION HISTORY																				
REV.	A	B	C	D	E	F	H	J												
ECO NO.	INIT	M7485-CX001 MR	M7485-CX002	M7485-CX003	M7485-CX004	M7485-CX005 JN	M7485-CX006 JN	M7485-CX007 JN												
DATE	25 AUG 82	1680 SMS 18 FEB 83	1686 SMS 4 MAR 83	1820 SMS 5 JULY 83	1862 SMS 8 SEPT 83	1863 SMS 11 NOV 83	SMS 8 JANUARY 5013	5194 SMS 28 MAR 84												

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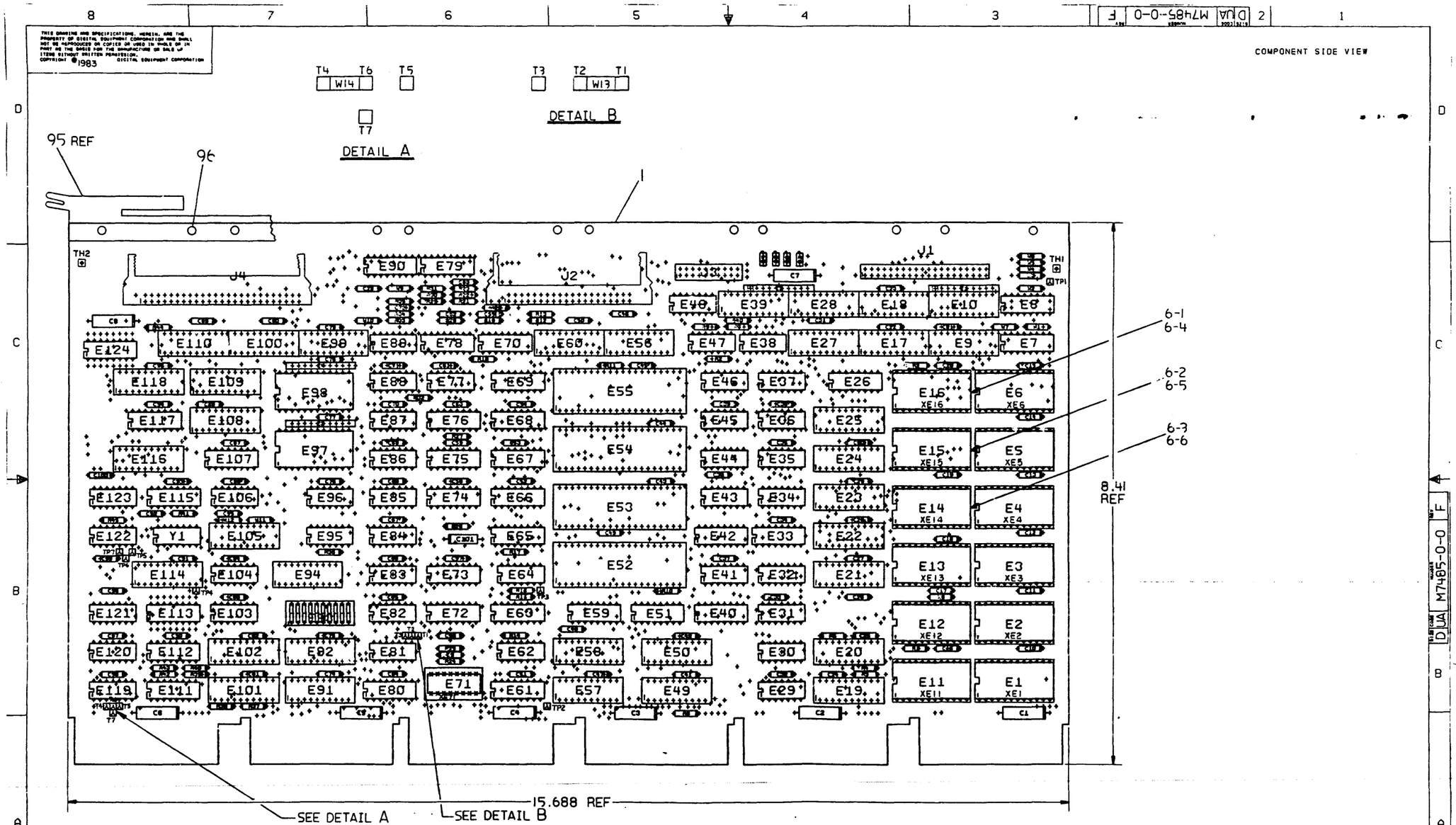
USED ON OPTION/MODEL

DRN. R. Mulvihill	DATE 24 Aug 82	TITLE: UDA PR
CHK'D J. Bourbeau	DATE 24 Aug 82	DOCUMENT NUMBER
DES. ENG. C. Rodgers	DATE 8-26-82	SIZE B / CODE DD / NUMBER M7485-0-0 / REV. J
RESP. ENG. C. Rodgers	DATE 8-26-82	SHEET 1 OF 2
MFG. ENG. Roy Bourbeau	DATE 8-26-82	

BDD M7485-0

SIZE	CODE	NUMBER	REV
B	DD	M-7485-0-0	J

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
D-MD-5015403-0-0	3		Drill and Etch Drawing	A A A A A — —
E-EC-5015403-0-0	2		Etch Cut Drawing	A A A A A — —
B-DD-5015403-0	1		ETCHED CIRCUIT BOARD	— — — — — F F



NOTES: 1. DO NOT INSTALL EYELET IN POSITION (ITEM 96).
2. DO NOT MOUNT Y1 FLUSH WITH BD. (METAL)
3. THE FOLLOWING ARE SPARES: E39, E94, E105, E113, E116, E124, E85, R8, R44, R45, C101, Z3, Z4, W2-W5, W7, W9-W11, TP1-TP7.

STEP E	↑ Y AXIS ____ STEP ____ TIMES	
REPEAT	→ X AXIS ____ STEP ____ TIMES	

CHK	CHANGE NO	REV
1863	ECO M7485-CX005 J.R. 14 NOV 83 J.VAGIAS	D
	ECO M7485-CX006 W.M.B. JUN 84 J.VAGIAS	E
	M7485-CX007 W.M.24 JAN 86 J.VAGIAS	F

ETCH REV. B1-P1

SIGNATURES	DATE
DRN. Eric Somers	24 Jun 83
CHK'D. [signature]	15-11-83
MECH. ENG. [signature]	11-21-83
PROJ. ENG. [signature]	11-21-83
PROD. W.E. Myers	12-13-83
SCALE: 1.5/1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. B-DD-M7485-0-0	

digital

TITLE UDA PR

SIZE	CODE	NUMBER	REV
D	UA	M7485-0-0	F

1 MS# 400538B

DUA M7485-0-0

1 of 2

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ECO M7485-CX006

COMPONENT DELETES: SIDE 1

6-1. DELETE E16 (23121F4-00) OR (23146F4-00).
6-2. DELETE E15 (23122F4-00) OR (23147F4-00).
6-3. DELETE E14 (23123F4 00) OR (23148F4 00).

COMPONENT ADDS: SIDE 1

6-4. ADD E16 (23184F4-00).
6-5. ADD E15 (23185F4-00).
6-6. ADD E14 (23186F4-00).

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UDA PR	D	UA	M7485-0-0	F
SCALE	SHEET 2 OF 2	DIST.		

UDA M7485-00

2 of 2

AUTOMATED BY VAXKPL (V1.0) — P A R T S L I S T — SHEET A1 OF A3

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 00 D2	YA H2	REFERENCE DESIGNATORS
1	1	B-DD-5015403-0	50-15403-01	B	DRILL & ETCH	1	1	
2	2		10-12784-00		.047 MFD 50V +80-20% CER	91	91	C10-C100
3	3		10-13466-08		680.0 MMF 50V 10% X7R CER	1	1	C9
4	4		10-16549-00		47 MFD 10V +50-10% AL EL	8	8	C1-C8
5	5		11-14136-01		LED 6.5MA 5V 1.2MCD	4	4	D1-D4
6	6		12-09838-00		SKT,IC 16PIN DIP GOLD	1	1	XE71
7	7		90-09149-00		PIN,STAKNG 0.025ODX0.345LG SQUAR	7	7	T1-T7
8	8		12-11164-06		SW,DIP 10POS/1PST 5VDC100MA F	1	1	E93
9	9		12-12965-04		PCB,HEADER 20PIN(2X05).100CC 90D	1	1	J3
10	10		12-18783-00		JUMPER 02POS(1X02).100CC	2	2	W13,W14
11	11		12-14993-00		PCB,HEADER 40POS(2X20).100CC 90D	1	1	J1
12	12		12-15006-01		*** THIS ITEM IS NOT USED ***	-	-	
13	13		12-16832-02		PCB,HEADER 40POS(2X20).100CC 90D	1	1	J2
14	14		12-16832-03		PCB,HEADER 50POS(2X25).100CC 90D	1	1	J4
15	15		13-00229-00		100.0 .25 W 5.0 % CF	8	8	R3,R5-R7,R9,R16,R27,R36
16	16		13-00316-00		470.0 .25 W 5.0 % CF	4	4	R10,R11,R17,R25
17	17		13-00365-00		1.0 K .25 W 5.0 % CF	2	2	R14,R24
18	18		13-00447-00		4.70 K .25 W 5.0 % CF	2	2	R1,R2
19	19		13-01421-00		15.0 .25 W 5.0 % CF	1	1	R41
20	20		13-01972-00		270.0 .25 W 5.0 % CF	2	2	R4,R15
21	21		13-02377-00		39.0 .25 W 5.0 % CF	7	7	R12,R19,R30-R34
22	22		13-02379-00		75.0 .25 W 5.0 % CF	6	6	R13,R18,R20,R23,R28,R29
23	23		13-05125-00		383.0 .25 W 1.0 % RN55D-F10	2	2	R38,R43
24	24		13-11422-00		178.0 .25 W 1.0 % RN55D-F10	4	4	R37,R39,R40,R42
25	25		13-12929-00		62.0 .25 W 5.0 % CF	3	3	R21,R22,R35
26	26		13-16395-00		R NETWORK 9-4.7K 2.0 % 10PIN	1	1	Z2
27	27		13-16395-02		R NETWORK 9-1.0K 2.0 % 10PIN	1	1	Z1
28	28		13-18784-01		R NETWORK MULTI-VALUE 16PIN	1	1	E71
29	29		16-17533-00		DELAY= 250NS,5TAPS 14PIN DIP	1	1	E103
30	30		16-18344-00		DELAY= 58NS,5TAPS	1	1	E88
31	31		18-11660-16		OSCILLATOR, XTAL 17.280 MHZ	1	1	Y1
32	32		19-09705-00		DEC 8881 NAND GATE-QUAD 2IN O	1	1	E81

REVISION HISTORY			KPL MODULE FORMAT	SECTION A OF A		DRN: SHERI LEHMAN	D I G I T A L
ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX			DATE: 30-JUN-83	
JV	M7485-CX005	F	[A] 00,YA	[M]		CHK'D: SUE BOURBEAU	TITLE PARTS LIST
RB	M7485-CX006	H	[B]	[N]		DATE: 30-JUN-83	UDA PR
JV	M7485-CX007	J	[C]	[P]		DES.ENG: CURT RIDGEWAY	DOCUMENT NUMBER
			[D]	[Q]		DATE: 30-JUN-83	SIZE: K CODE: PL NUMBER: M7485-0-DBP REV: J
			[E]	[R]			
			[F]	[S]		RESP.ENG.: CURT RIDGEWAY	
			[H]	[T]		DATE: 30-JUN-83	
			[J]	[V]			
			[K]	[W]		MFG.ENG: ROY BOWERS	RELEASE DATE: 28-JAN-86
			[L]	[Y]		DATE: 30-JUN-83	RELEASE STATUS: RELEASED
			BASIC PART NUMBER: M7485	ASSEMBLY NUMBER: B-UA-M7485-0-0	TOP DOCUMENT NUMBER: B-DD-M7485-0-0	FILE NAME: Z3715J.PLS	EDIT #: 9

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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 00 D2	YA H2	REFERENCE DESIGNATORS
33	33		19-10532-00		74S00 NAND GATE-QUAD 2IN	2	2	E31,E44
34	34		19-10534-00		74S04 INVERTER GATE-HEX 1I	2	2	E77,E89
35	35		19-10536-00		74S10 NAND GATE-TRIPLE 3IN	1	1	E87
36	36		19-10537-00		74S11 AND GATE-TRIPLE 3INP	1	1	E43
37	37		19-10542-00		74S64 A-O-I GATE 4-2-3-2	2	2	E41,E86
38	38		19-10544-00		74S74 FF-D DUAL,EDGE TRIGG	1	1	E48
39	39		19-10545-00		74S112 FF-JK DUAL,EDGE TRIG	1	1	E115
40	40		19-10546-00		74S140 NAND GATE-DUAL 4INPU	1	1	E47
41	41		19-10548-00		74S157 MUX 1 OF 2 (QUAD)	5	5	E33,E65-E68
42	42		19-10550-00		74S174 FF-D HEX	2	2	E7,E8
43	43		19-10552-00		74S194 SHIFT REG.,4BIT RIGH	2	2	E51,E59
44	44		19-10950-00		74S74 FF-D DUAL (-45 VERSI	1	1	E38
45	45		19-11116-00	DEC	8837 RECEIVER,BUS,HEX,UNI	1	1	E61
46	46		19-14987-00		8641-2 TRANSCEIVER,UNIBUS,	1	1	E80
47	47		19-11675-00		74S138 DECODER/DEMUX 3-8 LI	3	3	E70,E79,E90
48	48		19-11676-00		74S139 DECODER-DUAL TWO-INP	2	2	E40,E78
49	49		19-11712-00		74S51 AND-OR GATE-INVERT D	1	1	E46
50	50		19-11983-00		74S133 NAND GATE-POSITIVE 1	1	1	E26
51	51		19-12097-00	SN	74S182 LOOK AHD CARRY GEN	1	1	E42
52	52		19-12388-00		74S02 NOR GATE-QUAD 2IN,PO	2	2	E64,E121
53	53		19-12389-00		74S08 AND GATE-QUAD 2IN,PO	2	2	E45,E83
54	54		19-12728-00		74S251 MUX 1 OF 8 TRI-STA	4	4	E69,E74-E76
55	55		19-12799-00		LS00 NAND-GATE-QUAD 2IN,P	1	1	E95
56	56		19-12803-00		LS04 INVERTER GATE,HEX	2	2	E82,E104
57	57		19-12808-00		LS11 AND GATE-TRIPLE 3IN	1	1	E62
58	58		19-12820-00		LS51 A-O-I GATE 2-WIDE 2I	1	1	E96
59	59		19-12824-00		LS74 FF-D DUAL,EDGE TRIGG	1	1	E120
60	60		19-12842-00		LS138 DECODER-THREE INPUT,	1	1	E72
61	61		19-12850-00		LS164 SHIFT REG. 8BIT SERI	1	1	E119
62	62		19-12860-00		LS259 LATCH 8BIT	1	1	E63
63	63		19-12863-00		LS273 FF-D OCTAL W/CLEAR	2	2	E99,E114
64	64		19-12864-00		LS279 LATCH,QUAD-S-R	1	1	E73
65	65		19-13040-00	DC	005 TRANSCEIVER 4BIT	4	4	E91,E92,E101,E102
66	66		19-13245-02		2901A-1 MICROPRESCESSOR 4-	4	4	E52-E55
67	67		19-13340-00		74S32 OR GATE-QUAD 2IN	1	1	E37
68	68		19-13414-00		LS14 INVERTER GATE-HEX SC	1	1	E84
69	69		19-13671-00		74S374 FF-D,OCTAL,TR1 STATE	3	3	E20,E22,E23
70	70		19-13939-00		LS191 COUNTER,SYNCHR. UP/D	2	2	E107,E117
71	71		19-14214-00		LS374 FF-D OCTAL EDGE TRIG	7	7	E19,E21,E24,E25,E108,E109,E118
72	72		19-14438-00	DC	013 UNIBUS INTERRRUPT-BIP	2	2	E111,E112
73	73		19-14451-00		LS393 COUNTER,BINARY,4BIT	3	3	E106,E122,E123
74	74		19-15193-00		LS244 DRIVER,LINE,OCTAL,TR	2	2	E56,E60
75	75		19-15218-00		LS245 TRANSCEIVER,BUS,OCTA	2	2	E100,E110
76	76		19-15305-00	AM	2908 TRANSCEIVER,BUS,LATC	4	4	E49,E50,E57,E58
77	77		19-16680-01		2911A MICROPROGRAM SEQUENC	6	6	E9,E10,E17,E18,E27,E28
78	78		19-17956-00		LS280 PARITY GEN/CHK,9BIT,	6	6	E29,E30,E32,E34-E36
79	79		23-184F4-00	F4-01		-	1	E16
80	80		23-185F4-00	F4-01		-	1	E15
81	81		23-186F4-00	F4-01		-	1	E14
82	82		23-149F4-00	F4-01		-	1	E13

D	I	G	I	T	A	L	TITLE	SECTION A OF A
							UDA PR	

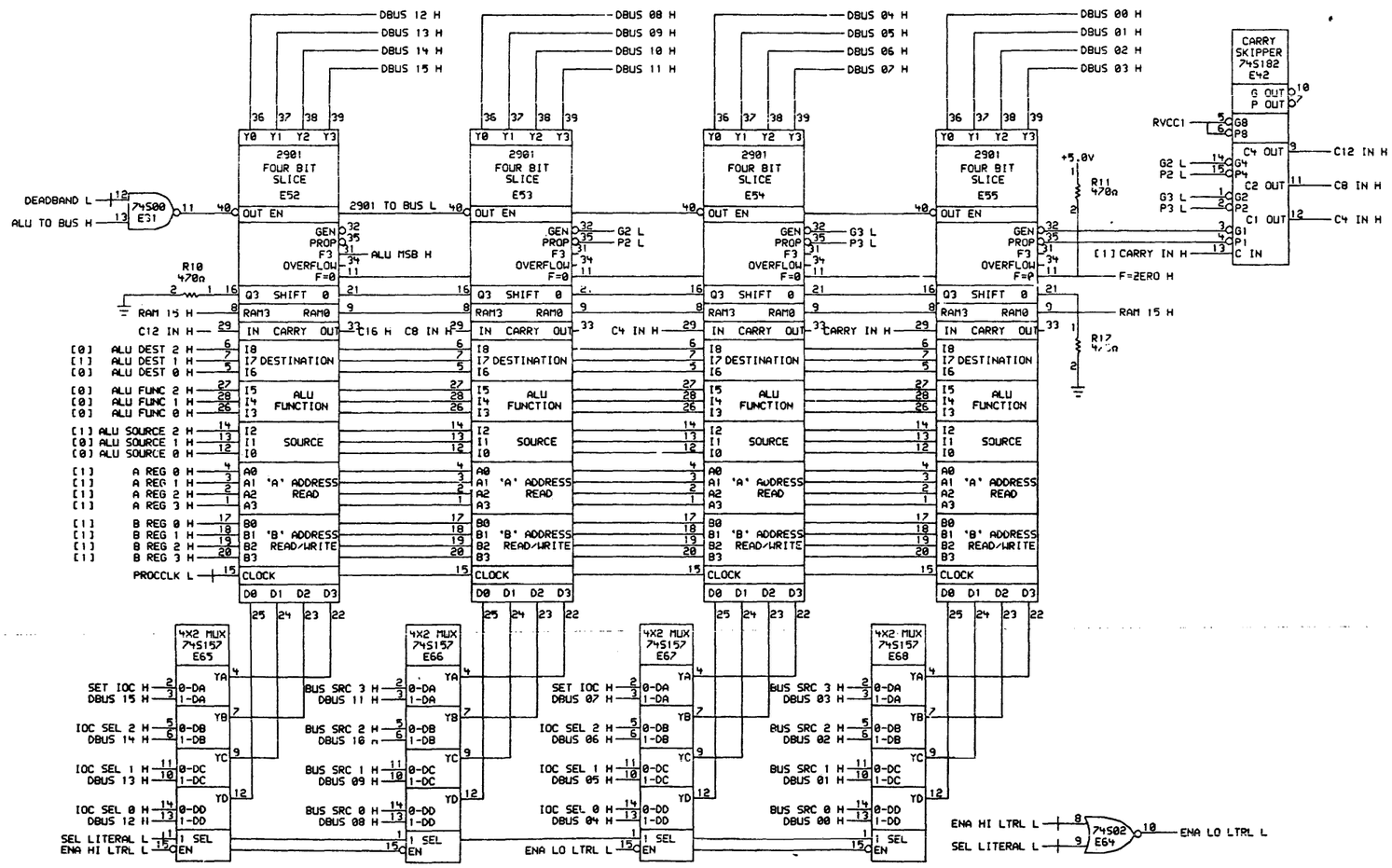
SIZE	CODE	DOCUMENT NUMBER	REV
K	PL	M7485-0-DBP	J

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 00 D2	YA H2	REFERENCE DESIGNATORS
83	83		23-150F4-00	F4-01		-	1	E12
84	84		23-151F4-00	F4-01		-	1	E11
85	85		23-152F4-00	F4-01		-	1	E6
86	86		23-153F4-00	F4-01		-	1	E5
87	87		23-154F4-00	F4-01		-	1	E4
88	88		23-155F4-00	F4-01		-	1	E3
89	89		23-156F4-00	F4-01		-	1	E2
90	90		23-157F4-00	F4-01		-	1	E1
91	91		23-13F4 -00	F4-01		1	1	E97
92	92		23-14F4 -00	F4-01		1	1	E98
93	93		90-09185-00		JUMPER, WIRE, INSULATED, BLACK B	4	4	W1,W6,W8,W12
94	94		12-15006-06		SKT,IC 24PIN DIP TIN SOLD	12	12	XE1-XE6,XE11-XE16
95	95		12-16988-02		HANDLE,MODULE,HEX TWO EJECTORS	1	1	
96	96		90-00024-01		EYELET,ROLLED 0.1210DX0.192	11	11	
97	97		13-00417-00		2.20 K .25 W 5.0 % CF	1	1	R26
98	98				*** THIS ITEM IS NOT USED ***	-	-	

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							UDA PR		K	PL	M7485-0-DBP	J

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 5%.
2. GATES MARKED WITH A STAR (*)
   MAY BE "S" OR "LS".
3. 2901 RAM REGISTERS CONFIGURED FOR
   A 16 BIT ROTATION WHILE THE "Q"
   REGISTER IS A 16 BIT SHIFT.
4. LITERAL BITS 0-7 CORRESPOND TO
   BUS SRC 0-3, IOC SEL 0-3 AND
   SET IOC.
5. NUMBERS SHOWN IN BRACKETS, [ ],
   INDICATE LOGIC LEVEL FOR
   INSTRUCTION ZERO.



UDA50A 5015403B ALU

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REVISIONS			
CHK	CHANGE NO.	REV
867	M7485-C1005	F

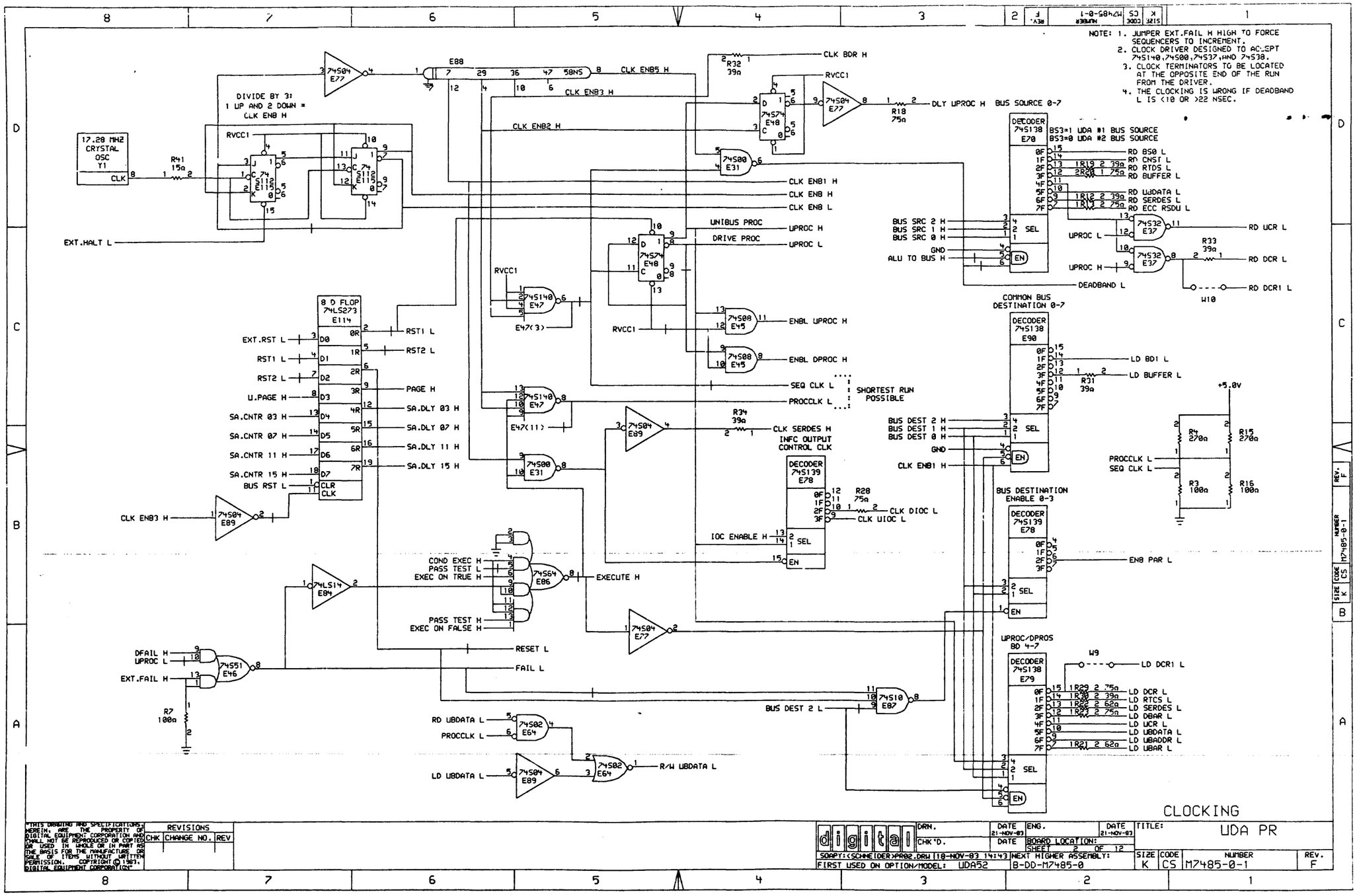
DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK	DATE	BOARD LOCATION:	
SHEET 1 OF 12			

TITLE: UDA PR

SOAPY:<SCHNEIDER>PR01.DRW 18-NOV-83 14:39 | NEXT HIGHER ASSEMBLY: B-DD-M7485-0

FIRST USED ON OPTION/MODEL: UDA52

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F


NOTE: 1. JUMPER EXT.FAIL H HIGH TO FORCE SEQUENCERS TO INCREMENT.
2. CLOCK DRIVER DESIGNED TO ACCEPT 74S140,74S00,74S37,AND 74S38.
3. CLOCK TERMINATORS TO BE LOCATED AT THE OPPOSITE END OF THE RUN FROM THE DRIVER.
4. THE CLOCKING IS WRONG IF DEADBAND L IS <10 OR >22 NSEC.
17.28 MHZ CRYSTAL OSC Y1
DIVIDE BY 3: 1 UP AND 2 DOWN = CLK ENB H
CLK ENB5 H
CLK ENB3 H
CLK ENB2 H
CLK BDR H
DLY UPROC H
BUS SOURCE 0-7
DECODER 74S138 E70
BS3=1 UDA #1 BUS SOURCE
BS3=0 UDA #2 BUS SOURCE
RD BS0 L
RD CNST L
RD RTDS L
RD BUFFER L
RD UBDATA L
RD SERDES L
RD ECC RSDU L
RD UCR L
RD DCR L
RD DCR1 L
DEADBAND L
UNIBUS PROC
DRIVE PROC
UPROC H
UPROC L
ENBL UPROC H
ENBL DPROC H
SEQ CLK L
PROCCLK L
SHORTEST RUN POSSIBLE
COMMON BUS DESTINATION 0-7
DECODER 74S138 E90
LD BD1 L
LD BUFFER L
BUS DEST 2 H
BUS DEST 1 H
BUS DEST 0 H
CLK ENB1 H
CLK SERDES H
INFC OUTPUT CONTROL CLK
DECODER 74S139 E78
CLK DIOC L
CLK UIOC L
IOC ENABLE H
BUS DESTINATION ENABLE 0-3
DECODER 74S139 E78
ENB PAR L
UPROC/DPROS BD 4-7
DECODER 74S138 E79
LD DCR1 L
LD DCR L
LD RTCS L
LD SERDES L
LD DBAR L
LD UCR L
LD UBDATA L
LD UBADDR L
LD UBAR L
8 D FLOP 74LS273 E114
EXT.RST L
RST1 L
RST2 L
U.PAGE H
SA.CNTR 03 H
SA.CNTR 07 H
SA.CNTR 11 H
SA.CNTR 15 H
BUS RST L
PAGE H
SA.DLY 03 H
SA.DLY 07 H
SA.DLY 11 H
SA.DLY 15 H
CLK ENB3 H
COND EXEC H
PASS TEST L
EXEC ON TRUE H
PASS TEST H
EXEC ON FALSE H
EXECUTE H
RESET L
FAIL L
DFAIL H
UPROC L
EXT.FAIL H
RD UBDATA L
PROCCLK L
LD UBDATA L
R/W UBDATA L
BUS DEST 2 L
EXT.HALT L
CLOCKING
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REVISIONS
CHK CHANGE NO. REV
digital
DRN.
CHK'D.
DATE 21-NOV-83
ENG.
DATE 21-NOV-83
DATE
BOARD LOCATION:
SHEET 2 OF 12
SOAPY:<SCHNEIDER>PR02.DRW 18-NOV-83 14:43
FIRST USED ON OPTION/MODEL: UDA52
NEXT HIGHER ASSEMBLY: B-DD-M7485-0
TITLE: UDA PR
SIZE K
CODE CS
NUMBER M7485-0-1
REV. F

SIGNITURE ANALYSER CONTROL

BRANCHING

CROM PARITY CHECKING

NOTE: SIGNATURE ANALYZER CONNECTIONS:
CLOCK = CLK ENB L = P3-19 RISING EDGE
START = SA.START H = RISING EDGE
STOP = SA.STOP L = FALLING EDGE
JUMPER INT.RESET L TO EXT.RST L

NOTE: AN ERROR WILL ALLOW THE INSTRUCTION WITH THE ERROR TO COMPLETE THE NEXT ONE, THEN VECTOR TO THE ERROR ROUTINE.

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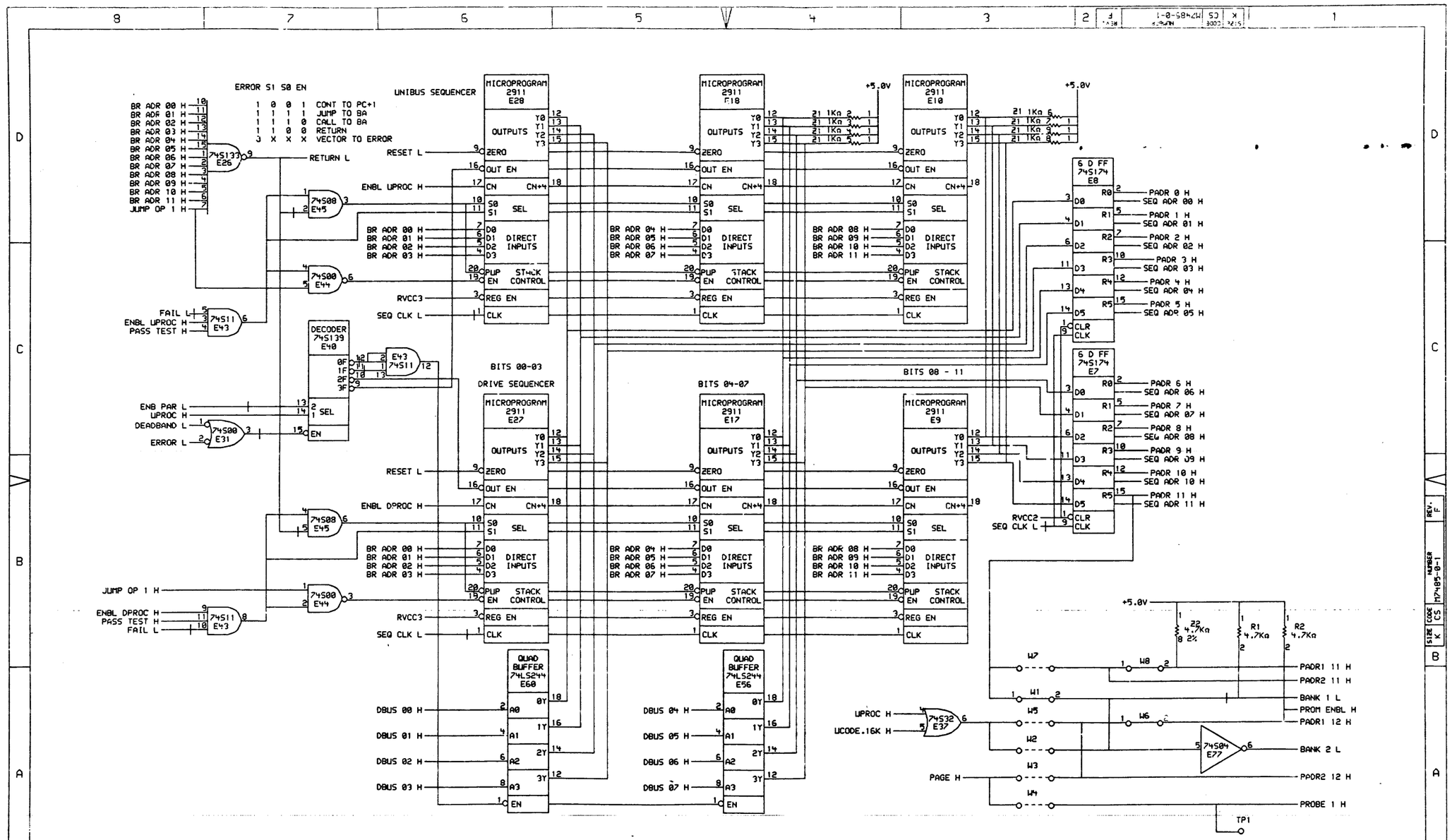
REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83	TITLE:	UDA PR
CHK'D.	DATE	BOARD LOCATION: SHEET 3 OF 12			
SOAPY:(SCHNEIDER)PR03.DRW 18-NOV-83 14:46		NEXT HIGHER ASSEMBLY:		SIZE K / CODE CS / NUMBER M7485-0-1	REV. F
FIRST USED ON OPTION/MODEL: UDA52		B-DD-M7485-0			



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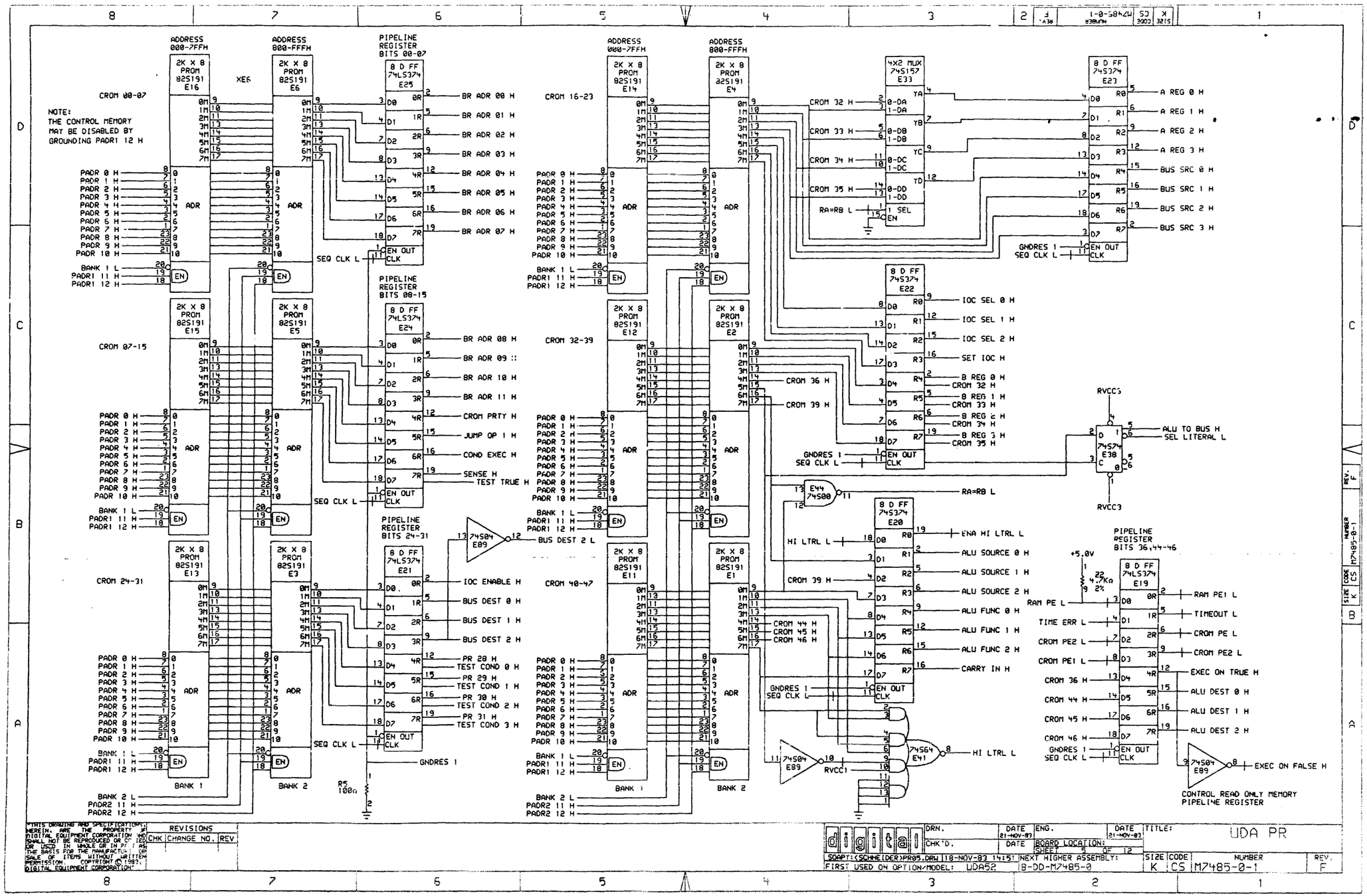
REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83	TITLE: UDA PR
	CHK'D.	DATE	BOARD LOCATION: SHEET 4 OF 12		
SOAPY:<SCHNEIDER>PR04.DRW 18-NOV-83 14:49			NEXT HIGHER ASSEMBLY: B-DD-M7485-0		SIZE K / CODE CS / NUMBER M7485-0-1 / REV. F
FIRST USED ON OPTION/MODEL: UDA52					



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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK'D.	DATE	BOARD LOCATION:	SHEET 5 OF 12

TITLE: UDA PR

SOAPY:<SCHNEIDER>PR05.DRW 18-NOV-83 14:51 | NEXT HIGHER ASSEMBLY: B-DD-M7485-0

FIRST USED ON OPTION/MODEL: UDA52

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F

UDASA

NOTE: UNIBUS INTERFACE 5-14 PIN, 12-16 PIN, 10-30PIN.

UNIBUS/CONSTANT ADDRESS REGISTER

8 D FF 74_S374 E109

UP/DOWN COUNTER 74LS191 E117

UP/DOWN COUNTER 74LS191 E107

INCRIMENT WORD

AUTO-INCREMENT FOR 256 WORDS MAX.

UNIBUS ADDRESS DRIVER/COMPARATOR

4 BIT TRANS CEIVER DC005 E92

4 BIT TRANS CEIVER DC005 E91

4 BIT TRANS CEIVER DC005 E101

4 BIT TRANS CEIVER DC005 E102

UNIBUS ADDRESS SELECTOR SWITCH
W4=765 XX0,2Q
W5=765 XX4,6Q
RANGE:
765 000Q-
777 776Q
NORMALLY= 772150,2

SWITCH OPEN=0
SWITCH CLOSED=1
A3 A12

UNIBUS DATA REGISTER

2908 E58 BUS TRANCEIVER

2908 E57 BUS TRANCEIVER

2908 E50 BUS TRANCEIVER

2908 E49 BUS TRANCEIVER

2908
+5V = PIN 20
GND = PINS 5,15
TXCLK IS AN EDGE TRIGGERED LATCH
RX/LCH/EN IS AN ENABLE FOR A TRANSPARENT LATCH

UNIBUS DATA AND ADDRESS

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83	TITLE: UDA PR
CHK'D.	DATE	BOARD LOCATION: SHEET 6 OF 12		
SOAPY::<SCHNEIDER>PR06.DRW 18-NOV-83 14:53		NEXT HIGHER ASSEMBLY:		SIZE K | CODE CS | NUMBER M7485-0-1 | REV. F
FIRST USED ON OPTION/MODEL: UDA52		B-DD-M7485-0		

NOTES:
1) BUS NPG IN TO OUT JUMPER MUST BE REMOVED (CB1 FROM CA1).
2) C8 IS UNDRIVEN AND PULLED INACTIVE
3) GATES MARKED WITH A STAR (*) MAY BE 74SXX OR 74LSXX.
4) INTR H CONNECTION TO 8641 IS TO GENERATE SSYNC FOR NON-EXISTENT MEMORY.

ENSLAVE H	INIT MODE =0	RUN MODE =1
UDAIP R X0/4 W	-	POLL
UDASA R X2/6 W	INIT STATUS	INIT ADDR/DATA
		0 PURGE

UNIBUS I/O PAGE ADDRESS DECODER
DECODER 74LS138 E72
0F RDX0.RUN L
1F RDX2.RUN L
2F WRTX0.RUN L
3F WRTX2.RUN L
4F RDX0.INIT L
5F RDX2.INIT L
6F WRTX0.INIT L
7F WRTX2.INIT L

INTR L → 74LS279 E73 R → PURGED L (VAX BUFFER PURGED)
ENSLAVE H → 74LS14 E84 → 74LS279 E73 R → SCAN L (POLL OF COMMAND BUFFER REQUESTED)

BUS AC LO L (CV1) → 8837 E61 → ACLO H
BUS DC LO L (CN1) → 8837 E61
BUS INIT L (DL1) → 8837 E61
BUS PA L (CC1) → 8837 E61
BUS PB L (CS1) → 8837 E61
TP2

SSYNC EN H, C1 H → 74S08 E83 → DEVSEL H
C1 H, A01 H → 74S138 E72 2 SEL, EN
DEVSEL H → 8881 E81 → BUS RST L → 74LS14 E62

+5.0V → R24 1Kn → 74LS04 E82 → SSYNC EN H
BUS LTCH L, DEVSEL H → 8881 E81 → BUS SSYNC L
R25 470n, C9 680pF 50V 10%

DEVSEL H TO SSYNC EN H
145-752 NSEC DELAY HIGH
201-755 NSEC DELAY LOW

UNIBUS PARITY ERROR DETECTION
BUS PA L, BUS PB L → 74S02 E121 → 74LS74 E120 → PRTYERR H
BUS LTCH L, I/O CLR L

I/O CONTROL REGISTER
8 BIT LATCH 74LS259 E53 TP4
0F UTEST H
1F U.PAGE H
2F NPR REQ H
3F I/O CLR L
4F DATO H
5F ENSLAVE H
6F BUS REQ H
7F

IOC SEL 2 H, IOC SEL 1 H, IOC SEL 0 H → 74LS138 E72 2 SEL
SET IOC H, RST1 L → 74S08 E83 → CLK UIOC L → DATA EN, RESET

INTR L → 74LS04 E82 → INTR H → 8881 E81 → BUS INTR L
BUS REQ H → 74LS04 E82

INSTRUCTION ZERO NEED NOT HAVE AN IOC (@SCLR) TO CAUSE THE RESET OF EACH LATCH BIT

SHIFT REG 74LS164 E119 DATA IN
0R, 1R, 2R, 3R, 4R, 5R, 6R, 7R
T4, T6, T7, W14, T5
SA.CNTR 02 H → CLR, CLK

MSTR H, SSYNC L → 74LS279 E73 S1 Q, S2, R
MCLR H → 74S08 E83 → 74LS04 E82
ADVADDR H

E103: 60NS 120NS 160NS 190NS 250NS
RVCC1, I/O CLR L, R/W UBDATA L → 74LS74 E120
START L → 74LS11 E62 → UDATARDY H
WRTX2.INIT L, XFER L → 74S08 E83

INITIALIZATION BASE ADDRESS WRITTEN

BUS C1/C0 L
DATO 0 1 DATA XFER MASTER TO SLAVE
DATI 1 1 DATA XFER SLAVE TO MASTER

+5.0V → R42 178n 1%, R40 178n 1%
NOTE: FOR INTERRUPT LEVEL 5 THE JUMPERS ARE: 2-7,3-6, 4-5,8-9,10-11,12-14.
E71 16 PIN SOCK
BG4 OUT H (DT2) BG4 IN H (DS2) BG5 OUT H (DR2) BG5 IN H (DP2) BG6 OUT H (DN2)
DD2 BUS BR7 L, DE2 BUS BR6 L, DF2 BUS BR5 L, DH2 BUS BR4 L
XE71: DK2 BG7 IN H, DL2 BG7 OUT H, DM2 BG6 IN H
R43 383n 1%

UNIBUS CONTROL DC013 E112
REQUEST, MASTER, STL GRANT, BG OUT, BG IN, BUS REQ, BUS SSYN, BUS BBST, BUS NPR, BUS SACK, SACK, CLR EN, MASTER CLR INIT
INTRPTMSTR L
SSYNC L → 74LS04 E82
INTERRUPT CONTROL

+5.0V → R39 178n 1%
UBMASTER L

BUS NPG IN H (CA1) → R37 178n 1% +5.0V
UNIBUS CONTROL DC013 E111
RVCC1 → R38 383n 1%
CB1 BUS NPG OUT H
FJ1 BUS NPR L
FD1 BUS BBSY L
FT2 BUS SACK L
NPR CONTROL

MSTR H
74LS00 E95 → RDX2.INIT L → 74LS11 E62 → BUS ENB L
74S02 E121 → BUS LTCH L
BUS SSYNC L
EJ1 BUS SSYNC L → SSYNC H → 74LS04 E104 → SSYNC L
EF2 BUS C1 L → C1 H
DATO H
EF1 BUS A02 L → A02 H → 74LS04 E104 → A02 L
UA02 H
EH1 BUS A01 L → A01 H → 74LS04 E104 → A01 L
UA01 H
TMSYN H
INTR H
8641 E80
UNIBUS CONTROL

BUS PA/PB L
1 1 NO ERROR IN SLAVE DATI/P
1 0 SLAVE ERROR IN DATAI/P
1 X RESERVED

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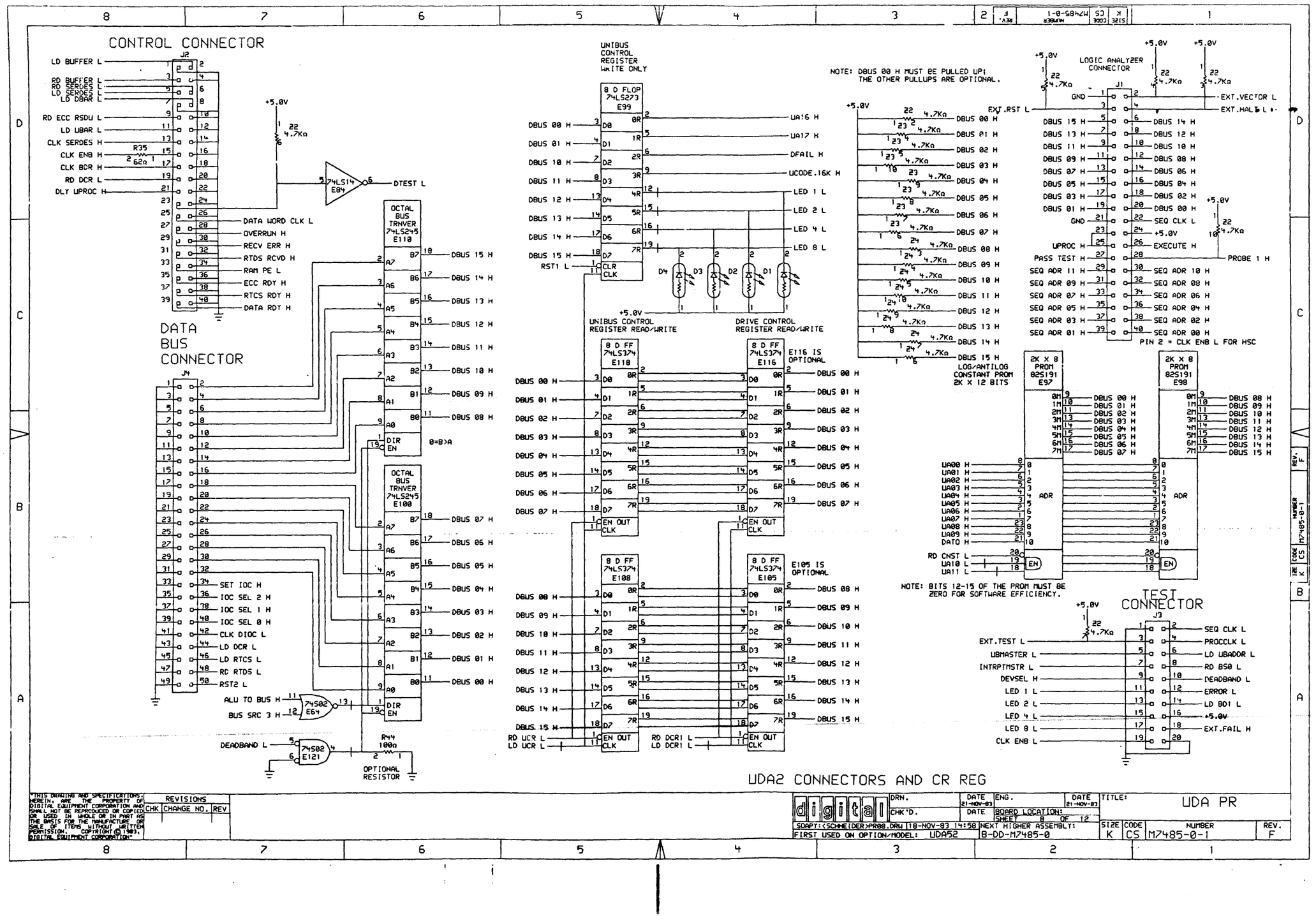
REVISIONS		
CHK	CHANGE NO.	REV

digital
DRN. | CHK'D. | DATE 21-NOV-83 | ENG. | DATE 21-NOV-83 | BOARD LOCATION: | SHEET 2 OF 12
TITLE: UDA PR
SOAPY:<SCHNEIDER>PR07.DRW;18-NOV-83 14:56 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA52 | B-DD-M7485 0
SIZE K | CODE CS | NUMBER M7485-0-1 | REV. F



UDA2 CONNECTORS AND CR REG

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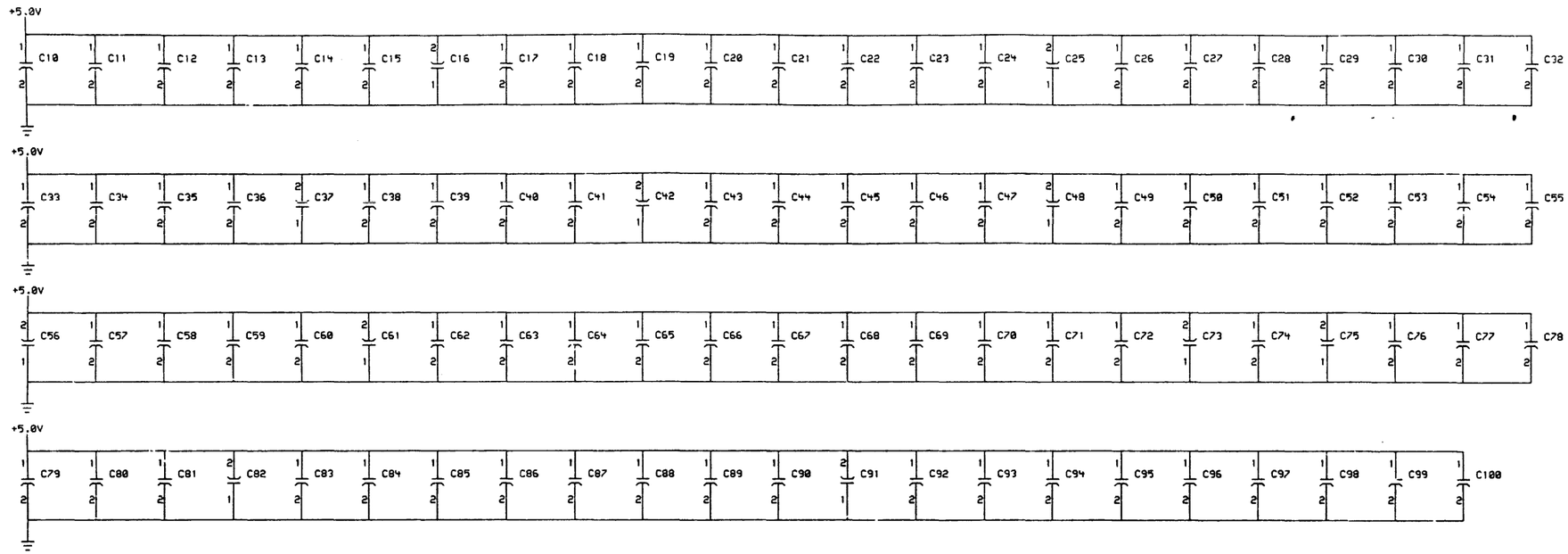
REVISIONS		
CHK	CHANGE NO.	REV

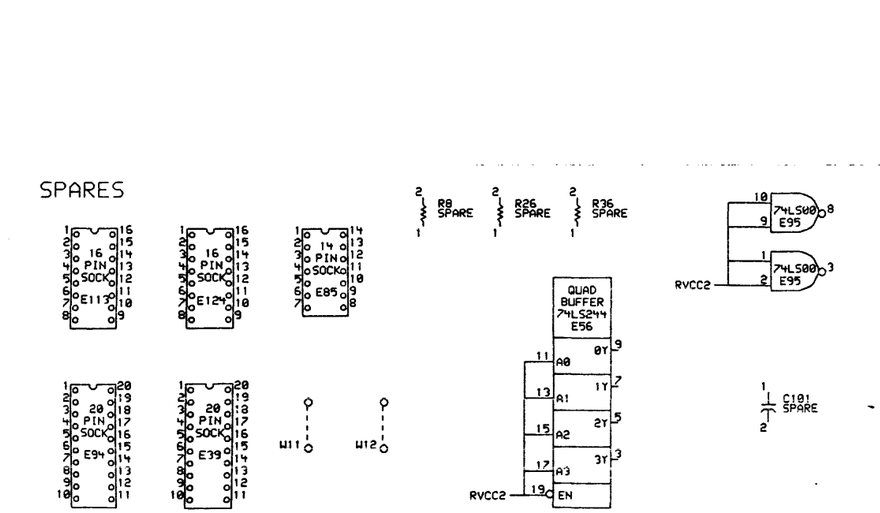
digital

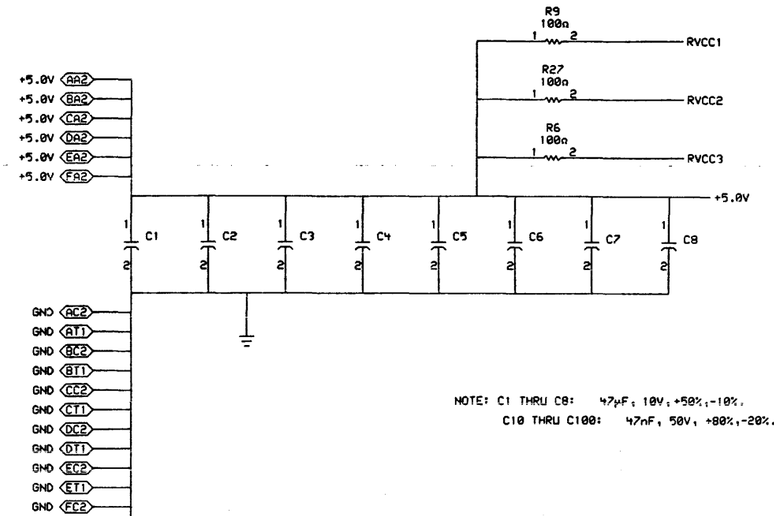
DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK'D.	DATE	BOARD LOCATION:	
SOAPY:<SCHNEIDER>PR88.DRW 18-NOV-83 14:58		SHEET 8 OF 12	
FIRST USED ON OPTION/MODEL: UDA52		NEXT HIGHER ASSEMBLY: B-DD-M7485-0	

TITLE: UDA PR

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F







NOTE: C1 THRU C8: 47μF, 10V, +50%,-10%.
C10 THRU C100: 47nF, 50V, +80%,-20%.

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83	TITLE: UDA PR
CHK'D.	DATE	BOARD LOCATION:		
		SHEET 2 OF 12		
SOAPY:<SCHNEIDER>PR09.DRW 18-NOV-83 15:00		NEXT HIGHER ASSEMBLY:		SIZE K | CODE CS | NUMBER M7485-0-1 | REV. F
FIRST USED ON OPTION/MODEL: UDA52		8-DD-M7485-0		

Vertical location (A-D) Direction of line (Left, Right, Up, Down)
KEY: SS-VH,D or electrical (Input, Output, Both) or backplane pin (Pin)
Schematic Sheet Horizontal location (1-8)

+5.0V	1-D4,D	2-C1,D	4-B2,R	4-D2,D	4-D4,D	5-B2,D	
	6-D5,D	7-C1,D	7-C3,R	7-D2,R	7-D4,D	8-A1,L	8-A2,D	8-C1,L
	8-C5,R	8-D1,D	8-D1,D	8-D1,D	8-D2,D	8-D3,D	8-D7,D	9-B1,L
	9-C8,D	9-C8,D	9-D8,D	9-D8,D	9-B4,R <AA2>		9-B4,R <BA2>	
	9-B4,R <CA2>		9-B4,R <DA2>		9-B4,R <EA2>		9-B4,R <FA2>	
2901 TO BUS L	1-C7,L							
A REG 0 H	1-B7,R	5-D2,L						
A REG 1 H	1-B7,R	5-D2,L						
A REG 2 H	1-B7,R	5-D2,L						
A REG 3 H	1-B7,R	5-D2,L						
A01 H	7-A2,L	7-D6,R						
A02 H	6-D6,R	7-A2,L						
A02 L	6-D6,R	7-A1,L						
ACLO H	3-A7,R	3-C7,R	7-D7,L					
ADVADDR H	6-A8,R	7-B4,L						
ALU DEST 0 H	1-C7,R	3-A3,R	5-A1,L					
ALU DEST 1 H	1-C7,R	3-A2,R	5-A1,L					
ALU DEST 2 H	1-C7,R	3-A2,R	5-A1,L					
ALU FUNC 0 H	1-C7,R	3-A3,R	5-B3,L					
ALU FUNC 1 H	1-C7,R	3-A3,R	5-A3,L					
ALU FUNC 2 H	1-C7,R	3-A3,R	5-A3,L					
ALU MSB H	1-C7,L	3-C8,R						
ALU SOURCE 0 H	1-C7,R	3-A3,R	5-B3,L					
ALU SOURCE 1 H	1-C7,R	3-A3,R	5-B3,L					
ALU SOURCE 2 H	1-C7,R	3-A3,R	5-B3,L					
ALU TO BUS H	1-C8,R	2-C3,R	3-A3,R	5-B2,L	8-A7,R			
B REG 0 H	1-B7,R	3-B3,R	5-C3,L					
B REG 1 H	1-B7,R	3-B3,R	5-C3,L					
B REG 2 H	1-B7,R	3-B3,R	5-C3,L					
B REG 3 H	1-B7,R	3-B3,R	5-B3,L					
BANK i L	4-A1,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R		
	5-C8,R							
BANK 2 L	4-A1,L	5-A5,R	5-A8,R					
BG4 IN H	7-D2,R <DS2>							
BG4 OUT H	7-D2,R <DT2>							
BG5 IN H	7-D2,R <DP2>							
BG5 OUT H	7-D2,R <DR2>							
BG6 IN H	7-D1,L <DM2>							
BG6 OUT H	7-D2,R <DN2>							
BG7 IN H	7-D1,L <DK2>							
BG7 OUT H	7-D1,L <DL2>							
BR ADR 00 H	3-D3,R	4-B6,R	4-D6,R	4-D8,R	5-D6,L			
BR ADR 01 H	3-D3,R	4-B6,R	4-D6,R	4-D8,R	5-D6,L			
BR ADR 02 H	3-D3,R	4-B6,R	4-C6,R	4-D8,R	5-D6,L			
BR ADR 03 H	3-D3,R	4-B5,R	4-C6,R	4-D8,R	5-D6,L			
BR ADR 04 H	3-D3,R	4-B5,R	4-D5,R	4-D8,R	5-D6,L			
BR ADR 05 H	3-D3,R	4-B5,R	4-D5,R	4-D8,R	5-D6,L			
BR ADR 06 H	3-D3,R	4-B5,R	4-C5,R	4-D8,R	5-D6,L			
BR ADR 07 H	3-D3,R	4-B5,R	4-C5,R	4-D8,R	5-C6,L			
BR ADR 08 H	3-D3,R	4-B4,R	4-D4,R	4-D8,R	5-C6,L			
BR ADR 09 H	3-C3,R	4-B4,R	4-D4,R	4-D8,R	5-C6,L			
BR ADR 10 H	3-C3,R	4-B4,R	4-C4,R	4-D8,R	5-C6,L			
BR ADR 11 H	3-C3,R	4-B4,R	4-C4,R	4-D8,R	5-C6,L			
BUS A01 L	7-A2,L <EH1>							
BUS A02 L	7-A2,L <EF1>							
BUS A03 L	6-B5,R <EV2>							
BUS A04 L	6-B5,R <EU2>							
BUS A05 L	6-B5,R <EV1>							
BUS A06 L	6-C5,R <EU1>							
BUS A07 L	6-C5,R <EP2>							
BUS A08 L	6-C5,R <EN2>							
BUS A09 L	6-B6,R <ER1>							
BUS A10 L	6-B6,R <EP1>							
BUS A11 L	6-B6,R <EL1>							
BUS A12 L	6-C6,R <EC1>							
BUS A13 L	6-C6,R <EK2>							
BUS A14 L	6-C6,R <EK1>							
BUS A15 L	6-C6,R <ED2>							
BUS A16 L	6-C5,R <EE2>							
BUS A17 L	6-B6,R <ED1>							
BUS AC LO L	7-D8,R <CV1>							
BUS BBSY L	7-B1,L <FD1>							
BUS BR4 L	7-D1,L <DH2>							
BUS BR5 L	7-D1,L <DF2>							
BUS BR6 L	7-D1,L <DE2>							
BUS BR7 L	7-D1,L <DD2>							
BUS C1 L	7-A2,L <EF2>							
BUS D00 L	6-D2,L <CS2>							
BUS D01 L	6-D2,L <CR2>							
BUS D02 L	6-D2,L <CU2>							
BUS D03 L	6-D2,L <CT2>							
BUS D04 L	6-C2,L <CN2>							
BUS D05 L	6-C2,L <CP2>							
BUS D06 L	6-C2,L <CV2>							
BUS D07 L	6-C2,L <CM2>							
BUS D08 L	6-B2,L <CL2>							
BUS D09 L	6-B2,L <CK2>							
BUS D10 L	6-B2,L <CJ2>							
BUS D11 L	6-B2,L <CH1>							
BUS D12 L	6-A2,L <CH2>							
BUS D13 L	6-A2,L <CF2>							
BUS D14 L	6-A2,L <CE2>							
BUS D15 L	6-A2,L <CD2>							
BUS DC LO L	7-C8,R <CN1>							
BUS DEST 0 H	2-B3,R	3-B3,R	5-B6,L					
BUS DEST 1 H	2-B3,R	3-B3,R	5-B6,L					
BUS DEST 2 H	2-C3,R	3-B3,R	5-A6,L					
BUS DEST 2 L	2-A4,R	5-B5,L						
BUS ENB L	6-A3,R	7-B1,L						
BUS INIT L	7-C8,R <DL1>							
BUS INTR L	7-C4,L <FM1>							
BUS LTCH L	6-A3,R	7-B1,L	7-C3,R	7-C7,R				
BUS MSYN L	6-B5,R <EE1>							
BUS NPG IN H	7-C3,R <CA1>							
BUS NPG OUT H	7-C1,L <CB1>							
BUS NPR L	7-C1,L <FJ1>							
BUS PA L	7-C8,R <CC1>							
BUS PB L	7-C8,R <CS1>							
BUS REQ H	7-C5,L							
BUS RST L	2-B7,R	7-C5,L						
BUS SACK L	7-B1,L <FT2>							
BUS SRC 0 H	1-A5,R	1-A7,R	2-C3,R	3-C3,R	5-D2,L			
BUS SRC 1 H	1-A5,R	1-A7,R	2-C3,R	3-C3,R	5-D2,L			
BUS SRC 2 H	1-B5,R	1-B7,R	2-D3,R	3-C3,R	5-D2,L			
BUS SRC 3 H	1-B5,R	1-B7,R	3-C3,R	5-D2,L	8-A7,R			
BUS SSYNC L	7-A2,L	7-C3,L	7-A2,L <EJ1>					
C1 H	7-A2,L	7-C6,R	7-D6,R					
C12 IN H	1-C7,R	1-D2,L						
C16 H	1-C7,L	3-C8,R						
C4 IN H	1-C2,L	1-C5,R						
C8 IN H	1-C2,L	1-C6,R						
CARRY IN H	1-C3,R	1-C4,R	3-A2,R	5-A3,L				
CLK BDR H	2-D4,L	8-D8,R						
CLK DIOC L	2-B3,L	8-A7,L						
CLK ENB H	2-D4,L	8-D8,R						
CLK ENB L	2-D4,L	8-A2,R						
CLK ENB1 H	2-B3,R	2-D4,L	3-B2,R					
CLK ENB2 H	2-D6,L							
CLK ENB3 H	2-B8,R	2-D5,L	3-C3,R					
CLK ENB5 H	2-D5,L							
CLK SERDES H	2-B4,L	8-D8,R						
CLK UIOC L	2-B3,L	7-B6,R						
COND EXEC H	2-B6,R	3-C3,R	5-B6,L					
CROM 32 H	5-C3,L	5-D3,R						
CROM 33 H	5-C3,L	5-D3,R						
CROM 34 H	5-C3,L	5-D3,R						
CROM 35 H	5-B3,L	5-D3,R						
CROM 36 H	5-A2,R	5-C4,L						
CROM 39 H	5-B4,R	5-C4,L						
CROM 44 H	5-A2,R	5-B4,L						
CROM 45 H	5-A2,R	5-A4,L						
CROM 46 H	5-A2,R	5-A4,L						
CROM ERR L	3-D7,L							
CROM PE L	3-D2,R	3-D8,R	5-A1,L					
CROM PE1 L	3-A1,L	5-A2,R						
CROM PE2 L	5-A1,L	5-A2,R						
CROM PRTY H	3-C3,R	5-C6,L						
D TIMEOUT H	3-B1,L	3-C2,R						
DATA RDY H	3-B7,R	8-C7,L						
DATA WORD CLK L	3-B7,R	8-D7,L						
DATO H	7-A3,R	7-C5,L	8-B3,R					
DBUS 00 H	1-A5,R	1-D4,L	3-C8,R	4-A6,R	6-D2,L	6-D3,R		
	6-D8,R	8-A6,L	8-C2,L	8-C4,L	8-C5,R	8-D1,L	8-D3,L	8-D5,R
DBUS 01 H	1-A5,R	1-D4,L	4-A6,R	6-A8,R	6-D2,L	6-D3,R		
	8-A6,L	8-C2,L	8-C4,L	8-C5,R	8-D2,R	8-D3,L	8-D5,R	
DBUS 02 H	1-A5,R	1-D4,L	4-A6,R	6-A8,R	6-D2,L	6-D3,R		
	8-A6,L	8-B2,L	8-B5,R	8-C4,L	8-D1,L	8-D3,L		
DBUS 03 H	1-B5,R	1-D4,L	4-A6,R	6-A8,R	6-D2,L	6-D3,R		
	8-A6,L	8-B2,L	8-B4,L	8-B5,R	8-D2,R	8-D3,L		
DBUS 04 H	1-A6,R	1-D5,L	4-A5,R	6-A8,R	6-C2,L	6-C3,R		
	8-B2,L	8-B4,L	8-B5,R	8-B6,L	8-D1,L	8-D3,L		
DBUS 05 H	1-A6,R	1-D5,L	4-A5,R	6-B8,R	6-C2,L	6-C3,R		
	8-B2,L	8-B4,L	8-B5,R	8-B6,L	8-D2,R	8-D3,L		
DBUS 06 H	1-A6,R	1-D5,L	4-A5,R	6-B8,R	6-C2,L	6-C3,R		
	8-B2,L	8-B4,L	8-B5,R	8-B6,L	8-D1,L	8-D3,L		
DBUS 07 H	1-B6,R	1-D5,L	4-A5,R	6-B8,R	6-C2,L	6-C3,R		
	8-B2,L	8-B4,L	8-B5,R	8-B6,L	8-C3,L	8-D2,R		
DBUS 08 H	1-A7,R	1-D6,L	6-B2,L	6-B3,R	6-B8,R	8-B4,L		
	8-B5,R	8-B6,L	8-C1,L	8-C3,L	8-D1,L			
DBUS 09 H	1-A7,R	1-D6,L	6-B2,L	6-B3,R	6-D8,R	8-A4,L		
	8-A5,R	8-C1,L	8-C3,L	8-C6,L	8-D2,R			
DBUS 10 H	1-A7,R	1-D6,L	6-B2,L	6-B3,R	6-D8,R	8-A4,L		
	8-A5,R	8-B1,L	8-C3,L	8-C6,L	8-D1,L	8-D5,R		
DBUS 11 H	1-B7,R	1-D6,L	6-B2,L	6-B3,R	6-C8,R	8-A4,L		
	8-A5,R	8-B1,L	8-C3,L	8-C6,L	8-D2,R	8-D5,R		
DBUS 12 H	1-A8,R	1-D7,L	6-A2,L	6-A3,R	6-C8,R	8-A4,L		
	8-A5,R	8-B1,L	8-C3,L	8-C6,L	8-D1,L	8-D5,R		

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REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK'D.	DATE	BOARD LOCATION: SHEET 10 OF 12	
DSK:PR.T2PL4,243]	21-NOV-83 17:11	NEXT HIGHER ASSEMBLY: B-DD-M7485-0	
FIRST USED ON OPTION/MODEL: UDA52			

TITLE: UDA PR

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F

DBUS 13 H	1-A8,R	1-D7,L	6-A2,L	6-A3,R	6-C8,R	8-A4,L
	8-A5,R	8-B1,L	8-C3,L	8-C6,L	8-D2,R	8-D5,R
DBUS 14 H	1-A8,R	1-D7,L	6-A2,L	6-A3,R	6-C8,R	8-A4,L
	8-A5,R	8-B1,L	8-C3,L	8-C5,R	8-C6,L	8-D1,L
DBUS 15 H	1-B8,R	1-D7,L	6-A2,L	6-A3,R	6-C8,R	8-A4,L
	8-A5,R	8-B1,L	8-C3,L	8-C5,R	8-C6,L	8-D2,R
DEADBAND L	1-C8,R	2-C2,L	4-C8,R	8-A1,L	8-A7,R	
DEVSEL H	6-D4,L	7-C5,R	7-C6,R	8-A2,R		
DFAIL H	2-A8,R	8-D4,L				
DLY UPROC H	2-D3,L	8-D8,R				
DTEST L	2-A7,R	8-D6,L				
E47(11)	2-B5,R					
E47(3)	2-C5,R					
ECC RDY H	3-B7,R	8-C7,L				
ENA HI LTRL L	1-A4,R	1-A8,R	5-B3,L			
ENA LO LTRL L	1-A3,L	1-A6,R				
ENB PAR L	2-B2,L	4-C8,R				
ENBL DPROC H	2-C4,L	4-B6,R	4-B8,R			
ENBL UPROC H	2-C4,L	4-C8,R	4-D6,R			
ENSLAVE H	7-C5,L	7-D4,R				
ERROR L	3-B2,R	3-C1,L	4-C8,R	8-A1,L		
EXEC ON FALSE H	2-A6,R	5-A1,L				
EXEC ON TRUE H	2-B6,R	3-A3,R	5-A1,L			
EXECUTE H	2-P5,L	8-C1,L				
EXT.FAIL H	2-A8,R	8-A1,L				
EXT.HALT L	2-C8,R	3-B2,R	8-D1,L			
EXT.RST L	2-C7,R	8-D2,R				
EXT.TEST L	3-A7,R	3-C7,R	8-A2,R			
EXT.VECTOR L	3-C2,R	8-D1,L				
F=ZERO H	1-C3,L	3-C8,R				
FAIL L	2-A6,L	3-C2,R	4-B8,R	4-C8,R		
G2 L	1-C6,L	1-D3,R				
G3 L	1-C3,R	1-C5,L				
GND	2-B3,R	2-C3,R	6-A5,R	6-A6,R	6-A8,R	6-B8,R
	6-C5,R	6-C6,R	6-C8,R	8-D2,R	8-D2,R	9-A4,R <AC2>
	9-A4,R <AT1>		9-A4,R <BC2>		9-A4,R <BT1>	9-A4,R <CC2>
	9-A4,R <CT1>		9-A4,R <DC2>		9-A4,R <DT1>	9-A4,R <EC2>
			9-A4,R <ET1>		9-A4,R <FC2>	9-A4,R <FT1>
GNDRES 1	5-A2,R	5-A4,R	5-A6,L	5-B4,R	5-C2,R	
HI LTRL L	5-A3,L	5-B4,R				
I/O CLR L	3-D8,R	7-A7,R	7-C5,L	7-C7,R		
INTR H	7-A3,R	7-C4,L				
INTR L	7-C4,L	7-D4,R				
INTRPTMSTR L	3-D7,R	7-C1,L	8-A2,R			
IOC ENABLE H	2-B4,R	3-B3,R	5-B6,L			
IOC SEL 0 H	1-A6,R	1-A8,R	3-C3,R	5-C3,L	7-C6,R	8-A7,L
IOC SEL 1 H	1-A6,R	1-A8,R	3-C3,R	5-C3,L	7-C6,R	8-A7,L
IOC SEL 2 H	1-B6,R	1-B8,R	3-C3,R	5-C3,L	7-C6,R	8-B7,L
JUMP OP 1 H	3-C3,R	4-B8,R	4-D8,R	5-B6,L		
LD BD1 L	2-C2,L	8-A1,L				
LD BUFFER L	2-C2,L	8-D8,R				
LD DBAR L	2-A2,L	8-D8,R				
LD DCR L	2-A2,L	8-A7,L				
LD DCR1 L	2-A2,L	8-A4,R				
LD RTCS L	2-A2,L	8-A7,L				
LD SERDES L	2-A2,L	8-D8,R				
LD UBADDR L	2-A2,L	6-A8,R	8-A1,L			
LD UBAR L	2-A2,L	8-D8,R				
LD UBDATA L	2-A2,L	2-A6,R	6-A3,R			
LD UCR L	2-A2,L	8-A5,R				
LED 1 L	8-A2,R	8-D4,L				

LED 2 L	8-A2,R	8-D4,L				
LED 4 L	8-A2,R	8-C4,L				
LED 8 L	8-A2,R	8-C4,L				
MCLR H	7-B3,L					
MSTR H	6-A6,R	7-B1,L	7-B7,R			
NPR REQ H	7-C5,L					
ODD PARITY H	3-A2,L					
OVERRUN H	3-B7,R	8-C7,L				
P2 L	1-C6,L	1-D3,R				
P3 L	1-C3,R	1-C5,L				
PADR 0 H	4-D2,L	5-A5,R	5-A8,R	5-C5,R	5-C8,R	5-D5,R
	5-D8,R					
PADR 1 H	4-D2,L	5-A5,R	5-A8,R	5-C5,R	5-C8,R	5-D5,R
	5-D8,R					
PADR 10 H	4-B2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-C8,R					
PADR 11 H	4-B2,L					
PADR 2 H	4-D2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-D5,R
	5-D8,R					
PADR 3 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-D5,R
	5-D8,R					
PADR 4 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-D5,R
	5-D8,R					
PADR 5 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-D5,R
	5-D8,R					
PADR 6 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-D5,R
	5-D8,R					
PADR 7 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-D8,R					
PADR 8 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-C8,R					
PADR 9 H	4-C2,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-C8,R					
PADR1 11 H	4-B1,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-C8,R					
PADR1 12 H	4-A1,L	5-A5,R	5-A8,R	5-B5,R	5-B8,R	5-C5,R
	5-C8,R					
PADR2 11 H	4-A1,L	5-A5,R	5-A8,R			
PADR2 12 H	4-A1,L	5-A5,R	5-A8,R			
PAGE H	2-C6,L	4-A3,R				
PASS H	3-D4,L					
PASS TEST H	2-B6,R	3-D4,L	4-B8,R	4-C8,R	8-C2,R	
PASS TEST L	2-B6,R	3-B2,R	3-D4,L			
PR 28 H	3-B3,R	5-A6,L				
PR 29 H	3-B3,R	5-A6,L				
PR 30 H	3-B3,R	5-A6,L				
PR 31 H	3-B3,R	5-A6,L				
PROBE 1 H	4-A1,L	8-C1,L				
PROCCLK L	1-B7,R	2-A6,R	2-B2,R	2-C4,L	3-C8,R	8-A1,L
PROM ENBL H	4-A1,L					
PRTYERR H	3-D7,R	7-C6,L				
PURGED L	3-D7,R	7-D3,L				
R/W UBDATA L	2-A5,L	7-A7,R				
RA=RB L	5-B3,L	5-D3,R				
RAM 15 H	1-C3,L	1-C7,R				
RAM PE L	3-B7,R	5-B2,R	8-C7,L			
RAM PE1 L	3-D2,R	5-B1,L				
RD BS8 L	2-D2,L	8-A1,L				
RD BUFFER L	2-D2,L	8-D8,R				
RD CNST L	2-D2,L	8-B3,R				
RD DCR L	2-C1,L	8-D8,R				

RD DCR1 L	2-C1,L	8-A4,R				
RD ECC RSDU L	2-D2,L	8-D8,R				
RD RTDS L	2-D2,L	8-A7,L				
RD SERDES L	2-D2,L	8-D8,R				
RD UBDATA L	2-A6,R	2-D2,L	6-A3,R			
RD UCR L	2-D1,L	8-A5,R				
RDX0.INIT L	7-D5,L					
RDX0.RUN L	7-D5,L					
RDX2.INIT L	7-B2,R	7-D5,L				
RDX2.RUN L	7-D5,L					
RECV EPR H	3-B7,R	8-C7,L				
RESET L	2-A6,L	3-C2,R	4-B6,R	4-D6,R		
RETURN L	4-D7,L					
RST TIMER H	3-B1,L					
RST1 L	2-C6,L	2-C7,R	7-B7,R	8-C5,R		
RST2 L	2-C6,L	2-C7,R	8-A7,L			
RTCS RDY H	3-B7,R	8-C7,L				
RTDS RCVD H	3-B7,R	8-C7,L				
RVCC1	1-D3,R	2-C5,R	2-C6,D	2-D4,L	2-D7,R	3-D8,R
	5-A4,R	6-D6,R	7-A7,R	7-C3,R	9-B1,L	
RVCC2	3-A7,R	3-A8,R	3-B1,R	3-C7,R	3-C8,R	4-B3,R
	9-A5,R	9-A6,R	9-B1,L			
RVCC3	3-C4,D	3-D4,D	4-B6,R	4-C6,R	5-B2,D	5-C2,D
	9-B1,L					
SA.CNTR 00 H	3-C5,L					
SA.CNTR 01 H	3-C5,L					
SA.CNTR 02 H	3-C5,L	7-B5,R				
SA.CNTR 03 H	2-C7,R	3-C5,L				
SA.CNTR 04 H	3-C5,L					
SA.CNTR 05 H	3-C5,L					
SA.CNTR 06 H	3-C5,L					
SA.CNTR 07 H	2-B7,R	3-C5,L				
SA.CNTR 08 H	3-B5,L					
SA.CNTR 09 H	3-B5,L					
SA.CNTR 10 H	3-B5,L					
SA.CNTR 11 H	2-B7,R	3-B5,L				
SA.CNTR 12 H	3-B5,L					
SA.CNTR 13 H	3-B5,L					
SA.CNTR 14 H	3-B5,L					
SA.CNTR 15 H	2-B7,R	3-A5,L				
SA.DLY 03 H	2-C6,L	3-B5,R				
SA.DLY 07 H	2-B6,L	3-B5,R				
SA.DLY 11 H	2-B6,L	3-A5,R				
SA.DLY 15 H	2-B6,L	3-B1,R				
SCAN L	3-D7,R	7-D3,L				
SEL LITERAL L	1-A4,R	1-A8,R	5-B2,L			
SENSE H	3-C3,R	5-B6,L				
SEQ ADR 00 H	3-D1,L	4-D2,L	8-C1,L			
SEQ ADR 01 H	3-D1,L	4-D2,L	8-C2,R			
SEQ ADR 02 H	3-D1,L	4-C2,L	8-C1,L			
SEQ ADR 03 H	3-D1,L	4-C2,L	8-C2,R			
SEQ ADR 04 H	4-C2,L	8-C1,L				
SEQ ADR 05 H	4-C2,L	8-C2,R				
SEQ ADR 06 H	4-C2,L	8-C1,L				
SEQ ADR 07 H	4-C2,L	8-C2,R				
SEQ ADR 08 H	4-C2,L	8-C1,L				
SEQ ADR 09 H	4-B2,L	8-C2,R				
SEQ ADR 10 H	4-B2,L	8-C1,L				
SEQ ADR 11 H	4-B2,L	8-C2,R				
SEQ CLK L	2-B2,R	2-C4,L	3-C5,R	4-B3,R	4-B6,R	4-C6,R
	5-A2,R	5-A4,R	5-A7,R	5-B4,R	5-B7,R	5-C2,R	5-C6,R	8-A1,L

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK'D.	DATE	BOARD LOCATION:	

TITLE: UDA PR

DSK:PR.T2P[4,243] 21-NOV-83 17:12 NEXT HIGHER ASSEMBLY: SHEET 1 OF 18

FIRST USED ON OPTION/MODEL: UDA52 B-DD-M7485-0

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F

8 7 6 5 4 3 2 1

	8-D1,L						
SET IOC H	1-B6,R	1-B8,R	3-C3,R	5-C3,L	7-B7,R	8-B7,L	
SSYNC EN H	7-D3,L	7-D6,R					
SSYNC H	7-A2,L						
SSYNC L	3-D7,R	7-A1,L	7-B7,R	7-C2,R			
START L	7-A6,L						
TEST COND 0 H	3-A7,R	5-A6,L					
TEST COND 1 H	3-A7,R	5-A6,L					
TEST COND 2 H	3-A7,R	5-A6,L					
TEST COND 3 H	3-B8,R	5-A6,L					
TEST TRUE H	3-D6,R	5-B6,L					
TIME ERR L	3-C1,L	5-B2,R					
TIMEOUT L	3-D2,R	5-B1,L					
TIISYN H	6-B4,L	7-A2,L					
U.PAGE H	2-C7,R	7-C5,L					
UA00 H	6-D7,L	8-B3,R					
UA01 H	6-A7,L	7-A3,R	8-B3,R				
UA02 H	6-A7,L	7-A3,R	8-B3,R				
UA03 H	6-A7,L	6-B4,L	8-B3,R				
UA04 H	6-A7,L	6-B4,L	8-B3,R				
UA05 H	6-B4,L	6-B7,L	8-B3,R				
UA06 H	6-B7,L	6-C4,L	8-B3,R				
UA07 H	6-B7,L	6-C4,L	8-B3,R				
UA08 H	6-B7,L	6-C4,L	8-B3,R				
UA09 H	6-B5,L	6-D7,L	8-B3,R				
UA10 H	6-B5,L	6-D7,L					
UA10 L	6-D6,L	8-B3,R					
UA11 H	6-B5,L	6-C7,L					
UA11 L	6-C6,L	8-B3,R					
UA12 H	6-C5,L	6-C7,L					
UA13 H	6-C5,L	6-C7,L					
UA14 H	6-C5,L	6-C7,L					
UA15 H	6-C5,L	6-C7,L					
UA16 H	6-C4,L	8-D4,L					
UA17 H	6-B5,L	8-D4,L					
UBMASTER L	3-D7,R	7-C1,L	8-A2,R				
UCODE.16K H	4-A4,R	8-D4,L					
UDATARDY H	3-D7,R	7-A5,L					
UPROC H	2-C2,R	2-D4,L	3-C2,R	3-C8,R	3-D2,R	4-A4,R	
	4-C8,R	8-C2,R					
UPROC L	2-A8,R	2-C2,R	2-C4,L	3-A8,R	3-B2,R	3-B8,R	
	3-C2,R						
UTEST H	3-C7,R	7-C5,L					
WRTX0.INIT L	7-D5,L						
WRTX0.RUN L	7-D5,L						
WRTX2.INIT L	7-A8,R	7-D5,L					
WRTX2.RUN L	7-D5,L						
XFER L	7-A8,R						

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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 21-NOV-83	ENG.	DATE 21-NOV-83
CHK'D.	DATE	BOARD LOCATION: SHEET 12 OF 12	

TITLE: UDA PR

DSK:PR.T2P[4,243] 21-NOV-83 17:12 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA52 B-DD-M7485-0

SIZE	CODE	NUMBER	REV.
K	CS	M7485-0-1	F

DRAWING NUMBER	QTY SHTS	PART NO.	TITLE	REVISIONS
K-DD-M7486-0-0	1		UDA S1	M
	-	M7486-00	UDA SI (PART REV)	H4
K-PL-M7486-0-DBP	3		UDA SI	L
D-UA-M7486-0-0	2		UDA SI	J
K-CS-M7486-0-1	15		UDA SI	J
K-PC-M7486-0-DBI	-		P C DATA BASE	C
B-DD-5015402-0-0	1		ETCHED CIRCUIT BOARD	D

NOTES:

REVISION HISTORY	ECO	CXS 01 18 09	REV
	DATE	24 JAN 86	

OPTIONS:	NEXT HIGHER DOC.	FILE NAME:
UDA50-A		DDM748600.M

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DRN: W MAJOR	DATE: 24 JAN 86	d i g i t a l
CHK'D: SUE BOURBEAU	DATE: 24 JAN 86	TITLE: UDA S1
DES. ENG: J. VAGAIS	DATE: 24 JAN 86	
RESP. ENG: J. VAGAIS	DATE: 24 JAN 86	DOCUMENT NUMBER
MFG. ENG: PAM GOMEZ-GIL	DATE: 24 JAN86	SIZE: K | CODE: DD | NUMBER: M7486-0-0 | REV: M
		SPEC: I DE I

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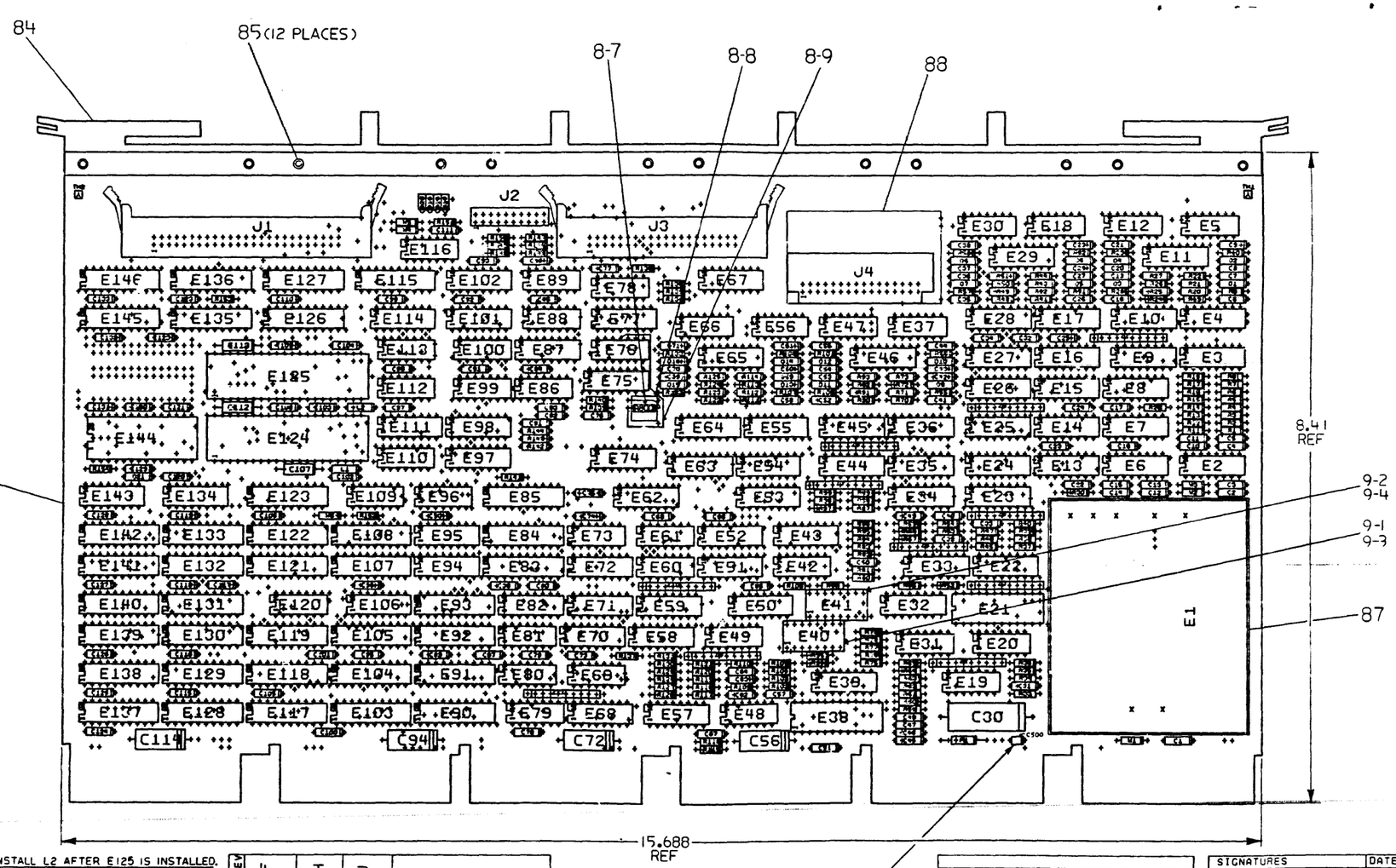
COMPONENT SIDE VIEW



NOTES: 1. INSTALL L2 AFTER E125 IS INSTALLED.
2. SPARES ARE: E2, E6, E7, E14, E15, E67, E74, E75, E97, E98, E111, E134, W4, C102, C103, R3, R12, R14, R15, R30, R54, R67-R69, R84-R86, R97-R99, R140, R142-R144, R148.
3. C5C0 WILL BE HAND INSERTED.

STEP E	↑ Y AXIS ____ STEP ___ TIMES
REPEAT	→ X AXIS ____ STEP ___ TIMES

CHK	CHANGE NO	REV
1882	ECO M7486-CX007 J.R. 15 NOV83 J.VAGIAS	F
	ECO M7486-CX008 WM 17 APR84 J.VAGIAS	H
	M7486-CX009 WM 9 NOV84 J.VAGIAS	J

ETCH REV. C1-P3

SIGNATURES	DATE
DRN.	
CHK'D	
MECH.ENG.	
PROJ.ENG.	
PROD. W. E.	
SCALE 1.5/1	
SHT. 1 OF 2	
NEXT HIGHER ASSY. B-DD-M7486-0-0	

digital

TITLE UDA SI

SIZE	CODE	NUMBER	REV
D	UA	M7486-0-0	J

1 MS#400534C

DUA M7486-0-0

1 of 2

M7486-CX008

COMPONENT DELETES

8- 1 DELETE E40 (16-20546-01)
8- 2 DELETE E41 (16-20546-01)

COMPONENT ADDS

8- 5 ADD E40 (16-23207-01)
8- 6 ADD E41 (16-23207-01)
8- 7 ADD R800(13-00219-00) SOLDERING PIN 1 INTO
FEEDTHRU BELOW E75 PIN 6 AND PIN 2 INTO
FEEDTHRU BELOW THAT
8- 8 ADD MYLAR (74-29181-01)(.500 X .500) UNDER R800

WIRE ADDS - SIDE 1

8- 9 ADD WIRE FROM 2ND PTH HOLE BELOW E75 PIN 6 TO E76 PIN 11

PART MARKING

8-10 AFTER ALL REWORK IS COMPLETED MARK MODULE REV H2

ECO M7486-CX009

COMPONENT DELETES: (SIDE 1)

9-1 DELETE E40 (1623207-01)
9-2 DELETE E41 (1623207-01)

COMPONENT ADDS: (SIDE 1)

9-3 ADD E40 (1623779-01)
9-4 ADD E41 (1623779-01)

PART MARKING

9-5 AFTER ABOVE REWORK IS COMPLETE,
MARK MODULE REV H3

AUTOMATED BY VAXKPL (V1.0) — P A R T S L I S T — SHEET A1 OF A3

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 00 H4	REFERENCE DESIGNATORS
1	1	B-DD-5015402-0	50-15402-01	D	DRILL AND ETCH	1	
2	2		10-01796-00		50 MFD 25V +75-10% AL EL	1	C30
3	3		10-12784-00		.047 MFD 50V +80-20% CER	113	C2-C8,C10,C11,C13-C20,C22-C28,
							CONT C31-C37,C39-C43,C45-C54,
							CONT C57-C60,C62-C70,C73-C93,
							CONT C95-C101,C104-C106,C108-C111,
							CONT C115-C133
4	4		10-10279-00		.47 MFD 25V 20% CER	1	
5	5		10-13466-11		.22 MFD 50V +80-20% Z5U CER	3	C107,C112,C113
6	6		10-15878-00		.01 MFD 50V +80-20% CER	8	C9,C21,C29,C38,C44,C55,C61,C71
7	7		10-16549-00		47 MFD 10V +50-10% AL EL	4	C56,C72,C94,C114
8	8		11-04860-00		VZ= 3.3 5% 400 MW 1N746A	8	D1,D2,D5,D6,D9,D10,D13,D14
9	9		11-05275-00		PIV= 60 IO=300 MA -15NS	8	D3,D4,D7,D8,D11,D12,D15,D16
10	10		11-10836-00		VZ= 12.0 5% 400 MW 1N759A	1	D21
11	11		11-14136-01		LED 6.5MA 5V 1.2MCD	4	D17-D20
12	12		12-05747-00		FUSE PICO 5.0 A 125V AXIAL LEA	1	F1
13	13		12-10385-01		*** THIS ITEM IS NOT USED ***	-	
14	14		12-12965-04		PCB,HEADER 20PIN(2X05).100CC 90D	1	J2
15	15		12-14314-00		*** THIS ITEM IS NOT USED ***	-	
16	16		16-23779-01		PULSE GENERATOR 20NS ECL	2	E40,E41
17	17		12-16832-02		PCB,HEADER 40POS(2X20).100CC 90D	1	J3
18	18		12-16832-03		PCB,HEADER 50POS(2X25).100CC 90D	1	J1
19	19		12-18348-00		PCB,HEADER 32PIN(2X16).100CC 90D	1	J4
20	20		13-00202-00		47.0 .25 W 5.0 % CF	16	R19,R22,R24,R26,R41,R44,R48,
							CONT R50,R70,R72,R90,R92,R111,R113,
21	21		13-00247-00		120.0 .25 W 5.0 % CF	18	CONT R122,R124 R35,R37,R39,R53,R63,R66,R76,
							CONT R79,R80,R94,R109,R110,R115,
							CONT R119,R120,R126,R127,R130
22	22		13-00271-00		220.0 .25 W 5.0 % CF	8	R28,R29,R57,R58,R100,R101,R132,
							CONT R133
23	23		13-00316-00		470.0 .25 W 5.0 % CF	12	R1,R2,R4,R5,R11,R87-R89,R129,

REVISION HISTORY			KPL MODULE FORMAT	SECTION A OF A	DRN: SUE BOURBEAU	D I G I T A L
ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX		DATE: 09-JUL-82	
	INITIAL	A	[A] 00 [M]		CHK'D: RON MICHAUD	TITLE PARTS LIST
JP	M7486-CX001	B	[B] [N]		DATE: 09-JUL-82	UDA SI
JP	M7486-CX002	C	[C] [P]		DES.ENG: JIM PULSIPHER	DOCUMENT NUMBER
JP	M7486-CX003	D	[D] [Q]		DATE: 09-JUL-82	SIZE CODE NUMBER REV
JP	M7486-CX004	E	[E] [R]		RESP.ENG.: JIM PULSIPHER	K PL M7486-0-DBP L
JP	M7486-CX006	F	[F] [S]		DATE: 09-JUL-82	
JV	M7486-CX007	H	[H] [T]		MFG.ENG: ROY BOWERS	RELEASE DATE: 28-JAN-86
JV	M7486-CX008	J	[J] [V]		DATE: 09-JUL-82	RELEASE STATUS: RELEASED
JV	M7486-CX009	K	[K] [W]			
JV	M7486-CX010	L	[L] [Y]			

BASIC PART NUMBER:	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:	EDIT #
M7486	D-UA-M7486-0-0	K-DD-M7486-0-0	Z3696L.PLS	7

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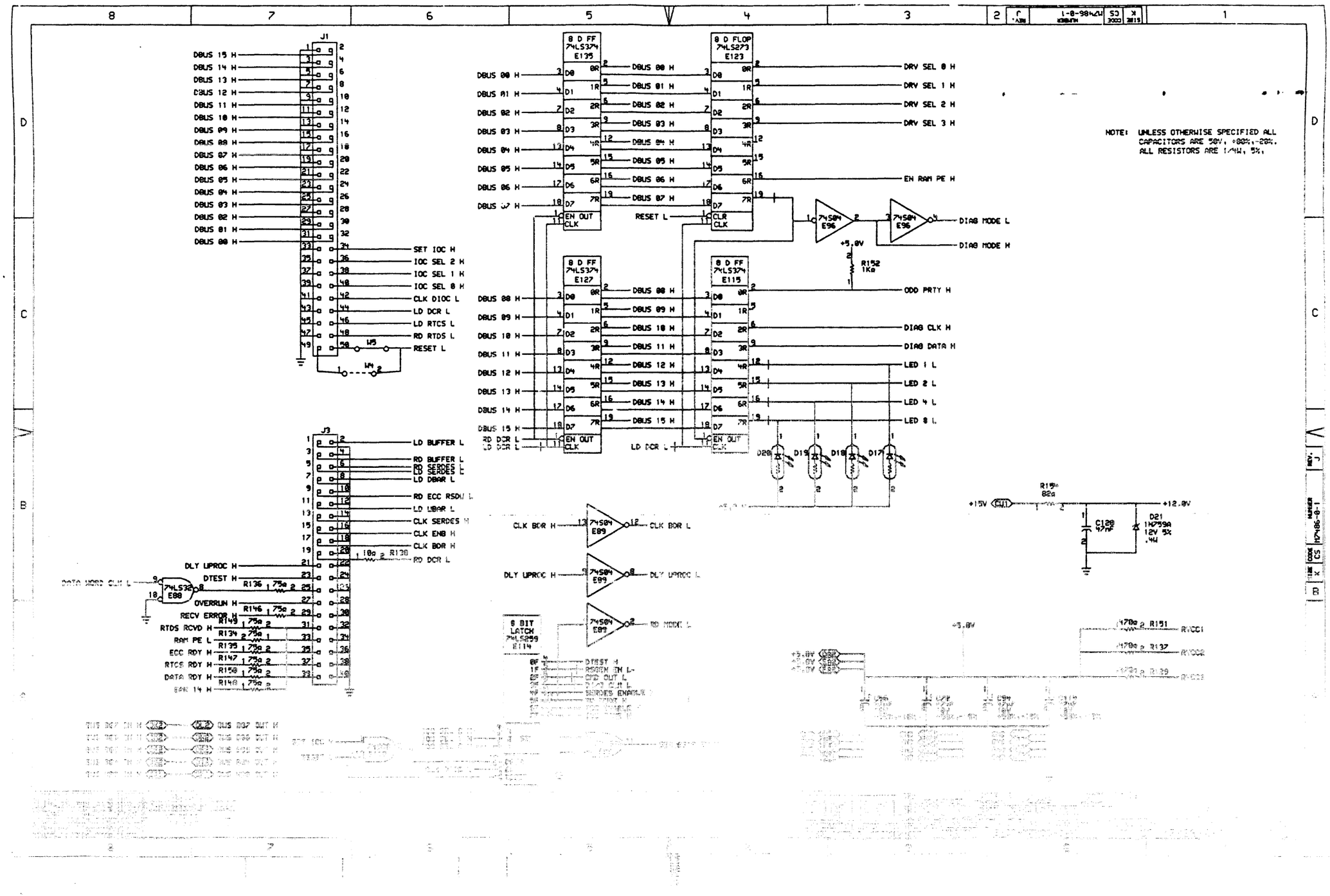
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 00 H4	REFERENCE DESIGNATORS
							CONT R137,R139,R151
24	24		13-00365-00	1.0 K	.25 W 5.0 % CF	1	R152
25	25		13-00430-00	3.0 K	.25 W 5.0 % CF	1	R153
26	26		13-00479-00	10.0 K	.25 W 5.0 % CF	1	R145
27	27		13-01317-00	10.0	.25 W 5.0 % CF	2	R138,R141
28	28		13-01477-00	82.0	.25 W 5.0 % CF	5	R6,R13,R17,R18,R154
29	29		13-02379-00	75.0	.25 W 5.0 % CF	7	R134-R136,R146,R147,R149,R150
30	30		13-02873-00	261.0	.25 W 1.0 % RN55D-F10	8	R33,R34,R60-R62,R64,R83,R96
31	31		13-02887-00	130.0	.25 W 1.0 % RN55D-F10	4	R7,R8,R16,R23
32	32		13-11522-00	200.0	.25 W 5.0 % CF	18	R36,R40,R45,R47,R52,R75,R77,
							CONT R78,R81,R95,R102,R105,
							CONT R116-R118,R121,R128,R131
33	33		13-12114-01	R NETWORK	8-470 5.0 % 10PIN	11	Z1-Z11
34	34		13-12929-00	62.0	.25 W 5.0 % CF	8	R9,R10,R31,R32,R55,R56,R107,
							CONT R108
35	35		13-18341-01	162.0	.25 W 1.0 % RN55D-F10	8	R38,R46,R59,R65,R82,R103,R104,
							CONT R106
36	36		13-18341-02	187.0	.25 W 1.0 % RN55D-F10	16	R20,R21,R25,R27,R42,R43,R49,
							CONT R51,R71,R73,R91,R93,R112,R114,
							CONT R123,R125
37	37		13-18342-00	R NETWORK	8-56.2 8-316 16PIN	4	E11,E29,E46,E65
38	38		16-11257-01	CHOKE(CERAMIC BEAD)AXIAL LEAD,ON		2	L1,L2
39	39		16-17533-00	DELAY= 250NS,5TAPS 14PIN DIP		1	E112
40	40		16-18336-00	DELAY= 10NS		4	E20,E31,E48,E49
41	41		16-18337-00	DELAY= 18NS		2	E19,E42
42	42		16-18343-00	PULSE XFMR,RATIO 1:1:1, 80UH		8	E5,E12,E18,E30,E37,E47,E56,E66
43	43		19-10534-00	74S04	INVERTER GATE-HEX 1I	2	E89,E96
44	44		19-10544-00	74S74	FF-D DUAL,EDGE TRIGG	6	E73,E76,E78,E79,E86,E116
45	45		19-10545-00	74S112	FF-JK DUAL,EDGE TRIG	1	E68
46	46		19-10956-00	74S151	MUX 1 OF 8	1	E62
47	47		19-10957-00	74S175	FF-D QUAD COMMON CLO	2	E72,E82
48	48		19-11399-00	10102	NOR GATE,QUAD 2IN	4	E8,E26,E44,E45
49	49		19-11401-00	10104	AND GATE,QUAD 2IN	1	E13
50	50		19-11404-00	10107	XOR/NOR GATE,3-2IN	1	E32
51	51		19-11414-00	10124	TTL TO ECL TRNSLTR	3	E52,E53,E58
52	52		19-11415-00	10125	ECL TO TTL TRNSLTR	2	E51,E59
53	53		19-11420-00	10174	DUAL 4 TO 1 MUX	2	E33,E39
54	54		19-11573-00	74S280	PARITY GEN/CHKR,9BIT	2	E81,E120
55	55		19-11676-00	74S139	DECODER-DUAL TWO-INP	1	E143
56	56		19-11712-00	74S51	AND-OR GATE-INVERT D	4	E80,E99,E109,E113
57	57		19-12389-00	74S08	AND GATE-QUAD 2IN,PO	1	E110
58	58		19-12801-00	LS02	NOR-GATE-QUAD 2IN	1	E100
59	59		19-12816-00	LS32	OR GATE-QUAD 2IN,POS	1	E88
60	60		19-12833-00	LS109	FF-JK DUAL,POS EDGE	1	E87
61	61		19-10548-00	74S157	MUX 1 OF 2 (QUAD)	1	
62	62		19-12848-00	LS158	MUX 1 OF 2 (QUAD)	1	E101
63	63		19-12853-00	LS175	FF-D QUAD	1	E102
64	64		19-12860-00	LS259	LATCH 8BIT	1	E114
65	65		19-12863-00	LS273	FF-D OCTAL W/CLEAR	2	E85,E123
66	66		19-12864-00	LS279	LATCH,QUAD-S-R	1	E77

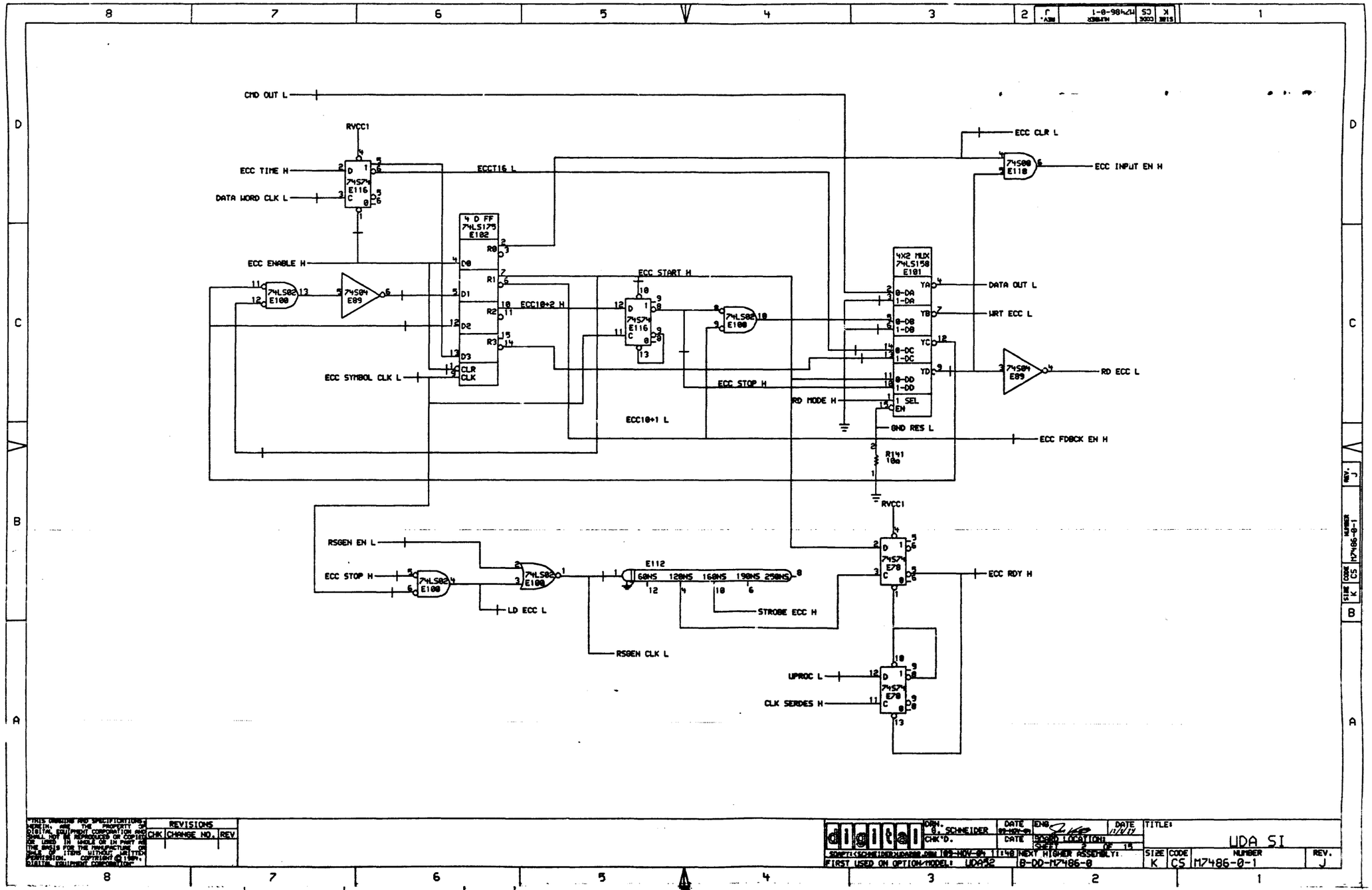
D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							UDA SI		M	PL	M7486-0-DBP	L

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV		DESCRIPTION	QTY PER VAR/REV 00 H4	REFERENCE DESIGNATORS
67	67		19-13340-00		74S32	OR GATE-QUAD 2IN	2	E60,E69
68	68		19-13671-01		74S374	FF-D,OCTAL,TRI STATE	8	
69	69		19-13939-00		LS191	COUNTER,SYNCHR. UP/D	2	E94,E95
70	70		19-14082-01		74S163	COUNTER,SYNCH,UP/DOW	2	E70,E71
71	71		19-14214-00		LS374	FF-D OCTAL EDGE TRIG	7	E83,E84,E115,E126,E127,E135,
							CONT	E146
72	72		19-15193-00		LS244	DRIVER,LINE,OCTAL,TR	2	E136,E145
73	73		19-16574-00		10114	RECEIVER,LINE,TRIPLE	8	E4,E10,E17,E25,E28,E36,E55,E64
74	74	SEE NOTE 1	19-17043-02	DC	018	SERIALIZER/DESERIALI	2	
75	75		19-17289-00		100102	OR/NOR GATE,QUINT,2	2	E21,E38
76	76		19-17839-00		10192	DRIVER, LINE, QUAD D	8	E3,E9,E16,E24,E27,E35,E54,E63
77	77		19-17956-00		LS280	PARITY GEN/CHK,9BIT,	1	E61
78	78		19-18352-00	PS	4317	DC-DC CONVERTER	1	E1
79	79		19-18353-00		10231	FF-D, MASTER-SLAVE,	6	E22,E23,E34,E43,E50,E57
80	80		21-15102-00	DEC	DC309	NMOS CUSTOM LSI FOR	1	E144
81	81		21-18054-03			16K MOS RAM 55NS 2	2	E90,E91
82	82		21-19250-00			4KX4 STATIC RAM 55NS	16	E92,E93,E103-E105,E117-E119,
							CONT	E128-E131,E137-E140
83	83		90-09185-00			JUMPER, WIRE, INSULATED, BLACK B	5	W1-W3,W5,W6
84	84		12-16988-02			HANDLE,MODULE,HEX TWO EJECTORS	1	
85	85		90-00024-01			EYELET,ROLLED 0.121ODX0.192	12	
86	86		10-10274-02			1 MFD 50V +80-20% CER	1	C500
87	87		12-16188-03			TAPE,MYLAR ADH BK 3.00"X2.50"	1	
88	88		12-16188-01			TAPE,MYLAR ADH BK 1.00"X2.00"	1	
89	89		13-00219-00			68.0 .25 W 5.0 % CF	1	R800
90	90		12-16188-02			TAPE,MYLAR ADH BK .50"X .50"	1	
91	91					*** THIS ITEM IS NOT USED ***	-	

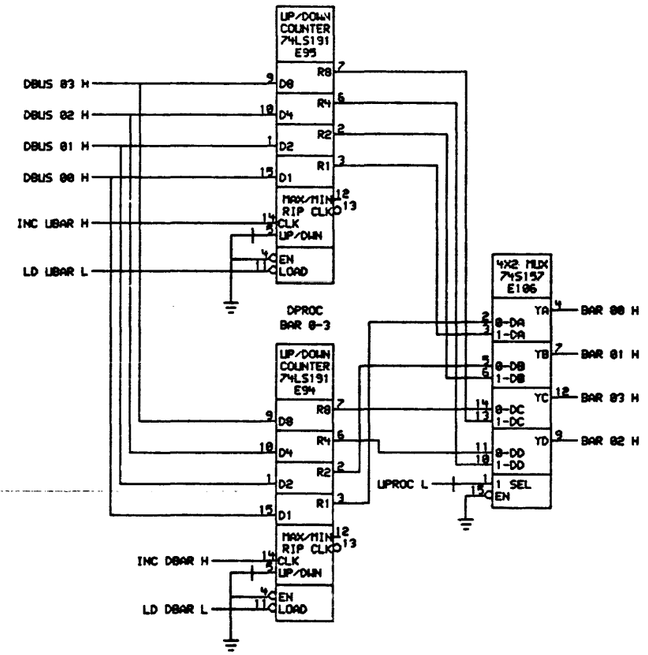
1 GEN: 1. 1917043-00 MAY BE USED IN E124 ONLY UNTIL STOCK IS DEPLETED
2 GEN: ONCE STOCK IS DEPLETED, USE ONLY 1917043-02

D	I	G	I	T	A	L	TITLE	SIZE	CODE	DOCUMENT NUMBER	REV
							UDA SI	K	PL	M7486-0-DBP	L
							SECTION A OF A				


J1
DBUS 15 H
DBUS 14 H
DBUS 13 H
DBUS 12 H
DBUS 11 H
DBUS 10 H
DBUS 09 H
DBUS 08 H
DBUS 07 H
DBUS 06 H
DBUS 05 H
DBUS 04 H
DBUS 03 H
DBUS 02 H
DBUS 01 H
DBUS 00 H
SET IOC H
IOC SEL 2 H
IOC SEL 1 H
IOC SEL 0 H
CLK DIOC L
LD DCR L
LD RTCS L
RD RTDS L
RESET L
W5
W4
8 D FF 74LS374 E135
8 D FLOP 74LS273 E123
8 D FF 74LS374 E127
8 D FF 74LS374 E115
DRV SEL 0 H
DRV SEL 1 H
DRV SEL 2 H
DRV SEL 3 H
EN RAM PE H
DIAG MODE L
DIAG MODE H
+5.0V
R152 1KΩ
ODD PRTY H
DIAG CLK H
DIAG DATA H
LED 1 L
LED 2 L
LED 4 L
LED 8 L
D20
D19
D18
D17
NOTE: UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE 50V, +80%,-20%. ALL RESISTORS ARE 1/4W, 5%.
J3
LD BUFFER L
RD BUFFER L
LD SERDES L
LD DBAR L
RD ECC RSDU L
LD LBAR L
CLK SERDES H
CLK ENB H
CLK BDR H
RD DCR L
DLY UPROC H
DTEST H
OVERRUN H
RECV ERROR H
RTDS RCVD H
RAM PE L
ECC RDY H
RTCS RDY H
DATA RDY H
DATA WORD CLK L
74LS32 E88
CLK BDR H
DLY UPROC H
8 BIT LATCH 74LS259 E114
+15V (OUT)
+12.0V
C128 47nF
D21 1N759A 12V 5%


CMD OUT L
RVCC1
ECC TIME H
DATA WORD CLK L
74S74 E116
ECCT16 L
4 D FF 74LS175 E102
ECC ENABLE H
74LS02 E100
74S04 E89
ECC SYMBOL CLK L
ECC START H
ECC10+2 H
ECC10+1 L
ECC STOP H
4X2 MUX 74LS158 E101
RD MODE H
GND RES L
R141 10Ω
ECC CLR L
74S00 E110
ECC INPUT EN H
DATA OUT L
WRT ECC L
RD ECC L
ECC FDBCK EN H
RSGEN EN L
ECC STOP H
LD ECC L
E112
60NS 120NS 160NS 190NS 250NS
STROBE ECC H
RSGEN CLK L
74S74 E78
ECC RDY H
UPROC L
CLK SERDES H
REVISIONS
CHK CHANGE NO. REV
DRN. G. SCHNEIDER
CHK'D.
DATE 09-NOV-84
ENG.
DATE 11/1/84
SCARD LOCATION:
SHEET 2 OF 15
TITLE: UDA SI
SIZE K
CODE CS
NUMBER M7486-0-1
REV. J
NEXT HIGHER ASSEMBLY: B-DD-M7486-0
FIRST USED ON OPTION/MODEL: UDA52

BUFFER MEMORY



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REVISIONS		
CHK	CHANGE NO.	REV

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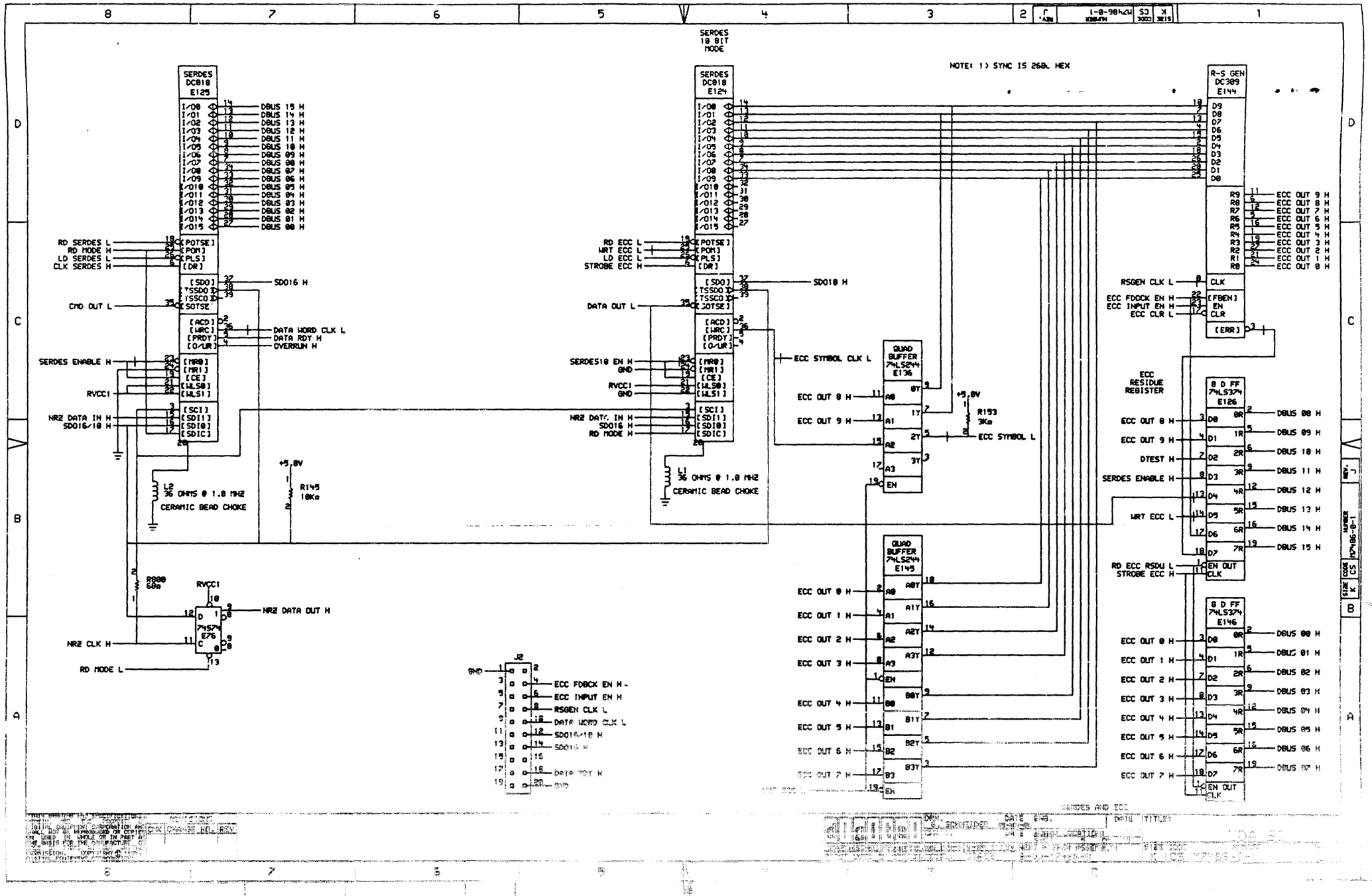
DRN. G. SCHNEIDER | DATE 09-NOV-84 | ENG. | DATE | TITLE: UDA SI

CHK'D. | DATE | BOARD LOCATION: SHEET 4 OF 15

SOAPT:<SCHNEIDER>UDA84.DBU 09-NOV-84 11:52 | NEXT HIGHER ASSEMBLY: B-DD-M7486-0

FIRST USED ON OPTION/MODEL: UDA52

SIZE	CODE	NUMBER	REV.
K	CS	M7486-0-1	J



SERDES 10 BIT MODE
NOTE: 1) SYNC IS 26BC HEX
SERDES DC018 E125
SERDES DC018 E124
R-S GEN DC309 E144
QUAD BUFFER 74LS244 E136
QUAD BUFFER 74LS244 E145
8 D FF 74LS374 E126
8 D FF 74LS374 E146
74S74 E76
ECC RESIDUE REGISTER
CERAMIC BEAD CHOKE
L2 36 OHMS @ 1.0 MHZ
L1 36 OHMS @ 1.0 MHZ
R145 10KΩ
R153 3KΩ
R800 68Ω
+5.0V
RVCC1
J2
SERDES AND ECC

RTDS
(REAL TIME DRIVE STATUS)

RTDS DATA H
RTDS DATA L
74S51 E80
RVCC2
RTDS CLK H
74S74 E79
RTDS PE H
CLR P1Y L

4 D FF 74S175 E72
RTDS DATA H
RTDS DATA 1 L
DATA SHIFTED INVERTED
RTDS DATA 2 L
RTDS DATA 3 L
AVAILABLE H
INDEX PULSE H

4 D FF 74S175 E82
RTDS DATA 3 L
RTDS DATA 4 L
RTDS DATA 5 L
RTDS DATA 6 L
SECTOR PULSE H
R/W READY H
ATTENTION H
RECEIVER RDY H

QUAD BUFFER 74LS244 E136
DATA XMIT ERROR H
RTCS RDY H
RTDS RCVD H
RECV ERROR H
DBUS 07 H
DBUS 02 H
DBUS 03 H
DBUS 00 H

8 D FF 74LS374 E83
DBUS 06 H
DBUS 05 H
DBUS 04 H
DBUS 15 H
DBUS 01 H
DBUS 00 H
RD RTDS L

RTDS PE H
74S32 E69
SYNCH DET H
HOLD DATA H
RTDS CLK H
+5.0V
211 470Ω
74S74 E86
74S74 E79
74S112 E68
74S112 E68
CLR PTY L
74LS279 E77
RTDS RCVD H

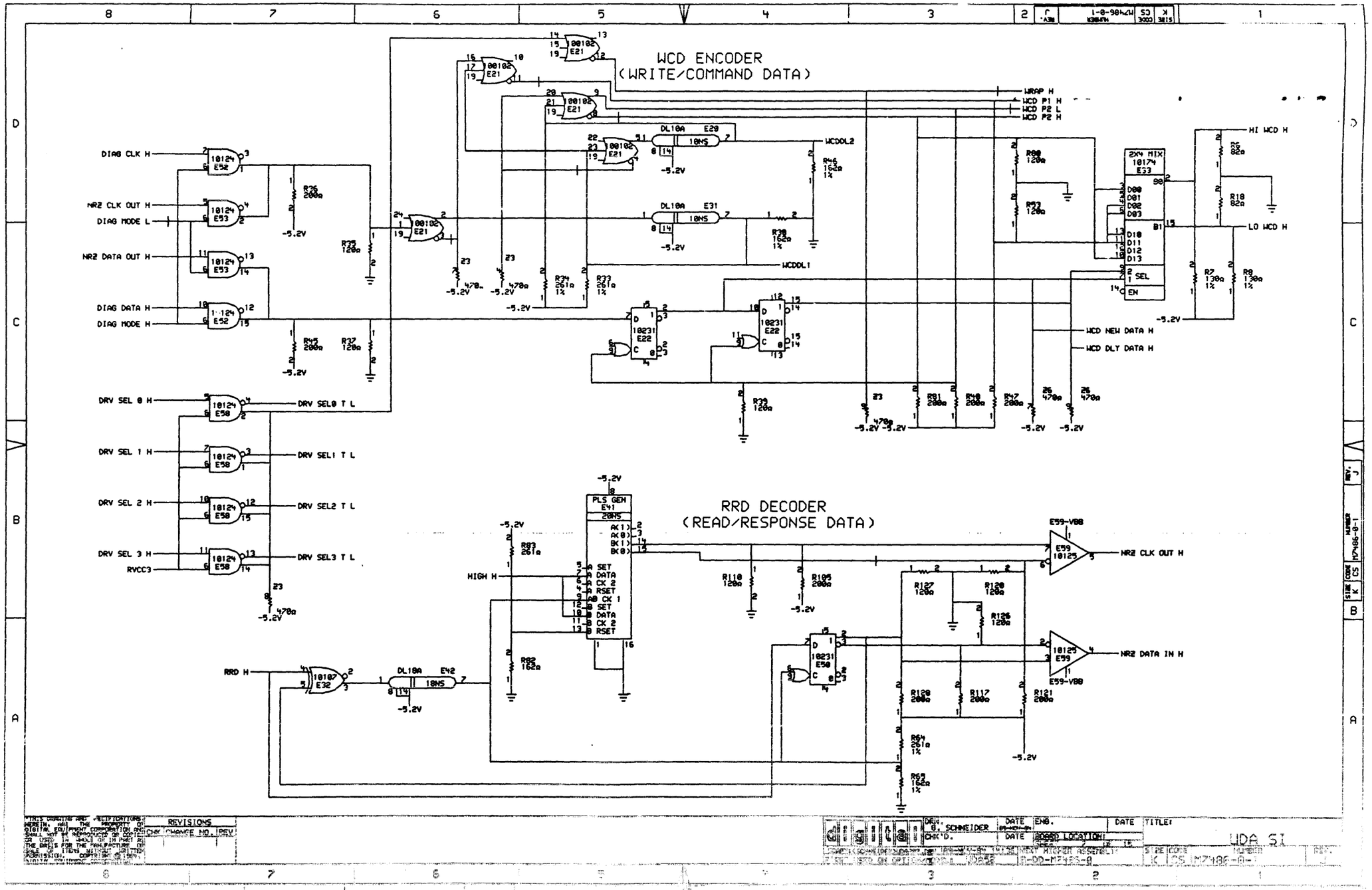
COUNT 7 ZEROES
BIN CTR 74S163 E70
RVCC2
RTDS CLK H
7 ZEROES +1 ONE
SYNC BIT L

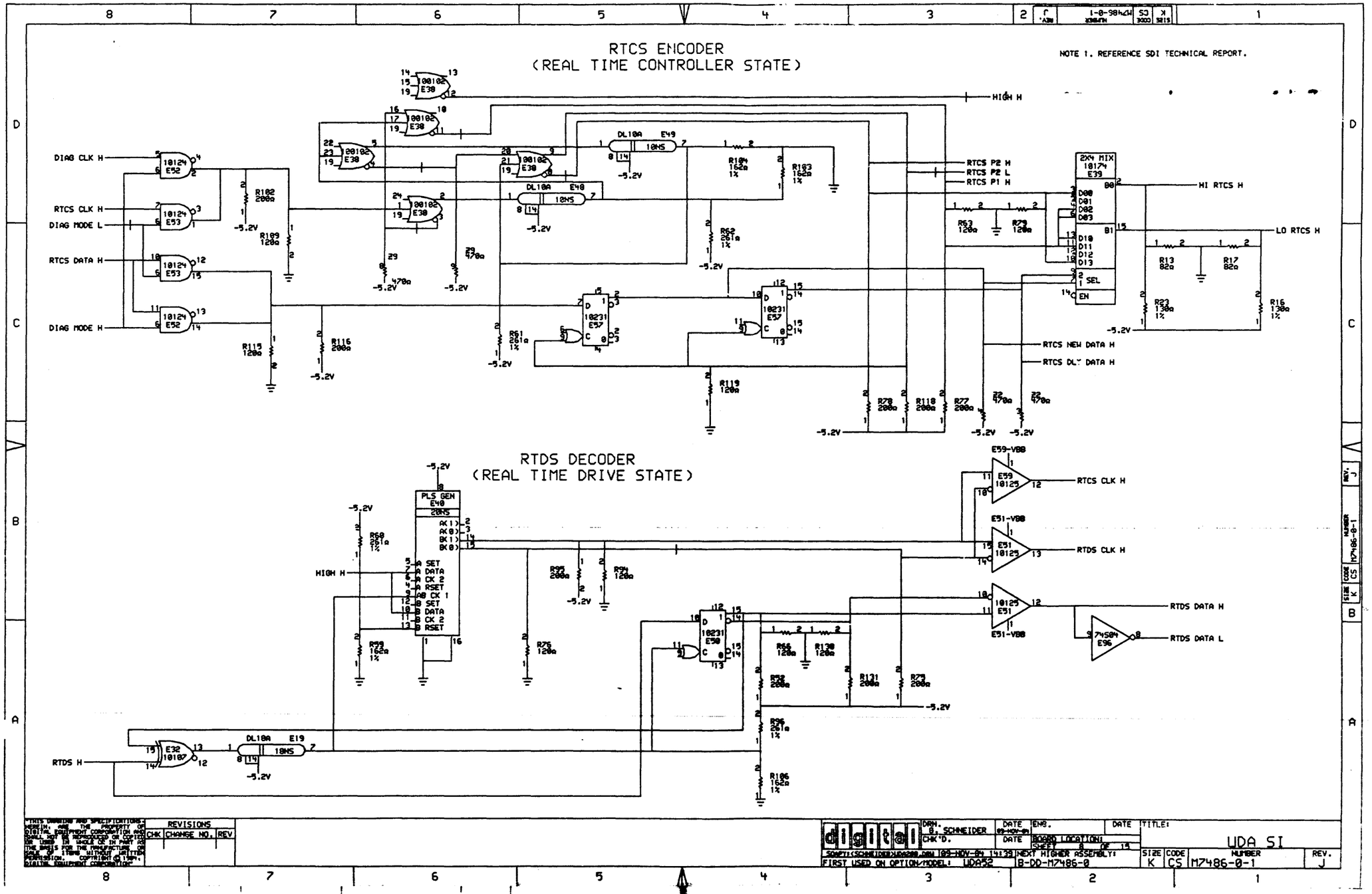
RTCS
(REAL TIME CONTROLLER STATUS)

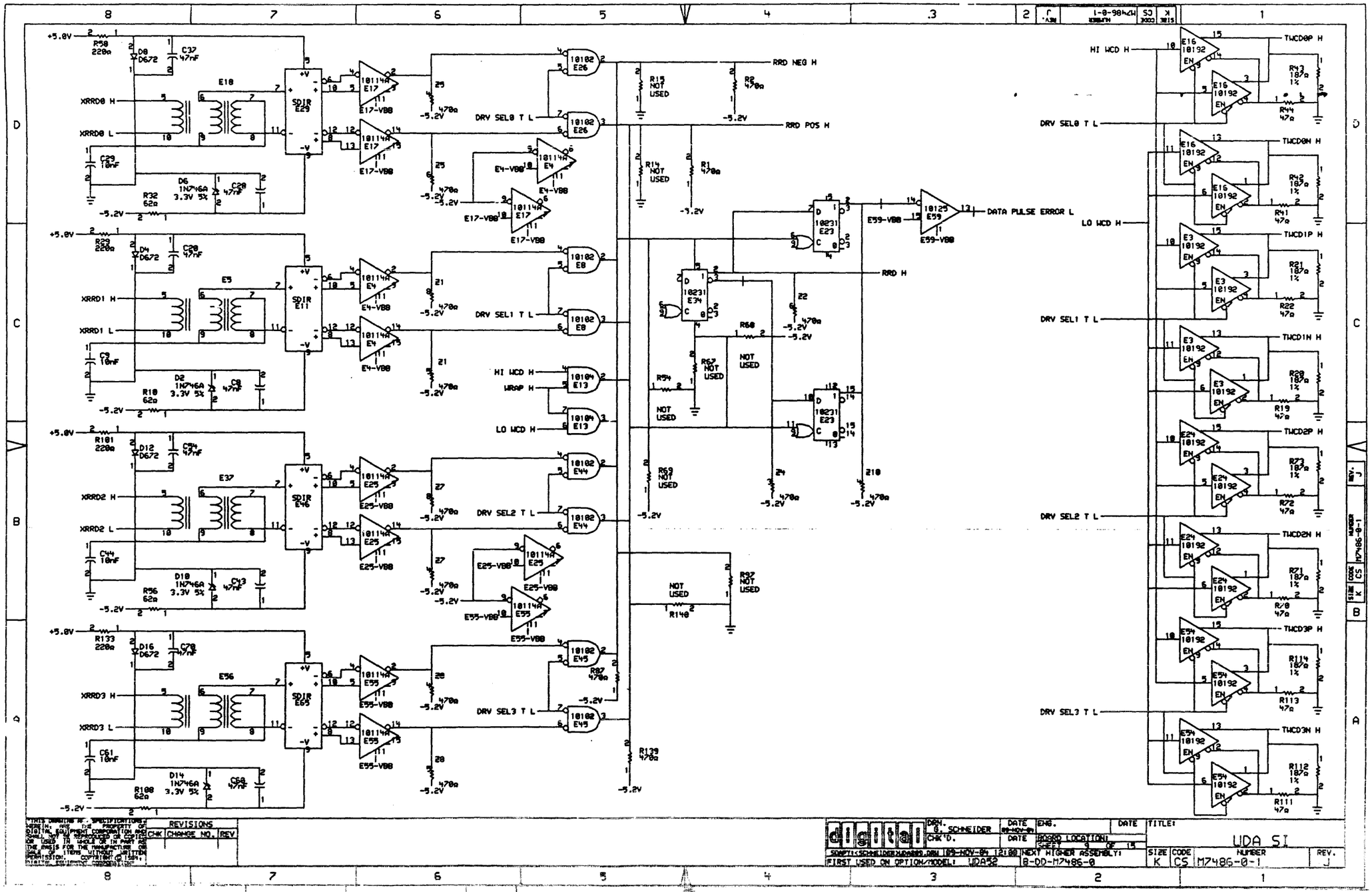
BIN CTR 74S163 E71
RVCC2
RTCS CLK H
RTCS CNT 16 L
74S32 E60
74S04 E96
8 MUX 74S151 E62
RCVR RDY
XMIT GATE
RD GATE
INIT
RESERVED
RESERVED
PARITY
SEL
EN
MRC L
74S74 E73
RTCS DATA H

8 D FF 74LS374 E84
DBUS 00 H
DBUS 01 H
DBUS 02 H
DBUS 03 H
DBUS 04 H
DBUS 05 H
DBUS 06 H
DBUS 07 H
GND RES L
LD RTCS L
8 D FLOP 74LS273 E85
PARITY GEN 74LS280 E61
FEVEN
FODD
EVEN PARITY H
74S00 E110
RTCS CNT 12 H
DATA PULSE ERROR L
74LS279 E77
DATA XMIT ERROR H
REAL TIME PULSE ERROR L
RTCS RDY H
RTDS PE H
SYNCH DET H
74S74 E76
RECV ERROR H
DI/O CLR L

| | | |


WCD ENCODER
(WRITE/COMMAND DATA)
RRD DECODER
(READ/RESPONSE DATA)
DIAG CLK H
NRZ CLK OUT H
DIAG MODE L
NRZ DATA OUT H
DIAG DATA H
DIAG MODE H
DRV SEL 0 H
DRV SEL 1 H
DRV SEL 2 H
DRV SEL 3 H
RVCC3
DRV SEL0 T L
DRV SEL1 T L
DRV SEL2 T L
DRV SEL3 T L
WRAP H
WCD P1 H
WCD P2 L
WCD P2 H
WCDDL2
WCDDL1
HI WCD H
LO WCD H
WCD NEW DATA H
WCD DLY DATA H
HIGH H
RRD H
NRZ CLK OUT H
NRZ DATA IN H
PLS GEN
E41
20NS
2X4 MIX
10174
E33
DL10A
E20
E31
E42
18NS
10124
E52
E53
E58
10107
E32
10231
E22
E50
10125
E59
E59-VBB
-5.2V
REVISIONS
CHK
CHANGE NO.
REV
DRN. B. SCHNEIDER
CHK'D.
DATE
ENG.
BOARD LOCATION
TITLE:
UDA SI
SIZE
CODE
NUMBER
REV.
K
CS
M7486-0-1


RTCS ENCODER
(REAL TIME CONTROLLER STATE)
NOTE 1. REFERENCE SDI TECHNICAL REPORT.
DIAG CLK H
RTCS CLK H
DIAG MODE L
RTCS DATA H
DIAG MODE H
HIGH H
RTCS P2 H
RTCS P2 L
RTCS P1 H
HI RTCS H
LO RTCS H
RTCS NEW DATA H
RTCS DLY DATA H
RTDS DECODER
(REAL TIME DRIVE STATE)
RTCS CLK H
RTDS CLK H
RTDS DATA H
RTDS DATA L
RTDS H
DIGITAL
DRN. B. SCHNEIDER
CHK'D.
ENG.
BOARD LOCATION:
SHEET 8 OF 15
TITLE: UDA SI
SIZE K
CODE CS
NUMBER M7486-0-1
REV. J
FIRST USED ON OPTION/MODEL: UDA52
NEXT HIGHER ASSEMBLY: B-DD-M7486-0
REVISIONS
CHK
CHANGE NO.
REV



REVISIONS		
CHK	CHANGE NO.	REV

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DRN. G. SCHNEIDER DATE 09-NOV-84 ENG. DATE

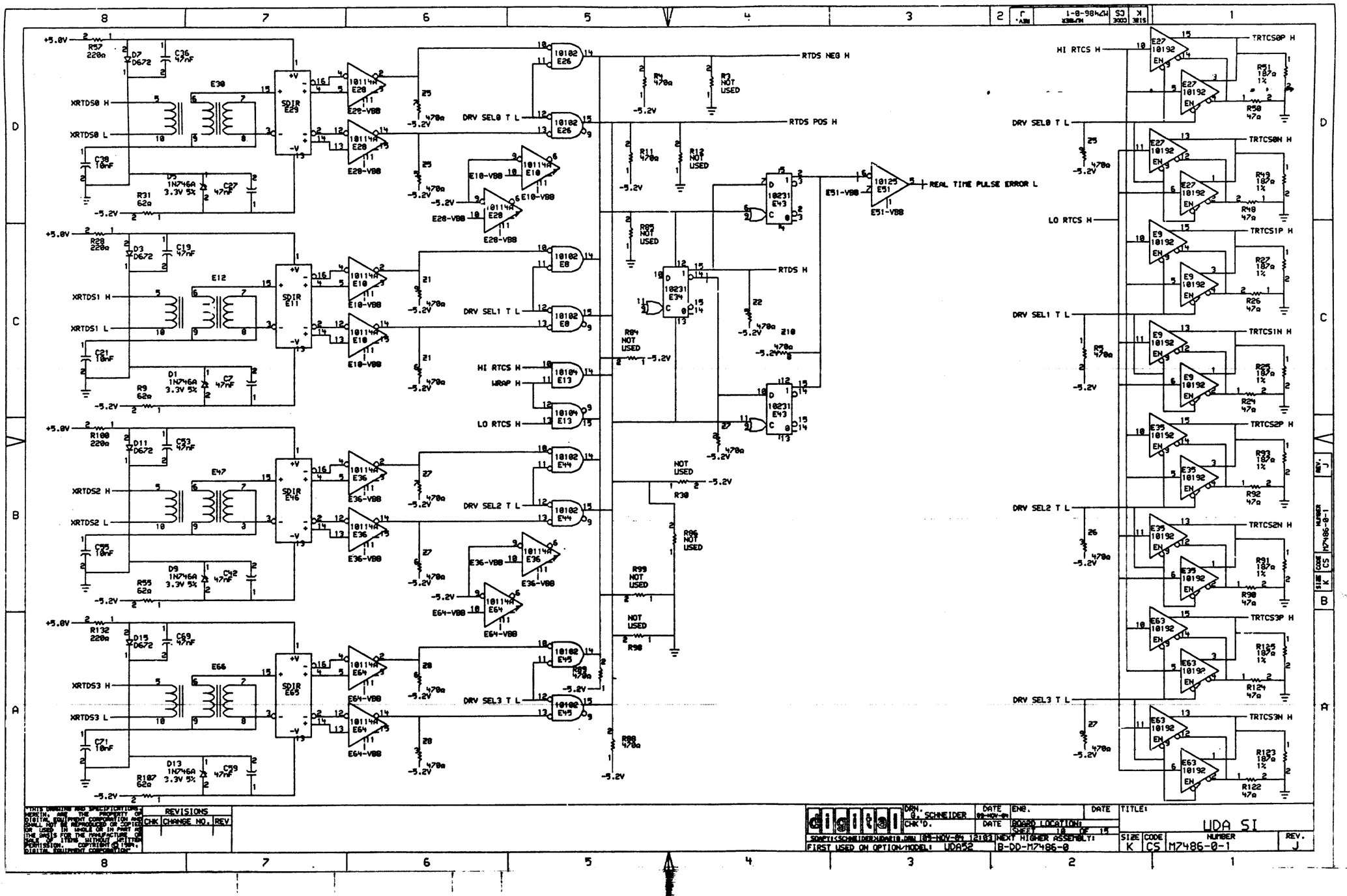
CHK'D. DATE BOARD LOCATION: SHEET 9 OF 15

SCAPT: SCHNEIDER UDA200.DRW 09-NOV-84 12:00 NEXT HIGHER ASSEMBLY:

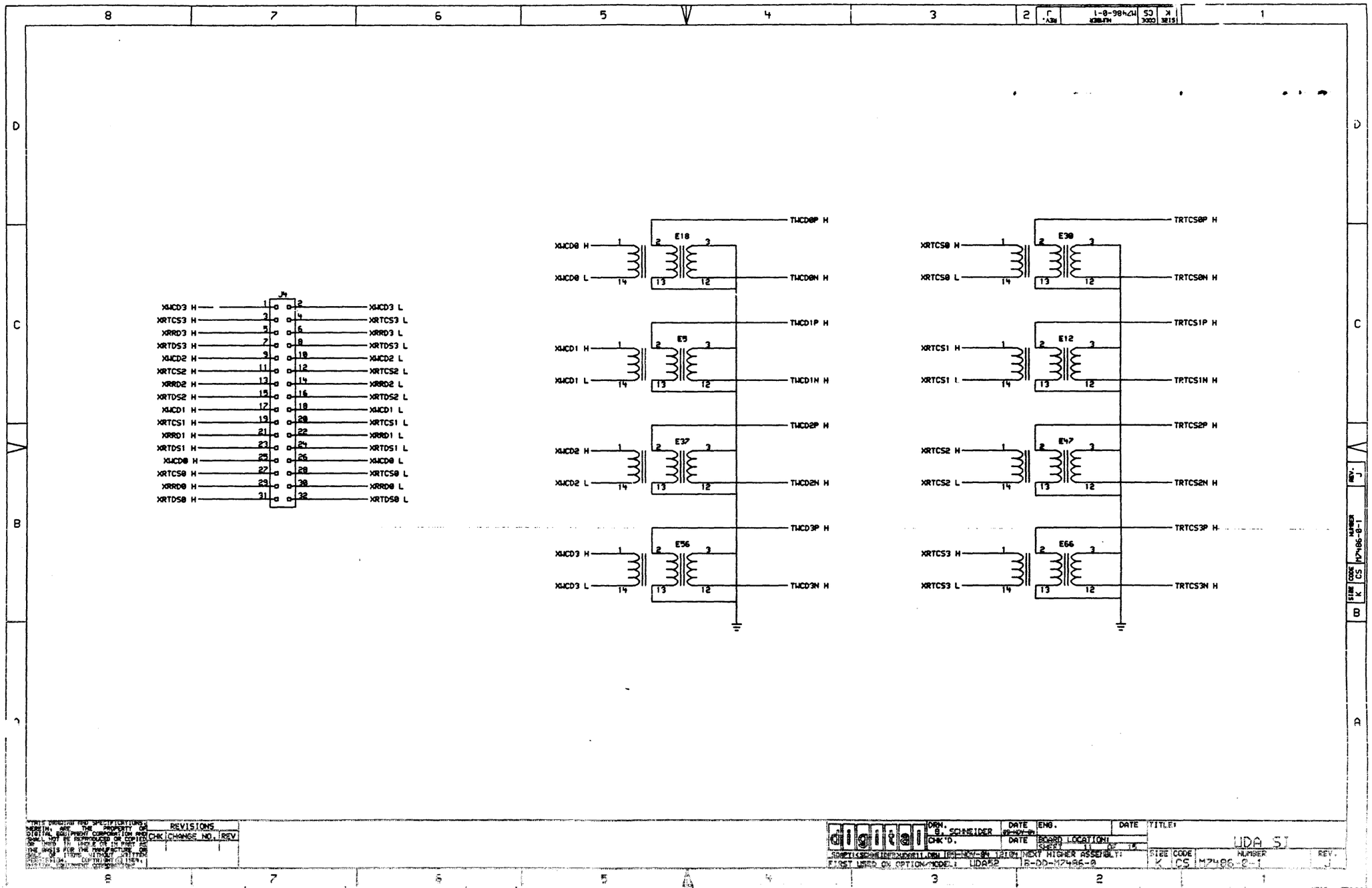
FIRST USED ON OPTION/MODEL: UDA52 B-DD-M7486-0

TITLE: UDA SI

SIZE	CODE	NUMBER	REV.
K	CS	M7486-0-1	J



XRTDS0 H
XRTDS0 L
XRTDS1 H
XRTDS1 L
XRTDS2 H
XRTDS2 L
XRTDS3 H
XRTDS3 L
SDIR E29
SDIR E11
SDIR E46
SDIR E65
DRV SEL0 T L
DRV SEL1 T L
DRV SEL2 T L
DRV SEL3 T L
HI RTCS H
WRAP H
LO RTCS H
RTDS NEG H
RTDS POS H
RTDS H
REAL TIME PULSE ERROR L
TRTCS0P H
TRTCS0N H
TRTCS1P H
TRTCS1N H
TRTCS2P H
TRTCS2N H
TRTCS3P H
TRTCS3N H
REVISIONS
CHK
CHANGE NO.
REV
DRN. G. SCHNEIDER
CHK'D.
DATE
ENG.
BOARD LOCATION:
SHEET 10 OF 15
TITLE:
UDA SI
SIZE K
CODE CS
NUMBER M7486-0-1
REV. J
FIRST USED ON OPTION/MODEL: UDA52
NEXT HIGHER ASSEMBLY: B-DD-M7486-0



REVISIONS		
CHK	CHANGE NO.	REV

digital

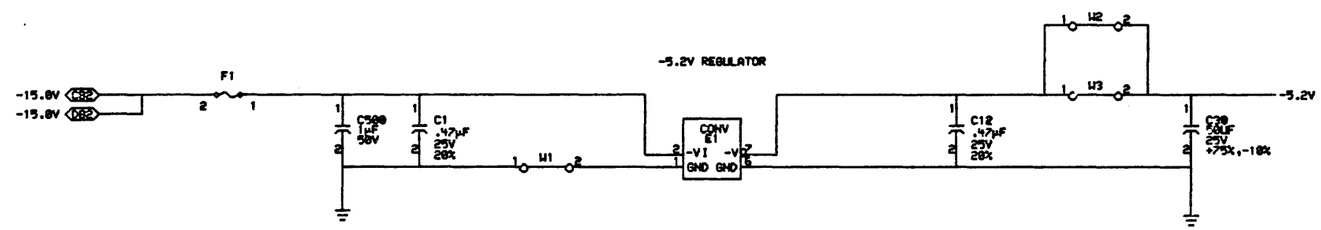
DRN. G. SCHNEIDER | DATE 09-NOV-84 | ENG. | DATE | TITLE: UDA SI

CHK'D. | DATE | BOARD LOCATION: SHEET 11 OF 15

SCOPY:(SCHNEIDER)UDA811.DWG [09-NOV-84 12:10] NEXT HIGHER ASSEMBLY: B-DD-M7486-0

FIRST USED ON OPTION/MODEL: UDA52

SIZE K | CODE CS | NUMBER M7486-0-1 | REV. J



REVISIONS		
CHK	CHANGE NO.	REV

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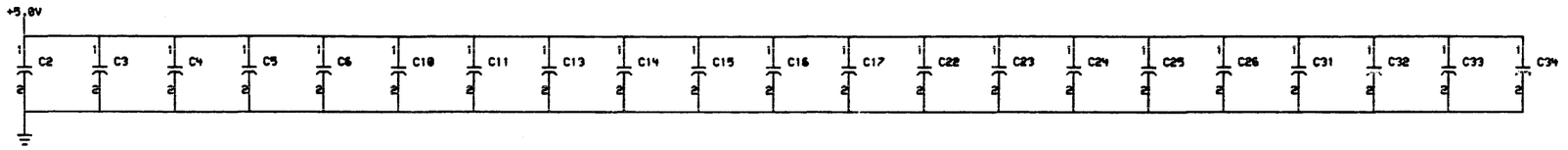
digital

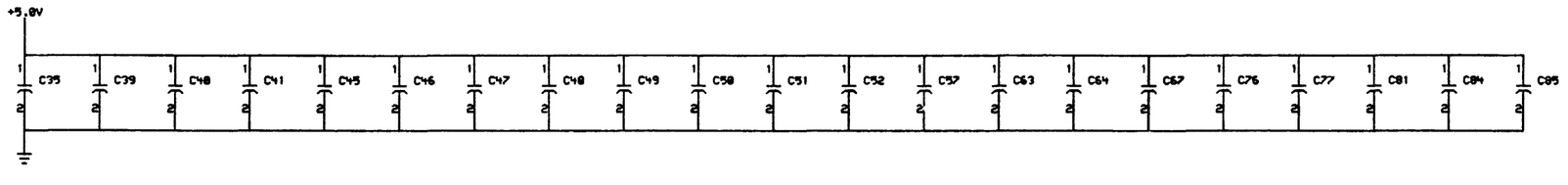
DRN. G. SCHNEIDER	DATE 09-NOV-84	ENG.	DATE
CHK'D.	DATE	BOARD LOCATION: SHEET 12 OF 15	
SOAPT:<SCHNEIDER>UDA12.DRW 09-NOV-84 12:05		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL: UDA52		B-DD-M7486-0	

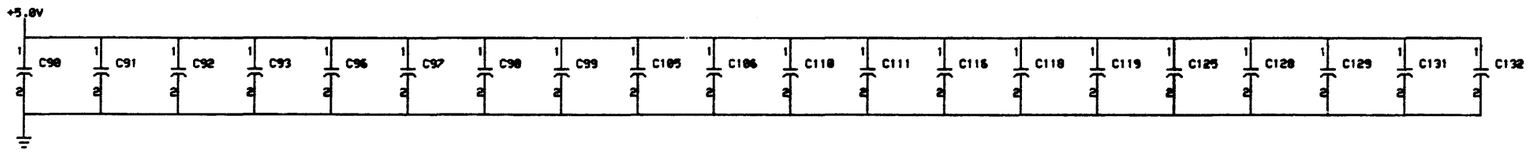
TITLE: UDA SI

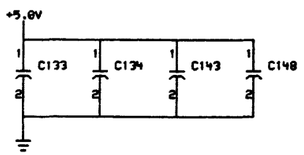
SIZE	CODE	NUMBER	REV.
K	CS	M7486-0-1	J

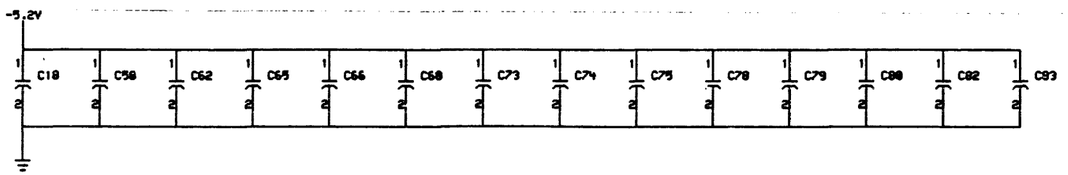
NOTE: UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ON THIS SHEET ARE:
47nF, 50V, +80%,-20%.

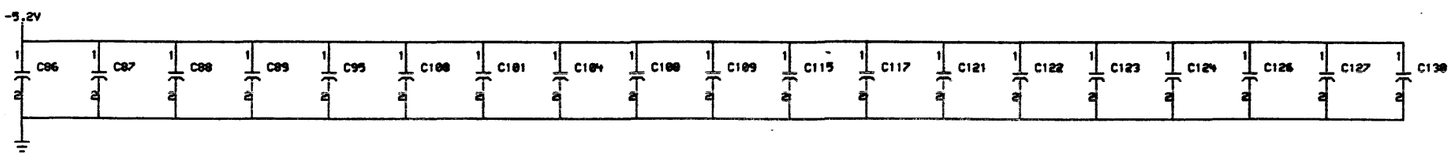




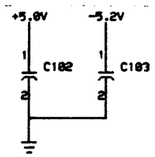


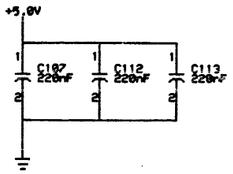






NOTE: C102 AND C103 ARE FOR FERRITE BEAD USE ONLY.





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REVISIONS		
CHK	CHANGE NO.	REV

DRN. G. SCHNEIDER — DATE 29-NOV-84
CHK'D. — DATE
ENG. — DATE
SCHEM LOCATION:
SHEET 13 OF 15
TITLE: UDA SI
SYSTEM NAME: M7486 REV: J 29-NOV-84 12:12
FIRST USED IN OPTION MOD: UDA52
NEXT HIGHER ASSEMBLY: B-DD-M7486-B
SIZE X | CODE CS | NUMBER M7486-B-1 | REV. J

Vertical location (A-D) Direction of line (Left, Right, Up, Down)
or electrical (Input, Output, Both)
KEY: SS-VH,D or backplane pin (Pin)
Schematic Sheet Horizontal location (1-8)

```
+12.0V ..... 1-B1,L
+15V ..... 1-B2,R <CU1>
+5.0 V ..... 1-B4,R
+5.0V ..... 1-A3,D 1-C3,D 5-B7,D 5-C3,D 9-A8,R 9-B8,R
9-C8,R 9-D8,R 10-A8,R 10-B8,R 10-C8,R 10-D8,R 13-A2,D 13-B2,D
13-B8,D 13-C8,D 13-C8,D 13-D8,D 1-A3,R <DA2> 1-A3,R <EA2>
1-A3,R <FA2>
-15.0V ..... 12-C7,R <CB2> 12-C7,R <DB2>
-5.2V ..... 7-A2,D 7-B3,R 7-B4,D 7-B5,D 7-B6,D 7-C1,R
7-C5,R 7-C7,D 7-C7,D 8-A3,L 8-B4,R 8-B5,D 8-B6,D 8-B6,D
8-C2,R 8-C4,D 8-C6,D 8-C7,D 8-D7,D 9-A5,D 9-A5,R 9-A8,R
9-B5,D 9-B6,R 9-B8,R 9-C4,L 9-C8,R 9-D4,D 9-D4,D 9-D6,R
9-D8,R 10-A5,D 10-A5,R 10-A8,R 10-B4,L 10-B6,R 10-B8,R 10-C2,D
10-C5,L 10-C8,R 10-D5,D 10-D5,D 10-D6,R 10-D8,R 12-C2,L 13-A8,D
13-B1,D 13-B7,D
ATTENTION H ..... 5-C6,L
AVAILABLE H ..... 6-C6,L
BAR 00 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,R 4-C4,L
BAR 01 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,R 4-B4,L
BAR 02 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,R 4-B4,L
BAR 03 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,R 4-B4,L
BAR 04 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,L 3-D7,R
BAR 05 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,L 3-D7,R
BAR 06 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,L 3-D7,R
BAR 07 H ..... 3-C1,R 3-C7,R 3-D1,R 3-D7,L 3-D7,R
BAR 08 H ..... 3-C1,R 3-C7,L 3-C7,R 3-D1,R 3-D7,R
BAR 09 H ..... 3-C1,R 3-C7,L 3-C7,R 3-D1,R 3-D7,R
BAR 10 H ..... 3-C1,R 3-C7,L 3-C7,R 3-D1,R 3-D7,R
BAR 11 H ..... 3-B7,L 3-C1,R 3-C7,R 3-D1,R 3-D7,R
BAR 12 H ..... 3-B7,R 3-C1,R 3-C7,L 3-D1,R
BAR 13 H ..... 3-B7,R 3-C1,R 3-C7,L 3-D1,R
BAR 14 H ..... 1-A7,R 3-C7,L
BAR 15 H ..... 3-C7,L
BUS BG4 IN H ..... 1-A8,R <DS2>
BUS BG4 OUT H ..... 1-A8,L <DT2>
BUS BG5 IN H ..... 1-A8,R <DP2>
BUS BG5 OUT H ..... 1-A8,L <DR2>
BUS BG6 IN H ..... 1-A8,R <DM2>
BUS BG6 OUT H ..... 1-A8,L <DN2>
BUS BG7 IN H ..... 1-A8,R <DK2>
BUS BG7 OUT H ..... 1-A8,L <DL2>
BUS NPG IN H ..... 1-A8,R <CA1>
BUS NPG OUT H ..... 1-A8,L <CB1>
CLK BDR H ..... 1-B5,R 1-B6,L
CLK BDR L ..... 1-B5,L 3-A1,R 3-A3,R 3-A5,R 3-A5,R
CLK DIOC L ..... 1-A6,R 1-C6,L
CLK ENB H ..... 1-B6,L 3-B7,R
CLK SERDES H ..... 1-B6,L 2-A4,R 5-C8,R
CLR PTY L ..... 6-A4,L 6-D7,R
CMD OUT L ..... 1-A5,L 2-D7,R 5-C8,R
DATA OUT L ..... 2-C3,L 5-C5,R
DATA PULSE ERROR L ..... 6-B2,R 9-D3,L
DATA RDY H ..... 1-A7,R 5-A5,L 5-C7,L
DATA WORD CLK L ..... 1-B8,R 2-D7,R 5-A5,L 5-C7,L
DATA XMIT ERROR H ..... 6-B1,L 6-D5,R
```

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DBUS 00 H ..... 1-C7,R 1-D5,L 1-D5,R 3-B4,R 3-D8,R 4-C5,R
5-A1,L 5-D7,L 6-C4,R 6-C5,L
DBUS 01 H ..... 1-C7,R 1-D5,L 1-D5,R 3-B4,R 3-D8,R 4-C5,R
5-A1,L 5-D7,L 6-C4,R 6-C5,L
DBUS 02 H ..... 1-D5,L 1-D5,R 1-D7,R 3-B4,R 3-D8,R 4-C5,R
5-A1,L 5-D7,L 6-C4,R 6-D5,L
DBUS 03 H ..... 1-D5,L 1-D5,R 1-D7,R 3-B4,R 3-D8,R 4-C5,R
5-A1,L 5-D7,L 6-B4,R 6-D5,L
DBUS 04 H ..... 1-D5,L 1-D5,R 1-D7,R 3-B4,R 3-D8,R 5-A1,L
5-D7,L 6-B4,R 6-C5,L
DBUS 05 H ..... 1-D5,L 1-D5,R 1-D7,R 3-B4,R 3-D8,R 5-A1,L
5-D7,L 6-B4,R 6-C5,L
DBUS 06 H ..... 1-D5,L 1-D5,R 1-D7,R 3-A4,R 3-D8,R 5-A1,L
5-D7,L 6-B4,R 6-C5,L
DBUS 07 H ..... 1-D5,L 1-D5,R 1-D7,R 3-A4,R 5-A1,L 5-D7,L
6-B4,R 6-D5,L
DBUS 08 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-C8,R 5-C1,L
5-D7,L 6-D5,L
DBUS 09 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-C8,R 5-B1,L
5-D7,L
DBUS 10 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-C8,R 5-B1,L
5-D7,L
DBUS 11 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-B8,R 5-B1,L
5-D7,L
DBUS 12 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-C8,R 5-B1,L
5-D7,L
DBUS 13 H ..... 1-C5,L 1-C5,R 1-D7,R 3-B2,R 3-C8,R 5-B1,L
5-D7,L
DBUS 14 H ..... 1-C5,L 1-C5,R 1-D7,R 3-A2,R 3-C8,R 5-B1,L
5-D7,L
DBUS 15 H ..... 1-B5,L 1-B5,R 1-D7,R 3-A2,R 3-C8,R 5-B1,L
5-D7,L 6-C5,L
DI/O CLR L ..... 1-A5,L 6-A2,R
DIAG CLK H ..... 1-C3,L 7-D8,R 8-D8,R
DIAG DATA H ..... 1-C3,L 7-C8,R
DIAG MODE H ..... 1-C3,L 7-C8,R 8-C8,R
DIAG MODE L ..... 1-D3,L 7-D8,R 8-D8,R
DLY UPROC H ..... 1-B5,R 1-B7,R 3-A5,R
DLY UPROC L ..... 1-B5,L 3-A1,R 3-A5,R
DRV SEL 0 H ..... 1-D3,L 7-C8,R
DRV SEL 1 H ..... 1-D3,L 7-B8,R
DRV SEL 2 H ..... 1-D3,L 7-B8,R
DRV SEL 3 H ..... 1-D3,L 7-B8,R
DRV SEL0 T L ..... 7-C7,L 9-D2,R 9-D5,R 10-D2,R 10-D5,R
DRV SEL1 T L ..... 7-B7,L 9-C2,R 9-C5,R 10-C2,R 10-C5,R
DRV SEL2 T L ..... 7-B7,L 9-B2,R 9-B5,R 10-B2,R 10-B5,R
DRV SEL3 T L ..... 7-B7,L 9-A2,R 9-A5,R 10-A2,R 10-A5,R
DTEST H ..... 1-A5,L 1-B7,R 5-B2,R
E10-V88 ..... 10-C6,D 10-C6,D 10-D5,D 10-D6,R
E17-V88 ..... 9-C5,D 9-D6,D 9-D6,D 9-D6,R
E25-V88 ..... 9-B5,D 9-B6,D 9-B6,D 9-B6,R
E28-V88 ..... 10-C6,D 10-D6,D 10-D6,D 10-D6,R
E36-V88 ..... 10-B5,D 10-B6,D 10-B6,D 10-B6,R
E4-V88 ..... 9-C6,D 9-C6,D 9-D5,D 9-D5,R
E51-V88 ..... 8-A3,D 8-B3,D 10-D3,D 10-D3,R
E55-V88 ..... 9-A5,D 9-A6,D 9-A6,D 9-B6,R
E59-V88 ..... 7-A2,D 7-B2,D 8-B3,D 9-C3,D 9-D3,R
E64-V88 ..... 10-A6,D 10-A6,D 10-A6,D 10-A6,R
ECC CLR L ..... 2-D3,L 5-C2,R
ECC ENABLE H ..... 1-A5,L 2-C7,R
ECC FDBCK EN H ..... 2-B2,L 5-A5,L 5-C2,R
```

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ECC INPUT EN H ..... 2-D2,L 5-A5,L 5-C2,R
ECC OUT 0 H ..... 5-A2,R 5-B3,R 5-C1,L
ECC OUT 1 H ..... 5-A2,R 5-B3,R 5-C1,L
ECC OUT 2 H ..... 5-A2,R 5-A3,R 5-C1,L
ECC OUT 3 H ..... 5-A2,R 5-A3,R 5-C1,L
ECC OUT 4 H ..... 5-A2,R 5-A3,R 5-C1,L
ECC OUT 5 H ..... 5-A2,R 5-A3,R 5-D1,L
ECC OUT 6 H ..... 5-A2,R 5-A3,R 5-D1,L
ECC OUT 7 H ..... 5-A2,R 5-A3,R 5-D1,L
ECC OUT 8 H ..... 5-C2,R 5-C3,R 5-D1,L
ECC OUT 9 H ..... 5-B2,R 5-C3,R 5-D1,L
ECC RDY H ..... 1-A7,R 2-B3,L
ECC START H ..... 2-C5,L
ECC STOP H ..... 2-B6,R 2-C5,R
ECC SYMBOL CLK L ..... 2-C6,R 5-C4,L
ECC SYMBOL L ..... 5-B3,L
ECC TIME H ..... 1-A5,L 2-D7,R
ECC10+2 H ..... 2-C6,L
ECCT16 L ..... 2-D6,L
EN RAM PE H ..... 1-D3,L 3-A7,R
EVEN PARITY H ..... 6-B1,L
GND ..... 5-A5,L 5-A6,R 5-C5,R 5-C5,R 1-A3,R <AC2>
1-A3,R <AT1> 1-A3,R <BC2> 1-A3,R <BT1> 1-A3,R <CC2>
1-A2,R <CT1> 1-A3,R <DC2> 1-A2,R <DT1> 1-A3,R <EC2>
1-A2,R <ET1> 1-A3,R <FC2> 1-A2,R <FT1>
GND RES L ..... 2-B3,L 6-B4,R
HI RTCS H ..... 8-D1,L 10-C5,R 10-D2,R
HI WCD H ..... 7-D1,L 9-C5,R 9-D2,R
HIGH H ..... 7-B6,R 8-B7,R 8-D3,L
HOLD DATA H ..... 6-B6,L
INC DBAR H ..... 3-A4,L 4-B5,R
INC UBAR H ..... 3-A4,L 4-C5,R
INDEX PULSE H ..... 6-C6,L
IOC SEL 0 H ..... 1-A6,R 1-C6,L
IOC SEL 1 H ..... 1-A6,R 1-C6,L
IOC SEL 2 H ..... 1-A6,R 1-C6,L
LD BUFFER L ..... 1-B6,L 3-A2,R 3-A4,R 3-A5,R 3-A5,R
LD DBAR L ..... 1-B6,L 3-B8,R 3-C8,R 4-B5,R
LD DCR L ..... 1-B5,R 1-B5,R 1-C6,L
LD ECC L ..... 2-B6,L 5-C5,R
LD RTCS L ..... 1-C6,L 6-B4,R
LD SERDES L ..... 1-B6,L 5-C8,R
LD UBAR L ..... 1-B6,L 3-B8,R 3-C8,R 4-C5,R
LED 1 L ..... 1-C3,L
LED 2 L ..... 1-C3,L
LED 4 L ..... 1-C3,L
LED 8 L ..... 1-B3,L
LO RTCS H ..... 8-C1,L 10-B5,R 10-D2,R
LO WCD H ..... 7-D1,L 9-B5,R 9-D2,R
NRZ CLK H ..... 5-A6,R
NRZ CLK OUT H ..... 7-B2,L 7-D8,R
NRZ DATA IN H ..... 5-C5,R 5-C8,R 7-A2,L
NRZ DATA OUT H ..... 5-B7,L 7-C8,R
ODD PRTY H ..... 1-C3,L 3-A8,R 3-A8,R
OVERRUN H ..... 1-A7,R 5-C7,L
R/W READY H ..... 6-C6,L
RAM 00 H ..... 3-B3,L 3-B8,R 3-C4,L 3-C6,L 3-D4,L 3-D6,L
RAM 01 H ..... 3-B3,L 3-B8,R 3-C4,L 3-C6,L 3-D4,L 3-D6,L
RAM 02 H ..... 3-B3,L 3-B8,R 3-C4,L 3-C6,L 3-D4,L 3-D6,L
RAM 03 H ..... 3-B3,L 3-B4,L 3-B6,L 3-B8,R 3-D4,L 3-D6,L
RAM 04 H ..... 3-B3,L 3-B8,R 3-C3,L 3-C6,L 3-D3,L 3-D6,L
```

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REVISIONS		
CHK	CHANGE NO.	REV

DWN. G. SCHNEIDER | DATE 03-NOV-84 | ENG. | DATE
CHK D. | DATE | BOARD LOCATION: SHEET 14 OF 15
DSK:UDA,T2PLT,243) 03-NOV-84 15:45 | NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: UDA52 | B-DD-M7486-0

TITLE: UDA SI

SIZE	CODE	NUMBER	REV.
K	CS	M7486-0-1	J

| | | |