EXPERIMENTAL DISPLAY SYSTEM

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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PREFACE

This manual is one of a series of documents needed for understanding and operating the General Purpose Experimental Display System. Included in this manual are descriptions of the system and its programming language, an explanation of those parts of the system which are not contained in other Digital publications, and reproductions of the engineering drawings used in this explanation.

This display system consists of a modified Program Data Processor-4, a modified Type 340 Incremental Display, and special interface and control equipment. The PDP-4 and 340 maintenance manuals should be consulted for all information on the operation and maintenance of their respective equipment. In addition, the subsidiary documents listed in these manuals are necessary adjuncts to the system documentation.

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SECTION 1

DESCRIPTION

INTRODUCTION

The General Purpose Experimental Display System described in this manual consists of a PDP-4C computer with 8192 words of core memory, a perforated tape reader, and a modified high-speed data multiplexer; a modified 340 Incremental CRT Display; a special operator's console and associated electronic circuitry; and interface equipment for connecting the system to a CDC 1604A digital computer. The PDP-4/340 system is normally operated as a piece of input-output equipment by the 1604A, but is also capable of independent operation.

This display system presents information that has been stored in the PDP-4's memory to the operator as dots, lines, curves, and characters on the face of a cathode ray tube. The operator may generate new data by depressing various buttons and keys on the console, moving knobs or a track ball, and placing a light pen over a particular displayed area. This information is placed in either the memory or the accumulator of the PDP-4, where it may be used to modify the display, indicate various conditions, or cause the system to perform different operations.

COMPUTER

The computer used in this system is Digital Equipment Corporation's standard PDP-4C with slight modifications and additional equipment, some of it standard Digital options and some unique to this system. An extra bay has been added to the computer to house the additional equipment. Figure 1-1 shows the rack layout of the computer.

The standard PDP-4C consists of a central processor, an operator's console, a 4096-word core memory, a real time control (referred to as the Type 25 Real Time Option in the PDP-4 Maintenance Manual), and a paper tape reader. The standard options added to the central processor include a 133 Data Interrupt Multiplexer, a 134 Core Memory Module, and a 140 Relay Buffer and Control, as well as 728 Power Supplies.

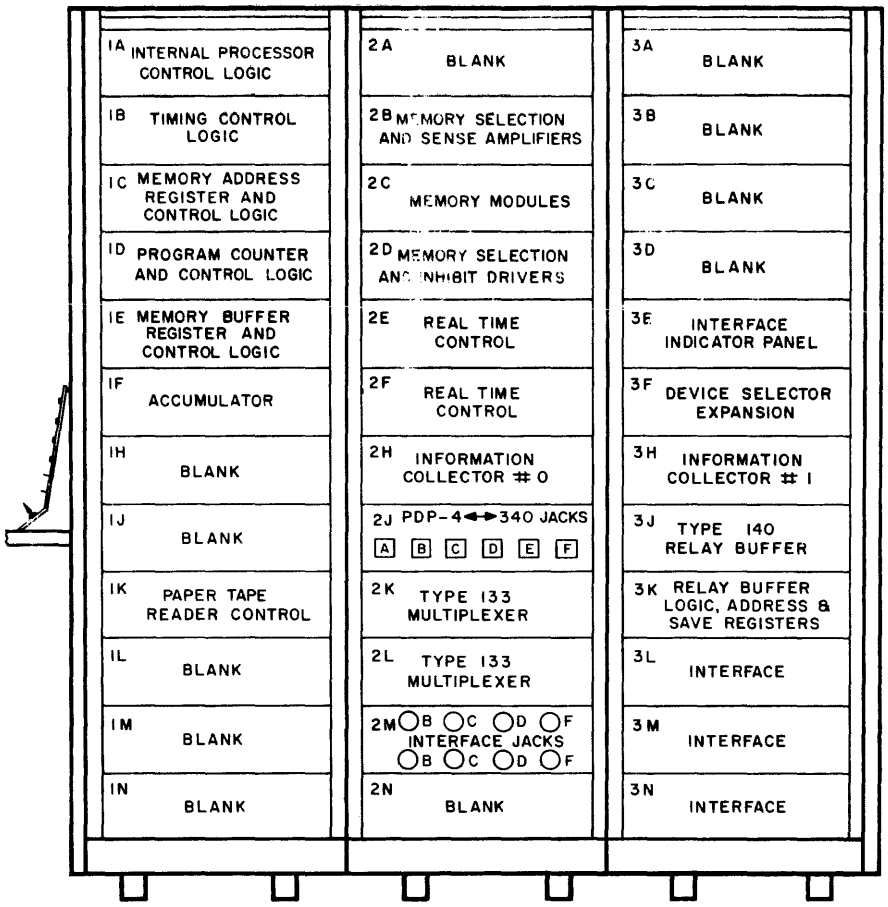

Figure 1-1 PDP-4C-24 Rack Layout

The modifications to the standard PDP-4C are in the real time control, and affect the real time clock and the information collector. The real time clock's overflow flag circuit has been disabled, and circuits have been added to include a gatable variable-frequency clock, a program servicing condition, and a new computer state (limbo).

The additional equipment added to the central processor includes address and save registers for the 340 Display, and interface control and status circuits to permit this system to be operated by CDC's 1604A computer. The latter circuits consist of an information buffer register for the 1604A's input, an interface address register for the PDP-4's memory location, level changing amplifiers to convert between CDC and Digital logic levels, a decoding network to allow the 1604A to correspond with this or other systems via the same buffer channels, and a group of status flip-flops for exchanging control information between the two computers.

DISPLAY

The CRT display used in this system is a standard Digital Type 340 Precision Incremental Display with slight modifications and additional equipment. Most of the extra equipment is specially designed for this system, and the standard items are a Type 370 Light Pen and Type 728 Power Supplies.

The special equipment added to the display consists of an operator's table with pushbuttons, lights, a keyboard, knobs, and a track ball; and the electronic control circuits associated with these items. Figure 1-2 shows the location of these various items on the operator's table. This equipment is not connected directly to the 340, but only obtains information which can be placed in the memory or accumulator of the PDP-4, and used by a program to change data or modify the display file.

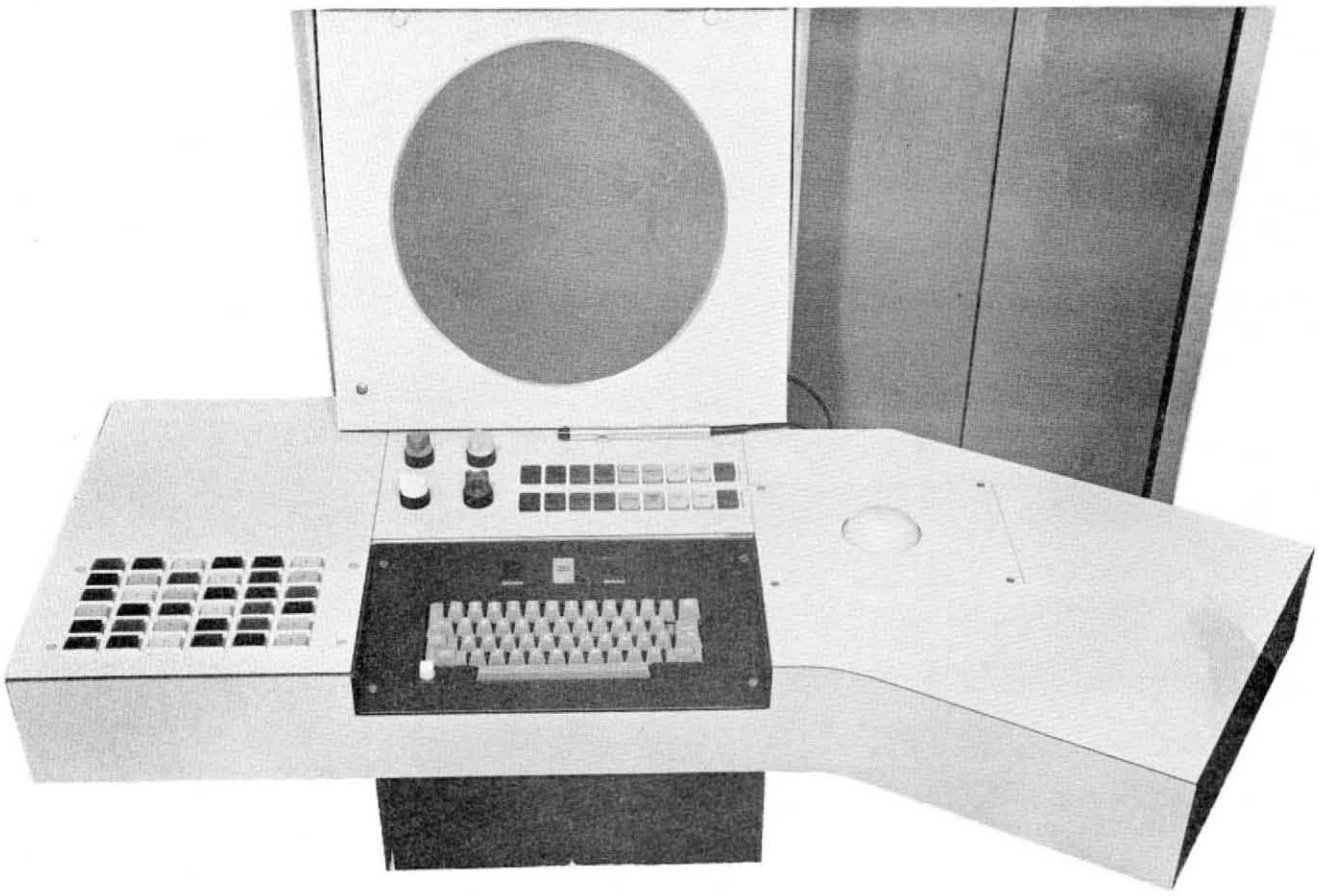

Figure 1-2 General Purpose Experimental Display Operator's Console

The extra electronic circuits consist of switch input filters for smoothing switch input signals; light driver registers that select and control the indicator lights within the pushbuttons; knob and track ball counters that convert and store physical movements; and an information collector that processes data from the above items and applies it to the accumulator of the PDP-4 on command.

The modifications to the 340 consist of adding a circuit which enables the display to decode input information and perform various operations based on this information. In this way the display acts as a small computer, using the same memory as the PDP-4. Figure 1-3 shows the rack layout of the display.

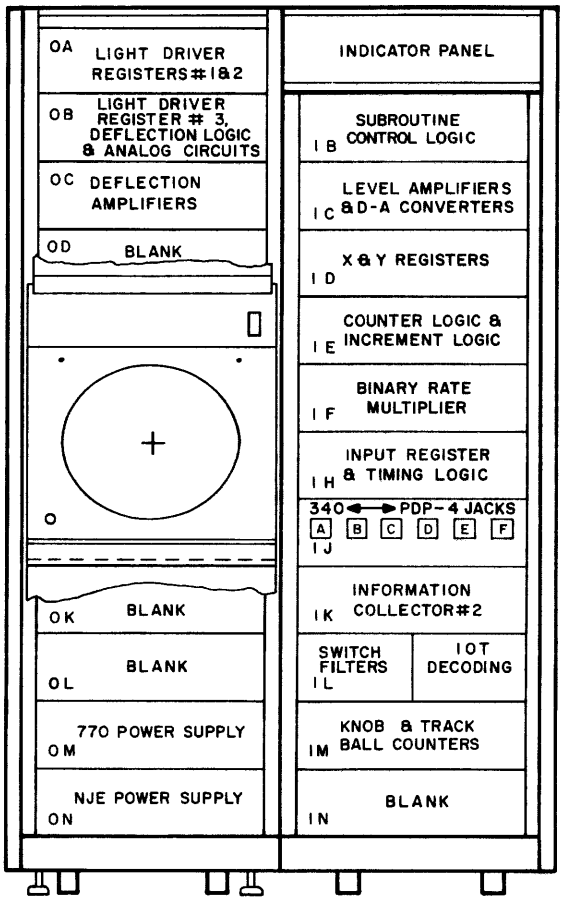

Figure 1-3 Modified Type 340 Display Rack Layout

SECTION 2

PROGRAMMING

TYPE 340 INCREMENTAL DISPLAY

The 340 Display employed in the general purpose experimental display system interprets the 18-bit input word in one of five modes as directed by the mode information contained in the mode register. The five modes which the 340 recognizes are: control mode, point mode, vector mode, vector continue mode, and increment mode. The operation of these modes is described in the Type 340 Incremental Display Maintenance Manual, H-340. The operation of the display in this system is somewhat different from that of the standard 340. The differences are explained below.

Control Mode (000)

This is a combination of the parameter and subroutine modes for the standard 340. Bits 0 and 1 compose the operation code for the control mode. When they are 00, the display operates similarly to the regular parameter mode. When the bits are other than 00, the display operates similarly to the subroutine mode.

Mode 000, OP Code 00

In the standard 340, bits 9 and 10 are unused in the parameter mode. The display in this system interprets these two bits in the following manner:

Bit 9 - Bit 9 is the skip bit. If bit 9 is set, the contents of the DAC are incremented by one count, fetching the next instruction from location N+2, (where N is the location containing the skip instruction) rather than from N+1.

Bit 10 - If bit 10 is set and the save flip-flop is set indicating that the 340 is in the process of performing a subroutine, the 340 escapes from the subroutine. The contents of the DAC are replaced by the contents of the DSR (which is not altered) and the save flip-flop is cleared. As

a result of this action, the 340 takes its next instruction from the memory address following the one which initiated entry into the subroutine. The effect is the same as if a DDS had been executed. Note that this action takes place only if the save flip-flop is set.

If both bit 7 (the stop bit) and bit 9 (the skip bit) are set, the display stops as a result of bit 7 being set. The skipping action is not performed until the PDP-4 issues the resume IOT, 700504. This allows the PDP-4 program to interrupt the DAC after the stop has occurred. Then, when the resume IOT is issued, the display requests data from a location one greater than the address read from the DAC.

If both bits 9 and 10 are set and the save flip-flop is set, the subroutine escape process is performed before the skipping action. When the above conditions are met, the 340 requests data from a location two greater than the instruction that caused entry into the subroutine. The subroutine escape has precedence over the skipping action.

> NOTE: The above actions can be microprogrammed with the other actions possible in a control mode word.

Mode 000, OP Code 01 - DDS (Display Deposit Save Register in A)

In PDP-4 memory register A, deposit a display Jump to the C (Display Save Register) instruction, replaces the mode register contents with bits 2 through 4 and clears the save flip-flop. This instruction generates an exit from a subroutine. The exit transfers the 340 program sequence to the location following the one which contained the DJS at the start of the subroutine.

Mode 000, OP Code 10 - DJP (Display Jump to A)

The contents of the 13-bit display address counter (DAC) are replaced with bits 5 through 17 of the BR. The present contents of the DAC are lost. The contents of the mode register are replaced with bits 2 through 4 of the BR. This instruction allows the 340 to receive its next word from the PDP-4 cell whose address corresponds to A, rather than from the address following the one containing the DJP instruction.

Mode 000, OP Code 11 - DJS (Display Jump to A, Save)

The contents of the 13-bit DAC are replaced with bits 5 through 13 of the BR. The present contents of the DAC are saved in the 13-bit display save register (DSR). This is signified by Setting the save flip-flop, and replacing the present mode register contents with bits 2 through 4. This instruction allows multi-level subroutining to be performed by the 340 since the contents of the DSR are accessible for generating an exit from the subroutine.

Point (XY) Mode (001)

Operation of the point mode is described in the 340 Maintenance Manual.

Vector Mode (100)

Operation of the vector mode differs from that described for the standard 340 in that violating an edge does not cause the display to escape to the control (parameter) mode. When a vector word with the escape bit set is encountered and the save flip-flop is set, the 340 performs the subroutine escape described previously.

Vector Continue Mode (101)

Operation of the vector continue mode differs from that described for the standard 340 only when the save flip-flop is set. If the save flip-flop is set and an edge is violated, the 340 performs the subroutine escape action. Violating an edge causes the mode to be changed to the control mode regardless of the setting of the save flip-flop.

Increment Mode (110)

Operation of the increment mode differs from that described for the standard 340 in that incrementing beyond the edge does not cause the display to escape to the control mode. Also, if an increment word is encountered with the escape bit set and the save flip-flop is set, the subroutine escape action takes place.

IOT 7X05Y4, Resume

In the standard 340, the IOT resume is used only following the detection of light by the light pen, when it causes the picture that is interrupted at the time of light detection to be continued.

In this display, the IOT resume does the following:

1. If the display is interrupted by the light pen while drawing a vector, resume causes the vector to be continued as in normal 340 operation.

2. If the display is stopped by a control parameter mode stop (bit 7 set), resume causes the display to request new data from the address in the DAC (the word following the stop instruction).

3. If the display is stopped due to control mode stop and the word that caused the stop also had the skip bit (bit 9) set, the skip is performed and data is requested from the address which is one location beyond that containing the stop and skip word.

4. If bit 4 (MB4) is set, resume does not affect state of LP enable (i.e., if set it remains set; if cleared, it remains cleared). If bit 4 is cleared, LP enable is cleared. Note that resume does not automatically reset LP enable.

5. If bit 5 (MB5) is set, resume will set the temporary blind flip-flop, effectively disabling the light pen.

6. If bit 12 (MB12) is set, resume will set the temporary dark flip-flop, preventing a spot from being displayed on the CRT.

The various microprogramming instructions possible with the resume family of IOT's is given in Table 2-1.

IOT 0912, Display Read Address Counter (DRA)

Issuing the IOT display read address counter (DRA) reads the C(DAC) = AC and also stops the 340, since DRA sets the 340 lockout flip-flop. This prevents the display from requesting data cycles and gives the programmer the ability to determine the current location of the display program while the display is running.

TABLE 2-1 RESUME FAMILY OF IOT's

Octal Value	LP Enable	Temp Blind	Temp Dark
700504	cleared	--	--
700524	cleared	--	cleared
700544	cleared	--	set
710504	cleared	set	--
710524	cleared	set	cleared
710544	cleared	set	set
720504	--	--	--
720524	--	--	cleared
720544	--	--	set
730504	--	set	--
730524	--	set	cleared
730544	--	set	set

PDP-4 COMPUTER

Almost all of the PDP-4 instructions will operate the PDP-4/340 system as they are described in the PDP-4 Handbook. The only exceptions are the IOT clock skip on flag, 700001, and the IOT's for the paper tape punch, teleprinter, Type 30 displays, magnetic tape, card reader, card punch, and line printer.

PDP-4/340 SYSTEM

Many of the standard instructions and all of the special instructions have been given new mnemonic names, generally three digits long. Table 2-2 lists these instructions by name, gives their octal numerical values, and describes their functions. All possible instructions are not named or listed because some additional microprogramming is possible.

TABLE 2-2 PDP-4/340 INSTRUCTIONS

Mnemonic	Octal	Name/Remarks
1	020000	/INDIRECT BIT
6S	77	/BCD MASK
13S	17777	/ADDRESS MASK
ADD	300000	ADD/1'S COMPLEMENT, ADDRESS AND AC
AGI	702244	ALLOW GENERATOR INTERRUPT/ALLOW INTERRUPT FROM INTERFACE INTERRUPT FLAG
AND	500000	AND/LOGICAL AND, ADDRESS AND AC
API	700044	ALLOW PERIODIC INTERRUPT
CAL	000000	CALL SUBROUTINE/IN ADDRESS
CGI	702401	CLEAR GENERATOR FLAG I/CLEAR 1604 INPUT CHANNEL INTERRUPT FLAG
CGO	702402	CLEAR GENERATOR FLAG)/CLEAR 1604 OUTPUT CHANNEL INTERRUPT FLAG
CGP	702202	CLEAR GENERATOR FLAG P/CLEAR INTERFACE FLAG
CLA	750000	CLEAR AC
CLC	750001	CLEAR AND COMPLEMENT AC
CLF	700004	CLOCK OFF AND FLAG CLEARED
CLL	744000	CLEAR LINK
CL1	703101	CLEAR LIGHT BUFFER 1/ NUMBERS 1-18
CL2	703121	CLEAR LIGHT BUFFER 2/ NUMBERS 19-30
CL3	703141	CLEAR LIGHT BUFFER 3/ INSTRUCTIONS
CLN	700044	CLOCK ON AND FLAG CLEARED
CMA	740001	COMPLEMENT AC
CME	000200	CONTROL MODE, ESCAPE BIT SET
CML	740002	COMPLEMENT LINK
CRR	703161	CLEAR RELAY REGISTER
CSI	000010	CONTROL MODE, INTENSITY BIT SET
CSS	000100	CONTROL MODE, SCALE BIT SET
DAC	040000	DEPOSIT IN AC/FROM ADDRESS
DCA	700604	DISPLAY CLEAR ADDRESS COUNTER
DCE	703302	DISPLAY CLEAR EDGE FLAGS
DCF	700704	DISPLAY CLEAR FLAGS
DCL	702701	DISPLAY CLEAR 340 LOCKOUT
DCM	000000	DISPLAY CONTROL MODE/SETS MODE BITS TO CONTROL MODE
DCS	702601	DISPLAY CLEAR SAVE REGISTER
DDS	200000	DEPOSIT DISPLAY SAVE REGISTER/IN ADDRESS
DGI	702204	DISALLOW GENERATOR INTERRUPT/DISALLOW INTERRUPT FROM 1604
DHI	003000	DISPLAY HALT AND INTERRUPT
DHQ	002000	DISPLAY HALT QUIETLY/WITHOUT INTERRUPT
DIM	140000	DISPLAY INCREMENT MODE/SETS MODE BITS TO INCREMENT MODE
DJP	400000	DISPLAY JUMP/TO SUBROUTINE

TABLE 2-2 PDP-4/340 INSTRUCTIONS (continued)

Mnemonic	Octal	Name/Remarks
DJS	600000	DISPLAY JUMP AND SAVE/DISPLAY JUMP TO SUBROUTINE
DLA	700606	DISPLAY LOAD ADDRESS COUNTER AND START DISPLAY
DLS	702603	DISPLAY LOAD ADDRESS SAVE REGISTER
DNP	000000	DISPLAY NO OPERATION
DPI	700004	DISALLOW PERIODIC INTERRUPTS
DPM	020000	DISPLAY POINT MODE/SETS MODE BITS TO POINT MODE
DRA	700512	DISPLAY READ ADDRESS COUNTER AND STOP
DRP	702712	DISPLAY READ PARAMETERS
DRS	700504	DISPLAY RESUME/FAMILY OF EIGHT
DRX	702512	DISPLAY READ X COORDINATE
DRY	702514	DISPLAY READ Y COORDINATE
DSI	700601	DISPLAY SKIP ON INTERRUPT FLAG AND CLEAR
DSK	000400	DISPLAY SKIP
DSP	700701	DISPLAY SKIP ON LIGHT PEN FLAG AND CLEAR
DSQ	002000	DISPLAY STOP QUIETLY/WITHOUT INTERRUPT
DSR	702614	DISPLAY READ SAVE REGISTER
DSS	702501	DISPLAY SKIP ON STOP INTERRUPT
DSX	700501	DISPLAY SKIP ON X EDGE
DSY	703301	DISPLAY SKIP ON Y EDGE
DVC	120000	DISPLAY VECTOR CONTINUE MODE/SETS MODE BITS TO VECTOR CONTINUE MODE
DVM	100000	DISPLAY VECTOR MODE/SETS MODE BITS TO VECTOR MODE
DZM	140000	DEPOSIT ZERO IN MEMORY/AT ADDRESS
GLK	750010	GET LINK
HLT	740040	HALT
IGI	702441	SET GENERATOR'S INPUT INTERRUPT, FLAG I/1604 INPUT CHANNEL INTERRUPT FLAG
IGO	702442	SET GENERATOR'S OUTPUT INTERRUPT, FLAG O/1604 OUTPUT CHANNEL INTERRUPT FLAG
IGP	702242	SET GENERATOR'S PERMIT INTERRUPT FLAG P/1604 INTERRUPT PERMIT FLAG
IOF	700002	TURN OFF INTERRUPT
ION	700042	TURN ON INTERRUPT
IOT	700000	BASIC INPUT-OUTPUT INSTRUCTION
ISZ	440000	INDEX AND SKIP IF 0
JMP	600000	JUMP
JMS	100000	JUMP TO SUBROUTINE
LAC	200000	LOAD AC
LAM	000000	/USED IN DEC DISTRIBUTED PROGRAMS
LAS	750004	LOAD AC FROM SWITCHES
LAW	760000	LOAD AC WITH THIS INSTRUCTION/INCLUDING ADDRESS
LGA	702303	LOAD GENERATOR'S ADDRESS COUNTER
LLI	703105	CLEAR AND LOAD LIGHTS IN BUTTONS OF RBI/ NUMBERS 1-18

TABLE 2-2 PDP-4/340 INSTRUCTIONS (continued)

Mnemonic	Octal	Name/Remarks
LL2	703125	/CLEAR AND LOAD LIGHTS IN BUTTONS OF RB2, NUMBERS 19-36
LL3	703144	/CLEAR AND LOAD LIGHTS IN BUTTONS OF RB3/INSTRUCTIONS
LRR	703165	LOAD RELAY REGISTER/BIT 17 CLEARS THE RELAY REGISTER
NOP	740000	NO OPERATION
OAS	740004	INCLUSIVE OR AC AND SWITCHES
OPR	740000	OPERATE
POF	010000	LIGHT PEN OFF
PON	014000	LIGHT PEN ON
RAL	740010	ROTATE AC AND LINK LEFT ONE PLACE
RAR	740020	ROTATE AC AND LINK RIGHT ONE PLACE
RB1	703112	READ BUTTON BANK 1/NUMBERS 1-18
RB2	703132	READ BUTTON BANK 2/NUMBERS 19-30
RB3	703152	READ BUTTON BANK 3/INSTRUCTION
RB4	703172	READ BUTTON BANK 4/SPECIAL FUNCTION BUTTONS
RB5	703212	READ BUTTON BANK 5/0-9, A-H
RB6	703232	READ BUTTON BANK 6/I-Z
RCF	700102	CLEAR THE READER FLAG
RCL	744010	CLEAR LINK THEN RAL
RCR	744020	CLEAR LINK THEN RAR
RGA	702314	READ GENERATOR'S ADDRESS COUNTER
RIF	702414	READ 8 INTERFACE FLAGS
RKN	703256	READ KNOBS 1, 2, AND 3 AND CLEAR FLAG/BIT 15 CLEARS KNOB REGISTERS
RRB	700112	READ READER BUFFER INTO AC, CLEAR READ FLAG
RSA	700104	SELECT READER FOR ALPHANUMERIC, CLEAR RDR FLAG
RSB	700144	SELECT READER FOR BINARY, CLEAR READER FLAG
RSF	700101	SKIP ON READER FLAG
RSR	700314	READ STATUS OF IO EQUIPMENT
RTB	703276	READ TRACK BALL AND CLEAR FLAG/BIT 15 CLEARS TRACK BALL REGISTER
RTL	742010	ROTATE AC LEFT TWICE
RTR	742020	ROTATE AC RIGHT TWICE
SAD	540000	SKIP IF AC AND Y ARE DIFFERENT
SGI	702201	/INTERFACE INTERRUPT SKIP ON GENERATOR INTERRUPT/
SGP	702242	SET PDP-4 INTERFACE INTERRUPT FLAG/FLAG P
SKO	703201	SKIP ON KNOB OVERFLOW
SKP	741000	SKIP ALWAYS
SMA	740100	SKIP ON MINUS AC/NEGATIVE
SNA	741200	SKIP ON NON-ZERO AC
SNL	740400	SKIP ON NON-ZERO LINK
SPA	741100	SKIP ON POSITIVE AC
SPI	700001	SKIP ON PERIODIC INTERRUPT

TABLE 2-2 PDP-4/340 INSTRUCTIONS (continued)

Mnemonic	Octal	Name/Remarks
SPL	741400	/USED IN DEC DISTRIBUTED ROUTINES
SRF	700101	SKIP ON READER FLAG
STL	744002	SET THE LINK
SZA	740200	SKIP ON ZERO AC
SZL	741400	SKIP ON ZERO LINK
TAD	340000	TWOS COMPLEMENT ADD/ADDRESS AND AC
XCT	400000	EXECUTE INSTRUCTION IN ADDRESS
XFL	002000	POSITION X AND FLASH
XNF	000000	POSITION X AND DON'T FLASH
XOR	240000	EXCLUSIVE OR/ADDRESS WITH AC
YFL	202000	POSITION Y AND FLASH
YNF	200000	POSITION Y AND DON'T FLASH
ZRO	000000	ZERO

Knob and Track Ball Counters

It is possible for the knob or track ball counters to overflow after the interrupt generated when ±8 was reached and before the interrupt program can read and reset the counters. However, the sign bit is still valid for an additional count of 8 so the programmer can obtain some data if this event occurs. The counting sequence is given in Table 2-3.

TABLE 2-3 KNOB AND TRACK BALL COUNTING SEQUENCE

Sign	Bit 1	Bit 2	Bit 3	Bit 4	Value	Comments
0	0	0	0	0	+16	Next clockwise count
0	1	1	1	1	+15	Clockwise Counts
0	1	1	1	0	+14	
0	1	1	0	1	+13	
0	1	1	0	0	+12	
0	1	0	1	1	+11	
0	1	0	1	0	+10	
0	1	0	0	1	+ 9	
0	1	0	0	0	+ 8	
0	0	1	1	1	+ 7	

TABLE 2-3 KNOB AND TRACK BALL COUNTING SEQUENCE (continued)

Sign	Bit 1	Bit 2	Bit 3	Bit 4	Value	Comments
0	0	1	1	0	+ 6	
0	0	1	0	1	+ 5	
0	0	1	0	0	+ 4	
0	0	0	1	1	+ 3	Clockwise Counts
0	0	0	1	0	+ 2	
0	0	0	0	1	+ 1	
0	0	0	0	0	0	(cleared to this value)
1	1	1	1	1	- 1	
1	1	1	1	0	- 2	
1	1	1	0	1	- 3	
1	1	1	0	0	- 4	
1	1	0	1	1	- 5	
1	1	0	1	0	- 6	
1	1	0	0	1	- 7	
1	1	0	0	0	- 8	Counterclockwise Counts
1	0	1	1	1	- 9	
1	0	1	1	0	-10	
1	0	1	0	1	-11	
1	0	1	0	0	-12	
1	0	0	1	1	-13	
1	0	0	1	0	-14	
1	0	0	0	1	-15	
1	0	0	0	0	-16	
1	1	1	1	1	-17	Next counter clockwise count

Sample Interruption Saving Program

When it is desired to interrupt the 340's background program to flash a short message and then to return to the main program at the point of interruption, it is necessary that the interrupting program have the ability to restore the conditions of the various registers in the 340. A basic program which allows the interrupting routine to save the contents of the important 340 registers and then to restore these register is as follows:

(Saving Routine:)

```
DSR                 /READ SAVE REGISTER
DAC SAVE
DRA                 /READ DISPLAY ADDRESS COUNTER AND SET 340 LOCKOUT
DAC JUMP
DRP                 /READ DISPLAY PARAMETERS
DAC GO
DRY                 /READ DISPLAY Y COORDINATE
DAC GO+1
DRX                 /READ DISPLAY X COORDINATE
DAC GO+2
.....
```

Interrupting Message

```
.....
```

(Restoring Routine:)

```
LAW GO
DLA                  /LOAD DISPLAY ADDRESS COUNTER AND START DISPLAY
DCL                  /RESET 340 LOCKOUT
DSS
JMP.-1               /WAIT FOR DISPLAY TO STOP
LAC SAVE
DLS                  /LOAD DISPLAY SAVE REGISTER ACCORDING TO AC
DRS+20000
```

(Display File:)

```
GO,                  /STORAGE LOCATION FOR PARAMETER INFORMATION
GO+1,                /STORAGE LOCATION FOR Y COORDINATE INFORMATION
GO+2,                /STORAGE LOCATION FOR X COORDINATE INFORMATION
GO+3,                /DISPLAY HALT
JUMP,                /STORAGE LOCATION FOR DAC CONTENTS.  WILL BE EXECUTED
                     /AS DJP (DAC)
SAVE                 /STORAGE LOCATION FOR CONTENTS OF SAVE REGISTER
```

SECTION 3

MAINTENANCE

In any complicated logic system which includes a digital computer, it is useless to attempt to list all the possible problems which might occur and their probable causes. However, efficient maintenance is still possible, because all malfunctions are either caused by operator error or equipment failure. Operator error, which includes programming bugs, is by far the most common. Complete familiarity with the system minimizes this source of trouble.

Equipment failures fall into three catagories: mechanical; power; and logic. A mechanical failure is due either to misadjustment, wear, or breakdown. These failures can almost always be spotted by a visual check of the equipment or by operation of the equipment. Power failures are caused either by no power or the wrong power, or else by a condition which causes the regulation and filtering of the power supplies to exceed their specifications. The former cases are usually due either to the main switch on the power supply being turned off or to a marginal voltage switch on some rack being thrown to the marginal (up) position. The latter case usually indicates either too great a load on the power supply (as a low-resistance short), or not enough load (such as some circuits not connected). A logic failure is a failure of a logical circuit to operate in its normal manner. It is usually caused by a bad component or connection in a module. This may be a random failure, but is usually caused by aging.

An equipment failure can be found by a method based on thorough understanding of the system's operation, common sense and logical thinking, and an organized step-by-step procedure. If a mechanical failure is suspected, a thorough visual check of the equipment should be made first. Then, if no more danger to the equipment will result, an operational check should be made. The only complicated mechanical equipment in this system is the perforated tape reader. Procedures for adjusting this equipment are given in Paragraph 11-4 (d) of the PDP-4 Maintenance Manual and the perforated tape reader maintenance manual. Equipment power failures can usually be found by oscilloscope checking of the power supply to each rack. Logical failures of the equipment are most easily found by using a repetitive diagnostic program loop to exercise the desired function or operation, and tracing the signal path through the circuits

of the equipment with an oscilloscope. Special attention should be paid to noise and extra signals, or to signals whose timing is wrong. If a signal is found to be missing, the input to that circuit should be investigated both for amplitude and duration. A marginal voltage check should be made to determine if the preceding circuit is a causative or aiding agent of the failure.

The operation of the vast majority of this system is covered in the PDP-4, 340, and 370 maintenance manuals. The operation of the standard options, modifications of the standard equipment, and the special equipment is given later in this section. An explanation of each MAINDEC program is given in the associated MAINDEC manual. With this information it should be possible to set up any repetitive testing loop program to check any part of this system. As an additional aid in maintaining this system, two special test cables are provided which allow the light buffers and pushbutton groups to simulate the operation of the 1604A.

PREVENTIVE MAINTENANCE

The best way to insure troublefree operation is to locate and correct all potential failures before they occur in normal operation. This can be done by running a MAINDEC or other diagnostic test program in the system and/or operating various portions of the equipment under marginal voltage conditions until a failure occurs. When this is done routinely and a record kept of the voltages at which failures occur, it is possible to note any progressive deterioration due to aging. Any particular circuit or module which may later cause a failure is often noticed by a steadily decreasing margin voltage. Replacement of the module and/or correction of the aging component is indicated when such a long-term drift is detected, even though the margin at which failure occurs has not exceeded normal limits.

> NOTE: Before attempting to replace any module with a spare, check to see if the module has any jumpers or adjustments. Modules which have jumpers can only be replaced with similar modules with the same jumper connections. Modules which have adjustments require that these be set for the same operating conditions as the replaced module.

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When the switch is in the up position, it connects the associated terminals on its rack to the output of a 734 Power Supply located at the top of the plenum door behind bay 1 of the PDP-4. The 734 supplies power between 0 and ±20 volts dc, as shown on its voltmeter. The polarity of this voltage is determined by the MARGINAL CHECK switch. This switch must be in the +10 MC position when marginal checking either a +10 volt A or a +10 volt B line, and in the -15 MC position when checking the -15 volt C line. When this switch is in the OFF position, normal voltages are applied to all three lines in every panel, regardless of the setting of the marginal voltage switches on the panels.

Raising the bias voltage above +10 volts increases the cutoff bias that must be overcome by the previous driving transistor, causing low-gain transistors to fail. Lowering the bias voltage below +10 volts reduces the transistor base bias at noise rejection and thus provides a test to provide high-leakage transistors and stimulates high temperature conditions (to check for thermal runaway). All Digital modules should operate normally when the +10 volt bias varies by more than ±5 volts (unless there is exceptional noise on the line).

Since the -15 volt supply is the collector load voltage (which is clamped at -3 volts in most modules), raising and lowering this source has little effect upon the logic circuits. Therefore, the -15 volt marginal testing is only done on pulse amplifiers and other equipment which produces pulses through a pulse transformer. Raising and lowering the -15 volt supply increases and decreases the output pulse, respectively. These modules should operate normally with the -15 volts varying between -8 and -18 volts.

CAUTION

Do not increase the -15 volt supply beyond -18 volts. Damage to the electronic circuit may result if this voltage exceeds -18 volts.

1604A Simulation

As an aid in maintaining this system, two special test cables are supplied which allow the PDP-4 to simulate the output signals from the 1604A and to test the response of the interface electronic circuits to these signals. When using these test cables, the four cables from the 1604A are removed, and a diagnostic test program is run by the PDP-4. The only part of the

interface equipment not tested is the Digital→ CDC level converting portion. This may be checked with a dc voltmeter or oscilloscope directly on the pins of 2MB, 2MC, 2MF.

NOTE: Type 1703 Switch Filters located in 1L01, 1L02, and 1L03 in the display must be removed when performing the simulation tests.

Test cable 1 connects the input signals of the Digital → CDC level converters to the conditioning level inputs of the remote information collector 2, as shown in Figure 3-2. Plug 3L29 is connected to the jack at the right rear of rack 3L in the PDP-4 and plug 1K29 is connected to the jack at the right rear of rack 1K in the 340. Jack 1K29 is connected to the remote information collector 2 in parallel with the inputs from the group of 36 pushbuttons. The IOT 703102 (read button group 1) inclusive ORs the simulated 1604A input data bits with the contents of the accumulator, and IOT 703122 (read button group 2) inclusive ORs the simulated 1604A input sense response bits with the contents of the accumulator. Table 3-1 lists the bit allocations for these simulated functions.

TABLE 3-1 SIMULATED 1604A INPUT SIGNAL BIT ASSIGNMENTS

"read pushbutton group 1" IOT 703102		"read pushbutton group 2" IOT 703122	
AC Bit	Simulated Function	AC Bit	Simulated Function
0	Input Data Bit 17	0	Not Used
1	Input Data Bit 16	1	Not Used
2	Input Data Bit 15	2	Sense Response
3	Input Data Bit 14	3	Output Data Resume
4	Input Data Bit 13	4	Input Interrupt and All on Input Interrupt
5	Input Data Bit 12	5	Output Interrupt and All on Output Interrupt
6	Input Data Bit 11	6	Not Used
7	Input Data Bit 10	7	Input Data Ready
8	Input Data Bit 9	8	Not Used
9	Input Data Bit 8	9	Not Used

TABLE 3-1 SIMULATED 1604A INPUT SIGNAL BIT ASSIGNMENTS (continued)

"read pushbutton group 1" IOT 703102		"read pushbutton group 2" IOT 703122	
AC Bit	Simulated Function	AC Bit	Simulated Function
10	Input Data Bit 7	10	Not Used
11	Input Data Bit 6	11	Not Used
12	Input Data Bit 5	12	Not Used
13	Input Data Bit 4	13	Not Used
14	Input Data Bit 3	14	Not Used
15	Input Data Bit 2	15	Not Used
16	Input Data Bit 1	16	Not Used
17	Input Data Bit 0	17	Not Used

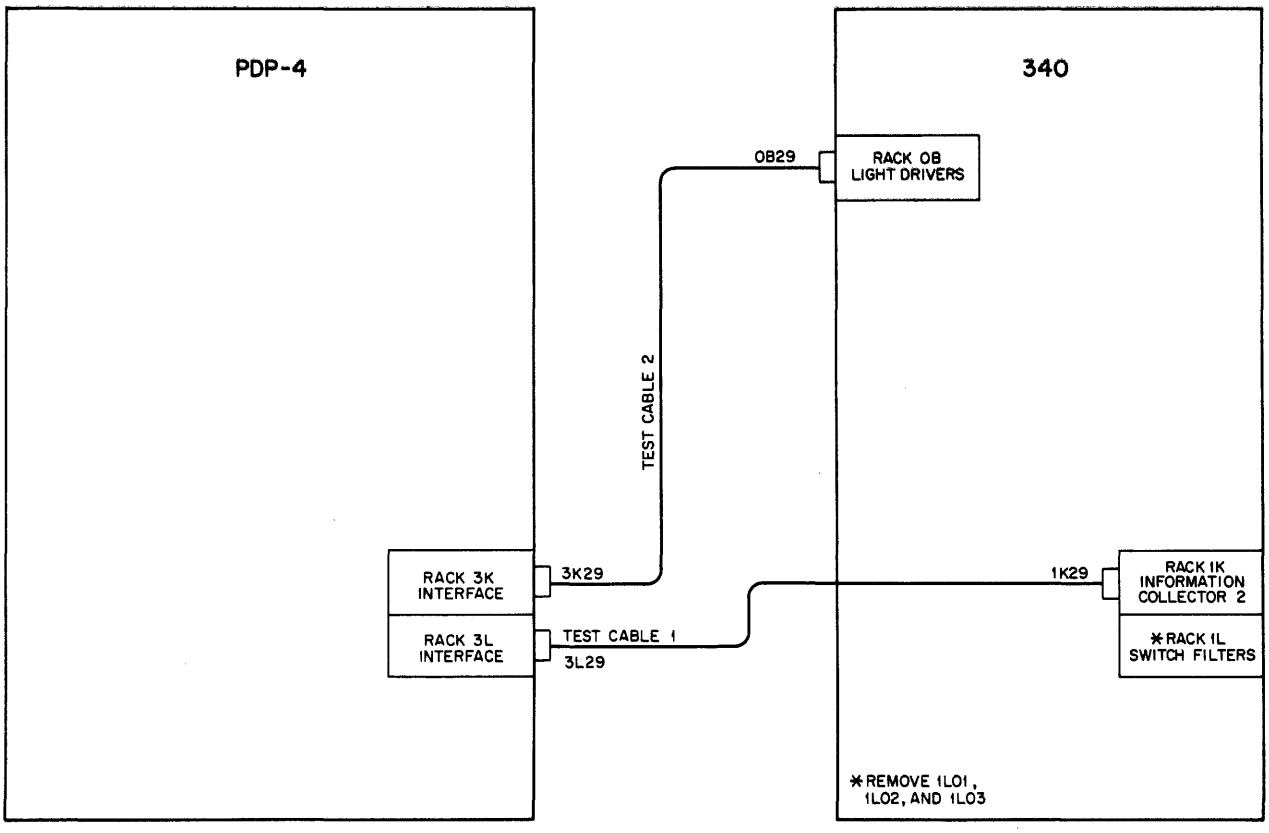

Figure 3-2 1604A Simulation Block Diagram

Test cable 2 connects the outputs of the three light driver registers to the inputs of the CDC → Digital level converters. The signals from the light drivers are ground or -15 volts instead of -0.5 or -16 volts, so these circuits receive slightly attenuated simulated inputs. Plug 0B29 is connected to the jack at the right rear of rack 0B in the 340, and plug 3L29 is connected to the jack at the right rear of rack 3L in the PDP-4. IOT 703105 (clear and load light buffer 1) transfers a word from the accumulator into light driver register 1, simulating the 1604A output data bits. IOT 703125 (clear and load light buffer 2) transfers another word from the accumulator into light driver register 2, simulating the 1604A output sense levels and data bit 18. IOT 703145 (clear and load light buffer 3) transfers a third word from the accumulator into light driver register 3, simulating the 1604A function bits. Table 3-2 lists the bit allocations for the simulated function.

TABLE 3-2 SIMULATED 1604A OUTPUT SIGNAL BIT ASSIGNMENTS

"clear and load light buffer 1" IOT 703105		"clear and load light buffer 2" IOT 703125		"clear and load light buffer 3" IOT 703145	
Bit	Simulated Function	Bit	Simulated Function	Bit	Simulated Function
0	Output Data Bit 17	0	Master Clear	0	Not Used
1	Output Data Bit 16	1	Output Function Ready	1	Not Used
2	Output Data Bit 15	2	Output Sense Ready	2	Not Used
3	Output Data Bit 14	3	Output Data Ready	3	Not Used
4	Output Data Bit 13	4	Input Function Ready	4	Not Used
5	Output Data Bit 12	5	Input Sense Ready	5	Not Used
6	Output Data Bit 11	6	Input Buffer Active	6	Function Bit 11
7	Output Data Bit 10	7	Input Data Resume	7	Function Bit 10
8	Output Data Bit 9	8	Not Used	8	Function Bit 9
9	Output Data Bit 8	9	Not Used	9	Function Bit 8
10	Output Data Bit 7	10	Not Used	10	Function Bit 7
11	Output Data Bit 6	11	Not Used	11	Function Bit 6
12	Output Data Bit 5	12	Not Used	12	Function Bit 5
13	Output Data Bit 4	13	Not Used	13	Function Bit 4

TABLE 3-2 SIMULATED 1604A OUTPUT SIGNAL BIT ASSIGNMENTS (continued)

"clear and load light buffer 1" IOT 703105		"clear and load light buffer 2" IOT 703125		"clear and load light buffer 3" IOT 703145	
Bit	Simulated Function	Bit	Simulated Function	Bit	Simulated Function
14	Output Data Bit 3	14	Not Used	14	Function Bit 3
15	Output Data Bit 2	15	Not Used	15	Function Bit 2
16	Output Data Bit 1	16	Not Used	16	Function Bit 1
17	Output Data Bit 0	17	Output Data Bit 18	17	Function Bit 00

OPERATION OF EXTRA EQUIPMENT

If any malfunction should occur in the logic portions of the system, a deductive reasoning approach is recommended to find the faulty circuit. This requires knowledge of how the various portions of the logical circuitry operate in order to compare the actual operation with the normal operation. When a discrepancy is found, the faulty circuit can be isolated and repairs made.

Most of the logical circuits in the general purpose experimental display are described in either the PDP-4, 340, or 370 maintenance manuals. Those which are not, are described in the following portion of this section. They are divided into the standard Digital options, modifications of the standard equipment normally in the PDP-4 and 340, and the special equipment used in this system.

Standard Options

Type 133 Data Interrupt Multiplexer

This standard option allows up to three external devices to have access to the PDP-4 core memory in order to receive data from or deliver data to the memory. The data transfer is directly to or from the memory buffer register (MB) to the input or output register of the external device, therefore none of the working registers of the PDP-4 are disturbed. The transfer

of data takes one memory cycle from the PDP-4. Each device is assigned to a unique channel in the 133. The three external devices are set up in a priority network. The device attached to channel 0 has highest priority.

The external device must provide three things:

1. A signal denoting that the device is ready for a data transfer. This is a negative level, usually denoted as "data request" or "request for data", etc.

2. A signal to denote the desired direction of transfer (to or from memory in the PDP-4). An input device goes to memory, while an output device receives from memory. This is a negative level if the direction is toward the PDP-4. (It is not necessary for a device which only receives information to present this signal.)

3. A register of some sort to store the address of the desired PDP-4 memory location.

Example - An external device on channel 0 wishes to present a word to the PDP-4 memory. When the timing of this device says that conditions are proper for the transfer, the device produces a request for a data cycle. This negative level comes into Figure 4-1 (BS-D-133-0-2) at the lower left side. The data interrupt request signal, DI REQ_0, turns on an inverter in 2L06, generating a ground level that enables the capacitor-diode gate at the 1 input of flip-flop MPX_0. Time pulse T6 then sets MPX_0 to the 1 state. It is possible that channels 1 and 2 also had requests at T6, but as soon as MPX_0 is set, it resets all lower priority MPX flip-flops by the inverters in 2L04, bottom left, which constitute the priority chain. MPX_0 stays set until the PDP-4 is in a condition in which it recognizes data request (at the end of the instruction). The ground MPX_0 output is applied to three parallel inverters at right center, producing the output labeled DIMPX·SEL 0. The DI REQ_0 signal also cuts off an inverter at left center, producing the DI REQUEST signal.

This signal is applied to the data interrupt control at the upper left corner of Figure 4-2 (BS-D-125-0-1) (labeled 57A and DATA REQ). At time T5 this signal causes the data sync flip-flop to be set to its ONE state, applying a ground to a positive NOR gate at the center of

Figure 4-2. This produces a break request signal (BK RQ) that is sent to the major states section and produces the break cycle at time T7. When the break cycle flip-flop is set (-3 volt signal, B), the function DATA·B is produced by the negative NAND gate at the upper left corner.

At T1 of the following cycle the signal DI ADD → MA is produced, strobing the address information presented by the requesting channel into the memory address (MA) register of the PDP-4. This information is found on Figure 4-3 (BS-D-133-0-1), and labeled DI ADD_{5-0} through DI ADD_{17-0}. (The function DIMPX·SEL zero gates the proper address information for the channel.) The DI ADD → MA pulse also goes to the left center of Figure 4-1 (BS-D-133-0-2); and, since MPX_0 is set to a 1, produces a signal called DIADD ACCEPT-0, signifying to the external device that the PDP-4 has acknowledged its request and that the external device can now remove the request.

Since the external device is presenting information to the memory, a signal labeled DI $IN\text{-}OUT_0$ at the left center of Figure 4-1 (BS-D-133-0-2), is applied to the data interrupt section of the real time control. This signal (labeled DATA IN) is inverted at the left center of Figure 4-2 (BS-D-125-0-1), producing the DATA IN signal. The purpose of this level is to inhibit the strobing of the memory, since data is to be placed in memory. If DATA IN is ground and DATA·B is also ground, the function DATA·B·DATA IN is produced, enabling a capacitor-diode gate in 2E18. At time T3 this gate is triggered, activating a pulse amplifier (PA) which produces the DATA INFO → MB signal. This pulse transfers the information presented by the external device into the memory buffer (MB). This information is shown on top of Figure 4-3 (BS-D-133-0-1) as DI IN_{0-0} through DI IN_{17-0}. At time T5 the flip-flop MPX_0 is reset to 0.

If this had been an output device rather than an input device, the signal DI $IN\text{-}OUT_0$ would not have been produced, memory would have been strobed, and the external device would receive its data from the memory buffer bus drivers (BD) located on top of Figure 4-1 (BS-D-133-0-2).

Type 140 Relay Buffer and Control Register

The relay buffer and control register are located in the PDP-4. The relay buffer, which consists of 18 single-pole double-throw relays, is located in rack J of bay 3. The control register, which consists of 18 unbuffered flip-flops, is located in part of rack K of bay 3. Figure 3-1

shows these items in the machine. The input and both outputs of each form "D" relay contact are available at two connectors on the back of the panel, and at test points on the front of the panel. Each output is filtered to smooth out contact bounce. A separate indicator light is wired in parallel with each relay coil and is on when the coil is energized. The 140 Relay Buffer is shown schematically in Figure 4-4 (BS-D-24903).

The relay buffer control register consists of 18 unbuffered flip-flops and indicator drivers. The 18 bits from the accumulator (AC) are applied to the conditioning level inputs of positive capacitor-diode gates in the 4220 modules located in 3K05 and 3K07, as shown in Figure 4-5 (BS-D-24902). When the PDP-4 issues the IOT 703165, clear and load pulses occur that first clear the register to zero, then set each flip-flop, whose corresponding bit in the AC is a logic 1 (ground), to the 1 state. When any flip-flop is set to 1, its 1 output (internally jumpered) goes to -3 volts and activates the associated indicator driver in 3K04 and/or 3K06. The indicator driver outputs then go to ground and complete a circuit from the -15 volt supply through the relay coil, energizing the relay and turning on the indicator light.

MODIFICATIONS

Real Time Control

The real time control has been modified:

1. By adding a variable-frequency clock and a programmable gating circuit for generating periodic interrupt signals.

2. By removing the overflow flag circuit by modifying the real time clock circuit.

3. By adding a circuit which precludes the 340 Display from requesting data while the PDP-4 is in a break cycle.

4. By adding a circuit that allows the 1604A to set the PDP-4 into a continuous break cycle (limbo state).

5. By increasing the number of inputs to the information collector.

These changes are shown in Figure 4-2 (BS-D-125-0-1).

Periodic Interrupt

The source of pulses which cause the periodic interrupts is a 4401 Variable Clock located at 2E12. This produces negative pulses that are applied to the trigger pulse input of a capacitor-diode gate located at 2E18. The conditioning level input of the capacitor-diode gate is fed from the clock enable flip-flop in 2E17. This input is negative when the clock enable flip-flop is set, allowing a negative pulse from the 4401 to produce a positive pulse at the output of the pulse inverter. This pulse is applied to the clock flag flip-flop, setting it to 1 and producing a negative output level. This is sent to two places: the program interrupt request logic; and the I/O skip logic. The action of the program interrupt request logic and the I/O skip logic is described in the PDP-4 program and maintenance manuals. The clock enable flip-flop is set and cleared under program control by MB_{12} in the IOT 700004 (clock off), or IOT 700044 (clock on). The clock flag flip-flop is turned off by both IOT's 700004 and 700044.

Real Time Clock

The real time clock pulses are derived from a filament transformer located in the 813 Power Control Panel of the PDP-4. The 60-cycle sine wave is converted into pulses by the 4410 module at 2E19, and applied to a capacitor-diode gate in 2E18. The conditioning level input of this gate is always enabled by -3 volts; so the clock pulses (occurring at approximately a 16.7 millisecond repetition rate) continually set the clock count request flip-flop to the 1 state, causing the clock sync flip-flop in 2E15 to be set by timing pulse T5. The clock sync flip-flop causes the PDP-4 to go into a clock break cycle, during which location 7 in memory is addressed and the contents incremented by one. The difference between this operation and that described in the PDP-4 maintenance manual is no flag signal is generated if an overflow occurs when the contents of location 7 are incremented.

340 Lockout

The normally unused flip-flop in the 4218 module in 2E17, shown in the lower left of Figure 4-2, is the 340 lockout flip-flop. The capacitor-diode input gates of this flip-flop are permanently disabled by a negative potential, preventing the IOT 700004 from setting or clearing it. The flip-flop is initially cleared by the RTO BEGIN pulse, the IOT enable program interrupt, 700042,

or the IOT display clear lockout, 702701. These IOT's apply a negative pulse to the base of an inverter gate (the inverter gate in 2E16 is enabled by a ground on its emitter from MB12 (1)), producing a temporary ground output that is applied to terminal Y of the 340 lockout flip-flop that clears it to 0.

Whenever the PDP-4 grants a program break cycle to an interrupting device, the program sync flip-flop enables a NAND gate in 2E14 which produces the ground PGM·B signal. This is complemented by an inverter in 2E13 and applied to terminal Z of the 340 lockout flip-flop, setting it to 1. A -3 volt signal is then produced and applied to an inverter in 2E22, whose collector is connected to the 340 data request input. This grounds the request for data line and prevents the -3 volt request from being generated. The IOT display read address counter, 700502, also sets the 340 lockout flip-flop.

Limbo State

The PDP-4 used in this system can be placed into a fifth major state by the external 1604A computer if allowed by the operator. In the limbo state the computer continuously repeats break cycles. The circuits which control the limbo state are located both in the interface control section and the real time control.

If the operator wishes to allow the 1604A to place the PDP-4 in the limbo state, he must throw the LIMBO switch on the interface indicator panel, 3E, to the RECOGNIZE position. This places a -3 volt enabling potential on a 3-input negative NAND gate in 2L19, Figure 4-6 (BS-E-4C-24-2), allowing the 1604A to sense the state of the switch with the output sense command EXF765010, and connects the buffered output of the limbo flip-flop to the real time control. When the LIMBO switch is in the LOCKOUT position, ground potentials are applied to both the limbo switch sensing gate and the real time control, which then operates in the normal fashion.

The 1604A can set the limbo flip-flop in 3L09 to its ONE state with the command EXF065001, which applies a ground input to the buffer inverter in 3L25. This causes a -3 volt LIMBO signal to be applied to one part of the LIMBO switch. The limbo flip-flop is initially cleared by the power clear (PWR CLR) pulses, which occur when the PDP-4 is first turned on, and thereafter is cleared by the EXF055001 instruction from the 1604A.

When the limbo flip-flop is set and the LIMBO switch is on RECOGNIZE, the -3 volt LIMBO signal is applied to the emitter of the program enable inverter in 2E16, shown in Figure 4-2 (BS-D-125-0-1) near the prog sync flip-flop. This disables the inverter and prevents the program enable flip-flop from clearing the prog sync flip-flop, which would normally occur at time T5 of the first break cycle. The prog sync flip-flop can now only be set or cleared by pulse T5 according to the PROG REQ signal.

The -3 volt LIMBO (1) signal is also applied to a negative OR gate at the upper right of Figure 4-2, producing a -3 volt PROG REQ signal. This signal is complemented by an inverter in 2E13, and both potentials are applied to the conditioning level inputs of the capacitor-diode gates which control the prog sync flip-flop. The first T5 pulse which occurs then sets the flip-flop to the 1 state, causing the computer to enter a break cycle.

As long as the limbo flip-flop remains set and the switch is closed, the computer remains in the limbo state. The 1604A must clear the limbo flip-flop to release the PDP-4 from this condition. When this is done, the PDP-4's program counter (PC) is set to 1; so the computer executes that instruction which is in memory location 1.

While the PDP-4 is in the limbo state, data or clock breaks are granted during a break cycle, with data breaks having priority over clock breaks. After granting these breaks, the computer reverts back to the limbo state. Since the 340 lockout flip-flop can prevent the display from generating a data request, it is possible for the 1604A to monopolize the data break cycles of the PDP-4.

Information Collector

The information collector in this system consists of three sections; information collector 0, information collector 1, and information collector 2. Essentially the information collector consists of a group of 18 pulse amplifiers, each one controlled by 24 gated inputs. Most of these gates (not all are used) continually monitor the state of various flip-flops throughout the system and, when a particular IOT occurs, produce output pulses if the controlling flip-flops are in the 1 state. These pulses activate the pulse amplifiers which are connected to the set input gates of the accumulator (AC). The IOT therefore causes the information in the selected flip-flops to be read into the AC for future use. Refer to paragraphs 7-2a and 9-2c in the PDP-4 manual for further description.

Information Collector 0 - This is the standard information collector for the real time control. The block schematic is shown in Figure 9-3, page A-100 in the PDP-4 manual. However, only the IOT's 700102 (read and clear flag) and 700304 (read status register) are valid because no paper tape punch or console typewriter is used in this system.

Information Collector 1 - This section is just like the gates of information collector 0 except that no load resistors are used. The outputs of the two pulse inverters in each bit are in parallel with the corresponding two pulse inverters in information collector 0. Since these four pulse inverters share a common clamped load resistor, their positive pulse outputs are ORed together. Figure 4-7 (BS-D-4C-24-14) shows this section. Each pulse inverter is controlled by four negative capacitor-diode gates, whose outputs are ORed together. Each gate is enabled by a -3 volt level (or negative potential) approximately 1 microsecond after it occurs, and is disabled by a ground level approximately 1 microsecond after it occurs. Seven IOT's are applied to the trigger pulse inputs, as follows:

1. DRP - Read Display Parameters, 702501. This IOT causes the current states of the light pen enable (bit 6), size (bits 12 and 13), and intensity level (bits 15, 16, and 17) flip-flops to be read into the indicated positions of the AC. Bits 4, 5, 11, and 14 are set to 1 and the remaining bits are cleared to 0.

2. DRX - Read Display's X Coordinate, 702502. This IOT causes the current states of the X coordinate counter flip-flops to be read into bits 8 through 17 of the AC. Bit 4 is set to 1 and the remaining bits are cleared to 0.

3. DRY - Read Display's Y Coordinate, 702504. This IOT causes the current states of the Y coordinate counter flip-flops to be read into bits 8 through 17 of the AC. Bit 7 is set to 1 and the remaining bits are cleared to 0.

4. DRA - Read Display's Address Counter, 700512. This IOT causes the current states of the flip-flops in the display address counter to be read into bits 5 through 17 of the AC and the current states of the three mode flip-flops to be read into bits 2, 3, and 4. Bit 0 is set to 1 and bit 1 is cleared to 0.

5. DSR - Read Address Save Register, 702604. This IOT causes the current states of the flip-flops in the address save register to be read into bits 5 through 17 of the AC; and reads the current state of the save flip-flop into bit 0, the temporary dark flip-flop into bit 1, the temporary blind flip-flop into bit 2, the X edge violated flip-flop into bit 3, and the Y edge violated flip-flop into bit 4.

6. RIF - Read Interface Flags, 702414. This IOT causes the current state of the interface flag flip-flops to be read into bits 0 through 8 of the AC. The remaining flip-flops are cleared to 0.

7. RGA - Read Generator's Address Register, 702304. This IOT causes the current state of the flip-flops in the interface address register to be read into bits 5 through 17 of the AC. The remaining bits are cleared to 0.

Information Collector 2 - This section is electrically identical with information collector 0 and operates in the same manner. The output of each pulse amplifier is applied to the negative input of the corresponding pulse amplifier in information collector 0, so the output of each gate can be considered to be ORed with the outputs of the gates of the other two sections.

This information collector is shown in Figure 4-8 (BS-D-4C-24-4), and is located in rack K of bay 1 in the 340 Display. It senses the status of the 54 indicating pushbuttons, 54 typewriter keys, and the knob and track ball counters. When any pushbutton or key is depressed, -15 volts is applied to a switch filter, located in rack L of bay 1 in the 340 Display. The switch filter delays and smooths out any impulses in this signal to eliminate errors due to contact bounce, and reduces the signal to -3 volts. The console table switches and switch filters are shown in Figure 4-9 (BS-E-4C-24-3). The outputs of the switch filters are applied to the conditioning level inputs of the capacitor-diode gate in information collector 2.

When the computer issues an IOT to read a particular group of switches or keys during the time the capacitor-diode gates are enabled by -3 volt levels, pulses are produced which activate the associated pulse amplifiers. Since the pushbuttons and keys are activated manually, their contacts remain closed for approximately 100 milliseconds or more. Therefore, the computer must issue its information gathering IOT's at least ten times each second if no

operator's action is to be skipped. The same method is used to enter the knob and/or track ball information into the PDP-4's memory. However, this information consists of a 5-bit word for each knob or track ball counter.

There are eight IOT's used by information collector 2. These produce the pulses listed on the left side of Figure 4-8 (BS-D-4C-24-4), which trigger the associated enable gates. These pulses are produced by pulse amplifiers in the IOT decoding circuit, shown in Figure 4-10 (BS-D-340-5-16). The IOT families 7031X2 and 7032X2 are decoded according to bits 12 and 13 from the memory buffer (MB). These two bits are complemented because a -3 volt assertive level is needed for both their 0 and 1 states. MB_{12} is complemented by an inverter in 3H25, and MB_{13} is complemented by one of the gates in 3H03. The other four gates in 3H03 are 2-input negative NAND gates. Each receives one MB_{12} and one MB_{13} input and produces a ground output when both inputs are -3 volts. Both the normal and inverted bits are applied to two gates, in the four possible configurations. This produces four outputs which are labeled according to the octal value of X (assuming MB_{14} is 0).

The three 4603 Pulse Amplifier modules in the upper left of Figure 4-10 (BS-D-340-5-16) produce the eight trigger pulses for remote information collector 2. Each pulse is obtained from a pulse amplifier which is controlled by an inverter gate. The IOT 7031X2 pulse is applied to the base of four of these inverter gates, and the four decoded MB levels are applied to the emitters, therefore only one of these gates is enabled at a time. The IOT 7032X2 pulse is applied to the other four inverter gates, whose emitters are paralleled with the corresponding inverters of IOT 7031X2. The pulses produced by the particular IOT's are listed below.

1. 703102 - Read Button Group 1 produces the RB_1 pulse which causes the current status of the 18 numbered pushbuttons on the left side of the group of 36 pushbuttons to be ORed with the contents of the AC. These are numbered 1 through 18, in three vertical rows as shown in Figure 1-2, but may be different if the pushbutton panels are replaced.

2. 703122 - Read Button Group 2 produces the RB_2 pulse which causes the current status of the 18 numbered pushbuttons on the right side of the group of 36 pushbuttons to be ORed with the contents of the AC. These are numbered

19 through 36, in three vertical rows as shown in Figure 1-2, but may be different if the pushbutton panels are replaced.

3. 703142 - Read Button Group 3 produces the RB_3 pulse which causes the current status of the 18 control pushbuttons above the keyboard to be ORed with the contents of the AC.

4. 703162 - Read Button Group 4 produces the RB_4 pulse which causes the current status of the 15 function keys and 3 extra function pushbuttons to be ORed with the contents of the AC. These are the punctuation keys, control bars, and pushbuttons on the keyboard shown in Figure 1-2.

5. 703202 - Read Button Group 5 produces the RB_5 pulse which causes the current status of 18 keys on the keyboard to be ORed with the contents of the AC. These keys are labeled 0 through 9 and A through H, as shown in Figure 1-2, but may be different if the keys are replaced.

6. 703222 - Read Button Group 6 produces the RB_6 pulse which causes the current status of 18 keys on the keyboard to be ORed with the contents of the AC. These keys are labeled I through Z, as shown in Figure 1-2, but may be different if the keys are replaced.

7. 703242 - Read Knob Counters produces the RK_1 pulse which ORs the current value of the three knob counters with the contents of the AC.

8. 703262 - Read Track Ball Counters produces the RK_2 pulse which reads the current value of the three track ball counters into AC.

> NOTE: To clear the AC previous to the OR operation, bit 14 can be set in any of the above instructions. This adds 1_8 to the octal value of X, the second least significant bit of the octal instruction number.

340 Display

The 340 Incremental Display used in this system has been modified by changing:

1. The edge violation circuit to allow the flip-flops to be cleared by a new instruction.

2. The light pen flag circuit to gate the clearing of the LP enable flip-flop by the RESUME pulse and to gate the setting of the LP flag flip-flop by the temporary blind flip-flop.

3. The read to mode circuit to allow the READ TO MODE pulse to divide.

4. The transfer circuit to gate the DATA SYNC pulse by the direction flip-flop.

5. The parameter store circuit to gate the input by the OPERATE signal when performing subroutine operations.

6. The intensify circuit to gate the INT signal by the temporary dark flip-flop.

7. The stop flag circuit to allow the stop flip-flop to be sensed.

8. The escape circuit so an edge violation only produces the ESCAPE pulse in the vector continue mode.

9. The request for data circuit to add an extra input for use when performing subroutine operations.

10. The RFD flag circuit to delay the request for data signal when necessary while performing subroutine operations.

Edge Violation Circuit

The edge violation circuit has been changed by adding another method for clearing the vertical and horizontal edge violation flag flip-flops. This modification consists of adding a 6102 Inverter

in 1H24 in parallel with the two other inverters in 1F06 and 1H21, as shown on the left side of Figure 4-11 (BS-E-340-5-19). When the IOT display clear edge flags, 703302, occurs, this inverter conducts and grounds the clear gated inputs of the flip-flops, setting both flip-flops to their 0 states.

Light Pen Flag Circuit

Two modifications have been made to the light pen flag circuit. The first modification consists of substituting the TEMP BLIND (0) signal for the LP ENABLE signal to terminal X of the 4113 NAND gate in 1F08, shown in the lower left of Figure 4-12 (BS-E-340-5-20). As long as the temporary blind flip-flop is cleared (in the 0 state), this signal is -3 volts and allows the LP flag flip-flop to be set when the LP find flip-flop is set. The IOT's DLS and DRS can each sets the temporary blind flip-flop, preventing the LP flag flip-flop from being set and generating an interrupt when the light pen sees a spot.

The second modification consists of the way the RESUME pulse clears the LP enable flip-flop, as shown in the lower right corner of Figure 4-13 (BS-D-340-5-22). The RESUME pulse is applied to the pulse input of a 4127 Capacitor-Diode Gate whose level input is supplied by the 0 output of MB4. As long as the second octal digit in the resume IOT is 0 or 1, MB4 is a 0 and enables the gate, permitting the RESUME pulse to clear the flip-flop. When the second digit is 2 or 3, MB4 is a 1 and disables the gate, thereby preventing the flip-flop from being cleared.

Read to Mode Circuit

The read to mode circuit has been modified to allow the READ TO MODE (or RTM) pulse to be divided. The RTM pulse is applied directly to the set and clear gates of the LP enable flip-flop in the normal manner. These are shown in the lower right corner of Figure 4-13 (BS-D-340-5-22). The RTM pulse is also applied to a 4606 Pulse Amplifier in 1B09, (shown in the upper right of Figure 4-14, BS-E-340-5-14), which produces the READ TO MODE pulse that loads the mode register (shown in the left center of Figure 4-12). This READ TO MODE pulse is also produced by the subroutine timing chain when the display jump IOT's occur.

Transfer Circuit

The transfer circuit has been modified to gate the DATA SYNC pulse with the DIRECTION signal. This is shown at the lower left edge of Figure 4-15 (BS-E-340-5-18) as the DATA SYNC · DIRECTION pulse. This pulse is produced by a 4606 Pulse Amplifier in 1B02, shown at the center right of Figure 4-14 (BS-E-340-5-14). As long as the direction flip-flop is cleared (in the 0 state), its 0 output is at -3 volts and enables the capacitor-diode gate in the pulse amplifier, permitting the DATA SYNC pulse to trigger the pulse amplifier and start the display operation. When the direction flip-flop is set, however, the capacitor-diode gate is disabled and the display will not start.

Parameter Store Circuit

The parameter store circuit has been changed to substitute the OPERATE signal for the RI(0) signal. As long as the display is in the control (parameter) mode and the OP code is 00, the OPERATE signal is -3 volts and the circuit functions normally. However, when the OP code is any other value, the OPERATE signal is ground, preventing the parameter store circuit from operating. This is shown at the left center of Figure 4-15 (BS-E-340-5-18).

Intensify Circuit

The intensify circuit has been modified to allow the temporary dark flip-flop to gate the INT signal that unblanks the CRT. This signal is produced by a 6102 Inverter in 1F18, shown at the center right of Figure 4-14 (BS-E-340-5-14). The modification consists of placing the 0 output of the temporary dark flip-flop in parallel with the intensify inverter. Since the two signal sources share a common clamped load resistor, their outputs are ORed together. As long as the temporary dark flip-flop is cleared (in the 0 state), its 0 output is cut off and does not affect the operation of the intensify inverter. However, when the temporary dark flip-flop is set to the 1 state, its 0 output goes to ground and prevents the -3 volt INT signal from being produced.

Stop Flag Circuit

The stop flag circuit has been modified by adding a buffer inverter to the 0 output of the stop flip-flop. This produces a -3 volt BSTOP signal when the flip-flop is set (in the 1 state),

allowing the computer to sample the state of the flip-flop at any time. This inverter is the 6102 in 1E12 shown at the upper center of Figure 4-15 (BS-E-340-5-18).

Escape Circuit

The escape circuit has been modified by changing a gate so that the display can escape to the parameter mode when an edge is violated only if the display is in the vector continue mode. This is the 6115 NAND gate in 1H15, and it replaces the old 6102 Inverter in 1H24 that supplied the enabling level to the 6106 Inverter gate in 1H21. It is in parallel with the 6113 NAND gate in 1H23, and is shown in the lower right of Figure 4-15.

Request For Data Circuit

The request for data circuit has been modified by adding an additional input to the RFD pulse amplifier in 1H22, shown at the right center of Figure 4-15. This is the 1⟶ RFD pulse produced by the pulse amplifier in 1B17 at the end of each subroutine timing chain.

RFD Flag Circuit

This circuit has been modified by adding an inhibit signal to the output of the RFD inverter, as shown at the right side of Figure 4-15. The inhibit signal is produced by the 4102 Inverter in 1B17, shown above the 4301 Delay in 1B10 at the right center of Figure 4-14 (BS-E-340-5-14). This delay is activated by two conditions: The ESCAPE pulse occurs in the increment, vector, or vector continue modes and the save flip-flop is set; the parameter mode pulse (PMP) occurs when the excape bit (BR10) and save flip-flops are set. While the delay is operating, the inverter is on and produces a ground DELAY RFD signal that prevents the RFD⟶ LT request for data signal from being produced. When the delay stops operating, the DELAY RFD (and RFD⟶ LT) signal goes to -3 volts to request a new data break cycle.

Operator's Console

The general purpose experimental display system has a special operator's console added to the 340 Display. This console, shown in Figure 1-2, enables the operator to enter information into the memory of the PDP-4 via the AC by two different methods: either by depressing

a key or pushbutton; or rotating a knob or ball. These controls and their electronic circuits are independent of the PDP-4 and the 340.

Knob and Track Ball

The console table contains three knobs and a track ball for generating parameter information. Each knob is a different shape, and is directly attached to the shaft of an Incrosyn Model IC25-256-11N shaft angle encoder. Provision is made for a fourth knob and encoder to be added later. The track ball is a 3.5-inch nylon sphere which has three degrees of rotational freedom. The sphere rests on three 1.75-inch steel disks, arranged to contact the ball on its three orthogonal axes as shown in Figure 3-3. Each disk is directly attached to the shaft of the encoder. Movement of the sphere causes the shaft encoder to be rotated by twice the axial component of the rotation of the sphere.

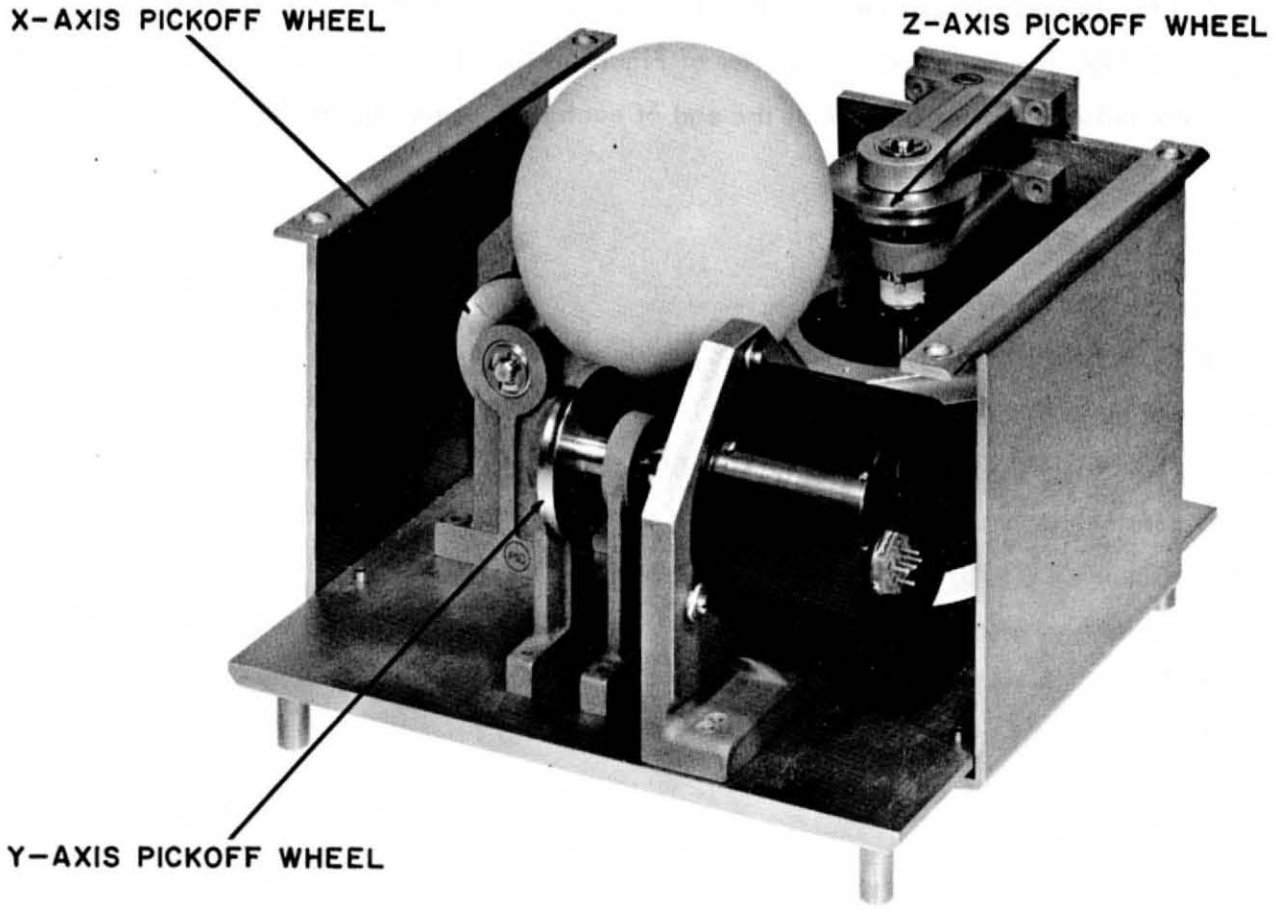

Figure 3-3 Track Ball Assembly

The shaft encoders are devices which produce electrical pulses based on the amount of rotation of the shaft, producing 256 pulses per 360 degrees of rotation, or 1 pulse per 1.4 degrees. The pulses occur on one output for clockwise rotation of the shaft, and on another output for counter-clockwise rotation. These pulses are applied to up-down counters, which store the rotational information in binary form. The pulses themselves are -3 volt pulses with a rise time of approximately 1 microsecond, duration of approximately 6 microseconds, and fall time of approximately 0.3 microseconds.

Pushbuttons

There are two groups of indicating pushbuttons on the console and three extra function pushbuttons on the keyboard, as shown in Figure 1-2. Each pushbutton, when depressed, activates a microswitch, applying -15 volts to the input of a switch filter. This is delayed, smoothed, and reduced to -3 volts which is used to enable a capacitor-diode gate in information collector 2. The PDP-4 must issue an IOT to read any information from the pushbuttons into its AC. Since the pushbuttons are mechanically operated, their contacts remain closed at least 100 milliseconds, so the PDP-4 must issue IOT's to read the information collector at least ten times a second if no information is to be lost.

Each indicating pushbutton contains two lights which are operated independently from the pushbutton switch. These lights may be replaced simply by pulling the pushbutton panel up and extracting the bulb. A separate set of blank pushbutton panels is supplied which can be used to replace any of the engraved panels.

Numbered Pushbuttons - A group of 36 pushbuttons located on the left side of the operator's console. These pushbuttons have engraved numbers on their indicator panels, and are arranged in six vertical rows. The three left-hand rows are read by IOT 703112. Their lights are turned off by IOT 703101 and lighted according to the word in the AC by IOT 703105. The three right-hand rows are read by IOT 703132. Their lights are turned off by IOT 703121 and lighted according to the word in the AC by IOT 703125.

Control Pushbuttons - A group of 18 pushbuttons located on the operator's console above the keyboard. These pushbuttons have various control words engraved on their indicator panels,

and are arranged in two horizontal rows. The IOT 704152 reads the state of these pushbuttons into the AC with the upper row occupying the left half of the word (bits 0 through 8) and the lower row occupying the right half of the word (bits 9 through 17). Their lights are turned off by IOT 703141 and are lighted by IOT 703145 according to the word in the AC, in the same order as they are read.

Extra Function Pushbuttons - A group of three pushbuttons located on the keyboard. These pushbuttons are read by IOT 703172 and occupy the three least-significant bits (15, 16, and 17). Their lights are controlled by the three corresponding relays in the Type 140, and are turned off by IOT 703161 and lighted according to the word in the AC by IOT 703165.

Keyboard - The operator's keyboard is located in the center of the console, and is recessed so that it may be covered. As shown in Figure 1-2, it consists of 51 keys arranged in the same order as the Selectric typewriter, three indicating pushbuttons, and an indicating light. The indicating light is operated by the third most-significant relay in the Type 140 with the same IOT's used to operate the extra function pushbuttons.

The alphanumeric and control keys operate microswitches in the same manner as the pushbuttons. Three IOT's are needed to read their status into the memory of the PDP-4 (via the AC). These are IOT 703212 for 0 through 9 and A through I, IOT 703232 for J through Z, and IOT 703172 for the remaining symbol keys, control keys, and pushbuttons. A separate set of key buttons is supplied which can be exchanged with the engraved set.

Interface Electronics

The controls mounted on the operator's console operate electronic circuits in the interface section. Additional control circuits are included in this section to connect and disconnect the system to the 1604A and to allow communication between the two computers. These circuits are described in the following pages.

Switch Filters

The 108 microswitches on the operator's console are in the normally closed position when they are undisturbed. Each microswitch then is applying a ground input to a 1703 Switch Filter

which produces a ground output, as shown in Figure 4-9 (BS-E-340-5-16). When a microswitch is depressed, it connects the input of the switch filter to the -15 volt bus. This causes the output to go to -3 volts after a delay of at least 2.5 milliseconds, effectively eliminating any false signal from contact bounce. When the microswitch is released, it again grounds the input of the switch filter. The output now rises back to ground after at least 5 milliseconds, again eliminating false signals due to contact bounce.

Light Driver Registers

The console table contains 54 indicating pushbuttons in two separate groups, see Figure 1-2. Each pushbutton contains two lights in parallel that can be turned on or off by the PDP-4. The computer loads an 18-bit word into its accumulator (AC) and then issues an IOT instruction which transfers this word to one of three light driver registers. Each bit of the word that is a logic 1 sets the associated flip-flop in the selected register to its 1 state, lighting the two lights in the pushbutton indicator. The IOT instruction first clears the register before loading it; so those bits which are logic 0 do not change the flip-flops from their 0 states, and the lights remain dark.

The three 18-bit light driver registers are located in racks A and B of bay 1 in the 340 Display (see Figure 1-3). Rack A contains registers 1 and 2 (LB1 and LB2), which control the lights in the group of 36 pushbuttons on the left side of the console table. Rack B contains register 3 (LB3), which controls the lights in the group of 18 pushbuttons above the keyboard. These circuits are all shown on Figure 4-16 (BS-E-340-5-13). Since the three registers operate in an identical fashion, only one is described.

Each light driver register is composed of three modules containing six flip-flops each. When a negative clear pulse (CLB) occurs, it is applied to a pulse inverter in each module, clearing all six flip-flops. A negative load pulse (LB) occurs 3.3 microseconds later and is applied to another pulse inverter in each module, producing a positive trigger gate pulse. This pulse is applied to the trigger inputs of six capacitor-diode gates. In some previous instruction the accumulator (AC) has supplied a potential for the conditioning level input of each of these capacitor-diode gates. Those gates which are grounded (logic 1) are enabled and differentiate the trigger pulse, applying a positive signal to the 1 input of the associated flip-flop that sets

it to the 1 state. The 0 outputs of the flip-flops are applied to inverters to gain power, and the resulting -3 volt signal is applied to two indicator drivers, turning them on. When the indicator drivers are on, their output goes to ground, allowing current to flow through the light bulbs from the -15 volt supply.

The IOT family 7031BX controls the operation of the three buffers. The octal digit B is decoded into 0, 2, or 4 according to MB bits 12 and 13 to select the particular register. Figure 4-10 (BS-D-340-5-16) shows how the IOT is decoded to produce the clear and load pulses. (Refer to the description of information collector 2 for a detailed operation of the decoder.)

The octal digit X may be 1, 4, or 5. If it is 1, a clear pulse is produced at T5. If it is 4, a load pulse is produced at T1 of the next PDP-4 memory cycle. If it is 5, both pulses are produced.

Knob and Track Ball Counters

The pulse outputs from the knob and track ball shaft encoders are applied to six separate 5-bit up-down counters located in rack M of bay 1 in the 340, see Figure 1-3. The block schematic of these counters is shown in Figure 4-17 (BS-E-340-5-8). These counters are divided into two sections, one for the three knob encoders and one for the three track ball encoders. Each section is cleared by a single pulse, $RKCF_1$ or $RKCF_2$, which occurs when the IOT 703244 or 703264, respectively, is issued. All the counters operate identically, so the discussion is general.

The counters use only the four less-significant flip-flops for storing the output of the shaft encoders, and the most-significant bit (subscript 4, on the right side) is used to indicate the direction of the count, as well as gating an overflow signal. The counters use 2's complement arithmetic, with 1111 assigned the value minus one. The clear pulse sets them to zero. They can accumulate up to 15 valid counts beyond zero, and then repeat with invalid data. An overflow pulse occurs on the eighth pulse when counting from zero.

The input pulses from the shaft encoder are applied to the trigger pulse input of four capacitor-diode gates, two for up counts and two for down counts. The outputs from each pair of capacitor-diode gates are ORed together by sharing a common clamped load resistor, and are applied to

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When the number in the counter goes from 7 to 8, the transition of the fourth bit is used to trigger one of another pair of capacitor-diode gates. These gates are enabled by the sign bit, so they can only be triggered by an increasing count. The outputs of the two pulse inverters are ORed together and applied to the 0 output of the counter overflow flip-flop, along with the overflow signals from all the other counters. When any counter produces an overflow pulse, it sets the flip-flop, causing a program interrupt request to be generated. The counter overflow flip-flop is shown in Figure 4-17 (BS-D-340-5-8).

Logic Level Transposition

The normal -0.5 and -3.0 volt logic levels in the 1604A are changed to -0.5 and -16 volt levels in the input and output amplifiers of the computer. The -0.5 volt level represents the logic 1 state, and the -16 volt level represents the logic 0 state. The output levels exist for one or more cycles of 12.8 microseconds each, and their transitions take from 2 to 4 microseconds. These voltage levels must be converted to the Digital standards of ground and -3 volts (both levels can represent either logic state), and the slow transitions speeded up to at least 0.2 microseconds. This is done by various circuits within the interface equipment.

1604A Output Data - Only the 19 low-order bits of the 48-bit data word from the 1604A are used as data by the PDP-4. Bits 00-17 represent the 18 bits used as one word by the PDP-4, where bit 00 is the least-significant (bit 17 in PDP-4 notation) and bit 17 is the most-significant (bit 0 in PDP-4 notation). Bit 18 is used as a control level to separate the information into either addresses or data.

The 19 bits from the 1604A output register 0^3 enter the PDP-4 at 2MD via cable D. These bits are applied directly to 4509 Level Changing Amplifiers in 3N01-04 as shown in Figure 4-18 (BS-D-4C-24-3). Each level changing amplifier (LCA) converts the CDC output voltage levels to Digital voltage levels, inverting the sense at the same time. A -0.5 volt input produces a -3 volt output, while a-16 volt input produces a ground output. The converted bits are identified by the postscript A.

Bits 00A through 17A are applied directly to the input of the 133 Data Interrupt Multiplexer. When the 1604A requests an interrupt to place data into the memory of the PDP-4 and the PDP-4 allows an interrupt, this word is written into memory during one PDP-4 memory cycle.

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Figure 4-19 (BS-D-4C-24-4), by a series of instructions in both the PDP-4 and 1604A. The 1 output of each flip-flop in the buffer is applied to one input of a 2-input positive NAND gate. The other input is a level called INPUT SETUP · ALLOW PDP-4 INTERRUPT which is ground when the word is to be transferred. Those gates which are enabled by a ground from the flip-flop (0 state) produce a -3 volt output which is applied to a 4656 Level Changing Amplifier (LCB).

The LCB's produce a -0.5 volt output when their input is at -3 volts, and a -16 volt output when their input is ground. Therefore, when a flip-flop in the information buffer is in the 0 state, a CDC logic 0 level is produced; and when the flip-flop is in the 1 state, a CDC logic 1 level is produced.

Note that the bit numbering in the word is reversed between the PDP-4 and the 1604A. The most-significant bit from the PDP-4 is MB_0. This is applied to the IB_{17} flip-flop, which produces bit 17 for the 1604A. In a similar fashion the numbering of all other bits is reversed.

1604A Input Control Signals - When a data word is loaded into the information buffer, the input data ready flip-flop is set and applies a -3 volt level to an LCB in 3L24, see Figure 4-20 (BS-D-4C-24-9). This LCB then produces a -0.5 volt logic 1 level for the 1604A, called the INPUT DATA READY control signal.

The OUTPUT DATA RESUME control level is produced in a similar manner by an LCB which is controlled by the OD RES flip-flop, shown in Figure 4-18 (BS-D-4C-24-3). This flip-flop is set whenever the 1604A loads the interface address register or when the 133 Data Interrupt Multiplexer transfers the location in the interface address register to the memory address register of the PDP-4. The flip-flop is cleared by the ODRA level whenever the 1604A has information to be transferred to the PDP-4.

The INPUT INTERRUPT, OUTPUT INTERRUPT, and SENSE RESPONSE control signals are generated by the three LCB's in 3L24 shown in the upper right of Figure 4-6 (BS-E-4C-24-2). The INPUT INTERRUPT signal is -0.5 volts (logic 1) when the input select, allow input interruption, and input interrupt flip-flops in the interface control are all set to 1. The 0 outputs of these flip-flops are applied to a positive NAND gate in 2L23 which controls the LCB. Similarly, the OUTPUT INTERRUPT signal is controlled by the output select, allow output interruption, and output interrupt flip-flops.

The SENSE RESPONSE is also developed by an LCB that is controlled by two positive NAND gates in 3L21, an inverter in 3L05, and another inverter in 3L25. The outputs of these circuits are ORed together by sharing a common clamped load resistor. The SENSE RESPONSE signal is a logic 0 for 4 microseconds whenever an INPUT or OUTPUT FUNCTION READY or an INPUT or OUTPUT SENSE READY signal occurs. It remains a logic 0 if either of the sense signals was not meant for the display system and, when sensing the conditions of the display system, if the selected flip-flop is not set to a 1. The SENSE RESPONSE signal goes to a logic 1 if the selected flip-flop is set.

Phone Number Decoding

The general purpose experimental display system is nominally device 5 on channels 5 and 6 of the 1604A. The device number is an octal digit determined by function bits 9, 10, and 11 (1604A notation), and is referred to as the device's phone number.

Bits FB_9A, $FB_{10}A$, and $FB_{11}A$ are applied to inverters in 3L05, located at the lower left of Figure 4-6 (BS-E-4C-24-2) to obtain their complementary levels. The six levels are then applied to the inputs of a 4150 Binary-to-Octal Decoder in 3L06. One of the eight outputs of the decoder is -3 volts and the other seven are ground, depending on the octal value of the 3-bit input. Output number 5, which is jumpered to terminal E on terminal strip 3L62, applies the phone number to the wrong number inverter. Two complementary signals are thus produced, the phone number and the wrong number, each of which is -3 volts for assertion.

EXF Decoding

The interface control circuits shown in Figure 4-6 (BS-E-4C-24-2) decode the external function (EXF) sense and select instructions from the 1604A. These instructions are first examined to see if they are addressed to this system. If they are not (wrong phone number), the control and status flip-flops are cleared, disconnecting the system from the 1604A. If the EXF instruction is addressed to this system, one of the three select flip-flops at the top center of Figure 4-6 is set, allowing function bits FB_0 through FB_8 to be decoded. These either set and/or clear the control and status flip-flops or produce a sense response from one or more of them.

Each of the four types of EXF instruction produces an identifying level. These four levels are applied to level converting amplifiers in 3L01, located at the upper left of Figure 4-6. The outputs of these LCA's are applied to a negative NOR gate in 3L04, producing a ground level whenever any one of the four 1604A levels is a logic 1. This signal is complemented by an inverter in 3L05 and applied to a pulse generator in 3L07, which produces a negative 400-nanosecond pulse when the leading edge of its input reaches -2.5 volts. This changes the 2-microsecond rise time of the 1604A signal to the faster 10 nanosecond rise time needed for Digital pulse operation.

Sense EXF's - Both the converted INPUT SENSE READY (ISRA) and OUTPUT SENSE READY (OSRA) levels are applied to two inverters at coordinate B3 whose outputs are ORed together by sharing a common clamped load resistor. If the EXF instruction is a sense instruction, these inverters produce a ground output that is complemented by a third inverter, applying a -3 volt enabling level to two 2-input negative NAND gates. One of these gates is enabled and one disabled by the complementary PHONE NUMBER and WRONG NUMBER device selection levels. These gates enable the two capacitor-diode gates on the set and clear inputs of the sense select flip-flop. If the EXF instruction is addressed to this system (phone number = 5), the set gate is enabled and the clear gate disabled.

The negative pulse from the PG is applied to a delay in 3L08, starting it operating for a fixed period of time. (This is marked as 4 microseconds, but may be reduced. A minimum of 1 microsecond is necessary to allow the capacitor-diode gates to be set up.) During the time the delay is operating, a -3 volt level is produced at terminal J. This signal is inverted and applied to the input of the sense response level converting amplifier (the LCB at the upper right of Figure 4-6), producing a -16 volt logic 0 output. This prevents the SENSE RESPONSE signal from being produced if the EXF instruction is meant for another device on the same channels.

The delay produces a negative pulse at the end of its operating period. This signal, named the DELAY READ IN pulse, is applied to a pulse inverter in the select flip-flop module in 3L09 and to the input of a second delay in 3L11, located in the lower left of Figure 4-6. The pulse inverter produces a positive trigger gate pulse which is applied to all the capacitor-diode gates on the module. This sets or clears the sense select flip-flop, depending on which capacitor-diode gate is enabled.

The sense select flip-flop is initially cleared to the 0 state by the power clear (PWR CLR) pulses. In this state it produces a -3 volt signal from its 0 output. This is inverted and applied to the input of the sense response LCB, producing a -16 volt logic 0 output. When the flip-flop is set to the 1 state, a ground is applied to the inverter at the upper right of Figure 4-6 allowing NOR gate in 3L21 to control the sense response LCB.

Function EXF's - The input select and output select flip-flops, located at the top of Figure 4-6, provide decoding levels for the control and status circuits in the interface equipment. These flip-flops are initially cleared to their 0 states by the PWR CLR pulses. Each EXF select instruction that occurs sets or clears one of them. These flip-flops are controlled by the IFRA (INPUT FUNCTION READY) or OFRA (OUTPUT FUNCTION READY) levels and the complementary WRONG NUMBER and PHONE NUMBER device selection levels in the same manner as the sense select flip-flop.

Control and Status Flip-Flops

The nine control and status flip-flops in the interface equipment make possible communication between the 1604A and PDP-4 computers. Both computers can sense the current state of all nine flip-flops at any time. The 1604A can set or clear eight of these, and the PDP-4 can set or clear four.

All these flip-flops are initially cleared by the PWR CLR pulses which occur when the PDP-4 is first turned on. Seven of the eight flip-flops in 3L14 and 3L18 are set or cleared every time an EXF select instruction addressed to this system occurs; and two out of four of these are cleared by every EXF instruction addressed to any other device on the same channels. This is accomplished by the DELAY READ IN pulse generating trigger pulses that are applied to the set and clear capacitor-diode gates for these flip-flops and the EXF instruction decoding which enables the appropriate gates. (The 4-microsecond delay of the trigger pulses may be reduced to as little as 1 microsecond).

1604A Input - When the 1604A is to receive information from the display system, the input setup flip-flop must be set to specify the direction of transfer; the allow input interrupt flip-flop must be set if it is permissible for the PDP-4 to interrupt the 1604A program, and the input interrupt flip-flop (flag 1) must be set when the information is ready to be transferred.

The INPUT FUNCTION READY EXF sets the input select flip-flop when the instruction is addressed to this system. This generates a -3 volt INPUT SEL(1) enabling level which is applied to one of the three inputs of the negative NAND gates which control the three flip-flops. These gates also receive the IFRA level on another input to insure that only this EXF is decoded, not some previous one which set the input select flip-flop. The third input for these gates is a converted function bit. Since any combination of these bits (in pairs) can occur, microprogramming of the instruction is possible. Table 3-3 lists the operation of the various function bits.

> NOTE: An EXF instruction that does not enable a capacitor-diode gate does not affect the state of a control and status flip-flop.

The IFRA level is applied to a 2-input negative NAND gate in 3L12 (located at the bottom center of Figure 4-6) along with the WRONG NUMBER signal. The output of this gate is ORed with the output of the decoding gates which clear the input setup and allow input interrupt flip-flops. Therefore whenever an INPUT FUNCTION READY EXF instruction is addressed to some other device, these flip-flops are cleared, disconnecting the display system from the common channels.

The PDP-4 can inform the 1604A that it has information ready to be transferred by setting the input interrupt flip-flop. This is accomplished with the IOT IGI, 703441, which produces a pulse at time T4. This pulse is complemented by an inverter in 2L16, located in the lower right of Figure 4-6, and applied to the 0 output of the input interrupt flip-flop. The IOT CGI, 702401, clears the flip-flop in a similar manner.

1604A Output - When the 1604A is to send information to the display system, the following flip-flops must be set: 1. Output setup, specifying the direction of transfer. 2. Allow output interrupt, if the 1604A can be interrupted to supply the information. 3. Output interrupt (flag O), when the information is ready to be transferred. 4. Flag P, to signal the need of an interruption to the PDP-4. 5. Allow PDP-4 interrupt to effect the transfer. The output setup, allow output interrupt, and output interrupt flip-flops are set and cleared in the same manner as the corresponding input flip-flops. Table 3-3 lists the function bits which control these flip-flops.

TABLE 3-3 FUNCTION BIT ASSIGNMENTS

Bit	EXF Sense Instructions		EXF Function Instructions	
	Input	Output	Input	Output
FB_8	Sense INPUT SETUP	Sense OUTPUT SETUP	Set INPUT SETUP	Set OUTPUT SETUP
FB_7			Clear INPUT SETUP	Clear OUTPUT SETUP
FB_6	Sense ALLOW INPUT INTERRUPT	Sense ALLOW OUTPUT INTERRUPT	Set ALLOW INPUT INTERRUPT	Set ALLOW OUTPUT INTERRUPT
FB_5			Clear ALLOW INPUT INTERRUPT	Clear ALLOW OUTPUT INTERRUPT
FB_4	Sense INPUT INTERRUPT	Sense OUTPUT INTERRUPT	Set INPUT INTERRUPT	Set OUTPUT INTERRUPT
FB_3			Clear INPUT INTERRUPT	Clear OUTPUT INTERRUPT
FB_2		Sense FLAG P		Set FLAG P
FB_1		Sense ALLOW PDP-4 INTERRUPT		Clear FLAG P
FB_0		Sense LIMBO Switch	Clear LIMBO	Set LIMBO

NOTE: It is possible to have simultaneous 2-way communication between the 1604A and PDP-4 if the PDP-4 provides information and the 1604A provides the storage location of this information.

The flag P flip-flop is set and cleared in the same manner as the output interrupt flip-flop. However, no request for a data break can be generated unless the allow PDP-4 interruption flip-flop is also set. The capacitor-diodes for this flip-flop are permanently disabled so the 1604A cannot control it. The PDP-4 sets and clears it with the IOT's SGP (702242) and CGP (702202), respectively.

Interface Address Register

This register consists of the 13-bit up counter and control circuits shown in Figure 4-18 (BS-D-4C-24-3). It is used to specify the location in the memory of the PDP-4 of a word for transfer between the 1604A and the PDP-4. When a block of successive words is to be transferred, the initial (or starting) location is loaded into the counter, and each transfer operation increments the counter by 1. Either the 1604A or the PDP-4 can load the counter, and the PDP-4 can read the address contained in the counter into its accumulator.

PDP-4 Operation - The interface address register is controlled by three PDP-4 instructions:

1. IOT Clear Generator Address, CGA, 702301. This instruction is decoded by a 4605 Pulse Amplifier in 3F01, located at the left of Figure 4-21 (BS-D-4C-24-15), producing a positive CGA pulse at time T5. The CGA pulse is applied to a pulse amplifier in 3M04, located in the center of Figure 4-18 (BS-D-4C-24-3), producing a pulse that is applied to another pulse amplifier in 3H05 which produces the positive CLR IAR pulse. This pulse is applied to the direct clear input of all the interface address register flip-flops, IAR_5 through IAR_{17}, setting them to their 0 states.

2. IOT Load Generator Address, LGA, 702302. This instruction is decoded in a similar manner as the CGA instruction, but a negative LGA pulse is produced at time T7. This pulse is applied to a pulse inverter in each counter module, producing trigger gate pulses that are applied to the set capacitor-diode

gates. Those gates whose conditioning level inputs have been at ground (logic 1) are enabled setting their associated flip-flops. The buffered outputs of the accumulator supply the conditioning levels for the gates.

NOTE: These two operations can be combined by the IOT 702303.

3. IOT Read Generator Address, RGA, 702304. This instruction reads the address held by the IAR into the same bit locations of the AC. This is explained in the information collector description.

1604A Output Operation - When the 1604A places information into its output buffer for transfer to the PDP-4, the first word must be the location in the memory of the PDP-4 where the first data word is to go. Address information is specified by a 1 in bit 18 (1604A notation), whose converted and inverted level applies an enabling ground to a positive NAND gate in 3M03, located near the left center of Figure 4-18 (BS-D-4C-24-3). The output setup flip-flop has been set, enabling another input of this gate. The third input is supplied by the allow PDP-4 interruption flip-flop; therefore, when the flip-flop is set, the gate produces a -3 volt level that enables a capacitor-diode gate in the 4606 Pulse Amplifier module in 3M04, and is complemented to supply an enabling ground to an inverter gate in 3M01.

After the 1604A has set up the control and status flip-flops, it activates the output buffer. The OUTPUT DATA READY signal then goes to -0.5 volts, and its converted level, ODRA, goes to -3 volts. This triggers the pulse generator in 3M06, producing a 400-nanosecond negative ODRP pulse that activates the two enabled gates. The pulse amplifier then produces a / J▶ IAR pulse 2.5 microseconds later.

The / J▶ IAR pulse is applied to one input of the 13 NAND gates on the top of Figure 4-18. Each of these gates which is enabled by a -3 volt logic 1 input produces a positive pulse that is applied to the 0 output of the associated flip-flop. This sets the flip-flops to their 1 states, thereby loading the address information into the counter by a jam transfer.

The / J▶ IAR is also applied to a 4113 NAND gate in 3M10, which, when enabled by the input setup flip-flop, applies a ground to the 0 output of the output data resume (OD RES) flip-flop in 3M09, which sets it to the 1 state. This produces a -3 volt OD RES B signal from the

buffer inverter in 3L25 that is converted by an LCB to the -0.5 volt OUTPUT DATA RESUME level. This signals the output buffer of the 1604A that the first word has been accepted; so it loads the first information word into the buffer. When this is done, the OUTPUT DATA READY signal again becomes a logic 1 (it went to a -16 volt logic 0 state during the process of changing the words in the buffer) and generates a new ODRP pulse. If the new word is another address (bit 18 is 1), the previous cycle repeats itself. This can continue until no new address is held by the output buffer of the 1604A, and the OUTPUT DATA READY signal does not occur.

If the new word is data and not an address (bit 18 is 0), the NAND gate at the left corner of the logic is disabled and prevents the ODRP pulse from clearing and loading the counter. Since the 1604A can only present address information to the PDP-4 in 2-way communication, the input setup flip-flop is cleared and the 4114 NAND gate at below and to the right of the OD RES flip-flop is activated. This enables a capacitor-diode gate in 3M02, allowing it to pass the ODRA pulse to a pulse inverter, producing a positive pulse that sets the interface data request (ID REQ) flip-flop.

When the ID REQ flip-flop is set to the 1 state it generates a negative DI REQ_1 data request signal. This is applied to the 133 Data Interrupt Multiplexer on channel 1, causing a data break to occur at the end of the current PDP-4 memory cycle. In the following break cycle at time T1 a DI ADD ⟶ MA pulse is produced which reads the address held by the IAR into the memory address (MA) register of the PDP-4.

Since information is being read into the memory of the PDP-4, the input setup flip-flop is cleared and the output setup flip-flop is set. This cuts off an inverter in the lower right corner of Figure 4-18, producing the DI IN-OUT signal, which is -3 volts for information going into the memory of the PDP-4.

The DI ADD ⟶ MA pulse produces an address accepted signal called DI ADD ACCEPT-1 that is applied to two 4113 NAND gates in Figure 4-18 (BS-D-4C-24-3) at right center, and to a pulse inverter in 3M09 that clears the ID REQ flip-flop. One of the gates produces a positive pulse which complements the least significant flip-flop (IAR_{17}) in the counter, increasing the number held by one. The other NAND gate is enabled by the output setup flip-flop when it is in the 0 state, and produces a positive pulse that sets the OD RES flip-flop, producing an

OUTPUT DATA RESUME level. (This flip-flop is cleared each time the OUTPUT DATA READY signal goes back to the logic 0 state.) At time T3 (2.0 microseconds later) the data in bits 0A through 17A is strobed into the memory buffer (MB) of the PDP-4.

If more information is to be placed into the memory of the PDP-4, this cycle repeats itself. When the output buffer of the 1604A transfers the last information word, it does not produce another OUTPUT DATA READY signal and the process halts. Note that the OD RES flip-flop is cleared, removing the OUTPUT DATA RESUME signal, and that the IAR holds an address one greater than the last word transferred.

Simultaneous Input and Output Operation - Simultaneous communication between the two computers is limited to the transfer of location information from the 1604A to the PDP-4 and data information from the PDP-4 to the 1604A. Effectively, the 1604A asks the PDP-4 for information contained in certain specified locations. After setting and clearing the appropriate control and status flip-flops, the 1604A places the location information in its output buffer, and transfers it to the interface address register when the buffer is activated, as explained in the 1604A output description. This in itself does not generate the necessary data request signal. The 1604A must ignore the OUTPUT DATA RESUME signal, or it will continue to place addresses in the IAR.

When the input buffer is activated, the INPUT BUFFER ACTIVE signal becomes -0.5 volts (logic 1), and its converted level IBAA goes to -3 volts. This is complemented and applied to one input of the 4114 NAND gate in 3M3, shown in the lower right of Figure 4-18. This gate is activated when the output select flip-flop is 0, the INPUT DATA READY signal is ground (logic 0), and the OUTPUT DATA READY signal is -3 volts (logic 1); therefore the gate produces a negative pulse that is applied to a capacitor-diode gate in 3M02. If this gate is enabled (by the input setup and allow PDP-4 interruption flip-flops), it passes the pulse to its pulse inverter, which produces a positive pulse that is applied to the 0 output of the ID REQ flip-flop, generating the DI REQ_1 data break request.

Since the input setup flip-flop is in the 1 state, the inverter at the lower right of Figure 4-18 is turned on and produces a ground DI IN-OUT signal. This is applied to the NOR gate in 2L16 of the Type 133 Data Interrupt Multiplexer (shown near the left center of Figure 4-3, BS-D-133-0-1) which produces the DI IN-OUT signal. Both of these signals are -3 volts if data is to be taken out of memory.

Because this is a request for data, DI IN-OUT is ground and allows memory to be strobed at time T3. This places the word into the memory buffer (MB). At time T5 another pulse occurs which loads this word into the interface input information buffer (IB) and produces the INPUT DATA READY signal. The 1604A must read this word into its input buffer. If no more information is requested, the INPUT DATA READY signal remains a logic 1.

If another word of information is requested from the PDP-4, the 1604A must again load the location of the word into the IAR as described previously. However, the input buffer is still active, so the data break request is produced in another manner. This is accomplished with the INPUT DATA RESUME signal, which goes to a logic 1 when the input buffer is ready for another word. The IDRA signal produces an IDRA pulse that is applied to a capacitor-diode gate in 3M02, shown at the bottom of Figure 4-19 (BS-D-4C-24-4). This gate is enabled by -3 volts on its conditioning level input. Since the 1BAA (0) level still exists, the IDRA pulse is complemented, clearing the input data ready flip-flop and temporarily removing the INPUT DATA READY signal. This sequence can be repeated as long as necessary, and is terminated when the 1604A stops supplying addresses and does not produce an INPUT DATA RESUME signal.

Interface Input Information Buffer

All information that is transferred from the memory of the PDP-4 to the input buffer of the 1604A must go through the interface input information buffer (IB). This is a simple 18-bit register whose inputs are obtained directly from the memory buffer (MA) and whose outputs are converted to the required CDC levels. Figure 4-20 (BS-D-4C-24-4) shows this register and its control circuits.

The IB can only be cleared and loaded when the input setup flip-flop is set. This applies an enabling level to a capacitor-diode in 3M04, allowing the ADDRESS ACCEPTED (DIADD ACCEPT-1) pulse to trigger a pulse amplifier at time T1 of an output data break cycle. This pulse amplifier produces a negative 0 ⟶ IB pulse that is applied to a pulse inverter in each IB flip-flop module, clearing all of the flip-flops to 0. One of these flip-flops produces a -3 volt RESET signal which enables another capacitor-diode gate in 3M04.

At time T3 the memory is strobed and transfers its word into the MB. At time T5 the PDP-4 applied a pulse to the enabled capacitor-diode gate in 3M04, triggering its associated pulse amplifier. This pulse amplifier produces a negative 1⟶ IB pulse that is applied to a pulse inverter in each IB flip-flop module and to a capacitor-diode gate in 3M02. Each pulse inverter produces a positive trigger pulse that is applied to the pulse inputs of all the capacitor-diode gates in the module. Those gates which have ground (logic 1) signals applied to their conditioning level inputs from the MB pass the pulse to the associated flip-flop, setting it to the 1 state. In this way the IB is cleared and loaded by every break cycle when the input setup flip-flop is set.

If the allow PDP-4 interruption flip-flop is also set, it applies an enabling level to a 4113 NAND gate in 3M10 and to a capacitor-diode gate in 3M02. The NAND gate produces a ground INPUT SETUP · ALLOW PDP-4 INT signal that is applied to one input of 18 2-input 4112 NAND gates, enabling each positive gate. The other input of each of these gates is obtained from an IB flip-flop, whose output is jumpered internally to the 0 side. These signals are ground when the flip-flop is in the 1 state and -3 volts when it is in the 0 state. Therefore, those flip-flops which hold 1's activate their associated NAND gates, producing a -3 volt output. These signals are applied to level converting amplifiers (LCB's), which change them to their required CDC levels.

At the same time the 1⟶ IB pulse is passed by the capacitor-diode gate in 3M02 to its pulse inverter. This produces a positive pulse that is applied to the 0 output of the input data ready flip-flop, setting it to the 1 state. The flip-flop then applies a -3 volt signal to an LCB, producing the -0.5 volt INPUT DATA READY signal. The input data ready flip-flop is cleared by the IDRA pulse from the INPUT DATA RESUME signal, from the 1604A's input buffer, and also by the IBAA(0) signal when the INPUT BUFFER ACTIVE signal is a logic 1. When the input

data ready flip-flop is cleared its 1 output is ground and cuts off a 4102 inverter in 3L25, producing the IDBR(1) signal.

Display Address Counter

The display address counter (DAC) is a 13-bit up counter that functions as a program counter for the 340. It contains an address in the memory of the PDP-4 of a word that is to be transferred to the 340 by the next data break cycle. The DAC is directly loaded from three sources: either the accumulator (AC) of the PDP-4; the buffer register (BR) of the 340; or the display save register (DSR). Each time a data word is transferred to the 340 the DAC is incremented, so it always contains a number one greater than the address of the current data word. The DAC is also incremented whenever the 340 receives a display resume (DSR) or operate instruction which has the skip bit set (bit 9 = 1).

The DAC, shown in the lower half of Figure 4-20 (BS-D-4C-24-9), consists of two 4222 7-Bit Counter modules. All except one of the flip-flops on each module have only one output terminal available. This terminal is internally jumpered to the 0 side of the flip-flop, which is -3 volts when the flip-flop is in the 0 state and ground when the flip-flop is in the 1 state. The 0 output of each flip-flop therefore applies a ground to a buffer inverter, producing the -3 volt logic 1 output signal [BDAC5(1) through BDAC17(1)] when the flip-flop is set.

The DAC is cleared by the CLR DAC pulse, which occurs whenever the PDP-4 issues either a display jump (DJP) or display jump and save (DJS) instruction to the 340. This negative pulse is applied to a pulse inverter in each module, producing positive pulses that are applied to the direct clear inputs of all the flip-flops. The clear pulses are 1 microsecond in duration to override any carries that may be produced in the counter.

The 13 buffered address bits from the AC are applied to the conditioning level inputs of the set capacitor-diode gates in the DAC. These bits are ground in the logic 1 state, enabling the gates after approximately 1 microsecond. Whenever the PDP-4 issues a display load address counter IOT (DLA, 700606), a LOAD DAC pulse is produced at time T7. This is applied to a pulse inverter in each module, producing positive trigger pulses that are applied to the pulse inputs of the set capacitor-diode gates. Those gates which have been enabled by grounds (since the previous LAC instruction) pass the pulse to their associated flip-flops, setting them to their 1 states.

The display save register (DSR) and the address bits of the buffer register (BR) are loaded into the DAC in the same manner. Each bit is applied to the conditioning level input of a negative capacitor-diode gate. (These bits are -3 volts for logic 1.) When a negative trigger pulse occurs, those gates which are enabled activate their associated pulse inverters. The outputs of each pair of pulse inverters are ORed together and applied to the 0 output of their associated flip-flop. Every gate which is triggered causes the associated flip-flop to be set, jam transferring the selected address. The DSR is loaded into the DAC by the DSR ⟶ DAC pulse, which occurs whenever the 340 escapes from the increment, vector, or vector continue modes or the escape bit is set in an operate instruction; provided the save flip-flop is set (DSR contains an address). The address portion of the buffer register is loaded into the DAC by the BR ⟶ DAC pulse, which occurs on any DJP or DJS instruction.

Each time the counter is incremented, a positive pulse (+1 ⟶ DAC) is applied to the complement input of the least-significant flip-flop, DAC_{17}. This causes the flip-flop to reverse its state. The 1 output of each single-terminal flip-flop is internally connected to the complement input of the next more-significant flip-flop. When any of these flip-flops change from the 1 state (1 output is -3 volts) to the 0 state (1 output is ground), the positive transition complements the flip-flop. In this manner a carry signal can ripple upwards (at a 50 nanosecond per flip-flop rate) whenever the counter is incremented. Note that the 1 output of the most-significant flip-flop in 3K14 is applied to the output terminal of the least-significant flip-flop in 3K11 as the letter is not used. This terminal is jumpered to the 1 side to complete the path to the complement input of the next more-significant flip-flop.

The buffered outputs of the DAC are applied directly to conditioning level inputs of negative capacitor-diode gates in 3K19 and 3K20, and to one input each of 13 2-input negative 4113 NAND Gates in 2K15, 2K16, and 2K21 shown in Figure 4-22 (BS-D-4C-24-11). The capacitor-diode gates load the address held by the DAC into the display save register (DSR) with the DAC ⟶ DSR pulse, which occurs whenever a DJS instruction is issued by the PDP-4. The NAND gates apply the address held by the DAC to channel 2 of the 133 Data Interrupt Multiplexer's address information collector whenever the direction of transfer is from the 340 to the PDP-4. This is implemented by the DI $IN\text{-}OUT_2$ level from the direction flip-flop.

Display Save Register

The display save register (DSR) is a 13-bit register used to save the current address held by the display address counter (DAC) when the PDP-4 issues a display jump and save instruction DJS, 600000. The DSR can also be loaded directly from the AC by the display load save register IOT (DLS, 702602). Whenever the DSR is loaded, the save flip-flop is set to its 1 state.

The address held in the DSR is automatically read back into the DAC whenever the display escapes from the vector, vector continue, or increment modes or when an operate instruction is issued by the PDP-4 with the escape bit (bit 10) set to 1. The address is also read into the PDP-4 as part of a subroutine return instruction by the display deposit save register instruction, DDS.

The DSR consists of two 4220 8-Bit Buffer Register modules in 3K21 and 3K22. It is shown on the top of Figure 4-20 (BS-D-4C-24-9). Each of these flip-flops has only one output terminal available: this is internally jumpered to the 0 output of the flip-flop. These outputs are buffered by inverters, producing the BDSR5 through BDSR17 output levels from the save register.

The DSR is cleared by the 0 ⟶ DSR pulse (shown on Figure 4-21 as the CLR DSR pulse). This pulse is generated by the 4606 Pulse Amplifier in 1B14 at the upper center of Figure 4-14 (BS-E-340-4-14), which is activated directly by the display clear save register IOT (DCS, 702601) and by the pulse which starts the subroutine timing chain, gated by the display jump and save instruction level DJS. The DSR is loaded directly from the AC by the display load save register IOT (DLS, 702602) in the same manner as the address counter.

> NOTE: The DCS and DLS instructions can be combined by the IOT 702603.

The current state of the DAC is loaded into the DSR by the DAC ⟶ DSR pulse. This pulse is produced by a 4606 Pulse Amplifier at the top of Figure 4-14 (BS-E-340-5-14). This PA is activated by the second pulse in the subroutine timing chain (which occurs 3 microseconds after the first pulse), gated by the display jump and save level DJS.

The buffered outputs of the DSR are applied to capacitor-diode gates which load the address back into the DAC and to 4113 Negative NAND Gates which load the address into the address mixer of the 133 Data Interrupt Multiplexer. These NAND gates, shown in Figure 4-22 (BS-D-4C-24-11), are controlled by the TO⟶133 level produced by the direction flip-flop. This signal is -3 volts (enabling all the gates) when the flip-flop is cleared, indicating that the 340 is placing information into the memory of the PDP-4. The output of these NAND gates goes through the 18 positive NOR gates shown in Figure 4-22, producing the DI ADD 5-2 through DI ADD 17-2 bits. These are applied to the information collector shown in Figure 4-3 (BS-D-133-0-1).

Subroutine Timing Chain

A chain of timing pulses controls the operation of this display when it is in the control mode. These pulses are produced by the circuit shown across the top of Figure 4-14 (BS-D-340-5-14). Most of the pulses control the operation of the display address counter and the save register when the display is in the control mode, but a few are used when ending certain subroutines.

When the PDP-4 sends to the 340 an instruction which places the display in the control mode (referred to as the parameter mode in the 340 maintenance manual), a parameter mode level (PM) is generated by the mode decoder. This signal is applied to a 4115 NAND gate in 1B15, at the upper center of Figure 4-14, along with the $\overline{\text{OPERATE}}$ level. If the instruction is a DJP, DJS, or DDS, the gate is enabled and grounds the emitter of a Type 1102 Inverter. The intensify delay pulse, IDP, occurs 3.3 microseconds later and is passed by the inverter, activating in 1B12 a 4604 Pulse Amplifier which produces the first subroutine timing pulse, ST0. This pulse is applied in 1B13 to an inverter which triggers a 3.0-microsecond delay. At the end of this period the second subroutine timing pulse, ST1, is produced. This pulse is applied to another inverter in 1B11 which triggers a second 3.0-microsecond delay. At the end of this period the third subroutine timing pulse, ST2, is produced.

> NOTE: These delays may be exchanged for Type 1304 Delays and adjusted for a minimum time of 1.0 microsecond.

The display jump instruction, DJP, clears and loads the display address counter with the specified address held in the buffer register and sets the mode decoder flip-flops to the state desired

for the next instruction. The BR is loaded 2.8 microseconds after the instruction occurs, so the transfer must occur at least 1 microsecond later. Since another instruction requires that ST1 clear the DAC, the transfer actually takes place almost 10 microseconds after the instruction occurs. ST1 is applied in 1B08 to a 4113 NAND Gate which is enabled by the BBR0(1) signal. (This bit enables the gate on both the DJP and DJS instructions.) The output of the gate is applied to a 4604 Pulse Amplifier in 1B12, producing the 0⟶DAC pulse that clears the display address counter.

The 0⟶DAC pulse is also produced when the display escapes from the increment, vector, or vector continue modes in which the save flip-flop was set, and by the CGA IOT, 700602. This is accomplished by the circuits in the center of Figure 4-14 which produce the SAVE PMP pulse. When this occurs, the request for data must be delayed for 3.0 microseconds. The 4301 Delay in 1B10 does this, as explained in the 340 changes.

The ST2 pulse is similarly applied to a capacitor-diode gate in 1B14 that is enabled by the same BBR0(1) signal. This gate activates its associated pulse amplifier, producing the BR⟶DAC pulse which loads the address held by the BR into the DAC. The ST2 pulse is also applied in 1B09 to another capacitor-diode gate that is permanently enabled by a -3 volt level on its conditioning level input. This activates the associated pulse amplifier, producing the READ TO MODE pulse which is applied to the read-in gates of the mode decoder flip-flops. These flip-flops are holding 000, and this pulse sets them to the present value of BR bits 2, 3, and 4 for the mode of the next instruction.

The ST2 pulse is also applied to an inverter in 1B17, producing the I⟶RFD pulse. This is applied to the request for data pulse amplifier in 1H22, shown in Figure 4-15 (BS-E-340-5-18) at the lower right side, which produces the RFD pulse. This pulse is also applied to the 4604 Pulse Amplifier in 1H22, producing the RFD pulse which sets the RFD flip-flop to its 1 state and generates a RFD ⟶ LT request for data signal. This is returned to the 133 Data Interrupt Multiplexer as the DI REQ_2 signal.

The display jump and save instruction, DJS, clears and loads the address save register with the current address held by the DAC during the previous display cycle and sets the save flip-flop to its 1 state, as well as the operations of the DJP instruction. In this case ST0 is applied to a

capacitor-diode gate in 1B14 which is enabled by the DJS level from the subroutine instruction decoder. This produces the 0⟶DSR pulse produced by the display clear save register IOT (DCS, 702601), which is generated by the device selector IOT decoder shown in Figure 4-21 (BS-D-4C-24-15). In a similar manner ST1 generates the DAC⟶DSR pulse by activating the pulse amplifier in 1B14. (The DAC⟶ DSR pulse occurs 75 nanoseconds before the 0⟶DAC pulse.) The DAC⟶ DSR pulse loads the save register and is applied to an in verter in 1B17 which sets the save flip-flop.

The display deposit save register instruction, DDS, transfers the address held by the save register to the PDP-4, clears the temp blind and save flip-flops, and sets the mode decoder flip-flops to the states desired for the next instruction. This is accomplished by applying the DSR bits to the address portion of the 133 Data Interrupt Multiplexer's input information mixer on channel 2 and setting the rest of the bits (0 through 4) to 10000, which represents a DJP instruction to this address. This information is read into memory at the location specified by the address in the DDS instruction, which is contained in the BR.

The subroutine instruction decoder produces a -3 volt DDS level which is applied to two negative NAND gates in 1B08 and 1B19. The IDP pulse then starts the timing chain. Pulses ST0 and ST1 do not do anything, as their gates are disabled. However, ST2 produces the RTMP and 1⟶ RFD pulses which reset the mode flip-flops with the current mode bits and set the request for data flip-flop. ST2 is also applied to the two NAND gates which are enabled by the DDS level setting the direction flip-flop to its 1 state and the save flip-flop to its 0 state. (The read-in capacitor-diode gates are permanently disabled by -3 volts on their conditioning level inputs to prevent the display load save register IOT, DLS, from affecting them.)

Setting the direction flip-flop produces a -3 volt DATA IN level from its 0 output buffer inverter. This signal is applied to the other group of NAND gates in the DDS address selector circuit, enabling those gates which are connected to the BR. In this manner the address part of the DDS instruction is first read into the BR, then transferred to the address mixer of the 133 Data Interrupt Multiplexer, and finally loaded into the memory address register (MA) of the PDP-4.

The DATA IN signal is also applied to the data interrupt control part of the real time section, where it produces a level that inhibits the strobing of memory.

The direction flip-flop is cleared by the clear buffer register pulse CLBR, which occurs at the start of each display cycle. The IOT display load address counter (DLA, 700606) also clears this flip-flop as well as the save flip-flop. When the direction flip-flop is cleared, it produces the -3 volt TO 340 level from its 1 output buffer inverter. This signal is applied to the group of NAND gates of the DDS address selector circuit, Figure 4-14 (BS-D-340-5-14), enabling those gates which are connected to the DAC.

Operation Code Decoder

What is referred to as the parameter mode (PM) in the 340 maintenance manual is the control mode in this display. When the 340 decodes bits 2, 3, and 4 of its instruction word, additional circuitry decodes bits 0 and 1 to select the way in which the rest of the bits will be interpreted. If bits 0 and 1 are both 0, the information in the word is used to change the control registers and flip-flops in the display, much as in the normal parameter mode. Seven instructions can be microprogrammed on this basic display operate instruction, whose first five bits are 0.

When bit 0 and/or bit 1 is a 1, then the 13 least-significant bits are interpreted as an address, and the two bits are decoded to determine how this address will be used. If they are 01, the display interprets the instruction as a display deposit save register (DDS), and loads the address into the SR. If they are 10, the display interprets the instruction as a display jump (DJP) and loads the address into the DAR. If they are 11, the display interprets the instruction as a display jump and save (DJS) and loads the address into the DAR after transferring the address that was in the DAR into the DSR.

Bits 0 and 1 are decoded by the inverters in the lower right of Figure 4-14 (BS-D-340-5-14), according to the Kaunaugh map on the bottom of the drawing. Bit BBR0 is applied to two inverters in 1B16, and bit BBR1 is applied to an inverter in 1B17 and to another inverter in 1B16. The outputs of two of these inverters are ORed together by sharing a common clamped load resistor, producing the OPERATE signal. This is -3 volts as long as both bits are 0. However, if either or both BBR0 and BBR1 become a 1, the OPERATE signal goes to ground. This is complemented by another inverter in 1B16 to produce the -3 volt $\overline{\text{OPERATE}}$ signal.

The OPERATE signal is also applied to two other inverters, each of which is cut off when either or both bits are a 1. The output of each of these inverters is ORed with the output of one or

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request for data signal. When the delay stops operating, the data request is produced and the 4604 Pulse Amplifier in 1B12 is triggered. This produces the DSR⟶DAC pulse which transfers the address saved in the DSR to the DAC.

The DSR⟶DAC pulse is a negative 400-nanosecond pulse. When it returns to ground, it triggers a 4606 Pulse Amplifier in 1B03 which produces the DELAYED DSR⟶DAC pulse. This is applied to the pulse inputs of the two capacitor-diode gates at the upper left corner of Figure 4-14. One gate is permanently enabled and produces a positive pulse that clears the escape skip flip-flop. The other gate is enabled by the flip-flop and produces a positive pulse that triggers the incrementing pulse amplifier, producing the second + 1⟶DAC pulse.

When both the stop bit (BR7) and the skip bit (BR9) are set, the display stops operating until the resume IOT occurs, at which time the DAC is incremented so that the display skips the next instruction when it finishes its interrupted operation. The resume skip flip-flop stores the skip requirement until the RESUME pulse occurs. This flip-flop is set by a positive pulse from the 4115 NAND gate beneath it in the upper left of Figure 4-14. This gate is activated by the PMP pulse when it is enabled by the BR7(1) and BR9(1) levels.

As long as the resume skip flip-flop is set it enables the capacitor-diode gate in 1B04 above it. The RESUME pulse (shown as DRS) activates both capacitor-diode gates when it occurs, clearing the flip-flop and triggering the incrementing pulse amplifier.

In order to prevent more than one interrupt from occurring when the display stops and generates a stop program interrupt request, the one interrupt flip-flop is set at the same time as the stop flip-flop. This is accomplished by the 4115 NAND gate in 1B06 located below the flip-flop in the top left of Figure 4-14. The stop bit (BR7) and the interrupt on stop bit (BR8) enable the gate, allowing the PMP pulse to produce a ground output that sets the flip-flop. This causes a ground level to be applied to the 4102 Inverter in 1B07, whose collector is in parallel with the two inverters in 1F06, shown in the upper right of Figure 4-15 (BS-E-340-5-18). As long as all three inverters are cut off, a -3 volt STOP INTER program interrupt request is produced. When the PDP-4 executes the IOT skip on stop and interrupt, 700601, the program counter is incremented and a pulse is produced by the IOT decoder. This pulse, IOT 0601, is applied to the pulse input of a capacitor-diode gate in 1B21, shown at the top of Figure 4-14. Since this

gate is enabled by the -3 volt level from the inverter, it produces a positive pulse that clears the one interrupt flip-flop. This turns on the inverter in 1B07 and removes the STOP INTER signal even though the buffer register and stop flip-flops have not yet been cleared.

Special Controls

The four 4218 Flip-Flops in 1B20, shown at the center of Figure 4-14 (BS-E-340-5-14) compose the special control flip-flops in this display. Three of these flip-flops are set or cleared by the IOT display load address save register, 702603, according to AC bits 0, 1, and 2.

The temporary dark flip-flop is cleared by the PMP pulse in any control mode instruction if the intensify bit (BR14) is set or if BR14 is not set when BR17 is set. The IOT resume, 700524, also clears this flip-flop since MB13 is set. When BR14 is not set and BR16 is set, the PMP pulse sets the flip-flop, as will the IOT resume, 700544, since MB12 is set. The buffered output of the temporary dark flip-flop prevents the INT pulse from being produced when the flip-flop is set.

The temporary blind flip-flop is set by the DLS IOT with AC2 a 1, by the PMP pulse in a control mode instruction if BR5 is set, and by the SAVE PMP pulse when the display escapes from the vector, vector continue, or increment mode or from a subroutine. When the flip-flop is set, it disables the LP find gate, preventing the LP flag from being set when the light pen sees a spot. The temporary blind flip-flop is cleared by the DLS IOT with AC2 a 0, by a control mode instruction with bit 5 cleared (this gate is not shown), or when the save flip-flop is cleared (except as a result of a DDS IOT).

The direction flip-flop controls the source of the address read into the 133 Data Interrupt Multiplexer. See Figure 4-22 (BS-D-4C-24-11). When it is cleared, it enables the DAC gates; and when it is set, it enables the BR gates. The DLS IOT sets it when AC2 is a 1 and clears it when AC2 is a 0. The flip-flop also cleared by the IOT display load address counter, 700604, and by the DELAYED ADDRESS⟶ MA pulse. This pulse is obtained from the 4301 located in 2L01 in the PDP-4 (shown at the lower left side of Figure 4-14), 3 microseconds after the DATA ADD⟶ MA pulse occurs.

The save flip-flop is set by the IOT display load save register (DLS, 702603) if AC0 is a 1, and by the DAC ⟶ DSR pulse. When AC0 is a 0, the DLS IOT clears the flip-flop, as do the IOT display load address register, 700606, and the DSR ⟶ DAC pulses.

SECTION 4

ENGINEERING DRAWINGS

This section consists wholly of reduced copies of the pertinent block schematics for this system. Each drawing is identified by a figure number for easy reference in Section 3, a name, and the DEC drawing number. If difficulty is experienced in reading any of these drawings, obtain the full-sized drawing from Digital Equipment Corporation. Be sure to specify the drawing by its number.

These engineering drawings use Digital's drawing symbology. Refer to the 340 and PDP-4 Maintenance Manuals for an explanation of these symbols. To understand the function of any module circuit, refer to the System Modules Catalog, C-100.

TABLE 4-1 ENGINEERING DRAWINGS

Figure	Title	DEC Number
4-1	Type 133 Control and Output Driver	BS-D-133-0-2
4-2	Type 125 Real Time Control	BS-D-4C-24-16
4-3	Type 133 Information Collectors	BS-D-133-0-1
4-4	Type 140 Relay Buffer	BS-D-24903
4-5	Type 140 Control Register	BS-D-4C-24-8
4-6	Interface Control	BS-E-4C-24-2
4-7	Information Collector 1	BS-D-4C-24-14
4-8	Information Collector 2	BS-D-340-5-10
4-9	Switches and Switch Filters	BS-E-340-5-9
4-10	IOT and MB Decoding	BS-D-340-5-16
4-11	Horizontal and Vertical Deflection Registers	BS-E-340-5-19
4-12	Binary Rate Multiplier and Increment Logic	BS-E-340-5-20
4-13	Buffer Register and Parameter Registers	BS-D-340-5-22
4-14	Subroutine Timing Control	BS-E-340-5-14
4-15	Timing and Pulse Control Logic	BS-E-340-5-18

TABLE 4-1 ENGINEERING DRAWINGS (continued)

Figure	Title	DEC Number
4-16	Light Driver Registers	BS-E-340-5-13
4-17	Knob and Track Ball Counters	BS-E-340-5-8
4-18	Interface Address Register	BS-D-4C-24-3
4-19	Interface Input Register and Logic	BS-D-4C-24-4
4-20	Address and Save Registers	BS-D-4C-24-9
4-21	Device Selector IOT Decoding	BS-D-4C-24-15
4-22	DDS Instruction Implementation	BS-D-4C-24-11
4-23	Type 340 Deflection Circuitry	BS-D-340-5-21

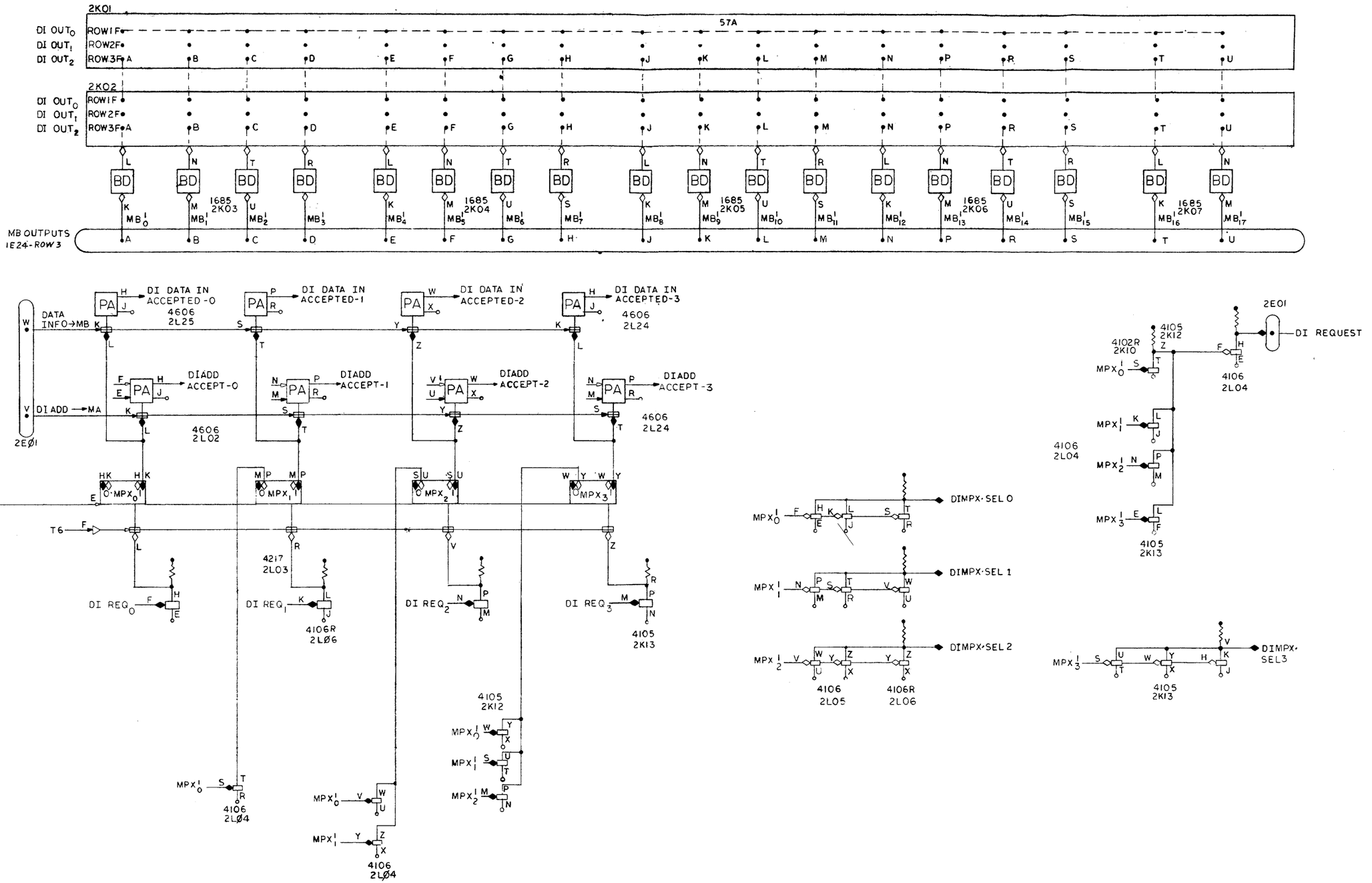


Figure 4-1 Type 133 Control and Output Driver

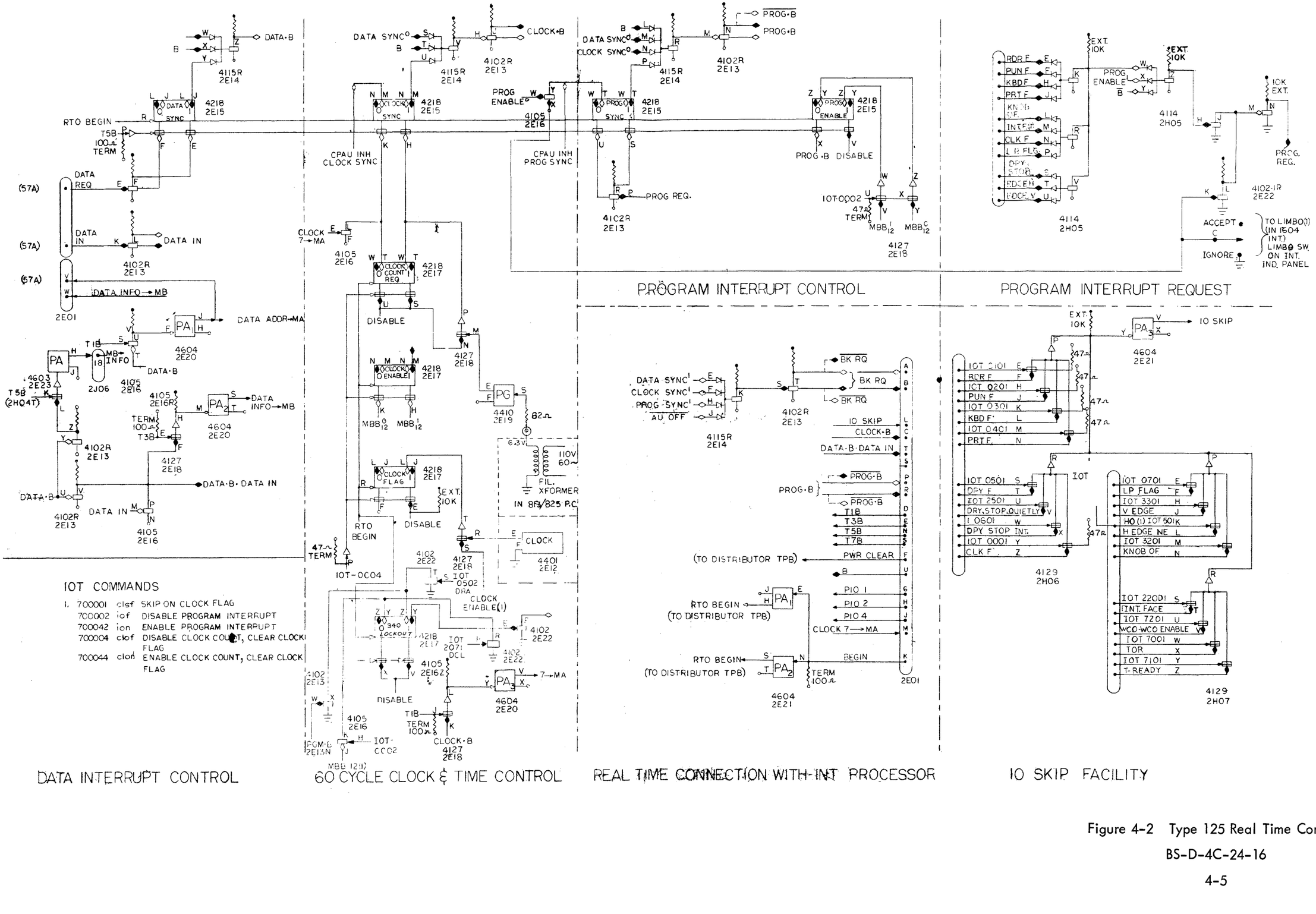


Figure 4-2 Type 125 Real Time Control

BS-D-4C-24-16

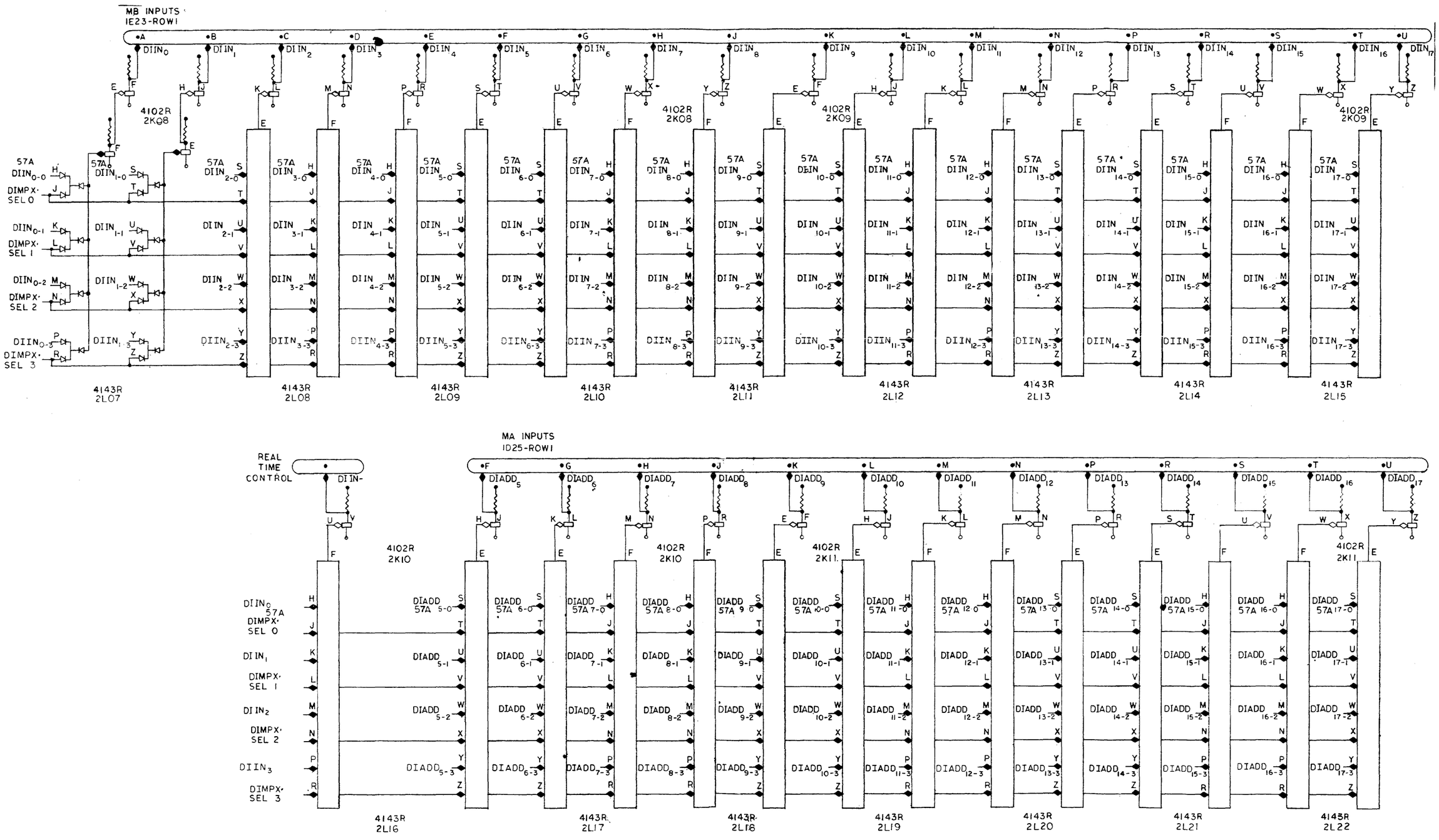


Figure 4-3 Type 133 Information Collectors

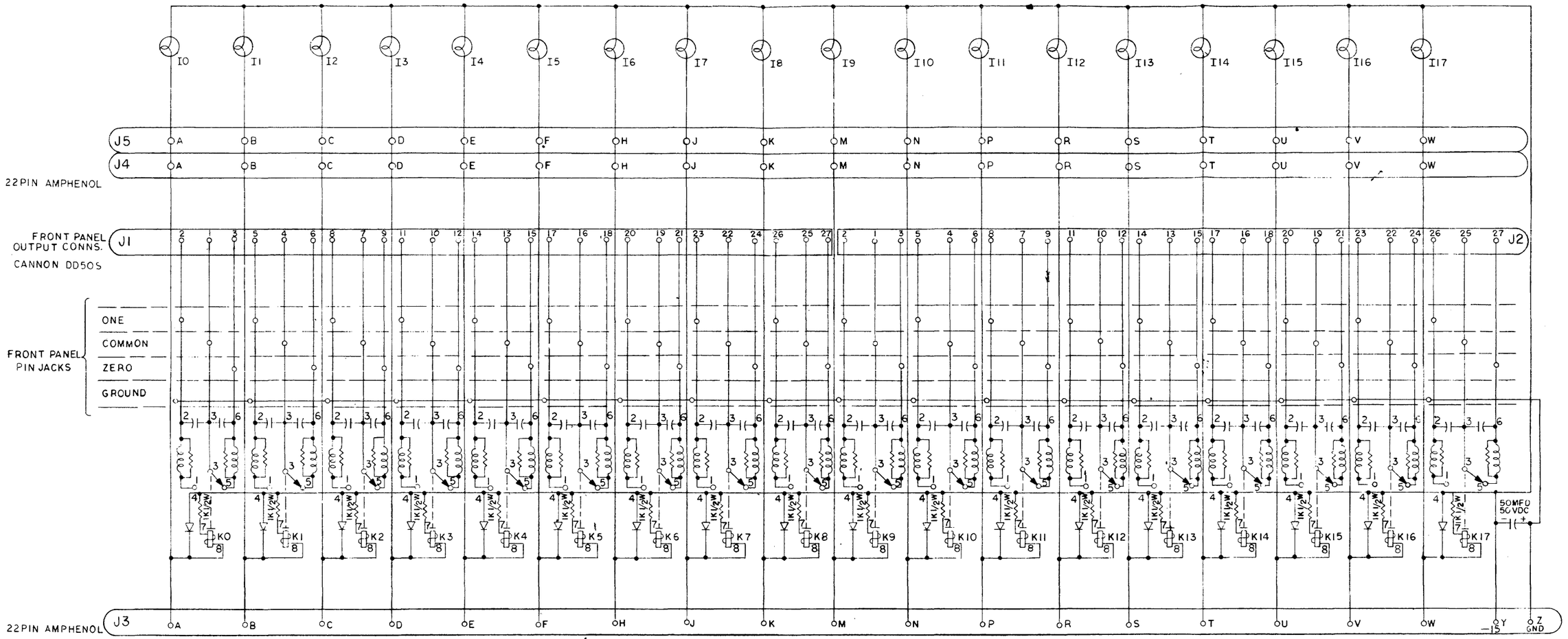
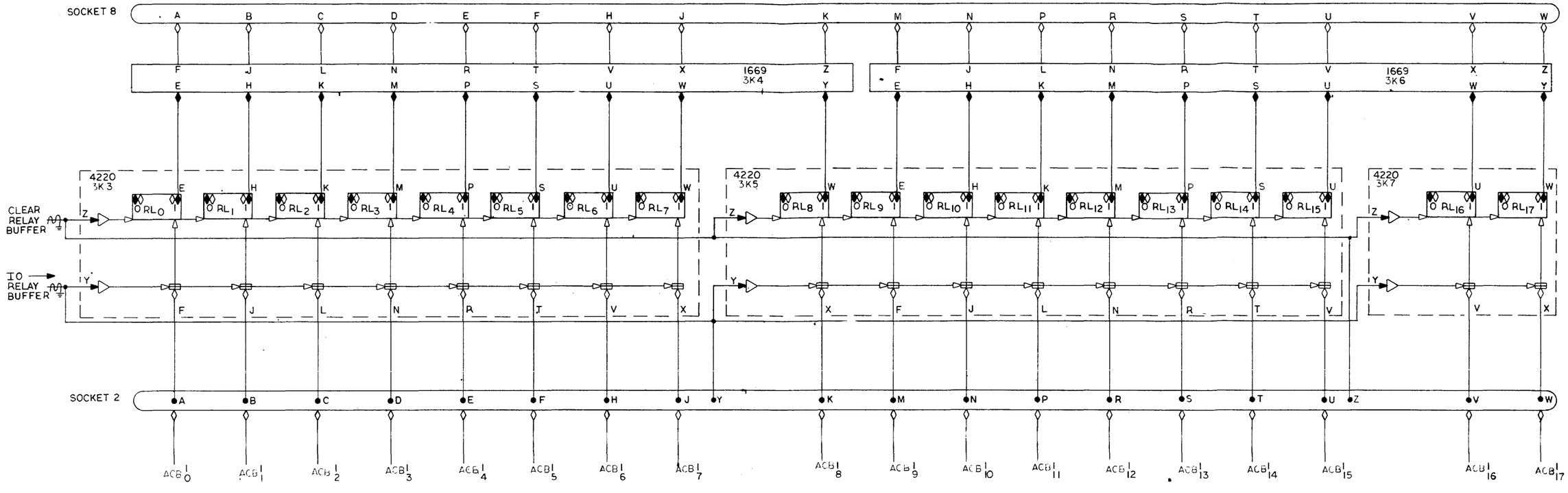


Figure 4-4 Type 140 Relay Buffer

BS-D-24903



NOTES.

1. ALL 4220'S SHOULD HAVE OUTPUTS JUMPED TO THE "ONE" SIDE.

Figure 4-5 Type 140 Control Register

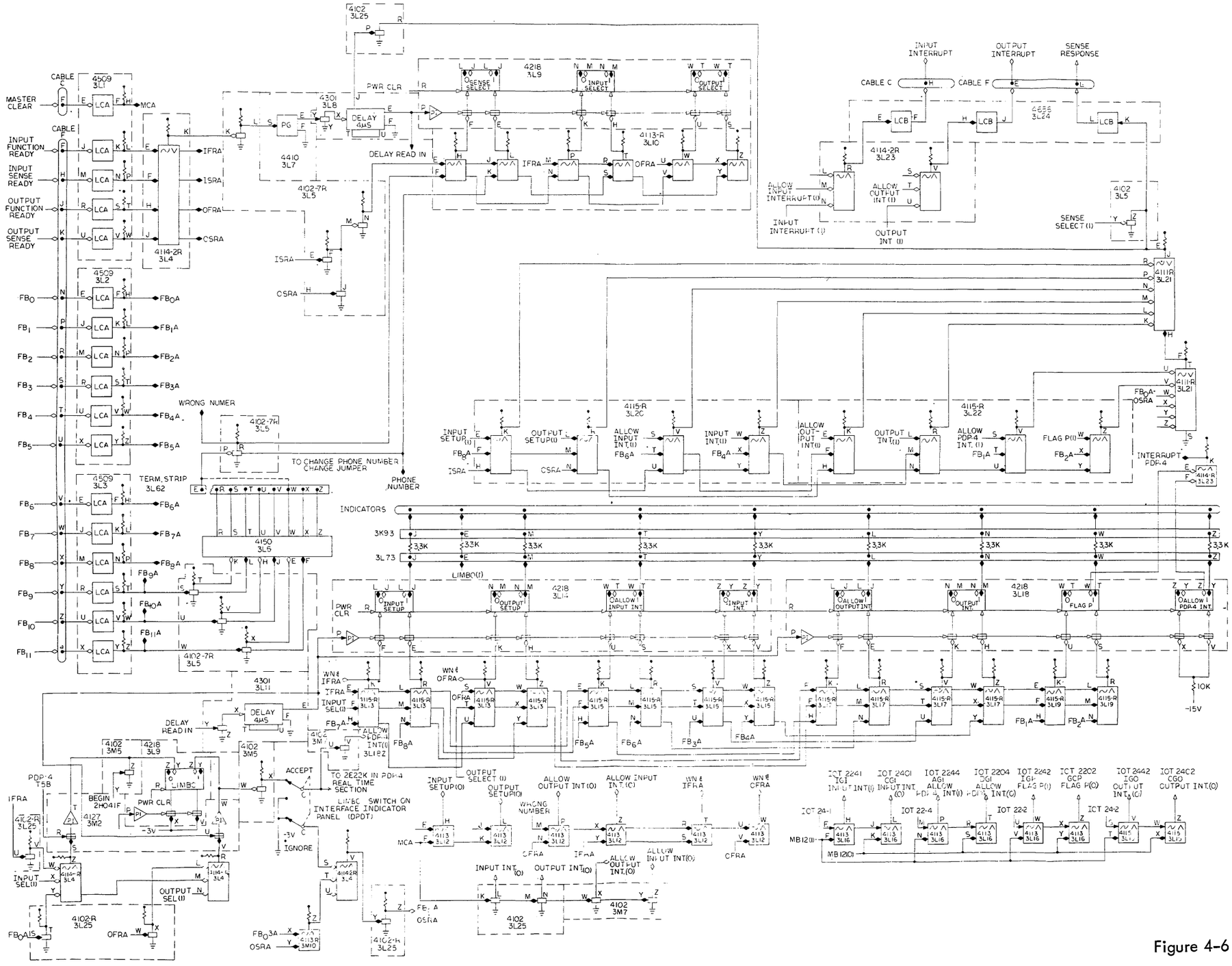


Figure 4-6 Interface Control

BS-E-4C-24-2

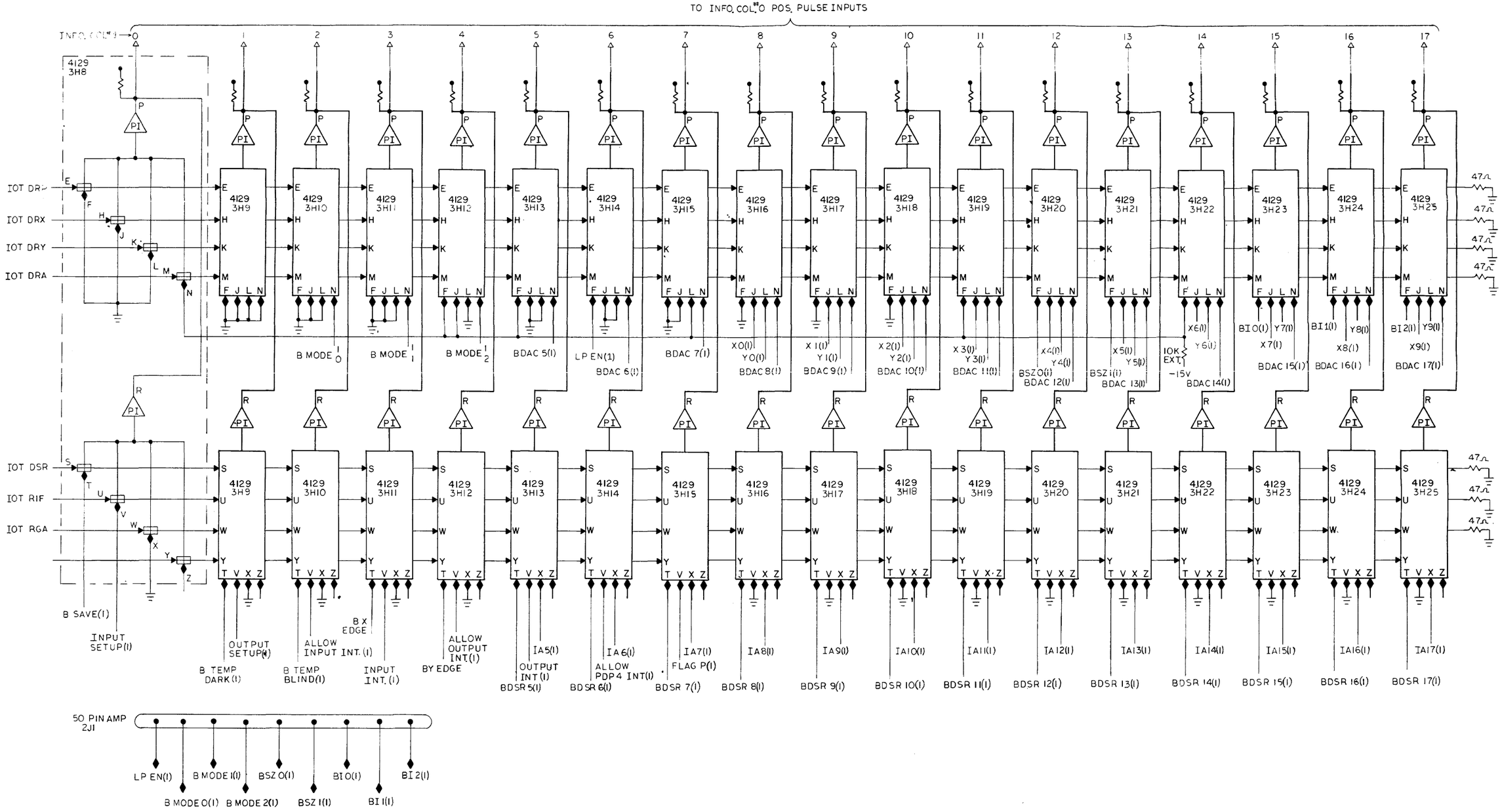


Figure 4-7 Information Collector 1

BS-D-4C-24-14

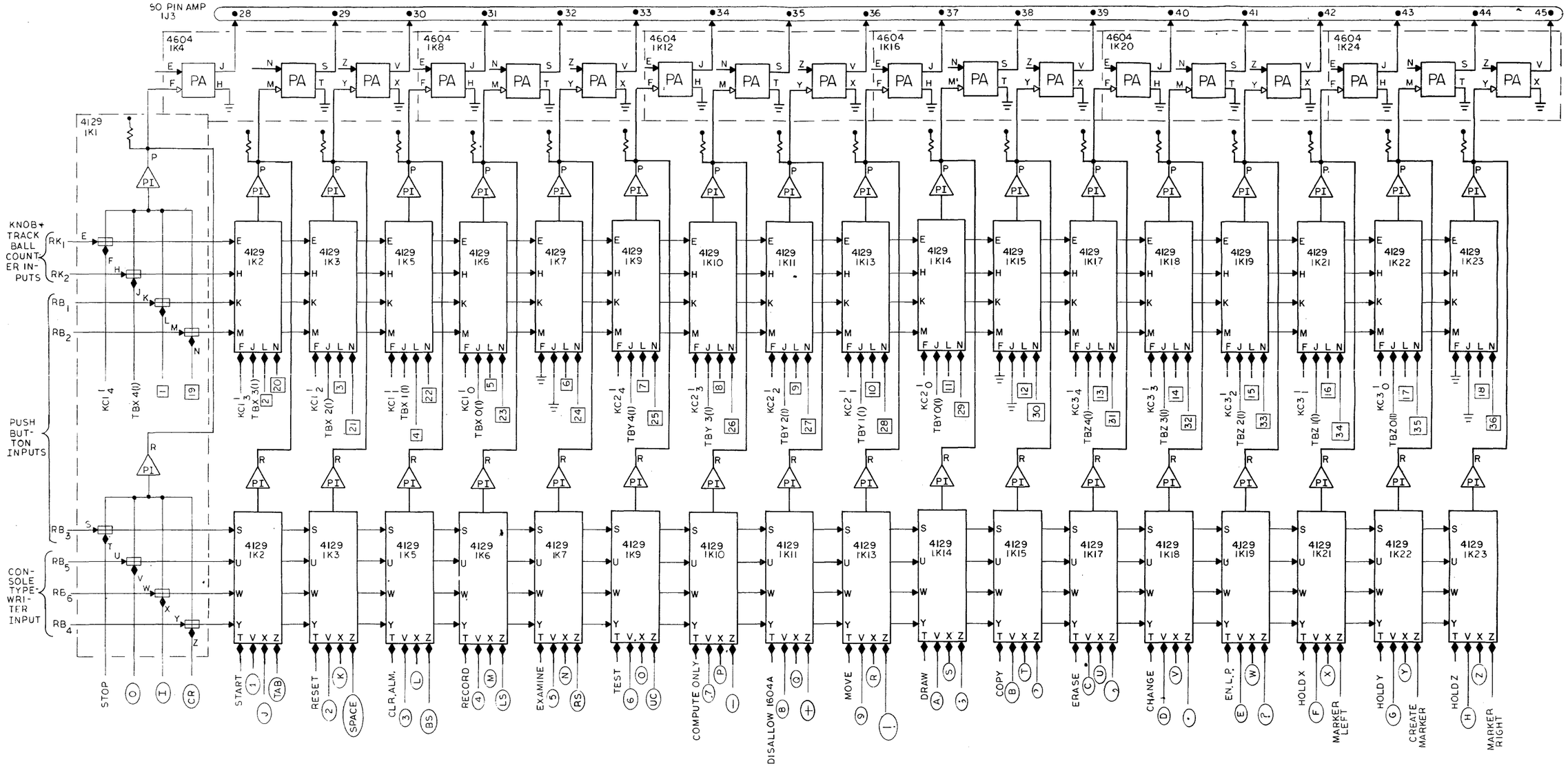


Figure 4-8 Information Collector 2

BS-D-340-5-10

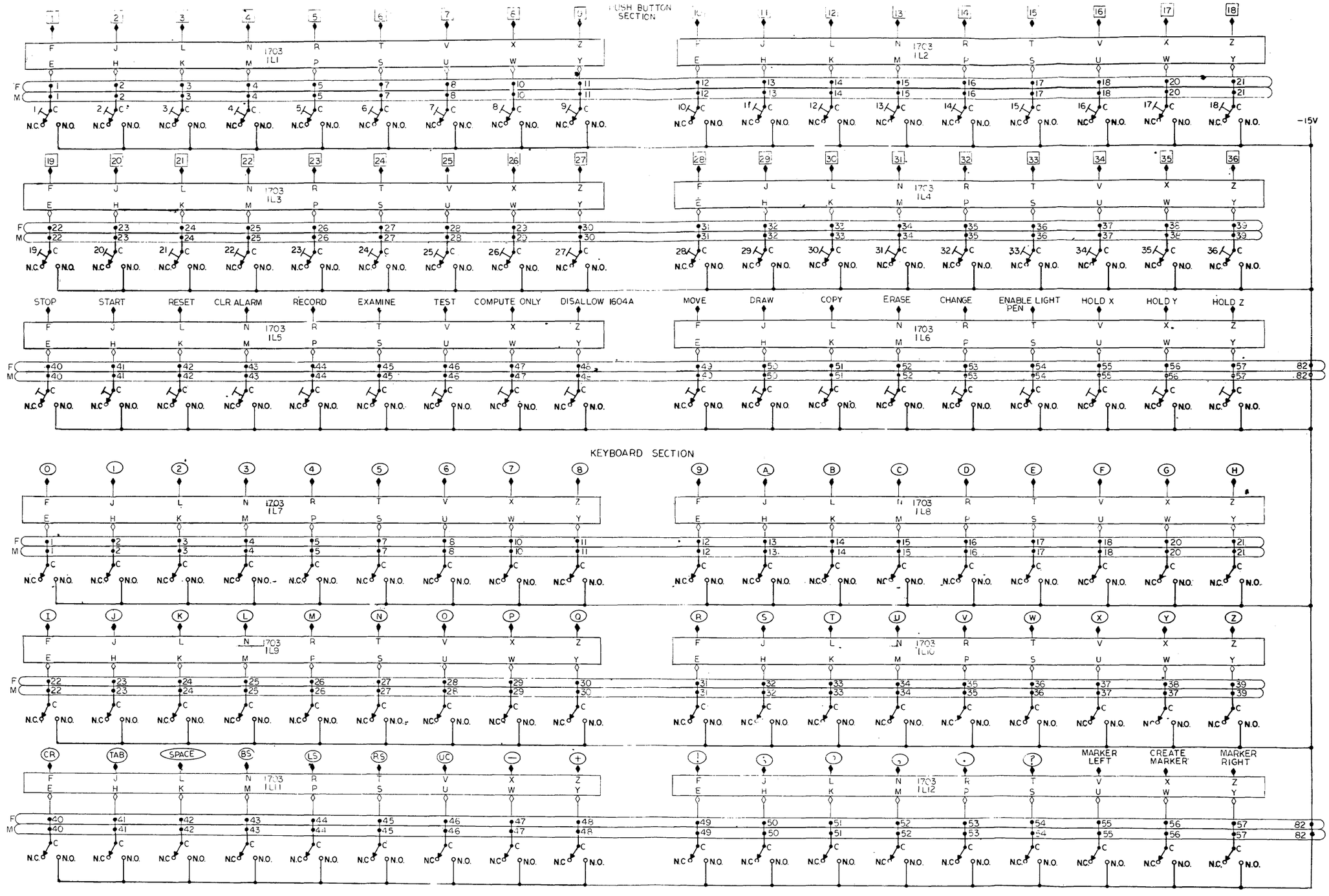
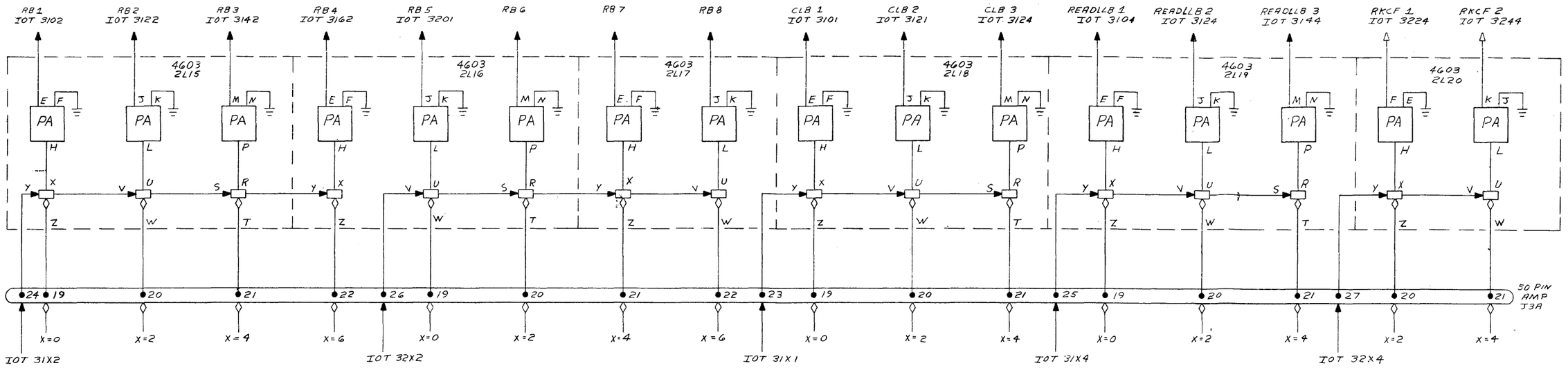
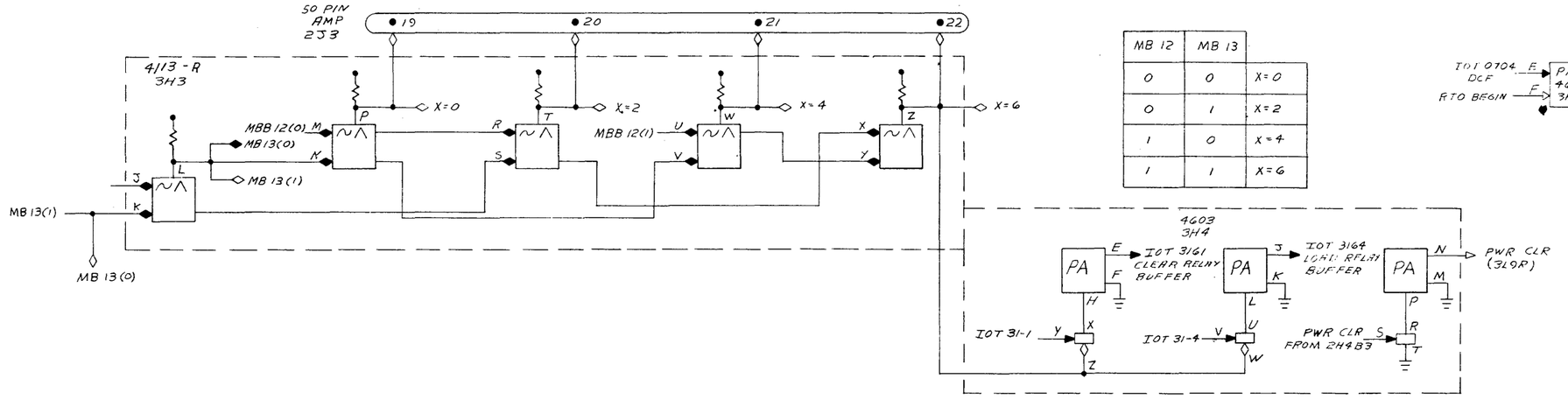


Figure 4-9 Switches and Switch Filters





MB 12	MB 13	
0	0	X=0
0	1	X=2
1	0	X=4
1	1	X=6

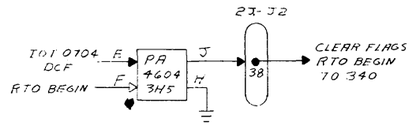


Figure 4-10 IOT and MB Decoding

BS-D-340-5-16

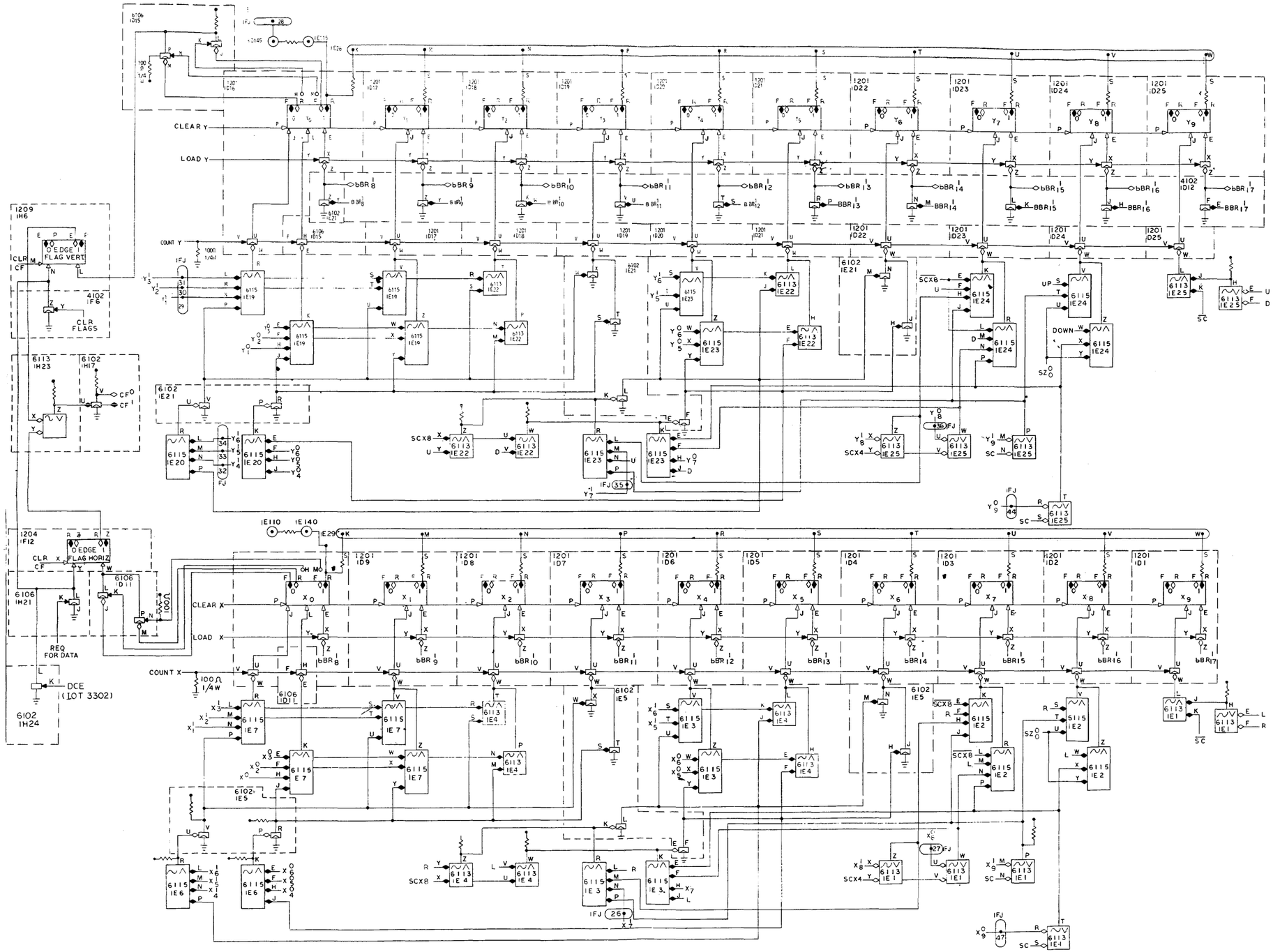


Figure 4-11 Horizontal and Vertical Deflection Registers

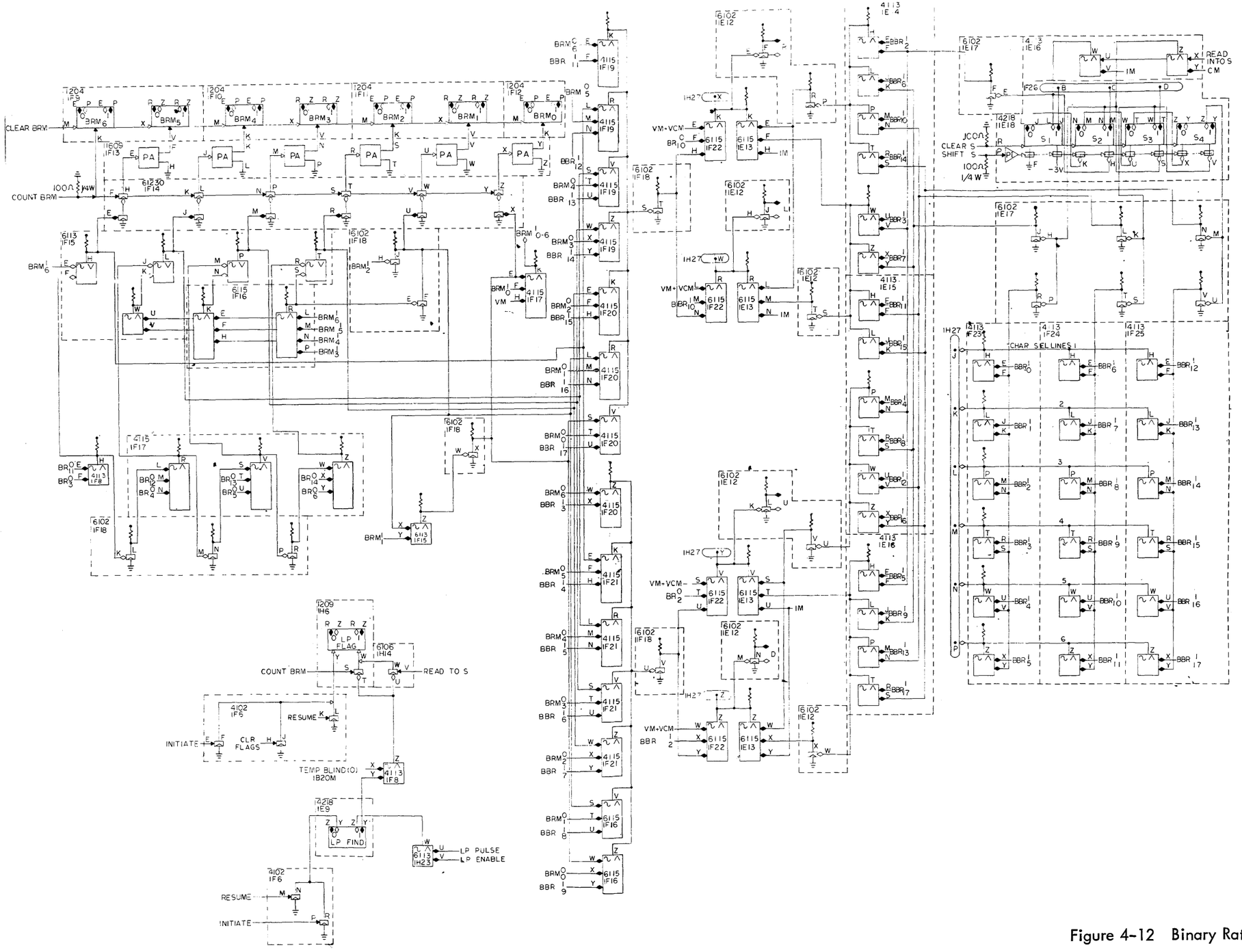


Figure 4-12 Binary Rate Multiplier and Increment Logic

BS-E-340-5-20

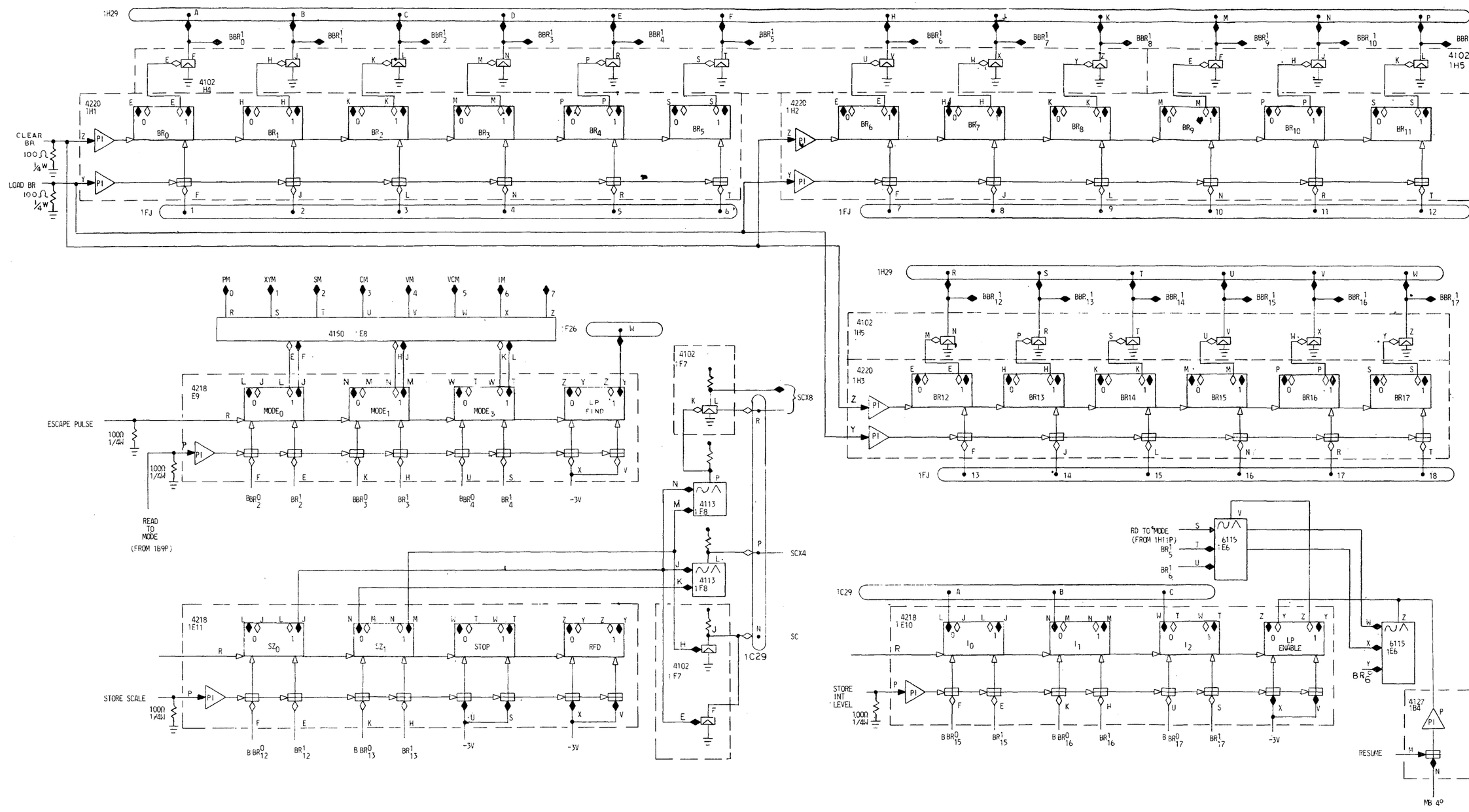


Figure 4-13 Buffer Register and Parameter Registers

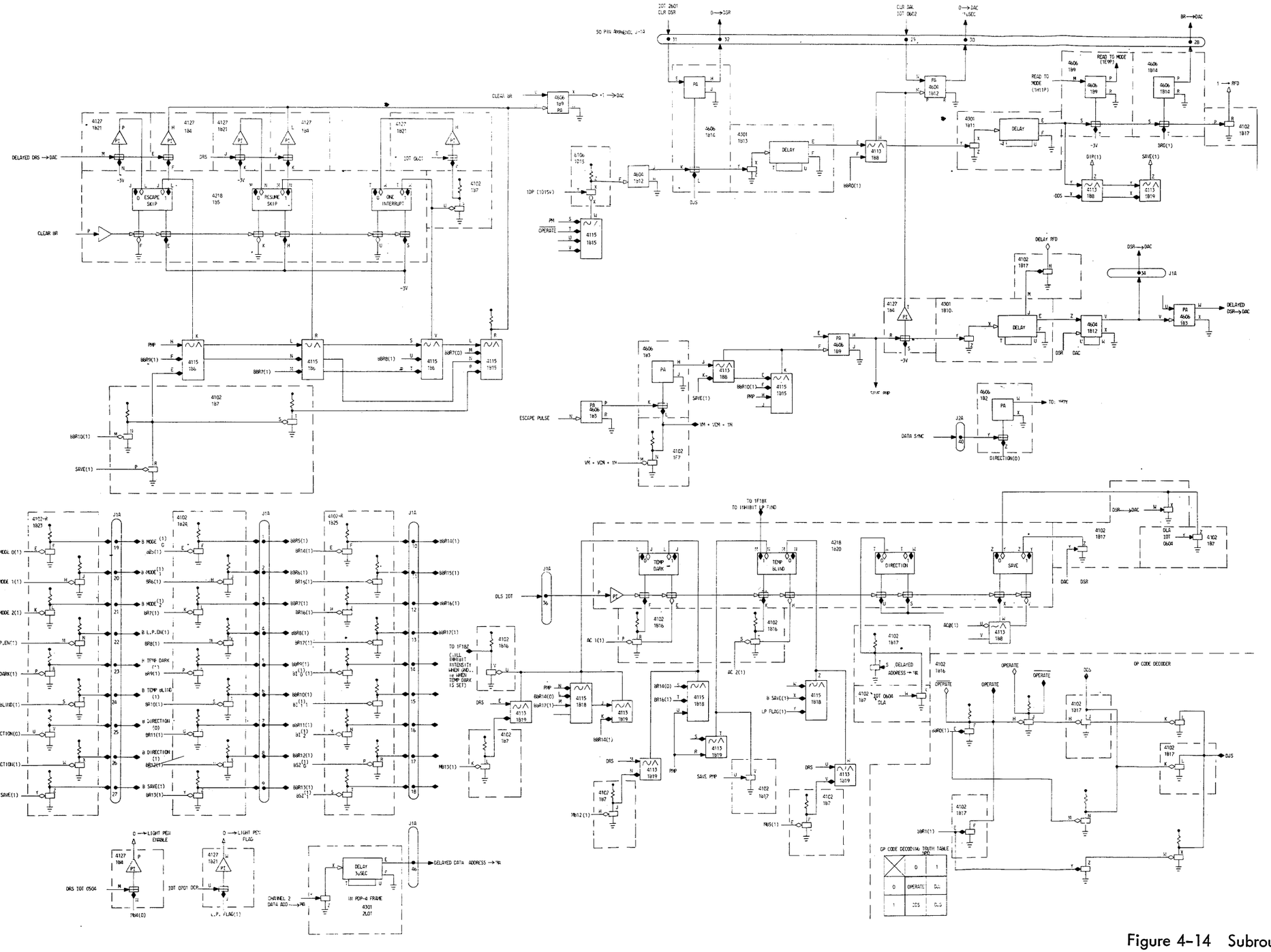


Figure 4-14 Subroutine Timing Control

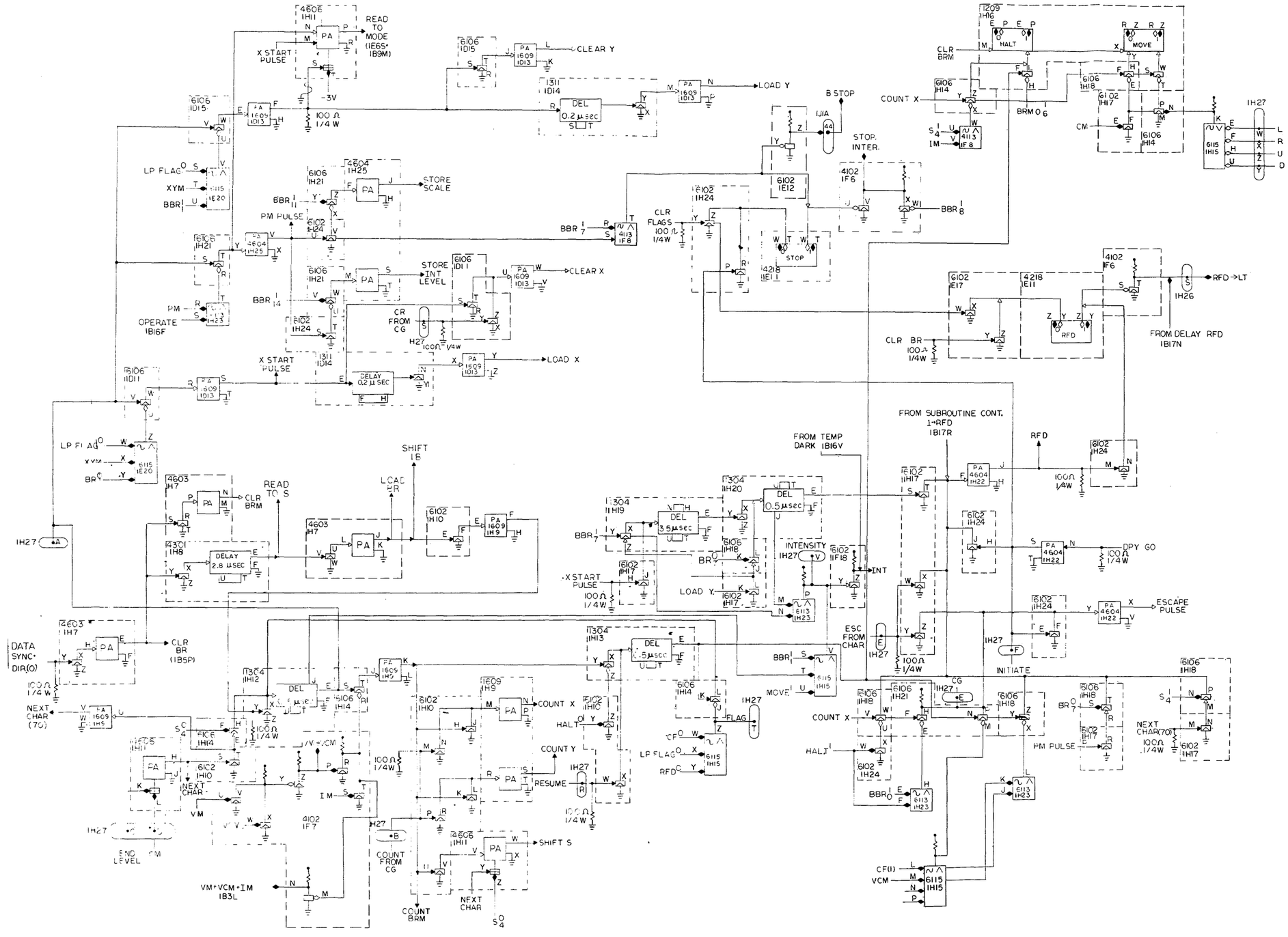


Figure 4-15 Timing and Pulse Control Logic

BS-E-340-5-18

Figure 4-16 Light Driver Registers

BS-E-340-5-13

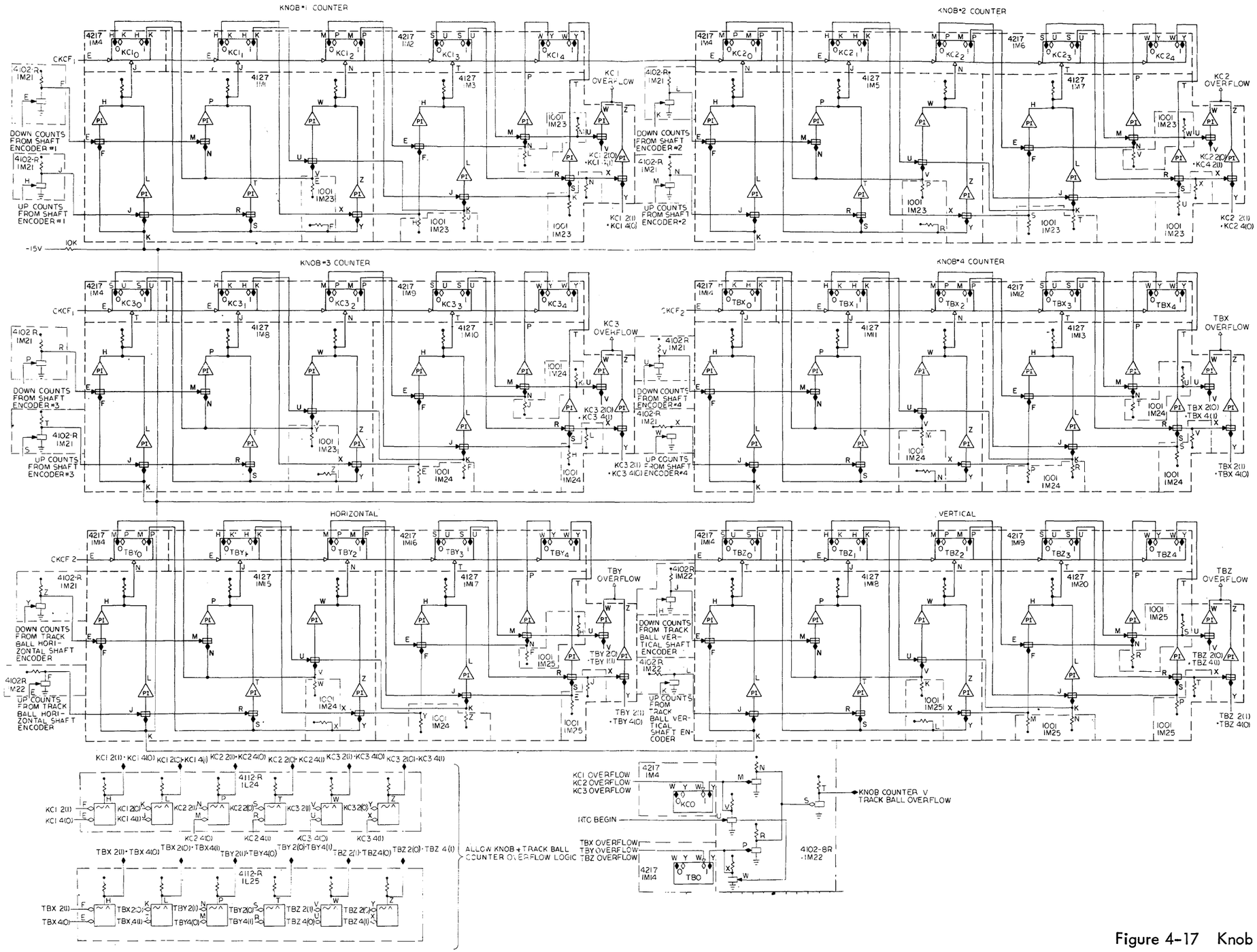


Figure 4-17 Knob and Track Ball Counters

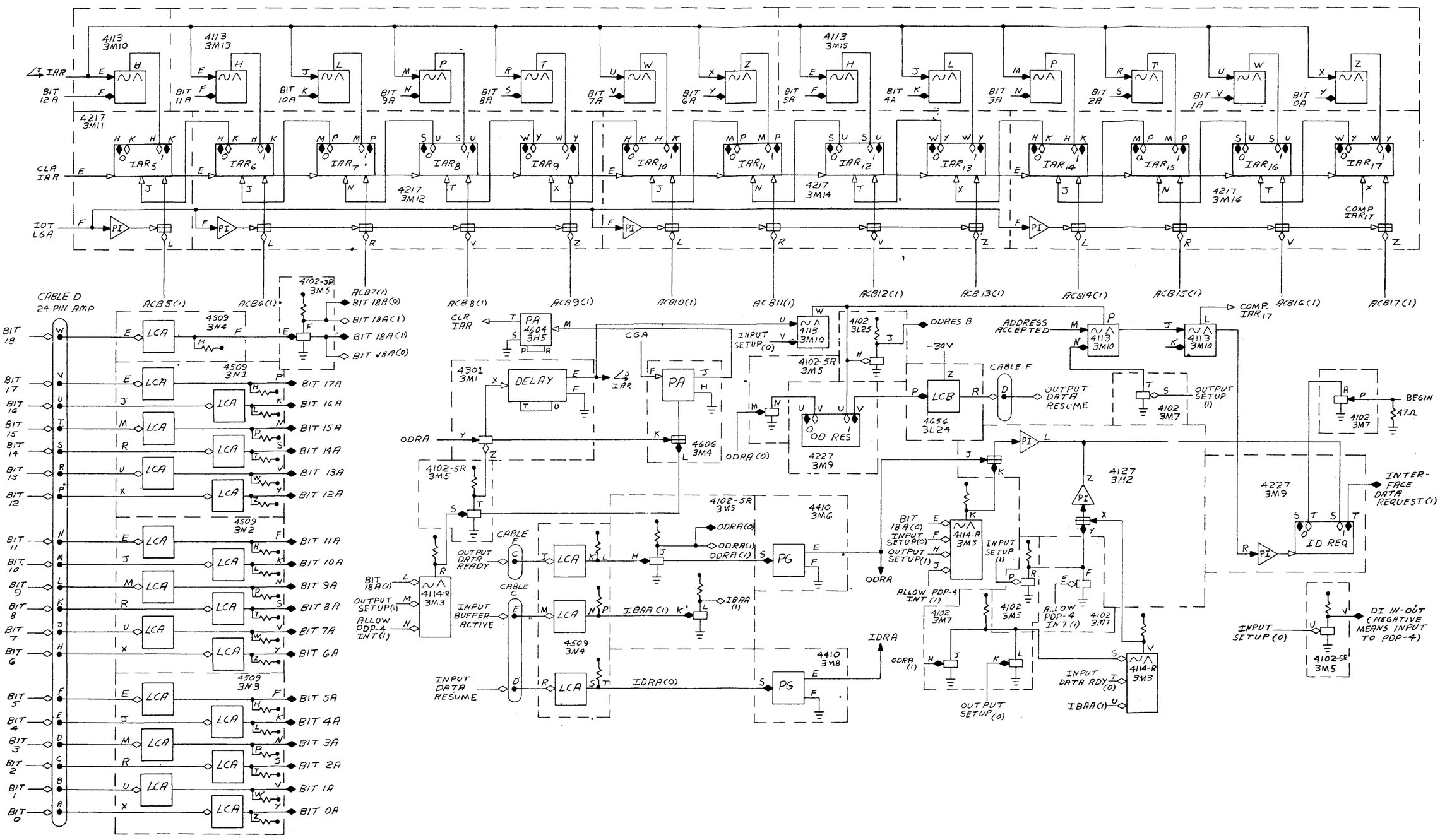
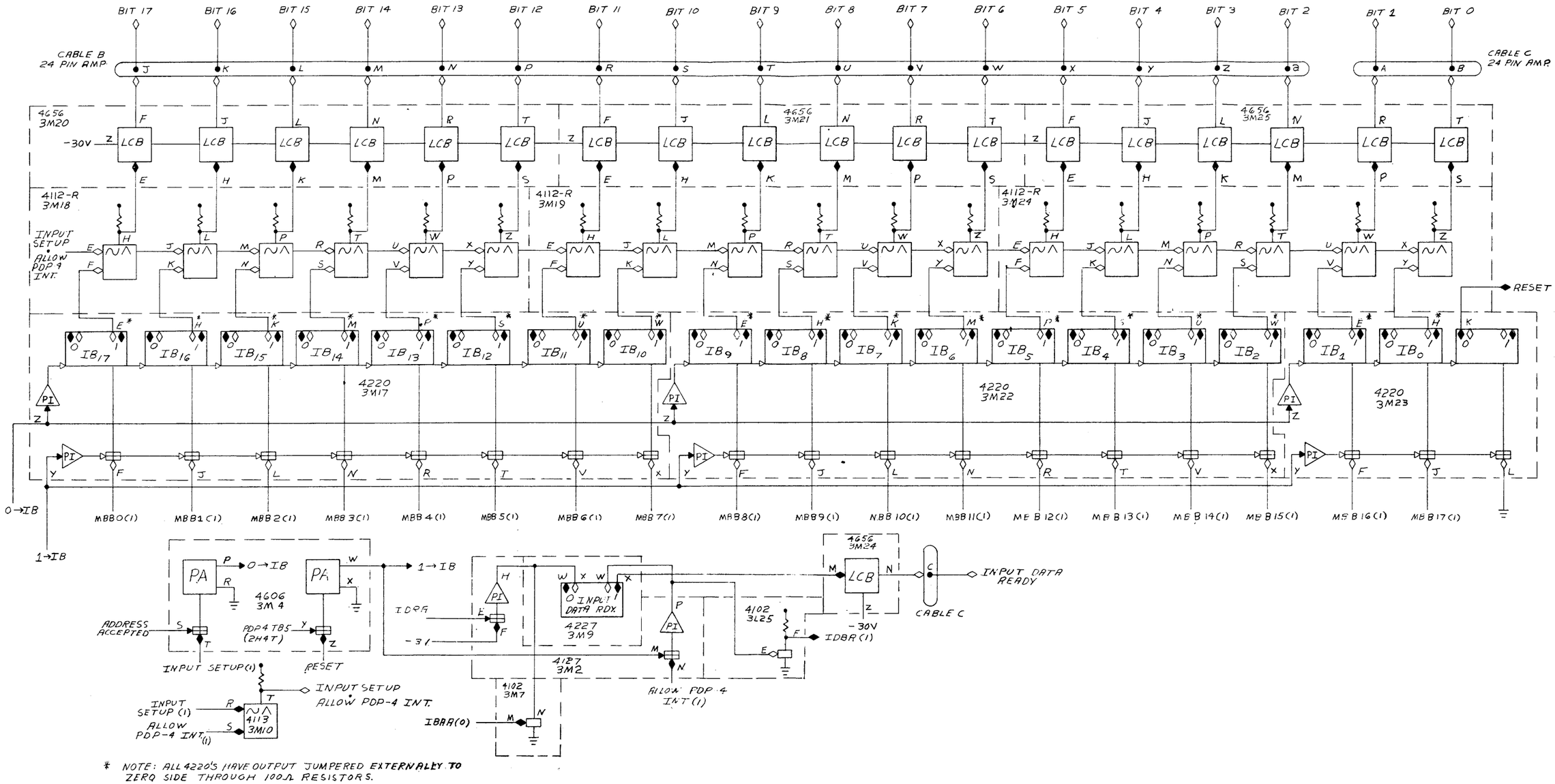


Figure 4-18 Interface Address Register

BS-D-4C-24-3



* NOTE: ALL 4220'S HAVE OUTPUT JUMPERED EXTERNALLY TO ZERO SIDE THROUGH 100Ω RESISTORS.

Figure 4-19 Interface Input Register and Logic

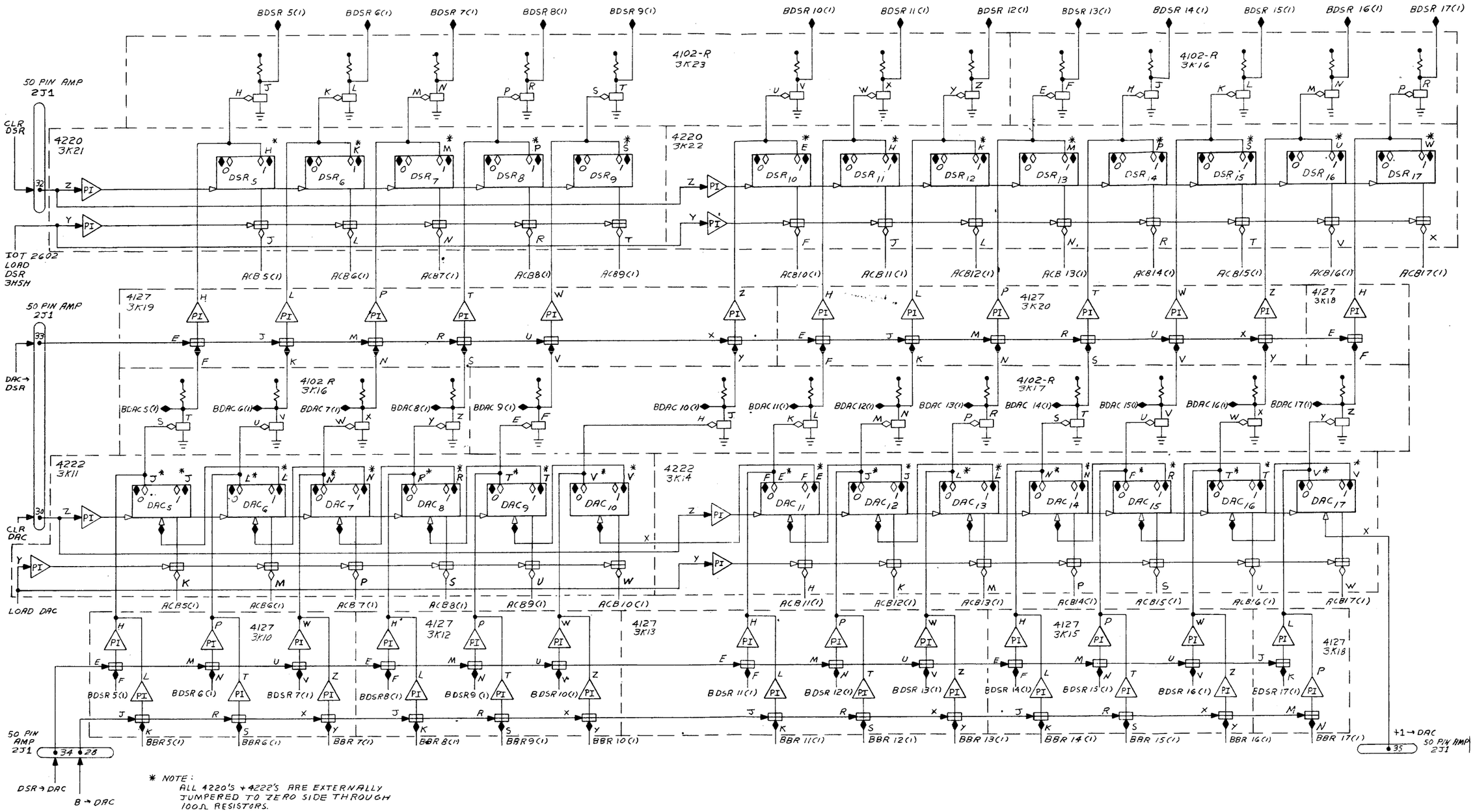


Figure 4-20 Address and Save Registers

BS-D-4C-24-9

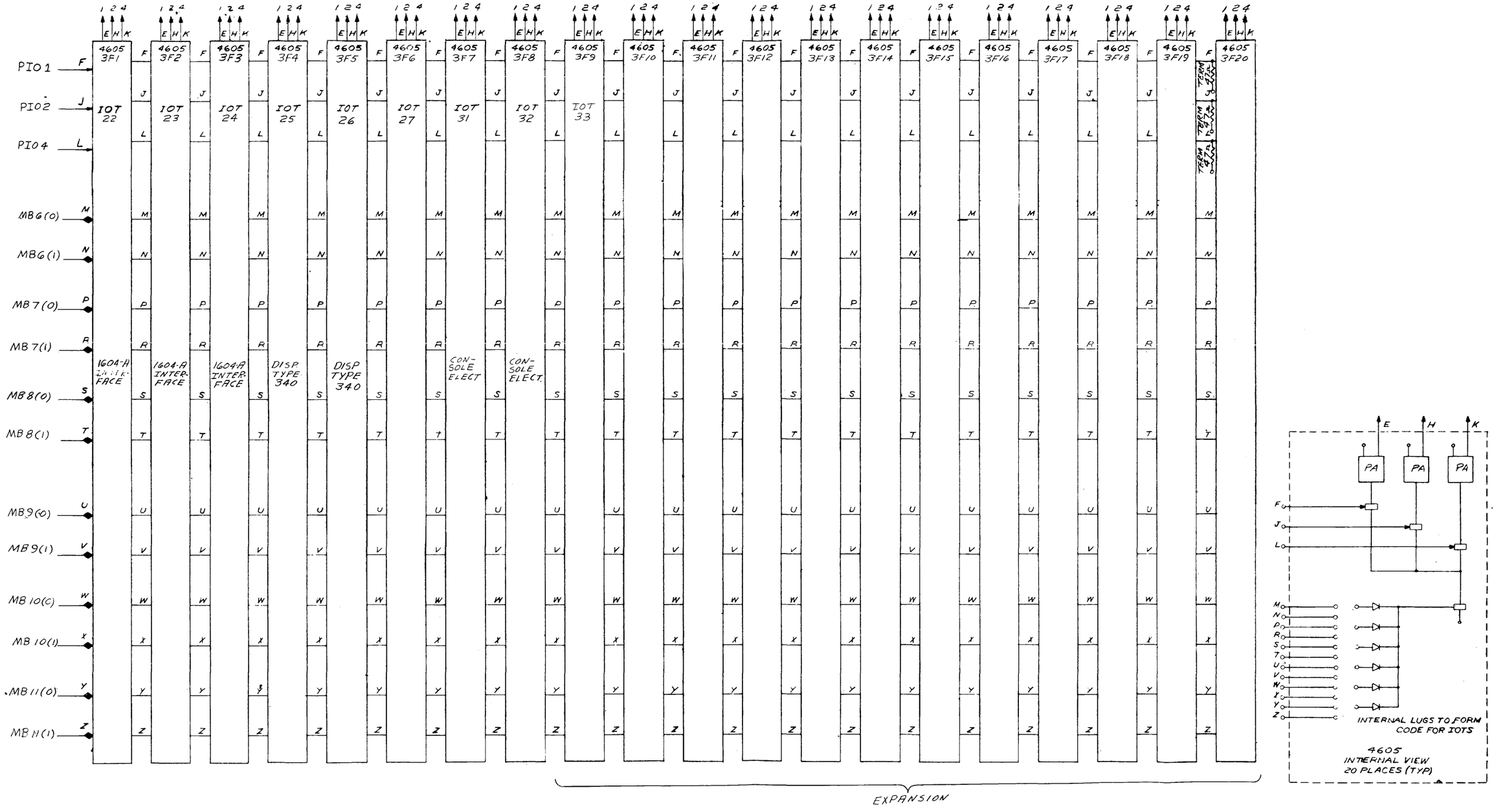


Figure 4-21 Device Selector IOT Decoding

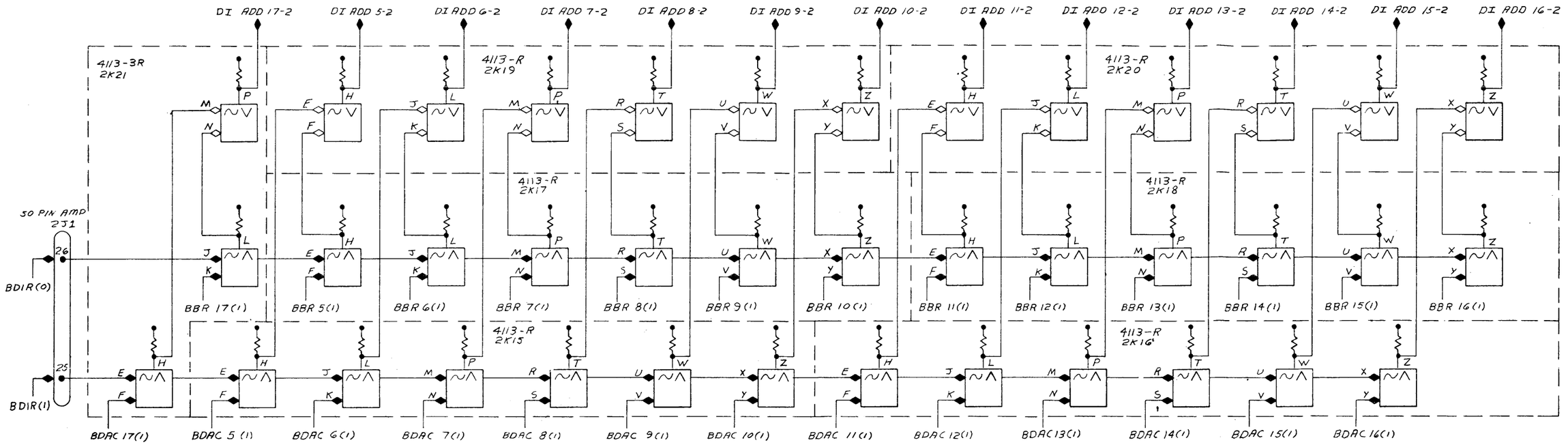


Figure 4-22 DDS Instruction Implementation