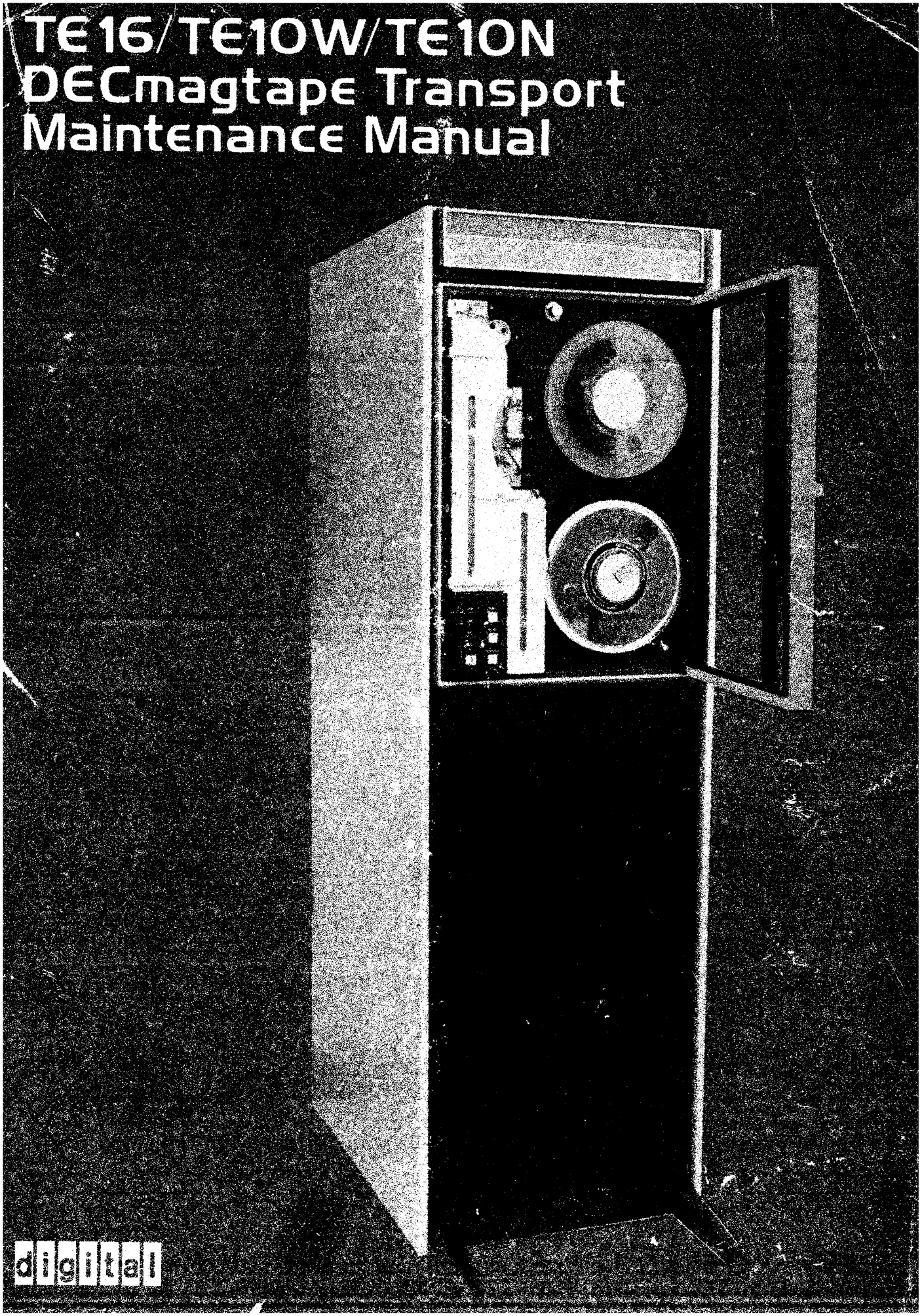
TE16/TE10W/TE10N DECmagtape Transport Maintenance Manual



digital

TE16/TE10W/TE10N
DECmagtape
Technical Manual

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PREFACE

This manual is formatted to aid the user in quickly locating information at the level desired. To accomplish this, the manual is divided into six chapters:

Chapter 1 – Introduction: This chapter contains general information, such as basic and functional descriptions, specifications, and a list of related documents.

Chapter 2 – Installation: This chapter provides complete installation information. Because the TE16 can be used with many different processor-controller/formatter combinations, cabling diagrams for all such systems are provided. In addition, unpacking and inspection instructions and acceptance test procedures are included.

Chapter 3 – Operating Instructions: This chapter is directed toward the operator/user, so that the reader will have a complete understanding of how to power up, load/unload tape, and apply basic troubleshooting techniques. No programming information is provided, as it appears in the respective controller/formatter manuals.

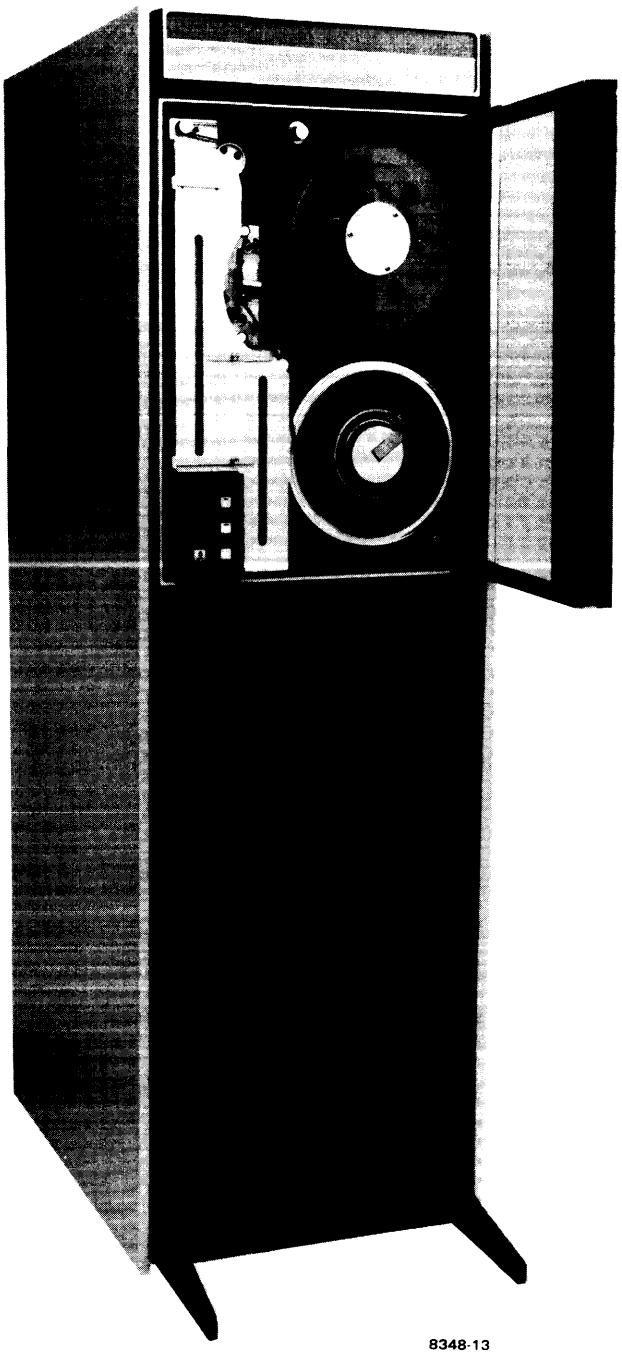
Chapter 4 – Customer Care and Preventive Maintenance: This chapter lists customer responsibilities, magnetic tape care fundamentals, and customer preventive maintenance procedures.

Chapter 5 – Theory of Operation: This chapter provides three levels of theory for a total TE16 description. First, a basic description of the TE16 is discussed. Then, a functional overview is presented, providing a "big picture" of the TE16. Diagrams complement the text, taking the reader through entire operations from the application of power through tape buffering, power supply operation, and the read/write action.

Then, a unit level discussion of each TE16 module is presented. The discussion identifies functional components of each circuit schematic in the print set. The reader will be able to use these descriptions with the function overview section to gain an overall understanding of TE16 operation. Also presented here are descriptions of the M8926 and M8927 interface modules. Use of these modules allows the TE16 to function in many system configurations. When used with one of these interface modules, the TE16 option designation changes. With an M8926, the TE16 becomes a TE10W master; with an M8927, it becomes a TE10N.

Detailed explanations of PE and NRZI read and write circuitry operation complete this chapter.

Chapter 6 – Servicing: This chapter provides complete servicing information. Included are test equipment requirements, preventive maintenance procedures adjustment and alignment procedures, removal and replacement procedures, and corrective maintenance procedures.



TE16/TE10W/TE10N DECmagtape System

CHAPTER 1
INTRODUCTION

1.1 GENERAL INFORMATION

The TE16 is an industry-compatible 7- or 9-track tape transport capable of reading and writing on 1.27 cm (1/2 in) magnetic tape at 1600 char/in (PE) and 800, 556, and 200 char/in (NRZI). Tape density and tape character format are program selectable. Forward/reverse tape speed is 1.14 m/s (45 in/s), while rewind is performed at 3.8 m/s (150 in/s). The transport consists of a tape deck with associated reel and capstan motors, H607 motor driver module, transformer and capacitor assembly, a logic box that integrates the read/write electronics, the control electronics and the power supply regulator, and a vacuum system assembly. An off-line test function generator is included in the control package, which allows most maintenance procedures to be completed off-line.

1.1.1 Improvements Over TU16

Many differences between the TU16 and TE16 transports exist. Also, many improvements have been made. A summary of the differences/improvements is listed below:

1.1.1.1 Electronic Improvements

1. The G056 read amplifier is replaced by the G066, for increased reliability. All discrete transistors are replaced by integrated circuits. All amplitude adjustment potentiometers are at right angles to the module so that the module does not have to be extended for routine adjustments. The G066 is interchangeable with the G056.

2. The M8910 logic and write module is replaced by the M8916, which includes logic for an automatic load feature and a new LED style control box. The modules are not interchangeable.

3. The H606 power and servo module is replaced by the H607. The H607 is a "mother-daughter" assembly (hinged for access), which contains all of the original H606 circuitry plus dynamic reel motor braking and unload circuitry. This module is not interchangeable with the H606.

4. A hardware-activated, dual threshold feature during a PE read (forward or reverse) is added. During the preamble, the head amplifier threshold is automatically lowered, enabling the drive to read weak or damaged records that were previously unreadable.

5. The 5410451 voltage regulator module is replaced by a 5412242, increasing the +5 V current rating from 5 A to 8 A. These modules are interchangeable.

1.1.1.2 Mechanical Improvements

1. Improved fixed guide spacing relative to the tape head now follows the industry standard.

2. The spacing between the capstan and the upper fixed guide has been increased, making steering adjustments easier and less critical.

3. The fixed guides are now mounted directly to the deckplate casting rather than on the headplate, to maintain an accurate tape path. The headplate can distort when performing azimuth adjustments, thus throwing off fixed guide perpendicularity.

4. A third roller guide has been added between the existing upper left-hand roller guide and the take-up reel to aid in tape stacking.

5. The flange around the capstan motor has been eliminated, making capstan steering shim adjustments easier.

6. The upper take-up reel is fixed in place (no hub) and is constructed of a material that reduces warping.

7. The lower hub is a snap-lock type, which reduces service calls and makes the operator's job easier.

1.1.1.3 Electromechanical Improvements

1. The new control box is easier to operate than the previous control box. It features Hall-effect pushbuttons and LED indicators.

2. A semiautomatic tape loading feature is now provided. The operator must still manually thread the tape. However, once the tape is threaded, a single button is pushed and the tape automatically loads to BOT. If the operator has wound the tape past BOT, the drive times out and rewinds tape to BOT.

3. An automatic unload is accomplished when the tape is at BOT and OFFLINE. When the REW/UNLOAD switch is depressed, the panel tape unthreads automatically from the tape path and the drive stops.

4. The head contour has been changed from a relatively flat style to a sharper contour. The new head reads marginal or damaged tape much better than the previous head.

5. A switch panel, used for maintenance purposes, is mounted under the logic cage, as off-line forward and reverse capabilities are not possible with the new control box.

1.2 BASIC DESCRIPTION

The TE16 tape transport is contained in a single 48.3 cm (19 in) cabinet (H950), along with an 861 power control (Figure 1-1). Optionally, the TE16 may be mounted in an H9500 cabinet. The transport transfers digital data to and from magnetic tape, as commanded by the tape controller. The 861 power control controls power in the TE16 controller cabinet. Figures 1-2 and 1-3 illustrate front, rear, and side views of the transport and identify many of the TE16 components and subassemblies.

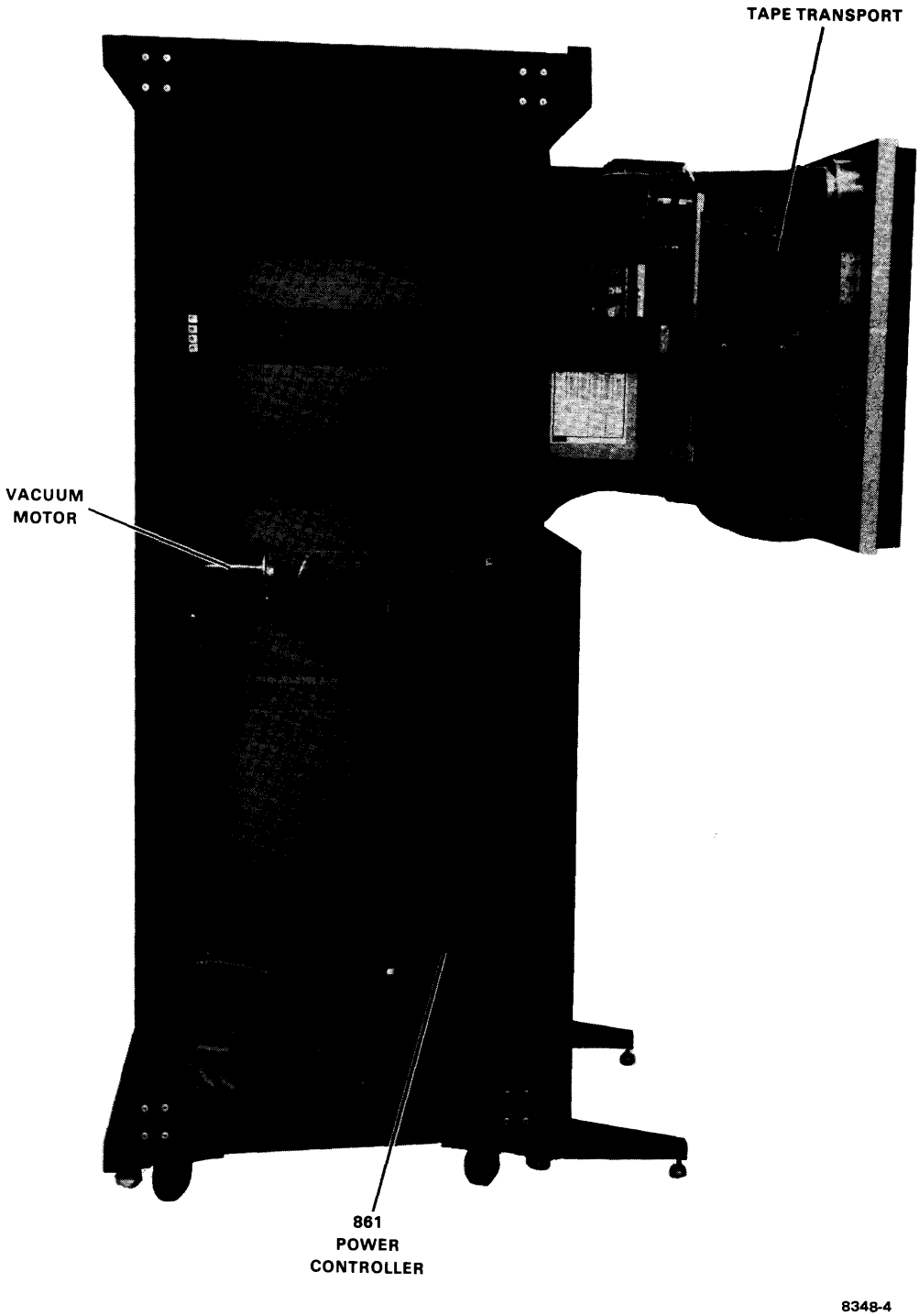
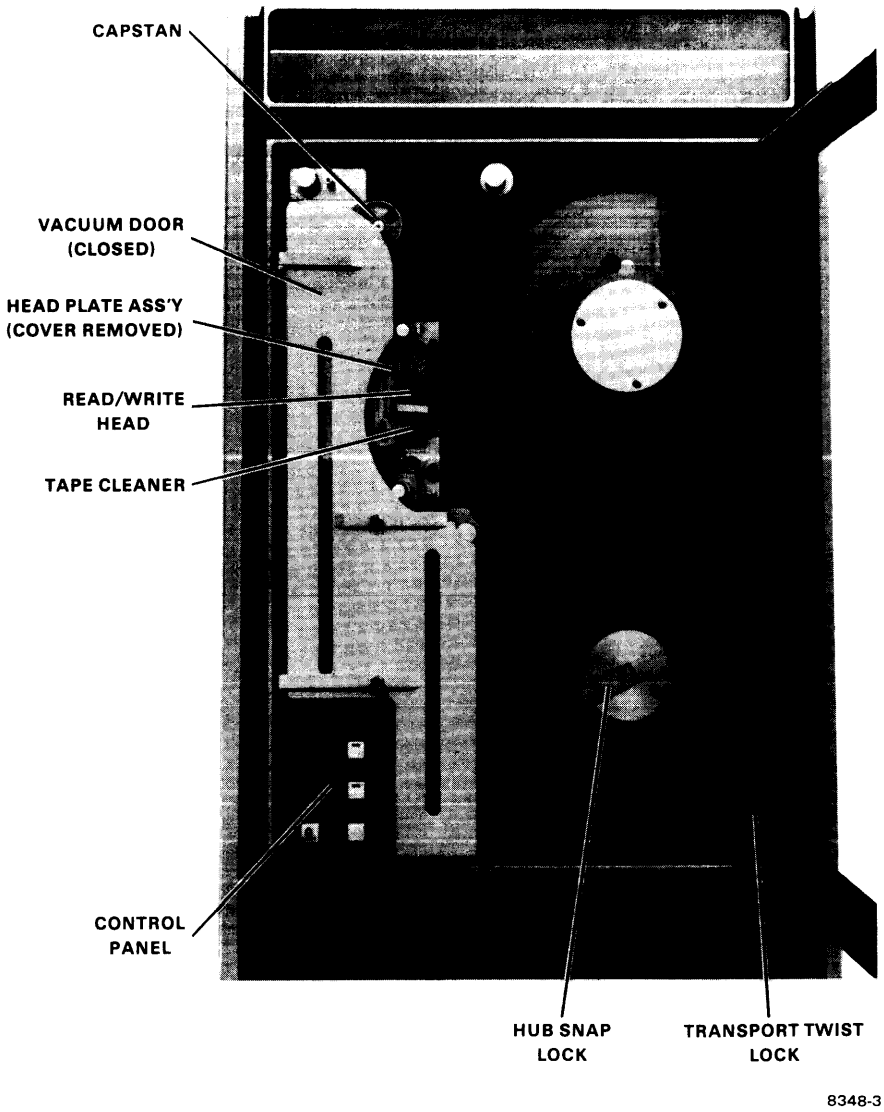
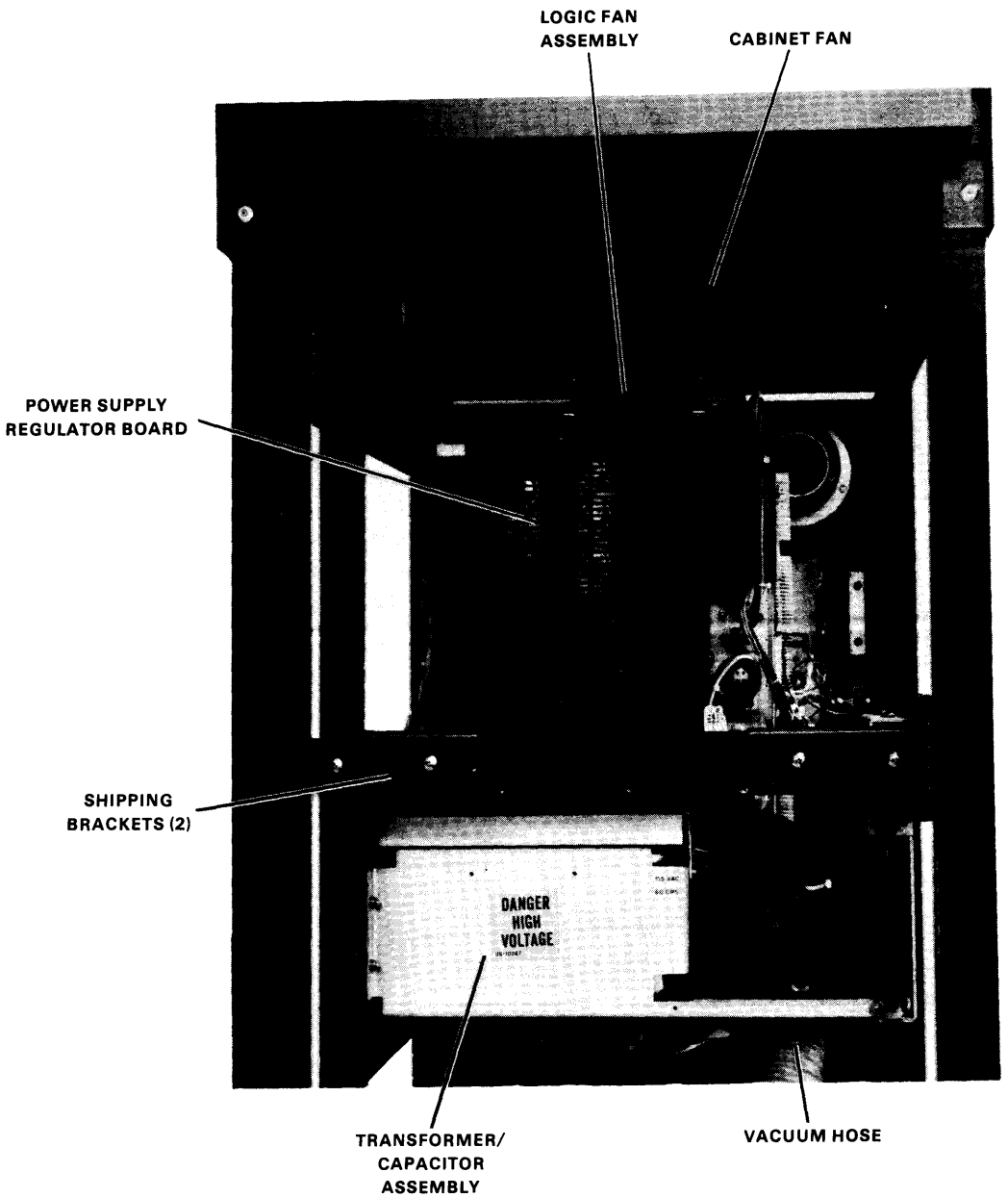


Figure 1-1 TE16 with Transport Extended and Side Panels Removed



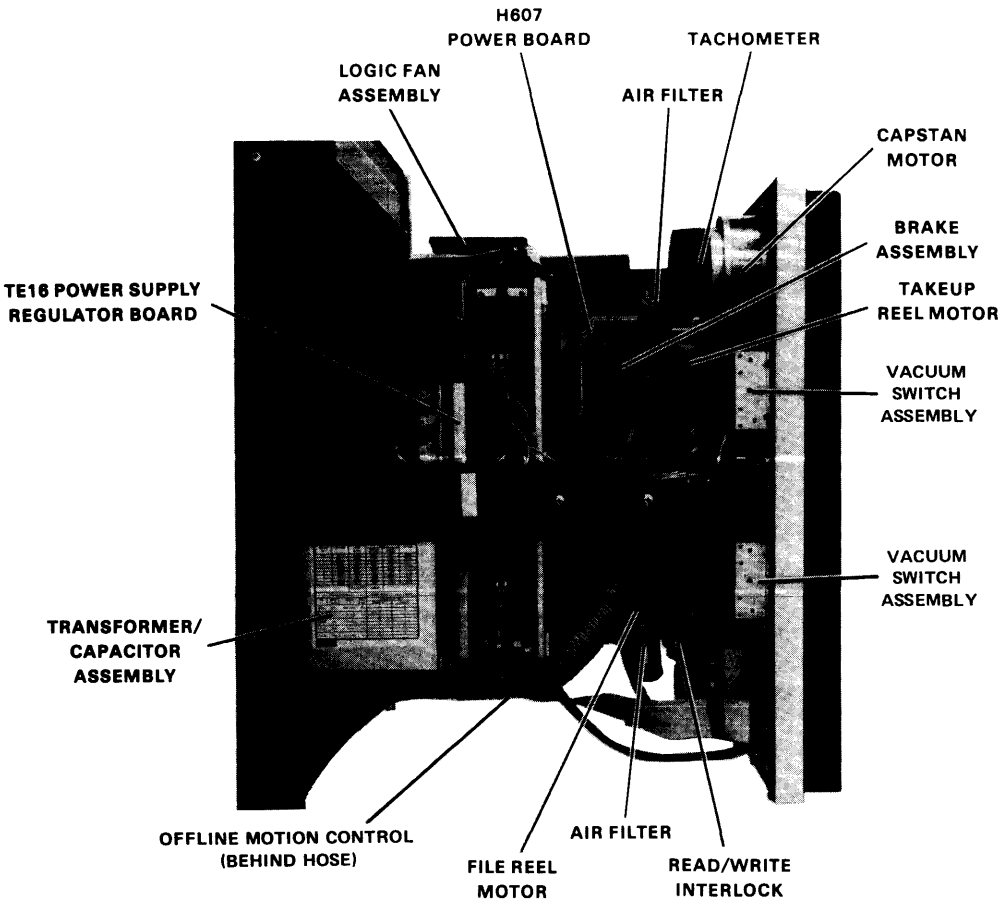
A. Front View

Figure 1-2 TE16 Transport, Front and Rear Views (Sheet 1 of 2)



B. Rear View

Figure 1-2 TE16 Transport, Front and Rear Views (Sheet 2 of 2)

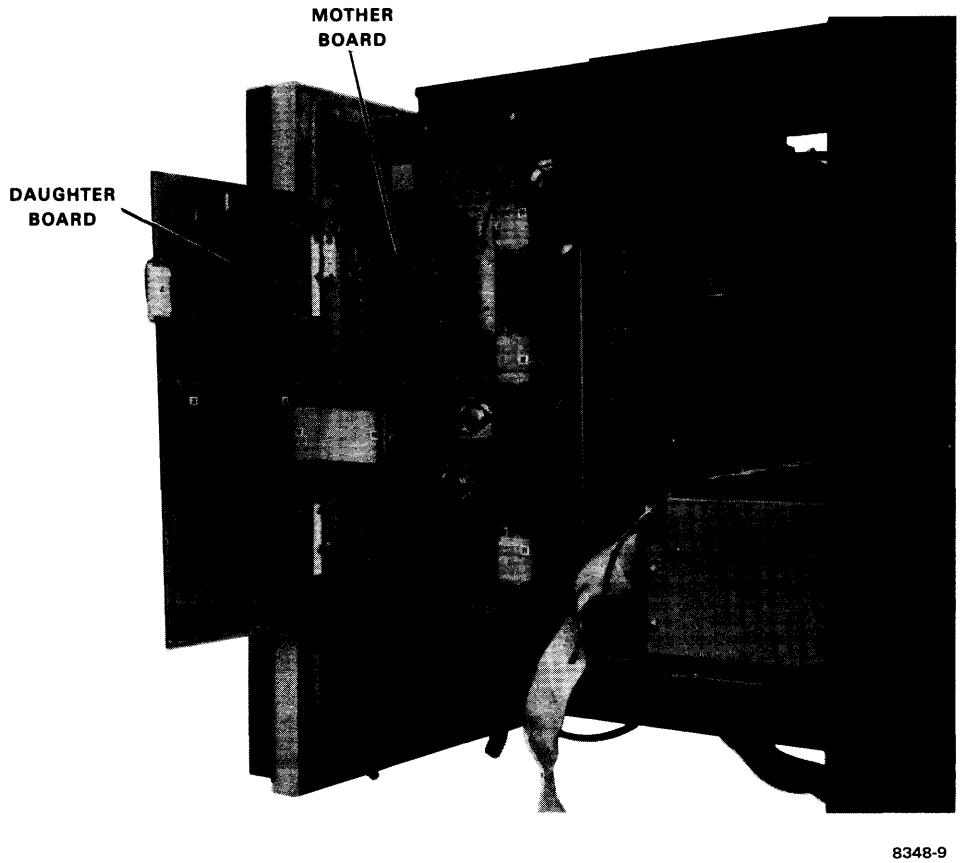


NOTE:
THE CAPSTAN MOTOR AND TACHOMETER FORM AN INTEGRAL UNIT. DO NOT DISASSEMBLE THE UNIT.

A. Left Side

8348-12

Figure 1-3 TE16 Transport, Side Views (Sheet 1 of 2)



B. Right Side

Figure 1-3 TE16 Transport, Side Views (Sheet 2 of 2)

The TE16 master transport comprises interface logic (e.g., M8926, M8927) and a "host" transport. The interface logic processes commands from a controller and issues motion and read/write commands to the host and slave transports; the interface logic also monitors status lines from the host and slave transports. Any status changes at the selected transport are immediately reported to the controller. In response to inputs from the interface logic, the host transport (if selected) controls tape motion and records on and reads from magnetic tape.

The TE16 slave transport consists of a tape transport only. In response to inputs from the interface logic in the master transport, it controls tape motion and records on and reads data from magnetic tape.

Table 1-1 lists the models available in the TE16 Tape Transport.

Table 1-1 TE16 Options

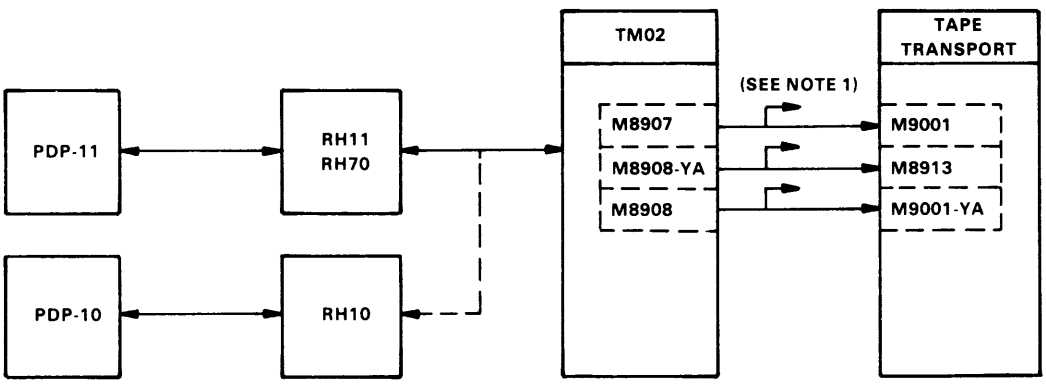
Unit Designation	Data Features	Power Requirements
TE16-EE	9-track PE/NRZI	115 Vac @ 60 Hz
TE16-EF	9-track PE/NRZI	230 Vac @ 60 Hz
TE16-EH	9-track PE/NRZI	115 Vac @ 50 Hz
TE16-EJ	9-track PE/NRZI	230 Vac @ 50 Hz

1.2.1 TE10W/TE10N Information

The TE16 drive may be used in many different controller/processor configurations. When a massbus peripheral is desired, the TE16 is outfitted with cable connector modules that interface directly to the TM02. Up to eight TE16 drives may be interfaced to a TM02 (Figure 1-4).

The TE16 may be outfitted with an M8926 interface module, converting the drive to a TE10W master drive. The TE10W is both electrically and software compatible with a TU10 Master tape drive. Up to seven additional TE10W slave drives may be connected to a TE10W master drive. The TE10W family interfaces to the TM11, TMA11, or TMB11 (unibus) or TM8E (omnibus) controllers (Figure 1-5).

The TE16 may also be outfitted with an M8927 interface module, converting the drive to a TE10N. In this configuration, it is both electrically and software compatible with a TU10 slave tape drive. Additional TE10W slave drives may be interfaced to the TE10N. The TE10N may be used as an add-on drive in any existing TU10 tape system (Figure 1-6).



Notes:

1. Additional slave drives connect (daisy-chain) here.
2. Last slave on bus substitutes M9001-YB for M9001, M8913-YA for M8913 and M9001-YC for M9001-YA.

CP-3026

Figure 1-4 TE16/TM02 Configuration

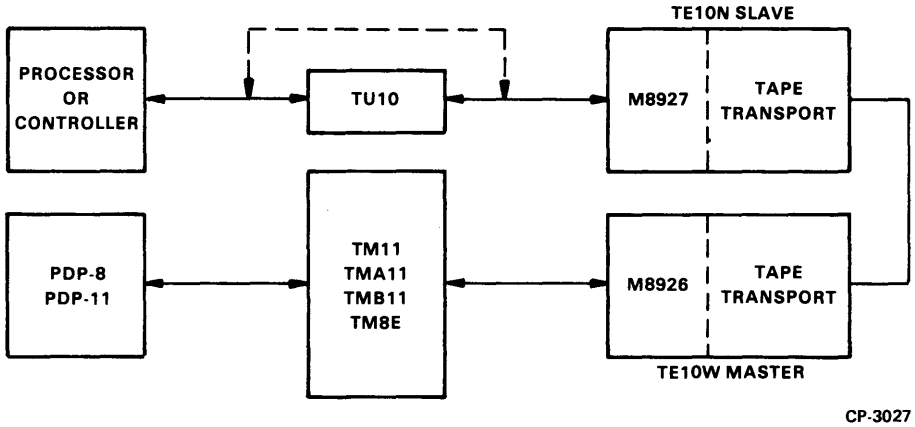


Figure 1-5 M8926 System Configuration

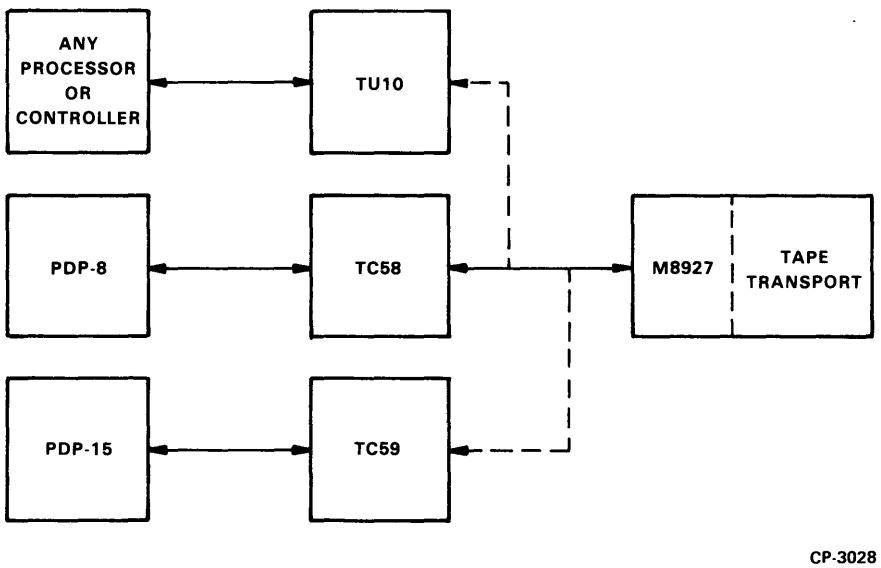


Figure 1-6 M8927 System Configuration

The TE10N also interfaces to Digital's negative logic tape controllers: TC58 (Omnibus), TC59 (PDP-15) or TM10 (PDP-10).

In applications utilizing the TE10N, the total number of transports attached to one controller is limited to eight (8). Thus, in an add-on situation, the total of TU10s, TE10W slaves, and the TE10N must be less than or equal to eight (8). In new systems utilizing negative-logic controllers, the total number of TE10W slaves plus the TE10N must also be less than or equal to eight (8).

From the above discussion, it is apparent that the TE16/TE10W/TE10N tape transports can be used in any application that uses either TU16 or TU10 tape drives. Table 1-2 lists all the available options and the respective replacement transports to be used in various applications.

Table 1-2 Variation List for TE Family

Old	New	Description	
TWU16-EA	TWE16-EA	11/70 Magtape System	115 V/60 Hz
TWU16-EB	TWE16-EB	11/70 Magtape System	230 V/60 Hz
TWU16-EC	TWE16-EC	11/70 Magtape System	115 V/50 Hz
TWU16-ED	TWE16-ED	11/70 Magtape System	230 V/50 Hz
TJU16-EA	TJE16-EA	Magtape System 800/1600	115 V/60 Hz
TJU16-EB	TJE16-EB	Magtape System 800/1600	230 V/60 Hz
TJU16-EC	TJE16-EC	Magtape System 800/1600	115 V/50 Hz
TJU16-ED	TJE16-ED	Magtape System 800/1600	230 V/50 Hz
TU16-EE	TE16-EE	9T 45 in/s Slave Drive	115 V/60 Hz
TU16-EF	TE16-EF	9T 45 in/s Slave Drive	230 V/60 Hz
TU16-EH	TE16-EH	9T 45 in/s Slave Drive	115 V/50 Hz
TU16-EJ	TE16-EJ	9T 45 in/s Slave Drive	230 V/50 Hz
TMB11-EA	TME11-EA	Unibus 9T Tape System	115 V/60 Hz
TMB11-EB	TME11-EB	Unibus 9T Tape System	230 V/60 Hz
TMB11-EC	TME11-EC	Unibus 9T Tape System	115 V/50 Hz
TMB11-ED	TME11-ED	Unibus 9T Tape System	230 V/50 Hz
TMB11-FA	TME11-FA	Unibus 7T Tape System	115 V/60 Hz
TMB11-FB	TME11-FB	Unibus 7T Tape System	230 V/60 Hz
TMB11-FC	TME11-FC	Unibus 7T Tape System	115 V/50 Hz
TMB11-FD	TME11-FD	Unibus 7T Tape System	230 V/50 Hz
	TE10W-EA	9T 1.114 m/s (45 in/s) Master Transport	115 V/60 Hz
	TE10W-EB	9T 1.114 m/s (45 in/s) Master Transport	230 V/60 Hz
	TE10W-EC	9T 1.114 m/s (45 in/s) Master Transport	115 V/50 Hz
	TE10W-ED	9T 1.114 m/s (45 in/s) Master Transport	230 V/50 Hz
TU10W-EE	TE10W-EE	9T 1.114 m/s (45 in/s) Slave Drive	115 V/60 Hz
TU10W-EF	TE10W-EF	9T 1.114 m/s (45 in/s) Slave Drive	230 V/60 Hz
TU10W-EH	TE10W-EH	9T 1.114 m/s (45 in/s) Slave Drive	115 V/50 Hz
TU10W-EJ	TE10W-EJ	9T 1.114 m/s (45 in/s) Slave Drive	230 V/50 Hz
	TE10W-FA	7T 1.114 m/s (45 in/s) Master Transport	115 V/60 Hz
	TE10W-FB	7T 1.114 m/s (45 in/s) Master Transport	230 V/60 Hz
	TE10W-FC	7T 1.114 m/s (45 in/s) Master Transport	115 V/50 Hz
	TE10W-FD	7T 1.114 m/s (45 in/s) Master Transport	230 V/50 Hz
TU10W-FE	TE10W-FE	7T 1.114 m/s (45 in/s) Slave Drive	115 V/60 Hz
TU10W-FF	TE10W-FF	7T 1.114 m/s (45 in/s) Slave Drive	230 V/60 Hz
TU10W-FH	TE10W-FH	7T 1.114 m/s (45 in/s) Slave Drive	115 V/50 Hz
TU10W-FJ	TE10W-FJ	7T 1.114 m/s (45 in/s) Slave Drive	230 V/50 Hz
TU10N-EE	TE10N-EE	Add-On to 9T TU10	115 V/60 Hz
TU10N-EF	TE10N-EF	Add-On to 9T TU10	230 V/60 Hz
TU10N-EH	TE10N-EH	Add-On to 9T TU10	115 V/50 Hz
TU10N-EJ	TE10N-EJ	Add-On to 9T TU10	230 V/50 Hz

Table 1-2 Variation List for TE Family (Cont)

Old	New	Description	
TU10N-FE	TE10N-FE	Add-On to 7T TU10	115 V/60 Hz
TU10N-FF	TE10N-FF	Add-On to 7T TU10	230 V/60 Hz
TU10N-FH	TE10N-FH	Add-On to 7T TU10	115 V/50 Hz
TU10N-FJ	TE10N-FJ	Add-On to 7T TU10	230 V/60 Hz

Both the M8926 and M8927 modules have connections available to expand a DECmagtape system. All additional transports are TE10W slaves, which are virtually identical to the TE16 slave. The three modules (M9001, M8908, and M9001-YA) interface the positive slave bus outputs of the M8926/M8927 in the first transport to the add-on TE10W slave(s). Refer again to Figure 1-4 for more information.

As noted earlier, both the TE10W and TE10N drives are basically identical to the TE16; only the interfacing is different. Therefore, unless otherwise specified, all further references to a transport in this manual are to the TE16 only. Information regarding the M8926 and M8927 interface modules is provided in detail in Sections 5.3.7 and 5.3.8, respectively, of this manual.

1.3 TAPE DRIVE FUNCTIONAL DESCRIPTION

When the TE16 is interfaced with one of the controllers mentioned in the previous section, a magnetic tape system is created.

Figure 1-7 is representative of such a system. Detailed system configurations of many controller/transport combinations are provided in Chapter 2 of this manual. The basic functions performed by a controller in a system are off-line, read, write, write EOF, space forward, space reverse, write-with-extended IRG, and rewind. Each of these functions is briefly described in Table 1-3.

Again, detailed operation of the various controllers and processors that can function with the TE16 is discussed in the respective controller/processor maintenance manuals or technical descriptions. A list of reference documents is supplied in Section 1.5 of this manual.

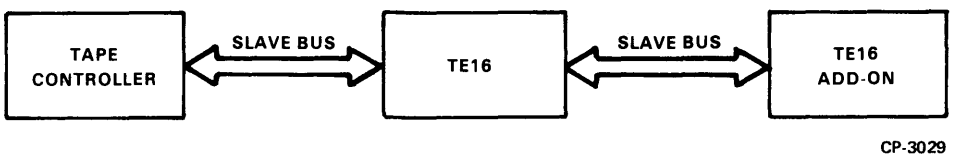


Figure 1-7 TE16 System Block Diagram

1.4 UNIT SPECIFICATIONS

Table 1-4 contains operational, environmental, mechanical and electrical specifications for the TE16 tape drive.

1.5 RELATED DOCUMENTS

Table 1-5 lists literature that supplements the information in this manual.

Table 1-3 TE16 System Functions

Function	Description
Off-Line	The off-line function is used when control is to be returned to the tape transport so that tape can be rewound, reels changed, etc., without using processor time. The off-line function places the selected tape transport in the off-line (local) mode and causes it to begin a rewind operation. A controller cannot write on or read from the magnetic tape when the off-line function is used. Manual intervention is required to return the drive to on-line status (i.e., ON-LINE bottom must be pressed).
Read	This function permits reading from the magnetic tape. During the read operation, the data portion of the record is loaded into the controller data buffer for transfer to the memory. The LRC and CRC characters are read but not transferred into memory
Write	This function permits writing on the magnetic tape. During the write operation, data from the bus is loaded into the controller data buffer register. The controller then transfers the data to the tape transport write heads. The necessary LRC and CRC characters are generated and written on the tape following the data. The write function advances the tape one record.
Write EOF	This function writes an end-of-file (EOF) mark on the tape. When selected, this function erases a 7.6 cm (3 in) segment of tape prior to writing the first character. The EOF mark and the associated LRC character are considered one record. The EOF mark is an octal 23-character (9-track drive; octal 17 for 7-track drive) followed by an octal (or octal 27) LRC character.
Space Forward	This function is used to skip over a number of records to find a specific record on the tape. When selected, the space forward function causes the tape transport to advance a specific number of records. The program loads the byte/record counter with the two's complement of the number of records to be spaced over. Detection of an end-of-file mark terminates a space operation. Space forward is used for tape positioning only and, therefore, does not affect information stored on the tape or in memory.
Space Reverse	This function is identical to the space forward function except the tape moves in the reverse, rather than in the forward direction.
Write-with-Extended-IRG	This function is identical to the write function except that a 7.6 cm (3 in) segment of tape is erased before writing the first character.

Table 1-3 TE16 System Functions (Cont)

Function	Description
Rewind	This function is used for rewinding the tape on the feed reel so that the tape can either be loaded from the transport or operation can start at the beginning of the tape. When this function is used, the tape moves in the reverse direction at a much higher speed, 3.8 m/s or 150 in, than for other functions, until the beginning-of-tape (BOT) marker is detected. When the BOT marker is detected, the tape slows down and comes to a complete stop at a point beyond the BOT marker. It then moves forward until the BOT marker is again detected, where it comes to a final stop. Rewind is used only for tape positioning and has no effect on information stored on the tape or in the memory.

Table 1-4 TE16 Specifications

Category	Parameter	Specification
Main Specifications	Storage medium	1.27 cm (1/2 in) wide magnetic tape (industry compatible)
	Capacity/tape reel	23 million characters (NRZI); 46 million characters (PE)
	Data transfer rate	36,000 char/s (NRZI); 72,000 char/s (PE)
	Transports/Formatter, maximum	8
Data Organization	Number of tracks	9 (or 7 TE10W/N only)
	Recording density	200, 556, 800 bits/in (TE10); 800 and 1600 bits/in (TE16); program selectable
	Interrecord gap	1.27 cm (0.5 in) minimum; 1.65 cm (0.65 in) nominal
	Recording method	NRZI or phase-encoded; industry compatible.
Tape Motion	Speed; forward and reverse	1.14 m/s (45 in/s)
	Rewind speed	3.8 m/s (150 in/s) nominal
	Tape transport	Single capstan; vacuum columns
	Start/stop distance	6.3 mm (0.25 in) nominal
	Start/stop time	8 ms maximum

Table 1-4 TE16 Specifications (Cont)

Category	Parameter	Specification	
Tape Characteristics	Width	1.27 cm (0.5 in)	
	Length	731.6 m (2400 ft) maximum	
	Type	Mylar base; iron-oxide coated	
	Thickness	0.038 mm (1.5 mils)	
	Tension	227 g (8.0 oz)	
	Reel diameter	26.7 cm (10.5 in)	
	Reel hub	9.37 cm (3.69 in) diameter (industry standard)	
Mechanical	Tape transport, mounting	Mounts on slides in a standard 48.3 cm (19 in) cabinet.	
	TE16 Transport	Without Cabinet	With H950 Cabinet
	Depth	0.64 m (25 in)	.76 m (30 in)
	Width	0.48 m (19 in)	.53 m (21 in)
	Height	0.66 m (26 in)	.83 m (72 in)
	Weight	70 kg (150 lb)	204 kg (450 lb)
	861 power controller		
	Depth	0.20 m (8 in)	
	Width	0.48 m (19 in)	
	Height	0.13 m (5 in)	
	Weight	4.54 kg (10 lb)	
Interchannel Displacement	Write	1.9 μm (75 μin) maximum	
	Read	1.9 μm (75 μin) maximum	
	Erase head	Full width	
Power	Input current	8 A at 115 V; 6 A at 230 V	
	Input Power	920 VA; 1380 VA	
	Voltage	115/230 Vac ±10% (Note 1)	
	Frequency	47–63 Hz; single phase (Note 2)	
Operating Environment	Temperature	15° to 32°C (Note 3)	
	Relative Humidity	20% to 80%, with maximum wet bulb 25° C and minimum dew point 2°C (no condensation)	
	Altitude	2438 m (8000 ft) maximum	

Table 1-4 TE16 Specifications (Cont)

Category	Parameter	Specification
Miscellaneous	BOT, EOT detection	Photoelectric sensing of reflective strip, industry compatible
	Broken tape detection	Vacuum fail-safe
	Read/Write head displacement	3.8 mm (0.15 in)
	Electrical skew	Write deskew only; Read skew mechanically aligned.
	Interlocks	Interlocks disengage the tape transport mechanism and reel motors when vacuum has been lost in the vacuum columns.
	Tape Packing	The tape handling system provides consistent packing of the tape on the supply and take-up reels during any operational mode of the transport.
	Transport Bus	8 transports per controller, maximum 22.8 m (75 ft) cable length, maximum. **NOTE** **Maximum length of 15.2 m (50 ft) from TC59 to first TE10 N.**

NOTE 1. Transformer taps allow for nominal line voltages of 105 and 125 Vac.

NOTE 2. Vacuum system must be configured for operation at either 47–53 Hz or 57–63 Hz.

NOTE 3. Magnetic tape operation is more reliable if the temperature is limited to 65° to 75° F (18° to 24° C) and the relative humidity to 40 to 60%.

Table 1-5 Related Documents

Title	Number	Description
PDP-B/E Processor Maintenance Manual, Vol 1	DEC-8E-HMM1A-A-D	Contains maintenance and user information for the PDP-8 Family of computers.
PDP-11 Peripherals Handbook (1976)	EB0596176	Devoted to the discussion of the various peripherals used with PDP-11 systems. Describes the unibus structure.

Table 1-5 Related Documents

Title	Number	Description
PDP-15 Users Handbook, Vol 1 (Processor); PDP-15 Users Handbook, Vol 2 (Peripherals).	15H 172 15H 175	Devoted to the operation of the PDP-15 and its related peripherals.
861 A, B, C Power Control Maintenance Manual	EK-861AB-MM-002	Contains theory of operation and maintenance instructions for the 861 Power Controller.
TC58 Magnetic Tape Control System Description	EK-TC58-TM-001	Contains a detailed description of TC58 Controller operation.
TC59 Magnetic Tape Control Instruction Manual, Vol. 1	15H188	Contains a detailed description of the TC59 Controller (User Information).
TU16/TM02 Tape Drive System Maintenance Manual	EK-TU16-MM-002	Contains detailed theory and user operation information for the TM02 Controller.
TM03 Magnetic Tape Formatter User Manual	EK-TM03-OP-001	Contains complete user operation information for the TM03 Formatter.
TM03 Magnetic Tape Formatter Maintenance Manual	EK-TM03-MM-001	Contains detailed theory and maintenance information for the TM03 Formatter.
TS03/TM02 Tape Drive System Maintenance Manual	EK-T3TMB-MM-001	Contains detailed theory and user operation information for the TM8E Controller.
TM11 DECmagtape System Maintenance Manual	EK-TM11-TM-004	Contains detailed information on the TM11.
TMA11 DECmagtape System Maintenance Manual	EK-TMA11-MM-PRE	Contains detailed information on the TMA11.
TMB11/TU10W DECmagtape Maintenance Manual (TMB11-E/F System)	EK-TMBEF-MM-001	Contains detailed information on the TMB11-E/F System.
RH10 Massbus Controller Maintenance Manual	EK-RH10-MM-002	Contains detailed information on the RH10.

CHAPTER 2
INSTALLATION

2.1 SITE PLANNING AND CONSIDERATIONS

Space, power, and environmental requirements are discussed in this section.

2.1.1 Space Requirements

The TE16 is housed in either an H950 or H9500 cabinet. Figures 2-1 and 2-2 illustrate the space and service clearances required for each cabinet, respectively. Adequate space must be provided to slide the equipment out of the rack for servicing and to open the front door on the TE16 DECmagape transport. A tape controller may be housed in either of the above mentioned cabinets or in an expansion cabinet.

2.1.2 Power Requirements

The TE16 DECmagtape unit can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained to within 20 percent of the nominal value, and the frequency should not vary more than 3 Hz.

2.1.3 Environmental Requirements

The TE16 DECmagtape unit should be located in an area free of excessive dust and dirt or corrosive fumes and vapors. To ensure proper cooling, the bottom of the cabinet and the fan inlet at the top of the cabinet must not be obstructed. The operating environment should have cool, well-filtered, humidified air, a temperature range of 15° to 27°C (49° to 80°F) and relative humidity of 40 to 60 percent.

2.2 UNPACKING

The TE16 DECmagtape may be shipped with or without a controller. Unpacking and installation procedures may vary slightly, depending on the system configuration. For example, if the user has ordered a complete processor/controller/tape transport system, the controller is shipped installed in its appropriate rack in the TE16 cabinet. However, if only part of the system is shipped because the user already has a basic computer system, then the controller may be shipped separately with the appropriate cables.

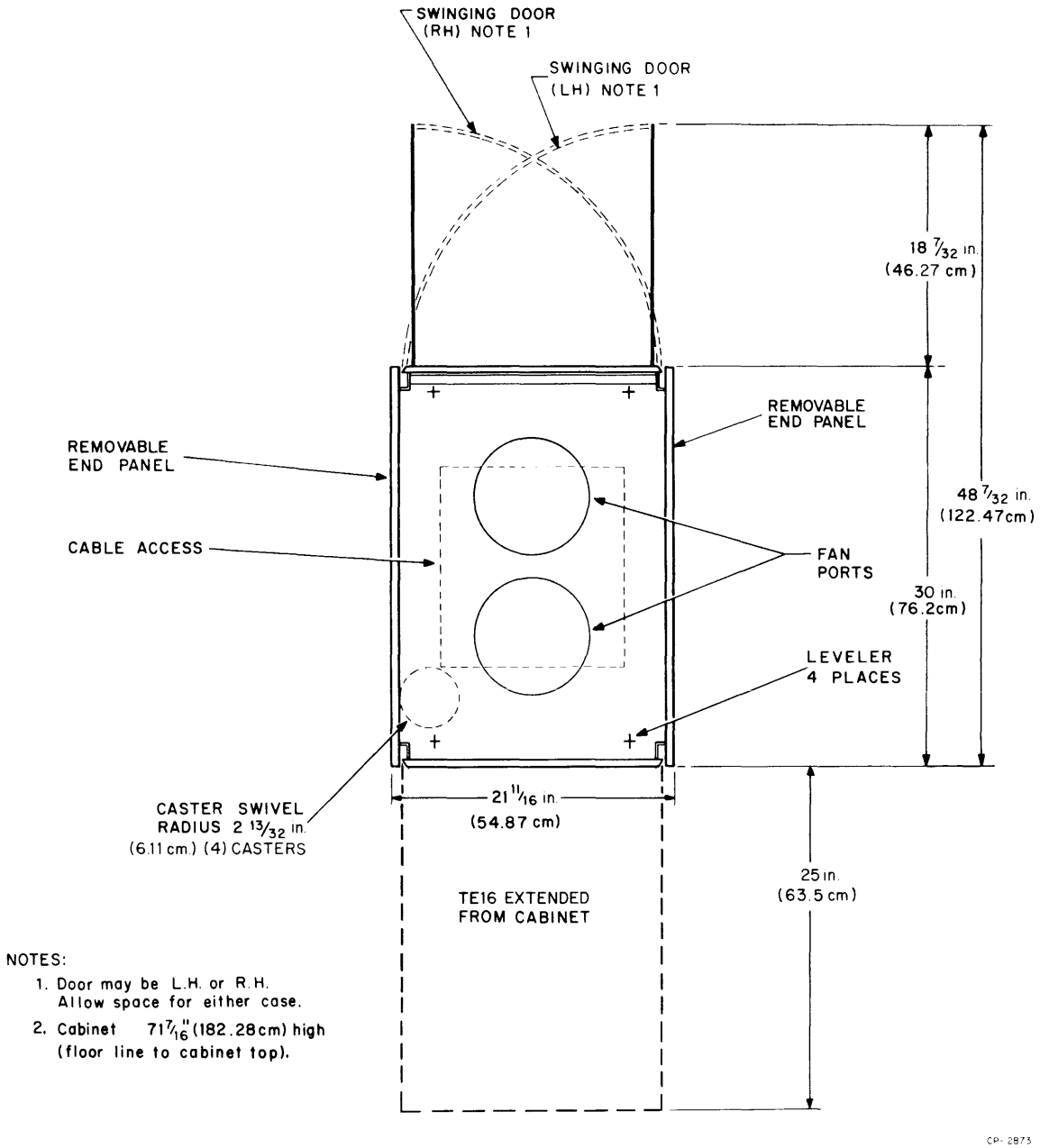


Figure 2-1 H950 Cabinet: Space and Service Clearance, Top View

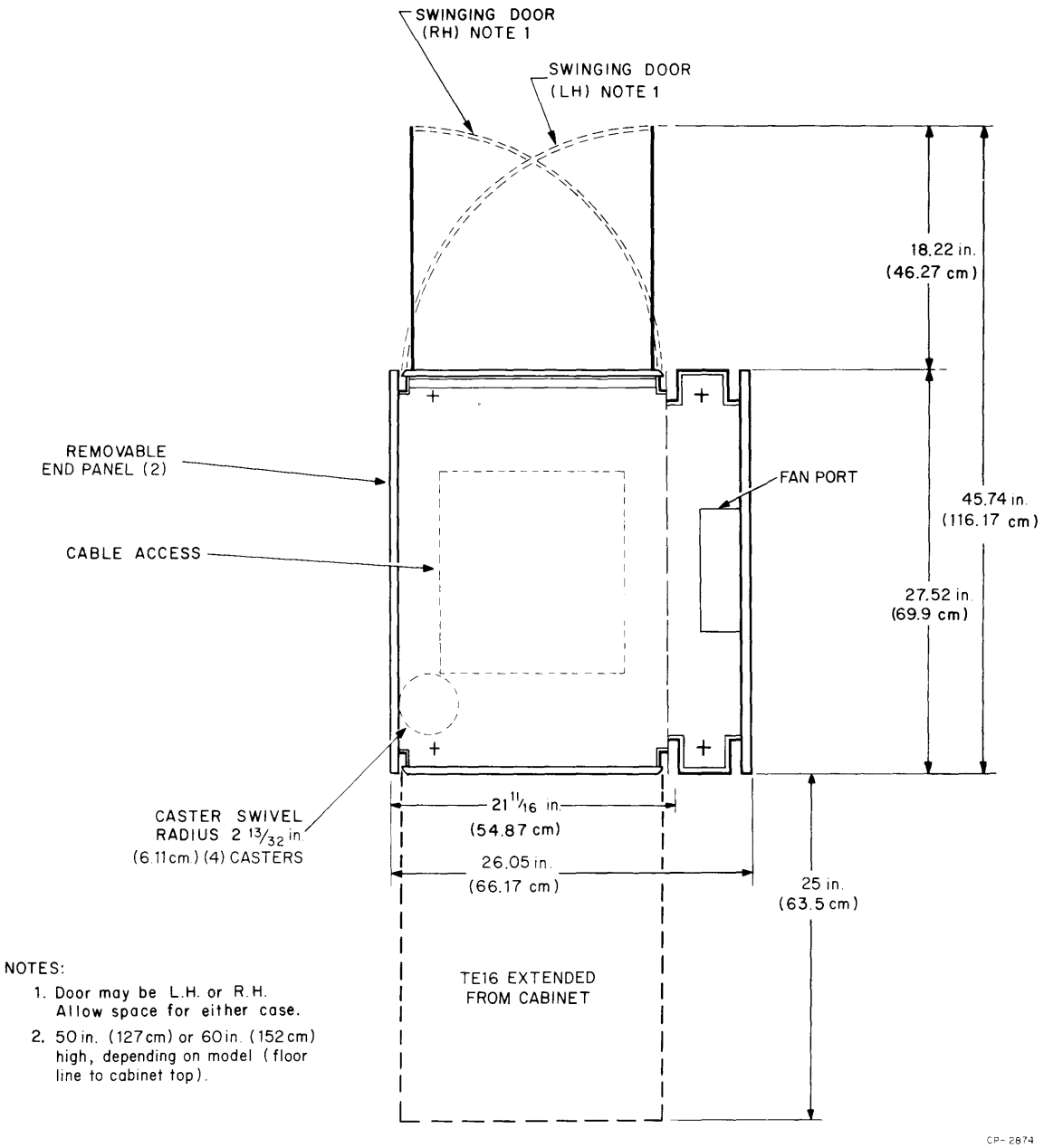


Figure 2-2 H9500 Cabinet: Space and Service Clearance, Top View

2.2.1 TE16 Cabinet Unpacking

To unpack the cabinet, proceed as follows:

1. Remove outer shipping container.

> **NOTE**
>
> **The container may be either heavy corrugated cardboard or plywood. In either case, remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter.**

2. Remove the polyethylene cover from the cabinet.

3. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting side rails and are exposed by opening the access door(s). Remove the bolts.

4. Raise the leveling feet above the level of the roll-around casters.

5. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

6. Roll the system to the proper location for installation.

2.2.2 Controller Unpacking

Refer to the relevant documentation, furnished with the specific controller used, for unpacking information.

2.3 INSPECTION

After removing the equipment from its container(s), inspect it and report any damage to the responsible shipper and the local DIGITAL sales office. Inspect as follows:

1. Inspect all switches, indicators, and panels for damage.

2. Remove equipment covers where necessary and inspect for loose or broken modules, blower or fan damage, and loose nuts, bolts, screws, etc.

3. Inspect the wiring side of logic panels for bent pins, broken wires, loose external components, and foreign material.

4. Check the TE16 transport(s) for any foreign material that may have lodged in the take up reel or other moving parts.

5. Check the TE16 power supply for proper seating of fuses and power connectors.

2.4 TE16 INSTALLATION AND CABLING

To install the TE16 (either H950 or H9500) cabinet, proceed as follows:

1. Lower the leveling feet so that the cabinet is resting on the floor, not on the roll-around casters.

2. Use a spirit level to level the cabinet; ensure that all leveling feet are firmly on the floor.

3. Remove the shipping screws that secure the equipment to the cabinet.

4. If the TE16 being installed is housed in an H950 cabinet and the cabinet is to be bolted to another, install filler strips (P/U H952-G) between the cabinets as shown in Figure 2-3. Tighten the bolts that secure the cabinet groups together, and then recheck that the cabinets are level. (H9500 cabinets do not require filler strips when bolted together.)

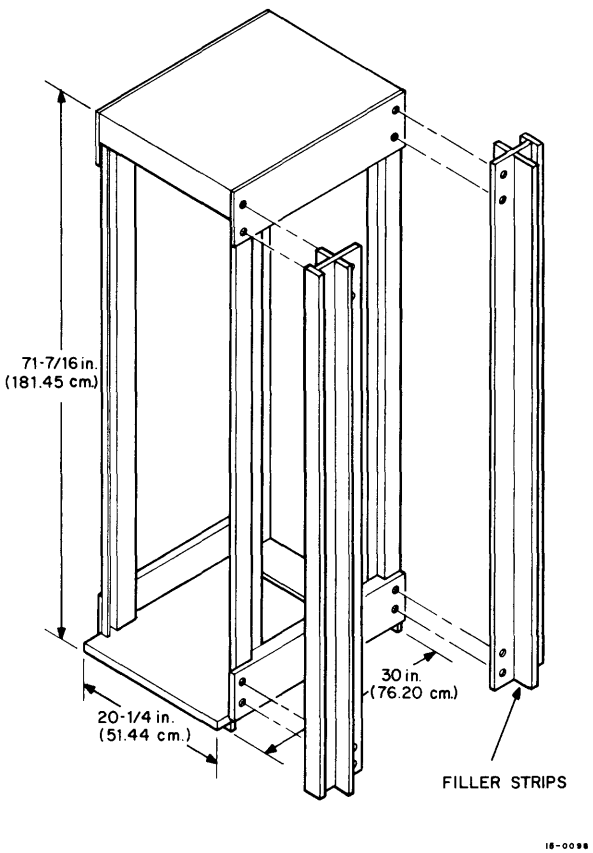


Figure 2-3 Installation of Filler Strips

5. Remove the plastic shipping pin from the top of the cabinet rear access door.

6. Ensure that the TE16 cabinet and the controller are connected to the same ground. Be sure that the cabinet ground strap is installed.

7. After the TE16 has been positioned per the site plan, open the TE16 front door and loosen the two twist-locks located in the upper left and lower right corners of the transport front panel.

8. Loosen the two shipping brackets that secure the transport to the rear of the cabinet frame. Slide the brackets toward the center of the cruciform, as shown in Figure 2-4, and then tighten the shipping brackets.

NOTE

Do not remove the shipping brackets. If the TE16 is to be reshipped or installed in a new location, the shipping brackets must be repositioned over the vertical members and then tightened.

9. If necessary, clean all outer surfaces.

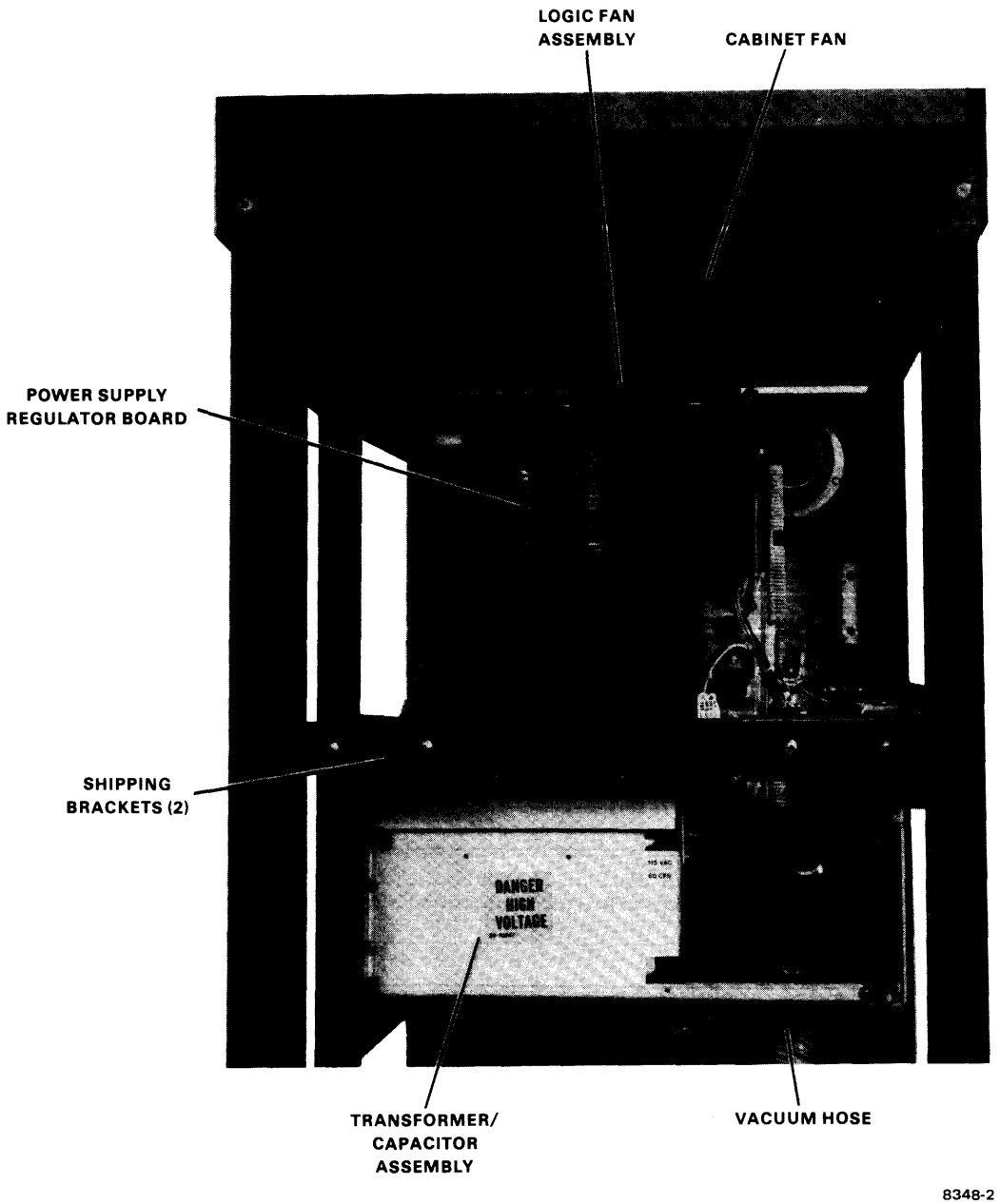


Figure 2-4 Transport Hold-Down Shipping Brackets

2.4.1 Cable Connections

All power and interconnecting cabling is discussed in this section.

2.4.1.1 Power Cable – The power cable supplied with the TE16 is plugged into a local power outlet.

CAUTION

Before connecting the TE16 to the local power source, ensure that the line voltage and frequency are compatible with the TE16 power requirements.

2.4.1.2 System Cabling – The TE16 (or variations of the TE16, i.e., TE10W, TE10N) may be used with many different processor/controller combinations. Figures 2-5 through 2-14 illustrate a possible system configuration for each possible combination. Each illustration lists all the cables, modules, and locations used for that system.

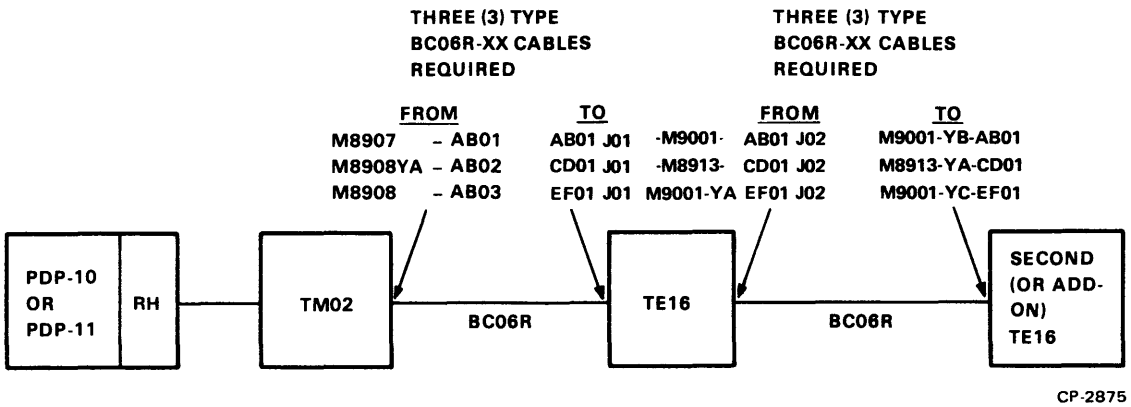


Figure 2-5 Cabling a TE16 in a New PDP-10/11 System with Massbus Controller (RH11, RH70); i.e., RH10/20 with TM02

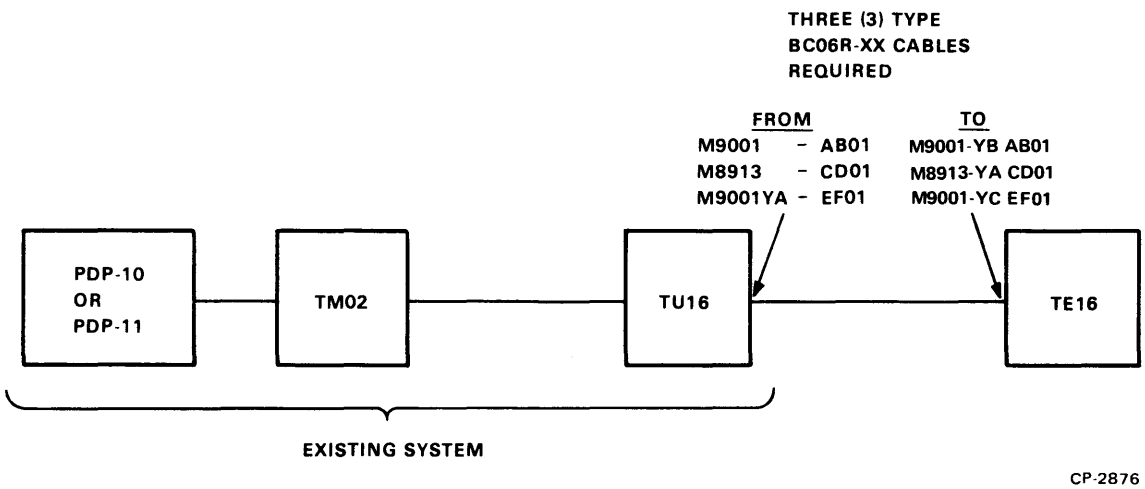
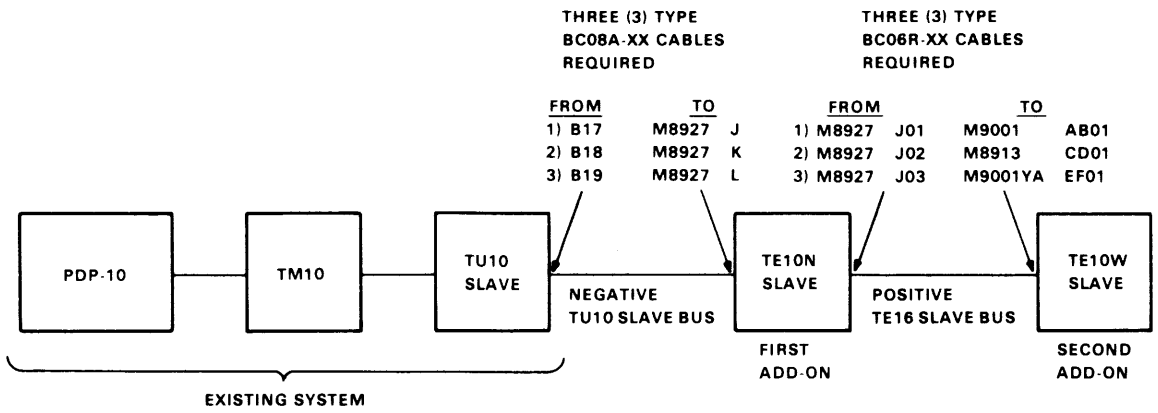


Figure 2-6 Adding Transports to Existing Massbus System



NOTES:

1) -XX denotes cable length, in feet.

2) TU10(s) would be present when adding to an existing system. When configuring new system, TE10N could cable directly to TM10.

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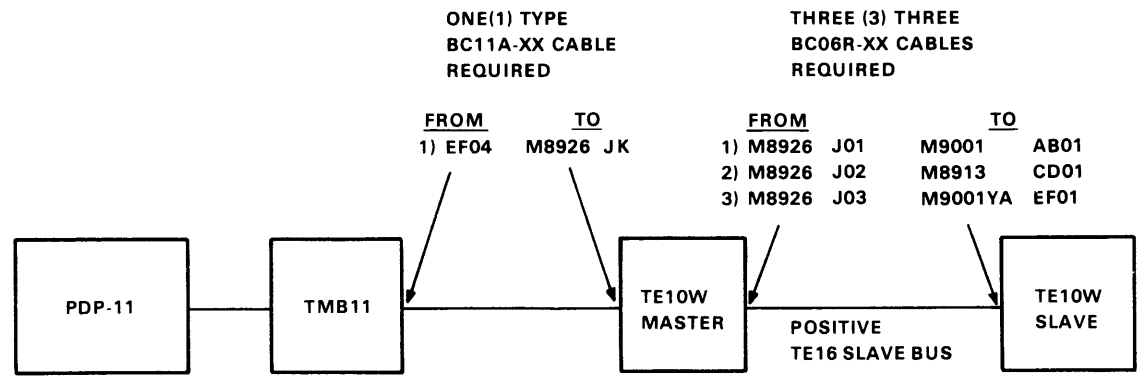
Figure 2-7 Adding Drives to PDP-10 System When Formatter Is TM10



NOTE: -XX denotes cable length, in feet.

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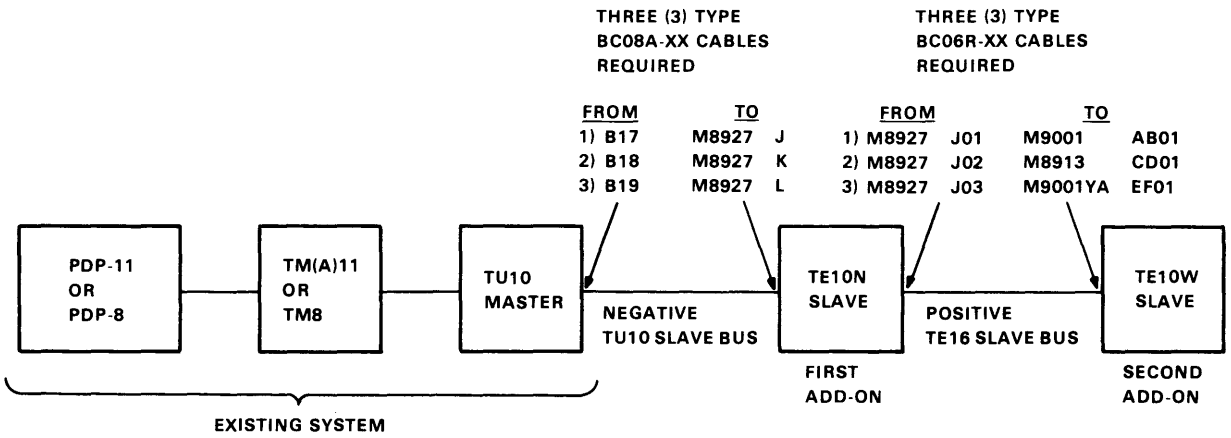
Figure 2-8 Installing Transports in a New PDP-11 System



NOTES:

1) -XX denotes cable length, in feet.

2) If adding to an existing TU10 system that has more than one transport, the TE10N should be cabled to the last TU10 slave. TE10N must be electrically last drive on negative bus, G741 and G741-YA terminators are required in TU10 Master. No other external terminators are required, as they are contained in the M8927 module.

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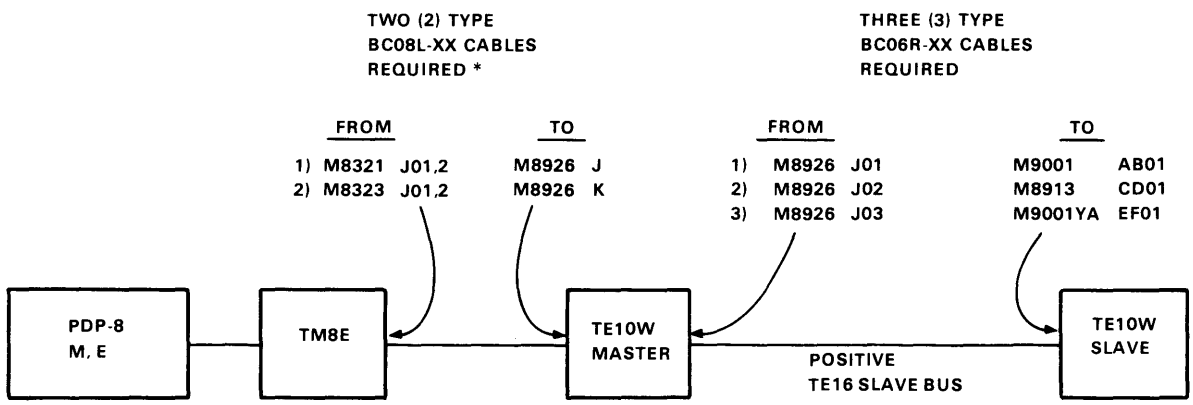
Figure 2-9 Installing Slave Transports to an Existing PDP-11 or PDP-8 System



NOTES:

* - Modified per D-AD-7011571-0-0

-XX denotes cable length, in feet.

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Figure 2-10 Installing Transports in a New PDP-8 System

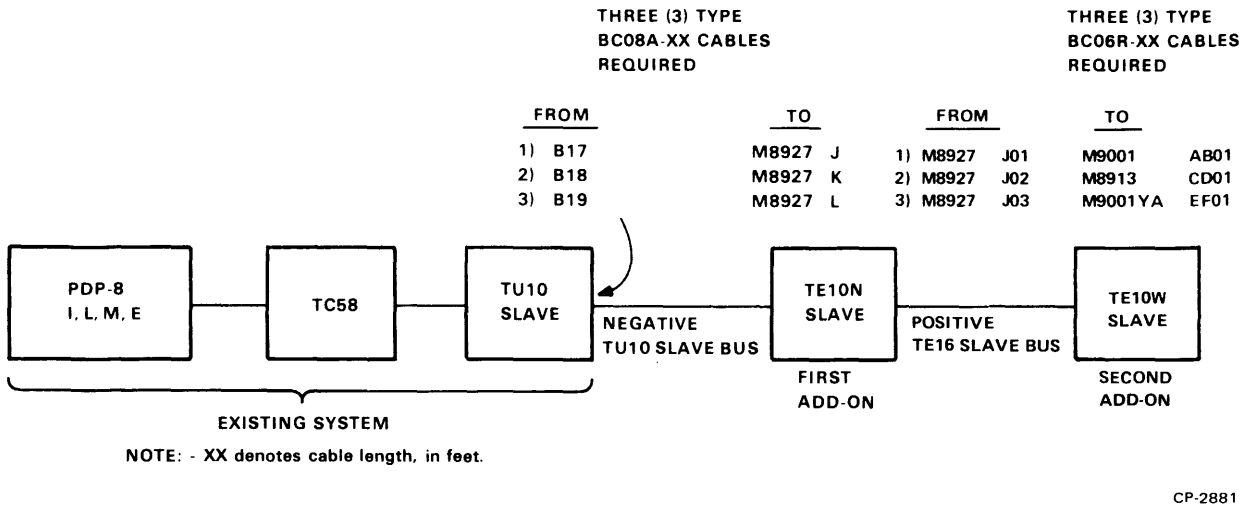


Figure 2-11 Adding Transports to an Existing PDP-8/TC58 System

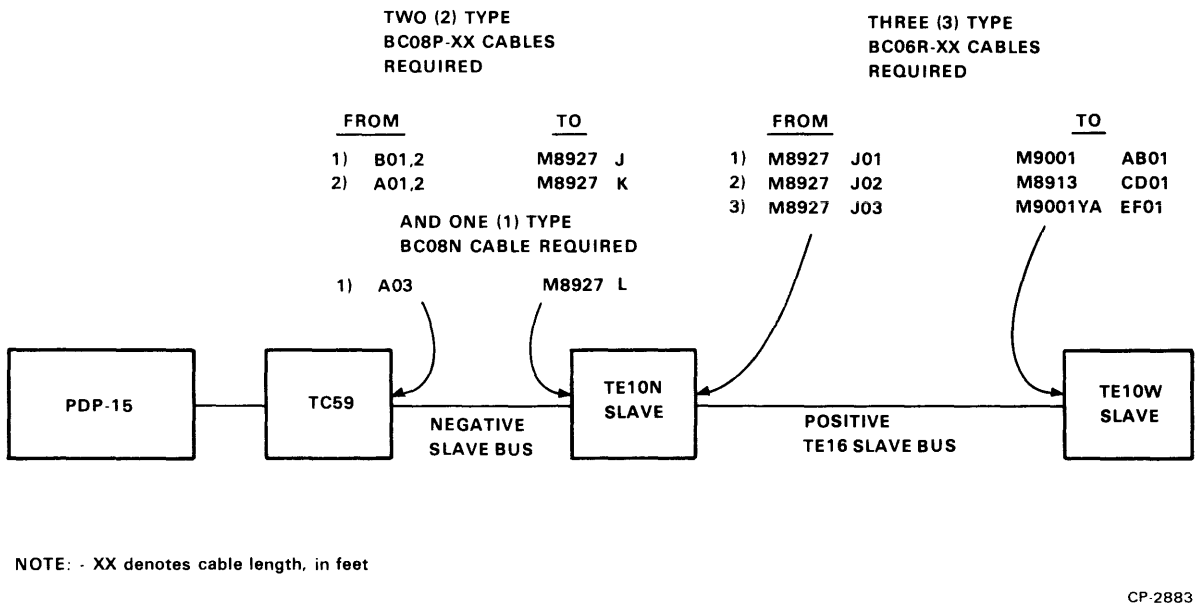


Figure 2-12 Installing Transports in a New PDP-15 System

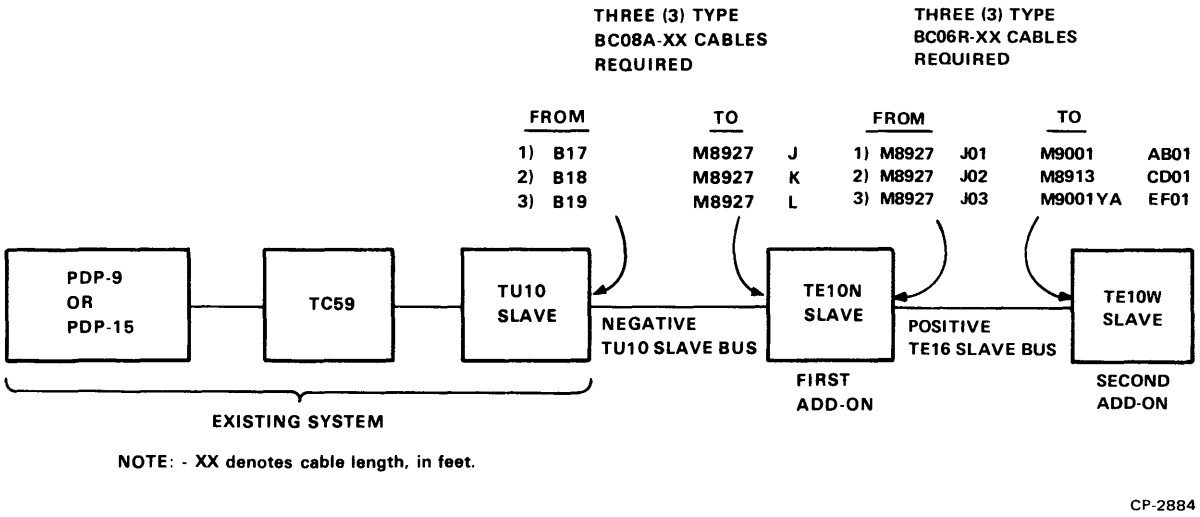


Figure 2-13 Adding Transports to an Existing TC59/TU10 System

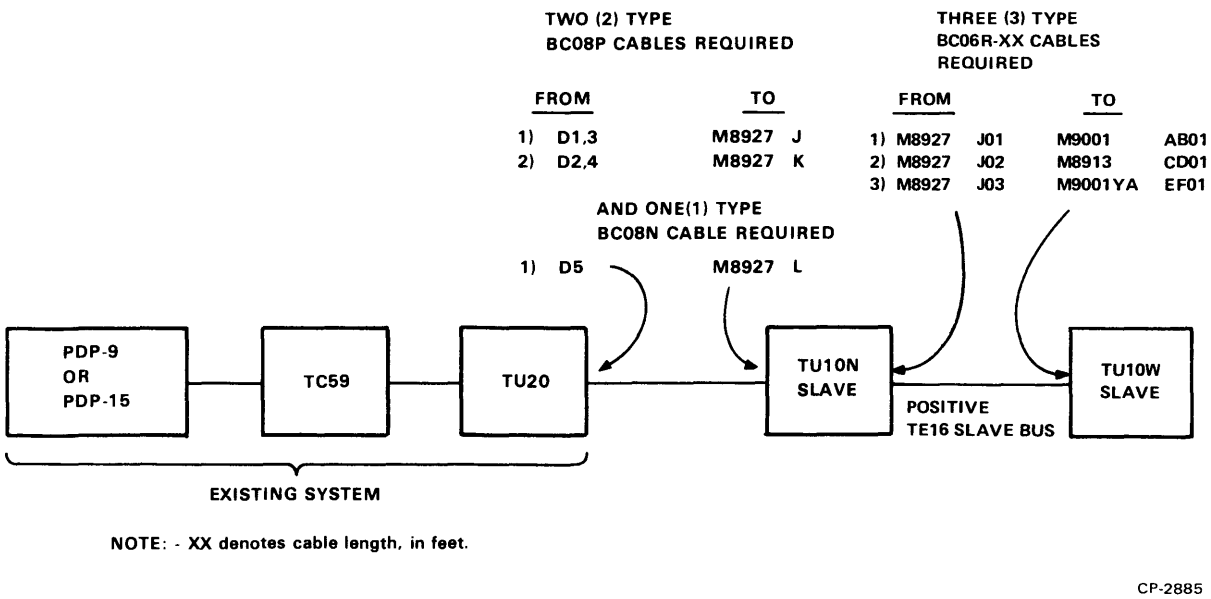


Figure 2-14 Adding Transports to an Existing TC59/TU20 System

To aid in locating the relative figure for this particular installation, the figure numbers and titles are listed below.

Figure No.	Title
2-5	Cabling a TE16 in a New PDP-10/11 System
2-6	Adding Drives to an Existing Massbus System
2-7	Adding Drives to PDP-10 System when Controller is TM10
2-8	Installing Drives in a New PDP-11 System
2-9	Installing Slave Drives to an Existing PDP-11/8 System
2-10	Installing Drives in a New PDP-8 System
2-11	Adding Drives to an Existing PDP-8/TC58 System
2-12	Installing Drives in a New PDP-15 System
2-13	Adding Drives to an Existing TC59/TU10 System
2-14	Adding Drives to an Existing TC59/TU20 System

Locate the figure relative to the particular installation,and configure the system according to the information provided on the figure.

Figure 2-15 provides an overview of system cabling.

2.4.1.3 Module Utilization – Figures 2-16, 2-17, 2-18 and 2-19 show the module types and locations of a TE10W master and slave, TE10N slave, and TE16, respectively. When configuring a system, refer to the relevant diagram for a summary of MU information.

2.5 ACCEPTANCE TESTING

This section lists and describes all the tests and test procedures necessary to properly test and accept the TE16 DECmagtape Transport.

The TE16 operates with many different processor/controller combinations. The paragraphs listed below refer to the acceptance test procedures for the various combinations:

2.5.1	TM02/TE16
2.5.2	TMB11/TE10W/N
2.5.3	TM8E/TE10W/N
2.5.4	TC59/TE10N

When those tests listed in the relevant paragraph are passed, the TE16 is operating correctly.

2.5.1 TM02/TE16 Acceptance Test Procedure

This section describes the TM02/TE16 Acceptance Test Procedure. When the following tests are complete, the TM02/TE16 is operating correctly.

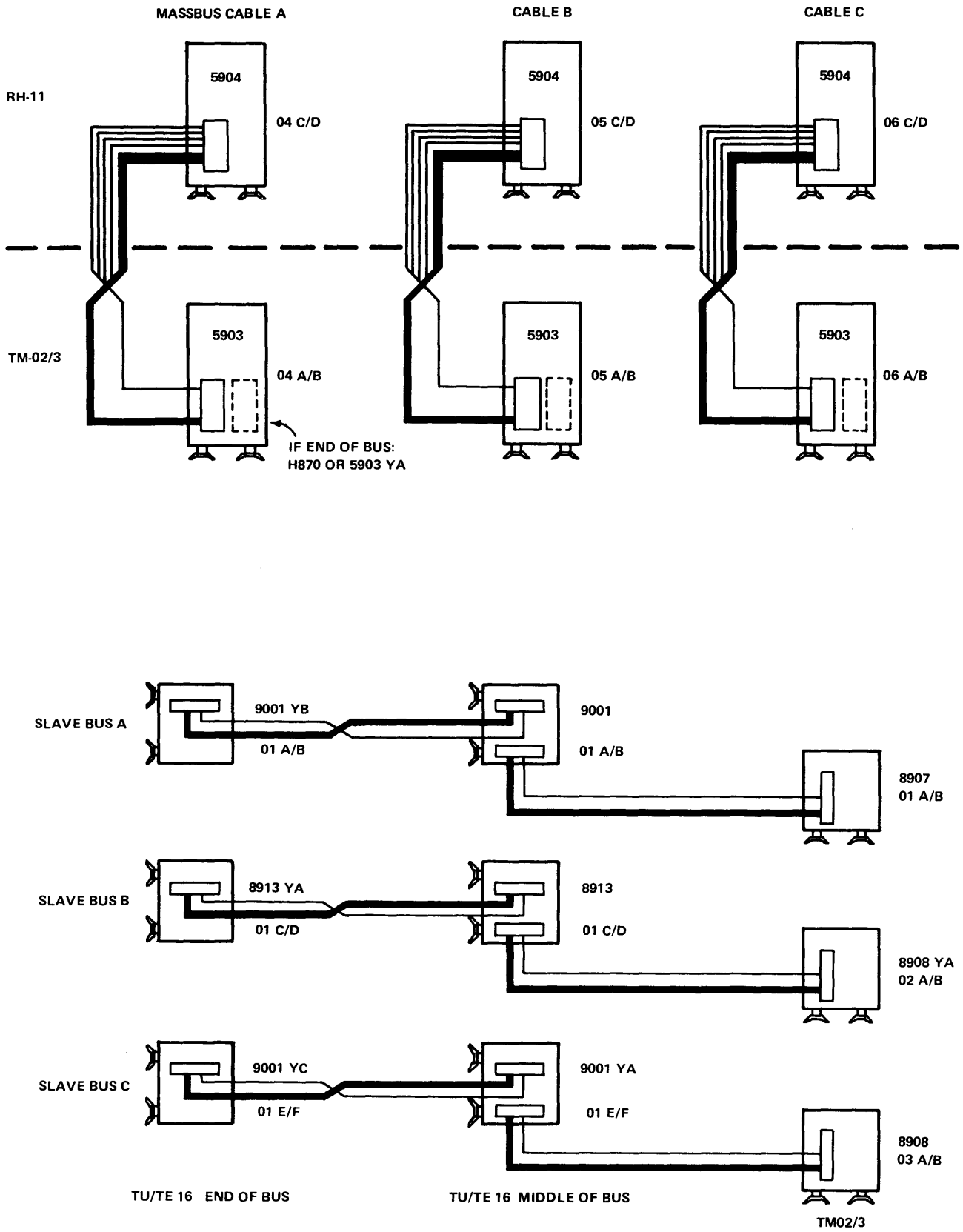


Figure 2-15 Overview of System Cabling

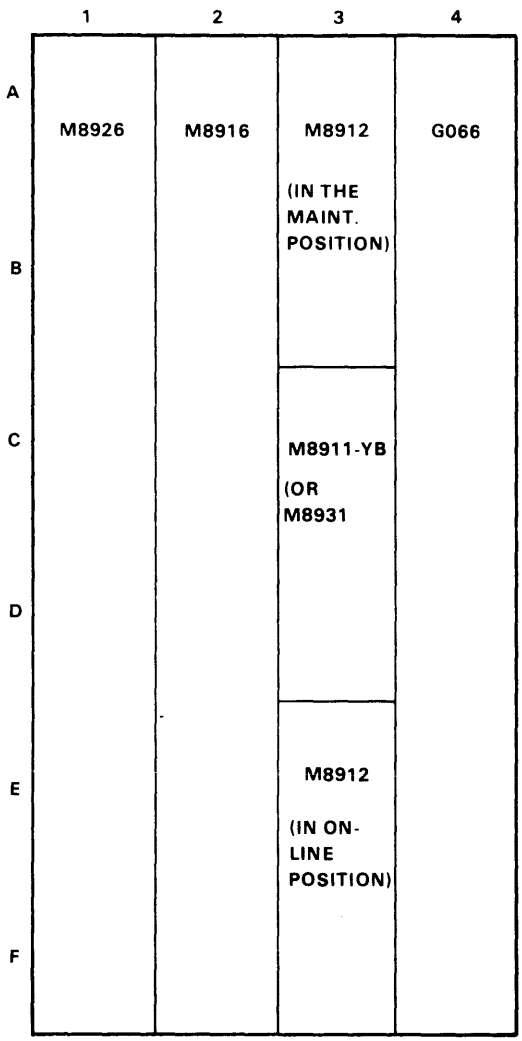
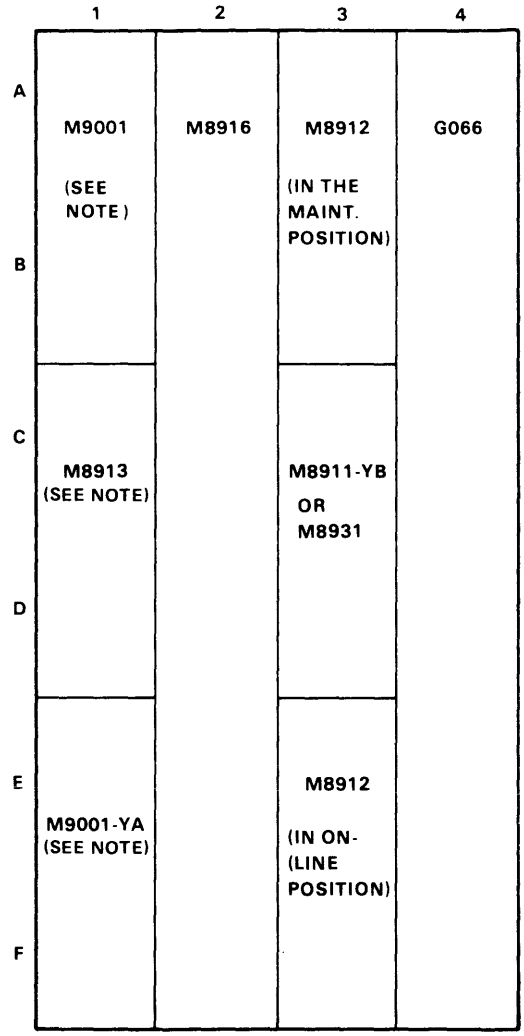


Figure 2-16 TE10W Master, Module Utilization Diagram



NOTE:

Module utilization of TE10W Slave is identical to that of TE16 with the exception that a TE16 on end of slave bus requires M9001-YB, M8913-YA, and M9001-YC.

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Figure 2-17 TE10W Slave Module Utilization Diagram

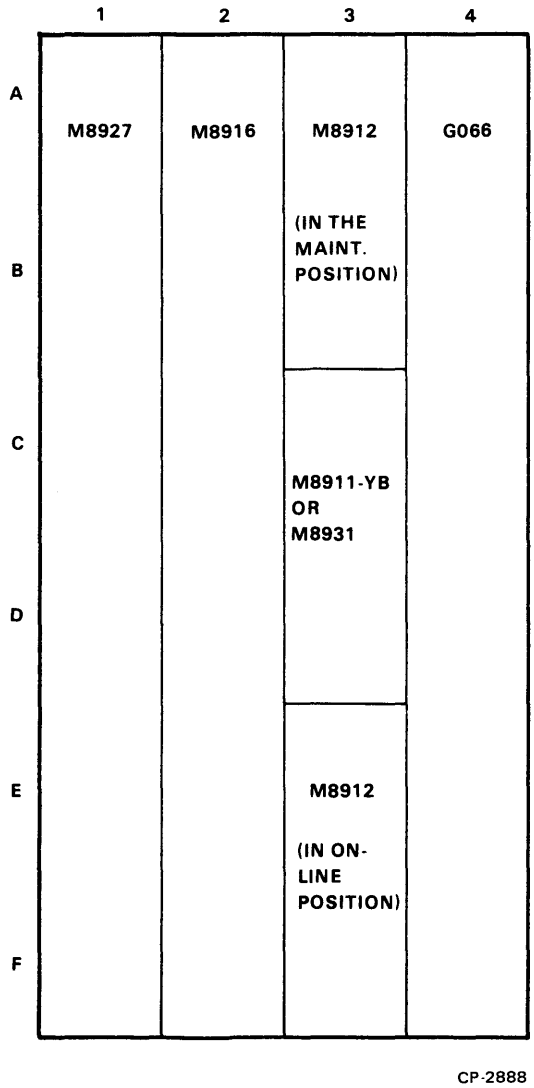
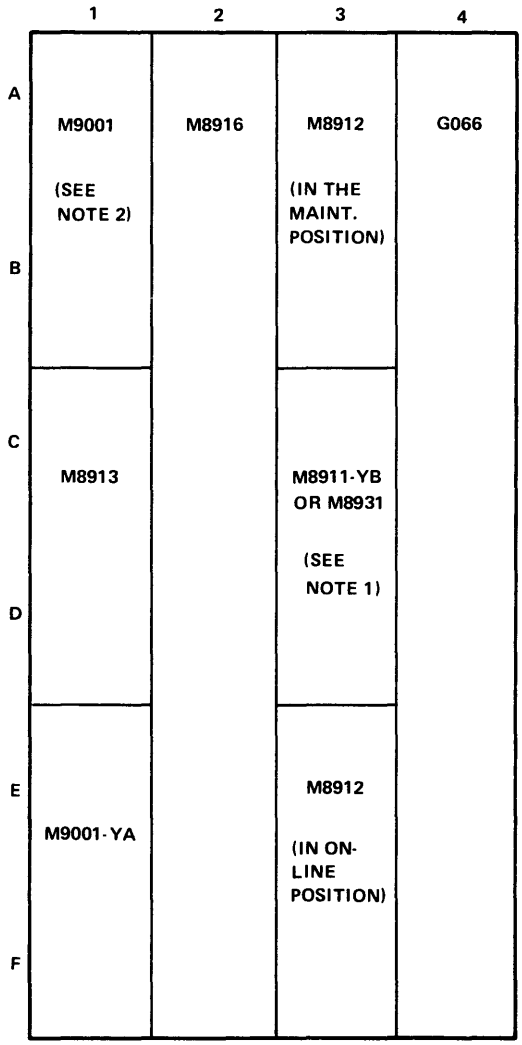


Figure 2-18 TE10N Slave, Module Utilization Diagram



NOTES:

1) Early transport models contain M8911-YB. Later models contain M8931. Either module may be used unless formatter is TM03; TM03 requires M8931.
2) Last TE16 on slave bus requires M9001-YB, M8913-YA and M9001-YC. Later models require M9001, M8913 and M9001-YA in slots A-F01 (inputs) and H8800, H8801 and H8800 terminators on A-F01 output connectors.

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Figure 2-19 TE16, Module Utilization Diagram

The diagnostic programs used in this procedure are:

Data Reliability Test	MAINDEC-11-DZTUA
TE16 BAsic Function Test	MAINDEC-11-DZTUB
TE16/TM02 Logic Test	MAINDEC-11-DZTUC
TE16 Drive Function Timer	MAINDEC-11-DZTUG

Perform the following tests:

1. Run the TE16/TM02 Logic Test (MAINDEC-11-DZTUC) for one complete pass. No errors are allowed. Run the test again with manual intervention.

2. Run the TE16 Basic Function Test (MAINDEC-11-DZTUB) for complete pass. No errors are allowed.

3. Run the TE16 Drive Function Timer Test (MAINDEC-11-DZTUG) for one pass. No out of range errors are allowed.

NOTE

After running this test, tape the teletypewriter (or terminal) printout to the inside of the front access door for future reference.

4. Run the TE16 Data Reliability Test (MAINDEC-11-DZTUA) as follows: Check the DEC-magtape system NRZI mode by running one pass with the following parameters:

```
DENSITY = 3
PARITY = 0
FORMAT = 14
RECORD COUNT = 1
CHARACTER COUNT = 20
PATTERN NUMBER = 1
TAPE MARK = 1
INTERCHANGE READ = 0
SINGLE PASS = 1
STALLS
    READ = 1
    WRITE = 1
    TURN AROUND = 1
```

Run the test with the console switches set to 000720.

A total of two write errors, one soft read forward and one soft read reverse error, are allowed with no hard read errors.

Check the DECmagtape system PE mode by running one (1) pass with the following parameters:

```
DENSITY = 4
PARITY = 0
FORMAT = 14
RECORD COUNT = 1
CHARACTER COUNT = 20
PATTERN NUMBER = 1
TAPE MARK = 1
INTERCHANGE READ = 0
SINGLE PASS = 1
STALLS
    READ = 1
    WRITE = 1
    TURN AROUND = 1
```

Run the test with the console switches set to 000720.

A total of two write errors, one soft read forward error and one (1) soft read reverse error, are allowed with no hard read errors.

2.5.2 TMB11/TE10W/N Acceptance Test Procedure

This section describes the TMB11/TE10W/N acceptance test procedures. When the following tests are complete, the TMB11/TE10W/N is operating correctly.

The diagnostic programs used in this procedure are:

Instruction Test	MAINDEC-11-DZTMA
Drive Function Timer	MAINDEC-11-DZTME
Supplemental Instruction Test	MAINDEC-11-DZTMF
Multidrive Data Reliability Exerciser	MAINDEC-11-DZTMH

Perform the following tests:

1. Run the Instruction test (MAINDEC-11-DZTMA) for one pass, with manual intervention. No errors are allowed.

2. Run the Supplemental Instruction test (MAINDEC-11-DZTMF) for one complete pass. No errors are allowed.

3. Run the Drive Function Timer (MAINDEC-11-DZTME) for one complete pass. No out-of-range errors are allowed.

NOTE

After running this test, tape the teletypewriter (or terminal) printout to the inside of the front access door for future reference.

4. Run the Multidrive Data Reliability Exerciser (MAINDEC-11-DZTMH) for one pass on a 731.6 m (2400 ft) tape with the following parameters:

   DENSITY = 2 or 3 (7- or 9-Track)
   PARITY = 0
   RECORD COUNT = 1
   CHARACTER COUNT = 20
   PATTERN NUMBER = 1
   TAPE MARK = 1
   SINGLE PASS = 1
   STALLS
       READ = 1
       WRITE = 1
       TURN AROUND = 1

   Run the test with the console switches set to 000700.

   A total of two write errors and one soft read error are allowed with no hard read errors.

2.5.3 TM8E/TE10W/N acceptance test procedures

This section describes the TM8E/TE10W/N Acceptance Test Procedure. When the following tests are complete, the TM8E/TU10W/N is operating correctly.

The diagnostic programs used in this procedure are:

Control Test, Part 1	MAINDEC-08-DHTMA
Control Test, Part 2	MAINDEC-08-DHTMB
Drive Function Timer	MAINDEC-08-DHTMC/E
Data Reliability Test (7- or 9-Track)	MAINDEC-08-DHTMD
Random Exerciser Program	MAINDEC-08-DHTMF

Perform the following tests:

1. Run the Control Test, Part 1 (MAINDEC-08-DHTMA) for one complete pass with the switch register set to 4200. No errors are allowed.

2. Run the Control Test, Part 2 (MAINDEC-08-DHTMB) for one complete pass with the "TA←" command. The switch register must be set to 4200. No errors are allowed.

3. Run the Drive Function Timer test (MAINDEC-08-DHTMC) for one complete pass and compare the timing printout with the Time Limit Table in the Diagnostic listing.

NOTE

After running this test, tape the teletypewriter (or terminal) printout to the inside of the front access door for future reference.

4. Run the Data Reliability test, 7- or 9-Track (MAINDEC-08-DHTMD/E) for one complete pass on a 731.6m (2400 ft) tape with the following parameters:

TST	PAT	PAR	DEN	RLS	WMO	RMO
4	7	1	800	2	2	2

Run this test with the console switches set to 1300. A total of two write errors and one soft read error are allowed with no hard read errors.

5. Run the Random Exerciser Program (MAINDEC-08-DHTMF) for one hour, with the switch register set to 0000. No catastrophic errors are allowed.

2.5.4 TC59/TE10W/N Acceptance Test Procedure

This section describes the TC59/TE10W/N Acceptance Test Procedure. When the following tests are complete, the TC59/TE10W/N is operating correctly.

The diagnostic programs used in this procedure are:

Instruction Test	MAINDEC-15-D4A
Drive Function Timer	MAINDEC-15-D4C
Data Reliability Test (7-9-Track)	MAINDEC-15-D4D/E
Random Exerciser Program	MAINDEC-15-D4G

Perform the following tests:

1. Run the Instruction Test (MAINDEC-15-D4A) for one complete pass, with the switch register set to 0002X0, where:

   X = 0 for 7-Track
   X = 4 for 9-Track

   No errors are allowed.

2. Run the Drive Function Timer (MAINDEC-15-D4C) for one complete pass and compare the timing printout with the Time Limit Table in the Diagnostic listing. No out-of-range errors are allowed.

   NOTE
   After running this test, tape the teletypewriter (or terminal) printout to the inside of the front access door for future reference.

3. Run the Data Reliability Test 7- or 9-Track (MAINDEC-15-D4D/E) for one complete pass on a 731.6 m (2400 ft) tape with the following parameters:

TST	PAT	PAR	DEN	RLS	WMO	RMO
4	7	1	8	2	2	2

   Run this test with the console switches set to 050000. A total of two write errors and one soft read error are allowed with no hard read errors.

4. Run the Random Exerciser Program (MAINDEC-15-D4G) for one hour, with the switch register set to 000000. No catastrophic errors are allowed.

CHAPTER 3
OPERATING INSTRUCTIONS

3.1 CONTROLS AND INDICATORS

The operator control box (Figure 3-1) is located at the lower left-hand corner. The functions of the control box switches and indicators are listed in Tables 3-1 and 3-2, respectively. All operator controls are momentary contact switches. Indicators are yellow and red.

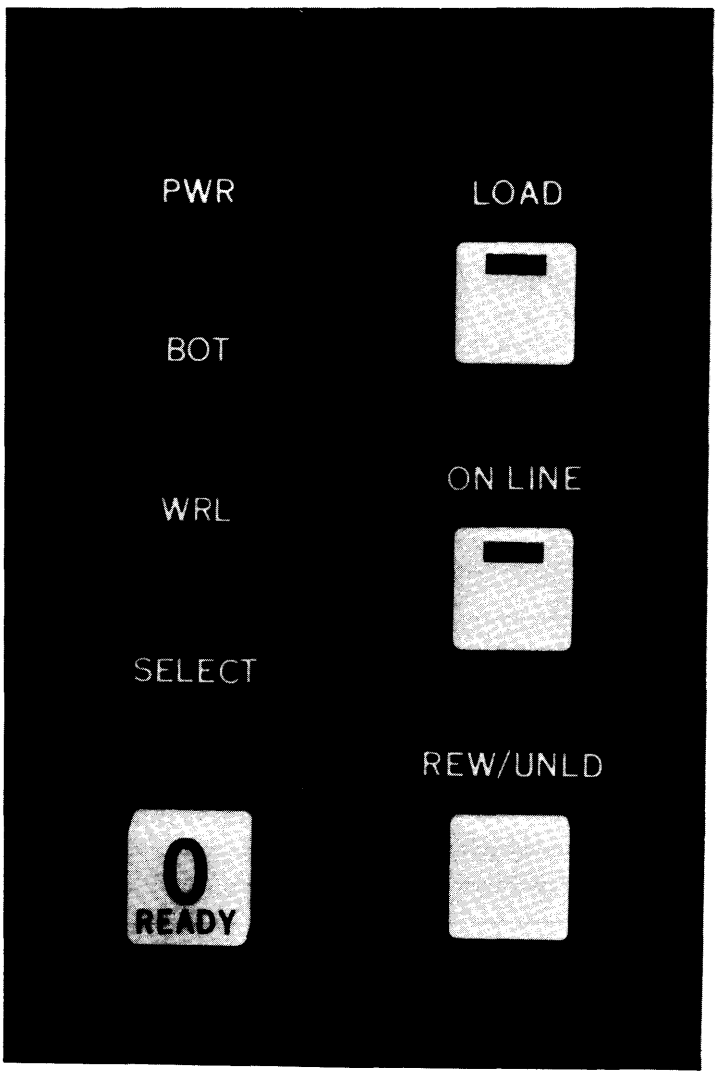

Figure 3-1 Operator Control Box

Table 3-1 TE16 Switch Functions

Switch	Function
LOAD	Pushing this switch, when tape is correctly threaded, causes tape to be pulled into the vacuum columns and the drive to seek the BOT marker and go on-line when it is at rest at BOT. The indicator on this switch glows when tape is in the vacuum columns and proper vacuum has been established. NOTE **A seek-for-BOT sequence consists of five seconds of forward motion, followed by a rewind to BOT.**
ONLINE	Pushing this switch causes the drive to make a transition between the on-line and off-line states. For example, pushing the switch when the drive is off-line causes it to go on-line. This switch is inoperative when the LOAD indicator is off and no LOAD sequence is happening. The indicator on this switch glows when the drive is on-line.
REWIND/ UNLOAD	This switch is inoperative when the drive is on-line. Pushing this switch when the drive is off-line and not at BOT causes the drive to execute a high-speed rewind to BOT. Pushing this switch when the drive is off-line and at BOT causes the drive to execute an UNLOAD sequence, gently winding all tape onto the lower reel. This is not an indicating switch. NOTE **Pushing this switch while the drive is executing a LOAD sequence (LOAD indicator on) and seeking forward for the BOT marker, aborts the LOAD sequence and causes a normal off-line rewind procedure. Never push this switch before the BOT marker is sensed.**

Table 3-2 TE16 Indicators

Indicator	Function
POWER	This indicator glows when ac power has been applied to the device. It is powered by the +5 V regulated supply.
BOT	This indicator glows when the BOT marker is positioned over its sensor.
WRL	This RED indicator glows when either no tape reel is mounted, or a reel is mounted without a write-enable ring.
SELECT	This indicator glows when the drive is both on-line and selected.

3.1.1 Address Selection Plug Receptacle

This receptacle accepts plugs labeled 0 through 7, which define the logical address of the device. If no plug is in the receptacle, the drive cannot be selected. This is not an indicating plug.

3.1.2 Maintenance Aids

Two switches are located under the logic assembly to assist in TE16 maintenance. Both switches are deactivated when the drive is on-line.

1. FWD/REV - The FWD/REV switch determines the direction of tape motion. It does not, however, initiate tape motion.

NOTE

Off-line tape motion may be initiated by the START/STOP switch or by the test function generator (TFG) module.

2. START/STOP - This switch initiates tape motion when moved from the STOP to the START position. It halts tape motion when switched from the START to the STOP position.

3.2 OPERATING PROCEDURES

TE16 operating procedures are described in the following paragraphs.

3.2.1 Application of Power

1. If the 861 power controller REMOTE ON/OFF/LOCAL ON switch is in the REMOTE ON position, TE16 power is controlled by the processor POWER key switch. This method is used in normal operation.

2. If the processor POWER key switch is not activated, TE16 power may be turned on locally by setting the 861 power controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON. This method may be used during maintenance.

3.2.2 Loading and Threading Tape

Use the following procedure to mount and thread magnetic tape.

1. Apply power to the transport. Ensure that the transport is off-line (the ON LINE switch does not glow).

2. Place a write enable ring in the tape reel groove if data is to be written on the tape. Ensure that there is no ring in the groove if data on the tape is not to be erased or written over.

3. Mount the file reel onto the lower hub in the following manner. Release the snap-lock lever on the lower hub by pulling it firmly outward on the rim end. Then, with the reel groove facing away from the operator, mount the file reel onto the lower hub. When the reel is firmly seated against the hub flange (press the reel firmly, but not heavily), close the snap-lock lever on the hub. The file reel is now correctly mounted.

4. Manually unwind tape from the file reel and thread the tape by the tape guides and head assembly as shown in Figure 3-2.

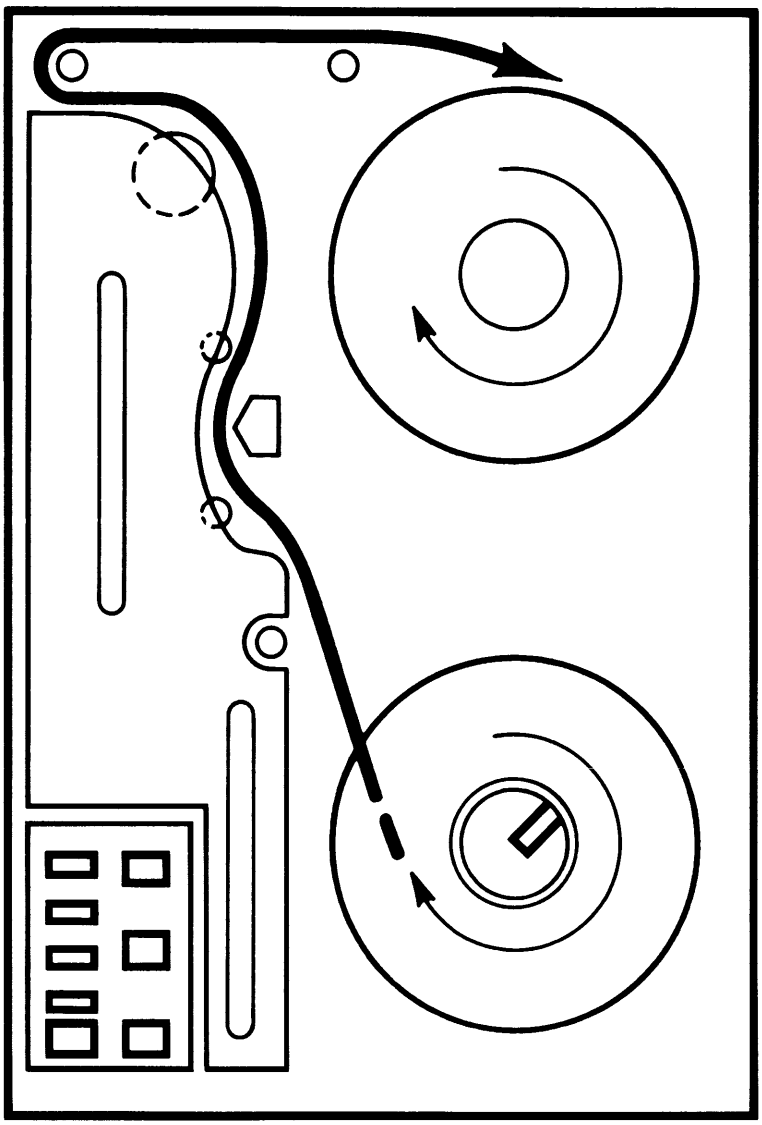

Figure 3-2 Tape Loading Path

5. Wind about four turns of tape onto the take-up reel. Ensure that the tape is in the guides.

CAUTION

Wind tape flat onto the take-up reel. Do not bend tape back or place tape end outside of reel (out the window). While winding tape on take-up reel, simultaneously unwind the file reel to relieve tension on the tape. Rotate the reels gently. Do not jerk the tape, as this could cause the tape to stretch.

6. When the tape is mounted and threaded, press the LOAD button. After a 2-second delay to allow vacuum to be established, tape will be pulled into the vacuum columns and the seek-for-BOT sequence will begin. This sequence consists of 5 seconds of forward tape motion followed by a rewind to BOT. When the BOT marker is sensed, tape motion stops and the transport goes on-line (both the ON LINE switch and BOT indicators glow). The tape is now positioned at the load point (at the BOT marker), and the transport is ready for use.

3.2.3 Unloading Tape

Depending on whether or not tape is at the BOT marker, use one of the following unloading procedures.

3.2.3.1 Tape not at BOT

1. Ensure the transport is off-line.
2. With the transport off-line and the tape not at BOT, press the REWIND/UNLOAD button.
3. The transport executes a high-speed rewind operation. When the BOT marker is sensed, tape motion stops.
4. Press the REWIND/UNLOAD button again. An unload sequence begins, with the tape gently winding onto the lower file reel. When all the tape is on the file reel, tape motion stops.
5. To remove the file reel, unlock the snap-lock lever on the hub and gently pull the reel off.

3.2.3.2 Tape at BOT

1. Ensure the transport is off-line.
2. With the transport off-line and the tape at the BOT marker, press the REWIND/UNLOAD button.
3. The unload sequence begins, with the tape gently winding onto the lower file reel. When all the tape is on the file reel, tape motion stops.
4. To remove the file reel, unlock the snap-lock on the hub and gently pull the reel off.

3.2.4 Restart After Power Failure

In the event of a power failure, the TE16 automatically shuts down and tape motion stops, without physical damage to the tape. However, if the transport was on-line and was either reading or writing at the time of the power failure, the last record should be assumed lost. Refer to the system recovery procedures documentation if this happens. To restart the transport, proceed as follows:

NOTE
Return of power is indicated when the POWER LED glows.

1. Ensure that the TE16 is off-line.

2. Using the top tape reel, manually wind up any loose tape so that it is just snug in the tape loading path (Figure 3-2).

3. Press the LOAD button. This causes the tape to be drawn into the vacuum columns, go forward for five seconds, and rewind to BOT.

3.2.5 Restart After Fail-Safe

If the tape loop in either buffer column exceeds the limit shown in Figure 3-3, the vacuum system automatically shuts down and tape motion stops without damage to the tape. When this fail-safe condition occurs, the TE16 does not respond to either on-line or off-line commands. To restart the transport, follow the procedure listed in Paragraph 3.2.4.

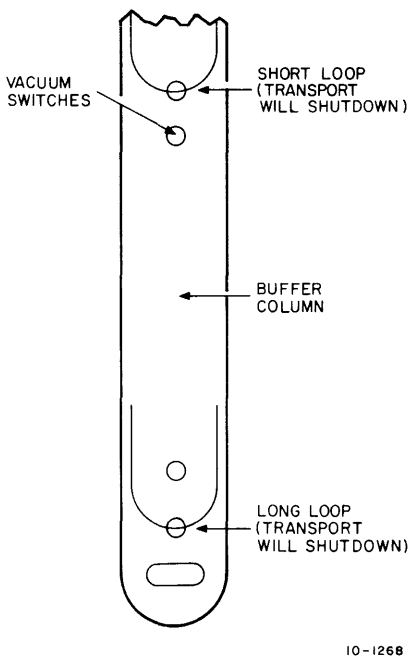

Figure 3-3 Fail-Safe Limits

Before restarting, this failure should be noted in the system log, together with an indication of which fail-safe switch was exceeded and the distance by which it was exceeded.

This information will aid Field Service in preventing a reoccurrence, should the fail-safe condition be due to a tape drive problem.

3.3 OPERATOR TROUBLESHOOTING

Before any maintenance personnel are called to correct a problem, the operator can make several checks with minimal effort. These precautions may isolate an easily correctable error:

1. Ensure that the vacuum door (Figure 1-2) is closed and sealed properly.

2. If the tape does not stop at BOT, be certain the tape has a BOT marker. [The BOT marker is 4.87 m ± 3.05 m (16 ft ± 1 ft) from the beginning of tape.]

3. Ensure that the write enable ring is inserted in the tape reel if a write operation is to be performed.

4. Clean the tape path according to the daily (8-hour) preventive maintenance procedures in Chapter 4, if problems are related to the ability of the drive to read and write.

5. Check the POWER indicator. If it is not glowing, ensure that the 861 power control circuit breaker is on. Also, ensure that the REMOTE/OFF/LOCAL 861 power control switch is in the REMOTE position.

CHAPTER 4
CUSTOMER CARE AND PREVENTIVE MAINTENANCE

4.1 CUSTOMER RESPONSIBILITIES

The customer is directly responsible for:

1. Obtaining operating supplies, including disk cartridges, disk packs and filters, magnetic tape, DECtape, paper tape, cassettes, printer paper, printer ribbons, plotter paper, etc.

2. Supplying accessories, including disk storage racks, DECtape storage racks, carrying cases for disk cartridges and DECtape, cabinetry, tables, and chairs.

3. Maintaining the required logs and report files consistently and accurately.

4. Making the necessary documentation available in a location convenient to the system.

5. Keeping the exterior of the system and the surrounding area clean.

6. Turning off the teletypewriter and/or line printer when these devices are not in use.

7. Ensuring that ac plugs are securely plugged in each time equipment is used.

8. Performing the specific equipment care operations described in Paragraphs 4.2 and 4.3 at the suggested periods or more often if usage and environment warrant.

4.2 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; keeping tape clean is imperative.

2. Always store tape reels inside containers when the tape is not in use; keep the empty containers tightly closed to keep out dust and dirt.

3. Never touch the portion of tape between the BOT and EOT markers; oil from fingers attracts dust and dirt.

4. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and could have an adverse effect on tape transport reliability.

5. Always handle tape reels by the hub hole; squeezing the reel flanges could lead to tape edge damage in winding or unwinding tapes.

6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.

7. Do not place magnetic tape near any line printer or other device that produces paper dust.

8. Do not place magnetic tape on top of the tape transport or in any other location where it might be affected by hot air.

9. Do not store magnetic tape in the vicinity of electric motors.

4.3 CUSTOMER PREVENTIVE MAINTENANCE

Digital Equipment Corporation tape transports are highly reliable precision instruments that will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The following information will assist the customer in caring for his equipment and ensure the highest level of performance and reliability.

4.3.1 Preventive Maintenance

To ensure trouble-free operation, a preventive maintenance schedule should be kept. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is very important to proper tape transport operation. The frequency of maintenance will vary somewhat with the environment and degree of use of the transport. Therefore, a rigid schedule applying to all machines is difficult to define. Daily cleaning is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Paragraph 4.3.3 contains the cleaning instructions.

Before performing any cleaning operation, remove the file reel and store it properly. All items in the tape path should be cleaned on a daily basis. In cleaning, be thorough, yet gentle.

CAUTION

Do not use acetone or lacquer thinner, rubbing alcohol, trichlorethane, or excessive cleaner. Isopropyl alcohol (91%) is an acceptable cleaning agent. Be extremely careful not to allow any cleaner to penetrate to ball bearings and motors.

4.3.2 Magnetic Tape Drive Cleaning Kit

A magnetic tape drive cleaning kit (TUC01) has been carefully configured to provide cleaning materials that will not harm tape equipment and will not leave any residue behind to interfere with data reliability. The hints contained in the following few paragraphs will ensure that the very best results possible will be obtained from the kit.

The cleaning fluid in this kit is one of the best cleaners available. To ready the can of fluid for service, unscrew the top and punch a small hole in the metal seal covering the pour spout.

WARNING

When using DECmagtape cleaning fluid, avoid excessive skin contact. Do not allow it to come in contact with the eyes, and do not swallow it. Use cleaning fluid only in a well ventilated area.

When cleaning tape equipment, never dip a dirty cleaning swab or wipe into the can. To transfer fluid onto the swab, pour a little out into the screw cap and dip the swab into the cap. Discard the remaining fluid when the cleaning operation is complete.

Always keep the can of fluid tightly closed when not in use, because the fluid evaporates rapidly when exposed to air.

Use the cleaning materials contained in the kit to clean tape heads, tape guides, the tape cleaner, reel hubs, and any part of the drive where a dirty residue could ultimately come in contact with tape. To clean other parts of the drive, such as the exterior surfaces of doors, use any reasonably clean, lint-free material with or without cleaning fluid.

NOTE

An unusually stubborn dirt deposit that appears to resist cleaner may require mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with cleaning fluid to remove soapy residues.

4.3.3 Cleaning the TE16 DECmagtape Drive

1. Remove the tape reel from the unit.

2. Clean the following components of the drive using a foam-tipped swab soaked in cleaning fluid (Figure 4-1).

   a. Read/write head (Location A)
   b. Erase head (Location B)
   c. Tape cleaner (Location C)
   d. Upper left-hand roller guide (Location D)
   e. Lower roller guide (Location E)
   f. Upper middle roller guide (Location H)

NOTE

Be careful to keep cleaning fluid only on the tape-bearing surface of roller guides to prevent degreasing the roller guide bearings.

3. When cleaning the head area, avoid the spring-loaded ceramic washers on the tape drive assemblies. If it appears necessary to run the swab over the tape bearing surface of these guides to remove oxide deposits, do so; however, when cleaning is completed, be sure that the washer is pressed snugly up against the tape guide surface and not "hung up" on its shaft (Figure 4-2).

4. Next, clean the vacuum pockets (F), the inner surface of the vacuum door (G), and the rubber capstan wheel (J), using a lint-free wipe and cleaning fluid. Pass another lint-free wipe over the head using a polishing action to remove any remaining deposits.

5. Use a dry wipe to clean the reel-contacting metal surfaces of the lower hub. Dirt on these surfaces may result in slippage of the tape reel.

6. Inspect upper reel tape-contacting surfaces. If the surfaces are dirty, clean them using a swab or wipe moistened in cleaning fluid.

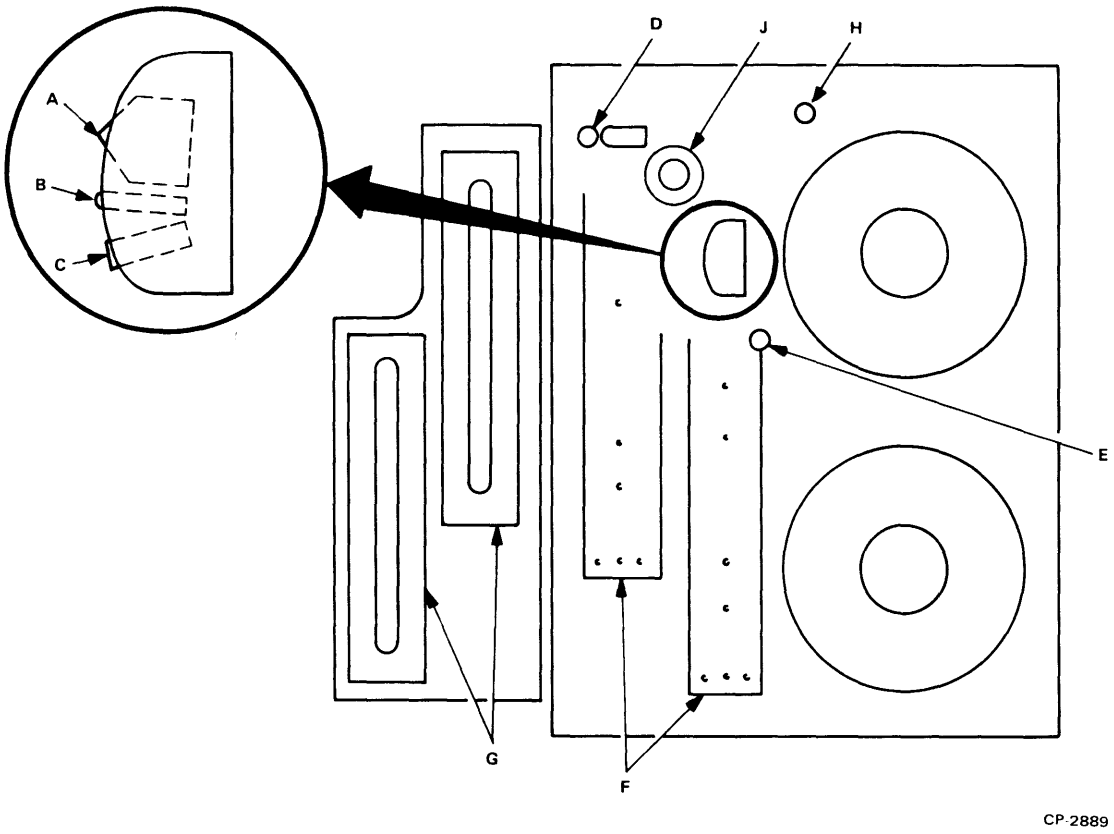

Figure 4-1 Location of Read/Write and Erase Heads and Tape Cleaner

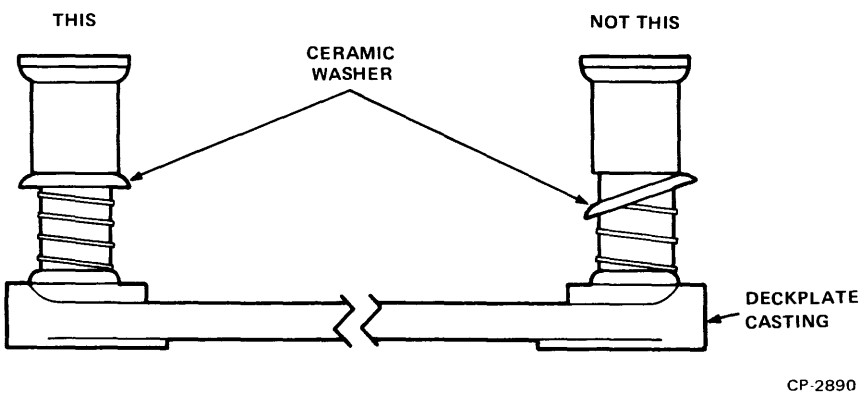

Figure 4-2 Proper Ceramic Washer Positioning

CHAPTER 5
THEORY OF OPERATION

5.1 INTRODUCTION

This chapter is divided into five main sections: Introduction, Functional Theory of Operation, Detailed Circuit Descriptions, Write Circuitry, and Read Circuitry.

The Introduction references a basic block diagram to briefly describe TE16 system operation. Major TE16 operations are detailed in a functional format in the second section. Block and flow diagrams detail entire operations from the application of power through tape buffering, power supply operation, and the read/write action.

The third section provides a unit level discussion of each TE16 module. Included in this section are descriptions of the M8926 and M8927 interface modules that are used to permit the TE16 to be used in many different system configurations. The discussion references and identifies functional components of each drawing of the print set. The reader may then use these detailed logic descriptions with the more basic functional diagrams in the previous section to gain an overall understanding of the TE16.

The use of circuit schematic mnemonics prefacing signal names is exhibited throughout this chapter. These mnemonics inform the reader where the signal originates. For example, signal LAW3 RELAY ENABLE L originates on the third sheet of the Logic and Write (LAW) circuit schematics and the TMD1 HI FREQ CLOCK (1) H signal originates on the first sheet of the Tape Motion Daughter (TMD) circuit schematics.

Completing this chapter are detailed explanations of PE and NRZI read and write circuitry operation. Flow and timing diagrams complement this section.

All references to the TE16 imply the TE10W/N options inclusively, unless otherwise specified.

5.1.1 Basic Description

This section outlines the manner in which a programmer's commands are transmitted to the TE16. It is presented to provide a background for the controller-transport interaction, which is described in greater detail in later sections of this chapter.

Figure 5-1 is a functional block diagram of the TE16 DECmagtape transport. The processor initiates a controller/TE16 operation by addressing the controller registers by way of an address decoder and loading the operation parameters into the registers. The processor specifies an out transfer (with respect to itself), causing a select out signal to be asserted for the particular register addressed. As each register is selected, the processor places the appropriate data on its data lines, which is then loaded into the register with a strobe pulse. Thus, the command register receives the type of operation to be performed, the byte-record count register receives the number of bytes to be transferred, and the current memory address register receives the memory address of the first byte to be transferred.

The controller command logic selects which transport is to be involved in the transfer and supplies a function command to the command decoder, which generates the required commands for the tape transport. When the start logic senses that the tape transport has been selected and is ready, it asserts a SET pulse to the interface logic. This asserts the SLAVE SET PULSE signal to the TE16, starting the operation. If a read, write, or space forward operation is commanded, the transport command logic asserts FOR to the tape drive system, which drives the capstan servo and starts the tape moving forward.

If a write command is in progress, the controller counts a delay that is long enough to allow the tape to come up to speed and then notifies the transport via the ACCL signal. The drive sends WRT CLK pulses to the interface write channels, and writing of the data character begins. A WRITE command signal from the controller enables the write channels, which transfer the write data from the controller to the write heads in the transport. The controller write channel logic produces REC pulses, which record the data characters on tape via the write heads. A parity bit is generated for each character and is recorded on tape along with the character. When a transfer completes, the controller byte/record counter is incremented, and the controller prepares for another transfer. When the byte/record counter senses that the desired number of bytes has been transferred (i.e., written), it notifies the interface write logic to write the end of record characters (NRZI mode) or the postamble (PE mode).

Typically, the interface read logic is enabled during a write operation and reads each character approximately 3 ms after it is written. The read heads are displaced from the write heads by 3.8 mm (0.15 inches). Thus, depending on density, 30 to 240 characters are written between the time a given character is written and the time it is read back.

The controller error logic monitors transport status, including parity and other data related errors and asserts an error signal to the done logic if an error condition exists. Some types of errors warrant terminating an operation before it is completed, while others wait until the end of the operation before asserting an error signal.

If a read operation is in progress, the RD0 - RD7 read data is gated to the controller data buffer register, where it is loaded into the register. When the end of the operation is detected, the motion control logic loads a post-operation delay code into the operation timing logic. When the post-operation delay is complete, the controller asserts STOP to halt tape motion. For detailed information relative to processor or controller functions during read/write operations, refer to the correct processor and controller manuals.

The processor can read the controller registers by addressing them and requesting an in-transfer, with respect to the processor. The address decoder then asserts select in for the particular register selected, which gates the register bits out to a data bus through a register select output multiplexer.

The slave bus signals (Figure 5-1) are listed and described in Table 5-1.

5.2 FUNCTIONAL THEORY OF OPERATION

This section provides the reader with a general overview of the TE16 in its various modes of operation. Stress is placed on exhibiting all major components that are necessary to the operation under study and on the major signal lines that interface those components. No attempt is made in this section to explain the operation of any particular circuit. Such explanations are located in Paragraph 5.3, where each TE16 module is divided into its major subsections and analyzed.

When troubleshooting, this section of the TE16 Maintenance Manual should be used as an aid in narrowing the area of search for a problem cause. Chapter 6 should then be referenced for more explicit information about the suspected problem area, whether it is a module or a power supply.

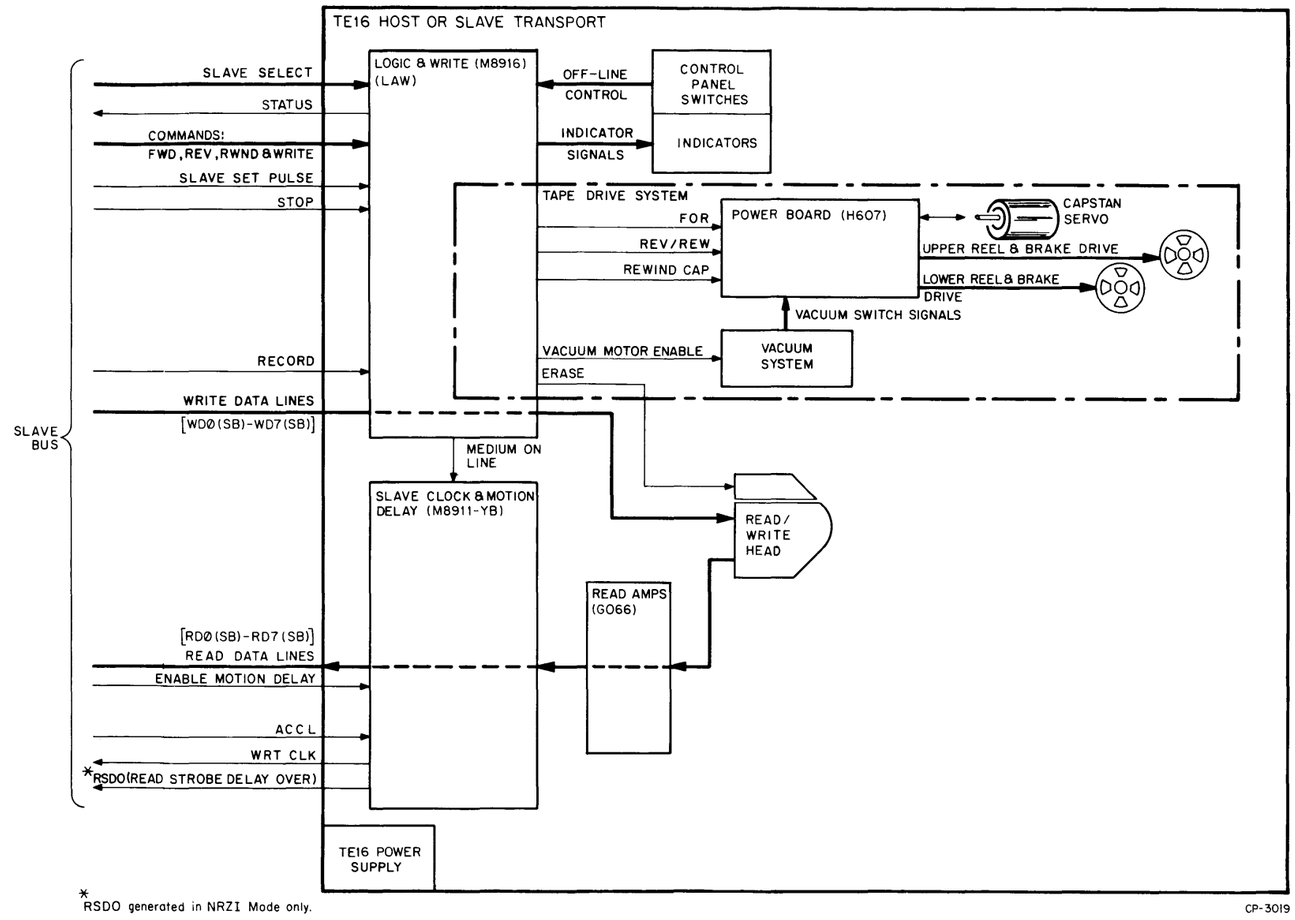

Figure 5-1 TE16 Functional Block Diagram

Table 5-1 Slave Bus Interface Signals

Slave Bus Signal	Function
Slave Select [SS(0:2)]	These lines select one out of eight possible TE16 Transports for command execution.
Forward (FWD) Reverse (REV) Rewind (RWND) Write Enable (WRITE)	These are the four command lines that determine TE16 operation.
Slave Set Pulse (SLAVE SET PLS)	This signal initiates TE16 response to the four command lines.
Stop (STOP)	This signal causes the TE16 to terminate motion. (Does not apply to rewind, which terminates independently.) Must be negated before assertion of the SET Pulse.
Enable Motion Delay (EMD)	This signal enables the TE16 to gate out a coded motion delay preset onto the read lines.
Accelerate (ACCL)	Asserted by the controller while the transport is getting up to speed or not moving tape. Not asserted while the Identification Burst (IDB) is being written.
Write Data [WD(0:7,P)]	These nine lines transmit data to be written by the TE16.
Record (REC)	A pulse that causes data to be written on tape.
Density Select [DEN(0:2)]	These three lines control the density at which data is written on tape. They must also represent the density of tape data during a read operation. **DEN 2 DEN 1 DEN 0 BPI** 0 0 0 200 } TE10 } TE16 0 0 0 556 0 1 0/1 800 1 0 0 1600
Clock (CLOCK)	A 144-kHz clock, generated in the TE16, present at all times when the unit is on-line.
Write Clock (WRT CLK)	This clock is transmitted to the controller by a powered, on-line TE16 loaded with tape when it is running at speed (ACCL not asserted). The frequency of WRT CLK is a function of the DEN lines and controls the write timing frequency.
LRC Strobe (LRC STRB)	Asserted by the interface logic prior to the REC pulse that writes the LRC character.
Read Data [RD(0:7,P)]	These nine lines transmit read data from the TE16 to the controller. (They also transmit the motion delay preset.)
Read Strobe Delay Over (RSDO)	A read strobe pulse generated by the transport at the end of the skew delay in NRZI mode.

Table 5-1 Slave Bus Interface Signals (Cont)

Slave Bus Signal	Function
Set Vertical Parity Error* (SET VPE)	Asserted by the TE16 during a write or interchange read operation when data violates the skew window.
Beginning of Tape (BOT)	Asserted when the TE16 detects the BOT marker.
End of Tape (EOT)	Asserted when the TE16 detects the EOT marker.
Rewind Status (RWS)	Asserted while the selected TE16 is performing a rewind opertion.
7-Channel (7 CH)	Always negated by a selected TE16 or 9-track TE10. Always present for a 7-track TE10.
Slave Present (SPR)*	Asserted by a selected, powered TE16.
Medium On-Line (MOL)	Asserted by a selected, powered TE16 that is loaded with tape.
Tape Unit Read (TUR)	Asserted by a selected TE16 to indicate that tape motion has stopped.
Settle Down (SDWN)	Asserted while the transport is decelerating, until it has stopped.
Phase Encoded Status (PES)*	Asserted by a TE16 when instructed to operate in PE mode (DEN 2 asserted).
Slave Attention (SLA)*	Asserted by a TE16 when it comes on-line.
Set Slave Status Change (SET SSC)*	Asserted at the completion of a rewind or when the unit comes on-line. It is also pulsed when the transport goes off-line or when the TE16 power fails. This line may be asserted by any slave, selected or not.
Write Lock (WRL)	Asserted when the selected TE16 detects that the write enable ring has been removed from the tape reel.
Interchange Read (IRD)*	A maintenance function. When asserted in NRZI mode, skew delays are tightened; in PE mode, a low read threshold is used.
Drive Type (DT)*	In the TEl6, these three bits are always asserted as follows: DT0 1 DT1 0 DT2 0

*TE16/TM02 configuration only.

Table 5-1 Slave Bus Interface Signals (Cont)

Slave Bus Signal	Function
Serial Number [SN(0:15)]*	These 16 lines contain the BCD code of the last four digits of the serial number of the selected TE16.
Drive Clear Pulse (DRV CLR PLS)*	When asserted by the controller, DRV CLR PLS clears SLA in the selected slave.
Initialize Pulse (INIT PLS)*	When asserted by the controller, INIT PLS L clears SLA in all on-line transports.
+5 V	The controller supplies this voltage to power the slave bus terminator networks.

*TE16/TM02 configuration only.

5.2.1 Tape Loading

Elements shown in Figure 5-2 illustrate key events in a loading sequence. With the transport in the unloaded state, the 5412242 regulator board supplies the following voltages:

1. +5 Vdc is supplied to the M8916. It is distributed on the M8916 to both the control panel (via the M8916-control panel connecting cable) and the H607 daughter board. The daughter board then distributes +5 Vdc to the mother board via the mother-daughter cable.

2. +17 Vdc, -17 Vdc, and COMMON are supplied to the brake control circuitry via the power harness connecting the 5412242 and the mother board.

3. +16 Vdc, -16 Vdc, and COMMON are supplied to the capstan control circuitry via the same power harness mentioned in step 2.

4. - 17 Vdc and COMMON are supplied to the reel motor circuitry. +17 Vdc is not present until the relay is energized.

When the LOAD switch on the control panel is depressed and released, the CTRL 1 LOAD SW L signal asserts and then returns to the negated state upon release of the switch. The trailing edge of this signal initiates the load sequence by setting the RELAY ENABLE flip-flop. Both LAW3 RELAY ENABLE H and LAW3 RELAY ENABLE L are then transmitted from the M8916 to the H607 daughter board.

LAW3 RELAY ENABLE L simply passes through the daughter board, travels to the mother board (via the mother–daughter cable), and finally to the 5412242 board along the power harness connecting the mother board to the 5412242.

Once LAW3 RELAY ENABLE L reaches the power board, it energizes the relay, causing it to pull in with an audible click. The relay contacts then make available the following voltages:

1. 115 Vac is supplied to the vacuum motor assembly. (For 230 Vac units, the transformer is used as an autotransformer to step 230 Vac down to 115 Vac.)

2. +17 V INTERRUPT is supplied to the mother board, thus powering the reel motor driver circuits.

3. POWER COMMON INTERRUPT is supplied to the capstan motor, providing a return path for capstan motor current.

Signal LAW3 RELAY ENABLE H is transmitted to the H607 daughter board, where it triggers a circuit that delays for 2 seconds and then (if either lower fail-safe switch is still open) provides a 70 ms pulse, TMD2 LOAD PULSE l, to the H607 mother board. Note that the LOWER FAIL SAFE H signal is transmitted to the M8916 via a back panel connector and is passed through the M8916 and over to the H607 daughter board.

The TMD2 LOAD PULSE signal causes both reel motors to dump small loops of tape, sealing off both vacuum columns. Once this occurs, vacuum is established in both columns, closing the lower fail-safe switches. Closing these switches results in negation of LOWER FAIL SAFE H and, 100 ms later, the assertion of LAW3 REEL MOTOR ENABLE (0) L. This signal passes through the H607 daughter board to the H607 mother board and enables the reel motor driver circuits there. At this time, the reel motor control circuitry (distributed between the H607 mother and daughter boards) acts to position both left and right hand loops between the vacuum sensing control switches.

Finally, approximately 4 seconds after the LOAD switch is pushed, the LAW3 LOAD LED signal is pulled low by circuitry on the M8916 and the front panel LOAD indicator glows.

If a failure had occurred during the loading sequence, circuitry on the M8916 that senses both the upper fail-safe and lower fail-safe switches would have been enabled at the 4-second time. Detection of failure clears the RELAY ENABLE flip-flop, thus opening the relay on the 5412242 power board.

5.2.2 Reel Motor and Brake Control

This discussion illustrates the mechanism by which tape loops are maintained in the buffer columns throughout all modes of tape motion. Figure 5-3 shows all modules, supply voltages, and major signals involved in this mechanism.

The heart of the loop control system is the H607 daughter module (5412262). Inputs to this module consist of the three motion commands (LAW3 FOR H, REV/REW H, and REWIND CAP H) and four vacuum-sensing switch outputs. The signal LAW3 REEL MOTOR ENABLE L is also input to the logic module but, as it is not utilized there, passes directly through to the power module. For a description of the manner in which the three motion signals are generated, refer to Paragraph 5.2.3 for a tape motion outline and Paragraph 5.3.6 for detail.

The H607 logic board uses the direction and magnitude of tape motion, together with the information provided by the vacuum-sensing switches, to determine appropriate times for brake and motor actuation. The left-hand vacuum column switches control the upper motor and brake, while the right-hand switches control the lower reel motor and brake. The upper and lower reel motors use completely independent circuits, simplifying diagnosis of problems in this area.

The major outputs of the H607 module are two brake control signals and four reel motor direction control signals. These signals are used to control the power driver circuits controlling the brakes and motors.

Note that +16 V and -16 V are not required to provide power for the reel motor and brake circuits. However, in case of a failure in the ±17 V power, diodes on the H607 (not shown in the figure) can bleed power from the +16 V power line to allow brake actuation. While it is not apparent from the diagram, the drivers for the brake circuits run from +17 Vdc, while the reel motor drive circuits utilize -17 V and +17 V INTERRUPT. Thus, the RELAY ENABLE signal must energize the relay on the 5412242 regulator board before the reel motors can be energized.

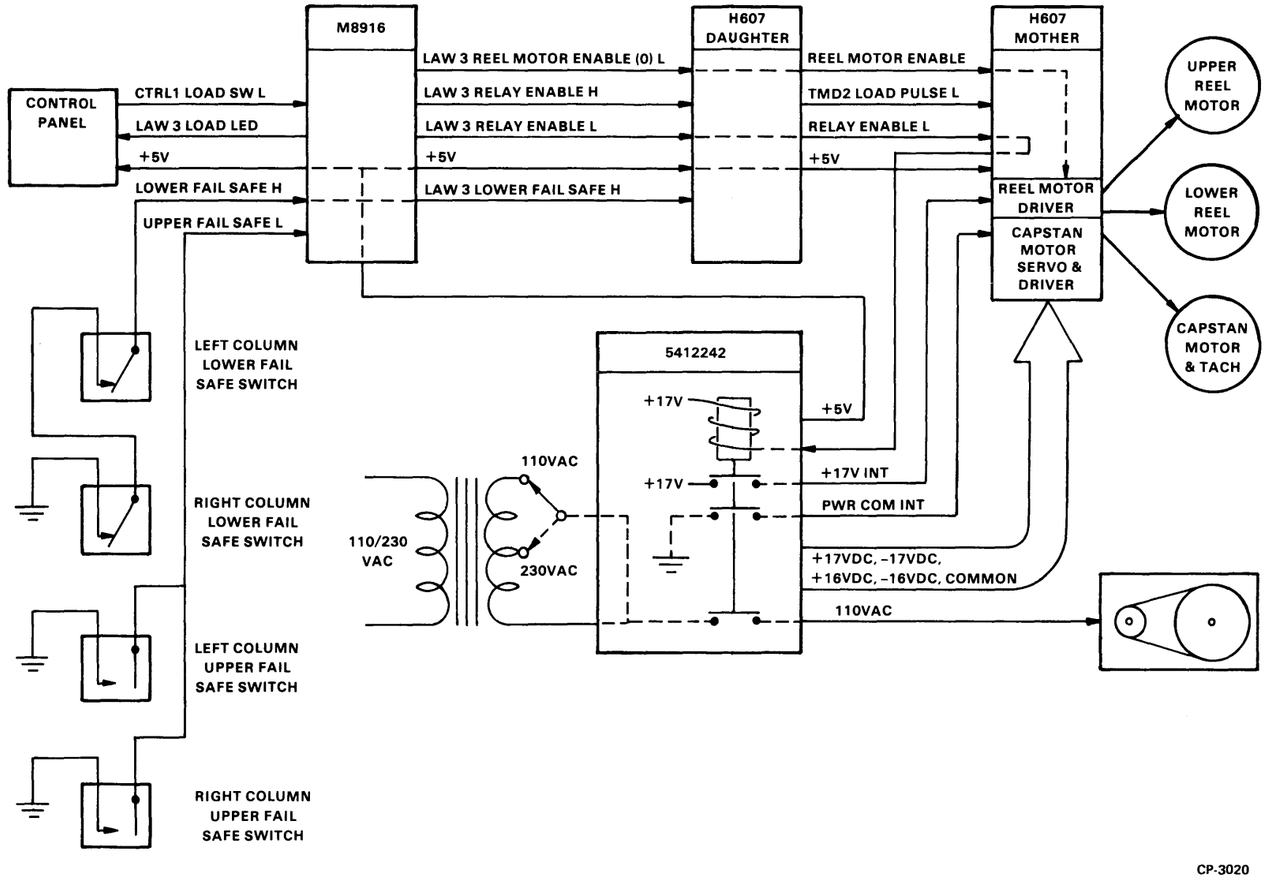

Figure 5-2 Tape Loading Functional Block Diagram

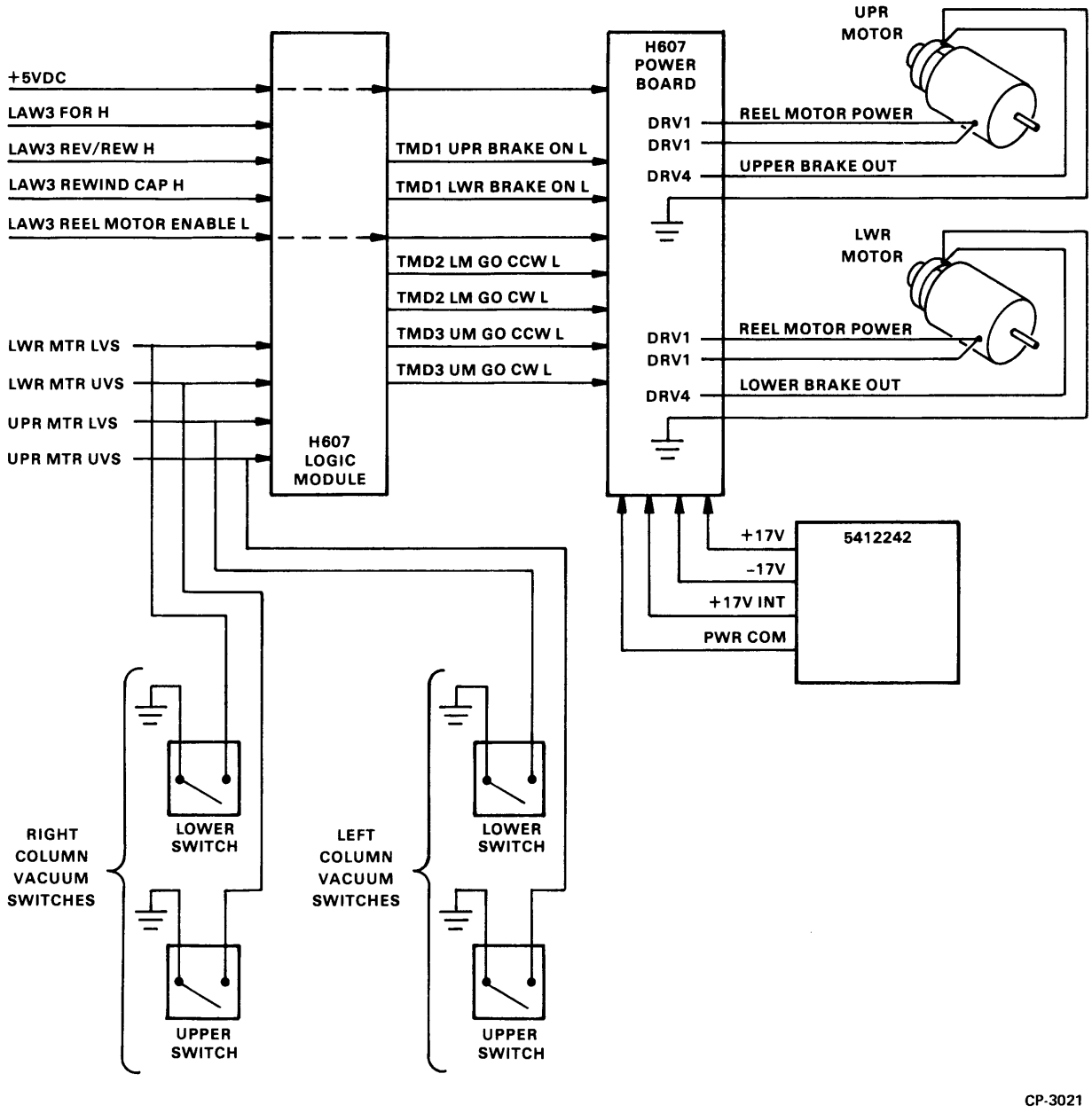

Figure 5-3 Reel Motor and Brake Control Functional Block Diagram

5.2.3 TE16 Capstan Motion

This discussion illustrates and describes the mechanism by which tape motion is initiated and shows all modules, supply voltages, and major signals involved in tape motion. Refer to Figure 5-4 while reading this section.

To begin, tape motion can be initiated through two major signal groups: an on-line group and an off-line group. The on-line signal group consists of five major signals. In order for the drive to respond to this group of signals, it must be both on-line and selected. The signal SBUS1 STOP (SB) L is an overriding command and, when asserted, prevents all tape motion. The set pulse [SBUS1 SLAVE SET PULSE (SB) L] is used to load a motion command into the TE16. The controller must negate STOP before asserting SET PULSE to the TE16. The three remaining command signals, SBUS2 FOR (SB) L, SBUS2 REV (SB) L, and SBUS2 REWIND (SB) L, define the direction and speed of tape motion requested by the SET PULSE. The controller must assert only one of these command lines when requesting tape motion.

The off-line signal group used to initiate tape motion consists of seven signals. The drive must be off-line in order for it to respond to any of these signals. Off-line rewinds can be initiated only by the REW/UNLOAD switch, which is located on the TE16 front panel. Note that this switch requires +5 Vdc to power its Hall-effect closure mechanisms. Off-line operation at 1.14 m/s (45 in/s) is controlled by the remaining six signals. The TE16 maintenance panel (located under the logic chassis) is the source for four of these signals, while the M8912 test function generator module supplies the remaining two.

The FORWARD/REVERSE switch on the maintenance panel defines the direction for all off-line operation at 1.14 m/s (45 in/s). The START/STOP switch is used to initiate and halt tape motion.

When the M8912 is inserted in slots A/B 03 of the TE16, use of the STOP/START READ and STOP/START WRITE switches results in generation of the signals TFG3 FIRST ONE SHOT L and TFG3 FOURTH ONE SHOT L. These signals have the same effect as flicking the STOP/START maintenance switch from side to side.

The drive "jogs" in the direction indicated by the FORWARD/REVERSE maintenance switch.

5.2.3.1 Capstan Motion Control - Once a motion command has been loaded into the TE16, the command is processed on the M8916 Logic and Write module. The M8916 then asserts the appropriate command lines to the capstan motor circuitry: LAW3 FOR H, REV/REW H, and REWIND CAP H are transmitted to the H607 logic board via the flat cable connecting the M8916 to the logic board. These signals are simply passed through the logic board to the H607 power board via the interconnecting cable. Logic power travels along this same path to supply the integrated circuits used in the first stage of the capstan motor control circuitry.

The last stage of capstan power drivers applies current to the capstan motor. Note that the return path for this current passes through the H607 and terminates on the 5412242 power regulator module at the relay on that board. As a result, the capstan motor will not move unless the RELAY ENABLE signal is asserted. This signal energizes the relay, applying POWER COMMON INTERRUPT to the capstan motor return lead and allowing the "push-pull" power driver circuit to direct the flow of current to the capstan motor.

As the capstan motor turns, the tachometer attached to it generates the CAPSTAN TACH VOLTAGE signal, a voltage proportional to motor speed. This voltage is applied to the capstan servo circuitry and is used to regulate motor speed.

For more information on the signal processing mentioned here, refer to the detailed logic descriptions for the module or modules in question.

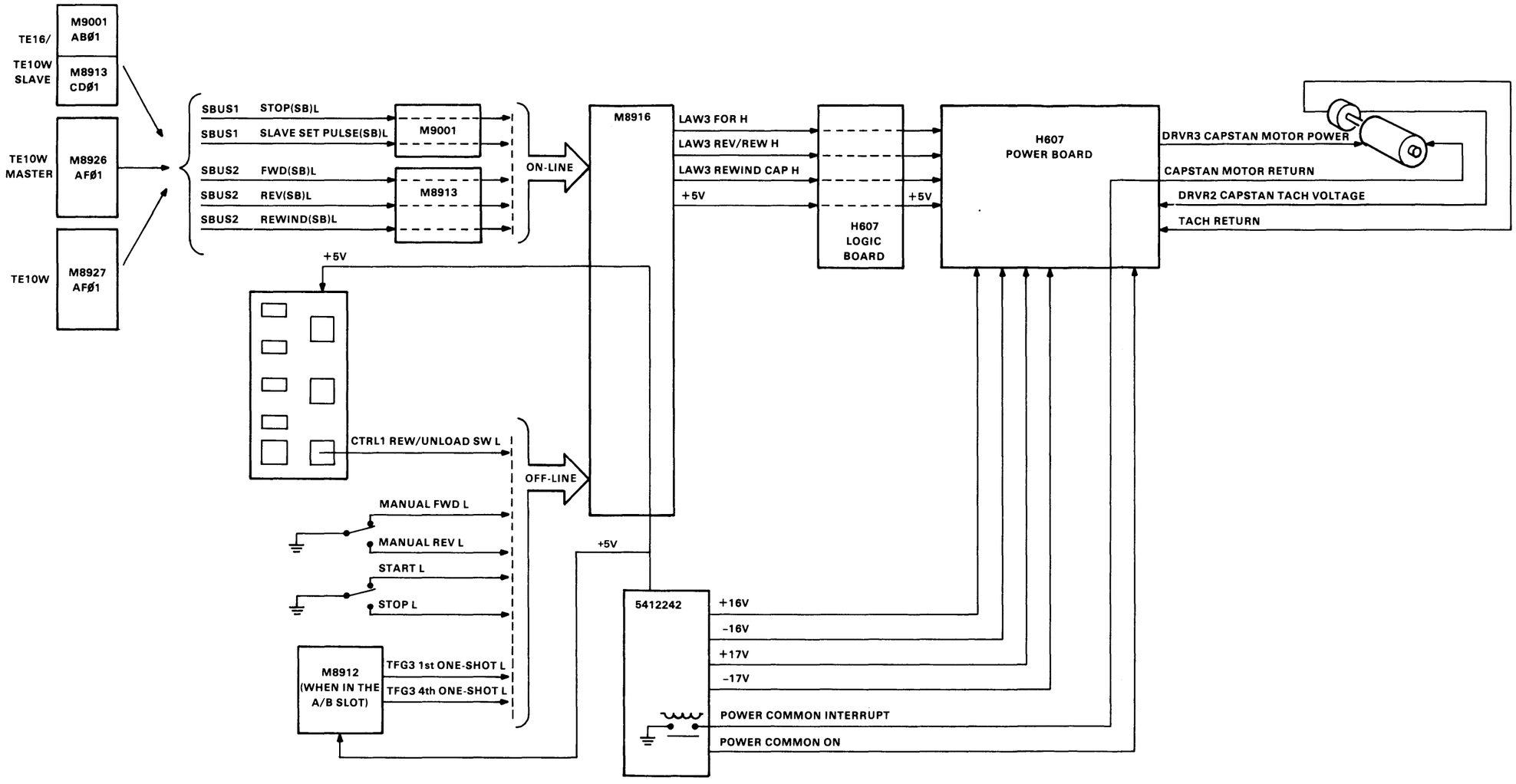

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Figure 5-4 CAPSTAN Motion Functional Block Diagram

5.2.4 TE16 Read/Write Data Paths

As with all other major transport functions, the TE16 can write data on tape under either direct program control or off-line test control. This section outlines the data paths utilized in both on-line and off-line write operations and traces the flow of data onto tape and back through the read recovery chain. The read recovery scheme is identical to that of a normal read operation. Refer to Figure 5-5 while reading this section.

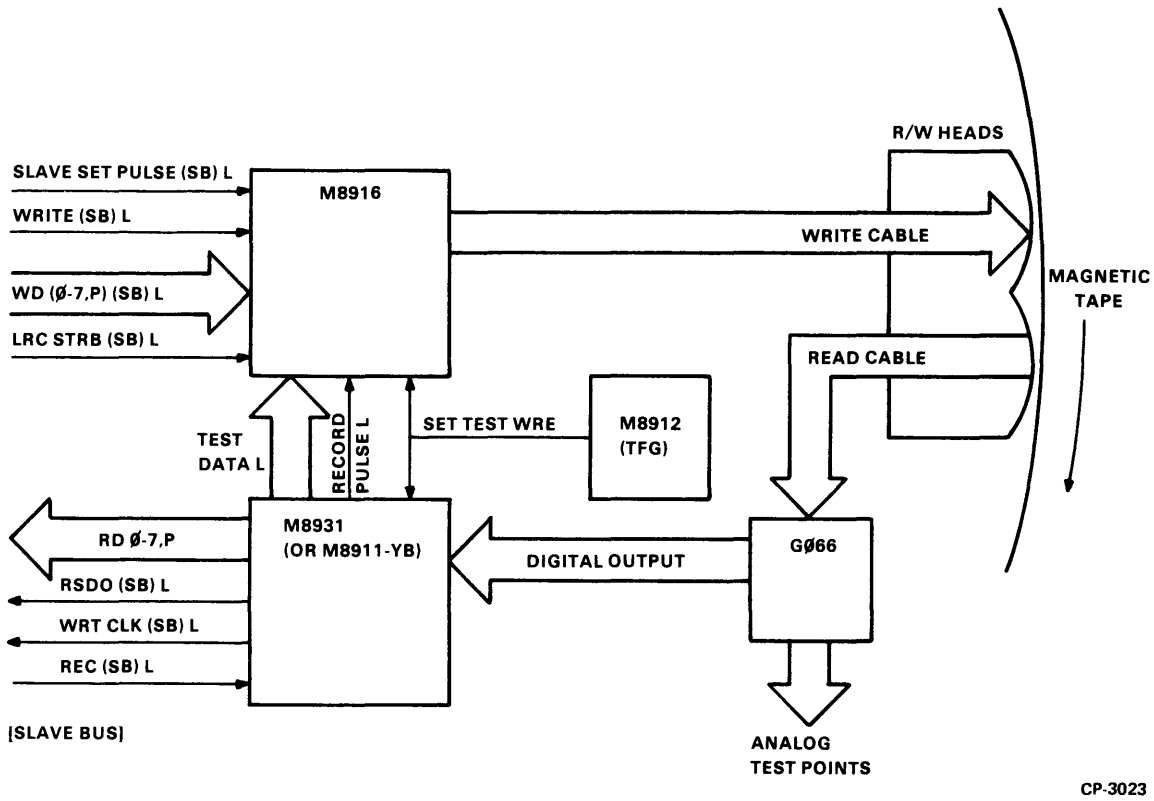


Figure 5-5 Read/Write Functional Block Diagram

5.2.4.1 On-Line Writing – A controller uses only four signals to control TE16 writing. First, the DEN 2 (SB) L signal (not shown in Figure 5-5) is used to determine whether the TE16 will operate in NRZI or PE Mode. (Operation of the write buffer on the M8916 LAW module is dependent upon the mode in which the TE16 operates. In particular, when in PE Mode, one of the major write control signals, LRC STRB (SB) L, is ignored.) Once the operating mode has been chosen, the controller commands the TE16 to write on tape by asserting WRITE (SB) L and strobing this signal with SLAVE SET PLS (SB) L. Next, the controller uses the WRT CLOCK (SB) L signal (generated by M8911) to assert write strobes [REC (SB) L] and transmits these REC pulses to the TE16. REC (SB) L pulses are received on the M8931 (or M9811-YB) module and then transmitted to the M8916 logic and write module.

In NRZI operation, the signal LRC STRB (SB) L is used to write the LRC character on tape. All other data, including cyclical redundancy check (CRC) data is carried on the WD lines.

5.2.4.2 Off-Line Writing – In off-line test mode, the M8912 test function generator module is inserted in slot A/B 03. In this mode, the STOP/START WRITE and WRITE switches on the M8912 module can be used to generate a signal called SET TEST WRE. This signal is transmitted to the M8931 (or M8911-YB), where it results in automatic generation of RECORD PULSEs, which are then transmitted to the M8916 in a manner identical to that of an on-line write operation. Generation of LRC STRB signals in off-line mode is not possible. Signal SET TEST WRE L is also transmitted to the M8916, where it turns on the write circuits.

5.2.4.3 Common Write Data Path – Once RECORD PULSEs have been generated, they are transmitted to the write buffer. Here, data is processed in a fashion that is dependent upon the mode selected. In PE mode, the data contained on the WD lines (test data lines in off-line writing) is simply clocked into the write buffer. In NRZI mode, the write buffer is used to format the data. (See Paragraph 5.3.6, M8916–Logic and Write Module Description, for a more detailed description of the write operation.)

The write buffer outputs are transmitted through current-driver networks into the write head, where data is recorded on tape as the tape moves past the write head at 1.14 m/s (45 in/s).

5.2.4.4 Read Recovery – The data recorded/written on tape then travels from the write head to the read head. This distance is 3.8 m/s (150 in/s) so that a data bit deposited on tape by the write head appears at the read head 3.3 ms later.

At the read head, data is picked up and passed along the read cable to the G066 read amplifier module. (Test points are provided to inspect the analog stages of this module.) The output of the G066 module consists of digitized read data. This read data is passed along to the M8931 (or M8911-YB) module, where it is multiplexed with motion delay data. Read data is then transmitted as RD (0-7, P) to the controller.

In NRZI mode, a read strobe is generated in the TE16 [RSDO (SB) L]; while in PE mode, the controller assumes all responsibility for read data recovery.

5.3 DETAILED CIRCUIT DESCRIPTIONS

A unit level discussion of each module is presented in this section. The descriptions reference functional components on the circuit schematics; therefore, a complete TE16 engineering drawing set should supplement this section. The reader can also use these descriptions with the functional diagrams in the previous section to gain an overall understanding of TE16 (TE10W/TE10N) operation.

The sections and corresponding module descriptions are summarized below:

5.3.1 H607 Tape Motion Power Board
5.3.2 5412242 Power Supply
5.3.3 G066 Read Amplifier
5.3.4 M8911-YB/M8931 Slave Clock and Motion Delay Module
5.3.5 M8912 Test Function Generator
5.3.6 M8916 Logic and Write Module
5.3.7 M8926 (TE10W) Interface Module
5.3.8 M8927 (TE10N) Interface Module
5.3.9 TE16 Switch Box

5.3.1 H607 Power Board

The H607 comprises the tape motion power board (5412264-DRVR) and the tape motion daughter board (5412262-TMD). Together (as the H607), they contain the capstan drive circuitry and the tape reel braking and motor control circuits. Individually, the two modules are referred to as the mother (DRVR) and daughter (TMD) modules. The mother module is rigidly mounted to the deckplate, while the daughter module is hinged. It swings outward for access while troubleshooting or adjusting.

5.3.1.1 Tape Motion Power Board (DRVR) - The tape motion power board (mother) is divided into two main areas: capstan servo control and driver circuits, and the tape reel braking and motor control circuits. This discussion references the 5412264 (DRVR) schematics.

5.3.1.1.1 Capstan Servo Control and Driver - The heart of the transport mechanism is the capstan subsystem, which transports the tape across the read/write/erase head assembly at the desired speed. The capstan is controlled by a velocity feedback servo loop (Figure 5-6). Refer also to sheet 2 of the 5412264 (DRVR) schematics.

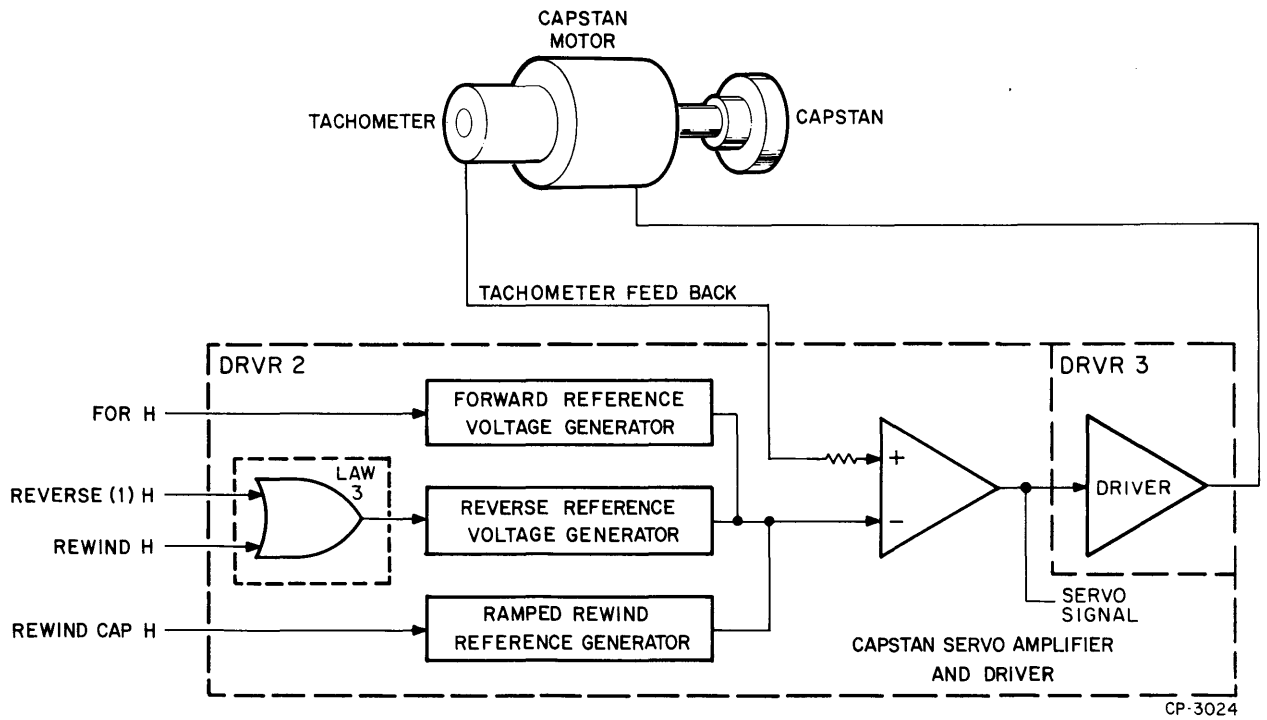


Figure 5-6 Servo Feedback Loop

As a forward command enters the logic (FOR H), Q29 is biased correctly to turn on. With Q29 turned on, the voltage at the base of Q44 is higher than the -8 V at the emitter, resulting in Q44 being turned on.

If either reverse or rewind is selected, signal REV/REW H becomes true and turns Q45 on. Notice that the collectors of Q44 and Q45 are connected and that the output line is the running speed line going to the "-" input of the 72741 operational amplifier. Diodes D55 and D54 detect the more positive and more negative levels from Q44 and Q45 respectively when selected. Therefore, when Q45 is on (Q44 off), D54 conducts and when Q44 is on (Q45 off), D55 conducts.

Resistors R91 and R87 are the forward and reverse speed adjustments; each is adjusted to move tape at 1.14 m/s (45 in/s).

Transistors Q46, Q47, and Q48 constitute a -8 V series regulator that biases the forward (Q44) logic. Transistors Q36, Q37, and Q38 make up a +8 V series regulator that supplies +8 V to the reverse (Q45) logic. Circuit schematic DRVR2 lists test points available for checking these supplies.

The tachometer feedback signal (TACH V) is filtered and applied to the "+" input of the operational amplifier (comparator). The tachometer produces an output voltage (TACH V) proportional to the velocity of the capstan. The capstan servo amplifier (72741 at E10) compares the tachometer output with a reference voltage that is proportional to the desired capstan velocity and generates an appropriate error voltage. The error voltage (SERVO SIGNAL) is further amplified by the capstan motor driver, which drives the capstan motor. Thus, if the capstan is running slower than the desired speed, the SERVO SIGNAL and, consequently, the voltage impressed on the capstan motor increase, speeding up the capstan. If the capstan is running too fast, the capstan velocity is similarly decreased.

When the capstan is at rest and a forward command is issued, the difference between TACH V (0V) and the forward (Q44) circuitry is quite large. This causes the error voltage comparator to produce a large amplitude SERVO SIGNAL, which goes to the driver circuitry to allow the capstan velocity to approach 1.14 m/s (45 in/s) forward velocity.

Resistor R177 is the balance adjustment. It is adjusted for zero capstan creep, with no input.

For normal [1.14 m/s (45 in/s) forward and reverse] operation, the vacuum columns buffer enough tape to allow time for the reels to catch up with the rapid accelerations and decelerations of the capstan. However, the buffer columns cannot contain enough tape to allow the capstan to accelerate and decelerate at its normal high rates to and from the 3.8 m/s (150 in/s) rewind velocity. For this reason, the rewind command logic uses two signals (REV/REW H and REWIND CAP H) to control the rewind velocity of the capstan.

When a rewind command is issued, signal REV/REW H is asserted, causing the capstan to accelerate immediately to 1.14 m/s (45 in/s) just as in a normal reverse operation. Then, REWIND CAP H is asserted approximately 200 ms later; transistor Q30 is turned on, placing an increasing current in the running speed line. This causes a ramped rewind reference voltage generator (R79/C19 time constant) to gradually increase the rewind speed, exponentially approaching 3.8 m/s (150 in/s) at a rate at which the reels can be accelerated. Resistor R84 is used to fine-adjust the rewind speed.

Refer to schematic DRVR 3. This is the circuitry that drives the capstan motor. When SERVO SIGNAL enters, it is applied to the bases of two transistors, Q33 and Q41. Transistors Q33 and Q41 sense the SERVO SIGNAL polarity for the forward (+) and reverse (-) directions, respectively. The circuitry involving transistors Q28, Q31, and Q32 supplies current amplification for the forward direction, providing CAPSTAN MOTOR POWER with the current necessary to drive the motor. Transistors Q39, Q40, and Q49 operate in a similar manner for the reverse direction.

The SERVO SIGNAL is also diode-coupled to the outputs of two differential amplifiers. These amplifiers compare the capstan motor current with two fixed reference voltages. When the capstan motor current produces 0.8 V across R103 (corresponding to an 8 A motor current), one of these differential preamplifiers senses the fact and clamps the SERVO SIGNAL, preventing the capstan motor current from becoming greater.

Because the capstan motor acceleration is directly proportional to the motor current, this differential amplifier circuit accurately controls capstan acceleration. By controlling the capstan acceleration, the size of inter-record gaps on tape is also controlled.

In normal operation, the current limiting circuitry is activated only during the 8 ms (approximately) interval during which the capstan is accelerating to speed at the beginning of a motion operation or decelerating to a halt. Once operating speed is reached, capstan motor current drops to approximately 1 A and is controlled entirely by the SERVO SIGNAL acting to hold the motor at a ±1.14 m/s (±45 in/s) velocity.

Transistor Q34 is used in the forward line; Q42 in the reverse. Resistor R86 is the "+" current adjustment used to fine-tune the positive acceleration current, eliminating large changes in the MOTOR RETURN line. Resistor R104 adjusts negative acceleration current, following a similar philosophy.

5.3.1.1.2 Motor Control and Tape Reel Braking Circuits – Circuit schematics DRVR 1 and DRVR 4 illustrate the motor control and braking circuits. As explained in the previous paragraphs, it is necessary to maintain a small "buffer" of tape on either side of the read/write/erase head, because the massive tape reels cannot accelerate at the same pace as the smaller, much lighter capstan. Vacuum-buffer columns are used to hold these "buffer" loops of tape. The capstan does not directly move tape from one reel to another; rather, it removes tape from one vacuum-buffer column and deposits it in another. Each reel servo system endeavors to keep its associated vacuum-buffer column partially filled with tape, ready either to supply or to take up tape, as might be required by a sudden acceleration of the capstan.

Figure 5-7 shows the tape transport vacuum-buffer columns and the respective tape-position-sensing vacuum switches. A vacuum port at the bottom of each vacuum-buffer column provides the vacuum that draws the tape loops into the columns with a constant tension (252 g or 8 oz), independent of the position or velocity of the tape loop. This helps assure a uniform wrap of the tape on the reel. In normal operation, the position of the tape loop in each vacuum-buffer column is sensed by vacuum switches located near the top and bottom of each column. These vacuum switches close when subject to a vacuum exceeding 35.4 cm (10 in) of water and open when exposed to ambient air pressure. Thus, if the tape loop is above a particular vacuum switch in the buffer column, that switch is exposed to vacuum; the switch is then closed and its corresponding signal (UVS for the upper vacuum switches and LVS for the two additional lower vacuum switches) is at ground. If, however, the tape loop is below a vacuum switch in either column, the switch is exposed to ambient air pressure; it opens and the corresponding signal is high. The reel servo systems endeavor to keep the respective tape loops oscillating near their respective vacuum switch pairs.

Figure 5-8 shows an equivalent circuit of the reel motor drive. Each reel motor is connected across a transistor bridge, which connects the motor between the -17 V and +17 V INT power supplies in either direction. When the relay supplying +17 V INT opens, no power can be applied to the motors, providing a fail-safe condition. When transistors A and B (Figure 5-8) are on, current flows through the motor in a "+ to –" direction and the motor turns clockwise (CW). When transistors C and D are turned on, current goes through the motor in a "– to +" direction and the motor turns counterclockwise (CCW).

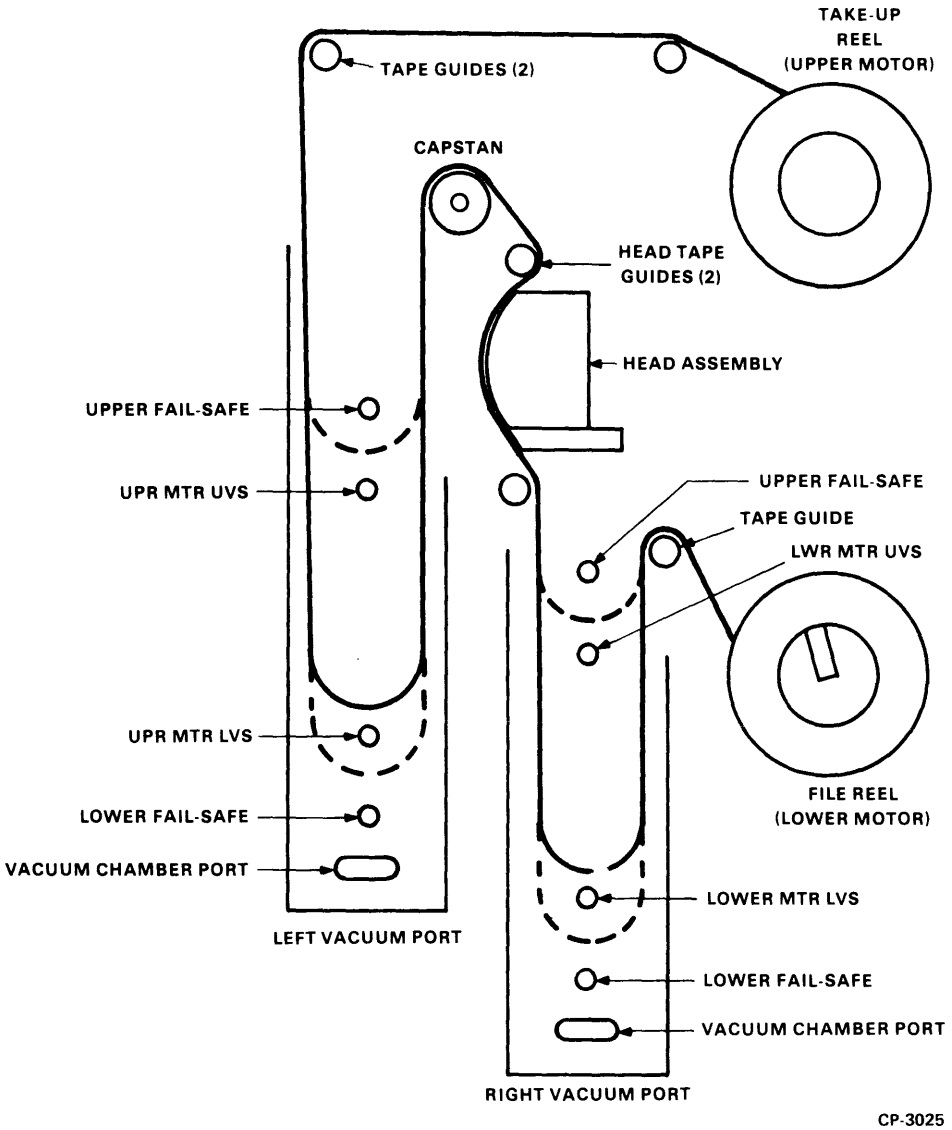


Figure 5-7 Tape Transport Mechanism

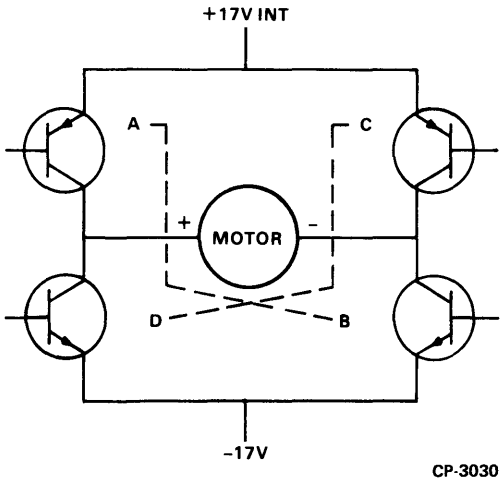


Figure 5-8 Reel Motor Amplifier Equivalent Circuit

The motor circuitry interfaces with the remainder of the drive with six signals:

UPR MTR GO CW
UPR MTR GO CCW
LWR MTR GO CW
LWR MTR GO CCW
REEL MTR ENABLE
LOAD PULSE

The LOAD PULSE is used only during a tape loading sequence. The remaining five signals control normal operation. Signal REEL MOTOR ENABLE is generated on the M8916 (LAW) module. It indicates that tape is in the columns and no fail-safe condition exists. Because the upper motor (UPR MTR) circuitry (take-up reel) functions identical to the lower motor (LWR MTR) circuitry (file reel), only the UPR MTR circuitry is detailed in this description.

On circuit schematic DRVR 1, signal UPR MTR GO CW L comes through J3-X and is ANDed with REEL MTR ENABLE L. The output goes to a 75452 current buffer. Its output (low) pulls R17 to ground and turns on Q6, providing additional current gain. Q6 draws current from the base of Q16 and supplies it to the base of Q9. Both transistors turn on, resulting in J1-1 going close to +17 V and J1-2 going close to -17 V; the motor turns CW.

If signal UPR MTR GO CCW is asserted, a similar operation occurs; only this time transistor Q7 turns Q13 and Q15 on. This reverses the + and - 17 V on pins J1-1 and J1-2 and drives current through the upper motor in the opposite direction, resulting in the upper motor turning CCW.

The lower motor circuitry works in an identical manner to turn CW or CCW. LWR MTR GO CCW and REEL MTR ENABLE turn transistor Q5 on, which allows transistors Q8 and Q1 to pass current in a "+ to -" direction through the lower motor and turn it CCW. The LWR MTR GO CW signal uses transistors Q4, Q2, and Q3 to turn the lower motor CW.

The LOAD PULSE signal (asserted only in a loading sequence) bypasses REEL MTR ENABLE. It passes through a 75451 gate and pulls R19 low. This has the same effect as if both UPR MTR GO CCW and REEL MTR ENABLE had been asserted. With respect to the lower motor, the effect is the same as if LWR MTR GO CW and REEL MTR ENABLE had been asserted. The result is that a small tape loop is dumped into each column, sealing both columns.

The brake control logic is illustrated on schematic DRVR 4. The brakes used on the TE16 are electromagnetically operated friction brakes. In normal 1.14 m/s (45 in/s) operation, signals UPR BRAKE ON and LWR BRAKE ON individually create the UPPER BRAKE OUT and LOWER BRAKE OUT signals. These signals drive approximately 310 mA of current through the brake windings. Braking is not used during a rewind operation.

Signal UPR BRAKE ON L asserts, placing a low level at pin 13 of the 7400 NOR gate in E6. The output asserts high and, because signal UPR MTR START L is not true, the output of the 7408 in E7 asserts and supplies brake current for the upper brake to the base of transistor Q23. With Q23 on, transistor Q20 also turns on. This places the R55/R59 resistor combination into the UPPER BRAKE OUT circuit, limiting and establishing the operating brake current. The 310 mA of brake current applied to the brake winding produces enough torque to rapidly bring the upper (take-up) reel to a stop.

The lower brake works in an identical manner. Also, the FORCE BRAKE ON (1) L signal, a 4-second delay generated on the LAW (M8916) module during power-up, fail-safe, power fail or an accident applies both brakes simultaneously.

When the tape loop leaves a brake zone, brake current is shut off. Because the braking current tends to produce a significant residual magnetism in the brakes, a short (15 ms) pulse of approximately 150 mA current is applied in the reverse direction when the brakes are released to ensure complete demagnetization and release of braking. When the brakes are to be shut off, the output of 7408 in E7 negates and goes low. This low transition is ac coupled through C13 to Q22 and Q21 (as UPPER BRAKE OUT), resulting in the short pulse. Zener diode D30 and R51 (collector resistor of Q22) cause the smaller (150 mA) current.

5.3.1.1.3 Automatic Unload Sequence – The main objective of the unload circuitry is to gently wind tape back onto the lower reel. In order to do this, a regulated voltage is applied to the lower reel motor during the unload sequence. This voltage (adjustable) determines the speed at which the lower motor turns. The upper motor is also activated during the unload sequence by a "trickle" current intended to overcome internal friction in that motor.

The BRIDGE TURN ON L signal turns on Q14, which supplies base current to Q50, turning it on. J1-2, the "–" side of the upper motor, is pulled up toward +17 V. The Q14 collector also supplies base current to Q1, resulting in a voltage at J1-6. Essentially, a power voltage is applied to one lead of each motor. Two additional circuits are used to limit the amount of power that can be dissipated in the motors, thus limiting the torque each motor can produce so that a gentle unwind results.

Coincident with BRIDGE TURN ON L, signal INIT TORQUE SETTING H asserts. The current through Q17, varied by R42, is just enough to start the upper motor turning so that the unload sequence can continue. If the upper motor does begin turning and the lower motor is successfully taking up tape, the DAC signal is not required. However, if the tape binds, for example, or if the upper motor sticks, then the DAC CONTROL signal begins to go negative. This signal goes through a 741 operational amplifier, with two additional transistors for current gain. This trickles greater currents to the upper motor, trying to break if free. Once the motor breaks free and the capstan is turning in a current unload sequence, the DAC CONTROL signal stops incrementing, but remains at its last output voltage. Note that the capstan motor is not activated during the unload sequence; rather, it is dragged around as the lower motor pulls tape onto itself.

As the capstan motor is dragged, the capstan tachometer outputs a voltage proportional to its speed. Circuitry on the daughter board senses whether the capstan is being turned and uses this information to either maintain or increase the power available to the upper and lower motors.

INIT TORQUE SETTING and DAC CONTROL control the amount of current to be drained through the upper motor. By sensing the voltage across R38 (.47 ohms) and by inputting that to the sensing node of the 741, a current driving network is produced. The more current through R38, the more the operational amplifier output goes negative. This tends to turn off the current gain transistors (Q18 and Q19). This feedback path senses the current through the motor and controls it through the 741. Reiterating, this is a current controlled operation.

A different technique is used with the lower motor during the unload sequence. The 723 references from -17 V, not ground, and supplies a precise voltage across the lower motor. The 723 input is floating at approximately -17 V. When the unload begins, the BRIDGE TURN ON signal asserts, turning on Q14. In addition to supplying current to the base of Q1, transistor Q14 also supplies power for the 723 regulator, which then puts 8 V across the lower motor. Resistor R28 adjusts the voltage across the lower motor during the rewind sequence. Whereas current was trickled through the upper motor to control torque, regulated voltage is used across the lower motor to control the speed.

The MAX FORCE signal is to the lower motor what the DAC CONTROL signal is to the upper motor. It asserts about two seconds after the beginning of the unload sequence if no tape motion is sensed. If asserted, the MAX FORCE signal causes the 723 regulator to operate in a current limiting mode instead of a voltage controlling mode, which then attempts to break the lower motor free.

Whether or not the MAX FORCE signal is ever used, the regulator circuit is current limited. The voltage across R26 (.47 ohm) is sensed and fed back to the regulator; current is limited to approximately 2 A.

5.3.1.2 Tape Motion Daughter Board - The tape motion daughter board (TMD) controls braking and reel motor operation (both in normal tape motion and in rewind) and also contains the sequencing logic for the unload circuitry. This discussion references the TMD (5412262) schematics.

Drawing TMD1 illustrates the common logic used to control the brakes and reel motors. The vacuum switch signals the module (left hand side of drawing) through the J2 connector. An RC filter eliminates crosstalk among the four control switches. The 8640 gates send the filtered signals to type 74123 one-shots connected in a retriggering mode, each for approximately 1 ms. Look, for example, at the UPR MTR UVS (upper motor vacuum switch) signal. If vacuum is sensed, the left hand upper vacuum switch closes, pulling the UPR MTR UVS signal to ground. This signal then becomes inverted in an 8640 gate, which applies a high level to pin 1 of the 74123 one-shot in E27. The high level disqualifies the delay and it begins to time out. Therefore, within 1 ms of the switch sensing vacuum, the delay output (pin 13) would go low. Similarly, when vacuum is removed from the UVS, pin 1 of the delay would be low, thus qualifying the delay. That qualification prepares the delay and the HI FREQ CLOCK signal (discussed later) retriggers it. So, as long as vacuum is not sensed, pin 13 of the delay is high. Essentially, the delays filter switch bounce at the leading and trailing edges of vacuum switch activation.

The FWD MOTION flip-flop remembers the last direction of tape motion and controls reel motor direction. Its output feeds the select input of a multiplexer (E32). The output of this multiplexer controls the direction in which the corresponding reel motor is driven.

The multiplexer does not observe all the vacuum switches all the time, but rather picks those vacuum signals that are of particular interest. For example, assume forward tape motion (FOR H asserted); this direct sets FWD MOTION, which places a low at the S0 input of the multiplexer. A low here selects the "A" inputs. In this example, therefore, the multiplexer would observe UPR MTR LVS and LWR MTR UVS. When tape is moving forward, the tape loops should be located near these two vacuum switches, not the other two, UPR MTR UVS and LWR MTR LVS (Figure 5-9). (A tape loop outside a fail-safe switch automatically shuts down transport operation.) The multiplexer actually defines those vacuum switches that are of interest, keeping the tape loops near those switches. By using these switches during forward motion, it can be seen that in a sudden capstan direction reversal, most of the buffer column is available to let the reel motor "catch up" with the capstan. In forward motion, tape is pulled out of the right column and is deposited into the left column.

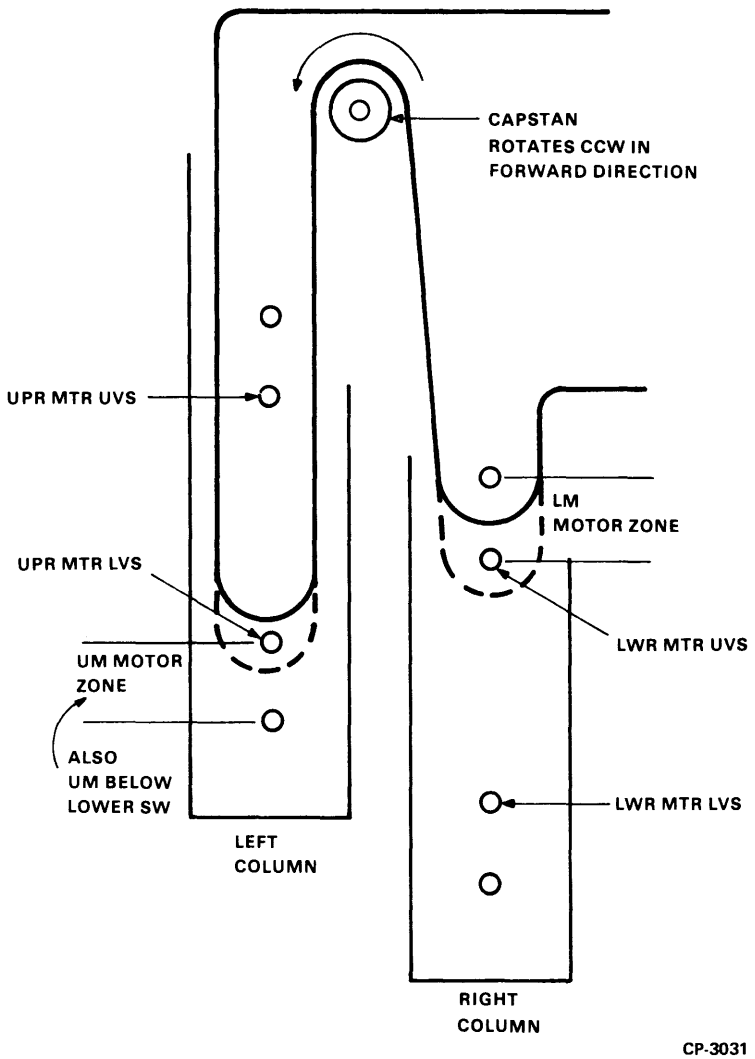


Figure 5-9 Tape Loop Location - Forward Motion

Looking at the location of the tape loop in the left column, notice that almost an entire column length exists between the loop (near LVS) and the UVS. In the case of a tape motion reversal, the entire column's worth of tape may be used to make whatever changes are necessary in reel motor velocity to keep up with the new (reverse) tape motion. A similar situation holds true for the right column.

In a reverse tape motion sequence, the capstan is pulling tape out of the left column and depositing it in the right column (Figure 5-10). The theory dictates that the tape loops should oscillate near the UPR MTR UVS and the LWR MTR LVS. Again, any tape loop outside a fail-safe switch automatically shuts down transport operation. As was the case in the forward direction with the tape loops in these locations, the greatest margin exists for permitting reel motor velocity changes in a direction change. The multiplexer observes only one vacuum switch per side in any tape motion sequence. It outputs a MOTOR ZONE and BELOW LOWER SWITCH signal for each column.

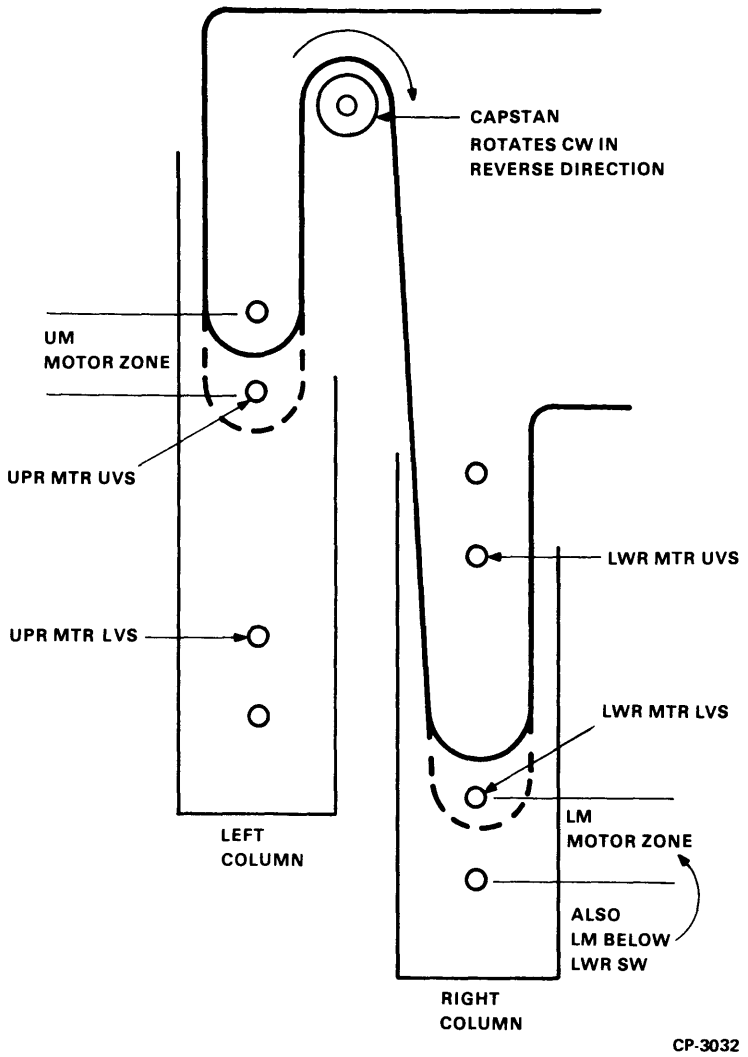


Figure 5-10 Tape Loop Location - Reverse (and Rewind) Motion

Referring back to the forward motion diagram (Figure 5-9), the upper motor (UM) MOTOR ZONE in forward tape motion is between the UPR MTR LVS and the lower fail-safe switch, while the LM MOTOR ZONE is between the LWR MTR UVS and its upper fail-safe switch. In reverse (see Figure 5-10), the UM MOTOR ZONE is between the UPR MTR UVS and its fail-safe switch and the LM MOTOR ZONE is between the LWR MTR LVS and its fail-safe switch.

In forward motion, the UM BELOW LOWER SW signal is defined (for the upper motor only) when the tape loop is between the UPR MTR LVS and its fail-safe switch. Similarly, in the reverse direction, the LM BELOW LOWER SW signal can be asserted only when the loop attached to the lower motor is between the LWR MTR LVS and its fail-safe switch (Figures 5-9 and 5-10).

The main point here is that the direction of the last tape motion sequence defines which vacuum switches the tape loops are to be positioned near.

Also on TMD1, signals REW CAP H, FOR H, and REV/REW H are ORed, generating signal MOTION L. Basically, the MOTION signal is asserted whenever the capstan motor is moving. MOTION is ORed again, with each MOTOR ZONE signal, and each 7408 output is input to a 74123 one-shot (both halves of E19). When either MOTION or the relevant motor zone signal (UMZ, LMZ) is asserted, this circuit detects whether tape is moving, or is just about to stop after a motion sequence, or is still in a MOTOR ZONE. If any of these conditions are true, the relevant BRAKE ENABLE flip-flop is not set. However, should tape motion cease for a longer period than the E19 one-shots are timed for (2 or 3 ms) and the tape loop is successfully brought back into the middle zone, the SET BRAKE ENABLE signal would assert and the brake would be applied. By ORing MOTOR ZONE with MOTION, the logic can never turn the brakes on in the middle of a data transfer; it always waits until motion stops. The brakes are used to stop a tape loop only at the end of the motion sequence. As long as MOTION is asserted, the brakes cannot be turned on.

A second method is also used to generate the BRAKE ENABLE signals. The 74123 one-shot in E40 observes the FWD MOTION flip-flop, which changes state with every tape motion direction change. When tape motion changes direction, the one-shot fires, generating a 2 to 3 ms pulse and setting the BRAKE ENABLE signals. The main reason for this alternate method is that changing direction creates drastic change in capstan velocity, and the reel motor control circuits cannot respond to a sudden direction reversal. By design, the reel motors can only respond to a capstan speed change from a dead stop to 1.14 m/s (± 45 in/s). Therefore, if tape speed changes, for example, from +1.14 m/s to -1.14 m/s (± 45 in/s), the reel motor control cannot respond fast enough. The brakes must be used to bring the reel motor to a stop. It can then respond to the change in tape velocity direction.

The MID ZONE signals assert when tape is in the middle zone (i.e., UVS open and LVS closed). Each MID ZONE signal is ANDed with its corresponding BRAKE ENBL flip-flop output to generate the UPR/LWR BRAKE ON signals. These are the signals that apply brake current to the reel brakes.

The one-shots associated with the BRAKE ON signals ensure that once a brake is turned on, it remains on for a minimum of 10 ms. If the brakes (when applied) are not held on for this minimum time, they may be degaussed before they are fully turned off. This would result in an improper degauss spike and a "dragging" brake.

The HI FREQ CLOCK used to retrigger the vacuum switch one-shots comprises two 74123 one-shots. The output (adjusted by R16) is counted down by a single flip-flop into a 7497 variable frequency counter. Its output, CLOCK H, is a 5 ms period pulsed wave form.

Drawing TMD2 and TMD3 are identical, except that TMD2 references the lower motor while TMD3 references the upper motor. Because they are similar, just TMD2 is discussed, unless otherwise specified.

In general, throughout the reel motor control circuitry discussion, the assumptions are made that the capstan and reel motors are at a dead stop and the tape is in a middle zone. Therefore, referring to TMD2, assume that signal SET LM BRAKE ENABLE L is initially asserted. This direct sets the LWR BRAKE ENBL flip-flop and turns on the brake circuits; this also direct sets the LM NO DUTY CYCLE flip-flop. When a tape motion command is executed, the SET LM BRAKE ENABLE signal is negated, removing the direct set signal from the LWR BRAKE ENBL flip-flop; the flip-flop, however, remains set.

Now, tape moves into the MOTOR ZONE. The acquisition of the LMZ signal places a low level at the data input of the LWR BRAKE ENBL flip-flop and causes a pulse to be generated by the 7486 in E21. The pulse generator triggers a 74123 one-shot, which outputs a 1 ms pulse to the 74190 sequencing counter (E3); it also clocks and clears the LWR BRAKE ENBL flip-flop. The LWR BRAKE ENBL flip-flop is turned off, so the brakes are off. Now, current can be applied to the reel motor.

When the LMZ signal generated a 1 ms pulse from the E5 one-shot, that output went to the E3 sequencing counter and loaded a preload count, consisting of GROUND and a combination of:

LM NO DUTY CYCLE and
LM BELOW LOWER SW

E3 is a divide-by-ten counter and sequences at the CLOCK rate (5 ms). When the counter overflows, it clocks and sets the LM START DUTY CYCLE flip-flop, placing a low level at the clock input of the LM NO DUTY CYCLE flip-flop. The counter recycles (ten additional CLOCK pulses); this overflow clears LM START DUTY CYCLE, which then clears the LM NO DUTY CYCLE flip-flop. So, the LM NO DUTY CYCLE flip-flop remains on during the time tape moves into the MOTOR ZONE for a period equal to 10 minus the preset count, plus another 10 counts. Then LM NO DUTY CYCLE is turned off.

During its on period, LM NO DUTY CYCLE is presenting a high level to pin 2 of the 7427 NOR gate, which results in a constant enable at the inputs of the LM GO CW and CCW gates. When the enable is present, the gates are guided by a direction flip-flop to turn the motor in the desired direction.

Once the LM NO DUTY CYCLE flip-flop is off, the GO CW/CCW (motor enable circuitry) gates are dependent on the pin 6 output of the sequencing counter. Because the 74190 is connected as a divide-by-ten counter, the pin 6 output is low for four counts (0 through 3), goes high for four counts (4 through 7), and then goes low again through the tenth count. Essentially, the pin 6 output is low 60 percent of the time and high 40 percent. The output is XORed with LM BELOW LOWER SWITCH H. When LM BELOW LOWER SWITCH is negated (low), the pin 6 counter output is sent directly (non-inverted) to E22, pin 13. Therefore, assuming NO DUTY CYCLE is off and the logic is dependent on the pin 6 output to determine the motor driving duty cycle, that duty cycle is 40 percent. However, if the LM BELOW LOWER SWITCH signal is true (tape loop is below the lowest control switch), the pin 6 output signal is inverted by the XOR, presenting a 60 percent duty cycle to the motor enable gates. Whenever tape is below the lowest control switch, the motor is driven harder than anywhere else.

Again, assume a stopped condition with tape in the middle zone. Tape then moves to a MOTOR ZONE and the NO DUTY CYCLE holds the motor on. Then, when the NO DUTY CYCLE flip-flop clears, the logic enters a "duty cycling" mode, where the motor receives pulses of power, rather than steady current. This pulsed power is sufficient to force the tape loop back into the middle zone. The reel motor control is stable as long as the capstan velocity remains stable. Under control of the E3 counter, the logic attempts to push the motor in the opposite direction.

The counter still controls the duty cycle (through the XOR in E28), but the direction is still controlled by the 7474 flip-flop in E30. As mentioned previously, this flip-flop, controlled by the FWD MOTION flip-flop and HI FREQ CLOCK, controls the reel motor direction.

As the capstan is moving tape, the tape loop oscillates about the appropriate control switch. The reel motor is continually pulsed at the appropriate duty cycle rate in the direction to drive the tape loop back toward the switch (i.e., if the loop is above the switch, pulse the motor to force the loop up). In a stable fashion, this circuitry continually "hunts" for the relevant vacuum switch.

When tape motion first starts from a dead stop, the LM NO DUTY CYCLE flip-flop is set. This causes a long time (approximately 100 ms) that the reel motor is full on, trying to aproach the capstan tangential velocity. If a tape loop goes below the LVS, the motor is pulsed again with a 100 ms pulse to ensure bringing the tape loop out of the column and up toward the UVS. After this pulse, the regular duty cycle is used to pulse the motor. In the event of a tape motion sequence that drives tape past the LVS, a 100 ms pulse of 100 percent voltage is applied to the motor every time the loop goes below the LVS.

Every time the tape loop goes below LVS, the LM BELOW LOWER SWITCH signal triggers a 74123 one-shot in E20, and its output direct sets the LM NO DUTY CYCLE flip-flop. As a result, every time the loop goes below the LVS (on the lower motor), a 100 ms pulse is applied to the motor. Then the sequencing counter pulses the motor as before, until the tape loop comes above the LVS. Again, the duty cycling resumes to push the tape loop down, "hunting" the switch.

So far, two methods of generating the motor direction signals (GO CW/CCW) have been explained: LM NO DUTY CYCLE and E3 Sequencing Counter.

One additional method of producing these direction signals exists. Rewinding tape forces the reel motors to operate near their top speed, and the normal duty cycle is not sufficient to drive the motors when tape is in the MOTOR ZONE. As soon as the tape loop enters the MOTOR ZONE during a rewind sequence, the reel motors are turned on and remain on until the tape loop reenters the middle zone.

Signals REW CAP H and LM MOTOR ZONE H are ANDed in a 7408 gate and the output is sent to the third input of the motor enable NOR gate (7427, E22, pin 1), causing a 100 percent duty cycle.

Again at rewind velocity, the motor control logic attempts to remove the tape loop from the MOTOR ZONE (away from the fail-safe switch) and into the middle zone. The normal duty cycle then resumes. In rewind, just as in normal forward or reverse operation, the logic is always "hunting" for the vacuum switch.

5.3.1.2.1 Load - Unload Sequence - The RELAY ENABLE signal is sent to the TMD board from the LAW board (M8916, Paragraph 5.3.6) during a load sequence. The RELAY ENABLE signal fires a 2 second 74123 one-shot (E4). When it times out, the LOWER FAIL SAFE signal is observed. If the switch is open (indicating no tape in the column), then a second one-shot is fired, producing a 70 ms LOAD PULSE. The RELAY ENABLE signal is delayed 2 seconds, in order to provide sufficient time for the vacuum motor to establish vacuums in the columns. Then, a check is made to see if tape is in the columns. If tape is not in the columns, a LOAD PULSE dumps approximately 70 ms worth of tape into the columns.

The unload sequencing logic is illustrated on the TMD4 circuit schematic. When the UNLOAD switch is pressed on the front panel (i.e., transport is at BOT and the REW/UNLD switch is pressed), the INHIBIT UNLOAD signal (lower left corner of TMD4) is negated by the M8916. The M8916 (LAW) module then sends an UNLOAD PULSE to the 7474 flip-flop (E29) and asserts the START signal.

A counter network comprising three 74197s is located in the lower middle of TMD4. When START (1) H is true, the clear lines on the counters are lifted, thus enabling the counters. The CLOCK signal (5 ms rate) begins clocking the counter, which provides twelve bits (4096) of counting. During the unload sequence, this logic makes sure that the capstan is moving and, if it is not moving, working to drive greater amounts of current to the reel motors to try to break them free. This module receives its feedback from the CAPSTAN TACH VOLTAGE signal. An assumption is made that if the capstan is not moving, then something is stuck or stalled. Two methods are used to break free whatever is stuck or stalled.

A 339 comparator in E42 (pin 6) observes the CAPSTAN TACH VOLTAGE signal and compares it to V1, a 7.5 mV level. If the capstan is moving at all, the comparator output asserts and then clears the 7474 flip-flop (pin 1) in E24. This results in the CAPSTAN RESET flip-flop being held clear all the time the capstan is moving. Therefore, the unload sequence lasts until either the capstan stops moving or the counter produces a timed clear pulse.

The CAPSTAN TACH VOLTAGE is also compared with a second level (V2), a 100 mV level. The output from this 339 comparator (pin 14), through an AND gate, generates DAC CLOCK, which clocks another counter (74191). This is a 4-bit counter that generates an analog output from pin 6; it essentially is a DAC converter, with the output (pin 6) incrementing with CAPSTAN TACH VOLTAGE. As long as CAPSTAN TACH VOLTAGE is less than 100 mV, the 74191 is counted and a continually more negative voltage outputs from pin 6. That negative voltage then causes more current to input to the upper motor. Assuming the CAPSTAN TACH VOLTAGE does not become greater than 100 mV, then something is stuck and the extra current to the upper motor attempts to break free whatever is stuck.

A similar operation provides extra current to the lower motor in a sticking unload sequence. If the counter network reaches a count of 2^{11} before the unload sequence completes, the 2^{11} signal sets a 7474 flip-flop and generates the MAXIMUM FORCE H signal. If the unload sequence does not complete by the 2^{11} count, the MAXIMUM FORCE H signal (a higher current) is applied to the lower motor to break free whatever is stuck. The two most significant bits of the counter network (2^{11} and 2^{12}) are decoded in a 74H11, E33. Once this count is decoded (3000_{10}), approximately 15 seconds from the beginning count, the START flip-flop is cleared by the MAX TIME OUT signal. The lower time limit (when the capstan is not turning at all) is set by the condition that the capstan voltage remains at zero. Then a count of 1000_{10} (2^{11} or 2^{12}) is decoded (7427, E23) and, at that time (approximately 5 seconds), the two 7474 flip-flops associated with CAPSTAN RESET are set; this clears the START flip-flop. When the capstan is not moving, the unload sequence lasts approximately 5 seconds.

For the situation where the capstan motor continues to turn (CAPSTAN TACH VOLTAGE greater than 7.5 mV), the CAPSTAN RESET flip-flop is cleared. If an extra long tape leader is encountered, the unload continues to the 15 second point before the START flip-flop is cleared. Any time up until then, the logic waits for the capstan voltage to cease and, if it does cease, ignores the CAPSTAN RESET signal. Basically, this circuit is adaptive to a 5 to 15 second range. Anywhere within the range, the logic senses a stop command; outside the range, it does not sense a stop command. In general, a 5 to 7 second unload is desirable.

The circuitry in the lower right corner of TMD4 waits for a count of 2^9 (approximately 2.5 seconds). At that time, two signals are generated: INIT TORQUE SETTING H and UPPER MTR START L. The INIT TORQUE SETTING enables trickle current to the upper motor. The UPPER MTR START signal releases the upper motor brakes. During the first 2.5 seconds of an unload sequence, the lower motor is doing nothing except drawing tape out of the columns and creating a good tight loop. After the 2.5 second delay, the brakes are turned off and the unload is permitted to continue.

5.3.2 TE16 Power Supply

The TE16 power supply is a forced air-cooled unit that converts single-phase, 115 V or 230 V nominal, 47 or 63 Hz line voltage to four regulated output dc voltages (+5.3 V, +12 V, +12 V, and -6.3 V) and four unregulated voltages (±16 V and ±17 V). The power supply is controlled by an 861 power control. Each of the regulated voltages has short circuit (current foldback) protection.

Overvoltage (Crobar) protection is incorporated in the +5.3 V, one of the +12 V supplies and -6.4 V circuits.

The power supply is divided into two sections (Figure 1-3A): the ac input circuitry, consisting of the transformer and large filter capacitors (transformer-capacitor assembly), and a regulator board, which contains the remaining circuitry. The power supply circuit description references schematic D-CS-5412242-0-1. The regulator board (Figures 5-11 and 5-12) contains all the circuitry between the transformer secondary winding and the power supply output cables. A 4-pin Mate-N-Lok connector (J1) supplies voltage to the fan and vacuum motor. Connector J2 connects the transformer secondary winding outputs to the regulator board, while J3 adds the large filter capacitors to the circuitry. Connector J4 connects the supply to the H607 power board servo circuitry and J5 supplies voltages to the TE16 backplane.

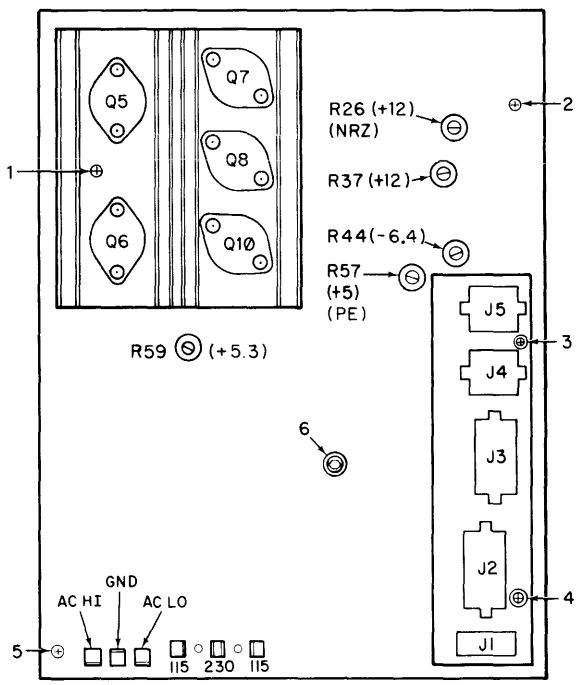


Figure 5-11 TE16 Power Supply Regulator Board

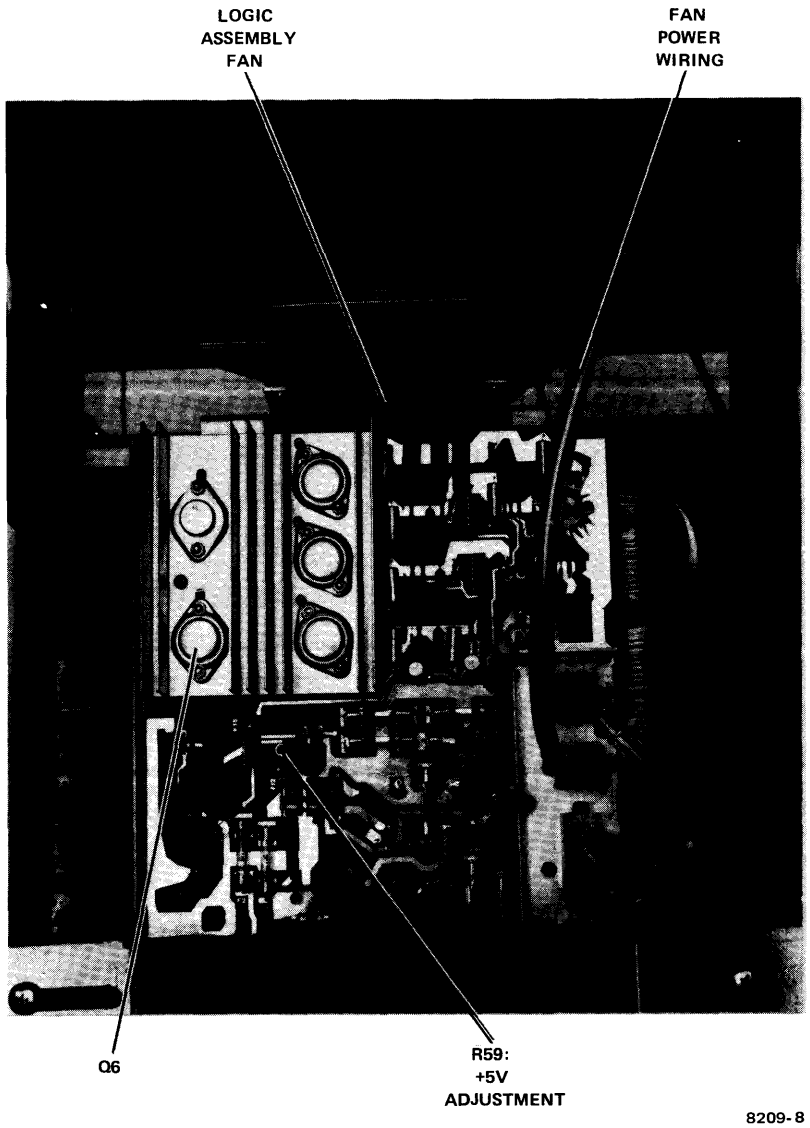


Figure 5-12 TE16 Power Supply Regulator Board (Cover Removed) and Fan

5.3.2.1 Generation of Raw ±dc – The ac power line cord, terminated with tab connectors, is brought to the lower left-hand area of the regulator board (as viewed from the rear of the TE16 cabinet) and connected to the input power tabs (AC HI, GND, and AC LO). Two wires (in the same area) connect to either the 230 V tab or the 115 V tabs and configure the power supply for 115 V or 230 V operation. The J2 Mate-N-Lok connector interconnects the regulator board and the main transformer.

A general block diagram of the power supply is shown in Figure 5-13. The center-tapped transformer voltage is fused, rectified, and filtered prior to being fed to the various voltage regulators and J4. The fuses do not normally blow when an output is shorted because of an overcurrent (current foldback) protection. Overvoltage protection (crobar) is also used on all regulated outputs except the +12 V (write circuits) output, which does not require it.

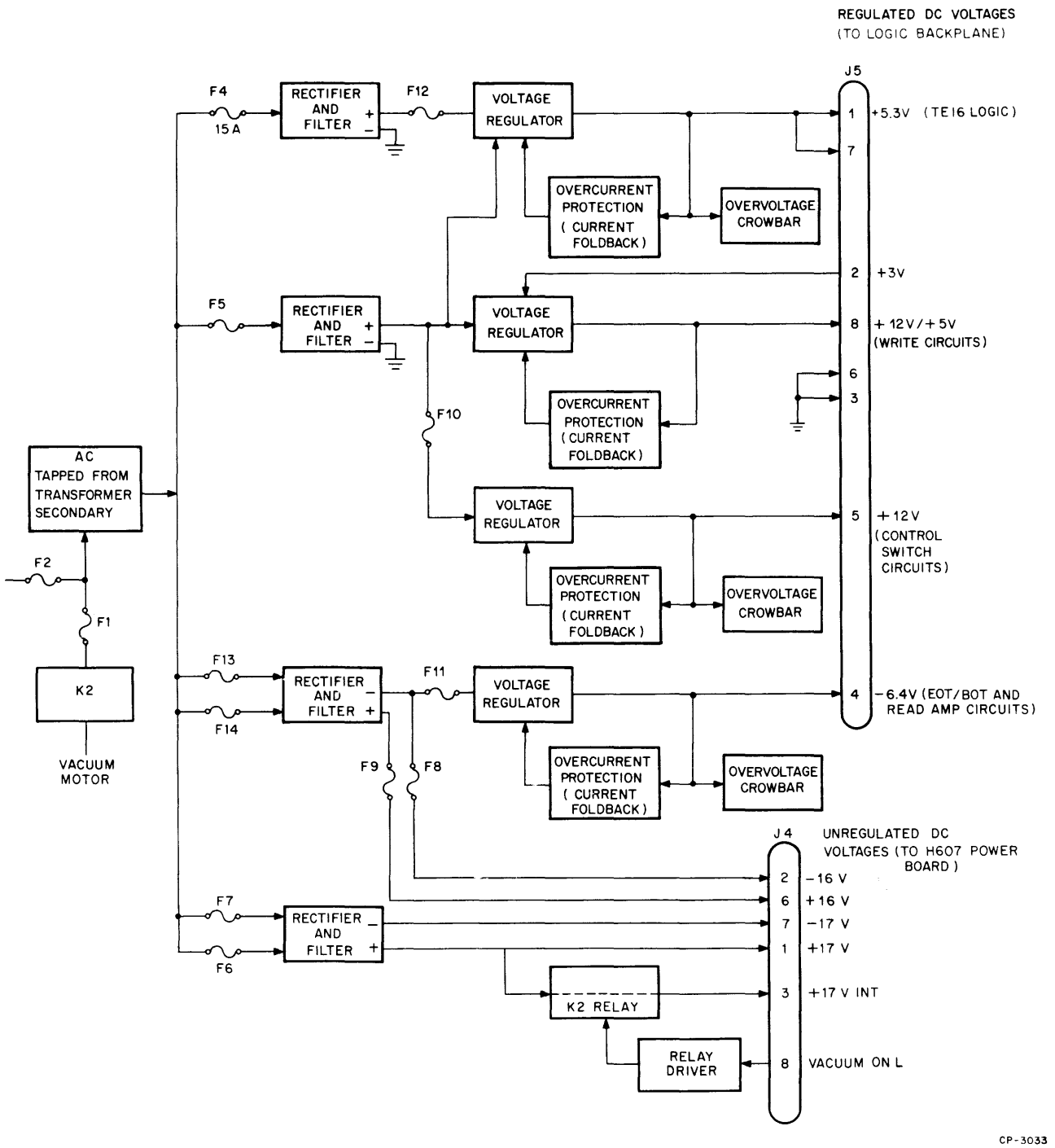


Figure 5-13 TE16 Power Supply Clock Diagram

The J4 Mate-N-Lok plug connects the TE16 power supply's unregulated voltages to the TE16 Power Board (H607, plug P2). Once tape is loaded onto the transport, signal RELAY ENABLE L is asserted. This places a low signal at the inputs of the 75451 gate (schematic D-CS-5412242-0-1, location A7) that enables the K2 relay. This relay passes required voltages on to the H607 module when tape is loaded.

5.3.2.2 +5.3 Vdc Regulator Circuit - The +5 Vdc regulator circuit is shown in Figure 5-14. Raw dc voltage is input to pins 11 and 12 of the 712 voltage regulator. The output voltage from pin 10 is fed to transistors Q5 and Q6, which are series regulators used to increase the current output capabilities of the circuit. Resistors R62 through R66 (inclusive) sense the output current. R62 is used as a current limit monitor by the 723. As the current increases, the voltage across R62 increases. When a reference voltage is exceeded, the 723 begins to turn off Q5 and Q6, impeding current flow. The current does not stop but decreases to a safer level; this is called current foldback. It assures that the output current never goes over 10.0 A. Figure 5-15 shows how the current foldback procedure works. As the current surpasses the limit of 10.0 A, the conduction of Q5 and Q6 slows down (toward being shut off) until no voltage is produced (at the short circuit current rating). The output voltage may be regulated. Resistors R58, R59, and R60 divide the reference voltage. The adjustment of R59 changes the +5.3 V output.

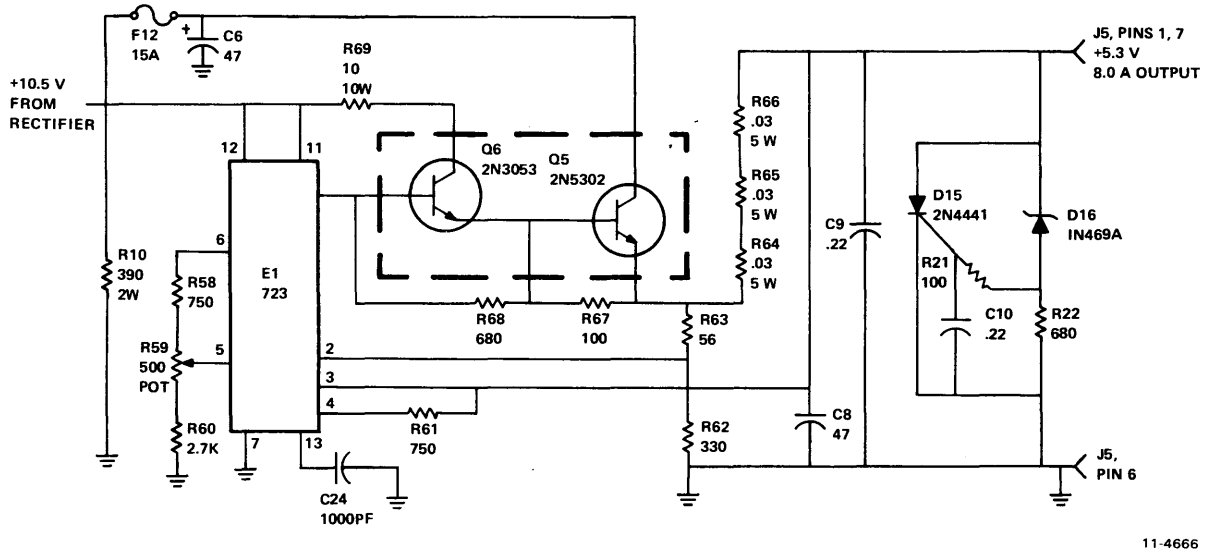


Figure 5-14 +5.3 Vdc Regulator Circuit

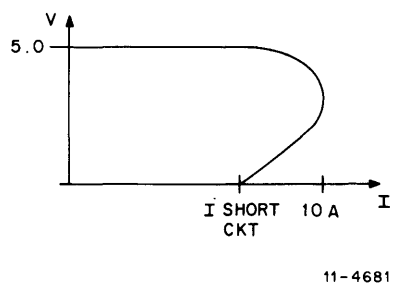


Figure 5-15 Current Foldback Operation

In addition to the current foldback feature, a voltage crobar circuit is used, offering overvoltage protection. If for some reason Q5 or Q6 becomes shorted, the overvoltage protection circuit protects any load connected to the power supply. When Q5 or Q6 short circuits, the output voltage starts increasing very rapidly. As the voltage across the D16 zener diode becomes greater than 6.8 V, it breaks down and begins conducting; it does not conduct during normal operation. Current now begins to flow through R22. When the voltage at the junction of D16 and R22 becomes greater than approximately 0.7 V (at the gate of D15), the SCR fires and begins conducting. This offers a path for current from the output to ground, shunting any load and thus protecting it. The SCR continues conducting until the power supply is turned off or the 15 A (F12) fuse is blown.

5.3.2.3 +12 Vdc Regulator Circuit (Write Circuits) - The 12/5 Vdc regulator circuit is shown in Figure 5-16. It operates in a manner similar, but not identical to, the +5.3 Vdc regulator circuit discussed previously. In the case of the +12 Vdc regulator, a type 723 regulator is again used.

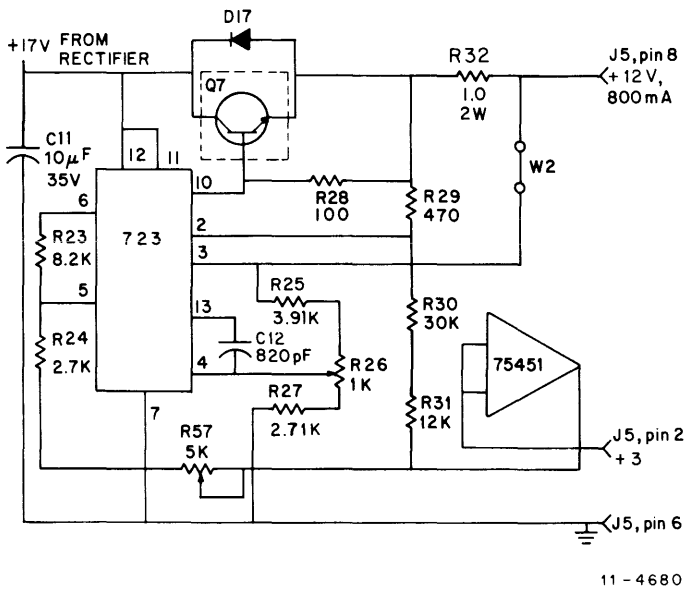


Figure 5-16 +12 V Regulator Circuit (Write Circuits)

The 723 is a precision voltage regulator. It is a two-level regulator, in that it can output two selectable voltages. Raw dc from the bridge rectifier network enters pins 12 and 11 of the 723. The TE16 write driver circuits require +12 V for NRZI. A high level is presented through J5, pin 2, to the inputs of the 75451, which outputs a high level through R57 by R23 and R24 and lets the full reference voltage from pin 6 of the 723 enter the noninverting input (pin 5). A +15 V output is produced.

The output (from pin 10) of the 723 is applied to Q7, where higher current is produced for the output. The current foldback and sense circuits operate in a manner similar to those of the +5.3 V regulator. Output voltage is divided by R25, R26, and R27 and is adjusted by R26. Resistor 57 is also a voltage adjustment. It adjusts the reference line to the 723. When adjustments are made, R26 must be adjusted before R57, because the reference voltage is dependent on the actual output voltage.

As output current increases, the voltage across R30 and R31 also increases. As the voltage reaches the limit of the 723, it is sensed at pin 2. The output from the 723 starts reducing, starting to shut off Q7 and keeping the output current from reaching unsafe levels.

No overvoltage protection is provided in this +12 power supply section because it is not necessary. The circuit that this supply feeds can stand voltage higher than this regulator can supply.

5.3.2.4 +12 Vdc Regulator Circuit (Control Switch Circuits) – The type 723 regulator used in this +12 V supply operates in exactly the same way as the previous 723 regulator (Figure 5-17).

In this +12 V regulator circuit, resistor R37 is the fine adjustment for the output voltage. Resistors R41, R39, R40, and R55 offer the sense for the current foldback network. The overvoltage network acts in the same way as the network in the +5 V supply, except the zener diode (D23) does not conduct until the voltage across it becomes greater than 15 V. Then the SCR fires and offers a path for output current, if Q8 becomes shorted for some reason.

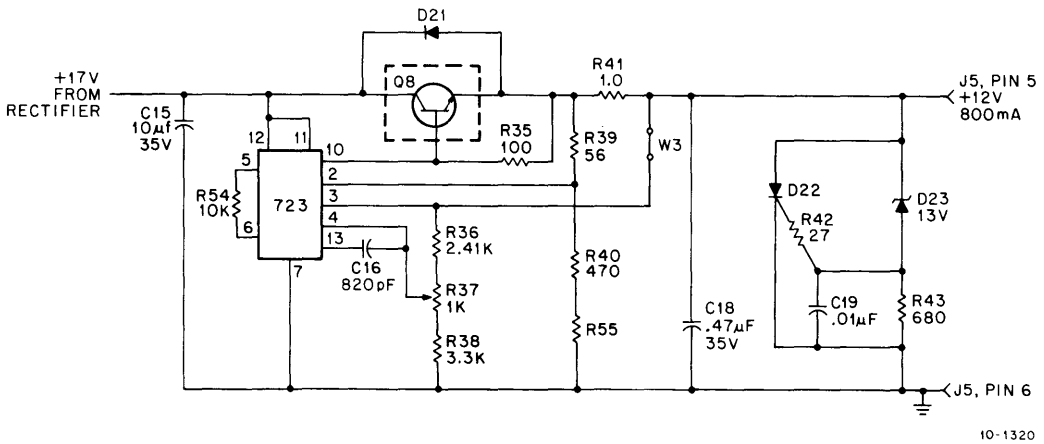


Figure 5-17 +12 V Regulator Circuit (Control Switch Circuits)

5.3.2.5 -6.4 Vdc Regulator Circuit – The TE16 power supply also furnishes a regulated -6.4 V (Figure 5-18). The LM304 is intended for systems requiring regulated negative voltages. Rectified negative voltage is presented to the LM304 from the negative output of the D11 diode bridge.

The LM304 output from pin 7 goes to the base of transistor Q11. Transistor Q11, connected with Q10, looks and acts like a normal PNP device; the combination supplies high current to the output.

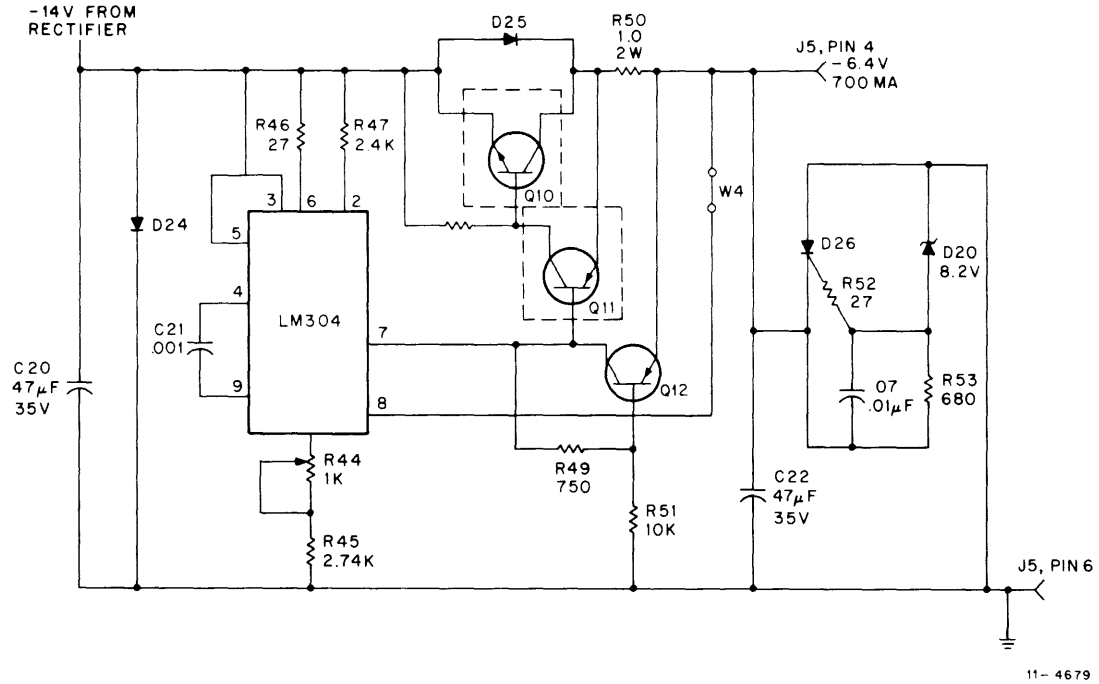


Figure 5-18 -6.4 V Regulator Circuit

Transistor Q12 is used in the current foldback network. Output current is sensed by R50, the V_{eb} of Q11, R49, and R51. As the output increases (becomes more negative), the voltage at the base of Q12 also increases (becomes more negative). Transistor Q12 starts to turn on and, as it does, shunts LM304 output current away from Q11-Q12, limiting output current. Then, as the output decreases, Q12 begins to shut off and allows the output current to rise again.

The overvoltage protection works identically to the other networks. Zener diode D20 begins conduction at approximately -8.2 V, which fires the SCR (D26) and creates a path to ground if Q10 and/or Q11 should short out. Again, the supply must be turned off to allow C22 to discharge before D26 stops conducting. Diodes D24 and D25 protect the LM304 against any over-voltage surges.

5.3.2.6 Specifications

Tables 5-2 and 5-3 list the power supply specifications.

5.3.3 G066 Module Description

The G066 Read Amplifier comprises a threshold generating circuit and nine identical read amplifier circuits, one for each tape track. This discussion references the G066 circuit schematic diagrams; refer to the relevant drawing(s) while reading this description.

5.3.3.1 Threshold Voltages - Sheet 1 of the G066 schematic illustrates the threshold voltage generation logic.

Table 5-2 Power Supply Input Specifications

Parameter	Specifications
Input Voltage (1 phase, 2 wires, and ground)	95–132/190–264 V
Input Frequency	47–63 Hz
Input Current	7 A nominal at 115 V, 60 Hz
Inrush	85 A at 115 V rms, 60 Hz

Table 5-3 Power Supply Output Specifications

Parameter	Specification
+5 V Regulator Circuit	
Load Range	10 A maximum
Overvoltage Crobar	6.4 V 10%
Current Foldback at 25° C	7 A nominal
Backup Fuse	15 A
Adjustment	5% minimum
Regulation	Less than 2%
+12 V Regulator Circuit (Write Circuits)	
Circuit Load Range	0.75 A
Overvoltage Crobar	None
Current Foldback at 25° C	0.5 A
Backup Fuse	1 A
Adjustment	35% minimum
Regulation	Less than 3%
+12 V Regulator Circuit (Control Switch Circuits)	
Load Range	0.75 A
Overvoltage Crobar	15.5 V 10%
Current Foldback at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%
-6.4 V Regulator Circuit	
Load Range	0.75 A
Overvoltage Crobar	8 V
Current Foldback at 25° C	0.75 A to 0.3 A
Backup Fuse	0.75 A
Adjustment	10% minimum
Regulation	Less than 3%

Figure 5-19 is an equivalent circuit of this programmable threshold logic. A type 74156 MUX uses a 2-bit code formed by signals WRE H and PES L to select one of the four A output lines. When an output line is selected, a low voltage is produced, which draws current through the resistor attached to that output. This sets up a reference current at the sensing node of the 324 operational amplifier. For example, if a select code of 0 (i.e., WRE H false and PES L true) is used, output A0 goes low. This places 3 V across a 30k resistor (from the +3 V reference at the noninverting 324 input) and draws .1 mA through it and feedback resistor R101. An output voltage is produced from the 324 (pin 7) that is slightly more positive than the +3 V reference; that voltage is approximately +3.3 V. The output feeds two additional sections of the 324 op amp, which provides current buffering. Pins 10 and 3 are non-inverting inputs, while pins 2 and 9 are inverting inputs. Pin 8 supplies the positive threshold (+TH) voltage (in this example approximately 3.3 V) to the threshold detection network. Similarly, the inverting amplifier (connected for a gain of 1) produces a positive voltage slightly less than +3 V from pin 1. This is again buffered and supplies the negative threshold (-TH) voltage (in this example approximate +2.7 V) to the threshold detection network. The chart on Figure 5-19 lists the approximate ±TH voltages produced by the possible selected inputs.

All of the threshold voltages are centered about a +3 V source. This is done to provide the use of the full dynamic ranges of the power supplies: +12 V and -6 V. By referencing +3 V, a full 9 V excursion can be used. The -TH is the same reference to +3 V as the +TH, only it is inverted.

One additional resistor can be used by the 74156. When the TE16 is reading PE records, the controller sends a signal called Interchange Read [IRD (SB)I] to the G066 over the slave bus. When true, the signal selects the B0 output of the 74156, placing a 12k resistor into the circuit. The result is a very low threshold voltage (+3.1 V, -2.9 V). This is done to try to pick up every bit of signal possible from the PE record. Signal IRD (SB) L is always negated in the gaps, so very little stray signal and spurious noise can be picked up. The signal becomes true in the middle of the record, thus picking up as much of the signal as possible.

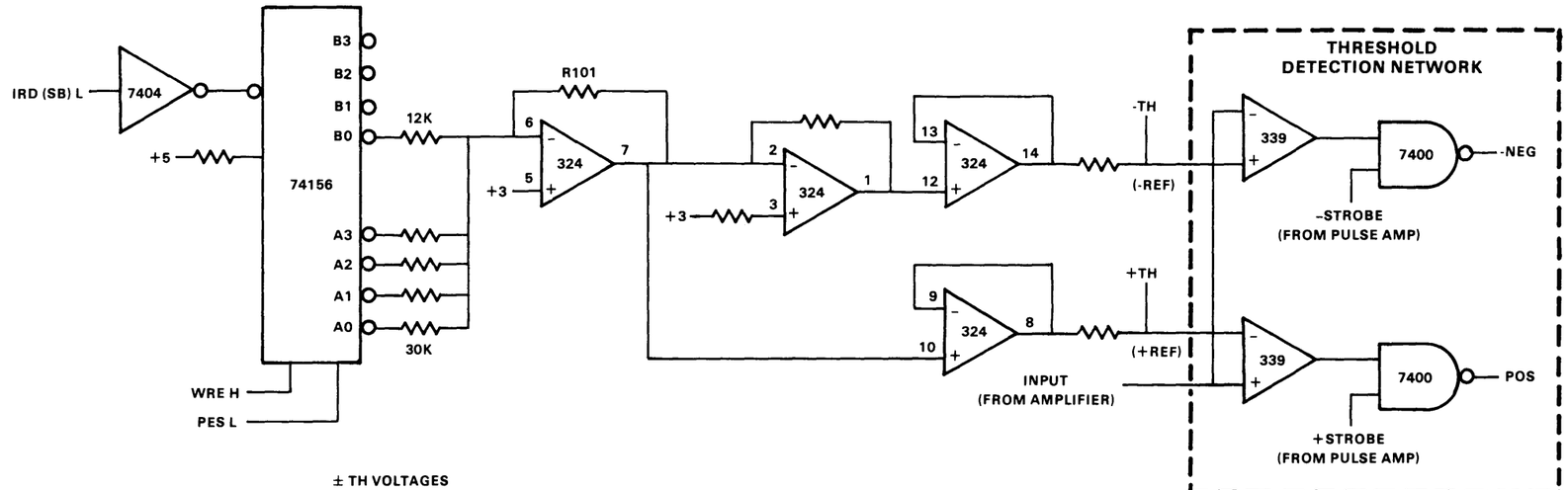
The PACKET H signal (G066, Sheet 1) is useful for maintenance purposes. It follows all of the data outputs, reflecting gap scatter, jitter, and skew. The signal is also sent to the M8911-YB or M8931 where it is used in formatting data characters in NRZI mode.

5.3.3.2 Read Heads and Amplifiers – Nine identical read amplifier circuits are on the G066 module, one for each tape track. Because these circuits are identical, just one is explained.

As tape moves past the read head, magnetic flux transitions on the tape cause the read head to produce voltage pulses. The direction of flux transition determines the polarity of the output pulses. The head signal inputs to the module (G066, Sheet 2 and Figure 5-20) at pins J1-15, and 16 and goes through a filter network to provide high frequency boost to the head signal. The filtering has little effect in NRZI mode, but it does accentuate the high frequency PE signals. Without the network, larger differences between the two signal amplitudes would exist.

The signal goes into a high gain /BW 733 amplifier. Adjoining track signals are decoupled from one another by the capacitor/inductor networks tied to voltage input pins 5 and 10. The gain adjustment (R56 for this track) is a 2k resistor between pins 4 and 11. All 9-track adjustments are accessible from the rear of the module.

The dual 733 outputs are further decoupled (on a dc basis) and input to a 318 operational amplifier, connected for a gain of 34. The inputs to the read head are relatively small (i.e., 12 mV p-p NRZI; 6 mV p-p PE). However, by the time they output from the 318 amplifier, the signal is approximately 12 V p-p. Only ac coupling is used from the 733, as the offset voltage coming from the 733 is removed by capacitors C35 and C36.



± TH VOLTAGES

	PES = 0		PES = 1	
	+TH	-TH	+TH	-TH
WRE = 0	3.9	2.1	3.3 SEE NOTE	2.7
WRE = 1	5.1	0.9	3.6	2.4

NOTE:

When IRD(SB)L is true (i.e., during PE Read), then
+TH = 3.1V
-TH = 2.9V

CP-3034

Figure 5-19 Programmable Threshold

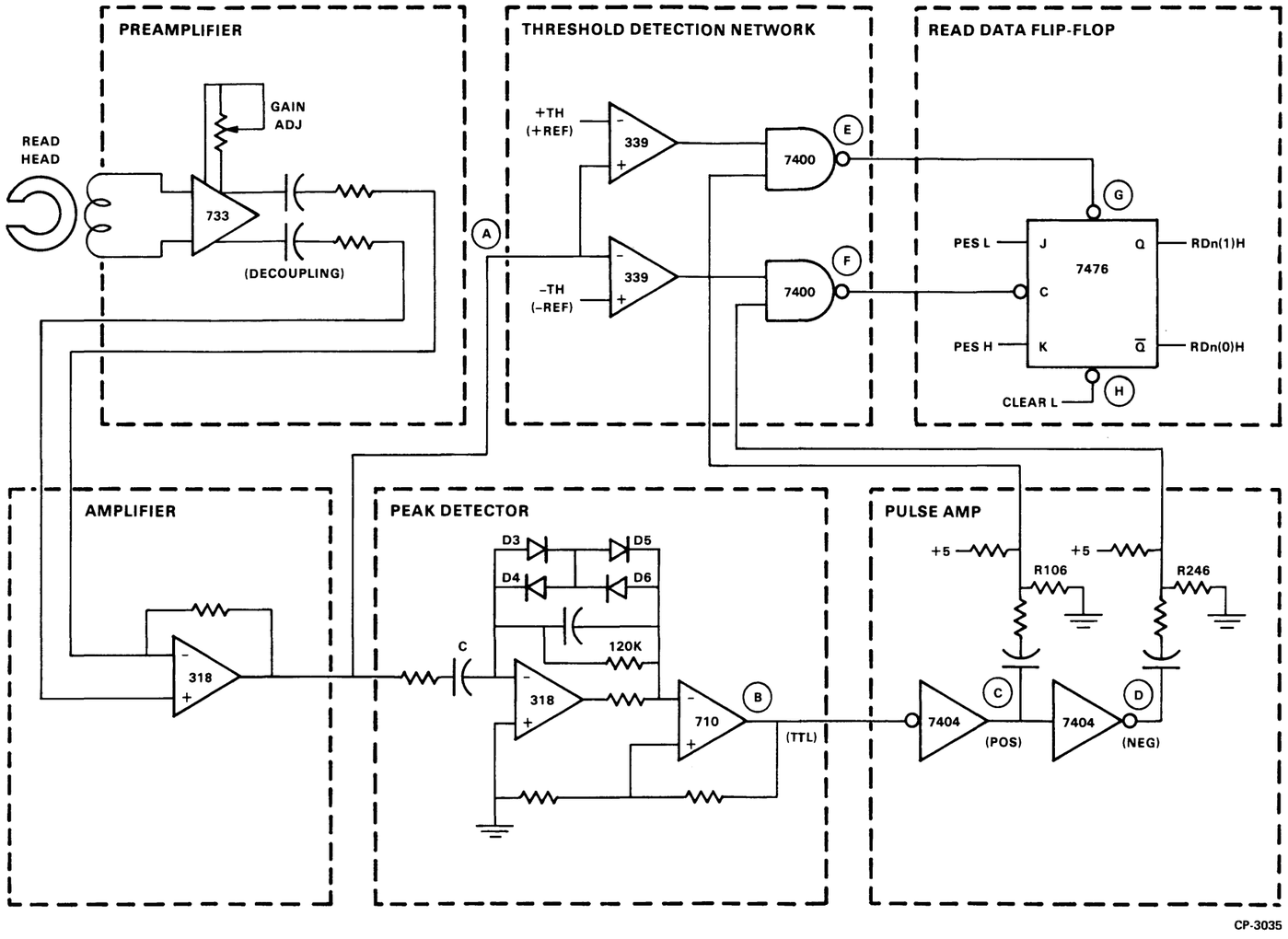


Figure 5-20 One Read Track Equivalent Circuit

The 318 output feeds two areas: peak detector and threshold detection network.

The threshold detection network comprises two type 339 comparators. The 318 amplifier output feeds the plus input of one comparator and the minus input of the other. This circuit detects if the amplifier out is either above the positive threshold voltage (+TH value) or below the negative threshold voltage (-TH value). Head signals do not pass through the comparators; the comparators only supply a logical high (only one can be true) to one leg of a 7400 NAND gate. The other input to the NAND gate is the head signal, after passing through the peak detector. Both a peak detector output pulse and a threshold qualification output are required to generate a POS or NEG signal (pulse) from the 7400s. The outputs of the 7400s (POS and NEG) are always low going, but they are responding to a positive or negative peak, respectively, from the tape.

The output of the 318 amplifier also feeds the peak detector, another 318. This circuit operates on the principle that the only place on a sinusoidal waveshape where the derivative of that waveshape is zero is at the peaks.

The 318 peak detector looks at the output of the previous 318 amplifier. When it has differentiated that output, the peak detector then looks for zero crossings; that is where the peaks occurred.

The 318 peak detector op amp is coupled through a capacitor from the second stage 318 amplifier. The current through that capacitor (e.g., C155) is C dv/dt. Therefore, the current going into the minus input of the peak detector is the derivative of the signal voltage. When the 318 output of the peak detector is close to ground, the feedback diodes (D3 to D6) are all open, leaving only the 120k resistor in the feedback path. If the signal voltage from the amplifier is a positive peak, then the current through C155 will be a small positive current pulse while the signal voltage is rising, followed by a transition through 0 A at the peak, and followed by a negative current while the voltage is decreasing (Figure 5-21).

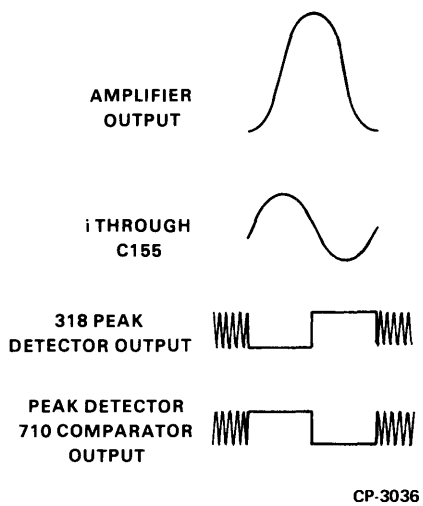


Figure 5-21 Peak Detector Waveforms

Therefore, the 318 peak detector output voltage first goes negative, until it is limited by the feedback diodes (D3, D5). Once the level reaches approximately -.7 V, the diodes turn on and clamp the level. This level remains until the signal voltage approaches its peak. When this happens, the current through C155 goes through its zero crossing (derivative of voltage signal is zero). Then, as the signal voltage starts down, the current through C155 is a small negative current pulse. Now diodes D4 and D6 limit the 318 peak detector output.

A 710 comparator completes the peak detector network. It accurately isolates the point where the transition at the output of the 318 portion of the network occurred and converts that ±.7 V swing to TTL levels.

The 318 peak detector output oscillates during signal gaps because dv/dt is also zero there. The 710 follows accordingly, and its output stabilizes. When the current through C155 reaches the zero crossing, the 318 goes from -.7 V to +.7 V and the 710 comparator output goes low.

This transition inputs to a pulse amplifier, comprising two 7404s; the second provides an inverted signal. The PA outputs normally sit at approximately +.4 V. When the peak detector fires, the outputs go to about 2.6 V and -1.4 V. If, for example, a positive signal voltage is being read, a -1.4 V pulse feeds the NEG 7400 NAND gate input and a +2.6 V pulse feeds the POS 7400 NAND gate input (Figure 5-22).

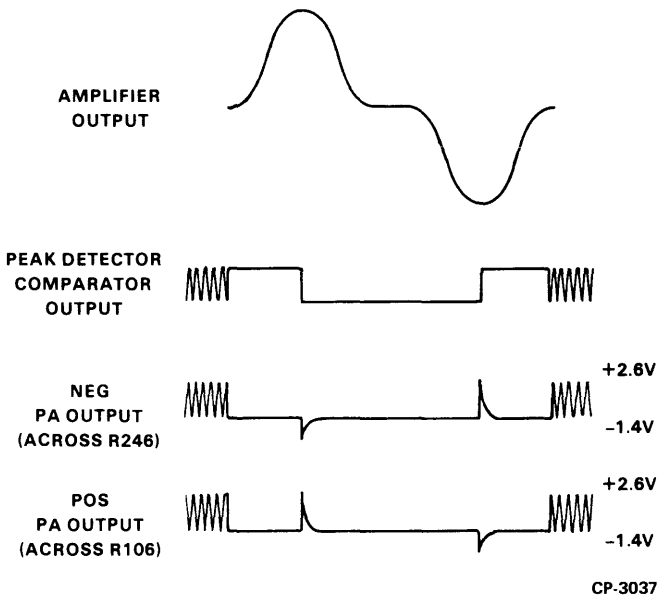


Figure 5-22 POS and NEG Waveforms

Until this time, the G066 operates the same for either PE or NRZI read data except, of course, for the threshold. The setting of the various read data flip-flops is where the difference occurs.

In NRZI mode, a low pulse from either POS or NEG sets the read data flip-flop to the 1 state, either by direct set (POS) or by the clock input (PES L is high in NRZI mode). Therefore, any pulse going through the read amplifier chain sets the flip-flop.

The PACKET signal is sent to the M8911-YB (or M8931) to help format the data. The result is that signal CLR READ BOARD L, generated on the M8911-YB, is sent to the G066 (Sheet 1) and asserts signal CLEAR L. This signal clears the read data flip-flop at the end of the data character period.

Figure 5-23 shows the waveforms of the various designated areas of the read amplifier circuit (Figure 5-20). The read data flip-flop functions differently in a PE Read operation (Figure 5-24). A pulse at the POS output of the threshold detection network sets the 7476 J-K read data flip-flop. Accordingly, a pulse at the NEG output clears the flip-flop, because when reading in PE mode, the J input (PES L) is low and the K input (PES H) is high. The output of the read data flip-flop follows the polarity of the magnetic field on the tape; it contains the data in phase encoded (PE) form.

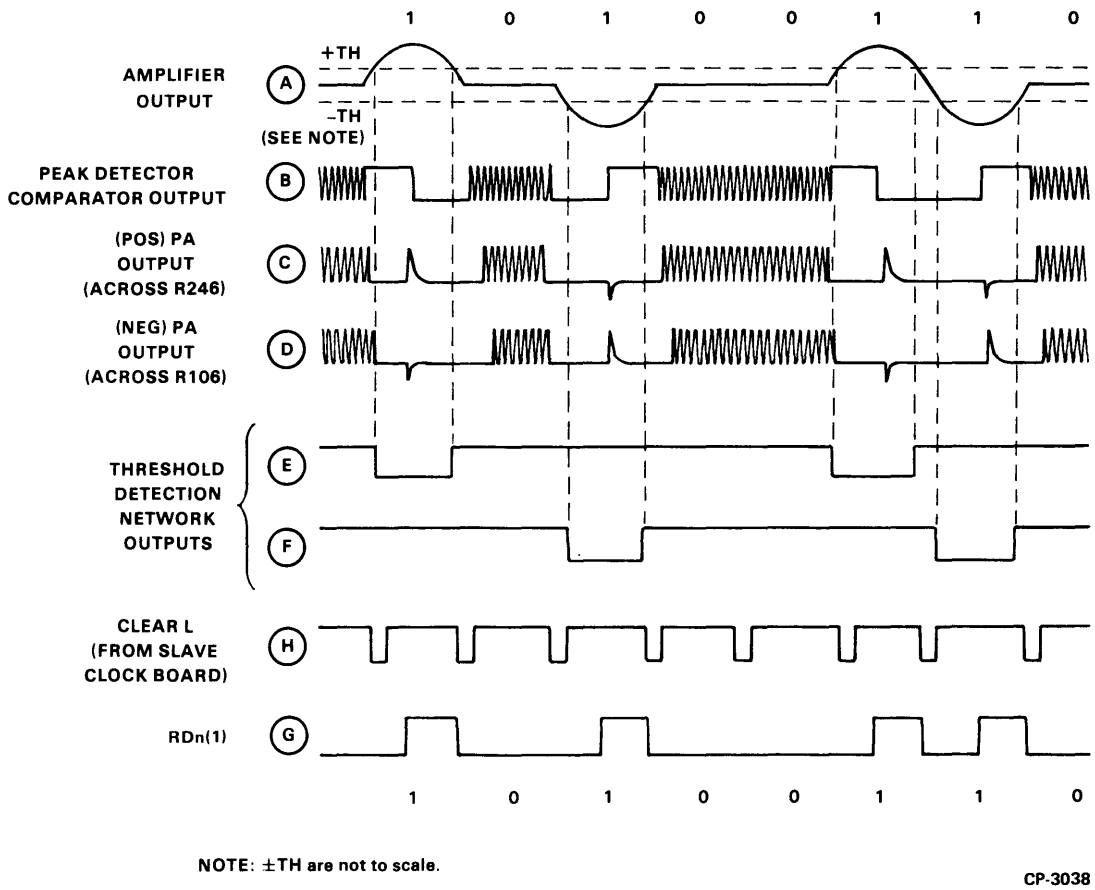


Figure 5-23 Read Amplifier Waveforms (NRZI)

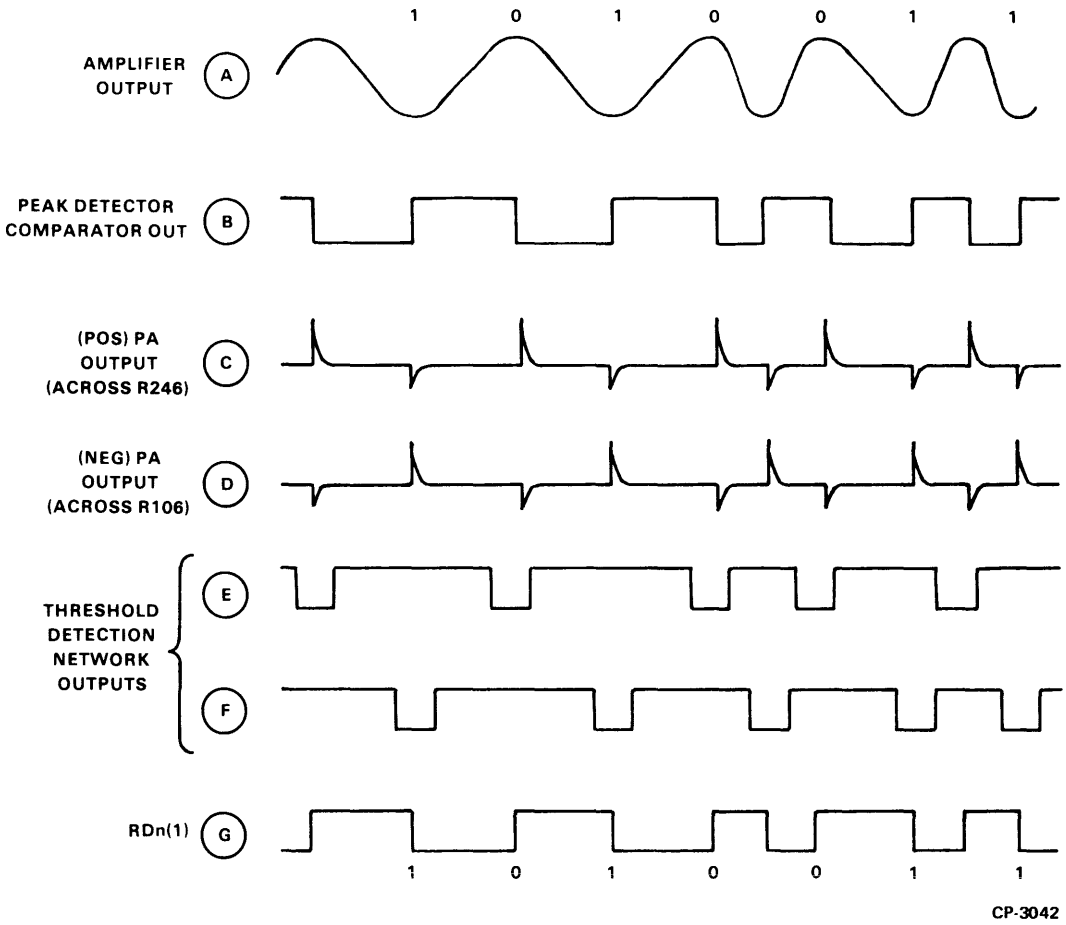


Figure 5-24 Read Amplifier Waveforms (PE)

5.3.4 M8911-YB/M8931 Slave Clock and Motion Delay

All free-running clock waveforms used in the TE16/controller system are generated by a 2.3 MHz, crystal controlled clock located on the slave clock and motion delay (SC) module (M8911, M8911-YB, M8931). The 2.3 MHz clock is divided down to 144 kHz and is transmitted to the controller over the slave bus [CLOCK (SB)] by any TE16 that is on-line and selected. The 144 kHz frequency has been used, because it is the highest frequency clock needed by the controller; 144 kHz is twice the 1600 bits/in data rate.

5.3.4.1 Write Clock - With a controller, the TE16 is capable of reading and writing data at several bit densities. In order to read and write at various bit densities, a separate clock signal is developed: signal WRT CLK (drawing SC3). WRT CLK is transmitted to the controller by an on-line, selected TE16 whenever the ACCL (SB) L control signal is negated by the controller.

WRITE CLOCK is generated in the following manner. A number is preset into a 74161 (synchronously loaded) binary counter (SC3), which is then counted up at 575 kHz. When the counter overflows, WRT CLK H is asserted, which causes the counter to preset at the leading edge of the next 575 kHz clock pulse. With the counter preset, WRT CLK H is negated by the trailing edge of the same 575 kHz clock pulse. The counter clocks as before, until an overflow, and the cycle is repeated.

The presets of the 74161 counter are determined by combinations of the various signals listed in Table 5-4. Also listed in Table 5-4 are the resulting counter presets, the WRT CLK frequency, and the density. Note that the WRT CLK frequency for 1600 bits/in is four times that of 800 bits/in. This is because 1600 bits/in is used only in PE mode, and PE mode requires a double WRT CLK frequency.

Table 5-4 Write Clock Frequencies

	DEN 2	DEN 1	DEN 0	Test PE	Test DEN	WRT CLK Counter Presents LSB MSB	Frequency kHz (bits/in)
On-Line	0	0	0	1	1	10000011	9 (200)
	0	0	1	1	1	01010111	28 (556)
	0	1	0	1	1	10001111	36 (800)
	0	1	1	1	1	10001111	36 (800)
	1	0	0	1	1	10111111	N/A
	1	0	1	1	1	00111111	N/A
	1	1	0	1	1	10111111	N/A
	1	1	1	1	1	10111111	N/A
Off-Line	x	x	x	0	0	01010011	10.7 (238)
	x	x	x	0	1	10001111	36 (800)
	x	x	x	1	0	00111111	N/A
	x	x	x	1	1	10111111	N/A

The frequency of the counter cycle varies with the magnitude of the preset. Figure 5-25 shows timing diagrams for presets of -1 (-n = 2's complement of n), -2, and -3. Note that for a preset of -n, the frequency of WRT CLK ($f_{WRT\ CLK}$) = [575/(n + 1)] kHz.

5.3.4.2 Motion Delay - The slave clock and motion delay module also generates presets for the motion delay counter in the controller. Simultaneous with tape motion initiation, the controller generally asserts signal EMD (SB) L (Enable Motion Delay). This signal gates the motion delay presets onto the read data lines (SC2) of the slave bus and loads them into the controller motion delay counter. When EMD L is negated, the counter is counted up until it reaches a count of 2^{14}, at which time signals ACCL H and READING L are asserted; all further clocking is inhibited. The presets of the counter determine the time interval necessary to reach the count of 2^{14} and hence the duration of the motion delay.

All presets depend on the type of operation (e.g., read/write) performed, the direction of tape motion, and some additional parameters. Table 5-5 lists the motion delays generated under the various conditions.

The READING L signal enables the read circuitry in the controller. ACCL L is sent to the TE16, where it enables generation of WRT CLK and other read and write functions.

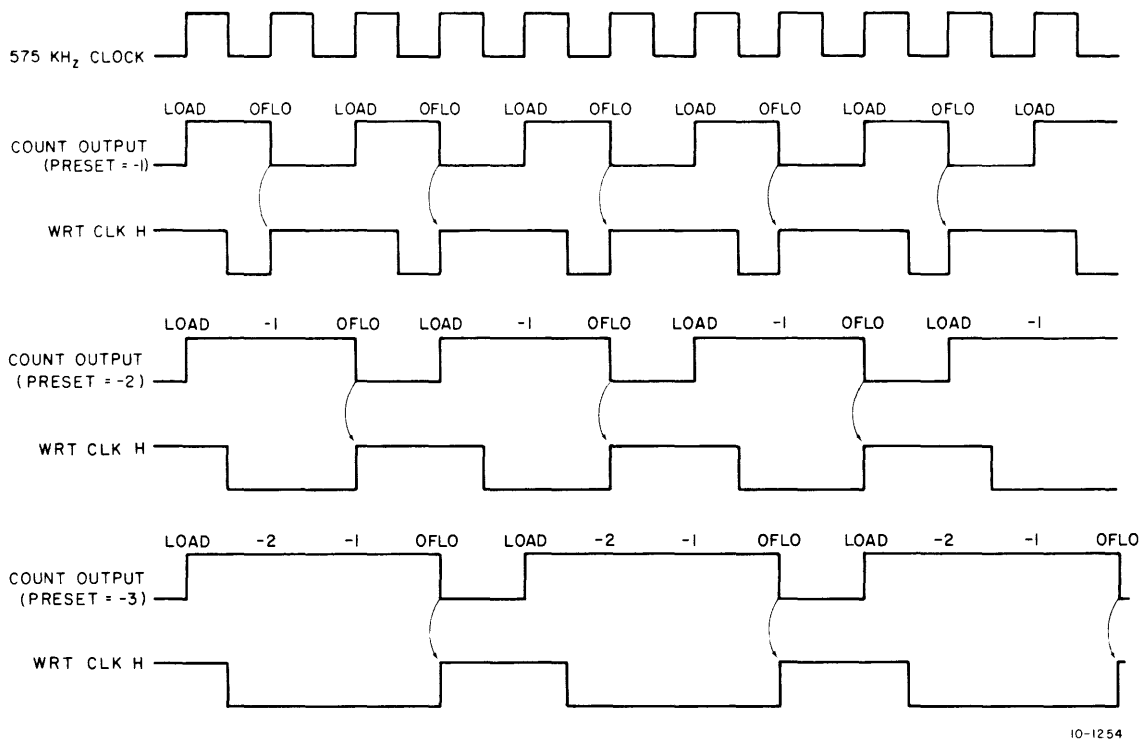


Figure 5-25 WRT CLK Generation Timing

Table 5-5 Start and Stop Motion Delays

Start/Stop	Mode	Operation Time (ms)	
		9-Track	7-Track
Start Motion Delays	Write from BOT	184.60	200.70
	WRITE	8.99	15.26
	Read from BOT	150.60	86.94
	READ/SPACE FWD/SPACE REV	2.72	.92
Stop Motion Delays	WXG/WFMK/WRITE	2.72	2.72
	READ/SPACE FWD/SPACE REV	1.82	1.82

When the end of each data record is detected by the TE16's controller, a shutdown sequence is started. Again, EMD L is asserted, initiating a stop motion delay. EMD L loads the motion delay counter with presets gated by the TE16 onto the read data lines of the slave bus, just as occurred during motion initiation. The presets, however (again refer to Table 5-4), are different during start and stop delays.

5.3.4.3 Read Strobe Generation - The M8911 generates the Read Strobe Read Skew [RSDO (SB) L Delay Over], and generates the CLEAR READ BOARD signal in NRZI mode. In PE mode, this read strobe generation circuitry is inoperative, because the controller does the entire job of data recovery.

The manner by which read strobe can be generated is: The eight-input NOR gate, together with a two-input OR gate, are used to generate the logical OR of all digital read signals. Whenever one of the digital read signals becomes asserted as the result of a signal read from tape, a flip-flop is set that loads the two-chip counter E23 and E28. The value loaded into this counter is provided by the Clock PROM and is dependent upon the density code and the signals WRITE ENABLE and IRD. In general, the counter is preset to a value such that it overflows in precisely 50 percent of one data cell time. However, when signals WRITE ENABLE or IRD are asserted, the preset value is altered so that the counter overflows in 35 percent of one data cell time.

When the counter overflows, the Skew Delay Over signal is asserted. Assertion of this signal generates the CLEAR READ BOARD pulse, enables the sending of RSDO back to the controller, and loads a second delay into the counter. This delay is also variable. It is generally approximately one microsecond long. However, if IRD or WRITE ENABLE is asserted, this second delay is increased to approximately 50 percent of one data cell time and forms a NO TRESPASS ZONE, during which no data pulses are expected. Occurrence of a data pulse during this interval results in assertion of the SET VPE signal. Thus, the skew delay circuitry is less tolerant of jittery or skewed data in the WRITE or IRD modes.

Once the NO TRESPASS ZONE time is over, the skew delay counter returns to a state in which it simply awaits the next detection of a data bit.

5.3.5 M8912 Module Description

The test function generator (TFG) module (M8912) is used for off-line testing of the TE16 tape transport. During normal, on-line operation of the TE16, the TFG is only used to transmit the serial number and certain drive-type bits to the tape controller; to do so, it must be located in section EF of slot 3 of the TE16 backplane. The serial number and drive-type information required is wired on the backplane at this location. For use as an off-line tester, the TFG module must be moved to section AB of slot 3.

An operating procedure for the TFG is presented in flow chart form in Figure 5-26. Figure 5-27 provides additional information on TFG switch settings. The TFG module is illustrated in Figure 5-28.

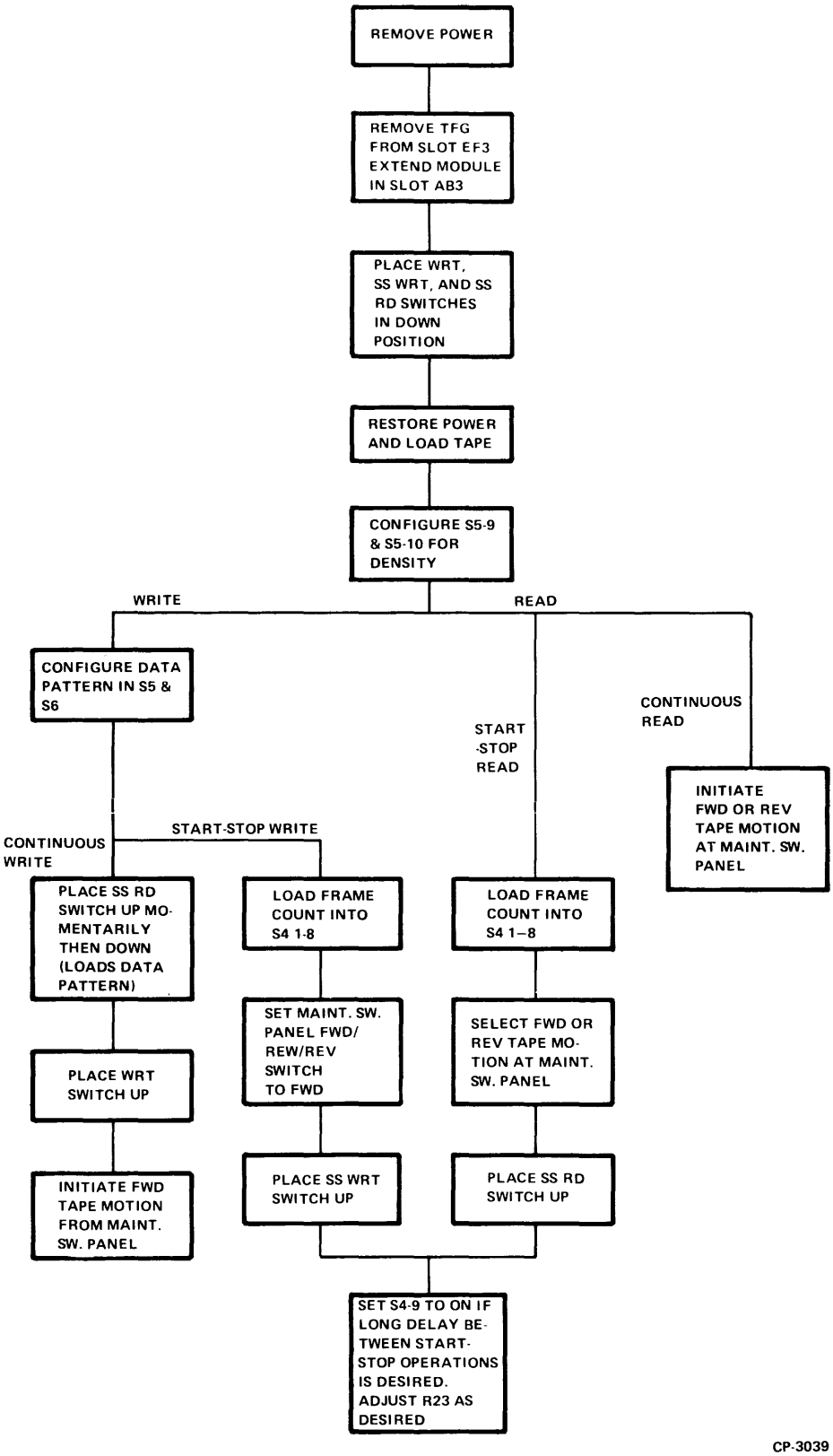
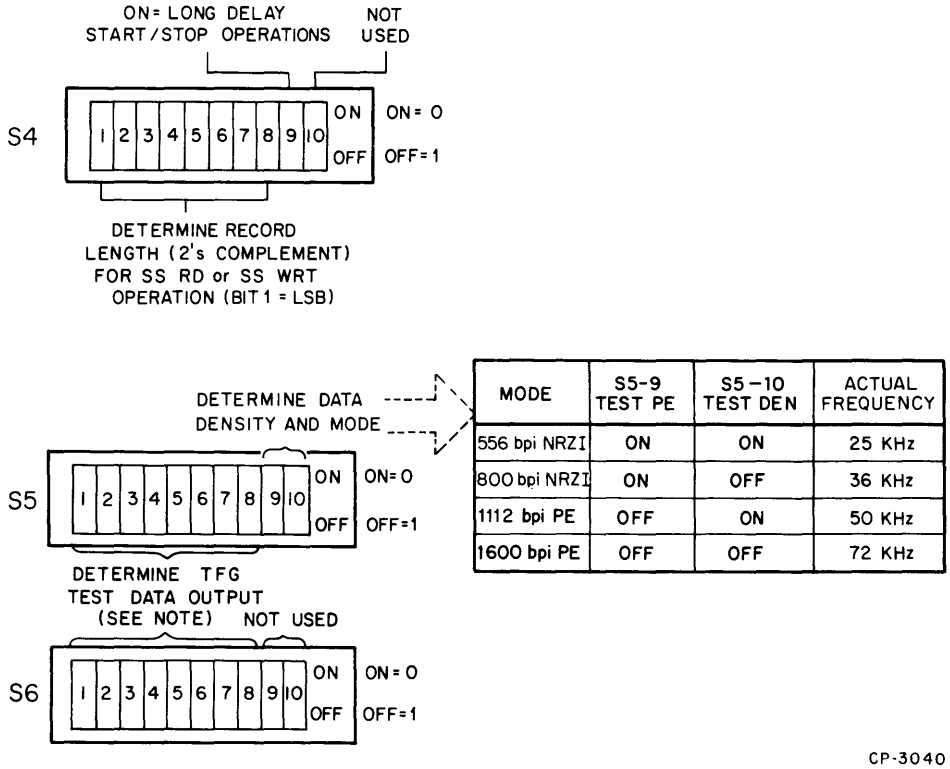


Figure 5-26 TFG Operating Procedure Sequence



MODE	S5-9 TEST PE	S5-10 TEST DEN	ACTUAL FREQUENCY
556 bpi NRZI	ON	ON	25 KHz
800 bpi NRZI	ON	OFF	36 KHz
1112 bpi PE	OFF	ON	50 KHz
1600 bpi PE	OFF	OFF	72 KHz

Figure 5-27 TFG Switch Settings

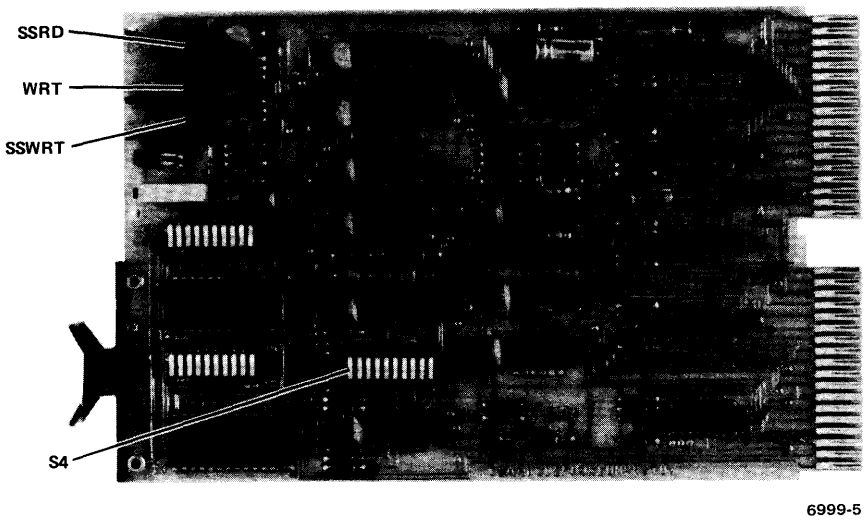


Figure 5-28 Test Function Generator Module

As an off-line tester, the TFG module (Figure 5-28) controls tape motion, enables TE16 read and write circuitry, and generates test patterns to be written on tape. Three modes of operation are possible.

1. Start-Stop Read (SS RD) - When the SS RD switch (S3) is activated (raised), tape motion is initiated; a record of predetermined length is read; tape motion is then terminated. This cycle is repeated as long as the SS RD switch is up.

2. Start-Stop Write (SS WRT) - When the SS WRT switch (S2) is activated (raised), tape motion is initiated; a record of predetermined length, consisting of preselected characters, is written on tape; tape motion is then terminated. This cycle is repeated as long as the SS WRT switch is up.

3. Continuous Write (WRT) - When the WRT switch (S1) is activated (raised), power is supplied to the write drivers and they are continuously driven with a preselected pattern. Tape motion is controlled from the maintenance switch panel.

When the tester card is located in the TE16, location AB, the pin labeled TESTER ENABLE L is at ground potential (Drawing M8912, Sheet 3). This enables the TEST PE H and TEST DEN H switches. With the LED on, the TEST PE H and TEST DEN H switches affect the recording density as controlled by the M8911-YB slave clock module. The TESTER ENABLE L level asserts LOCAL H, preventing the transport from going on line.

An 8-bit counter, constructed from two 74197 up-counters, controls a preset record length. The preset count is entered from the S4 switches S4 (1 to 8). Both the SS RD and SS WRT functions use the counter to control record length. The WRT function is continuous and does not use a preset panel.

A 16-bit shift register, constructed from two 74199 8-bit shift registers, allows various data test patterns to be generated. Switches on S5 and S6 select the data pattern to be loaded into the register. When shifted out, the test data patterns (TEST DATA A, H, and L and TEST DATA B, H, and L) are wired to the data multiplex on the LAW module (M8916) and written on tape.

The start-stop repetition rate during SS RD and SS WRT can be modified by adjusting R23. The range of adjustment is determined by switch S4, segment 9.

5.3.5.1 Theory of Operation - The following paragraphs describe the theory of operation of the TFG module in its three functional modes. The discussions reference the TFG schematic (TFG 3).

1. **SS RD Function** - Figure 5-29 illustrates the SS RD function timing. When the SS RD switch (S3) is closed, E1 - pin 10 goes low and triggers the first one-shot delay. FIRST ONE SHOT L, input to the LAW module (M8916), initiates tape motion; the direction of tape motion is determined by the direction switch on the TE16 maintenance switch panel. FIRST ONE SHOT also presets the 8-bit counter (E15 and E22) and loads the 16-bit shift register (E13 and E23).

   When the first one-shot delay times out, flip-flop E8 is clocked set and asserts WRT CLK TEST ENB L. This signal is used in the slave clock and motion delay module (M8911-YB) to enable WRT CLK and RECORD PULSE L pulses. The RECORD PULSE L pulses now clock the TFG 8-bit counter and 16-bit shift register. When the counter overflows, the third one-shot delay is triggered and engages WRT CLK TEST ENB L, inhibiting further RECORD PULSE L pulses.

   When the third one shot delay times out, FOURTH ONE SHOT H is generated and causes tape motion to terminate. When the fourth one shot delay times, the first one shot is again triggered; the cycle begins again. The start-read-stop cycle continues as long as the SS RD switch is depressed.

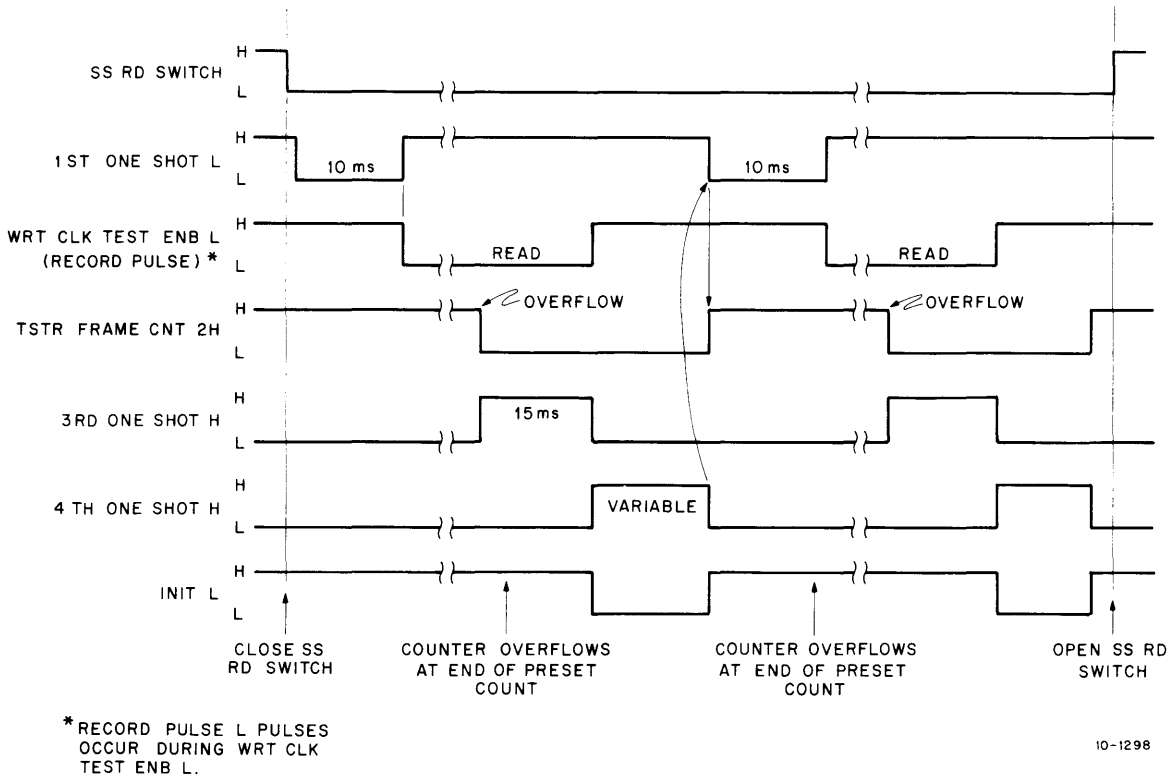


Figure 5-29 SS RD Function Timing

2. **SS WRT Function** – Figure 5-30 illustrates the start-stop write function timing. The SS WRT function operates in a manner similar to the SS RD function, except that SET TEST WRE L is asserted along with WRT CLK TEST ENB L. SET TEST WRE L causes the write and erase heads to be energized. When RECORD PULSE L pulses clock the shift register (E13 and E23), the contents of the register are rotated. The shift register outputs (TEST DATA A, H, and L and TEST DATA B, H, and L) are jumpered to the LAW data write multiplex and written on tape.

3. **Continuous Write Function** – The continuous write function works differently than the SS WRT function in that in the continuous test mode, no starting and stopping occurs. One continuous write operation commences with the setting of the WRT switch and ends with the opening of the switch. Tape motion (starting and stopping) is controlled at the TE16 maintenance switch panel.

   As the WRT switch is closed, WRT CLK TEST ENB L and SET TEST WRE L are asserted. This enables RECORD PULSE L pulses and passes write current to the heads. The 8-bit counters are not used in a continuous write operation. Instead, the shift registers are clocked by inverted RECORD PULSE L pulses, and whatever data pattern was in the shift register switches is shifted out on the TEST DATA lines to be written and observed. The THIRD ONE SHOT delay is inhibited, which eliminates the start-stop operations.

   If the operator desires a test data pattern other than the pattern presently in the shift register switches, he must first run an SS RD operation with the desired test data pattern. It is the only method for loading new information from the switches into the shift register.

   The continuous write operation continues until the WRT switch is opened; this clears the WRT flip-flop and removes the write current and record pulses.

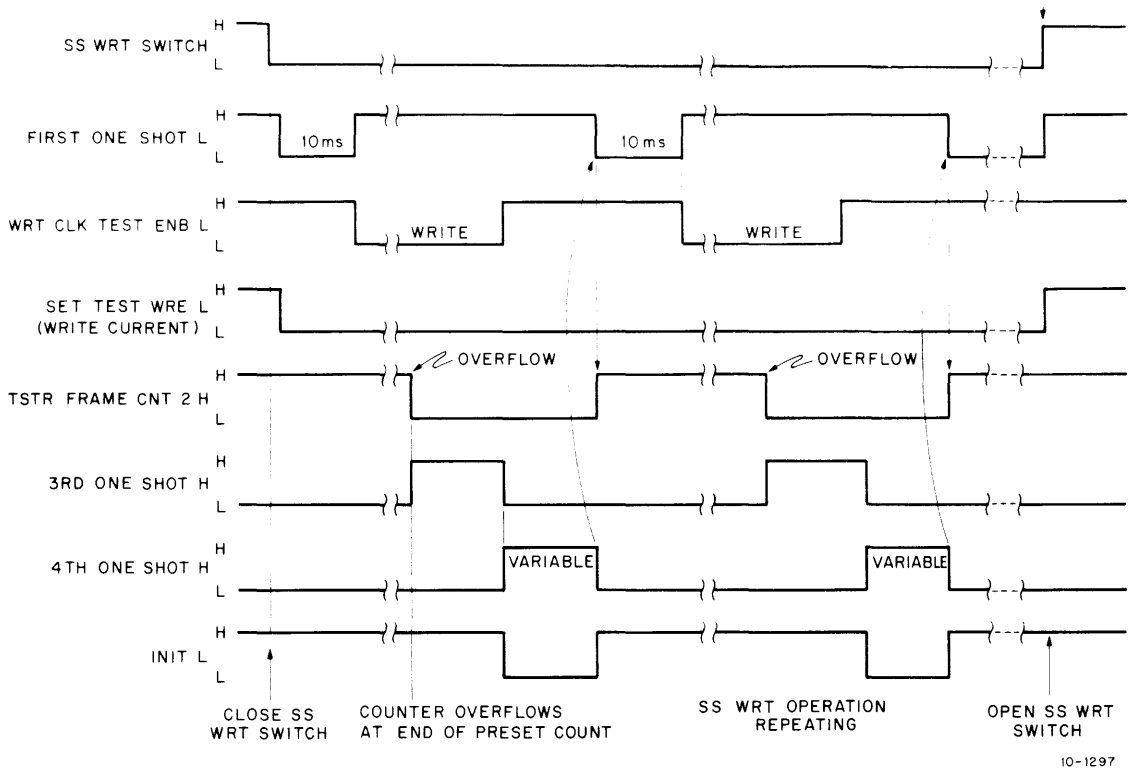


Figure 5-30 SS RD Function

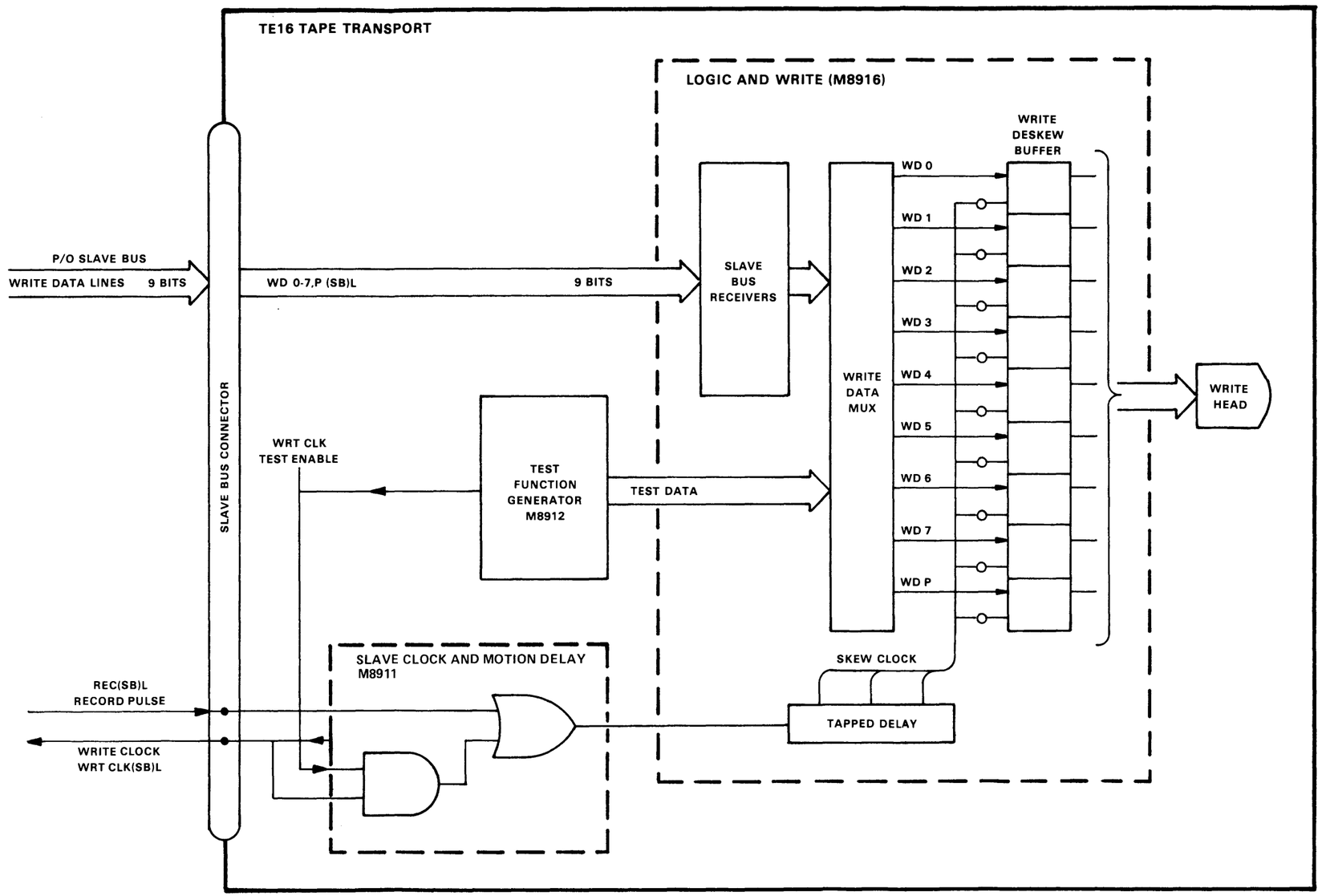
5.3.6 M8916 - Logic and Write Module Description

The logic and write (LAW) module (M8916) interfaces the tape controller motion control signals, status signals, and write data path to the TE16. It also controls the loading sequence and initiates the unloading sequence.

5.3.6.1 Write Data Path - Input to the LAW circuitry of each track is the data line corresponding to that track and a delayed RECORD pulse. (The delay is prewired and corrects for static write skew inherent in the write head.) PE write data has been formatted (converted from binary to PE mode) in the controller. NRZI write data is still in binary mode and is converted (formatted) to NRZI mode (transition for 1s; no transition for 0s) in the LAW module. The write data signals are then applied to the write head.

The write data path within the TE16 is shown in Figure 5-31. Once the slave bus write data line signals are received by the slave bus receivers, they are sent to the write multiplexer. The output from the write multiplexer is then clocked into the write deskew buffer. Note that the M8912 TFG module can also supply data to the write deskew buffer for off-line test purposes (Paragraph 5.3.5).

In NRZI mode, a clock pulse occurs once for every character written on tape. The data is presented to the drive in terms of 1s and 0s, and the drive must format the data stream. In PE mode, the clock occurs twice for every character written: once when normal data is output from the write multiplexer and once again when inverted data is output from the write multiplexer. In this mode, all formatting is done in the controller, prior to the data being sent to the drive. PE write data goes out on the data lines in the same waveshape as will be read back. The double clocking operation produces phase encoding (in PE mode).



NOTE:

WRT CLK also goes to M8912 and REC pulse can be generated by M8912.

CP-3041

Figure 5-31 Write Data Path

Figure 5-32 shows the timing of the write operation for NRZI and PE mode.

Timing for both on- and off-line write operations is derived from WRT CLK, which is generated in the TE16 by the MB911-YB or M8931 modules and transmitted to the controller. WRT CLK is then gated in the controller to produce RECORD pulses, which are transmitted back to the TE16. The RECORD pulses are input to a tapped delay, which outputs to the clock inputs of the write deskew buffer. This arrangement provides write deskew; it compensates for dimensional tolerances inherent in the manufacture of tape heads. These tolerances prevent all the tape tracks from ideally lining up.

The write deskew buffer circuitry also converts the binary NRZI data into its NRZI form (i.e., transition for 1s; no transition for 0s). The write deskew buffer output is then driven to the write heads.

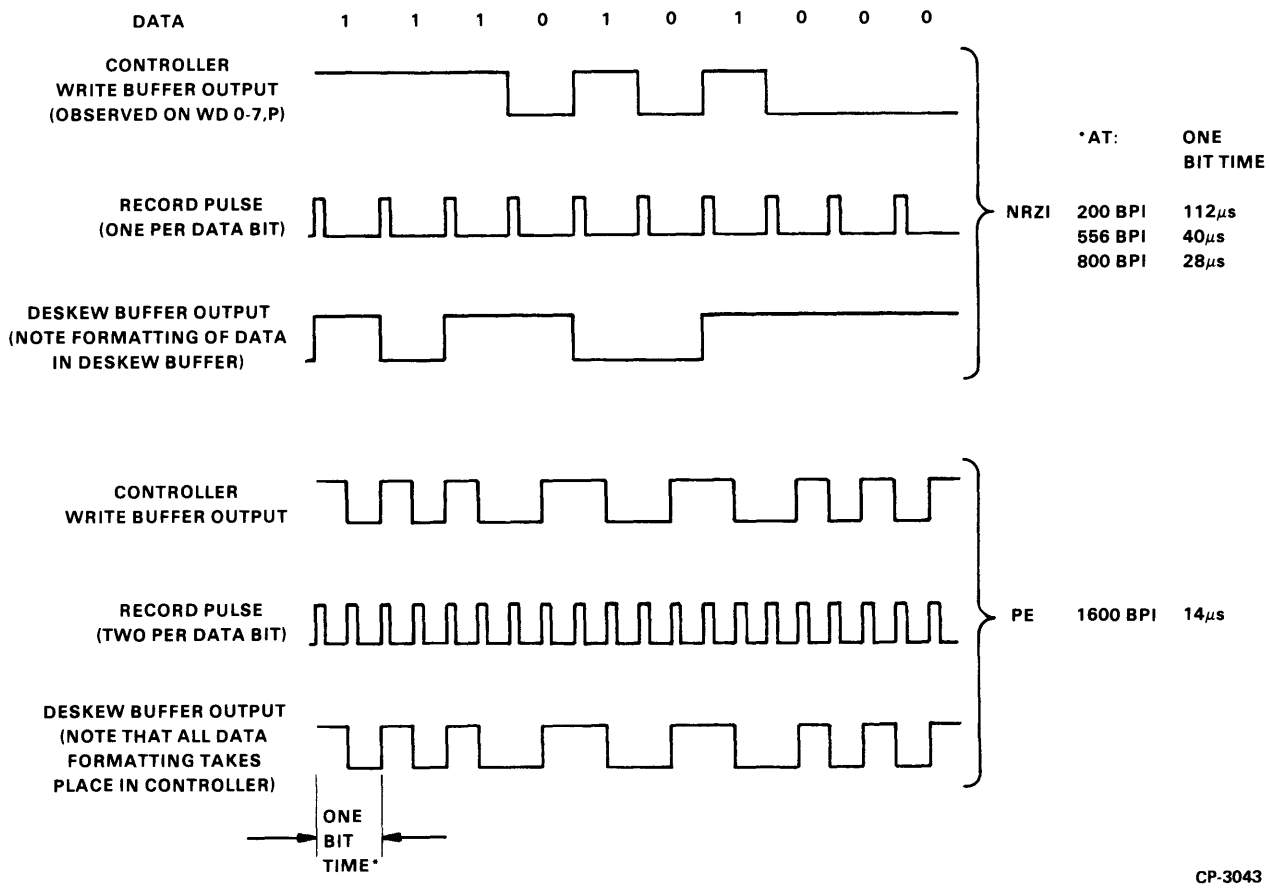


Figure 5-32 Write Operation Timing

5.3.6.2 Tape Motion – The signals that control the power board (H607), which, in turn, controls capstan and tape reel motion, are generated on the LAW module. The LAW module contains motion control flip-flops and various sequencing circuits. The sequencing circuits provide smooth mechanical operation, protecting both data and hardware. The flip-flops enable reel motion and vacuum operation, determine the direction and speed of capstan rotation, and control panel indicators. These flip-flops are controlled by the tape controller via the slave bus when the TE16 is on-line and by the TE16 control panel and maintenance panel when the transport is off-line. When the TE16 is on-line and receives a motion/write command from the controller, the flip-flop(s) corresponding to that command is set upon receipt of the DRV SET pulse, at which time the motion will commence and the write amplifiers become enabled. Receipt of the STOP L signal from the controller causes the motion flip-flops to reset, and the motion terminates. Note that if the STOP L signal is never negated, motion and write enable flip-flops cannot be set.

The motion control logic is illustrated on the M8916 (LAW) drawings. The remainder of the discussion of the motion control logic uses the M8916 drawings to complement the text.

5.3.6.3 Power Clear – The power clear circuitry is a "power-low" detector. When the +5 V power supply is turned on, the circuit asserts P CLR L until the logic supply stabilizes at +5 V. This results in the resetting of all the various status flip-flops in the TE16 to the idle state, unloaded, off-line condition; keeps all motors turned off; and asserts braking on the reels. Similarly, whenever the +5 V power supply drops to approximately 4.5 V, P CLR is asserted until the power supply either drops too low to operate the power clear circuitry (approximately 3 V) or rises back above the trip voltage (4.5 V).

5.3.6.4 Servo System Failure Detection – Two fail-safe switches, located in each vacuum-buffer column, define the permissible limits of tape excursion into those columns. If the tape loop in either buffer column goes below its lower fail-safe switch, the switch opens and signal LFS H is asserted. If either tape loop travels above its upper fail-safe switch, then that switch closes and asserts UFS L. When VACUUM ON (0) L is asserted, indicating that tape is loaded and either LFS H goes low or UFS L goes H, then the FAIL flip-flop (LAW 3) is set. The effect of FAIL (1) H is essentially the same as that of the P CLR pulse, except that FAIL (1) H is a level and remains asserted, preventing tape unit operation until manually reset by pressing the LOAD switch on the TE16 control panel.

5.3.6.5 Loading Sequence Logic – Initiation and shutting down of the reel motors, brakes, and function control logic is controlled by the loading sequence logic. The loading sequence logic consists of the RELAY ENABLE flip-flop, the REEL MTR ENABLE L, and VACUUM ON L one-shots and their associated logic. The RELAY ENABLE flip-flop is reset by either FAIL (1) or the pressing of the REW/UNLOAD switch at the initiation of an UNLOAD sequence. When RELAY ENABLE is reset, the vacuum motor is turned off. Also, power to the reel and capstan motors is turned off. The REEL MTR ENABLE L one-shot is held to its 1 state, negating REEL MTR ENABLE L; the VACUUM ON L one-shot is held to its 1 state, negating VACUUM ON L. These prevent the function control logic from responding to any command.

The RELAY ENABLE flip-flop is set by signal LOAD PULSE (1) H, a signal produced when the LOAD switch is pressed and released. When the RELAY ENABLE flip-flop is set, the vacuum motor is turned on and power is applied to both the reel motor drive circuits (+17 V INT power line is connected to +17 V unregulated supply) and the capstan motor drive circuit (PWR COMMON INT power line is connected to power common). As soon as the RELAY ENABLE flip-flop is set, the VACUUM ON one-shot begins to time out. This one-shot provides a "grace period," during which the vacuum motor is allowed to accelerate to its running speed. Tape can be loaded into the vacuum columns (tape loading is accomplished on the H607) during this period. Once vacuum is established and tape is loaded in the buffer columns, the LFS H signal goes low as vacuum pulls both lower fail-safe switches closed. When LFS H does go low, the REEL MOTOR ENABLE one-shot begins to time out. Approximately 100 ms later, the REEL MOTOR ENABLE one-shot times out, allowing the reel servos to control reel motor motion.

Finally, the "grace period" expires as the VACUUM ON one-shot times out. If the load sequence has been successful, both upper fail-safe switches are open (no vacuum at their intake ports), causing the UFS L signal to be high. Also, both lower fail-safe switches are closed, causing the LFS H signal to be low. The assertion of VACUUM ON does not clock the FAIL flip-flop. At this time, the LOAD indicator glows and the seek-for-BOT sequence is initiated.

If the load sequence has not been successful and all four fail-safe switches are not in the appropriate operating state, assertion of VACUUM ON clocks the FAIL flip-flop to the "1" state, thus clearing RELAY ENABLE and all its associated logic.

5.3.6.6 Brake Release – When the FORCE BRAKE ON (1) L delay signal is asserted, full braking is applied to both reels. It is triggered by the assertion of the FAIL signal and lasts for approximately 4 seconds. When the delay times out, the brakes are released. FORCE BRAKE ON is also asserted during the power-on sequence

5.3.6.7 Rewind Control – Due to the limited rate at which the reels can be accelerated and decelerated, a special sequence of control signals must be generated to perform a high-speed rewind operation. The sequence is shown in Figure 5-33. When the function control logic accepts a rewind command, it asserts (Drawing LAW 5) signal SET RWD CMD L, which direct-sets the Rewind Status (RWS) flip-flop.

A high level is presented to the pin 12 input of the 7400 gate in location E41 (LAW 3). This asserts signal REV/REW H, which accelerates the capstan servo to 1.14 m/s (45 in/s) in the reverse direction. At the same time, RWS (1) triggers a 200 ns delay, which allows the reels to stabilize at 1.14 m/s (45 in/s). When the delay times out, it asserts signal REWIND CAP H. The REWIND CAP H signal causes the capstan servo to gradually accelerate to 3.8 m/s (150 in/s) in the reverse direction. Approximately 10 seconds are required to achieve full rewind velocity. Normally, rewinding continues until the function control logic detects the beginning of tape (BOT) marker. When BOT is detected, the function control logic asserts FWD (1) L (LAW 5) and removes REWIND CAP H. The assertion of FWD (1) L triggers the 80 ms delay [enabled by RWS (1) H]. Normal braking is applied and the capstan servo gradually decelerates toward 1.14 m/s (45 in/s), still traveling in the reverse direction past BOT.

When this delay times out, the forward command is passed on to the capstan servo as FOR H (LAW 3). The capstan accelerates from 1.14 m/s (45 in/s) in the reverse direction to 1.14 m/s (45 in/s) forward. The tape then moves forward until the BOT marker is again detected. At this time, the function control logic clears the FWD and RWS flip-flops, negates FOR H, and the capstan comes to a stop, terminating the rewind.

5.3.6.8 Unload Control – At the completion of the rewind function, the tape is sitting at rest at the BOT marker. When the REW/UNLOAD switch on the TE16 control panel is pressed again (the first time was to initiate the rewind function), the unload function begins. Pressing the switch triggers a 5 μs pulse (LAW 3 UNLOAD PULSE), which clears the RELAY ENABLE flip-flop.

When the RELAY ENABLE flip-flop clears, it clears the VACUUM ON signal, removing both vacuum from the tape columns and power from the capstan and reel motors. Special H607 circuitry then applies limited power to the reel motors to accomplish unloading. The motor brakes are gated off during this sequence. The tape is removed from the vacuum columns and the unload sequence continues until all tape is on the lower reel.

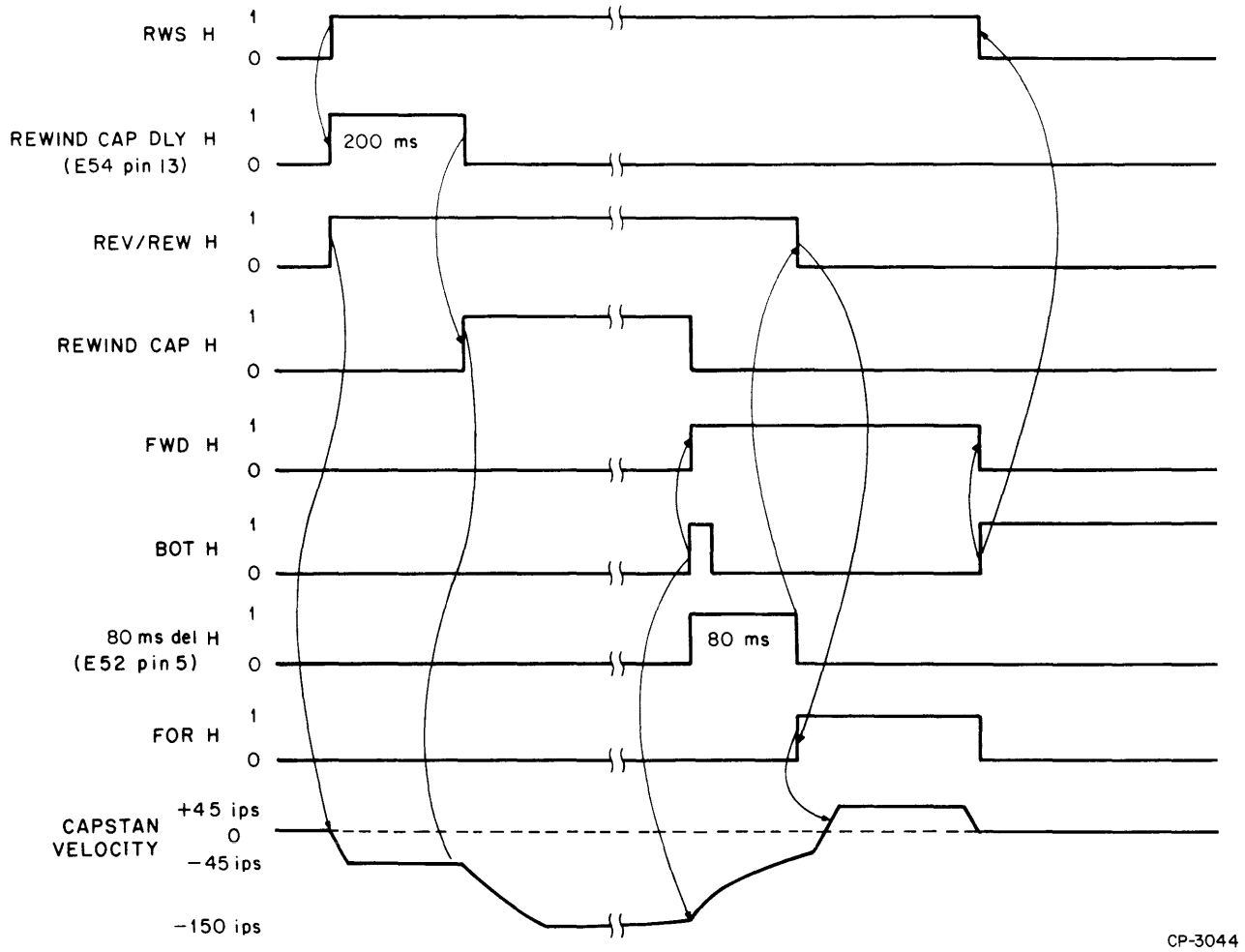


Figure 5-33 Rewind Sequence Timing

5.3.6.9 Tape Unit Ready and Transport Settling Down - The TUR (SB) L and the transport settling down [SDWN (SB) L] signals indicate whether the transport is idle (ready to begin an operation), moving, or settling down (coming to a halt after performing an operation). When the tape transport is on-line and selected by its controller, it transmits these signals to the controller to notify the controller when it is able to accept another command.

Whenever an operation is being performed, the function control logic asserts MOTION H. The OR of MOTION H (operation in progress) and LOCAL H (unit off-line) sets the RUNNING H one-shot delay (LAW 3), thereby asserting RUNNING H and also inhibiting the settle-down signal SDWN (SB) L. When both MOTION H and LOCAL H are negated, the RUNNING H one-shot begins to time out and SDWN (SB) L is asserted, indicating the transport is slowing to a halt. After approximately 12 ms, when the capstan has had time to come to a complete stop following any previous command, the RUNNING H one-shot times out, negating SDWN (SB) L and, provided MOL H is asserted, asserting Tape Unit Ready [TUR (SB) L], thereby indicating that the unit is ready to accept any command.

5.3.6.10 Manual Control Operation – Manual operation of the TE16 Tape Transport is effected by the operator control box switches. The detailed operation of those switches is explained in this section.

1. **LOAD** – When the LOAD switch is pressed, the FAIL flip-flop is cleared, which then clears the RELAY ENABLE flip-flop. Pressing and releasing this switch also triggers a delay, asserting LOAD PULSE (1) H (LAW 3) for about 1 μs. This sets the RELAY ENABLE flip-flop and initiates the tape loading feature discussed earlier in this section.

2. **ON-LINE** – Pressing and releasing this switch changes the transport status from on-line to off-line or vice versa, depending on the switch indicator. When the indicator is on, the transport is on-line; pressing the switch would place the transport off-line (indicator would go out).

   Assuming the transport is off-line, pressing the ON-LINE switch asserts ON LINE SW which clears the LOCAL flip-flop (LAW 4), asserting LOCAL (0) H and turning on the indicator (ON LINE LED). Pressing the switch a second time asserts ON LINE SW again, asserting LOCAL (1) H and turning off the indicator.

   NOTE
   If the TFG (M8912) module is in the testing position, the drive cannot be placed on-line (Paragraph 5.3.5).

   Unless a rewind operation is in progress, the ON LINE SW signal asserts INIT L (LAW 6). The assertion of INIT L clears the FWD and REV flip-flops and brings tape motion to a halt.

   The LOCAL flip-flop (LAW 4) controls the operating mode of the TE16 Tape Transport. When LOCAL (0) H is true, the transport is on-line and all operations of the transport are controlled by the tape controller over the slave bus (SB). When LOCAL (1) H is true, the transport is off-line and is, effectively, isolated from the slave bus. In this mode (off-line), tape motion is controlled by the FWD/REV and START/STOP switches (located under the logic assembly), as discussed next, and also by the TFG (M8912) module.

3. **FWD/REV** – This two-position switch selects the direction of tape motion for off-line operations (LAW 5). When the switch is in the FWD position, MANUAL FWD L is asserted; in the REV position, MANUAL REV L is asserted. These signals do not initiate tape motion but are strobed by the START L pulse, as discussed next.

4. **START/STOP** – When this switch is moved from its START position to the STOP position, signal STOP L is asserted. If the transport is off-line [LOCAL (1) H asserted], this causes a corresponding pulse at INIT L, clearing the FWD, RWS, and REV flip-flops and bringing tape motion to a halt. When the START/STOP switch is moved to the START position, START L is asserted, directly setting a flip-flop in E53 (LAW 5). The high-going transition of this flip-flop is ANDed with LOCAL (1) H (transport off-line) and MOTION L (no operation in progress) to produce a pulse that strobes the MANUAL FWD and REV lines, the "B" inputs on an 8266 multiplexer. The assertion of either line causes the respective FWD or REV flip-flop to set, initiating tape motion in the indicated direction. Note, however, that if BOT L is asserted, the signal that sets the RWS flip-flop is gated off because the tape is already at BOT. Note also that if END PT H is asserted and FWD (1) H is true, then INIT L is asserted to clear the FWD flip-flop and prevent running off the end of the tape.

5.3.6.11 Tape Unit Status Sensors - The tape status (EOT/BOT) and write-lock sensor features are discussed in this section.

1. **EOT/BOT SENSOR** - To locate the beginning and the end of the recording area on the tape, the load and end points are marked by reflective strips mounted on the nonoxide side of the tape. The dimensions and placement of these strips are shown in Figure 5-34.

   The strips are detected by the phototransistors of the EOT/BOT sensor assembly. The EOT/BOT assembly is located in the wall of the lower vacuum column. It consists of an EOT sensor phototransistor, located to detect light reflected from the EOT strip; a BOT sensor phototransistor, located to detect light reflected from the BOT strip; and two light-emitting diodes (LED) located opposite the center of the tape, which illuminate both the EOT and BOT strips. The LED operates in the infra-red region and, therefore, produces no visible light. The outputs of the EOT and BOT signals are amplified, filtered, and converted to logic levels (Drawing LAW 4), producing signals BOT H, BOT (SB) L, END PT H, and END PT (SB) L.

   The assertion of END PT H sets a flip-flop, which remains set until either the tape is rewound or EOT is negated while tape is traveling in the reverse direction.

   Thus, if tape is moved forward past the EOT marker, the END PT flip-flop remains set, even after the marker is passed and is cleared only by rewinding or reversing the tape back past the EOT marker. Setting the END PT flip-flop has the following effects:

   a. If the TE16 is off-line[LOCAL (1) H asserted], forward tape motion stops and the transport does not accept a manual forward command until the tape is rewound or reversed off the EOT marker.

   b. If the TE16 is on-line and selected by its controller, the TE16 signal END PT (SB) L is asserted, indicating to the controller that tape has passed the end point.

   NOTE

   Notice that if the TE16 is on-line, it does not automatically stop upon detecting EOT. Data may be written up to 3.05 m (10 ft) past the end point. The programmer must ensure that he does not run past this point.

   The assertion of BOT H has the following effects:

   a. The TE16 accepts no new rewind commands.

   b. When the TE16 rewinds into BOT [i.e., RWS (1) L is asserted, FWD (1) L is asserted, and BOT H becomes asserted], the FWD flip-flop is set (Drawing LAW 5).

   c. When the TE16 moves forward into BOT, the FWD flip-flop is cleared. (If the RWS flip-flop is set at this time, clearing FWD also clears RWS, terminating the rewind sequence.)

   d. If the TE16 is on-line [LOCAL (0) H asserted] and selected by the controller, it asserts the transport bus signal BOT (SB) L, indicating to the controller that it is at BOT.

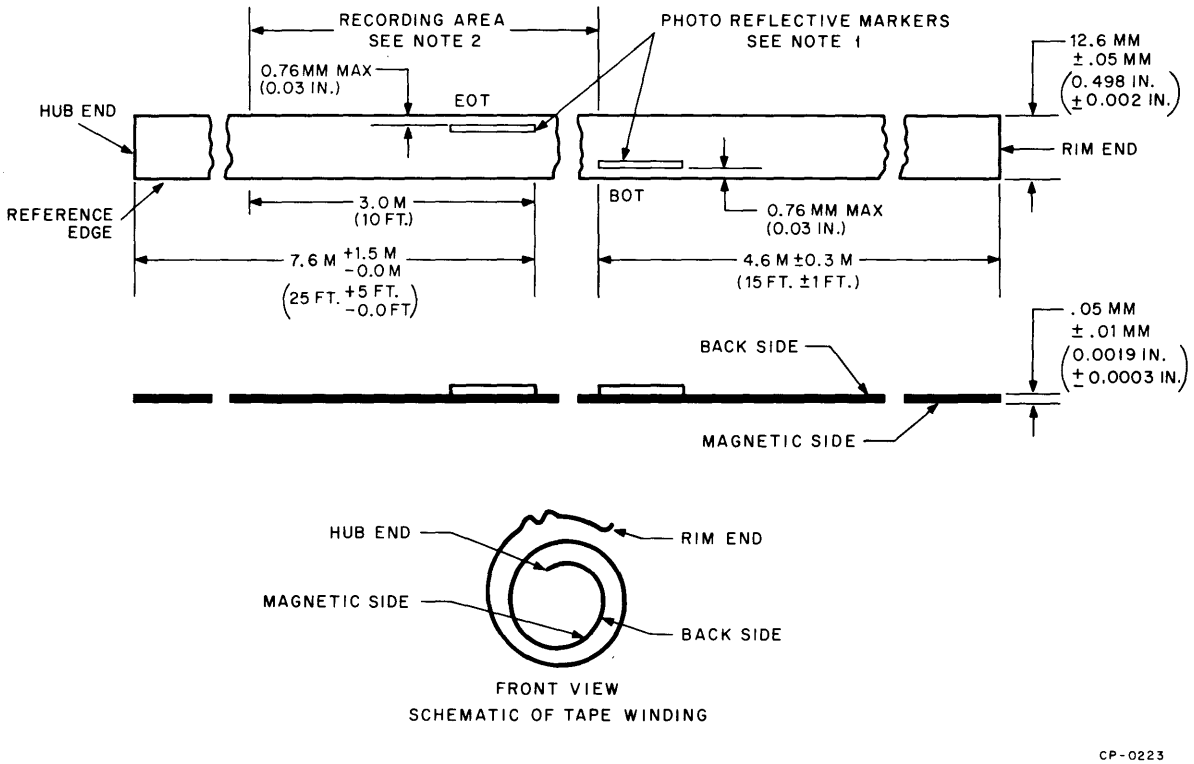


Figure 5-34 Tape Markers, Recording Area, and Tape Wind

2. **Write Lock** – To protect tapes from inadvertent erasure, tape reels are provided with a write enable ring. If a reel of tape is mounted on the TE16 Tape Transport with its write enable ring removed, the condition is sensed and the transport refuses to honor any write commands. Further, if the transport is on-line and selected by the controller, it asserts WRL (SB) L to the controller, indicating to the controller that it is write-locked.

   The write-lock assembly consists of the write-lock solenoid and the write-lock switch. When no write enable ring is inserted in the file reel, a feeler attached to the end of the solenoid shaft extends into the write-lock slot on the back of the reel. This feeler places the write-lock switch in its normally closed position, asserting WR LOCK L (Drawing LAW 6). When a write enable ring is inserted in the file reel, the ring pushes back the solenoid shaft, actuating the write-lock switch and negating WR LOCK L. If the write-enable switch is actuated when tape is loaded in the buffer columns, the write-lock solenoid is engaged to withdraw the feeler from contact with the ring. This keeps the write-lock switch actuated until the tape is unloaded and reduces wear of the write-lock assembly and write enable ring during tape unit operation.

5.3.6.12 On-Line Operation – When signal LOCAL (0) H is asserted, the TE16 is on-line. In this state, all transport operations are directed by the tape controller over the slave bus. The slave bus connects the controller to up to eight TE16 Tape Transports.

1. **Transport Selection and Status Reporting** – All of the tape transports in a system are wired to the same slave bus, but only one transport can be logically connected to the bus at one time (i.e., only one transport can transmit its status to the tape controller and respond to its commands, and only one transport can be reading or writing data at a given time).

   To select the particular tape transport to communicate with the tape controller, the controller transmits a binary code on bus lines SS 0 (SB) L, SS 1 (SB) L, and SS 2 (SB) L. As shown on Drawing LAW 4, each transport on the bus compares this code to the transport number determined by the address selection plug (signals SW0, SW1, and SW2). If the selection code transmitted by the controller matches the transport number and the transport is on-line, then the SELECT indicator glows and the transport is logically connected to the slave bus. All other transports remain logically disconnected and neither transmit nor respond to bus signals. If no address selection plug is inserted in the TE16 front panel, the SELECT QUALIFY L signal is pulled up to +5 V and prevents drive selection. Also, during the loading sequence, LOADING (1) H qualifies a 7405 gate which also prevents drive selection.

   When a particular transport is logically connected to the slave bus, it transmits status information to the tape controller as follows:

7 CH (SB) L	Always negated in the TE16 Tape Transport
BOT (SB) L	Asserted when the tape is positioned at load point (beginning of tape).
END PT (SB) L	Asserted when the end point flip-flop is set.
WRL (SB) L	Asserted when the TE16 Tape Transport is write-locked.
RWS (SB) L	Asserted when the extended rewind status (EXT RWS) flip-flop is set.
SDWN (SB) L	Asserted when the tape transport is settling down following an operation (i.e., asserted for 12 ± 4 ms following the command to terminate an operation while the capstan is coming to a halt).
TUR (SB) L	Asserted when the tape unit is ready to receive any command (i.e., when the transport is neither performing an operation nor settling down following an operation).

2. **Tape Motion** – If a TE16 is selected, on-line, and loaded with tape (MOL H asserted), it responds to the SLAVE SET PLS and the FWD, REV, and RWND command lines of the slave bus by setting the corresponding motion control flip-flops [i.e., FWD, REV, and RWS (Rewind Status) flip-flops on LAW 5]. If the WRITE command line is asserted with the RWND command line, signal SET OFF LINE L is generated, setting the LOCAL flip-flop (LAW 4). If WRITE is asserted but RWND is not, SLAVE SET PLS produces SET WRE (Set Write Enable), which sets the WRITE ENABLE flip-flop (LAW 6).

The outputs of the motion control flip-flops produce FOR H, REV/REW H, and REWIND CAP H (LAW 3) signals that control the capstan servo and drive circuits. At the same time, the WRITE ENABLE flip-flop (if set) generates WRITE ENABLE (1) L, which shunts WRITE voltage to the write and erase heads, thereby energizing the heads. Figure 5-35, the Tape Motion Initiation Flowchart, complements this description.

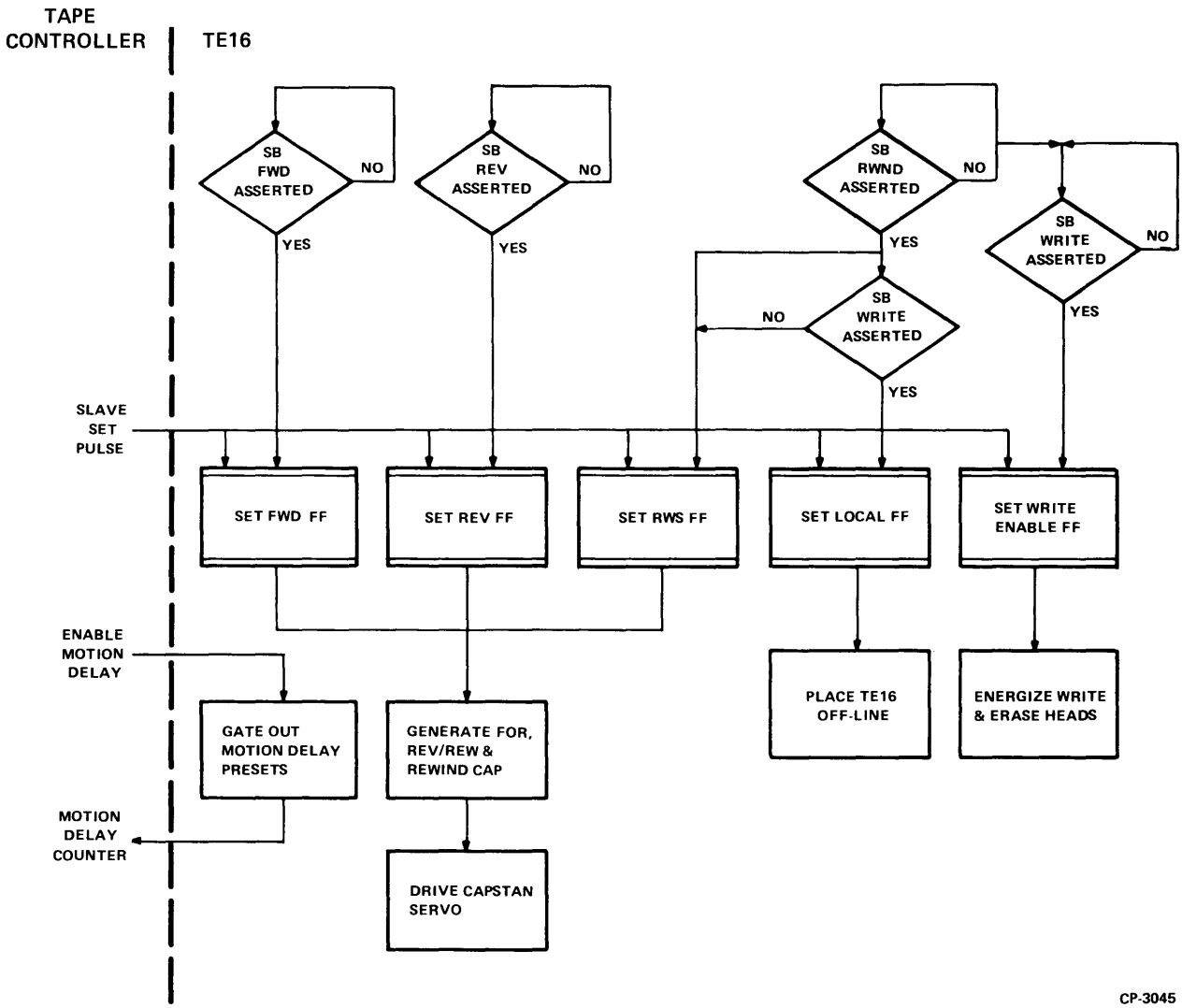


Figure 5-35 Tape Motion Initiation Flowchart

Once forward or reverse tape motion is initiated, it continues (unless a TE16 mechanical or power failure is sensed) until the tape controller transmits a STOP signal to the transport.

If a rewind operation is being performed, STOP L is asserted as soon as SLAVE SET PLS is negated. However, because the RWS flip-flop is already set, this does not produce an INIT L pulse (LAW 6) and does not terminate motion. Once the RWS flip-flop is set, the TE16 performs the rewind operation independently, as previously described. The TE16 notifies the tape controller that it is performing a rewind by asserting RWS (SB) L on the slave bus. When the rewind control sequence is over, motion terminates automatically and the controller is notified when the TE16 asserts SET SSC L (Status State Change) on the slave bus (LAW 6).

The TE16 terminates tape motion when an INIT L pulse (generated on LAW 6) clears the motion control flip-flops (LAW 5). An INIT (SB) L signal also exists; it is different than INIT. The INIT signal is an internal M8916 signal, generated by various conditions that determine the need to halt or inhibit tape motion.

INIT (SB) L simply clears the SET SSC and SLA flip-flops. When the TE16 controller is initialized, it halts tape motion by asserting STOP to the selected slave and uses INIT (SB) L to clear the SSC and SLA flip-flops.

5.3.7 M8926 Interface Module Description

As stated in Paragraph 1.2.1, the TE10W Tape Transport is based upon the TE16. The TE16 becomes a TE10W master when an M8926 interface module replaces the three standard cable cards (M9001, M9001-YA, and M8913) in a TE16. This is done in order to achieve an interface with a positive logic tape controller.

5.3.7.1 General (Figures 5-36, 5-37, and 5-38) – Figure 5-36 is a simplified flow diagram of the M8926 interface board. The CSET command from the controller triggers a drive start-up sequence. The start-up sequence signals the drive to start the capstan motor and introduces a delay period for the capstan motor to get up to speed (1.14 m or 45 in/s) before enabling a read or write sequence.

All commands from the controller, except rewind, cause a read sequence to occur. The read sequence transfers data from the drive to the M8926 board. A write command (CWRE) must be asserted by the controller to enable a write sequence. If a write command is asserted by the controller, data is transferred from the controller to the drive to be written on tape (write sequence). The data written on tape is then read back via the read sequence. This read-after-write feature allows the recorded data to be checked for errors by the M8926 board. The read-after-write data is made available to the controller where it can be accessed by the processor for maintenance purposes. During normal operation, read data is not accepted by the controller unless a read command is asserted.

When the read circuits detect the end of the record, a drive stop sequence is triggered. The stop sequence signals the drive to stop the capstan motor and initiates another delay period. The delay allows the capstan motor to slow down to a stop before the command operation is terminated.

The M8926 detailed flow diagram (Figure 5-37) provides a more detailed functional description of the M8926 interface board. This diagram should be read in its entirety while referencing the functional block diagram, Figure 5-38. Subsequent paragraphs in this chapter treat the M8926 board according to the functional divisions shown in Figures 5-36, 5-37, and 5-38, namely:

1. Status/Command logic
2. Drive startup
3. Write sequence
4. Read sequence
5. Drive stop.

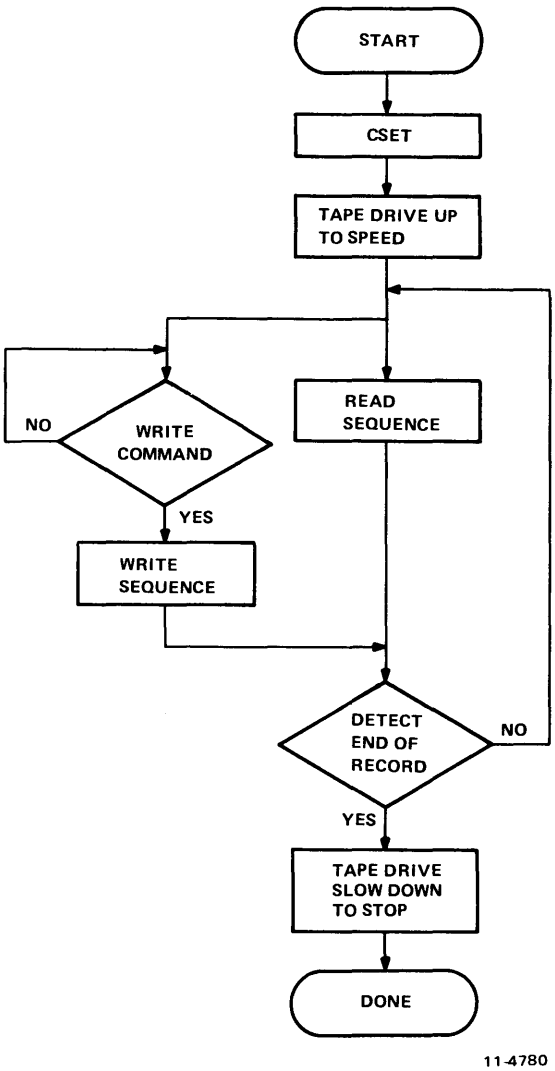


Figure 5-36 M8926 Simplifier Flow Diagram

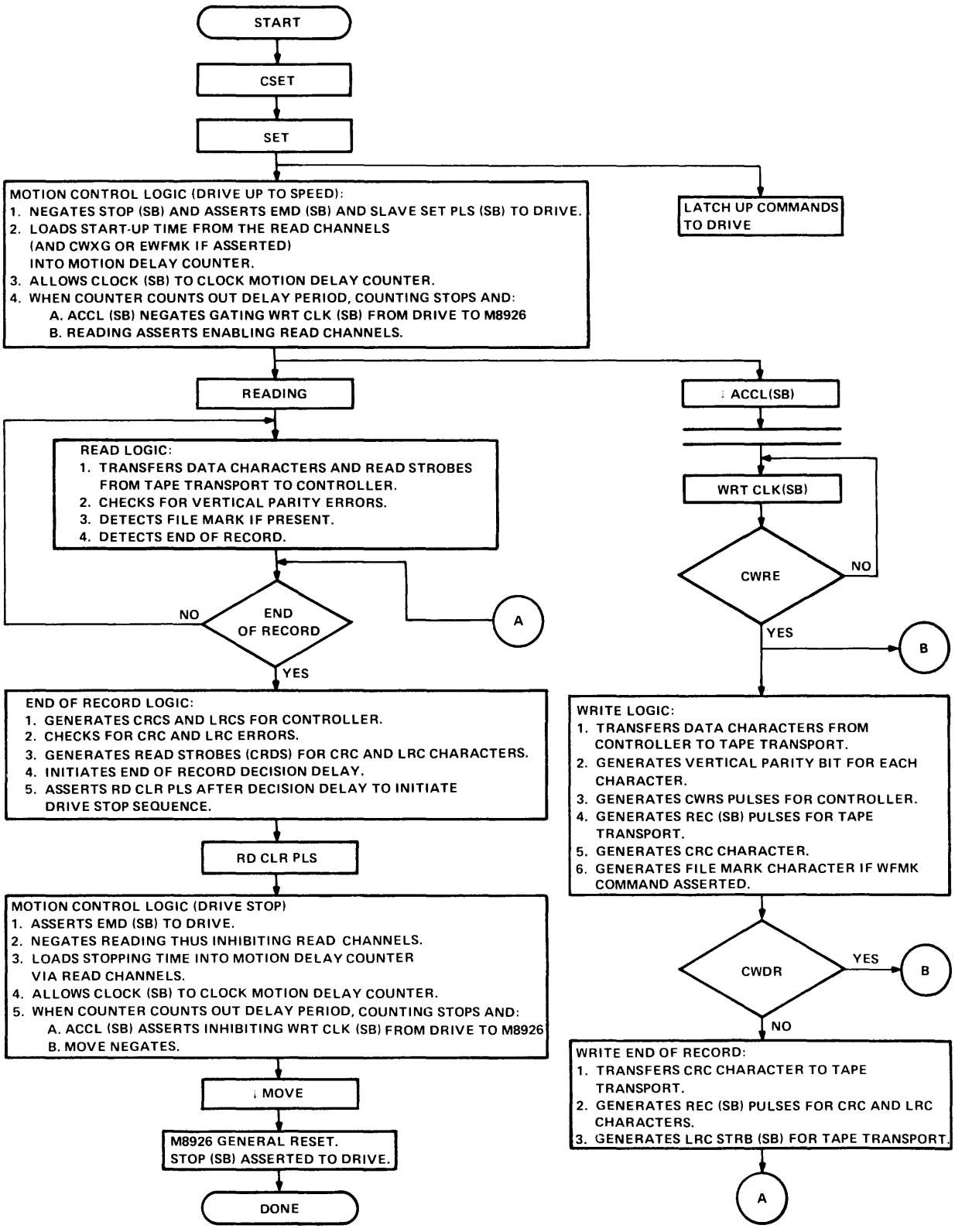


Figure 5-37 M8926 Detailed Flow Diagram

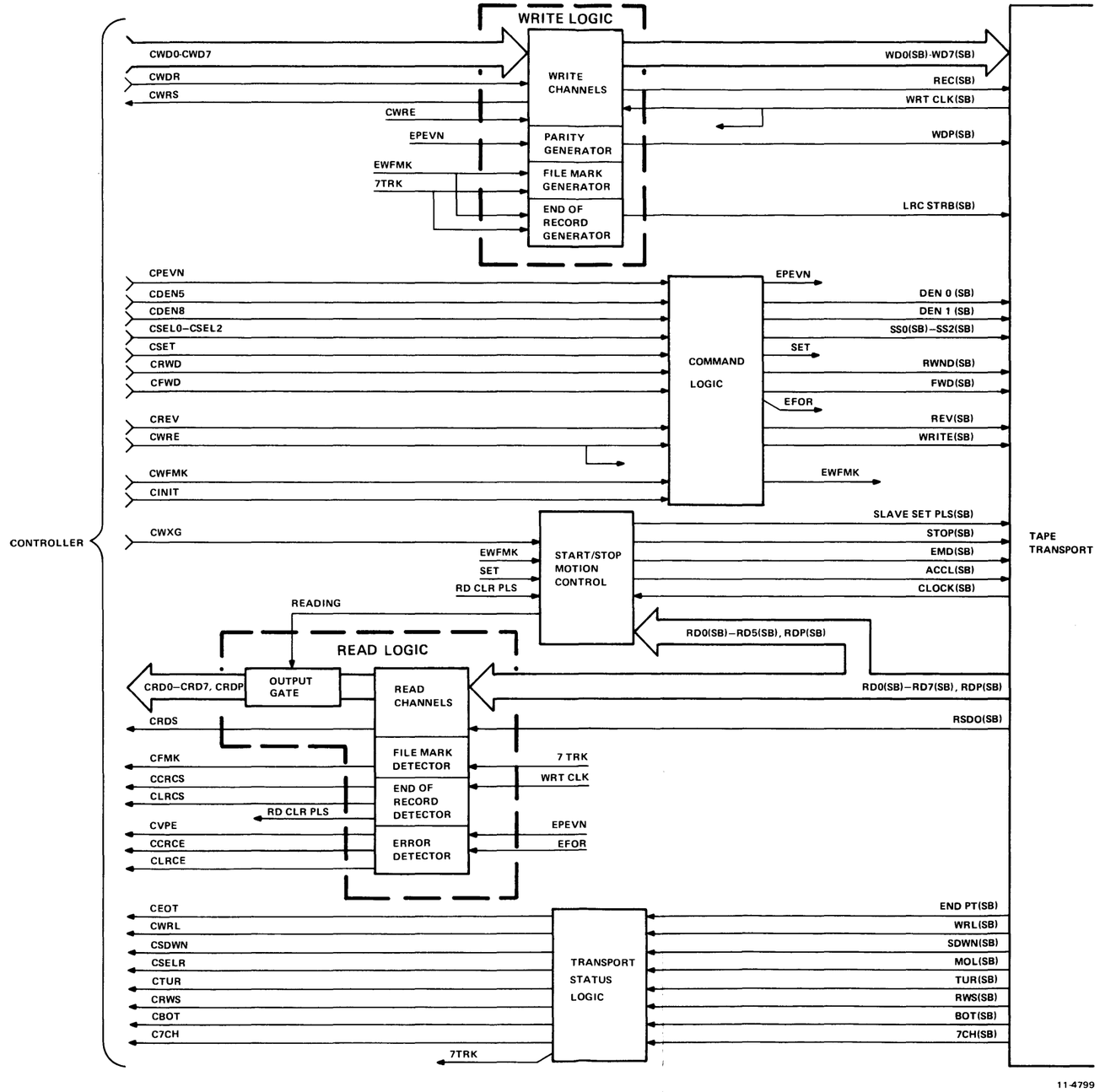


Figure 5-38 M8926 Block Diagram

It will be helpful to reference Figures 5-37 and 5-38 as an overview while reading through this section.

NOTE

The block diagrams that follow use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the controller logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate, yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Other signal names or notes are enclosed in parentheses.

5.3.7.2 Command Logic – Certain operational commands are coupled from the controller to the drive via combinational logic circuits. Other commands, which must stay asserted during the entire operation, are latched up in flip-flops set by CSET from the controller. Note the conversion of CDEN5 to DEN0 (SB) and CDEN8 to DEN1 (SB) during the latch-up process.

CSEL0-CSEL2 selects a slave unit via a 3-bit code. The 3-bit code is latched up in the slave select latch-up flip-flops, which output SS0 (SB)-SS2 (SB) to the drive (Figure 5-39). The input code from the controller is compared to the output code in the slave select comparator. If the two codes do not match, the latch-up flip-flops are clocked, forcing SS0 (SB)-SS2 (SB) to agree with the select code from the controller. An AND gate must be enabled by MOVE before clocking of the flip-flops can occur. MOVE is asserted true during every command operation except rewind. Thus, a new slave drive cannot be selected during a read, write, or spacing operation. Note that a bit reversal takes place in the latch flip-flops where the CSEL0, 1 and 2 input bits become bits SS2 (SB), 1 and 0 respectively in the output.

Figure 5-40 shows four signal lines coupling fixed potentials to the host drive. These signals lines are not used but the host drive requires that the lines be held at a fixed voltage level. Three of the lines [DRV CLR PLS (SB), INIT PLS (SB), 1 RD, (SB)] are tied to +3 V and the fourth (SLAVE BUS ENBL) is tied to ground.

5.3.7.3 Status Logic – Certain status signals are transmitted directly from the drive to the controller, while others such as RWS (SB) and MOL (SB) undergo conditional gating. Rewind status, RWS (SB), from the drive negates at the end of SDWN (SB) simultaneously with the assertion of TUR (SB) (Figure 5-41). A timing requirement within the controller demands that CRWS negate before TUR asserts. This requirement is met by ANDing RWS (SB) with SDWN DELAYED, thus producing the proper CRWS timing as shown in Figure 5-41. SDWN is delayed approximately 100 ns, producing SDWN DELAYED before being ANDed with RWS (SB). This is done to eliminate the possibility of a spurious assertion of CRWS should SDWN (SB) negate while RWS is still true.

CSELR is negated for 1 μs, while a new drive is being selected by the slave select logic. This is accomplished by the gating of MOL(SB) with the 0 output of the slave select one-shot. The 1 μs delay allows settling of the select code before CSELR is asserted for the new drive.

When a 7-track drive is being used 7CH(SB) is asserted from the drive causing the assertion of C7CH to the controller and R7CH to the 7TRK flip-flop. When SET asserts, 7TRK becomes true to indicate the presence of a 7-track, slave drive to the M8926 board. Note that the assertion of EDEN5 will also cause 7TRK to become true at SET time. Compatibility among the TU10, TU10W, and TE10W drives requires that both EDEN5 and R7CH cause the assertion of 7TRK at SET pulse time.

5.3.7.4 Drive Start Signals (Figures 5-42, 5-43, and 5-44) - The SET pulse starts the command operation in the drive by:

1. Setting the EMD flip-flop and asserting EMD (SB) to the drive
2. Asserting SLAVE SET PLS (SB) to the drive
3. Setting the MOVE flip-flop thereby negating STOP (SB) to the drive.

MOVE remains asserted and holds STOP (SB) false during the entire command operation. During a rewind operation the MOVE flip-flop is not set. In this case, SLAVE SET PLS negates STOP (SB) at SET time. This negation of STOP is sufficient for the drive to start the rewind sequence.

5.3.7.5 Startup Delay - The output of the EMD flip-flop loads the motion delay counter with delay data set onto read lines BRD0-RRD6, RRDP by the drive. Bit 13 of the counter is preset to a 1 and gates in the clock pulses. The clock pulses are obtained from a divide-by-four counter that receives CLOCK (SB) pulses from the slave bus. An output from the divide-by-four counter is obtained after the first 2 CLOCK (SB) pulses and every 4 CLOCK (SB) pulses thereafter. When the delay counter has been clocked through the delay period, bit 13 of the delay counter is counted down to 0 and bit 14 is asserted. At this time:

1. Input clock pulses to the delay counter are inhibited.
2. READING is asserted enabling the read sequence.
3. ACCL (SB) is negated to the drive thus gating WRT CLK (SB) pulses from the drive for the write sequence.

If the command is CWXG or CWFMK, an extended interrecord gap is generated prior to writing the record. CWXG or EWFMK, if asserted, input into the delay counter increases the delay time and allows the tape to travel an extra distance before the read and write sequences are enabled. The delay increase is from 8.99 to 95.00 ms for a 9-track drive and from 15.26 to 101.3 ms for a 7-track drive. The CWXG and EWFMK inputs to the delay counter are via a gate enabled by ACCL. Thus, only the startup time or gap prior to the record is extended.

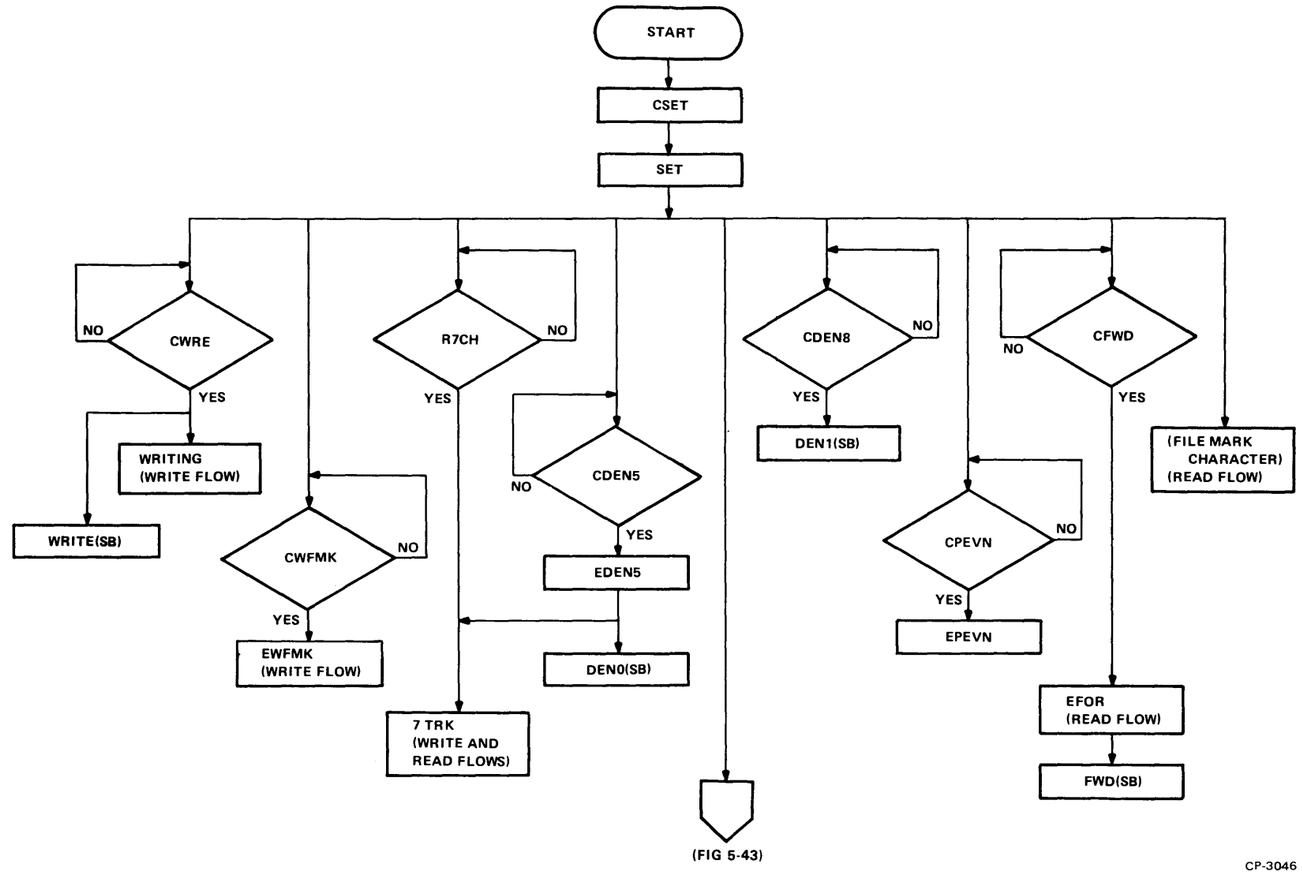


Figure 5-39 Command Latch-Up Flow Diagram

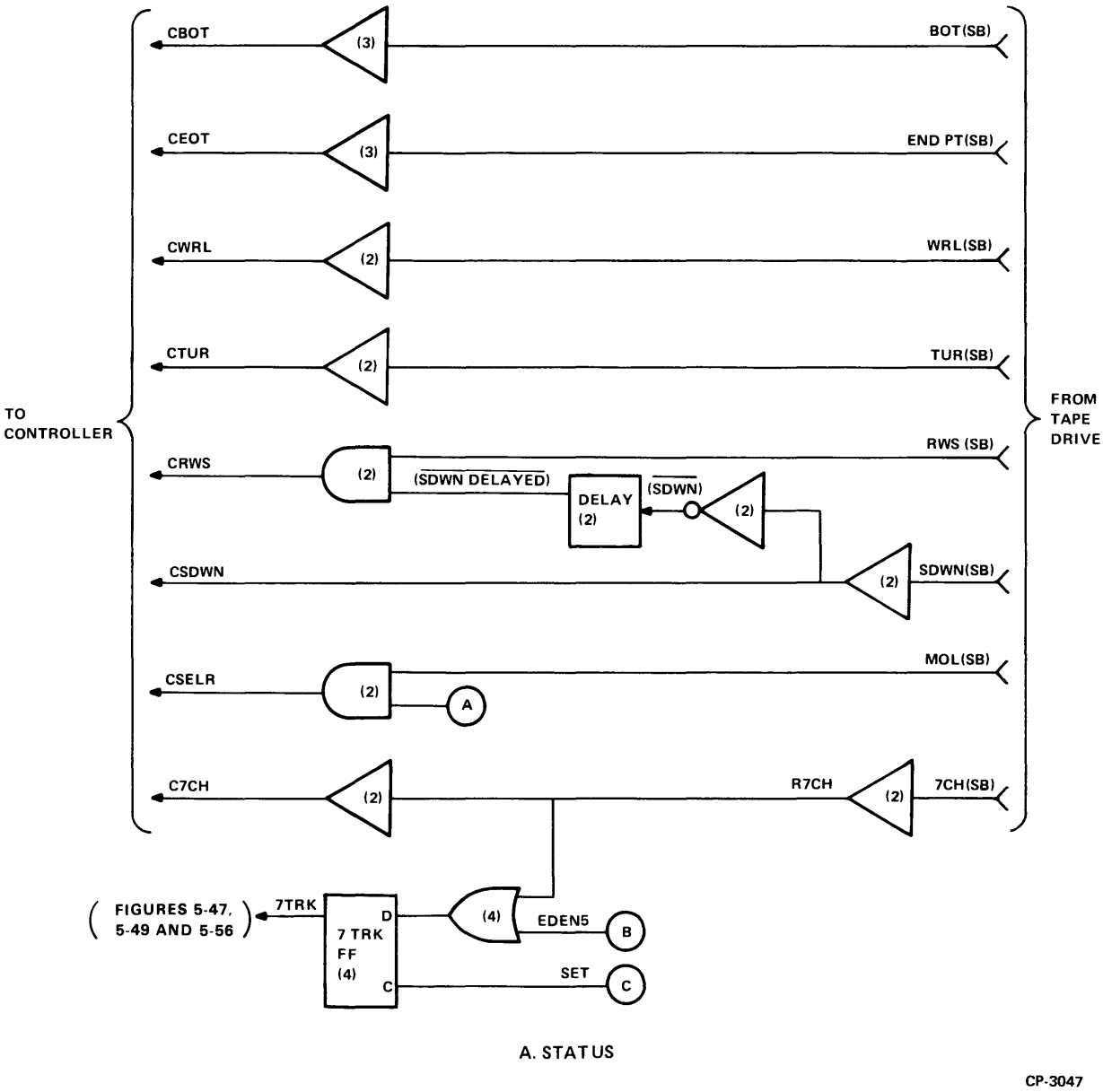


Figure 5-40 Status/Command Block Diagram (Sheet 1 of 2)

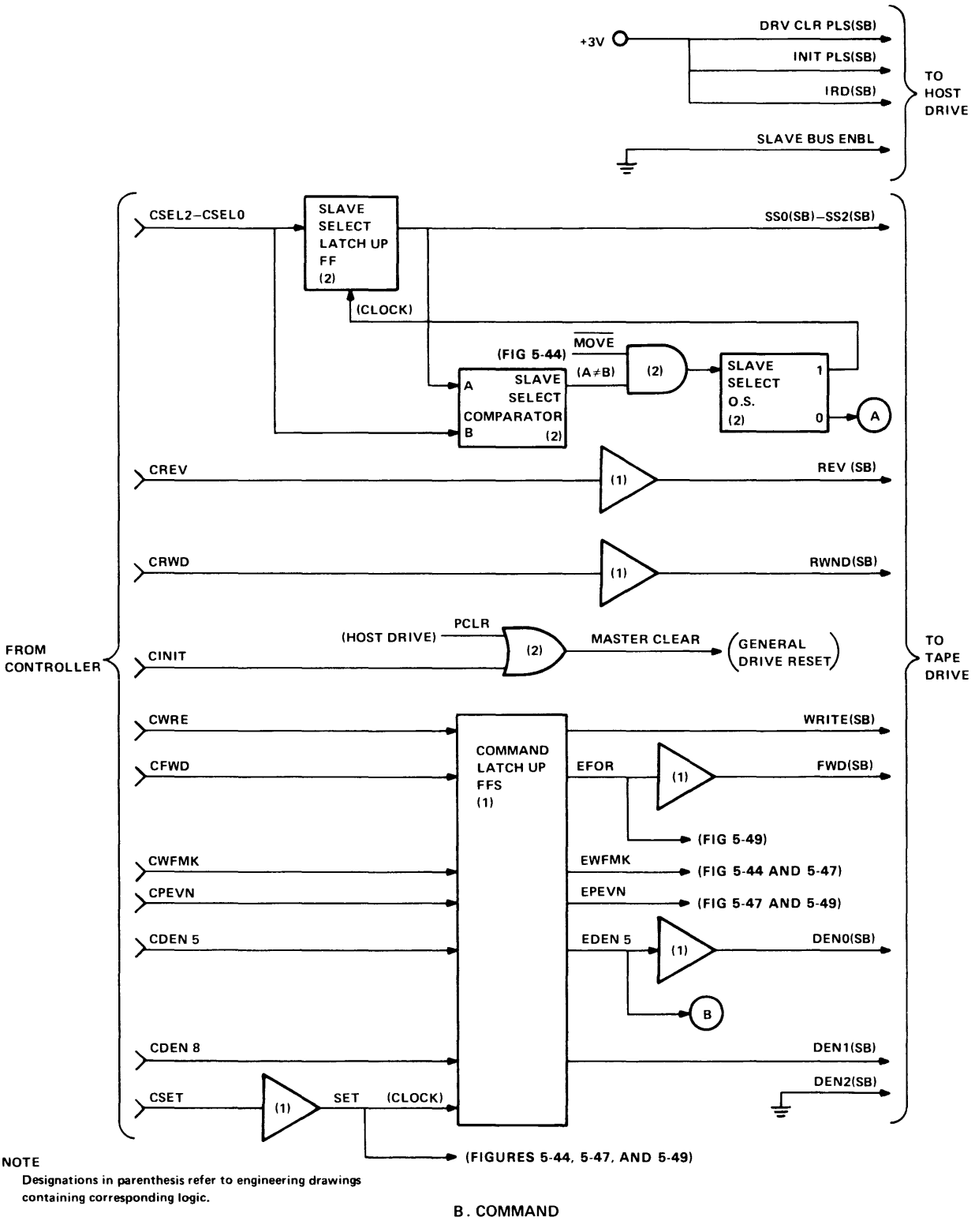


Figure 5-40 Status/Command Block Diagram (Sheet 2 of 2)

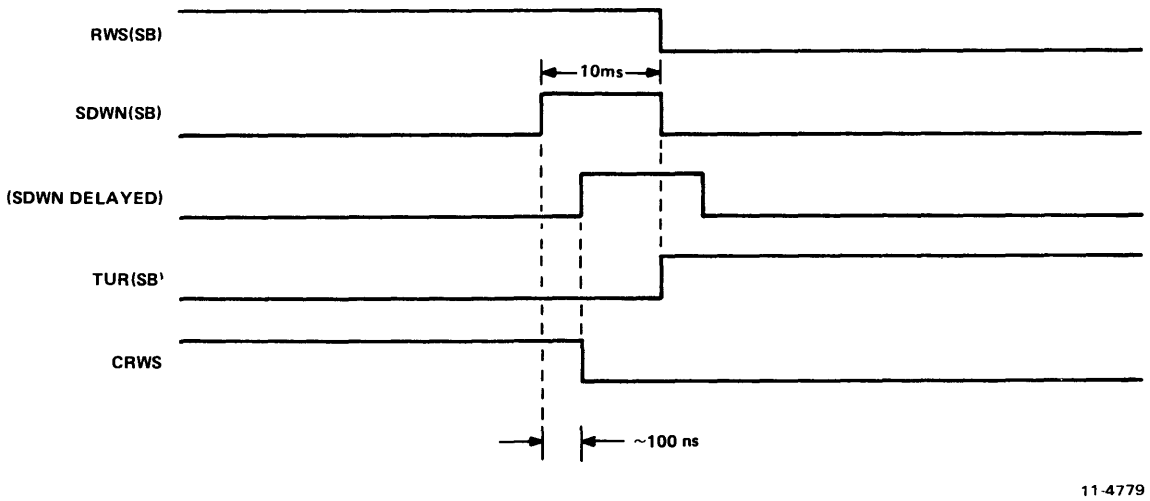


Figure 5-41 RWS and CRWS Timing Diagram

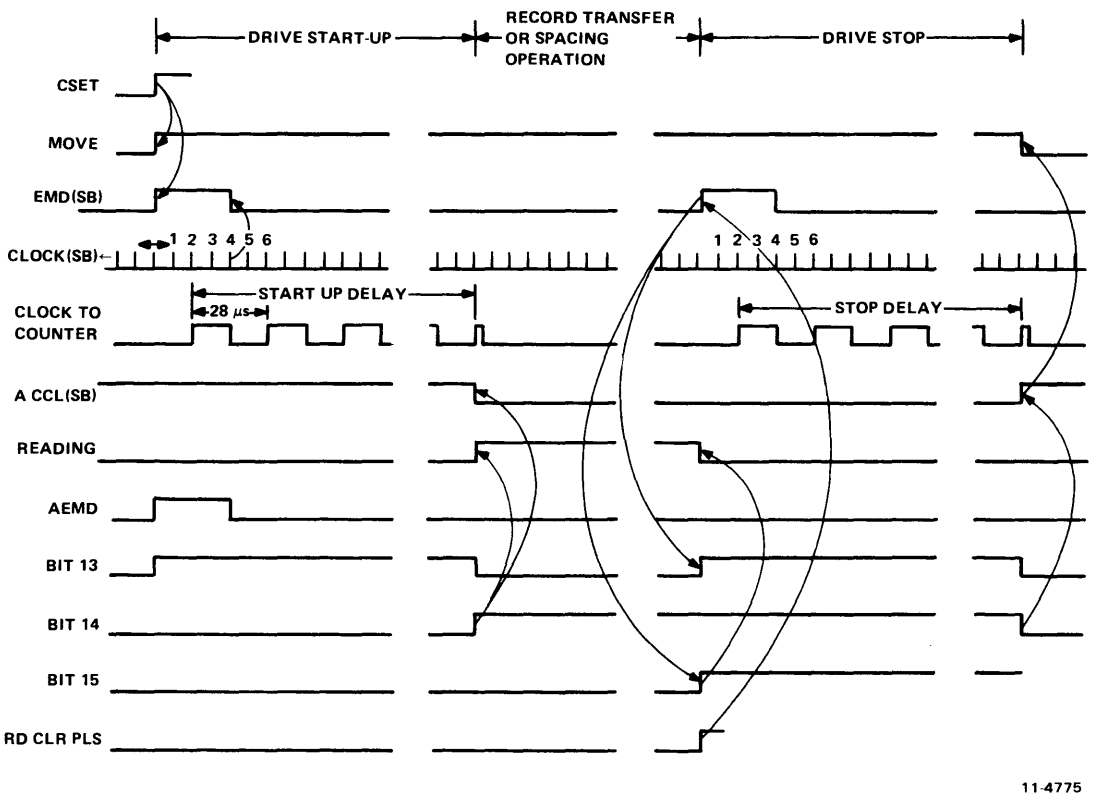


Figure 5-42 M8926 Timing Diagram

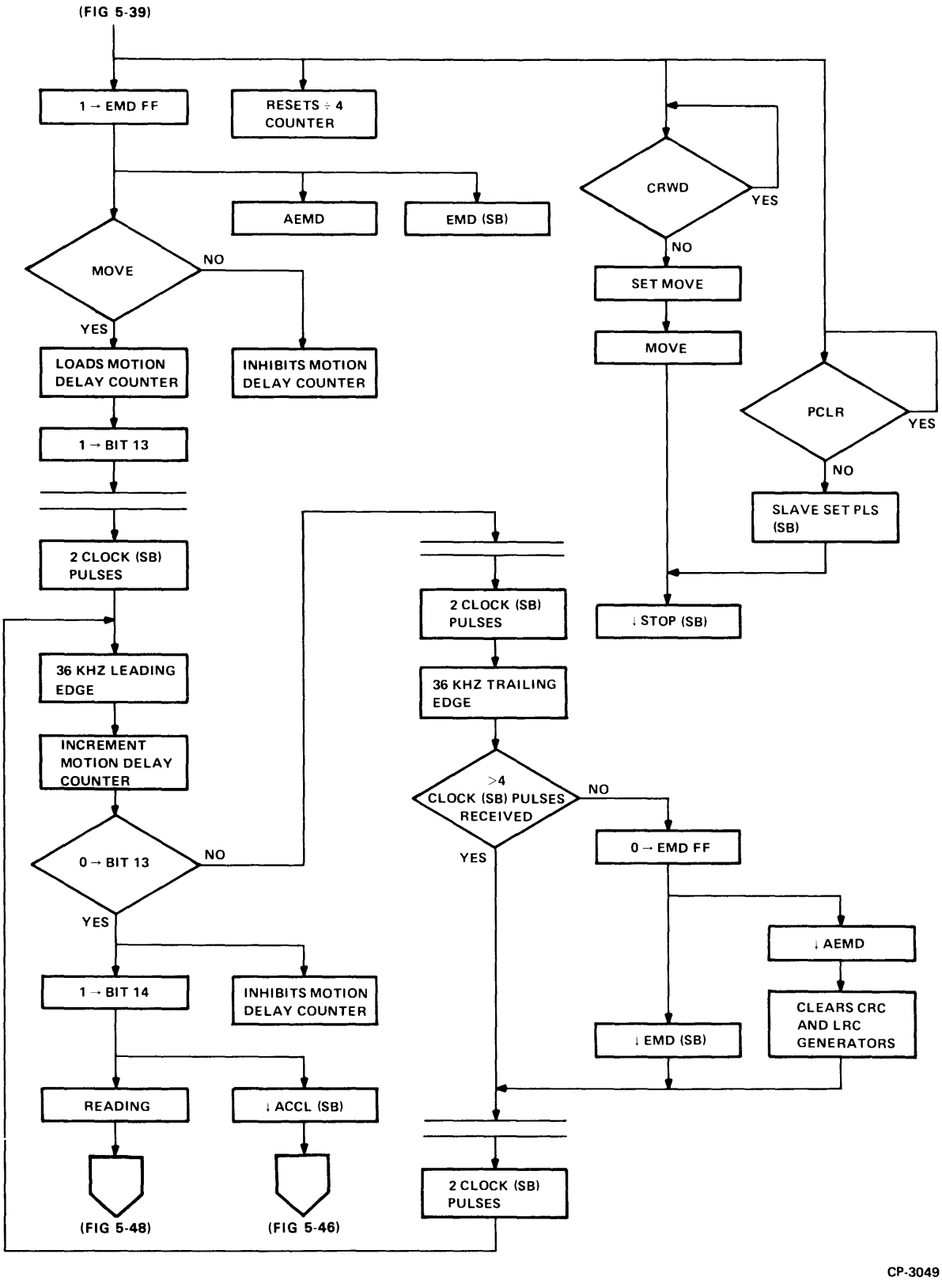


Figure 5-43 Drive Start-Up Flow Diagram

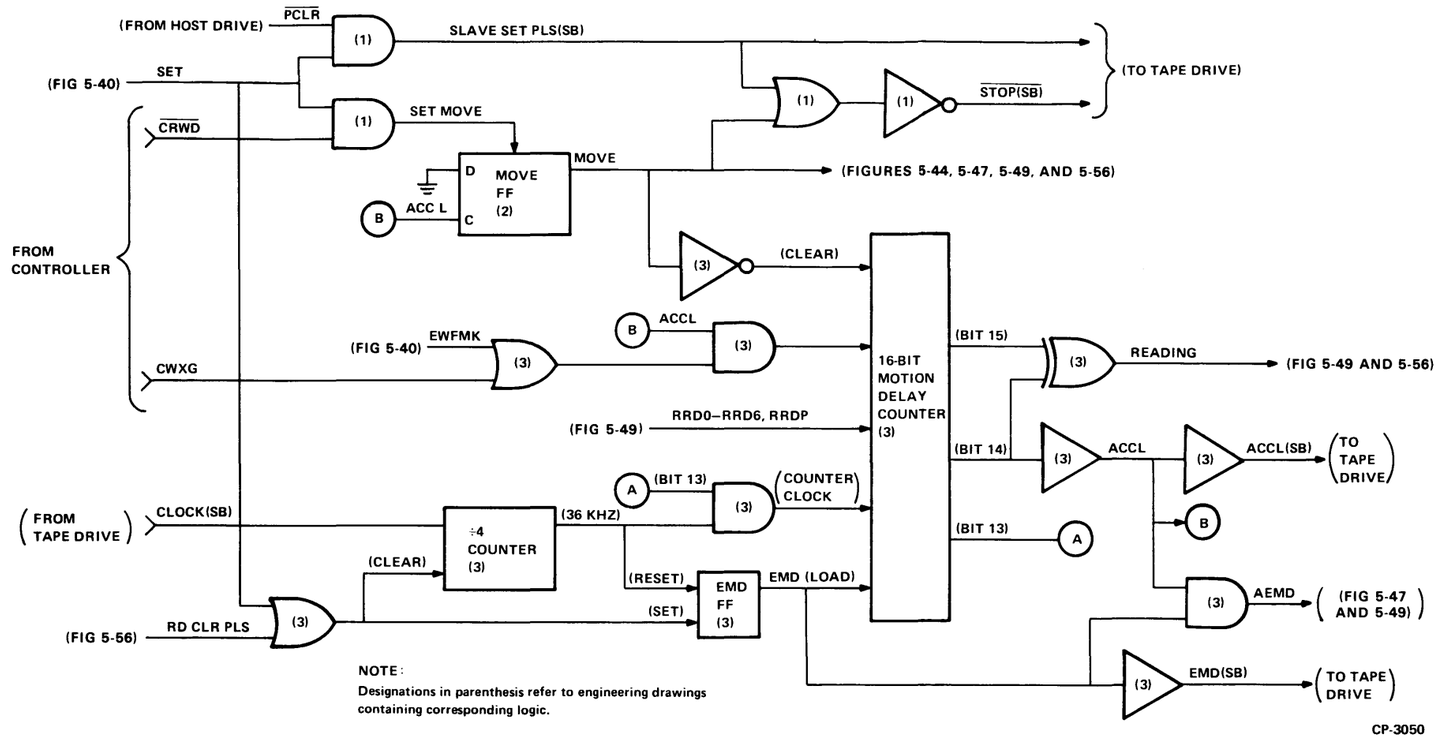


Figure 5-44 Start/Stop Control Block Diagram

5.3.7.6 Write Sequence (Figures 5-45, 5-46, and 5-47)

1. **Nine-Track Normal; Write Data** – If a write command is asserted by the controller, CWRE is true, allowing the SET pulse to set the WRITING flip-flop. The assertion of WRITING loads the end-of-record counter, which is preset to a count of 8. The 8-bit output from the counter gates R WRT CLK pulses from the drive to produce WRITE STROBE pulses. The assertion of each WRITE STROBE pulse will:

   a. Latch-up write data from the controller making it available to the drive via the output gates

   b. Assert CWRS to the controller to extract the next character from memory

   c. Assert REC (SB) to the drive and to the CRC generator.

   Vertical parity is produced by a parity generator, which monitors the eight write lines and outputs a true or false parity bit according to the number of 1 bits and whether odd or even parity is specified (EPEVN).

   The write logic contains a circuit to detect a zero-character condition when even parity is specified. Such a condition results in a blank space on the tape that can not be sensed by the read logic. Should an attempt be made to write a zero character with even parity, the zero character detector output would assert WRX3, thereby generating a 1 bit on the third write channel. A single bit character demands a 1 parity bit when EPEVN is true. The parity bit is also artificially generated via the zero character detector output, which asserts WRXP to the parity write channel.

   The CRC generator receives each data character from the write channels. REC (SB) pulses clock the generator which develops the CRC character during the body of the record.

2. **Nine-Track Normal; Write End-of-Record** – When the data transfer has been completed, CWDR and WRITING are negated, and REC and CWRS strobes are inhibited. The sequence is illustrated in the data transfer timing diagram (Figure 5-45). It can be seen in Figure 5-47 that data characters are moved from memory to tape in two steps: first from memory to the write data latch-up register and then from the register to the transport write logic. The last four characters of a record are shown in the timing diagram (Figure 5-45). CWRS 1, issued to the controller, extracts data character 2 from memory, which moves through the controller and over to the M8926 write data latch-up register. The next write clock pulse (R WRT CLK 2) generates WRITE STROBE 2, REC 2, and CWRS 2. WRITE STROBE 2 latches up data character 2 in the register, making it available to the transport write logic; REC 2 records data character 2 on tape, and CWRS 2 extracts data character 3 from memory. The next CWRS pulse (CWRS 3) extracts the last character (data character 4) from memory. R WRT CLK 4 generates WRITE STROBE 4 to latch-up the last character and REC 4 to record it on tape. CWRS 4 is issued to the controller which, having sensed that the last character has been transferred, inhibits a data extraction from memory (no NPR bus cycle) and negates CWDR. The negation of CWDR conditions the WRITING flip-flop to reset. The trailing edge of an R WRT CLK 4 clocks the flip-flop reset, thus negating WRITING. When WRITING negates:

   a. CWRS pulses to the controller are inhibited.

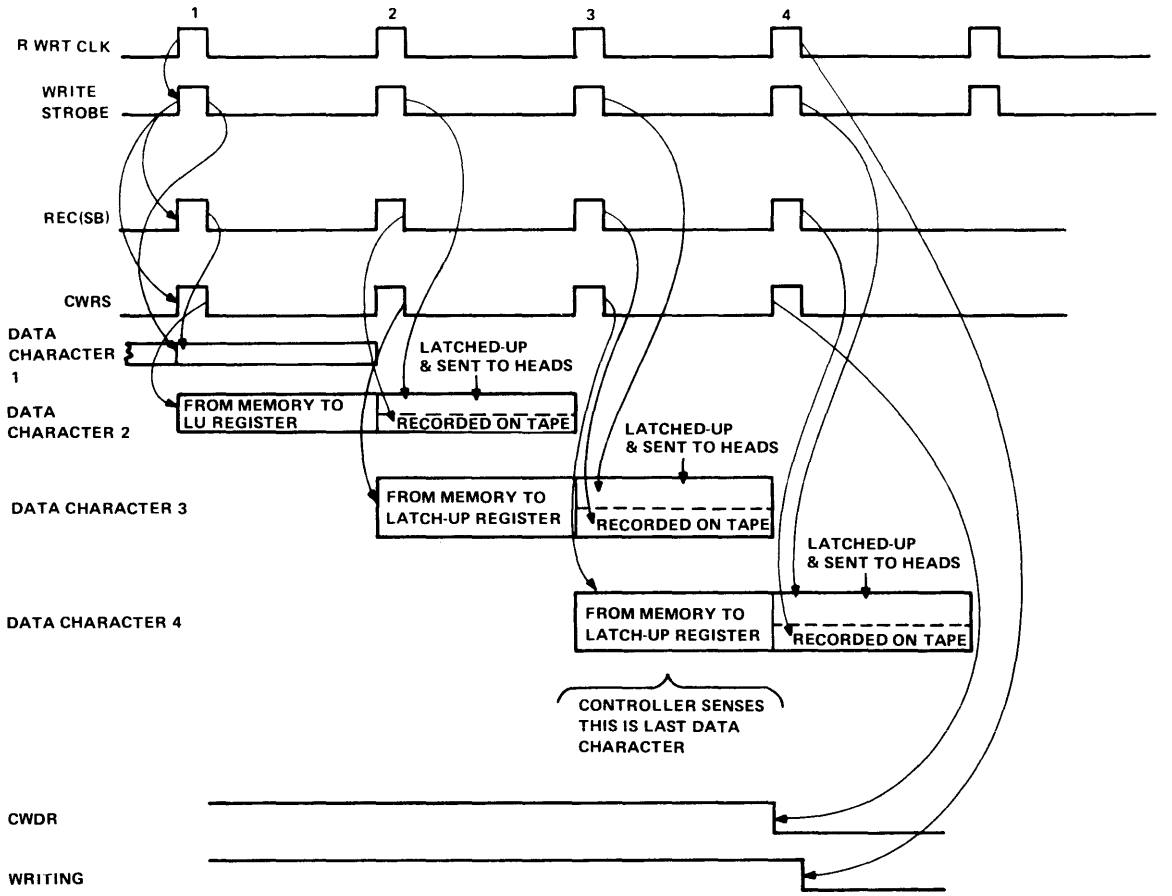
   b. REC (SB) pulses to the drive are inhibited.

   c. The end-of-record counter is enabled.

   WRITE STROBE pulses clock the end-of-record counter. When the counter reaches a count of 3, CHK CHAR STRB asserts and:

   a. Switches the CRC character onto the write lines via the write data/CRC mux

   b. Enables the REC AND gate.



NOTE:

Each R WRT CLK pulse generates WRITE STROBE which generates REC and CWRS. Arrows shown only for R WRT CLK 1.

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Figure 5-45 Write Data Timing Diagram

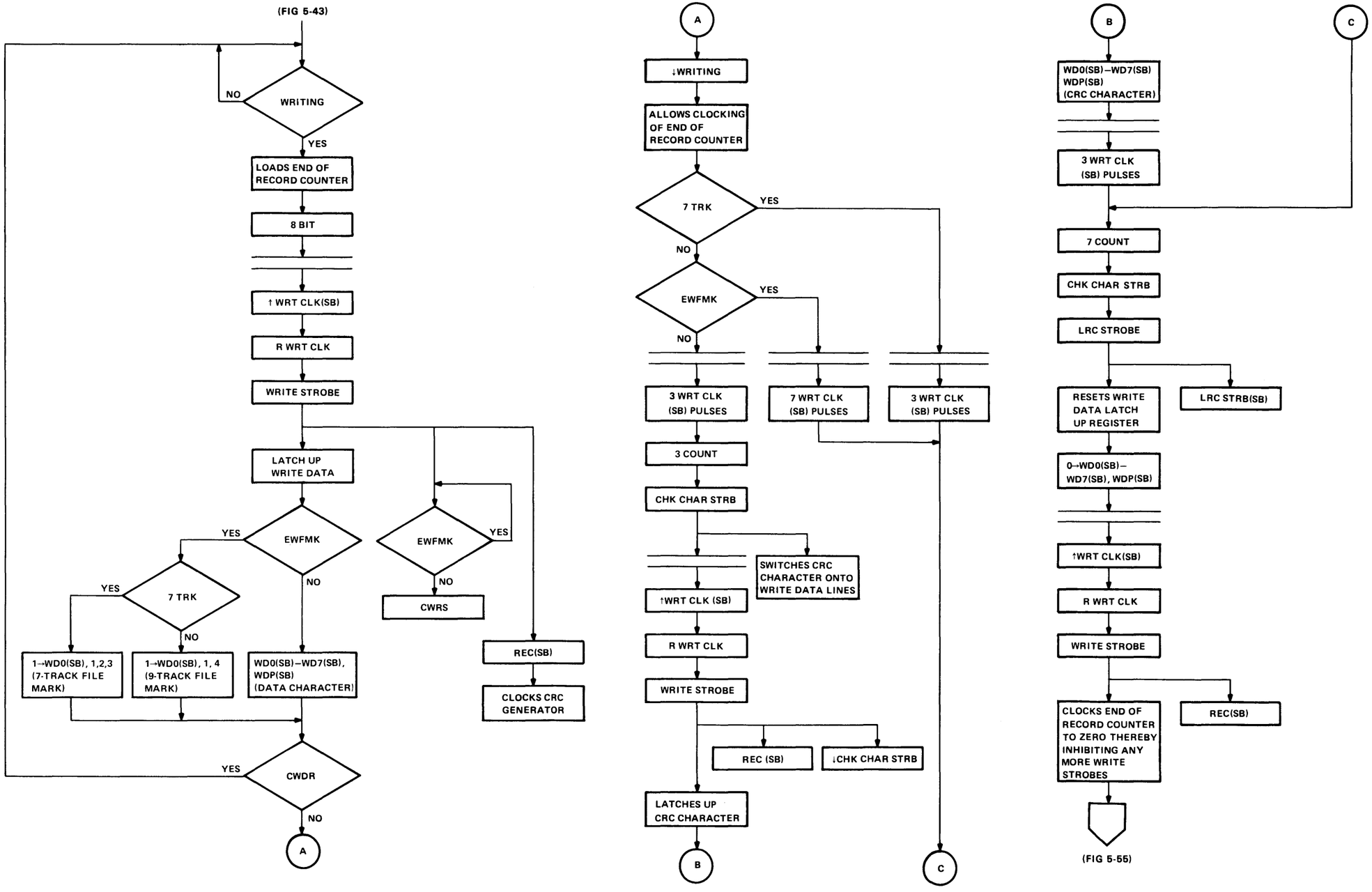


Figure 5-46 Write Flow Diagram

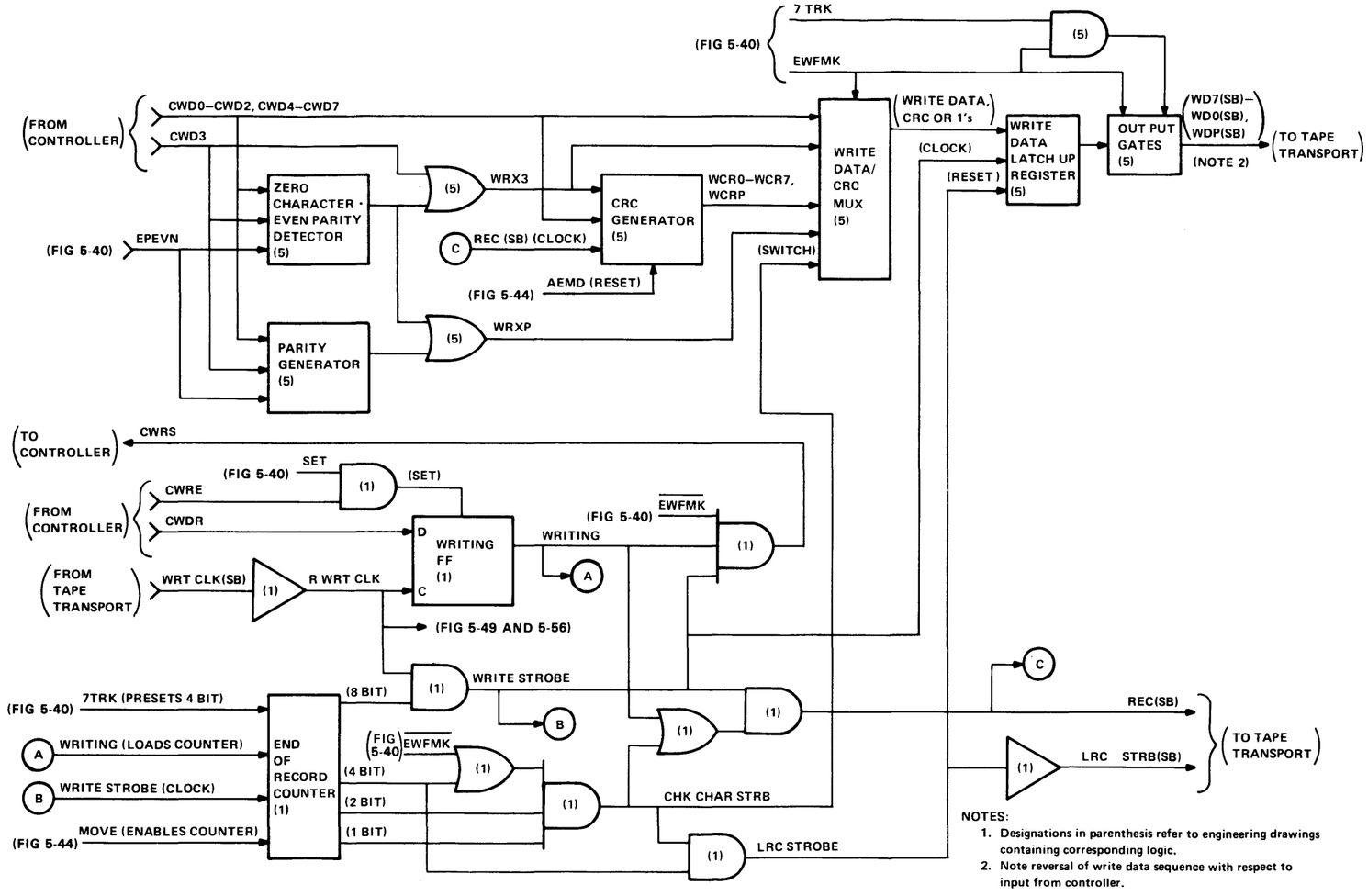


Figure 5-47 Write Block Diagram

The next WRITE STROBE pulse latches up the CRC character and generates a REC (SB) pulse for the drive to record the CRC character. Three WRITE STROBES later, the counter is at a count of 7 and again asserts CHK CHAR STRB, which:

a. Enables the REC AND gate

b. Asserts LRC STROBE via the enabled L RC STROBE AND gate.

LRC STROBE asserts LRC STRB (SB) to the drive and resets the write data latch up register, setting all the write lines to zero. (The LRC character is generated in the drive.) The next WRITE STROBE asserts REC (SB) to record the LRC character and resets the end-of-record counter, thereby inhibiting any further WRITE STROBE pulses.

Summarizing, the 9-track end-of-record sequence is:

a. Last data character
b. Three blanks
c. CRC character
d. Three blanks
e. LRC character
f. Reset end-of-record counter.

3. **Seven-Track Normal** – Seven-track normal operation is identical to 9-track normal except for the write end-of-record sequence. In 7-track operation, both the 4 and the 8 bits of the end-of-record counter are preset to a 1. Thus, when the counter reaches a count of 3, the same conditions exist as a count of 7 in 9-track operation. The 7-track end-of-record sequence is:

   a. The last data character
   b. Three blank spaces
   c. The CRC character
   d. Reset end-of-record counter to terminate the write sequence.

4. **Nine-Track File Mark; Write Data** – In file mark operation, EWFMK is true and forces the write data/CRC mux to output all 1s into the write data latch-up register. After the 1s are clocked into the register, they are applied to the output gates. With EWFMK true and 7TRK false, all the output gates are inhibited except 0, 1, and 4, thus outputting an octal 23 (9-track file mark) to the drive.

   CWRE is true and CWDR is false for a CWFMK command. CWRE allows the SET pulse to set the WRITING flip-flop. The first WRT CLK (SB) pulse asserts WRITE STROBE and then REC(SB), because CWDR is false, also resets the WRITING flip-flop. Thus, one WRITE STROBE and one REC pulse is issued for the file mark character.

   No CWRS pulses are returned to the controller in file mark operation.

5. **Write End-of-Record** – The write end-of-record sequence for a 9-track file mark is identical to the write end-of-record sequence for 9-track normal, except that the CRC character is shipped and only the LRC character is written. The end-of-record counter must reach a count of 7 before a CHK CHR STRB is asserted. At this point, the same conditions exist as in the 9-track normal mode; thus, the LRC character is recorded and the write sequence is terminated. The 9-track file mark end-of-record sequence is:

   a. The last data character (the file mark character)
   b. Seven blank spaces
   c. The LRC character
   d. Reset end-of-record counter to terminate the write sequence

6. **Seven-Track File Mark** – The write data sequence for the 7-track file mark is identical to that for the 9-track file mark except that 7TRK is asserted to the output gates via the enabled EWFMK gate. Output gates now enabled are 0, 1, 2, and 3, thus outputting an octal 17 (7-track file mark) to the drive.

   The end-of-record sequence for the 7-track file mark is identical to that for a 7-track normal sequence.

5.3.7.7 Read Sequence (Figures 5-48 and 5-49)

1. **Read Data** – RSDO (SB) pulses from the drive assert COMP RD STRB, which:

   a. Clocks the read data latch-up register

   b. Triggers the read strobe one-shot, asserting CRDS to the controller

   c. Uses a second output from the read strobe one-shot (CHECK REG PLS) to clock the CRC generator and the LRC generator (and the LRCS flip-flop in the end-of-record detection sequence).

   When the read data latch-up register is clocked by COMP RD STRB, read data is made available to the controller via the read data output mux. (Note the order reversal of the read data in the latch-up register.) When READING is true, the multiplexer selects the data character from the read lines for the controller. When READING is false (i.e., after a data transfer operation), the resultant LRC register is output to the controller for maintenance purposes.

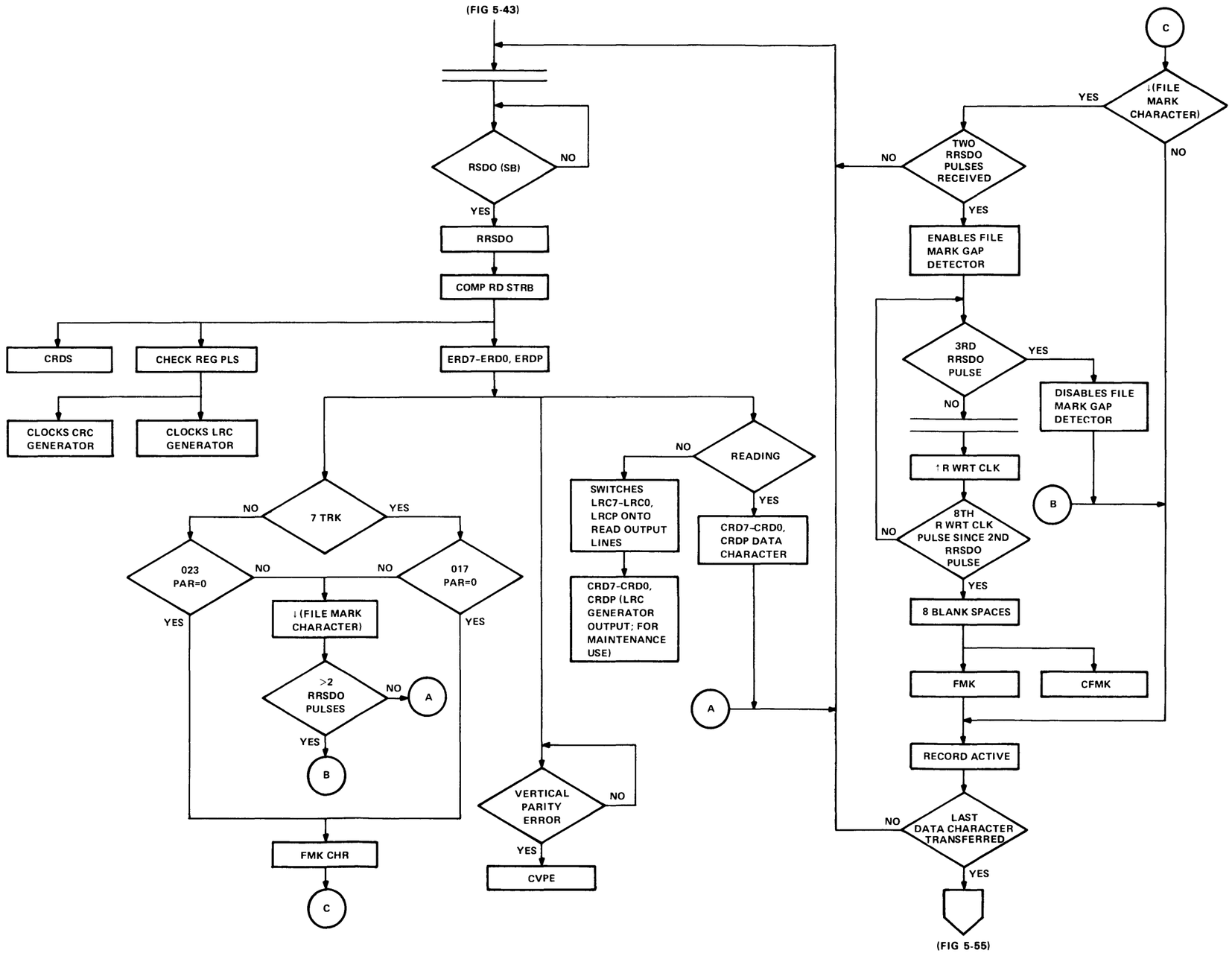
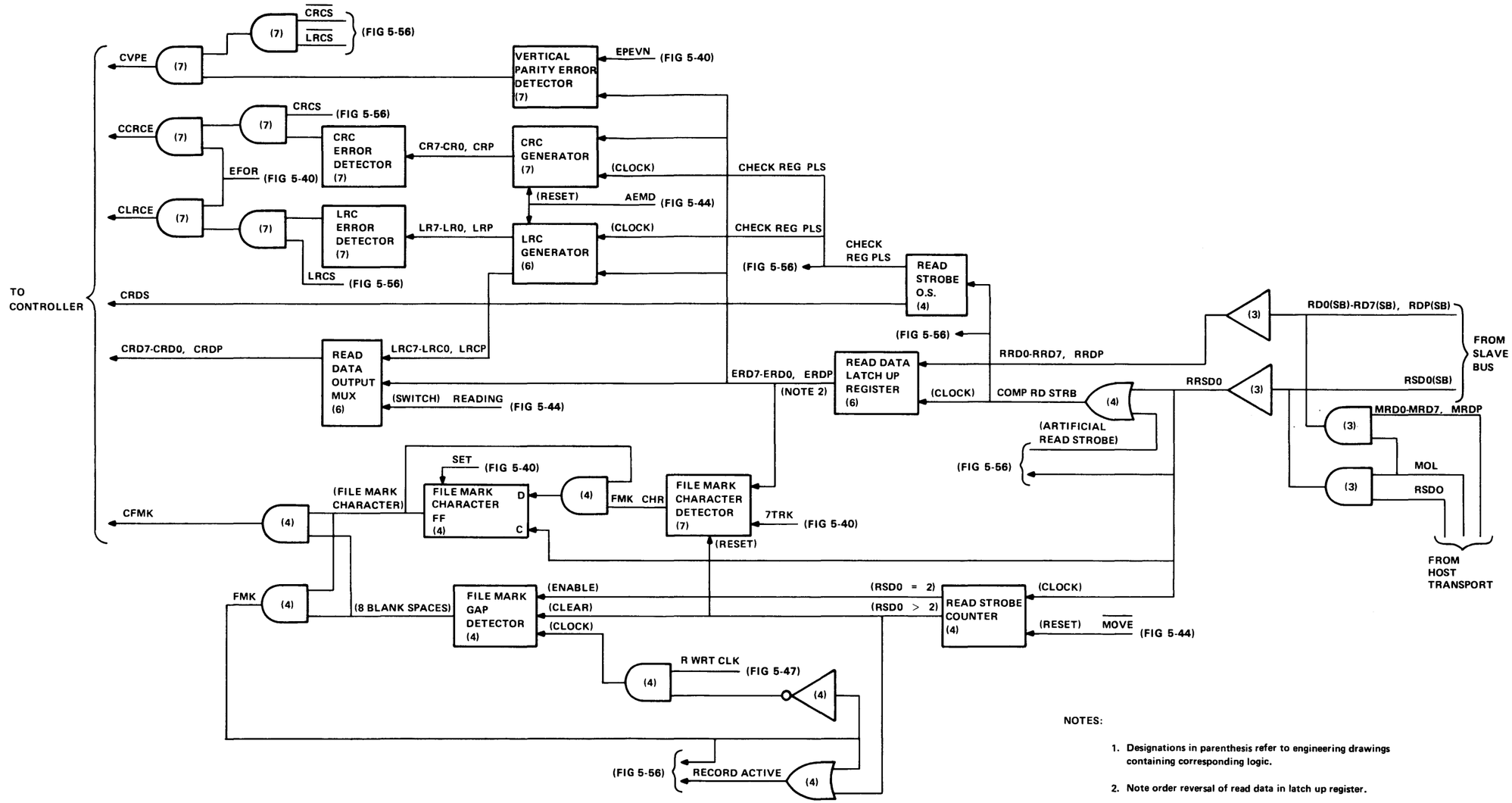


Figure 5-48 Read Flow Diagram



NOTES:

1. Designations in parenthesis refer to engineering drawings containing corresponding logic.
2. Note order reversal of read data in latch up register.

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Figure 5-49 Read Block Diagram

2. **Error Detection (Figures 5-48 and 5-49)** - Read data ERD7-ERD6, ERDP is checked for CRC, LRC, and vertical parity errors. Each data character is clocked into the CRC and LRC generators by the CHECK REG PLS. At the end of the record, the CRC character is compared with the contents of the CRC generator, causing the CR7-CR6, CRP output to be all zeros. The CRC error detector looks for an all-zeros output, resulting from the comparison. If the CRC generator output is not all zeros when CRCS is true, CCRCE is asserted to the controller, indicating a CRC error. In a similar manner, the LRC character is compared with the contents of the LRC generator, causing the LR7-LR0, LRP output to be all zeros. The LRC error detector looks for an all-zeros output, resulting from the comparison. If the LRC generator output is not all zeros when LRCS is true, CLRCE is asserted to the controller, indicating an LRC error.

   CRC and LRC error outputs are enabled only when the drive is executing a forward motion command. (This is due to the location of the CRC and LRC characters at the end of the record.)

   Accordingly, EFOR must be true for CCRCE or CLRCE to assert.

   Each data character occurring during the body of a record is checked for vertical parity error by a vertical parity error detector circuit. If a parity error is sensed by the detector, CVPT is asserted to the controller. CVPE is inhibited during CRCS and LRCS times, as the parity of these characters may be either odd or even, depending on the data contained in the record.

3. **File Mark Detection (Figures 5-48 and 5-49)** - The file mark detection logic monitors the read data and outputs CFMK to the controller if a file mark is detected. Three conditions must be met before the record is identified as a file mark. These are:

   a. There must be two characters in the record

   b. Both characters must be file mark characters

   c. The second file mark character must be followed by at least eight blank spaces.

   To meet condition b, read data (ERD7-ERD0, ERDP) is examined by the file mark character detector, which outputs FMK CHR if a file mark character is sensed. A file mark character flip-flop is set by the SET pulse at the start of the operation and then clocked by RRSDO pulses. The flip-flop is conditioned to set by FMK CHR via an AND gate, such that if the flip-flop is clocked to the reset state, it cannot be set again during the current operation. Thus, the first two characters read must be file mark characters in order to keep the file mark character flip-flop set.

   Conditions a and c are met by means of a file mark gap detector and a read strobe counter. When the read strobe counter reaches a count of two, the file mark gap detector is enabled and starts counting R WRT CLK pulses. When the strobe counter reaches a count of three, RSDO > 2 asserts and resets the gap detector. If the gap detector reaches a count of eight, it outputs 8 BLANK SPACES and CFMK is asserted to the controller via an enabled AND gate. If a third RSDO pulse occurs before the gap detector reaches eight, the detector is cleared and the file mark character flip-flop is reset, indicating that the record is not a file mark and a normal record transfer is in progress.

   The end-of-record detection sequence is enabled from the read data channels via a record active OR gate. If a normal record transfer is in progress (RSDO> 2 is true) or a file mark has been detected (FMK true), RECORD ACTIVE is asserted and enables (but does not start) the end-of-record detection sequence.

4. **Nine-Track Normal; End-of-Record Detection (Figures 5-55, 5-56 and 5-50)** - The end of a record is detected by looking for the three blank spaces that occur between the last data character and the CRC character (LRC character for 7-track). The blank spaces are detected by an end of record counter that is clocked by R WRT CLK pulses and effectively reset by COMP RD STRB pulses. (Actually the COMP RD STRB pulses load the counter with a count of 8.) COMP RD STRB pulses are asserted by RRSDO pulses from the drive. The R WRT CLK pulses and the RRSDO pulses are not necessarily in sync, but they are of the same frequency. Hence, the end-of-record counter is continually being clocked and "reset" during the body of a record. Two R WRT CLK pulses might squeeze between two RRSDO pulses, thereby clocking the counter to a count of two before it is reset, but it should never reach a count higher than two during the body of a record. If the counter does reach a count of three (three R WRT CLK pulses with no RRSDO pulse), 3 COUNT is asserted, signifying that this is the end of the record and the end-of-record sequence is started.

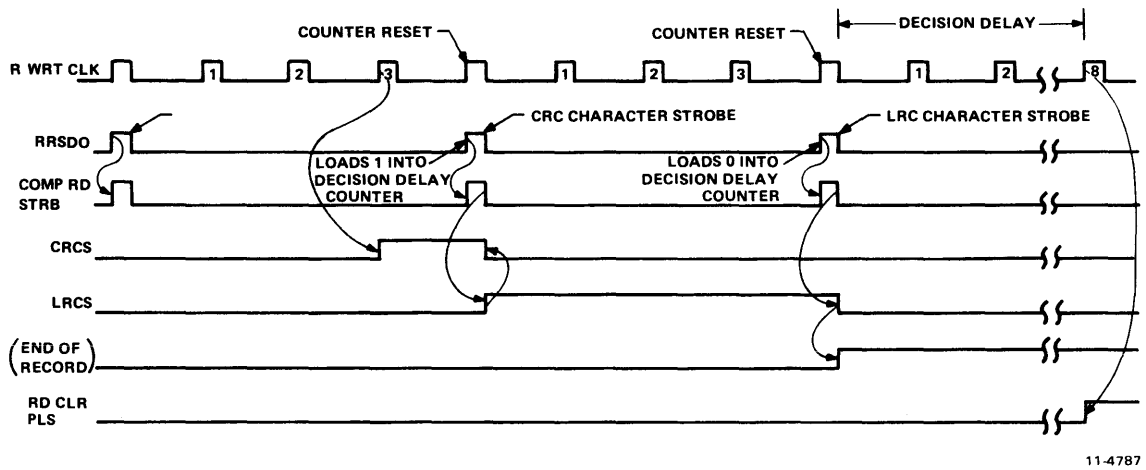


Figure 5-50 End-of-Record Timing, Nonzero CRC and LRC

The assertion of a 3 COUNT clocks the CRCS flip-flop set, outputting CCRCS to the controller and indicating that the next character will be the CRC character. The next RRSDO pulse will be the CRC character strobe, which will:

a. Latch-up the CRC character in the read data latch-up register

b. "Reset" the end-of-record counter

c. Assert CRDS to the controller

d. Assert CHECK REG PLS, which clocks the LRCS flip-flop to the asserted state.

The asserted output of the LRCS flip-flop will reset the CRCS flip-flop and assert CLRCS to the controller, indicating that the next character will be the LRC character. The next RRSDO will be the LRC character strobe, which will:

a. Latch-up the LRC character in the read data latch-up register

b. "Reset" the end-of-record counter

c. Assert CRDS to the controller

d. Assert CHECK REG PLS, which resets the LRCS flip-flop.

The negation of LRCS sets the end-of-record flip-flop, asserting END OF RECORD, which locks the CRCS flip-flop in the reset state until the next operation.

When END OF RECORD asserts, a decision delay period begins. The decision delay period is a time interval (normally eight R WRT CLK pulses long) between the assertion of END OF RECORD and the assertion of RD CLR PLS. The delay period is a "last chance" look for more RRSDO pulses before triggering the drive stop sequence. At the start of the decision delay, the end-of-record counter is "reset" (preset to a count of eight) and starts counting R WRT CLK pulses. When the counter reaches a count of eight, it overflows into the decision delay counter, which then asserts RD CLR PLS to the drive stop logic. Should RRSDO pulses reoccur any time during the decision delay period, the end-of-record counter will be "reset," and the read sequence will continue. When the actual end-of-record does occur, the decision delay count will start again but the end-of-record sequence will not repeat.

The end-of-record sequence is inhibited if a write operation is in progress (WRITING true). During a write operation, defective spots in the tape may simulate a gap and erroneously trigger the end-of-record sequence. In this case the end-of-record logic is functioning to stop the drive while the controller is still trying to write data. To prevent this, -WRITING is gated with the R WRT CLK pulses into the end-of-record counter, thereby allowing the counter to operate only if WRITING is false.

5. **Zero CRC or LRC Characters** – The possibility exists that the CRC or the LRC character could be a zero character, resulting in no corresponding RRSDO pulse being received from the drive. In this case, a COMP RD STRB pulse is generated artificially so clocking of the end-of-record sequence can continue. If no RRSDO pulse is received to "reset" the end-of-record counter, counting will continue up to six, at which time COMP RD STRB will be asserted via a gate enabled by CRCS or LRCS. Figures 5-51 and 5-52 illustrate, respectively, the timing sequence for a zero CRC and a zero LRC character.

The decision delay is normally eight R WRT CLK pulses long but is extended to 24 pulses if no LRC character is detected. Failure to detect an LRC character may be because the character is zero, but it could also be due to a bad area in the tape. Thus, when no LRC character is detected, some doubt exists whether the end of the record has been reached.

Extending the decision distance to 24 pulses provides extra assurance that the end of the record has been reached. The decision delay counter is a down counter, which is loaded by each RRSDO pulse. The counter is loaded with zeros except for the 1 bit that is loaded with LRCS. If there is an LRC character, then LRCS is true during the last RRSDO pulse (Figure 5-50) and the counter is loaded with all zeros. If there is no LRC character, then LRCS is false during the last RRSDO pulse (Figure 5-52) and the delay counter is loaded with a 1. In this case, the end of record counter must count an additional 16 pulses to count down the 1 and assert RD CLR PLS.

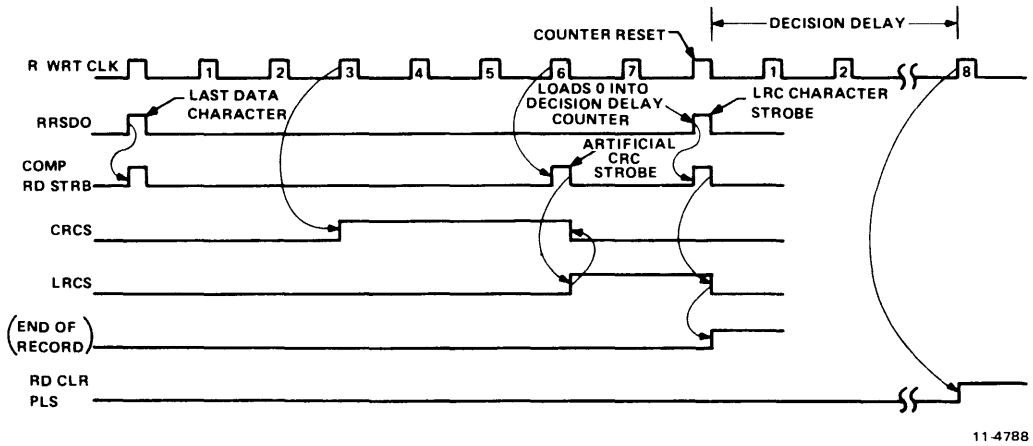


Figure 5-51 End-of-Record Timing, Zero CRC

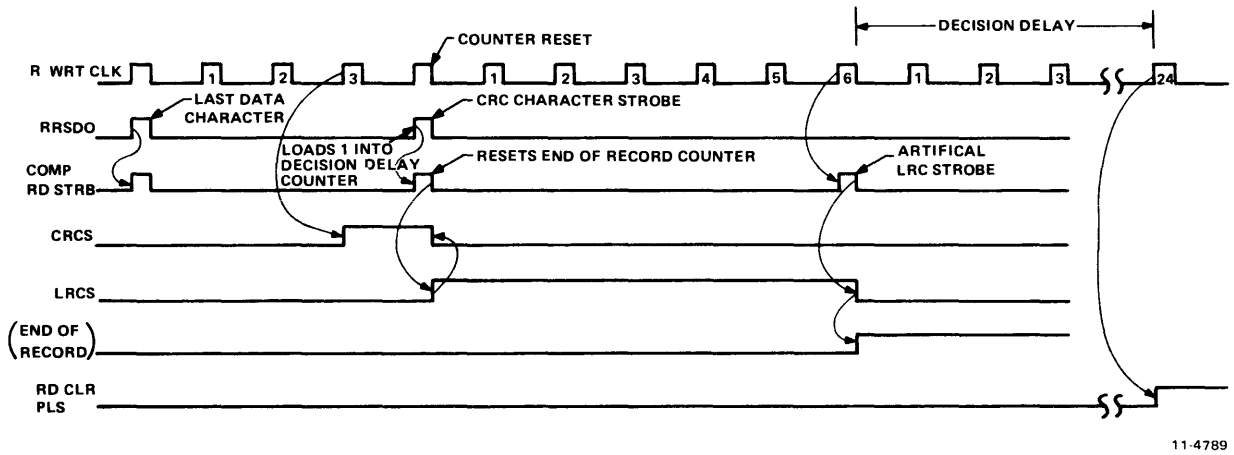


Figure 5-52 End-of-Record Timing, Zero LRC

6. **Seven-Track and File Mark (Figures 5-53 and 5-54)** – In 7-track or file mark operation, the end-of-record sequence is modified to eliminate the CRC character from the sequence. With either FMK or 7TRK true, the three count output from the end-of-record counter directly sets the LRCS flip-flop, which in turn holds the CRCS flip-flop reset. When in file mark operation, the decision delay is 8 R WRT CLK pulses.

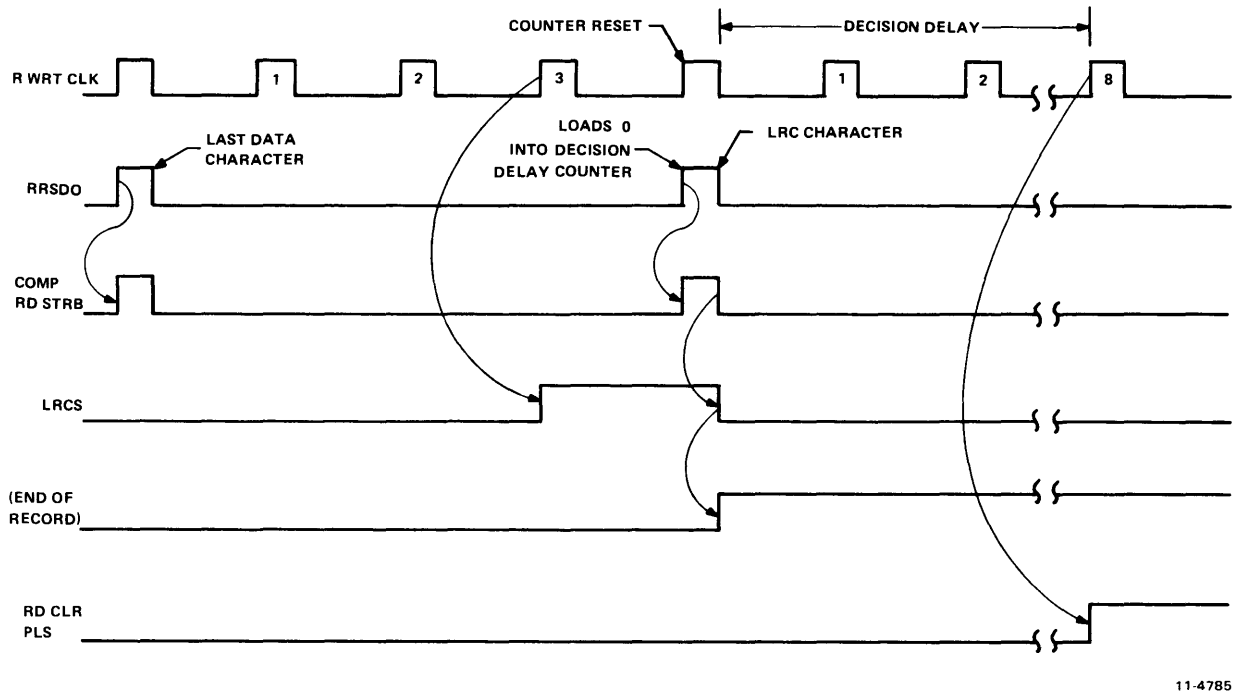


Figure 5-53 End-of-Record Timing, 7-Track

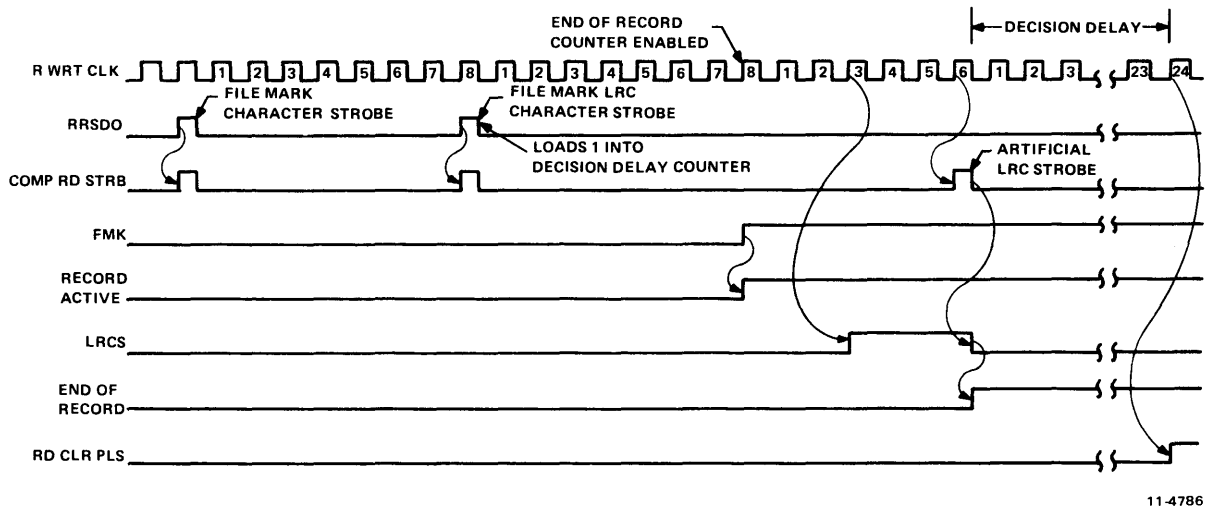


Figure 5-54 File Mark Timing

5.3.7.8 Drive Stop (Figures 5-43, 5-44 and 5-57) - RD CLR PLS triggers the drive stop sequence by setting the EMD flip-flop and asserting EMD (SB) to the drive. The output of the EMD flip-flop also loads the motion delay counter with the data set onto read lines RRD0–RRD6, RRDP by the drive. Bit 13 of the counter is preset to a 1. The bit 14 output, which has been a 1 all during the record transfer, is connected to the data input of bits 14 and 15. Thus, when EMD loads the counter, output bits 13, 14, and 15 become 1s. READING negates due to exclusive ORing of output bits 14 and 15 while bit 13 gates clock pulses into the counter from the divide-by-four counter. The divide-by-four counter receives CLOCK (SB) pulses from the slave bus. An output from the divide-by-four counter is obtained after the first two CLOCK pulses and every four CLOCK pulses thereafter. After the delay period the motion delay counter is clocked reset and:

1. Input clock pulses to the delay counter are inhibited (bit 13 = 0).

2. ACCD (SB) is asserted to the drive (bit 14 = 0) and inhibits WRT CLK pulses from the drive to the write logic.

The assertion of ACCL resets the MOVE flip-flop, which negates MOVE and asserts STOP(SB) to the drive, thereby terminating the command operation.

5.3.8 M8927 Interface Module Description

As stated in Paragraph 1.2.1, the TE10N Tape Transport is based upon the TE16. The TE16 becomes a TE10N when an M8927 interface module replaces the three standard cable cards (M9001, M9001-YA, and M8913) in a TE16. This is done to achieve an interface with a negative logic tape controller or when adding additional tape drives to a system using a negative logic tape drive bus.

5.3.8.1 General - Figure 5-58 is a block diagram of the M8927 interface module. The signals on the negative-voltage slave bus are described in Table 5-6. The signals on the positive-voltage TU10W slave bus are described in Table 5-7. The M8927 interface logic primarily converts slave bus signals from one logic polarity to the other. The signals are grouped in four categories: multiplexed, control/status, write data, and read data; and are discussed accordingly in this chapter. In the functional block diagrams in this section, the signal connectors shown interfacing with the positive slave bus also show a lettered connector orientated toward the lower edge of the illustration. These refer to the six module connectors that plug into the TU10N logic assembly and carry the positive slave bus to the "host" TU10N.

5.3.8.2 Multiplexed Interface (Figure 5-59) - BSET from the negative slave bus is converted to positive logic by Q25 and triggers a slave set one-shot that outputs SLAVE SET PLS(SB) to the positive bus. The Q25 output also clocks command data into command latch-up flip-flops. The command data is coupled from the negative slave bus via negative-to-positive converts Q17 through Q20. The command data must be latched up for the positive slave bus, as it is present on the negative slave bus only while BSET is true. [The reverse (BREV) command is also latched up by the SET pulse. BREV is not multiplexed with status information and therefore appears in Figure 5-61, the Control/Status Interface Block Diagram.] The forward (FOR) and rewind (REW) commands are output to the TE10W bus as FWD(SB) and RWND(SB). The off-line (OFF) and write enable (WRE) commands are ORed together and output to the TU10W bus as WRITE(SB). An off-line command asserts WRITE(SB) because an off-line operation is indicated on the TE10W slave bus by the simultaneous assertion of WRITE(SB) and RWND(SB).

When BSET negates and if a transport on the positive slave bus has been selected (MOL is true), four status gates are enabled that couple RWS(SB), WRL(SB), END PT(SB), and BOT(SB) to the negative slave bus via positive-to-negative converters Q46 through Q43.

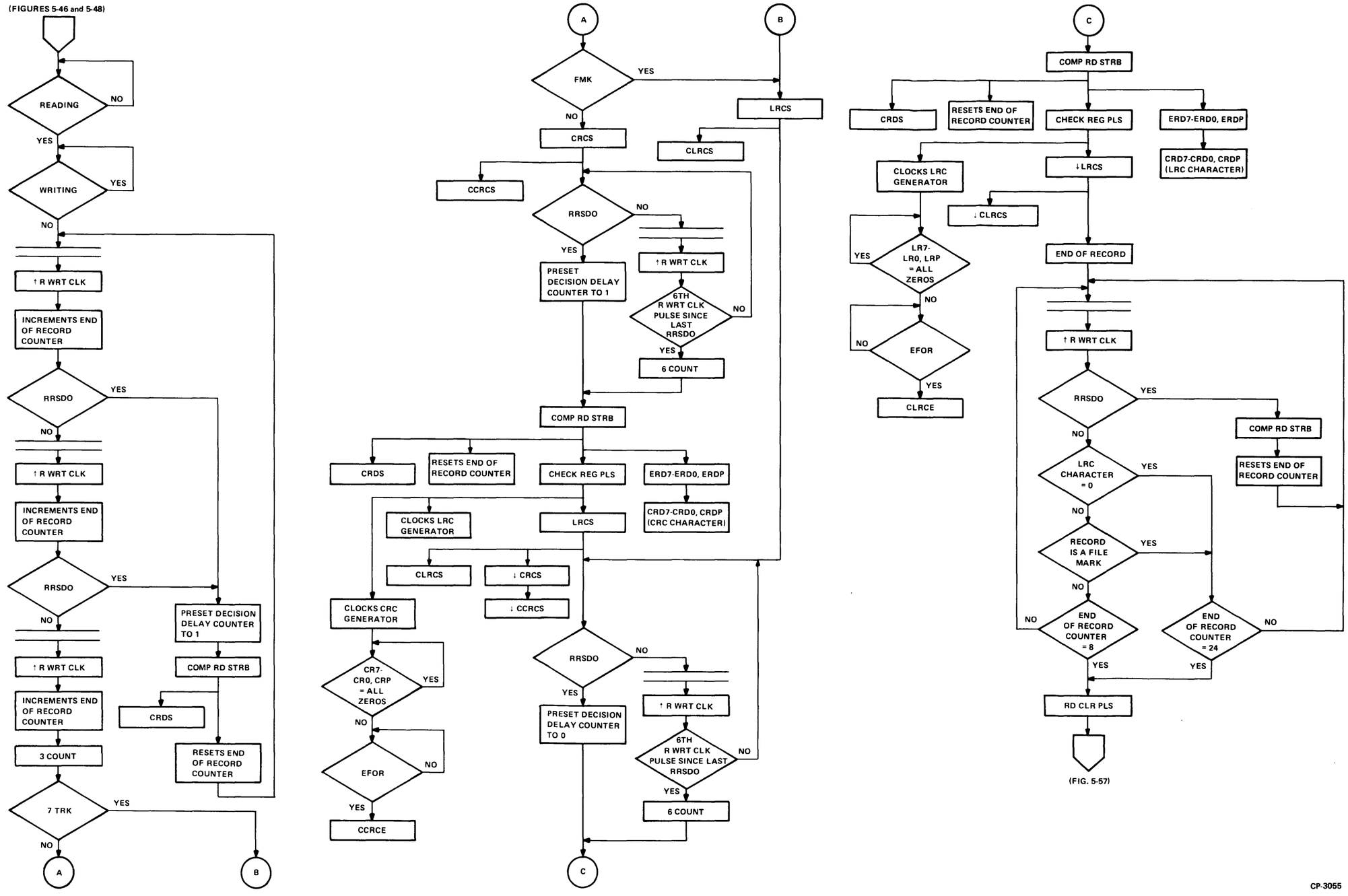


Figure 5-55 End-of-Record Flow Diagram

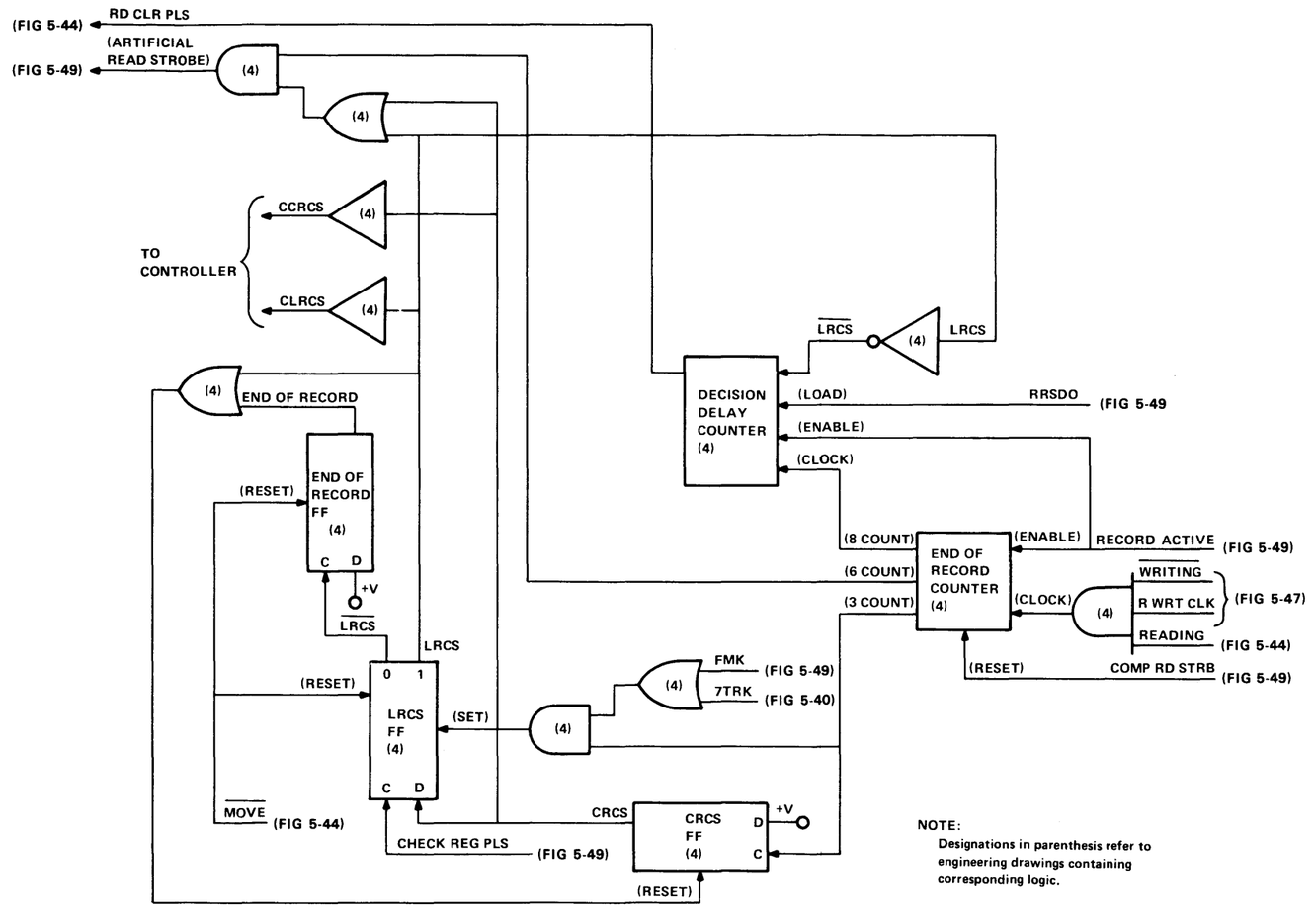


Figure 5-56 End-of-Record Block Diagram

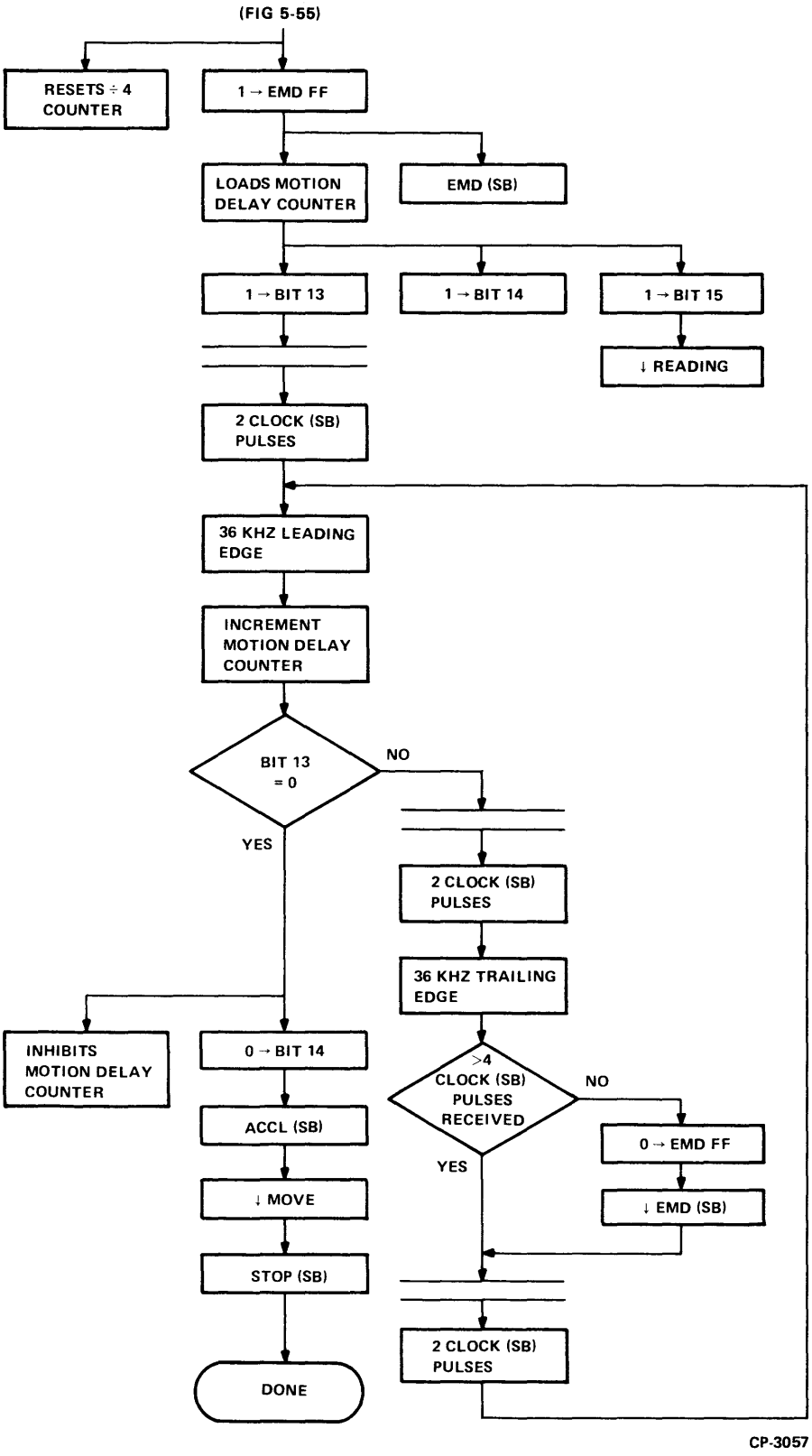
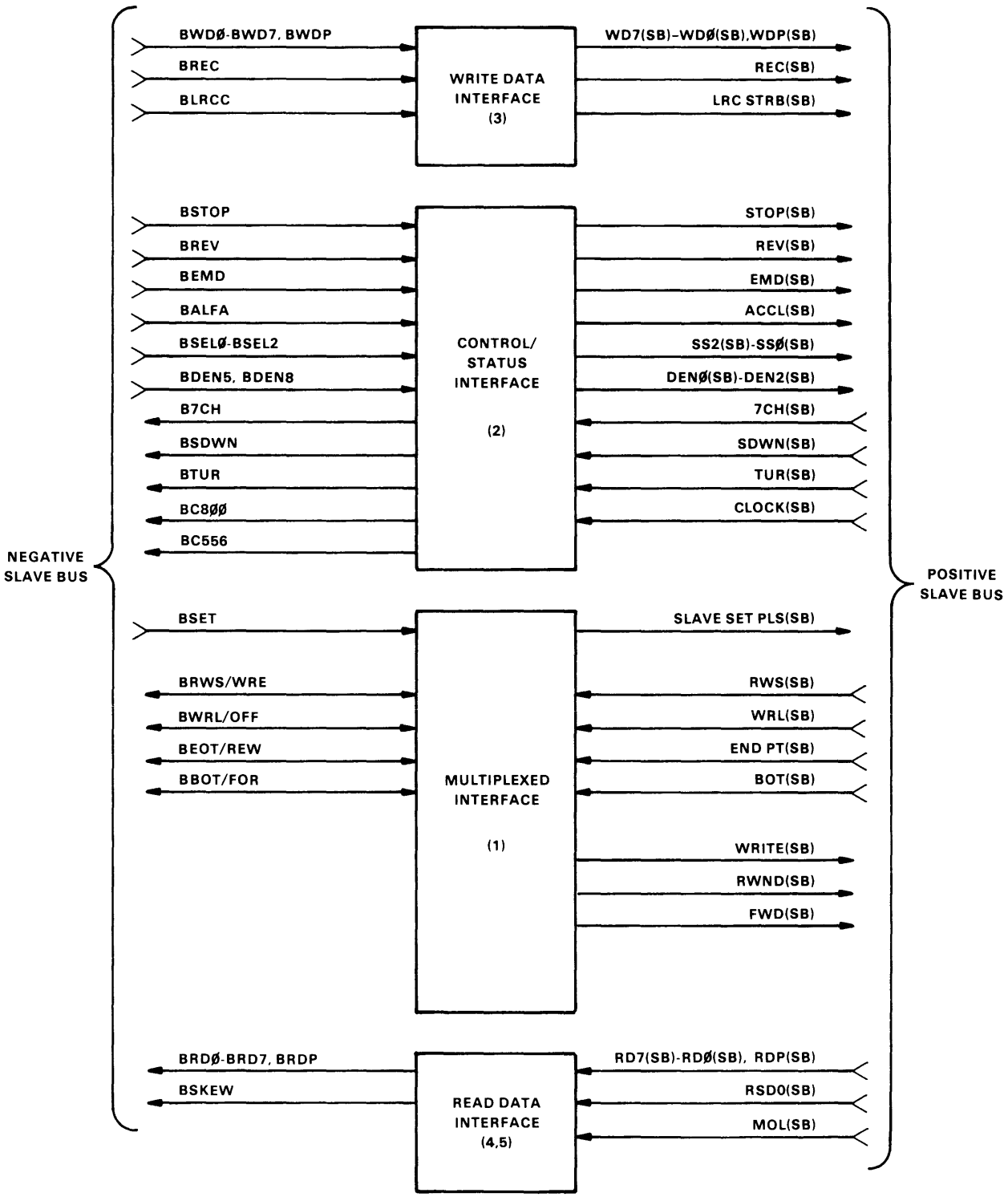


Figure 5-57 Drive Stop Flow Diagram



NOTE:
Designations in parenthesis refer to engineering drawing number containing corresponding logic.

CP-3058

Figure 5-58 M8927 Block Diagram

Table 5-6 Negative Slave Bus Signals

Bus Signal	Function
BSEL0-BSEL2	A 3-bit code that selects one of eight possible drives for command execution.*
BREV	Commands a reverse motion operation.*
BRWS/WRE	A multiplexed line that carries a write enable command* when BSET is true and rewind status** when BSET is false.
BWRL/OFF	A multiplexed line that carries an off-line command* when BSET is true and write lock status** when BSET is false.
BEOT/REW	A multiplexed line that carries a rewind command* when BSET is true and an end-of-tape indication** when BSET is false.
BBOT/FOR	A multiplexed line that carries a forward motion* command when BSET is true and a beginning-of-tape** indication when BSET is false.
BDEN5, BDEN8	A 2-bit code* that indicates the recording density on the tape (200 bit/in, 556 bit/in, 800 bit/in) for a write operation (BC556).
BSET	A pulse* that initiates the response of the selected drive to the input commands.
BEMD	A pulse* asserted at BSET time that places a motion delay code onto bus read lines BRD1-BRD7, BRDP. The controller will not allow a data transfer to start until the delay period specified by the code has expired and the tape has come up to speed.
BALFA	Negates when the motion delay period is over and a data transfer can start.*
BWD0-BWD7, BWDP	Nine bus lines carrying the data character to be written on tape. The data character consists of 8 data bits and 1 parity bit.*
BREC	The recording pulse for the tape drive. There is one BREC pulse for each data character to be written.*
BLRCC	Asserted after the body of a record has been written. It indicates the LRC character can now be written.*
BRC0-BRD7, BRDP	Nine bus lines carrying the data character read from tape. The data character consists of 8 data bits and 1 parity bit. During the BEMD pulse, the read data lines carry the motion delay code.**
BSKEW	A read strobe pulse generated for each data character read from tape.**

* = generated by controller
** = generated by selected slave

Table 5-6 Negative Slave Bus Signals (Cont)

Bus Signal	Function
BC800	A 36 kHz clock present when MOL(SB) is true. Used to clock write strobes (BREC) when a DEN code of 800 bits/in is selected. Controller divides BC800 by four when 200 bits/in is selected.**
BC556	A 25.02 kHz clock present when MOL(SB) is true and a 556 bits/in DEN code is asserted. Used to clock write strobes (BREC).**
B7CH	Asserted by the selected drive if it is a 7-track transport.**
BSDWN	Asserted while the capstan motor is decelerating. Negates when the motor is stopped.**
BTUR	Asserted when the capstan motor has stopped and the drive is ready to accept a new command.**
BSTOP	Command signal, asserted by controller, which causes the capstan motor to stop. BSTOP is negated when SET pulse is asserted to initiate a tape motion operation.

* = generated by controller
** = generated by selected slave

Table 5-7 Positive Slave Bus Signals

Slave Bus Signal	Function
Slave Select [SS(0:2)(SB)]	These lines select a tape transport on the positive slave bus for command execution.
Forward [FWD(SB)] Reverse [REV(SB)] Rewind [RWND(SB)] Write Enable [WRITE(SB)]	These are the four command lines that determine mode of operation of the selected transport.
Slave Set Pulse [SLAVE SET PLS(SB)]	This signal initiates response of the selected drive to the four command lines.
Stop [STOP(SB)]	This signal causes the drive to terminate motion. (Does not apply to rewind, which terminates independently.)
Enable Motion Delay [EMD(SB)]	Asserted to the drive at set pulse time.

Table 5-7 Positive Slave Bus Signals (Cont)

Slave Bus Signal	Function
Accelerate [ACCL(SB)]	Asserted by the controller while the transport is getting up to speed or not moving tape.
Write Data [WD(0:7,P)(SB)]	These nine lines transmit data to be written by the drive.
Record [REC(SB)]	A pulse that causes data to be written on tape.
Density Select [DEN(0:1)(SB)]	These two lines control the density at which data is written on tape. They also represent the density of tape data during a read operation.
Clock [CLOCK(SB)]	A 144-kHz clock, generated in the selected TU10N or TU10W; present at all times when the unit is on-line.
Write Clock [WRT CLK(SB)]	Not used.
LRC Strobe [SRC STRB(SB)]	Asserted by the interface logic prior to the REC pulse that writes the LRC character.
Read Data [RD(0:7,P(SB)]	These nine lines transmit read data from the selected TU10N or TU10W to the M8927 module.
Read Strobe Delay Over [RSDO(SB)]	A read strobe pulse generated by the transport at the end of the skew delay.
Beginning of Tape [BOT(SB)]	Asserted when the drive detects the beginning-of-tape marker.
End of Tape [END PT(SB)]	Asserted when the drive detects the end-of-tape marker.
Rewind Status [RWS(SB)]	Asserted while the selected drive is performing a rewind operation.
7-Channel [7CH(SB)]	Asserted when the selected drive is a 7-track transport.
Medium On-Line [MOL(SB)]	Asserted by a selected, powered drive that is loaded with tape.
Tape Unit Ready [TUR(SB)]	Asserted by a selected drive to indicate that tape motion has stopped.
Settle Down [SDWN(SB)]	Asserted while the transport is decelerating.
Write Lock [WRL(SB)]	Asserted when the selected drive detects that the write-enable ring has been removed from the tape reel.

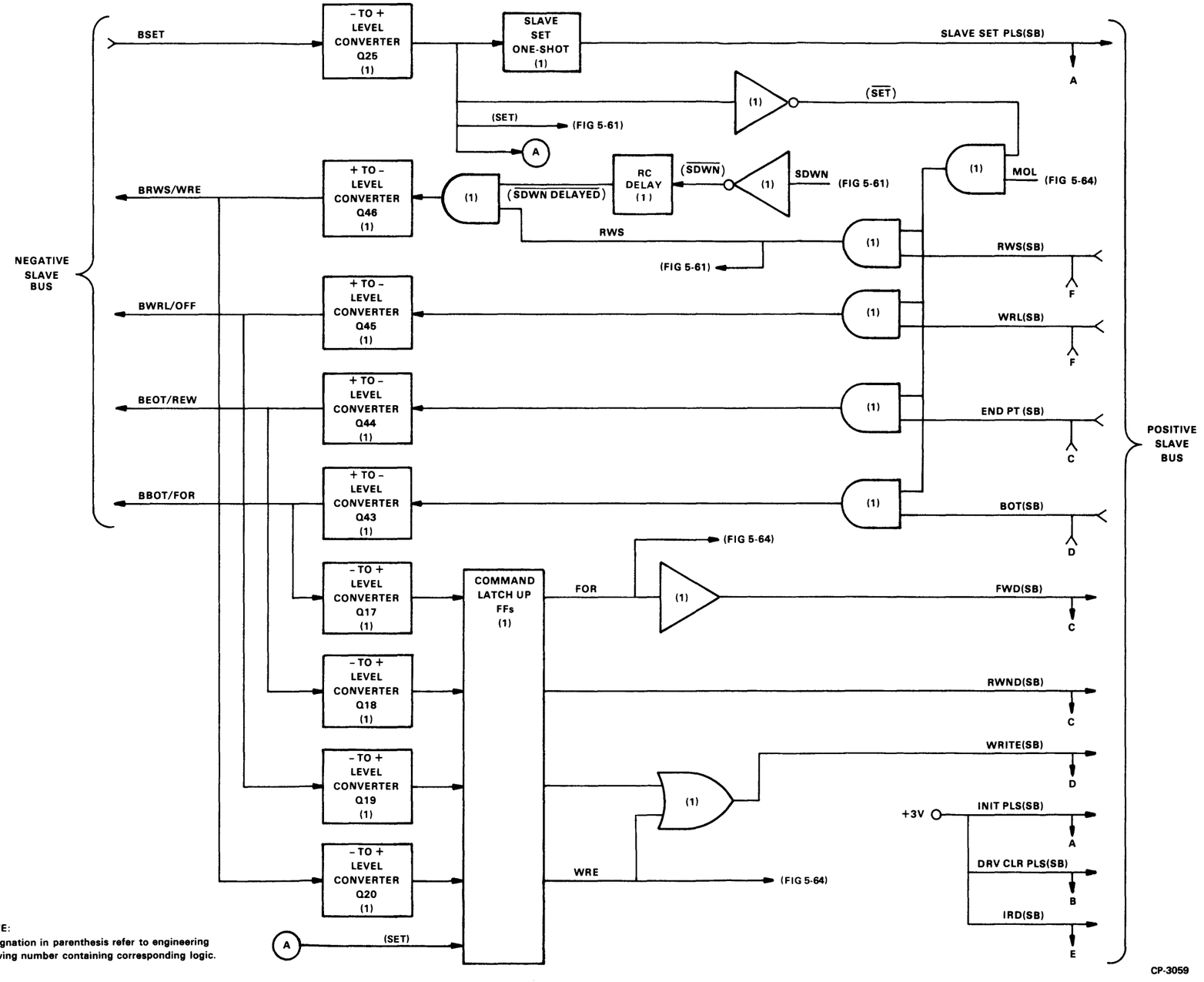


Figure 5-59 Multiplexed Interface Block Diagram

The rewind status signal [RWS(SB)] passes through a second gate prior to its conversion to negative logic. The purpose of the second gate is to cause BRWS to negate before RWS(SB). RWS(SB) from the TE10N or TE10W drive negates at the end of SDWN(SB) simultaneous with the assertion of TUR(SB) (see Figure 5-60).

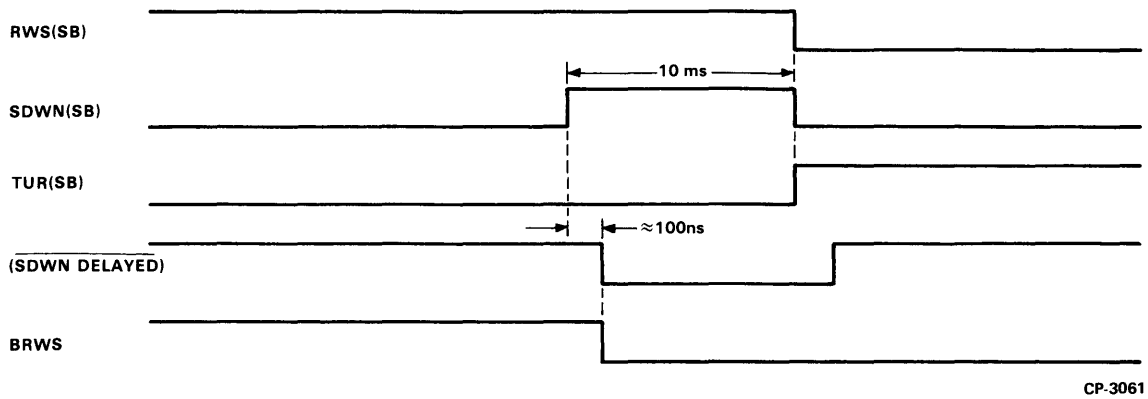


Figure 5-60 RWS(SB) and BRWS Timing Diagram

A timing requirement within the controller demands that BRWS negate before BTUR asserts. This requirement is met by ANDing RWS(SB) with -SDWN DELAYED, thus producing the proper BRWS timing as shown in Figure 5-60. -SDWN is delayed approximately 100 ns and becomes -SDWN DELAYED before being ANDed with RWS(SB). This is done to eliminate the possibility of a spurious assertion (i.e., race condition of BRWS) should SDWN(SB) negate while RWS is still true.

The drives on the positive slave bus require that unused bus lines INIT PLS(SB), DRV CLR PLS(SB), and IRD(SB) be held high; thus the application of +3 V to these three lines on the M8927 module.

5.3.8.3 Control/Status Interface (Figure 5-61) - Control signals BDEN5, BDEN8, BSTOP, BREV, BSEL0-BSEL2, BEMD and BALFA are converted from negative to positive logic for the TE10W slave bus. Note the order reversal of the BSEL input lines with respect to the SS output lines. Note that the reverse command line (BREV) is latched by SET during a reverse motion operation. Another requirement during a rewind operation is that ACCL(SB) be true to inhibit the tape transport from making a data transfer from the tape. Hence the application of RWS to the ACCL(SB) line on the positive slave bus.

Status lines 7CH(SB), SDWN(SB), and TUR(SB) are ANDed with MOL before being converted to negative logic. Thus, a drive on the positive slave bus (either the TE10N or a TE10W) must be selected before these status signals will be placed on the negative slave bus.

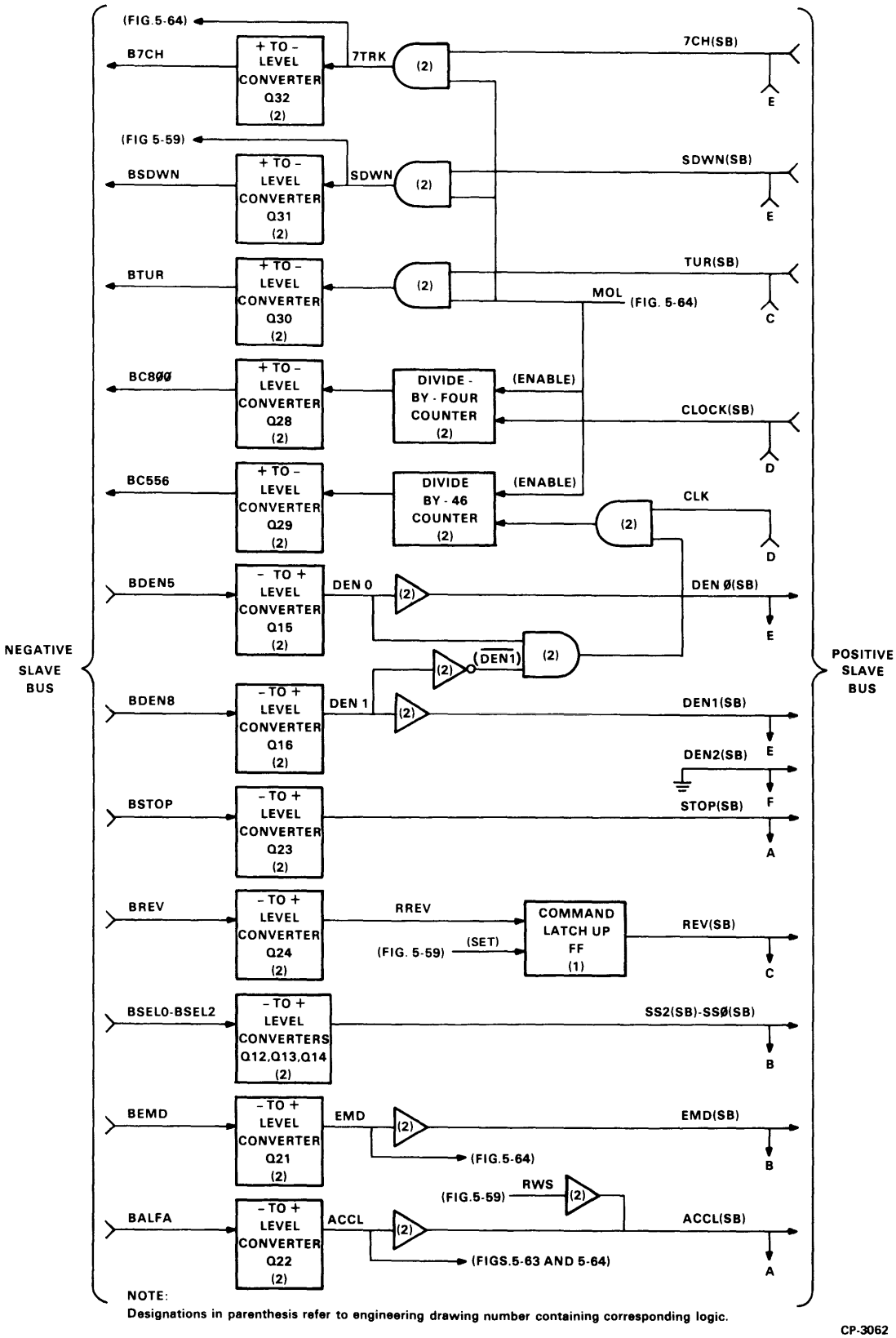


Figure 5-61 Control/Status Interface Block Diagram

Count down circuits are used to generate BC800 and BC556 clock signals for the negative slave bus. A CLOCK(SB) signal of 144 kHz is received from the positive slave bus, reduced to 36 kHz by a divide-by-four counter, converted to negative logic by Q28, and output as BC800. A CLK input of 1.152 MHz is received from the TE10N "host" drive, reduced to 25 kHz by a divide-by-46 counter, converted to negative logic by Q29, and output as BC556. The selected tape drive must be on the positive slave bus (MOL true) to enable the divide-by-four and the divide-by-46 counters. An additional requirement for the assertion of the BC556 clock is that the DEN code for 556 bits/in be true. The 556 bits/in DEN code is BDEN5 (DEN 0) true and BDEN8 (DEN 1) false.

The logic for the divide-by-46 counter is on Sheet 2 of Engineering Drawing CS-M8927. Figure 5-62 is a timing diagram of the counter operation and should be referenced along with the circuit schematic during the following discussion. Counter E11 is clocked by the CLK input from the "host" drive. E11 is a 4-bit counter whose R3(1) asserted output clocks E9-3, alternately setting and resetting the E9 flip-flop. Note that when E9 resets, the cycle is distorted by the action of one-shot flip-flop E5. Each time E9 resets, E9-6 goes high and triggers one-shot E5. The output from E5 presets counter E11 to a count of one. (This is the actual starting condition represented at time zero in Figure 5-62.) Thus, each time the counter is loaded, only seven clock pulses are required to assert R3(1) instead of eight. On the 23rd clock pulse, E9-6 goes high again, thereby presetting counter E11 to one and the cycle is repeated. E9-11 is clocked by the E9-5 output, resulting in the E9-9 output shown in Figure 5-62. E9-9 and E9-6 are ANDed by E13, generating the E13-8 output, which is the 25 kHz clock output from the divide-by-46 counter. It can be seen from Figure 5-62 that the ratio between the CLK input waveform and the E13-8 output waveform is 46-to-1.

5.3.8.4 Write Data Interface (Figure 5-63) - Write data BWD0-BWD7, BWDP on the negative slave bus is converted to positive logic by negative-to-positive converters Q1 through Q9 and then applied to write data latch-up flip-flops. When the flip-flops are clocked, the write data is output to the positive slave bus in a reversed order [i.e., WD7(SB)-WD0(SB), WDP(SB)]. BREC is converted to positive logic and triggers a one-shot that outputs the recording pulse REC(SB) to the positive bus. The REC converter output also serves as the clock for the write data latch-up flip-flops. BLRCC from the negative slave bus is converted to positive logic and sets the LRC STRB flip-flop. The assertion of LRC STRB(SB) on the positive slave bus indicates that the body of the record has been written and the LRC character can now be written. The LRCC converter output resets the write data latch up flip-flops, setting write lines WD7(SB)-WD0(SB), WDP(SB) to zero. (The LRC character is generated internally within the selected drive.)

BREC, BLRCC, and the nine write data lines are not coupled through the M8927 module unless MOL from the positive slave bus is true. Thus, the host drive or a TE10W must be selected before any of the write signals are placed onto the positive slave bus.

MOL enables the write signal lines by asserting a -0.7 V bias voltage to level converters Q1 through Q11. A -6.3 V from the "host" drive is the source for the -0.7 V bias voltage.

Another -0.7 V (independent of MOL) and a -2.4 V are also derived from the -6.3 V input and serve as operating voltages for the M8927 module.

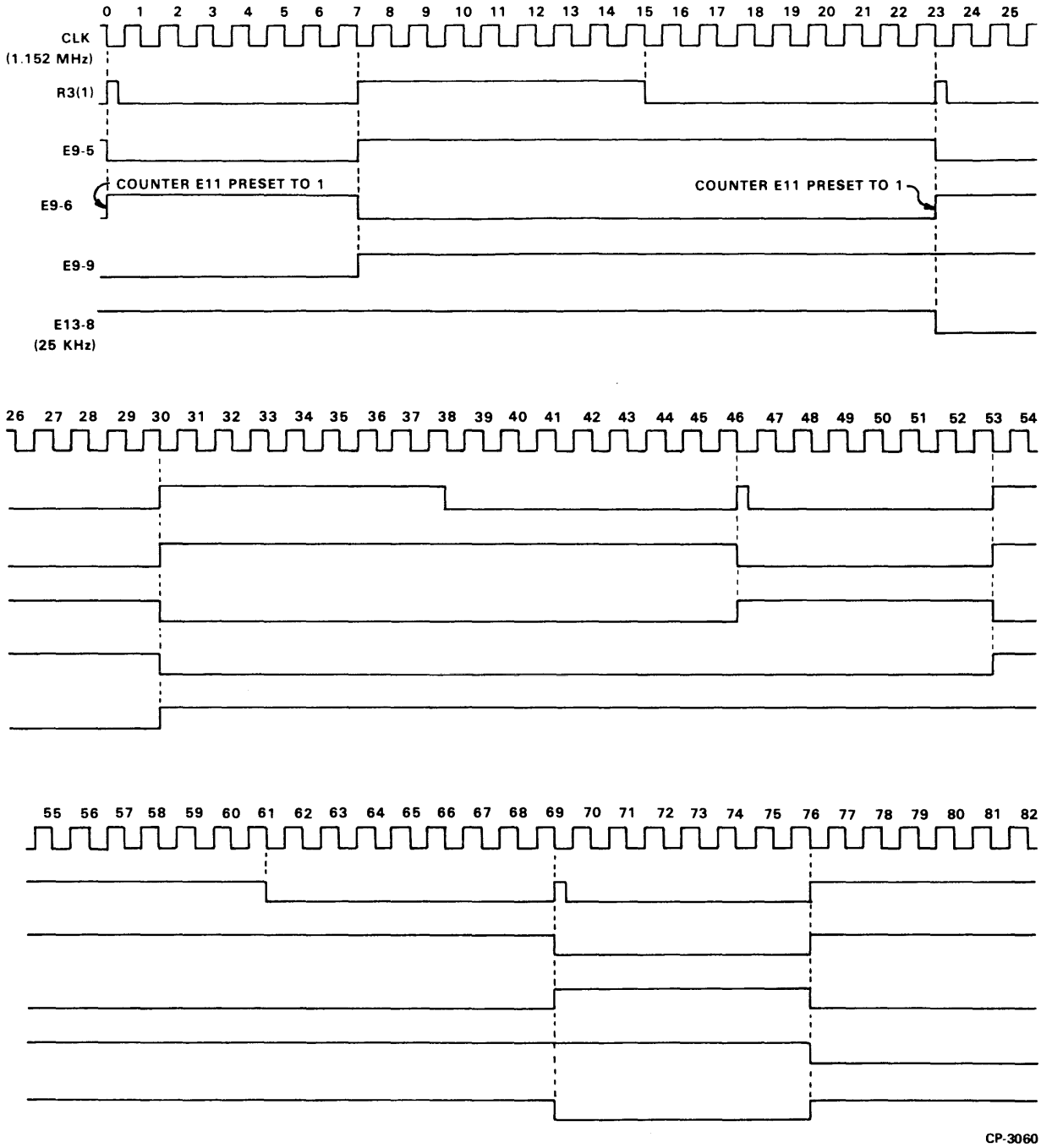


Figure 5-62 Timing Diagram of Divide-by-46 Counter

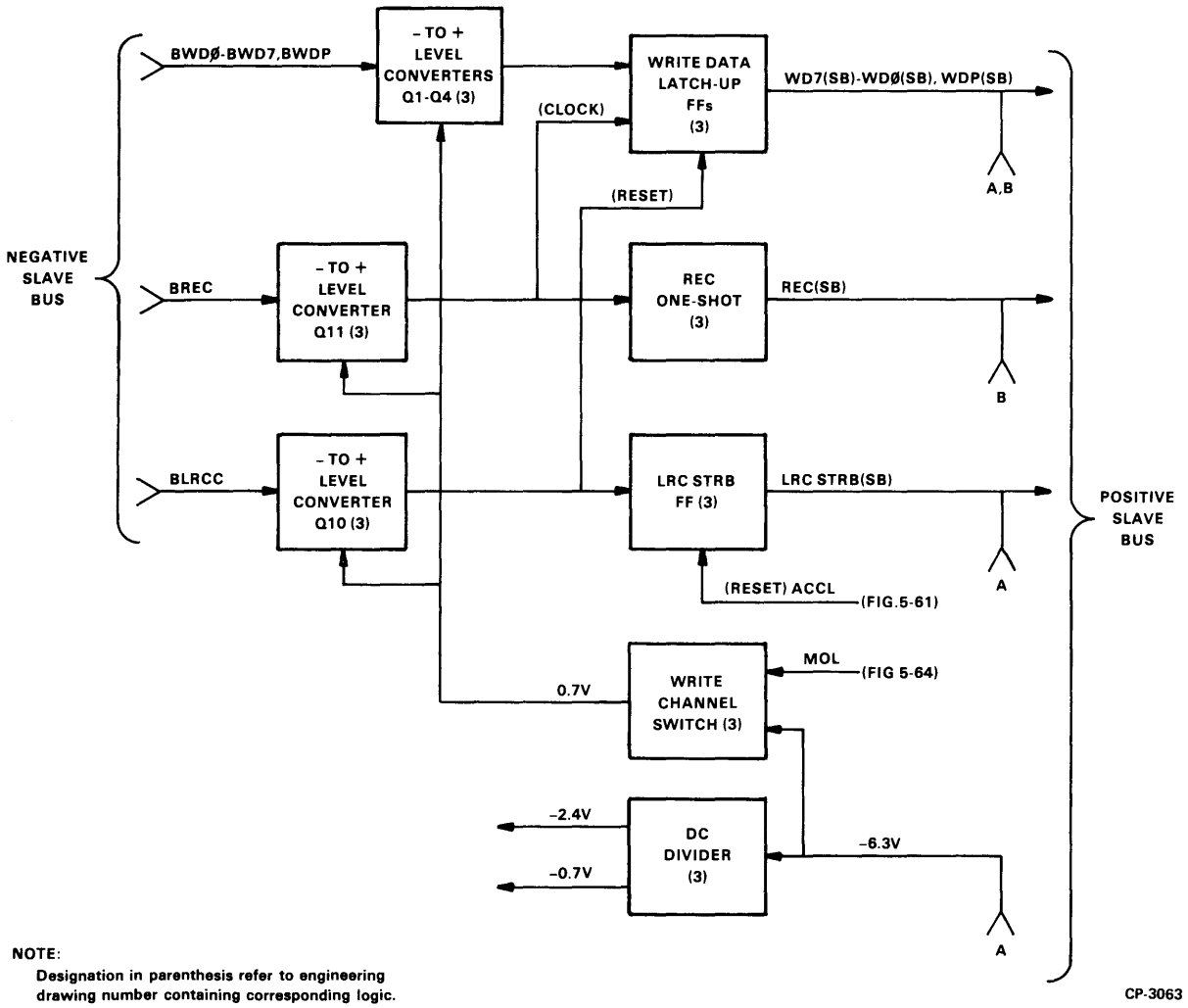


Figure 5-63 Write Data Interface Block Diagram

5.3.8.5 Read Data Interface (Figure 5-64) – Read data RD7(SB)-RD0(SB), RDP(SB) is received from the positive slave bus and applied to read data flip-flops. The flip-flops are clocked by RSDO(SB) pulses also received from the positive slave bus. (Note that the logic that gates the TE10N read data and RSDO pulses to the positive slave bus is on the M8927 module.) The output of the read data flip-flops, which is in reverse order with respect to the input, is converted to negative logic by level converters Q33 through Q41 and placed onto the negative slave bus. Data bit RD0 is directly coupled from the read data flip-flops to the level converters. Data bits RD1-RD7, RDP are applied to the converters via a read data/delay mux. In the body of the record, the mux passes the read data to the negative slave bus. At BSET time EMD asserts, which in turn asserts DELAY switch (if MOL is true) and switches the mux. Thus, if a drive on the positive slave bus is selected (TE10N or TE10W), the EMD pulse switches the delay code from the delay ROM onto read lines RD1-RD7, RDP. The delay code is used by the controller to establish the delay period for capstan motor acceleration and deceleration. The delay code is a function of the type of drive selected (7TRK), whether the drive is starting or stopping (ACCL), and the type of operation the drive is executing (WRE, FOR). The delay periods are shown in Table 5-8.

RSDO(SB) pulses trigger a skew one-shot. The one-shot output is gated with MOS, converted to negative logic by Q42 and placed on the negative slave bus. Each SKEW pulse resets the read data flip-flops via a read data reset one-shot.

5.3.9 TE16 Switch Box

The TE16 switch box is illustrated on the 5412347 circuit schematic. All of the switches in the switch box are Hall-effect switches and, therefore, require +5 V to operate. They are solid-state momentary, not mechanical, switches. The outputs are low when the switches are depressed and high when released.

All indicators are LEDs, powered by the +5 Vdc logic supply. If one (or more) of the LED indicators burns out, do not attempt to replace it; the entire switch box assembly must be replaced. Refer to Chapter 6 of this manual for detailed replacement procedures.

5.4 READ OPERATION

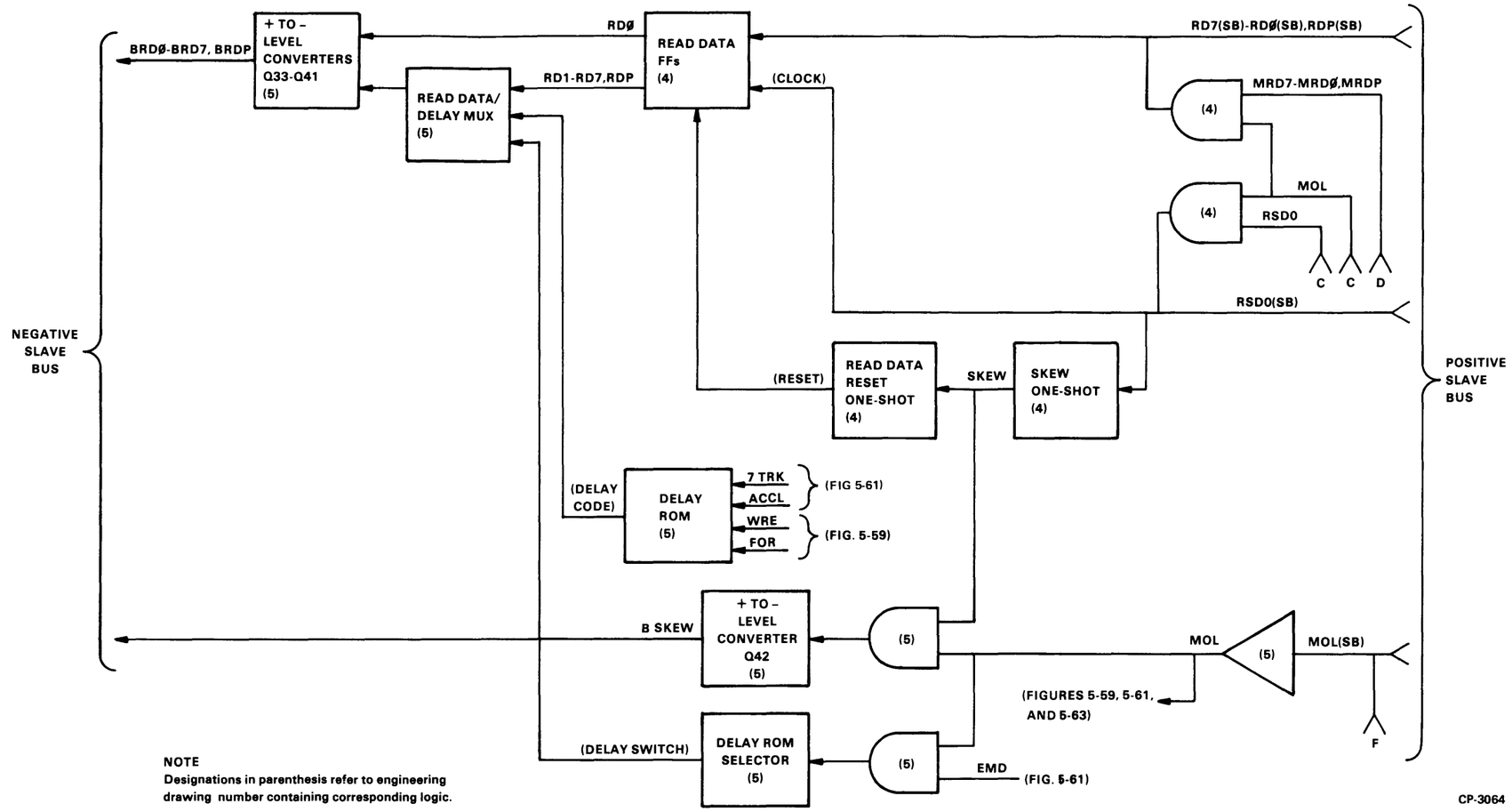
This section describes the read operation for both PE and NRZI reading. Flow diagrams complement the discussions.

5.4.1 PE Read (TE16 Only)

Figure 5-65 illustrates the major functional sequences of a PE read operation and the following paragraphs describe this operation in slightly greater depth. A detailed description of the PE read operation may be found in Paragraph 5.3.3, the detailed read amplifier (G066) module description.

5.4.1.1 Command Initiation – Once the controller is selected, it specifies the selected TE16, tape character format, and tape data density (1600 bits/in for PE).

The controller places the slave select (SS 0-2) and density (DEN 0-2) bits of the tape control register on the slave bus. The operational code of a read operation is decoded and the controller asserts FWD L or REV L on the slave bus. It then transmits SLAVE SET PULSE to the TE16 and initiates a motion delay.



NOTE
Designations in parenthesis refer to engineering drawing number containing corresponding logic.

Figure 5-64 Read Data Interface Block Diagram

Table 5-8 TE10N Motion Delay Periods

Drive Type	Start/Stop	Mode	Delay Period (ms)
9-Track	Start	Write	8.99
		Read	0.92
		Reverse	0.92
	Stop	Write	2.72
		Read	1.82
		Reverse	1.82
7-Track	Start	Write	15.26
		Read	0.92
		Reverse	0.92
	Stop	Write	2.72
		Read	1.82
		Reverse	6.30

5.4.1.2 Command Execution – The TE16, which is enabled by its address code on the slave select lines (SS 0-2) of the slave bus, responds to SLAVE SET PULSE by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion.

The TE16 read amplifiers are on continuously. Even as the tape accelerates, the controller PE read circuitry checks for a PE identification burst (IDB) and begins looking for a preamble. When the tape is at speed, the preamble will be detached and read; the tape characters immediately after the preamble all-1s character are data characters. These are deskewed in the controller, which then assembles the characters into data words and places them on the data bus to the processor. The controller continues this assembly of data characters into words until the first character of the postamble is detached.

5.4.1.3 Command Termination – The controller reads the postamble, which signifies the end of the record. When the postamble has been read, a motion delay sequence is initiated, at the end of which STOP L is asserted on the slave bus. STOP L resets the motion flip-flop in the TE16 and terminates tape motion.

5.4.2 NRZI Read (TE16, TE10W, TE10N)

Figure 5-66 illustrates the major functional sequences of an NRZI read operation and the following paragraphs describe this operation in slightly greater depth. A detailed description of the NRZI read operation may be found in Paragraph 5.3.3, the detailed read amplifier (G066) module description.

5.4.2.1 Command Initiation – Once the controller is selected, it specifies the selected TE16, tape character format, and tape data density. The controller places the slave select (SS 0-2) and density (DEN 0-2) bits of the tape control register on the slave bus. The operational function code of a read operation is decoded, and the controller asserts FWD L or REV L on the slave bus. It then transmits SLAVE SET PULSE to the TE16 and initiates a motion delay.

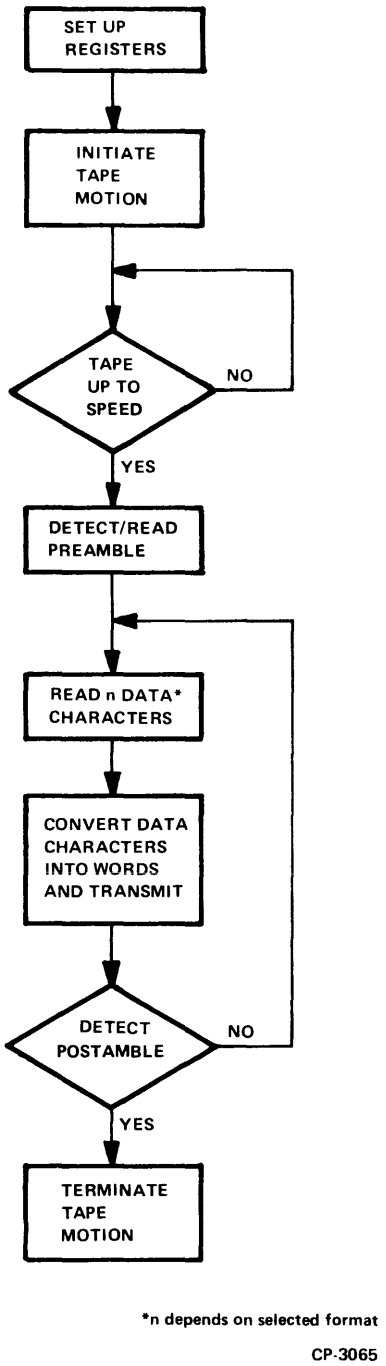


Figure 5-65 PE Read Operation Flowchart

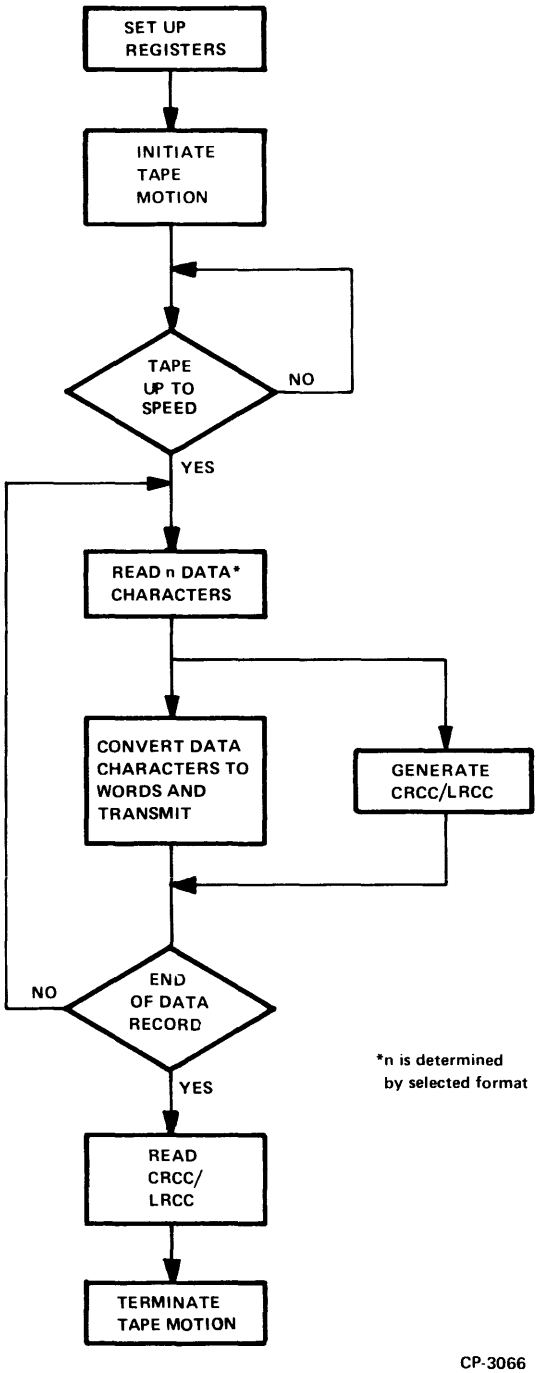


Figure 5-66 NRZI Read (Forward) Operation Flowchart

5.4.2.2 Command Execution – The TE16, which is enabled by its address code on the slave select lines (SS 0-2) of the slave bus, responds to SLAVE SET PULSE by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion. When the motion delay has timed out, the controller negates ACCL L on the slave bus. The signal enables the TE16 NRZI read circuitry.

When a tape character is detected by the TE16, RSDO (Read Strobe Delay Over) is transmitted via the slave bus to the controller and the tape character is multiplexed onto the slave bus read data lines. The controller assembles the characters into words and places them on the data bus to the processor. The controller continues this assembly of data characters into words, until the end of the data records.

During a forward read, the rest of the read circuitry continues its operation, reading the CRCC and then reading the LRCC. Discrepancies between generated CRCC/LRCC and detected CRCC/LRCC cause their respective error bits to set.

During a reverse read, the LRCC character is encountered first at the start of the read operation, followed by the CRCC. No CRC or LRC is generated. Then the data is read; assembly of characters into data words may differ when reading in the reverse direction, but this depends on the data format selected.

5.4.2.3 Command Termination – When the data and LRCC/CRCC have been read, the read heads will encounter the IRG. This absence of tape characters causes a motion delay, at the end of which STOP L is asserted on the slave bus. STOP L resets the motion flip-flop in the TE16 and terminates tape motion.

5.5 WRITE OPERATION

This section describes the write operation for both PE and NRZI writing. Flow diagrams complement the discussions.

5.5.1 PE Write (TE16 Only)

Figure 5-67 illustrates the major functional sequences of a PE write operation and the following paragraphs describe this operation in slightly greater depth. A detailed description of the PE write operation may be found in Paragraph 5.3.6, the detailed logic and write (M8916) module description.

5.5.1.1 Command Initiation – Once the controller is selected, it specifies the selected TE16, tape character format, and tape data density (1600 bits/in for PE). The controller places the slave select (SS 0-2) and density (DEN 0-2) bits of the tape control register on the slave bus. Then, the two's complement of the number of tape characters to be written is loaded into the controller frame count register. The controller decodes the write command function code and asserts FWD L and WRITE L on the slave bus. SLAVE SET PULSE is asserted on the slave bus, and the controller accepts the first data word to be written.

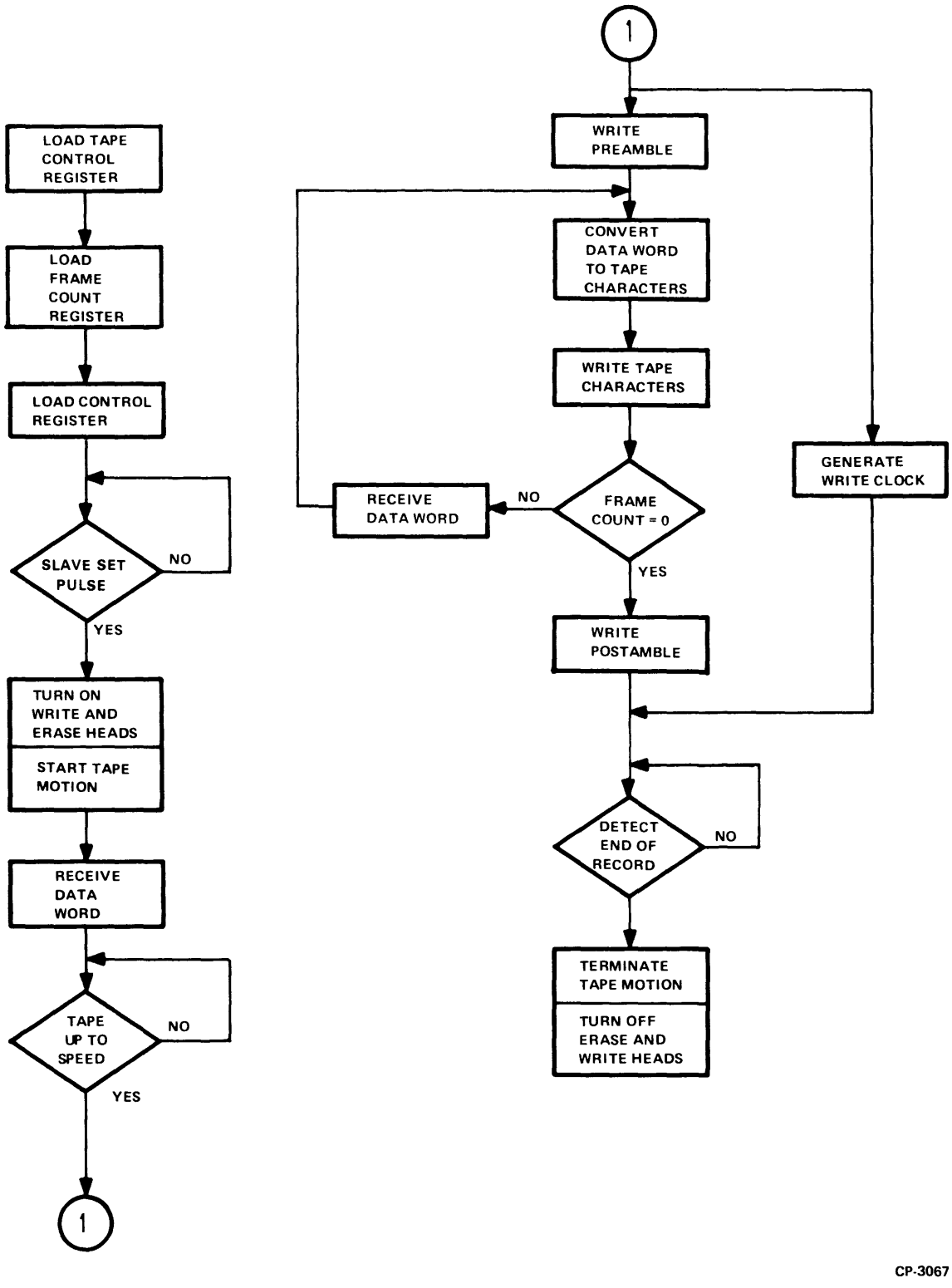


Figure 5-67 PE Data Write Operation Flowchart

5.5.1.2 Command Execution – The TE16, which is enabled by its address code on the slave select (SS 0-2) lines of the slave bus, responds to SLAVE SET PULSE by setting its forward motion and write enable flip-flops. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

After a motion delay during which the TE16 erases tape while coming up to speed, the controller negates ACCL L on the slave bus. This signifies that the TE16 is at speed and enables it to transmit WRT CLK to the controller. Upon receipt of WRT CLK, the controller begins generating a preamble. When this is written, the controller begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word and continues to do so until all the data words have been transferred. Each time the controller generates a character, the frame count register is incremented, a vertical parity bit is generated, and the tape character is converted to PE mode and transmitted to the TE16 write circuitry. When the frame count register overflows, the controller generates a postamble, which is written on a tape. During the entire operation, the TE16/controller read operation is active and reads the record being written.

5.5.1.3 Command Termination – When the TE16/controller read circuitry detects the end of the record, a motion delay is generated, at the end of which, the controller asserts STOP L on the slave bus, resetting the TE16 forward motion flip-flop, thereby terminating tape motion.

5.5.2 NRZI Write (TE16, TE10W, TE10N)

Figure 5-68 illustrates the major functional sequences of an NRZI write operation and the following paragraphs describe this operation in slightly greater depth. A detailed description of the NRZI write operation may be found in Paragraph 5.3.6, the detailed logic and write (M8916) module description.

5.5.2.1 Command Initiation – Once the controller is selected, it specifies the selected TE16, tape character format, and tape data density. The controller places the slave select (SS 0-2) and density (DEN 0-2) bits of the tape control register on the slave bus. Then, the two's complement of the number of tape characters to be written is loaded into the controller frame count register. The controller decodes the write command function code and asserts FWD L and WRITE L on the slave bus. SLAVE SET PULSE is asserted on the slave bus, and the controller accepts the first data word to be written.

5.5.2.2 Command Execution – The TE16, which is enabled by its address code on the slave select lines (SS 0-2) of the slave bus, responds to SLAVE SET PULSE by setting its forward motion control and write enable flip-flops. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

After a motion delay during which the TE16 erases tape while coming up to speed, the controller negates ACCL L on the slave bus. This notifies the TE16 that it is at speed and enables it to transmit WRT CLK to the controller.

Upon receipt of WRT CLK by the controller, it begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word and continues to do so until all the data words have been transferred. Each time the controller generates a character, the frame count register is incremented. A vertical parity bit is generated, the CRCC is generated and the tape character is transmitted to the TE16 write circuitry, where it is converted from binary to NRZI mode (1s become transitions) and written on the tape. When the frame count register overflows to zero, the controller generates the timing to write the generated CRCC and the LRCC.

During the time that the tape is moving at speed (ACCL L negated), the TE16/controller performs a read-after-write operation.

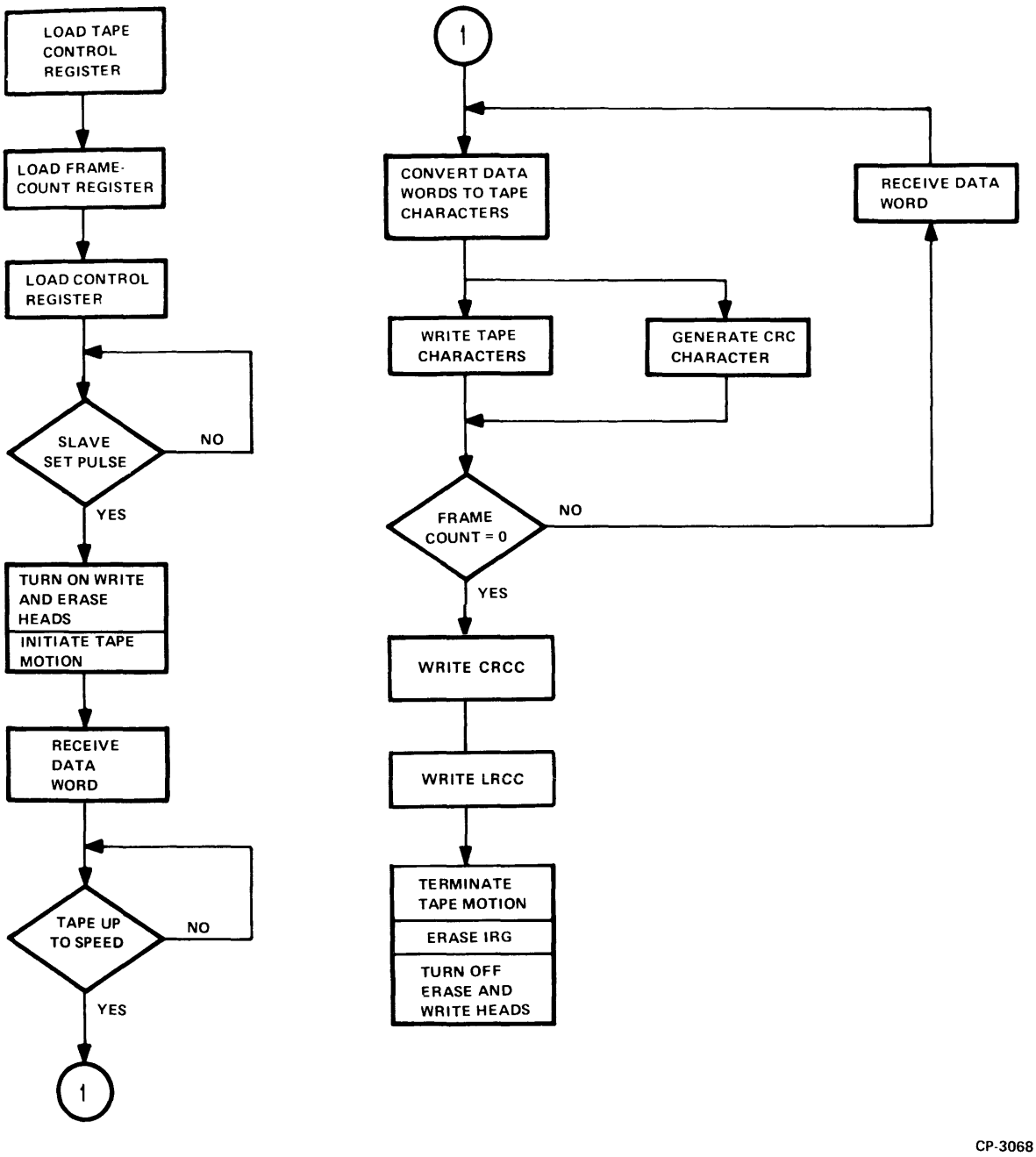


Figure 5-68 NRZI Data Write Operation Flowchart

5.5.2.3 Command Termination - When the TE16/controller read circuitry detects the end of the record, a motion delay is generated, at the end of which the controller asserts STOP L on the slave bus, resetting the TE16 forward motion flip-flop, thereby terminating tape motion. When tape motion ceases, the write enable flip-flop is cleared and the write and erase heads are de-energized.

CHAPTER 6
SERVICING

6.1 SCOPE

This chapter provides complete TE16 (TE10W/N) preventive and corrective maintenance procedures. No tape controller maintenance information is provided. For that information, refer to the specific controller maintenance manual.

The major TE16 assemblies referenced throughout this chapter are shown in Figure 6-1. Access the interior TE16 components by rotating the service lock (located on the lower right corner of the transport front) to release the transport assembly from the cabinet (Figure 6-2).

6.2 MAINTENANCE PHILOSOPHY

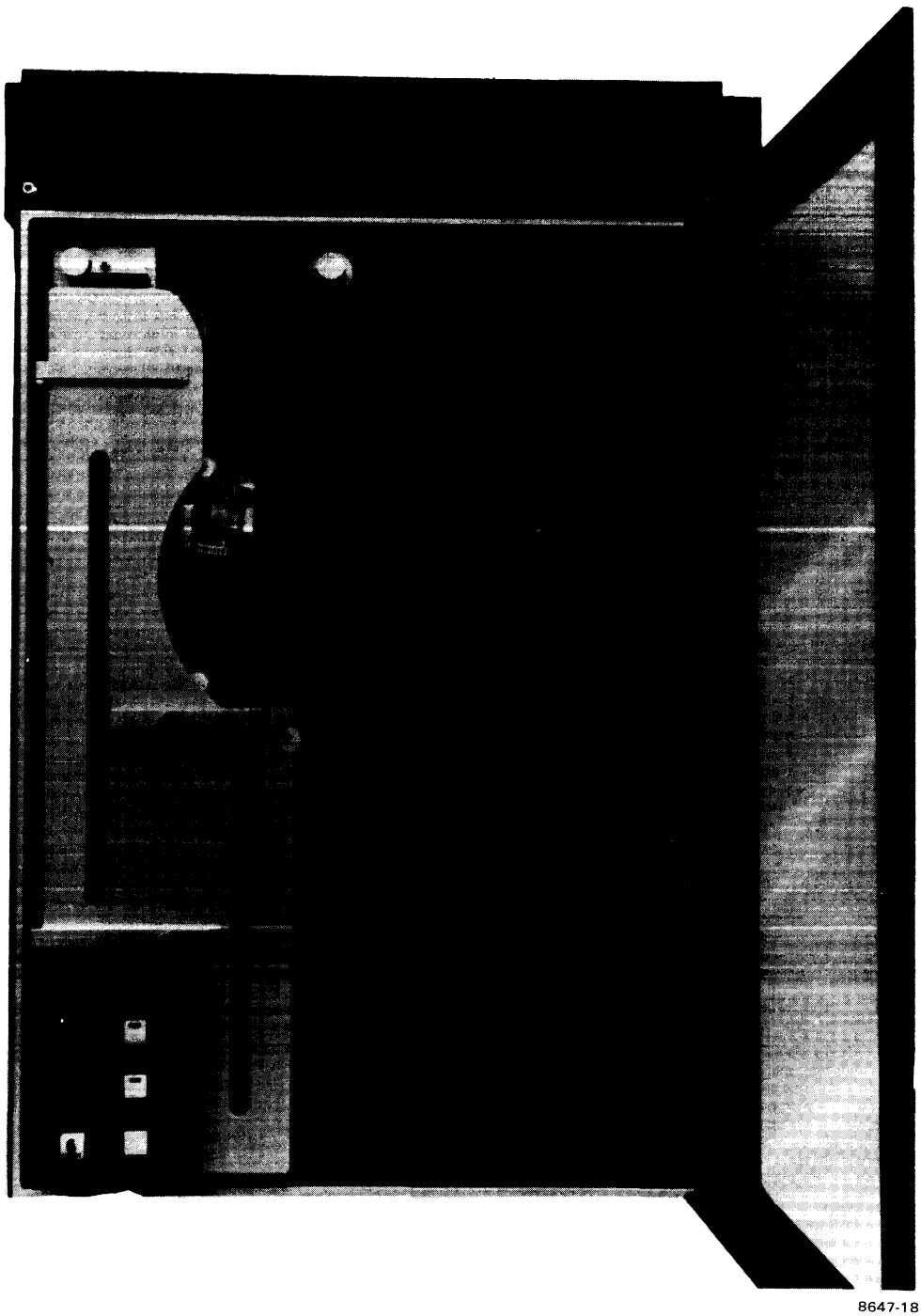
The TE16 DECmagtape Transport is a highly reliable tape transport that will provide years of trouble-free performance when it is properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

Preventive maintenance (PM) includes daily head and tape path cleaning and additional monthly, quarterly, and semiannual procedures. The transport requires few adjustments, and the procedures should not be performed unless problems are encountered in transport operation. Refer to Paragraph 6.4 for the recommended preventive maintenance procedures.

Corrective maintenance (CM) consists of troubleshooting at the system level, using system diagnostics, visual methods, and the Test Function Generator (TFG). Once a fault is thought to be in the transport, functional block diagrams and engineering logic diagrams are used to localize the failure to an electrical area (module) or a mechanical part. Then, when the faulty module or mechanical part is located, it should be replaced.

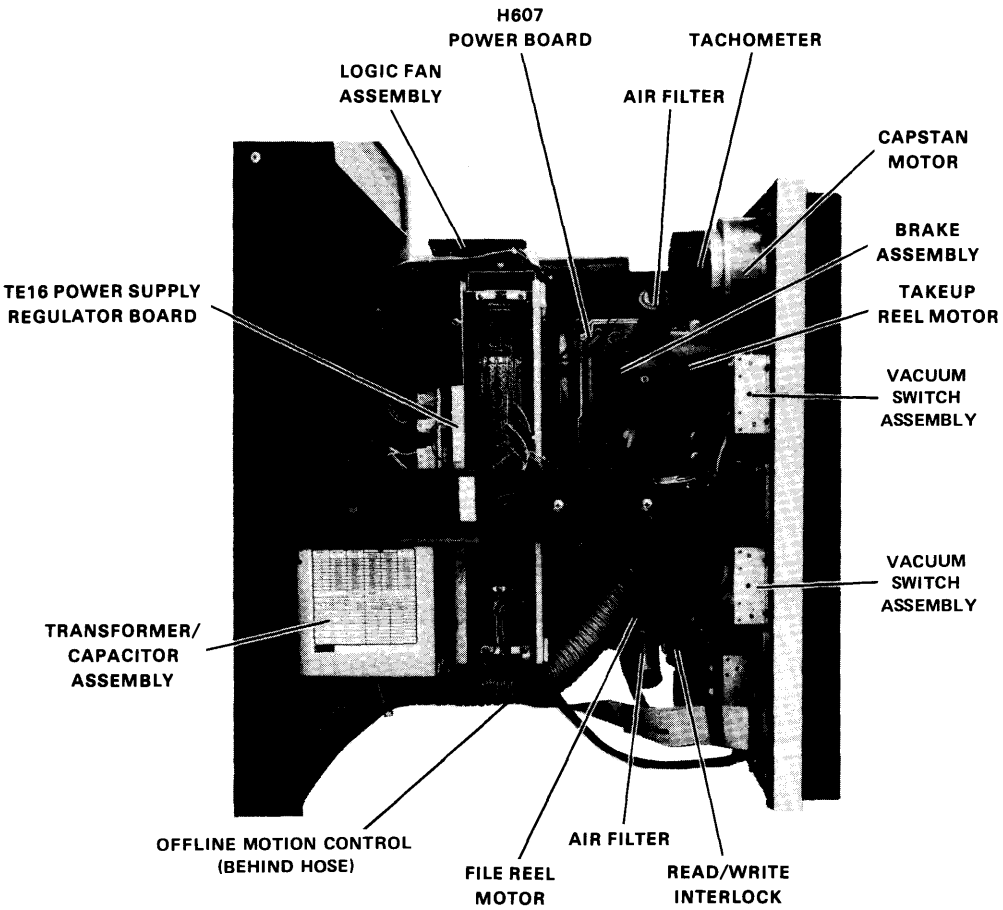
6.3 TEST EQUIPMENT

Table 6-1 lists tools that are required to maintain the TE16 (TE10W/N) DECmagtape Transport. Refer to Paragraph 6.3.1 for a list of required diagnostic programs.



A. Front View

Figure 6-1 TE16 DECmagtape Transport Assemblies (Sheet 1 of 2)



NOTE:
THE CAPSTAN MOTOR AND TACHOMETER FORM AN INTEGRAL UNIT. DO NOT DISASSEMBLE THE UNIT.

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B. Left Side View

Figure 6-1 TE16 DECmagtape Transport Assemblies (Sheet 2 of 2)

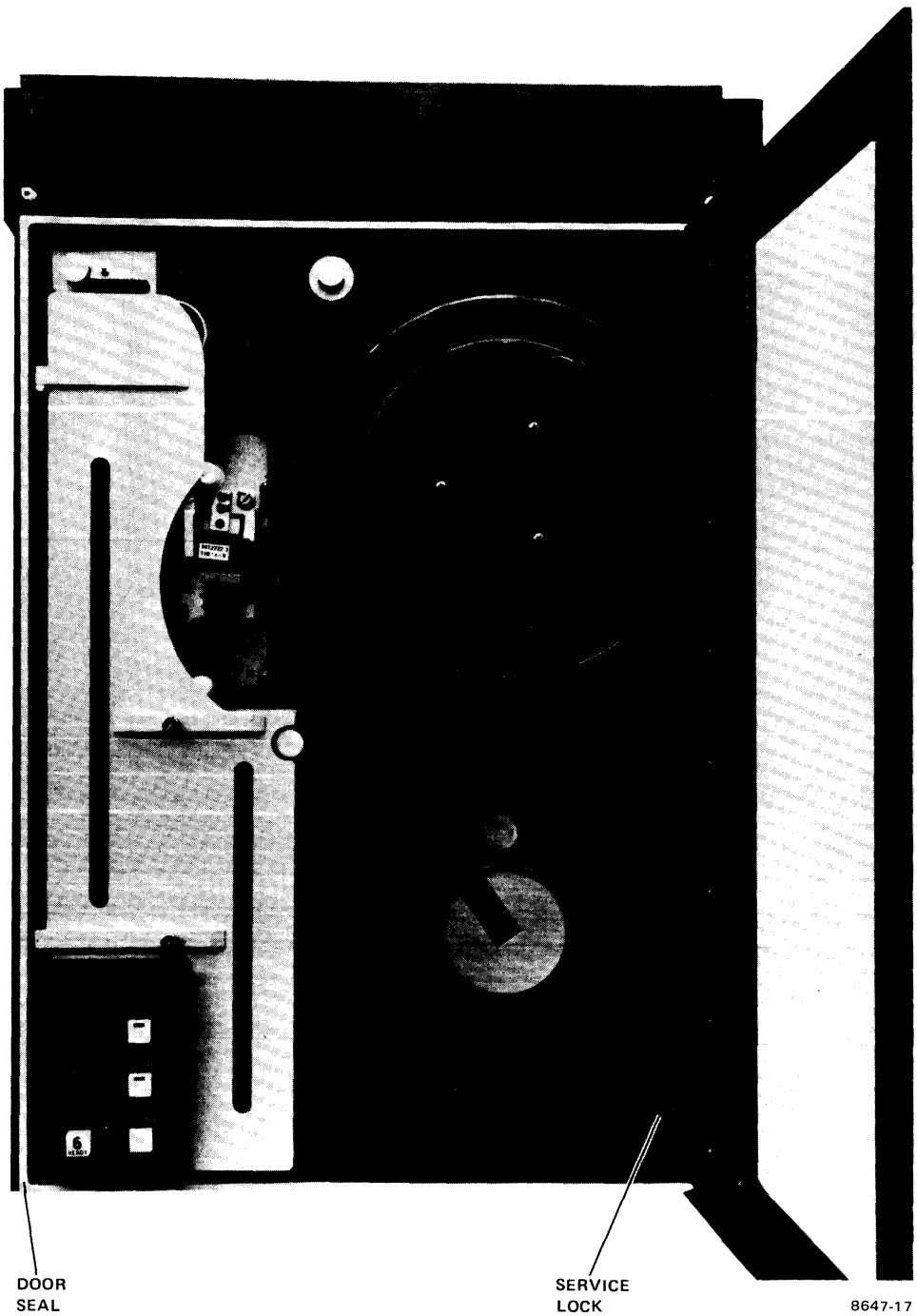

Figure 6-2 Front View, Transport Casting

Table 6-1 Test Equipment

Item	Part No.	Description	Usage*							
			1	2	3	4	5	6	7	8
1		Oscilloscope with probes	X		X	X		X		
2	29-18303	Digital tool kit	X		X	X	X	X	X	X
3	29-19224	Skew tape	X		X			X		
4	29-16871	Magna-See™				X		X		
5	29-20273	Microscope				X		X		
6	29-10780	Penlight		X		X		X		
7	29-22265	Vacuum system belt tension gauge			X					X
8	74-16187	Vacuum system pulley height gauge							X	
9	90-09299	Silicone grease			X					
10	90-08268	Heat sink compound	X							
11	90-09177	EOT/BOT markers				X		X		
12	Local Purchase	Metal straight edge (scale)						X		
13	48-50023-01	Shim stock .001 (purple)						X		
14	48-50023-03	Shim stock .002 (red)						X		
15	48-50023-04	Shim stock .003 (green)						X		
16	48-50023-05	Shim stock .004 (tan)						X		
17	48-50023-06	Shim stock .005 (blue)						X		
18	48-50023-07	Shim stock .0075 (clear)						X		
19	48-50023-08	Shim stock .010 (brown)						X		
20	29-13515	Feeler gauge set					X			
21	74-13969	Alignment doors						X		
22	29-22039	Depth micrometer						X		
23	94-05144	Hub spanner wrench and adapter spacer						X		
24	94-05143	Block gauge (hub height)					X	X		
25	Local Purchase	1-3/8 in socket (3/4-in drive) (see Note)						X		
26	Local Purchase	3/4-in drive breaker bar (see Note)						X		
27		Snap lock hub shim stock						X		
28	W984	Double height extender	X		X	X				
29	Local Purchase	Teflon tape					X			

Note:
1-3/8 in socket: Sears 9 GT 47549
3/4-in breaker bar: Sears 9 GT 4443

*Usage Legend

1. Routine corrective maintenance
2. Monthly PM
3. Quarterly PM
4. Semiannual PM
5. Annual PM
6. Major tape path alignment
7. 50–60 Hz conversion
8. Vacuum system belt change

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6.3.1 Diagnostics

This section lists the various PDP-11 diagnostic programs that are used in maintaining the TE16 (TE10N/W) Transport. The group of programs that is listed for the customer configuration is considered to be required standard test equipment (see Table 6-1). Each diagnostic designation (e.g., DZTUA) is prefixed by "MAINDEC-11."

1. Diagnostic programs used with a TM02/TU16 configuration:

    a. DZTUA Multidrive Data Reliability
    b. DZTUB Basic Function Test
    c. DZTUC Control Logic Test
    d. DZTUE Utility Driver (BRUTIS)
    e. DZTUF Data Tape Create
    f. DZTUG Drive Function Timer

2. Diagnostic programs used with a TM03/TE16 configuration:

    a. DZTEA Multidrive Data Reliability
    b. DZTEB Basic Function Test
    c. DZTEC Control Logic Test 1
    d. DZTED Control Logic Test 2
    e. DZTEE Drive Function Timer
    f. DZTEF Utility Driver (BRUTIS)
    g. DZTUF Data Tape Create

3. Diagnostic programs used with the TMB11/TE10W/TE10N configuration:

    a. DZTMA Instruction Test
    b. DZTME Drive Function Timer
    c. DZTMF Supplemental Instruction Test
    d. DZTMG Utility Driver
    e. DZTMH Data Reliability

4. Diagnostic programs used with TM8E/TE10W/TE10N configuration:

    a. DHTMA Control Test 1
    b. DHTMB Control Test 2
    c. DHTMC Drive Function Timer
    d. DHTMD Data Reliability (9-track)
    e. DHTME Data Reliability (7-track)
    f. DHTMF Random Exerciser

5. Diagnostic programs used with TC59/TE10W configuration:

    a. D4A Instruction Test
    b. D4C Drive Function Timer
    c. D4D Data Reliability (7-track)
    d. D4E Data Reliability (9-track)
    e. D4G Random Exerciser

6.4 PREVENTIVE MAINTENANCE

TE16 preventive maintenance to be performed by the Field Service technician is presented in this section. Care and preventive maintenance of the TE16 to be performed by the user are listed in Chapter 4.

6.4.1 Preventive Maintenance Schedule

The recommended frequency for performing the preventive maintenance (PM) procedures in this section are based on moderate use of the equipment. In cases where use is heavy, certain steps should be performed more frequently. For example, items 5 through 11 of the quarterly procedure (Paragraphs 6.4.3.5 through 6.4.3.11) assume that tape motion does not exceed 150 hours per quarter; if tape motion exceeds that figure, those procedures should be performed more often.

The semiannual procedure (Paragraph 6.4.4) assumes that tape motion does not exceed 300 hours during a six-month period; if tape motion exceeds that figure, the procedure should be performed more frequently.

6.4.2 Monthly PM Procedures

The items listed in this section are to be performed on a monthly basis.

6.4.2.1 Tape Path Cleaning and Inspection – Clean the tape path and inspect it for wear as follows:

1. Turn power off at the 861 Power Controller by moving the circuit breaker handle down. Remove the supply reel (if one is installed). Using water-dampened wipes, clean the front door glass and frame.

> **CAUTION**
> **Be careful not to saturate the lining on the vacuum column walls with fluid; this could cause damage to the lining.**

2. Remove the head cover and open the vacuum column door. Using a penlight, inspect the read/write head and erase head for oxide accumulation. A worn head will normally show oxide accumulation on the worn spot. If the read/write head is unevenly worn or if the erase head shows any wear, replace the head plate assembly (refer to Figure 6-3); shiny spots indicate uneven wear. Procedures for replacing the head plate assembly can be located in Paragraph 6.6.7.

> **NOTE**
> **Wear spots of any kind on the erase head indicate head plate replacement is mandatory.**

3. Using DECmagtape cleaning fluid and foam or cotton-tipped wooden swabs, clean any accumulated oxide from the read/write head, erase head, and tape cleaner. Clean the tape bearing surfaces of the fixed guides near the head assembly. (Pay particular attention to removing oxide buildup from the ceramic washers on the fixed guides.)

> **NOTE**
> **Ensure that the inner (spring loaded) washers move freely after cleaning and that they are not jammed under the fixed guides.**

4. Using DECmagtape cleaning fluid and swab, clean the tape bearing surface of the three roller guides (upper left, upper middle, and lower middle).

CAUTION

Do not allow fluid to penetrate the shaft area of the roller guide, as this will degrease the bearings.

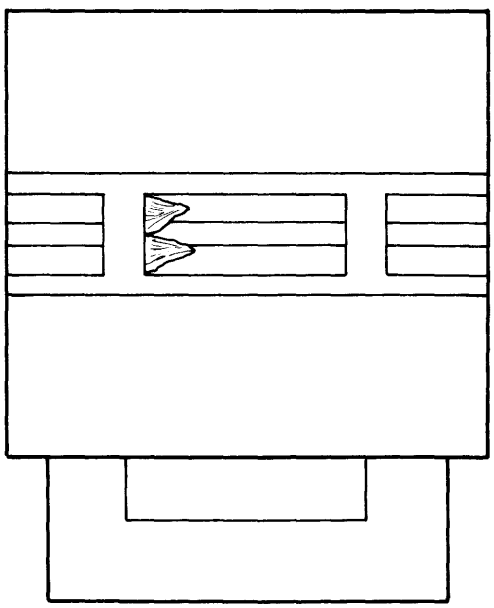
5. With DECmagtape cleaning fluid and wipes, clean the vacuum columns and column door glass.

6. With DECmagtape cleaning fluid and a lint free cloth, gently clean the rubber surface of the capstan wheel.

7. Finally, using a dry wipe, clean the reel contacting metal surface of the lower snap-lock hub, paying particular attention to the rear flange. Dirt on these surfaces may result in slippage of the tape reel.

NOTE

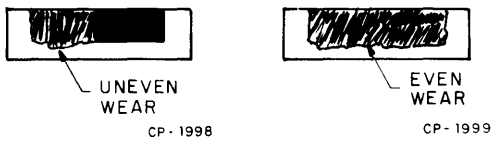
If a quarterly PM is to be performed at this time, proceed to Paragraph 6.4.3. If not, continue with Paragraph 6.4.2.2.



CP-3189

A. Unacceptable Read/Write Head Assembly Wear

Figure 6-3 Oxide Accumulation (Sheet 1 of 2)



B. Unacceptable Erase Head Assembly Wear

Figure 6-3 Oxide Accumulation (Sheet 2 of 2)

6.4.2.2 NRZI Diagnostic (on all DECmagtape systems) – Turn power on; mount tape and load it to BOT. Run the On-Line Reliability Diagnostic applicable to the computer system for 10 minutes in 800 bits/NRZI in mode. If any soft read errors occur, it will be necessary to run a complete pass to determine whether the frequency of soft read errors is within specification or not. No hard read errors are allowed.

NOTE
Acceptable soft read error rate for one 2400-ft reel of tape is:

Forward Read	**1**
Reverse Read	**1**
Write	**2**

Retries on the same spot do not increase the soft read error tally (i.e., a read error on Block 1, Record 1, that required three retries to recover is recorded as one soft read error).

6.4.2.3 Phase Encoding Diagnostic (TE16 Systems only) – Rewind tape to BOT and run the relevant On-Line Reliability Diagnostic for 10 minutes in 1600 bits/in PE mode. If any soft read errors occur, it will be necessary to run a complete pass to determine whether the frequency of soft read errors is within specification or not. No hard read errors are allowed.

NOTE
Acceptable soft read error rate for one 2400-ft of tape is:

Forward Read	**1**
Reverse Read	**2**
Write	**2**

Retries on the same spot do not increase the soft error tally (i.e., a read error on Block 1, Record 1, that required three retries to recover is recorded as one soft read error).

6.4.3 Quarterly PM Procedures

The items listed in this section are to be performed on a quarterly basis.

6.4.3.1 Operator Panel Check - Check the operator panel switches and indicators as follows:

1. Apply power to the TE16 by placing the circuit breaker on the 861 Power Controller up. The POWER and WRL indicators will glow.

2. Place a scratch tape (with write ring) on the lower hub and secure it with the latch lever. Thread the tape through the tape path, and take three wraps around the take-up reel.

3. Depress and release the LOAD pushbutton. The tape will load into the vacuum columns and run forward for approximately 5 seconds and then rewind to BOT. The BOT, ON/OFF LINE, and LOAD indicators will glow. The WRL indicator should not glow with the write ring installed. The SEL indicator will glow if the TM02/03 is currently selecting that TE16.

4. The LOAD, RWD/UNLD pushbutton should not have any effect with the ON/OFF LINE indicator on.

5. Depress and release the ON/OFF LINE pushbutton, which will extinguish the ON/OFF LINE and SEL (if previously lit) indicators.

6. Depress the REW/UNLD pushbutton. If tape is positioned after BOT, the tape will rewind to BOT and stop, and the BOT indicator will glow. If the tape was positioned at BOT, an unload operation is executed. The vacuum system will be shut off, and tape will be taken out of the columns and wound onto the supply reel. The LOAD indicator will extinguish.

7. Dismount the tape, and remove the write enable ring. Mount the tape and load it to BOT. Ensure that the WRL indicator stays lit.

NOTE

If any discrepancies are found and the problem is diagnosed to the operator panel, the entire panel/cable assembly, as a unit, must be replaced. The individual switches and LEDs are not field replaceable.

8. Off-Line motion control switches are provided under the TE16 logic chassis (Figure 6-1B). The FWD/REV switch controls, but does not initiate, tape motion. The START/STOP switch initiates tape motion when it is moved from STOP to the START position and halts tape motion when moved from the START to the STOP position. Check these switches for proper functioning.

6.4.3.2 Supply Reel Hub Inspection and Lubrication - Perform the following to inspect and lubricate the supply reel hub. Refer to Figure 6-4 for a cross-sectional view of the reel hub.

1. Disassemble the hub as follows:

   a. Release the snap-lock lever.

   b. Note the position of the index screw by placing a pencil mark opposite the screw on the surface of the inner hub.

   c. Remove the index screw.

   d. Remove the outer hub by rotating it and the lock lever counter clockwise.

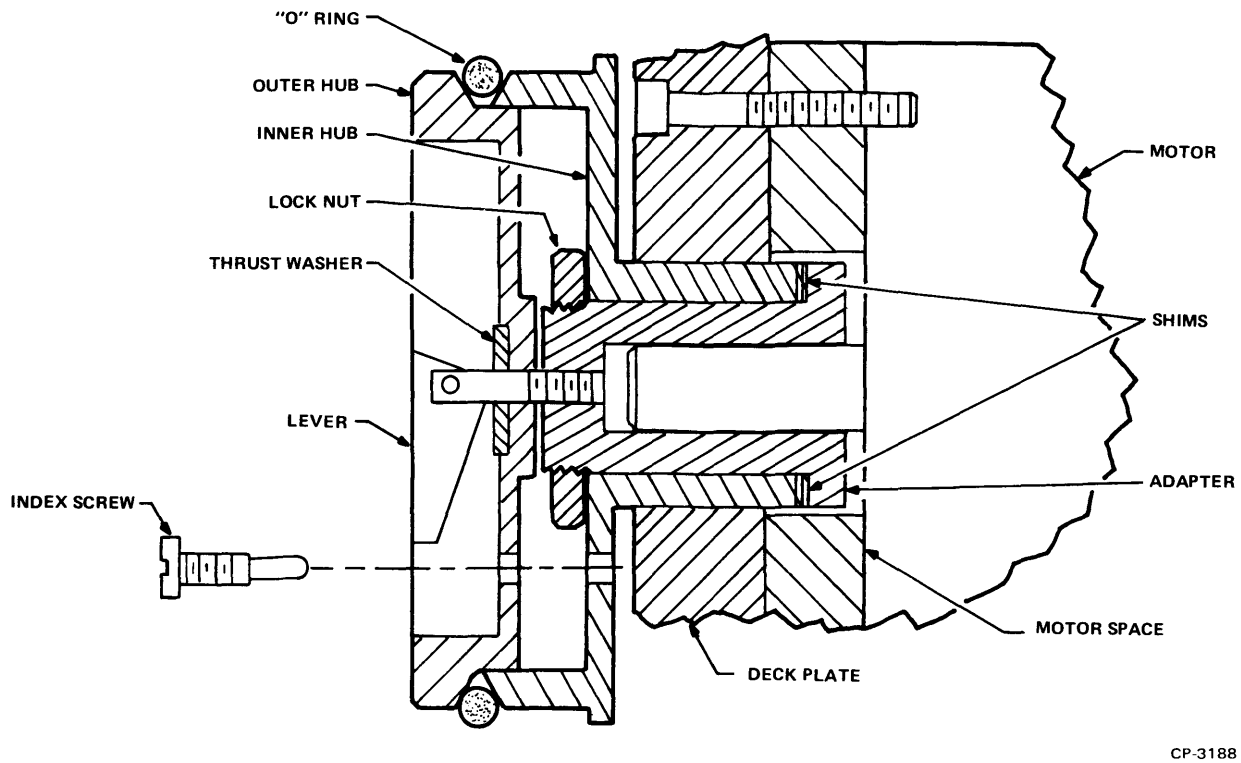


Figure 6-4 Cross-Sectional View of Snap-Lock Hub

2. Examine the "O" ring for any gouges or cracks. If any wear is noted, replace the "O" ring, thrust washer, and lock lever. (All three items are contained in a kit envelope.)

3. Lubricate the assembly as follows:

   a. Lightly lubricate the "O" ring chamfer on the outer and inner hubs with silicone grease. (Do not use heat sink compound.)

   b. Place the "O" ring onto the outer hub, being careful not to contaminate the outer surface of the ring with grease. Wipe the outer surface of the hub and "O" ring to remove all excess lubricant.

   c. Lightly lubricate the thrust washer before sliding it over the snap lock lever shaft.

4. Reassemble the hub as follows:

   a. Rotate the outer hub clockwise, such that the shaft of the latch lever will thread its way into the adapter.

   b. Hold the inner hub while rotating the outer hub clockwise, until it bottoms. Continue to hold the inner hub and rotate the outer hub counter clockwise until the lock lever closes smoothly.

   c. Locate the original hole, and replace the index screw.

d. Wipe away any excess grease that may have found its way to the surface of the hub assembly.

e. Mount a tape and ensure that the lock lever closes smoothly, while checking to see that the reel is held securely. If either parameter is not met, remove the index screw and rotate the outer hub to fine-tune it. Replace the index screw when a proper alignment has been made.

6.4.3.3 Vacuum System Belt Inspection – Follow these procedures to inspect the vacuum belt system:

1. Remove the guard plate with four quarter-turn fasteners.

2. Visually inspect the drive belt for any signs of wear or cracks. If necessary, replace the belt.

3. To check belt tension, position the gauge as shown in Figure 6-5. Push against the knob until the third tab on the gauge just touches the belt. Read the tension from the scale just under the spring. The belt is properly adjusted if the gauge reads 4.1 ± 1.8 kg (9 ± 4 lb). Refer to section 6.5.11, for adjustment procedures, if adjustment is necessary.

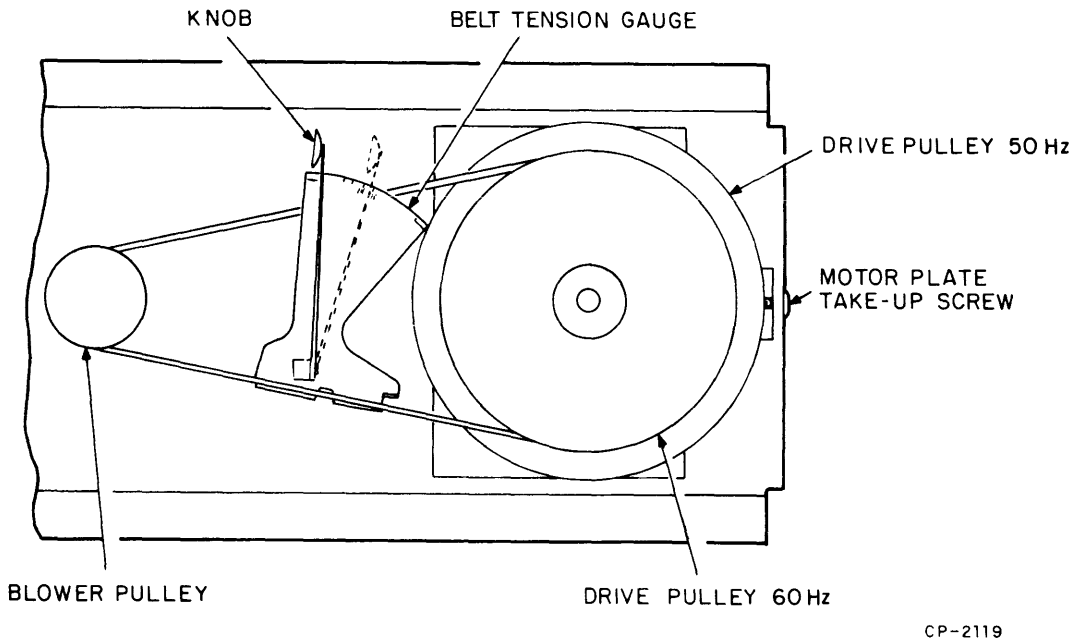


Figure 6-5 Belt Tension Gauge

6.4.3.4 Voltage Checks – Follow these procedures to check voltages:

1. Turn power off at the 861 Power Controller. Remove the M8912 (TFG) from slot EF03, and place it on a module extender in slot AB03.

2. Place the SS RD, SS WRT, and WRT switches (on the TFG) down; turn power on.

NOTES

For a description of the TFG module, refer to Paragraph 5.3.5.

For all voltage checks, refer to Figure 6-6 for the location of the potentiometers that control adjustments. If any voltages cannot be adjusted to meet specifications, replace the regulator board.

a. Check the +5 Vdc drive logic voltage:

Reference Point = D01A2 (red wire)
Nominal Value = +5.25 ± 0.05 Vdc

If necessary, adjust potentiometer R59.

b. Check the +12 Vdc Check (Drive Voltage):

Reference Point = A04V1 (yellow wire)
Nominal Value = 12.05 ± 0.05 Vdc

If necessary, adjust potentiometer R37.

c. Check the -6.4 Vdc drive voltage:

Reference Point = C04N2 (green wire)
Nominal Value = -6.35 ± 0.05 Vdc

If necessary, adjust potentiometer R44.

d. With S5-9 (M8912) ON, check the +12 Vdc (NRZI) drive voltage:

Reference Point = C02J2 (orange wire)
Nominal Value = 11.875 ± 0.125 Vdc

If necessary, adjust potentiometer R26.

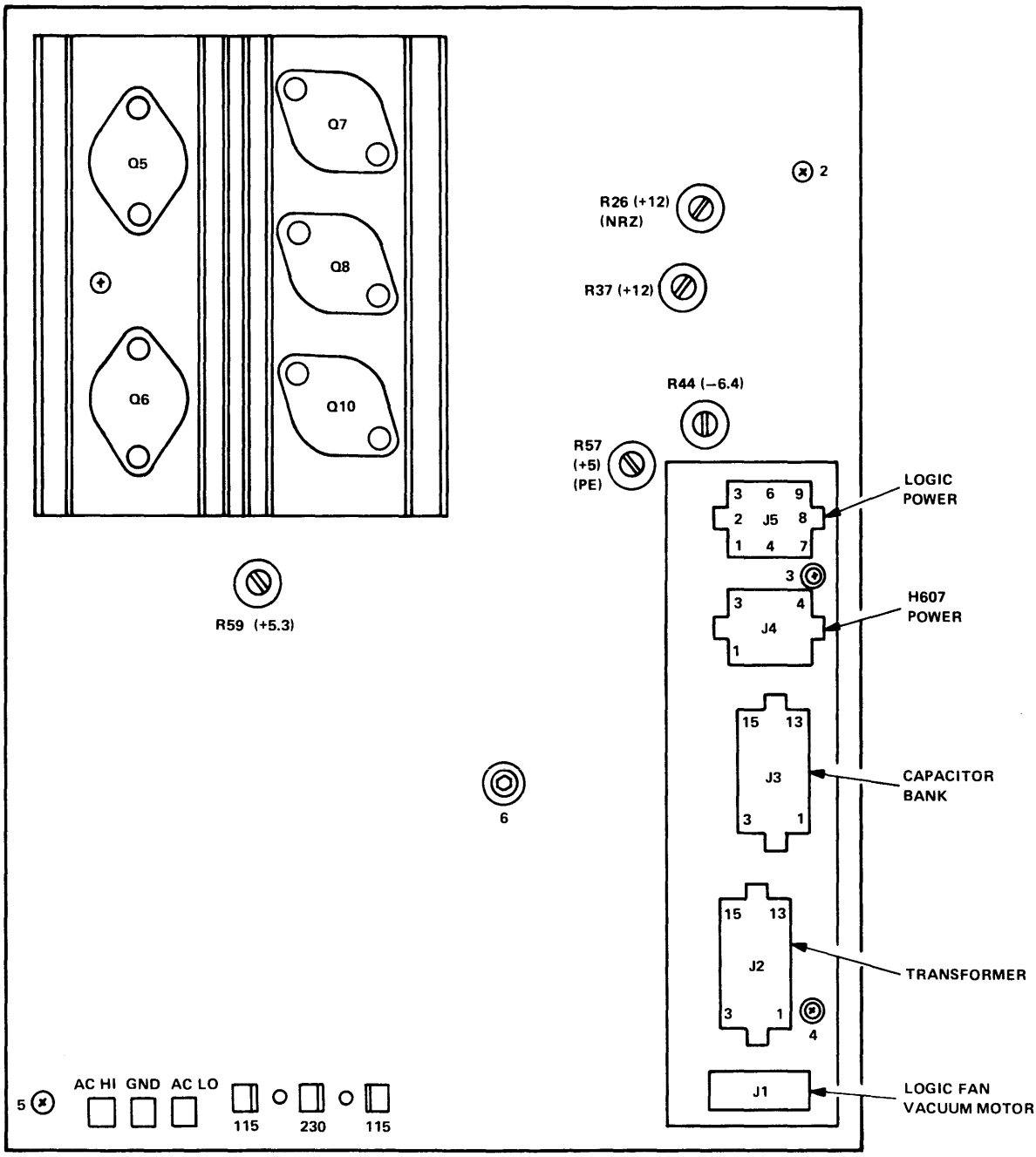
NOTE

Steps d and e are interactive and must be performed in that sequence. Disregard step e for TE10N and TE10W models.

e. With S5-9 (M8912) OFF, check the +5 Vdc (PE) drive voltage:

Reference point = C02J2 (orange wire)
Nominal Value = +5.6 ± 0.1 Vdc

If necessary, adjust potentiometer R57.



NOTES:

1) 1 - 5 represent 5 Phillips head screws.
2) 6 represent Allen screw - must be secured very tightly, or damage to the power supply may result.

CP-3196

Figure 6-6 TE16 Power Supply Regulator Board

6.4.3.5 Forward Tape Speed and dc Balance Check - Check dc balance as follows:

1. Turn power off at the 861 Power Controller. Disconnect the erase/write head cable from the M8916 LAW module, and loosen the two screws in the upper and lower right hand corners of the H607 daughter board. Swing the board away from the H607 mother board.

2. Turn power on; load a master skew alignment tape, and position the tape at BOT.

3. Set the oscilloscope's vertical gain to 50 mV/cm, and reference mother board TP 13 (Figure 6-7 and Table 6-2).

4. Approximately 50 mV of ac ripple will be seen on the oscilloscope screen. This ripple should be centered around 0 Vdc. If necessary, adjust R117 on the mother board in order to obtain 0.0 V ± 0.04 Vdc.

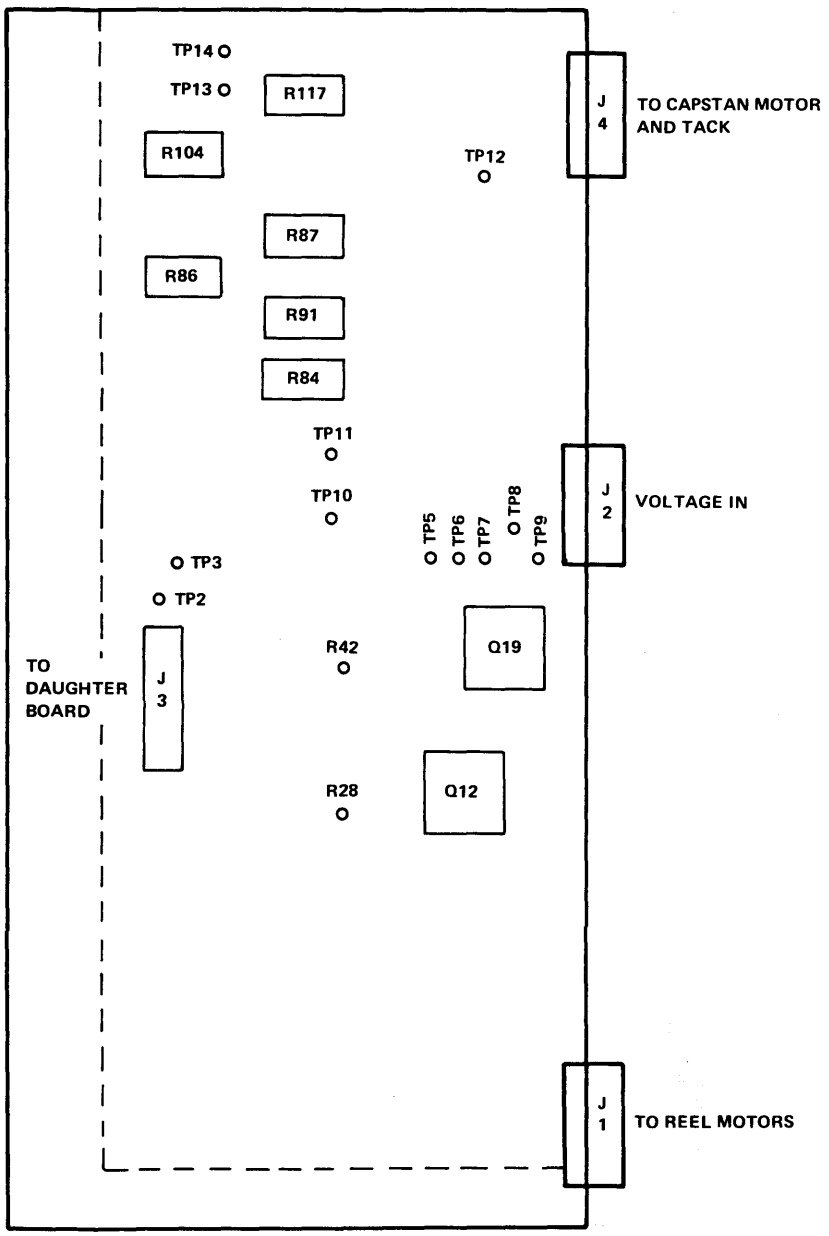


Figure 6-7 H607 Mother Board: Adjustments and Test Points

Table 6-2 H607 Mother Board Test Points

Test Point No.	Signal
1	Not Used
2	LOWER BRAKE OUT
3	UPPER BRAKE OUT
4	Not Used
5	REWIND CAP H
6	REV/REW H
7	FOR H
8	+8 V
9	-8 V
10	UPPER BRAKE OUT H
11	LOWER BRAKE OUT H
12	GROUND
13	SERVO SIGNAL
14	CAPSTAN BALANCE

5. Check forward tape speed as follows:

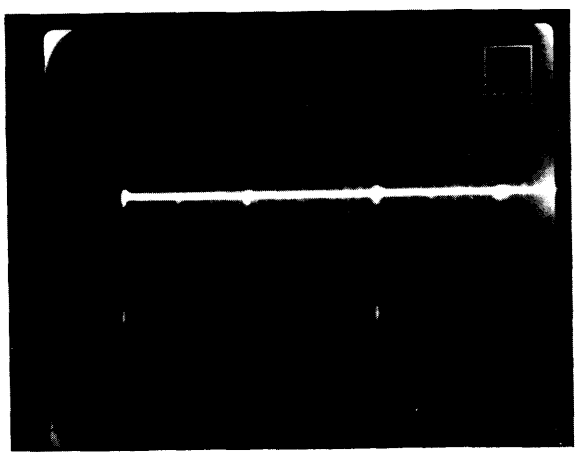
   a. Set the oscilloscope as follows:

      Horizontal: 10 μs/cm
      Vertical: 2 V/cm (channel 1)
      Triggering: Normal
      Negative slope
      Channel 1 triggered

      Place the Channel 1 probe to pin B04L1 (track 5)

      NOTE
      The probe is placed on pin A04H1 (Track 8) for 7-channel TE10 transports.

   b. Initiate forward tape motion with the maintenance switches. Check that the negative pulses are 55-57 μs apart (refer to Figure 6-8). If the pulses are not 55-57 μs apart, adjust potentiometer R91 to the mother board to obtain a 56 μs reading.



M-0610

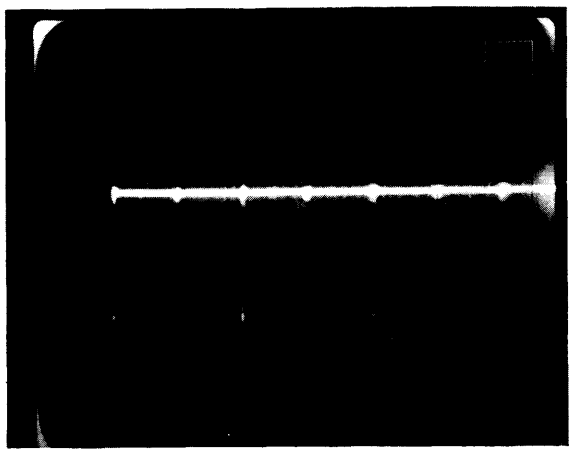
Figure 6-8 Tape Speed Check: 10 μs Sweep Speed

6.4.3.6 Reverse Tape Speed – Initiate reverse tape motion with the maintenance switches. Check that the negative pulses are 55-57 μs apart. If the pulses are not 55-57 μs apart, adjust potentiometer R87 on the mother board to obtain a reading of 56 μs.

6.4.3.7 Forward Jitter Check – Check forward jitter as follows:

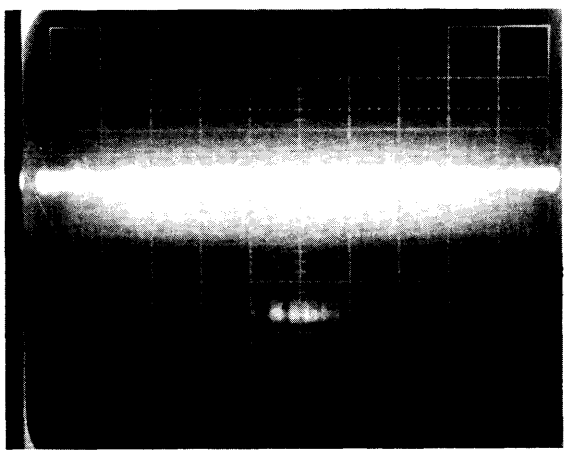
1. Change the horizontal sweep to 20 μs/cm. Initiate forward tape motion. Check that four negative pulses appear on the oscilloscope screen (see Figure 6-9).

2. Use the horizontal X10 magnifier to increase the horizontal display. Using the horizontal position knob, place the third pulse in the center of the screen. Check that the jitter is less than 6 μs (3 cm on the oscilloscope, as indicated in Figure 6-10). If jitter exceeds 6 μs (as indicated in Figure 6-11), replace the capstan motor.



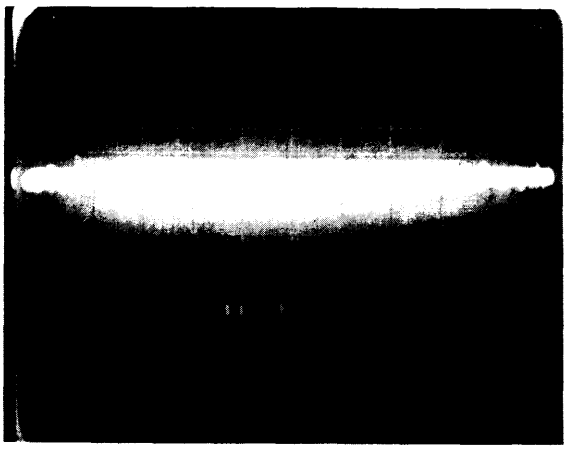
M-0611

Figure 6-9 Jitter Check: Scope Setup



M-0612

Figure 6-10 Jitter Check: Capstan Motor Good



M-0613

Figure 6-11 Capstan Motor Bad

6.4.3.8 Reverse Jitter Check – Initiate reverse tape motion. Repeat Paragraph 6.4.3.7 to check reverse jitter. Remove the X10 horizontal magnification feature from the oscilloscope.

6.4.3.9 Forward Skew (Azimuth) Check – Perform the skew check as follows:

1. Set up the oscilloscope as follows:

Horizontal:	2 μs/cm
Vertical:	0.1 V/cm (channels 1 and 2)
Vertical coupling:	ac
Triggering:	Normal Positive Slope Channel 1 triggered
Mode:	Chopped

   Place the channel 1 probe to pin A04L1 (channel 1) and place the channel 2 probe to pin F04R1 (channel 9).

2. Initiate forward tape motion, and synchronize the oscilloscope. Bring channels 1 and 2 into close proximity, as shown in Figure 6-12. The two channels should be aligned horizontally, to within 0.5 μs at their peaks. Some jitter is allowable, but any greater than 0.5 μs (in either direction) indicates a transport in need of tape path alignment (assuming, of course, a good skew tape).

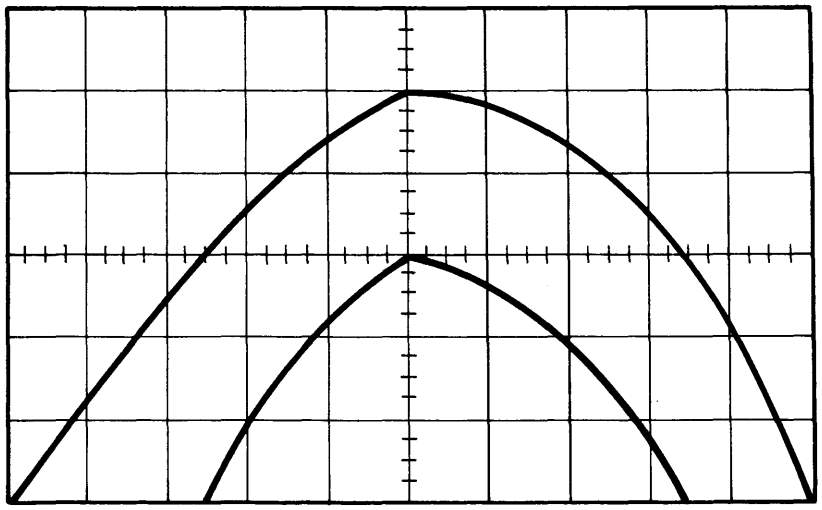


Figure 6-12 Skew Check (Azimuth)

6.4.3.10 Reverse Skew Check – Initiate reverse tape motion, and check that the waveforms do not separate by more than 2.5 μs. Here again, ± 0.5 μs of jitter is acceptable, but if it is greater or the waveforms separate more than 2.5 μs, the tape path alignment must be checked, especially in the area of capstan perpendicularity.

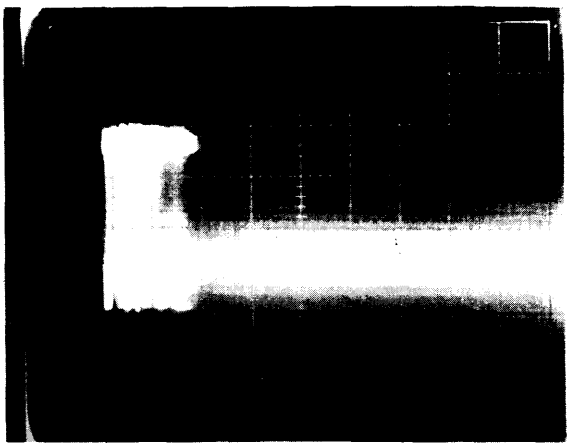
6.4.3.11 Dynamic Read Skew Packet Check – Check the dynamic read skew as follows:

1. Set up the oscilloscope:

Horizontal:	0.5 μs/cm
Vertical:	1 V/cm (channel 1)
Vertical Coupling:	dc
Triggering:	Normal
	Positive slope
	Channel 1 triggered

   Place the channel 1 probe to pin E04K1 (signal PACKET H).

2. Initiate forward tape motion and synchronize the oscilloscope. A waveform similar to Figure 6-13 should be observed. This PACKET H waveform (a logical OR of all nine tracks) should be no more than 2.5 μs from the beginning of the trace to the leading edge of the latest pulse seen. If a wider waveform is observed, the head may be worn (gap scatter increased), or the tape path may be in need of realignment.



M-0614

Figure 6-13 PACKET Waveform

3. Initiate reverse tape motion. PACKET width should not exceed 3.5 μs. If the PACKET width does exceed 3.5 μs, the tape path may be in need of realignment.

NOTE
An occasional jump in PACKET width of 1 μs is allowable in Paragraph 6.4.3.16 (usually due to tape defect); however, this should not occur more often than once per second.

4. Allow the skew tape to continue in reverse mode to BOT. Do not rewind. Remove the skew tape and reconnect the erase/write head cable to the M8916 module.

NOTE
If a semiannual PM procedure is scheduled, proceed to Paragraph 6.4.4; if not, continue with Paragraph 6.4.3.12.

6.4.3.12 Functional Test Diagnostic - Power down the transport and return the M8912 TFG module to slot EF03. Power up the transport. Load a good work tape to BOT and run the function, control, or instruction tests that are applicable to the CPU and DECmagtape/Controller system.

NOTE
Proceed to Paragraph 6.4.2.2 of the monthly PM procedure.

6.4.4 Semiannual PM Procedures

The items listed in this section are to be performed on a semiannual basis.

6.4.4.1 Forward Ramp Check – Check and adjust the forward acceleration ramp as follows:

1. Set these switches on the TFG module (M8912):

   SS RD, SS WRT, and WRT - DOWN
   S4-9 - OFF

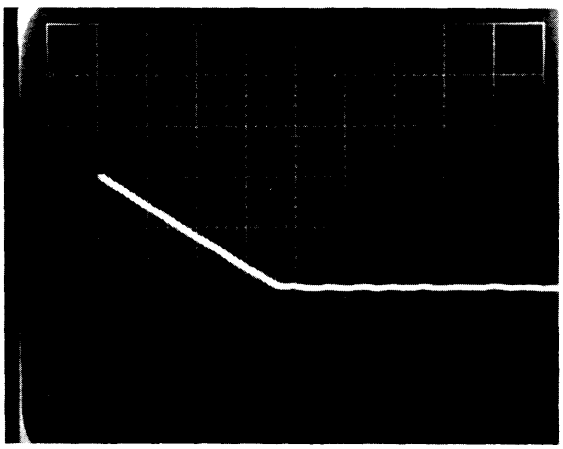
2. Set up the oscilloscope:

Horizontal:	2 ms/cm
Vertical:	0.2 V/cm (channel 1)
Triggering:	External Sync Negative slope Normal

   Place the channel 1 probe to pin P4-7 of the H607 mother board (TACH–V); refer to Figure 6-7. Connect the ground lead of the channel 1 probe to P2-7 of the H607 mother board. Place the external trigger probe to pin A03S1.

3. Load a scratch tape on the transport, and position it to BOT. The tape must have a write ring in place.

4. Initiate forward motion and place the SS RD switch (M8912) up. Synchronize the oscilloscope and a waveform similar to that in Figure 6-14 should appear. The duration of the negative-going slope should be 7 to 8 ms. If necessary, adjust R86 on the H607 mother board. Refer to Figure 6-7 for location of R86.



M-0615

Figure 6-14 Forward Acceleration Ramp

6.4.4.2 Reverse Ramp Check - Check and adjust the reverse acceleration ramp as follows:

Initiate reverse tape motion and set the oscilloscope to positive. Synchronize the oscilloscope, and a waveform similar to that in Figure 6-15 should appear. The duration of the positive-going slope should be 7 to 8 ms. If necessary, adjust R104 on the H607 mother board. Refer to Figure 6-7 for location of R104.

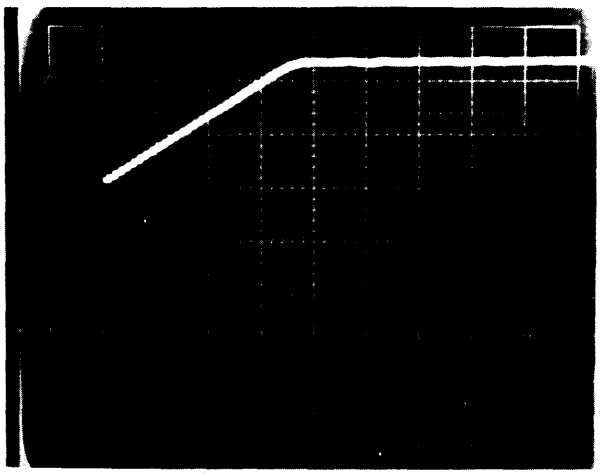


Figure 6-15 Reverse Acceleration Ramp

6.4.4.3 Tracking Check - Place the SS RD switch on the TFG (M8912) down and remove the oscilloscope probes. Check industry compatible tape tracking as follows:

1. Set up the TFG:

   SS WRT, SS RD and WRT - DOWN
   S5-1 through 8 - OFF
   S5-9, 10 - ON
   S6-1 through 10 - OFF

2. Set the FWD-REV maintenance switch to FWD, but do not initiate tape motion. Place SS RD momentarily up, then down. (This loads data into the TFG Write buffer.)

3. Position a scratch tape on the transport at BOT.

4. Place the WRT switch on the TFG up, and initiate forward tape motion.

5. Allow the tape to be written for approximately 10 seconds.

6. Place the WRT switch down, and rewind the tape.

7. Remove the tape from the transport, take it to a work area and proceed as follows:

   a. Unwind tape until BOT is reached, and cut the tape just before the marker.

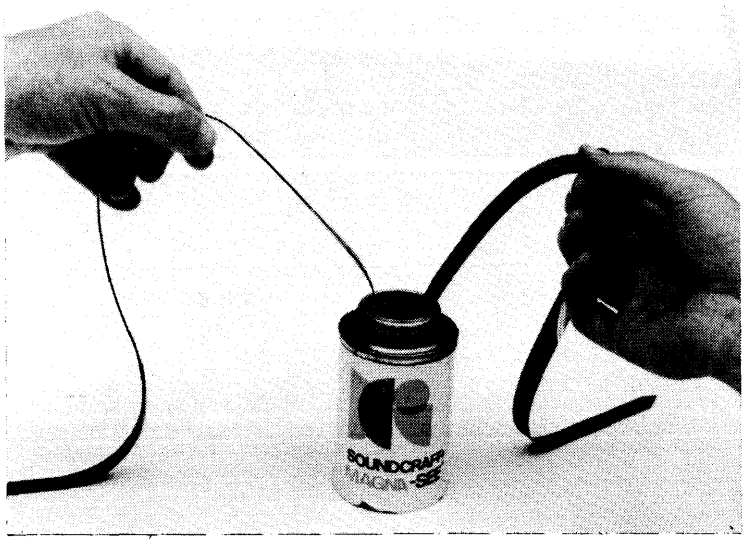
   b. Unwind .9 m (3 ft) of tape beyond the BOT marker, and cut the tape again.

   c. Shake the can of Magna-See™ solution vigorously.

   d. Dip the .9 m (3 ft) section of tape in Magna-See™ solution (refer to Figure 6-16). Try to keep a loop of tape in the bottom of the can.

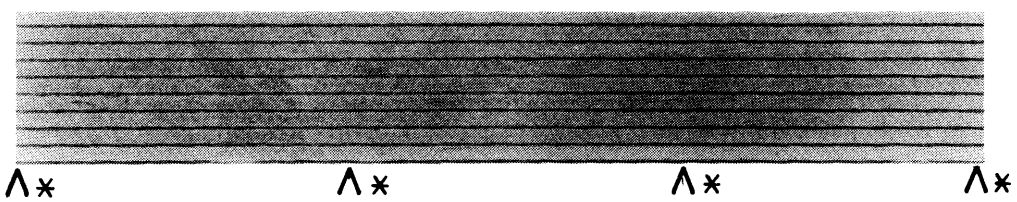
   e. Work the tape back and forth until the entire .9 m (3 ft) section (except for the ends being held) has been dipped into the solution.

   f. Allow the tape to dry. Data written on the tape should appear as the solution dries (Figure 6-17). If necessary, dip the tape again.



7660-24

Figure 6-16 Developing Magnetic Tape



7660-27

Figure 6-17 Developed Magnetic Tape

8. When the tape has been developed, proceed as follows:

   a. Place the developed tape flat on a white background.

   b. Make sure the tape is flat, then place a weight on each end.

   c. Check four points along the reference edge (the edge with the BOT marker) 3.7 cm (1.5 in) apart.

   d. Set the microscope according to Figure 6-18. Lay the penlight flat on the table, positioned so that it shines on the reflector.

   e. Ensure that a distance of .18 ± .08 mm (0.007 ± 0.003 in) from the reference edge to track 1 exists (see inset in Figure 6-18) at each of the four points mentioned in step c.

NOTE

If the tracking check described above fails, tape path alignment must be checked. If tape path alignment is within tolerance, the fault is probably in the head assembly and the head assembly should be replaced.

9. Install a new BOT marker 4.9 m (16 ft) from the front of the tape on the nonoxide side, against the reference edge. The reference edge faces the operator when the tape is installed on the transport.

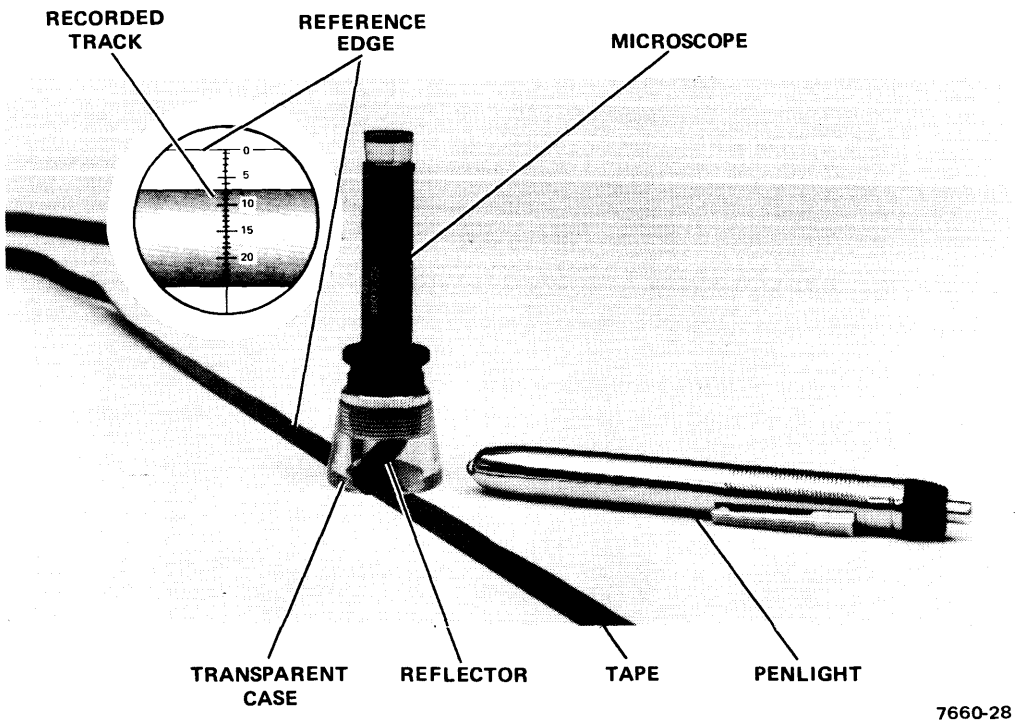


Figure 6-18 Track No. 1 Reference Edge Measurement

6.4.4.4 Erase Head Check – Check erase head functioning as follows:

1. Set up the TFG module:

   SS WRT, SS RD and WRT – DOWN
   S5-1 through 8 – OFF
   S5-9, 10 – ON
   S6-1 through 10 – OFF
   S4-1 through 10 – OFF
2. Load a work tape and position it to BOT.
3. Set the maintenance switch to FWD.
4. Place SS RD on the TFG module up, momentarily, then down.
5. Place the WRT switch on the TFG up and initiate tape motion.
6. Allow the tape to be written for at least 30 seconds, but not more than one minute.

NOTE
Steps 1 through 6 record an all "1s" tape at low density (full saturation). The following steps check the ability of the TE16 to erase a saturated tape by writing all "0s" at high density.

7. Halt tape motion, place the WRT switch down, and rewind the tape to BOT.
8. Set up the TFG module as follows:

   SS WRT, SS RD and WRT – DOWN
   S4-1 through 8 – ON
   S4-9, 10 – OFF
   S5-1 through 8 – ON
   S5-9, 10 – OFF
   S6-1 through 10 – ON
9. Set the maintenance switch to FWD, place SS WRT on the TFG up, and initiate tape motion.
10. Allow the tape to be written for at least one minute.
11. Lower the SS WRT switch, and rewind the tape.
12. Set up the oscilloscope as follows:

Horizontal:	1 ms/cm
Vertical:	0.1 V/cm (channel 1)
Vertical Coupling:	ac
Triggering:	Auto
	Channel 1 triggered

Place the channel 1 probe to pin A04L1 and the probe ground to pin B04C2.

13. Initiate forward tape motion. Measure the unerased (residual) signal level for maximum level. Ensure a good oscilloscope ground while doing this. Maximum level must be less than 400 mV p-p. Failure to meet this criteria (in steps 13, 14, or 15) will require replacement of the head plate assembly. The erase head is not adjustable in the field.

14. Rewind the tape. Place the channel 1 probe on pin C04L1; ensure a good ground. Initiate forward motion. Check the unerased signal level (maximum = 400 mV).

15. Rewind the tape. Place the Channel 1 probe on pin F04R1; ensure a good ground. Initiate forward motion. Check the unerased signal level (maximum = 400 mV).

6.4.4.5 Read Amplifier Check

NOTE
Paragraphs 6.4.4.5, 6, and 7 require comparison of read amplifier outputs under varied conditions. Photocopy Table 6-3, or prepare a similar table.

Table 6-3 Read Amplitude, Residual Amplitude, and Balance Checks

Track	Pin No.	Read Amplitude	Residual Amplitude	Reverse Balance Amplitude
1	A4-L1			
2	B4-B1		N/A	N/A
3	B4-M1		N/A	N/A
4	C4-K1		N/A	N/A
5	C4-L1			
6	D4-P1		N/A	N/A
7	D4-R1		N/A	N/A
8	F4-P1		N/A	N/A
9	F4-R1			

Check the Read Amplifier outputs as follows:

1. Rewind the tape, and remove it from the transport.

2. Clean the read/write head, erase head, and tape cleaner.

3. Load a good quality work tape and position it at BOT.

4. Set up the oscilloscope as follows:

Horizontal:	2 ms/cm
Vertical:	2 V/cm (channel 1)
Trigger:	Normal
	Channel 1 triggered

5. Set the switches on the TFG module as follows:

   S4-1 through 8 - ON
   S4-9, 10 - OFF
   S5-1 through 8 - OFF
   S5-9, 10 - ON
   S6-1 through 8 - OFF
   SS WRT, SS RD and WRT - DOWN

6. Place the SS WRT switch on the TFG up, and place the channel 1 probe to pin A04L1. The peak-to-peak amplitude of the signal should be in the range of 10 to 13 V. Record the results in the read amplitude column of Table 6-3 beside track 1.

7. Repeat step 6, for all nine tracks, recording the results in the same column. If any track is out of the acceptable range, adjust all nine channels to 12 V p-p. The adjustment potentiometers for the tracks are arranged sequentially from top (track 1) to bottom (track 9) on the G066 module. They are accessible from the side.

8. Place the SS WRT switch on the TFG module down and rewind the tape.

6.4.4.6 Residual Amplitude Check - Perform the residual amplitude check as follows. (Residual amplitude is the amplitude left on the tape after several read operations. Some amount of erasure can be expected during the first few read passes due to residual magnetism in the write and erase head poles.):

1. Set the maintenance switch to FWD and raise SS WRT. Allow start-stop data to be recorded for at least 30 seconds. Place SS WRT down and rewind the tape.

2. Initiate forward tape motion and allow the tape to run in a forward direction for 15 seconds. Rewind the tape. Repeat this operation ten times.

3. Leave the oscilloscope set up as in Paragraph 6.4.4.5. Place the channel 1 probe on pin A04L1 and initiate forward tape motion. Record the p-p amplifier output in the residual amplitude column of Table 6-3. Rewind the tape.

4. Repeat step 3 for tracks 5 (C04L1) and 9 (F04R1), recording their results in the same column.

NOTE

In steps 3 and 4, the assumption is that the tape does not run in a forward direction for more than 15 seconds. If there is any doubt, rewind the tape and recheck the forward residual amplitude.

5. Compare the entries in the residual amplitude column of the table with entries in the read amplitude column. If the residual amplitude entries show a decrease of greater than 20 percent of any of the three tracks, replace the head assembly and perform the tracking check (Paragraph 6.4.4.3).

6.4.4.7 Reverse Balance Check – Perform the reverse balance check as follows:

1. Rewind the tape.

2. Place the channel 1 probe on pin A04L1 (oscilloscope still remains set up the same). Initiate forward tape motion and run tape forward for 10 seconds. Now initiate reverse tape motion and record the p-p amplifier output in the reverse amplitude column of Table 6-3.

3. Repeat step 2 for tracks 5 (C04L1) and 9 (F04R1), recording their results in the same column.

4. Compare entries in the reverse balance column to entries in the residual amplitude column. If the reverse amplitude entries show an increase or decrease of greater than 10 percent, the tape path alignment must be rechecked or the head assembly may have to be replaced.

6.4.4.8 H607 Clock Check – Perform the H607 clock check as follows:

1. Set up the oscilloscope:

Horizontal:	1 ms/cm
Vertical:	1 V/cm (Channel 1)
Triggering:	Normal Positive slope Channel 1 triggered

   Place the channel 1 probe to chip E8, pin 5 of the H607 daughter board (5412262).

2. A pulse waveform should be observed, with a period (leading edge to leading edge) of 5 ms ± 0.5 ms. If the waveform is out of this specification, adjust potentiometer R16 on the daughter board so that the waveform period becomes 5 ms ± 0 ms. Refer to Figure 6-19 for the location of R16.

3. Resecure the H607 daughter board to the mother board.

6.4.4.9 G066 Read Threshold Check – Perform the G066 read threshold check as follows:

1. Replace the TFG module (M8912) in slot EF03.

2. Set up the oscilloscope:

Horizontal:	50 ms/cm
Vertical:	1 V/cm (channel 1)
Triggering:	Auto

   Place the channel 1 probe to pin E04D1.

3. Load a good work tape, and position it at BOT.

4. Load and start the TE10/16 Reliability Test that is applicable to the specific CPU and DECmagtape system.

5. Select an 800 bits/in NRZI write operation with an all "1s" data pattern via the tests conversation mode.

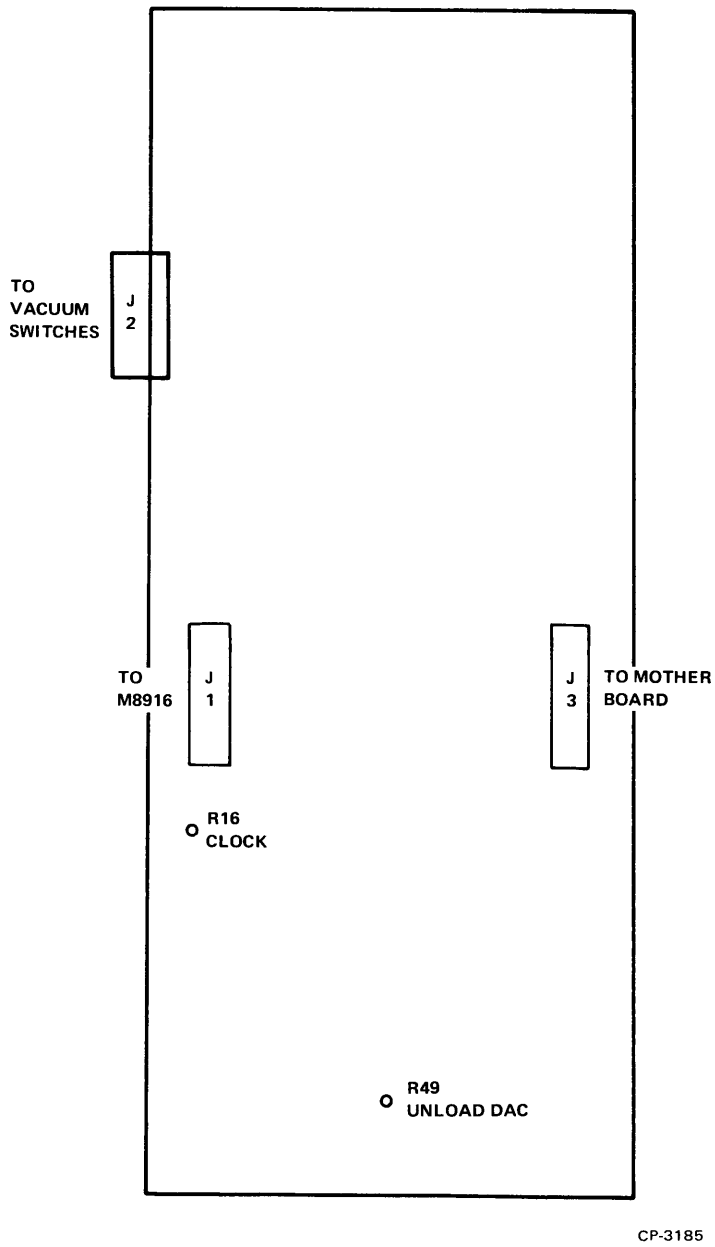


Figure 6-19 H607 Daughter Board

6. During the NRZI write command, the voltage read on the oscilloscope should be +5.1 ± 0.4 V.

7. Stop the test and rewind the tape.

8. Now select an 800 bits/in NRZI read operation with an all "1s" data pattern.

9. During the NRZI read operation, the oscilloscope should indicate +3.9 ± 0.4 V.

NOTE
If any voltage is out of range, replace the G066.

10. The following steps apply to TE16/TM02,3 DECmagtape systems only:

    a. Stop the test and rewind the tape.

    b. Now select a 1600 bits/in phase encoded (PE) write operation with an all "1s" data pattern.

    c. During the PE write operation, the oscilloscope should indicate +3.6 ± 0.4 V.

    d. Stop the test and rewind the tape.

    e. Now select a 1600 bits/in PE read operation with all "1s" data pattern.

    f. Due to the dual threshold feature, this operation will result in two voltage readings and a step in the waveform (Figure 6-20). During the interrecord gap, the voltage should be +3.35 ± 0.4 V. However, when the formatter recognizes the preamble, the threshold will drop to -3.25 ± 0.4 V.

NOTE
If an annual PM is to be performed at this time, proceed to Paragraph 6.4.5. If an annual PM is not to be performed now, continue with Paragraph 6.4.3.17 of the quarterly PM procedure.

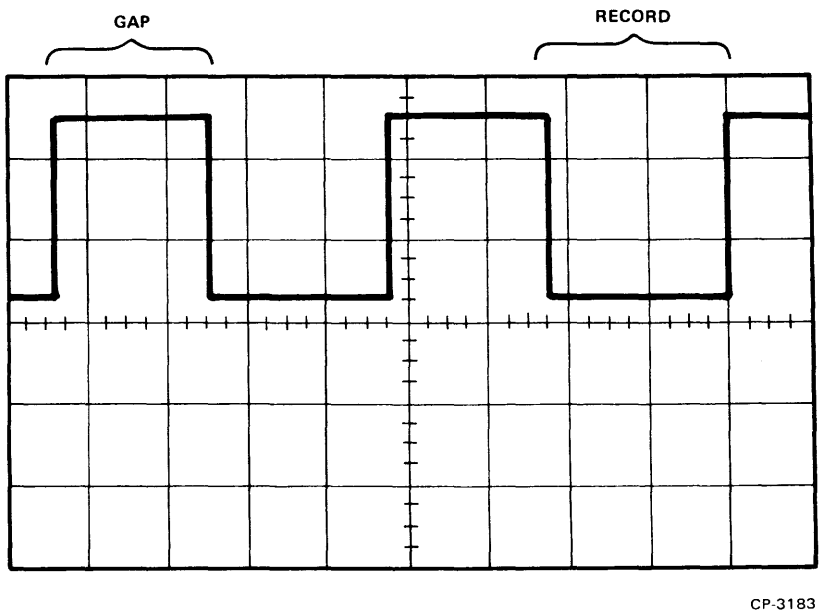


Figure 6-20 Dual PE Read Threshold

6.4.5 Annual PM Procedure

These steps should be performed on an annual basis:

6.4.5.1 Reel Motor Filter Replacement - Replace the reel motor filters as follows:

1. Remove the entire filter assembly from the rear of the lower reel motor by unscrewing it in a counter clockwise direction.

2. Wrap 1-1/4 turns of Teflon tape around the threads of a new filter assembly, and thread it into the lower reel motor. Hand tighten it only.

3. Repeat steps 1 and 2 for the upper reel motor filter.

6.4.5.2 Clean and Regap Reel Motor Brakes - Disassemble, clean, and reassemble the reel motor brakes using this procedure:

1. With power off, loosen the Allen head screw located on the clamp for the lower brake. (Access both upper and lower brakes from the left hand side of the transport; refer to Figure 6-21.)

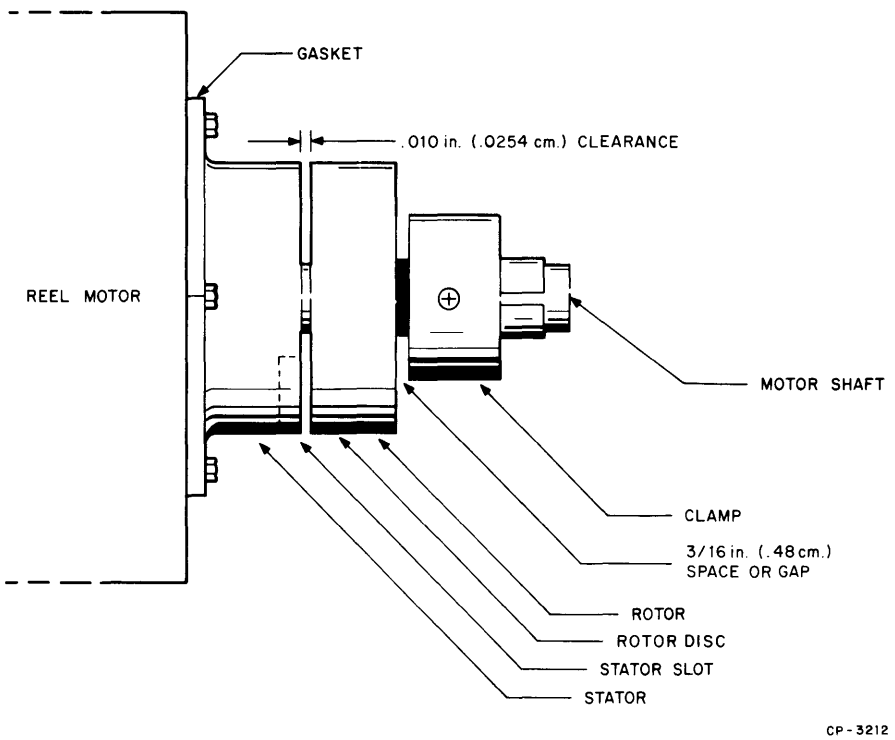


Figure 6-21 Brake Assembly

2. Remove the clamp, rotor, and rotor disk. Push a cotton swab through each of the inserts (locating holes) that hold the rotor disk and rotor to ensure they are securely held in the rotor and that they do not protrude so as to interfere with operation of the rotor disk. If the inserts are loose, replace the entire brake assembly as a unit (Paragraph 6.6.11.)

3. Using a dry, clean, lint-free cloth or wipe, clean the following:

   a. The brake surface of the stator (stator is mounted to the reel motor).

   b. Both sides of the rotor disk, including locating pins.

   c. The face of the rotor next to the rotor disk.

NOTE
Avoid skin contact with the brake surfaces; body oils are detrimental to brake function.

4. Install the rotor disk into the rotor. Select the mating combination that allows for smoothest insertion and retraction of rotor disk pins into the rotor locating holes. Try each of the 120-degree intervals for the best fit.

5. Replace the brake, leaving a clearance of .254 mm (.010 in) between the rotor disk and the stator. When clearance is correct, tighten the Allen screw on the clamp.

6. With the .254 mm (.010 in) feeler gauge inserted between the stator and the rotor, rotate the reel motor manually from the front of the unit to see that the brake is spaced uniformly all around. If necessary, rotate the rotor disk at 120-degree intervals to determine the best position for uniform separation. An excessively high or low spot is cause for replacing the brake assembly.

7. Repeat steps 1 through 6 for the upper brake assembly.

8. When the above steps have been completed for both reels, rotate both reels, feeling for free rotation and listening to ensure that there is no squealing from stator/rotor disk contact.

NOTE
Return to Paragraph 6.4.3.12 of the quarterly PM procedure.

6.5 ADJUSTMENT/ALIGNMENT PROCEDURES

All adjustments and alignment procedures are listed in this section.

6.5.1 Tape Path Alignment Procedure

The tape path alignment procedure should be followed when:

1. The capstan wheel, capstan motor, roller guide, or fixed guide is replaced.

2. The forward and/or reverse skew is found to exceed specifications.

3. An amplitude difference of more than 10 percent is seen between forward and reverse amplifier output.

4. A visible change in the tape path across the capstan is apparent when changing from forward to reverse tape motion.

5. The measurement of the reference edge to track 1 of a developed (with Magna-See™ solution) tape shows a result different from .18 ± .08 mm (0.007 ± 0.003 in), and it is not the fault of the head.

6. Diagnostics indicate a "read reverse" error rate that exceeds specification in the monthly PM procedures (TE16 only).

7. Incompatibility with other tape transports persists after performing tape speed, mechanical skew, capstan ramp, and read amplitude adjustments and all diagnostic tests run.

The objectives of the tape path alignment procedure are:

1. To establish a single plane for tape to travel from supply reel to take-up reel, independent of the capstan and fixed guides. This is accomplished by aligning reel hubs and roller guides.

2. To mount the head plate and fixed guides in the plane established in step 1. This is accomplished by establishing the relationship between the reference surfaces used in step 1 and the surface onto which the head plate and guides are mounted. If the relationship is not nominal, appropriate shims are placed underneath the head plate and guides to bring the reference edges of the fixed guides into the proper plane.

3. To minimize the amount of distortion to the tape as it travels through the plane established in steps 1 and 2. This is accomplished by shimming the capstan motor so that the capstan motor shaft becomes perpendicular to the tape path.

NOTE

The effect of accomplishing the above steps is to minimize static skew, dynamic skew, and tracking error in both forward and reverse directions. Skew is the total amount of nonperpendicularity of characters written on tape. Tracking is defined by ANSI standards as the measurement from the reference edge to each track center line. Improper tracking takes two forms:

1. **Read – A tape transport that is tracking incorrectly will not have its read head elements centered over tracks correctly written by another tape transport.**

2. **Write – A tape transport tracking incorrectly will write data tracks that are not correctly spaced from the reference edge of the tape. Therefore, a transport with proper tracking alignment would not have its read head elements centered on the incorrectly written tracks.**

6.5.1.1 Basic Tape Path Plane – Perform the following steps to establish a basic tape path plane:

1. Fixed Reel Hub Height

a. Remove the trim plate and the inner and outer reel flanges by unscrewing the three Phillips head pan screws holding them to the hub (Figure 6-22).

b. Loosen the two Allen head set screws holding the hub to the reel motor shaft.

c. Using the block gauge (94-05143), set the hub height (Figure 6-23) and then tighten the set screws.

d. Reassemble the flanges and trim plate to the hub casting.

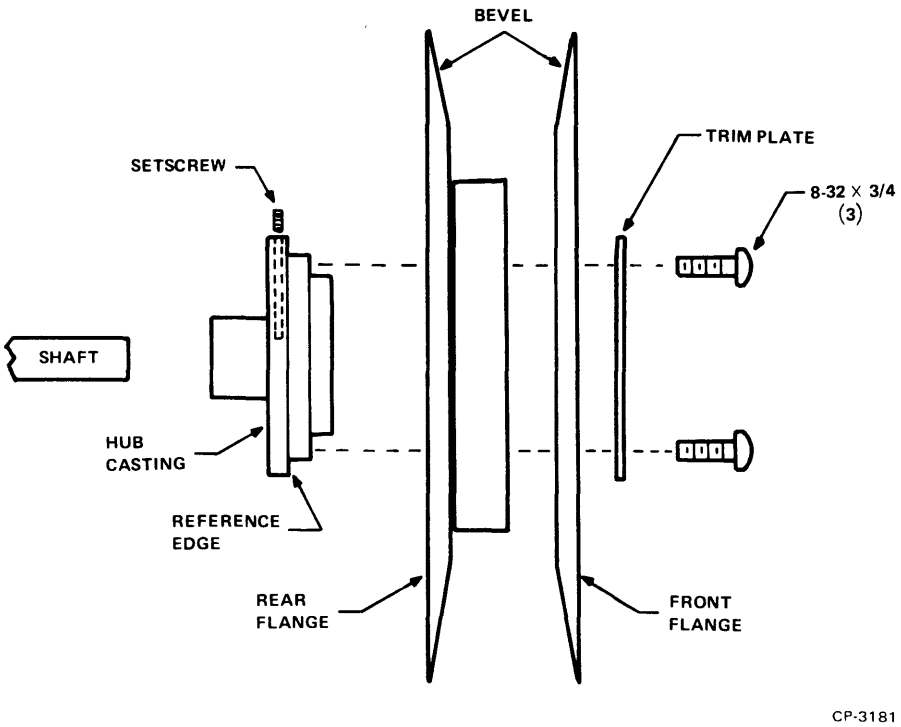


Figure 6-22 Fixed Reel Assembly

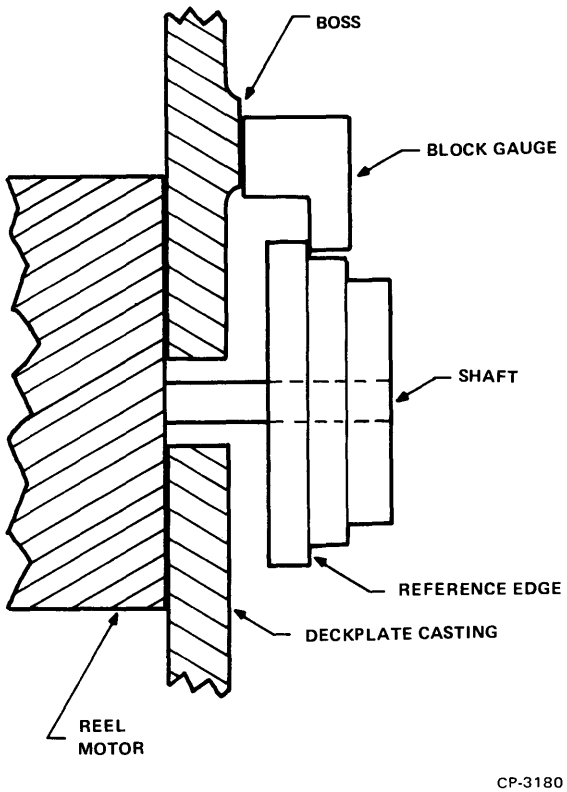


Figure 6-23 Hub Height Adjustment

2. **Snap-Lock Hub Height** - The snap-lock (supply reel) hub height is checked in the same manner as the fixed reel hub height. The block gauge is pressed against the casting boss above the hub and referenced to the step in the hub. If adjustment is necessary, circular shims must be added to or removed from the adapter-rear hub interface. Refer to Paragraph 6.6.1 for disassembly instructions.

3. Roller Guide Adjustment

a. Adjust the two vacuum column roller guides as follows:

(1) Prepare a gauge according to Figure 6-24.

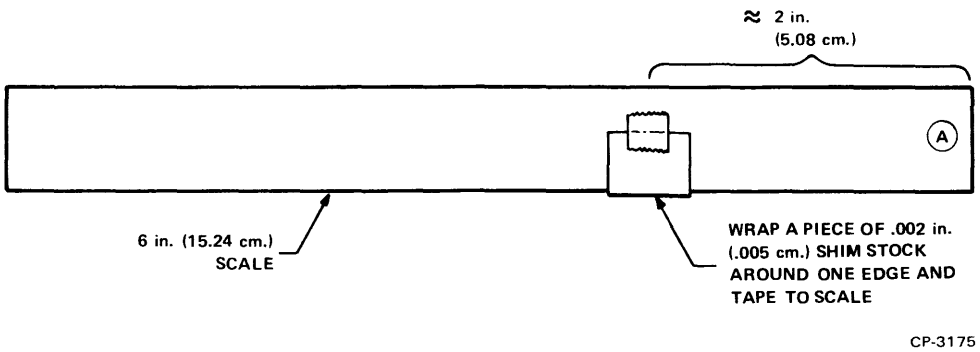


Figure 6-24 Roller Guide Gauge

(2) Loosen the roller guide clamp screw, and pull the guide slightly away from the casting.

(3) With point A of the gauge contacting the bottom inside surface of the roller guide (Figure 6-25), push the gauge down toward the casting until the 2-mil shim just contacts the bottom of the vacuum column. This ensures that the tape guide is set to the middle of the buffer column.

(4) Tighten the locking clamp.

b. Adjust the top center (take-up reel) roller guide as follows:

(1) Push the roller guide shaft into the casting and roughly (by eye) adjust its height. Tighten the locking clamp.

(2) Load a scratch tape and run forward past BOT. Observe the edges of the roller at points A and B (Figure 6-26) to check for tape puckering. If the tape is puckering, the clamp should be loosened and the roller moved in or out as necessary.

(3) The tape should now be run to EOT, rechecking the roller guide for puckering in the process. Readjust as necessary. Also, check to see that the edges of the tape are not striking the flanges of the take-up reel.

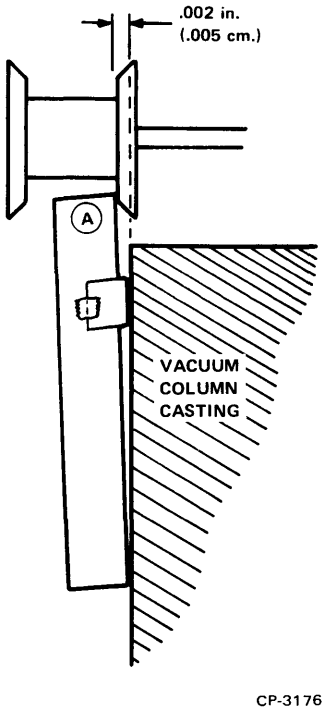


Figure 6-25 Roller Guide Adjustment

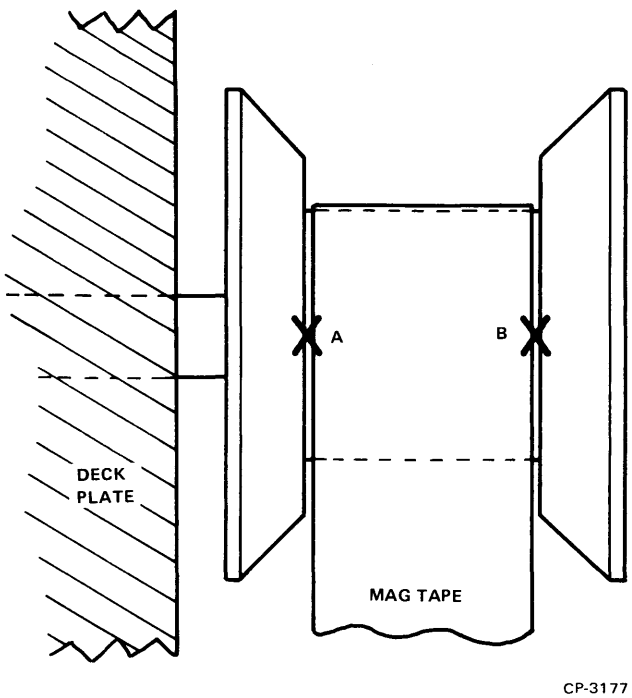


Figure 6-26 Take-Up Reel Roller Guide

6.5.1.2 Head Plate and Fixed Guide Tape Path Plane – Proceed as follows to establish the head plate and fixed guide alignment:

1. Two measurements are written on the deckplate, underneath the headplate. The first measurement is the depth of the left hand buffer column. It will be in the range of 1.26 cm to 1.28 cm (0.502 in to 0.504 in). The second measurement value is the distance from the top right hand rail of the left buffer column to the head mounting surface (HMS). It is this measurement that is used to determine the size of the shim that is necessary under the head plate. This value will be in the range of 2.84 cm to 2.85 cm (1.119 in to 1.123 in). If these values are not written or are unreadable, proceed to perform the measurements:

   NOTES

   1. **Measure the depth with the depth micrometer from the outer surface of the left vacuum column to the surface onto which the head plate was mounted. The nominal value is 2.84 cm (1.120 in). Call this value HMS (Figure 6-27).**

   2. **If this measurement is difficult because only one side of the micrometer can be seated on the vacuum column surface, it is, therefore, advised to:**

      a. **Place the micrometer base at 45 degrees to the vacuum column surface (gives greater seating area).**

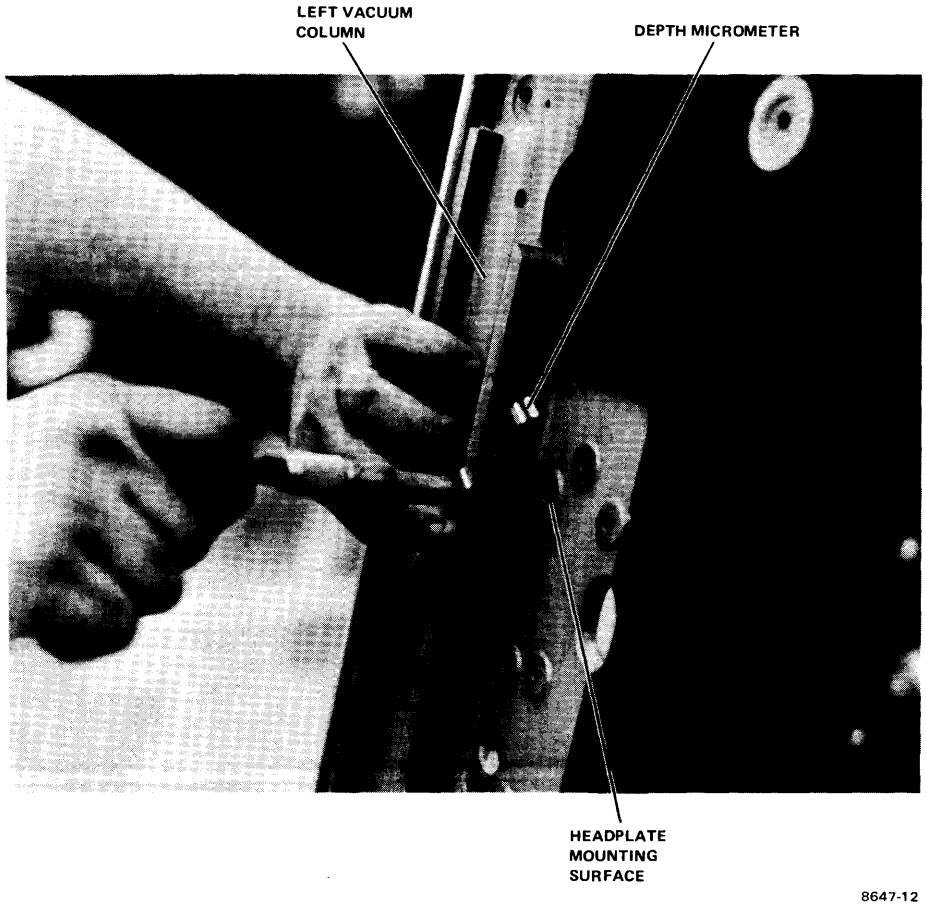
      b. **Make the measurement with the micrometer shaft as close as possible to the vacuum column wall (gives more leverage to keep the micrometer base seated and less distance to project error).**

      c. **Repeat the measurement several times to verify results.**

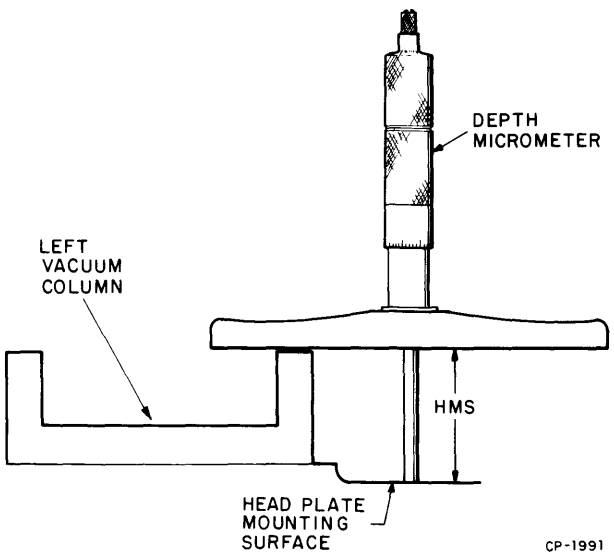
2. Now subtract 2.84 cm (1.120 in) from the HMS value obtained in step 1 (i.e., HMS - 2.84 cm or 1.120 in).

3. If the result obtained in step 2 is zero or negative, mount the head plate and both fixed guides without shims.

4. If the result obtained in step 2 is positive, cut six shims (Figure 6-28), of which the thickness value is that of the result, and place them as follows: one under each of the three shoulder screws, one at the vacuum port, and one under each of the two fixed guides. See Paragraph 6.6.6 and 6.6.7 for mounting instructions and Figure 6-29 for locations.



A. Placement of Depth Micrometer



B. Bottom View of HMS Measurement

Figure 6-27 Measurement of Head Plate Mounting Surface

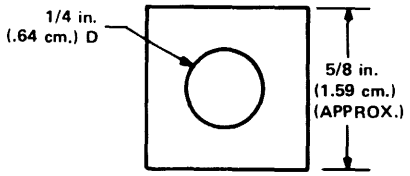


Figure 6-28 Shim Dimension

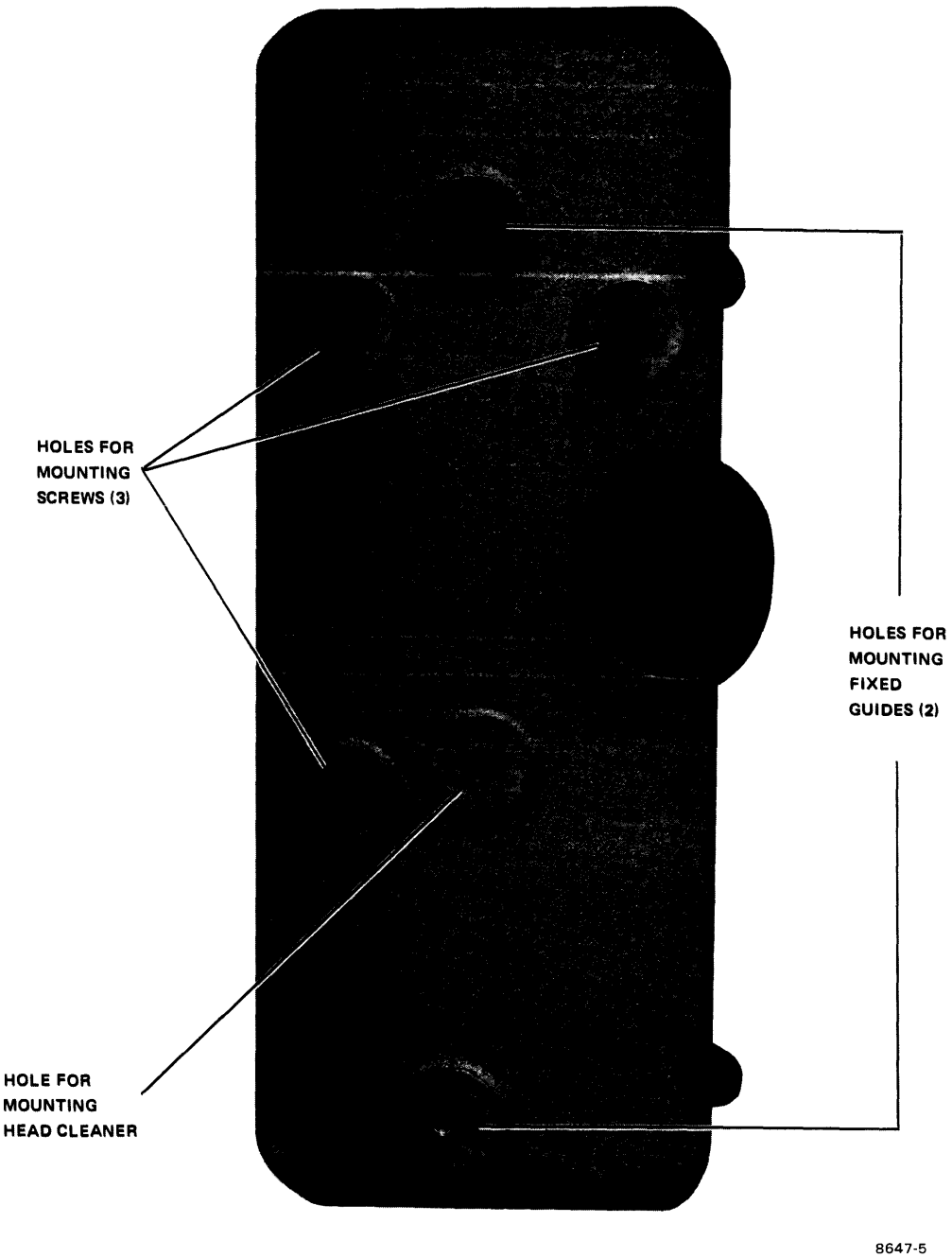


Figure 6-29 Location of Shims under Head Plate Assembly

Summary:

1. Paragraph 6.5.1.1 procedures set the reel hubs and roller guides in the same plane as the vacuum columns.

2. Paragraph 6.5.1.2 procedures set the reference edge of the fixed guides into the plane of the tape coming out of the vacuum columns and the head centered in that plane.

NOTE

Paragraph 6.5.1.3 procedures will set the shaft of the capstan motor perpendicular to the tape path, to minimize distortion of the plane established in steps 1 and 2.

6.5.1.3 Aligning Capstan Motor Shaft Perpendicular to Tape Path – Steps 1 through 21 ensure that the capstan motor shaft is perpendicular to the tape path. Two conditions can cause nonperpendicularity of the motor shaft to the tape path: One is the capstan motor shaft not being perpendicular to the mounting face of the motor. Figure 6-30A and C are examples of this condition. [Specifications allow .0127 cm (0.005 in) of nonperpendicularity of the motor shaft.] The other condition is nonparallelism between the motor mounting surface on the back of the casting and the front surface of the casting. Figure 6-30B illustrates this situation. [Specifications allow .0102 cm (0.004 in) of nonparallelism between the machined surfaces on the front and back of the casting.]

The effect of the capstan motor shaft not being perpendicular to the tape path depends on the direction of the nonperpendicularity (i.e., whether the motor shaft is pointing up, down, toward the left, or the right). When the shaft is pointing down (Figure 6-30A), the top of the capstan is away from the casting, causing the tape to track away from the casting. Hard guiding occurs on the vacuum door glass and the fixed guides in both forward and reverse directions. When the shaft is pointing up (Figure 6-30B), the bottom of the capstan is away from the casting, causing the tape to track toward the casting. Hard guiding occurs on the vacuum column floor and the spring-loaded guides in both forward and reverse directions. When the shaft is pointing toward the left (Figure 6-30C), the tape tracks away from the casting in the forward direction and toward the casting in the reverse direction. If the shaft were pointing toward the right, the opposite would be true (i.e., the tape would track toward the casting in the forward direction and away from the casting in the reverse direction).

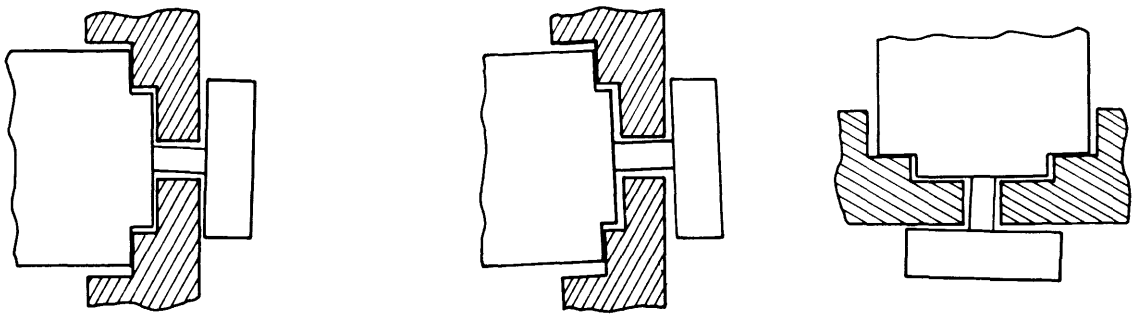
Figure 6-41 is a flowchart of capstan alignment, summarizing and complementing this alignment procedure.

Perform the following steps to align the capstan motor shaft perpendicular to the tape path.

1. Remove the capstan by loosening the capstan locking clamp with an Allen wrench, and remove the capstan and clamp.

NOTE

If the capstan is hard to remove, it may be bent and should be replaced. The inside of the capstan should be checked for burrs in the area of the slots. The end of the capstan motor shaft should also be checked for burrs (Figure 6-31).



A. Side View – Capstan Motor Shaft Pointing Down due to Non-Perpendicularity of Shaft

CP-1994

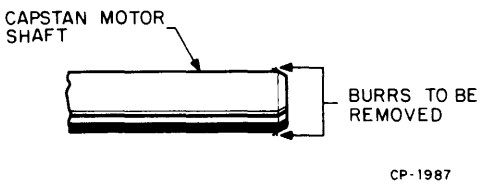
B. Side View – Capstan Motor Shaft Pointing Up due to Non-parallelism of Machined Motor Mounting Surfaces

CP-1995

C. Top View – Capstan Tipped Toward Casting on Left Side and Away from Casting on Right Side due to Non-perpendicularity of Motor Shaft

CP-1996

Figure 6-30 Examples of Capstan Nonperpendicularity



CP-1987

Figure 6-31 Location of Possible Capstan Burrs

2. Remove the capstan motor by unplugging P4 from the H607 mother board and removing the four bolts holding the capstan motor on the casting.

CAUTION

Because the bolt heads are in front of the casting and the motor is on the rear, caution should be used so that the motor does not fall when the screws are removed.

NOTE

Do not attempt to remove the tachometer portion of the motor; the two are replaced as an assembly.

3. Check the capstan motor and casting for the following:

   a. The capstan motor specification template does not interfere with the motor mounting on the casting. If there is interference, remove the template.

   b. The motor does not have any burrs on the mounting surface that would prevent it from mounting squarely on the casting.

   c. Ensure the mounting surface of both the motor and casting are free of dirt, gummy substances, and burrs pushed up by machining operations.

4. Lift up and remove the vacuum column door.

5. Use the depth micrometer to measure depth, if it is not already known, from the outer surface of the left vacuum column to the floor of the left vacuum column. Nominal depth is 1.26 cm (0.502 in). Call this value "LVC" (Figure 6-32).

6. Subtract 0.500 from LVC; call the resulting value "X" (LVC - 0.500 = X). Record value "X," as it will be used in Step 16.

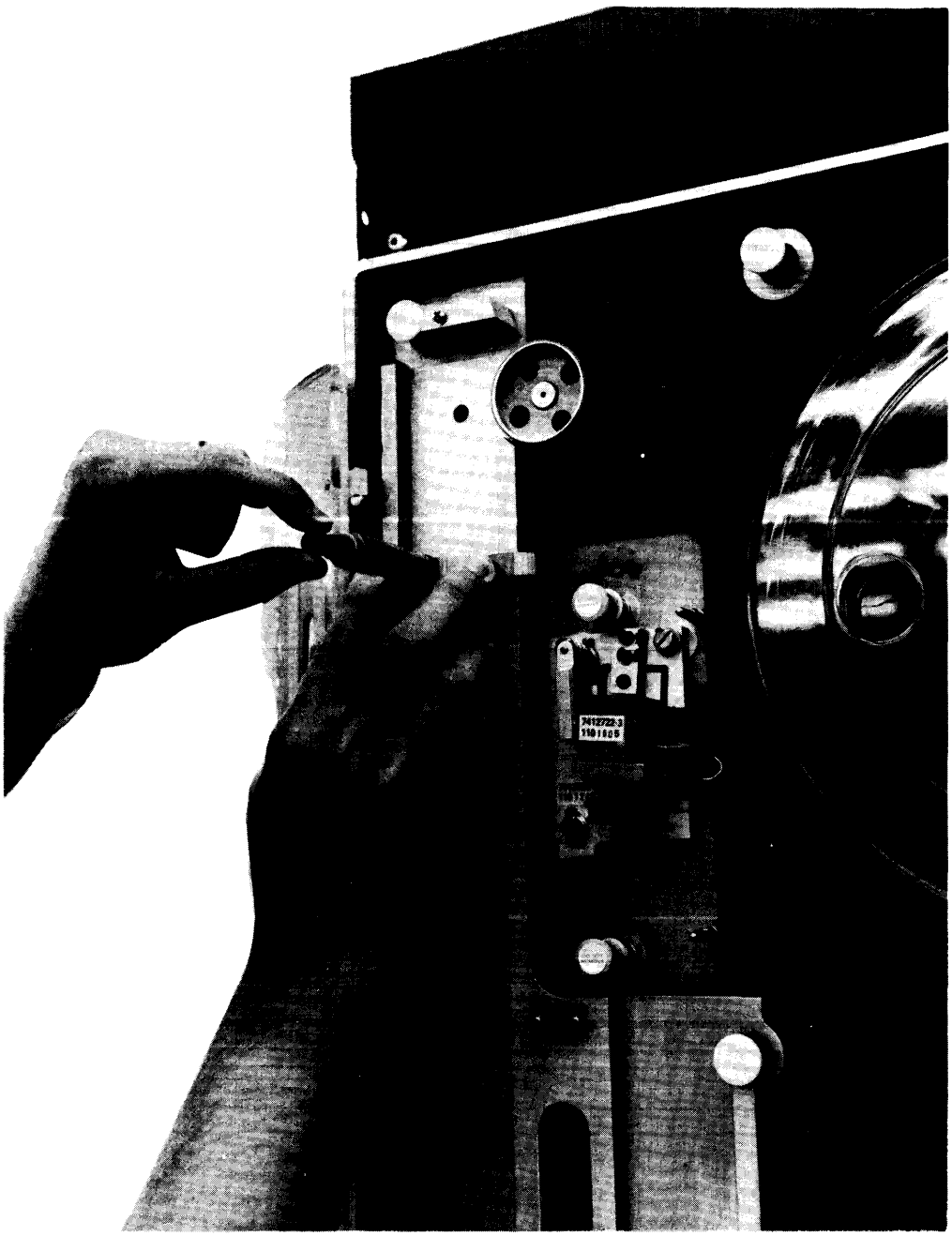
NOTE

"X" is the distance that the inside edge of the tape should be from the floor of the left vacuum column when the outside edge is .005 cm (.002 in) from the outer surface of the left vacuum column. If the capstan motor shaft is perpendicular to the tape path and if Paragraphs 6.5.1.1 and 6.5.1.2 procedures were performed correctly, "X" is equal to this distance.

7. Remount the capstan motor on the casting (four bolts). Tighten the mounting bolts.

8. Clean the capstan with a water-dampened wipe or lint-free cloth. Do not use any cleaner other than water on the capstan.

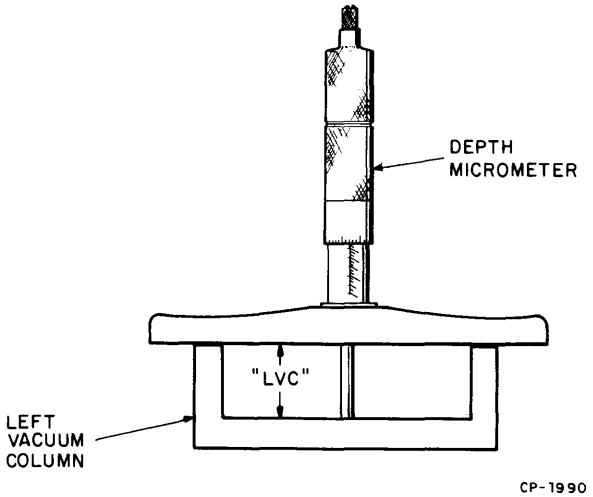
9. Reposition the capstan on the capstan motor shaft. Tighten the clamp.



8647-13

A. Placement of Depth Micrometer

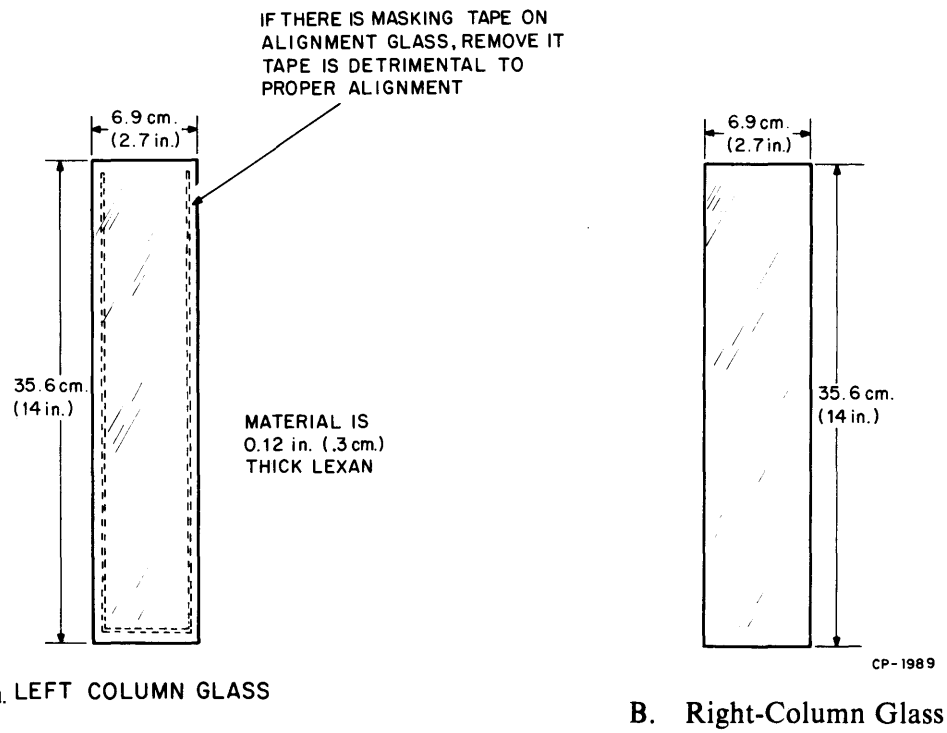
Figure 6-32 Measuring Depth of Left Vacuum Column (LVC) (Sheet 1 of 2)



B. Top View of LVC Measurement

Figure 6-32 Measuring Depth of Left Vacuum Column (LVC) (Sheet 2 of 2)

10. Load a good quality tape, using the alignment glass (Figure 6-33). It will be necessary to hold the glass doors with one hand while pressing LOAD with the other (Figure 6-34).



a. LEFT COLUMN GLASS

B. Right-Column Glass

Figure 6-33 Alignment Glass

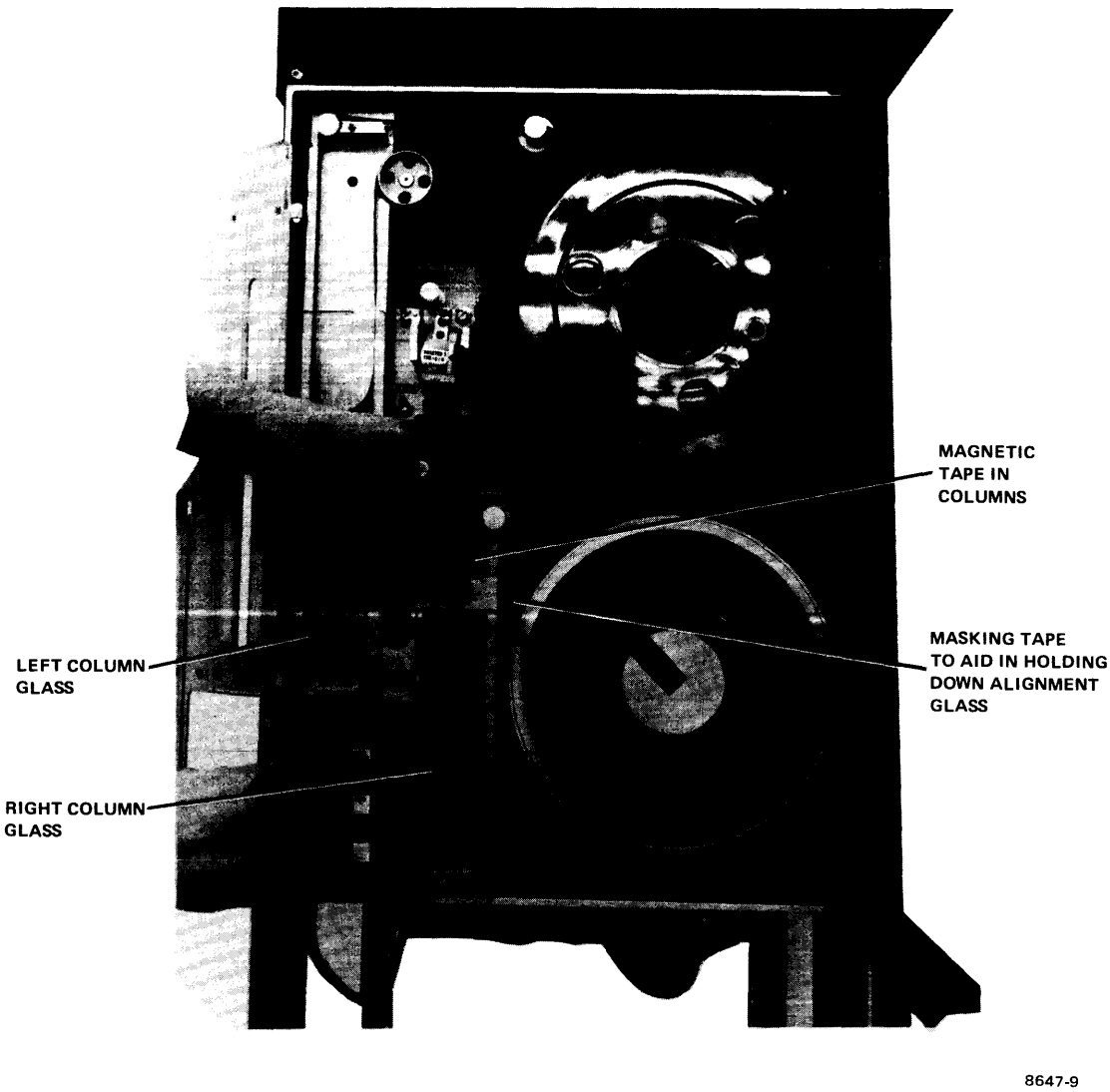


Figure 6-34 Using Alignment Glass to Load Tape

11. Ensure the tape rides in the center of the capstan. This can be done by running the tape forward several feet and checking the tape position on the capstan. The capstan can be moved in or out to ensure the tape is in the middle of the capstan.

    Ensure the capstan is clamped securely to the capstan motor shaft.

12. Now begin aligning the capstan motor shaft (making it perpendicular to the tape path). This is done by placing shims between the capstan motor mounting face and the casting surface onto which the capstan motor is mounted. Shims are placed in the vertical axis to correct for capstan steering when both forward and reverse tape motion produces the same steering characteristic (i.e., tape steers toward the deck plate or toward the vacuum column glass in both directions). Shims are placed in the horizontal axis if forward and reverse tape motion show opposite steering characteristics. Figure 6-35 shows shim placements.

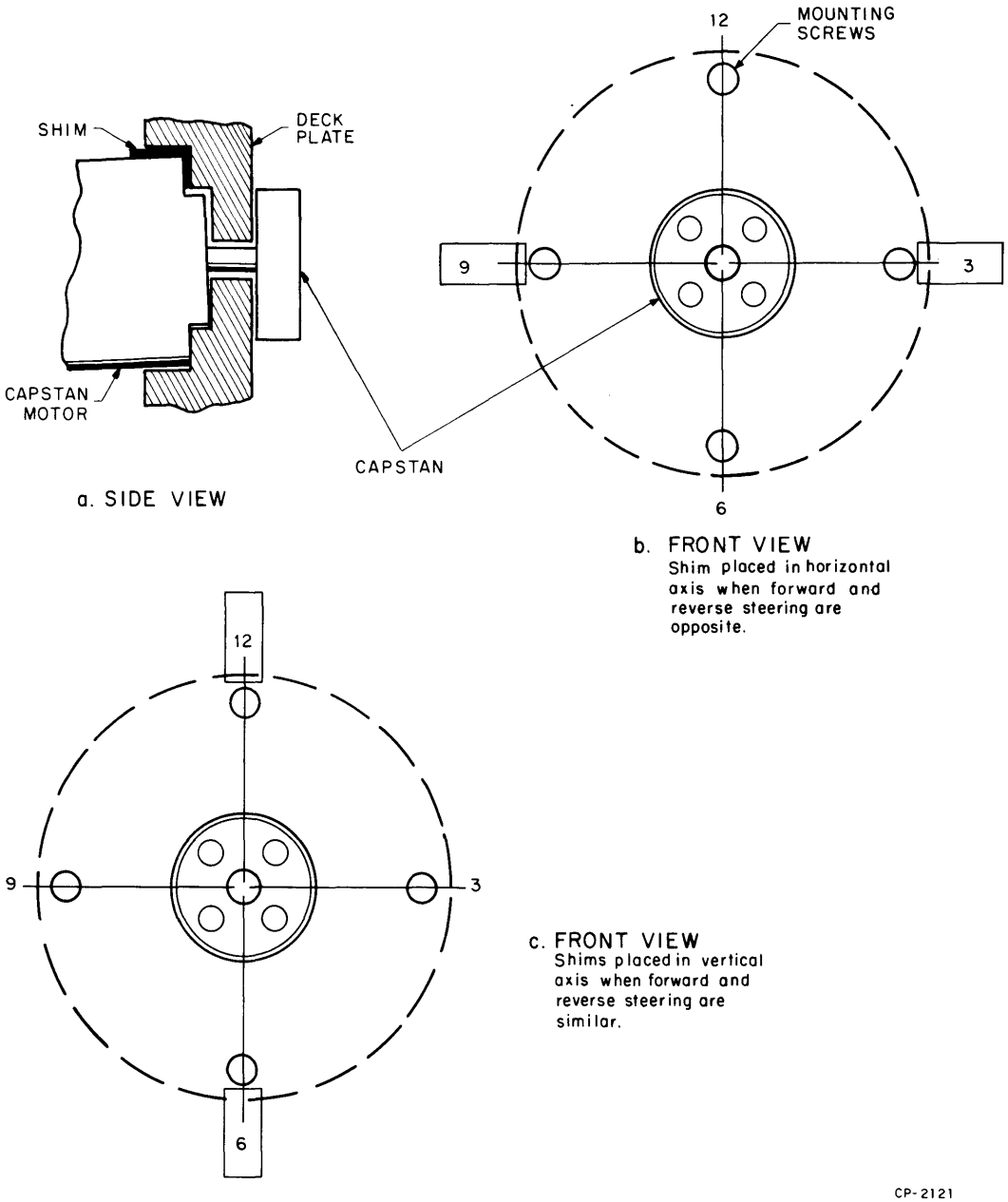


Figure 6-35 Capstan Motor Shim Placement

A few hints will assist in performing the procedure in the shortest possible time:

a. The sequence of tightening the bolts on the capstan motor is important. Each time the bolts are tightened in a particular procedure, they must be tightened in the same order and with the same torque. This allows the procedure to be repeated while keeping the motor in the exact same position.

b. The use of sharp scissors on the plastic shim stock is necessary to keep the edges from curling up.

   The plastic shim stock sizes are identifiable by the color coding.

Amber	.001 in
Red	.002 in
Green	.003 in
Tan	.004 in
Blue	.005 in
Transparent	.0075 in
Brown	.010 in

c. The use of a good quality tape is necessary for correct capstan alignment. A used or abused tape does not run true over the capstan, causing false readings during the capstan alignment procedure.

13. Cut one piece of each type of shim stock as indicated in Figure 6-36. Exact dimensions of shim stock are not critical; the main idea is to have a manageable size to use as a feeler gauge. The blunt point shown in Figure 6-36 also minimizes curling of the end that will be used.

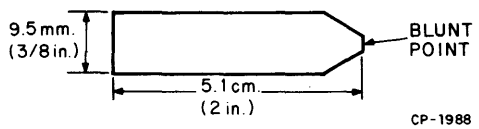


Figure 6-36 Capstan Motor Shim

14. Run tape forward from BOT for 5 seconds.

15. Using shim stock and penlight, determine the spacing (Y) between the inside edge of the tape and the floor of the left vacuum column (Figure 6-37). The method of measuring space Y is shown in Figure 6-38 and is described here in steps a, b, and c.

    a. Slide the shim stock under the inside edge of the tape at the slot between the top of the left column and the capstan.

    b. Shine the light on the full width of the tape while moving the shim stock back and forth; look for puckering.

    c. Measurement has been obtained when a piece of shim stock causes a small amount of friction yet no visible pucker when sliding back and forth.

NOTE

Value "Y" (obtained in step 15) must be equal to value "X" (obtained in step 6). The tolerance for value "Y" is ±.005 cm (±.002 in). In no case shall value "Y" be less than .0025 cm (.001 in). If it is, continue with the procedure to determine corrective action.

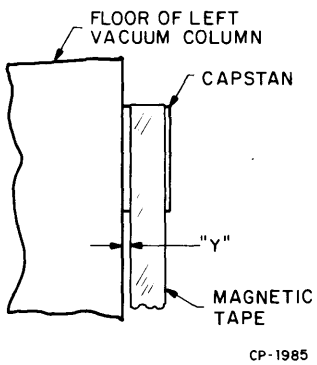


Figure 6-37 Gap (Y) from Tape to Floor of Left Column

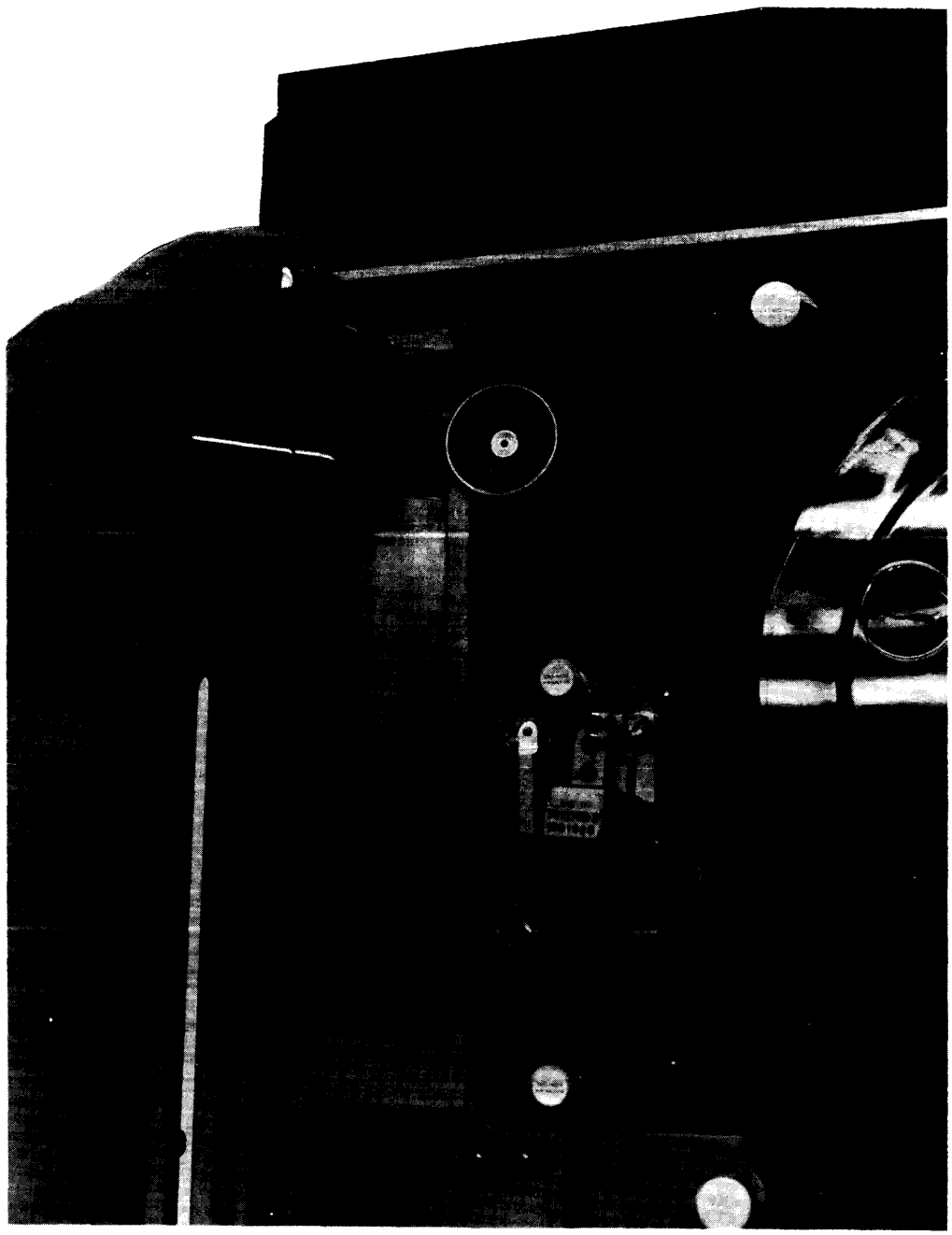


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Figure 6-38 Measurement of Tape Gap (Y) with Penlight and Shim

16. Run tape reverse for 5 seconds. Measure tape-to-column spacing to obtain value "Y." Value "Y" obtained in step 15 must equal value "Y" obtained in step 6, ±.001 in.

    a. Basically, the capstan motor must continually be shimmed, as described in step 12, until:

        - Value "Y" is no greater than value "X" plus .005 cm (.002 in) in forward or reverse.
        - Value "Y" is no less than value "X" less .005 cm (.002 in) in forward or reverse [less than .0025 cm (.001 in) in any case].
        - The difference between forward and reverse does not exceed .0025 cm (.001 in).

    b. Shimming is accomplished as follows:

        - If the tape is too close to the casting in forward and reverse: loosen motor mounting bolts and place a shim under the motor adjacent to the bolt at the 6 o'clock position, tighten bolts, and repeat steps 14, 15, and 16.
        - If the tape is too far away from the casting in both forward and reverse: loosen motor mounting bolts, place a shim under the motor adjacent to the bolt at the 12 o'clock position, tighten bolts, and repeat steps 14, 15, and 16.
        - If the tape is too close to casting in forward and too far away from casting in reverse: loosen motor mounting bolts, place a shim under the motor adjacent to the bolt at the 3 o'clock position, tighten bolts, and repeat steps 14, 15, and 16.
        - If the tape is too far away from casting in forward and too close to casting in reverse: loosen motor mounting bolts, place a shim under the motor adjacent to the bolt at the 9 o'clock position, tighten bolts, and repeat steps 14, 15, and 16.
        - If measurements meet the value "Y" criteria stated in step 16a, go to step 17.

    c. The following guidelines should be adhered to:

        - A .005 in shim is usually a good starting point, but almost any size shim (up to .010 in) may be necessary to accomplish the criteria stated in step 16a.
        - If a shim size greater than .010 in is called for, it is advisable to rotate the motor mounting 90 degrees and try again or change the motor.
        - In no case should there be a shim at the two ends of the same axis (i.e., 3 and 9 o'clock or 6 and 12 o'clock). If the formula in step 16b calls for a shim to be placed at 6 o'clock and there is already a shim at 12 o'clock, decrease the shim size at the 12 o'clock position.
        - It is quite normal to have one shim in each of the two axes. In fact, it is desirable, as this will make the procedure less subject to irregularities due to variations in bolt tightening sequences (a shim in the vertical axis will allow the motor to rock in the horizontal axis). For this reason, when a shimming session is started, place a shim of half the value in the horizontal axis if a shim is placed in the vertical axis due to the formula in step 16a (or vice versa); this is only a time-saving starting point, and both shims may need adjustment on reruns through steps 15 and 16.

- It is acceptable to use multiple shims under a given bolt to obtain the desired value (e.g., placing a .004 in and .005 in shim together to obtain .009 in).

- If steps 15 and 16 seem impossible to accomplish or if measurements taken in these steps are inconsistent, see step 19 for an explanation of capstan and tape phenomena.

- It should be noted that, while a guiding surface exists on the right side of the capstan (the head plate guides), none exists on the left side (left vacuum column). This will tend to make forward capstan steering look less severe than the reverse capstan steering. Therefore, small differences between forward and reverse are sometimes better corrected by shims in the vertical axis.

17. Mount a skew tape and adjust the mechanical skew per Paragraph 6.5.3.1.

18. With the skew tape mounted and scoping PACKET (E4-K1), evaluate capstan alignment as follows:

    a. Run the tape forward, looking at the PACKET signal on the scope. PACKET width must be less than 2.5 μs.

    b. While the tape is running forward, move the upper spring-loaded guide away from the tape. PACKET width should not increase more than 4 μs; take care not to touch the tape (Figure 6-39).

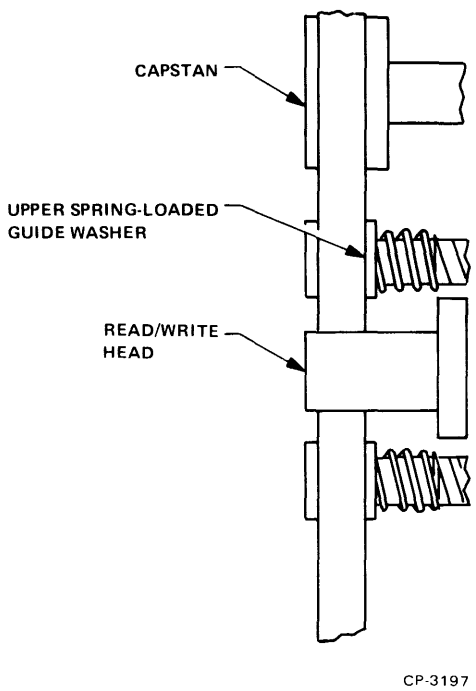


Figure 6-39 Upper Spring-Loaded Guide Location

c. While the tape is running forward, look at the tape interface to the upper fixed guide (use a penlight to reflect light off the tape surface); ensure that no puckering exists.

d. Run tape reverse, looking at the PACKET signal on the scope. PACKET width must be less than 3.5 μs.

e. While the tape is running reverse, move the upper spring-loaded guide washer away from the tape. PACKET width must not increase more than 4 μs.

f. While the tape is running reverse, look at the tape interface to the upper fixed guide; ensure that no puckering exists.

Corrective action:

a. If PACKET width increases by more than 4 μs in either forward or reverse when the spring guide is depressed, it should be assumed the tape is running too close to the casting in that direction of tape travel.

b. If tape is puckering on the guide in either forward or reverse or if the PACKET width is excessive in forward or reverse, yet does not increase when the upper spring guide is depressed, it should be assumed that the tape is running too far away from the casting in that direction of tape motion.

c. If neither a nor b exists, go to step 19.

d. If a or b exists, make final shimming corrections according to the procedure in step 16b.

NOTE

After all shimming is completed in this step, it will be necessary to verify that the criteria in step 16 (tape-to-column spacing) are still met.

19. Run tape forward. Look in the slot between the inside tape edge and the left vacuum column floor while the tape is moving forward. If room light is not adequate, shine the penlight through from the inside of the vacuum column (Figure 6-40).

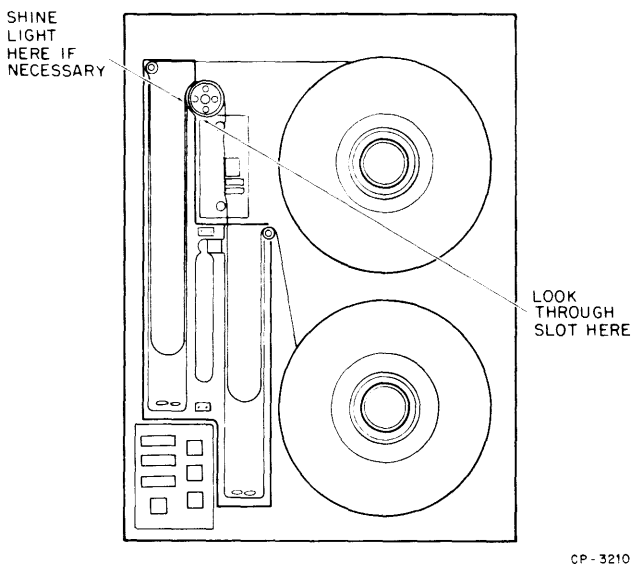
    There should be a constant space (width of light) in this slot as the tape moves forward. Periodic width change at a very low frequency (less than one per second) is probably due to tape defects; do not worry about these, unless they are very repetitive and cause wide excursions. Higher frequency width changes (5 to 10 times per second) are usually caused by a bent capstan. If this occurs, it will be necessary to replace the capstan and recheck the tape-to-column spacing with shim shock feeler gauges.

20. Run tape in reverse. Check the slot width using the criteria in step 19.

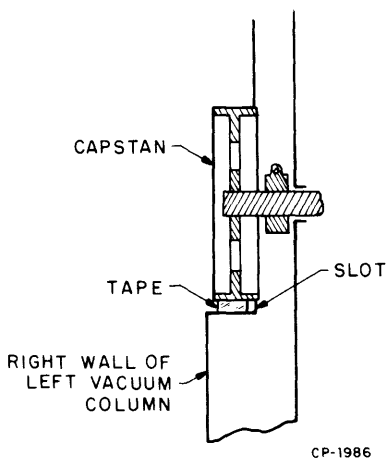
21. Replace the vacuum column door. Run skew tape forward; ensure that the PACKET width does not exceed 2.5 μs. Run tape reverse; ensure that the PACKET width does not exceed .5 μs. If either criterion fails, suspect a roller guide adjustment problem.

22. Now perform the tracking check as outlined in Paragraph 6.4.4.3.

23. To return the tape transport to good working condition now that the tape path has been aligned, it may be necessary to perform a number of electrical checks and adjustments (depending on which parts have been replaced in this alignment procedure). Figure 6-41 is a flowchart, which indicates checks that should be done and the order in which they should be accomplished.



A. Front View



B. Right Side View

Figure 6-40 Capstan Wobble Check

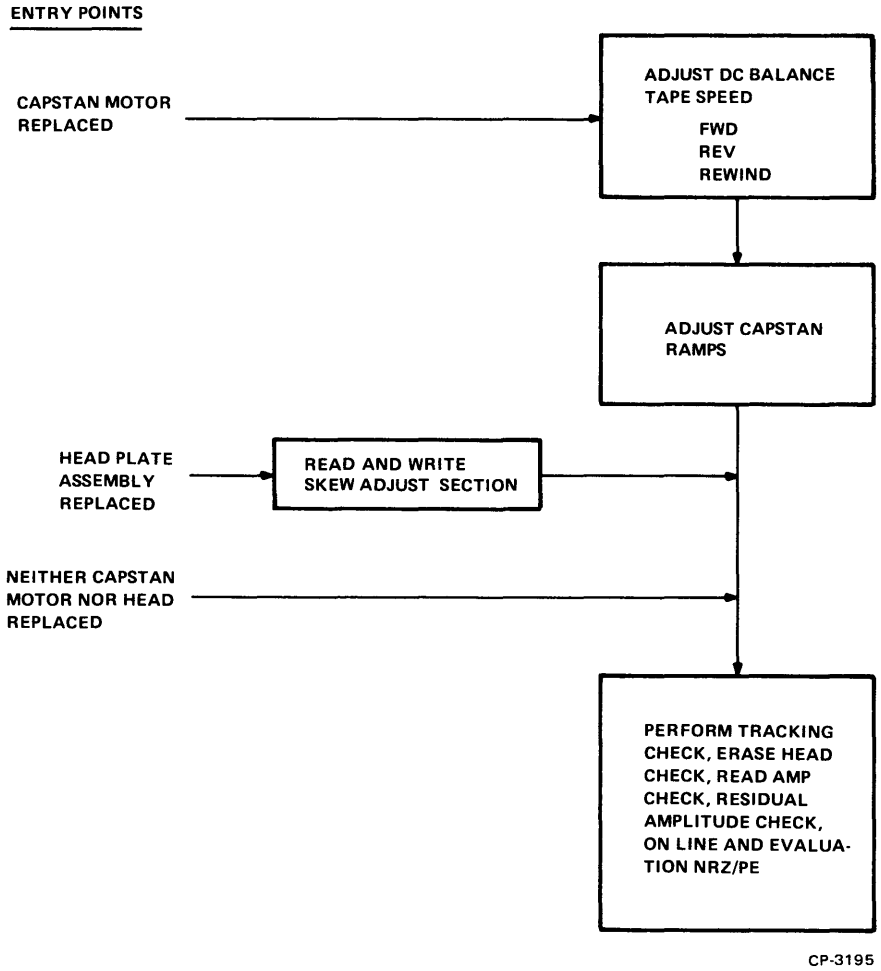


Figure 6-41 Summary, Capstan Alignment Flow Diagram

6.5.2 Snap-Lock Hub Adjustment

Proceed as follows to adjust the supply reel hub gripping force:

1. Flip the snap-lock lever up to expose an index screw.
2. Remove the index screw.
3. While holding the inner hub half, rotate the outer hub half to perform the adjustment. A clockwise rotation will increase the gripping force, whereas a counterclockwise rotation will decrease it. Mount a tape and ensure that the lock lever closes smoothly and holds the reel securely.
4. When that point is reached, locate the closest index hole and replace and tighten the index screw.

6.5.3 Skew Adjustments

The deskewing procedures must be performed whenever a head plate assembly is replaced. All skew adjustments are listed and defined in this section.

6.5.3.1 Mechanical Azimuth (Read Skew) Adjustment – Proceed as follows to perform the Read Skew Adjustment:

1. Clean the tape transport and load a skew tape.

2. Set up the oscilloscope as follows:

Horizontal:	2 μs/cm
Vertical:	0.1 V/cm (channels 1 and 2)
Vertical Coupling:	ac
Triggering:	Normal Positive Channel 1
Mode:	Chopped

   Place the channel 1 probe to pin A04L1 (channel 1) and the channel 2 probe to pin B04B1 (channel 2).

3. Initiate a forward motion command from the off-line maintenance switches, and put the two channels in close proximity, as shown in Figure 6-42. On the head plate, just above the recording head, is a Phillips head screw. Adjust this screw so that the peaks of channel 1 and 2 line up in the vertical axis (Y). After performing this course adjustment, move the channel 2 probe to pin F04R1 (channel 9) and fine tune the adjustment screw so that the peaks line up.

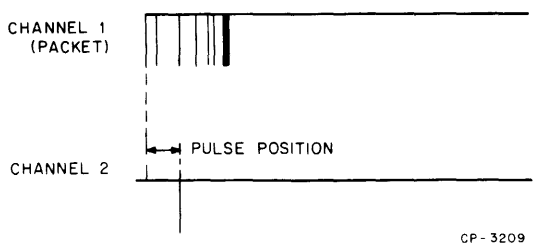


Figure 6-42 Measurement of Pulse Positions Relative to PACKET

4. Now initiate a reverse motion command and observe the proximity of the channel 1 peak versus the channel 9 peak. The two peaks should not be more than 2.5 μs apart. If they are, investigate a possible tape path misalignment.

5. Now perform a PACKET analysis. Place the channel 1 probe on pin E04K1. This is the PACKET signal, a logical OR of all nine tracks. Readjust the oscilloscope as follows:

Horizontal:	0.5 μs/cm
Vertical (channel 1):	1 V/cm (dc coupling)

6. Initiate a forward motion command and observe an oscilloscope waveform similar to Figure 6-42. PACKET should be no more than 2.5 μs from the beginning of the trace to the leading edge of the latest pulse in the composite waveform. If a wider waveform is observed, the tape path may have to be realigned or the head may be badly worn.

NOTE
An occasional jump in PACKET width of 1 μs is allowable (usually due to a tape defect); however, this should not occur more often than once per second.

7. Now initiate a reverse motion command and observe PACKET. PACKET should not be wider than 3.5 μs. If it is, tape path realignment may be necessary.

6.5.3.2 Write Skew Adjustments – Proceed as follows to perform the Write Skew adjustment:

NOTE
This adjustment must be preceded by the Read Skew adjustment (Paragraph 6.5.3.1) and is required when replacing a head assembly or when excessive head pole wear is suspected.

1. Set up the oscilloscope as follows:

Horizontal:	0.5 μs/cm
Vertical:	1 V/cm (channels 1 and 2)
Triggering:	Normal Positive Channel 1
Mode:	Chopped

Place the channel 1 probe to pin E04K1 (PACKET) and the channel 2 probe to pin A04J1 (track 1).

2. Photocopy Table 6-4, or prepare a similar one.

3. Load a skew tape on the transport and initiate a forward motion command from the maintenance switches.

4. Synchronize the oscilloscope to the leading edge of PACKET and look at channel 2. Channel 2 is now displaying the position of track 1 within PACKET. Determine the time displacement between the leading edge of PACKET and the leading edge of track 1 pulse, and record it on the first line of the skew tape bit position column of Table 6-4. Continue tabulating the relative bit positions for tracks 2 through 9.

Table 6-4 TE16 PACKET Analysis and Write Deskew Worksheet

Track No.	Channel 9/7	Pin No.	Skew Tape Read Bit Position	Work Tape Uncorrected Write Bit Position
1	2/B	A04J1		
2	0/*	A04H1		
3	4/8	B04N1		
4	P/C	B04L1		
5	5/4	C04U1		
6	6/2	C04S1		
7	7/1	E04H1		
8	1/*	E04F1		
9	3/A	F04M1		

*9-track only

5. After tabulating the data for all nine tracks, run the skew tape in reverse to BOT and remove it.

6. Remove power from the transport. Remove all nine wire wraps that jumper the record pulses (SK CLK A through D) to the Write Deskew Buffer inputs (SK CLK 0 through 7 plus P). For backplane pin numbers, refer to Engineering Drawing D-CS-M8916-0-1, sheets 1 and 2 in the customer print set. Now, with termi-points or temporary wire wraps, jumper the SK CLK B output to all nine buffer inputs. This is to allow all nine tracks to be written at the same time for measurement purposes.

7. Plug the TFG module (M8912) into slots AB03, configured as follows:

   S5-1 through 8 and 10 - OFF
   S5-9 - ON
   S6-1 through 8 - OFF
   SS RD, WRT and SS WRT - DOWN

8. Apply power and load a work tape to BOT. Raise and lower the SS RD switch to load an all "1s" data pattern. Place the transport off-line, raise the WRT switch, and initiate forward motion from the maintenance switches. Allow the transport to perform this continuous write operation for 5 minutes. Put the WRT switch down and rewind the tape.

9. Now initiate a forward motion command from the maintenance switches and read back what was just written in step 8. Again, monitor all nine read channel test points and record the pulse positions under the column labeled "Uncorrected Write Bit Position."

CAUTION

While performing step 9, do not allow the tape to go past the point where the write operation in step 8 was terminated, or incorrect data may be gathered.

10. Now, for each track, compute the difference between the position of that track when reading a skew tape (tape A) and its position when reading a tape (tape B) just written by the head being deskewed.

11. If the pulse generated by tape B occurs more than 0.5 μs later than that generated by tape A, connect the Deskew Buffer input for that track to the record pulse labeled SK CLK A. If the pulse generated by tape B occurs less than 0.5 μs later than that generated by tape A, leave the write clock for that track on SL CLK B.

12. If any pulse generated by tape B occurs more than 1.5 μs later than that generated by tape A, perform the following steps:

    a. Disconnect all tracks connected to SK CLK B, and reconnect them to SK CLK D.

    b. Disconnect all tracks connected to SK CLK A, and reconnect them to SK CLK C.

    c. Connect all tracks where the difference is between 1.5 and 2.5 μs to SK CLK B.

    d. Connect all tracks where the difference is greater than 2.5 μs to SK CLK A.

    e. If any track shows greater than 4.0 μs difference between tape A and tape B, the head assembly should be replaced, as it is out of tolerance.

NOTE

Some early TM02s contain M8903 modules that generate NRZI Tape Mark errors if SK CLK C and D are used. If these skew clocks are used and if NRZI Tape Mark errors are detected, then M8903 ECO No. 7 must be installed.

13. Now replace all the temporary jumpers with permanent wire wraps.

14. Rewrite tape B using the all "1s" pattern, rewind the tape, and initiate a forward command. Examine PACKET and verify that the corrected write time does not exceed the value measured with a skew tape in Paragraph 6.5.3.1, step 6, by more than 0.5 μs. If it does, a further refinement of the write deskew jumpers may be necessary, in which case, go back to step 9 and proceed to the end of this paragraph again.

6.5.4 Read Amplitude Adjustments

The following procedure should be followed to adjust the read amplitudes. This should be performed after replacing the read amplifier or head assembly:

1. Clean the entire tape path and load a good quality work tape.

NOTE

The brand of tape used for this adjustment should be typical of that used in the operating environment where the transport resides. Tape output amplitudes vary among manufacturers by as much as 35 percent. Also, ensure that tape speeds are set properly (Paragraph 6.5.6).

2. Set up the oscilloscope as follows:

Horizontal:	2 ms/cm
Vertical:	2V/cm (channel 1)
Triggering:	Normal Channel 1 triggered

Place the channel 1 probe on pin A04L1.

3. Configure the TFG module switches as follows:

S4-1 through 8 - ON
S4-9, 10 - OFF
S5-1 through 8 - OFF
S5-9, 10 - ON
S6-1 through 8 - OFF
SS RD and WRT - DOWN

4. Place SS WRT up and observe the oscilloscope trace. The amplitude of each channel should be adjusted to 12 V p-p. Refer to Figure 6-43 for adjustment potentiometer locations on the G066 Read Amplifier. Proceed in this manner through all nine channels. Table 6-5 lists the various test point locations.

6.5.5 Regulated Power Supply Voltages
Five potentiometers, located on the power supply regulator board, are used to adjust the following voltages: +5, -6.4, +12, +12 (NRZI), and +5 (PE). The remaining voltages (+16, -16, +17, and -17) are not adjustable. A small insulated screwdriver or trimpot tool is required to make the adjustments. Clockwise rotation of any of the potentiometers increases voltage. Refer to Figure 6-44 for the potentiometer locations. Use a calibrated voltmeter, preferably a DVM. All measurements are referenced to ground at pin C04C2.

CAUTION
Do not adjust voltages beyond their 105 percent rating, and adjust slowly to avoid overvoltage crowbar.

Remove power from the tape transport. Then remove the regulator board cover; reapply power and proceed as follows:

6.5.5.1 +5 V Adjustment - Attach the DVM probe to backplane pin D01A2 (red wire) and adjust R59 for +5.25 ± 0.05 V.

6.5.5.2 +12 V Adjustment - Attach the DVM probe to backplane pin A04V1 (yellow wire) and adjust R37 for +12.05 ± 0.05 V.

6.5.5.3 -6.4 V Adjustment - Attach the DVM probe to backplane pin C04N2 (green wire), and adjust R44 for -6.35 ± 0.05 V.

6.5.5.4 +12 V (NRZI) Adjustment - Attach the DVM probe to backplane pin C02J2 (orange wire) and adjust R26 for +11.875 ± 0.125 V.

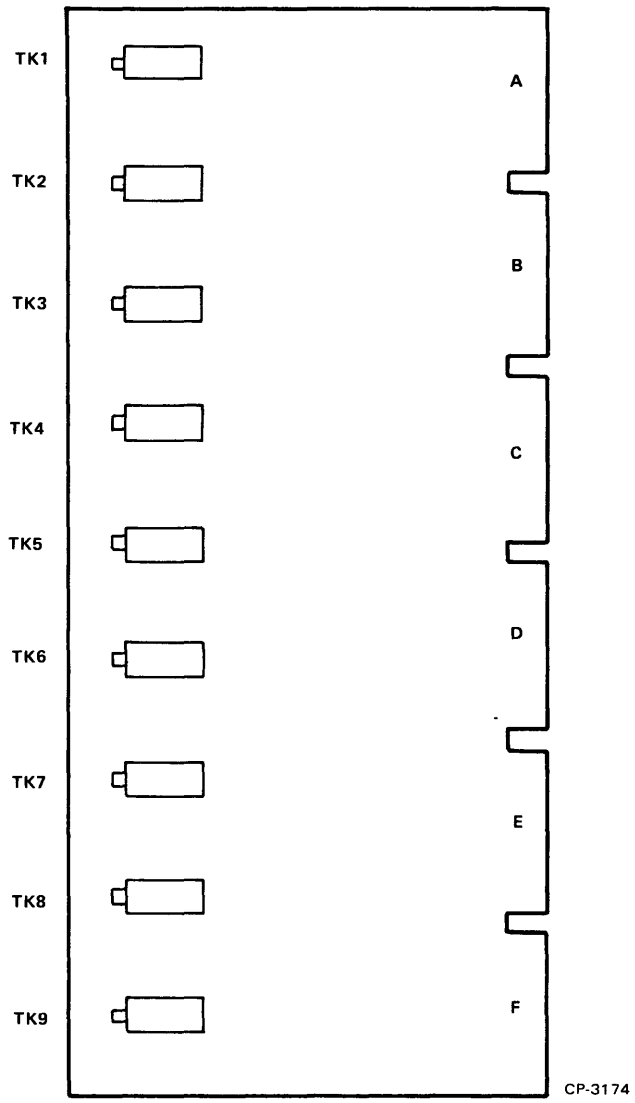
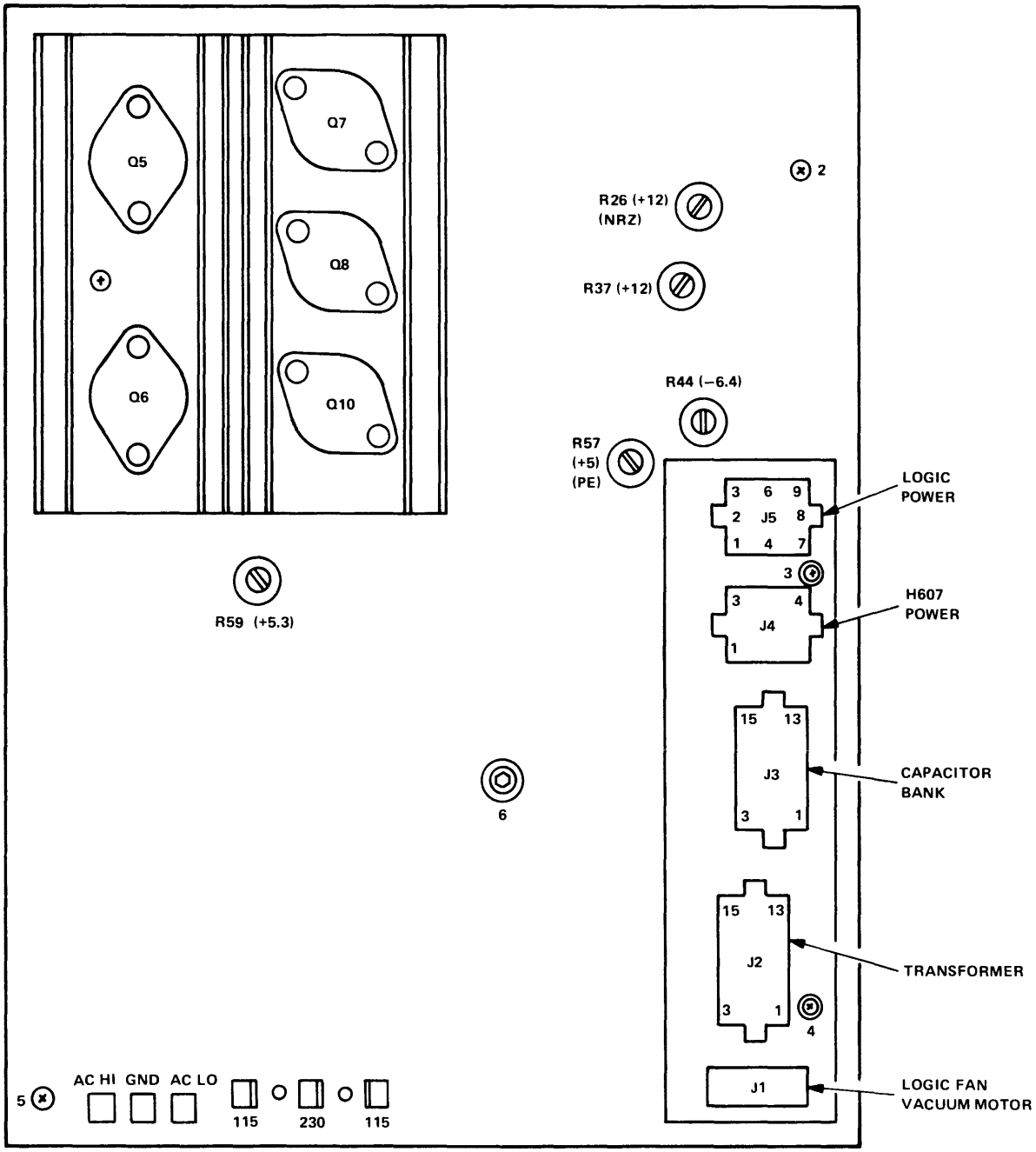


Figure 6-43 G066 Adjustment Potentiometers

Table 6-5 Read Amplifier Test Points

Track No.	Channel 9/7	Pin No.
1	2/B	A04L1
2	0/*	B04B1
3	4/8	B04M1
4	P/C	C04K1
5	5/4	C04L1
6	6/2	D04P1
7	7/1	D04R1
8	1/*	F04P1
9	3/A	F04R1

*9-track only



NOTES:

1) 1 - 5 represent 5 Phillips head screws.
2) 6 represent Allen screw - must be secured very tightly, or damage to the power supply may result.

CP-3196

Figure 6-44 TE16 Power Supply Regulator Board

6.5.5.5 +5 V (PE) Adjustment (TE16 only) - Leave the DVM probe at pin C02J2 and ground pin C03B1 (PES L). Adjust R57 for +5.6 ± 0.1 Vdc.

NOTE
Paragraphs 6.5.5.4 and 6.5.5.5 are interactive and must be performed in that sequence. Paragraph 6.5.5.5 may be ignored for TE10W/N models.

6.5.6 Capstan Balance and Speed

Adjustments to the capstan servo preamp are made as follows. Refer to Figure 6-45 and Table 6-6 for the various adjustment locations.

6.5.6.1 Balance

1. Turn power OFF. Disconnect the erase/write head cable from the M8916 LAW module. Loosen the two screws in the upper and lower right hand corners of the H607 daughter board and swing it away from the H607 mother board.

2. Turn power ON and load a master skew alignment tape. Position the tape at BOT.

3. Set the oscilloscope's vertical gain to 50 mV/cm and reference mother board TP 13. Connect the probe ground to TP 12.

4. Approximately 50 mV of ac ripple will be seen on the oscilloscope. This ripple should be centered around 0 Vdc. If necessary, adjust R117 on the mother board to obtain 0.0 ± 0.04 Vdc.

6.5.6.2 Forward Tape Speed - Check forward tape speed as follows:

1. Set the oscilloscope:

Horizontal:	10 μs/cm
Vertical:	2 V/cm (channel 1)
Triggering:	Normal
	Negative slope
	Channel 1 triggered

   Place the channel 1 probe to pin B04L1 (track 5). If working on a 7-channel TE10W/N transport, place the probe on pin A04H1 (track 8).

2. Initiate forward tape motion with the maintenance switches. Check that the negative pulses are 55 to 57 μs apart (Figure 6-8). If the pulses are not within this specification, adjust potentiometer R91 on the mother board so the spacing is 56 μs.

6.5.6.3 Reverse Tape Speed - Initiate reverse tape motion with the maintenance switches. Check that the negative pulses are 55 to 57 μs apart. If they are not within this specification, adjust potentiometer R87 on the mother board so the spacing is 56 μs.

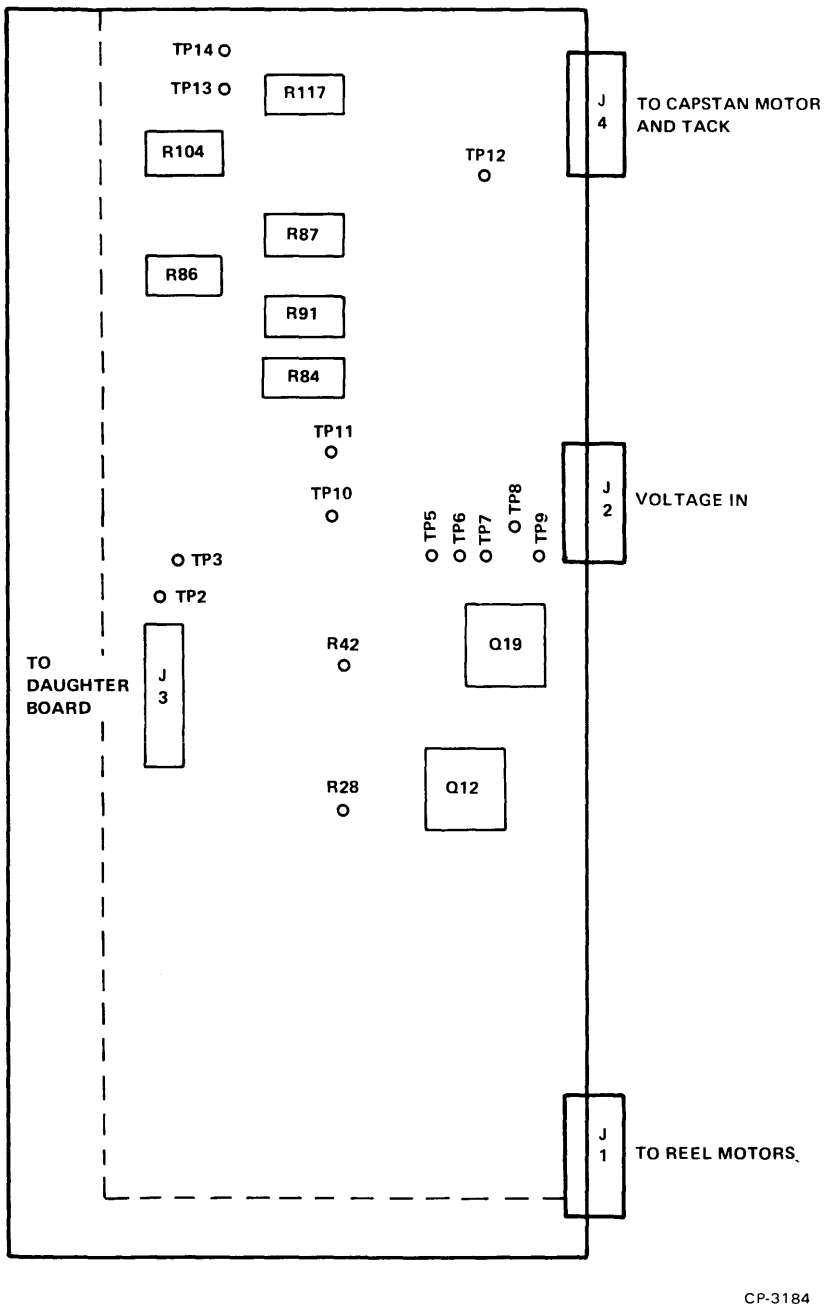


Figure 6-45 H607 Mother Board: Adjustments and Test Points

Table 6-6 H607 Mother Board Test Points

Test Point No.	Signal
1	Not used
2	LOWER BRAKE OUT
3	UPPER BRAKE OUT
4	Not used
5	REWIND CAP H
6	REV/REW H
7	FOR H
8	+8 V
9	-8 V
10	UPPER BRAKE OUT H
11	LOWER BRAKE OUT H
12	GROUND
13	SERVO SIGNAL
14	CAPSTAN BALANCE

6.5.6.4 Rewind Tape Speed

1. Remove the master skew tape and load a scratch tape on the transport. Reconnect the erase/write cable at the M8916.

2. Configure the TFG module for an 800 bits/in write of all "1" bits on tape.

3. After ensuring that there is adequate tape on the take up reel, run the transport in RWD. Now the negative pulses should be 16.6 μs apart. If they are not, adjust potentiometer R84 on the mother board so that the spacing is 16.6 μs.

6.5.7 Capstan Current (Acceleration Ramps)

Adjust the FWD/REV acceleration ramps as follows:

1. Set the switches of the TFG (M8912) module as follows:

   SS RD, SS WRT, and WRT - DOWN
   S4-9 - OFF

2. Set the oscilloscope:

Horizontal:	2 ms/cm
Vertical:	0.2 V/cm (channel 1)
Triggering:	External sync Negative Slope Normal

   Place the channel 1 probe to P4-7 of the H607 mother board (signal TACH -V). Also, connect the probe ground to TP 12 and the external trigger probe to pin A03S1.

3. Load a scratch tape on the transport and position the tape to BOT. The tape must have a write enable ring.

4. Initiate forward motion and place the SS RD switch (M8912) up. Synchronize the oscilloscope, and a waveform similar to that in Figure 6-46 should appear. The duration of the negative-going slope should be 7 to 8 ms. If necessary, adjust R104 (-CUR) on the H607 mother board to obtain this period.

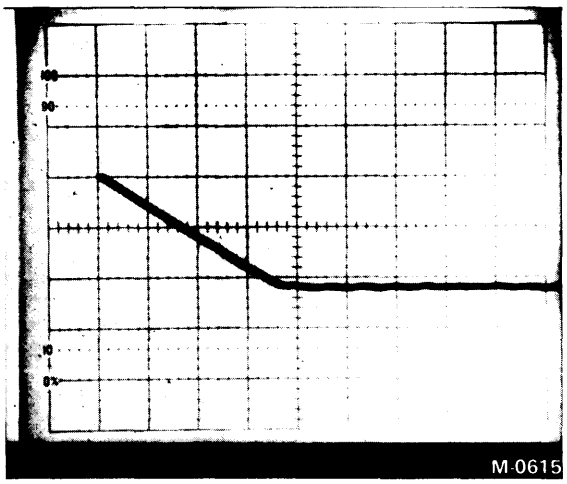


Figure 6-46 Forward Acceleration Ramp Waveform

5. Now initiate reverse tape motion, and set the oscilloscope trigger level to positive. Synchronize the oscilloscope, and a waveform similar to that in Figure 6-47 should appear. The duration of the positive slope should be 7 to 8 ms. If necessary, adjust R86 (+CUR) on the H607 mother board to obtain this period.

NOTE

Deceleration times are not adjustable and will be somewhat shorter than acceleration times.

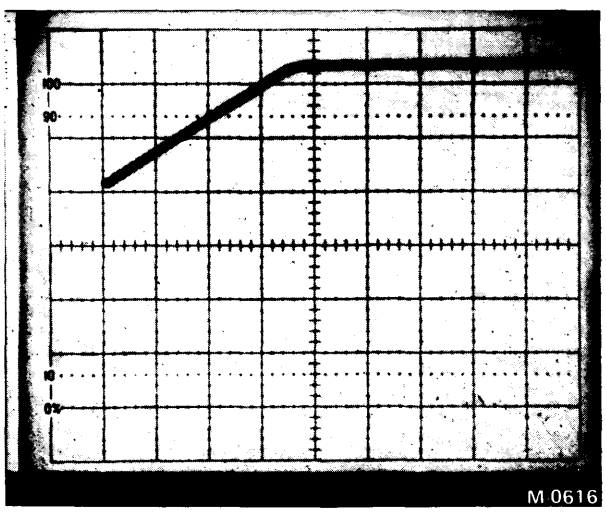


Figure 6-47 Reverse Acceleration Ramp Waveform

6.5.8 Tape Unload Adjustment

Adjust the tape unload circuitry as follows:

1. With power OFF, extend the transport on its slides and swing the H607 daughter board away from the mother board.

2. Ensure that the capstan wheel is clean. This is extremely important, as the capstan wheel is the velocity feedback element in the unload circuitry.

3. Load a scratch tape with a standard length tape leader 4.9 ± .6 m or 16 ± 2 ft on the transport.

4. With the transport OFF LINE, press UNLOAD. The entire unload operation should take no less than 5 seconds and no more than 7 seconds to complete. If the transport unloads within this time frame, leave it alone. If not, proceed with step 5.

5. Turn potentiometers R28 and R42 on the H607 mother board fully counterclockwise. (For location, refer to Figure 6-45.) Turn potentiometer R49 on the H607 daughter board to its mid position.

6. Now perform the unload operation. If the tape unloads too quickly (i.e., less than 5 seconds), turn R28 one-quarter turn clockwise. This reduces the level of voltage and, therefore, torque applied to the lower motor. Continue adjusting R28 until the unload time parameter is met.

7. If the tape unloads too slowly (i.e., more than 7 seconds have elapsed, and there is still tape to be taken up), turn R42 one-quarter turn clockwise. This increases the current applied to the upper motor. Continue adjusting R42 until the unload time parameter is met. If R42 is adjusted fully clockwise and the unload is still too slow, adjust R49 on the daughter board fully clockwise.

6.5.9 Reel Motor Brake Adjustments

Proceed as follows to adjust the reel motor brakes:

1. With power OFF, loosen the clamp on the motor shaft with an Allen wrench (Figure 6-48).

2. Insert a .254 mm (.010 in) feeler gauge between the stator and the rotor. When clearance is correct, tighten the Allen screw on the clamp.

3. With the .254 mm (.010 in) feeler gauge inserted between the stator and the rotor, rotate the reel motor manually from the front of the unit to see that the brake is spaced uniformly all around. If necessary, rotate the rotor disk at 120-degree intervals to determine the best position for uniform separation. An excessively high or low spot is cause for replacing the brake assembly.

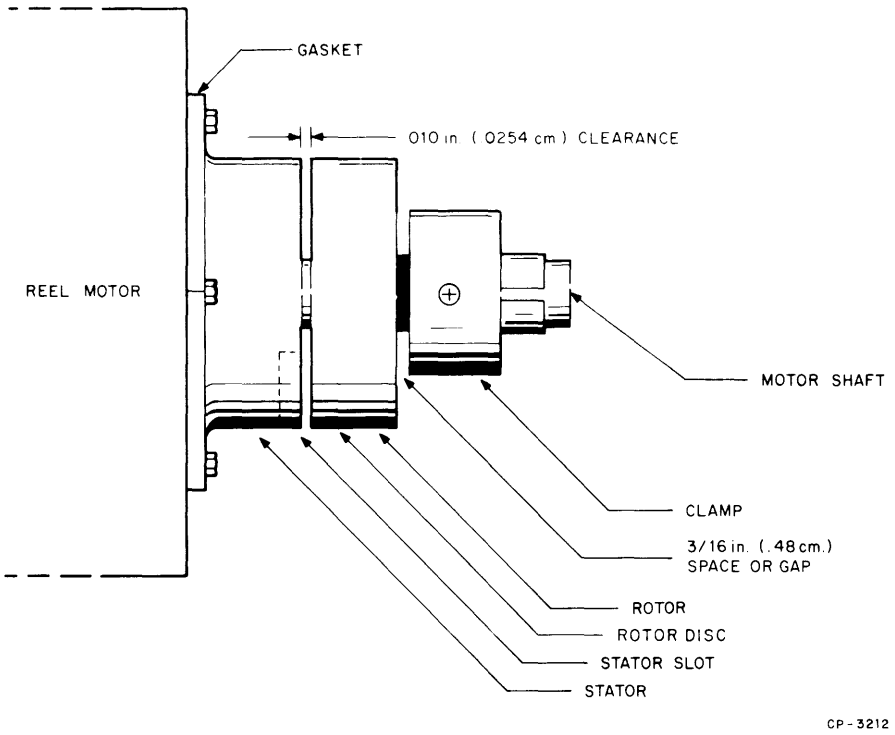


Figure 6-48 Brake Assembly

6.5.10 Read/Write Interlock Assembly Adjustment

To perform the following adjustment, refer to Figure 6-49.

1. Loosen the two screws securing the switch to the bracket just enough to allow the switch to be moved.

2. Loosen the locknut and adjust the screw several turns (detail B, Figure 6-49).

3. Insert the small end of the setting gauge (No. 29-18610) in front of the roll pin through the bottom of the bracket so that it fits between the pin and bracket body edge. Tighten the adjusting screw until the switch just actuates.

4. Tighten the two screws, securing the switch to the bracket and the lock adjusting screw using the locknut.

5. Loosen the two solenoid mounting screws on the left of the interlock assembly (Figure 6-49A).

6. Insert the large end of the setting gauge in front of the roll pin as described in step 3. Push the solenoid body forward until the plunger bottoms out, then tighten the solenoid mounting screws, keeping the solenoid body parallel to the upper edge of the bracket.

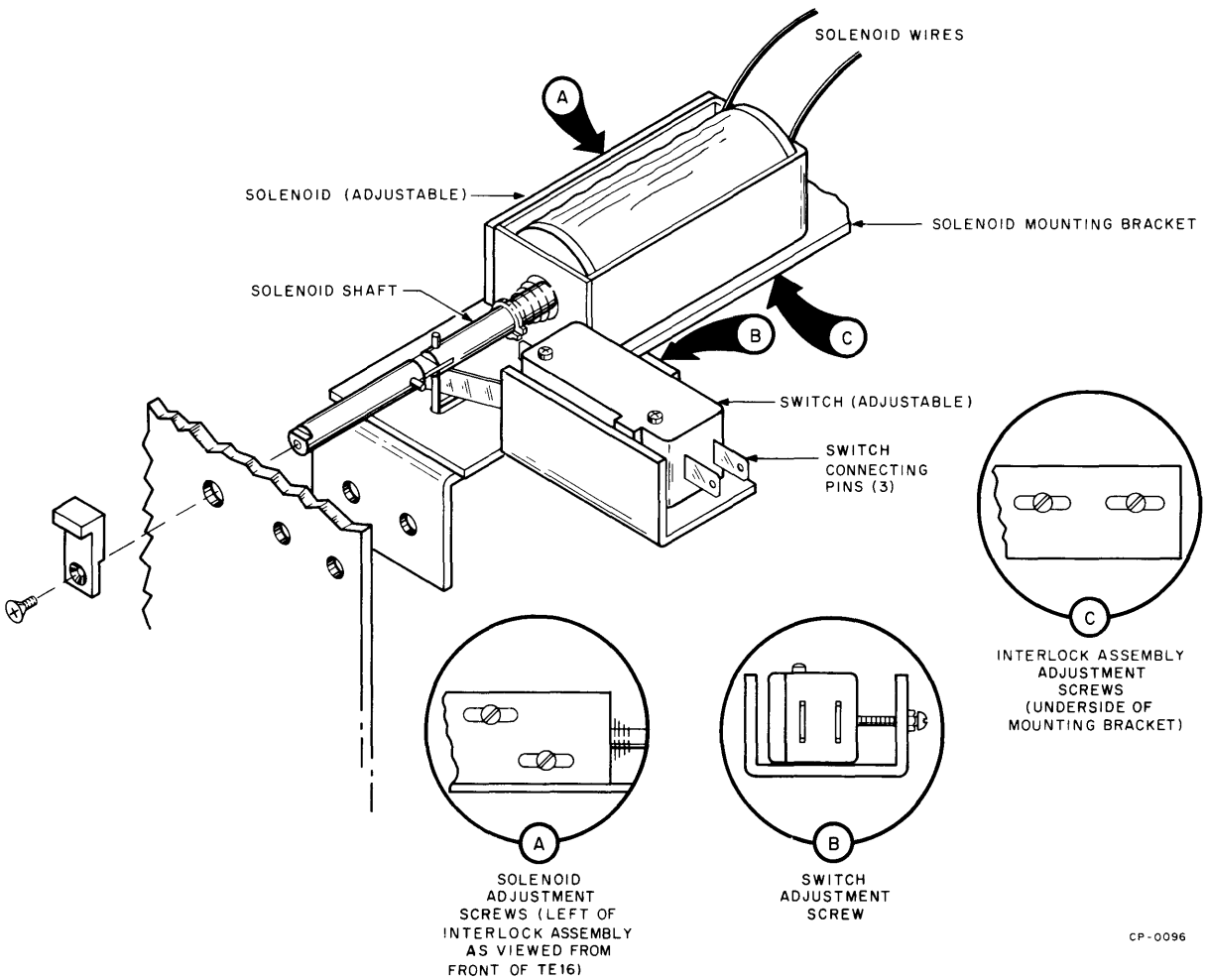


Figure 6-49 Read/Write Interlock Assembly

7. Loosen the bottom screws, securing the interlock assembly to the mounting bracket (Figure 6-49C).

8. Insert the ring gauge (No. 29-18608) onto the reel, lock it, and spin the reel to check for even rotation.

9. Push the interlock assembly forward until the shaft bottoms in the solenoid and the small spring is fully depressed.

10. Tighten the screws, securing the assembly to the bracket, remove the ring gauge, and check for free movement of the solenoid shaft in the casting.

6.5.11 Vacuum Motor Belt Tension Adjustment

Perform the vacuum belt tension adjustment as follows:

1. Position the belt tension gauge as shown in Figure 6-50; push against the knob at the end of the spring until the third tab on the gauge just touches the belt.

2. Read the tension from the scale just under the spring; adjust the belt tension adjustment screw for 4.1 ± .9 kg (9 ± 2 lb) of tension.

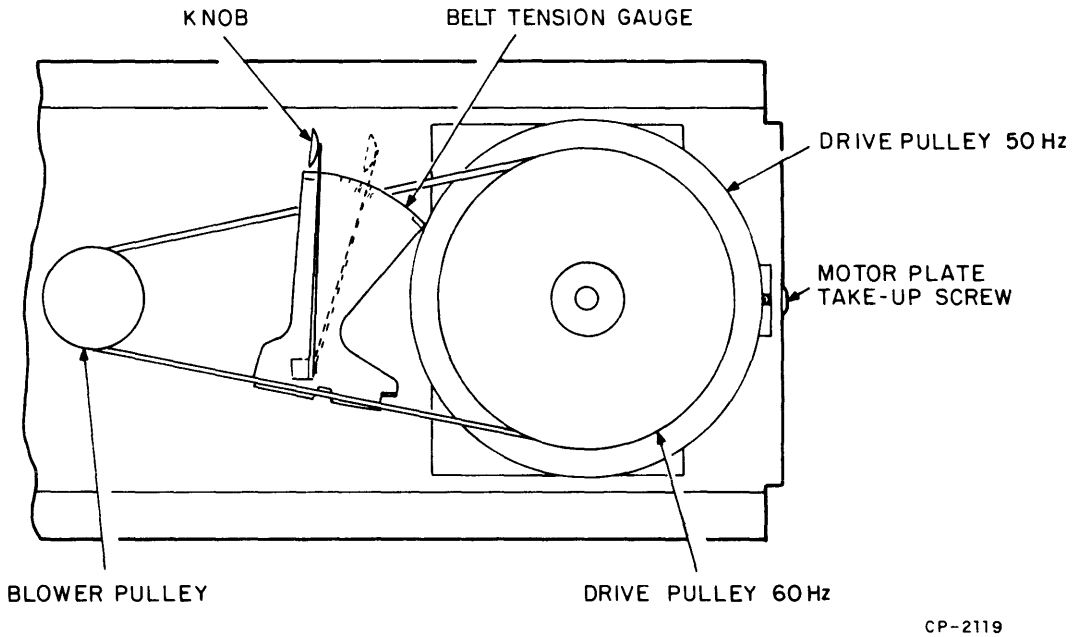


Figure 6-50 Belt Tension Gauge

6.5.12 Vacuum Motor Pulley Height Adustment

To adjust the pulley height when performing a frequency conversion, proceed as follows:

1. Remove the black anodized pulley from the motor shaft by removing the set screw holding it in place.

2. Inspect the set screw for stripped threads or a damaged tip; replace the set screw if it appears damaged.

3. Inspect the motor mounting plate, which should have an open set of four motor-mount holes. Remove the four socket-head screws holding the motor in place, and remount them in the open set of holes, as shown in Figure 6-51.

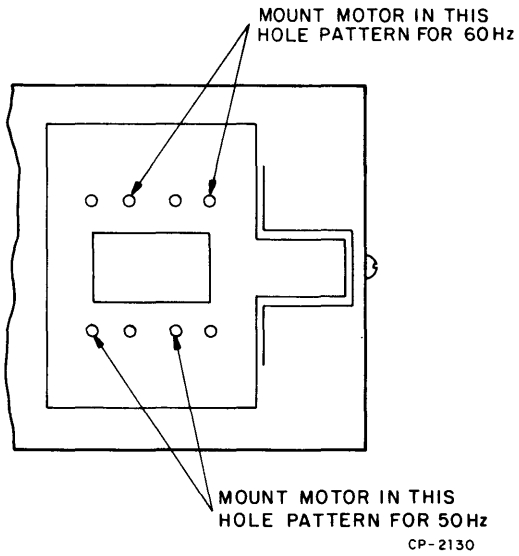


Figure 6-51 Motor-Mounting Holes for 50/60 Hz Operation

4. Replace the pulley; use the pulley height gauge (No. 74-16187) to set the pulley height—2.08 cm (0.82 in) for 50 Hz and 1.32 cm (0.52 in) for 60 Hz.

5. Ensure that the set screw rests on the flat part of the motor shaft. Retighten the set screw.

6. Now perform the belt tension adjustment (Paragraph 6.5.11).

6.5.13 BOT/EOT Sensor Alignment

Perform the BOT/EOT sensor alignment as follows (reference Figure 6-52):

1. Remove power from the transport.

2. Attach one end of a 4.7k ohm resistor to backplane pin B04E1 (-6 V). Use a Termi-point to hold the resistor on the pin.

3. Attach the negative probe of a DVM to the -6 V end of the resistor and the positive probe to the free end of the resistor.

4. Apply power to the transport and load a tape to BOT (assuming that the sensor has been aligned roughly enough to sense BOT).

5. Remove the orange BOT sense lead from pin C02D1, and attach it to the free end of the resistor.

6. Loosen the screw holding the BOT sensor, and rotate the sensor until the meter reads maximum. Tighten the sensor screw and check to make sure the DVM reading has not changed.

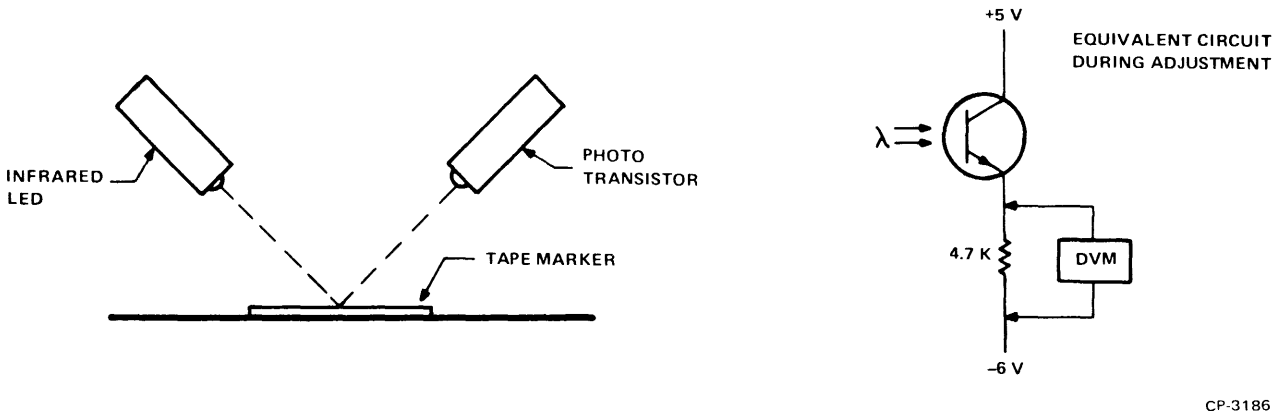


Figure 6-52 EOT/BOT Sensor Alignment

7. Verify that the DVM reading is greater than 2.5 V. If it is not, make sure that the sensor lenses are clean and that the BOT marker on the tape is aligned properly and is new and shiny. If these items are all right, and the DVM reading is still not greater than 2.5 V, then the sensor must be replaced.

8. Next, move the tape forward, using the maintenance panel controls. As soon as the marker leaves the sensor area, verify that the DVM reading drops to less than 0.5 V. If it does not, replace the sensor.

9. When the tape reaches EOT, replace the orange wire on pin C02D1 and remove the brown wire from pin C02D2. Attach the brown wire to the resistor.

10. Verify that the DVM reading is at least 2.5 V. If it is not, adjust the sensor to 2.5 V and recheck the BOT reading. If the sensor cannot be adjusted to greater than 2.5 V output at both BOT and EOT, replace the sensor.

11. With the orange wire on pin C02D1 and the brown wire on the resistor, rewind tape to BOT. The DVM must now read less than 0.5 V. If it does not, replace the sensor.

12. Replace the brown wire on pin C02D2, and remove the resistor and DVM.

6.6 REMOVAL AND REPLACEMENT PROCEDURES

This section outlines the removal and replacement procedures for the TE16 transport component assemblies. The major assemblies referenced throughout this section are shown in Figure 6-1. Also, Table 6-1 lists the special tools and equipment required for performing these proceedings.

NOTE

The capstan, capstan motor, roller guides, and head plate directly affect the path of the tape as it moves through the tape transport. If any one of these items requires replacement, an entire tape path alignment is necessary. Refer to Paragraph 6.5.1 for the tape path alignment procedure.

6.6.1 File Reel Snap-Lock Hub

Assemble the snap-lock hub as follows:

1. With the reel motor removed from the transport casting, assemble the adapter to the motor shaft by sliding it on and lining up the two set screws with the two flats on the shaft. Use the opposite end of the spanner wrench to set the spacing between the adapter and the motor mounting surface. Once the spacing (.198 mm or .078 in) has been established, tighten the two set screws (Figure 6-53).

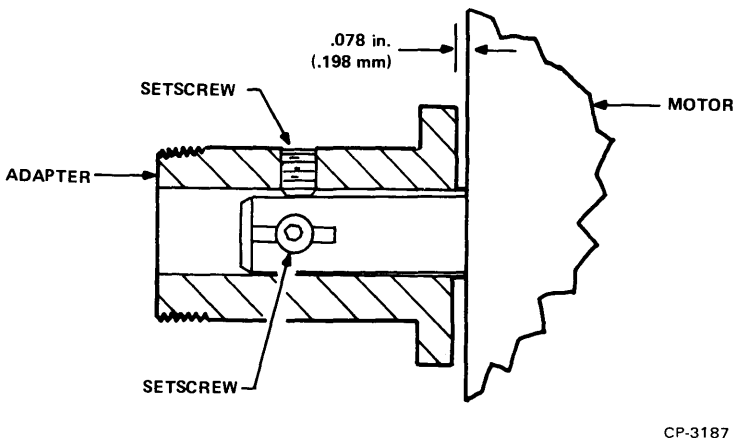


Figure 6-53 Reel Motor Adapter

2. Position the motor spacer on the motor mounting surface, making sure to align the mounting holes of the spacer (outer system of clearance holes) with the mounting holes of the motor. The inner system of holes should line up with the motor cooling holes (see Figure 6-54).

3. Install the motor and spacer on the deckplate using four 10-32 × 1-1/4 socket head cap screws and four No. 10 split washers. The motor and spacer cooling holes will line up with the open vacuum slot on the deckplate.

4. Slide four .010 circular metal shims onto the adapter.

5. Place the Woodruf key into the keyway in the adapter, and slide the inner hub onto the adapter, lining up the keyway.

6. Thread the large 1-3/8 nut onto the adapter and tighten it, using a 1-3/8 socket and rachet or breaker bar, while holding the inner hub in place with the spanner wrench (Figure 6-55).

7. Lightly lubricate the "O" ring chamfer on both outer and inner hub pieces with silicone grease.

8. Place the "O" ring over the outer hub assembly.

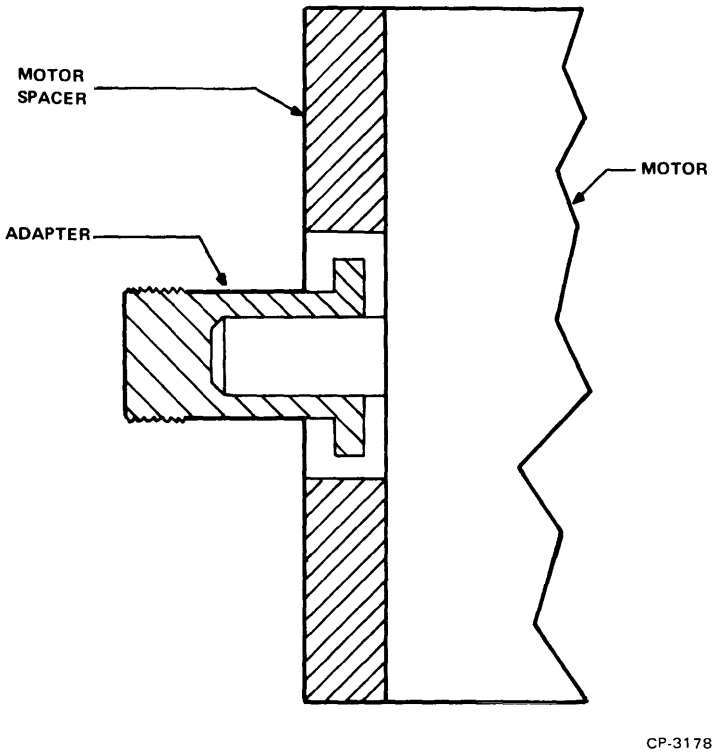


Figure 6-54 Motor Spacer Positioning

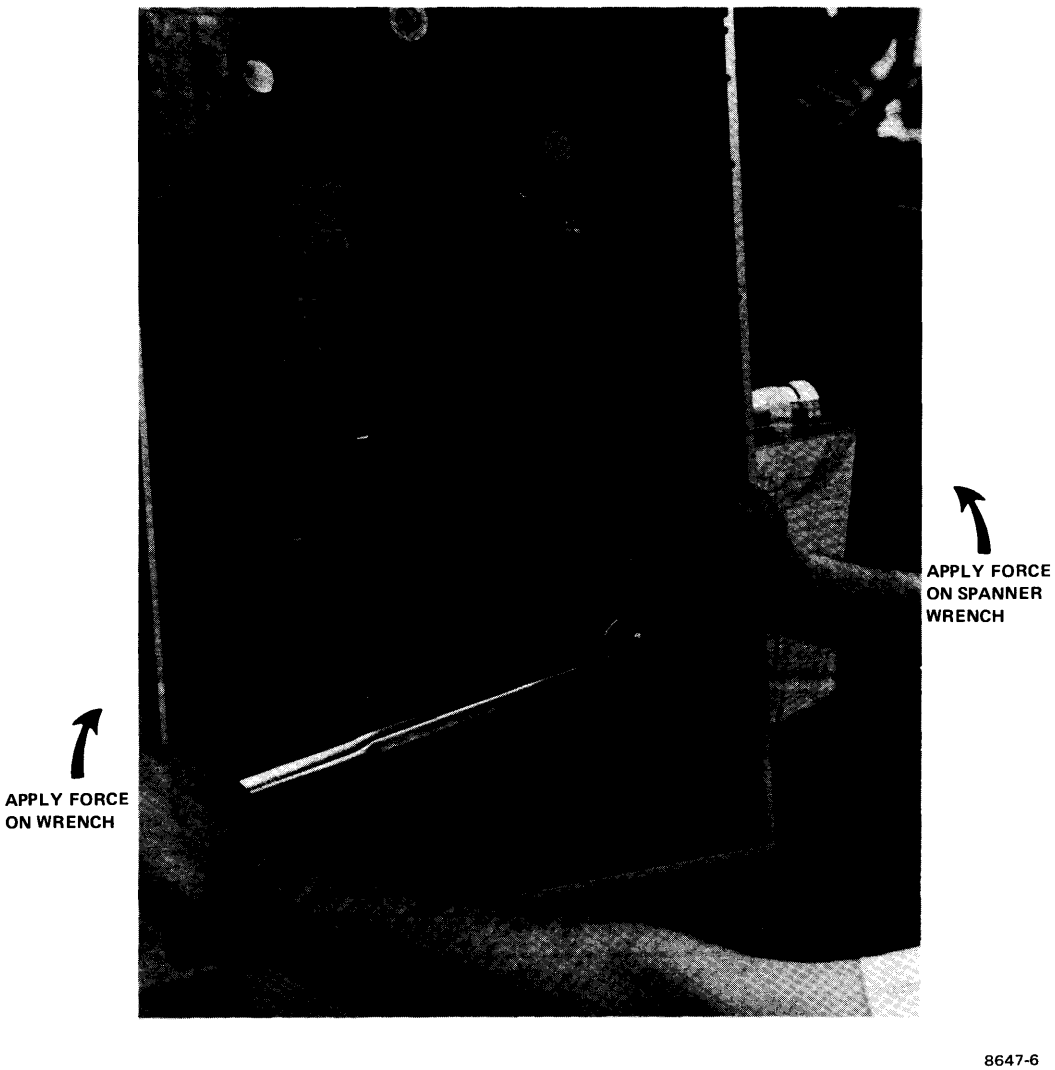


Figure 6-55 Tightening Motor Adapter Nut

9. Lubricate the thrust washer with silicone grease prior to sliding it over the latch lever shaft.

10. Install the shaft through the outer hub, and thread it into the adapter, making sure that the "O" ring indicated in step 8 is in place.

11. Hold the inner hub while rotating the outer hub clockwise, until the outer hub bottoms. Continue to hold the inner hub and rotate the outer hub counter clockwise until the latch lever closes smoothly.

12. Wipe away any excess grease from the outer surfaces of the hub assembly and mount a number of tape reels, fine tuning this rotational adjustment to ensure a constant engagement of all the reels.

13. Install the index screw through the outer hub into the inner hub. Locate the nearest hole in the inner hub prior to screwing it in (Figure 6-56).

14. Verify that the write-protect switch adjustment is still within tolerance (Paragraph 6.5.10).

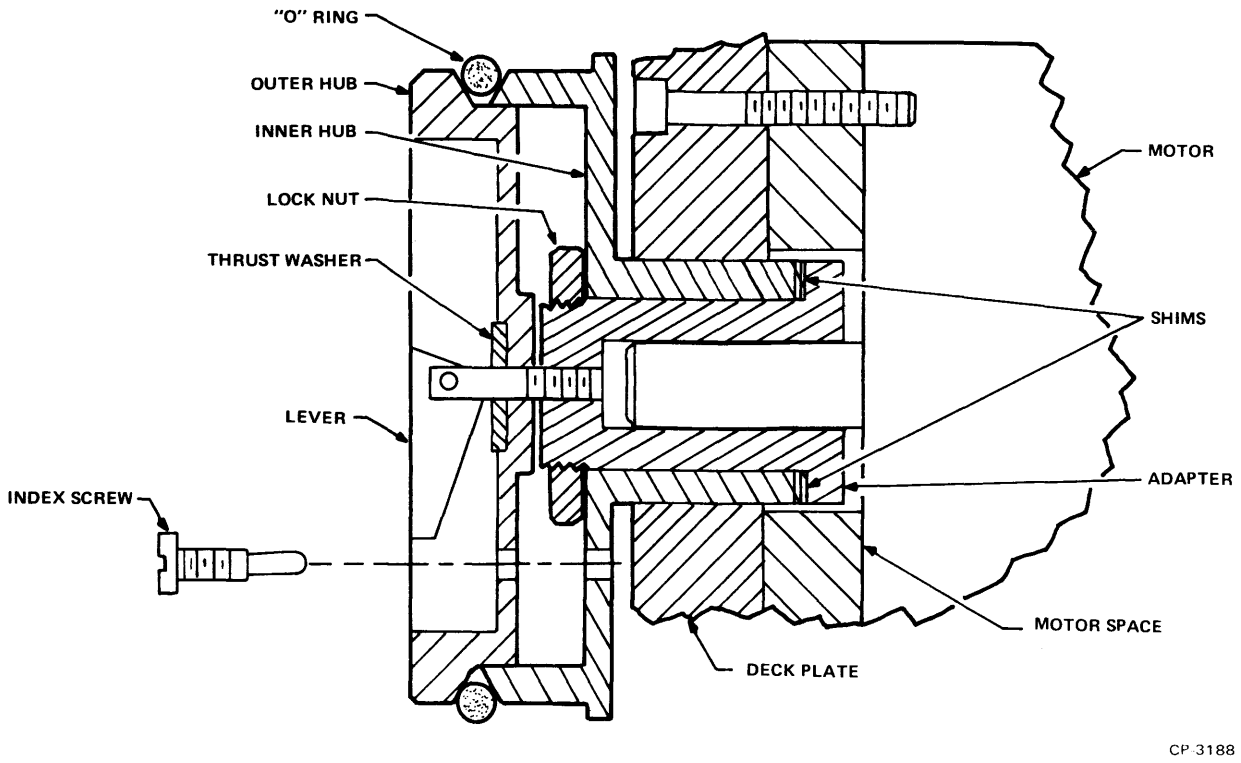


Figure 6-56 Snap-Lock Hub Cross Section

6.6.2 Take-Up Reel

Remove and install the fixed take-up reel as follows:

1. Remove the fixed take-up reel:
   a. Remove the three Phillips head screws from the front.
   b. The reel now comes apart in three pieces: trim plate, front flange, and rear flange.
2. Replace the fixed take-up reel:
   a. Replace the rear flange (Figure 6-57) over the hub casting, being sure to line-up the three mounting holes.
   b. Place the front flange in place over the rear flange, again being careful to line-up the mounting holes.
   c. Place the trim plate over the front flange and secure it with the three Phillips head screws.

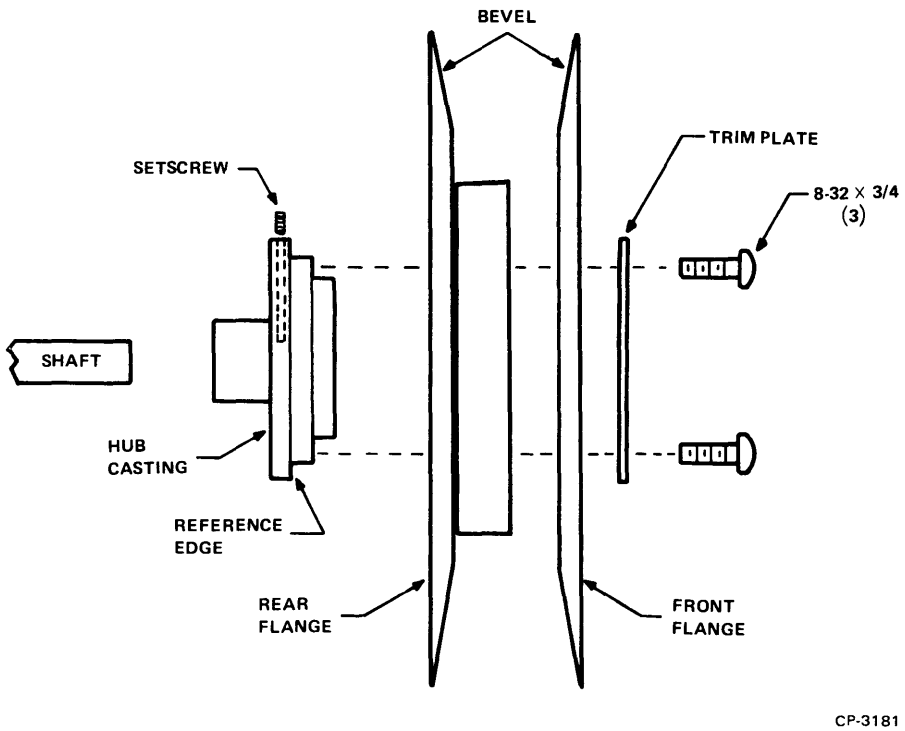


Figure 6-57 Mounting Fixed Take-Up Reel

6.6.3 Capstan Motor/Tachometer

Remove and/or replace the capstan motor and tachometer (12-09786) as follows:

NOTE
The tachometer portion of the assembly is not individually replaceable nor are its brushes.

1. Remove power from the transport.
2. Unplug P4 from the H607 mother board.
3. Remove the capstan wheel (Paragraph 6.6.4).
4. While supporting the motor from the rear, remove the four Allen head cap screws from the front of the casting.
5. Replace the motor by performing steps 2 through 4 in reverse order.
6. Replace the capstan wheel (Paragraph 6.6.4).
7. Perform the capstan perpendicularity adjustment (Paragraph 6.5.1.1).

6.6.4 Capstan Wheel

Remove and/or replace the capstan wheel (74-07957) as follows:

1. Remove the capstan by loosening the locking clamp (between the wheel and the casting) with an Allen wrench and by sliding the wheel and clamp off the capstan motor shaft.
2. Check the end of the shaft for burrs (Figure 6-58). If any burrs exist, remove them with crocus cloth.

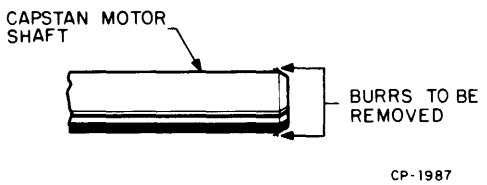


Figure 6-58 Location of Possible Capstan Burrs

3. Install the new capstan wheel by placing the clamp over the split ring and sliding the wheel over the shaft.
4. Tighten the clamp on the shaft.
5. Load a tape and run it back and forth, noting the position of the tape on the rubber capstan wheel. If the tape is not centered, loosen the clamp and slide the wheel to the point where the tape is centered, and tighten the clamp.
6. Perform the capstan perpendicularity adjustment (Paragraph 6.5.1.1).

6.6.5 Roller Guides

Remove and/or replace the roller guides (70-10145) as follows:

1. Loosen the locking clamp at the rear of the deckplate casting, and slide the roller guide out the front (Figure 6-59).

2. Install the new roller guide in the reverse manner, and align it according to the procedure in Paragraph 6.5.1.1.

3. Ensure that a flange cover (74-11590) is affixed to the end of the roller guide shaft with Locktite 404 (29-16578).

NOTE

Be extremely careful to keep Locktite off the roller guide. After affixing the flange cover and after the glue has set, spin the guide to make certain it spins freely.

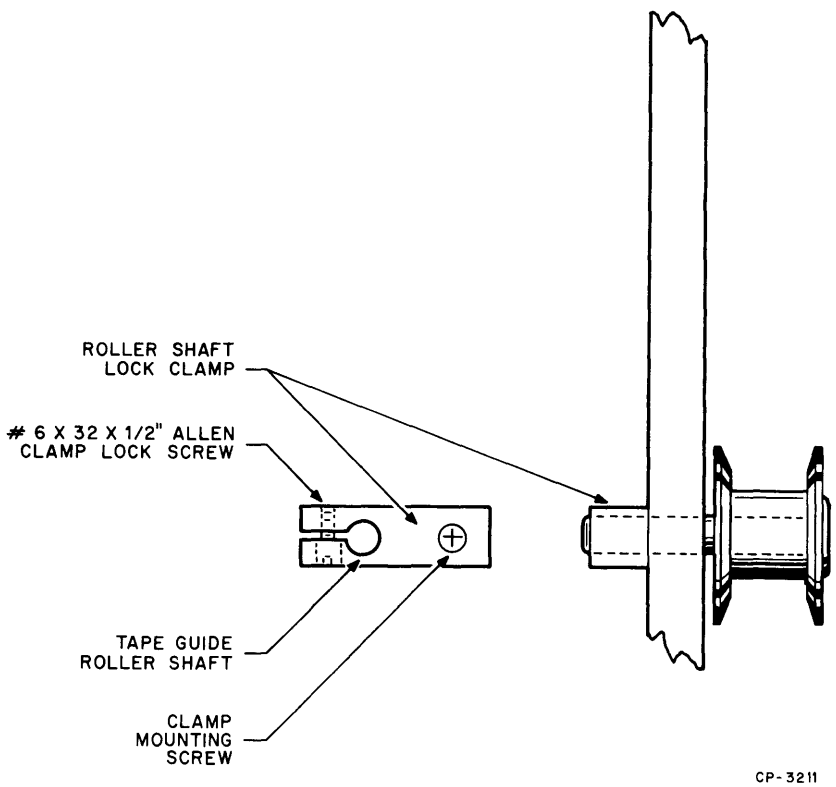


Figure 6-59 Side View of Roller Guide

6.6.6 Fixed Guides

Remove either of the fixed guides as follows:

1. Break the sealing sticker at the end of the guide, in order to expose a slotted screw. Unthread the screw from the casting. It is now possible to replace any of the damaged parts of the guide (e.g., ceramic washer, stainless steel post, spring).

2. Install the fixed guide by reassembling its component parts and threading the screw back into the casting.

NOTE

If a shim was employed between the guide and the casting, be sure to reinstall it as well.

3. Gently tighten the guide screw in order to secure it; too much pressure will fracture the upper (reference edge) ceramic guide washer.

6.6.7 Head Plate Assembly

Remove and/or replace the head assembly as follows:

NOTE

The components of this assembly are not field replaceable. Do not attempt to replace or align the read/write head, erase head, or tape cleaner.

1. Unplug the read, write, and erase head cables.

2. Remove the BOT/EOT sensor (Paragraph 6.6.8).

3. While supporting the head assembly, remove the three shoulder screws holding it in place.

4. Mount the new assembly in place, using the three screws removed in step 3.

NOTE

If shims were employed between the old head plate and the casting, be sure to reinstall them under the new head plate (one under each mounting screw and one under the tape cleaner).

5. Plug in the read, write, and erase head cables.

6. Mount and align the BOT/EOT sensor assembly (Paragraphs 6.6.8 and 6.5.13).

7. Perform the read and write deskewing procedures and tracking check (Paragraph 6.5.3).

6.6.8 BOT/EOT Sensor Assembly

To remove the BOT/EOT sensor assembly (12-11720), proceed as follows:

1. Remove power from the tape transport.

2. Disconnect four wires from the back panel:

C02A2	Red
C02D1	Orange
C02C1	Yellow
C02D2	Brown

3. Locate the sensor mounted on the head plate assembly.

4. Loosen and remove the mounting screw, being careful not to come in contact with any of the head surfaces.

5. Remove the sensor by pulling the wire harness out through the casting.

6. Install the new assembly by performing steps 2 through 5 in reverse order.

7. Align the new sensor using the procedure outlined in Paragraph 6.5.13.

6.6.9 Operator Control Panel

Remove the control panel (70-13339) as follows:

1. Remove power from the tape transport.

2. Disconnect the cable that runs from the rear of the control panel to the M8916 module.

3. Remove the two cable clamp screws.

4. Loosen and remove the four nuts securing the control panel to the casting.

5. Remove the control box by pulling both it and the cable straight out of the casting.

6. Install the new control panel by performing steps 2 through 5 in reverse order.

7. Perform the Operator Panel Check outlined in Paragraph 6.4.3.1.

6.6.10 Reel Motor

Proceed as follows to remove and replace the reel motor (70-09677) (Figure 6-1):

NOTE
The reel motor brushes are not field replaceable.

1. Remove power from the tape transport.

2. Remove the reel hub assembly. Refer to Paragraphs 6.6.1 and 6.6.2 for instructions.

3. Unplug connector P1 from the rear of the H607 mother board.

4. Remove the pins from the P1 plug, and observe that the motor and brake wires are now disconnected from the connector.

5. Remove the four socket head screws that secure the motor to the deck casting. Remove the motor. (When removing the lower motor, also remove the spacer between it and the casting.)

CAUTION
When removing these four screws, the motor must be supported from the rear. If support is not supplied, the motor will fall when the screws are removed.

6. Remove the air filter(s) from the motor(s) (Paragraph 6.6.12).

7. Using the brake assembly removal procedure (Paragraph 6.6.11), remove the brake from the rear of the motor.

8. Reinstall the brake assembly and air filter on the new reel motor (Paragraphs 6.6.11 and 6.6.12).

9. Replace the reel motor and tighten the four screws to a torque value of 1.13 N-m (10 in-lb)

10. Reinstall the reel hub assembly and replace the pins in plug P1.

6.6.11 Reel Motor Brakes

Proceed as follows to remove and replace the reel motor brakes (12-10027):

1. Remove power from the tape transport.

2. Unplug the brake connector (P1) from the rear of the H607 mother board.

3. Remove the pins from P1, holding the wires for the particular brake being removed. Observe that the wires for that particular brake are now disconnected from the respective pin locations in P1.

4. Loosen the hub clamp with an Allen wrench and withdraw the clamp, rotor, and rotor disk (Figures 6-60 and 6-61).

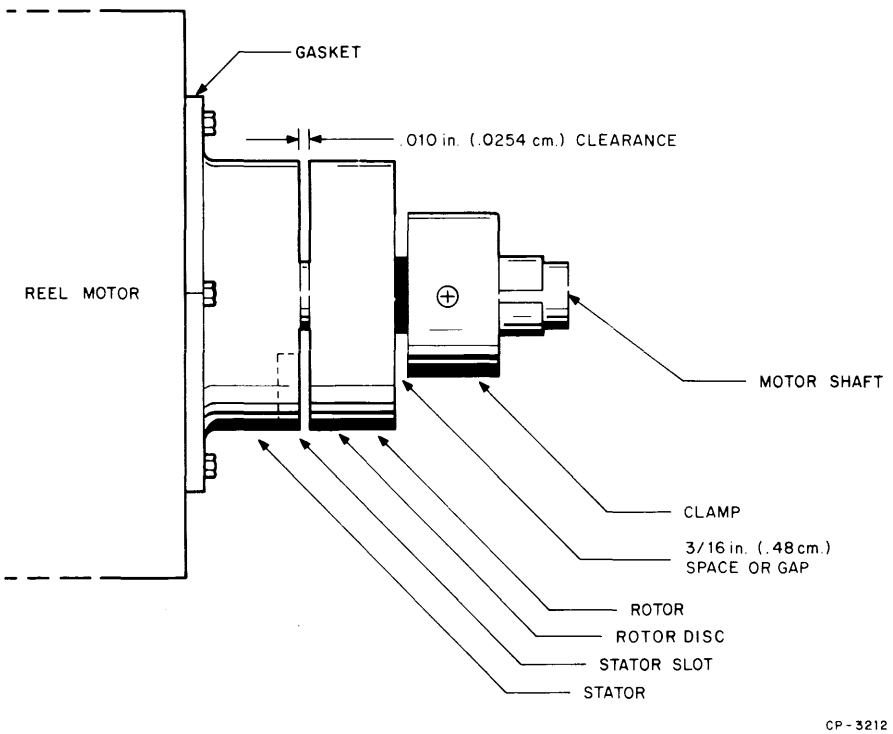


Figure 6-60 Side View Brake Assembly

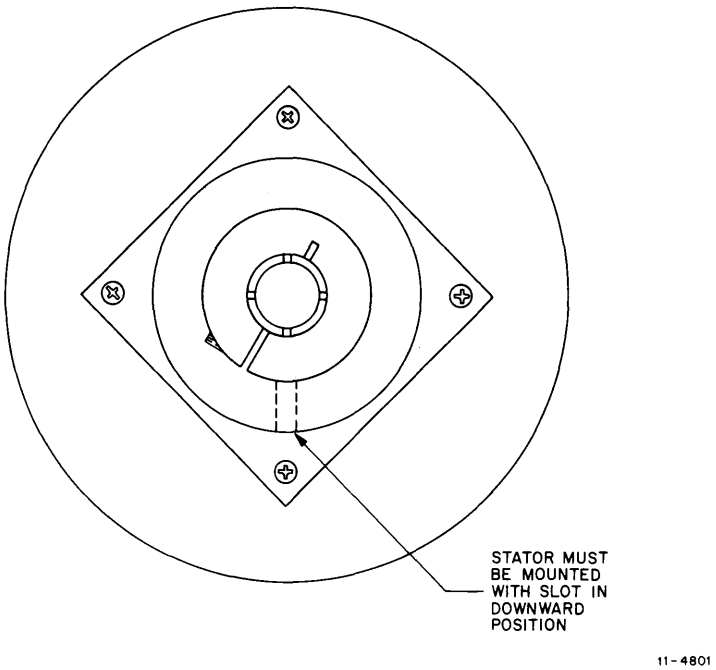


Figure 6-61 Rear View Brake Assembly

5. Remove the four 10-32 screws securing the stator to the reel motor.

6. Discard the stator, rotor, and rotor disk, but retain the clamp and cork gasket.

7. Mount the new stator to the motor using four 10-32 screws. Ensure that the cork gasket is positioned between the stator and the motor. Ensure that the stator slot is at the "6 o'clock" position.

8. Install the rotor disk in the rotor. Select the mating combination that allows for smoothest insertion and retraction of rotor disk pins into the rotor locating holes. Try each of the 120-degree intervals for the best fit.

9. Replace the brake, leaving a clearance of .254 mm (.010 in) between the rotor disk and the stator. When clearance is correct, tighten the Allen screw on the clamp.

10. With the .254 mm (.010 in) feeler gauge inserted between the stator and the rotor, rotate the reel motor manually from the front of the unit to see that the brake is spaced uniformly all around. If necessary, rotate the rotor disk at 120-degree intervals to determine the best position for uniform separation.

11. Reinsert the brake wires into connector P1 (polarity is of no consequence), and plug P1 back into the H607 mother board.

6.6.12 Reel Motor Filter Replacement

Replace the reel motor filter (12-09956) as follows:

1. Refer to Figure 6-62. Remove the entire filter assembly from the rear of the lower reel motor by unscrewing it in a counterclockwise direction.

2. Wrap approximately 1-1/4 turns of Teflon tape around the threads of a new filter assembly, and thread it into the lower reel motor. Hand Tighten Only.

3. Repeat steps 1 and 2 for the upper reel motor filter.

6.6.13 Vacuum Switches and Rubber Sleeves

Proceed as follows to replace the vacuum switches and/or rubber sleeves (12-10477/91-07717) on the switches (Figure 6-63):

1. Remove power from the tape transport.

2. Release the service locks, and pull the transport out on the cabinet slides.

3. Carefully detach the pair of fast-on connectors from each switch and note the respective positions for reassembly purposes.

4. Remove the switch from the bracket by removing the two 2-56 screws and nuts.

5. Cover the vacuum port of the switch with a 2.5 cm × 2.5 cm (1 in × 1 in) square of Texwipe (lint-free cleaning material provided in DIGITAL cleaning kit). This prevents contamination of the switch interior. If Texwipe material is not available, do not substitute anything else; leave the port open. Install Texwipe when it is available.

6. Replace the rubber sleeve on each switch with approximately 2.2 cm (7/8 in) length of tubing. Replace the switch when necessary.

7. Mount the switch to the bracket with two 2-56 screws and nuts.

CAUTION

Guide the switch assemblies so each switch sleeve fits snugly into its respective hole in the casting without any lateral strain. Never overtighten the screws securing the vacuum switches to the bracket; damage to the switch may result.

8. Reconnect the fast-on connectors to all switches.

9. Operate the transport off-line to verify switch functions.

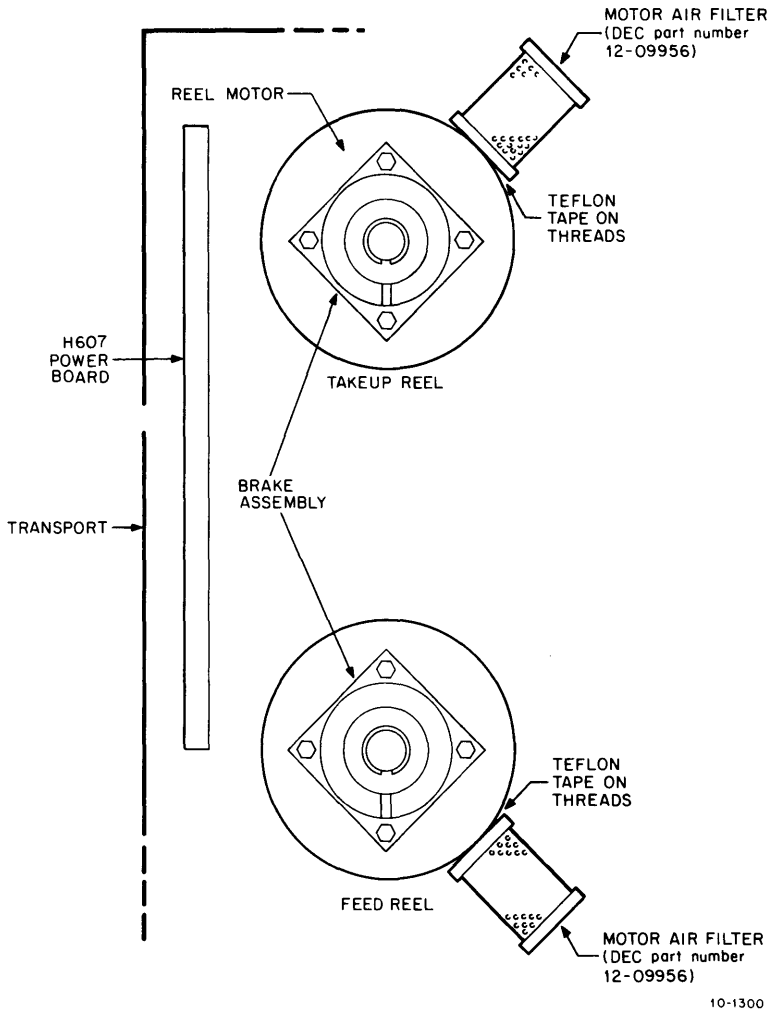


Figure 6-62 Rear View, Reel Motors

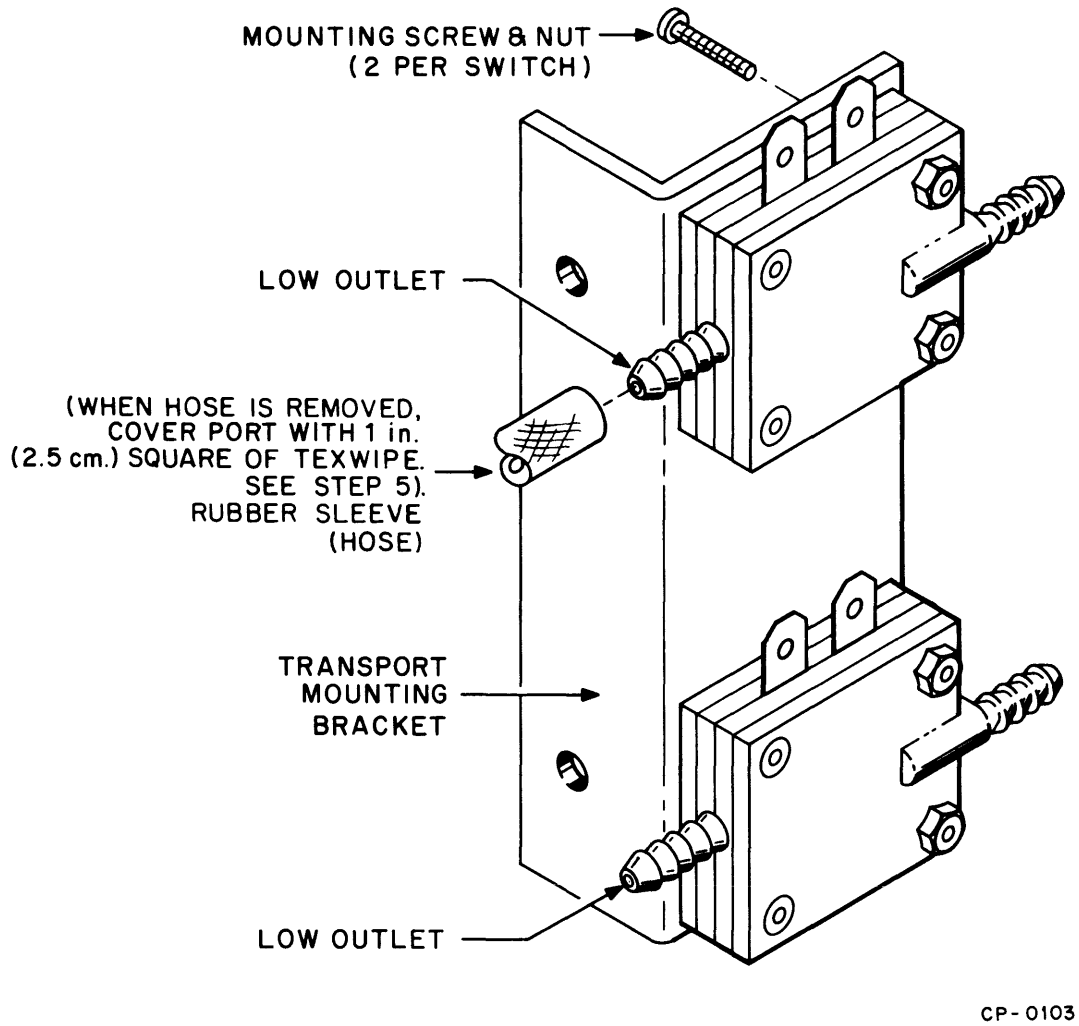


Figure 6-63 Vacuum Switches

6.6.14 Vacuum Assembly Drive Belt

Remove the drive belt (12-11581) as follows:

1. Remove power from the tape transport.
2. From the rear of the transport, remove the vacuum assembly access cover by releasing the four 1/4-turn fasteners.
3. Slip the drive belt off the drive motor pulley, and discard the drive belt.

Install the new drive belt as follows:

1. Loop one end of the new drive belt around the small pulley on the vacuum pump shaft.

2. While rotating the belt, slip the other end over the large pulley on the drive motor shaft.

NOTE
The drive pulley has two diameters; the smaller diameter is used in 60 Hz systems and the larger diameter is used in 50 Hz systems.

3. Refer to Paragraph 6.5.11 for the belt adjustment procedure.

6.6.15 Vacuum Pump Assembly

Proceed as follows to remove and/or replace the vacuum pump assembly (70-09638):

1. Remove power from the tape transport.

2. Slide the transport forward on its slides to facilitate access.

3. From the rear of the cabinet unplug power connector P9 from J9 at the vacuum assembly.

4. Loosen the hose clamp at the vacuum pump, and slide the hose off the shroud.

5. Disconnect the ground wire from the rear of the drive motor.

6. While supporting the vacuum assembly from underneath, remove the four screws holding it captive to the cabinet. Remove the assembly.

7. To replace the assembly, perform steps 3 through 6 in reverse order.

6.6.16 Power Supply Regulator

To remove and/or replace the power regulator (54-12242), proceed as follows:

1. Ensure that power to the tape transport is turned off; then unplug the transport from its outlet at the 861 power controller.

2. Approach the power supply from the rear of the transport cabinet.

3. Remove all plugs (P1 through P5) from the power supply board.

4. Remove the regulator board cover.

5. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

6. Remove the five Phillips head mounting screws and the single Allen head mounting screw (Figure 6-44) from the regulator board.

7. Carefully lift the regulator board out of the cabinet.

8. To reinstall the regulator board, perform steps 1 through 7 in reverse order.

CAUTION

When replacing a power supply regulator board, apply a thin coating of Wakefield No. 128 compound or Dow silicon grease to the diode pack heat sink, and ensure that the Allen head screw is secured very tightly. This provides adequate heat flow and prevents the diode packs from overheating.

9. Next to the AC HI, AC LO, and GND connector tabs in the lower left corner of the power supply regulator board are three additional tab connectors and two wires. Two of the tabs are marked "115"; the other (central) tab is marked "230." If the transport is operating from a 115 V source, the two wires are connected to the two outside tabs (marked 115); for 230 V operation, the wires are connected to the central tab (marked 230).

10. After applying power to the transport, perform the steps outlined in Paragraph 6.5.5 to adjust the regulated voltages.

6.6.17 Transformer-Capacitor Assembly

Proceed as follows to remove and/or replace the transformer-capacitor assembly (7009636) (Figure 6-1):

1. Ensure that power to the tape transport is turned off; then unplug the transport from its outlet at the 861 power controller.

2. If possible, approach the transformer-capacitor assembly from the rear of the transport cabinet. If this is not possible, pull the transport forward on its slides and work from either side.

3. Remove connectors J2 and J3 from the power supply board.

4. Remove the regulator board cover.

5. Remove the transformer-capacitor assembly cover.

6. Unplug the three power connections (AC HI, AC LO, and GND) from the bottom left corner of the regulator board.

7. Remove the four Phillips head mounting screws that hold the transformer-capacitor assembly.

NOTE

Do not remove the two Phillips head screws that hold the transformer-capacitor assembly bracket.

8. Remove the Phillips head screw holding the ground strap in place.

9. Carefully lift the transformer-capacitor assembly out of the cabinet.

10. To reinstall the transformer-capacitor assembly, perform steps 1 through 8 in reverse order.

6.7 CORRECTIVE MAINTENANCE

Corrective maintenance information is provided to guide and assist the Field Service engineer when he is isolating and repairing faults. Photographs, line art, and tabular summaries complement this section, to aid the Field Service engineer.

6.7.1 Tape Loading/Motion Troubleshooting

This section relates strictly to tape loading/motion problems and does not discuss problems dealing with motion/data transfer. Refer to Paragraphs 5.2.1 (Tape Loading) and 5.2.3 (Capstan Motion) for further information.

The following list summarizes where the various adjustment procedures are documented.

Adjustment	Paragraph
Tape Path Alignment Procedure	6.5.1
Snap Lock Hub Adjustment	6.5.2
Skew Adjustments	6.5.3
Read Amplitude Adjustments	6.5.4
Regulated Power Supply Voltages	6.5.5
Capstan Balance and Speed	6.5.6
Capstan Current	6.5.7
Tape Unload Adjustment	6.5.8
Reel Motor Brake Adjustments	6.5.9
Read/Write Interlock Assembly Adjustment	6.5.10
Vacuum Motor Belt Tension Adjustment	6.5.11
Vacuum Motor Pulley Height Adjustment	6.5.12
BOT/EOT Sensor Alignment	6.5.13

Complete troubleshooting information covering Tape Loading, Improper Off-line Tape Motion, and Improper On-Line Motion is provided in Tables 6-7, 6-8, and 6-9 respectively; refer to the correct table(s) whenever necessary.

6.7.2 Reel Motor/Brake Control Troubleshooting

This section is divided into three parts:

6.7.2.1 Initial Checks

6.7.2.2 Suggestions for isolating failing components

6.7.2.3 Suggestions for troubleshooting intermittent fail-safe conditions.

6.7.2.1 Initial Checks - Before the TE16 reel motors can operate to maintain the tape loops in the buffer columns, several requirements must be met.

Table 6-7 Tape Loading Troubleshooting Chart

Symptom	Possible Solutions
Vacuum motor does not turn on with LOAD switch, and relay on 5412242 board does not energize.	Check cable connections from switch box to M8916, specifically LOAD SW L at E60 pin 12 of M8916.
	Check cable connections from M8916 to H607 daughter board.
	Check cable connections from H607 daughter board to H607 mother board, specifically J2 pin 1.
	Check harness between H607 mother board and 5412242 regulator board.
	Check for +17 V.
	Possible bad 5412242 regulator board or open relay coil.
Vacuum motor does not turn on with LOAD switch, but relay on 5412242 energizes.	Check fuse F1 (Figure 6-69).
	Check cable harness from 5412242 P1 to vacuum motor assembly.
	Possible bad vacuum motor assembly.
Vacuum motor turns on, but reel motors do not dump tape into columns.	Check for +17 V INT and ±17 V at H607 mother board J2.
	Check LOAD PULSE L at H607 daughter E45 pin 8 and H607 mother board E11 pin 1.
	Check that reel motors are plugged into the H607 mother board.
	Check wiring and operation of lower fail-safe switches.
Reel motors dump tape and vacuum motor turns off.	Check belt tension on vacuum motor assembly.
	Check vacuum hose for leaks.
	Check door seal of vacuum cover door.
	Check roller guide adjustment.
	Check all fail-safe switches.
	Check for obstructions (e.g., dirt, paint) at the top of vacuum columns.
Reel motors dump tape into columns, then vacuum motor shuts off.	Check wiring to all vacuum column fail-safe switches.
	Possible bad fail-safe switch.
	Possible bad M8916.

Table 6-8 Off-Line Tape Motion Troubleshooting Chart

Symptom	Possible Solutions
Tape loads into columns, runs forward then rewinds, and runs off reel.	Check that tape has a BOT marker and that it is positioned properly [i.e., 4.9 ± .3 m (16 ± 1 ft)] from the beginning. Check for -6 Vdc at pin C02B2. Check for misaligned BOT/EOT sensor. Possible bad M8916.
Capstan does not respond to motion commands given by maintenance switches.	Check harness connection between capstan motor and H607 mother board J4. Check for +16 Vdc, -16 Vdc, and PWR COM INT at H607 mother board J2. Check direction signals FWD (1) H (pin E02N1) and REV (1) L (pin E02P2).
Capstan moves tape, but tape leaves vacuum column.	Refer to Paragraph 6.7.1.2, Reel Motor Brake Control Troubleshooting.

Table 6-9 On-Line Tape Motion Troubleshooting Chart

Symptom	Possible Solutions
Tape moves in off-line mode but will not respond to on-line commands.	Ensure that the control panel SEL indicator is lit. If it is not, find out why the formatter or the controller is not selecting the transport. Check cable connections from controller or formatter to module(s) in slot 1. Check the following lines for proper level: STOP A01V2 +3 Vdc INIT PLS A01U2 +3 Vdc DRV CLR B01D2 +3 Vdc Troubleshoot with the appropriate instruction test and/or data reliability test. If transport is a TE16, use UTILITY DRIVER (BRUTIS).

Power Supply Voltages – Logic power (+5 Vdc) is supplied to the reel motor control circuitry via the cable connecting the M8916 and 5412262 daughter module. From the 5412262, it is transmitted to the 5412264 along the cable connecting those two boards. Logic power should be present at pin 14 or pin 16 of all 74-series integrated circuits. Motor power is supplied at the middle connector on the 5412264 module. The voltages indicated in Figure 6-64 should be present.

Although the capstan power lines are shown (orange and yellow wires), they are not necessary for operation of the reel motors and brakes.

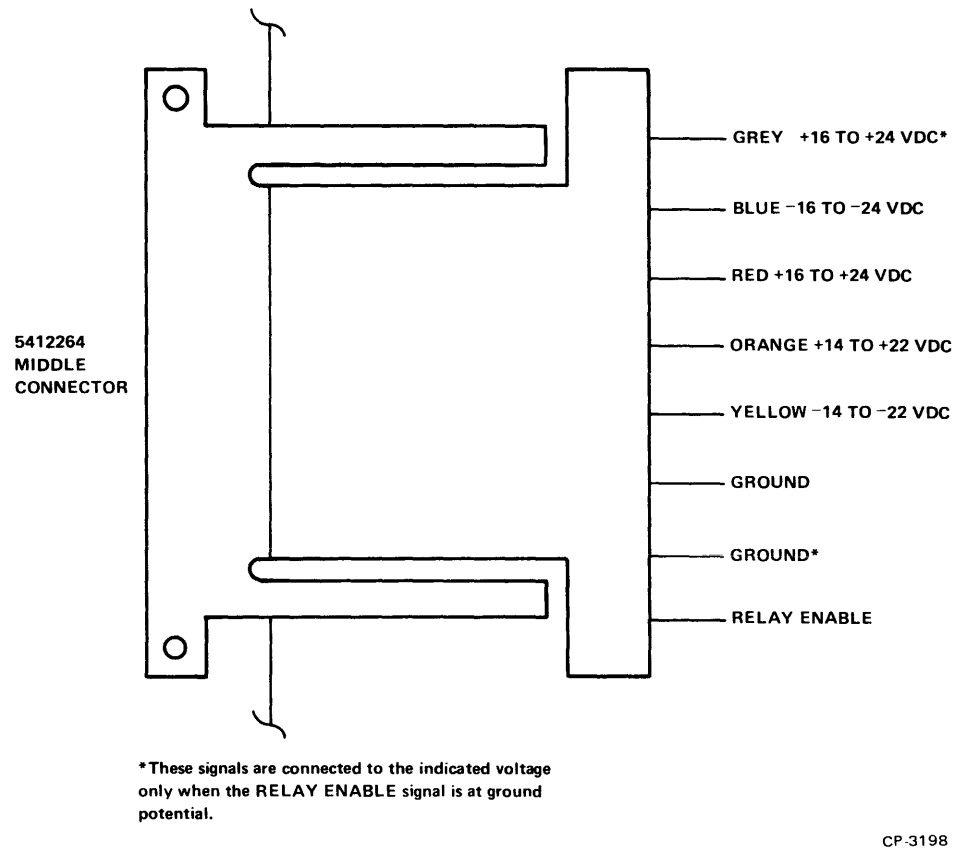


Figure 6-64 Motor Power Voltages

Control Signals – Control signals for reel motor and brake control are supplied along the M8916-daughter cable and on the Mate-N-Lok connectors attached to the daughter board. Motor and brake commands are transmitted from the daughter board to the mother board along the flat cable connecting them. Ensure that all connectors are firmly seated.

Reel Motor Enable – The M8916 generates the REEL MOTOR ENABLE signal when both lower fail-safe switches close. Faulty fail-safe switches, harnesses, or an M8916 may cause this signal to remain in the negated state, preventing the reel motors from turning.

Sequencing Clock on 5412262 – A train of clock pulses should appear at E8 pin 5 of the 5412262; they are used to sequence the logic that controls reel motors and brakes. The pulses should appear in a 5 ms rate. If the pulse train frequency is incorrect, it can be adjusted with the R16 potentiometer (Figure 6-19).

6.7.2.2 Suggestions For Isolating Failed Components – Failures in the reel motor control portion of the TE16 are extremely difficult to troubleshoot, because they are not repetitive enough and, therefore, cannot be "scoped." The following hints should prove to be very helpful when confronted with a reel motor failure.

Bypassing the Capstan – The capstan motor can be bypassed so that the "dynamic braking" mode of operation can be exercised without the danger of immediate tape loop fail-safes. To do this, open the TE16 buffer column door and thread the magnetic tape under the capstan (Figure 6-65). Be sure to use a "scratch" tape, as this procedure does damage tape. Leave a loop in each column so that the loop is positioned roughly midway between the fail-safe switches in either column (Figure 6-66).

NOTE

If the reel motors are totally out of control, a 1.5 m (5 ft) section of tape may be cut away from a reel, threaded as shown in Figure 6-65 and secured at either end with adhesive tape. Now this arrangement may be manipulated to determine if reel motors are being properly controlled, but without damage of reel motors driving tape past fail-safe switches.

Once the loop is properly positioned, close the buffer column door and press LOAD. Vacuum should be established in a normal fashion, and the LOAD indicator will come on. The capstan will start moving counterclockwise (forward) and, after about four seconds, will reverse direction in its attempt to rewind to BOT. Use the maintenance switches to stop the capstan. Now manually move the tape loops and observe the behavior of the reel motors. Issue forward, reverse, and rewind commands to the capstan and check each mode of operation. Table 6-10 lists the recommended sequences through which the loops in the right column can be moved, while Table 6-11 lists the same information for the loops in the left column. Always start with the tape loop positioned in the center of the column and then load the motion command.

NOTE

The state of sequencing logic in the reel control logic is dependent upon the last tape motion command that the drive executed. For this reason, it is necessary to be careful to examine operations only under the conditions described in Table 6-10.

6.7.2.3 Suggestions For Troubleshooting Intermittent Reel Operations

Sluggish Loop Performance – Sluggish loop performance is generally due to one of the following items. A suggested remedy accompanies each problem area:

1. **Insufficient Degaussing of Brake** – This can be detected as a medium-to-heavy "drag" when the reel is moved. Remedy: replace the H607.

2. **Dirty Brake** – Disassemble and clean the brake.

3. **Overheated Reel Motor** – Sluggishness should be more pronounced with a full reel of tape. The motor temperature should be too hot to touch. Remedy: replace clogged air filter; if that does not eliminate the problem, replace the motor.

4. **Clogged Vacuum-Sensing Hole or Vacuum-Sensing Switch** – Remove the switch assembly, clean the hole, and replace the switch assembly.

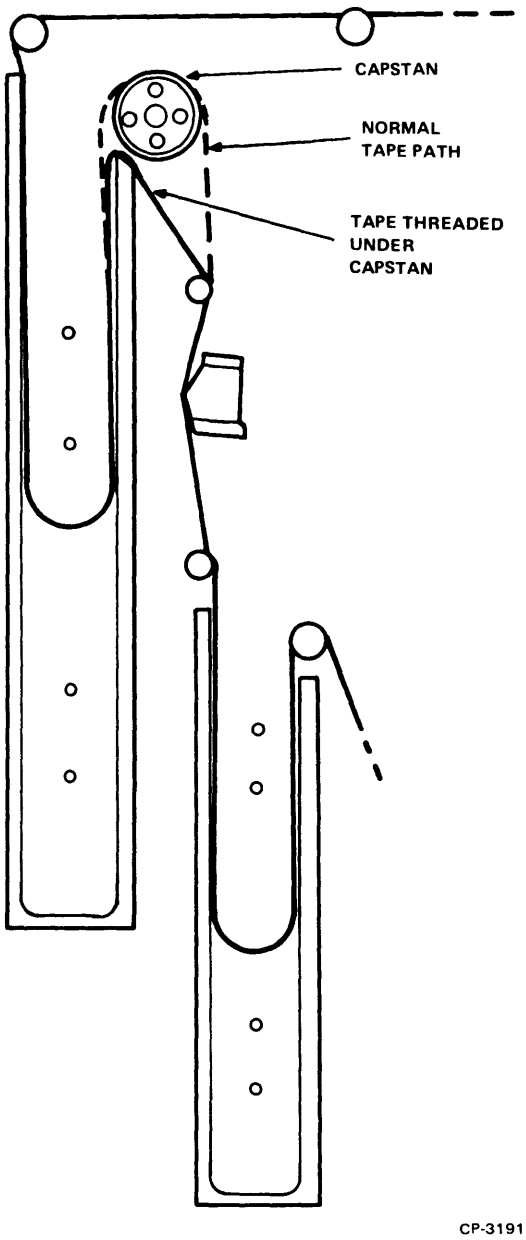


Figure 6-65 Bypassing Capstan, Tape Test Setup

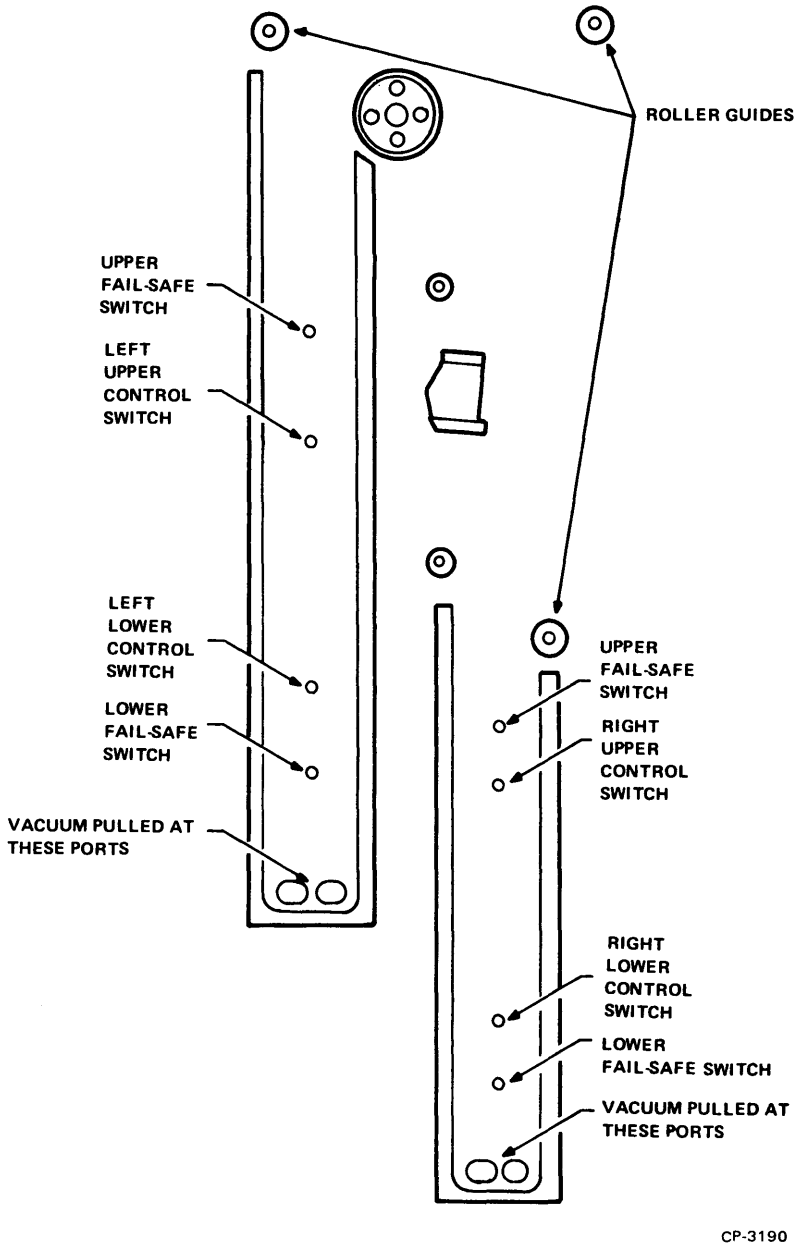


Figure 6-66 Locations to Remember During Test

Table 6-10 Loop Motion Sequences For Right Column (Lower Motor)

CAPSTAN ACTION	LOOP POSITION				
	Between Control Switches	**Below Lower Control Switch**	**Between Control Switches**	**Above Upper Control Switch**	**Between Control Switches**
Moving Forward	Brake ON initially	Full power, Counter-clockwise	Brake ON again	Pulsing power, clockwise	Pulsing power, counter-clockwise
Moving Reverse	Brake ON initially	Pulsing power, counter-clockwise*	Pulsing power, clockwise	Pulsing power, clockwise	Pulsing power, clockwise
Rewinding	Brake ON initially	Full power, counter-clockwise	Pulsing power, clockwise	Pulsing power, clockwise	Pulsing power, clockwise

*For each subsequent turn that the loop travels below the lower control switch, a short "kick" should be felt, followed by pulsing power.

Table 6-11 Loop Motion Sequences For Left Column (Upper Motor)

CAPSTAN ACTION	LOOP POSITION				
	Between Control Switches	**Below Lower Control Switch**	**Between Control Switches**	**Above Upper Control Switch**	**Between Control Switches**
Moving Forward	Brake ON initially	Pulsing power, clockwise*	Pulsing power, counter-clockwise	Pulsing power, counter-clockwise	Pulsing power, counter-clockwise
Moving Reverse	Brake ON initially	Full power, clockwise	Brake ON again	Pulsing power, counter-clockwise	Pulsing power, clockwise
Rewinding	Brake ON initially	Full power, clockwise	Brake ON again	Full power, counter-clockwise	Pulsing power, clockwise

*For each subsequent turn that the loop goes below the lower control switch, a short "kick" should be felt, followed by pulsing power.

Intermittent Loop-Outs – Intermittent loop-outs (fail-safes) are generally caused by a failed mechanical component or connection. The following are some characteristic loop-out symptoms, followed by a suggested remedy:

1. **Loop Winds Up 5+ cm (2+ in) Above Fail-Safe Switch** – This is probably due to an intermittent open in a vacuum-sensing switch, caused by contamination. In such a case, all vacuum-sensing switches should be replaced.

2. **Loop Winds Up Slightly Above or Below Fail-Safe Switch** – This is probably an intermittent open in the reel motor leads or contamination of the motor brushes. Replace the motor and/or the H607.

3. **Loop Winds Up Below Lower Fail-Safe Switch in Right Hand Column** – This symptom may occur only during rewinds or during both rewind and normal reverse operation. Generally, this is caused by a false trigger of the LOAD PULSE circuitry. Check for proper filtering of the LOWER FAIL-SAFE H signal on the M8916. Also, check for proper filtering at E4 pin 9 on the 5412262 module (this is the LOAD PULSE one-shot). Ensure that the electrostatic shield is installed between the 5412262 and 5412264 modules.

4. **Fail-Safe Occurs Only During On-Line Read/Write** – If a fail-safe condition occurs only during on-line motion when reading and writing, the problem may be caused by an intermittent control cable (BC06R) connecting the TE16 to its controller.

6.7.3 Clocks Troubleshooting

Figures 6-67 and 6-68 provide a guide for analyzing TE16 (TE10) transport clock-related problems. Refer also to the engineering print set and Paragraph 5.3.4(M8911-YB) of this manual. Careful evaluation of the trouble symptoms and good troubleshooting judgment are necessary to successfully apply Figures 6-67 and 6-68 to practical troubleshooting situations.

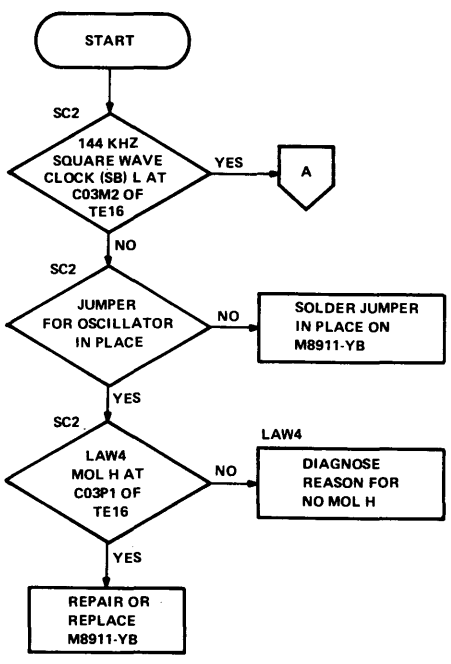


Figure 6-67 TE16 Clock Troubleshooting Flow Diagram (Sheet 1 of 2)

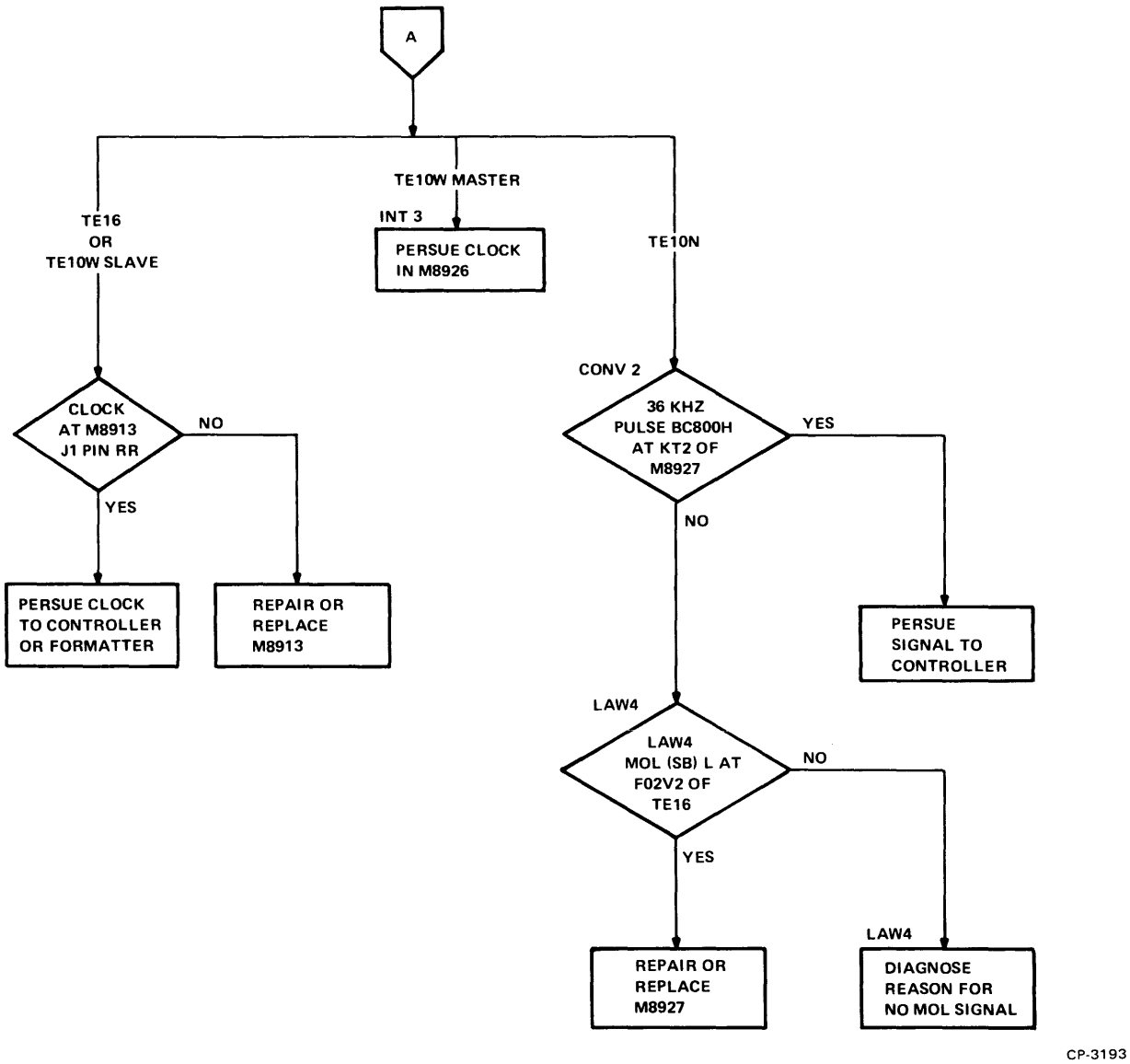


Figure 6-67 TE16 Clock Troubleshooting Flow Diagram (Sheet 2 of 2)

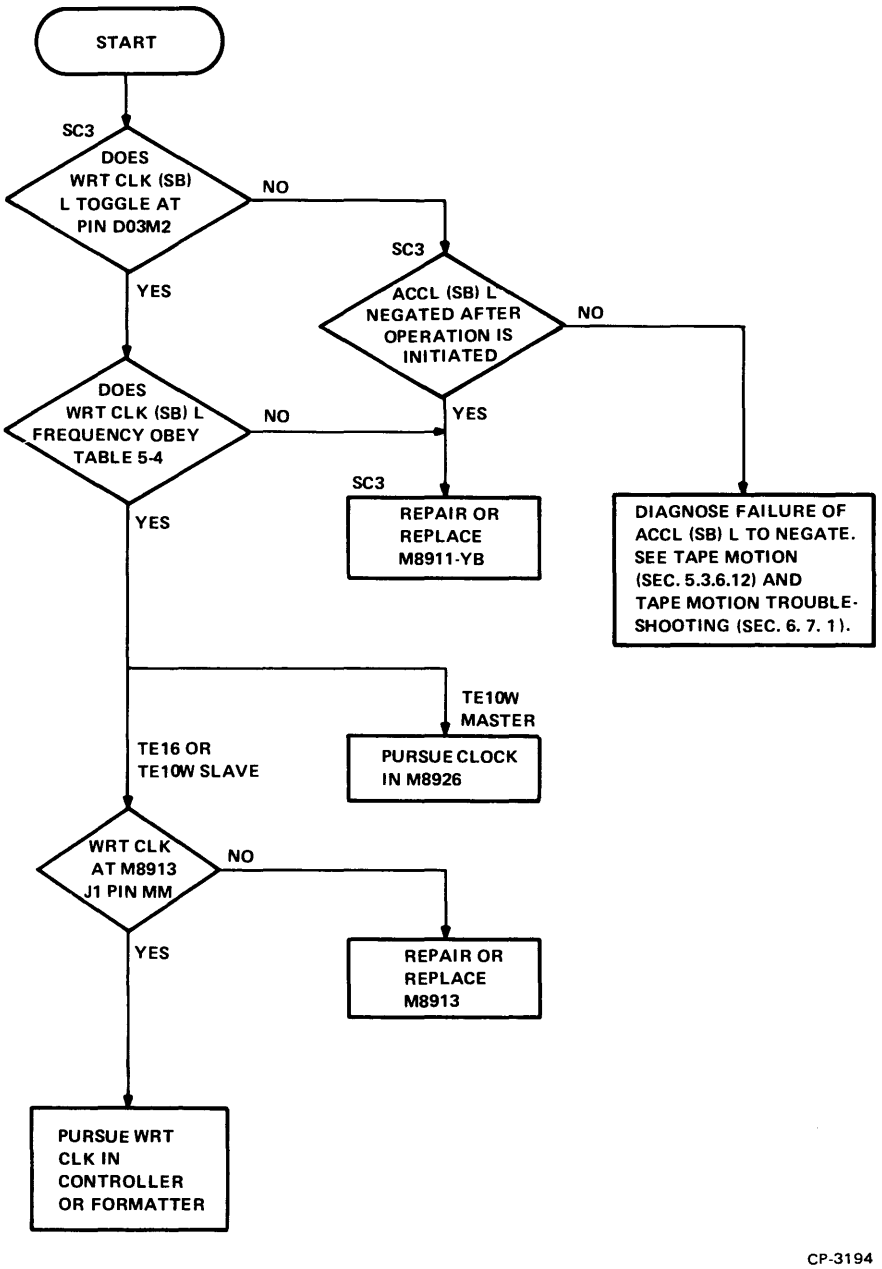


Figure 6-68 TE16 Clock Troubleshooting Write Clock Signals

6.7.4 Power Supply Troubleshooting

This section relates to the failure analysis of the power supply, especially the 5412242 regulator module, both internal and external to the module. Refer also to Paragraph 5.3.2 for theory and Engineering Drawing D-CS-5412242-0-1, the circuit schematic.

The following list summarizes where the various adjustment procedures are documented. If, during troubleshooting, one or more of these adjustments must be performed, refer to the relevant section for the correct procedure.

Adjustment	Paragraph
+5 Vdc	6.5.5.1
+12 Vdc	6.5.5.2
-6.4 Vdc	6.5.5.3
+12 Vdc (NRZI)	6.5.5.4
+5 Vdc (PE)	6.5.5.5

6.7.4.1 Troubleshooting Rules – When troubleshooting power supply problems, be sure to adhere to the rules listed below:

1. Ensure that power is turned OFF and the transport is unplugged before attempting to service the power supply.

2. Ensure that capacitors C6, C8, C11, C15, and C20 are discharged before servicing the power supply. A 10-to-100 ohm 10 W resistor can be used to hasten the discharge of the capacitors. (Be sure power is OFF.)

3. Any cartridge-type fuse that must be replaced can be replaced without removing the regulator module portion of the power supply.

4. For proper operation, all hardware must be secured tightly to approximately 1.36 N-m (12 in-lb). All hardware should be replaced with identical hardware replacement parts.

5. The module portion of the power supply may be removed from its mounting area by removing five Phillips head screws and one Allen head screw.

6. If the 5412242 regulator fails, it should be replaced as a unit. However, if the need arises, troubleshoot the regulator to the component level. Should component level troubleshooting take place, the following rules must be adhered to:

   a. When replacing semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield No. 128 compound to the heat sink contact side (bottom) of the semiconductor. Insulating wafers are not required.

   b. If a diode pack is replaced, the Allen screw used to secure it must be secured very tightly. If the screw is not tightened securely, overheating of the diode pack can result.

7. While troubleshooting with power on and a load applied (P5 plugged in), do not remove plug P1 from the regulator board or allow the small fan above the heat sink to stop turning, or damage to the regulator will result.

CAUTION

Voltages up to 220 Vac are present on the power supply regulator module. Use caution when making measurements and adjustments with power applied to the transport. Keep one hand behind your back or in a pocket, and do not come in contact with any metal parts on the transport.

6.7.4.2 Troubleshooting Hints

1. Make a visual examination of the circuitry, check for burnt printed circuit board etch, oil leakage from capacitors, and loose connections. A good visual check can prove to be a quick method of locating the cause of a malfunction.

2. The +5, +12, and -6.4 V regulators contain overvoltage detection circuitry. If any one of the potentiometers (used to adjust regulated output voltage) is adjusted too far clockwise, the corresponding Crobar circuit may trip. To avoid this, adjust the particular potentiometer fully counterclockwise and readjust it per Paragraph 6.5.5.

6.7.4.3 Troubleshooting Charts – In checking the various areas of the power supply, the rules listed in the preceding section should be adhered to. In addition to the main troubleshooting chart (Table 6-12), a separate fuse chart (Table 6-13) is included. Also, refer to Figure 6-69 for fuse locations.

Table 6-12 Power Supply Troubleshooting Chart

Problem	Cause	
	5412242 Regulator	**Transformer/Capacitor Bank**
No +5 Vdc (J5; 1, 7)	• F4, F5, or F12 open • D9 totally open • +5 V adjusted too high (Crobar) • C6, C8, or C9 shorted • D15 shorted anode to cathode • R64, R65, R66 open	• C5 or C6 shorted • Transformer open (no voltage at J2; 10, 13)
+5 Vdc output too low	• E1 (723) bad • Q5 (2N5302) open • Q6 (2N3055) shorted • D9 partially open	
+5 Vdc output too high	• E1 (723) bad • Q5 (2N5302) shorted • Q6 (2N3055) open • D16 open	
No +12/+5 Vdc (J5; 8)	• F5 open • R32 open • D10 and D19 or D18 and D27 open • C11 or C13 shorted	• C5 shorted • Transformer open (no voltage at J2; 8, 12)
+12/+5 Vdc output too low	• E2 (723) bad • Q7 (2N3055) open • D10, D18, D19, or D27 open	
+12/+5 Vdc output too high	• E2 (723) bad • Q7 (2N3055) shorted • E5 (75451) shorted	

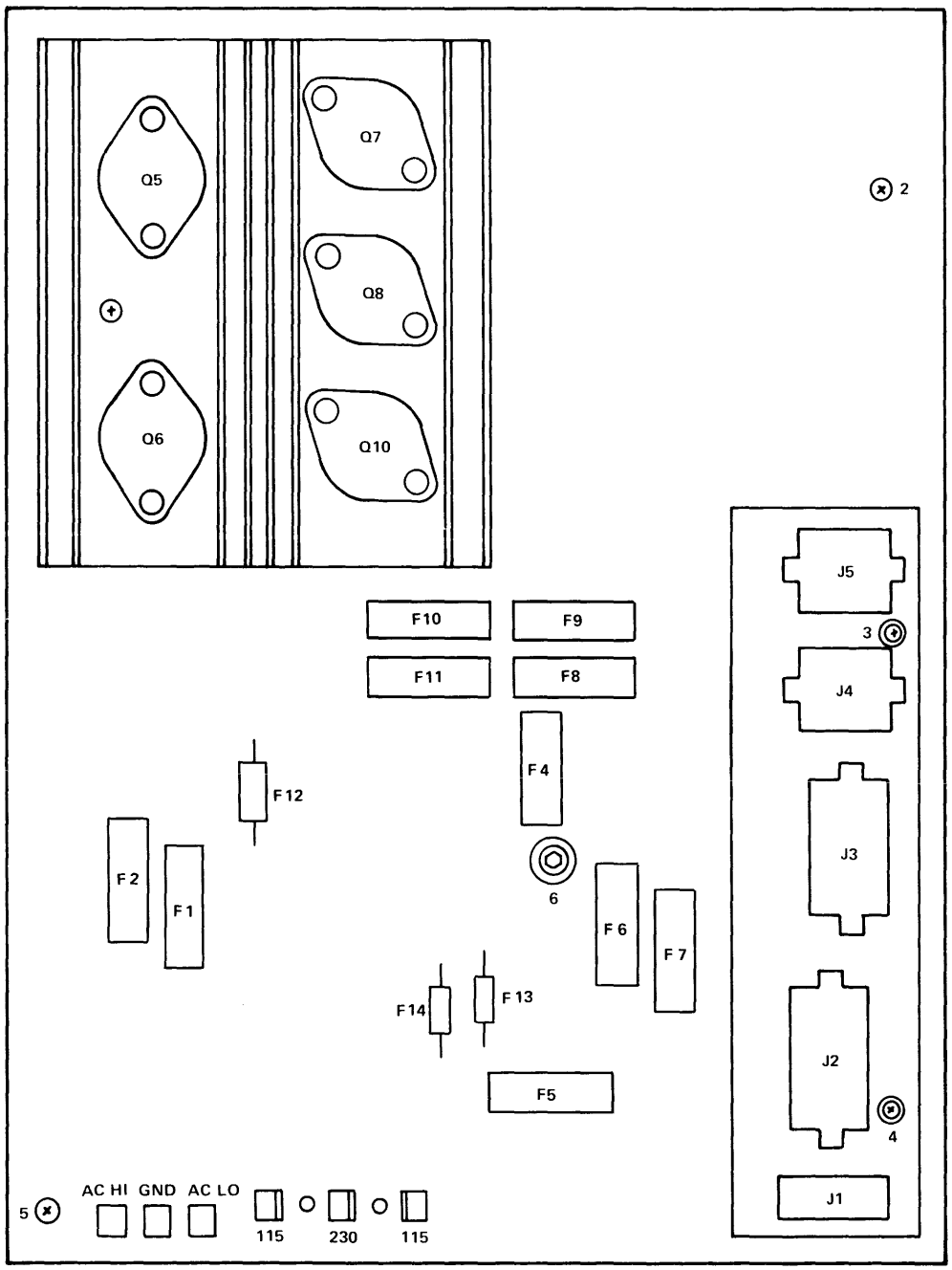
Table 6-12 Power Supply Troubleshooting Chart (Cont)

Problem	Cause	
	5412242 Regulator	**Transformer/Capacitor Bank**
No +12 Vdc (J5; 5)	• F5 or F10 open • Diodes D10 and D19 or D18 and D27 open • C11, C15, or C18 shorted • R41 open • D22 shorted anode to cathode	• C5 shorted • Transformer open (no voltage at J2; 8, 12)
+12 Vdc output too low	• E3 (723) bad • Q8 (2N3055) open • D10, D18, D19, or D27 open	
+12 Vdc output too high	• E3 (723) bad • Q8 (2N3055) shorted • D23 open • D21 shorted	
No -6.4 Vdc (J5; 4)	• F11 or F13 open • D11 totally open • C20 or C22 shorted • D24 shorted	• C3 shorted • Transformer open (no voltage at J2; 2, 3)
-6.4 Vdc output too low	• E4 (LM304) bad • R50 open • Q10 open • Q11 shorted • D12 partially open • Q12 shorted	
-6.4 Vdc output too high	• E4 (LM304) bad • Q10 shorted • Q11 open • D20 open • D25 shorted	
No +16 Vdc (J4; 6)	• F9 or F14 open • D11 open	• C4 shorted • Transformer open (no voltage at J2; 1, 2)
No -16 Vdc (J4; 2)	• F8 or F13 open • D11 open	• C3 shorted • Transformer open (no voltage at J2; 2, 3)
No +17 Vdc (J4; 1)	• F6 open • D12 open	• C2 shorted • Transformer open (no voltage at J2; 14, 15)
No -17 Vdc (J4; 7)	• F7 open • D12 open	• C1 shorted • Transformer open (no voltage at J2; 9, 14)

Table 6-13 Fuse Chart*

Fuse	Type	Indication When Fuse is Open
F1	5 ASB	Vacuum motor not on
F2	115 V = 6-1/4 ASB 230 V = 4 ASB	No voltage outputs in 115 V configuration Low voltage outputs in 230 V configuration
F4	15 ASB	No +5 Vdc No indicators No logic response
F5	3 ASB	No +5 Vdc No +12 Vdc No +5/+12 Vdc No logic response No indicators
F6	20 A	No +17 Vdc to H607 power board No LOAD function No brakes
F7	20 A	No -17 Vdc to H607 power board No reel motor action
F8	8 A	No -16 Vdc to H607 power board No reverse capstan
F9	8 A	No +16 Vdc to H607 power board No forward capstan
F10	.75 A	No +12 Vdc No write current
F11	.75 A	No -6.4 Vdc No EOT/BOT sensed No read data
F12	15 A	No +5 Vdc No indicators No logic response
F13	15 A	No -16 Vdc; therefore, no reverse capstan. No - 6.4 Vdc; therefore, no EOT/BOT sensed.
F14	15 A	No +16 Vdc; therefore, no forward capstan.

*Refer to Figure 6-69 for location of fuses.



NOTES:
1) 1–5 represent 5 Phillips head screws.
2) 6 represent Allen screw - must be secured very tightly, or damage to the power supply may result.

Figure 6-69 5412242 Regulator Board Fuse Locations

6.7.4.4 Troubleshooting Blown Fuses – Do the following to troubleshoot a blown fuse.

Steady State – If a particular fuse blows every time power is applied to the transport and conventional troubleshooting methods are exhausted, follow steps outlined in Figure 6-70, the Fuse Troubleshooting Chart.

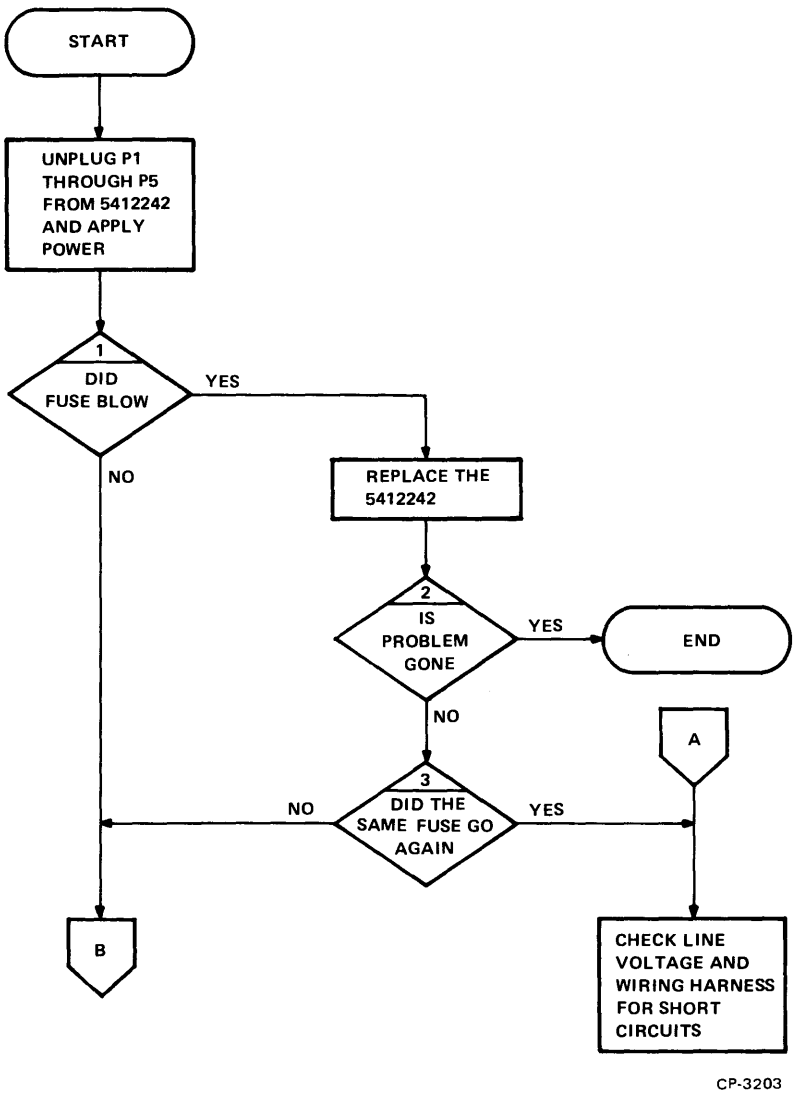


Figure 6-70 Fuse Troubleshooting Chart (Sheet 1 of 7)

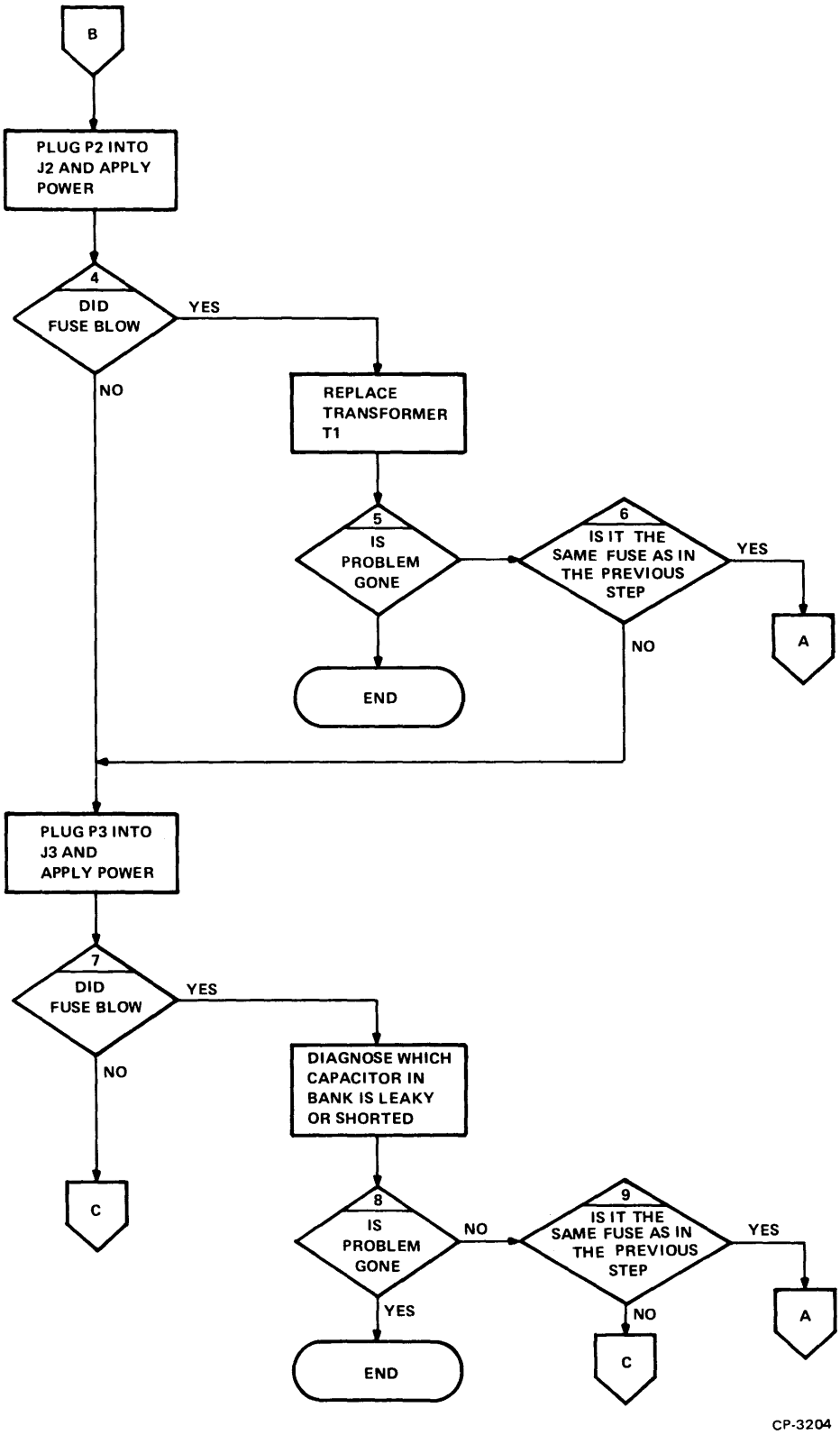


Figure 6-70 Fuse Troubleshooting Chart (Sheet 2 of 7)

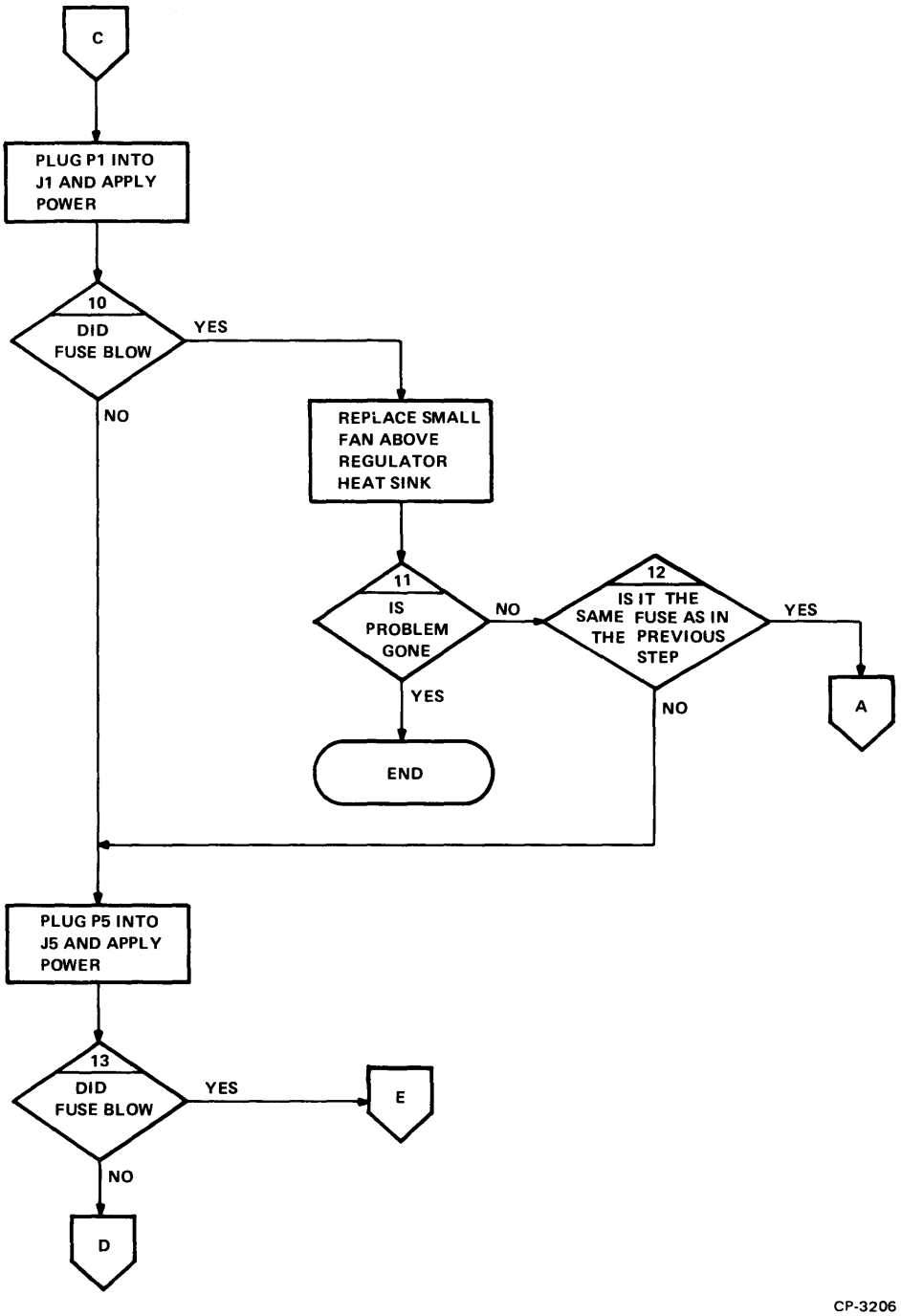


Figure 6-70 Fuse Troubleshooting Chart (Sheet 3 of 7)

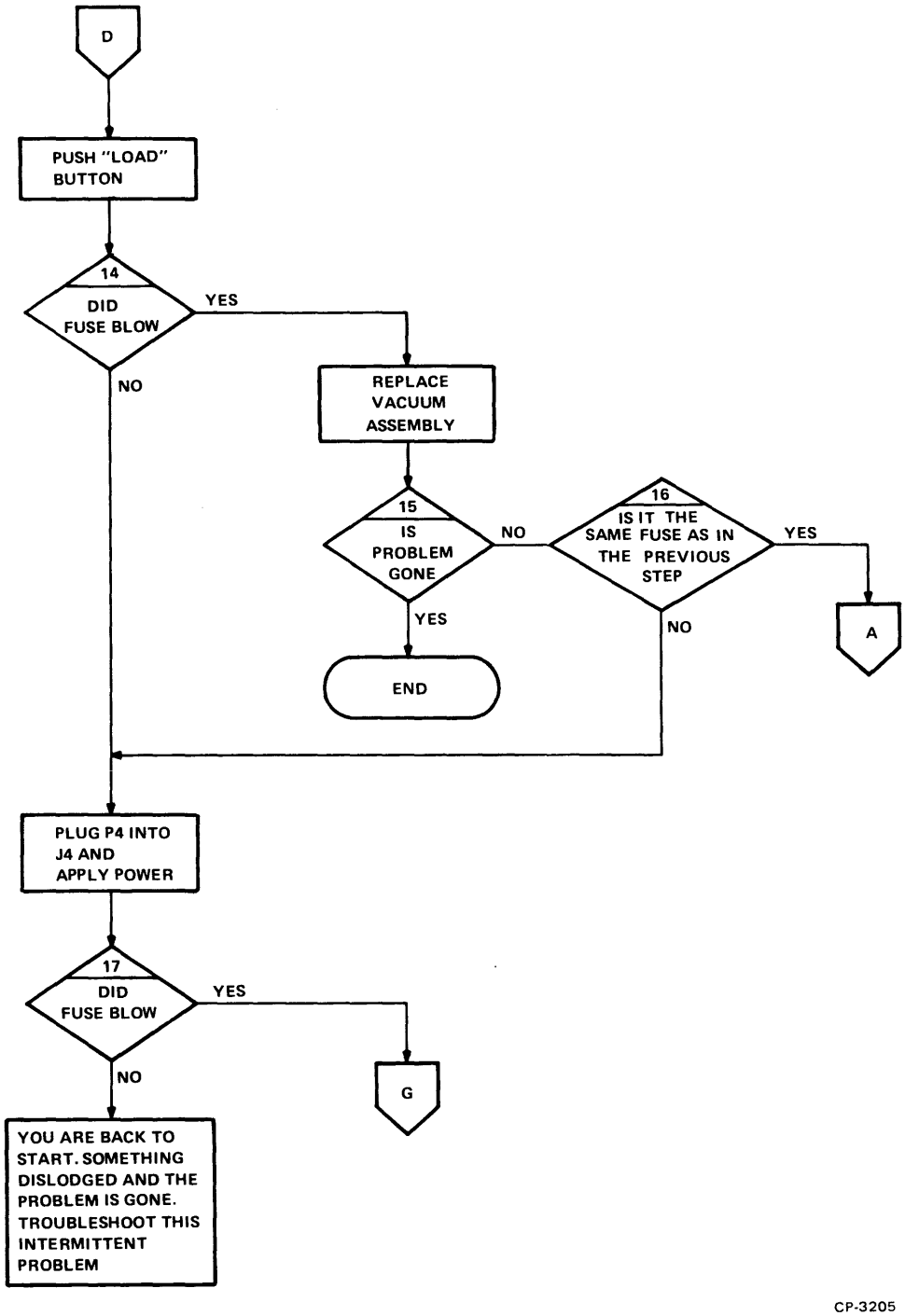


Figure 6-70 Fuse Troubleshooting Chart (Sheet 4 of 7)

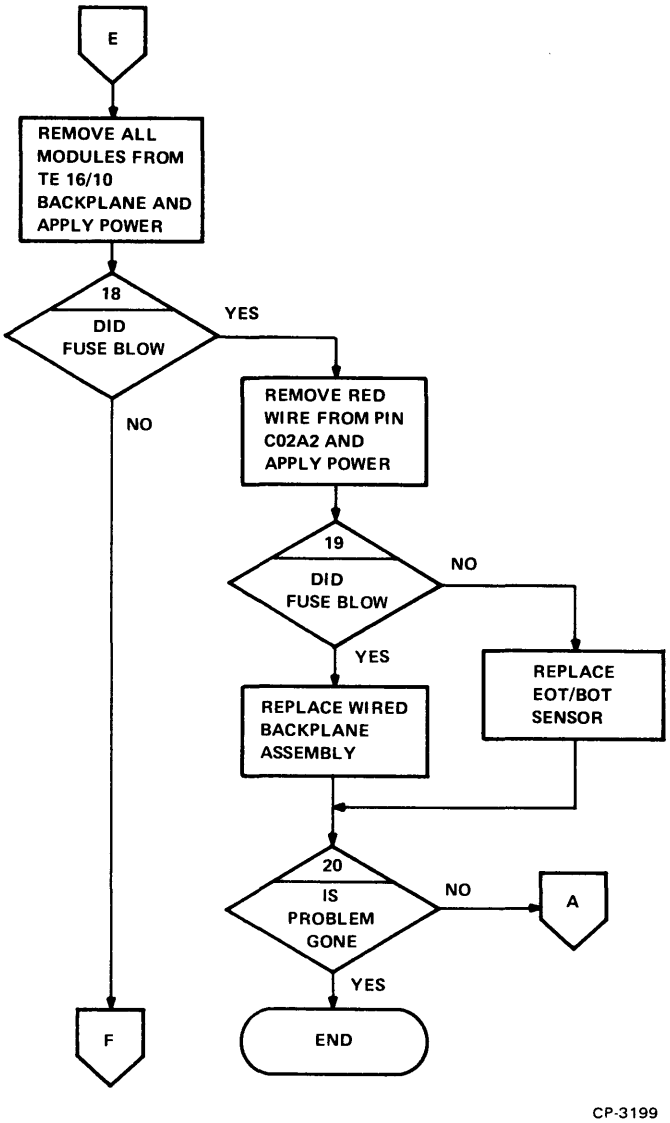


Figure 6-70 Fuse Troubleshooting Chart (Sheet 5 of 7)

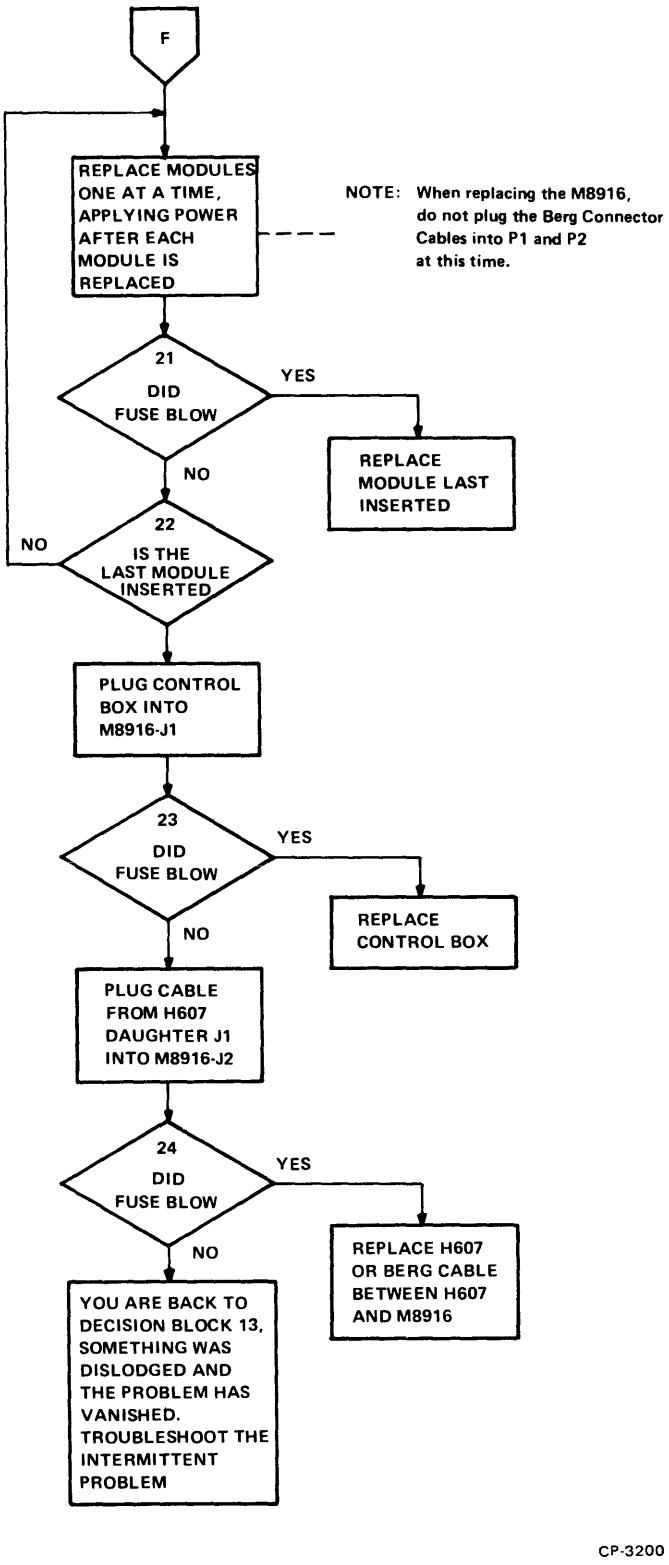


Figure 6-70 Fuse Troubleshooting Chart (Sheet 6 of 7)

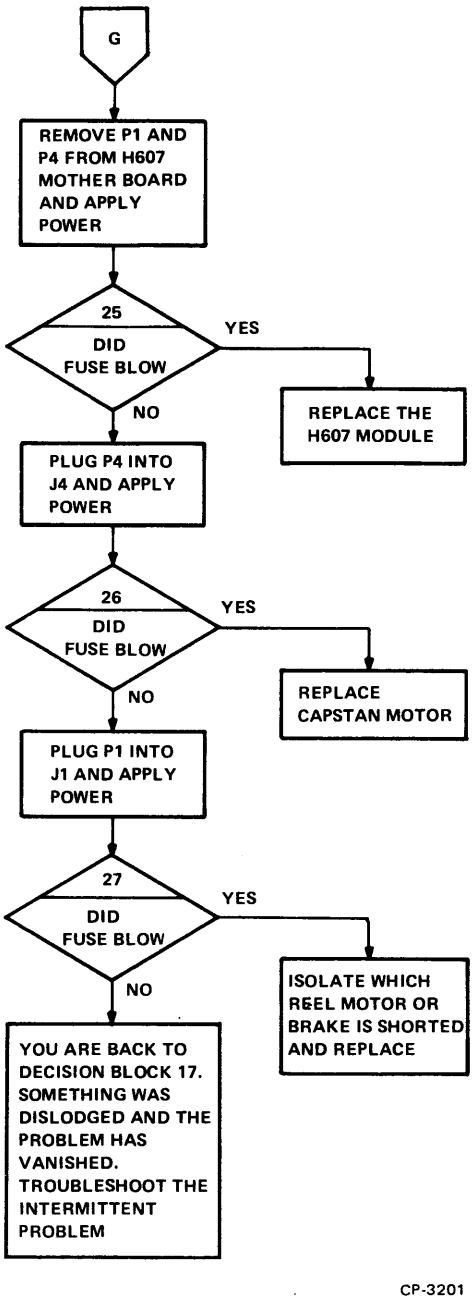


Figure 6-70 Fuse Troubleshooting Chart (Sheet 7 of 7)

Only When Tape Motion Occurs – If a particular fuse blows every time a motion command is given (on- or off-line) and conventional troubleshooting methods are exhausted, the following subassemblies should be considered for replacement:

H607
M8916
Berg cable going from M8916-J2 to H607 (daughter) J1
Reel motors
Capstan motor
Brakes

6.7.5 Troubleshooting with Off-Line Write Operations

When performing off-line write operations with the TFG (M8912) module, five signals do most of the testing. If there is no analog signal at all when performing an off-line write operation, check the items listed in Table 6-14. If only a few channels (signals) are missing, check the signals listed in Table 6-15.

Table 6-14 Signals to Check When All Channels are Dead

Signal	Source	What to Look For
Write Voltage	C02J2, K2 (orange wire)	+12 V in NRZI mode and +5.6 V in PE mode
CLK L	D03C1	900 ns clock
REC PLS L	D03L2	With M8912 S5–9, 10 on, one low-going pulse every 40 μs
SKEW CLOCK A	A02B1	900 ns pulse every 40 μs
SKEW CLOCK B	A02L1	900 ns pulse every 40 μs
SKEW CLOCK C	A02N1	900 ns pulse every 40 μs
SKEW CLOCK D	A02R1	900 ns pulse every 40 μs
Test Data Inputs	Ref. D-CS-M8916 sheets 1 and 2	Check all inputs for low logic levels (less than 0.8 V). If the test data inputs are high, the transport will write all 0s in all tracks.

NOTE
All of the above checks are to be made with the TFG module (M8912) in slot AB03 and the WRT SW in the up position.

If all these signals are present, the only remaining possibilities are: a bad head, head cable, or M8916 module.

Table 6-15 Signals to Check When Some Tracks Are Missing

Test Point	Pin
Track 1	B02C1
Track 2	B02B2
Track 3	B02F1
Track 4	A02P1
Track 5	A02S1
Track 6	A02T2
Track 7	A02V1
Track 8	A02B1
Track 9	A02A1

NOTES

1. **For each track, make sure that the associated clock skew jumper is properly wire wrapped.**

2. **For each track, make sure that the data coming from the multiplexers is at a logic high.**

Table 6-16 Trouble Analysis of Data Reliability Diagnostic

Problem	Remedy
Runaway: A runaway condition exists when the program starts and depressing the HALT key does not stop tape motion.	
Symptoms:	
No CLOCK (SB) L(144 kHz, 7 μs period) on wire wrap pin D01E1. (See sheet 2 of M8911 schematic.)	Check for bad cable. Check for bad cable connector card. Check for bad M8911. Check for wire wrap pin short. Check that jumper is installed on M8911. Check M8911. Check M8913YA.
Pin D01E1 stays at ground level.	Check for bad cable. Check for bad cable connector card. Check for bad M8911. Check for wire wrap pin short.
Pin D01E1 stays at a logic level (approximately +0.3 to +3.4 Vdc).	Check that jumper is installed on M8911. Check M8911. Check M8913YA.

Table 6-16 Trouble Analysis of Data Reliability Diagnostic (Cont)

Problem	Remedy
No CLR READ BOARD L on pins C03V1 and C04J1: Approximately 12.5 ms after SET pulse, a series of 100 ns negative going pulses should appear on pins C03V1 and C04J1. These pulses should be 28 ms apart and within 0.5 V of ground.	Check C03V1 and C04J1 for shorts. Check the following G066 output pins for shorts: A04B1 A04F1 B04F1 B04K1 C04P1 C04R1 D04V1 E04E1 F04K1 Replace or repair M8911.
G066 outputs stay low and will not reset.	Replace or repair G066.
Unsafe (UNS) error bit asserted in the error register (TE16 only): Unsafe error indicates that the formatter attempted to execute a command with a TE16 that was not on-line or that the formatter itself is faulty.	Check that TE16 is on-line.
Symptoms: Check MOL(SB)L at pin F01V2 for +0.2 to +0.4 Vdc. (See sheet 4 of M8916 schematic.)	Check that cable connector cards are not loose. Check that cables are routed correctly. Check cables. Check cable cards. Check formatter.
MOL is low.	Check that cable connector cards are not loose. Check that cables are routed correctly.
Set the TE16 to off-line mode. MOL does not go to +3 Vdc.	Check cables. Check cable cards. Check formatter.
On-line mode is selected at the switch box but the TE16 goes off-line when the program is started.	Trouble is in formatter. Replace M8916.
REWIND(SB)L on pin C01P2 stays low.	Trouble is in formatter.
REWIND(SB)L on pin C01P2 changes state.	Replace M8916.
Operation Incomplete (OPI) error	Run TE16 Utility Driver Diagnostic. Go to Paragraph 6.7.7.

6.7.6 Troubleshooting Using the Data Reliability Diagnostic Program

When troubleshooting nondata transfer problems, reference Table 6-16 for runaway, UNS, and OPI errors. When troubleshooting NRZI mode problems, run the TE16 (or TE10) Data Reliability Program using pattern 1 (all 1s), 800 bits/in NRZI, 20 char/record. Reference Table 6-17 and Figures 6-71 and 6-72 to analyze the results.

NOTE

If an OPI error occurs with a VPE error, troubleshoot the OPI error first. This type of problem is usually caused by too few RSDO pulses.

Table 6-17 Trouble Analysis of Data Reliability Diagnostic Using Pattern 1

Problem	Remedy
CRC and LRC errors	Check gain adjustment of G066.
Symptoms:	
1. Look for a dead channel by letting the program run until some error printouts are obtained.	Check the WD line of the dead channel with an oscilloscope triggered from the REC line. The waveform of Fig. 6-71 should be obtained.
If the error printout resembles CRC 377-777 LRC 377-777 the parity channel is dead.	Check G066. Check read head cable. Check read head. Repair or replace M8916. Check write head cable. Check write head. Check RD line. Check M8911 and cables. Check G066 and cables. Check M8913 and cables.
If the error printout resembles BN: 20 G 377 B 357 a dead channel exists.[1]	
2. Analog signal for dead channel[2] is missing or distorted. Check analog signals (Fig. 6-72A) on pins A04L1, B04B1, B04M1, C04K1, C04L1, D04P1, D04R1, F04P1, and F04R1. Mount a skew tape and check the read channel (Fig. 6-72B) on pins A04B1, A04F1, B04F1, B04K1, C04P1, C04R1, D04V1, E04E1, and F04K1.	Repair or replace M8916. Check write head cable. Check write head. Check RD line. Check M8911 and cables. Check G066 and cables. Check M8913 and cables.

Table 6-17 Trouble Analysis of Data Reliability Diagnostic Using Pattern 1 (Cont)

Problem	Remedy
3. Read channel is bad.	Check G066. Check read head cable. Check read head.
4. Read channel is good.	Repair or replace M8916. Check write head cable. Check write head. Check RD line. Check M8911 and cables. Check G066 and cables. Check M8913 and cables.
CRC, LRC, and VPE errors without data errors	Check for "clean" analog signals (Fig. 6-72A). Check that the data pulses are approximately 10 V p-p. Check that the CRC and LRC pulses are less than 5 V above and below ground. Check pin E04K1 for the packet waveform shown in Fig. 6-72C, D. Ensure that each pulse is less than 2 μs wide and that pulses occur every 28 μs. Check that logic "highs" are greater than +2.4 Vdc and all logic "lows" are less than +0.8 Vdc.
Nonexecutable Function (NEF) error Symptoms: 1. The Phase Encoded Status Signal (PESB) signal is incorrect. The signal should be +3 Vdc for density 0, 1, 2, and 3, and 0 volts for density 4, 5, 6, and 7.	Check that WRL (Write Lock) at pin F01K2 is at +3 Vdc.[3] Check that DEN lines are in correct state. Check that 7 CH is not floating.
Nonstandard Gap (NSG) error Excessive number of RSDO pulses are being generated.	Check read circuitry.
Format error (FMT) Format code formatter control register (bits 4, 5, 6, and 7 of location 172432) is not 14.	Stop and restart the program and retype the format code.

Table 6-17 Trouble Analysis of Data Reliability Diagnostic Using Pattern 1 (Cont)

Problem	Remedy
Illegal Tape Mark (ITM) error	Check for system fault. Check for bad tape. Check data channels 0, 1, and 4.
When the program starts, check the response to TM = 0.	
Typed response is 0 or RETURN.	Check for system fault.
Typed response is 1.	Check for bad tape.
Typed response is 1, and ITM is printed more than once.	Check data channels 0, 1, and 4.
Frame Count (FCE) error.	
Error occurs at end of read operation.	Check for 18 RSDO pulses.
Error occurs at end of write operation.	Trouble is in formatter or Massbus controller.
Drive Timing Error (DTE) Data Bus Parity Error (DBPE) Control Bus Parity Error (CBPE) Register Modification Refuse (RMR) Illegal Register (ILR) Illegal Function (ILF)	Trouble is in formatter, controller, or processor.

1. To determine which channel is dead, convert the G and B numbers, which are in octal, to binary.

   Channel 4 Channel 0
   G = 377 = 011 111 111
   B = 357 = 011 101 111

   Channel 0 is the least significant (right-most) bit. In the above example, channel 4 is dead.

3. If WRL is at ground, a write-lock condition will exist and it will be impossible to execute a write command. Refer to the M8916 circuit schematic.

Table 6-17 Trouble Analysis of Data Reliability Diagnostic Using Pattern 1 (Cont)

Problem	Remedy
2. Convert the data channel number to the physical track number as follows:	

Data Channel No. = Physical Track No.

P	4
7	7
6	6
5	5
4	3
3	9
2	1
1	8
0	2

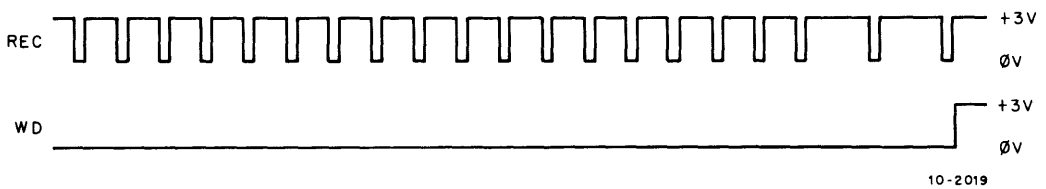


Figure 6-71 REC and WD Signal Waveforms

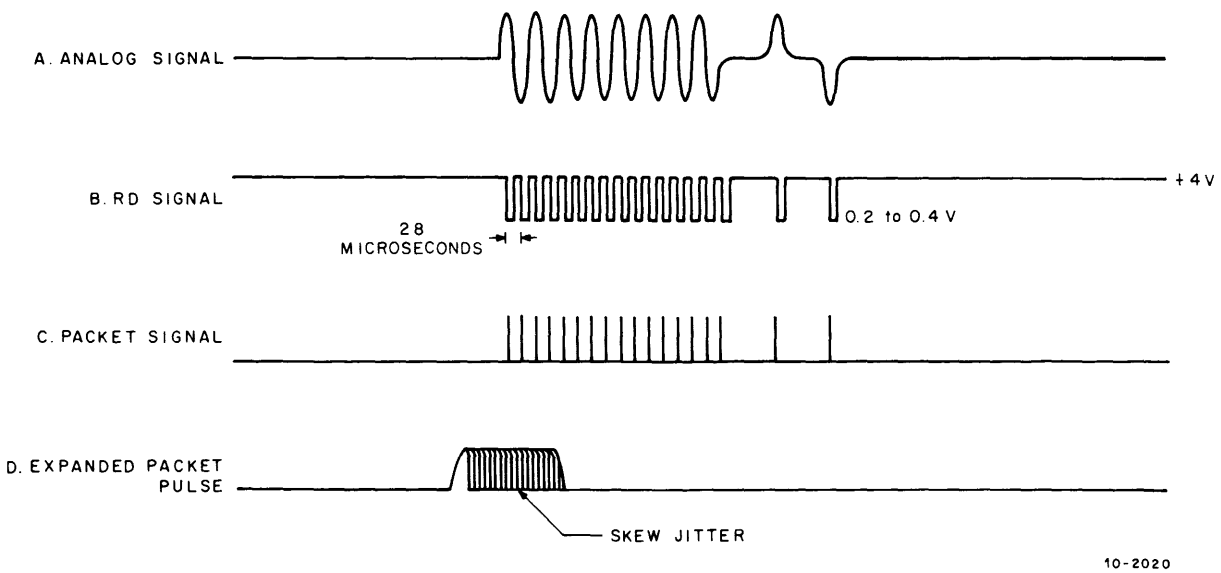
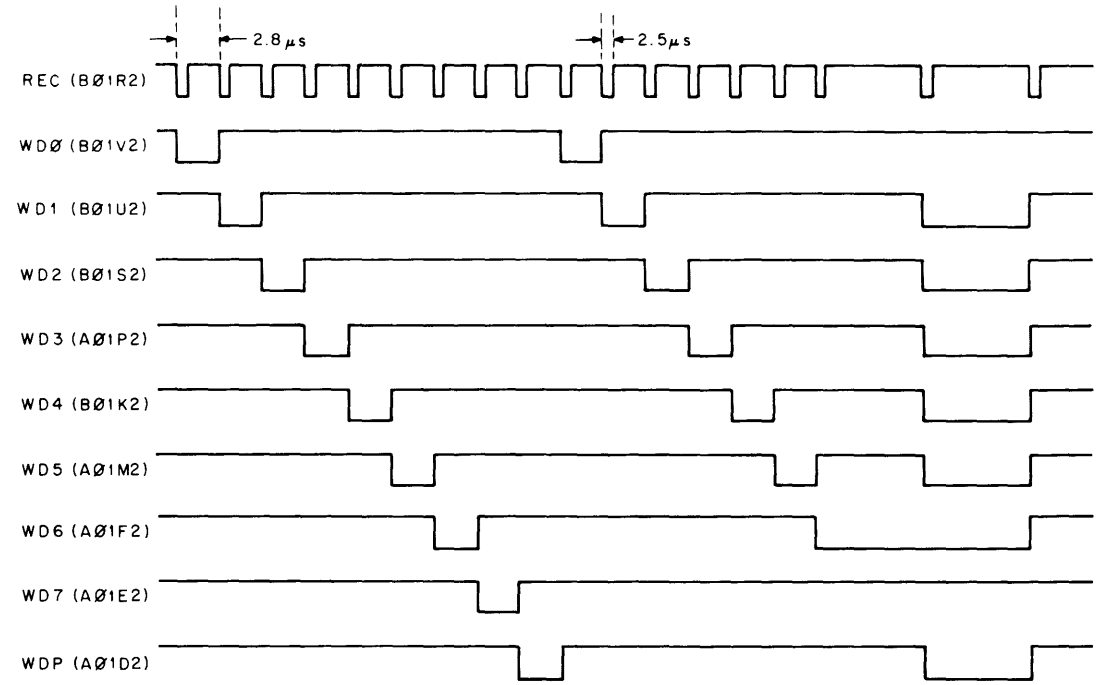


Figure 6-72 Read Signals

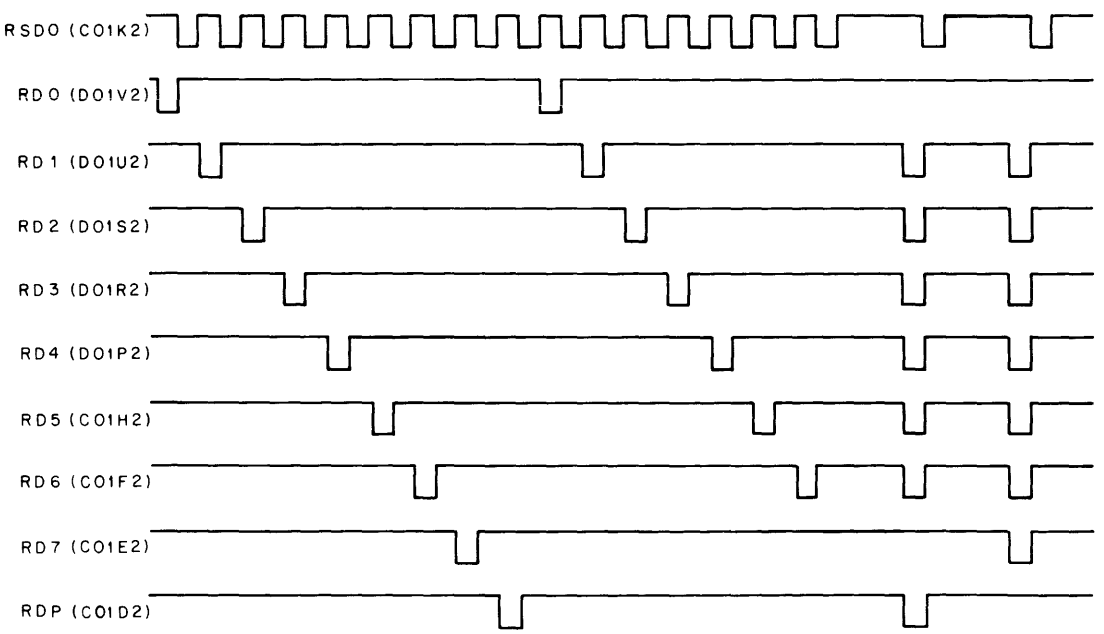
If the trouble is not located, change the pattern to Pattern 3 (rippling 1s) and rerun the diagnostic program. Reference Table 6-18 to analyze the results. When troubleshooting PE mode problems (TE16 only), reference Table 6-19, for help in troubleshooting Phase Encoded Data Reliability errors.

Table 6-18 Trouble Analysis of Data Reliability Diagnostic Using Pattern 3

Problem	Items to Check	Remedy
Grounded RD or WD line	Check printout as follows to locate bad channel. CN: 1 Channel 0 G 0 0 0 0 0 0 1 0 B 0 0 0 0 0 0 1 1 CN: 2 G 0 0 0 0 0 1 0 0 B 0 0 0 0 0 1 0 1 CN: 3 G 0 0 0 0 1 0 0 0 B 0 0 0 0 1 0 0 1 Note that for each B (bad data) printout, channel 0 is a one (1). This indicates that either RD0 or WD0 is shorted to ground.	Check RD and WD of faulty channel for short to ground.
Data lines tied together	Check printout as follows to locate data lines. CN: 1 Channel 6 Channel 1 G 0 0 0 0 0 0 1 0 B 0 1 0 0 0 0 1 0 CN: 6 G 0 1 0 0 0 0 0 0 B 0 1 0 0 0 0 1 0 CN: 17 G 0 0 0 0 0 0 1 0 B 0 1 0 0 0 0 1 0 Note that for each B (bad data) printout, channels 1 and 6 are always the same. This indicates that WD1 and WD6 are tied to each other.	Check on slave bus (cable A) for connection between two data lines indicated by printout.
Intermittent errors on data channel 0.	Error printout indicates that data channel 0 is intermittent.	Check that both ends of cables A and B are correctly installed. Using an oscilloscope, check for the wave shapes of Figure 6-73.



A. WRITE SIGNAL WAVEFORMS USING NEGATIVE EDGE OF REC(SB) L FOR SCOPE TRIGGER



B. READ SIGNAL WAVEFORMS USING NEGATIVE EDGE OF RSDO FOR SCOPE TRIGGER

NOTES:

1. When checking these waveforms, put PDP-11 keys 2, 3, 10, 11, 12, and 13 up. Keys 2 and 3 cause a foward write. Keys 10 through 13 inhibit error checking and printout.
2. Record count = 1; character count = 20_8; switches 2 and 3 up.
3. Set oscilloscope for 0.1 ms/cm.

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Figure 6-73 NRZI Signal Waveforms Using Pattern 3 and 800 bits/in.

Table 6-19 Troubleshooting Phase Encoded Mode

Problem	Remedy
FCE CORR skew and CORR data Symptoms: Postamble detected too soon.	Check formatter or Massbus controller.
One track is missing.	Check for damaged tape.
NSG error	Check for poorly written tape. Check G066.
During a read operation one or more channels of read data completes a record in the wrong state; e.g., overshoot on the last transition being recognized as an extra transition.	
Some unerased data left in the IRG.	Check for misaligned erase head.
PEF, CDE, INC errors	Check tape for dirt and defects. Check for capstan jitter. Check G066. Check formatter.
Incorrectable data error with all zeros in check character register and no CS/ITM error.	
Parity error exists with no dead track.	Check formatter.
Check character register repeatedly contains the same bit set.*	
Trouble is in only one track. Swap data sync modules in formatter.	Check analog and digital outputs of G066. Check data sync module in formatter.
Trouble is in same track.	Check analog and digital outputs of G066.
Trouble is in different track.	Check data sync module in formatter.
PEF error	
More than one dead track due to improper detection of preamble and postamble.	Check for poor quality tape. Check tape speed regulation.
Records are being written improperly	Check M8916 (head drivers). Check +5 V (PE) write voltage. Check formatter.

*A 777 in the check character register may indicate a late detection of postamble which causes the check character register to be strobed at the wrong time.

6.7.7 Troubleshooting Using the TE16 Utility Driver Diagnostic

An OPI error occurring in the TM02/TE16 Data Reliability Program diagnostic of Paragraph 6.7.6 can be caused by any of the following:

- SET PULSE is not sent to the TE16.
- Write circuitry fails to write on tape.
- Read circuitry fails.

To troubleshoot an OPI error, run the TE16 Utility Driver Diagnostic by performing the following steps:

1. Load the TE16 Utility Driver Diagnostic.
2. Set the following program parameters:

Density	800 bits/in
Word Count	10_8
Frame Count	20_8
Data Pattern	All ones
Operation	Write

3. Check that the TE16 is loaded at BOT and is on-line.
4. The tape should move forward.

Refer to Table 6-20 to analyze the results of the Utility Driver Diagnostic.

Table 6-20 Trouble Analysis of Utility Driver Diagnostic

Problem	Remedy
Tape does not move. Symptoms: Put HALT ON ERROR switch up (bit 15) to cause the program to pause. Wait for the RUN indicator to go out.	Check the formatter error register for set-up errors. Check the SET PULSE line for shorts. Check for faulty M8916. Check for bad cable. Check for faulty M9001.
Restart the program.	Check pin A01S2 for SET PULSE (Fig. 6-74A and sheet 5 of M8916 schematic). Check FWD at pin C01V2 for a low (0 V). Check REV at pin C01V2 for a high (+3 V). Check WRITE at pin D01D2 for a low (0 V). Check REWIND at pin C01P2 for a high (+3 V). Check for bad cables. Check for bad cable card connectors. Check M8916.
TE16 SEL indicator is not lit.	Check the following signals for a high level (+3 Vdc) (Fig. 6-74B). SEL 0 Pin B01H2 SEL 1 Pin B01P2 SEL 2 Pin B01M2 STOP Pin A01V2 INIT PLS Pin A01U2 DRV CLR Pin B01D2
Tape moves and REC pulses (pin B01R2) are present (Fig. 6-75).	Check cable. Check cable card connector. Check that EMD pulse on pin B01E2 goes low for 2.8 or 42 ms after SET PULSE and then goes high.
Signal is low	Check M8916.
The 144 kHz pulse train CLOCK is not present on pin D01E1.	Check M8911/M8931.
ACCL (SB) L on pin A01H2 should go low (0 V) for approximately 9.5 ms after SET PULSE and then go high (+3 Vdc). ACCL never goes high.	Check that data lines RD0, RD1, RD2, RD3, RD4, RD5, RD6, RD7, and RDP are between +3.5 and +4.5 Vdc. (Some RD lines may go low when the SET PULSE occurs, but most of them should remain high.)

Table 6-20 Trouble Analysis of Utility Driver Diagnostic (Cont)

Problem	Remedy
Symptoms: WRITE CLOCK is missing.	Check M8911/M8931.
No analog signals on Pin A04L1 (Figs. 6-74E and 6-76).	Check the write cable. Check M8916 (see Sheets 1 and 2 of M8916 schematic); write amplifiers.
Symptoms: Tape moves and REC pulses are present.	Check that WRITE CLOCK jumpers are properly connected to back panel. Check that write buffer is being clocked. Check that write voltage (orange wire) is approximately +12 Vdc (+5.5 Vdc for PE or off-line mode). Check that the following wires to G066 are at the specific voltages: Red = +5 Vdc Yellow = +12 Vdc Green = -6 Vdc Check the read and write cables. Check that the WD lines (WD0, WD1, . . .) go low (0 V) for approximately 400 μs during the period when REC pulses occur.
No RSDO pulses on pin C01K2 (Figs. 6-74F and 6-77). Tape moves, REC occurs, and analog signals are present.	Check that all RD lines on G066 go low. Check for 100 ms CLEAR RD BRD L pulse on pin C03V1 (see Sheet 3 of M8911 schematic). Check for back panel wiring shorts.
OPI error remains. Tape moves, REC occurs, analog signals are present, and RSDO pulses are present.	Replace or repair M8913 and cable B. Troubleshoot formatter.

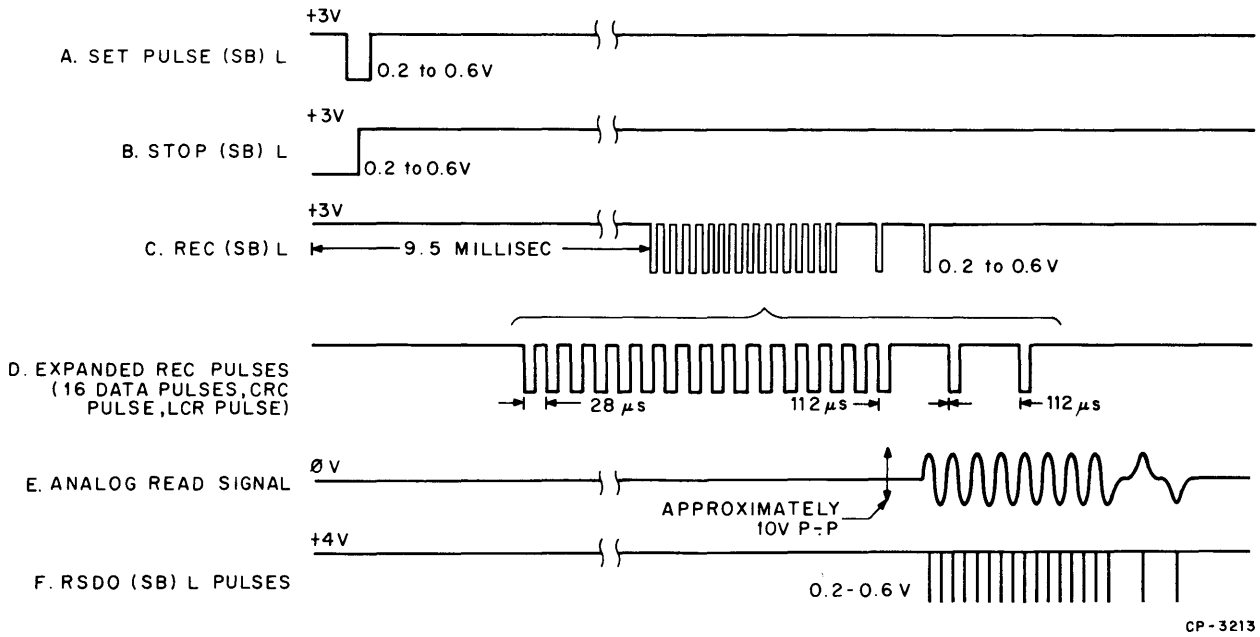
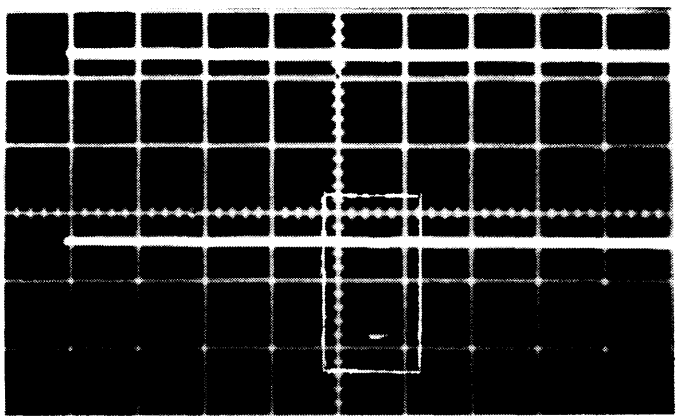


Figure 6-74 Time Relationships of Write Operation Signals

VERTICAL = 2 V/CM

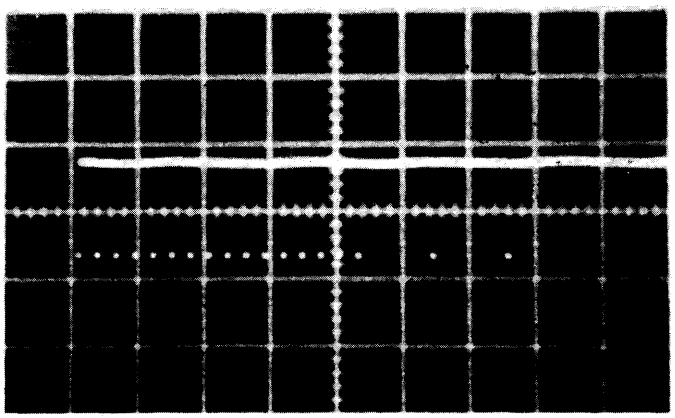


Note: REC Pulses in box

A. SWEEP SPEED = 2 MS/CM
TRIGGER = SET PULSE

M-0754

VERTICAL = 2 V/CM

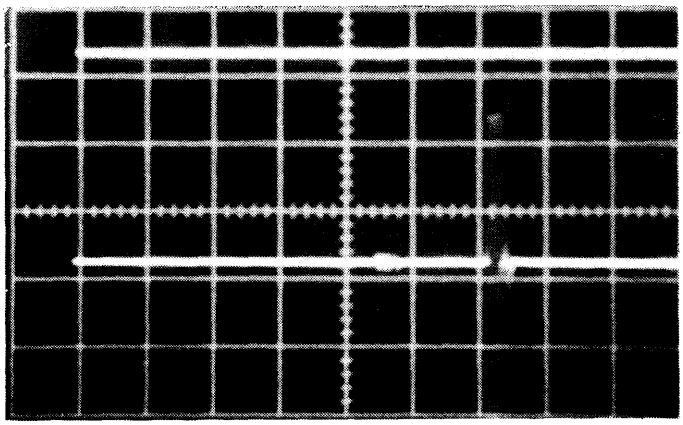


B. SWEEP SPEED = 0.1 MS/CM
TRIGGER = FIRST REC PULSE

M-0755

Figure 6-75 Waveforms of REC Pulses (16 data pulses, CRC pulse, LRC pulse)

VERTICAL = 2 V/CM

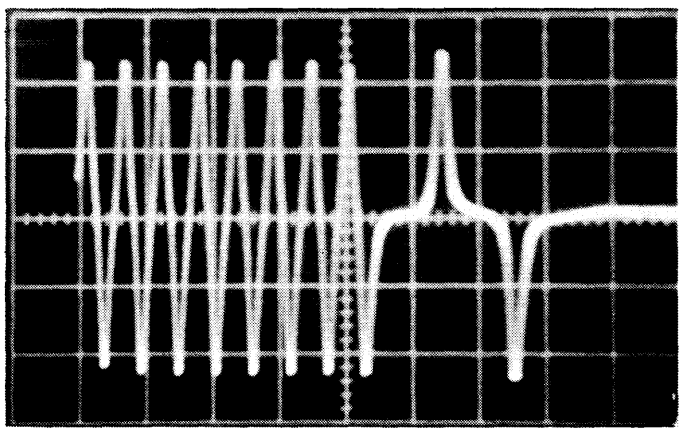


Note write crosstalk 9 ms from start of trace.

A. SWEEP SPEED = 2 MS/CM
TRIGGER = SET PULSE

M-0756

VERTICAL = 2 V/CM



B. SWEEP SPEED = 0.1 MS/CM
TRIGGER = FIRST ANALOG SIGNAL

M-0757

Figure 6-76 Waveforms of Analog Read Signals

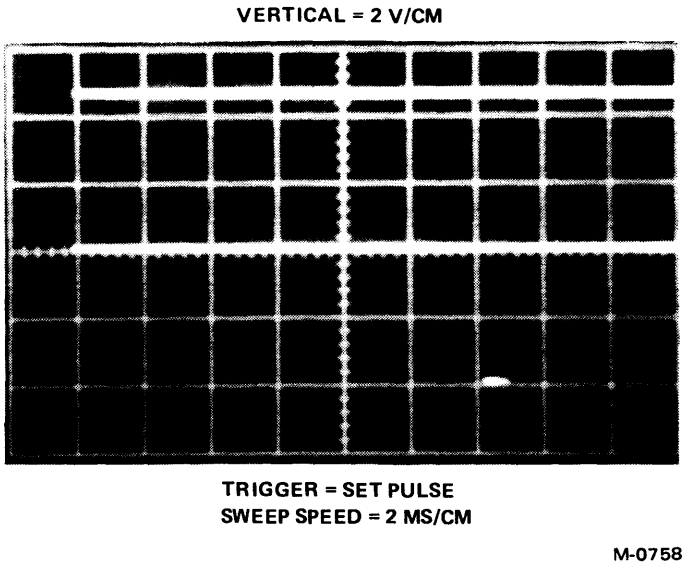


Figure 6-77 Waveform of RSDO Pulses

6.7.8 Use Of The Drive Function Timer

Load and start the Drive Function Timer Program. If an error occurs, allow two or three printouts and put the "continue on error" switch up until the next test begins; then, put it down. Continue this until one complete pass of the program has run. In this manner, an error typeout for each failing test will be obtained. The remainder of this section describes possible causes and corrections of each failed test.

1. **Write From BOT** - If this is the only test that fails, the probable fault is the M8911 Delay ROM. If other tests fail, check that pin D03F2 on the TE16 back panel is not shorted to some other signal. This pin should be open. Also, check that CLOCK (SB) L on pin D01E1 is a 144 kHz square wave. All printed times can be out of range, if this frequency is incorrect. Section 1 failure can also be caused by a faulty read data (RD) line on cable B or by a marginal EMD line on cable A.

   Bad RD lines would result in data errors, write errors, and read errors with other diagnostics. A bad EMD line might only be detected by Drive Function Timer.

2. **Write Start** - Go to Paragraph 1.

3. **Write Shutdown** - Make the same checks as in Paragraph 1, but also note the printout of Paragraphs 23 and 24 (Data Time, 200 bits/in and 556 bits/in). A frequent cause of failure of Paragraph 3 is a "hung" density line, particularly DEN 0 (SB) L. It should be +0.2 to 0.4 V. Also check tape speed.

4. **Write Settle Down** – This test checks the timing of a one-shot delay on the M8916 (refer to sheet 5, upper left-hand section of the M8916 circuit schematics). This failure usually indicates a bad IC or out-of-tolerance capacitor. Changing the M8916 should fix this problem.

5. **Read from BOT** – Go to Paragraph 1.

6. **Read Start** – Go to Paragraph 1.

7. **Read Shutdown** – Go to Paragraph 3.

8. **Read Settledown** – Go to Paragraph 4.

9. **Read Reverse Start** – Go to Paragraph 1.

10. **Read Reverse Shutdown** – Go to Paragraph 3.

11. **Read Reverse Settledown** – Go to Paragraph 4.

12. **Turn Around F-R** – This test measures the time-out duration of the settle-down one-shot delay with the time-out of the read start delay. If this test fails without Paragraphs 8 and 9 failing, the formatter or controller is probably at fault.

13. **Turn Around R-F** – This test is the sum of Paragraphs 6 and 11. Go to Paragraph 12.

14. **Gap Size-Stop Half** – This test checks start/stop ramp times. If other tests fail, repair them first, particularly Gap Size Interrecord, Paragraph 16. If this test is the only test that fails, check forward/reverse start/stop times.

15. **Gap Size-Start Half** – Go to Paragraph 14.

16. **Gap Size Interrecord** – This test checks tape speed. If other tests fail, repair them first. If this test is the only test that fails, check tape speed with a skew tape.

17. **Gap Consistency** – Go to Paragraph 12.

18. **Data Time 200 bits/in** – The most probable cause of failure of this test is a "hung" density line. Check that when the three density bits in the control register are 0, the three DEN (SB) lines are also 0.

19. **Data Time 556 bits/in** – Identical to Paragraph 19, except DEN 0 (SB) is true.

20. **Data Time 800 bits/in** – Identical to Paragraph 19, except DEN 0 (SB) and DEN 1 (SB) are both true.

21. **Data Time 1600 bits/in** – Identical to Paragraph 19, except DEN 2(SB) is true.

22. **Erase** – Go to Paragraph 1.

23. **Tape Mark** – Go to Paragraph 3.

6.7.9 Cable/Wire Harness Troubleshooting

Included in this section are the various cable and wire harness locations. Use this information to verify correct placement of cables and harnesses.

1. **EOT/BOT Sensor** - Check that the BOT/EOT sensor is wired correctly, as follows:

   Red wire to pin C02A2
   Orange wire to pin C02D1
   Yellow wire to pin C02C1
   Brown wire to pin C02L2

2. **Maintenance Panel Harness** - Check that the maintenance panel harness is wired correctly, as follows:

   Red wire to pin F02E2
   Green wire to pin F02D2
   Yellow wire to pin F02F2
   Brown wire to pin F02C1
   Black wire to pin F02C2

3. **Fail-safe Switches** - Check that the Fail-safe switches are wired correctly, as follows:

   White/Yellow wire to pin C02U1
   Green wire to pin C02U2

4. **Power Supply Connections** - Referring to Figure 6-78, check that the wiring harness is connected correctly to the power supply regulator board. Also, check that the power cord and transformer taps are installed correctly.

5. **Control Box Cable** - Check that the flat cable from the control box is plugged into the bottom of the M8916. Connect the 50.8 cm (20 in) piece of flat cable from J1 on the H607 logic board to the jack of the side of the M8916. Finally, connect the short 12.7 cm (5 in) piece of flat cable from the H607 logic board to the H607 power board.

NOTE

Be careful. When connecting the flat cables, be sure that the smooth side of the cable is always facing up from the board.

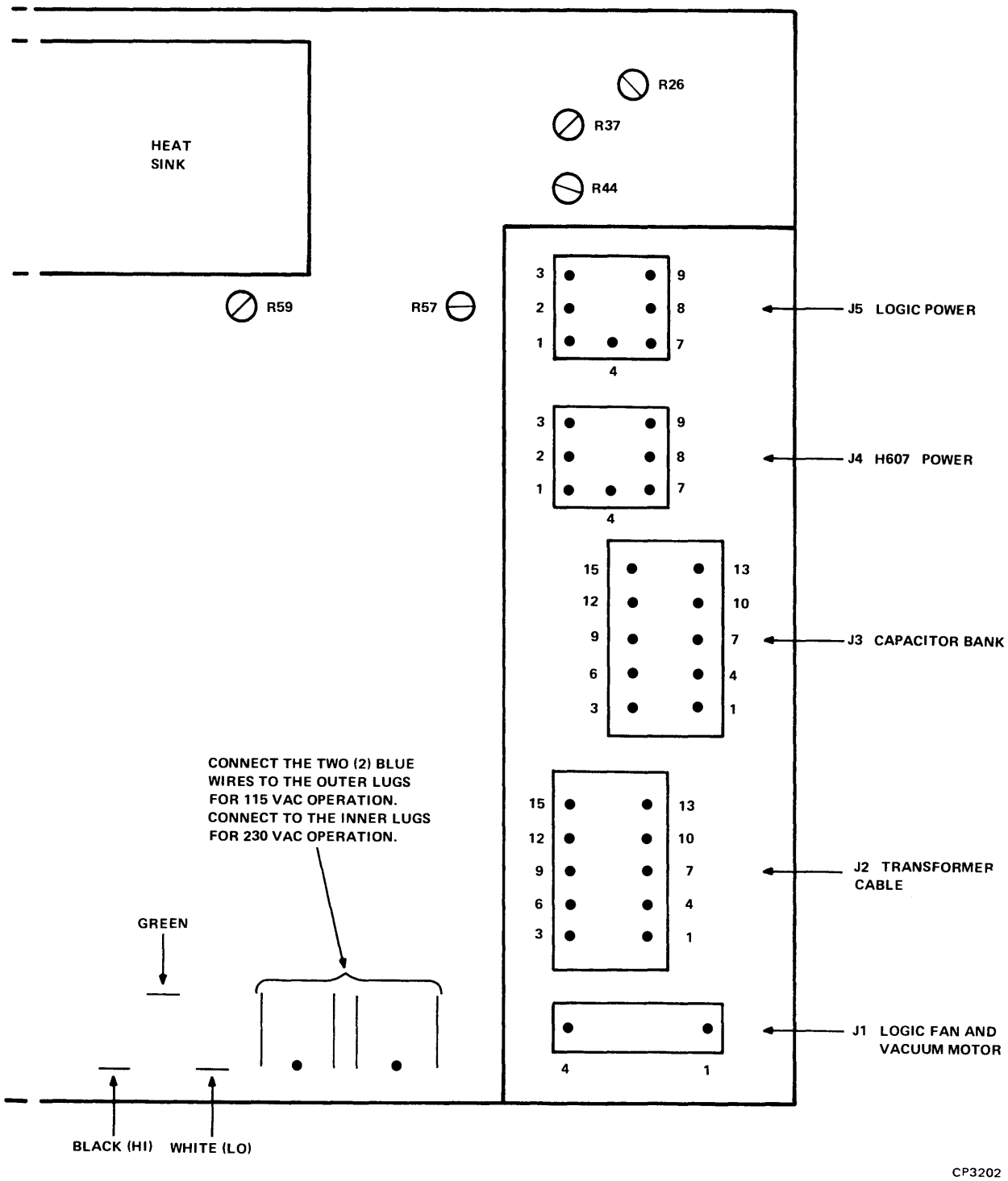


Figure 6-78 Wiring Harness to Power Supply Connections

APPENDIX A
MAGNETIC TAPE FUNDAMENTALS

A.1 DEFINITIONS

1. Reference Edge – The edge of the tape as defined by Figure A-1. For tape loaded on a tape transport, the reference edge is toward the observer.

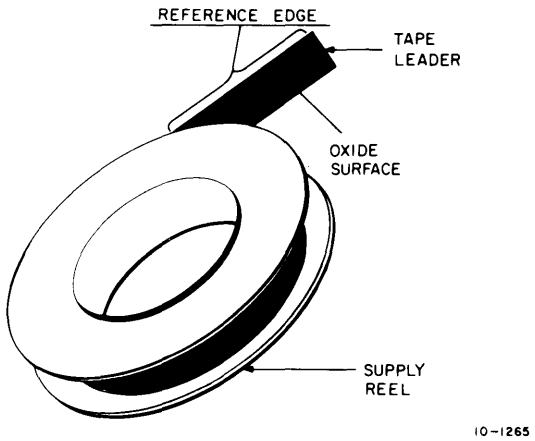


Figure A-1 Reference Edge of Tape

2. BOT (Beginning-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the reference edge, 457 cm ± 30.5 cm (15 ft ± 1 ft) from the beginning of the tape.

3. EOT (End-of-Tape) Marker – A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 762 to 914 cm (25 to 30 ft) from the trailing edge of the tape.

4. 9-Channel Recording – Eight tracks of data plus one track of vertical parity. Figure A-2 shows the relationship between track and bit weight for a 9-channel transport.*

*When the track vs. bit channel standard was adopted, the outer tracks were more susceptible to bit dropping errors. Consequently, channels containing the least 1s were assigned the outer locations on the tape.

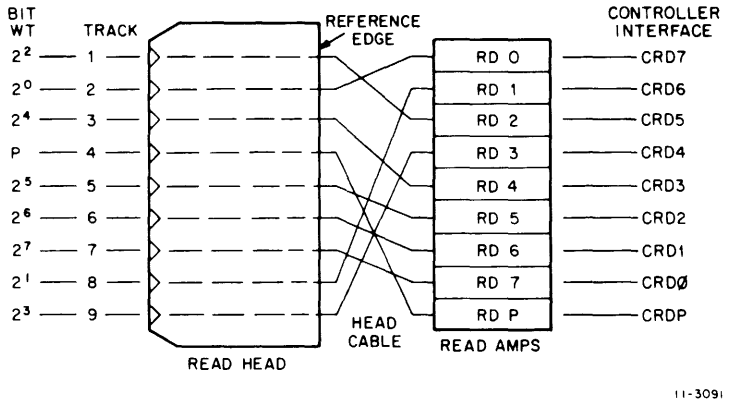


Figure A-2 Track-Bit Weight Relationship for 9-Channel Transport

5. Tape Character - A bit recorded in each of the nine channels.

6. Record - A series of consecutive tape characters.

7. File - An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) - A length of erased tape used to separate records [1.27 cm (0.5 in) minimum for 9-track; maximum IRG is 762 cm (25 ft)].

9. Extended IRG - A length of erased tape [7.62 cm (3 in) minimum] optionally used to separate records.

10. Tape Speed - The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density - The density of sequential characters on the tape. It is normally specified in bits per inch (bpi), which is equivalent to characters per inch.

12. Write Enable Ring - A ring that must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

13. Tape Mark (TM) - A record written on the tape to designate the end of a file; sometimes referred to as file mark (FMK).

A.2 RECORDING METHODS AND MAGNETIC TAPE FORMATS

A magtape system is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows called characters. Each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program-selected as even or odd. The odd parity bit guarantees that each character records at least one 1 bit.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even. For example, if odd parity is used and the character contains an even number of 1 bits, the parity bit is generated as a 1 bit and an odd number of 1 bits are recorded; then, if an even number of bits are read back from tape, a vertical parity error is generated to notify the program that the data is in error.

The data characters are recorded in blocks of characters termed records (Figure A-3). Each record contains a specified number of characters determined by the word count.

Records are separated by interrecord gaps (IRGs). The IRG is 1.27 cm (0.5 in) minimum [approximately 1.5 cm (0.6 in) in normal operation], but may be extended to 7.62 cm (3 in) by performing an extended gap operation. Tape IRGs (unrecorded areas) provide areas on the tape for the transport to start or stop and also separate data records.

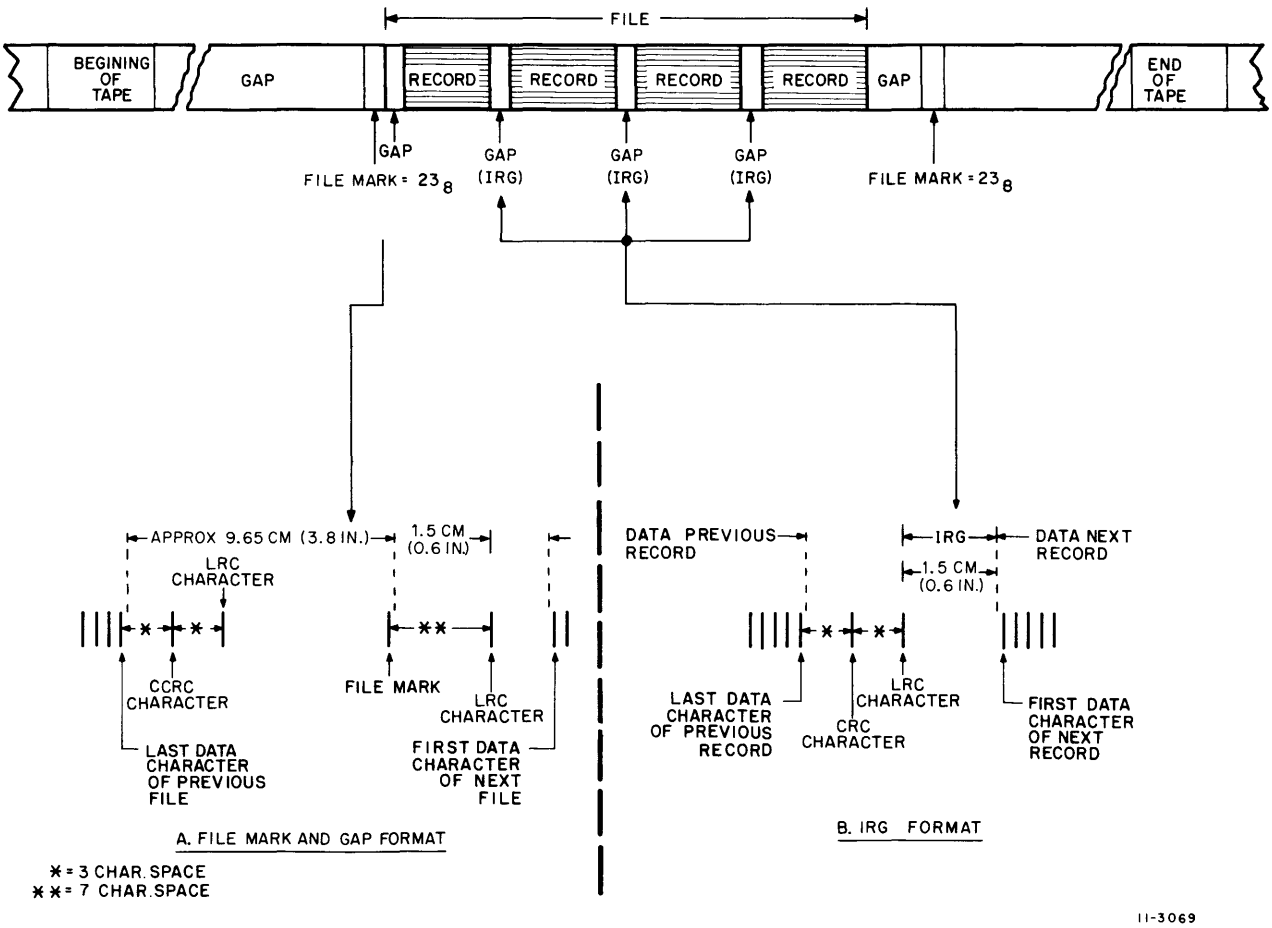


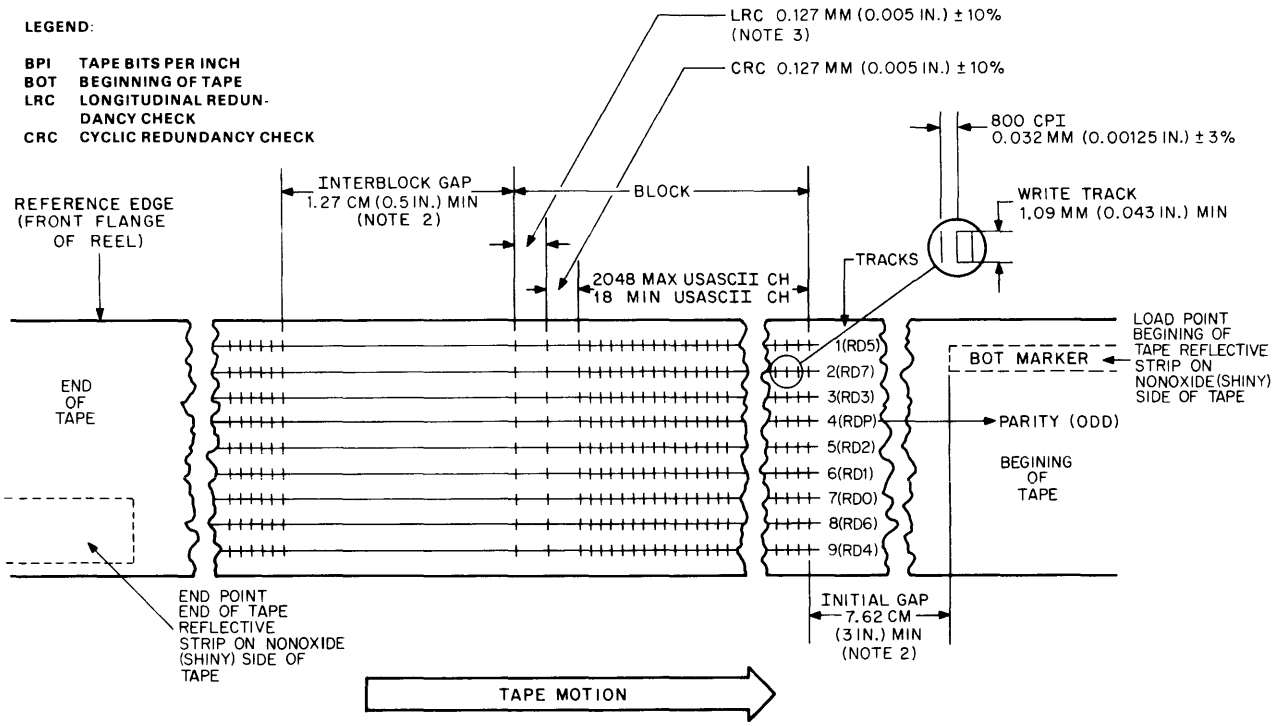
Figure A-3 Data Recording Scheme

A.2.1 NRZI Recording Method (Non-Return-To-Zero Inverted)

In the NRZI recording method, a 1 bit is represented by a reversal in the direction of tape magnetization on a track; a 0 bit is represented by no change in tape magnetization.

A.2.2 9-Channel Tape Format

The format (Figure A-4) is composed of from 18* to 2048 9-bit characters spaced 3 mm (1/800 in) apart, followed by 3 character spaces, a CRC character, 3 more spaces and an LRC character. This unit of data is called a record. At 800 characters per inch, the record is between 0.79 mm (1/32 in) minimum and 12.7 cm (5 in) maximum. Between each record is a gap of at least 1.27 cm (0.5 in). The tape structure consists of a number of records followed by a file mark (Figure A-3). Since data is recorded and read at high speed, IRGs are used to provide space for starting and stopping a tape transport. A transport accelerates from standstill to full speed in approximately 0.5 cm (0.2 in) of tape and decelerates from full speed to standstill in 0.5 cm (0.2 in) of tape; thus, the minimum IRG of 1.27 cm (0.5 in) provides adequate space for starting and stopping the tape transport.



NOTES:

1. TAPE IS SHOWN WITH OXIDE SIDE UP, READ/WRITE HEAD ON SAME SIDE AS OXIDE. TAPE IS SHOWN REPRESENTING 1 BITS IN ALL NRZI RECORDING. 1 BIT PRODUCED BY REVERSAL OF FLUX POLARITY, TAPE FULLY SATURATED IN EACH DIRECTION.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INTERRECORD GAP AND THE INITIAL GAP.
3. AN LRC BIT IS WRITTEN IN ANY TRACK IF THE LONGITUDINAL COUNT IN THAT TRACK IS ODD. CHARACTER PARITY IS IGNORED IN THE LRC CHARACTER.
4. CRC - PARITY OF CRC CHARACTER IS ODD IF AN EVEN NUMBER OF DATA CHARACTERS ARE WRITTEN, AND EVEN IF AN ODD NUMBER OF CHARACTERS ARE WRITTEN.

BE 0500

Figure A-4 Tape Recording Format

The CRC character is generated during a write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character.

*USASCII program standards, not a hardware limit.

The LRC character is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the tape transport after the CRC character is written. The LRC strobe resets the write buffer, causing a 1 to be written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.

A.2.3 7-Channel Tape Format

Each character frame in a 7-channel tape (Figure A-5) consists of six character bits (B, A, 8, 4, 2, 1) in descending order of significance. The parity bit, or check bit (C), is the seventh bit and is set or cleared by the transport write head. One byte of a data word corresponds to one tape character. However, because one byte contains eight bits and a tape character contains only six data bits, two bits within each byte are not used. During a read operation, the extra bits are forced to 0; during a write operation, the bits remain unchanged. During the core dump mode of operation, one byte corresponds to two tape characters. Thus, all bits within the byte are used; however, the two most significant bits on the tape are not used.

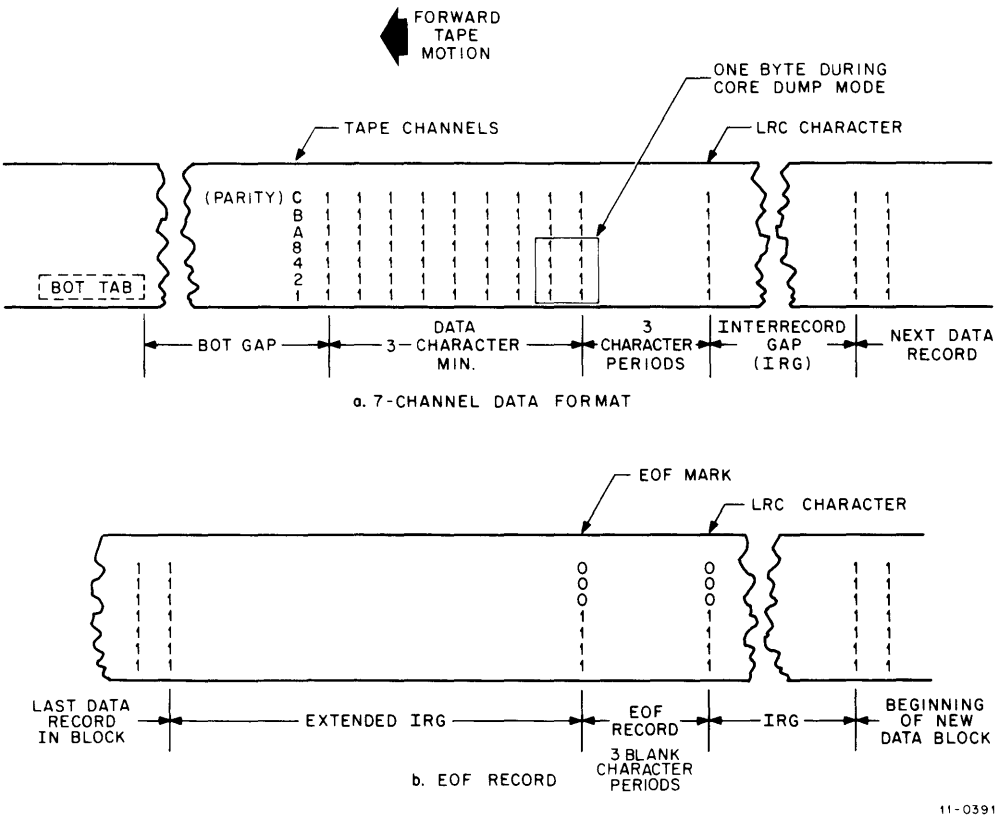


Figure A-5 7-Channel Tape Format

The magnetic tape is divided into data records, each record separated by an interrecord gap (IRG).

In a block format, a number of records are written together with an IRG before the first record and after the last record. In either case, the IRG is an unused portion of tape preceding and following the record or the block.

The longitudinal redundancy check (LRC) character is written after the data and is separated from the data by three character spaces. Each bit in the LRC is such that the total number of bits in any specific channel is even.

The end of a block of records is indicated by an end-of-file mark character. The end-of-file (EOF) mark is separated from the data by an extended IRG. The extended IRG is a 7.6 cm (3 in) strip of blank tape compared to the standard 1.9 cm (3/4 in) IRG for 7-channel tape and the 1.27 cm (1/2 in) IRG for 9-channel tape. The EOF mark and associated LRC character are considered to be one complete record.

The 9-channel tape format (Figure A-6) is similar to the 7-channel format; however, because each character consists of eight data bits and one parity bit, a byte corresponds to a tape character. Therefore, there is no need for a core dump mode, because information can be transferred from the system to the tape on a one-to-one ratio.

In addition, the 9-channel format includes a cyclic redundancy check (CRC) character. Data is followed by three blank character periods, the CRC character, three more blank character periods, and the LRC character. The LRC character is followed by an IRG as before.

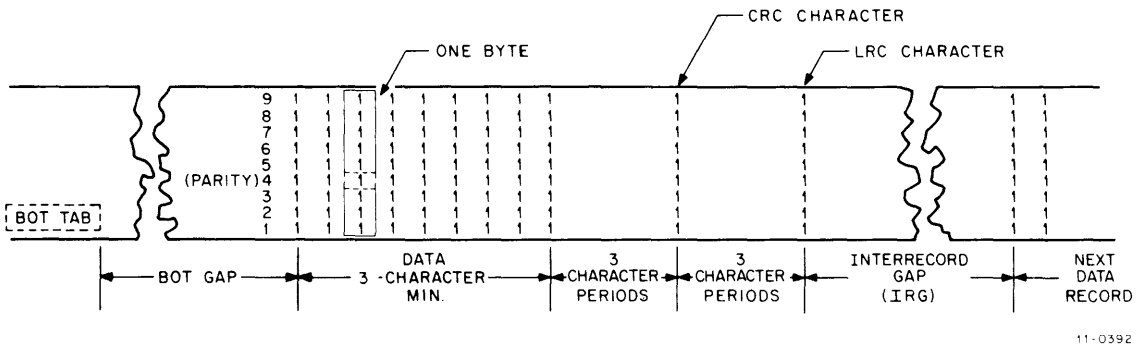


Figure A-6 9-Channel Tape Format

A.3 CYCLIC REDUNDANCY CHECK (CRC) CHARACTER

The CRC character provides a method of error detection and correction on magtape transports. The code has nine check bits that form a check character at the end of each record. To perform a correction, a record in which an error has been detected must be reread into memory with the CRC character for program evaluation. Errors involving more than one track can be detected but not corrected.

The CRC character is generated as follows:

1. The CRC register is cleared at the beginning of each record. As each data bit is written on tape, it is exclusively ORed with its corresponding bit in the CRC register.

2. The CRC register is shifted one position to the right after the exclusive OR operation has taken place.

3. The bits entering CRC2, CRC3, CRC4, and CRC5 of the CRC register are inverted if the bit entering CRCP is a 1. Data is shown in Table A-1; the resultant CRC character is shown in Table A-2.

Table A-1 Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
P	0	0	1	0	1
0	1	0	0	1	0
1	0	1	0	1	0
2	0	1	0	1	1
3	1	0	1	1	0
4	0	1	1	0	1
5	0	1	1	0	1
6	1	0	1	0	1
7	0	1	0	1	0

Table A-2 CRC Character in Register When Writing

CRC Bits	CRC Register						CRC Character On Tape
	Cleared	Character 1	Character 2	Character 3	Character 4	Final	
CRCP	0	0	0	0	1	1	0
CRC0	0	0	0	1	0	0	1
CRC1	0	1	0	0	0	0	1
CRC2	0	0	0	0	0	1	1
CRC3	0	0	1	0	0	0	1
CRC4	0	1	0	0	0	1	1
CRC5	0	0	0	1	1	0	1
CRC6	0	0	1	1	1	0	1
CRC7	0	1	0	0	1	0	1

4. Steps 1–3 are repeated for each data character of record.

5. At CRC time, all positions of the CRC register, except CRC2 and CRC4, are complemented and the resultant CRC character is written on tape.

6. The CRC register is cleared for the next record.

A.4 LONGITUDINAL REDUNDANCY CHECK (LRC) CHARACTER

The LRC character is written three spaces after the CRC character. The vertical parity bit is always written on the LRC character; the vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC character is generated by the LRC register in the following manner:

1. The LRC register is cleared at the beginning of a record.

2. As characters are written on tape, corresponding 1 bits complement the LRC register at the time data is written on tape.

3. At LRC time, the LRC strobe clears the write buffer and 1s are written on tape in only those channels for which the write buffer is set prior to clearing.

4. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character.

A.5 DATA FILES

As previously stated, a record is a group of characters preceded by an IRG and terminated by three spaces, a CRC character, three more spaces, and an LRC character. A file is a group of records separated by IRGs and terminated by a 7.62 cm (3 in) gap followed by a file mark. The file mark is a record consisting of a single data character [the end-of-file (EOF) character] followed by seven blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a file mark is a duplicate of the EOF character (23_8).

A.6 TRACK ASSIGNMENTS

The track assignments for read, write, and parity bits are shown in Table A-3.

Table A-3 Track Assignments for Data and Parity

Transport Track Number	Write Data Bits*	Read Data Bits*	Binary Weight
1 furthest from transport	CWD5	CRD5	2^2
2	CWD7	CRD7	2^0
3	CWD3	CRD3	2^4
4	CWDP	CRDP	-
5	CWD2	CRD2	2^5
6	CWD1	CRD1	2^6
7	CWD0	CRD0	2^7
8	CWD6	CRD6	2^1
9 closest to transport	CWD4	CRD4	2^3

*At controller interface.

APPENDIX B
GLOSSARY

Mnemonic	Meaning
ACCL	Accelerate
ATTN	Attention
BOT	Beginning of Tape
CAP	Capstan
CCW	Counter Clockwise
CLK	Clock
CLR	Clear
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRCC	Cyclic Redundancy Check Character
CS	Control Status
CW	Clockwise
7CH	7-Channel
DAC	Digital-to-Analog Converter
DEM	Demand
DEN	Density
DPR	Drive Present
DRV	Drive
DRVR	Driver
DRY	Drive Ready
DS	Drive Status
DT	Drive Type
EMD	Enable Motion Delay
ENBL	Enable
END PT	End Point
EOF	End of File
EOT	End of Tape
ER	Error
ERR	Composite ERR
F	Function
FMK	File Mark
FOR	Forward
FREQ	Frequency
FWD	Forward

Mnemonic	Meaning
IDB	Identification Burst
INIT	Initialize
IRD	Interchange Read
IRG	Inter Record Gap
LAW	Logic and Write
LM	Lower Motor
LMZ	Lower Motor Zone
LRC	Longitudinal Redundancy Check
LRCC	Longitudinal Redundancy Check Character
LVS	Lower Vacuum Switch
MOL	Medium on Line
MTR	Motor
NEG	Negative
NRZI	Nonreturn to Zero Inverted
OP	Operation
P	Parity
PE	Phase Encoded
PES	Phase Encoded Status
PLS	Pulse
POS	Positive
PT	Point
RD	Read Data
RDS	Read Strobe
REC	Record
REV	Reverse
REW	Rewind
RSDO	Read Strobe Delay Over
RWND	Rewind
RWS	Rewind Status
SB	Slave Bus
SC	Slave Clock
SDWN	Settle Down
SEL	Select
SLA	Slave Attention
SN	Serial Number
SPR	Slave Present
SS	Slave Select
STRB	Strobe
SW	Switch
TACH	Tachometer
TFG	Test Function Generator
TH	Threshold
TMD	Tape Motion Daughter
TUR	Tape Unit Ready

Mnemonic	Meaning
UM	Upper Motor
UMZ	Upper Motor Zone
UNLD	Unload
UVS	Upper Vacuum Switch
VPE	Vertical Parity Error
WCLK	Write Clock
WD	Write Data
WRE	Write Enable
WRL	Write Lock
WRT	Write
WRT CLK	Write Clock

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