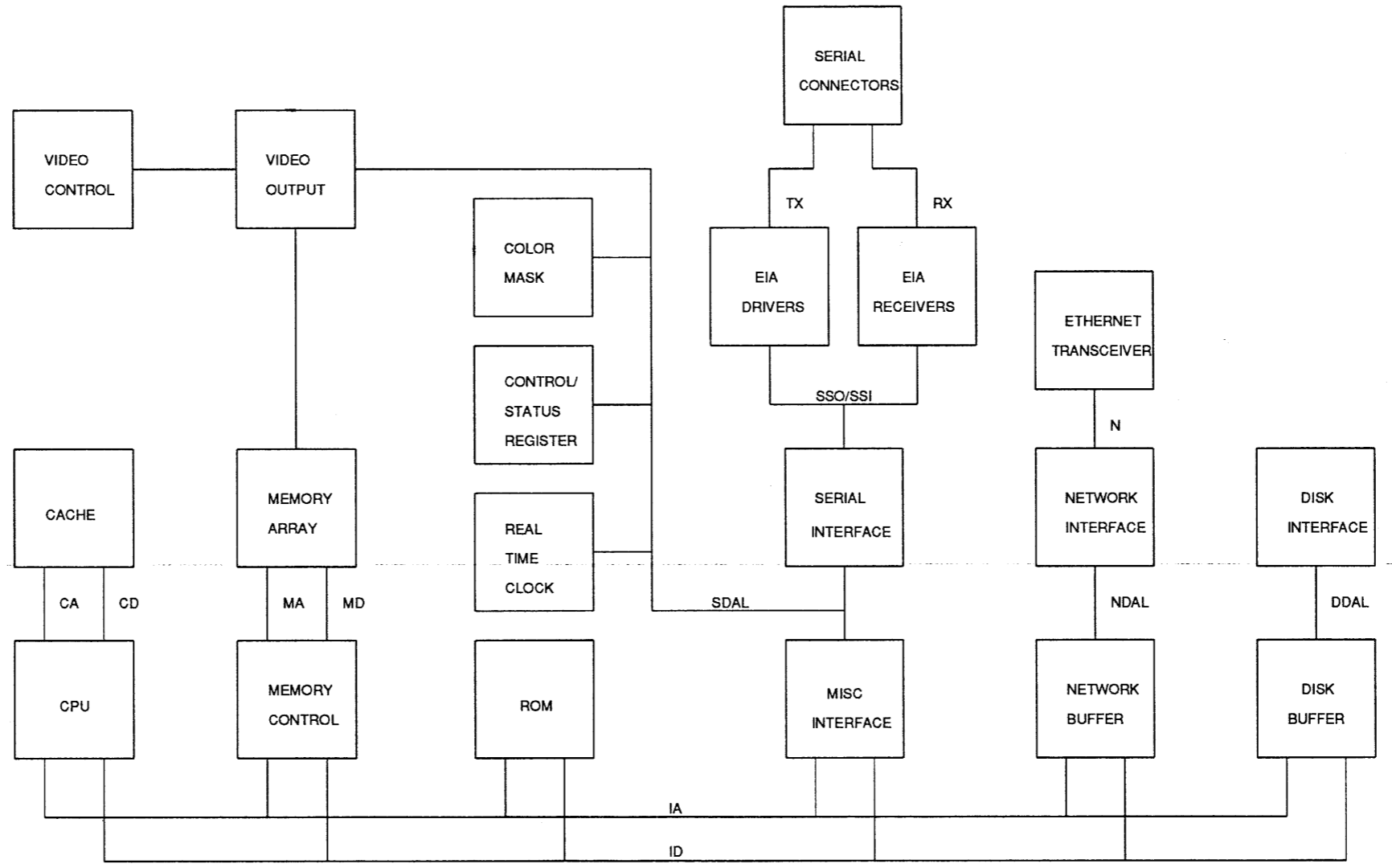


Include  
decls



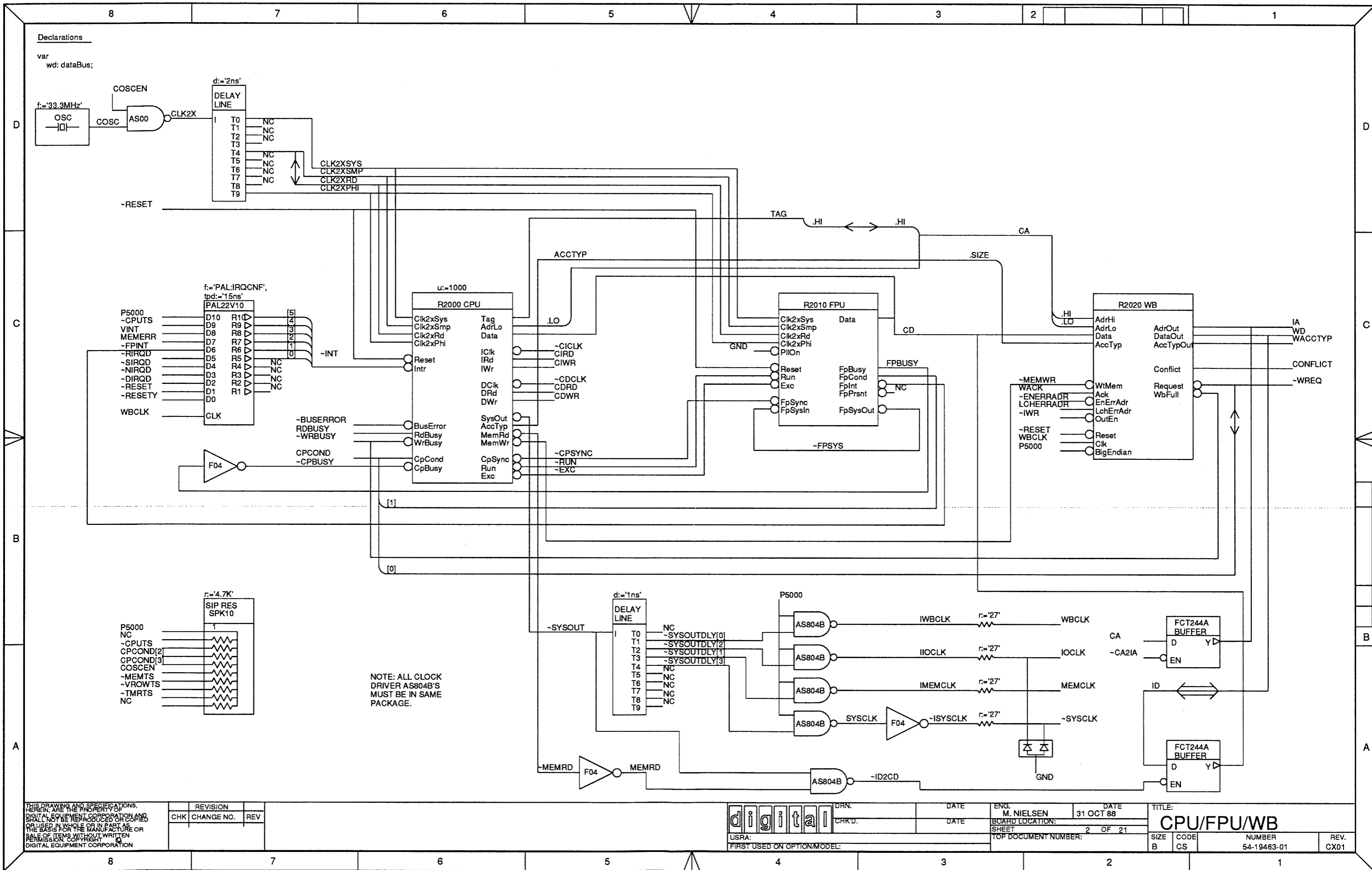
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REVISION		
CHK	CHANGE NO.	REV.

**digital** DRN. \_\_\_\_\_ DATE \_\_\_\_\_  
 CHKD. \_\_\_\_\_ DATE \_\_\_\_\_  
 USRA: \_\_\_\_\_  
 FIRST USED ON OPTION/MODEL: \_\_\_\_\_

ENG. M. NIELSEN	DATE 31 OCT 88
BOARD LOCATION:	SHEET 1 OF 21
TOP DOCUMENT NUMBER:	

TITLE: PMAX System Module			
SIZE B	CODE CS	NUMBER 54-19463-01	REV. CX01



Declarations

```
var
  wd: dataBus;
```

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

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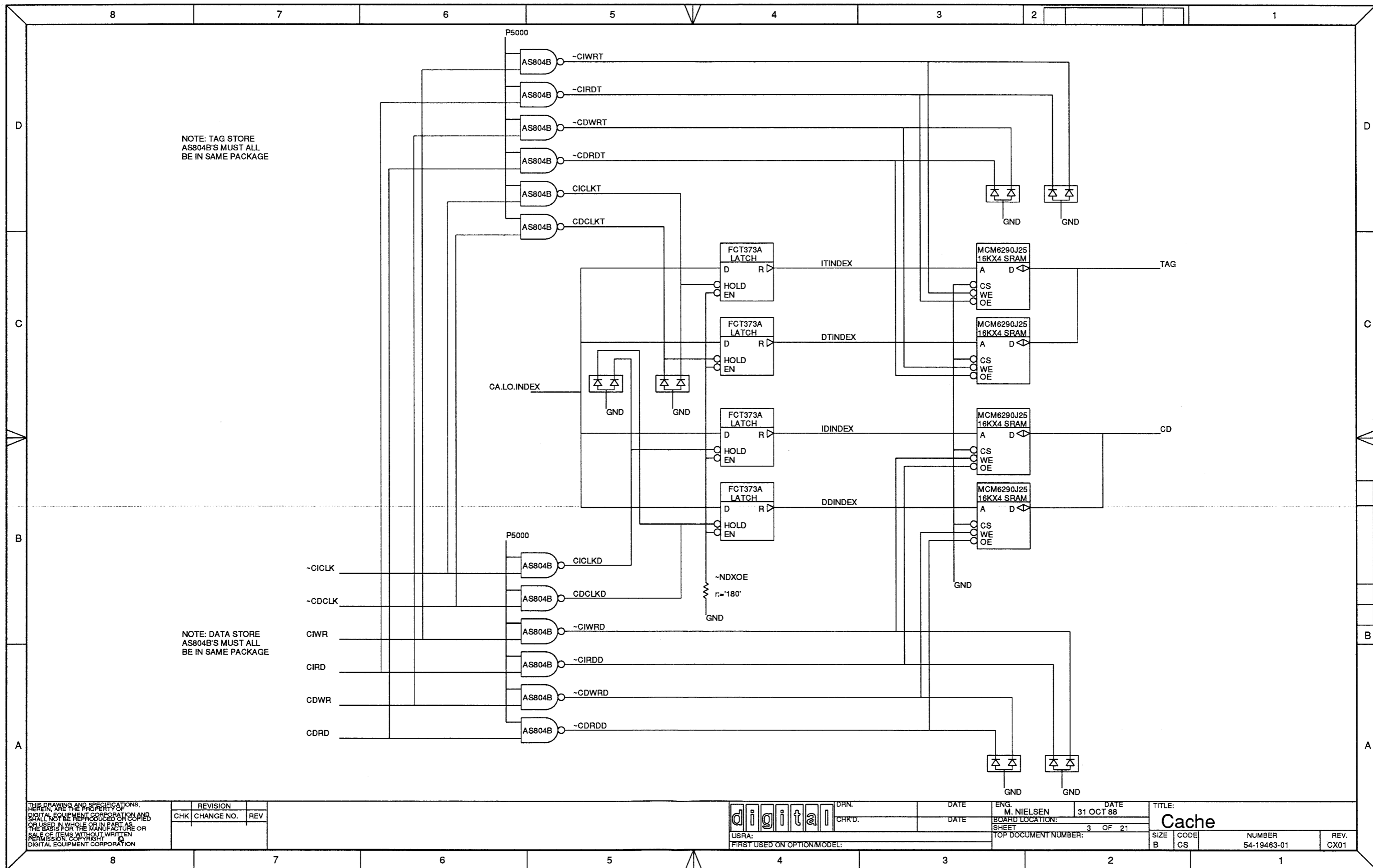
REVISION	
CHK	CHANGE NO.

**digital** DRN.  
CHK'D.

DATE	ENG.	DATE
	M. NIELSEN	31 OCT 88

SHEET		TOP DOCUMENT NUMBER:	
	2 OF 21		

TITLE:			
CPU/FPU/WB			
SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01



NOTE: TAG STORE  
AS804B'S MUST ALL  
BE IN SAME PACKAGE

NOTE: DATA STORE  
AS804B'S MUST ALL  
BE IN SAME PACKAGE

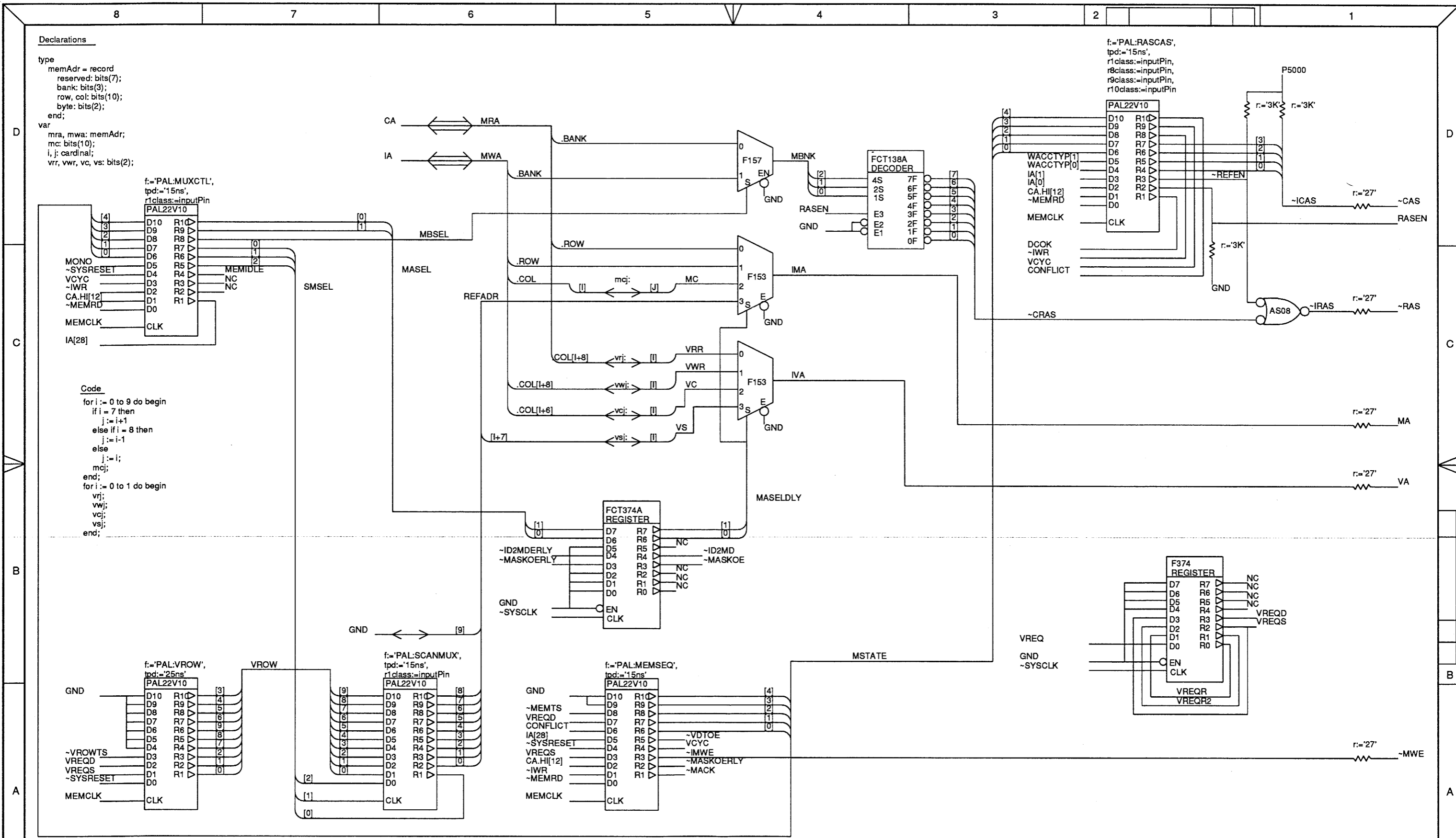
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	CHANGE NO.	REV

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CHKD. DATE  
USRA:  
FIRST USED ON OPTION MODEL:

ENG.	DATE
M. NIELSEN	31 OCT 88
BOARD LOCATION:	
SHEET 3 OF 21	
TOP DOCUMENT NUMBER:	

TITLE:			
Cache			
SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01



**Declarations**

```

type
  memAdr = record
    reserved: bits(7);
    bank: bits(3);
    row, col: bits(10);
    byte: bits(2);
  end;
var
  mra, mwa: memAdr;
  mc: bits(10);
  i, j: cardinal;
  vrr, vwr, vc, vs: bits(2);

```

```

f:="PAL:RASCAS";
tpd:="15ns";
r1class:=inputPin,
r8class:=inputPin,
r9class:=inputPin,
r10class:=inputPin

```

```

f:="PAL:MUXCTL";
tpd:="15ns";
r1class:=inputPin

```

```

Code
for i := 0 to 9 do begin
  if i = 7 then
    j := i+1
  else if i = 8 then
    j := i-1
  else
    j := i;
  mcj;
end;
for i := 0 to 1 do begin
  vrr;
  vwr;
  vcj;
  vsj;
end;

```

```

f:="PAL:VROW";
tpd:="25ns";

```

```

f:="PAL:SCANMUX";
tpd:="15ns";
r1class:=inputPin

```

```

f:="PAL:MEMSEQ";
tpd:="15ns";

```

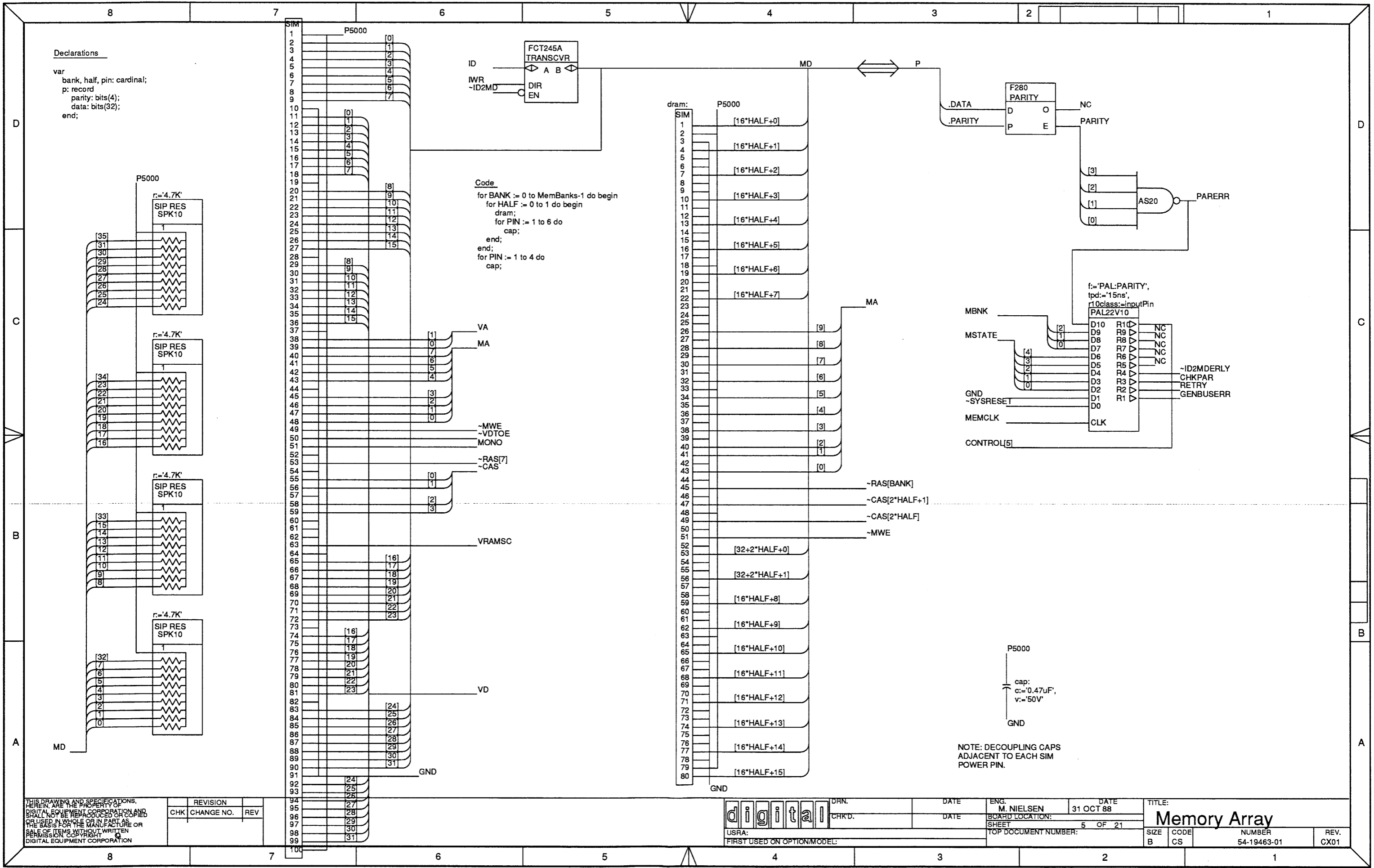
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REVISION	CHK	CHANGE NO.	REV

**digital** ORN.  
 DATE: 31 OCT 88  
 ENG: M. NIELSEN  
 BOARD LOCATION: SHEET 4 OF 21  
 TOP DOCUMENT NUMBER: 54-19463-01

DATE	ENG.	DATE	TITLE:
	M. NIELSEN	31 OCT 88	Memory Control

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01



**Declarations**

```

var
  bank, half, pin: cardinal;
  p: record
    parity: bits(4);
    data: bits(32);
  end;
end;

```

**Code**

```

for BANK := 0 to MemBanks-1 do begin
  for HALF := 0 to 1 do begin
    dram;
    for PIN := 1 to 6 do
      cap;
    end;
  end;
  for PIN := 1 to 4 do
    cap;
  end;
end;

```

```

f:= 'PAL:PARITY',
tpd:= '15ns',
r10class:= 'inputPin
PAL22V10

```

NOTE: DECOUPLING CAPS  
ADJACENT TO EACH SIM  
POWER PIN.

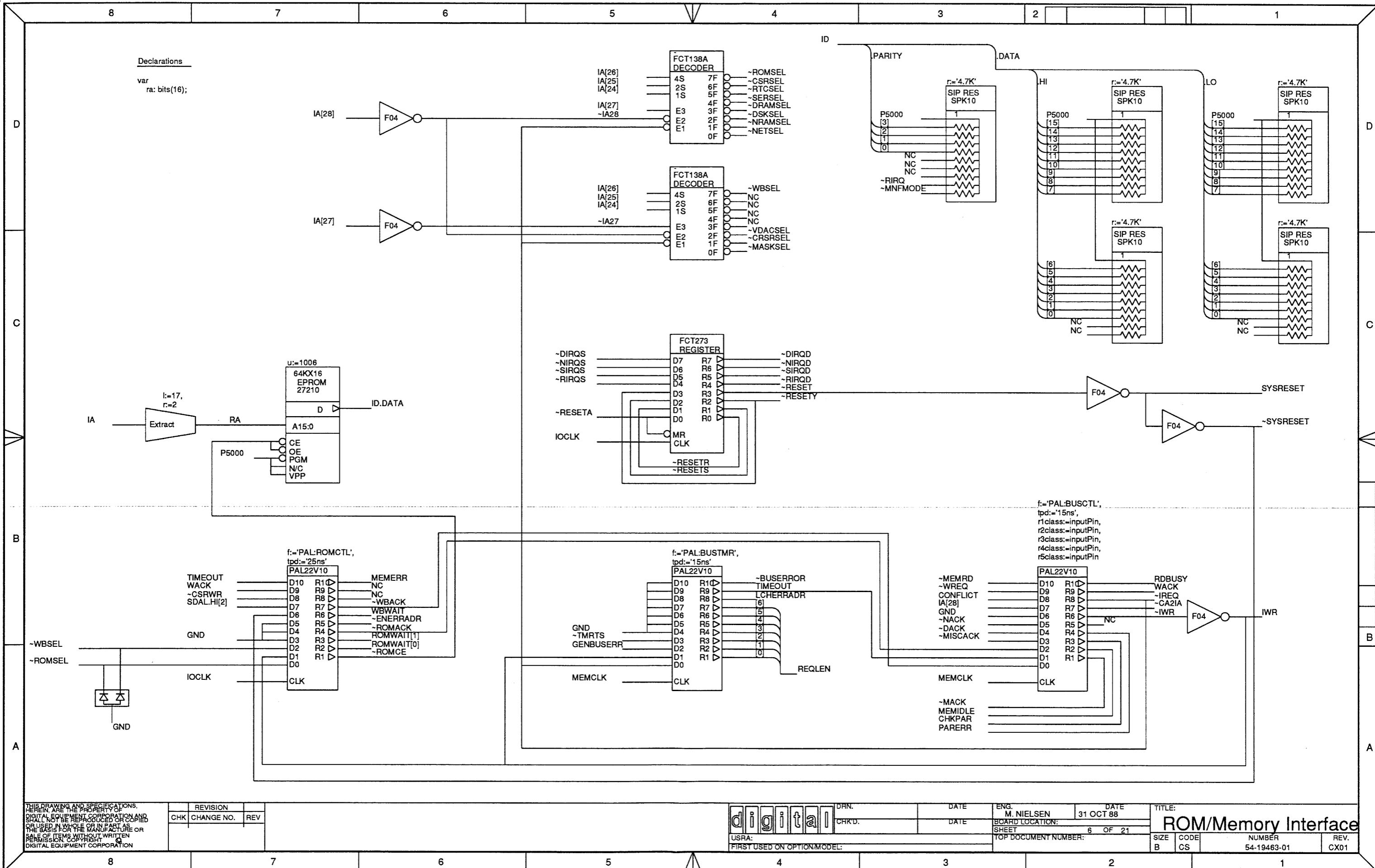
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REVISION		REV
CHK	CHANGE NO.	REV
94		27
95		28
96		29
97		30
98		31
99		
100		

**digital** DRN.  
CHKD.

DATE	ENG.	DATE	TITLE:
	M. NIELSEN	31 OCT 88	<b>Memory Array</b>
DATE	BOARD LOCATION:	5 OF 21	
SHEET	TOP DOCUMENT NUMBER:		

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01



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CHK	CHANGE NO.	REV

REVISION	

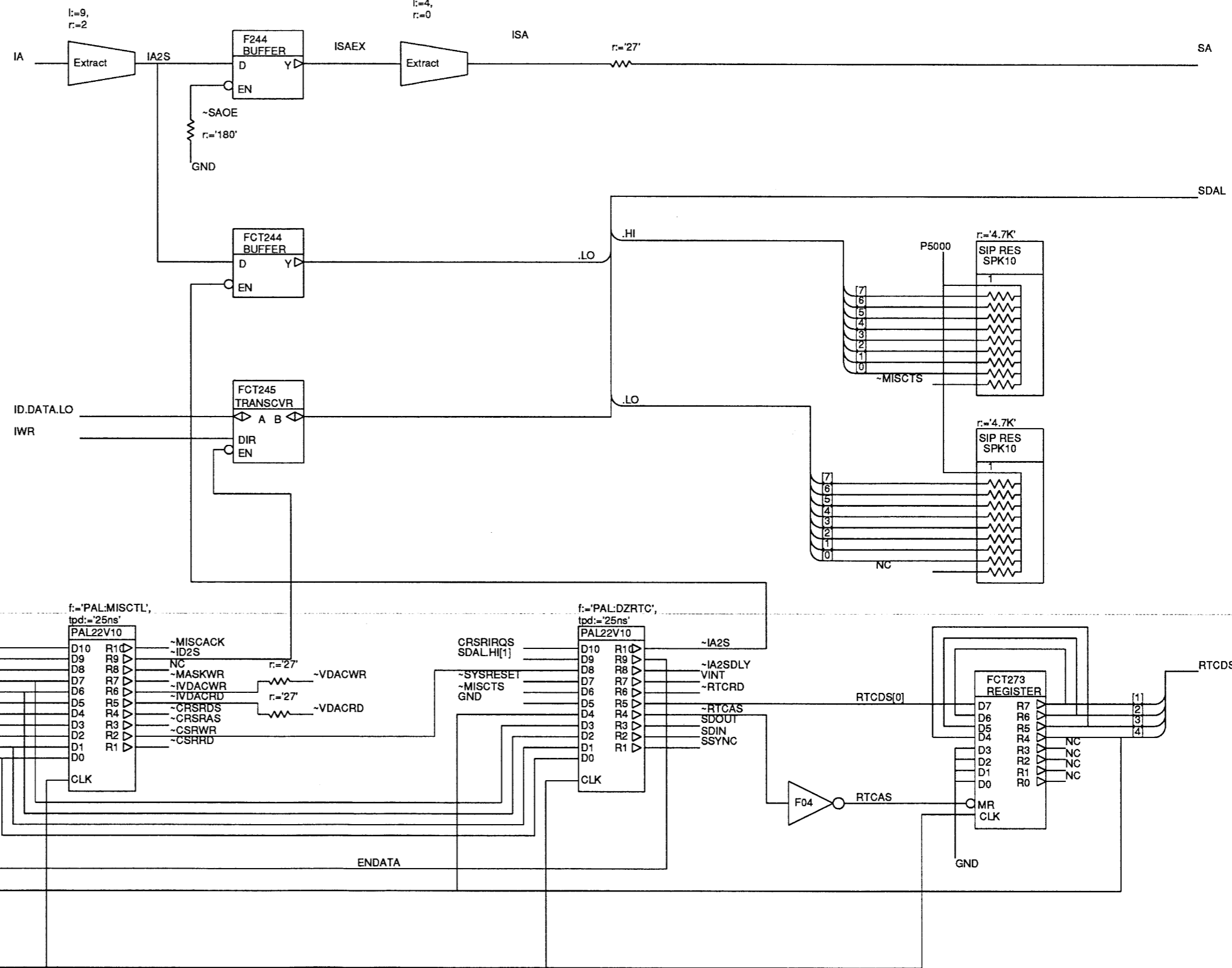
**digital** DRN.  
CHK'D.

DATE  
DATE

ENG. M. NIELSEN  
DATE 31 OCT 88  
BOARD LOCATION:  
SHEET 6 OF 21

TITLE:  
**ROM/Memory Interface**  
SIZE B CODE CS NUMBER 54-19463-01 REV. CX01

Declarations  
var  
ia2s: bits(8);



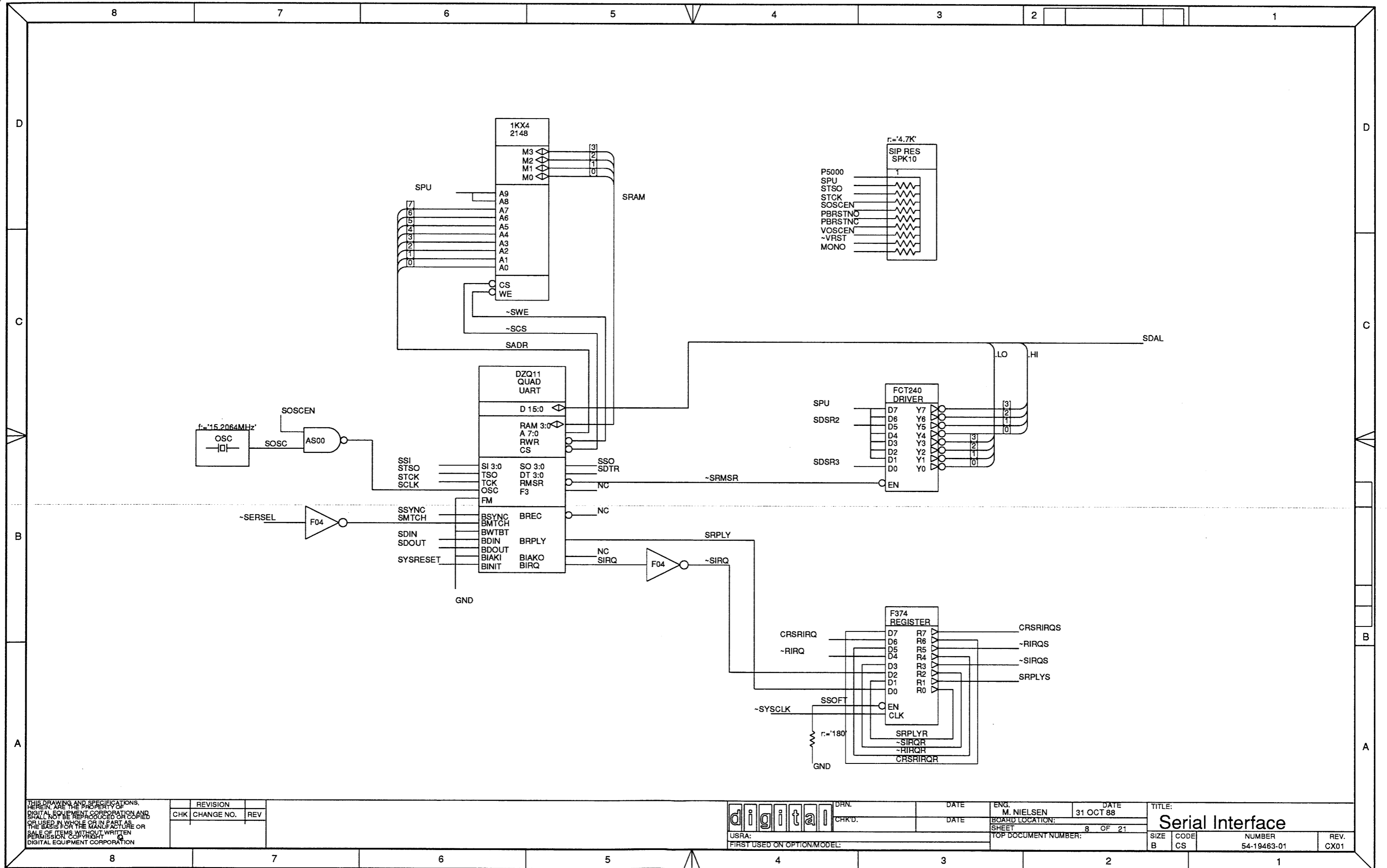
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CHK	REVISION	CHANGE NO.	REV

**digital** DRN.  
CHK'D.  
USRA:  
FIRST USED ON OPTION/MODEL:

DATE  
DATE  
ENG. M. NIELSEN  
BOARD LOCATION:  
SHEET 7 OF 21  
TOP DOCUMENT NUMBER:

TITLE:  
**Misc Interface**  
SIZE B CODE CS NUMBER 54-19463-01 REV. CX01



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REVISION	
CHK	CHANGE NO. REV

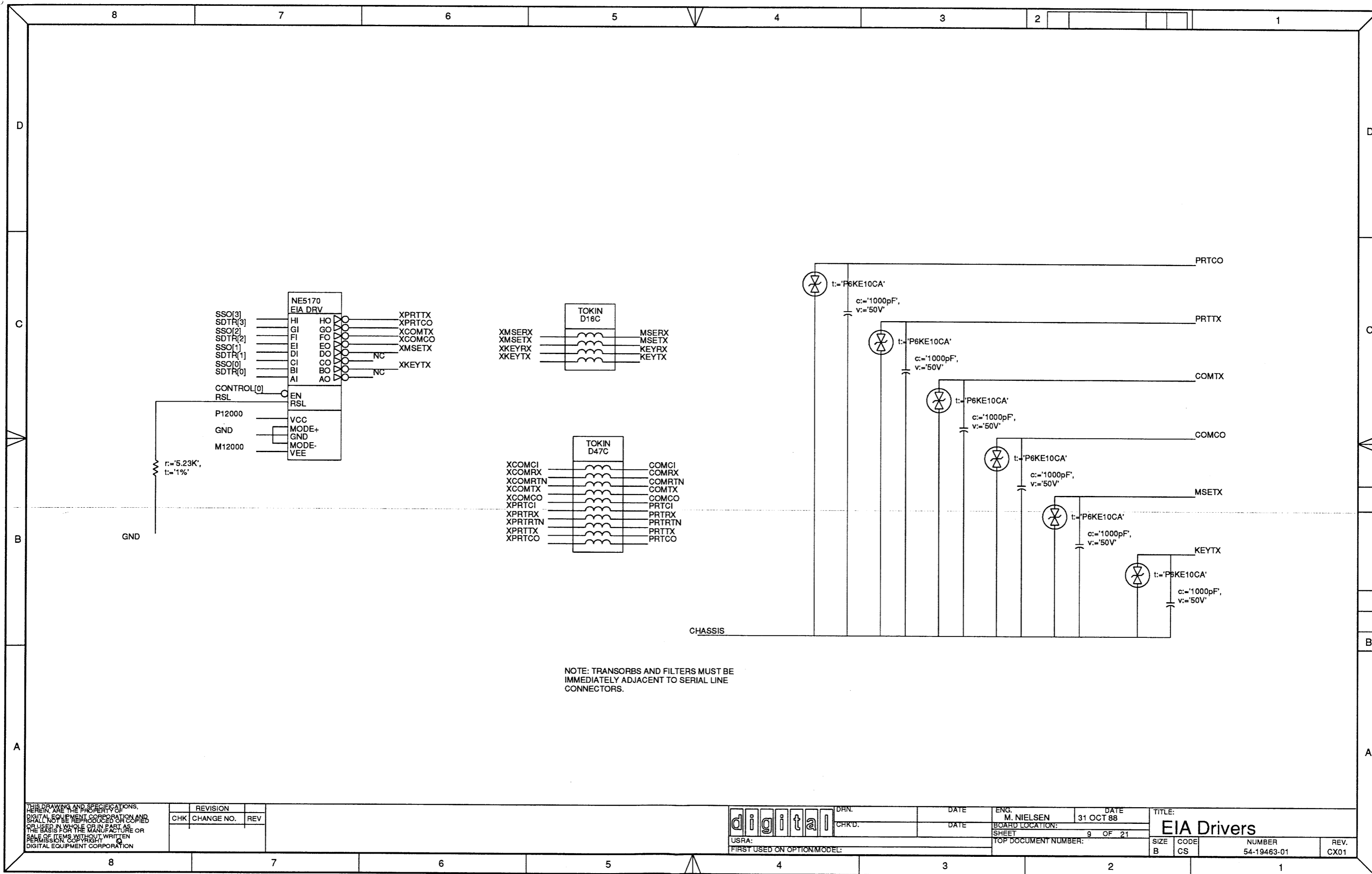
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CHK'D. DATE  
USRA: FIRST USED ON OPTION/MODEL:

ENG. M. NIELSEN DATE 31 OCT 88  
BOARD LOCATION:  
SHEET 8 OF 21  
TOP DOCUMENT NUMBER:

SIZE B CODE CS NUMBER 54-19463-01 REV. CX01

TITLE: **Serial Interface**



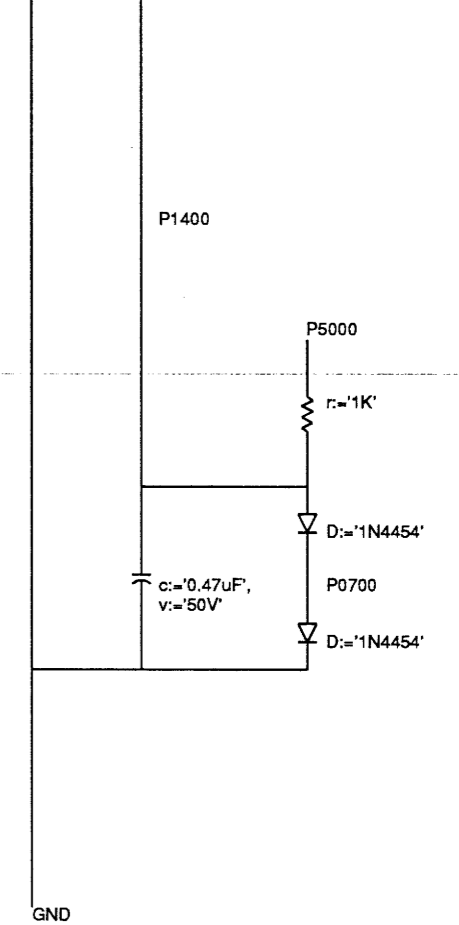
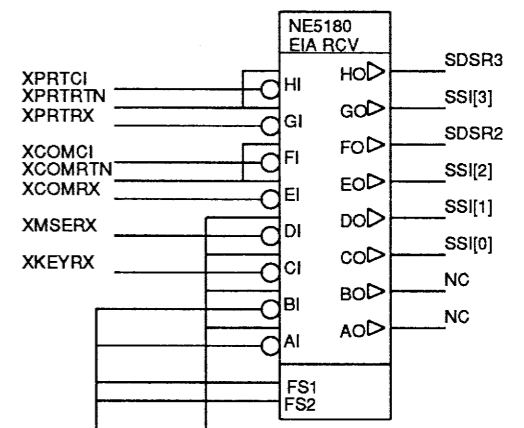
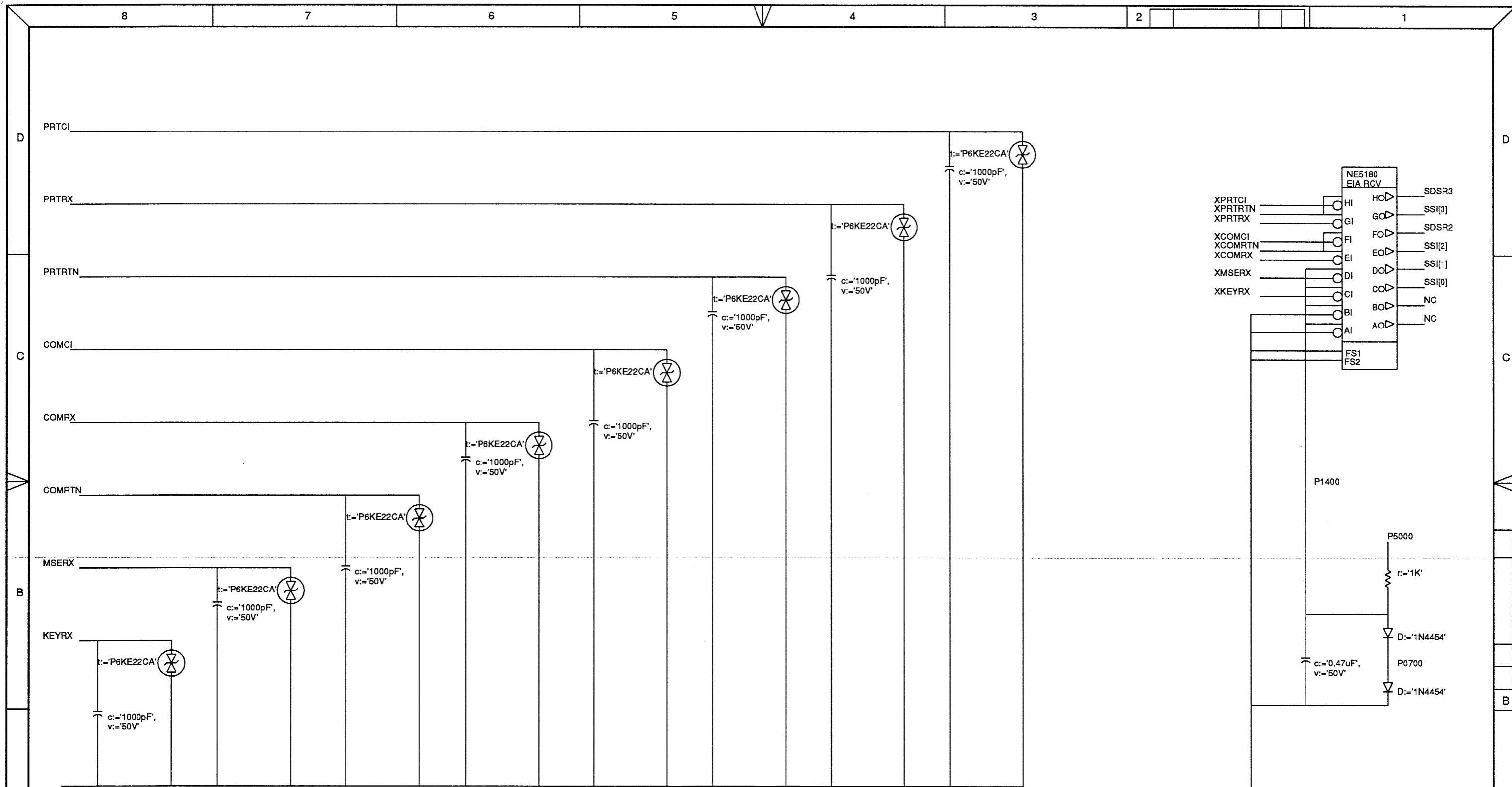


NOTE: TRANSORBS AND FILTERS MUST BE IMMEDIATELY ADJACENT TO SERIAL LINE CONNECTORS.

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REVISION	
CHK	CHANGE NO.

	DHN.	DATE	ENG.	DATE	TITLE:
	CHK'D.	DATE	M. NIELSEN	31 OCT 88	EIA Drivers
USRA:	TOP DOCUMENT NUMBER:		SHEET		9 OF 21
FIRST USED ON OPTION/MODEL:			SIZE	CODE	NUMBER
			B	CS	54-19463-01
					REV.
					CX01



NOTE: TRANSORBS AND FILTERS MUST BE IMMEDIATELY ADJACENT TO CONNECTOR PINS.

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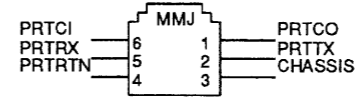
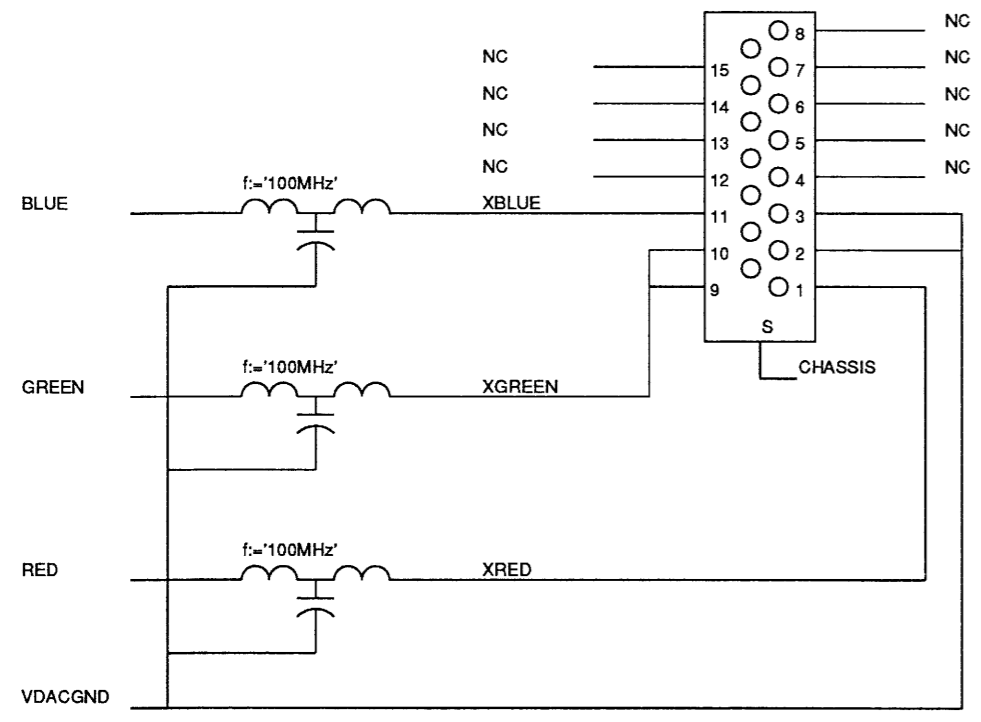
REVISION		
CHK	CHANGE NO.	REV

**digital** DRN. DATE ENG. M. NIELSEN DATE 31 OCT 88  
 CRK'D. DATE BOARD LOCATION: SHEET 10 OF 21  
 USRA: TOP DOCUMENT NUMBER: FIRST USED ON OPTION/MODEL:

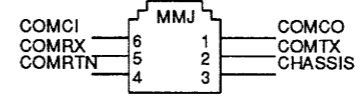
TITLE: EIA Receivers		NUMBER: 54-19463-01	REV. CX01
SIZE: B	CODE: CS		

8 7 6 5 4 3 2 1

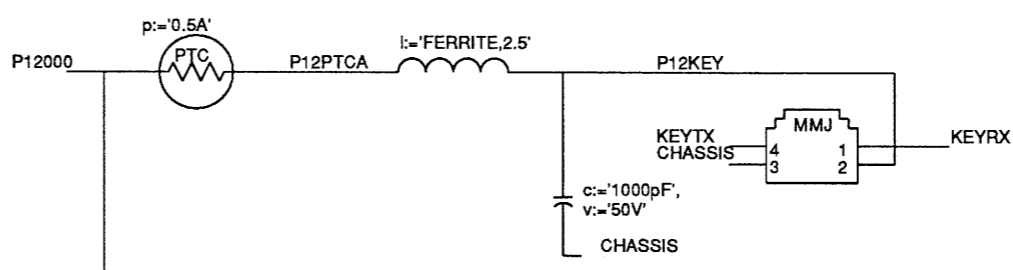
Video Connector



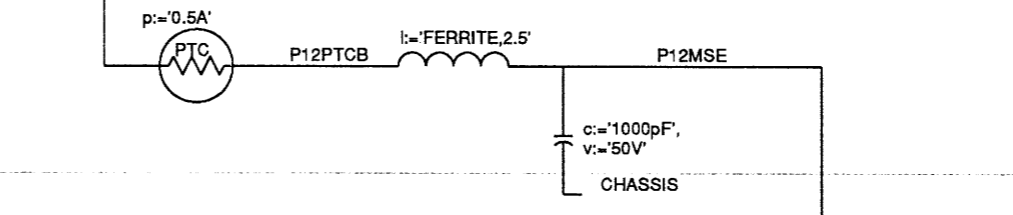
Printer Connector



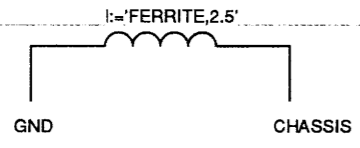
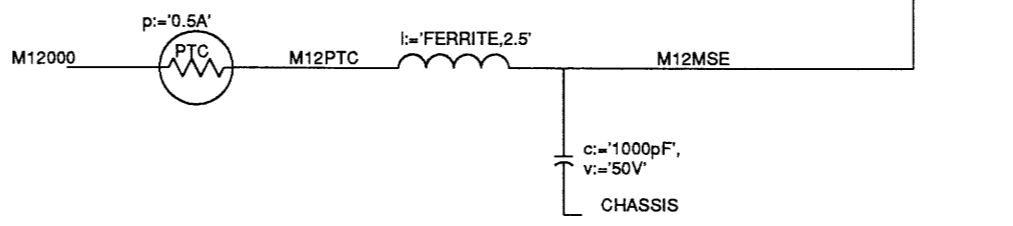
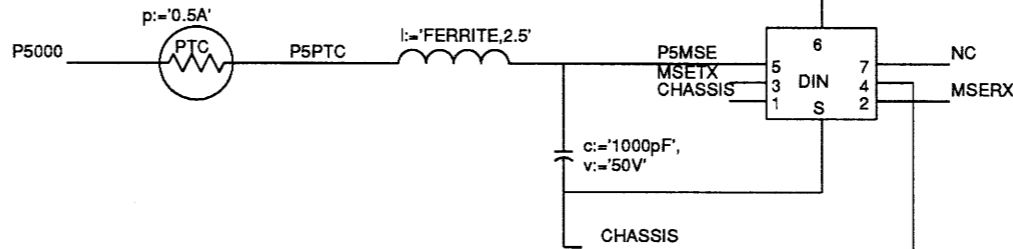
Comm Connector



Keyboard Connector



Mouse Connector

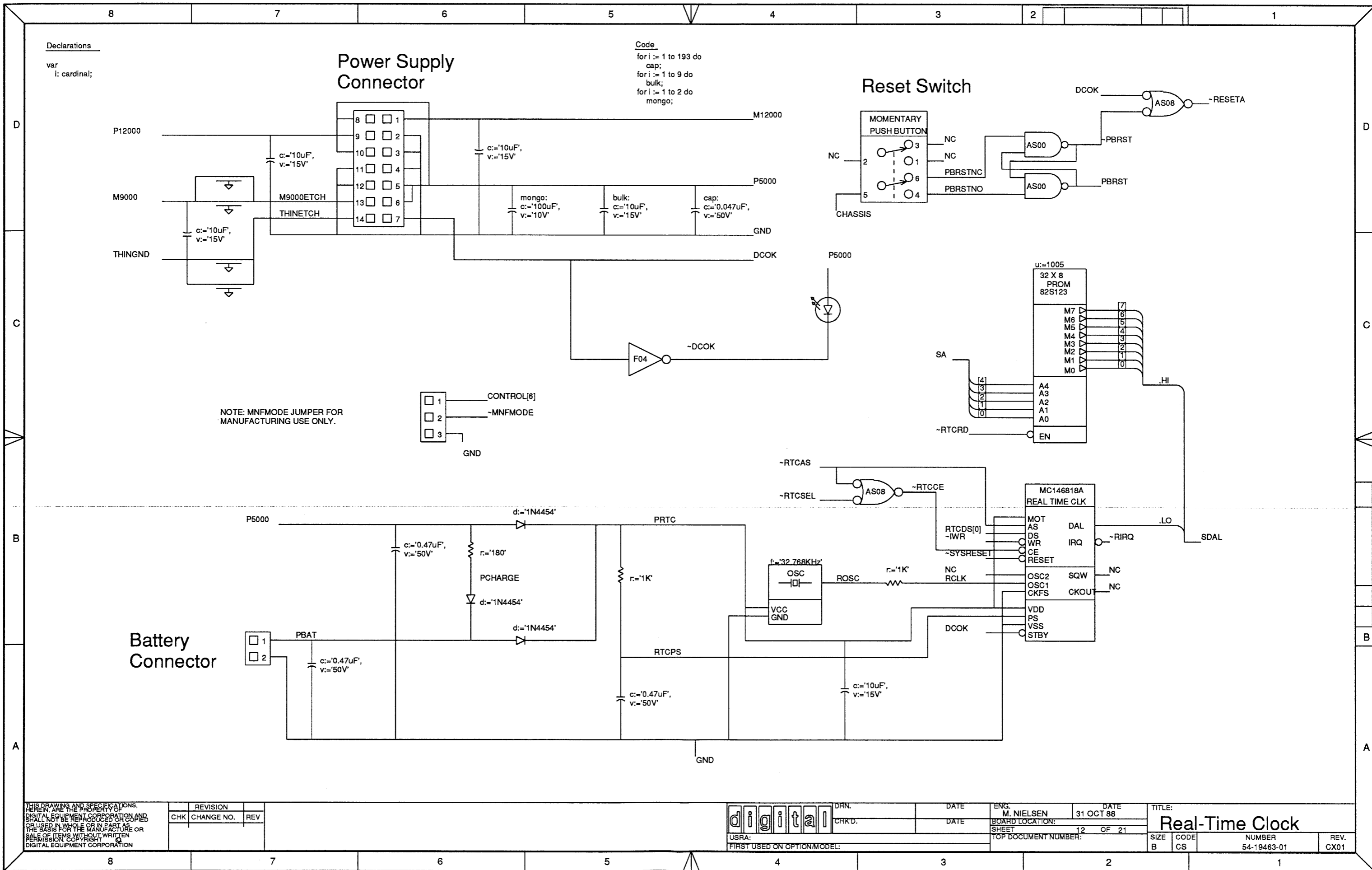


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REVISION	
CHK	CHANGE NO. REV

**digital** DRN. DATE ENG. M. NIELSEN 31 OCT 88 TITLE: Serial Connectors  
 USRA: DATE BOARD LOCATION: SHEET 11 OF 21  
 FIRST USED ON OPTION/MODEL: TOP DOCUMENT NUMBER: SIZE CODE NUMBER REV. A CS 54-19463-01 CX01

8 7 6 5 4 3 2 1



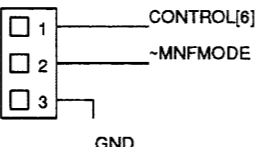
Declarations

```
var
i: cardinal;
```

Code

```
for i := 1 to 193 do
cap;
for i := 1 to 9 do
bulk;
for i := 1 to 2 do
mongo;
```

NOTE: MNFMODE JUMPER FOR MANUFACTURING USE ONLY.



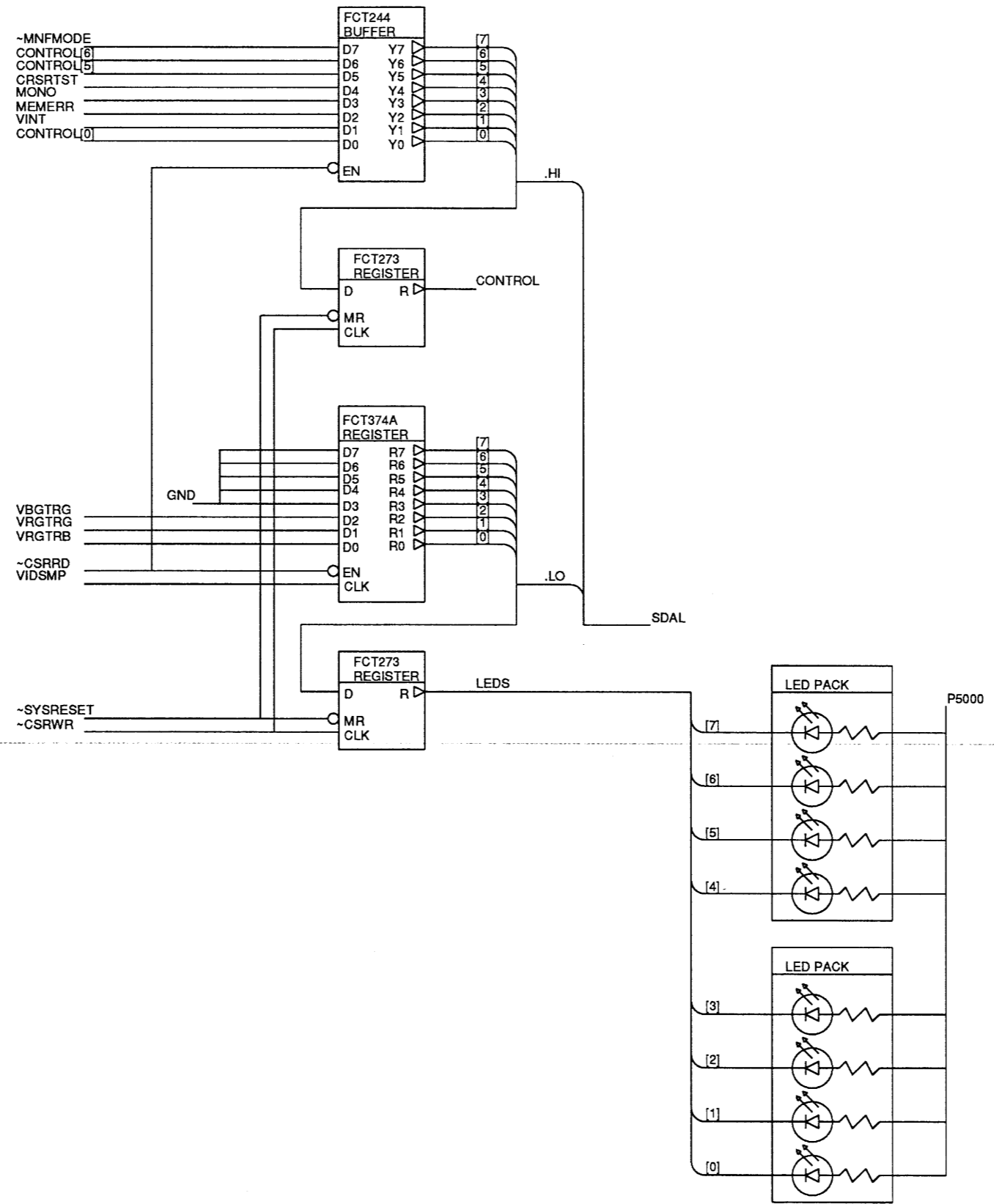
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REVISION	
CHK	CHANGE NO. REV

digital DRN. DATE ENG. M. NIELSEN DATE 31 OCT 88 TITLE: Real-Time Clock

USRA: FIRST USED ON OPTION/MODEL: SHEET 12 OF 21 TOP DOCUMENT NUMBER:

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01



NOTE: LEDS ILLUMINATED DURING/AFTER RESET ASSERTION.

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REVISION		
CHK	CHANGE NO.	REV

<b>digital</b>	DRN.	DATE	ENG.	DATE	TITLE:
	CHK'D.	DATE	M. NIELSEN	31 OCT 88	<b>Control/Status Register</b>
USRA:	SHEET		BOARD LOCATION:		SIZE
FIRST USED ON OPTION/MODEL:	13 OF 21		TOP DOCUMENT NUMBER:		CODE
					NUMBER
					54-19463-01
					REV.
					CX01

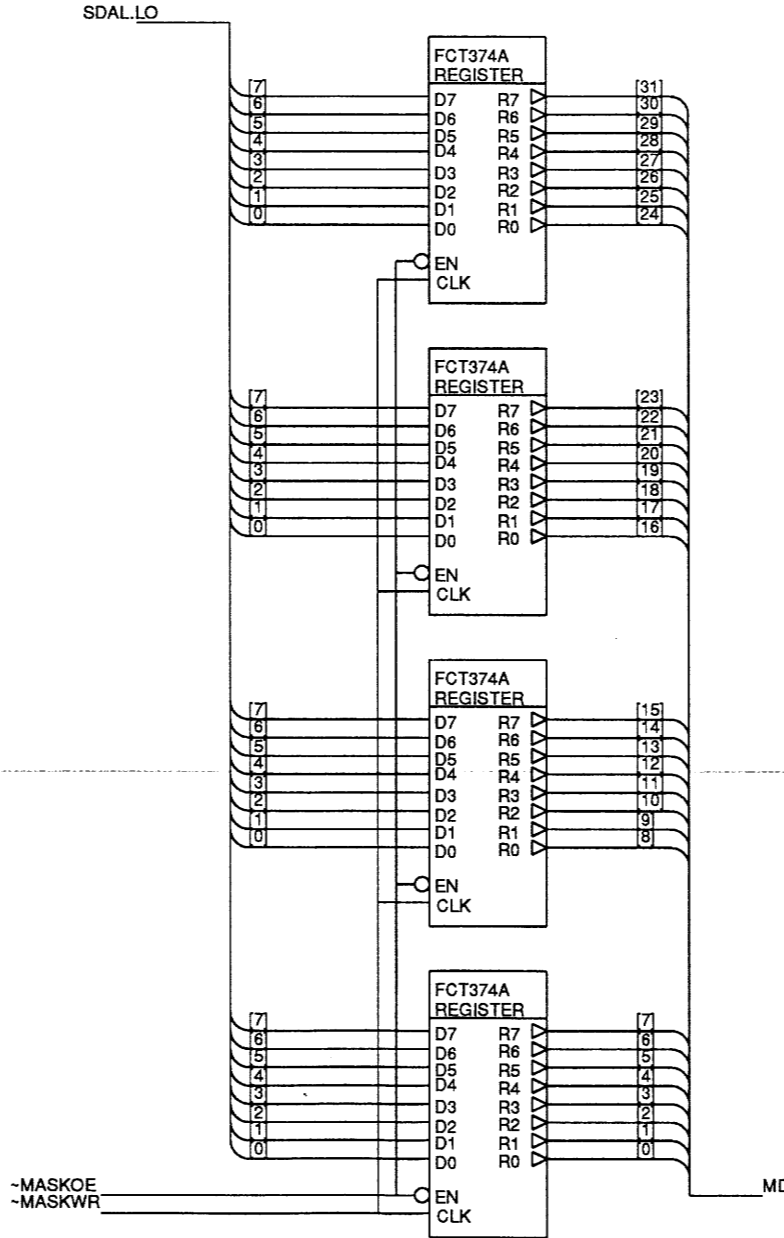
8 7 6 5 4 3 2 1

D D

C C

B B

A A



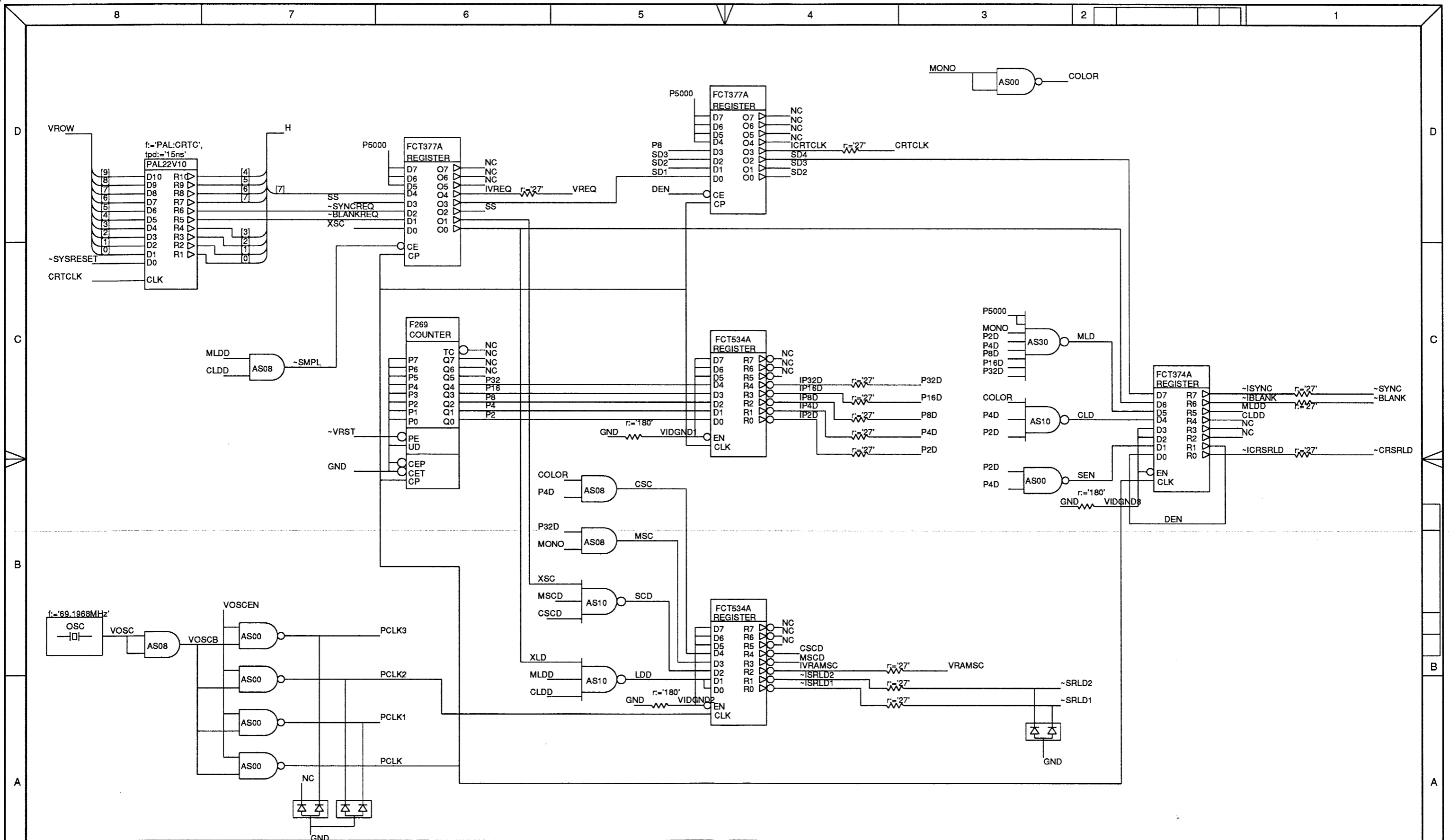
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CHK	CHANGE NO.	REV

**digital** DRN. DATE ENG. M. NIELSEN DATE 31 OCT 88  
 CHK'D. DATE BOARD LOCATION: SHEET 14 OF 21  
 USRA: TOP DOCUMENT NUMBER: SIZE B CODE CS NUMBER 54-19463-01 REV. CX01  
 FIRST USED ON OPTION/MODEL:

TITLE: **Color Plane Mask**

8 7 6 5 4 3 2 1



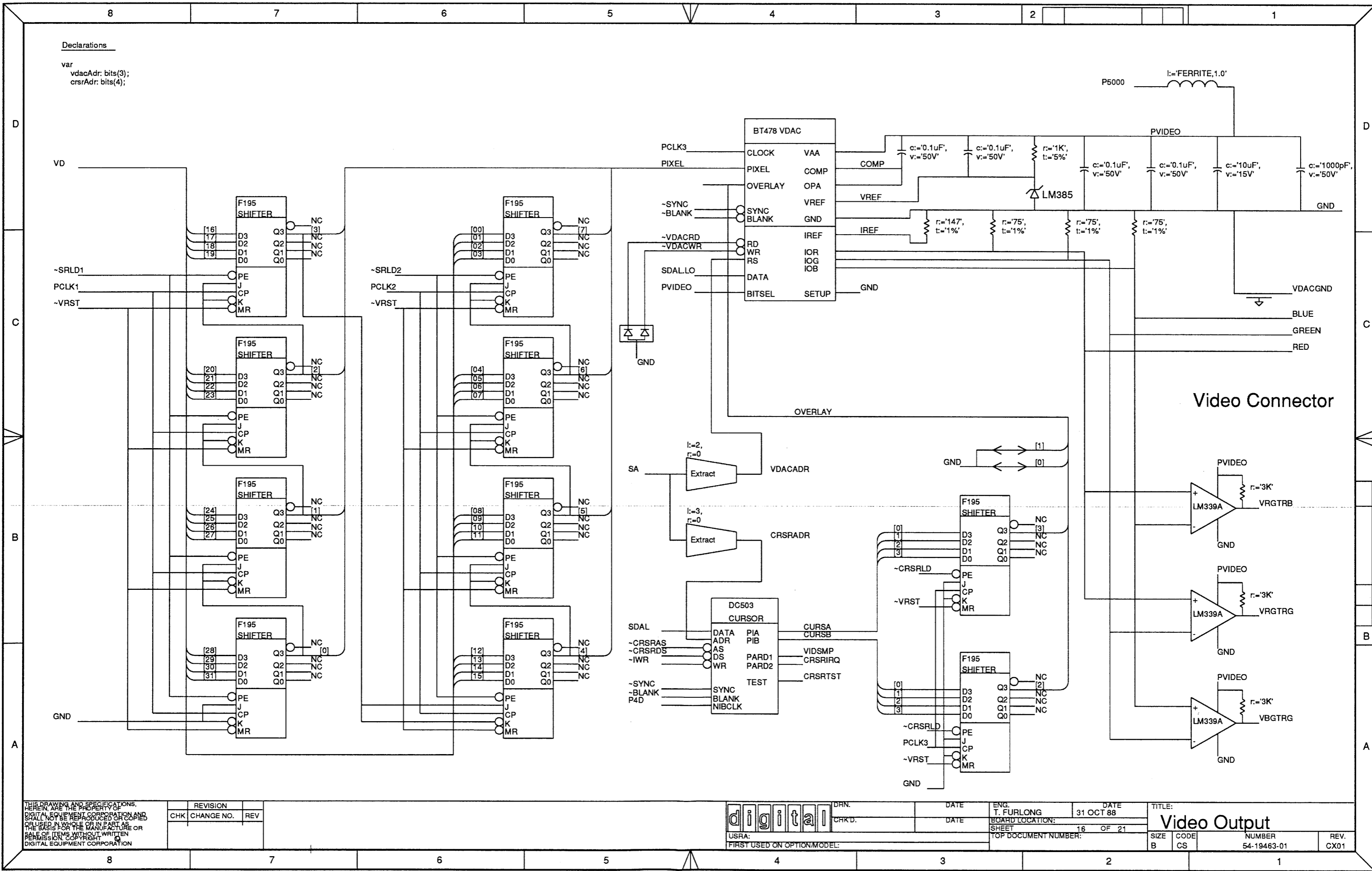
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**digital** DRN. DATE: T. FURLONG 31 OCT 88  
 CKRD. DATE: BOARD LOCATION: SHEET 15 OF 21  
 USRA: TOP DOCUMENT NUMBER: FIRST USED ON OPTION/MODEL:

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01

TITLE: **Video Control**



Declarations  
var  
vdacAdr: bits(3);  
crsrAdr: bits(4);

Video Connector

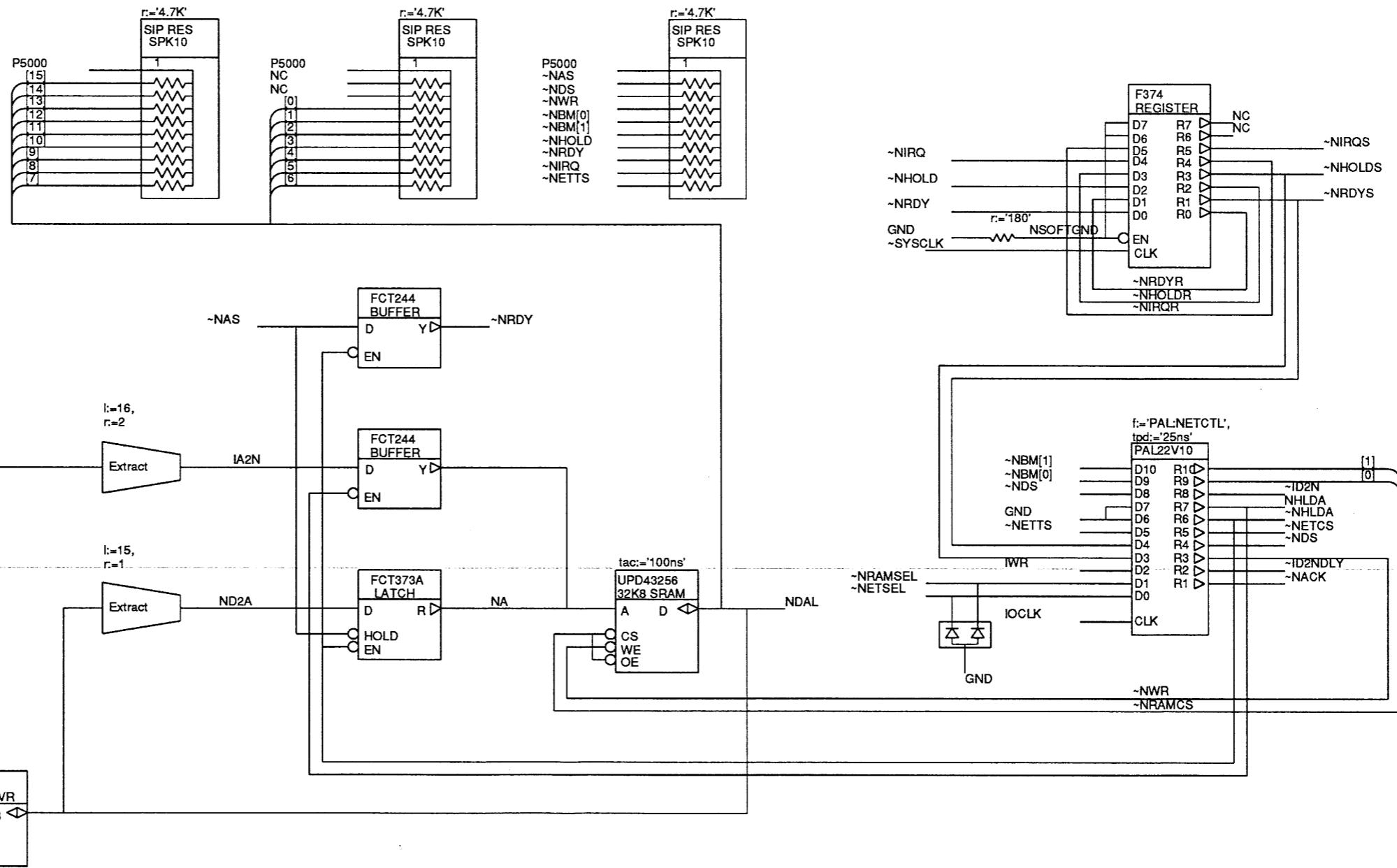
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REVISION	CHK	CHANGE NO.	REV

digital DRN. DATE ENG. T. FURLONG DATE 31 OCT 88 TITLE: Video Output  
 CRKD. DATE BOARD LOCATION: SHEET 16 OF 21 SIZE CODE NUMBER REV. B CS 54-19463-01 CX01  
 USRA: FIRST USED ON OPTION/MODEL:



Declarations  
var  
ia2n: bits(15);  
nd2a: bits(15);



NOTE: NET BUFFER IS 32K 16-BIT WORDS. BUFFER IS 16-BIT-ALIGNED TO LANCE, 32-BIT-ALIGNED TO CPU. BUFFER HAS 8-BIT ACCESS TO LANCE, 16-BIT ACCESS TO CPU. CPU IS DEFAULT MASTER OF NDAL, AND IS STALLED FOR LANCE-CSR OR BUFFER ACCESS IF LANCE DMA IS IN PROGRESS.

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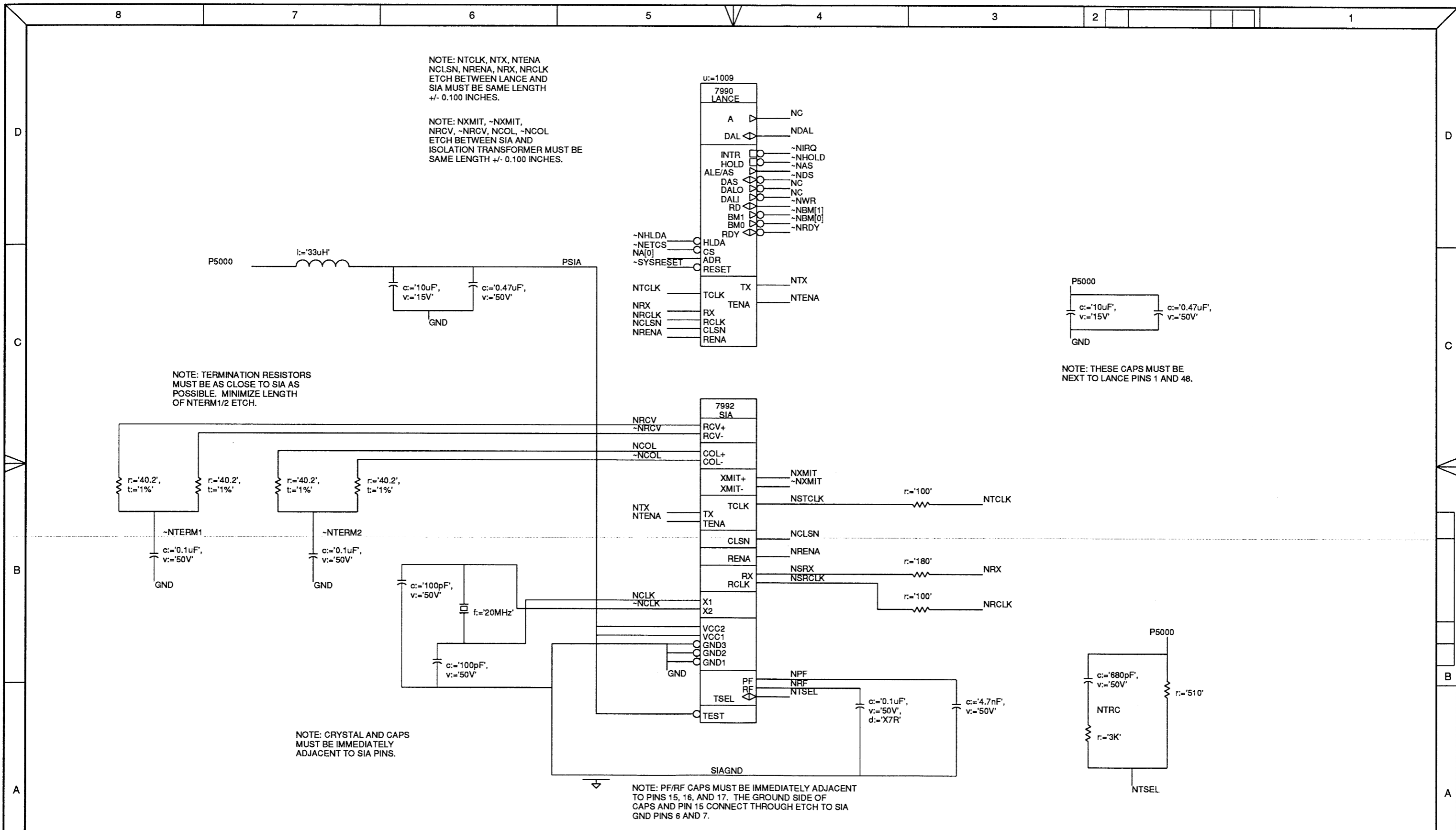
CHK	REVISION	CHANGE NO.	REV

digital  
USRA:  
FIRST USED ON OPTION/MODEL:

DRN.	DATE	ENG.	DATE
		M. NIELSEN	31 OCT 88
CHK'D.	DATE	BOARD LOCATION:	
		SHEET	17 OF 21
		TOP DOCUMENT NUMBER:	

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01

TITLE:  
**Network Buffer**



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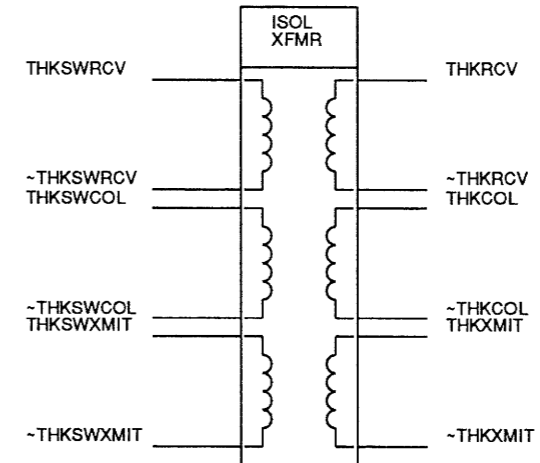
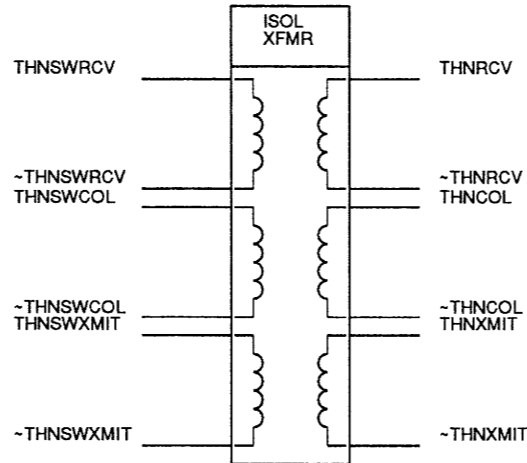
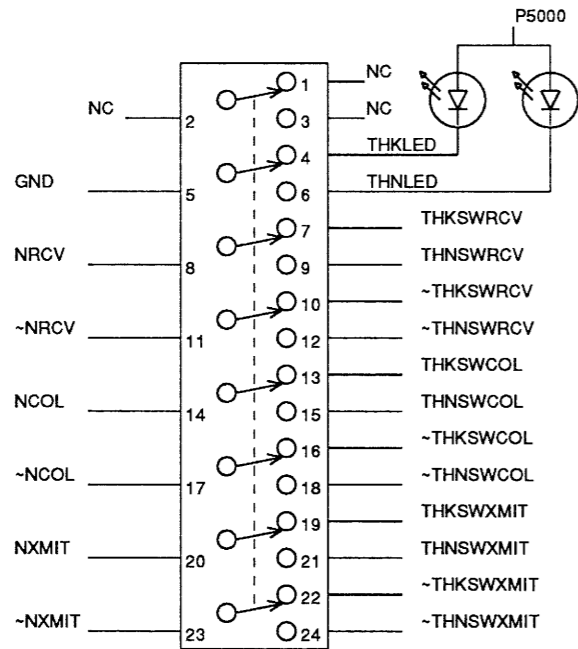
REVISION	
CHK	CHANGE NO. REV

**digital** DRN. DATE  
CHK'D. DATE  
USRA:  
FIRST USED ON OPTION/MODEL:

ENG. M. NIELSEN	DATE 31 OCT 88
BOARD LOCATION:	SHEET 18 OF 21
TOP DOCUMENT NUMBER:	

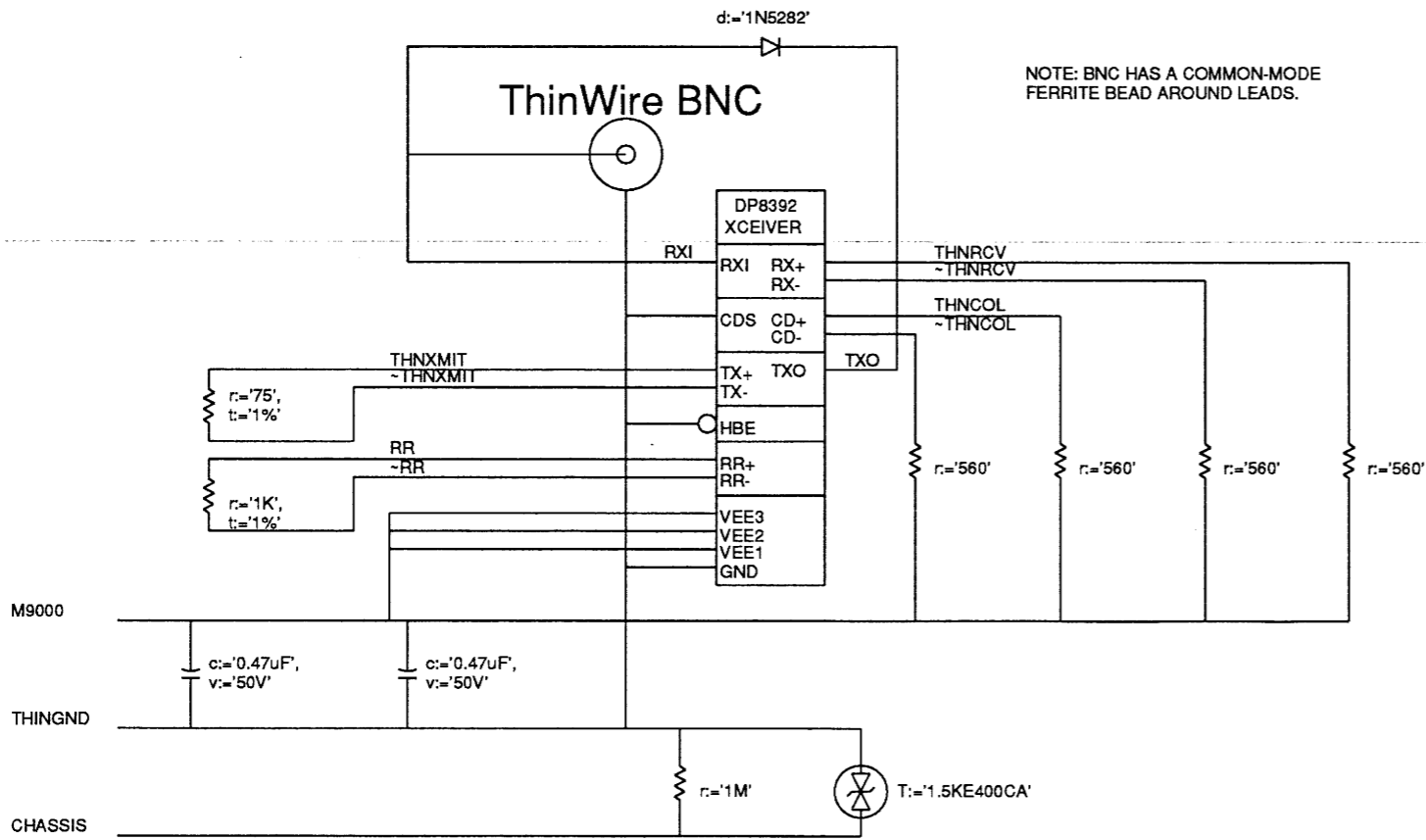
TITLE: Network Interface			
SIZE B	CODE CS	NUMBER 54-19463-01	REV. CX01

### Thin/Thick Selector Switch

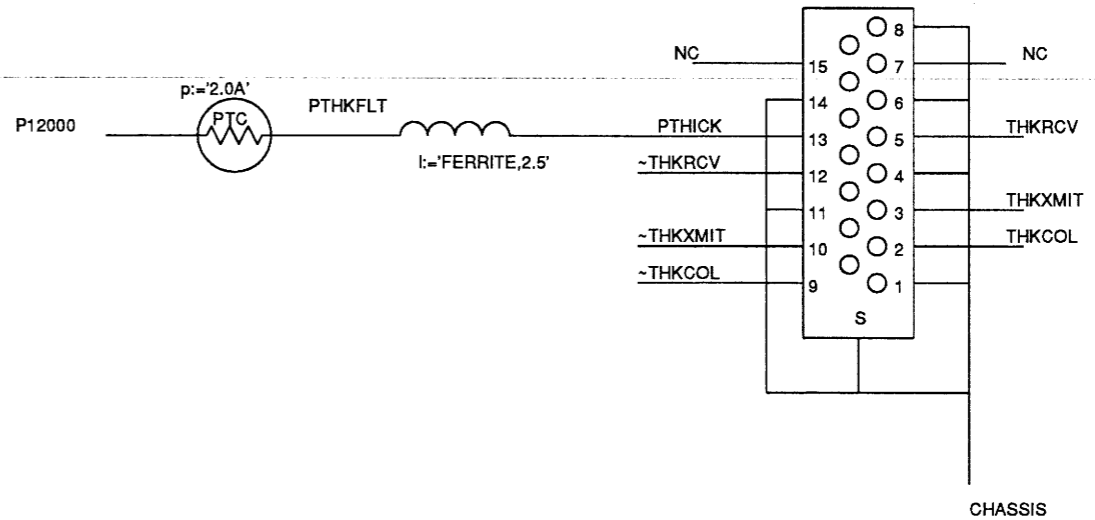


### ThinWire BNC

NOTE: BNC HAS A COMMON-MODE FERRITE BEAD AROUND LEADS.



### ThickWire Connector



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CHK	CHANGE NO.	REV

REVISION

digital DRN. DATE ENG. M. NIELSEN 31 OCT 88 TITLE: Ethernet Transceiver  
 CHK'D. DATE BOARD LOCATION: SHEET 19 OF 21  
 USRA: TOP DOCUMENT NUMBER: SIZE B CODE CS NUMBER 54-19463-01 REV. CX01  
 FIRST USED ON OPTION MODEL:

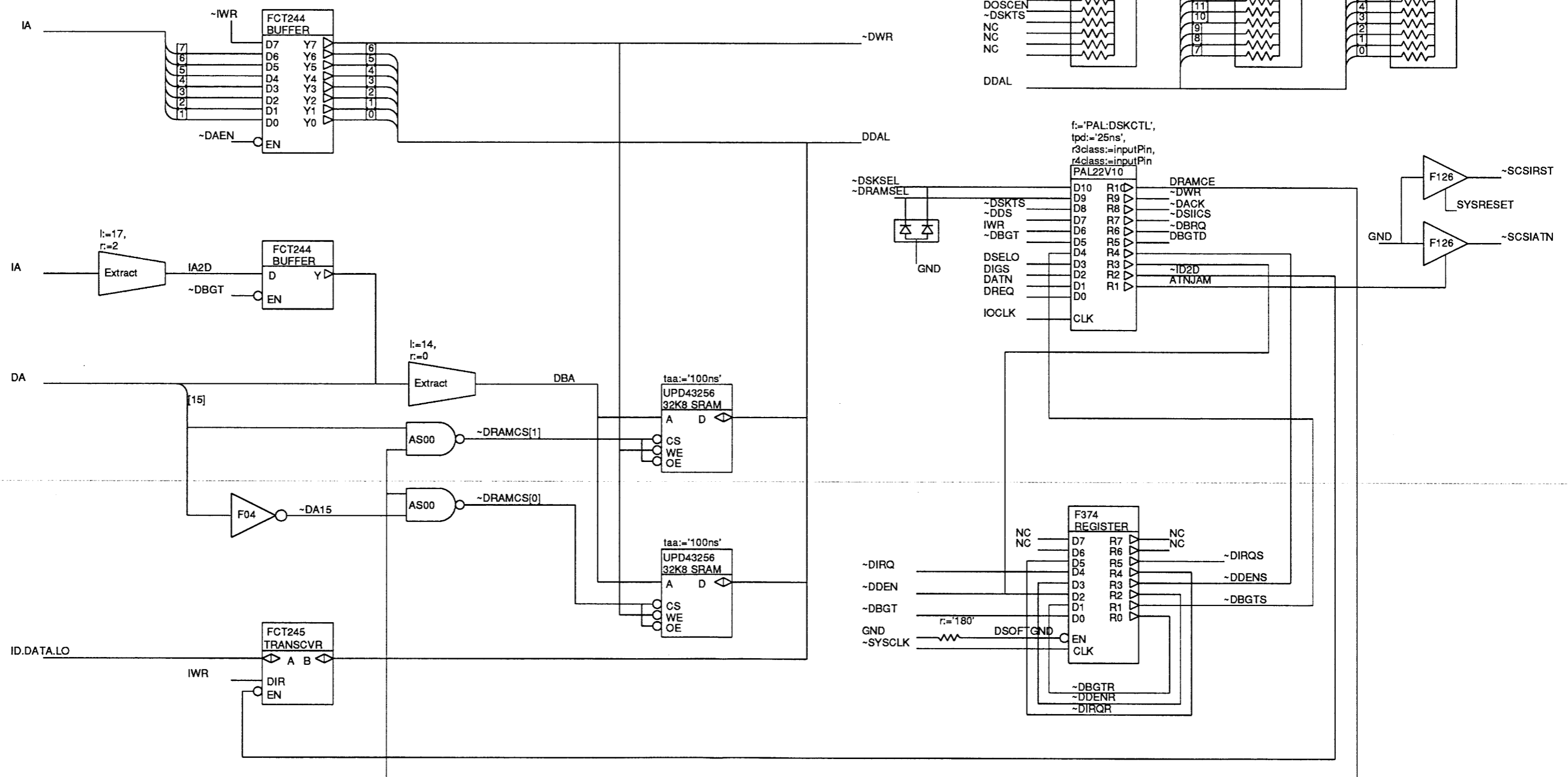
SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01

8 7 6 5 4 3 2 1

Declarations

```
var
  ia2d: bits(16);
  dba: bits(15);
```

NOTE: DISK BUFFER IS 64K 16-BIT WORDS. BUFFER IS 16-BIT-ALIGNED TO SII, 32-BIT-ALIGNED TO CPU. BUFFER HAD 16-BIT ACCESS TO SII AND CPU. SII IS DEFAULT MASTER OF DDAL. CPU IS STALLED FOR SII-CSR OR BUFFER ACCESS IF SII DMA IS IN PROGRESS.

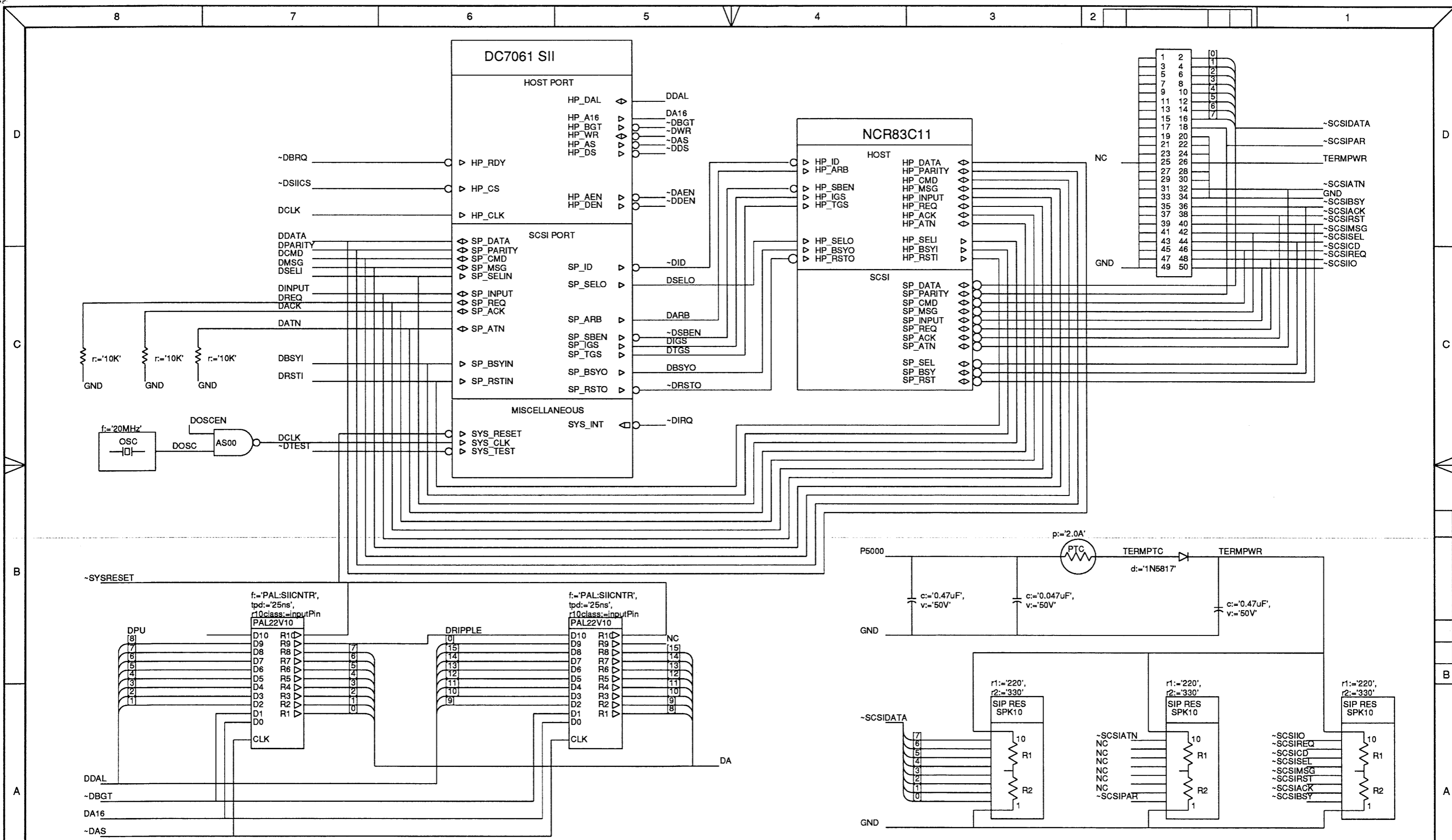


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REVISION		
CHK	CHANGE NO.	REV

**digital** DRN. DATE ENG. M. NIELSEN 31 OCT 88 TITLE: Disk Buffer  
 CHK'D. DATE BOARD LOCATION: SHEET 20 OF 21  
 USRA: TOP DOCUMENT NUMBER: SIZE B CODE CS NUMBER 54-19463-01 REV. CX01  
 FIRST USED ON OPTION/MODEL:

8 7 6 5 4 3 2 1



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REVISION	
CHK	CHANGE NO. REV.

**digital**  
USRA:  
FIRST USED ON OPTION MODEL:

DRN.	DATE	ENG.	DATE	TITLE:
CHK'D.	DATE	M. NIELSEN	31 OCT 88	Disk Interface
SHEET		21 OF 21		SIZE
TOP DOCUMENT NUMBER:		B		CODE
		NUMBER		REV.
		54-19463-01		CX01

SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01