INTEROFFICE MEMORANDUM

M-1099

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SUBJECT Type 14 Memory Expansion

TO PDP Distribution List

FROM Gordon Bell

DESCRIPTION OF THE OPERATION OF MEMORY SWITCHING TYPE 14

Program:

Two types of core memory extension are available for PDP-1. Type 11 allows a total memory size of up to 16K words, and Type 14 up to 32K words. Type 11 uses type 11, type 12, and type 13 memories plus the original machine memory to allow the 16K words. Type 14 memory uses type 14, type 12, type 13, type 15, type 16, type 17, and type 18 plus the original memory to allow the 32K words.

For Type 14 memory, two commands are available to the programmer to allow memory state switching. The command, jump field, jfd Y, is the main command for memory state switching. The command is a two cycle instruction and has the following affect: Memory location Y is taken as an 18-bit memory state code word. The program counter is reset according to bits 5 through 17, bits 0 through 2 are placed in a 3-bit register called DFW, or DATA FIELD WORKING - register, bits 3 to 5 go to a 3-bit register called INSTRUCTION FIELD (IF - register). The DFW register bits are decoded into 8 states which address the data part of one of the eight-4096 word modules. The IF register is decoded into 3 states and address the instruction part of one of eight - 4096 word memory modules.

Normally, the memory address register, a 12-bit register, selects one of 4096 words to be read into the memory buffer register. In the event that Type 14 memory switching is involved, the above registers, i.e., DFW and IF, select which of the eight 4096 word modules are to be taken as the memory, as specified by MA.

The MA and the IF select the memory cell and module if the instruction is a single cycle instruction, i.e., IOT, law, jsp, jmp, and skp. It is also used for the first cycle of a two cycle instruction, except as follows: jda Y, cal Y, jmp Y, jfd Y, and jsp Y all use the memory module specified by IF for cell Y. The DFW and MA registers select the memory module and cell when the address is part of a cycle one instruction, except the above.

When high speed channel transfers are involved, the high speed channel specifies a 3-bit address for one of the eight memories. The high speed channel in this case, also refers to the DFW register. The break cycles also take their module address from the DFW register.

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As was previously stated, the jfd Y command switches the memory fields. Under certain circumstances, it is quite useful to have a previous state of the machine saved in the accumulator when this occurs. Under these circumstances, the defer bit of the jump field command, that is bit 5, specifies whether the jump field command is to save the previous memory state or not. If the defer bit is a one, then the accumulator is cleared and the previous DFW and IF registers are placed in the accumulator (bits 0 - 5) along with the contents of the program counter. When jda or cal commands are given, the DFW and IF registers are also stored along with the program counter.

In many cases, it is desirable to use instructions in a program which operate on instructions, that is instructions tend to treat every operand as data, but in reality the instructions may operate on program. In order to avoid giving a large number of field switching commands (which require 10 microseconds per field switch and also change the program counter) it is desirable to have a 5 microsecond command which will merely change the DFW register. The command sdf changes only the data field register and does not effect the program counter or the instruction field register. The sdf command is actually an in-out transfer command which does not, of course, have the defer bit. The sdf command is specified by the last 6 bits of the in-out transfer. The new contents of the DFW register is specified by bits 9 through 11.

When a break to a sequence occurs, then the AC is stored in the first register, the current instruction field (IF), the current data field (DFW) register, and the program counter (PC), are stored in the second register, and the In-Out is stored in the following register. The sequence break addresses are always taken from memory module zero. Thus, when the break occurs, IF and DFW are both set to zero. A sequence break is terminated by giving a jfd Y command with IF = 0. Y must refer to a register holding the PC, IF and DFW.

MODIFICATIONS TO THE PRINTS USING PDP-1B PRINT NOMENCLATURE

On print D104 which is the PDP-1B accumulator, instead of program counter ones going to the accumulator, program counter, DFT, IF ones go to the accumulator. DFT 1 through 3 goes to AC 0 through 2. IF 1 through 3 goes to AC 3 through 5.

On PDP-1B D105 MA, PC, MB and IO pulse control, the test address ones go to the program counter. Thus, when the test address goes to the program counter, the extended test address specifying the initial IF and DFW all go to the IF and DFT flip-flops. Another

modification is made to allow the program counter to be cleared and to go to PC during the jump field and cycle one. In the control for the AC PDP-1B of print D102, several transistors must be added so that on tp 7, the AC is cleared when there is a jump field command and cyc. ≠ 0, and the MB-5 is a one. On tp 8, the program counter, DFT and IF one's side goes to the accumulator. On BC1, DFT and IF also go to the accumulator.

On print D106, the instruction register and buffers for PDP-1B command 12, which has been previously saved, is defined as the jfd Y command.

On D107, PDP-1B defers cycle and control, it is necessary to add in jump field into the defer cycle so that in the event that MB-5 is a one and a jump field command is present, the machine does not defer.

On Break System Control D-113, the break termination conditions must be modified to occur on tp 2 instead of tp 0, because cy 1 may be slow in occurring. Also, so that this won't occur on any jfd Y, the instruction field register must contain zero, thus for OC 15, three more conditions must be added to make sure that the instruction field is zero.

PDP-1B, D108, mr, mw, and mi flip-flops are removed.

MODIFICATIONS TO REGULAR MACHINE OPERATIONS

Memory Modifications:

The memories must be modified to allow type 11 and type 14 operation. In this regard, a 1540 sense amplifier is used in the memory systems and these sense amplifiers have the property that a strobe (or sample) pulse is put into this sense amplifier package so that the output is a pulse if the memory is reading a one. These 18 pulses for each memory are returned to be mixed for MB outputs.

In the local memory, six packages of 1106's must be added, five of which will be 1106 R and the sixth one a half breed which has three R's. The inverters are used to buffer and isolate the memory address decoder lines. In addition, now, the read, write, and inhibit flip-flops are removed from the main machine and each memory will have a local read, write, and inhibit flip-flop. The read strobe will be generated within each memory. In doing this, a 1607 PA package is added with a 1310 delay plus a 1213 (4 flip-flops) for the read, write, and inhibit flip-flops.

Five select pulses are sent to a memory. One pulse starts the read, (i.e., turns on the read f/f) a pulse turns on the write flip-flop, a pulse turns on the inhibit flip-flop, and a pulse clears the read, write and inhibit flip-flops. There is also a pulse to a memory which starts the local read delay strobe. A pulse is sent

back to the computer, at strobe time, and the computer timing is thus restarted according to the characteristics of a memory.

MODIFICATION TO THE MEMORY BUFFER INPUT, MEMORY INHIBIT, AND MA DECODERS FOR TYPE 14 FIELD SWITCHING

Several line driving circuits will have to be added for field switching. The polarity of the MA decoding has to be reversed to allow a selected line to be at ground. The MA decoders, in turn, drive line driving amplifiers. These levels will then drive directly the 8 memories in parellel. The MB outputs will be beefed up to drive the 18 x 8 memory inhibit lines.

The memory buffer inputs are pulse lines which come back from the individual memories. These pulse lines are mixed locally through a diode package and PA, and then sent on to the MB input as a pulse.

MEMORY MODULE SELECTION FOR TYPE 14

The memory module selection is accomplished by a level which selects either the instruction field register or the data field working register, and the levels enable memory control pulses. The memory restart pulses come back and are mixed in a common mixing PA similar to the sense amplifier output mixing, and the pulse mixer output restarts the time pulse chain.

FIELD FLIP-FLOPS FOR MEMORY MODEL 14

As I previously mentioned, two registers, the data field working register or DFW has three flip-flops, and the IF register has three flip-flops. In addition, there is a register called DFT or DATA FIELD TEMPORARY - register. The purpose for this register is to retain the state of the working register at tp 10 so that if a high speed channel break occurs, the working register will be free to receive the high speed channel address. Memory buffer 9 through 11 go to the working DFW when the switch data field command is given. There is logic to select either data or instructions. Data is selected when a sequence break occurs, the high speed channel is on a one, or cycle one and a data type address. The data type address occurs when not a jump field and not a jda or a cal is given. In addition, there are two other pulse amplifiers which place the ones side of the DFW into the DFT, and DFT ones side goes to DFW. This transfer occurs freely as long as high speed channel is on a zero. In this event, both transfers are inhibited, thus on tp 0, the temporary does not go to the working and the temporary state is retained in DFT, and DFT clearing is inhibited (which normally occurs on tp 9) and on tp 10, the working goes back to the temporary. DFW

ones side goes to DFT unless the high speed channel has occured. The start clear pulse, clears DFT, DFW and IF and then when the test address is set up, the test address goes to DFT and then into the working register, preparatory for the beginning of an instruction on start, examine, or deposit.

The other logic and control allows for a jump field command to begin. When a jump field occurs, the IF and DFW are changed and on the sdf command only, DFW is changed.

On a sequence break, which finds the machine with DFW on a zero on tp 10, on tp 1, DFW again has to be cleared again with DFT keeping the previous state, this DFW = 0 must be used for the first break count module address. On tp 9, the instruction field is cleared and then the thing can operate in a normal mode for the remainder of the break cycles, since IF, DFW and DFT are all zero anyway.