DEC-10-HTMB-D

decsystem10

TM10 MAGNETIC TAPE CONTROL MAINTENANCE MANUAL VOLUME I

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual contains general information, operating, programming, technical reference, and maintenance data for the TM10 Magnetic Tape Control (see Figure 1-1). A working knowledge of the PDP-10 central processor, DF10 Data Channel, TU10, TU20, TU30, and TU40/41 Tape Transports is essential. To aid maintenance personnel in locating reference material, a list of pertinent documents is provided in Paragraph 1.5.

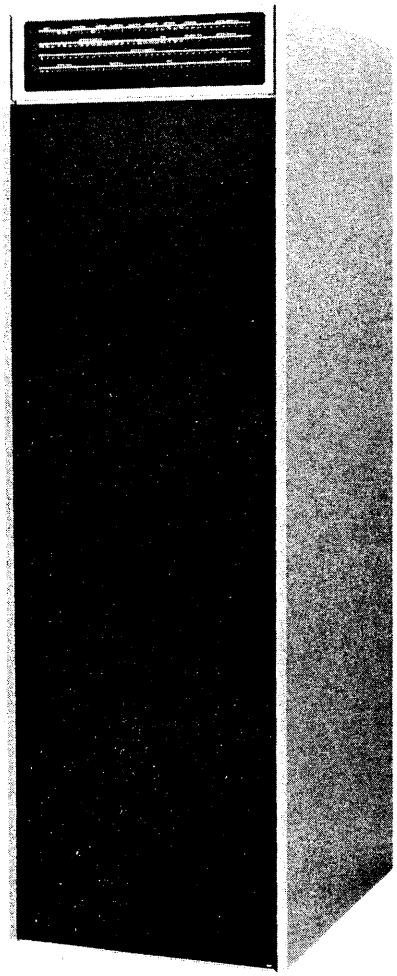


Figure 1-1 TM10 Tape Control

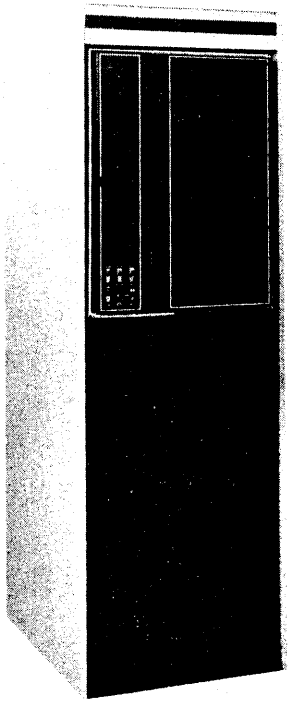
1.2 GENERAL DESCRIPTION

The TM10 Tape Control is an interface between DECsystem-10 core memory and a maximum combination of eight TU10, TU20, TU30, or TU40/41 Magnetic Tape Transports (see Figure 1-2). Each transport is available in two versions that enable information to be recorded in both 7-track and 9-track formats. Data transfer rates and timing depend on the transport, but each transport supplies information to the TM10 such that transports of different speeds and recording formats can be operated by a single TM10 Tape Control. The TU10 and TU20 operate at 45 in. per second, the TU30 operates at 75 in. per second, and the TU40/41 operates at 150 in. per second. Packing density for the various transports is either 200, 556, or 800 bits per inch (bpi).

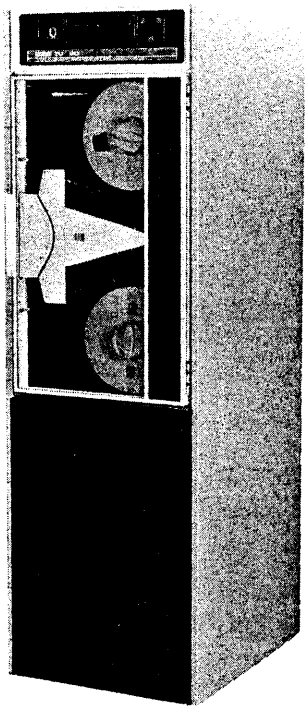
There are two configurations of the TM10: TM10A where transfers between the tape control and core memory are handled by the program over the I/O bus; TM10B where the control is connected to a DF10 Data Channel for automatic transfer of data to and from memory, thus bypassing the central processor. (The TM10B still requires the I/O bus for status and control information transfers.)

1.3 FUNCTIONAL DESCRIPTION

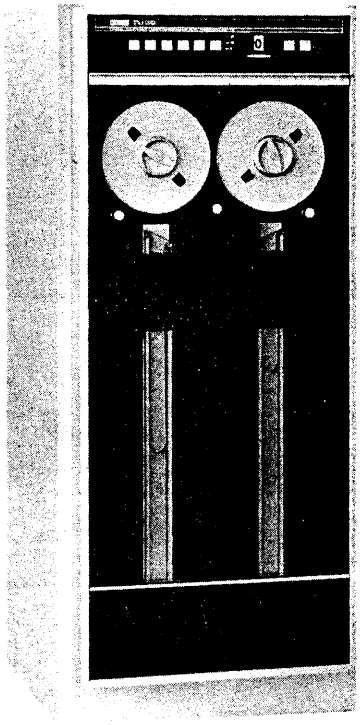
The basic operation of the TM10A and TM10B is identical. During a write operation, the PDP-10 central processor transfers a full 36-bit word to the TM10 Tape Control, which then sends one 7- or 9-bit character at a time to the transport. For a read operation, the control assembles incoming characters into a word for eventual transfer to the DECsystem-10 core memory. The main difference between the TM10A and TM10B is the manner in which the data is transferred between core memory and the control.



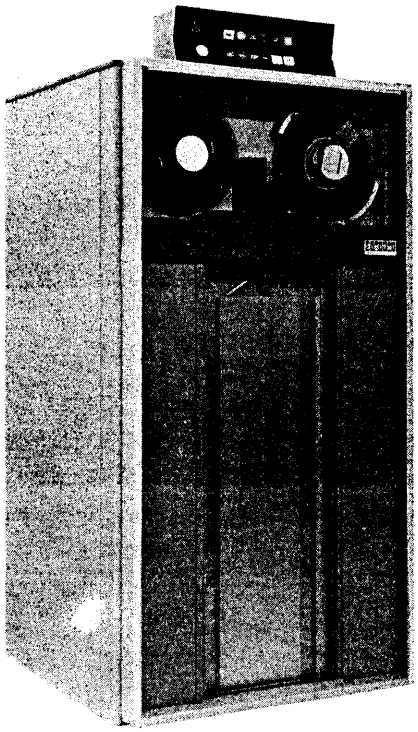
TU10



TU20



TU30



TU40/41

Figure 1-2 TU10, TU20, TU30 and TU40/41 Magnetic Tape Transports

The TM10A uses the PDP-10 I/O bus to transfer data between core memory and the tape control (see Figure 1-3). To write a data word on tape, it must first be transferred to the 36-bit Hold register (HR) in the TM10A and is then loaded into the BR register, which sends one character at a time to the transport. When reading data, the BR register is loaded with the incoming characters until a full word is assembled. The word is then loaded into the HR register. An executive program monitors the data flag interrupt for data requests (either read or write), and data is transferred between the HR and the central processor under control of the I/O instruction.

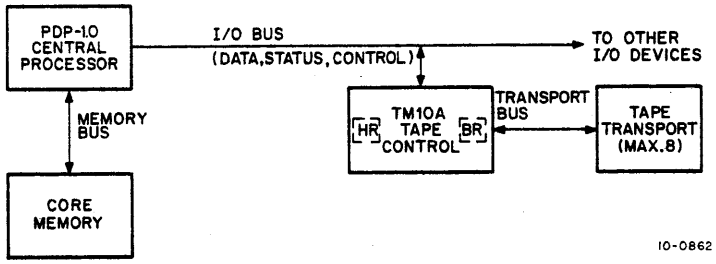


Figure 1-3 TM10A Tape Control Configuration

The TM10B uses the DF10 Data Channel to transfer data between core memory and the tape control (see Figure 1-4). The computer program initializes the TM10B Tape Control and, thereafter, the tape control operates under control of the DF10 Data Channel when transferring data. In the TM10B, the BR register functions the same as in the TM10A: it sends one character at a time to the transport for a write operation and re-assembles characters into words during a read operation. However, unlike the TM10A, the BR register is connected directly to the DF10 Data Channel. The DF10 provides the same buffering feature as the HR register in the TM10A.

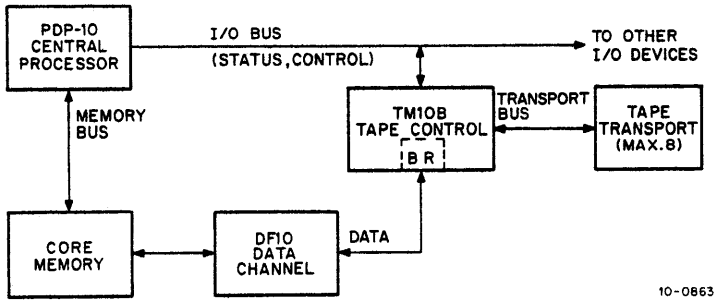


Figure 1-4 TM10B Tape Control Configuration

1.4 SPECIFICATIONS

The following is a list of specifications for the TM10 Tape Control:

Voltage:	115 Vac ±10%, 60 Hz, ±2% 230 Vac ±10%, 50 Hz, ±2%
Current at 115 Vac:	2A, Surge 4A
Power/Heat Dissipation:	300W, 1000 Btu/hr.
Operating Temperature:	60° to 95°F (15° to 35°C)
Storage Temperature:	40° to 110°F (5° to 45°C)
Relative Humidity:	20% to 80%
Height:	69 in. (1.75 m)
Width:	22 in. (0.56 m)
Depth:	29 in. (0.72 m)
Weight:	450 lb (200 kg)

1.5 REFERENCE DOCUMENTS

For further information relevant to the TM10, consult the following related publications:

PDP-10 System Reference Manual	DEC-10-HGAC-D
PDP-10 Interface Manual	DEC-10-HIFB-D
DECsystem-10 Site Preparation Guide	DEC-10-SITE-D
TU10 Magnetic Tape Transport Maintenance Manual	DEC-00-TU10-DA
TU20 Magnetic Tape Transport Maintenance Manual	DEC-00-I4AB-D
TU30 Magnetic Tape Transport Maintenance Manual	DEC-10-H4GA-D
Operation and Maintenance Handbook, Magnetic Tape Systems, Models 20245 and 20247 (Bucode, Inc. manual for TU40 and TU41 Transports).	
DF10 Data Channel Maintenance Manual	DEC-10-I8BB-D
USA Standard Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI)	USAS X3.22-1967

Copies of the above documents are available from:

Digital Equipment Corporation
Communication Services
146 Main Street
Maynard, Massachusetts 01754

CHAPTER 2
INSTALLATION

This chapter contains general information on installation and cabling requirements for both the TM10A and TM10B Tape Control.

2.1 UNPACKING AND INSPECTION

Both the TM10A and TM10B are packed in accordance with the best commercial practices. No special handling procedures are required beyond the normal care afforded any piece of electronic equipment of comparable size and weight. On receipt, the equipment should be inspected for visible damage such as dents and abrasions that may have occurred in transit. Inspect the logic modules for foreign matter that may have lodged in them during shipment. Any damage observed should be reported immediately to both the carrier and DEC.

2.2 SITE CONSIDERATIONS

The TM10A or TM10B should be located in an area free of excessive dirt or corrosive fumes and vapors. Adequate clearance must be provided for servicing the tape control. Refer to Figure 2-1 for applicable cabinet dimensions.

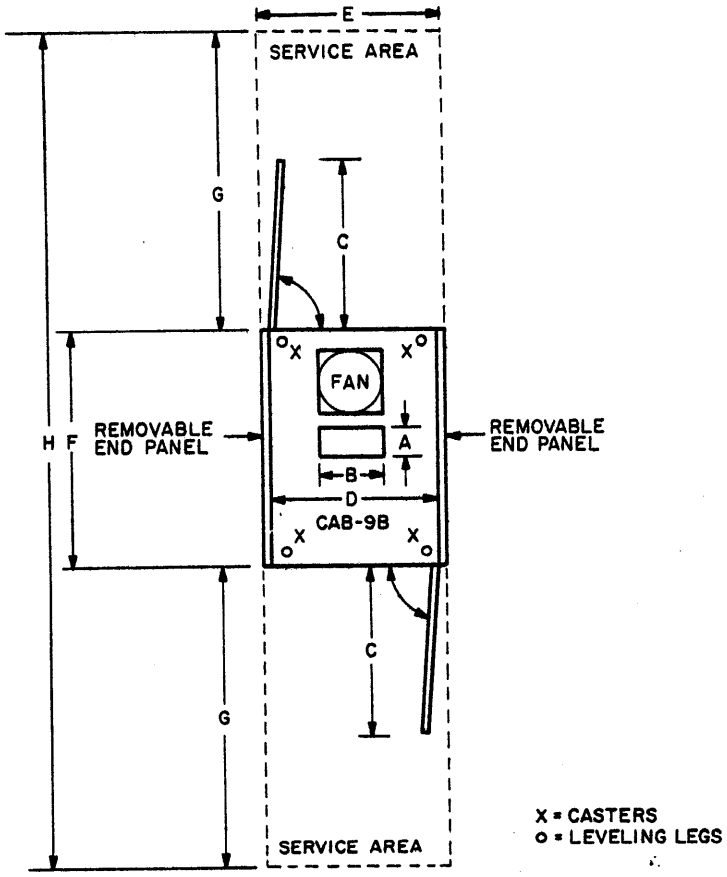
2.3 CABLE CONNECTIONS

Interface connections are required between the PDP-10 CP and the TM10A/TM10B and between the TU10, TU20, TU30, or TU40/41 transport and the TM10A/TM10B. In addition, the TM10B requires interconnections with a DF10 Data Channel.

2.3.1 PDP-10 to TM10A/TM10B

The PDP-10 I/O bus (designated BC10A) is the only connection between the PDP-10 central processor and the TM10A. The physical configuration of the I/O bus is comprised of two coaxial cable sets, which terminate in two W851 Flip-Chip connector assemblies. Table 2-1 lists the I/O bus connections in the TM10. The length of the cables depends on the proximity of the cabinetry and the configuration of the system (maximum I/O cable length is 150 ft). See drawing IOBC for I/O cable pin assignments.

The TM10B also utilizes the PDP-10 I/O bus but only for status and control information transfers. Data transfers between DECsystem-10 core memory and the TM10B occur through the DF10 Data Channel and require three cable assemblies. The cable that carries the actual data is designated BC10A and is similar to the I/O bus cable in that it consists of 36 bidirectional lines and is comprised of two coaxial cable sets, which terminate in two W851 Flip-Chip connector assemblies. The other two channel cables carry the information necessary to synchronize the DF10 with the TM10B. These cable assemblies have six conductors and are terminated at both ends in Type W021 connectors. Table 2-2 lists the DF10/TM10B cable connections.



DIMENSIONS	A	B	C	D	E	F	G	H
INCHES	3.5	7.0	19.3	20.3	22.0	29.0	36.0	100
METERS	0.09	0.18	0.49	0.52	0.54	0.72	0.90	2.50

10-0452

Figure 2-1 TM10A/TM10B Cabinet

Table 2-1
TM10 I/O Bus Connections

Cable	In	Out
I/O Cable #1	KL21,22	KL25,26
I/O Cable #2	KL23,24	KL27,28

Table 2-2
DF10/TM10B Cable Connections

DF10		TM10B	
		Out	In
Channel Cable #1	KL31,32	EF31,32	EF23,24
Channel Cable #2	K21	D31	D29
Channel Cable #3	L21	D32	D30

2.3.2 Tape Transport to TM10A/TM10B

Communication between the TM10A/TM10B and a TU10, TU20, TU30, or TU40 transport is via the transport bus. The bus for the TU20 and TU30 transports is comprised of five cable sets with each one terminating in a W021 connector module. The bus for TU10 and TU40 transports is a single cable equipped with a Quicklatch connector that plugs into the transport. Table 2-3 lists the cable connections between the TM10 and the associated transports.

Table 2-3
TM10/Transport Connections

Function	TM10	Transport	
		TU10, TU40	TU20, TU30
Read Data	N04	Quicklatch connector. Access to receptacle is at bottom rear of cabinet.	C04/D04
Status/Command	N02		C02/D02
Density	N05		C05/D05
Write Data	N01		C01/D01
Control	N03		C03/D03

CHAPTER 3
OPERATION AND PROGRAMMING

This chapter provides information on the TM10 indicator panel, tape format and handling guidelines, and the DECsystem-10 I/O instructions as they apply to the TM10.

3.1 CONTROLS AND INDICATORS

The TM10 has no operating controls; operation is under automatic control of the PDP-10 program. (The operator has local control of motion, e.g., forward, reverse, etc., of the tape system at the respective TU10, TU20, or TU30 transport control panel.) The indicator panel at the top of the TM10 cabinet enables the operator to monitor the status of the internal operation of the TM10 Control. Figure 3-1 shows the indicator panel, and Table 3-1 defines the functions of each indicator when lit. Except where noted, the descriptions pertain to both the TM10A and TM10B.

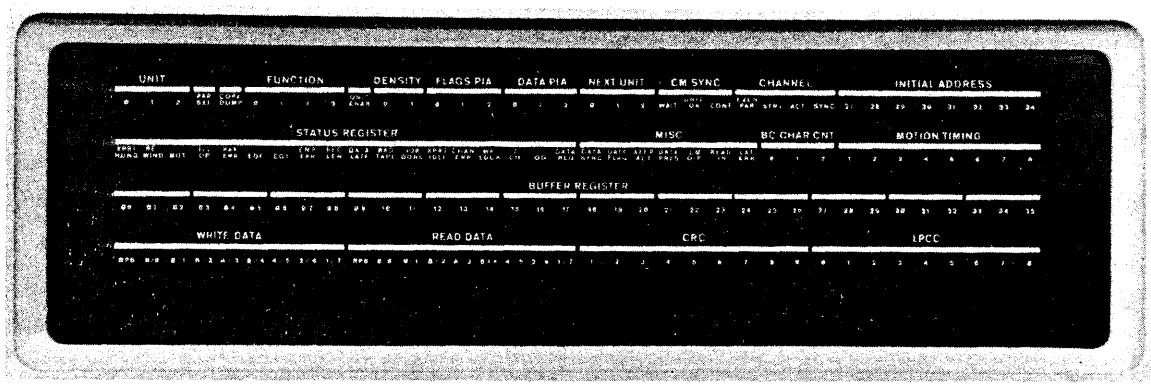


Figure 3-1 TM10 Indicator Panel

Table 3-1
Indicator Panel Description

Group	Indicator	Function
UNIT	0, 1, 2	Indicates the current selected transport. Numbers 0–7 correspond to transports 0–7.
	PAR SEL	Indicates the type of parity; odd parity when lit.
	CORE DUMP	The control is processing tape in core dump format.
FUNCTION	0, 1, 2, 3	Indicates the particular tape function such as Rewind, Read Record or Write (see Table 3-3 for each function code).

(continued on next page)

Table 3-1 (Cont)
Indicator Panel Description

Group	Indicator	Function
FUNCTION (cont)	UNIT ENAB	The LOAD NEXT UNIT flag is enabled to request an interrupt on the flag channel.
DENSITY	0, 1	Indicates the density of the tape being processed. The bits are configured as follows. **Bits** — **Density** 00 — 200 bpi 01 — 556 bpi 10 — 800 bpi 11 — For all transports available at this writing, 11 selects 800 bpi. Should a new density be added, 11 will select it.
FLAGS PIA	0, 1, 2	Indicates the priority assigned to the flag priority interrupt channel.
DATA PIA	0, 1, 2	Indicates the priority assigned to the data priority interrupt channel. Used only in the TM10A; these bits are ignored by the TM10B.
NEXT UNIT	0, 1, 2	Indicates the next transport to be selected for operation after the current transport is finished.
CM SYNC	WAIT	This indicator is on from the time a tape function is given until the addressed transport is ready.
	UNIT OK	This indicator is on from the time a new transport number is loaded until the TM10 starts moving tape.
	CONT	This indicator is on between tape functions when the tape remains in motion.
CHANNEL (TM10B only)	EVEN PAR	The data channel is requested to write even parity into memory.
	STRT	The data channel is connected to this TM10B or any device of lower priority.
	ACT	This indicator is on from the time the TM10B needs the channel until it disconnects.
	SYNC	The TM10B is waiting to connect to the data channel.
INITIAL ADDRESS (TM10B only)	27, 28, 29, 30 31, 32, 33, 34	Indicates the core memory address, which contains the control word for the data channel. The control word contains the starting data address and the word count of the data transfer to be performed by the data channel.
STATUS REGISTER	XPRT HUNG	The addressed transport has failed to respond within one second to a tape-moving function or the addressed transport has gone off-line during a function.
	REWIND	The selected tape is rewinding.
	BOT	The selected tape is at loadpoint.
	ILL OP	A transport has been selected but the TM10 cannot place it in operation because of an illegal condition. Refer to the *PDP-10 System Reference Manual* description of a CONI TMS instruction for an explanation of illegal conditions.

(continued on next page)

Table 3-1 (Cont)
Indicator Panel Description

Group	Indicator	Function
STATUS REGISTER (cont)	PAR ERR	The TM10 encountered a lateral or longitudinal parity error during a Read, Write, or Read-Compare tape function.
	EOF	The TM10 has encountered a file mark on the tape.
	EOT	The selected tape is beyond the endpoint.
	CMP ERR	During a Read-Compare, a word read from tape is not identical to the corresponding word supplied from memory.
	REC LEN	During a Read or Read-Compare, the program underestimated or overestimated the number of words in the record being read.
	DATA LATE	During a Read, Write, or Read-Compare, the program failed to respond in time to a data request.
	BAD TAPE	The TM10 has encountered either data in a record gap or a false end of record.
	JOB DONE	The TM10 has completed a tape function and is ready for the program to give a new function.
	XPRT IDLE	The currently addressed transport is selected and is not now in operation.
	CHAN ERR (TM10B only)	One or more of the following conditions in the data channel has occurred: control word parity error, no such memory, data parity error, and control word written.
	WR LOCK	The supply reel of the selected transport does not have a write enable ring inserted.
	7 CH	The selected transport handles 7-track tape (when not lit, the indicator signifies either 9-track tape or no transport selected).
	GO	The TM10 is moving tape.
	DATA REQ	The TM10 is ready for a data transfer.
MISC	DATA SYNC	Synchronization is achieved between the data I/O instructions and the TM10A or between the data channel and the TM10B.
	DATA FLAG	Synchronizes transfers to and from the internal BR register.
	XFER ACT	Transfers or spacing are occurring.
	DATA PRES	The tape is within a data record.
	CM DIR	The selected tape is up to speed in reverse. Remains lit until a tape is up to speed forward or the TM10 stops tape and executes a function that does not move tape.
	READ IN	The TM10 is initiating Rewind in readin mode.
	LAT ERR	Lateral parity error.
BC CHAR CNT	0, 1, 2	Character counter.
MOTION TIMING	1, 2, 3, 4, 5, 6, 7, 8	Counter that controls motion timing outside of the record areas.

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Table 3-1 (Cont)
Indicator Panel Description

Group	Indicator	Function
BUFFER REGISTER	00 through 35	Displays contents of BR buffer register.
WRITE DATA	WPB, 0/0, 0/1, B/2, A/3, 8/4, 4/5, 2/6, 1/7	Write character buffer; 9-bit characters are on right-hand side of slash.
READ DATA	RPB, 0/0, 0/1, B/2, A/3, 8/4, 4/5, 2/6, 1/7	Read character buffer; 9-bit characters are on right-hand side of slash.
CRC	1 through 9	Cyclic redundancy character (CRC) register.
LPCC	0 through 8	Longitudinal parity check character (LPCC) register.

3.2 TAPE FORMAT

The TM10 Control, in conjunction with the selected tape transport, writes characters containing seven or nine bits of information; one bit is written in each track. The following paragraphs describe the 7- and 9- track formats.

3.2.1 Seven-Track Format

The 7-track system uses 1/2 in. tape with seven information channels; the format is shown in Figure 3-2. The left side of Figure 3-2 shows the tape in relation to the read and write heads. This tape is composed of a Mylar base coated on one side with an iron oxide composition. The oxide, or dull side of the tape, faces the heads with the left edge toward the transport drive plate. The recording density is 200 bpi (bits per inch), 556 bpi, or 800 bpi. The method of recording is non-return-to-zero, change on one (NRZI).

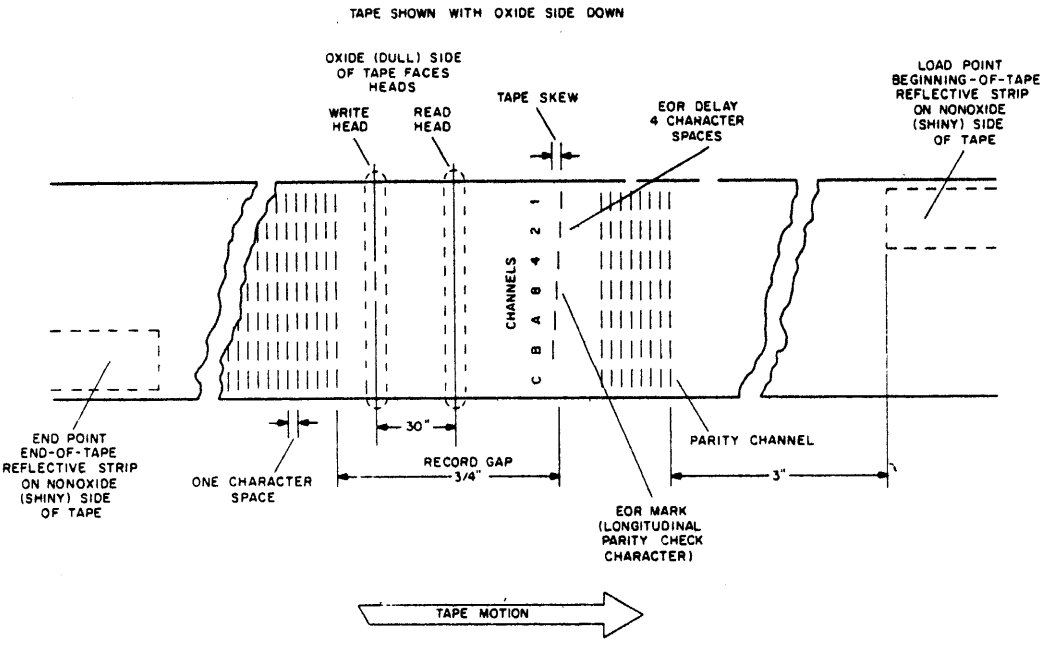

Figure 3-2 7-Track Tape Format

In NRZI recording, the direction of the writing current is reversed every time a logical 1 is to be recorded. Therefore, a 1 is represented by either a positive or negative pulse, while a 0 is represented by the absence of a pulse.

The structure and relative spacing of the individual tape characters are shown in the right portion of Figure 3-2. Each 36-bit computer word is divided into six 6-bit characters. However, the writers contain seven flip-flops corresponding to the seven tape channels; the seventh channel is a lateral parity channel. The parity of the character may be either odd (binary) or even (BCD) as specified by the program. In reading the tape, only 1s are detected.

The smallest unit of information that can be written on the tape is a record; since each computer word contains six 6-bit characters, a record contains N X 6 data characters, where N is the number of words that the processor transfers.

After the last data character of the record is written, the tape travels slightly over three character spaces of blank tape (EOR gap), and then clears the write buffer to produce an end-of-record character, the EOR mark. The bit configuration of the EOR mark produced by clearing the write buffer leaves an even number of 1 bits in each of the seven channels of the tape. All bits of the write buffer start in the 0 state; to end in the 0 state, they must undergo an even number of transitions. For this reason, the EOR mark is referred to as the longitudinal parity-check character (LPCC). Besides detecting changes in magnetization through the read heads, the tape transport also includes a photo-electric system for sensing the beginning and end of the tape (BOT and EOT).

The load and end points of the tape are marked by reflective strips mounted on the side of the tape away from the head (see Figure 3-2). These strips are detected by photodiodes, which sense the light reflected from them. In writing on a rewound tape, a gap of about 3 in. is left from the load point before writing begins. When the load point is sensed during a fast rewind condition, the sensing device shuts off the high-speed rewind.

3.2.2 Nine-Track Format

The 9-track tape format, shown in Figure 3-3, is similar to 7-track except that eight data bits and one parity bit are provided across the width of the tape. In addition, a CRC (cyclic redundancy check) character is written after the EOR gap and then followed by the LPCC character.

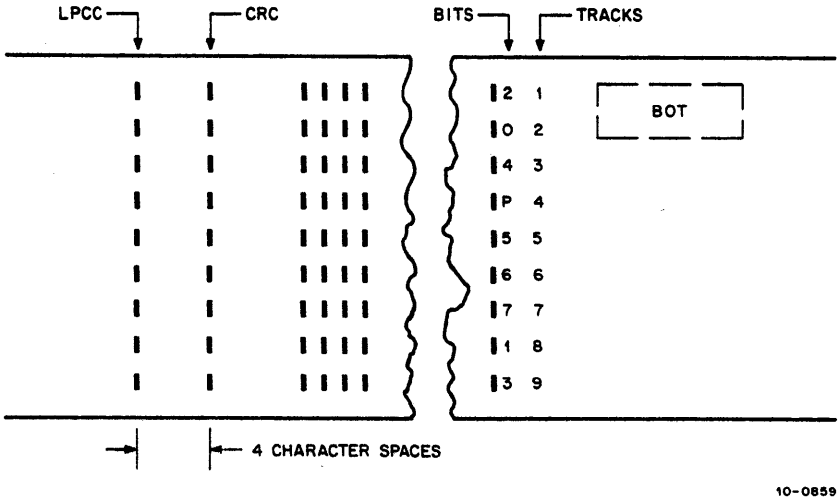

Figure 3-3 9-Track Tape Format

The TM10 writes bits 0–31 of each 36-bit word in four 8-bit characters, ignoring bits 32–35 altogether (see Figure 3-4). When the TM10 reads a record, it assembles data into 36-bit words. Each word is composed of four data bytes in bits 0–31 and the corresponding character parity error indicators in bits 32–35 (e.g., a 1 in bit 33 indicates an error in the character from which the byte in bits 8–15 was taken).

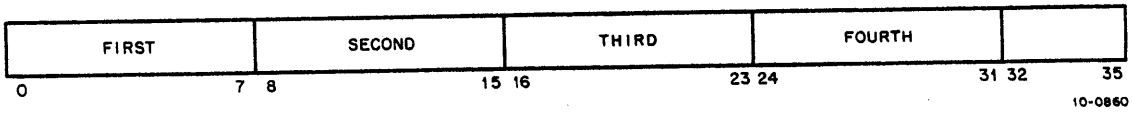

Figure 3-4 9-Track Byte Distribution

The CRC character is an error correcting feature whereby a suitable program can determine if errors are in one channel of the tape and, if so, correct them. If errors are confined to a single track, the program can correct the record by complementing the bit from the bad track in every byte whose error bit is 1.

To write the CRC character, the TM10 Control incorporates a nine-position register CRC1 through CRC9 with the following track assignments:

Register Position	CR1	CR2	CR3	CR4	CR5	CR6	CR7	CR8	CR9
Track Number	4	7	6	5	3	9	1	8	2

To derive the CRC character, all data characters are exclusive ORed into the CRC register. Between character transfers, the CRC is rotated one position, CRC1 to CRC2, CRC2 to CRC3, . . . , and CRC9 to CRC1. If shifting causes a 1 in CRC1, then the bits shifted into CRC4, CRC5, CRC6, and CRC7 are inverted. After the last data character has been added (exclusive ORed), the CRC register is again shifted and, if CRC1 becomes 1, CRC4, CRC5, CRC6, and CRC7 are inverted.

To write the CRC character on tape, all bit positions except CRC4 and CRC6 are inverted. An odd parity CRC character occurs if the number of data characters within the block is even, and an even parity CRC character occurs if the number of data characters within the block is odd. The CRC character may contain all 0 bits; in that case, the number of data characters was odd.

The LPCC character for 9-track format is the same as for the 7-track format.

To facilitate the use of 9-track tape for binary data applications, a core dump format is available in which the program can select any density. The TM10 uses the 9-track record format but writes full 36-bit words as five characters each: the first four bytes are taken from bits 0–31 of a word in the same manner as in 9-track format; the fifth data byte contains 0s in tracks 0 and 1, a repeat of bits 30 and 31 in tracks 2 and 3, and bits 32–35 in tracks 4–7 (see Figure 3-5). During reading, the two bits that overlap (bits 30,31) are ORed together. The CRC is written in the usual manner, but no error bits are supplied with the data bytes.

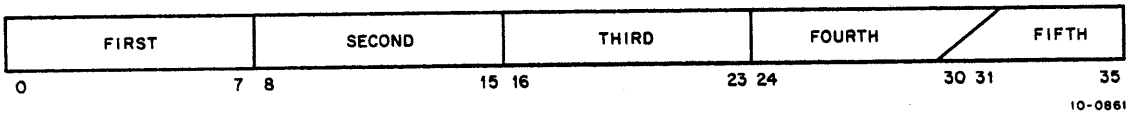

Figure 3-5 Core Dump Byte Distribution

3.3 TAPE HANDLING

When handling magnetic tapes and reels, it is important to observe certain precautions to prevent loss of data and/or damage to tape handling equipment. These precautions are:

a. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

(continued on next page)

c. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape transport operation.

d. Always store tape reels inside their containers. Keep empty containers closed to prevent dust and dirt from getting inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the transport or tape storage area. Tobacco smoke and ash are expecially damaging to tape.

g. Do not place the transport near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Methods of storing and cleaning magnetic tape are presented in Chapter 5 of this manual.

3.4 PROGRAMMING

This section describes the programming of both the TM10A and TM10B systems to satisfy any detailed programming requirements. Frequently, however, the programmer will not need the detailed procedures for programming the TM10A and TM10B described because the PDP-10 monitor provides call statements to the magnetic tape I/O driver subroutine that satisfy most of his requirements. The applicable PDP-10 document should be consulted for these procedures and call statements. Refer also to the *PDP-10 System Reference Manual* for detailed descriptions of the I/O instructions for the TM10.

The TM10 has two device codes, 340 and 344, mnemonics TMC and TMS. Device code 340 is used for transmitting data (with a TM10A) and command information; device code 344 is used for sending the initial data channel control word address to a TM10B and reading status. Device codes 350 and 354 are used for a second TM10 tape system.

3.4.1 TM10A Programming

The TM10A operates under complete control of an executive program for all tape operations. The executive initiates an operation by issuing a CONO 340 (CONO MTC) instruction. The format of this instruction (see Tables 3-2 and 3-3) specifies the parameters, the particular tape function, and starts the operation. A request for data transfer (either to or from core memory) is accomplished by use of the data interrupt channel. For example, during a write operation the DATA REQUEST flag is raised to signify that the tape control requires the next 36-bit word to be recorded. The flag generates a DATA interrupt and the executive program responds to this interrupt by issuing a DATAO 340 instruction to transfer the 36-bit word to the tape control via the I/O bus. Moreover, the executive monitors the number of data transfers to determine when to stop the write operation. It stops the operation by issuing a CONO 344 (CONO MTS) with bit 35 set to 1. The program monitors tape status (see Table 3-4) by use of the CONI 344 (CONI MTS) instruction.

Table 3-2
CONO/CONI 340 (MTC) Instructions

Bit	Name	Function
15–17	NEXT UNIT NUMBER	Specifies the next tape transport number selected for operation.
18–20	UNIT NUMBER	Specifies the current tape transport number selected for operation.
21	PARITY	1 = Odd; 0 = Even
22	CORE DUMP	0 = 4 Bytes; 1 = 4-1/2 Bytes (applicable only for 9-channel tape)

(continued on next page)

Table 3-2 (Cont)
CONO/CONI 340 (MTC) Instructions

Bit	Name	Function
23–26	FUNCTIONS	Tape functions (see Table 3-3 for encoded functions).
27	NEXT UNIT ENAB	When set, enables the NEXT UNIT flag to generate an interrupt.
28, 29	DENSITY	0 = 200 bpi; 1 = 556 bpi; 2 = 800 bpi; 3 = reserved for future use (presently will also select 800 bpi)
30–32	FLAG PIA	Specifies the priority assigned to the flag priority interrupt channel.
33–34	DATA PIA*	Specifies the priority assigned to the data priority interrupt channel.

*Used only on the TM10A, always contains 1s in TM10B.

Table 3-3
TM10 Functions

Function	Octal Code	Description
0000	0	No-op, clear interrupt flags.
1000	10	No-op, interrupt when transport becomes idle.
0001	1	Rewind
1001	11	Rewind/Unload
0010	2	Read
1010	12	Read across record boundaries.
0011	3	Read/Compare
1011	13	Read/Compare across record boundaries.
0100	4	Write
1100	14	Write with long EOR gap.
0101	5	Write end-of-file.
1101	15	Write blank tape.
0110	6	Space forward one or more records.
1110	16	Space to end-of-file.
0111	7	Space reverse one or more records.
1111	17	Space reverse to end-of-file.

3.4.2 TM10B Programming

The TM10B uses the DF10 Data Channel to transfer data from PDP-10 core memory to the TM10B. An executive program must control the operation of both the DF10 Data Channel and the TM10B. (Refer to the *DF10 Data Channel Manual* for program control of the data channel.) The executive program starts operation when it issues a CONO MTC instruction as it does for the TM10A. But first, the program must issue a DATAO 344 to transfer the initial control word address for the data channel to the TM10B where it is held until the TM10B gains access to the data channel.

3.4.3 Command Bits – TM10A, TM10B

Bits transmitted via CONO MTC have the meanings described in Tables 3-2 and 3-3. The unit number bits select one of eight transports. The parity bit selects even or odd parity checking; 0 for even, 1 for odd (preferred parity is odd). The core dump bit should be used with 9-channel transports only. With the core dump bit = 1 and 9-channel tape, the TM10 writes out 36-bit words onto 9-channel tape by splitting the data up among five 8-bit bytes.

Function encoding is shown in Table 3-3. A detailed description of each function is provided in Paragraphs 3.4.5 (TM10A) and 3.4.6 (TM10B).

The NEXT UNIT INTERRUPT ENABLE is used in conjunction with the no-op function to allow testing of the transport status bits. If the control is not free when a CONO MTC is given (between JOB DONE and IRD OVER), there is a delay until the current transport can be deselected and the new one selected. The next unit interrupt allows the program to examine the transport status bits at the earliest opportunity. Without the enable bit, the earliest possible interrupt that could be forced would occur when the transport becomes ready (which may be long delayed, by a rewind for instance).

Any one of three bit densities may be selected, 200 bpi, 556 bpi, or 800 bpi. The encodings for these are 00, 01, and 10, respectively; with encoding 11 currently acting the same as 10, but reserved for future revisions. If 9-track tape is being used without the core dump bit, the program must select 800 bpi.

3.4.4 Status Bits – TM10A, TM10B

Table 3-4 lists the functions of each status bit as sensed by the CONI instruction. Detailed descriptions of each bit assignment (when set) follow the table.

Table 3-4
Status Register (CONI 344 Format)

Bit	Name	Interrupt
11	CW PAR ERR*	
12	NO-EX MEM*	
13	DATA PAR ERR*	Flag Channel
14	WT CW DONE*	Flag Channel
15–17	Character Counter	
18	TRANSPORT HUNG	Flag Channel
19	REWINDING	
20	BOT (beginning of tape)	
21	ILLEGAL OPERATION	Flag Channel
22	PARITY ERROR	
23	EOF (end-of-file)	
24	EOT (end-of-tape)	
25	READ/COMPARE ERROR	
26	RECORD LENGTH INCORRECT	
27	DATA LATE	
28	BAD TAPE	
29	JOB DONE	Flag Channel
30	TRANSPORT IDLE	
31	CHANNEL ERROR*	
32	WRITE LOCK	
33	7-CHANNEL TRANSPORT	
34	NEXT UNIT	Flag Channel, if enabled
35	DATA REQUEST	Data Channel**

*TM10B only
**TM10A only

Bit 11 (Control Word Parity Error) — Signifies the DF10 Data Channel encountered a core memory parity error when fetching a control word. Data transfers cease immediately, and the TM10B terminates the function at the end of the current record. (The TM10A reads this bit as a 1 but ignores its significance.)

Bit 12 (No Such Memory) — Signifies the DF10 Data Channel encountered a non-existent memory location on a core memory reference. Data transfers cease immediately, and the TM10B terminates the function at the end of the current record. (The TM10A reads this bit as a 1 but ignores its significance.)

Bit 13 (Data Parity Error) — The DF10 Data Channel encountered a core memory parity error when fetching a data word. This bit causes an interrupt on the flag channel. (The TM10A reads this bit as a 1 but ignores its significance.)

Bit 14 (Control Word Written) — Indicates that the DF10 Data Channel has written the current control word into initial address +1 (as requested). This bit causes an interrupt on the flag channel. (The TM10A reads this bit as a 1 but ignores its significance.)

Bits 15, 16, 17 (Character Counter) — These bits are primarily for maintenance; the character counter controls the division and assembly of data words.

Bit 18 (Transport Hung) — Signifies the TM10 has waited for one second and the selected transport has not completed its operation or else has been switched off-line during an operation. This bit causes an interrupt on the flag channel.

Bit 19 (Rewinding) — Indicates the selected tape is rewinding.

Bit 20 (Loadpoint) — Indicates the selected tape is at loadpoint.

Bit 21 (Illegal) — Signifies that an improper command has been issued, such as write with the file protect ring out (write lock on).

Bit 22 (Tape Parity Error) — Signifies incorrect parity, either lateral or longitudinal. (This bit is not significant until after JOB DONE sets.)

Bit 23 (End of File) — Signifies an end-of-file record was read from the tape.

Bit 24 (Endpoint) — Indicates the selected tape is beyond the endpoint.

Bit 25 (Read-Compare Error) — Signifies that during a Read/Compare operation the data read from the tape was not the same as the data sent out by a DATAO MTC.

Bit 26 (Record Length Differs) — Indicates that the number of words in a record to be read were underestimated or overestimated.

Bit 27 (Data Late) — Signifies that the program (TM10A) or the data channel (TM10B) failed to respond in time to a data request.

Bit 28 (Bad Tape) — Signifies that data was detected in the end-of-record gap. This could indicate missed characters or noise in the end-of-record gap, either of which are caused by faulty tape.

Bit 29 (Job Done) — Indicates the control has completed a function and is ready for the program to give a new function. The setting of this bit requests an interrupt on the flag channel.

Bit 30 (Unit Idle) — Indicates the currently addressed transport is selected and is not now in operation.

Bit 31 (Channel Flag) — Signifies that either bit 11, 12, 13, or 14 (described above) is a 1.

Bit 32 (Write Lock) — Indicates the supply reel of the selected transport does not have a write enable ring inserted.

Bit 33 (7 Track) – Signifies the selected transport handles 7-track tape (a 0 indicates 9-track tape or no transport selected).

Bit 34 (Load Next Unit) – Signifies the TM10 is not moving tape and a CONO MTC given now will select a transport. The setting of this bit requests an interrupt on the flag channel if NEXT UNIT INTERRUPT ENABLE is a 1.

Bit 35 (Data Request) – Indicates the TM10 control is ready for a data transfer. In the TM10A, the setting of this bit requests an interrupt on the data PI channel.

3.4.5 TM10A Tape Functions

This section describes the TM10A tape functions as listed in Table 3-3. The octal code is included adjacent to the function name.

No-op (0) – Clears all status bits except those associated with the transport and NEXT UNIT.

No-op (10) – Loads a new current transport number and sets JOB DONE when the transport becomes ready.

Rewind (1) – Rewinds the selected transport. Sets JOB DONE as soon as the transport is up to speed. To interrupt at the end of a rewind, wait for JOB DONE and then use no-op (10).

Rewind and Unload (11) – Rewinds the selected transport, places the transport off-line, and pulls the tape all the way out of the vacuum columns. Status bit XPORT HUNG is set after 1 second because the transport is off-line; JOB DONE is not set.

Read (2) – Data is read in the forward direction only. The parity and density must be set the same as when the data was written. ILLEGAL OP is set if the transport is 9-channel and neither 800 bpi nor core dump mode is selected. The DATA REQUEST flag is raised whenever a 36-bit word is ready for the processor. JOB DONE is set at the end of record. If the program issues a CONO MTS, 1 after the last word in a record is read, the RECORD LENGTH INCORRECT flag stays off; this flag comes on if the record ends prematurely (the program never issues CONO MTS, 1 or does so late) or if another data word follows the CONO MTS, 1; in the latter case, the following words are ignored. DATA LATE is set when the control assembles a 36-bit word and the program has not done a DATAI for the previous 36-bit word. The average DATAI rate must equal the word rate from the tape transport. The maximum time between DATAIs, assuming the most favorable possible timing, is 2-1/6 times the word rate for 7-channel tape, 2-1/5 for 9-channel core dump mode, and 2-1/4 for 9-channel compatible mode. If an end-of-file is encountered in READ mode, there are no DATA REQUESTS and the EOF flag will be set along with JOB DONE.

Read Across Record Boundaries (12) – Like READ (2), except that JOB DONE is set only at the first end-of-record after an error, or at an end-of-file, or after CONO MTS, 1 is given, or if the number of characters in a record is not a multiple of six for 7-channel tape. Thus, a single BLKI can read in several records.

Read/Compare (3) – Data is read from the tape by the control and the program sends data from core via DATAO. The two words are compared in the control and, if equal, the process continues with the next pair of words. If not equal, there are no further DATA REQUEST flags and the READ/COMPARE ERROR flag is set at the end of the record. The first DATA REQUEST occurs when the tape begins to move. For other flags, modes, and timing considerations, see READ mode.

RD/CMP Across Record Boundaries (13) – Like READ ACROSS RECORD BOUNDARIES (12), but compares each word read with a word supplied from core memory.

Write (4) – Data may be written in any of three densities (200 bpi, 556 bpi, or 800 bpi) on 7-channel transports, at 800 bpi in IBM-compatible format on 9-channel transports, or at any of three densities in core dump mode on 9-channel transports. Either even or odd parity may be selected. When selecting even parity, care must be taken

to never write a character of all 0s on tape, because such a character will be ignored while reading. A WRITE command to a write-locked tape results in the ILLEGAL OP flag and no tape motion. To terminate a record, the program must follow the last DATAO with the CONO MTS, 1. There will be no further data requests; JOB DONE is set when the read-after-write circuit reads and checks the longitudinal parity. The BAD TAPE flag could be set at this time. If the CONO MTS, 1 is not given, the TM10A raises the DATA LATE flag, rewrites the last data word, and then writes an end-of-record and stops. The first DATA REQUEST occurs when the tape starts moving. Other timing considerations are the same as for READ mode.

Write With Extended EOR Gap (14) — Similar to WRITE (4) except that a 3 in. gap of blank tape (instead of 3/8 in.) is written prior to the start of the WRITE operation.

Write End Of File (5) — An end-of-file character and end-of-file gap are written on the tape. The parity is set automatically. The END-OF-FILE and JOB DONE flags are raised when the function is completed. ILLEGAL OP is raised and no tape motion results if the tape is write-locked. BAD TAPE and PARITY ERROR can also be set, indicating miswriting.

Write Blank Tape (15) — Writes approximately 3 in. of blank tape and sets JOB DONE when completed. On 9-channel tape, the density must be 800 bpi.

Space Forward (6) — Any number of records may be spaced with a single SPACE FORWARD command. For each record, the TM10A raises the DATA REQUEST flag. The program should respond with a DATAO MTC, or BLKO (the data word itself is irrelevant). If the program does not respond (or responds late), the TM10A spaces one record and stops the tape. If the program responds, the TM10 spaces one record and raises the DATA REQUEST flag again. To space a second record, the program must give another DATAO MTC. If the program gives a CONO MTS, 1, the TM10 does not raise the DATA FLAG again and stops at the end of the current record. To summarize: the TM10A spaces one record for each DATAO from the program except that one record is spaced for 0 DATAOs. The TM10 stops spacing at an end-of-file, regardless of DATAOs. The TM10 also stops spacing at the first end-of-record following the EOT marker. JOB DONE is raised when the TM10 has finished spacing the last record.

The same density in which the tape was written must be selected. At lower density, the TM10 can miss an end-of-file mark. Parity is not relevant. CORE DUMP must be selected to allow a density of 200 bpi or 556 bpi on 9-channel tape. Other relevant flags are BAD TAPE and EOF.

Space Forward To End Of File (16) — Spaces any number of records and stops only for an END-OF-FILE or EOT flag. The DATA REQUEST flag is never raised. Otherwise, this function is similar to SPACE FORWARD (6).

Space Reverse (7) — Spaces one or more records in reverse. The control of the number of records spaced is the same as for SPACE FORWARD (6). Regardless of the number of DATAOs given, the TM10 stops a SPACE REVERSE operation at an END-OF-FILE or at the BOT (beginning of tape, or loadpoint) marker. The EOT marker is ignored. ILLEGAL OP is raised if SPACE REVERSE is attempted and the tape is at the BOT at the start of the operation (no tape motion results). Otherwise, this function is similar to SPACE FORWARD (6).

Space Reverse To End-Of-File (17) — Spaces any number of records in reverse and stops only for an END-OF-FILE or BOT flag. The DATA REQUEST flag is never raised. Otherwise, this function is similar to SPACE REVERSE (7).

3.4.6 TM10B Tape Functions

This section describes the TM10B tape functions as listed in Table 3-3. The octal code is included adjacent to the function name.

No-op (0) — Clears all status bits except those associated with the transport and NEXT UNIT.

No-op (10) — Loads a new current transport number and sets JOB DONE when the transport becomes ready or sets TRANSPORT HUNG after one second. Note the NEXT UNIT ENABLE bit description.

Rewind (1) — Rewinds the selected transport. Sets JOB DONE as soon as the transport is up to speed. To interrupt at the end of a rewind, wait for JOB DONE and then use no-op (10).

Rewind and Unload (11) — Rewinds the selected transport, places the transport off-line, and pulls the tape all the way out of the vacuum columns. Status bit XPORT HUNG is set after 1 second because the transport is off-line; JOB DONE is not set.

Read (2) — Data is read in the forward direction only. The WC register in the data channel specifies the number of words to read. The parity and density must be set the same as when the data was written. ILLEGAL OP is set if the transport is 9-channel and neither 800 bpi nor core dump mode is selected. JOB DONE is set at the end of the record. Tape begins to move when the data channel is seized. If the data channel terminates operation after the last word in a record is read, the RECORD LENGTH INCORRECT flag stays off; this flag comes on if the record ends prematurely (data channel never terminates operation) or if another data word follows the data channel termination; in the latter case, the following words are ignored. DATA LATE is set when the control assembles a 36-bit word and the data channel has not transferred the previous 36-bit word.

Read Across Record Boundaries (12) — Like READ (2), but JOB DONE is set only at the first end-of-record after an error, or at an end-of-file, or after the data channel terminates operation, or if the number of characters in a record is not a multiple of six for 7-channel tape (or a multiple of four or five for 9-channel tape in the IBM-compatible or core dump modes, respectively).

Read/Compare (3) — Data is read from the tape by the control, and the program sends data from core via the data channel. The WC register in the data channel specifies the number of words to read/compare. The two words are compared in the control and, if equal, the process continues with the next pair of words. If not equal, the READ/COMPARE ERROR flag is set at the end of the record.

In READ/COMPARE mode (3 or 13), the data channel supplies the first data word before the TM10 is ready to receive it. Therefore, the first word of data from memory must be a 0. The second word from memory must match the first word from tape, and so on. The 0 word may be inserted conveniently into the data stream through use of the data channel's data-chaining facility. If the first word from memory is not 0, a READ/COMPARE ERROR always occurs.

For other flags, modes, and timing considerations, see READ mode.

RD/CMP Across Record Boundaries (13) — Like READ ACROSS RECORD BOUNDARIES (12), but compares each word read with a word from core memory.

Write (4) — Data may be written in any of three densities (200 bpi, 556 bpi, or 800 bpi) on 7- or 9-channel transports, at 800 bpi in IBM-compatible format on 9-channel transports, or at any of three densities in core dump mode on 9-channel transports. The WC register in the data channel specifies the number of words to write. Either even or odd parity may be selected. When selecting even parity, care must be taken never to write a character of all 0s on tape, because such a character will produce a false EOR indication while reading. A WRITE command to a write-locked tape results in the ILLEGAL OP flag and no tape motion. To terminate a record, the data channel terminates CHANNEL BUSY. JOB DONE is set when the read-after-writing circuit reads and checks the longitudinal parity. The BAD TAPE flag could be set at this time.

Write With Extended EOR Gap (14) — Similar to WRITE (4) except that a 3 in. gap of blank tape (instead of 3/8 in.) is written prior to the start of the WRITE operation.

Write End-Of-File (5) — An end-of-file character and end-of-file gap are written on the tape. Parity is set automatically, and the data channel is not used for this operation. The END-OF-FILE and JOB DONE flags are raised when the function is completed. ILLEGAL OP is raised and no tape motion results if the tape is write-locked. BAD TAPE and PARITY ERROR can also be set, indicating miswriting.

Write Blank Tape (15) — Writes approximately 3 in. of blank tape and sets JOB DONE when completed.

Space Forward (6) — For this operation, the data channel uses its WC register to count the number of records to space. When the specified number of records are spaced, the data channel terminates operation. However, one record is spaced for a 0 WC. The TM10 stops spacing at an end-of-file, regardless of the WC and also at the first end-of-record following the EOT marker. JOB DONE is raised when the TM10 has finished spacing the last record.

The same density at which the tape was written must be selected. At lower density, the TM10B can miss an end-of-file mark. Parity is not relevant. CORE DUMP must be selected to allow 200 bpi or 556 bpi on 9-channel tape. Other relevant flags are BAD TAPE and EOF.

Space Forward To End-Of-File (16) — Spaces any number of records and stops only for END-OF-FILE or EOT. The data channel is not used for this operation. Otherwise, this function is similar to SPACE FORWARD (6).

Space Reverse (7) — Spaces one or more records in reverse. Control of the number of records spaced is the same as for SPACE FORWARD (6). Regardless of the number of records specified by the data channel, the TM10 stops a SPACE REVERSE operation at an EOF or at the BOT (beginning of tape, or loadpoint) marker. The EOT marker is ignored. ILLEGAL OP is raised if SPACE REVERSE is attempted and the tape is at the BOT at the start of the operation (no tape motion results). Otherwise, this function is similar to SPACE FORWARD (6).

Space Reverse To End-Of-File (17) — Spaces any number of records in reverse and stops only for EOF or BOT. The data channel is not used. Otherwise, this function is similar to SPACE REVERSE (7).

3.4.7 TM10 Command Timing

At an end-of-record, the TM10 raises the JOB DONE flag before stopping the tape. If the program supplies a new command to the same transport requiring the same direction of motion as the previous command, the tape never stops moving provided the program does not take too long. The exact duration of *too long* depends on the stopping characteristics of the particular transport involved. If the program is slow, or if the direction of motion is different for the new command, the tape is automatically stopped and the command is held up until the transport becomes idle. If the new command is for a different transport number, the TM10 retains the old transport number until the appropriate time for giving the stop signal. Thus, CONI MTS will return the former unit number until that unit is stopped, whereupon the unit number is automatically changed to the new one. The TM10 then waits for the newly selected unit to become idle before starting tape. If this waiting period is more than 1 second, the TRANSPORT HUNG flag is raised.

If a CONO MTC is given before the JOB DONE flag comes on, the command in progress is aborted.

CHAPTER 4
THEORY OF OPERATION

This chapter provides a complete description of the theory of operation of the TM10A and TM10B Magnetic Tape Control Units. General and summary information of the DF10 Data Channel is presented first, followed by a detailed logic description of the circuits common to both the TM10A and TM10B; where the TM10A and TM10B differ is also fully discussed. The logic drawings referenced in this discussion are contained in the TM10 Engineering Drawing Set. These logic drawings are referenced only by the last suffix. For example, logic drawing D-BS-TM10-0-CM1 is referenced as drawing CM1.

4.1 DF10 DATA CHANNEL DESCRIPTION

A complete description of the DF10 Data Channel is given in the *DF10 Data Channel Maintenance Manual.* However, in order to understand the operation of the TM10B, it is necessary to understand how the DF10 communicates with the TM10B. Therefore, a brief description of the DF10 is given below.

This description is relevant for the TM10B and not for the TM10A. The MTS DATAO instruction is issued to provide an initial control word address. The control word address is held by the TM10B until it gains access to the data channel. When the TM10B gains access to the data channel, it sends the initial control word address to the data channel, which stores this address in the control word address register. The data channel then fetches the control word normally consisting of WC (word count) and DA (data address). The WC and DA are stored in their respective data channel registers. The WC register specifies the 2's complement of the number of data words to transfer, and the DA specifies the core memory location minus 1. The DA is incremented by 1 prior to the first transfer. After a word transfer between core memory and the device communicating with the data channel, the WC is decremented and the DA is incremented. When the WC is reduced to 0, the number of words initially specified have been transferred. The control word address register is incremented and the next control word is fetched from core memory. If the control word contains all 0s, the end of communications is specified and the data channel terminates operation.

A number of devices can be connected to the data channel; however, the data channel communicates with only one at a time. To establish, maintain, and terminate communications, the following signals are exchanged between the device and the data channel.

Signal	Description
DATA BUS	This incorporates 36 bidirectional data pulse lines. These signals are 100-ns negative-going pulses swinging from ground to -3V.
CHANNEL PULSE	This 100-ns negative-going pulse is sent from the channel. It accompanies the data pulses when the channel is sending data to the device. It also signifies a readiness to receive data when the device is trying to send data to memory.

(continued on next page)

Signal	Description
DEVICE PULSE	The signal is similar in function to the channel pulse signal. It accompanies the data when the device is sending and signifies readiness to receive when data flow is toward the device.
CHANNEL START	This is a level (-3V for true) which is sent from the device to the channel. It starts the channel into operation when asserted.
SA WRITE	This signal controls the direction of data transfer. When true, it signifies the device is writing some medium (reading memory). The timing is the same as that for the CHANNEL START.
CHANNEL BUSY	This signal comes from the channel and is asserted (-3V) some time after CHANNEL START is asserted from the device. The device must not put anything on the bus until this signal is asserted. When this signal goes false after having been true, the channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must *all* be false for at least 400 ns prior to reassertion of CHANNEL START.
WRITE CONTROL WORD REQUEST	This negative 100-ns pulse from the device causes the channel to store the current contents of the data address register and the control word address register into memory location B + 1, where B (an even number) is the channel initial control word address. The contents of the control word address register go into bit positions 0—17, and the contents of the data address register into 18—35. Upon any channel termination, an automatic WRITE CONTROL WORD REQUEST is made.
WRITE CONTROL WORD COMPLETE	This pulse from the channel signals the completion of the operation requested above. This pulse does not occur on the automatic termination.
NO SUCH MEMORY	This pulse is sent from the channel as CHANNEL BUSY goes off and indicates that the memory addressed failed to respond.
CONTROL WORD PARITY ERROR	If a control word is fetched from the memory by the channel and this word has a parity error, CHANNEL BUSY is reset and this pulse is sent to the device from the channel.
DATA WORD PARITY ERROR	This pulse accompanies the data and the CHANNEL PULSE when a data word which was read from memory with a parity error is sent to the device.

The I/O devices attached to a data channel are arranged as shown in Figure 4-1 (only the pertinent signals are shown). In order for a device to gain access to the data channel, it must generate a CHANNEL START and receive a CHANNEL BUSY. If a device is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY. A device that is relaying CHANNEL START is prevented from generating its own CHANNEL START. A device that is busy with the data channel does not relay CHANNEL BUSY.

To further examine data channel communication, assume that devices 1 and 2 are not busy and device 3 initiates communication by asserting its CHANNEL START signal. CHANNEL START is applied to device 2 and because device 2 is not busy it relays the CHANNEL START. Similarly, device 1 relays CHANNEL START. The data channel acknowledges the CHANNEL START by asserting the CHANNEL BUSY. The data channel does not know which device requested access; it only knows that it received a CHANNEL START, and it responds by asserting CHANNEL BUSY. Furthermore, the data channel responds only to stimulus of the control signals by

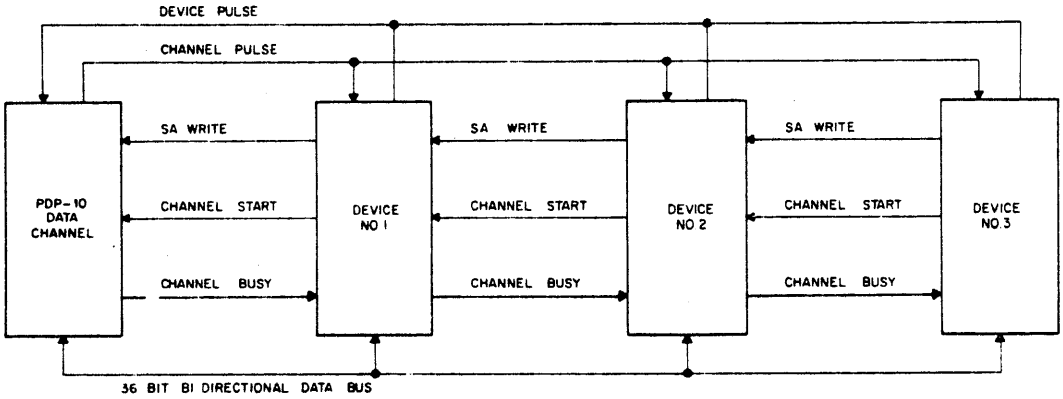

Figure 4-1 Data Channel Interface

transferring data to and from the data bus or starting or stopping operation. It is the responsibility of devices to determine which has access.

Because devices 1 and 2 are not busy, they relay the CHANNEL BUSY signal to device 3. Upon receipt of CHANNEL BUSY, device 3 has access to the data channel and can communicate via the data bus. A device requires two conditions to gain access to the data channel: the assertion of its own CHANNEL START and the receipt of CHANNEL BUSY.

To demonstrate this dual requirement, assume that device 2 is communicating with the data channel. It has asserted its CHANNEL START and received a CHANNEL BUSY. It does not relay CHANNEL BUSY to device 3. If now, device 3 attempts communications, it can assert at CHANNEL START because it is not relaying CHANNEL START. Device 2 is already generating a CHANNEL START; thus, it essentially ignores the CHANNEL START from device 3. The CHANNEL BUSY is not relayed to device 3; therefore, device 3 does not gain access to the data channel because of two requirements: assertion of CHANNEL START and receipt of CHANNEL BUSY. Device 3 now must wait until device 2 has finished with the data channel.

Either device 2 or the data channel can terminate operation. The data channel terminates operation by removing CHANNEL BUSY, and the device responds by negating CHANNEL START. After termination, device 3 is free to communicate; however, the data channel requires at least 400 ns between the negation of CHANNEL BUSY and CHANNEL START and the assertion CHANNEL START. In this case, this requirement is imposed on device 2 (or any other device that is generating or relaying CHANNEL START and receiving the on-to-off transition of CHANNEL BUSY). When termination occurs, all devices must inhibit the generation or relaying of CHANNEL START for 400 ns.

4.2 NRZI RECORDING

The actual technique of recording on magnetic tape is called the non-return-to-zero, inverted (NRZI) method. In this recording method, a reversal of the direction of magnetization in a channel represents a 1 bit, a lack of reversal represents a 0 bit. Writing is achieved by using a flip-flop to control the direction of magnetizing current in each channel write head; the group of flip-flops is called the write buffer. By applying the 1s lines to the complement inputs of the write-buffer, each channel reverses its flux only when a 1 bit is to be written for a character. Further, the write buffer accumulates the LPCC (longitudinal parity check character) to be written as an EOR character. When the write buffer is cleared at EOR time, the LPCC character is thus written automatically.

The NRZI recording method provides self-clocking during reading because a transition (or flux reversal) in any channel, signifying a 1 bit for that character in that channel, is used to strobe or sense all seven channels for that character. Ideally, all transitions for a single character would be sensed simultaneously by the 7-channel read head.

In fact, tape skew makes these transitions (if more than one in a single character) nonsimultaneous on reading. There may be a difference in alignment of the read head with respect to the write head recording the tape (static skew). The tape alignment to the read head is apt to vary during tape travel (dynamic skew). To accommodate these timing variations between channels due to skewing, the first detected transition for a character initiates a delay before the character is strobed. This delay is selected to accept the maximum skewing produced at the linear tape transport speed with the designated tape density.

A simplified block diagram of the tape system write and read paths for a single channel is presented in Figure 4-2. The write path (WP) is shown at the top of the figure. The WRITE flip-flop in the write amplifier is complemented at each WP pulse if the data buffer for that particular character contains a 1. When gated by a WRITE ENABLE signal, the write amplifier drives one or the other of the two opposing directions at the write head. If the WRITE ENABLE level is not present, no current flows through the coil. Whenever a 1 is to be written on a tape, the WRITE flip-flop is complemented by the WP pulse. The transition of the WRITE flip-flop terminates the current in one direction and starts it in the other direction, changing the direction of the tape magnetization, and thus writing a 1 on tape. As long as the WRITE flip-flop remains in the same state, the current flows in the same direction, and 0s are written on the tape. The tape is then magnetized in the same direction over a series of character spaces.

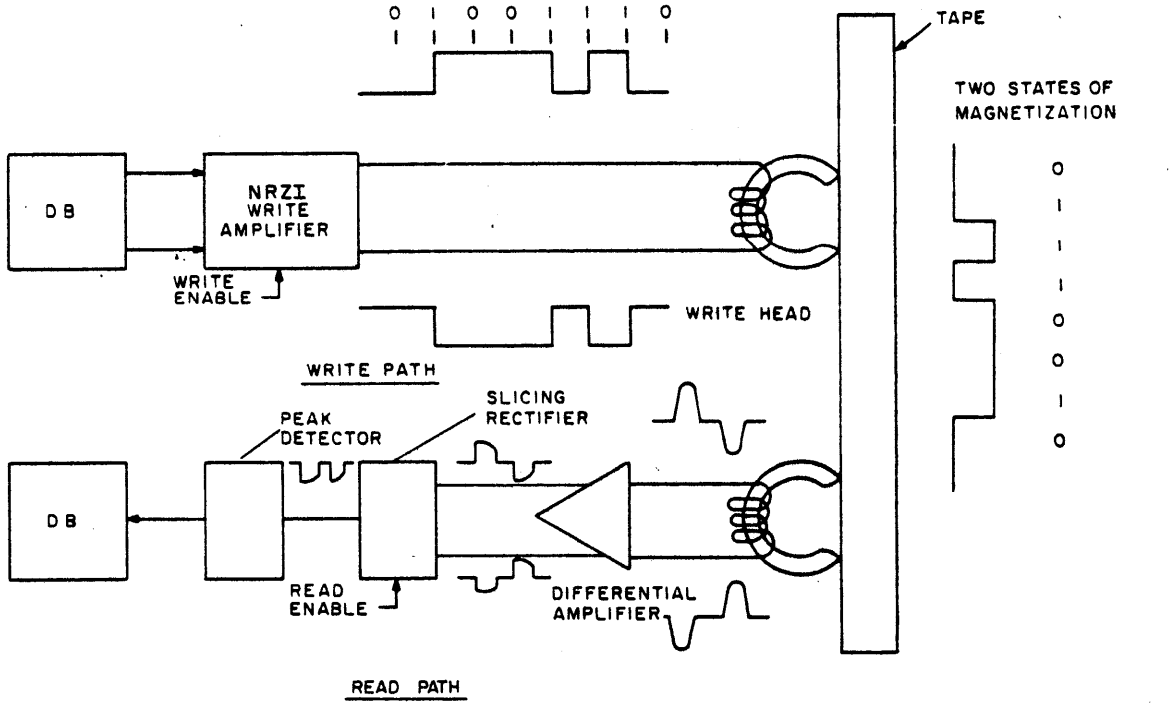

Figure 4-2 Tape Write and Read Signal Flow

The read path is shown at the bottom of Figure 4-2. The tape reaches the read heads shortly after traversing the write head. As long as the direction of tape magnetization remains constant, no current flows through the read head coil. Each change in the direction of tape magnetization induces a current in the read head. The read current produced by two consecutive tape 1s is shown in the waveform near the read head. These signals are applied to a differential read amplifier to provide amplification for different mode signals, but only fractional amplification for common mode signals. The output of the read amplifier is then sent through a slicing rectifier. The rectifier output pulse is of a single polarity although input pulses are of both polarities from the read amplifier. No slice output is generated, however, unless the input exceeds a designated voltage threshold level. A low-level noise input cannot generate an output pulse. Next, the slicing rectifier output is applied to a peak detector. The peak detector produces a logic pulse output at the peak of the input pulse.

4.3 SYSTEM DESCRIPTION

4.3.1 TM10A

A simplified block diagram of the TM10A is shown in Figure 4-3. Assuming a write operation, the program issues a CONO 340 I/O instruction. It is decoded by the I/O bus control circuits to generate the MTC CONO pulses that load the specified parameters (i.e., write, parity mode, density, etc.) into the command register. The appropriate motion commands are transferred to the selected tape transport. A short delay is implemented to provide the tape inter-record gap. During this delay, the DATA REQUEST signal enables the data interrupt channel to generate an interrupt. The executive program responds to the interrupt by issuing a DATAO 340, which loads the hold register (HR). The program cannot respond quickly enough to load the buffer register (BR) directly before recording (or reading) starts. Therefore, the HR register is provided to buffer the data between the PDP-10 and the BR register. Whenever the BR register is empty, the TM10A transfers the data word in the HR register to the BR register and generates a DATA REQUEST to obtain the next word to be written.

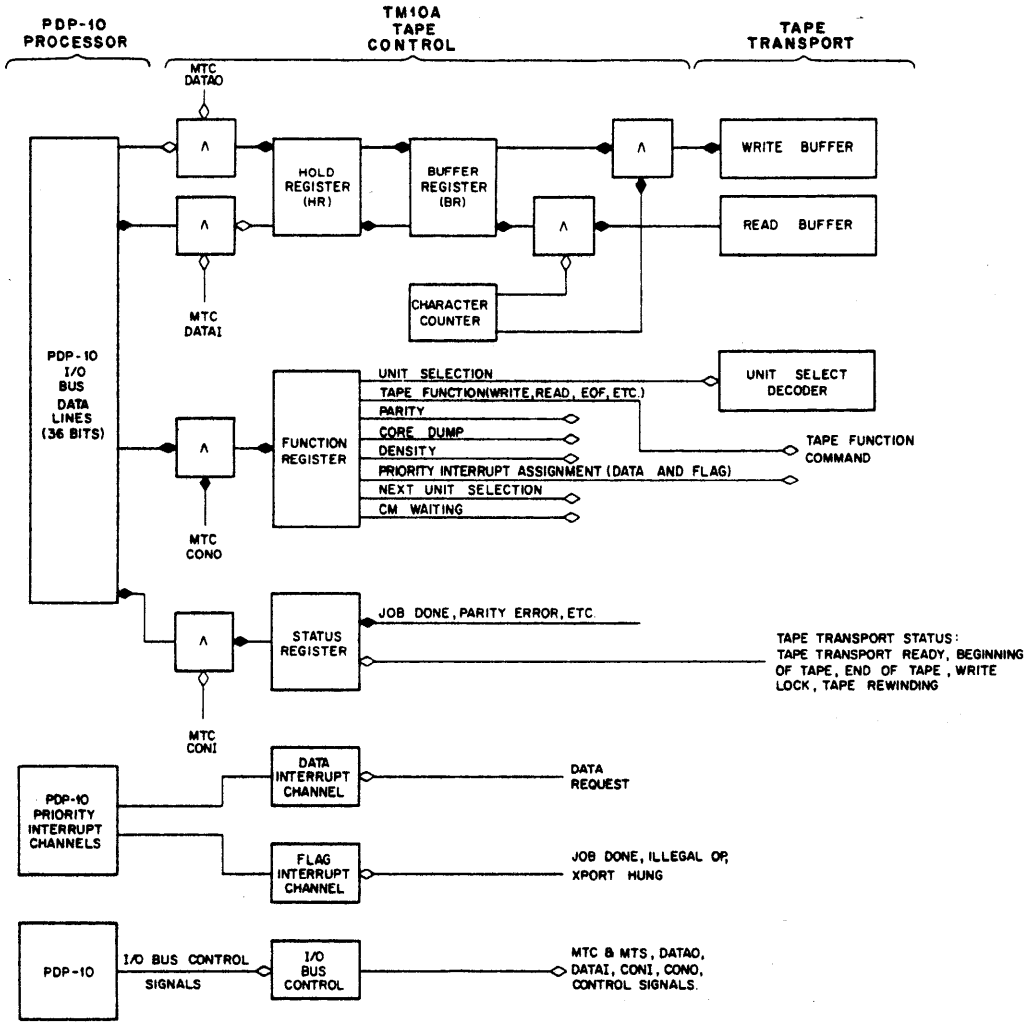

Figure 4-3 TM10A Tape Control Block Diagram

After the inter-record gap delay and BR register loading, the write operation begins. Assuming 7-track operation, the BR register 36-bit word must be divided into six 6-bit characters for writing on tape. The character counter sequences the 6-bit character from the data buffer. As a 6-bit character is written from the high-order bits of the BR register, the character counter is incremented to sequence the next low-order 6-bit character. After the six

6-bit characters from the data buffer are written, the DATA REQUEST is set to initiate another word transfer to the BR register via the HR register.

Operation continues in this manner until the program determines that the desired number of words have been written, at which time the TM10A tape control is notified via a CONO MTS, 1 instruction. The LPCC character is written, and write operation terminates. The tape continues in the forward motion until the read circuits detect the end-of-record passing under the read head. At this point the deceleration delay is initiated, and the JOB DONE flag is set.

For the read operation, the initial programming sequence is similar to the one for the write operation. As 6-bit characters are read from tape, they are sequenced into the buffer by the character counter. When the BR register is full, the data is transferred to the HR register and the DATA REQUEST initiates a programmed transfer of the data into core memory. Operation continues until the read circuits detect the end-of-record.

As shown in Figure 4-3, the tape control status can be transferred to the central processor by using the appropriately coded CONI instructions. Moreover, the JOB DONE flag and the error bits generate an interrupt separate from the DATA REQUEST interrupt.

4.3.2 TM10B

A simplified block diagram of the TM10B is shown in Figure 4-4. Assuming a write operation, the program issues a CONO 340 and a DATAO 344 instruction. The DATAO 344 is decoded by the I/O bus control circuits to generate MTS DATAO, which loads the control word initial address register. The content of this register will be subsequently transferred to the DF10. The CONO 340 instruction is decoded to generate the MTC CONO pulses that load the specified parameters (write, read, parity mode, density, etc.) into the function register.

Before writing can begin, the TM10B must gain access to the data channel. Therefore, it makes a request by generating CHANNEL START. If data channel is not busy, it responds with CHANNEL BUSY. The TM10B sends the initial control word address to the data channel. The channel control circuits then generate the OK TO GO signal.

A short delay is implemented to provide the tape inter-record gap delay. The DEVICE PULSE requests the first 36-bit data word to be recorded. The data channel responds by loading the BR register.

After the inter-record gap delay and BR register loading, the write operation begins. Assuming 7-track operation, the BR register 36-bit word must be divided into six 6-bit characters for writing on tape. The character counter sequences the 6-bit character from the data buffer. As a 6-bit character is written from the high-order bits of the data buffer, the character counter is incremented to sequence the next low-order 6-bit character. After the six 6-bit characters from the data buffer are written, the DEVICE PULSE initiates another word transfer to the BR register via the data channel.

Operation continues in this manner until the data channel fetches a 0 control word, signifying that the required data has been recorded. The data channel thus removes the CHANNEL BUSY signal to terminate operation. The LPCC character is written and write operation terminates. The tape continues in the forward motion until the read circuits detect the end-of-record passing under the read head. At this point, the deceleration delay is initiated, and the JOB DONE flag is set.

For the read operation, the initial programming sequence is similar to write. As 6-bit characters are read from tape, they are sequenced into the BR register by the character counter. When the BR register is full, the DEVICE PULSE initiates a data channel transfer of the BR register word into core memory. Operation continues until the read circuits detect the end-of-record.

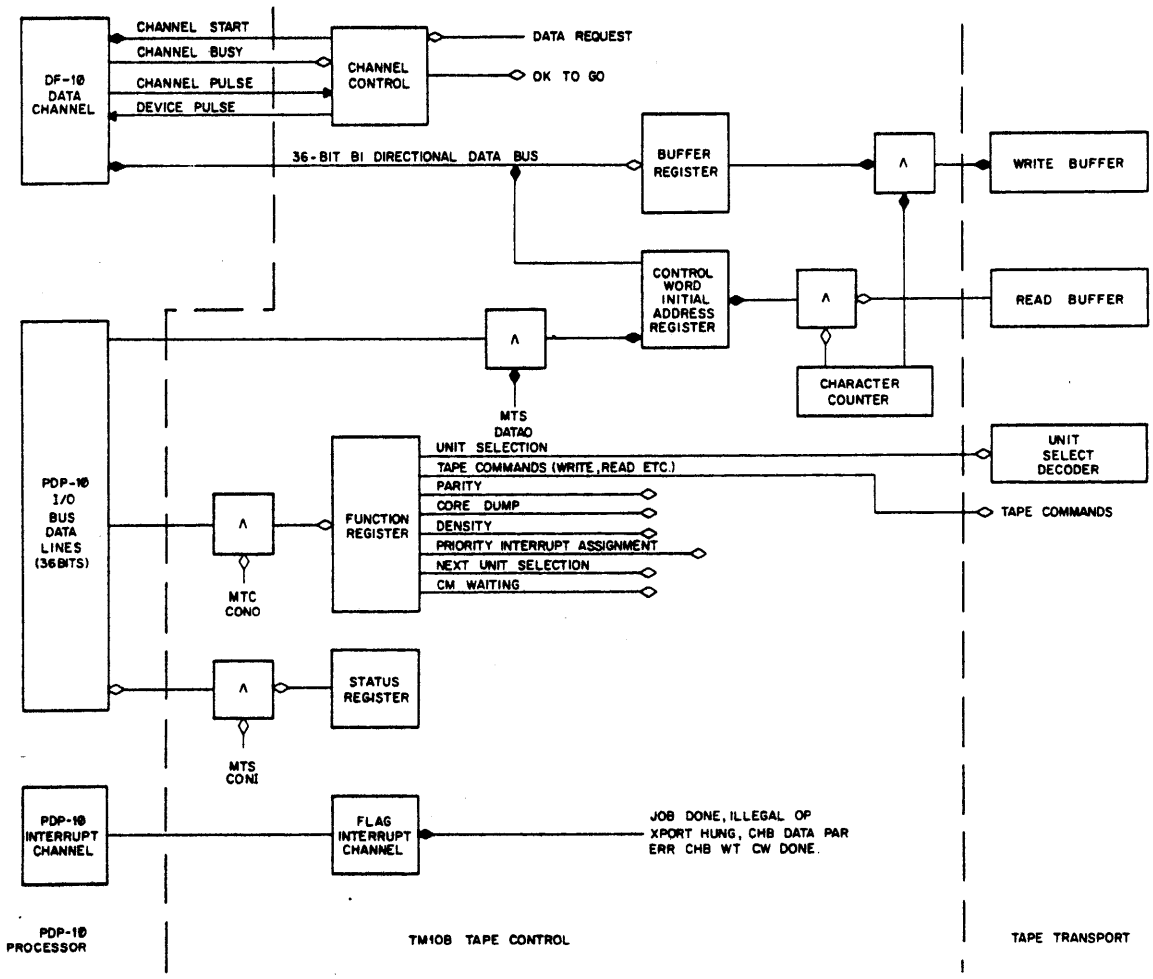

Figure 4-4 TM10B Tape Control Block Diagram

4.4 TM10A INITIAL OPERATION

The MTC CONO instruction loads the parameters (tape function, density mode, unit number, priority interrupt channel numbers, etc.) into the command register as shown on drawings CM1 and CM2. The tape function register (CM FCN0—FCN3) is decoded to specify the operation. Since this is initial operation, the content of CM NEXT UNIT (0—2) register (drawing CM2) is transferred to CM UNIT (0—2) register (drawing CM1). The T GO signal is false at this time. The CM UNIT register (via drawing TB) selects the desired tape drive.

The MTC CONO SET pulse also sets the CM WAITING flip-flop (drawing CM2). After a 1 μs delay, the CM UNIT OK flip-flop is set. If the selected tape unit is ready (signal TB TUR is true), the CM LEGAL TEST pulse is generated. This pulse tests the legal conditions (drawing ST). If any of the following illegal conditions are true, the ST ILLEGAL OP flip-flop is set.

a. Writing on a protected tape (CM WRITING and TB WL are true).

b. Space reverse and tape at beginning of tape (CM SP REV and TB BOT true).

c. Nine-channel operation and not 800 bpi density; and not core dump mode.

If the ST ILLEGAL OP flip-flop gets set, an interrupt is generated (drawing CM2), and the operation terminates. Assuming no illegal operation, the CM LEGAL TEST DONE signal generates CC OK TO GO, which fires the CM MT GO pulse. (Note the jumper between H15 pins U and V, which is present only on TM10A). The CM MT GO sets the T GO flip-flop (drawing T2) to start the operation as described in Paragraph 4.6. The CM NO-OP DONE pulse (if present) sets the ST JOB DONE flip-flop.

4.5 TM10B INITIAL OPERATION

Operation of the TM10B starts when the PDP-10 processor issues an MTS DATAO instruction to transfer the data channel initial control word address and an MTC CONO instruction to set up initial parameters. The MTS DATAO instruction loads the IA27—IA34 (initial address, drawing CC) register with the control word initial address. This will be subsequently transferred to the data channel.

The MTC CONO instruction loads the parameters (tape function, density mode, unit number, priority interrupt channel number, etc.) into the command register as shown on drawing CM1 and CM2. The tape function register (CM FCN0—FCN3) is decoded to specify the operation. Since this is initial operation, the CM NEXT UNIT 0—2 register (drawing CM2) is transferred to CM UNIT 0—2 register (drawing CM1). The T GO signal is false at this time. The CM UNIT register (via drawing TB) selects the desired tape drive.

The MTC CONO SET pulse also sets the CM WAITING flip-flop (drawing CM2). After a 1 μs delay, the CM UNIT OK flip-flop is set. If the selected tape unit is ready (signal TB TUR is true), the CM LEGAL TEST pulse is generated. This pulse tests the legal conditions (drawing ST). If any of the following illegal conditions are true, the ST ILLEGAL OP flip-flop is set.

a. Writing on a protected tape (WRITING and TB WL are true).

b. A space reverse specified, and tape is at beginning of tape (CM SP REV and TB BOT true).

c. Nine-channel operation and not 800 bpi density; and not core dump mode.

If the ILLEGAL OP flip-flop gets set, an interrupt is generated (drawing CM1), and the operation terminates. Assuming no illegal operation, the CM LEGAL TEST DONE signal (drawing CM2) sets the CC CHN SYNC (drawing CC) to request access to the data channel. Note on drawing CM2 that the W990 module is removed for TM10B operation. Therefore, the logic must wait for the CC OK TO GO signal, which signifies that the tape control has access to the data channel for those operations that require the data channel. For operations not requiring the data channel, the CC NEED CHANNEL signal (drawing CC) immediately generates CC OK TO GO.

With CC CHN SYNC set, the TM10B requests access to the data channel. The TM10B must now wait until it gains access to the data channel. If the data channel is busy with another device, the TM10B must wait until the data channel has completed its operation. For the ensuing description of channel control, it is assumed that the data channel is initially busy with another device.

The CC NEED CHANNEL (drawing CC) is true as previously described to request access to the data channel. The CC ACTIVE flip-flop, which signifies that the TM10 control has access to the data channel, is reset because it is assumed that the data channel is busy with another device. The CHB CHANNEL START IN signal (drawing CHB) is asserted, and it asserts CHB CHANNEL START OUT. (Here it is assumed that the TM10B is between another device and the data channel.) Similarly, CHB CHANNEL BUSY IN is relayed as CHB CHANNEL BUSY OUT, and CHB SA WRITE IN is relayed as CHB SA WRITE OUT.

The normal termination point of a data transfer is when the data channel fetches a 0 control word. It then terminates operation by removing the CHANNEL BUSY signal. The device that is busy recognizes the removal of CHANNEL BUSY as the key to stop operation and thus inhibits its CHANNEL START out. On the other hand, the device can terminate the operation for reasons such as parity errors, etc., by removing its CHANNEL START.

The data channel responds by inhibiting CHANNEL BUSY. Regardless of which terminates, it requires the negation of both CHANNEL START IN and CHANNEL BUSY IN before the TM10B gains access to the data channel. When CHB CHANNEL BUSY IN, CC ACTIVE (0), and CHB CHANNEL START are true, the CC TERMINATE pulse is generated to set the CC INHIB (inhibit) flip-flop. Two hundred and fifty nanoseconds later CC TERMINATE DY clears the CC CHANNEL STARTED, which in turn sets the CC ACTIVE flip-flop. Note that INHIB prevents ACTIVE from generating a CHANNEL START at this point. After another 250 ns, the CC RESET pulse is generated and resets the INHIB flip-flop. With CC INHIB reset and CC GRAB CHANNEL true, ACTIVE now generates a CHANNEL START, which tells the data channel that the TM10B is ready to start operation, assuming no illegal status (ST ILLEGAL OP (0) true). CC GRAB CHANNEL is true due to CC CHN SYNC (1) being true. CHANNEL START also prevents any other device on the bus (closer to the data channel) from gaining access to the data channel in the same manner that the CHANNEL STARTED flip-flop inhibits the TM10B (note that CHB CHANNEL START OUT holds CC CHANNEL STARTED in the set state).

The data channel responds to CHANNEL START by asserting CHANNEL BUSY. The receipt of CHANNEL BUSY by the TM10B is the acknowledgement that is has access to the data channel. The TM10B receives CHANNEL BUSY IN (CHB CHN BUSY IN, drawing CHB) but does not relay it. The CHB CHN BUSY IN signal, ANDed with CC ACTIVE, generates CC CHN SEIZED.

The CC CHAN SEIZED generates the CC DATA TO CHN pulses, which transfer the content of BR to the channel bus (drawings CHND 1 and 2). This transfer sends the initial address data contained in BR 27–BR 34 to the data channel. CC CHAN SEIZED now generates CC MT START and CC OK TO GO. The CC OK TO GO signal (drawing CM2) now generates CM MT GO, which sets the T GO flip-flop to start the operation as described in Paragraphs 4.4 and 4.5. CM MT GO also generates the initial device pulse (CHB DEV PLS, drawing CHB) to inform the data channel that the tape control is ready to transfer data. Because the tape control has access to the data channel, the CM MT GO pulse clears CC CHN SYNC and CC WAIT DEL.

Operation now continues as explained in Paragraph 4.6 with the inter-record delay, after which data is read from or recorded onto the tape. The subsequent data transfer between tape control and data channel is described in Paragraph 4.13.

4.6 INTER-RECORD GAP DELAY

According to tape format, between each record there is an inter-record gap. Assuming that the tape is stopped, before reading or writing the tape must attain operating speed within the inter-record gap. To provide the inter-record gap, the tape control timing circuits incorporate a timing delay which is explained as follows: the T GO flip-flop (drawing T2) is set as previously described; the T GO signal performs the following functions.

a. Sets the T ACCEL (acceleration delay) flip-flop (drawing T1).

b. Generates the SET TAPE FCN pulse (drawing T2), which shuts the transport status off the bus and sends to the transport, the command direction, forward reverse, rewind, and write (drawing TB). The transport that receives the command sets the function into the tape transport register.

c. Generates the TB MOVE signal (drawing TB) to move the tape in the specified direction.

The T ACCEL flip-flop being set generates T ENABLE MUC (drawing T1), which enables the motion up-counter (MUC on drawing MT). For the write command, the T ACCEL signal sets the BC DATA REQ flip-flop (drawing BC2) to obtain the first word to be recorded to the data buffer. T ENABLE MUC (drawing MT) now generates MT COUNT pulses at the 800 bpi clock frequency of the selected tape transport. The MUC bits are decoded so that the thirtieth MUC pulse sets the MT DLY SYNC flip-flop (MT DLY XFERRED will be 0 at this time). MT DLY SYNC synchronizes the motion transfer sequence to enable the motion-delay character from the selected tape transport to appear on the read buffer lines. The binary number, representing motion delay duration, represents the start-stop characteristics and operating speed of the attached tape transport. The next MT COUNT pulse

generates the MT STROBE DELAY pulse, which strobes the contents of the read buffer lines into the MT register (drawing MT); the MT register is the timing register that provides the necessary acceleration or deceleration delay. MT STROBE DELAY then sets the MT DLY XFERRED flip-flop (indicating transfer complete) and clears the DLY SYNC flip-flop. The next MT COUNT pulse generates a DOWN COUNT pulse and begins to count down the MT register. The MT COUNT pulses continue producing DOWN COUNT pulses on every thirty-second MT COUNT pulse. Because the MT DLY XFERRED flip-flop is set thereafter, the thirtieth and thirty-first pulse will not reinitialize the MT register. When the MT register has counted down to a 1, the next DOWN COUNT pulse strobes the MT register to 0 and produces the MT IRD OVER (inter-record delay over) pulse. The IRD OVER pulse clears the T DEACCEL and T ACCEL flip-flops, thus ending the acceleration or deceleration delay. It should be noted that the delay sequence just described is used for deceleration of the tape following a tape spacing function as well as the acceleration of the tape before a tape spacing function.

The MT IRD OVER pulse, enabled by the T ACCEL signal, generates the T BEGIN OP pulse (drawing T1), which initiates the write and write end-of-file operations. If the rewind command is selected, the T BEGIN OP pulse clears the T GO flip-flop, which frees the tape control for a new command to a different tape transport while the previously selected tape transport rewinds.

4.7 WRITE

The write operation is initiated by the T BEGIN OP pulse, which sets the T SYNC WRITE flip-flop (drawing T1). The T CLOCK, which is the clock pulse for the selected density mode, clocks the write operation. The WD CLOCK DEL (drawing WD2), which is a delayed T CLOCK, is enabled to set WRITE ENABLE (drawing T1). The WRITE ENABLE signal then enables the T CLOCK pulses to generate T WP (write pulses, drawing T2). The WD CLOCK DEL pulses increment the character counter (BCC0–BCC2) in order to disassemble the 36-bit word in the data buffer into the appropriate 6-bit (7-track operation) or 8-bit (9-track operation) characters that are to be recorded. In the 7-track operation, there are six characters per word. In 9-track operation, there are four characters per word. (In 9-track core dump operation, there are five characters per word.)

For 7-track operation, the character count circuits sequentially generate BC 1ST/7, BC 2ND/7, BC 3RD/7, ... BC 6TH/7 signals (drawing BC1), which sequentially disassemble the 36-bit data buffer word into 6-bit characters and apply them to the bus of the tape transport. In a similar manner, the 9-track decoding signals are formed. Drawing WD1 shows the decoding of the 36-bit buffer register word for both 7-track and 9-track operation.

The T WP pulse also produces T RECORD DATA pulses (drawing T2) that are sent to the tape transport to record the characters on the tape. For 9-track operation, the write pulse (T WP) exclusive ORs the characters into the CRC register (drawing WD2) one character at a time. The CRC register then performs the necessary manipulation of the data to conform to 9-track format. The characters are also decoded in the write parity circuit (drawing WD2), and the parity bit pertaining to that character is sent to the tape transport to be recorded.

When a complete word has been written on tape, the BC ENB DATA REQ signal (drawing BC1) is generated. This signal enables the WD DEL pulse to generate BC WRITING SET DF (drawing BC1), which in turn sets the T DATA FLAG flip-flop (drawing T2) to request the next 36-bit word to be recorded. The next word to be recorded is transferred into the BR register. The manner in which data transfers between core memory and buffer register occur is described in Paragraph 4.13.

Operation continues until the desired number of words are transferred as indicated by BC LAST WORD signal. (The BC LAST WORD signal generation is described in later paragraphs.) When the last character of the last word has been written, BC LAST WORD enables the generation of BC LAST COUNT and BC LAST BYTE. BC LAST BYTE enables the WD DEL to clear the WRITE ENABLE (drawing T1) flip-flop and T WP to set the WRITE EOR flip-flop. Since it is the end-of-record, a 3-character space must be left on tape and the LPCC character must be written. This is accomplished as follows.

The WRITE EOR (1) signal enables T CLOCK pulses to count up the EOR1 and EOR2 counter (drawing T1) to produce the required 3-character space signified by the 4 CHAR pulse. For the 7-track system, the 4 CHAR pulse generates the T WRITE LPCC pulse, which is sent to the tape transport to write the longitudinal parity check character.

For a 9-track system, the CRC character is written following the first 3-character space. The EOR1 and EOR2 counter recycles for a second 3-character space count and then the LPCC is written.

Tape motion continues at full speed until the read circuits detect the end-of-record passing under the read head in the tape transport. When the read circuits detect the end-of-record, the T RECORD OVER pulse sets T DEACCEL to initiate the deceleration delay (refer to the READ discussion for generation of T RECORD OVER pulse). At the start of the deceleration delay, MT STROBE DELAY ANDed with T STOP sets the ST JOB DONE flip-flop (drawing ST). If the interrupt is enabled, JOB DONE flag generates a flag interrupt (drawing CM2), signifying that the record has been completed. Subsequently, at the end of the deceleration delay, the MT IRD OVER pulse is produced and clears T DEACCEL. The T STOP signal enables MT IRD OVER to generate CM CLR GO (drawing CM2), which clears the T GO flip-flop, terminates the MOVE signal, and stops the tape thus completing the write operation.

4.8 CONTINUED OPERATION

If the CM CONTINUE flip-flop (drawing CM2) is set when CM CLR GO occurs, then CM LEGAL TEST is generated to start operation again for the function specified. The CM CONTINUE flip-flop is set if the new function command does not require a change of tape direction and a different unit is not selected (~CM STOP TAPE is true). If a different tape unit has been selected for operation, then ~T GO and CM WAITING set CM UNIT OK after a 1 μs delay to allow the transport bus to settle down.

For the TM10B, the data channel is released as soon as it fetches a 0 control word. The tape, of course, continues through the deceleration delay. If the program wishes to continue operation with the same unit, it issues the appropriately coded MTC CONO instruction. The MTC CONO SET pulse sets CC WAIT DEL. If the new function does not require a reversal of tape direction, then CC GRAB CHANNEL is generated to request access to the data channel for the ensuing function. In this manner, the data channel request is in process while waiting for the deceleration delay to terminate. Signals CM UNIT OK and TB TUR (tape unit ready) generate CM LEGAL TEST to start operation.

4.9 WRITE END-OF-FILE MARK

After the inter-record delay, the T BEGIN OP pulse sets the T SYNC EOF flip-flop (drawing T1), which synchronizes the tape operation to write the 17_8 EOF character on 7-channel tape or 023_8 on 9-channel tape. SYNC EOF enables the next T CLOCK pulse to set the WRITE EOR flip-flop. The transition of WRITE EOR, enabled by CM WR EOF, generates the T RECORD DATA pulse (drawing T2), which is sent to the tape transport to write the EOF character on tape. WRITE EOR then enables the 4-character sequence prior to LPCC character; WRITE EOR enables the T CLOCK pulses (drawing T1) to increment EOR1 and EOR2 to a 4-count and generate the T 4TH CHAR pulse. For a 7-track system, T 4TH CHAR generates T WRITE LPCC (drawing T1), which writes the LPCC character. For a 9-track system, the first T 4TH CHAR pulse writes a 0 CRC character; a second T 4TH CHAR pulse is generated to write the LPCC. Operation terminates when the read circuits detect missing data and begin the deceleration of the tape.

4.10 READ

After the initial programming sequence sets up for reading and the inter-record delay sequence is complete, operation begins when the read circuits in the tape transport detect data. For each character detected, the tape transport

sends to the tape control a TB RD SKEW OVER pulse (drawing TB). TB RD SKEW OVER pulse produces the T READ STROBE (drawing T1); and ERF (0) enables the T RD STROBE to generate the T READ pulse. The character counter (BCC0—BCC2, drawing BC1) is 0 at this time; therefore, BC 1ST/7 signal enables the T READ pulse to strobe the 6-bit character from the tape transport into the BR0—BR6 bits of the BR register (drawing BR1). The T READ pulse also increments the character counter. Parity is checked by the T READ STROBE (drawing RD) by setting the RD LATERAL PAR ERR flip-flop when an error occurs. Note that T READY FOR DATA (drawing T1) enables the parity detection circuit only at the appropriate time. The READ STROBE also accumulates the LPCC character (drawing RD) by complementing the LPCC register for those bits that are 1. Operation continues in this manner until the BR register is full. The character count now generates BC 6TH/7 (assuming 7-track operations), which initiates a data transfer from the BR register to the processor (drawing BC1). The BC 6TH/7 signal,enabled by ~BC LAST WORD,generates BC ENB DATA REQ which generates BC READING SET DF, which in turn sets the DATA FLAG flip-flop (drawing T2). As explained later, the DATA FLAG enables the transfer of data to the processor.

Operation continues in this manner until the read circuits detect missing data, thus signifying end-of-record. It should be noted that if the processor specifies a record length less than the record length read, only the number of words specified by the processor are transferred to memory. If the length specified by the processor is greater than the record length read, the entire record, of course, is transferred into memory. In any case, the detection of end-of-record by read circuits is the determining factor for stopping operation. This is accomplished as follows.

The first T READ STROBE, which signifies that the first character has been read from tape, is enabled by CM MOTION FWD and T DEACCEL (0) to set the DATA PRESENT flip-flop (drawing T1). DATA PRESENT then permits the T CLOCK pulse to toggle the EOR 3 flip-flop. As long as data is present, the T READ STROBE (B) clears EOR3 before EOR4 can be set. When data is missing, the READ STROBE does not occur and EOR4 gets set. The next T CLOCK pulse sets the SYNC REC OVER flip-flop, which enables the WD CLOCK DEL to generate T RECORD OVER. T RECORD OVER sets T DEACCEL to initiate the deceleration delay and thus terminate operation. The LPCC register (drawing RD) should be 0 at JOB DONE time; if not, ~RD LPCC = 0 (drawing ST) generates a ST PAR ERR (parity error).

4.11 READ/COMPARE

In the read/compare operation (CM RD/CMP, drawing CM1), a complete 36-bit word is read from tape and assembled into the BR register. After the word is assembled, the data transfer is initiated to obtain the word from processor memory for comparison. The word from memory is exclusive ORed into the BR register. Consequently, the data buffer should contain all 0s (BC BR = 0, drawing BC2); if not, the ST R/C ERROR (read/compare error, drawing ST) is set.

Operationally, the read/compare mode is similar to the read mode with the exceptions that follow. In the read/compare mode of operation, the data transfer cycle is initiated (via READING SET DF, drawing BC1) to obtain a word from memory to compare to the BR register. During the word transfer, the CM WRITE OR RD/CMP signal permits the BC HR TO BR XOR pulses (drawing BC2) to exclusive OR the word from memory into the BR register (drawing BR1 and BR2). (The discussion on Data Transfer explains more explicitly how the data transfer to the BR register is accomplished.) The BR register is then decoded to determine if it contains all 0s. The read/compare error prevents any data transfer cycles. The ST R/C ERROR signal generates T STOP CONDITION (drawing T2). T STOP CONDITION prevents (via BC LAST WORD, drawing BC1) any further data requests. Operation continues until the read circuits detect the end-of-record. At that time, the program may examine read/compare status and if a read/compare error is found, the program can further examine its internal structure to determine the memory location that was in error.

4.12 DENSITY MODES

Three different tape densities are available: 800, 556, and 200 bpi. Bits CM DENS0 and DENS1 of the command circuits (drawing CM1) select the densities. The different recording densities are effected by changing the clock pulse frequency. For 800 bpi operation, the 800 bpi clock pulses from the tape transport are enabled by CM 800 to produce the T CLOCK pulse (drawing T1); for 556 bpi operation, the 556 bpi CLOCK pulses from the tape transport are enabled by CM 556 to produce T CLOCK pulses. For 200 bpi operation, the 800 bpi clock is counted-down by flip-flops TA and TB producing T ENABLE 200 every fourth count to enable the 800 bpi clock to produce T CLOCK pulses.

4.13 DATA TRANSFER

4.13.1 TM10A

There are two flip-flops, BC DATA SYNC and BC DATA REQ (drawing BC2), that control the data transfer operation. BC DATA REQ flip-flop requests data (during write or read/compare) from the processor and during read requests that the processor take the data that has been read from tape. When set, BC DATA REQ enables the data priority interrupt to the computer. Through the interrupt and sense circuits, the processor is made cognizant of the request.

During write, BC DATA SYNC, when set, specifies that the HR (hold register) is loaded and ready to load the BR (buffer) register. It waits for T DATA FLAG (1) to specify that the BR register is ready for the next data word. Similarly, during read, BC DATA SYNC specifies that the HR register is ready to receive data from the BR register.

During the write mode, the BR register must be loaded and ready to go as soon as the inter-record delay is complete. To accomplish this, T ACCEL (1) (which occurs at the beginning of inter-record delay) generates BC WRITING SET DF (drawing BC1) and sets BC DATA REQ (drawing BC2). BC WRITING SET DF sets the T DATA FLAG flip-flop (drawing T2). Note that the T SET DF pulse, which sets T DATA FLAG, generates BC BR CLR (drawing BC1) to clear the BR register. The BC DATA REQ signal enables the DATA priority interrupt channel (drawing CM2).

The processor responds (i.e., the executive program responds) to the interrupt by putting the 36-bit word onto the I/O bus and generating the MTC DATAO instruction. The MTC DATAO CLR pulse clears the HR register (drawing HR), and the MTC DATAO SET pulse strobes the data into the HR. The MTC DATAO CLR pulse also clears BC DATA REQ. The MTC DATAO SET pulse also sets BC DATA SYNC. With T DATA FLAG (1) true, the BC BUFFERS READY signal is generated and clears BC DATA SYNC. It further generates BC HR TO BR XOR, which, in turn, generates CHND 00 through CHND 35 (drawing CHND 3). The CHND pulse then exclusive-ORs the HR register into the BR register (drawing BR1). For write mode, the BR register was previously cleared, therefore, the exclusive-OR function transfers the content of HR into BR. However, for the read/compare operation, the BR register contains the assembled 36-bit word when the exclusive-OR function occurs, thus effecting the read/compare function. Subsequently, BC BUF RDY DEL is generated, which sets BC DATA REQ. The data interrupt is again generated to load the HR.

The BR register is now loaded (assuming write mode), and subsequently the HR register will be loaded from the processor. As soon as the inter-record delay is complete, writing begins. After the first 36-bit word has been written, the T DATA FLAG flip-flop is set which, as explained above, transfers the content of the HR into the BR and subsequently (via BC BUF RDY DEL) sets the BC DATA REQ flip-flop. Operation continues in this manner until the desired number of words have been written as determined by the executive program. When this occurs, the executive program issues an MTS CONO instruction with bit 35 set. This clears the BC DATA XFER ACT (data transfer active) flip-flop, which was initially set by the CM MT GO pulse (drawing BC1). During a write operation, BC LAST WORD is not asserted until BC DATA SYNC is cleared because, until this is so, the HR

contains another data word to be written on the tape that has not yet been transferred to the BR. The BC LAST WORD signal is generated and, as explained for the write operation, as soon as the last character of the BR register has been recorded, BC LAST BYTE prepares the circuits to write the LPCC. Since BC DATA XFER ACT is no longer set, BC BUF RDY DEL can no longer set the BC DATA REQ flip-flop. The T DEACCEL (1) and BC LAST WORD (drawing T1) generate T STOP. The ensuing MT STROBE DELAY pulse is enabled by T STOP to set the JOB DONE flip-flop (drawing ST).

For the read operation, the BC DATA SYNC is initially set by CM READ and T ACCEL. When the first word read from the tape has been assembled in the BR, the T DATA FLAG flip-flop is set. Thus, BC BUFFERS READY clears DATA SYNC and generates BC LOAD HR, which transfers the BR content into HR. Subsequently, BC BUF RDY DEL sets BC DATA REQ to generate the data interrupt. The executive program responds to the interrupt by executing a MTC DATAI to obtain the word from the HR. MTC DATAI also resets BC DATA REQ and sets BC DATA SYNC.

When the required number of words have been read, the executive program issues a MTS CONO instruction with bit 35 set, which clears BC DATA XFR ACT (drawing BC1); BC LAST WORD is then generated, which, in turn, generates BC LAST BYTE. BC LAST WORD ANDed with T DEACCEL (drawing T1) generates T STOP, which sets the ST JOB DONE flip-flop (drawing S1). JOB DONE now generates a flag interrupt to inform the executive program of the JOB DONE status.

4.13.2 TM10B

The data transfer between the TM10B Magnetic Control Unit and DECsystem-10 memory is accomplished by the DF10 Data Channel. Previous paragraphs described the initial operation of data channel whereby the TM10B Control requested and received access to the data channel.

After the TM10B has gained access to the data channel (when CC CHN SEIZED becomes true), the T GO flip-flop is set by CM MT GO. The CM MT GO pulse also generates the initial device pulse (CHB DEV PLS, drawing CHB) to tell the data channel that is is ready to start operation. If it is a write operation, as signified by CHB SA WRITE being asserted, the data channel responds by putting the 36-bit word onto the channel bus and generating the CHB CHN PLS (channel pulse). The data channel also responds with the data pulses (a pulse is a 1; absense of a pulse is a 0) that come in on the data channel bus (drawing CHND1 and CHND2). The CC DATA FROM CHAN signal enables these input pulses to generate the CHND 00—CHND 35 pulses. These pulses strobe data into the BR (buffer register, drawings BR1 and BR2). The HR00 (1) – HR35 (1) signals are at ground. They are grounded through pins C, E, and R of the W990 modules, which are inserted in place of the S205 modules (used only for TM10A) as shown on drawing HR. The BR was initially cleared by BC BR CLR. The BC BR CLR pulse (drawing BC1) was generated from T SET DF (drawing T2), which was generated from BC WRITING SET DF (drawing BC1).

Simultaneous with the loading of BR, the CHB CHN PLS sets the BC DATA SYNC flip-flop (drawing BC2). The CHB CHN PLS (still assuming a write operation) also generates the CC COMPLETION pulse (drawing CC), which strobes the 1-μs one-shot to generate BC XFER DONE. The BC XFER DONE signal resets the T DATA FLAG flip-flop (drawing T2).

The magnetic tape control now operates as previously described to write the 36 bits from BR onto tape. When all 36 bits have been written, the T DATA FLAG flip-flop is set by WRITING SET DF. The T DATA FLG (1) signal is ANDed (drawing BC2) with BC DATA SYNC to generate BC READY and after the 1-μs delay, the BC BUFFERS READY pulse. The BC BUFFERS READY pulse resets BC DATA SYNC and generates the CHB DEV PLS for the data channel. Again the data channel responds by loading the BR and generating the CHB CHN PULSE. Subsequently, the T DATA FLAG flip-flop is cleared by BC XFER DONE.

The write operation continues until the data channel fetches a 0 control word. When this occurs, the data channel terminates the CHB CHN BUSY signal, which then generates the CC CHAN END (drawing CC). The CC TERMINATE pulse sets the INHIB flip-flop to prevent the CHANNEL START signal from being generated or relayed from another device. After a delay, CC RESET resets the INHIB flip-flop to permit normal data channel operation.

The CC CHAN END pulse also resets CC ACTIVE (drawing CC). The CC CHN SEIZED signal goes false. CC MT START now goes false and generates T STOP CONDITION (drawing T2). T STOP CONDITION (drawing BC1) generates BC LAST WORD, which, in turn, generates BC LAST BYTE. BC LAST BYTE resets WRITE ENABLE and sets WRITE EOR (drawing T1). Operation continues in the manner previously described to write EOR mark and terminate the write operation when end-of-record is detected by read circuits.

It should be noted that the channel is released as soon as it fetches a 0 control word. However, tape operation continues through the decleration delay. If program control desires to continue operation with the same unit, it issues an MTC CONO instruction appropriately coded for the next function. This MTC CONO instruction sets CC WAIT DEL (drawing CC). If the new function does not require a reversal of tape direction, then CC GRAB CHANNEL is generated to request access to the data channel for the ensuing function. In this manner, the request for data channel access is in process while tape control waits for the deceleration delay to terminate.

The data transfer of the read operation using the data channel starts (assuming data channel seized) when the first 36-bit word has been assembled in the BR. The READING SET DF signal (drawing BC1) sets the T DATA FLAG flip-flop (drawing T2). BC DATA SYNC (which was set by the initial CHB CHN PLS) enables T DATA FLAG to generate BC BUFFERS READY (drawing BC2) which generates the CHB CHN DEV PLS. The data from the BR is applied to the data channel bus (drawings CHND 1 and 2). The BC BUFFERS READY pulse generates the CC DATA TO CHN pulses. These pulses strobe the BR data onto the data channel bus. The data pulses on the channel bus trigger corresponding GND00–35 pulses that complement those BR flip-flops that contain 1s, thus clearing the BR.

The BC BUFFERS READY pulse also generates CC COMPLETION (drawing CC), which after a delay (drawing BC2) generates BC XFER DONE. BC XFER DONE clears the T DATA FLAG flip-flop. The read operation continues in this manner until the data channel fetches a 0 control word. When it does, the CHB CHN BUSY signal goes false to terminate operation as described previously.

4.14 ERRORS

4.14.1 Data Late Errors

The data late error indicates that an extraneous word was either written or read from tape before the data transfer facility could supply another word for write, or store the present data buffer word for read. The ST DATA LATE flip-flop (drawing ST) is set when T DATA FLAG is still set (indicating that the data transfer to or from the BR has not occurred) when the BC COUNT or T STROBE CRC pulse occurs.

4.14.2 Parity Error

As discussed during write and read operation, the parity error is the result of either a longitudinal or lateral parity error.

4.14.3 Read/Compare Error

The read/compare error is discussed in the read/compare discussion.

4.14.4 Record Length Incorrect

During read or read/compare operation, this error signifies that the record-length specified differs from the record-length read from tape. The ST REC LEN INC flip-flop (drawing ST) is set for a long record by the READ STROBE (enabled by BC LAST WORD and T ERF, which indicates end-of-record) and by the RECORD OVER pulse (enabled whenthe ~BC LAST WORD and CM FCN 0 (0), which specifies more data) for a short record.

4.14.5 Bad Tape Error

This error indicates that data was in the inter-record gap. The BAD TAPE flip-flop (drawing ST) is set by the T READ STROBE (indicating data present), which is enabled by T DEACCEL and T INTO RECORD.

4.15 ILLEGAL COMMANDS

The ST ILLEGAL OP flip-flop (drawing ST) is set by the CM MT GO pulse when one of the following events occur.

a. Nine-track operation specified and density not set to 800 bpi (with CORE DUMP = 0).

b. Write or write EOF operation specified and the write-lockout bit (WL) from the tape transport is set.

c. Beginning-of-tape status and a reverse motion specified.

4.16 SPACE

There are two commands for spacing records: space forward and space reverse. The initial operation (for either TM10A or TM10B) of space forward or space reverse is accomplished in a similar manner to read or write. The program initiates operation by loading the command register with the space command. Operation is initiated and a record is read. The read strobe is monitored for end-of-record. While spacing over a record, no data is transferred; however, the BC DATA REQ flip-flop is set at the beginning of every record by CM SP RECORD and T ACCEL (B).

Note that CM SP RECORD is the result of CM SPACING ANDed with CM FCN 0 (0), which specifies spacing only one record. Therefore, BC DATA REQ is set only for CM SP RECORD and not for SPACING RECORD.

End-of-record detection, as in normal operation, produces the T RECORD OVER pulse, which initiates the deceleration delay. However, in a spacing operation, it also initiates a data channel transfer by setting T DATA FLAG (drawing T2). The T DATA FLAG initiates a transfer in a manner as explained previously for the TM10A or TM10B. The purpose of the transfer is to determine whether to stop or to space over another record. If the controlling device (data channel for TM10B, executive program for TM10A) responds (with a CHB CHN PULSE or DATAO MTC respectively) and does not terminate the operation, an additional record is spaced.

After spacing over the required number of records, the TM10A or TM10B terminates operation in a manner as previously described.

The detection of end-of-record in the space reverse mode is different from that for a forward motion, because the LPCC is always the first character detected. This is accomplished by the INTO RECORD flip-flop (drawing T2). The READ STROBE, which occurs as the result of the LPCC character, sets the INTO RECORD flip-flop. Note that DATA PRESENT is not set by this READ STROBE. The next READ STROBE occurs when the last character of the record (the first in reverse motion) moves under the read head; this READ STROBE sets the DATA PRESENT flip-flop. When no more READ STROBES occur, EOR 3 (drawing T1) remains set and the next CLOCK pulse sets EOR 4; the following CLOCK pulse generates RECORD OVER, which initiates the deceleration delay.

4.17 SPACE TO END-OF-FILE

In this mode, the space forward or space reverse mode is specified and the tape spaces forward or reverse as described in Paragraph 4.16. The difference, however, is that the tape continues spacing over records until the end-of-file, beginning-of-tape and space reverse, or end-of-tape and space forward occur. The logic implementation of this feature is as follows.

This mode is specified by CM FCN 0 bit a 1. Therefore, CM SPACING does not generate CM SP RECORD, which otherwise generates BC DATA REQ at the start of a record. Because BC DATA REQ is not set, the T STOP CONDITION (drawing T2) is not generated by CM SPACING and BC DATA REQ (1). Instead, T STOP CONDITION waits for CM SP REV ∧TB BOT; T ERF ∧ST EOF (end-of-file); or CM SP FWD ∧TB EOT.

4.18 READ OR READ/COMPARE ACROSS RECORD BOUNDARIES

This operation is similar to read or read/compare except that tape continues after a record is read. This mode is specified by the read or read/compare command with CM FCN0 set to 1. In read or read/compare operation with CM FCN0 set to 0, if operation is not terminated by a CONO MTS, 1 then it is terminated by gate A24-H on drawing T2. This gate generates T STOP CONDITION at the end-of-record (T ERF (1)) when CM FCN0 is 0. With CM FCN0 at 1, read or read/compare operation continues until end-of-record with T DATA FLAG set or the end-of-record and the record read does not contain a multiple of six characters for 7-channel operation (i.e., ~BCC = 0 is true). These conditions generate T STOP CONDITION. Also, any other error will stop operation at the end-of-record. Of course, a CONO MTS, 1 will stop operation.

4.19 READ-IN MODE

The read-in mode permits a completely assembled program to be loaded from an I/O device without a resident memory loader program. When the tape control is selected for read-in mode, tape unit 0 is automatically selected and the tape is rewound to beginning-of-tape on that unit. The read mode is then automatically selected to read one record into memory. This record should contain information specifying further loading procedures.

The read-in mode is initiated by the operation at the central processor control panel. The control panel controls permit selection of an I/O device for the read-in mode. When the tape control is selected, the IOBC MTC SEL signal is enabled by the control panel selection and the IOBC RDI PULSE sets the CM RD IN flip-flop (drawing CM2). The CM RD IN signal ANDed with ST JOB DONE (0) sets the rewind code into the command function register (drawing CM1). The CM RD IN signal also sets the CM WAITING flip-flop to start operation. CM WAITING sets CM UNIT OK, which, in turn, generates CM LEGAL TEST (assuming TB TUR is 1) and subsequently CM MT GO sets the T GO flip-flop. Subsequently, MT IRD OVER generates T BEGIN OP, which resets T GO and ST JOB DONE. During this time, the T SET TAPE FCN signal has transferred the rewind command to unit 0.

With ST JOB DONE coming on and CM RD IN still set, the read command is strobed into the CM FCN register, and core dump, 556 bpi density, and odd parity are set into their respective flip-flops (drawing CM2). CM RD IN sets the CM UNIT OK flip-flop again. When the tape has rewound, the TB TUR level comes on and generates CM LEGAL TEST and subsequently CM MT GO. CM MT GO starts the read operation, which is the same as described previously except that the ST JOB DONE status remains on.

CHAPTER 5
MAINTENANCE

Maintenance procedures are classified into two major categories; preventive maintenance and corrective maintenance. Preventive maintenance procedures are repeated periodically to ensure that system performance is not degrading. Corrective maintenance procedures are performed in the event of equipment malfunctions.

5.1 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the TM10 and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by discovering progressive deterioration at an early stage. A log book should be used to record data found during the performance of each preventive maintenance task. This log book indicates the rate of circuit operation deterioration and provides information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; checks of specific elements such as the power supplies; and margin checks, which aggravate border-line conditions or intermittent failure so that they can be detected and corrected. All preventive maintenance tasks should be performed as a function of conditions at the installation site and downtime limitations of equipment use. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filters. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every four months or 700 equipment operating hours, whichever occurs first, is suggested.

5.1.1 Mechanical Checks

To ensure good mechanical operation of the equipment, perform the following steps and the indicated corrective action for any substandard conditions found:

Step	Procedure
1	Clean the exterior and the interior of the equipment cabinet, using a vacuum cleaner or clean cloths moistened in nonflammable solvent.
2	Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filters in soapy water, allow them to air dry, and spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin) before replacing them in the cabinets.
3	Lubricate door hinges and casters with a light machine oil. Wipe off excessive oil.
4	Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC enamel.

(continued on next page)

Step	Procedure
5	Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.
6	Inspect all mounting panels of logic to ensure that each module is securely seated in its connector.
7	Verify that all bus cables are firmly seated in their respective connectors.
8	Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors giving these signs of malfunction.

5.1.2 Weekly Checks

The transport timing should be checked weekly with the transport timing test (MAINDEC-10-DCTMG).

5.1.3 Monthly Checks

Check the power supply output. It should fall within the ranges listed below. Measure the output ripple with an oscilloscope; if it is greater than the limit given, the power supply at fault can be considered defective.

Nominal Output	Acceptable Range	Maximum Peak-to-Peak Output Ripple	
		60 Hz	50 Hz
+10V	+ 9.5 to 11.5V	.7V	.9V
-15V	-14.5 to 16.5V	.5V	.6V

Run the reliability test (MAINDEC-10-DCTMH) and margin all racks except L to these limits.

+10V	+2 to +20V
-15V	-12 to -18V (Do not exceed these limits)
Panel L	+6 to +18V, -12 to -18V

Individual rack margin limits can be found in the TM10A Acceptance Test Specifications.

NOTE

To ensure reliable operation of the tape transport unit, the maintenance procedures outlined in the tape transport manual should be performed as specified.

5.1.4 Tape Handling

Whenever tape is handled, the operator's hands must be clean to prevent contamination of the tape by body oils and salts. The use of sticky masking tape or cellulose tape for splicing or for holding down the end of the tape on a reel is not recommended because small deposits of the adhesive stick to the tape.

5.1.4.1 Cleaning Tape Reels – If the tape is covered with dust, carefully wipe the surface and backing of the tape with a soft, lint-free cloth such as a very soft chamois. Contamination that does not brush off easily can be washed off with a cloth lightly moistened with Freon TF. Aliphatic hydrocarbon-type solvents (heptane, gasoline, naphtha) can also be used, but extreme care must be used because these compounds are highly flammable. Never use carbon tetrachloride, ethyl alcohol, trichlorethylene, or any other unknown cleaning agent, because these compounds may soften the oxide coating on the tape, deform the backing, or both.

5.1.4.2 Storing Tapes – The best method of tape storage is to place the reel of tape in the self-sealing plastic case supplied for that purpose by DEC. The case should then be stored on edge in a storage bin equipped with partitions between each reel. The plastic case protects tape from dust and sudden changes in humidity and temperature. It also guards both tape and reel from damage that may occur in handling when the tape is transported between work and storage areas. Plastic tape cases and storage bins can be ordered from DEC.

If the tape must be stored in the presence of magnetic fields (either ac or dc), special containers are available from DEC that protect the data from erasure in all but extremely high fields. However, it is desireable to store magnetic tapes away from any such fields if at all possible.

Temperature and humidity extremes should be avoided when possible. Recommended storage conditions are at a temperature of between 60° and 80°F, and within a relative humidity range of 40% to 60%. If extreme temperatures are encountered during storage or transit, the tape should be allowed to be brought up to the ambient temperature before it is used.

5.1.4.3 Physical Distortion – Most signal dropouts in digital recordings are caused by specks of dust and other contaminants which lift the tape away from the head. However, two other significant causes are dents and creases in the base material. Dents are caused by particles wound up tightly in the roll or by roughness in the surface of the hub on which the tape is wound. These can cause permanent dents or creases in many layers of the tape that cannot be stretched out flat as the tape passes over the head. Stresses in the roll that stretch the backing more than 5% usually leave a permanent impression; stresses below this level are usually not permanent. Creases are caused by improper tape handling (threading, splicing, removing tape from guides) or by damage to the edges of the tape caused by uneven winding.

5.1.4.4 Accidental Erasure (or Saturation) – The magnetic properties of magnetic tapes are extremely stable and the magnetic retention is permanent unless altered by strong magnetic fields such as those generated by permanent magnets or electromagnets. If magnets of this type are placed near a tape, partial erasure may occur.

Both unrecorded and recorded magnetic tapes should be kept away from electromagnetic bulk erasures and storage cabinets with magnetic latches. Unrecorded tapes should not be placed near dc magnetic fields (such as travelling wave tubes or magnetron magnets), because the tapes may become heavily biased or may even cause gross distortion during the recording process (in other words, the signal-to-noise ratio may be reduced).

If portions of the tape transport become magnetized, they can cause tape erasure, possible tape saturation, and signal degradation. Periodic demagnetization of critical transport components, particularly the recording heads, is recommended as a preventive maintenance measure.

5.2 CORRECTIVE MAINTENANCE

Corrective maintenance is any maintenance procedure performed to correct a malfunction within the TM10 Magnetic Tape Control. The best tool for corrective maintenance is a sound knowledge of TM10 operation. Test equipment suggested is a broadband oscilloscope and a standard multimeter. A suggested approach for localizing any fault and a method for correcting it as follows.

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the system.

b. System troubleshooting to locate the fault to within a module through the use of signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of a malfunction.

(continued on next page)

e. Validation testing to ensure that the fault has been corrected.

f. Log entry to record pertinent data.

5.2.1 Preliminary Investigation

Before proceeding into any detailed troubleshooting procedure, check that cables and modules are secured, test jumpers are removed, and switches are placed in their correct position. The programmer should check the program on which the malfunction occurred.

5.2.2 System Troubleshooting

Do not attempt to troubleshoot the tape control unit without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings, and note all indicator light operations before and at the time of the error. Careful checks should be made to ensure that the system is actually at fault before continuing with corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a common source of trouble.

If the fault has been isolated to the tape control unit, but cannot be localized to a specific logic function, perform the diagnostic program procedure (see Table 5-1). When the location of the fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation testing should be employed to locate the source of the fault.

Table 5-1
Diagnostic Programs

Program No.	Description	Equipment
MAINDEC-10-DCTMA	Static Test	TM10A
MAINDEC-10-DCTMB	Dynamic Test P1	TM10A
MAINDEC-10-DCTMC	Dynamic Test P2	TM10A
MAINDEC-10-DCTMD	Static Test	TM10B
MAINDEC-10-DCTME	Dynamic Test P1	TM10B
MAINDEC-10-DCTMF	Dynamic Test P2	TM10B
MAINDEC-10-DCTMG	Transport Timing Tests	TM10A and TM10B
MAINDEC-10-DCTMH	Reliability Tests	TM10A and TM10B

5.2.3 Signal Tracing

If the fault has been located within a functional logic element, program the PDP-10 to repeat some instruction in which all functions of that logic element are utilized. If this test is to be performed without the use of the computer, control flip-flops or register flip-flops can be cleared or set manually by momentarily supplying a ground potential to the appropriate flip-flop output terminals. Counting operations of registers can be checked by supplying count pulses to the register from the output of a variable clock. Under these conditions, use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep may be synchronized with any control signal by connecting the trigger input to the appropriate module terminal on the wiring side (front) of the equipment. Trace output signals from the connector back to the origin, and trace input signals from the connector to its final destination. The signal-tracing method can be used to determine with absolute certainty the quality

of pulse amplitude, duration, rise time, and the correct timing sequence of this signal. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

5.2.4 Intermittent Failures

Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive routine, such as the diagnostic program. Often, wiping the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, the module connector for wear and misalignment, and the module wiring for cold solder joints or wiring kinks.

5.2.5 Module Circuits

The basic functions and specifications for standard modules are presented in the *Digital Logic Handbook* (C-105). Circuit schematics of each module are provided in the *Module Schematic Notebook.*