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PDP-11/45, 11/50, and 11/55 system maintenance manual

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INTRODUCTION

The basic PDP-11/45 and 11/50 systems, prior to 1976, were available with a KB11-A central processor, an FP11-B floating point unit, and MOS or bipolar memory. With the introduction of a high-performance floating point unit (the FP11-C), the KB11-A underwent extensive revision, generating a new CPU version – the KB11-D. An entirely new system, including the KB11-D, FP11-C, and bipolar memory, is now available as a PDP-11/55. The PDP-11/45 and 11/50 systems are still available as they were prior to 1976, but the PDP-11/45 is now also available with the KB11-D and its compatible options.

This manual explains the installation and maintenance procedures that apply to all components and options of the PDP-11/45, PDP-11/50, and PDP-11/55 systems. The basic PDP-11/50 system uses a KB11-A central processor and solid-state (MOS) memory. The basic PDP-11/55 system uses the KB11-D central processor and bipolar memory. The basic PDP-11/45 system uses a KB11-A or KB11-D central processor and can have either (or both) MOS and bipolar memory. The basic PDP-11/45, 11/50, and 11/55 systems each generally contain a minimum of 16K words of memory.

All references to PDP-11/45 system in this manual also apply to PDP-11/50 and 11/55 systems, except where otherwise indicated. The manual is organized as follows:

Chapter 1 describes the basic system configurations and specifications and lists related reference documents and engineering drawings.

Chapter 2 details site preparation, unpacking and installation procedures, and installation checkout procedures for the basic system.

Chapter 3 presents a general description of the power distribution within the CPU cabinet.

Chapter 4 details ac power control and distribution.

Chapter 5 describes dc power distribution and voltage regulators.

Chapter 6 lists test equipment requirements, preventive maintenance procedures, diagnostic programs and procedures, use of special maintenance cards and extender boards, disassembly procedures, techniques for the removal and replacement of integrated circuits on multilayer modules, and a special MOS device handling procedure.

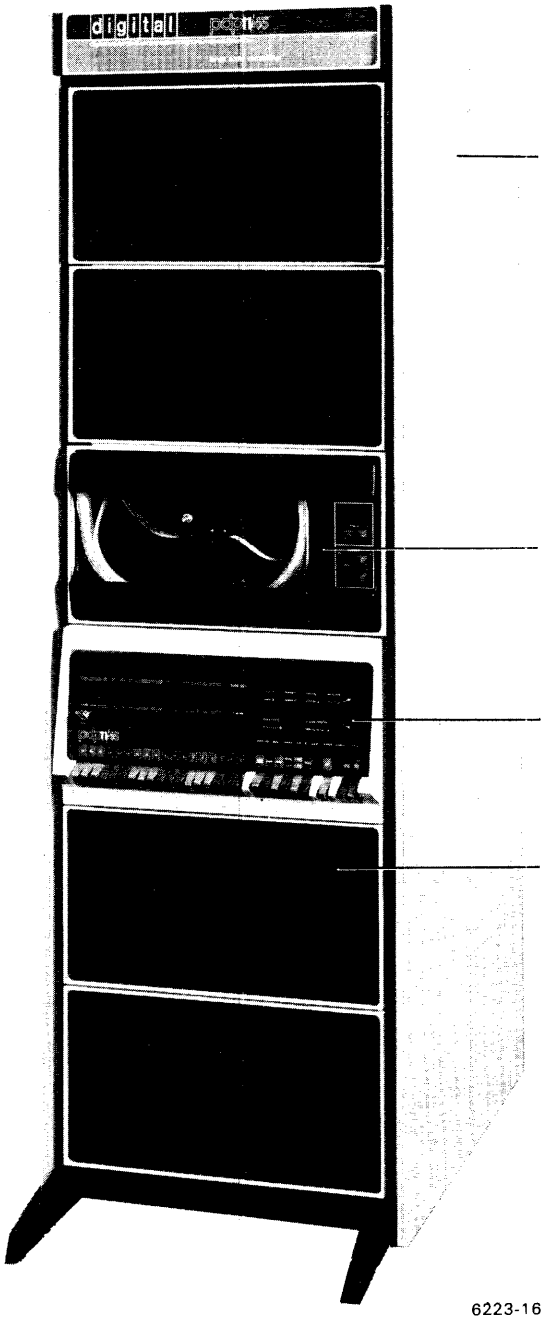
Chapter 7 specifically refers to plug-in card options and Chapter 8 to system unit options.

Appendix A describes the more complex integrated circuits that are used in the PDP-11/45, 11/50, 11/55, and options.

Appendix B is a peripheral preventive maintenance schedule.

Appendix C lists PDP-11 options and their specifications.

The major components and options for the PDP-11/45, 11/50, 11/55 systems are individually described in a series of manuals listed in Table 1-8, Related Documentation.


H960-C CABINET
PR11 PAPER TAPE READER
(PERIPHERAL OPTION)
KB11-A CENTRAL PROCESSOR
UNIT CONSOLE
BA11-FA
MOUNTING BOX

6223-16

CHAPTER 1
GENERAL DESCRIPTION

1.1 BASIC SYSTEM DESCRIPTION

The basic PDP-11/45, 11/50, 11/55 system components are located in a single H960 Cabinet Assembly (Figures 1-1 and 1-2). Table 1-1 lists the major components and assemblies included in the basic PDP-11/45 system. Table 1-2 lists components and major assemblies included in the basic PDP-11/50 system. Table 1-3 lists the major components and assemblies included in the basic PDP-11/55 system.

Note that four different power distribution systems exist for the PDP-11/45, 11/50, and 11/55 systems due to accumulated revisions. Paragraph 3.3 explains the revisions and Table 3-2 lists the power system versions. Note also that the PDP-11/55 uses only the latest version; the PDP-11/50 and the PDP-11/45 can have any of the four power system versions depending upon the date of manufacture.

1.1.1 Physical Characteristics

The overall dimensions of the cabinet supplied with the basic PDP-11/45, 11/50, 11/55 systems are:

Height: 71-7/16 in. (181.3 cm)
Width: 21-11/16 in. (54 cm)
Depth: 30 in. (76 cm)
With Cabinet Feet: 39 in. (99 cm)

A fully configured cabinet with all options implemented and three additional system units weighs approximately 300 lb (135 kg). Maximum weight, with peripherals, is approximately 500 lb (225 kg).

Additional details are provided on engineering drawings D-UA-H960-D-0, Cabinet Assembly, and E-UA-H950-A-0, H950A 19-Inch Frame Assembly.

1.1.2 General Power Requirements and Electrical Specifications

The 11/45, 11/50, and 11/55 come in many configuration variations depending upon the various combinations of options that are used together. However, from an input power standpoint only two variations need be considered: a 115 V two-phase (or two of three phases) variation of which the 11/45-CA will be taken as an example, and a 230 V variation of which the 11/45-CB will be taken as an example.

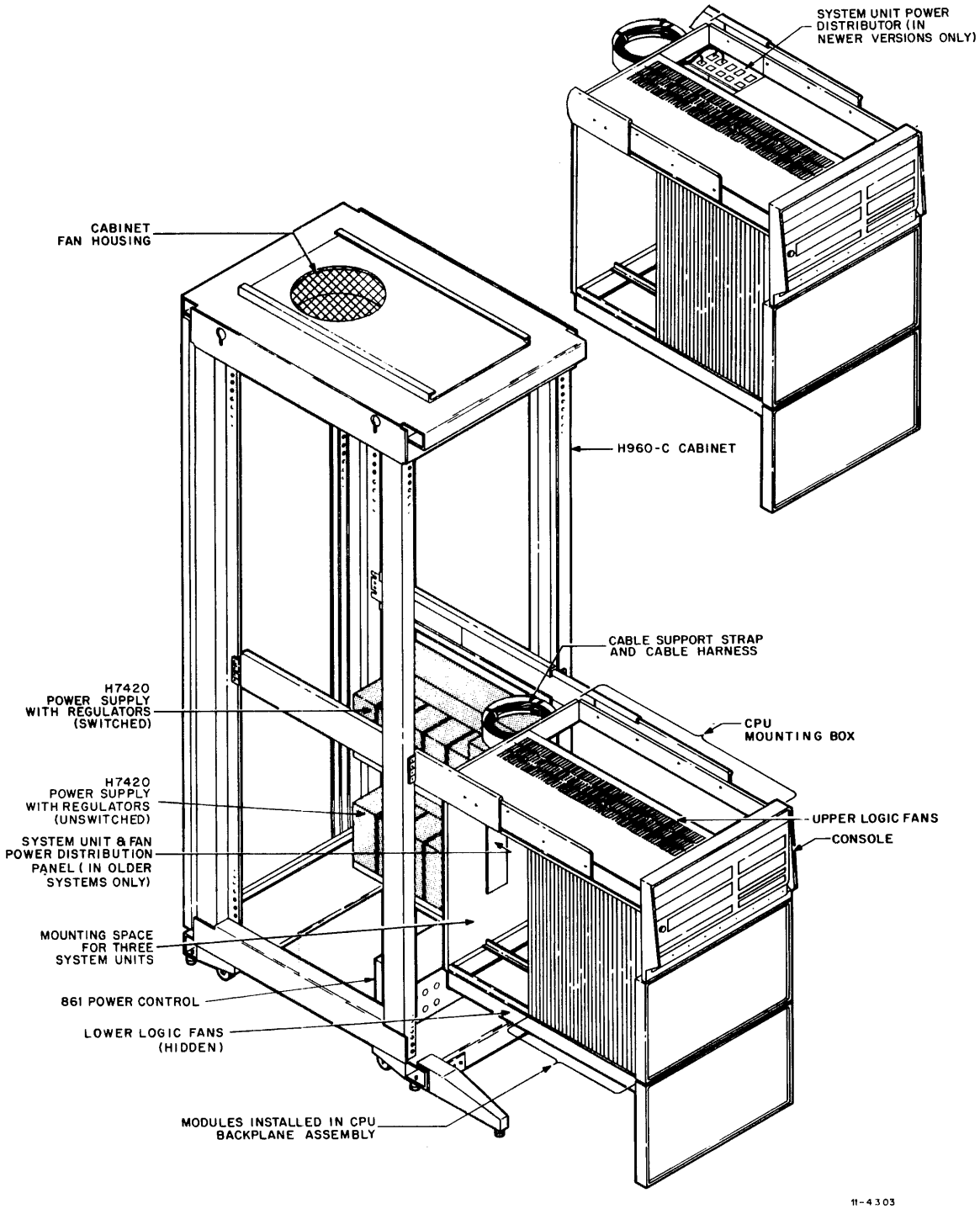


Figure 1-1 Location of Major Components and Assemblies Showing New Models Using 861 Power Control

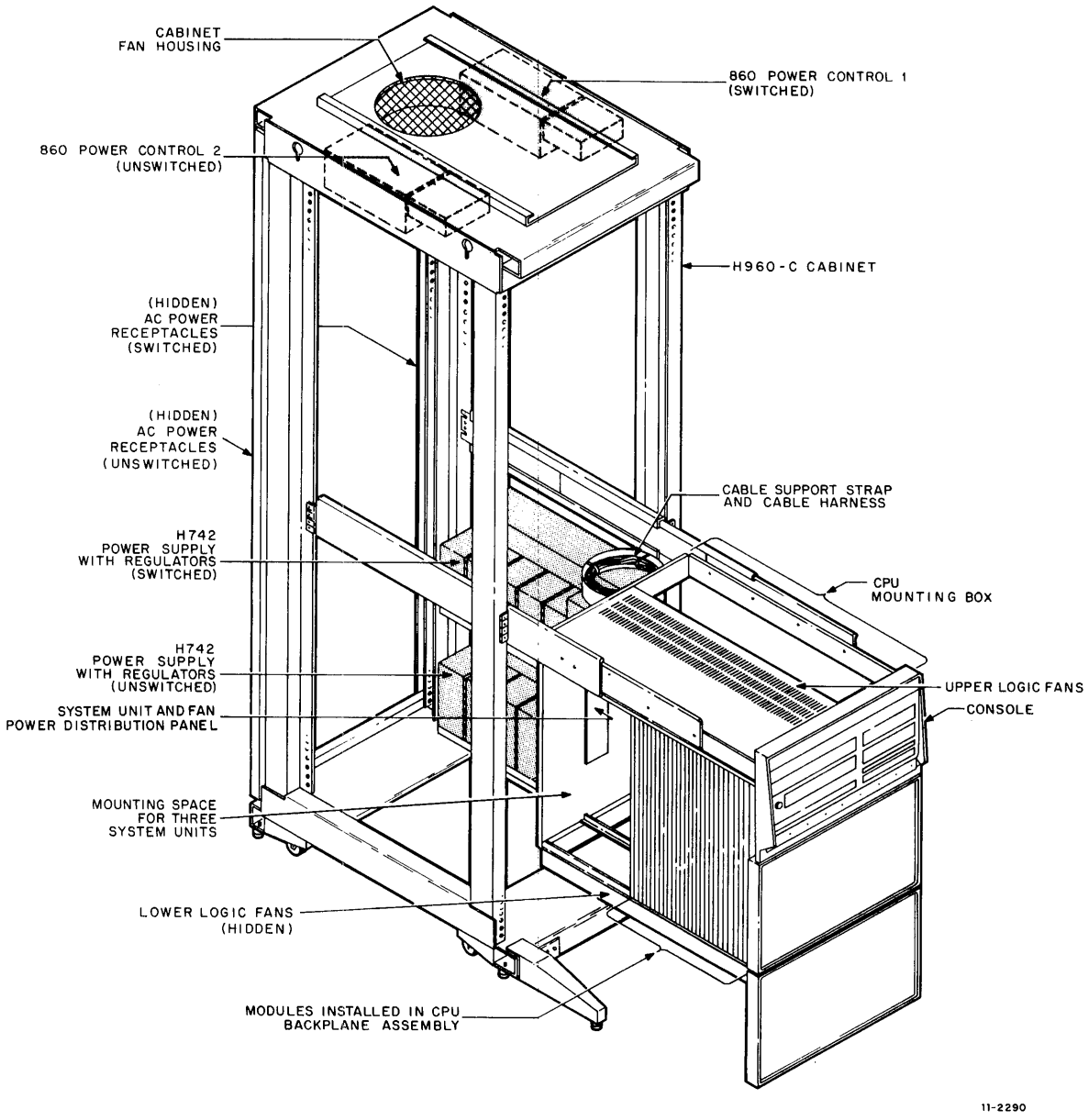


Figure 1-2 Location of Major Components and Assemblies Showing 860 Power Controls Used on Early Models

Table 1-1 Basic PDP-11/45 Configuration

Item*	Description
Cabinet Assembly	Refer to Figure 1-1. Houses all other major assemblies and components, except terminal.
CPU Mounting Box	Refer to Figure 1-1. Houses KB11-A, D CPU plus other 11/45 options.
KB11-A, D Central Processor Unit	Basic 16-bit processor logic module installed in wired CPU backplane (part number 7008871). See Table 1-2 for KB11-A modules and Table 1-3 for KB11-D modules.
H7420 Power Supplies†	Refer to Figure 1-1. Upper H7420 provides switched power; lower H7420 provides unswitched power.
H744 +5 Regulators	Three H744 +5 V regulators installed in upper H7420 power supply (slots B, C, and D).
H745 -15 Regulator	One H745 -15 V regulator installed in upper H7420 power supply (slot E).
861 Power Control	Refer to Figure 1-1. Controls both switched and unswitched H7420 power supplies. Replaces two 860 power controls used on early systems as shown in Figure 1-2.
MF11-UP 16K Core Memory and Control	Provides 16K core memory, with parity. Mounts in two system unit locations on BA11-FA.
MM11-UP 16K Core Memory	Additional 16K core memory to provide total 32K core memory for basic system.
LA36 DECwriter	Serial I/O terminal; described in related manual.
DL11-A Terminal Control	LA36 DECwriter II interface to Unibus; described in related manual.

*Items listed are major components of basic PDP-11/45-CC, -CD systems. Refer to engineering drawing A-PL-11/45-0-0 for complete parts list for all PDP-11/45 systems.
†Early versions of the PDP-11/45 used H742 power supplies.

Table 1-2 Basic PDP-11/50 Configuration

Item*	Description
Cabinet Assembly	Refer to Figure 1-1. Houses all other major assemblies and components, except terminal supplied.
CPU Mounting Box	Refer to Figure 1-1. Houses KB11-A CPU, plus other 11/50 options.
KB11-A Central Processor Unit	Basic 16-bit processor logic modules installed in wired CPU backplanes (part number 7008871).
Consists of the following:	
M8100 DAP Module	Data and address paths (slot 6)
M8101 GRA Module	General registers and control (slot 7)
M8102 IRC Module	Instruction register and decode (slot 8)
M8103 RAC Module	ROM and ROM control (slot 9)
M8104 PDR Module	Processor data and Unibus registers (slot 10)
M8105 TMC Module	Trap and miscellaneous control (slot 11)
M8106 UBC Module	Unibus and console control (slot 12)
M8116 SJB Module	System jumper board (slot 14)
M8109 TIG Module	Timing generator (slot 15)
H7420 Power Supplies†	Refer to Figure 1-1. Upper H7420 provides switched power, lower H7420 provides unswitched power for MOS memory.
H744 +5 Regulators	Three H744 +5 V regulators installed in upper H7420 power supply (slots B, C, and D).
H745 -15 Regulator	One H745 -15 V regulator installed in upper H7420 power supply (slot E).
861 Power Control	Refer to Figure 1-1. Controls both switched and unswitched H7420 power supplies. Replaces two 860 power controls used on early systems as shown in Figure 1-2.
MS11-BC MOS Memory Control	Controls up to two 16K of MOS memory; described in related manual.
Consists of the following:	
M8110 SMC Module	Semiconductor memory control (slots 16 and 21)
H744 +5 Regulator	One H744 +5 V regulator installed in lower H7420 power supply (slot J)
H746 MOS Regulator	One H746 MOS regulator installed in low H7420 power supply
MS11-BP 4K MOS Memory	Up to eight can be used to provide up to 32K MOS memory.
Consists of the following:	
G401 YA MOS Memory Matrix	Each provides 4K words of MOS memory with two additional bits for byte parity storage (slots 17, 18, 19, and 20).
LA36 DECwriter	Serial I/O terminal; described in related manual.
DL11-A Terminal Control	LA36 DECwriter II interface to Unibus; described in related manual.

* Items listed are major components of basic PDP-11/50-CC,-CD systems. Refer to engineering drawing A-PL-11/50-0-0 for complete parts list for all PDP-11/50 systems.
† Early versions of the PDP-11/50 used H742 power supplies.

Table 1-3 Basic PDP-11/55 Configuration

Item*	Description
Cabinet Assembly	Refer to Figure 1-1. Houses all other major assemblies and components, except terminal supplied.
CPU Mounting Box	Refer to Figure 1-1. Houses KB11-D CPU, plus other 11/55 options.
KB11-D Central Processor Unit	Basic 16-bit processor logic modules installed in wired CPU backplane (part number 7008871).
Consists of the following:	
M8100 DAP Module	Data and address paths (slot 6)
M8101 GRA Module	General registers and control (slot 7)
M8132 IRC Module	Instruction register and decode (slot 8)
M8123 RAC Module	ROM and ROM control (slot 9)
M8104 PDR Module	Processor data and Unibus registers (slot 10)
M8105 TMC Module	Trap and miscellaneous control (slot 11)
M8119 UBC Module	Unibus and console control (slot 12)
M8109 TIG Module	Timing generator (slot 15)
KT11-CD Memory Management Unit	Basic 18-bit extension of the processor address space.
Consists of the following:	
M8107 SAP Module	System address path (slot 14)
M8108-YA SSR Module	System status register
H7420 Power Supples	Refer to Figure 1-1. Upper H7420 provides switched power, lower H7420 provides unswitched power for bipolar memory.
H744 +5 Regulators	Three H744 +5 V regulators installed in upper H7420 power supply (slots B, C, and D).
H745 -15 Regulator	One H745 -15 V regulator installed in upper H7420 power supply (slot E).
861 Power Control	Refer to Figure 1-1. Controls both switched and unswitched H7420 power supplies. Replaces two 860 power controls.
MS11-CC Bipolar Memory Control	Controls up to two 16K bipolar memory; described in related manual.
Consists of the following:	
M8120 SMC Module	Semiconductor memory control (slots 16 and 21)
H744 +5 Regulator	Two H744 +5 V regulator installed in lower H7420 power supply (slots H and J)
MS11-AP 4K Bipolar Memory	Up to eight can be used to provide up to 32K bipolar memory.
Consists of the following:	
M8121-YA Bipolar Memory	Each provides 4K words of bipolar memory with two additional bits for byte parity storage (slots 17, 18, 19, and 20).
M9301-YB Bootstap Loader	Provides memory space for bootstrap programs (slots A and B).

Table 1-3 Basic PDP-11/55 Configuration (Cont)

Item*	Description
LA36 DECwriter	Serial I/O terminal; described in related manual.
DL11-W Terminal Control	LA36 DECwriter II interface to Unibus; described in related manual. Replaces DL11-A and KW11-L of early 11/55 version (slot DEV.1).
DL11-A Terminal Control†	LA36 DECwriter II interface to Unibus; described in related manual.
KW11-L Line Time Clock†	Provides timing pulses for DECwriter; described in related manual (slot 1).

*Items listed are major components of basic PDP-11/55-CC,-CD systems. Refer to engineering drawing A-PL-11/55-0-0 for complete parts list for all PDP-11/55 systems.
†Items used only in early production versions instead of the DL11-W Terminal Control

The 11/45-CA and 11/45-CB variations consist of the following:

	11/45-CA	11/45-CB
Central Processor (no options installed)	KB11-A,D	KB11-A,D
Cabinet	H960-C	H960-C
Mounting Box	BA11-FA	BA11-FA
Power Control	861-A (115 V two-phase)	861-B (230 V single-phase)
Power Supply (2)	H7420-A (or H742-A)	H7420-B (or H742-B)

Table 1-4 provides the input specifications for the 11/45-CA and 11/45-CB variations. These specifications will apply equally to the corresponding 11/50 and 11/55 configurations.

1.1.2.1 Internal Option Power Requirements – For a given 11/45, 11/50, 11/55 CPU configuration the total power required will be dependent on the options installed. Table 1-5 lists option dc power, ac power, and ac currrent. To determine the total ac power and ac current for a given system configuration, the ac powers and ac currents for the options (from Table 1-5) must be added to the basic power and current specified in Table 1-4.

Table 1-4 Input Specifications

Characteristic	11/45-CA	11/45-CB
Voltage		
Range	95–130 Vrms-ac	190–260 Vrms-ac
Nominal	115 Vrms-ac	230 Vrms-ac
Frequency	47–63 Hz	47–63 Hz
Power	870 W* (2971 Btu/hour)	870 W* (2971 Btu/hour)
Current	9 Arms*	4.5 Arms*
Over-Voltage (period < 50 ms)	Up to 180 Vrms-ac	Up to 360 Vrms-ac
Inrush Current (< 20 ms)	240 A peak/phase	150 A peak/phase
Line Dips and Outages		
Extended Operation:	> 95 Vrms-ac	> 190 Vrms-ac
Temporary Line Loss:	The dc outputs of the power supplies will remain within tolerance for at least 20 ms after loss or reduction of power below operating range. The power-fail warning signals to the KB11-A, D will be generated in time for an orderly shutdown before loss of dc regulation.	
Circuit Breaker Rating	20 A/phase for each of two phases, simultaneous trip	
Voltage Dynamic Variation	< ±10%/second	
Harmonic Distortion	< 5% of fundamental	
Single Harmonic	< 3% of fundamental	
High Voltage Transients (either polarity, differential or common mode)	< 300 V peak (< 0.2 watt-second) < 0.5 W average power	
Single Transients	< 600 V peak (< 2.5 watt-second)	

*Basic configuration only, for calculating total input power and current with options installed, see Paragraph 1.1.2.1.

Table 1-5 Option Power Requirements (Maximum)

Option	Name	DC Power (watts)	AC Power		AC Current (AMPS)	
			(watts)	(Btu/hour)	@ 115 V	@ 230 V
KB11-A	Central Processor	145	290	990	3.8	1.9
KB11-D	Central Processor	145	290	990	3.8	1.9
FP11-B	Floating Point Processor	75	150	512	1.5	0.75
FP11-C	Floating Point Processor	125	250	854	2.6	1.3
KT11-C	Memory Management	40	80	273	0.8	0.4
KT11-CD	Memory Management	40	80	273	0.8	0.4
MS11-AP	4K Bipolar Parity Memory Matrix	60	120	410	1.3	0.7
MS11-BC, BD	MOS Memory Control	15	30	130	0.3	–
MS11-BM, BP, BR, BT	4K MOS Memory Matrix	40	80	273	0.8	0.4
MS11-CC	Bipolar Memory Control	15	30	102	0.3	0.15
MS11-CM, CP	1K Bipolar Memory	55	110	376	1.2	0.6

NOTES

1. **KB11-A and KB11-D are included for reference only. They are already included in the basic 11/45-CA and 11/45-CB specifications.**
2. **Each type of memory matrix requires a memory control.**

There is mounting space for three system unit options (SU) at the rear of the CPU box. In addition, the CPU backplane is prewired for three quad-height small-peripheral controller modules (SPC). The processor power supply provides power to these option mounting areas via the harness and backplane. The amount of power available is shown below.

+5.0 V :24.0 A
+15.0 V :1.5 A
+20.0 V :8.0 A } SU locations only
-5.0 V :8.0 A }
-15.0 V :9.5 A

NOTE

The slot E H754 may be removed and an H745 installed in its place. (Machines with serial numbers less than 2000 always have the H745 in slot E.) With the H745 regulator in slot E:

1. **There is an additional 9.5 A of -15 V available to the three SPC slots (in the CPU backplane).**
2. **There is an additional 10 A of -15 V available to the three system unit locations at the back of the CPU box.**
3. **Ther is NO +20 V or -5 V available to the three system unit locations at the back of the CPU box.**

1.1.2.2 Determining Option Power and Line Current Requirements – To determine the power and line current required by non-CPU options not listed in Table 1-5, perform the calculations below. An example is also provided.

1. Find the maximum total dc current for each supply voltage used by an option and then multiply the total current by its respective voltage and add the products to determine the total dc power requirement.

   Example:

MF11-U =	+5 V @ 6.1 A =	30.5 watts dc
	+20 V @ 3.4 A =	68.0 watts dc
	-5 V @ 0.5 A =	2.5 watts dc
Total dc power requirement =		101.0 watts dc

2. Double the dc power requirement to obtain the ac power requirement. (Combined efficiency of regulator and transformer is 50% minimum.)

   Example:

   101 watts dc (from step 1)
   ×2
   202 watts ac

3. Divide ac power by 0.85 to compensate for worst case power factor to give maximum input volt-amperes (reactive) and then divide again by 115 V (or 230 V) to obtain nominal ac current for the option.

   Example:

   a. $0.85\overline{)202.0}$ watts ac → 237.6 volt-amperes (reactive)

   b. $115\overline{)237.6}$ volt-amperes (reactive) → 2.07 amperes rms ac

   Total ac current requirement = 2.07 amperes rms

4. To obtain Btu/hour, multiply total watts ac (step 2) by 3.415 (Btu/watt-hour).

   Example:

   202 watts
   ×3.415 Btu/watt-hour
   689.8 Btu/hour

1.1.3 H7420 Power Supply Characteristics

Each H7420 contains space for up to five plug-in voltage regulators (See Paragraphs 1.1.4 and 1.1.5). These regulators furnish dc to the processor backplane and the processor console. In addition to the regulators, each H7420 contains a 5411086 regulator. The 5411086 in the upper H7420 provides +8 and 15 V to the processor backplane and functions as a power line monitor for the upper supply. The upper 5411086 also produces the line clock output that is used to drive the KW11-L or DL11-W (Line Frequency Clock option). The 5411086 in the lower H7420 provides -15 V to the processor and monitors the lower power supply's input line voltage.

Each H7420 also contains an input terminal block and transformer assembly. The input terminal block in the upper H7420 provides 115 Vac to the elapsed time meter, power supply fans, and transformer primary. The input terminal block in the lower H7420 provides 115 Vac to the power supply fans, transformer primary, and the processor mounting box fans. By altering a jumper configuration on the terminal block, 230 Vac operation is available. The transformer produces 20–30 Vac for its associated voltage regulators.

1.1.4 H742 Power Supply Characteristics

Each H742 power supply has space for five plug-in voltage regulator modules. One function of each H742 power supply is to provide 20–30 Vac to its associated voltage regulators. They also provide the power fail control signals AC LO and DC LO, to the processor. The upper H742 provides +15 Vdc at 3A to enable the H745 -15 V regulators and the M8109 TIG module, +8 Vdc for maintenance card indicators, and the line clock signal. The lower H742 provides -15 Vdc to the M8110 SMC module when the MS11 Semiconductor Memory System is installed in the system.

1.1.5 Voltage Regulator Characteristics

In a basic system, the upper H742 is equipped with three H744 +5 V regulators (in slots B, C, and D) and an H745 -15 V regulator (in slot E). As options are added to the basic system, additional H744 +5 V, H745 -15 V, and/or an H746 MOS regulator are added to slots A, F, H, J, K, and L; an H754 regulator replaces the slot E -15 V regulator if options requiring +20 V and -5 V (such as MF11-U/UP) are installed in system units 1, 2, or 3 (refer to Table 1-6). Output characteristics of these plug-in regulators are shown in Table 5-2.

1.1.6 Interface Specifications

The PDP-11/45, 11/50, 11/55 system is completely compatible with the standard PDP-11 Unibus interface, which is fully described in a related manual. Provision is made on the CPU backplane for two separate PDP-11 Unibus interface connections, designated Unibus A and Unibus B. Block diagrams of the system Unibus interfaces are shown in Figure 1-3. Briefly, Unibus A connects directly to the KB11-A, D, and Unibus B connects to the MS11 Semiconductor Memory System when that option is implemented in the system. Unibus interconnection details are provided in Chapter 2 of this manual (Paragraph 2.3.5.1).

1.1.7 Environmental Specifications

The basic PDP-11/45, 11/50, 11/55 electronics operate in the following environment (at sea level):

Temperature range	50° to 110° F (10° to 40° C)
Relative humidity (without condensation)	10% to 90%

For operation above sea level, the maximum operating temperature must be reduced by 1.0° F/1000 ft (1.6° C/1000 m).

Peripheral equipment associated with the system may require closer environmental tolerances. Refer to Appendix C for specifications.

1.2 SYSTEM CONFIGURATIONS AND OPTIONS

Table 1-6 lists some of the PDP-11/45 options that can be implemented within the CPU mounting box. A block diagram that shows the relationship of these options is provided in Chapter 1 of the *KB11-A, D Central Processor Unit Maintenance Manual.* Peripherals or options that may be installed in the upper half of the H960-CD cabinet are not included in Table 1-6.

1.3 EXPANSION CABINET OPTION

An H960-D expansion cabinet option is available with the PDP-11/45, 11/50, 11/55 systems. It is not included as part of the basic system, but may be ordered as required to house additional peripheral devices or memory. The basic components that may be included in each expansion cabinet option are summarized in Appendix C. Chapter 4 provides instructions for interconnecting the H960-D remote power control to the CPU Cabinet Assembly.

The H960-D cabinet includes a BA11-FB mounting box in the lower half of the cabinet which provides space for nine system units. The upper half of the H960-D cabinet is available for mounting other equipment. The H960-D includes an H7420 power supply that can adequately service the nine system units that can be installed in the BA11-FB mounting box. Additional power supplies must be provided for or included as part of the additional equipment that is installed in the upper half of the cabinet.

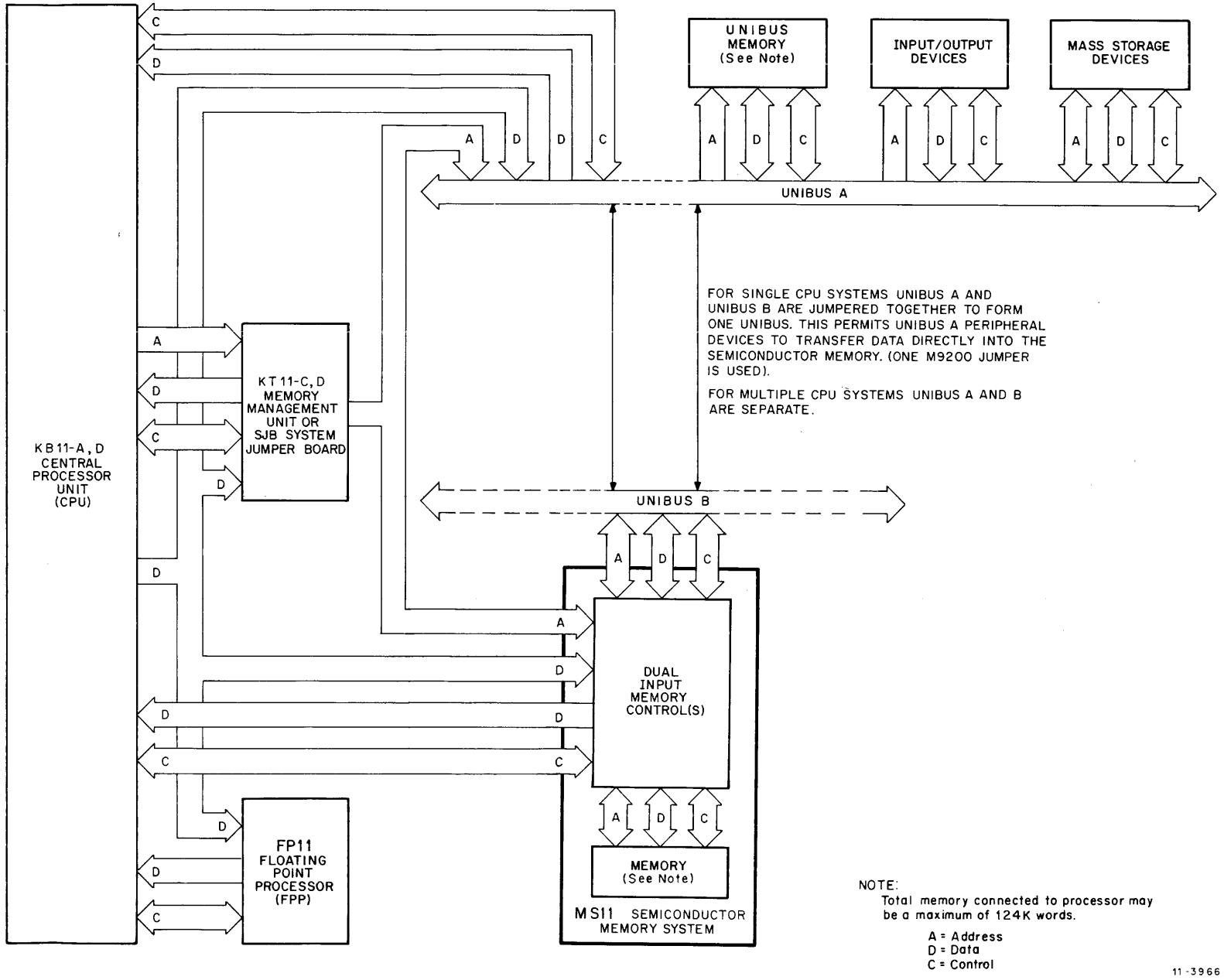


Figure 1-3 Unibus A and B Connectors

Table 1-6 PDP-11/45 System Options

Option*	Description
FP11-B, C Floating Point Processor	
Consists of the following:	Described in related manual.
FP11-C FP11-B	Logic modules mount in CPU backplane, in slots indicated.
M8128 M8112 FRM Module	FP ROM and ROM control (slot 4).
M8129 M8113 FXP Module	FP exponent and data path (slot 5).
M8126 M8114 FRH Module	Fraction data path – high order (slot 2).
M8127 M8115 FRL Module	Fraction data path – low order (slot 3).
H744 +5 V Module	Mounts in space provided on upper H7420 power supply (slot A).
KT11-C, CD Memory Management Unit	
Consists of the following:	
	Described in related manual. Required for all systems with more than 28K of memory. Permits addressing of up to 124K of memory.
KT11-CD KT11-C	Logic modules mount in CPU backplane in slots indicated.
M8108-YA M8108 SSR Module	System status registers (slot 13).
M8107 SAP Module	System address path (slot 14, replaces the M8116 SJB module).
KW11-L Line Frequency Clock	
Consists of the following:	
M787 Line Time Clock Module	Described in related manual. Mounts in CPU backplane slot 1, row C. Refer to Paragraph 7.4.
MS11-B MOS Memory	
MS11-BC MOS Memory Control	Described in MS11 manual. Controls up to four G401 or G401YA MOS memory matrix modules (16K words of MOS memory).
Consists of the following:	
M8120 SMC Module	Semiconductor memory control for first 16K of MOS memory. Mounts in CPU backplane (slot 16).
H744 +5 V Regulator	One required. Mounts in slot J of lower H7420 power supply.
H746 MOS Regulator	One required. Mounts in slot H of lower H7420 power supply.

*See engineering drawings for complete parts lists.

Table 1-6 PDP-11/45 System Options (Cont)

Option*	Description
	MS11-B MOS Memory (Cont)
MS11-BD MOS Memory Control Consists of the following:	Second MOS memory control for up to additonal 16K words of MOS memory.
M8110 SMC Module	Semiconductor memory control for second 16K of MOS memory. Mounts in CPU backplane (slot 21).
H746 MOS Regulator	One additional H746 voltage regulator is required for second 16K of MOS memory. Mounts in slot L of lower H7420 power supply.
MS11-BM 4K MOS Memory Consists of the following:	Provides 4K words of MOS memory.
G401 MOS Memory Matrix	Mounts in CPU backplane. Slots 17 through 20 accommodate first four 4K modules. Slots 22 through 25 accommodate second four 4K modules.
MS11-BP 4K MOS Memory Consists of the following:	Provides 4K words of MOS memory with two additional bits for byte parity storage.
G401YA MOS Memory Matrix	Mounted in CPU backplane in same configuration indicated for G401 modules.

NOTE
A complete 32K MOS memory system consists of two M8110 SMC Modules, eight G401 MOS Memory Matrix Modules, one H744 +5 V Regulator, and two H746 MOS Regulators.

	MS11-A, C Bipolar Memory
MS11-CC Bipolar Memory Control Consists of the following:	Described in MS11 manual. Controls up to four M8111 or M8121-YA Bipolar Memory Matrix Modules.
M8120 SMC Module†	Semiconductor memory control. Mounts in CPU backplane Control for first 4K of bipolar memory mounts in slot 16 Control for second 4K of bipolar memory mounts in slot 21.
H744 +5 V Regulators	Two required for each 4 bipolar memory matrix modules. If no MOS memory is implemented, H744s mount in lower H7420 power supply slots H and J. If MOS is implemented, H744s for bipolar memory mount in lower H7420 power supply slots K and L.

*See engineering drawings for complete parts lists.
†Early versions of the MS11-CC used an M8110 SMC Module.

Table 1-6 PDP-11/45 System Options (Cont)

Option*	Description
MS11-A, C Bipolar Memory (Cont)	
MS11-AP 4K Bipolar Memory Consists of the following: M8121-YA Bipolar Memory Matrix Module	Provides 4K words (18 bits: 16 bits plus 2 bits for byte parity storage) of bipolar memory. Mounts in CPU backplane. Slots 17 through 20 accommodate first four 4K modules. Slots 22 through 25 accommodate second four 4K modules.
MS11-CM 1K Bipolar Memory Consists of the following: M8111 Bipolar Memory Matrix Module	Provides 1K word of bipolar memory. Mounts in CPU backplane. Slots 17 through 20 accommodate first four 1K modules. Slots 22 through 25 accommodate second four 1K modules. If bipolar is mixed with MOS, M8111 modules mount in slots 22 through 25.
MS11-CP 1K Bipolar Memory Consists of the following: M8111-YA Bipolar Memory Matrix Modules	Provides 1K words of bipolar memory with two additional bits for byte parity storage. Mounted in CPU backplane in same configuration as M8111 modules.

NOTE

A complete 8K bipolar memory system consists of two M8120† SMC modules, eight M8111 bipolar memory matrix modules and four 744 +5 V regulators. A complete 32K bipolar memory system consists of two M8120† SMC modules, eight M8121 bipolar memory matrix modules and four H744 +5 V regulators.

MF11-U/UP 16K Core Memory and Control	
Includes the following: MF11-U M8293 16K Unibus Timing Module G114 Sense Inhibit Module G235 X–Y Driver Module H217D Stack Module (16 bits) 7009295 Backplane Assembly	Described in related manual. Mount space and power for one of these units is provided in the CPU mounting box. Additional MF11-U/UP units can be installed in separate H960-D Cabinets.

*See engineering drawins for complete parts lists.
†Early versions of the MS11-CC used an M8110 SMC Module.

Table 1-6 PDP-11/45 System Options (Cont)

Option*	Description
MF11-U/UP 16K Core Memory and Control (Cont)	
MF11-UP M8293 16K Unibus Timing Module G114 Sense Inhibit Module G235 X–Y Driver Module H217C Stack Module (18 bits including parity) 7009295 Backplane Assembly M7259 Parity Control Module MM11-U Module Set Includes all modules listed in MF11-U but does not include backplane assembly MM11-UP Module Set Includes all modules listed in MF11-UP but does not include backplane assembly	
NOTE **The MF11-U/UP option cannot be installed in CPU Cabinets containing the older power distribution system. It can, however, be used in the older version of the Expansion Cabinets. Refer to Paragraph 8.5d.**	
MF11-L, MF11-LP 8K Core Memory and Control	
Includes the following: MF11-L G110 Control Module G231 Driver Module H214 8K Core Stack (16 bits) 11/45 System Unit MF11-LP G109 Control Module G231 Driver Module H215 8K Core Stack with Parity (18 bits) M7259 Parity Module 11/45 System Unit	Described in related manual. Mount space and power for three of these units is provided in the CPU Mounting Box. Additional MF-11 units can be installed in the spearate H960-D Expansion Cabinets.

*See engineering drawings for complete parts lists.

Table 1-6 PDP-11/45 System Options (Cont)

Options*	Description
Bootstrap Loaders	
MR11-DB Bootstrap Loader	64-word bulk storage bootstrap loader (slots 27 and 28).
Consists of the following:	
M792-YD ROM Diode Matrix M792-YE ROM Diode Matrix	
M9301-YB Bootstrap/Terminator	512-word bulk storage bootstrap loader and Unibus termination (slot 1).
BM873-YB Restart/Loader	256-word bulk storage bootstrap loader (slot 27).
DL11-A,W DECwriter Interface	
DL11-A Asynchronous Interface	Interface between a single teletypewriter and the PDP-11 (slot 26).
DL11-W Asynchronous Interface	
Consists of the following:	
M7856	Interface between a single teletypewriter and the PDP-11 with a line frequency clock (DL11-A and KW11-L)

*See engineering drawings for complete parts lists.

1.4 REFERENCE DOCUMENTS

Table 1-7 describes the following reference material:

1. A six-manual series of PDP-11/45, 11/50, 11/55 maintenance manuals.
2. The maintenance manuals for the various components supplied as part of the basic system.
3. Several reference manuals that describe the PDP-11/45, 11/50, 11/55 system and provide essential information pertaining to all PDP-11 systems.

Documentation for specific peripherals and options that are external to the CPU cabinet are not listed in the table. When peripherals and options are included in the system, the appropriate manuals are supplied with the system.

1.5 ENGINEERING DRAWINGS

PDP-11/45, 11/50, 11/55 systems are shipped with a set of engineering drawings for the basic components and applicable options. Table 1-8 lists the contents of the drawing sets that are provided. Information pertaining to additional engineering drawings is contained within each set.

Table 1-7 Related Documentation

Title	Document Number
PDP-11/45 Manuals*	
KB11-A, D Central Processor Unit Maintenance Manual	EK-KB11A-MM-004
MS11-A, B, C Memory Systems Maintenance Manual	EK-MS11A-MM-005
FP11-B Floating Point Processor Maintenance Manual	EK-FP11-MM-003
FP11-C Floating Point Processor Maintenance Manual	EK-FP11C-MM-PRE
KT11-C, CD Memory Management Unit Maintenance Manual	EK-KT11C-MM-005
MF11-U/UP Core Memory System Maintenance Manual	EK-MF11U-MM-003
MM11-S, MF11-L, and MF11-LP Core Memory Systems	EK-MM11S-TM-004
Reference Manuals	
PDP-11/04, 05, 10, 35, 40, 45 Processor Handbook, 1975, 76	EB 05138 75 070/20-9 50
PDP-11 Peripherals Handbook, 1975	EB 05117 060/20-90 50

*A set of engineering drawings is provided with each of the components and options in the PDP-11/45, 11/50, 11/55 systems.

DEC drawing numbers are interpreted as indicated in the following example:

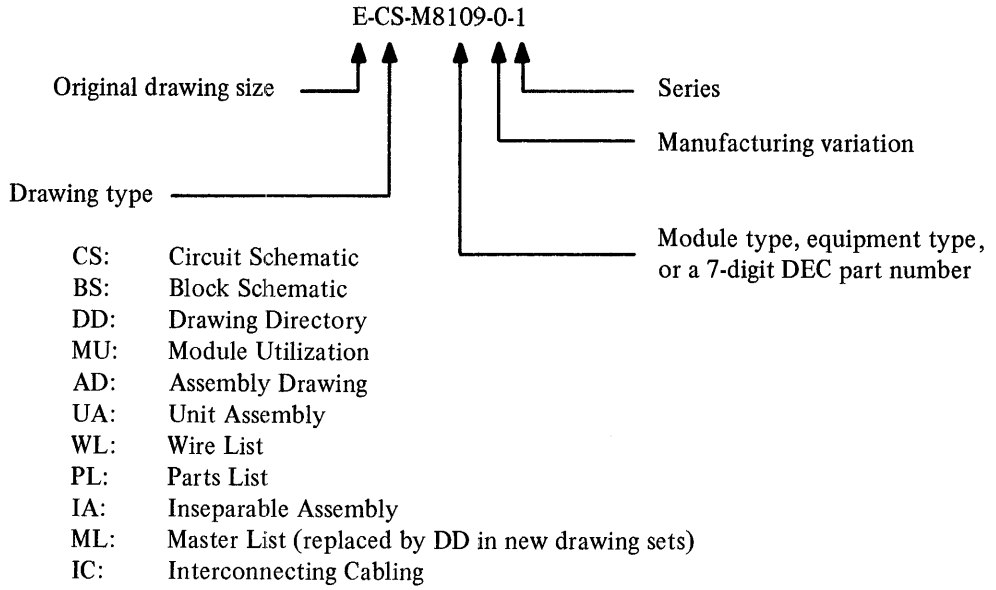


Table 1-8 Reference Drawing Summary

Drawing Number	Title
PDP-11/45 System Engineering Drawings	
B-DD-11/45-0-0	Drawing Directory
D-CS-5409684-0-1	Circuit Schematic – Console Board
D-IC-11/45-0-2	11/45 Back Panel PC Board
KB11-A Central Processor Unit	
B-DD-KB11-A-0	Drawing Directory
E-MU-KB11-A-1	Module Utilization
D-BD-KB11-A-2	Block Diagram
D-FD-KB11-A-3	Flow Diagram
E-CS-M8100-0-1	M8100 DAP Module Schematic
E-CS-M8101-0-1	M8101 GRA Module Schematic
E-CS-M8102-0-1	M8102 IRC Module Schematic
E-CS-M8103-0-1	M8103 RAC Module Schematic
E-CS-M8104-0-1	M8104 PDR Module Schematic
E-CS-M8105-0-1	M8105 TMC Module Schematic
E-CS-M8106-0-1	M8106 UBC Module Schematic
E-CS-M8116-0-1	M8116 SJB Module Schematic
E-CS-M8109-0-1	M8109 TIG Module Schematic
D-IC-KB11-A-BG	Bus Cables and Grant Chain
C-CS-M930-0-1	Circuit Schematic – Bus Terminator
C-CS-M920-0-1	Circuit Schematic – Internal Bus Connector
E-CS-5409910-0-1	Circuit Schematic
E-CS-5409912-0-1	Circuit Schematic
KB11-D Central Processor Unit	
B-DD-KB11-D	Drawing Directory
E-MU-KB11-D-1	Module Utilization
D-IC-KB11-A-BG	Bus Cables and Grant Chain
D-BD-KB11-D-2	Block Diagram
D-FD-KB11-C-1	KB11-C Flow Diagrams
E-CS-M8100-0-1	M8100 DAP Module Schematic
E-CS-M8101-0-1	M8101 GRA Module Schematic
E-CS-M8132-0-1	M8132 IRC Module Schematic
E-CS-M8123-0-1	M8123 RAC Module Schematic
D-CS-M8104-0-1	M8104 PDR Module Schematic
E-CS-M8105-0-1	M8105 TMC Module Schematic
E-CS-M8119-0-1	M8119 UBC Module Schematic
E-CS-M8109-0-1	Timing Generator
D-CS-M8116-0-1	System Jumper Board
C-CS-M930-0-1	Circuit Schematic
C-CS-M920-0-1	Circuit Schematic
E-CS-5409910-0-1	Circuit Schematic
E-CS-5409912-0-1	Circuit Schematic

Table 1-8 Reference Drawing Summary (Cont)

Drawing Number	Title
FP11-B Floating-Point Processor	
B-DD-FP11-B-0	Drawing Directory
E-CS-M8112-0-1	M8112 FRM Module Schematic
E-CS-M8113-0-1	M8113 FXP Module Schematic
E-CS-M8114-0-1	M8114 FRH Module Schematic
E-CS-M8115-0-1	M8115 FRL Module Schematic
D-FD-FP11-B	FP Data Paths and Flow Diagrams
FP11-C Floating-Point Processor	
B-DD-FP11-C-0	Drawing Directory
D-FD-FP11-C-	Flow Diagrams
D-CS-M8126-0-1	M8126 FRH Module Schematic
D-CS-M8127-0-1	M8127 FRL Module Schematic
D-CS-M8128-0-1	M8128 FRM Module Schematic
D-CS-M8129-0-1	M8129 FXP Module Schematic
KT11-C, CD Memory Management Unit	
B-DD-KT11-C-0	Drawing Directory
D-BD-KT11-C-1	Block Diagrams
E-CS-M8107-0-1	M8107 SAP Module Schematic
E-CS-M8108-0-1	M8108 and M8108-YA SSR Module Schematic
MS11-AP Bipolar Memory	
B-DD-MS11-A	Drawing Directory
D-CS-M8121-YA-1	Bipolar Memory Matrix
A-SP-MS11-A-1	MS11-A, C Bipolar Installation Procedure
MS11-B MOS Memory	
B-DD-MS11-B-0	Drawing Directory
D-BD-MS11-0-1	Block Diagram
E-CS-M8110-0-1	M8110 SMC Module Schematic
E-CS-G401-0-1	G401 MOS Memory Matrix Schematic
E-CS-G401-YA-1	G401YA MOS Memory Matrix Schematic with parity
MS11-C Bipolar Memory	
B-DD-MS11-C-0	Drawing Directory
D-BD-MS11-0-1	Block Diagram
E-CS-M8110-0-1	M8110 SMC Module Schematic
E-CS-M8111-0-1	M8111 Bipolar Memory Matrix Schematic
E-CS-M8111-YA-1	M8111YA Bipolar Memory Matrix Schematic with parity

Table 1-8 Reference Drawing Summary (Cont)

Drawing Number	Title
	MF11-U 16K Core Memory
B-DD-MF11-U	Drawing Directory
D-CS-G114-0-1	16K Sense Memory
D-CS-G235-0-1	16K X–Y Drive
D-CS-M8293-0-1	16K Unibus Timing
D-CS-H217-0-1	Memory Stack (16K X 16)
D-MU-MF11-U-MU	Module Utilization
D-TD-MF11-U-1	Timing Diagram
D-CS-5410345-0-1	Backplane
	MF11-LP 8K Core Memory
B-DD-MM11-F-0	Drawing Directory
D-MU-MM11-F-0	Module Utilization
D-CS-G109-0-1	G109 Module Schematic
D-CS-G231-0-1	G231 Module Schematic
D-CS-H215-0-1	H215 8K Memory Matrix Schematic
D-CS-M7259-0-1	M7259 Parity Module Schematic
	KW11-L Line Frequency Clock
A-ML-KW11-L-0	KW11-L Master List
	Power Systems
D-IC-11/45-0-1	Interconnection Diagram
B-DD-H7420-0	H7420 Drawing Directory
D-CS-H7420-0-0	Wiring Diagram
D-CS-5411086-0-1	Power Line Monitor (Regulator)
E-UA-H7420-0-0	H7420 Power Supply
A-PL-H7420-0-0	H7420 Power Supply
B-DD-H742-0	H742 Drawing Directory
D-CS-H742-0-1	H742 Circuit Schematic
C-CS-5409730-0-1	H742 Power Control Board Circuit Schematic
B-DD-H744-0	H744 Drawing Directory
D-CS-H744-0-1	H744 Circuit Schematic
B-DD-H745-0	H745 Drawing Directory
D-CS-H745-0-1	H745 Circuit Schematic
B-DD-H746-0	H746 Drawing Directory
D-CS-H746-0-1	H746 Circuit Schematic
D-CS-H754-0-1	H754 Circuit Schematic
B-DD-860-0	860 Drawing Directory
C-CS-860-0-1	860 Circuit Schematic
C-CS-5409770-0-1	860 Power Control Board
D-CS-861-A-1	861-A Power Control
D-CS-861-B-1	861-B Power Control

Table 1-8 Reference Drawing Summary (Cont)

Drawing Number	Title
DL11-A Asynchronous Line Interface	
B-DD-DL11-0	Drawing Directory
C-UA-DL11-0-1	Asynchronous Line Interface
A-PL-DL11-0-0	Asynchronous Line Interface
E-CS-M7800-YA-11	Asynchronous Line Interface
D-IA-7008360-0-0	Cable, Modem BC05C
A-SL-DL11-0-4	Cable Assembly (KL8/E)
A-AL-DL11-0-5	Modem Test Connector
A-SP-DL11-0-2	Installation Procedure

1.6 DRAWING CONVENTIONS

Figure 1-4 illustrates some of the drawing conventions used on the circuit schematics. Example A defines the meaning of each part of a typical signal mnemonic. Example B provides the following information:

1. CLR SL YEL L, originating on sheet D of the TMC drawing (on which this gate is shown), is asserted when low (0 V).

2. UBCE INIT H is input to TMC module on pin CJ1, as indicated by the arrow. (This pin mates with backplane connector pin C11J1.)

3. The NOR gate is provided by pins 1, 2, and 3 of a type 8885 integrated circuit located at position E24 on the TMC module.

4. TMCC SERF (1) H is the high (+3 V) output of the SERF flip-flop, when the flip-flop is set.

Example C shows the arrows indicating signals that leave the module. TMCE BUST OUT L is output on pin DL1 of the TMC module.

Examples D and E show the flip-flop conventions. Note in D that IRCA IR05 (1) H is the same pin as IRCA IR05 (0) L, and that IRCA IR05 (1) L is the same pin as IRCA IR05 (0) H.

The same type of flip-flop has been re-defined in example E – the D input is inverted; the 1 and 0 outputs are interchanged as are the Set and Reset inputs.

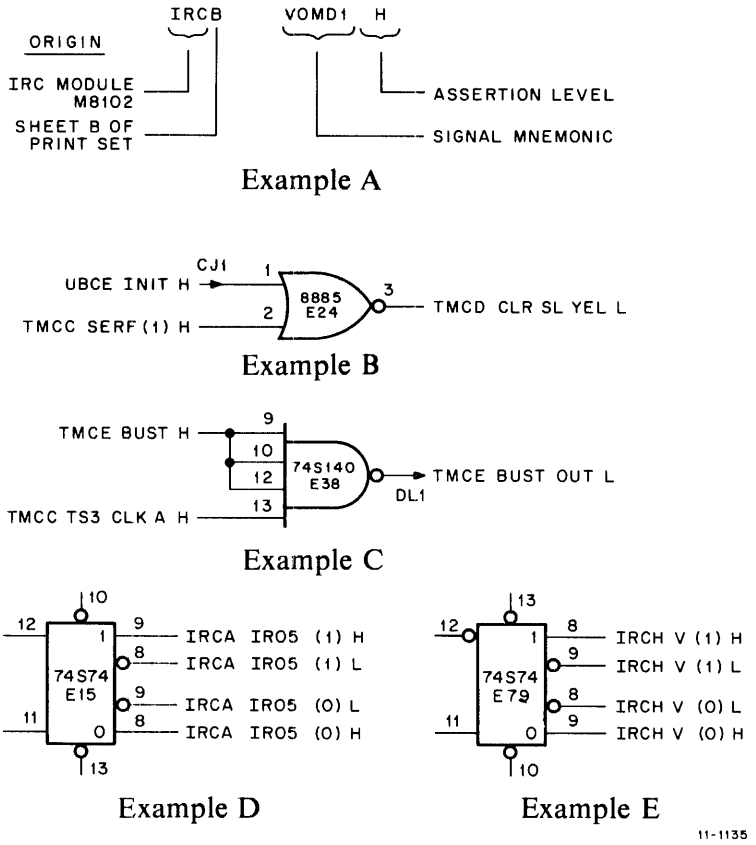


Figure 1-4 PDP-11/45, 11/50, 11/55 Drawing Convention Examples

CHAPTER 2
SYSTEM INSTALLATION

2.1 GENERAL

This chapter contains installation information and recommendations to ensure a successful PDP-11/45 installation. Installation of new options is an existing PDP11/45, 11/50, 11/55 system is described in Chapters 7 and 8 for PC board and system units options.

Customer assistance is provided during site planning, preparation, and installation; the final layout plan should be approved by both the customer and DEC prior to delivery of the equipment.

Planning considerations should include:

- Shipping and access routes; e.g., door, hall, passageway, elevator restrictions, etc.
- Floor plan layout for equipment
- Electrical and environmental considerations
- Fire and safety precautions
- Storage facilities for accessories and supplies

Site preparation is dictated by the customer's requirements and can range from providing the required source power to complete construction or remodeling of the selected installation site. Therefore it is recommended that any and all requirements and restrictions be considered and effected prior to shipment and installation of the equipment.

2.2 SITE PREPARATION

Adequate site planning and preparation simplifies the installation process. DEC Sales and Field Service Engineers are available for consultation and planning with customer representatives regarding objectives, course of action, and progress of the installation. The information in this paragraph is provided primarily to permit review of the site planning; use the *PDP-11/45 Site Configuration Worksheet* to perform the initial site planning.

2.2.1 Physical Dimensions

The overall dimensions and total weight of a particular system – the dimensions, weight of any optional cabinets, cable lengths, and the number of free-standing peripherals – should be known prior to shipment.

The route the equippment is to travel from the customer receiving area to the installation site should be studied; measurements of doors, passageways, etc., should be taken to facilitate delivery of the equipment. All measurements and floor plans should be submitted to the DEC Sales Engineer and Field Service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DEC.

If an elevator is to be used for transferring the PDP-11/45, 11/50, or 11/55 and its related equipments to the installation site, DEC should be notified of the size and gross weight limitations of the elevator so that the equipment can be shipped accordingly.

The site space requirements are determined by the specific system configuration to be installed and, when applicable, provision for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout is helpful. When applicable, space should be provided in the machine room for storing tape reels, printer forms, card files, etc. The integration of the work area with the storage area should be considered in relation to the work flow requirements between areas.

In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room.

Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights, and cable lengths of freestanding peripheral equipment must be known prior to installation – preferably during site preparation and planning. The computer peripherals must not be located at distances where connecting cables exceed maximum limits. The following points should be considered when planning the system layout:

1. Ease of visual observation of input/output devices by operating personnel.

2. Adequate work area for installing tapes, access to console, etc.

3. Space availability for contemplated future expansion.

4. Proximity of the cabinets and peripherals to any humidity-controlling or air-conditioning equipment.

5. Adequate access to equipment (e.g., rear door, etc.) for service personnel.

The final layout will be reviewed by the DEC Sales Engineer, Field Service, and in-house engineering personnel to ensure that cable limitations have not been exceeded and that proper clearances have been maintained.

2.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented to aid the customer in maintaining an installation that affords adequate operational safeguards for personnel and system components.

1. If an overhead sprinkler system is used, a *dry pipe* system is recommended. Upon detection of a fire, this system removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

2. If the fire detection system is the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.

3. If an automatic carbon dioxide fire protection system is used, an alarm should sound prior to release of the CO_2 to warn personnel within the installation.

4. If power connections are made beneath the floor of a raised-floor installation, waterproof electrical receptacles and connections should be used.

5. An adequate earth ground connection should be provided to protect operating personnel.

2.2.3 Environmental Requirements

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

2.2.3.1 Humidity and Temperature – The PDP-11/45, 11/50, and 11/55 electronics are designed to operate in a temperature range of from 50° F (10° C) to 110° F (40° C) at a relative humidity of 10 to 90 percent with no condensation. However, system configurations that use input/output devices such as magnetic tape units, card readers, etc., may require closer control of the environment. See Appendix C for detailed specifications. Nominal operating conditions for a typical system configuration are a temperature of 70° F (20° C) and a relative humidity of 45 percent with no condensation. (For operation above sea level, see Paragraph 1.1.7)

2.2.3.2 Air Conditioning – When used, computer room air-conditioning equipment should conform to the requirements of the "Standard for the Installation of Air Conditioning and Ventilating Systems (non-residential)," N.F.P.A. No. 90A, as well as the requirements of the *Standard for Electronic Computer Systems,* N.F.P.A. No. 75. Remember, air flow in a PDP-11 is from top to bottom of cabinets.

2.2.3.3 Acoustical Damping – Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise-level devices, an acoustically damped ceiling will reduce the noise.

2.2.3.4 Lighting – If CRT peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to conveniently observe the display.

2.2.3.5 Special Mounting Conditions – If the system will be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard ship), the cabinetry should be securely anchored to the installation floor by mounting bolts. Since such installations require modifications to the cabinets, DEC must be notified when the order is placed so that the necessary modifications can be made.

2.2.3.6 Static Electricity – Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the PDP-11/45, 11/50, 11/55 and related peripheral equipments. If carpeting is installed on the computer floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

2.2.4 Electrical Requirements

The PDP-11/45, 11/50, 11/55 operates from a nominal 115 V, 50/60 Hz or 230 V, 50/60 Hz, ac power source. The primary ac operational voltages should be maintained within the tolerances defined in Paragraph 1.1.2 and in Chapter 4.

For certain options that use synchronous motors, line voltage tolerance should be maintained within ±15 percent of the nominal values, and the 50/60 Hz line frequency should not vary more than ±2 Hz.

Primary power to the system should be provided on a line separate from lighting, air-conditioning, etc., so that computer operation will not be affected by voltage transients. The wiring should conform to the following general guidelines:

1. All electrical wiring must conform with the National Electric Code (NEC).

2. The ground terminal on the receptacle will normally have a green colored screw; the neutral terminal will be white or silver colored; and the "hot" terminals will be brass colored.

3. Under the NEC (in the U.S. only), the color coding for the neutral wire is either white or gray, and the ground wire is solid green, green with one or more yellow stripes, or bare. There are no specified colors for the "hot" wires.

The PDP-11/45, 11/50, 11/55 cabinet grounding point should be connected to the building power transformer ground or the building ground point. Direct any questions regarding power requirements and installation wiring to the local DEC Field Service Engineer.

Chapter 4 contains a detailed description of the ac power system and includes a list of connectors and plugs used.

2.3 INSTALLATION AND INSPECTION

CAUTION
Do not attempt to install the system until DEC has been notified and a DEC Field Service Representative is present.

The procedures in Paragraphs 2.3.1 through 2.3.5 are provided to assist in receipt, unpacking, inspection, and installation of the PDP-11/45, 11/50, 11/55, and associated peripherals and equipments. Paragraphs 2.4 and 2.5 describe the procedures recommended for bringing the system up.

2.3.1 Unpacking

Before unpacking the equipment, check the shipment against the packing list provided. Check that the correct number of packages has been delivered and that each package contains all the items listed on the accompanying packing slip. Also, check that all items on the accessories list in the Customer Acceptance Procedures have been included in the shipment. Unpack the cabinets as follows:

1. Remove outer shipping container.
2. Remove the polyethylene cover from the cabinets.
3. Remove the tape or plastic shipping pins from the cabinet(s) rear access door(s).
4. Unbolt cabinet(s) from the shipping skid as follows: to remove shipping bolt from right side of cabinet.
    a. Remove the shipping bracket. Pull CPU mounting box out to locked position and remove side panels from cabinet.
    b. Remove nut and washer from the underside of the shipping skid.
    c. There are three 10-32 screws attaching the lower power supply to the front upright of the cabinet; loosen these three screws (no more than three turns).
    d. At the rear of the lower power supply are three additional screws. Remove these completely and swing the power supply toward the middle of the cabinet 1 to 1-1/2 in. Holding the power supply, remove the shipping bolt by pulling straight up.
    e. Swing the power supply back to the original position, replace the rear screws and tighten the front screws.
5. Raise the leveling feet so that they are above the level of the roll-around casters.

6. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

7. Roll the system to the proper location for installation.

8. If necessary, repeat steps 1 through 7 for the expansion cabinets. When the cabinets are properly oriented, follow the procedure of Paragraph 2.3.3 to install the cabinets(s).

2.3.2 Inspection

After removing the equipment packing material, inspect the equipment and report any damage to the local DEC sales office. Inspect as follows:

1. Inspect external surface of the cabinets and related equipments for surface, bezel, switch, light damage, etc.

2. Open the rear door of the cabinet, and internally inspect the cabinet for console, processor, and interconnecting cable damage; loose mounting rails; loose or broken modules; blower or fan damage; any loose nuts, bolts, screws, etc.

3. Inspect the wiring side of the logic panels for bent pins, broken wires, loose external components, and foreign material.

4. Inspect the power supply for proper seating of fuses and power connections.

5. Inspect all peripheral equipment – including magnetic tape and DECtape transport heads, motors, paper-tape sprockets, etc. – for internal and external damage.

CAUTION

Do not operate any peripheral device that employs motors, tape heads, sprockets, etc., if these items appear to be damaged.

2.3.3 Cabinet Installation

The cabinets are provided with roll-around casters and adjustable leveling feet so it is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). In multiple cabinet installations, receiving restrictions may require that cabinets be shipped individually or in pairs. In such cases, the cabinets are connected at the installation site. Cabinet installation procedures are as follows:

1. With the cabinets positioned in the room, install H952-GA filler strips between cabinet groups (filler strips are shipped attached to the end of a cabinet group). Remove four bolts each from the front and rear filler strips. Butt the cabinet groups together while holding the filler strips in place and rebolt through both cabinets and the filler strips (drawing C-UA-H952-G-0). Do not tighten the bolts securely at this time.

2. Lower the leveling feet so that the cabinets are not resting on the roll-around casters but are supported on the leveling feet.

3. Tighten the bolts that secure the cabinet groups together. Ensure that all leveling feet are planted firmly on the floor.

4. Electrical connections, including intercabinet ground strapping, are described in Paragraphs 2.3.4 and 2.3.5.

2.3.4 AC Power Connections

Paragraph 2.2.4 and Chapter 4 define the electrical requirements and the ac power outlets required at the site. Early systems include two 860 power controls as shown in Figure 1-2. Current versions are equipped with a single 861 power control as shown in Figure 1-1. Most of the additional cabinets in a system include a power control and ac connector that are similar to that supplied in the basic CPU cabinet. All ac power is distributed from the power control to the appropriate power supplies within the cabinet.

The power controls in all cabinets are connected to provide central control of power turn-on and turn-off from the CPU console POWER switch. Before connecting any power cables to the site source power, check all building wiring. Ensure that power receptacles of the appropriate types have been provided for each cabinet and that the receptacles are positioned close enough to the cabinet positions to allow the cables to be connected without stretching or crossing the cables. In particular, check that the phase and neutral wires have been connected to the same pins in each receptacle.

2.3.5 Intercabinet Connections

When a multi-cabinet system is assembled, three types of electrical connections must be made between cabinets (refer to Paragraph 2.3.3 for mechanical connections). These connections are:

1. Unibus connections – A BC11-A cable must connect the last system unit in a cabinet to the first system unit in the next cabinet.

2. Remote power connections – All cabinet power controls are connected to a control bus that provides for system turn-on and turn-off.

3. Ground strapping – The frame ground of the system is distributed through the cabinets by direct electrical connections between the cabinet frames.

2.3.5.1 Unibus Connections – The BC11-A Unibus cable is the I/O bus that connects all system components. To connect the Unibus between the CPU cabinet and an expansion cabinet, insert the BC11-A cable in the rear system unit slot of the mounting box of the CPU cabinet. The cable runs through a cable clamp in the upper left corner at the rear of the CPU mounting box and passes under the power supply mounting rails into the next cabinet. In the expansion cabinet, the cable passes through a similar cable clamp and is inserted in the appropriate slot of the first system unit of the mounting box.

2.3.5.2 Remote Power Connections – The power controls in all cabinets must be interconnected to ensure common power turn-on and turn-off. Detailed cabling instructions are provided in Paragraph 4.2 of this manual.

2.3.5.3 Ground Strapping – Electrical safety is provided by connecting all the cabinet frames to the ground level of the site power system. This is accomplished by connecting a wire in each power cable between the frame and the power system ground; this is not a load-carrying wire – it is intended only as an emergency ground path. The green wire in each power cable is the frame ground, while the white wire is the neutral, or return wire, that carries the load current.

To improve the level of safety provided by the frame ground connections, all cabinet frames are connected by braided copper straps or No. 4 AWG solid wire with crimp-on lugs which are fastened to copper studs that are welded to the frames (this also prevents the generation of ground loops between cabinets that are connected by signal-carrying cables). The studs are welded to the bottom side rails of the cabinet frame, facing inward; the stud on the left side of the cabinet is slightly forward of center while the stud on the right side is slightly to the rear.

The ground strap supplied with each cabinet is fastened to one stud, passed over the side rail of that cabinet and the side rail of the adjacent cabinet, and fastened to the stud in that cabinet. The copper studs are threaded and nuts are supplied on the studs.

Similar strap/stud grounding is used to ground the H7420 power supplies to the cabinet frame.

2.3.5.4 Wire Trough Cabling – An optional wire trough system can be installed which provides cable organization that improves the appearance of the system's cabling and helps reduce cable damage. Device location in the CPU cabinet and expansion cabinet determines required cable lengths and trough configuration. For planning and installation procedures, refer to the *Wire Trough Installation Manual* (EK-WIRET-IN-001).

2.4 INITIAL POWER TURN-ON

CAUTION

The following checks and those in Paragraph 2.5 should be performed as part of the initial system installation checkout procedures.

Inspect the CPU backplane assembly for bent connector pins, loose wires, imperfections in the dc power distribution board etch, or any other physical defects that can be observed. Correct any problems discovered.

With the power off, check the power distribution system to determine if any short-circuits to ground exist. Refer to power supply dc distribution charts in Chapter 5 of this manual for circuit and connector information.

Check the dc power system as described below. Figures 5-1A, B, and C show the power distribution harness for newer systems (CPU cabinet serial numbers 2000 and higher, H960D cabinets and higher) while Figure 5-2 shows the same for older systems. Paragraph 3.3 defines old and new systems.

1. Unplug the ac power cables. Disconnect the following Mate-N-Lok plugs:

New Harness	Old Harness
P2–P13	P2–P13
P17–P21	P17–P21
P25–P31	P25–P31
P36, P37, P40	

   P1, P14–P16, P22–P24 and P32–P35 remain connected in all cabinets.

2. Turn off the circuit breakers on all the 860 or 861 power controls. The console switch must be on or the LOCAL/REMOTE switch on the power control must be set to LOCAL to check the ac voltages on the upper supply.

3. Plug in the ac power cable(s), turn on the circuit breaker(s), and check the 20–30 Vac generated by the H7420 power supplies. These voltages can be checked at the pins of plugs P17 through P21, P25 through P31 (also P40 in newer systems). Table 5-2 provides specific pin numbers.

4. Turn off the circuit breakers and connect plugs P17 through P21, P25 through P31 (and P40 if applicable).

5. Turn the circuit breakers on and check the dc voltages generated by the regulators. Note that not all regulators need be present. The voltages should be checked on the following connectors (P8 through P11 are ground returns for these voltages):

New Harness	Old Harness
P2–P7	P2–P7
P12	P12 & P13
P36 & P37	P36

Table 5-2 provides specific pin numbers.

If a regulator shows no output, turn off the circuit breakers, lower the voltage adjustment for this regulator, then reapply power and check again (the regulator may have crowbarred due to overvoltage).

6. Turn the circuit breakers off and plug in the remaining connectors.

7. Turn the power on and check the voltages at the points listed in Table 6-2. Adjust if necessary.

8. Verify correct operation of the console power switch. Refer to Table 6-1 of the *KB11-A, D Central Processor Unit Maintenance Manual.*

9. Check the operation of all fans.

10. Refer to Paragraph 2.5 for an initial test procedure of the KB11-A, D, which should be performed after this initial power turn-on procedure.

2.5 SYSTEM CONFIGURATION TEST PROCEDURES

The test procedures require the following basic PDP-11/45, 11/50, 11/55 system components:

1. KB11-A or KB11-D Central Processor Unit, with console and power supplies, installed in cabinet.

2. Magnetic core memory with Unibus connection to KB11-A, D or MS11 Semiconductor Memory System installed in the CPU backplane assembly.

3. M8116 SJB module or KT11-C, CD option (M8107 SAP module and the SSR module – M8108 in the KT11-C, M8108-YA in the KT11-CD).

2.5.1 Special Test Equipment

The following special test equipment is required:

1. Maintenance card with W130 or W133 driver module. Use of the maintenance card is described in Paragraph 6.5.

2. Tektronix model 454 oscilloscope, or equivalent, is preferred; however, Tektronix model 453, or equivalent, is adequate for most tests.

2.5.2 Preliminary Checks

The following procedures are recommended as preliminary precautions when installing a PDP-11/45, 11/50, 11/55.

1. Check the power supplies as detailed in Paragraph 2.4.

2. Turn the power supplies off. Refer to the module location drawing to either install, or check for proper installation of all required modules. These include:

   a. The KB11-A or KB11-D module complement and console connectors.

   b. The M8116 SJB module or the KT11-C, CD modules (M8107 and M8108 in the KT11-C, or M8107 and M8108-YA in the KT11-CD).

   c. The Unibus A cable connector to the magnetic core memory or the MS11 modules.

3. If a problem is detected, install the maintenance and driver cards. Install the W130 driver module in slot 1, row F, on the CPU backplane. If dual driver module W133 is used, install it in slot 1, rows E and F. The maintenance card plugs into the driver module connector associated with row F for KB11-A, D test purposes.

2.5.3 Detailed Procedure

The following test proceudre is used to verify the correct operation of sufficient logic elements in the KB11-A, D to enable the initial KB11-A, D diagnostic programs to be executed. The sequence of these tests leads to the ultimate execution of an unconditional branch instruction, which is the first instruction tested by the diagnostic programs.

The logic elements are checked in small groups. Each step uses only previously tested logic elements to perform tests on additional logic elements. Test results only verify that the logic under test is operating; they do not test speed or quality of performance.

NOTE

Use the KB11-A, D block diagrams shown in the *KB11-A, D Central Processor Unit Maintenance Manual,* Chapter 4, Figure 4-1 and 4-4, as an aid to visualize which groups of logic elements are being verified by each test.

2.5.3.1 RC Maintenance and Crystal Clock Test

1. Install the maintenance card and set CLK switch S3 to RC.

2. Turn the power supplies on and use the console key switch to apply power to the KB11-A, D.

3. Connect oscilloscope to observe TIGA TPH MAT H clock output at pin FU1 of slot 15.

4. Adjust potentiometer R104 on the TIG module (RC clock adjustment) to produce a 60 ns period for each complete TIGA TPH MAT H clock pulse. This ensures a 300 ns machine state made up of five 60 ns time states.

5. Set maintenance card CLK switch S3 to XTAL and observe that the crystal clock is operating properly.

2.5.3.2 Microprogram ROM Cycle Test

1. Turn power off.
2. Set console ENABL/HALT switch to HALT.
3. Turn power on.
4. Set DATA display select switch to μADRS FPP/CPU. Verify that the CPU ROM address is 170_8. This is displayed in the low-order byte of the DATA display.

When the correct DATA display is observed, proper operation of the following processor logic elements is verified:

1. The ROM microaddress (UADR) logic
2. One microprogram branch (console)
3. The microprogram ROM and buffer (drawing RACA through RACD)
4. Part of the display multiplexer (low byte drawing PDRF)
5. Part of the console DATA indicator lamps (drawing KNLA)

2.5.3.3 Single Time Start Test

1. Set maintenance card switches S1 and S2 to 2 to select SING TP operation.
2. Press console START switch. The DATA display should display microprogram ROM address 200_8 in the low byte indicators.

This test provides additional checks of the ROM microaddress (UADR) logic, the display multiplexer, and the DATA display indicator lamps.

2.5.3.4 Single Time Step Test

1. Press maintenance card MAINT STPR switch to produce time pulses.
2. Note that each time the MAINT STPR switch is pressed, the TPH indicator changes state.
3. Verify that the μADRS changes at T3, and the processor sequences through several machine states. Maintenance card indicators T1 through T5 will light in sequence, progressing from T1 through T5 each time TPH goes off.
4. Verify that after several machine states, the μADRS becomes 170_8. After arriving at 170_8, the processor continues to cycle through that machine state.

When correct results are observed for this test, the microprogram branch and microprogram address logic is further verified.

2.5.3.5 Switch Register and Display Test

1. Reset the maintenance card switches S1 and S2 to 0 and advance the MAINT STPR switch to allow normal timing cycles.

2. Set the DATA display select switch to BUS REGISTER.

3. Set the console switch register for various switch inputs to test all switches and DATA display indicators.

When this test is successfully completed, all parts of the console DATA display, the display multiplexer, and data inputs from the switch register are verified for proper operation. When correct test results are obtained for all tests up to this point, the following logic elements are operating properly:

1. Console switch register

2. Basic microprogram control and address logic

3. Processor timing circuits

4. Part of the bus register multiplexer (BRMX), bus register (BRA), and part of the display multiplexer, all located on M8104 PDR module

2.5.3.6 Internal Data Transfer Test – The following test is the initial data path test; it involves transferring data from the switch register to one of the general registers.

1. Set maintenance card switch S1 to 0 and S2 to 1 to select ROM CYCL operation.

2. Set the console ADDRESS display select switch to CONS PHY.

3. Set up various address selections on the console switches and press LOAD ADRS for each selection.

4. Observe that the ADDRESS display corresponds to the address selected.

When correct test results are observed, proper operation of the following parts of the processor is verified:

1. The A multiplexer (AMX) (passing the BR input without error)

2. The ALU (passing the A input without error)

3. The shifter (SHFR) (passing the data without error)

4. The source register (SR)

5. The bus address multiplexer (BAMX) (passing the BR input)

6. The console ADDRESS display indicator lights

2.5.3.7 Register Deposit/Examine Test

KB11-A Test:

1. Set the console ADDRESS display select switch to CONS PHY and set the DATA display select switch to DATA PATHS.
2. Set switches to all 0s.
3. Press LOAD ADRS.
4. Press REG DEP.
5. Increment the switch register by 1, by setting the switches accordingly.
6. Repeat steps 3, 4, and 5 for successive values from 0_8 through 17_8. (Register 0 contains 0, register 1 contains 1, etc.)
7. Load address 0 and press REG EXAM. Observe that the DATA display indicates the contents of Register 0 are 0s.
8. Increment switch register contents by 1 and press LOAD ADRS.
9. Press REG EXAM.
10. Continue to examine the contents of each register by repeating steps 8 and 9 to determine if the correct data was deposited during steps 2 through 6.

NOTE

If a register has the number of some other register in it, the address logic is probably at fault. If the numbers in the register have any bits other than the four least-significant bits set, the register storage elements are probably the cause of the trouble.

11. As a further test, deposit other switch register data into the general register to ensure that all bits are stored and displayed correctly.

KB11-D Test:

1. Set the console ADDRESS display select switch to CONS PHY and set the DATA display select switch to DATA PATHS.
2. Set switches to all 0s.
3. Press LOAD ADRS.
4. Press REG DEP.
5. Increment the switch register by 1, by setting the switches accordingly.

6. Repeat steps 3, 4, and 5 for successive values from 0_8 through 17_8. (Register 0 contains 0, register 1 contains 1, etc.)

7. Load address 0 and press REG EXAM. Observe that the DATA display indicates the contents of Register 0 are 0s.

8. Continue to examine the contents of each register by consecutively pressing REG EXAM to determine if the correct data was deposited during steps 2 through 6. (Each consecutive REG EXAM automatically steps the address.)

NOTE

If a register has the number of some other register in it, the address logic is probably at fault. If the numbers in the register have any bits other than the four least-significant bits set, the register storage elements are probably the cause of the trouble.

9. As a further test, deposit other switch register data into the general registers to ensure that all bits are stored and displayed correctly.

When the test results are correct, the following parts of the KB11-A,D processor have been verified for proper operation:

1. The general destination (GD) register (drawings GRAD through GRAH)

2. The destination register multiplexer (DRMX) (drawings GRAD through GRAH)

3. The destination register (DR) (drawings GRAD through GRAH)

4. The program counter registers (PCA and PCB) (drawings DAPF and DAPH) if register 07_8 is deposited and examined

2.5.3.8 I/O Data Transfer Test – The tests performed up to this point have verified that the processor can transfer data to an external location.

1. Set the console switches to an address within the range assigned to the available memory (either Unibus memory or MS11 Semiconductor Memory System).

2. Press LOAD ADRS.

3. Set ENABL/HALT switch to HALT.

4. Set various data into the switch register and perform alternate DEP and EXAM functions. With the DATA display select switch set to DATA PATHS, the DATA displayed by the deposit should match the DATA displayed by the EXAM for each test.

5. After checking the DATA display for each test switch the DATA display select to μADRS FPP/CPU and observe that the processor returns to ROM state CON.00 (ROM address 170_8) after each DEP and EXAM is performed.

When the correct test results are observed, the following parts of the processor are verified to be operating properly:

1. The Unibus (or semiconductor memory) control logic on the UBC module (M8106 in the KB11-A, M8119 in the KB11-D).

2. The data multiplexer (DMX), passing the BR inputs without error (drawing PDRE).

3. The BRMX Unibus inputs (drawing PDRA) and the BAMX PCB inputs (drawings DAPB, DAPC, and DAPD).

4. Additional timing pulse logic on the M8109 TIG module.

If the deposit and examine tests are unsuccessful, the problem is probably in the external data transfer operation. To further isolate the cause of malfunction, perform either the Unibus test outlined in Paragraph 2.5.3.9 or the Fastbus test outlined in Paragraph 2.5.3.10.

2.5.3.9 Unibus Test

1. Set maintenance card switches S1 and S2 to 1 to select SING TP operation. Center CLK switch S3 for single time pulse operation.

2. Repeat Step 4 of the I/O data transfer test (Paragraph 2.5.3.8).

3. Press the MAINT STPR switch to perform the deposit and examine functions in single time steps.

Look for the following normal indications:

1. Step through time states until the maintenance card BBSY indicator lights.

2. Several more time states should elapse before the MSYN indicator lights. If not, ground MSYN SET H at pin E12 U1 on the UBC module and repeat step to see if MSYN ever lights.

3. The SSYN indicator should appear to light simultaneously with MSYN.

4. There should be several clock ticks before the MSYN and SSYN indicators go off.

5. There should be several more clock ticks before the BBSY indicator goes off.

NOTE

Data transferred into the processor during the examine function should appear in the BR at the end of ROM cycle at μADRS 153_8. Set DATA display select switch to BUS REGISTER. The input data should be located in the DR at the end of ROM cycle at μADRS 137_8. Set DATA display select switch to DATA PATHS.

2.5.3.10 Fastbus Test – Use the same test procedure as described for the Unibus test (Paragraph 2.5.3.9). Look for the following normal Fastbus indications:

1. The BBSY indicator lights.
2. Several more time states should elapse before the MEM indicator lights.
3. The CNTL OK and T3 indicators should appear to light simultaneously.

2.5.3.11 ALU Arithmetic Test

1. Select an address and deposit data into that location.
2. Press DEP again several times to deposit the data into several successive word locations.
3. Load the original address and press EXAM several times to determine that the data was stored in the several successive locations.

When correct test results are observed, the following parts of the processor are verified to be operating properly:

1. The constant multiplexer KOMX (drawing DAPD).
2. The B multiplexer (BMX) (drawing DAPB, DAPC, and DAPD).
3. The ALU arithmetic function A plus B (drawing DAPF and DAPH).

2.5.3.12 Unconditional Branch Test

1. Deposit a branch instruction (000777_8) in a memory location.
2. Load the address of the instruction.
3. Set maintenance card switches S1 and S2 to select ROM CYCL operation.
4. Set ENABL/HALT switch to ENABL.
5. Press START.
6. Use the MAINT STPR to step the processor through single machine states as indicated by the μADRS FPP/CPU DATA display. Look for the following events:
   a. The processor should enter the RES.00 machine state at μADRS 015 after executing machine states 200, 154, 170, and 176.
   b. The processor should cycle through the RES.20 state at μADRS 374 at least twice. If this does not occur, the microprogram branch has failed and the processor cannot execute instructions at full speed.
   c. The processor should enter the IRD.00 state at μADRS 343 with the correct data in the BR.

7. Set DATA display select switch to BUS REGISTER to check for the correct data (000777_8).

8. Press the MAINT STPR. The next μADRS indication should be 326, which is the BXX.02 machine state.

NOTE

When the correct test results are observed, the processor fork A logic is operating properly. Once this test has been successfully completed, reset maintenance card switches S1 and S2 for normal operation and repeat the test, allowing the processor to loop through the branch instruction. If it does, the offset is being computed properly.

9. While the processor continues to loop through the BR instruction, press the HALT switch. The processor should halt in the CON.00 state at μADRS 170. If it does not, check the processor in single ROM cycle mode to determine that the BRQ branch during instruction fetch works and that the trap sequence ends in the console state.

2.5.3.13 Register-to-Register Data Move Test

1. Load address 000002_8 and press REG DEP to deposit data into general register 2.

2. Deposit a MOV R2, R3 instruction (010203_8) into a memory location, followed by BR.4 instruction (000776_8).

3. Load the address of the MOV instruction.

4. Set maintenance card switches S1 and S2 for ROM CYCL operation.

5. Press START and then step through the MOV instruction that moves data from R2 to R3.

6. Upon completion of the instruction, press HALT and check the contents of general register R3 for correct data (000002_8).

When the correct test results are observed, this test verifies that the fork A and BRQ branch logic are operating properly.

2.5.3.14 Move-Immediate-to-Register Test

1. Deposit a move-immediate-to-R0 instruction in memory, followed by a HALT instruction, as follows:

Address	Contents	Symbolic
X	012700	MOV # 77, R0
X + 2	000077	
X + 4	000000	HLT

2. Set DATA display select switch to DATA PATHS.

3. Execute the sequence deposited in Step 1. The immediate data, 77_8, should be displayed.

When the correct result is observed, the processor fork C logic has been verified to be operating properly.

NOTE

The preceding tests check all the KB11-A, D logic required to load and execute the initial diagnostic program. When the correct test results have been observed, load the diagnostic programs as described in Chapter 6 of the *KB11-A, D Central Processor Unit Maintenance Manual.* These programs provide a complete check of all KB11-A, D operations and are listed in Chapter 6 of this manual. Run each diagnostic as described in the related MAINDEC program description.

2.6 CUSTOMER ACCEPTANCE

Verify correct system operation by performing the Customer Acceptance Procedures. The Customer Acceptance Procedure document is shipped with the system, and lists all the tools, programs, and tests required to certify correct operation.

A properly running system must be able to execute the system diagnostic program successfully without error. These programs are loaded and run according to procedures described in the related Customer Acceptance Procedure.

CHAPTER 3
POWER SYSTEM

This chapter describes the several versions of power distribution, both ac and dc, in the CPU cabinet. The ac power system is described in Chapter 4, the dc power system in Chapter 5, and expansion cabinet power in Chapter 8.

3.1 OVERALL SYSTEM DESCRIPTION

Figure 3-1 is a block diagram of the CPU cabinet power system. The basic components are two H7420 power supplies and their associated power control(s). AC power from the building mains is fed to the power control unit(s), which provides two sets of ac outlets: one switched, the other unswitched. Two H7420 power supplies are provided in the CPU cabinet; one is plugged into the switched power control outlet, the other is plugged into the unswitched power control outlet. These H7420 power supplies are designated *upper* and *lower* according to their mounting location in the cabinet (refer to Figures 1-1 and 1-2). Each H7420 contains a complement of voltage regulators, which depend upon the system configuration.

The power system block diagram shows a typical complement of voltage regulators installed in the appropriate slots of the upper and lower H7420 power supplies (Figure 3-1). Some voltage regulators are supplied with the basic system and others are supplied as part of system options. The voltage regulator complement for the basic system and options is summarized in Tables 3-1 and 3-2. Circuit descriptions of each voltage regulator type are provided in Paragraph 5.2

The primary purpose of the switched supply is to provide dc power to the KB11-A, D and to the options, other than semiconductor memory, that are installed in the CPU mounting box. The lower H7420 subsystem (except for the H745 –15 Vdc regulator in slot F) is unswitched because it must remain on at all times during normal operation to provide dc power to the optional MS11 Semiconductor Memory System, plus ac power to the logic fans and cabinet fans. The power supplied to these components must not be inadvertently switched off because

1. If the power is switched off, the semiconductor memory contents are lost.

2. Other Unibus devices, or another processor, may be accessing the MOS or bipolar memories. Core memory is shut off (–15 V) via +15 V from the upper supply.

3. Fan voltage is required for cooling semiconductor memories.

3.2 115 Vac AND 230 Vac MODELS

The PDP-11/45, 11/50, 11/55 power system operates with 115 Vac or 230 Vac primary source power inputs. The 861-A (CPU cabinet) or -C (expansion cabinet) or the 860-A power controls are used with 115 Vac source power and the 861-B or 860-B power controls are used with 230 Vac source power. The differences between the power controls are described in Chapter 4. The H742-A or H7420-A power supply is used with the 115 Vac source and the H742-B or H7420-B power supply is used with the 230 Vac source. Appropriate jumper connections are made at its primary input for operation on 115 or 230 Vac input power, as shown on drawing No. D-CS-H742-0-1, sheet 1, or D-CS-H7420-0-1, sheet 1.

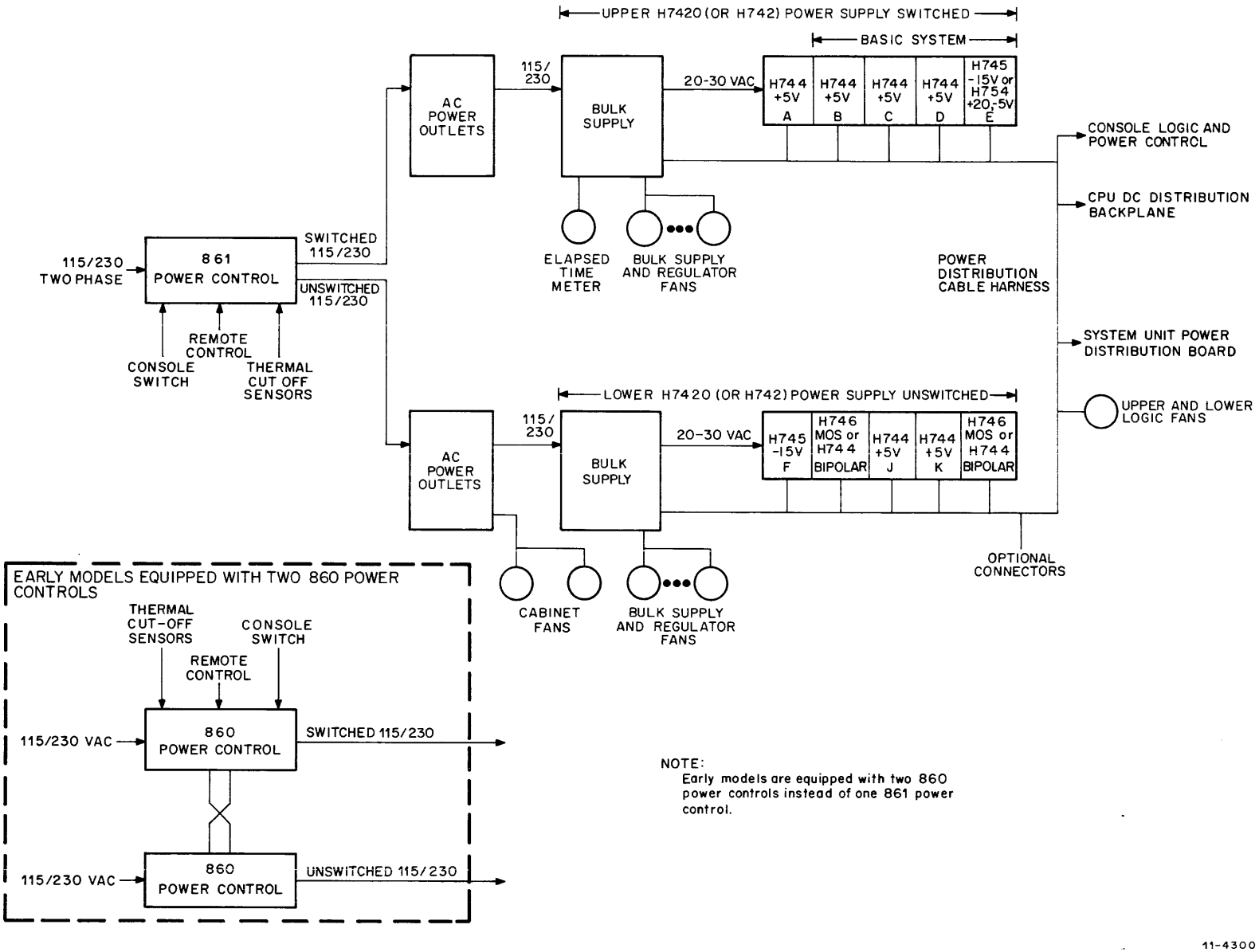


Figure 3-1 Typical PDP-11/45, 11/50, 11/55 Power System

Table 3-1 Voltage Regulator Configuration Data CPU Cabinet Serial Numbers 2000 and Higher

Type	Name	Quantity	Location	Comments
			Basic System	
H744	+5 V Regulator	3	B	+5 V to CPU modules slots 6–9.
			C	+5 V to CPU and KT11-C, CD modules, slots 10–15.
			D	+5 V to internal options, slots 26–28, systems units 1, 2, and 3, and Console.
H745	-15 V Regulator	1	F	-15 V to CPU and internal option modules and to system until 1, 2, and 3, if slot E regulator is a H754. This supply is switched, even though in the lower H742, because it is fed by +15 Vdc from the upper H742.
			FP11-B, C Floating-Point Processor	
H744	+5 V Regulator	1	A	+5 V to FP11 modules, slots 2–5.
			MS11-A, C Bipolar Memory	
H744	+5 V Regulator	2	H	+5 V to control and first two matrix modules (slots 16–18).
			J	+5 V to third and fourth matrix modules (slots 19–20).
		2	K	+5 V to control and first two matrix modules (slots 21–23).
			L	+5 V to third and fourth matrix modules (slots 24–25).
			MS11-B MOS Memory	
H744	+5 V Regulator	1	J	+5 V to control and matrix modules, slots 16–25.
H746	MOS Regulator	2	H, L	+19.7 V, +23.2 V, and -5 V to MOS matrix modules; H slots 17–20; L slots 22–25.
			MM11 Core Memories and Controls	
H745	-15 V Regulator	1	E	-15 V to Systems Units 1–3 (if MF11-UP is not installed).
H754	+20, -5 V Regulator	1	E	+20 and -5 Vdc to MF11-U/UP.

Table 3-2 Voltage Regulator Configuration Data CPU Cabinet Serial Numbers Less Than 2000

Type	Name	Quantity	Location	Comments
		Basic System		
H744	+5 V Regulator	3	B	+5 V to CPU modules, slots 6–9.
			C	+5 V to CPU and KT11-C, CD modules, slots 10–15.
			D	+5 V to internal options, slots 26–28, system units 1, 2, and 3, and Console.
H745	-15 V Regulator	1	E	-15 V to CPU and internal option modules and system units 1 and 2.
		FP11-B, C Floating-Point Processor		
H744	+5 V Regulator	1	A	+5 V to FP11 modules, slots 2–5.
		MS11-A, C Bipolar Memory		
H744	+5 V Regulator	2	H, J	+5 V to control and matrix modules if no MOS memory is installed, or only 4K is used. H: slots 16–18; J: slots 19–20.
		2	K, L	If MOS memory is also installed, or if more than 4K of bipolar is used. K: slots 21–23, L: slots 24–25.
		MS11-B MOS Memory		
H744	+5 V Regulator	1	J	+5 V to control and matrix modules, slots 16–25.
H746	MOS Regulator	2	H, L	+19.7 V, +23.2 V, and -5 V to MOS matrix modules; H slots 17–20; L slots 22–25.
		MM11 Core Memories and Controls		
H745	-15 V Regulator	1	F	-15 V to System Unit 3. H745 provided in basic system supplies System Units 1 and 2. This supply is switched even though in the lower H7420, because it is fed by +15 Vdc from the upper H7420.

3.3 DIFFERENT POWER SYSTEM VERSIONS

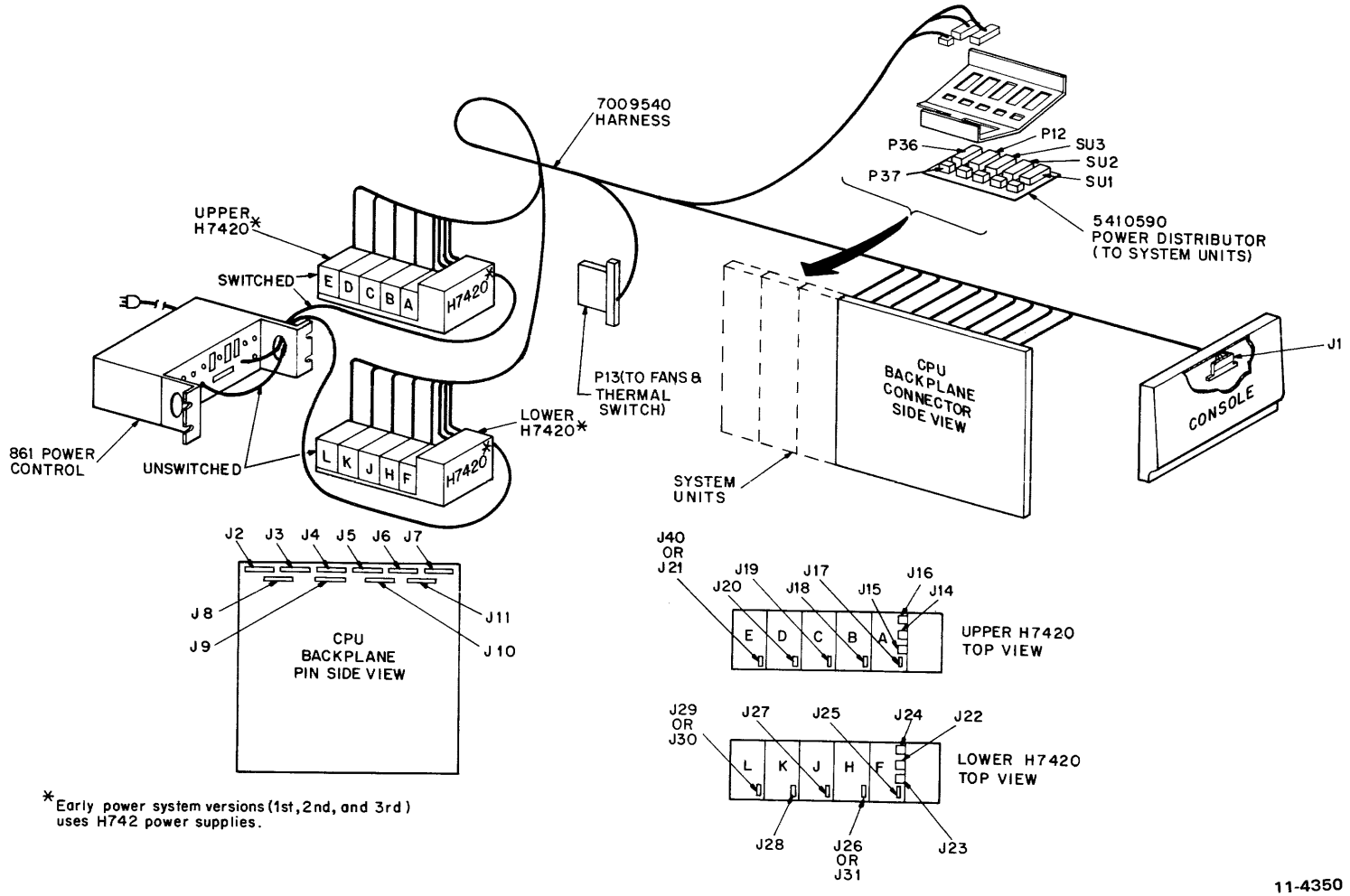
The CPU Cabinet Power Distribution System exists in four versions. The types of power control, harness, and supply used in the CPU cabinet determine the version of power system. Table 3-3 lists each version. The first version includes two 860 power controls, a 7008784 power harness and a H742 power supply. The two 860 power controls were then replaced by one 861 power control to generate the second version. A different power harness was then utilized, when CPU cabinet serial number 2000 was produced, to generate the third version. The latest version contains the previous revisions and a different power supply – the H7420 instead of the H742. Figure 3-2 shows a pictorial representation of the second and third versions. Figure 3-3 shows a pictorial representation of the first and second versions.

Each 11/45 or 11/50 uses one of the four versions of the power systems. The 11/55 uses only the most current power system version (4th).

Table 3-3 Power System Versions

	Power System Version			
	1st	**2nd**	**3rd**	**4th (Current)**
Power Control	(2) 860	861	861	861
Power Harness*	7008784	7008784	7009540	7009540
Power Supply	H742	H742	H742	H7420
	Below CPU cabinet serial numer 2000		Above CPU cabinet serial number 2000	

*Power harness of the CPU cabinet. Note the entire power system uses a number of power harnesses.



*Early power system versions (1st, 2nd, and 3rd) uses H742 power supplies.

Figure 3-2 Newer Versions (3rd and 4th) of Power System; CPU Cabinet Serial Numbers 2000 and Higher

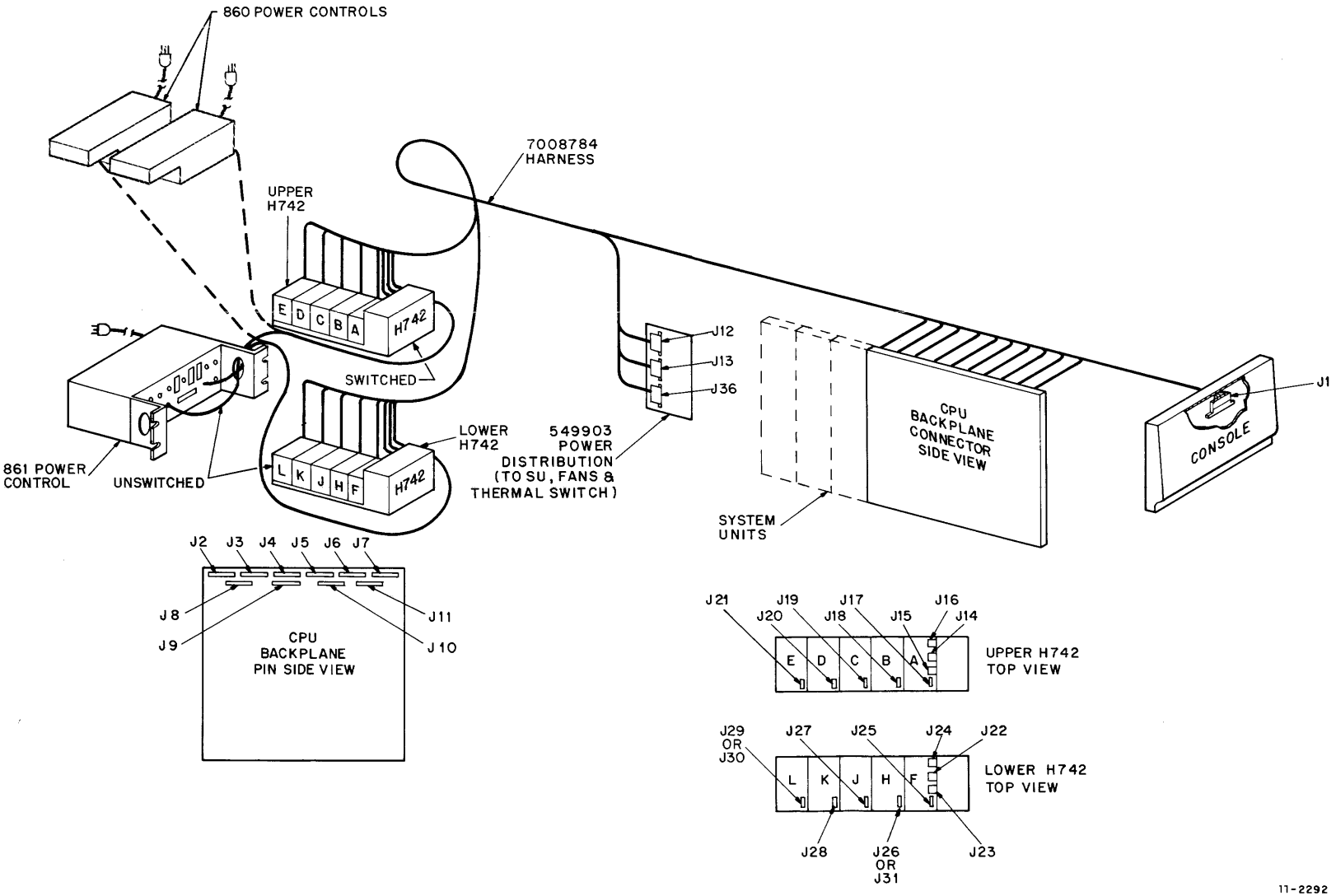


Figure 3-3 Early Versions (1st and 2nd) of Power System;
CPU Cabinet Serial Numbers Less Than 2000

CHAPTER 4
AC POWER DISTRIBUTION

This chapter contains information relative to ac power control and distribution in the PDP-11/45, 11/50, 11/55 CPU cabinet. Input specifications for ac power are discussed in Paragraphs 1.1.2 and 2.2.4. Appendix C lists ac power requirements for the various components of the PDP-11 system.

4.1 PRIMARY AC POWER OUTLETS

4.1.1 Primary AC Power Outlets, 861 Power Control

The type of input power cable provided depends on which version of the 861 power control is being installed (see Table 4-1). Cables supplied with all versions are 15 feet long and composed of insulated stranded conductors. The power cable connector types provided also differ depending upon which 861 version is being installed. Table 4-2 lists the plug and receptacle types with NEMA, Hubbell, and DEC designations. Figure 4-1 illustrates the power connector outlines and provides color coding information.

Table 4-1 Input Power Cables

Control	Conductors	Size	Coding
861-A	4	#12 AWG	Green, black, white, red
861-B	3	#14 AWG	Green, black, white
861-C*	3	#12 AWG	Green, black, white

*Used on peripheral cabinets.

Table 4-2 Input Power Cable Connections

Model No.	NEMA Configuration	Description	Poles	Wires	PLUG		RECEPTACLE	
					DEC #	HUBBELL #	DEC #	HUBBELL #
861A	L14-20*	120 V, 2ϕ, 20 A 120 V, Split phase, 20 A	3	4	12-11045	2411	12-11046	2410
861-B 860-B	L6-20*	240 V, 1ϕ, 20 A	2	3	12-11192	2321	12-11191	2320
861-C 860-A	L5-30*	120 V, 1ϕ, 30 A	2	3	12-11193	2611	12-11194	2610

* Add Suffix "P" for plug, "R" for receptacle

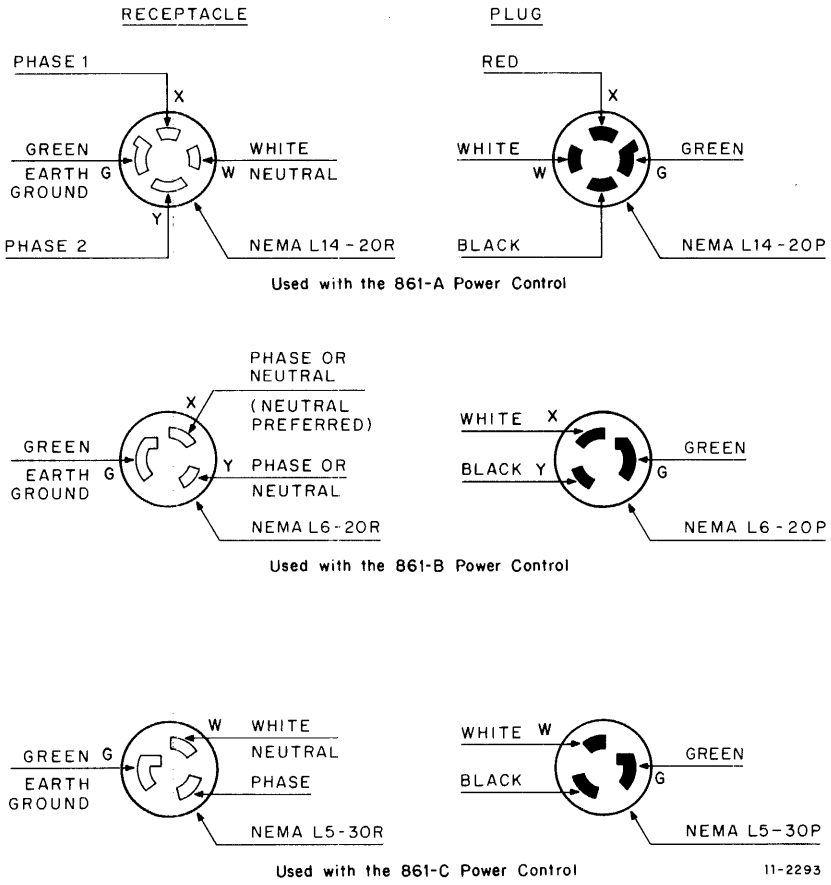


Figure 4-1 Power Connectors

An 861-A must be supplied with two power phases that are displaced by either 180° (120/240 V split phase) or 120° (two phases of a 120/208 V 3-phase Y). The same phase must not be connected to both X and Y terminals because this would cause current in excess of 20 A to flow through the neutral wire, causing the circuit breaker to trip. Figure 4-2 shows the proper connections for an 861-A power control.

861-B and 861-C power controls use the plugs and receptacles shown in Table 4-2; these are wired as shown in Figure 4-1.

4.1.2 Primary AC Power Outlets, 860 Power Controls

Primary power outlets at the installation site must be compatible with the primary power input connectors. The PDP-11/45, 11/50, 11/55 requires two recepticles – one for the 860 power control associated with the switched H742 power supply, and one for the 860 power control associated with the unswitched H742 power supply. Table 4-2 describes the plugs and receptacles used with the 860-A and 860-B power control units. Figure 4-1 shows the outline of the plugs and receptacles and the connections to them. (Plugs and receptacles of the 861 are the same for the 860.)

4.2 AC POWER CONTROL

Power from the building mains is applied to the system components in each cabinet through power control unit(s). These units are interconnected to allow power in all the cabinets of a system to be controlled from the console (power ON/OFF) or from emergency shut-down devices (OFF only). Interconnections are explained in Paragraph 4.2.1, and the power control units in Paragraph 4.2.2.

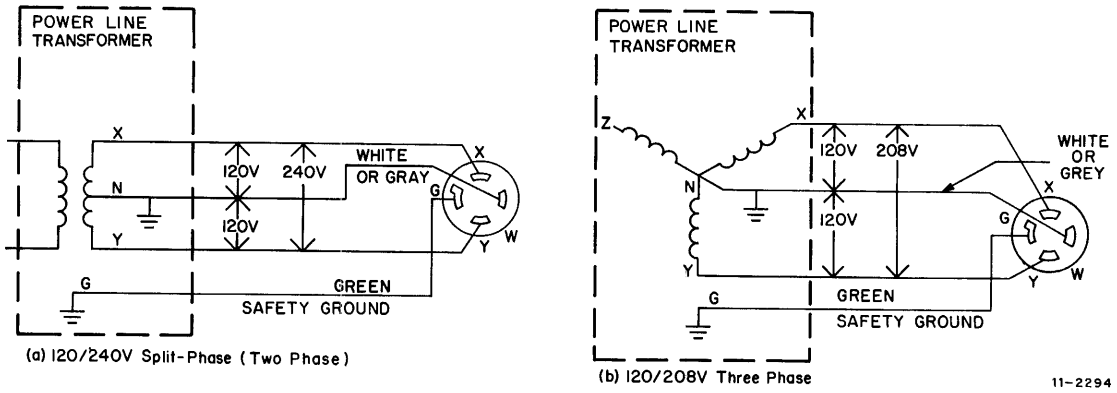


Figure 4-2 Two-Phase Outlet Connections for Use with 861-A Power Control

4.2.1 Remote Power Connections

Each cabinet in a PDP-11/45, 11/50, 11/55 system has one 861 or two 860 power controls. All the power controls are connected by a 3-wire bus that carries a remote turn-on signal (line 1), an emergency turn-off signal (line 2) and a control ground (line 3). These signals appear on pins 1, 2, and 3, respectively of the power control's J1, J2, and J3 connectors. Operation occurs as follows:

1. Connection between line 1 and line 3 energizes the power control relay and applies power to the components under control. When the LOCAL/OFF/REMOTE switch on the power control is in LOCAL, line 1 and line 3 are connected.

2. Connection between line 2 and line 3 overrides all other conditions to disconnect input power to the components under control.

3. If no connection exists between either lines 1 or 2 and line 3, the components will remain in the power off state unless the LOCAL/OFF/REMOTE switch is in LOCAL.

Refer to Figure 4-3. Three identical paralled-wired Mate-N-Lok connectors are provided on each power control. A cable, DEC part number 7008288, is supplied with each cabinet to connect the power control of that cabinet to the power control in the next cabinet. Because each power control must be capable of connecting to the power controls in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet cables; a third connector is provided for connection to thermal switches and other shut-off devices within the cabinet.

The 3-wire power control cable, DEC part number 7008288, can also be used to interconnect H720 power supplies. A special power control cable, DEC part number 7008964, is used to connect an 860 or 861 power control to an H720 power supply. This cable is available for use with special multiprocessor systems that include both a PDP-11/45, 11/50, 11/55 and a PDP-11/15 or a PDP-11/20.

4.2.2 Power Controllers

Circuit schematics of the 861-A, 861-B and 861-C power controls are included in the engineering drawing set (D-CS-861-A-1, D-CS-861-B-1, and D-CS-861-C-1). (Figure 4-8 shows circuit details of the 860 power control used in early systems.) Two identical 860 power controls are used in each cabinet, one for the switched, and one for the unswitched power supplies.

Table 4-3 summarizes the operation of the power controls.

A detailed description of the 861 and of the 860 circuitry is given in the following paragraphs.

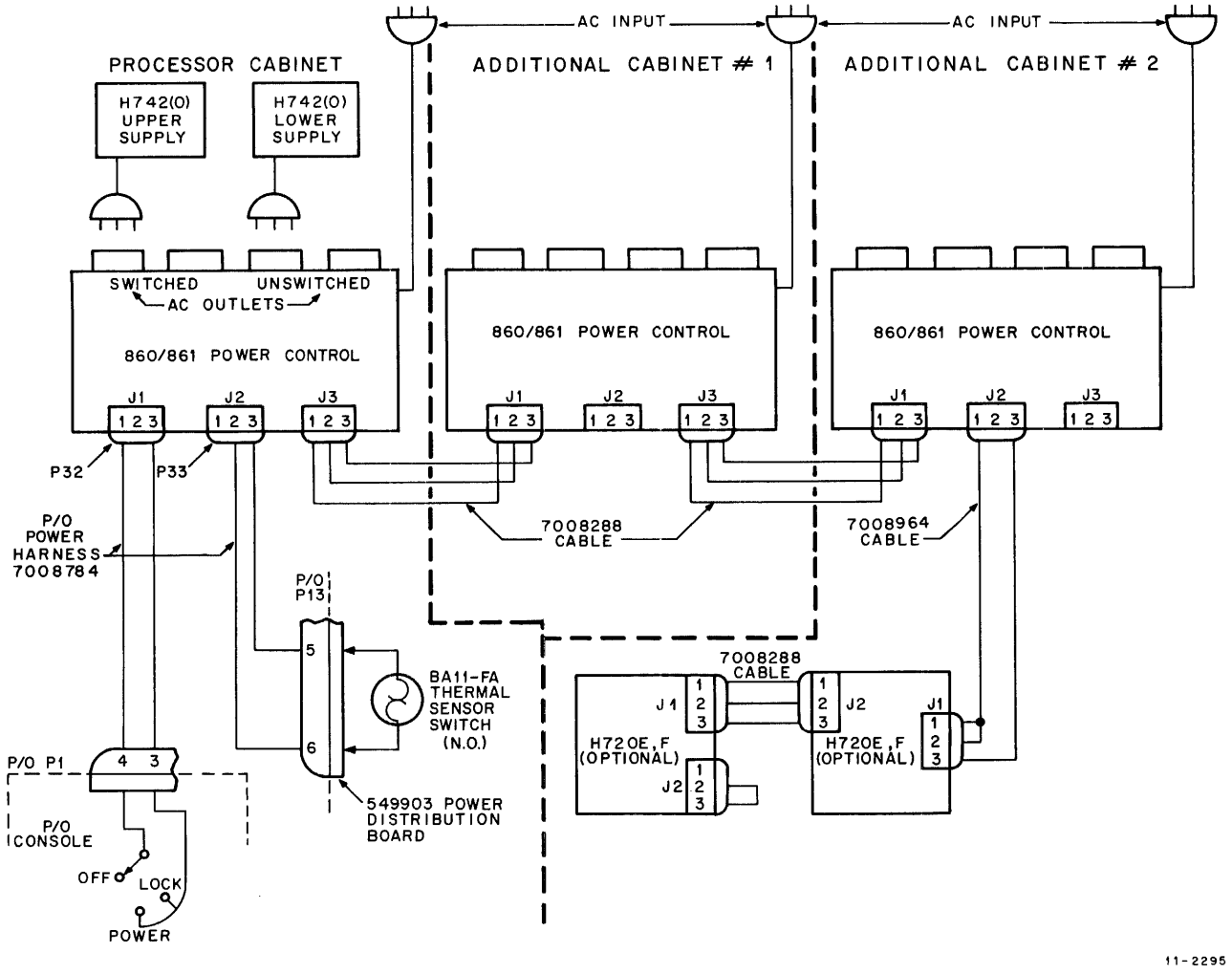


Figure 4-3 Example of Remote Power Control

Table 4-3 Power Control Operation

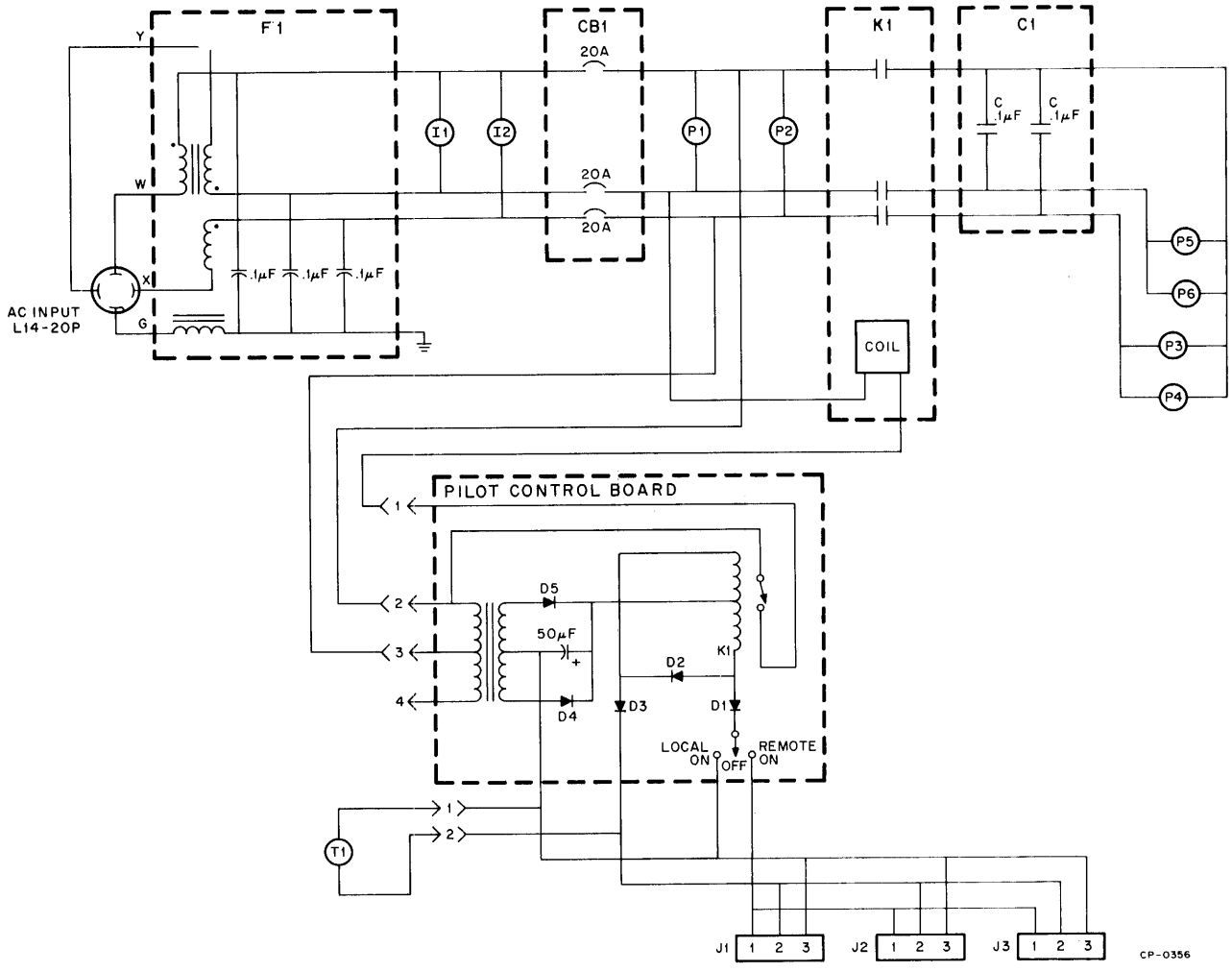
CONNECTIONS BETWEEN CONTROL LINES	SWITCH POSITION		
	LOCAL	OFF	REMOTE
	SWITCHED POWER IS	SWITCHED POWER IS	SWITCHED POWER IS
NONE	ON	OFF	OFF
1-3	ON	OFF	ON
2-3	OFF	OFF	OFF
1-3, 2-3	OFF	OFF	OFF

4.2.2.1 861 Power Controls – There are three versions of the 861 power control:

- 861-A, 90–135 Vac, 2 phase, 32 A (20 A circuit breaker)
- 861-B, 180–270 Vac, 1 phase, 16 A (20 A circuit breaker)
- 861-C, 90–135 Vac, 1 phase, 24 A (30 A circuit breaker)

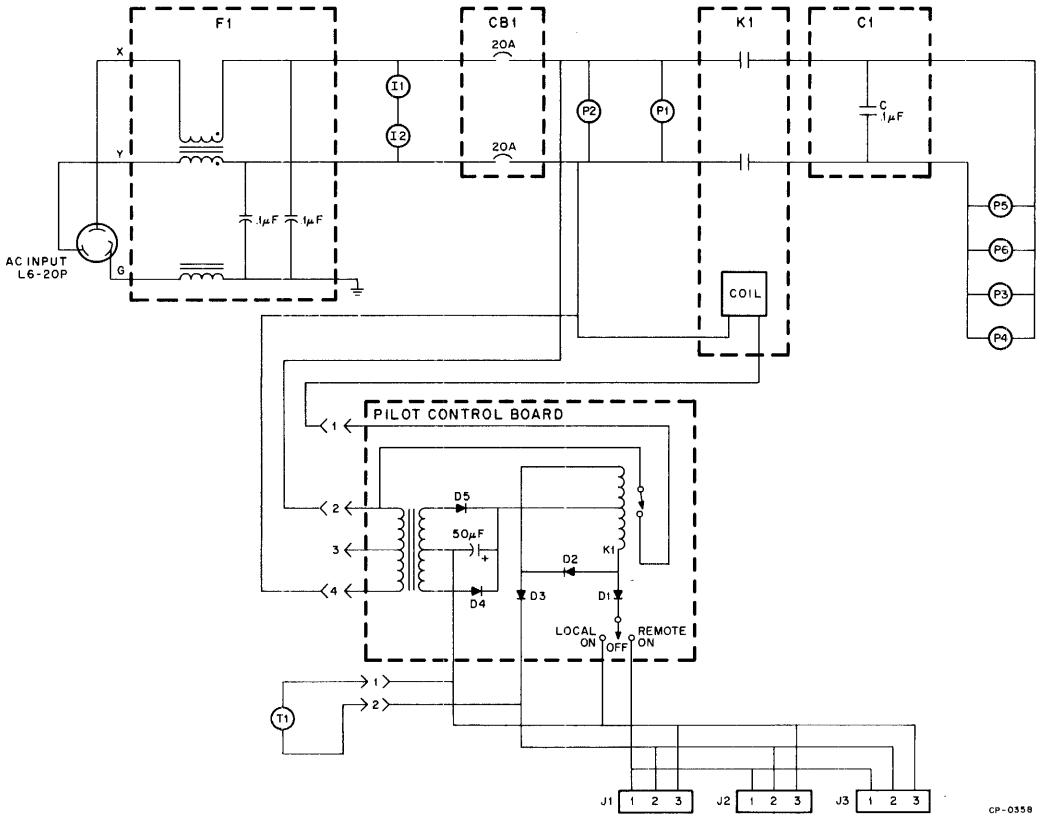
The following paragraphs describe the operation of the 861 power controls in general terms; Figures 4-4A, B, and C are simplified schematics of the three 861 models.

861 Operation – Refer to Figure 4-4. Power is applied to the terminal block mounted on the power line filter, which is an L-type L-C filter with series RF chokes and shunt capacitors to ground. If the rated voltage is present at the indicator terminals, I1 and/or I2 light. All ac lines are connected to elements at the circuit breaker CB1. All loads connected to the power controller (both switched and unswitched) are controlled by CB1.

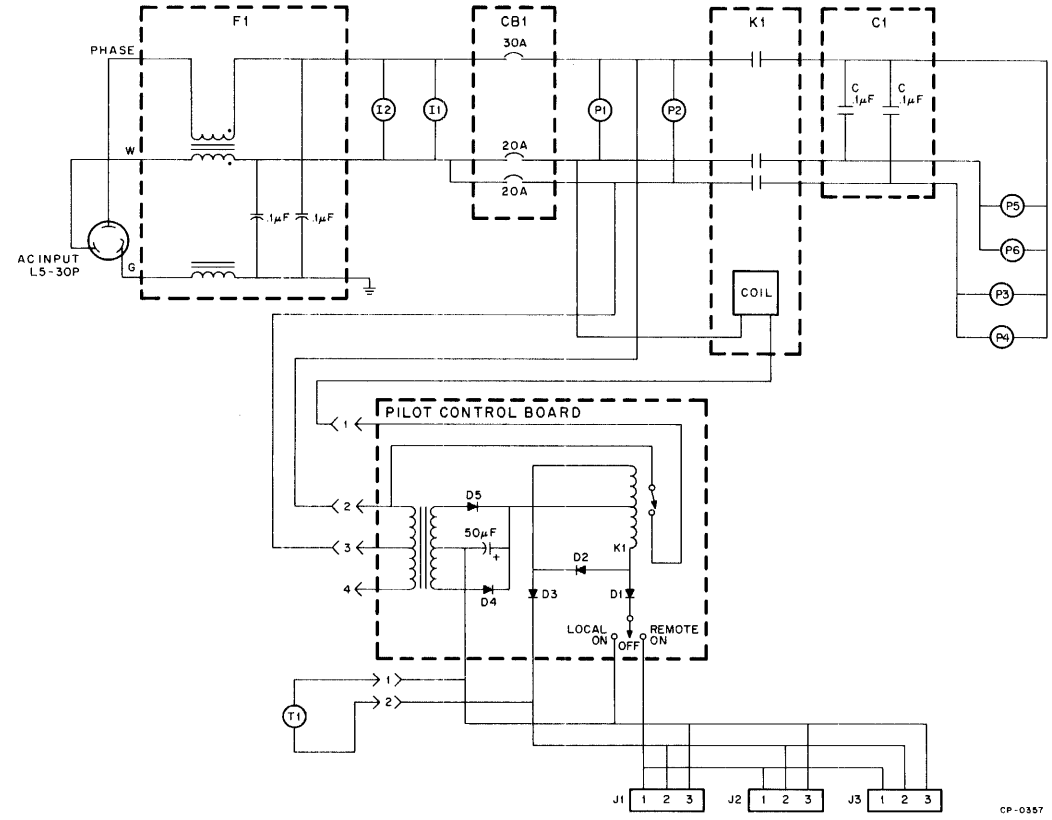


A. 861-A

Figure 4-4 861 Power Controller Schematic (Sheet 1 of 2)



B. 861-B



C. 861-C

Figure 4-4 861 Power Controller Schematic (Sheet 2 of 2)

If the current through any of the ac lines exceeds the rating of CB1, CB1 trips, removing power from the loads. Power outlets P1 and P2 connect across the circuit breaker output. These outlets are energized whenever the circuit breaker is closed. Each outlet line from CB1 is connected to a normally open contact on relay K1. The field coil associated with K1 is energized by the output of CB1 if a relay on the pilot control board is closed (see below for a description of the pilot control board).

When K1 is closed, ac power is applied across outlets P3, P4, P5, and P6. The two 0.1 μF capacitors (C1) connected across the lines at the relay reduce the amplitude of voltage spikes at the output of the controller when switching inductive loads, thereby preventing interference to nearby electronic data processing equipment.

Pilot Control Board Circuit Description – Figures 4-4A, B, and C illustrate the pilot control board simplified circuit schematic. The pilot control board contains the circuitry that allows remote turn-on and emergency turn-off of the switched power outlets (P3, P4, P5, and P6) in all 861 power controller versions. These functions are accomplished by controlling the voltage applied to the field coil of relay K1 in the 861 power controller.

The circuit consists basically of a full-wave rectifier loaded by the center-tapped field coil of a relay. Three control lines connect to the board. Pin 3 connects to the center-tapped secondary of the full wave rectifier transformer. Pin 2 is the disable (emergency shutdown) line from the signal bus; pin 1 is the enable (power request) line from the signal bus. Two additional lines (from the thermal switch) are connected to the lines associated with pins 3 and 2.

When the LOCAL/OFF/REMOTE switch is in the REMOTE position and pins 3 and 1 are connected, current flows through the lower portion of the center-tapped relay field coil to the full-wave rectifier transformer. This action closes the relay on the pilot control board and causes an energizing potential to be applied across the field coil associated with K1 in the power controller energizing the controlled outlets P3, P4, P5, and P6. When pins 3 and 2 are connected (emergency shutdown is true), current flows through the lower and upper halves of the centertapped field coil in opposite directions before returning to the power supply transformer. The resultant current through the field coil is less than that required for holding the relay closed. Energizing potential, therefore, is not present at relay K1 and power is removed from controlled outlets P3, P4, P5, and P6.

Diode D2 provides a current path in the lower section of the coil to prevent closing the relay in instances where pins 3 and 2 are connected but pins 1 and 3 are not.

Closing T1 (the thermal switch) performs the same function as emergency shutdown (connects pins 2 and 3 together). This switch is exposed to the ambient air surrounding the power controller. Temperatures above 160° F close the switch (disabling P3, P4, P5, and P6). The switch resets automatically when the temperature drops below 120° F.

Placing the LOCAL/OFF/REMOTE switch in the LOCAL position provides a connection between pin 3 and the lower portion of the coil to energize K1, regardless of the state of the power request line on the signal bus. This switch position is normally used for maintenance purposes; operations on the pilot control board are exactly the same for situations where a connection is provided between pins 3 and 1 of the signal bus connector due to closing of a circuit in an external device. A connection between pins 2 and 3 disables the switched outlets regardless of the position of the LOCAL/OFF/REMOTE switch.

The power supply that provides the potential for closing the relay need not be returned to ground. It can be operated in a floating configuration where a connection between pins 3 and 2 (as by the thermal switch or emergency shutdown) disables the switched outlets and a connection between pins 1 and 3 (power request) enables the switched outlets.

4.2.2.2 860 Power Controls – Figure 4-8 shows circuit details of the 860 power control for the switched power supply. Either an 860-A or 860-B power control is supplied, depending on the power source voltage. The 860-A operates with 115 Vac input power, and the 860-B operates with 230 Vac power. The basic differences between these 860 types are that:

1. CB1 is a 30 A circuit breaker in the 860-A and a 15 A circuit breaker in the 860-B.

b. T1 primary is connected for 115 Vac in the 860-A and 230 Vac in the 860-B.

The 860 power controls for both switched and unswitched power supplies are identical.

The T1 secondary voltage is half-wave rectified to provide +24 V, which is used to provide V_{CC} to control transistors Q1 and Q2, and to energize relay K1. The +24 V output of each 860 is used to energize the K1 relay in the opposite 860 power control. The purpose of this interlock circuit is to shut down either power supply if input power to the opposite subsystem fails.

4.2.2.3 Switched 860 Power Control – In the switched 860 power control REMOTE/OFF/LOCAL switch S1 is normally set to REMOTE. When the console POWER switch is turned to ON, it completes a ground circuit that causes Q1 to cut off. When Q1 cuts off, Q2 conducts and causes relay K1 to be energized, which closes the switched output circuit. Other connectors are provided on the 860 power control so that power in other system cabinets can be controlled from the console.

Thermal switch 52 provides protection against fire or excessive heat. It is normally open but closes if the ambient temperature exceeds 130° F (54° C). If it closes, Q2 cuts off, relay K1 de-energizes, and ac output is switched off. Pin 2 on J1, J2, and J3 allows additional thermal switches in the cabinet and the extension mounting box to be connected in parallel with S2 to perform the same function.

4.2.2.4 Unswitched 860 Power Control – The unswitched 860 power control is identical to the switched power control except that the REMOTE/OFF/LOCAL switch S1 is always set to LOCAL. Thus, Q1 is always cut off, Q2 always conducts, and K1 remains energized under normal operating conditions.

Note that only excessive temperature or an input power failure to the switched 860 power control will cause unswitched power control relay K1 to de-energize.

4.3 BACK-UP AC POWER SOURCE FOR SEMICONDUCTOR MEMORY

The semiconductor memory (MOS or bipolar) offered on the PDP-11/45, 11/50, and 11/55 is volatile (i.e., stored data is not retained when power is removed from the memory). For those applications that require data to be retained in the event of ac power failure, it is necessary to provide a back-up source of power. In the event of power line outage, brown-outs, etc., this back-up source will supply minimum power to only the memory sections, cabinet fans, and CPU fans until power can be restored. This guarantees that data stored in this memory will not be lost; however, system power must be restored before the data can be accessed.

Figure 4-5 is a simplified diagram of the power system in the CPU cabinet of the PDP-11/45, 11/50, 11/55 with a back-up ac power source. Note the power source must be installed to suply ac to the CPU fans and cabinet fans and dc supply for the semiconductor memory in the event of a power line failure.

Although a back-up ac source is not available through DEC, the back-up source employed for this application must meet or exceed the ac line specifications listed in Table 4-4.

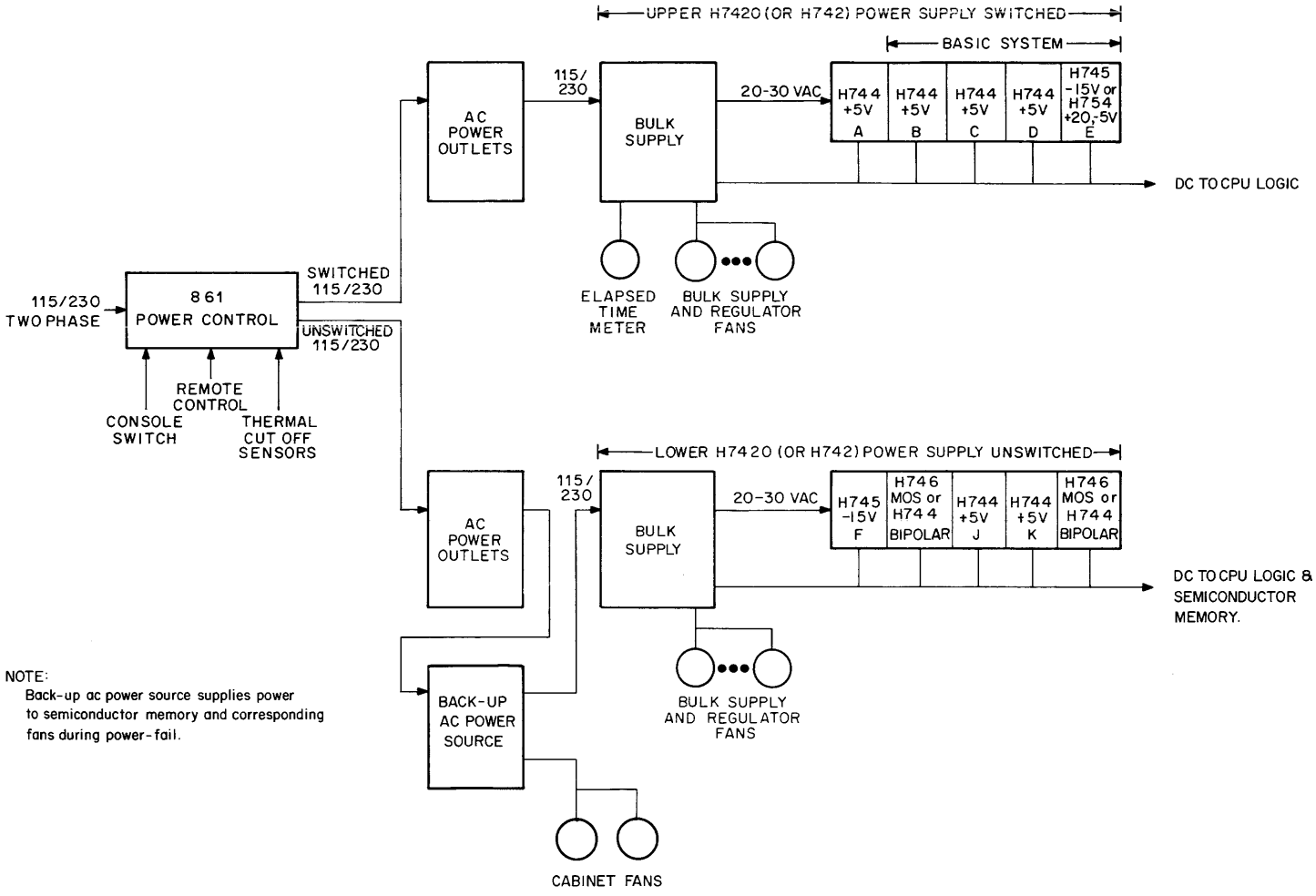


Figure 4-5 Power System Configuration with Back-Up AC Power Source

Table 4-4 Back-Up Source Specifications Requirements

Output Voltage	105–130 Vac 210–260 Vac
Output Frequency	47–63 Hz
Output Power	2000 VA (minimum)
Output Voltage Dynamic Variation	Maximum: ±10% of nominal voltage (duration <0.1 second occurring less than once every 10 seconds)
Output Harmonic Distortion	
Total	<5% maximum of fundamental
Single Harmonic	<3% maximum of fundamental
Output Transients	
Peak Voltage	<±300 V (differential and common mode)
Energy	<0.2 watt-second
Average Power	<0.5 watt
Single Transients	
Peak Voltage	<±600 V (differential and common mode)
Energy (non-repetitive)	<2.5 watt-second
Output Current	20 Arms (minimum)
Load Inrush Current	
Peak Current	±300 A (duration < ms, steady state >50 ms)

NOTE

If the input current of the back-up supply exceeds the 861 power control limit, provisions must be made for a separate ac source for the back-up supply.

Table 4-4 Back-Up Source Specifications Requirements (Cont)

861 Power Control Output Limits	861-A	861-B	861-C
Voltage	105–130 Vac	210–260 Vac	105–130 Vac
Phase	Two (120° or 180° dis-placed)	Single	Single
Frequency	47–63 Hz	47–63 Hz	47–63 Hz
Outlet Current			
Per Outlet	12 A	12 A	12 A
Per Branch Circuit	16 A	–	16 A
Total	32 A	16 A	24 A
Outlet Inrush Current (peak, 1 cycle)			
Per Branch Circuit	240 A	–	240 A
Total	480 A	240 A	360 A

4.3 AC POWER DISTRIBUTION

Figures 4-6, 4-7, and 4-8 show the ac connections for various power controls, power supplies, and fans. Figure 4-8 shows the connections of two 860 power controls and two H742 power supplies. Figure 4-7 shows an 861 power control and two H742 power supplies. The most current power system is shown in Figure 4-6 which consists of an 861 power control and two H7420 power supplies. In all three variations, any options that require an ac input are also plugged into the power control ac outlets.

Refer to Figures 3-2 and 3-3 for a pictorial view of the power connections.

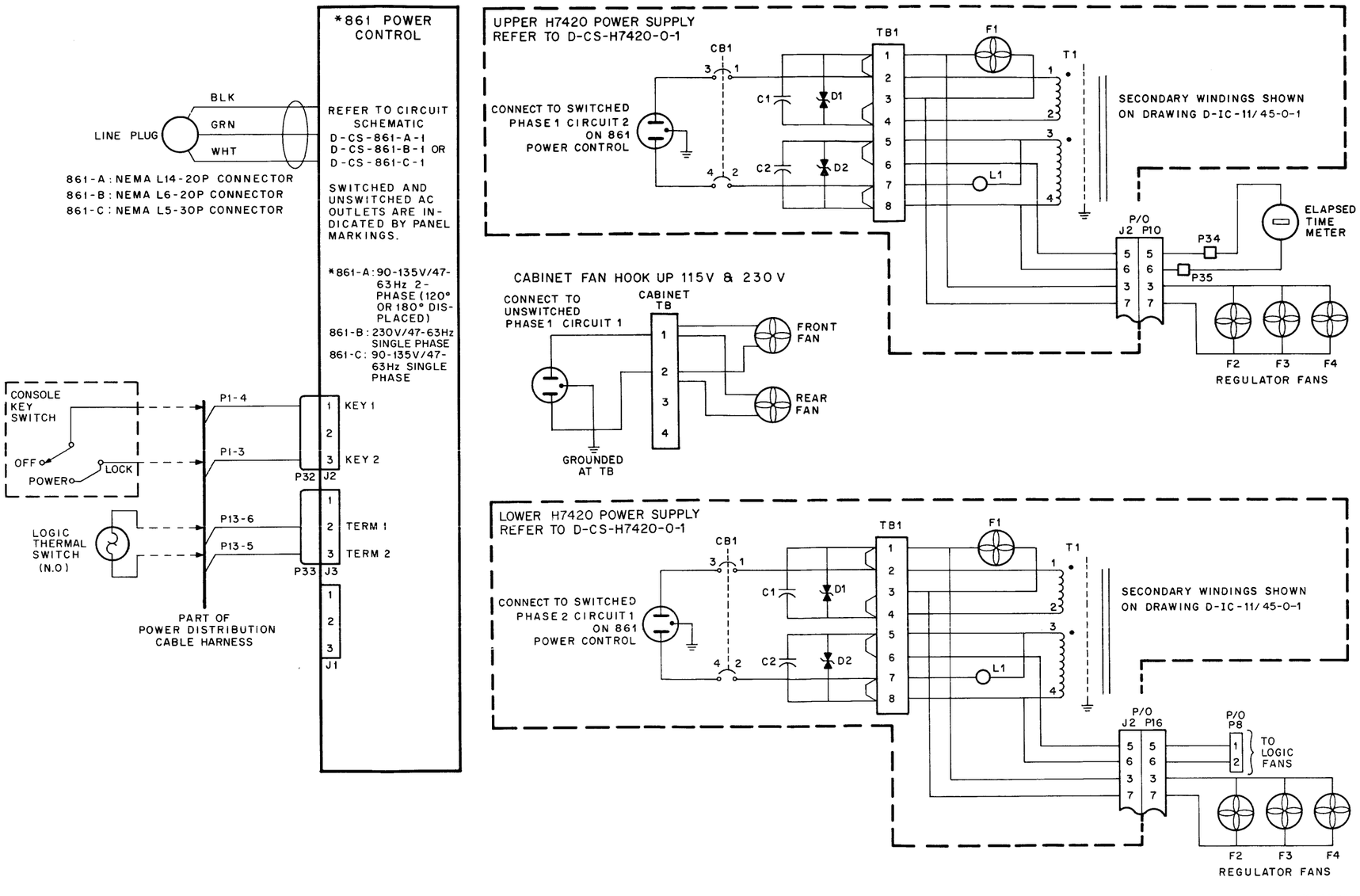


Figure 4-6 AC Power Interconnections (H7420 and 861)

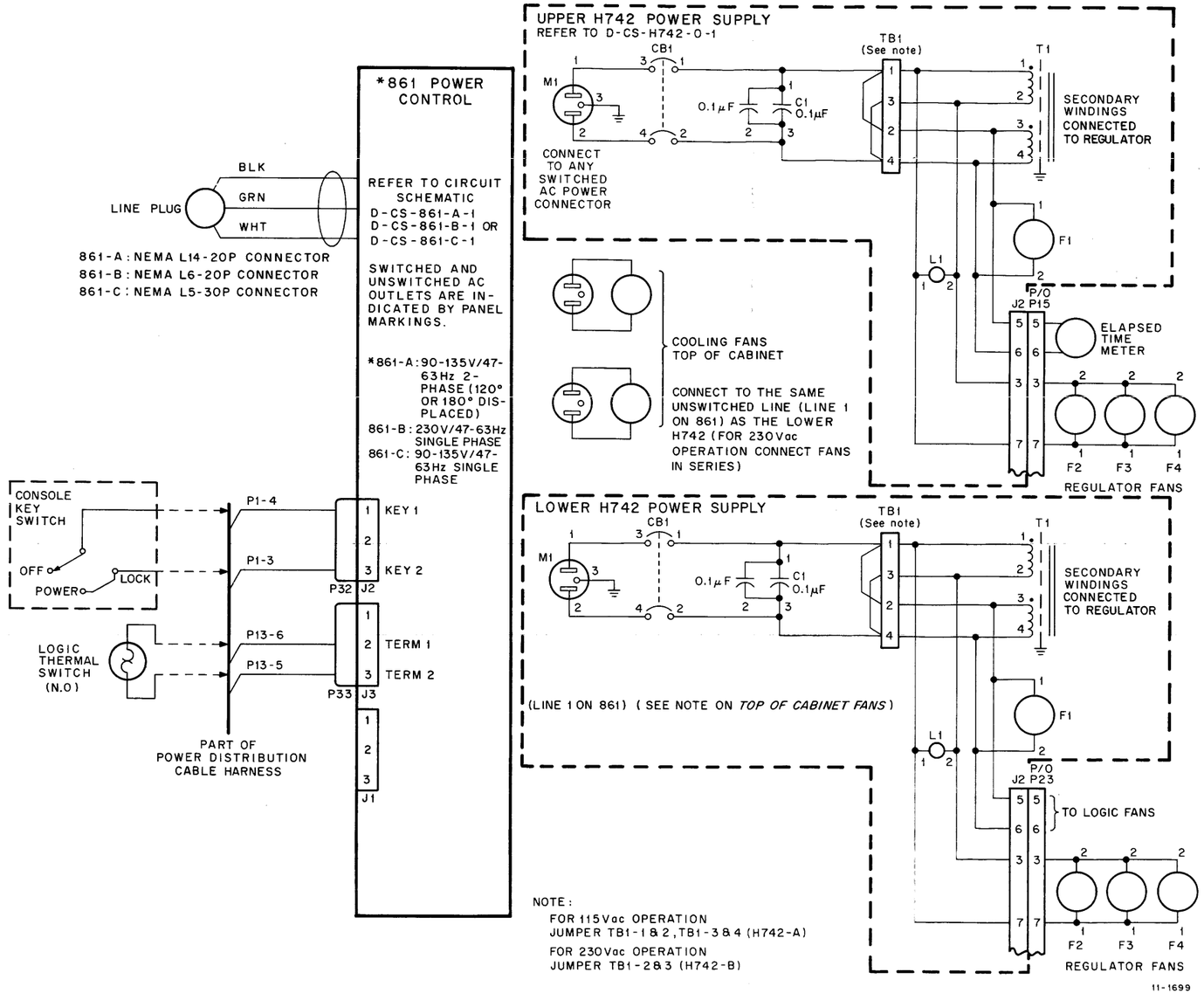


Figure 4-7 AC Power Interconnections (H742 and 861)

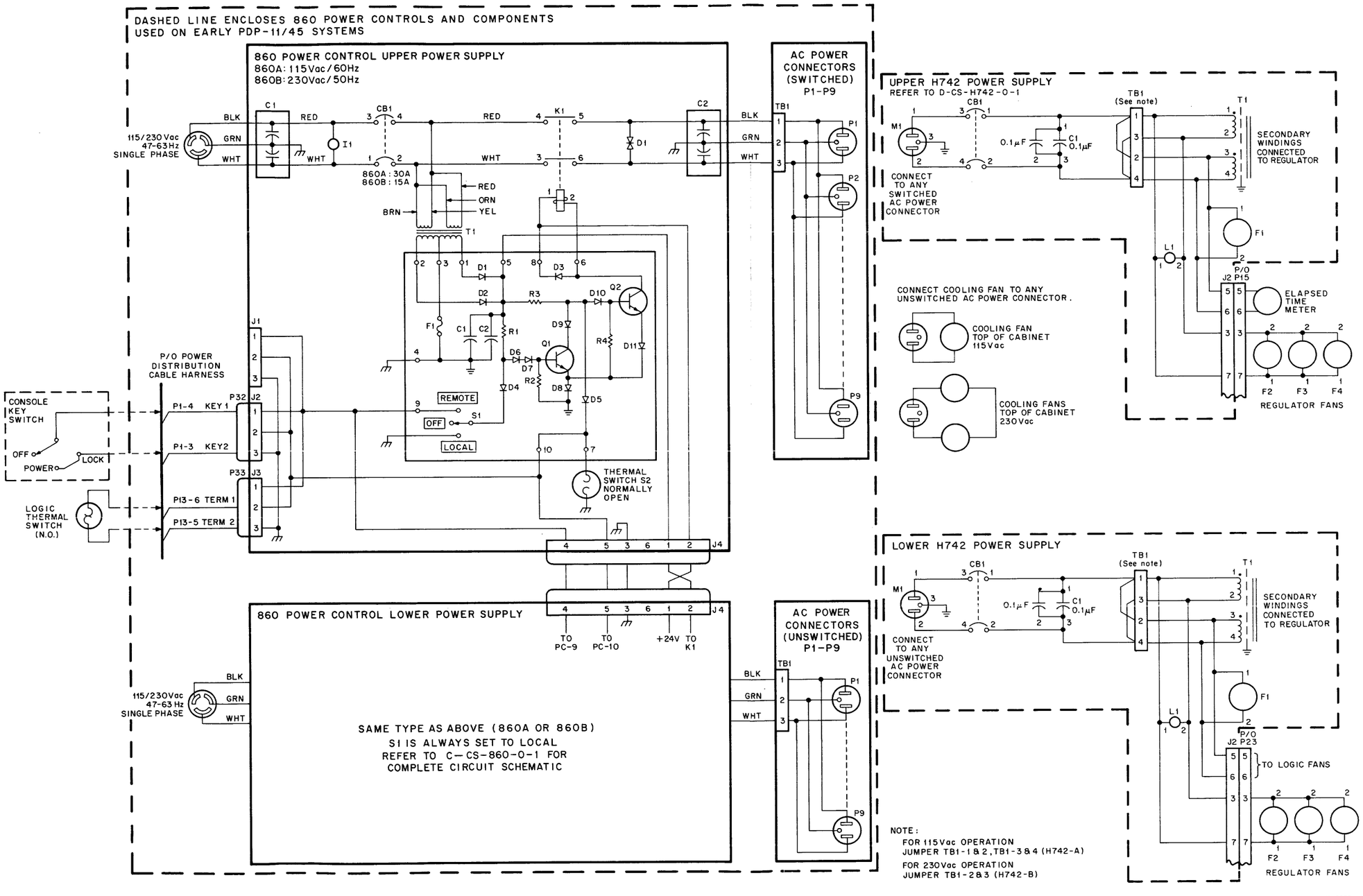


Figure 4-8 AC Power Interconnections (H742 and 860)

CHAPTER 5
DC POWER DISTRIBUTION

This chapter explains the distribution of dc power through the power harness and the configuration, and theory of the regulators.

5.1 DC POWER DISTRIBUTION

The outputs from the switched and unswitched power supplies and the voltage regulators are applied through the power distribution cable harness to the CPU backplane, the system unit power distribution board, and the console. The ac power is also supplied through the power distribution cable harness to CPU mounting box logic cooling fans; this ac power distribution is schematically shown in Figures 4-6, 4-7, and 4-8.

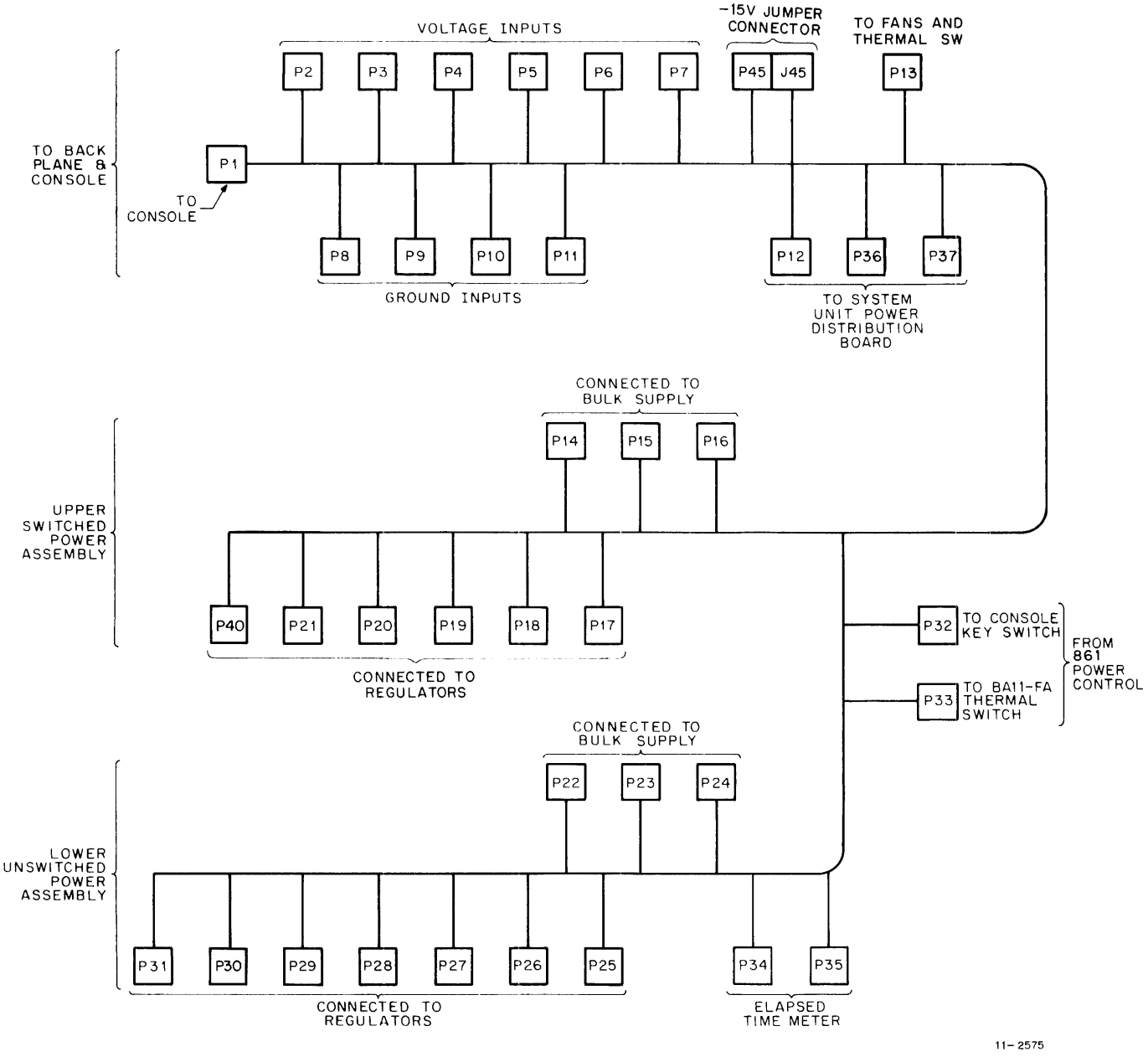
5.1.1 Power Distribution Cable Harnesses

Figures 5-1A, B, and C illustrate the revisions to the 7009540 power harness for CPU cabinets with serial numbers 2000 and higher. Figure 5-2 illustrates the earlier version of the harness (7008784) for CPU cabinets with serial numbers below 2000. Table 5-1 relates the various revisions of the harness to ECOs and specific hardware modifications.

The power distribution cable harnesses consist of three distinct connector groups that connect to the upper power supplies, the lower power supplies, and the CPU backplane and console, as shown in Figures 5-1 and 5-2. In these figures, the power harness connectors are designated with a "P" prefix; e.g., P1, P2, etc., whereas the connectors that are mounted on the bulk supplies, regulators, back panel, etc., are assigned a "J" prefix. The power harness used the male (P) half of the Mate-N-Lok connector(s), and the bulk supplies, regulators, etc., use the female (J) half of the connector(s). When a connector reference appears in the text, a "P" designation (P1, P10, etc.) refers to the power harness, and a "J" designation refers to one of the female connectors mounted on the bulk supplies, regulators, back panel, etc.

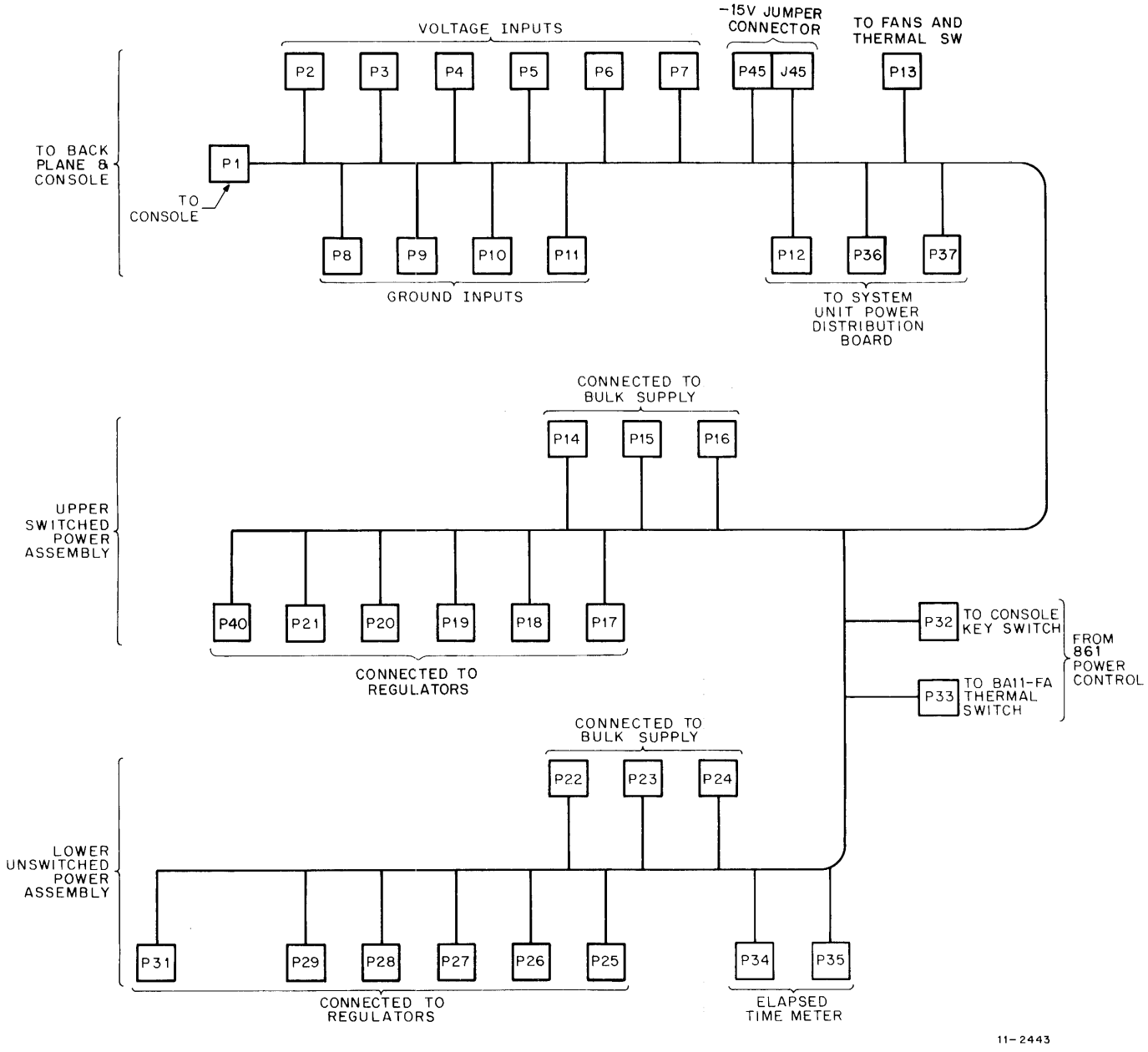
5.1.2 Backplane Power Distribution

The bulk power supply and individual regulators supply dc power, and apply it via the power harness to the ten connectors (J2 through J11) on the backplane, to the connectors on the system unit power distribution board, and to the console. The harnesses that distribute this power are shown schematically in the engineering drawings.



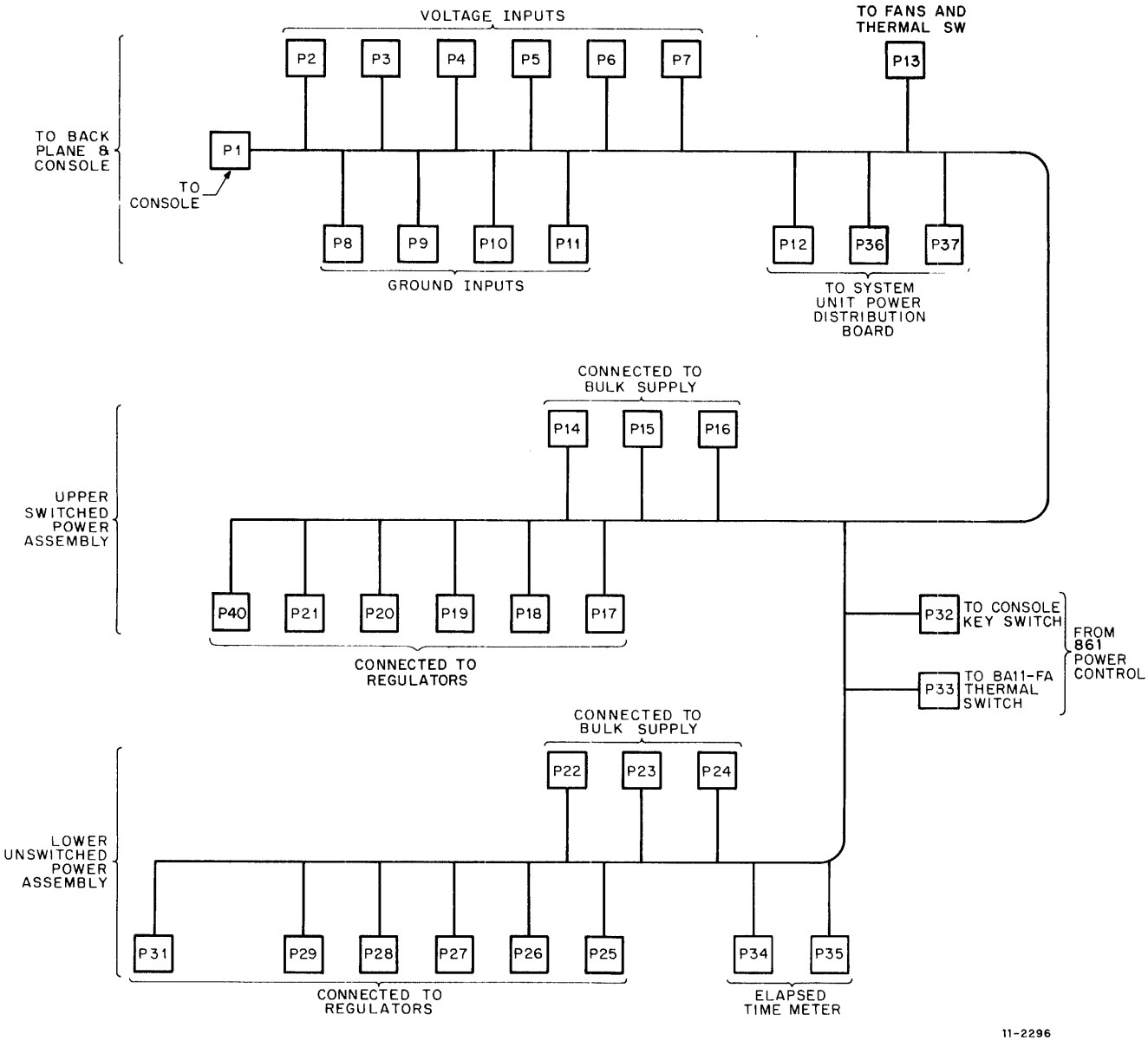
A. Revision F and H

Figure 5-1 Power Distribution Cable Harness 7009540,
CPU Cabinet Serial Numbers Greater Than 2000 (See Table 5-1) (Sheet 1 of 3)



B. Revision E

Figure 5-1 Power Distribution Cable Harness 7009540, CPU Cabinet Serial Numbers Greater Than 2000 (See Table 5-1) (Sheet 2 of 3)



C. Revision D

Figure 5-1 Power Distribution Cable Harness 7009540,
CPU Cabinet Serial Numbers Greater Than 200 (See Table 5-1) (Sheet 3 of 3)

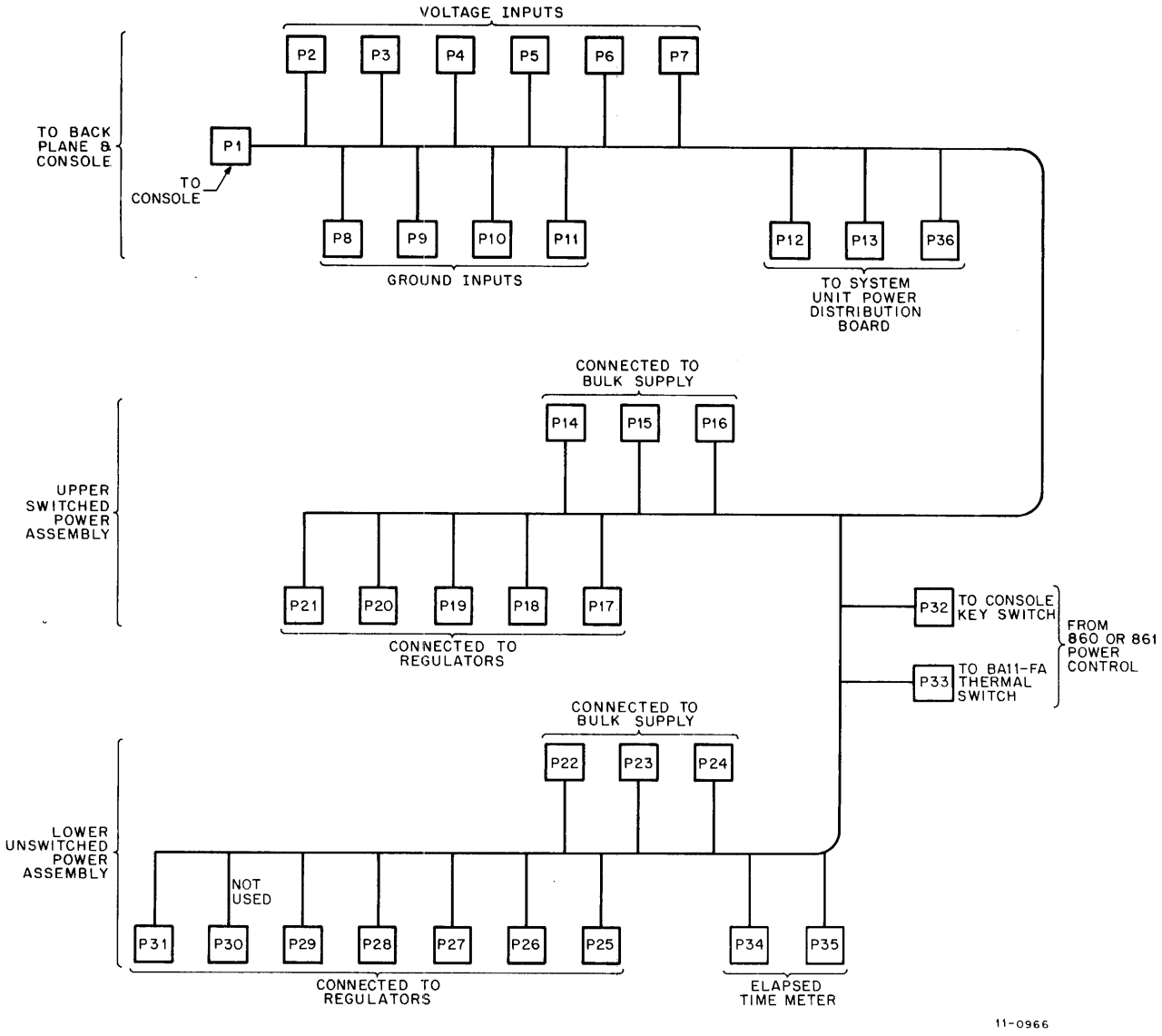


Figure 5-2 Power Distribution Cable Harness 7008784, Revisions A Through C
CPU Cabinet Serial Numbers Less Than 2000 (See Table 5-1)

Table 5-1 Major ECO Summary for the Power System

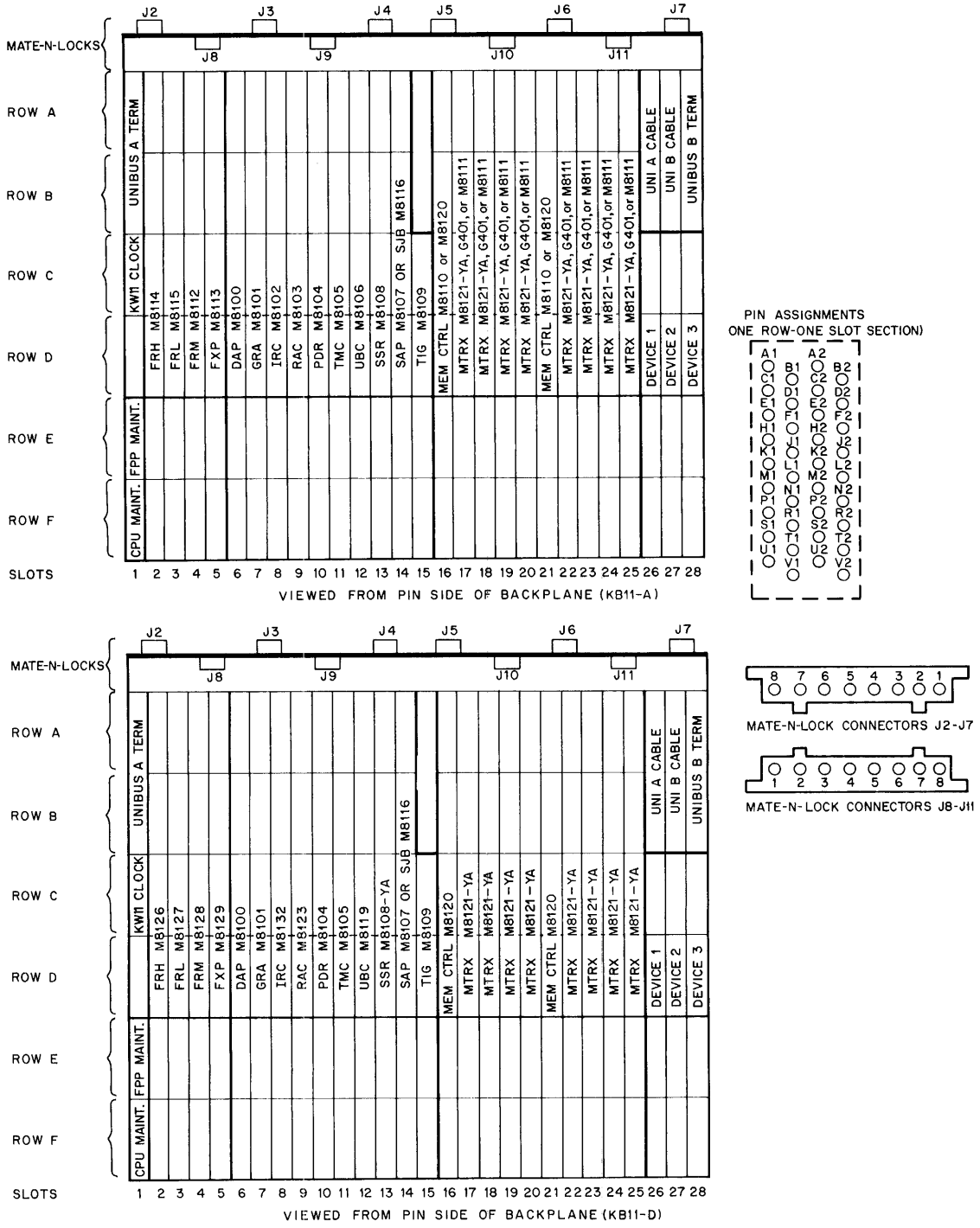
ECO No.	From Rev.	To Rev.	Description
11/45-00031	A	B	Replaced 860 Power Control with 861 Power Control. Drawing D-IC-11/45-0-1, Revision A, documents machines with the 860 Power Control.
11/45-00054	C	D	Power distribution redesigned to accommodate an H754 Regulator (+20 V and -5 V) for 16K memory. Power harness changed from Part No. 7008784 to Part No. 7009540. System unit power distribution harness moved from back of CPU box to top rear of CPU box. System unit connectors changed from flat 8-pin connector to 15-pin and 6-pin pair of rectangular connectors.
11/45-00057	D	E	7009540 harness modified for distribution of -15 V to system units when H754 Regulator is installed for 16K memory.
11/45-00060	E	F	+5 V from slot D H744 rewired to lower voltage drops to system units.
11/45-00061	F	H	CPU harness modified to accommodate second H746 MOS Regulator. Add P30 to 7009540 harness near P29 machine with S/N $\geqslant$ 2000). If S/N $<$ 2000 P30 of the 7008784 harness is rewired to distribute MOS voltage from an H746 in slot L of the lower H742. KB11-A ECO (KB11A-S0023) must be installed at the same time.

The ten connector (J2 through J11) power distribution board on the CPU backplane is etched to carry dc voltages, AC LO, DC LO, and clock signals on the outer side of the board, while the various grounds connect to the inner side to form a common ground. The CPU backplane row and slot assignments are shown in Figure 5-3. Backplane connectors and pins are shown in Figure 5-4.

Table 5-2 shows the distribution of dc power from its source at the regulator to its destination on the backplane. Connectors, slots, rows, and pins are listed.

5.2 DC POWER SUPPLIES

The theory of dc power supplies and voltage regulators are discussed in this section. Table 5-3 lists the regulator specifications.



NOTE:
For single unibus systems, an M9200 jumper module is used to connect Unibus A and Unibus B (A,B26 and A,B27) together. The unibus is then continued from slot A,B28 (M930 terminator removed).

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Figure 5-3 CPU Backplane Slot and Row Assignments

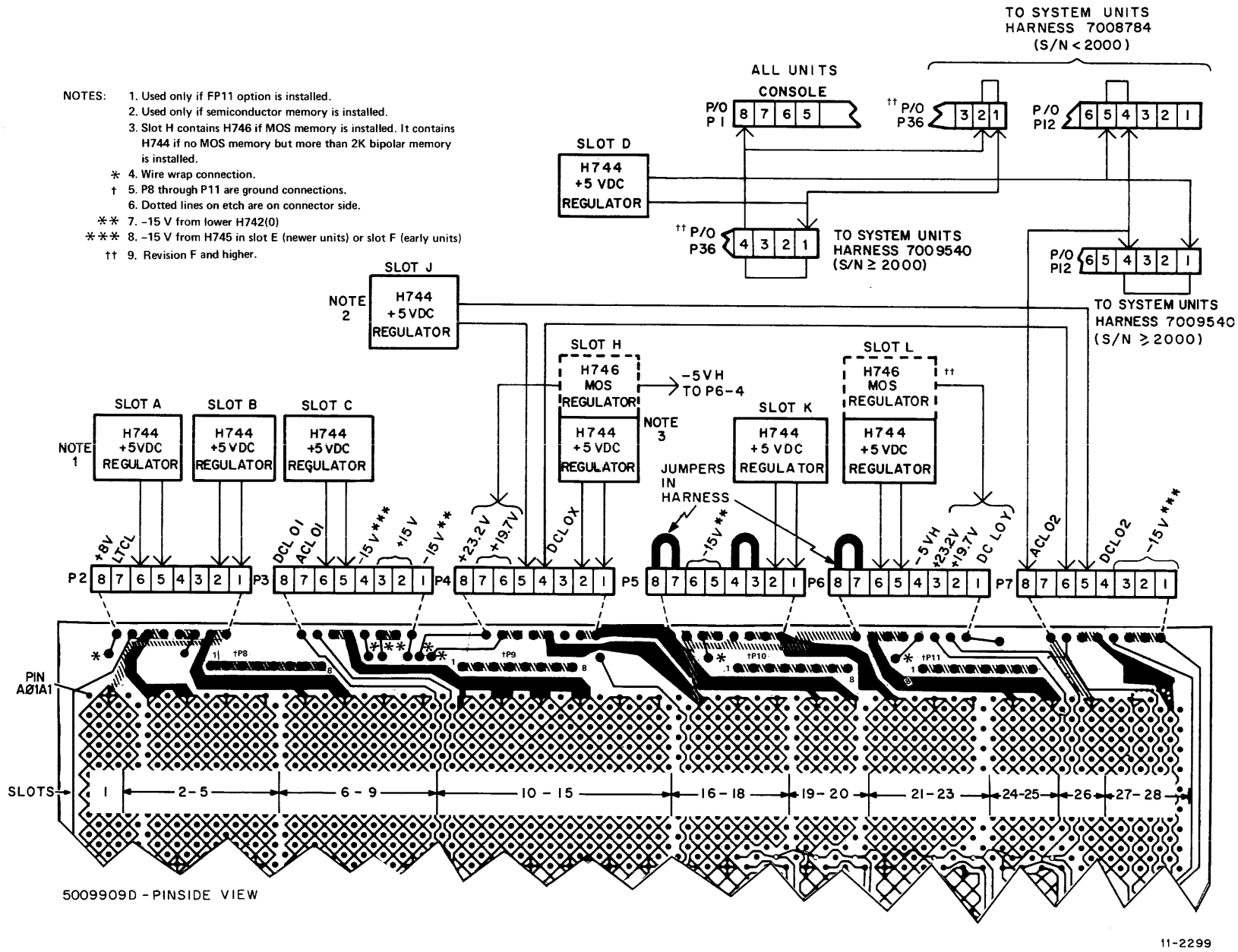


Figure 5-4 Backplane Connectors and Pins

Table 5-2 Voltage Distribution, PDP-11/45, 11/50, 11/55

VOLTAGE	REGULATOR Slot	REGULATOR Plug	HARNESS Plug	BACKPLANE Slot	BACKPLANE Row	BACKPLANE Pins	MODULES
+5 Vdc	**KB11-A, D – NO OPTIONS**						
	B	P18-2,5	J2-1,2	1,6-9	A–F	A2	Slot 1: KW11-L, W131, W133
	B	P18-2,5	J1-1,2	6-9	A–F	V1	Slots 6–9: DAP, GRA, IRC, RAC
	C	P19-2,5	J3-5,6	10-15	A–F	A2,V1	PDR, TMC, UBC, SSR, SAP or SBJ, TIG & PHK
	D	P20-2	J1-8	–	–	–	Console
*	D	P20-5	J12-1,4	–	–	–	System Units
†	D	P20-5	J12-5,4	–	–	–	System Units
	D	P20-5	J7-8	26	A, B	A2	Unibus A, Peripheral Controller
	D	P20-5	J7-8	26-28	C–F	A2	Peripheral Controllers
	FLOATING POINT OPTION						
	A	P17-2,5	J2-5,6	2-5	A–F	A2, V1	FRH, FRL, FXP, FRM
	MOS ONLY MEMORY						
	J	P27-2,5	J4-1,2,4,5	16-25	A–F	A2, V1	Slots 16 & 21[8]: M8110 Controllers
			J5-1,4,7,8	-			Slots 17–20 & 22–25: G401 Matrix Modules[5]
			J7-5,6	27-28	A, B	A2	Unibus B
	BIPOLAR ONLY MEMORY						
	J[1]	P27-2,5	J4-4,5	16-18	A–F	A2,V1	Slot 16: M8120[3]; Slots 17–18: Two M8111[1] or M8121-YA[6]
			J7-5,6	27-28	A, B	A2	Unibus B
	H[2]	P31-2,5	J4-1,2	19,20	A–F	A2, V1	Two M8111[2] or M8121-YA[7]
	K[3]	P28-2,5	J5-1,2	21-23	A–F	A2, V1	Slot 21: M8120[3], Slots 22–23: Two M8111[8] or M8121-YA[8]
	L[4]	P29-2,5	J6-5,6	24-25	A–F	A2, V1	Two M8111[8] or M8121-YA[8]
	BIPOLAR AND MOS MEMORIES						
	J[5]	P27-2,5	J4-4,5	16–20	A–F	A2, V1	Slot 16: M8110[4]; Slots 17–20: G401 (-YA)[5]
			J7-5,6	27-28	A, B	A2	Unibus B
	K[6]	P28-2,5	P5-1,2	21-23	A–F	A2, V1	Slot 21: M8120[3]; Slots 22–23: M8111[8] or M8121-YA[8]
	L[7]	P29-2,5	P6-5,6	24, 25	A–F	A2, V1	Two M8111[8] or M8121-YA[8]

* Newer systems only (S/N > 2000)
† Early systems only (S/N ≤ 2000)
[1] 1st and 2nd 1K of Bipolar Memory
[2] 3rd and 4th 1K of Bipolar Memory
[3] Bipolar Controller (early versions use an M8110)
[4] MOS Controller
[5] Up to 16K of MOS
[6] 1st and 2nd 4K of Bipolar
[7] 3rd and 4th 4K of Bipolar
[8] As required

Table 5-2 Voltage Distribution, PDP-11/45, 11/50, 11/55 (Cont)

VOLTAGE	REGULATOR		HARNESS	BACKPLANE			MODULES
	Slot	Plug	Plug	Slot	Row	Pins	
+8 Vdc	Upper H7420 (or H742)	P14-1	P2-8	1	E, F	B1	W131
+15 V †		P14-2	P21-5	–	–	–	-15 V Regulator Slot E
†			P25-5	–	–	–	-15 V Regulator Slot F
*		P14-2	P25-4	–	–	–	-15 V Regulator Slot F
*			P21-4	–	–	–	-15 V Regulator Slot E
†		P14-3	P36-8,7	–	–	–	System Units
			P3-2,3	15	E	A1	TIG
				26–28	C	A1	Peripheral Controllers
			P1-1	–	–	–	Console
*		P14-3	P12-2	–	–	–	System Units
*			P36-2	–	–	–	System Units
AC LO 1		P14-8	P3-7	12	C	S1	UBC
			P22-10	–	–	–	Lower H7420 (or H742)
AC LO 2		P14-10	P22-8	–	–	–	Lower H7420 (or H742)
			P7-7	28	B	F1	Unibus B
CLOCK		P14-11	P36-6,5	–	–	–	System Units
			P2-7	1	C	R1	KW11-L
DC LO 1		P14-12	P3-8	12	C	U1	UBC

* Newer systems only (S/N > 2000)
† Early systems only (S/N ≤ 2000)

Table 5-2 Voltage Distribution, PDP-11/45, 11/50, 11/55 (Cont)

VOLTAGE	REGULATOR		HARNESS	BACKPLANE			MODULES
	Slot	Plug	Plug	Slot	Row	Pins	
AC LO 2	Lower H7420 (or H742)	P22-8	P14-10 P7-7	– 28	– B	– F1	Upper H7420 (or H742) Unibus B
AC LO 1		P22-10	P14-8 P3-7	– 12	– C	– S1	Upper H7420 (or H742) UBC
DC LO 2		P22-9	P7-4	28	B	F2	Unibus B
DC LO X		P22-12	P4-3	16, 21	B	U2	SMC
–15 Vdc unswitched		P22-4	PP5-6,5 P3-1	21 16	E E	B2 B2	Second M8110 First M8110
–15 Vdc †	E	P21-1	P12-7,2	–	–	–	System Units No. 1 & 2
switched †			P7-1,2,3	26–28	C–F	B2	Peripheral Controllers
†			P3-4	15	E	B2	PHK
†				2,3	E	B2	FRH, FRL
†			P1-5	–	–	–	Console
*		P21-1	P36-13	–	–	–	System Units – Only if no +20, –5 V Options
†	F	P25-1	P13-7	–	–	–	System Unit No. 3
*		P25-1	P7-1,2,3	26–28	C–F	B2	Peripheral Controllers
*			P3-4	15	E	B2	PHK
*				2,3	E	B2	FRH, FRL
*			P1-5	–	–	–	Console
		P25-1	P45-3/J45-3 to P12-13				System Units - Only if Slot E Regulator is a H754 (+20, -5 V)

* Newer systems only
† Early systems only

Table 5-2 Voltage Distribution, PDP-11/45. 11/50, 11/55 (Cont)

VOLTAGE	REGULATOR		HARNESS	BACKPLANE			MODULES
	Slot	Plug	Plug	Slot	Row	Pins	
-5 Vdc MOS	H	P26-3	P6-4	17–20 22–25	F F	C1 C1	G401 (-YA) MOS Matrix
+19.7 Vdc MOS ††	H L	P26-4 P31-4	P4-6 P6-2	17–20 22–25	A,C,E A,C,E	U2 U2	
+23.2 Vdc MOS ††	H L	P26-5 P31-5	P4-8 P6-3	17–20 22–25	A,C,E A,C,E	V2 V2	
-5 Vdc	E	P40-3	P12-14	–	–	–	MM11-U/UP
+20 Vdc		P40-5	P12-3	–	–	–	

†† Revision F and higher.

Table 5-3 Regulator Specifications

Regulator	Voltage and Tolerance	Output Current (max)	Peak-to-Peak Ripple (max)
H744	+5 Vdc ± 5%	25 A	200 mV
H745	-15 Vdc ± 5%	10 A	450 mV
H746	+23.2 Vdc +3, -5% +19.7 Vdc -5 Vdc	1.6 A 3.3 A (1) 1.6 A	700 mV 700 mV 150 mV
H754	+20 Vdc ± 5% -5 Vdc ± 5%	8 A 1 A - 8 A (4)	5% 5% (3)
H742	+15 Vdc ± 10% +8 Vdc ± 15% 20–30 Vac (5 outputs)	3 A 1 A (2) 300 W ea output, 1 Kw max. total output.	– – – – – – – – –

Notes:

1. Refer to drawing D-CS-H746-0-1. Since the 19.7 V output is obtained by regulating down from the +23.2 volt level, any combination of loads on the two outputs is acceptable as long as the sum does not exceed 5 A.

   Negative 5 V level is obtained by inserting a 5.1 V Zener diode in series with the +23.2 and +19.7 loads, and using the Zener cathode as GND. Therefore, maximum -5 V load current is equal to the greater of 1.6 A or the sum of the two positive load currents (+23 and +19).

2. Total not to exceed 3 A continuously.

3. At backplane. Typical ripple ≈±3%.

4. Maximum -5 V current is dependent upon +20 V current. It is equal to 1 A + $I_{(+20)}$ up to a total of 8 A. ($I_{(+20)}$ is the amount of +20 V current.)

Each H7420 and H742 power supply provides 5 slots for regulator positioning. (See Figures 5-5 and 5-6.) The types of regulators used in these slots are dependent on the dc power requirements of the particular PDP-11/45, 11/50, or 11/55 system.

Figure 5-7A shows the voltage regulator slot assignments for the various configurations in a system with the new power harness (CPU cabinet serial numbers greater than 2000). Figure 5-7B shows the same for a system with the old harness (serial numbers 1999 or lower). Note these figures are decals that are located on the back of their related power supplies.

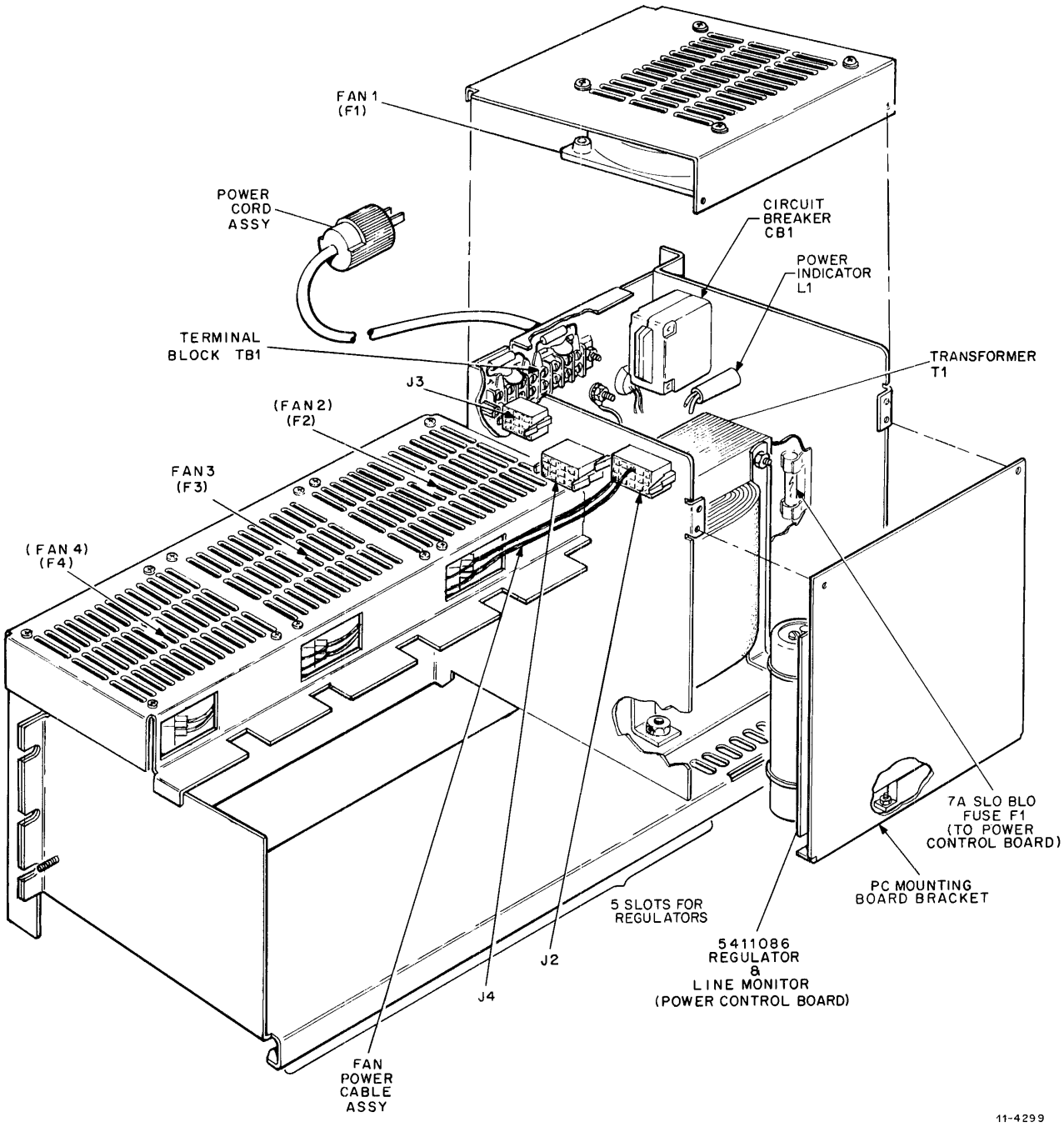
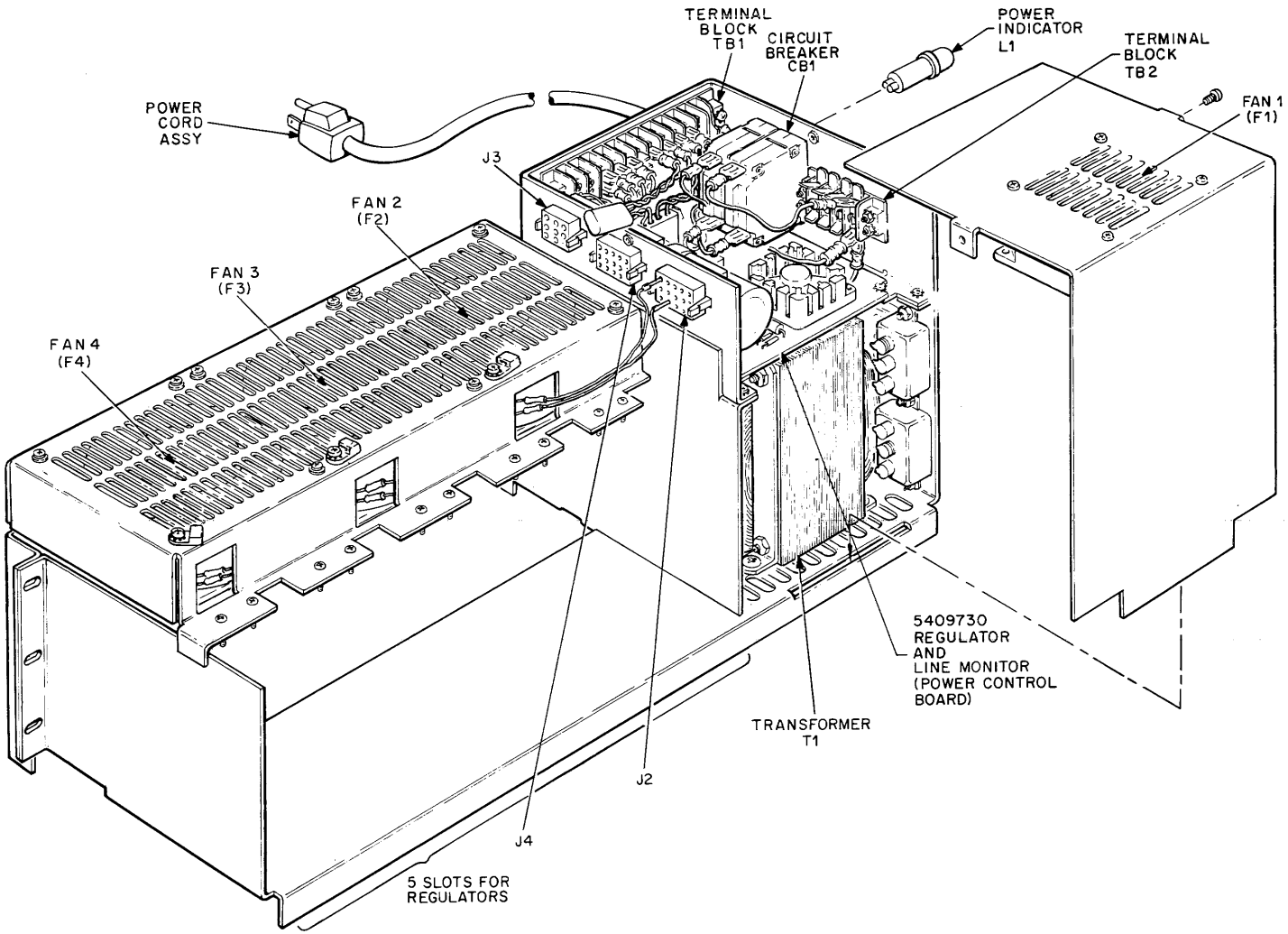


Figure 5-5 H7420 Power Supply



NOTE:
A and B version of the H742 is shown here.

Figure 5-6 H742 Power Supply

dec upper power supply

SWITCHED REGULATORS					
E	D	C	B	A	BULK SUPPLY
-15V TO SYSTEM UNITS 1.2.3	+5V INTERNAL OPTIONS +5V TO ROWS 26.27.28	+5V CENTRAL PROCESSOR	+5V CENTRAL PROCESSOR	+5V FLOATING POINT	+15V TO REGS E.F. ROW 13 & CONSOLE
					ACLO.DCLO
+20V. -5V ALTERNATE TO SYSTEM UNITS 1.2.3	+5V TO SYSTEM UNITS 1.2.3				+8V TO ROW 1 FOR MAINT MODULES
					50/60 HZ SIG (0 TO +5V) TO ROW 1 FOR CLOCK MODULE
		+5V TO ROWS 10-15	+5V TO ROWS 1.6.7.8.9	+5V TO ROWS 2.3.4.5	

Engineering Drawing No. A-DC-5310709

dec lower power supply

UNSWITCHED REGULATORS					
L	K	J	H	F	BULK SUPPLY
+5V BIPOLAR MEMORY	+5V BIPOLAR MEMORY	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO ROWS 19.20	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO ROWS 16.17.18	+15V CENTRAL PROCESSOR -15V TO ROWS 1. 2. 15	-15V TO CENTRAL PROCESSOR
		+5V IF MOS MEMORY IS INSTALLED	+19V +23V -5V IF MOS MEMORY IS INSTALLED	INTERNAL OPTIONS -15V TO ROWS 26.27.28 CONSOLE	
+5V TO ROWS 24.25	+5V TO ROWS 21.22.23	+5V TO ROWS 16-25	MOS VOLTAGES TO ROWS 16-25		ACLO DCLO

Engineering Drawing No. A-DC-5310709

A. Serial Numbers 2000 and Higher

Figure 5-7 Regulator Slot Assignments, CPU Cabinet (Sheet 1 of 2)

dec power supply

h742 a

REGULATORS					BULK SUPPLY A
E	D	C	B	A	
+15V CENTRAL PROCESSOR −15V TO ROWS 1.2.15	+5V INTERNAL OPTIONS	+5V CENTRAL PROCESSOR	+5V CENTRAL PROCESSOR	+5V FLOATING POINT	REGULATORS A.B.C.D.E SWITCHED
INTERNAL OPTIONS −15V TO ROWS 26.27.28 CONSOLE	+5V TO ROWS 26.27.28				+15V TO REGS E.F
					+15V TO ROW 13 CONSOLE
	SYSTEM UNITS +5V TO SYSTEM UNITS #1. #2. #3				+8V TO ROW 1. FOR MAINT MODULES
SYSTEM UNITS −15V TO SYS UNITS #1. #2		+5V TO ROWS 10.11.12.13.14.15	+5V TO ROWS 1.6.7.8.9	+5V TO ROWS 2.3.4.5	50/60 HZ SIG (0 TO +5V) TO ROW 1 FOR CLOCK MODULE

Engineering Drawing No. A-DC-5309993

dec power supply

h742 a

REGULATORS					BULK SUPPLY B
L	K	J	H *	F	
+5V BIPOLAR MEMORY	+5V BIPOLAR MEMORY	+5V IF BIPOLAR MEMORY IS INSTALLED	+5V IF BIPOLAR MEMORY IS INSTALLED	−15V SYSTEM UNITS	REGULATORS F.H.J.K.L NOT SWITCHED
		+5V TO ROWS 19.20	+5V TO ROWS 16.17.18		
		+5V IF MOS MEMORY IS INSTALLED	+19V +23V −5V IF MOS MEMORY IS INSTALLED		
+5V TO ROWS 24.25	+5V TO ROWS 21.22.23	+5V TO ROWS 16.17.18.19.20. 21.22.23.24.25	MOS VOLTAGES TO ROWS 16.17.18.19.20. 21.22.23.24.25	−15V TO SYS UNIT #3	* REG H WILL BE EITHER A +5V OR MOS VOLTAGE REG

Engineering Drawing No. A-DC-5309994

B. Serial Numbers Less Than 2000

Figure 5-7 Regulator Slot Assignments, CPU Cabinet (Sheet 2 of 2)

5.2.1 AC Input/Output

The input circuits of the upper and lower power supplies are shown in Figures 4-6, 4-7, and 4-8. Refer to Figures 5-5 and 5-6. Jumper connections for 115 or 230 Vac operation are provided by TB1 at the primary of T1. Each power supply contains a bulk supply cooling fan F1 and three voltage regulator cooling fans F2, F3, and F4. An elapsed time meter receives 115 Vac from the upper supply to indicate total time power is applied to the CPU. On the lower supply, the corresponding output is applied to the nine cooling fans in the CPU mounting box to provide unswitched cooling for the logic modules installed in the CPU backplane.

5.2.2 Power Control Boards

Each H7420 power supply contains a 5411086 power control board (Figure 5-5). Each H742 power supply contains a 5409730 power control board (Figure 5-6). Both types of power control boards provide dual functions as regulators and line monitors. As regulators, they provide +15 V, -15 V, and +8 V sources. As line monitors, they provide AC LO and DC LO power fail signals. They also provide an LTC signal to drive the KW11 clock options. Thus, the power control board may be referenced as a regulator or a line monitor.

AC LO L indicates that the line voltage is below a perscribed minimum. DC LO L indicates that the line voltage is below the minimum operating tolerance and that the +15 V regulator circuit cannot be expected to produce an output within specified normal operating limits. These signals are not affected by the outputs of the individual voltage regulators.

5.2.2.1 5411086 Power Control Board – Figure 5-8 shows a simplified diagram of the 5411086 control board.

+15 V and +8 V Supply

In the regulator circuit the 20–30 Vac input is full-wave rectified by bridge D11 to provide dc voltage (25 to 45 Vdc, depending on line voltage and load on +15 V) across filter capacitor C1 and bleeder resistor R15. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified diagram of E1 is shown in Figure 5-8. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, an error amplifier series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q7, predriver Q4, and level shifter Q6. Zener diode D17 is used with R11 to provide +15 V for E1.

The output circuit is standard for most switching regulators and consists of free-wheeling diode D12, choke coil L1, and output capacitor C3. These components make up the regulator output filter. Free-wheeling diode D12 is used to clamp the emitter of Q7 to ground when Q7 shuts off, thus providing discharge path for L1. This output circuit and waveforms are shown in Figure 5-9.

In operation, Q7 is turned on and off, generating a square wave of voltage that is applied across D12 at the input of the LC filter (L1 and C10). Basically, this filter is an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q7, the output (average) voltage may be varied or controlled, thus supplying regulation. The output voltage is sensed and fed back to E1, where it is compared with a fixed reference voltage. E1 turns pass transistor Q7 on and off, according to whether the output voltage level approaches its upper and lower limits (approximately +15.15 V and +14.85 V respectively).

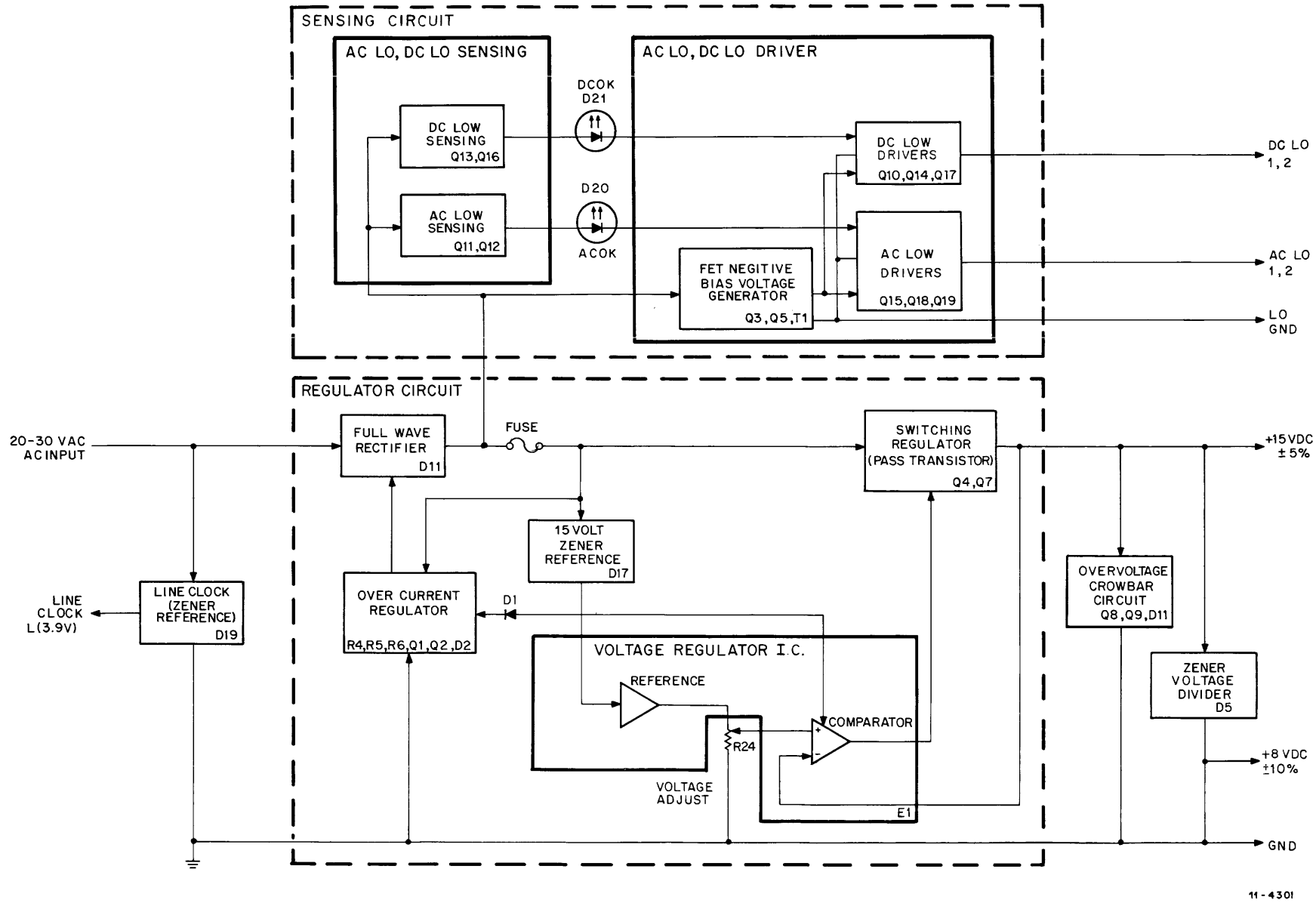
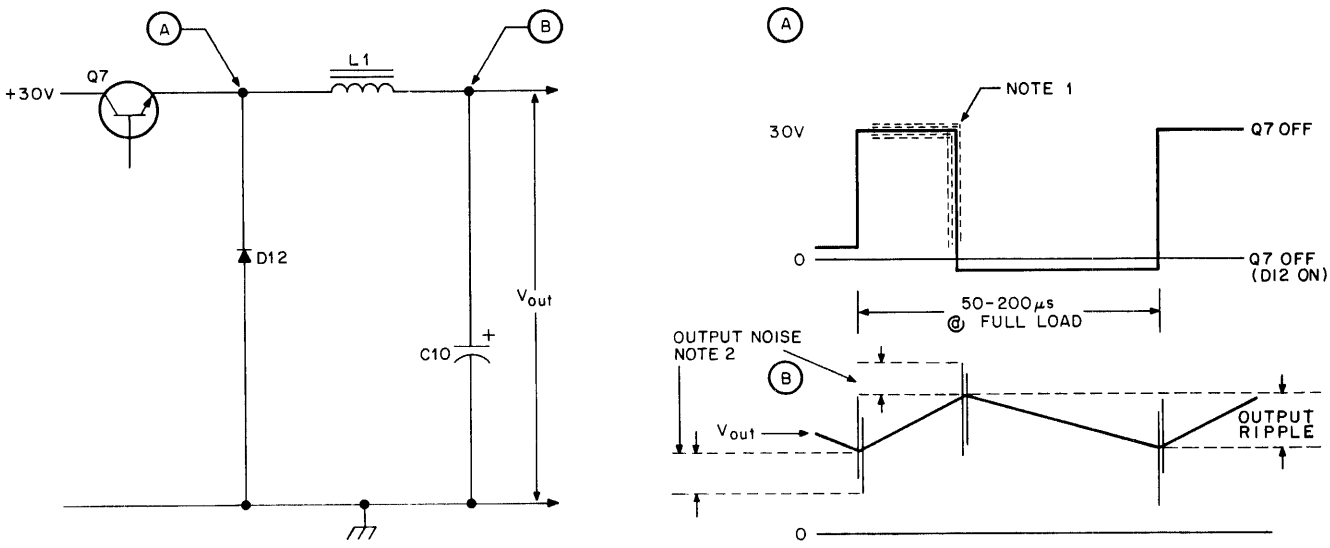


Figure 5-8 5411086 Block Diagram



NOTE 1: 30 volt level shifts with AC input voltage. Small 120Hz jitter is normal.

NOTE 2: Peak noise=1% max.

Measure noise with a short 100Ω terminated piece of foil coax. Normal 10:1 scope probe will not give an accurate noise measurement.

NOTE 3: Noise and ripple amplitudes are exaggerated in this figure for illustrative purposes.

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Figure 5-9 H744 Regulator Waveforms

During one full cycle of operation, the regulator operates as follows: Q7 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +15 V level, then a constant +15 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitor C10 absorbs this changing current, causing the output level (+15 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +15.15 V, E1 shuts off, turning Q7 off; the emitter of Q7 is then clamped to ground. L1 reverses polarity and discharges through D12 into capacitor C10, and the load. Predriver Q4 is used to increase the effective gain of Q7, thus ensuring that Q7 can be turned and off in a relatively short period of time.

Conversely, once Q7 is turned off and the output voltage begins to decrease, a predetermined value of approximately +14.85 V will be reached, causing E1 to turn on; E1 in turn, causes Q7 to conduct, beginning another cycle of operation.

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+15.15 V) and minimum (+14.85 V) values by E1. When +15.15 V is reached, E1 turns Q7 off; when +14.85 V is reached, E1 turns Q7 on. This type of circuit action is called a ripple regulator.

The overcurrent regulator circuit functions as a current regulator when the current, monitored at D11, exceeds 5 A. The current regulator consists of R4, R5, R6, Q1, Q2, and D2. During normal operation Q1 and Q2 are not conducting. Q2 starts conducting when the voltage drop across R5 and R6 (sensed by D2) exceeds approximately 0.6 V. When Q2 conducts, D1 becomes forward biased and E1 is shut off, turning off the pass transistor Q7 and predriver Q4. The conduction of Q2 will also turn on Q1 providing a constant current source (1 mA) to the base of Q2. Q1 will hold Q2 on until the current across R5 and R6 drop below approximately 4 A.

With Q1 and Zener D2 tied to the +15 V Zener reference for E1, the conduction of Q1 will hold E1 off. When Q1 and Q2 stop conducting E1 will turn on, enabling the current to exceed the regulator limits. With a continuous overcurrent condition Q1 and Q2 will be turning and off, causing the circuit to become a constant current regulator.

The +15 V overvoltage crowbar consists of the following components: Zener diode D18, and silicon-controlled rectifier (SCR) Q8, Q9, R38, R40, C13, and Q9. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across Zener diode D3 is less than 18 V. If the output voltage becomes dangerously high (above 18.0 V), diode D18 conducts, turning Q9 on, and the voltage drop across R40 draws gate current and triggers the SCR. The SCR fires, short circuits the +15 V output to ground, and turns off E1 by shorting out the +15 V reference at D17.

Line Clock Output

The line clock output (LTCL) is derived from one leg of full-wave rectifier bridge D11, by voltage divider R22 and Zener diode D19. The clock output is a 0 to +3.9 V square wave, at the line frequency of the power source (47 to 63 Hz). The clock output is used to drive the KW11 clock options.

AC LO and DC LO Circuits

The AC LO and DC LO sensing circuit has a 20–30 Vac input from a secondary winding of transformer T1. The sensing circuits are shown on drawing D-CS-5411086-0-1; a simplified version is shown in Figure 5-8. The ac input is rectified by diodes D15 and D16, and filtered by capacitors C20 and C24. A common reference voltage is derived by Zener diodes D13 and D14. Both sensing circuits operate similarly; each contains a differential amplifier and associated circuits. The major difference is that the base of Q12 in the AC LO circuit differential amplifier is at a slightly lower value than that of Q16 in the DC LO differential amplifier. The operation of both sensing circuits depends on the voltage across capacitor C8.

The AC LO and DC LO driver circuit produces the power fail signals. When an ac low condition is sensed the output of differential amplifier Q12 turns off Q9. Q19 in turn gates on FETS Q15 and Q18, generating AC LO 1 and AC LO 2 signals.

Approximately 7 ms after AC LO is sensed the DC LO sensing circuit will generate DC LO. The DC LO sensed output from differential amplifier Q16, turns off Q10. Q10 in turn gates on FETs Q14 and Q17, generating DC LO 1 and DC LO 2 signals.

The +25 Vdc to +45 Vac from rectifier D11 is applied to T1, Q3, and Q5. Q3 and Q5, due to their switching action, create a pulsating dc which is applied to the primary of transformer T1. The output from the secondary of T1 (approximately 15 V) is rectified by D6, D7, D8, and D9, producting -10 Vdc to -15 Vdc. The -10 Vdc to -15 Vdc is a negative bias used to gate OFF J FETs Q15, Q18, Q14, and Q17 via Q19 and Q10. Unlike most transistors, the negative bias is used to turn off the J FETs. The J FETs are turned on when there is zero volts between gate (G) and source (S) terminals.

Light-emitting diodes D20, (ACOK) and D21 (DCOK) are normally lit. When AC LO L and/or DC LO L are asserted, the light-emitting diodes go off, indicating that this regulator is the source of AC LO L or DC LO L on the Unibus.

Figure 5-10 shows the H7420 power-up and power-down sequences.

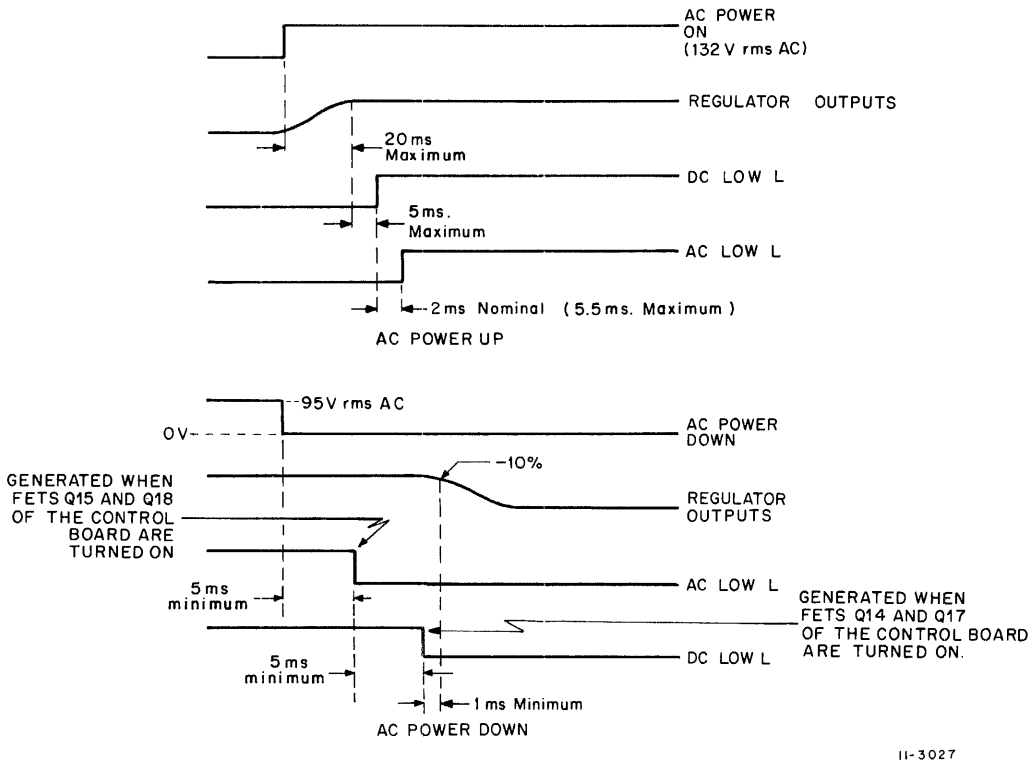


Figure 5-10 H7420 Power-Up and Power-Down Sequences

5.2.2.2 5409730 Power Control Board – Figure 5-11 shows a simplified diagram of the 5409730 control board.

+15 V and +8 V Supply – The power control board of each H742 power supply contains a +15/+8 Vdc supply (drawing C-CS-5409730-0-1). The dc supply receives 20 to 30 Vac from the secondary of transformer T1. The ac input is full-wave rectified by diode bridge D1. The resultant dc is applied to Darlington voltage regulator Q1 through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3, with respect to output pins 4, 5, and 6. Zener diode D7 provides approximately +8 Vdc at output pin 1. The combined output of this supply (+15 V and +8 V) is rated at 3 A.

The power control board outputs of the upper H742 are used as positive (+15 V, +8 V) voltages with respect to ground. On the lower H742 power control board, the positive output pins are at ground and the negative output pins are used to provide a -15 Vdc output with respect to ground. This -15 V output is used by the M8110 SMC modules.

When DC LO 1 (or DC LO 2) is grounded at pin 9, Q2 conducts hard and cuts off Q1 completely, thus removing the +15 V and +8 V outputs.

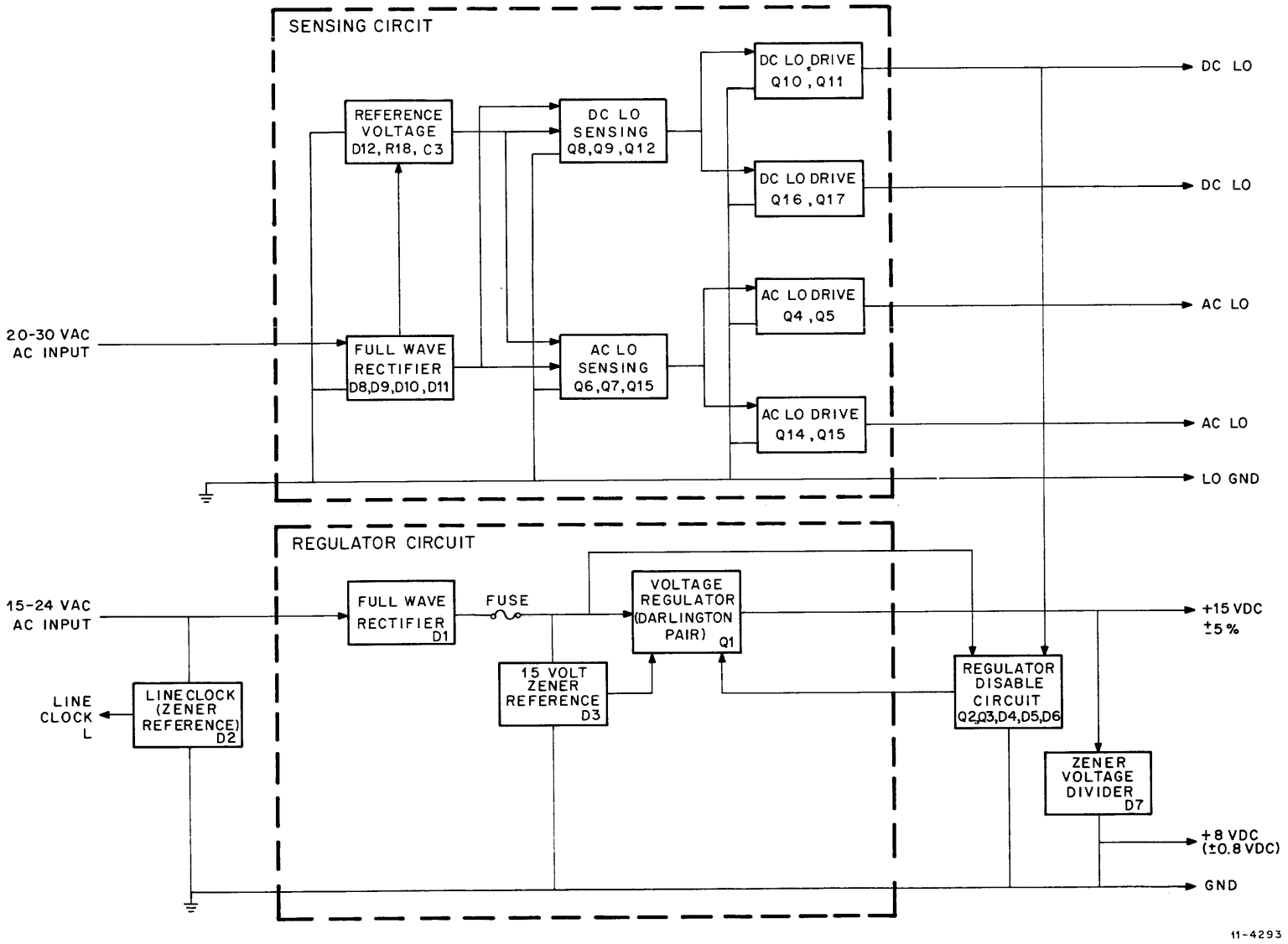


Figure 5-11 5409730 Block Diagram

Line Clock Output – The clock output (LTC L) is derived from one leg of full-wave rectifier bridge D1, by voltage divider R10 and R11, and Zener diode D2 (drawing C-CS-5409730-0-1). The clock output is a 0 to +5 V square wave, at the frequency of the power source (47 to 63 Hz). The clock output is used to drive the KW11-L line frequency and KW11-P real-time clock options.

AC LO and DC LO Circuits – A 20–30 Vac input from the secondary of transformer T1 is applied to the AC LO and DC LO sensing circuits on each of the H742 power control boards. The sensing circuits are shown on drawing C-CS-5409730-0-1. The ac input is rectified by diodes D8 through D11, and filtered by capacitor C3. A common reference voltage is derived by resistor R18 and Zener diode D12. Both sensing circuits operate similarly; each contains a differential amplifier, a transistor switch, and associated circuits. The major difference is that the base of Q6 in the AC LO circuit differential amplifier is at a slightly lower value than that of Q9 in the DC LO differential amplifier. The operation of both sensing circuits depends on the voltage across capacitor C3.

For AC LO sensing, the 20–30 Vac input is rectified and stored in capacitor C3, which will charge and discharge at a known rate whenever the ac power is switched on or off. Thus, the voltage applied to the emitters of differential amplifier Q6/Q7 through R17 is a rising or falling waveform of known value. For example, when power fails or is shut down, the dc voltage decays at a known rate, as determined by the RC time constant. If the voltage decreases to the point where the base of Q6 becomes negative with respect to the base of Q7, the increased forward bias on Q6 causes it to conduct more, and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Q5 and Q4 to conduct. The AC LO line at pin 8 is grounded. An extra AC LO line (AC LO X on pin 10) is also grounded by the similar switching of transistors Q15 and Q14.

AC LO 1 is applied through the cable harness and CPU backplane to the power fail initialize logic shown on drawing UBCE. The mnemonic assigned to the input is BUSA AC LO L. AC LO 2 is applied through the cable harness to the Unibus B terminator as BUSB AC LO L. The AC LO outputs from the upper and lower H742 power supplies are interconnected for use in multiprocessor systems.

A regulator disable circuit is also provided that disables the regulator outputs when a DC LO is detected. (AC LO may also trigger a disable since it eventually generates a DC LO.) The regulator disable circuit consists of Q2, Q3, and associated circuitry. When a DC LO is generated, Q3 is biased on which turns on Q2. This disables the regulator by turning off Q1 and clamping the output to ground through D4 and R5.

The DC LO sensing circuit operates in a manner similar to that described for AC LO. The difference between these circuits is the voltage level at which they trip. For example, if the ac input starts to decrease, as a result of a power failure or shutdown, the AC LO lines are grounded before the DC LO lines. As power is restored, the ground is removed from the DC LO lines before it is removed from the AC LO lines. A description of how the AC LO and DC LO control signals are used in the KB11-A, D is provided in the *KB11-A, D Central Processor Unit Maintenance Manual.*

DC LO 1, generated by the switched H742 power control board, is applied to the power fail initialize logic shown on drawing UBCE as input BUSA DC LO L. DC LO 2, generated by the unswitched H742 power control board, is applied to the Unibus B terminator module as BUSB DC LO L. A DC LO X output from the lower H742 power supply is applied to the M8110 SMC modules.

AC LO and DC LO indicate the status of the associated H742 bulk supply, as described in the preceding paragraphs. These signals are not affected by the outputs of the individual voltage regulators.

Figure 5-12 shows the H742 power-up and power-down sequences.

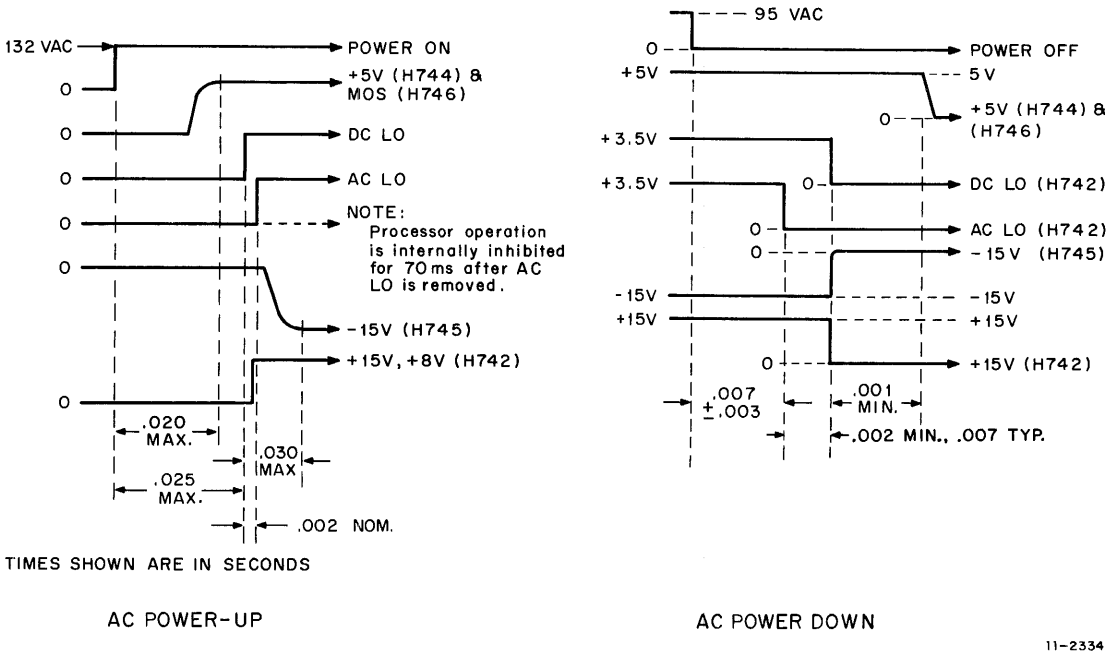


Figure 5-12 H742 Power-Up and Power-Down Sequences

5.2.3 H744 +5 V Regulator

From three to eight H744 +5 V regulators are used in the PDP-11/45, 11/50, 11/55 power system, depending on the system configuration (drawing D-CS-H744-0-1).

Regulator Circuit – The 20–30 Vac input is full-wave rectified by bridge D1 to provide a dc voltage (24 to 40 Vdc, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 5-13. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, error amplifier series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, predrivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15 V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary because the raw input voltage is well above that required for E1 operation. This +15 V input is supplied while still retaining the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

The output circuit is standard for most switching regulators and consists of free-wheeling diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free-wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, thus providing a discharge path for L1. (Circuit and waveforms are similar to those of Figure 5-9.)

In operation, Q2 is turned on and off, generating a square wave of voltage that is applied across D5 at the input of the LC FILTER (L1, C8, and C9). Basically, this filter is an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, thus supplying regulation. The output voltage is sensed and fed back to E1 where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on and off, according to whether the output voltage level decreases or increases. Defined upper and lower limits for the output are approximately +5.05 V and +4.95 V.

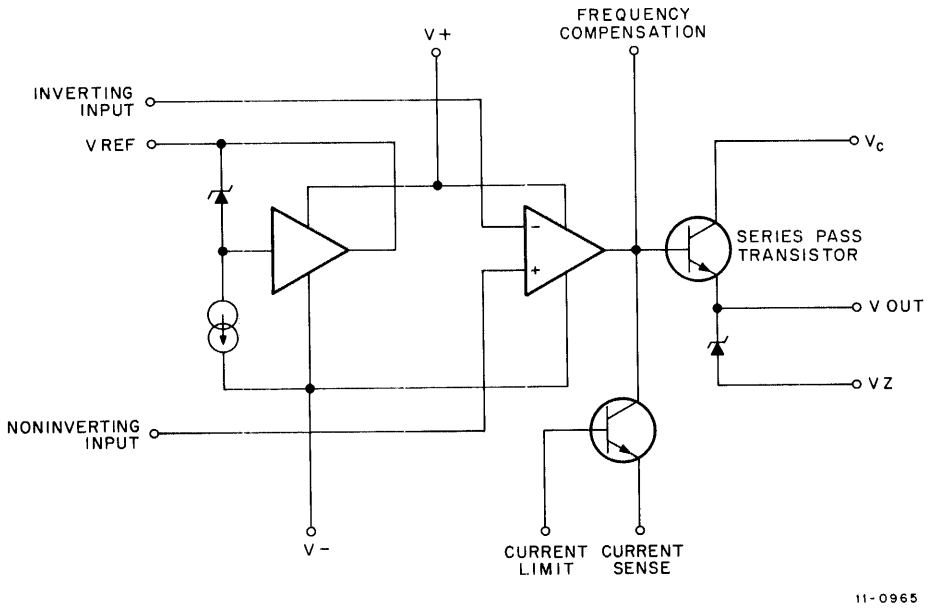


Figure 5-13 Voltage Regulator E1, Simplified Diagram

During one full cycle of operation, the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +5 V level, then a constant +25 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current, causing the output level (+5 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +5.05 V, E1 shuts off turning Q2 off; the emitter of Q2 is then clamped to ground. L1 discharges into capacitors C8, C9, and the load. Predrivers Q3 and Q4 are used to increase the effective gain of Q2, thus ensuring that Q2 can be turned on and off in a relatively short period of time.

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95 V will be reached, causing E1 to turn on; E1, in turn, causes Q2 to conduct, beginning another cycle of operation.

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05 V) and minimum (+4.95 V) values by E1. When +5.05 V is reached, E1 turns Q2 off; when +4.95 V is reached, E1 turns Q2 on. This type of circuit action is called a *ripple regulator.*

+5 V Overcurrent Sensing Circuit – The overcurrent sensing circuit consists of: Q1, R3 through R6, R25, R26, programmable unijunction Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30 A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the gate of Q7, Q7 turns on and E1 will be biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35 A (approximately) and that the regulator is short circuit protected. The regulator continues to oscillate in this new mode until the overload condition is removed. C4 then discharges until E1 is again allowed to turn on and the cycle repeats.

+5 V Overvoltage Crowbar Circuit – The following components comprise the overvoltage crowbar circuit: Zener diode D3, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across Zener diode D3 is less than 5.1 V. If the output voltage becomes dangerously high (above 6.0 V), diode D3 conducts, and the voltage drop across R23 draws gate current and triggers the SCR. The SCR fires and short circuits the +5 V output to ground.

5.2.4 H745 -15 V Regulator

According to the power requirements of the particular PDP-11/45, 11/50, 11/55 system configuration, one or two H745 -15 V regulators may be included in the power system. Operation of the H745 is basically the same as that of the +5 V regulator (drawing C-CS-H745-0-1). Input power (20 to 30 Vac) is taken from the transformer secondary and input to full-wave bridge D1, whose output is a variable 24 to 40 Vdc input across capacitor C1 and resistor R1.

-15 V Regulator Circuit – Regulator operation is almost identical to that of the +5 V regulator; however, the +15 V input that is required for E1 operation is derived externally and is input across capacitor C2 to E1, and the inverting and noninverting inputs to E1 are reversed. In addition, the polarities of the various components are reversed. For example, Q5, which is used as a "level shifter," is an NPN transistor on the +5 V regulator; whereas a PNP is required on the -15 V regulator, thus allowing the regulator to operate below ground (at -15 V).

Under normal operating conditions, regulator operation centers around linear regulator E1 and pass transistor Q2, which is controlled by E1. Predetermined output voltage limits are -14.85 V minimum and -15.15 V maximum. When the output reaches -15.15 V, E1 will shut off, turning Q2 off, and L1 discharges into C8 and C9. When the output reaches -14.85 V, E1 will conduct, causing Q2 to turn on, thus increasing the output voltage.

-15 V Overcurrent Sensing Circuit – The -15 V regulator overcurrent sensing circuit is basically made up to the same components used in the +5 V regulator, except Q1 is an NPN transistor in the -15 V regulator. Q1 is normally not conducting; however, once the output exceeds 15 A, Q1 will turn on and C3 will charge. When C3 reaches the same value as the gate of Q7, E1 will be biased off, which turns Q2 off, thereby stopping current flow and turning the -15 V regulator off. Thus, the regulator is short circuit protected.

-15 V Overvoltage Crowbar Circuit – When SCR D5 is fired, the '5 V output is pulled up to ground and latched to ground until input power or the +15 V input is removed. A negative slope on the +15 V line can be used to trip the crowbar for power-down sequencing, if desired.

5.2.5 H746 MOS Regulator

If the particular PDP-11/45, 11/50 system configuration contains MOS memory, the MOS regulator must be included in the PDP-11/45, 11/50 power system. The MOS regulator supplies regulated outputs of -5, +19.7, and +23.2 Vdc. Basic MOS regulator operation and circuitry is similar to that of the +5 V regulator; however, major differences do exist between the input and output circuitry of the two (+5 V and MOS) regulators, because a higher input voltage is required in the MOS regulator, and multiple outputs of -5 V, +19.7 V, and +23.2 V are supplied by the regulator (drawing C-CS-H746-0-1).

Regulator Circuit – As in the +5 V and -15 V regulators, operation of the MOS regulator centers around E1, pass transistor Q2, predriver Q3 and level shifter Q5. The input uses a voltage doubler as opposed to the full-wave diode bridge used in the +5 V and -15 V regulator. This is necessary because the +23 V output requires a much higher input voltage (48 to 80 Vdc) to ensure the circuit operates efficiently. The remaining regulator components are identical to those of the +5 V regulator except that the individual components are selected to operate at the higher voltage levels.

The output circuitry contains additional components to yield the required multiple outputs of -5, +19.7 and +23.2 Vdc. Transistor Q6 is a Darlington power amplifier that is employed as a linear pass transistor to drop the +23.2 Vdc down to +19.7 Vdc. This is necessary because a constant 3 to 4 V difference in the two voltages is required in MOS memory operation. All of the current drawn by the +23.2 and +19.7 V outputs is fed back to the rectifier source via the ground line, through Zener diode D10, to yield the -5 Vdc output from the anode of D10.

Overcurrent Sensing Circuit - The overcurrent sensing circuit, consisting of Q1, R4 through R7, Q8, R29, and C3, operates in exactly the same manner as in the +5 V regulator.

Overvoltage Crowbar Circuit - The overvoltage circuit consists of D7 through D9, Q7, and associated circuitry, and operates in exactly the same manner as the +5 V regulator crowbar circuit.

5.2.6 H754 +20, -5 V Regulator

If the system contains an option requiring +20 and -5 V, such as the MF11-U/UP, H754 regulator(s) must be added. They are mounted into slot E of the PDP-11/45, 11/50, 11/55 cabinet or into slots D and/or E of an expanded cabinet.

Regulator Circuit - The circuit (schematic D-CS-H754-0-1) is similar to that of the other regulators: like the H746, it has a voltage doubler input, but the output consists of two shunt regulator circuits, one for the +20 V, the other for the -5 V. The +20 V shunt regulator consists of transistors Q4, Q10, and Q11; the -5 V shunt regulator, of Q6 and Q9. Q10 and Q9 are the pass transistors.

The output of the basic regulator is 25 V (-5 to +20 V). The shunt regulators are connected across this output, with a tap to ground between the pass transistors Q9 and Q10. The voltage at the bases of Q6 and Q4 will vary with respect to ground, depending on the relative amount of current drawn from the +20 V and -5 V outputs of the regulator. If the +20 V current increases while the -5 V current remains constant, the output voltage at the +20 V output will tend to go more negative with respect to ground; this will cause the -5 V output to go more negative also, since the output of the basic regulator is a fixed 25 V. This change is sensed at the bases of Q6 and Q4: Q6 will conduct, causing Q9 to conduct also, thus increasing the current between -5 V and ground until the balance between the +20 V and the -5 V is restored. At this time, neither Q6 nor Q4 will be conducting. If the -5 V current increases, Q4 and Q10 will conduct to balance the outputs.

Overvoltage Crowbar Circuits - There are two crowbar circuits in the H754: Q7 and its associated circuitry for the +20 V, and Q12 and its circuitry for the -5 V. Either one will trigger SCR D9.

Overcurrent Sensing Circuit - The overcurrent circuit is comprised of Q1, Q8, Q13, Q14, and associated circuitry. the total peak current is sampled through R4. When the peak current reaches approximately 14 A, Q1 turns on sufficiently to establish a voltage across R7 and R38, thus firing Q8. This pulls the voltage on pin 4 of the 723 up above the reference voltage on pin 5, thereby shutting off Q2. D6 now conducts, and the current through R37 turns on Q14, which turns on Q13. This keeps Q8 on for a time which is determined by the output voltage and L1. This action, in turn, allows the off-time of Q2 to be greater than the on-time; the off-time increases as the overload current increases, thereby changing the duty cycle in proportion to the load. The output current is thus limited to approximately 10 A.

Voltage Adjustment - The +20 V adjustment is located on the side of the H754; and the -5 V potentiometer is on the top, next to the connector. To set the output voltages: power down, disconnect the load, power up, adjust for a 25 V reading between the +20 and -5 V outputs with the 20 V potentiometer. Then set the -5 V between its output and ground. Power down, reconnect the load, power up and then check and adjust the outputs again. This procedure is necessary because the +20 V potentiometer (R17) actually sets the overall output of the regulator (25 V from +20 to -5 V), while the -5 V adjustment (R21) controls the -5 V to ground output. (See schematic drawing D-CS-H754-0-1)

CHAPTER 6
MAINTENANCE

PDP-11/45, 11/50, 11/55 maintenance procedures are divided into two categories: preventive maintenance and corrective maintenance. Corrective maintenance should be performed to isolate a fault or malfunction and to make necessary adjustments and/or replacements. Using diagnostic programs that test the functional units of the system and special calibration and test procedures aid in performing corrective maintenance.

This chapter contains the following sections:

6.1 MAINTENANCE EQUIPMENT REQUIRED

Maintenance procedures for the PDP-11/45, 11/50, 11/55 require the standard equipment (or equivalent) listed in Table 6-1.

Generally the voltage regulators are not field repairable. However, guidelines are given in Paragraph 6.3.3 for depot or factory repairs.

6.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks performed periodically to prevent failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failure resulting in module replacement on a projected module or component reliability basis.

Table 6-1 Maintenance Equipment Required

Equipment or Tool	Manufacturer	Model, Type or Part No.	DEC Part No.
Oscilloscope	Tektronix	453*	
Digital Voltmeter (DVM)	Weston (or the like)	6000	
Volt/Ohmeter (VOM)	Triplett		29-13510
Unwrapping Tool	Gardner-Denver (DEC Catalog #H812A)	505 244-475	29-18387
Hand Wrap Tool	Gardner-Denver (DEC Catalog #H811A)	A-20557-29	29-18301
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-19551
Miniature Needle Nose Pliers	Utica	23-4-1/2	29-13462
Wire Strippers	Millers	101S	29-13467
Solder Extractor	Solder Pullit	Standard	29-13451
Soldering Iron (30W)	Paragon	615	29-13452
Soldering Iron Tip	Paragon	605	29-19333
16-Pin IC Clip	AP Incorporated	AP923700	29-10246
24-Pin IC Clip	AP Incorporated	AP923714	29-19556
Maintenance Cards	DEC		W131, W133**
Maintenance Card Overlay	DEC		5509974-0-1
Module Extender Boards (3)	DEC		W900

* Tektronix Type 453 Oscilloscope is adequate for most test procedures; Type 454, or equivalent, may be required for some measurements.

** W133 is a dual version of W130. It provides the drivers for two W131 maintenance cards.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to environmental conditions at the particular installation site. Mechanical checks should be performed as often as required to enable fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 1000 operation hours or every three months, whichever occurs first. Appendix B is a suggested preventive maintenance schedule for peripheral equipment.

6.2.1 Physical Checks

The following is a list of the steps required for mechanical checks and physical care of the PDP-11/45, 11/50, 11/55:

1. Check all fans to ensure that they are not obstructed in any way. Vacuum-clean the air vents of the upper and lower logic fan housings, and upper and lower regulator fan housings. Remove and wash the filters in the cabinet fan, located in the top of the cabinet.

2. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

3. Inspect the following for mechanical security: lamp assemblies, jacks, connectors, switches, power supply regulators, fans, capacitors, etc. Tighten or replace as required.

4. Inspect all module mounting panels to ensure that each module is securely seated in its connector and the locking-releasing mechanism is working properly.

5. Inspect power supply capacitors for leaks, bulges, or discoloration, and replace as required.

6. Inspect module guides for wear, damage, and secure fastening.

6.2.2 Electrical Checks and Adjustments

6.2.2.1 Regulator Voltage Checks – Perform the power system checks listed in Table 6-2. Use a volt/ohmeter (VOM) to check the output voltages under normal load conditions. Use an oscilloscope to measure the peak-to-peak ripple content on all dc outputs. Each voltage regulator has an adjustment potentiometer located just below the output indicator lamp (indicator lamp not present on earliest versions). If the regulator output is not within the specified tolerance, adjust as required to obtain an acceptable output. If a voltage regulator cannot be adjusted to meet specifications, remove and replace the regulator. (See Paragraph 6.3.3.)

6.2.2.2 Power Control – Operate the REMOTE/OFF/LOCAL switch S1 on each power control to ensure that power is turned on in the LOCAL position and disconnected in the OFF position. Return S1 to its original position after performing this test. On early systems equipped with two 860 power controls, the upper 860 S1 should be set to REMOTE, the lower 860 S1 to LOCAL. Figure 1-2 shows which 860 power control is associated with each H742 power supply.

6.2.2.3 AC Power Connector Receptacles – Test the output voltage at each plug to ensure that 115 or 230 Vac is available.

6.2.3 Timing Margins

A preventive maintenance timing margin chart is provided at the back of this manual. The timing margin chart can be used to maintain a record of margin test results. Such a record of timing variations over a period of time will serve to point out any deterioration in system timing margins and indicate when corrective maintenance may be required to prevent a system failure.

Paragraph 6.5 describes how to use the maintenance cards to vary the CPU and FPP RC clocks to perform timing margin tests on the CPU and FPP. As each diagnostic program listed on the preventive maintenance timing margin chart is run, vary the appropriate RC clocck to determine the minimum and maximum clock speed at which the program fails. Nominal margins are 28–50 ns for the KB11-A, 27–450 ns for the KB11-D, and 50–290 ns for the FP11-B at 70° F. Refer to the note in Paragraph 6.5.1. Record these speeds on the chart for each test. In the space provided above each entry, record the date of the preventive maintenance procedure.

NOTE

Appendix B provides a table of peripheral preventive maintenance schedules.

Table 6-2 CPU DC Output Voltage Checks

Output	Measure at CPU Backplane Pin	Voltage	Max. Ripple Peak-to-Peak V
H744 +5V Regulator (slot A)	A02A2	+5.0	0.15
H744 +5V Regulator (slot B)	A06A2	+5.0	0.15
H744 +5V Regulator (slot C)	A10A2	+5.0	0.15
H744 +5V Regulator (slot D)	A26A2	+5.0	0.15
H744 +5V Regulator (slot H)	A19A2 (Bipolar)	+5.0	0.15
H744 +5V Regulator (slot J)	A16A2	+5.0	0.15
H744 +5V Regulator (slot K)	A21A2	+5.0	0.15
H744 +5V Regulator (slot L)	A24A2	+5.0	0.15
H745 -15V Regulator (slot E)	E02B2	-15.0	0.45
H746 MOS Regulator (slot H)	A17V2	+23.2	0.70
*(slot L)	A22V2		
H746 MOS Regulator (slot H)	A17U2	+19.7 (3–4V less than +23.2)	0.60
*(slot L)	A22U2		
H746 MOS Regulator (slot H)	F17C1	-5.0	0.15
Switched H7420 P.S.	E15A1	+15.0 (13.5–16.5)	0.45
Switched H7420 P.S.	E01B1	+8.0 (6.8–9.2)	0.24

*Revision F and higher.

6.2.4 General Diagnostic Testing

Run all applicable diagnostic programs listed in Paragraph 6.4 for a minimum of one complete pass, or three minutes, whichever is longer, to ensure that no machine problems exist that were not detected in the timing margin tests.

6.3 POWER SYSTEM MAINTENANCE

WARNING
Dangerous voltages (115 or 230 Vac) are present in the power system! Be careful when servicing these circuits.

6.3.1 Circuit Tracing

A thorough knowledge of the location and operation of the various components of the PDP-11/45, 11/50, 11/55 power system is essential for troubleshooting this system. The drawings and text of Chapters 3 (Power System), 4 (AC Power) and 5 (DC Power) of this manual, in conjunction with the schematics listed below should provide all the necessary information in this respect.

H7420 Power Supply	D-CS-H7420-0-1
H742 Power Supply	D-CS-H742-0-1
H7420 Power Control Board	C-CS-5411086-0-1
H742 Power Control Board	C-CS-5409730-0-1
H744 +5 V Regulator	D-CS-H744-0-1
H745 -15 V Regulator	D-CS-H745-0-1
H746 MOS Regulator	D-CS-H746-0-1
H754 +20, -5 V Regulator	D-CS-H754-0-1
PDP-11/45 Console Board	D-CS-5409684-0-1 (drawing KNLC)
861 Power Control	D-CS-861-A-1, -B-1, or-C-1
860 Power Control	D-CS-860-0-1, -A-1

6.3.2 Visual Aids to Troubleshooting

If a power system fault is suspected, visually inspect the system components for obvious fault indications. For example, each of the voltage regulator modules is provided with an output indicator lamp that lights when the output voltage is within range. If a single indicator lamp within the group (A-E or H-L) is not lit, the fault is probably within that voltage regulator module. In the case of the H744 +5 V regulator, this can be verified by swapping H744 modules. (See Paragraph 6.3.3.) Once the fault has been isolated to a voltage regulator module, refer to the voltage regulator checkout procedure described in Paragraph 6.3.3. A decal is placed on the rear of the BA11-FA chassis to indicate the location and function of each voltage regulator. (See Figure 5-7.)

If none of the voltage regulator output indicator lamps in the group are lit, the fault is probably in the associated power supply or power control. Visually inspect the power indicator lamps and circuit breakers provided with these components to determine whether the fault can be isolated to either the H7420 or the power control. Figures 4-6, 4-7, and 4-8 show where these indicator lamps and circuit breakers are located (electrically) in each component. A description of the power controls is given in Paragraph 4.2.

The following steps can be used to aid in locating the cause of a power system failure in a system using an H7420 power supply and an 861 power supply control. Similar steps can be used for earlier power system versions.

1. Ensure that the H7420 is plugged in and getting primary power (115/230 Vac) from the 861 power control.

2. Check the power indicator and circuit breaker CB1 on the H7420.

3. Check the individual regulator lights. (Regulator lights are lit during normal operation.)

4. Check the two LEDs on the 5411086 power line monitor. They should be on during normal operation. The first two steps of the 5411086 removal procedure (Paragraph 6.3.4.4) must be performed in order to view the two indicators.

5. Measure regulator voltages at the processor backplane (Paragraph 6.2.2.1 and Table 6-2).

6. If all regulator outputs are within specifications, check the backplane for faulty wiring.

7. If one or more regulator outputs are incorrect, check the regulator fuse(s), the transformer assembly, the power harness connections, and the load.

8. If the +8 V, -15 V, or +15 V outputs are incorrect, check the 5411086 power line monitor.

9. If the fault is isolated to a voltage regulator, refer to Paragraphs 6.3.3 and 6.2.2.1 for regulator troubleshooting and adjustment procedures.

6.3.3 Voltage Regulator Test Procedures

This paragraph suggests procedures to troubleshoot and test the H744 +5 V regulator, H745 -5 V regulator, H746 MOS regulator, and H754 +20 -5 regulator modules. The procedures are intended to aid in locating a fault, provided the fault has not destroyed the etched circuits.

When replacing a faulty voltage regulator, the new voltage regulator may need adjustment to compensate for the load. In some instances, if the new regulator is initially adjusted too high, it may activiate the crowbar circuit and therefore provide no output when initially installed. If this happens, turn power off and rotate the adjustment potentiometer counterclockwise. Then reapply power (regulator should not crowbar) and adjust the regulator output.

6.3.3.1 Initial Tests – When a power system fault has been isolated to a voltage regulator, examine internal fuse F1. A blown fuse usually indicates that the main pass transistor Q2 and/or one of its drivers Q3 and Q4 has short-circuited.

1. Check for damage to base-emitter bleeder resistors and scorched etched board in the area of Q3 (and Q4 if applicable).

2. If the pass transistor and drivers check OK on a VOM, the fault may be caused by continuous base drive to the first driver Q4 (Q3 in H754). Check level shifter Q5 for a short-circuit.

3. Check the resistance to ground at the input to the precision voltage regulator integrated circuit E1 (pins 4 and 5) to determine if an external short-circuit is holding the IC in conduction.

4. Use the VOM to check for short-circuit between fuse terminals and ground. Possible short-circuit involving mounting TO-3 conponents to the heat sink may be located by connecting VOM leads between TO-3 cases and a regulator bracket mounting screw on the end of the heat sink.

6.3.3.2 Output Short-Circuit Tests – A voltage regulator that provides no output, or low output, without causing fuse F1 to blow is probably working into a short-circuited output.

NOTE

An activated crowbar or a short-circuited output in an otherwise properly operating voltage regulator will not cause F1 to blow.

1. If fuse F1 is not blown, and the area of etched circuit around the ac input to the bridge circuit is not damaged, it is safe to apply an ac input to the voltage regulator to determine if the regulator is overloaded by a short-circuit across the output.

2. Connect the voltage regulator to a test bench source and advance the Variac to about 90 V. If the output is near 0 V, turn the voltage adjustment fully counterclockwise and repeat the test.

3. If the regulator appears overloaded, check for short-circuit across the output and for a component failure in the crowbar circuit.

6.3.3.3 Testing a "Dead" Regulator – Use the following procedure to test a faulty voltage regulator that does not exhibit the symptoms described above.

1. Apply 115 Vac to the test bench source (25 Vac at the voltage regulator input), with no load on the regulator output.

2. Check for f30 Vdc across filter capacitor C1 (and C2 if applicable).

3. Check for +15 Vdc at pin 12 of precision voltage regulator E1. No voltage at this point could mean Zener diode D2 (H744) or D3 (H746 or H754) has failed.

4. Check for 6.8–7.5 Vdc at pin 6 of E1 with respect to ground, pin 7.

5. If all voltage measurements in Steps 2, 3, and 4 are OK and there is no output voltage, pin 5 of E1 should be positive with respect to pin 4.

   E1, pin 2 should be +0.6 V with respect to pin 3. If it is not, connect emitter and base of Q5 together. If 0.6 V indication is obtained, precision voltage regulator E1 is OK and the fault probably is caused by Q5 or Q4 (Q3 in H754).

6.3.3.4 Testing a Voltage Regulator After Repairs – Before returning a repaired voltage regulator to service, it should be checked as follows:

1. Connect the repaired voltage regulator to the appropriate source connector.

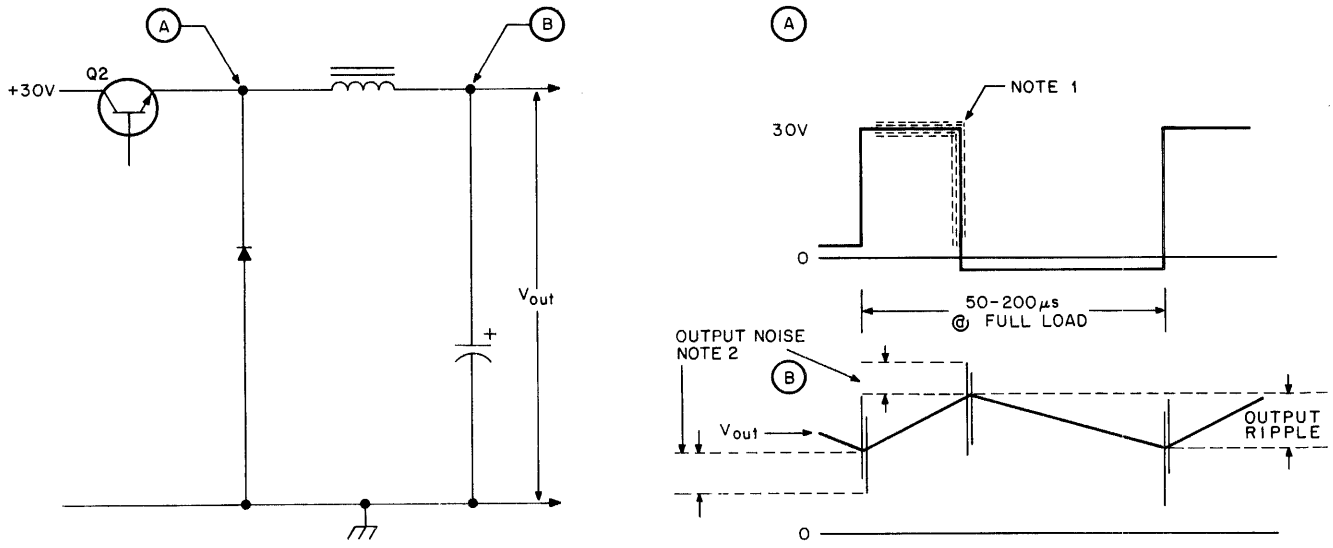
2. Set the voltage adjustment fully counterclockwise and set the load to zero.

3. Close the input circuit breaker and advance the Variac until output voltage is indicated (at approximately 60–80 Vac input). No audible noise should be heard under no-load conditions.

4. Be sure Q2 is connected and soldered before loading the regulator.

5. Advance the Variac to 130 Vac and return to 115 Vac.

6. Apply a 30–50 percent load. The output voltage should remain nearly constant. A clean whistle may be heard. A buzz or a harsh hissing sound indicates possible instability. Check waveforms as indicated in Figure 6-1.



NOTE 1: 30 volt level shifts with AC input voltage. Small 120Hz jitter is normal.

NOTE 2: Peak noise=1% max.

Measure noise with a short 100Ω terminated piece of foil coax. Normal 10:1 scope probe will not give an accurate noise measurement.

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Figure 6-1 Typical Voltage Regulator Output Waveforms (Maximum Output Ripple Is Specified in Table 5-3)

7. Apply 100 percent load and set the voltage adjustment for nominal output, as listed in the following chart:

H744	+5.10 Vdc
H745	-15.10 Vdc
H754	+25 Vdc between +20 and -5 V outputs.
H746	+23.2 Vdc. After this adjustment, the regulator should be slid out to allow access for the 19.7 Vdc adjustment.

8. Apply 200 percent load and check for a decrease in the frequency and the output voltage.

CAUTION

If the output voltage does not decrease noticeably (approximately 1 V on H744, or 1 to 5 V on the H745, H754, and H746), do not attempt the following short-circuit test.

9. Short circuit the output. The regulator should continue to operate at a low frequency with a clean, smooth whistle and stable waveforms.

10. Increase the voltage adjustment and observe the output voltage when the crowbar circuit fires. The output voltage should be within the following ranges:

H744	6.00--6.65 V
H745	16.8--20.5 V
H746	26.0--30.0 V
H754	25.0--30.0 V and -6.00 through -7.00 V

6.3.4 H7420 Power Supply Subassembly Removal and Installation Procedures

The power supply access procedure enables the supply to be accessed for adjustments and subassembly removal. The procedures listed below are described in the following paragraphs:

1. Power supply access procedure.
2. H744 regulator removal and installation.
3. 5411086 15 V regulator/power line monitor board removal and installation.

Removal and installation procedures are similar for the H742 power supply.

6.3.4.1 Power Supply Access Procedure

1. Power down the equipment.
2. Fully extend the processor frame from the rack, ensuring that the cables do not bind.
3. Remove the ac power connection by disconnecting the H7420 power cord from the 861 power control.

CAUTION
Since both H7420s are connected to the same 861, make certain that the correct H7420 power cord is disconnected.

6.3.4.2 H744 Regulator Removal

1. Perform the power supply access procedure described above.

WARNING
Power must be removed prior to removing regulators.

2. Disconnect the Mate-N-Lok connector from the regulator to be removed.
3. Remove the two screws and lockwashers that fasten the top of the regulator to the H7420 (Figure 6-2, Sheet 1 of 2). Loosen, but do not remove, the knurled screw that fastens the bottom of the regulator to the H7420.
4. Slide the regulator out of the H7420 (Figure 6-2, Sheet 2 of 2).

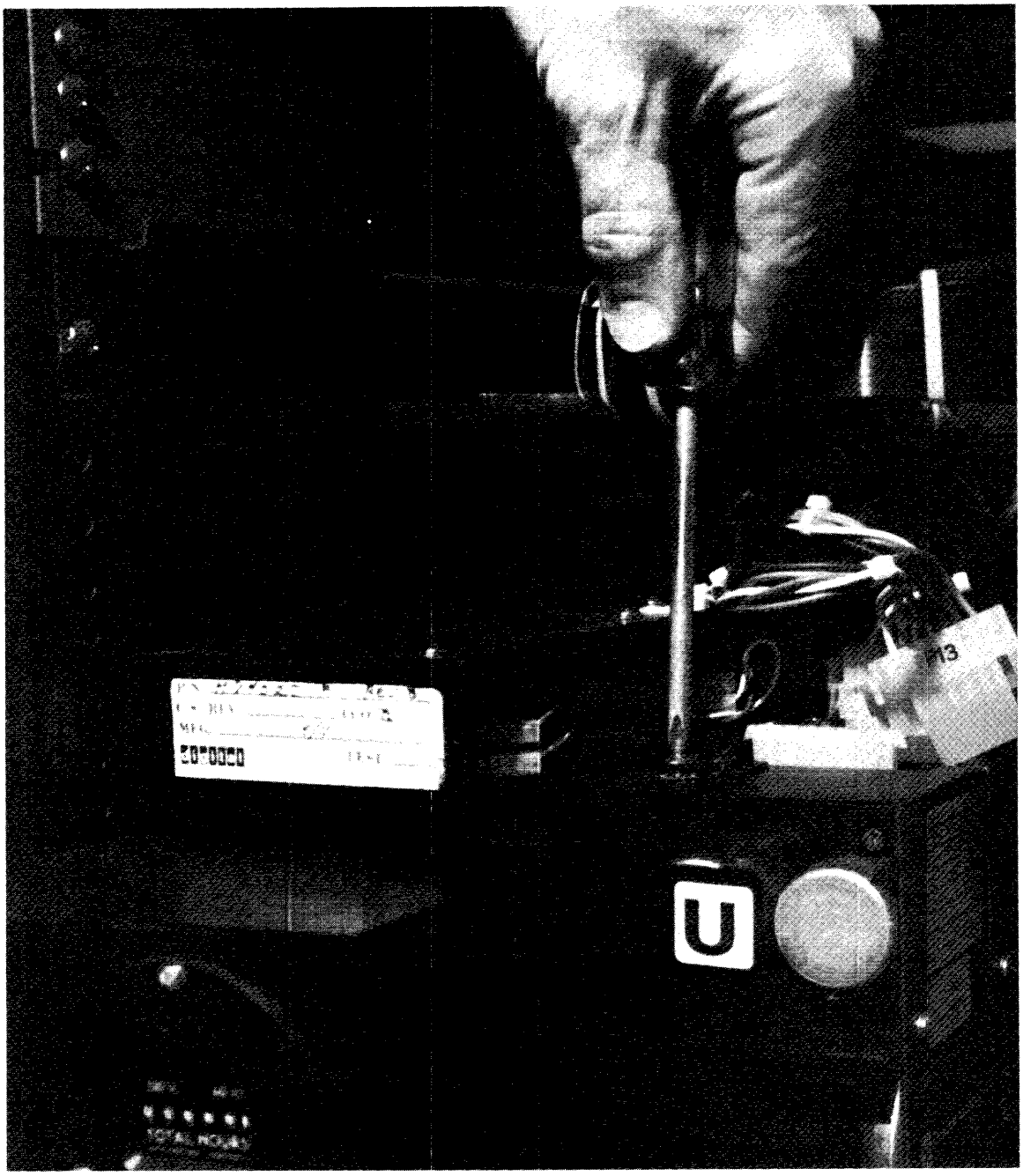

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Figure 6-2 H7420 Regulator Removal (Sheet 1 of 2)

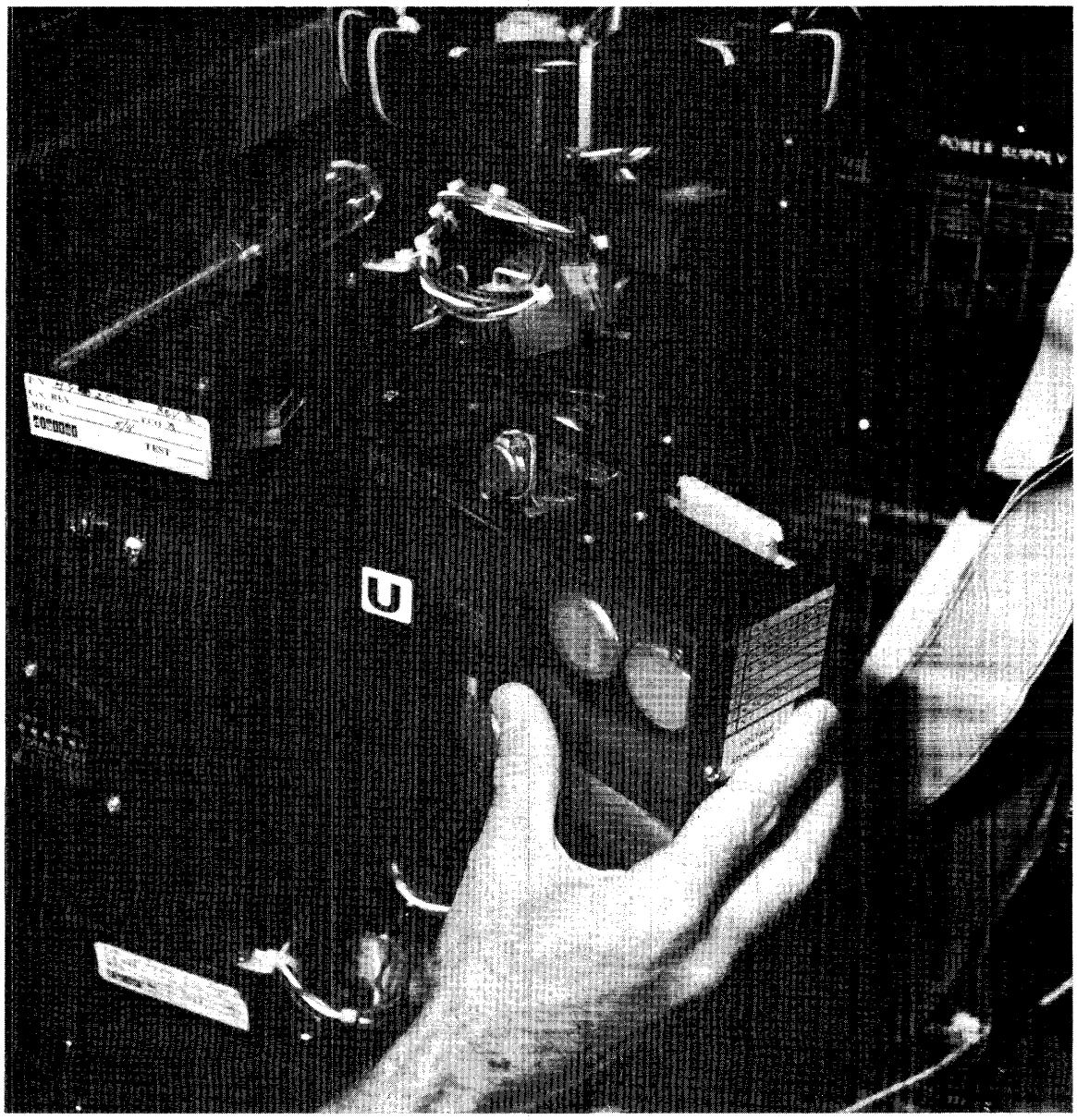

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Figure 6-2 H7420 Regulator Removal (Sheet 2 of 2)

6.3.4.3 H744 Regulator Installation – The following steps describe the procedure for installing H744 regulators in the H7420.

1. Perform the power supply access procedure (Paragraph 6.3.4.2).

WARNING
Power must be removed prior to installing regulators.

2. Place the H744 regulator in the correct position in the H7420. Tighten the knurled screw on the bottom of the H7420.

3. Fasten the top of the H744 to the H7420 with two screws and lockwashers.

4. Connect the Mate-N-Lok connector (in the power harness) for this regulator position to the connector on the top of the regulator.

5. Turn on power and measure the regulator voltage at the processor backplane (Paragraph 6.2.2.1). Adjust the voltage (Paragraph 6.2.2.1) if the measured voltage is not within the tolerances listed in Table 6-2.

6.3.4.4 5411086 15 V Regulator/Power Line Monitor Board Removal

1. Perform the power supply access procedures described in Paragraph 6.3.2.

WARNING
Power must be removed prior to removing the 5410086 board.

2. Remove the two screws at the top of the PC mounting board bracket (Figure 6-3, Sheet 1 of 3). The bracket then swings down from the top and remains suspended from the bottom edge.

3. Remove the two hex nuts from the end of the 5411086 board (Figure 6-3, Sheet 2 of 3). Do not lose the attached hardware (screws, washers, and spacers).

4. Remove the 5411086 board from the PC mounting board bracket. This is accomplished by carefully pulling the board to separate the edge connector on the board from J1 (Figure 6-3, Sheet 3 of 3).

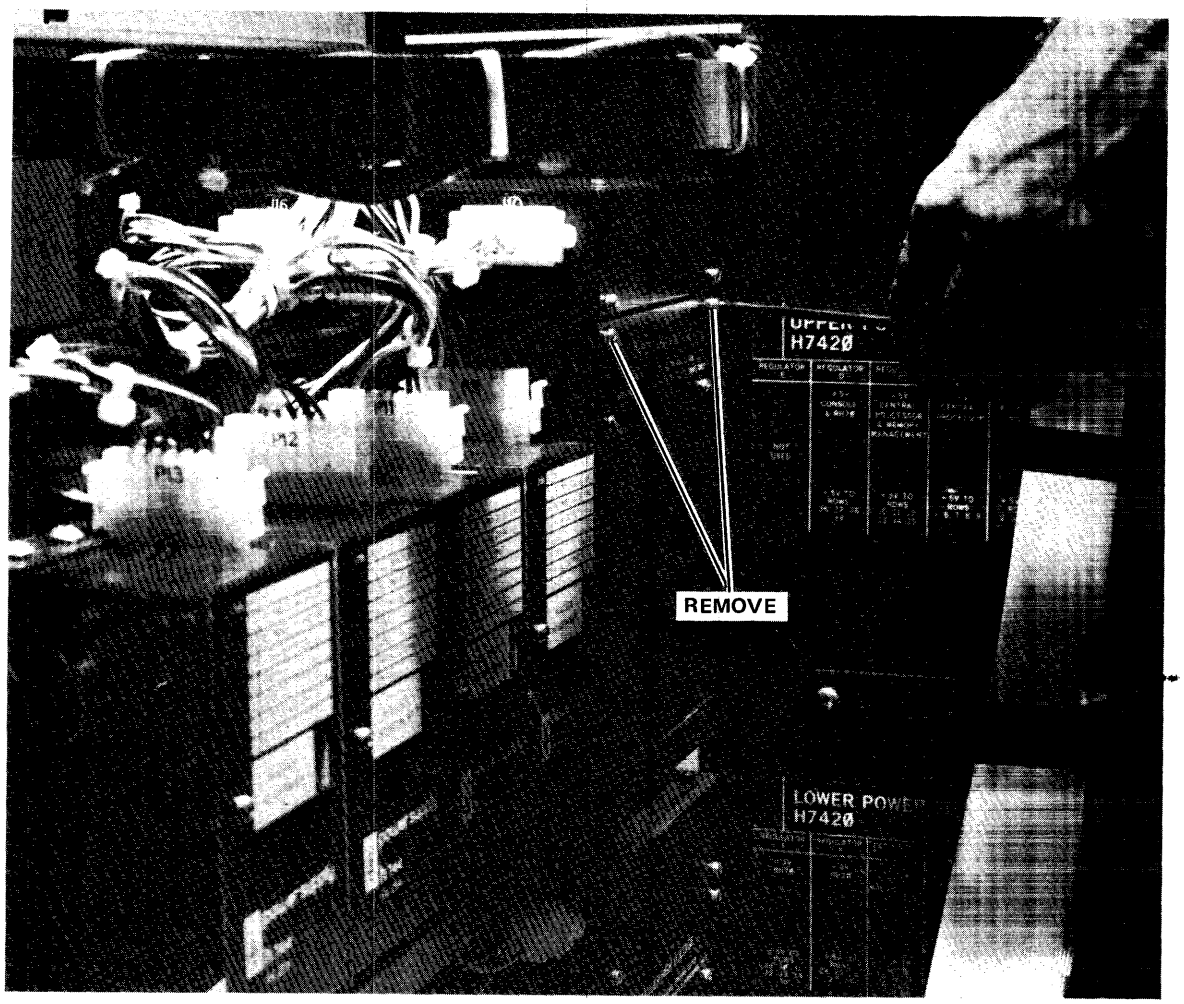

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Figure 6-3 5411086 Removal (H7420) (Sheet 1 of 3)

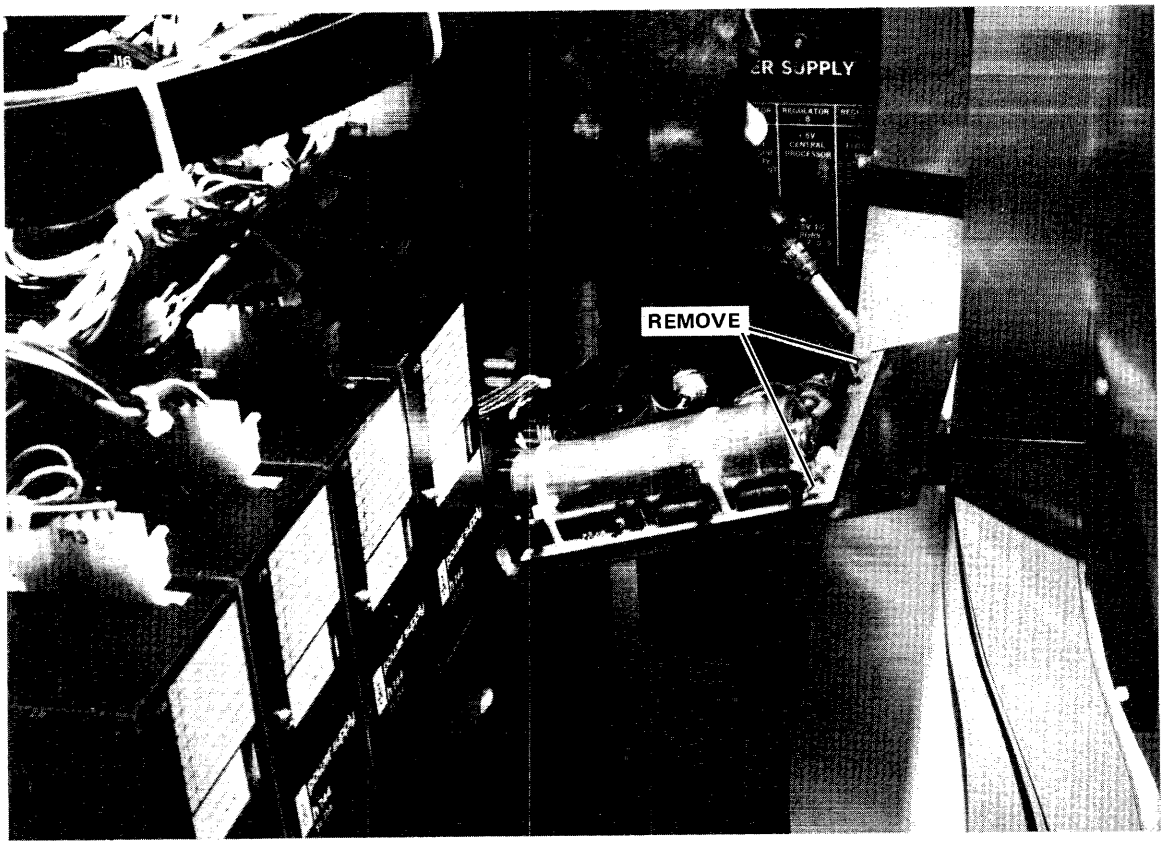

Figure 6-3 5411086 Removal (H7420) (Sheet 2 of 3)

6.3.4.5 5411086 15 V Regulator/Power Line Monitor Board Installation

1. Perform the power supply access procedure in Paragraph 6.3.4.2.

WARNING
Power must be removed prior to installing the 5411086.

2. Connect the edge connector on the 5411086 to J1. (Refer to Figure 6-15.)

3. Fasten the opposite end of the board to the PC mounting board bracket with the necessary hardware (screws, washers, spacers, and hex nuts).

4. Attach the top of the PC mounting board to the H7420 chassis with two screws and washers.

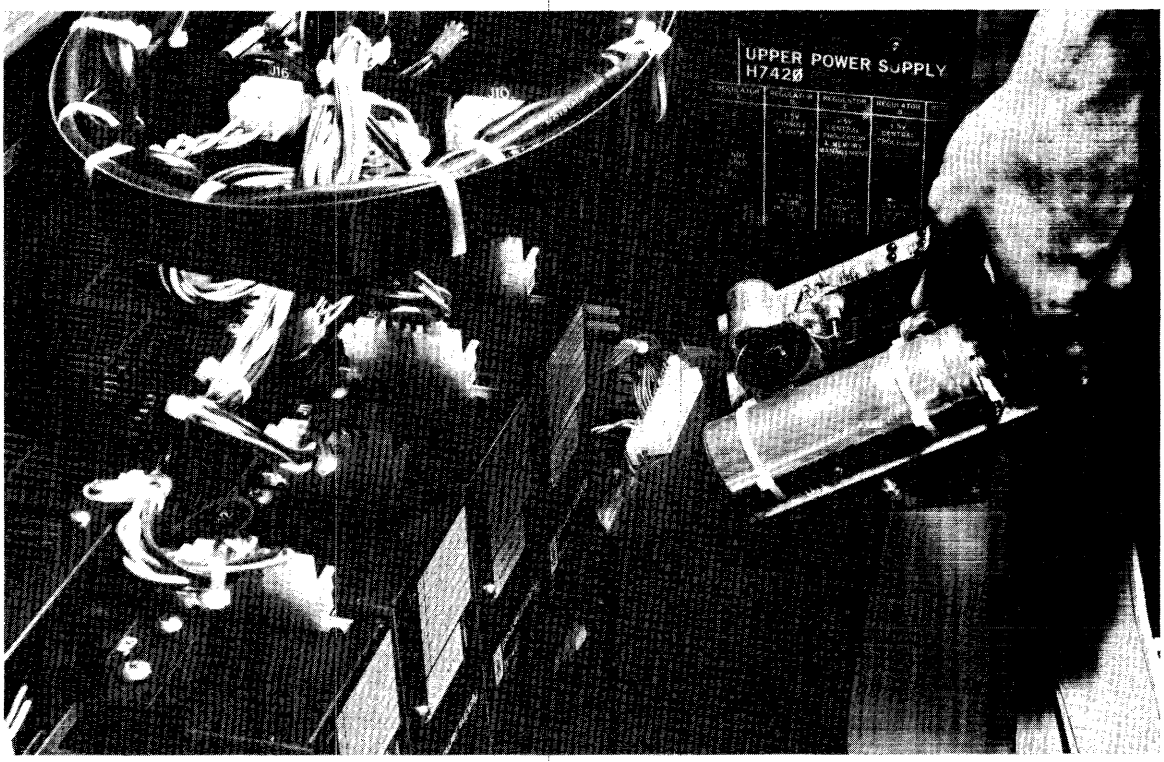

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Figure 6-3 5411086 Removal (H7420) (Sheet 3 of 3)

5. Turn on power and check the backplane voltages (upper H7420: +15 V and +8 V; lower H7420: -15 V). Refer to Paragraph 6.2.2.1 for 5411086 voltage check and adjustment procedures.

6. Power down the equipment.

7. Carefully push the processor frame into the cabinet, observing that the cables do not bind.

6.4 CPU MAINTENANCE

Maintenance of the PDP-11/45, 11/50, 11/55 CPU consists mainly of running diagnostic tests and making the adjustments, if any, that may be required.

The following groups of diagnostic programs are applicable for the basic PDP-11/45, 11/50, 11/55 system and options:

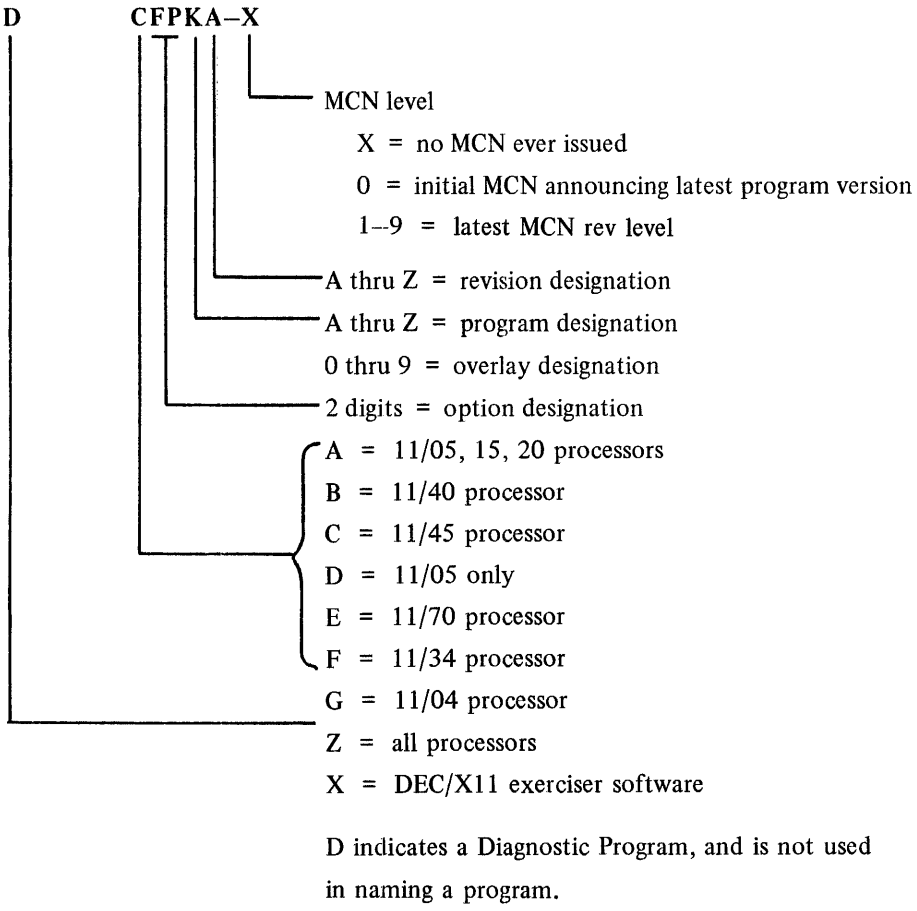
1. KB11-A, D Central Processor Unit Diagnostics
2. Memory System Diagnostics
3. FP11-B, C Floating-Point Processor Diagnostics
4. KT11-C, CD Memory Management Unit Diagnostics
5. KL11 Teletype Unit Diagnostics
6. KW11-L Line Clock Diagnostics

Diagnostic programs for all MF11 memory systems are listed in Paragraph 8.4; those for the MMS11, FP11, and KT11 options are described in Chapter 7.

Diagnostic programs for peripherals and I/O devices in the system are listed and described in their associated maintenance manuals. Detailed descriptions and specific operating procedures for each diagnostic program are provided in related diagnostic program description (MAINDEC) documentation. A *Libkit* lists all the diagnostics that are supplied with a particular piece of equipment.

The following program naming convention is now in use for MAINDECs.

Program Naming Convention 1 is a test written for the PDP-11/45 to test the FP11 option and is test number K version A.



Program Naming Convention 1

6.4.1 KB11-A, D CPU Diagnostics

In general, all diagnostic programs are loaded into the lowest 4K words of physical memory. All diagnostic programs start at address 200. The programs run in Kernel mode. If the KT11-C, CD option is implemented in the system it is disabled by clearing SR0 bit 0.

Any trap or interrupt vectors not used by the test in progress are set up as "trap catchers;" the new PC, stored in the first word of the vector, points to the second word of the vector, which contains a 0. When the 0 is fetched as an instruction, the processor interprets it as a HALT instruction. The instruction being executed when the trap occurred can be identified as follows:

1. Do a REG EXAM operation to determine the contents of register 6.

2. Set the number found in R6 in the switch register and do a LOAD ADRS operation.

3. Do an EXAM operation to determine the contents of the top word in the stack. This is the PC at the time that the false trap/interrupt occurred.

4. Set the same number minus two, four or six, depending upon addressing mode, into the switch register and perform a LOAD ADRS operation.

5. Perform a second EXAM operation to determine the instruction. This procedure will fail if the last instruction before the trap altered the PC.

Whenever an error is identified by a diagnostic program the program executes a HALT instruction. The location of the HALT identifies the type of error identified. To loop continuously through a particular test, replace the instruction following the HALT with a branch instruction to a location preceding the test – if possible, to a SCOPE instruction (if the test is failing consistently, the branch can replace the HALT instruction). The SCOPE instruction is a MOV PC, R1 (octal code 010701) in the DCKB tests. The later type of SCOPE provides a tag that identifies the last successfully completed subtest.

The diagnostic programs are listed in Table 6-3 in the order in which they are normally run.

Table 6-3 KB11-A, D Central Processor Unit Diagnostic Programs

Number	Tests
MAINDEC-11-DCKBA-	Sign extend instruction
MAINDEC-11-DCKBB-	Subtract one and branch instruction
MAINDEC-11-DCKBC-	Exclusive-OR instruction
MAINDEC-11-DCKBD-	Mark instruction test
MAINDEC-11-DCKBE-	Trap and interrupt return
MAINDEC-11-DCKBF-	Stack limit test
MAINDEC-11-DCKBG-	Set priority level instruction
MAINDEC-11-DCKBH-	Register test
MAINDEC-11-DCKBI-	Arithmetic shift instruction
MAINDEC-11-DCKBJ-	Arithmetic shift combined instruction
MAINDEC-11-DCKBK-	Multiply instruction
MAINDEC-11-DCKBL-	Divide instruction
MAINDEC-11-DCKBM-	Trap instructions and error traps
MAINDEC-11-DCKBN-	Program interrupt request test
MAINDEC-11-DCKBO-	Processor states test
MAINDEC-11-DCKBP-	Power fail test
MAINDEC-11-DCKBQ-	Console test
MAINDEC-11-DCKBR-*	CPU Parity test
MAINDEC-11-DCQKC-	Instruction exerciser

*Used only with systems containing Parity Memory.

DCKBA SXT Instruction – This is a test of the SXT instruction that ensures correct results and condition code operation. The SXT instruction is tested in all address modes in a general register and the PC.

DCKBB SOB Instruction – This is a test of the SOB instruction that ensures correct branching and condition code operation.

DCKBC XOR Instruction – This is a test of the XOR instruction that ensures correct results and condition code operation. The XOR instruction is executed using various operands; all address modes are executed using a general register and the PC.

DCKBD MARK Instruction – This is a test of the MARK instruction. The test executes the MARK instruction using all values of "N" and checks the results. Correct condition code operation is also tested.

DCKBE RTT Instruction – This is a test of the RTT and RTI instructions and uses "T" bit traps in the test. Proper stack operation and proper status changes are tested.

DCKBF Stack Limit Test – This is a test of the stack limit register and ensures correct YELLOW zone and RED zone boundaries, and overflow traps for all values of the stack limit register (dependent on available memory).

DCKBG SPL Instruction – This is a test of the SPL instruction. The test checks that only the priority level bits in the PSW (PS7-5) are affected by the SPL instruction.

DCKBH 11/45, 11/50, 11/55 Registers – This is a test of all the PDP-11/45, 11/50, 11/55 hardware registers (R10–R15), supervisor stack pointer (R16), user stack pointer (R17), and the microbreak register. This test ensures that all bits in each of the registers can be set and cleared, and are selected properly.

DCKBI ASH Instruction – This is a test of the ASH instruction. It tests ASH with different shift counts and in all the registers.

DCKBJ ASHC Instruction – This is a test of the ASHC instruction. It tests ASHC with different shift counts and in all the registers, including odd registers (test of circular shift).

DCKBK MUL Instruction – This is a test of the MUL instruction. It tests MUL with different number patterns in all registers, including single precision (odd registers).

DCKBL DIV Instruction – This is a test of the DIV instruction. It tests DIV with different number patterns in all even registers. Error conditions are also checked.

DCKBM Traps Test – This program tests all trap instructions and error traps (time out, odd address, and overflow). Interrupt logic is also tested, using the Teletype.

DCKBN PIRQ Interrupt – This is a test of the program interrupt request (PIRQ) logic.

DCKBO 11/45, 11/50, 11/55 Processor States – This program tests that PDP-11/45 instructions are executed properly in the three 11/45 modes (Kernel, Supervisor, and User). Also, the MIPD/I and MFPD/I instructions are tested.

DCKBP 11/45, 11/50, 11/55 Power Fail Test – This test checks out the power fail system.

DCKBQ – This test checks out the console.

DCKBR – This program will test parity aborts during CPU execution of read/restore (DATI) and read/pause (DATIP) memory operations. Normal parity is generated when writing to Memory (DATO) and checked for "other" parity when reading from memory (DATI or DATIP). Parity aborts are forced by setting a Parity Control Register for "other" parity (not normal) before execution of DATI or DATIP instructions.

This program does not test memory; it tests the processor and assumes memory to be functioning properly. MAINDEC-11-DCMFA will test memory and should be run in conjunction with this program to provide a through test of parity.

DCQKC – This diagnostic program is designed to be a comprehensive check of the PDP-11/45, 11/50, 11/55 processors. The program executes each instruction in all address modes and includes tests for traps and the Teletype interrupt sequence. The program relocates the test code throughout memory, 0-124K.

Table 6-4 lists the 13 general PDP-11 processor diagnostic programs. Each program thoroughly exercises a given instruction group. These programs are available as an additional CPU troubleshooting aid. They are the original PDP-11 CPU diagnostics; however, they now can only be obtained under the new MAINDEC numbers.

Table 6-4 General PDP-11 Processor Diagnostic Programs

MAINDEC No. *		
Old	**New**	**Instructions Tested**
DOAA	DZKAA-A	Branch
DOBA	DZKAB-A	Condition Branch
DOCA	DZKAC-A	Unary
DODA	DZKAD-A	Unary and Binary
DOEA	DZKAE-A	Rotate/Shift
DOFA	DZKAF-A	Compare Non-Equality
DOGA	DZKAG-A	Compare Equality
DOHA	DZKAH-A	Move
DOIA	DZKAI-A	BIS, BIC, BIT
DOJA	DZKAJ-A	Add
DOKA	DZKAK-A	Subtract
DOLA	DZKAL-A	JMP
DOMA	DZKAM-A	JSR, RTS, RTI

* All numbers are preceded by MAINDEC-11-.

6.5 HOW TO USE MAINTENANCE CARDS

The maintenance card that is used to perform maintenance tests and troubleshooting procedures on the PDP-11/45, 11/50, 11/55 system is shown in Figure 6-4. The maintenance card is constructed from a W131 maintenance module. The W131 is used with a W133 driver module. Figure 6-5 shows the special overlay that is used to designate switches and indicators for the KB11-A, D and FP11-B, C test functions. Table 6-5 lists the indicator lamp functions and the sources of the inputs from the KB11-A, D and FP11-B, C.

NOTE

The KB11-A uses one maintenance card. With an FP11-B also installed, another card is required for maintenance procedures. The KB11-D and FP11-C, however, together only require one maintenance card.

6.5.1 Clock Selection

CLK switch S3 is used to select the crystal clock (XTAL), the RC maintenance clock (RC), or the MAINT STPR switch as the timing source for the CPU or FPP. The KB11-A timing and FP11-B timing are independent; thus the switches on each maintenance card need not be set for the same selection. The FP11-C clock is syncronized to the KB11-D clock; thus settings on the one maintenance card effect the speed and maintenance mode of both the KB11-D and FP11-C.

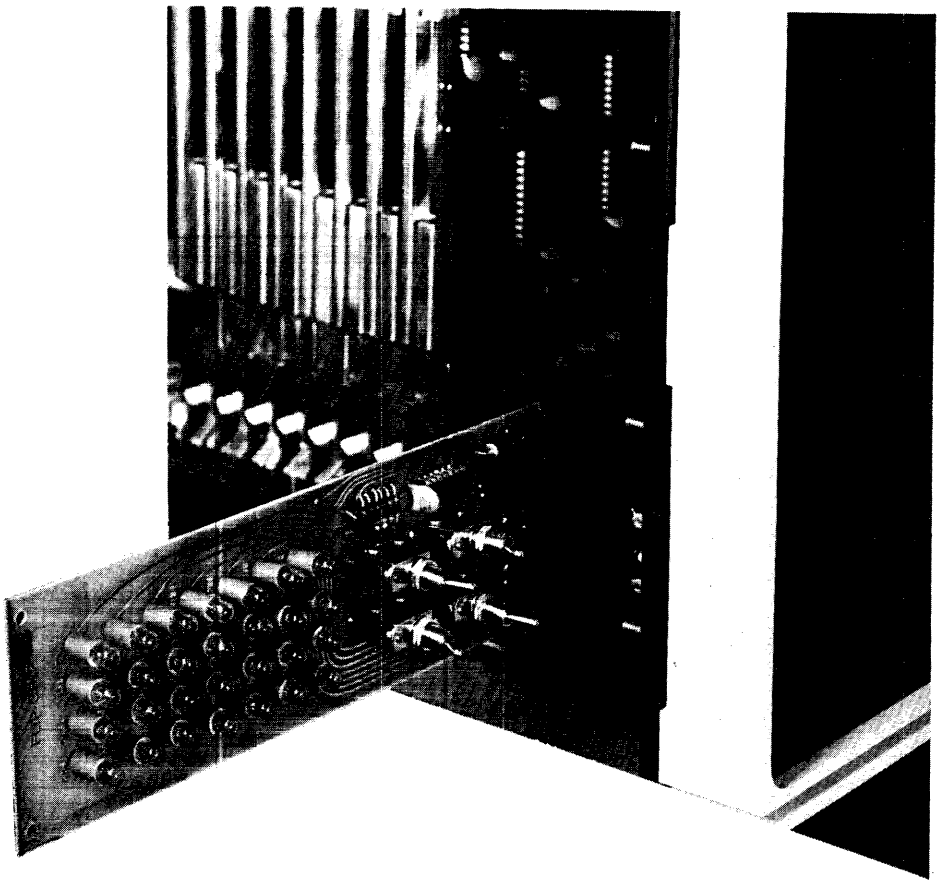


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Figure 6-4 Maintenance Card Installed for Test Purposes

Table 6-5 Maintenance Card Indicators

Indicator	Source		Signal Description
	KB11-A and KB11-D/FP11-C	FP11-B	
TPH	TIGA TPH MAT H	FRHJ MSTEP CLOCK (0) H	KB11-A, D: Basic processor timing pulse, whether crystal clock, RC clock, or MAINT STPR is selected. FP11-B, C: Indicates MAINT STPR clock pulse.
T1 through T5	TIGA ⟨T1:T5⟩ MAT H	FRHH ⟨T1S:T4S⟩ H	Indicates major time states for KB11-A, D and FP11-B, C. T5 is not used for FP11-B.
BUST	UBCB BUST MAT H	UBCB BUST MAT H	KB11-A, D Bust Cycle. Not asserted by FP11-B, C.
MEM	TMCF MEM H	TMCF MEM H	MS11 Semicondutor Memory System response to Fastbus memory address. From SMC Module (MOS-M8110, Bipolar-M8120).
REF REQ 1 REF REQ 2	SMCA RREQ IN PROG H (1st SMC) SMCA RREQ IN PROG H (2nd SMC)	SMCA RREQ IN PROG H	Indicates semiconductor memory recycle is in progress. Asserted only by an SMC module that is controlling Memory Matrix Modules.
EN T3 DLY	TIGB ENABLE T3 DLY H	TIGB ENABLE T3 DLY H	Asserts TIGA STOP T3 L when KT11-C, CD option is installed and enabled.
BBSY	UBCA BBSY MAT H	UBCA BBSY MAT H	Indicates Unibus A is busy.
MSYN	UBCB MSYN B MAT H	UBCB MSYN B MAT H	Indicates Unibus A Master Sync is asserted.
SSYN	UBCC SSYN MAT H	UBCC SSYN MAT H	Indicates Unibus A Slave Sync is asserted.
CNTL OK	UBCA CONTROL OK MAT H	UBCA CONTROL OK MAT H	Asserted by processor to allow Fastbus memory cycle to be completed by MS11.
FP SYNC	UBCE FP SYNC H	UBCE FP SYNC H	Indicates that the FP11-B, C is ready to send or receive data. Asserted by FRMJ FP SYNC L.
FP REQ	RACK FP REQ H	RACH FP REQ H	Used with FP SYNC to indicate to CPU that more data words are required. If FP SYNC is returned to CPU without FP REQ, the memory cycles are terminated.

Table 6-5 Maintenance Card Indicator (Cont)

Indicator	Source		Signal Description
	KB11-A and KB11-D/FP11-C	FP11-B	
FP ATTN	UBCD FP ATTN H	UBCD FP ATTN H	Decoded from CPU ROM states where MSC = 5, indicating floating-point instruction has been decoded.
FP WAIT	FRHH WAITS H	FRHH WAITS H	Represents the Wait state of the FP11-B.
CPFC1/FPEC1	No connection	No connection	Spare indicator. For future use, wire to row E, pin C1 (FPP) or row F, pin C1 (CPU).
AERF	TMCC AERRF MAT H	TMCC AERF MAT H	Indicates state of KB11-A, D Address Error Flag.
SERF	TMCC SERF MAT H	TMCC SERF MAT H	Indicates state of KB11-A, D Stack Error Flag.
PAR ERR	UBCB PARITY ERR MAT H	UBCB PARITY ERR MAT H	Indicates Unibus A or Fastbus memory has detected a parity error.
T	TMCB PS04 MAT H	TMCB PS04 MAT H	Indicates processor status word trace bit is set.
N	IRCH MAT N H	FRLP FN (1) H	KB11-A, D: N (negative) bit of the CPU processor status word condition code. FP11-B, C: N bit of the FPP program status register.
Z	IRCH MAT Z H	FRLP FZ (1) H	KB11-A, D: Z (zero) bit of the CPU processor status word condition code. FP11-B, C: Z bit of the FPP program status register.
V	IRCH MAT V H	FRLP FV (1) H	KB11-A, D: V (overflow) bit of the CPU processor status word condition code. FP11-B, C: V bit of the FPP program status register.
C	IRCH MAT C H	FRLP FC (1) H	KB11-A, D: C (carry) bit of the CPU processor status word condition code. FP11-B, C: C bit of the FPP program status register.

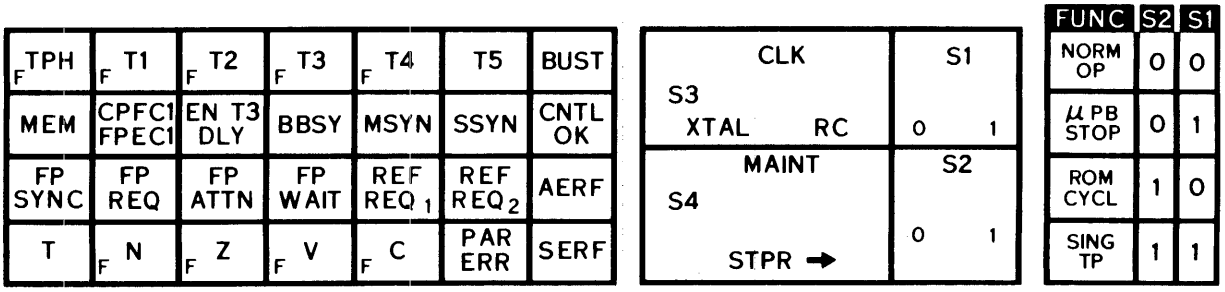

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Figure 6-5 Maintenance Card Control and Indicator Overlay for KB11-A,D and FP11-B,C Test Procedures

When S3 is set to XTAL, the 33.3 MHz crystal clock is selected for the CPU timing source and the 18 MHz crystal clock is selected for the FPP. When the CLK switch is set to RC, the variable frequency RC maintenance clock is selected as the timing source. By setting the potentiometer (Table 6-6), the useful range of the period of the RC maintenance clock pulse can be adjusted. Note that this potentiometer (on both the TIG and FRH boards) is mounted on the front edge of the module and thus does not require W900 Extender modules to be adjusted.

NOTE

When using both KB11-A and FP11-B RC clocks, half of the FP11-B clock period must be shorter than two KB11-A ROM cycles. This ratio must be maintained when using the RC clock or single-stepping the FP11-B, otherwise the two processors will not remain syncronized.

Table 6-6 RC Maintenance Clock Pulse Adjustment

Potentiometer	Module	Module Location	Range (ns)	Device Affected
R162	M8109 (TIG)	KB11-A	28–50*	KB11-A
R32	M8114 (FRH)	FP11-B	50–290*	FP11-B
R162	M8109 (TIG)	KB11-D	27–450	KB11-D, FP11-C

*See note above on RC clocks

6.5.2 Maintenance Mode Control

Maintenance card switches S2 and S1 are used to select the maintenance mode, as indicated in Table 6-7.

6.5.2.1 Single ROM Cycle – When switches S1 and S2 are set for single ROM cycle mode, the processor will proceed through a single ROM cycle each time the console CONT switch is pressed. For convenience, MAINT STPR switch S4 on the maintenance card can also be used to initiate the single ROM cycle. In this mode of maintenance operation, TIGA STOP T3 L is asserted at time state T1, causing the processor to stop at time state T2 of each microstate.

Table 6-7 Maintenance Mode Selection

S2	S1	Mode	Operation
0	0	NORM OP	No effect on KB11-A, D or FP11-B, C operation.
0	1	μPB STOP	The KB11-A, D or FP11-B, C will execute instructions until the microprogram ROM address matches the contents of the Program Break (PB) register. It halts at T2 of that ROM state.
1	0	ROM CYCL	The KB11-A, D or FP11-B, C will execute a single ROM state each time the MAINT STPR is pressed.
1	1	SING TP	The basic clock changes state each time the MAINT STPR is pressed. Thus, pressing MAINT STPR twice provides a single time pulse.

6.5.2.2 μPB STOP – When switches S1 and S2 are set for μPB (microprogram break) STOP mode, the KB11-A, D or FP11-B, C will continue to execute program instructions each time CONT is pressed, until the ROM address register contents match the Program Break (PB) Register contents. When both microstate addresses are equal, the processor stops at time state T2 of the selected microstate. At that point, S1 and S2 can be set for SING TP mode as described in Paragraph 6.5.2.3. Load the PB with the desired microprogram address as follows:

1. Press HALT switch. Processor halts at microprogram CON.00 (CPU μADRS 170).
2. Set PB register address 777770 into console switch register.
3. Press LOAD ADRS. ADDRESS display will be 777770.
4. Set desired microprogram break address into the low byte of the switch register. For example, to stop at FET.00, set 217_8 into the switch register.
5. Press DEP. The DATA display will display this input in the low order byte with the Data Display Select switch set to DATA PATHS.
6. Press CONT. The processor will execute program instructions until the RAR equals the PB, then stop.

6.5.2.3 Single Step – When switches S1 and S2 are set for SING TP mode, gating logic shown on drawing TIGB inhibits the source synchronizer from selecting either the crystal clock or the RC maintenance clock. Under these conditions, each time MAINT STPR switch S4 is pressed, TP H changes levels.

NOTE
MAINT STPR must be pressed twice to complete each time pulse.

This feature allows events that occur on the leading edge or trailing edge of the same time pulse to be examined separately.

6.5.3 Using the Maintenance Card with KB11-A, D

Chapter 7 of the *KB11-A, D Central Processor Unit Maintenance Manual* explains how to use the processor flow diagrams. The same compare instruction example is used to demonstrate how to use the maintenance card for test purposes.

6.5.3.1 Deposit Test Instruction – Set the Address Display Select switch to CONS PHY, load address 1000, and deposit the Test Instruction 6-1.

Address (octal)	Data (octal)	Comments
1000	022767	Compare instruction,
1002	000015	Source operand immediate
1004	000100	Destination operand indexed
.		
.		
1106	000000	Word = 0

Test Instruction 6-1

6.5.3.2 μPB STOP MODE – This setup loads the test instruction address into PCA; then into PCB. The processor performs the RES.00 microprogram sequence (flows 3) and then fetches the test instruction.

1. Set up the PB for a μPB STOP at FET.10 (CPU μADRS 260).
2. Load address 1000_8.
3. Set maintenance card switches S1 and S2 for μPB STOP mode.
4. Set ENAB/HALT to ENABL and press START.

The processor will stop at FET.10 microstate 260 in T2. Refer to Paragraph 6.4 in the KB11-A, D manual to review the processor events. Table 6-8 indicates normal console indications as a result of these events.

Table 6-8 Console Indications

Console Display		Contents (octal)
ADDRESS:	CON PHYS	1000
DATA:	DATA PATHS	1002
	BUST REGISTER	1000
	μADRS FPP/CPU	260
PAUSE		

Maintenance card indicator T2 lights.

6.5.3.3 Single ROM Cycle Mode – This setup causes the processor to execute one ROM cycle of the test instruction and stop each time MAINT STPR switch S4 is pressed.

1. Set maintenance card switches S1 and S2 for single ROM cycle mode.
2. Press maintenance card MAINT STPR switch S4 or CONT switch on the console.

Refer to the test instruction description in the KB11-A, D manual, Paragraph 6.4. Table 6-9 lists normal ADDRESS and DATA displays resulting from each ROM cycle execution, starting with FET.10, T2 of the example test instruction.

Table 6-9 Normal Display Indications for Single ROM Cycle Example

After Executing ROM Microstate:	The Console Displays will be:			
	μADRS CPU	DATA PATH	BUS REGISTER	ADDRESS CON PHYS
FET.10	343	1002	022767	1002
IRD.00	022	1004	022767	1002
S13.00	027	1004	022767	1002
S13.10	117	15	15	1004*
D67.80	006	1006	15	1004
D67.00	251	1106	100	1004
D67.10	122	15	100	1106
D10.30	177	15	15	1106
D10.60	-FAST 032 FAST 033	-16**	0	1006
TST.00	217	--	--	--
TST.01	260	--	--	--

* Indicates BUST
** 1's complement of 15
\- Determined by next instruction; not included in this example.

6.5.3.4 SING TP Mode - This procedure allows the maintenance card user to step through microstates of the test instructions example in the SING TP mode.

1. Set ENABL/HALT to HALT and press START.
2. Load the example instruction address 1000.
3. Set maintenance card switches S1 and S2 to μPB STOP mode.
4. Set ENABL/HALT to ENABL and press START.

When the processor stops at T2 of FET.10 (CPU μADRS 260), set S1 and S2 to select SING TP mode. Then press MAINT STPR switch S4 twice to step through each time state.

NOTE
A time state is only valid when the associated time state indicator and the TP H indicator are both lit.

Table 6-9 lists the normal DATA and ADDRESS displays for each time state of the example, starting with T2 of FET.10 (CPU μADRS 260).

NOTE
The example assumes the test instruction is deposited in a semiconductor memory location.

If the test instruction is deposited in a core memory location, Unibus control signals MSYN and SSYN will be displayed on the maintenance card indicators. Also, if the KT11-C, CD option is implemented, the EN T3 DLY indicator lights. While EN T3 is lit, the processor will remain in T2 until the delay counter is stepped through three complete time periods.

6.6 HOW TO USE THE W900 MODULE EXTENDERS

The W900 module extender is a double-height, multilayer etch board that provides one-to-one connections between module connectors and corresponding CPU backplane connector slots. Thus, three W900 module extenders can be used to extend a PDP-11/45 hex-size module from the CPU backplane to provide access to ICs and discrete components for test purposes under active operating conditions.

Alternatively the W904 hex height multilayer extender can be used.

NOTE

Do not attempt to extend more than one module at a time while performing test procedures.

6.7 MODULE AND ASSEMBLY REMOVAL AND REPLACEMENT

No special procedures are required to disassemble and reassemble most of the components and assemblies in the H960-C cabinet or the BA11-FA mounting box. This paragraph outlines the procedures for removing and replacing modules and the steps required to disassemble the console.

6.7.1 Module Removal and Replacement

The multilayer modules used in the PDP-11/45, 11/50, 11/55 are equipped with lock/release type handles, and each slot in the backplane has card edge and center guides that allow the modules to be installed easily. The card guides ensure that the modules are not removed or inserted at an angle so great that module or connector slots are damaged.

CAUTION

Even though these features are provided, always install and remove the modules carefully.

6.7.2 Console Disassembly

Refer to Figure 6-6. The following steps are required to disassemble the console. (Note that very-early-manufactured 11/45 systems have a slightly different console mounting bracket, but disassembly is similar.)

1. Turn power OFF at the circuit breakers.
2. Remove the four screws (A) and washers that secure the bezel (B); remove the bezel.
3. Remove the five screws (C) and washers that secure the console panel (D); remove the console panel.
4. Unplug the harness power plug P1 from J3 and the signal cables from J1 and J2.
5. Remove the three screws (E) and washers that hold the bottom of the console PC board to the processor mounting box. Also remove the three screws (F), washers, and spacers (G) that hold the top of the console PC board to the processor mounting box. This will free the PC board (H).

Reassembly requires reversal of the previous steps.

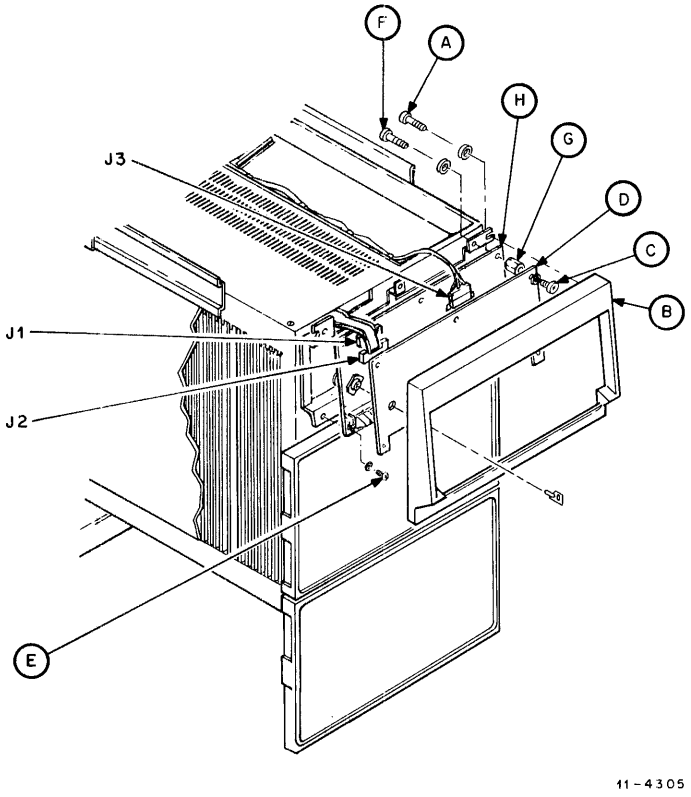


Figure 6-6 Console Assembly

To replace a faulty indicator bulb on the console, follow the above steps 1 through 5 and replace the faulty indicators. This requires soldering. When indicator replacement has been completed, test all indicators. Reassemble the console partially for indicator testing by reversing steps 5 and 4. Test all indicators by turning power ON at the circuit breakers and lifting the indicator test switch. This is an unlabeled white switch located between switch register bit 0 and the LOAD ADRS switch. All indicator bulbs should light. Turn power OFF at circuit breakers before reassembing the console.

6.8 REMOVAL AND REPLACEMENT OF ICs

The PDP-11/45, 11/50, 11/55 modules are multilayer etched circuit boards. The four layers consist of two power and ground internal planes, and two etched circuit external layers (Figure 6-7). The inner power and ground planes form a decoupling capacitor between the power and ground planes providing shielding between the etched circuit layers and reducing the possibility of noise and crosstalk. One advantage in using this type of module construction is that the need to route power and ground signals to each individual component and IC via etching on the two outer etched boards is eliminated, allowing a much greater component density on each board.

6.8.1 Location of ICs

On the handle end of the board, the physical location of the last IC in each row is E-numbered to aid in locating ICs during maintenance and troubleshooting.

The first sheet of each module circuit schematic is a physical layout showing the location of the ICs and discrete components on that module.

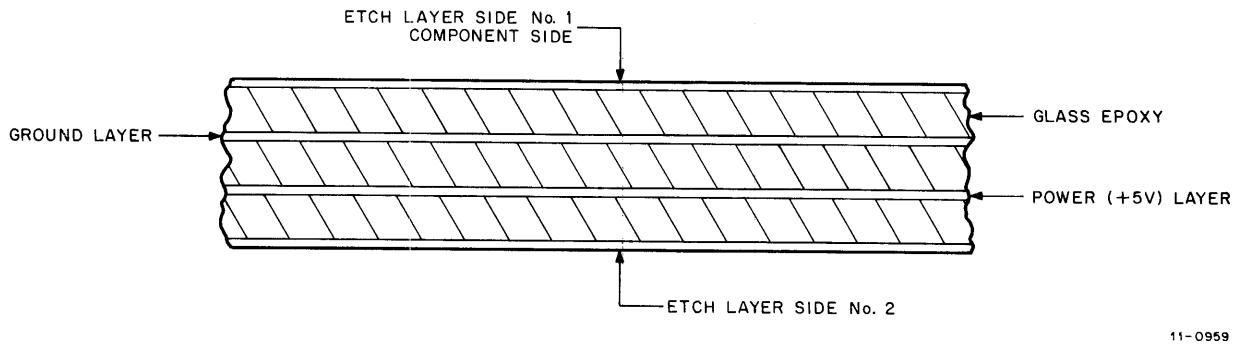


Figure 6-7 Cross Section of Multilayer Board

When possible, some IC locations on most boards are not used; these spare locations, provided on a space available basis, ensure that if future ECOs (engineering change orders) involving additions are required, they can be more easily implemented.

When spare locations are provided on the module, each spare location has a number just like one of the ICs. The spare locations must also be counted when locating ICs on the board.

When an IC is added to a board (e.g., because of an ECO), the IC assumes the preassigned number of the location into which it is installed. Thus the numbered IC locations at the handle end of the board, as well as all other IC locations, always remain the same.

6.8.2 IC Connections

IC and component connections to the power and/or ground inner layers are normally made as shown in Figure 6-8A. The ICs and components are connected to the inner layers in this manner to allow the IC or component to be more easily replaced.

When a component is tied directly to an inner layer as shown in Figure 6-8B, instead of connecting through an etch as shown in Figure 6-8A, it is difficult to remove the component because most of the heat from the soldering iron is absorbed by the inner layer, preventing the solder around the leads of the component or IC from melting. To minimize this difficulty, direct connections to the inner layer are made by a vein-type connection as shown in Figure 6-9. This type of connection reduces the connected area between the plated-through hole and the inner layer. This reduces the amount of heat transfer to the inner layer when heat is applied to the plated-through hole when melting solder and removing component leads, or removing excess solder once the lead has been removed.

6.8.3 IC and Component Removal and Replacement

Because the etch and plated-through hole eyelets are so small, extra care shold be taken during the maintenance and repair of the multilayer modules, especially when soldering and unsoldering components. Certain tools (or their equivalent) are recommended for use duing removal and replacement of ICs on the multilayer modules; they are listed in Table 6-1. The manufacturer and type of part number of each tool is indicated in parentheses at its first occurrence in the procedure.

6.8.3.1 Removal and Replacement of Plastic Case ICs – To remove and replace a plastic case IC and to preclude damage to the multilayer board, the procedure described by Figures 6-10 through 6-17 should be strictly adhered to. Removal and replacement of ceramic ICs are covered in Paragraph 6.8.3.2.

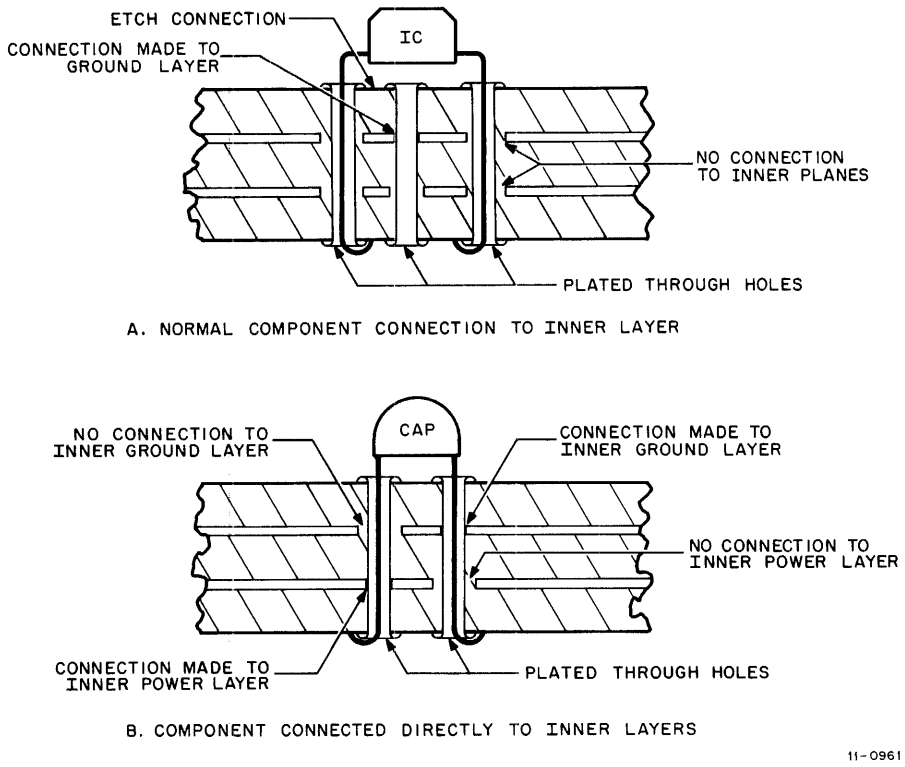


Figure 6-8 Component Connections to Inner Layers

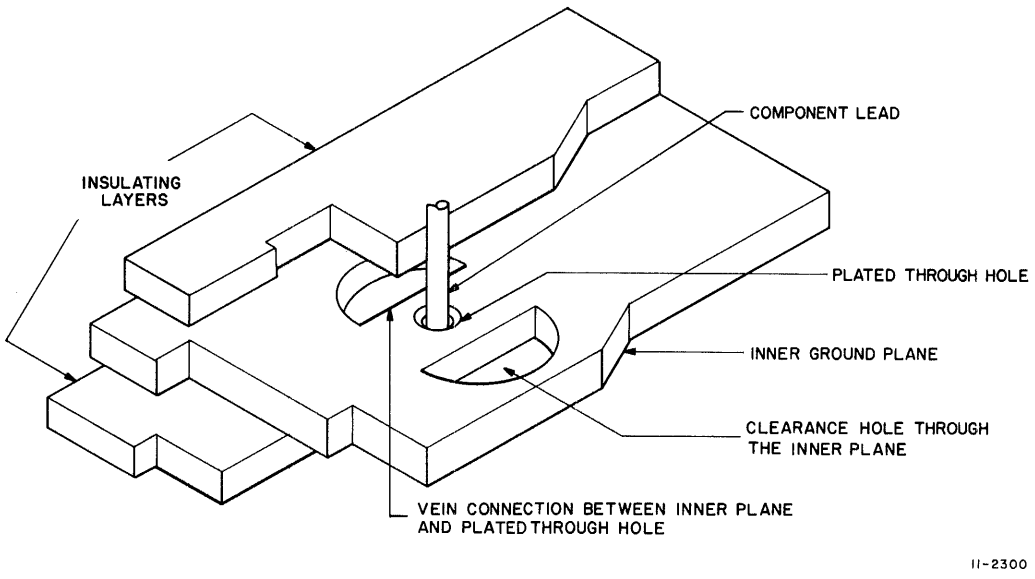
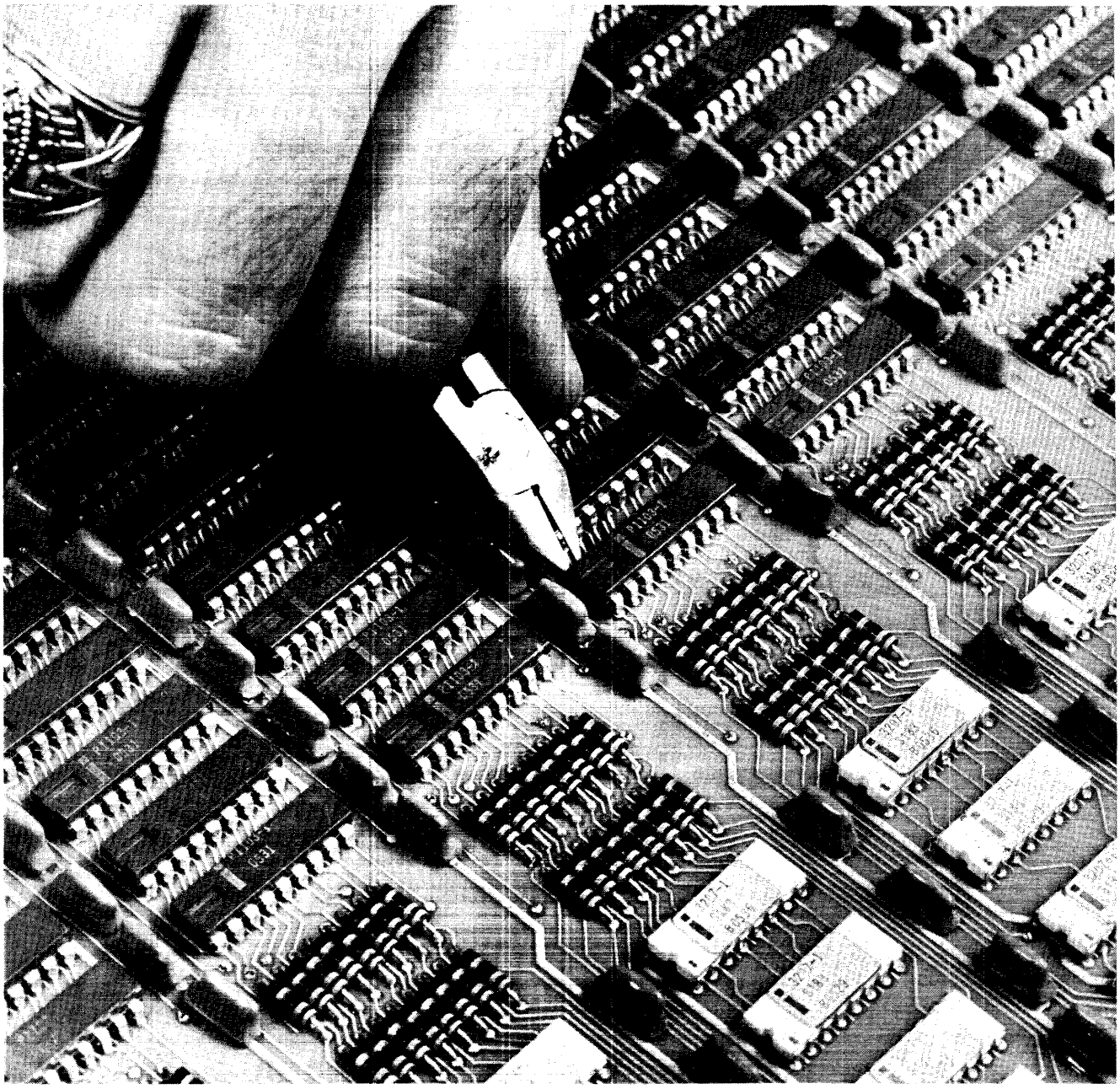


Figure 6-9 Top View of Component Connection Made Directly to Inner Layer

6201-1

This sample module is a G401 MOS Memory Matrix Module which has components that are connected directly to the inner layers using the vein method described in Figures 6-8 and 6-9.

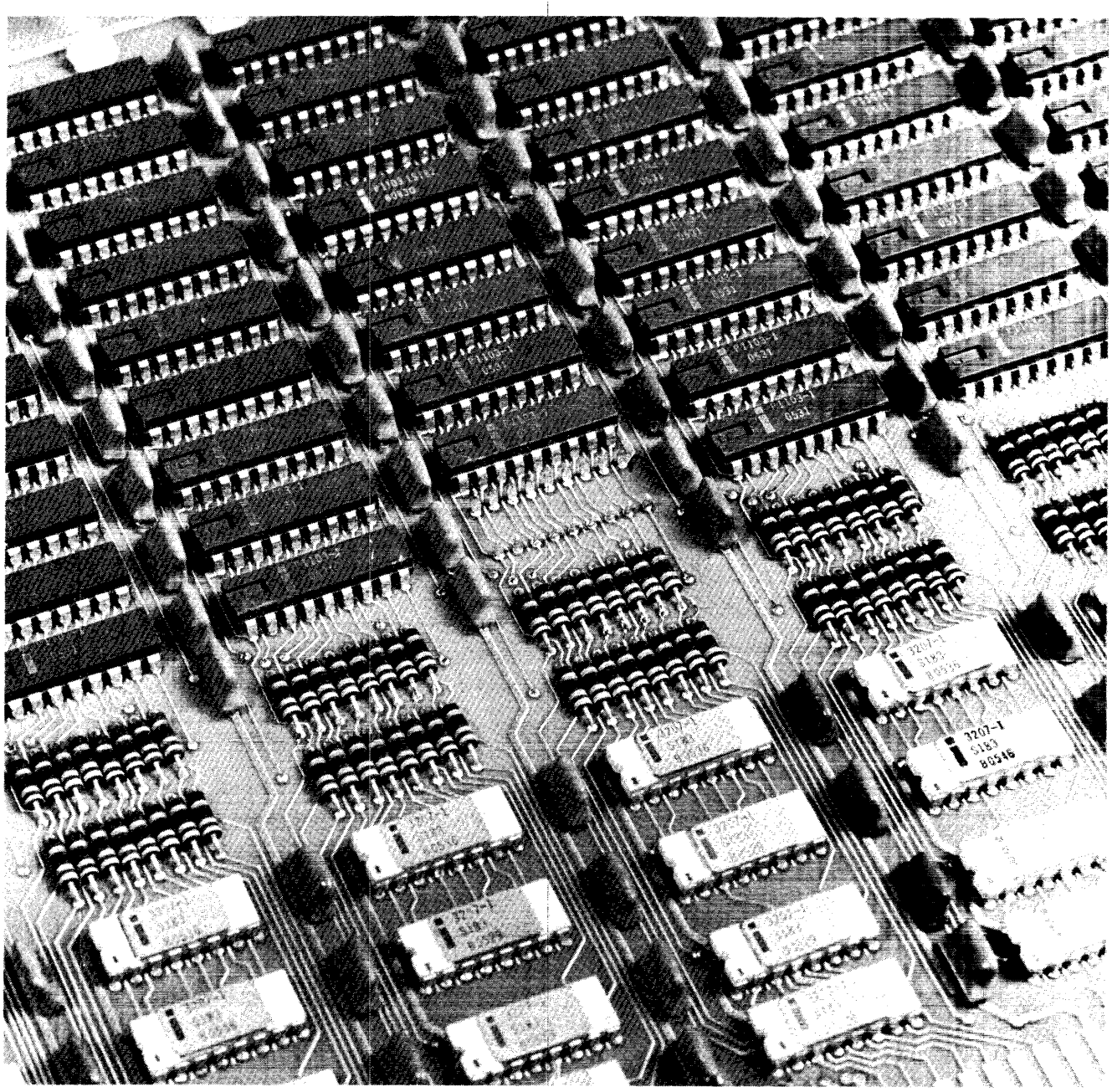
Figure 6-10 Module to be Repaired and Tools Required



6201-2

Defective IC leads are clipped, using small diagonal cutters (Utica, Part No. 47-4). Cut the leads as close to the body of the IC as possible to allow the remaining leads to be more easily removed.

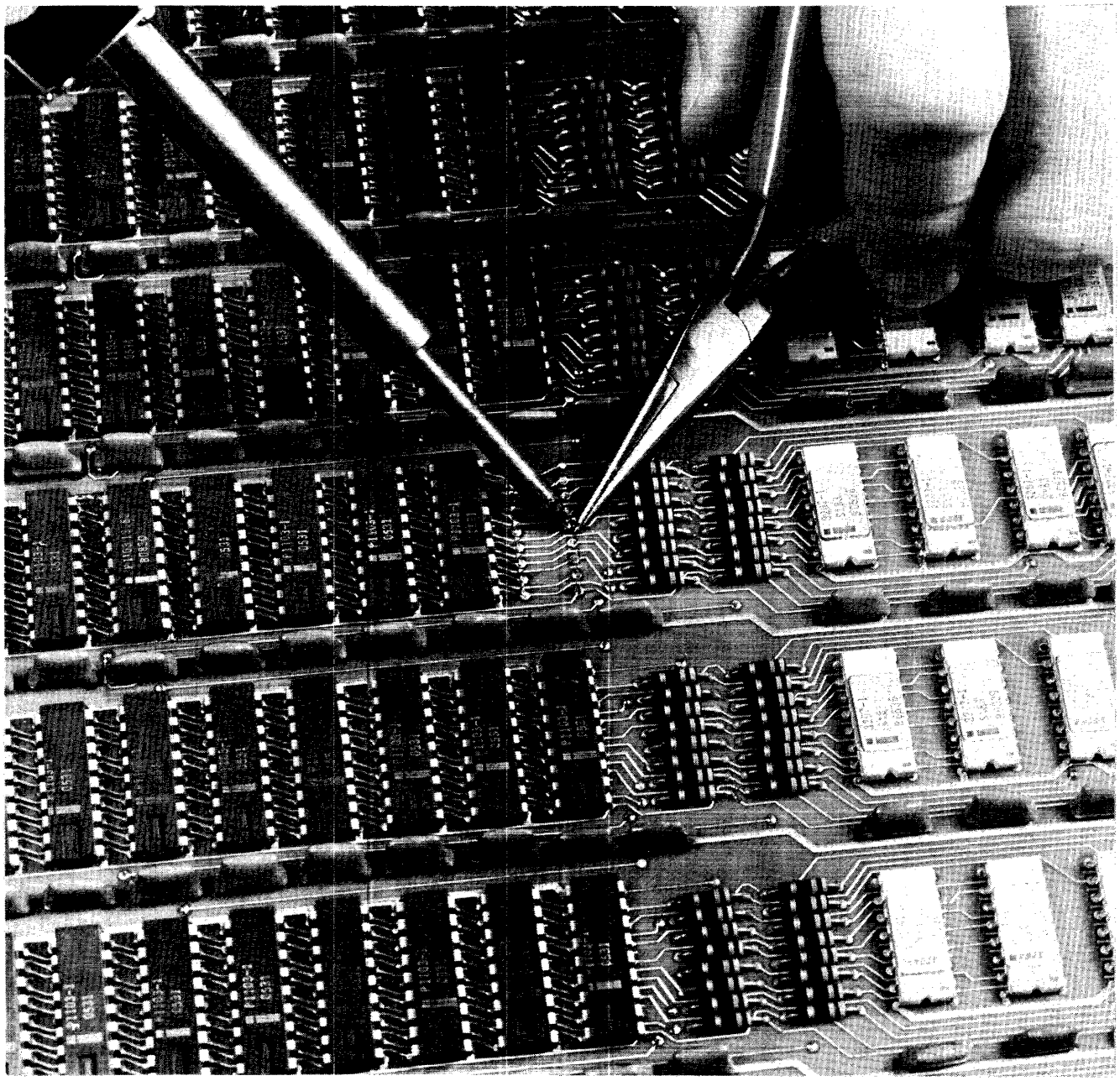
Figure 6-11 Removing a Defective IC from the Module



6201-3

IC location after the IC has been removed – with the IC leads still in the board. Locate the leads of the IC just removed on the soldered (back) side of the board and cut all leads to avoid difficulty during their removal

Figure 6-12 Defective IC Removed



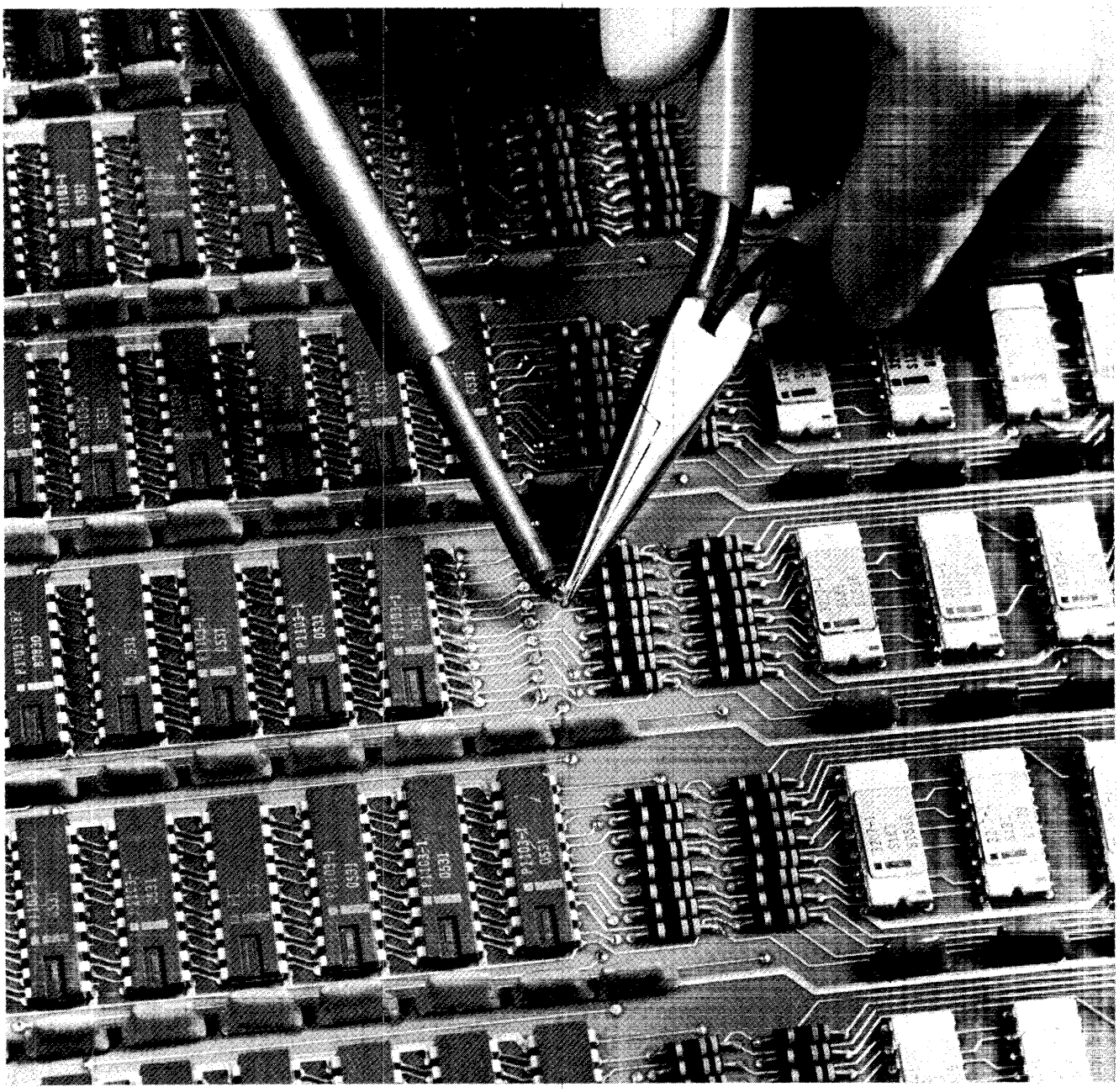
6201-4

IC leads being removed from side 1 of the board. Apply heat to the lead until the lead becomes loose. Then remove the lead by pinching with the soldering iron (Paragon, Part No. 615) and pliers (Utica, Part No. 23-4).

CAUTION

Leads that are connected to an inner layer require more heat because much of the heat is absorbed by the inner layer. It is helpful to add solder to the lead first causing more heat to be conducted to the solder in the eyelet around the lead.

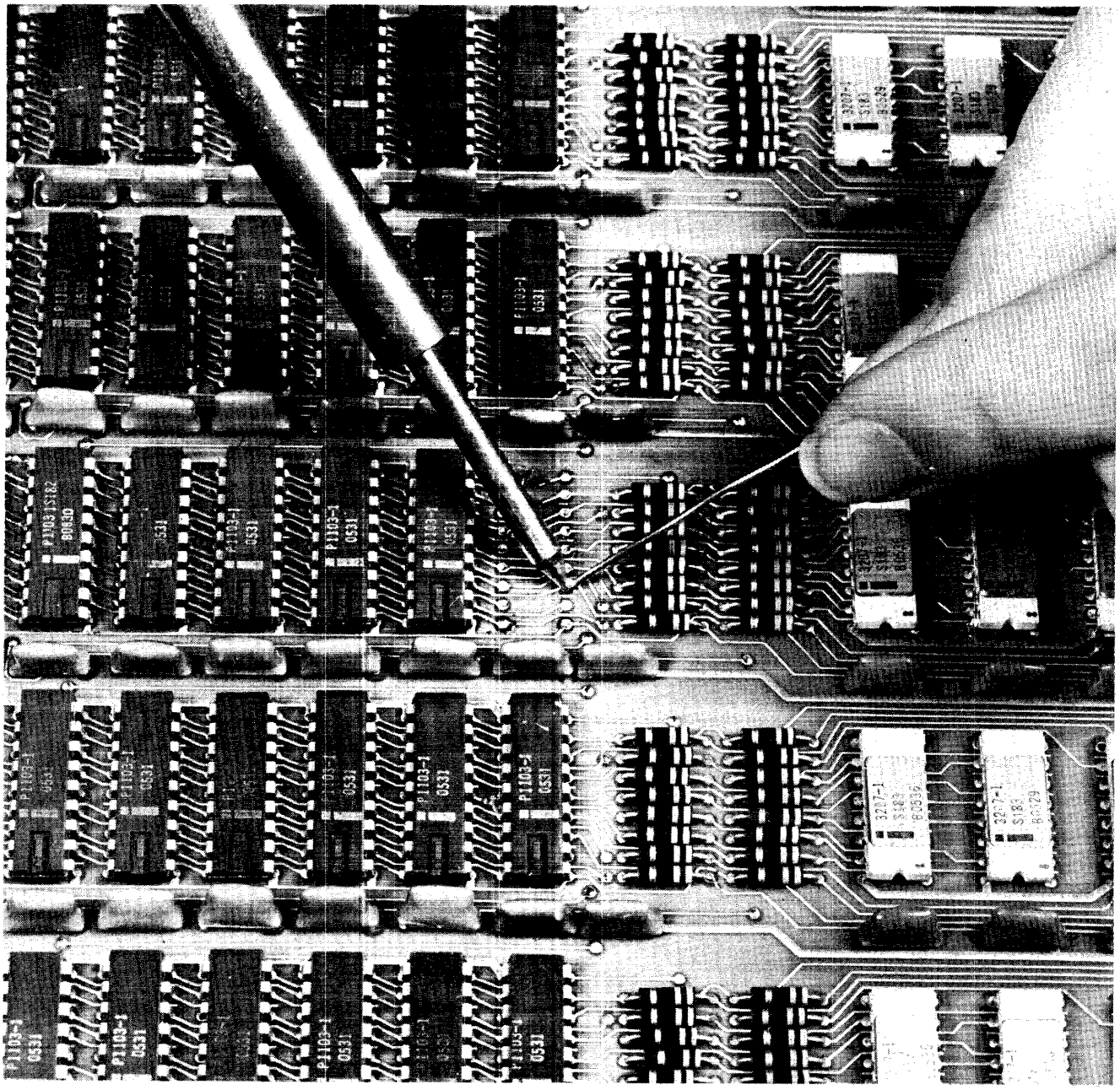
Figure 6-13 Removing IC Leads



6201-5

Lead directly after removal from the eyelet using the soldering iron and pliers.

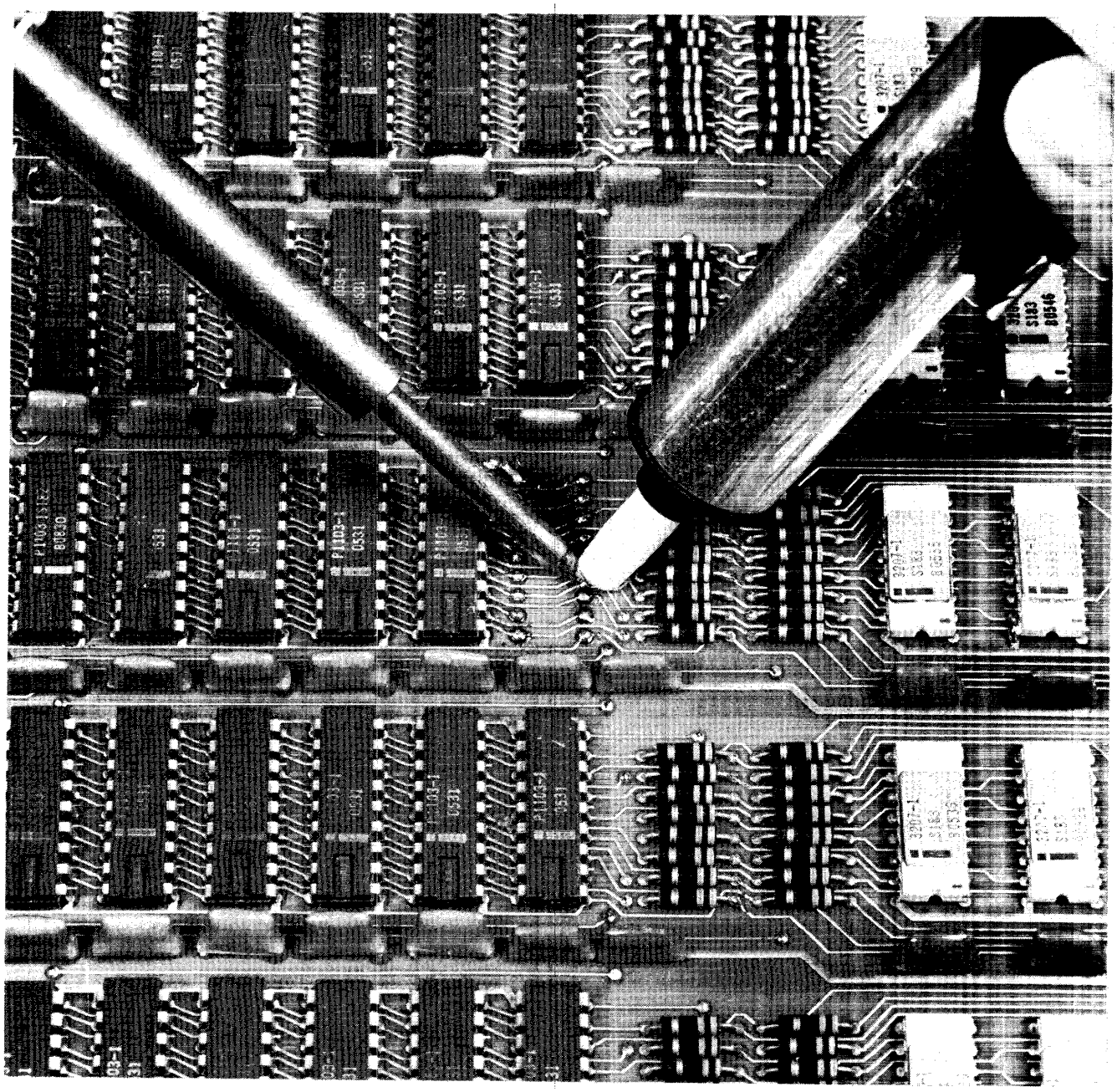
Figure 6-14 IC Lead Removed



6201-6

After all of the IC leads have been removed, remove the excess solder remaining in the eyelets prior to inserting the new IC. This figure shows solder being applied to the eyelets after all the leads have been removed. The extra solder absorbs excess heat and keeps it from being applied directly to the etch of the plated-through holes.

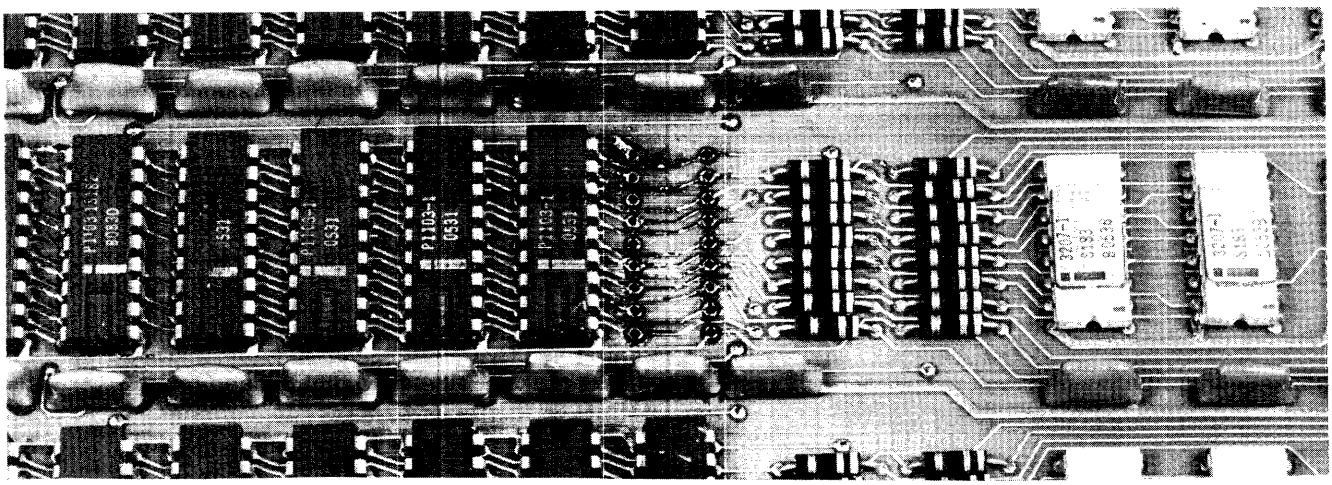
Figure 6-15 Applying Solder to Refill Eyelet



6201-9

Once the eyelets have been refilled with solder, as described in Figure 6-10, remove the solder using the soldering iron and solder extractor as shown above. In this figure, the eyelet has no connection to the board inner layers; thus, the solder can be extracted from the same side of the module to which the heat is applied. However, in cases where direct connections to the inner layer are made, heat must be applied to one side of the module and the solder must be extracted from the opposite side due to the heat sinking properties of the inner layers. In this case, the module should be in a vertical position to allow access to both sides of the module simultaneously.

Figure 6-16 Removing Excess Solder from Eyelet



6201-8

IC location after all the eyelets have been cleared of solder.

1. Inspect the eyelets to ensure that no excess solder remains. If all the solder is not removed, refill the hole as described in Figure 6-15 and remove the solder again as described in Figure 6-16. Continue this procedure as required, until all of the eyelets are cleared of excess solder.

2. Use a cleaning solvent and brush to clean the IC location of any excess solder flux.
3. Thoroughly inspect the IC location and surrounding area for solder splash and damage to etch lines and plated-through holes.
4. Ensure that none of the leads are bent, and insert the replacement IC in the holes. When inserting the replacement IC into place, avoid bending the leads on the opposite side of the module; this makes future removal of the IC easier, should it be necessary.

CAUTION

If the leads must be bent to hold the IC in position for soldering, avoid bending leads more than 45°, using only one lead at each end and on opposite sides of the IC.

5. Solder in the new IC from the opposite side of the module. Use enough solder to fill the holes and make a good connection. Avoid using an excess of solder to prevent overflow on the top side of the board, which could cause a short under the body of the IC.

6. Once all the solder connections are made, clean and inspect the area for any damage. Cut off IC leads close to the board. Take necessary corrective action for any defects that are found.

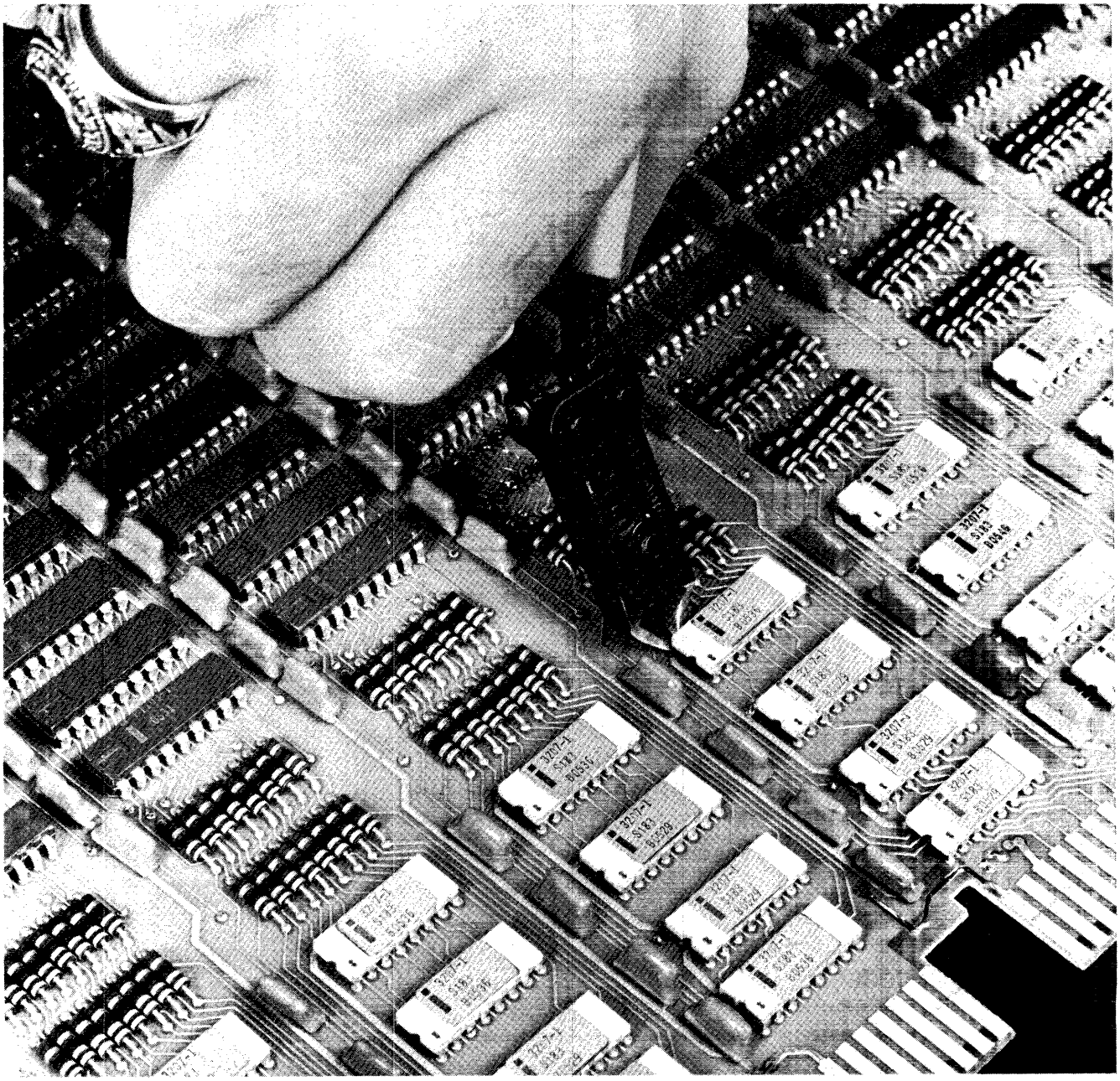
CAUTION

After installing the ECO or replacing a faulty IC on a module, ensure that no short circuit exists between the power and ground planes of the module. Do this before replacing the module in the equipment.

Figure 6-17 IC Location Ready for Insertion of New IC

6.8.3.2 Removal and Replacement of Ceramic ICs – Ceramic ICs require a different removal/replacement procedure than the plastic ICs because of their different construction. Leads of the plastic ICs extend out and down from the case of the IC, whereas the leads on the ceramic ICs extend straight down from the case of the IC, and are harder and thicker than those found on plastic ICs. Thus, certain steps of the removal/replacement procedure for the plastic ICs do not apply to removal and replacement of ceramic ICs. To remove a ceramic IC, use the following procedure:

1. Special diagonal cutters (DEC Part No. 29-12551) are required to remove ceramic ICs. (See Figure 6-18) Cut all the IC leads and remove the IC from the module.



6201-7

Figure 6-18 Special Tool and Method Used to Clip Ceramic IC Leads

2. Inspect the component side of the module for any burrs that may be present from cutting the IC lead. If any burrs are present, carefully remove them using the special diagonal cutters.

3. Perform procedure listed in Paragraph 6.8.3.1 starting with Figure 6-12.

NOTE

Because the leads will be cut flush with the board surface, it is not possible to pinch leads between pliers and soldering iron. Use the following procedure to remove leads.

4. Cut the leads on side 2 of the board to allow easy removal.

5. On side 1, heat the plate-through hole and extract lead and solder with solder extractor. If lead cannot be extracted from side 1, try to extract it from side 2.

NOTE

Do not attempt to remove melted solder or lead by banging the module on the bench.

6.8.4 Solder Mask Removal

Side 2 of PDP-11/45, 11/50, 11/55 module (the side opposite the component side) is coated with a solder mask to prevent short circuits between adjacent electrical connection points. To repair side 2 of these modules, scrape off the solder mask chemical. Use a knife or X-acto tool to remove the solder mask.

6.9 SPECIAL MOS HANDLING PROCEDURES

Because of the high input impedance of MOS (metal oxide semiconductor) devices, they are susceptible to damage from static discharge. These devices, such as the Intel 1103-1, are employed extensively on the G401 and G401YA MOS memory matrix modules.

Many manufacturers of MOS devices use various types of internal protection against damage from static discharge. These types of protection range from Zener diodes to limiting resistors. However, the effectiveness of these protection schemes is questionable and many manufacturers suggest that additional precautions be taken to ensure safe handling of these devices.

This paragraph outlines some basic rules for handling MOS devices in the field. The precautions taken at the factory are more extensive than those that are practical for field implementation. Therefore, the following rules represent only the basic requirements for safely handling MOS devices in the field.

These rules are intended to keep the MOS device at the same electrical potential as the work area, tools, and personnel. Do not handle MOS devices in areas of high static susceptibility such as carpeted areas or areas of extremely low humidity.

1. Choose a work area that exhibits minimal potential for the generation of static electricity.

2. Use a power receptacle that has a connection to earth ground.

3. Only use a soldering iron that offers a 3-wire ground such as the new DEC-supplied soldering iron (DEC Part No. 29-13452). Do not use a transformer-type soldering iron.

4. Removal of defective MOS devices from a module requires no special handling procedures. MOS devices, once soldered on the board, offer no danger of damage from static discharge.

5. If you are sitting in a chair while working with MOS devices, it is suggested that the chair be electrically connected to the frame of the work table. If this is not possible, use care to prevent the chair from touching the work table, thus preventing a static discharge from the chair to the work table.

6. If you are standing while handling MOS devices, avoid rubbing your clothing against the work table or nearby furniture, thereby preventing the build-up of static electricity.

7. MOS devices (as supplied by DEC) are packaged in a conductive plastic bag. Before opening the bag, touch the work table or metal connected to it to discharge any static build-up.

8. Empty the contents of the bag onto the work area without touching the MOS devices.

9. Prior to touching the MOS device, always discharge yourself by touching the work area or attached metal.

10. Insert the MOS device into the module using care to ensure minimal handling of the device leads. Try to grasp the chip by the body of the device and not by its leads.

11. Using the soldering techniques described in Paragraph 6.8.3.1, Figure 6-14, solder the MOS device using the 3-wire grounded soldering iron. If a grounded iron is not available, always attach a wire from the iron tip to ground (or the work area) to prevent any potential difference between the device and the soldering iron.

12. Replace the unused spare MOS devices in the conductive plastic bag by grasping the body of the IC, after previously discharging yourself against the work table. Reseal the bag using tape or a stapler.

All of the above are precautions to reduce the possibility of a potential difference between the MOS device being handled and the surrounding environment. Again, common sense is essential when choosing a good work area and method of handling these devices.

6.10 EQUIPMENT CONFIGURATION AND REVISION STATUS

The following paragraphs describe the MUL sticker, the ECO status sticker, and module revision status. The MUL sticker lists the equipment complement system serial number, etc.; the ECO status sticker provides information about the current ECO status of wire-wrap devices; module revision status shows the current ECO status of the module.

6.10.1 Mechanical Status Sticker

See Figure 6-19. This sticker is located on the rear of the Mounting Box. *Box Type* is 11/45, 11/50, 11/55, H960-D or H960-E. A letter designates the *Revision Level at Manufacturing*. Field installed ECOs should be entered as performed.

6.10.2 ECO Status Sticker

The ECO status sticker (Figure 6-20) is located on the inside of the module door in the CPU or BA11-FB mounting box. This sticker is filled out for installation of ECOs to wire-wrap devices such as the KB11-A, D or the various system units. Table 6-10 describes how the various columns are to be filled out and the department responsible for filling out these items. Later versions have an additional MUL sticker for BA11-FB mounting boxes, used in expansion cabinets. It consists of nine system unit sections similar to those shown for system units 1, 2, and 3. It is used for the same purpose.

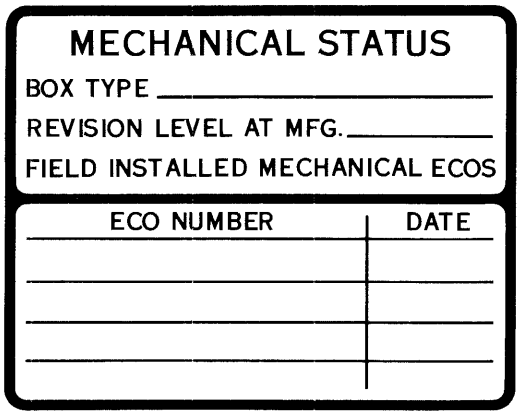


Figure 6-19 Mechanical Status Sticker

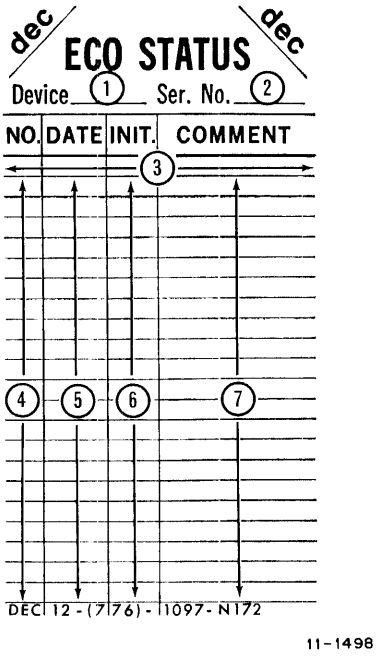


Figure 6-20 ECO Sticker

Table 6-10 Completing the ECO Status Sticker

Item No.	Responsibility	Description
1	Production	Option designation code for applicable device (e.g., KB11-A, D, MM11-S, etc.).
2	Production	Device serial number.
3	Production	Original wire wrap revision letter (e.g., ORIGINAL REV. B).
4	Production/Field Service*	Numerical portion of ECO number (e.g., for ECO KB11-0002 write only 02 in this column).
5	Production/Field Service*	Installation date of ECO.
6	Production/Field Service*	Initials of person installing ECO.
7	Production/Field Service*	Necessary comments about ECO or its installation, (e.g., only part 2 installed).

* If option is installed in factory, production has responsibility for filling out ECO sticker. If the option is an add-on in the field, field service will fill out items 4 through 7.

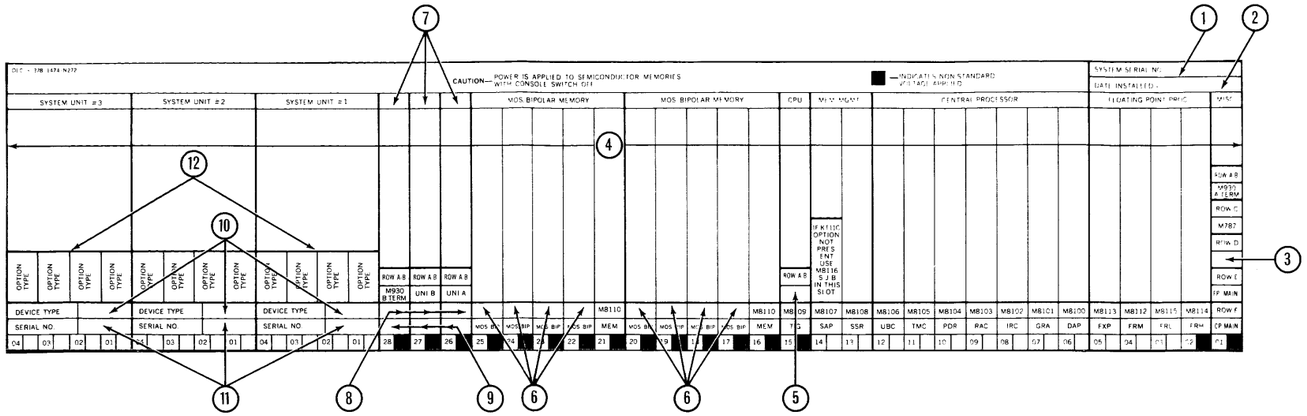
Note: ECO STATUS STICKER is located on the inside of the module door for BA11-FA and BA11-FB Mounting Boxes.

6.10.3 Module ECOs

Each module is stamped with the alphabet (except for G, I, and O) to record various circuit schematic revisions to a module. When a module is shipped from the factory, the actual revision letter from production is stamped on the handle. When ECOs that revise modules are installed in the field, scratch off the appropriate letters from the module. For example, if an ECO corresponding to revision F of the module were installed and an ECO corresponding to revision E of the module were not installed, the letter F would be scratched out and the letter E would remain intact.

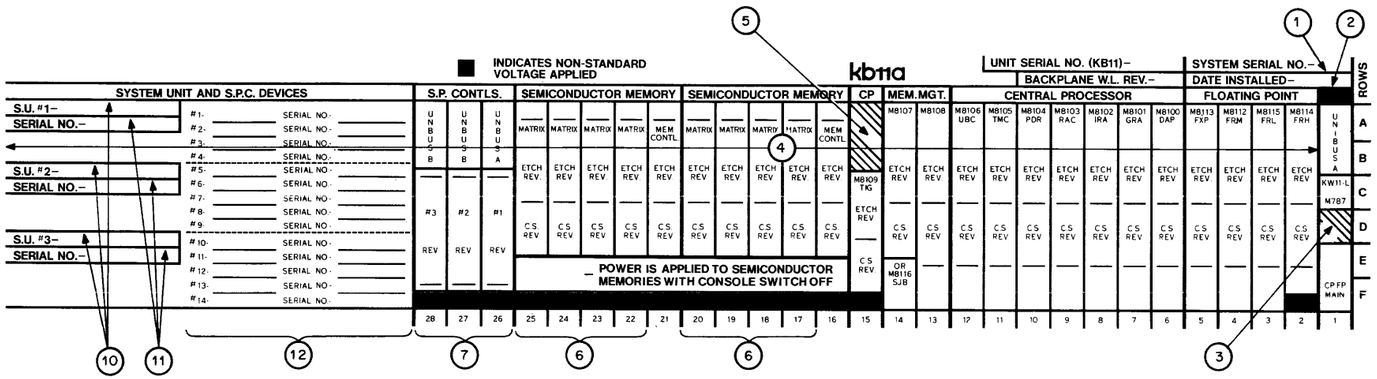
6.10.4 Module Utilization List (MUL) Sticker

This sticker (Figure 6-21), located on the top panel of the BA11-FA mounting box (left-hand side), provides a quick convenient tabulation of the various equipments located in a particular processor box. Additional information such as serial numbers, comments, technical tips, and installation of partial ECOs is also shown on the sticker. Table 6-11 describes the manner in which the sticker is to be filled out and indicates the department (production/field service) responsible for filling out the various items.

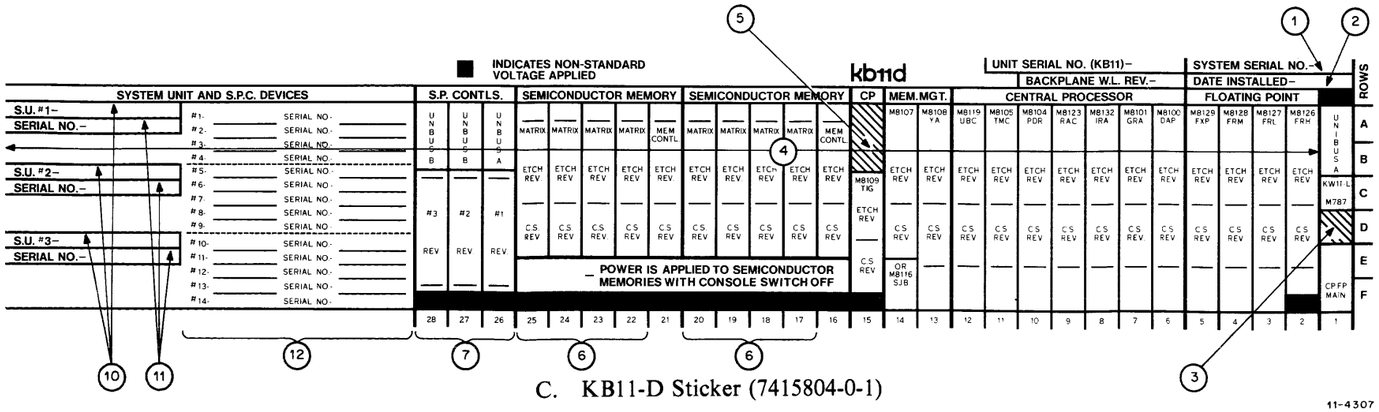


11-1499

A. Early KB11-A Sticker (DEC-3-378-1474-N272)



B. New KB11-A Sticker (7415804-0-0)



C. KB11-D Sticker (7415804-0-1)

11-4307

Figure 6-21 MUL Stickers

Table 6-11 Completing MUL Sticker

Item No.	Responsibility	Description
1	Production	System Serial Number
2	Field Service	Acceptance Date of installation at customer site.
3	None	Unused
4	Field Service	Comment area. Note tech tips installed, partial ECOs, miscellaneous information about module or slot.
5	None	For in-house use.
6	Production/Field Service*	Enter memory type as installed (G401, G401YQ, M8111, M8111-YA, M8121-YA). Comments should list address of memory.
7	Production/Field Service*	List option designation as installed (e.g., KL11, PC11, etc.).
8	Production/Field Service*	Enter module type for control module (e.g., M780 for KL11, etc.).
9	Production/Field Service*	Enter option serial number.
10	Production/Field Service*	List system unit device type (e.g., MM11-S, DD11-A, MM11-F, etc.).
11	Production/Field Service*	List system unit serial number.
12	Production/Field Service*	List option designation code devices within DD11-A, B, D if applicable (e.g., LP11, CR11, etc.). Also include small peripheral serial numbers.

* To be filled out by production if option or device is factory installed. If option or device is an add-on in the field, field service will complete these items.

Note: The MUL STICKER is located on the top of the KB11-A, D cover over the modules.

CHAPTER 7
PLUG-IN CARD OPTIONS

This chapter provides the information needed to install PC board options in an existing PDP-11/45, 11/50, 11/55 system. Options included are:

FP11-B Floating Point Processor (for the KB11-A)
FP11-C FLoating Point Processor (for the KB11-D)
KT11-C Memory Management Unit (for the KB11-A)
KT11-CD Memory Management Unit (for the KB11-D)
MS11 Semiconductor Memory Systems
KW11 Line Clock

Additional SPC Space
The DD11 system interfacing unit provides additional SPC slot positions for plug-in card options other than those provided by the standard backplanes and system units. It is usually mounted in the processor cabinet or expansion cabinet. The DD11-A and DD11-B each provide four SPC slots and are described in the *PDP-11 Peripherals Handbook*. The DD11-D provides nine SPC slots and a modified Unibus connection. (A description of the DD11-D is provided in the *PDP-11/34 System User Guide* - EK-11034-OP.)

7.1 FP11-B, C FLOATING POINT PROCESSOR

7.1.1 Installation
The following steps outline the procedure necessary to install the FP11-B, C Floating-Point Processor.

1. Turn power off at the console by shutting off both circuit breakers on the power supplies.

2. Install the H744 +5 V regulator in slot A of the upper H742 power supply as indicated on the power supply decal located at the rear of the CPU mounting box.

3. Install FRH module (M8114 for the FP11-B or M8126 for the FP11-C) in slot 2 of the CPU backplane assembly (Figure 5-12).

4. Install FRL module (M8115 for the FP11-B or M8127 for the FP11-C) in slot 3 of the CPU backplane assembly.

5. Install FRM module (M8112 for the FP11-B or M8128 for the FP11-C) in slot 4 of the CPU backplane assembly.

6. Install FXP module (M8113 for the FP11-B or M8129 for the FP11-C) in slot 5 of the CPU backplane assembly.

7. Turn circuit breakers on and recheck the +5 Vdc and -15 Vdc regulator outputs for proper voltages. Readjust as required in accordance with Paragraph 6.2.2. Refer to Table 6-2 for test points.

8. Set the Data Display switch on the console to μADRS FPP/CPU and press the HALT switch. The FP11-B, C microaddress should display 076. Connect an oscilloscope probe to A2A1 to determine that the oscillator is running. Press the START switch and check that the FP11-B, C cycles back to address 076.

9. Run the diagnostic programs listed below.

7.2 FP11 DIAGNOSTICS

7.2.1 FP11-B Diagnostics

Table 7-1 lists the diagnostic programs for the FP11-B Floating-Point Processor. These programs test the FP11-B in all modes with fixed number patterns. Additional test procedures for the FP11-B are provided in Paragraph 7.1.5.

Table 7-1 FP11-B Floating-Point Processor Diagnostic Programs

Number	Tests
MAINDEC-11-DCFPA-	CFCC, LDFPS, STFPS, SETI, SETL, SETF, and SETD Diagnostic
MAINDEC-11-DCFPB-	STST Diagnostic
MAINDEC-11-DCFPC-	LDF and STF, LDD and STD Diagnostic
MAINDEC-11-DCFPD-	ADDF and SUBF, ADDD and SUBD Diagnostic
MAINDEC-11-DCFPE-	CMPF, CMPD Diagnostic
MAINDEC-11-DCFPF-	MULF, MULD Diagnostic
MAINDEC-11-DCFPG-	DIVF, DIVD Diagnostic
MAINDEC-11-DCFPH-	CLRF, NEGF, ABSF, and TSTF Diagnostic
MAINDEC-11-DCFPI-	LDCDF, LDCFD, STCFD, and STCDF Diagnostic
MAINDEC-11-DCFPJ-	LDCIF, LDCID, LDCLF, LDCLD, STCFI, STCFL, STCKI, and STCDL Diagnostic
MAINDEC-11-DCFPK-	LDEXP and STEXP Diagnostic
MAINDEC-11-DCFPL-	MODF and MODD Diagnostic
MAINDEC-11-DCFPM-	LDUB, LDSC, STAO, MRS, and STQO Maintenance Instructions
MAINDEC-11-DCFPO-	Exercises all instructions
MAINDEC-11-DCFPR-	LDD and STD Exerciser
MAINDEC-11-DCFPS-	ADDF, ADDD, SUBF, and SUBD Exerciser
MAINDEC-11-DCFPT-	MULF and MULD Exerciser
MAINDEC-11-DCFPU-	DIVF and DIVD Exerciser
MAINDEC-11-DCQOA	OVERLAY

DCFPA through DCFPL Diagnostic - These programs test the FP11-B in all modes with fixed number patterns. The programs should be run in order for at least two passes with all switches down.

DCFPM Maintenance Instruction Test - This program tests the maintenance instructions and microtraps.

DCFPO Basic Instruction Exerciser - This program is a general test of all instructions.

DCFPR LDD/STD Exerciser – This program tests the load and store instructions, using random numbers.

DCFPS Add and Subtract Exerciser – This program tests the add and subtract instructions, using random numbers, and compares the results of these instructions with FORTRAN software.

DCFPT Multiply Exerciser – This program tests the multiply instruction, using random numbers, and compares the results of this instruction with FORTRAN software.

DCFPU Divide Exerciser – This program tests the divide instruction, using random numbers, and compares the results of this instruction with FORTRAN software.

DCQOA – Overlay diagnostic.

7.2.2 FP11-C Diagnostics

The diagnostic programs for the FP11-C Floating Point Point Processor are listed below. These programs consist of 237(8) individual tests designed and sequenced to detect and identify logic faults at a minimum hardware/software level. These tests are partitioned into two stand-alone programs as described below.

DEFPA Basic Instruction Tests – This program is a logically sequenced set of instruction tests designed to verify the logic operations and data paths used by the more complex instructions such as multiply and divide.

DEFPB Multiply and Divide ROM Tests – This program is a logically sequenced set of tests for the multiply, modulo, and divide instructions and the memory management ROM. Also included is a test of all the locations of the A-branch, No-mem branch, and ADX ROMs that have not previously been tested. This last test is also used to verify the "Disable Interrupt" bit in the control store of the FPP.

The error reports in these programs assume there are no previous errors and that there is only one failure in the FPP. This means that if the programs are not run in sequence, the error message may be invalid.

7.2.3 Using the Maintenance Card with the FP11-B, C

FP11-B, C operation in the maintenance modes selected by maintenance card switches S1 and S2 is similar to those operations described for the KB11-A, D. See Paragraph 6.5.

μPB STOP Mode – The FP11-B, C microbreak register is loaded with the required microprogram ROM address, using the FP11-B, C maintenance instruction LDUB (Load Microbreak Register), 170003, as described in the FP11-B or FP11-C manual. Basically, this procedure requires that the ROM address be deposited into the low-order byte of CPU general register R3. The LDUB instruction transfers this address to the FP11-B, C microbreak register. When the CONT switch is pressed, program execution will proceed until the contents of the FP11-B, C control ROM address register matches the contents of the microbreak register. When a match occurs, the FP11-B, C stops in time state TS2 of the ROM state.

ROM CYCL Mode – FP11-B operation in the ROM CYCL maintenance mode is identical to KB11-A, D operation in that mode (Paragraph 6.5.2.1). The FP11-B, C stops at time state TS2 of each successive ROM cycle.

SING TP Mode – Same operation as described for KB11-A, D (Paragraph 6.5.2.3).

7.2.3.1 FPP Test Timing – When FP11-B maintenance is required, the FP11-B module is extended with M900 module extenders and the FP11-B RC maintenance clock is used as a source of FPP timing. When FP11-C maintenance is required, the FP11-C module is extended with M900 module extenders and the KB11-D RC maintenance clock is used as a source of FPP timing. This is because the FP11-C is synchronized to the KB11-D.

Clock selection is described in Paragraph 6.5.1.

1. Connect an oscilloscope to measure FRHJ CLOCK A H (pin A02B2) for the FP11-B or T1GC TF H (pin D15M2) for the FP11-C at the CPU backplane.

2. For the FP11-B, adjust the potentiometer on the FRH module to provide a 50 ns FRHJ CLOCK A H repetition rate. (Note that this does not affect CPU timing.) For the FP11-C, adjust the potentiometer R162 on the T1G module (in the KB11-D) to provide a 30 ns T1GC TF H repetition rate. (Note that this affects CPU timing.)

7.2.4 FP11-B, C Floating-Point Processor Procedures

This paragraph describes maintenance techniques available for the FP11-B, C Floating-Point Processor. The procedures involve the use of the maintenance card (W131) and driver module (W130 or W133), mounted in slot E1 of the KB11-A, D CPU backplane. The use of the maintenance card is described in Paragraphs 6.5 and 7.1.3.

7.2.4.1 Time Margining of the FP11-B – The timing of the FP11-B RC clock can be varied by using the maintenance card with switch S3 in the RC position. Timing is adjusted by potentiometer R32 on the M8114 FRH module. The nominal limits are from 50 ns to 290 ns. Refer to the note in Paragraph 6.5.1.

7.2.4.2 Time Margining of the FP11-C – The timing of the FP11-C RC clock can be varied using the maintenance module with S4 in the RC position, by adjusting potentiometer R162 on the M8139 T1G module. (Note that this also adjusts the KB11-D maintenance timing.) The limits are from 27 ns minimum to 450 ns maximum. The time margins should be checked periodically to locate any potential problems due to increase in propagation delays of flip-flop switching times due to IC degradation.

7.2.4.3 Special Maintenance Instructions of the FP11-B – A set of five maintenance instructions is available to assist maintenance personnel. These instructions are described in the following paragraphs.

LDUB – Load Microbreak Register (170003) – This instruction causes the lower eight bits of general register 3 in the CPU to be loaded into the microbreak register LDUB can be used for the functions described in the following paragraphs, depending on the FMM bit (bit 4) in the program status word (FPS).

NOTE

The FMM bit in the status word is used to enable special maintenance logic. To set this bit, the CPU must be in Kernel mode.

With the FMM bit set, the microprogram will be aborted through the trap routine ROM address to the ready state after the state specified by the address (next sequential ROM state) in the microbreak register is detected. If the Interrupt Enable bit (bit 14) of the floating-point processor status word is set, the CPU will trap to location 244. An exception code of 16 will be stored in the FEC (floating exception code) register. The contents of the FEC register can be transferred to the CPU by the STST (store status) instruction. A second function, available as a result of the LDUB instruction, allows maintenance personnel to use the address match as a scope sync independent of the FMM bit. When the ROM address matches the contents of the microbreak register, the UMATCH flip-flop is set at the leading edge of TS1. The set output of this flip-flop (pin DK1 of slot 4 in the FXP module) is used as a scope sync to allow visual observation of events that occur duing a particular ROM state. UMATCH is cleared at the trailing edge of TS4, providing maintenance personnel with a sync signal that occurs at the beginning of a specified ROM state and ends at the beginning of the next ROM state.

LDSC – Load Step Counter (170004) – This maintenance instruction loads the 1's complement of the least significant six bits of general register 4 into the step counter. LDSC sets the SC LOADED flip-flop, provided FMM (bit 4) of the processor status word is set (CPU must be in Kernel mode to set FMM), which inhibits the ROM from loading the step counter. When the step counter is incremented to all 1s, the SC LOADED flip-flop is cleared. As a result of this instruction, maintenance personnel can set up the step counter to perform a specified number of steps in a multiply or divide routine and can stop where desired to examine the contents of the registers.

STA0 – Store AR in AC0 (170005) – This instruction transfers the contents of the AR to AC0, as described below:

AR ⟨57:35⟩ → AC0 ⟨57:35⟩ if FD = 0
AR ⟨57:3⟩ → AC0 ⟨57:3⟩ if FD = 1

STQ0 – Store QR in AC0 (170007) – This instruction transfers the contents of the QR to AC0, as described below:

QR ⟨57:35⟩ → AC0 ⟨57:35⟩ if FD = 0 QR
QR ⟨57:3⟩ → AC0 ⟨57:3⟩ if FD = 1

NOTE

The STA0 and STQ0 instructions are used to store the contents of the AR and QR (internal registers) in an AC. Since the contents of the AC can be transferred to memory, maintenance personnel are able to check the contents of the AR and QR registers.

MRS – Maintenance Right Shift (170006) – The Maintenance Right Shift instruction shifts the AR or QR one bit position to the right. This instruction is used with the STA0 instruction to allow AR59 and AR58 to be examined. Two MRS instructions are necessary to transfer AR59 to AR57 and AR58 to AR56. The MRS instruction is also used with the STQ0 instruction to allow bits QR59 and QR58 to be examined. Two MRS instructions are necessary to shift QR59 to QR57 and QR58 to QR56. AR59 and AR58 as well as QR59 and QR58 represent the sign bit and hidden bit, respectively. These bits are not transferred between the CPU and the FP11-B but are used in data calculations by the floating-point processor. Therefore, to examine the state of these two bits, the use of the MRS instruction is required.

7.2.4.4 Special Maintenance Instructions of the FP11-C – A set of four maintenance instructions is available to assist maintenance personnel. These instructions are described in the following paragraphs.

LDUB – Load Microbreak Register (170003) – This instruction causes the lower eight bits of general register 3 in the CPU to be loaded into the microbreak register. LDUB can be used for the functions described in the following paragraphs, depending on the FMM bit (bit 4) in the program status word (FPS).

NOTE

The FMM bit in the status word is used to enable special maintenance logic. To set this bit, the CPU must be in Kernel mode.

With the FMM bit set, the microprogram will be aborted through the trap routine ROM address to the ready state after the state specified by the address (next sequential ROM state) in the microbreak register is detected. If the Interrupt Enable bit (bit 14) of the floating-point processor status word is set, the CPU will trap to location 244. An exception code of 16 will be stored in the FEC (floating exception code) register. The contents of the FEC register can be transferred to the CPU by the STST (store status) instruction. A second function, available as a result of the LDUB instruction, allows maintenance personnel to use the address match as a scope sync independent of the FMM bit. When the ROM address matches the contents of the microbreak register, the UMATCH signal is present. This output is pin DB1 (slot 5 in the FXP module) and is used as a scope sync to allow visual observation of events that occur during a particular ROM state. Note that match occurs at T2 of the previous state and is negated at T2 of the selected state.

STA0 – Store AR in AC0 (170005) – This instruction transfers the contents of the AR to AC0, as described below:

AR ⟨57:35⟩ → AC0 ⟨57:35⟩ if FD = 0
AR ⟨57:3⟩ → AC0 ⟨57:3⟩ if FD = 1

STQ0 – Store QR in AC0 (170007) – This instruction transfers the contents of the QR to AC0, as described below:

QR ⟨57:35⟩ → AC0 ⟨57:35⟩ if FD = 0 QR
QR ⟨57:3⟩ → AC0 ⟨57:3⟩ if FD = 1

NOTE

The STA0 and STQ0 instructions are used to store the contents of the AR and QR (internal registers) in the AC. Since the contents of the AC can be transferred to memory, maintenance personnel are able to check the contents of the AR and QR registers.

MSN – Maintenance Shift by N (170004) – This instruction transfers the contents of register R4 to the shift control logic and causes the contents of the AR and QR to be right or left shifted by N. A negative number in R4 causes a right shift by that number and a positive number in R4 causes a left shift by that number.

7.2.4.5 Maintenance Instruction Programming Example – Program Example 7-1 demonstrates the use of the FP11-B maintenance instructions. A similar program can be written for the FP11-C. The program is a multiplication example, whereby the contents of the AR and QR are typed out with each incrementation of the step courter from 1 through 71. Note that the MRS instruction is used to get AR and QR bits 59 and 58 into general register R5 for the typeout in each pass through the loop.

Program Example 7-1

```
001000  012706  START:  MOV     #600,%6     ;SET UP STACK POINTER AT 600
001002  000600
001004  170127          LDFPS   #40220      ;DISABLE INTERRUPTS; SET DOUBLE AND MAINT. MODE
001006  040220
001010  172667          LDD     MLYR,AC2    ;LOAD MULTIPLIER IN AC2
001012  000204
001014  012703          MOV     #230,%3     ;SET REG. 3 to 230
001016  000230
001020  170003          LDUB                ;SET MBR TO 230
001022  005004          CLR     %4          ;CLEAR COUNTER
001024  005204  NXTMUL:  INC     %4          ;INCREMENT COUNTER
001026  170004          LDSC                ;LOAD 1'S COMPLEMENT OF R4 INTO SC
001030  012705  LSTMUL:  MOV     #QR+10,%5   ;SET UP REG. 5 TO STORAGE TABLE
001032  001166
001034  172567          LDD     MCND,AC1    ;LOAD MULTIPLICAND INTO AC1
001036  000150
001040  171102          MULD    AC2,AC1     ;DO PARTIAL MULTIPLY
001042  170007          STQ0                ;TRANSFER QR TO AC0
001044  174045          STD     AC0,-(5)    ;STORE QR IN TABLE
001046  042715          BIC     #177600,@5  ;CLEAR SIGN AND EXPONENT
001050  177600
001052  170005          STA0                ;STORE AR IN AC0
001054  174045          STD     AC0,-(5)    ;STORE AR IN TABLE
001056  042715          BIC     #177600,@5  ;CLEAR SIGN AND EXPONENT
001060  177600
001062  170006          MRS                 ;SHIFT AR AND QR RIGHT ONE PLACE
001064  170006          MRS                 ;SHIFT AR AND QR RIGHT ONE PLACE
001066  170007          STQ0                ;TRANSFER QR TO AC0
001070  174067          STD     AC0,TEMP    ;MOVE AC0 TO TEMP
001072  000134
001074  016703          MOV     TEMP,%3     ;MOVE MOST SIGNIFICANT 7 BITS OF QR TO R3
001076  000130
001100  042703          BIC     #177600,%3  ;CLEAR SIGN AND EXPONENT
001102  177600
001104  006303          ASL     %3          ;SHIFT MSB OF QR ONE PLACE LEFT
001106  006303          ASL     %3          ;SHIFT MSB OF QR ONE PLACE LEFT
001110  050365          BIS     %3,10(5)    ;SET QR59 AND QR58 IN TABLE
001112  000010
001114  170005          STA0                ;STORE AR IN AC0
001116  174067          STD     AC0,TEMP    ;MOVE AC0 TO TEMP
001120  000106
001122  016703          MOV     TEMP,%3     ;MOVE MOST SIGNIFICANT 7 BITS OF AR TO R3
001124  000102
001126  042703          BIC     #177600,%3  ;CLEAR SIGN AND EXPONENT
```

Program Example 7-1 (Cont.)

```
001130  177600
001132  006303          ASL     %3          ;SHIFT MSB OF AR ONE PLACE LEFT
001134  006303          ASL     %3          ;SHIFT MSB OF AR ONE PLACE LEFT
001136  050315          BIS     %3,@5       ;SET AR59 AND AR58 IN TABLE
001140  004567          JSR     %5,PRINT    ;PRINT AR AND QR
001142  000234
001144  000410          BR      .+22        ;BRANCH OVER ARGUMENTS
001146  000000  AR:     .FLT4   0           ;AR STORED IN THESE FOUR LOCATIONS
001150  000000
001152  000000
001154  000000
001156  000000  QR:     .FLT4   0           ;QR STORED IN THESE FOUR LOCATIONS
001160  000000
001162  000000
001164  000000
001166  020427          CMP     %4,#71      ;HAVE 71 PASSES BEEN DONE
001170  000071
001172  100714          BMI     NXTMUL      ;NO-DO NEXT PASS
001174  001402          BEQ     LSTPAS      ;YES-DO LAST PASS
001176  000167          JMP     START       ;THIS MULTIPLY COMPLETE-DO NEXT ONE
001200  177576
001202  005204  LSTPAS: INC     %4          ;INDICATE 72ND PASS
001204  000167          JMP     LSTMUL      ;DO LAST PASS WITHOUT LOADING SC.
001206  177620
001210  040052  MCND:   .WORD   040052
001212  125252          .WORD   125252
001214  125252          .WORD   125252
001216  125252          .WORD   125252
001220  040000  MYLAR:  .WORD   040000
001222  000000          .WORD   000000
001224  000000          .WORD   000000
001226  000000          .WORD   000000
001230  000000  TEMP:   .FLT4   0
001232  000000
001234  000000
001236  000000
        000001          .END
```

The fractional part of the multiplicand (1/2 or 0.1) is stored in the BR and fractional part of the multiplier (consisting of alternating 1s and 0s) is stored in the QR.

The multiplier has an exponent of 200 and the multiplicand has a exponent of 204. The sign bit is a 0 and the hidden bit is a 1. The result of each step of the multiplication is stored in the AR. The typeout of the listing after each step of the multiplication is shown in Table 7-2.

The contents of the AR and QR are typed out 57 times. On the 58th typeout, the step counter is not set and this last typeout represents the final product.

7.2.4.6 Console Display Features – The console can be used to display the floating-point ROM address and, under certain conditions, can display the contents of the EALU.

Table 7-2 Typeout of QR and AR

Step	AR	QR	Step	AR	QR
			29	1252525252000000000	0000000000525252525
			30	0525252525000000000	0000000000252525252
1	0000000000000000000	1252525252525252525	31	1252525252400000000	0000000000125252525
2	0000000000000000000	0525252525252525252	32	0525252525200000000	0000000000052525252
3	1000000000000000000	0252525252525252525	33	1252525252500000000	0000000000025252525
4	0400000000000000000	0125252525252525252	34	0525252525240000000	0000000000012525252
5	1200000000000000000	0052525252525252525	35	1252525252520000000	0000000000005252525
6	0500000000000000000	0025252525252525252	36	0525252525250000000	0000000000002525252
7	1240000000000000000	0012525252525252525	37	1252525252524000000	0000000000001252525
8	0520000000000000000	0005252525252525252	38	0525252525252000000	0000000000000525252
9	1250000000000000000	0002525252525252525	39	1252525252525000000	0000000000000252525
10	0524000000000000000	0001252525252525252	40	0525252525252400000	0000000000000125252
11	1252000000000000000	0000525252525252525	41	1252525252525200000	0000000000000052525
12	0525000000000000000	0000252525252525252	42	0525252525252500000	0000000000000025252
13	1252400000000000000	0000125252525252525	43	1252525252525240000	0000000000000012525
14	0525200000000000000	0000052525252525252	44	0525252525252520000	0000000000000005252
15	1252500000000000000	0000025252525252525	45	1252525252525250000	0000000000000002525
16	0525240000000000000	0000012525252525252	46	0525252525252524000	0000000000000001252
17	1252520000000000000	0000005252525252525	47	1252525252525252000	0000000000000000525
18	0525250000000000000	0000002525252525252	48	0525252525252525000	0000000000000000252
19	1252524000000000000	0000001252525252525	49	1252525252525252400	0000000000000000125
20	0525252000000000000	0000000525252525252	50	0525252525252525200	0000000000000000052
21	1252525000000000000	0000000252525252525	51	1252525252525252500	0000000000000000025
22	0525252400000000000	0000000125252525252	52	0525252525252525240	0000000000000000012
23	1252525200000000000	0000000052525252525	53	1252525252525252520	0000000000000000005
24	0525252500000000000	0000000025252525252	54	0525252525252525250	0000000000000000002
25	1252525240000000000	0000000012525252525	55	1252525252525252524	0000000000000000001
26	0525252520000000000	0000000005252525252	56	0525252525252525252	0000000000000000000
27	1252525250000000000	0000000002525252525	57	1252525252525252525	0000000000000000000
28	0525252524000000000	0000000001252525252	58	1252525252525252525	0000000000000000000
				1252525252525252525	0000000000000000000

Display of ROM Address – The 16 DATA indicators on the console can be used to display the 8-bit FPP ROM address and the 8-bit CPU ROM address. The FPP ROM address is diplayed on the high order byte DATA indicators (bits 15–08) and the CPU ROM address is displayed on the low order byte indicators (bits 07–00). The four-position data selector switch on the console must be set to the μADDR FPP/CPU position to display the ROM address.

NOTE

If the maintenance card is set up to perform single ROM cycles or micromatch, the FPP ROM address displayed is the next ROM address, i.e., the address of the next ROM state to be cycled, because the ROM address changes at the end of time state 2 and a pause or wait state occurs between time state 2 and time state 3. If the maintenance card is set up to perform single clock cycles during time states 1 and 2, the ROM address displayed is the current address; for single clock cycles during time states 3 and 4, the ROM address displayed is the next address.

Display of EALU Contents – In certain ROM states of the CPU, the contents of the EALU may be displayed on the lower 16 ADDRESS indicators (bits 15–00) on the console. These CPU ROM states are unique to F class instructions and are listed in Table 7-3.

Table 7-3 Class F CPU ROM States

ROM State	Octal Address
FOP.30	173
FOP.50	211
FOP.60	362
FOP.70	316
FOP.80	376
FOP.90	375
FOP.40	36
FSV.20	225

NOTE
The contents of the EALU at any of these ROM states is dependent on the FP ROM state occurring at that time. Both the FPP and the CPU should be set up for single step operation, using both the CPU and FPP maintenance cards to see meaningful data in these ROM states.

The 8-position address selector switch on the console must be set to CONS.PHYS or PROG.PHYS.

7.3 KT11-C, CD MEMORY MANAGEMENT UNIT

7.3.1 Installation

Use the following procedure to install the KT11-C, CD Memory Management Unit.

1. Turn switched power off at the console by shutting off both circuit breakers on the power supplies.

2. Install SSR module (M8108 for the KT11-C or M8108-YA for the KT11-CD) in slot 13 of the CPU backplane assembly.

3. Install SAP module M8107 in slot 14 of the CPU backplane assembly.

NOTE
SAP Module M8107 replaces the SJB Module M8116, which is located in slot 14 when the KT11-C, CD is not installed.

4. Turn circuit breakers on.

5. Measure the voltage at pin A13A2, which receives +5 Vdc from the H744 +5 V regulator located in slot C of the H7420 power supply. If voltage is not correct, adjust voltage as required (Paragraph 6.2.2).

6. Run the KT11-C, CD Memory Management Unit diagnostic programs listed below to verify that the KT11-C, CD is operating properly.

7.3.2 Diagnostics

Table 7-4 lists the diagnostic programs for the KT11-C, CD Memory Management Unit option. If a fault is suspected in the KT11-C, CD prior to running the diagnostics, the internal registers (status, page address, and page description) should be checked at the console for proper operation. The addresses of the status registers are:

SR0 - 777572
SR1 - 777574
SR2 - 777576
SR3 - 772516

Table 7-4 KT11-C, CD Memory Management Unit Diagnostic Programs

Number	Tests
MAINDEC-11-DCKTA-A	Basic Logic Test, Part 1
MAINDEC-11-DCKTB-A	Basic Logic Test, Part 2
MAINDEC-11-DCKTC-A	Access Keys Test
MAINDEC-11-DCKTD-A	Move to Previous I/D Space Test
MAINDEC-11-DCKTE-A	Move from Previous I/D Space Test
MAINDEC-11-DCKTF-A	Abort Tests
MAINDEC-11-DCKTG-A	Memory Management Exerciser

The addresses of the page address and page description registers are given in Table 2-1 of the KT11-C, CD manual. Bits 12 through 15 of the Page Address Registers are not used, and bits 4, 5 and 15 of the Page Description Registers are not used. Press the DEP and EXAM switches for each of the registers.

DCKTA and DCKTB Basic Logic Tests One and Two - Tests the basic logic, including write into PAR and PDR, and all status registers.

DCKTC Access Keys Tests - Performs a test of all access control field (ACF) keys to verify that each key provides the required results for valid and invalid access attempts.

DCKTD MTPD/I with Memory Management - Tests the MTPD and MTPI instructions with the KT11-C, CD enabled. The instructions are executed in all combinations of current and previous mode conditions.

DCKTE MFPD/I with Memory Management - Tests the MFPD and MFPI instructions with the KT11-C, CD enabled. The instructions are executed in all combinations of current and previous mode conditions.

DCKTF Memory Management Abort Tests – Tests the memory management abort errors. This diagnostic causes an abort of each BUST of the KB11-A, D. Following the abort, the diagnostic checks for correct information in the status registers and on the stack. The sequence of tests begins with Page 1 of the microflows and proceeds from left to right.

DCKTG KT11-C, CD Exerciser – Exercises basic KT11-C, CD Memory Management Unit functions. In addition, this diagnostic uses all available memory and will run many I/O devices simultaneously with KT11-C, CD tests.

7.4 MS11 SEMICONDUCTOR MEMORY

7.4.1 Installation

Table 1-2 and 1-3 indicates the wide range of MOS and bipolar memory configurations that can be implemented in a PDP-11/45, 11/50, 11/55 system. Table 7-5 provides a summary of the semiconductor memory available. Before installing a semiconductor memory system, the user should be completely familiar with the MS11-B MOS and MS11-A, C bipolar memory options, described in the *MS11-A, B, C Memory Systems Maintenance Manual.* The MS11 manual presents comprehensive coverage of all optional jumper connections.

Table 7-5 MS11 Memory Configurations

Matrix	MS11-AP*	MS11-BR, BT	MS11-CM, CP
Matrix Size	4K Bipolar	4K MOS	1K Bipolar
Matrix Module	M8121-YA	G401	M8111
Controller	MS11-C	MS11-B	MS11-CC
Controller Capacity	4K Bipolar	4K MOS	1K Bipolar
Controller Module	M8120	M8110	M8120†

*Only the parity version (MS11-AP, M8121-YA) is available.

†Early versions use the M8110.

7.4.1.1 Semiconductor Memory Jumper Connections – When MOS or bipolar memory is installed, certain jumpers are to be cut or installed, depending on the range of memory addresses desired. The following paragraphs describe the jumper connections for the MOS and bipolar memory matrix boards, followed by a description of the jumpers for the memory controller.

NOTE

To fully utilize MOS or bipolar memory speed, the MOS memory address should be cut for the *lower* portion of memory (0–XK). However, if power fail recovery is a critical requirement, it may be more desirable to locate core memory in the 0–4K portion of the total memory range.

In either case, the DEC Field Service Representative should contact the customer so that optimum use can be made of the memory system. We suggest that MS11-CM or -CP bipolar memory be addressed as the last segment of memory because it is expandable in 1K increments; however, when configuring a total memory system, the customer should always be advised of the variables to determine the optimum configuration for each installation.

MOS – Table 7-6 contains the required jumper configuration for the assignment of the 4K block of MOS memory addresses. If, for example, a G401 MOS memory matrix has jumpers C and B installed, then that matrix contains memory locations XX4096 through XX8191. The Xs preceding the number denote that the memory addresses can be selected anywhere in the range from 0 to 128K. Any address from 4096 to 8191 is recognized and responded to by the matrix.

Table 7-6 G401 MOS Memory Matrix Selected Address Configuration (4 of 16K)

MAD		Required Jumpers		MOS Matrix Memory Address Assignment
14	13	(MAD 14)	(MAD 13)	
0	0	C	A	0 – 4095
0	1	C	B	4096 – 8191
1	0	D	A	8192 – 12,287
1	1	D	B	12,288 – 16,383

MAD 02 and MAD 01 (not jumper selected) further define a particular 1K block of addresses within the specified 4K block (Table 7-7).

Table 7-7 G401 MOS Memory Matrix Control Level Generation and Selected Memory Address Block (1 of 4K)

MAD		Memory Address Block Selected
02	01	
0	0	0 – 1023
0	1	1024 – 2047
1	0	2048 – 3071
1	1	3072 – 4095

Bipolar – The M8111 and M8121-YA bipolar memory matrix decodes Unibus or Fastbus address bits ⟨14:11⟩. The selective jumpering of these bits on an M8111 1K memory module, or the selective switching of these bits on an M8121-YA 4K memory module, can designate that memory module as having a unique set of consecutive addresses within the total set of 16K addresses. Table 7-8 lists the jumper connections and the corresponding address set selected by each jumper configuration on the M8111 module. Table 7-8 also lists the switch positions and the corresponding address set selected by each switch configuration on the M8121-YA module. The M8111 jumpers are wire-wrapped in place. As in the MOS matrix, addresses can be selected on both types of bipolar matricies from 0 to 128K when used with an M8120 or M8110 control module.

M8110 and M8120 SMC Module – The jumper connections on the M8110 and M8120 SMC module are designated by E numbers. Jumpers are located on E67, E75, E78 and E87 (described in the following paragraphs). All jumpers are prewired on the controller module; for a specific address configuration, jumper wires must be cut. If the configuration is changed it is necessary to reinstall some jumpers previously cut. Refer to the *MS11-A, B, C Memory Systems Maintenance Manual* and related engineering drawing set for detailed information pertaining to the various jumper connections.

Table 7-8 M8111 and M8121-YA Bipolar Matrix Selected Address Configuration

Unibus/Fastbus				M8111 Required Jumpers				M8121-YA SI Switches Closed (Denoted by X)				Memory Address Assignment
14	13	12	11					MAD 14		MAD 13		
MAD								1	0	1	0	
14	13	11	10	(MAD 14)	(MAD 13)	(MAD 11)	(MAD 10)	A	B	C	D	
0	0	0	0	D	F	H	B		X		X	0 to 1023
0	0	0	1	D	F	H	A		X		X	1024 to 2047
0	0	1	0	D	F	J	B		X		X	2048 to 3071
0	0	1	1	D	F	J	A		X		X	3072 to 4095
0	1	0	0	D	E	H	B		X	X		4096 to 5119
0	1	0	1	D	E	H	A		X	X		5120 to 6143
0	1	1	0	D	E	J	B		X	X		6144 to 7167
0	1	1	1	D	E	J	A		X	X		7168 to 8191
1	0	0	0	C	F	H	B	X			X	8192 to 9215
1	0	0	1	C	F	H	A	X			X	9216 to 10,239
1	0	1	0	C	F	J	B	X			X	10,240 to 11,263
1	0	1	1	C	F	J	A	X			X	11,264 to 12,287
1	1	0	0	C	E	H	B	X		X		12,288 to 13,311
1	1	0	1	C	E	H	A	X		X		13,312 to 14,335
1	1	1	0	C	E	J	B	X		X		14,336 to 15,359
1	1	1	1	C	E	J	A	X		X		15,360 to 16,383

E67 – Figure 7-1 shows the jumper connections at E67 that interface the Fastbus to the controller for MOS and bipolar memory. Note that bits 13 and 14 are designated for MOS and 4K bipolar, and bits 11 and 12 for 1K bipolar. Note also that SMCF DECODE 14 and SMCF DECODE 13 are connected only for MOS memory and 4K bipolar.

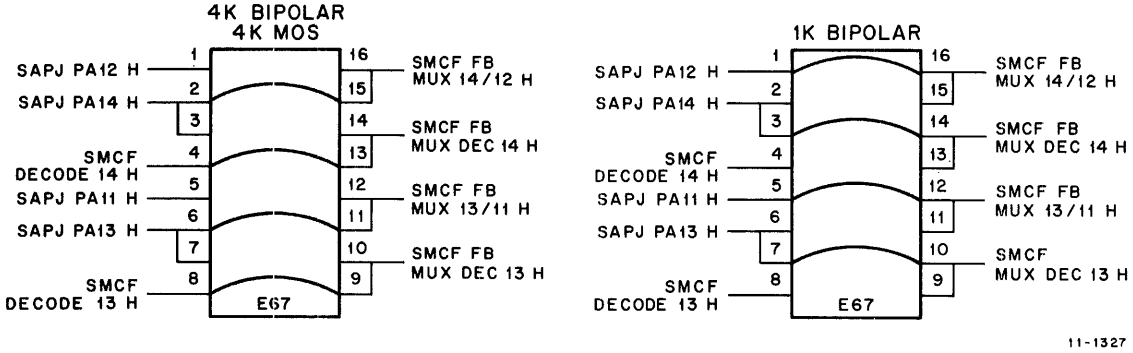


Figure 7-1 Fastbus Multiplexing ⟨14:11⟩ Required E67 Jumper Configuration

E78 – Figure 7-2 shows the jumper connections at E78 that interface the Unibus to the controller for MOS and bipolar memory. Note that bits 13 and 14 are associated with MOS and 4K bipolar, and bits 11 and 12 are associated with 1K bipolar. Also note that SMCF DECODE 14 and SMCF DECODE 13 are not connected for 1K bipolar.

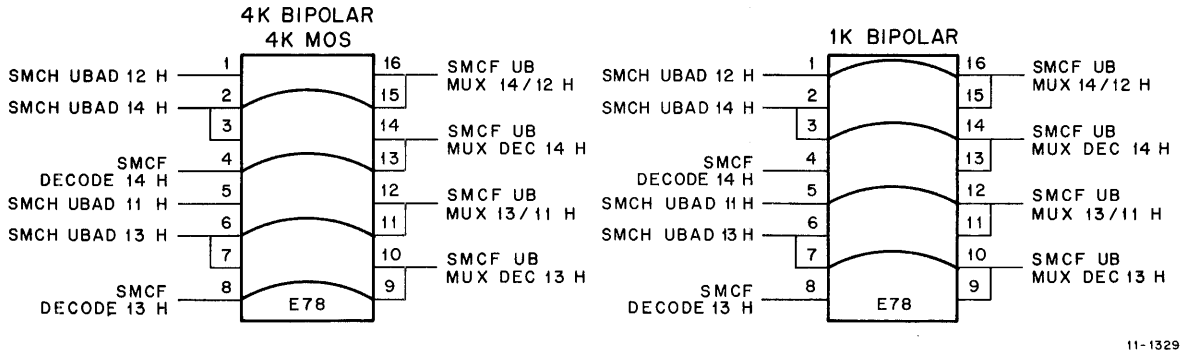


Figure 7-2 Unibus Multiplexing ⟨14:11⟩ Required E78 Jumper Configuration

E75 – The jumpers at E75 permit Fastbus and Unibus address selection. Four of these jumpers correspond to Fastbus addresses and four correspond to Unibus addresses. Each jumper allows the M8110 or M8120 control to respond to a 4K group of addresses; thus, each M8110 or M8120 can control up to 16K words. The corresponding jumper is removed if memory is present for the associated address group.

Table 7-9 illustrates the required jumper connections for both MOS and bipolar memory. Assume that MOS memory is connected to a controller and jumper J is cut. In this case, memory addresses from 0 to 4K are assigned to memory, and the controller will recognize and respond to this group of addresses from the Fastbus. If jumper N is cut, the controller will recognize and respond to these addresses from the Unibus. Table 7-10 shows the jumper configuration as additional memory matrices are added to a memory controller. For example, if MOS memory is connected to the controller, and it is desired to have the controller respond to addresses from 0 to 12K from the Unibus jumpers N, P, and R must be cut. If, at some future date, it is desired to reconfigure the memory from 4K to 12K, for example, jumper N must be reinstalled.

Table 7-9 MOS/Bipolar Module Addressing

4K MOS or 4K Bipolar			Fastbus	Unibus	1K Bipolar		
Address Bit		Memory Address Assignment	Remove Jumper	Remove Jumper	Memory Address Assignment	Address Bit	
14	13					12	11
0	0	0–4095	J	N	0–1023	0	0
0	1	4096–8191	K	P	1024–2047	0	1
1	0	8192–12,287	L	R	2048–3071	1	0
1	1	12,288–16,383	M	S	3072–4095	1	1

Table 7-10 MOS/Bipolar Memory Addressing (More Than One Matrix)

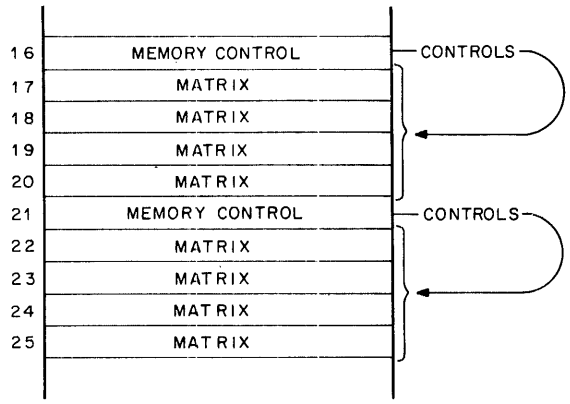
No. of Memory Modules in Memory	Memory Capacity		Remove Jumpers	
	4K MOS or 4K Bipolar	1K Bipolar	Fastbus Address Select	Unibus Address Select
1	4K	1K	J	N
2	8K	2K	JK	NP
3	12K	3K	JKL	NPR
4	16K	4K	JKLM	NPRS

*Connected to one M8110/M8120 Control.

E87 – Jumpers C, D, E, F, and H are used to assign a block of MOS or bipolar addresses to a controller from the total available address area from 0 to 12K (Table 7-11). For example, to have the controller respond to bipolar memory addresses from 120K to 124K, jumpers C, D, E, and F must be cut. Jumpers C, D, and E allow assignment of 16K words within the total address space; jumpers F and H allow assignment of 4K words within the assigned 16K.

For MOS memory, jumper A is cut. If this jumper is not cut, the controller is configured for bipolar memory and refresh is inhibited. If the parity option is installed, jumper B is cut to enable the Parity Control Register. If jumper T, is cut, Parity Register address bit 1 will be a 1; if jumper T is not cut, this bit will be a 0. See Drawing D-CS-M8110-0-1, sheet SMCF or the equivalent M8120 drawing.

7.4.1.2 Installation of Bipolar Memory – The CPU backplane of the PDP-11/45, 11/50, 11/55, provides slots for eight memory matricies and two memory controllers. Refer to Figure 7-3. Note the CPU backplane section and dedicated slots. The controller of slot 16 addresses the matricies of slots 17 through 20. The controller of slot 21 addresses the matricies of slots 23 through 25. Each M8120 controller is jumpered to provide either 4K or 1K matrix operation; thus only that type of matrix can be placed in the corresponding matrix slots. For example, if the M8120 controller is jumpered for 1K operation, one, two, three or four M8111 modules of bipolar memory may be placed in its corresponding slots to provide 1K, 2K, 3K, or 4K of memory.



NOTE:
Slots 17-20 can contain either 1K BIPOLAR, 4K BIPOLAR, or 4K MOS modules according to the jumper configuration on the corresponding memory control. Likewise for slots 22-25; however, MOS can be used in slots 22-25 ONLY if slots 17-20 contain MOS. (For MOS/BIPOLAR combination, MOS MUST be in slots 17-20.

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Figure 7-3 CPU Backplane Memory Slots

Table 7-11 Fastbus/Unibus Memory Address (Assign and Decode)

Fastbus/Unibus Address Decoder Bits					Memory Address Assignment		M8120 or M8110 Jumpers (E87) (NOTE 1, NOTE 2)				
17	16	15	14	13	1K Bipolar	4K MOS or 4K Bipolar	C	D	E	F	H
0	0	0	0	0	0–4K	0–16K					
0	0	0	0	1	4–8K	↓					X
0	0	0	1	0	8–12K					X	
0	0	0	1	1	12–16K	↓				X	X
0	0	1	0	0	16–20K	16–32K			X		
0	0	1	0	1	20–24K	↓			X		X
0	0	1	1	0	24–28K				X	X	
0	0	1	1	1	28–32K	↓			X	X	X
0	1	0	0	0	32–36K	32–48K		X			
0	1	0	0	1	36–40K	↓		X			X
0	1	0	1	0	40–44K			X		X	
0	1	0	1	1	44–48K	↓		X		X	X
0	1	1	0	0	48–52K	48–64K		X	X		
0	1	1	0	1	52–56K	↓		X	X		X
0	1	1	1	0	56–60K			X	X	X	
0	1	1	1	1	60–64K	↓		X	X	X	X
1	0	0	0	0	64–68K	64–80K	X				
1	0	0	0	1	68–72K	↓	X				X
1	0	0	1	0	72–76K		X			X	
1	0	0	1	1	76–80K	↓	X			X	X
1	0	1	0	0	80–84K	80–96K	X		X		
1	0	1	0	1	84–88K	↓	X		X		X
1	0	1	1	0	88–92K		X		X	X	
1	0	1	1	1	92–96K	↓	X		X	X	X
1	1	0	0	0	96–100K	96–112K	X	X			
1	1	0	0	1	100–104K	↓	X	X			X
1	1	0	1	0	104–108K		X	X		X	
1	1	0	1	1	108–112K	↓	X	X		X	X
1	1	1	0	0	112–116K	112–128K	X	X	X		
1	1	1	0	1	116–120K	↓	X	X	X		X
1	1	1	1	0	120–124K		X	X	X	X	
1	1	1	1	1	124–128K	↓	X	X	X	X	X

NOTES: 1. "X" denotes jumper to be cut.
2. Jumpers F and 11 are left intact for all 4K memory assignments, i.e., when assigning address to G401 and M8121 modules.

Note that a combination of 1K and 4K modules may be utilized on the same backplane provided the respective controller is jumpered for such operation. Thus, a maximum of two types of memory may be used in one backplane (two controllers). The following steps outline the procedures for installation of the bipolar memory.

1. Turn off H7420 (or H742) power supply circuit breakers.

2. Install H744 regulators and M8120 SMC control modules, and cut power harness jumpers per Table 7-12, depending on amount of Bipolar memory.

Table 7-12 Bipolar Memory Configurations

M8121	⩽ 8K	⩽ 16K	⩽ 24K	> 24K
M8111	⩽ 2K	⩽ 4K	⩽ 6K	> 6K
	Slot J no jumpers cut	Slots J, H cut P5-7, 8	Slots J, H, K cut P5-7, 8 cut P5-3, 4	Slots J, H, K, L cut P5-7, 8 cut P5-3, 4 cut P6-7, 8
	M8120 in CPU Slot 16		M8120 in CPU Slot 21	

Note: Early Bipolar versions used an M8110 control.

3. Install the M8121(4K) or M8111(1K) memory matrix modules (-YA versions signify memory with parity).

4. Note that:

   a. Each M8120 can control up to four M8111s or up to four M8121s.

   b. Each H744 +5 V regulator can supply enough current for only one M8120, plus two M8111s or M8121s. The H744 is rated at 25A.

   c. Installation of bipolar memory must start at slot 16.

   d. Refer to Figure 5-3 for +5 V regulator configurations.

5. Turn on the power supply circuit breakers.

6. Measure +5 V at each of the points indicated in Table 7-13.

7. Adjust voltages if required as described in Paragraph 6.2.2.

8. Refer to the *MS11-A, B, C Memory Systems Maintenance Manual* and the MS11 engineering print set for appropriate timing adjustments.

Table 7-13 Bipolar Memory Voltage Checks

Regulator Slot	Voltage	Point of Measurement
Slot H	+5 Vdc	Between A19A2 and ground
Slot J	+5 Vdc	Between A16A2 and ground
Slot K	+5 Vdc	Between A21A2 and ground
Slot L	+5 Vdc	Between A24A2 and ground

7.4.1.3 Installation of MOS Memory (MS11-B) – From 4K to 32K of MOS memory in increments of 4K, can be installed in the PDP-11/45, 11/50 system. The MS11-BC memory option controls 16K of MOS memory (Table 1-2). If more than 16K of MOS memory capacity is desired, an additional MS11-BD memory control is required. The procedure for installing MOS memory is described below.

1. Turn off circuit breakers on both the H7420 power supplies. Install the H744 +5 V regulator (part of the MS11-BC) in slot J of the lower H7420 power supply.

2. Install the H746 MOS regulator in slot H of the lower H7420 power supply.

3. Install the M8110 SMC module in slot 16 of the CPU backplane assembly and install the G401 MOS memory matrix modules in the CPU backplane assembly in slots 17–20 (maximum of four G401 modules per M8110).

NOTE

If MS11-BP (memory parity) option is selected, the MOS memory matrix modules are designated G401YA.

4. If more than 16K of memory is required, install the second M8110 SMC module that comprises the MS11-BD memory control in slot 21 of the CPU backplane assembly. Install the additional G401 MOS memory matrix modules starting at slot 22 of the CPU backplane assembly. Install additional H746 regulator in slot L of the lower H7420. Modification of the backplane is required if the power system revision letter is E or lower. See Table 5-1.

5. Turn on circuit breakers and measure the voltage from A16A2 of the CPU backplane to ground for +5 Vdc.

6. Measure the following voltages at the points indicated below:

Voltage	CPU Backplane Point of Measurement
+23.2 Vdc	Pin A17V2 and ground (Rev F and up A22V2 and ground)
+19.7 Vdc	Pin A17U2 and ground (Rev F and up A22U2 and ground)
−5 Vdc	Pin F17C1 and ground

7. Readjust as required in accordance with Paragraph 6.2.2.

NOTE

Do not cut any jumpers on the power harness when installing MOS memory.

8. Refer to the *MS11-A, B, C Memory Systems Maintenance Manual* and the MS11 engineering print set for appropriate timing adjustments.

7.4.1.4 Installation of both MOS and Bipolar Memory – The installation for combined MOS and bipolar memory is described below.

1. Turn off H7420 (or H742) power supply circuit breakers.

2. Cut the jumper between P5-3 and -4 on the power harness.

3. Install the H746 MOS regulator in slot H of the lower H7420 power supply.

4. Install one H744 +5 V regulator in slot J of the lower H7420 power supply.

5. Install second H744 +5 V regulator in slot K of the lower H7420 power supply.

6. If more than 2K of M8111 or more than 8K of M8121 bipolar memory is installed, install third H744 +5 V regulator in slot L of the lower H7420 power supply. Cut the jumper between P6-7 and -8 on the power distribution cable harness.

7. Install the M8110 SMC module supplied as part of the MS11-BC MOS memory control option in slot 16 of the CPU backplane assembly.

8. Install the G401 MOS memory matrices (G401YA if memory parity is selected), starting at slot 17 of the CPU backplane assembly. Up to four modules can be installed.

9. Install the M8120 SMC module supplied as part of the MS11-CC (or -AP) bipolar memory control in slot 21 of the CPU backplane assembly.

10. Install the M8111 or M8121 bipolar memory matrix modules in the CPU backplane assembly (-YA with memory parity) starting at slot 22 of the CPU backplane assembly.

11. Turn on power supply circuit breakers.

12. Measure the following voltages between the points indicated.

Voltage	CPU Backplane
+ 5.0 Vdc	Between A16A2 and ground
+23.2 Vdc	Between A17V2 and ground
+19.7 Vdc	Between A17U2 and ground
− 5.0 Vdc	Between F17C1 and ground
+ 5.0 Vdc	Between A21A2 and ground
+ 5.0 Vdc	Between A24A2 and ground

13. Adjust voltages if required as described in Paragraph 6.2.2.

NOTE

All M8110 and M8120 module adjustments have been made at the factory. If further adjustment is required, use the latest SMC module circuit schematic for the proper adjustment procedure.

7.4.2 Semiconductor Memory Calibration

Semiconductor memories must be calibrated before use. The procedures for this are set forth in the MS11 print set and Chapter 4 of the *MS11-A, B, C Memory Systems Maintenance Manual.*

7.4.3 Diagnostics

The diagnostic programs used with the MS11 Semiconductor Memory System are briefly described in the following paragraphs. Specific calibration and maintenance procedures are provided in Paragraph 7.3.2 of this manual, as well as the *MS11-A, B, C Memory Systems Maintenance Manual.* Table 7-14 lists the diagnostic programs used with the MS11.

Table 7-14 MS11 Semiconductor Memory System Diagnostic Programs

Number	Tests
MAINDEC-11-DZMSA- (1)	Logic
MAINDEC-11-DZQMA- (2)	Mem Ex > 28K
MAINDEC-11-DZQMB-	0–124K Memory Exerciser
MAINDEC-11-DCMFA- (3)	Parity Check

(1) MOS Memories only
(2) Requires NPR device input
(3) Parity memories only

DZMSA Memory Parity Test – The Memory Parity Test reads the semiconductor control parity register addressed and prints out on the 33 ASR whether or not the register exists. If the addressed register does exist, the function of each register bit is tested. This diagnostic will also load the addressed register and initiate parity write/read tests in the memory section designated, and permit error interrupts as specified by the state of the pertinent parity register bit.

DZQMA – This test checks memory up to 124K, using NPR devices.

DZQMB – This test checks 0–124K of memory for unique addressing and worst-case noise patterns.

DCMFA – This program locates the Parity Memory Registers for both the core and MOS parity memories and performs a check of the bits in each. It then creates a map showing the memory controlled by each Parity Register. The Parity Registers and the memory are then tested using the information in the map.

7.5 KW11-L LINE CLOCK

1. Shut power off.
2. Cut the jumper between C01R2 and C01V2 on the CPU backpanel.
3. Install the KW11-L module in slot 1, row C of CPU.
4. The following programs may be used to check the operation of the KW11-L:

   a. INTERRUPT MODE
   The following program is an example of one way the KW11-L can be used in the interrupt mode. This program is intended to enter the routine TIME after every N interrupts. The mnemonic LKS represents the permanent memory address of the KW11-L, 777546; LKV represents the vector address, 100. When the main program is interrupted, it is directed to LKV, and then to LKV +2, which is 102. The word in location 100 is the address of the first instruction in the interrupt service routine; this address is transferred into the program counter of the processor. The word in location 102 is the new status word, which is transferred into the status register of the processor. The new status word contains the number 300, which indicates a priority level of 6, with all five condition codes, T, Z, N, V, and C equal to 0.

```
        LKS = 777546
        LKV = 100
MAIN:   MOV #N, CNTR
        MOV #100, LKS       ;ENB INTR
              .
              .
              .
LKV:    LKSERV
        300
LKSERV: MOV #100, LKS       ;Clear bit 7. This instruction is optional
        DEC CNTR
        BEQ TIME            ;If counter is zero, go to time.
                            ;If counter is not
                            ;zero, continue.
        RTI
TIME:   MOV #N, CNTR        ;Reset counter
              .
              .
              .
        RTI
```

Program Example 7-2

b. NONINTERRUPT MODE

The following program is an example of one way the KW11-L can be used in the noninterrupt mode. In this example, it is assumed that an INIT or a previous DATO with D06 = 0 has placed the KW11-L in the noninterrupt mode. This program alternates between two program routines – each lasting for approximately the time period between line clock changes, which is either 16.67 ms or 20 ms. Each routine contains a program loop that lasts for a considerably shorter time than the period between line clock changes. The mnemonic LKS represents the permanent memory address of the KW11-L, 777546.

```
          LKS = 777546
START:    CLRB  LKS         ;Reset bit 7
SYNC:     TSTB  LKS         ;Wait until bit 7 is set,
          BPL   SYNC        ;Then reset it
          CLRB  LKS         ;Clear bit
ON:               .         ;Do first routine
                  .
                  .
          TSTB  LKS         ;Each time through loop test bit 7
          BPL   ON          ;When bit is set
          CLRB  LKS         ;Clear bit
OFF:              .         ;Do second routine
                  .
                  .
          TSTB  LKS         ;Test bit 7
          BPL   OFF         ;If not set, do loop again
          CLRB  LKS         ;If set, clear bit
          JMP   ON          ;Do first program again
```

Program Example 7-3

CHAPTER 8
SYSTEM UNIT OPTIONS

8.1 SYSTEM UNITS

Many of the options available for the PDP-11/45, 11/50, 11/55 systems consist either in whole or in part of system units. Appendix C lists these as SU in the Mounting Code column. A system unit consists of:

1. The backplane, which can be be either single (four card slots) or double (nine card slots), and either wire-wrapped or printed circuit etch connected.

2. PC module(s) that plug into the backplane.

3. A power harness (option harness) that brings power from the cabinet power distribution system to the option backplane. Harness numbers are listed in Appendix C.

If the system unit is a peripheral device controller, the cable to the peripheral device plugs into a connector on one of the modules. System units may be installed, within the limits set by the applicable configuration rules, in either the CPU or in an expansion cabinet. Three single system units can be installed in the PDP-11/45, 11/50, 11/55 CPU cabinet and nine in an H960-D expansion cabinet; a double SU takes up the space of two single units.

8.2 EXPANSION CABINETS

The H960-D cabinet contains one BA11-FB mounting box containing up to nine system units and an associated H7420 (or H742) power supply. The H960-C Version of the expansion cabinet is merely the empty cabinet frame and panels. The ac power distribution for the cabinet is shown in engineering drawing D-IC-H960-0.

The ac power control system is the same as that for the CPU cabinet, which is explained in Chapter 4 of this manual, with the exception that only one (switched) H7420 (or H742) is provided per BA11-FB mounting box.

The voltage regulator complement varies with the system unit configuration. DC power distribution is explained in Paragraph 8.3.

8.3 DC POWER DISTRIBUTION

Refer to the block diagram of Figure 8-1. Chapter 3 of this manual refers to the power harness in the lower half of the figure connecting the power supplies with the CPU backplane, console, and distribution board. A second power harness is needed to connect a third power supply and the distribution boards of the expansion cabinet. The power distribution boards provide a link between the power harnesses and option harnesses (SU power harnesses). Each power distribution board can handle three system units; therefore, the CPU cabinet contains one distribution board and the expansion cabinet contains three distribution boards.

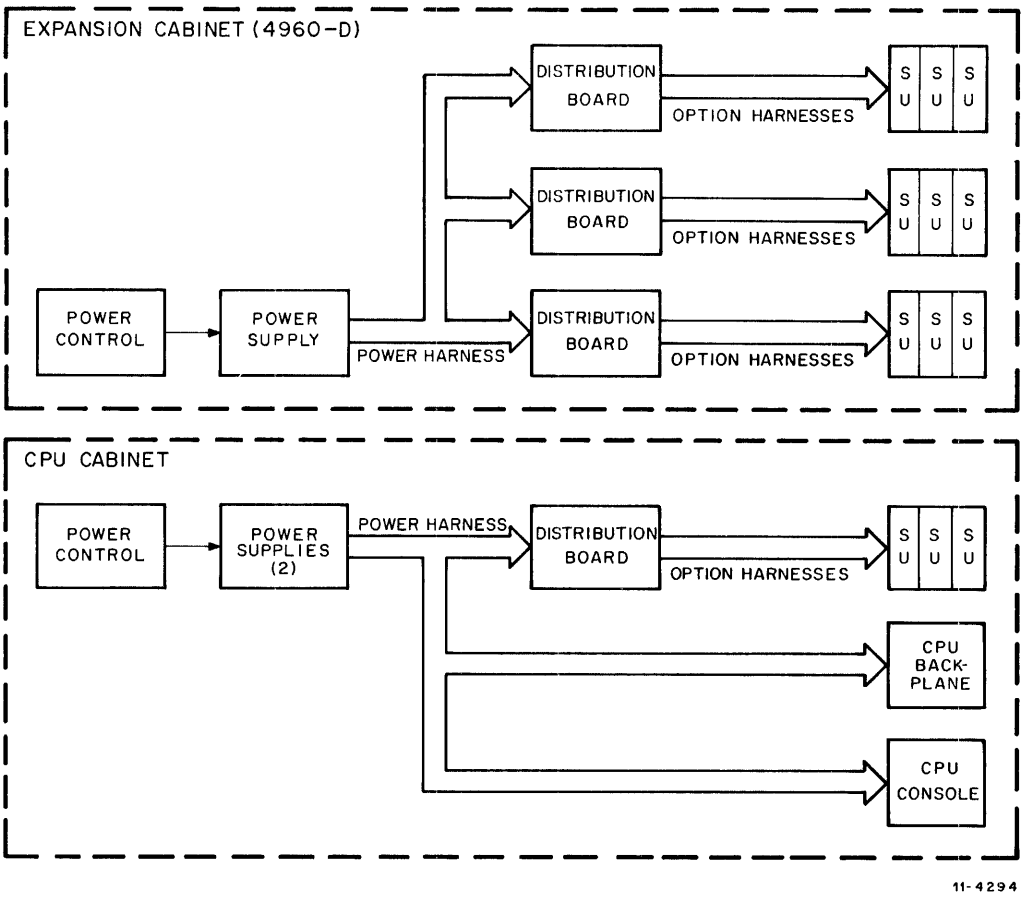


Figure 8-1 DC Power Distribution; Simplified Block Diagram

Paragraph 3.3 of this manual defines four versions of the dc power distribution system in terms of control, harness, and supply. When CPU cabinet serial number 2000 was produced, its power distribution board was also changed with the power harness. When expansion cabinet serial number 7000 was produced, its power distribution boards and power harness were also changed. These changes are tabulated in Table 8-1.

Distribution board location is described in the following paragraphs.

Table 8-1 Power Distribution Components

Part	Version	Cabinet	
		CPU	H960-D
Harness	Older	7008784	7008754
	Newer	7009540	7009566
Distribution Board	Older	5409903	5409944
	Newer	5410590	5410590

8.3.1 CPU Cabinet

The connectors of the distribution board for the SU power harnesses (option harnesses) are at the rear of the CPU mounting box in the older versions (Figures 8-3 and 1-1) and at the top of the CPU box in the newer versions (Figures 8-2 and 1-1). See engineering drawings D-UA-11/45-0-1 for more detail on both versions. (Equivalent 11/50 or 11/55 drawings present detail on newer versions only.)

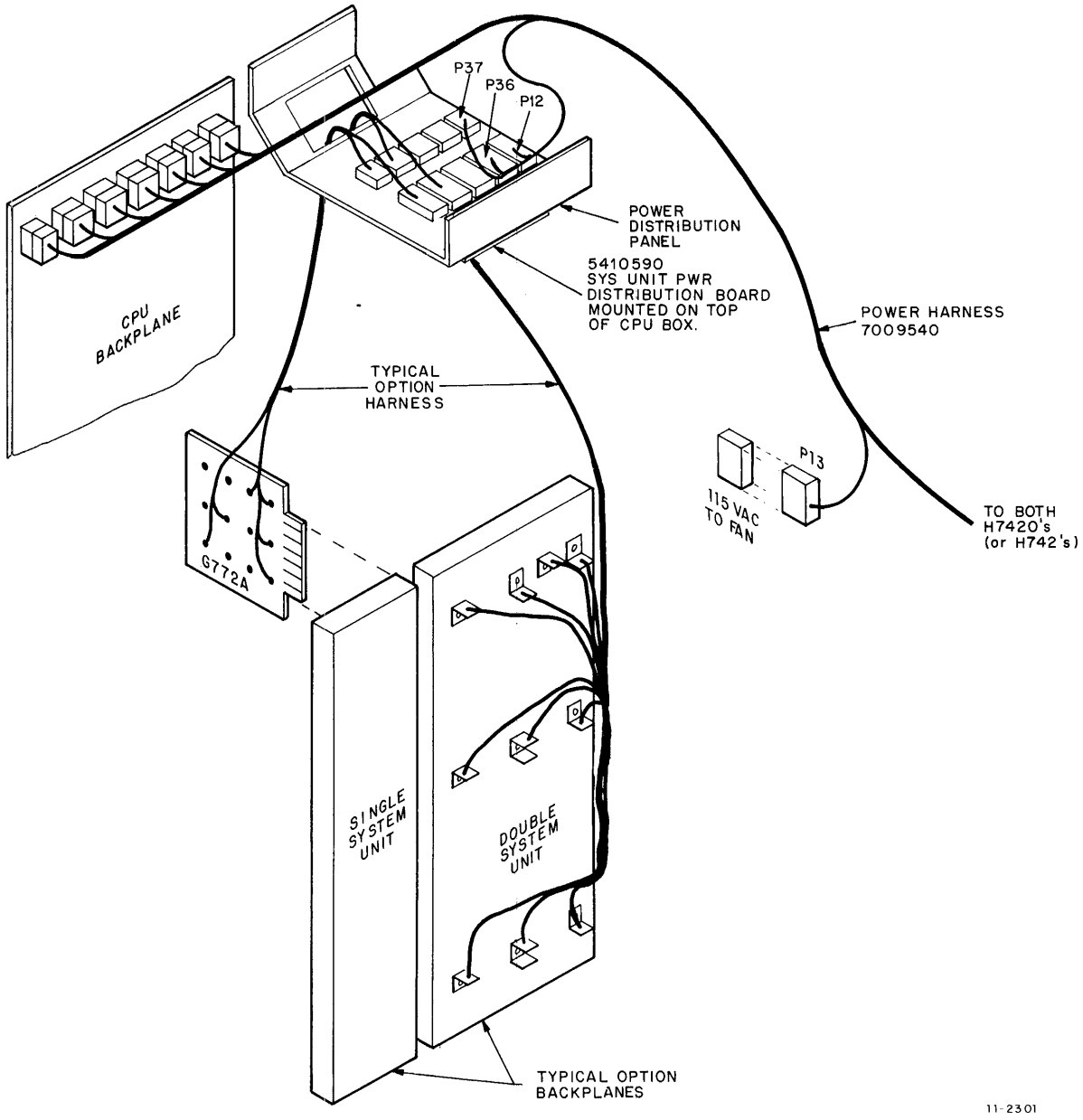


Figure 8-2 Installation of System Units, Later Systems, CPU Cabinet Serial Numbers 2000 and Higher

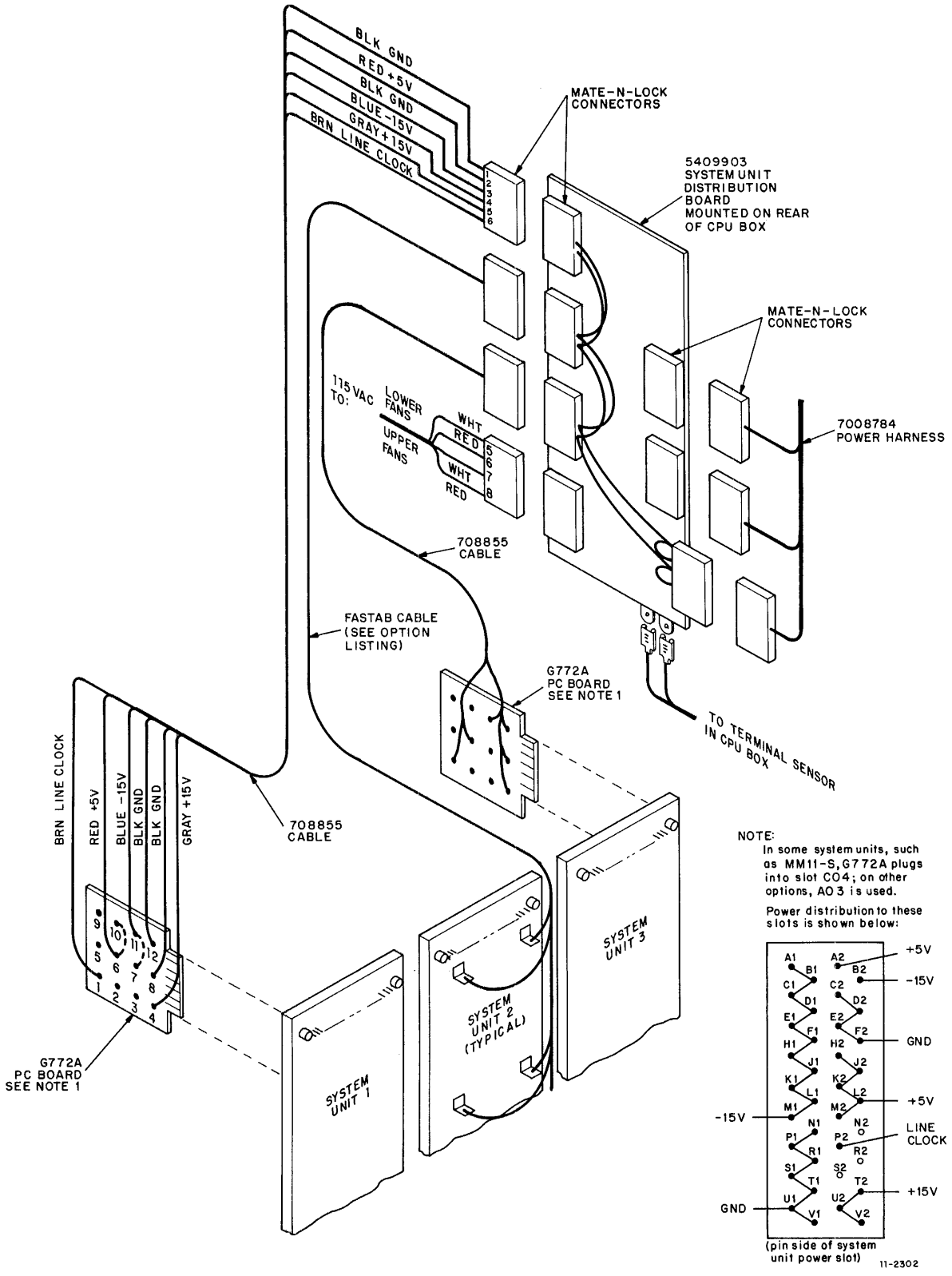


Figure 8-3 Installation of System Units, Early Systems, CPU Cabinet Serial Numbers Less than 2000

8.3.2 Expansion Cabinets

In the older versions the power distribution boards are mounted vertically and are shown in Figure 8-5; the newer ones are mounted horizontally and shown in Figure 8-4. Drawings D-UA-H960-D-0 show the complete assembly of both old and new expansion cabinets. The newer harness is installed in cabinets bearing serial numbers 7000 and higher.

8.4 MF11 CORE MEMORY

A system unit option for the PDP-11/45, 11/50, and 11/55 is the MF11 Core Memory System. Refer to the *MF11-U/UP Core Memory System Maintenance Manual* (EK-MF11U-MM-003) for installation and maintenance procedures. The diagnostic programs used with the MF11 Memory Systems are described briefly below. Table 8-2 lists the diagnostic programs used with the MF11.

Table 8-2 MF11 Core Memory System Diagnostic Programs

Number	Tests
MAINDEC-11-DZMMJ	Mem 0–24K
MAINDEC-11-DZQMA (1)	Mem I/O Exerciser
MAINDEC-11-DZQMB	0–124K Memory Exerciser
MAINDEC-11-DCMFA (2)	Mem Parity Control Logic Check

(1) Requires NPR device input
(2) Parity memories only

DZMMJ – This program is a combination of eight test patterns that can be used to test 0–24K of memory. This program may find problems not found by DZQMB.

DZQMA – This test checks memory up to 124K, using NPR devices.

DZQMB – This test checks 0–124K of memory for unique addressing and worst-case noise patterns.

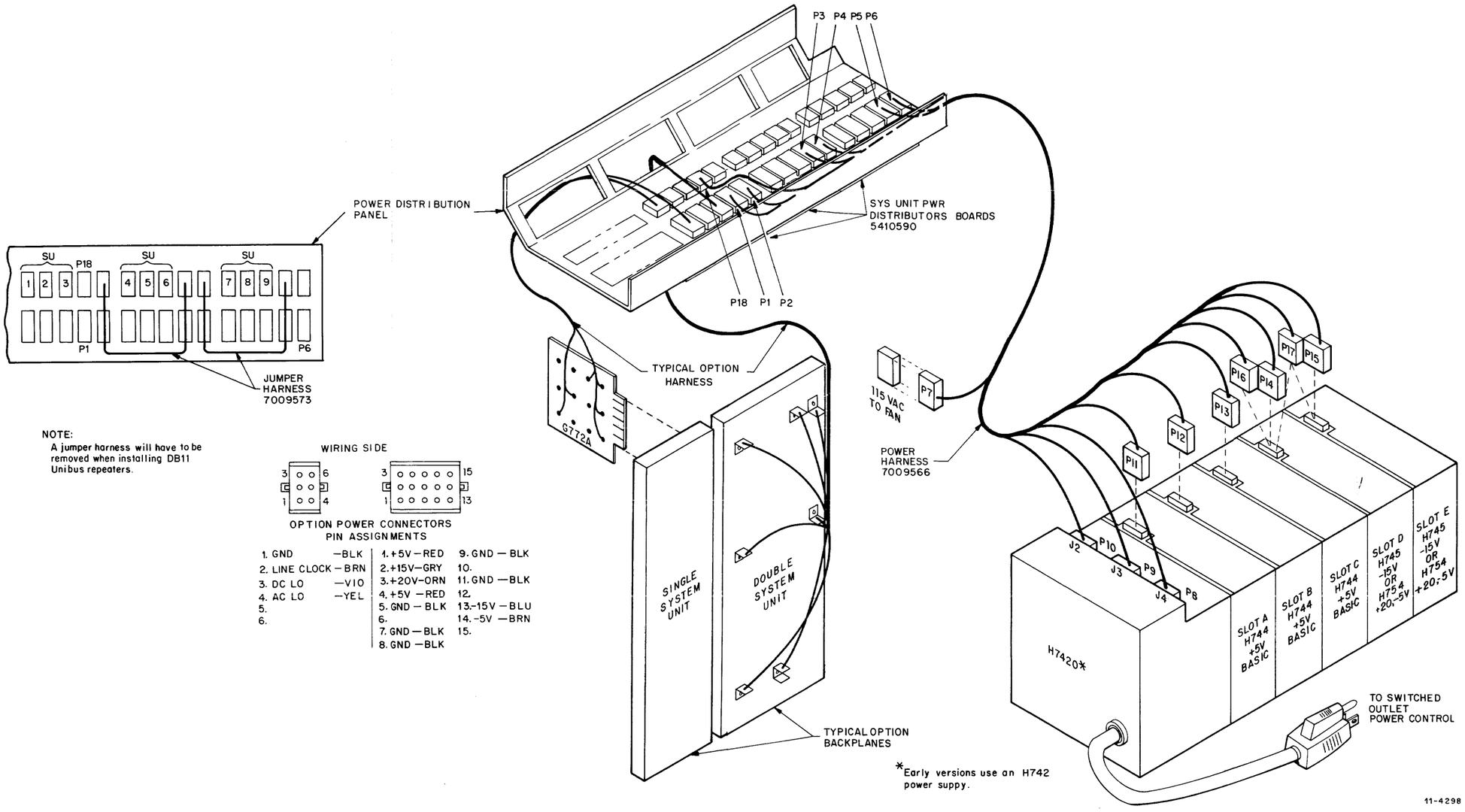
DCMFA – This program locates the Parity Memory Registers for the memory and performs a check of the bits in each. It then creates a map showing the Memory controlled by each parity register. The Parity Registers and the memory are then tested using the information in the map.

8.5 INSTALLATION OF SYSTEM UNIT

The installation of a system unit requires the items listed in Table 8-3.

Table 8-3 SU Installation Requirements

Qty	Item	Remarks
1	Backplane	
1	Power Harness	See Appendix C
1	M920 Unibus Jumper Module	Except when the SU is the first installed in a BA11-FB expansion box.



NOTE:
A jumper harness will have to be removed when installing DB11 Unibus repeaters.

WIRING SIDE

OPTION POWER CONNECTORS
PIN ASSIGNMENTS

1. GND	—BLK	1. +5V — RED	9. GND — BLK
2. LINE CLOCK	— BRN	2. +15V—GRY	10.
3. DC LO	—VIO	3. +20V—ORN	11. GND —BLK
4. AC LO	—YEL	4. +5V —RED	12.
5.		5. GND — BLK	13. -15V — BLU
6.		6.	14. -5V —BRN
		7. GND — BLK	15.
		8. GND —BLK	

Figure 8-4 Expansion Cabinet Power Distribution
Cabinet Serial Numbers 7000 and Higher

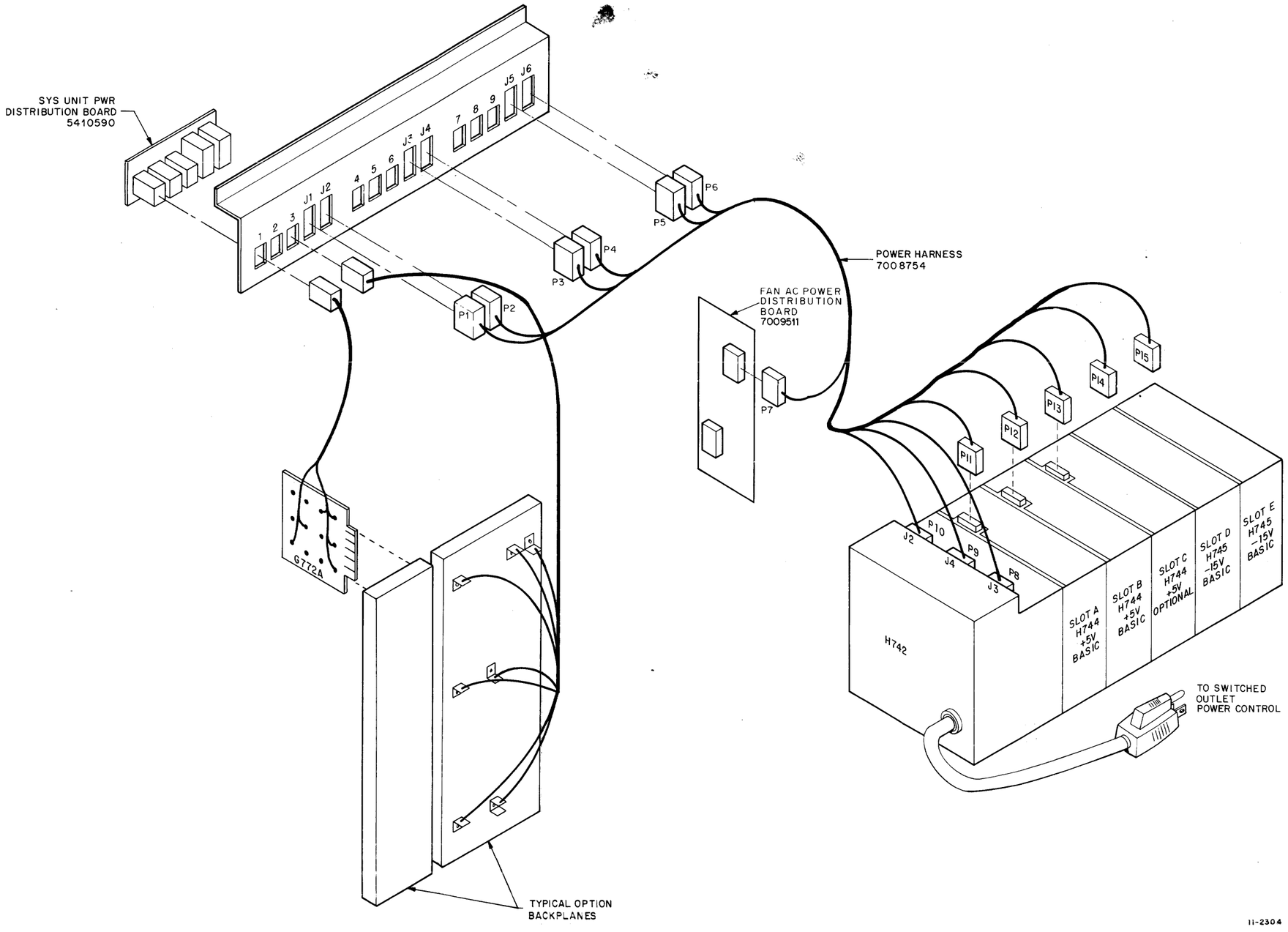


Figure 8-5 Expansion Cabinet Power Distribution
Cabinet Serial Numbers Less than 6999

The following steps outline the procedure to be used when installing a system unit option. The rear of the CPU mounting box, which is housed in the H960-CA or H960-DB (Table 1-1) processor cabinet, can accommodate three system units. An additional nine system units can be installed in an expansion cabinet mounting box, which is housed in the H960-D cabinet.

1. Install the required number of system units in the H960 cabinets and secure them to the mounting boxes, using the thumbscrews provided.

2. Plug in the system unit power cables. Two types are used: one connects to the SU backplane by means of a G772A power connector card (see Figure 8-3 for wiring details); the other uses Fastab connectors. The G772As are standard, while the Fastab harnesses vary with the option. The other end of this cable has one (older systems) or two (newer versions) Mate-N-Lok connectors which plug into the power distributor panels. Installation is shown in detail as indicated in Table 8-4.

Table 8-4 SU Power Cable Installation

Version	Cabinet	
	CPU	H960-D
older	Figure 8-3	Figure 8-5
newer	Figure 8-2	Figure 8-4

3. Plug in an M920 Unibus jumper module for each system unit that is installed. This module jumpers the Unibus from one system unit to slots A01, B01 of the next system unit.

   When system units are to be installed in an H960-D expansion cabinet, a Unibus cable is connected from the last system unit in the processor cabinet to the first system unit in the expansion cabinet.

4. A special case is that of an MF11-U/UP 16K memory installed in an old style H960-D cabinet (it cannot be used in an old version CPU cabinet). In this case (Figure 8-6) a 7009569 conversion harness must be used between the H754 +20, -5 Vdc regulator and the backplane, in addition to the 7009568 harness to the power distributor. One 7009569 can power two MF11-U/UP backplanes. If only one is used, the jumpers between backplanes should be cut. One 7009568 is required per backplane.

   A field modification kit (FM11-U) is available for these installations. The FM11-U permits installation of one or two MF11-U/UP backplanes. Refer to the field modification kit print set for installation procedures (DD-FM11-U).

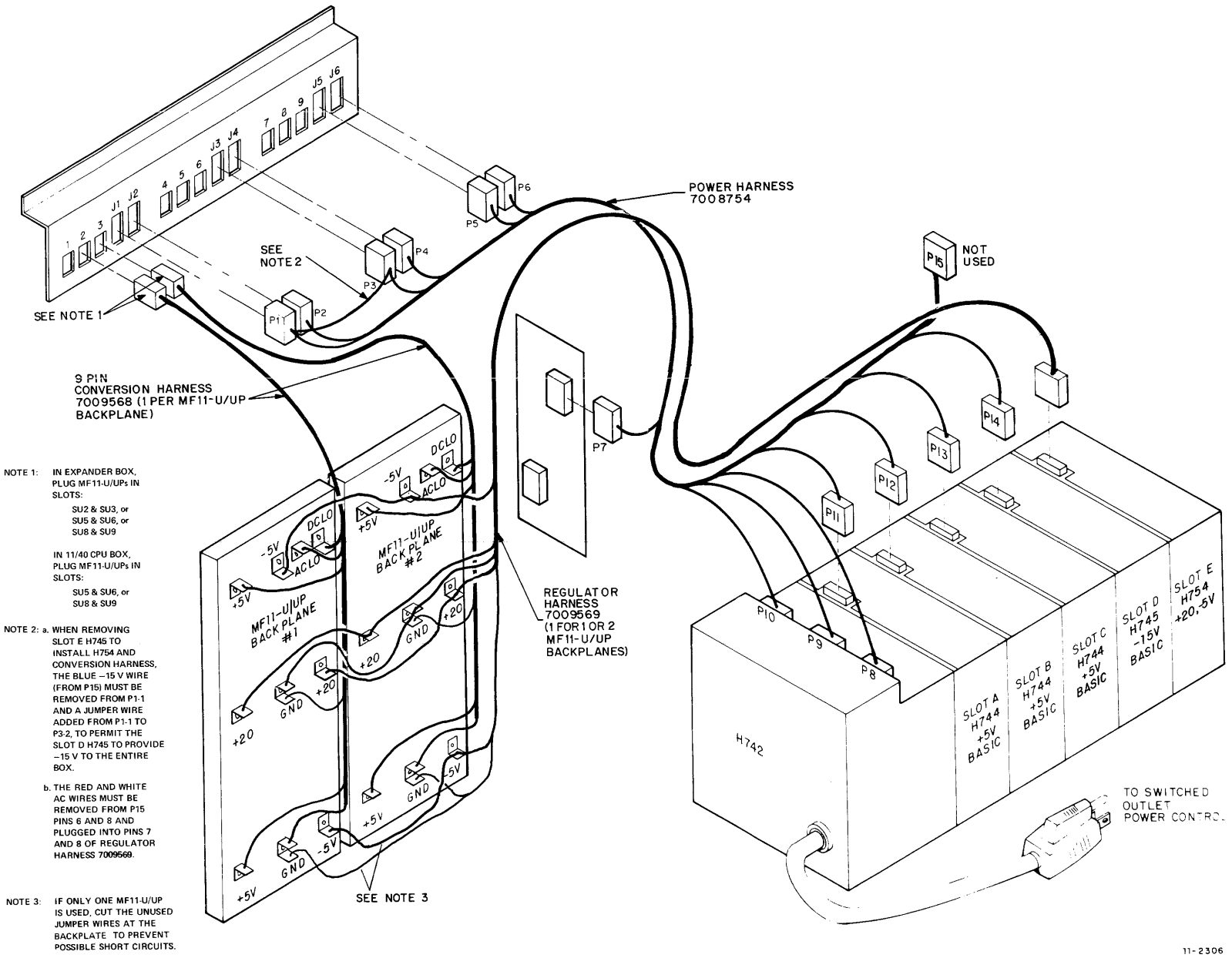


Figure 8-6 Installation of MF11-U/UP and FM-11 Kit In Early Systems, Expansion Cabinet Serial Numbers Less than 6999

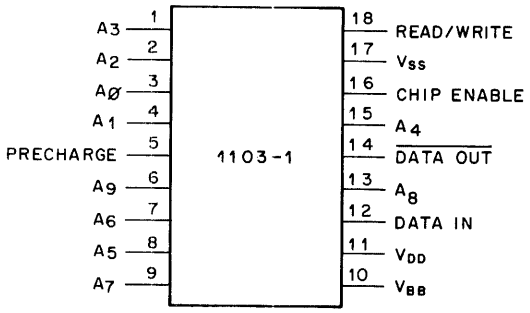
APPENDIX A
IC DESCRIPTIONS

The following ICs are described in this appendix. The S or H version of an IC listed below merely indicates high speed.

1103-1	1024-Bit MOS RAM
3101	Random Access Memory
3404	Latch
7474	D-Type Edge-Triggered Flip-Flops
7485	4-Bit Comparator
82S10*	1024-Bit Bipolar RAM
8251	BCD to Decimal Decoders
8598	Read-Only Memory
74112	Dual J-K Edge-Triggered Flip-Flops
74123	One-Shot
74151	8-Line to 1-Line Multiplexer
74153	Dual 4-Line to 1-Line Data Selector/Multiplexers
74154	4-Line to 16-Line Demultiplexer
74155	3-Line to 8-Line Decoder
74157	Quad 2-Line to 1-Line Multiplexer
74158	Quad 2-Line to 1-Line Multiplexer
74161	4-Bit Binary Counter
74174	Hex D-Type Flip-Flops
74175	Quad D-Type Flip-Flops
74181	4-Bit Arithmetic Unit with Full Look-Ahead
74182	Look-Ahead Carry Generator
74187	1024-Bit Read-Only Memory
74191	4-Bit Binary Counter
74193	4-Bit Binary Counter
74194	Parallel-Access Shift Register with Mode Control
75107	Sense Amplifier (Dual-In-Line)

* 82S10 is not the high-speed version of the 8210. (The 8210 is an 8-channel digital switch and not a product of the 82S10 vendor.)

1103-1 1024-BIT MOS RAM



LOGIC Ø = high voltage level
LOGIC 1 = low voltage level

TRUTH TABLE

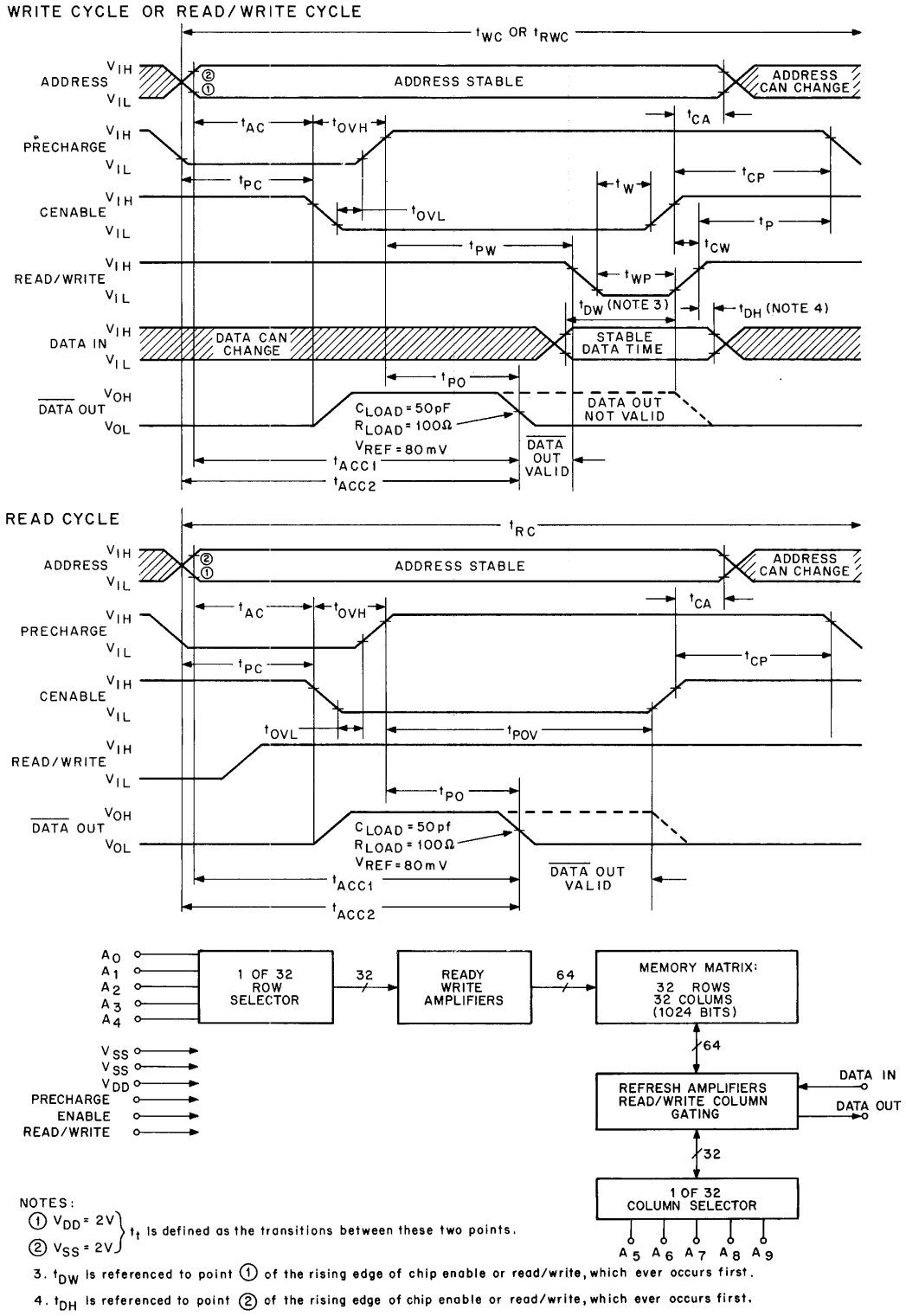
INPUTS		OUTPUT	MODE
CE	R/W		
H	X	L	not selected
L	H	D_{OUT}	Read
L ↓ L	H ↓ L	D_{OUT} ↓ L	Write or Read/Write

H=high voltage level
L=low voltage level
X=irrelevant

NOTES:
1. A chip enable is provided for memory array expansion.

2. Before any read/write, or read/write cycle, a precharge pulse is required to refresh the addressed memory bit. For a read cycle the data is read from the addressed location when the chip is selected during the end of a precharge pulse and read/write is held high. For a write or read/write cycle the read cycle is executed, however before any enable is unasserted, read/write is held low. This writes the new data (DATA IN) into the addressed location.

IC-1103-1A



NOTES:

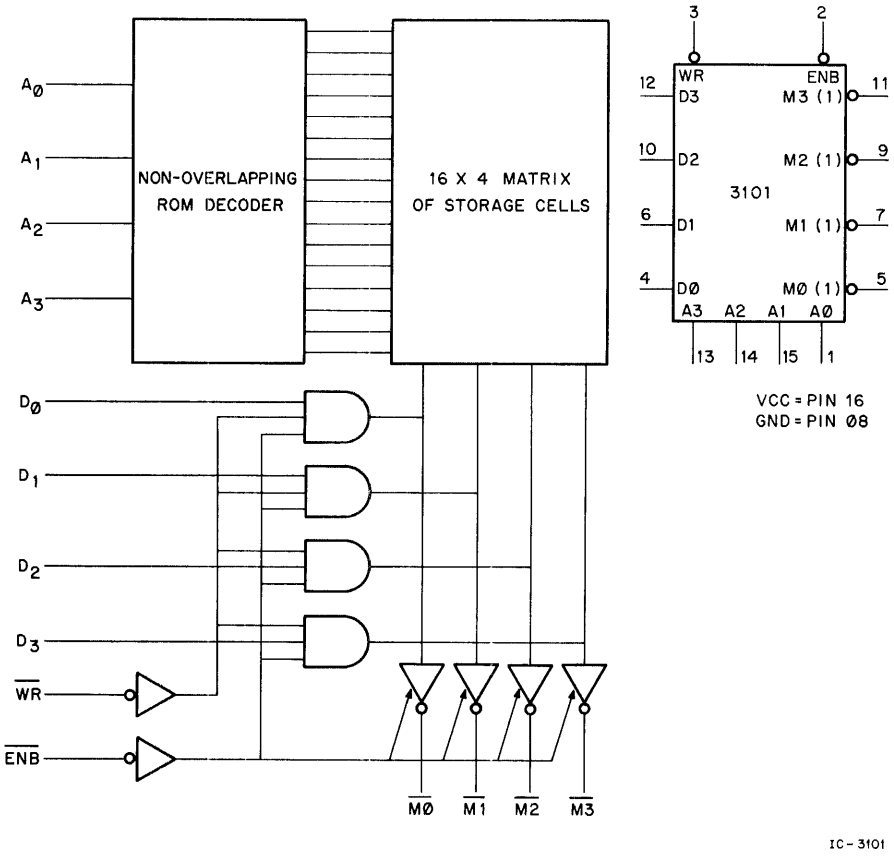
① V_{DD} = 2V
② V_{SS} = 2V
} t_t is defined as the transitions between these two points.

3. t_{DW} is referenced to point ① of the rising edge of chip enable or read/write, which ever occurs first.

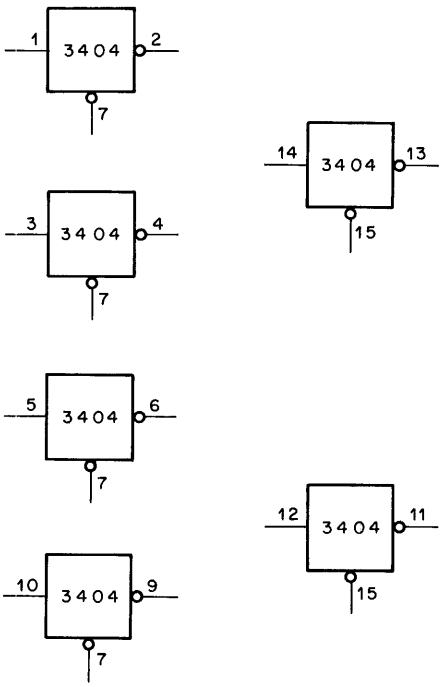
4. t_{DH} is referenced to point ② of the rising edge of chip enable or read/write, which ever occurs first.

IC-1103-1 B

3101 RANDOM ACCESS MEMORY



3404 LATCH (DUAL-IN-LINE)



+5V = PIN 16
GND = PIN 8

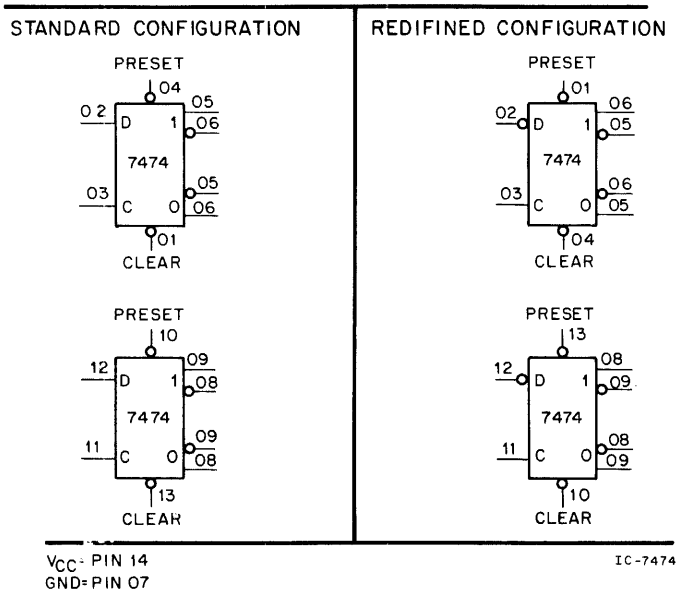
IC-3404

7474 DUAL FLIP-FLOP

TRUTH TABLE FOR
7474 STANDARD CONFIGURATION
(EACH FLIP-FLOP)

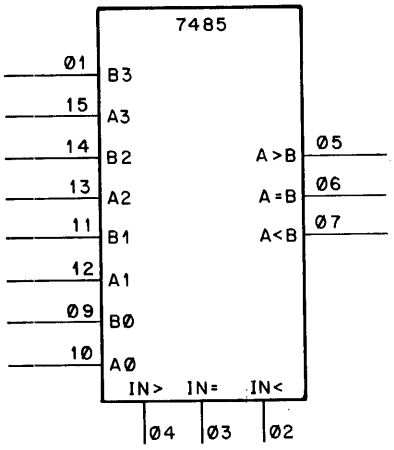
t_n			t_n+1	
Preset Pin 4(10)	Clear Pin 1(13)	D Input Pin 2(12)	1 Side Pin 5	0 Side Pin 6
High	High	Low	Low	High
High	High	High	High	Low
High	Low	X	Low	High
Low	High	X	High	Low
Low	Low	X	High	High

t_n = bit time before clock pulse.
t_n+1 = bit time after clock pulse.
X = irrelevant



7485 4-BIT COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B) about two 4-bit words (A,B) are made and externally available at three outputs.



VCC = PIN 16
OND = PIN Ø8

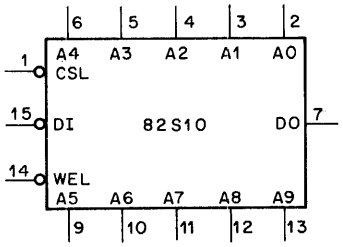
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

IC-7485

82S10 1024-BIT BIPOLAR RAM



V_{CC} = 16
GND = 8
CSL = $\overline{CS}$ = Chip select
WEL = $\overline{WE}$ = Write enable

TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN COLLECTOR	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE 0
L	L	H	H	WRITE 1
L	H	X	D_{OUT}	READ

H=HIGH VOLTAGE LEVEL
L=LOW VOLTAGE LEVEL
X=IRREVELANT

NOTES:
1. A chip select (CS) input provides for memory array expansion.

2. Data is written into the addressed location when WE is held low and the chip is selected.

3. Data is read from the addressed location when WE is held high and the chip is selected.

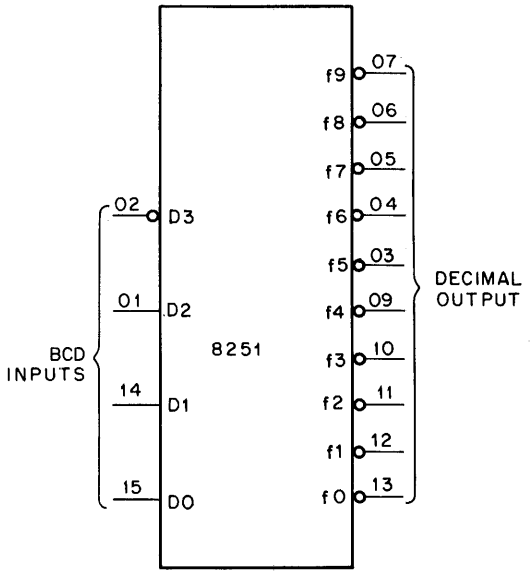
IC-82S10

8251 4 TO 10 DECODER

8751 TRUTH TABLE

INPUT				f OUTPUT									
D0	D1	D2	D3	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0

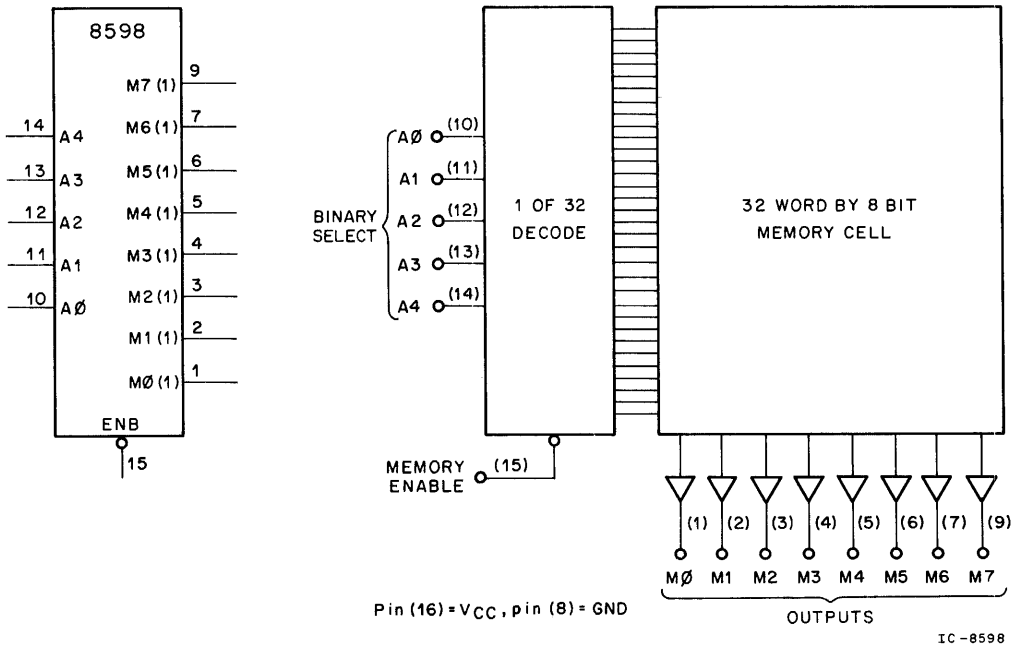
1 = High
0 = Low



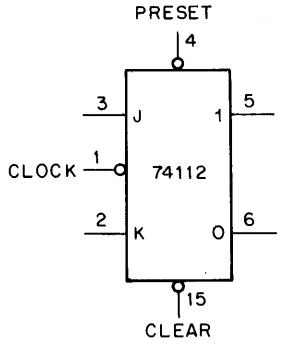
IC-8251

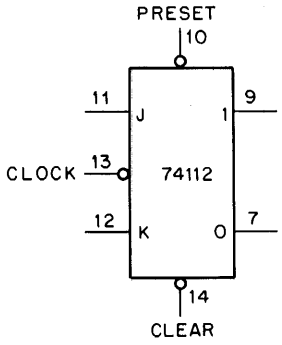
8598 READ-ONLY MEMORY

The 8598 is a 256-bit, read-only memory organized as 32 words of 8-bits each. Addressing is accomplished in straight 5-bit binary with full decoding. An overriding memory enable input is provided which, when taken high, will inhibit the 32 address gates and cause all 8 outputs to remain high.



74112 DUAL J-K FLIP-FLOP





74112 Truth Table

t_n		t_{n+1}
J	K	Pin 5 or 9
L	L	No change
L	H	L
H	L	H
H	H	Complement

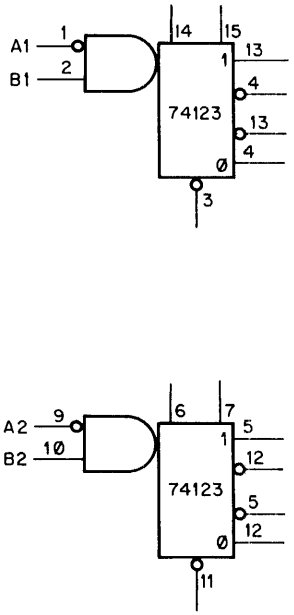
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

IC-74112

74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The 74123 Monostable Multivibrator provides d-c triggering from gated low-level active (A) and high-level active (B) inputs. Overriding direct clear inputs and complementary outputs are also provided.

By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time, independently of the external timing components.



IC-74123A

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	1	0
H	X	L	H
X	L	L	H
L	↑	⎍	⎴
↓	H	⎍	⎴

NOTE: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎴ = one low-level pulse, X = irrelevant (any input, including transitions).

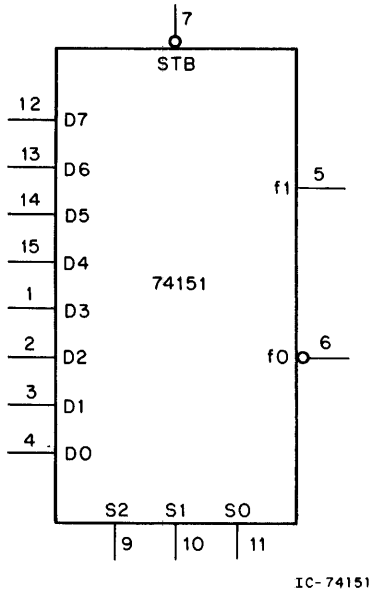
IC-74123B

74151 8 TO 1 MULTIPLEXER

74151 TRUTH TABLE

Inputs												Outputs	
S2	S1	S0	STB	D0	D1	D2	D3	D4	D5	D6	D7	f1	f0
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.

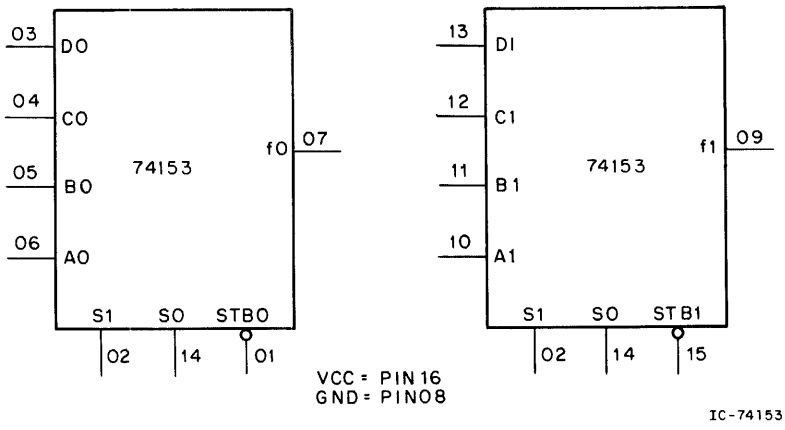


IC-74151

74153 DUAL 4 TO 1 MULTIPLEXER

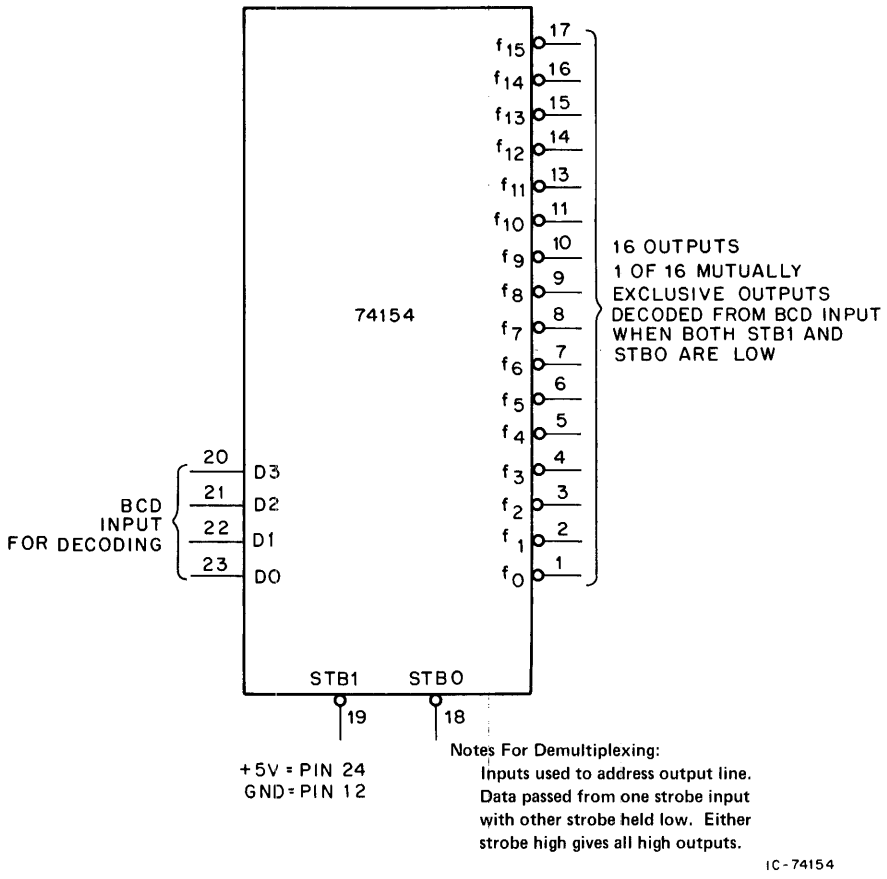
ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
S1	S0	A	B	C	D	STB	f
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S0 and S1 are common to both sections.
H = high level, L = low level, X = irrelevant.

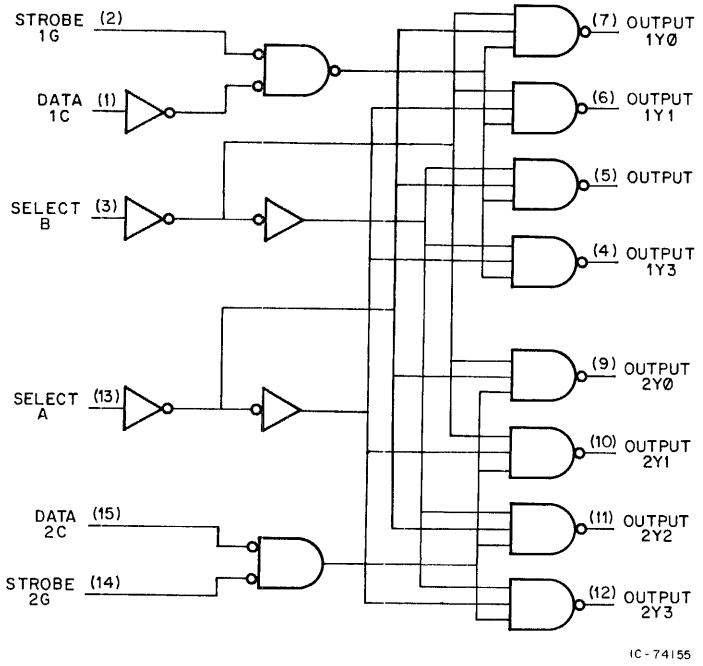


74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



74155 3-LINE TO 8-LINE DECODER



FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

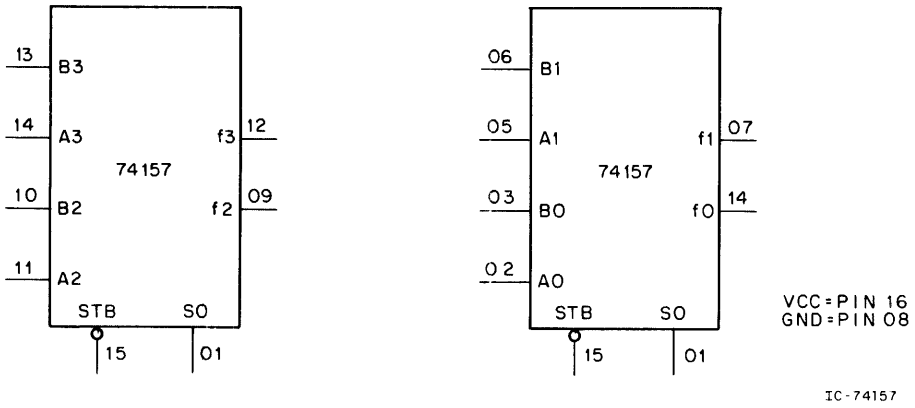
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

74157 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

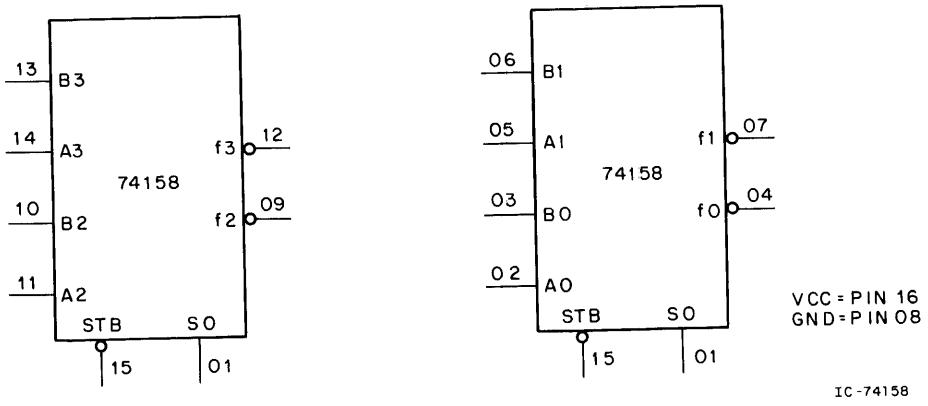
H = high level, L = low level, X = irrelevant.



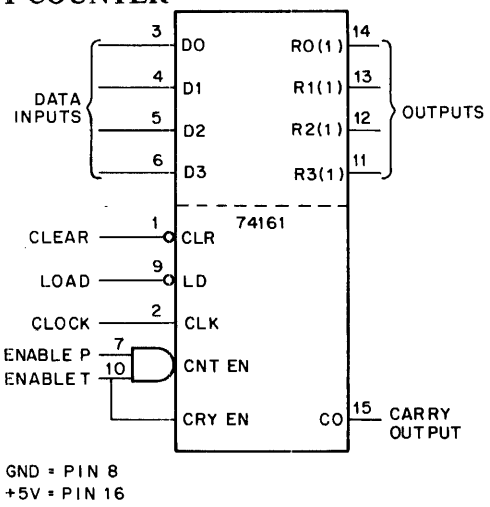
74158 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant.



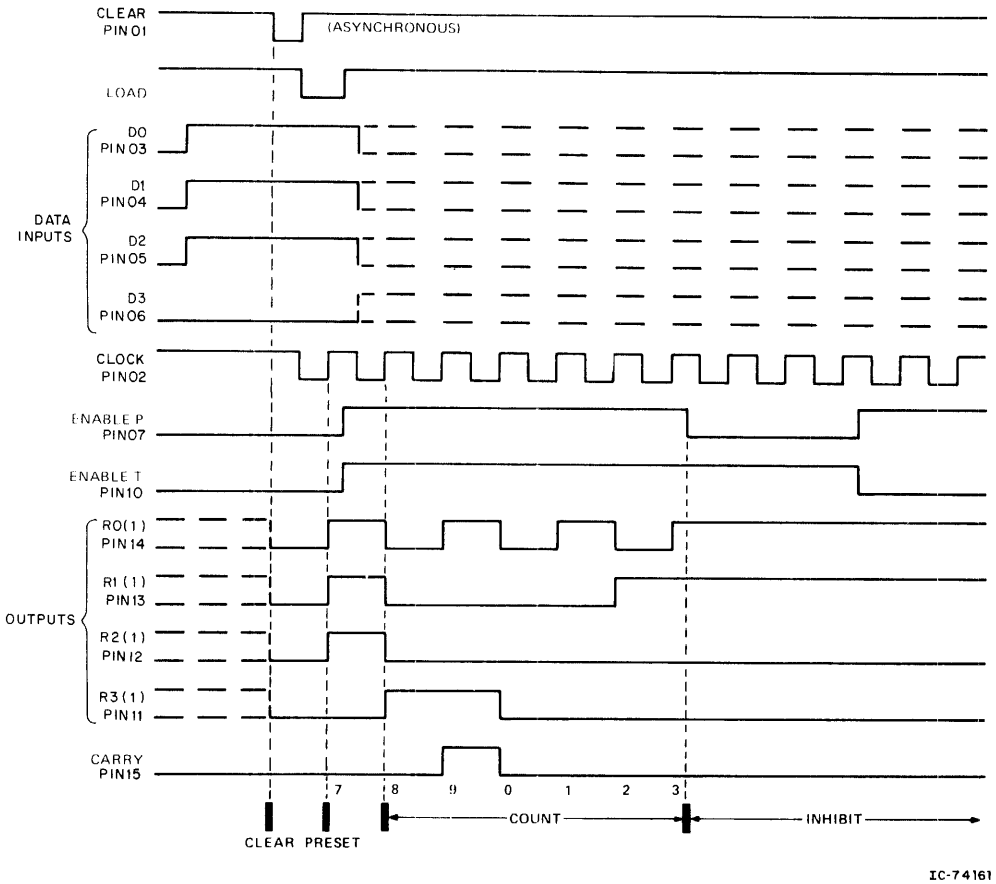
74161 SYNCHRONOUS 4-BIT COUNTER



typical clear, preset, count, and inhibit sequences for 74161

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit

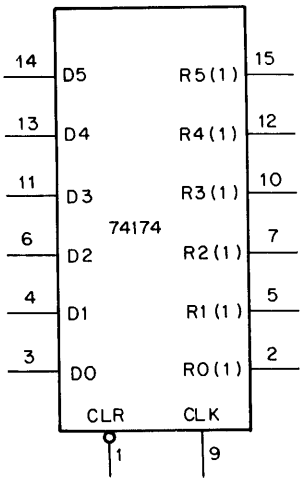


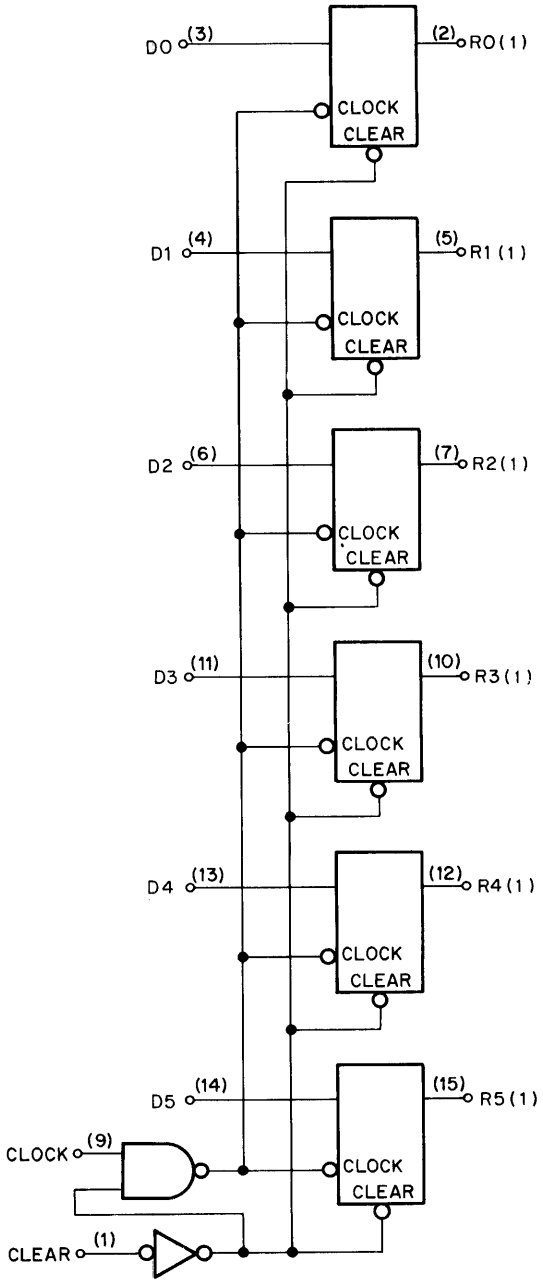
74174 HEX D FLIP-FLOP REGISTER

TRUTH TABLE

INPUT t_n	OUTPUT t_{n+1}
D	R(1)
H	H
L	L

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.





Pin (16) = V_{CC}, Pin (8) = GND

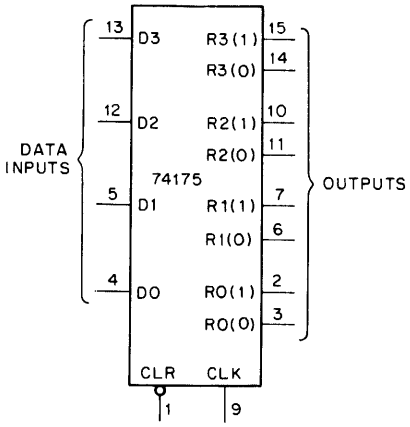
IC-74174

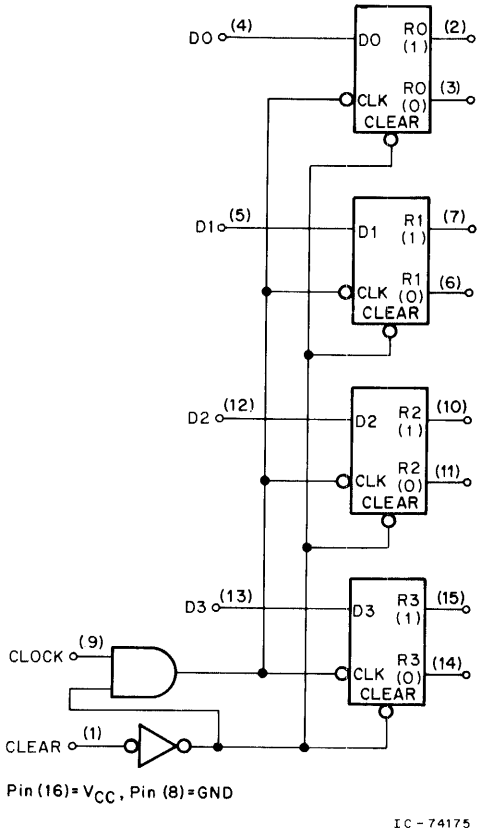
74175 QUAD STORAGE REGISTER

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}
D	R(1) R(0)
H	H L
L	L H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.





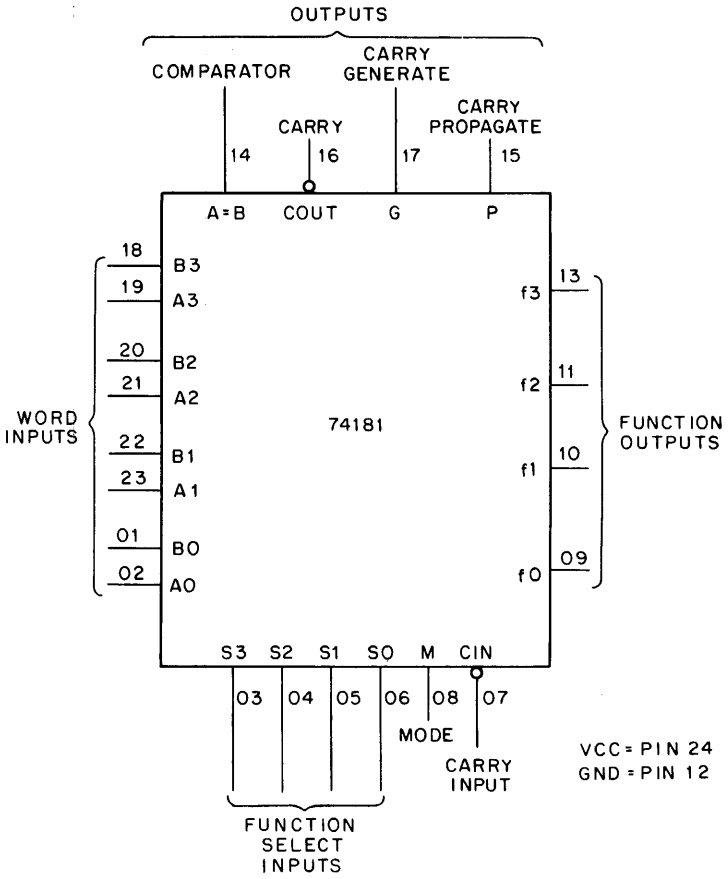
74181 4-BIT ARITHMETIC LOGIC UNIT, ACTIVE HIGH DATA

The 74181 performs up to 16 arithmetic and 16 logic functions. Arithmetic operations are selected by four function-select lines (S0, S1, S2, and S3) with a low-level voltage at the mode control input (M), and a low-level carry input. Logical operations are selected by the same four function-select lines except that the mode control input (M) must be high to disable the carry input.

74181
TABLE OF LOGIC FUNCTIONS

Function Select				Output Function	
S3	S2	S1	S0	Negative Logic	Positive Logic
L	L	L	L	$f = \overline{A}$	$f = \overline{A}$
L	L	L	H	$f = \overline{AB}$	$f = \overline{A + B}$
L	L	H	L	$f = \overline{A} + B$	$f = \overline{A}B$
L	L	H	H	f = Logical 1	f = Logical 0
L	H	L	L	$f = \overline{A + B}$	$f = \overline{AB}$
L	H	L	H	$f = \overline{B}$	$f = \overline{B}$
L	H	H	L	$f = \overline{A \oplus B}$	$f = A \oplus B$
L	H	H	H	$f = A + \overline{B}$	$f = A\overline{B}$
H	L	L	L	$f = \overline{A}B$	$f = \overline{A + B}$
H	L	L	H	$f = A \oplus B$	$f = \overline{A \oplus B}$
H	L	H	L	f = B	f = B
H	L	H	H	f = A + B	f = AB
H	H	L	L	f = Logical 0	f = Logical 1
H	H	L	H	$f = A\overline{B}$	$f = A + \overline{B}$
H	H	H	L	f = AB	f = A + B
H	H	H	H	f = A	f = A

With mode control (M) high: C_{in} irrelevant
For positive logic: logical 1 = high voltage
logical 0 = low voltage
For negative logic: logical 1 = low voltage
logical 0 = high voltage



IC-74181

74181
TABLE OF ARITHMETIC OPERATIONS

Function Select				Output Function	
S3	S2	S1	S0	Low Levels Active	High Levels Active
L	L	L	L	f = A minus 1	f = A
L	L	L	H	f = AB minus 1	f = A + B
L	L	H	L	$f = A\overline{B}$ minus 1	$f = A + \overline{B}$
L	L	H	H	f = minus 1 (2's complement)	f = minus 1 (2's complement)
L	H	L	L	f = A plus $[A + \overline{B}]$	$f = A$ plus $A\overline{B}$
L	H	L	H	f = AB plus $[A + \overline{B}]$	f = $[A + B]$ plus $A\overline{B}$
L	H	H	L	f = A minus B minus 1	f = A minus B minus 1
L	H	H	H	$f = A + \overline{B}$	$f = A\overline{B}$ minus 1
H	L	L	L	f = A plus [A + B]	f = A plus AB
H	L	L	H	f = A plus B	f = A plus B
H	L	H	L	$f = A\overline{B}$ plus [A + B]	f = $[A + \overline{B}]$ plus AB
H	L	H	H	f = A + B	f = AB minus 1
H	H	L	L	f = A plus A†	f = A plus A†
H	H	L	H	$f = A\overline{B}$ plus A	f = [A + B] plus A
H	H	H	L	$f = A\overline{B}$ plus A	f = $[A + \overline{B}]$ plus A
H	H	H	H	f = A	f = A minus 1

With mode control (M) and C_{in} low
† Each bit is shifted to the next more significant position.

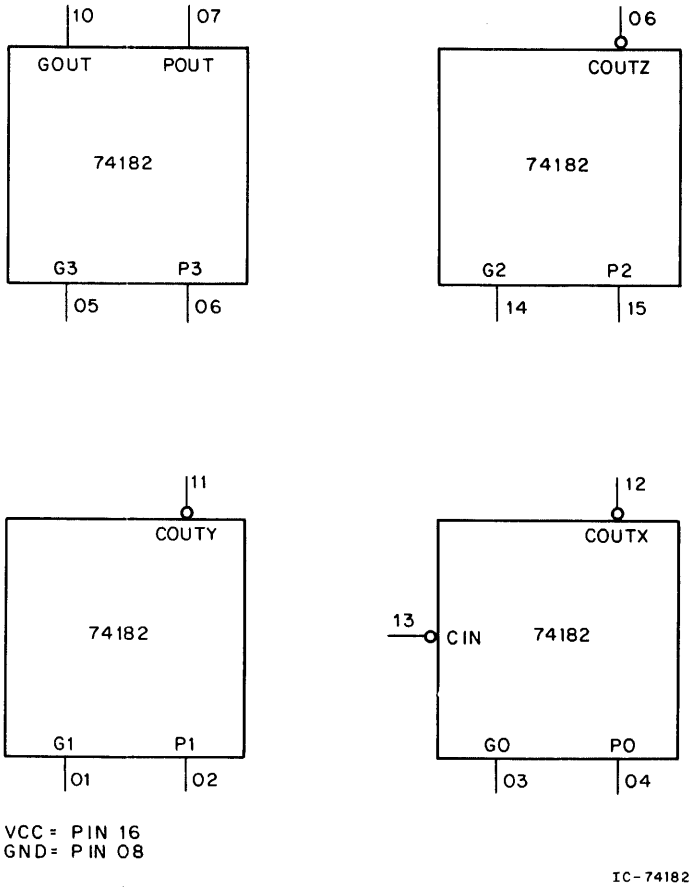
74182 LOOK-AHEAD CARRY GENERATOR

The 74182 Look-Ahead Carry Generator, when used with the 74181 ALU, provides carry look-ahead capability for up to n-bit words. Each 74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

Carry inputs and outputs of the 74181 ALU are in their true form, and the carry propagate (POUT) and carry generate (GOUT) are in negated form.

PIN DESIGNATIONS

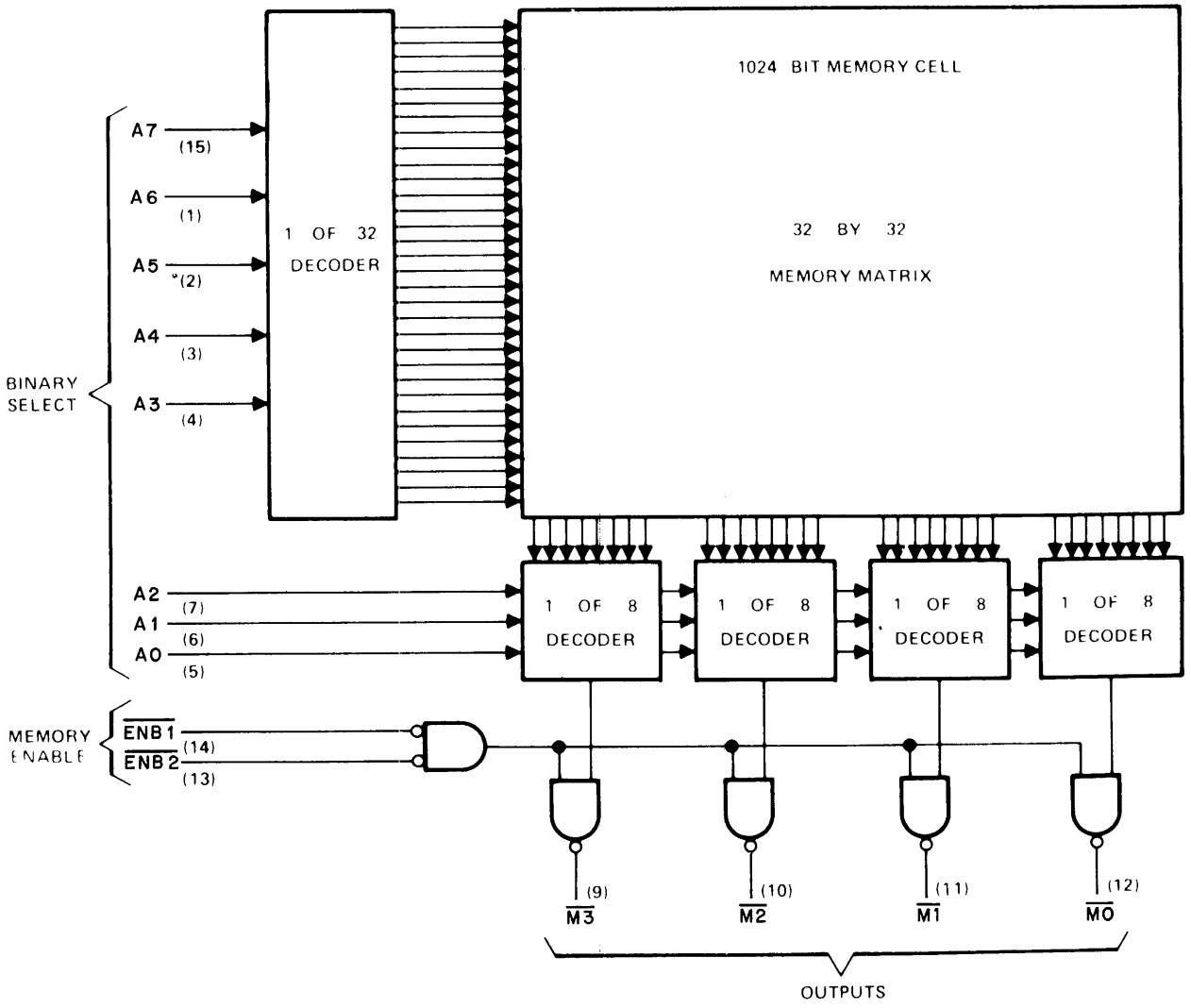
Designation	Pin No.	Function
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
CIN	13	CARRY INPUT
COUTX, COUTY, COUTZ	12, 11, 9	CARRY OUTPUTS
GOUT	10	ACTIVE-LOW CARRY GENERATE OUTPUT
POUT	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

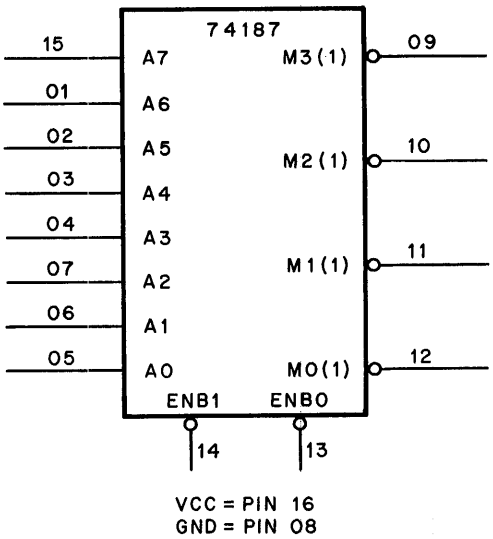


VCC = PIN 16
GND = PIN 08

IC-74182

74187 1024-BIT READ-ONLY MEMORY





VCC = PIN 16
GND = PIN 08

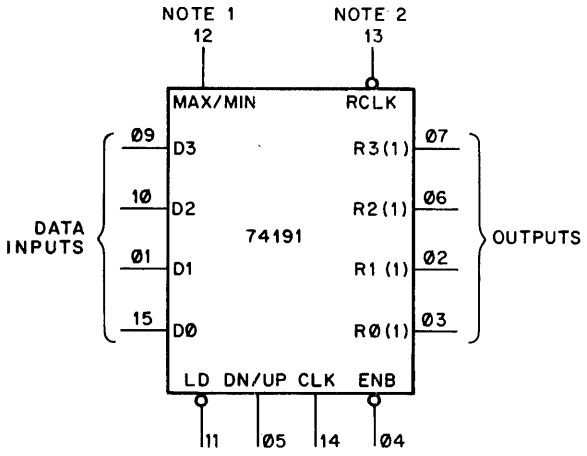
IC-74187

74191 4 BIT UP/DOWN COUNTER

The 74191 is a 4-bit binary counter that counts in BCD or binary and can operate as an up or down counter. The counter can be preset by the load control and uses a ripple clock output for cascading.

DOWN/UP	ENABLE	LOAD	MODE
X	X	L	Parallel Load
X	H	H	No Change
L	L	H	Count Up
H	L	H	Count Down

H = high level L = low level X = irrelevant



VCC = PIN 16
GND = PIN 08

NOTES:

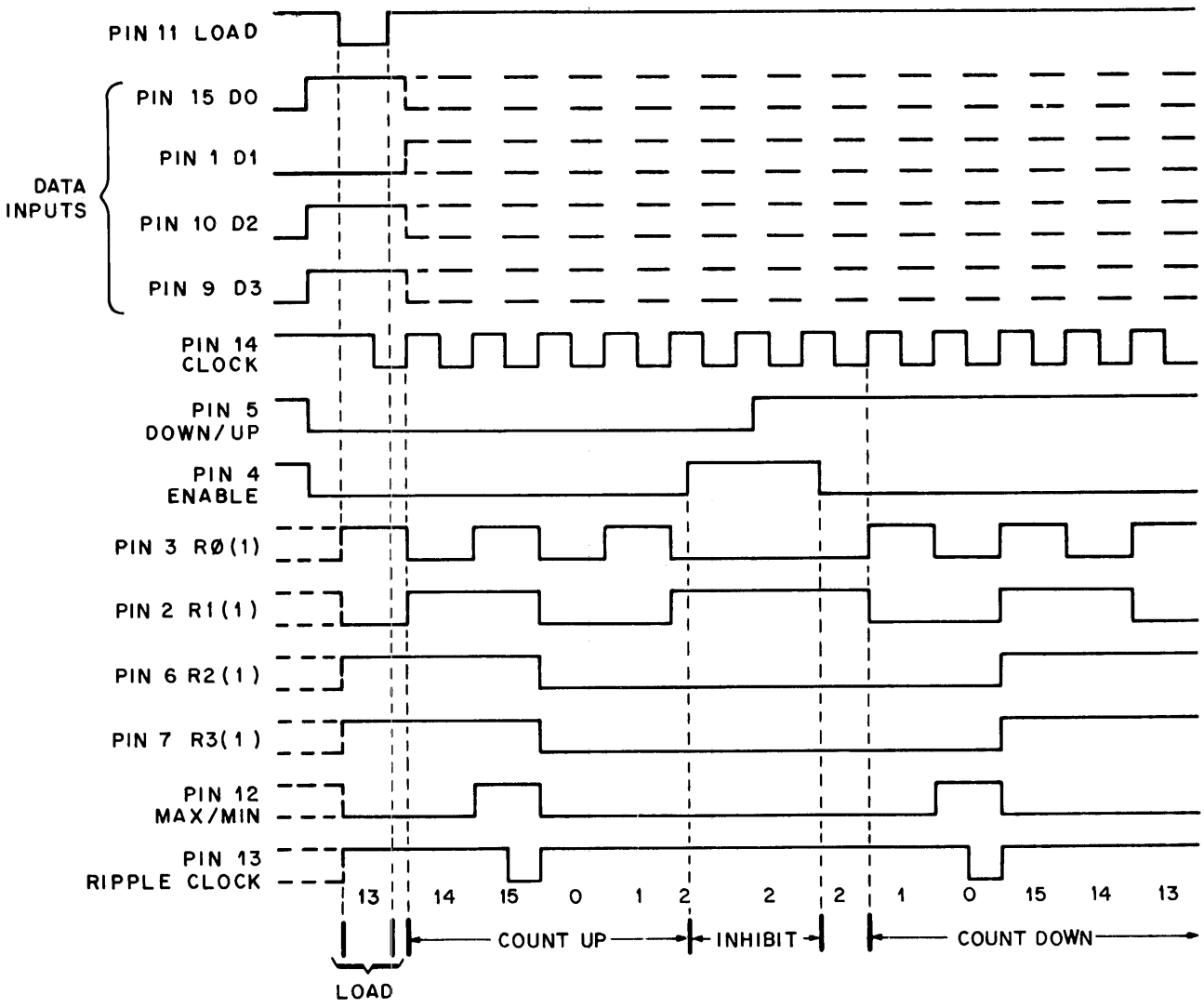
1. MAX/MIN produces a high level output pulse when the counter overflows or underflows.
2. Ripple clock produces a low level output pulse when an overflow or underflow condition exists.

IC-74191A

typical load, count, and inhibit sequence:

Illustrated below is the following sequence.

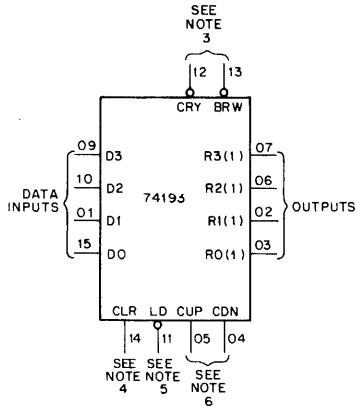
1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



IC-74191B

74193 4-BIT UP/DOWN COUNTER

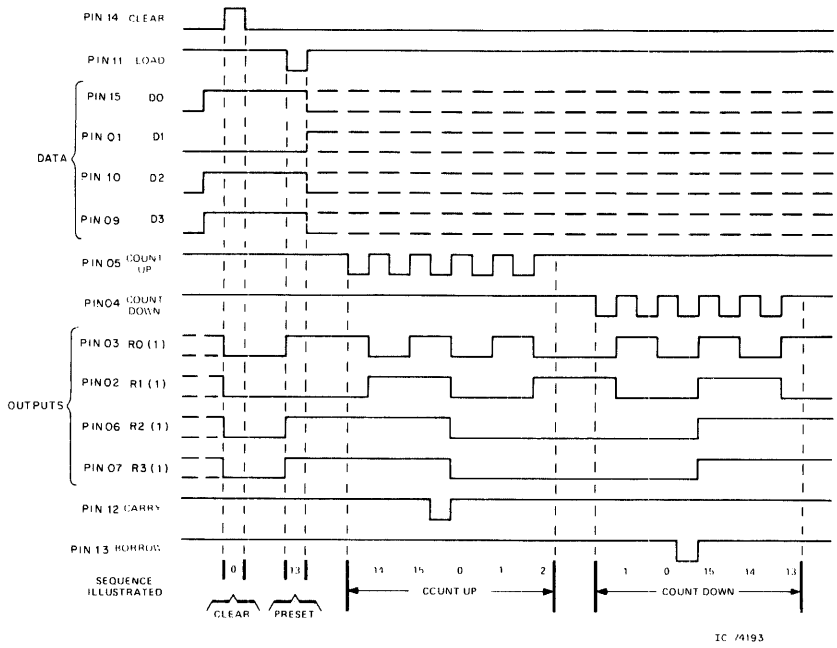
The 74193 Binary Counter has a individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.



NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count down input must be high; when counting down, count-up input must be high.
3. Produce pulses equal to width of count pulses during: Underflow (BORROW)
   Overflow (CARRY)
4. CLR input high forces all outputs low. CLR overrides load, data and DN/UP inputs.
5. Preset to any state by applying input data with load input low. Output changes to agree with inputs independent of count pulses.
6. Select DN or UP clock while other is held high.

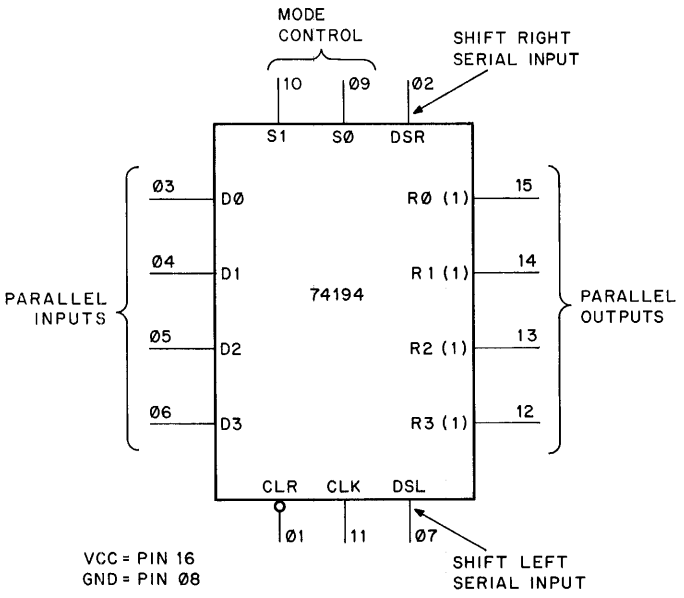
typical clear, load, and count sequences for 74193

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



IC /4193

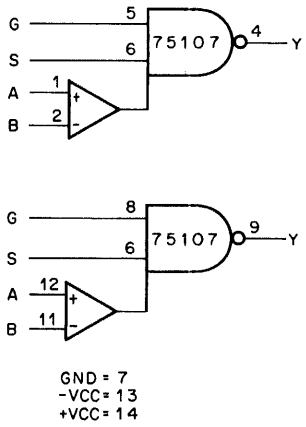
74194 PARALLEL-ACCESS SHIFT REGISTER WITH MODE CONTROL



	MODE CONTROL	
	S1	S0
PARALLEL LOAD	H	H
SHIFT RIGHT (IN THE DIRECTION R0 TOWARD R3)	L	H
SHIFT LEFT (IN THE DIRECTION R3 TOWARD R0)	H	L
INHIBIT CLOCK (DO NOTHING)	L	L

IC-74194

75107 SENSE AMPLIFIER (DUAL-IN-LINE)



TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

IC-75107

APPENDIX B
PERIPHERAL PREVENTIVE MAINTENANCE SCHEDULE

Peripheral	Man-Hours (approximate)
Monthly	
LA30 DECwriter	0.25
TU56 DECtape Transport	
weekly	0.25
monthly	1.0
RK05 Disk Drive	0.5
TU10 DECmagtape Transport	
weekly	0.5
monthly	1.25
CR11-A Card Reader (300 cpm M200)	0.25
CD11 Card Readers (M1000, M1200)	0.25
Quarterly	
LA30 DECwriter	0.75
RK05 Disk Drive	1.0
RP11-C/RP03 Disk Pack System	0.75
PC05 Paper Tape Reader/Punch	0.75
TU10 DECmagtape Transport	1.75
LP11-F, H Line Printer	1.0
LP11-J, K Line Printer	1.0
LP11-M, Q Line Printer	2.0

Quarterly (Cont)	
LP11-R, S Line Printer	2.0
CR11-A Card Reader (M200)	0.75
CD11 Card Readers (M1000, M1200)	0.5
LPS11 Laboratory Peripheral System	3.0
*KB11-A Central Processor	3.0
*MS11 Semiconductor Memory System	0.5
*KT11-C Memory Management Unit	0.5
*FP11-B Floating Point Processor	0.75
*MM11-S Core Memory	0.5
*Run all diagnostics on system	

Semi-Annual	
RK05 Disk Drive	1.0
LP11-M, Q Line Printer	3.5
LP11-R, S Line Printer	3.5
LV11 Printer/Plotter	3.0
RK03 Disk Drive	1.0
RP11-C/RP03 Disk Pack System	2.75

NOTES:

1. For any devices not listed, run their associated diagnostics programs quarterly.

2. Analog devices are not included in this list because of the numerous options and variations that are available.

3. All man-hour requirements are approximations.

PDP-11/45 Timing Margins Preventive Maintenance Chart

Margin Clock	Test Program														
		+ns	−ns	+ns	−ns	+ns	−ns	+ns	−ns	+ns	−ns	+ns	−ns	+ns	−ns
KB11-A, D	DCKBO States Test														
	DZQGA General Test Program														
	DCKTG If KT11-C is implemented														
	DZFPO If FP11-B is implemented														
	DIGB Use MS11 if implemented														
	DEFPA If FP11-C is implemented														
	DEFPB If FP11-C is implemented														
FP11-B	DZFPO FP Exerciser														
	DZFPP General Test Program with FP Overlay														

Note: Refer to Paragraph 6.2.1 (Clock Selection) for timing adjustment procedures.

APPENDIX C
SUMMARY OF EQUIPMENT SPECIFICATIONS

This table provides mechanical, environmental, and programming information for PDP-11 optional equipment. The equipment is arranged in alphanumeric order by model number.

NOTES

1. Mounting Codes

   CAB = Cabinet mounted. If a cabinet is included with the option, it is indicated by an X in the "Cab Incl" column.

   FS = Free standing unit. Height × Width × Depth dimensions are shown in inches.

   TT = Table top unit.

   PAN = Panel mounted. Front panel height is shown in inches. An included cabinet is indicated when applicable.

   SU = System Unit. SU mounting assembly is included with the option.

   SPC = Small Peripheral Controller. Option is a module that mounts in a quad module, SPC slot.

   MOD = Module. Height is single, double, or quad.

   ( ) = Option mounts in the same space as the equipment shown within the parentheses.

   Some options include 2 separate physical parts and are indicated by use of a plus (+) sign.

2. Cabinet and peripheral equipment (such as magnetic tape) are included in the specifications.

3. Relative humidity specifications mean without condensation.

4. Equipment that can supply current is indicated by parentheses ( ) around the number of amps in the POWER section. *MEMORY POWER:* MF11- and MM11- require the same amount of power. In this table, MF11- power figures show the power required when the memory is active, while MM11- figures reflect that required by an inactive unit.

5. Non-Processor Request devices are indicated by an X in the "NPR" column.

6. 7008855 in 11/45, 11/50, 11/55 CPU; 7008909 in H960-D and 11/40.

7. 7009174. If first MF11-L in 11⁴0, use 7009103.

8. 7009560. If first MF11-L in 11/40, use 7009565.

9. H960-C, D only (not CPU Cabinet): one 7009568 per backplane (9 pin conversion) and one 7009569 for two backplanes (regulator harness).

10. 7009162 in 11/45, 11/50, 11/55 CPU; 7009099 in H960-D and 11/40.

CONVERSION FACTORS

(inches)	× 2.54	=	(cm)
(lbs)	× 0.454	=	(kg)
(Watts)	× 3.41	=	(Btu/hr)
[(°C)×9/5]+32		=	(°F)

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H X W X D (inches)	Cab Incl	Weight (lbs)	Power Harness Early	Power Harness New	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V	Cur needed/(supplied) 115 Vac / Other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
AA11-D	D/A Subsystem	SU				Note 6	7009562	10–50	20–95	3	0.5	60	776 756	140,144	4,5		1	AA11-D
AD01-D	A/D Subsystem	PAN	5¼					0–55	10–95		0.5	60	776 770	130	4–7		1	AD01-D
AFC11	A/D Subsystem	CAB						10–55	10–95		15	1700	772 570	134	4		1	AFC11
BA11-ES	Mounting Box	PAN	10½		100													BA11-ES
BA614	D/A Converter	(AA11-D)																BA614
BB11	Blank Mntg Panel	SU																BB11
BB11-A	Blank Mounting Panel (non-slotted blocks)	SU																BB11-A
BC11A	UNIBUS Cable									0.3								BC11A
BM792-Y	Bootstrap Loader	SPC															1	BM792-Y
CB11	Telephone Switching Interface	Cab		X	300			10–50	10–90		5.6	650	764 000	float	4–7		1,2	CB11
CD11-A	Card Reader	SU + TT	14 X 24 X 18		85	Note 6	7009562	10–50	10–90	2.5	4	450	772 460	230	4	X	1	CD11-A
CD11-E	Card Reader	SU + TT	38 X 24 X 38		200	Note 6	7009562	10–50	10–90	2.5	6	700	772 460	230	4	X	1	CD11-E
CM11-F	Card Reader	SPC + TT	11 X 19 X 14		60			10–50	10–90	1.5	4	400	777 160	230	6		1	CM11-F
CR11	Card Reader	SPC + TT	11 X 19 X 14		60			10–50	10–90	1.5	4	400	777 160	230	6		1	CR11
DA11-B	UNIBUS Link	SU				Note 6	7009562			4			772 410	124	5	X	1	DA11-B
DA11-F	UNIBUS Window	SU				7009099	7009563			5				float	7	X	1	DA11-F
DB11	Bus Repeater	SU				Note 6	7009562	5–50	10–95	3.2							1 + 1	DB11
DC11-A	Asynch Line Inter	SU				Note 6	7009562	10–50	20–90		see Product Bull		774 000	float	5		1	DC11-A
DD11-A	Periph Mntg Panel	SU				Note 6	7009562											DD11-A
DD11-B	Periph Mntg Panel	SU				Note 10	7009563											DD11-B
DD11-D	Periph Mntg Panel	2 SU																DD11-D
DECkit 01-A	Remote Analog Data Concentrator: 8 Channels, Serial	PAN	5¼ X 19 X 13		15			0–50	10–95		1.5 @ 115 Vac 0.75 @ 230 Vac	175						DECkit 01-A
DECkit 11-F	I/O Interface: 3 Words In/4 Words Out	SU				Note 6		0–70	10–95	1.84			User	User	7		4	DECkit 11-F
DECkit 11-H	I/O Interface: 4 Words In/4 Words Out	SU				Note 6		0–70	10–95	3.91			User	User	5–6		4	DECkit 11-H
DECkit 11-K	I/O Interface: 8 Words In	SU				Note 6		0–70	10–95	1.97			User				2	DECkit 11-K
DECkit 11-M	I/O Interface: Instrumentation Interface	SU				Note 6		0–70	10–95	1.75			User	User	4		2	DECkit 11-M
DF01-A	Acoustic Coupler	TT	6 X 7 X 12		6			0–60			0.3							DF01-A
DF11	Line Sig Cond	DF slot									see Product Bull.							DF11
DH11	Asynch Line MX	2 SU				7009466	7009561	5–45	10–95	8.4	0.24 A @ -15 V		float	float	5	X	2	DH11
DJ11	Asynch Line MX	SU				7009099	7009563			5	see Product Bull.		float	float	5		1	DJ11
DL11-A	Terminal Control	SPC								1.8	0.15 A @ -15 V		777 560	060,064	4		1	DL11-A
DL11 (others)	Asynch Line Inter	SPC								1.8	0.15 A @ -15 V		776 500	float	4		1	DL11 (others)
DL11-W	Asynchronous Interface and Line Clock	SPC	Quad Ht							2	0.05 A @ +15 V 0.15 A @ -15 V	10	Switch Selectable (SS)	A. Int.-SS Line CLK-104	A. Int.-4 Line CLK-6		1	DL11-W
DM11-BB	Modem Ctr. MUX	(DH11)								2.8			775 000	float			1	DM11-BB
DMC-11	Microprocessor and Line Unit	2 SPC	2 Hex Ht							4.5					5	X	1	DMC-11
DN11	Auto Calling Unit	SU				Note 6	7009562	0–40	20–90	3	0.10 A @ ± 15 V		775 200	float	4		1	DN11
DP11	Synch Line Inter	SU				Note 6	7009562	0–40	20–90	2.5	0.10 A @ ± 15 V		774 400	float	5		1	DP11
DQ11	DMA Sync Line Interface	SU				7009099	7009563	10–50	10–90	5.7	0.04 A @ +15 V 0.07 A @ -15 V		float	float	5	X	1	DQ11
DR11-B	DMA Interface	SU				Note 6	7009562	10–50	20–90	3.3			772 410	124	5	X	1	DR11-B
DR11-C	General Interface	SPC						10–50	20–90	1.5			767 770	float	5		1	DR11-C
DT03-F	UNIBUS Switch	PAN	5¼								2			user	7		1 + 1	DT03-F
DX11	IBM Chan. Interface	CAB		X	180			10–55	10–90		2.5	300	776 200	float	4–7	X	1	DX11-B
GT40	Graphics Terminal	TT	18 X 20 X 24		150			15–35	20–80		15	1500	float	float			1	GT40

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER				PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Power Harness Early	Power Harness New	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	Cur needed/(supplied) 115 Vac / Other (amps)		Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
H312-A H720-E H722 H742	Null Modem Power Supply Transformer Power Supply	(BA11) (PC11-A) (H960-D)			30			0–50	20–95	(22)	6 8	(10A) @ -15 V 1.5 A @ 230 Vac (1 A) @ +15 V	700						H312-A H720 H722 H742
H7420 H744 H745 H746	Power Supply +5 V Regulator -15 V Regulator MOS Regulator	(H960-D) (H7420 or H742) (H7420 or H742) (H7420 or H7420								(25) (25)		(10 A) @ -15 V (1.6 A) @ 23.2 V (3.3 A) @ 19.7 V (1.6 A) @ -5 V							H7420 H744 H745 H746
H754 H933-C	+20, -5 V Regulator Mounting Panel (H803 blocks)	(H742) SU										(8 A) @ +20 V (1 A) @ -5 V							H754 H933-C
H933-D H960-C H960-D	Mounting Panel (H808 blocks) Cabinet Cab (1 drawer)	SU FS FS	72 X 21 X 30 72 X 21 X 30	X X	120 300	7008754	7009566			(75)	8	(20 A) @ -15 V	900						H933-D H960-C H960-D
H960-E H961-A KE11-A KG11-A	Cab (2 drawers) Cab w/o side pan Ext. Arith. Elem. Comm Arith Unit	FS FS SU SPC	72 X 21 X 30 72 X 21 X 30	X X	470 120	7008754 Note 6	7009566 7009562			(150) 4 1.5	16	(40 A) @ -15 V	1800	 777 300 770 700				1 1	H960-E H961-A KE11-A KG11-A
KW11-L KW11-P LA30 LC11-A	Line Clock Programmable Clock DECwriter LA30 Control	MOD SPC FS SPC	single ht 31 X 21 X 24		110			15–35	20–80	0.8 1 1.5	3		300	777 546 772 540 777 560	100 104 060,064	6 6 4		1 1 1	KW11-L KW11-P LA30 LC11-A
LP11-F LP11-J LP11-R LPS11	Printer (80 col) Printer (132 col) Ptr (heavy duty) Lab Periph System	SPC + FS SPC + FS SPC + FS PAN	46 X 24 X 22 46 X 48 X 25 48 X 49 X 36 5¼		200 575 800 80			10–43 10–43 10–43 5–43	15–80 15–80 15–80 20–80	1.5 1.5 1.5	2 4 17 3		250 500 2000 300	777 514 777 514 777 514 float	200 200 200 float	4 4 4 4–6	 opt	1 1 1 2	LP11-F LP11-J LP11-R LPS11-S
LS11 LT33 LV11 M105	Line Printer Teletype Electrostatic Ptr Adrs Select Module	SPC + TT FS SPC + FS MOD	12 X 28 X 20 34 X 22 X 19 38 X 19 X 18 single ht		155 60 160			5–38 15–35 10–43	5–90 20–80 20–80	1.5 1.5 0.34	3 2 5		300 200 600	777 514 777 514	200 200	4 4		1 1	LS11 LT33 LV11 M105
M783 M784 M785 M792	Bus Transmitter Bus Receiver Bus Transceiver Diode ROM	MOD MOD MOD SPC	single ht single ht single ht							0.2 0.2 0.3 0.23				 773 000				 1	M783 M784 M785 M792
M795 M796 M920 M930	Word Count Bus Control Bus Jumper Bus Terminator	MOD MOD MOD MOD	 double ht							 1.25									M795 M796 M920 M930
M1501 M1502 M1621	Bus Input Interface Bus Output Interface DVM Data Input Interface	MOD MOD MOD	single ht double ht quad ht					0–70 0–70 0–70	10–95 10–95 10–95	0.3 0.75 0.78									M1501 M1502 M1621
M1623 M1710 M1801	Instrument Remote Control Interface Unibus Interface Foundation 16-Bit Relay Output Interface	MOD MOD & SPC MOD	quad ht quad ht quad ht					0–70 0–70 0–70	10–95 10–95 10–95	1.6 0.79 1.46								opt	M1623 M1710 M1801

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Power Harness Early	Power Harness New	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	Cur needed/(supplied) 115 Vac / Other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
M7820	Interrupt Control	MOD	single ht															M7820
M7821	Interrupt Control	MOD	single ht															M7821
M9301(-YA), (-YB), (-YD)	Bootstrap Terminator	Unibus Slot	Double Ht							2							1	M9301(-YA), (-YB), (-YD)
ME11-L	Core Memory (8K)	PAN	5¼					0–50	10–90		5	125					1	ME11-L
MF11-L	Core Memory (8K)	2 SU				Note 7	Note 8	0–50	10–90	3.4	6 A @ -15 V	125					1	MF11-L
MF11-LP	Parity Memory (8K)	2 SU				Note 7	Note 8	0–50	10–90	4.9	6 A @ -15 V	125					2	MF11-LP
MF11-U	Core Memory (16K)	2 SU				Note 9	7009535	0–50	0–90	4.5	3.5 A @ 20 V 0.5 A @ -5 V	120					1	MF11-U
MF11-UP	Parity Memory (16K)	2 SU				Note 9	7009535	0–50	0–90	6	3.4 A @ 20 V 0.5 A @ -5 V	120					2	MF11-UP
MM11-L	Core Memory (8K)	(MF11-L)						0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-L
MM11-LP	Parity Memory (8K)	(MF11-LP)						0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-LP
MM11-U										4.5	0.5 A @ 20 V 0.5 A @ -5 V							MM11-U
MM11-UP	Parity Memory (16K)	(MF11-UP)						0–50	0–90	4.5	0.5 A @ 20V 0.5 A @ -5 V							MM11-UP
MR11-DB	Bootstrap	2 SPC								0.6							2	MR11-DB
MS11	Semiconductor Mem	(11/45)						0–50	10–80				772 100	114			1	MS11
PC11	Paper Tape	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	777 550	070,074	4		1	PC11
PDM70	Programmable Data Mover	TT	5¼ X 19 X 23	X	55			0–40	10–95		115 Vac 230 Vac	250 250						PDM70
PR11	Paper Tape (rdr)	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	777 550	070	4		1	PR11
RC11-A	Disk & Control	PAN	10½		115			17–50	20–80		2.2	250	777 440	210	5	X	1	RC11-A
RF11-A	Disk & Control	PAN + PAN	16 + 16	X	500			17–33	20–55		6.5	750	777 460	204	5	X	1	RF11-A
RK05	Disk Drive	PAN	10½		110			15–43	20–80		2	160						RK05
RK11-D	Disk & Control	SU + PAN	10½	X	250	7008992	7009562	15–43	20–80	7.5	2	200	777 400	220	5	X	1	RK11-D
RP03	Disk Drive	FS	40 X 30 X 24		415			15–33	10–80		6 A @ 230 Vac	1300						RP03
RP11-C	Disk & Control	CAB + FS		X	740			15–33	10–80		7 6 A @ 230 Vac	2100	776 710	254	5	X	1	RP11-C
RS11	Disk Drive	PAN	16		100			17–33	20–55		2	200						RS11
RS64	Disk	PAN	10½		65			17–50	20–80		2.2	250						RS64
RT01	Numeric Data Entry Terminal	TT	6.5 X 12.5 X 15	X	12			0–40	10–90		0.25 @ 115 Vac 0.12 @ 220 Vac	30						RT01
RT02	Alphanumeric Data Entry Terminal	TT	6.3 X 14.4 X 16	X	14			0–40	10–90		110 Vac 220 Vac	50 50						RT02
TA11	Cassette	SPC + PAN	5¼					10–40	20–80	1.5	1	120	777 500	260	6		1	TA11
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250			15–27	40–60		9	870	777 340	214	6	X	1	TC11-G
TM11	Magtape & Control	PAN + PAN	26 + 10½	X	500			15–27	40–60		9	1000	772 520	224	5	X	1	TM11
TU10	Magtape Transport	PAN	26	X	450			15–27	40–60		9	1000						TU10
TU56	DECtape Transport	PAN	10½		80			15–27	40–60		3	350						TU56
UDC11	I/O Subsystem	CAB						5–50	10–90		15	1700	771 774	234	4,6		2	UDC11
VR01	Display	PAN	10½		30			10–50	10–90		1	120						VR01
VR14	Display	PAN	10½		75			10–50	10–90		4	400						VR14
VT01	Display	TT	12 X 12 X 23		50			0–50	10–80		2.2	250						VT01
VT05	Alphanum Terminal	TT	12 X 19 X 30		55			10–43	8–90		2	130						VT05

Reader's Comments

PDP-11/45, 11/50, 11/55 System
Maintenaance Manual
EK-11045-MM-007

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

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Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

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Would you please indicate any factual errors you have found. _____

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