KDJ11–B CPU System Maintenance

Order Number EK–247AA–MG–001

digital equipment corporation
maynard, massachusetts

November 1988

Printed in U.S.A.

The READER'S COMMENTS form on the last page of this document requests the user's critical evaluation to assist in preparing future documentation.

ML–S983

FCC NOTICE: The equipment described in this manual generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such radio frequency interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his own expense may be required to take measures to correct the interference.

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Preface

This guide describes a base system, configuration, ROM-based diagnostics, and troubleshooting procedures for systems containing the KDJ11–BB, KDJ11–BC, and KDJ11–BF central processing unit (CPU).

Intended Audience

This document is intended only for DIGITAL Field Service personnel and qualified self-maintenance customers.

Organization

This guide has three chapters and three appendixes.

Chapter 1 provides an overview of the KDJ11–B CPU and three memory modules: the MSV11–P, the MSV11–Q, and the MSV11–J.

Chapter 2 contains system configuration guidelines and lists current, power, and bus loads for supported options.

Chapter 3 contains ROM-based diagnostic troubleshooting procedures for systems containing the KDJ11–B CPU.

Appendix A describes the differences between the three KDJ11–B ROM code versions: V6.0, V7.0, and V8.0.

Appendix B explains how to format RD- and RX-series disk drives in MicroPDP–11 systems.

Appendix C provides a list of related documentation.

Warnings, Cautions, and Notes

Warnings, cautions, and notes appear throughout this guide. They have the following meanings:

WARNING	Provides information to prevent personal injury.
CAUTION	Provides information to prevent damage to equipment or software.
NOTE	Provides general information about the current topic.

Chapter 1
KDJ11–B CPU Description

1.1 Introduction

This chapter describes the KDJ11–B CPU modules. There are three variants: KDJ11–BB, KDJ11–BC, and KDJ11–BF. Unless otherwise stated, the term KDJ11–B refers to all three variants.

This chapter also describes the following three memory modules: MSV11–PK/–PL, MSV11–QA/–QB/–QC, and MSV11–JD/–JE.

The KDJ11–B is designed for systems that use the extended LSI–11 bus, commonly called the Q22-bus. Depending on the system, the KDJ11–B CPU uses either the MSV11–P, MSV11–Q, or MSV11–J memory modules and a set of standard Q22-bus options.

1.2 KDJ11–B Overview

The KDJ11–B (M8190) is a quad-height processor module for the Q22-bus systems listed in Table 1–1.

Table 1–1: KDJ11–B Systems

CPU	System	CPU Description
KDJ11–BB KDJ11–BC	MicroPDP–11/73	Contains a 15-MHz clock and uses the Q22-bus to communicate with the MSV11–P or MSV11–Q memory modules.
KDJ11–BF	MicroPDP–11/83	Contains an 18-MHz clock and a floating point accelerator (FPA) chip. Uses the private memory interconnect (PMI) as a high-speed communication path to the MSV11–J memory module. The KDJ11–BF module is not installed in slot 1 of the system backplane. It is installed in slot 2, 3, or 4, immediately following the last MSV11–J memory module.

The enclosures and memory modules for the KDJ11–B systems are listed in Table 1–2.

Table 1–2: KDJ11–B System Enclosures and Memory

System	Enclosure	Memory
MicroPDP–11/73	BA23 (rack mount, pedestal, and tabletop) BA123	MSV11–P MSV11–Q
MicroPDP–11/83	BA23 (rack mount and pedestal) BA123 H9642–J cabinet containing two BA23s BA200-series	MSV11–J

The KDJ11–B CPU provides the following features:

- A PDP–11 instruction set, including extended instruction set (EIS) and floating point instruction set
- Four-level interrupt protocol
- Memory management
- An 8-Kbyte cache memory
- A 32-Kbyte boot and diagnostic facility with LED indicators
- Console serial line unit (SLU)

Figure 1–1 shows the KDJ11–B module with a dual in-line package (DIP) switchpack (E83), diagnostic LEDs, and connectors and jumpers.

To enable the baud rate select switch on the SLU display panel, set the switches in switchpack E83 to the Off position.

Table 1–3 lists the factory configuration for the switches and jumpers.

Figure 1–1: KDJ11–B Module Layout (M8190)

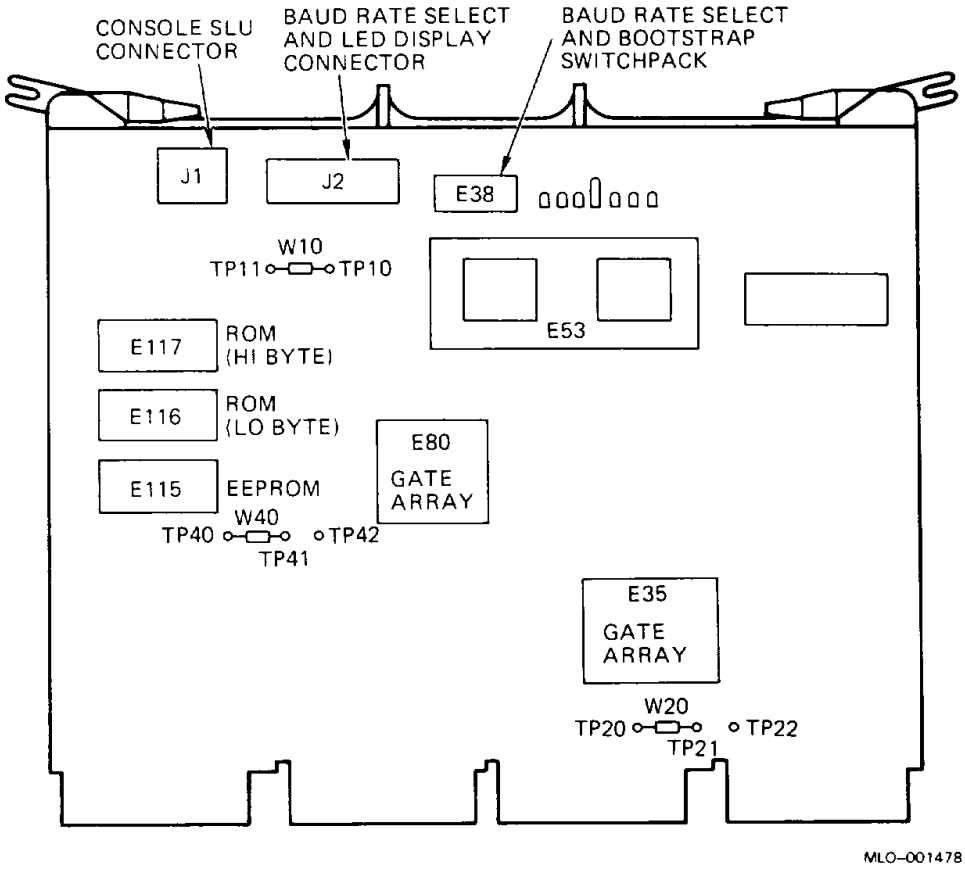


Table 1–3: KDJ11–B Switch and Jumper Factory Configuration

Type	Designation	Position
Switchpack	E83	All Off
Jumpers[1]	W10	Installed between TP10 and TP11
	W20	Installed between TP20 and TP21
	W40	Installed between TP40 and TP41

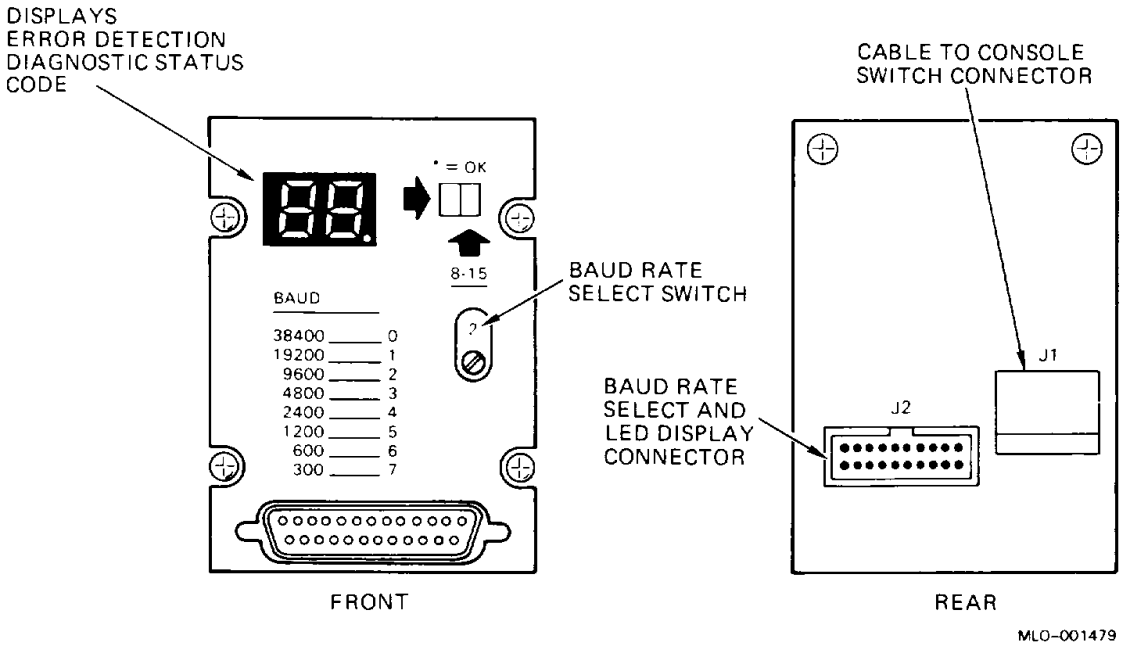
[1]Do not remove. For manufacturing test purposes only.

Seven LEDs on the KDJ11–B module provide status information. A green LED indicates the status of +5 Vdc and +12 Vdc. Six red LEDs show error detection and diagnostic status codes. These codes also appear in octal format on the SLU panel.

1.3 Baud Rate Select Switch

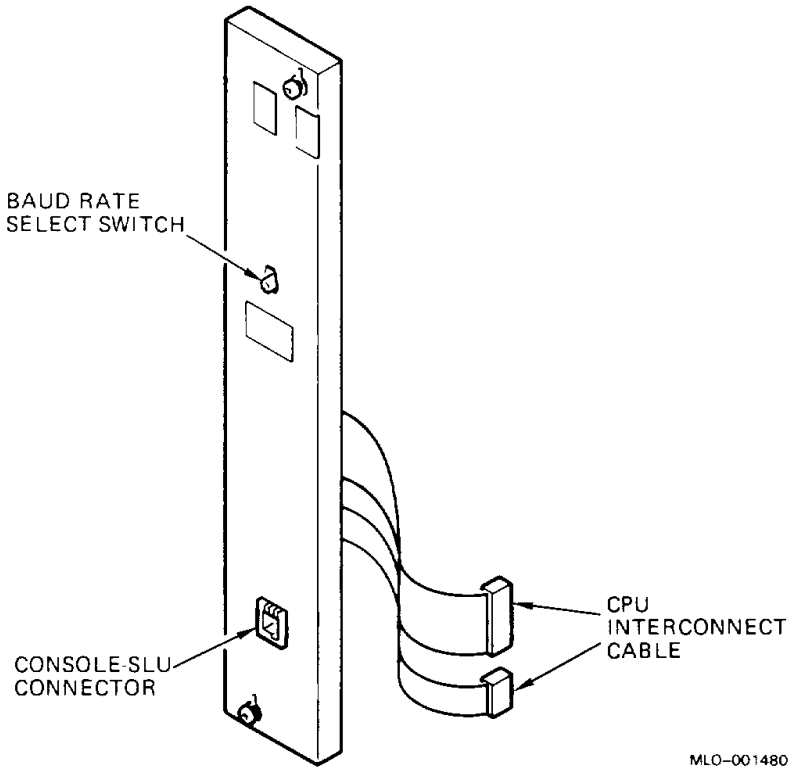
In BA23 and BA123 enclosures, the baud rate select switch is located on the SLU display panel, as shown in Figure 1–2. The cabinet kit for the KDJ11–B CPU contains the SLU panel and two cables that connect the SLU panel to the CPU. The SLU panel mounts onto the I/O panel of the enclosure.

Figure 1–2: SLU Display Panel, BA123 Enclosure



In BA200-series enclosures, the KDJ11–BF CPU is covered by a special bulkhead I/O panel (H3601–SA), which contains a baud rate select switch and the console SLU connection. The H3601–SA panel, shown in Figure 1–3, covers the CPU and one additional backplane slot.

Figure 1–3: KDJ11–BF CPU I/O Panel (BA200-Series)



The baud rate select switch has 16 positions, 0 through 15. The first eight positions (0 through 7) select a baud rate and force the system to enter a boot mode specified by the EEPROM. Positions 8 through 15 select the same baud rates as positions 0 through 7, but override the EEPROM settings and put the system into dialog mode (Section 1.6).

Switch positions 0 through 7 force the system to access the EEPROM. The EEPROM determines what action to take after successful completion of the power-up self-test. The default setting of the EEPROM causes an automatic boot at power-up and restart. Table 1–4 lists the baud rate and mode switch settings.

Table 1–4: KDJ11–B Baud Rate and Mode Switch Settings

Baud Rate	EEPROM Selects Boot Mode	Dialog Mode
48,500	0	8
19,200	1	9
9600	2[1]	10
4800	3	11
2400	4	12
1200	5	13
600	6	14
300	7	15

[1]Factory setting

1.4 Boot and Diagnostic ROM Code

The KDJ11–B module contains two EPROMs and one EEPROM. The EPROMs contain CPU boot and diagnostic read-only memory (ROM) code. The ROM uses the EEPROM to store information needed to set up the KDJ11–B for normal operation.

The original KDJ11–B module contains Version 6.0 (V6.0) ROMs. The updated KDJ11–B modules contain either V7.0 or V8.0 ROMs. Appendix A explains the ROM differences and describes how to identify the KDJ11–B version. The ROM descriptions in this chapter reflect the V8.0 ROMs.

The EPROMs and the EEPROM have the following uses:

EPROM (16K x 16 bits in two EPROMs):

- Power-up diagnostics for CPU and memory
- Bootstrap programs
- EEPROM setup program

EEPROM (2K or 8K x 8 bits in one EEPROM):

- Hardware parameters
- Boot device selection
- Foreign language test
- Optional customer bootstrap programs

1.5 Automatic Boot Mode

After the successful completion of the KDJ11–B start-up self-test, the ROM code loads the first 105 bytes of the EEPROM into memory beginning at location 2000. This area in memory is referred to as the *setup table.*

The factory configuration of the setup table initiates automatic boot mode, which searches an automatic boot sequence table for the appropriate action to take. The default setting (selection A) in the automatic boot sequence table directs the system to search for, identify, and attempt to boot an operating system from available mass storage control protocol (MSCP) devices (units 0 through 7). If an MSCP device is not found, the system searches for a non-MSCP device.

When a bootable medium is found, the system boots. If a bootable medium is not available, the following message appears:

```
Testing in progress - Please wait.
1 2 3 4 5 6 7 8 9
Waiting for media to be loaded, or drive to go ready.
Press the Return key when ready to continue.
```

When you press RETURN, the following message appears:

```
Message 07
None of the selected devices were bootable.
Press the Return key when ready to continue or to list boot
messages.
```

When you press RETURN, the system lists the boot messages and enters dialog mode.

1.6 Dialog Mode

The KDJ11–B dialog mode lets you perform the following functions:

- Change the CPU parameters
- Select the boot source
- Display a list of all boot programs
- List all memory and occupied register locations in the system
- Run the start-up self-test in a loop
- Enter ROM octal debugging technique (ODT)

The system enters dialog mode if any of the following actions occur:

- The user enters CTRL/P or CTRL/C during the start-up self-test.
- Parameter D (power-up) or E (restart) is set to 0 in the setup table.
- The baud rate select switch is set to any position from 8 to 15.

Dialog mode has the following six commands, which you select by typing the first letter of the command:

1. HELP. Displays a one-screen help file that provides a short description of each command.
2. BOOT. Allows you to select the boot source. You select the source using a mnemonic for a device name, followed by a unit number (for example, DU1). You can specify the unit number as an octal value by typing /O after the unit number (for example, DU1/O). You can assign a nonstandard CSR address by typing /A after the unit number (for example, DU1/A). If you specify an octal value and a nonstandard address, do not repeat the slash (for example, DU1/OA).
3. LIST. Displays a list of all boot programs available in the ROM and the EEPROM. The list includes the device name, unit number range, source of the program, and device type.
4. SETUP. Enters setup mode. You can access and change the operating parameter settings and any bootstrap programs stored in the EEPROM. Setup mode consists of 15 commands, listed in Section 1.7.
5. MAP. Searches for, identifies, and lists all memory in the system and all occupied register locations in the I/O page.
6. TEST. Runs the ROM code start-up self-test in a loop. Type CTRL/C to exit the loop.

1.7 Setup Mode

Table 1–5 lists the setup mode commands to change the operating parameter settings and any bootstrap programs stored in the EEPROM.

Sections 1.7.1 through 1.7.15 explain the setup mode commands.

Table 1–5: KJD11–B Setup Mode Commands

Command Number[1]	Description
1	Exit.
2	List or change the parameters.
3	List or change the boot translations.
4	List or change the automatic boot selections.
5	Reserved.
6	List or change the switch boot selections.
7	List the boot programs.
8	Initialize.
9	Save the setup table into the EEPROM.
10	Load EEPROM data.
11	Delete an EEPROM boot.
12	Load an EEPROM boot into memory.
13	Edit or create an EEPROM boot.
14	Save the boot into the EEPROM.
15	Enter the ROM ODT.

[1]Use these numbers to enter the setup commands.

1.7.1 Command 1: Exit Setup Table

Setup command 1 returns you to dialog mode. Entering this command is equivalent to entering CTRL/C.

1.7.2 Command 2: List or Change Parameters in Setup Table

Setup command 2 allows you to set 15 CPU parameters using parameters A through O. Command 2 also allows you to disable the setup mode and the testing using parameters P and Q. Table 1–6 describes the setup parameters.

Table 1–6: KDJ11–B Setup Parameters

Parameter/Description	Values		Default
A. Enable halt-on-break	0 = No	1 = Yes	0
B. Disable user-friendly format	0 = No	1 = Yes	1
C. ANSI video terminal (1)	0 = No	1 = Yes	1
D. Power up[1]	2 = ODT	3 = 24	1

[1]0 = dialog, 1 = automatic

Table 1–6 (Cont.): KDJ11–B Setup Parameters

Parameter/Description	Values		Default
E. Restart[1]	2 = ODT	3 = 24	1
F. Ignore battery	1 = No	1 = Yes	0
G. PMG count		0–7	7
H. Disable clock CSR	0 = No	1 = Yes	0
I. Force clock interrupts	0 = No	1 = Yes	0
J. Clock[2]	2 = 60 Hz	3 = 80 Hz	0
K. Enable ECC test	0 = No	1 = Yes	1
L. Disable long memory test	0 = No	1 = Yes	0
M. Disable ROM[3]	2 = Dis 173	3 = Both	0
N. Enable trap on halt	0 = No	1 = Yes	0
O. Allow alternate boot block	0 = No	1 = Yes	0
P. Disable setup mode	0 = No	1 = Yes	1
Q. Disable all testing	0 = No	1 = Yes	0

[1] 0 = dialog, 1 = automatic

[2] 0 = power supply, 1 = 60 Hz

[3] 0 = No, 1 = Dis 165

The ROM code displays the current status of all parameters, repeats the first parameter, and then waits for your input:

- To move to the desired parameter, type the letter of the parameter and press RETURN.
- To change a parameter, type in the new value and press RETURN.
- To return to a previous parameter, type a caret (^) or a dash (–).
- If you do not want to make changes, press RETURN.
- To exit, enter CTRL/Z.

The functions of the setup parameters are as follows:

- **A. Enable halt-on-break**. Determines how the processor handles a break condition from the console terminal.

  0 = Ignore a break condition. Default.
  1 = Halt on a break.

- **B. Disable user-friendly format**. Enables or disables the user-friendly mode. Normally used with the automatic boot mode.

  0 = Disable user-friendly mode. Default.
  1 = Enable user-friendly mode.

- **C. ANSI video terminal**. Indicates the type of console terminal. If you use a terminal in the VT200 or VT300 series as the console device, set this parameter to 0.

  0 = Hardcopy terminal. Pressing the delete key enters a slash character.
  1 = ANSI video terminal. Pressing the delete key erases the previous character on the screen. Default.

- **D. Power-up mode**. Same as E.

- **E. Restart mode**. Parameters D and E use the same settings. When the ROM code starts, it determines if the power-up or restart switch was activated. In either case, the ROM code enters a mode based on one of the following:

  0 = Enters dialog mode at the completion of the diagnostics.
  1 = Enters automatic boot mode at the completion of diagnostics. Tries to boot devices in the order you select in the boot sequence table. Default.
  2 = Enters ODT mode at the completion of a limited set of tests. The ROM code executes a halt instruction and passes control to the micro-ODT.
  3 = Enters location 24 mode. The ROM code loads the processor status word (PSW) with the contents of location 26, then jumps to the address stored in location 24. This mode is used for power fail recovery when battery backed-up memory or nonvolatile memory is present.

- **F. Ignore battery**. Use this parameter when parameters D and E are set to 3.

  0 = Memory battery OK signal must be present to execute 24 mode. Default.
  1 = Ignore battery.

- **G. Processor mastership grant (PMG) count**. Sets the PMG count in the boot control and status register (BCSR). The range is 0 through 7.

  0 = Counter disabled.
  1 through 7 = KDJ11–B suppresses DMA requests and gives bus mastership to the processor during the next DMA cycle. Default = 7.

- **H. Disable clock CSR**. Enables or disables the clock control status register (CSR).

  0 = Enable clock CSR. Default.
  1 = Disable clock CSR at address 17777546.

- **I. Force clock interrupts**. Requests interrupts. If you select force clocks, disable the clock CSR with parameter H.

  0 = The clock requests interrupts only if the clock CSR is enabled. Default.
  1 = The clock unconditionally requests interrupts when the processor priority is 5 or less.

- **J. Clock select**. Determines the source of the clock to use as follows:

  0 = Backplane pin BR1. The power supply normally drives this signal internally at 50 or 60 Hz. Default.
  1 = 50 Hz.
  2 = 60 Hz.
  3 = 80 Hz.

- **K. Enable error correction code (ECC) test**. Enables or disables the ECC test.

  0 = ROM code bypasses the ECC test.
  1 = Enables the ECC memory test if the memory type is ECC. The test is disabled automatically for parity-type memories. Default.

- **L. Disable long memory test**. Selects an address-shorts-data test for memory.

  0 = Run an address-shorts-data test on all available memory.
  1 = Bypass the memory address-shorts-data test for all memory above 256 Kbytes.

- **M. Disable ROM**. Disables all or part of the ROM code after the selected device has booted.

  0 = ROM code responds to two 256 work pages in the I/O pages. The I/O pages are enabled at power-up or restart. Default.
  1 = Disable 165.
  2 = Disable 173.
  3 = Disable both.

- **N. Enable trap-on-halt**. Controls how the processor reacts to a halt instruction in kernel mode.

  0 = Processor enters micro-ODT if it executes a halt instruction in kernel mode. Default.
  1 = Processor jumps to location 4 if it executes a halt instruction in kernel mode.

- **O. Allow alternate boot block**. The boot ROM code checks for bootable media on a device by loading the boot block from the device into memory and then testing it.

  0 = ROM code considers the medium bootable if the word at location 0 is between 240 and 277, and the word at location 2 is between 400 and 777. If the medium is bootable, the ROM code jumps to location 0 of the boot block. Default.
  1 = ROM code considers the medium bootable if the word at location 0 is any nonzero number. To boot properly, operating systems that are not DIGITAL systems may require you to set this parameter to 1.

- **P. Disable setup mode**. If you select the forced dialog mode, setup mode is enabled unconditionally regardless of the value of this parameter. This parameter prevents unauthorized entry into setup mode, assuming the forced dialog mode switch (switch 5 on the KDJ11–B CPU module) is on. Not available in V6.0 ROM code.

  0 = Setup mode enabled.
  1 = User cannot enter the setup mode from dialog mode. The command lines with the commands normally available in dialog mode do not show the setup commands.

- **Q. Disable all testing**. If you select this parameter at the start of the ROM code and you do not select the forced dialog mode, the ROM code bypasses virtually all testing. In addition, the ROM code does not change any locations in memory, unless the selected boot program makes a change. Parameter Q is not available in V6.0 ROM code.

  Use this parameter only if you need immediate response at power-up, with the contents of memory unaltered.

1.7.3 Command 3: List or Change Boot Translation in Setup Table

Setup command 3 prints out the current contents of the translation table and allows you to change the table. Use this command to perform the following functions:

- Boot devices that use nonstandard CSR addresses
- Change a CSR address when two or more devices share the same address
- Boot multiple MSCP devices with different controllers
- Handle multiple controllers of the same type

Setting a Nonstandard CSR Address

As an example of the use of command 3, suppose a system contains the following devices:

- RD50-series fixed-disk drive
- RX50 dual-diskette drive
- RC25 fixed and removable disk drive

The RX50 and RD-series drives use an RQDX3 controller module at the standard CSR address of 17772150. The RC25 controller module also uses a standard CSR address of 17772150. Since two devices cannot use the same CSR address in one system, you must change the CSR jumpers on one module.

The RD-series drive is disk unit 0 (DU0). The dual-diskette RX50 drive uses DU1 and DU2. The RC25 has a unit number select plug on its front panel that is set for units 4 and 5. (The first unit number of an RC25 is always even.) Since the RC25 has two unit numbers, there are two entries in the translation table. These entries set the CSR address to the new value as follows:

```
TT1 blank
Device name = DU
Unit number = 4
CSR address = 17760500
TT1  DU4 address 17760500
TT2  blank
Device name = DU
Unit number = 5
CSR address = 17760500
TT2  DU5 address 17760500
TT3  blank
Device name = press Return for no change
```

1.7.4 Command 4: List or Change the Automatic Boot Selection in Setup Table

Setup command 4 lets you select the devices to be tried in the automatic boot sequence. You create a list and then define the devices, their unit numbers, and the order the system is to try them. There are four special single-letter device names as follows:

- **A. MSCP automatic boot**. Causes the ROM code to find up to eight MSCP devices (units 0 through 7) at the standard CSR address. The ROM code tries to boot each removable media device in turn, then each fixed-media device. Using setup command 3, you must individually select each MSCP device that does not have a standard CSR address.
- **B. Off-board boot**. Causes the ROM code to check for an off-board ROM at address 17773000. When an off-board ROM exists and its first location is not 0, the ROM code disables the internal code and jumps to address 17773000 of the off-board ROM.

  NOTE: *Device name B implements a method of supporting boot devices that are not DIGITAL devices on the Q22-bus.*
- **E. Exit automatic boot**. Signals the ROM code that there are no other devices to try. When fewer than six devices exist, follow the last device to be tried with this entry.
- **L. Exit automatic boot-reboot (V7.0 and V8.0 only)**. Similar to the D option except that when this mnemonic is reached, the ROM code restarts the boot sequence at the beginning of the list until either a successful boot has occurred or the sequence is terminated when you enter CTRL/C.

1.7.5 Command 5: Store up to 20 Bytes in the EEPROM

Setup command 5 lets you store up to 20 bytes of serial numbers in the EEPROM. The setup mode initialize command (setup command 8) resets this data to zero.

1.7.6 Command 6: List or Change the Switch Boot Selection in Setup Table

Setup command 6 lets you define the value of switches 2, 3, and 4 of the E83 DIP switch, to boot specific devices. When the switches are all off (default), the EEPROM determines the action to take. When switch 5 is off and the baud rate select switch is set from 8 to 15, the ROM code selects dialog mode and overrides any switch settings you selected.

1.7.7 Command 7: List Boot Programs

Setup command 7 lists all available boot programs in the two EPROMs and the EEPROM. It displays the device name, unit number range, source of the boot program, and a short device description. This command works the same as the dialog mode LIST command.

1.7.8 Command 8: Initialize Setup Table

Setup command 8 initializes the current contents of the setup table in memory to the default values and resets the contents of the EEPROM to zero. To save the setup table into the EEPROM, you must execute the SAVE command (setup command 9).

1.7.9 Command 9: Save Setup Table into the EEPROM

Setup command 9 copies the current contents of the setup table into the EEPROM. This command writes data into the first 105 bytes of the EEPROM.

1.7.10 Command 10: Load EEPROM Data into Setup Table

Setup command 10 restores the setup table in memory with the values stored in the EEPROM.

1.7.11 Command 11: Delete an EEPROM Boot

Setup command 11 asks you for the device name of the EEPROM boot you wish to delete. Enter the device name. The ROM code searches for and deletes the first boot program in the EEPROM (if it is found). Then the ROM code moves all the following boot programs up, to use the space made available by the deleted program.

1.7.12 Command 13: Load an EEPROM Boot into Memory

Setup command 12 lets you load an EEPROM boot program into memory to examine or edit it. The ROM code prompts you for the device name of the EEPROM boot.

1.7.13 Command 13: Edit or Create an EEPROM Boot

Setup command 13 lets you create a new EEPROM boot program or edit a program that was loaded with command 12. This command can change the following items:

- Device name. Designated by the firmware for the device; for example, disk unit (DU).
- Device description. Usually the physical name of the device. The maximum length allowed for this description is 11 characters and spaces.
- Allowable unit number range. The highest unit number defines the allowable range of valid unit numbers for the device.

- Beginning and ending address of the program in memory. The address of the last byte of code used in memory.
- The starting address of the program. The address to which the ROM code passes control.

This command lists the available space in the EEPROM for boots and prompts for entries. The ROM code enters ROM ODT when changes are completed. (See setup command 15.) You must use command 14 to save any changes you made with command 13.

1.7.14 Command 14: Save Boot into EEPROM

Setup command 14 is the only command that writes a boot from memory into the EEPROM. Other commands only change a copy of the boot program that resides in memory. When you save a boot program into memory, the device name of the program must not match the name of a program that already exists in the EEPROM. If you write two or more programs into the EEPROM with the same name, only the first one is bootable.

1.7.15 Command 15: Enter ROM ODT

Setup command 15 invokes the ROM octal debugging technique (ODT). The ROM code opens the address defined by the beginning address of the program. ROM ODT is not the same as micro-ODT. The only allowable addresses in ROM ODT are the addresses of memory from 0 to 28K words (0 to 00157776). You cannot access the I/O page from ROM ODT. Table 1–7 lists the ROM ODT commands.

Table 1–7: KDJ11–B ROM ODT Commands

Command	Symbol	Function
Forward slash	/	Prints contents of specified address location or prints contents of last opened location. If opened location is an odd number, prints only the contents of the byte. If the location is even, the mode is word. If the location is odd, the mode is byte. ROM ODT assumes leading zeros and uses only the last six octal digits. (See the example following this table.)
Return	<CR>	Closes an open location.
Line Feed	<CR>	Closes an open location and then opens the next location. If in word mode, increment by 2; if in byte mode, increment by 1.
Period	.	Alternate character for line feed. Used with VT200-series terminals.

Table 1–7 (Cont.): KDJ11–B ROM ODT Commands

Command	Symbol	Function
Caret	^	Closes an open location and then opens the previous location. If in word mode, decrement by 2; if in byte mode, decrement by 1.
Minus	–	Alternate character for caret. Used with VT200-series terminals.
Delete	DELETE	Deletes the previous character typed.
CTRL/Z	CTRL/Z	Exit ROM ODT and return to setup mode.

Here are some examples of the use of the forward slash:

```
ROM ODT> 200/1000000              ! Open location 200
ROM ODT> 1001/240                 ! Open byte location 1001
ROM ODT> 77777750020/100000       ! Open location 00150020
ROM ODT> 77770000/                ! Illegal location >157776
```

1.8 MSV11–P Memory

The MSV11–P memory is a quad-height module that occupies the slot(s) in the backplane immediately following the KDJ11–BB or –BC CPU in slot 1.

The MSV11–P module contains 64K metallic oxide semiconductor (MOS) chips that provide storage for 18-bit words (16 data bits and 2 parity bits). The MSV11–P also contains parity control circuitry and a control status register. The memory module variants and their storage capacities are as follows:

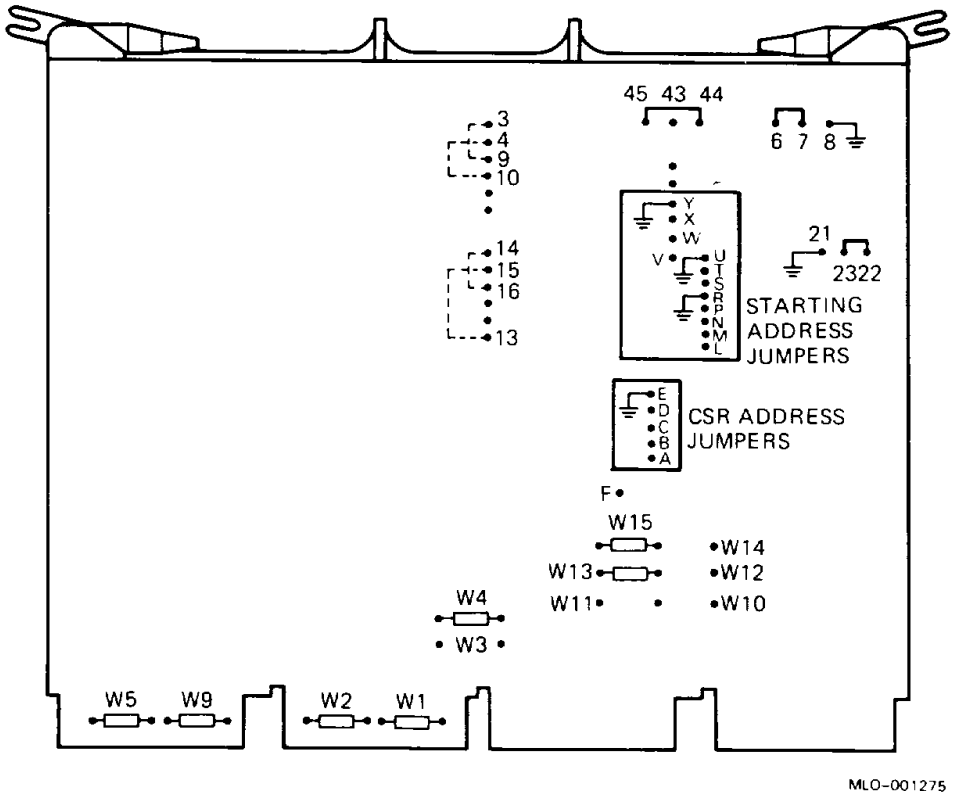
- MSV11–PK (M8967–K): 256 Kbytes
- MSV11–PL (M8067–L): 512 Kbytes

You configure the MSV11–P, shown in Figure 1–4, by means of jumpers and wire-wrap pins. The –PK and –PL modules have the same factory configuration.

The MSV11–P module has two LEDs that show the following status:

- A green LED: lights to indicate that +5 Vdc is present.
- A red LED: lights to indicate that a parity error has been detected.

Figure 1–4: MSV11–P Module Layout



1.8.1 MSV11–P Expansion Addresses

You can install additional MSV11–P modules for system expansion.

For each memory module that you add to the Q22-bus, you must reposition jumpers on the wire-wrap pins to provide a CSR address and a starting address.

Figure 1–4, above, shows the CSR address jumpers on the MSV11–P module. Table 1–8 lists the CSR address and corresponding jumper configurations for each memory module (–PK or –PL) added to the system.

Table 1–8: MSV11–P CSR Addresses and Jumpers

Module No. in System	Pins to Wire-Wrap	CSR Address x = 177721
1	None	x00
2	A to E	x02
3	B to E	x04
4	A to B, B to E	x06
5	C to E	x10
6	A to C, C to E	x12
7	B to C, C to E	x14
8	A to B, B to C, C to E	x16

The starting address depends on the amount of memory already present in the system.

Table 1–9 lists the first address ranges (FAR) to select the 256K word range. Table 1–10 lists the partial starting address (PSA) ranges for additional MSV11–P memory modules.

Table 1–9: MSV11–P First Address Ranges

First Address Ranges		
Decimal K Words	**Octal K Words**	**Pins to Wire-Wrap**
000–248	00000000–01740000	None
256–504	02000000–03740000	V to Y
512–760	04000000–05740000	W to Y
768–1016	06000000–07740000	W to Y, V to Y
1024–1727	10000000–11740000	X to Y
1280–1528	12000000–13740000	X to Y, V to Y
1526–1784	14000000–15740000	X to Y, W to Y
1742–2040	16000000–17740000	X to Y, W to Y, V to Y

Table 1–10: MSV11–P Partial Starting Address Ranges

Partial Starting Address		
Decimal K	**Octal**	**Pins to Wire-Wrap**
0	00000000	None
8	00040000	T to R
16	00100000	L to R
24	00140000	L to R, T to R
32	00200000	M to R
40	00240000	M to R, T to R
48	00300000	M to R, L to R
56	00340000	M to R, L to R, T to R
64	00400000	N to R
72	00440000	N to R, T to R
80	00500000	N to R, L to R
88	00540000	N to R, L to R, T to R
96	00600000	N to R, M to R
104	00640000	N to R, M to R
112	00700000	N to R, M to R, L to R
120	00740000	N to R, M to R, L to R, T to R
128	01000000	P to R
136	01040000	P to R, T to R
144	01100000	P to R, L to R
152	01140000	P to R, L to R, T to R
160	01200000	P to R, M to R
168	01240000	P to R, M to R, T to R
176	01300000	P to R, M to R, L to R
184	01340000	P to R, M to R, L to R, T to R
192	01400000	P to R, N to R
200	01440000	P to R, N to R, T to R
208	01400000	P to R, N to R, L to R
216	01540000	P to R, N to R, L to R, T to R
224	01600000	P to R, N to R, M to R
232	01640000	P to R, N to R, M to R, T to R
240	01700000	P to R, N to R, M to R, L to R
248	01740000	P to R, N to R, M to R, L to R, T to R

Table 1–11 lists the jumper configuration for additional MSV11–PK modules. Table 1–12 lists the jumper configuration for additional MSV11–PL modules.

Table 1–11: MSV11–PK Starting Address Jumpers (256-Kbyte increments)

Module No. in System	Pins to Wire-Wrap
1	None
2	P to R
3	V to Y
4	V to Y, P to R
5	W to Y
6	W to Y, P to R
7	W to Y, V to Y
8	W to Y, V to Y, P to R

Table 1–12: MSV11–PL Starting Address Jumpers (512-Kbyte increments)

Module No. in System	Pins to Wire-Wrap
1	None
2	V to Y
3	W to Y
4	V to Y, W to Y
5	X to Y
6	X to Y, V to Y
7	X to Y, W to Y
8	X to Y, W to Y, V to Y

For more information on the MSV11–P memory, refer to the *MSV11–P User's Guide* (EK–MSVOP–UG).

1.9 MSV11–Q Memory

The MSV11–Q memory is a quad-height module that occupies the slot(s) in the backplane immediately following the KDJ11–BB or –BC CPU in slot 1. The MSV11–Q module has a 1, 2, or 4 Mbyte capacity using either 64K or 256K MOS dynamic RAMs. The control status register (CSR) contains bits used to store the parity error address bits. You can force wrong parity by setting a bit in the CSR to check the parity logic.

Figure 1–5 shows the MSV11–Q module. Table 1–13 lists the memory module variants and their storage capacities.

Figure 1–5: MSV11–Q Module Layout

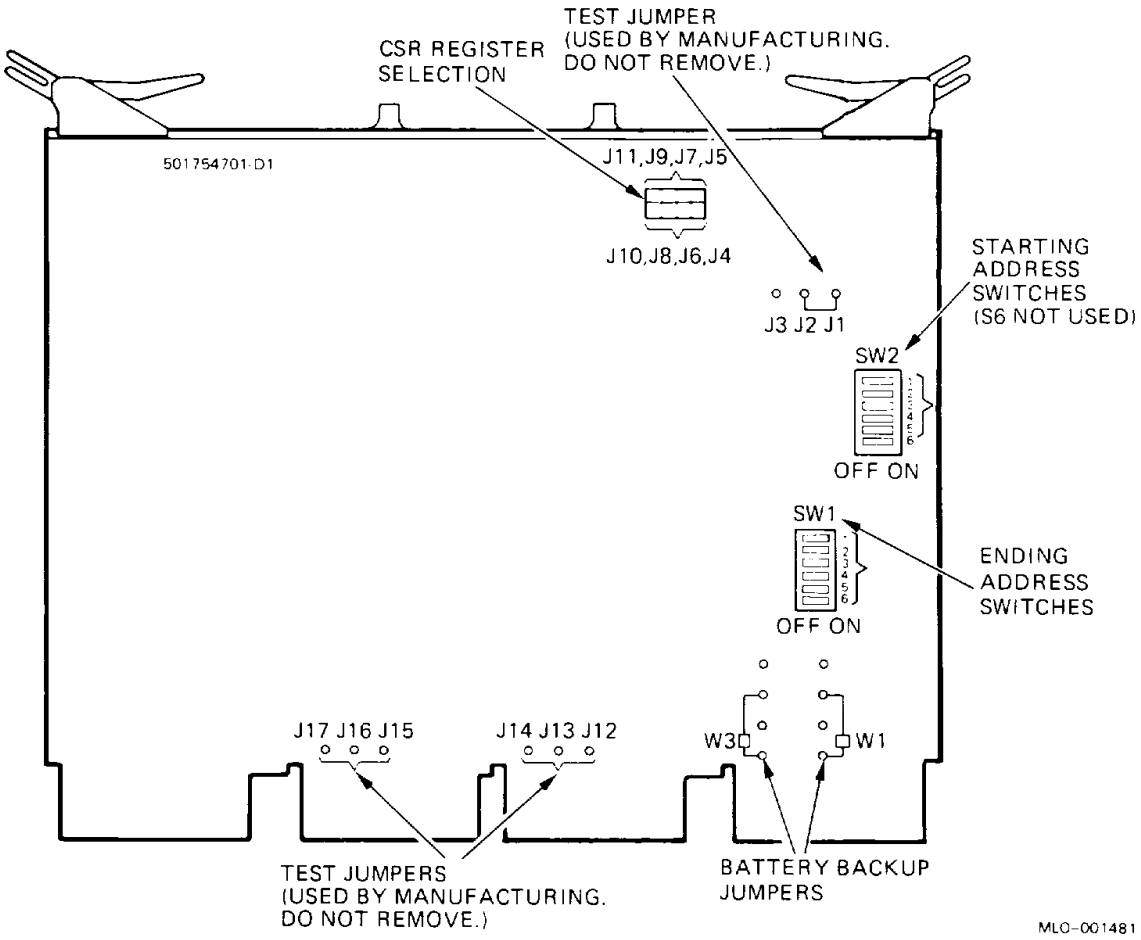


Table 1–13: MSV11–Q Variants

Revision[1]	Option	Module	Storage	RAM Size
A, C	MSV11–QA	M7551–AA	1 Mbyte	56K
C	MSV11–QB	M7551–BA	2 Mbyte	256K (half populated)
C	MSV11–QC	M7551–CA	4 Mbyte	256K (fully populated)

[1]Identify the revision level by the following printed circuit board number:

A = 5017547A1 on upper right corner of component side of module
C = 5017547–01–C1 on upper left corner of component side of module

You must configure the MSV11–Q starting and ending addresses using DIP switches SW1 and SW2 (Figure 1–5, above). SW1 is the ending address and SW2 is the starting address.

Table 1–14 lists the switch settings for the starting and ending addresses.

Table 1–14: MSV11–Q Starting and Ending Addresses

Starting Address (in Kbytes)	SW2 Position[1] 12345[2]	SW1 Position 6	Ending Address (in Kbytes)	SW1 Position 12345[2]
0	00000	0	128	1111
128	11111	1	256	01111
256	01111	1	384	10111
384	10111	1	512	00111
512	00111	1	640	11011
640	11011	1	768	01011
768	01011	1	896	10011
896	10011	1	1024 (1 Mbyte)	00011
1024 (1 Mbyte)	00011	1	1152	11101
1152	11101	1	1280	01101
1280	01101	1	1408	10101
1408	10101	1	1536	00101
1536	00101	1	1664	11001
1664	11001	1	1792	01001
1792	01001	1	1920	10001
1920	10001	1	2048 (2 Mbytes)	00001
2048 (2 Mbytes)	00001	1	2176	11110
2176	11110	1	2304	01110
2304	01110	1	2432	10110
2432	10110	1	2560	00110
2560	00110	1	2688	11010
2688	11010	1	2816	01010
2816	01010	1	2944	10010
2944	10010	1	3072 (3 Mbytes)	00010
3072 (3 Mbytes)	00010	1	3200	11100

[1]Switch S6 of SW2 is not used. For a memory starting address of 0, set switch S6 of SW1 to on (0). For all other starting addresses, set switch S6 of SW1 to off (1).

[2]1 = off; 0 = on

Table 1–14 (Cont.): MSV11–Q Starting and Ending Addresses

Starting Address (in Kbytes)	SW2 Position[1] 12345[2]	SW1 Position 6	Ending Address (in Kbytes)	SW1 Position 12345[2]
3200	11100	1	3328	01100
3328	01100	1	3456	10100
3456	10100	1	3584	00100
3584	00100	1	3712	11000
3712	11000	1	3840	01000
3849	01000	1	3968	10000
3968	10000	1	4096 (4 Mbytes)	00000

[1]Switch S6 of SW2 is not used. For a memory starting address of 0, set switch S6 of SW1 to on (0). For all other starting addresses, set switch S6 of SW1 to off (1).

[2]1 = off; 0 = on

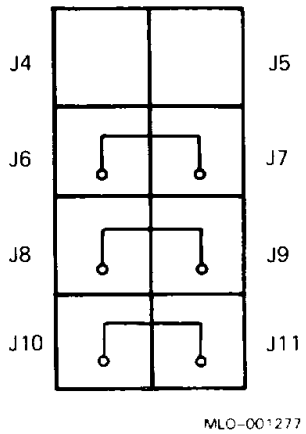
You configure the MSV11–Q CSR address by setting jumpers J4 through J11 (Figure 1–5, above). Table 1–15 shows the jumper positions and the corresponding CSR register addresses for up to 16 locations. Figure 1–6 shows the jumper settings for a CSR register address of 17772102, representing a second MSV11–Q.

Table 1–15: MSV11–Q CSR Addresses

Number CSR Memory[1]	Jumper J4 to J5	Jumper J6 to J7	Jumper J8 to J9	Jumper J10 to J11	CSR Address
1	In	In	In	In	x00
2	Out	In	In	In	x02
3	In	Out	In	In	x04
4	Out	Out	In	In	x06
5	In	In	Out	In	x10
6	Out	In	Out	In	x12
7	In	Out	Out	In	x14
8	Out	Out	Out	In	x16
9	In	In	In	Out	x20
10	Out	In	In	Out	x22
11	In	Out	In	Out	x24
12	Out	Out	In	Out	x26
13	In	In	Out	Out	x30
14	Out	In	Out	Out	x32
15	In	Out	Out	Out	x34
16	Out	Out	Out	Out	x36

[1]If more than one CSR parity-type memory is installed, use care to ensure that no two modules have the same address.

Figure 1–6: MSV11–Q CSR 17772102 Setting



The factory configuration for the remaining jumpers is listed in Table 1–16.

Table 1–16: MSV11–Q Factory Jumper Settings

Jumper	State	Condition
J1 to J2	In	For manufacturing test only. Do not remove.
J13 to J14	In	Selects 64K RAMs. Do not remove.
J15 to J16	In	Selects 64K RAMs. Do not remove.
W3, W1	In	Battery backup configuration.

For more information on the MSV11–Q, see *MSV11–Q MOS Memory User's Guide* (KE–MSV1Q–QG).

1.10 MSV11–J Memory

The MSV11–J memory is a quad-height module that occupies the first slot(s) in the backplane, before the KDJ11–BF CPU. The MSV11–J provides the following features:

- Error correction code (ECC) for increased reliability
- A CSR to store status and error information
- Support for the private memory interconnect (PMI) protocol and normal Q22-bus protocol
- Four jumpers and two switchpacks
- Starting addresses on 8K word boundaries
- Two LEDs

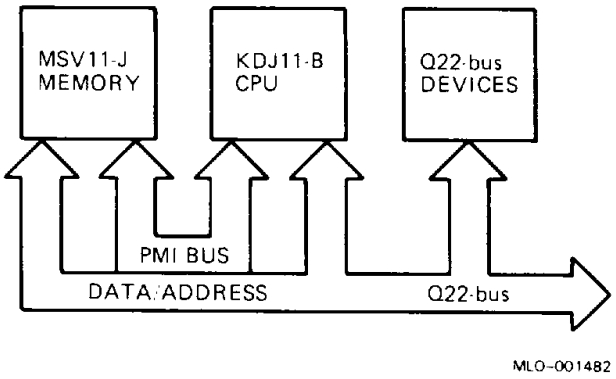
You can configure the MSV11–J with half populated or fully populated 256K dynamic RAMs. The MSV11–J variants and storage capacities are as follows:

- MSV11–JD (M8637–D): 1 Mbyte
- MSV11–JE (M8637–E): 2 Mbytes

The location of the MSV11–J in the backplane determines the protocol used between the KDJ11–BF CPU and the memory module.

The PMI protocol is shown in Figure 1–7.

Figure 1–7: PMI/Q22-Bus Interface



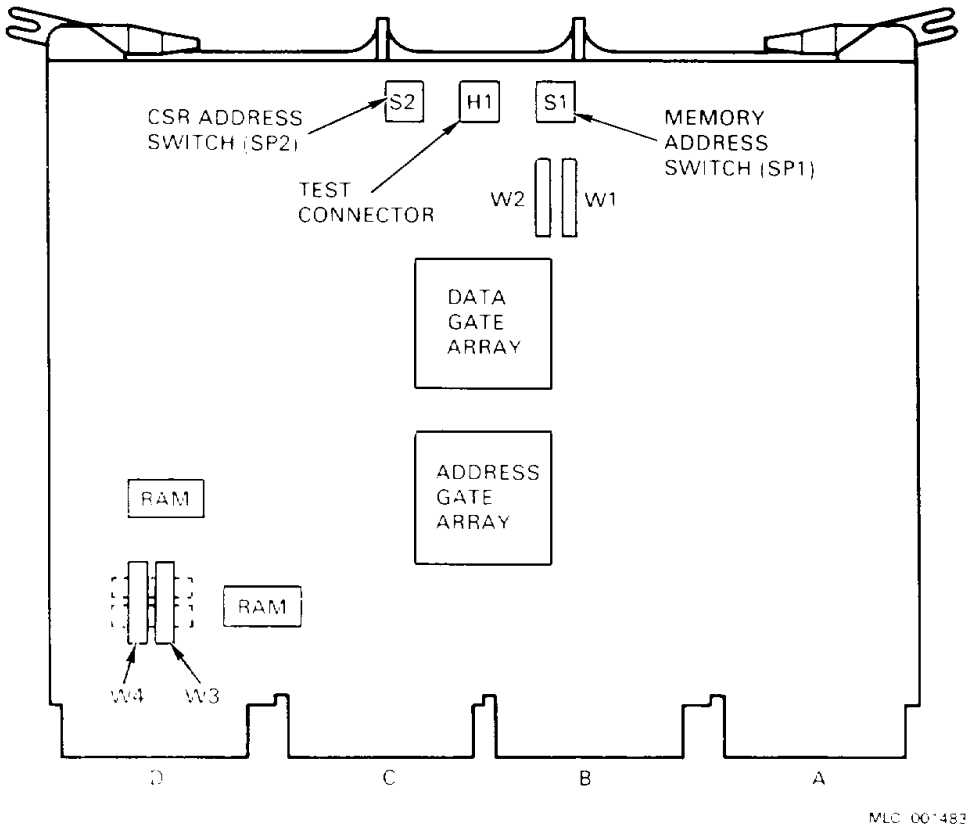
To use the PMI protocol, you must install the MSV11–J in the first backplane slot(s), followed by the KDJ11–BF CPU. Otherwise the memory and CPU communicate with the Q22-bus protocol. There can be no open slots between the memory and the CPU, nor can any open slots precede the MSV11–J.

Table 1–17 lists and describes the four factory installed jumpers on the MSV11–J module, shown in Figure 1–8. Confirm this configuration and change it as necessary.

Table 1–17: MSV11–JD/–JE Jumper Configuration

Jumper	Description
W1 In	Reserved for DIGITAL use only
W1 Out	256K dynamic RAMs
W2 In	Half populated module
W2 Out	Fully populated module
W3, W4 mounted left/right	Reserved for future battery backup
W3, W4 mounted up/down	+5 Vdc (factory position)

Figure 1–8: MSV11–JD/–JE Module Layout (M8637–D/M8637–E)



1.10.1 MSV11–J Addresses

The MSV11–J memory address switch is SP1, shown in Figure 1–8, above. You must set this switch to select the starting memory address.

Table 1–18 lists the switch settings in 8K increments. Table 1–19 shows typical settings.

Table 1–18: MSV11–J Starting Memory Address Ranges

Decimal (K Word)	Octal	Switch Setting (SP1)[1] 1 2 3 4 5 6 7 8
0	00000000	0 0 0 0 0 0 0 0
8	00040000	0 0 0 0 0 0 0 1
16	00100000	0 0 0 0 0 0 1 0
24	00140000	0 0 0 0 0 0 1 1
32	00200000	0 0 0 0 0 1 0 0
40	00240000	0 0 0 0 0 1 0 1
48	00300000	0 0 0 0 0 1 1 0
56	00340000	0 0 0 0 0 1 1 1
64	00400000	0 0 0 0 1 0 0 0
72	00440000	0 0 0 0 1 0 0 1
80	00500000	0 0 0 0 1 0 1 0
88	00540000	0 0 0 0 1 0 1 1
96	00600000	0 0 0 0 1 1 0 0
104	00640000	0 0 0 0 1 1 0 1
112	00700000	0 0 0 0 1 1 1 0
120	00740000	0 0 0 0 1 1 1 1
000–120	00000000–00740000	0 0 0 0 x x x x
128–248	01000000–01740000	0 0 0 1 x x x x
256–376	02000000–02740000	0 0 1 0 x x x x
384–504	03000000–03740000	0 0 1 1 x x x x
512–632	04000000–04740000	0 1 0 0 x x x x
640–760	05000000–05740000	0 1 0 1 x x x x
768–888	06000000–06740000	0 1 1 0 x x x x
896–1016	07000000–07740000	0 1 1 1 x x x x
1024–1144	10000000–10740000	1 0 0 0 x x x x
1152–1272	11000000–11740000	1 0 0 1 x x x x
1280–1400	12000000–12740000	1 0 1 0 x x x x
1408–1528	13000000–13740000	1 0 1 1 x x x x
1536–1656	14000000–14740000	1 1 0 0 x x x x
1664–1784	15000000–15740000	1 1 0 1 x x x x
1792–1912	16000000–16740000	1 1 1 0 x x x x
1920–2040	17000000–17740000	1 1 1 1 x x x x

[1] 1 = on; 2 = off; x = can be either off or on

Table 1–19: MSV11–J Typical Memory Starting Addresses

Option	Module No. in System	SP1 Switches[1] 1 2 3 4 5 6 7 8
MSV11–JD	1	0 0 0 0 0 0 0 0
	2	0 1 0 0 0 0 0 0
	3	1 0 0 0 0 0 0 0
MSV11–JE	1	0 0 0 0 0 0 0 0
	2	1 0 0 0 0 0 0 0

[1] 1 = on, 0 = off

The MSV11–J CSR address switch is SP2, shown in Figure 1–8. You must set this switch to configure the CSR address.

Table 1–20 lists the 16 possible CSR switch settings. Table 1–21 lists the settings according to the module number in the system.

Table 1–20: MSV11–J CSR Address Switch Settings

CSR Address (x = 177721)	Switch Setting 1 2 3 4
x00	0 0 0 0
x02	0 0 0 1
x04	0 0 1 0
x06	0 0 1 1
x10	0 1 0 0
x12	0 1 0 1
x14	0 1 1 0
x16	0 1 1 1
x20	1 0 0 0
x22	1 0 0 1
x24	1 0 1 0
x26	1 0 1 1
x30	1 1 0 0
x32	1 1 0 1
x34	1 1 1 0
x36	1 1 1 1

Table 1–21: MSV11–J Typical CSR Switch Settings

Module No. in System	Switch Setting 1 2 3 4	CSR Address x = 177721
1	0 0 0 0	x00
2	0 0 0 1	x02
3[1]	0 0 1 0	x04

[1]MSV11–JE only

Chapter 2
Configuration

2.1 Introduction

This chapter describes the rules and guidelines for changing the configuration of a KDJ11–B system. Before you change a system's configuration, you must consider the following factors:

Module order in the backplane
Module configuration
Mass storage device configuration

Section 2.2 lists the guidelines for module order and configuration. These guidelines apply to the KDJ11–B CPU in the BA23, BA123, and BA200-series enclosures.

If you are adding a device to a system, you must know the capacity of the system enclosure in the following areas:

Backplane
I/O panel
Power supply
Mass storage devices

Worksheets for the enclosures (Section 2.5) provide information about system capacities.

2.2 Module Order

The order of modules in the backplane depends on four factors:

- Relative use of devices in the system
- Expected performance of each device relative to other devices
- The ability of a device to tolerate delays between bus requests and bus grants (known as "delay tolerance" or "interrupt latency")
- The tendency of a device to prevent devices farther from the CPU from accessing the bus

The relative use and performance of devices depends on the application. This means the order of modules also depends on the application. Most applications try to balance the use of devices. To achieve maximum system performance, use the recommended order listed in Table 2–1. The order is based on the Q-bus DMA transfer characteristics; use it as a guideline. Make sure you read the rules and guidelines in Section 2.3 for placement of the CPU and memory modules.

Table 2–1: Q-Bus Recommended Module Order

Option Type	Option Example	Comments
Communications	DPV11	Synchronous
	DEQNA	Ethernet interface
	DRV11–J	General purpose
Line printer	LPV11	
Communications	DLVJ1	Asynchronous
	DMV11	Synchronous (DMA)
Disk controller	RLV12	
	RRD50	Read only
	KDA50	
	RQDX3	MSCP
Disk/tape controller	KLESI	
Tape controller	TQK50	
Disk controller	RQDX2	
General purpose interface	DRV11	

CAUTION: *If an option has Q/CD jumpers, check the documentation for that option for the correct Q/CD jumper settings. An incorrect jumper setting can cause damage to the option.*

When devices do not perform as expected, you can change the recommended module order to meet the needs of the application. Often, performance problems involve a device that is heavily used or has a low delay tolerance. Usually, there are other heavily used devices between the device with the low delay tolerance and the CPU. In this case, move the problem device closer to the CPU.

2.3 Configuration Rules

Follow these configuration rules when you install or remove modules from the card cage:

KDJ11–BB/–BC CPU with MSV11–P or MSV11–Q Memory (MicroPDP–11/73)

- Always install the KDJ11–BB/–BC CPU module in slot 1.
- Always install the MSV11–P or MSV11–Q memory module(s) in the slots immediately following the CPU, beginning with slot 2.
- Make sure you maintain the Q22-bus grant continuity for all Q22-bus devices in the system. Each Q22-bus slot that comes before a Q22-bus device on the grant continuity chain must contain an M9047 grant continuity card or another Q22-bus device.
- Install modules following the CPU and memory using the sequence shown in Table 2–1.
- Refer to the applicable enclosure maintenance documentation for enclosure-specific guidelines for the I/O panel and configuration of the backplane.

KDJ11–BF CPU with MSV11–J Memory (MicroPDP–11/83)

- Always install the MSV11–J memory module(s) first, beginning with slot 1.
- Always install the KDJ11–BF CPU module in the slot immediately following the MSV11–J module(s).
- Make sure you maintain the Q22-bus grant continuity for all Q22-bus devices in the system. Each Q22-bus slot that comes before a Q22-bus device on the grant continuity chain must contain an M9047 grant continuity card or another Q22-bus device.
- Install modules following the CPU and memory using the sequence shown in Table 2–1.
- Refer to the applicable enclosure maintenance documentation for enclosure-specific guidelines for the I/O panel and configuration of the backplane.

2.4 Configuration Procedure

Each module in a system must use a unique device address and interrupt vector. The device address is also known as the control status register (CSR) address. Most modules have switches or jumpers for setting the CSR address and interrupt vector values.

Calculating address and vector values is a complex procedure because some modules use floating addresses and vectors. The value of a floating address depends on the other modules in the system.

See *Microsystems Options* for CSR addresses and interrupt vectors for MicroPDP–11 options. Most modules have switches and jumpers to change their operating characteristics. For some applications, you may have to change the factory switch and jumper positions according to the guidelines in *Microsystems Options*.

NOTE: *Changing the factory positions may affect the operation of the diagnostics for the device.*

2.5 Configuration Worksheets

Use the following configuration worksheets, located at the end of this chapter, to make sure a configuration does not exceed a system's limits for expansion space, I/O space, power, and bus loads:

Enclosure	Worksheet
BA23	Figure 2–1
BA123	Figure 2–2
H9642–J	Figure 2–3
BA200-series	Figure 2–4

If you use standard DIGITAL modules, you will not exceed the limits for bus loads.

Use the configuration worksheet as follows:

1. List all the devices already installed in the system.
2. List all the devices you plan to install in the system.
3. Fill in the information for each device, using the data listed in Table 2–2 for BA200-series enclosures or Table 2–3 for all other enclosures.
4. Add up the columns. Make sure the totals are within the limits for the enclosure power supply.

Table 2–2: Power and Bus Load Data (BA200-Series)

		Current (Amps)		Power	Bus Loads	
Option	**Module**	**+5 V**	**+12 V**	**Watts**	**AC**	**DC**
AAV11–SA	A1009–PA	1.8	0.0	9.0	2.1	0.5
ADV11–SA	A1008–PA	3.2	0.0	16.0	2.3	0.5
AXV11–SA	A026–PA	2.0	0.0	10.0	1.2	0.3
KWV11–SA	M4002–PA	2.2	0.130	11.16	1.0	0.3
CXA16–M	M3118–YA	1.6	0.20	10.4	3.0	0.5
CXB16–M	M3118–YB	2.0	0.0	10.0	3.0	0.5
CXY08–M	M3119–YA	1.8	0.30	12.6	3.2	0.5
DELQA–SA	M7516–PA	2.7	0.5	19.5	2.2	0.5
DEQNA–SA	M7504–PA	3.5	0.50	23.5	2.2	0.5
DFA01	M3121–PA	1.97	0.40	14.7	3.0	1.0
DPV11–SA	M8020–PA	1.2	0.30	9.6	1.0	1.0
DRV1J–SA	M8049–PA	1.8	0.0	9.0	2.0	1.0
DRV1W–SA	M7651–PA	1.8	0.0	9.0	2.0	1.0
DZQ11–SA	M3106–PA	1.0	0.36	9.3	1.4	0.5
IEQ11–SA	M8634–PA	3.5	0.0	17.5	2.0	1.0
KDJ11–BB	M8190	5.5	0.1	28.7	2.3	1.1
KDJ11–BC	M8190	5.5	0.1	28.7	2.3	1.1
KDJ11–BF	M8190	5.5	0.2	29.9	2.6	1.0
KMV1A–SA	M7500–PA	2.6	0.2	15.4	3.0	1.0
KWV11–SA	M4002–PA	2.2	0.13	11.16	1.0	0.3
LPV11–SA	M8086–PA	1.6	0.0	8.0	1.8	0.5
M9060	M9060–YA	5.3	0.0	26.5	0.0	0.0
MSV11–JD	M8637–D	3.74	0.0	18.7	2.7	0.5
MSV11–JE	M8637–E	4.1	0.0	20.5	2.7	0.5
MSV11–PK	M8067–K	3.45	–	17.25	2.0	1.0
MSV11–PL	M8067–L	3.6	–	17.5	2.0	1.0
MSV11–QA	M7551–AA	2.4	0.0	12.0	2.0	1.0
MSV11–QB	M7551–BA	2.3	0.0	11.5	2.0	1.0
MSV11–QC	M7551–CA	2.5	0.0	12.5	2.0	1.0
RF30–S	–	1.25	2.85	18.3	–	–
TK50	–	1.35	2.4	33.55	–	–
TQK50	M7546	2.9	0.0	14.5	2.0	1.0

Table 2–3: Power, Bus Load, and I/O Insert Data (BA23, BA123)

		Current (Amps)		Power	Bus Loads		
Option	**Module**	**+5 V**	**+12 V**	**Watts**	**AC**	**DC**	**Insert[1]**
AAV11-D[2]	A1009	1.8	0.0	9.0	1.0	1.0	–
ADV11-D[2]	A1008	3.2	0.0	16.0	1.0	1.0	–
DEQNA	M7504	3.5	0.5	23.5	2.8	0.5	A
DELQA	M7516	2.7	0.5	19.5	2.2	0.5	A
DHV11	M3104	4.5	0.55	29.1	2.9	0.5	B (2)
DLVEI-DP	M8017	1.0	1.5	23.0	1.6	1.0	A
DLVJ1	M8043	1.0	0.25	8.0	1.0	1.0	B
DMV11-M	M8053	3.4	0.4	21.8	2.0	1.0	A
DMV11-AP	M8053-MA	3.4	0.38	21.6	2.0	1.0	B
DMV11-BP	M8053-MA	3.4	0.38	21.6	2.0	1.0	A
DMV11-CP	M8064-MA	3.35	0.26	19.9	2.0	1.0	B
DMV11-FP	M8053-MA	3.4	0.38	21.6	2.0	1.0	A (2)
DMV11-N	M8064	3.4	0.4	21.8	2.0	1.0	A
DPV11	M8020	1.2	0.3	9.6	1.0	1.0	A
DUV11-DP	M7951	1.2	0.39	10.7	3.0	1.0	A (2)
DZV11	M7957	1.2	0.39	10.7	3.9	1.0	B
KDJ11-BB	M8190	5.5	0.1	28.7	2.3	1.1	–
KDJ11-BC	M8190	5.5	0.1	28.7	2.3	1.1	–
KDJ11-BF	M8190	5.5	0.2	29.9	2.6	1.0	–
KWV11-C[2]	M4002	2.2	0.013	11.2	1.0	1.0	–
LPV11	M8027	0.8	0.0	4.0	1.4	1.0	A
MRV11-D[3]	M7942	1.6	0.0	8.0	3.0	0.5	–
MRV11-D	M7942	2.8	0.0	14.0	1.8	1.0	–
MSV11-JD	M8637-D	3.74	0.0	18.7	2.7	0.5	–
MSV11-JE	M8637-E	4.1	0.0	20.5	2.7	0.5	–
MSV11-PK	M8067-K	3.45	0.0	17.25	2.0	1.0	–
MSV11-PL	M8067-L	3.6	0.0	17.5	2.0	1.0	–
MSV11-QA	M7551-AA	2.4	0.0	12.0	2.0	1.0	–
MSV11-QB	M7551-BA	2.3	0.0	11.5	2.0	1.0	–
MSV11-QC	M7551-CA	2.5	0.0	12.5	2.0	1.0	–
RC25	–	1.0	2.5	35.0	–	–	–
RD33	–	0.9	1.0	15.7	–	–	–
RD51	–	1.0	1.6	24.2	–	–	–

[1]A = 2.5 cm x 10.0 cm (1 in x 4 in)
B = 5.0 cm x 7.5 cm (2 in x 3 in)

[2]Usually connected through a universal data input panel (UDIP), using a 13.13-cm (5.25-in) mass storage slot

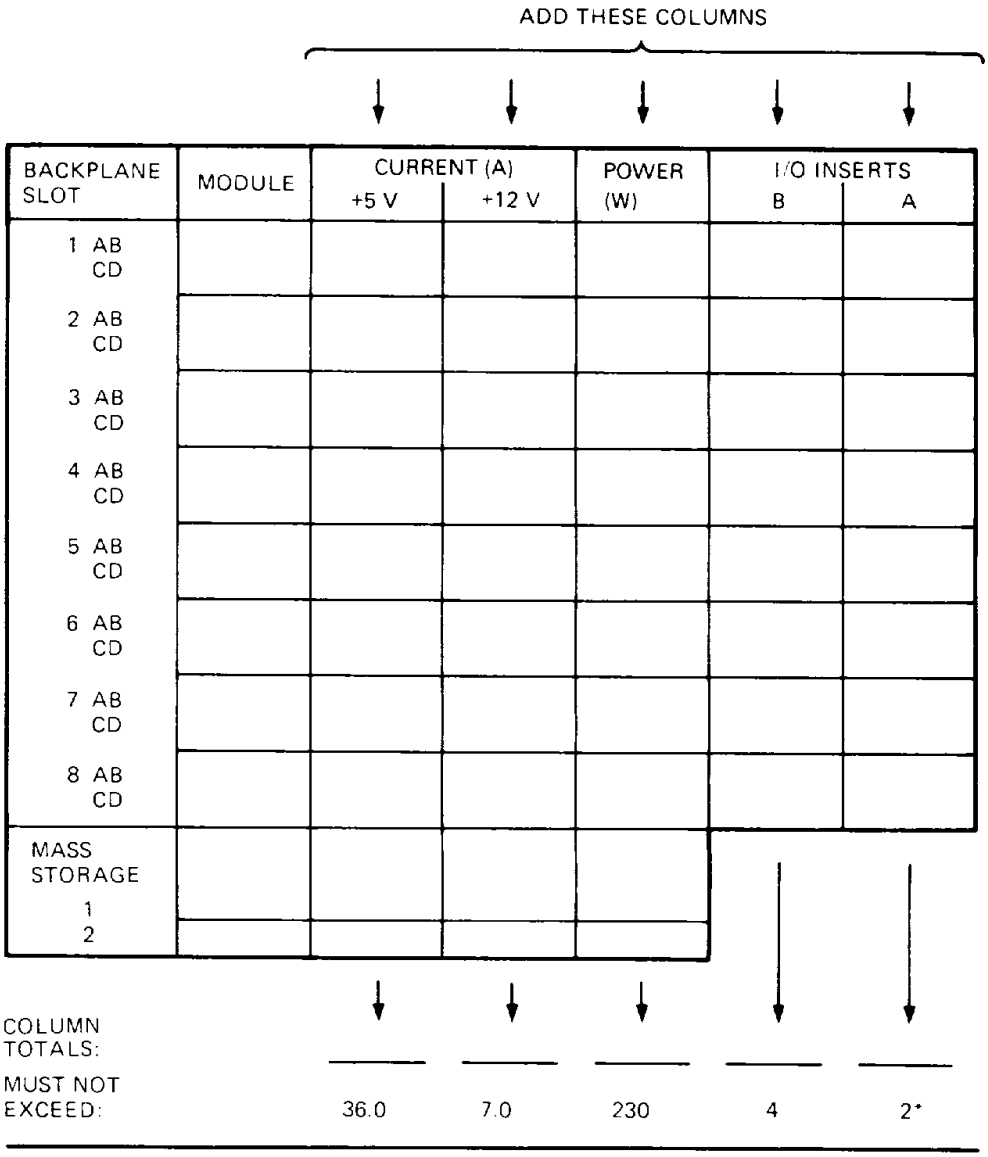
[3]Unpopulated module

Table 2–3 (Cont.): Power, Bus Load, and I/O Insert Data (BA23, BA123)

Option	Module	Current (Amps) +5 V	Current (Amps) +12 V	Power Watts	Bus Loads AC	Bus Loads DC	Insert[1]
RD52	–	1.0	2.5	35.0	–	–	–
RD53	–	0.9	2.5	34.5	–	–	–
RD54	–	1.3	1.34	23.7	–	–	–
RD54A–EA	–	1.3	1.34	22.6	–	–	–
RLV12–AP	M8061	5.0	0.10	26.2	2.7	1.0	A
RQDX1	M8639–YA	6.4	0.25	35.0	2.0	1.0	–
RQDX2	M8639–YB	6.4	0.1	33.2	2.0	1.0	–
RQDX3	M7555	2.48	0.06	13.2	1.0	1.0	–
RQDXE	M7513	0.5	0.0	2.5	1.0	0.0	–
RX33	–	0.5	0.3	5.6	–	–	–
RX50	–	0.85	1.8	25.9	–	–	–
TK50	–	1.35	2.4	33.55	–	–	–
TK50–AA	–	1.35	2.4	34.5	–	–	–
TK50E–EA	–	1.35	2.4	35.6	–	–	–
TQK25–KA	M7605	4.0	–	20.0	2.0	1.0	A
TQK50	M7546	2.9	0.0	14.5	2.8	0.5	–
TSV05	M7196	6.5	0.0	32.5	3.0	1.0	A

[1]A = 2.5 cm x 10.0 cm (1 in x 4 in)
B = 5.0 cm x 7.5 cm (2 in x 3 in)

Figure 2–1: BA23 Enclosure Worksheet



*IF MORE THAN TWO TYPE-A FILTER CONNECTORS ARE REQUIRED, AN ADAPTER TEMPLATE (PN 74-27740-01) MAY BE USED. THE ADAPTER ALLOWS THREE ADDITIONAL TYPE-A FILTER CONNECTORS, BUT REDUCES THE AVAILABLE TYPE-B CUTOUTS TO TWO.

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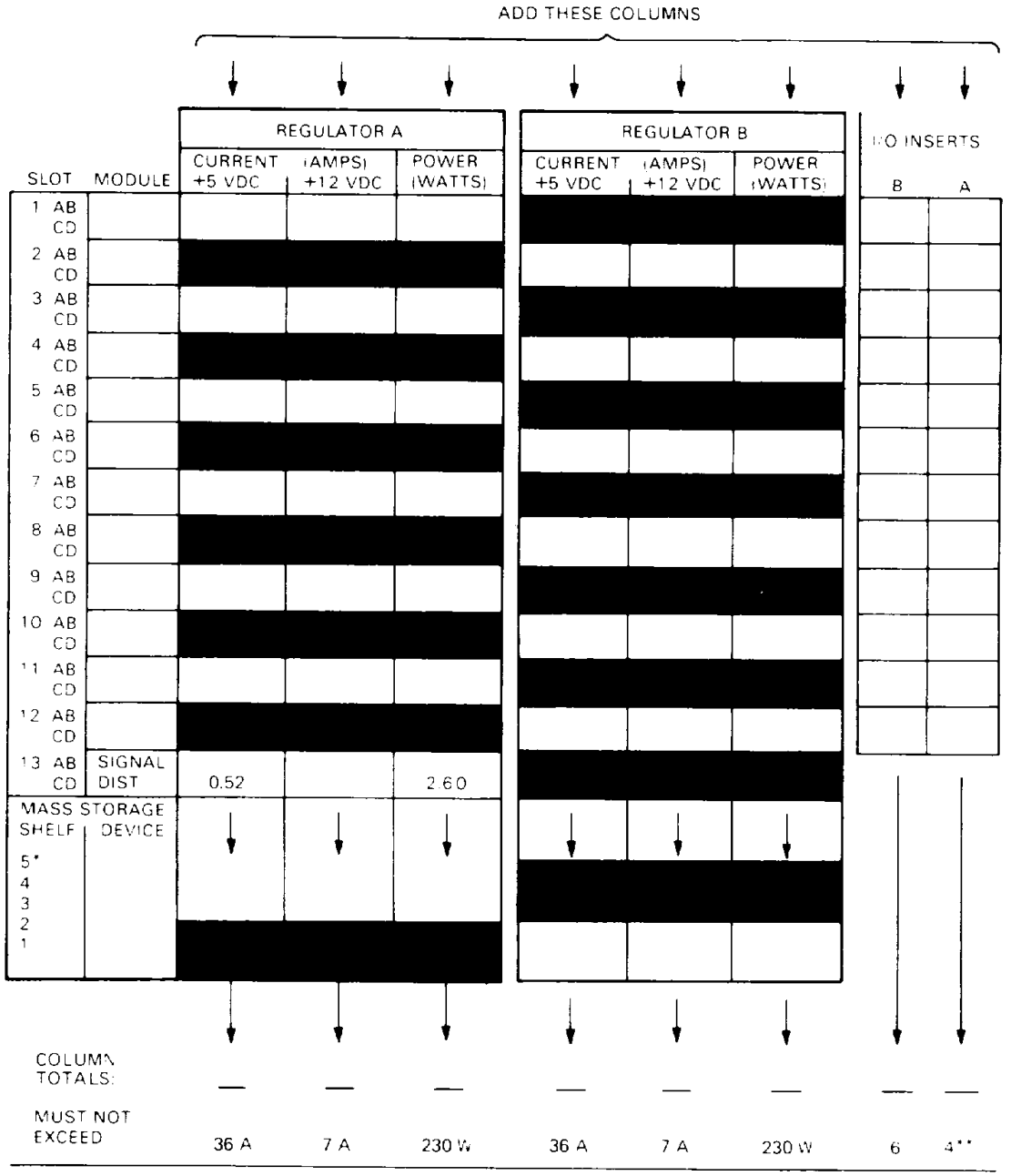
Figure 2–2: BA123 Enclosure Worksheet



*RECOMMENDED FOUR DRIVES MAXIMUM: TWO IN SHELVES 1 AND 2, TWO IN SHELVES 3, 4, OR 5.

**IF MORE THAN FOUR 1 X 4 I/O INSERTS ARE REQUIRED, AN ADAPTER TEMPLATE MAY BE USED.

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Figure 2–3: H9642–J Cabinet Worksheet

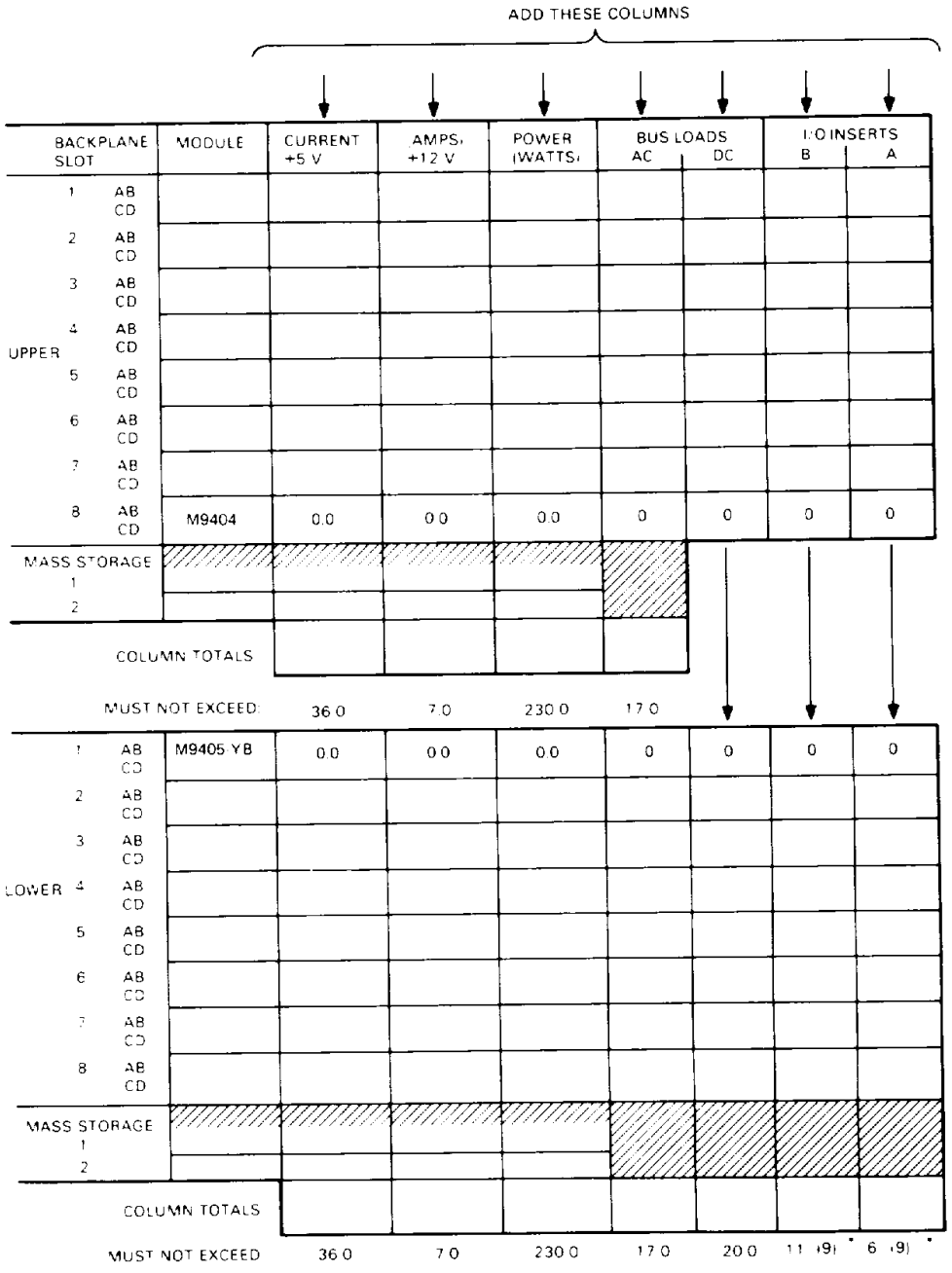

Figure 2–4: BA200-Series Enclosure Worksheet

12 SLOT ENCLOSURE

RIGHT-HALF POWER SUPPLY						
SLOT (ABCD)	MODULE	CURRENT 5 V	AMPS 12 V	POWER (WATTS)	BUS LOADS AC	BUS LOADS DC
1						
2						
3						
4						
5						
6						
MASS STORAGE TAPE 1					0.0	0.0
DISK 1					0.0	0.0
TOTAL RIGHT-HALF POWER SUPPLY					—	—
MUST NOT EXCEED		33.0	7.0	230.0 *	—	—
LEFT-HALF POWER SUPPLY					—	—
SLOT (ABCD)	MODULE	CURRENT 5 V	AMPS 12 V	POWER (WATTS)	—	—
7						
8						
9						
10						
11						
12						
MASS STORAGE DISK					0.0	0.0
DISK					0.0	0.0
DISK					0.0	0.0
TOTAL LEFT-HALF POWER SUPPLY						
MUST NOT EXCEED		33.0	7.0	230.0 *		
TOTAL BUS LOADS						
MUST NOT EXCEED					35.0	20.0

6 SLOT ENCLOSURE

POWER SUPPLY						
SLOT (ABCD)	MODULE	CURRENT 5 V	AMPS 12 V	POWER (WATTS)	BUS LOADS AC	BUS LOADS DC
1						
2						
3						
4						
5						
6						
TOTAL POWER SUPPLY					—	—
MUST NOT EXCEED		33.0	7.0	230.0 *	—	—
TOTAL BUS LOADS						
MUST NOT EXCEED					35.0	20.0

* NOTE: POWER SUPPLIES MAY DIFFER. CHECK YOUR POWER SUPPLY SPECIFICATIONS TO CONFIRM THE MAXIMUM WATTAGE.

MLO-001487

Chapter 3
Troubleshooting

3.1 Overview

This chapter describes the KDJ11–B CPU power-up self-test procedure and error messages, and the console emulator mode and octal debugging technique (ODT).

NOTE: *The XXDP V2 diagnostic monitor is described in the XXDP User's Manual.*

Read the Troubleshooting section of the customer documentation before using this chapter. Many apparent system problems have simple causes, such as incorrect external cabling or monitor settings. Always check for obvious problems before troubleshooting the system.

The KDJ11–B CPU and most option modules run self-tests when you power up the system. A module self-test can detect hard or repeatable errors, but not intermittent errors.

The LEDs on the module indicate test results. A successful module self-test does not guarantee that the module is performing correctly, because the test checks the controller logic only. The test does not check the module's Q22-bus interface, line drivers and receivers, or connector pins. An unsuccessful module self-test is accurate; the test does not require any other part of the system to be working.

Refer to *Microsystems Options* for a description of self-tests for individual modules. For detailed information, including the contents of the command status register (CSR) of the module's Q22-bus interface, see the user's guide for the module.

3.2 General Procedures

System problems are generally of two types:

- The system fails to boot (Section 3.2.1).
- The system boots, but a device in the system fails (Section 3.2.2).

You should ask two questions before troubleshooting any problem:

- Has the system been used before, and did it work correctly?
- Have changes been made to the system recently?

Two common problems occur when you make a change to the system:

- Cabling is incorrect.
- Module configuration errors (incorrect CSR addresses and interrupt vectors) are introduced.

When you troubleshoot problems, note the status of cables and connectors before you perform each step. Since cables are not always keyed, you can easily install them backward, or into the wrong connector. Label cables before you disconnect them, to prevent introducing new problems that make it more difficult to diagnose the original problem.

3.2.1 System Fails To Boot

The KDJ11–B CPU module self-tests are described in Section 3.3. If the system fails (or appears to fail) to boot the operating system, load and boot the XXDP diagnostic monitor.

If you cannot boot XXDP V2, do the following:

- Check the console terminal screen for an error message. Error messages are listed in Section 3.3.1.
- If no error message appears, make sure the on/off power switches on the console terminal and the system are set to on (1). Check the DC OK light on both, if applicable.
- Check the cabling to the console terminal.
- Check the hex display on the CPU I/O panel. If the display does not light, check the CPU module's LEDs and the CPU cabling. If a hex error message appears (F through 1) on the I/O panel or the module, see Section 3.3.1.
- If the console terminal remains off, check the power supply and power supply cabling.

If you can boot XXDP V2, and the system passes all tests, then the fault may be in the operating system.

3.2.2 System Boots, but Device Fails

If the system boots successfully, but a device seems to fail or an intermittent failure occurs, run the XXDP diagnostic monitor to isolate the failure to an FRU. The failing device is usually in one of the following areas:

CPU
Memory
Mass storage
Communications devices

Here are some common indications of an intermittent or device-specific problem:

- Operating system error messages appear at power-up for a particular communications device.
- Periodic operating system error messages indicate that a device is not present or cannot be found.
- Periodic data loss or scrambled data occur on one or more communications lines.
- Attached devices either do not work, or work incorrectly.
- The system cannot communicate with another computer.

3.3 KDJ11–B Self-Test

The KDJ11–B CPU is configured at the factory for automatic self-test and boot mode. The self-test is stored in boot ROMs, and runs each time the system is turned on or restarted. The self-test performs tests on the following:

- CPU
- Memory
- Connections between both CPU and memory modules and the Q22-bus

The self-test first tests a small portion of the CPU module, then progressively tests the rest of the system. The system enters automatic boot mode (Section 1.5) upon successful completion of the self-test. If the self-test discovers an error or failure, the system displays a message (Section 3.3.1).

The self-test program contains 40 separate parts, beginning with test 77 octal and counting down to 30 octal. The serial line unit (SLU) panel displays the number of the current self-test. The SLU panel also displays boot messages (27 to 00 octal). Table 3–1 lists the messages and describes the tests.

Table 3–1: KDJ11–B Self-Tests

Test	Description
77	CPU hung or Halt switch on at power-up or restart.
76	CPU pretests, then memory management unit (MMU) register tests.
75	Turns on MMU. Runs MMU tests and CPU tests.
74	Not used.
73	Powers up to octal debugging technique (ODT).
72	Powers up to 24/26.
71	EEPROM checksum test.
70	CPU ROM and page addressing test.
67	Miscellaneous CPU and extended instruction set (EIS) tests.
66	SLU 1. Checks all four registers.
65	SLU 2. Checks receivers and transmitters in maintenance mode.
64	SLU 3. Checks interrupts and errors in maintenance mode.
63	Test MMU abort logic.
62	Standalone CPU cache mode tests (memory off).
61	Line clock test.
60	Floating point processor (FPP).
57	CPU commercial instruction set (CIS) test.
56	Standalone mode exit. Checks address 1776000 for guaranteed timeout.
55	Not used.
54	Memory sizing test.
53	Checks for memory at address 0.
52	Tests memory from 0 to 4K words.
51	Cache test using memory.
50	Memory data byte tests for all memory.
47	Parity and error correction code (ECC) for all memory.
46	Memory address line shorts for all memory.
45 to 31	Not used.
30	Test exit. Test completed successfully.
27	Not used.
26	Not used.
25	Not used.
24	DECnet boot (DLV11–E/F or DUV11) waiting for a reply from host.
23	XON not received after XOFF. To correct, enter CTRL/Q.
22	XMIT ready bit never sets in DLART transmit CSR.

Table 3–1 (Cont.): KDJ11–B Self-Tests

Test	Description
21	Drive error.
20	Controller error.
17	Boot device selection invalid (for example, AA).
16	Invalid unit number.
15	Nonexistent drive.
14	Nonexistent controller.
13	No tape.
12	No disk.
11	Invalid boot block.
10	Drive not ready.
07	For Q-bus only. No bootable device found in automatic boot mode.
06	Console disabled by switch 1 = on and no force dialog. For V6.0 only, APT break received and ROM code entered ODT.
05	Not used.
04	Dialog mode.
03	Off-board ROM boot in progress.
02	EEPROM boot in progress.
01	CPU ROM boot in progress.
00	Control transferred from ROM code to booted device. The display goes blank when it receives a code of 00.

3.3.1 Self-Test Messages

Table 3–2 lists and describes the self-test boot and diagnostic ROM messages.

Table 3–2: KDJ11–B Self-Test Boot and Diagnostic ROM Messages

Error Number	Probable FRU Failure
177 to 100	(Subtract 100, and refer to the codes below.)
77	Halt switch; CPU; power supply.
73	Not a failure. Selected mode is ODT.
61	Clock from power supply.
54, 53, 52, 50, 47, and 46	Memory module.
23	Console terminal not ready due to XOFF received from terminal while attempting to print a message.
Any other number	CPU.

Before removing and replacing the recommended FRU, boot from the XXDP diagnostic monitor and verify the fault. To boot from XXDP V2, you must restart the built-in diagnostics after the test that found the error. Use the following procedure:

1. Remove all removable media containing user data.
2. Write-protect all other on-line data storage devices (devices containing fixed media).

   NOTE: *Restart testing after the test that found the fault only when you are attempting to boot write-protected media containing software diagnostics. In this case, write-protect all other on-line data storage devices to prevent possible data loss.*

3. Install the bootable diagnostic.
4. Enter CTRL/O followed by a 4, then press RETURN to restart the testing. This procedure restarts the built-in diagnostics.

If this restart procedure fails, you cannot load the diagnostic diskettes to verify the error and the failing FRU. In this case, replace the FRU recommended in Table 3–2.

3.3.2 Self-Test Console Terminal Messages

If any part of the self-test or boot diagnostics fail, the system normally displays a message in three locations:

- On the console terminal
- On the KDJ11–B LEDs
- On the SLU panel

The console terminal messages follow this format, usually displayed on two screens:

```
Testing in progress - Please wait.
Memory size is 256 Kbytes
9 step memory test
Step 1 2 3 4 5 6 7 8 9

Error 46
Memory CSR Error

See troubleshooting documentation.

Error PC = 173436   Page = 15   Program listing address = 015436

R0 = 060000   R1 = 052525   R2 = 172100   R3 = 172344
R4 = 100000   R5 = 040000   R6 = 172300   PAR3 = 010000
```

```
Command     Description

1           Rerun test
2           Loop on test
3           Map memory and I/O page
4           Advance to the next test

Type a command then press the Return key:
```

These messages contain the following information:

1. An error number (error 46 in this example). This is the number of the self-test that failed and is typically an octal number from 30 to 77. Sometimes the system displays an octal number from 130 to 177. The system displays this exception when an **unexpected trap to location xxx** error occurs. In this case, the failing self-test is the number minus 100.
2. A one-line description of the error (memory CSR error in this example).
3. A message to refer to the troubleshooting documentation.
4. The address of the error. This address information locates the error to the ROM address itself and the address in the program listing.
5. The contents of R0 to R6 of register set 0 and the contents of kernel PAR 3.
6. For some memory tests, the system displays expected data, found data (that is, faulty data), and any faulty memory address.
7. A command line with up to four user-selectable options that show how to continue the system testing. These options include:
   - **Rerun test**. Rerun the test once and, if it passes, continue with the remaining tests.
   - **Loop on test**. Run a continuous loop on the failing test. To stop this loop, enter CTRL/C. When the loop stops, the system displays the number of successful passes and number of error passes.
   - **Map memory and I/O page**. Available for tests 56 to 30. Helps locate a misconfigured or failing memory module.
   - **Advance to the next test**. Allows you to restart the system testing after the failing test.

NOTE: *Use the "advance to the next test" command only when attempting to boot write-protected media containing software diagnostics. Write-protect all other on-line data storage to prevent possible loss.*

If the system does not display this command, enter CTRL/O *followed by 4; then press* RETURN.

3.4 Console Emulator Mode

Some errors cause the system to halt any type of program. In this case, control passes to the console emulator mode. This mode allows you to simulate error conditions using the octal debugging technique (ODT).

The system enters console emulator mode when one of the following occurs:

- The program executes a halt instruction.
- You press the Halt button on the control panel.

Console emulator mode replaces the use of control switches and indicators for communicating directly with the system. When you type commands, the system displays responses on the console terminal instead of lighting indicators on the control panel.

When the system halts, it enters console emulator mode and displays the following:

```
nnnnnn
@
```

The number nnnnnn is the contents of PC (R7), and @ is the ODT prompt character. You can examine or modify the contents of the registers and memory by entering ODT commands (Section 3.5).

A portion of the microcode on the KDJ11–B module emulates the capability normally found on a programmer's console. The CPU interprets streams of ASCII characters from the console terminal as console commands. The micro-ODT accepts 18-bit addresses, allowing it to access 248 Kbytes of memory and the 8-Kbyte I/O page.

3.5 Octal Debugging Technique (ODT)

The octal debugging technique (ODT) functions only when the system is in console emulator mode. ODT consists of a group of commands and routines for finding error conditions and for simple communication with the system. ODT helps you interactively debug binary programs that reside in memory. When using ODT commands, express all addresses, registers, and memory location contents in octal. Letters and symbols make up the command set for ODT.

The hardware ODT commands are a subset of commands within a larger ODT program. The hardware program, which resides on the KDJ11–B module, is intended primarily for diagnosis of hardware problems. The system's response to ODT commands helps trace events that occur in the system.

Table 3–3 lists the basic ODT commands for the KDJ11–B CPU module.

Table 3–3: KDJ11–B Console ODT Commands

Command	Symbol	Function
Forward slash	/	Prints the contents of a specified register or memory location.
Carriage return	<CR>	Closes an open location.
Line feed	<LF>	Closes an open location and opens the next contiguous location.
Internal register designator	$ or R	Used with forward slash (/) to open a specified CPU register.
Processor status word designator	S	Used with forward slash (/) to open the CPU's processor status PS register, R6; must follow a $ or R command.
Go	G	Starts program execution at a specified address.
Proceed	P	Resumes execution of a program.
Binary dump	CTRL/S	Manufacturing use only.
(Reserved)	H	Reserved for future use.

For more information on ODT commands, see *KDJ11–BA CPU Module User's Guide.*

Appendix A
ROM Differences

A.1 Introduction

The KDJ11–B CPU modules (M8190) ship with an enhancement to the ROM code. The newest ROMs are Version 8.0 (V8.0); they upgrade V7.0 and V6.0.

You can check to make sure of the version of the existing KDJ11–B. When you enter setup mode from dialog mode, the system displays the version of the ROM code in the upper right corner of the screen.

Table A–1 lists the ROM versions and the DIGITAL part numbers. Section A.2 describes the differences between the V7.0 and V6.0 ROMs. Section A.3 explains the V8.0 ROMs.

Table A–1: KDJ11–B CPU ROM Part Numbers

Socket Location on CPU (M8190)	V8.0	V7.0	V6.0
E116 (low byte)	23–168E5	23–116E5	23–077E5
E117 (high byte)	23–169E5	23–117E5	23–078E5

A.2 V7.0 and V6.0 ROM Differences

The differences between the V7.0 and V6.0 ROMs on the KDJ11–B CPU EPROMS are as follows:

Boot Support for Tape Devices (TK50)

V7.0 contains a built-in tape mass storage control protocol (MSCP) boot program for the TK50. The device name is MU.

V6.0 does not contain this feature.

Disable Setup Mode Parameter

V7.0 adds setup mode parameter P to setup command 2. Parameter P allows you to disable entry into setup mode if you do not select force dialog mode. This feature prevents unauthorized entry into setup mode.

This change assumes that the force dialog switch is controlled, or that switch 5 on the KDJ11–B CPU is on to prevent unauthorized access to setup mode. When setup mode is disabled and the ROM code is in dialog mode, all references to the setup command are eliminated. If you type SETUP, the ROM code displays an error message.

In V6.0, you can always enter setup mode from dialog mode.

Disable All Testing Parameter

V7.0 adds setup mode parameter Q to setup command 2. Parameter Q disables all memory and cache testing if you do not select force dialog. Force dialog causes all testing to run.

V6.0 does not contain this feature.

Edit or Create Command

In the V7.0 setup mode edit or create command (setup command 13) for EEPROM boots, the highest unit number entry is decimal.

In V6.0, you must type an octal number that then converts to a decimal value.

Disk MSCP Autoboot Routine

In V7.0 MSCP autoboot, the boot program tries to boot removable media from units 0 to 255, then tries fixed-media units from 0 to 255.

The boot program attempts to boot each unit using the standard disk MSCP address. If this fails, the program attempts to boot the same unit number using the first floating MSCP device (if present) before continuing to the next unit number. The first floating MSCP address is 17760334 if there are no floating devices from 17760010 to 17760330.

In V6.0 MSCP autoboot, the boot program tries to boot removable media from units 0 to 7, then tries fixed-media units 0 to 7. The program tries only drives connected to the controller at the standard disk MSCP address (17772150).

Disk MSCP Boot Differences

In the V7.0 dialog mode BOOT command, the ROM code automatically tries the first floating controller if the standard controller reports an error. If an error exists on both controllers, the system displays an error message for each controller. The system does not display error messages unless the unit is not present on both controllers. If the second controller does not exist at the proper floating address, the ROM code displays only messages associated with the standard controller.

If you use the translation table or the /A switch, the ROM code tries only one controller regardless of the existence of two or more controllers.

In the V6.0 dialog mode boot command, the ROM code tries the standard controller only. The system displays an error message if the unit is not present on the standard controller.

In V6.0, a floating controller can boot MSCP devices under software control.

Initialize Setup Table

In V7.0, setup command 8 sets the PMG count value to 7. In V6.0, setup command 8 sets the PMG count value to 0.

NOTE: *The recommended value for the PMG count is 7 for all KDJ11-B CPUs.*

Memory Testing

In V7.0, all consecutive memory starting from location 0 is written at least once at power-up, unless all testing has been disabled.

In V6.0, memory above 248 Kbytes cannot be written if the long memory test is disabled or if you enter CTRL/C.

Power-Up Set to 3 with Battery Backed-up Memory

In V7.0, if you select mode 3 at power-up, the battery indicates that the voltages are lost and the Ignore Battery function is not set. Execute the restart mode selection if it is not mode 3. Otherwise, go to dialog mode.

In V6.0, if you select mode 3 at power-up, the battery indicates that the voltages are lost, and the Ignore Battery function is not set. Go to dialog mode regardless of the restart mode selection.

Enabling Halt-on-Break

In V7.0, the halt-on-break bit is set immediately after the `Testing in progress - Please wait` message is displayed. Since halt-on-break is generally enabled only in a single-user environment, this feature was not needed and has been removed. This change allows the ROM code to ignore the break that often comes from certain terminals when they are powered up. In V6.0, the halt-on-break bit in the BCSR is not enabled until one of the following occurs:

- One break is received and discarded.
- Any valid character is received except XON.
- The ROM code gives up control of the CPU.

CTRL/R and CTRL/U Echoing

V7.0 does not echo the CTRL/R and CTRL/U commands. V6.0 echoes these commands as ^R and ^U.

Setup Mode Command 5

Setup mode command 5 was deleted in V7.0. If you enter command 5, it is ignored.

In V6.0, setup command 5 (List or Change Terminal Setup Message) allows you to specify an octal message of up to ten characters to be sent to the console terminal. Use this command if the console terminal does not power up with the current language characters.

Automatic Boot Sequence Message

In V7.0, if you select autoboot mode, the ROM code prints a message when the autoboot boot sequence starts. The following message indicates that all tests are complete, that the ROM code is starting the autoboot sequence, and the name and unit number of the device booted:

```
Testing in progress - Please wait.
Memory size is 512 Kbytes
9 step memory test
Step 1 2 3 4 5 6 7 8 9
Starting automatic boot
Starting system from DU0
```

Addition to Boot Command List

In V7.0, L was added to the boot command list. Typing L causes the automatic boot sequence to continuously loop until one of the selected devices boots. Normally, the last device in the autoboot table is followed by an E, which terminates the table.

If no devices are bootable, the ROM code prints an error message and requests input before proceeding. The ROM code continuously tries every device in the table until one boots or until you enter CTRL/C.

V6.0 ROMs do not contain this feature, but you can implement it by writing a small EEPROM boot.

A.3 V8.0 ROMs

The V8.0 ROMs on the KDJ11–B CPU EPROMS contain the following changes:

RQDX3 Small Memory Automatic Boot Problem

In the MSCP INITIALIZE sequence, V7.0 checks to ensure that the disk controller starts step 1 within 100 msec of a hard initialize command. This is not true of many RQDX3 controller modules at power-up. The problem happens in small memory systems (less than 1 Mbyte) and on large memory systems if some of the memory tests are bypassed. The problem occurs at power-up only.

As in V6.0, V8.0 allows at least 10 seconds for step 1 to start.

RA-Series Disk Spin-Up Time Delay for Automatic Boot

In V6.0 and V7.0, the disk MSCP bootstrap assumes accurate off-line error codes from the disk being booted. If the disk is an RA-series on a KDA controller, and if the disk is spinning up or down, it can incorrectly identify a disk spinning up as being off line (not available). This causes the ROM code to skip this unit and try another, even though there is no problem.

V8.0 corrects this problem. The device promptly reports any errors if they occur. Some RA-series devices work adequately without this change.

CAUTION: *When you configure a system with MSCP devices, the wait loop in V8.0 delays the automatic boot process for 60 seconds or more. This is especially true when you boot fixed-media devices, since the disk automatic boot ignores fixed-media devices until it has tried all removable media devices.*

Using setup command 4, remove A (disk MSCP automatic boot) from the boot table in the EEPROM. Replace A with the desired order of devices to be booted (for example, DU0 and DU2). Remember that the disk automatic boot tries each unit at the standard controller address and then at the first floating address. This is also true for individual unit numbers (for example, DU0 and DU2) unless the unit number is described in the translation table (setup command 3).

Addition of RESET Instruction

V8.0 executes a RESET instruction (bus reset) at the beginning of the code, after POK is asserted.

V6.0 and V7.0 do not include this instruction.

Addition of Setup Command 5

V8.0 adds a new setup command 5, similar to the setup command 5 in V6.0. Setup command 5 allows you to store up to 20 bytes of information in the EEPROM. However, the data stored in the EEPROM is not sent to the console, as it is in V6.0. You must enter the data in octal numbers, from 0 to 377.

Setup command 5 was deleted in V7.0.

Memory Test Coverage

V6.0 and V7.0 test only the first 4K words of memory when running test 50. V8.0 checks all available consecutive memory. Test 50 performs byte testing and checks two locations for floating ones and zeros.

List Command Device Descriptions

Some of the messages displayed during the V8.0 list command are new. The changes are listed in Table A–2.

Table A–2: List Command Device Messages

Message Type	V6.0 and V7.0 Messages	V8.0 Messages
DU	RD51, RD52, RC25, RA80, RA81, RA60	RDnn, RXnn, RC25, RAnn
XH	DECnet DEQNA	DECnet Ethernet

Manufacturing Test Loop

The manufacturing test loop in V7.0 does not execute all of the tests. V8.0 corrects this problem.

The manufacturing test loop in V6.0 works correctly.

Appendix B
Formatting RD- and RX-Series Disk Drives

B.1 Disk Formatting

Format an RD- or RX-series disk drive as follows:

CAUTION: *Do not format disks without first backing up the data. The disk formatting procedure destroys previous disk contents.*

1. Insert the formatter diskette or the tape cartridge into its drive. Press RETURN.
2. Type R ZRQx?? after the . (period) prompt; x is B for RQDX1 or RQDX2, C for RQDX3, and F for RX33. The question marks allow you to use any revision of the program. Press RETURN.

   NOTE: *When formatting an RD52 drive, make sure you have Version C0 or later. Earlier versions format the RD52 (31 Mbytes) as though it were an RD51 (11 Mbytes).*

   A prompt similar to the following appears on the terminal:

   ```
   DR>
   ```

3. To run the program, type START and press RETURN. The following dialog takes place:

   ```
   CHANGE HW (L)?
   ```

   Type N (no) and press RETURN.

   ```
   CHANGE SW (L)?
   ```

   Type N and press RETURN.

   ```
   ENTER DATE (in mm-dd-yy format) (A)
   ```

   Type the current date (for example, 11–15–88). Press RETURN.

   ```
   ENTER UNIT NUMBER TO FORMAT <0>
   ```

Type 0 for the first fixed-disk drive, or type 1 for the second. Press RETURN.

```
USE EXISTING BAD BLOCK INFORMATION?
```

Type Y (yes) and press RETURN. This activates the reformat mode (Section B.1.1).

NOTE: *The program requires about 12 minutes to format an RD51 and about 30 minutes to format an RD52 or RD53. Typing N (no) doubles the time required to format the disk drive.*

```
CONTINUE IF BAD BLOCK INFORMATION IS INACCESSIBLE?
```

Type Y and press RETURN.

```
ENTER A NON-ZERO SERIAL NUMBER:
```

Type your serial number (located on top of the disk drive) and press RETURN.

```
FORMAT BEGUN
```

After about 12 minutes, the system displays a completion message as follows:

```
FORMAT COMPLETED
```

If the formatting is not successful, the system displays a message when the error occurs (Section B.1.2). Remove the diskette or tape cartridge if the formatting has completed successfully.

B.1.1 Format Modes

The program can run three types of format modes: reformat, restore, or reconstruct, In order, the program asks you the following questions. Your answers determine the format mode that runs.

1. Use existing bad block information?
2. Down-line load?
3. Continue if bad block information is inaccessible?

The second question does not appear unless you answer N to the first question. Answering N to the third question causes the diagnostic program to stop and print a message if a problem is found.

The format modes operate as follows:

- **Reformat mode**. If you answer Y to question one, no further questions are asked. The format program reads the manufacturer's bad blocks from a block on the disk. It then formats the disk except for these bad

blocks. The process requires about 12 minutes. If the program fails, try restore mode.

- **Restore mode**. If you answer N to question one, the program asks you to type in a list of the bad blocks. It then formats the disk except for the bad blocks you specify. You can specify the bad blocks using the list that comes with the drive. The program asks you for the last eight digits of the serial number (found at the top of the disk drive). Restore mode requires about 15 minutes.
- **Reconstruct mode**. If you answer N to questions one and two, the program searches the disk and identifies the bad blocks. It does not use the manufacturer's bad block information. It then formats the disk except for the identified bad blocks. Reconstruct mode requires about 30 minutes.

B.1.2 Formatter Messages

Table B–1 lists the formatter messages, their probable causes, and actions to correct the problem. The first few errors can occur almost immediately. The remaining errors can occur from one minute to longer than ten minutes after the program starts.

Table B–1: MicroPDP–11 Formatter Messages

Message	Description/Action
Unit is not Winchester or cannot be selected.	Unit is either unavailable or is an RX-series diskette drive. Check to make sure the fixed-disk is not write-protected. Make sure the jumper on the disk drive is set correctly.
Initial failure accessing FCT.	The format control table (FCT) cannot be read. Try reconstruct mode (Section B.1.1).
Factory bad block information is inaccessible.	Occurs only in reformat mode. Run in reconstruct mode (Section B.1.1).
Seek failure during actual formatting.	There is a hardware error. Check for hardware problems.
Revector limit exceeded.	The disk is bad. Replace the disk.
RCT write failure.	Write to disk failed after successful formatting and surface analysis. Check write-protect status.
Failure closing FCTS.	Disk is marked as unformatted.

Appendix C
Related Documentation

The following documents contain information relating to MicroVAX or MicroPDP–11 systems.

Document Title	Order Number
Modules	
CXA16 Technical Manual	EK–CAB16–TM
CXY08 Technical Manual	EK–CXY08–TM
DEQNA Ethernet User's Guide	EK–DEQNA–UG
DHV11 Technical Manual	EK–DHV11–TM
DLV11–J User's Guide	EK–DLV1J–UG
DMV11 Synchronous Controller Technical Manual	EK–DMV11–TM
DMV11 Synchronous Controller User's Guide	EK–DMV11–UG
DPV11 Synchronous Controller Technical Manual	EK–DPV11–TM
DPV11 Synchronous Controller User's Guide	EK–DPV11–UG
DRV11–J Interface User's Manual	EK–DRV1J–UG
DRV11–WA General Purpose DMA User's Guide	EK–DRVWA–UG
DZQ11 Asynchronous Multiplexer Technical Manual	EK–DZQ11–TM
DZQ11 Asynchronous Multiplexer User's Guide	EK–DZQ11–UG
DZV11 Asynchronous Multiplexer Technical Manual	EK–DZV11–TM
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KDJ11–D/S CPU Module User's Guide	EK–KDJ1D–UG
KDJ11–B CPU Module User's Guide	EK–KDJ1B–UG
KDF11–BA CPU Module User's Guide	EK–KDFEB–UG
KMV11 Programmable Communications Controller User's Guide	EK–KMV11–UG
KMV11 Programmable Communications Controller Technical Manual	EK–KMV11–TM

Document Title	Order Number
Modules	
LSI–11 Analog System User's Guide	EK–AXV11–UG
Q-Bus DMA Analog System User's Guide	EK–AV11D–UG
RQDX2 Controller Module User's Guide	EK–RQDX2–UG
RQDX3 Controller Module User's Guide	EK–RQDX3–UG
Disk and Tape Drives	
RA60 Disk Drive Service Manual	EK–ORA60–SV
RA60 Disk Drive User's Guide	EK–ORA60–UG
RA81 Disk Drive Service Manual	EK–ORA81–SV
RA81 Disk Drive User's Guide	EK–ORA81–UG
SA482 Storage Array User's Guide (for RA82)	EK–SA482–UG
SA482 Storage Array Service Manual (for RA82)	EK–SA482–SV
RC25 Disk Subsystem User's Guide	EK–ORC25–UG
RC25 Disk Subsystem Pocket Service Guide	EK–ORC25–PS
RRD50 Subsystem Pocket Service Guide	EK–RRD50–PS
RRD50 Digital Disk Drive User's Guide	EK–RRD50–UG
RX33 Technical Description Manual	EK–RX33T–TM
RX50–D, –R Dual Flexible Disk Drive Subsystem Owner's Manual	EK–LEP01–OM
TK50 Tape Drive Subsystem User's Guide	EK–LEP05–UG
TS05 Tape Transport Pocket Service Guide	EK–TSV05–PS
TS05 Tape Transport Subsystem Technical Manual	EK–TSV05–TM
TS05 Tape Transport System User's Guide	EK–TSV05–UG

Document Title	Order Number
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MicroVAX Special Systems Maintenance	EK–181AA–MG
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Microsystems Options	EK–192AA–MG
Microsystems Site Preparation Guide	EK–O67AB–PG
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MicroVAX II Hardware Information Kit (for BA123)	00–ZNAAB–GZ
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VAXstation II/GPX Owner's Manual (BA123)	EK–105AA–OW

Document Title	Order Number
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DEC/X11 User's Manual	AC–FO53D–MC
XXDP User's Manual	AZ–GNJAA–MC
XXDP DEC/X11 Programming Card	EK–OXXDP–MC
MicroVAX Diagnostic Monitor Ethernet Server User's Guide	AA–FNTAC–DN
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MicroVAX Diagnostic Monitor User's Guide	AA–FM7AB–DN
Networks	
Ethernet Transceiver Tester User's Manual	EK–ETHTT–UG
VAX/VMS Networking Manual	AA–Y512C–TE
VAX NI Exerciser User's Guide	AA–HI06A–TE

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NOTES

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