KDJ11-B Processor Spec.

REVISION

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

Approval and Date	
Author:	Date:
Elect. Design Eng.:	Date:
Mech. Design Eng.:	Date:
Resp. Support Eng.:	Date:

Table of Contents

1.0 Introduction

1.1 Scope of Document

This specification documents the functional and environmental characteristics of the KDJ11-B CPU module.

1.2 Applicable Documents

The following reference material contains detailed information regarding the PDP-11 family, KDJ11-B module, and required environment.

J-11 Programmer's Reference
J-11 Chip System Specification
J-11 Control Chip Specification
J-11 Data Chip Specification
PDP-11/04/24/34a/44/70 Handbook

KDJ11-BA Boot and Diagnostic ROM Functional Specification
KDJ11-B DC350/394 Gate-Array Specification
KDJ11-B DC351 Gate-Array Specification
KTJ11-B Unibus Adapter Functional Specification
MSV11-J ECC Memory Engineering Specification

DEC STD 102 Environmental Specification
DEC STD 158 Unibus Specification
DEC STD 160 Q-Bus Specification

REVISION HISTORY

REV	DATE	REASON
0.1	01-Feb-82	Preliminary Spec: Sent out for review.
0.2	25-May-82	Updated specification to reflect the following changes: (1) Cache Response to Parity Errors revised and more clearly defined; (2) Architecture for Boot and Diagnostic Facility revised; and (3) Signetics DUART replaced with a single DLART, revising Console SLU functionality and eliminating second serial line. Refer to sections 6, 9 and 11.
0.3	04-Oct-82	Updated specification to improve the descriptions for "Red Stack Aborts" and to reflect the following changes to the Boot and Diagnostic CSR: (1) Stand-Alone Mode is now a read-write bit, allowing diagnostic reentry; (2) The Battery Backup Okay bit has been redefined as Battery Backup Reboot Enable; (3) On-board 50Hz and 800Hz have been added as selectable sources for the line clock and (4) the WRT BSY bit has been eliminated. Refer to sections 4.4.5, 4.6.3, 9.1.1 and 10.1.
0.4	25-Apr-83	Updated specification to correct errors in the Cache Control Register description in Section 6.2.
A	28-Jun-84	Updated section 9.3.3 and 9.3.4 to reflect changes in available ROM's and EPROM's. In section 11.2.1, RX Done is not cleared by Bus INIT. Sections 7.0 and 8.0 have been completed. CIS option has been deleted, module pinout has been completed, and spec has been reviewed for release.

2.0 General Description

The KDJ11-B is a quad height Q22-Bus PDP-11 which consist of a single KDJ11-B CPU Module. The KDJ11-B can also serve as a Unibus PDP-11 when used in conjunction with the KTJ11-B Unibus Adapter Module.

The KDJ11-B Module contains a Central Processor, Memory Management, Floating Point Instruction Set, Commercial Instruction Set (optional), an 8K byte cache, a line frequency clock, a Boot and Diagnostic Facility and a console serial line unit.

The KDJ11-B Module interfaces to the standard Q22-Bus, but also features the additional control signals necessary for communication via the PMI (Private Memory Interconnect) Protocol. This protocol allows high speed data transfers, including double word reads. The MSV11-J ECC Memory Module and the KTJ11-B Unibus Adapter Module are compatible with the KDJ11-B and can also communicate via the PMI protocol.

The KDJ11-B instruction set consists of the 11/70 base instruction set including the extended instruction set (EIS), plus the MTPS, MFPS, MFPT, CSM, TSTSET and WRTLCK instructions, as well as the floating point (FP11) instruction set compatible with the FP11-A/C/E/F floating point processors.

The KDJ11-B memory management is compatible with the 11/44 and features a 22-bit physical address, instruction/data (I/D) address spaces, and kernel/supervisor/user (K/S/U) addressing modes.

The processor (base instruction set and FP11 instruction set) and memory management functions are implemented on two custom CMOS chips, the Data chip and the Control chip. These are mounted on a 60(to 68) pin hybrid package (two die per side) measuring approximately 1.3" x 3.0". The Q22 bus interface on the module conforms to DEC standard 160.

The KDJ11-B is intended to run RT-11, RSX-11M, RSX-11M+, RSTS/E, DSM-11, UNIX, and other PDP-11 compatible operating systems.

The KDJ11-B contains hooks for a Floating Point Accelerator (FPA) Chip. However, the FPA Option will not be available when the initial KDJ11-B Modules are shipped and the presence of these hooks shall imply no commitment that the initial KDJ11-B Modules will actually support the FPA.

The KDJ11-B Boot and Diagnostic Facility features two sockets for ROM memory containing the boot and diagnostic programs. It also contains a third socket for EEPROM Memory containing the KDJ11-B Configuration Data plus space for customer loadable boot code. The Boot and Diagnostic ROM Programs included with the KDJ11-BA Processor Module are described briefly in section 9 of this document and more fully in the KDJ11-BA Boot and Diagnostic ROM Functional Specification.

3.0 Environmental and Electrical Specifications

3.1 Storage Conditions

THE KDJ11-B MODULE HAS AN AMBIENT STORAGE TEMPERATURE RANGE OF -40'C (-40'F) TO +65'C (149'F). STORAGE RELATIVE HUMIDITY IS 10% TO 90%, NON-CONDENSING, ALTITUDES TO 9.1 KM (50,000 FT).

3.2 OPERATING CONDITIONS

THE OPERATING TEMPERATURE FOR A KDJ11-B MODULE MOUNTED IN A box within a cabinet is 5'C (41'F) to 60'C (140'F) ambient at the module. The maximum outlet temperature rise allowed is 5'C (9'F) above 60'C (140'F). Derate maximum temperature by 1'C for each 1000 meters (1'F for each 1000 ft) of altitude. Operating relative humidity is 10% to 90%, non-condensing.

3.3 Power Consumption (Estimated)

The KDJ11-B CPU module power requirements are:

+5V +/- 5%	@	5.5 Amps max
	@	4.8 Amps typ
+12V +/- 5%	@	0.1 Amps max
	@	0.05 Amps typ

3.4 Module Pinouts

The KDJ11-B CPU module plugs into slot 1 of either a Q22/CD backplane or of a backplane specifically designed for the PMI Interconnect. The KDJ11-B is not compatible with Q22/Q22 or Q/Q backplanes. The AB row module pinouts are compatible with the Q22-bus specification (DEC standard 160). The SRUN L signal appears on pins AF1. The CD row module pinouts are compatible with the Private Memory Interconnect (PMI) defined for the interconnection of this module with the MSV11-J ECC Memory Module and the KTJ11-B Unibus Adapter Module.

Appendix 6 summarizes the module pinouts for the KDJ11-B module.

3.5 Mean Time Before Failure -- MTBF (Estimate)

	CLASS B (GROUND BENIGN)	CLASS C (GROUND FIXED)
KDJ11-B module	25000 hrs	15000 hrs

4.0 Processor Description

4.1 Processor Chip Description

The J-11 is a MOS/LSI chip set that implements a high performance PDP-11 processor with memory management, FP-11 floating point instructions. The chip set is composed of two different types of chips. The data chip contains the data path and relocation logic. The control chip, of which there are several different microprogramm versions, contains the microprogram sequencing logic and control sto

4.1.1 Data Chip

The Data Chip is composed of three major pieces: an Execution Unit (EU), a Memory Management Unit (MMU) and a Prefetch Mechanism. The Execution Unit contains the PDP-11 general purpose registers, eight scratch pad registers, the ALU, a shifter/swapper and shift register and necessary word/byte multiplexers. The Memory Management Unit contains the relocation registers, the relocation logic, the error status registers and the FP-11 floating point accumulators. The Prefetch Mechanism contains a copy of the PC, a relocated version of the PC, a prefetch buffer, and various status flags. The Data Chip performs all arithmetic and logic functions, handles all data and address transfers, including relocation, and operates most of the signals used for interchip communication and system timing.

4.1.2 Control Chip

The Control Chip contains the microprogram sequence logic as well as 1280 words of local microprogram storage consisting of both Programmed Logic Arrays (PLA) and Read-Only Memory (ROM). Architecturally, there are several major function blocks in the chip: the microstore array, the next address logic, the counter logic, the prefetch logic, the interrupt service logic, the abort service logic, the AIO code generator, the coprocessor support logic (for the floating point accelerator), and the state sequencer. During the course of a microcycle, the chip accesses the appropriate microinstruction from the microstore, sends it along to the external Micro-Instruction Bus (MIB-H) to the Data Chip for execution, and simultaneously generates the address for the next microinstruction to be accessed. Note that the control chip is responsible for accessing only its local storage.

Three different microprogrammed versions of the Control Chip are required to completely implement the J-11 macroinstruction set. The Base Control Chip emulates the basic PDP-11 instruction set, the extended instruction set (EIS), the FP-11 floating point instruction set and the console microcode (micro-ODT). It also provides the microcode hooks for the floating point accelerator (FPA).

4.1.3 The J-11 Hybrid Packages

The chips are packaged in 84-pin leadless carriers. The carriers are mounted on hybrid substrates in two configurations. The DCJ11-AA consists of a hybrid substrate with a Data Chip and a Base Control Chip mounted on the top. The DCJ11-BA consists of a hybrid substrate with a Data Chip and a Base Control Chip mounted on the top.

4.2 Instruction Set

The KDJ11-B instruction set consists of the following:

- 11/70 Base Instruction Set including the Extended Instruction set (EIS), plus the MTPS, MFPS, MFPT, CSM, TSTSET and WRTLCK instructions. Appendix 1 contains a complete list of the J-11 Base Instruction Set.

- Floating Point (FP11) Instruction Set compatible with the FP11-A/C/E/F floating point processors. Appendix 2 contains a complete list of the J11 floating point instructions.

4.2.1 PDP-11 Differences

Appendix 12 describes the differences between the KDJ11-B and all other PDP-11 processors.

4.2.2 MFPT Instruction

For all processors based on the J11 Chip Set, the Move From Processor Type (MFTP) Instruction loads a "5" into R0.

4.3 Instruction Timing (Estimates)

A memory fetch which results in a cache hit requires 200 nsec. memory fetch which results in a cache miss, and which accesses memory via PMI protocol requires 900 nsec to fetch two words. A memory write which accesses memory via PMI protocol requires 400 nsec.

4.3.1 Interrupt Latency (Estimates)

Interrupt latency is defined as the time between receiving an interrupt request (BIRQ L) and acknowledging (BIAK L) the request assuming MO DMA activity. The table below summarizes the latency calculations:

CONDITION	INSTRUCTION	LATENCY
worst case base instructions including EIS	ASHC	<10uS *
worst case base instructions excluding EIS	Traps	<10uS *
worst case FP11 instruction set	ABSD/NEGD	<20uS *

* 20 MHZ CPU

4.3.2 Interrupt Service Time (Estimate)

Interrupt service time is defined as the time between acknowledging the interrupt and fetching the first instruction of the service routine. The KDJ11-B service time is TBD (<10uS).

4.3.3 DMA Latency

DMA latency is defined as the time between receiving a DMA Request (BDMR L) and granting the request (BDMG L). The worst case DMA latency is TBD.

4.4 Processor Architectural Features

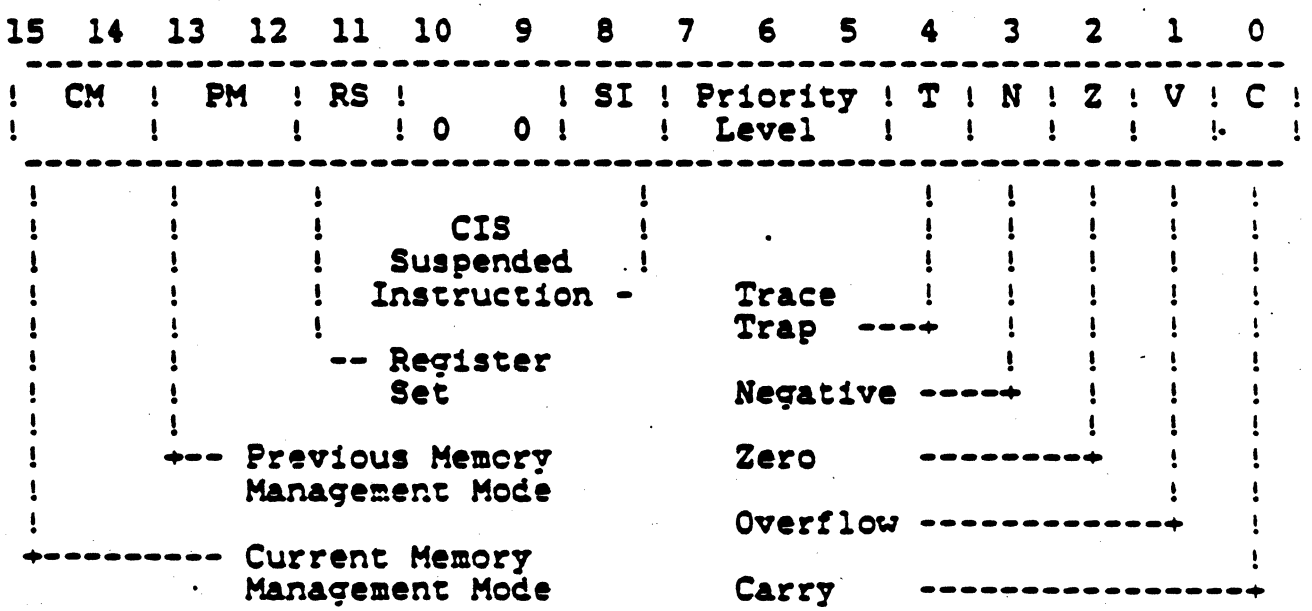
4.4.1 General Registers

These include:

- Two sets of six working registers (R0-R5)
- Kernel/supervisor/user stack pointers (R6)
- Program counter (R7).

4.4.2 Processor Status Word - PS (17 777 776)

The Processor Status Word (PS) contains information on the status of the processor.



BIT	NAME	FUNCTION
15:14	Current Mode (RW, protected)	Current processor mode: 00 = kernel 01 = supervisor 10 = illegal (traps) 11 = user.
13:12	Previous Mode (RW, protected)	Previous processor mode, same encoding as current mode.
11	Register Set (RW, protected)	General register set select: 0 = register set 0 1 = register set 1.
8	Suspended Instruction (R/W)	Set to indicate that a CIS instruction was suspended to service an interrupt.
7:5	Priority (RW, protected)	Processor interrupt priority level.
4	Trace Trap (RW, protected)	Set to force a trace trap.
3:0	Condition Codes (RW)	Processor condition codes.

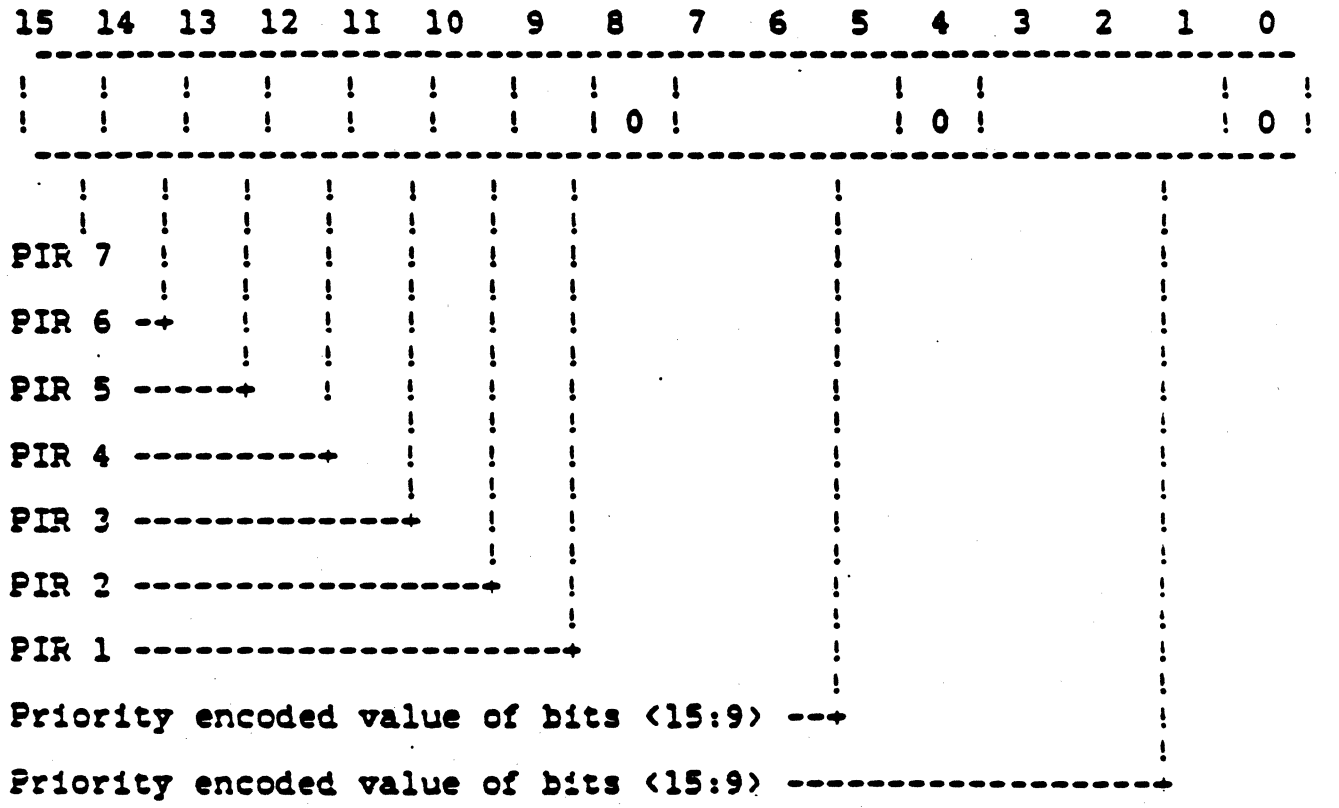
For the protection of the PS under various conditions, see the tables in section 3.2 of the J-11 Programmers Reference Specification. The PS is initialized at power up (depends on power up options) and is cleared at console start. The RESET instruction does not affect the PS.

4.4.3 Program Interrupt Request Register (Address: 17 777 772)

The Program Interrupt Request Register (PIRQ) implements a software interrupt facility.

A request is queued by setting one of the bits <15:9> which corresponds to a program interrupt request at levels 7 thru 1. Bits <7:5> and <3:1> are set by hardware to the encoded value of the highest pending request set.

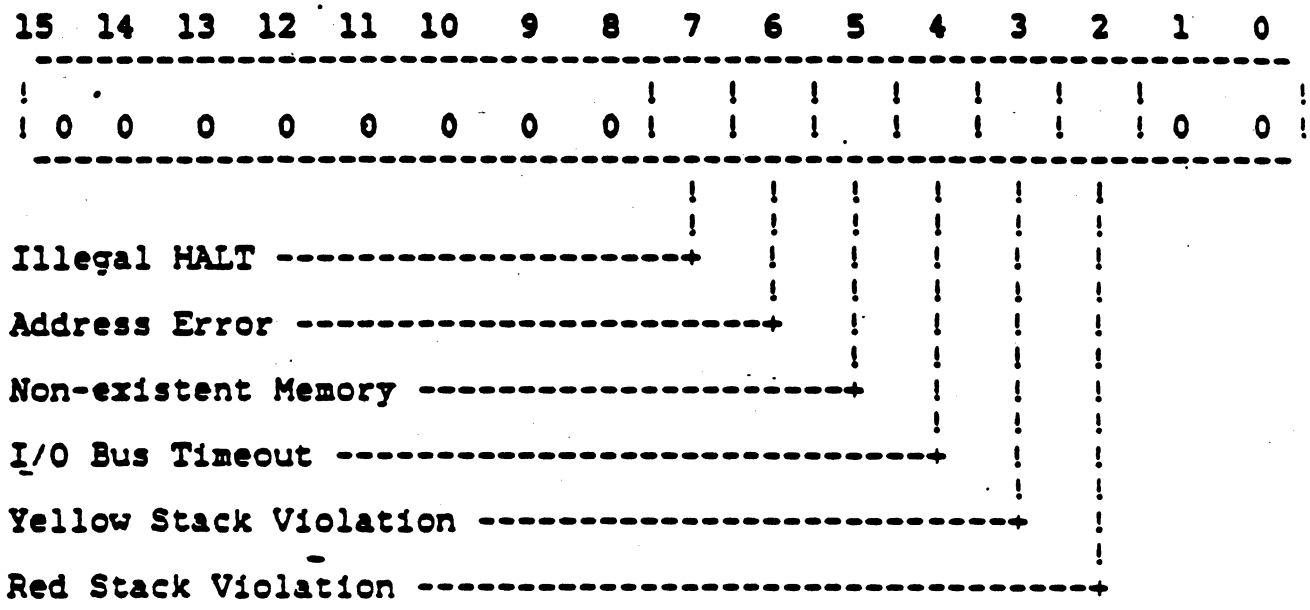
When the program interrupt request is granted, the processor traps through location 240. It is the interrupt service routine's responsibility to clear the appropriate bit in PIRQ before exiting.



PIRQ bits <15:9> are read/write, bits <7:5,3:1> are read-only and the remaining bits always read as zeroes. PIRQ is cleared at power up, by a console start and by the RESET instruction.

4.4.4 CPU Error Register (Address: 17 777 766)

This register identifies the source of any abort or trap that caused a trap through location 4.



BIT	NAME	FUNCTION
7	Illegal HALT	Set when execution of a HALT instruction is attempted in user or supervisor mode.
6	Address Error (RO)	Set when word access to an odd byte address or an instruction fetch from an internal register is attempted.
5	Non-existent Memory (RO)	Set when a reference to main memory times out.
4	I/O Bus Timeout (RO)	Set when a reference to the I/O page times out.
3	Yellow Stack Violation (RO)	Set on a yellow zone stack overflow trap.
2	Red Stack Violation (RO)	Set on a red zone stack overflow trap.

The CPU Error Register is cleared when it is written. It is also cleared at power up or by console start. It is unaffected by a RESET instruction.

4.4.5 Stack Limit Protection

The KDJ11-B checks kernel stack references against a fix limit of 400(8). If the virtual address of the stack reference less than 400(8), a yellow stack trap occurs at the end of the current instruction.

A stack trap can only occur in kernel mode and only on a stack reference, which is defined as a mode 4 or 5 reference through R6, or a JSR, trap, or interrupt stack push.

In addition, the J11 checks for kernel stack aborts during interrupt, trap, and abort sequences. If, during one of these sequences, a kernel stack push causes an abort, the J11 initiates a red zone stack trap by setting CPU Error Register bit <2>, loading virtual address 4 into the kernel stack pointer (R6) and trapping thru location 4 in kernel data space. The old PC and PS are saved in kernel data space locations 0 and 2 respectively.

NOTE: The J-11 treatment of yellow stack trap is identical to the 11/44. The 11/70 includes a stack limit register, and a more inclusive definition of stack reference. The J11's definition of a red stack trap is unique.

4.4.6 Kernel Protection

In order to protect the kernel operating system against interference, the KDJ11-B incorporates a number of protection mechanisms:

- In kernel mode, HALT, RESET, and SPL execute as specified In supervisor or user mode, HALT causes a trap through location 4, while RESET and SPL are treated as NOPs.

- In kernel mode, RTI and RTT can alter PS <15:11> and PS <7:5> freely. In supervisor or user mode, RTI and RTT can only set PS <15:11> and cannot alter PS <7:5>.

- In kernel mode, MTPS can alter PS <7:5>. In supervisor or user mode, MTPS cannot alter PS <7:5>.

- All trap and interrupt vector references are classified as kernel data space references, irrespective of the memory management mode at the time of the trap or interrupt.

- Kernel stack references are checked for stack overflow. Supervisor and user stack references are not checked.

4.5 Trap and Interrupt Service Priorities

In both traps and interrupts, the currently executing progra is interrupted and a new program, the starting address of which specified by the trap or interrupt vector, is executed. The hardware process for traps and interrupts through a vector V is identical:

```
PS --> temp 1                    !save PS, PC in temporaries
PC --> temp 2
0 --> PS <15:14>                 !force kernel mode

M[V] --> PC                      !fetch PC from vector, data space
M[V+2] --> PS                    !fetch PS from vector, data space
temp1<15:14> --> PS<13:12>       !set previous mode
SP-2 --> SP                      !selected by new PS
temp1 --> M[SP]                  !push old PS on stack, data space
SP-2 --> SP
temp2 --> M[SP]                  !push old PC on stack, data space
                                 !go execute next instruction
```

Note: If an abort occurs during either the vector fetch or the stack push, the PS and PC are restored to their original state (i.e. to the state prior to trap sequence execution).

The priority order for traps and interrupts is as follo

red stack trap
address error
memory management violation
timeout/non-existent memory
parity error
trace (T-bit) trap
yellow stack trap
power fail
floating point trap
PIRQ 7
interrupt level 7
PIRQ 6
interrupt level 6
PIRQ 5
interrupt level 5
PIRQ 4
interrupt level 4
PIRQ 3
PIRQ 2
PIRQ 1
halt line

Note: The halt line is given highest priority when the processor hangs up within most identified sunset loops. Refer to Section 4.5.1.

4.5.1 Sunset Loops

Any combination of the following sunset loops can all be exited by asserting the halt line:

Interrupts:

Parity error - will loop if parity vector has bad parity
Trace trap - will loop if trace vector has T-bit set
All PIRQs - will loop if PIRQ vector priority level does not block that level

Aborts:

Any abort that occurs during a vector sequence (reading a vector or pushing to the stack). These are NXM, I/O timeout, MMU aborts, parity aborts, and odd address aborts.

Sunset loops that can not be exited will occur if any of the following inputs are continuously asserted (i.e. does not clear when acknowledged): MPWRF-L, MFPE-L, MIRQ<3:0>-H, MEVENT-L.

4.6 Hardware Detected Errors

The KDJ11-B detects certain error conditions during program execution. These conditions, and the resultant actions, are described below.

4.6.1 Bus Timeout Errors

A bus timeout error can occur during KDJ11-B bus cycles. If BRPLYL is not asserted within 10 microseconds following the assertion of BDIN L or BDOUT L, the processor recognizes the error condition and immediately traps through virtual address 4 in kernel data space. Furthermore, if the address which caused the timeout referenced the I/O page, CPU error register bit <4> is set to signal an I/O bus timeout; otherwise bit <5> is set to signal a non-existant memory error. In Unibus Systems, the KDJ11-B does not timeout after 10 usec, but relies on the KTJ11-B to assert the PMI Time Out Signal.

4.6.2 Addressing Errors

An addressing error occurs when an odd address is used with a word reference (odd addressing error), or an instruction stream fetch attempts to access an internal processor register. The following are the internal processor registers: PAR's, PDR's, CPU error, PS, PIRQ, MMR0-MMR3, hit/miss, and cache control. When recognized, the processor immediately traps through virtual address 4 in kernel data space and sets bit <6> in the CPU error register.

4.6.3 Red Stack Aborts

A Red Stack abort occurs if, during the servicing of an abort, interrupt or TRAP instruction, an abort occurs while pushing the PS and PC onto the kernel stack. A Red Stack abort sets CPU Error Register bit <2>, loads virtual address 4 into the kernel stack pointer (R6) and then traps thru location 4 in kernel data space. The old PC and PS are saved in kernel data space locations 0 and 2 respectively.

CPU Error Register bit <2>, then reads the vector at virtual address 4 in kernel data space, then sets up an emergency stack in the new mode at virtual address 4, and then executes a trap through virtual address 4. The result is that old PC and PS get saved in locations 0 and 2, respectively.

4.6.4 Interrupt Vector Timeouts

An interrupt vector timeout occurs when BRPLY L is not asserted within 10 microseconds after an interrupt is acknowledged (BIAK L). The timeout is ignored and the processor continues as if the interrupt request never occurred. In Unibus Systems, the KDJ11-B does not timeout after 10 usec, but relies on the KTJ11-B to assert the PMI Time Out Signal.

4.6.5 No Sack Timeouts

A no Sack timeout occurs when BSACK L is not asserted within 10 microseconds(Q-Bus systems only) after a DMA is granted (BDM[illegible]). The timeout is ignored. The processor continues as if the DMA request never occurred.

4.7 Power Up Protocol

The power up protocol is fully compatible with DEC STD 160 and, when operating with the KTJ11-B, with DEC STD 158.

4.8 Power Down Protocol

The Power Down protocol is fully compatible with DEC STD 160 and, when operating with the KTJ11-B, with DEC STD 158.

5.0 Memory Management

The KDJ11-B implements 11/44 compatible memory management. This features:

- 22 bit physical address translation.
- Instruction and data (I/D) address spaces.
- Kernel, supervisor, and user (K/S/U) processor modes.

The visible memory management state consists of 48 Page Address Registers (PARs), 48 Page Descriptor Registers (PDRs), and four Memory Management Registers (MMR0-3).

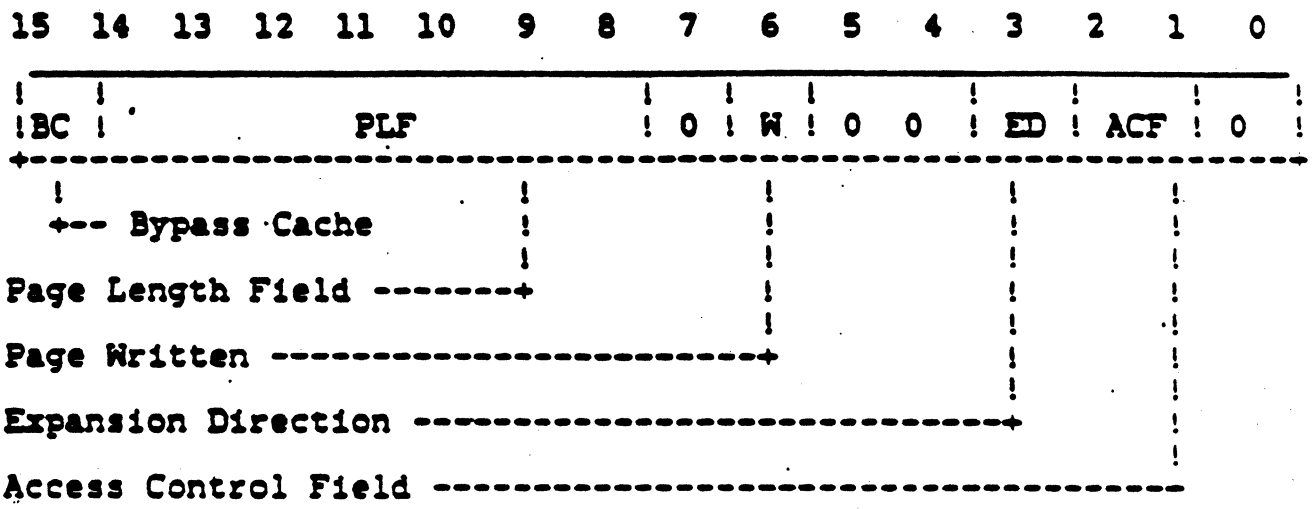
5.1 Page Address Registers - PARs

The Page Address Registers (PARs) contain the 16-bit Page Address Field (PAF). The PAF specifies the base address of the page.

All bits are read/write. These registers are not affected by console start or a RESET instruction. Their state at power up is UNDEFINED.

5.2 Page Descriptor Registers - PDRs

The Page Descriptor Registers (PDRs) contain information relative to page expansion, page length, and access control.



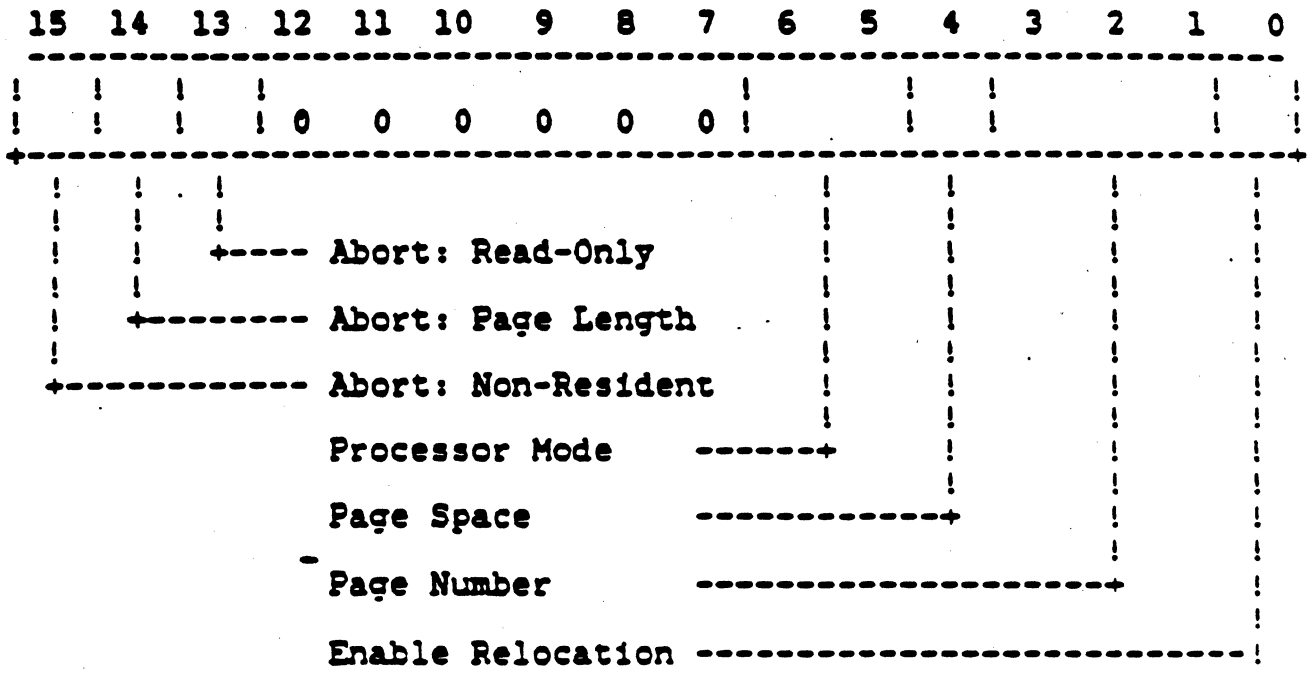
BIT	NAME	FUNCTION
15	Bypass Cache (RW)	This bit implements a conditional cache bypass mechanism. If set, references to the selected virtual page will bypass the cache. As shown in Section 6.3, a cache bypass causes the cache location to be invalidated whenever a read or write hit occurs.
14:8	Page Length Field (RW)	This field specifies the block number which defines the boundary of the current page. The block number of the virtual address is compared against the Page Length Field to detect length errors. An error occurs when expanding upwards if the block number is greater than the Page Length Field, and when expanding downwards if the block number is less than the Page Length Field.
6	Page Written (RO)	This bit indicates whether or not this page has been modified (i.e. written into) since either the PAR or PDR was loaded (1 is affirmative). It is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and hence must be saved in their new form and which pages have not been modified and can simply be overlaid. This bit is reset to 0 whenever either the PDR or the associated PAR is written into.

BIT	NAME	FUNCTION
3	Expansion Direction (RW)	This bit specifies in which direction the page expands. If ED=0 the page expands upwards from block number 0 to include blocks with higher addresses; if ED=1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.
2:1	Access Control Field (RW)	This field contains the access rights to this particular page. The access codes or "keys" specify the manner in which a page may be accessed and whether or not a given access should result in an abort of the current operation. The access codes are: 00 Non-resident - abort all accesses 01 Read only - abort on writes 10 Not used - abort all accesses 11 Read/write

These registers are not affected by console start or a RESET instruction. Their state at power up is UNDEFINED. All unused bits read as zero and cannot be written.

5.3 Memory Management Register 0 (Address 17 777 572)

Memory management Register 0 (MMR0) contains error flags, the page number whose reference caused the abort, and various other status flags.



BIT	NAME	FUNCTION
15	Abort - Non Resident (RW)	Bit 15 is set by attempting to access a page with an Access Control Field key equal to 0 or 2. It is also set by attempting to use memory relocation with a mode (PS<15:14>) of 2.
14	Abort - Page Length (RW)	Bit 14 is set by attempting to access a location in a page with a block number (virtual address bits <12:6>) that is outside the area authorized by the Page Length Field of the Page Descriptor Register for that page.
13	Abort - Read Only (RW)	Bit 13 is set by attempting to write in a "Read Only" page. "Read-Only" pages have access keys of 1.

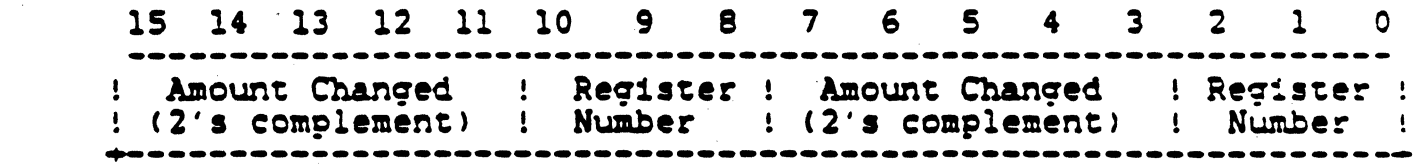
Note that bits <15:13> can be set by an explicit write; however such an action does not cause an abort. Whether set explicitly or by an abort, bits <15:13> cause memory management to freeze the contents of MMR0<6:1>, MMR1, and MMR2. The status registers remain frozen until MMR0 <15:13> are cleared by an explict write or any initialization sequence.

6:5	Processor Mode (RO)	Bits (6:5) indicate the processor mode (kernel/supervisor/user/illegal) associated with the page causing the abort (kernel = 00, supervisor = 01, user = 11, illegal = 10). If the illegal mode is specified, an abort is generated and bit (15) is set.
4	Page Space (RO)	Bit 4 indicates the address space (I or D) associated with the page causing the abort (0 = I space, 1 = D space).
3:1	Page Number (RO)	Bits (3:1) contain the page number of the page causing the abort.
0	Enable Relocation (RW)	Bit 0 enables relocation. When it is set to 1, all addresses are relocated. When bit 0 is set to 0, memory management is inoperative and addresses are not relocated.

MMR0 is cleared at power up, by a console start, and by a RESET instruction.

5.4 Memory Management Register 1 (Address: 17 777 574)

Memory Management Register 1 (MMR1) records any auto increment or decrement of the general purpose registers. This register supplies necessary information needed to recover from a memory management abort.



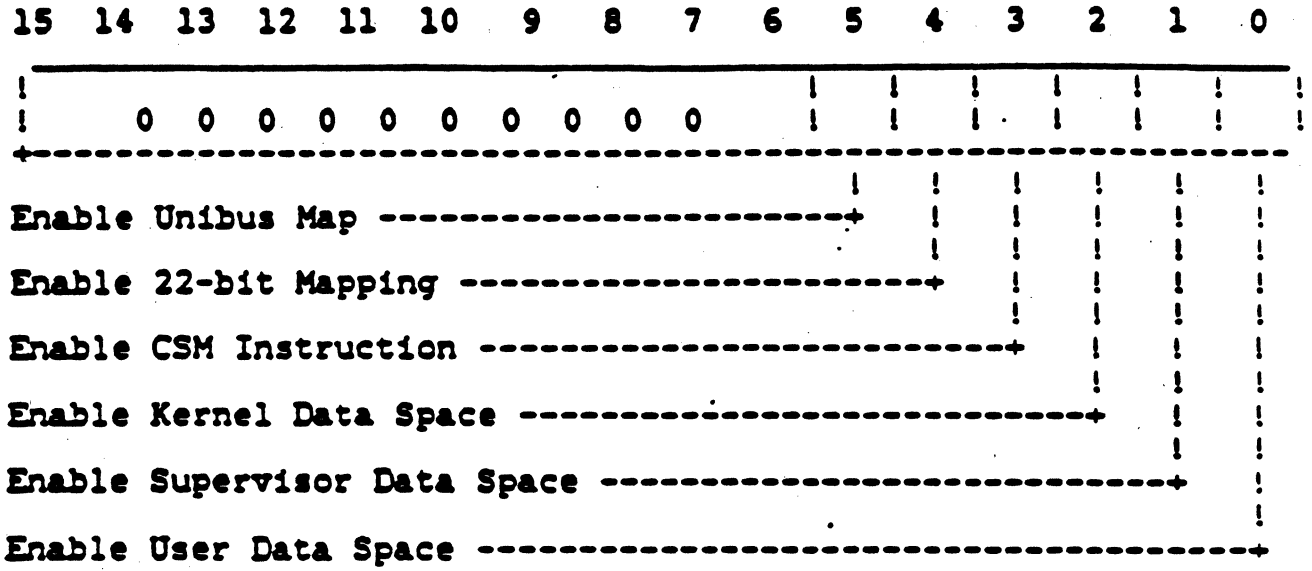
MMR1 is read only. Its state at power up is UNDEFINED.

5.5 Memory Management Register 2 (17 777 576)

Memory Management Register 2 (MMR2) is loaded with the virtual address at the beginning of each instruction fetch. MMR2 is read only. Its state at power up is UNDEFINED.

5.6 Memory Management Register 3 (Address: 17 772 516)

Memory Management Register 3 (MMR3) enables or disables D space, 22-bit mapping, the CSM instruction, and the I/O map (when applicable).



BIT	NAME	FUNCTION
5	Enable Unibus Map	This read-write bit enables the I/O Map when an external UNIBUS Adapter is provided. Otherwise, it has no effect.
4	Enable 22-bit Mapping	This read-write bit, when set, selects 22-bit memory addressing. When this bit is clear, 18-bit addressing is selected. (18 or 22-bit addressing is actually enabled only when MMR0 bit 0 is set).
3	Enable CSM Instruction	This read-write bit enables recognition of the Call Supervisor Mode instruction.
2:0	Enable Data Space	These three read-write bits enable Data Space mapping for kernel, supervisor, and user mode, respectively.

MMR3 is cleared at power up, by a console start, and by a RESET instruction.

6.0 KDJ11-B Cache Memory

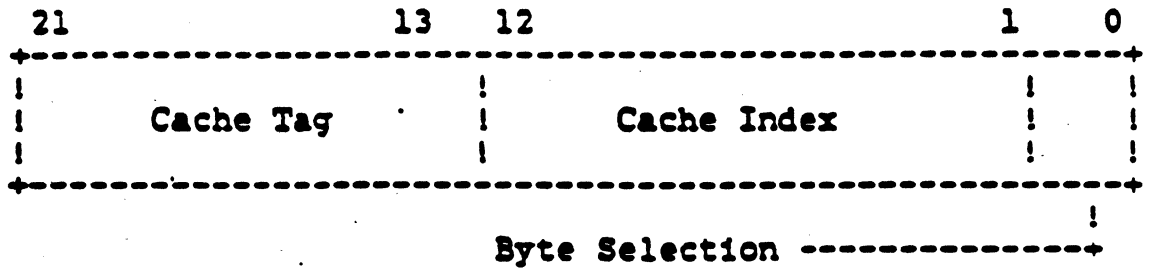
Cache memory is a small, high speed memory that maintains a copy of selected portions of main memory for faster access of instructions and data. When the KDJ11-B requires instructions or data from main memory, it checks the Cache memory, located on the KDJ11-B module, for availabilty of that data. When the needed data is found in the cache, a "hit" is said to occur. A "miss" occurs when the data is not in the cache.

6.1 Cache Organization

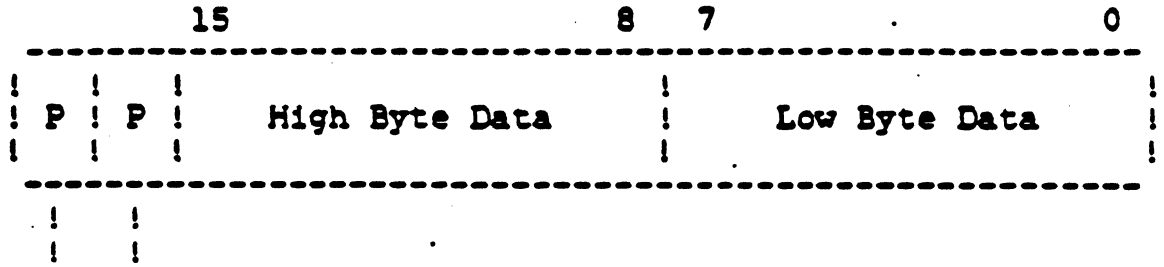
The KDJ11-B contains an 8K byte direct map cache with dual TAG Store which allows more concurrent operation of the CPU and DMA. The Cache Memory can be subdivided into three distinct sections: the Data Store, the CPU TAG Store and the DMA TAG Store.

The KDJ11-B Cache interprets the CPU (or DMA) physical address as shown in figure 6-1. Physical address bits 12-01 directly select one of 4,096 cache memory locations. Each cache memory location contains a Data Store (figure 6-2), a CPU Tag Store (figure 6-3) and a DMA Tag Store (figure 6-4). The CPU and DMA Tag Stores are updated at the same time, and contain identical information. During CPU read and write operations, the CPU Tag Store is compared against the CPU physical address bits 21-13 to determine cache hit or miss. During DMA write operations, the DMA Tag Store is compared against the DMA physical address for a cache hit or miss. In both cases, if the Tag Valid Bit is set, and if Tag bits 21-13 are equal to physical address bits 21-13 and no parity error, a cache hit is indicated.

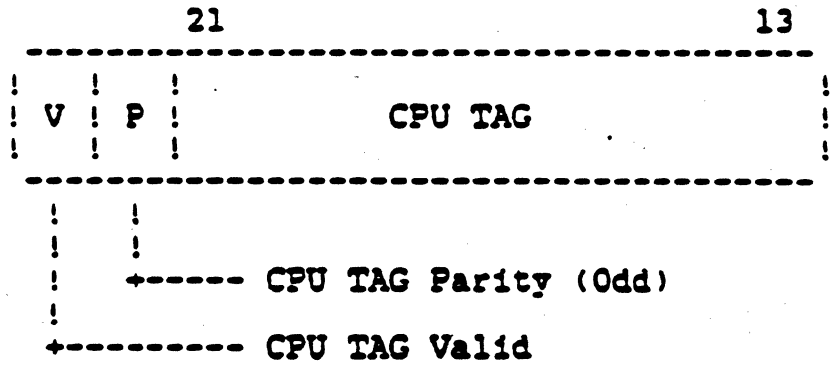
The High Byte Parity bit reflects odd parity on data bits <15-08>. The Low Byte Parity bit reflects even parity on data bits <07-00>. The CPU Tag Parity bit reflects odd parity on CPU Tag bits <21-13>. The DMA Tag Parity bit reflects odd parity on DMA Tag bits <21-13>. The CPU and DMA Tag Valid bits are not included in the CPU and DMA Tag parity calculations.



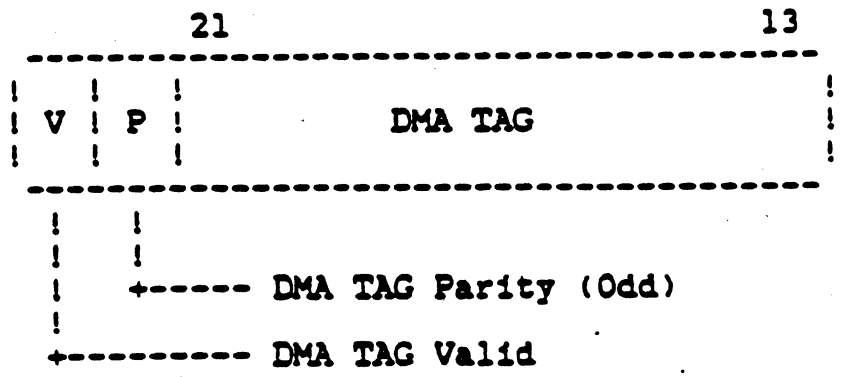
Physical Address Interpretation
Figure 6-1



Cache Data Organization
Figure 6-2



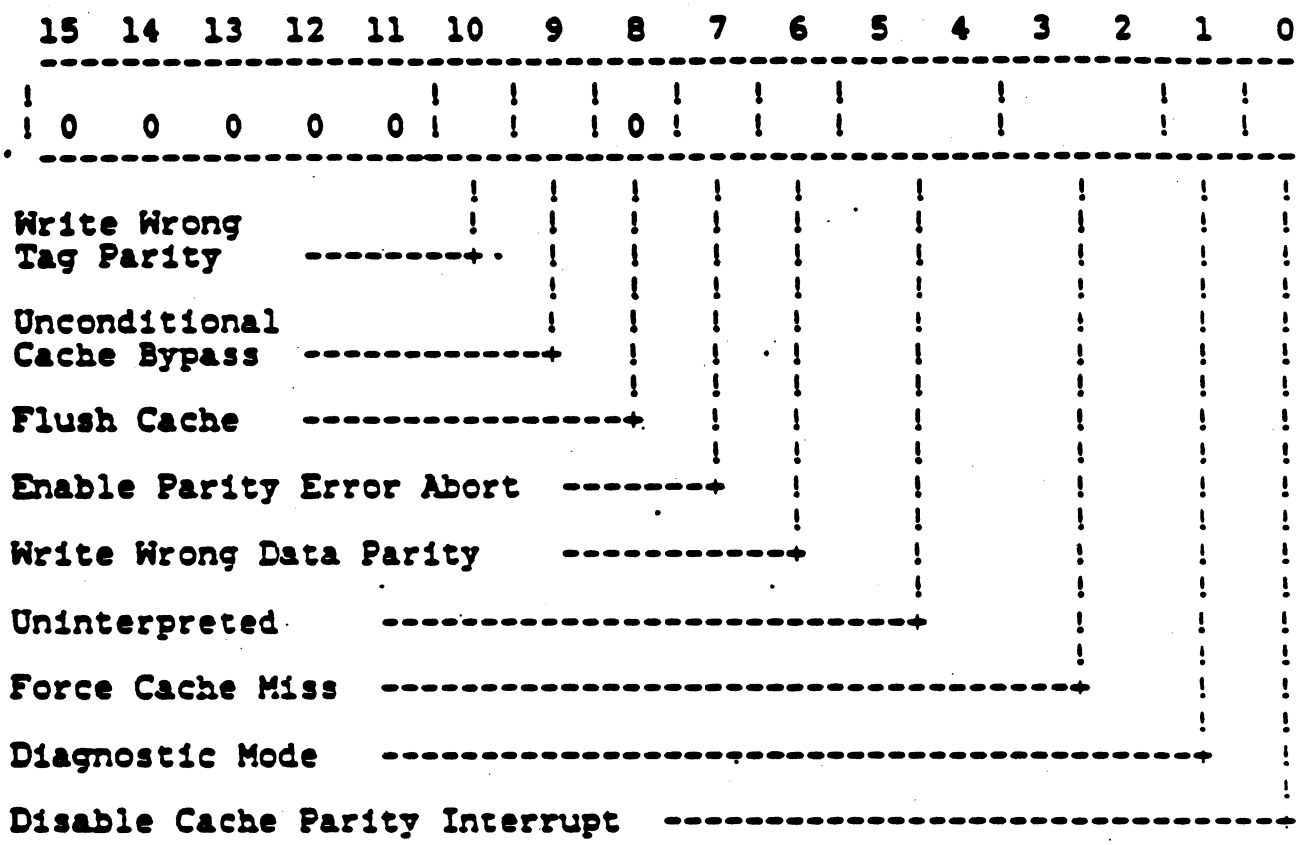
Cache CPU Tag Organization
Figure 6-3



Cache DMA Tag Organization
Figure 6-4

6.2 Cache Control Register (Address: 17 777 746)

The Cache Control Register (CCR) controls the operation of the cache. It is organized as follows:



Bits <15:11> always read as zeros. Bits<5:4,1> are read/write but are not interpreted by the KDJ11-B.

Two copies of the cache control register are kept on the KDJ11-B. One copy is kept in the chip set; the other on the board. The chip copy implements bits<10:0> as read/write but interprets only bits <9,3:2>. This copy is used as the source of data when the register is read. The board copy implements bits<10,8,7,6,0>. This is a write only copy. It can not be explicitly accessed.

Bit(s)	Name	Function
15-11		Unused. These bits always read as "0".
10		Write Wrong Tag Parity. When this read/write bit is set, the CPU and DMA Tag Parity bits are both written as wrong parity during all operations which update these bits. A cache tag parity error will thus occur on the next access to that location.
09		Unconditional Cache Bypass. When this read/write bit is set, all references to memory by the CPU will bypass the cache and go directly to main memory. Read or write hits will result in the invalidation of the corresponding cache location; misses will not affect the cache contents.
08		Flush Cache. Writing a "1" into this write-only bit clears clears all CPU Tag and DMA Tag Valid bits invalidating the entire contents of the cache. Writing a "0" into this bit has no effect. Flush Cache always reads as zero. The KDJ11-B requires approximately 1 msec to flush the cache. During this period, DMA activity is not possible and CPU activity is suspended.
07		Parity Error Abort. This read/write bit is set for diagnostic purposes only. When it is set, a cache parity error (during a CPU cache read) will cause the CPU to abort the current instruction and trap to parity error vector 114. When this bit is clear, a cache parity error (during a CPU cache read) results in a force miss and data fetch from main memory. The CPU will trap to 114 only if CCR bit <0> is clear. DMA cycle cache parity errors will cause a trap to 114 if CCR <7> is set or if CCR <0> is clear. CCR <7> has no effect on main memory parity errors which always cause the CPU to abort the current instruction and trap to 114.
06		Write Wrong Data Parity. When this read-write bit is set, both the high and low data parity bits are written with wrong parity during all operations which update these bits. This will cause a cache data parity error to occur on the next access to that location.

BITS	NAME	FUNCTION
03-02		Force Miss. When either of these read-write bits is set, CPU reads will be reported as cache misses.
01		Diagnostic Mode. When this read/write bit is set, a 10 usec nonexistant memory timeout during a word write will not cause a nonexistant memory trap and will not set CPU Error Register bit 05. All non-bypass and non-forced miss word writes will allocate the cache irrespective of the nonexistant memory timeout.
00		Disable Cache Parity Interrupt. This read-write bit controls Cache Parity Interrupts when CCR <7> is clear (normal operation). If CCR <7> is clear, a cache parity error (during a CPU cache read) results in a force miss and data fetch from main memory. The CPU will trap to 114 only if CCR bit <0> is clear. DMA cycle cache parity errors will cause a trap to 114 if CCR <7> is set or if CCR <0> is clear.

The following table summarizes the effect of CCR <7,0> on parity errors during CPU cache reads:

CCR<7>	CCR<0>	Result of Cache Parity Error
0	0	Cache Miss and Update Cache; Interrupt to 114.
0	1	Cache Miss and Update cache; No Interrupt.
1	X	Abort Instruction and Trap to 114.

The following table summarizes the effect of CCR <7,0> on DMA Tag Parity errors during DMA Writes:

CCR<7>	CCR<0>	Result of Cache Parity Error
0	0	Interrupt to 114.
0	1	No Interrupt.
1	X	Trap to 114.

The Cache Control Register is cleared by the negation of DCOK and by a console start. It is not affected by BUS INIT. The OUT command "G" will cause cache to be flushed and CCR to be cleared.

6.3 Cache Response Matrix

	DMA		CPU	
	HIT	MISS	HIT	MISS
Read	Read Memory	Read Memory	Read Cached Data	Read Memory & Allocate Cache
Write Word	Invalidate Cache-Write Memory	Write Memory	Write both Cache and Memory	Write both Cache and Memory
Write Byte	Invalidate Cache-Write Memory	Write Memory	Write both Cache and Memory	Write Memory -No Cache Change
Read Bypass	-	-	Invalidate Cache & Read Memory	Read Memory -No Cache Change
Write Bypass	-	-	Invalidate Cache & Write Memory	Write Memory -No Cache Change
Read Force Miss	Read Memory	Read Memory	Read Memory -No Cache Change	Read Memory -No Cache Change
Write Force Miss	Write Memory-Invalidate Cache	Write Memory	Write Memory -No Cache Change	Write Memory -No Cache Change

Cache Parity Errors affect the Cache Response Matrix in the following ways:

1. During DMA Write Cycles, a DMA Tag Parity Error forces a Cache Hit response, and the cache location is invalidated.

2. During CPU Read Cycles (Non-Bypass), a CPU Tag or Data Parity Error forces a Cache Miss response.

3. During CPU Write Byte Cycles (Non-Bypass; Non-Force Miss), a CPU Tag Parity Error forces a Cache Hit response, but the data is loaded with bad parity.

4. During CPU Read Bypass or Write Bypass Cycles, a CPU Tag or Data Parity Error forces a Cache Hit Response. The cache location is invalidated.

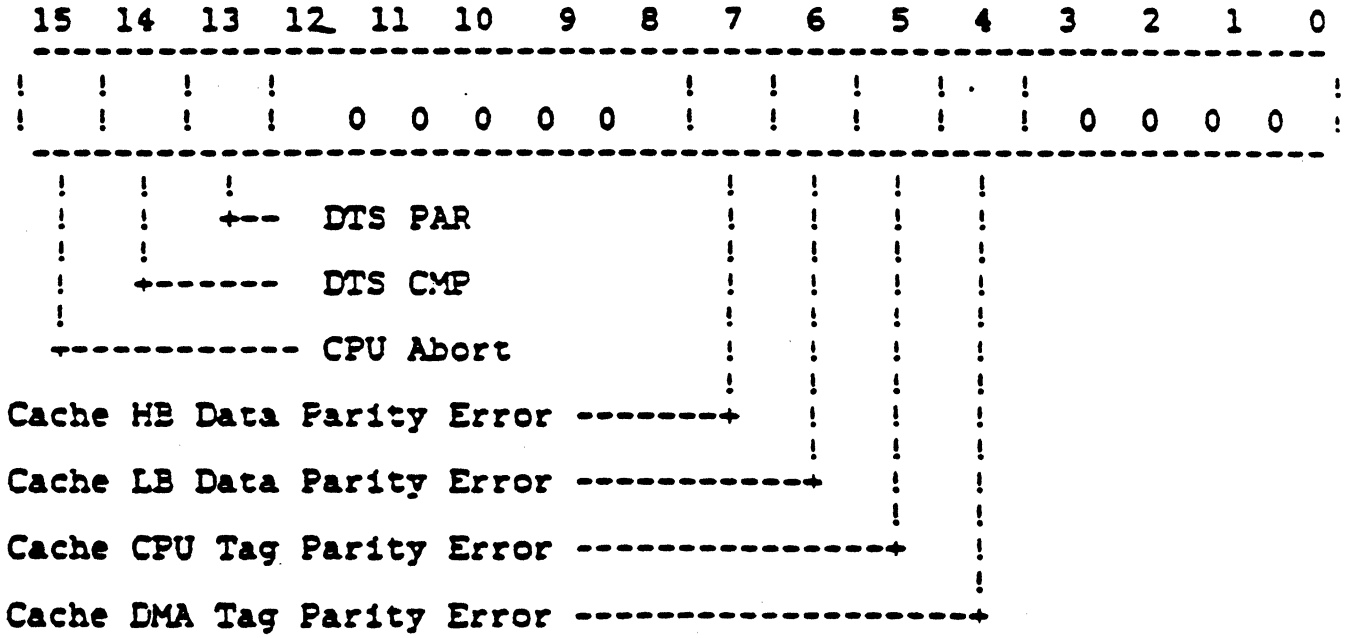
5. For all Force Miss Cycles, and for the CPU Write Word (Non-Bypass) Cycle, Cache Parity is ignored.

6.4 Memory System Error Register (Address: 17 777 744)

The Memory System Error Register (MSER) reflects the status of cache and main memory parity errors. MSER bit 15 is set if a cache or main memory parity error results in an instruction abort. MSER bits 14 and 13 are used by the KDJ11-B Boot and Diagnostic programs to test the Cache DMA Tag Store. They are only valid when the Boot and Diagnostic Controller Status Register Stand-Alone Mode bit (BCSR <8>) is set.

If the Cache Control Register Parity Error Abort bit (CCR <7>) is set, MSER <7>, <6> and/or <5> are set individually if a cache parity error occurs in the high data byte, low data byte or CPU tag fields, respectively, during a CPU cache access. Similarly, MSER bit 04 is set if a DMA tag field parity error occurs during a DMA cache cycle.

If CCR bit 07 is clear, operation of MSER bits 07-05 is altered for software compatibility reasons. MSER bits 07-05 are all set if any parity error occurs during a CPU cache access. Similarly, MSER bits 07, 06 and 04 are all set if a DMA tag field parity error occurs during a DMA cycle.



Bit	Name	Function
15		CPU Abort. This read-only bit is set if a cache or main memory parity error results in an instruction abort (i.e. only during the demand read cycle). Cache parity errors cause an abort only if CCR <7> is set. Main memory parity errors always cause an abort.
14		DMA Tag Store Comparator (DTS CMP). In Stand-Alone Mode (BCSR <8> set), this read-only bit indicates the output of the Cache DMA Tag Store Comparator for the previous Non-I/O Page reference with cache miss. When BCSR <8> is clear, DTS CMP reads as "0".
13		DMA Tag Store Parity (DTS PAR). In Stand-Alone Mode (BCSR <8> set), this read-only bit indicates the output of the DMA Tag Store Parity Check Logic for the previous Non-I/O Page Reference with cache miss. When BCSR <8> is clear, DTS PAR reads as "0".
12-08		Unused. These bits always read as "0".
07		Cache HB Data Parity Error. This read-only bit is set if a parity error is detected in the high data byte during a CPU cache read. If CCR <7> is clear, MSER <7> is also set by a low byte parity error and by the set condition of MSER <5> or <4>.
06		Cache LB Data Parity Error. This read-only bit is set if a parity error is detected in the low data byte during a CPU cache read. If CCR <7> is clear, MSER <6> is also set by a high byte parity error and by the set condition of MSER <5> or <4>.
05		Cache CPU Tag Parity Error. This read-only bit is set if a parity error is detected in the CPU tag field during a CPU cache read. If CCR <7> is clear, MSER <7> is also set by a high or low data byte parity error.
		Note: Cache parity errors are ignored (do not affect MSER <7-5>), if either CCR <3> or <2> (Force Miss) is set or if the CPU Tag Valid bit is clear.

BIT	NAME	FUNCTION

04 Cache DMA Tag Parity Error. This read-only bit is set if a parity error is detected in the DMA tag field during a during a DMA write operation.

Note: Cache parity errors are ignored (do not affect MSER <4>), if either CCR <3> or <2> (Force Miss) is set or if the DMA Tag Valid bit is-clear.

03-00 Unused. These bits always read as zero.

Main memory parity errors always cause the CPU to abort the current instruction, to set MSER <15> and to trap thru vector location 114.

Cache parity errors which occur during a CPU Cache access may result in an instruction abort and/or a trap to location 114, depending on CCR <7> and <0>:

1. If CCR <7> (Parity Error Abort) is set, a cache parity error causes the CPU to abort the current instruction, to set MSER <15> and the relevant error bit(s) MSER <7:5> and to trap thru vector location 114.

2. If CCR <7> is clear, and if CCR <0> is also clear, a cache parity error causes the CPU to force a cache miss, set the relevant error bits MSER <7:5> and to trap thru vector location 114.

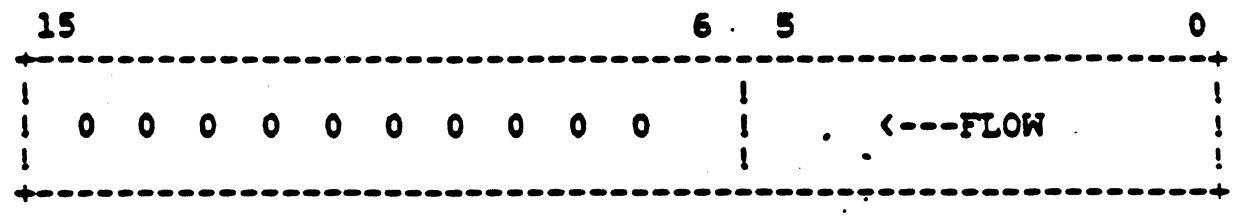
3. If CCR <7> is clear, and if CCR <0> is set, a cache parity error causes the CPU to force a cache miss and to set the relevant error bits MSER <7:5>. The CPU does not trap thru vector location 114.

Cache DMA tag field parity errors which occur during a DMA cycle cause a trap to location 114 if CCR <7> is set or if CCR <0> is clear.

The Memory System Error Register is cleared by any MSER write reference. It is also cleared on power up or by a console start. It is unaffected by a RESET instruction.

6.5 Hit/Miss Register (17777752)

This register indicates whether the six most recent CPU memory references resulted in cache hits or cache misses:



Bits enter from the right (at bit <0>) and are shifted leftward. A one indicates a cache hit, a zero indicates a cache miss.

The Hit/Miss Register is read only. Its value at power up is UNDEFINED. The Hit/Miss Register is not affected by console start or a RESET instruction. The Hit/Miss Register will always read zero when cpu is console ODT mode.

6.6 Cache Multi-Processor Hooks

The following multi-processor cache "hooks" exist in the KDJ11-B:

- Conditional cache bypass - selected virtual pages can be made to bypass the cache. Bit <15> in the PDRs sets this condition.

- Unconditional cache bypass - all CPU references can be made to bypass the cache. Bit <9> in the Cache Control Register sets this condition.

- Flush cache - all valid bits in the cache are cleared.

- Lock instruction (ASRB, TSTSET, and WRTLCK) - these instructions guarantee a cache bypass reference.

7.0 Private Memory Interconnect

7.1 General Description

The private Memory interconnect (PMI) consists of 14 signals which are unique to PMI protocol plus additional signals which are shared with the Q-Bus protocol. The PMI provides a high performance communication path between the KDJ11-B CPU, the MSV11-J Memory and, for Unibus Systems, the KTJ11-B Unibus Adapter. Data and address information is multiplexed and uses the same data/address lines used by the Q-Bus protocol.

PMI protocol is specifically designed for and used in the PDP-11/83 Q-Bus System and the PDP-11/84 Unibus System.

A PDP-11/83 Q-Bus system is configured using the KDJ11-B CPU Module, one or more MSV11-J Memory Modules and a selection of Q-Bus compatible devices. Data transfers between the KDJ11-B CPU and MSV11-J Memory follow PMI protocol. All other communications whether originated by the CPU or by a DMA device, occur via Q-Bus protocol.

A PDP-11/84 Unibus system is configured using the KDJ11-B CPU Module, one or two MSV11-P Memory Modules, the KTJ11-B Unibus Adaptor (UBA) Module and a selection of Unibus compatible devices. The KDJ11-B, MSV11-P and KTJ11-B Modules communicate via PMI protocol. All communication between Unibus devices and the KTJ11-B occur via Unibus protocol. The KTJ11-B provides the appropriate interface between PMI and Unibus protocols.

Q-Bus devices can not be configured in a system containing the KTJ11-B Unibus Adapter Module.

7.2 The PMI Specification

All information on the Private Memory Interconnect is contained in the PMI Specification.

8.0 Micro-ODT Console

The console octal debugging technique or console ODT allows the KDJ11-B to respond to commands and information entered via the console terminal interface. Console ODT is a very useful aid in running and debugging programs.

For complete information on the Micro-ODT console, refer to sections 5.3.2- 5.3.7 of the DCJ11 Microprocessor User's Guide.

9.0 KDJ11-B Boot and Diagnostic Facility

The KDJ11-B Boot and Diagnostic Facility features four hardware registers, two ROM Sockets for 4K, 8K or 16K words of 16-bit read-only memory and a third ROM Socket for 2K, 4K or 8K bytes of either 8-bit read-ony memory or 8-bit Electrically Erasable PROM memory. The 16-bit ROM typically contains executable code including both diagnostics and a selection of boot programs. The 8-bit ROM or EEPROM typically contains the KDJ11-B Configuration Data plus space for optional, operator supplied boot programs.

The KDJ11-BA CPU Module populates the first two ROM sockets with 8K words of 16-bit ROM. This ROM contains stand-alone KDJ11-B diagnostics, the KDJ11-B configuration routines, both memory and system diagnostics and boot programs for various standard devices. If this ROM is replaced for special applications, the new ROM must contain some form of configuration routine and should also contain both stand-alone and system diagnostics.

The KDJ11-BA CPU Module populates the third ROM socket with 2K of 8-bit EEPROM, allocating 256 bytes for configuration data and leaving the remaining space available for operator supplied boot programs. For special applications, this ROM may be replaced either by 4K or 8K EEPROM or, if the application does not require alterable Configuration Data, by up to 8K bytes of ROM.

9.1 KDJ11-B Boot and Diagnostic Registers

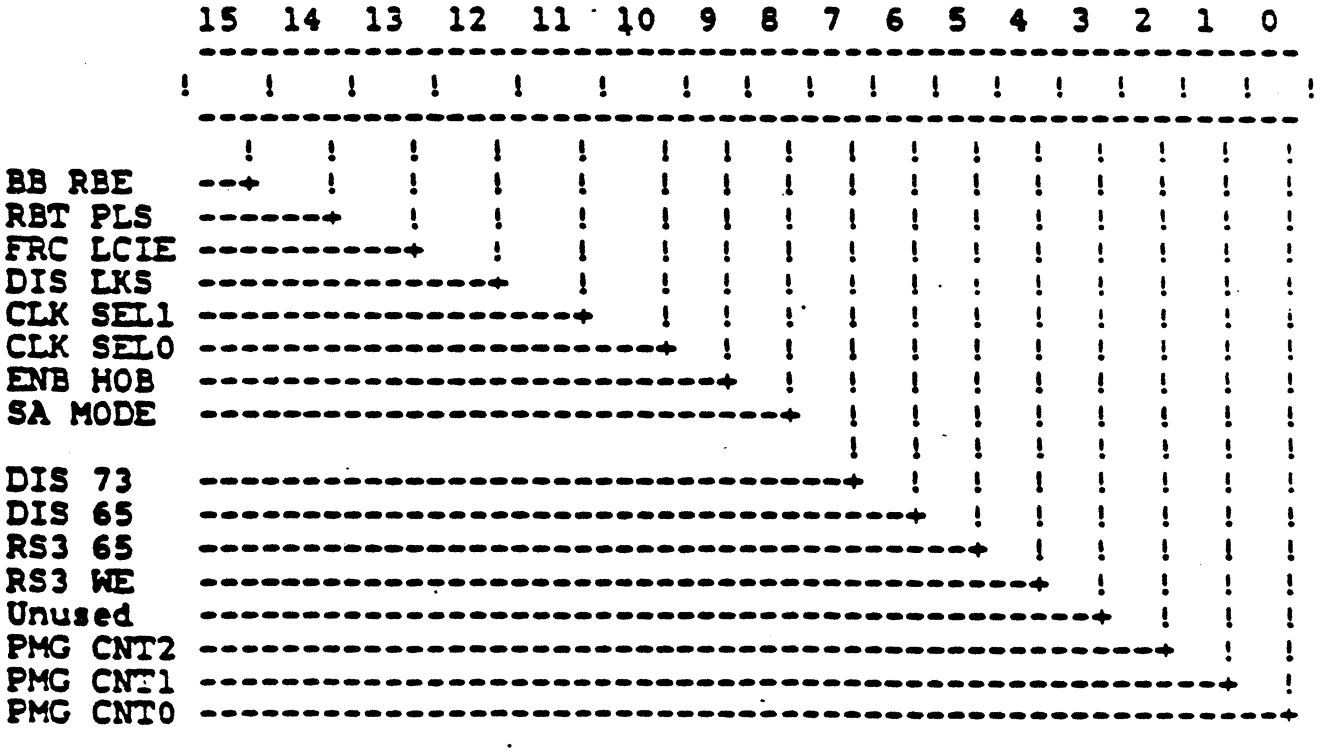
The KDJ11-B Boot and Diagnostic Registers include the Controller Status Register, the Page Control Register, and the Configuration and Display Register. The Boot and Diagnostic Facility also uses the KDJ11-B Maintenance Register, described in section 9.2.

9.1.1 Controller Status Register (Address: 17 777 520)

The Boot and Diagnostic Controller Status Register (BCSR) is both word and byte addressable. The BCSR allows the Boot and Diagnostic ROM programs to test battery backup and reboot status, to set parameters for the PMG (Processor Mastership Grant) Counter and for line clock, to enable the Console Halt on Break feature and to enter or exit from stand alone mode.

The BCSR also allows these programs to selectively disable the response of the Boot and Diagnostic ROM's to addresses 17765000 - 17765776 and/or to addresses 17773000 - 17773776 and to control read/write access to the EEPROM memory.

Programs which access the I/O Page can use the BCSR to alter PMG and line clock parameters, to enable or disable the Halt on Break feature and to control access to the ROM and and EEPROM memories.



BIT	MNEMONIC	MEANING
15	BB RBE	Battery Backup Reboot Enable. This bit, when set, indicates that battery backup failed to maintain voltages to the memory system during the previous power failure. This bit, when clear, indicates that the system does not feature battery backup or that battery backup maintained voltages during the previous power failure. This signal is received from backplane pin BH1 and latched when DCOK is asserted.
14	RBT PLS	Reboot Pulse. This read-only bit is set if DCOK pulses while POK remains asserted. This condition, which can only occur in Q-Bus Systems, indicates that a system reboot has been requested by the front panel switch or by a special Q-Bus device. RBT PLS is cleared by the negation of POK. A similar bit, contained in the KTJ11-B Diagnostic CSR, provides reboot status for Unibus Systems.
13	FRC LCIE	Force Line Clock Interrupt Enable. If this bit is set, assertion of the signal selecte by BCSR <11,10> (Clock Select Bits 1 and 0) will unconditionally request interrupts. If FRC LCIE is clear, assertion of the selecte signal will request interrupts only if the Line Clock Status Register bit <6> (LCIE) is set under program control. FRC LCIE is cleared by the negation of DCOK.
12	DIS LKS	Line Clock Status Register Disable. If this bit is set, the Line Clock Status Register (LKS) is disabled. If this bit is clear, LKS is enabled and responds to bus address 17777546. LKS DIS is cleared by the negation of DCOK.

BIT	MNEMONIC	MEANING
11 10	CLK SEL1 CLK SEL0	Clock Select Bits 1 and 0. These read-write bits select the source of the line clock interrupt request:

CLK SEL1	CLK SEL0	Source of Interrupt
0	0	External BEVENT Line
0	1	On-Board 50 Hz
1	0	On-Board 60 Hz
1	1	On-Board 800 Hz

CLK SEL1 and CLK SEL0 are cleared by the negation of DCOK.

09	ENB HOB	Enable Halt on Break. When this read-write bit is set, the Console Serial Line Unit Halt on Break feature is enabled. When this bit is clear that feature is disabled. ENB HOB is cleared by the negation of DCOK.
08	SA MODE	Stand-Alone Mode. When this read-write bit is set, the KDJ11-B operates in stand-alone mode, using its Cache as main memory. External memory and peripherals are all disabled. When SA MODE is clear, Stand-Alone Mode is turned off, enabling external memory and peripherals. SA MODE is set by the negation of DCOK.
07	DIS 73	Disable 17773000. When this read-write bit is set, response of the 16-bit ROM memory to addresses 17773000 - 17773776 is disabled, allowing the operation of an external ROM which uses those addresses. When DIS 73 is clear, the 16-bit ROMs respond to those addresses, using the high byte of the page control register as the most significant address bits. DIS 73 is cleared by the negation of DCOK.

BIT	MNEMONIC	MEANING
06	DIS 65	Disable 17765000. When this read-write bit is set, response of the Boot and Diagnostic 16-bit and 8-bit ROM memory to addresses 17765000 - 17765776 is disabled, allowing the operation of external ROM which uses those addresses. When DIS 65 is clear, the the rom memory selected by bcsr <5> respond to those addresses, using the low byte of the page control register as the most most significant address bits. DIS 65 is cleared by the negation of DCOK.
05	RS3 65	ROM Socket 3 at 17765000. This read-write bit selects whether the 16-bit ROM in ROM Sockets One and Two or the 8-bit ROM in ROM Socket Three responds to addresses 17765000 - 17765776 (assuming that BCSR <4> is clear). If RS3 65 is set, the 8-bit ROM is selected. If RS3 65 is clear the 16-bit ROM is selected. In either case the low byte of the page control register provides the most significant address bits. RS3 65 is cleared by the negation of DCOK.
04	RS3 WE	ROM Socket 3 Write Enable. If BCSR <6> (DIS 65) is clear, and if BCSR <5> and <4> (RS3 65 and RS3 WE) are both set, then the program can write access ROM socket 3 which typically contains an EEPROM. RS3 WE is cleared by Power Up and by Bus Initialize.
03	Unused	Unused. This bit always reads as "0".
02	PMG CNT2	Processor Mastership Grant Count bits 2, 1

BIT	MNEMONIC	MEANING
01	PMG CNT1	and 0. These read-write bits enable the PMG
00	PMG CNT0	Counter and select the length of time for PMG Counter overflow. When enabled, the PMG Counter is begins counting whenever the KDJ11-B must access an I/O Page location or external memory. Counter overflow causes the KDJ11-B to suppress all DMA Requests and to give the processor bus mastership during the next DMA arbitration cycle. When the PMG Counter is disabled, the processor is blocked from bus mastership as long as DMA Requests are pending.

PMG CNT2	PMG CNT1	PMG CNT0	Count Time
0	0	0	(Disabled)
0	0	1	0.4 usec
0	1	0	0.8 usec
0	1	1	1.6 usec
1	0	0	3.2 usec
1	0	1	6.4 usec
1	1	0	12.8 usec
1	1	1	25.6 usec

PMG CNT2, PMG CNT1 and PMG CNT0 are cleared by the negation of DCOK.

9.1.2 Page Control Register (Address: 17 777 522)

The Page Control Register is a read-write register which is both byte and word addressable. Only bits 14-09 and 06-01 can be loaded. The other bits always read as zero. The PCR high byte provides the most significant ROM address bits when the 16-bit ROM sockets are accessed by bus addresses 17773000 - 17773776. The PCR low byte provides the most significant ROM (or EEPROM) address bits when the 16-bit or 8-bit ROM (or EEPROM) sockets are accessed by bus addresses 17765000 - 17765776. BCSR bits 07-04 control access to the ROM and EEPROM memory.

When the 16-bit ROM sockets are accessed by bus addresses 17773000 - 17773776, PCR <14-09> are used as ROM address bits 14-09. The nine least significant bits of the bus address (bits 08-00) are used as bits 08-00 of the ROM address. The resulting 15-bit ROM address accesses the 16-bit ROM.

When the 16-bit ROM sockets are accessed by bus addresses 17765000 - 17765776, PCR <06-01> are used as ROM address bits 14-09. The nine least significant bits of the bus address (bits 08-00) are used as bits 08-00 of the ROM address.

When the 8-bit EEPROM (or ROM socket) is accessed by bus addresses 17765000 - 17765776, PCR bits 05-01 are used as EEPROM address bits 13-09.

This register is cleared by the negation of DCOK.

9.1.3 Configuration and Display Register

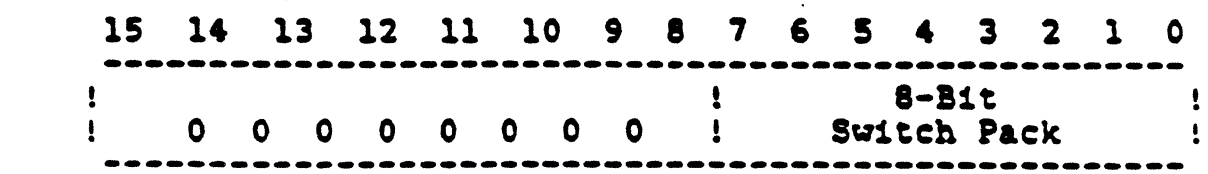
The Configuration and Display Register actually consists of two independent registers which share the same physical address: the read-only Configuration Register and the write-only Display Register.

9.1.3.1 The Configuration Register (Address: 17 777 524)

The read-only Boot and Diagnostic Configuration Register (BCR) reflects the status of eight switches (Switches <7-0>) edge mounted at the top of the module. Three of those switches (Switches <2-0>) can be asserted remotely via an external connector, also mounted at the top of the module.

During normal operation, switch <7> is in the clear position and switches <2-0> determine the Console Terminal Baud Rate. The Boot and Diagnostic ROM programs use the Configuration Data in the 8-bit EEPROM (or ROM) to select the various KDJ11-B and system parameters, including the Power Up Mode and/or the Boot Device.

For systems which do not have a Console Terminal, and for which the operator can not set up the EEPROM, switch <7> is placed in the set condition. The Boot and Diagnostic ROM programs use switches <6-0> to select a limited range of KDJ11-B and system parameters, including the Power UP Mode and/or the Boot Device. Setting switch <7> does not actually disable the console terminal interface which still responds to the Console Device Addresses and which runs at the Baud Rate reflected by switches <2-0>. The setting of switches <2-0> is determined by system configuration considerations and may not correspond to a usable Baud Rate.



BIT(S)	MEANING
15-08	Unused. These bits always read as zero.
07-00	Switches 07-00. These bits reflect the status of the eight switches edge mounted at the top of the KDJ11-B Module. Switches 02-00 can be asserted remotely via an external connector mounted at the top of the module. Each switch setting can be asserted by placing the switch in the "1" position or by grounding the appropriate external signal. Switches 02-00 are used by the console terminal interface to determine the Baud Rate. If switch 07 is in the set position, the Boot and Diagnostic ROM Programs suppresses communication with the console terminal and uses switches 06-00 to select a limited range of KDJ11-B and system parameters.

9.3 KDJ11-B ROM Memory (Addresses 17773XXX and 17765XXX)

The KDJ11-B Boot and Diagnostic Facility features two sockets which accept 4K, 8K or 16K words of 16-bit ROM memory and a third socket which accepts 2K, 4K or 8K bytes of 8-bit EEPROM (or ROM) memory. The KDJ11-BA features 8K words of Boot and Diagnostic ROM programs which are installed in the first two sockets and 2K bytes of EEPROM which are installed in the third socket.

9.3.1 KDJ11-B ROM Memory Addresses 17773000 - 17773776

KDJ11-B ROM Memory Addresses 17773000 - 17773776 can be used to access the 16-bit memory, but not the 8-bit memory. The 16-bit memory responds to these addresses only if Boot and Diagnostic Controller Status Register bit 07 (DIS 73) is clear.

When the read-only memory is accessed by bus addresses 17773000 - 17773776, Page Control Register (PCR) bits 14-09 are used as ROM address bits 14-09. The nine least significant bits of the bus address (bits 08-00) are used as bits 08-00 of the ROM address. The resulting 15-bit ROM address accesses up to 16K words of 16-bit ROM.

9.3.2 KDJ11-B ROM Memory Addresses 17765000 - 17765776

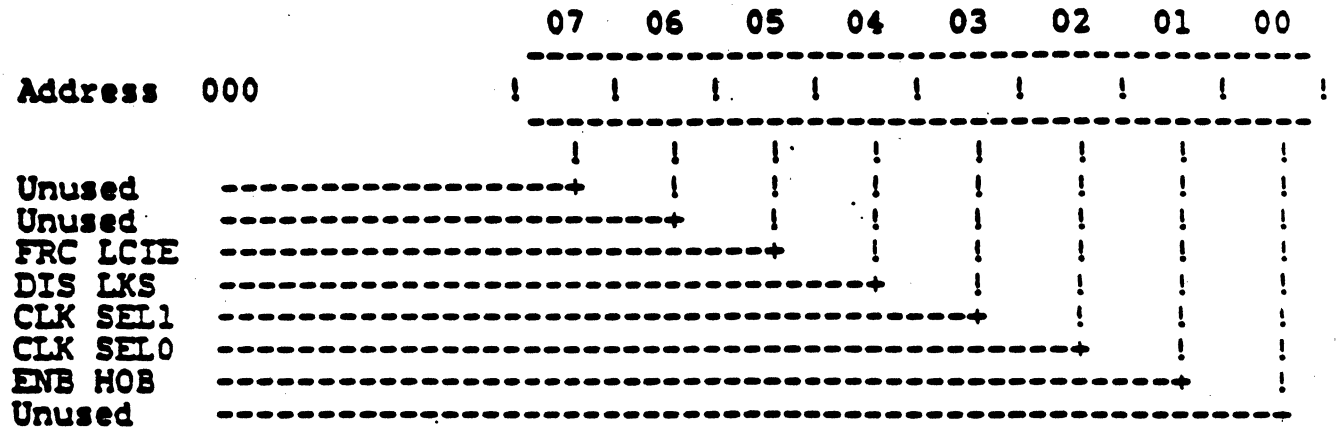
KDJ11-B ROM Memory Addresses 17765000 - 17765776 can be used to access either the 16-bit or the 8-bit memory. The 16-bit memory responds to these addresses if the Boot and Diagnostic Controller Status Register bits 06 (DIS 65) and 05 (RS3 65) are both clear. The 8-bit memory responds to these addresses if BCSR <6> (DIS 65) and <5> (RS3 65) are clear and set respectively.

When the read-only memory is accessed by bus addresses 17765000 - 17765776, Page Control Register (PCR) bits 06-01 are used as ROM address bits 14-09. The nine least significant bits of the bus address (bits 08-00) are used as bits 08-00 of the ROM address. The resulting 15-bit ROM address accesses up to 16K words. In the case of the 16-bit ROM, each word contains a full 16 bits of data. In the case of the 8-bit ROM, each word contains 8 bits of data, located in the low byte (bits 07-00). Because the maximum size for the 8-bit ROM is 8K, only the 14 least significant bits of ROM address are actually used.

Bit(s)	Name	Meaning
15-11		Unused. Reserved for future expansion. Read as zeros.
10		Multiprocessor Slave. This read-only bit reflects the status of an external line. A "1" indicates that this CPU is a multiprocessor slave. A "0" indicates that this CPU is either in a single processor system or is the arbirtrator in a multiprocessor system.
09		Unibus System. This read-only bit reflects the status of the externally applied Unibus Adapter line. A "1" indicates that the system includes a Unibus Adapter. A "0" indicates a Q-Bus System.
08		FPA Available. This bit is set (1) if a Floating Point Accelerator Chip is installed on the module.
07-04		Module Type. This 4-bit code is hard-wired as a "2", indicating a KDJ11-B Module.
03		Halt/Trap Option. This read/write bit determines the response of a processor to a Kernel Mode Halt instruction. A "1" selects the Trap Option, causing the CPU to trap to location 4. A "0" selects the Halt Option, causing the CPU to halt and enter ODT. This bit is cleared by the negation of DCOK and is set by the Boot and Diagnostic ROM code if the Trap Option is selected by a bit in the Configuration RAM. The Trap Option is not intended for normal use and is reserved for controller applications.
02-01		Power Up Code. This 2-bit code is hard-wired as a "2". At power up, the processor sets the PC to 173000 and sets the PSW to 370. It then starts program execution at location 173000, which is the starting location for the KDJ11-B Boot and Diagnostic ROM program. These programs test out the KDJ11-B Module and then implement the user selected power up option specified in the Configuration Data.
00		BPOK H. This bit is set (1) if the Q-Bus signal BPOK H is asserted, indicating that AC Power is okay.

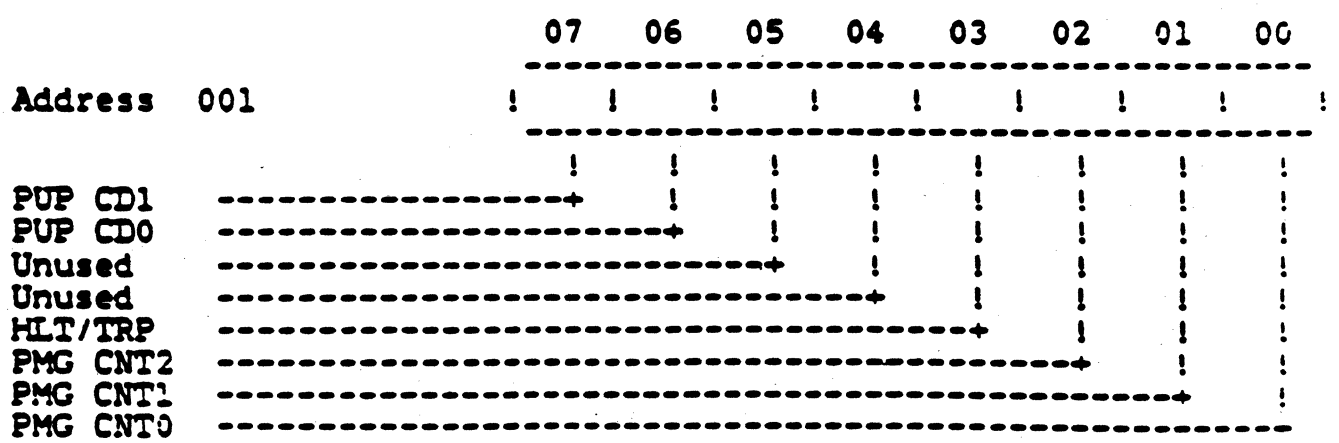
9.4.1 Configuration Data Formats

The Configuration Data Formats will be defined in the specification for the KDJ11-BA Boot and Diagnostic ROM Program. This section contains a first pass at these formats and will be updated later to reflect the actual formats:



Bit(s)	Mnemonic	Meaning
07		Unused.
06		Unused.
05	FRC LCIE	Force Line Clock Interrupt Enable.
04	LKS DIS	Line Clock Status Register Disable.
03	CLK SEL1	Clock Select Bit 1
02	CLK SEL0	Clock Select Bit 0
01	ENB HOB	Enable Halt on Break.
00		Unused

Refer to section 9.1.1 for a description of these bits.
Bits <5-1> are loaded into BCSR <13-09>.



Bit(s)	Mnemonic	Meaning
07 06	PUP CD1 PUP CD0	Power Up Code Bits 01 and 00. These two bits select the Power Up Option. Code 00: Run selected stand-alone tests and then simulate a trap to 24/26. Code 01: Run selected stand-alone tests and then halt, causing processor to enter ODT. Note that the Halt Option must be specified (see bit 03 below). Code 02: Run all selected tests and then enter dialogue mode, allowing operator to either specify a Boot Device or to enter Setup Mode. Code 03: Run all selected tests and then boot system via the specified boot device.
05-04		Unused.
03	HLT/TRP	Halt/Trap Option. The Boot and Diagnostic Program loads this bit into Maintenance Register bit 03. Refer to section 9.2.
02 01 00	PMG CNT2 PMG CNT1 PMG CNT0	Processor Mastership Grant Count bits 2-0. The Boot and Diagnostic Program loads these bits into BCSR <02-00>. Refer to section 9.1.1.

The bits in Memory locations 002 and 003 will be used to define test selection.

The bits in Memory locations 004 and 005 will be used to select a boot device.

The bits in RAM locations 014-017 will be used for error detection or, perhaps, error correction codes

9.5 KDJ11-BA ROM Code Operation

The KDJ11-B always powers up and reboots to location 17773000. At this point the KDJ11-B is running in stand-alone mode. If the HALT Switch is set, the system halts and enters ODT. If the Halt switch is clear, the system begins execution of the Boot and Diagnostic ROM program.

All configurable system parameters are programmed by the Boot and Diagnostic Program. Most of them could be altered later by the operating system, but there is currently no software support in that area.

To change the system configuration, the operator powers up, reboots, and select the "S" option. The Boot and Diagnostic Reconfiguration Program will then walk him thru the various parameters. After reconfiguration is complete, the program gives the operator the option of storing the new configuration in the EEPROM before booting up the system with the new configuration.

The Boot and Diagnostic Program runs stand-alone diagnostics before, during and after the programming of configurable system parameters. Some of these tests may be selectable by bits in the configuration RAM. After completing these diagnostics, the program clears the Stand-Alone Mode bit. Depending on the power up mode defined in the Configuration RAM, the program will then either enter ODT, simulate a power up vector to 24/26, or boot the system, with the selected boot device, after running selected system diagnostics.

Details on KDJ11-BA ROM Code operation will be contained in the yet to be written "KDJ11-BA Boot and Diagnostic ROM Fuctional Specification. This section will be fleshed out a bit as more information is available.

10.0 LINE FREQUENCY CLOCK

10.1 Line Clock Function

The Line Clock provides the system with timing information at fixed intervals determined by the Q-Bus BEVENT line or by the one of the on-board KDJ11-B frequency signals as programmed by Boot and Diagnostic Controller Status Register bits 11 and 10. Typically, BEVENT cycles at the AC line frequency, producing intervals of 16.7 msec (60 Hz line) or 20.0 msec (50 Hz line). The three on-board frequencies are 50 Hz, 60 Hz and 800 Hz.

10.2 Clock Status Register (LKS) 17777546

The Clock Status Register (LKS) allows Line Clock interrupts to be enabled and disabled under program control. Alternatively, line clock interrupts can be unconditionally enabled by setting BCSR <13> (FRC LCIE). Program recognition of the Clock Status Register can be disabled by setting BCSR <12> (LKS DIS). The normal KDJ11-B configuration is FRC LCIE and LKS DIS both clear. These bits are set up by the Boot and Diagnostic ROM programs from the KDJ11-B Configuration Data. For additional information, refer to sections 9.1.1 and 9.4.

BIT(S)	MNEMONIC	MEANING AND OPERATION
15-08		Unused. Always read as zero.
07	LCM	Line Clock Monitor. This read-only bit is set by the leading edge of the external BEVENT line (or of one of the three on-board frequencies) and by Bus Initialize. LCM is cleared automatically on processor interrupts acknowledge. It is also cleared by writes to the LKS with bit <7> = "0".

BITS	MNEMONIC	MEANING AND OPERATION
06	LCIE	Line Clock Interrupt Enable -- This read-write bit, when set, causes the set condition of LCM (LKS <7>) to initiate a program interrupt request. When LCIE is clear, line clock interrupts are disabled. LCIE is cleared by Power Up and by Bus INIT. LCIE is held set when BCSR <13> (FRC LCIE) is set.
05-00		Unused. Always read as zeros.

10.3 Additional Specifications

Interrupt vector address: 100
Priority level: BR6

11.0 CONSOLE SERIAL LINE UNIT

11.1 Console Functionality

The console serial line provides the KDJ11-B processor with a serial interface for the console terminal. The console serial serial line is full duplex. It provides an RS-423 EIA interface which is also RS-232C compatible.

This serial line interface is based on the DC319 Digital Link Asynchronous Receiver Transmitter (DLART), described in Digital Purchase Specification A-PS-2117312-0-0.

The receive and transmit baud rates are always identical and are determined by three switches settings which can be asserted via directly, via three switches mounted on top of the KDJ11-B Module, or remotely, via an external connector which is also mounted at the top of the module. Each switch setting can be asserted by placing the switch in the "1" position or by grounding the appropriate external signal.

The Baud Rates are selected as follows:

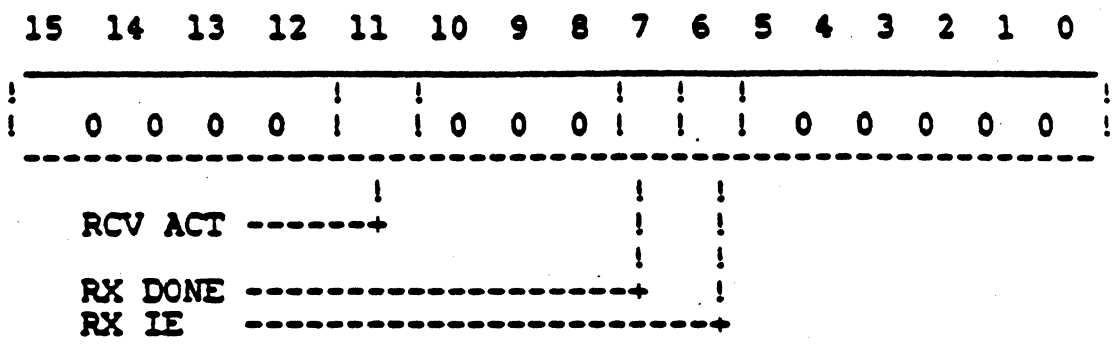
Switch Setting 02	01	00	Baud Rate
0	0	0	300
0	0	1	600
0	1	0	1200
0	1	1	2400
1	0	0	4800
1	0	1	9600
1	1	0	19200
1	1	1	38400

These switch settings, plus five additional switches settings (Switches 07-03), may be read via the Boot and Diagnostic Facility Configuration Register (BCR). If switch 07 is a "1" the Boot and Diagnostic Programs assumes that the system does not have a console terminal and uses switches 06-00 to select a limited range of KDJ11-B and system parameters. Setting switch 07 does not disable the console terminal interface which runs at the baud rate reflected by switches 02-00. The setting of these switches, however, is determined by system configuration considerations and may not correspond to a usable baud rate.

11.2 Console Registers

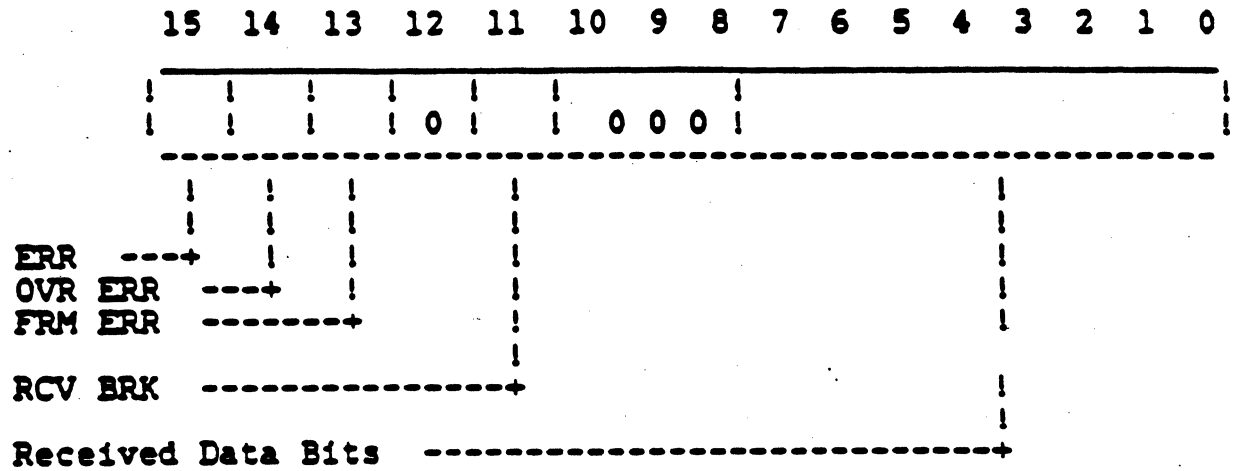
There are four console serial line unit registers: the Receiver Status Register, the Receiver Data Buffer, the Transmitter Status Register, and the Transmitter Data Buffer. Program recognition of these registers can not be disabled.

11.2.1 Receiver Status Register (RCSR address: 17 777 560)



BIT(S)	MNEMONIC	MEANING
15-12		Unused. Read as zeros.
11	RCV ACT	Receiver Active. This read-only bit is set at the center of the start bit of the serial input data and is cleared at the expected center (per DLART timing) of the stop bit at the end of the serial data. RX DONE is set one bit time after RCV ACT clears.
10-08		Unused. Read as zeros.
07	RX DONE	Receiver Done. This read-only bit is set when an entire character has been received and is ready to be read from the RBUF Register. This bit is automatically cleared when RBUF is read. It is also cleared by Power Up.
06	RX IE	Receiver Interrupt Enable. This read-write bit is cleared by Power Up and Bus INIT. If both RCVR DONE and RCVR INT ENE are set, a program interrupt is requested.
05-00		Unused. Read as zeros.

11.2.2 Receiver Data Buffer (RBUF address: 17 777 562)



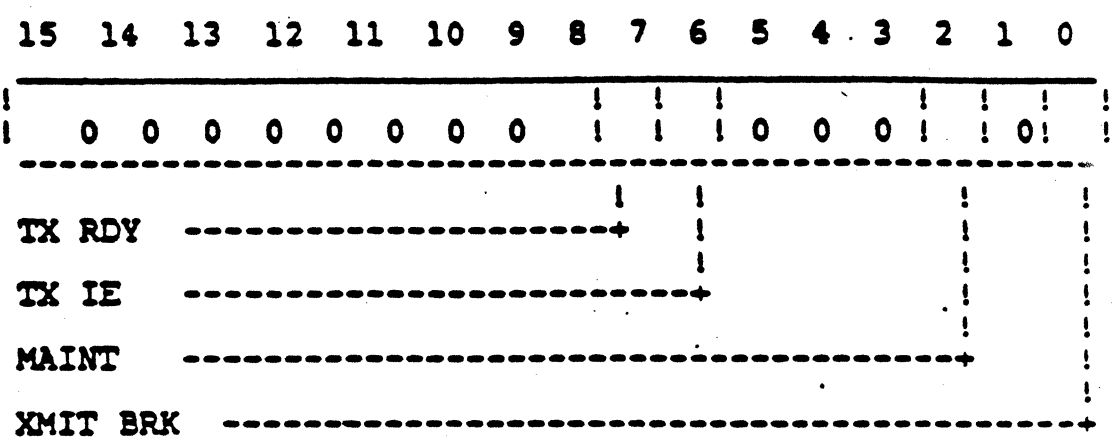
BIT(S)	MNEMONIC	MEANING
15	ERR	Error. This read-only bit is set if RBUF <14> or <13> is set. ERR is clear if these two bits are clear. This bit cannot generate a program interrupt.
14	OVR ERR	Overrun Error. This read-only bit is set if a previously received character was not read before being overwritten by the present character.
13	FRM ERR	Framing Error. This read-only bit is set if the present character had no valid stop bit. This bit is used to detect break.

NOTE: Error conditions remain present until the next character is received, at which point, the error bits are updated. The Error bits are not necessarily cleared by Power Up.

12		Unused. This bit always reads as "0".
11	RCV BRK	Received Break. This read-only bit is set at the end of a received character for which the serial data input remained in the SPACE condition for all 11 bit times. RCV BRK then remains set until the serial data input returns to the MARK condition.
10-08		Unused. These bits always read as "0".
07-00		Received Data Bits. These read-only bits contained the last receiv[illegible]

DOCUMENT NUMBER

11.2.3 Transmitter Status Register (XCSR address: 17 777 564)



BIT(S)	MNEMONIC	MEANING
15-08		Unused. Read as zeros.
07	TX RDY	Transmitter Ready. This read-only bit is cleared when XBUF is loaded and sets when XBUF can receive another character. XMT RDY is set by Power Up and by Bus INIT.
06	TX IE	Transmitter Interrupt Enable. This read-write bit is cleared by Power Up and by Bus INIT. If both TX RDY and TX IE are set, a program interrupt is requested.
05-03		Unused. Read as zeros.
02	MAINT	Maintenance. This read-write bit is used to facilitate a maintenance self-test. When MAINT is set, the external serial input is disconnected and the serial output is used as the serial input. This bit is cleared by Power Up and by Bus INIT.
01		Unused. Read as zero.
00	XMIT BRK.	Transmit Break. When this read-write bit is set, the serial output is forced to the SPACE CONDITION. XMIT BRK is cleared by Power Up and by Bus INIT.

11.2.4 Transmitter Data Buffer (XBUF Address: 17 777 566)

XBUF bits <15-08> are not used. XBUF bits <7-0> are write-only bits used to load the transmitted character.

11.3 Additional Specifications

Interrupt Vectors:	060	Receiver
	064	Transmitter
Interrupt Priority:	BR4	

11.4 Break Response

The KDJ11-B Console Serial Line Unit may be configured either to perform a halt operation or to have no response when a break condition is received. A halt operation will cause the processor to halt and enter the octal debugging technique (ODT) microcode. The Halt on Break Option is selected via bit 02 of the Boot and Diagnostic Controller Status Register. During power up, this bit is loaded from the Configuration Data by the Boot and Diagnostic ROM programs. For more information, refer to sections 9.1.1 and 9.4)

The DLART recognizes a break condition at the end of a received character for which the serial data input remained in the SPACE condition for all 11 bit times. The Break Recognition line remains asserted until the serial data input returns to the MARK condition.

APPENDIX 1 - KDJ11-A Base Instruction Set

Double Operand Instructions	ADD	BISB	MOV
	ASH	BIT	MOVB
	ASHC	BITB	MUL
	BIC	CMP	SUB
	BICB	CMPB	XOR
	BIS	DIV	
Single Operand Instructions	ADC	DEC	ROR
	ADCB	DECB	RORB
	ASL	INC	SBC
	ASLB	INCB	SBCB
	ASR	MFPS	SWAB
	ASRB	MTPS	SXT
	CLR	NEG	TST
	CLRB	NEGB	TSTB
	COM	ROL	
	COMB	ROLB	
Branch Instructions	BCC/BHIS	BHI	BNE
	BCS/BLO	BLE	BPL
	BEQ	BLOS	BR
	BGE	BLT	BVC
	BGT	BMI	BVS
Jump and Subroutine Instructions	CSM	JSR	RTS
	JMP	MARK	SOB
Trap and Interrupt Instructions	BPT	IOT	RTT
	EMT	RTI	TRAP
Miscellaneous Instructions	HALT	MFPT	RESET
	MFPD	MTPD	SPL
	MFPI	MTPI	WAIT
Condition Code Operators	CCC	CLZ	SEN
	CLC	NOP	SEV
	CLN	SCC	SEZ
	CLV	SEC	
Multiprocessor Instructions	TSTSET	WRTLCK	

APPENDIX 2 - KDJ11-A Floating Point Instruction Set

Floating Point Instructions			
	ABSD	LDCLF	STCDI
	ABSF	LDD	STCDL
	ADDD	LDEXP	STCFD
	ADDF	LDF	STCFI
	CFCC	LDFPS	STCFL
	CLRD	MODD	STD
	CLRF	MODF	STEXP
	CMPD	MULD	STF
	CMPF	MULF	STFPS
	DIVD	NEGD	STST
	DIVF	NEGF	SUBD
	LDCDF	SETD	SUBF
	LDCFD	SETF	TSTD
	LDCID	SETI	TSTF
	LDCIF	SETL	
	LDCLD	STCDF	

PPENDIX 3 - Base Instruction Timing

efer to DCJ 11 Micropocessor User's Guide
Documentation Number EK-DCJ11-UG)

APPENDIX 4 - Integral Floating Point Instruction Timing

Refer to DCJ 11 Micropocessor User's Guide
(Documentation Number EK-DCJ11-UG)

APPENDIX 5

KDJ11-B MODULE PIN ASSIGNMENTS

ROW A		ROW B		ROW C		ROW D	
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
AA1	BIRQ5 L	BA1	BDCOK H	CA1	NOT USED	DA1	NOT USED
AB1	BIRQ6 L	BB1	BPOK H	CB1	PSSEL L	DB1	PWTSTB L
AC1	BDAL16 L	BC1	BDAL18 L	CC1	SRUN L	DC1	PBYT L
AD1	BDAL17 L	BD1	BDAL19 L	CD1	PUBMEM L	DD1	PMAPE L
AE1	NOT USED	BE1	BDAL20 L	CE1	PBCYC L	DE1	NOT USED
AF1	SRUN L	BF1	BDAL21 L	CF1	PUBSYS L	DF1	NOT USED
AH1	NOT USED	BH1	BOOT EN L	CH1	PHBPAR L	DH1	NOT USED
AJ1	GND	BJ1	GND	CJ1	PSBFUL L	DJ1	NOT USED
AK1	NOT USED	BK1	NOT USED	CK1	PLBPAR L	DK1	NOT USED
AL1	NOT USED	BL1	NOT USED	CL1	NOT USED	DL1	NOT USED
AM1	GND	BM1	GND	CM1	PRDSTB L	DM1	NOT USED
AN1	BDMR L	BN1	BSACK L	CN1	NOT USED	DN1	CONSOLE LOCK L
AP1	BHALT L	BP1	BIRQ7 L	CP1	PBLKM L	DP1	NOT USED
AR1	BREF L	BR1	BEVENT L	CR1	PBSY L	DR1	NOT USED
AS1	NOT USED	BS1	NOT USED	CS1	NOT USED	DS1	NOT USED
AT1	GND	BT1	GND	CT1	GND	DT1	GND
AU1	+15V	BU1	NOT USED	CU1	NOT USED	DU1	NOT USED
AV1	NOT USED	BV1	+5V	CV1	PUBTMO L	DV1	NOT USED
AA2	+5V	BA2	+5V	CA2	+5V	DA2	+5V
AB2	NOT USED	BB2	NOT USED	CB2	NOT USED	DB2	NOT USED
AC2	GND	BC2	GND	CC2	GND	DC2	GND
AD2	+12V	BD2	+12V	CD2	NOT USED	DD2	NOT USED
AE2	BDOUT L	BE2	BDAL2 L	CE2	NOT USED	DE2	NOT USED
AF2	BRPLY L	BF2	BDAL3 L	CF2	NOT USED	DF2	NOT USED
AH2	BDIN L	BH2	BDAL4 L	CH2	NOT USED	DH2	NOT USED
AJ2	BSYNC L	BJ2	BDAL5 L	CJ2	NOT USED	DJ2	NOT USED
AK2	BWTBT L	BK2	BDAL6 L	CK2	NOT USED	DK2	NOT USED
AL2	BIRQ4 L	BL2	BDAL7 L	CL2	NOT USED	DL2	NOT USED
AM2	NOT USED	BM2	BDAL8 L	CM2	NOT USED	DM2	NOT USED
AN2	BIAK0 L	BN2	BDAL9 L	CN2	NOT USED	DN2	NOT USED
AP2	BBS7 L	BP2	BDAL10 L	CP2	NOT USED	DP2	NOT USED
AR2	NOT USED	BR2	BDAL11 L	CR2	NOT USED	DR2	NOT USED
AS2	BDMG0 L	BS2	BDAL12 L	CS2	NOT USED	DS2	NOT USED
AT2	BINIT L	BT2	BDAL13 L	CT2	NOT USED	DT2	NOT USED
AU2	BDAL0 L	BU2	BDAL14 L	CU2	NOT USED	DU2	NOT USED
AV2	BDAL1 L	BV2	BDAL15 L	CV2	NOT USED	DV2	NOT USED

APPENDIX 6

The following is the jumper summary for the KDJ11-B

JUMPER	FUNCTION
W10	(*) When IN, connects 614.4KHZ on board OSC. to SLU. When OUT, SLU inputs external OSC.
W20	(*) When IN KDJ11-B is in single processor mode. When OUT KDJ11-B is in multiprocessor slave mode.
W40	(*) when 2K EEPROM is used, TP40 connected to TP41. When 8K EEPROM is used, TP41 connected to TP42.

(*) = Manufacturing configured

APPENDIX 7 - PDP-11 Programming Differences

Refer to DCJ 11 Micropocessor User's Guide
(Documentation Number EK-DCJ11-UG)

APPENDIX 8 - Console Commands

Refer to DCJ 11 Micropocessor User's Guide
(Documentation Number EK-DCJ11-UG)

APPENDIX 9 - Micro-ODT Differences

Refer to DCJ 11 Micropocessor User's Guide
(Documentation Number EK-DCJ11-UG)

PPENDIX 10 - System Differences

efer to DCJ 11 Micropocessor User's Guide
Documentation Number EK-DCJ11-UG)