DEC-06-I5AA-D

INSTRUCTION MANUAL

DRUM PROCESSOR
TYPE 167

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PROPRIETARY DATA STATEMENT

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The 167 Drum Processor is designed to transfer data directly between an input/output device and the random access memory of a modular PDP-6 system. The drum processor can transfer characters of various sizes at a 4-mhz rate.

1.2 GENERAL DESCRIPTION

In systems using magnetic drums, the drum processor is normally housed in a single-bay cabinet, which also provides space for the Type 236 Magnetic Drum Control. The front panel of the cabinet displays register and status indicators, as shown in figure 1-1, and the cabinet contains an integral power supply and a cooling system. The logic circuits are packaged on standard DEC FLIP CHIP [TM] modules.

1.3 PERTINENT DOCUMENTS

The following documents are pertinent to the study of the material in this manual:

PDP-6 Handbook, F-65

Type 166 Central Processor Maintenance Manual, F-67

Digital System Modules Handbook

FLIP CHIP Modules Handbook

1.4 SPECIFICATIONS

Physical and electrical specifications for the drum processor are listed in section 3-1.

1.5 REFERENCE CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the reference conventions in this paragraph and chapter 6 will save considerable time and preserve thought continuity when reading the text that follows. Any reference to figure numbers or table numbers indicates that the illustration or table is located in text.

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All engineering drawings have a full drawing number. These drawings are included in chapter 6. In text, references to engineering drawings are abbreviated. For example:

Full drawing no. D-167-0-SBD

- SBD — Mnemonic identifier
- 0 — Drawing set identifier and no. in set
- D — Drawing original size

For this number, the first reference in text is 167-0-SBD; all subsequent references are -SBD.

CHAPTER 2
THEORY OF OPERATION

Discussion of the operation of the 167 Drum Processor (DP), for the purpose of this manual, begins with general system operations. These are illustrated by a DP system block diagram and a comprehensive flow diagram. Detailed treatment of functional units, with particular reference to the engineering drawings in the appendix, follows.

2.1 FUNCTIONAL DESCRIPTION

The primary functional units of the 167 DP in furnishing a direct memory path for high-speed input/output devices are represented in the following diagram (figure 2-1):

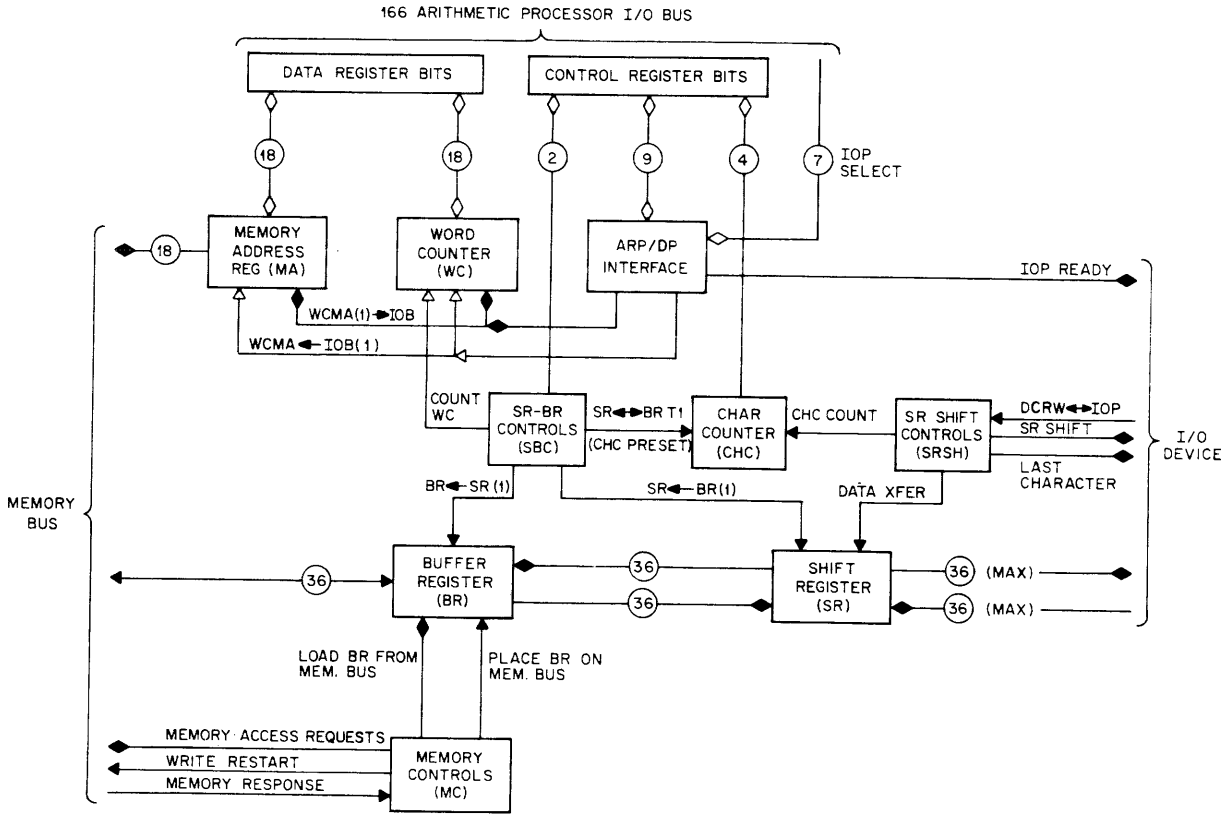
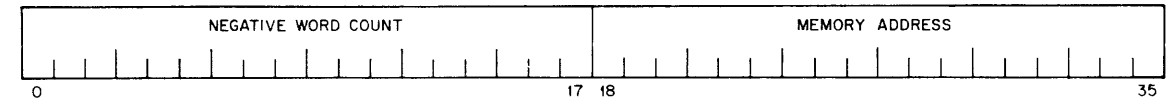


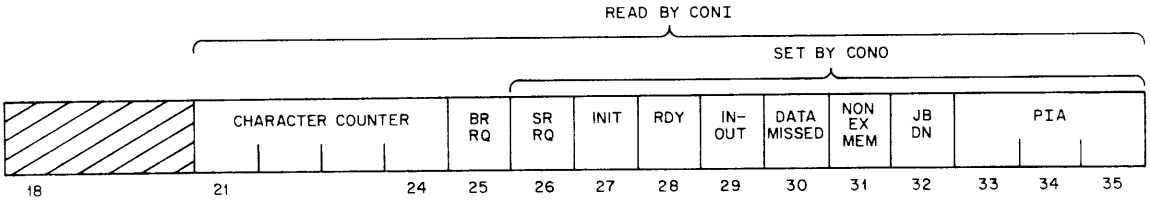
Figure 2-1 Type 167 Drum Processor System Block Diagram

In operation, the volume of data for transfer and the memory addresses for use in the transfer process are established in a 166 Arithmetic Processor (AP) program, noted below in chapter 4. (The data transfer continues asynchronously without regard for further attention from the program which may operate simultaneously in other memory areas.) When the transfer is complete, the 167 DP requests an interrupt. Its units perform the following functions:

a. Interface - The AP/DP interface section sets up the data transfer between the I/O device and system memory under control of the AP program. The interface contains bits 26-35 of the DP control register (figure 2-2), which can be examined by a CONI instruction or set by a CONO instruction. The significance of control register bits is explained in table 2-1 at the end this chapter.



A. DRUM PROCESSOR DATA REGISTER



B. DRUM PROCESSOR CONTROL REGISTER

Figure 2-2 Drum Processor Data and Control Registers

b. Memory Address Register (MA) - This 18-bit register controls the addressing of memory locations required for the data transfer operation, and is incremented by one with each word transferred. The memory address register comprises bits 18-35 of the DP data register (figure 2-2), and is loaded with the starting memory address by a DATAO or BLKO instruction.

c. Word Counter (WC) - This is an 18-bit register loaded with the negative of the number of words to be transferred by a DATAO or BLKO instruction, and is incremented by one with each word transferred. The word counter comprises bits 0-17 of the DP data register. The contents of the word counter and memory address registers may be read at any time by the AP program with a DATAI or BLKI instruction, provided that the RDY flag is reset.

d. Buffer Register (BR) - The buffer register buffers the flow of 36-bit words between the system memory and the shift register, in response to signals from the memory control and the SR-BR controls.

e. Shift Register (SR) - Characters or bytes from the I/O device are assembled into 36-bit words in the shift register for transfer to memory through the buffer register during a memory write operation. During a memory read operation, 36-bit memory words are disassembled in the shift register for character-sequential transfer to the I/O device. Bytes transferred between the DP and the I/O device may assume one of several sizes, as shown in table 3-1.

f. SR Shift Controls (SRSH) - The SR shift controls control word assembly and disassembly in the shift register, and synchronizes character transfer between the DP and the I/O device.

g. Character Counter (CHC) - The character counter counts the characters or bytes transferred between the DP and the external I/O device, to determine when one complete 36-bit word has been transferred. The contents of the character counter prior to each word transfer are determined by a plug-in card, wired to accommodate the number of I/O device characters that make up one memory word. The character counter forms bits 21-24 of the DP control register (figure 2-2), and may be examined by means of a CONI instruction.

h. SR-BR Controls (SBC) - The SBC controls the parallel transfer of 36-bit words between the shift register and the buffer register. Data word transfers are synchronized by the SR RQ and BR RQ flip-flops located within the SBC. These flip-flops form bits 25 and 26 of the DP control register (figure 2-2), and may be examined by a CONI instruction.

i. Memory Controls (MC) - The memory controls synchronize the flow of data between the buffer register and the system memory, and step the memory address register with each word transferred.

2.1.1 System Flow Diagram

In executing a programmed data transfer through the DP 167, as shown in the system flow diagram, drawing D-167-0-FD, the following principle phases are significant (the numbers in parentheses refer to the index numbers on the flow diagram):

a. Initializing the DP (1, 2, 3, 4)

b. Requesting memory access to transfer data between the DP and the system memory (5)

c. Transferring characters between the DP and the I/O device (7)

d. Internal transfer of the data word between the shift register and the buffer register (6)

In the initialization phase, the AP program may elect to read the control and data registers with CONI and DATAI instructions, respectively. Then, when the control and data words returned to the computer indicate that the DP is ready for a programmed data transfer, a CONO instruction may be issued. The CONO instruction causes the AP to send a CONO CLR pulse, followed by a CONO SET

pulse to the interface. The CONO CLR pulse clears the DP control register. The CONO SET pulse enables loading of the control register with the direction of the requested data transfer and the number of the priority interrupt line assigned to the DP by the program.

A DATAO instruction (index no. 4 on the flow chart) may now be issued to clear and reload the word counter and memory address registers, clear the JB DN flag, and enable presetting of the character counter. The system sets certain control flip-flops (explained in table 2-1), and branches to one of two control cycles, depending upon the requested direction of data transfer:

a. IN: Data from the I/O device is to be written into system memory. The first step is to accept sequential characters from the I/O device, and assemble them into a 36-bit word in the shift register (data transfer cycle).

b. OUT: Data is to be read from memory for disassembly and transfer to the I/O device. The first step is to request memory access to read one word (memory request cycle).

After one of the two cycles listed above is executed, a 36-bit data word is present in either the buffer register or the shift register, and the system moves to point 7 on the flow chart to transfer the word to the alternate internal register (BR or SR). The three word-transfer cycles thus generated operate as follows:

2.1.1.1 Memory Request Cycle (Index No. 5) - The memory request cycle is initiated by a transition of the BR RQ flip-flop to the set state. Logic for controlling the memory request cycle is shown in drawing D-167-0-MC. For a memory write operation, the DP sends a RQ CYC signal to memory, accompanied by a WR RQ signal. The core memory responds to the request by decoding the lines from the DP memory address register and initiating a write cycle at the resultant address. The memory then returns on address acknowledge (ADR ACK) pulse to the DP. The DP clears the RQ CYC flip-flop, steps the memory address, and sends a write restart (WR RS) pulse to memory, accompanied by data pulses on 36 lines.

For a memory read operation, the DP sends simultaneous RQ CYC and RD RQ signals to memory, and enables loading of the buffer register from the memory bus. If the memory responds with an ADR ACK within 100 μsec, the MA is stepped and the RQ CYC flag is cleared. A read restart pulse is sent from memory at MC T0 time, indicating that memory has transferred the word to the buffer register.

Data transfer in either direction is completed at MC T1 time, established by a delay line in the memory control section of the DP. The BR RQ and read-or-write request flags are cleared at this time.

2.1.1.2 Data Transfer Cycle (Index No. 5) - The presence of the IOP ~ BUSY level signals the I/O device to start sending or receiving characters. The I/O device responds with a DCRW ⟷ IOP pulse that causes the IOP to

a. assemble the sequential characters from the I/O device if a memory write operation is in progress; or

b. disassemble the 36-bit word in the SR for character-sequential transmission to the I/O device if a memory read operation is in progress.

The character counter is incremented with each character transferred, and the word assembly/disassembly process is stopped when the character counter reaches zero. The SR RQ flag is set at this time.

The word assembly/disassembly process is discussed in detail in the subsections on the buffer and shift registers, the shift register shift controls, and the character counter.

2.1.1.3 Internal Transfer Cycle (Index No. 7) - Word transfer between the buffer register and the shift register is initiated by either

a. a transition of the BR RQ flip-flop from 1 to 0 when the SR RQ flip-flop is in the set state, shown in drawing D-167-0-SBC, which indicates that the BR has been loaded from memory, and the DP responds by transferring the contents of the BR to the SR; or

b. a transition of the SR RQ flip-flop from 0 to 1 while the BR RQ flip-flop is in the set state, which indicates that the SR has been loaded from or unloaded by the I/O device, and the DP responds by transferring the contents of the SR to the BR.

Note that the set states of these request flip-flops (SR RQ and BR RQ) indicate that the corresponding register is ready to accept a word from the alternate internal register (SR or BR). Consequently, transitions of these flip-flops indicate that the corresponding register is ready to transfer a word to the alternate internal register.

The character counter is preset at the start of the internal word transfer cycle. The transfer is completed at time T1, and the INIT flag is checked. If the INIT flag is set, indicating that the first word has just been read from memory, the system transfers the contents of the BR to the SR, and branches to the data transfer cycle. If the INIT flag is clear, the word counter is incremented as the internal transfer is executed. If the word counter is equal to -1, the system sets the JB DN flag, and completes the word transfer operation in progress.

Note that in the output operation, the DP reads the next word from memory while the current word is being disassembled and transferred to the I/O device. Similarly, in the input operation, the DP begins assembly of the next word from the drum while the current word is being written into memory.

2.1.2 System Timing Diagram

A read/write timing diagram for the DP, operating in conjunction with a 163 Core Memory and a 236 Drum Control is shown on drawing D-167-0-RWT. The 236 Drum Control generates and accepts 4-bit characters. Note that the relatively slow word assembly/disassembly process governs the data rate.

The system timing diagram must be studied in connection with the previous description of the system flow chart, and referenced as necessary in the discussions of functional units that follow.

2.2 DETAILS OF FUNCTIONAL UNITS

2.2.1 AP/DP Interface

The communication link between the AP and the DP is set up in the interface section, shown in drawings D-167-0-IOPI 1, 2. Each control signal to the interface (CONO CLR, CONO SET, DATAO CLR, DATAO SET, DATAI, CONI) is accompanied by the DP selection code, formed by the program in bits 3-9 of the I/O instruction word. The selection code is interpreted in the interface, which generates an enabling level, and permits an exchange of data between the control and data registers and the AP.

The interface section contains nine flip-flops, which comprise bits 27-35 of the DP control register (refer to figure 2-2 and table 2-1). The three PIA flip-flops store the number of the priority interrupt line assigned to the DP by the AP program. This number is decoded by a binary-to-octal decoder (A2 and B2), to enable a transition on one of the seven PIA lines whenever one of the three interrupt flip-flops (DATA MISSED, NON EX MEM, JB DN) is set.

2.2.2 Word Counter (WC)

The word counter (drawings D-167-0-WC 1, 2) is an 18-bit register that comprises bits 0-17 of the DP data register. The word counter is loaded from the I/O bus by a DATAO SET pulse to the interface with the number of words to be transferred in negative, 2's complement form. (Thus, three would be represented as octal 777775, and decimal 310 would be represented as octal 777324.) The counter is stepped with each word transferred by a count pulse from the SBC. The count pulse toggles all flip-flops that have been enabled by their associated interstage NAND gates (A18, A24, and A30). Each NAND gate monitors the states of all less significant flip-flops to inhibit toggling of its associated flip-flop until the previous stages have reached their maximum count.

When the word counter reaches -1, a logic level transition is generated at terminal T of A18 to signal the SBC that the last data word is in the DP.

Signals from the interface provide for clearing the word counter (WCMA ← 0), loading the word counter from the I/O bus (WCMA ← IOB(1)), and placing the contents of the word counter on the I/O bus (WCMA (1)→ IOB).

2.2.3 Memory Address Register (MA)

The 18-bit memory address register and its associated memory bus drivers are shown in drawings D-167-0-MA 1, 2, and D-167-0-MAI. The memory address register comprises bits 18-35 of the DP data register. The memory address register is a binary counter similar to the word counter, and is stepped with each data word transferred by count pulses from the memory controls. Signals from the interface clear the word counter, load the word counter from the I/O bus, and place the contents of the word counter on the I/O bus. The contents of the memory address register are statically available to memory via the memory bus.

2.2.4 Buffer (BR) and Shift (SR) Registers

The buffer register and shift register (drawings BRSR 1- 4) buffer the flow of data through the DP under control of signals from the SR-BR controls (drawing SBC), SR shift controls (drawing SRSH), and the memory controls (drawing MC).

The SRSH DATA XFER pulse transfers characters of up to 36 bits from the I/O device to the shift register. To implement an output operation, characters of less than 36 bits must be transferred to the low-order stages of the shift register from the I/O device. Conversely, to implement an output operation, characters of less than 36 bits must be accepted by the I/O device from the high-order stages of the shift register. If, for example, the 236 Drum Control is the I/O device, and data is to be written into memory, the first 4-bit character will be loaded into stages 32-35 of the shift register. The first shift pulse from the SR shift controls (SR SH 4) will transfer this character to SR stages 28-31, to permit loading the next character into stages 32-35, and so on.

The shift register is also capable of shifting on increments of three bits (SR SH 3). Shift register control is discussed below. Signals controlling parallel data word transfers are as follows:

Signal Designation	Origin	Effect
MEM BUS ← BR LT(1)	MC	Contents of BR to memory
MEM BUS EN LT	MC	Memory data word allowed to enter BR
BR ← SR(1)	SBC	Contents of SR to BR
SR ← BR(1)	SBC	Contents of BR to SR

2.2.5 Shift Register Shift Controls (SRSH)

The SRSH shift controls (drawing D-167-0-SRSH) send shift pulses to the SR to control assembly/disassembly of 36-bit data words for transfer between the I/O device and the DP. The SR is shifted in increments of either three or four bits, and at intervals of 100 nsec. Five shift pulses (SRSH T0 - SRSH T4) are available to position each chracter or byte within the shift register, either for character transfer to the I/O device or for word assembly and transfer to the buffer register.

The number of shift pulses used for positioning each byte and the shift line selected for each pulse (SRSH 3 or SRSH 4) are determined by a module. The wiring of the module for the several possible modes of operation is shown on the referenced drawing. The drawing also includes a table showing the shift pulses generated by the SRSH controls for each mode. All five shift pulses, for example, are used to position an 18-bit character within the shift register. The first three pulses are applied on the SH4 line, and the next three pulses are applied on the SH3 line, for a total shift of 18 positions.

A pulse designated DCRW⟷IOP is sent from the I/O device to initiate each shift cycle. During an input operation, this pulse gives rise to a DATA XFER pulse, which loads the shift register with a character from the I/O device. During an output operation, the DCRW⟷IOP pulse indicates that the I/O device has accepted the character placed on the data lines by the IOP.

A pulse is generated to step the character counter after each character is positioned in the shift register. The SHIFT flip-flop is reset at this time, causing the DP to generate a transition on the IOP~BUSY line. This informs the I/O device that the DP is ready for another character, if an operation is in progress.

2.2.6 Character Counter (CHC)

The character counter (drawing D-167-0-CHC) counts down with each character transferred between the DP and the I/O device. When the character counter reaches zero, a CHC = 0 signal is generated, to signal the SBC that the word assembly/disassembly and transfer between the SR and the I/O device is complete. The character counter is preset to the number of characters per word, minus one, by a pulse from the SBC prior to each word transfer operation between the DP and the external device. The number loaded into the character counter is determined by a plug-in module. Wiring of the plug-in module to implement the several possible modes of operation is shown in a table appearing on the referenced drawing.

The character counter forms bits 21-24 of the DP control register, and may be examined by a CONI instruction.

2.2.7 SR-BR Controls

The shift register and buffer register (SBC) controls monitor the status of the buffer register and the shift register to determine

a. If the BR is ready to accept a word from memory

b. If the BR is ready to send a word to memory

c. If the SR is ready to accept a word from the BR

d. If the SR is ready to send a word to the BR

The SR-BR controls contain the SR RQ and BR RQ flip-flops, which define the ready states of the buffer register and the shift register. The sequencing of the SR RQ and BR RQ flip-flops as the DP executes word transfer operations is covered previously in this section in the discussion of the system flow diagram.

The SR-BR controls contain a timing generator, consisting of one 100 nHz delay. The generator times the internal transfer cycle, described earlier in this section and illustrated in the system flow diagram. The SBC also contains logic for clearing the BR and the SR, enabling BR/SR transfer, enabling character counter preset, and stepping the word counter.

2.2.8 Memory Controls (MC)

The memory controls (drawing D-167-0-MC) synchronize the exchange of data words between the buffer register and system memory, and generate a count pulse to step the memory address register with each word transferred. The memory controls execute the memory request cycle, discussed earlier in this section and illustrated in the system flow diagram.

TABLE 2-1 EXPLANATION OF CONTROL REGISTER BITS

Bits	Name	Function
21-24	CHC	Character counter. Contains one less than the number of bytes necessary to complete the current word transfer. Preset to the number of bytes/word minus one for each new word, and is counted down for each byte transferred.
25	BR RQ	Buffer register request. Set on input to memory each time a word has been transferred from the shift register to the buffer register, and reset when the word is accepted by memory. Set on output when initializing, and each time a word is sent to the shift register, unless the word transferred was the last one. Reset when a new word arrives from memory.
26	SR RQ	Shift register request. Set on output from memory when initializing, and when shift register is emptied. Reset when the shift register is reloaded from the buffer register. Set on input when shift register is full, and reset when shift register contents have been transferred to the buffer register. This bit may be set by the AP program to force a jam transfer between the BR and the SR.
27	INIT	Initialize. Set by a DATAO on output. Reset by RDY turning on. Causes first word to be read from memory. Always reset on input to memory.
28	RDY	Ready. Indicates DP ready to transmit data to/from the I/O device. Set on input by a DATAO, and on output by first word arriving in shift register. Reset by occurrence of an interrupt condition (JB DN, NON EX MEM, or DATA MISSED).
29	IN/OUT	A 1 indicates output to the device; 0 indicates input to the memory.
30	DATA MISSED	Set if I/O device attempts to transfer a byte when SR RQ is on. Requests interrupt and turn off RDY.
31	NON EX MEM	Set if non-existent memory location is addressed, or if a memory cycle cannot be obtained within 100 μsec after requested. Requests interrupt and turns off RDY.
32	JB DN	Set when last word has been transferred to the DP on input or output. If an input operation is in progress, the last word will be written into memory before interrupt is acknowledged, provided that the DP has at least as high a memory access priority as the AP. Otherwise, it may be necessary to wait for the BR RQ to clear before issuing another CONO or DATAO to the DP. The JB DN flag requests an interrupt, and may be reset by a DATAO.
33-35	PIA	Priority interrupt assignment. Specifies which of seven program interrupt lines is to be used to inform the AP of an interrupt condition.

CHAPTER 3
INSTALLATION AND INTERFACE

3.1 SPECIFICATIONS FOR 167 DRUM PROCESSOR

The physical and electrical specifications for the processor are listed below.

Dimensions	23-1/2 inches wide 27-1/16 inches deep 69-1/8 inches high
Weight	
Cabinet	160 lbs.
Logic	84
728 Power Supply	20
836 Power Control	18
Indicator panels and blank panels	30
Total	312
Service clearances	8-3/4 inches in front, 14-3/4 inches in back
Color	Raffi and Swansen Tweed, DEC Blue #5150-565
Power	115 vac 60 cps 3-wire single phase; 6-amp starting current, 4-amp operating current
Ambient temperature	50-105° F
Signal cables	8 Type W028 I/O Bus Cables 8 Type W028 Memory Bus Cables 7 Type W020 Indicator Cables 9 Type W028 DP Interface Cables (Lengths of all types above dependent upon system configuration.)

3.2 INSTALLATION

The drum processor requires 115v, single-phase, 60-cps power, and must be operated within an environment defined in section 3.1. Locations of cable connectors are shown in drawing D-167-0-IOCD.

Jumpers on modules on the DP determine the number of characters or bytes from the I/O device that make up one memory word and the number of shifts required to position each byte for transfer between the DP and the I/O device. The modules are normally wired before shipment of the unit. Module wiring is shown in drawing D-167-0-SRSH. The data rates for the several possible byte sizes are shown in table 3-1.

TABLE 3-1 DATA RATES FOR VARIOUS BYTE SIZES

Byte Size	Bytes per Word	Min. Time Between Bytes	Max. Byte Rate
3	12	250 nsec	4.0 hz
4	9	250 nsec	4.0 hz
6	6	350 nsec	2.86 hz
7	5	350 nsec	2.86 hz
8	4	350 nsec	2.86 hz
9	4	400 nsec	2.5 hz
10-12	3	400 nsec	2.5 hz
13-16	2	500 nsec	2.0 hz
17-18	2	600 nsec	1.67 hz
36	1	250 nsec*	4.0 hz

3.3 INTERFACE

Drawing D-167-0-IOSD gives a functional picture of all signals passing between the DP and the AP, the core memory, and the connected I/O device. Drawing D-167-0-IODI shows the pin assignments for each of the interface signals between the DP and the I/O device. In table 3-2, functions of all interface signals are explained.

* Limited also by memory speed.

TABLE 3-2 167 DP INTERFACE SIGNALS

Type	Name	Function
	POWER ON -15v	Turn on DP power. Present whenever AP power is on.
	POWER RESET	Clears control register. Present (a) Whenever the I/O reset key on the computer console is pressed. (b) Whenever the program gives a CONO instruction to the priority interrupt system to clear the system. (c) Whenenver the power is turned on.
Signals Between 166 AP and 167 DP	IOS 3-9 (0/1)	Carry 167 selection code. Set up 1 μsec before any other command signal occurs.
	DATAO CLR,	Sequential pulses generated by DATAO command.
	DATAO SET	Clears and loads data register.
	CONO CLR,	Sequential pulses generated by CONO command.
	CONO SET	Clears and loads control register.
	IOB ← DATA	Places data register bits on I/O bus.
	IOB ← STATUS	Places control register on I/O bus.
	PIA 1-7	A signal is present on one of these lines when an interrupt request occurs.
	IOB 0-35	AP input/output bus lines.
	DCRW⟷IOP	Indicates I/O device is ready to send/receive one character (byte).
Signals Between DP and I/O Device Note All data levels are -3v for a logic 1.	IOP READY	Data is available at the DP, or the DP is ready to accept data.
	SR LAST CHAR	Sent by DP to indicate DP has only two characters to send or receive to complete operation in progress.
	IOP ~BUSY	Signals I/O device whether an I/O operation is in progress.
	DATA IN 0-35	Input data lines available to I/O device.
	DATA OUT 0-35	Output data lines available to I/O device.

TABLE 3-2 167 DP INTERFACE SIGNALS (continued)

Type	Name	Function
Signals Between DP and Memory	RQ CYC	Read cycle-DP requests memory access for a read or write operation.
	RD RQ	Read request-DP requests memory read operation.
	WR RQ	Write request-DP requests memory write operation.
	ADR ACK	Address acknowledge-returned by memory within 0.2 μsec in response to RQ CYC signal if memory module is free.
	RD RS	Read restart-indicates memory has transferred one word to DP (sent by memory).
	WR RS	Write restart-sent by DP to indicate that next word is available.
	MA (18-35)	Memory address lines from DP.
	MB (0-35)	Memory bus lines for bidirectional transfer of data.

CHAPTER 4
OPERATION AND PROGRAMMING

4.1 PROGRAMMING

The AP program must condition the DP for a data transfer before initializing the connected I/O device. The DP is set up by a CONO instruction to specify the direction of data transfer, followed by a DATAO instruction specifying the number of words to be transferred and the initial memory address selected for the transfer. (See figure 2-2 for the configurations of the DP control and data registers.)

As an example, the following symbolic instructions may be used to set up the DP for output:

```
CONO    DP,    OUT
DATAO   DP,    WCMA
```

The location OUT might contain the octal configuration 101, to set the DP output bit and allocate priority interrupt channel number 1 for the DP. Similarly, location WCMA contains the desired word count in negative 2's complement form, plus the first memory address to be used. The mnemonic DP causes the PDP-6 assembler (MACRO-6) to generate the DP selection code in bits 3-9 of the CONO and DATAO instruction words.

The AP program to service DP interrupts should include a CONI instruction to enable examination of bits 30, 31, and 32 of the DP control register. The program can then respond appropriately to the condition that caused the interrupt (DATA MISSED, NON EX MEM, or JB DN).

CHAPTER 5
MAINTENANCE

Since the Type 167 Drum Processor must operate with a Data Processor Type 166, a full knowledge and understanding of the descriptions of chapter 9 of Type 166 Arithmetic Processor Maintenance Manual form the basis of maintenance instructions. Many of the drum processor maintenance procedures can be conducted using Maindec programs associated with the 166.

Suggested tools and test equipment suitable for use while performing maintenance procedures on the 167 Drum Processor are listed in chapter 9 of the Type 166 Maintenance Manual. The principal maintenance tool is a detailed understanding of the principles of operation of the drum processor, as outlined in chapter 2 of this manual. Diagnostic programs (Maindecs) are provided to check on-line operation of the DP. For more specific checks, the maintenance technician may use the PDP-6 console controls and indicators to exercise the communication links between the DP and the AP, the DP and the system memory, and the DP and the connected I/O device. The DP front panel indicators allow visual monitoring of the DP registers as instructions are executed in the single step mode.

CHAPTER 6
ENGINEERING DRAWINGS

This section contains reduced copies of the engineering drawings and replacement schematics required for understanding and maintaining the 167 Drum Processor. These reduced copies are in addition to the complete set of full-size drawings forwarded with each DP. Maintenance personnel should use only the full-size drawings for work on units. The replacement schematics are furnished only for test and maintenance purposes. These circuits are proprietary in nature and should be treated accordingly.

6.1 CIRCUIT SYMBOLS

The block schematics of DEC equipment are multipurpose drawings that combine signal flow, logical function, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those appearing in "The Digital Logic Handbook" but are often simplified. Figure 6-1 illustrates some of the symbols used in the DEC engineering drawings for the 167 Drum Processor.

6.1.1 Logic Levels

The standard DEC logic level is either ground (0 to −0.3v) or −3v (−2.5 to 3.5v). DEC logic levels are indicated by an open diamond (——◇) for a ground level and by a closed diamond (——◆) for a negative (−3v) level. The DEC logic symbols shown at the inputs of most circuits indicate the enabling conditions required to produce a desired output; e.g., an open diamond at a circuit input indicates that a ground level is required to produce the desired output.

6.1.2 FLIP CHIP Pulse

Two types of pulses, R series and B series, are used in FLIP CHIP circuit operation. The pulse produced by R-series modules (see figure 6-2) starts at −3v, goes to ground (−0.2v) for 100 nsec, then returns to −3v.

The B-series negative pulse is 2.5v in amplitude and 40 nsec in width as shown in figure 6-3. If this pulse is applied to the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series pulse.

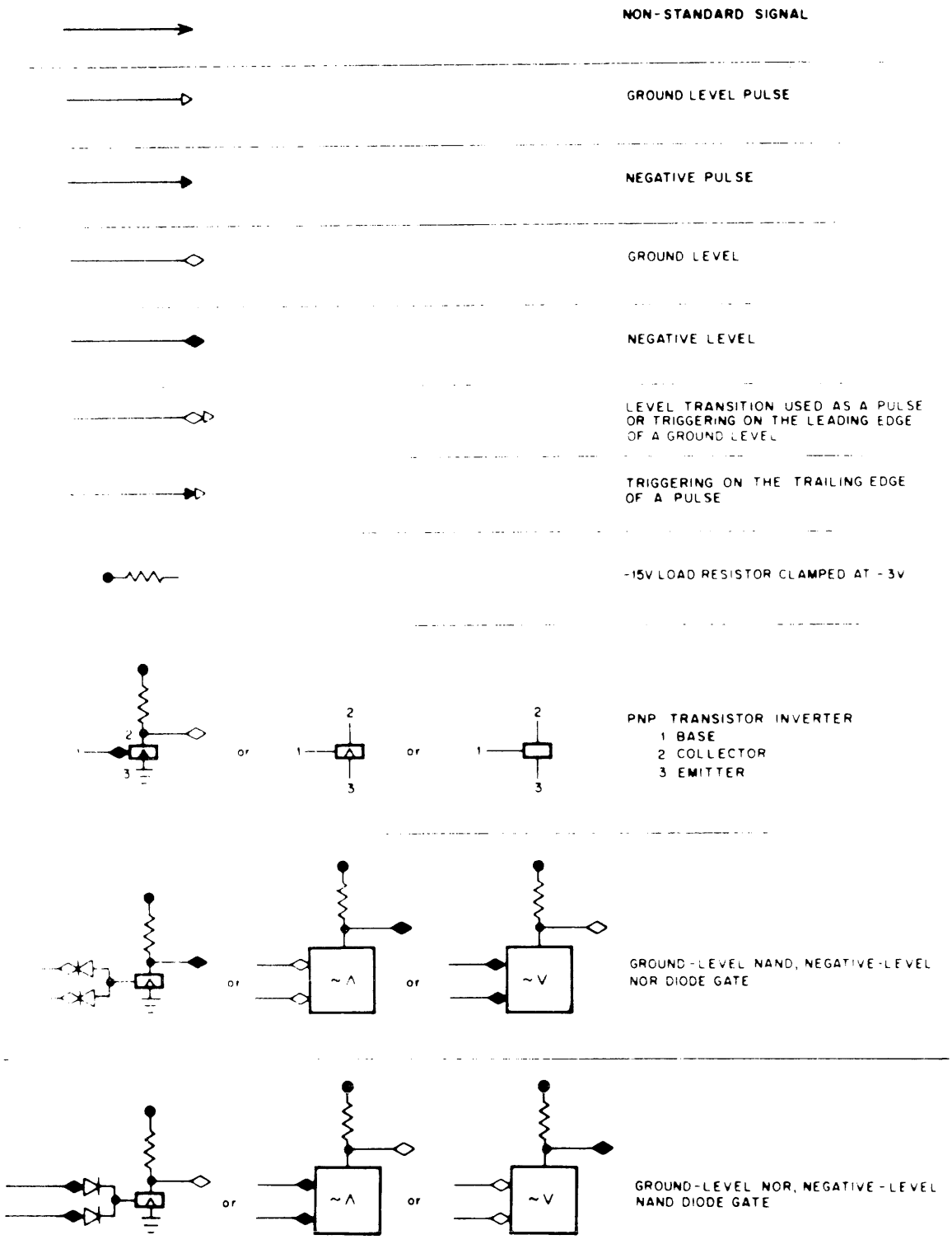
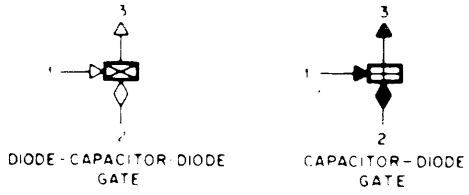
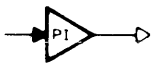


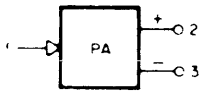
Figure 6-1 DEC Symbols



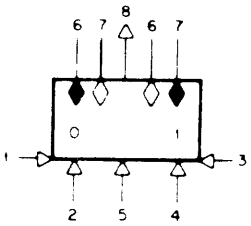
1. PULSE INPUT
2 CONDITIONING LEVEL INPUT
3 PULSE OUTPUT



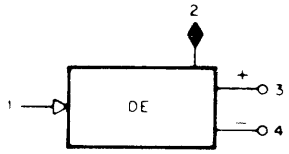
PULSE INVERTER



PULSE AMPLIFIER
1 PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3 TRANSFORMER-COUPLED PULSE OUTPUT EITHER TERMINAL MAY BE GROUNDED



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1 DIRECT CLEAR INPUT
2 GATED-CLEAR INPUT
3 DIRECT-SET INPUT
4 GATED-SET INPUT
5 COMPLEMENT INPUT
6 OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7 OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8 CARRY PULSE OUTPUT, UPON BEING CLEARED



DELAY (ONE-SHOT MULTIVIBRATOR)
1 INPUT PULSE
2 OUTPUT LEVEL, -3 V DURING DELAY
3,4 TRANSFORMER-COUPLED PULSE OUTPUT EITHER TERMINAL MAY BE GROUNDED

Figure 6-1 DEC Symbols (continued)

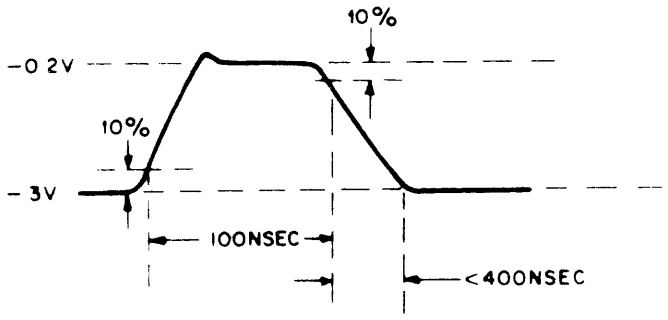


Figure 6-2 FLIP CHIP R-Series Standard Pulse

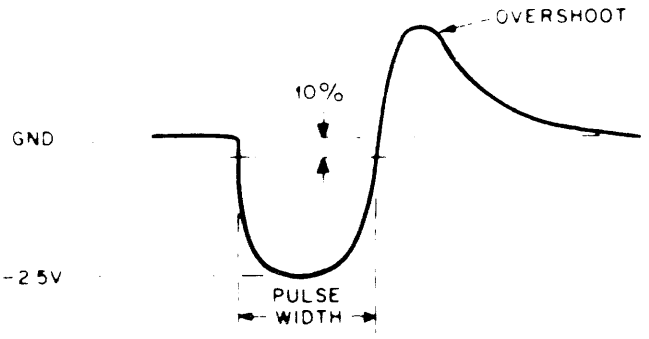


Figure 6-3 FLIP CHIP B-Series Standard Pulse

6.2 DEC ENGINEERING DRAWING CONVENTIONS

6.2.1 Coordinate System

DEC engineering drawings are subdivided into zones bounded by horizontal sections A through D and vertical sections 1 through 8. Circuit locations are referenced by a numeral(s)- letter-numeral combination (e.g., 3A3). The first numeral is the last number of the drawing number; the letter-numeral combination (e.g., A3) designates the module location in drawing coordinates.

6.2.2 Module Identification and Symbology

Circuits enclosed by dotted lines on the engineering drawings are FLIP CHIP modules and are labeled on the drawings by two 4-character designations. The upper designation (i.e., a letter followed by three numerals) specifies the module type as listed in DEC catalog C-105, "The Digital Logic Handbook." The lower 4-character designation indicates the location of the module. In this designation,

the first character (sometimes omitted) is a numeral specifying the number of the bay that contains the equipment; the second character is a letter indicating the mounting panel; the third and fourth characters are numerals indicating the module location from left to right within a specified panel. Individual module pins are labeled from top to bottom by the letters A through Z (excluding letters G, I, O, and Q). Pin letters on logic diagrams are written near their respective terminals. On flow charts and timing diagrams, pin designations are formed by adding the pin letter to the module location code; e.g., 2M10H indicates pin H of module 10 in panel M of bay 2.

Figure 6-4 is an example illustrating module identification, DEC symbols and nomenclature on engineering drawings. The module shown is a Type R202 Flip-flop and is located in the twelfth slot from the left (when viewed from the wiring side) of row B (the second row of modules from the top). The symbol marked FF is a flip-flop with two complementary outputs, terminals S and T. The output of terminal S is connected to terminals D18F and B6M, while the output at terminal T is connected to terminal A3C.

In the 0 state, terminal S is at −3v and terminal T is at ground (as shown by the diamonds inside the symbol at the left). The −3v output is the enabling condition for D18F (SAFE signal) and is also the disabling level for B6M. The ground level at terminal T is a disabling condition for A3C. In the 1 state, terminal T is at −3v and terminal S is at ground (as shown by the diamonds at the right). The ground level is enabling condition for B6M ($\overline{\text{SAFE}}$) and is also a disabling level for D18F. The −3v at terminal T is the enabling for A3C (GO).

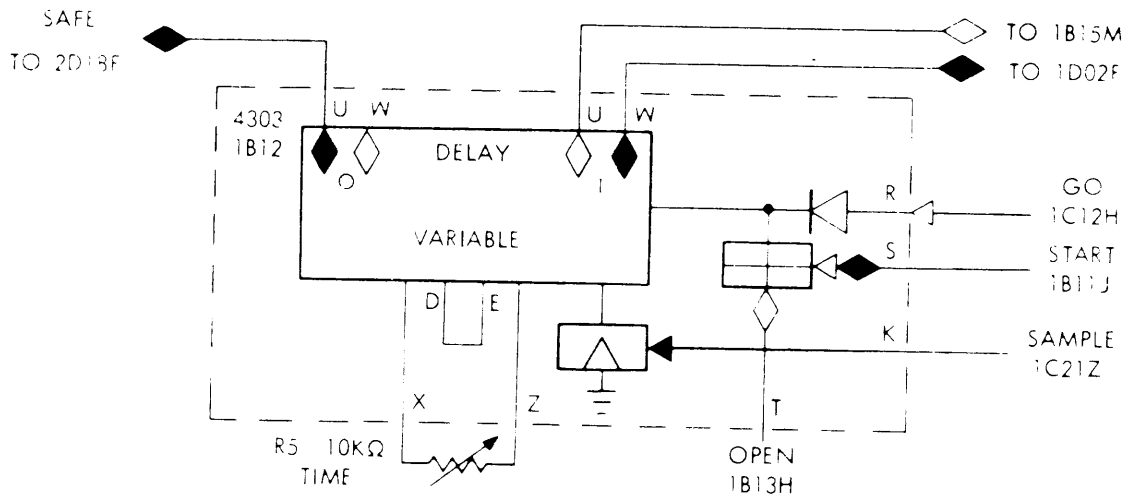


Figure 6-4 Typical DEC Logic Symbology

Ti flip-flop is triggered to the 1 state through its DCD (diode-capacitor-diode) set gate. The two ground-level enabling inputs to this gate are the START pulse (applied to pulse-input terminal B12U) and the OPEN signal (applied to level-input terminal B12V). The OPEN signal must be present for at least 400 nsec before the START pulse can enable the DCD gate to set the flip-flop. The START pulse comes from terminal B11J, and the OPEN signal from terminal C21C.

The flip-flop is cleared to the 0 state either through its DCD reset gate or through its direct-clear input terminal. Since the level-input terminal (B12P) of the DCD gate is permanently grounded, the flip-flop is cleared whenever the RST pulse arrives at terminal B12N. This pulse is received from terminal F4A. The flip-flop is also cleared by the CLR pulse which arrives at direct-clear B12R from D6B.

6.3 REPLACEMENT SCHEMATICS

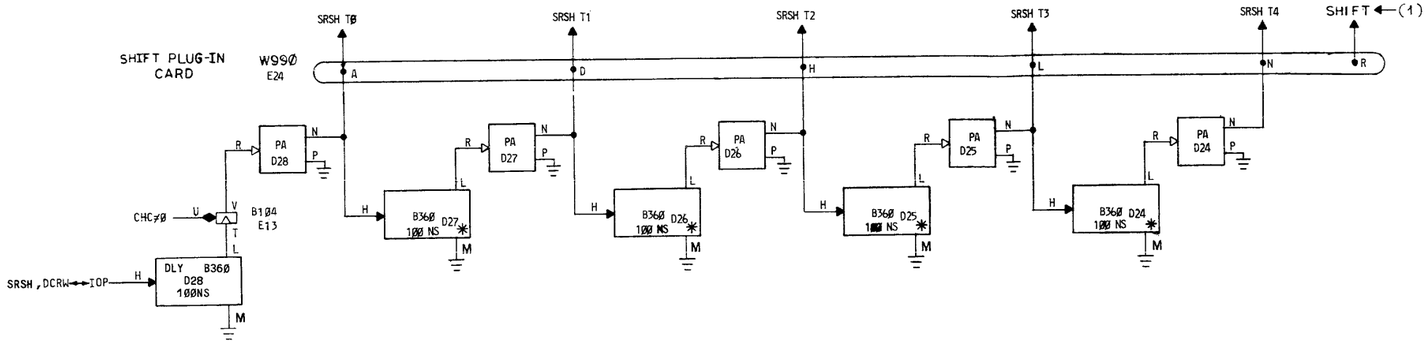
Drawing numbers for replacement schematics are formed by a letter-numeral combination as follows: RS-(letter)-(3 or 4 numerals). The letter indicates the drawing size, and the numerals indicate the circuit type. Another numeral to the right of these numerals indicates the number of the revision, while a letter to the left indicates the circuit board revision. This revision letter is etched on the circuit board and embossed after the type numbers on the aluminum frame of the module.

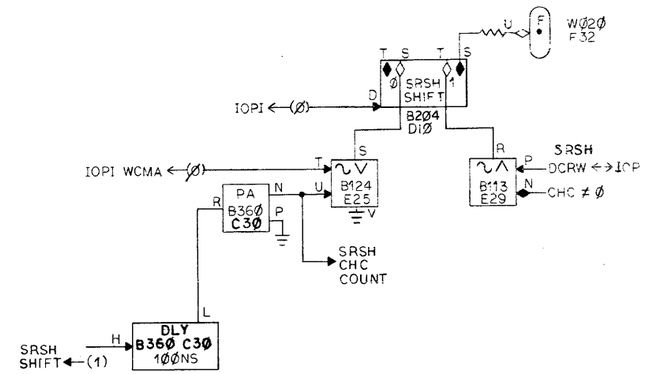
6.3.1 Semiconductor Substitution

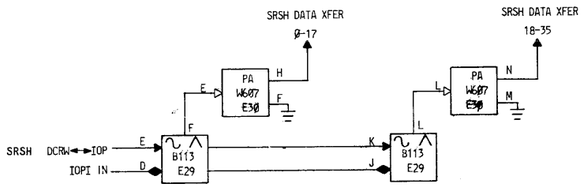
Standard EIA components specified in table 6-1 can replace the majority of DEC semiconductors used in modules of the drum processor. Exact replacement is recommended for semiconductors not listed.

TABLE 6-1 SEMICONDUCTOR SUBSTITUTION

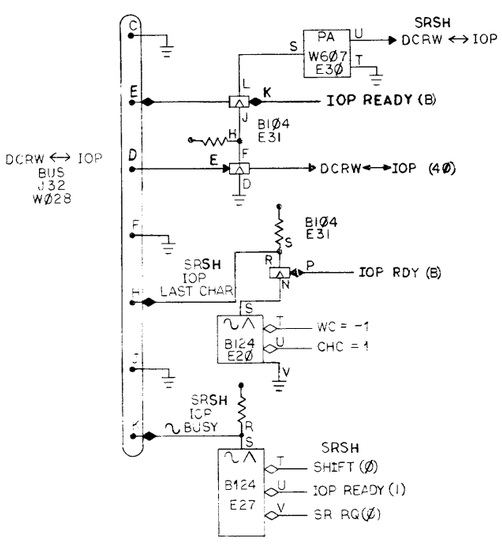
DEC	EIA	DEC	EIA
D662	1N645	DEC2894-3B	DEC2894-3A
D664	1N3606	D3009	2N3009
D668	Two 1N3606 in series	DEC3639,-0	2N3639
DEC2219	2N2219	DEC3639B	2N3639
DEC2894,-1,-2,-3	DEC2894		

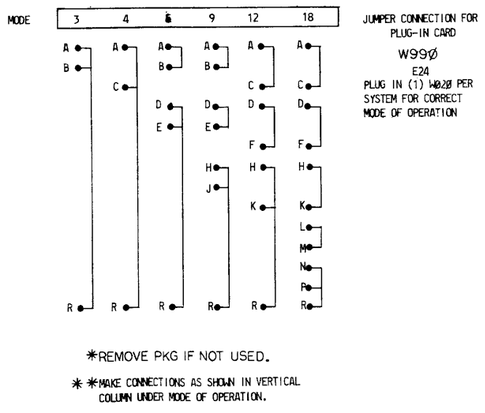






MODE	TØ	T1	T2	T3	T4
3	3				
4	4				
6	3	3			
9	3	3	3		
12	4	4	4		
18	4	4	4	3	3

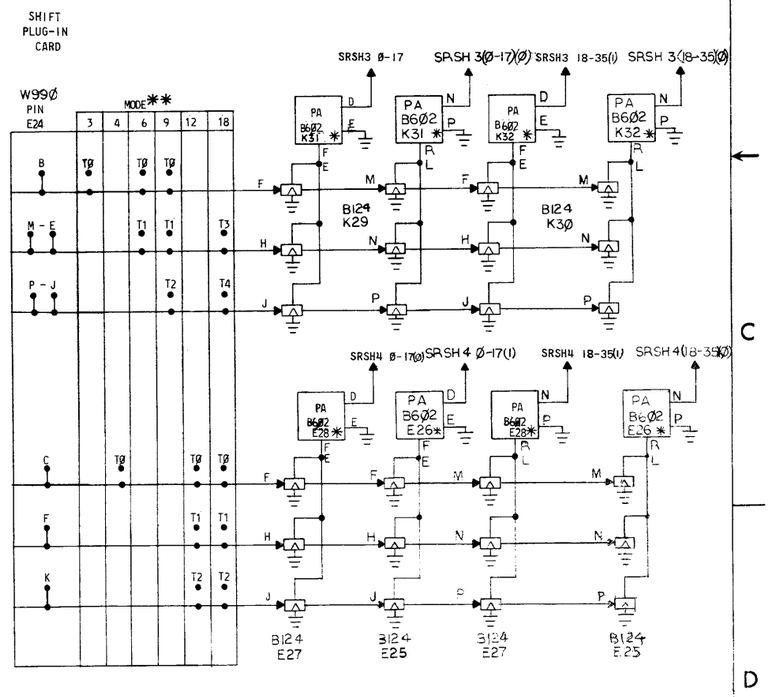




JUMPER CONNECTION FOR PLUG-IN CARD W99Ø E24 PLUG IN (1) W2Ø PER SYSTEM FOR CORRECT MODE OF OPERATION

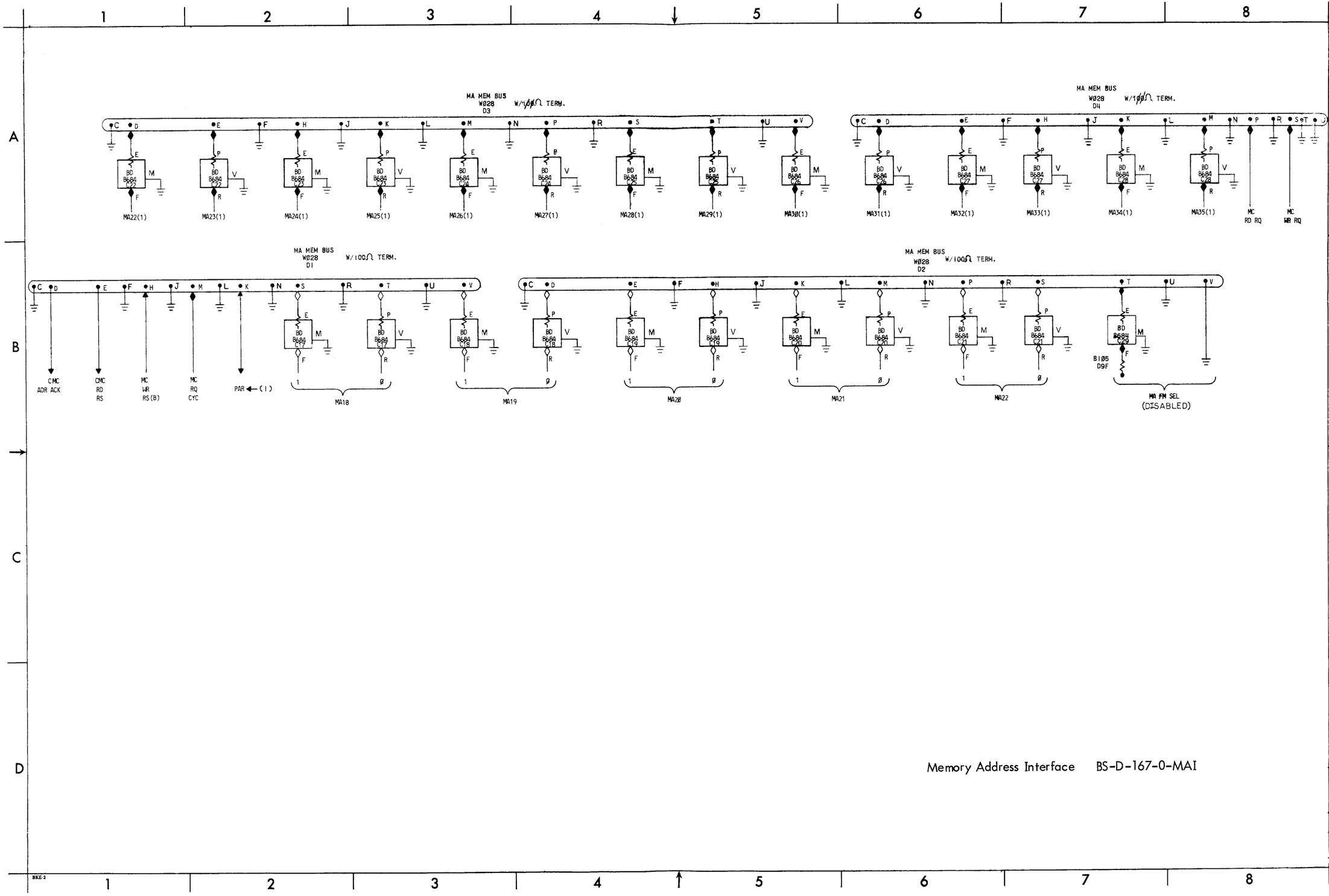
*REMOVE PKG IF NOT USED.

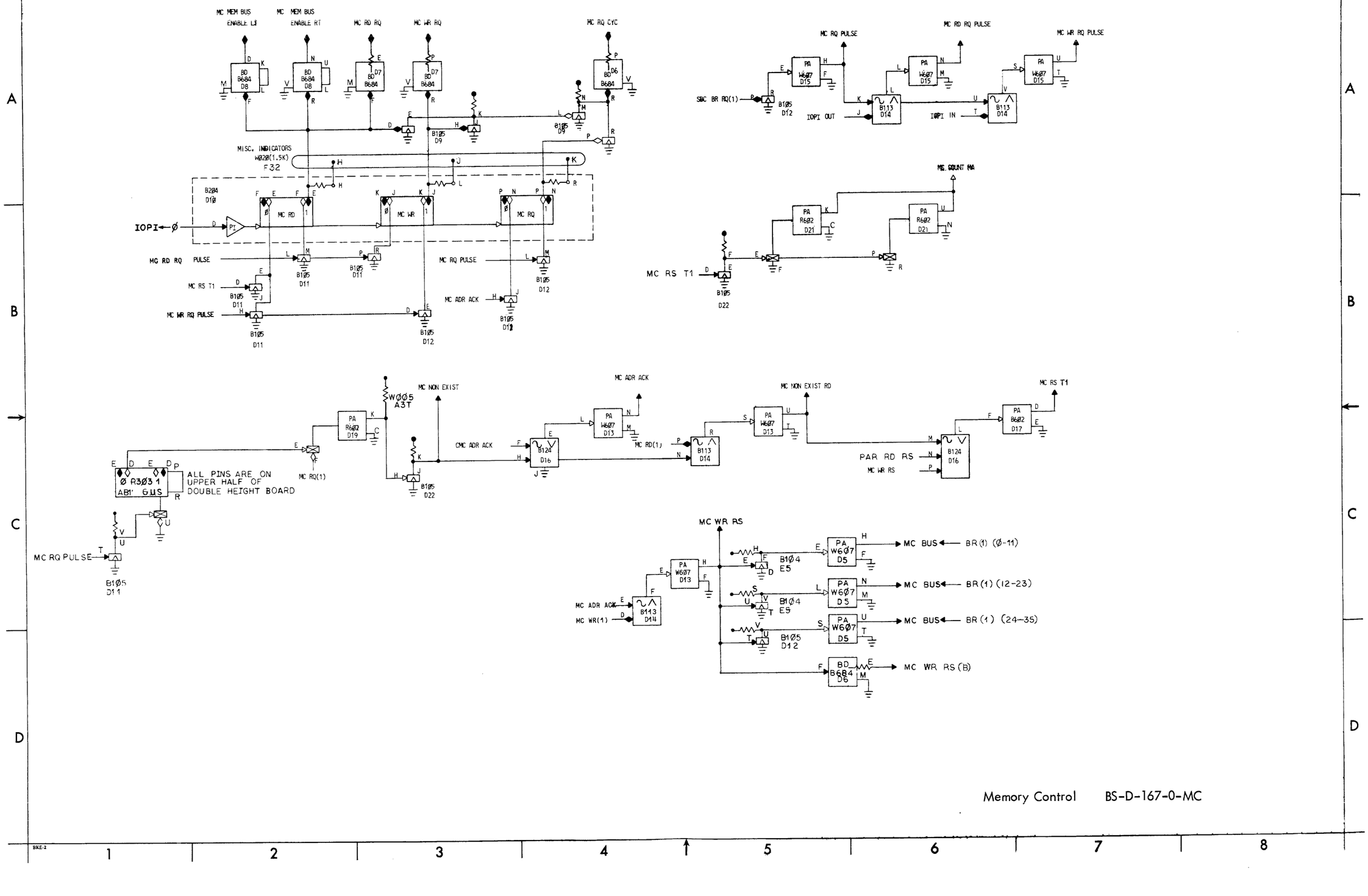
**MAKE CONNECTIONS AS SHOWN IN VERTICAL COLUMN UNDER MODE OF OPERATION.



SR Shift BS-D-167-0-SRSH

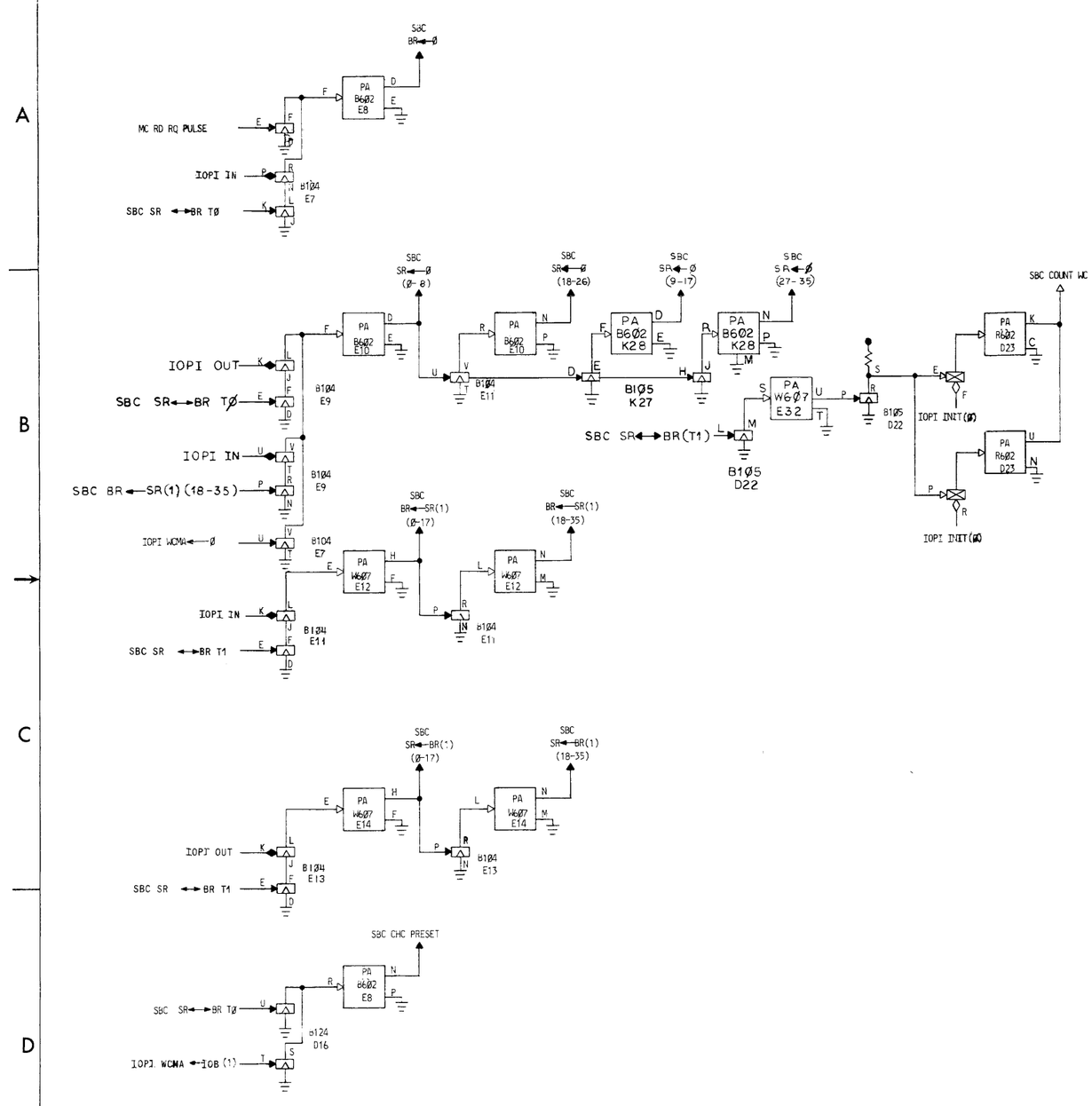
BKE-2

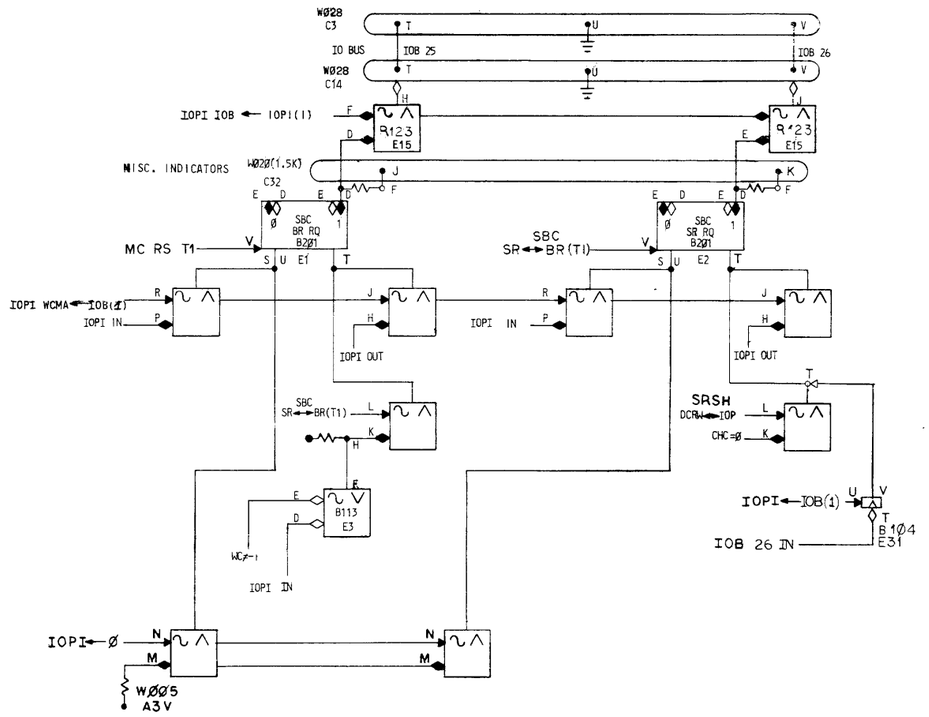

MA MEM BUS
WØ28
D3
W/1ØØΩ TERM.
MA22(1)
MA23(1)
MA24(1)
MA25(1)
MA26(1)
MA27(1)
MA28(1)
MA29(1)
MA3Ø(1)
MA MEM BUS
WØ28
D4
W/1ØØΩ TERM.
MA31(1)
MA32(1)
MA33(1)
MA34(1)
MA35(1)
MC
RD RQ
MC
WR RQ
MA MEM BUS
WØ28
D1
W/1ØØΩ TERM.
CMC
ADR ACK
CMC
RD
RS
MC
WR
RS(B)
MC
RQ
CYC
PAR ◄ (1)
MA18
MA19
MA MEM BUS
WØ28
D2
W/1ØØΩ TERM.
MA2Ø
MA21
MA22
B1Ø5
D9F
MA FM SEL
(DISABLED)
Memory Address Interface BS-D-167-0-MAI
BKE-2

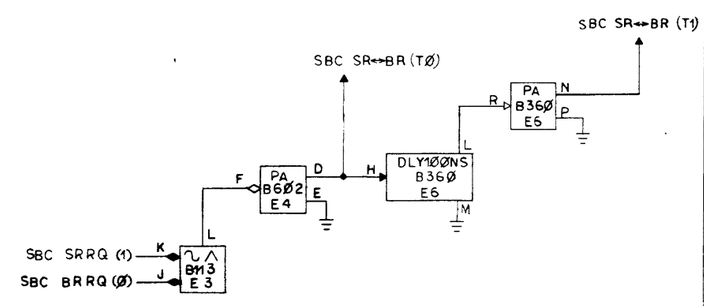


Memory Control BS-D-167-0-MC

BKE-2

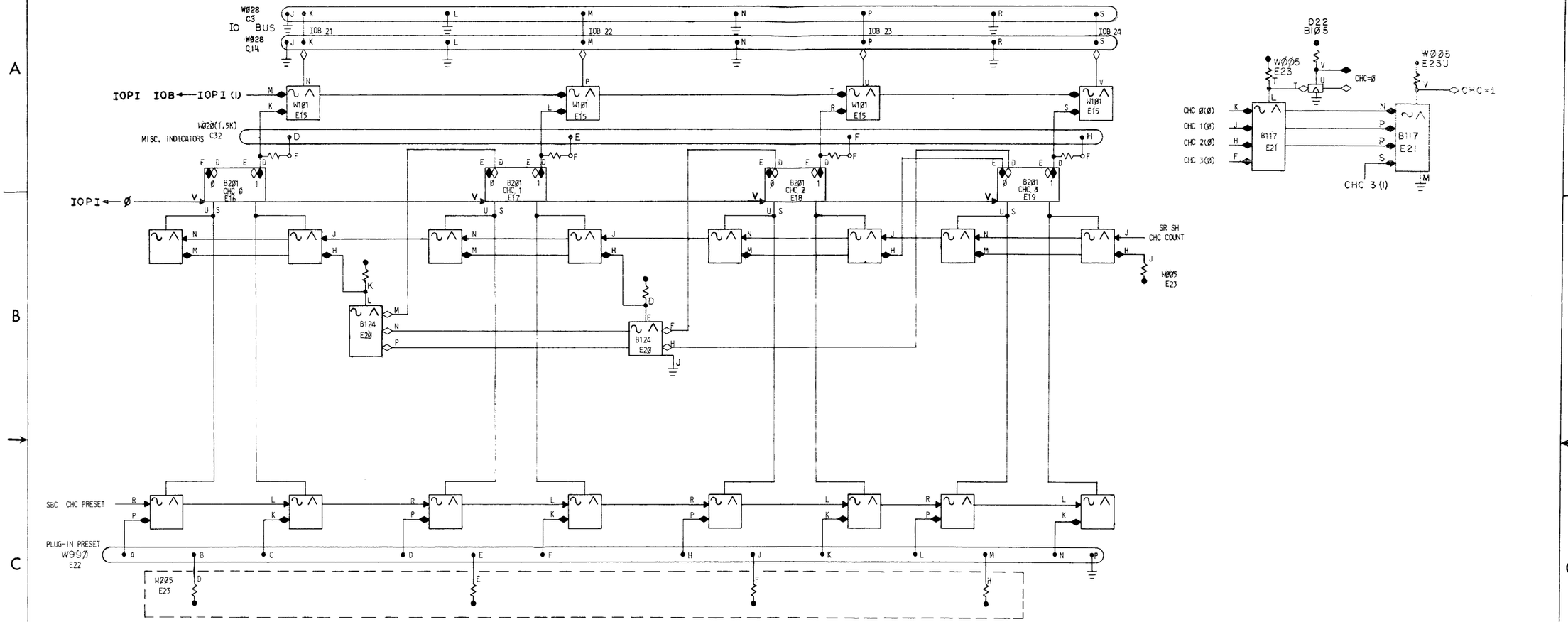






SR BR Control BS-D-167-0-SBC

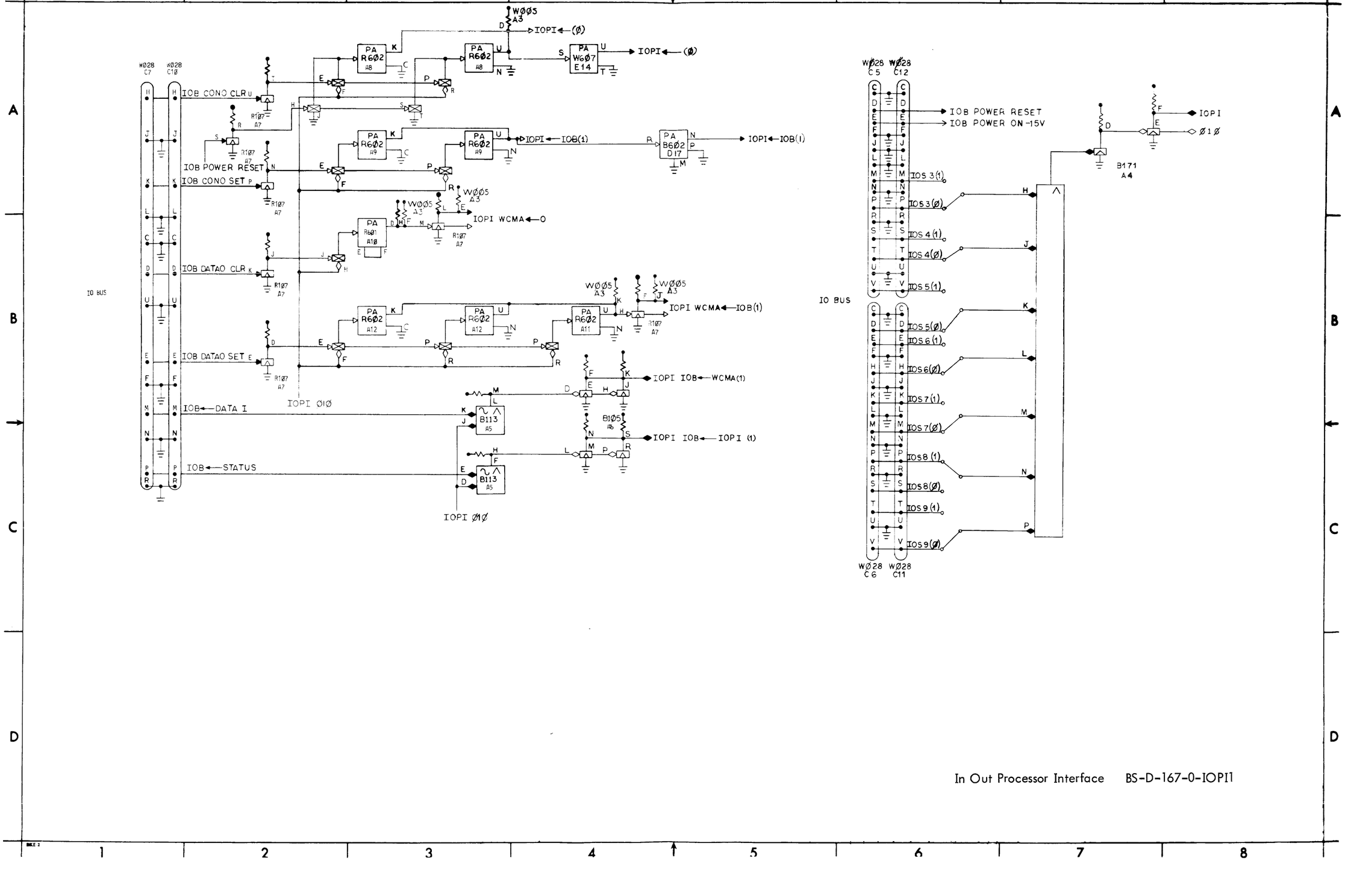
BKE-2



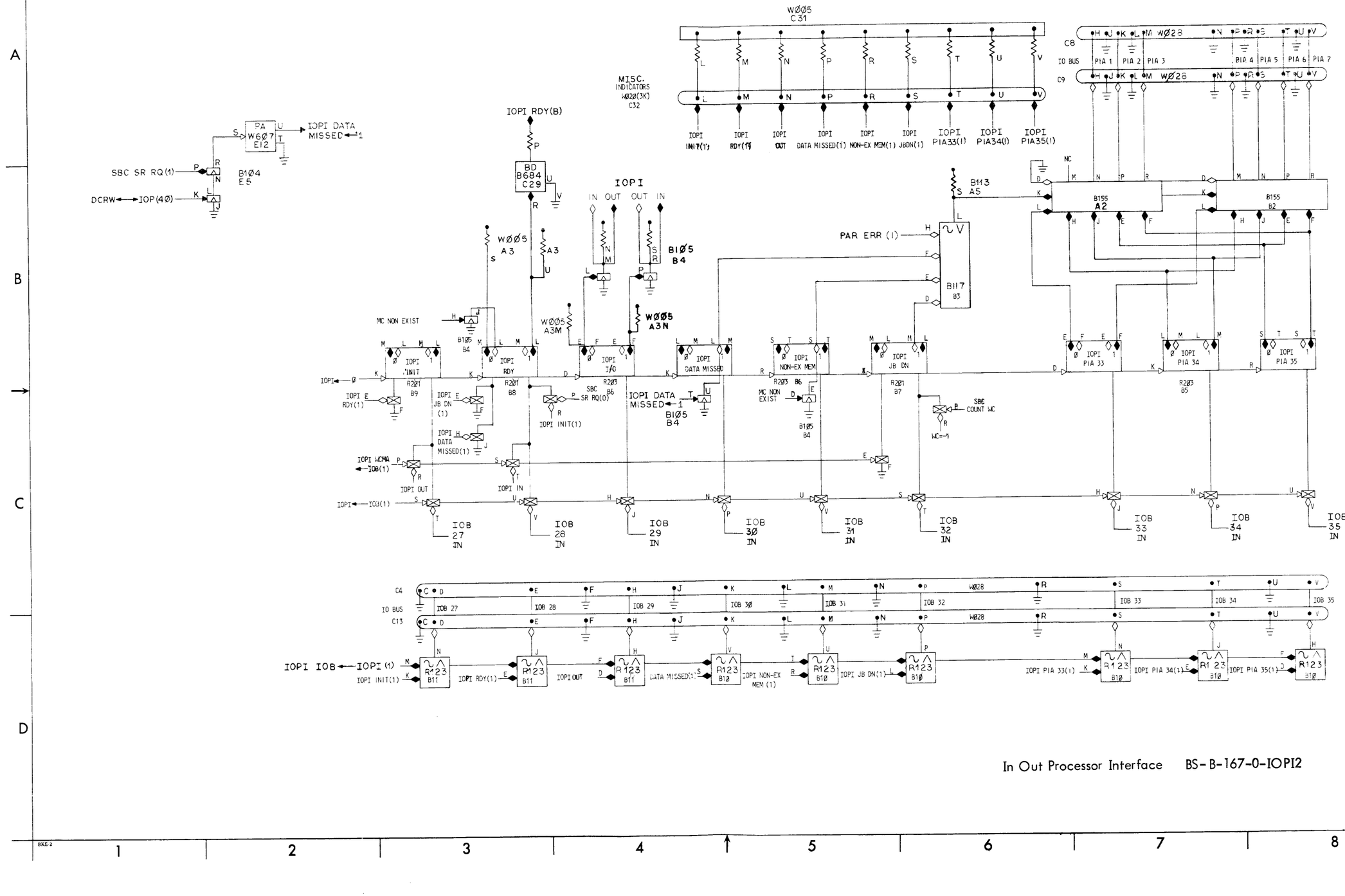
MODE	#CH/WRD	OCTAL	SH-1 (PRESET)	CARD CONNECTIONS
3	12	14	1@11	(B-C) (D-E) (J-K) (M-N) (A-F-H-L-P)
4	9	11	1@@@	(B-C) (D-E) (H-J) (M-L) (A-F-K-N-P)
6	6	6	@1@1	(A-B) (E-F) (H-J) (M-N) (C-D-K-L-P)
9	4	4	@@11	(A-B) (D-E) (J-K) (M-N) (C-F-H-L-P)
12	3	3	@@1@	(A-B) (D-E) (J-K) (M-L) (C-F-H-N-P)
18	2	2	@@@1	(A-B) (D-E) (H-J) (M-N) (C-F-K-L-P)
36	@	@	@@@@	(A-B) (D-E) (H-J) (M-L) (C-F-K-N-P)

JUMPER CONFIGURATION
FOR
PLUG-IN PRESET
W9@
E22

Character Counter BS-D-167-0-CHC

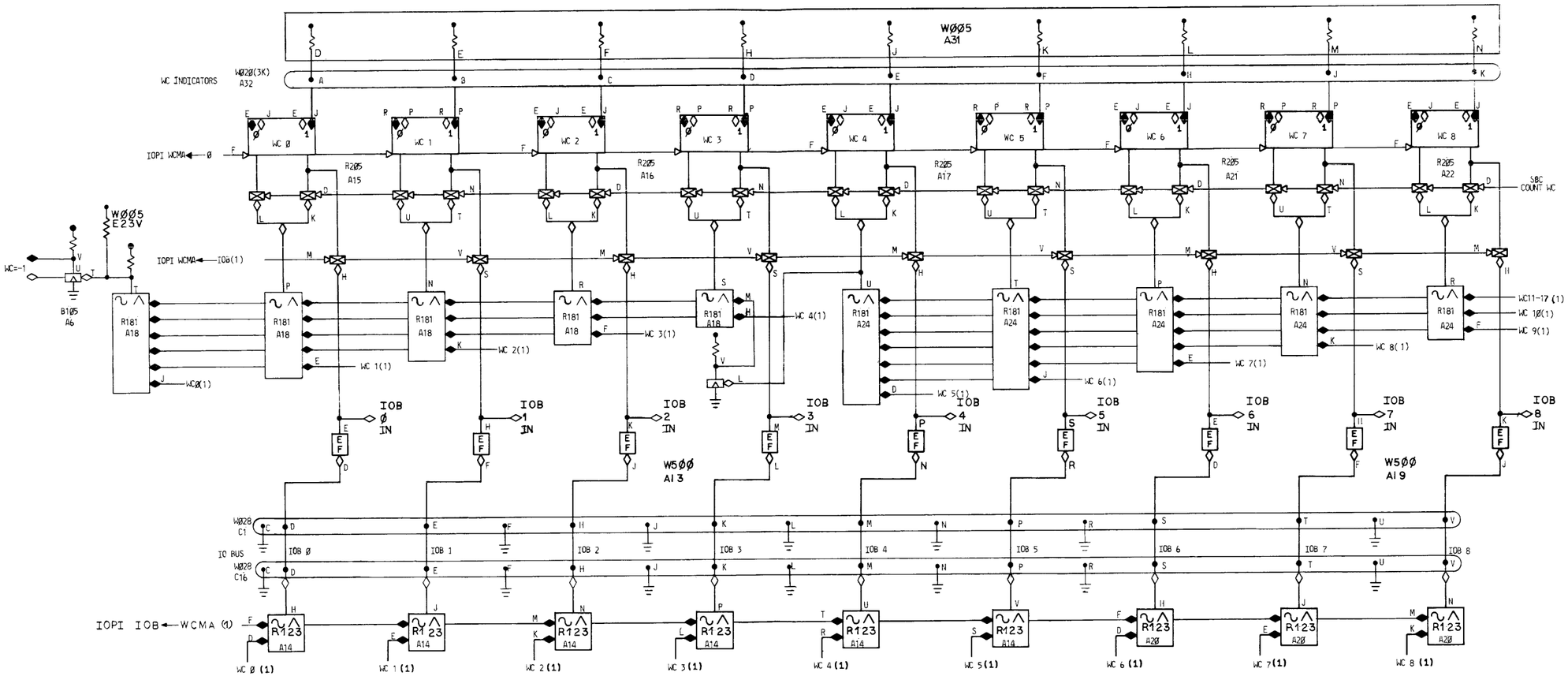


In Out Processor Interface BS-D-167-0-IOPI1



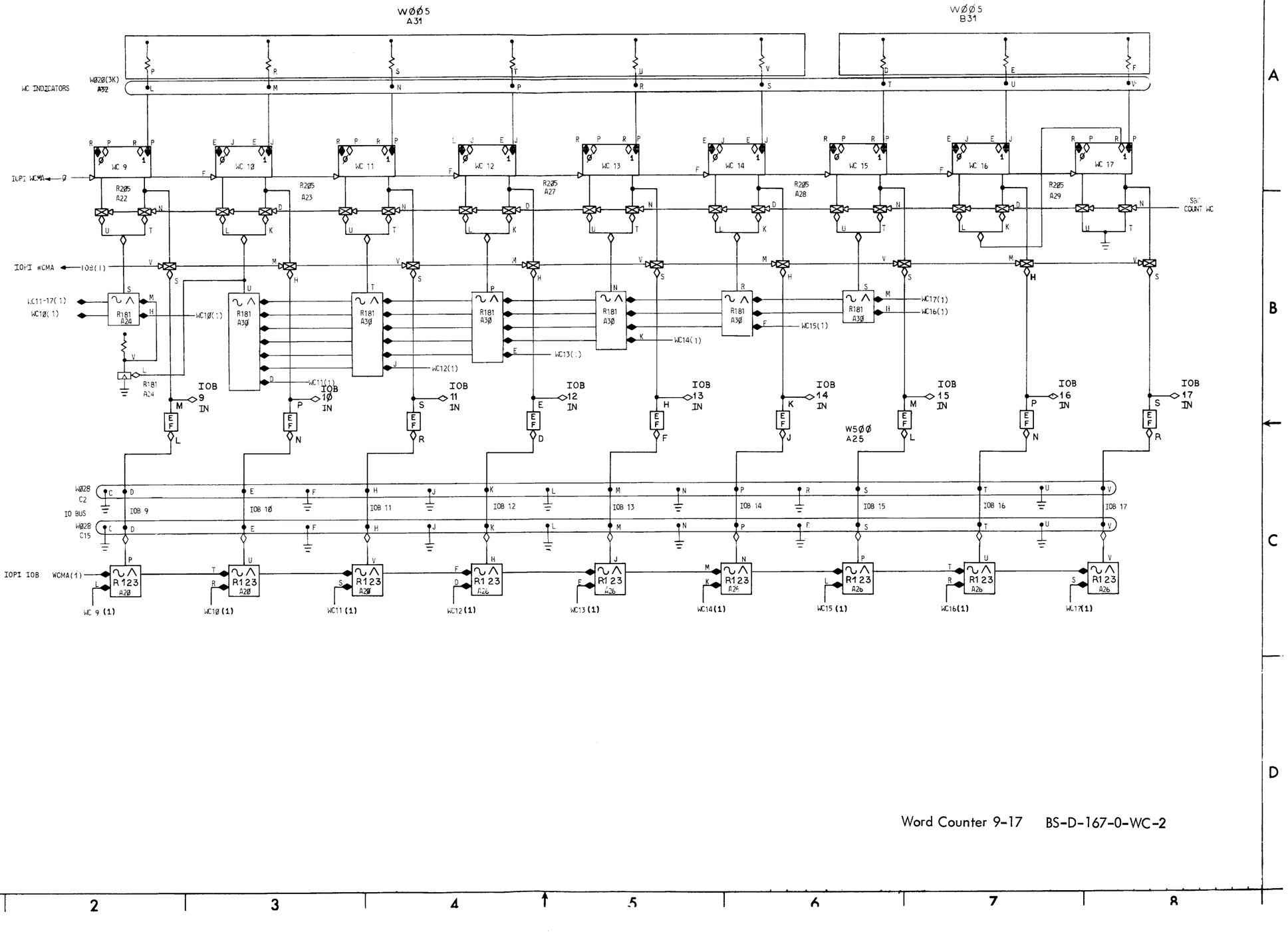
In Out Processor Interface BS-B-167-0-IOPI2

Word Counter 0-8 BS-D-167-0-WC-1

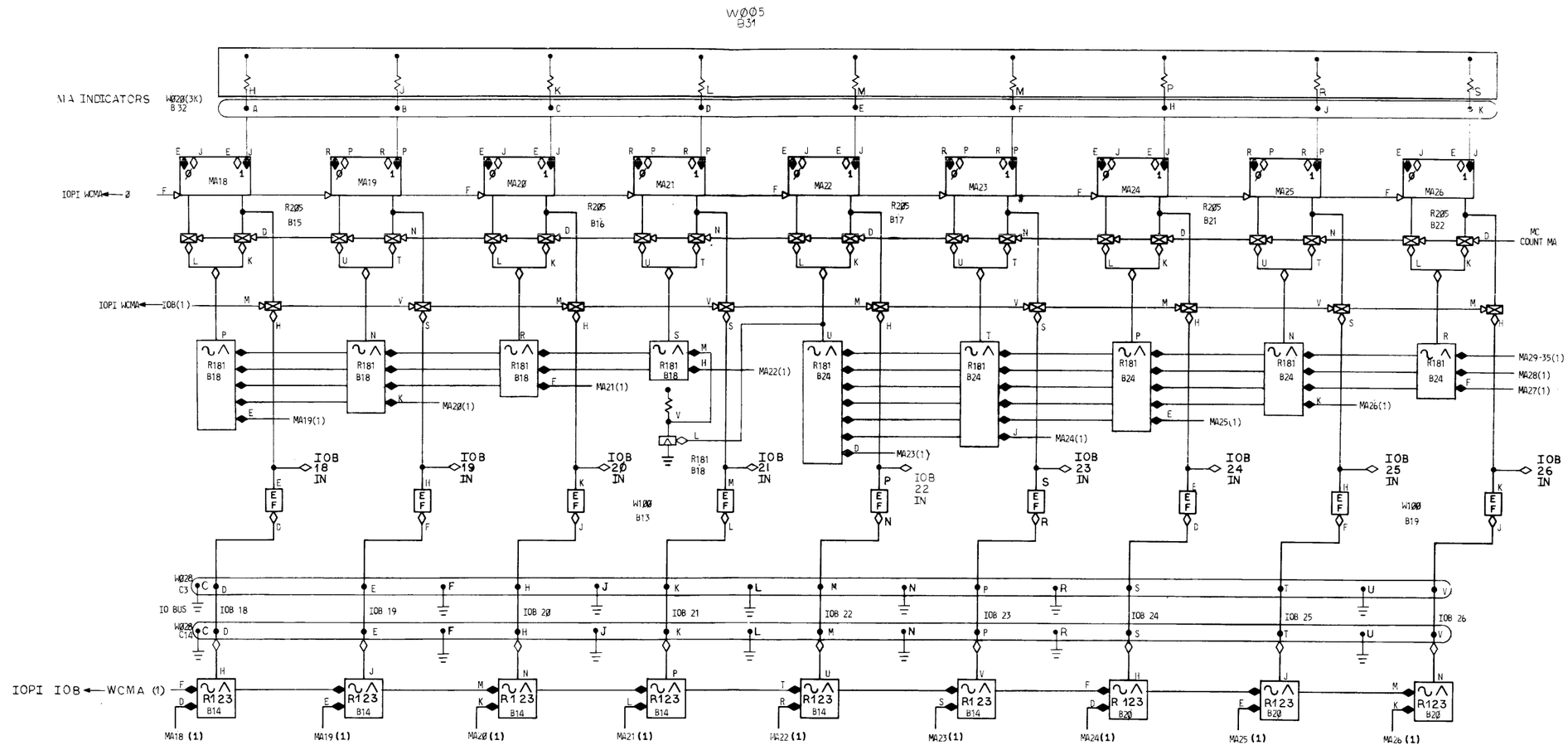


Word Counter 0-8 BS-D-167-0-WC-1

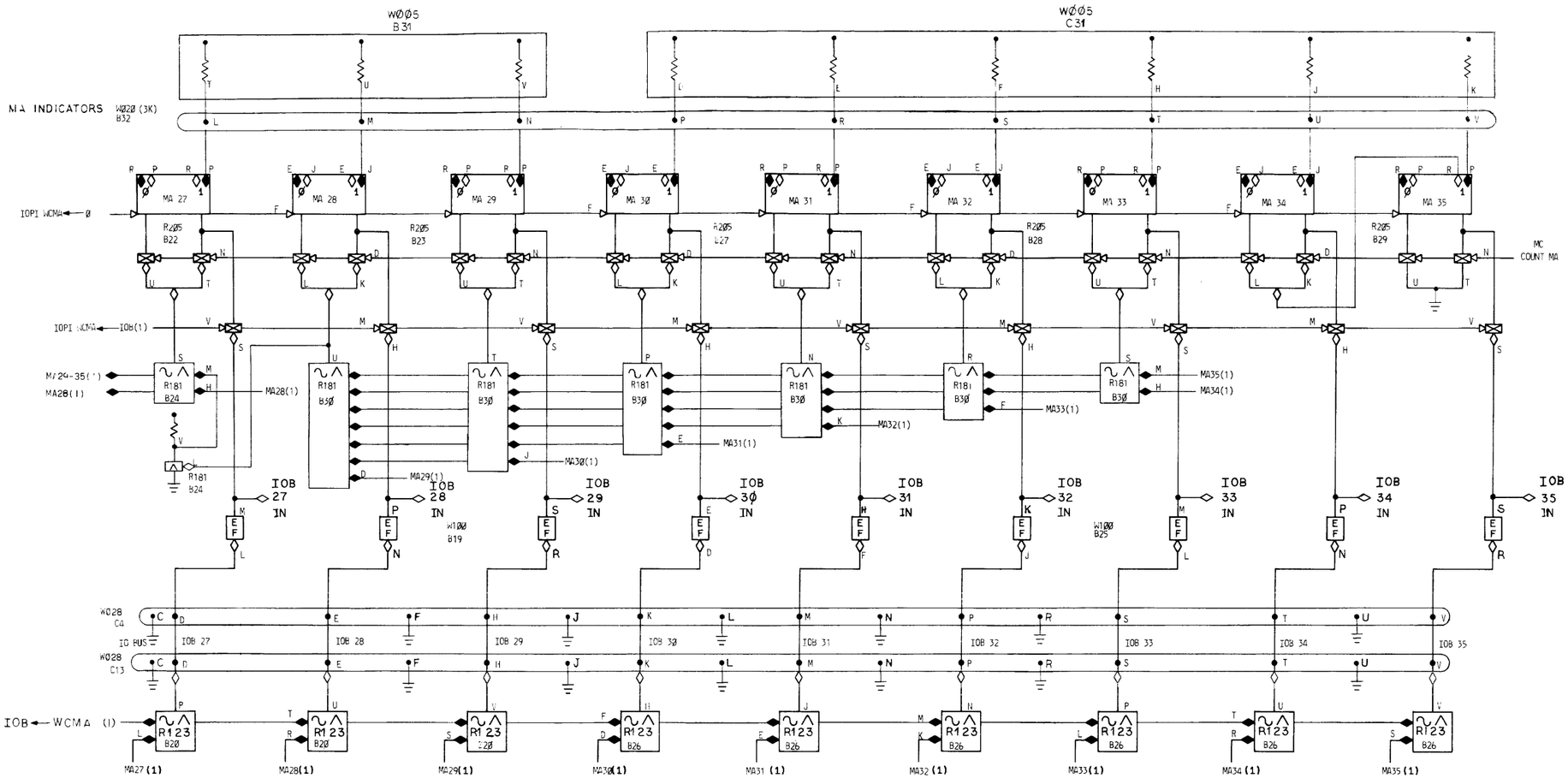
Word Counter 9-17 BS-D-167-0-WC-2



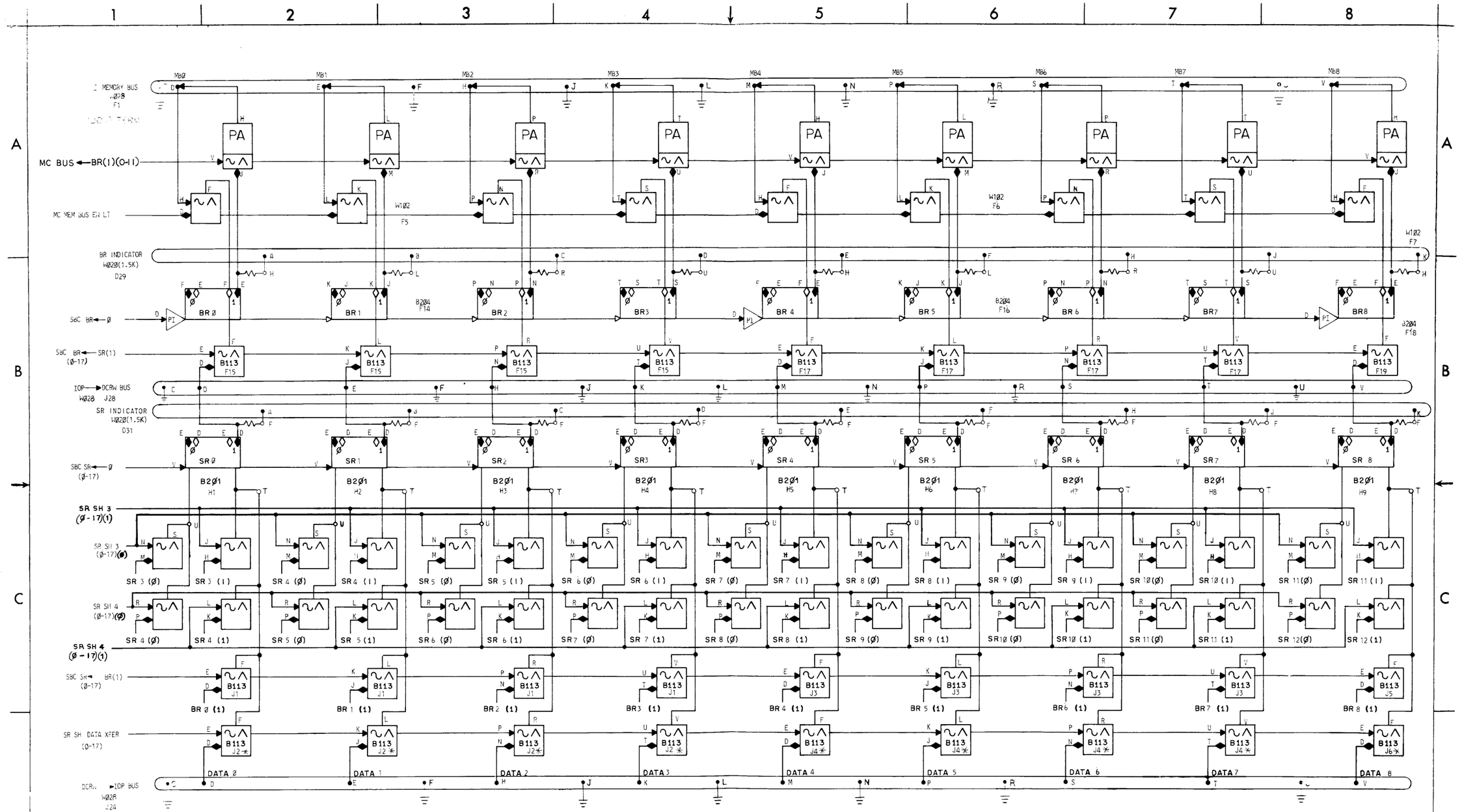
Word Counter 9-17 BS-D-167-0-WC-2



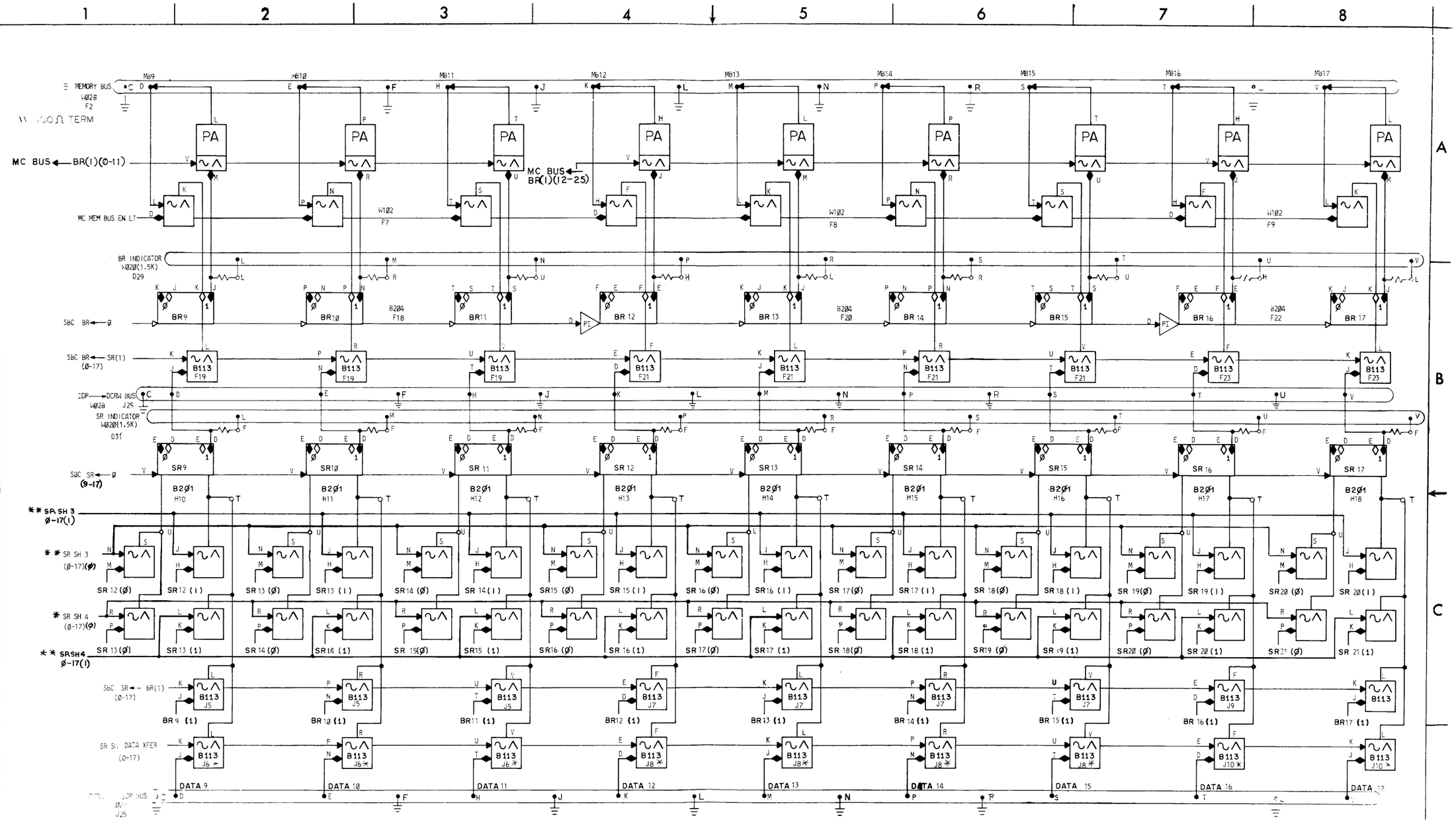
Memory Address 18-26 BS-D-167-0-MA-1



Memory Address 27-35 BS-D-167-0-MA-2

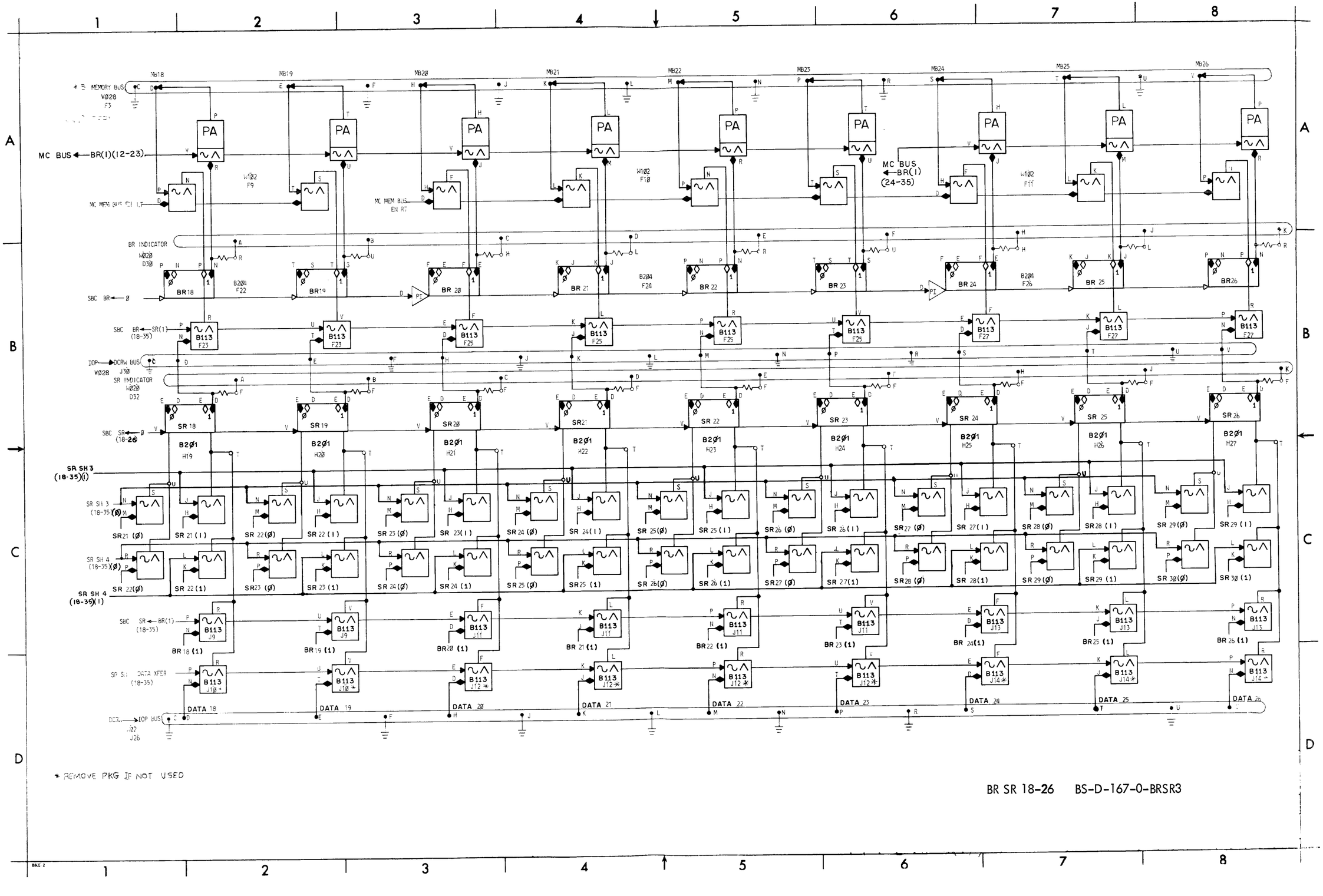


BR SR 0-8 BS-D-167-0-BRSR1



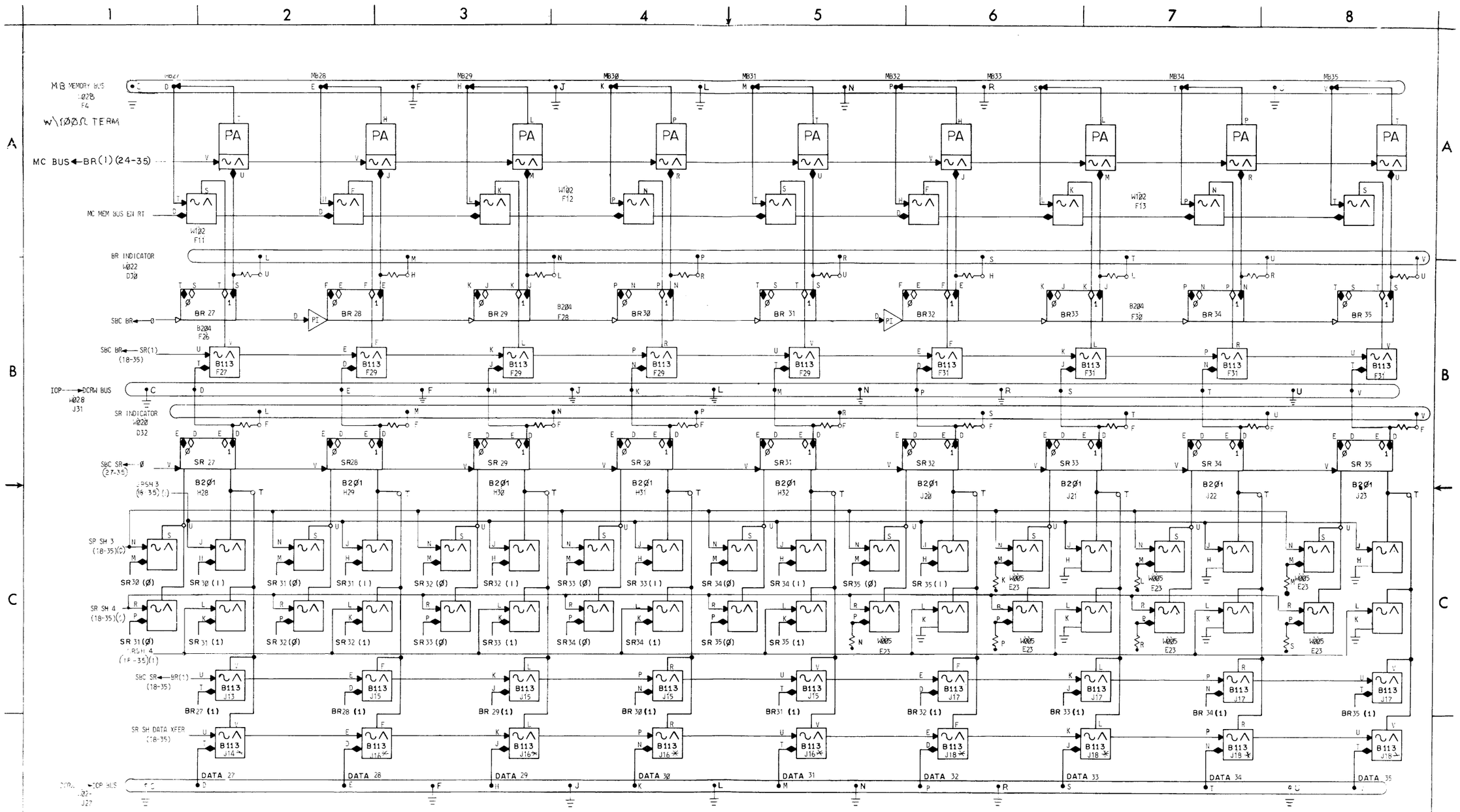
** IHIØ-N,J,R,L, ARE BUSSED SEPARATELY, THERE IS NO PHYSICAL WIRING BETWEEN N,J OR R,L.

BR SR 9-17 BS-D-167-0-BRSR2



* REMOVE PKG IF NOT USED

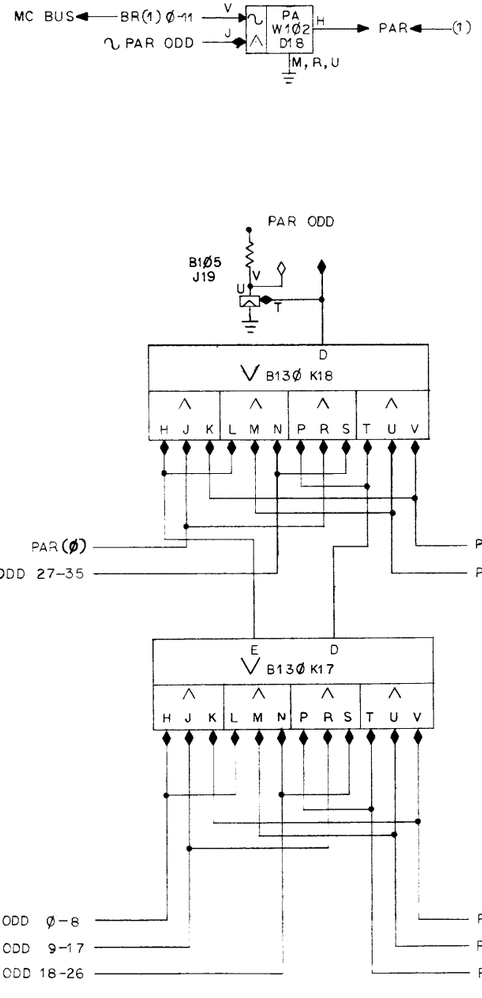
BR SR 18-26 BS-D-167-0-BRSR3

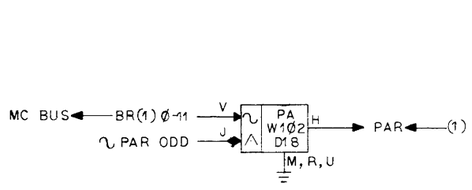


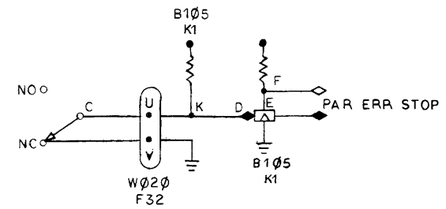
*REMOVE PKG IF NOT USED

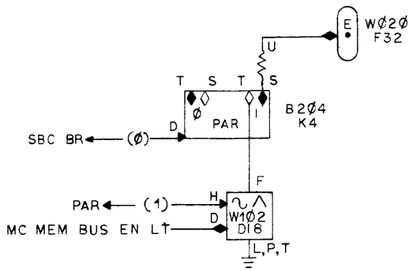
BR SR 27-35 BS-D-167-0-BRSR4

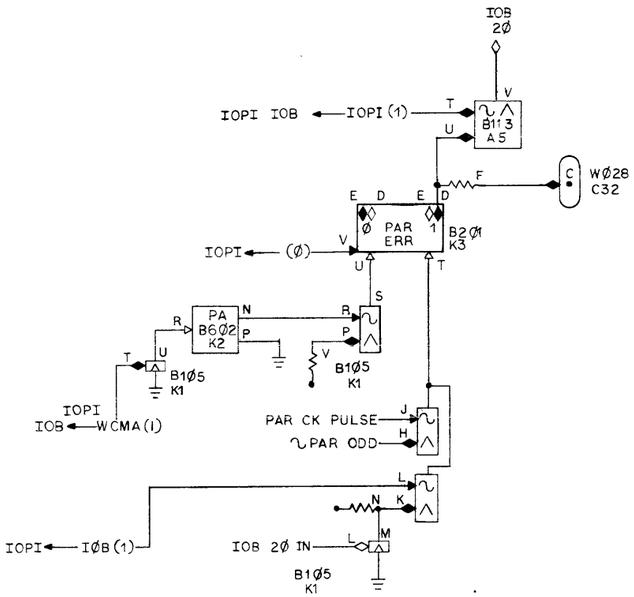
Parity Control and Net (Sheet 1) BS-D-167-0-PAR

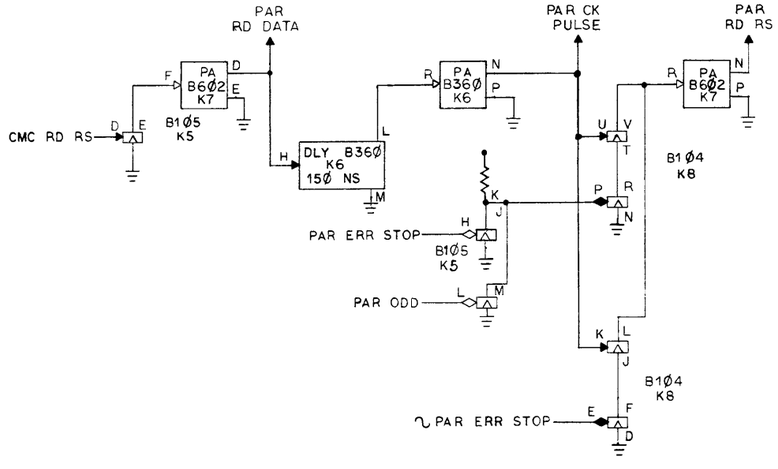






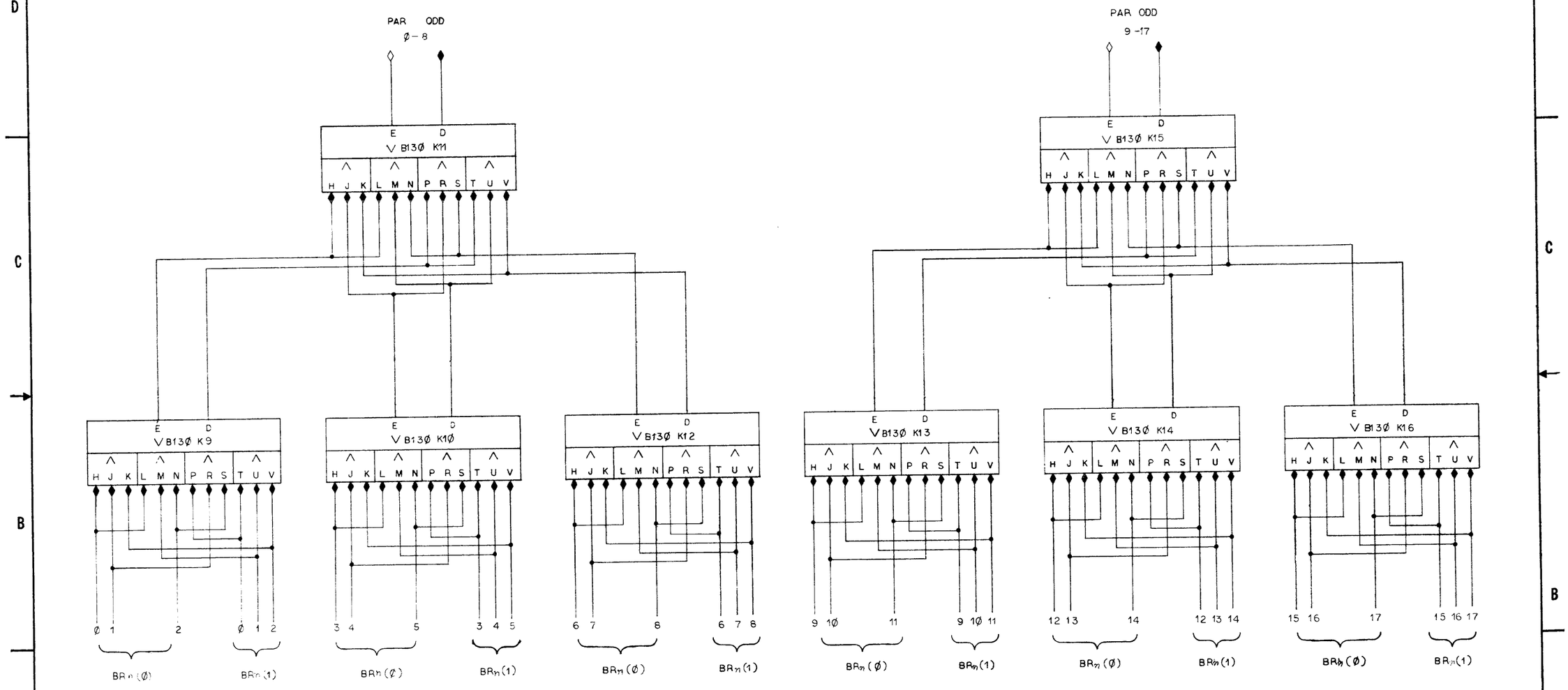






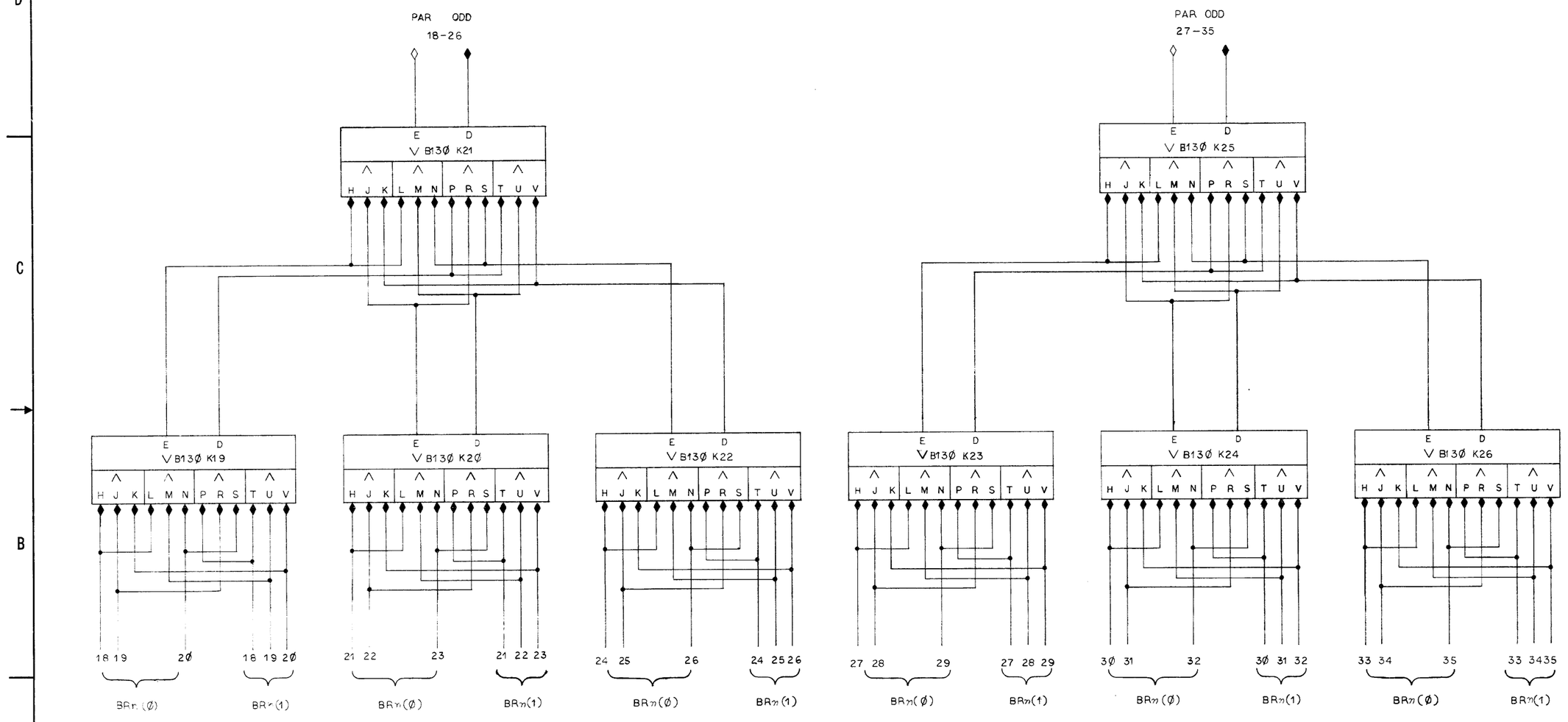
Parity Control and Net (Sheet 1) **BS-D-167-0-PAR**

Parity Control and Net (Sheet 2) BS-D-167-0-PAR

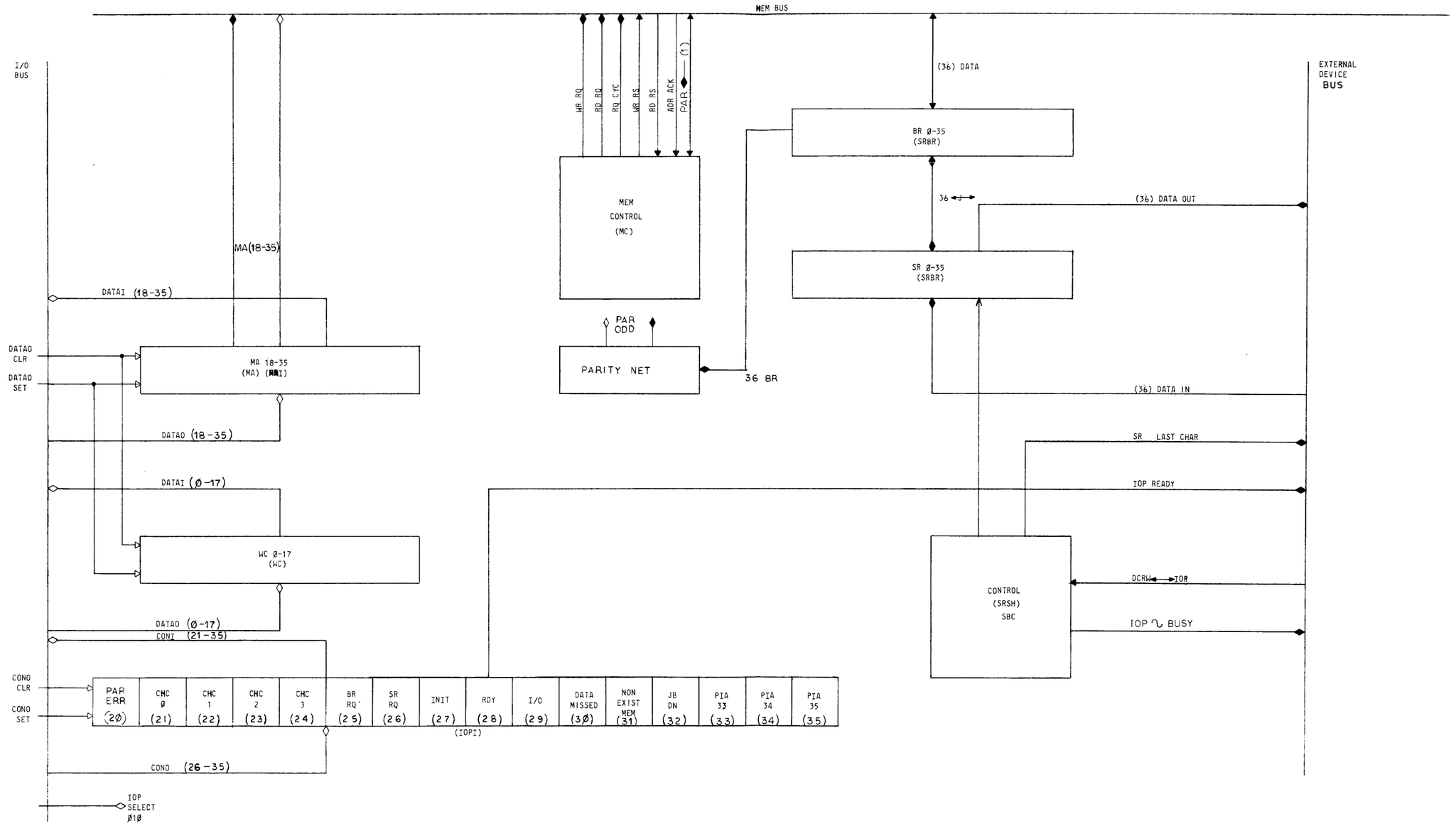


Parity Control and Net (Sheet 2) BS-D-167-0-PAR

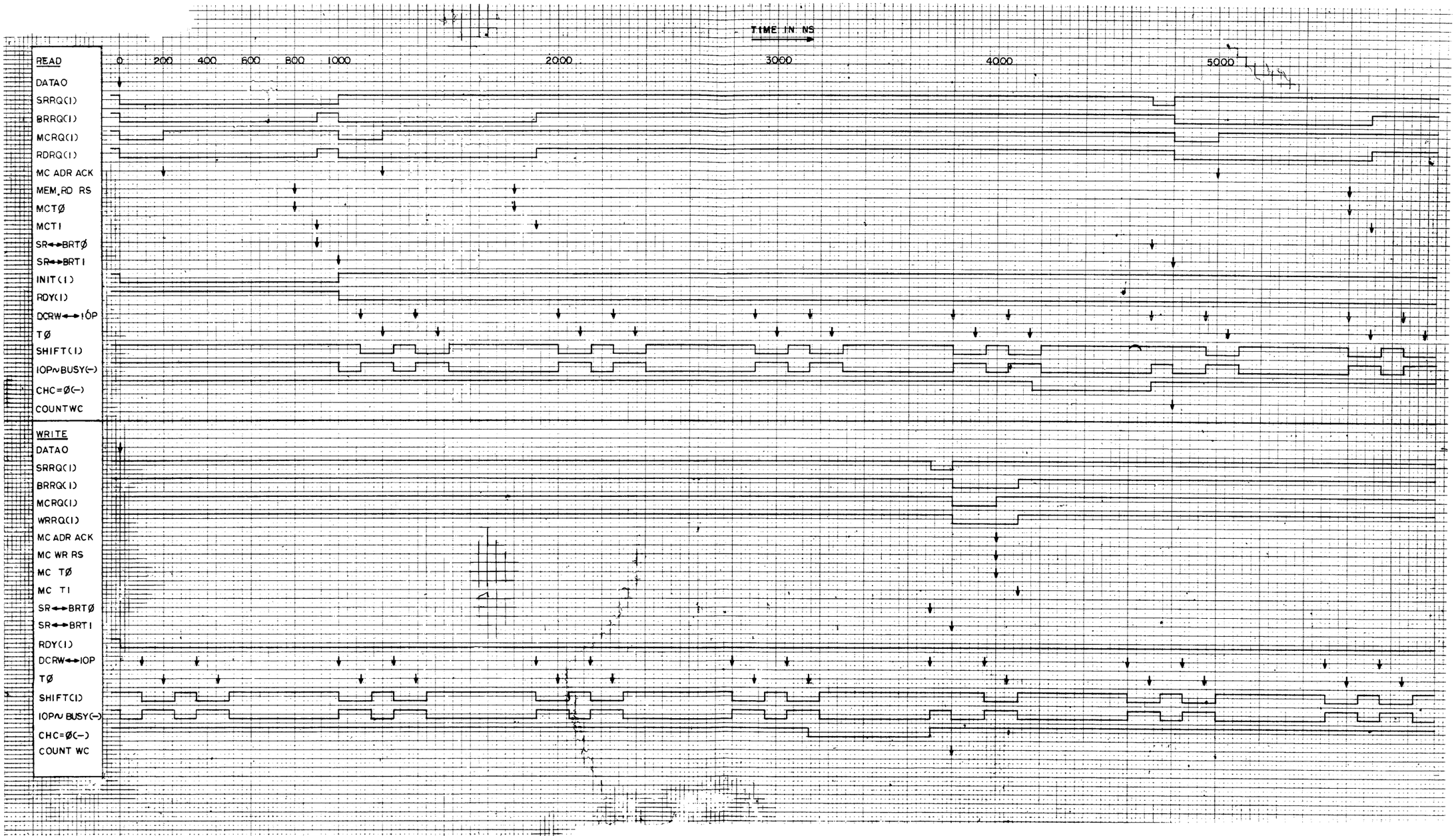
Parity Control and Net (Sheet 3) BS-D-167-0-PAR



Parity Control and Net (Sheet 3) BS-D-167-0-PAR



System Diagram SD-D-167-0-SD



Read-Write Timing TD-D-167-0-RWT

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
R3Ø3	B155	WØØ5	B171	B113	B105	R107	R602	R602	R601	R602	R602	W5ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	W5ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	W5ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	WØØ5	WØ2Ø
MC NON EXIST	PIA 1,2,3	IOPI ← Ø IOPI WCMA IOPI I/O IOPI RDY MC NONEXS IOPI RDY(B) SBC BR RQ	IOPI ØIØ	IOPI IOB IOPI(1) IOPI IOB ← WCMA(1) IOPI IOB IOB 2Ø	IOPI IOB ← WCMA(1) IOPI IOB ← IOPI(1) WC=1	IOPI WCMA IOB(1) IOPI WCMA ← Ø IOPI ← IOB(1) IOPI ← Ø	IOPI ← Ø	IOPI WCMA ← Ø	IOPI WCMA Ø	IOPI WCMA IOB(1)	IOPI WCMA ← IOB(1)	IOB Ø IN IOB 1 IN IOB 2 IN IOB 3 IN IOB 4 IN IOB 5 IN IOB 6 IN	IOB Ø-1 IOB 2-3 IOB 4-5	WC Ø WC 1	WC 2 WC 3	WC 4 WC 5	WC Ø-3 WC 3	IOB 6 IN IOB 7 IN IOB 8 IN IOB 9 IN IOB 1Ø IN IOB 11 IN	IOB 6-7 IOB 8-9 IOB 1Ø-11	WC 6 WC 7	WC 8 WC 9	WC 1Ø WC 11	WC 4-1Ø	IOB 12 IN IOB 13 IN IOB 14 IN IOB 15 IN IOB 16 IN IOB 17 IN	IOB 12-13 IOB 14-15 IOB 16-17	WC 12 WC 13	WC 14 WC 15	WC 16 WC 17	WC 1Ø-15	WC Ø WC 1 WC 2 WC 3 WC 4 WC 5 WC 6 WC 7 WC 8 WC 9 WC 1Ø WC 11 WC 12 WC 13 WC 14	WC Ø THRU WC 17
	B155	B117		R2Ø3	R2Ø3	R2Ø1	R2Ø1	R2Ø1	R123	R123		W1ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	W1ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	W1ØØ	R123	R2Ø5	R2Ø5	R2Ø5	R181	WØØ5	WØ2Ø
	PIA 4,5,6,7	PIA 1,2,3	IOPI RDY IOPI IOPI DATA MISS.	IOPI PIA 33 IOPI PIA 34 IOPI PIA 35	IOPI I/O IOPI DATA MISSED IOPI NON-EX MEM	IOPI JB DN	IOPI RDY	IOPI INIT	IOB 3Ø-31 IOB 32-33 IOB 34-35	IOB 27-28 IOB 29		IOB 18 IN IOB 19 IN IOB 20 IN IOB 21 IN IOB 22 IN IOB 23 IN	IOB 18-19 IOB 20-21 IOB 22-23	MA 18 MA 19	MA 2Ø MA 21	MA 22 MA 23	MA 18-21 MA 21	IOB 24 IN IOB 25 IN IOB 26 IN IOB 27 IN IOB 28 IN IOB 29 IN	IOB 24-25 IOB 26-27 IOB 28-29	MA 24 MA 25	MA 26 MA 27	MA 28 MA 29	MA 22-27 MA 27	IOB 3Ø IN IOB 31 IN IOB 32 IN IOB 33 IN IOB 34 IN IOB 35 IN	IOB 3Ø-31 IOB 32-33 IOB 34-35	MA 3Ø MA 31	MA 32 MA 33	MA 34 MA 35	MA 28-33	WC 15 WC 16 WC 17 MA 18 MA 19 MA 2Ø MA 21 MA 22 MA 23 MA 24 MA 25 MA 26 MA 27 MA 28 MA 29	MA 18 THRU MA 26 THRU MA 35
WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	WØ28	B684	B684	B684	B684	B684	B684	B684	B684	B684	B684	B684	B684	B684	B36Ø	WØØ5	WØ2Ø
IOB Ø THRU IOB 8	IOB 9 THRU IOB 17	IOB 18 THRU IOB 26	IOB 27 THRU IOB 35	IO BUS	IO BUS	IO BUS	IO BUS	IO BUS	IO BUS	IO BUS	IO BUS	IOB 27 THRU IOB 35	IOB 18 THRU IOB 26	IOB 9 THRU IOB 17	IOB Ø THRU IOB 8	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	SRSH CHC COUNT	MA 3Ø MA 31 MA 32 MA 33 MA 34 MA 35 INIT(1) RDY(1) OUT DATA MIS(1) NON-EXMEM(1) JB DN(1) PIA33(1) PIA34(1) PIA35(1)	PAR ERR MISC INDICATORS
WØ28	WØ28	WØ28	WØ28	WØ67	B684	B684	B684	B105	R204	B105	B105	WØ67	B113	WØ67	B124	B602	W102	R602		R602	B105	R602	B36Ø	B36Ø	B36Ø	B36Ø	B36Ø	WØ2Ø	WØ2Ø	WØ2Ø	WØ28
MA MEM BUS	MA MEM BUS	MA MEM BUS	MA MEM BUS	MC BUS ← BR(1) (Ø-11) MC BUS ← BR(1) (12-23) MC BUS ← BR(1) (24-35)	MC WR RS (B) MC RQ CYC	MC RD RQ MC WR RQ	MC MEM BUS ENABLE LT & RT	MC RQ CYC MC RQ CYC	MC RD MC WR MC RQ SRSH SHIFT	MC RD MC RD MC WR MC WR MC NON EXIST	MC WR MC RQ MC RQ MC RQ PULSE MC BUS ← BR(1) (24-35)	MC WR RS MC ADR ACK MC NON EXIST RD	MC WR RS MC RD RQ PULSE MC NON EXIST RD MC WR RQ PULSE	MC RQ PULSE MC RD RQ PULSE MC WR RQ PULSE	MC ADR ACK MC RS TI SBC CHC PRESET	MC RS TI IOPI ← IOB(1)	PAR PAR	MC NON EXIST	MC COUNT MA	MC COUNT MA MC NON EXIST SBC COUNT WC CHC = Ø	SBC COUNT WC	SRSH T4	SRSH T3	SRSH T2	SRSH T1	SRSH TØ	BR Ø THRU BR 8 THRU BR 17	BR 18 THRU BR 35	SR Ø THRU SR 8 THRU SR 17	SR 18 THRU SR 35

Utilization Module List (Sheet 1) UML-D-167-0-UML

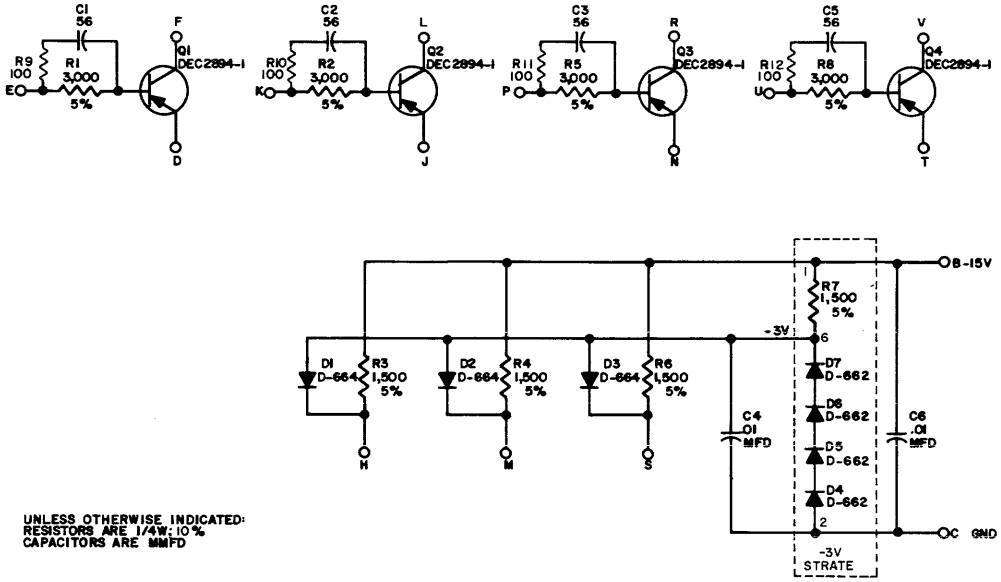
Utilization Module List (Sheet 2) UML-D-167-0-UML

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
B201	B201	B113	B602	B104	B36Ø	B104	B602	B104	B602	B104	W607	B104	W607	R123	B201	B201	B201	B201	B124	B117	W99Ø	W0Ø5	W99Ø	B124	B602	B124	B602	B113	W607	B104	W607
SBC BR RQ	SBC SR RQ	SBC BR RQ SBC SR ← BR(TØ)	SBC SR ↔ BR (TØ)	MC BUS ← BR(1) (Ø-11) IOPI DATA MISSED ← IOPI DATA MISSED ← MC BUS ← BR(1) (12-23)	SBC SR ↔ BR (T1)	SBC BR ← Ø SBC BR ← Ø SBC BR ← Ø SBC SR ← Ø Ø-17	SBC BR ← Ø SBC CHC	SBC SR ← Ø Ø-17 SBC SR ← Ø Ø-17 SRC SR ← Ø Ø-17 SBC SR ← Ø Ø-17	SBC SR ← Ø Ø-8 SBC SR ← Ø 8-26	SBC BR ← SR Ø-17 SBC BR ← SR Ø-17 SBC BR ← SR 18-35 SBC BR ← SR 18-26	SBC BR ← SR Ø-17 SBC BR ← SR 18-35 IOP DATA MISSED	SBC SR BR(1) Ø-17 SBC SR BR(1) Ø-17 SBC SR BR(1) 18-35 SRSH TØ	SBC SR ← BR(1) Ø-17 SBC SR ← BR(1) 18-35 IOPI ← Ø	IOB 25-26	CHC Ø	CHC 1	CHC 2	CHC 3	SRSH IOP LAST CHAR	CHC = Ø CHC = 7	CHC PRESET JUMPER BOARD	SR 33 SR 34 SR 35 SR 32 SR 33 SR 34 SR 35 WC=1	SRSH TØ-T4 SRSH SHIFT	SRSH 4 Ø-17 (1) SRSH 4 18-35(Ø) SRSH SHIFT	SRSH 4 Ø-17(1) SRSH 4 18-35(Ø)	SRSH 4 Ø-17(Ø) SRSH IOP BUSY SRSH 4 18-35(1)	SRSH 4 Ø-17(Ø) SRSH 4 18-35(1)	SRSH DATA XFER Ø-17 SRSH DATA XFER 18-35 SRSH SHIFT SRSH DCRW IOP	SRSH DATA XFER Ø-17 SRSH DATA XFER 18-35 SRSH DCRW IOP	SRSH DCRW ↔ IOP SRSH DCRW ↔ IOP SRSH IOP LAST CHAR SBC SR RQ	SBC COUNT WC
W028	W028	W028	W028	W102	W102	W102	W102	W102	W102	W102	W102	W102	B204	B113	B204	B113	B204	B113	B204	B113	B204	B113	B204	B113	B204	B113	B204	B113	B204	B113	W020
MB Ø THRU MB 8	MB 9 THRU MB 17	MB 18 THRU MB 26	MB 27 THRU MB 35	MB Ø MB 1 MB 2 MB 3	MB 4 MB 5 MB 6 MB 7	MB 8 MB 9 MB 10 MB 11	MB 12 MB 13 MB 14 MB 15	MB 16 MB 17 MB 18 MB 19	MB 20 MB 21 MB 22 MB 23	MB 24 MB 25 MB 26 MB 27	MB 28 MB 29 MB 30 MB 31	MB 32 MB 33 MB 34 MB 35	BR Ø BR 1 BR 2 BR 3	BR Ø BR 1 BR 2 BR 3	BR 4 BR 5 BR 6 BR 7	BR 4 BR 5 BR 6 BR 7	BR 8 BR 9 BR 10 BR 11	BR 8 BR 9 BR 10 BR 11	BR 12 BR 13 BR 14 BR 15	BR 12 BR 13 BR 14 BR 15	BR 16 BR 17 BR 18 BR 19	BR 16 BR 17 BR 18 BR 19	BR 20 BR 21 BR 22 BR 23	BR 20 BR 21 BR 22 BR 23	BR 24 BR 25 BR 26 BR 27	BR 24 BR 25 BR 26 BR 27	BR 28 BR 29 BR 30 BR 31	BR 28 BR 29 BR 30 BR 31	BR 32 BR 33 BR 34 BR 35	BR 32 BR 33 BR 34 BR 35	PAR ERR STOP PAR(1) MC RD MC WR MC RQ SRSH SHIFT
B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201	B201
SR Ø	SR 1	SR 2	SR 3	SR 4	SR 5	SR 6	SR 7	SR 8	SR 9	SR 10	SR 11	SR 12	SR 13	SR 14	SR 15	SR 16	SR 17	SR 18	SR 19	SR 20	SR 21	SR 22	SR 23	SR 24	SR 25	SR 26	SR 27	SR 28	SR 29	SR 30	SR 31
B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B113	B105	B201	B201	B201	B201	W028	W028	W028	W028	W028	W028	W028	W028	W028
SR Ø SR 1 SR 2 SR 3	SR Ø SR 1 SR 2 SR 3	SR 4 SR 5 SR 6 SR 7	SR 4 SR 5 SR 6 SR 7	SR 8 SR 9 SR 10 SR 11	SR 8 SR 9 SR 10 SR 11	SR 12 SR 13 SR 14 SR 15	SR 12 SR 13 SR 14 SR 15	SR 16 SR 17 SR 18 SR 19	SR 16 SR 17 SR 18 SR 19	SR 20 SR 21 SR 22 SR 23	SR 20 SR 21 SR 22 SR 23	SR 24 SR 25 SR 26 SR 27	SR 24 SR 25 SR 26 SR 27	SR 28 SR 29 SR 30 SR 31	SR 28 SR 29 SR 30 SR 31	SR 32 SR 33 SR 34 SR 35	SR 32 SR 33 SR 34 SR 35	PAR ODD	SR 32	SR 33	SR 34	SR 35	DATA Ø THRU DATA 8	DATA 9 THRU DATA 17	DATA 18 THRU DATA 26	DATA 27 THRU DATA 35	SR Ø THRU SR 8	SR 9 THRU SR 17	SR 18 THRU SR 26	SR 27 THRU SR 35	DCRW ↔ IOP BUS

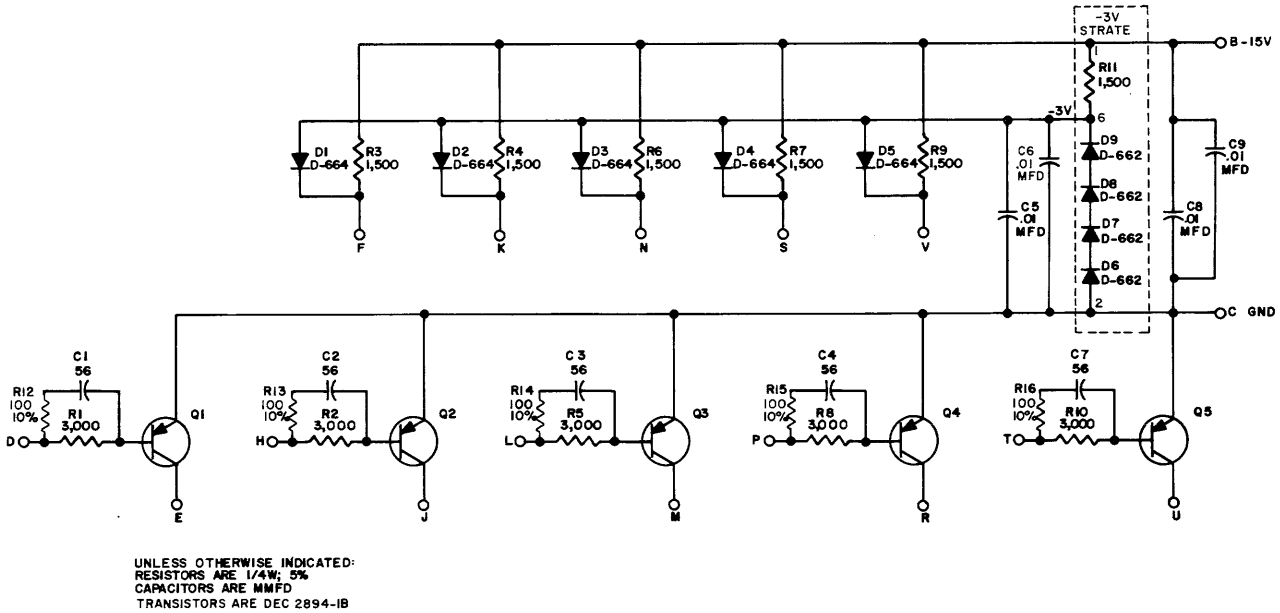
Utilization Module List (Sheet 2) UML-D-167-0-UML

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
B105	B602	B201	B204	B105	B360	B602	B104	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B130	B105	E602	B24	B23	B22	B21
PAR ERR STOP				PAR RD DATA			PAR RD DATA																			SBC SR←Ø (9-7)					
																											SBC SR←Ø	SBC SR←Ø (9-7)	SRSH3 Ø-17(Ø)	SRSH 3 18-35(Ø)	SRSH 3 Ø-17(Ø)	SRSH 3 18-35(Ø)
				PAR RD DATA	PAR CK PULSE	PAR RD DATA																				(27-35)					
PAR ERR STOP		PAR ERR					PAR RD DATA	PAR ODD Ø-8	PAR ODD Ø-8	PAR ODD Ø-8	PAR ODD Ø-8	PAR ODD 9-17	PAR ODD 9-17	PAR ODD 9-17	PAR ODD 9-17	PAR ODD	PAR ODD	PAR ODD 18-26	PAR ODD 18-26	PAR ODD 18-26	PAR ODD 18-26	PAR ODD 27-35	PAR ODD 27-35	PAR ODD 27-35	PAR ODD 27-35						
	PAR ERR																										SBC SR←Ø (27-35)	SRSH 3 Ø-7(Ø)	SRSH 3 18-35(Ø)	SRSH 3 Ø-17(Ø)	SRSH 3 18-35(Ø)
			PAR		PAR CK PULSE	PAR RD RS																									
PAR ERR STOP							PAR RD DATA																								

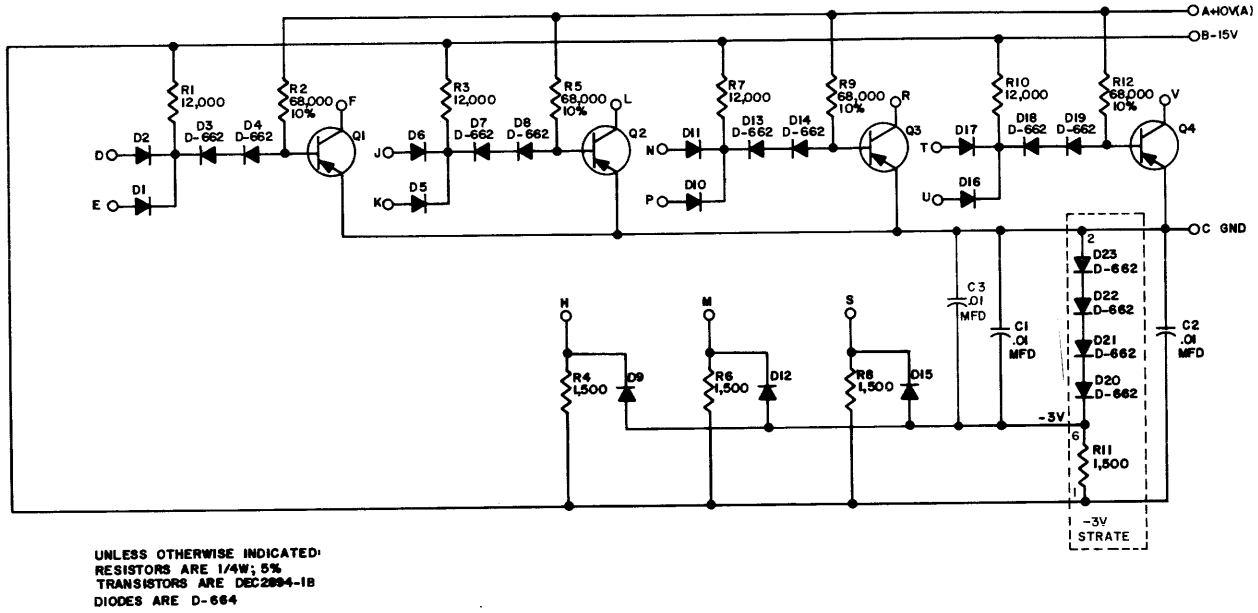
Utilization Module List (Sheet 3) UML-D-167-0-UML



Inverter CS-B-B104

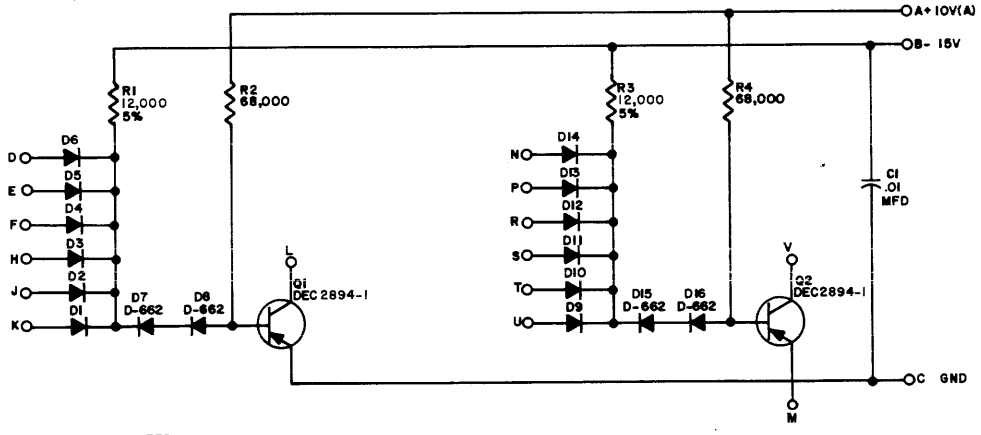


Inverter CS-B-B105



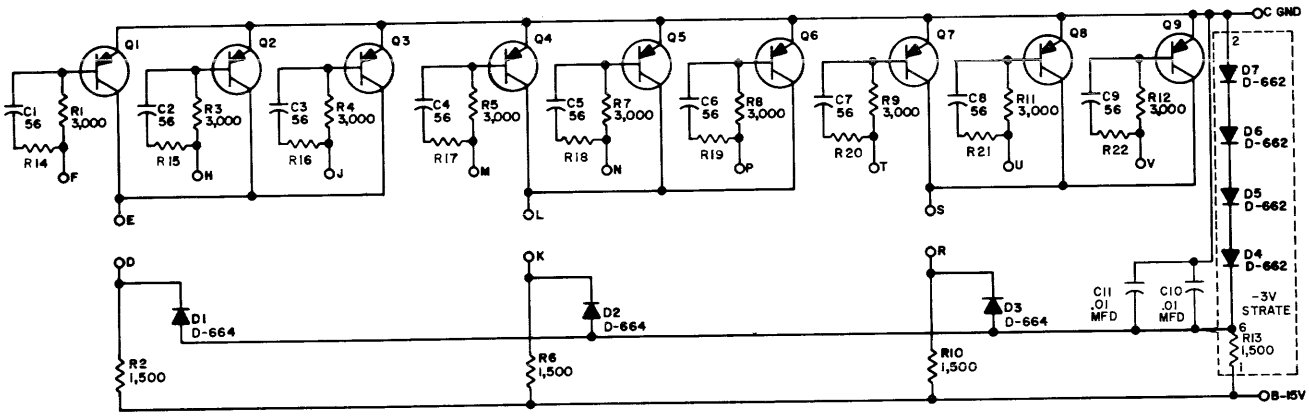
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
TRANSISTORS ARE DEC2894-1B
DIODES ARE D-664

Diode Gate RS-B-B113



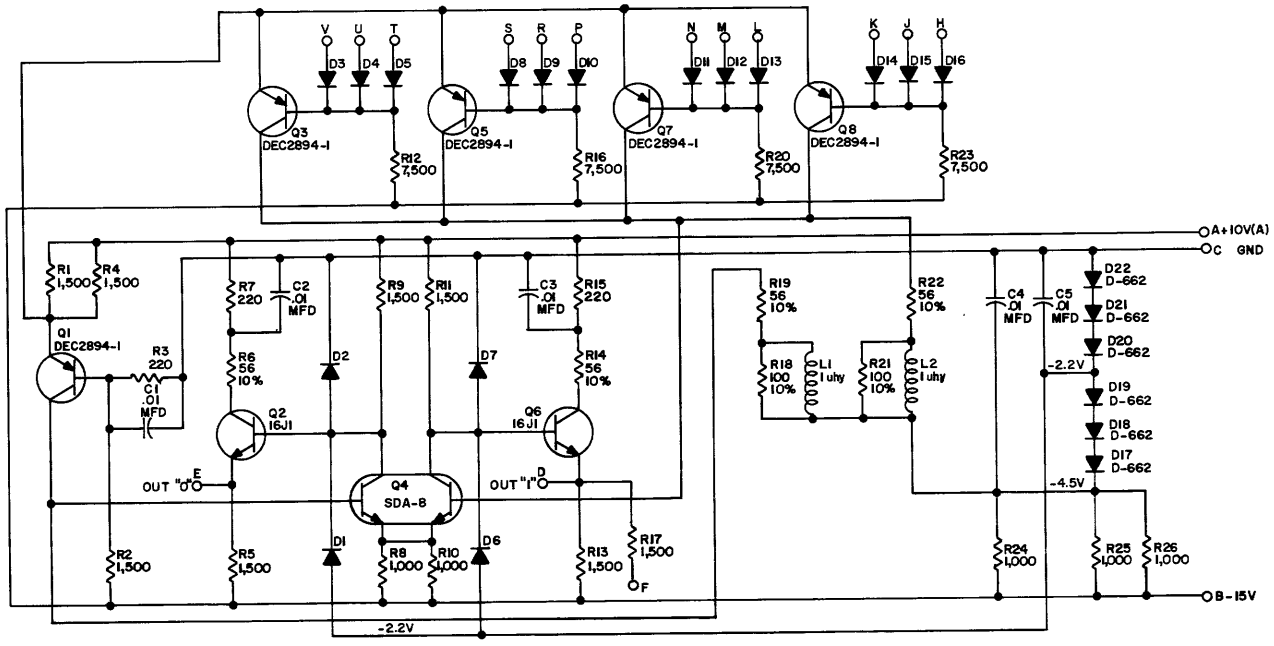
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-664

Diode Gate CS-B-B117



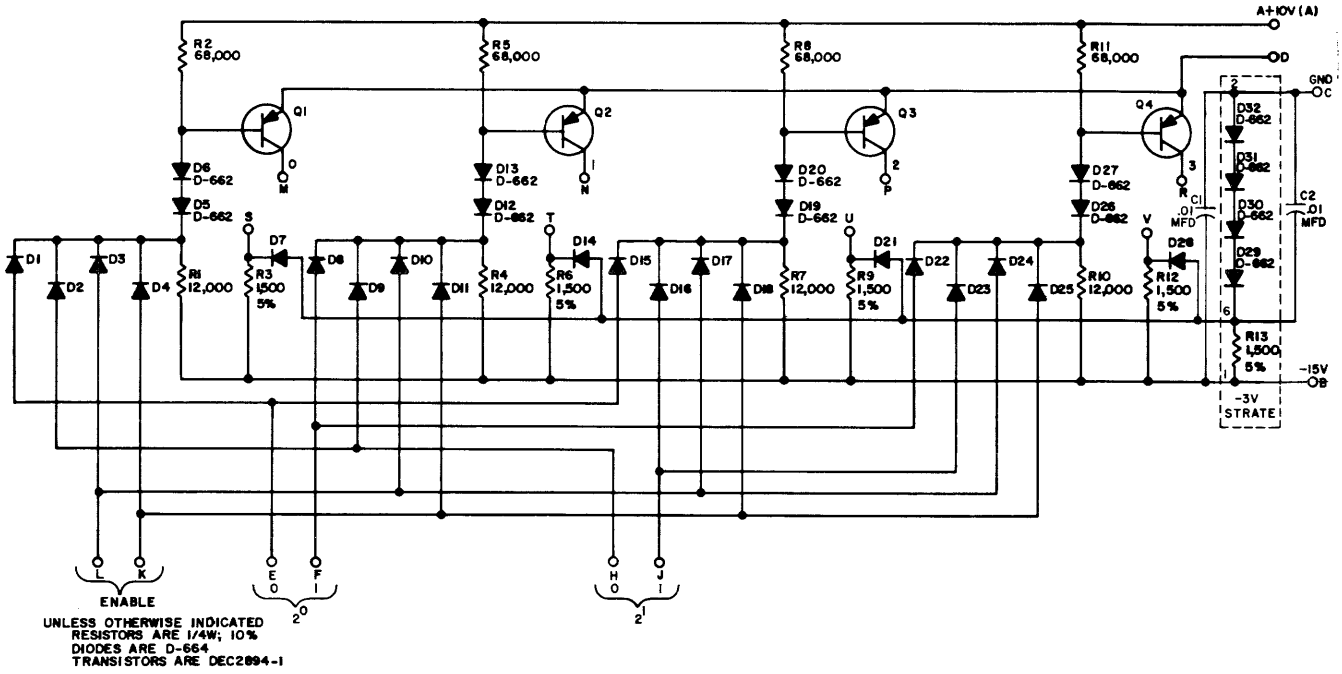
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-I
RESISTORS ARE 100; 1/4 W; 10%

Inverter RS-B-B124

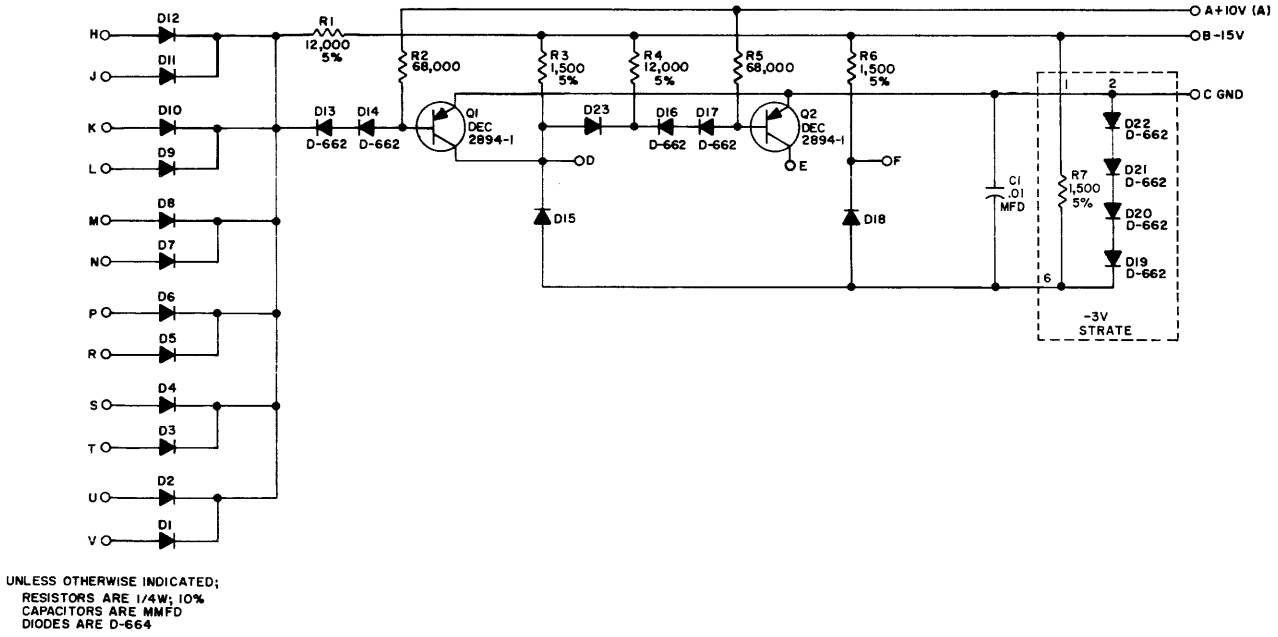


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664

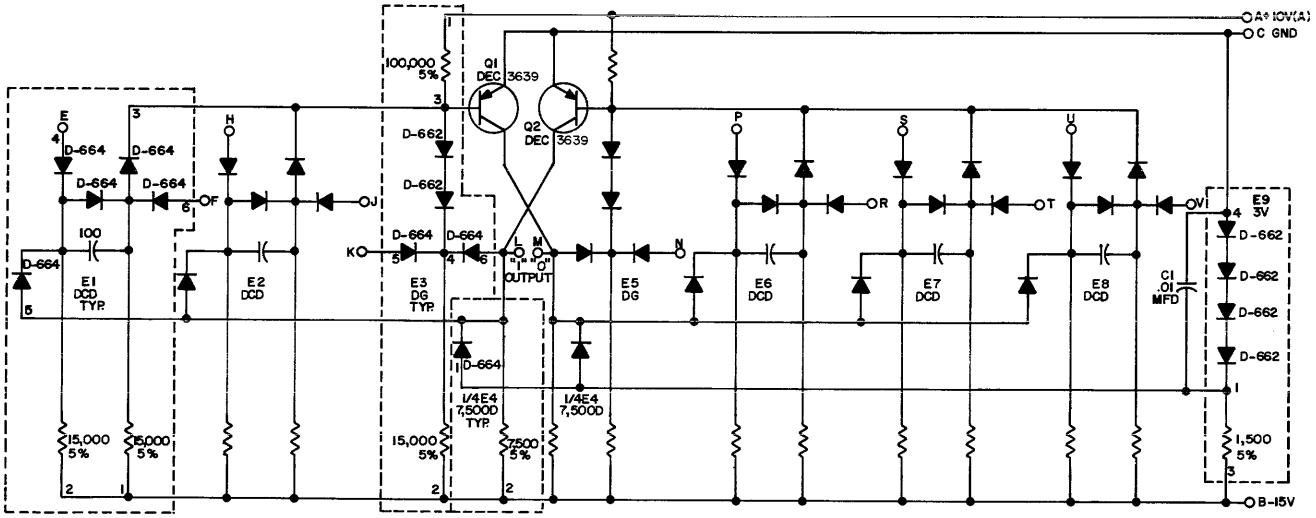
Three-Bit Parity Circuit RS-B-B130



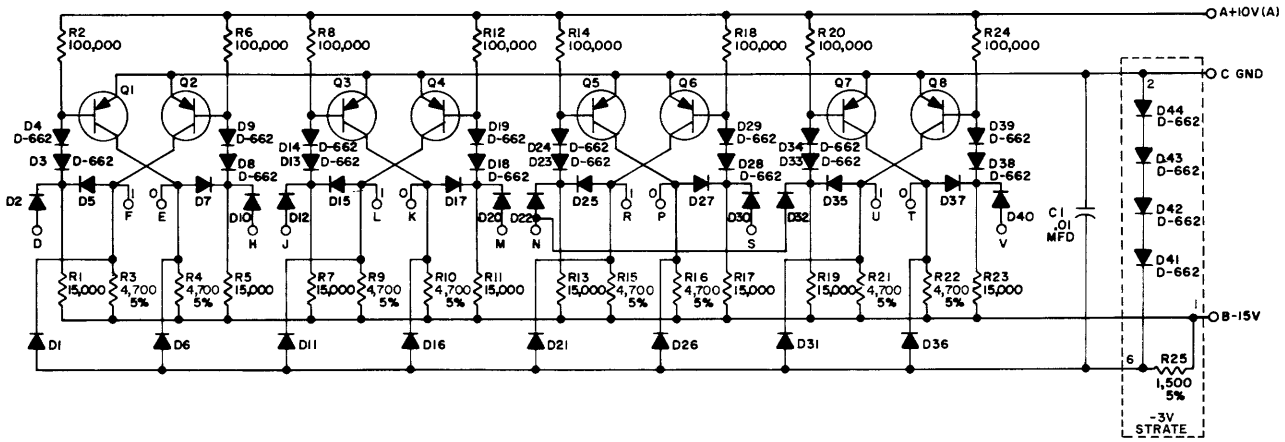
Half Binary to Octal Decoder RS-B-B155



Diode Gate RS-B-B171

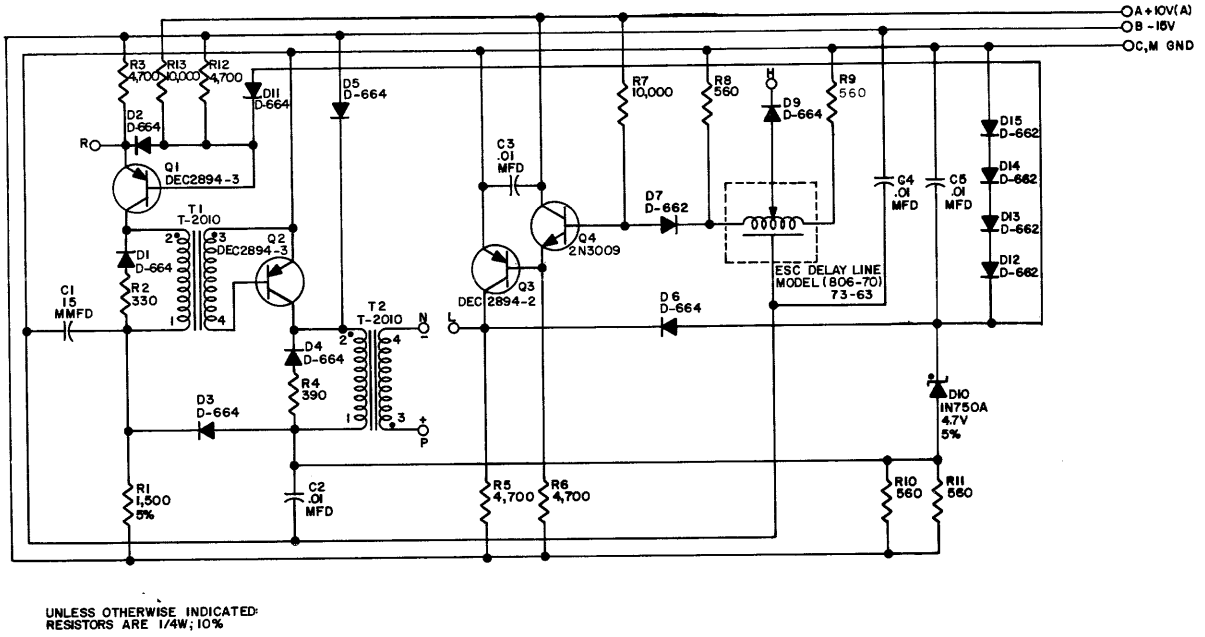


Flip-Flop RS-B-B201



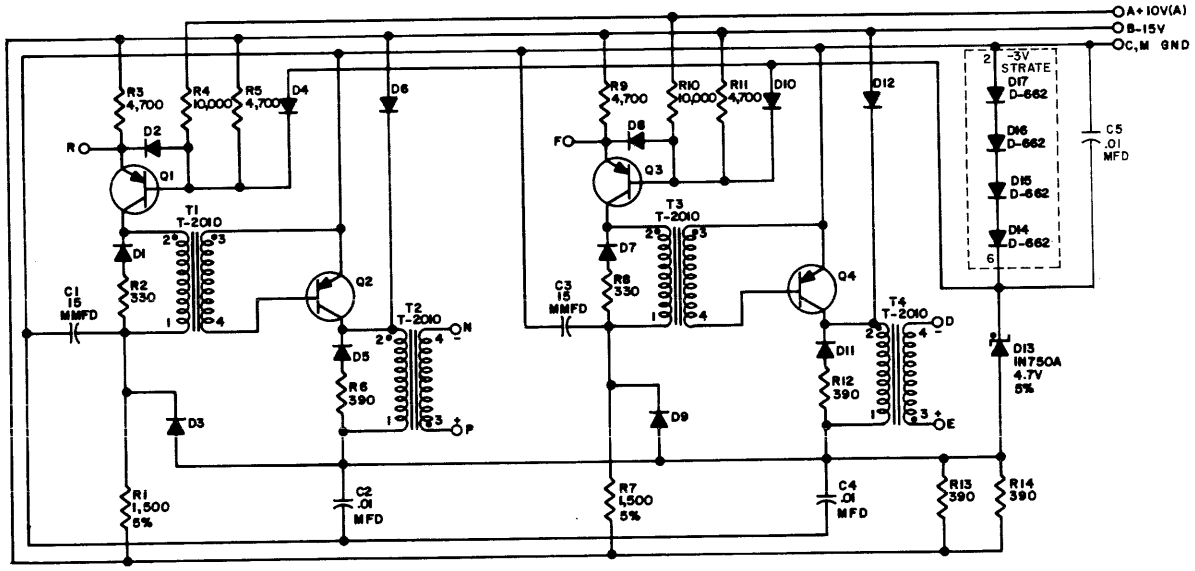
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639

Four Flip-Flops CS-B-B204



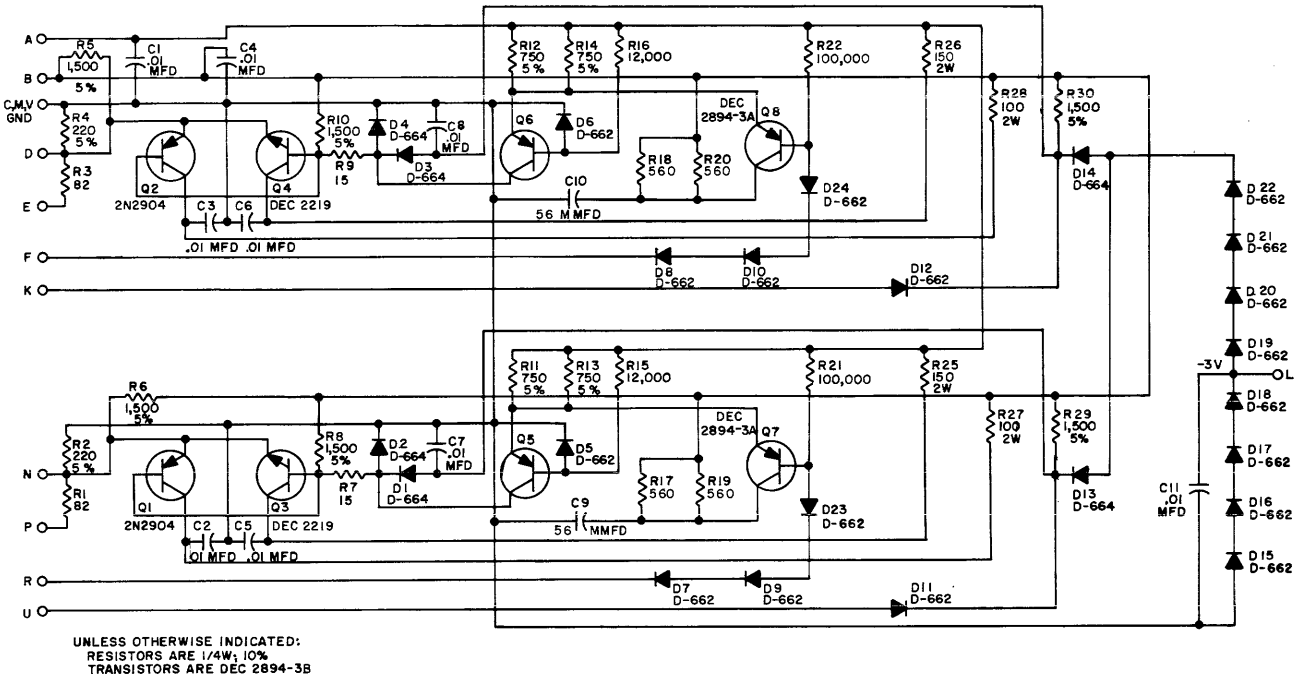
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%

Delay with Pulse Amplifier RS-B-B360



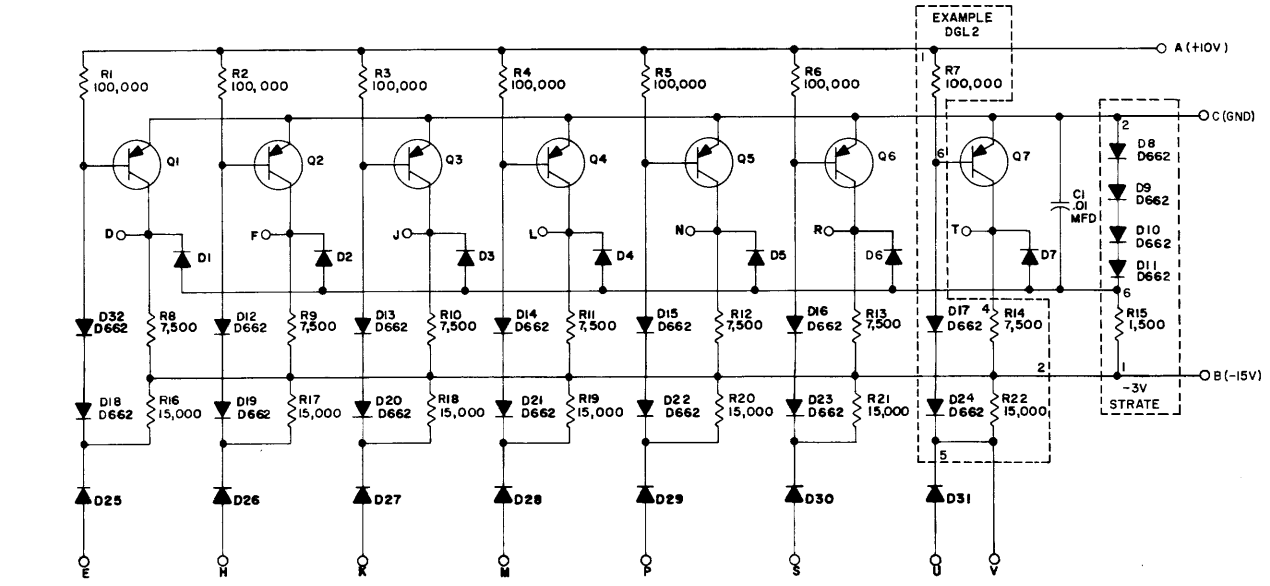
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC2894-3
DIODES ARE D-664

Pulse Amplifier RS-B-B602



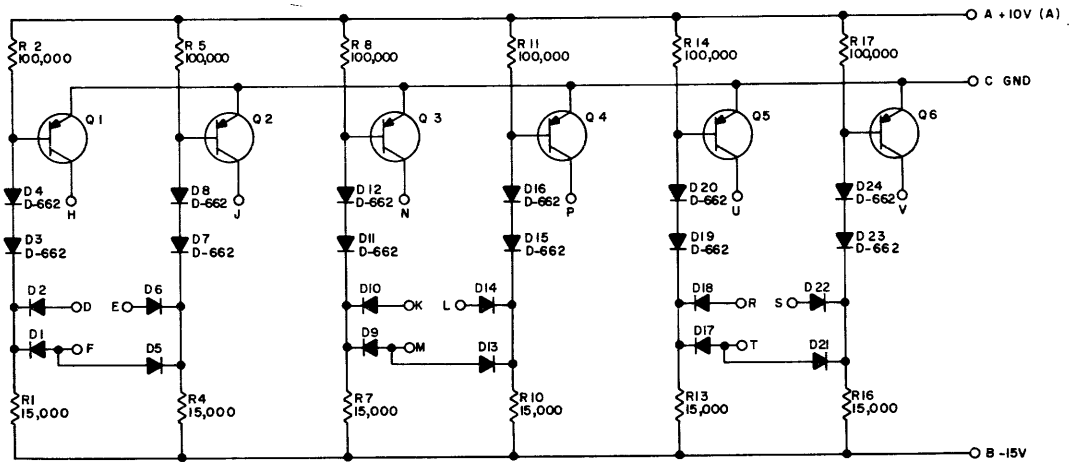
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC 2894-3B

Two Bus Drivers RS-B-B684



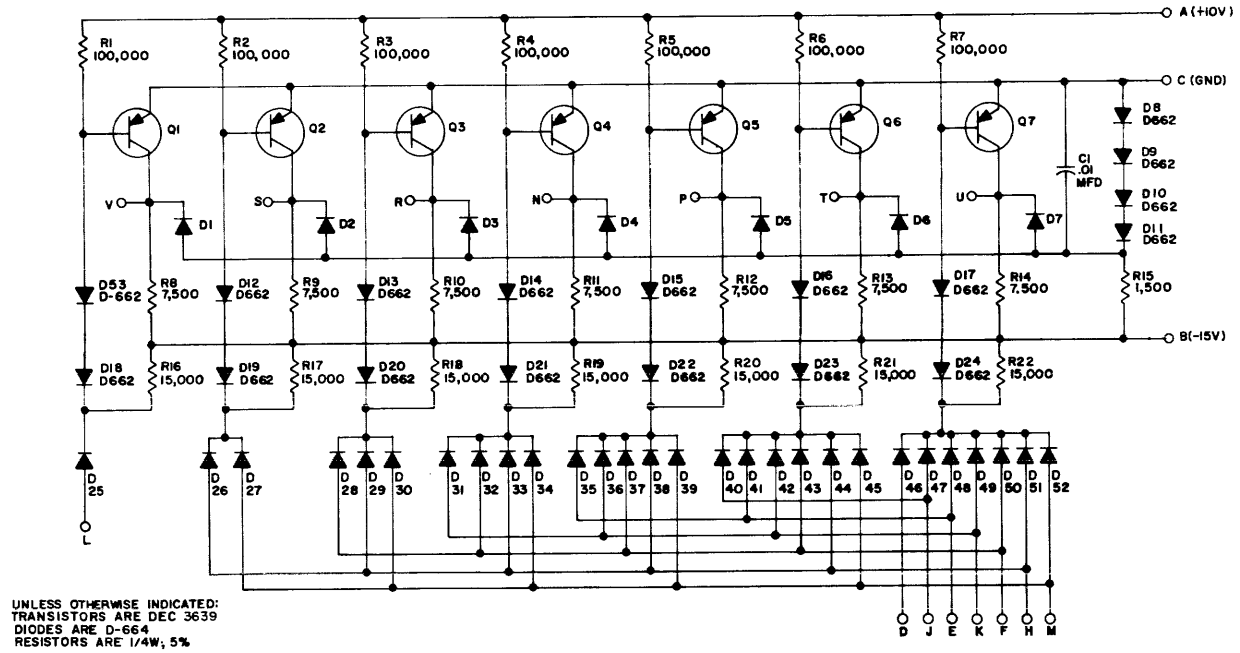
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Inverter CS-B-R107



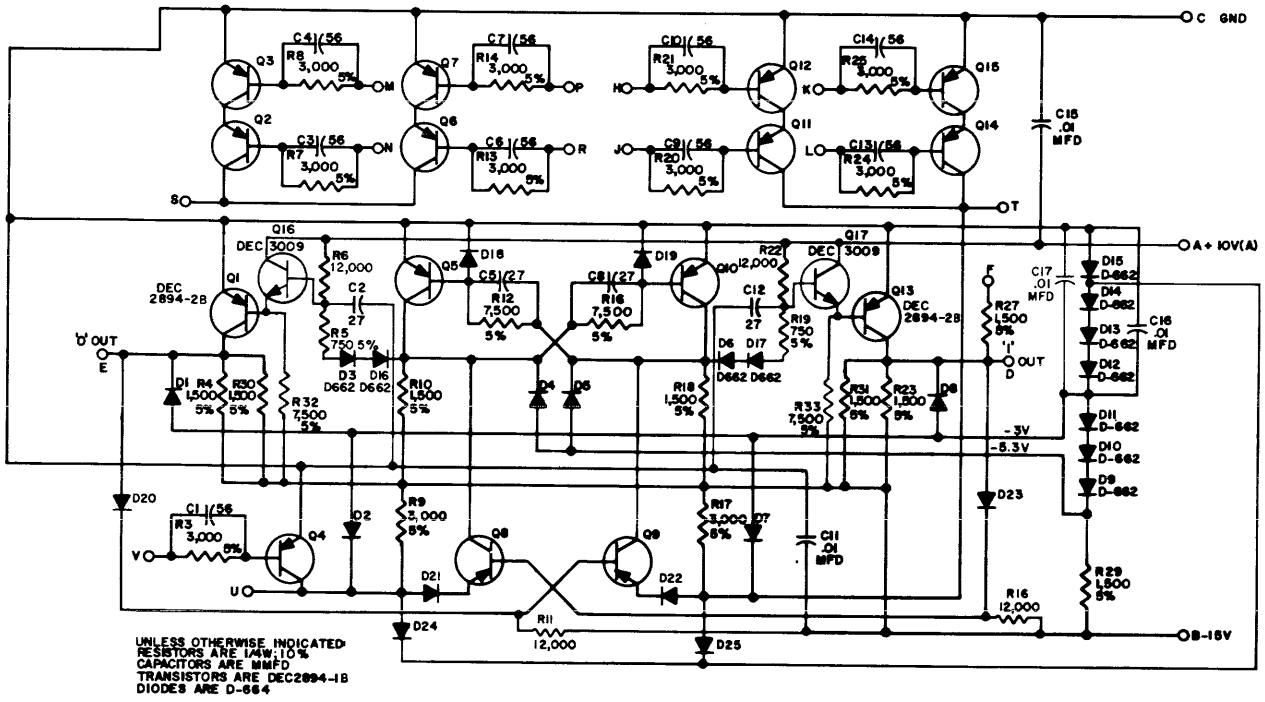
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

Diode Gate RS-B-R123

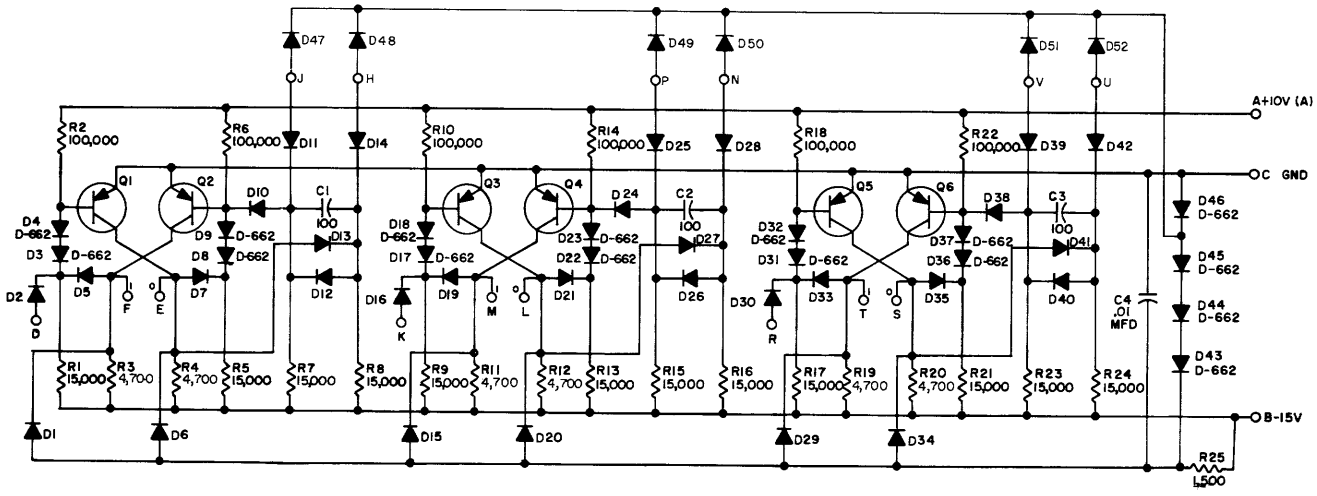


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
DIODES ARE D-664
RESISTORS ARE 1/4W; 5%

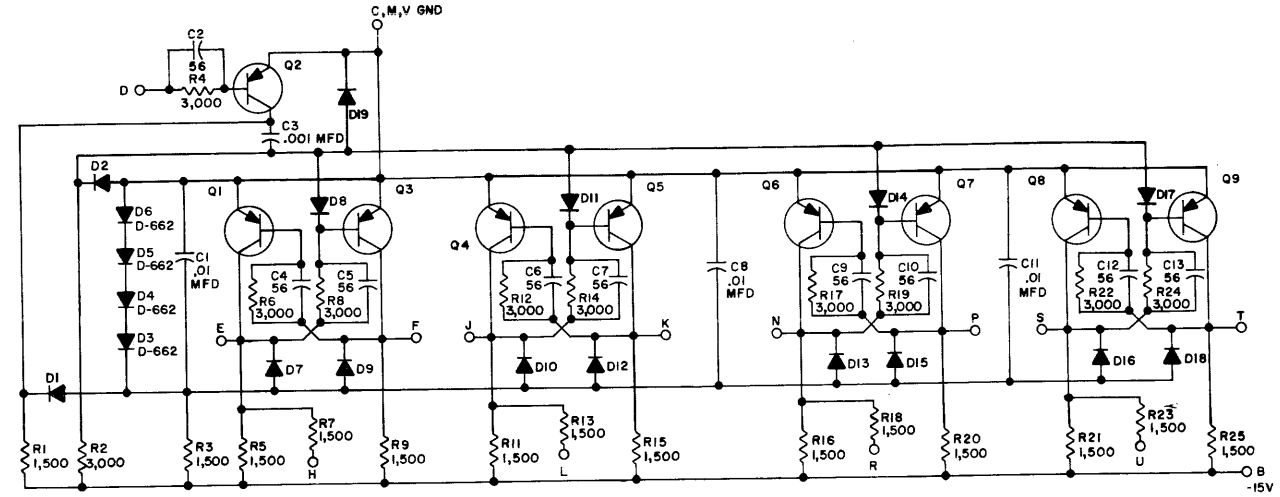
DC Carry Chain CS-B-R181



Flip-Flop RS-B-R201

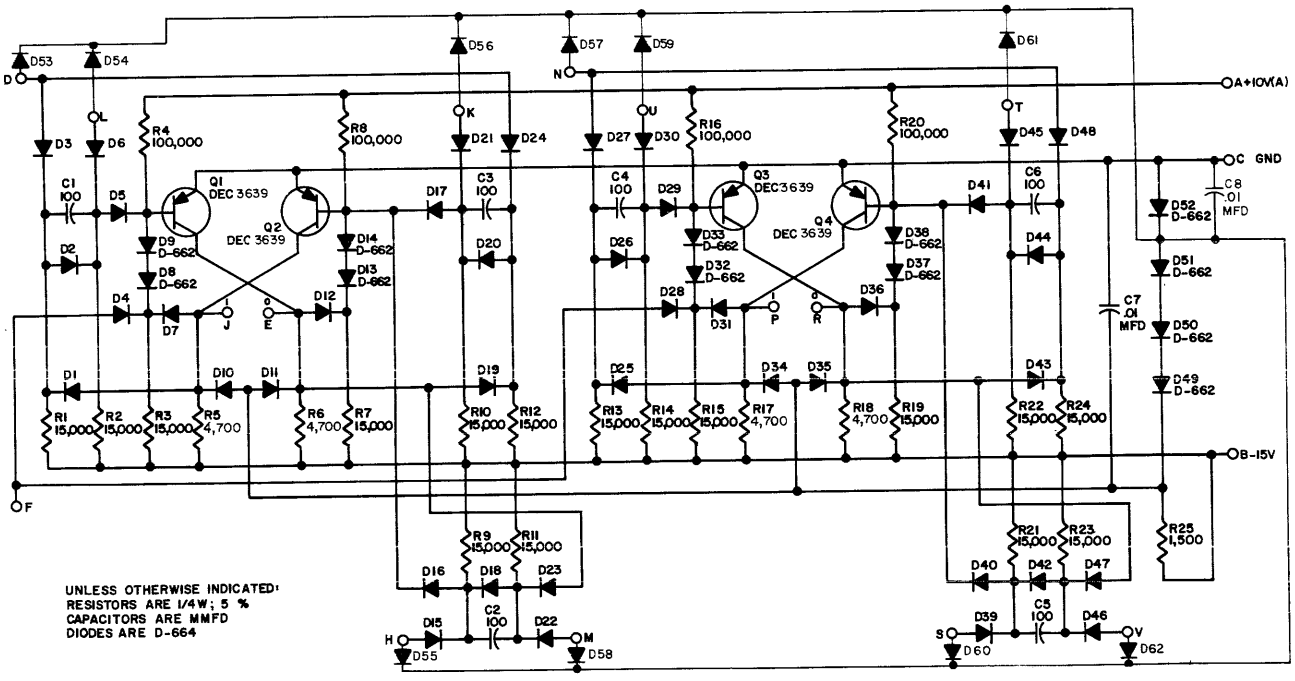


Triple Flip-Flop RS-B-R203



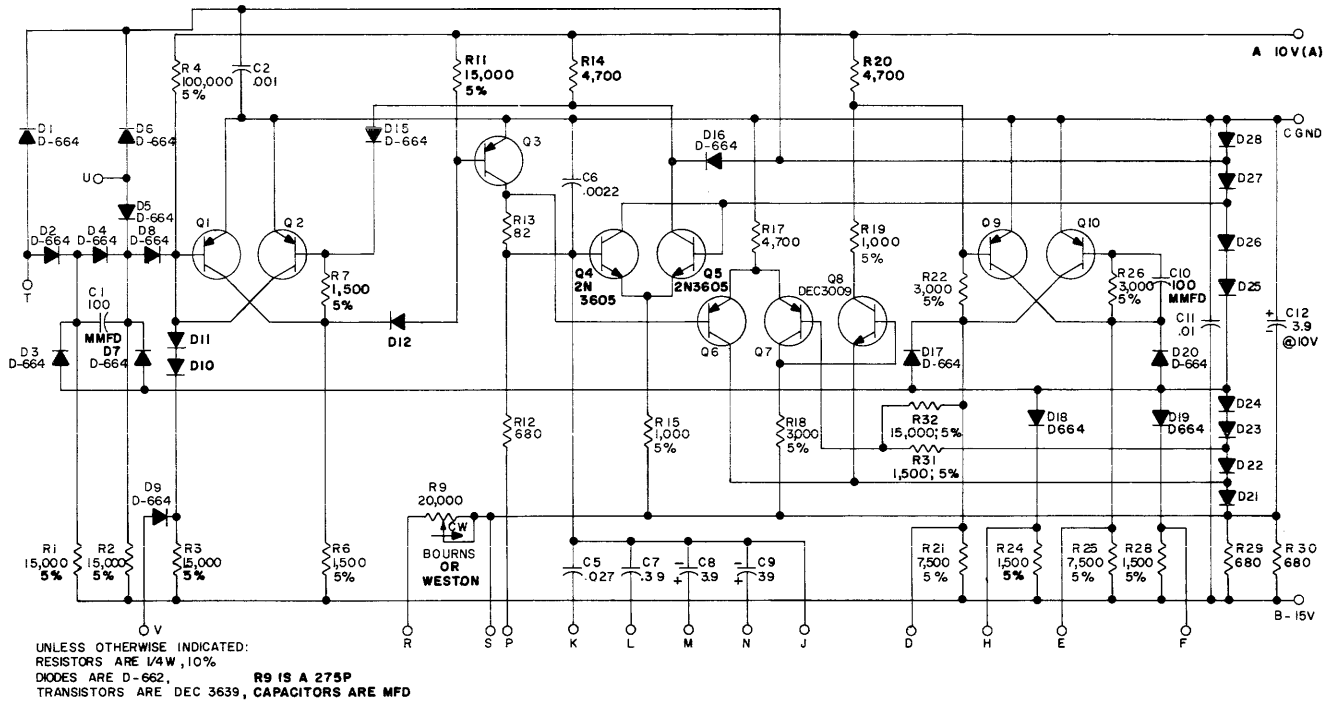
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC2894-18

Quadruple Flip-Flop RS-B-R204

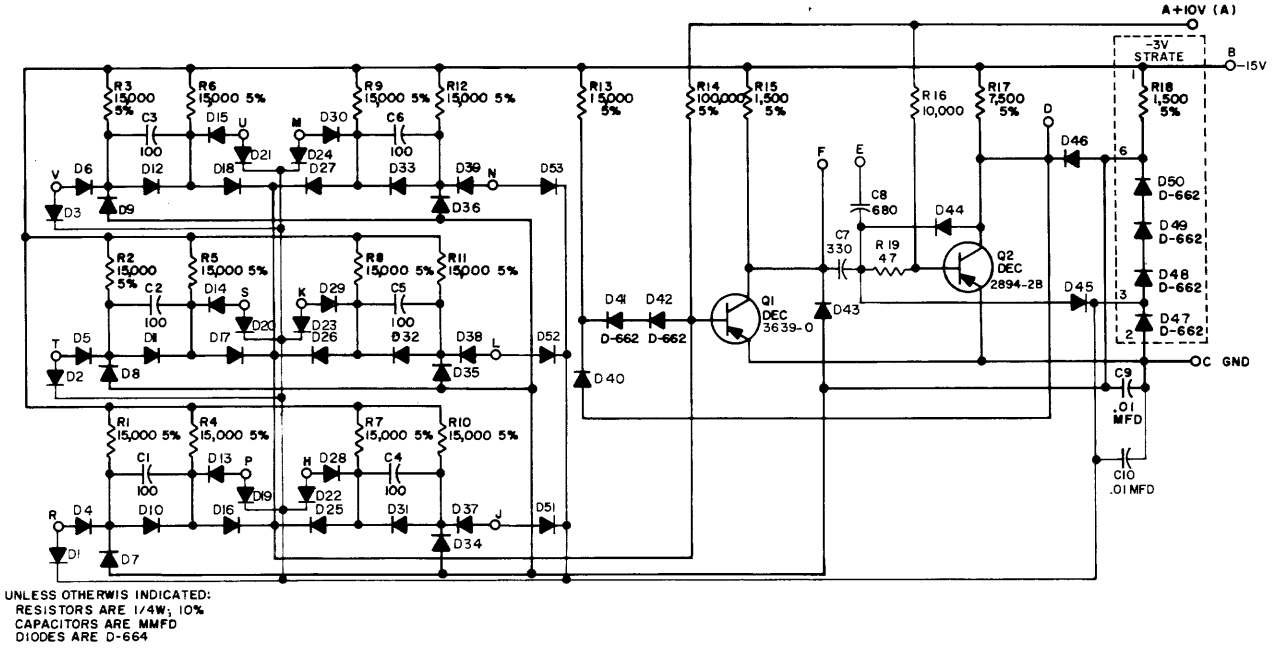


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5 %
CAPACITORS ARE MMFD
DIODES ARE D-664

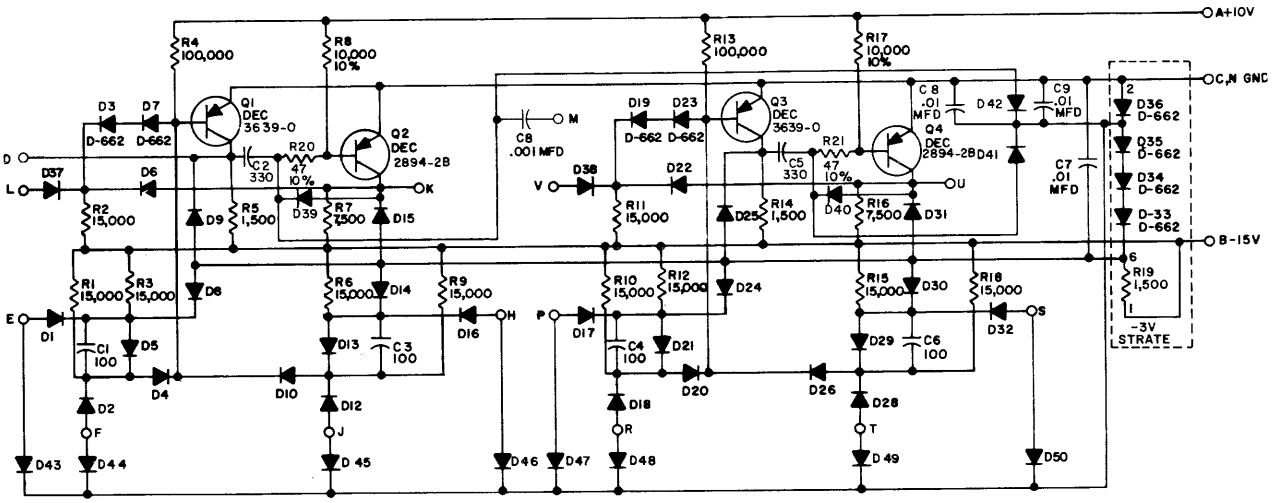
Dual Flip-Flop RS-B-R205



Intergrating One-Shot CS-B-R303

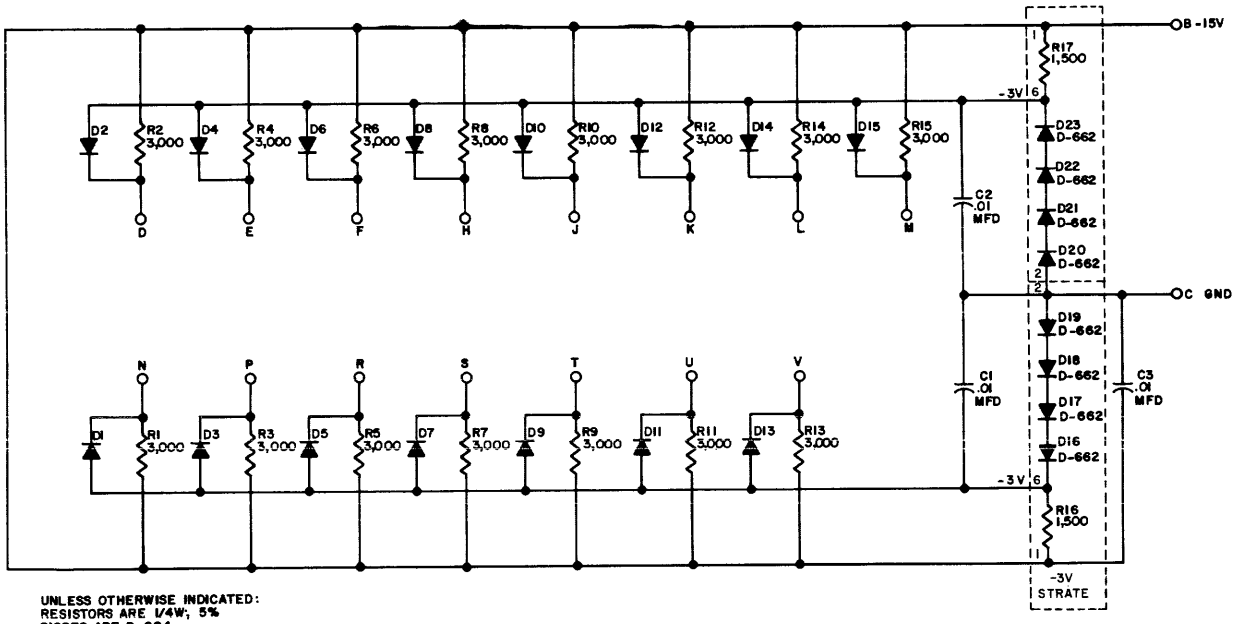


Pulse Amplifier RS-B-R601



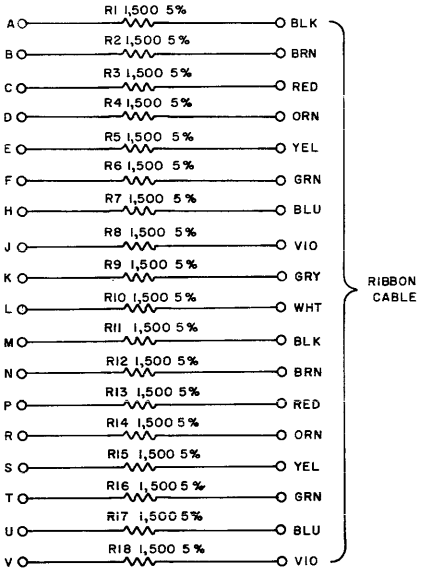
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Pulse Amplifier CS-B-R602



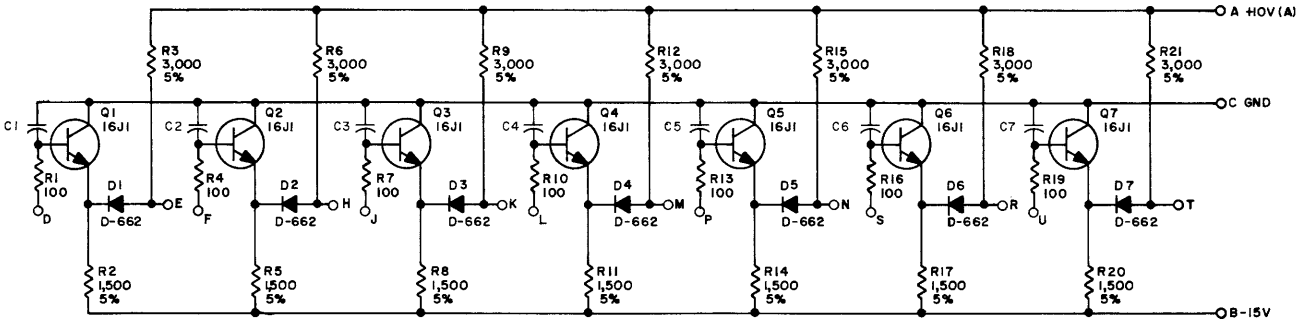
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664

Clamped Loads CS-B-W005



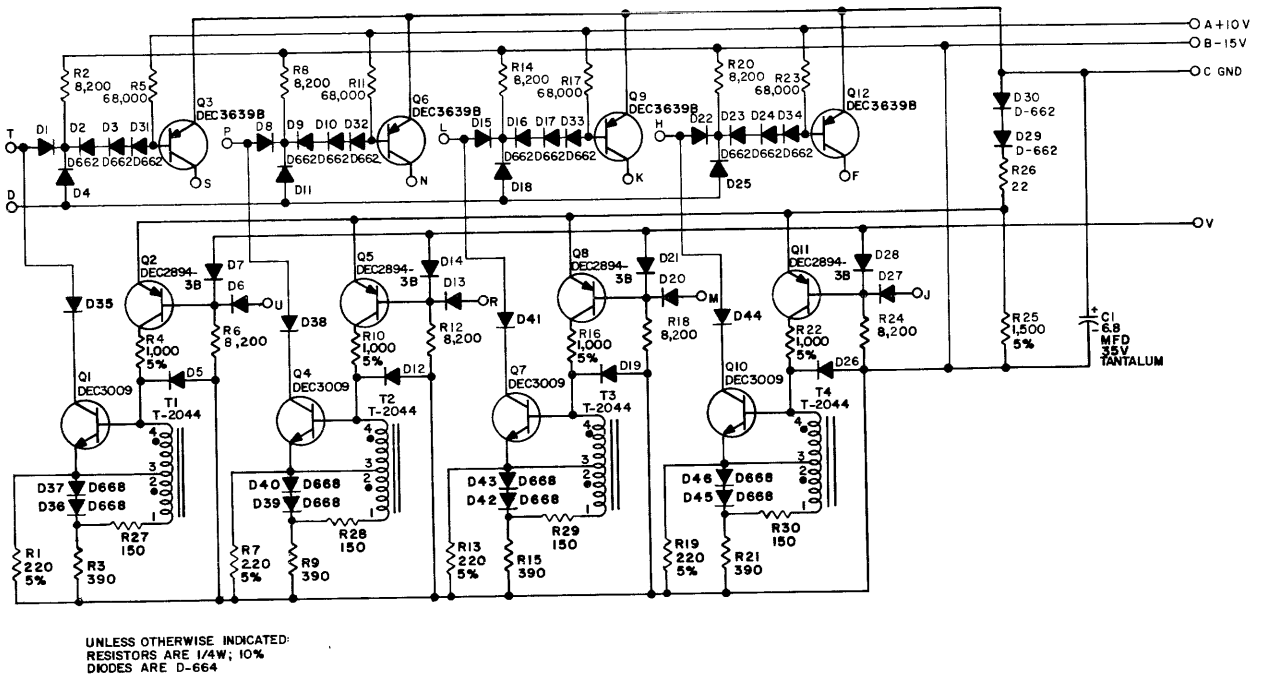
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W

Indicator Cable Connector RS-B-W020

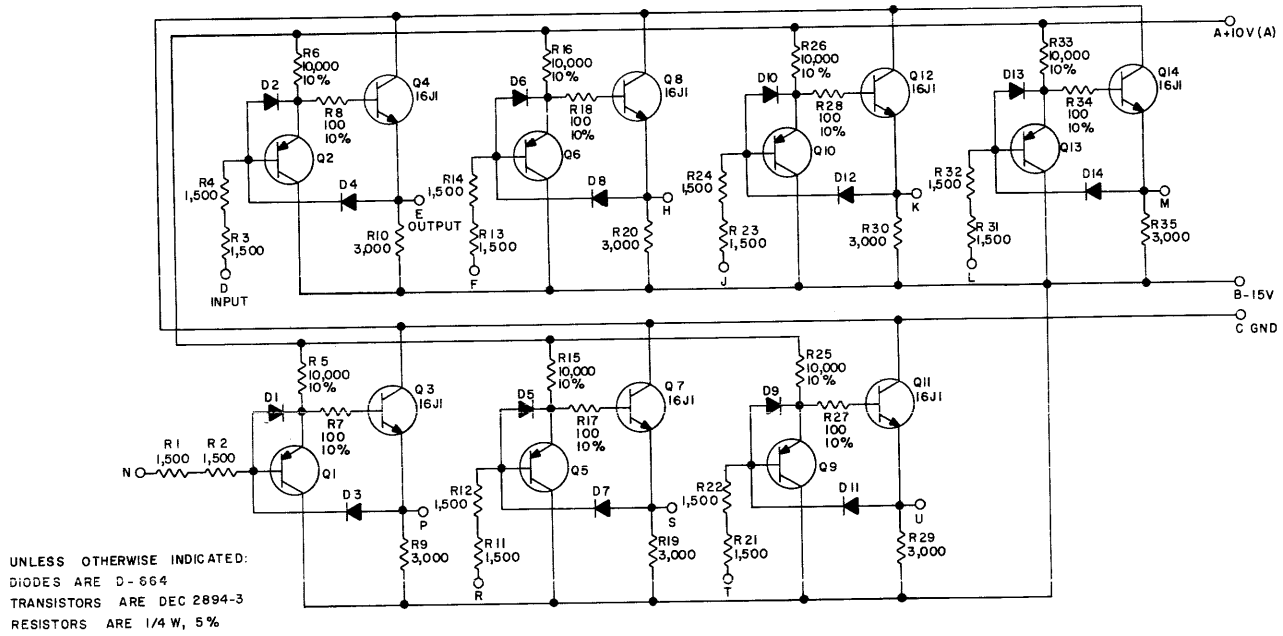


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE 120 MMFD

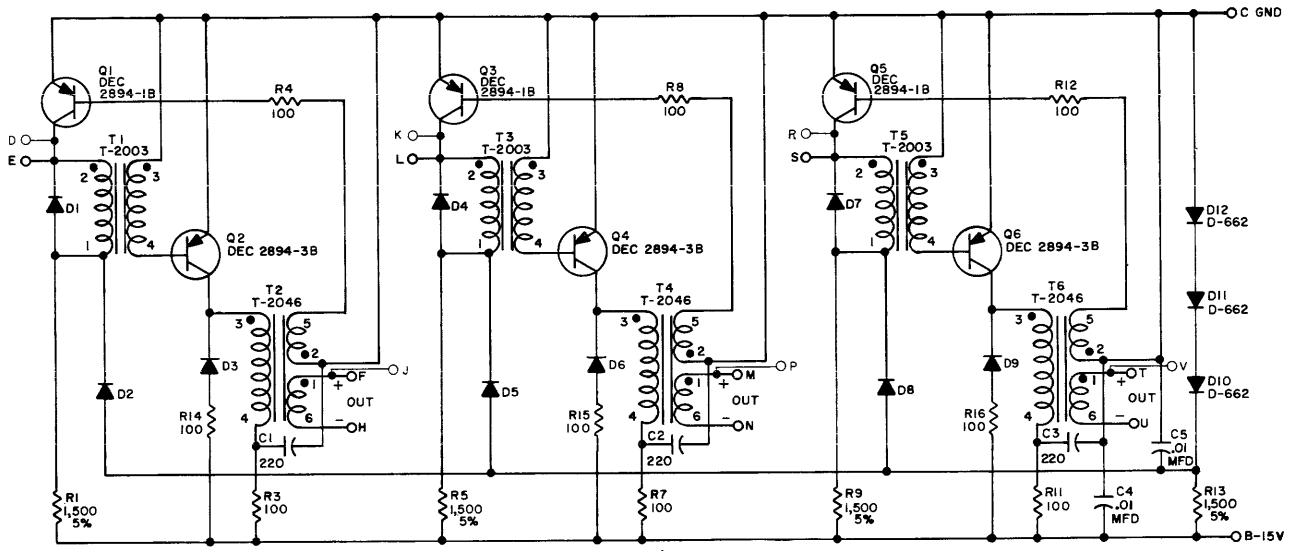
Emitter Follower RS-B-W100



Pulse Bus Transceiver CS-B-W102



High Impedance Follower RS-B-W500



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

Pulse Amplifier CS-B-W607