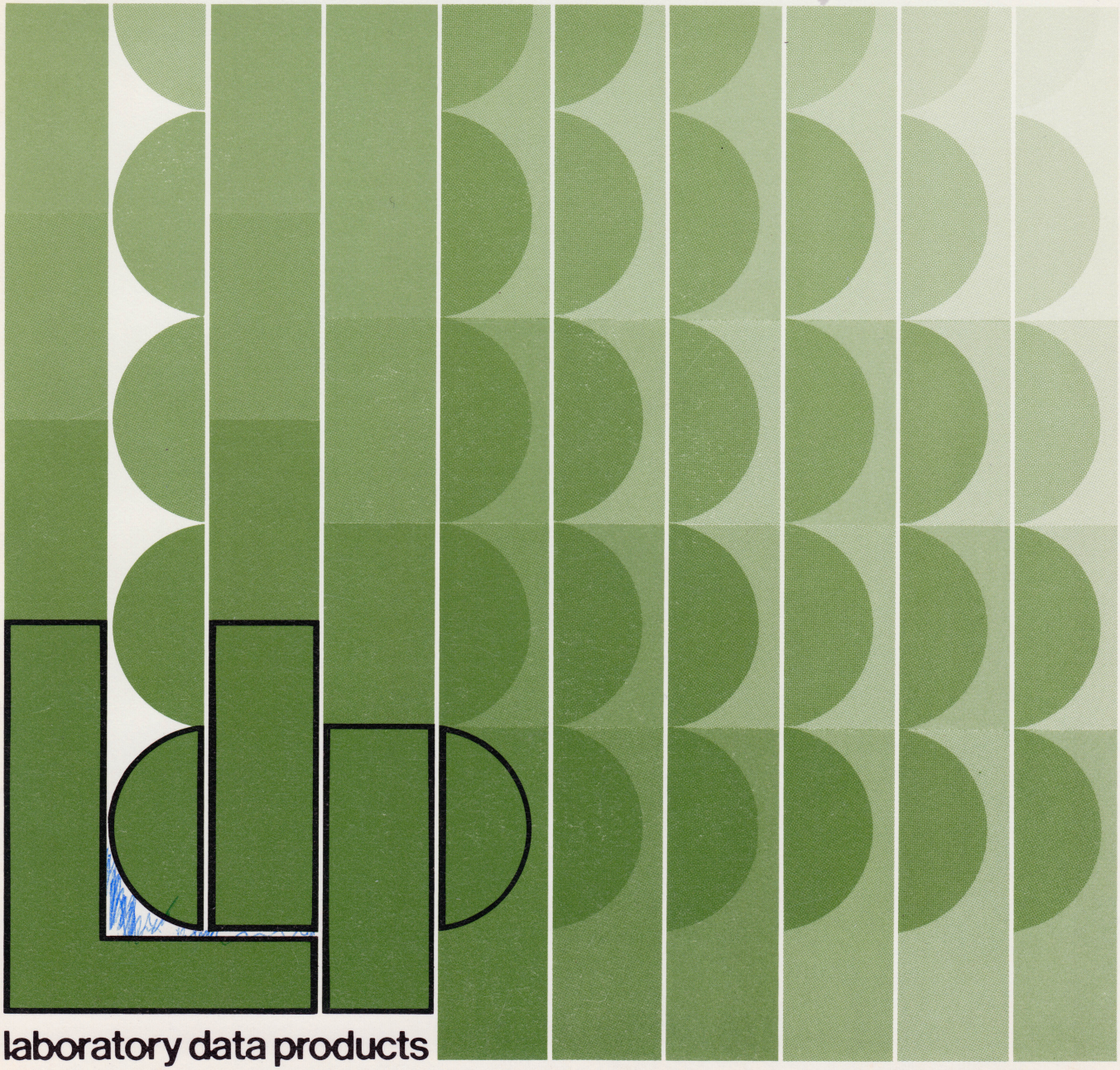
Digital Equipment Corporation
Maynard, Massachusetts

digital

AD8-A A/D converter user's guide



EK-AD8A-TM-001

AD8-A A/D converter user's guide

digital equipment corporation • maynard, massachusetts

1st Edition, April 1975

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CHAPTER 1
DESCRIPTION

1.1 GENERAL DESCRIPTION

The AD8-A A/D Converter enables the user to sample analog data at specified rates and to store the equivalent digital value for subsequent processing. The basic subsystem consists of a 16-channel multiplexer (16 single-ended inputs), sample-and-hold circuitry and a 10-bit A/D converter. The analog inputs can be programmed for unipolar (0–+5 V) or bipolar (±2.5 V) operation.

With the device code set to 53 and bit 06 (the Unipolar bit of the Enable register) cleared, the AD8-A is operationally compatible with the AD8-E.

1.2 FUNCTIONAL DESCRIPTION

The AD8-A is a 10-bit successive approximation converter, where the data output is right-justified in 2's complement binary for bipolar mode. The converter is controlled through the A/D Status, Enable, and MUX registers.

An A/D conversion may be started in three ways: under program control, on overflow of the real-time clock, or on an external input. These methods give the system the flexibility to serve in most applications requiring data acquisition.

The user can choose one of 16 single-ended channels of analog input through the MUX register and he can program for unipolar or bipolar input.

When a conversion is complete, a flag is set, and if the A/D interrupt is enabled, the processor is interrupted. The user can run in the interrupt mode or wait for the appearance of the A/D DONE flag.

The multi-channel throughput rate is 25 kHz for mixed unipolar and bipolar channels, and 28 kHz for non-mixed channels on the PDP-8E.

Because of a double-buffered data output, a second conversion can be started before the results of the first conversion are read so that these operations can be overlapped to achieve high throughput. Single-channel throughput rate with clocked or external starts is 30 kHz.

Since the device code is user-selected, multiple AD8-As may be used per system by setting each AD8-A for a different device code. Illegal codes such as 00 (internal IOT microinstructions) or other option codes should *not* be used.

1.3 SPECIFICATIONS

1.3.1 Electrical

Input voltage range	0 – +5 V -2.5 – +2.5 V } Program-selectable
Resolution	10 bits (1 part in 1024)
Accuracy (at 25° C)	0.1% of full scale
Number of channels	16 (single-ended)
Switching	break-before-make
Linearity	1/2 LSB (0.05% of full scale range)
Differential linearity	95% of states within ±1/2 LSB; no skipped states
+5 V Supply output	20 mA, max.

A/D Timing (μs)

Programmed Start	Multiplexer switching (S & H)	0–11*
	Clock synchronization	0–2
	Hold delay	2
	Conversion	20
		22–35
Single channel External or Clock Start	Clock synchronization	0–2
	Hold delay	2
	Conversion	20
	S & H reacquisition	4
		26–28

Minimum single channel throughput rates with optimal coding:	PDP-8,E,M,F	PDP8-A
Programmed start	28.5 kHz	27.5 kHz
Overflow or external start	30.0 kHz	29.0 kHz

Input impedance	10M min.; $-5\ V \leq V_{in} \leq +5\ V$
Input bias current	100 nA max., unselected channel -2 μA max., selected channel } $-5\ V \leq V_{in} + 5\ V$
S & H tracking	Small signal bandwidth 700 kHz Large signal slew rate limit 1 V/μs
S & H aperture	200 ns max. delay 1 ns jitter

*Depends on time from last MUX change to A/D start; may be made 8 μs by removing W3.

Repeatability	1/4 LSB max. rms noise
Crosstalk	-80 dB at 1 kHz, rolling off at -20 dB per decade
Temperature stability	Gain = 50 ppm/° C Linearity = 25 ppm/° C
Warmup time	5 minutes
Control	Programmed instructions, clock counter overflow, or external input
Output format	Parallel, 10 bits, right-justified, binary, double-buffered
Power	+5 Vdc ± 5% @ 3.25 A max.

1.3.2 Environmental (ref. DEC STD. 102, Class C)

Operating	
Temperature	5° – 50° C system amb. 5° – 70° C module amb.
Humidity	10% – 90%
Storage	
Temperature	-40° – +66° C
Humidity	95% max

1.3.3 Packaging

The AD8-A is a single A008 quad size module which mounts in a PDP-8 Omnibus. Two RFI shields are included with this option which should be mounted on each side of the A008 module. These shields do not require an Omnibus slot. For improved performance, the AD8-A may be mounted so that at least one slot adjacent to each side of the A008 is left empty, or that the A008 is the last module on the bus assembly with the adjacent slot left empty.

CHAPTER 2
USER INTERFACING

2.1 BERG CONNECTOR

Analog input signals are interfaced through the Berg connector located in the upper right corner of the AD8-A module. Pin assignments for connector lines are shown in Table 2-1.

Table 2-1
A/D Berg Cable Pin Assignments

Signal	Pin	Pin	Signal
Channel 0	VV	MM	Analog Ground
Channel 1	TT		
Channel 2	RR	KK	Analog Ground
Channel 3	NN		
Channel 4	LL	HH	Analog Ground
Channel 5	JJ		
Channel 6	FF	EE	Analog Ground
Channel 7	DD		
Channel 10	BB	CC	Analog Ground
Channel 11	Z		
Channel 12	X	AA	Analog Ground
Channel 13	V		
Channel 14	T	Y	Analog Ground
Channel 15	R		
Channel 16	N	W	Analog Ground
Channel 17	L		
+5 V out	UU	K, M	Analog Ground
EXT ST L	U	S, P	Logic Ground
-13 V (test only)	PP	SS	+13 V (test only)

2.2 ANALOG INPUTS

2.2.1 Grounded and Floating Inputs

Two types of analog signals may be used as AD8-A inputs – grounded and floating. A *grounded* signal level is referenced to the instrument ground which is producing the signal (Figure 2-1). Since the instrument may be located some distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the AD8-A input is the sum of this unwanted ground difference voltage and the desired signal voltage.

In cases where the input voltage is referenced to the user's ground a wire should not be run from the user's ground to the AD8-A analog ground; this could cause undesirable ground loop currents which affect results not only on the input channel in question, but also on other channels. The ground difference should be minimized by plugging the instrument into an ac socket as close to the computer as possible.

A *floating* signal voltage is measured with respect to a point which is not connected to ground. Examples of this type of analog input are shown in Figure 2-2.

The return line of a floating signal must be connected to one of the AD8-A analog input grounds (Table 2-1). Although there are only 10 analog input grounds for the 16 analog input channels, these grounds may be shared among channels (as illustrated by the battery-powered sources in Figure 2-2) in which multiple inputs from a single battery-powered instrument share a common return line. Note that the identifying characteristic of a floating source is that connecting the signal return to the AD8-A ground does *not* result in a current path between the AD8-A ground and the instrument ground.

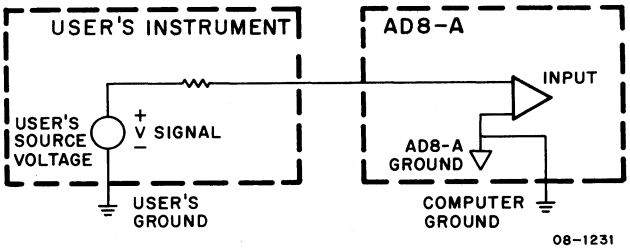


Figure 2-1 AD8-A Input Referenced to User's Ground

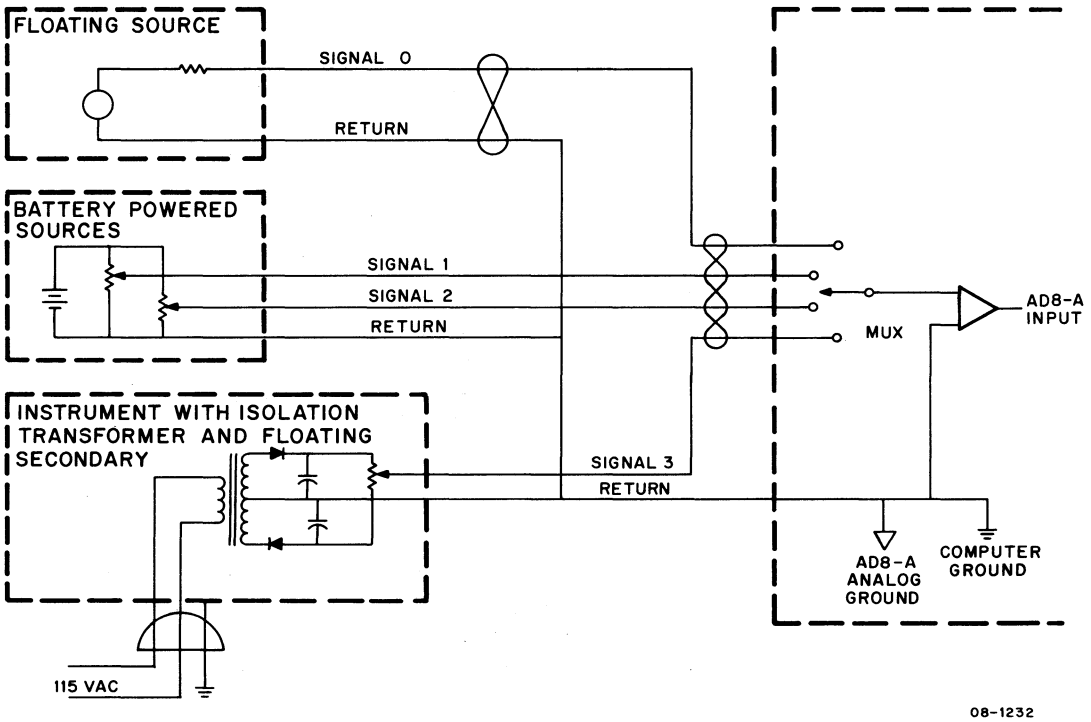


Figure 2-2 Floating AD8-A Input Signals

2.2.2 Twisted Pair Input

The effects of magnetic coupling on the input signals may be reduced for floating inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the AD8-A input is zero. Twisted pairs have no effect with a single-ended, non-floating signal (referenced to ground at the instrument end).

2.2.3 Shielded Input

The effects of electrostatic coupling on the input signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. The shield should be connected to ground at *one* end of the cable only so that it does not carry any current.

2.2.4 Input Settling with High Source Impedance

All solid-state multiplexers have the unavoidable side effect of injecting a small amount of charge into their input lines when changing channels, causing a transient error voltage which is discharged by the input signal's source impedance.

When starting a conversion, an 11-μs interval is allowed for the AD8-A multiplexer and sample-and-hold to settle to the correct value of the newly selected channel before the conversion begins. Normally, this is sufficient time for the input transient to settle out, however, more time may be needed when switching into an input channel with high source impedance. It may be necessary to either reduce the signal's source impedance or preset the multiplexer channel and provide a software delay before starting the conversion.

2.3 +5 VOLT SUPPLY

The +5 V supply output, pin UU of the AD8-A Berg connector, may be used to power potentiometers whose wipers provide AD8-A input signals, as shown in Figure 2-3. Such potentiometers may be repeaters, measuring mechanical shaft positions, or panel-mounted, for use as program parameter inputs.

The AD8-A input channel should be run with unipolar range (0 – +5 V) so that full travel of the potentiometer wiper corresponds to 7000–0777 A/D output (ignoring the effect of the potentiometer's end resistance).

No more than 20 mA of current should be drawn from the +5 V output. Use of 5K potentiometers is recommended; this value will limit current from the +5 V output to 16 mA with potentiometers on all channels, while presenting a maximum signal source impedance of 1.25K to the AD8-A input.

Depending upon which PDP-8 Omnibus processor is used, significant ripple (up to 3%) may exist on the +5 V output, and appropriate digital filtering or averaging should be considered on potentiometer channels utilizing this reference voltage. If absolute gain accuracy is important for the application, it will be necessary to adjust the processor power supply for exactly +5 V at pin UU.

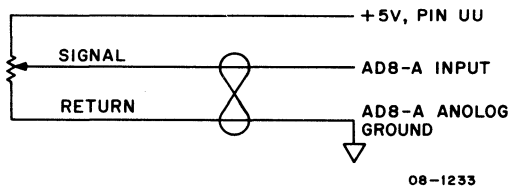


Figure 2-3 Use of +5 V Supply Output

2.4 EXTERNAL STARTS

The external start signal line (EXT ST L), pin U of the Berg connector, is a TTL-compatible input which sees two TTL unit loads. Conversions start on the high-to-low transition of this signal.

In most cases, the source of the external start signal is a grounded (non-floating) signal generator or logic circuitry located in a grounded instrument. Like the analog input signals, the return path for the EXT ST signal is through the grounds; a separate return wire should not be run. The ground difference between the signal source and the computer should be minimized in order to prevent spurious start pulses due to ground noise.

In the case of a floating pulse generator only, the pulse generator's logic ground should be connected to the AD8-A's logic ground, pin S of the Berg connector.

2.5 JUMPERS

The Analog section of the AD8-A option is equipped with a jumper (W3) which may be removed at the user's option. The AD8-A is shipped with a nominal multiplexer sample-and-hold settling delay of 11 μs, which is sufficient to guarantee inter-channel settling to within 1/2 LSB when switching between a bipolar and unipolar channel. (7.5 V maximum inter-channel voltage). If the user can guarantee switching between bipolar and bipolar or unipolar and unipolar (5 V maximum inter-channel difference), he may elect to disconnect jumper (W3), changing the settling time from 11 μs to 8 μs and decreasing the multi-channel throughput time by 3 μs.

CHAPTER 3
PROGRAMMING

3.1 DEVICE CODES

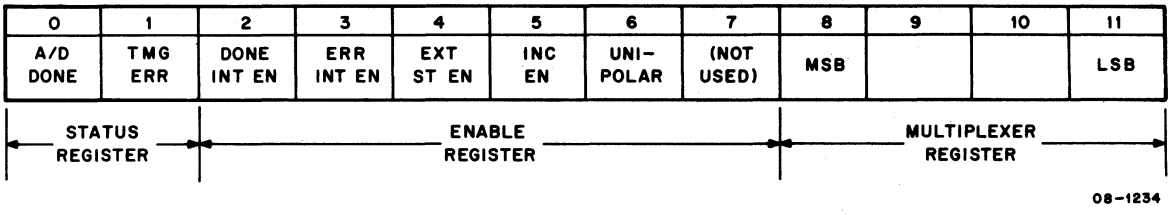
The switch pack (S1) on the A008 module selects the device code of the A/D converter: An OFF switch decodes a 1; an ON switch decodes a 0. Switches S1-1 and S1-2 are unused, S1-3 is the MSB of the device code, and S1-8 is the LSB.

Example

Desired device code = $53_{(8)}$
= 101011 (binary)

SET:	S1-3	OFF	(1)	
	S1-4	ON	(0)	$5_{(8)}$
	S1–5	OFF	(1)	
	S1–6	ON	(0)	
	S1–7	OFF	(1)	$3_{(8)}$
	S1–8	OFF	(1)	

3.2 REGISTERS



The initialized state of all bits of all registers is 0.

3.2.1 Status Register (AC bits 0 and 1)

A/D DONE (Bit 0) is set (1) when a conversion is completed; the buffer is updated 1 μs later.

TMG ERR (Bit 1) is set (1) when a start conversion is attempted while a conversion is in progress; when the buffer is updated while it is being read.

3.2.2 Enable Register (AC bits 2–7)

DONE INT EN (Bit 2) when set (1) from the AC, enables the INT RQST line to interrupt when A/D DONE is set.

ERR INT EN (Bit 3) when set (1) from the AC, enables the INT RQST line to interrupt when TMG ERR is set.

EXT ST EN (Bit 4) when set (1) from the AC, enables the external A/D start conversion circuit to initiate conversion from DK8-E or an external source.

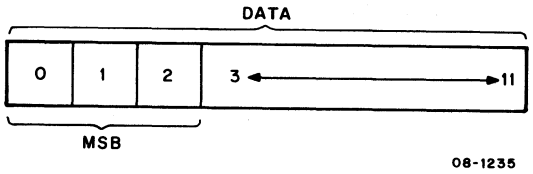
INC EN (Bit 5) when set (1) from the AC, auto increments the MUX register to the next sequential channel at the end of each conversion.

UNIPOLAR (Bit 6) when set (1) the input voltage range is 0 to +5 V. When reset to 0, the input voltage range is ±2.5 V.

3.2.3 Multiplexer Register (AC Bits 8–11)

The MUX register is loaded from the AC and is the current channel being monitored by the AD8-A. One of 16 channels is selected by loading the channel number ($00–17_8$) into this register.

3.2.4 A/D Buffer



Input Volts	10-Bit Results (octal)	Type
Bipolar		
Most positive – 2.495	0777	Sign extended
Mid range – 0	0000	2's complement
Most negative – -2.5	7000*	binary
Unipolar		
Most positive – 4.995	0777	10 bits
Mid range – 2.5	0000	right-justified
Most negative – 0	7000*	binary

*The three MSBs are tied together.

3.3 INSTRUCTIONS

Eight instructions are used to program the AD8-A. The device code (XY) is preset by the user using switches (Section 3.1) on the AD8-A (A008 module).

CLEAR ALL (ADCL) – 6XY0

Clear MUX and Enable registers
Clear DONE and ERROR flags (Status register)

LOAD MUX REGISTER (ADLM) – 6XY1

Load MUX register from AC, then clear AC

START CONVERSION (ADST) – 6XY2

Clear A/D DONE and ERROR flags, then initiate a conversion on the current channel

READ A/D BUFFER (ADRB) – 6XY3

Transfer contents of A/D buffer into AC bits 0–11 (bits 0–2 are MSB) and clear the A/D DONE flag

SKIP ON A/D DONE (ADSK) – 6XY4

Skip the next instruction if A/D DONE = 1

SKIP ON TIMING ERROR (ADSE) – 6XY5

Skip the next instruction if TMG ERR flag = 1

LOAD ENABLE REGISTER (ADLE) – 6XY6

Load the Enable register from AC bits 2–7 and clear the AC

READ REGISTERS (ADRS) – 6XY7

Transfer Status, Enable, and MUX registers to AC bits 0–11

3.4 PROGRAMMING EXAMPLES

Take 1000_8 Samples

```
Start,      CLA, CLL          /Clear the accumulator and link
            TAD Number        /Get the number of samples
            DCA Counter       /Store in counter
            TAD ADDRESS       /Get the start of the table
            DCA POINTER       /Store it in the auto increment register
            TAD CHN           /Get a channel
            ADLM              /Store it in the multiplexer register
Again,      ADST              /Start the A/D conversion
            ADSK              /Skip on DONE flag
            JMP.-1            /Did not skip – try again
            ADRB              /Skipped Read the A/D Buffer
            DCA I POINTER     /Store it away in a table
            ISZ COUNTER       /Have the required number of samples been taken?
            JMP AGAIN         /No, take another sample
            HLT               /Yes, you're done

CHN, 0                        /Channel to be sampled
POINTER, 10                   /Auto increment register address
ADDRESS, N–1                  /Beginning of a data table at N
NUMBER, 7000                  /Minus the number of samples
COUNTER, 0
```

Program used to Check ERROR Flag

```
        .
        .
        .
ADSE            /Skip the next instruction on ERROR
SKP             /Unconditional skip
JMS ERROR       /Go to ERROR routine
        .
        .
        .
```

GLOSSARY OF A/D TERMS

Absolute Accuracy

The analog error, expressed as a percentage of full scale, referenced to the National Bureau of Standards volt.

Acquisition Time

The time duration between the giving of the sample command and the point when the output remains within a specified error band around the input value.

Aperture Delay Time

The time elapsed between the hold command and the point at which the sampling switch is completely open.

Aperture Jitter

The variation in the aperture for a particular sample-and-hold.

Crosstalk

The amount of signal coupled to the output as a percentage of input signal applied to all off channels.

Differential Inputs

Two external signals applied to the input circuitry of an A/D system whereby the first is subtracted from the second. The difference is applied to the A/D system. This is generally used with twisted pair wiring to reduce noise pickup.

Example

$$V_O = (V+) - (V-)$$

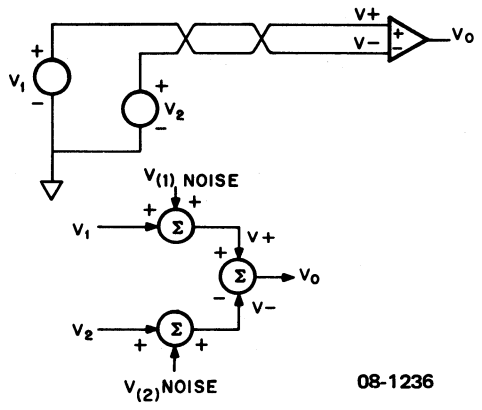
$$= [V_1 + V(_1) \text{ noise}] - [V_2 + V(_2) \text{ noise}]$$

$$= [V_1 - V_2] + [V(_1) \text{ noise} - V(_2) \text{ noise}]$$

For twisted pair wiring:

$$V(_1) \text{ noise} \doteq V(_2) \text{ noise}$$

$$\therefore V_O \doteq V_1 - V_2$$



Differential Linearity

The maximum deviation of an actual stated width from its theoretical value for any code over the full range of the converter. A differential linearity of ±1/2 LSB means that the width of each code over the range of the converter is 1 LSB ±1/2 LSB. Missing codes in an A/D converter occur when the output code skips a digit. This happens when the differential linearity is worse than ±1 LSB. Many A/D systems have a monotonicity test which looks for continuously increasing outputs for continuously increasing inputs (ramp function) over the full range of the converter. If all other factors are ignored, to pass this test, the A/D system must have a differential linearity of better than ±1 LSB. However, for these tests to be valid, the A/D system must be noiseless. Noise spikes could give false differential linearity readings.

Drift

Drift is a function of the temperature coefficients of the components. It is the major contributor to gain and offset error.

Gain Error

The error, expressed as a percentage, by which the actual full scale range differs from the theoretical full scale range. This error is adjustable to zero.

Input Bias Current

The amount of current that flows out of an off channel into the source.

Input Impedance (dc)

The resistance seen at the input to an A/D system.

Linearity

Linearity is defined as the maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity may be expressed as a percentage of full scale or as a fraction of an LSB size. The linearity of a good converter is ±1/2 LSB.

Multiplexer

The multiplexer is a set of switches that permits analog data from different sources (channels) to be supplied to the sample-and-hold (or A/D converter) individually.

Multiplexer Settling Time

The maximum time required to reach a specified error band around the input value when switching channels.

Offset Error

The error by which the transfer function fails to pass through the origin. This is usually adjustable to zero, or set automatically as in the AD8-A.

Quantization Error

Quantization error is defined as the basic uncertainty associated with digitizing an analog signal, due to the finite resolution of an A/D converter. An ideal converter has a maximum quantization error of ±1/2 LSB.

Relative Accuracy

This is defined as the input to output error as a fraction of full scale, with gain and offset errors adjusted to zero. Relative accuracy is dependent on linearity.

Resolution

The resolution of an A/D converter is defined as the smallest analog change that can be distinguished. Resolution is the analog value of the least significant bit.

$$\text{Resolution} = \frac{\text{Full scale}}{\text{Least significant bit}}$$

For example, if a system requires a weight measurement range of 2540 lbs., measured to the nearest 3 lbs,

$$\text{Resolution} = \frac{2540}{3} = 847 \text{ code combinations}$$

The closest standard A/D converter resolution available is 10-bits binary. A binary resolution of 10-bits is selected. The new resolution for this channel is recalculated for 10 bits.

$$1 \text{ LSB (least significant bit)} = \frac{\text{Full scale range}}{2^n} = \frac{2540}{1024} = 2.5 \text{ lbs.}$$

Sample-and-Hold

In order to ensure that input voltage does not change during a conversion, a sample-and-hold is required. If the change during a conversion cycle is less than 1/2 LSB, then a sample-and-hold circuit is not required.

Example

Conversion Speed = 20 μs
Full Scale Input Range (FSR) = 10.24 V
Converter Word Size = 10 bits
LSB Value = .01 V/bit
1/2 LSB = .005 V

Maximum slew = .005 V/20
(Rate required for no sample-and-hold)

for $e_{in} = 1/2$ (FSR) sin ω t

then $de/dt = 1/2\ \omega$ (FSR) cos ω t

$\therefore |de/dt|$ max. $= 1/2\ \omega$ (FSR)

or 250 V/sec. $= \pi$ (BW) (FSR)

BW = 250 V/sec./π (10.24 V) $\doteq$ 7.77 Hz

Source Impedance

The Thevenin equivalent resistance which is seen at the source of the analog inputs. It is important to note that the input impedance should be chosen so as not to degrade the accuracy of the A/D system.

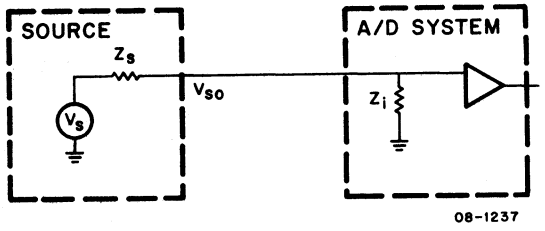
Example

Z_s = source impedance (Thevenin)

Z_i = input impedance

V_s = source voltage (Thevenin)

V_{so} = actual source output voltage



$$V_{so} = V_s \frac{Z_i}{Z_i + Z_s} \text{ (voltage division)}$$

if Z_i is shorted then $V_{so} = 0$ V

if Z_i is infinite then $V_{so} = V_s$ (source)

To measure to 1/2 LSB in a 10-bit A/D system, we require to resolve 1 in 2048. We do not want to degrade V_{so} by more than 1/2 LSB, therefore,

$$V_{so} = \frac{2047}{2048} V_o = \frac{2^{n+1}-1}{2^{n+1}} V$$

(n is the number of bits in the A/D system)

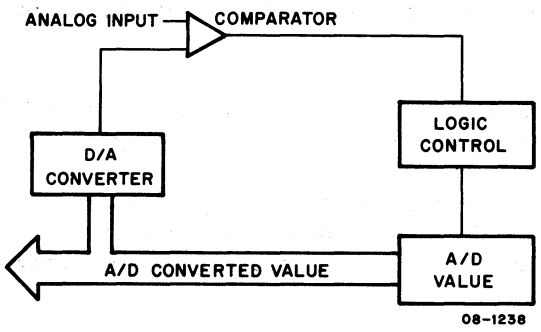
$$\frac{Z_i}{Z_i + Z_s} = \frac{2047}{2048}$$

$$Z_i = 2047\, Z_s$$

If the output source impedance is 1 KΩ, then input impedance must be greater than 2 MΩ.

Successive Approximation

A method that is used to transform the analog signal to a digital number.

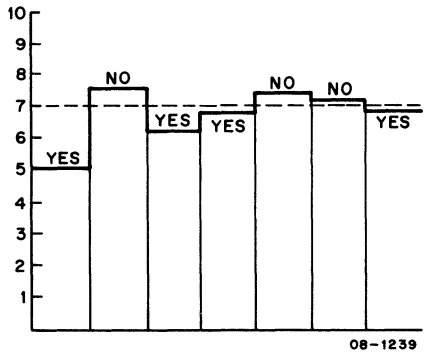


An analog signal is compared to a computer generated signal. The computer always supplies a half range signal initially. For example, the full scale input to an A/D converter system is 10 V and the input to the system is 7 V.

Try*	New Computer Voltage	Is the Input Greater Than New Voltage	A/D Buffer Bits	Decision	A/D Register Value
5 V	5 V	Yes	6	Add +5 = +5	1000000
2.5 V	5 + 2.5 V	No	5	Do nothing	1000000
1.25 V	5 + 1.25 V	Yes	4	Add 1.25 = 6.25	1010000
.625 V	6.25 + .625 V	Yes	3	Add .625 = 6.875	1011000
.3125 V	6.875 + .3125 V	No	2	Do nothing	1011000
.15625 V	6.875 + .1562 V	No	1	Do nothing	1011000
.078125 V	6.875 + .078125 V	Yes	0	Add .078175	1011001

*This is a 7-bit A/D

1011001 ≈ 7 V in 10 V full scale range.



Throughput Speed

The Nyquist sampling theorem states that a minimum of two samples per cycle are required to completely recover continuous signals in a noiseless environment. In typical instrumentation systems noise does exist and from 5–10 samples per cycle are required.

For single-channel applications with dc and very low frequency signals, sample rate is usually a sub-multiple of the powerline frequency to provide essentially infinite rejection of these frequencies.

The minimum sampling speed required is the number of samples per cycle multiplied by the highest frequency component of the data. For time multiplexed systems, the speed requirement of the A/D converter is dependent on system throughput speed. System conversion speed is determined from data bandwidth, the number of channels, and the sampling factor by:

System throughput = (N) (n) (B.W.) samples/second
n = number of channels

where

N = number of samples/cycle (sampling factor)
B.W. = largest bandwidth of any channel

Example

Channel 1 bandwidth 100 Hz
Channel 2 bandwidth 200 Hz
Channel 3 bandwidth 250 Hz

throughput = 10 X 3 (250) = 7500 sample/second

N = 10
n = 3
BW = 250 Hz

The A/D throughput is comprised of the following:

Multiplexer settling time
Sample & Hold settling time
A/D conversion speed
A/D recovery time
Computer acquisition time

Printed in U.S.A.