EK-DMZ32-UG-001

DMZ32
User Guide

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PREFACE

The *DMZ32 User Guide* is a standalone document that describes typical 24-line asynchronous multiplexer use, features and capabilities, installation, programming, service, and troubleshooting procedures, based on a module replacement philosophy. T-carrier techniques are covered in Appendix A, while floating device addresses and vectors are covered in Appendix B.

Additional information about the DMZ32 24-line asynchronous multiplexer can be found in the following:

- *DMZ32 Technical Manual* (EK-DMZ32-TM),
- *Communications Options Minireference Manual* (EK-CMIVI-RM), and
- *DMZ32 Print Set* (MP00997-01).

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This chapter contains a brief introduction to the DMZ32. The term DMZ32, as used throughout this manual, denotes the 24-line asynchronous multiplexer.

1.2 DMZ32 GENERAL DESCRIPTION

The DMZ32 is a 24-line asynchronous multiplexer consisting of a single hex height module and a distribution panel. The DMZ32 has a maximum line speed of 19.2K bits/s.

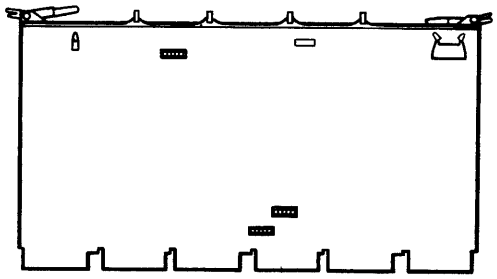
Features of the DMZ32 include:

- Split baud rate and modem control on all lines,
- Transmit and receive character silos,
- DMA capability on transmit,
- Programmable silo alarm time-out period for the receive silo, and
- Improved connectivity.

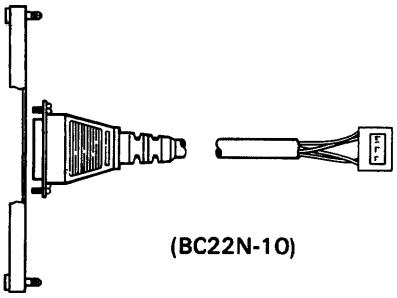
These features result in increased system throughput. An added feature is the improved connectivity of the DMZ32. The connection between the VAX UNIBUS interface module (M8398) and the remote distribution panel (H3014) is accomplished by two cables (BC22N-10 and BC18L-15).

The remote distribution panel (H3014) of the DMZ32 can be mounted up to 1524 m (5000 ft) away from the UNIBUS interface module (M8398) with additional cable. (See Appendix B.) The H3014 is an active distribution panel that requires external power. Located on the distribution panel are 24 RS-232-C male DB25 connectors which allow connection to 24 different lines.

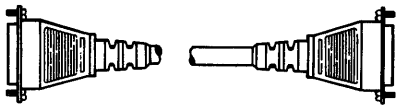
The DMZ32 plugs into a Small Peripheral Controller (SPC) slot and runs under the VMS operating system (Version 4.0 or later). (Refer to Figure 1-1 for the component parts of the DMZ32 and Figure 1-2 for the DMZ32 functional block diagram.)



(M8398)



(BC22N-10)



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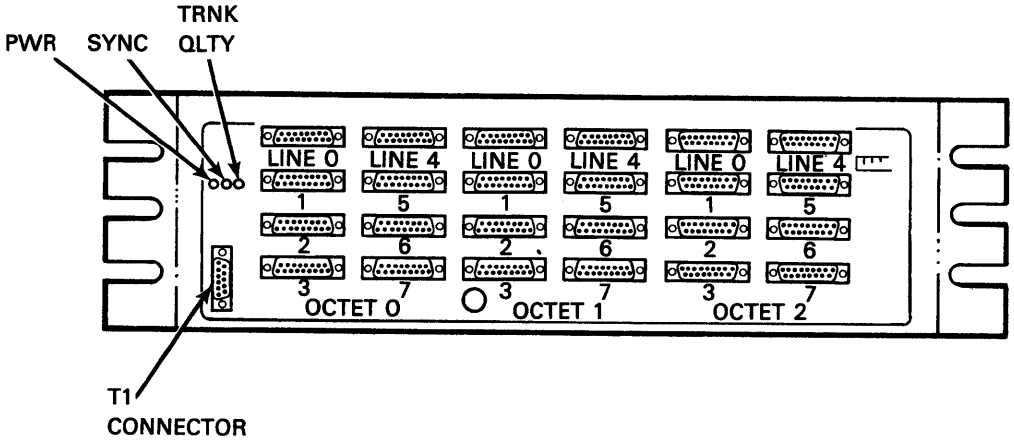
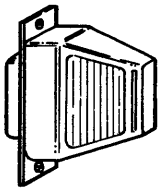


(H3014)



H3027

H3028

MKV84-0470

Figure 1-1 DMZ32 Component Parts

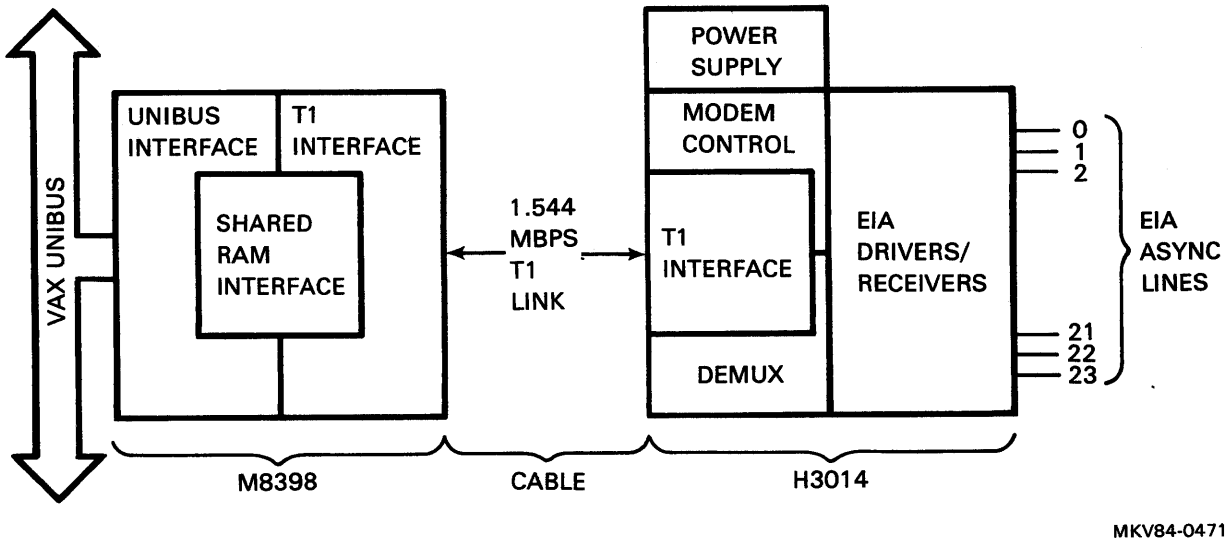


Figure 1-2 DMZ32 Functional Block Diagram

1.2.1 UNIBUS Interface Module (M8398)

The first interface component of the DMZ32 asynchronous multiplexer is the UNIBUS Interface Module (UIM). The UIM is mounted on a single hex height board and is divided into the following logical sections:

- UNIBUS Interface (UBI),
- Shared RAM Interface (SR), and
- T1 Interface Unit (TIU).

1.2.1.1 UNIBUS Interface – The UNIBUS Interface (UBI) is the section of logic that handles all UNIBUS interfacing. This section passes data between the VAX UNIBUS and the shared Random Access Memory (RAM) interface.

1.2.1.2 Shared RAM Interface – The Shared RAM interface (SR) is an area of shared access, a means of passing data from one asynchronous process to another. The Shared RAM interface allows access to the T1 interface unit from the UNIBUS Interface and to the UNIBUS interface from the T1 interface.

1.2.1.3 T1 Interface Unit – The T1 Interface Unit (TIU) is the time division multiplexer and the T1 carrier interface. It controls all data going on and off the high speed (1.544M bits/s) T1 trunk.

1.2.2 Remote Distribution Panel (H3014)

The second component of the DMZ32 asynchronous multiplexer is the remote distribution panel (H3014). The H3014 is an active distribution panel that is powered from its own independent power supply. The H3014 is responsible for coordinating all data transfers between any of 24 asynchronous lines and the T1 trunk. The configuration of the H3014 depends on the option purchased; therefore, it may also be responsible for passing modem signals if the appropriate option is installed. The distribution panel decodes the incoming T1 formatted serial data. In the reverse direction, it places outgoing asynchronous terminal data and modem control signals into the T1 serial bit stream, using bipolar encoding techniques.

The H3014 consists of the following major components:

- Power supply,
- Expansion module , and
- Processor module.

1.2.2.1 Power Supply – The power supply provides the operating voltages necessary for the electronic circuitry in the distribution panel. The voltages provided by the power supply are:

- +5 Vdc @ 10 A,
- +12 Vdc @ 2.5 A, and
- −12 Vdc @ 2.5 A.

1.2.2.2 Expansion Module – The expansion module provides drivers/receivers for six of the modem control signals. The modem control signals supported by the expansion module are:

- Data Signaling Rate Select,
- Request To Send,
- Data Set Ready,
- Clear To Send,
- RS-449 Local Loopback, and
- RS-449 Test Mode.

(Refer to Table 1-1 for pin assignment and signal descriptions.)

Table 1-1 V.24/RS-232 Pin Assignments

Description	Pin	CCITT	EIA	Origin
Protective Ground	1	101	AA	-
Transmitted Data	2	103	BA	DTE
Received Data	3	104	BB	DCE
Request To Send (RTS)	4	105	CA	DTE
Clear to Send(CTS)	5	106	CB	DCE
Data Set Ready (DSR)	6	107	CC	DCE
Signal Ground	7	102	AB	-
Carrier Detect (CD)	8	109	CF	DCE
RS-449 Local Loopback (LL)	18	-	-	DTE
Data Terminal Ready (DTR)	20	108.2	CD	DTE
Ring Indicator (RI)	22	125	CE	DCE
Data Signaling Rate	23	111	CH	DTE
Selector (DSRS)	-	-	-	-
RS-449 Test Mode (TM)	25	-	-	DCE

1.2.2.3 Processor Module - The processor module contains the microprocessor that controls the H3014 operation, status indicators (Pwr, Sync, and Trnk Qlty), drivers/receivers for data signals, and modem control signals. The modem control drivers/receivers contained on the processor module are:

- Data Terminal Ready,
- Carrier Detect, and
- Ring Indicator.

1.3 DMZ32 SYSTEM OPERATION

The DMZ32 can transmit data to and receive data from 24 different lines. During the transmission of data, the transmit line is enabled by setting the line enable bit in the specific line control (LINE CTRL) register. A line must be enabled before transmission of data can take place. A disabled line is held in the ON (or marking) state, except in special maintenance situations. Transmission of data is handled using two different techniques, Program Mode and DMA Mode. Although both of these techniques use silos, the program mode uses standard I/O and the DMA mode uses NPR/DMA to load the transmit silos.

For reception of data, the receiver is enabled by setting the line enable bit in the appropriate LINE CTRL register. A line must be enabled in order to receive data. Each octet (8-line group) shares a 128-character receive silo (total of three receive silos). There is no NPR/DMA mode in the receiving mode of the DMZ32.

1.4 T1 OVERVIEW

The DMZ32 uses a T1 transmission technique by way of two twisted pair cables to provide optimal channel utilization for transfer of data between the UIM and the distribution panel.

T1 or "T-Carrier" is a telecommunication industry term taken from the Bell System's carrier system. This transmission techique is based on Pulse Coded Modulation (PCM) and Time Division Multiplexing (TDM) techniques. Using these techniques, 24 independent data channels are encoded into 8 bits and are subsequently placed into a 1.544M bits/s serial bit stream. This bit stream is then converted into a specific format using a bipolar or Alternate Mark Inversion (AMI) technique, and is transmitted down the T1 link.

At the receive end of the T1 link, the clock is reconstructed from this serial bit stream and is used to synchronize the demultiplexing and distribution of the data to the appropriate line.

1.5 DMZ32 SPECIFICATIONS

The specifications for the two major components of the DMZ32 (M8398 module and H3014 distribution panel) are divided into the following:

- Physical specifications,
- Electrical specifications,
- Environmental specifications, and
- UNIBUS conductor specifications (M8398 only).

1.5.1 DMZ32 Module (M8398)

Physical Specifications

Single hex height module

Electrical Specifications

DC Voltage	+5 V @ 9.0 A +15 V @ 0.1 A
Data Baud Rates (Half or Full Duplex)	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 9600, and 19200

Environmental Specifications

Temperatures	
Operating	10 to 40°C (50 to 104°F)
Non-operating	−40 to 66°C (−40 to 151°F)
Relative Humidity	
Operating	10 to 90% with a maximum wet bulb of 28°C (82°F) Maximum dewpoint of 2°C (36°F), noncondensing
Non-operating	5 to 95% noncondensing

UNIBUS Specifications

UNIBUS Loads	6.2 ac unit loads 1.5 dc unit loads
Addresses (Octal)	760440 – 763740 (typical)
Vector (Octal)	300 (typical)
Interrupt Levels	BR 5

1.5.2 Distribution Panel (H3014)

Physical Specifications

Height	13.3 cm (5.25 in)
Width	48.2 cm (19 in)
Depth	43.18 cm (17 in)
Mounting	Standard 48.2 cm (19 in)
Weight	8.1 kg (18 lbs) maximum

Electrical Specifications

AC Line Voltage	90-130 Vac or 180-255 Vac
Line Frequency	47-63 Hz
Input Current	1.5 A @ 120 Vac .8 A @ 220-240 Vac

Grounding

Frame Ground	The chassis frame is electrically bonded to earth ground by means of the primary circuit connector
Logic Ground	This is signal reference ground
EIA Ground	This is a noncurrent carrying ground used as a reference for all Electronic Industries Association (EIA) receiver inputs

Environmental Specifications

Temperatures

Class B (Non air-conditioned)	10 to 40°C (50 to 104°F)

Relative Humidity

Class B (Non air-conditioned)	10 to 90% with a maximum wet bulb of 28°C (82°F) Maximum dewpoint of 2°C (36°F), noncondensing
Heat Dissipation	454 Btu per hour

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter contains procedures for unpacking, installing, and checking the DMZ32. A checklist, which can be used to verify the installation process, is included.

2.2 UNPACKING AND INSPECTION

The DMZ32 is packaged according to commercial packing practices. When unpacking a DMZ32 option, carefully remove all packing materials making sure not to damage the contents, and check the contents against the shipping list. Table 2-1 lists the contents of each DMZ32 option. Inspect all items carefully. Pay close attention to the module to check for cracks, loose components, and breaks in the etched paths.

Table 2-1 DMZ32 Option Packing List

Option	Part Number	Contents
DMZ32-M	M8398	• One UNIBUS hex module
	BC22N-10	• One internal cable and 2 × 4 bulkhead insert
	BC18L-15	• One external cable
	H3028	• One local T1 loopback
	H3027	• One remote T1 loopback
	EK-DMZ32-UG	• One user guide
CK-DMZ32-AY	H3014-CA	• Remote distribution panel (120 V/240 V) with modem control • Shipping bracket • 120 V power cord • 240 V power cord
CK-DMZ32-DY	H3014-AA	• Remote distribution panel (120 V/240 V) no modem control • Shipping bracket • Picture frame • 120 V power cord • 240 V power cord
DMZ32-AP		• DMZ32-M (system integrated) • CK-DMZ32-AY
DMZ32-DP		• DMZ32-M (system integrated) • CK-DMZ32-DY
DMZ32-N		• Remote distribution panel (H3014) expansion module for modem control

2.3 DEVICE ADDRESS ASSIGNMENTS

The DMZ32's device addresses are selected from the floating device address space of the UNIBUS input/output (I/O) page. (Refer to Appendix A.) Switchpack E-53 on the DMZ32 selects the first DMZ32 CSR address.

When there are no floating devices before the DMZ32, the first floating address space is 760440 (FFE120 hex). The second and third floating address spaces for the DMZ32 are 760500 (FFE140 hex) and 760540 (FFE160 hex), respectively. When operating under VMS (Version 4.0 or later), the actual address(es) can be determined by using the SYSGEN utility. Refer to the *VAX/VMS Guide to Writing a Device Driver* (AA-H499B-TE) for the procedure to determine CSR address assignments.

2.4 DEVICE VECTOR ASSIGNMENT

The DMZ32 interrupt vectors are controlled by the VMS operating system. During autoconfiguration, the operating system loads the value of the base vector into the DMZ32. The other DMZ32 vectors are calculated from the base vector. (Refer to Appendix A for floating vector addresses.)

2.5 INSTALLATION PROCEDURE

The installation of the DMZ32 is broken down into the following procedures:

- UNIBUS interface module (M8398) installation,
- Remote distribution panel (H3014) installation, and
- Cable installation.

The required installation tools are:

- VAX cabinet key (usually a 7/64 Allen wrench),
- Phillips screwdriver,
- 7/16 hex driver, and
- Flatblade screwdriver.

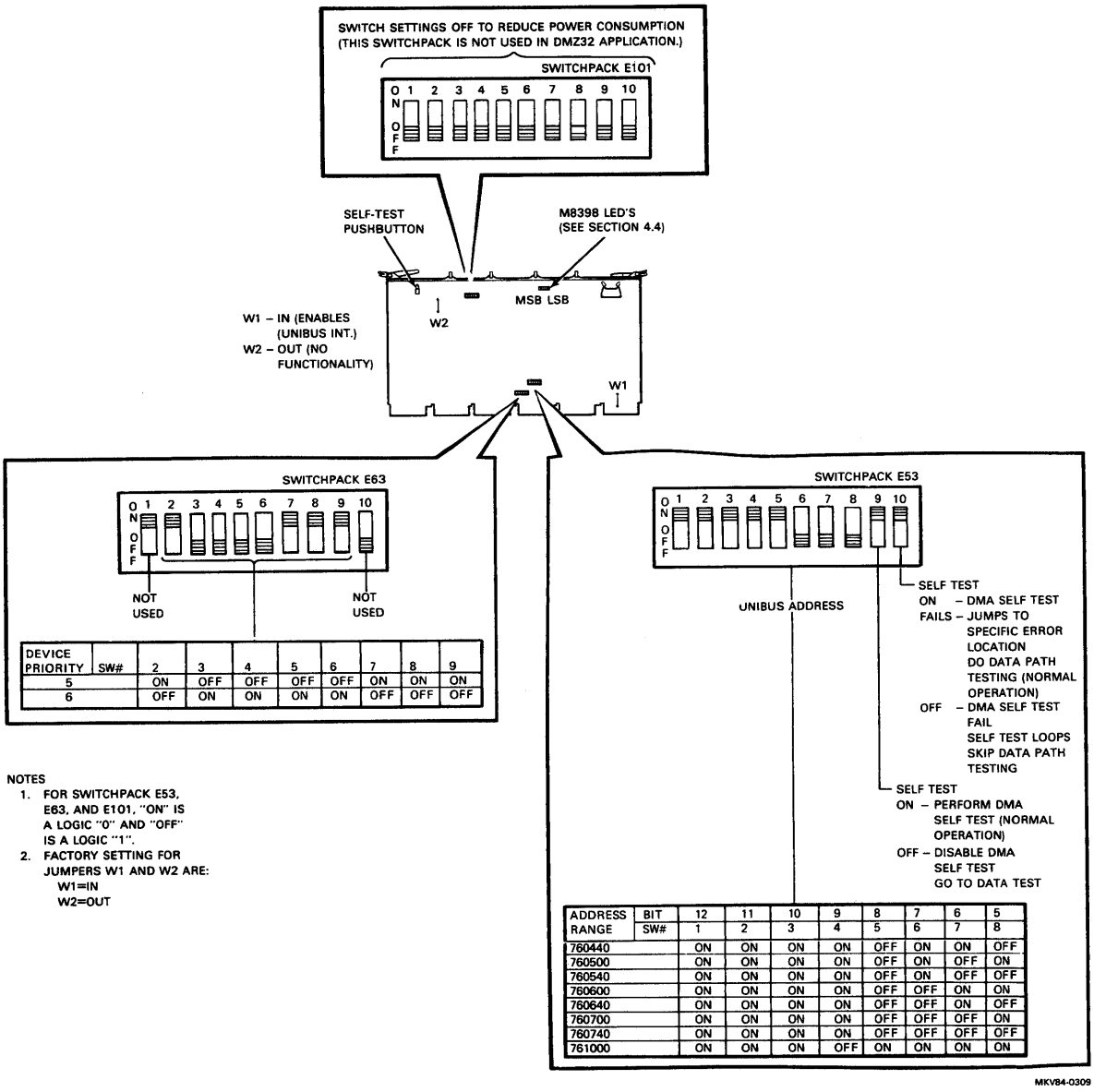
2.5.1 M8398 Module Installation

To install the M8398, perform the following steps in the sequence given, ensuring that no steps are skipped or overlooked. Figure 2-1 shows the location of the switchpacks.

1. Set switches 2 through 9 on switchpack E-63 to the correct priority level.
2. Set switches 1 through 8 on switchpack E-53 to the proper UNIBUS address.
3. Set switch 9 on switchpack E-53 to the ON position.
4. Set switch 10 on switchpack E-53 to the ON positon. (Refer to Figure 2-1 for switch settings.)
5. Power down the system in which the M8398 is being installed.

WARNING

Before performing this procedure, the system on which the DMZ32 is to be installed must be completely powered down and the power cord disconnected from the power source. Personal injury may result if this procedure is ignored.



DEVICE PRIORITY	SW#	2	3	4	5	6	7	8	9
5		ON	OFF	OFF	OFF	OFF	ON	ON	ON
6		OFF	ON	ON	ON	ON	OFF	OFF	OFF

ADDRESS RANGE	BIT / SW#	12 / 1	11 / 2	10 / 3	9 / 4	8 / 5	7 / 6	6 / 7	5 / 8
760440		ON	ON	ON	ON	OFF	ON	ON	OFF
760500		ON	ON	ON	ON	OFF	ON	OFF	ON
760540		ON	ON	ON	ON	OFF	ON	OFF	OFF
760600		ON	ON	ON	ON	OFF	OFF	ON	ON
760640		ON	ON	ON	ON	OFF	OFF	ON	OFF
760700		ON	ON	ON	ON	OFF	OFF	OFF	ON
760740		ON	ON	ON	ON	OFF	OFF	OFF	OFF
761000		ON	ON	ON	OFF	ON	ON	ON	ON

NOTES
1. FOR SWITCHPACK E53, E63, AND E101, "ON" IS A LOGIC "0" AND "OFF" IS A LOGIC "1".
2. FACTORY SETTING FOR JUMPERS W1 AND W2 ARE:
   W1=IN
   W2=OUT

Figure 2-1 DMZ32 UNIBUS Interface Module (M8398)

6. Remove the Non-Processor Grant (NPG) wire (CA1-CB1) from the Small Peripheral Controller (SPC) backplane slot where the M8398 module is to be installed.

7. Perform resistance checks on the backplane to ensure that no short circuits exist.

8. Install the M8398 module into the prepared SPC slot of the DD11-DK backplane.

9. Power up the system and verify that the +5.00 Vdc supplied to the M8398 measures +5.00 Vdc.

10. When the M8398 module installation is complete, proceed to the DMZ32 Installation Check-Off List (Section 2.7) for the remaining steps to be performed.

2.5.2 H3014 Distribution Panel Installation

H9642-FC/FD (UNIBUS Expansion Cabinet)

NOTE

Because of mounting limitations, the distribution panel can only be mounted in H9642-FC/FD model cabinets. Refer to Figure 2-2 for the rear view of a model H9642-FC/FD.

1. Remove the rear door assembly of the VAX cabinet using the 7/64 Allen wrench.

2. Remove the FCC shield gasket panel assembly (Figure 2-2) by removing the following:

   a. Two (2) 7/16 hex head screws are located on the top right side and top left side of the gasket panel assembly. These secure the FCC shield gasket panel to the vertical mounting rails of the cabinet.

   b. Nine (9) Phillips screws located under the gasket panel assembly. (These screws secure the FCC shield gasket panel to the FCC bulkhead frame).

NOTE

The FCC bulkhead frames must be removed from below the FCC shield gasket panel assembly down to the location where the H3014 is to be mounted. These bulkhead frames must be removed starting from the top frame to the bottom frame. (See Figure 2-2.)

3. Remove the nine (9) Phillips screws (Figure 2-2) that secure the FCC bulkhead frames.

4. Remove the six (6) mounting Phillips screws (Figure 2-2) that secure the FCC bulkhead frames to the vertical mounting rails of the cabinet.

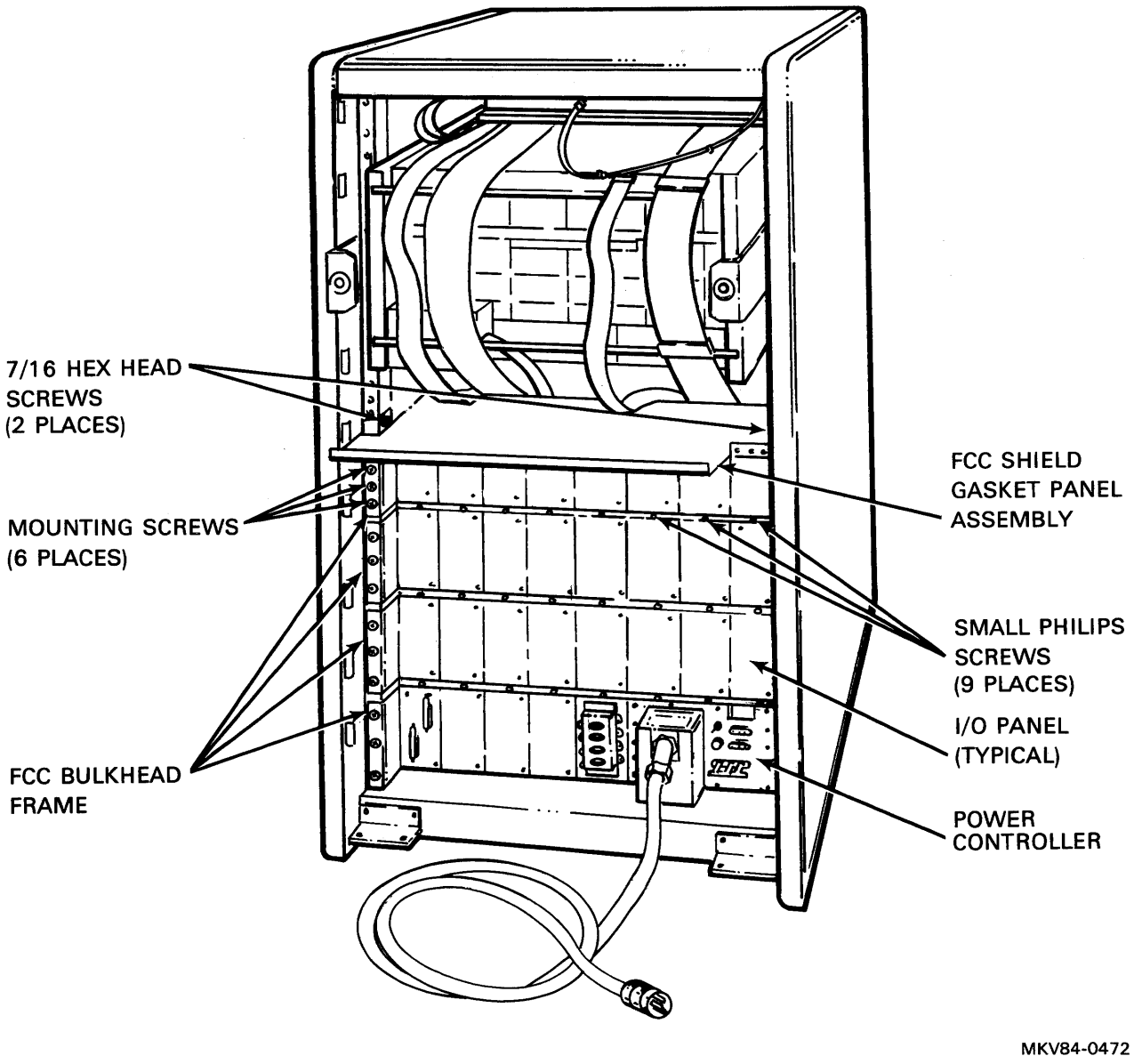


Figure 2-2 Typical H9642-FC/FD Shielded Cabinet Before H3014 Installation

5. Repeat Steps 3 and 4 until all required FCC bulkhead frames are removed, then proceed to Step 6.

NOTE
The distribution panel can be mounted to the cabinet only in the location shown in Figure 2-3.

6. Position the distribution panel and secure it to the cabinet vertical mounting rails using the six (6) Phillips mounting screws (Figure 2-3).

7. After the distribution panel is mounted, secure the bottom of the distribution panel to the FCC bulkhead frame beneath it using the nine (9) Phillips screws that were removed from the FCC bulkhead frame.

NOTE
If the H3014 is received in a cabinet, remove the shipping bracket (Figure 2-4).

8. Install the FCC shield gasket panel assembly by reversing the procedure in Step 2.

9. When the distribution panel installation is complete, proceed to the DMZ32 Installation Check-List (Section 2.7) for the remaining steps in the installation of the DMZ32.

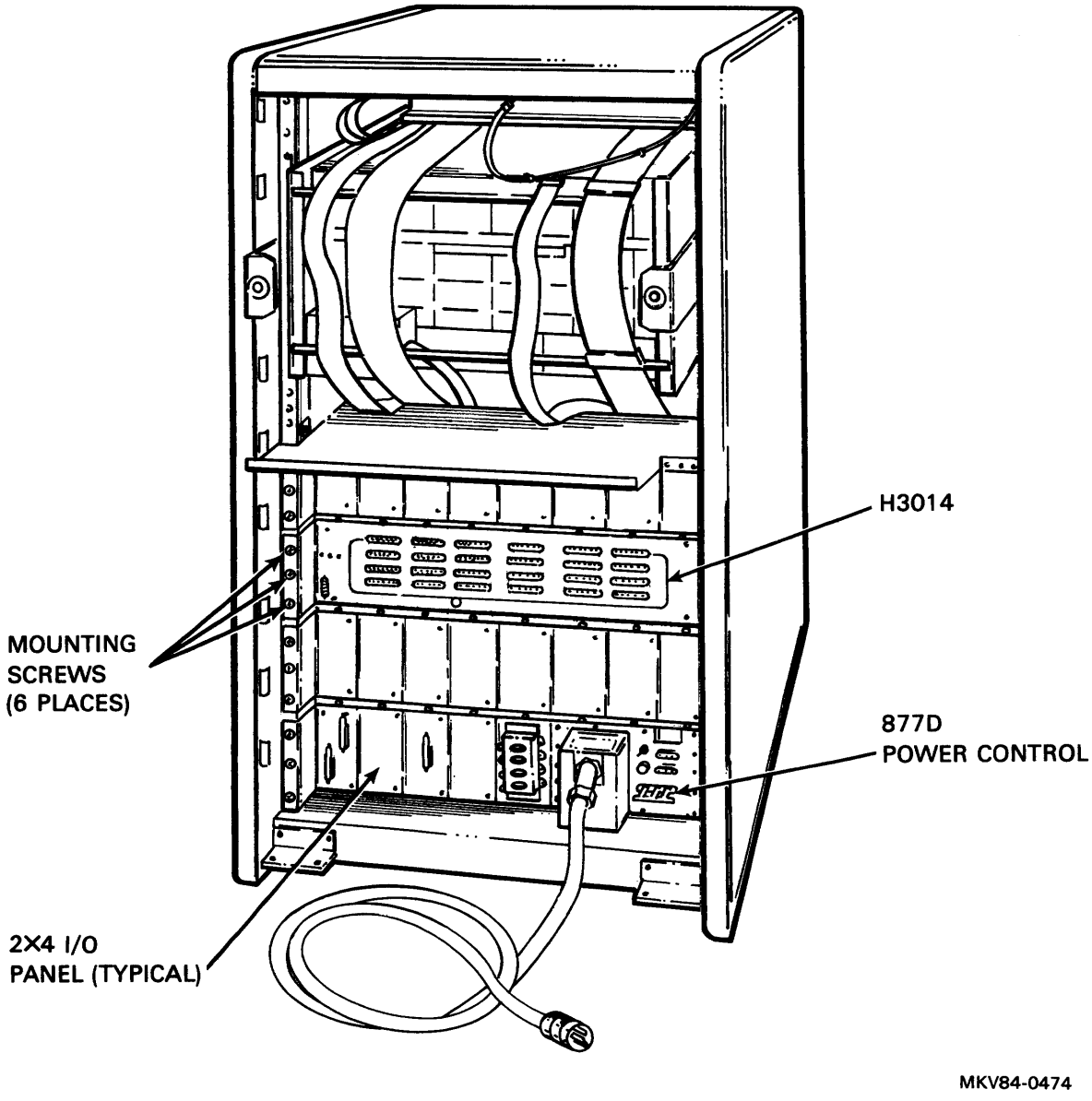


Figure 2-3 Typical H9642-FC/FD FCC Shielded Cabinet After H3014 Installation

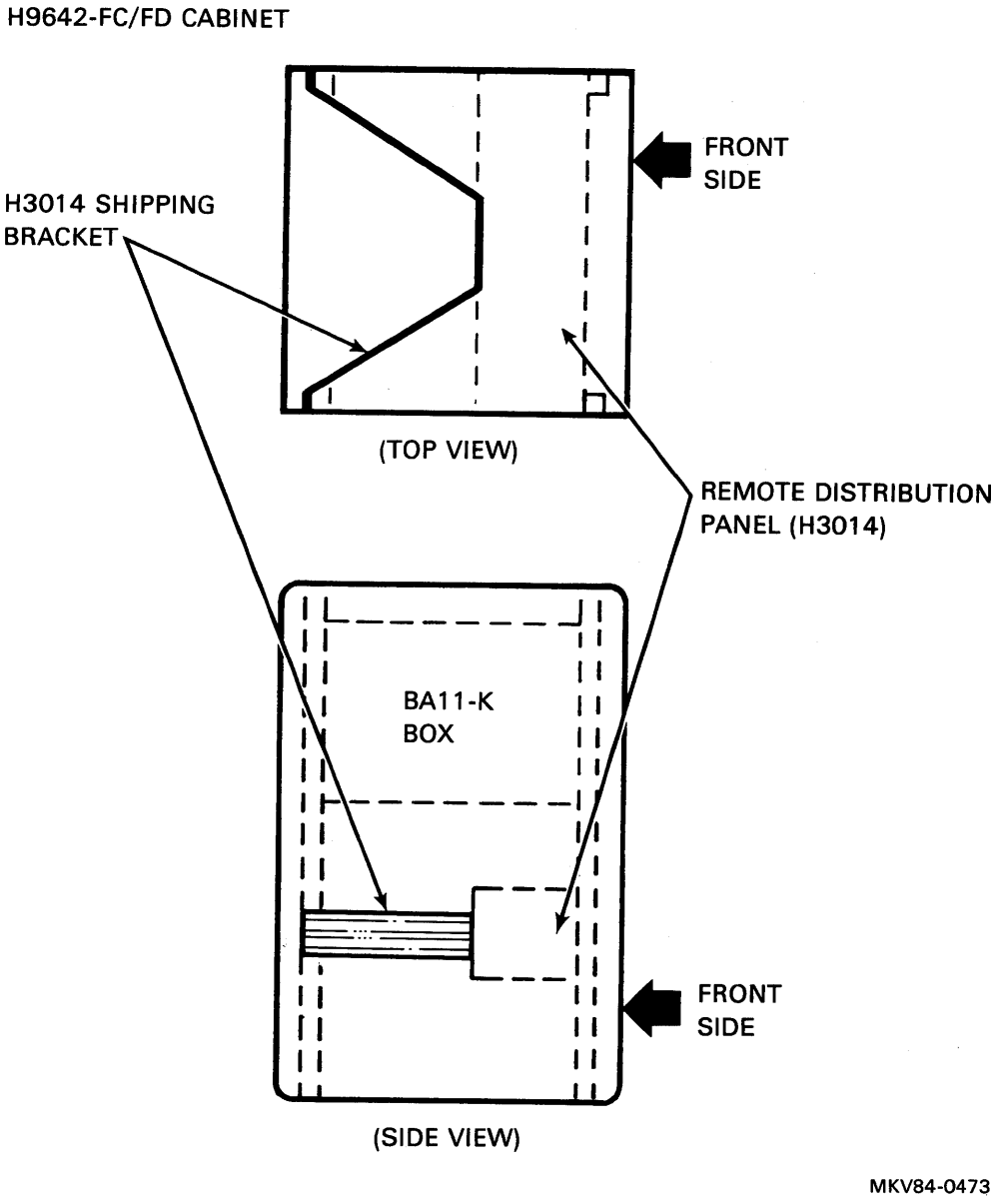


Figure 2-4 H3014 Shipping Bracket Position

H9652-MF (UNIBUS Expansion Cabinet)

NOTE

If the H9652-MF cabinet uses two (2) BA11 boxes, the distribution panel can not be mounted in the cabinet due to power limitations.

1. Remove the rear door assembly of the VAX cabinet using the 7/64 Allen wrench.

2. Remove the FCC shield gasket panel assembly (Figure 2-5) by removing the following parts.

   a. Two (2) 7/16 hex head screws are located on the top right side and top left side of the gasket panel assembly. These secure the FCC shield gasket panel to the vertical mounting rails of the cabinet.

   b. Nine (9) Phillips screws are located under the gasket panel assembly. These screws secure the FCC shield gasket panel to the FCC bulkhead frame.

3. Remove the nine (9) small Phillips screws (Figure 2-5) that secure the FCC bulkhead frame to the top of the cabinet frame.

4. Remove the six (6) mounting Phillips screws (Figure 2-5) that secure the top FCC bulkhead frame to the cabinet vertical mounting rails.

5. Repeat Steps 3 and 4 until all required FCC bulkhead frames are removed. When completed, proceed to Step 6.

NOTE

The distribution panel can be mounted only in the top two FCC bulkhead frame locations.

6. Position the distribution panel and secure it to the cabinet vertical mounting rails using the six (6) Phillips mounting screws (Figure 2-6).

7. After the distribution panel is mounted, secure the bottom of the distribution panel to the FCC bulkhead frame beneath it using the nine (9) Phillips screws that were removed in Step 3.

NOTE

If the H3014 is received in a cabinet, remove the shipping bracket (Figure 2-7).

8. If you are mounting two distribution panels, repeat Step 7. When completed, proceed to Step 9.

9. Install the FCC shield gasket panel assembly by reversing the procedure in Step 2.

10. When the distribution panel installation is complete, proceed to the DMZ32 Installation Check-Off List (Section 2.7) for the remaining steps in the installation of the DMZ32.

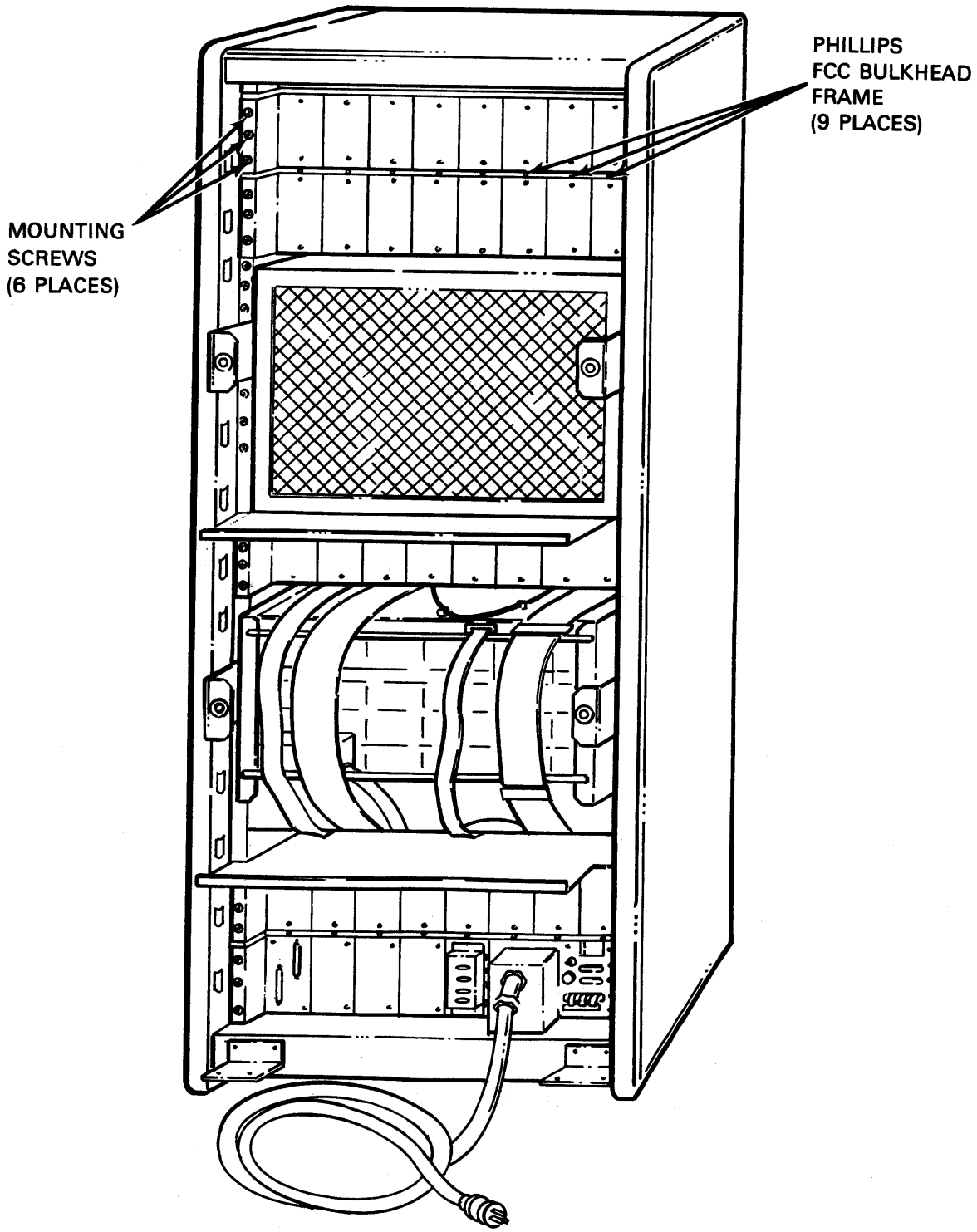


Figure 2-5 Typical H9652-MF (VAX-11/780) FCC Shielded Cabinet Before H3014 Installation

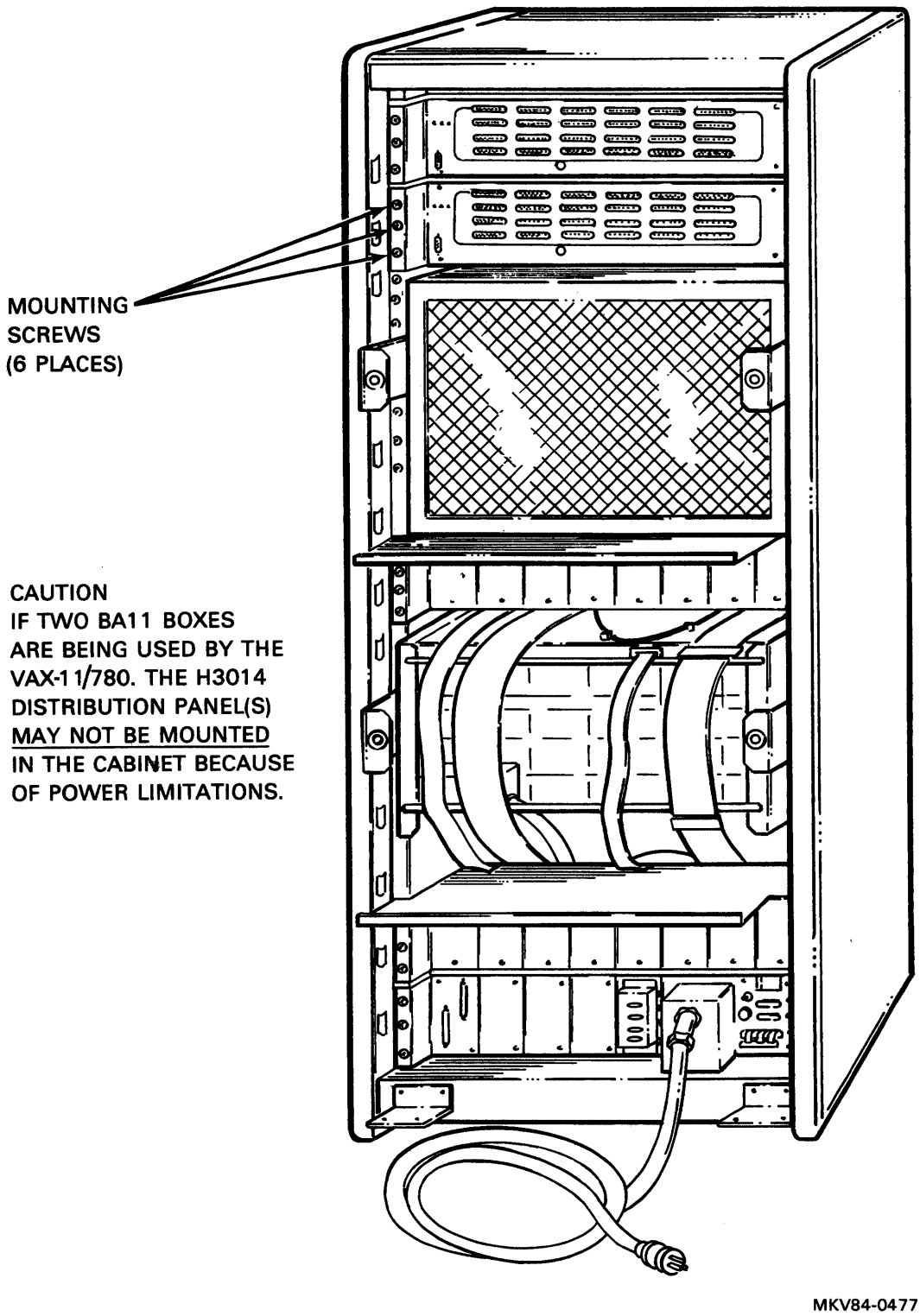


Figure 2-6 Typical H9652-MF (VAX-11/780) FCC Shielded Cabinet After H3014 Installation

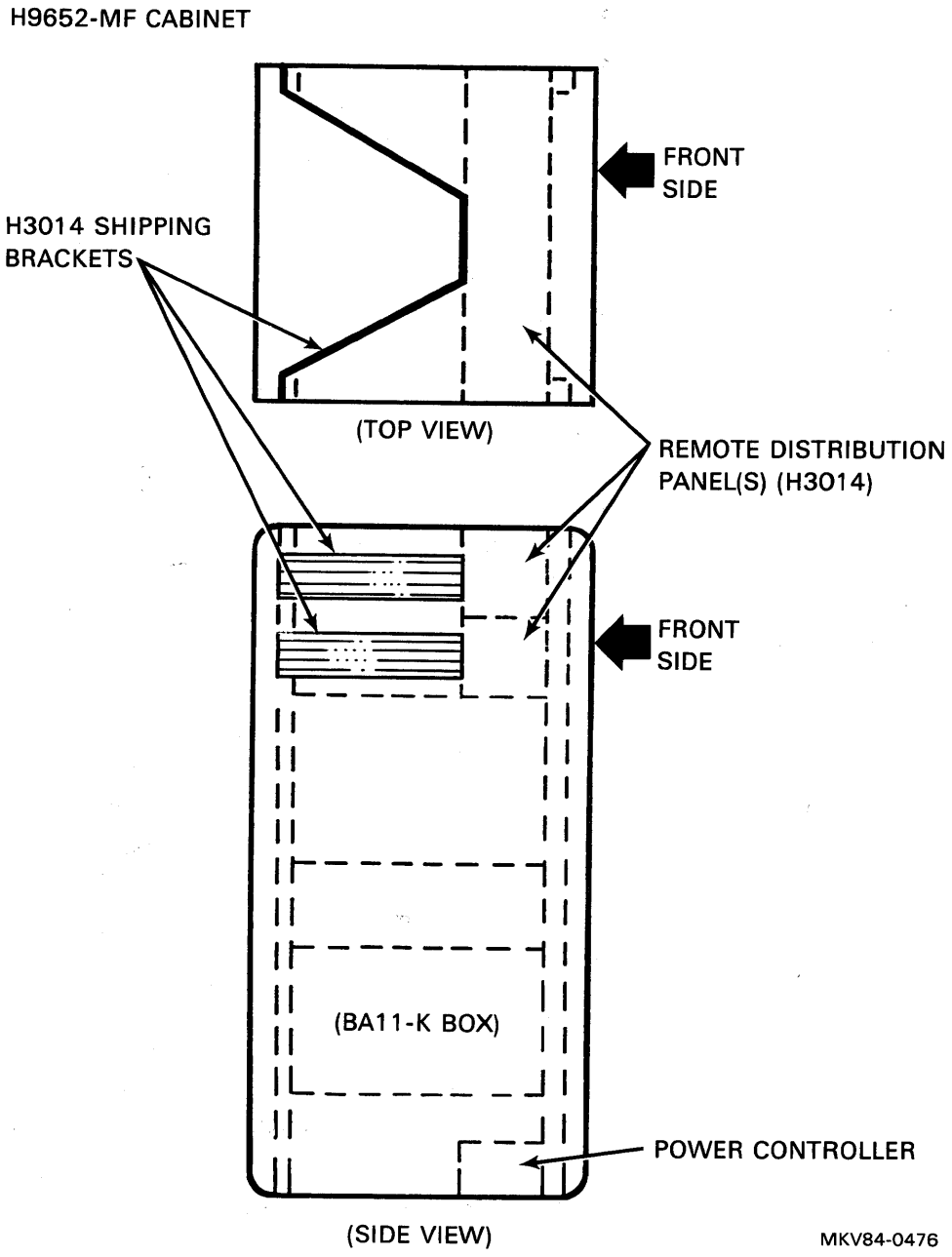


Figure 2-7 H3014 Shipping Bracket Position

Non-FCC Compliant Cabinet

1. Remove the rear door assembly of the VAX cabinet using the 7/64 Allen wrench.

2. Position the distribution panel where it is to be mounted, and secure it to the cabinet vertical mounting rails using the six (6) Phillips mounting screws.

3. If you are mounting two distribution panels, repeat Step 2 and proceed to Step 4.

4. When the distribution panel installation is complete, proceed to the DMZ32 Installation Check-Off List (Section 2.7) for the remaining steps in the installation of the DMZ32.

2.5.3 Cable Installation

NOTE

In an FCC cabinet, before the BC22N-10 is connected, it should be attached to the 2 × 4 I/O panel that is shipped with the cable. If installing in a non-FCC cabinet, discard the 2 × 4 I/O panel. (Refer to Figure 2-8.)

1. Remove a blank 2 × 4 I/O panel from the FCC bulkhead frame where the new 2 × 4 I/O panel (supplied with the cable) is to be located. Remove the two screws that secure the panel to the FCC bulkhead.

2. Feed the cable end of the BC22N-10 cable through the opening where the new I/O panel is to be secured.

3. Secure the new 2 × 4 I/O panel that is connected to the BC22N-10 cable to the FCC bulkhead frame where the blank panel was removed.

4. Connect the 10-pin Berg™ connector of the BC22N-10 cable to J1 of the M8398 module, located in the BA11-K box. Be sure that the "This Side Up" label is visible.

5. Connect one end of the BC18L-15 cable to the external side of the new I/O panel.

6. Connect the loose end of the BC18L-15 cable to the T1 connector on the distribution panel.

Berg is a trademark of Berg Electronics, Inc.

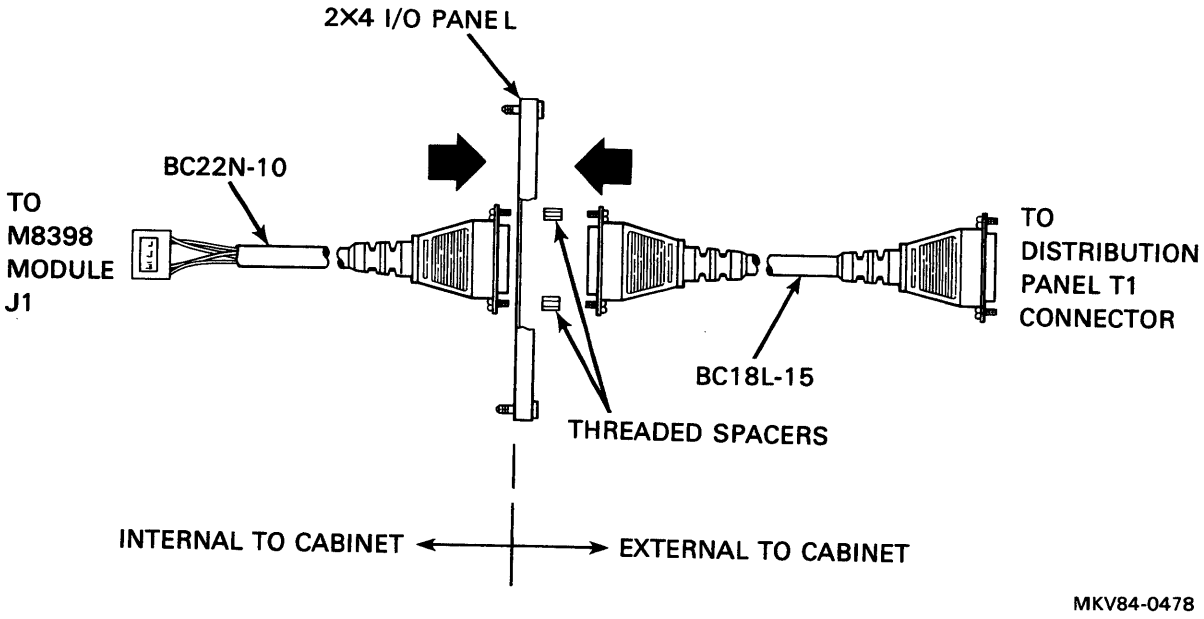


Figure 2-8 BC22N-10 to BC18L-15 Connection

2.6 DMZ32 INSTALLATION CHECKOUT

The following procedure is used to check out the installation of the DMZ32.

1. Remove the BC22N-10 cable from J1 of the M8398 module.

2. Install the local T1 loopback (H3028) connector into J1 of the M8398 module (Figure 2-9).

3. Power up the VAX system and execute diagnostic EVDAE for two passes with event flag 3 set. (Refer to Chapter 4 for details on how to execute EVDAE).

   If a failure occurs, check the following:

   - Seating of the M8398 module in the DD11-DK backplane,
   - ROM seating on the M8398 module, and
   - Seating of the H3028 loopback connector in J1.

   IF THE FAULT IS NOT CORRECTED, REFER TO CHAPTER 4 FOR CORRECTIVE ACTION.

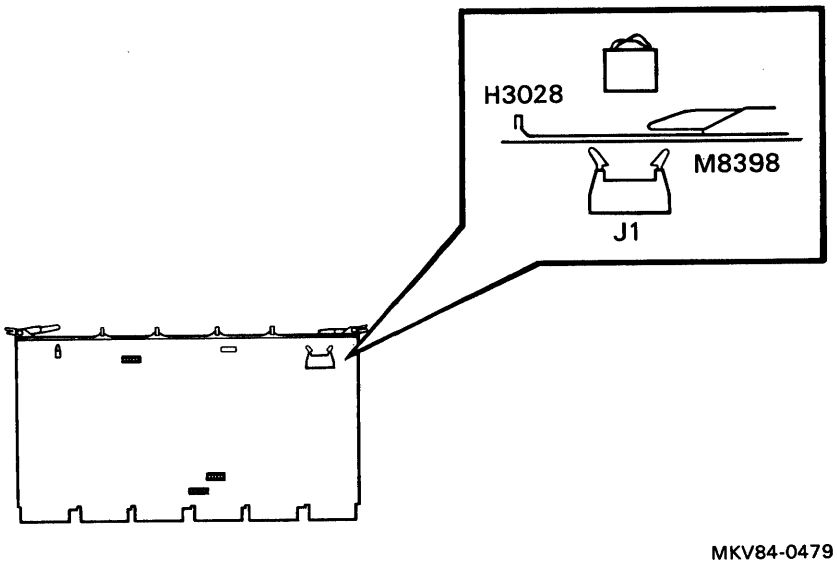


Figure 2-9 H3028 Loopback Connector Installed on M8398

4. After two successful passes, remove the H3028 loopback connector from the M8398 module and connect the BC22N-10 cable between M8398 module J1 and the 2 × 4 I/O panel insert. (Refer to Figure 2-10.)

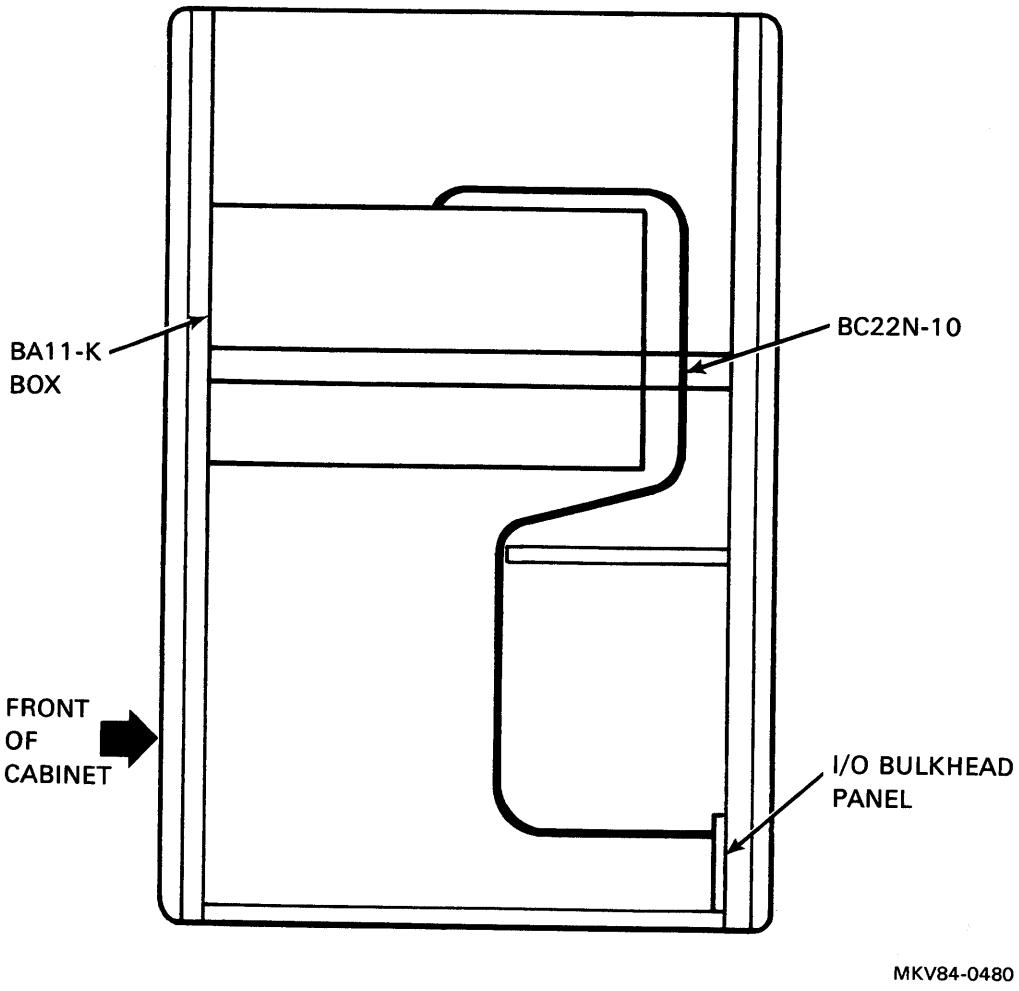


Figure 2-10 BC22N-10 Cable Between M8398 and I/O Bulkhead

5. Install the H3027 loopback connector (Figure 2-11) to the I/O panel side of the I/O panel connector (outside the cabinet), and execute diagnostic EVDAE, setting event flag 3 for two passes without errors.

   If a failure occurs, check the T1 cable for proper seating at both ends.

   IF THE FAULT IS NOT CORRECTED, REFER TO CHAPTER 4 FOR CORRECTIVE ACTION.

   If the H3014 is installed in a remote location, it is the customer's responsibility to supply and install the remote T1 cable. (Refer to Appendix B for T1 cable information.)

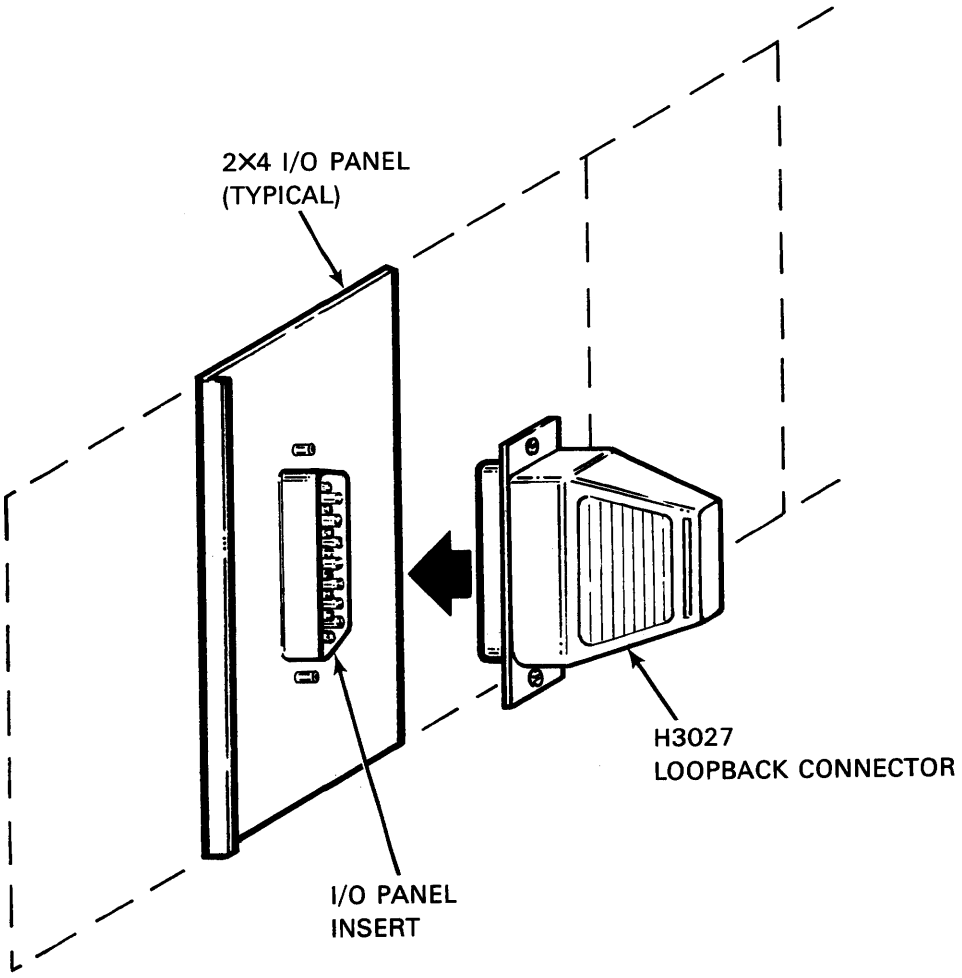


Figure 2-11 H3027 Loopback Connector Installed on I/O Bulkhead

6. Remove the H3027 loopback connector from the I/O bulkhead. Connect the remote T1 cable or BC18L-15 to the 2 × 4 I/O panel. (refer to Figure 2-12).

7. Install the H3027 loopback connector (Figure 2-12) to the opposite end of the remote T1 cable or BC18L-15, and execute EVDAE diagnostic for two passes with event flag 3 set.

NOTE
This loopback test can only be performed if the T1 cable length is 762 m (2500 ft) or less in length.

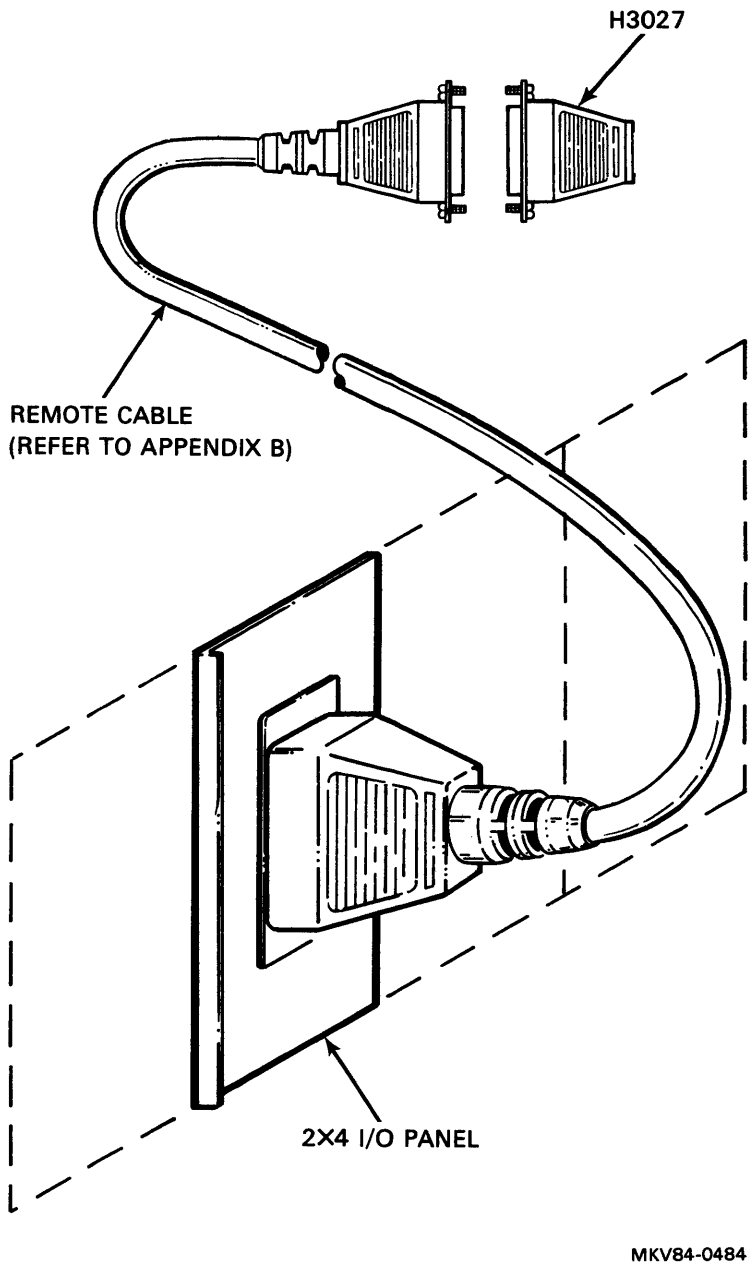


Figure 2-12 H3027 Loopback Connected to Remote End of T1 Cable

8. After two successful passes of EVDAE, stop the diagnostic and remove the H3027 loopback connector. Connect the remote T1 cable or BC18L-15 to the T1 input connector on the H3014 (Figure 2-13).

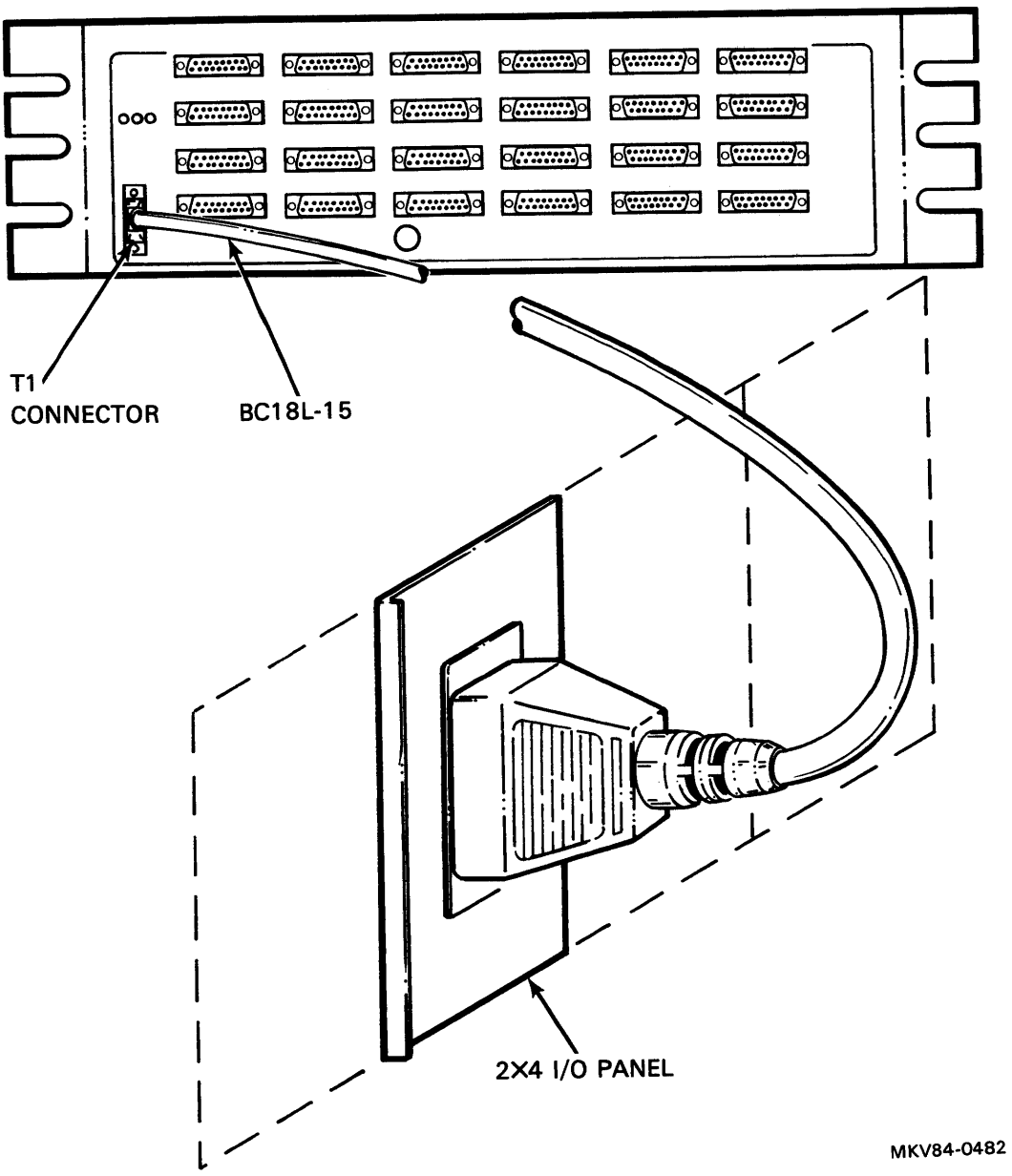


Figure 2-13 T1 Connector Between I/O and H3014

9. Install the six (6) 29-24929-00 staggered loopback connectors, which are supplied in the CD kit (Figure 2-14).

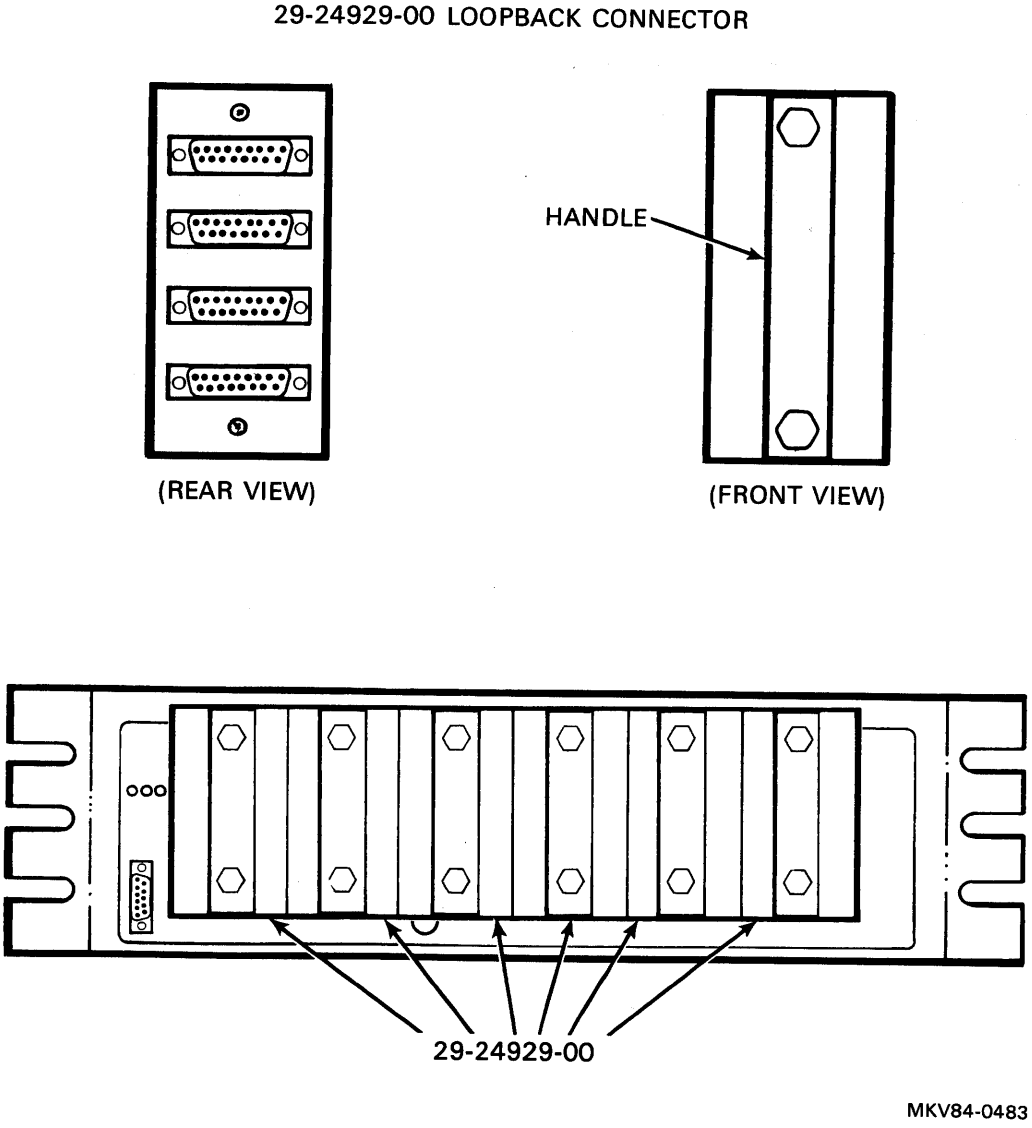


Figure 2-14 29-24929-00 Installed on H3014 Distribution Panel

10. Execute EVDAE diagnostic for two passes with event flag 6 set.

    If a failure occurs, check the following:

    - T1 cable for proper seating,
    - H3014 modules for proper seating, and
    - H3014 power supply voltages.

    IF THE FAULT IS NOT CORRECTED, REFER TO CHAPTER 4 FOR CORRECTIVE ACTION.

CAUTION

To check the H3014 boards for proper seating, refer to Chapter 4 for the procedures when removing the Field Replaceable Units (FRUs) of the H3014 and checking power supply voltages.

11. On successful completion of EVDAE, remove the 29-24929-00 loopback connectors from the H3014 distribution panel.

12. Execute the DMZ32 on-line diagnostic EVDAF with internal loopback set (loop type equals four). Refer to Chapter 4 for details.

    If a failure occurs, perform the following:

    - Check for proper module seating,
    - Verify proper UNIBUS placement, and
    - Check voltages.

    IF THE FAULT IS NOT CORRECTED, REFER TO CHAPTER 4 FOR CORRECTIVE ACTION.

13. After the DMZ32 has passed the EVDAF diagnostic, execute the User Exerciser Test Program (UETP). If a failure occurs during UETP, check the system configuration.

14. After the DMZ32 has passed UETP, return the system to the normal configuration and initiate customer acceptance.

NOTE

Refer to Figure 2-15 for the DMZ32 installation overview to see how all component parts tie together.

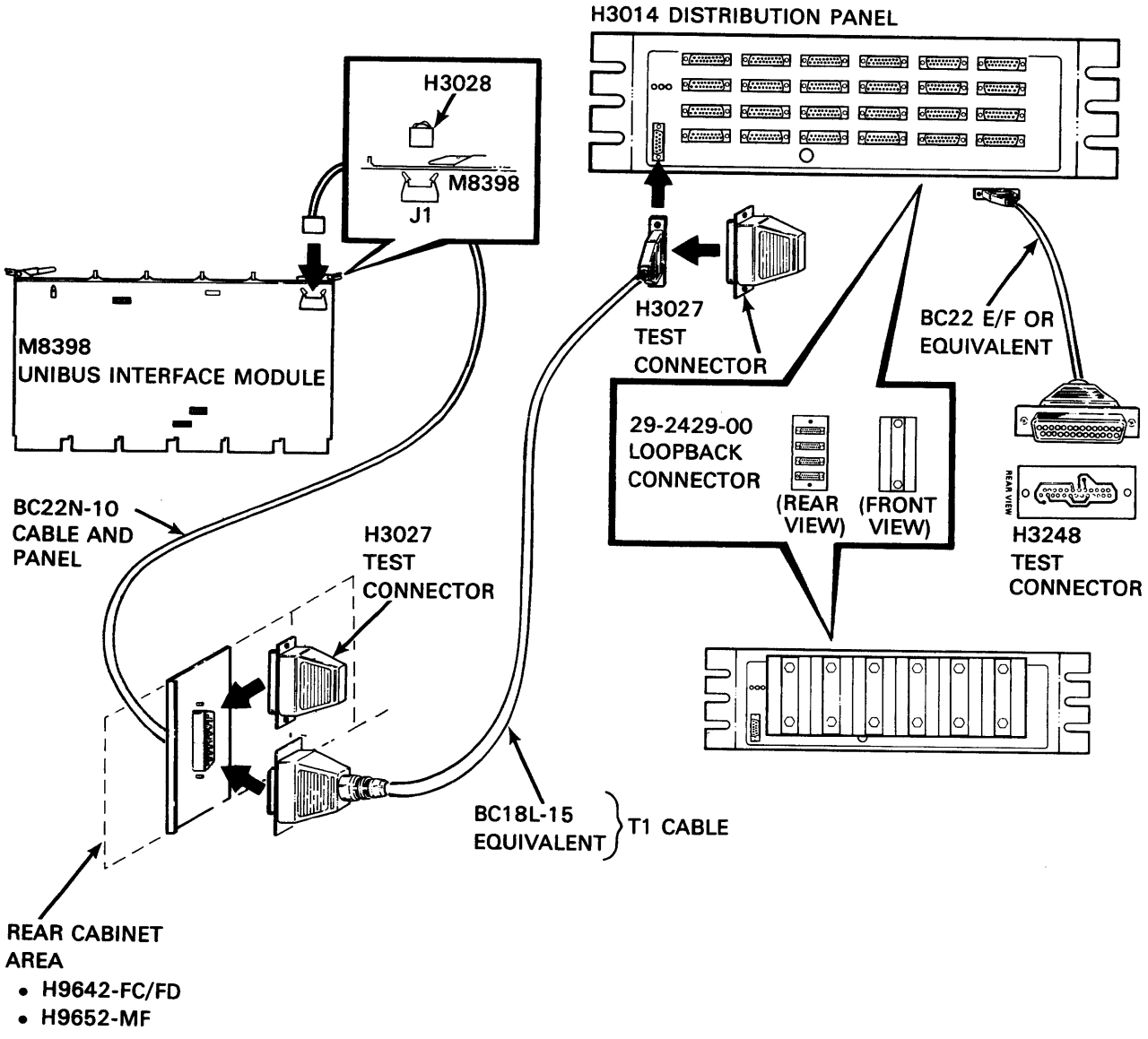


Figure 2-15 DMZ32 Installation Overview

2.7 DMZ32 INSTALLATION CHECKLIST

PHASE I – Preinstallation Considerations

1. System Requirements (Section 1.5)

   a. M8398 Module (Section 1.5.1)

UNIBUS Loading	___/___/___
Power Requirements	___/___/___
Interrupt Priority Level	___/___/___
DMZ32 Device Address Determination	___/___/___

   b. H3014 Distribution Panel (Section 1.5.2)

Power Requirements	___/___/___

PHASE II – M8398 Installation

1.	Unpack DMZ32 option and verify that all components were shipped (Section 2.2 and Table 2-1)	___/___/___
2.	E-63 set for proper priority level (Section 2.5.1 and Figure 2-1)	___/___/___
3.	E-53 S1 through S8 set to UNIBUS address, refer to Appendix A for UNIBUS address (Figure 2-1)	___/___/___
4.	E-53 S9 set to "ON" (Figure 2-1)	___/___/___
5.	E-53 S10 set to "ON" (Figure 2-1)	___/___/___
6.	NPG wire (CA1 –CB1) removed	___/___/___
7.	Backplane resistance checks complete	___/___/___
8.	With power ON, verify selected SPC backplane voltages	___/___/___
9.	Install M8398 module into selected SPC slot of the backplane	___/___/___

PHASE III – H3014 Installation

1. Unpack H3014 distribution panel and verify that all components were shipped ____/____/____
2. Install H3014 into proper cabinet ____/____/____
3. Connect power cable to switched output of power controller (Section 2.5.2) ____/____/____
4. If the H3014 is received in a cabinet, remove the shipping bracket ____/____/____

PHASE IV – Cable Installation

1. Connect the 2 × 4 I/O panel supplied with the DMZ32 to the BC22N-10 cable ____/____/____
2. Remove blank I/O panel from the FCC Bulkhead Frame to make space for the new I/O panel supplied with the DMZ32 ____/____/____
3. Connect BC22N-10 cable to the M8398 module ____/____/____
4. Connect BC18L-15 cable between the BC22N-10 2 × 4 I/O panel and the H3014 distribution panel ____/____/____

PHASE V – DMZ32 System Checkout

1. Run EVDAE with H3028 connected to J1 of the M8398 module (Section 2.6) ____/____/____
2. Connect M8398 module to the BC22N-10 cable I/O panel (Figure 2-10) ____/____/____
3. Run EVDAE with the H3027 connected to the BC22N-10 cable (Section 2.6) ____/____/____
4. When power is applied to the H3014, the front panel LEDs display a normal indication (Refer to Table 4-4) ____/____/____
5. Run EVDAE with BC18L-15 connected to the I/O panel with an H3027 turnaround connected to the open end of the cable. [If a remote cable, connect the H3027 to the far end of the T1 cable ONLY if the cable is 762 m (2500 ft) or less in length] ____/____/____

6. Disconnect the H3027 from the T1 cable and connect the T1 cable to the H3014 T1 connector. Then place six (6) 29-24929-00 staggered turnaround connectors on the H3014 distribution panel and run EVDAE. EVDAE runs successfully under all conditions (Section 2.6) ____/____/____

7. EVDAF runs successfully under all conditions (Section 2.6) ____/____/____

8. Remove all loopback connectors, and turn the system over to the customer ____/____/____

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter describes the different registers that control the operation of the DMZ32. Each register is listed and the different bits of each register are defined.

3.1.1 Overview

The DMZ32 asynchronous multiplexer contains three (3) octets of eight (8) transmit and eight (8) receive lines, each making a total of 24 lines available for data. These 24 lines may be programmed to operate at one of 14 baud rates from 50 bits/s to 19,200 bits/s. All 24 lines have the capability of operating with different receive and transmit baud rates. All lines have modem control and each receive and transmit line can be independently enabled or disabled. There is a separate receive and transmit interrupt vector for each of the 3 octets. These vectors may be enabled or disabled independently. Separate TX READY and RX DATA AVAILABLE bits exist for each octet to allow for non-interrupt driven device operation. These octets can be operated independently. For example, each octet can be reset without affecting any of the other octets.

In the DMZ32, receive characters with their respective line numbers and status information are stored in a 128-character silo. Each octet has its own RX silo. An interrupt may be generated for the following reasons:

- The RX silo contains 64 characters, or
- The RX silo has been nonempty for more than a programmed time interval since the last time the RX silo was read.

The DMZ32 may be programmed to echo all received characters.

Each transmit line has its own 32-character TX silo. All characters to be transmitted must first be loaded into the respective TX silo. The TX silo may be loaded in one of two ways. The first method (programmed mode) is to use CPU move instructions to load one or two characters at a time into the proper indirect address register. The second method (DMA mode) is by means of Direct Memory Access (DMA) transfers from main memory. Once a DMA transfer has been initiated, characters are automatically put into the TX silo every time the TX silo count drops below eight characters. This cycle continues until the DMA byte count is zero. When the last character to be transmitted is fetched from the TX silo, an interrupt will be generated if requested. If desired, each TX silo may be flushed, resulting in emptying the TX silo and zeroing any remaining DMA byte count. If the TX interrupt enable bit is HIGH, an interrupt is generated.

Each transmit line may be operated in an automatic XON/XOFF mode. The line's receiver must be enabled for this mode to operate. When enabled, a received XOFF character causes the respective transmit line to be disabled. In a similar manner, receiving an XON character causes the transmit line to be enabled. In both cases, the XON or XOFF character is stored in the octet's RX silo so that the operating system is aware that transmissions have been either enabled or disabled. This mode of operation allows for long RX silo timeouts as the time-critical XOFF instantly disables the transmitter.

3.1.2 Device Registers

The UNIBUS to DMZ32 interface uses three (3) groups of four (4) device registers, one for each octet. The four device registers are:

- Octet Control and Status Register (OCTET.CSR),
- Octet Line Parameter Register (LINE.PAR.REG),
- Octet Receive Buffer (RX.BUF)/OCTET Receive Silo Parameter (RSP.REG), and
- Octet Indirect Registers (IND.REG).

3.1.3 Octet Control and Status Register (OCTET.CSR)

The OCTET.CSR is used for the following:

- To select one of four indirect registers,
- To select a register line number,
- To initiate a Master Reset,
- To enable/disable receive and transmit interrupts,
- To indicate when data is in the RX silo,
- To indicate when a TX silo is empty, and
- To indicate a NXM error.

3.1.4 Octet Line Parameter Register (LINE.PAR.REG)

The LINE.PAR.REG is used to specify the following:

- The bits per character,
- The number of stop bits per frame,
- The receive and transmit baud rates, and
- The parity enable/disable and sense.

3.1.5 Octet Receive Buffer (RX.BUF)/OCTET Receive Silo Parameter (RSP.REG)

The RSP.REG is used to read the following:

- The received character, and
- The status byte associated with the received character.

The RSP.REG is used to write the RX silo alarm timeout value.

3.1.6 Octet Indirect Register (IND.REG)

The IND.REG is used as a window to one of four registers (IND.REG 0, IND.REG 1, IND.REG 2, or IND.REG 3). The following can be performed by the appropriate registers:

- IND.REG 0
  - Write to the TX silo
  - Read the TX silo count
  - Read the RX modem signals

- IND.REG 1

  - Enable a pre-empt character
  - Set the TX modem signals
  - Enable the maintenance control functions
  - Enable the reporting of an RX modem signal change
  - Flush the TX silo
  - Break the TX line
  - Enable the receiver and/or transmitter
  - Enable auto XON/XOFF

- IND.REG 2

  - Specify the lower 16 bits of a DMA buffer address

- IND.REG 3

  - Specify the upper two bits of a DMA buffer address
  - Specify the DMA transfer byte count

3.2 INITIAL OPERATION

Before the DMZ32 can be prepared for loading line parameters, the system itself must be checked for proper operation. A selfdiagnostic routine within the DMZ32 is run to verify proper operation. This self-diagnostic is run under the following conditions:

- On powerup,
- After UNIBUS Initialization (INIT),
- M8398 pushbutton switch, and
- AA00 to the diagnostic register.

3.3 PARAMETER INITIALIZATION

After an INIT or a Master Reset has occurred within the DMZ32, the transmit and receive buffers are empty and all lines are disabled. Before operation can begin, the operating system must load the line parameter register (LINE.PAR.REG<15:0>) with the desired parameters for specific lines before enabling these lines. (The line parameter registers must be loaded even if all parameters are zero.)

The line number whose parameters are to be loaded is contained in the lower order byte of the Line Parameter Register, LINE.SELECT <2:0>. After the program optionally sets the appropriate interrupt enable bits in the Control and Status Register (CSR<15:0>), the program is ready to enable the desired transmit and receive lines.

TX modem control signals coming from the DMZ32 can be set or cleared at any time after an INIT or a Master Reset. The TX modem signals are cleared only after an INIT and are not affected by a Master Reset.

RX modem control signals going to the DMZ32 are loaded into the respective device register every time there is a change on one or more of the signal lines. An INIT or a Master Reset also causes a device register update.

3.4 TRANSMIT OPERATION

Before the transmission of data can occur, a line must be enabled. The enabling of a transmit line is performed by setting the appropriate bit in the IND.REG 1 register. If the appropriate bit is not set, the line is disabled and held in the marking state (providing the line is not programmed for auto echo or remote loopback).

TX.RDY is asserted whenever a transmit silo becomes empty due to a character being tranmsitted from the silo or a silo flush.

If TX.I.E. is active when TX.RDY becomes set, then an interrupt to the transmit vector is posted. The program should read OCTET.CSR<15:0> in order to determine the cause of the interrupt. If TX.RDY is set, then OCTET.CSR<2:0> will contain the line number where the silo is empty. OCTET.CSR<13> is set if the transmission has been stopped due to an aborted DMA transfer. The act of reading OCTET.CSR<15:0> clears TX.RDY. This is important because TX.RDY has to be cleared before the DMZ32 can assert TX.RDY for another line.

To minimize the possibility of interrupt overload from occurring, the program should attempt to keep silos full at all times. If the program decides to fill a specific silo, it may inspect the transmit silo count register to determine how many characters have been transmitted from the silo while it is being filled. The silo count indicates how many full positions there are in the silo. Because of this, a silo count of zero indicates an empty silo, and a silo count of 32 indicates a full silo. The transmit silo count registers may be examined at any time and any particular line's silo may be loaded or flushed. These operations may be performed whether the respective transmit line is enabled or not. If a line is disabled while its silo is being emptied, transmission stops after the current character has been transmitted. However, if the silo has been loaded, the silo contents will remain and upon enabling the line, transmission from the silo will resume as normal.

3.5 RECEIVER OPERATION

The receive lines in the DMZ32 are enabled by setting appropriate bits in IND.REG 1. A line must be enabled in order to receive data. All lines in each octet share a 128-character receive silo. There is no DMA mode for the receiver.

3.6 DEVICE REGISTERS AND VECTOR ASSIGNMENTS

A block of 16 words has been assigned to the registers that control the DMZ32. This block includes the base CSRs and four line registers for each octet. The base address is selected in the floating CSR range by means of DIP switches on the DMZ32 module. (Refer to Appendix A for the floating device addresses and vectors.)

The floating CSRs for the DMZ32 are in a contiguous block of 14 words. (Refer to Figure 3-1.) Eight switches on the DMZ32 determine bits <12:5> of the starting address. The registers contained in this block can be addressed only by word except the registers that are used to access a line's transmit silo. Access by word means that the instruction operating on the register causes a data out (DATO) rather than a data out byte (DATOB) UNIBUS cycle. The DMZ32 pays no attention to the least significant UNIBUS address bit on registers that are word access only. Because of this, the register block must be located on a 20-hex address boundary. The 16 words are allocated to the devices as shown in Figure 3-1.

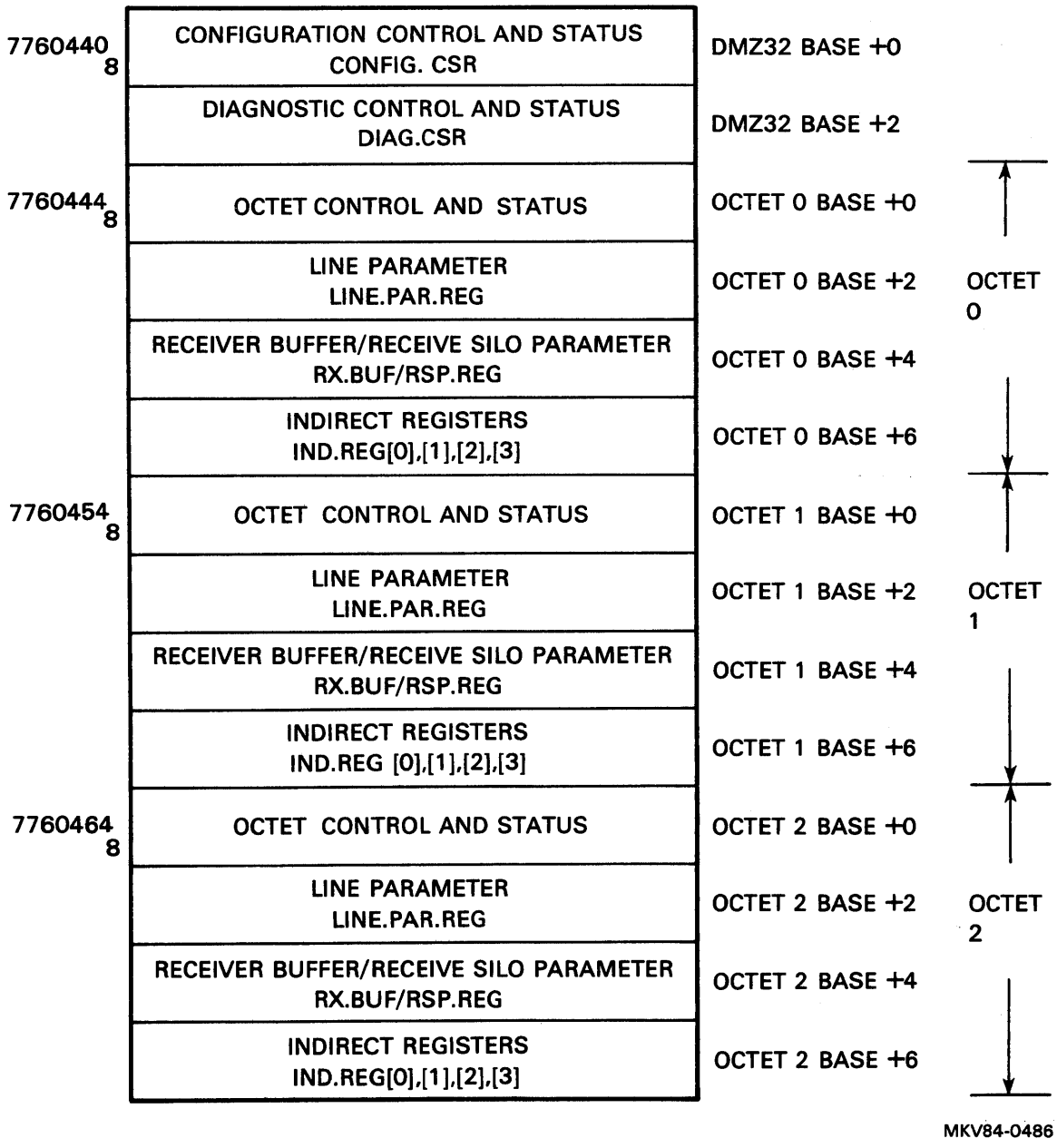


Figure 3-1 DMZ32 Word Allocation of Device Control/Status Registers

3.7 CONFIGURATION CONTROL AND STATUS REGISTER (CONFIG.CSR)

The configuration control and status register has an address that establishes the rest of the remaining addresses for the DMZ32. Refer to Appendix A for the floating device addresses and vectors. This register is used by the VAX/VMS operating system at the time the system is being automatically configured.

The autoconfiguration routine scans each bit of the CONFIG.CSR register to determine what type drivers should be loaded.

Refer to Figure 3-2 for a bit map overview of the DMZ32 registers.

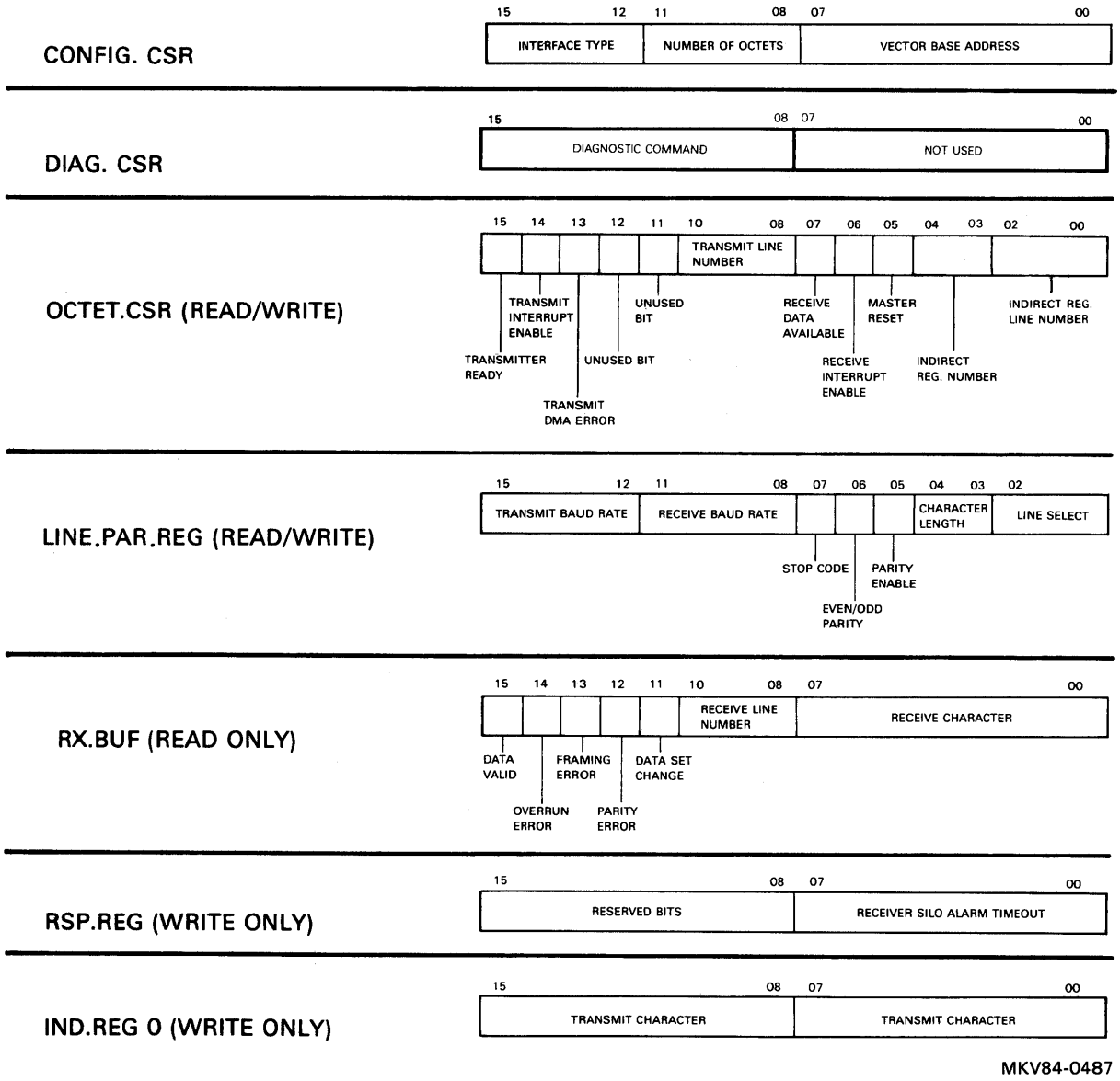


Figure 3-2 DMZ32 Register Bit Map Overview (Sheet 1 of 2)

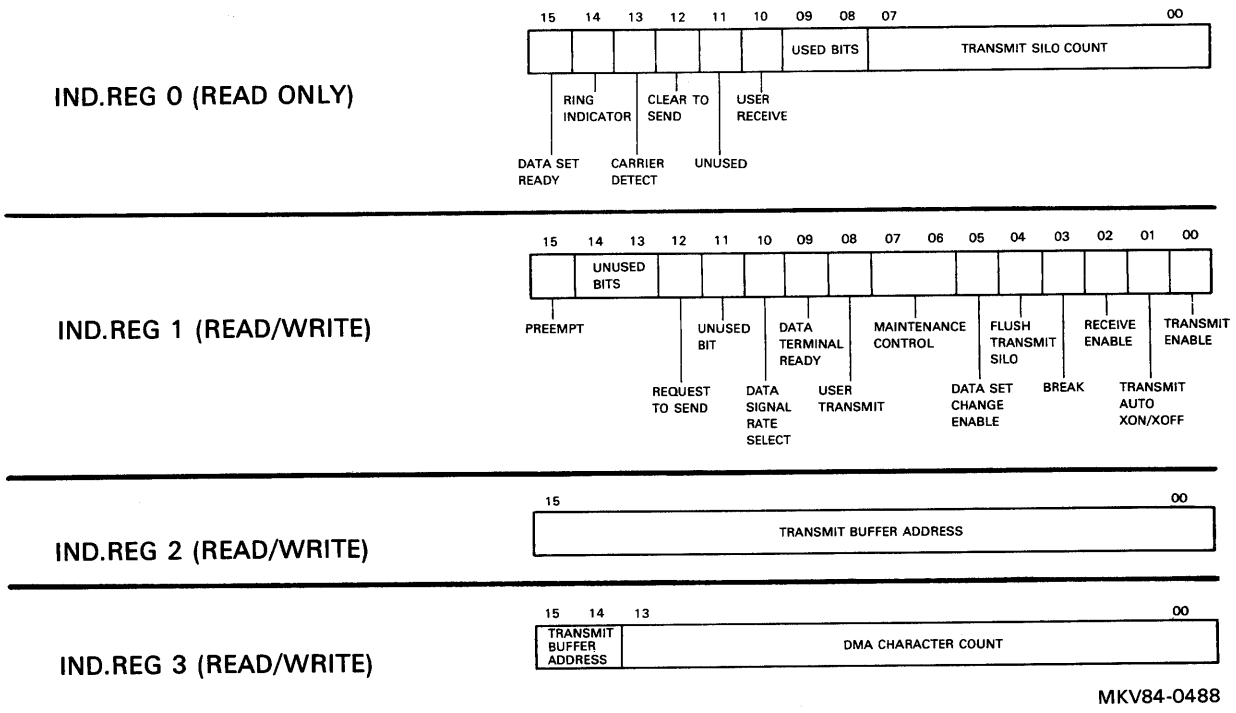


Figure 3-2 DMZ32 Register Bit Map Overview (Sheet 2 of 2)

There are six interrupt vectors used by the M8398 contiguous to the first vector. There are no switches on the M8398 module that have control over the interrupt vectors because the interrupt vectors are under software control. Refer to Figure 3-3 for the CONFIG.CSR bit map.

Refer to Table 3-1 for the bit map of the configuration control and status register (CONFIG.CSR<15:0>).

This register may be accessed with a Read Modify Write (RMW) cycle.

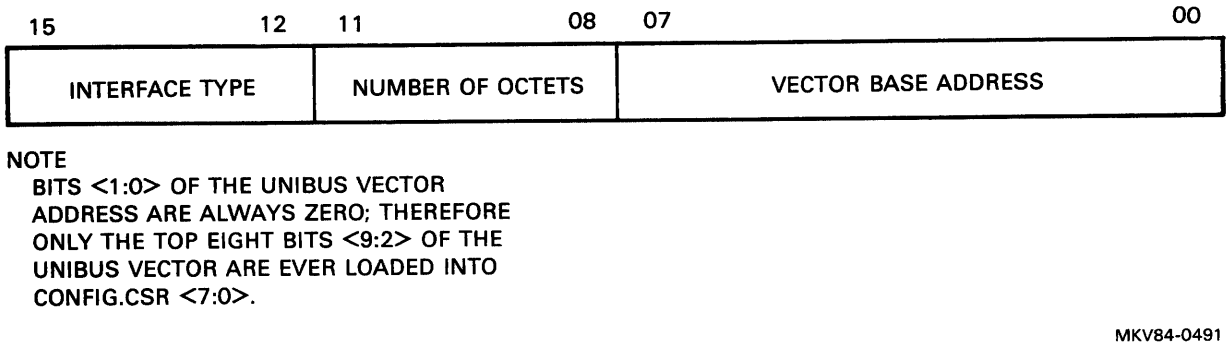


Figure 3-3 Configuration Control and Status Register (CONFIG.CSR) Bit Map

Table 3-1 Configuration Control and Status Register Functions

Bits	Title	Function
<7:0>	Vector	The CONFIG.CSR<7:0> is read/write and is loaded at autoconfiguration with the vector address of vector [0]<9:2>. The six floating interrupt vector addresses are: • Vector [0]<9:2> Receive vector for FIRST octet, • Vector [1]<9:2> Transmit vector for FIRST octet, • Vector [2]<9:2> Receive vector for SECOND octet, • Vector [3]<9:2> Transmit vector for SECOND octet, • Vector [4]<9:2> Receive vector for THIRD octet, and • Vector [5]<9:2> Transmit vector for THIRD octet. **NOTE** **There are no switches on the DMZ32 for interrupt vectors. The six vector locations are loaded by the operating system at autoconfiguration time. The other vectors are assumed to be contiguous as shown below.** • **Vector [0]<9:2> = 320** • **Vector [1]<9:2> = 324** • **Vector [2]<9:2> = 330** • **Vector [3]<9:2> = 334** • **Vector [4]<9:2> = 340** • **Vector [5]<9:2> = 344** **These bits are cleared upon receipt of INIT.D executing the microdiagnostic.**
<11:8>	Number	CONFIG.CSR<11:8> is always read as a binary value of three. When a binary three (11) is present in CONFIG.CSR<9:8>, a 24-line unit (three eight-line groups or octets) is to be configured.
<15:12>	Interface	CONFIG.CSR<15:12> is always read as zero and controls the loading of drivers. Because only asynchronous lines are available, only asynchronous drivers are loaded.

3.8 DIAGNOSTIC CONTROL AND STATUS REGISTER (DIAG.CSR)

The diagnostic control and status register has an address of Device Base + 2.

The diagnostic control and status register (DIAG.CSR) is the UNIBUS window into the DMZ32. The DIAG.CSR can be regarded as a device used by the host processor in controlling trunk loopback functions, monitoring test status, requesting/reporting microcode revision numbers, and starting on-board diagnostics.

3.8.1 Diagnostic Control and Status Register (DIAG.CSR<15:0>) – Write

The bit map for the DIAG.CSR<15:0> – Write – can be seen in Figure 3-4. *The DMZ32 uses only the upper byte (<15:8>) of this register for commands.* This is for DMF32 conformity. (Refer to Table 3-2 for the functions performed.)

This register may NOT be accessed with an RMW cycle; it can be accessed by word only.

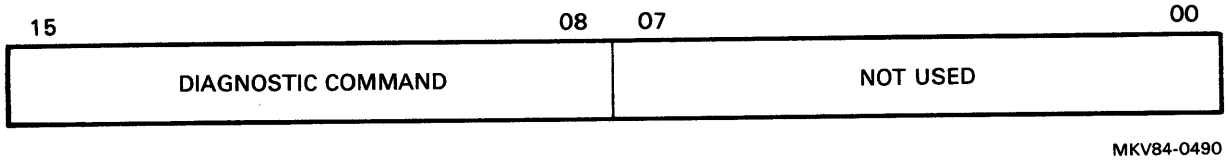


Figure 3-4 Diagnostic Control and Status Register DIAG.CSR<15:0> Bit Map – Write

Table 3-2 Diagnostic Control and Status Register DIAG.CSR<15:0> – Write

Bits	Hex	Decimal	Octal	Function/Test Description
<15:8>				
	AA	170	252	Start self-test
	55	85	125	Halt UBI microcode
	2A	42	52	Read UBI microcode version number
	2B	43	53	Read TIU microcode version number
	2C	44	54	Read RDP microcode version number
	2D	45	55	Set local trunk loopback
	2E	46	56	Clear local trunk loopback
	31	49	61	Set ALL lines loopback (EIA)
	32	50	62	Clear ALL lines loopback (EIA)
	33	51	63	Read T1 status register

3.8.2 Diagnostic Control and Status Register DIAG.CSR<15:0> – Read

The bit map for the DIAG.CSR<15:0> – Read – is shown in Figure 3-5. (Refer to Table 3-3 for the functions performed.)

This register may NOT be accessed with an RMW cycle, it can be accessed by word only.

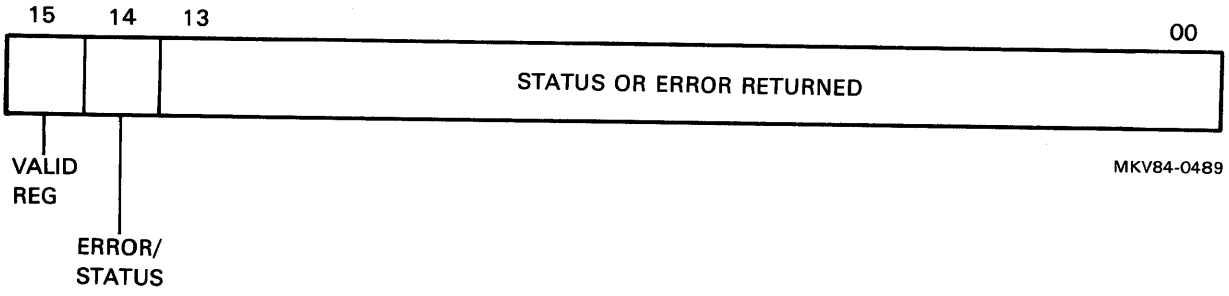


Figure 3-5 Diagnostic Control and Status Register DIAG.CSR<15:0> Bit Map – Read

Table 3-3 Diagnostic Control and Status Register DIAG.CSR<15:0>

Bits	Hex	Decimal	Octal	Function/Test Description
<15>	(Valid Data Flag)			This bit is used to indicate if the content of the diagnostic register is valid. If it is not set, the microcode is still executing the self-test.
<14>	(Status or Error Flag)			This bit indicates if the content of the diagnostic register is a status return or an error return. 0 = Status 1 = Error
<13:0>	(Status or Error Return)			

NOTE
Refer to Table 4-1 for details.

3.9 OCTET CONTROL AND STATUS REGISTER (OCTET.CSR) – READ/WRITE

The octet control and status register (OCTET.CSR<15:0>) has an address of Octet Base + 0. The bit map for the OCTET.CSR<15:0> is shown in Figure 3-6. (Refer to Table 3-4 for the bit functions performed by this register.)

This register may NOT be accessed with an RMW cycle.

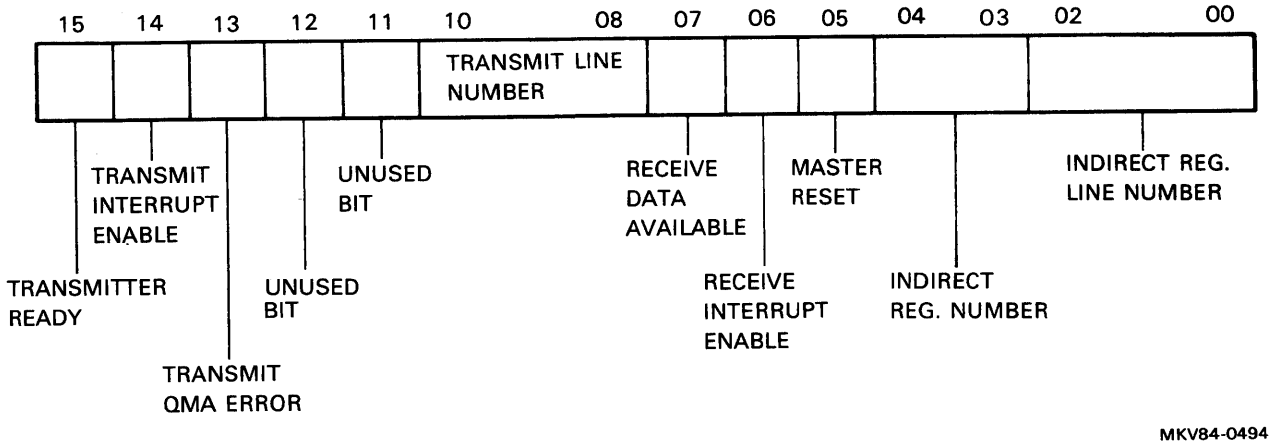


Figure 3-6 Octet Control and Status Register (OCTET.CSR) Bit Map

Table 3-4 Octet Control and Status Register Functions

Bits	Title	Function
<15>	Transmitter Ready	This bit is set when an enabled line (pointed to by OCTET.CSR <10:8>) has loaded the last character from the silo into the respective line holding register. This read/write bit is cleared by a Master Reset, INIT, or the act of reading this register.
<14>	Transmit Interrupt Enable	When set, this bit allows interrupt requests to be made to the transmit vector when TX.RDY is set. A Master Reset or INIT clears this read/write bit.
<13>	Transmit DMZ.NXM Error	This bit is used only when the respective line is in DMA mode. This bit is set for the indicated line if the DMZ32 UNIBUS controller either did not receive a SSYN at least 32 microseconds after issuing a MSYN, or the controller could not become bus master for at least 32 microseconds after having asserted BUS NPR. OCTET.CSR <2:0> points to the line in error. This read only bit is cleared when the program reads this register by Master Reset, or an INIT.

Table 3-4 Octet Control and Status Register Functions (Cont)

Bits	Title	Function
<12>	Not Used	
<11>	Not Used	
<10:8>	Transmit Line Number	When TX.RDY is set, the Transmit Line contains the number of the line whose silo has become empty. These bits are read only, and are cleared by a Master Reset, INIT, or the act of reading this register.
<7>	Receive Data Available	This read only bit is set whenever data is available in the receive silo and is automatically cleared when the receive silo is empty. Receive Data Available (RX.DATA.AVAIL) is cleared by a Master Reset or INIT.
<6>	Receive Interrupt Enable	When this read/write bit is set, interrupt requests can be made to the receive vector under the following conditions: • Receive Data Available has been set for longer than the timeout period, and • 64 characters have entered the receive silo. This read/write bit is cleared by a Master Reset or INIT.
<5>	Master Reset	When this read/write bit is set, a Master Reset is initiated. This bit remains set while resetting is taking place and is cleared after Master Reset has occurred. This bit remains set after a self-test failure. The program should not access device registers of the octet being reset (other than this one) while reset is occurring. Writing to this register while a Master Reset is taking place has no effect. Master Reset takes up to 500 microseconds. **NOTE** **Performing the Master Reset function affects only one octet. Each octet must be individually reset.**
<4:3>	Indirect Register Number	These read/write bits point to one of four (4) indirect registers. These bits are automatically cleared by Master Reset or INIT.
<2:0>	Indirect Register Line Number	These read/write bits point to one of eight (8) indirect register groups. This register is accessed through location Octet Base + 6. These bits are automatically cleared by Master Reset or INIT.

3.10 LINE PARAMETER REGISTER (LINE.PAR.REG<15:0>) - READ/WRITE

The line parameter register has an address of Octet Base + 2. The bit map for the line parameter register is shown in Figure 3-7. Refer to Table 3-5 for individual bit functions.

This register may be accessed with a RMW cycle.

NOTE

The line parameter register should ALWAYS be loaded with the parameter for the particular line before the line is enabled (even if the parameters are all zeros).

Bits <2:0> are used to specify the line number when writing only. When reading, OCTET.CSR <2:0> selects the line number.

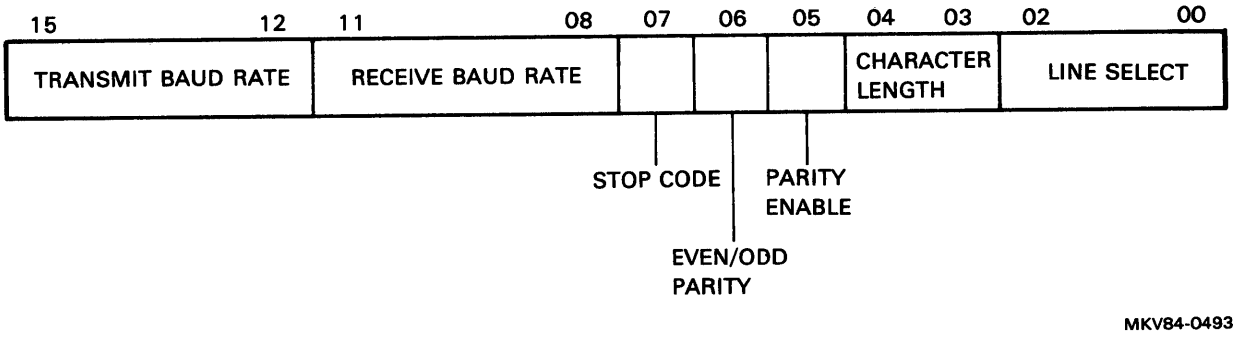


Figure 3-7 Line Parameter Register (LINE.PAR.REG.<15:0>)

Table 3-5 Line Parameter Register Functions

Bits	Title	Function
<15:12>	Transmit Baud Rate	When a line is selected, these bits specify one of the following 14 transmit baud rates:

Bits <15:12>	Baud	Rate
0000	50	Baud
0001	75	Baud
0010	110	Baud
0011	134.5	Baud
0100	150	Baud
0101	300	Baud
0110	600	Baud
0111	1200	Baud
1000	1800	Baud

Table 3-5 Line Parameter Register Functions (Cont)

Bits	Title	Function
		1001 2000 Baud 1010 2400 Baud 1100 4800 Baud 1110 9600 Baud 1111 19200 Baud
<11:8>	Receive Baud Rate	Split baud rate capability is supported. When a line is selected, the receive baud rate specifies the selected receiver's baud rate. Bits <15:12> Baud Rate 0000 50 Baud 0001 75 Baud 0010 110 Baud 0011 134.5 Baud 0100 150 Baud 0101 300 Baud 0110 600 Baud 0111 1200 Baud 1000 1800 Baud 1001 2000 Baud 1010 2400 Baud 1100 4800 Baud 1110 9600 Baud 1111 19200 Baud
<7>	Stop Code	This bit specifies the number of stop bits for the selected line as follows: Logic 0 = 1 stop bit Logic 1 = 2 stop bits
<6>	Even/Odd Parity	When parity enable is set, even/odd parity specifies which parity is being used as follows: Logic 0 = odd character parity Logic 1 = even character parity
<5>	Parity Enable	When set, this bit causes a parity bit to be generated on transmission. The parity bit is checked and stripped on reception of the selected line.
<4:3>	Character	These two bits specify the character length (not counting start, stop, and parity bits, if enabled) for the selected line as follows:

Table 3-5 Line Parameter Register Functions (Cont)

Bits	Title	Function
		00 = 5 bits per character 01 = 6 bits per character 10 = 7 bits per character 11 = 8 bits per character
<2:0>	Line Select	These bits contain the binary number of the line whose parameters are to be written. Selection of a particular line for reading is done by way of OCTET.CSR<2:0>.

3.11 RECEIVE BUFFER REGISTER (RX.BUF<15:0>) READ ONLY

The receive buffer register has an address of Octet Base + 4. Refer to Figure 3-8 for the bit map of the receive buffer register and Table 3-6 for the functions of each bit contained in this register.

It is through the receive buffer register that the program accesses the receive silo. Every time this register is read, data words in the silo shift down by one position. Successive read cycles access successive silo entries. This receive silo not only contains receive characters and associated status information, but also contains data set change information. Master Reset or INIT flushes the silo.

This register may NOT be accessed by an RMW cycle.

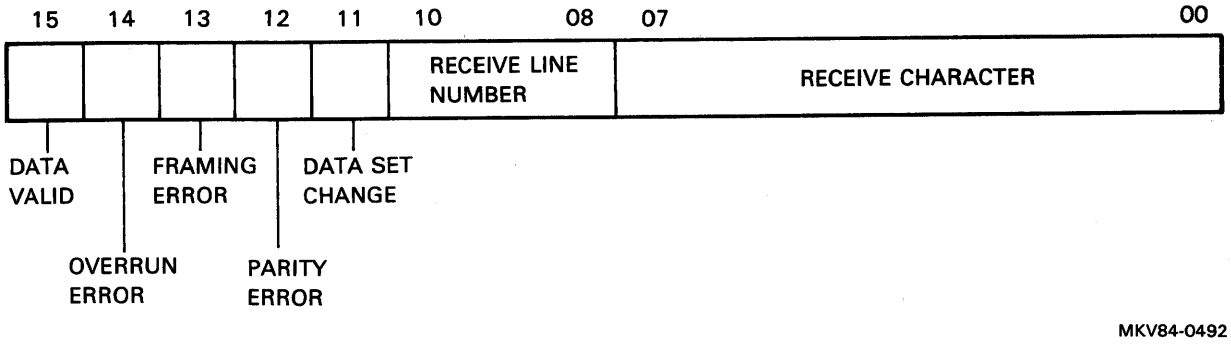


Figure 3-8 Receive Buffer Register (RX.BUF) Bit Map – Read Only

Table 3-6 Receive Buffer Register Functions

Bits	Title	Function
<15>	Data Valid	When this bit is set, the remaining bits are valid. This bit is set when data is loaded into the receive buffer register. This bit remains set as long as there is data in the buffer. This bit is cleared by Master Reset, INIT, or when the receive buffer becomes empty.
<14>	Overrun Error	This bit is useful only if Data Set Change (RX.BUF<11>) is clear. This bit is set if one or more previous characters were lost on the line due to the silo being full.
<13>	Framing Error	This bit is useful only if Data Set Change (RX.BUF<11>) is clear. This bit is set if the line on which the character was received was in the spacing (0) state at the time the first stop bit was sampled.
<12>	Parity Error	This bit is useful only if the Data Set Change (RX.BUF<11>) is clear. If parity error has been enabled for the line on which the character is received, and the character is received incorrectly, this bit will be set.
<11>	Data Set Change	When this bit is set, RX.BUF<7:0> is zero, and RX.BUF<10:8> contains the line number of the modem line that has changed.
<10:8>	Receive Line Number	These bits contain the binary number of the line on which a character was received and a data set change experienced.
<7:0>	Receive Character	These bits contain the received character only if RX.BUF<11> is clear. If parity is enabled, the parity bit is stripped off. Characters less than eight bits in length are right justified with the high order bits set to zero. If RX.BUF<11> is set, then RX.BUF<7:0> will be zero and the program should read the RX.MODEM signal.

3.12 RECEIVE SILO PARAMETER REGISTER (RSP.REG<15:0>) - WRITE ONLY

The receive silo parameter register has an address of Octet Base + 4. This register is write only and is accessed by word. The receive silo parameter register contains the receive silo alarm timeout. Refer to Figure 3-9 for the bit map and Table 3-7 for the bit description of the receive silo parameter register.

This register may NOT be accessed by an RMW cycle.

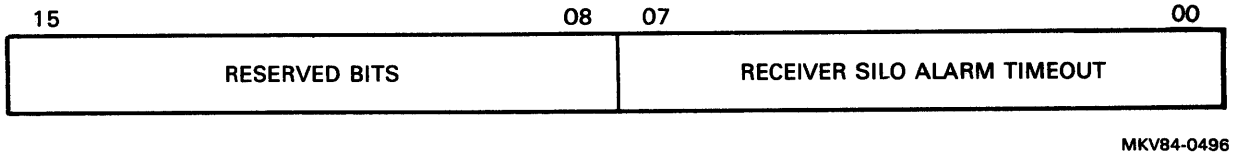


Figure 3-9 Receive Silo Parameter Register (RSP.REG) Bit Map - Write Only

Table 3-7 Receive Silo Parameter Register Functions

Bits	Title	Function
<15:8>		Reserved Bits
<7:0>	Receive Silo Alarm Timeout	These bits specify the silo alarm timeout period. An interrupt is generated if data has been sitting in the silo for a time equal to or longer than the timeout period. Every time the receive silo is read, a Master Reset occurs or an INIT occurs, restarting the internal timer. The timeout period can range from 0 to approximately 255 milliseconds. Loading a value of zero into this register causes an infinite timeout. The following shows the progression of how these eight bits specify the silo alarm rate: • 00000000 = Infinite timeout • 00000001 = Approximately one (1) millisecond timeout • 00000010 = Approximately two (2) milliseconds timeout • 00000011 = Approximately three (3) milliseconds timeout • 11111111 = Maximum timeout, approximately 255 milliseconds. Approximately one (1) millisecond is added for each bit increment. This timer is based on microcode loops and is not very accurate. The receive silo alarm timeout is set to a value of 1 after a Master Reset or INIT.

3.13 INDIRECT REGISTERS

There are 32 indirect registers associated with each octet of the DMZ32. Only the generic indirect registers are covered in this chapter. The generic indirect registers covered are IND.REG 0, IND.REG 1, IND.REG 2, and IND.REG 3.

The indirect registers are addressed by the five-bit address in the octet control and status register <4:0>. The lower three bits of the address OCTET.CSR<2:0> indicate the line number being referenced, and the upper two bits OCTET.CSR<4:3> select which indirect register of that line is being accessed.

3.14 INDIRECT REGISTER (IND.REG[0]<15:0>) – WRITE ONLY

The indirect register [0] has an address of Octet Base + 6. This write only register should be written to only while in the Programmed mode of operation. In the DMA mode of operation, writing to this register still loads characters into the TX silo. This is permissible but results in the mixing of the two data streams.

Writing to this register enters one or two characters into the 32-character transmit silo for the selected line. If the write to this register is a WORD; for example, UNIBUS DATO, then two characters are loaded into the silo. The character in the lower byte is loaded into the silo first. If the write to this register is a BYTE; for example UNIBUS DATOB, then only the lower byte is loaded into the silo, and the high order character is ignored.

Refer to Figure 3-10 for the bit map and Table 3-8 for the bit description of the indirect register 0 – Write Only.

This register may NOT be accessed by an RMW cycle.

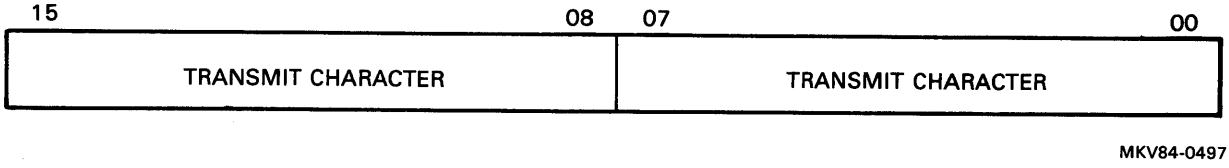


Figure 3-10 Indirect Register (IND.REG[0]<15:0>) Bit Map – Write Only

Table 3-8 Indirect Register 0 Functions

Bits	Title	Function
<15:0>	Transmit Character Buffer	This register is reserved for data that is being transmitted.

3.15 INDIRECT REGISTER (IND.REG[0]<15:0>) - READ ONLY

The indirect register [0] has an address of Octet Base + 6. Refer to Figure 3-11 for the bit map and Table 3-9 for the bit description of the indirect register 0 - Read Only.

This register may NOT be accessed by an RMW cycle.

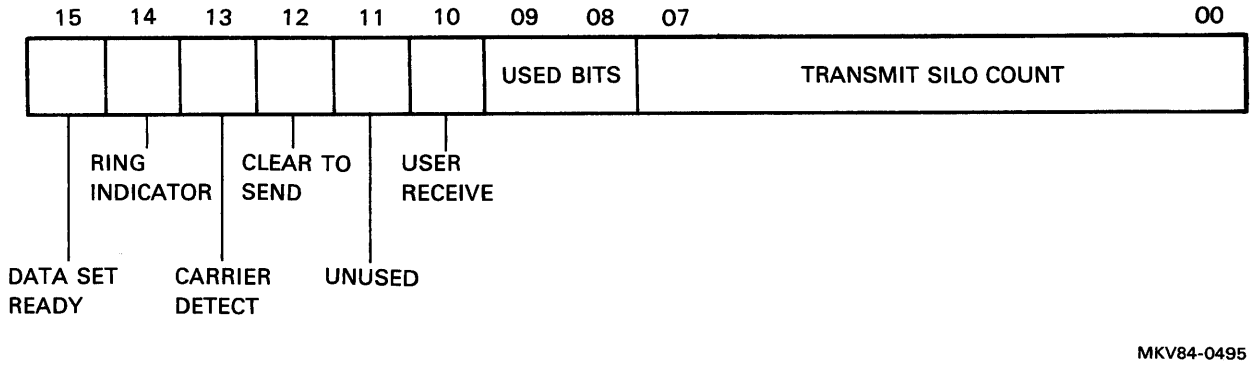


Figure 3-11 Indirect Register (IND.REG[0]<15:0>) Bit Map -Read Only

Table 3-9 Indirect Register 0 Functions – Read Only

Bits	Title	Function
<15:8>	Receive Modem Status	This byte contains the receive modem status for the selected line. All modem signals represented in this register come from the Data Communications Equipment (DCE). The MODEM.RX byte is updated after a Master Reset or INIT but not flagged in the RX silo. If the receive silo is full and data set change enable (IND.REG[1]<5>) is set, a data set change will be flagged only after the silo becomes nonfull. In this way, data set changes are not lost when the RX silo is full.
<15>	Data Set Ready	This bit reflects the state of the Data Set line (RS-232-C circuit CC) coming from the modem connected to the selected line.
<14>	Ring Indicator	This bit reflects the state of the Ring Indicator line (RS-232-C circuit CE) coming from the modem connected to the selected line.
<13>	Carrier Detect	This bit reflects the state of the Received Line Signal Detector line (RS-232-C circuit CF) coming from the modem connected to the selected line.
<12>	Clear To Send	This bit reflects the state of the Clear To Send line (RS-232-C circuit CB) coming from the modem connected to the selected line.
<11>	Not Used	
<10>	User Receive	This bit is connected to pin 25 of the RS-232-C connector on the distribution panel. This bit may be used for whatever purpose the user desires.
<9:8>	Not Used	
<7:0>	Transmit Silo Count	These bits contain the number of entries in the 32-character transmit silo for a selected line. They are cleared after Master Reset or INIT.

3.16 INDIRECT REGISTER (IND.REG[1]<15:0>) -READ/WRITE

The indirect register [1] has an address of Octet Base + 6. This read/write register is cleared by a Master Reset or INIT. This register must be loaded with the appropriate information prior to using a line after Master Reset.

Refer to Figure 3-12 for the bit map and Table 3-10 for the bit map description of the indirect register 1 – Read/Write.

This register may be accessed by an RMW cycle.

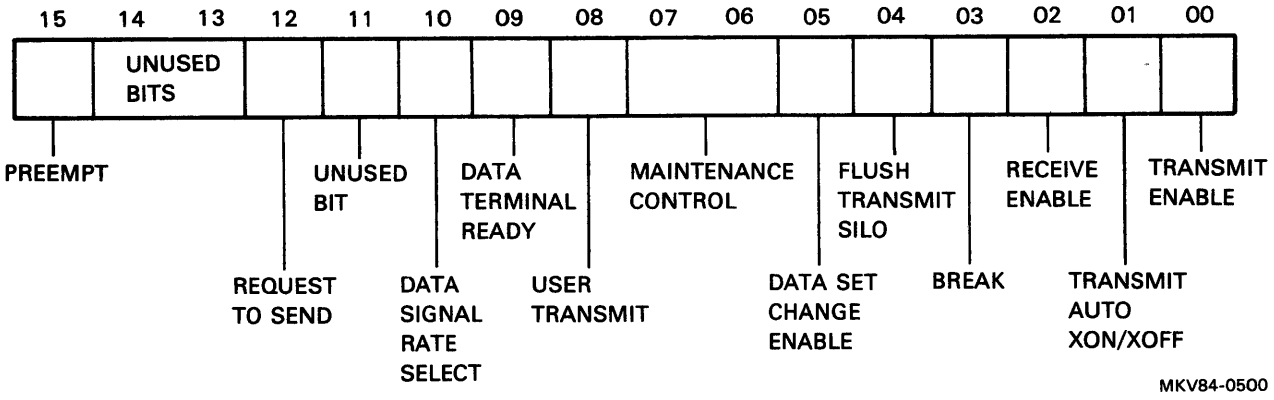


Figure 3-12 Indirect Register (IND.REG[1]<15:0>) Bit Map – Read/Write

Table 3-10 Indirect Register 1 Functions – Read/Write

Bits	Title	Function
<15:8>	Modem Transmit	These read/write bytes represent the transmit modem signals for the selected line. These bits are cleared by an INIT but not by a Master Reset. The modem signal lines always follow these bits.
<15>	Pre-empt	This bit is set by the program to pre-empt silo output. The user may then load the transmit character indirect register. The low byte that is loaded by the user will then be the next character to be transmitted. This allows the program to interrupt Programmed or DMA transmission to send a character (presumably an XON or XOFF) and then continue the Programmed or DMA transmission. When this process is performed, take note that there is no loss of characters or data. The pre-empt character is simply inserted into the effective transmit output stream of data. When indirect register 0 is loaded, this bit is automatically cleared. This bit is cleared by Master Reset or INIT.
<14:13>	Not Used	

Table 3-10 Indirect Register 1 Functions – Read/Write (Cont)

Bits	Title	Function
<12>	Request To Send	This bit controls the Request to Send line (EIA RS-232-C circuit CA) that is connected to the modem. When this bit is set, the Request To Send line is in the ON condition. When this bit is clear, the Request To Send line is in the OFF condition.
<11>	Not Used	
<10>	Data Signal Rate Select	This bit controls the Data Signal Rate Select line (EIA RS-232-C circuit CH) that is connected to the modem. When this bit is set, the Data Signal Rate Select line is in the ON condition. When this bit is clear, the Data Signal Rate Select line is in the OFF condition.
<9>	Data Terminal Ready	This bit controls the Data Terminal line (EIA RS-232-C circuit CD) that is connected to the modem. When this bit is set, the Data Terminal Ready line is in the ON condition. When this bit is clear, the Data Terminal Ready line is in the OFF condition.
<8>	User Transmit	This line is connected to pin 18 of the line's 25-pin RS-232-C connector on the distribution panel. This pin is an EIA RS-232-C unassigned pin. This line and the pin associated with it may be used for whatever purpose the user desires.
<7:0>	Line Control	These read/write bits are cleared by a Master Reset or INIT. These bits must be loaded with the appropriate information prior to using a line after a Master Reset has been generated.
<7:6>	Maintenance Control Function	These maintenance bits have the following meanings: 00 Normal Operation 01 Automatic Echo Mode In this mode of operation, data is put into the received silo and automatically retransmitted (regardless of the state of TX.ENA) at the same baud rate as the transmitter. RX.ENA must be set for this mode to work. Normal transmitter operation is not inhibited in this mode. 10 Internal Line Loopback In this mode of operation, the specific line's output is internally connected to the line's input (within the distribution panel). Received data is looped back. All modem signals are looped back when operating in this mode.

Table 3-10 Indirect Register 1 Functions – Read/Write (Cont)

Bits	Title	Function
		11 Shared RAM Loopback In this mode of operation, the specific line's output is internally connected to the line's input. All data and modem signals are looped back at the UBI - TIU interface (shared RAM).
<5>	Data Set Change Enable	When set, this bit enables the multiplexer to search for a transition in the modem receive signals for the selected line. When such a transition is found, the result is that the entry into the receive silo will have the Data Set Change bit set.
<4>	Flush TX Silo	The setting of this bit causes the transmit silo for the selected line to be flushed and DMA terminated. Disabling the transmitter does not cause the silo to be flushed. Disabling the transmitter simply inhibits character transmission. After the silo has been flushed, this bit is automatically cleared and TX.RDY is set.
<3>	Break	When this bit is set, the EIA Data line transmits spaces after the current character has finished being serialized. Transmission resumes after the break is cleared.
<2>	Receive Enable	When this bit is set, the receiver for the selected line is enabled. When this bit is clear, the receiver for the selected line is disabled. If receive enable is set to zero while a character is being assembled, the character is lost.
<1>	Tx Auto XON/XOFF	When this bit is set, the receipt of an XOFF causes the transmit enable bit to be reset. The receipt of an XON causes the bit to be set. The XON/XOFF character is put into the RX silo if the receiver is enabled.
<0>	Transmit Enable	When this bit is set, the transmitter for the selected line is enabled. When this bit is clear, the transmitter for the selected line is disabled. If transmit enable is cleared while a character is being transmitted, the disabling of the transmitter occurs after the complete character has been transmitted. Reception of an XON or XOFF character sets or resets this bit if IND.REG [1] <2> is set.

3.17 INDIRECT REGISTER (IND.REG[2]<15:0>) -READ/WRITE

The indirect register [2] has an address of Octet Base + 6. This read/write register is not cleared by a Master Reset or INIT. After a read or write to the buffer address register, OCTET.CSR<4:3> is automatically incremented to point to the respective line's DMA character count register.

The buffer address register is meaningful only if the respective line is in the DMA mode of operation. This register should be loaded with the lower 16 bits of the DMA buffer address for the respective line. Writing to this register while the DMA character count is nonzero will have unpredictable results.

Refer to the Figure 3-13 for the bit map of the indirect register (IND.REG[2]) and to Table 3-11 for the function of the bits contained in this register.

If a DMA error is encountered, the line will be taken out of DMA mode. The register will contain the address that caused the error.

This register may be accessed by an RMW cycle.

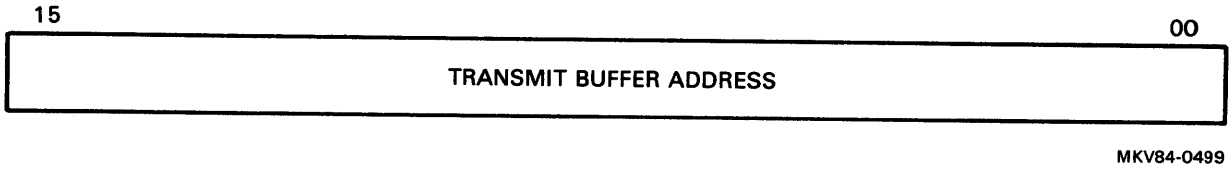


Figure 3-13 Indirect Register (IND.REG[2]<15:0>) Bit Map - Read/Write

Table 3-11 Indirect Register 2 Functions - Read/Write

Bits	Title	Function
<15:0>	Transmit Buffer Address	The lower 16 bits of the DMA buffer address

3.18 INDIRECT REGISTER (IND.REG[3]<15:0>) -READ/WRITE

The indirect register [3] has an address of Octet Base + 6. This read/write register contains the DMA character count and the upper two bits of the transmit buffer address. Writing to these registers initiates a DMA transfer. Refer to the Figure 3-14 for the bit map of indirect register (IND.REG[3]) and to Table 3-12 for the function of the bits contained in this register.

The DMA character count is cleared by a Master Reset or INIT. The two address bits are not cleared. If a DMA error is encountered, the DMA character count will be set to zero. Bits <15:14> will contain the UNIBUS address bit <17:16>, which caused the error.

This register may be accessed by an RMW cycle.

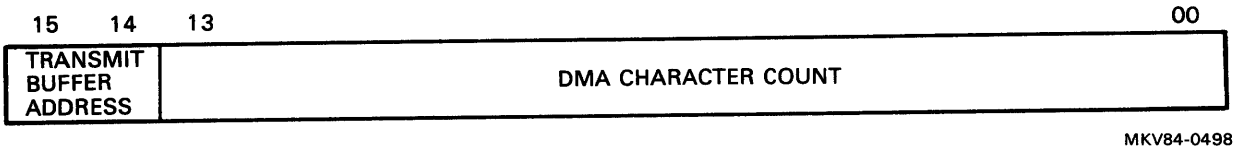


Figure 3-14 Indirect Register (IND.REG[3]<15:0>) Bit Map - Read/Write

Table 3-12 Indirect Register 3 Functions - Read/Write

Bits	Title	Function
<15:14>	Transmit Buffer Address	These bits contain the UNIBUS address bits <17:16>.
<13:0>	DMA Character Count	These bits contain the respective line's 14-bit character count.

NOTE

As characters are fetched by means of DMA cycles, the DMA character count is decremented. Writing to this register while the DMA character count is nonzero will have unpredictable results.

CHAPTER 4
SERVICE

4.1 INTRODUCTION

This chapter describes Field Replaceable Units (FRUs), preventive maintenance, self-test diagnostics, H3014 front panel indicators, and removal/replacement procedures.

4.2 DMZ32 FIELD REPLACEABLE UNITS

The DMZ32 is designed for ease of maintainability. Internal microdiagnostics and system diagnostics aid in isolating the fault to a specific FRU. The FRUs of the DMZ32 are as follows:

- UNIBUS interface module (M8398),
- H3014 processor module (29-24797-00),
- H3014 expansion module (29-24798-00),
- H3014 power supply assembly (29-24799-00),
- H3014 fan (29-24800-00),
- H3014 chassis with I/O panel (29-24796-00),
- 3.0 m (10 ft) internal cable (BC22N-10), and
- 4.6 m (15 ft) external cable (BC18L-15).

For the removal/replacement procedures for each of the FRUs, refer to Section 4.13.

4.3 PREVENTIVE MAINTENANCE

There is no scheduled preventive maintenance performed on the DMZ32. However, when system preventive maintenance is performed, check the following:

- The voltages on the DD11-DK backplane,
- The voltages on the processor module of the H3014 distribution panel,
- The voltages on the expansion module of the H3014 distribution panel, and
- The H3014 disribution panel fan operation.

DD11-DK Voltage Test Points

+5 V (CA2)
+15 V (CU1)

H3014 Voltage Test Points

Processor Module (Second Module) – Figure 4-1

TP14 (BLACK) = Ground
TP13 (RED) = +5 V
TP12 (BLUE) = +12 V
TP11 (WHITE) = −12 V

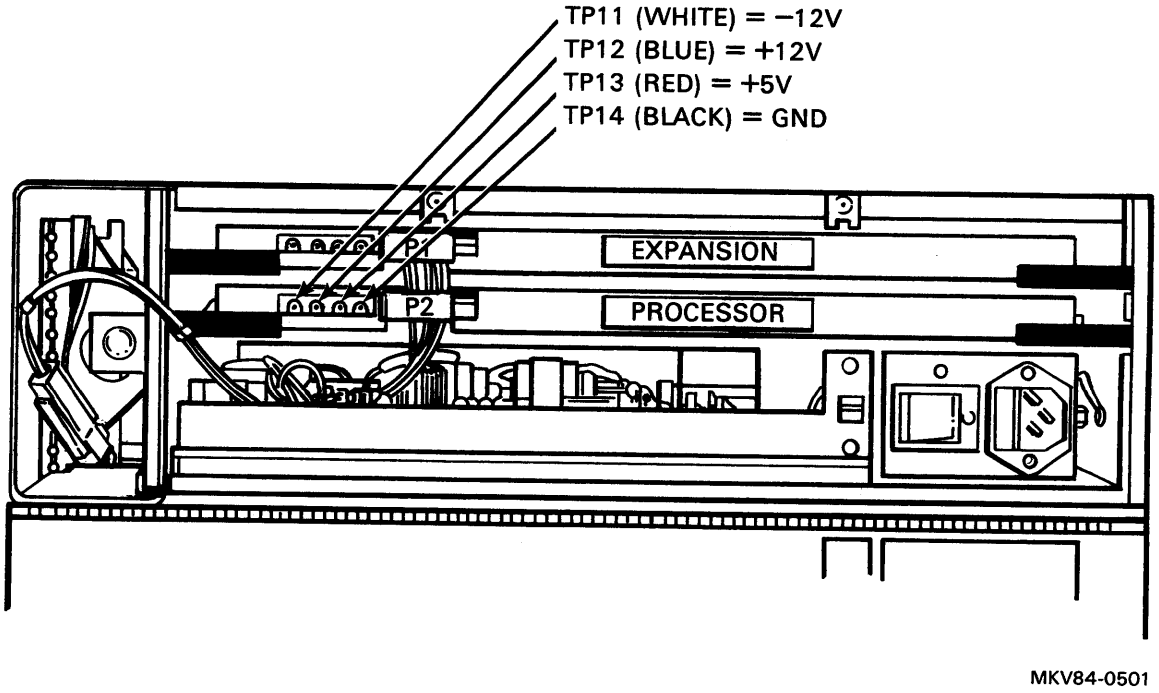


Figure 4-1 Processor Module Test Points

Expansion Module (Top Module) – Figure 4-2

TP14 (BLACK) = Ground
TP13 (RED) = +5 V
TP12 (BLUE) = +12 V
TP11 (WHITE) = −12 V

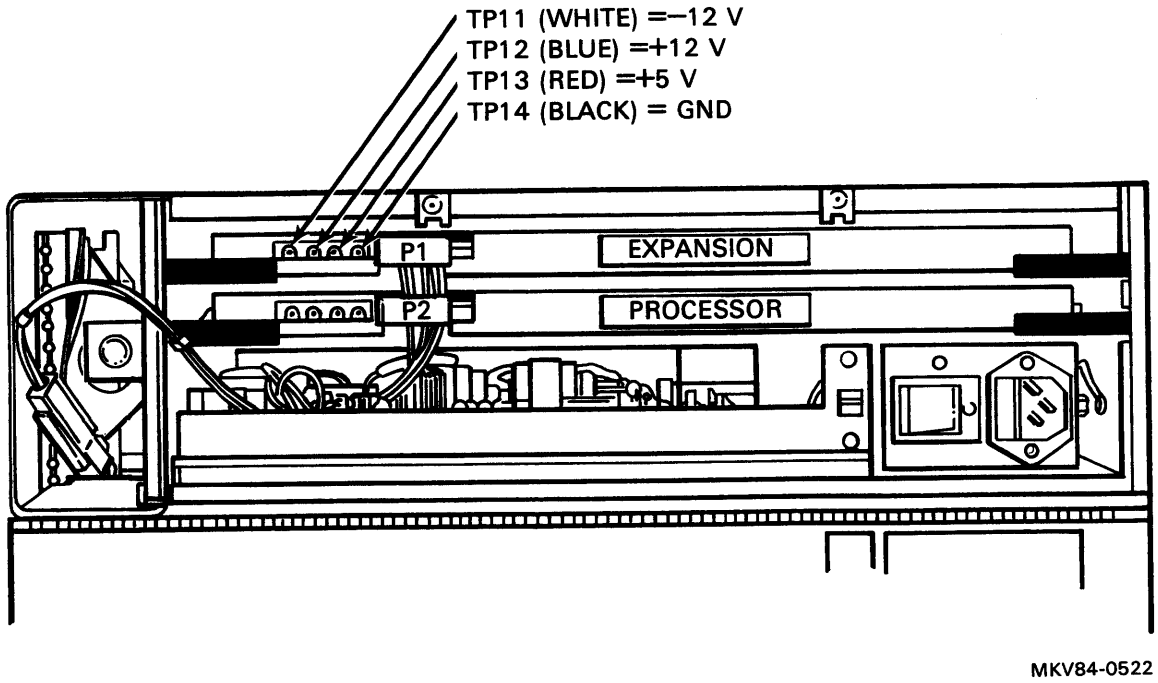


Figure 4-2 Expansion Module Test Points

Power Supply Assembly – Figure 4-3

TB1-1 TB1-2 TB1-3	–	Input Line Voltage
TB1-4	–	Not Used
TB1-5	–	−12 V
TB1-6	–	+12 V
TB1-7	–	Chassis Ground
TB1-8	–	+5 V

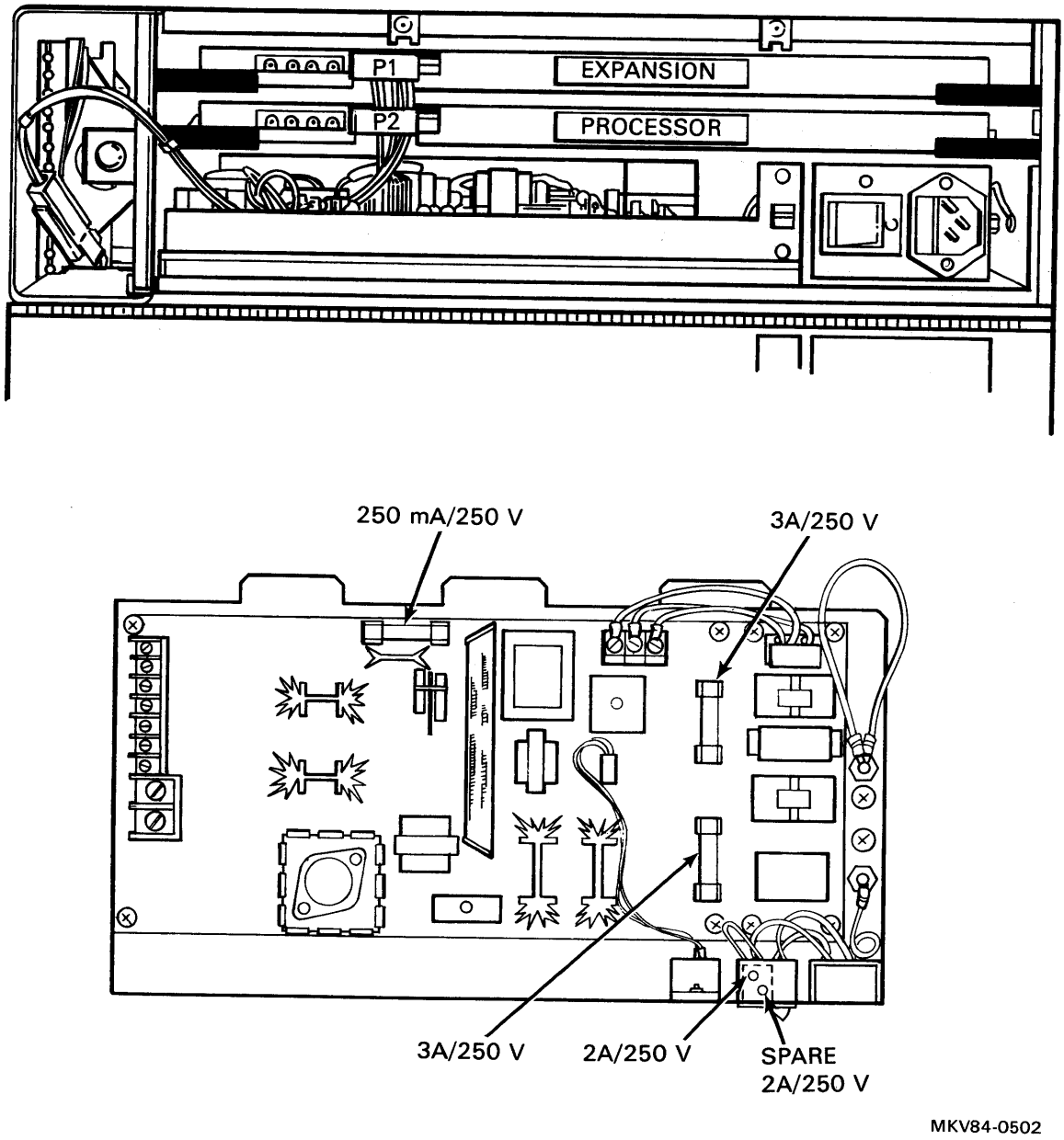


Figure 4-3 Power Supply Assembly Test Points

4.4 SELF-TEST DIAGNOSTIC

The self-test diagnostic for the DMZ32 is an on-board Read Only Memory (ROM) based microdiagnostic. The self-test diagnostic is executed during the following:

- Power-up,
- When the self-test pushbutton is pressed,
- At UNIBUS initialization, and
- When writing AA00 (HEX) to the diagnostic register.

The results of the ROM based microdiagnostics can be seen by reading the eight (8) Light-Emitting Diodes (LEDs) that are mounted on the M8398 module. Refer to Figure 4-4 for the proper orientation of how the LEDs are numbered. Refer to Table 4-1 for the LED coded display, the function tested when a display is seen, and the field replaceable unit that is faulty for each display.

When the self-test diagnostic is finished, and everything has passed the self-test, the LEDs cycle in a rotating pattern that repeats over and over. The pattern repeats from the MSB (LED 7) through the LSB (LED 0).

When all the microdiagnostics are successfully passed, the LEDs display a walking ones (1s) pattern. This is indicated by LEDs 7 through 0 flashing sequentially over a two (2) second time period. When completed, a binary number is displayed indicating the peak, 24-line receive character rate since the last peak character rate number was displayed. The binary number is displayed for approximately two seconds. After the two seconds, the first binary number is followed by a second binary number that displays the peak 24-line transmit character rate. This display also lasts for approximately two seconds. In both cases, the binary number displayed can be translated to peak characters per second by dividing by 2 and multiplying by 1000. For example, a binary number of 16 (00010000) translates to 8000 characters per second. The TX peak character rate number is then followed by the walking ones pattern again.

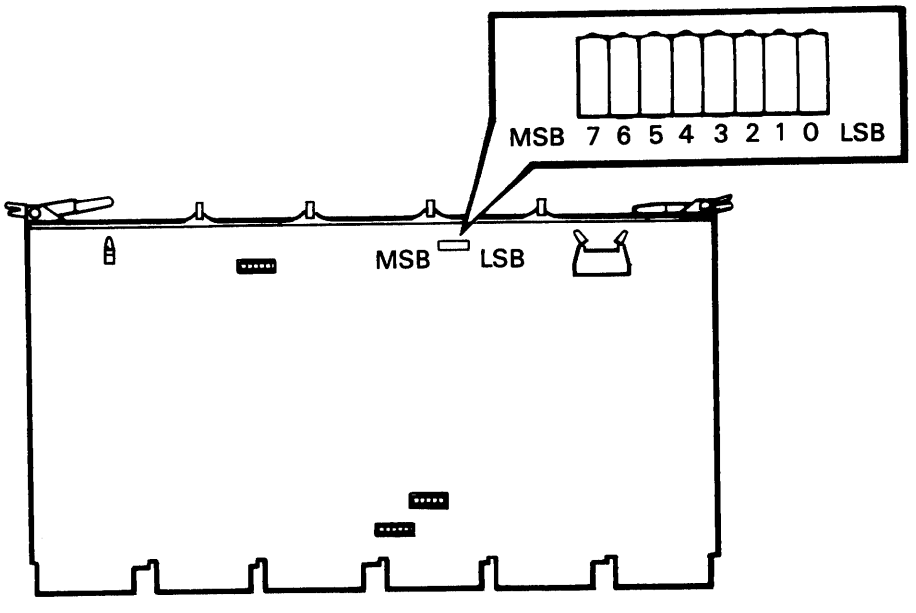


Figure 4-4 M8398 LEDs

Table 4-1 M8398 Coded LED Display

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
									Illegal Code	00	00	00
							●	M8398	Q Register Condition Code	01	01	01
						●		M8398	Working Registers 0-7	02	02	02
						●	●	M8398	Working Registers 8-18	03	03	03
					●			M8398	MSB of "A" & "B" Address of Working Register	04	04	04
					●		●	M8398	Subroutine calls (4 Levels)	05	05	05
					●	●		M8398	Set Negative Bit	06	06	06
					●	●	●	M8398	Set Carry Bit	07	07	07
				●				M8398	Clear N Bit, C Bit	08	08	10
				●			●	M8398	XOR Function, AUX Z Bit	09	09	11
				●		●		M8398	Rotate Left, Rotate Right WR & Q Register	0A	10	12
				●		●	●	M8398	Mask Function	0B	11	13
				●	●			M8398	Negate Function	0C	12	14
				●	●		●	M8398	Decrement Function	0D	13	15
				●	●	●		M8398	OR Function	0E	14	16
				●	●	●	●		- Not Used -	0F	15	17
			●						- Not Used -	10	16	20
			●				●		- Not Used -	11	17	21
			●			●			- Not Used -	12	18	22
			●			●	●	M8398	Shared RAM (Addressing)	13	19	23
			●		●			M8398	Shared RAM (Data)	14	20	24

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
			●		●		●	M8398	LS Addressing (1K Sections) EA PADR<1:>	15	21	25
			●		●	●		M8398	LS Addressing (.256K Blocks) COMF<24:25>	16	22	26
			●		●	●	●	M8398	LS Addressing (Direct Space) COMJ<23:16>	17	23	27
			●	●				M8398	LS Addressing (Process Space) PROC<2:0>	18	24	30
			●	●			●	M8398	LS Data Indirect LO Octet 0	19	25	31
			●	●		●		M8398	LS Data Indirect HI Octet 0	1A	26	32
			●	●		●	●	M8398	LS Data Indirect LO Octet 1	1B	27	33
			●	●	●			M8398	LS Data Indirect HI Octet 1	1C	28	34
			●	●	●		●	M8398	LS Data Indirect LO Octet 2	1D	29	35
			●	●	●	●		M8398	LS Data Indirect HI Octet 2	1E	30	36
			●	●	●	●	●	M8398	LS Data Indirect LO Maintenance Space	1F	31	37
		●						M8398	LS Data Indirect HI Maintenance Space	20	32	40
		●					●	M8398	Starting DMA Tests	21	33	41
		●				●		M8398	Slave Sync Time-Out During DMA DATO	22	34	42
			●			●	●	M8398	Data Compare Error On DMA DATO	23	35	43

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
		●			●			M8398	Slave Sync Time-Out On DMA DATI	24	36	44
		●			●		●	M8398	Data Compare Error On DMA DATI	25	37	45
		●			●	●		M8398	Failed To Become Master On DATO or DATI	26	38	46
		●			●	●	●		- Reserved -	27	39	47
		●		●				M8398	Starting TIU Self-Test	28	40	50
		●		●			●	M8398	TIU 2901	29	41	51
		●		●		●		M8398	TIU 2901	2A	42	52
		●		●		●	●	M8398	TIU 2901	2B	43	53
		●		●	●			M8398	TIU Shared RAM	2C	44	54
		●		●	●		●	M8398	TIU Micro-Sequencer	2D	45	55
		●		●	●	●		M8398	TIU Micro-Sequencer	2E	46	56
		●		●	●	●	●	M8398	TIU Micro-Sequencer	2F	47	57
		●	●					M8398	TIU Local Store	30	48	60
		●	●				●	M8398	TIU Local Store	31	49	61
		●	●			●		M8398	TIU T1 Interface	32	50	62
		●	●			●	●	M8398	TIU T1 Interface	33	51	63
		●	●		●			M8398	TIU A23 Channel	34	52	64
		●	●		●		●	M8398	T1 Link Synchronization Failure	35	53	65
		●	●		●	●			- Reserved -	36	54	66
		●	●		●	●	●		- Reserved -	37	55	67
		●	●	●					- Reserved -	38	56	70

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
		●	●	●			●		- Reserved -	39	57	71
		●	●	●		●			- Reserved -	3A	58	72
		●	●	●		●	●		- Reserved -	3B	59	73
		●	●	●	●				- Reserved -	3C	60	74
		●	●	●	●		●		- Reserved -	3D	61	75
		●	●	●	●	●			- Reserved -	3E	62	76
		●	●	●	●	●	●		- Reserved -	3F	63	77
	●							M8398	Internal Local T1 Data Path [Octet 0, Line 0]	40	64	100
	●						●	M8398	Internal Local T1 Data Path [Octet 0, Line 1]	41	65	101
	●					●		M8398	Internal Local T1 Data Path [Octet 0, Line 2]	42	66	102
	●					●	●	M8398	Internal Local T1 Data Path [Octet 0, Line 3]	43	67	103
	●				●			M8398	Internal Local T1 Data Path [Octet 0, Line 4]	44	68	104
	●				●		●	M8398	Internal Local T1 Data Path [Octet 0, Line 5]	45	69	105
	●				●	●		M8398	Internal Local T1 Data Path [Octet 0, Line 6]	46	70	106
	●				●	●	●	M8398	Internal Local T1 Data Path [Octet 0, Line 7]	47	71	107
	●			●				M8398	Internal Local T1 Data Path [Octet 1, Line 0]	48	72	110
	●			●			●	M8398	Internal Local T1 Data Path [Octet 1, Line 1]	49	73	111

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
	●			●		●		M8398	Internal Local T1 Data Path [Octet 1, Line 2]	4A	74	112
	●			●		●	●	M8398	Internal Local T1 Data Path [Octet 1, Line 3]	4B	75	113
	●			●	●			M8398	Internal Local T1 Data Path [Octet 1, Line 4]	4C	76	114
	●			●	●		●	M8398	Internal Local T1 Data Path [Octet 1, Line 5]	4D	77	115
	●			●	●	●		M8398	Internal Local T1 Data Path [Octet 1, Line 6]	4E	78	116
	●			●	●	●	●	M8398	Internal Local T1 Data Path [Octet 1, Line 7]	4F	79	117
	●		●					M8398	Internal Local T1 Data Path [Octet 2, Line 0]	50	80	120
	●		●				●	M8398	Internal Local T1 Data Path [Octet 2, Line 1]	51	81	121
	●		●			●		M8398	Internal Local T1 Data Path [Octet 2, Line 2]	52	82	122
	●		●			●	●	M8398	Internal Local T1 Data Path [Octet 2, Line 3]	53	83	123
	●		●		●			M8398	Internal Local T1 Data Path [Octet 2, Line 4]	54	84	124
	●		●		●		●	M8398	Internal Local T1 Data Path [Octet 2, Line 5]	55	85	125
	●		●		●	●		M8398	Internal Local T1 Data Path [Octet 2, Line 6]	56	86	126
	●		●		●	●	●	M8398	Internal Local T1 Data Path [Octet 2, Line 7]	57	87	127
	●		●	●				M8398	Manual T1 Connector Data Path [Octet 0, Line 0]	58	88	130

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
	●		●	●			●	M8398	Manual T1 Connector Data Path [Octet 0, Line 1]	59	89	131
	●		●	●		●		M8398	Manual T1 Connector Data Path [Octet 0, Line 2]	5A	90	132
	●		●	●		●	●	M8398	Manual T1 Connector Data Path [Octet 0, Line 3]	5B	91	133
	●		●	●	●			M8398	Manual T1 Connector Data Path [Octet 0, Line 4]	5C	92	134
	●		●	●	●		●	M8398	Manual T1 Connector Data Path [Octet 0, Line 5]	5D	93	135
	●		●	●	●	●		M8398	Manual T1 Connector Data Path [Octet 0, Line 6]	5E	94	136
	●		●	●	●	●	●	M8398	Manual T1 Connector Data Path [Octet 0, Line 7]	5F	95	137
	●	●						M8398	Manual T1 Connector Data Path [Octet 1, Line 0]	60	96	140
	●	●					●	M8398	Manual T1 Connector Data Path [Octet 1, Line 1]	61	97	141
	●	●				●		M8398	Manual T1 Connector Data Path [Octet 1, Line 2]	62	98	142
	●	●				●	●	M8398	Manual T1 Connector Data Path [Octet 1, Line 3]	63	99	143
	●	●			●			M8398	Manual T1 Connector Data Path [Octet 1, Line 4]	64	100	144
	●	●			●		●	M8398	Manual T1 Connector Data Path [Octet 1, Line 5]	65	101	145
	●	●			●	●		M8398	Manual T1 Connector Data Path [Octet 1, Line 6]	66	102	146
	●	●			●	●	●	M8398	Manual T1 Connector Data Path [Octet 1, Line 7]	67	103	147

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
	●	●		●				M8398	Manual T1 Connector Data Path [Octet 2, Line 0]	68	104	150
	●	●		●			●	M8398	Manual T1 Connector Data Path [Octet 2, Line 1]	69	105	151
	●	●		●		●		M8398	Manual T1 Connector Data Path [Octet 2, Line 2]	6A	106	152
	●	●		●		●	●	M8398	Manual T1 Connector Data Path [Octet 2, Line 3]	6B	107	153
	●	●		●	●			M8398	Manual T1 Connector Data Path [Octet 2, Line 4]	6C	108	154
	●	●		●	●		●	M8398	Manual T1 Connector Data Path [Octet 2, Line 5]	6D	109	155
	●	●		●	●	●		M8398	Manual T1 Connector Data Path [Octet 2, Line 6]	6E	110	156
	●	●		●	●	●	●	M8398	Manual T1 Connector Data Path [Octet 2, Line 7]	6F	111	157
	●	●	●						- NOT USED -	70	112	160
	●	●	●				●		- NOT USED -	71	113	161
	●	●	●			●			- NOT USED -	72	114	162
	●	●	●			●	●		- NOT USED -	73	115	163
	●	●	●		●				- NOT USED -	74	116	164
	●	●	●		●		●		- NOT USED -	75	117	165
	●	●	●		●	●			- NOT USED -	76	118	166
	●	●	●		●	●	●		- NOT USED -	77	119	167
	●	●	●	●					- NOT USED -	78	120	170
	●	●	●	●			●		- NOT USED -	79	121	171
	●	●	●	●		●			- NOT USED -	7A	122	172

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
	●	●	●	●		●	●		- NOT USED -	7B	123	173
	●	●	●	●	●				- NOT USED -	7C	124	174
	●	●	●	●	●		●		- NOT USED -	7D	125	175
	●	●	●	●	●	●			- NOT USED -	7E	126	176
	●	●	●	●	●	●	●	H3014 Processor	H3014 Self-Test Failure	7F	127	177
●								H3014 Processor	Internal EIA Data Path [Octet 0, Line 0]	80	128	200
●							●	H3014 Processor	Internal EIA Data Path [Octet 0, Line 1]	81	129	201
●						●		H3014 Processor	Internal EIA Data Path [Octet 0, Line 2]	82	130	202
●						●	●	H3014 Processor	Internal EIA Data Path [Octet 0, Line 3]	83	131	203
●					●			H3014 Processor	Internal EIA Data Path [Octet 0, Line 4]	84	132	204
●					●		●	H3014 Processor	Internal EIA Data Path [Octet 0, Line 5]	85	133	205
●					●	●		H3014 Processor	Internal EIA Data Path [Octet 0, Line 6]	86	134	206
●					●	●	●	H3014 Processor	Internal EIA Data Path [Octet 0, Line 7]	87	135	207
●				●				H3014 Processor	Internal EIA Data Path [Octet 1, Line 0]	88	136	210
●				●			●	H3014 Processor	Internal EIA Data Path [Octet 1, Line 1]	89	137	211
●				●		●		H3014 Processor	Internal EIA Data Path [Octet 1, Line 2]	8A	138	212

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDs								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
●				●		●	●	H3014 Processor	Internal EIA Data Path [Octet 1, Line 3]	8B	139	213
●				●	●			H3014 Processor	Internal EIA Data Path [Octet 1, Line 4]	8C	140	214
●				●	●		●	H3014 Processor	Internal EIA Data Path [Octet 1, Line 5]	8D	141	215
●				●	●	●		H3014 Processor	Internal EIA Data Path [Octet 1, Line 6]	8E	142	216
●				●	●	●	●	H3014 Processor	Internal EIA Data Path [Octet 1, Line 7]	8F	143	217
●			●					H3014 Processor	Internal EIA Data Path [Octet 2, Line 0]	90	144	220
●			●				●	H3014 Processor	Internal EIA Data Path [Octet 2, Line 1]	91	145	221
●			●			●		H3014 Processor	Internal EIA Data Path [Octet 2, Line 2]	92	146	222
●			●			●	●	H3014 Processor	Internal EIA Data Path [Octet 2, Line 3]	93	147	223
●			●		●			H3014 Processor	Internal EIA Data Path [Octet 2, Line 4]	94	148	224
●			●		●		●	H3014 Processor	Internal EIA Data Path [Octet 2, Line 5]	95	149	225
●			●		●	●		H3014 Processor	Internal EIA Data Path [Octet 2, Line 6]	96	150	226
●			●		●	●	●	H3014 Processor	Internal EIA Data Path [Octet 2, Line 7]	97	151	227

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Table 4-1 M8398 Coded LED Display (Cont)

M8398 LEDS								Function Tested		Diagnostic LEDs		
7	6	5	4	3	2	1	0	FRU	Description	Hex	Decimal	Octal
•			•	•					– Illegal Codes – UBI or TIU Failure	98	152	230
			•						•	•	•	•
			•						•	•	•	•
			(through)						(through)		(through)	
			•						•	•	•	•
			•						•	•	•	•
•	•	•	•	•	•	•	•		– Illegal Codes – UBI or TIU Failure	FF	255	377

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4.5 DIAGNOSTICS

This section describes the use of DMZ32 diagnostics. The DMZ32 is supported by both Level 3 and Level 2R diagnostics. The Level 3 diagnostic is a standalone diagnostic that runs under the Diagnostic Supervisor using direct I/O. EVDAE is the only Level 3 diagnostic. The purpose of EVDAE is to verify the functionality of the DMZ32.

Various loopback methods are used to isolate the fault to a specific component of the DMZ32. The different loopback methods used during the running of the EVDAE are either software controlled or manually inserted.

The Level 2R diagnostic enables Field Service to fault isolate to the option level while running under VMS. The Level 2R diagnostic, run under the Diagnostic Supervisor, uses the QIO interface of the VMS device driver. EVDAF is the only Level 2R diagnostic.

4.6 DIAGNOSTIC SUPERVISOR

Both Level 3 and Level 2R diagnostics run under the Diagnostic Supervisor. Loading and using the Diagnostic Supervisor are described in both the *VAX-11/730 Diagnostic System Overview Manual* (EK-DS730-UG) and the *VAX Diagnostic System User's Guide* (EK-VX11D-UG)

4.7 DMZ32 CSR ADDRESS AND VECTOR ADDRESS

The DMZ32 CSR address (760440) is used only as an example address in the following diagnostic procedures. The actual address depends on the switch setting of E-53 on the M8398 module. The vector is software controlled. (Refer to Appendix A for floating device addresses and vectors.)

4.8 MANUALLY CONTROLLED (HARDWARE) LOOPBACK METHODS

There are five manually controlled loopback methods that are used in running the DMZ32 diagnostics. These loopbacks require that a turnaround device be placed on the line(s) or that the local modem be manually put in a loopback mode of operation. The manually controlled loopback methods used with the DMZ32 are as follows:

- Local T1 loopback (H3028),
- Remote T1 loopback (H3027),
- Single line EIA loopback (H3248),
- Staggered multiline loopback (29-24929-00), and
- Manual analog modem loopback.

4.8.1 Local T1 Loopback (H3028)

The local T1 loopback test is conducted by Field Service personnel using the H3028 turnaround connector (Figure 4-5). The H3028 turnaround connector is inserted at J1 on the M8398 module. When the H3028 is inserted in J1 of the M8398 module, the T1 circuitry up to and including the analog I/O of the M8398 module is checked for proper operation.

This loopback is supported by EVDAE with event flag 3 set.

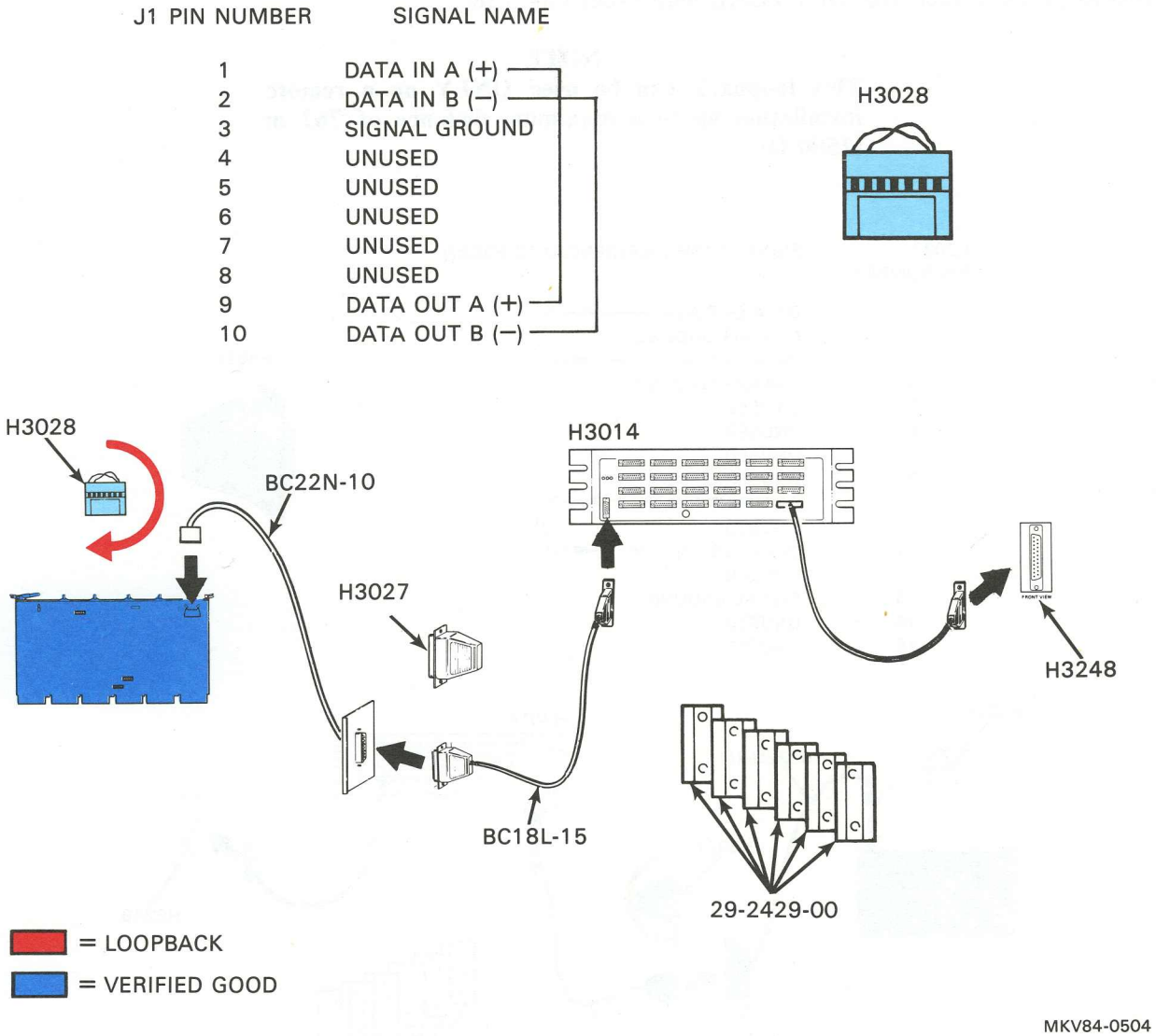


Figure 4-5 H3028 Loopback Connector

4.8.2 Remote T1 Loopback (H3027)

The remote T1 loopback test is conducted by Field Service personnel using the H3027 turnaround connector (Figure 4-6). The H3027 turnaround connector is inserted at either the I/O bulkhead or at the distribution panel end of the interconnecting cable between the M8398 module and the distribution panel. When inserted into the I/O panel insert connector (BC22N-10), the M8398 module and the internal interconnecting T1 cable are checked for proper operation. When the turnaround connector is connected to the distribution panel end of the T1 cable, the T1 cable (BC18L-15) is also checked for proper operation.

This loopback is supported by EVDAE with event flag 3 set.

NOTE

This loopback can be used ONLY on a remote installation up to a maximum distance of 762 m (2500 ft).

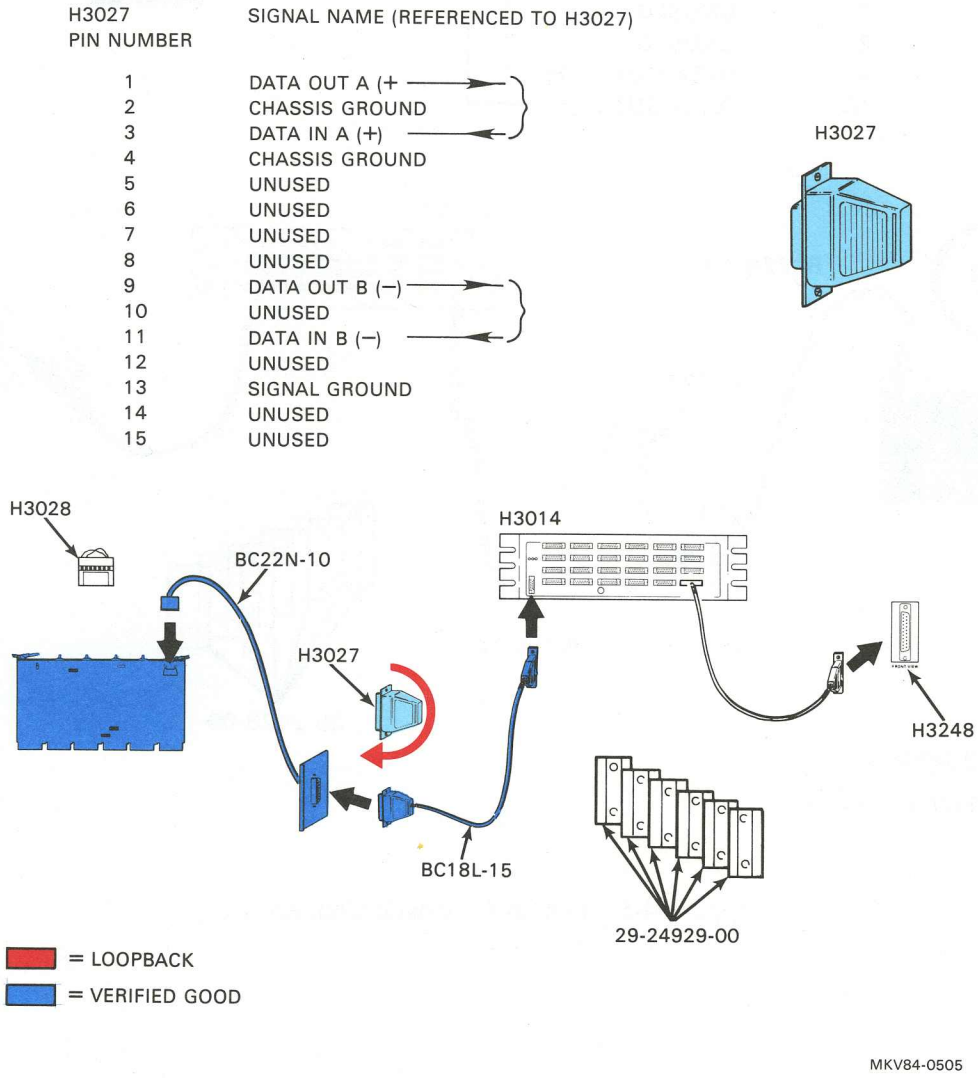


Figure 4-6 H3027 Loopback Connector

4.8.3 Single Line EIA Loopback (H3248)

The single line EIA loopback test is conducted by Field Service personnel using the H3248 turnaround connector (Figure 4-7), which is supplied in the CD Kit (A2-WO707-10). The H3248 turnaround connector is inserted either at the H3014 RS-232-C connector or at the EIA cable, which connects to the modem. When the H3248 is connected to the suspect channel (directly on the remote distribution panel), the connector, line drivers, receive/latches, and all modem signals for that channel are checked for proper operation. When the H3248 turnaround connector is connected to the EIA cable associated with the channel, the EIA cable is also checked for proper operation.

This loopback is supported by EVDAE with event flag 5 set and EVDAF loopback type 5 selected in the attach sequence.

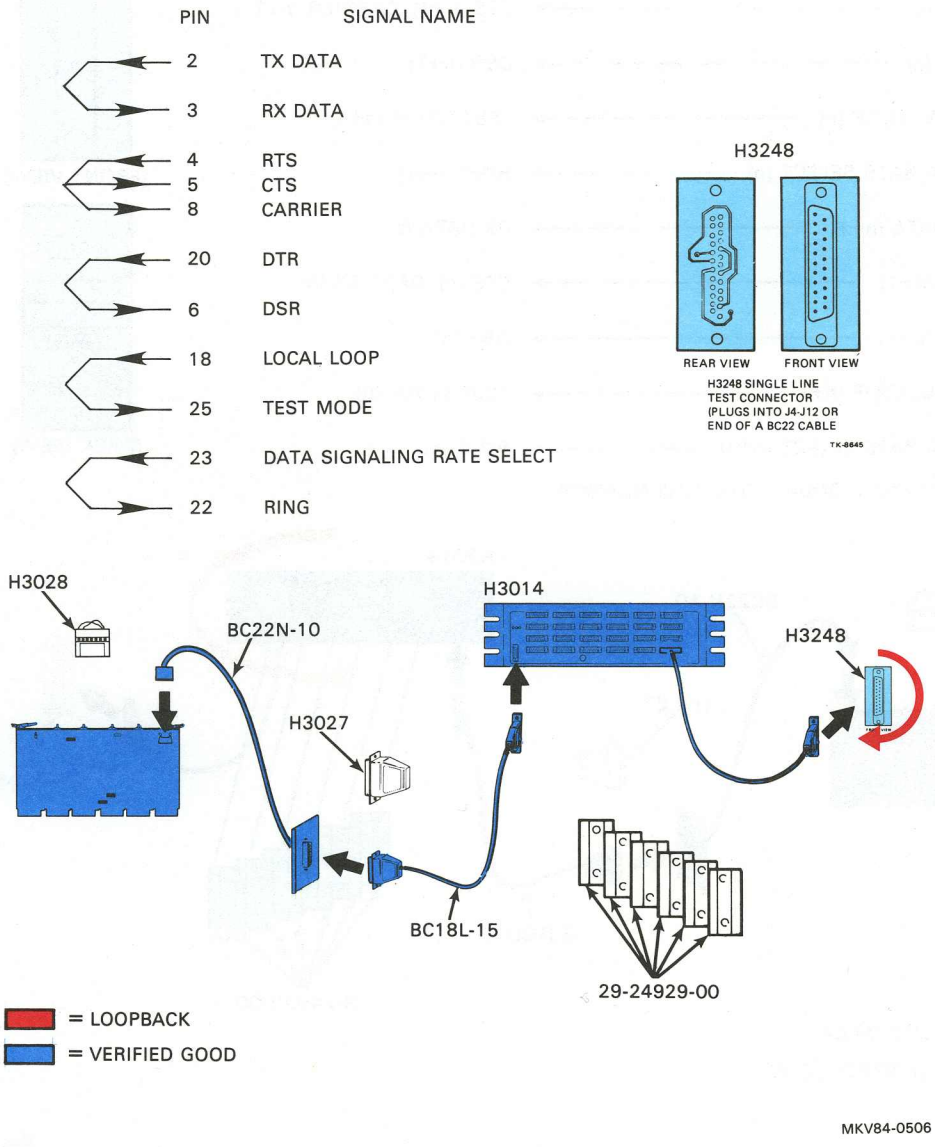


Figure 4-7 H3248 Turnaround Connector

4.8.4 Staggered Multiline Loopback (29-24929-00)

The staggered multiline loopback test is conducted by Field Service personnel using six (6) 29-24929-00 (Figure 4-8) turnaround connectors, which are supplied in the CD Kit (A2-WO707-10). The 29-24929-00 turnaround connectors are attached to the distribution panel so that all connectors have a loopback attached. When connected, this test checks for line interaction and asynchronous line problems.

This loopback is supported by EVDAE with event flag 6 set. Tests 35 through 41 of EVDAE are run when this connector is used.

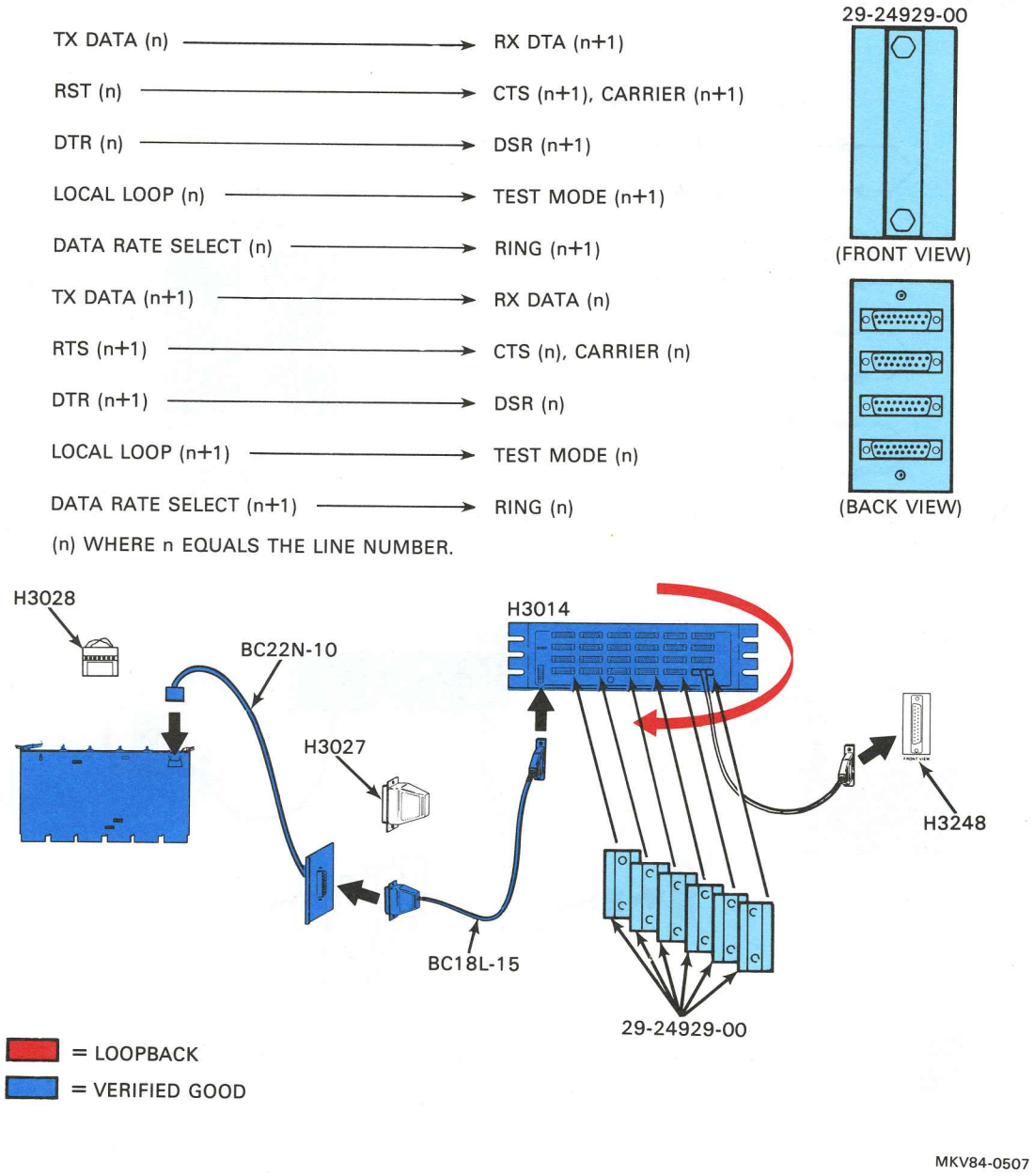


Figure 4-8 29-24929-00 Staggered Loopback Connector

4.8.5 Manual Analog Modem Loopback

The manual analog modem loopback test is conducted by Field Service personnel by pressing the analog loopback button (AL) on the modem (Figure 4-9). This loopback verifies that data can be sent to and received from the local modem.

This loopback is supported by EVDAE with event flag 7 set, and EVDAF with loopback type 7 selected in the attach sequence.

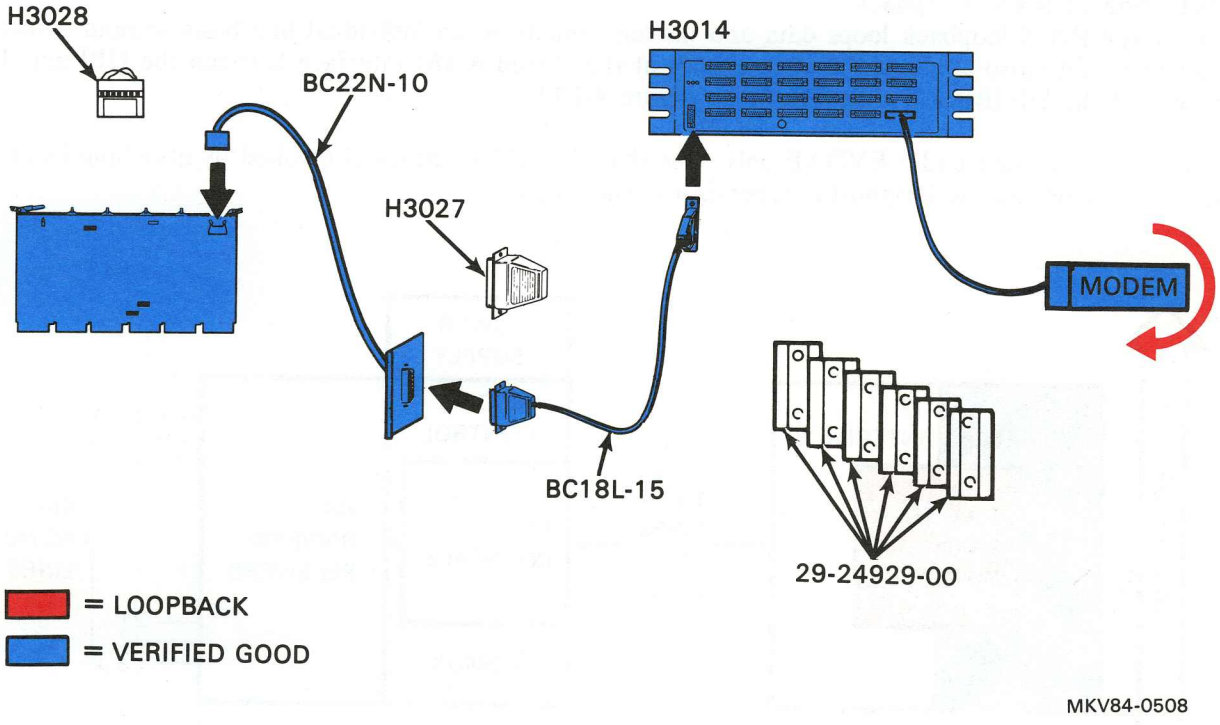


Figure 4-9 Manual Analog Modem Loopback

4.9 SOFTWARE LOOPBACK METHODS

There are many loopback methods that can be used in running the DMZ32 diagnostics. The software loopback methods that are used with the DMZ32 are as follows:

- Shared RAM loopback,
- Local trunk loopback,
- Internal single-line loopback, and
- Programmable local modem loopback.

4.9.1 Shared RAM Loopback

The shared RAM loopback loops data and modem signals on an individual line basis without affecting other lines. This also applies to modem signals at the shared RAM interface between the UBI and TIU sections of the UNIBUS module. (Refer to Figure 4-10.)

This loopback is used under EVDAE only. The shared RAM loopback is invoked by attaching loopback type 1 or by setting the Diagnostic Supervisor event flag 1.

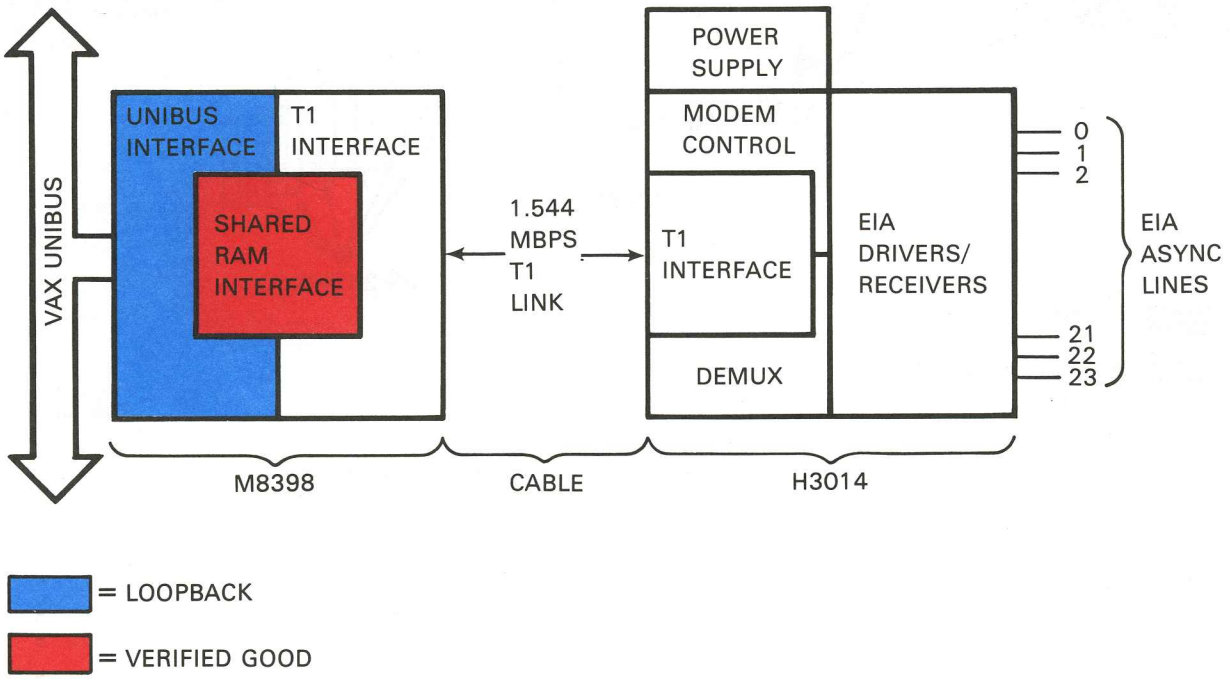


Figure 4-10 Shared RAM Loopback Test

4.9.2 Local Trunk Loopback

The local trunk loopback loops data back before the T1 driver/receiver on the M8398 module. (Refer to Figure 4-11.)

This loopback is supported by EVDAE and the microdiagnostics. The local trunk loopback is invoked by attaching loopback type 2 or by setting Diagnostic Supervisor event flag 2.

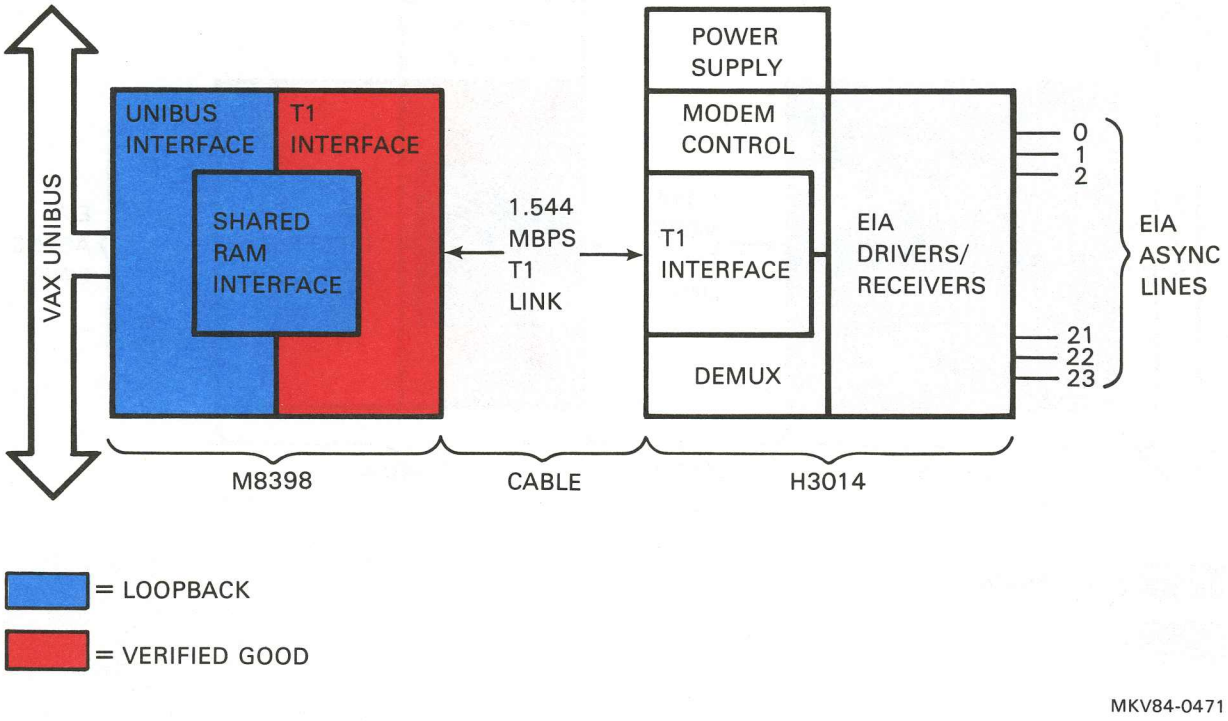


Figure 4-11 Local Trunk Loopback Test

4.9.3 Internal Single-line or All Lines Loopback

The single-line loopback is associated with the channel being tested. (Refer to Figure 4-12.) A message is sent, one line at a time, on all lines selected. EIA latches, drivers, and receivers are not tested with this loopback.

This loopback is used by EVDAE with event flag 4 set, and EVDAF with loopback type 4 selected in the attach sequence.

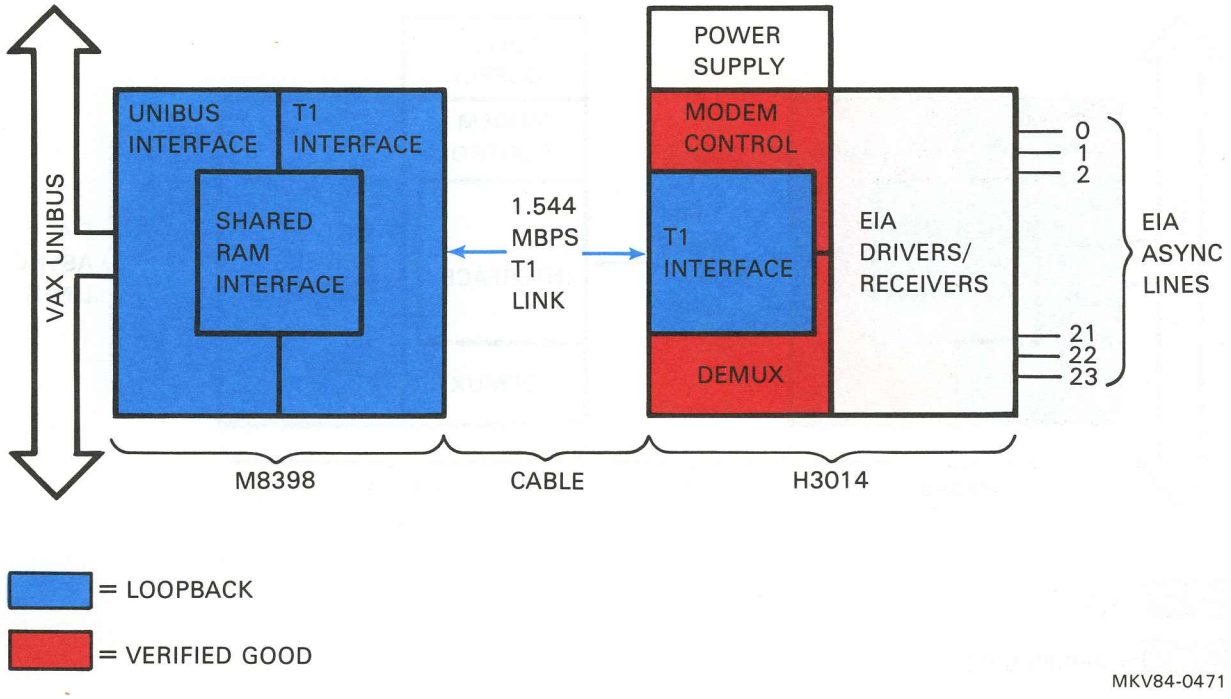


Figure 4-12 Single Line Loopback Test

4.9.4 Programmable Local Modem Loopback

NOTE

This loopback works only with a modem that supports programmable local loopback.

The programmable local modem loopback verifies the DMZ32 modem signals and will be executed if the programmable local modem loopback is selected in the supervisor attach sequence and if the modem control is available. (Refer to Figure 4-13.)

This loopback is supported by EVDAE with event flag 8 set, and EVDAF with loopback type 8 selected in the attach sequence.

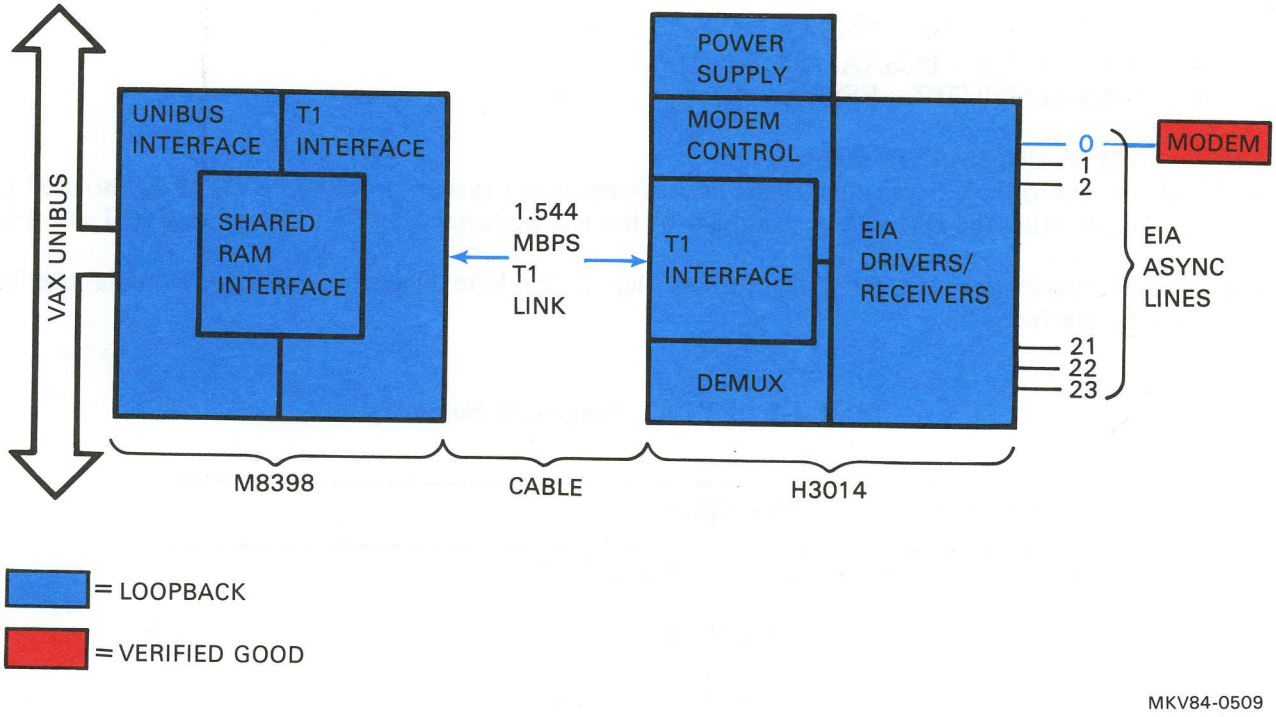


Figure 4-13 Analog Modem Loopback Test

4.10 DMZ32 LEVEL 3 (EVDAE) DIAGNOSTIC

There is only one Level 3 Diagnostic used to support the DMZ32, EVDAE. This diagnostic operates under the VAX Diagnostic Supervisor (VDS).

4.10.1 EVDAE Hardware Prerequisites

The following must be functional before the Level 3 diagnostic may be used:

- VAX-11 CPU,
- Memory (512K bytes), and
- UNIBUS adapter.

4.10.2 EVDAE Software Diagnostic Requirements

The Level 3 Diagnostic (EVDAE) requires VAX Diagnostic Supervisor 7.0 or later. The different VAX Diagnostic Supervisors are as follows:

- VAX-11/725/730 - ENSAA,
- VAX-11/750 - ECSAA, and
- VAX-11/780/782 - ESSAA.

4.10.3 EVDAE Diagnostic Description

EVDAE is an aid to Field Service personnel in verifying proper system operation. EVDAE is also used to aid in troubleshooting the DMZ32. A summary of the test performed by EVDAE is listed in Table 4-2.

The manual intervention test (test 42) verifies that a 256-byte block, or multiple, of data can be transmitted error-free.

Table 4-2 EVDAE Diagnostic Summary

Test Number	Description
1	Register Access Test
2	CSR Bit Test
3	Indirect Space Access
4	Master Reset Line Control & TX Modem Register
5	Master Reset Octet CSR
6	Line Parameter
7	TX Silo Count Master Reset
8	UNIBUS INIT
9	Flush Silo Test
10	TX Ready, TX Enable, and TX Silo Count

Table 4-2 EVDAE Diagnostic Summary (Cont)

Test Number	Description
11	RX Data Available & Master Reset
12	Data Loopback
13	TX Enable/Disable
14	Character Length
15	Load Word Test
16	Transmit Interrupt
17	Receive Interrupt
18	Receive Interrupt at 64 Characters
19	Multiple Interrupt
20	NPR-Nonexistent Memory
21	DMA Transfer (NO AUTO - INC)
22	DMA Transfer (AUTO - INC)
23	DMA Transfer, Unaligned Address
24	DMA Transfer (Memory Extension)
25	Receive Silo Alarm Time-out
26	TX Break Test
27	Receive Silo Overrun
28	Pre-empt
29	Interaction Test
30	Dynamic Baud Rate
31	Dynamic Word Length
32	Dynamic Parity
33	TX & RX Modem Signals (H3248)

Table 4-2 EVDAE Diagnostic Summary (Cont)

Test Number	Description
34	Data Test – Single Line (H3248) or Modem
35	XON/XOFF (Staggered)
36	Framing Error (Staggered)
37	Parity Error (Staggered)
38	Auto Echo Mode (Staggered)
39	RX & TX Modem (Staggered)
40	Data Set Change (Staggered)
41	Split Baud Rate (Staggered)
42	Manual Section

NOTE

To perform Tests 35 through 41, 29-29249-00 loop-back connectors must be installed on the distribution panel.

4.10.4 Loading, Attaching, and Running EVDAE

After the Diagnostic Supervisor is loaded, the operating instructions in Figure 4-14 can be used for the EVDAE diagnostic. The colored portions are what the user enters into the system.

EVDAE uses the standard VDS input sequence for attaching the UNIBUS adapter and loading the program. The user must select the lines to be tested, the baud rate to be used in external testing, and the loopback type.

On-line help may be obtained by typing HELP EVDAE.

```
DIAGNOSTIC SUPERVISOR.   ZZ-EXSAA-7.0-YYY    8-FEB-1983 09:40:14.80

DS> ATT DW780 SBI DWO 3 4     ; FOR VAX/780 ATTACH THE UBA ON THE SBI
       OR
DS> ATT DW750 HUB DWO         ; FOR VAX/750 TESTING
       OR
DS> ATT DW730 HUB DWO         ; FOR VAX/730 TESTING

DS> LOAD EVDAE                ; LOAD THE DMZ32 DIAGNOSTIC

DS> ATT DMZ32                 ; ATTACH THE DMZ32

DEVICE LINK? DWO              ; THE DMZ32 IS LINKED TO THE UBA

DEVICE NAME? TZA              ; THE GENERIC NAME FOR DMZ32 UNIT 1


CSR? 760440                   ; THE CSR ADRS IS 760440
                              ; (RANGE=760000-777776)

VECTOR? 300                   ; VECTOR ADRS IS 300 (RANGE=300-776)

BR? 5                         ; BR INTERRUPT LEVEL IS 5 (RANGE=5-6)

TEST LINES(OCTET0)? 377       ; LINES 0-7 OF OCTET 0 WILL BE TESTED

LEVEL 3 ONLY - TEST LINES(OCTET1)? 1

                              ; LINE 0 OF OCTET 1 WILL BE TESTED

LEVEL 3 ONLY - TEST LINES(OCTET2)? 200

                              ; LINE 7 OF OCTET 2 WILL BE TESTED

                              ; (OCTAL BIT MAP OF DESIRED LINES TO
                              ; TEST, BIT0 = LINE 0,
                              ;       BIT1 = LINE 1, ETC.
                              ;       RANGE = 000-377)
                              ; EXAMPLE: TEST LINES? 123
                              ; TEST LINES SIX, FOUR, ONE AND ZERO

BAUD RATE? 300                ; BAUD RATE TO BE USED IN TEST 34
                              ; MANUAL TEST.
                              ; BAUD RATES THAT CAN BE SELECT
                              ; ARE, 50, 75, 110, 135, 150, 300,
                              ; 600, 1200, 1800, 2000, 2400,
                              ; 4800, 9600, 19200
```

Figure 4-14 Loading, Attaching, and Running EVDAE (Sheet 1 of 2)

```
LOOPBACK TYPE?  6           ; Ø = INTERNAL (AUTO)
                            ; 1 = SHARED RAM
                            ; 2 = LOCAL T1 TRUNK
                            ; 3 = MANUAL T1 CONNECTION

                            ; 4 = INTERNAL LINE
                            ; 5 = SINGLE LINE - H3248 CONNECTOR
                            ; 6 = STAGGERED CONNECTOR
                            ; 7 = LOCAL MODE (MANUAL ANALOG LOOPBACK)
                            ; 8 = PROGRAMMABLE LOCAL MODEM

MODEM CONTROL?  Y           ; YES = H3Ø14 CONTAINS MODEM OPTION
                            ; (EXPANSION MODULE)
                            ; NO = DATA ONLY

DS> SELECT TZA              ; SELECT SPECIFIC DMZ32 TO BE RUN.
DS> START
```

Figure 4-14 Loading, Attaching, and Running EVDAE (Sheet 2 of 2)

4.10.5 EVDAE Event Flags

The loopback type is also selected by setting the appropriate event flag. Only ONE event flag is to be set at a time. The event flag set overrides the loopback type selected during the attach sequence. The colored portions are what the user enters into the system.

To use a specific loopback, type the following:

```
DS> CLEAR EVENT ALL          ; CLEAR PREVIOUS LOOPBACK, IF ANY
DS> SET EVENT X              ; X = EVENT FLAG = LOOPBACK TYPE
                               1 = SHARED RAM
                               2 = LOCAL TRUNK
                               3 = MANUAL T1 CONNECTOR (H3027
                                   or H3028)
                               4 = INTERNAL LINE
                               5 = SINGLE LINE (H3248)
                               6 = STAGGERED LOOPBACK
                               7 = LOCAL MODEM (MANUAL)
                               8 = LOCAL MODEM (PROGRAMMABLE)
```

4.11 DMZ32 LEVEL 2R (EVDAF) DIAGNOSTIC

EVDAF can run only with VAX/VMS Operating System Version 4.0 or later, the latest DMZ32 driver, and the VAX Diagnostic Supervisor Version 7.0 or later.

4.11.1 EVDAF Hardware Prerequisites

The following must be functional before the Level 2R diagnostic may be used:

- DW780, DW750, or DW730 fully tested without errors,
- VAX family of processors with at least the minimum VMS configuration, and
- Modem (optional).

4.11.2 EVDAF Software Diagnostic Requirements

This diagnostic is intended to test the DMZ32 product that is attached to a VAX family of processors. The host VAX system must have the following:

- Minimum memory required by VMS operating system, and
- One (1) DMZ32 module with H3014 distribution panel.

The VAX Diagnostic Supervisors are as follows:

- VAX-11/725/730 - ENSAA,
- VAX-11/750 - ECSAA, and
- VAX-11/780/782 - ESSAA.

4.11.3 EVDAF Diagnostic Description

This diagnostic is an aid to Field Service personnel in the following:

- Verification of customer installation, and
- Service calls: device isolation and verification.

A summary of the tests performed by EVDAF are listed in Table 4-3.

Table 4-3 EVDAF Diagnostic Summary

Test Number	Description
1	Single Line Internal EIA Data Loopback
2	Single Line Internal Data Loopback (DMA)
3	Modem Signals Loopback (H3248)
4	External Data Loopback

4.11.4 Loading, Attaching, and Running EVDAF

The DMZ32 architecture is similar to the DMF32; therefore, many programming similarities exist. The DMZ32 appears very much like the async portion of three (3) DMF32s. CSRs and vectors will appear as if there are three DMF32s on the UNIBUS conductor.

The program treats each octet selected as though it is a separate device. For example:

- When TZA alone is selected, only the first eight lines (octet) of the DMZ32 are tested.
- When TZA and TZB are selected, the program tests TZA (lines 0-7), then the program starts over and tests TZB (lines 8-15). The program treats the two octets as though they were two separate devices. Because of this, the program must run twice.
- When TZA, TZB, and TZC are selected, the program runs TZA first, TZB second, and TZC last.
- The attach sequence must be performed for each octet. (Refer to Figure 4-15.)

On-line help may be obtained by typing HELP EVDAF.

Before EVDAF will run, the following must be performed:

```
$ RUN ENSAA                    ; START SUPERVISOR (11/780/782=ESSAA,
                               ; 11/750=ECSAA, 11/725/730=ENSAA
```

After the Diagnostic Supervisor is loaded, the operating instruction in Figure 4-15 can be used for the EVDAF diagnostic.

The colored portions of Figure 4-15 are what the user enters into the system.

```
DIAGNOSTIC SUPERVISOR.   ZZ-ENSAA-6.10-YYY   9-OCT-1983 09:40:14.80
DS> ATT DW780 SBI DW0 5 7     ; ATTACH THE UBA TO THE SBI, VAX/780
       OR
DS> ATT DW750 HUB DW0         ; FOR VAX/750 TESTING
       OR
DS> ATT DW730 HUB DW0         ; FOR VAX/730 TESTING

DS> LOAD EVDAF                ; LOAD THE DIAGNOSTIC

DS> ATT DMZ32                 ; ATTACH THE 1ST OCTET

DEVICE LINK? DW0              ; THE OPTION IS LINKED TO THE UBA

DEVICE NAME? TZA              ; THE OPTION IS NAMED TZA

CSR? 760440                   ; THE CSR ADRS IS 760440
                              ; (RANGE=760000-777776)

VECTOR? 300                   ; VECTOR ADRS IS 300 (RANGE=300-776)

BR? 5                         ; BR INTERRUPT LEVEL IS 5 (RANGE=5-6)

TEST LINES (OCTET 0)? 377     ; LINES 0-7 IN OCTET 0 WILL BE TESTED
                              ; (OCTET BIT MAP OF DESIRED LINES TO
                              ; TEST, BIT0 = LINE 0,
                              ;       BIT1 = LINE 1, ETC.
                              ;       RANGE = 000-377)
                              ; EXAMPLE: ACTIVE LINES? 123
                              ; TEST LINES SIX, FOUR, ONE AND ZERO

LEVEL 3 ONLY - TEST LINES (OCTET 1) ?  0      ; Applies only to Level 3

LEVEL 3 ONLY - TEST LINES (OCTET 2) ?  0      ; Applies only to Level 3

BAUD RATE? 9600               ; BAUD RATE TO BE USED IN EXTERNAL DATA
                              ; TESTS.  BAUD RATES THAT CAN BE SELECTED
                              ; ARE, 50, 75, 110, 135, 150, 300,
                              ; 600, 1200, 1800, 2000, 2400, 4800,
                              ; 9600, 19200

LOOPBACK TYPE?  4             ; LOOPBACK TYPES ARE:
                              ; 4 = LOCAL LINE (EIA) (INTERNAL LOOPBACK)
                              ; 5 = H3248 TURNAROUND
                              ; 7 = LOCAL MOCEM IN ANALOG LOOP
                              ; 8 = LOCAL MODEM (PROGRAMMABLE LOOPBACK)

MODEM CONTROL?  Y             ; DOES THE DEVICE HAVE MODEM CONTROL,
                              ; YES OR NO.
```

Figure 4-15 Loading, Attaching, and Running EVDAF (Sheet 1 of 2)

```
DS> ATT DMZ32                    ; ATTACH THE 2ND OCTET

DEVICE LINK? DW0                 ; THE OPTION IS LINKED TO THE UBA

DEVICE NAME? TZB                 ; THE OPTION IS NAMED TZB

CSR? 760440                      ; THE CSR ADRS IS 760440
                                 ; (RANGE=760000-777776)

VECTOR? 300                      ; VECTOR ADRS IS 300 (RANGE=300-776)

BR? 5                            ; BR INTERRUPT LEVEL IS 5 (RANGE=5-6)

TEST LINES (OCTET 0)? 377

LEVEL 3 ONLY - TEST LINES (OCTET 1)? 0       ; Applies only to Level 3

LEVEL 3 ONLY - TEST LINES (OCTET 2)? 0       ; Applies only to Level 3

BAUD RATE? 9600

LOOPBACK TYPE?  4

MODE CONTROL?  Y

DS> ATT DMZ32                    ; ATTACH THE 3RD OCTET

DEVICE LINK? DW0                 ; THE OPTION IS LINKED TO THE UBA

DEVICE NAME? TZC                 ; THE OPTION IS NAMED TZC

CSR? 760440                      ; THE SCR ADRS IS 760440
                                 ; (RANGE=760000-777776)

VECTOR? 300                      ; VECTOR ADRS IS 300 (RANGE=300-776)

BR? 5                            ; BR INTERRUPT LEVEL IS 5 (RANGE=5-6)

TEST LINES (OCTET 0)? 377

LEVEL 3 ONLY - TEST LINES (OCTET 1)? 0       ; Applies only to Level 3

LEVEL 3 ONLY - TEST LINES (OCTET 2)? 0       ; Applies only to Level 3

BAUD RATE? 9600

LOOPBACK TYPE?  4

MODEM CONTROL?  Y

DS> SEL TZA                      ; SELECTS LINES 0-7

DS> SEL TZB                      ; SELECTS LINES 8-15

DS> SEL TZC                      ; SELECTS LINES 16-23

DS> START
```

Figure 4-15 Loading, Attaching, and Running EVDAF (Sheet 2 of 2)

4.12 H3014 FRONT PANEL INDICATORS

There are three (3) LED indicators on the H3014 distribution panel. These LED indicators are located directly above the T1 connector, as viewed from the connector side of the panel. (Refer to Figure 4-16.) These indicators are as follows:

- Power (PWR),
- Sync (SYNC), and
- Trunk Quality (TRNK QLTY).

The three LEDs display information that indicates the status of the H3014. (Refer to Table 4-4 for the different indication combinations.)

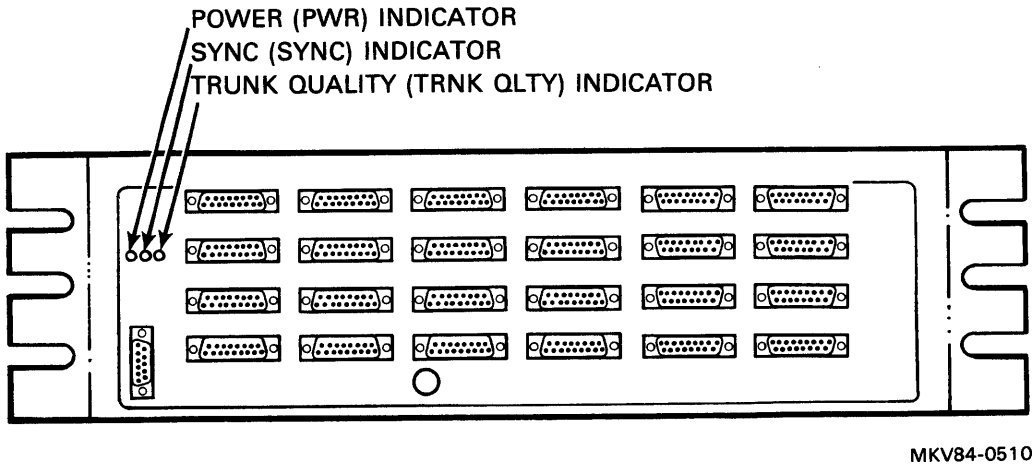


Figure 4-16 H3014 LED Indicators

4.12.1 Power Indicator (PWR)

The PWR LED indicator provides an on-line indication that the three power supply outputs (+12 V, −12 V, and +5 V) are good. If any of the three power supplies fail, the PWR indicator will go out.

Refer to Table 4-4 for the coded display indications.

4.12.2 Sync Indicator (SYNC)

The SYNC LED, when ON, indicates the presence of T1 synchronization.

Refer to Table 4-4 for the coded display indications.

4.12.3 Trunk Quality Indicator (TRNK QLTY)

When the T1 circuitry in the H3014 detects a bipolar violation, the TRNK QLTY LED will be turned OFF for approximately one (1) second.

Table 4-4 H3014 Front Panel Indicators

PWR	SYNC	TRNK	Signal Conditions	Probable Cause
ON	ON	ON	Power OK T1 link synchronized No bipolar violations	Normal operation
ON	OFF	ON	Loss of T1 synchronization	Refer to microdiagnostic status LEDs on M8398 for failing device
ON	BLINKING	ON	Two masters tied together	Wrong jumper settings on M8398 or H3014 processor module
ON	OFF	OFF	Loss of incoming T1 signal	T1 cable disconnected T1 cable broken T1 cable installed backwards on M8398 module
OFF	OFF	OFF	Power loss	Bad H3014 ac power fuse Bad H3014 power supply

4.13 H3014 REMOVAL/REPLACEMENT PROCEDURES

This section contains the removal and replacement procedures for all field replaceable units contained in the H3014 distribution panel.

The tools required are:

- 7/64 Allen wrench, and
- Small Phillips screwdriver.

WARNING

Before performing these removal or replacement procedures, make sure that the H3014 is turned OFF and the power cord is removed from the power controller.

4.13.1 H3014 Power Supply Assembly Removal/Replacement (29-24799-00)

1. Open the VAX cabinet using a 7/64 Allen wrench.
2. Disconnect input power cable from the H3014 power receptacle. (Refer to Figure 4 -17.)
3. Loosen the two (2) 1\4 turn Phillips head lock fasteners on the H3014 distribution panel. (Refer to Figure 4-17.)
4. Open the rear cover of the H3014 distribution panel.
5. Disconnect the power connector that is connected to the fan assembly. (Refer to Figure 4-18.)
6. Disconnect the power connectors from the processor module and the expansion module. (Refer to Figure 4-18.)
7. Remove the processor module. (Refer to Figure 4-18.)
8. Lift the power supply assembly about 12.7 mm (1/2 inch) and pull the assembly out of the H3014 chassis. (Refer to Figure 4-18).
9. Using a 3/8 nut driver, disconnect the CHASSIS GND connection from the power supply chassis.
10. To replace the power supply assembly, reverse Steps 1 through 9.

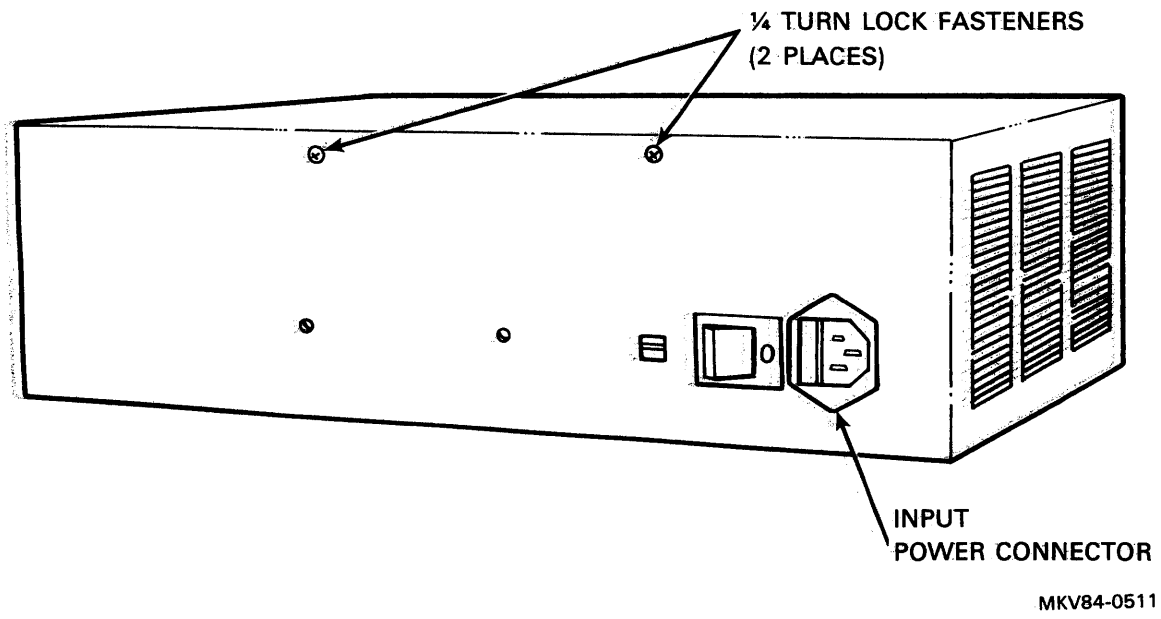


Figure 4-17 1/4 Turn Lock Fasteners

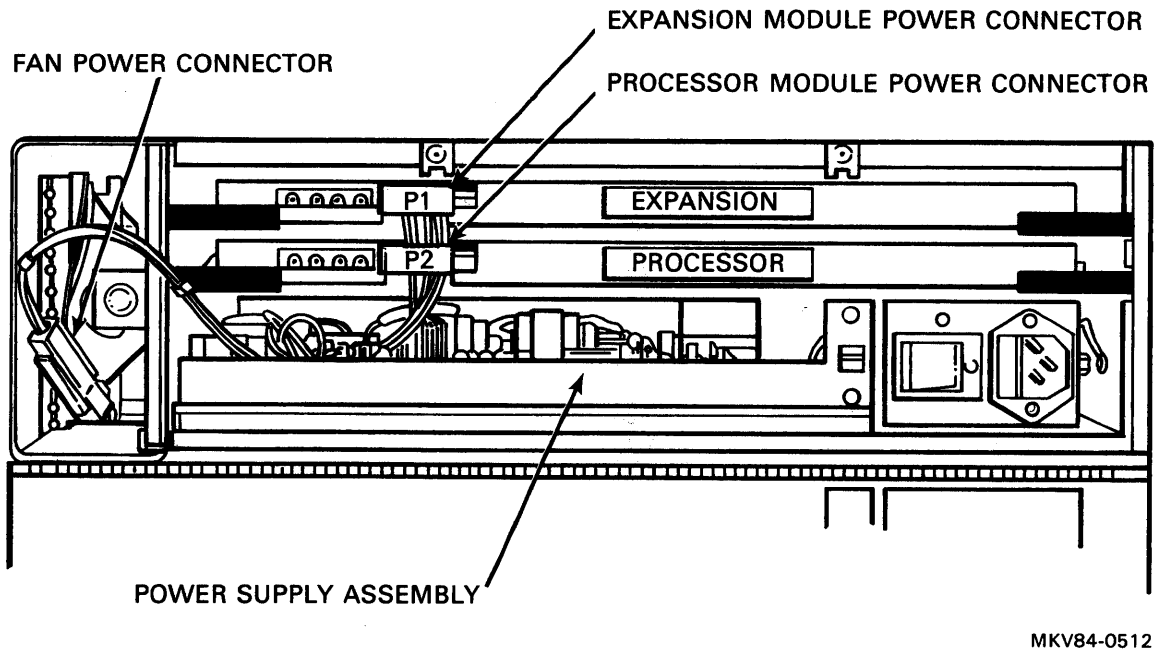


Figure 4-18 H3014 Power Supply Location

4.13.2 H3014 Fan Assembly Removal/Replacement (29-24800-00)

1. Open the VAX cabinet using a 7/64 Allen wrench.
2. Disconnect the input power cable from the H3014 power receptacle (Figure 4-17).
3. Loosen the two 1/4 turn Phillips head lock fasteners on the H3014 distribution panel. (Refer to Figure 4-17.)
4. Open the rear cover of the H3014 distribution panel.
5. Disconnect the power connector that is connected to the fan assembly. (Refer to Figure 4-19.)
6. Slide the fan assembly out of the H3014 chassis by pulling the fan mounting bracket toward the rear of the chassis (Figure 4-20).

CAUTION
Make certain that the fan is installed so that the air flows inward.

7. To replace the fan assembly, reverse Steps 1 through 6.

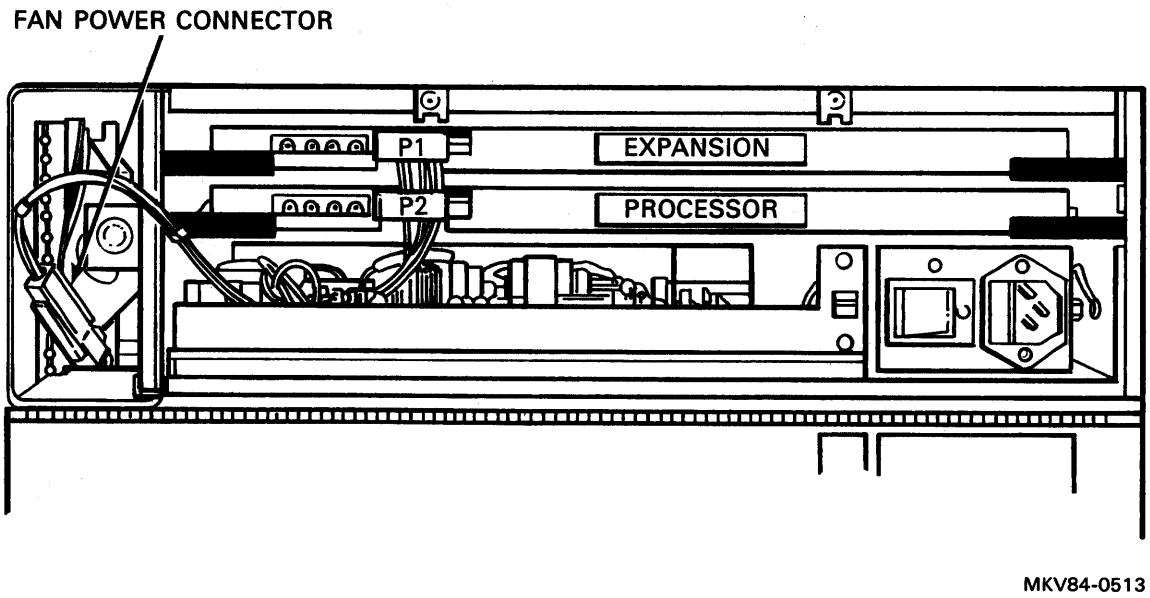


Figure 4-19 H3014 Fan Assembly Location

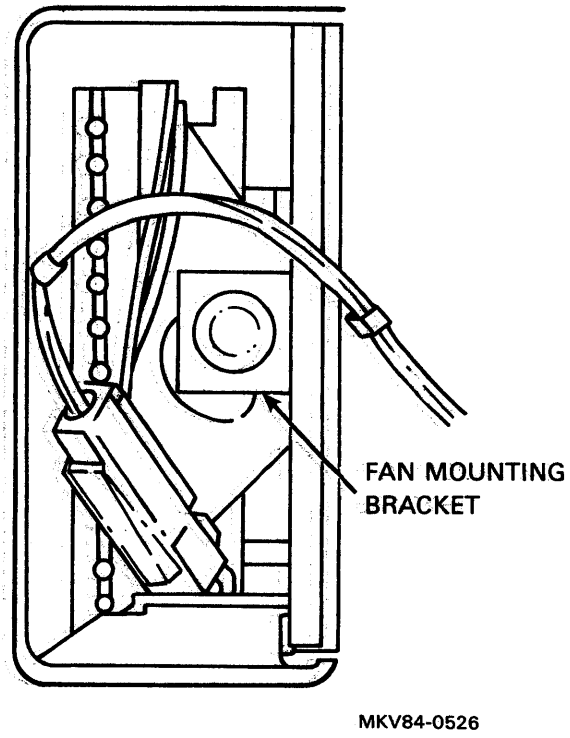


Figure 4-20 Fan Mounting Bracket Assembly

4.13.3 H3014 Expansion Module Remove/Replacement (29-24798-00)

1. Open the VAX cabinet using a 7/64 Allen wrench.
2. Disconnect the input power cable from the H3014 power receptacle (Figure 4-17).
3. Loosen the two 1/4 turn lock Phillips head fasteners on the H3014 distribution panel. (Refer to Figure 4-17.)
4. Open the rear cover of the H3014 distribution panel.
5. Disconnect the expansion module and the processor module power connectors. (Refer to Figure 4-21.)
6. Grasp the two finger handles on both sides of the expansion module (Figure 4-21). Pull the finger handles toward the back of the H3014 to physically remove the expansion module from the backplane.
7. To replace the expansion module, reverse Steps 1 through 6.

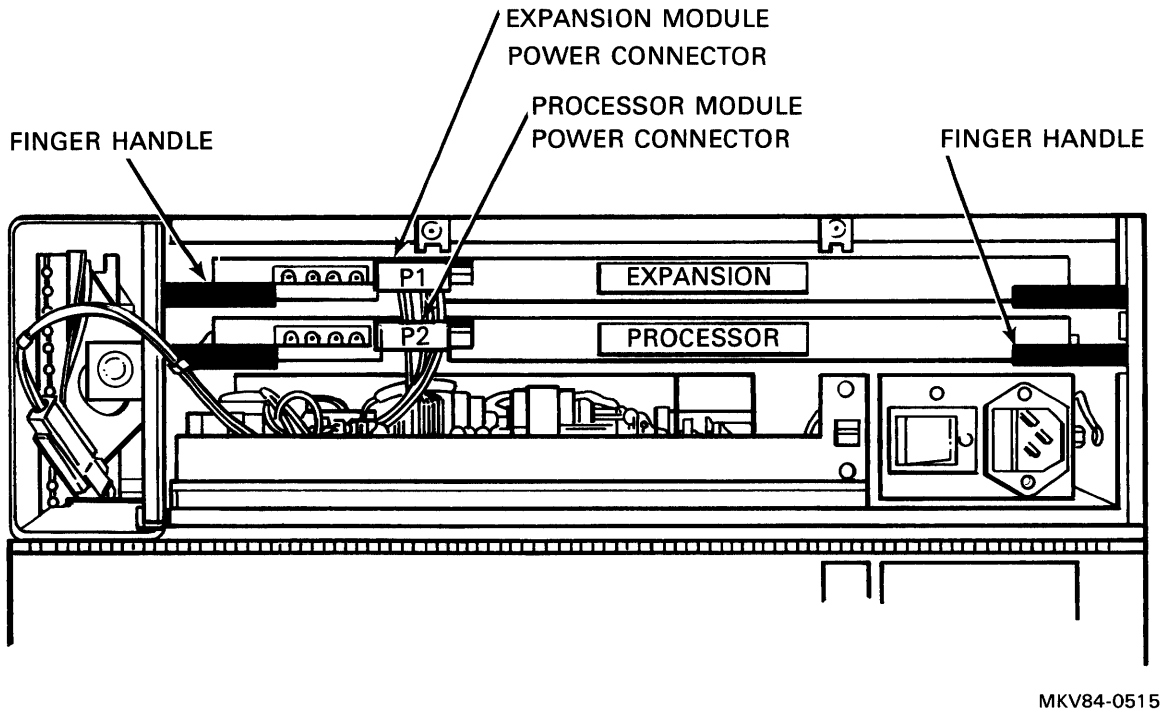


Figure 4-21 H3014 Expansion Module Location

4.13.4 H3014 Processor Module Removal/Replacement (29-24797-00)

1. Open the VAX cabinet using a 7/64 Allen wrench.

2. Disconnect the input power cable from the H3014 power receptacle (Figure 4-17).

3. Loosen the two 1/4 turn lock Phillips head fasteners on the H3014 distribution panel. (Refer to Figure 4-17.)

4. Open the rear cover of the H3014 distribution panel.

5. Disconnect the processor module and expansion module power connectors. (Refer to Figure 4-21.)

6. Grasp the two finger handles on both sides of the processor module (Figure 4-21). Pull the finger handles toward the back of the H3014 to physically remove the processor module from the backplane.

7. To replace the processor module, reverse Steps 1 through 6.

NOTE

Before placing the processor module back into the H3014, verify the following jumpers and switch settings.

- **Jumper between switch settings E6 and E7 is always in place. (Refer to Figure 4-22.)**

- **Jumper between switch settings E4 and E5 is always in place. (Refer to Figure 4-23.)**

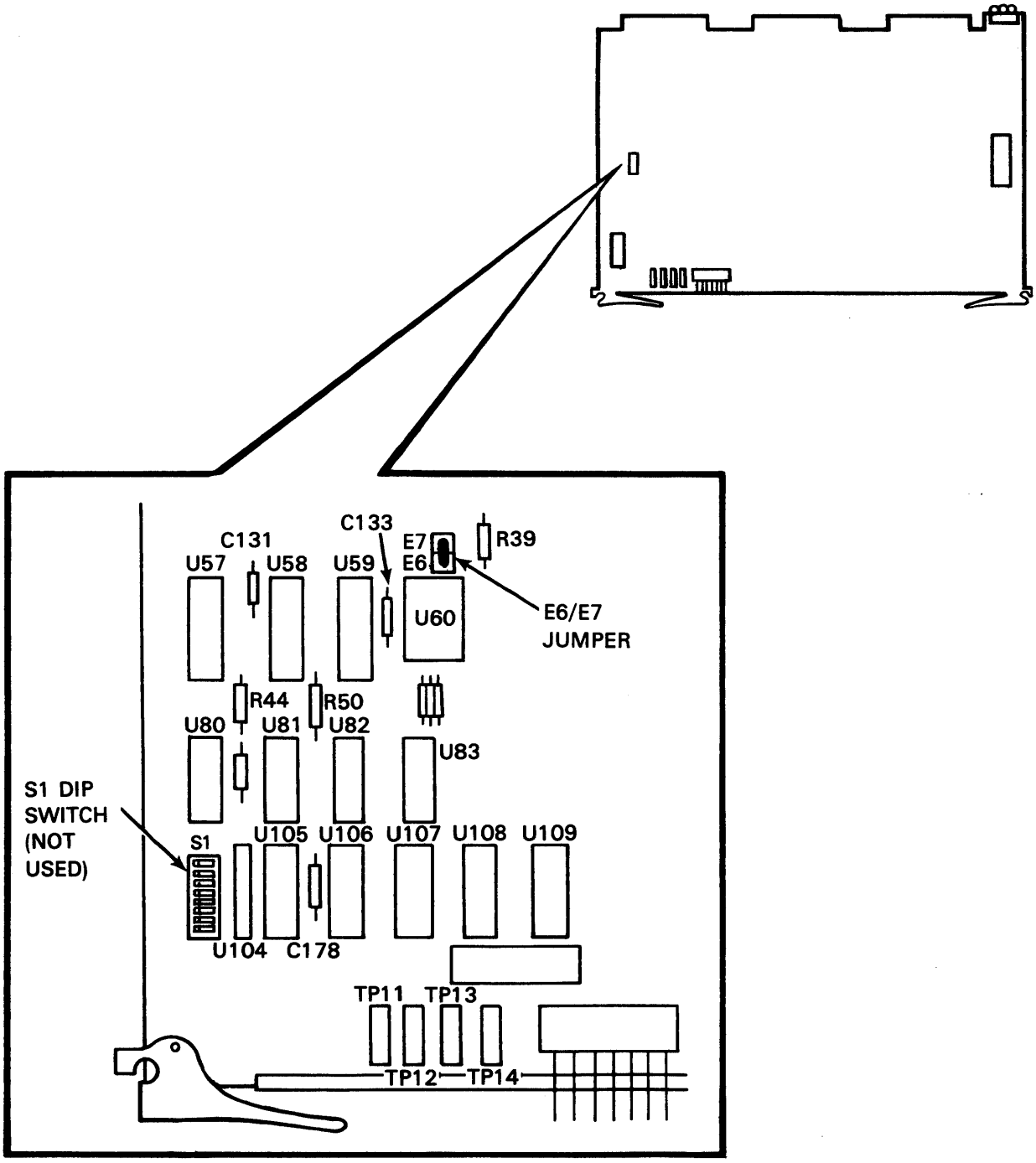


Figure 4-22 Processor Module Clock Jumper and Dip Switch

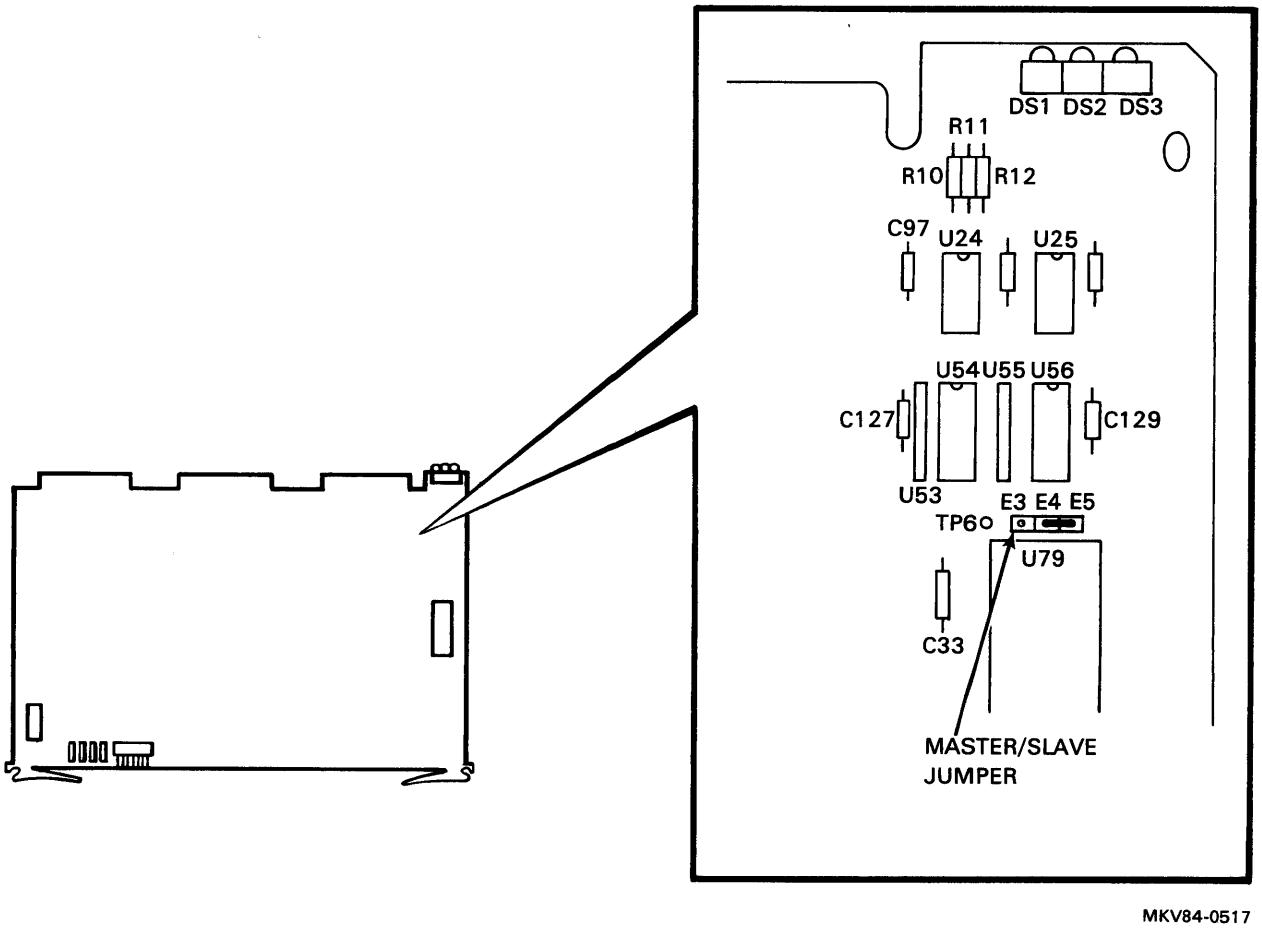
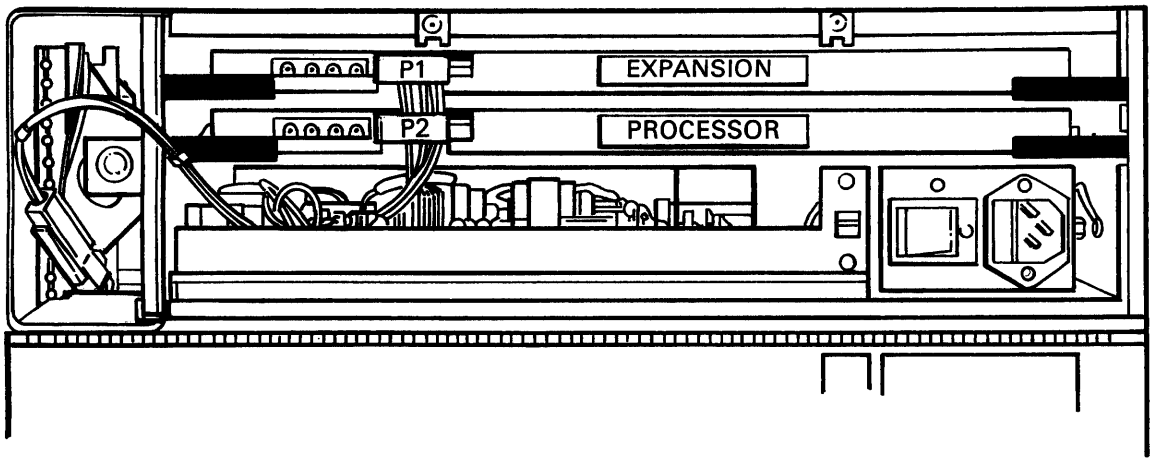


Figure 4-23 Processor Module Master/Slave Jumper

4.13.5 H3014 Chassis/Backplane Replacement

CAUTION
Two people are needed to perform this procedure. One person must hold the chassis in place while the other person removes the screws.

1. Disconnect all cables that are attached to the distribution panel.
2. Loosen the two 1/4 turn lock Phillips head fasteners on the H3014 distribution panel. (Refer to Figure 4-17.)
3. Disconnect the input power connectors to the expansion module and the processor module. (Refer to Figure 4-24.)
4. Remove the expansion module from the distribution panel. (Refer to Section 4.13.3.)
5. Remove the controller module from the distribution panel. (Refer to Section 4.13.4.)
6. Remove the power supply module from the distribution panel. (Refer to Section 4.13.1.)
7. Remove the fan assembly from the distribution panel. (Refer to Section 4.13.2.)
8. Remove the eighteen (18) Phillips screws that secure the mounting bracket of the distribution panel to the chassis. (Refer to Figure 4-25.)
9. To replace the H3014 chassis/backplane, reverse Steps 1 through 8.



MKV84-0523

Figure 4-24 Processor/Expansion Module Input Power

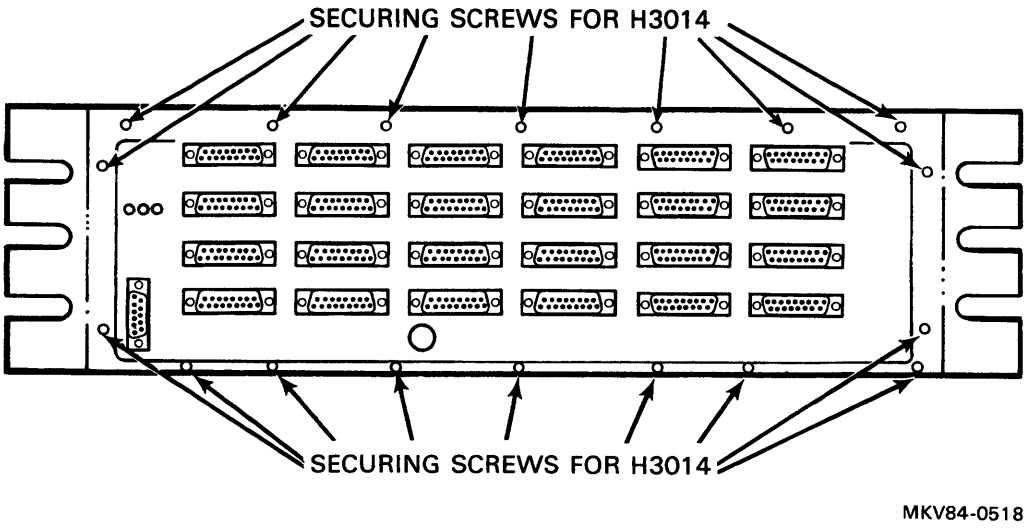


Figure 4-25 Chassis/Backplane Securing Screws Location

APPENDIX A
FLOATING DEVICE ADDRESSES AND VECTORS

A.1 FLOATING DEVICE ADDRESSES

UNIBUS addresses starting at 760010 and continuing through 763776 are designated as floating device addresses. (See Figure A-1.) These are used as register addresses for communications (and other) devices interfacing with VAX-11 computers.

A gap of 10_8 must be left between the last address of one device type and the first address of the next device type. The first address of the next device type must start on a module 10_8 boundary. The gap of 10_8 must also be left for devices that are not installed but are skipped over in the priority ranking list. Multiple devices of the same type must be assigned continuous addresses. Reassignment of device types already in the system may be required to make room for additional ones.

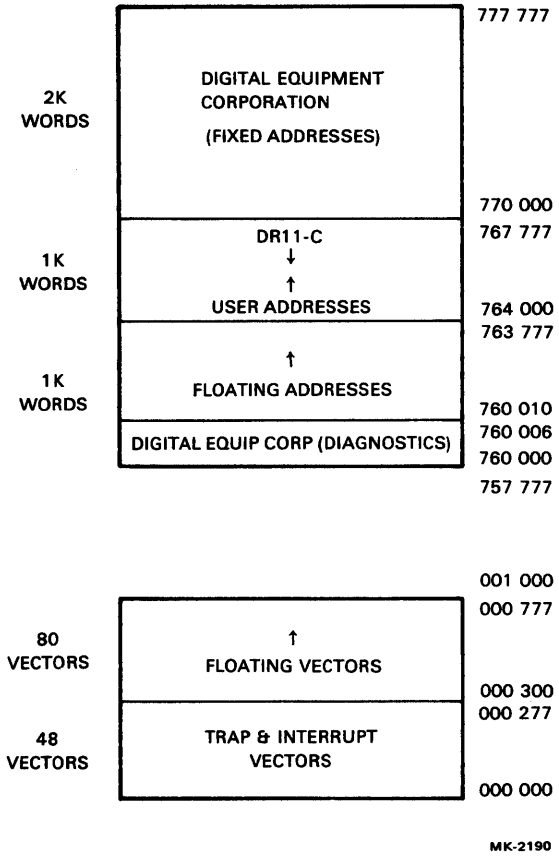


Figure A-1 UNIBUS Address Map

Table A-1 gives the floating CSR address assignments for UNIBUS and QBUS devices.

Table A-1 Floating CSR Address Assignments

Rank	Option	Decimal Size	Option Modulus	
1	DJ11	4	10	
2	DH11	8	20	
3	DQ11	4	10	
4	DU11,DUV11	4	10	
5	DUP11	4	10	
6	LK11A	4	10	
7	DMC11/DMR11	4	10	(DMC Before DMR)
8	DZ11/DZV11, DZS11,DZ32	4	10	(DZ11 Before DZ32)
9	KMC11	4	10	
10	LPP11	4	10	
11	VMV21	4	10	
12	VMV31	8	20	
13	DWR70	4	10	
14	RL11,RLV11	4	10	(After first)
15	LPA11-K	8	20	(After first)
16	KW11-C	4	10	
17	Reserved	4	10	
18	RX11/RX211 RXV11/RXV21	4	10	(After first) (RX11 Before RX211)
19	DR11-W	4	10	
20	DR11-B	4	10	(After second)
21	DMP11	4	10	
22	DPV11	4	10	
23	ISB11	4	10	
24	DMV11	8	20	
25	DEUNA	4	10	(After first)
26	UDA50	2	4	(After first)
27	DMF32	16	40	
28	KMS11	6	20	
29	VS100	8	20	
30	Reserved	2	4	(After first)
31	Reserved	8	20	
32	Reserved	8	20	
33	DMZ32	16	40	

A.2 FLOATING VECTOR ADDRESSES

Vector addresses starting at 300 and proceeding upward to 777 are designated as floating vectors. These are used for communications (and other) devices that interface with the VAX family of computers. Vector size is determined by the device type.

Multiple devices of the same type would be assigned vectors sequentially. Table A-2 shows the floating interrupt vector device assignment sequence.

Table A-2 Floating Interrupt Vector Device Assignment

Rank	Device	Decimal Size	Octal Modulus	
1	DC11	4	10	
1	TU58	4	10	
2	KL11	4	10	
2	DL11-A	4	10	
2	DL11-B	4	10	
2	DLV11-J	16	10	
2	DLV11,DLV11-F	4	10	
3	DP11	4	10	
4	DM11-A	4	10	
5	DN11	2	4	
6	DM11-BB/BA	2	4	
7	DH11 Modem Control	2	4	
8	DR11-A,DRV11-B	4	10	
9	DR11-C,DRV11	4	10	
10	PA611 (Reader + Punch)	8	10	
11	LPD11	4	10	
12	DT07	4	10	
13	DX11	4	10	
14	DL11-C	4	10	
14	DL11-D	4	10	
14	DL11-E/DLV11-E	4	10	
15	DJ11	4	10	
16	DH11	4	10	
17	GT40	8	10	
17	VSV11	8	10	
18	LPS11	12	10	
19	DQ11	4	10	
20	KW11-W,KWV11	4	10	
21	DU11,DUV11	4	10	
22	DUP11	4	10	
23	DV11 + Modem Control	6	10	
24	LK11-A	4	10	
25	DWUN	4	10	
26	DMC11	4	10	
26	DMR11	4	10	(DMC Before DMR)

Table A-2 Floating Interrupt Vector Device Assignment (Cont)

Rank	Device	Decimal Size	Octal Modulus	
27	DZ11/DZS11/DZV11, DZ32	4	10	(DZ11 Before DZ32)
28	KMC11	4	10	
29	LPP11	4	10	
30	VMV21	4	10	
31	VMV31	4	10	
32	VTV01	4	10	
33	DWR70	4	10	
34	RL11/RLV11	2	4	(After the first)
35	TS11,TU80	2	4	(After the first)
36	LPA11-K	4	10	
37	IP11/IP300	2	4	(After the first)
38	KW11-C	4	10	
39	RX11/RX211 RXV11/RXV21	2	4	(After the first) (RX11 Before RX211)
40	DR11-W	2	4	
41	DR11-B	2	4	(After the first)
42	DMP11	4	10	
43	DPV11	4	10	
44	ML11	2	4	(MASSBUS device)
45	ISB11	4	10	
46	DMV11	4	10	
47	DEUNA	2	4	(After the first)
48	UDA50	2	4	(After the first)
49	DMF32	16	4	
50	KMS11	6	10	
51	PCL11-B	4	10	
52	VS100	2	4	
53	Reserved	2	4	(After the first)
54	Reserved	4	10	
55	Reserved	4	10	
56	Reserved	4	10	
57	Reserved	4	10	
58	DMZ32	12	4	

APPENDIX B
T1 CABLE SPECIFICATIONS

B.1 INTRODUCTION

This appendix gives information concerning the T1 link from the 2 × 4 I/O panel insert on the FCC bulkhead frame to the T1 connector input of the remote distribution panel (H3014).

B.2 CABLE CONFIGURATION

The T1 cable (BC18L-xx or BC18M-xx) is connected between the 2 × 4 I/O panel insert on the FCC bulkhead frame and the T1 connector input of the H3014. This T1 cable configuration defines the detail requirements for a 4-conductor shielded cable assembly with a 15-position female D-subminiature connector at one end and a 15-position male D-subminiature connector at the other end.

A BC18L-15 is supplied with this option when purchased. Cables of other lengths may be fabricated using the component specifications listed in Table B-1 or ordered directly from Digital Equipment Corporation. (Refer to Table B-2.)

Table B-1 BC18L-xx Component Parts

DIGITAL Part Number	Description	Material & Finish
12-10493-39	Crimp terminal pin (contact) Accommodates AWG 20-24	Brass, gold flash over nickel 0.00005 minimum thickness on entire contact with additional 0.00002 gold thickness on mating end for length of 0.150/0.175 inch. Carrier strip may not be gold plated.
	NOTE **An AMP™ 90265-1 crimping tool is to be used when inserting pin into the connector housing (12-10493-57).**	
12-10493-41	Crimp terminal socket (contact) Accommodates AWG 20-24	Phosphor bronze gold flash over nickel 0.00005 minimum thickness on entire contact with additional 0.00002 gold minimum thickness on mating end for length of 0.150/0.175 inch.

AMP is a trademark of AMP, Inc.

Table B-1 BC18L-xx Component Parts (Cont)

DIGITAL Part Number	Description	Material & Finish
	NOTE **An AMP™ 90302-1 crimping tool is to be used when inserting the socket into the connector housing (12-10493-58).**	
12-10493-57	Connector housing for 15 male (pins) contacts with strain relief.	a. Shell: Steel with tin plating. b. Insulator: Glass filled nylon, color black.
12-10493-58	Connector housing for 15 female (sockets) contacts with strain relief.	a. Shell: Steel with tin plating. b. Insulator: Glass filled nylon, color black.

Table B-2 DIGITAL Cable Option Designations

Cable Length	DIGITAL Option Number
T1 External PVC Cable BC18L	
4.5 m (15 ft)	BC18L-15
15.2 m (50 ft)	BC18L-50
30.5 m (100 ft)	BC18L-A0
45.7 m (150 ft)	BC18L-A5
61.0 m (200 ft)	BC18L-B0
76.2 m (250 ft)	BC18L-B5
106.7 m (350 ft)	BC18L-C5
152.4 m (500 ft)	BC18L-E0
228.6 m (750 ft)	BC18L-H5
305.0 m (1000 ft)	BC18L0L0
T1 External Plenum Cable BC18M	
4.5 m (15 ft)	BC18M-15
15.2 m (50 ft)	BC18M-50
30.5 m (100 ft)	BC18M-A0
45.7 m (150 ft)	BC18M-A5
61.0 m (200 ft)	BC18M-B0
106.7 m (350 ft)	BC18M-C5
152.4 m (500 ft)	BC18M-E0
228.6 m (750 ft)	BC18M-H5
305.0 m (1000 ft)	BC18M-L0

B.3 T1 CONDUCTOR CHARACTERISTICS

The conductor that is used for the T1 link has the following characteristics.

Electrical Characteristics

Pairs:

Nominal impedance – 100 ohms

Nominal capacitance between conductors – 16 pF/ft

Nominal velocity of propagation – 66%

Nominal delay – 1.54 nanoseconds per ft

Capacitance unbalance (pair to pair) – 160 pF/1000 feet – maximum at 1000 Hz

Resistive unbalance (individual pair) – 1.20 ohms dc/1000 ft – maximum

Crosstalk – 70 dB/1000 ft minimum at 150 kHz far end

Insulation resistance – 10×10^6 ohms/1000 ft minimum at 200-500 Vdc for one (1) minute

Attenuation – 6.0 dB/1000 ft maximum at one (1) MHz

Shield coverage – 100%

Nominal shield dc resistance – 5.0 ohms/1000 ft

Nominal conductor dc resistance – 17.0 ohms/1000 ft

Maximum operating voltage – 150 Vac RMS

UL listed AWM style 2919

Physical Characteristics

Nominal weight/1000 ft – 40 lbs

Minimum bending radius – 3 inches

Temperature rating – –30 to 80°C

Shield type – foil and braid with 22 AWG drain wire

Maximum pulling tension – 64 lbs

Insulation material – polyethylene

Jacket material – PVC

Outside dimensions – .296 inches diameter

NOTE
Refer to Table B-3 for T1 cable color codes and point-to-point wiring.

Table B-3 T1 Cable Schematic

Wire Table

Description AWG	Color	From Connection	To Connection
22	WHT/BLU	P1-9	P2-9
22	BLU	P1-1	P2-1
22	WHT/ORN	P1-1	P2-11
22	ORN	P1-3	P2-3
22	DRAIN	P1 Shell	P2 Shell

EDUCATIONAL SERVICES DEVELOPMENT AND PUBLISHING UPDATE NOTICE

DMZ32 User Guide

EK-DMZ32-UG-CN1

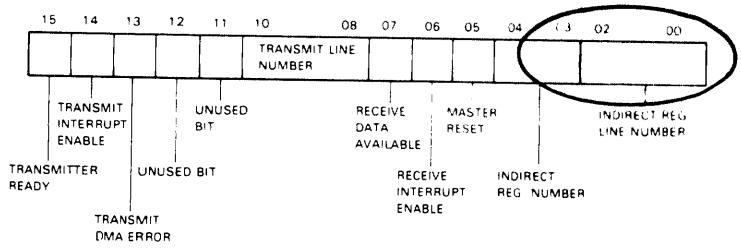
July 1984

The original *DMZ32 User Guide* is wire-o bound and cannot accommodate inserted update pages. This update notice directs the document user in the changes that must be made to correct errors. This update should be pasted on the reverse of the front cover in order to maintain a record of changes to the document.

CORRECTIONS

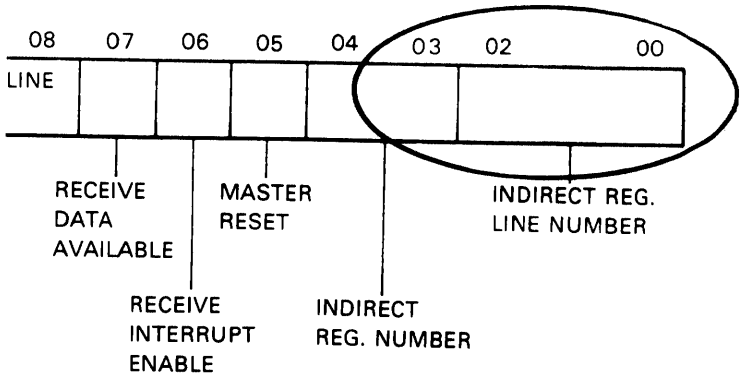
Page 3-6 – – Figure 3-2
[OCTET.CSR (READ/WRITE)]

Change bits 02 and 03 to agree with art shown.



Page 3-11 – – Figure 3-6

Change bits 02 and 03 to agree with art shown.



Page 4-22 – – Figure 4-10; Page 4-23 – – Figure 4-11;
Page 4-24 – – Figure 4-12; Page 4-25 – – Figure 4-13

In the color key, change LOOPBACK to VERIFIED GOOD and change VERIFIED GOOD to LOOPBACK. (See diagram.)