Firefox Workstation Q-Bus Adapter Module Functional Specification

Revision 3.0

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December 28, 1987

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Revision History

Date	Version	Content/Changes
11 Dec 87	3.0	Change status indicators from 6 to 5; move BOM and timing to Engineering specification
14 Aug 87	2.1	Design review update
01 May 87	2.0	Implementation description update
30 Jan 87	1.0	First external release
12 Jan 87	0.0	Preliminary draft

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11. Firefox Q-Bus Adapter Module

This functional specification for the Firefox Q-bus adapter module describes the functionality of the module, presents the specific implementation that achieves that function, and lists required software initialization and programming guidelines.

The Firefox Q-bus adapter module (FQAM), which is optional for a Firefox workstation, implements an M-bus-to-Q-bus adapter in a single L-series-quad module. The module functions are the following:

- M-bus interface
- Q-bus interface
- Diagnostic ROM
- Status indicators

If an FQAM is present in a Firefox workstation, it must be in M-bus slot 0. There can be no more than one FQAM per workstation.

11.1. Functionality

In this section, the functionality of the FQAM is defined without specific reference to actual implementation.

11.1.1. M-Bus Interface

The FQAM implements an M-bus interface that conforms to the *Firefox M-Bus Specification*. In addition to satisfying the M-bus interface requirements, the M-bus interface supports the following:

- Slave access to the control and status registers of the Q-bus interface
- Slave access to the diagnostic ROM and status indicators
- Master access to the M-bus for Q-bus interface DMA
- Generation and acknowledgement of interrupts for the Q-bus interface

The Q-bus 4-Mbyte memory space and the adapter diagnostic ROM reside in the 32-Mbyte I/O-space region associated with the M-bus slot of the FQAM module. The Q-bus interface control and status registers reside at a fixed addresses in I/O space.

11.1.2. Q-Bus Interface

The FQAM implements a Q-bus interface that conforms to the *DEC STD 160 Q22-Bus Specification* in the following ways:

- The Q-bus interface supports only the arbiter role on the Q-bus.
- The Q-bus interface supports a scatter/gather map for the 4-Mbyte Q-bus memory space into the first 512 Mbytes of M-bus memory space.
- The Q-bus interface supports forwarding of Q-bus interrupts onto the M-bus and M-bus interrupt-acknowledge cycles onto the Q-bus.

11.1.3. Diagnostic ROM

The FQAM implements 256 Kbytes of socketed ROM for use by diagnostics. The ROM is accessible to software via I/O-space references.

11.1.4. Status Indicators

The FQAM implements status indicators that convey five bits of information via red LEDs. The state of the status indicators is cleared at system reset, resulting in all LEDs illuminated. The state of the status indicators can be modified from software via I/O-space references.

11.1.5. External Connection

The FQAM connects to both the Q-bus and the M-bus through the A/B backplane connectors.

11.2. Implementation

The FQAM, which is implemented in a single *L-series-quad* module, implements an M-bus interface, a Q-bus interface, diagnostic ROM, and status indicators. Figure 11-1 shows a block diagram of the FQAM.

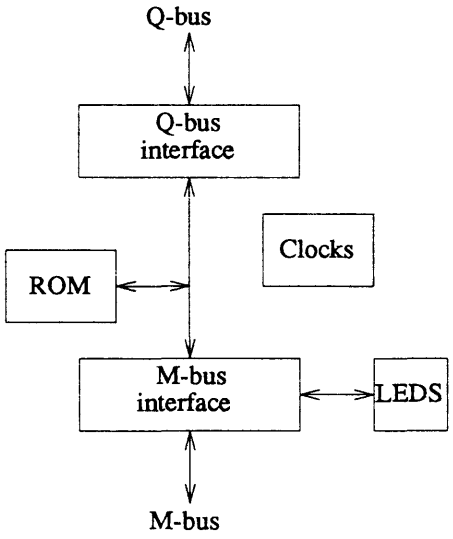

Figure 11-1: Firefox Q-Bus Adapter Module Block Diagram

11.2.1. M-Bus Interface

The M-bus interface consists of the Firefox Bus Interface Chip (FBIC), seven 74F245 M-bus transceivers, one 74F244 M-bus driver, one 74AS760 open collector M-bus driver and one 74F244 status indicator driver.

11.2.1.1. Device Features

The FBIC, currently under design by the WSE group in Palo Alto, is a multipurpose, bus interface and cache controller that connects a CVAX pin-bus to the M-bus and supports an optional snoopy cache. The chip functions as both a CVAX pin-bus master and CVAX pin-bus slave, depending on the needs of the particular module on which it resides. On the FQAM, it is the default C-bus master and controls arbitration of that bus. The FBIC also supports the M-bus write-back snoopy cache protocol defined in the *Firefox M-Bus Specification* for an internal single-entry cache or for an optional external cache. The FQAM does not use the external-cache option of the FBIC.

The chip contains two separately clocked, synchronous-state machines. The CVAX pin-bus state machine monitors and initiates transactions on the CVAX pin-bus. The M-bus synchronous-state machine monitors and initiates transactions on the system M-bus.

The FBIC implements all of the M-bus interface functions necessary to access FQAM control and status registers and ROM from the M-bus. It allows the Q-bus interface to access memory via the M-bus, connects the C-bus interrupt request signals from the Q-bus interface to the M-bus, and forwards M-bus

interrupt acknowledge cycles onto the C-bus. In addition, the FBIC controls the 32-bit diagnostic ROM and a 5-bit status indicator.

A detailed description of the FBIC's operation and the format of its control and status registers can be found in the *Firefox FBIC Functional Specification.*

11.2.1.2. Busses

The FBIC connects to both the M-bus and the C-bus and forwards transactions between the busses as appropriate. Table 11-1 lists the FBIC response to C-bus transactions. The other possible CVAX pin-bus transaction types--request D-stream read, external IPR read, interrupt acknowledge, request I-stream read, demand D-stream read modify intent, and external IPR write--are never generated on the FQAM.

Table 11-1: FBIC Response to CVAX Pin-Bus Transactions

CVAX Pin-bus Transaction	FBIC Response
Demand D-stream read	Internal-cache read/M-bus read
Write	Internal-cache write/M-bus write

Because the FBIC is the default C-bus master, it monitors DMR and asserts DMG as appropriate. The C-bus transactions listed in Table 11-2 can be initiated only after the bus has been acquired from the FBIC via DMR/DMG. When the FBIC is not the C-bus master, it monitors the C-bus and services transactions that reference it or the M-bus.

Table 11-2 lists the FBIC's response to M-bus transactions. For I/O-space transactions, a reference is in range if it is in the 32-Mbyte region assigned for the slot or if the FBIC address decoder matches. The address decoder is used to access the Q-bus interface and must be programmed after every workstation reset to match M-bus addresses 8000XXXX#16 and 8008XXXX#16 (VAX addresses 2000XXXX#16 and 2008XXXX#16). For interrupt-acknowledge transactions, a C-bus interrupt-acknowledge transaction is initiated if the IRQ signal for the specified interrupt level is asserted on the C-bus.

Table 11-2: FBIC Response to M-Bus Transactions

M-Bus Transaction	FBIC Response
Memory read	Supply cache data if shared and dirty
Memory write	Update cache if shared
I/O read	C-bus I/O read if in address range
I/O write	C-bus I/O write if in address range
Interrupt acknowledge	C-bus interrupt acknowledge if IRQ<n>

To avoid Q-bus/M-bus deadlocks, if a C-bus transaction in progress requires use of the M-bus at the same time as an M-bus transaction requires use of the C-bus, the M-bus transaction will receive a retry termination status.

11.2.1.3. Interrupts

The FBIC monitors the C-bus IRQ signals, and if enabled via the FBIC IRQMASK CSR, asserts the corresponding MIRQ signals. When an M-bus interrupt-acknowledge transaction for an asserted IRQ signal occurs, the FBIC generates a C-bus interrupt-acknowledge transaction that, in turn, generates a Q-bus interrupt-acknowledge transaction.

11.2.1.4. Reset

The FBIC is reset when the MRESET signal is asserted. The RESET function of the FBIC can be used as a software controlled I/O reset. That is, internal reset is the OR of MRESET and FBIC RESET.

11.2.1.5. FBIC Address Map

Table 11-3 lists the address offsets of the FBIC control and status registers. All registers are longword aligned. For example, to read the MODTYPE CSR, a VAX issues a longword read to address 31FFFFFC#16. Because the FQAM must be in backplane slot 0, the base address is always VAX address 30000000#16.

Table 11-3: FBIC CSR Offsets

Name	Address	Read/Write	Description
MODTYPE	01FFFFFC#16	Read	Module type register
BUSCSR	01FFFFF8#16	Read/Write	M-bus error status register
BUSCTL	01FFFFF4#16	Read/Write	M-bus error control signal log register
BUSADR	01FFFFF0#16	Read/Write	M-bus error address signal log register
BUSDAT	01FFFFEC#16	Read/Write	M-bus error data signal log register
FBICSR	01FFFFE8#16	Read/Write	FBIC control status register
RANGE	01FFFFE4#16	Read/Write	I/O space range decode register
IPDVINT	01FFFFE0#16	Read/Write	Interprocessor/device interrupt register
WHAMI	01FFFFDC#16	Read/Write	Unique software ID register
CPUID	01FFFFD8#16	Read	Unique hardware ID register
IADR1	01FFFFD4#16	Read/Write	Interlock-1 address register
IADR2	01FFFFD0#16	Read/Write	Interlock-2 address register
SAVGPR	01FFFFC4#16	Read/Write	Scratch register for halt code

11.2.2. Q-Bus Interface

The Q-bus interface consists of the CVAX Q-Bus Interface chip (CQBIC), four termination resistor SIPs, one wake-up capacitor, one 5.6K 1 percent bias resistor, and open-drain output pull-up resistors.

11.2.2.1. Device Features

The CQBIC implements a CVAX pin-bus to Q-bus interface, a 16-entry cache of the 8192-entry scatter/gather map, control and status registers, interrupt logic, and Q-bus transceivers.

The CQBIC supports byte, word, and longword transfers from the CVAX pin-bus to the Q-bus and internal registers, 16-word writes from the Q-bus to system memory via the CVAX pin-bus, and quadword reads from the system memory to the Q-bus via the CVAX pin-bus. On its CVAX pin-bus side, the CQBIC issues longword read/write, quadword read/write, and octaword write transactions to service scatter/gather map lookups and Q-bus transactions. Q-bus instruction types supported are DATI, DATIB, DATO, DATOB, DATIO, DATIOB, DATBO, and DATBI.

The CQBIC supports operation as both the Q-bus arbiter and a Q-bus auxiliary. The FQAM supports only operation as the Q-bus arbiter.

The CQBIC supports doorbell interrupt requests and Q-bus interrupt-acknowledge cycles.

For a detailed description of the chip's operation and the format of its control and status registers, see Appendix H, *CQBIC Specification,* in the *Firefox Designers' Guide.*

11.2.2.2. Busses

The CQBIC connects to both the C-bus and the Q-bus and forwards transactions between busses as appropriate. It also generates C-bus transactions to service caches misses to its scatter/gather map.

11.2.2.3. Interrupts

The CQBIC connects the Q-bus interrupt request signals to the C-bus interrupt request signals. The FBIC conditionally connects the C-bus interrupt request signals to the M-bus interrupt request signals. The CQBIC MEMERR signal connects to the FBIC device interrupt request signal (DEVIRQ<3>) to conditionally generate M-bus interrupts.

11.2.2.4. Reset

The CQBIC is reset when either MRESET or the FBIC RESET signal is asserted. During reset, the CQBIC tristates its I/O pins and initializes its internal registers.

11.2.2.5. CQBIC Address Map

Table 11-4 lists the addresses of the CQBIC control and status registers.

Table 11-4: CQBIC CSR Addresses

Name	M-Bus Address	VAX Address	Read/Write	Description
DBR0	80001F40#16	20001F40#16	Read/Write	Arbiter doorbell register
DBR1	80001F42#16	20001F42#16	Read/Write	Auxiliary #1 doorbell register
DBR2	80001F44#16	20001F44#16	Read/Write	Auxiliary #2 doorbell register
DBR3	80001F46#16	20001F46#16	Read/Write	Auxiliary #3 doorbell register
DBR4	80001F48#16	20001F48#16	Read/Write	Auxiliary #4 doorbell register
DBR5	80001F4A#16	20001F4A#16	Read/Write	Auxiliary #5 doorbell register
DBR6	80001F4C#16	20001F4C#16	Read/Write	Auxiliary #6 doorbell register
DBR7	80001F4E#16	20001F4E#16	Read/Write	Auxiliary #7 doorbell register
SCR	80080000#16	20080000#16	Read/Write	System configuration register
DSER	80080004#16	20080004#16	Read/Write	DMA system error register
MEAR	80080008#16	20080008#16	Read	DMA master error address register
SEAR	8008000C#16	2008000C#16	Read	DMA slave error address register
MAP_BASE	80080010#16	20080010#16	Read/Write	Scatter/gather-map base register
MAP_START	80088000#16	20088000#16	Read/Write	Start of scatter/gather map
MAP_END	8008FFFF#16	2008FFFF#16	Read/Write	End of scatter/gather map
Q22_IO_START	80000000#16	20000000#16	Read/Write	Q-bus I/O space start
Q22_IO_END	80001FFF#16	20001FFF#16	Read/Write	Q-bus I/O space end
Q22_MEM_START	90000000#16	30000000#16	Read/Write	Q-bus memory space start
Q22_MEM_END	903FFFFF#16	303FFFFF#16	Read/Write	Q-bus memory space end

11.2.3. Clocks

The FQAM requires the following clocks:

- 10-MHz, two-phase clocks for the FBIC
- 40-MHz clock for the CQBIC

The CVAX Clock chip (CCLOCK) supplies the two-phase clock to the FBIC. It also provides synchronization for the CRDY and CERR signals, thus allowing the CQBIC chip to operate asynchronously.

A single oscillator will be used to generate the 40-MHz and 10-MHz clocks.

11.2.4. Status Indicators

The FBIC status indicator outputs drive 4 red and 1 green LED indicators mounted at the FQAM module edge.

11.2.5. Bus Driver-Disable Circuit

A driver-disable circuit is implemented in the FQAM to prevent damage to a module inadvertently plugged into a wrong slot. The FQAM will disable its M-bus drivers when it is not in M-bus slots 0-7 and disable the Q-bus drivers when its not in M-bus slot 0. Likewise, all other M-bus modules implement similar circuits to disable their drivers if they are not in their designated slots.

11.3. Programming

In this section, required initialization of the FQAM is described and some programming guidelines are listed. The examples used herein are based on an FQAM in M-bus slot 0; all addresses are VAX physical addresses.

11.3.1. Locating Modules

After a workstation reset (M-bus MRESET asserted), console and diagnostic software must determine the workstation configuration. The FBIC saves, in its BUSCTL register, the value of the M-bus MBRQ signals during MRESET. Software can use this as a module-present indication to identify backplane M-bus slots that contain Firefox modules. To interpret the BUSCTL<MBRM> bits, a module must first determine its own M-bus slot by reading its FBIC CPUID<MID> register field. Table 11-5 lists the interpretation of BUSCTL<MBRM> as a function of a module's M-bus slot (from its CPUID<MID>). Software must use or save the value of BUSCTL<MBRM> before it enables FBIC error logging, or the information will be lost.

Table 11-5: Interpretation of FBIC BUSCTL<MBRM> Field

CPUID<MID>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
0	7	6	5	4	3	2	1
1	7	6	5	4	3	2	0
2	7	6	5	4	3	1	0
3	7	6	5	4	2	1	0
4	7	6	5	3	2	1	0
5	7	6	4	3	2	1	0
6	7	5	4	3	2	1	0
7	6	5	4	3	2	1	0

For example, if a module reads its CPUID<MID> register field and obtains 4, it is in M-bus slot 4. If it then reads its BUSCTL<6:0> register field and obtains 1011001#2, there are modules in M-bus slots 0, 3, 5, and 7.

To confirm the presence of a module in each slot, software should read the MODTYPE register of each of those slots. In the example just given, the MODTYPE registers would be at VAX addresses 31FFFFFC#16, 37FFFFFC#16, 3BFFFFFC#16, and 3FFFFFFC#16. Reading the FQAM's MODTYPE register will return the value 01010001. FQAM ROM should have a known location that more precisely identifies it as the FQAM.

11.3.2. Addressing

The CQBIC registers and scatter/gather map are at fixed addresses as defined by the CQBIC. Because the FQAM can only be in M-bus slot 0, the FBIC base address is always 30000000#16.

11.3.3. Initialization

After workstation reset (M-bus MRESET asserted), the FQAM requires initialization of the FBIC before normal operation can commence. Software must generate the following register writes:

1. MOVL FFFFFFFF#16 (31FFFFF8#16), to write the FBIC BUSCSR register to enable error logging.
2. MOVL 00FF003E#16 (31FFFFE8#16), to write the FBIC FBICSR register to connect the CVAX pin-bus CIRQ signals to the M-bus MIRQ signals for CQBIC interrupts and enter normal operating mode.
3. MOVL 80088008#16 (31FFFFE4#16), to write the FBIC RANGE register to make the CQBIC accessible.
4. MOVL 0002VVVV#16 (31FFFFE0#16), to write the FBIC IPDVINT register to enable device interrupts from CQBIC memory errors, where VVVV is the desired interrupt vector.

11.3.4. FQAM Module Restriction

Because of the electrical connection between the M-bus and Q-bus on the backplane, only one FQAM is allowed in a Firefox Workstation system.

11.3.5. FQAM ROM

The FQAM ROM is intended for FQAM self-test code and workstation Q-bus disk/tape/network bootstrap code. Access to the ROM from other modules is relatively slow, typically two microseconds per access. It is recommended that frequently used or time-critical code be copied to memory.

11.3.6. FQAM Access Restrictions

Because of a CQBIC implementation constraint, operating system software must restrict access to the Q-bus and CQBIC to a single processor. Interlock transactions to the FQAM are not supported, except those to the FBIC registers.