

# WC\_BRD2 Design

**\* IMPORTANT NOTICE \***

This schematic set has not been officially released by CXO Storage Subsystems engineering.

Information described within is subject to change without notice.

ALL SCHEMATIC PAGES

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55							

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REVISIONS		
CHK	CHANGE NO.	REV

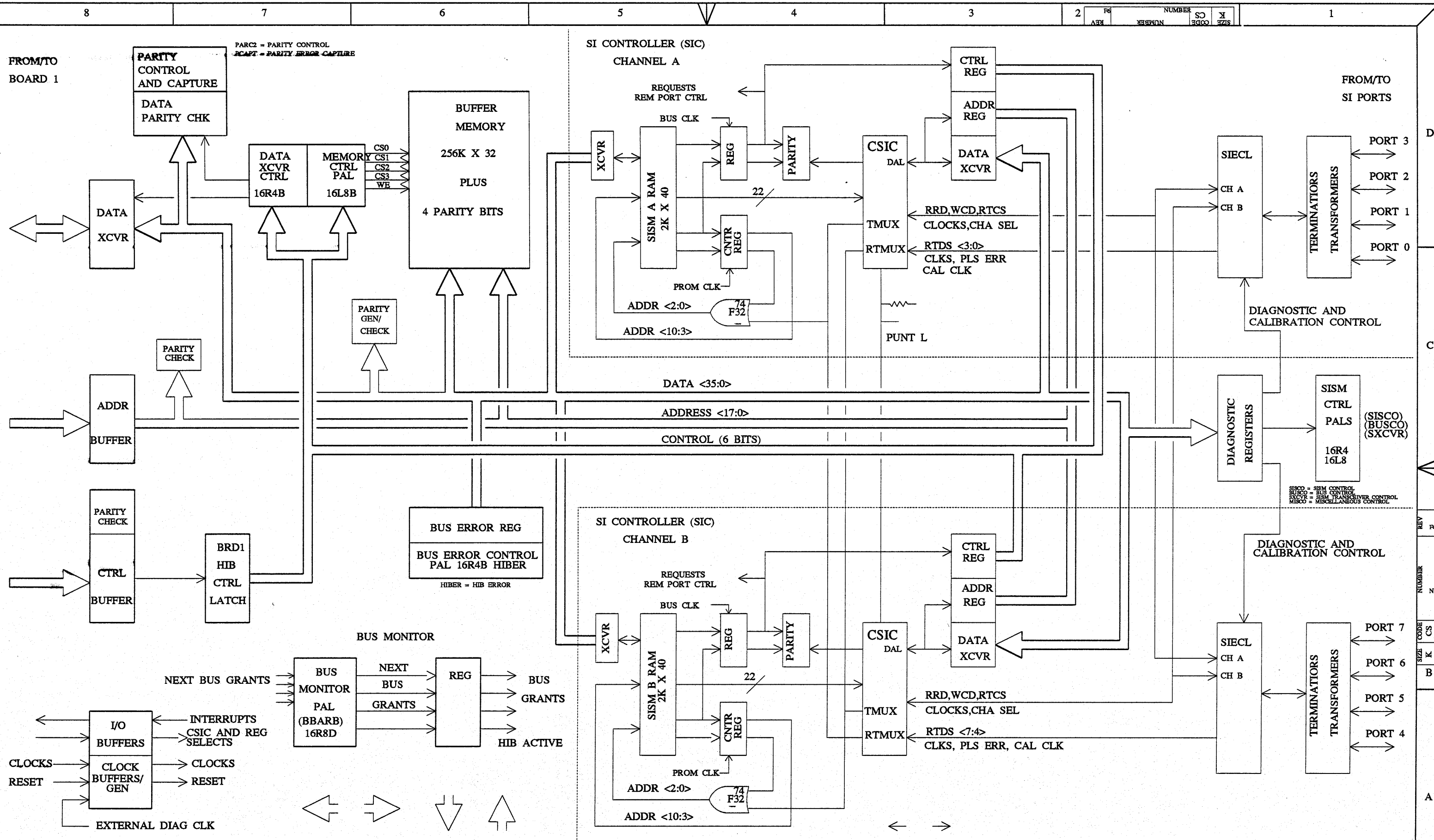
**digital**

LOGIC\_NAME = LOGIC SHEET NAME  
FIRST USED ON OPTION/MODEL:

DRN: Taskmaster	DATE	ENG: T. Nerger	DATE
CHK'D:	DATE	BOARD LOCATION: NAME	SHEET 1
NEXT HIGHER ASSEMBLY: NAME		SIZE K	CODE CS

TITLE: DRAWING TITLE
NUMBER CXO49
REV A1_21

SIZE K	CODE CS	NUMBER CXO49	REV A1_21
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CHK	CHANGE NO.	REV

# BOARD 2 BLOCK DIAGRAM

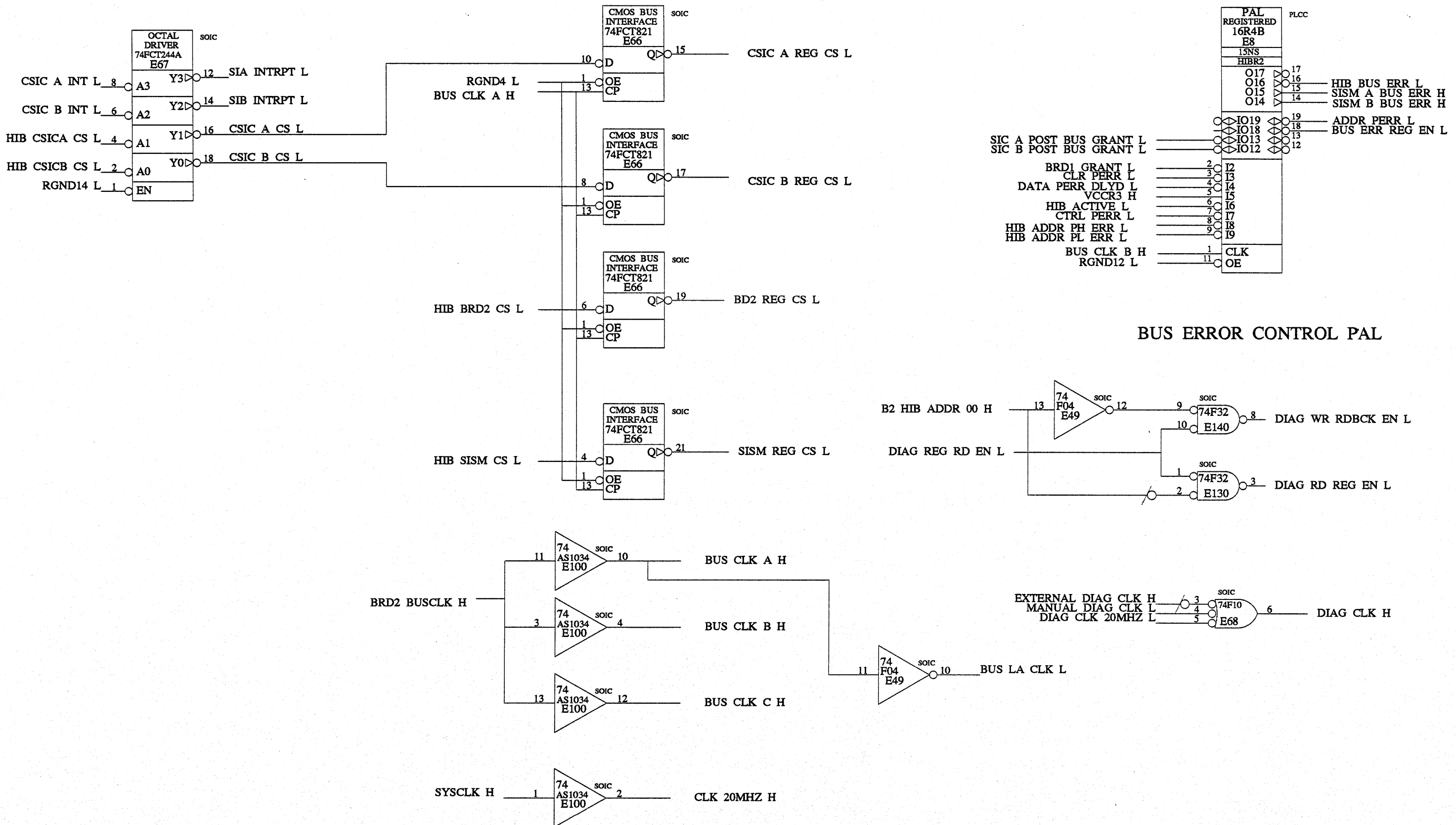
**digit**  
 DWG.LOGIC.1.2  
 FIRST USED ON OPTION/MODEL: NUMBER

DRN: T. Nerger  
 CHK'D: T. Nerger  
 DATE DA/MON/YR  
 Mon Oct 17 15:47:47 1988

ENG: NERGER  
 BOARD LOCATION: NAME  
 SHEET 2  
 NEXT HIGHER ASSEMBLY: NAME

DATE 20-MAY-88

TITLE: BOARD 2 BLOCK DIAGRAM			
SIZE	CODE	NUMBER	REV
K	CS	CXO62	WC



**BUS ERROR CONTROL PAL**

**CLOCK AND I/O BUFFERS**

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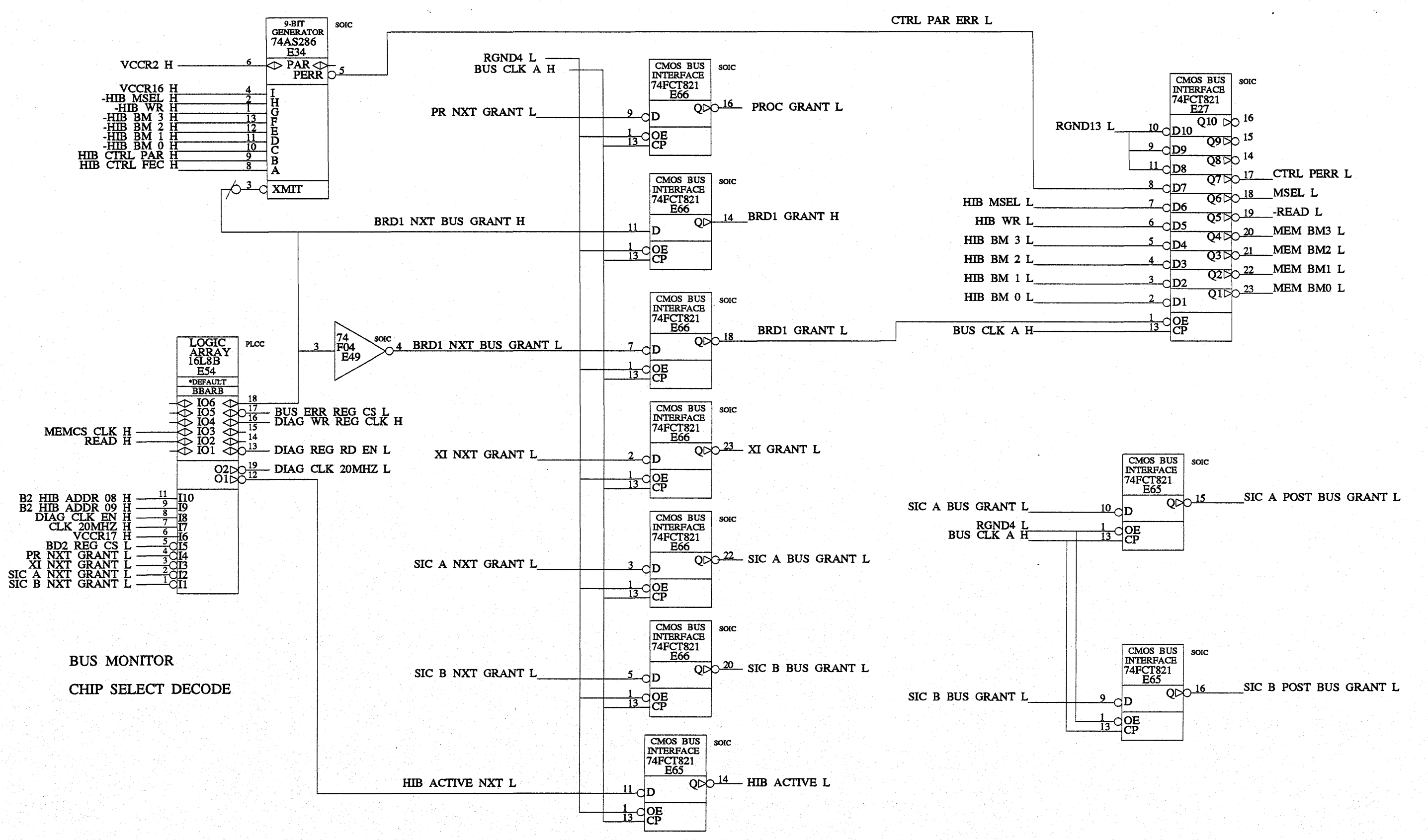
REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**CLOCK &  
 I/O BUFFERS**

**digital**  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D: -	DATE	BOARD LOCATION: CXO	SHEET 3	SIZE K
Mon Oct 17 15:51:07 1988		NEXT HIGHER ASSEMBLY: -	NUMBER CXO62	REV 17OCT88

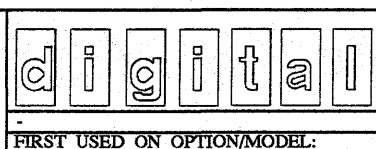
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88
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REVISIONS		
CHK	CHANGE NO.	REV

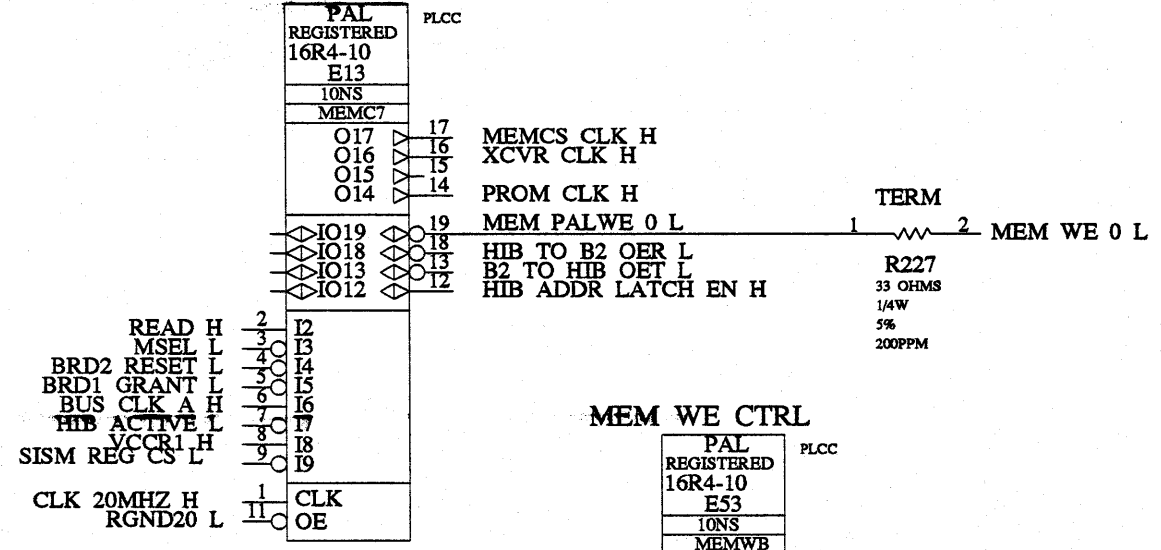
[Logic]  
**BUS MONITOR,  
 BIC & HIB CTRL SIGNALS**



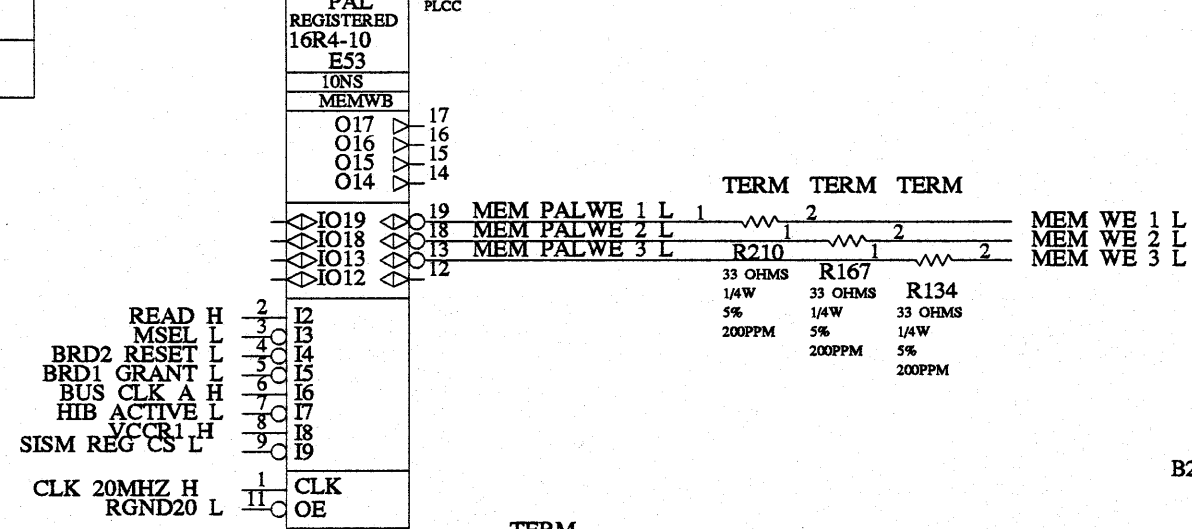
DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D: -	DATE	BOARD LOCATION: CXO	
FIRST USED ON OPTION/MODEL: Mon Oct 17 16:00:44 1988		SHEET 4	NEXT HIGHER ASSEMBLY:

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 170CT88

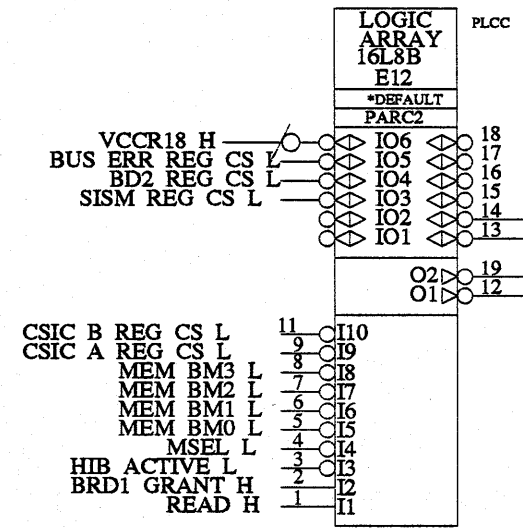
MEM/DATA CTRL 1



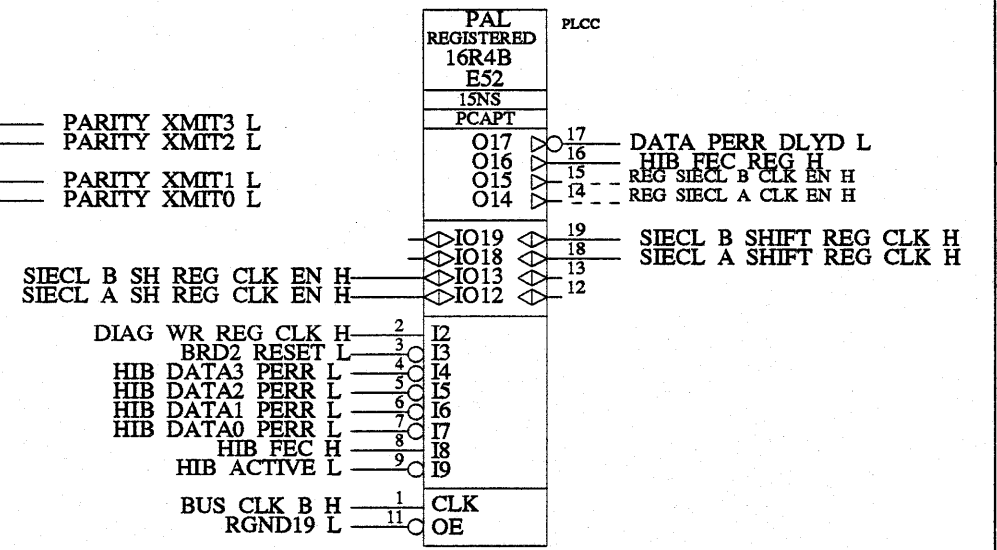
MEM WE CTRL



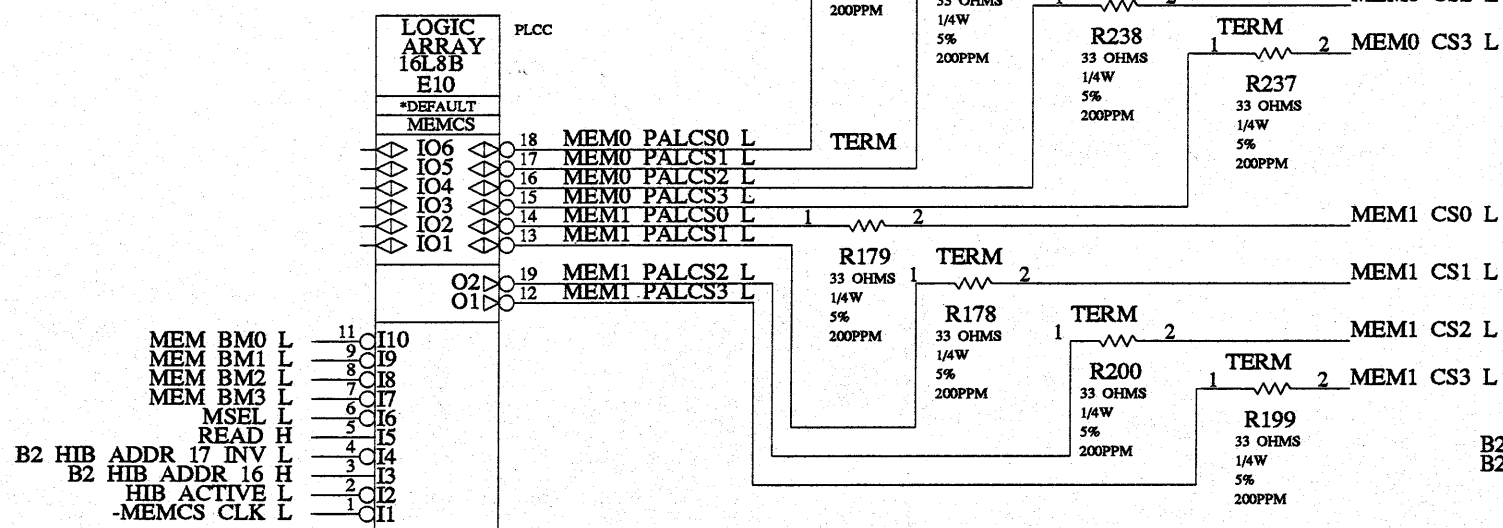
PARTY CHECKER CONTROL



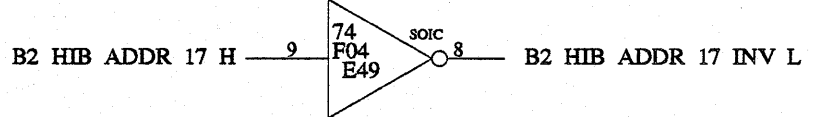
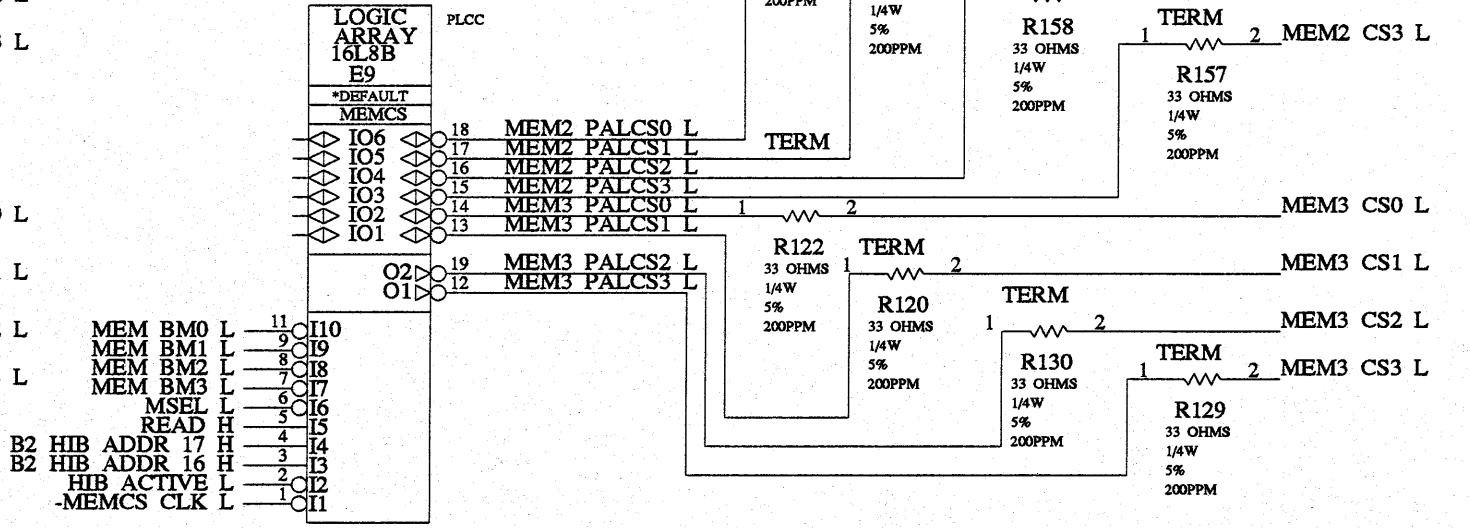
PARITY ERROR CAPTURE



MEM/DATA CTRL 2  
MEMORY CHIP SELECT GENERATOR



MEM/DATA CTRL 2  
MEMORY CHIP SELECT GENERATOR



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CHK	CHANGE NO.	REV

[Logic]  
**RAM CTRL,  
HIB XCVR CTRL,  
HIB PAR CKT**

**digital**  
FIRST USED ON OPTION/MODEL: -

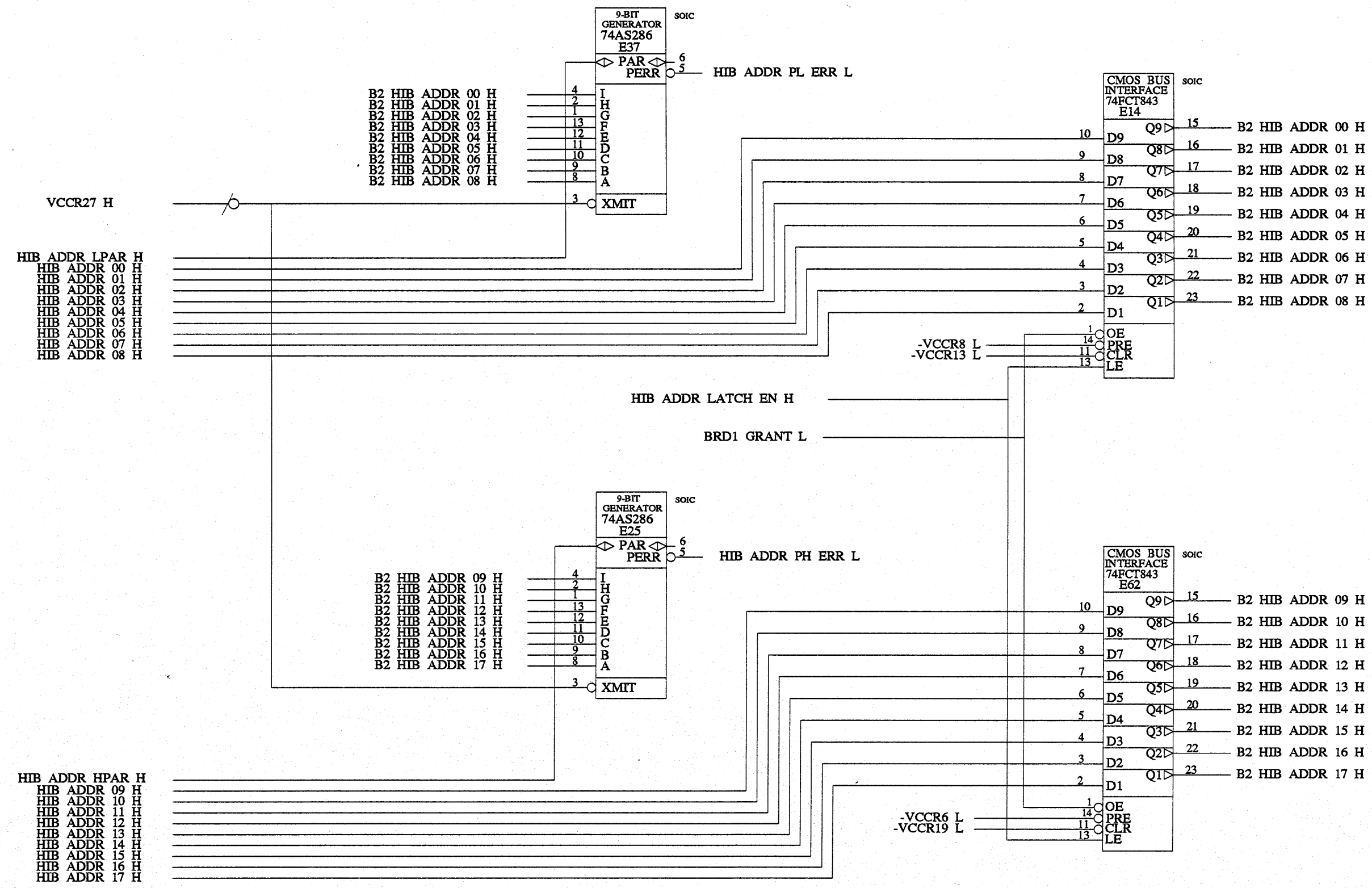
DRN: T. Nerger  
CHK'D: -  
DATE: -  
DATE: -  
Tue Oct 25 16:43:10 1988

ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET 5  
NEXT HIGHER ASSEMBLY: -

TITLE: **WILDCAT BOARD 2**  
SIZE K  
CODE CS  
NUMBER NUMBER  
REV 25OCT88

D  
C  
B  
A

D  
C  
B  
A



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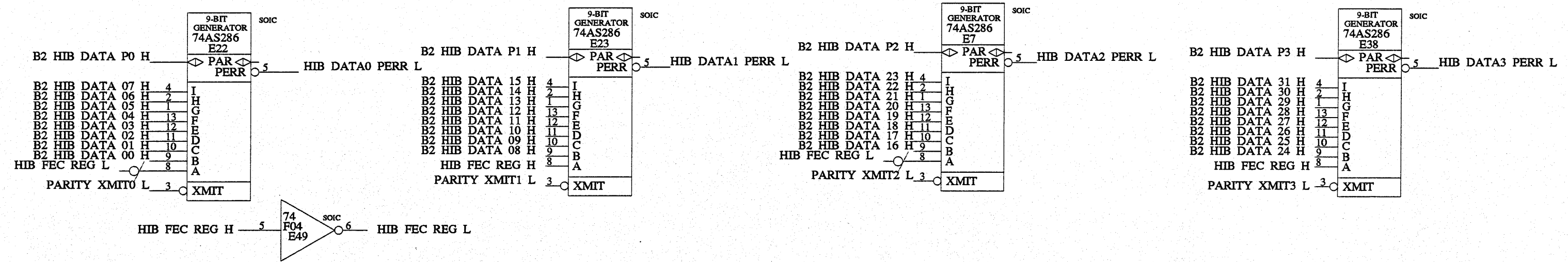
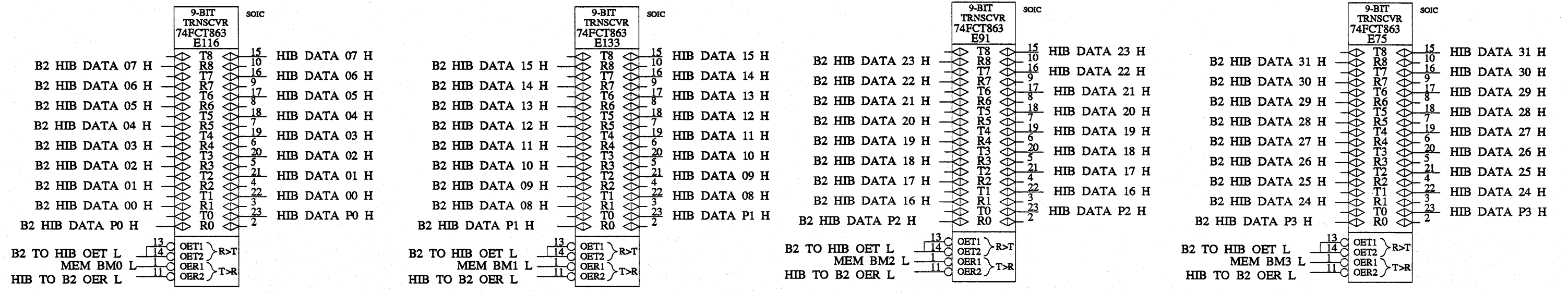
REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**HIB ADDR LATCHES & PAR CHK**

**digital**  
FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D:	DATE	BOARD LOCATION: CXO	TITLE: WILDCAT BOARD 2
Mon Oct 17 16:04:57 1988		SHEET 6	NEXT HIGHER ASSEMBLY:

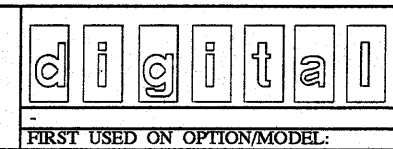
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88
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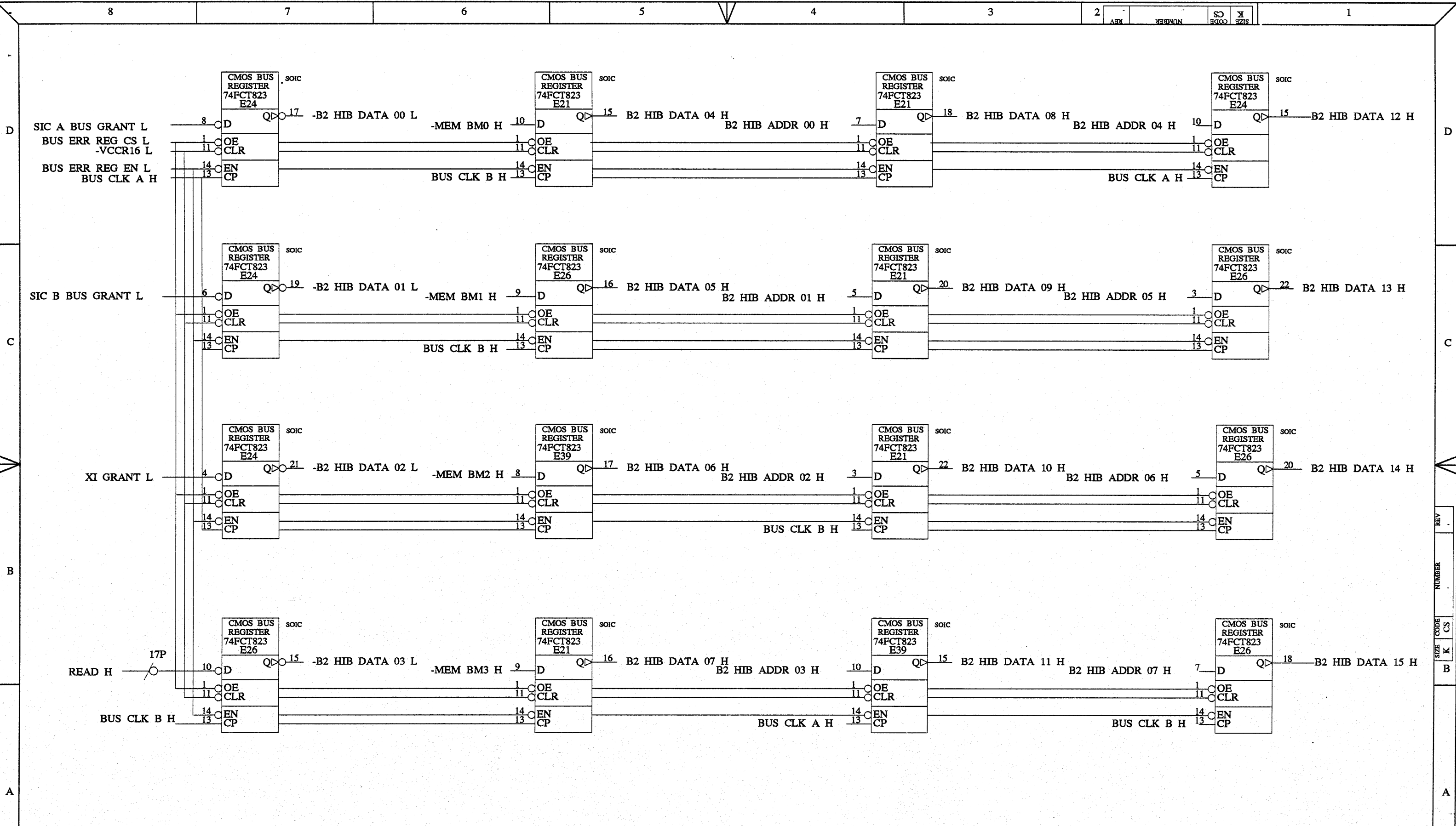
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CHK	CHANGE NO.	REV

[Logic]  
**HIB DATA BUFFER,  
 HIB PAR GENERATORS &  
 CHECKERS**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 7	SIZE K CODE CS NUMBER CXO62 REV 25OCT86
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY:		



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**LOWER WORD,  
 BUS ERR REG**

**digital**  
 DRN: T. Nerger  
 DATE: Mon Oct 17 16:10:11 1988  
 FIRST USED ON OPTION/MODEL: -

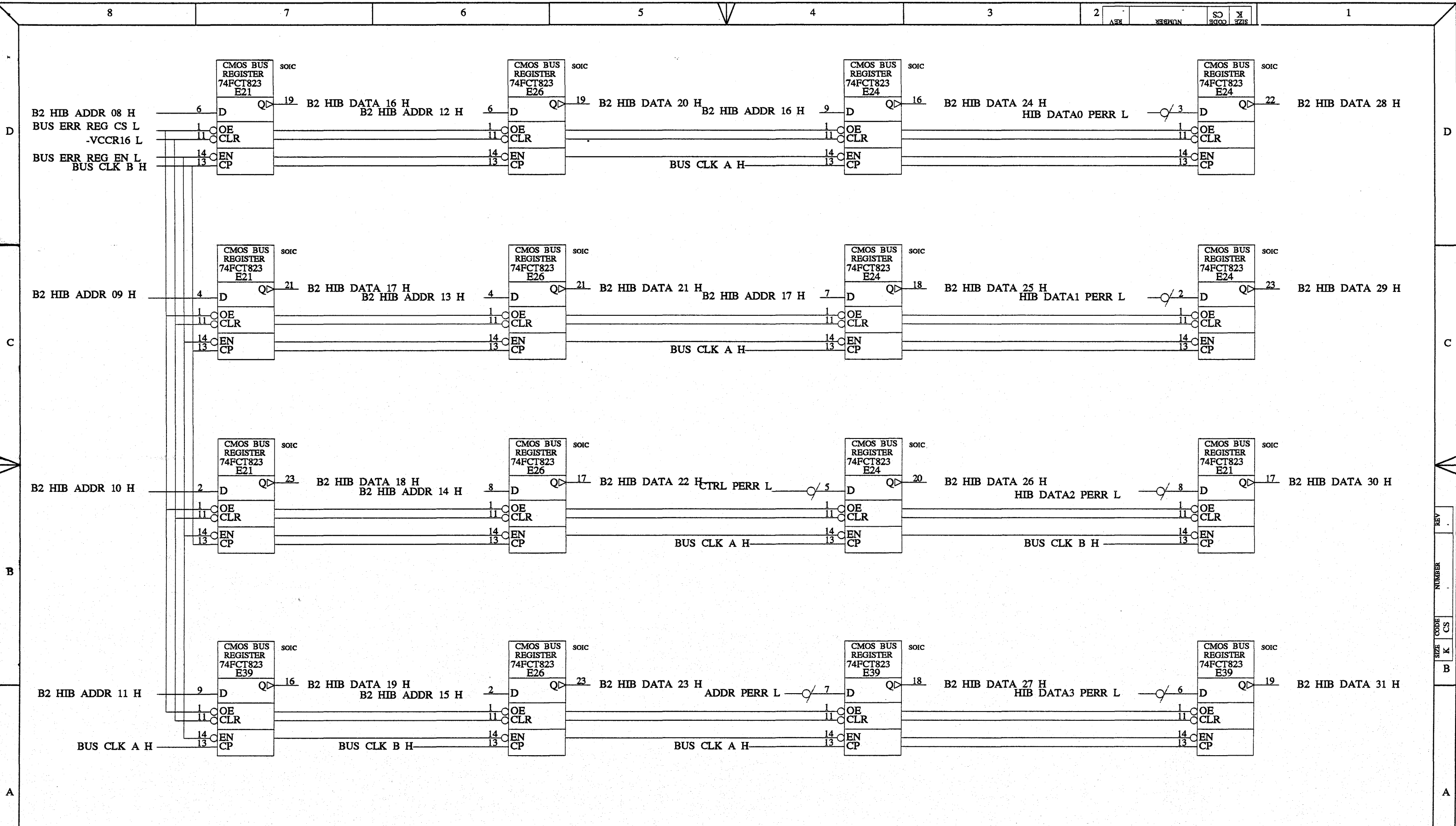
ENG: T. Nerger	DATE: -
CHK'D: -	DATE: -

ENG: T. Nerger	DATE: -
BOARD LOCATION: CXO	SHEET: 8
NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 2			
SIZE: K	CODE: CS	NUMBER: CX062	REV: 170CT88

REV NUMBER

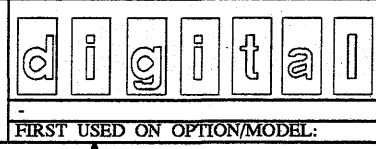




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[Logic]  
**UPPER WORD,  
 BUS ERR REG**

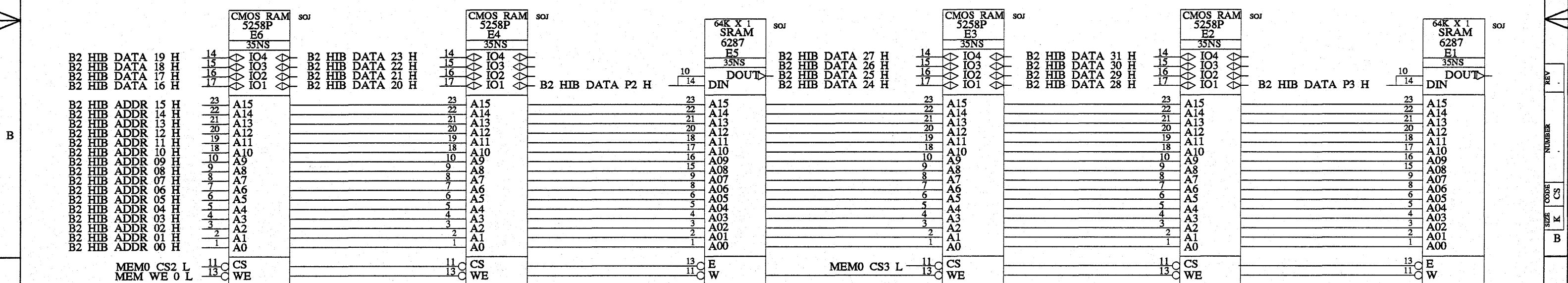
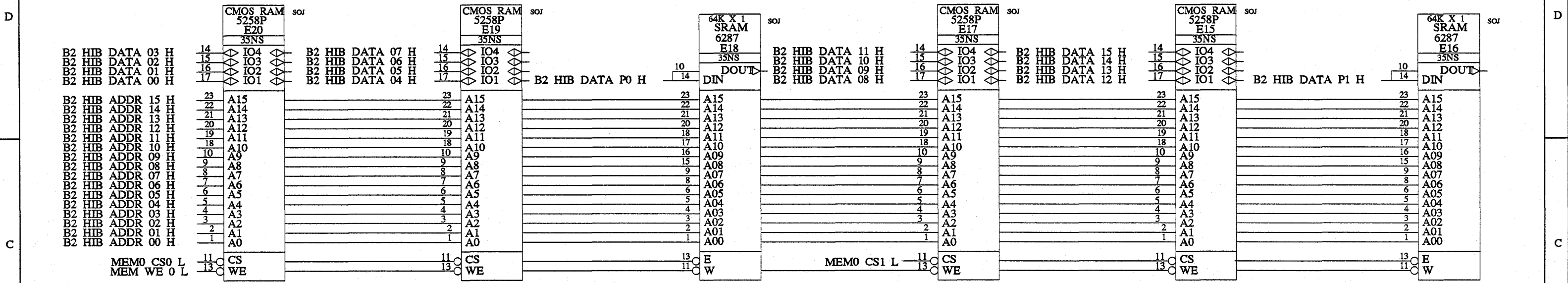


DRN: T. Nerger  
 DATE: -  
 CHK'D: -  
 DATE: -  
 FIRST USED ON OPTION/MODEL: -

ENG: T. Nerger  
 DATE: -  
 BOARD LOCATION: CXO  
 SHEET: 9  
 NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88

REV NUMBER



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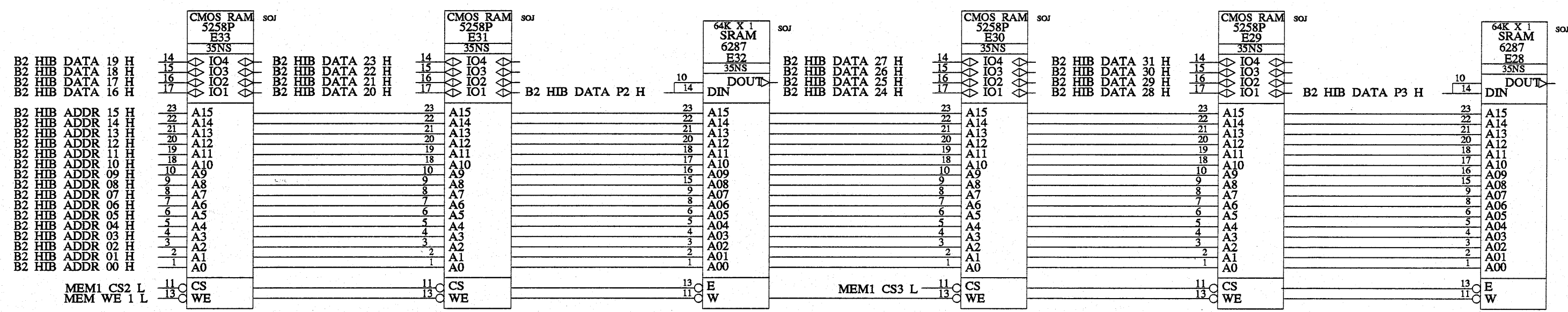
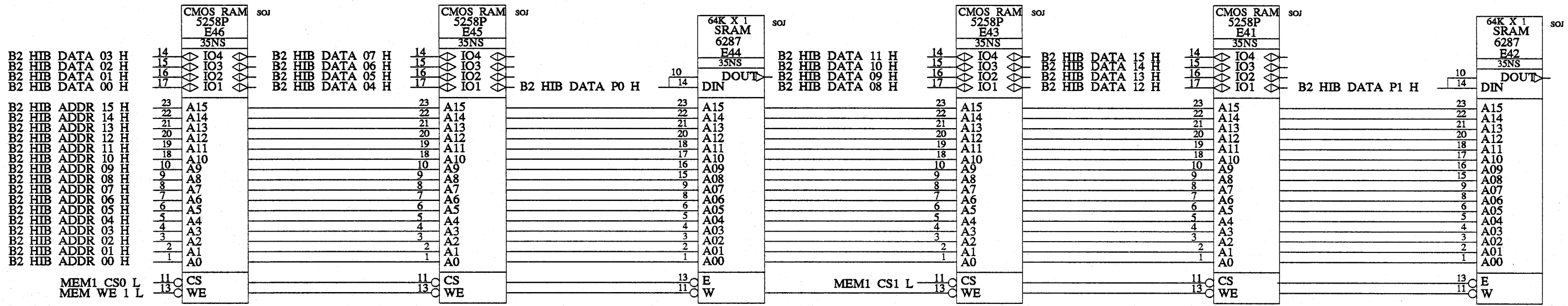
REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**STATIC RAMS  
 BANK 0**

**digital**

DRN: T. Nerger  
 DATE: -  
 ENG: T. Nerger  
 DATE: -  
 BOARD LOCATION: CXO  
 SHEET: 10  
 NEXT HIGHER ASSEMBLY: -  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE: -	ENG: T. Nerger	DATE: -	TITLE: WILDCAT BOARD 2
CHK'D: -	DATE: -	BOARD LOCATION: CXO	SHEET: 10	SIZE: K
				CODE: CS
				NUMBER: CXO62
				REV: 17OCT88



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CHK	CHANGE NO.	REV

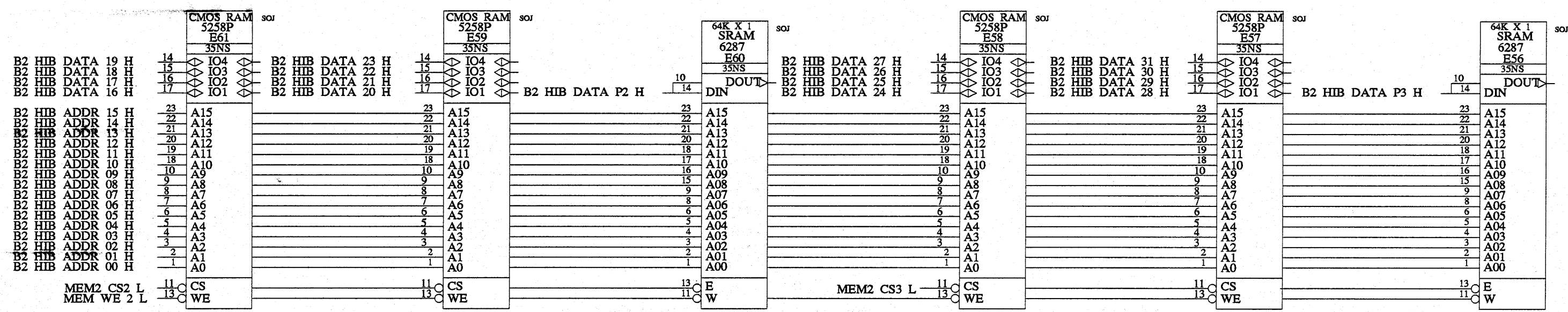
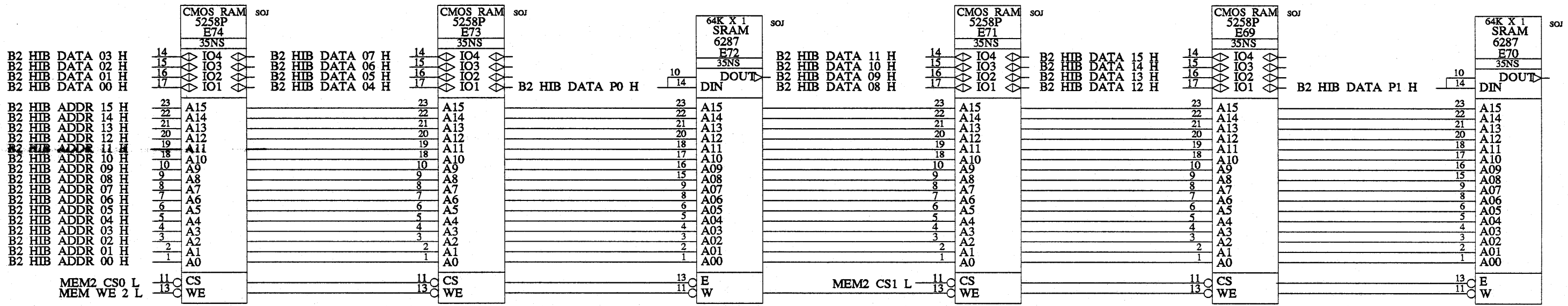
[Logic]  
**STATIC RAMS  
 BANK 1**

**digital**

DRN: T. Nerger  
 DATE: -  
 CHK'D: -  
 DATE: -  
 FIRST USED ON OPTION/MODEL: -

ENG: T. Nerger	DATE: -	TITLE: WILDCAT BOARD 2
BOARD LOCATION: CXO	SHEET: 11	SIZE: K
NEXT HIGHER ASSEMBLY: -	NUMBER: CXO62	CODE: CS

REV: 17OCT88	NUMBER: CXO62	CODE: CS	SIZE: K
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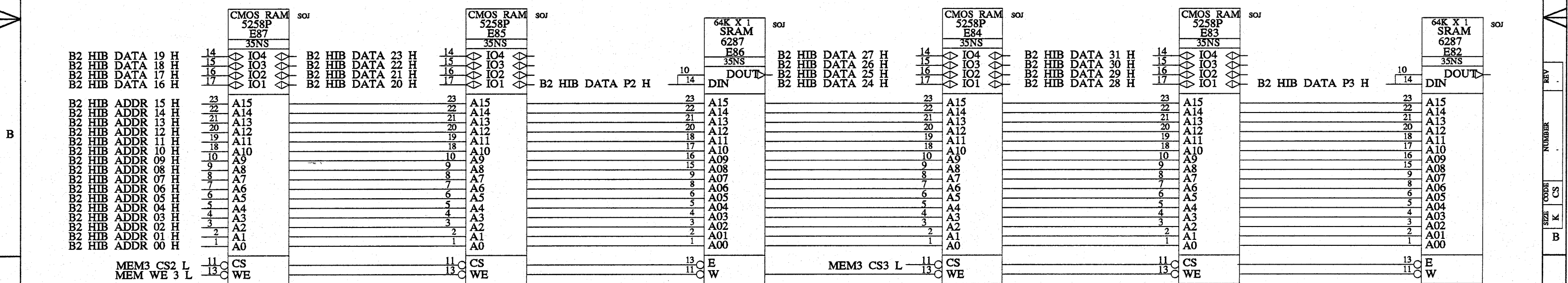
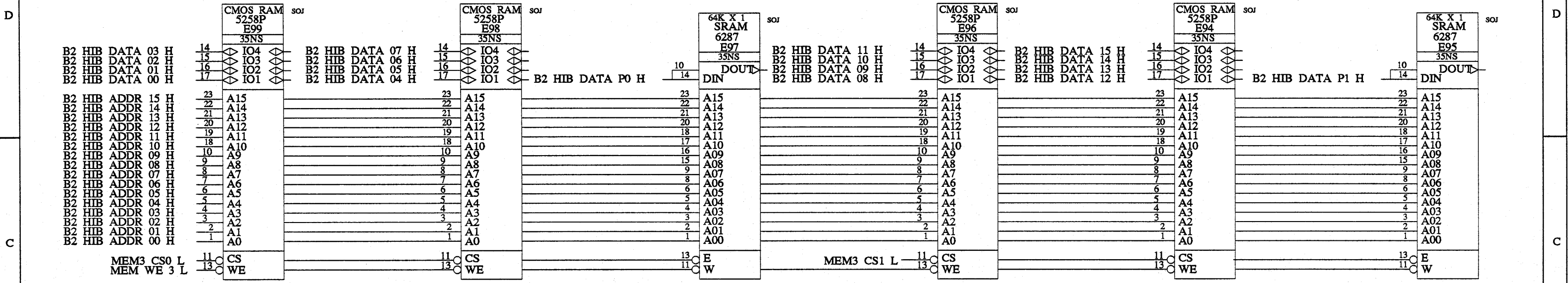
[Logic]  
**STATIC RAMS  
 BANK 2**

**digital**

DRN: T. Nerger  
 DATE: -  
 CHK'D: -  
 DATE: -  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE: -	ENG: T. Nerger	DATE: -
CHK'D: -	DATE: -	BOARD LOCATION: CXO	TITLE: WILDCAT BOARD 2
Mon Oct 17 15:43:58 1988		SHEET 12	NEXT HIGHER ASSEMBLY: -

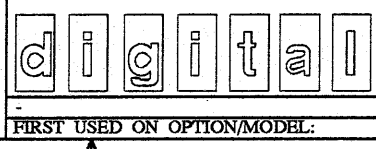
SIZE K	CODE CS	NUMBER CXO49	REV 17OCT88
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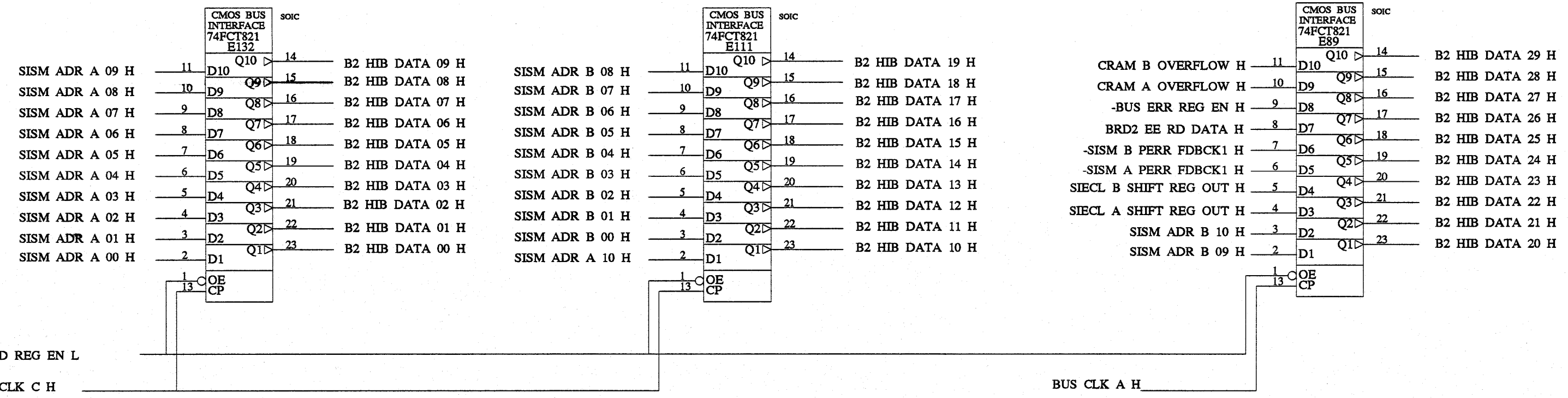
[Logic]  
**STATIC RAMS  
BANK 3**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 13
Mon Oct 17 15:45:02 1988		NEXT HIGHER ASSEMBLY:	

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88

### READ DIAG REGS



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**DIAGNOSTIC REGISTERS**

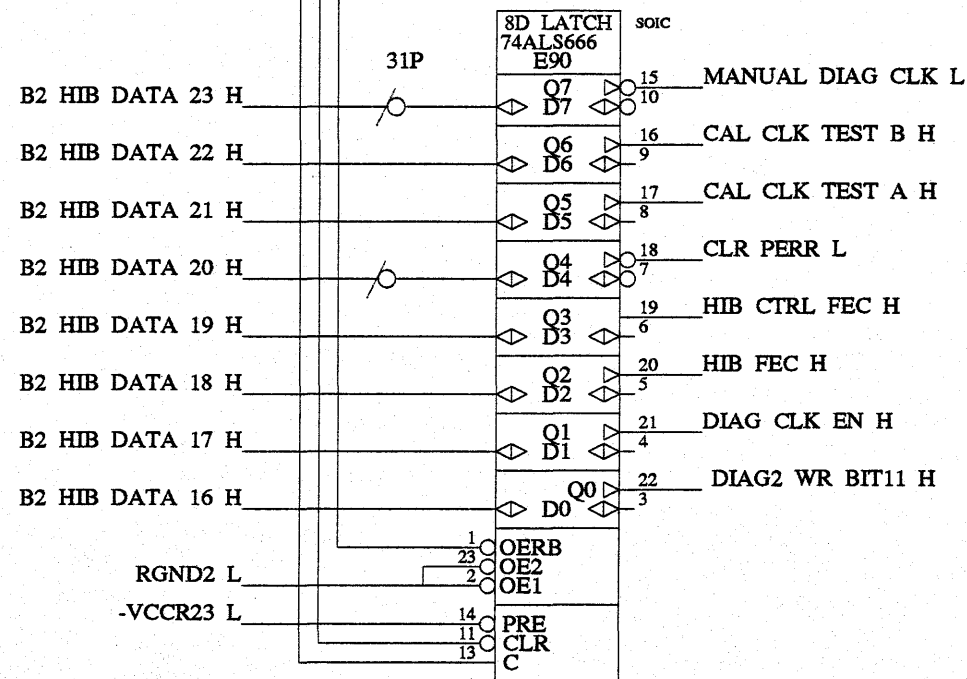
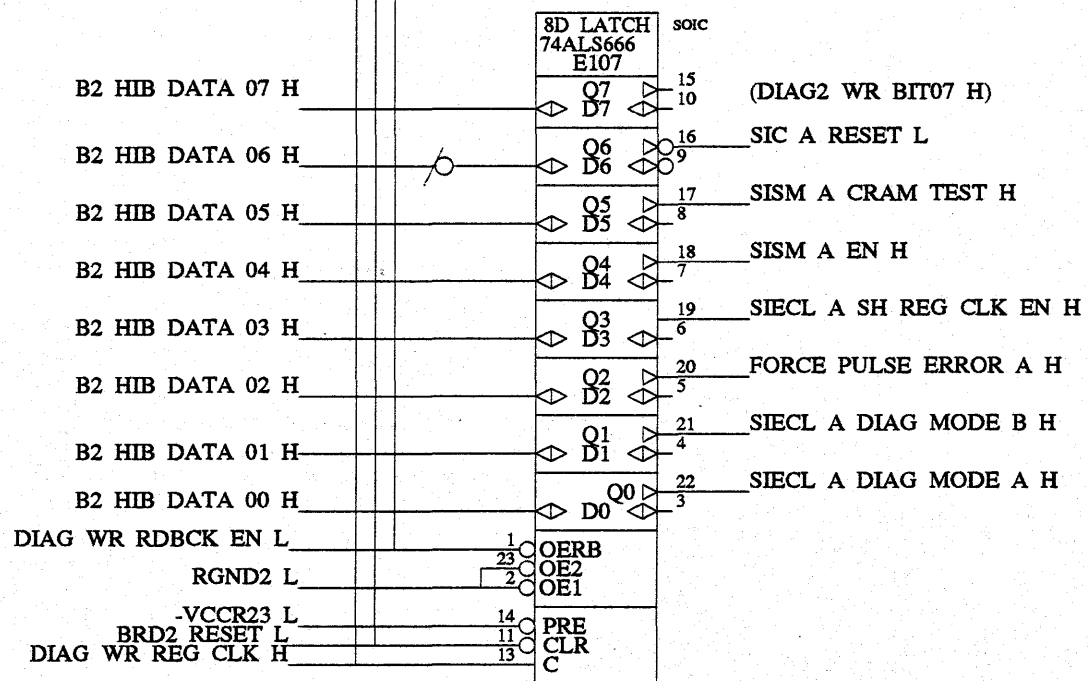
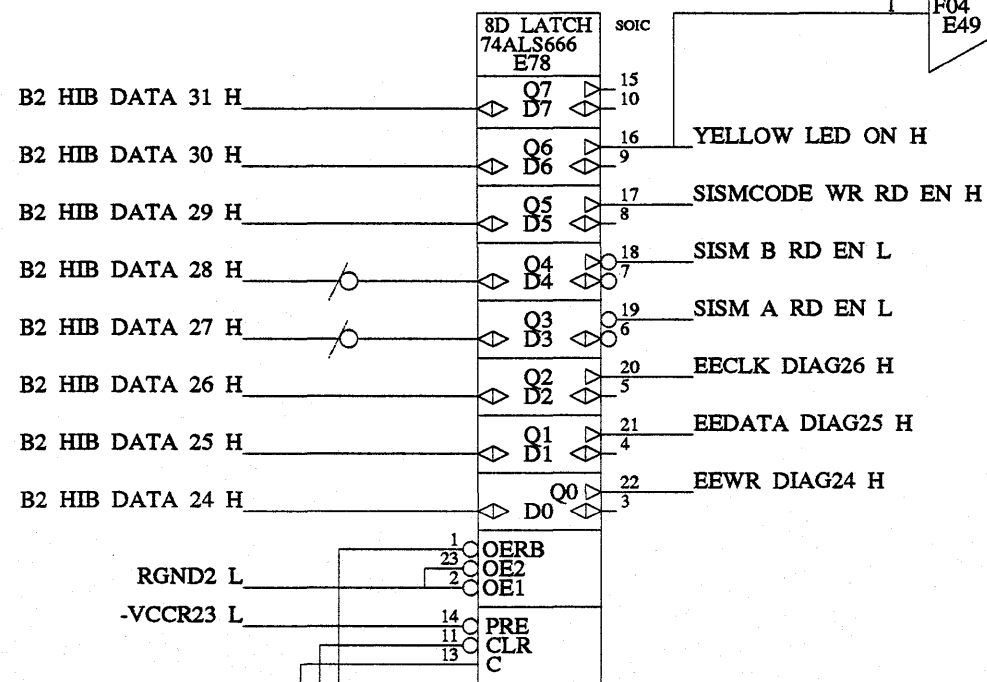
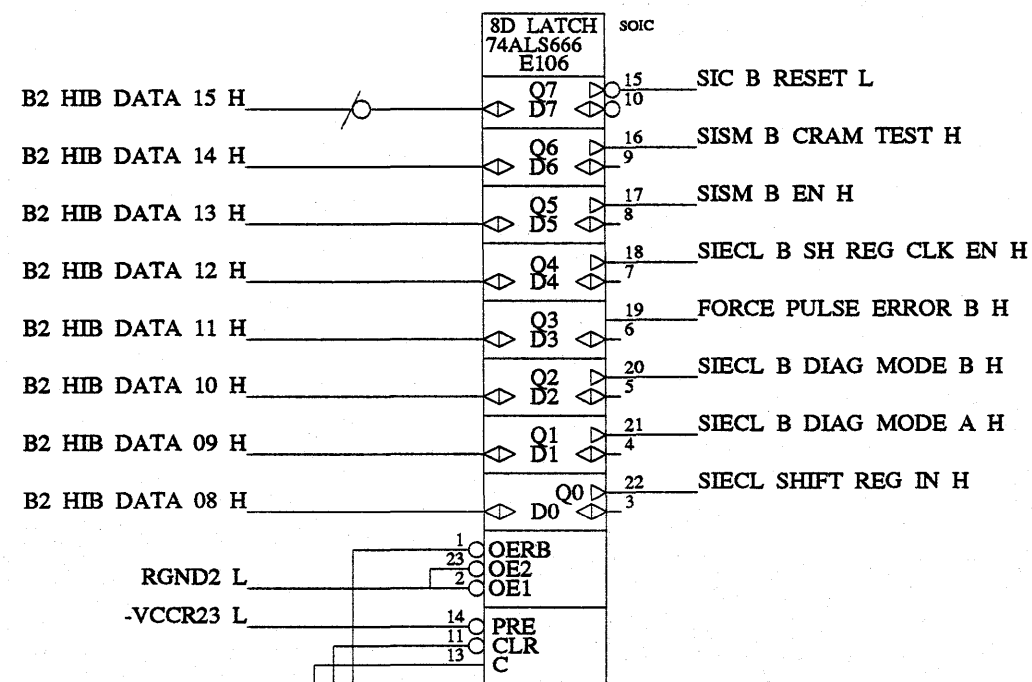
**digital**  
FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger  
CHK'D: -  
DATE: -  
DATE: -  
Mon Oct 17 15:45:19 1988

ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET 14  
NEXT HIGHER ASSEMBLY: -

TITLE: **WILDCAT BOARD 2**  
SIZE K  
CODE CS  
NUMBER CXO62  
REV 17OCT88

# WRITE DIAG REGS



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic] **DIAGNOSTIC REGISTERS**

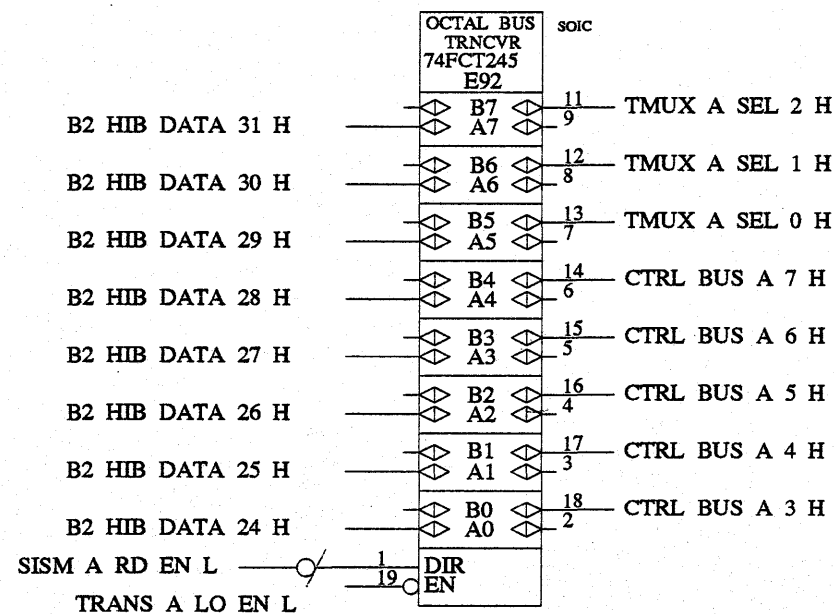
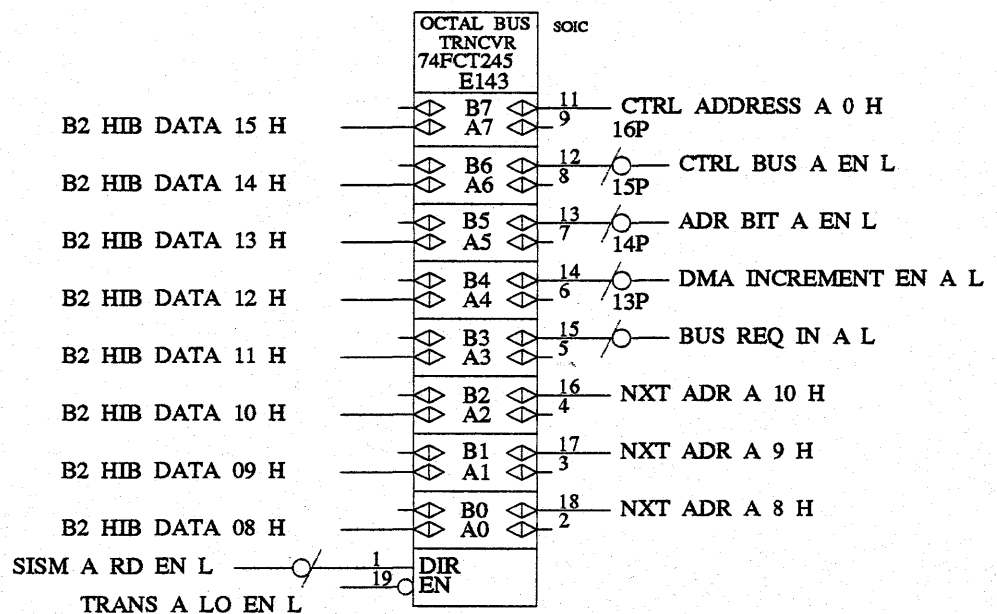
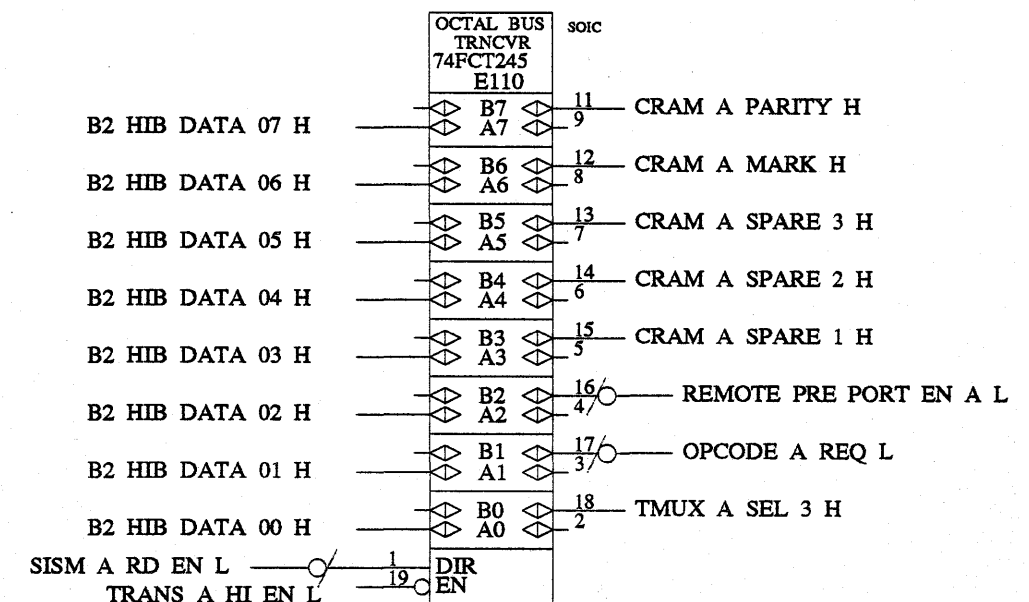
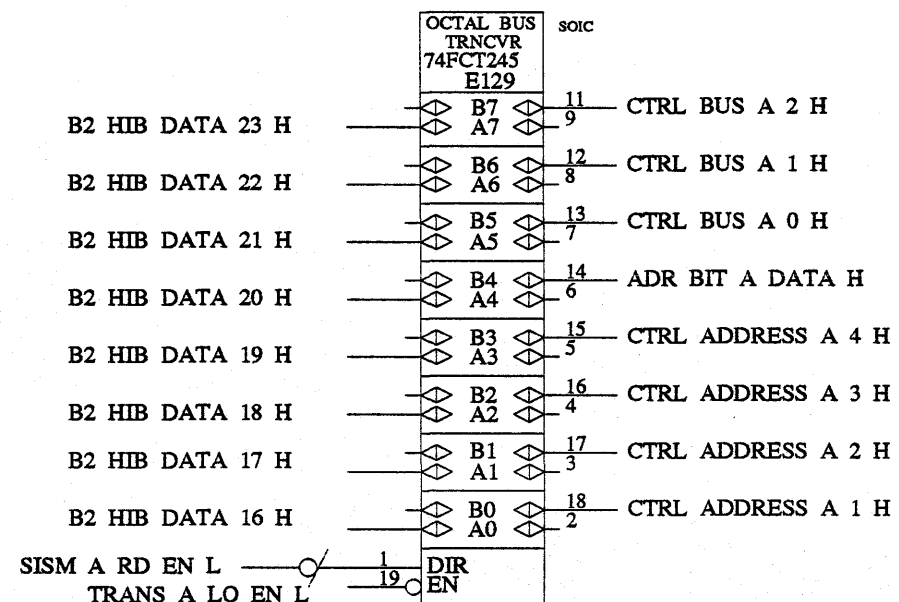
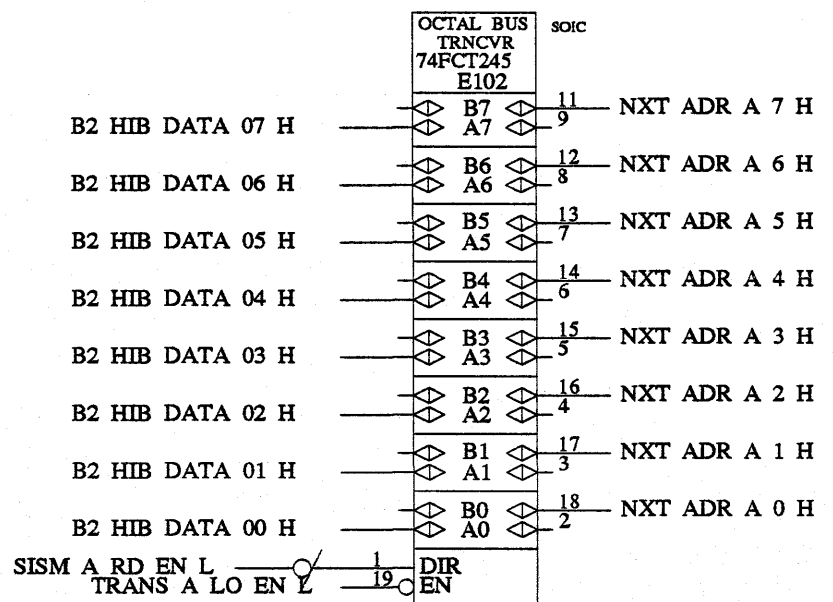


DRN: T. Nerger  
 DATE: -  
 CHK'D: -  
 DATE: -  
 Mon Oct 17 15:45:35 1988

ENG: T. Nerger  
 DATE: -  
 BOARD LOCATION: CXO  
 SHEET: 15

TITLE: **WILDCAT BOARD 2**  
 NEXT HIGHER ASSEMBLY: -

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88



USED FOR LOADING SISM RAMS

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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SISM A DATA XCVRS**

**digital**

DRN: J. LYLE DATE: - ENG: J. LYLE DATE: - TITLE: WILDCAT BOARD 2

CHK'D: - DATE: - BOARD LOCATION: CXO SHEET: 16

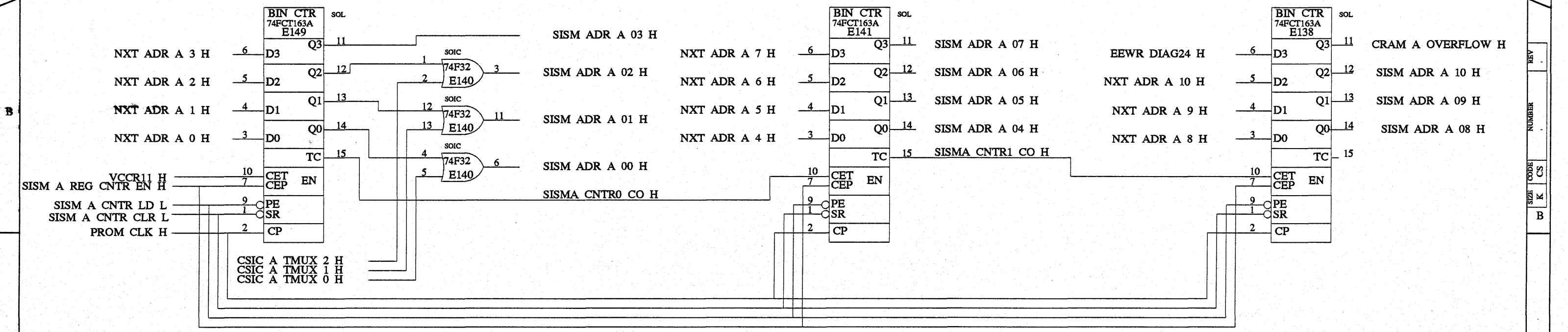
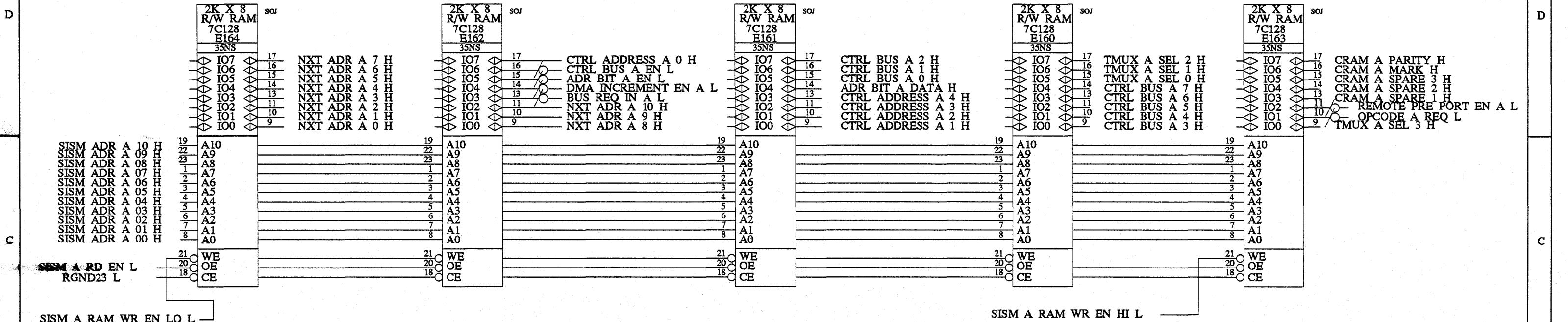
Mon Oct 17 15:45:56 1988

NEXT HIGHER ASSEMBLY: -

FIRST USED ON OPTION/MODEL: -

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

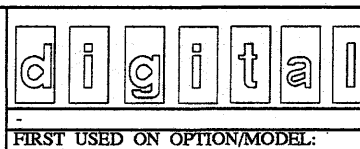




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REVISIONS		
CHK	CHANGE NO.	REV

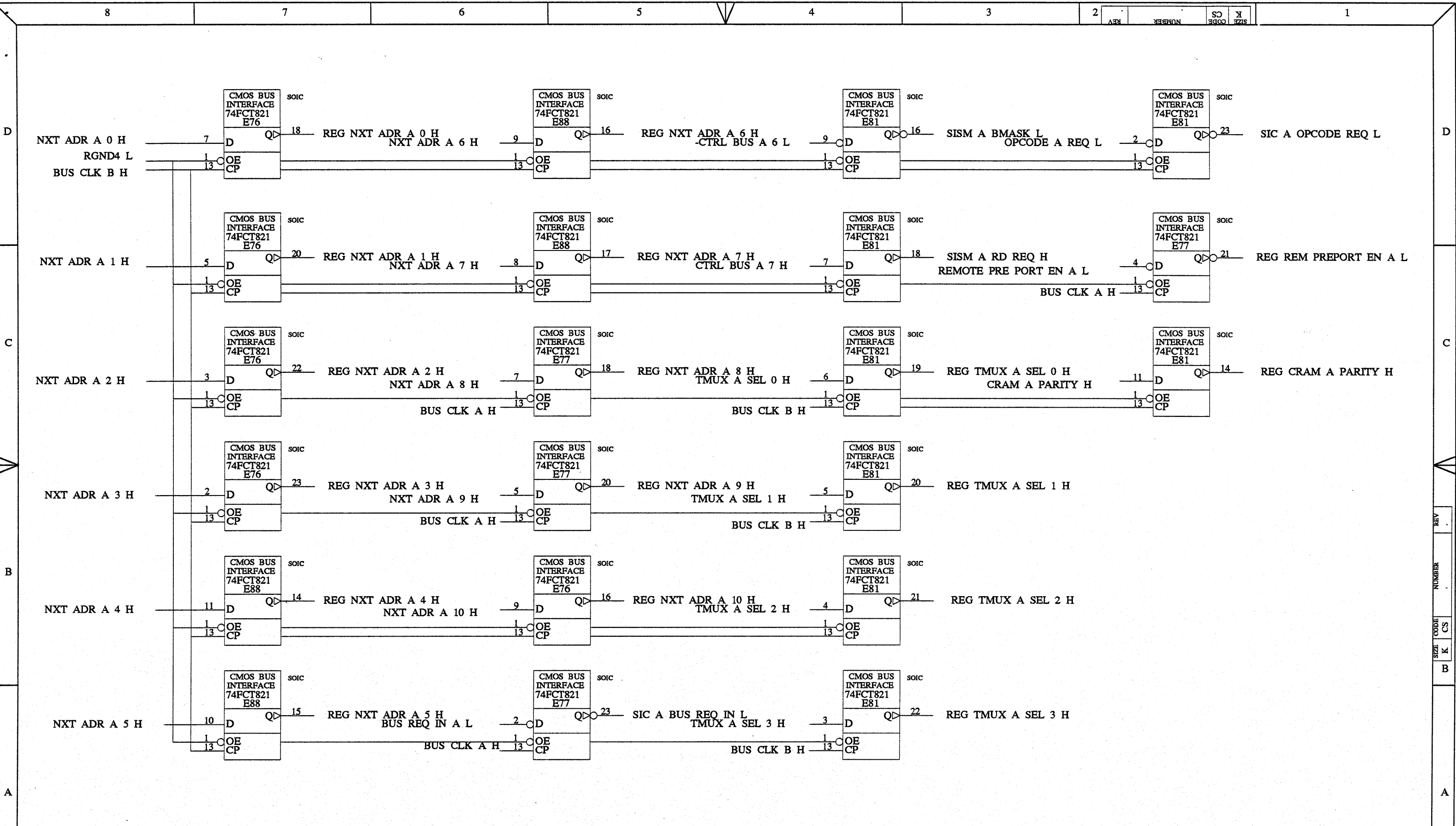
[Logic]  
**SI CHAN A STATE MACHINE**



DRN: T. Nerger  
 DATE: -  
 ENG: T. Nerger  
 DATE: -  
 BOARD LOCATION: CXO  
 SHEET: 17  
 NEXT HIGHER ASSEMBLY: -  
 FIRST USED ON OPTION/MODEL: -  
 Tue Oct 18 06:42:40 1988

TITLE:  
**WILDCAT BOARD 2**

SIZE	CODE	NUMBER	REV
K	CS	CX062	170CT88



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SI CHAN A STATE MACHINE  
 REGISTERS**

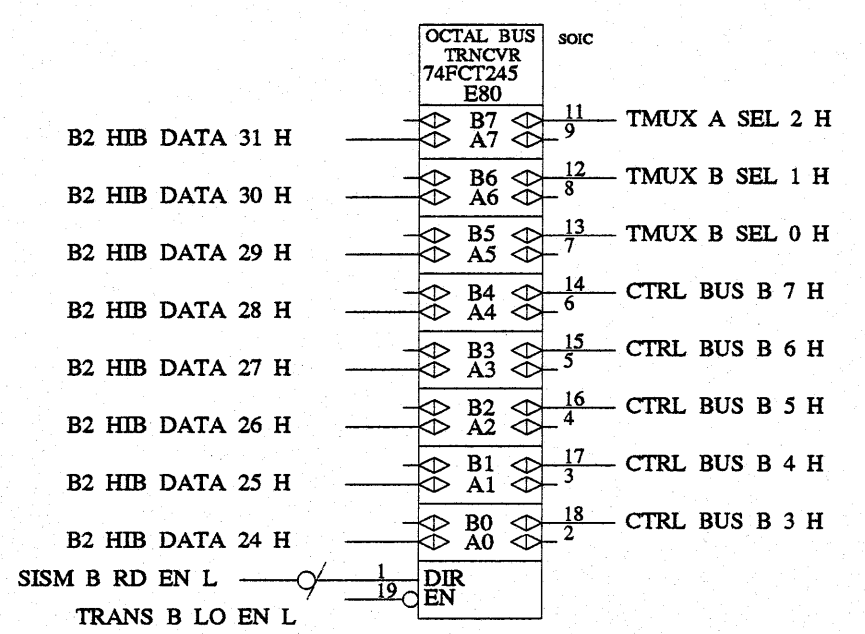
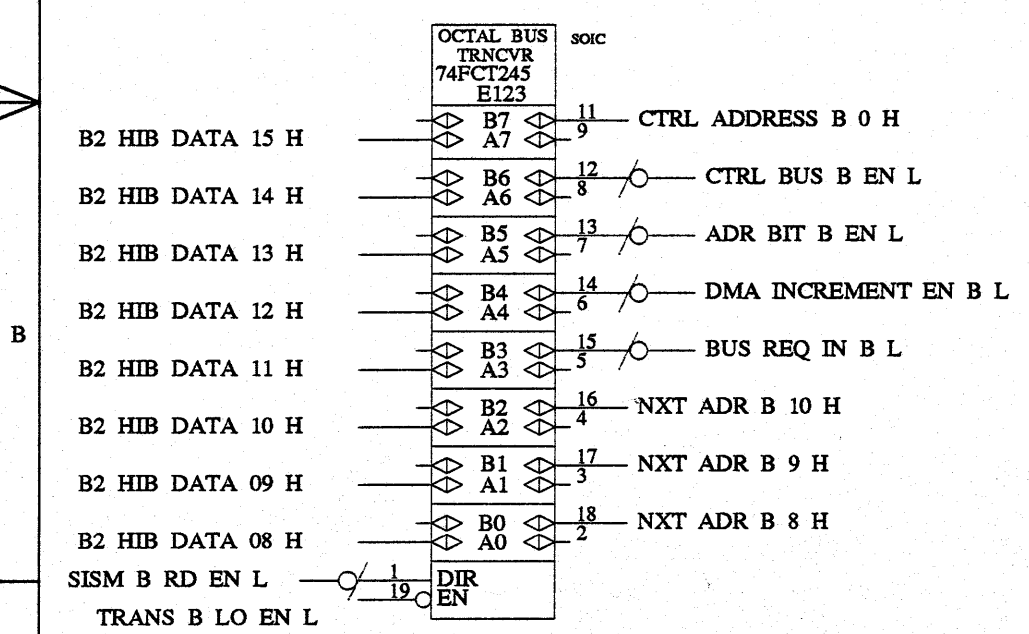
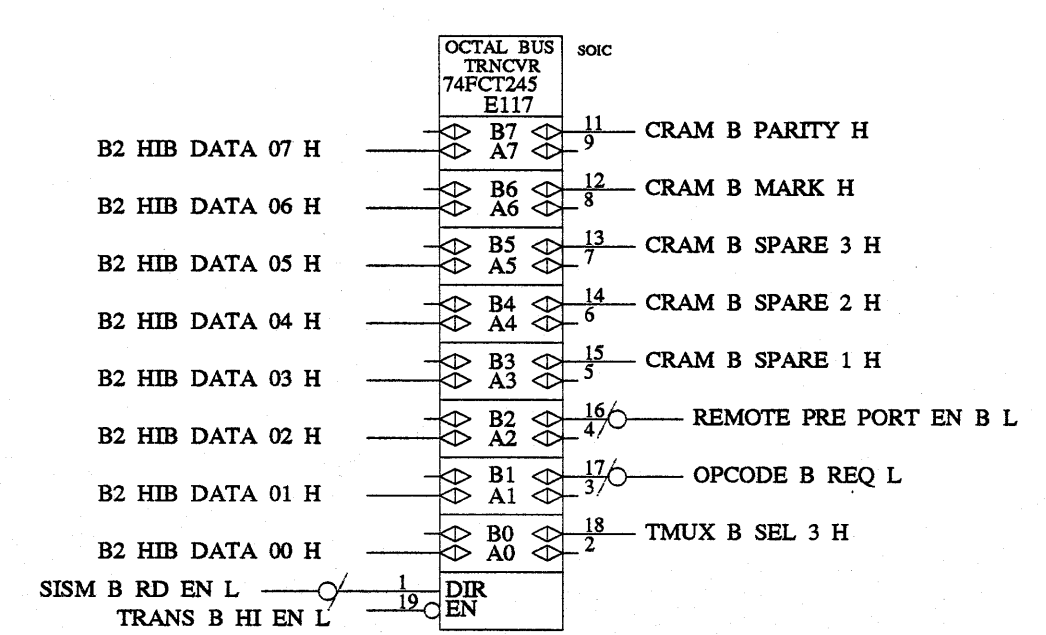
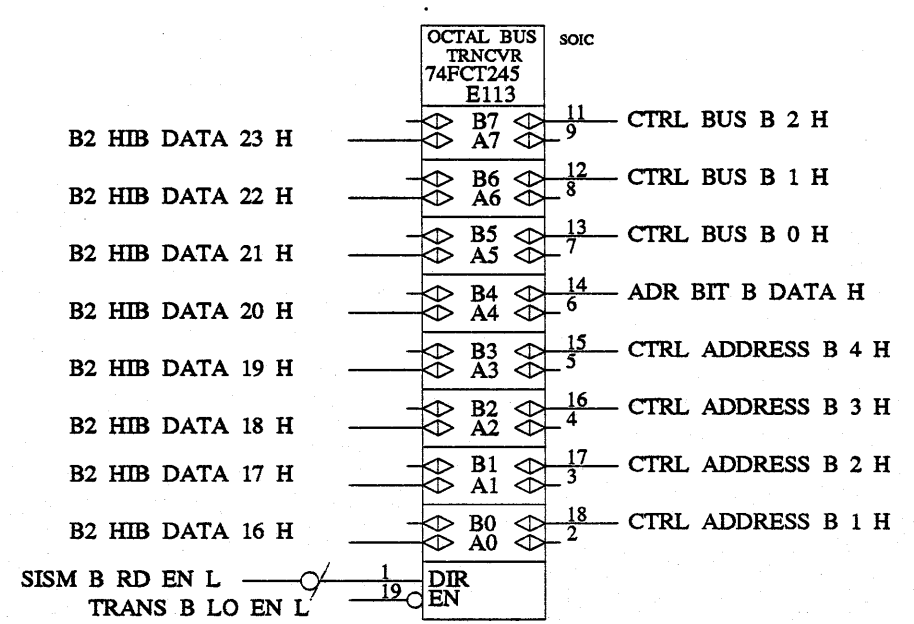
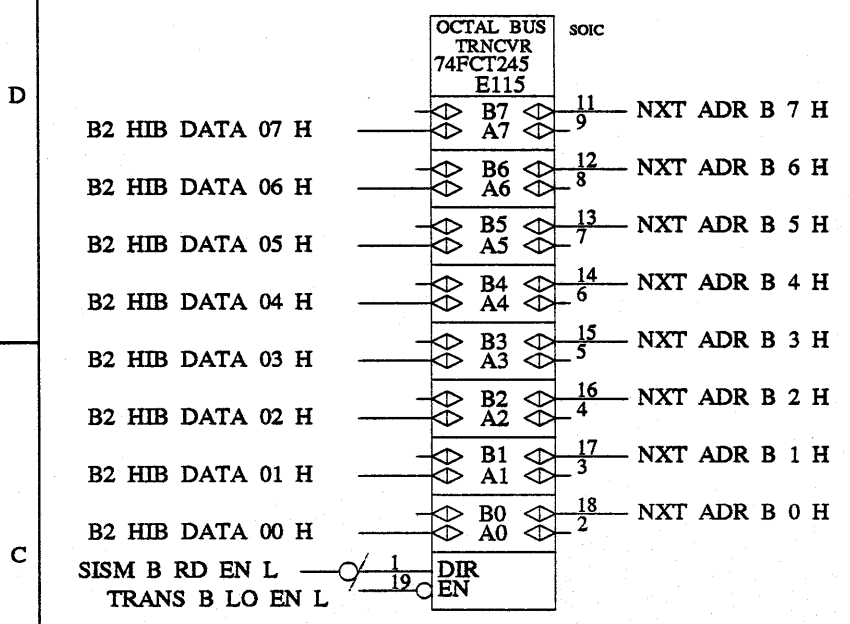
**digital**  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger  
 CHK'D: -  
 DATE: -  
 DATE: -  
 Mon Oct 17 15:46:48 1988

ENG: T. Nerger  
 BOARD LOCATION: CXO  
 SHEET 18  
 NEXT HIGHER ASSEMBLY: -

TITLE: **WILDCAT BOARD 2**  
 SIZE K  
 CODE CS  
 NUMBER CXO62  
 REV 17OCT88

REV  
 NUMBER  
 CS  
 K  
 B



USED FOR LOADING SISM RAMS

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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
SISM B DATA XCVRS

digital

FIRST USED ON OPTION/MODEL: -

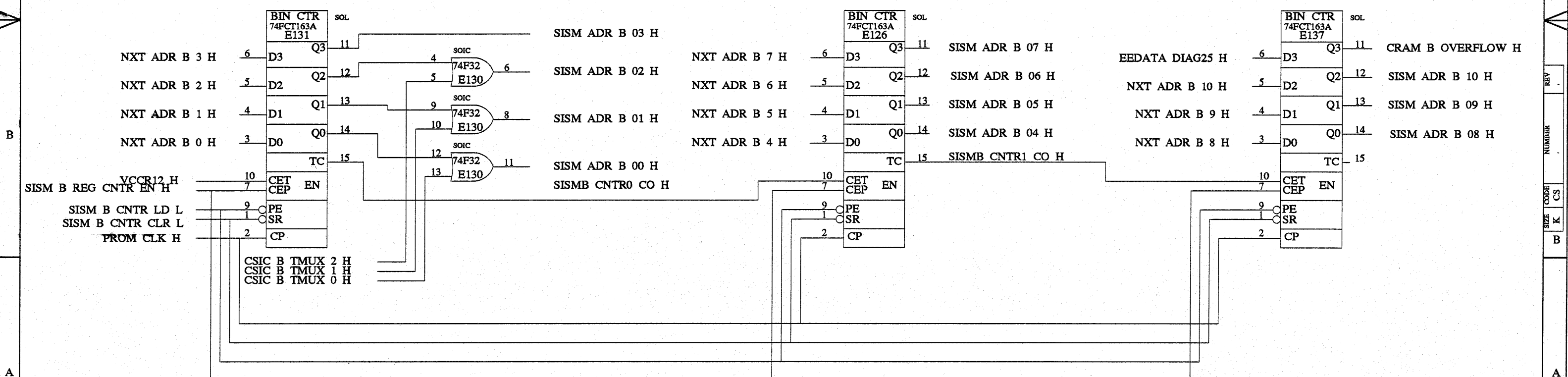
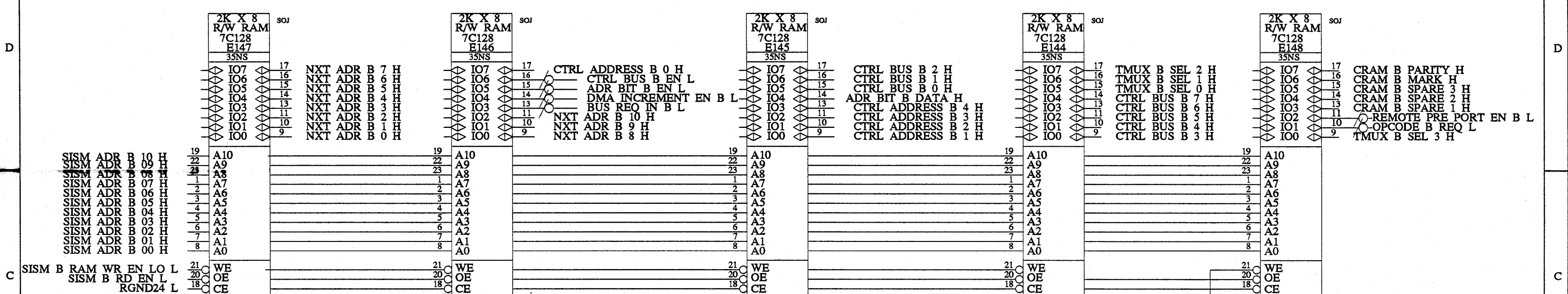
DRN: T. Nerger  
CHK'D: -  
DATE: -  
Mon Oct 17 15:47:08 1988

ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET 19  
NEXT HIGHER ASSEMBLY: -

DATE: -  
TITLE: WILDCAT BOARD 2

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

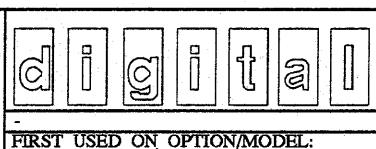
REV NUMBER SIZE CODE K CS B



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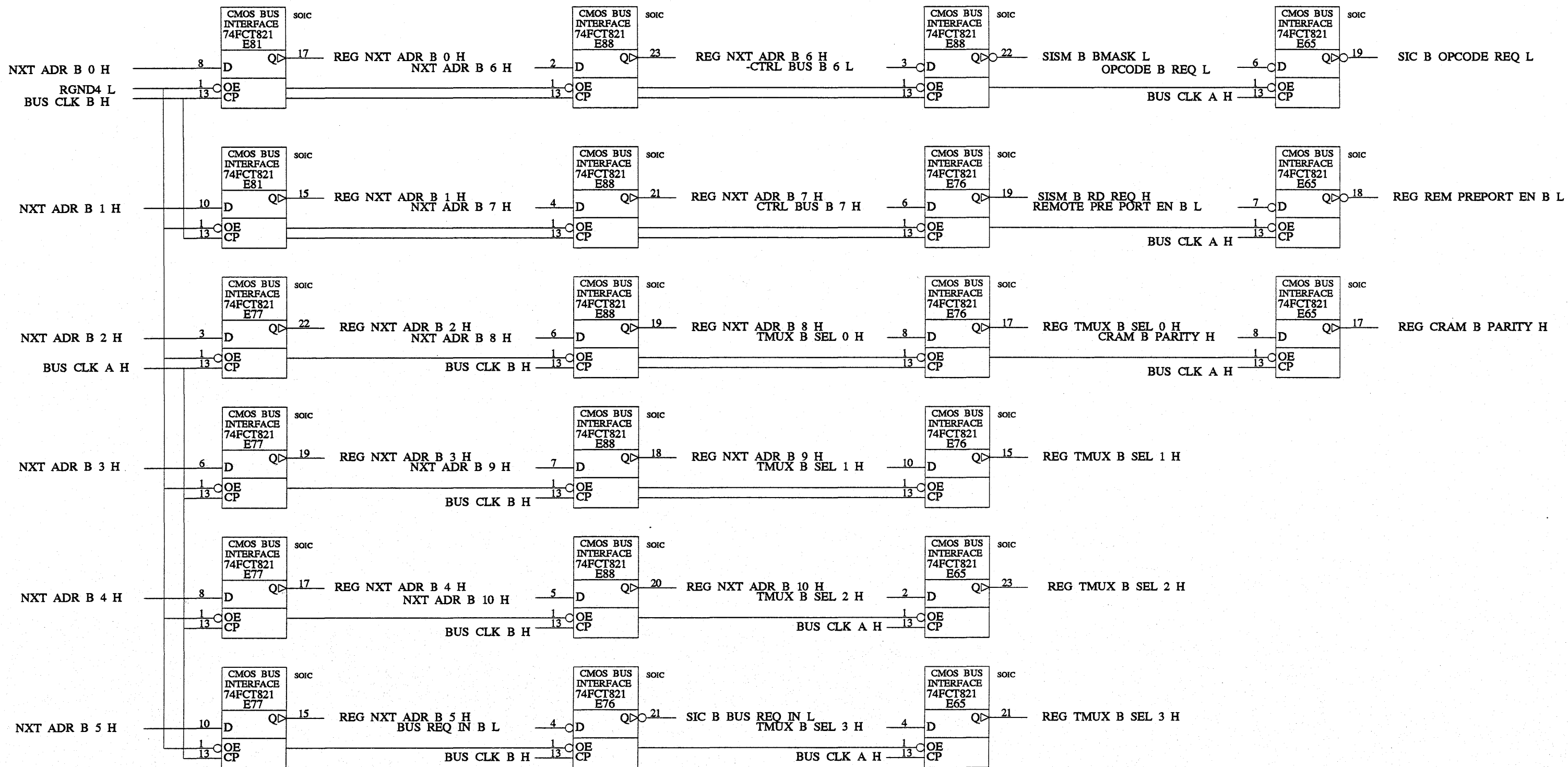
REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SI CHAN B STATE MACHINE**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 20	SIZE K
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: UNDO-	NUMBER CXO62	REV 17OCT88

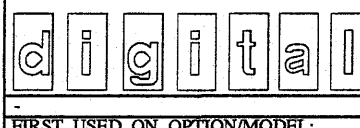
DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 20	SIZE K
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: UNDO-	NUMBER CXO62	REV 17OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SI CHAN B STATE MACHINE  
 REGISTERS**



DRN: T. Nerger  
 DATE: -  
 CHK'D: -  
 DATE: -  
 FIRST USED ON OPTION/MODEL: -

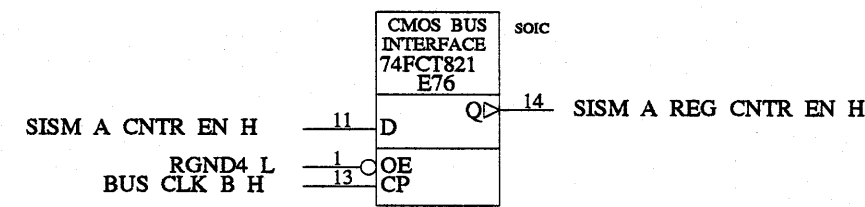
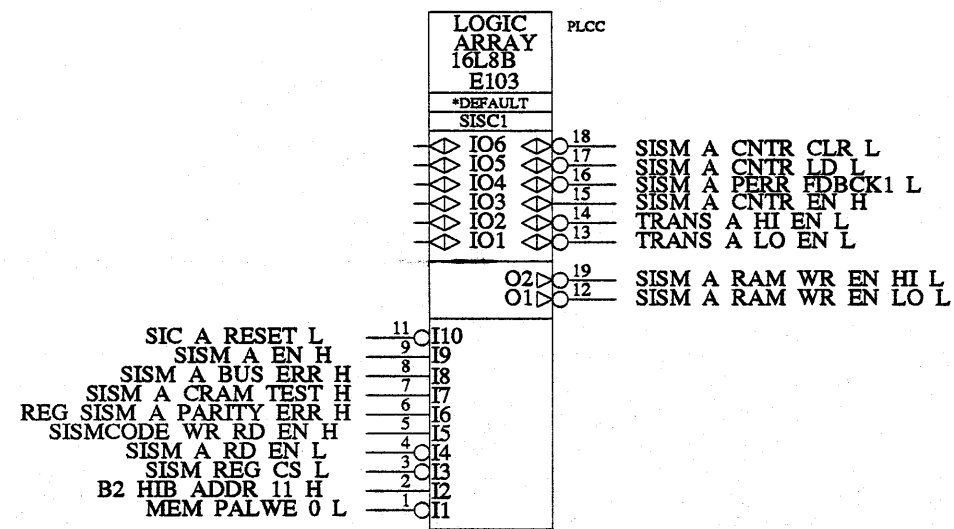
ENG: T. Nerger  
 DATE: -  
 BOARD LOCATION: CXO  
 SHEET: 21  
 NEXT HIGHER ASSEMBLY: -

TITLE:  
**WILDCAT BOARD 2**

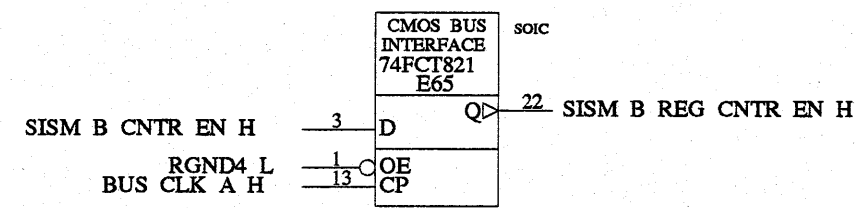
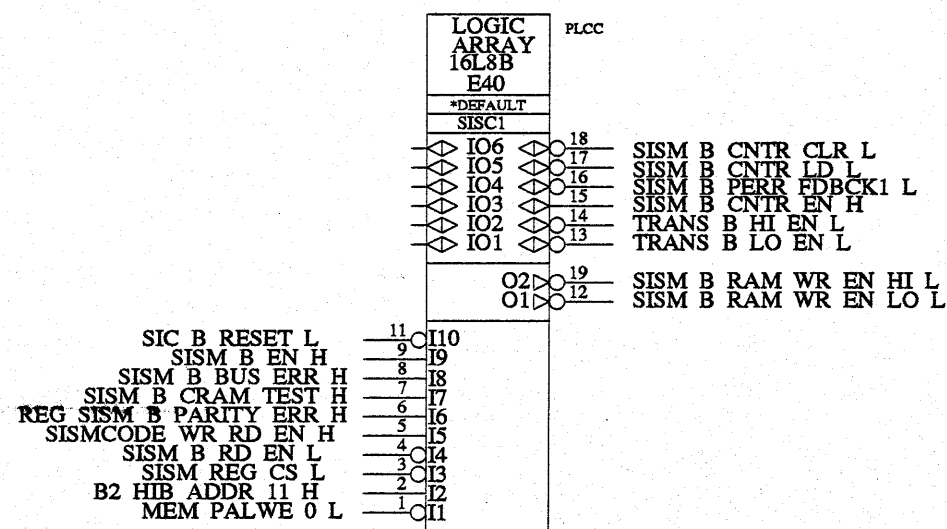
SIZE	CODE	NUMBER	REV
K	CS	CXO62	170CT88

REV NUMBER

### SISM CONTROL PAL A



### SISM CONTROL PAL B



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic] CSIC CHAN A DATA XCVRS

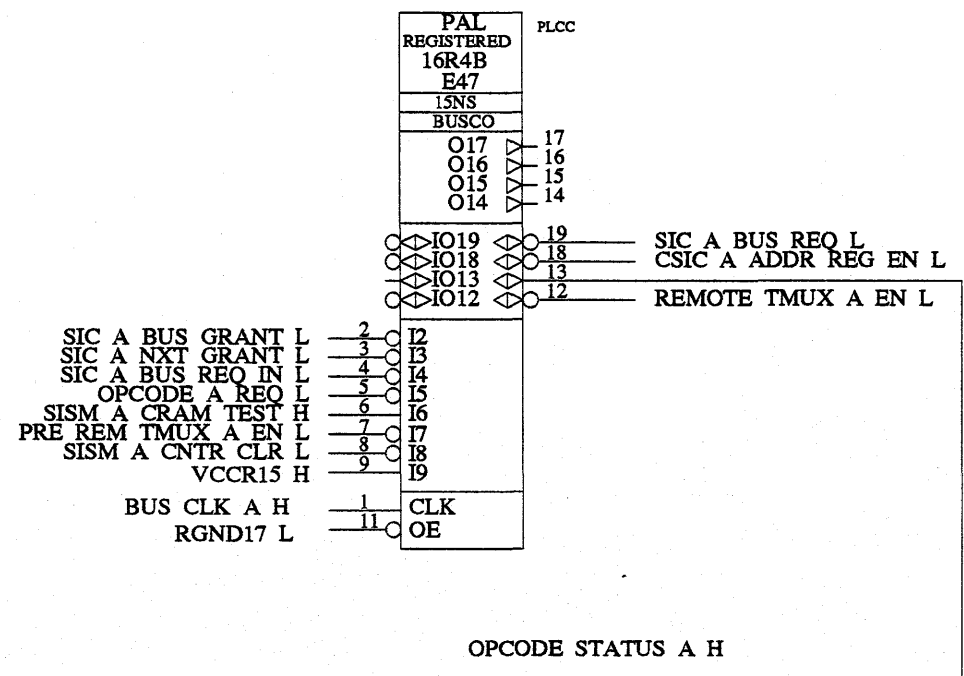
digital  
FIRST USED ON OPTION/MODEL: -

DRN: J. LYLE  
CHK'D: -  
DATE: -  
Mon Oct 17 15:48:41 1988

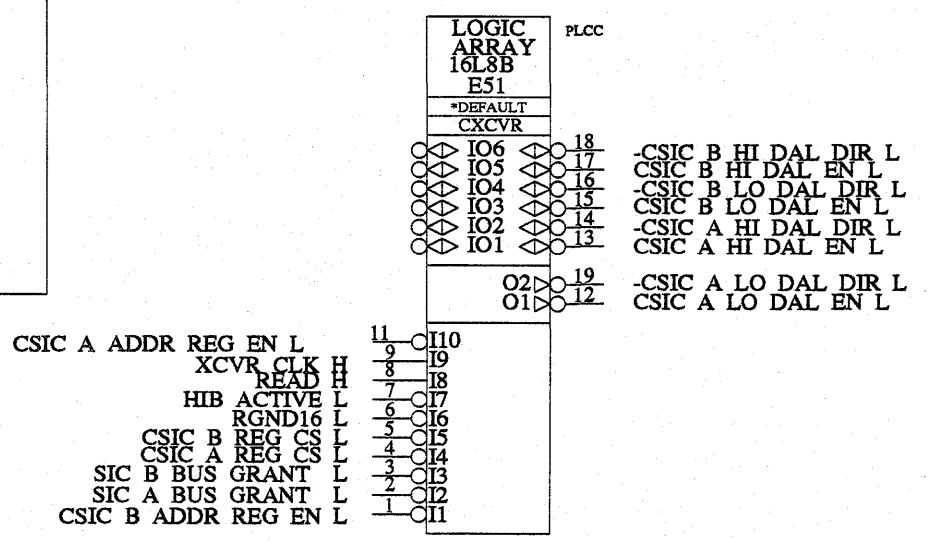
ENG: J. LYLE  
BOARD LOCATION: CXO  
SHEET 22  
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2  
SIZE K  
CODE CS  
NUMBER CXO62  
REV 17OCT88

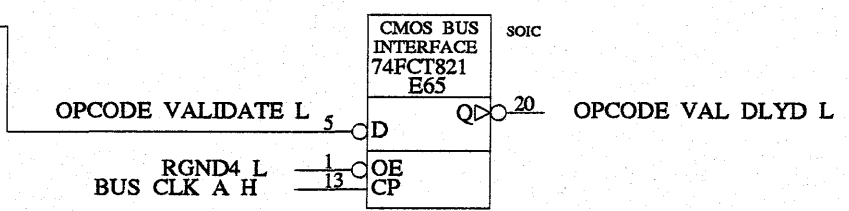
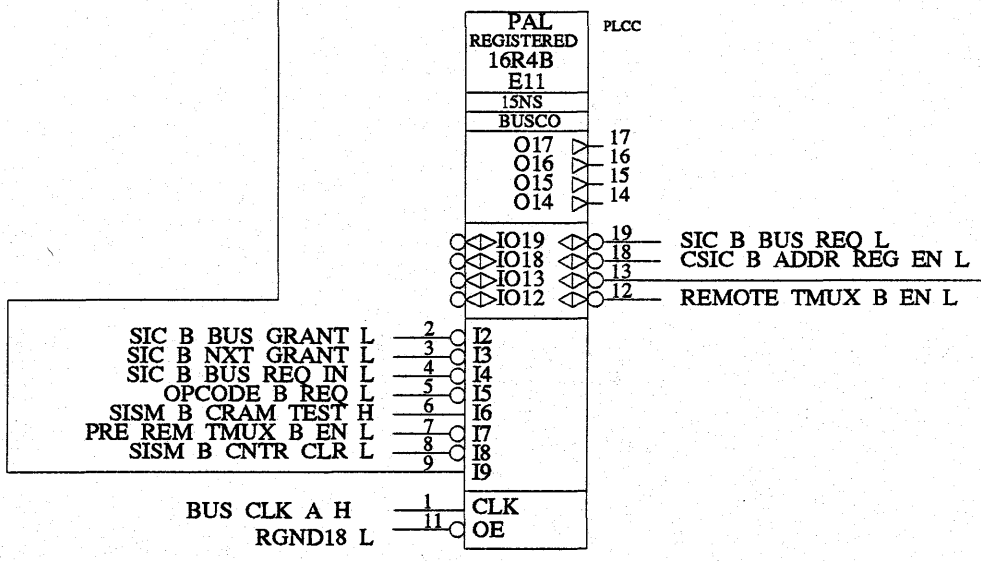
### BUS CONTROL PAL A



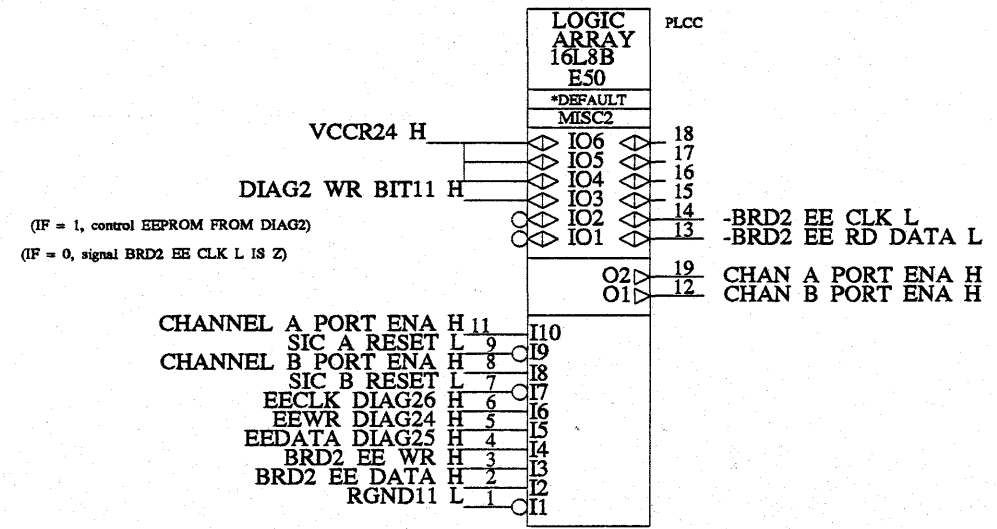
### SIC TRANSCEIVER CONTROL PAL



### BUS CONTROL PAL B



NOTE: FIRST PASS BOARD WILL CONTROL SERIAL EEPROM FROM BOARD 2 DIAGNOSTIC REGISTERS.  
FUTURE CHANGES WILL MOVE THIS PAL SUPPORT LOGIC TO BOARD 1.



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SISM CONTROL PALS**

**digital**  
FIRST USED ON OPTION/MODEL: -

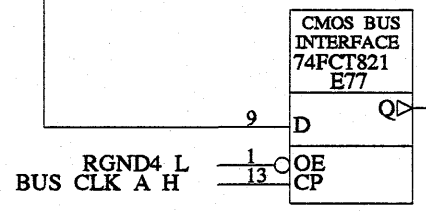
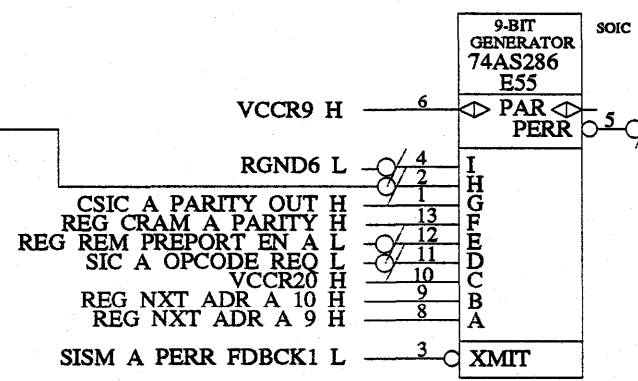
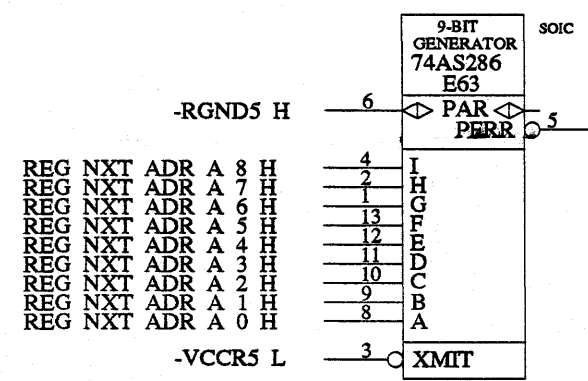
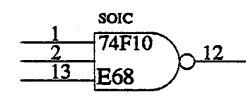
DRN: T. Nerger  
CHK'D: -  
Tue Oct 25 16:36:20 1988

DATE -  
DATE -

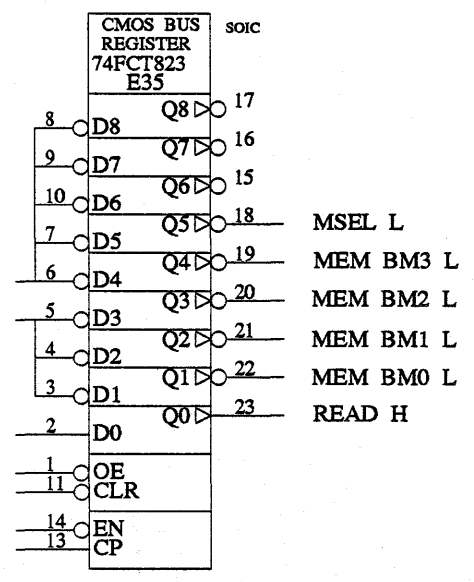
ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET 23  
NEXT HIGHER ASSEMBLY: -

TITLE: **WILDCAT BOARD 2**  
SIZE K CODE CS NUMBER CXO62 REV 25OCT88

REG TMUX A SEL 3 H  
 REG TMUX A SEL 2 H  
 REG TMUX A SEL 1 H

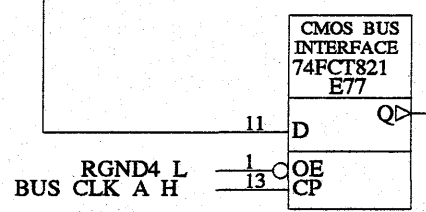
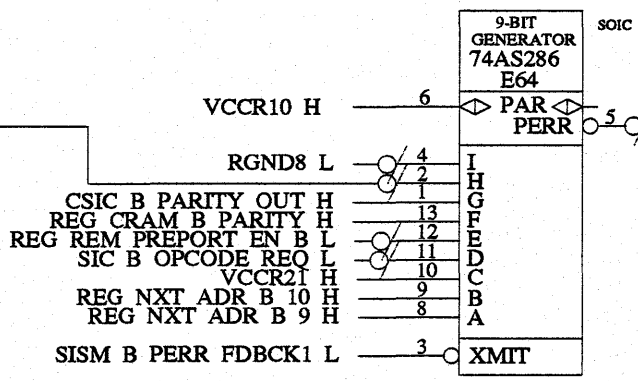
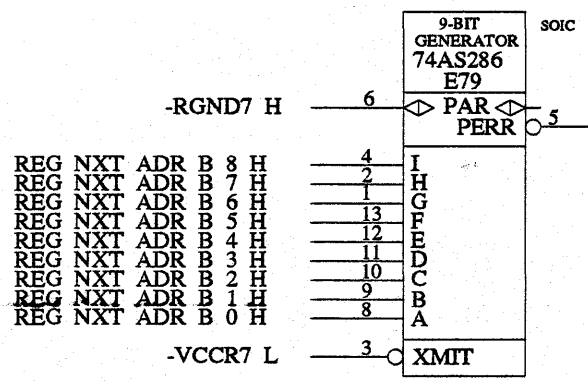
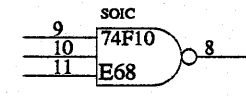


RGND9 L  
 SISM A BMASK L  
 SISM A RD REQ H  
 SIC A BUS GRANT L  
 SIC A RESET L  
 SIC A BUS REQ IN L  
 BUS CLK B H

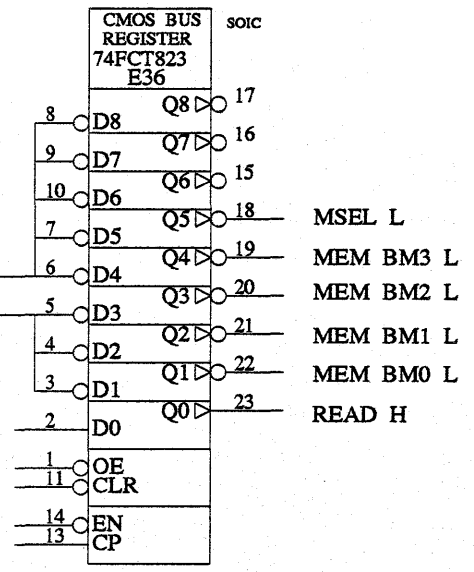


MSEL L  
 MEM BM3 L  
 MEM BM2 L  
 MEM BM1 L  
 MEM BM0 L  
 READ H

REG TMUX B SEL 3 H  
 REG TMUX B SEL 2 H  
 REG TMUX B SEL 1 H



RGND10 L  
 SISM B BMASK L  
 SISM B RD REQ H  
 SIC B BUS GRANT L  
 SIC B RESET L  
 SIC B BUS REQ IN L  
 BUS CLK B H



MSEL L  
 MEM BM3 L  
 MEM BM2 L  
 MEM BM1 L  
 MEM BM0 L  
 READ H

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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**SISM CHAN A & B  
 PARITY & BUS REGISTERS**

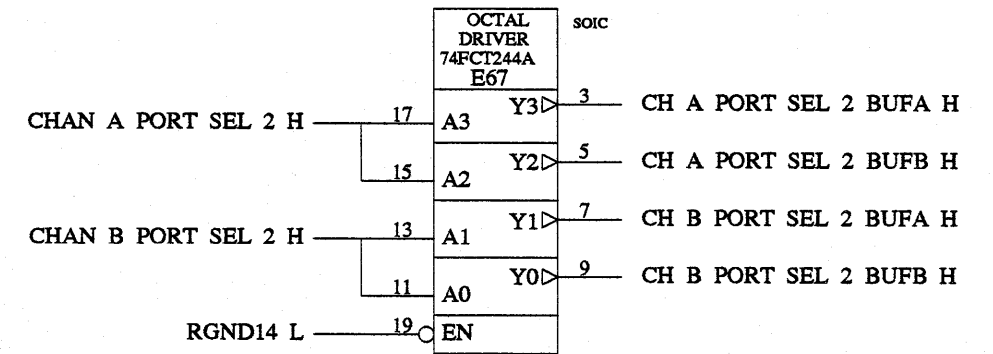
**digital**  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D: -	DATE	BOARD LOCATION: CXO	SHEET 24
Tue Oct 18 11:25:04 1988		NEXT HIGHER ASSEMBLY: -	

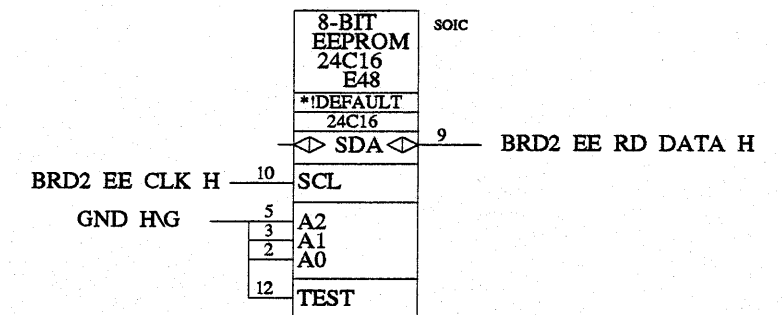
TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88



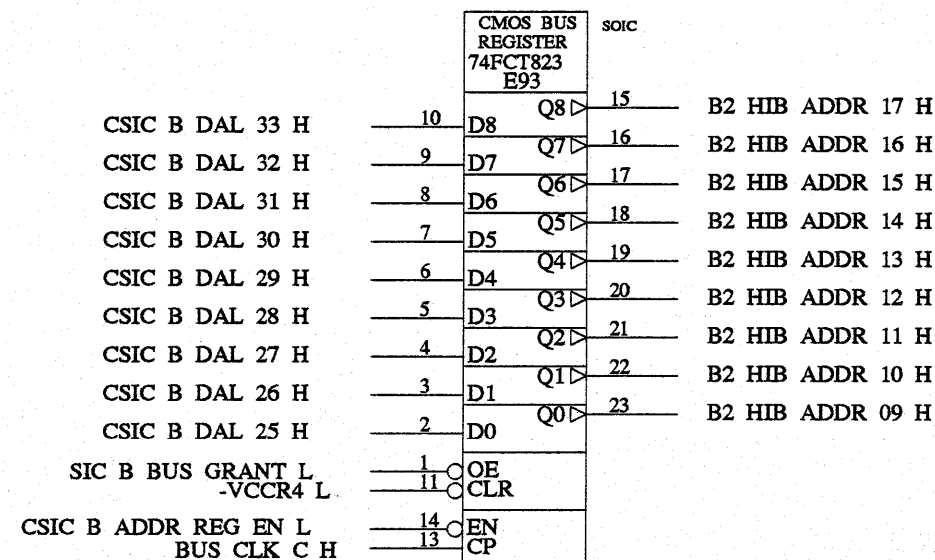
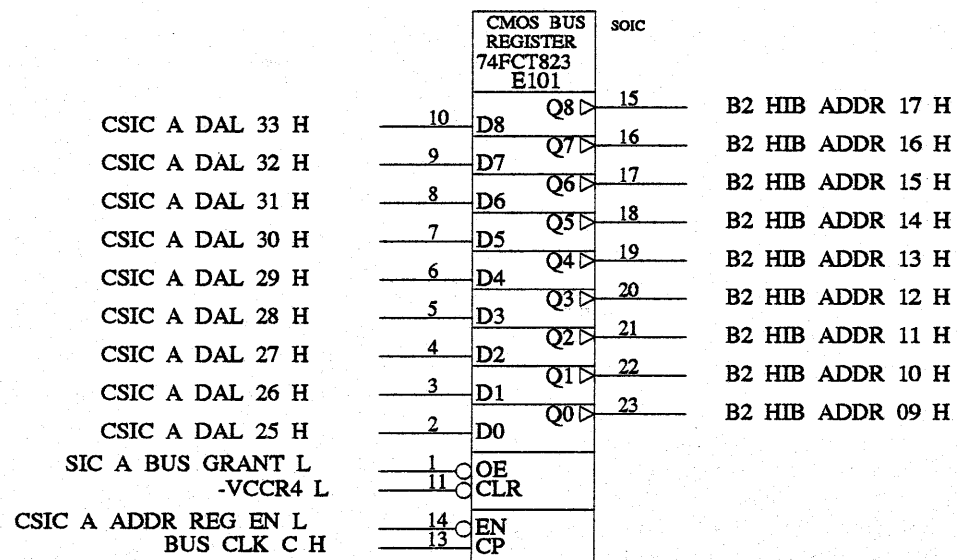
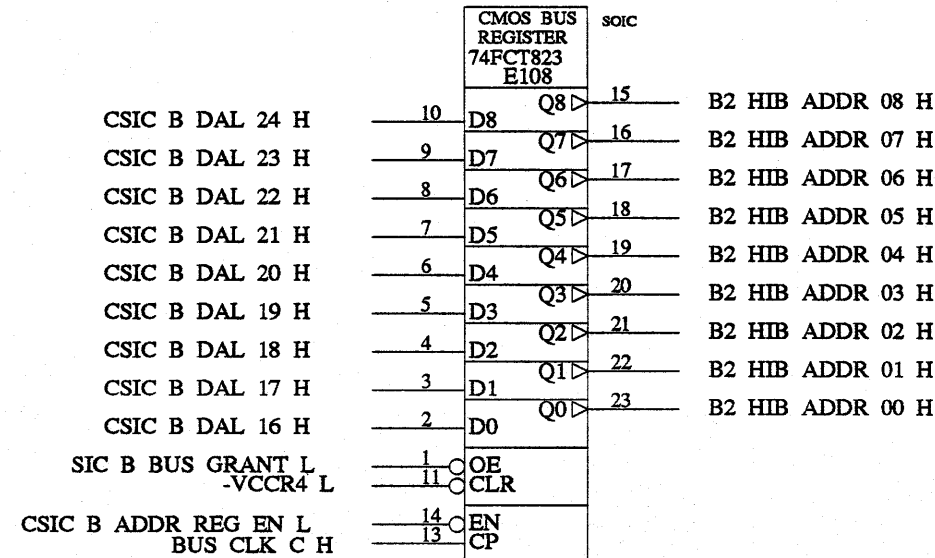
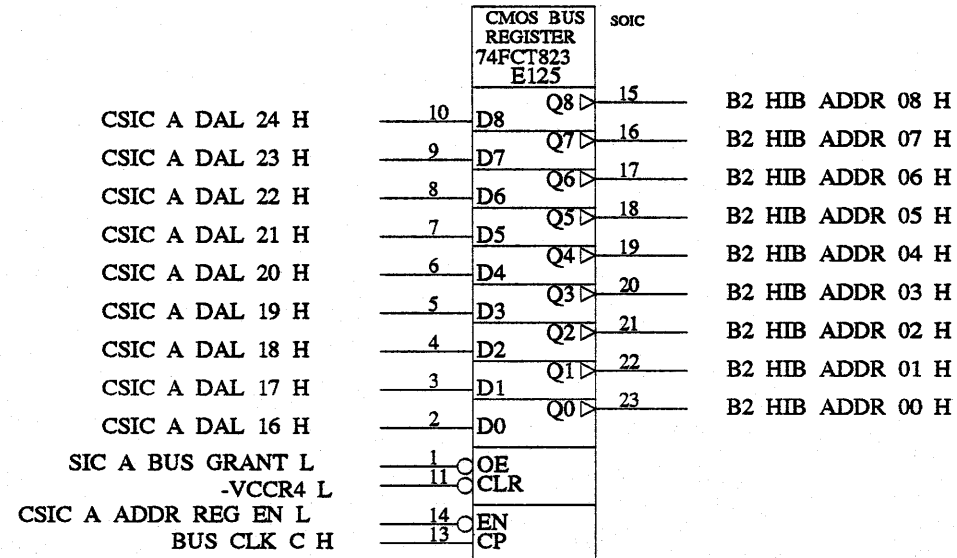
### PORT SELECT BUFFER



### SERIAL EEPROM



PIN 13 = VCC  
PIN 6 = VSS (GND)



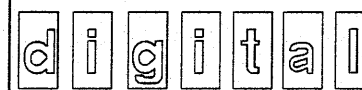
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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]

**CSIC CHAN A & B  
ADDRESS XCVRS  
SERIAL EEPROM**



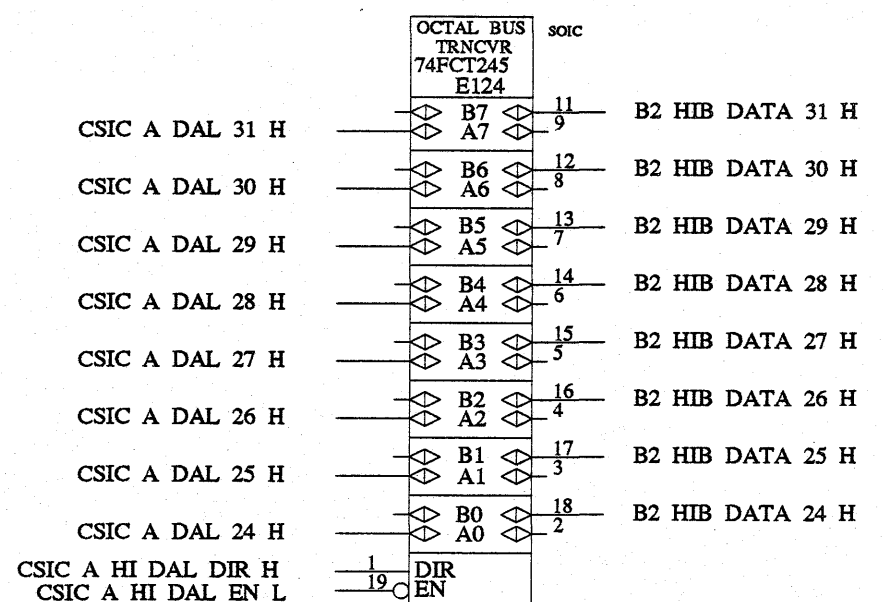
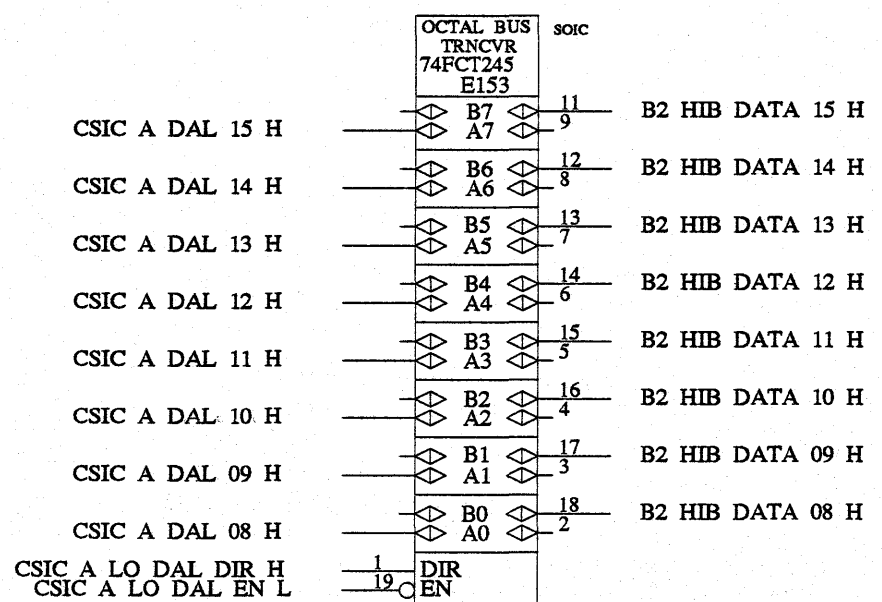
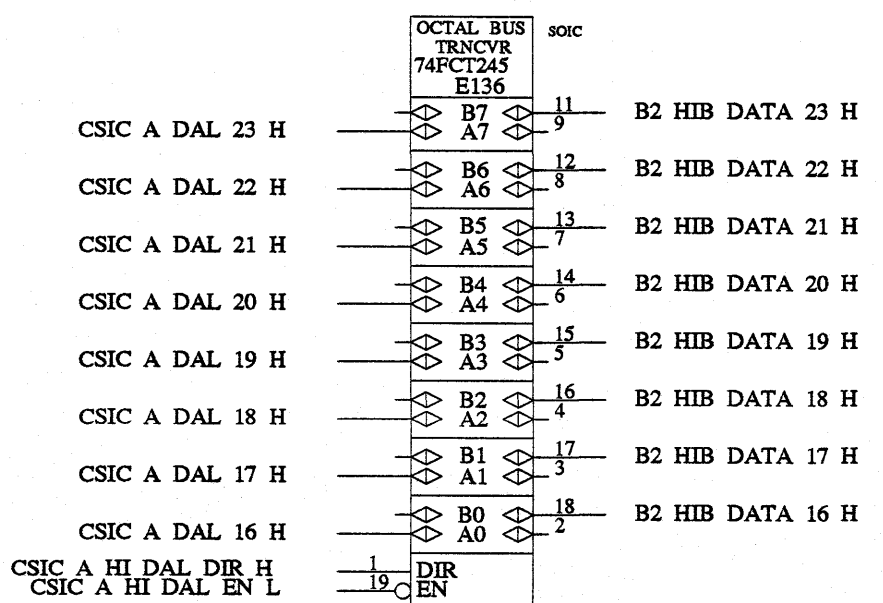
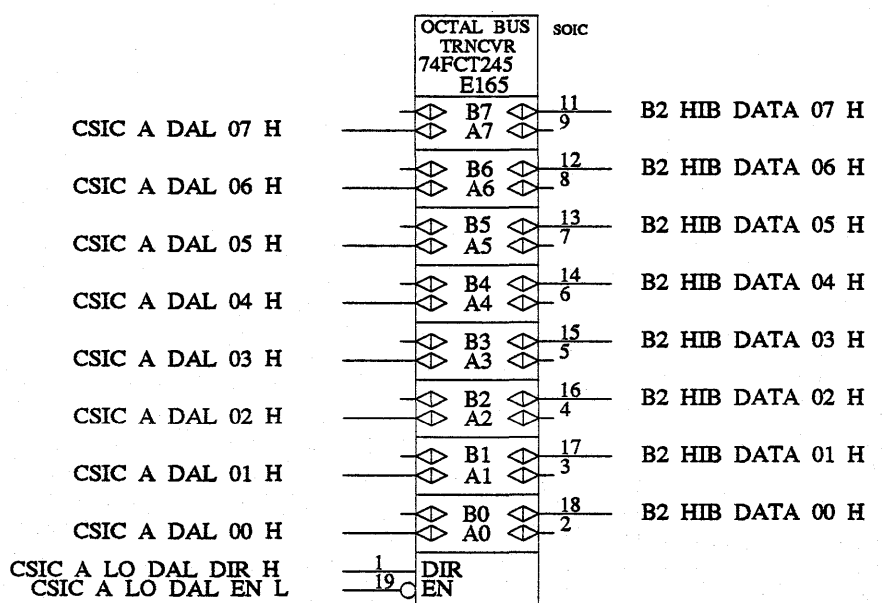
DRN: T. Nerger DATE: ENG: T. Nerger DATE: TITLE: WILDCAT BOARD 2

CHK'D: DATE: BOARD LOCATION: CXO SHEET 25

Mon Oct 17 15:49:21 1988 NEXT HIGHER ASSEMBLY:

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

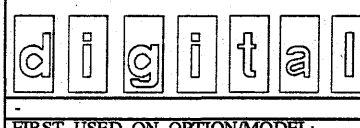
FIRST USED ON OPTION/MODEL:



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic] CSIC CHAN A DATA XCVRS

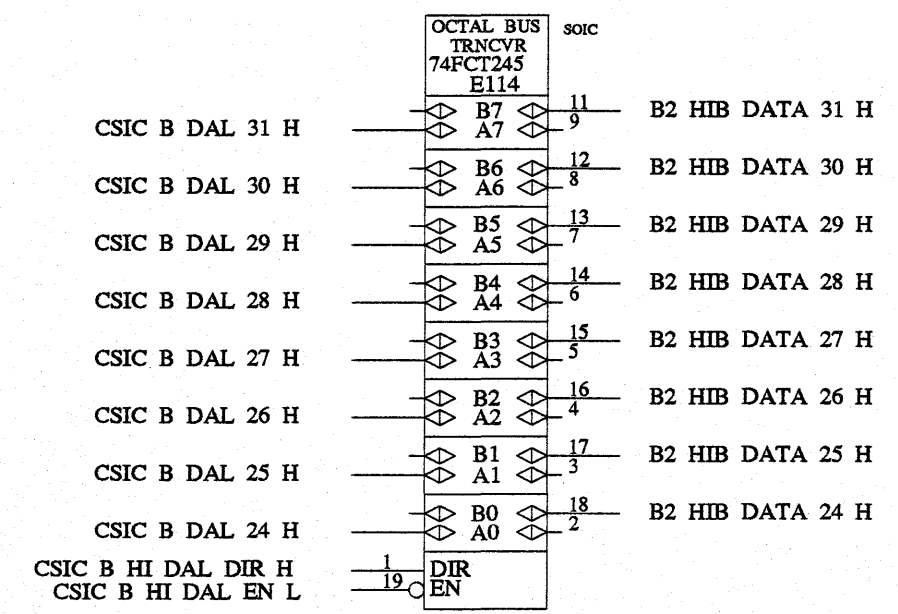
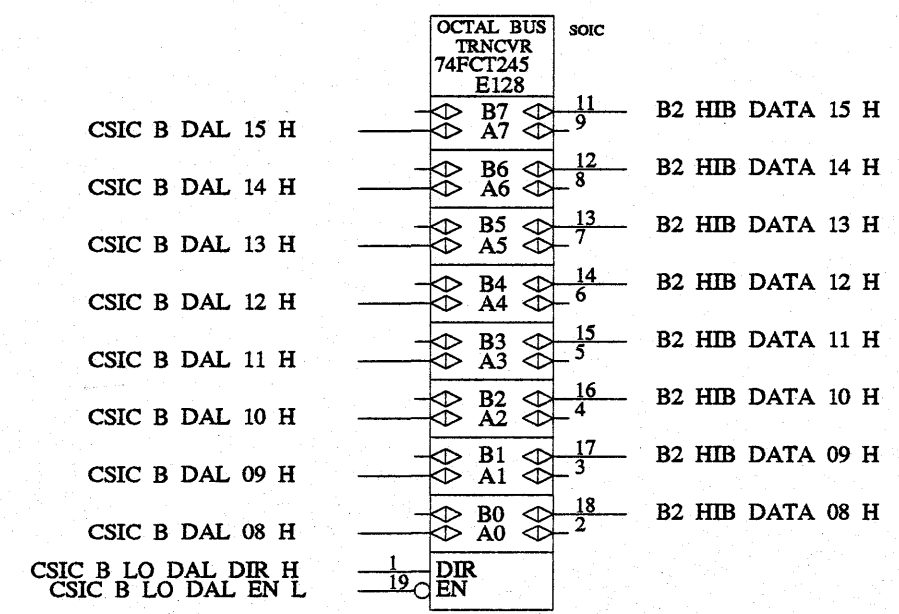
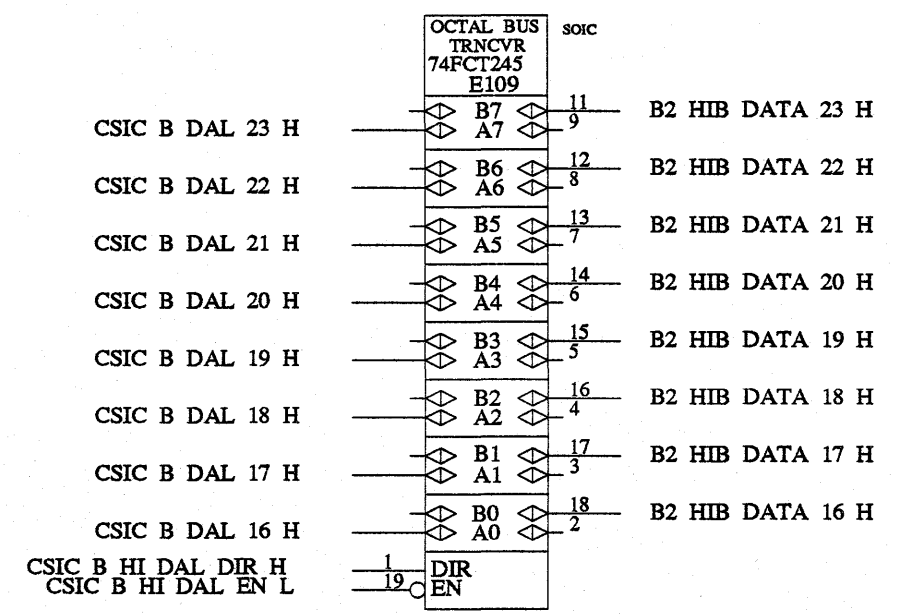
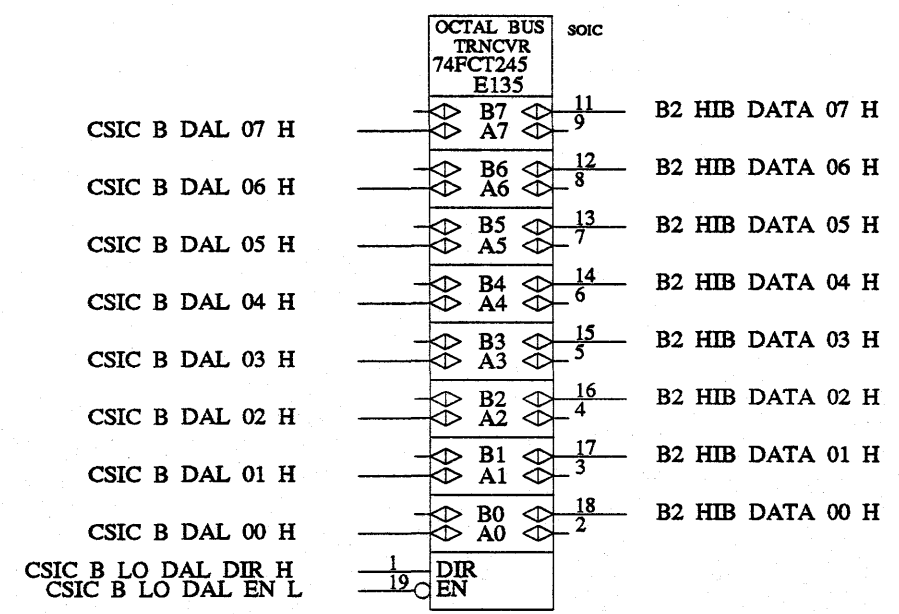


DRN: T. Nerger  
CHK'D: -  
DATE: -  
DATE: -  
Mon Oct 17 15:49:35 1988

ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET 26  
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2  
SIZE K  
CODE CS  
NUMBER CXO62  
REV 17OCT88

REV NUMBER CS K SIZE



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic] CSIC CHAN B DATA XCVRS

digital  
FIRST USED ON OPTION/MODEL: -

DRN: T. Neger	DATE -
CHK'D: -	DATE -
Mon Oct 17 15:49:50 1988	

ENG: T. Neger	DATE -
BOARD LOCATION: CXO	SHEET 27
NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88

REV NUMBER SIZE CODE CS K B

CSIC A DAL 00 H  
 CSIC A DAL 01 H  
 CSIC A DAL 02 H  
 CSIC A DAL 03 H  
 CSIC A DAL 04 H  
 CSIC A DAL 05 H  
 CSIC A DAL 06 H  
 CSIC A DAL 07 H  
 CSIC A DAL 08 H  
 CSIC A DAL 09 H  
 CSIC A DAL 10 H  
 CSIC A DAL 11 H  
 CSIC A DAL 12 H  
 CSIC A DAL 13 H  
 CSIC A DAL 14 H  
 CSIC A DAL 15 H  
 CSIC A DAL 16 H  
 CSIC A DAL 17 H  
 CSIC A DAL 18 H  
 CSIC A DAL 19 H  
 CSIC A DAL 20 H  
 CSIC A DAL 21 H  
 CSIC A DAL 22 H  
 CSIC A DAL 23 H  
 CSIC A DAL 24 H  
 CSIC A DAL 25 H  
 CSIC A DAL 26 H  
 CSIC A DAL 27 H  
 CSIC A DAL 28 H  
 CSIC A DAL 29 H  
 CSIC A DAL 30 H  
 CSIC A DAL 31 H  
 CSIC A DAL 32 H  
 CSIC A DAL 33 H

B2 HIB ADDR 00 H  
 CSIC A CS L  
 HIB WR H  
 SIC A NXT GRANT L  
 OPCODE VALIDATE L

REG SISM A PARITY ERR H  
 CSIC A PARITY OUT H  
 BUS REQ IN A L  
 DMA INCREMENT EN A L

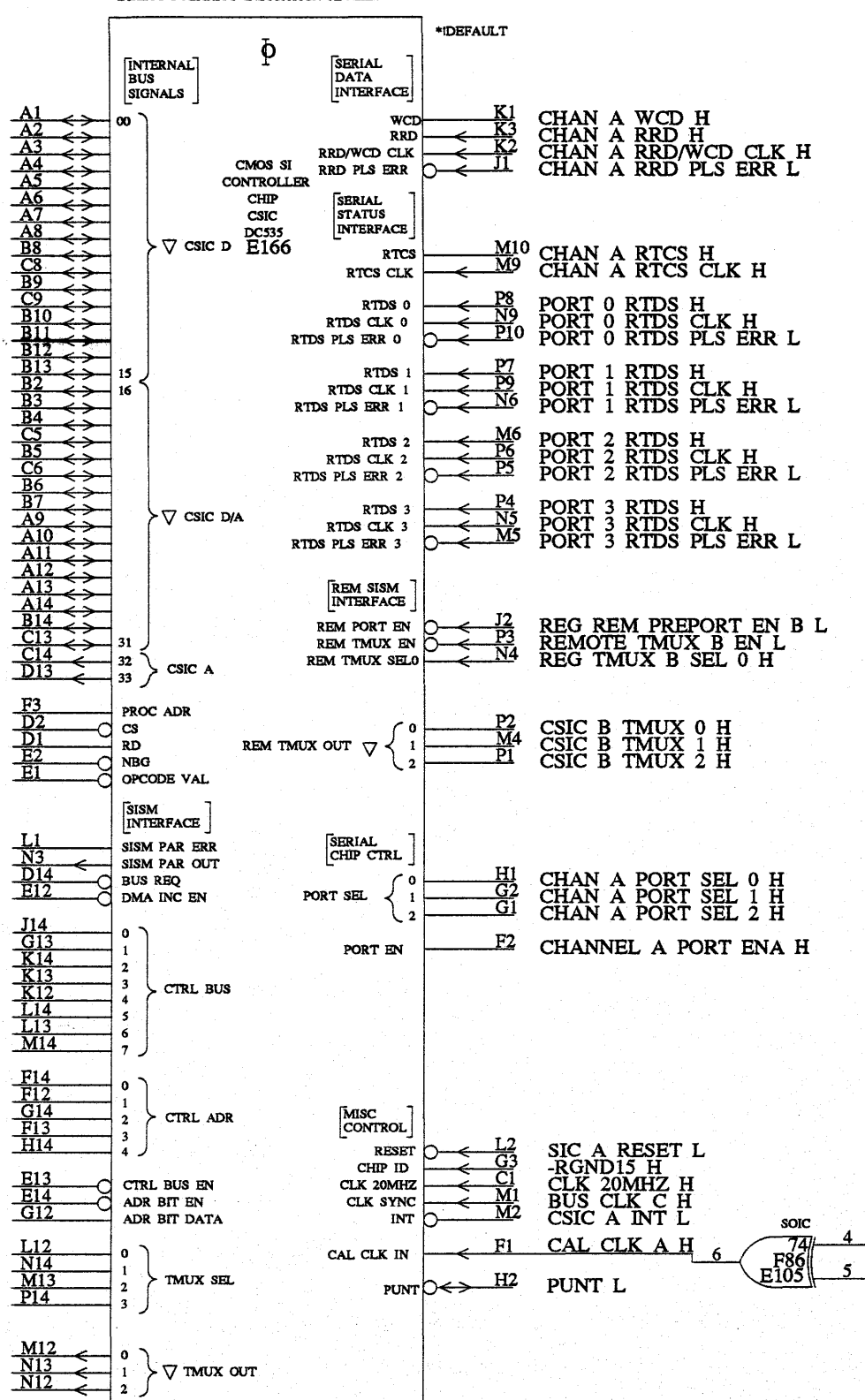
CTRL BUS A 0 H  
 CTRL BUS A 1 H  
 CTRL BUS A 2 H  
 CTRL BUS A 3 H  
 CTRL BUS A 4 H  
 CTRL BUS A 5 H  
 CTRL BUS A 6 H  
 CTRL BUS A 7 H

CTRL ADDRESS A 0 H  
 CTRL ADDRESS A 1 H  
 CTRL ADDRESS A 2 H  
 CTRL ADDRESS A 3 H  
 CTRL ADDRESS A 4 H

CTRL BUS A EN L  
 ADR BIT A EN L  
 ADR BIT A DATA H

TMUX A SEL 0 H  
 TMUX A SEL 1 H  
 TMUX A SEL 2 H  
 TMUX A SEL 3 H

CSIC A TMUX 0 H  
 CSIC A TMUX 1 H  
 CSIC A TMUX 2 H



CHAN A WCD H  
 CHAN A RRD H  
 CHAN A RRD/WCD CLK H  
 CHAN A RRD PLS ERR L

CHAN A RTCS H  
 CHAN A RTCS CLK H

PORT 0 RTDS H  
 PORT 0 RTDS CLK H  
 PORT 0 RTDS PLS ERR L

PORT 1 RTDS H  
 PORT 1 RTDS CLK H  
 PORT 1 RTDS PLS ERR L

PORT 2 RTDS H  
 PORT 2 RTDS CLK H  
 PORT 2 RTDS PLS ERR L

PORT 3 RTDS H  
 PORT 3 RTDS CLK H  
 PORT 3 RTDS PLS ERR L

REG REM PREPORT EN B L  
 REMOTE TMUX B EN L  
 REG TMUX B SEL 0 H

CSIC B TMUX 0 H  
 CSIC B TMUX 1 H  
 CSIC B TMUX 2 H

CHAN A PORT SEL 0 H  
 CHAN A PORT SEL 1 H  
 CHAN A PORT SEL 2 H

CHANNEL A PORT ENA H

SIC A RESET L  
 -RGND15 H  
 CLK 20MHZ H  
 BUS CLK C H  
 CSIC A INT L

CAL CLK A H

PUNT L

CHAN A PORT SEL 0 H  
 CHAN A PORT SEL 1 H  
 CH A PORT SEL 2 BUFA H  
 CHAN A PORT ENA H

CHAN A WCD H  
 CHAN A RRD H  
 CHAN A RRD/WCD CLK H  
 CHAN A RRD PLS ERR L

CHAN A RTCS H  
 CHAN A RTCS CLK H

CHAN B PORT SEL 0 H  
 CHAN B PORT SEL 1 H  
 CH B PORT SEL 2 BUFA H  
 CHAN B PORT ENA H

CHAN B WCD H  
 CHAN B RRD H  
 CHAN B RRD/WCD CLK H  
 CHAN B RRD PLS ERR L

CHAN B RTCS H  
 CHAN B RTCS CLK H

PORT 0 RTDS H  
 PORT 0 RTDS CLK H  
 PORT 0 RTDS PLS ERR L

PORT 1 RTDS H  
 PORT 1 RTDS CLK H  
 PORT 1 RTDS PLS ERR L

PORT 2 RTDS H  
 PORT 2 RTDS CLK H  
 PORT 2 RTDS PLS ERR L

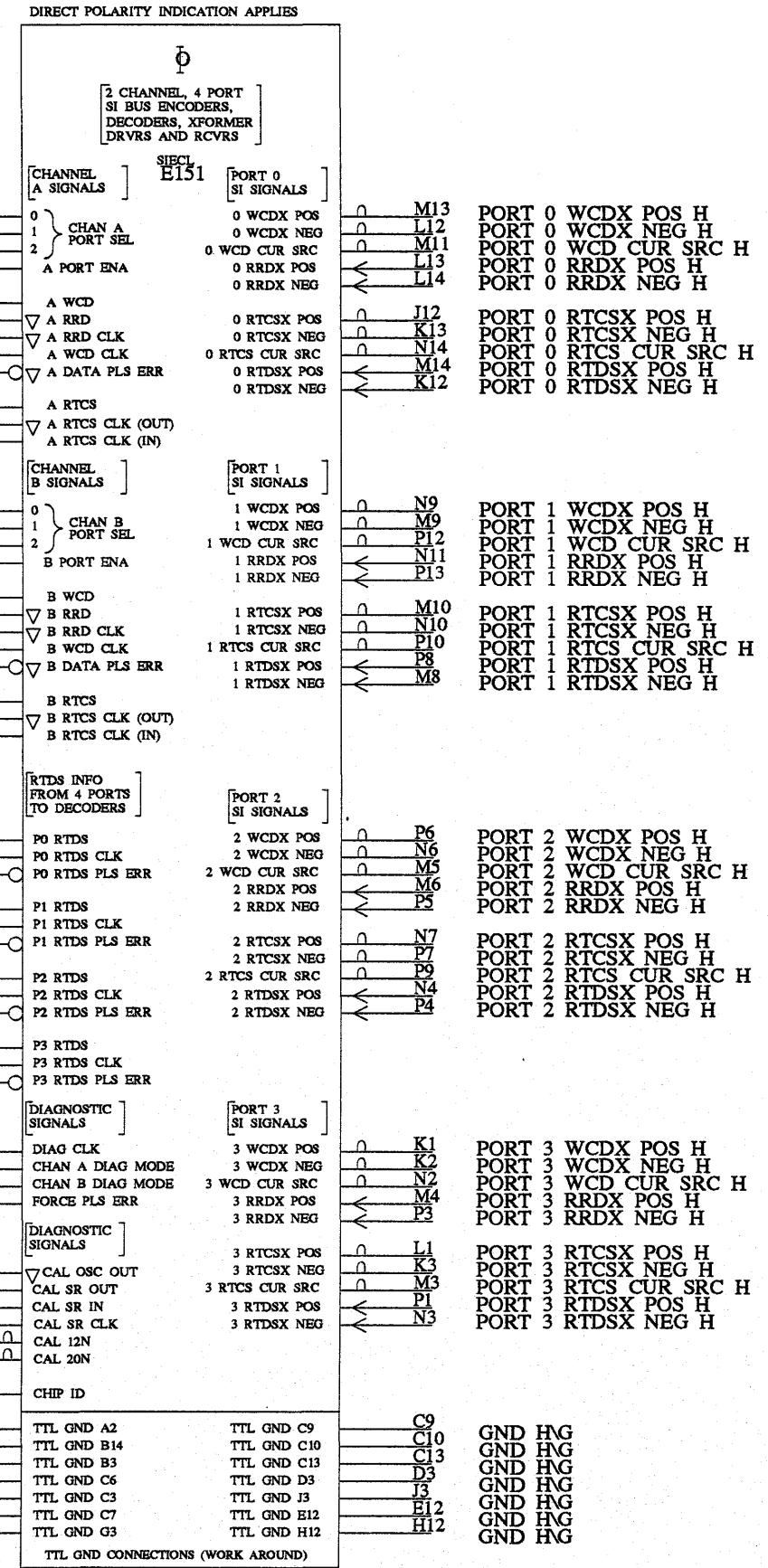
PORT 3 RTDS H  
 PORT 3 RTDS CLK H  
 PORT 3 RTDS PLS ERR L

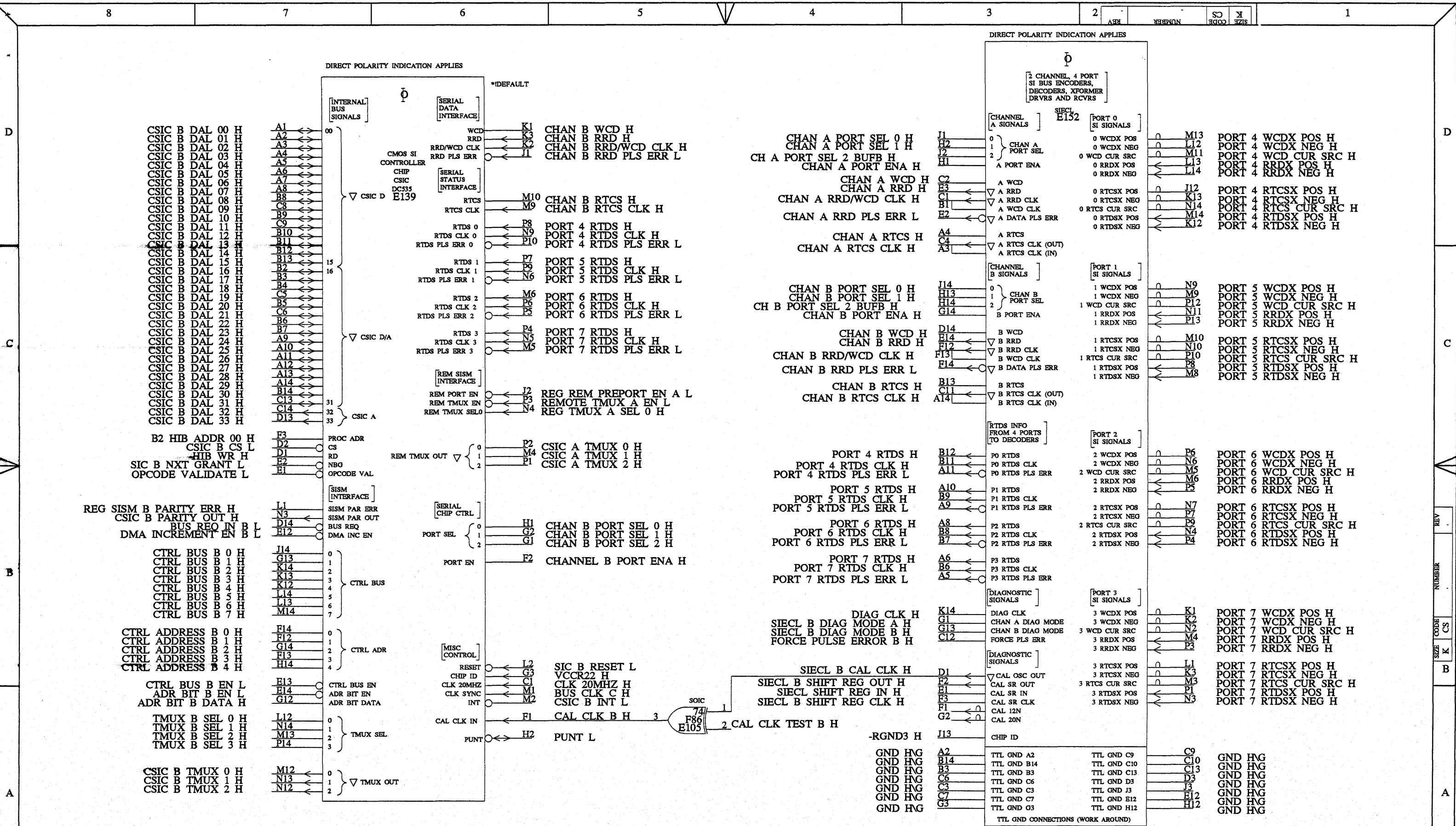
SIECL A DIAG MODE A H  
 SIECL A DIAG MODE B H  
 FORCE PULSE ERROR A H

SIECL A CAL CLK H

SIECL A SHIFT REG OUT H  
 SIECL SHIFT REG IN H  
 SIECL A SHIFT REG CLK H

CAL CLK TEST A H





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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**CHAN B CSIC &  
 HIGH ORDER SIECL**

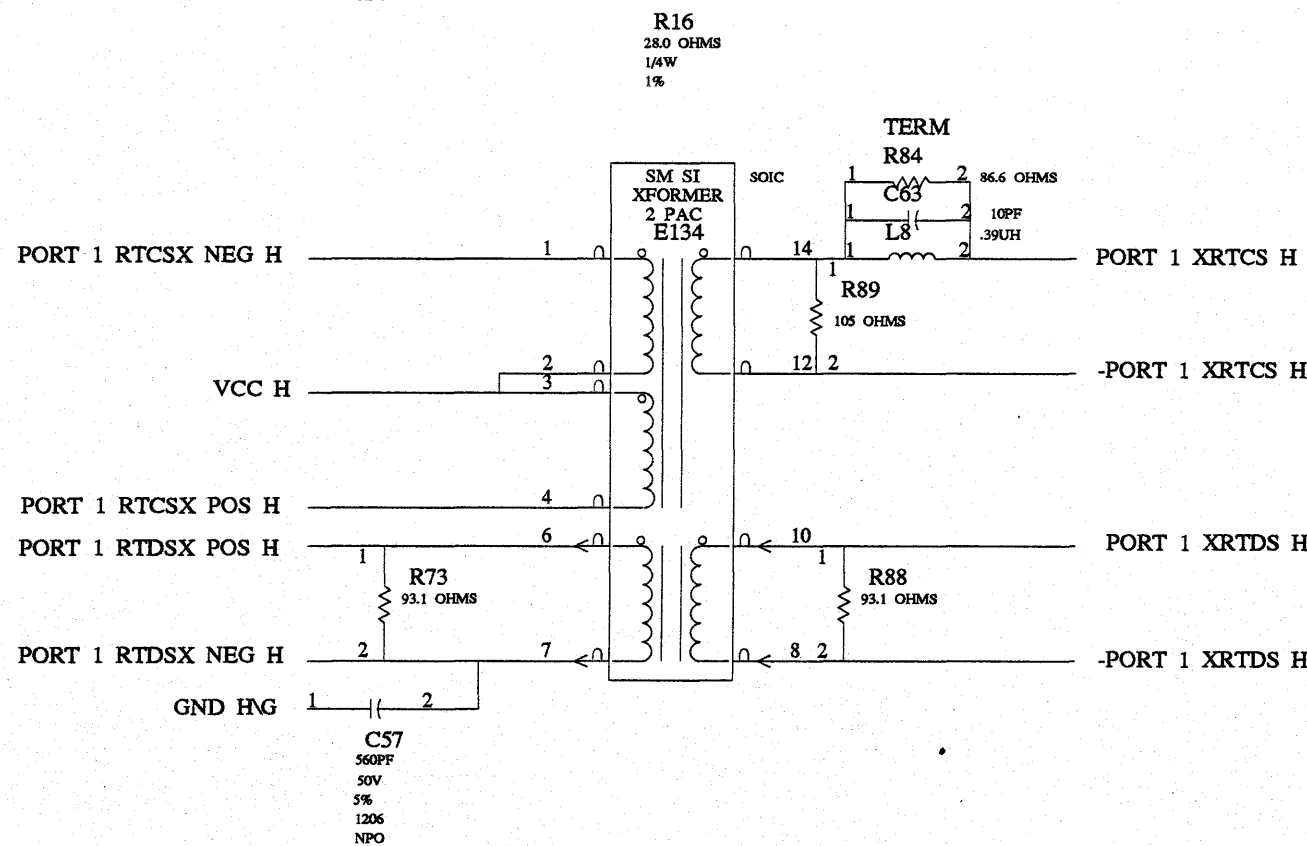
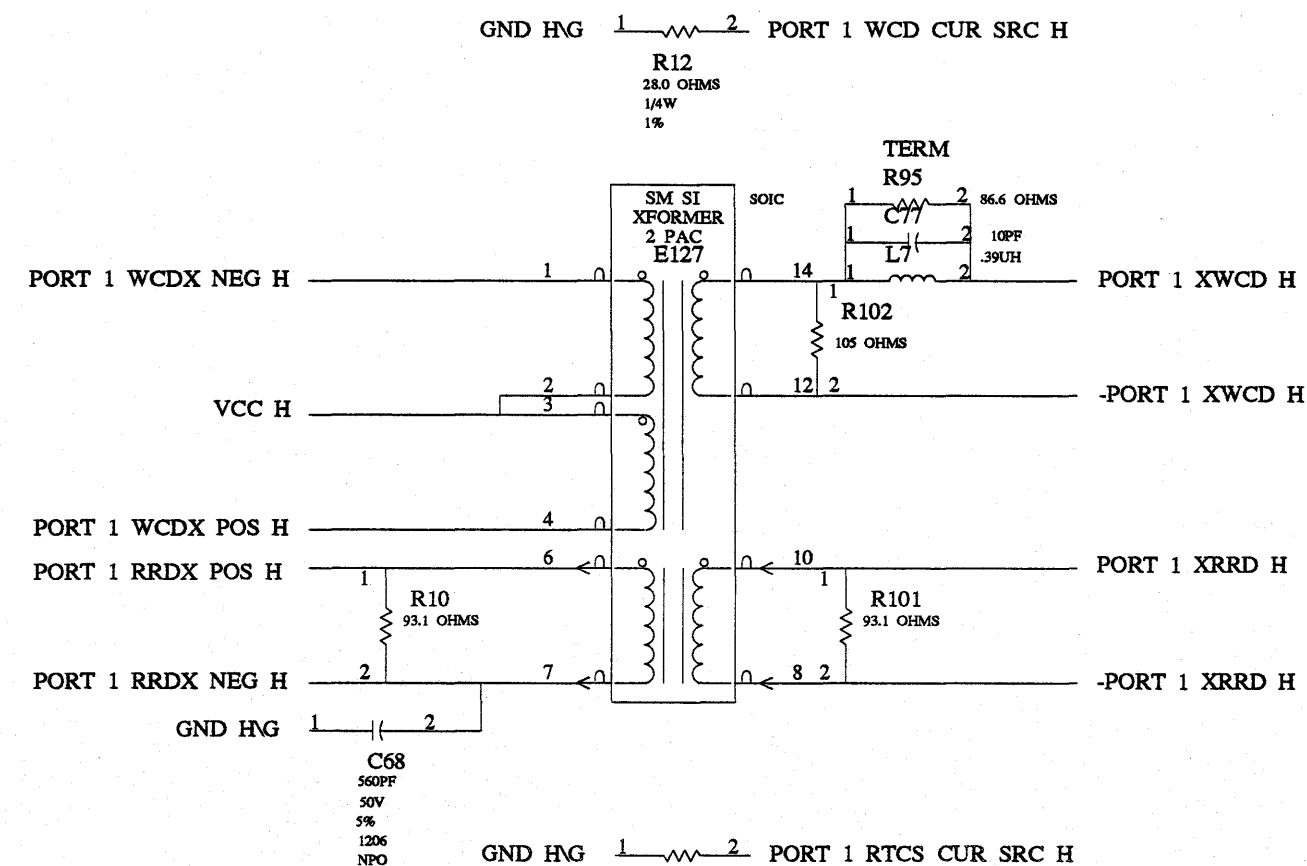
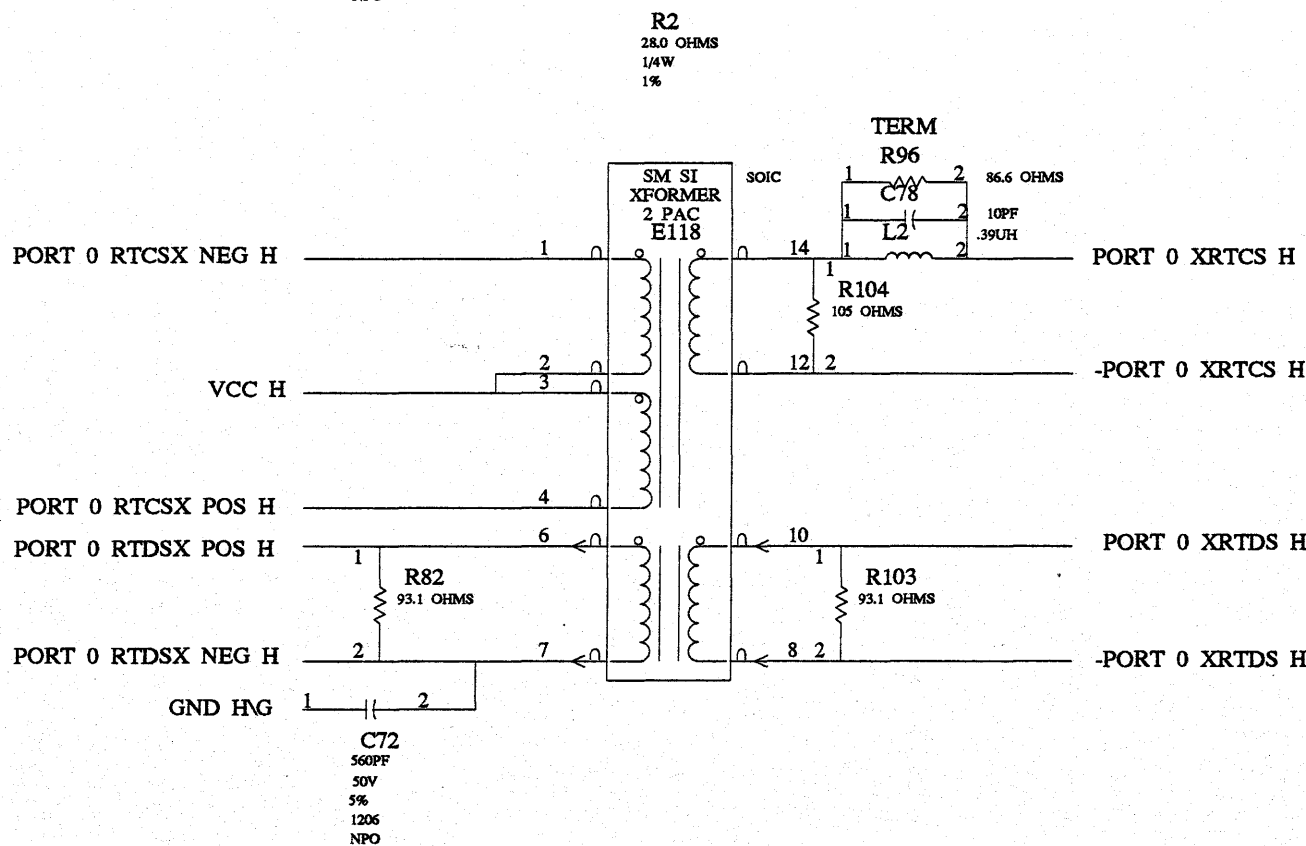
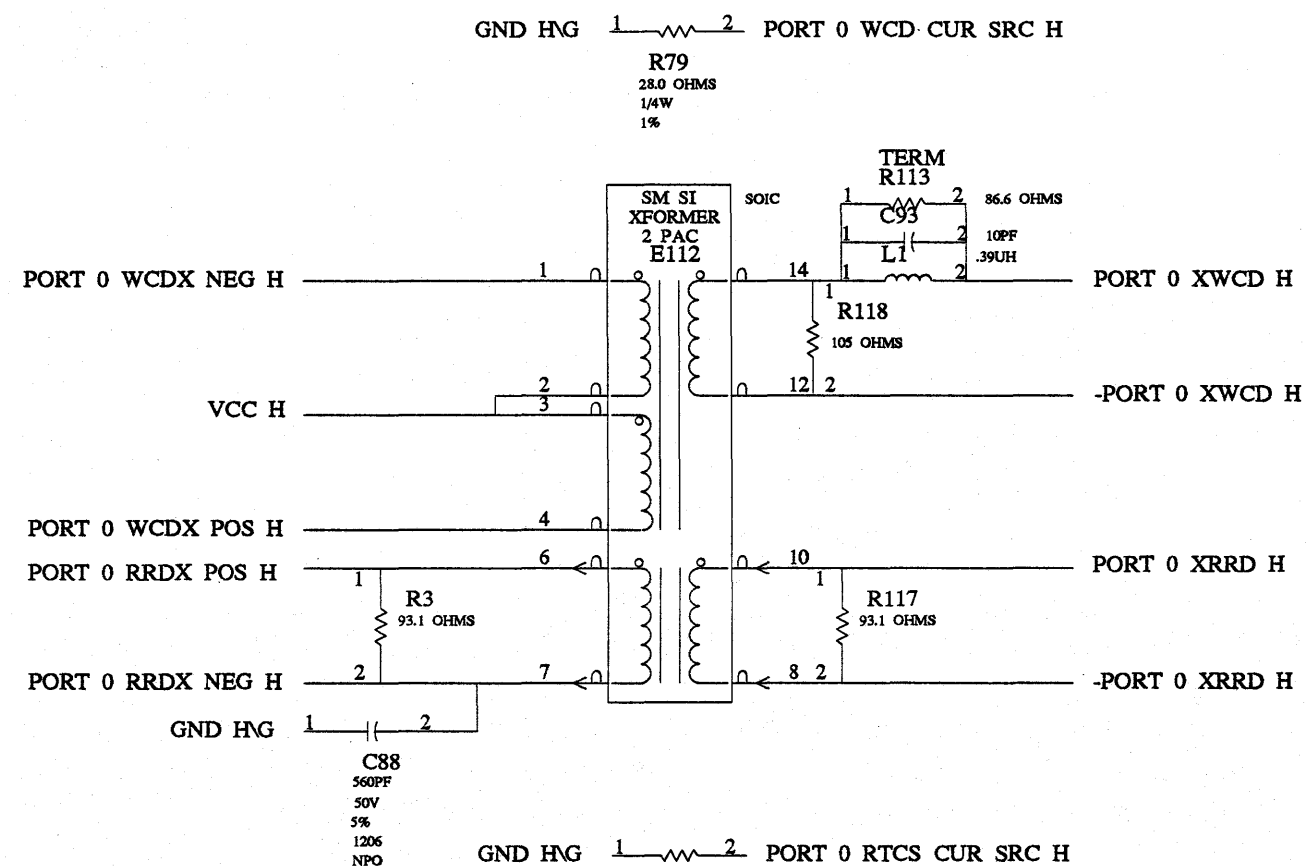
**digital**

DRN: T. Nerger  
 DATE: Mon Oct 17 15:50:52 1988  
 CHK'D:   
 FIRST USED ON OPTION/MODEL:   
 -RGND3 H

DATE	ENG:	DATE	TITLE:
	T. Nerger		WILDCAT BOARD 2

BOARD LOCATION: CXO  
 SHEET 29  
 NEXT HIGHER ASSEMBLY:   
 SIZE K CODE CS NUMBER REV  
 K CS CXO62 17OCT88

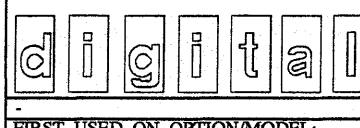
SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

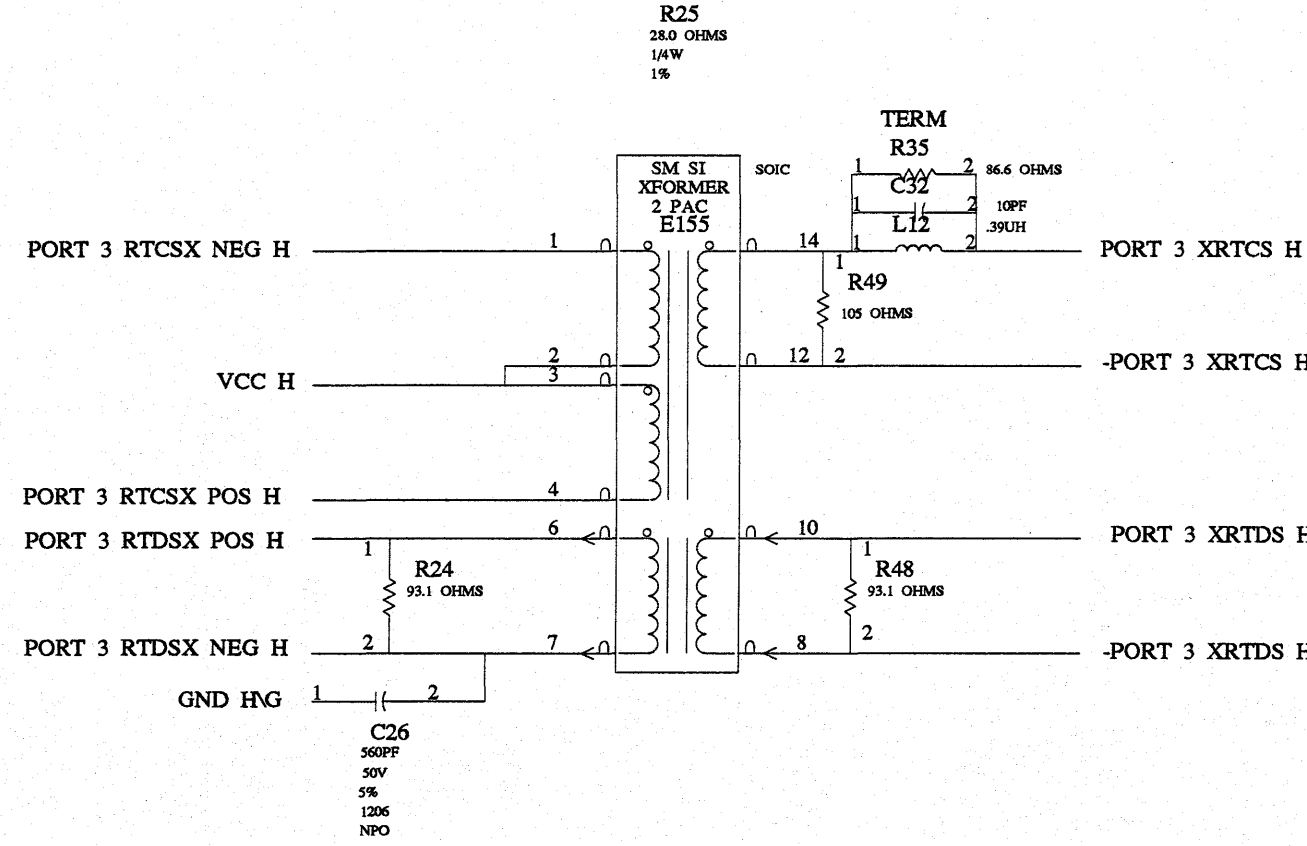
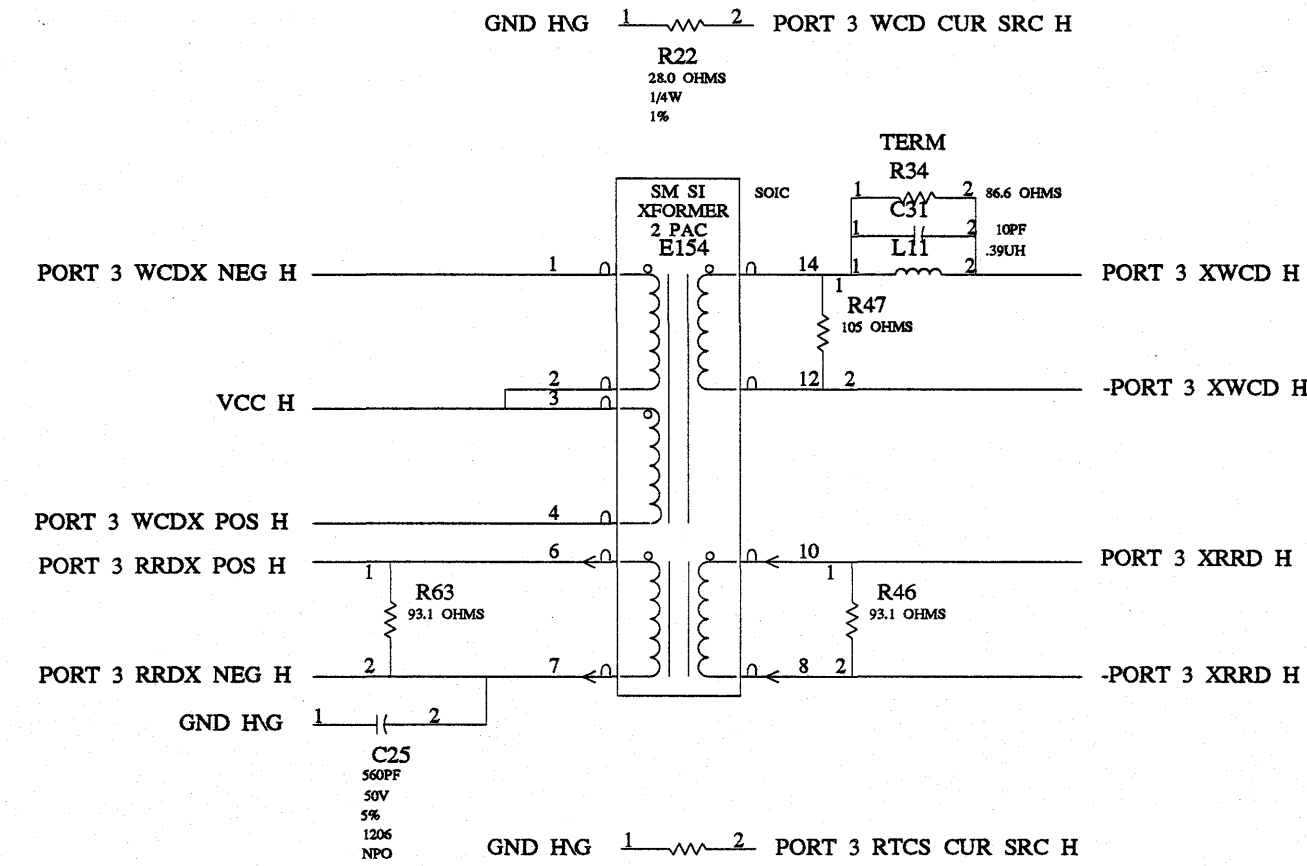
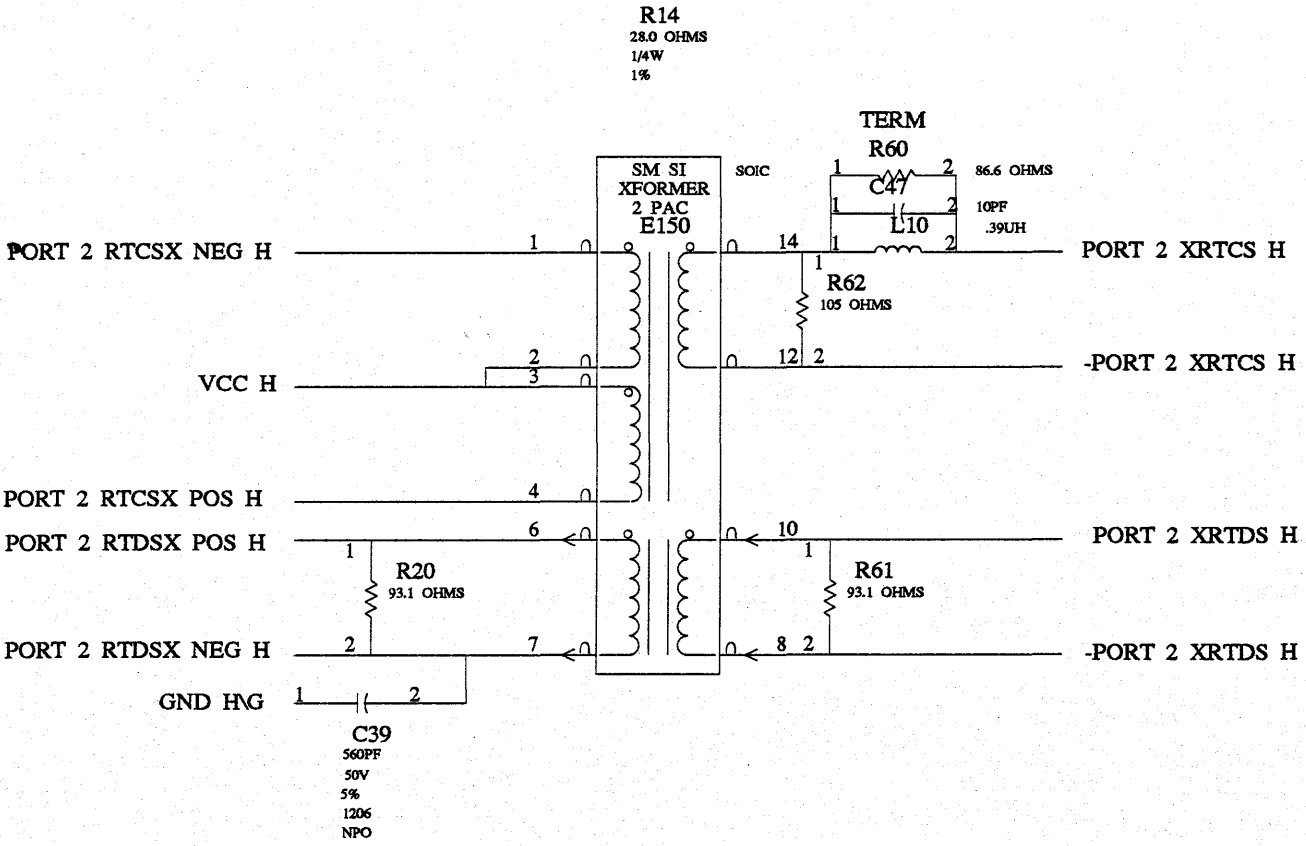
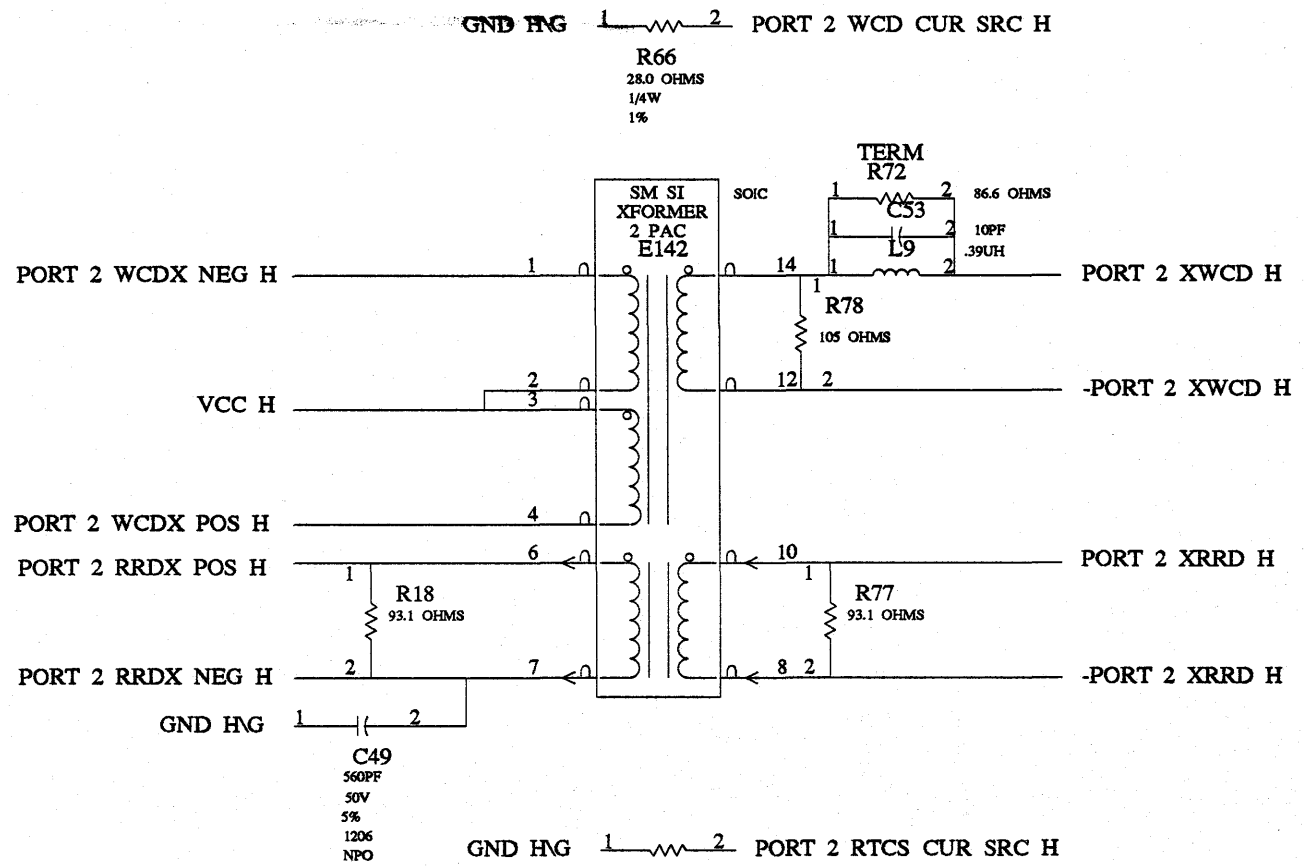
[Logic]  
**TRANSFORMERS & TERMINATORS FOR PORTS 0:1**



DRN: WORTHINGTON  
 DATE  
 CHK'D: DATE  
 FIRST USED ON OPTION/MODEL: Mon Oct 17 15:51:31 1988

ENG: TIM NERGER  
 DATE  
 BOARD LOCATION: CXO  
 SHEET 30  
 NEXT HIGHER ASSEMBLY:

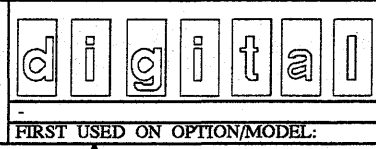
TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

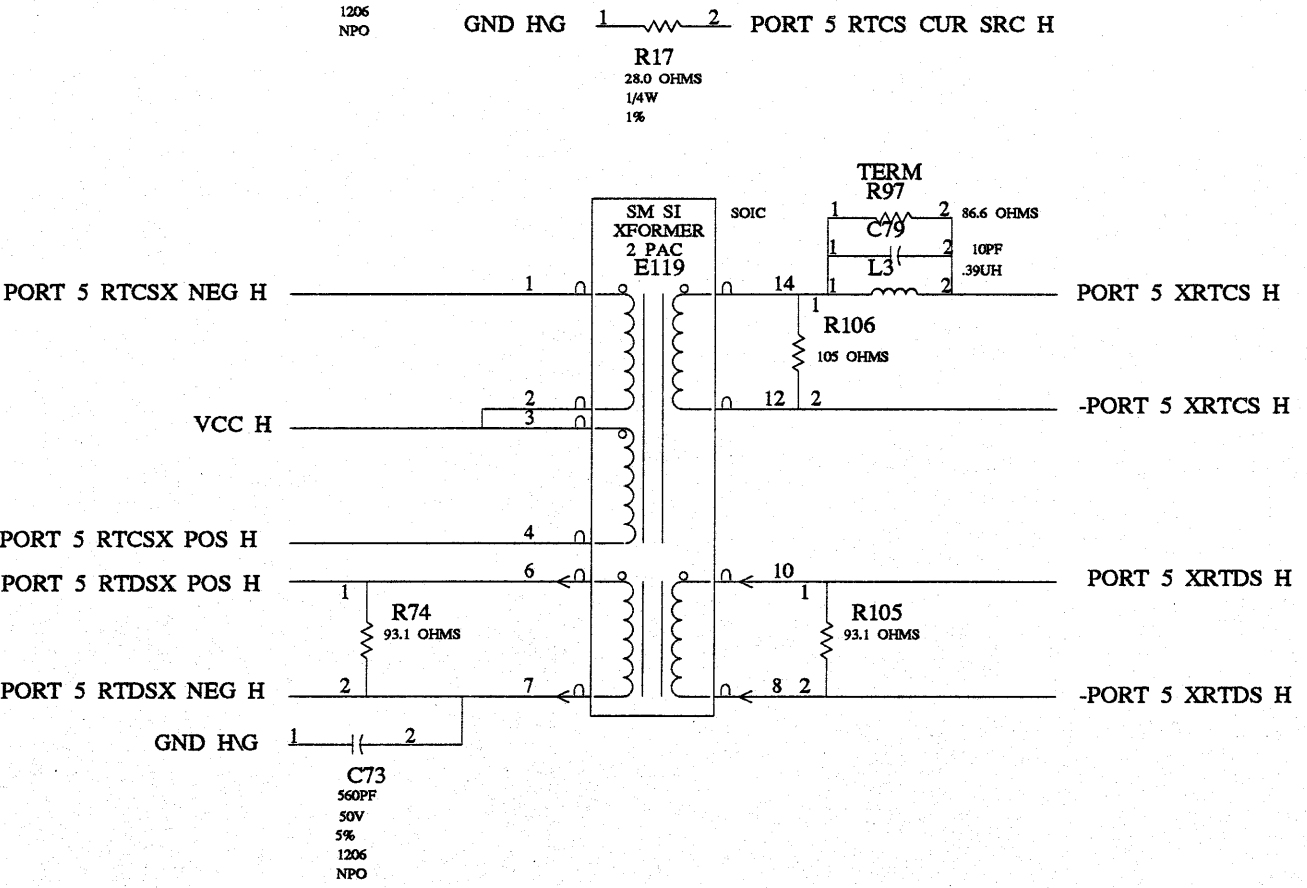
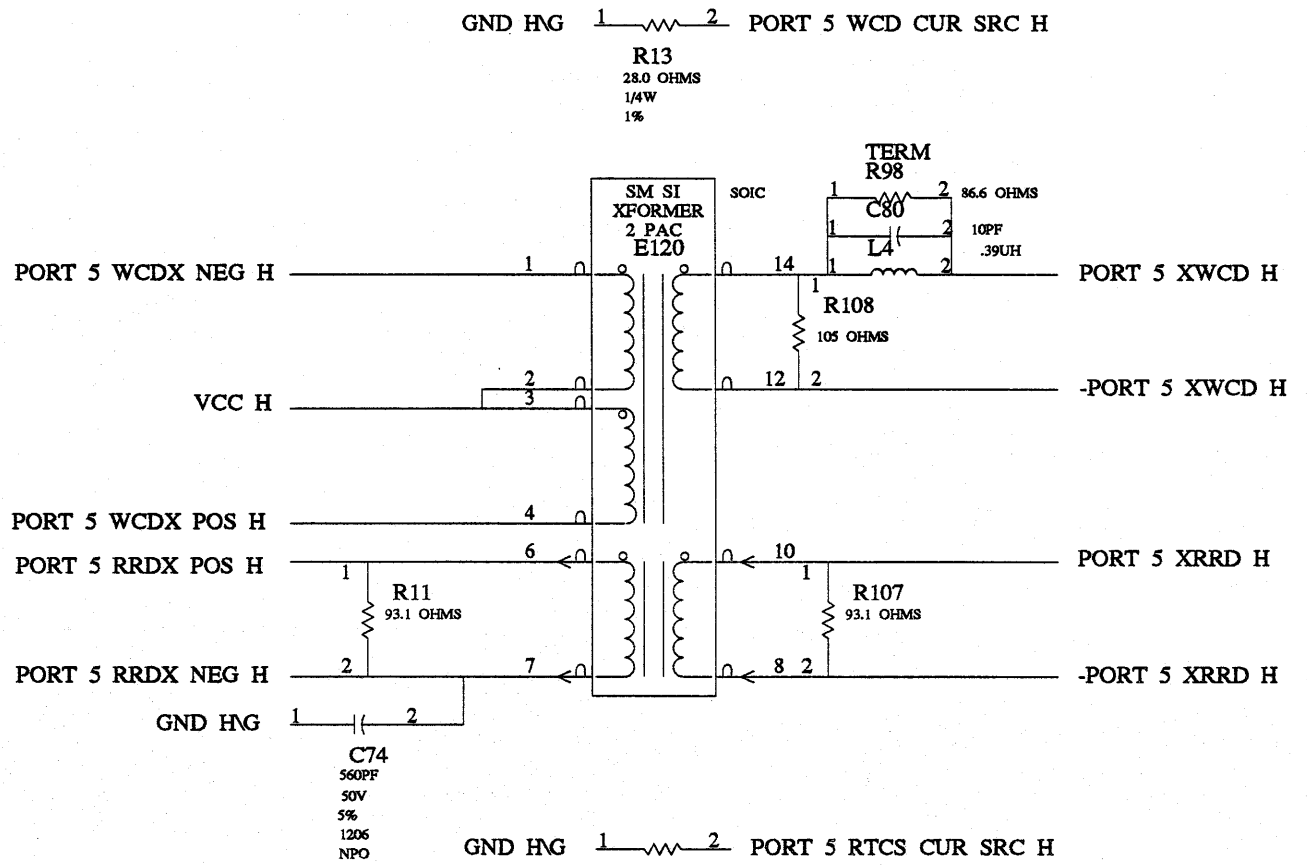
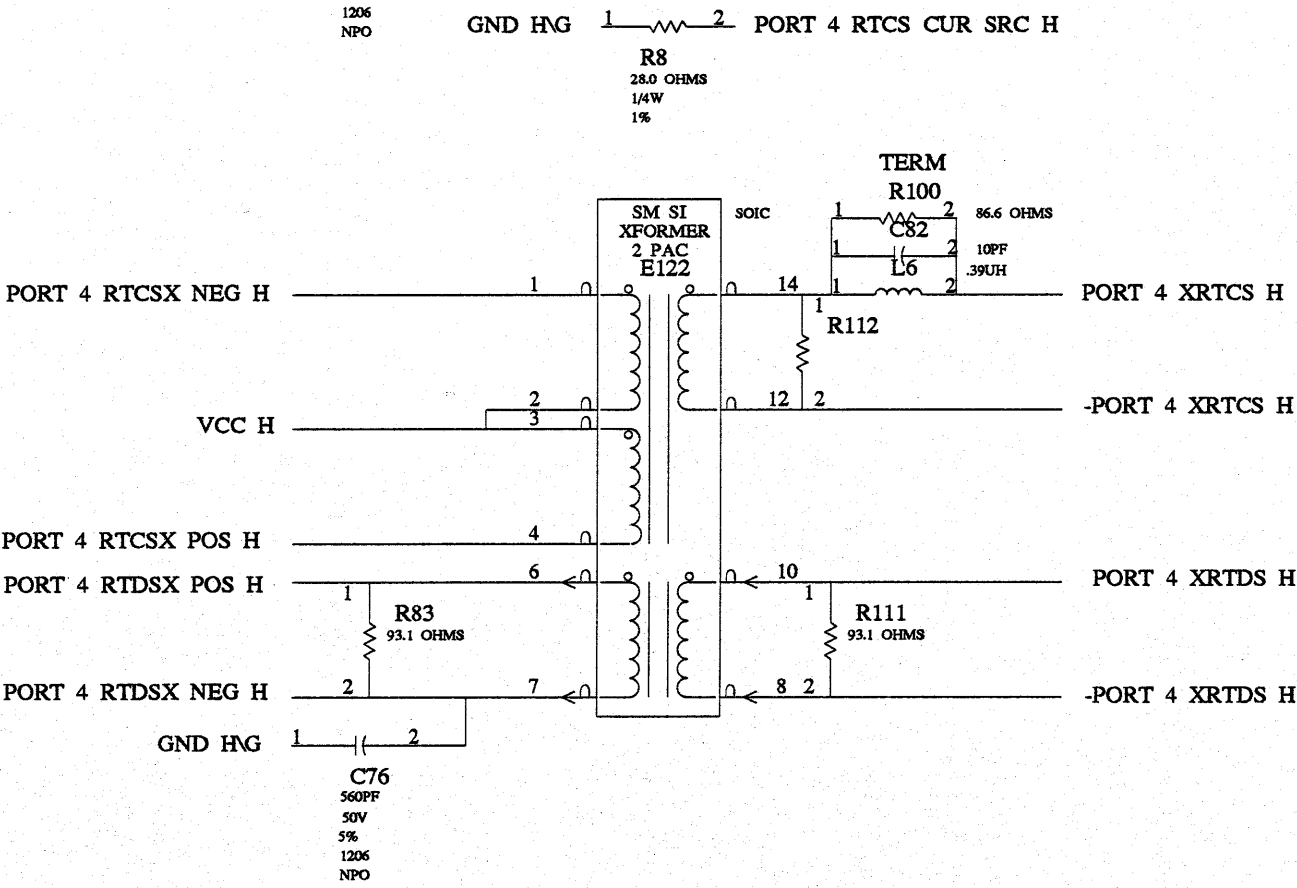
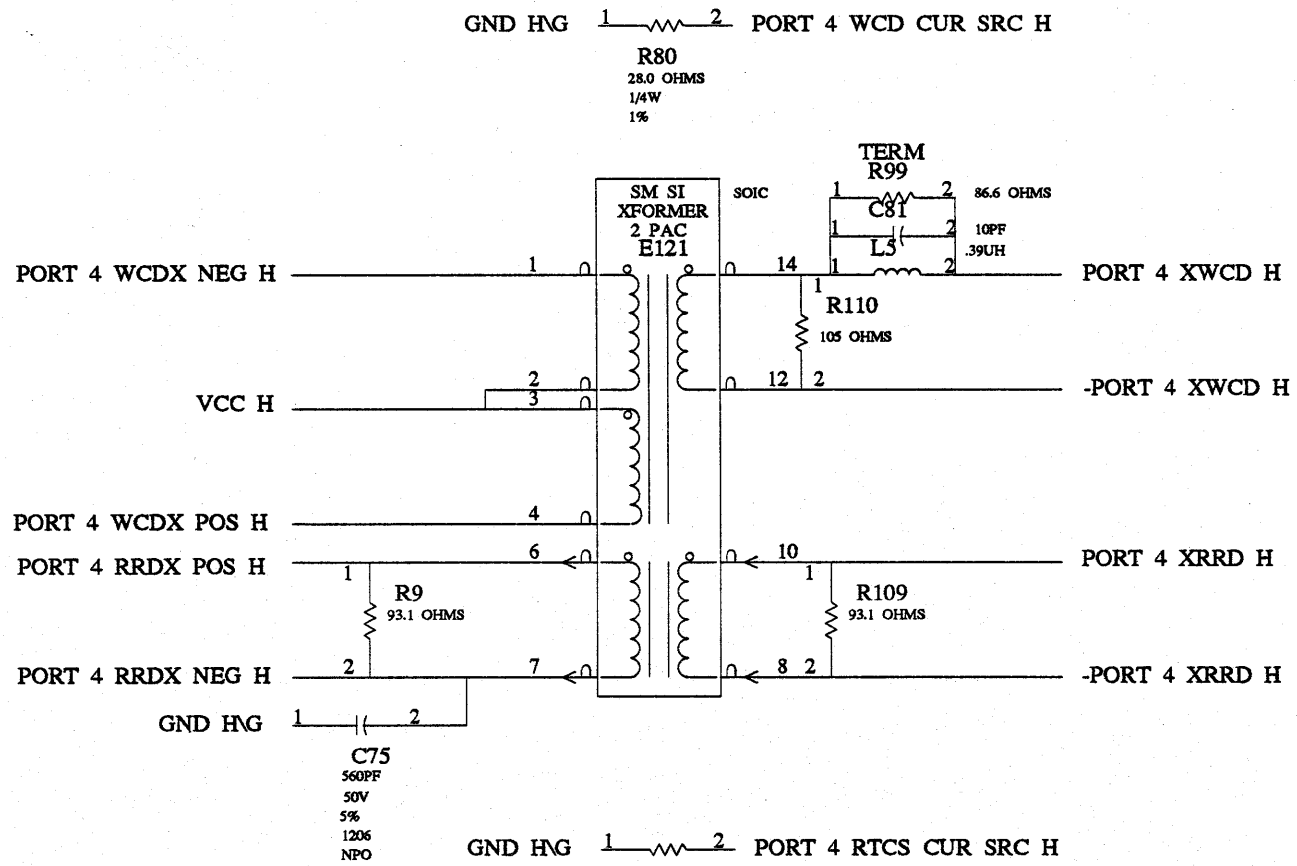
[Logic]  
**TRANSFORMERS & TERMINATORS FOR PORTS 2:3**



DRN: WORTHINGTON  
CHK'D: -  
DATE: -  
Mon Oct 17 15:51:55 1988

ENG: TIM NERGER  
DATE: -  
BOARD LOCATION: CXO  
SHEET 31  
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**TRANSFORMERS & TERMINATORS FOR PORTS 4:5**

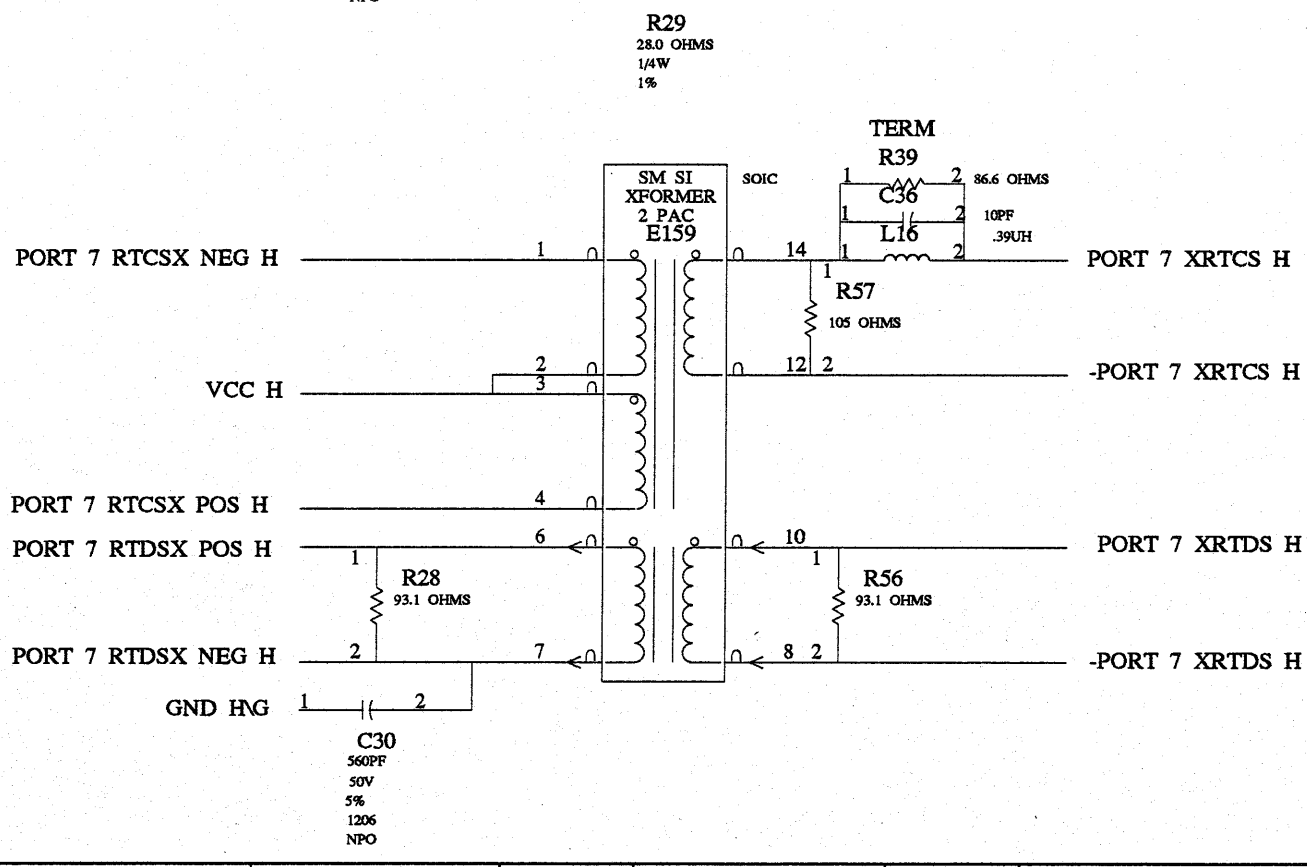
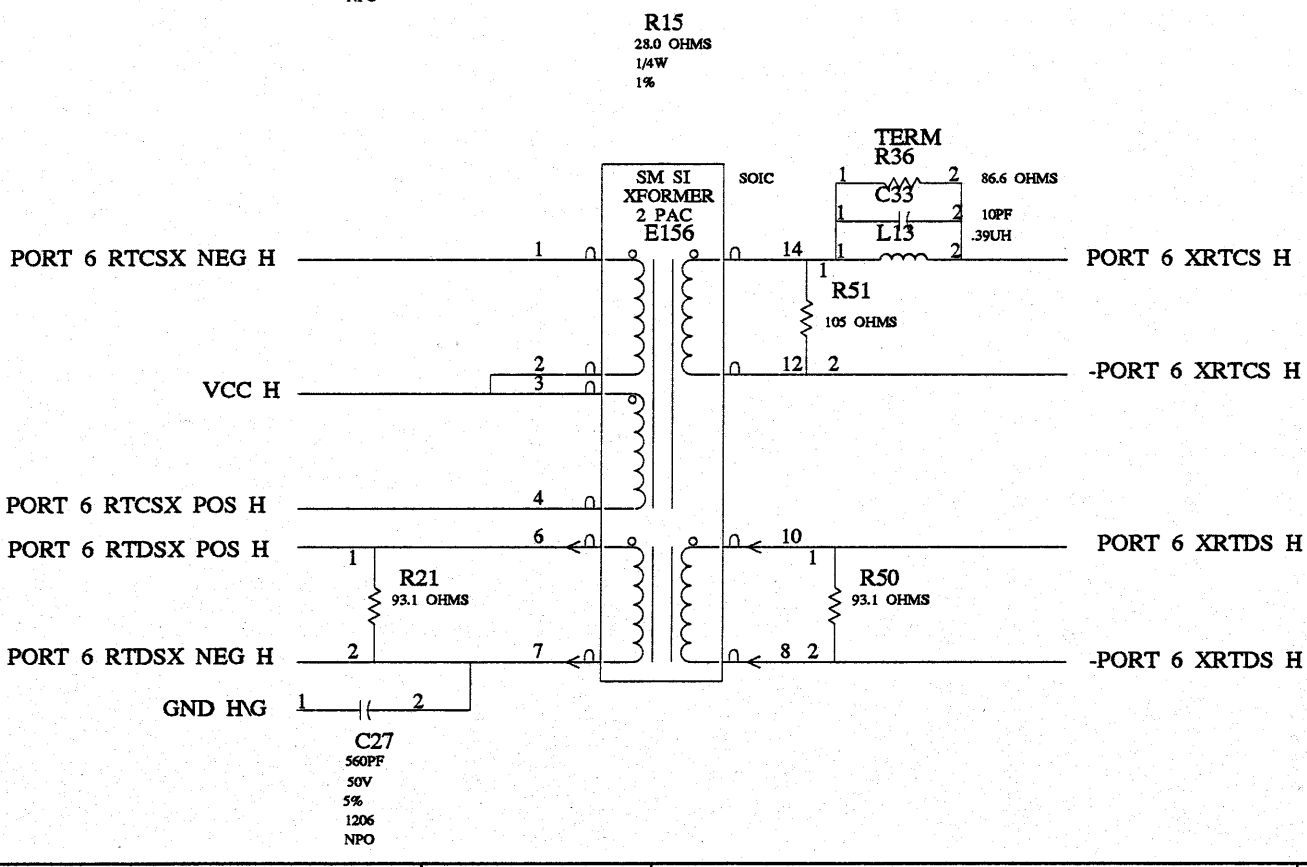
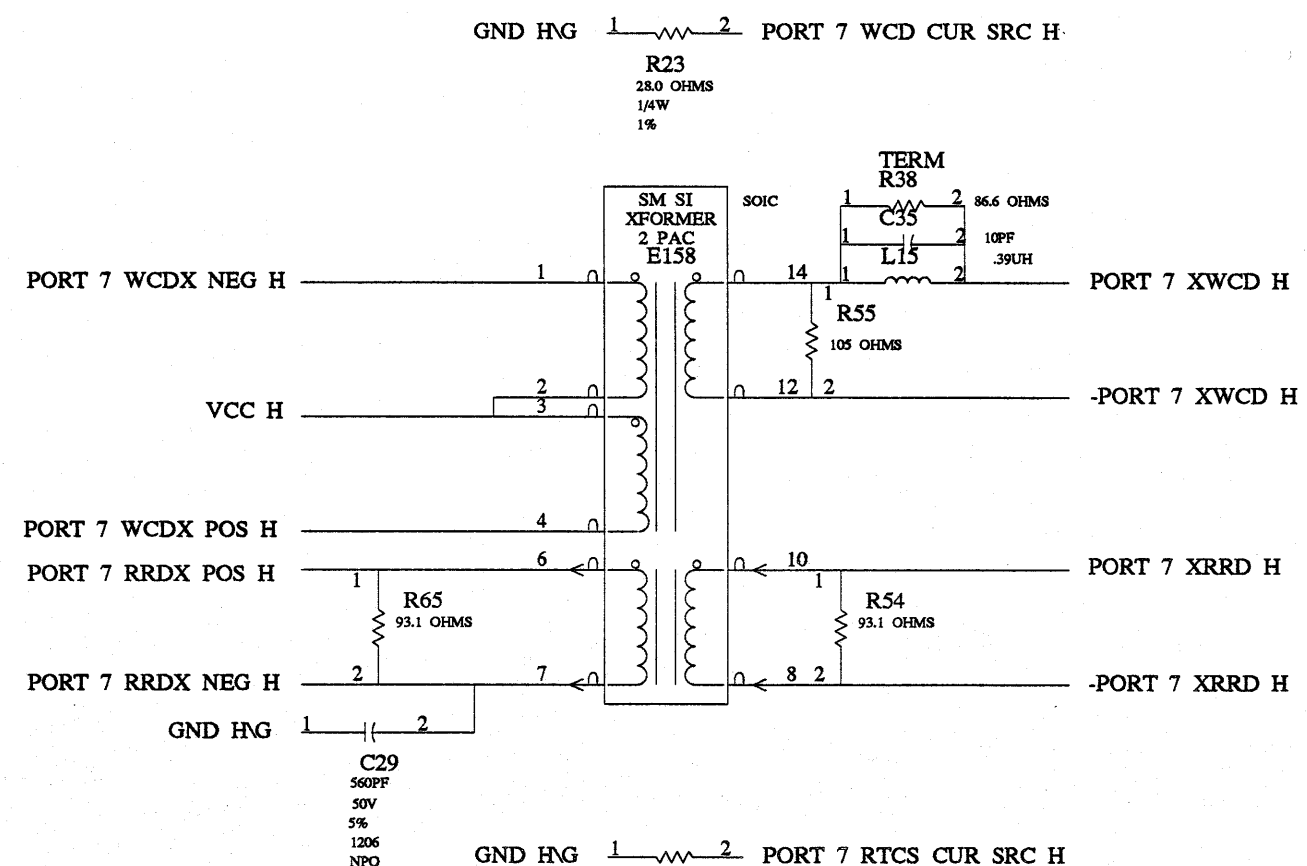
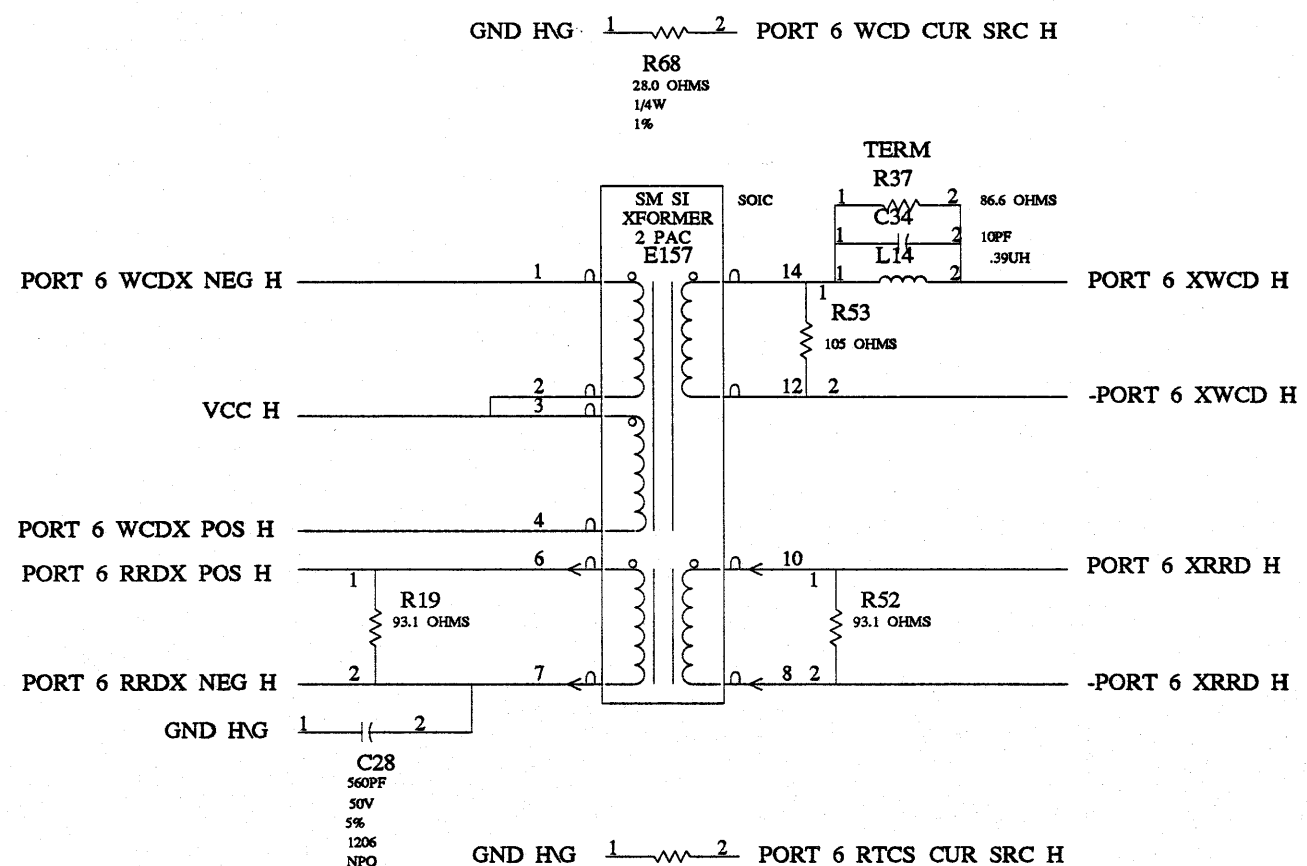
**digital**  
FIRST USED ON OPTION/MODEL: -

DRN: WORTHINGTON  
CHK'D: -  
DATE: -  
Mon Oct 17 15:52:19 1988

ENG: TIM NERGER  
BOARD LOCATION: CXO  
SHEET 32  
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2  
SIZE K  
CODE CS  
NUMBER CXO62  
REV 17OCT88

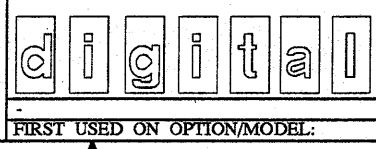




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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**TRANSFORMERS & TERMINATORS FOR PORTS 6:7**



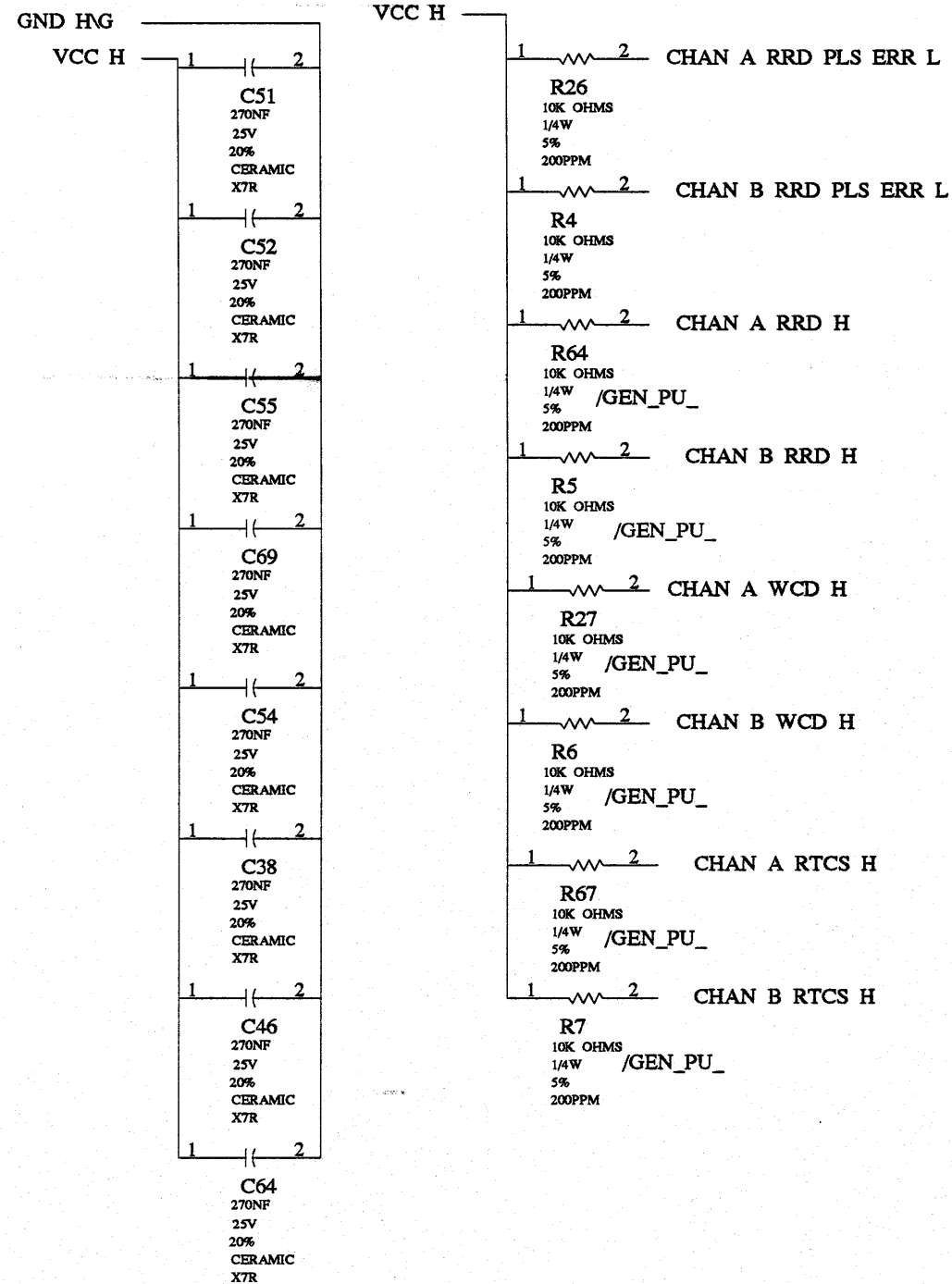
DRN: WORTHINGTON  
 CHK'D: Mon Oct 17 15:52:44 1988

DATE  
 DATE  
 ENG: TIM NERGER  
 BOARD LOCATION: CXO  
 SHEET 33  
 NEXT HIGHER ASSEMBLY:

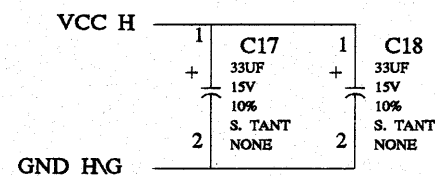
TITLE: WILDCAT BOARD 2  
 SIZE K  
 CODE CS  
 NUMBER CXO62  
 REV 170CT88

8 .27UF CAPS ABOVE ARE FOR THE SIECL AND CSIC CHIPS

SIECL AND CSIC TERMINATION



EXTRA LOW FREQ DECOUPLING CAPS



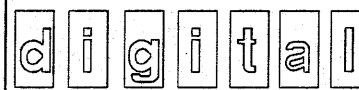
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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]

MISC SI CORNER COMPS



DRN: WORTHINGTON

DATE

ENG: NERGER

DATE

TITLE:

WILDCAT BOARD 2

CHK'D: -

DATE

BOARD LOCATION: CXO

SHEET 34

NEXT HIGHER ASSEMBLY:

SIZE K

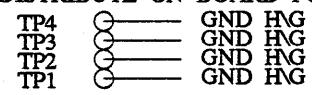
CODE CS

NUMBER CXO62

REV 17OCT88

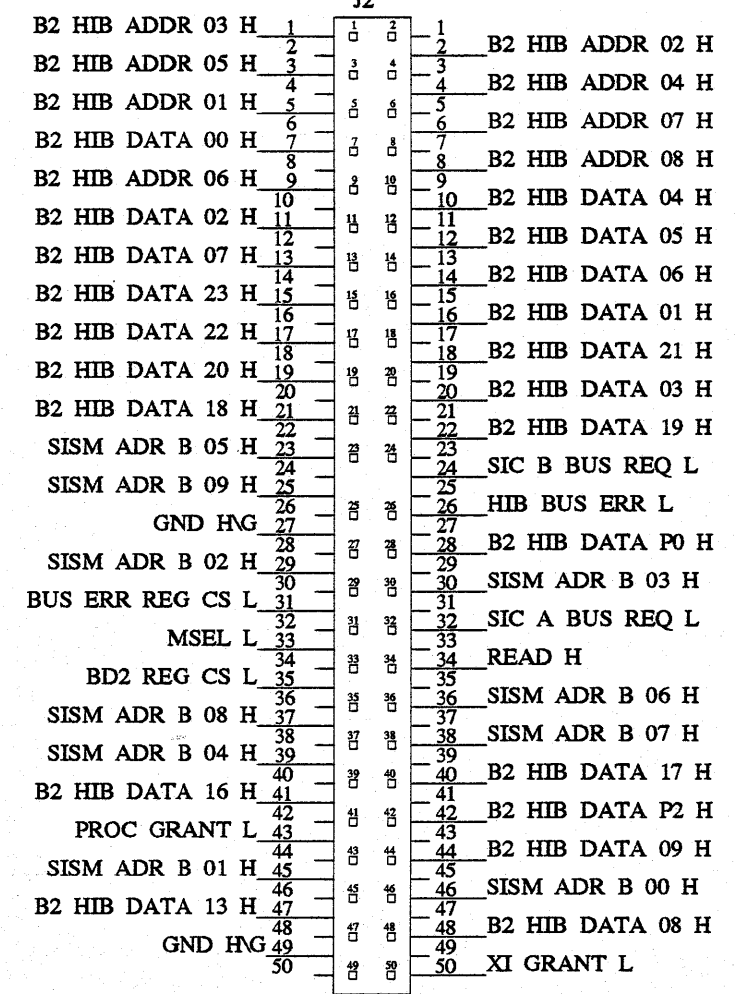
FIRST USED ON OPTION/MODEL: -

DISTRIBUTE ON BOARD FOR SCOPE GNDS



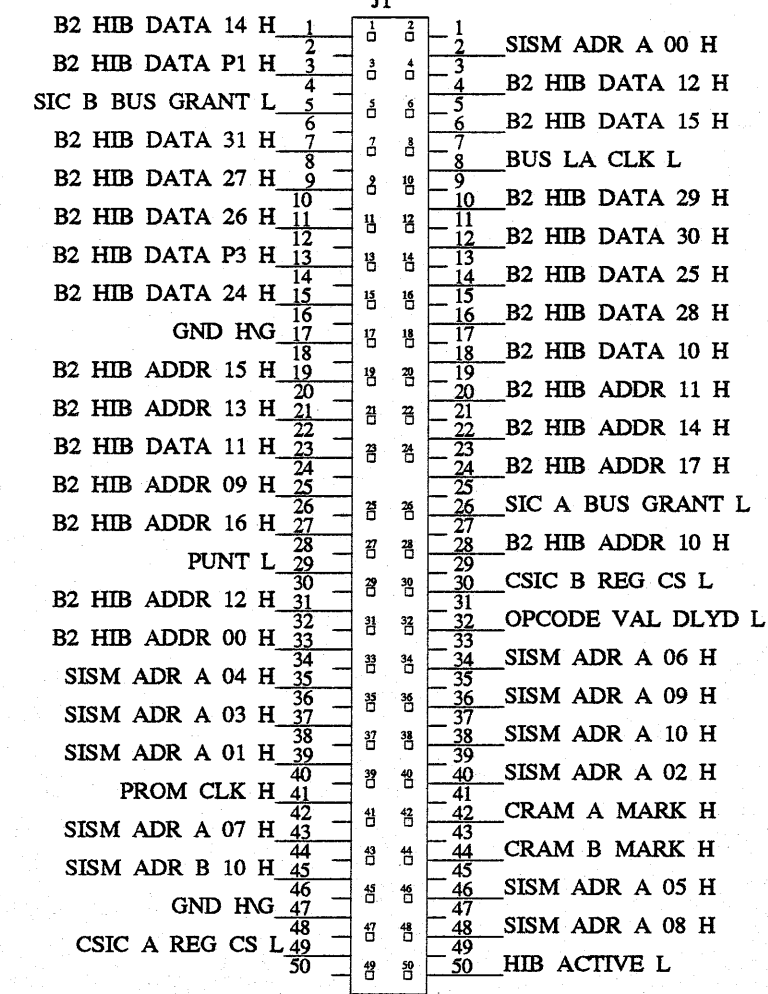
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 MOUNT = STR  
 HOUSING = NONE  
 PINS = .025X.125G  
 KEYING = NONE  
 CONFIG = STD

J2



SPACING = .100CC  
 MOUNT = STR  
 HOUSING = NONE  
 PINS = .025X.125G  
 KEYING = NONE  
 CONFIG = STD

J1



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**VIA LISTING  
 TEST CONNECTORS**

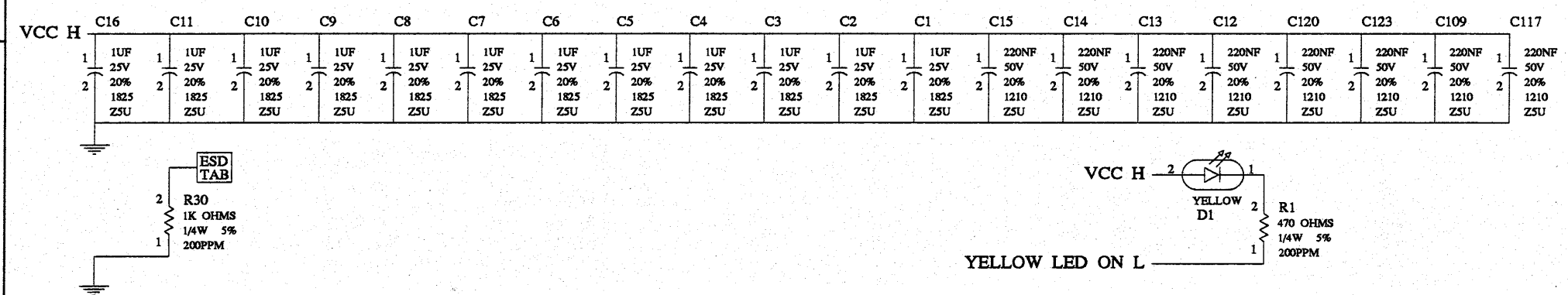
**digital**

FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D: -	DATE	BOARD LOCATION: CXO	SHEET 35
NEXT HIGHER ASSEMBLY: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88

	8	7	6	5	4	3	2	1		
SIDE 1 Board Edge Vias	A 46	XMI TOY BBU OK H	B 46	XMI D27 L	C 46	XMI SPAREBIT0 L	D 46	GND HNG	E 46	-PORT 1 XWCD H
	A 47	XMI D10 L	B 47	XMI SPARE0 L	C 47	XMI CNF0 L	D 47	USER D47 H	E 47	-PORT 1 XRTCS H
	A 48	5VBB H	B 48	VCC H	C 48	NEG 2V H	D 48	USER D48 H	E 48	-PORT 1 XRRD H
	A 49	XMI CON RCV H	B 49	XMI D42 L	C 49	XMI CNF1 L	D 49	USER D49 H	E 49	-PORT 1 XRTDS H
	A 50	XMI D12 L	B 50	GND HNG	C 50	XMI SPAREBIT1 L	D 50	USER D50 H	E 50	NO CONN E50 H
	A 51	XMI D1 L	B 51	GND HNG	C 51	GND HNG	D 51	USER D51 H	E 51	NO CONN E51 H
	A 52	XMI CON XMIT H	B 52	GND HNG	C 52	GND HNG	D 52	USER D52 H	E 52	NO CONN E52 H
	A 53	XMI D16 L	B 53	XMI D37 L	C 53	GND HNG	D 53	USER D53 H	E 53	NO CONN E53 H
	A 54	XMI RUN L	B 54	GND HNG	C 54	XMI DEFAULT H	D 54	USER D54 H	E 54	NO CONN E54 H
	A 55	XMI RESET L	B 55	XMI P1 L	C 55	XMI DC LO L	D 55	USER D55 H	E 55	NO CONN E55 H
A 56	GND HNG	B 56	GND HNG	C 56	GND HNG	D 56	USER D56 H	E 56	-PORT 6 XWCD H	
A 57	XMI D11 L	B 57	XMI D60 L	C 57	XMI TIME L	D 57	USER D57 H	E 57	-PORT 6 XRTCS H	
A 58	GND HNG	B 58	VEE H	C 58	GND HNG	D 58	USER D58 H	E 58	-PORT 6 XRRD H	
A 59	XMI D36 L	B 59	XMI LOCKOUT L	C 59	XMI TIME H	D 59	USER D59 H	E 59	-PORT 6 XRTDS H	
A 60	XMI CON SECURE L	B 60	GND HNG	C 60	GND HNG	D 60	USER D60 H	E 60	NO CONN E60 H	
Inside Vias	A 16	XMI D13 L	B 16	XMI D38 L	C 16	XMI AC LO L	D 16	EXTERNAL DIAG CLK H	E 16	PORT 1 XWCD H
	A 17	XMI D14 L	B 17	XMI D41 L	C 17	XMI F2 L	D 17	USER D17 H	E 17	PORT 1 XRTCS H
	A 18	5VBB H	B 18	VCC H	C 18	3V H	D 18	USER D18 H	E 18	PORT 1 XRRD H
	A 19	5VBB H	B 19	VCC H	C 19	3V H	D 19	USER D19 H	E 19	PORT 1 XRTDS H
	A 20	XMI D19 L	B 20	XMI D39 L	C 20	XMI ID4 L	D 20	USER D20 H	E 20	NO CONN E20 H
	A 21	XMI D20 L	B 21	XMI D58 L	C 21	XMI ID3 L	D 21	USER D21 H	E 21	NO CONN E21 H
	A 22	XMI D21 L	B 22	XMI D55 L	C 22	XMI ID2 L	D 22	USER D22 H	E 22	NO CONN E22 H
	A 23	XMI D17 L	B 23	XMI D56 L	C 23	XMI ID1 L	D 23	USER D23 H	E 23	NO CONN E23 H
	A 24	XMI D15 L	B 24	XMI D57 L	C 24	XMI ID0 L	D 24	USER D24 H	E 24	NO CONN E24 H
	A 25	XMI D32 L	B 25	XMI D59 L	C 25	XMI F3 L	D 25	USER D25 H	E 25	NO CONN E25 H
A 26	XMI D33 L	B 26	XMI D61 L	C 26	XMI F2 L	D 26	USER D26 H	E 26	PORT 6 XWCD H	
A 27	XMI D34 L	B 27	XMI D62 L	C 27	GND HNG	D 27	USER D27 H	E 27	PORT 6 XRTCS H	
A 28	GND HNG	B 28	VCC H	C 28	GND HNG	D 28	USER D28 H	E 28	PORT 6 XRRD H	
A 29	GND HNG	B 29	VCC H	C 29	GND HNG	D 29	USER D29 H	E 29	PORT 6 XRTDS H	
A 30	XMI D35 L	B 30	XMI D63 L	C 30	GND HNG	D 30	USER D30 H	E 30	NO CONN E30 H	
XMI Corner										
SIDE 2 Inside Vias	A 1	XMI D9 L	B 1	XMI D25 L	C 1	GND HNG	D 1	NO CONN D1 H	E 1	NO CONN E1 H
	A 2	XMI D8 L	B 2	XMI D24 L	C 2	XMI ID5 L	D 2	-PORT 4 XRTDS H	E 2	-PORT 2 XRTDS H
	A 3	5VBB H	B 3	VCC H	C 3	3V H	D 3	-PORT 4 XRRD H	E 3	-PORT 2 XRRD H
	A 4	XMI D7 L	B 4	XMI D23 L	C 4	GND HNG	D 4	-PORT 4 XRTCS H	E 4	-PORT 2 XRTCS H
	A 5	XMI D5 L	B 5	XMI D22 L	C 5	XMI HOLD L	D 5	-PORT 4 XWCD H	E 5	-PORT 2 XWCD H
	A 6	XMI D4 L	B 6	XMI D53 L	C 6	XMI NODEID0 H	D 6	NO CONN D6 H	E 6	NO CONN E6 H
	A 7	XMI D2 L	B 7	XMI D52 L	C 7	XMI NODEID1 H	D 7	-PORT 5 XRTDS H	E 7	-PORT 3 XRTDS H
	A 8	XMI D6 L	B 8	XMI D51 L	C 8	XMI NODEID2 H	D 8	-PORT 5 XRRD H	E 8	-PORT 3 XRRD H
	A 9	XMI D3 L	B 9	XMI D50 L	C 9	XMI NODEID3 H	D 9	-PORT 5 XRTCS H	E 9	-PORT 3 XRTCS H
	A 10	XMI FAULT L	B 10	XMI D49 L	C 10	GND HNG	D 10	-PORT 5 XWCD H	E 10	-PORT 3 XWCD H
A 11	XMI D29 L	B 11	XMI D48 L	C 11	XMI F1 L	D 11	NO CONN D11 H	E 11	NO CONN E11 H	
A 12	XMI P0 L	B 12	XMI D47 L	C 12	XMI F0 L	D 12	-PORT 0 XRTDS H	E 12	-PORT 7 XRTDS H	
A 13	GND HNG	B 13	VCC H	C 13	GND HNG	D 13	-PORT 0 XRRD H	E 13	-PORT 7 XRRD H	
A 14	XMI D31 L	B 14	XMI D46 L	C 14	GND HNG	D 14	-PORT 0 XRTCS H	E 14	-PORT 7 XRTCS H	
A 15	XMI D28 L	B 15	XMI D45 L	C 15	GND HNG	D 15	-PORT 0 XWCD H	E 15	-PORT 7 XWCD H	
Board Edge Vias	A 31	XMI SUP L	B 31	XMI D40 L	C 31	XMI D43 L	D 31	NO CONN D31 H	E 31	NO CONN E31 H
	A 32	GND HNG	B 32	GND HNG	C 32	GND HNG	D 32	PORT 4 XRTDS H	E 32	PORT 2 XRTDS H
	A 33	5VBB H	B 33	VCC H	C 33	NEG 2V H	D 33	PORT 4 XRRD H	E 33	PORT 2 XRRD H
	A 34	5VBB H	B 34	VCC H	C 34	NEG 2V H	D 34	PORT 4 XRTCS H	E 34	PORT 2 XRTCS H
	A 35	XMI SPAREBIT2 L	B 35	XMI D26 L	C 35	XMI CNF2 L	D 35	PORT 4 XWCD H	E 35	PORT 2 XWCD H
	A 36	GND HNG	B 36	GND HNG	C 36	GND HNG	D 36	NO CONN D36 H	E 36	NO CONN E36 H
	A 37	XMI SPAREBIT3 L	B 37	XMI BAD L	C 37	12V H	D 37	PORT 5 XRTDS H	E 37	PORT 3 XRTDS H
	A 38	XMI D18 L	B 38	XMI D54 L	C 38	XMI CMD REQ L	D 38	PORT 5 XRRD H	E 38	PORT 3 XRRD H
	A 39	XMI SPAREBIT4 L	B 39	GND HNG	C 39	NEG 12V H	D 39	PORT 5 XRTCS H	E 39	PORT 3 XRTCS H
	A 40	GND HNG	B 40	XMI BOOT EN L	C 40	XMI RES REQ L	D 40	PORT 5 XWCD H	E 40	PORT 3 XWCD H
A 41	XMI D0 L	B 41	XMI UPDATE EN H	C 41	GND HNG	D 41	NO CONN D41 H	E 41	NO CONN E41 H	
A 42	XMI TOY BBU PWR H	B 42	GND HNG	C 42	XMI GRANT L	D 42	PORT 0 XRTDS H	E 42	PORT 7 XRTDS H	
A 43	GND HNG	B 43	VEE H	C 43	GND HNG	D 43	PORT 0 XRRD H	E 43	PORT 7 XRRD H	
A 44	GND HNG	B 44	VEE H	C 44	GND HNG	D 44	PORT 0 XRTCS H	E 44	PORT 7 XRTCS H	
A 45	XMI D30 L	B 45	XMI D44 L	C 45	XMI PHASE L	D 45	PORT 0 XWCD H	E 45	PORT 7 XWCD H	



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
XMI CORNER PINS  
NOT USED ON BOARD 2

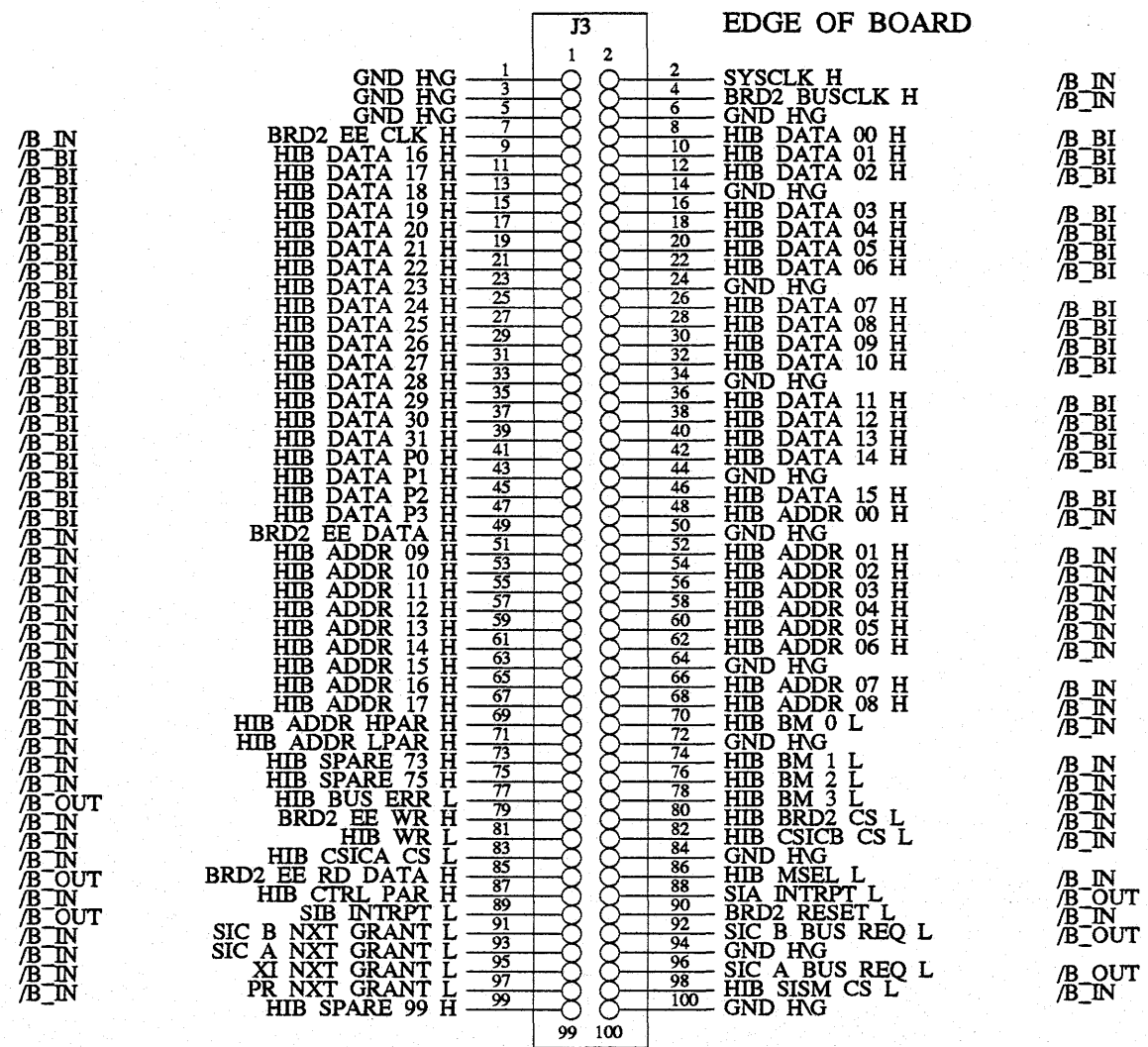
digital

FIRST USED ON OPTION/MODEL:

DRN: K. Yesse	DATE 12-Feb-1988	ENG: WORTHINGTON	DATE	TITLE: WILDCAT BOARD 2
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 36	SIZE K
Tue Oct 25 16:42:21 1988	NEXT HIGHER ASSEMBLY:	NUMBER CXO62	REV 25OCT88	

SPACING = .100CC  
 MOUNT = 90D  
 HOUSING = SHROUD W/O LTCH  
 KEYING = NONE  
 CONFIG = STD  
 PINS = .022X.100G

EDGE OF BOARD



NOTE: Connector pins have a property, IO\_DIRECTION, set according to input/output/bidirectional status.

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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**BOARD 1 <-> BOARD 2**  
**HIB BUS CONNECTOR**

**digital**

DRN: Worthington      DATE:      ENG: C. D. Light      DATE:      TITLE: WILDCAT BOARD 2

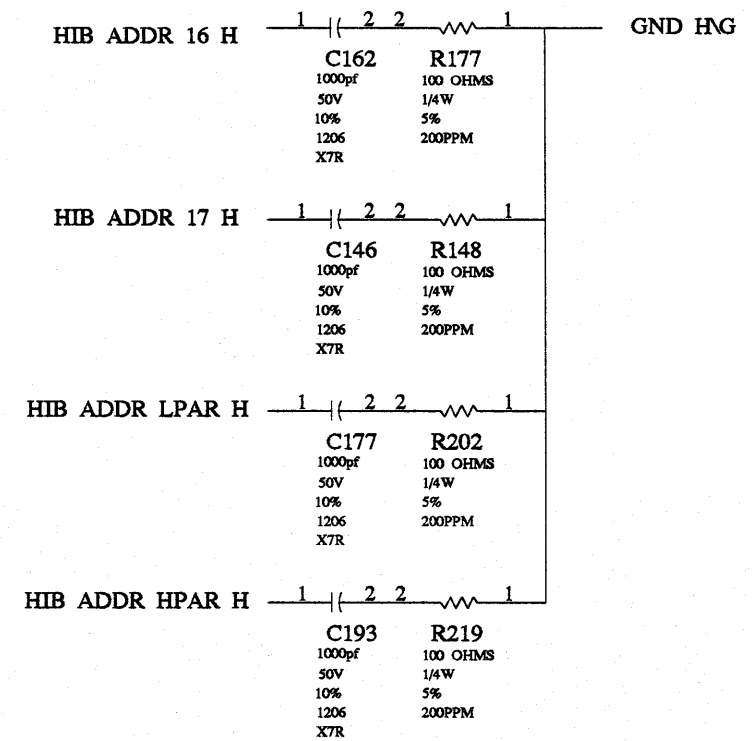
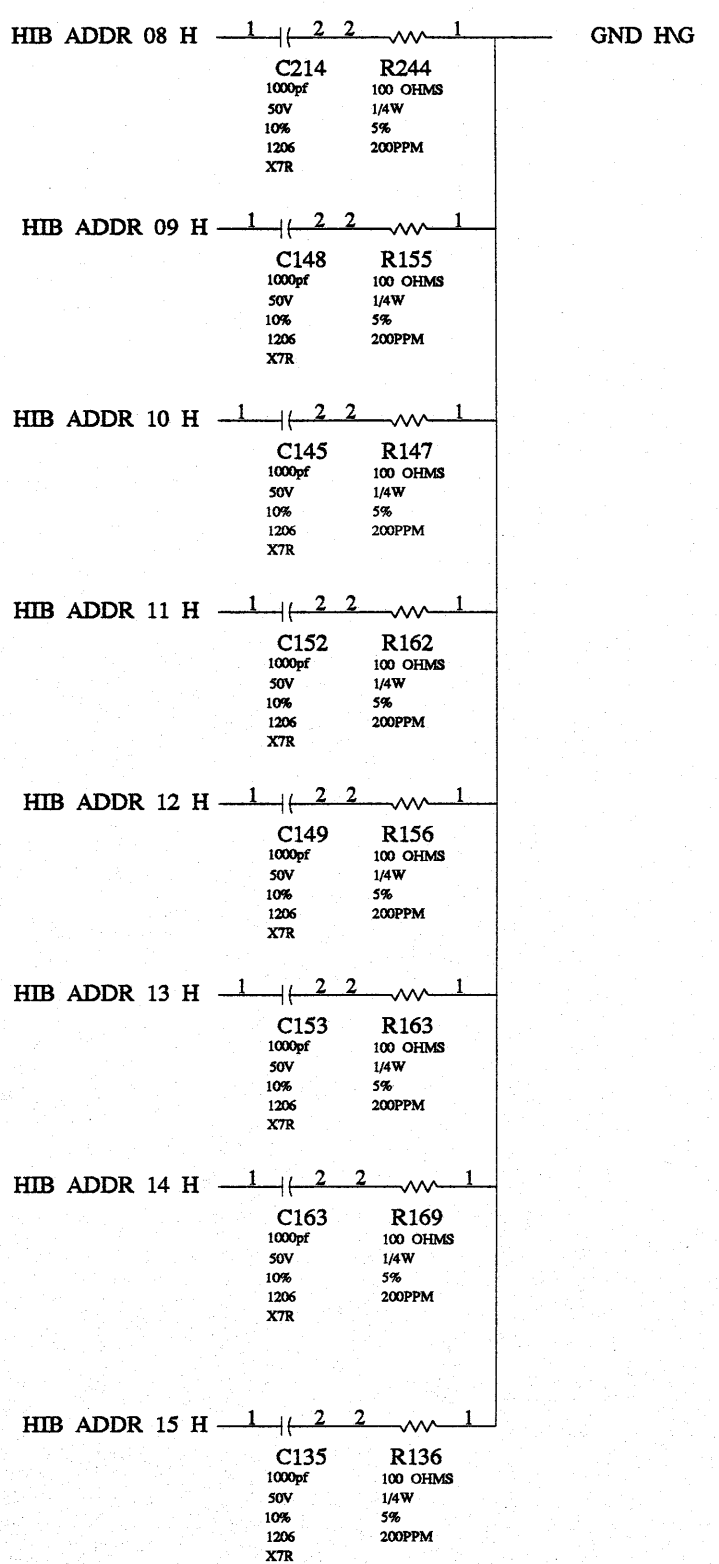
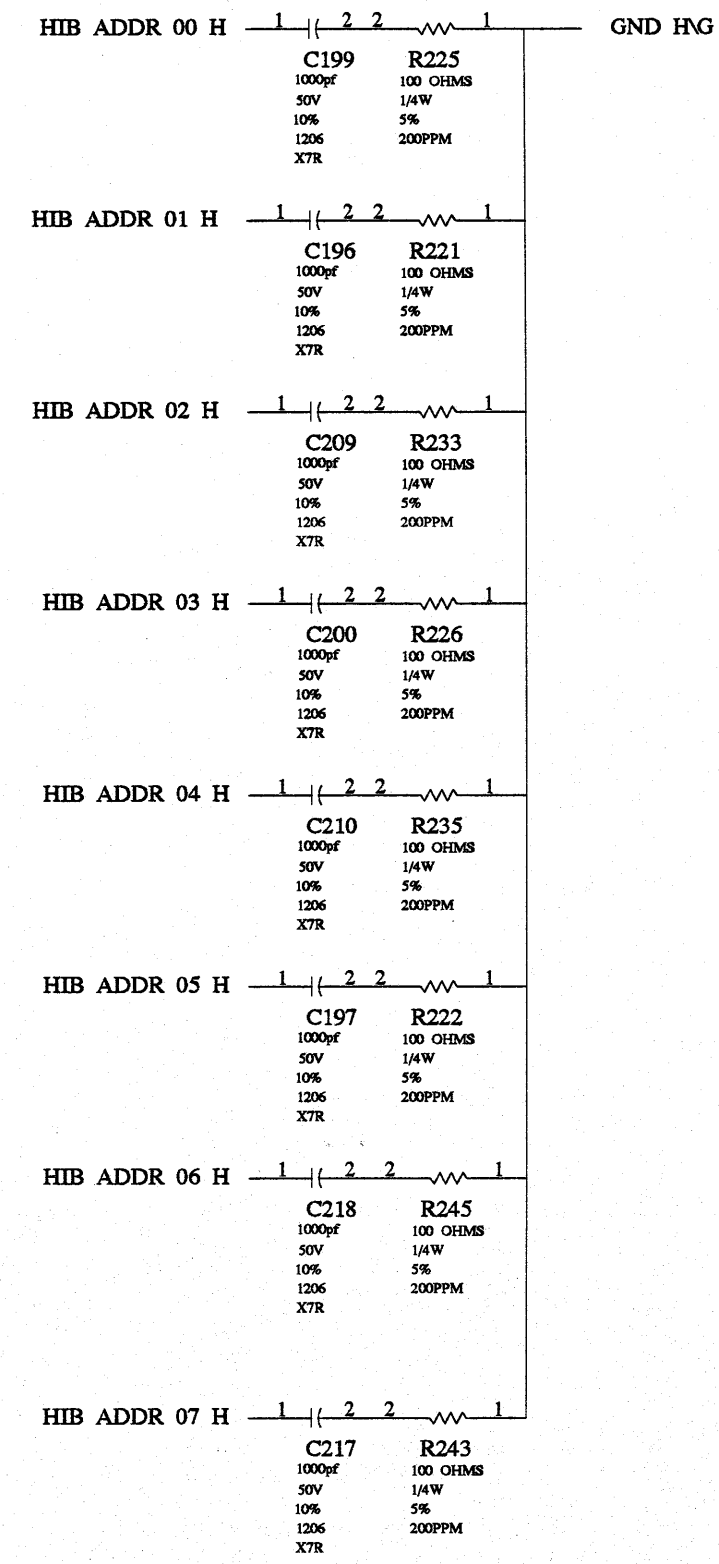
CHK'D:      DATE:      BOARD LOCATION: CXO

Mon Oct 17 16:00:03 1988      SHEET 37

FIRST USED ON OPTION/MODEL:      NEXT HIGHER ASSEMBLY:

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

D  
C  
B  
A

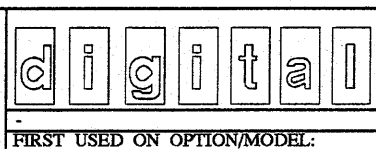


D  
C  
B  
A

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REVISIONS		
CHK	CHANGE NO.	REV

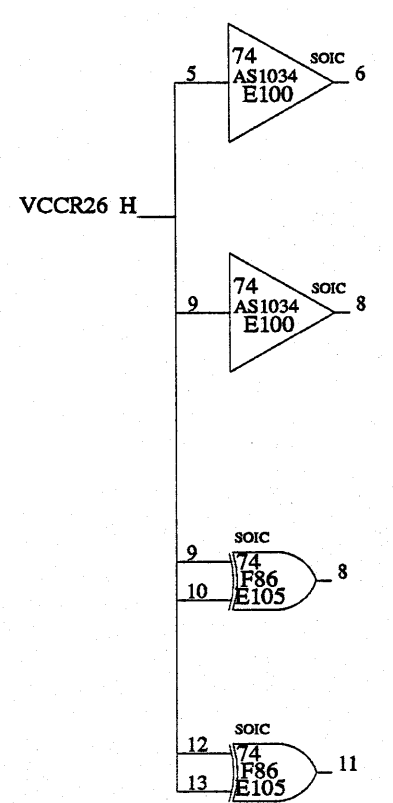
[Logic]  
HIB ADDR R/C NETWORKS



DRN: T. Nerger  
DATE: -  
CHK'D: -  
DATE: -  
FIRST USED ON OPTION/MODEL: -

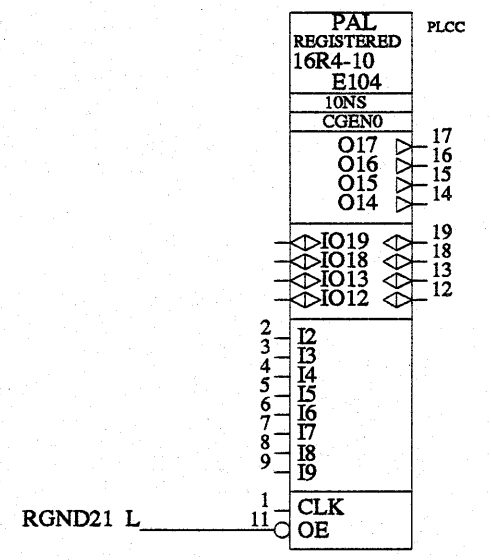
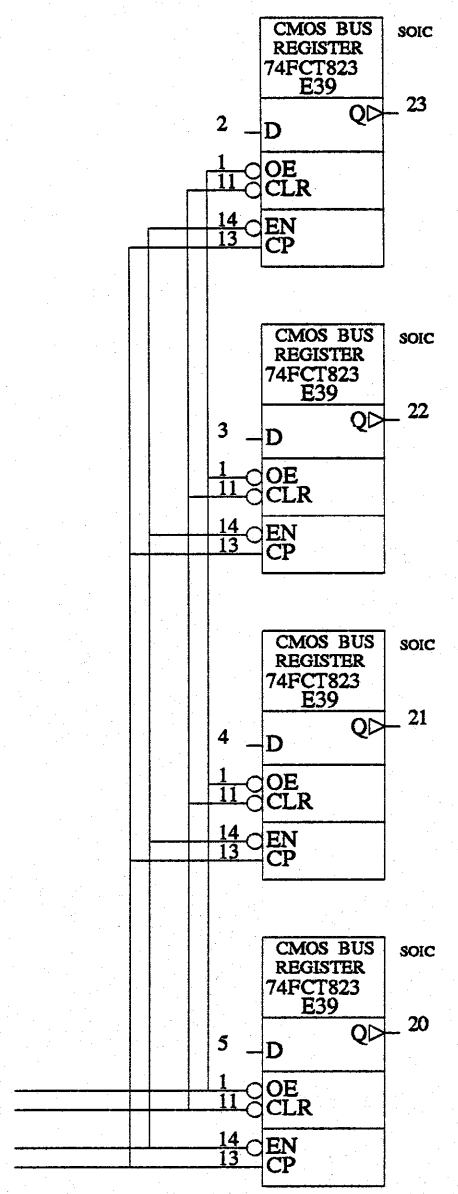
ENG: T. Nerger  
DATE: -  
BOARD LOCATION: CXO  
SHEET 38  
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88



BUS ERR REG CS L  
VCCR16 L

BUS ERR REG EN L  
BUS CLK A H



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REVISIONS		
CHK	CHANGE NO.	REV

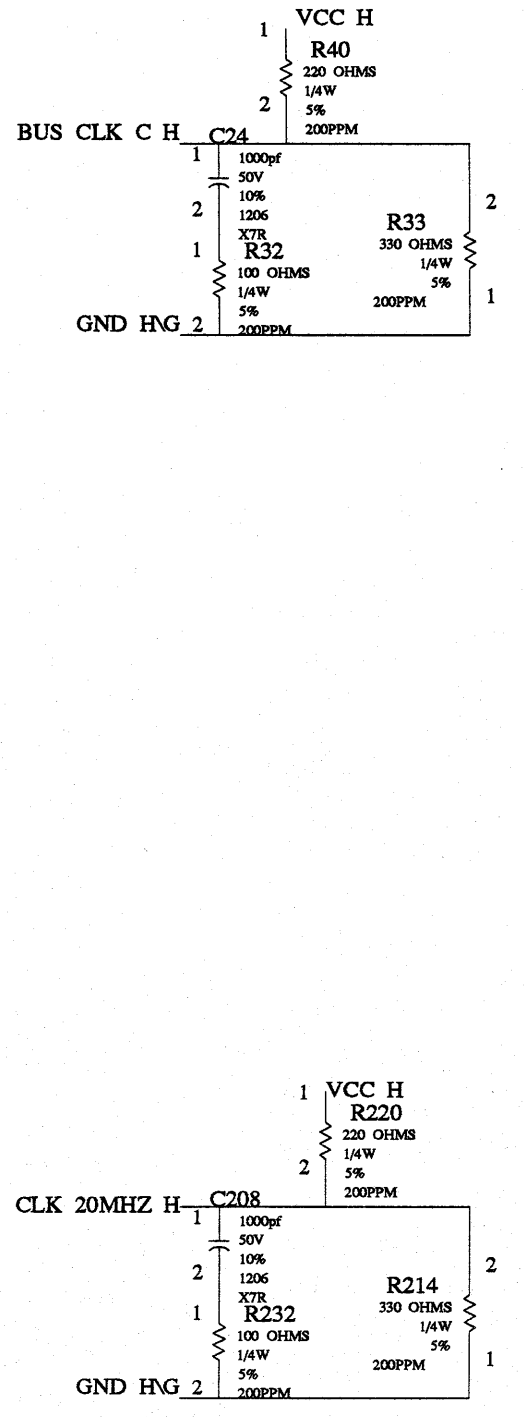
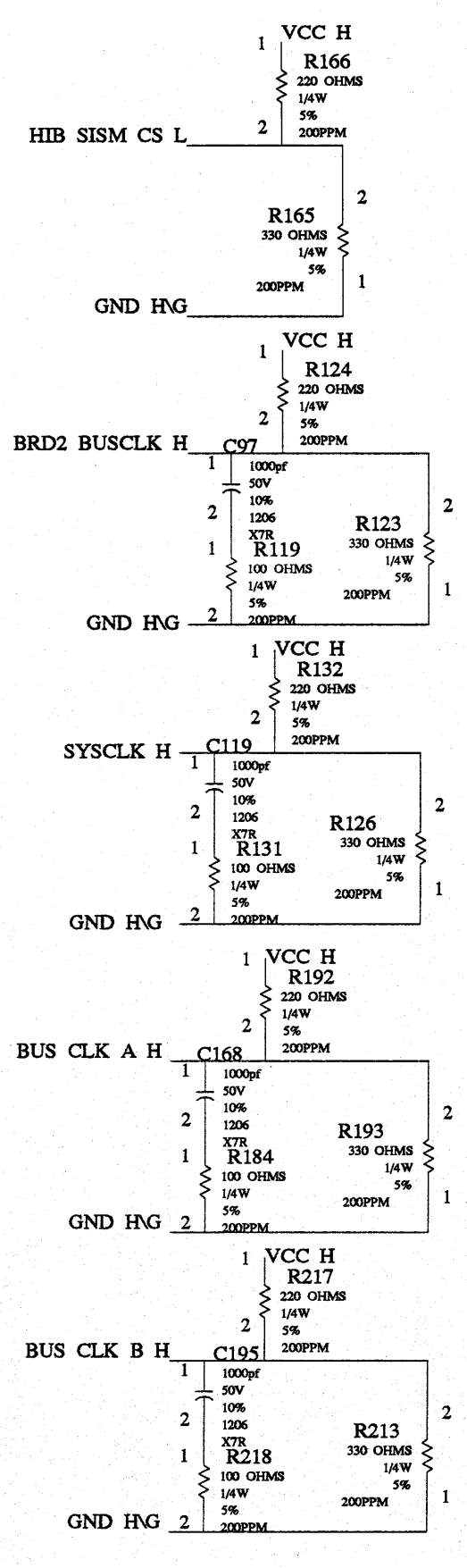
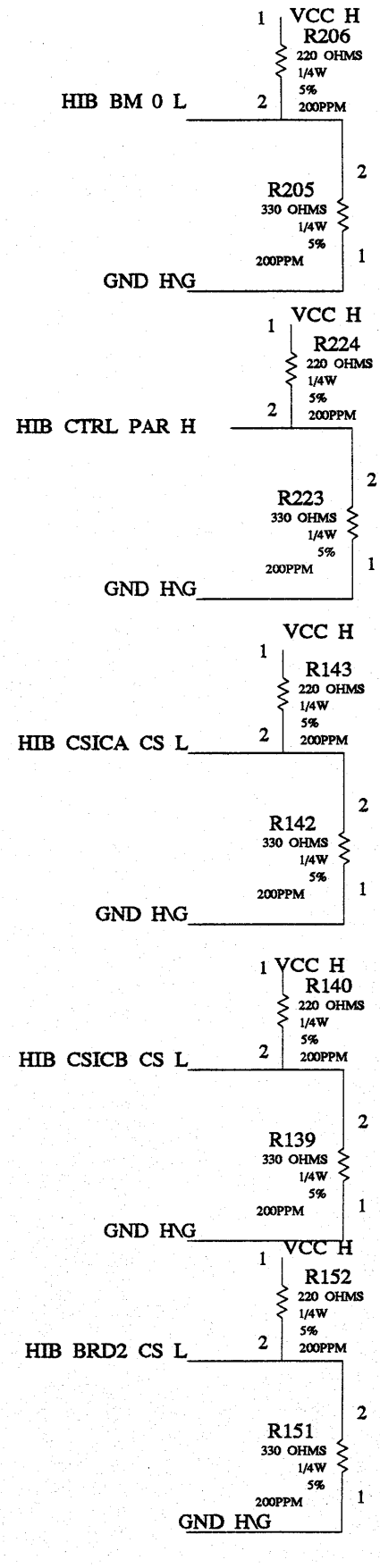
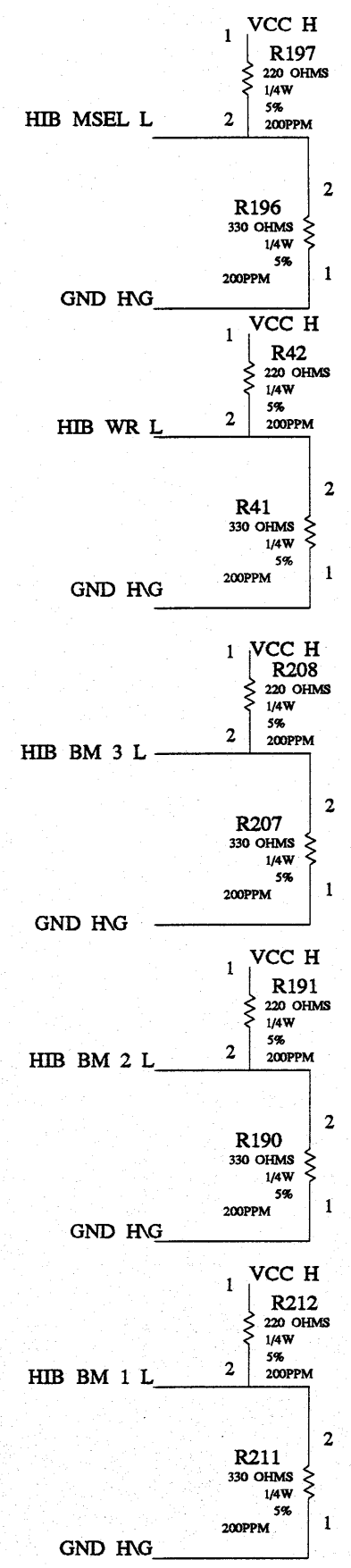
[Logic]  
**BLANK PAGE**

**digital**

FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D: -	DATE	BOARD LOCATION: CXO	SHEET 39	SIZE K
Mon Oct 17 16:00:32 1988		NEXT HIGHER ASSEMBLY:	NUMBER CXO62	REV 17OCT88

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**CONTROL TERMINATION**

**digital**

DRN: T. Nerger  
DATE: -  
ENG: T. Nerger  
DATE: -  
TITLE: WILDCAT BOARD 2

CHK'D: -  
DATE: -  
BOARD LOCATION: CXO  
SHEET: 40  
NEXT HIGHER ASSEMBLY: -

Mon Oct 17 16:01:10 1988

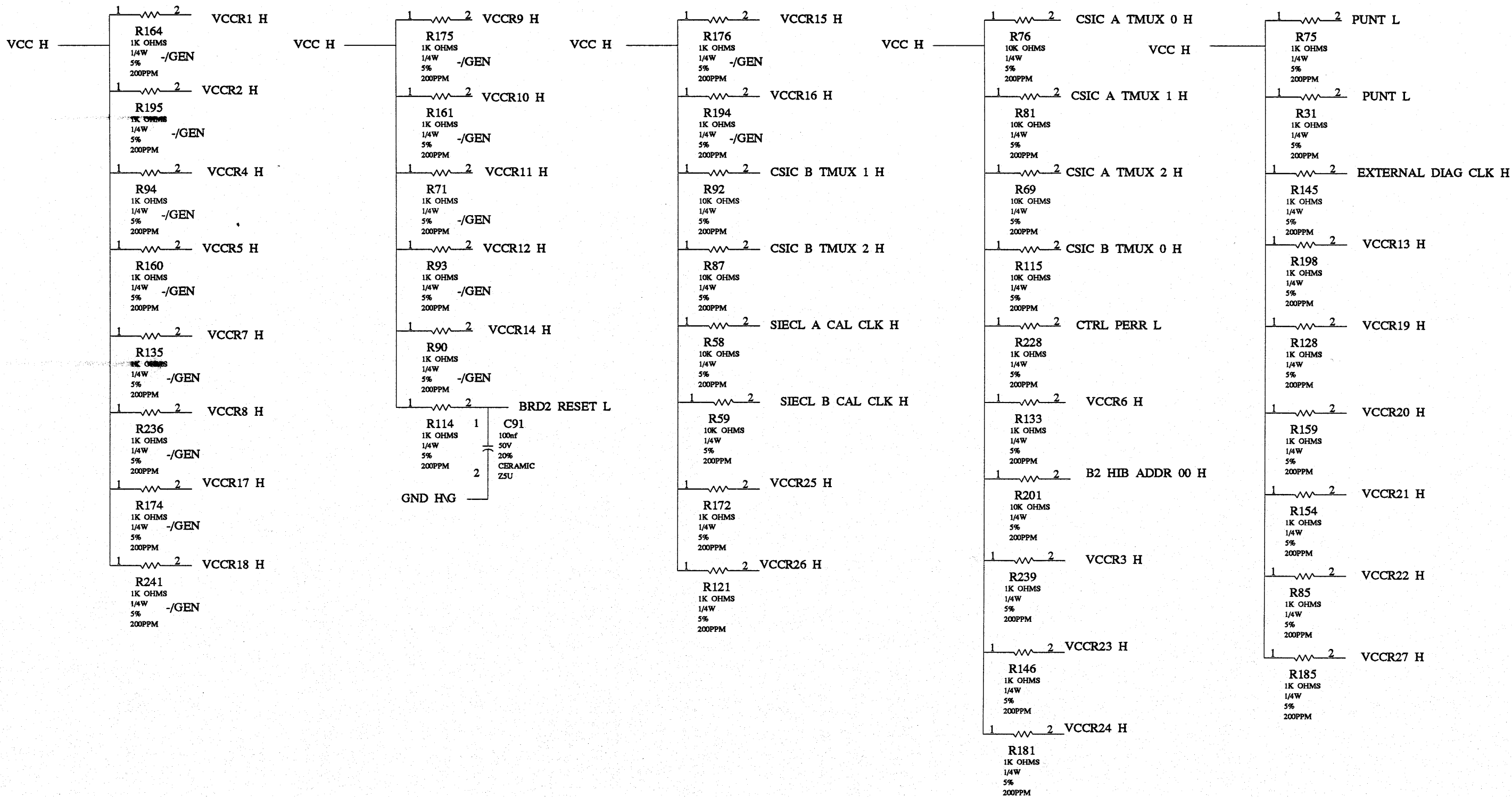
FIRST USED ON OPTION/MODEL: -

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88



# PULLUP RESISTORS

PULLUP RESISTANCE ON PUNT\_L = 500 OHMS

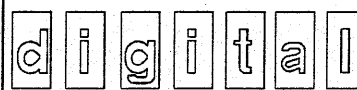


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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**PULLUP RESISTORS**



DRN: T. Nerger  
DATE: -  
CHK'D: -  
DATE: -  
Mon Oct 17 16:01:31 1988

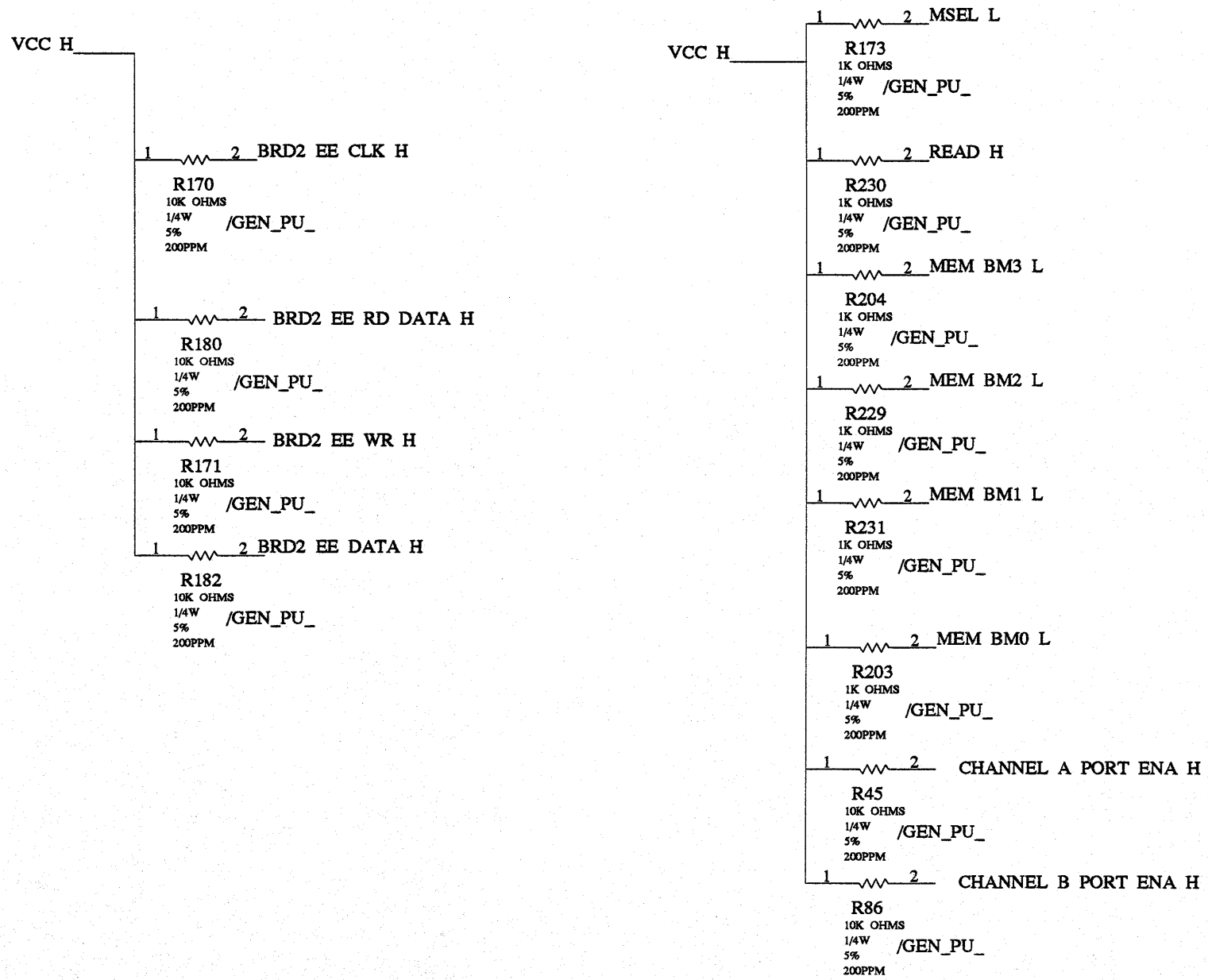
ENG: T. Nerger  
DATE: -  
BOARD LOCATION: CXO  
SHEET 41

NEXT HIGHER ASSEMBLY: -

TITLE: <b>WILDCAT BOARD 2</b>			
SIZE K	CODE CS	NUMBER CXO62	REV 170CT88

FIRST USED ON OPTION/MODEL: -

# PULLUP RESISTORS



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**PULLUP RESISTORS**



DRN: T. Nerger      DATE: -

CHK'D: -      DATE: -

Mon Oct 17 16:01:39 1988

FIRST USED ON OPTION/MODEL: -

ENG: T. Nerger      DATE: -

BOARD LOCATION: CXO

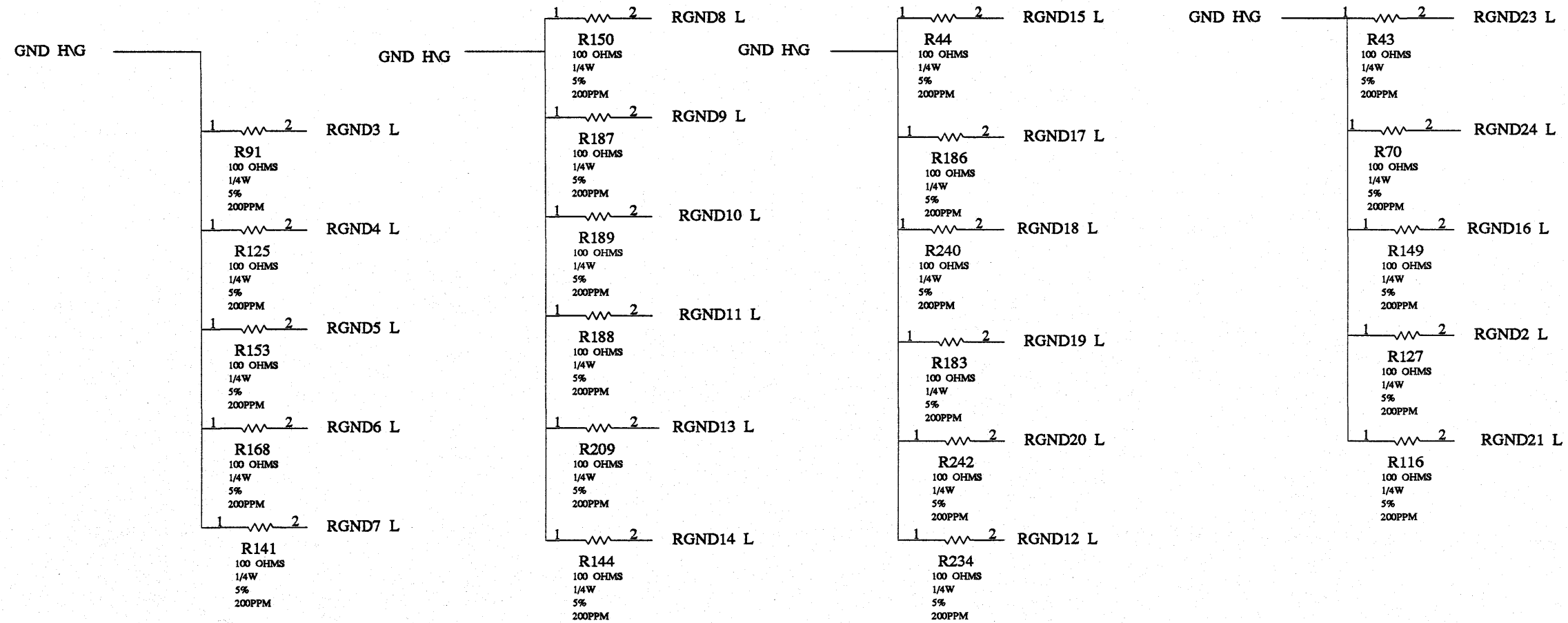
SHEET 42

NEXT HIGHER ASSEMBLY: -

TITLE:  
**WILDCAT BOARD 2**

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

# PULL DOWN RESISTORS



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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**PULLDOWN RESISTORS**



DRN: T. Nerger

DATE

ENG: T. Nerger

DATE

TITLE:  
**WILDCAT BOARD 2**

CHK'D:

DATE

BOARD LOCATION: CXO

SHEET 43

NEXT HIGHER ASSEMBLY:

SIZE	CODE	NUMBER	REV
K	CS	CXO62	17OCT88

FIRST USED ON OPTION/MODEL:

Mon Oct 17 16:01:47 1988



GND HNG  
VCC H

1   2 C219 100nf 50V 20% CERAMIC Z5U	1   2 C156 100nf 50V 20% CERAMIC Z5U	1   2 C112 100nf 50V 20% CERAMIC Z5U	1   2 C204 100nf 50V 20% CERAMIC Z5U	1   2 C224 100nf 50V 20% CERAMIC Z5U	1   2 C161 100nf 50V 20% CERAMIC Z5U
1   2 C201 100nf 50V 20% CERAMIC Z5U	1   2 C157 100nf 50V 20% CERAMIC Z5U	1   2 C113 100nf 50V 20% CERAMIC Z5U	1   2 C222 100nf 50V 20% CERAMIC Z5U	1   2 C223 100nf 50V 20% CERAMIC Z5U	1   2 C160 100nf 50V 20% CERAMIC Z5U
1   2 C185 100nf 50V 20% CERAMIC Z5U	1   2 C140 100nf 50V 20% CERAMIC Z5U	1   2 C127 100nf 50V 20% CERAMIC Z5U	1   2 C221 100nf 50V 20% CERAMIC Z5U	1   2 C205 100nf 50V 20% CERAMIC Z5U	1   2 C143 100nf 50V 20% CERAMIC Z5U
1   2 C220 100nf 50V 20% CERAMIC Z5U	1   2 C139 100nf 50V 20% CERAMIC Z5U	1   2 C126 100nf 50V 20% CERAMIC Z5U	1   2 C203 100nf 50V 20% CERAMIC Z5U	1   2 C206 100nf 50V 20% CERAMIC Z5U	1   2 C144 100nf 50V 20% CERAMIC Z5U
1   2 C202 100nf 50V 20% CERAMIC Z5U	1   2 C125 100nf 50V 20% CERAMIC Z5U	1   2 C141 100nf 50V 20% CERAMIC Z5U	1   2 C187 100nf 50V 20% CERAMIC Z5U	1   2 C190 100nf 50V 20% CERAMIC Z5U	1   2 C129 100nf 50V 20% CERAMIC Z5U
1   2 C186 100nf 50V 20% CERAMIC Z5U	1   2 C124 100nf 50V 20% CERAMIC Z5U	1   2 C142 100nf 50V 20% CERAMIC Z5U	1   2 C188 100nf 50V 20% CERAMIC Z5U	1   2 C189 100nf 50V 20% CERAMIC Z5U	1   2 C128 100nf 50V 20% CERAMIC Z5U
1   2 C171 100nf 50V 20% CERAMIC Z5U	1   2 C110 100nf 50V 20% CERAMIC Z5U	1   2 C159 100nf 50V 20% CERAMIC Z5U	1   2 C173 100nf 50V 20% CERAMIC Z5U	1   2 C174 100nf 50V 20% CERAMIC Z5U	1   2 C114 100nf 50V 20% CERAMIC Z5U
1   2 C170 100nf 50V 20% CERAMIC Z5U	1   2 C111 100nf 50V 20% CERAMIC Z5U	1   2 C158 100nf 50V 20% CERAMIC Z5U	1   2 C172 100nf 50V 20% CERAMIC Z5U	1   2 C175 100nf 50V 20% CERAMIC Z5U	1   2 C115 100nf 50V 20% CERAMIC Z5U

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REVISIONS		
CHK	CHANGE NO.	REV

[Logic]  
**DECOUPLING CAPACITORS**

**digital**

FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D: -	DATE	BOARD LOCATION: CXO	
	Mon Oct 17 16:03:00 1988	SHEET 45	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER CXO62	REV 17OCT88

File: 16L8BSL\_BBARB.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

Name BBARB;  
 Partno 16L8B;  
 Date 10-Aug-88;  
 Revision A5;  
 Designer LYLE;  
 Company DEC;  
 Assembly WILDCAT;  
 Location CXO;  
 Device P16L8;

```

/*****
*/
MISCELLANEOUS CONTROL PAL
/*****
*/
Allowable Target Device Types: 16L8B
/*****
*/
Used on Wildcat
/*****
*/
Revision A2: 28-Jun-1988;
add output enable conditions (TN)
/*****
*/
Revision A3: 1-Jul-1988; added 2nd address line for chip
selects (JL)
/*****
*/
Revision A4: 6-Jul-1988; corrected brd1_nxt_bus_grant_l/h
equations; inverted diag_clk_20mhz(TN)*/
/*****
*/
Revision A5: 10-Aug-1988; incorporate logic to support readable*/
diagnostic write registers. (TN)
/*****
*/

** Inputs **

Pin 15 = memcs_clk_h; /* used to qualify diag wr clk */
Pin 14 = read_h; /* output enable = 1 */
Pin 11 = b2_hib_addr_8_h; /* output enable = 1 */
Pin 9 = b2_hib_addr_9_h;
Pin 8 = diag_clk_en_h;
Pin 7 = clk_20mhz_h;
Pin 6 = oel;
Pin 5 = !bd2_reg_cs_l;
Pin 4 = !proc_nxt_grant_l;
Pin 3 = !xi_nxt_grant_l;
Pin 2 = !sic_a_nxt_bus_grant_l;
Pin 1 = !sic_b_nxt_bus_grant_l;

** Outputs **

Pin 18 = brd1_nxt_bus_grant_h;
Pin 17 = !bus_err_reg_cs_l;
Pin 16 = diag_wr_reg_clk_h; /* clock for diag write reg */
Pin 13 = !diag_reg_rd_en_l; /* time to read a diag reg */
Pin 19 = !diag_clk_20mhz_l;
Pin 12 = !hib_active_nxt_l;

** Declarations and Intermediate Variable Definitions **

** Logic Equations **

diag_clk_20mhz_l = diag_clk_en_h & clk_20mhz_h;

brd1_nxt_bus_grant_h = xi_nxt_grant_l # proc_nxt_grant_l;

bus_err_reg_cs_l = bd2_reg_cs_l & b2_hib_addr_8_h & b2_hib_addr_9_h;

diag_reg_rd_en_l = bd2_reg_cs_l & !b2_hib_addr_8_h & b2_hib_addr_9_h & read_h;

diag_wr_reg_clk_h = bd2_reg_cs_l & !b2_hib_addr_8_h & b2_hib_addr_9_h & !read_h
& memcs_clk_h;

hib_active_nxt_l = sic_a_nxt_bus_grant_l # sic_b_nxt_bus_grant_l
# xi_nxt_grant_l # proc_nxt_grant_l;

brd1_nxt_bus_grant_h.oe = oel;
bus_err_reg_cs_l.oe = oel;
diag_wr_reg_clk_h.oe = oel;
diag_reg_rd_en_l.oe = oel;
diag_clk_20mhz_l.oe = oel;
hib_active_nxt_l.oe = oel;

```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16L8BSL\_BBARB.PLD**

**digital**

FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE -	ENG: T. Nerger	DATE -
CHK'D: T. Nerger	DATE -	BOARD LOCATION: CXO	SHEET 50
Tue Oct 25 16:43:21 1988		NEXT HIGHER ASSEMBLY: -	

TITLE: WC BRD2			
SIZE K	CODE CS	NUMBER -	REV 25OCT88

REV NUMBER SIZE CODE CS B

File: 16L8BSL\_MEMCS.PLD  
 Source: DISK\$HSBSIM\_B-[SIMULATION.CMS]

Name MEMCS;  
 Partno 16L8B;  
 Date 06/08/88;  
 Revision A3;  
 Designer LYLE;  
 Company DEC;  
 Assembly T1005;  
 Location XXXXX;  
 Device P16L8;

```

  /*****
  /*
  /* MEMORY CONTROL PAL CHIP SELECT - 16L8B */
  /*
  /*
  /* Allowable Target Device Types: */
  *****/
  
```

```

  /** Inputs **
  |
  Pin 11 = !mem_bm0_l; /* */
  Pin 9 = !mem_bm1_l; /* */
  Pin 8 = !mem_bm2_l; /* */
  Pin 7 = !mem_bm3_l; /* */
  Pin 6 = !msel_l; /* */
  Pin 5 = read_h; /* */
  Pin 4 = b2_hib_addr_17_h; /* address bit used in cs decode */
  Pin 3 = b2_hib_addr_16_h; /* */
  Pin 2 = !hib_active_l; /* legitimate bus cycle = 0 */
  Pin 1 = !memcs_clk_h; /* */
  
```

```

  /** Outputs **
  |
  Pin 18 = !mem0_palcs0_l; /* */
  Pin 17 = !mem0_palcs1_l; /* */
  Pin 16 = !mem0_palcs2_l; /* */
  Pin 15 = !mem0_palcs3_l; /* */
  Pin 14 = !mem1_palcs0_l; /* */
  Pin 13 = !mem1_palcs1_l; /* */
  Pin 19 = !mem1_palcs2_l; /* */
  Pin 12 = !mem1_palcs3_l; /* */
  
```

/\*\* Declarations and Intermediate Variable Definitions \*\*/

/\*\* Logic Equations \*\*/

```

mem0_palcs0_l = hib_active_l & mem_bm0_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem0_palcs1_l = hib_active_l & mem_bm1_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem0_palcs2_l = hib_active_l & mem_bm2_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem0_palcs3_l = hib_active_l & mem_bm3_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem1_palcs0_l = hib_active_l & mem_bm0_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem1_palcs1_l = hib_active_l & mem_bm1_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

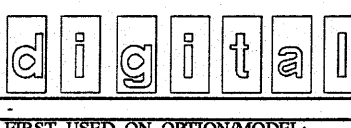
mem1_palcs2_l = hib_active_l & mem_bm2_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);

mem1_palcs3_l = hib_active_l & mem_bm3_l & msel_l &
((read_h) # (!read_h & memcs_clk_h))
&(b2_hib_addr_16_h & b2_hib_addr_17_h);
  
```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16L8BSL\_MEMCS.PLD**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WC BRD2
CHK'D: T. Nerger	DATE	BOARD LOCATION: CXO	SHEET 51	
FIRST USED ON OPTION/MODEL: Tue Oct 25 16:43:29 1988				NEXT HIGHER ASSEMBLY:

SIZE K	CODE CS	NUMBER	REV 25OCT88
--------	---------	--------	-------------

File: 16L8BSL\_MISC2.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

16L8BSL\_MISC2.PLD continued..

```
Name      MISC2;
Partno    16L8B;
Date      14-Sep-1988;
Revision  C;
Designer  Nerger;
Company   DEC;
Assembly  CXO62;
Location  XXXXX;
Device    P16L8;
```

```
brd2_ce_rd_data_h.oe = ce_rd_data_oe_h;
ce_rd_data_oe_h      = (diag2_wr_bit11_h & ce_wr_diag24_h & oe)
                      # (diag2_wr_bit11_h & brd2_ce_wr_h & oe);
|
brd2_ce_clk_h        = diag2_wr_bit11_h & ceclk_diag26_h;
brd2_ce_clk_h.oe     = diag2_wr_bit11_h & oe;
|
chan_a_port_ena_h.oe = oe;
chan_b_port_ena_h.oe = oe;
```

```
/* *****
/* MISCELLANEOUS CONTROL PAL */
/* *****
/* Allowable Target Device Types: 16L8B */
/* *****
/* Used on Wildcat */
/* *****
/* Revision A2: 22-Jun-1987 */
/* Revision A3: 29-Jun-1988;
/* add output enable conditions (TN) */
/* Revision A4: 18-Aug-1988; update input 2 to diag_wr_reg_clk_h;
/* necessary due to change to 74ALS666 diagnostic write
/* registers. (TN) */
/* *****
/* Revision B: 8-Sep-1988; remove siecl calibration shift register;
/* clock logic; old scheme wouldn't work with the transparent;
/* board 2 diagnostic registers; this logic moved to PCAPT;
/* (TN) */
/* *****
/* Revision C: 14-Sep-1988; switch to board 2 diagnostic register;
/* control of serial EEPROM */
/* *****
```

```
/* This PAL will support serial EEPROM access from either board 1;
/* diagnostic registers or board 2 diagnostic registers. In order;
/* to use board 2 diagnostic registers for control, diag2_wr_bit11_h;
/* must be set to a 1. This means that the default control is;
/* board 1 control because this bit is a 0 on reset.
/* *****
```

```
/* Inputs */
|
Pin 18 = nc18; /*
Pin 17 = nc17; /*
Pin 15 = diag2_wr_bit11_h; /* select EEPROM write from brd2 */
Pin 11 = channel_a_port_ena_h; /* csic a port enable to siecl */
Pin 9 = !sic_a_reset_l; /*
Pin 8 = channel_b_port_ena_h; /* csic b port enable to siecl */
Pin 7 = !sic_b_reset_l; /*
Pin 6 = ceclk_diag26_h; /* from diagnostic write */
Pin 5 = ce_wr_diag24_h; /*
Pin 4 = ce_data_diag25_h; /*
Pin 3 = brd2_ce_wr_h; /* set write mode from board 1 */
Pin 2 = brd2_ce_data_h; /* data to write to EEPROM */
Pin 1 = !oe; /*
```

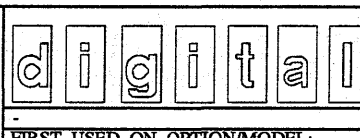
```
/* Outputs */
|
Pin 16 = ce_rd_data_oe_h; /* need OR for output enable, so;
/* use this unused input for the;
/* OR and wrap it back around. */
|
Pin 14 = brd2_ce_clk_h; /*
Pin 13 = brd2_ce_rd_data_h; /* need bidirectionality */
Pin 19 = chan_a_port_ena_h; /* port enable to siecl */
Pin 12 = chan_b_port_ena_h; /* port enable to siecl */
|
```

```
/* Logic Equations */
|
chan_a_port_ena_h = !sic_a_reset_l
                  & channel_a_port_ena_h;
|
chan_b_port_ena_h = !sic_b_reset_l
                  & channel_b_port_ena_h;
|
brd2_ce_rd_data_h = (diag2_wr_bit11_h & ce_data_diag25_h)
                  # (!diag2_wr_bit11_h & brd2_ce_data_h);
```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16L8BSL\_MISC2.PLD**



DRN:	T. Nerger	DATE	ENG:	T. Nerger	DATE	TITLE:	WC BRD2
CHK'D:	T. Nerger	DATE	BOARD LOCATION:	CXO	SHEET	52	
FIRST USED ON OPTION/MODEL:			NEXT HIGHER ASSEMBLY:		SIZE	CODE	NUMBER
Tue Oct 25 16:43:36 1988					K	CS	-

SIZE	CODE	NUMBER	REV
K	CS	-	25OCT88



File: 16L8BSL\_PARC2.PLD  
 Source: DISK\$HSBSIM\_B-[SIMULATION.CMS]

Name PARC2;  
 Partno 16L8B;  
 Date 6-Jun-1988;  
 Revision A2;  
 Designer Nerger;  
 Company DEC;  
 Assembly CXO36;  
 Location XXXXX;  
 Device P16L8;

```

/*****
/*      PARITY CONTROL PAL - 16L8B rev 1      */
/*      used on HOB and HSB50 PASS 3          */
/*****
/* Allowable Target Device Types: 16L8B      */
/*****

```

```

/** Inputs **/
Pin 17 = bus_err_reg_cs_l; /*
Pin 16 = dreg_cs_l; /*
Pin 15 = reg_cs_l; /*
Pin 11 = lcsic_b_reg_cs_l; /* csic b registered chip select */
Pin 9 = lcsic_a_reg_cs_l; /* csic a registered chip select */
Pin 8 = lmem_bm3_l; /* memory byte masks (0=perform */
Pin 7 = lmem_bm2_l; /* operation)*/
Pin 6 = lmem_bm1_l; /*
Pin 5 = lmem_bm0_l; /*
Pin 4 = lmem_l; /* memory select = 0 */
Pin 3 = hib_active_l; /* legitimate hib cycle = 0 */
Pin 2 = brd1_grant_h; /*
Pin 1 = read_h; /*
Pin 18 = output_enable; /*

```

```

/** Outputs **/
Pin 14 = lparity_xmit3_l; /* 74AS286 xmit pins */
Pin 13 = lparity_xmit2_l; /*
Pin 19 = lparity_xmit1_l; /*
Pin 12 = lparity_xmit0_l; /*

```

/\*\* Declarations and Intermediate Variable Definitions \*\*/

```

/** Logic Equations **/
parity_xmit0_l = hib_active_l &
(lmem_bm0_l #
(mem_bm0_l & read_h & !msel_l & brd1_grant_h) #
(mem_bm0_l & !read_h & msel_l & !brd1_grant_h));
parity_xmit1_l = hib_active_l &
(lmem_bm1_l #
(mem_bm1_l & read_h & !msel_l & brd1_grant_h) #
(mem_bm1_l & !read_h & msel_l & !brd1_grant_h));
parity_xmit2_l = hib_active_l &
(lmem_bm2_l #
(mem_bm2_l & read_h & !msel_l & brd1_grant_h) #
(mem_bm2_l & !read_h & msel_l & !brd1_grant_h));
parity_xmit3_l = hib_active_l &
(lmem_bm3_l #
(mem_bm3_l & read_h & !msel_l & brd1_grant_h) #
(mem_bm3_l & !read_h & msel_l & !brd1_grant_h));

```

```

parity_xmit3_loe = output_enable;
parity_xmit2_loe = output_enable;
parity_xmit1_loe = output_enable;
parity_xmit0_loe = output_enable;

```

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CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
 16L8BSL\_PARC2.PLD



DRN:	T. Nerger	DATE	-	ENG:	T. Nerger	DATE	-	TITLE:	WC BRD2
CHK'D:	T. Nerger	DATE	-	BOARD LOCATION:	CXO	SHEET	53	SIZE	K
FIRST USED ON OPTION/MODEL:				NEXT HIGHER ASSEMBLY:		NUMBER	-	REV	25OCT88

REV .  
 NUMBER .  
 CS  
 K  
 B

File: 16L8BSL\_SISC1.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

16L8BSL\_SISC1.PLD continued..

name SISC1;  
 Partno XXXXX;  
 Revision A1;  
 Date 08/28/86;  
 Designer NERGER/LYLE;  
 Company DEC;  
 Assembly WILD CAT;  
 Location XXXXX;  
 Device P16L8;

```

*****
/*          SISM Control PAL          */
*****
/* Allowable Target Device Types: 16L8 */
*****
  
```

```

/** Inputs **/
Pin 11 = !sic_reset_l      /* */
Pin 9  = sism_en_h        /* */
Pin 8  = sism_bus_err_h   /* */
Pin 7  = sism_crom_test_h /* */
Pin 6  = reg_sism_parity_err_h /* */
Pin 5  = sismcode_wr_rd_en_h /* */
Pin 4  = !sism_rd_en_l    /* */
Pin 3  = !sism_reg_cs_l   /* */
Pin 2  = b2_hib_addr_l1_h /* */
Pin 1  = !mem_we_l       /* */
  
```

```

/** Outputs **/
Pin 18 = !sism_cntr_clr_l /* */
Pin 17 = !sism_cntr_ld_l  /* */
Pin 16 = !sism_perr_fdbck1_l /* */
Pin 15 = sism_cntr_en_h   /* eqns written for NO CLEAR */
Pin 14 = !trans_hi_en_l  /* */
Pin 13 = !trans_lo_en_l  /* */
Pin 19 = !sism_ram_wr_en_hi_l /* eqns written for NO CLEAR */
Pin 12 = !sism_ram_wr_en_lo_l /* */
  
```

/\*\* Declarations and Intermediate Variable Definitions \*\*/

```

/** Logic Equations **/

/* written for NO CLEAR */
sism_cntr_clr_l = ! sic_reset_l
                  & sism_en_h ;

/* normal SISM run mode = load active */
sism_cntr_ld_l = ! sic_reset_l
                 & sism_en_h
                 & ! sism_crom_test_h
                 & ! sism_bus_err_h
                 & ! reg_sism_parity_err_h
                 & ! sismcode_wr_rd_en_h ;

/* enable count for SISM CROM test */
sism_cntr_en_h =
( sism_crom_test_h
  & ! sism_bus_err_h
  & ! reg_sism_parity_err_h & !sismcode_wr_rd_en_h ) #
( sismcode_wr_rd_en_h & sism_reg_cs_l ) ;

/* latch and hold parity error */
sism_perr_fdbck1_l = ! sic_reset_l
                    & sism_en_h
                    & (reg_sism_parity_err_h # sism_bus_err_h);

sism_ram_wr_en_lo_l = sism_en_h & !sic_reset_l
                     & !sism_rd_en_l
                     & !b2_hib_addr_l1_h
                     & sismcode_wr_rd_en_h
                     & mem_we_l
  
```

```

& sism_reg_cs_l;

!
sism_ram_wr_en_hi_l = sism_en_h & !sic_reset_l
                     & !sism_rd_en_l
                     & b2_hib_addr_l1_h
                     & sismcode_wr_rd_en_h
                     & mem_we_l
                     & sism_reg_cs_l;

!
trans_lo_en_l = sism_en_h & !sic_reset_l
               & sism_reg_cs_l
               & !b2_hib_addr_l1_h
               & sismcode_wr_rd_en_h;

!
trans_hi_en_l = sism_en_h & !sic_reset_l
               & sism_reg_cs_l
               & b2_hib_addr_l1_h
               & sismcode_wr_rd_en_h;

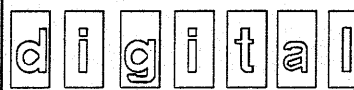
!
  
```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16L8BSL\_SISC1.PLD**



DRN:	T. Neger	DATE	-	ENG:	T. Neger	DATE	-	TITLE:	WC BRD2
CHK'D:	T. Neger	DATE	-	BOARD LOCATION:	CSXO	SHEET	54	SIZE	K
FIRST USED ON OPTION/MODEL:		Tue Oct 25 16:43:50 1988		NEXT HIGHER ASSEMBLY:		-		CODE	CS
-		-		-		-		NUMBER	-
-		-		-		-		REV	25OCT88

REV .  
 NUMBER .  
 CODE CS  
 K  
 B

File: 16L8BSL\_CXCVR.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

Name CXCVR;  
 Partno XXXXXX;  
 Date 11-Aug-1988;  
 Revision A;  
 Designer Nerger;  
 Company DEC;  
 Assembly WILDACAT;  
 Location CXO;  
 Device P16L8;

```

*****
/*          SISM TRANSCEIVER CONTROL PAL 16L8B          */
*****
/* Allowable Target Device Types: 16L8                  */
*****
/* Used on Wildcat                                     */
*****
/* Revision A: copied from 16L8BSL_SXCVR                */
*****
  
```

```

** Inputs **
Pin 1 = !csic_b_addr_reg_en_l; /*
Pin 2 = !sic_a_bus_grant_l; /*
Pin 3 = !sic_b_bus_grant_l; /*
Pin 4 = !csic_a_cs_l; /*
Pin 5 = !csic_b_cs_l; /*
Pin 6 = !we_l; /*
Pin 7 = !hib_active_l; /*
Pin 8 = !read_h; /*
Pin 9 = !xcvr_clk_h; /*
Pin 11 = !csic_a_addr_reg_en_l; /*
  
```

```

** Outputs **
Pin 12 = !csic_a_lo_dal_en_l; /*
Pin 19 = !csic_a_lo_dal_dir_h; /* 1 = CSIC -> HIB
Pin 13 = !csic_a_hi_dal_en_l; /*
Pin 14 = !csic_a_hi_dal_dir_h; /* 1 = CSIC -> HIB
Pin 15 = !csic_b_lo_dal_en_l; /*
Pin 16 = !csic_b_lo_dal_dir_h; /* 1 = CSIC -> HIB
Pin 17 = !csic_b_hi_dal_en_l; /*
Pin 18 = !csic_b_hi_dal_dir_h; /* 1 = CSIC -> HIB
  
```

```

** Declarations and Intermediate Variable Definitions **
sic_a_read = read_h & sic_a_bus_grant_l;
sic_a_write = !read_h & sic_a_bus_grant_l;
uvax_a_read = read_h & csic_a_cs_l;
uvax_a_write = !read_h & csic_a_cs_l;

sic_b_read = read_h & sic_b_bus_grant_l;
sic_b_write = !read_h & sic_b_bus_grant_l;
uvax_b_read = read_h & csic_b_cs_l;
uvax_b_write = !read_h & csic_b_cs_l;
  
```

```

** Logic Equations **
/* transceiver default direction is toward */
!csic_a_lo_dal_dir_h = sic_a_read # uvax_a_write # sic_b_read;
csic_a_lo_dal_en_l = (xcvr_clk_h
  & (sic_a_read # uvax_a_write # sic_b_read))
  # (sic_a_write # uvax_a_read);

!csic_a_hi_dal_dir_h = !csic_a_addr_reg_en_l & sic_a_read;
csic_a_hi_dal_en_l = (xcvr_clk_h & !csic_a_addr_reg_en_l & sic_a_read)
  # sic_a_write;

!csic_b_lo_dal_dir_h = sic_b_read # uvax_b_write # sic_a_read;
csic_b_lo_dal_en_l = (xcvr_clk_h
  & (sic_b_read # uvax_b_write # sic_a_read))
  # (sic_b_write # uvax_b_read);
  
```

16L8BSL\_CXCVR.PLD continued..

```

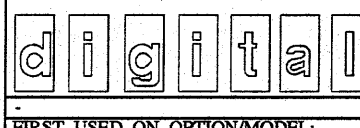
!csic_b_hi_dal_dir_h = !csic_b_addr_reg_en_l & sic_b_read;
csic_b_hi_dal_en_l = (xcvr_clk_h & !csic_b_addr_reg_en_l & sic_b_read)
  # sic_b_write;

csic_a_lo_dal_dir_h.oe = oe_l;
csic_a_lo_dal_en_loe = oe_l;
csic_a_hi_dal_dir_h.oe = oe_l;
csic_a_hi_dal_en_loe = oe_l;
csic_b_lo_dal_dir_h.oe = oe_l;
csic_b_lo_dal_en_loe = oe_l;
csic_b_hi_dal_dir_h.oe = oe_l;
csic_b_hi_dal_en_loe = oe_l;
  
```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16L8BSL\_CXCVR.PLD**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WC BRD2
CHK'D: T. Nerger	DATE	BOARD LOCATION: CXO	SHEET 55	SIZE K
FIRST USED ON OPTION/MODEL: Tue Oct 25 16:43:57 1988		NEXT HIGHER ASSEMBLY:	NUMBER	REV 25OCT88

File: 16R4BSL\_BUSCO.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

Name BUSCO;  
 Partno XXXXX;  
 Date 24-Oct-1988;  
 Revision C;  
 Designer NERGER;  
 Company DEC;  
 Assembly HSB2;  
 Location XXXXX;  
 Device P16R4;

```

  /******
  /*          SISM BUS CONTROL PAL          */
  /******
  /* Allowable Target Device Types: 16R4          */
  /******
  /* Used on HOB, HSB50 BD2, Wildcat          */
  /******
  /* Revision A2: 12-Mar-1987          */
  /******
  /* Revision A3: 29-Jun-1988;          */
  /* add output enable conditions for pins 12,13,18,19 (TN)*/
  /******
  /* Revision B: 23-Sep-1988: change sism_x_crom_test_h to          */
  /* sism_x_cram_test_h; add sism_x_cram_test_h as a          */
  /* qualifier to all outputs (this is needed when the          */
  /* sism's are being loaded or tested, i.e., a non-          */
  /* operational mode). TEN          */
  /******
  /* Revision C: 24-Oct-1988: change sic_x_opcode_req_l to          */
  /* opcode_x_req_l to resolve opcode validate race          */
  /* condition; remove output enable conditions for pins          */
  /* 12,13,18,19 (TEN)          */
  /******
  
```

```

  /** Inputs **/
  Pin 1 = bus_clk_a_h;          /*
  Pin 2 = !sic_x_bus_grant_l;    /*
  Pin 3 = !sic_x_next_bus_grant_l; /*
  Pin 4 = !sic_x_bus_req_in_l;   /*
  Pin 5 = !opcode_x_req_l;      /* was sic_x_opcode_req_l
  Pin 6 = sism_x_cram_test_h;    /*
  Pin 7 = !pre_rem_tmux_x_en_l;  /*
  Pin 8 = !sism_x_ctr_clr_l;     /*
  Pin 9 = !opcode_status_a_l;    /*
  Pin 11 = loc;                 /* output enable
  
```

```

  /** Outputs **/
  Pin 12 = !remote_tmux_x_en_l;  /*
  Pin 13 = !opcode_validate_l;   /*
  Pin 14 = bus_request_pending_x; /* registered
  Pin 15 = op_val_pending_x;     /* registered
  Pin 16 = addr_latch_delayed_x; /* registered
  Pin 17 = !opcode_x_req_reg_l;  /* registered
  Pin 18 = !sic_x_addr_reg_en_l; /*
  Pin 19 = !sic_x_bus_req_l;     /*
  
```

```

  /** Declarations and Intermediate Variable Definitions **/

  /** Logic Equations **/
  bus_request_pending_x.d = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & ((sic_x_bus_req_in_l & !sic_x_next_bus_grant_l)
    # (bus_request_pending_x & !sic_x_next_bus_grant_l));

  op_val_pending_x.d = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & (opcode_x_req_reg_l
    # (op_val_pending_x & !sic_x_bus_grant_l));

  addr_latch_delayed_x.d = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & sic_x_bus_req_in_l
    & sic_x_bus_grant_l;

  opcode_x_req_reg_l.d = opcode_x_req_l;
  
```

16R4BSL\_BUSCO.PLD continued..

```

  opcode_validate_l = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & ((opcode_x_req_reg_l & !sic_x_next_bus_grant_l)
    # (op_val_pending_x & !sic_x_next_bus_grant_l))
    # opcode_status_a_l;

  sic_x_bus_req_l = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & (sic_x_bus_req_in_l
    # bus_request_pending_x);

  csic_x_addr_reg_en_l = !sism_x_ctr_clr_l & !sism_x_cram_test_h
    & ((sic_x_bus_req_in_l & !sic_x_bus_grant_l)
    # addr_latch_delayed_x);

  remote_tmux_x_en_l = pre_rem_tmux_x_en_l & !sism_x_cram_test_h;
  
```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16R4BSL\_BUSCO.PLD**

**digital**  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE -	ENG: T. Nerger	DATE -	TITLE: WC BRD2
CHK'D: T. Nerger	DATE -	BOARD LOCATION: CXO	SHEET 56	
Tue Oct 25 16:44:04 1988				NEXT HIGHER ASSEMBLY:

SIZE K	CODE CS	NUMBER -	REV 25OCT88
--------	---------	----------	-------------

File: 16R4BSL\_HIBR2.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

16R4BSL\_HIBR2.PLD continued..

Name HIBR2;  
 Partno xxxx;  
 Date 14-Oct-1988;  
 Revision B;  
 Designer Nerger;  
 Company DEC;  
 Assembly CXO39;  
 Location XXXXX;  
 Device P16R4;

```

/* output will feed the error register*/
addr_perr_l = brd1_grant_l & (hib_addr_pl_err_l # hib_addr_ph_err_l);

/* The following illegal condition will tristate the output of
/* pins 18 and 19; implemented for test considerations. */
addr_perr_loe = oe2;
bus_err_reg_en_loe = oe2;

```

```

/******
/*
/* HIB BUS ERROR CONTROL PAL - 16R4B */
/******
/* Used on HOB, HSB50 BD2 rev C (pass 3), Wildcat */
/******
/* Allowable Target Device Types: 16R4B */
/******
/* Revision A2: 28-Jun-1988;
/* add output enable conditions for pins 18 and 19 */
/******
/* Revision B: 14-Oct-1988; add BRD1 GRANT L as a qualifier for */
/* address parity errors. (TEN) */
/******

```

```

/** Inputs **/
Pin 13 = !sic_a_post_bus_grant_l; /*
Pin 12 = !sic_b_post_bus_grant_l; /*
Pin 2 = !brd1_grant_l; /*
Pin 3 = !clr_perr_l; /*
Pin 4 = !data_perr_dlyd_l; /*
Pin 5 = oe2; /* output enable = 1
Pin 6 = !hib_active_l; /*
Pin 7 = !ctrl_perr_l; /*
Pin 8 = !hib_addr_ph_err_l; /*
Pin 9 = !hib_addr_pl_err_l; /*
Pin 11 = loe; /* output enable

```

```

/** Outputs **/
Pin 17 = latch_bit; /*
Pin 16 = !hib_bus_err_l; /*
Pin 15 = !sism_a_bus_err_h; /*
Pin 14 = !sism_b_bus_err_h; /*
Pin 19 = !addr_perr_l; /*
Pin 18 = bus_err_reg_en_l; /* written for the NOT ENABLED state */

```

```

/** Declarations and Intermediate Variable Definitions **/
address_error = brd1_grant_l & (hib_addr_pl_err_l # hib_addr_ph_err_l);
control_error = brd1_grant_l & ctrl_perr_l;

```

```

/** Logic Equations **/
latch_bit.d = !clr_perr_l & (
    latch_bit
    # control_error
    # address_error
    # data_perr_dlyd_l);

hib_bus_err_l.d = !latch_bit & !clr_perr_l & ( /* one-time pulse */
    control_error
    # address_error
    # data_perr_dlyd_l);

```

```

/* written for the NOT ENABLED state, i.e., = 1 */
/* This signal changing to a 1 will freeze the bus error register. */
/* Control/address errors are reported in the actual bus cycle. */
/* Data errors are reported one cycle later. */

```

```

bus_err_reg_en_l = !clr_perr_l & ( latch_bit # data_perr_dlyd_l);

```

```

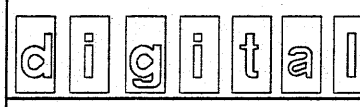
/* these signals will stop the SISM's */
sism_a_bus_err_h.d = !clr_perr_l & !sic_a_post_bus_grant_l & data_perr_dlyd_l;
sism_b_bus_err_h.d = !clr_perr_l & !sic_b_post_bus_grant_l & data_perr_dlyd_l;

```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
**16R4BSL\_HIBR2.PLD**



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WC BRD2
CHK'D: T. Nerger	DATE	BOARD LOCATION: CXO	SHEET 57	SIZE K
FIRST USED ON OPTION/MODEL: Tue Oct 25 16:44:12 1988		NEXT HIGHER ASSEMBLY:		CODE CS
			NUMBER	REV 25OCT88

REV NUMBER CS K B

File: 16R4BSL\_PCAPT.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

Name PCAPT;  
 Partno 16R4B;  
 Date 25-Oct-1988;  
 Revision D;  
 Designer Nerger;  
 Company DEC;  
 Assembly CXO62;  
 Location XXXXX;  
 Device P16R4;

```

/*****
/*
/* PARITY CAPTURE PAL - 16R4B */
/*
/*
/*****
/* Allowable Target Device Types: 16R4B */
/*****
/* Used on HOB, HSBS0 BD2 rev C (pass 3), Wildcat */
/*****
/* Revision A3: 29-Jun-1988; */
/* add output enable conditions for pins 18,19 (TN) */
/*****
/* Rev B: 8-sep-1988; remove siecl cal clock test logic and add */
/* siecl shift register logic (TN) */
/*****
/* Rev C: 5-Oct-1988; define the polarity of brd2_reset_1 as */
/* LOW (previously defined active HIGH, a mistake) TEN */
/*****
/* Rev D: 25-Oct-1988; create HIB FEC REG H by registering HIB */
/* FEC H (TN) */
/*****

```

```

/** Inputs **/
Pin 13 = siecl_b_sh_reg_clk_en_h; /*
Pin 12 = siecl_a_sh_reg_clk_en_h; /*from bd2 diagnostic register */
Pin 2 = diag_wr_reg_clk_h; /*
Pin 3 = lbrd2_reset_l; /*
Pin 4 = lhib_data3_perr_l; /*
Pin 5 = lhib_data2_perr_l; /*
Pin 6 = lhib_data1_perr_l; /*
Pin 7 = lhib_data0_perr_l; /*
Pin 8 = hib_fec_h; /*
Pin 9 = lhib_active_l; /*

/** Outputs **/
Pin 19 = siecl_b_shift_reg_clk_h; /*
Pin 18 = siecl_a_shift_reg_clk_h; /*
Pin 17 = ldata_perr_dlyd_l; /* sent to HIBER PAL
Pin 16 = hib_fec_reg_h; /* registered version of hib_fec_h*/
Pin 15 = reg_siecl_b_clk_en_h; /*
Pin 14 = reg_siecl_a_clk_en_h; /*

```

```

/** Declarations and Intermediate Variable Definitions **/

/** Logic Equations **/
data_perr_dlyd_l_d = (hib_active_l & hib_data0_perr_l)
# (hib_active_l & hib_data1_perr_l)
# (hib_active_l & hib_data2_perr_l)
# (hib_active_l & hib_data3_perr_l);

hib_fec_reg_h_d = hib_fec_h;

reg_siecl_a_clk_en_h_d = siecl_a_sh_reg_clk_en_h;
reg_siecl_b_clk_en_h_d = siecl_b_sh_reg_clk_en_h;

/* written for when signal goes low */
lsiecl_a_shift_reg_clk_h = diag_wr_reg_clk_h & !reg_siecl_a_clk_en_h
& lbrd2_reset_l;
lsiecl_b_shift_reg_clk_h = diag_wr_reg_clk_h & !reg_siecl_b_clk_en_h
& lbrd2_reset_l;

```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
 16R4BSL\_PCAPT.PLD

**digital**  
 FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE -	ENG: T. Nerger	DATE -	TITLE: WC BRD2
CHK'D: T. Nerger	DATE -	BOARD LOCATION: CXO	SHEET 58	
NEXT HIGHER ASSEMBLY: -				

SIZE K	CODE CS	NUMBER -	REV 25OCT88
--------	---------	----------	-------------

File: 16R4\_10SL\_MEMC7.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

16R4\_10SL\_MEMC7.PLD continued..

Name MEMC7;  
 Partno xxxxx;  
 Date 21-9-88;  
 Revision G;  
 Designer Nerger;  
 Company DEC;  
 Assembly HSB50;  
 Location XXXXX;  
 Device P16R4;

```

*****
/* MEMORY CONTROL PAL 6 - 16R4B */
/* board 2 pass 3 */
*****
/* Allowable Target Device Types: 16R4-10SL */
/* Used on HOB, HSB50 BD2 rev C (pass 3), Wildcat */
/* Revision D: 28-Jun-1988; */
/* add output enable conditions for pins 12,13,18,19 (TN)*/
/* 8/28/88 - removed !busclk from memwe1 term when writing to crams */
/* 8/8/88 - move prom_clk_h up by 50 ns (equivalent of the old */
/* bus_clk_reg1_h) and change bus_clk_reg1_h to */
/* bus_clk_reg2_h. (TN & JL) */
/* 8/15/88 - this pal is now a "D" version. The equations are */
/* unchanged - mr. rick */
/* changed to a 16R4-10SL Texas Instruments PAL; no */
/* change in equations. (TN) */
/* 19-Oct-88 moved prom_clk_h up 50ns by making old bus_clk_reg2_h*/
/* new prom_clk_h and changing old prom_clk_h to new */
/* bus_clk_reg1_h */
/* 21-Oct-88 go back to early prom clock and bus clk reg 2; */
/* change from bus_clk_reg_2 to !bus_clk_h on */
/* b2_to_hib_oet_1 (TEN) */

```

```

** Inputs **
Pin 1 = clk_20mhz_h; /* memory select */
Pin 2 = read_h; /* board 1 bus grant (BIC or proc)*/
Pin 3 = !mset_l; /* bus_clk_h; */
Pin 4 = !reset_l; /* legitimate hib cycle in process*/
Pin 5 = !brd1_grant_l; /* output enable 2 - pulled up */
Pin 6 = bus_clk_h; /* output enable 1 - pulled down */
Pin 7 = !hib_active_l;
Pin 8 = oe2;
Pin 9 = !sism_reg_cs_l;
Pin 11 = !oe1;

```

```

** Outputs **
Pin 12 = hib_addr_latch_en_h; /* enables board 1 address latches*/
Pin 13 = !b2_to_hib_oet_l; /* drive data to board 1 */
Pin 18 = !hib_to_b2_oer_l; /* receive data from board 1 */
Pin 19 = !mem_we_l; /* write enable for SRAM's */
Pin 14 = prom_clk_h; /* clocks SISM PROM registers */
Pin 15 = bus_clk_reg2_h; /* used only to register bus clk */
Pin 16 = xcvr_clk_h; /* equations written for active 1 */
Pin 17 = memcs_clk_h; /* clock to control sram chip selects */

```

```

** Logic Equations **

bus_clk_reg2_h_d = prom_clk_h;

prom_clk_h_d = bus_clk_h;

mem_we_l = !reset_l
          & hib_active_l

```

```

& !read_h
& ((!bus_clk_h
& bus_clk_reg2_h
& mset_l)
# (sism_reg_cs_l & bus_clk_reg2_h & prom_clk_h));

hib_to_b2_oer_l = !reset_l /* write from brd1 to brd2 */
& hib_active_l
& brd1_grant_l
& !read_h
& ((!mset_l & !(bus_clk_h & !prom_clk_h &
!bus_clk_reg2_h)
# ( mset_l & !bus_clk_h));

b2_to_hib_oet_l = !reset_l & /* read from brd2 to brd1 */
hib_active_l
& brd1_grant_l
& read_h
& !bus_clk_h;

xcvr_clk_h_d = prom_clk_h # bus_clk_reg2_h ;

hib_addr_latch_en_h = !reset_l
& hib_active_l
& brd1_grant_l
& bus_clk_h;

memcs_clk_h_d = hib_active_l
& !sism_reg_cs_l
& (read_h
& (!read_h &
# (bus_clk_h & prom_clk_h)
# (prom_clk_h & bus_clk_reg2_h)));

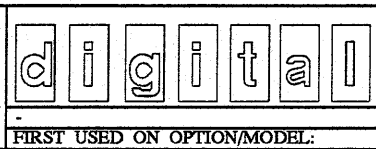
hib_addr_latch_en_h_oe = oe2;
b2_to_hib_oet_loe = oe2;
hib_to_b2_oer_loe = oe2;
mem_we_loe = oe2;

```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
 16R4\_10SL\_MEMC7.PLD



DRN:	T. Nerger	DATE	-	ENG:	T. Nerger	DATE	-	TITLE:	WC BRD2
CHK'D:	T. Nerger	DATE	-	BOARD LOCATION:	CXO	SHEET	59	SIZE	K
FIRST USED ON OPTION/MODEL:		Tue Oct 25 16:44:27 1988		NEXT HIGHER ASSEMBLY:		NUMBER	-	REV	25OCT88

SIZE	K	CODE	CS	NUMBER	-	REV	25OCT88
------	---	------	----	--------	---	-----	---------

File: 16R4\_10SL\_MEMWB.PLD  
 Source: DISK\$HSBSIM\_B:[SIMULATION.CMS]

16R4\_10SL\_MEMWB.PLD continued..

Name MEMWB  
 Partno XXXXX;  
 Date 8-sep-88;  
 Revision B;  
 Designer Nerger;  
 Company DEC;  
 Assembly W2;  
 Location XXXXX;  
 Device P16R4;

```

|
|
| mem_we1_loe = oe2;
| mem_we2_loe = oe2;
| mem_we3_loe = oe2;

```

```

|
| *****
| /* MEMORY CONTROL PAL 6 - 16R4B */
|
| *****
| /* Allowable Target Device Types: 16R4-10SL */
| *****
| /* Used on Wildcat SI board */
| *****
| /* This PAL duplicates the MEM WE L signal in the MEMCS L
| /* PAL. This PAL is needed in order to drive the additional
| /* load presented by the three added banks of SRAM memory.
| *****
| /* 8-sep-88 Change to a 16R4-10SL; no equation change
| *****
|
| ** Inputs **
|
| Pin 1 = clk_20mhz_h; /*
| Pin 2 = read_h; /*
| Pin 3 = !msel_l; /* memory select
| Pin 4 = !reset_l; /*
| Pin 5 = !brd1_grant_l; /* board 1 bus grant (BIC or proc)*/
| Pin 6 = bus_clk_h; /*
| Pin 7 = !hib_active_l; /* legitimate hib cycle in process*/
| Pin 8 = oe2; /* output enable 2 - pulled up
| Pin 9 = !sism_reg_cs_l; /* output enable 1 - pulled down
| Pin 11 = !oe1; /*
|
| ** Outputs **
|
| Pin 19 = !mem_we1_l; /* write enable for SRAM's
| Pin 18 = !mem_we2_l; /* write enable for SRAM's
| Pin 13 = !mem_we3_l; /* write enable for SRAM's
| Pin 14 = prom_clk_h; /* clocks SISM PROM registers
| Pin 15 = bus_clk_reg2_h; /* used only to register bus clk
|
|
| ** Logic Equations **
|
| bus_clk_reg2_h.d = prom_clk_h;
|
| prom_clk_h.d = bus_clk_h;
|
| mem_we1_l = !reset_l
| & hib_active_l
| & !read_h
| & ((!bus_clk_h
| & bus_clk_reg2_h
| & msel_l)
| # (sism_reg_cs_l & bus_clk_reg2_h & prom_clk_h));
|
| mem_we2_l = !reset_l
| & hib_active_l
| & !read_h
| & ((!bus_clk_h
| & bus_clk_reg2_h
| & msel_l)
| # (sism_reg_cs_l & bus_clk_reg2_h & prom_clk_h));
|
| mem_we3_l = !reset_l
| & hib_active_l
| & !read_h
| & ((!bus_clk_h
| & bus_clk_reg2_h
| & msel_l)
| # (sism_reg_cs_l & bus_clk_reg2_h & prom_clk_h));
|

```

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PAL EQN FILES:**  
 16R4\_10SL\_MEMWB.PLD

**digital**

FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D: T. Nerger	DATE	BOARD LOCATION: CXO	
Tue Oct 25 16:44:34 1988		SHEET 60	
		NEXT HIGHER ASSEMBLY:	

TITLE: WC BRD2			
SIZE K	CODE CS	NUMBER	REV 25OCT88

REV .  
 NUMBER .  
 CS  
 K  
 B  
 A



**PART I: PARTS COUNT SUMMARY**

Generic Parts Summary for WC\_BRD2/REVA1\_21 - Generated 25-OCT-1988 16:17:23

PROTO QTY	FRS QTY	Generic Part Name
8	8	16L8BSL
3	3	16R4-10SL
4	4	16R4BSL
1	1	24C16SO
32	32	5258PSOJ
16	16	6287SOJ
4	4	74ALS666SO
1	1	74AS1034SO
11	11	74AS286SO
1	1	74F04SO
1	1	74F10SO
2	2	74F32SO
1	1	74F86SO
6	6	74FCT163ASOL
1	1	74FCT244ASO
18	18	74FCT245ASO
10	10	74FCT821BSO
10	10	74FCT823BSO
2	2	74FCT843BSO
4	4	74FCT863BSO
222	222	CAP C
2	2	CPCAP
10	10	CY7C128SOJ
2	2	DC535
2	2	DCSIECLV2
1	1	ESDTAB
300	300	FINGER
16	16	INDUCTOR,C
1	1	LEDA
1	1	PC2CONN100A
2	2	PC2CONN50
4	4	POST
245	245	RES,C
16	16	XFORMERSO

**PART II: EXCESS SPARES LIST**

Excess Spare Parts/Gates Summary for WC\_BRD2/REVA1\_21 - Generated 25-OCT-1988 16:17:23

-- NO EXCESS SPARES FOUND --

**PART III: PACKAGE-SPECIFIC LOGIC PART SUMMARIES**

== PLCC-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
8	8	16L8BSL
3	3	16R4-10SL
4	4	16R4BSL

== SOIC-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
1	1	24C16SO
4	4	74ALS666SO
1	1	74AS1034SO
11	11	74AS286SO
1	1	74F04SO
1	1	74F10SO
2	2	74F32SO
1	1	74F86SO
6	6	74FCT163ASOL
1	1	74FCT244ASO
18	18	74FCT245ASO
10	10	74FCT821BSO
10	10	74FCT823BSO
2	2	74FCT843BSO
4	4	74FCT863BSO

== SOJ-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
32	32	5258PSOJ
16	16	6287SOJ
10	10	CY7C128SOJ

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**PART LIST INFO:**  
Part Summaries &  
Excess Spares List

**digital**  
FIRST USED ON OPTION/MODEL: -

DRN: T. Nerger	DATE	ENG: T. Nerger	DATE
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET 68
Tue Oct 25 16:44:40 1988		NEXT HIGHER ASSEMBLY:	

TITLE: WILDCAT BOARD 2			
SIZE K	CODE CS	NUMBER -	REV 25OCT88

PART IV: DETAILED PART LIST

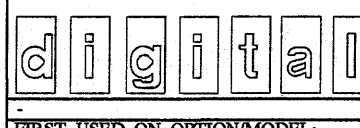
Detailed Parts List (w/Ref. Des.) for WC\_BRD2/REVA1\_21 - Generated 25-OCT-1988 16:17:47  
 [Sorted by Generic Part Number]

Quantity	Generic Name	DEC Part No.	Part Reference Designators
QTY: 1	16L8BSL	ID-BBARB-P1	E54
QTY: 1	16L8BSL	ID-CXCVR-P1	E51
QTY: 2	16L8BSL	ID-MEMCS-P1	E10,E9
QTY: 1	16L8BSL	ID-MISC2-P1	E50
QTY: 1	16L8BSL	ID-PARC2-P1	E12
QTY: 2	16L8BSL	ID-SISC1-P1	E103,E40
QTY: 1	16R4-10SL	ID-CGEN0-P1	E104
QTY: 1	16R4-10SL	ID-MEMC7-P2	E13
QTY: 1	16R4-10SL	ID-MEMWB-P2	E53
QTY: 2	16R4BSL	ID-BUSCO-P1	E11,E47
QTY: 1	16R4BSL	ID-HIBR2-P1	E8
QTY: 1	16R4BSL	ID-PCAPT-P1	E52
QTY: 1	24C16SO	21-30620-01	E48
QTY: 32	5258PSOJ	21-26937-05	E15,E17,E19,E2,E20,E29,E3,E30,E31,E33,E4,E41,E43,E45,E46,E57,E58,E59,E6,E61,E69 E71,E73,E74,E83,E84,E85,E87,E94,E96,E98,E99
QTY: 16	6287SOJ	21-24781-04	E1,E16,E18,E28,E32,E42,E44,E5,E56,E60,E70,E72,E82,E86,E95,E97
QTY: 4	74ALS666SO	19-28730-01	E106,E107,E78,E90
QTY: 1	74AS1034SO	19-26840-01	E100
QTY: 11	74AS286SO	19-26848-01	E22,E23,E25,E34,E37,E38,E55,E63,E64,E7,E79
QTY: 1	74F04SO	19-21307-02	E49
QTY: 1	74F10SO	19-21309-02	E68
QTY: 2	74F32SO	19-21312-02	E130,E140
QTY: 1	74F86SO	19-21315-02	E105
QTY: 6	74FCT163ASOL	21-30158-01	E126,E131,E137,E138,E141,E149
QTY: 1	74FCT244ASO	21-30486-01	E67
QTY: 18	74FCT245ASO	21-30487-01	E102,E109,E110,E113,E114,E115,E117,E123,E124,E128,E129,E135,E136,E143,E153,E165 E80,E92
QTY: 10	74FCT821BSO	21-30476-01	E111,E132,E27,E89,E65,E66,E76,E77,E81,E88
QTY: 10	74FCT823BSO	21-30473-01	E101,E108,E125,E35,E36,E93,E21,E24,E26,E39
QTY: 2	74FCT843BSO	21-30474-01	E14,E62
QTY: 4	74FCT863BSO	21-30475-01	E116,E133,E75,E91
QTY: 8	CAP,C	10-15605-02	C38,C46,C51,C52,C54,C55,C64,C69
QTY: 16	CAP,C	10-24051-01	C31,C32,C33,C34,C35,C36,C47,C53,C63,C77,C78,C79,C80,C81,C82,C93
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QTY: 26	CAP,C	10-24052-01	C119,C135,C145,C146,C148,C149,C152,C153,C162,C163,C168,C177,C193,C195,C196,C197 C199,C200,C208,C209,C210,C214,C217,C218,C24,C97
QTY: 136	CAP,C	10-24053-09	C100,C101,C102,C103,C104,C105,C106,C107,C108,C110,C111,C112,C113,C114,C115,C116 C118,C121,C122,C124,C125,C126,C127,C128,C129,C130,C131,C132,C133,C134,C136,C137 C138,C139,C140,C141,C142,C143,C144,C147,C150,C151,C154,C155,C156,C157,C158,C159 C160,C161,C164,C165,C166,C167,C169,C170,C171,C172,C173,C174,C175,C176,C178,C179 C180,C181,C182,C183,C184,C185,C186,C187,C188,C189,C19,C190,C191,C192,C194,C198,C20 C201,C202,C203,C204,C205,C206,C207,C21,C211,C212,C213,C215,C216,C219,C22,C220,C221 C222,C223,C224,C23,C37,C40,C41,C42,C43,C44,C45,C48,C50,C56,C58,C59,C60,C61,C62,C65 C66,C67,C70,C71,C83,C84,C85,C86,C87,C89,C90,C91,C92,C94,C95,C96,C98,C99 C109,C117,C12,C120,C123,C13,C14,C15 C1,C10,C11,C16,C2,C3,C4,C5,C6,C7,C8,C9 C17,C18
QTY: 8	CAP,C	10-24053-12	E144,E145,E146,E147,E148,E160,E161,E162,E163,E164
QTY: 12	CAP,C	10-24053-18	E139,E166
QTY: 2	CPCAP	10-24455-24	E151,E152
QTY: 10	CY7C128SOJ	21-17872-13	U1
QTY: 2	DC535	21-26499-01	L1,L10,L11,L12,L13,L14,L15,L16,L2,L3,L4,L5,L6,L7,L8,L9
QTY: 2	DCSIECLV2	19-26551-01	D1
QTY: 1	ESDITAB	99-99999-96	J3
QTY: 16	INDUCTOR,C	ID-X39UH-SM	J1,J2
QTY: 1	LEDA	11-17373-02	TP1,TP2,TP3,TP4
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QTY: 2	PC2CONN50	12-13488-14	R116,R119,R125,R127,R131,R136,R141,R144,R147,R148,R149,R150,R153,R155,R156,R162 R163,R168,R169,R177,R183,R184,R186,R187,R188,R189,R202,R209,R218,R219,R221,R222 R225,R226,R232,R233,R234,R235,R240,R242,R243,R244,R245,R32,R43,R44,R70,R91
QTY: 4	POST	90-07791-00	R124,R132,R140,R143,R152,R166,R191,R192,R197,R206,R208,R212,R217,R220,R224,R40 R42
QTY: 20	RES,C	13-23825-13	R123,R126,R139,R142,R151,R165,R190,R193,R196,R205,R207,R211,R213,R214,R223,R33 R41
QTY: 48	RES,C	13-23825-25	R1
QTY: 17	RES,C	13-23825-33	R114,R121,R128,R133,R135,R145,R146,R154,R159,R160,R161,R164,R172,R173,R174,R175 R176,R181,R185,R194,R195,R198,R203,R204,R228,R229,R230,R231,R236,R239,R241,R30,R31 R71,R75,R85,R90,R93,R94
QTY: 17	RES,C	13-23825-37	R115,R170,R171,R180,R182,R201,R26,R27,R4,R45,R5,R58,R59,R6,R64,R67,R69,R7,R76,R81 R86,R87,R92
QTY: 1	RES,C	13-23825-41	R12,R13,R14,R15,R16,R17,R2,R22,R23,R25,R29,R66,R68,R79,R8,R80
QTY: 39	RES,C	13-23825-49	R100,R113,R34,R35,R36,R37,R38,R39,R60,R72,R84,R95,R96,R97,R98,R99 R10,R101,R103,R105,R107,R109,R11,R111,R117,R18,R19,R20,R21,R24,R28,R3,R46,R48,R50 R52,R54,R56,R61,R63,R65,R73,R74,R77,R82,R83,R88,R9
QTY: 23	RES,C	13-23826-01	R102,R104,R106,R108,R110,R112,R118,R47,R49,R51,R53,R55,R57,R62,R78,R89 E112,E118,E119,E120,E121,E122,E127,E134,E142,E150,E154,E155,E156,E157,E158,E159
QTY: 16	RES,C	13-23827-44	
QTY: 16	RES,C	13-23827-91	
QTY: 32	RES,C	13-23827-94	
QTY: 16	RES,C	13-23828-03	
QTY: 16	XFORMERSO	16-29523-01	

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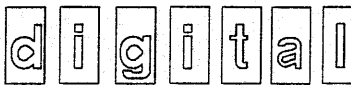


DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D: -	DATE	BOARD LOCATION: CXO	SHEET: 69	SIZE: K
FIRST USED ON OPTION/MODEL: Tue Oct 25 16:44:47 1988				NUMBER: -
NEXT HIGHER ASSEMBLY: -				REV: 25OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

12V H: C_37-1 p.36	o>E125-23 p.25 E130-2 p.3 E139-F3 p.29	E44-3 p.11 E45-3 p.11 E46-3 p.11	E1-5 p.10 E2-5 p.10 E3-5 p.10	E60-6 p.12 E61-6 p.12 E69-6 p.12	E15-8 p.10 E16-9 p.10 E17-8 p.10	E73-9 p.12 E74-9 p.12 E82-15 p.13	E21-2 p.9 E25-2 p.6 E28-17 p.11	E85-19 p.13 E86-18 p.13 E87-19 p.13	E31-21 p.11 E32-21 p.11 E33-21 p.11
3V H: C_3-1 p.36 C_18-1 p.36 C_19-1 p.36	E166-F3 p.28 J1-33 p.35 R201-2 p.41	E56-3 p.12 E57-3 p.12 E58-3 p.12	E4-5 p.10 E5-5 p.10 E6-5 p.10	E70-6 p.12 E72-6 p.12 E73-6 p.12	E18-9 p.10 E19-8 p.10 E20-8 p.10	E83-9 p.13 E84-9 p.13 E85-9 p.13	E29-18 p.11 E30-18 p.11 E31-18 p.11	o>E93-21 p.25 E94-19 p.13 E95-18 p.13	E41-21 p.11 E42-21 p.11 E43-21 p.11
5VBB H: A_3-1 p.36 A_18-1 p.36 A_19-1 p.36 A_33-1 p.36 A_34-1 p.36 A_48-1 p.36	B2 HIB ADDR 01 H: E1-2 p.10 E2-2 p.10 E3-2 p.10	E59-3 p.12 E60-3 p.12 E61-3 p.12	o>E14-19 p.6 E15-5 p.10 E16-5 p.10	E74-6 p.12 E76-6 p.12 E82-6 p.13	E21-9 p.10 E22-9 p.10 E29-8 p.11	E86-15 p.13 E87-9 p.13 E94-9 p.13	E32-17 p.11 E33-18 p.11 E41-18 p.11	E96-19 p.13 E97-18 p.13 E98-19 p.13	E44-21 p.11 E45-21 p.11 E46-21 p.11
ADR PERR L: b>E8-19 p.3 E39-7 p.9	o>E14-16 p.6 E15-2 p.10 E16-2 p.10	E72-3 p.12 E73-3 p.12 E74-3 p.12	E17-5 p.10 E18-5 p.10 E19-5 p.10	E83-6 p.13 E84-6 p.13 E85-6 p.13	E30-8 p.11 E31-8 p.11 E32-9 p.11	E95-15 p.13 E96-9 p.13 E97-15 p.13	E42-17 p.11 E43-18 p.11 E44-17 p.11	E99-19 p.13 o>E101-21 p.25 E103-2 p.22	E56-21 p.12 E57-21 p.12 E58-21 p.12
ADR BIT A DATA H: b>E129-14 p.16 b>E161-14 p.17 E166-G12 p.28	E17-2 p.10 E18-2 p.10 E19-2 p.10	E82-3 p.13 E83-3 p.13 E84-3 p.13	E20-5 p.10 E21-5 p.10 E22-5 p.10	E86-6 p.13 E87-6 p.13 E94-6 p.13	E33-5 p.11 E34-5 p.11 E35-5 p.11	E98-9 p.13 o>E108-15 p.25 o>E125-15 p.25	E45-18 p.12 E46-18 p.11 E56-17 p.12	E99-19 p.13 E1-20 p.10 E2-20 p.10	E59-21 p.12 E60-21 p.12 E61-21 p.12
ADR BIT A EN L: b>E143-13 p.16 b>E162-15 p.17 E166-E14 p.28	E20-2 p.10 E21-5 p.8 E28-2 p.11	E85-3 p.13 E86-3 p.13 E87-3 p.13	E23-5 p.11 E24-5 p.11 E25-5 p.11	E96-6 p.13 E97-6 p.13 E98-6 p.13	E36-5 p.11 E37-5 p.11 E38-5 p.11	J2-8 p.35 B2 HIB ADDR 09 H: E1-16 p.10	E58-18 p.12 E59-18 p.12 E60-17 p.12	E99-19 p.13 E1-20 p.10 E2-20 p.10	E62-21 p.12 E63-21 p.12 E64-21 p.12
ADR BIT B DATA H: b>E113-14 p.19 E139-G12 p.29 b>E145-14 p.20	E30-2 p.11 E31-2 p.11 E32-2 p.11	E93-3 p.13 E94-3 p.13 E95-3 p.13	E26-5 p.11 E27-5 p.11 E28-5 p.11	E99-6 p.13 o>E108-18 p.25 o>E125-18 p.25	E39-5 p.11 E40-5 p.11 E41-5 p.11	J2-3 p.35 B2 HIB ADDR 06 H: E1-8 p.10	E61-18 p.12 E62-16 p.6 E69-18 p.12	E6-20 p.10 E7-20 p.10 E8-20 p.10	E65-21 p.12 E66-21 p.12 E67-21 p.12
ADR BIT B EN L: b>E123-13 p.19 E139-E14 p.29 b>E146-15 p.20	E33-2 p.11 E37-2 p.6 E41-2 p.11	E96-3 p.13 E97-3 p.13 E98-3 p.13	E29-5 p.11 E30-5 p.11 E31-5 p.11	J2-2 p.35 B2 HIB ADDR 03 H: E1-4 p.10	E42-5 p.11 E43-5 p.11 E44-5 p.11	E15-7 p.10 E16-8 p.10 E17-7 p.10	E71-18 p.12 E72-17 p.12 E73-18 p.12	E9-20 p.10 E10-20 p.10 E11-20 p.10	E68-21 p.12 E69-21 p.12 E70-21 p.12
B2 HIB ADDR 00 H: E1-1 p.10 E2-1 p.10 E3-1 p.10 E4-1 p.10 E5-1 p.10 E6-1 p.10	E42-2 p.11 E43-2 p.11 E44-2 p.11	E99-3 p.13 o>E108-21 p.25 o>E125-21 p.25	E32-5 p.11 E33-5 p.11 E34-5 p.11	E15-7 p.10 E16-8 p.10 E17-7 p.10	E45-5 p.11 E46-5 p.11 E47-5 p.11	E18-16 p.10 E19-10 p.10 E20-10 p.10	E74-18 p.12 E82-17 p.13 E83-18 p.13	E12-20 p.10 E13-20 p.10 E14-20 p.10	E71-21 p.12 E72-21 p.12 E73-21 p.12
E7-1 p.10 E8-1 p.10 E9-1 p.10 E10-1 p.10 E11-1 p.10 E12-1 p.10	E45-2 p.11 E46-2 p.11 E56-2 p.12	E99-3 p.13 E1-4 p.10 E2-4 p.10	E35-5 p.11 E36-5 p.11 E37-5 p.11	E18-8 p.10 E19-7 p.10 E20-7 p.10	E48-5 p.11 E49-5 p.11 E50-5 p.11	E21-16 p.10 E22-16 p.10 E23-16 p.10	E84-18 p.13 E85-18 p.13 E86-17 p.13	E15-20 p.10 E16-20 p.10 E17-20 p.10	E74-21 p.12 E75-21 p.12 E76-21 p.12
E13-1 p.10 E14-1 p.10 E15-1 p.10 E16-1 p.10 E17-1 p.10 E18-1 p.10	E57-2 p.12 E58-2 p.12 E59-2 p.12	E15-4 p.10 E16-4 p.10 E17-4 p.10	E38-5 p.11 E39-5 p.11 E40-5 p.11	E21-10 p.10 E22-10 p.10 E23-10 p.10	E51-5 p.11 E52-5 p.11 E53-5 p.11	E24-16 p.11 E25-16 p.11 E26-16 p.11	E87-18 p.13 o>E93-22 p.25 E94-18 p.13	E18-20 p.10 E19-20 p.10 E20-20 p.10	E77-21 p.12 E78-21 p.12 E79-21 p.12
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E31-1 p.11 E32-1 p.11 E33-1 p.11 E37-4 p.6 E41-1 p.11 E42-1 p.11 E43-1 p.11	E62-2 p.12 E63-2 p.12 E64-2 p.12	E21-4 p.10 E22-4 p.10 E23-4 p.10	E44-5 p.11 E45-5 p.11 E46-5 p.11	E27-10 p.10 E28-10 p.10 E29-10 p.10	E57-5 p.11 E58-5 p.11 E59-5 p.11	E30-10 p.11 E31-10 p.11 E32-16 p.11	E98-18 p.13 E99-18 p.13 o>E101-22 p.25	E24-20 p.11 E25-20 p.11 E26-20 p.11	E83-21 p.13 E84-21 p.13 E85-21 p.13
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E39-1 p.11 E41-1 p.11 E42-1 p.11 E43-1 p.11 E44-1 p.11 E45-1 p.11	E70-2 p.12 E71-2 p.12 E72-2 p.12	E30-4 p.10 E31-4 p.10 E32-4 p.10	E53-5 p.11 E54-5 p.11 E55-5 p.11	E36-10 p.10 E37-10 p.10 E38-10 p.10	E66-5 p.12 E67-5 p.12 E68-5 p.12	E39-10 p.11 E40-10 p.11 E41-10 p.11	o>E101-19 p.25 J1-21 p.35 B2 HIB ADDR 14 H: E1-22 p.10	E33-20 p.11 E34-20 p.11 E35-20 p.11	E92-21 p.13 E93-21 p.13 E94-21 p.13
E47-1 p.11 E48-1 p.11 E49-13 p.3 E56-1 p.12 E57-1 p.12 E58-1 p.12	E73-2 p.12 E74-2 p.12 E75-2 p.12	E33-4 p.10 E34-4 p.10 E35-4 p.10	E56-5 p.11 E57-5 p.11 E58-5 p.11	E39-10 p.10 E40-10 p.10 E41-10 p.10	E69-5 p.12 E70-5 p.12 E71-5 p.12	E42-10 p.11 E43-10 p.11 E44-16 p.11	E95-21 p.13 E96-21 p.13 E97-21 p.13	E36-20 p.11 E37-20 p.11 E38-20 p.11	E95-21 p.13 E96-21 p.13 E97-21 p.13
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E73-1 p.12 E74-1 p.12 E82-1 p.13 E83-1 p.13 E84-1 p.13 E85-1 p.13	E80-2 p.12 E81-2 p.12 E82-2 p.12	E39-4 p.10 E40-4 p.10 E41-4 p.10	E62-5 p.11 E63-5 p.11 E64-5 p.11	E45-10 p.10 E46-10 p.10 E47-10 p.10	E75-5 p.12 E76-5 p.12 E77-5 p.12	E48-10 p.11 E49-10 p.11 E50-10 p.11	E1-22 p.10 E2-22 p.10 E3-22 p.10	E42-20 p.11 E43-20 p.11 E44-20 p.11	E1-22 p.10 E2-22 p.10 E3-22 p.10
E87-1 p.13 E94-1 p.13 E95-1 p.13 E96-1 p.13 E97-1 p.13 E98-1 p.13	E83-2 p.13 E84-2 p.13 E85-2 p.13	E42-4 p.10 E43-4 p.10 E44-4 p.10	E65-5 p.11 E66-5 p.11 E67-5 p.11	E48-10 p.10 E49-10 p.10 E50-10 p.10	E78-5 p.12 E79-5 p.12 E80-5 p.12	E51-10 p.11 E52-10 p.11 E53-10 p.11	E4-22 p.10 E5-22 p.10 E6-22 p.10	E45-20 p.11 E46-20 p.11 E47-20 p.11	E4-22 p.10 E5-22 p.10 E6-22 p.10
E99-1 p.13 o>E108-23 p.25	E86-2 p.13 E87-2 p.13 E88-2 p.13	E45-4 p.10 E46-4 p.10 E47-4 p.10	E68-5 p.11 E69-5 p.11 E70-5 p.11	E51-10 p.10 E52-10 p.10 E53-10 p.10	E81-5 p.12 E82-5 p.12 E83-5 p.12	E54-10 p.11 E55-10 p.11 E56-16 p.12	E7-22 p.10 E8-22 p.10 E9-22 p.10	E48-20 p.11 E49-20 p.11 E50-20 p.11	E7-22 p.10 E8-22 p.10 E9-22 p.10

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					CHK'D:	DATE:	BOARD LOCATION: CXO		SHEET: 70	SIZE: K	CODE: CS	NUMBER:
					FIRST USED ON OPTION/MODEL:		Tue Oct 25 16:45:45 1988		NEXT HIGHER ASSEMBLY:		REV: 25OCT88	

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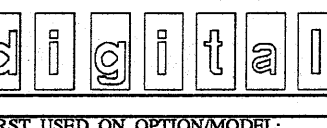
Output Source Key: o> general output t> tristate output b> bidirectional output

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E20-17 p.10 E22-9 p.7 E24-17 p.8</p>	<p>b&gt;E46-17 p.11 b&gt;E74-17 p.12 b&gt;E99-17 p.13 b&gt;E102-2 p.16 b&gt;E107-3 p.15 b&gt;E110-2 p.16 b&gt;E115-2 p.19 b&gt;E116-3 p.7 b&gt;E117-2 p.19 E132-23 p.14 b&gt;E135-18 p.27 b&gt;E165-18 p.26 J2-7 p.35 B2 HIB DATA 01 H: b&gt;E20-16 p.10 E22-10 p.7 E24-19 p.8 b&gt;E46-16 p.11 b&gt;E74-16 p.12 b&gt;E99-16 p.13 b&gt;E102-3 p.16 b&gt;E107-4 p.15 b&gt;E110-3 p.16 b&gt;E115-3 p.19 b&gt;E116-4 p.7 b&gt;E117-3 p.19 E132-22 p.14 b&gt;E135-12 p.27 b&gt;E165-12 p.26 J2-14 p.35 B2 HIB DATA 02 H: b&gt;E20-15 p.10 E21-16 p.8 E22-4 p.7 b&gt;E45-14 p.11 b&gt;E73-14 p.12 b&gt;E98-14 p.13 b&gt;E102-9 p.16 b&gt;E107-10 p.15 b&gt;E110-9 p.16 b&gt;E115-9 p.19 b&gt;E116-5 p.7 b&gt;E117-4 p.19 E132-21 p.14 b&gt;E135-16 p.27 b&gt;E165-16 p.26 J2-11 p.35 B2 HIB DATA 03 H: b&gt;E20-14 p.10 E22-12 p.7 E26-15 p.8 b&gt;E46-14 p.11 b&gt;E74-14 p.12 b&gt;E99-14 p.13 b&gt;E102-5 p.16 b&gt;E107-6 p.15 b&gt;E110-5 p.16 b&gt;E115-5 p.19 b&gt;E116-6 p.7 b&gt;E117-5 p.19 E132-20 p.14 b&gt;E135-15 p.27 b&gt;E165-15 p.26 J2-20 p.35 B2 HIB DATA 04 H: b&gt;E19-17 p.10 E21-15 p.8 E22-13 p.7 b&gt;E45-17 p.11 b&gt;E73-17 p.12 b&gt;E98-17 p.13 b&gt;E102-6 p.16 b&gt;E107-7 p.15 b&gt;E110-6 p.16 b&gt;E115-6 p.19 b&gt;E116-7 p.19 b&gt;E117-6 p.19 E132-19 p.14 b&gt;E135-14 p.27 b&gt;E165-14 p.26 J2-10 p.35 B2 HIB DATA 05 H: b&gt;E19-16 p.10 E22-1 p.7 E26-16 p.8 b&gt;E45-16 p.11</p>	<p>b&gt;E73-16 p.12 b&gt;E98-16 p.13 b&gt;E102-7 p.16 b&gt;E107-8 p.15 b&gt;E110-7 p.16 b&gt;E115-7 p.19 b&gt;E116-8 p.7 b&gt;E117-7 p.19 E132-18 p.14 b&gt;E135-13 p.27 b&gt;E165-13 p.26 J2-12 p.35 B2 HIB DATA 06 H: b&gt;E19-15 p.10 E22-2 p.7 E39-17 p.8 b&gt;E45-15 p.11 b&gt;E73-15 p.12 b&gt;E98-15 p.13 b&gt;E102-8 p.16 b&gt;E107-9 p.15 b&gt;E110-8 p.16 b&gt;E115-8 p.19 b&gt;E116-9 p.7 E132-17 p.14 b&gt;E135-12 p.27 b&gt;E165-12 p.26 J2-14 p.35 B2 HIB DATA 07 H: b&gt;E19-14 p.10 E21-16 p.8 E22-4 p.7 b&gt;E45-14 p.11 b&gt;E73-14 p.12 b&gt;E98-14 p.13 b&gt;E102-9 p.16 b&gt;E107-10 p.15 b&gt;E110-9 p.16 b&gt;E115-9 p.19 b&gt;E116-10 p.7 b&gt;E117-9 p.19 E132-16 p.14 b&gt;E135-11 p.27 b&gt;E165-11 p.26 J2-13 p.35 B2 HIB DATA 08 H: b&gt;E17-17 p.10 E21-18 p.8 E23-9 p.7 b&gt;E43-17 p.11 b&gt;E71-17 p.12 b&gt;E96-17 p.13 b&gt;E106-3 p.15 b&gt;E123-2 p.19 b&gt;E128-18 p.27 E132-15 p.14 b&gt;E133-3 p.7 b&gt;E143-2 p.16 b&gt;E153-18 p.26 J2-48 p.35 B2 HIB DATA 09 H: b&gt;E17-16 p.10 E21-20 p.8 E23-10 p.7 b&gt;E43-16 p.11 b&gt;E71-16 p.12 b&gt;E96-16 p.13 b&gt;E106-4 p.15 b&gt;E123-3 p.19 b&gt;E128-17 p.27 E132-14 p.14 b&gt;E133-4 p.7 b&gt;E143-3 p.16 b&gt;E153-17 p.26 J2-44 p.35 B2 HIB DATA 10 H: b&gt;E17-15 p.10 E21-22 p.8 E23-11 p.7 b&gt;E43-15 p.11 b&gt;E71-15 p.12 b&gt;E96-15 p.13 b&gt;E106-5 p.15 E111-23 p.14 b&gt;E123-4 p.19</p>	<p>b&gt;E128-16 p.27 b&gt;E133-5 p.7 b&gt;E143-4 p.16 b&gt;E153-16 p.26 J1-18 p.35 B2 HIB DATA 11 H: b&gt;E17-14 p.10 E23-12 p.7 E39-15 p.8 b&gt;E43-14 p.11 b&gt;E71-14 p.12 b&gt;E96-14 p.13 b&gt;E106-6 p.15 E111-22 p.14 b&gt;E123-5 p.19 b&gt;E128-15 p.27 b&gt;E133-6 p.7 b&gt;E143-5 p.16 b&gt;E153-15 p.26 J1-23 p.35 B2 HIB DATA 12 H: b&gt;E15-17 p.10 E23-13 p.7 E24-15 p.8 b&gt;E41-17 p.11 b&gt;E69-17 p.12 b&gt;E94-17 p.13 b&gt;E106-7 p.15 E111-21 p.14 b&gt;E123-6 p.19 b&gt;E128-14 p.27 b&gt;E133-7 p.15 b&gt;E143-6 p.16 b&gt;E153-14 p.26 J1-4 p.35 B2 HIB DATA 13 H: b&gt;E15-16 p.10 E23-1 p.7 E26-22 p.8 b&gt;E41-16 p.11 b&gt;E69-16 p.12 b&gt;E94-16 p.13 b&gt;E106-8 p.15 E111-20 p.14 b&gt;E123-7 p.19 b&gt;E128-13 p.27 b&gt;E133-8 p.7 b&gt;E143-7 p.16 b&gt;E153-13 p.26 J2-47 p.35 B2 HIB DATA 14 H: b&gt;E15-15 p.10 E23-2 p.7 E26-20 p.8 b&gt;E41-15 p.11 b&gt;E69-15 p.12 b&gt;E94-15 p.13 b&gt;E106-9 p.15 E111-19 p.14 b&gt;E123-8 p.19 b&gt;E128-12 p.27 b&gt;E133-9 p.7 b&gt;E143-8 p.16 b&gt;E153-12 p.26 J1-1 p.35 B2 HIB DATA 15 H: b&gt;E15-14 p.10 E23-4 p.7 E26-18 p.8 b&gt;E41-14 p.11 b&gt;E69-14 p.12 b&gt;E94-14 p.13 b&gt;E106-10 p.15 E111-18 p.14 b&gt;E123-9 p.19 b&gt;E128-11 p.27 b&gt;E133-10 p.7 b&gt;E143-9 p.16 b&gt;E153-11 p.26 J1-6 p.35 B2 HIB DATA 16 H: b&gt;E6-17 p.10 E7-9 p.7 E21-19 p.9 b&gt;E33-17 p.11 b&gt;E61-17 p.12</p>	<p>b&gt;E87-17 p.13 b&gt;E90-3 p.15 b&gt;E91-3 p.7 b&gt;E109-18 p.27 E111-17 p.14 b&gt;E113-2 p.19 b&gt;E129-2 p.16 b&gt;E136-18 p.26 J2-41 p.35 B2 HIB DATA 17 H: b&gt;E6-16 p.10 E7-10 p.7 E21-21 p.9 b&gt;E33-16 p.11 b&gt;E61-16 p.12 b&gt;E87-16 p.13 b&gt;E90-4 p.15 b&gt;E91-4 p.7 b&gt;E109-17 p.27 E111-16 p.14 b&gt;E113-3 p.19 b&gt;E129-3 p.16 b&gt;E136-17 p.26 J2-40 p.35 B2 HIB DATA 18 H: b&gt;E6-15 p.10 E7-11 p.7 E21-23 p.9 b&gt;E33-15 p.11 b&gt;E61-15 p.12 b&gt;E87-15 p.13 b&gt;E90-5 p.15 b&gt;E91-5 p.7 b&gt;E109-16 p.27 E111-15 p.14 b&gt;E113-4 p.19 b&gt;E129-4 p.16 b&gt;E136-16 p.26 J2-21 p.35 B2 HIB DATA 19 H: b&gt;E6-14 p.10 E7-12 p.7 b&gt;E33-14 p.11 E39-16 p.9 b&gt;E61-14 p.12 b&gt;E87-14 p.13 b&gt;E90-6 p.15 b&gt;E91-6 p.7 b&gt;E109-15 p.27 E111-14 p.14 b&gt;E113-5 p.19 b&gt;E129-5 p.16 b&gt;E136-15 p.26 J2-22 p.35 B2 HIB DATA 20 H: b&gt;E4-17 p.10 E7-13 p.7 E26-19 p.9 b&gt;E31-17 p.11 b&gt;E59-17 p.12 b&gt;E85-17 p.13 b&gt;E89-23 p.14 b&gt;E90-7 p.15 b&gt;E91-7 p.7 b&gt;E109-14 p.27 b&gt;E113-6 p.19 b&gt;E129-6 p.16 b&gt;E136-14 p.26 J2-19 p.35 B2 HIB DATA 21 H: b&gt;E4-16 p.10 E7-14 p.7 E26-21 p.9 b&gt;E31-16 p.11 b&gt;E59-16 p.12 b&gt;E85-16 p.13 b&gt;E89-17 p.14 b&gt;E90-8 p.15 b&gt;E91-8 p.7 b&gt;E109-13 p.27 b&gt;E113-7 p.19 b&gt;E129-7 p.16 b&gt;E136-13 p.26 J2-18 p.35 B2 HIB DATA 22 H: b&gt;E4-15 p.10</p>	<p>E7-2 p.7 E26-17 p.9 b&gt;E31-15 p.11 b&gt;E59-15 p.12 b&gt;E85-15 p.13 b&gt;E89-21 p.14 b&gt;E90-9 p.15 b&gt;E91-9 p.7 b&gt;E109-12 p.27 b&gt;E113-8 p.19 b&gt;E129-8 p.16 b&gt;E136-12 p.26 J2-17 p.35 B2 HIB DATA 23 H: b&gt;E4-14 p.10 E7-4 p.7 E26-23 p.9 b&gt;E31-14 p.11 b&gt;E59-14 p.12 b&gt;E85-14 p.13 b&gt;E89-20 p.14 b&gt;E90-10 p.15 b&gt;E91-10 p.7 b&gt;E109-11 p.27 b&gt;E113-9 p.19 b&gt;E129-9 p.16 b&gt;E136-11 p.26 J2-15 p.35 B2 HIB DATA 24 H: b&gt;E3-17 p.10 E24-16 p.9 b&gt;E30-17 p.11 E38-9 p.7 b&gt;E58-17 p.12 b&gt;E75-3 p.7 b&gt;E80-2 p.19 b&gt;E84-17 p.13 b&gt;E89-19 p.14 b&gt;E92-2 p.16 b&gt;E114-18 p.27 b&gt;E124-18 p.26 J1-15 p.35 B2 HIB DATA 25 H: b&gt;E3-16 p.10 E24-18 p.9 b&gt;E30-16 p.11 E38-10 p.7 b&gt;E58-16 p.12 b&gt;E75-4 p.7 E39-19 p.9 b&gt;E57-14 p.12 b&gt;E75-10 p.7 b&gt;E78-10 p.15 b&gt;E80-9 p.19 b&gt;E83-15 p.13 b&gt;E92-8 p.16 b&gt;E114-12 p.27 b&gt;E124-12 p.26 J1-12 p.35 B2 HIB DATA 31 H: b&gt;E2-14 p.10 b&gt;E29-14 p.11 E34-3 p.4 E49-3 p.4 b&gt;E54-18 p.4 E66-11 p.4 BRD1 NXT BUS GRANT L: E12-17 p.5 E21-1 p.9 E24-1 p.9 E26-1 p.9 E39-1 p.39 b&gt;E54-17 p.4 J2-31 p.35 B2 HIB DATA P0 H: E18-10 p.10 E18-14 p.10 b&gt;E22-6 p.7 E44-10 p.11 E72-10 p.12 E72-14 p.12 E97-10 p.13 E97-14 p.13 b&gt;E116-2 p.7 J2-28 p.35 B2 HIB DATA P1 H: b&gt;E16-10 p.10 E16-14 p.10 b&gt;E23-6 p.7 E42-10 p.11 E42-14 p.11 E70-10 p.12 E70-14 p.12 E95-10 p.13 E95-14 p.13 b&gt;E133-2 p.7 J1-3 p.35 B2 HIB DATA P2 H: E15-10 p.10</p>	<p>E5-14 p.10 b&gt;E7-6 p.7 E32-10 p.11 E32-14 p.11 E60-10 p.12 E60-14 p.12 E86-10 p.13 E86-14 p.13 b&gt;E91-2 p.7 J2-42 p.35 B2 HIB DATA P3 H: E1-10 p.10 E1-14 p.10 E28-10 p.11 E28-14 p.11 b&gt;E38-6 p.7 E56-10 p.12 E56-14 p.12 b&gt;E75-2 p.7 E82-10 p.13 E82-14 p.13 J1-13 p.35 B2 TO HIB OET L: E13-13 p.5 E75-13 p.7 E75-14 p.7 E91-13 p.7 E91-14 p.7 E116-13 p.7 E116-14 p.7 E133-13 p.7 E133-14 p.7 J1-10 p.35 BD2 REG CS L: b&gt;E2-15 p.10 E21-17 p.9 E54-5 p.4 E66-19 p.3 J2-35 p.35 BRD1 GRANT H: E12-2 p.5 E66-14 p.4 BRD1 GRANT L: E8-2 p.3 E13-5 p.5 E14-1 p.6 E27-1 p.4 E53-5 p.5 E62-1 p.4 E66-18 p.4 BRD1 NXT BUS GRANT H: E34-3 p.4 E49-3 p.4 b&gt;E54-18 p.4 E66-11 p.4 BRD1 NXT BUS GRANT L: E49-4 p.4 E66-7 p.4 BRD2 BUSCLK H: C97-1 p.40 E100-3 p.3 E100-11 p.3 E100-13 p.3 J3-4 p.37 E18-14 p.10 R123-2 p.40 R124-2 p.40 BRD2 EE CLK H: E48-10 p.25 E50-14 p.23 E89-9 p.14 R170-2 p.42 R170-2 p.42 BRD2 EE DATA H: E50-2 p.23 J3-49 p.37 R182-2 p.42 BRD2 EE RD DATA H: b&gt;E48-9 p.25 b&gt;E50-13 p.23 E89-8 p.14 J3-85 p.37 R180-2 p.42 BRD2 EE WR H: E50-3 p.23 J3-79 p.37 R171-2 p.42 BRD2 RESET L: C91-1 p.41 E13-4 p.5</p>	<p>E52-3 p.5 E53-4 p.5 E78-11 p.15 E90-11 p.15 E106-11 p.15 E107-11 p.15 J3-90 p.37 R114-2 p.41 BUS CLK A H: C168-1 p.40 E11-1 p.23 E13-6 p.5 E24-13 p.9 E27-13 p.4 E39-13 p.39 E47-1 p.23 E49-11 p.3 E53-6 p.5 E65-13 p.23 E66-13 p.24 E77-13 p.24 E89-13 p.14 E100-10 p.3 R192-2 p.40 R193-2 p.40 E75-14 p.7 E91-13 p.7 E91-14 p.7 E116-13 p.7 E116-14 p.7 E133-13 p.7 E133-14 p.7 J1-10 p.35 BD2 REG CS L: b&gt;E12-16 p.5 E54-5 p.4 E66-19 p.3 J2-35 p.35 BRD1 GRANT H: E12-2 p.5 E66-14 p.4 BRD1 GRANT L: E8-2 p.3 E13-5 p.5 E14-1 p.6 E27-1 p.4 E53-5 p.5 E62-1 p.4 E66-18 p.4 BRD1 NXT BUS GRANT H: E34-3 p.4 E49-3 p.4 b&gt;E54-18 p.4 E66-11 p.4 BRD1 NXT BUS GRANT L: E49-4 p.4 E66-7 p.4 BRD2 BUSCLK H: C97-1 p.40 E100-3 p.3 E100-11 p.3 E100-13 p.3 J3-4 p.37 E18-14 p.10 R123-2 p.40 R124-2 p.40 BRD2 EE CLK H: E48-10 p.25 E50-14 p.23 E89-9 p.14 R170-2 p.42 R170-2 p.42 BRD2 EE DATA H: E50-2 p.23 J3-49 p.37 R182-2 p.42 BRD2 EE RD DATA H: b&gt;E48-9 p.25 b&gt;E50-13 p.23 E89-8 p.14 J3-85 p.37 R180-2 p.42 BRD2 EE WR H: E50-3 p.23 J3-79 p.37 R171-2 p.42 BRD2 RESET L: C91-1 p.41 E13-4 p.5</p>	<p>CAL CLK TEST A H: E90-17 p.15 E105-5 p.28 CAL CLK TEST B H: E90-16 p.15 E105-2 p.29 CHAN A PORT ENA H: E50-19 p.23 E151-H1 p.28 E152-H1 p.28 CHAN A PORT SEL 0 H: E151-J1 p.28 E152-J1 p.29 E166-H1 p.28 CHAN A PORT SEL 1 H: E151-H2 p.28 E152-H2 p.29 E166-G2 p.28 CHAN A PORT SEL 2 H: E67-15 p.25 E67-17 p.25 E166-G1 p.28 CHAN A RRD H: E151-E3 p.28 E152-E3 p.29 E166-K3 p.28 R64-2 p.34 CHAN A RRD PLS ERR L: E151-E2 p.28 E152-E2 p.29 E166-J1 p.28 R26-2 p.34 CHAN A RRD/WCD CLK H: E151-B1 p.28 E151-C1 p.28 E152-B1 p.29 E152-C1 p.29 E166-K2 p.28 R217-2 p.40 CHAN A RTCS H: E151-A4 p.28 E152-A4 p.29 E166-M10 p.28 R67-2 p.34 CHAN A RTCS CLK H: E151-A3 p.28 E151-C4 p.28 E152-A3 p.29 E152-C4 p.29 E166-M9 p.28 R67-2 p.34 CHAN A WCD H: E151-C2 p.28 E152-C2 p.29 E166-K1 p.28 R27-2 p.34 CHAN B PORT ENA H: E50-12 p.23 E151-G14 p.28 E152-G14 p.29 CHAN B PORT SEL 0 H: E151-H1 p.29 E151-J14 p.28 E152-J14 p.29 CHAN B PORT SEL 1 H: E151-G2 p.28 E151-H13 p.28 E152-H13 p.29 CHAN B PORT SEL 2 H: E67-11 p.25 E67-13 p.25 E151-G1 p.29 CHAN B RRD H: E151-K3 p.29 E151-E14 p.28 E152-E14 p.29 R5-2 p.34 CHAN B RRD PLS ERR L: E151-F14 p.28 E151-F14 p.29 E151-F14 p.29 E152-F14 p.29 R4-2 p.34 CHAN B RRD/WCD CLK H: E151-K2 p.29 E151-F12 p.28 E151-F13 p.28 E152-F12 p.29 E152-F13 p.29</p>
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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**CROSS REFERENCE:**  
Signal Names



DRN:	T. Nerger	DATE	ENG:	T. Nerger	DATE	TITLE:
CHK'D:		DATE	BOARD LOCATION:	CXO		WILDCAT BOARD 2
			SHEET:	71		
			NEXT HIGHER ASSEMBLY:			
FIRST USED ON OPTION/MODEL:						

SIZE	CODE	NUMBER	REV
K	CS	-	25OCT88

Output Sources for nets listed in cross-reference available upon request

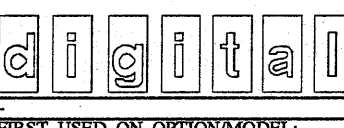
Output Source Key: o> general output t> tristate output b> bidirectional output

<p>CHAN B RTCS H: o&gt;E139-M10 p.29 E151-B13 p.28 E152-B13 p.29 R7-2 p.34</p> <p>CHAN B RTCS CLK H: E139-M9 p.29 E151-A14 p.28 o&gt;E151-C11 p.28 E152-A14 p.29 o&gt;E152-C11 p.29</p> <p>CHAN B WCD H: o&gt;E139-K1 p.29 E151-D14 p.28 E152-D14 p.29 R6-2 p.34</p> <p>CHANNEL A PORT ENA H: E50-11 p.23 o&gt;E166-F2 p.28 R45-2 p.42</p> <p>CHANNEL B PORT ENA H: E50-8 p.23 o&gt;E139-F2 p.29 R86-2 p.42</p> <p>CH A PORT SEL 2 BUFA H: o&gt;E67-3 p.25 E151-J2 p.28</p> <p>CH A PORT SEL 2 BUFB H: o&gt;E67-5 p.25 E152-J2 p.29</p> <p>CH B PORT SEL 2 BUFA H: o&gt;E67-7 p.25 E151-H14 p.28</p> <p>CH B PORT SEL 2 BUFB H: o&gt;E67-9 p.25 E152-H14 p.29</p> <p>CLK 20MHZ H: C208-1 p.40 E13-1 p.5 E53-1 p.5 E54-7 p.4 o&gt;E100-2 p.3 E139-C1 p.29 E166-C1 p.28 R214-2 p.40 R220-2 p.40</p> <p>CLR PERR L: E8-3 p.3 o&gt;E90-18 p.15</p> <p>CRAM A MARK H: b&gt;E110-12 p.16 b&gt;E163-16 p.17 J1-42 p.35</p> <p>CRAM A OVERFLOW H: E89-10 p.14 o&gt;E139-11 p.17</p> <p>CRAM A PARITY H: E81-11 p.18 b&gt;E110-11 p.16 b&gt;E163-17 p.17</p> <p>CRAM A SPARE 1 H: b&gt;E110-15 p.16 b&gt;E163-13 p.17</p> <p>CRAM A SPARE 2 H: b&gt;E110-14 p.16 b&gt;E163-14 p.17</p> <p>CRAM A SPARE 3 H: b&gt;E110-13 p.16 b&gt;E163-15 p.17</p> <p>CRAM B MARK H: b&gt;E117-12 p.19 b&gt;E148-16 p.20 J1-44 p.35</p> <p>CRAM B OVERFLOW H: E89-11 p.14 o&gt;E137-11 p.20</p> <p>CRAM B PARITY H: E65-8 p.21 b&gt;E117-11 p.19 b&gt;E148-17 p.20</p> <p>CRAM B SPARE 1 H: b&gt;E117-15 p.19 b&gt;E148-13 p.20</p> <p>CRAM B SPARE 2 H: b&gt;E117-14 p.19 b&gt;E148-14 p.20</p>	<p>CRAM B SPARE 3 H: b&gt;E117-13 p.19 b&gt;E148-15 p.20</p> <p>CSIC A ADDR REG EN L: b&gt;E47-18 p.23 E51-11 p.23 E101-14 p.25 E125-14 p.25</p> <p>CSIC A CS L: E66-10 p.3 o&gt;E67-16 p.3 E166-D2 p.28</p> <p>CSIC A DAL 00 H: b&gt;E165-2 p.26 b&gt;E166-A1 p.28 CSIC A DAL 01 H: b&gt;E165-3 p.26 b&gt;E166-A2 p.28 CSIC A DAL 02 H: b&gt;E165-4 p.26 b&gt;E166-A3 p.28 CSIC A DAL 03 H: b&gt;E165-5 p.26 b&gt;E166-A4 p.28 CSIC A DAL 04 H: b&gt;E165-6 p.26 b&gt;E166-A5 p.28 CSIC A DAL 05 H: b&gt;E165-7 p.26 b&gt;E166-A6 p.28 CSIC A DAL 06 H: b&gt;E165-8 p.26 b&gt;E166-A7 p.28 CSIC A DAL 07 H: b&gt;E165-9 p.26 b&gt;E166-A8 p.28 CSIC A DAL 08 H: b&gt;E165-10 p.26 b&gt;E166-A9 p.28 CSIC A DAL 09 H: b&gt;E165-11 p.26 b&gt;E166-B0 p.28 CSIC A DAL 10 H: b&gt;E165-12 p.26 b&gt;E166-B1 p.28 CSIC A DAL 11 H: b&gt;E165-13 p.26 b&gt;E166-B2 p.28 CSIC A DAL 12 H: b&gt;E165-14 p.26 b&gt;E166-B3 p.28 CSIC A DAL 13 H: b&gt;E165-15 p.26 b&gt;E166-B4 p.28 CSIC A DAL 14 H: b&gt;E165-16 p.26 b&gt;E166-B5 p.28 CSIC A DAL 15 H: b&gt;E165-17 p.26 b&gt;E166-B6 p.28 CSIC A DAL 16 H: b&gt;E165-18 p.26 b&gt;E166-B7 p.28 CSIC A DAL 17 H: E125-3 p.25 b&gt;E166-B8 p.28 CSIC A DAL 18 H: E125-4 p.25 b&gt;E166-B9 p.28 CSIC A DAL 19 H: E125-5 p.25 b&gt;E166-C0 p.28 CSIC A DAL 20 H: E125-6 p.25 b&gt;E166-C1 p.28 CSIC A DAL 21 H: E125-7 p.25 b&gt;E166-C2 p.28 CSIC A DAL 22 H: E125-8 p.25 b&gt;E166-C3 p.28</p>	<p>b&gt;E136-8 p.26 b&gt;E166-B6 p.28 CSIC A DAL 23 H: E125-9 p.25 b&gt;E136-9 p.26 b&gt;E166-B7 p.28 CSIC A DAL 24 H: b&gt;E124-2 p.26 E125-10 p.25 b&gt;E166-A9 p.28 CSIC A DAL 25 H: E101-2 p.25 b&gt;E124-3 p.26 b&gt;E166-A10 p.28 CSIC A DAL 26 H: E101-3 p.25 b&gt;E124-4 p.26 b&gt;E166-A11 p.28 CSIC A DAL 27 H: E101-4 p.25 b&gt;E124-5 p.26 b&gt;E166-A12 p.28 CSIC A DAL 28 H: E101-5 p.25 b&gt;E124-6 p.26 b&gt;E166-A13 p.28 CSIC A DAL 29 H: E101-6 p.25 b&gt;E124-7 p.26 b&gt;E166-A14 p.28 CSIC A DAL 30 H: E101-7 p.25 b&gt;E124-8 p.26 b&gt;E166-A15 p.28 CSIC A DAL 31 H: E101-8 p.25 b&gt;E124-9 p.26 b&gt;E166-C13 p.28 CSIC A DAL 32 H: E101-9 p.25 o&gt;E166-C14 p.28 CSIC A DAL 33 H: E101-10 p.25 o&gt;E166-D13 p.28 CSIC A HI DAL DIR H: b&gt;E51-14 p.23 E124-1 p.26 E136-1 p.26 CSIC A HI DAL EN L: b&gt;E51-13 p.23 E124-19 p.26 E136-19 p.26 CSIC A INT L: E67-8 p.3 o&gt;E166-M2 p.28 CSIC A LO DAL DIR H: o&gt;E51-19 p.23 E153-1 p.26 E165-1 p.26 CSIC A LO DAL EN L: o&gt;E51-12 p.23 E153-19 p.26 E165-19 p.26 CSIC A PARITY OUT H: E55-1 p.24 o&gt;E166-N3 p.28 CSIC A REG CS L: E12-9 p.5 E51-4 p.23 E66-15 p.3 J1-49 p.35 CSIC A TMUX 0 H: o&gt;E139-P2 p.29 E140-5 p.17 o&gt;E166-M12 p.28 R76-2 p.41 CSIC A TMUX 1 H: o&gt;E139-M4 p.29 E140-13 p.17 o&gt;E166-N13 p.28 R81-2 p.41 CSIC A TMUX 2 H: o&gt;E139-P1 p.29 E140-2 p.17 o&gt;E166-N12 p.28 R69-2 p.41</p>	<p>CSIC B ADDR REG EN L: b&gt;E11-18 p.23 E51-1 p.23 E93-14 p.25 E108-14 p.25 CSIC B CS L: E66-8 p.3 o&gt;E67-18 p.3 E139-D2 p.29 CSIC B DAL 00 H: b&gt;E135-2 p.27 b&gt;E139-A10 p.29 CSIC B DAL 01 H: b&gt;E135-3 p.27 b&gt;E139-A2 p.29 CSIC B DAL 02 H: b&gt;E135-4 p.27 b&gt;E139-A3 p.29 CSIC B DAL 03 H: b&gt;E135-5 p.27 b&gt;E139-A4 p.29 CSIC B DAL 04 H: b&gt;E135-6 p.27 b&gt;E139-A5 p.29 CSIC B DAL 05 H: b&gt;E135-7 p.27 b&gt;E139-A6 p.29 CSIC B DAL 06 H: b&gt;E135-8 p.27 b&gt;E139-A7 p.29 CSIC B DAL 07 H: b&gt;E135-9 p.27 b&gt;E139-A8 p.29 CSIC B DAL 08 H: b&gt;E128-2 p.27 b&gt;E139-B8 p.29 CSIC B DAL 09 H: b&gt;E128-3 p.27 b&gt;E139-C8 p.29 CSIC B DAL 10 H: b&gt;E128-4 p.27 b&gt;E139-B9 p.29 CSIC B DAL 11 H: b&gt;E128-5 p.27 b&gt;E139-C9 p.29 CSIC B DAL 12 H: b&gt;E128-6 p.27 b&gt;E139-B10 p.29 CSIC B DAL 13 H: b&gt;E128-7 p.27 b&gt;E139-B11 p.29 CSIC B DAL 14 H: b&gt;E128-8 p.27 b&gt;E139-B12 p.29 CSIC B DAL 15 H: b&gt;E128-9 p.27 b&gt;E139-B13 p.29 CSIC B DAL 16 H: E108-2 p.25 b&gt;E109-2 p.27 E135-19 p.27 CSIC B DAL 17 H: E108-3 p.25 b&gt;E109-3 p.27 b&gt;E139-B3 p.29 CSIC B DAL 18 H: E108-4 p.25 b&gt;E109-4 p.27 b&gt;E139-B4 p.29 CSIC B DAL 19 H: E108-5 p.25 b&gt;E109-5 p.27 b&gt;E139-C5 p.29 CSIC B DAL 20 H: E108-6 p.25 b&gt;E109-6 p.27 b&gt;E139-B5 p.29 CSIC B DAL 21 H: E108-7 p.25 b&gt;E109-7 p.27 b&gt;E139-C6 p.29 CSIC B DAL 22 H: E108-8 p.25 b&gt;E109-8 p.27 b&gt;E139-B6 p.29 CSIC B DAL 23 H: E108-9 p.25 b&gt;E109-9 p.27 b&gt;E139-B7 p.29</p>	<p>E108-9 p.25 b&gt;E109-9 p.27 b&gt;E139-B7 p.29 CSIC B DAL 24 H: E108-10 p.25 b&gt;E114-2 p.27 b&gt;E139-A9 p.29 CSIC B DAL 25 H: E93-2 p.25 b&gt;E114-3 p.27 b&gt;E139-A10 p.29 CSIC B DAL 26 H: E93-3 p.25 b&gt;E114-4 p.27 b&gt;E139-A11 p.29 CSIC B DAL 27 H: E93-4 p.25 b&gt;E114-5 p.27 b&gt;E139-A12 p.29 CSIC B DAL 28 H: E93-5 p.25 b&gt;E114-6 p.27 b&gt;E139-A13 p.29 CSIC B DAL 29 H: E93-6 p.25 b&gt;E114-7 p.27 b&gt;E139-A14 p.29 CSIC B DAL 30 H: E93-7 p.25 b&gt;E114-8 p.27 b&gt;E139-B14 p.29 CSIC B DAL 31 H: E93-8 p.25 b&gt;E114-9 p.27 b&gt;E139-C13 p.29 CSIC B DAL 32 H: E93-9 p.25 o&gt;E139-C14 p.29 CSIC B DAL 33 H: E93-10 p.25 o&gt;E139-D13 p.29 CSIC B HI DAL DIR H: b&gt;E51-18 p.23 E109-1 p.27 E114-1 p.27 CSIC B HI DAL EN L: b&gt;E51-17 p.23 E109-19 p.27 E114-19 p.27 CSIC B INT L: E67-6 p.3 o&gt;E139-M2 p.29 CSIC B LO DAL DIR H: b&gt;E51-16 p.23 E128-1 p.27 E135-1 p.27 CSIC B LO DAL EN L: b&gt;E51-15 p.23 E128-19 p.27 E135-19 p.27 CSIC B PARITY OUT H: E64-1 p.24 o&gt;E139-N3 p.29 CSIC B REG CS L: E12-11 p.5 E51-5 p.23 E66-17 p.3 J1-30 p.35 CSIC B TMUX 0 H: E130-13 p.20 o&gt;E139-M12 p.29 o&gt;E166-P2 p.28 R115-2 p.41 CSIC B TMUX 1 H: E130-10 p.20 o&gt;E139-N13 p.29 o&gt;E166-M4 p.28 R92-2 p.41 CSIC B TMUX 2 H: E130-5 p.20 o&gt;E139-N12 p.29 o&gt;E166-P1 p.28 R87-2 p.41 CTRL ADDRESS A 0 H: b&gt;E143-11 p.16 b&gt;E162-17 p.17</p>	<p>E166-F14 p.28 CTRL ADDRESS A 1 H: b&gt;E129-18 p.16 b&gt;E161-9 p.17 E166-F12 p.28 CTRL ADDRESS A 2 H: b&gt;E129-17 p.16 b&gt;E161-10 p.17 E166-G14 p.28 CTRL ADDRESS A 3 H: b&gt;E129-16 p.16 b&gt;E161-11 p.17 E166-F13 p.28 CTRL ADDRESS A 4 H: b&gt;E129-15 p.16 b&gt;E161-13 p.17 E166-H14 p.28 CTRL ADDRESS B 0 H: b&gt;E123-11 p.19 E139-F14 p.29 b&gt;E146-17 p.20 CTRL ADDRESS B 1 H: b&gt;E113-18 p.19 E139-F12 p.29 b&gt;E145-9 p.20 CTRL ADDRESS B 2 H: b&gt;E113-17 p.19 E139-G14 p.29 b&gt;E145-10 p.20 CTRL ADDRESS B 3 H: b&gt;E113-16 p.19 b&gt;E139-F13 p.29 b&gt;E145-11 p.20 CTRL ADDRESS B 4 H: b&gt;E113-15 p.19 E139-H14 p.29 b&gt;E145-13 p.20 CTRL BUS A 0 H: b&gt;E129-13 p.16 b&gt;E161-15 p.17 E166-J14 p.28 CTRL BUS A 1 H: b&gt;E129-12 p.16 b&gt;E161-16 p.17 E166-G13 p.28 CTRL BUS A 2 H: b&gt;E129-11 p.16 b&gt;E161-17 p.17 E166-K14 p.28 CTRL BUS A 3 H: b&gt;E92-18 p.16 b&gt;E160-9 p.17 E166-K13 p.28 CTRL BUS A 4 H: b&gt;E92-17 p.16 b&gt;E160-10 p.17 E166-K12 p.28 CTRL BUS A 5 H: b&gt;E92-16 p.16 b&gt;E160-11 p.17 E166-L14 p.28 CTRL BUS A 6 H: E81-9 p.18 b&gt;E92-15 p.16 b&gt;E160-13 p.17 E166-L13 p.28 CTRL BUS A 7 H: E81-7 p.18 b&gt;E92-14 p.16 b&gt;E160-14 p.17 E166-M14 p.28 CTRL BUS A EN L: b&gt;E143-12 p.16 b&gt;E162-16 p.17 E166-E13 p.28 CTRL BUS B 0 H: b&gt;E113-13 p.19 E139-J14 p.29 b&gt;E145-15 p.20 CTRL BUS B 1 H: b&gt;E113-12 p.19 E139-G13 p.29 b&gt;E145-16 p.20 CTRL BUS B 2 H: b&gt;E113-11 p.19 E139-K14 p.29</p>	<p>b&gt;E145-17 p.20 CTRL BUS B 3 H: b&gt;E80-18 p.19 E139-K13 p.29 b&gt;E144-9 p.20 CTRL BUS B 4 H: b&gt;E80-17 p.19 E139-K12 p.29 b&gt;E144-10 p.20 CTRL BUS B 5 H: b&gt;E80-16 p.19 E139-L14 p.29 b&gt;E144-11 p.20 CTRL BUS B 6 H: b&gt;E80-15 p.19 E88-3 p.21 E139-L13 p.29 b&gt;E144-13 p.20 CTRL BUS B 7 H: E76-6 p.21 b&gt;E80-14 p.19 E139-M14 p.29 b&gt;E144-14 p.20 CTRL BUS B EN L: b&gt;E123-12 p.19 E139-E13 p.29 b&gt;E146-16 p.20 CTRL PAR ERR L: E27-8 p.4 A 28-1 p.36 A 29-1 p.36 A 32-1 p.36 A 36-1 p.36 A 40-1 p.36 A 43-1 p.36 A 44-1 p.36 A 56-1 p.36 A 58-1 p.36 B 32-1 p.36 B 36-1 p.36 B 39-1 p.36 B 42-1 p.36 B 50-1 p.36 B 51-1 p.36 B 52-1 p.36 B 54-1 p.36 B 56-1 p.36 B 60-1 p.36 C1-2 p.36 C2-2 p.36 C3-2 p.36 C4-2 p.36 C5-2 p.36 C6-2 p.36 C7-2 p.36 C8-2 p.36 C9-2 p.36 C10-2 p.36 C11-2 p.36 C12-2 p.36 C13-2 p.36 C14-2 p.36 C15-2 p.36 C16-2 p.36 C17-2 p.36 C18-2 p.36 C19-2 p.36 C20-2 p.36 C21-2 p.36 C22-2 p.36 C23-2 p.36 C24-2 p.36 C25-2 p.36 C26-1 p.31 C27-1 p.33 C28-1 p.33 C29-1 p.33 C30-1 p.33 C37-2 p.44 C38-2 p.34 C39-1 p.31 C40-2 p.44 C41-2 p.44 C42-2 p.44 C43-2 p.44 C44-2 p.44 C45-2 p.44 C46-2 p.34 C48-2 p.44 C49-1 p.31 C50-2 p.44 C51-2 p.34</p>	<p>o&gt;E79-5 p.24 EECLK DIAG26 H: E50-6 p.23 o&gt;E78-20 p.15 EEDATA DIAG25 H: E50-4 p.23 o&gt;E78-21 p.15 E137-6 p.20 EHW DIAG24 H: E50-5 p.23 o&gt;E78-22 p.15 E138-6 p.17 EXTERNAL DIAG CLK H: D 16-1 p.36 E68-3 p.3 R145-2 p.41 FORCE PULSE ERROR A H: o&gt;E107-20 p.15 E151-C12 p.28 FORCE PULSE ERROR B H: o&gt;E106-19 p.15 E152-C12 p.29 GND H: A 13-1 p.36 A 28-1 p.36 A 29-1 p.36 A 32-1 p.36 A 36-1 p.36 A 40-1 p.36 A 43-1 p.36 A 44-1 p.36 A 56-1 p.36 A 58-1 p.36 B 32-1 p.36 B 36-1 p.36 B 39-1 p.36 B 42-1 p.36 B 50-1 p.36 B 51-1 p.36 B 52-1 p.36 B 54-1 p.36 B 56-1 p.36 B 60-1 p.36 C1-2 p.36 C2-2 p.36 C3-2 p.36 C4-2 p.36 C5-2 p.36 C6-2 p.36 C7-2 p.36 C8-2 p.36 C9-2 p.36 C10-2 p.36 C11-2 p.36 C12-2 p.36 C13-2 p.36 C14-2 p.36 C15-2 p.36 C16-2 p.36 C17-2 p.36 C18-2 p.36 C19-2 p.36 C20-2 p.36 C21-2 p.36 C22-2 p.36 C23-2 p.36 C24-2 p.36 C25-2 p.36 C26-1 p.36 C27-1 p.36 C28-1 p.36 C29-1 p.36 C30-1 p.36 C37-2 p.44 C38-2 p.34 C39-1 p.31 C40-2 p.44 C41-2 p.44 C42-2 p.44 C43-2 p.44 C44-2 p.44 C45-2 p.44 C46-2 p.34 C48-2 p.44 C49-1 p.31 C50-2 p.44 C51-2 p.34</p>	<p>C52-2 p.34 C54-2 p.34 C55-2 p.34 C56-2 p.44 C57-1 p.30 C58-2 p.44 C59-2 p.44 C60-2 p.44 C61-2 p.44 C62-2 p.44 C64-2 p.34 C65-2 p.44 C66-2 p.44 C67-2 p.44 C68-1 p.30 C69-2 p.34 C70-2 p.44 C71-2 p.44 C72-1 p.30 C73-1 p.32 C74-1 p.32 C75-1 p.32 C76-1 p.32 C83-2 p.44 C84-2 p.44 C85-2 p.44 C86-2 p.44 C87-2 p.44 C88-1 p.30 C89-2 p.44 C90-2 p.44 C91-2 p.41 C92-2 p.44 C94-2 p.44 C95-2 p.44 C96-2 p.44 C98-2 p.44 C99-2 p.44 C100-2 p.44 C101-2 p.44 C102-2 p.44 C103-2 p.44 C104-2 p.44 C105-2 p.44 C106-2 p.44 C107-2 p.44 C108-2 p.44 C109-2 p.36 C110-2 p.45 C111-2 p.45 C112-2 p.45 C113-2 p.45 C114-2 p.45 C115-2 p.45 C116-2 p.44 C117-2 p.36 C118-2 p.44 C119-2 p.36 C121-2 p.44 C122-2 p.44 C123-2 p.36 C124-2 p.36 C125-2 p.45 C126-2 p.45 C127-2 p.45 C128-2 p.45 C129-2 p.45 C130-2 p.44 C131-2 p.44 C132-2 p.44 C133-2 p.44 C134-2 p.44 C136-2 p.44 C137-2 p.44 C138-2 p.44 C139-2 p.45 C140-2 p.45 C141-2 p.45 C142-2 p.45 C143-2 p.45 C144-2 p.45 C147-2 p.44 C150-2 p.44 C151-2 p.44 C154-2 p.44 C155-2 p.44</p>	<p>C156-2 p.45 C157-2 p.45 C158-2 p.45 C159-2 p.45 C160-2 p.45 C161-2 p.45 C164-2 p.44 C165-2 p.44 C166-2 p.44 C167-2 p.44 C169-2 p.44 C170-2 p.45 C171-2 p.45 C172-2 p.45 C173-2 p.45 C174-2 p.45 C175-2 p.45 C176-2 p.44 C177-2 p.44 C178-2 p.44 C179-2 p.44 C180-2 p.44 C181-2 p.44 C182-2 p.44 C183-2 p.44 C184-2 p.44 C185-2 p.45 C186-2 p.45 C187-2 p.45 C188-2 p.45 C189-2 p.45 C190-2 p.45 C191-2 p.44 C192-2 p.44 C194-2 p.44 C198-2 p.44 C201-2 p.45 C202-2 p.45 C203-2 p.45 C204-2 p.45 C205-2 p.45 C206-2 p.45 C207-2 p.44 C211-2 p.44 C212-2 p.44 C213-2 p.44 C215-2 p.44 C216-2 p.44 C219-2 p.45 C220-2 p.45 C221-2 p.45 C222-2 p.45 C223-2 p.45 C224-2 p.45 C 1-1 p.36 C 4-1 p.36 C 10-1 p.36 C 13-1 p.36 C 14-1 p.36 C 15-1 p.36 C 27-1 p.36 C 28-1 p.36 C 29-1 p.36 C 30-1 p.36 C 32-1 p.36 C 36-1 p.36 C 41-1 p.36 C 43-1 p.36 C 44-1 p.36 C 51-1 p.36 C 52-1 p.36 C 53-1 p.36 C 56-1 p.36 C 58-1 p.36 C 60-1 p.36 D 46-1 p.36 E48-2 p.25 E48-3 p.25 E48-5 p.25 E48-12 p.25 E151-A2 p.28 E151-B3 p.28 E151-C3 p.28 E151-D3 p.28 E151-E3 p.28 E151-F3 p.28 E151-G3 p.28 E151-H3 p.28 E151-I3 p.28 E151-J3 p.28 E151-K3 p.28 E151-L3 p.28 E151-M3 p.28 E151-N3 p.28 E151-O3 p.28 E151-P3 p.28 E151-Q3 p.28 E151-R3 p.28 E151-S3 p.28 E151-T3 p.28 E151-U3 p.28 E151-V3 p.28 E151-W3 p.28 E151-X3 p.28 E151-Y3 p.28 E151-Z3 p.28</p>
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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**CROSS REFERENCE:**  
Signal Names



DRN: T. Nerger  
CHK'D: -  
FIRST USED ON OPTION/MODEL: -

DATE: -  
DATE: -  
DATE: -  
DATE: -

ENG: T. Nerger  
BOARD LOCATION: CXO  
SHEET: 72  
NEXT HIGHER ASSEMBLY: -  
TITLE: WILDCAT BOARD 2  
SIZE: K  
CODE: CS  
NUMBER: -  
REV: 250CT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

E151-G3 p.28 E151-J3 p.28 E151-B14 p.28 E151-C10 p.28 E151-C13 p.28 E151-E12 p.28 E151-H12 p.28 E152-A2 p.29 E152-B3 p.29 E152-C3 p.29 E152-C6 p.29 E152-C7 p.29 E152-C9 p.29 E152-D3 p.29 E152-G3 p.29 E152-J3 p.29 E152-B14 p.29 E152-C10 p.29 E152-C13 p.29 E152-E12 p.29 E152-H12 p.29 J1-17 p.35 J1-47 p.35 J2-27 p.35 J2-49 p.35 J3-1 p.37 J3-3 p.37 J3-5 p.37 J3-6 p.37 J3-14 p.37 J3-24 p.37 J3-34 p.37 J3-44 p.37 J3-50 p.37 J3-64 p.37 J3-72 p.37 J3-84 p.37 J3-94 p.37 J3-100 p.37 R2-1 p.30 R8-1 p.32 R12-1 p.30 R13-1 p.32 R14-1 p.31 R15-1 p.33 R16-1 p.30 R17-1 p.32 R22-1 p.31 R23-1 p.33 R25-1 p.31 R29-1 p.33 R30-1 p.36 R32-2 p.40 R33-1 p.40 R41-1 p.40 R43-1 p.43 R44-1 p.43 R66-1 p.31 R68-1 p.33 R70-1 p.43 R79-1 p.30 R80-1 p.32 R91-1 p.43 R116-1 p.43 R119-2 p.40 R123-1 p.40 R125-1 p.43 R126-1 p.40 R127-1 p.43 R131-2 p.40 R136-1 p.38 R139-1 p.40 R141-1 p.43 R142-1 p.40 R144-1 p.43 R147-1 p.43 R148-1 p.38 R149-1 p.43 R150-1 p.43 R151-1 p.40 R153-1 p.43 R155-1 p.38 R156-1 p.38 R162-1 p.38 R163-1 p.38 R165-1 p.40	R168-1 p.43 R169-1 p.38 R177-1 p.38 R183-1 p.43 R184-2 p.40 R186-1 p.43 R187-1 p.43 R188-1 p.43 R189-1 p.43 R190-1 p.40 R193-1 p.40 R196-1 p.40 R202-1 p.38 R205-1 p.40 R207-1 p.40 R209-1 p.43 R211-1 p.40 R213-1 p.40 R214-1 p.40 R218-2 p.40 R219-1 p.38 R221-1 p.38 R222-1 p.38 R223-1 p.40 R225-1 p.38 R226-1 p.38 R232-2 p.40 R233-1 p.38 R234-1 p.43 R235-1 p.38 R240-1 p.43 R242-1 p.43 R243-1 p.38 R244-1 p.38 R245-1 p.38 TP1-1 p.35 TP2-1 p.35 TP3-1 p.35 TP4-1 p.35 HIB ACTIVE L: E8-6 p.3 E9-2 p.5 E10-2 p.5 E12-3 p.5 E13-7 p.5 E51-7 p.23 E52-9 p.5 E53-7 p.5 E65-14 p.4 J1-50 p.35 HIB ACTIVE NXT L: E54-12 p.4 E65-11 p.4 HIB ADDR 00 H: C199-1 p.38 E14-10 p.6 J3-48 p.37 HIB ADDR 01 H: C196-1 p.38 E14-9 p.6 J3-52 p.37 HIB ADDR 02 H: C209-1 p.38 E14-8 p.6 J3-54 p.37 HIB ADDR 03 H: C200-1 p.38 E14-7 p.6 J3-56 p.37 HIB ADDR 04 H: C210-1 p.38 E14-6 p.6 J3-58 p.37 HIB ADDR 05 H: C197-1 p.38 E14-5 p.6 J3-60 p.37 HIB ADDR 06 H: C218-1 p.38 E14-4 p.6 J3-62 p.37 HIB ADDR 07 H: C217-1 p.38 E14-3 p.6 J3-66 p.37 HIB ADDR 08 H: C214-1 p.38 E14-2 p.6 J3-68 p.37 HIB ADDR 09 H: C148-1 p.38 E62-10 p.6 J3-51 p.37 HIB ADDR 10 H: C145-1 p.38 E62-9 p.6 J3-53 p.37 HIB ADDR 11 H: C152-1 p.38 E62-8 p.6 J3-55 p.37 HIB ADDR 12 H: C149-1 p.38 E62-7 p.6 J3-57 p.37 HIB ADDR 13 H: C153-1 p.38 E62-6 p.6 J3-59 p.37 HIB ADDR 14 H: C163-1 p.38 E62-5 p.6 J3-61 p.37 HIB ADDR 15 H: C135-1 p.38 E62-4 p.6 J3-63 p.37 HIB ADDR 16 H: C162-1 p.38 E62-3 p.6 J3-65 p.37 HIB ADDR 17 H: C146-1 p.38 E62-2 p.6 J3-67 p.37 HIB ADDR HPAR H: C193-1 p.38 E25-6 p.6 J3-69 p.37 HIB ADDR LATCH EN H: E13-12 p.5 E14-13 p.6 E62-13 p.6 E53-7 p.5 C177-1 p.38 E37-6 p.6 J3-71 p.37 HIB ADDR PH ERR L: E8-8 p.3 E25-5 p.6 HIB ADDR PL ERR L: E8-9 p.3 E37-5 p.6 HIB BM 0 L: E27-2 p.4 E34-10 p.4 J3-70 p.37 HIB ADDR 02 H: C209-1 p.38 E14-8 p.6 J3-54 p.37 HIB ADDR 03 H: C200-1 p.38 E14-7 p.6 J3-56 p.37 HIB ADDR 04 H: C210-1 p.38 E14-6 p.6 J3-58 p.37 HIB ADDR 05 H: C197-1 p.38 E14-5 p.6 J3-60 p.37 HIB ADDR 06 H: C218-1 p.38 E14-4 p.6 J3-62 p.37 HIB ADDR 07 H: C217-1 p.38 E14-3 p.6 J3-66 p.37 HIB ADDR 08 H: C214-1 p.38 E14-2 p.6 J3-68 p.37	C214-1 p.38 E14-2 p.6 J3-68 p.37 HIB ADDR 09 H: C148-1 p.38 E62-10 p.6 J3-51 p.37 HIB ADDR 10 H: C145-1 p.38 E62-9 p.6 J3-53 p.37 HIB ADDR 11 H: C152-1 p.38 E62-8 p.6 J3-55 p.37 HIB ADDR 12 H: C149-1 p.38 E62-7 p.6 J3-57 p.37 HIB ADDR 13 H: C153-1 p.38 E62-6 p.6 J3-59 p.37 HIB ADDR 14 H: C163-1 p.38 E62-5 p.6 J3-61 p.37 HIB ADDR 15 H: C135-1 p.38 E62-4 p.6 J3-63 p.37 HIB ADDR 16 H: C162-1 p.38 E62-3 p.6 J3-65 p.37 HIB ADDR 17 H: C146-1 p.38 E62-2 p.6 J3-67 p.37 HIB ADDR HPAR H: C193-1 p.38 E25-6 p.6 J3-69 p.37 HIB ADDR LATCH EN H: E13-12 p.5 E14-13 p.6 E62-13 p.6 E53-7 p.5 C177-1 p.38 E37-6 p.6 J3-71 p.37 HIB ADDR PH ERR L: E8-8 p.3 E25-5 p.6 HIB ADDR PL ERR L: E8-9 p.3 E37-5 p.6 HIB BM 0 L: E27-2 p.4 E34-10 p.4 J3-70 p.37 HIB ADDR 02 H: C209-1 p.38 E14-8 p.6 J3-54 p.37 HIB ADDR 03 H: C200-1 p.38 E14-7 p.6 J3-56 p.37 HIB ADDR 04 H: C210-1 p.38 E14-6 p.6 J3-58 p.37 HIB ADDR 05 H: C197-1 p.38 E14-5 p.6 J3-60 p.37 HIB ADDR 06 H: C218-1 p.38 E14-4 p.6 J3-62 p.37 HIB ADDR 07 H: C217-1 p.38 E14-3 p.6 J3-66 p.37 HIB ADDR 08 H: C214-1 p.38 E14-2 p.6 J3-68 p.37	HIB BUS ERR L: E8-16 p.3 J2-26 p.35 J3-77 p.37 HIB CSICA CS L: E67-4 p.3 J3-83 p.37 R142-2 p.40 R143-2 p.40 HIB CSICB CS L: E67-2 p.3 J3-82 p.37 R139-2 p.40 R140-2 p.40 HIB CTRL FEC H: E34-8 p.4 E90-19 p.15 HIB CTRL PAR H: E34-9 p.4 J3-87 p.37 R223-2 p.40 R224-2 p.40 HIB DATA 00 H: E116-22 p.7 J3-8 p.37 HIB DATA 01 H: E116-21 p.7 J3-10 p.37 HIB DATA 02 H: E116-20 p.7 J3-12 p.37 HIB DATA 03 H: E116-19 p.7 J3-16 p.37 HIB DATA 04 H: E116-18 p.7 J3-18 p.37 HIB DATA 05 H: E116-17 p.7 J3-20 p.37 HIB DATA 06 H: E116-16 p.7 J3-22 p.37 HIB DATA 07 H: E116-15 p.7 J3-26 p.37 HIB DATA 08 H: E113-22 p.7 J3-28 p.37 HIB DATA 09 H: E113-21 p.7 J3-41 p.37 HIB DATA P1 H: E133-23 p.7 J3-43 p.37 HIB DATA P2 H: E91-23 p.7 J3-45 p.37 HIB DATA P3 H: E75-23 p.7 J3-47 p.37 HIB FEC H: E52-8 p.5 E90-20 p.15 HIB FEC REG H: E23-8 p.7 E38-8 p.7 E49-5 p.7 E52-16 p.5 HIB FEC REG L: E7-8 p.7 E22-8 p.7 E49-6 p.7 HIB MSEL L: E27-7 p.4 E34-2 p.4 J3-86 p.37 R196-2 p.40 R197-2 p.40 HIB SISM CS L: E66-4 p.3 J3-98 p.37 R165-2 p.40 R166-2 p.40 HIB SPARE 73 H: E91-19 p.7 J3-15 p.37	HIB DATA1 PERR L: E23-5 p.7 E24-2 p.9 E52-6 p.5 HIB DATA 20 H: E13-18 p.5 E75-11 p.7 E91-11 p.7 E116-11 p.7 E133-11 p.7 HIB WR L: E27-6 p.4 E34-1 p.4 E139-D1 p.29 E166-D1 p.28 J3-81 p.37 R41-2 p.40 R42-2 p.40 HIB DATA 24 H: E75-22 p.7 J3-25 p.37 HIB DATA 25 H: E75-21 p.7 J3-27 p.37 HIB DATA 26 H: E75-20 p.7 J3-29 p.37 HIB DATA 27 H: E75-19 p.7 J3-31 p.37 HIB DATA 28 H: E75-18 p.7 J3-33 p.37 HIB DATA 29 H: E75-17 p.7 J3-35 p.37 HIB DATA2 PERR L: E7-5 p.7 E21-8 p.9 E52-5 p.5 HIB DATA 30 H: E75-16 p.7 J3-37 p.37 HIB DATA 31 H: E75-15 p.7 J3-39 p.37 HIB DATA3 PERR L: E38-5 p.7 E39-6 p.9 E52-4 p.5 HIB DATA P0 H: E116-23 p.7 J3-41 p.37 HIB DATA P1 H: E133-23 p.7 J3-43 p.37 HIB DATA P2 H: E91-23 p.7 J3-45 p.37 HIB DATA P3 H: E75-23 p.7 J3-47 p.37 HIB SPARE 75 H: E91-19 p.7 J3-15 p.37	J3-75 p.37 HIB SPARE 99 H: J3-99 p.37 HIB TO B2 OER L: E13-18 p.5 E75-11 p.7 E91-11 p.7 E116-11 p.7 E133-11 p.7 HIB WR L: E27-6 p.4 E34-1 p.4 E139-D1 p.29 E166-D1 p.28 J3-81 p.37 R41-2 p.40 R42-2 p.40 MANUAL DIAG CLK L: E68-4 p.3 E90-15 p.15 MEM0 CS0 L: E18-13 p.10 E19-11 p.10 E20-11 p.10 R216-2 p.5 MEM0 CS1 L: E15-11 p.10 E16-13 p.10 E17-11 p.10 R157-1 p.5 MEM0 CS2 L: E4-11 p.10 E5-13 p.10 E6-11 p.10 R238-2 p.5 MEM0 CS3 L: E1-13 p.10 E2-11 p.10 E3-11 p.10 R237-2 p.5 MEM0 PALCS0 L: E10-18 p.5 R216-1 p.5 MEM0 PALCS1 L: E10-17 p.5 R215-1 p.5 MEM0 PALCS2 L: E82-13 p.13 E83-11 p.13 E84-11 p.13 R129-2 p.5 MEM0 PALCS3 L: E10-15 p.5 R237-1 p.5 MEM1 CS0 L: E44-13 p.11 E45-11 p.11 E46-11 p.11 R179-2 p.5 MEM1 CS1 L: E41-11 p.11 E42-13 p.11 E43-11 p.11 R178-2 p.5 MEM1 CS2 L: E31-11 p.11 E32-13 p.11 E33-11 p.11 R200-2 p.5 MEM1 CS3 L: E28-13 p.11 E29-11 p.11 E30-11 p.11 R199-2 p.5 MEM1 PALCS0 L: E27-7 p.4 E34-2 p.4 J3-86 p.37 R196-2 p.40 R197-2 p.40 MEM1 PALCS2 L: E10-19 p.5 R200-1 p.5 R231-2 p.42 MEM1 PALCS3 L: E10-12 p.5 R199-1 p.5 MEM2 CS0 L: E72-13 p.12	E73-11 p.12 E74-11 p.12 R138-2 p.5 MEM2 CS1 L: E69-11 p.12 E70-13 p.12 E71-11 p.12 R137-2 p.5 MEM2 CS2 L: E59-11 p.12 E60-13 p.12 E61-11 p.12 R158-2 p.5 MEM2 CS3 L: E56-13 p.12 E57-11 p.12 E58-11 p.12 R157-2 p.5 MEM2 PALCS0 L: E9-1 p.5 E10-1 p.5 E13-17 p.5 E54-15 p.4 MEM2 PALCS1 L: E13-19 p.5 E19-11 p.5 E40-1 p.22 MEM2 PALCS2 L: E9-16 p.5 R158-1 p.5 MEM2 PALCS3 L: E9-15 p.5 R157-1 p.5 MEM3 CS0 L: E97-13 p.13 E98-11 p.13 E99-11 p.13 R122-2 p.5 MEM3 CS1 L: E94-11 p.13 E95-13 p.13 E96-11 p.13 R120-2 p.5 MEM3 CS2 L: E85-11 p.13 E86-13 p.13 E87-11 p.13 R130-2 p.5 MEM3 CS3 L: E82-13 p.13 E83-11 p.13 E84-11 p.13 R129-2 p.5 MEM3 PALCS0 L: E9-14 p.5 R122-1 p.5 MEM3 PALCS1 L: E9-13 p.5 R120-1 p.5 MEM3 PALCS2 L: E9-19 p.5 R130-1 p.5 MEM3 PALCS3 L: E9-12 p.5 R129-1 p.5 MEM BM0 L: E9-11 p.5 E10-11 p.5 E12-5 p.5 E21-10 p.8 E27-23 p.4 E35-22 p.24 E36-22 p.24 E116-1 p.7 R203-2 p.42 MEM BM1 L: E9-9 p.5 E10-9 p.5 E12-6 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E70-11 p.12 E71-13 p.12 E72-11 p.12 E73-13 p.12 E74-13 p.12 R167-2 p.5 MEM WE 3 L: E82-11 p.13 E83-13 p.13 E84-13 p.13 E85-13 p.13 E86-11 p.13 E87-13 p.13 E94-13 p.13 E95-11 p.13	E96-13 p.13 E97-11 p.13 E98-13 p.13 E99-13 p.13 R134-2 p.5 MSEL L: E9-6 p.5 E10-6 p.5 E12-4 p.5 E13-3 p.5 E27-18 p.4 E35-18 p.24 E36-18 p.24 E53-3 p.5 J2-33 p.35 R173-2 p.42 NC H: E27-14 p.4 E27-15 p.4 E27-16 p.4 E35-15 p.24 E35-16 p.24 E35-17 p.24 E36-15 p.24 E36-16 p.24 E36-17 p.24 E152-F1 p.29 E152-G2 p.29 E151-F1 p.28 E151-G2 p.28 E105-8 p.39 E105-11 p.39 E137-15 p.20 E138-15 p.17 E107-15 p.15 E78-15 p.15 E39-2 p.39 E2-13 p.10 E3-13 p.10 E4-13 p.10 E5-11 p.10 E6-13 p.10 E15-13 p.10 E39-5 p.39 E39-20 p.39 E104-1 p.39 E104-2 p.39 E104-3 p.39 E104-4 p.39 E104-5 p.39 E104-6 p.39 E104-7 p.39 E104-8 p.39 E104-9 p.39 E104-12 p.39 E104-13 p.39 E104-18 p.39 E104-19 p.39 E104-14 p.39 E104-15 p.39 E104-16 p.39 E104-17 p.39 E13-15 p.5 E53-12 p.5 E53-14 p.5 E53-15 p.5 E53-16 p.5 E53-17 p.5 E59-13 p.12 E58-13 p.12 E60-11 p.12 E61-13 p.12 E69-13 p.12 E70-11 p.12 E71-13 p.12 E72-11 p.12 E73-13 p.12 E74-13 p.12 R167-2 p.5 MEM WE 3 L: E82-11 p.13 E83-13 p.13 E84-13 p.13 E85-13 p.13 E86-11 p.13 E87-13 p.13 E94-13 p.13 E95-11 p.13	NO CONN D1 H: D_1-1 p.36 NO CONN D11 H: D_11-1 p.36 NO CONN D31 H: D_31-1 p.36 NO CONN D36 H: D_36-1 p.36 NO CONN D41 H: D_41-1 p.36 NO CONN D6 H: D_6-1 p.36 NO CONN E1 H: E_1-1 p.36 NO CONN E11 H: E_11-1 p.36 NO CONN E20 H: E_20-1 p.36 NO CONN E21 H: E_21-1 p.36 NO CONN E22 H: E_22-1 p.36 NO CONN E23 H: E_23-1 p.36 NO CONN E24 H: E_24-1 p.36 NO CONN E25 H: E_25-1 p.36 NO CONN E30 H: E_30-1 p.36 NO CONN E31 H: E_31-1 p.36 NO CONN E36 H: E_36-1 p.36 NO CONN E41 H: E_41-1 p.36 NO CONN E50 H: E_50-1 p.36 NO CONN E51 H: E_51-1 p.36 NO CONN E52 H: E_52-1 p.36 NO CONN E53 H: E_53-1 p.36 NO CONN E54 H: E_54-1 p.36 NO CONN E55 H: E_55-1 p.36 NO CONN E6 H: E_6-1 p.36 NO CONN E60 H: E_60-1 p.36 NXT ADR A 0 H: E76-7 p.18 E102-18 p.16 E149-3 p.17 E164-9 p.17 NXT ADR A 1 H: E76-5 p.18 E102-17 p.16 E149-4 p.17 E164-10 p.17 NXT ADR A 10 H: E76-9 p.18 E138-5 p.17 E143-16 p.16 E162-11 p.17 NXT ADR A 2 H: E76-3 p.18 E102-16 p.16 E149-5 p.17 E164-11 p.17 NXT ADR A 3 H: E76-2 p.18 E102-15 p.16 E149-6 p.17 E164-13 p.17 NXT ADR A 4 H: E88-11 p.18 E102-14 p.16 E141-3 p.17 E164-14 p.17 NXT ADR A 5 H: E88-10 p.18 E102-13 p.16 E141-4 p.17
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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**CROSS REFERENCE:**  
Signal Names



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE:
CHK'D:	DATE	BOARD LOCATION: CXO		<b>WILDCAT BOARD 2</b>
		SHEET 73		
		NEXT HIGHER ASSEMBLY:		
FIRST USED ON OPTION/MODEL:				

SIZE	CODE	NUMBER	REV
K	CS	-	25OCT88



Output Sources for nets listed in cross-reference available upon request

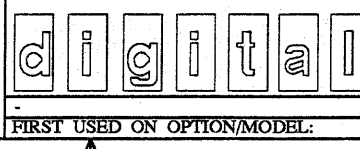
Output Source Key: o> general output t> tristate output b> bidirectional output

REG REM PREPORT EN B L: E64-12 p.24 E65-18 p.21 E166-J2 p.28	R183-2 p.43 RGND20 L: E13-11 p.5 E53-11 p.5 R242-2 p.43 RGND21 L: E104-11 p.39 R116-2 p.43 RGND23 L: E160-18 p.17 E161-18 p.17 E162-18 p.17 E163-18 p.17 E164-18 p.17 R43-2 p.43 RGND24 L: E144-18 p.20 E145-18 p.20 E146-18 p.20 E147-18 p.20 E148-18 p.20 R70-2 p.43 RGND2 L: E78-2 p.15 E78-23 p.15 E90-2 p.15 E90-23 p.15 E106-2 p.15 E106-23 p.15 E107-2 p.15 E107-23 p.15 R127-2 p.43 RGND3 L: E152-J13 p.29 R91-2 p.43 RGND4 L: E65-1 p.4 E66-1 p.3 E76-1 p.4 E77-1 p.8 E81-1 p.8 E88-1 p.8 R125-2 p.43 RGND5 L: E63-6 p.24 E153-2 p.43 RGND6 L: E55-4 p.24 R168-2 p.43 RGND7 L: E79-6 p.24 R141-2 p.43 RGND8 L: E64-4 p.24 R150-2 p.43 RGND9 L: E35-6 p.24 E35-7 p.24 E35-8 p.24 E35-9 p.24 E35-10 p.24 R187-2 p.43 SIA INTRPT L: E67-12 p.3 J3-88 p.37 SIB INTRPT L: E27-10 p.4 E27-11 p.4 R209-2 p.43 RGND14 L: E67-1 p.3 E67-19 p.25 R144-2 p.43 RGND15 L: E166-G3 p.28 R44-2 p.43 RGND16 L: E51-6 p.23 R149-2 p.43 RGND17 L: E47-11 p.23 R186-2 p.43 RGND18 L: E11-11 p.23 R240-2 p.43 RGND19 L: E52-11 p.5	SIC A NXT GRANT L: E47-3 p.23 E54-2 p.4 E66-3 p.4 E166-E2 p.28 J3-93 p.37 SIC A OPCODE REQ L: E55-11 p.24 E81-23 p.18 SIC A POST BUS GRANT L: E8-13 p.3 E65-15 p.4 SIC A RESET L: E35-11 p.24 E50-9 p.23 E103-11 p.22 E107-16 p.15 E166-L2 p.28 SIC B BUS GRANT L: E11-2 p.23 E24-6 p.8 E36-1 p.24 E51-3 p.23 E65-9 p.4 E66-20 p.4 E93-1 p.25 E108-1 p.25 J1-5 p.35 SIC B BUS REQ IN L: E11-4 p.23 E36-14 p.24 E76-21 p.21 SIC B BUS REQ L: E11-19 p.23 J2-24 p.35 J3-92 p.37 SIC B NXT GRANT L: E11-3 p.23 E54-1 p.4 E66-5 p.4 E139-E2 p.29 J3-91 p.37 SIC B OPCODE REQ L: E64-11 p.24 E65-19 p.21 SIC B POST BUS GRANT L: E8-12 p.3 E65-16 p.4 R168-2 p.43 RGND7 L: E79-6 p.24 R141-2 p.43 RGND8 L: E64-4 p.24 R150-2 p.43 RGND9 L: E35-6 p.24 E35-7 p.24 E35-8 p.24 E35-9 p.24 E35-10 p.24 R187-2 p.43 SIA INTRPT L: E67-12 p.3 J3-88 p.37 SIB INTRPT L: E27-10 p.4 E27-11 p.4 R209-2 p.43 RGND14 L: E67-1 p.3 E67-19 p.25 R144-2 p.43 RGND15 L: E166-G3 p.28 R44-2 p.43 RGND16 L: E51-6 p.23 R149-2 p.43 RGND17 L: E47-11 p.23 R186-2 p.43 RGND18 L: E11-11 p.23 R240-2 p.43 RGND19 L: E52-11 p.5	SIECL B SHIFT REG OUT H: E89-5 p.14 E152-F2 p.29 SIECL B SH REG CLK EN H: E52-13 p.5 E106-18 p.15 SIECL SHIFT REG IN H: E106-22 p.15 E151-E1 p.28 E152-E1 p.29 SISM A BMASK L: E35-3 p.24 E35-4 p.24 E35-5 p.24 E81-16 p.18 SISM A BUS ERR H: E8-15 p.3 E103-8 p.22 SISMA CNTR CO H: E141-10 p.17 E149-15 p.17 SISMA CNTR1 CO H: E138-10 p.17 E141-15 p.17 SISM A CNTR CLR L: E47-8 p.23 E103-18 p.22 E138-1 p.17 E141-1 p.17 E149-1 p.17 SISM A CNTR EN H: E76-11 p.22 E103-15 p.22 SISM A CNTR LD L: E103-17 p.22 E138-9 p.17 E141-9 p.17 E149-9 p.17 SISM A CRAM TEST H: E47-6 p.23 E103-7 p.22 E107-17 p.15 SISM ADR A 00 H: E132-2 p.14 E163-22 p.17 E164-22 p.17 J1-36 p.35 SISM ADR A 10 H: E111-2 p.14 E138-12 p.17 E160-19 p.17 E161-19 p.17 E162-19 p.17 E163-19 p.17 E164-19 p.17 J1-38 p.35 SISM ADR B 00 H: E111-3 p.14 E130-11 p.20 E144-8 p.20 E145-8 p.20 E146-8 p.20 E147-8 p.20 E148-8 p.20 J2-46 p.35 SISM ADR B 01 H: E111-4 p.14 E130-8 p.20 E148-21 p.22 E144-7 p.20 E145-7 p.20 E146-7 p.20 E147-7 p.20 E148-7 p.20 J2-45 p.35 SISM ADR B 02 H: E111-5 p.14 E130-6 p.20 E144-6 p.20 E145-6 p.20 E146-6 p.20 E147-6 p.20 E148-6 p.20 J2-29 p.35 SISM ADR B 03 H: E111-6 p.14 E131-11 p.20 E144-5 p.20	J1-35 p.35 SISM ADR A 05 H: E132-7 p.14 E141-13 p.17 E160-3 p.17 E161-3 p.17 E162-3 p.17 E163-3 p.17 E164-3 p.17 J1-46 p.35 SISM ADR A 06 H: E132-8 p.14 E141-12 p.17 E160-2 p.17 E161-2 p.17 E162-2 p.17 E163-2 p.17 E164-2 p.17 J1-34 p.35 SISM ADR A 07 H: E132-9 p.14 E141-11 p.17 E160-1 p.17 E161-1 p.17 E162-1 p.17 E163-1 p.17 E164-1 p.17 J1-43 p.35 SISM ADR A 08 H: E132-10 p.14 E138-14 p.17 E160-23 p.17 E161-23 p.17 E162-23 p.17 E163-23 p.17 E164-23 p.17 J1-48 p.35 SISM ADR A 09 H: E132-11 p.14 E148-1 p.20 E146-1 p.20 E147-1 p.20 E148-1 p.20 J2-38 p.35 SISM ADR B 08 H: E111-11 p.14 E137-14 p.20 E144-23 p.20 E145-23 p.20 E146-23 p.20 E147-23 p.20 E148-23 p.20 J2-37 p.35 SISM ADR B 09 H: E89-2 p.14 E137-13 p.20 E144-22 p.20 E145-22 p.20 E146-22 p.20 E147-22 p.20 E148-22 p.20 J2-25 p.35 SISM ADR B 10 H: E89-3 p.14 E137-12 p.20 E144-19 p.20 E145-19 p.20 E146-19 p.20 E147-19 p.20 E148-19 p.20 J1-45 p.35 SISM A EN H: E103-9 p.22 E103-9 p.22 SISM A PARIITY ERR H: E55-5 p.24 E77-9 p.24 SISM A PERR FDBCK1 L: E55-3 p.24 E89-6 p.14 E103-16 p.22 SISM A RAM WR EN HI L: E103-19 p.22 E163-21 p.17 J2-29 p.35 SISM A RAM WR EN LO L: E103-12 p.22 E160-21 p.17 E161-21 p.17 E162-21 p.17	E145-5 p.20 E146-5 p.20 E147-5 p.20 E148-5 p.20 J2-30 p.35 SISM ADR B 04 H: E111-7 p.14 E126-14 p.20 E144-4 p.20 E145-4 p.20 E146-4 p.20 E147-4 p.20 E148-4 p.20 J2-39 p.35 SISM ADR B 05 H: E111-8 p.14 E126-13 p.20 E144-3 p.20 E145-3 p.20 E146-3 p.20 E147-3 p.20 E148-3 p.20 J2-23 p.35 SISM ADR B 06 H: E111-9 p.14 E126-12 p.20 E144-2 p.20 E145-2 p.20 E146-2 p.20 E147-2 p.20 E148-2 p.20 J2-36 p.35 SISM ADR B 07 H: E111-10 p.14 E126-11 p.20 E144-1 p.20 E145-1 p.20 E146-1 p.20 E147-1 p.20 E148-1 p.20 J2-38 p.35 SISM ADR B 08 H: E111-11 p.14 E137-14 p.20 E144-23 p.20 E145-23 p.20 E146-23 p.20 E147-23 p.20 E148-23 p.20 J2-37 p.35 SISM ADR B 09 H: E89-2 p.14 E137-13 p.20 E144-22 p.20 E145-22 p.20 E146-22 p.20 E147-22 p.20 E148-22 p.20 J2-25 p.35 SISM ADR B 10 H: E89-3 p.14 E137-12 p.20 E144-19 p.20 E145-19 p.20 E146-19 p.20 E147-19 p.20 E148-19 p.20 J1-45 p.35 SISM A EN H: E103-9 p.22 E103-9 p.22 SISM A PARIITY ERR H: E55-5 p.24 E77-9 p.24 SISM A PERR FDBCK1 L: E55-3 p.24 E89-6 p.14 E103-16 p.22 SISM A RAM WR EN HI L: E103-19 p.22 E163-21 p.17 J2-29 p.35 SISM A RAM WR EN LO L: E103-12 p.22 E160-21 p.17 E161-21 p.17 E162-21 p.17	E164-21 p.17 SISM A RD EN L: E78-19 p.16 E92-1 p.16 E102-1 p.16 E103-4 p.22 E110-1 p.16 E129-1 p.16 E143-1 p.16 E160-20 p.17 E161-20 p.17 E162-20 p.17 E163-20 p.17 E164-20 p.17 SISM A RD REQ H: E35-2 p.24 E81-18 p.18 SISM A REG CNTR EN H: E76-14 p.22 E138-7 p.17 E141-7 p.17 E149-7 p.17 SISM B BMASK L: E36-3 p.24 E36-4 p.24 E36-5 p.24 E88-22 p.21 SISM B BUS ERR H: E8-14 p.3 E40-8 p.22 SISMB CNTR CO H: E126-10 p.20 E131-15 p.20 SISMB CNTR1 CO H: E126-15 p.20 E137-10 p.20 SISM B CNTR CLR L: E11-8 p.23 E140-18 p.22 E126-1 p.20 E131-1 p.20 E137-1 p.20 SISM B CNTR EN H: E81-3 p.18 E110-18 p.16 E163-9 p.17 SISM B CNTR LD L: E140-17 p.22 E126-9 p.20 E131-9 p.20 E137-9 p.20 SISM B CRAM TEST H: E11-6 p.23 E76-10 p.21 E106-16 p.15 SISM B EN H: E40-9 p.22 E106-17 p.15 SISM B PARIITY ERR H: E65-2 p.21 E139-M13 p.29 E144-17 p.20 SISM B PERR FDBCK1 L: E64-3 p.24 E89-7 p.14 SISM B RAM WR EN HI L: E40-19 p.22 E148-21 p.22 E144-7 p.20 E145-7 p.20 E146-7 p.20 E147-7 p.20 E148-7 p.20 SISM B RD EN L: E40-4 p.22 E78-18 p.15 E80-1 p.19 E113-1 p.19 E115-1 p.19 E117-1 p.19 E123-1 p.19 E144-20 p.20 E145-20 p.20 E146-20 p.20 E147-20 p.20 E148-20 p.20	SISM B RD REQ H: E36-2 p.24 E76-19 p.21 SISM B REG CNTR EN H: E65-22 p.22 E126-7 p.20 E131-7 p.20 E137-7 p.20 SISM CODE WR RD EN H: E40-5 p.22 E78-17 p.15 E103-5 p.22 SISM REG CS L: E12-15 p.5 E13-9 p.5 E40-3 p.22 E53-9 p.5 E66-21 p.3 E103-3 p.22 SYSCLK H: C119-1 p.40 E100-1 p.3 J3-2 p.37 R126-2 p.40 R132-2 p.40 TMUX A SEL 0 H: E81-6 p.18 E92-13 p.16 E160-15 p.17 E166-L12 p.28 TMUX A SEL 1 H: E81-5 p.18 E92-12 p.16 E160-16 p.17 E166-N14 p.28 TMUX A SEL 2 H: E80-11 p.19 E81-4 p.18 E92-11 p.16 E160-17 p.17 E166-M13 p.28 TMUX A SEL 3 H: E81-3 p.18 E110-18 p.16 E163-9 p.17 E166-P14 p.28 TMUX B SEL 0 H: E76-8 p.21 E80-13 p.19 E139-L12 p.29 E144-15 p.20 TMUX B SEL 1 H: E76-10 p.21 E80-12 p.19 E139-N14 p.29 E144-16 p.20 TMUX B SEL 2 H: E65-2 p.21 E139-M13 p.29 E144-17 p.20 TMUX B SEL 3 H: E65-4 p.21 E117-18 p.19 E139-P14 p.29 E148-9 p.20 TRANS A HI EN L: E103-14 p.22 E110-19 p.16 TRANS A LO EN L: E92-19 p.16 E102-19 p.16 E103-13 p.22 E129-19 p.16 E143-19 p.16 TRANS B HI EN L: E40-14 p.22 E117-19 p.19 E115-19 p.19 E123-19 p.19 E145-19 p.19 E146-19 p.19 E147-19 p.19 E148-19 p.19 TRANS B LO EN L: E40-13 p.22 E80-19 p.19 E113-19 p.19 E115-19 p.19 E123-19 p.19 E145-19 p.19 E146-19 p.19 E147-19 p.19 E148-19 p.19 USER D17 H: D 17-1 p.36 USER D18 H: D 18-1 p.36 USER D19 H: D 19-1 p.36 USER D20 H: D 20-1 p.36 USER D21 H: D 21-1 p.36 USER D22 H: D 22-1 p.36 USER D23 H: D 23-1 p.36 USER D24 H: D 24-1 p.36 USER D25 H: D 25-1 p.36 USER D26 H: D 26-1 p.36 USER D27 H: D 27-1 p.36 USER D28 H: D 28-1 p.36 USER D29 H: D 29-1 p.36 USER D30 H: D 30-1 p.36 USER D47 H: D 47-1 p.36 USER D48 H: D 48-1 p.36 USER D49 H: D 49-1 p.36 USER D50 H: D 50-1 p.36 USER D51 H: D 51-1 p.36 USER D52 H: D 52-1 p.36 USER D53 H: D 53-1 p.36 USER D54 H: D 54-1 p.36 USER D55 H: D 55-1 p.36 USER D56 H: D 56-1 p.36 USER D57 H: D 57-1 p.36 USER D58 H: D 58-1 p.36 USER D59 H: D 59-1 p.36 USER D60 H: D 60-1 p.36 VCC H: B 3-1 p.36 B 13-1 p.36 B 18-1 p.36 B 19-1 p.36 B 28-1 p.36 B 29-1 p.36 B 33-1 p.36 B 34-1 p.36 B 48-1 p.36 C1-1 p.36 C2-1 p.36 C3-1 p.36 C4-1 p.36 C5-1 p.36 C6-1 p.36 C7-1 p.36 C8-1 p.36 C9-1 p.36 C10-1 p.36 C11-1 p.36 C12-1 p.36 C13-1 p.36 C14-1 p.36 C15-1 p.36 C16-1 p.36 C17-1 p.36 C18-1 p.36 C19-1 p.36 C20-1 p.36 C21-1 p.36 C22-1 p.36 C23-1 p.36 C37-1 p.44 C38-1 p.34 C40-1 p.44 C41-1 p.44 C42-1 p.44 C43-1 p.44 C44-1 p.44 C45-1 p.44 C46-1 p.34 C48-1 p.44 C50-1 p.44 C51-1 p.34 C52-1 p.34 C54-1 p.34 C55-1 p.34 C56-1 p.44 C58-1 p.44 C59-1 p.44 C60-1 p.44 C61-1 p.44 C62-1 p.44 C64-1 p.34 C65-1 p.44 C66-1 p.44 C67-1 p.44 C69-1 p.34 C70-1 p.44 C71-1 p.44 C83-1 p.44 C84-1 p.44 C85-1 p.44 C86-1 p.44 C87-1 p.44 C89-1 p.44 C90-1 p.44 C92-1 p.44 C94-1 p.44 C95-1 p.44 C96-1 p.44 C98-1 p.44 C99-1 p.44 C100-1 p.44 C101-1 p.44 C102-1 p.44 C103-1 p.44 C104-1 p.44 C105-1 p.44 C106-1 p.44 C107-1 p.44 C108-1 p.44 C109-1 p.36 C110-1 p.45 C111-1 p.45 C112-1 p.45 C113-1 p.45 C114-1 p.45 C115-1 p.45 C116-1 p.44 C117-1 p.36 C118-1 p.44 C120-1 p.36 C121-1 p.44 C122-1 p.44 C123-1 p.36 C124-1 p.45 C125-1 p.45 C126-1 p.45 C127-1 p.45 C128-1 p.45 C129-1 p.45 C130-1 p.44 C131-1 p.44 C132-1 p.44 C133-1 p.44 C134-1 p.44 C136-1 p.44 C137-1 p.44 C138-1 p.44 C139-1 p.45 C140-1 p.45 C141-1 p.45 C142-1 p.45 C143-1 p.45 C144-1 p.45 C147-1 p.44 C150-1 p.44
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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]  
**CROSS REFERENCE:**  
Signal Names



DRN: T. Nerger	DATE	ENG: T. Nerger	DATE	TITLE: WILDCAT BOARD 2
CHK'D:	DATE	BOARD LOCATION: CXO	SHEET: 75	SIZE: K
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY:		NUMBER
Tue Oct 25 16:48:32 1988				REV: 25OCT88

SIZE: K	CODE: CS	NUMBER	REV: 25OCT88
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Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

C151-1 p.44	E158-3 p.33	b>E64-6 p.24	E79-3 p.24	A_11-1 p.36	C_55-1 p.36
C154-1 p.44	E159-2 p.33	R161-2 p.41	R135-2 p.41	XMI D2 L:	XMI DEFAULT H:
C155-1 p.44	E159-3 p.33	VCCR11 H:	VCCR8 H:	A_7-1 p.36	C_54-1 p.36
C156-1 p.45	R4-1 p.34	E149-10 p.17	E14-14 p.6	XMI D30 L:	XMI F0 L:
C157-1 p.45	R5-1 p.34	R71-2 p.41	R236-2 p.41	A_45-1 p.36	C_12-1 p.36
C158-1 p.45	R6-1 p.34	VCCR12 H:	VCCR9 H:	XMI D31 L:	XMI F1 L:
C159-1 p.45	R7-1 p.34	E131-10 p.20	b>E55-6 p.24	A_14-1 p.36	C_11-1 p.36
C160-1 p.45	R26-1 p.34	R93-2 p.41	R175-2 p.41	XMI D32 L:	XMI F2 L:
C161-1 p.45	R27-1 p.34	VCCR13 H:	VEB H:	A_25-1 p.36	C_26-1 p.36
C164-1 p.44	R31-1 p.41	E14-11 p.6	B_43-1 p.36	XMI D33 L:	XMI F3 L:
C165-1 p.44	R40-1 p.40	R198-2 p.41	B_44-1 p.36	A_26-1 p.36	C_25-1 p.36
C166-1 p.44	R42-1 p.40	VCCR14 H:	B_58-1 p.36	XMI D34 L:	XMI FAULT L:
C167-1 p.44	R45-1 p.42	E151-J13 p.28	XCVR CLK H:	A_27-1 p.36	A_10-1 p.36
C169-1 p.44	R58-1 p.41	R90-2 p.41	E13-16 p.5	XMI D35 L:	XMI GRANT L:
C170-1 p.45	R59-1 p.41	VCCR15 H:	E51-9 p.23	A_30-1 p.36	C_42-1 p.36
C171-1 p.45	R64-1 p.34	E47-9 p.23	XI GRANT L:	XMI D36 L:	XMI HOLD L:
C172-1 p.45	R67-1 p.34	R176-2 p.41	E24-4 p.8	A_59-1 p.36	C_5-1 p.36
C173-1 p.45	R69-1 p.41	VCCR16 H:	E66-23 p.4	XMI D37 L:	XMI ID0 L:
C174-1 p.45	R71-1 p.41	E21-11 p.8	J2-50 p.35	B_53-1 p.36	C_24-1 p.36
C175-1 p.45	R75-1 p.41	E24-11 p.8	XI NXT GRANT L:	XMI D38 L:	XMI ID1 L:
C176-1 p.44	R76-1 p.41	E26-11 p.8	E54-3 p.4	B_16-1 p.36	C_23-1 p.36
C178-1 p.44	R81-1 p.41	E34-4 p.4	E66-2 p.4	XMI D39 L:	XMI ID2 L:
C179-1 p.44	R85-1 p.41	E39-11 p.8	J3-95 p.37	B_20-1 p.36	C_22-1 p.36
C180-1 p.44	R86-1 p.42	R194-2 p.41	XMI AC LO L:	XMI D3 L:	XMI ID3 L:
C181-1 p.44	R87-1 p.41	VCCR17 H:	C_16-1 p.36	A_9-1 p.36	C_21-1 p.36
C182-1 p.44	R90-1 p.41	E54-6 p.4	XMI BAD L:	XMI D40 L:	XMI ID4 L:
C183-1 p.44	R92-1 p.41	B_174-2 p.41	B_37-1 p.36	B_31-1 p.36	C_20-1 p.36
C184-1 p.44	R93-1 p.41	VCCR18 H:	XMI BOOT EN L:	XMI D41 L:	XMI ID5 L:
C185-1 p.45	R94-1 p.41	b>E12-18 p.5	B_40-1 p.36	B_17-1 p.36	C_2-1 p.36
C186-1 p.45	R114-1 p.41	R241-2 p.41	XMI CMD REQ L:	XMI D42 L:	XMI LOCKOUT L:
C187-1 p.45	R115-1 p.41	VCCR19 H:	C_38-1 p.36	B_49-1 p.36	B_59-1 p.36
C188-1 p.45	R121-1 p.41	E62-11 p.6	XMI CNFO L:	XMI D43 L:	XMI NODEID0 H:
C189-1 p.45	R124-1 p.40	R128-2 p.41	C_47-1 p.36	C_31-1 p.36	C_6-1 p.36
C190-1 p.45	R128-1 p.41	VCCR2 H:	XMI CNF1 L:	XMI D44 L:	XMI NODEID1 H:
C191-1 p.44	R132-1 p.40	b>E34-6 p.4	C_49-1 p.36	B_45-1 p.36	C_7-1 p.36
C192-1 p.44	R133-1 p.41	R195-2 p.41	XMI CNF2 L:	XMI D45 L:	XMI NODEID2 H:
C194-1 p.44	R135-1 p.41	VCCR20 H:	C_35-1 p.36	B_15-1 p.36	C_8-1 p.36
C198-1 p.44	R140-1 p.40	E55-10 p.24	XMI CON RCV H:	XMI D46 L:	XMI NODEID3 H:
C201-1 p.45	R143-1 p.40	R159-2 p.41	A_49-1 p.36	B_14-1 p.36	C_9-1 p.36
C202-1 p.45	R145-1 p.41	VCCR21 H:	XMI CON SECURE L:	XMI D47 L:	XMI P0 L:
C203-1 p.45	R146-1 p.41	E64-10 p.24	A_60-1 p.36	B_12-1 p.36	A_12-1 p.36
C204-1 p.45	R152-1 p.40	R154-2 p.41	XMI CON XMIT H:	XMI D48 L:	XMI P1 L:
C205-1 p.45	R154-1 p.41	VCCR22 H:	A_52-1 p.36	B_11-1 p.36	B_55-1 p.36
C206-1 p.45	R159-1 p.41	E139-G3 p.29	XMI D0 L:	XMI D49 L:	XMI P2 L:
C207-1 p.44	R160-1 p.41	R85-2 p.41	A_41-1 p.36	B_10-1 p.36	C_17-1 p.36
C211-1 p.44	R161-1 p.41	VCCR23 H:	XMI D10 L:	XMI D4 L:	XMI PHASE L:
C212-1 p.44	R164-1 p.41	E78-14 p.15	A_47-1 p.36	A_6-1 p.36	C_45-1 p.36
C213-1 p.44	R166-1 p.40	E90-14 p.15	XMI D11 L:	XMI D50 L:	XMI RESET L:
C215-1 p.44	R170-1 p.42	E106-14 p.15	A_57-1 p.36	B_9-1 p.36	A_55-1 p.36
C216-1 p.44	R171-1 p.42	E107-14 p.15	XMI D12 L:	XMI D51 L:	XMI RES REQ L:
C219-1 p.45	R172-1 p.41	R146-2 p.41	A_50-1 p.36	B_8-1 p.36	C_40-1 p.36
C220-1 p.45	R173-1 p.42	VCCR24 H:	XMI D13 L:	XMI D52 L:	XMI RUN L:
C221-1 p.45	R174-1 p.41	b>E50-16 p.23	A_16-1 p.36	B_7-1 p.36	A_54-1 p.36
C222-1 p.45	R175-1 p.41	b>E50-17 p.23	XMI D14 L:	XMI D53 L:	XMI SPARE0 L:
C223-1 p.45	R176-1 p.41	b>E50-18 p.23	A_17-1 p.36	B_6-1 p.36	B_47-1 p.36
C224-1 p.45	R180-1 p.42	R181-2 p.41	XMI D15 L:	XMI D54 L:	XMI SPAREBIT0 L:
D1-2 p.36	R181-1 p.41	VCCR25 H:	A_24-1 p.36	B_38-1 p.36	C_46-1 p.36
E112-2 p.30	R182-1 p.42	R172-2 p.41	XMI D16 L:	XMI D55 L:	XMI SPAREBIT1 L:
E112-3 p.30	R185-1 p.41	VCCR26 H:	A_53-1 p.36	B_22-1 p.36	C_50-1 p.36
E118-2 p.30	R191-1 p.40	E100-5 p.39	XMI D17 L:	XMI D56 L:	XMI SPAREBIT2 L:
E118-3 p.30	R192-1 p.40	E100-9 p.39	A_23-1 p.36	B_23-1 p.36	A_35-1 p.36
E119-2 p.32	R194-1 p.41	E105-9 p.39	XMI D18 L:	XMI D57 L:	XMI SPAREBIT3 L:
E119-3 p.32	R195-1 p.41	A_105-10 p.39	A_38-1 p.36	B_24-1 p.36	A_37-1 p.36
E120-2 p.32	R197-1 p.40	E105-12 p.39	XMI D19 L:	XMI D58 L:	XMI SPAREBIT4 L:
E120-3 p.32	R198-1 p.41	E105-13 p.39	A_20-1 p.36	B_21-1 p.36	A_39-1 p.36
E121-2 p.32	R201-1 p.41	R121-2 p.41	XMI D1 L:	XMI D59 L:	XMI SUP L:
E121-3 p.32	R203-1 p.42	VCCR27 H:	A_51-1 p.36	B_25-1 p.36	A_31-1 p.36
E122-2 p.32	R204-1 p.42	E25-3 p.6	XMI D20 L:	XMI D5 L:	XMI TIME H:
E122-3 p.32	R206-1 p.40	E37-3 p.6	A_21-1 p.36	A_5-1 p.36	C_59-1 p.36
E127-2 p.30	R208-1 p.40	R185-2 p.41	XMI D21 L:	XMI D60 L:	XMI TIME L:
E127-3 p.30	R212-1 p.40	VCCR3 H:	A_22-1 p.36	B_57-1 p.36	C_57-1 p.36
E134-2 p.30	R217-1 p.40	E8-5 p.3	XMI D22 L:	XMI D61 L:	XMI TOY BBU OK H:
E134-3 p.30	R220-1 p.40	R239-2 p.41	B_5-1 p.36	B_26-1 p.36	A_46-1 p.36
E142-2 p.31	R224-1 p.40	VCCR4 H:	XMI D23 L:	XMI D62 L:	XMI TOY BBU PWR H:
E142-3 p.31	R228-1 p.41	E93-11 p.25	B_4-1 p.36	B_27-1 p.36	A_42-1 p.36
E150-2 p.31	R229-1 p.42	E101-11 p.25	XMI D24 L:	XMI D63 L:	XMI UPDATE EN H:
E150-3 p.31	R230-1 p.42	E108-11 p.25	B_2-1 p.36	B_30-1 p.36	B_41-1 p.36
E154-2 p.31	R231-1 p.42	E125-11 p.25	XMI D25 L:	XMI D6 L:	YELLOW LED ON H:
E154-3 p.31	R236-1 p.41	R94-2 p.41	B_1-1 p.36	A_8-1 p.36	E49-1 p.15
E155-2 p.31	R239-1 p.41	VCCR5 H:	XMI D26 L:	XMI D7 L:	o>E78-16 p.15
E155-3 p.31	R241-1 p.41	E63-3 p.24	B_35-1 p.36	A_4-1 p.36	YELLOW LED ON L:
E156-2 p.33	VCCR1 H:	R160-2 p.41	XMI D27 L:	XMI D8 L:	o>E49-2 p.15
E156-3 p.33	E13-8 p.5	VCCR6 H:	B_46-1 p.36	A_2-1 p.36	R1-1 p.36
E157-2 p.33	E53-8 p.5	E62-14 p.6	XMI D28 L:	XMI D9 L:	
E157-3 p.33	R164-2 p.41	R133-2 p.41	A_15-1 p.36	A_1-1 p.36	
E158-2 p.33	VCCR10 H:	VCCR7 H:	XMI D29 L:	XMI DC LO L:	

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CHK'D:		DATE	BOARD LOCATION:	CXO		WILDCAT BOARD 2
			SHEET	76		
			NEXT HIGHER ASSEMBLY:			

SIZE	CODE	NUMBER	REV
K	CS	-	25OCT88

