DataGeneral

Technical Manual

6045 SERIES CARTRIDGE DISC SUBSYSTEM

015-000057-02

Technical Manual

6045 SERIES CARTRIDGE DISC SUBSYSTEM

015-000057-02

NOTICE

Ordering No. 015-000057-02

Printed in the United States of America
Rev. 02, November 1977

6045 SERIES CARTRIDGE DISC SUBSYSTEM

Data General

PREFACE

This manual introduces the 6045 series 10 Mbyte cartridge disc subsystem. The manual is designed to give you a general idea of what the subsystem does and how it does it. It is not a repair manual, but enough information is provided here to help you feel comfortable with the schematics and programs. You may wish to supplement your reading with either the programmers reference manual for peripherals *(DGC no. 015-000021)* or the field service manual for the disc units used in this subsystem *(DGC no. 015-000058)*.

The contents of this manual are organized so that the information can reach a wide variety of readers. The first chapter introduces the subsystem. The next three chapters provide an overview of the controller, interface, and drive. The remaining six chapters present the controller, interface, and drive in much greater detail. The appendices further supplement the details given in the manual. Each chapter introduces its contents in a general way, and then proceeds to elaborate on the introduction.

Depending on individual needs, a reader can use this manual in a number of different ways. A system designer might read only the first chapter, while a maintainer might read the first four overview chapters and skim the introductions to the remaining chapters, leaving the body of the detailed chapters for later reference.

An understanding of the organization of this manual will help you to obtain the information you require, according to your particular needs. It will prevent you from dealing with material that is of no use to you or that is redundant.

PART I

Chapter 1, Subsystem Overview - Introduces the cartridge disc subsystem and presents its physical limits and capabilities.

Chapter 2, Controller Overview - Describes the general properties of the controller, and includes a programming summary.

Chapter 3, Interface Overview - Describes the general aspects of the bus buffering and dual processor access capabilities of the controller/drive interface.

Chapter 4, Drive Overview - Introduces the major subassemblies contained within the drive, shows where they are, and briefly tells what they do.

PART II

Chapter 5, Controller - Describes in detail the functional properties of the controller. Includes a close look at the format of sectors.

Chapter 6, Interface - Gives a more detailed look at the interface, with special emphasis on interface functions in a dual processor system.

Chapter 7, Drive: Spindle and Monitors - Describes the circuits that power the spindle and brush motors, monitor spindle speed, and detect and count sectors.

Chapter 8, Drive: Head Positoner and Servo - Describes the circuits that move the heads to selected tracks, detent on a track, and compensate for temperature variations which would otherwise cause position errors.

Chapter 9, Drive: Data Transcription - Explains the data encoding scheme and describes the data transcription mechanism.

Chapter 10, Drive: Power Supply - Describes the power supply and distribution circuits that power the positioner, spindle, brushes, and drive circuits.

APPENDICES

Appendix A, Operators Guide - Presents the mechanical procedures for operating the drive.

Appendix B, Documentation - Lists all the documents needed to study the subsystem in detail and to troubleshoot faults.

Appendix C, Drive Printed Circuit Boards - Describes the function of each board to help you isolate faults to the board-replacement level.

Appendix D, Internal Cables - Shows the locations of the drive internal cables and the signals they carry to assist you in tracing signals between pcb's.

Appendix E, Fault flags - Lists all the faults detected by the subsystem and tells what they mean, why they occur, and how they can be corrected.

Appendix F, Cyclic Redundancy Check Generator - Discusses the theory of operation of the subsystem CRC (checkword) data verifier.

Appendix G, Diffraction Grating - Shows how the position sensor uses a diffraction grating to detect head position.

CONTENTS

CONTENTS (Continued)

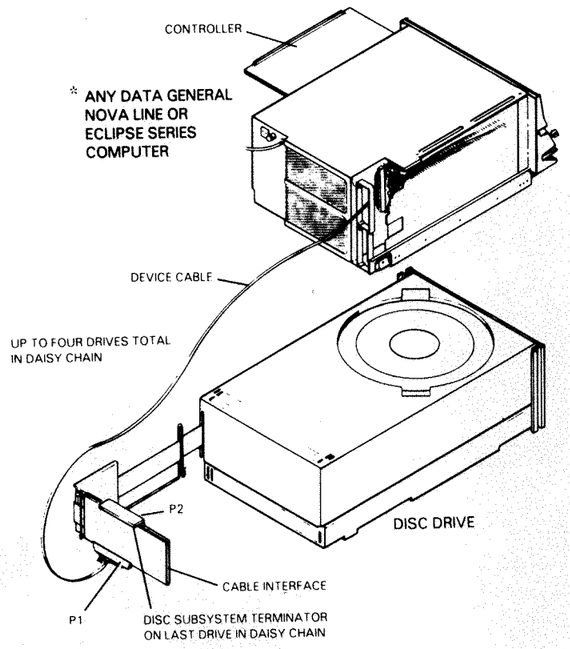
CONTENTS (Continued)

APPENDICES

PART I

TYPICAL SUBSYSTEM CONFIGURATIONS

SINGLE PROCESSOR ONE DRIVE



NOTE: DISKETTE DRIVE MAY BE INTERMIXED WITH 10Mbyte CARTRIDGE DISC DRIVE, UP TO FOUR DRIVE TOTAL PER SUBSYSTEM.

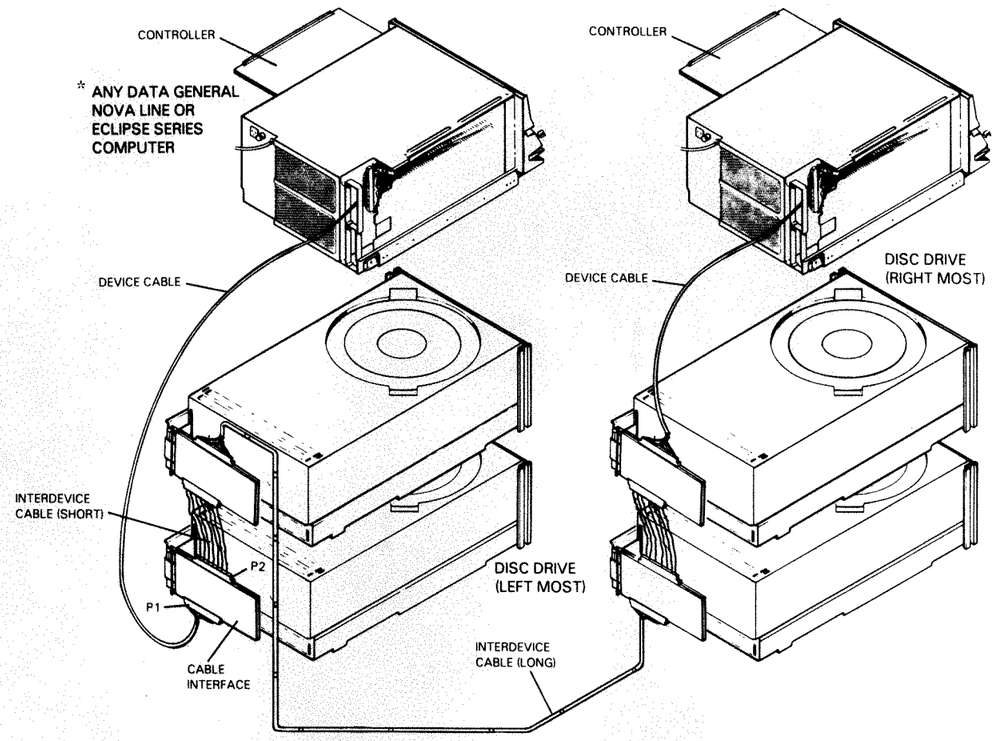
DGC DOES NOT RECOMMEND INTERMIXING 4234 TYPE DISC DRIVES IN THIS SUBSYSTEM.

NO MORE THAN TWO (2) DRIVES PER CABINET.

* EXCEPT MODEL 4001

DG-02630

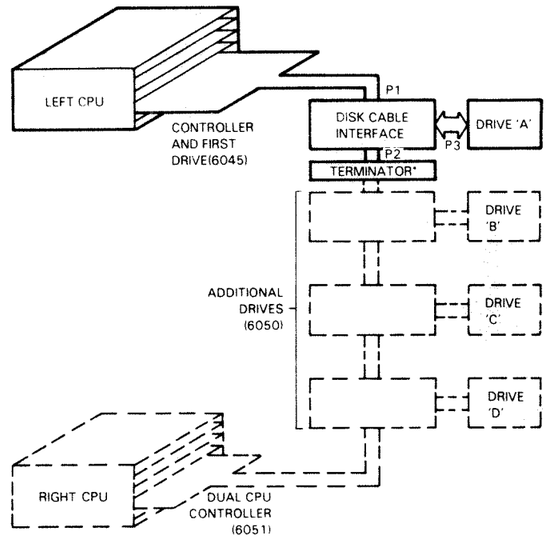
DUAL PROCESSOR/FOUR DRIVES



NOTE: BOTH PROCESSORS HAVE EQUAL PRIORITY, THE LEFT MOST DRIVE (WITH PLUG P1 CONNECTED TO PROCESSOR) CONTROLS THE PROCESSOR-SELECT SWITCHING.

DG-02631

INTERCONNECTIONS



*CONNECTED TO THE LAST DISC CABLE INTERFACE IN A SINGLE PROCESSOR SUBSYSTEM. DELETED IN A DUAL PROCESSOR SUBSYSTEM.

DG-04053

CHAPTER I
SUBSYSTEM OVERVIEW

Data General's 6045 series cartridge disc subsystem includes self-contained, medium density, 200 tpi mass storage units that provide direct access moving head disc memory for all NOVA line and ECLIPSE series computers. Each drive contains one fixed disc and one removable 5440 type cartridge disc, and has a total capacity of five million 16-bit words. Data is transferred between the disc and the computer memory in 256 word blocks at a rate of 6.4 usec per word. Subsystems may contain from one to four disc drives in both single and dual processor configurations.

INTRODUCTION

Data General's 6045 series cartridge disc subsystem provides 10 to 40 megabytes of online direct access disc storage. Each drive can store five megabytes of data on a non-removable platter, and five megabytes on a 5440-type cartridge which can be changed quickly and easily by the operator.

The disc drives interface to NOVA and ECLIPSE computers through a one board subsytem controller. These computers, and their disc-based operating systems, can support two controllers (two subsystems) on a single central processor. In addition, a controller may be installed in a second processor to support dual access. The dual access feature assigns control over the entire subsystem between the two processors on a demand basis. The diagram on the opposite page depicts typical cartridge disc subsystems. It also schematically presents the range of alternative subsystem configurations.

The Controller - is a 15 inch square printed circuit board which may be installed in any I/O slot of a NOVA or ECLIPSE computer to interface the disc drive(s) to the CPU. The controller is programmed using the basic I/O commands for NOVA and ECLIPSE computers. The programming commands prepare a disc drive for a data transfer (seek or recalibrate), initiate the transfer (read or write), and read drive status information. The data transfer itself takes place independently, through the data channel.

The Interface - connects a Disc Drive to the Controller. It conditions the controller's signals, and contains logic to mediate drive access in a dual processor environment.

The Disc Drive - is a self-contained data storage and retrieval system. It includes a data transcription assembly to read or write data on the disc surfaces , a head positioner assembly to move the heads to selected cylinders, a spindle drive assembly to rotate the discs, and a power supply to provide the internal operating voltages.

The subsystem is compatible with Data General's 6030 diskette subsystem; diskette drives can be freely intermixed with the cartridge disc drives in any subsystem.

SUMMARY OF CHARACTERISTICS

CHARACTERISTICS

Moving head (optical position sensor)
Type 5440 removable disc cartridge plus fixed disc
Four surfaces, twelve sectors per surface, 256 words per sector
408 cylinders
Transfers up to sixteen sectors per operation
Two word data channel buffer
Sixteen bit cyclic redundancy check
Four drives per subsystem (may intermix with 6030 diskette)
Dual processor access
Guaranteed cartridge interchangeability between drives
Temperature compensation reduces offset between positioner and media

CAPACITY AND TIMING

Capacity	10,027,008Bytes/drive 24,576Bytes/cylinder (408 cylinders) 6,144Bytes/track (4 surfaces) 512Bytes/sector (12 sectors)
Data transfer rate	156,250wps (6.4us/word)
Disc rotational speed	2400rpm
Rotational latency	12.5ms (average)
Sector access time	0.12ms(min)/25ms(max)
Sector time	2.08ms
Data block time	1.638ms
Bit density	1095BPI (431bit/Cm)
Track density	200tpi (78.7t/Cm) 0.005in/trk (0.127mm/trk)
Track width	0.004in (0.102mm)
Seek time	15ms (single cylinder) 100ms (full stroke)
Turn-on-to-Ready	27s - 36s (assumes media temperature is in compensation range)

DRIVE PROPERTIES

Dimensions	height 10.5in (26cm) width 19.0in (48cm) depth 29.7in (77cm)
Weight	157lb (65.5Kg)
Temperature (max)	cabinet: 110°F (43°C) room: 90°F (33°C) gradient: 10°F/hr (5.5°C)
Relative humidity	20 - 80% (non-condensing)
Altitude	0 - 10,000ft (0 - 3000m)

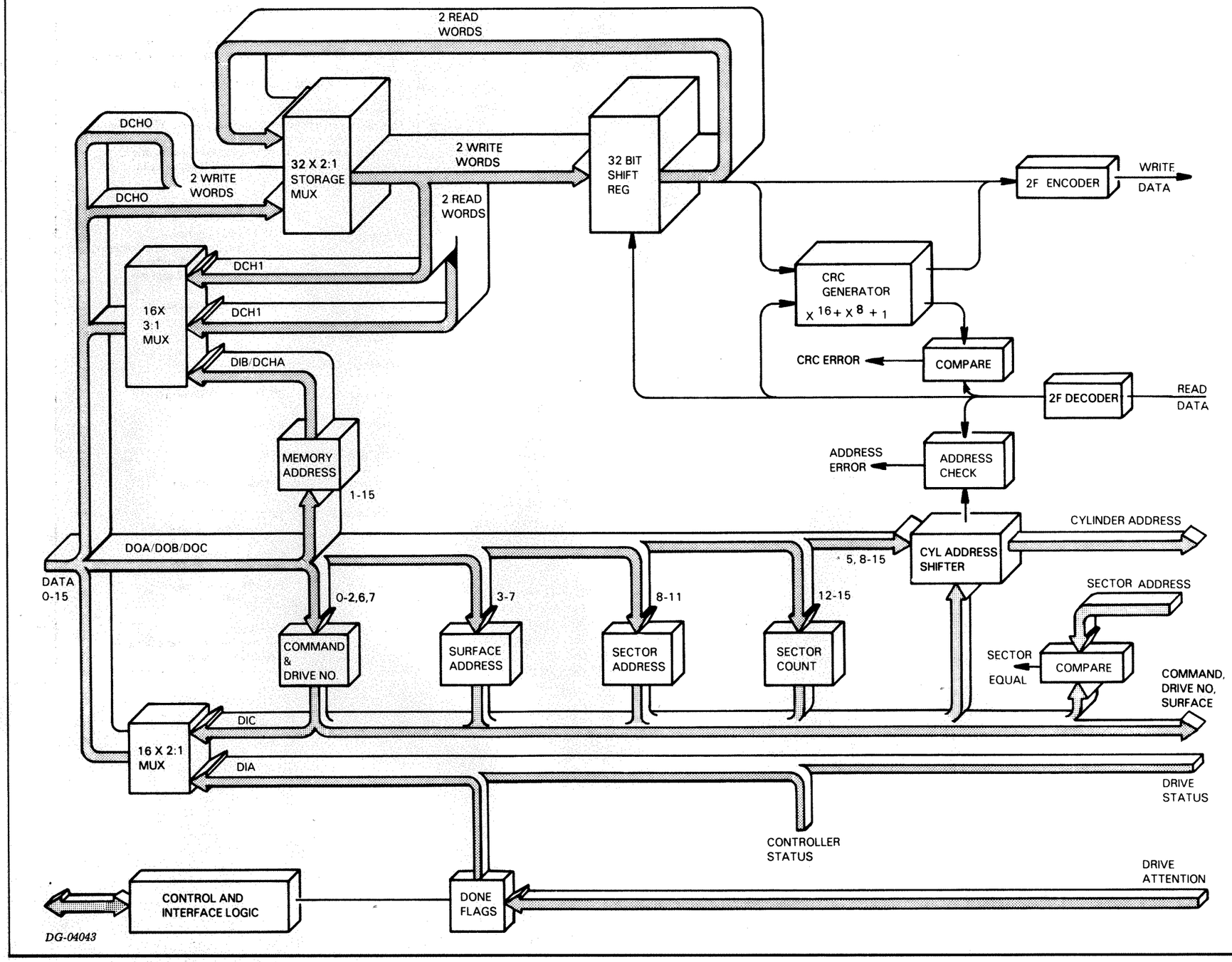
Input power

Volts (+10/-15%)	Amps	Freq (+-1Hz)
100	5.7	60
120	4.9	60
100	5.7	50
220	2.6	50
240	2.4	50

MODEL NUMBERS

6045	One 10 megabyte drive with controller, terminator and cables
6046	Two 10 megabyte drives with controller, terminator and cables
6047	Three 10 megabyte drives with controller, terminator and cables
6048	Four 10 megabyte drives with controller, terminator and cables
6050	Additional 10 megbyte drive with cable
6051	Additional controller with cables for dual processor access
1121A	One 5440 type disc cartridge
1121B	Six 5440 type disc cartridges

CONTROLLER BLOCK DIAGRAM



CHAPTER II
CONTROLLER OVERVIEW

INTRODUCTION

The controller directs the activities of the cartridge disc subsystem. It decodes instructions received from the processor, selects a drive, issues seek or recalibrate commands and supports data transfers.

The controller contains the following logical blocks;

- Command storage register
- Drive, surface, cylinder and starting sector address registers and sector count register.
- Sector address check logic
- Data encoder/decoder, serial/parallel converter and CRC generator
- Memory address register
- Two word data channel buffer
- Busy, Done, and miscellaneous control and interface logic

Drive Control

The drive control logic decodes instructions and initiates seek, recalibrate, read or write operations on selected drives. A seek command causes a drive to move its heads to the specified cylinder and a recalibrate command moves the heads to cylinder zero. A read or write command transfers a specified number of sectors (256 words per sector) between the selected disc and processor memory via the data channel.

Once the desired sector is reached, but before a sector data transfer occurs, the address verify logic reads the preformatted surface/track/sector address header written on each sector. The controller compares it to the address specified by the program. The verify logic sends an error signal to the program and terminates the data transfer, if the address is not correct. If no errors occur, the 256 word data block transfer follows.

Data Transfer

During a write operation, the processor transfers 16 bit data words to the 32-bit storage multiplexor via the data channel. When two words have been assembled, they are transferred to the 32-bit shift register. The serial output from the register is combined (in 2F encoded mode) with clock timing signals, and transferred to the drive, where the serial stream is written onto the disc. Data is transferred in blocks of 256 words. The CRC generator calculates a 16-bit Cyclic Redundancy Checkword as each block is written. The controller appends the resultant checkword to the data block.

During a read operation, the drive reads the serial stream; the controller strips the clock signal, and transfers binary data to the 32-bit shift register. When two words have been assembled, they are transferred to the 32-bit storage multiplexor which dumps one word at a time through the input multiplexor to the processor data channel. Data is transferred in blocks of 256 words. The CRC generator calculates a 16 bit Cyclic Redundancy Checkword as each block is read, and compares the resultant checkword to the one which follows the data block (calculated during the previous write operation). If they do not match, an error signal is sent to the program and the data transfer terminates.

The Busy and Done logic and the status register allow the program to determine in detail the status of the subsystem. The Busy flag sets when the program initiates the data transfer. The data transfer terminates and the Done flag sets when the sector counter overflows or an error occurs.

INSTRUCTIONS

The instructions that control the subsystem are described below. The *Specify command and cylinder* instruction passes a new command to the subsystem and indicates the new track address for a seek. The *Specify disc address and sector count* instruction selects a drive, and indicates the starting sector and surface and the sector count for a data transfer. The *Load memory address counter* instruction indicates the starting memory address for a data channel transfer. The remaining instructions allow the processor to determine the status of the subsystem.

The device flag commands control the disc controller's Busy and Done flags as follows:

f = S Sets the Busy flag to 1, the Done flag to 0, the Address Error, End of Cylinder, Checkword Error, Data Late, and Unsafe flags to 0, and initiates the operation specified by the contents of the command register.

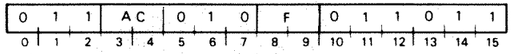
f = C Sets the Busy flag, the Done flag, all Error flags and all Seek Done flags to 0 and stops all data transfer operations; does not terminate a seek operation already in progress.

f = P Sets the Done flag and all Error flags to 0 and initiates the operation specified by the contents of the command register.

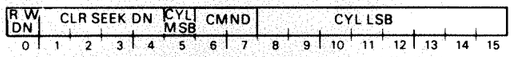
NOTE *The* **P** *flag command does not affect the controller's Busy flag. If the Busy flag is 0 and the program starts an operation with the* **P** *command, the controller does not initiate a program interrupt request at the conclusion of the operation unless it is a seek or recalibrate. The controller initiates an interrupt at the end of all seek or recalibrate operations.*

Specify Command and Cylinder

DOA *[f] ac,* **DKP**



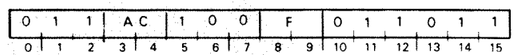
Loads bits 0-15 of the specified AC into the controller's combined command and cylinder select register. After the data transfer, sets the controller's Busy and Done flags according to the function specified by **F**. The contents of the specified AC remain unchanged; the format of the accumulator is as follows:



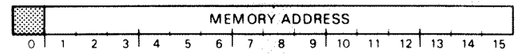
Bits	Name	Function
0	Clear R/W Done	Sets the status register's DC Done flag to 0; sets the following error flags to 0: Address Error, Checkword Error, End of Cylinder, and Unsafe.
1-4	Clear Seek Done (0-3)	Sets the Seek Done flags to 0 on drives 0-3, respectively.
5	Cylinder MSB	Most significant bit of cylinder address. Together with bits 8-15, specifies the desired cylinder.
6-7	Command	Specifies the command for the selected drive as follows: 00 Read 01 Write 10 Seek 11 Recalibrate
8-15	Cylinder LSB	Least significant bits of Cylinder Address. Together with bit 5, specifies the desired cylinder (0-627$_8$) for a Seek, Read or Write operation.

Load Memory Address Register

DOB *[f] ac,* **DKP**



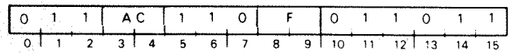
Loads bits 1-15 of the specified AC into the controller's memory address Register. After the data transfer, sets the controller's Busy and Done flags according to the function specified by **F**. The contents of the specified AC remain unchanged; the format of the accumulator is as follows:



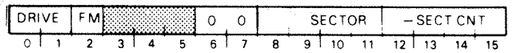
Bits	Name	Contents
0	---	Reserved for future use.
1-15	Memory Address	Location of the next word in memory to be used for a data channel transfer.

Specify Disc Address and Sector Count

DOC *[f] ac,* **DKP**



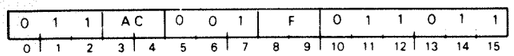
Loads bits 0-15 of the specified AC into the controller's disc address register and sector counter. After the data transfer, sets the controller's Busy and Done flags according to the function specifed by **F**. The contents of the specified AC remain unchanged; the format of the accumulator is as follows:



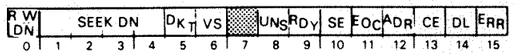
Bits	Name	Function
0-1	Drive	Selects drive 0-3$_8$
2	Format	If 1, places controller in FORMAT mode.
3-5	---	Reserved for future use.
6-7	Surface	Selects the surface (head) 0-3$_8$ for the start of a read or a write operation.
8-11	Sector	Selects the starting sector, 0-13$_8$ for the start of a read or a write operation.
12-15	-Sector Count	Specifies the two's complement of the number of sectors to be read or written in one operation (maximum of 16$_{10}$).

Read Status

DIA *[f]* *ac*, **DKP**



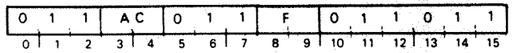
Places the contents of the controller's status register in bits 0-15 of the specified AC. After the data transfer, sets the controller's Busy and Done flags according to the function specified by **F**. The format of the specified accumulator is as follows:



Bits	Name	Meaning When 1
0	R/W Done	The subsystem has completed a read or a write operation.
1-4	Seek Done (0-3)	Drive 0-3, respectively, has completed a seek or recalibrate operation. *More than one of these bits can be set at any time.*
5	Diskette	The selected disc is a diskette drive unit.
6	Valid Status	When the read status command was issued, the controller had control of the disc subsystem.
7	---	Reserved for future use.
8	Unsafe	The selected drive is in an unsafe condition. The Unsafe flag can be reset with an **S**, **C**, **P**, or **IORST** command, but this action will not remove the drive's unsafe condition. Try to remedy the unsafe condition by powering down the drive, and then restarting it.
9	Unit Ready	The selected drive is not performing any head movements and is ready to carry out a command (read, write, seek, or recalibrate)
10	Seek Error	The selected drive was not able to carry out the last seek or recalibrate operation issued.
11	End of Cylinder	The last read or write operation attempted to continue beyond the fourth surface in the disc drive unit.
12	Address Error	The address read from the address field at the beginning of a sector does not match the last address specified to the disc controller.
13	Checkword Error	The checkword read from the disc at the end of a sector does not match the checkword calculated by the controller during the sector transfer.
14	Data Late	The data channel failed to respond in time to a data channel request.
15	Error	One or more of the following bits in the status register is set to 1: 8, 10, 11, 12, 13, or 14.

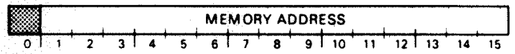
Read Memory Address Register

DIB *[f]* *ac*, **DKP**



Places the contents of the controller's memory address register in bits 1-15 of the specified AC; sets bit 0 to 0. After the data transfer, sets the controller's Busy and Done flags according to the function specified by **F**. The format of the specified AC is shown below.

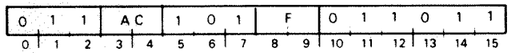
NOTE *At the end of a write operation, the memory address register points to a memory location* **two** *greater than that of the most recent word written to disc.*



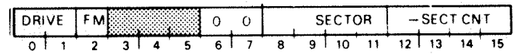
Bits	Name	Contents
0	---	Reserved for future use.
1-15	Memory Address	Location of the next word in memory to be used for a data channel transfer.

Read Disc Address and Sector Count

DIC *[f]* *ac*, **DKP**

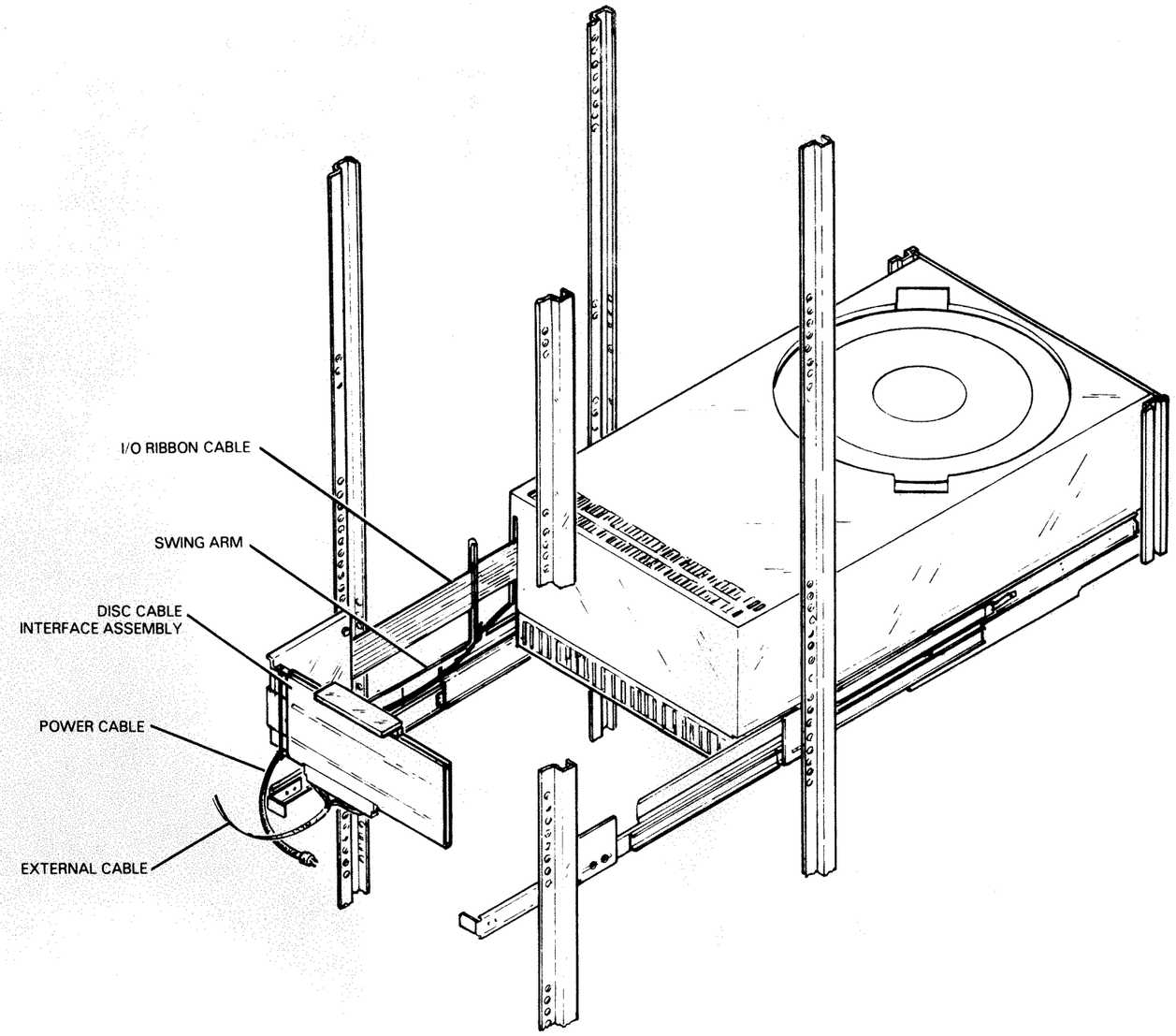


Places the contents of the controller's disc address register and sector counter in bits 0-15 of the specified AC. After the data transfer, sets the controller's Busy and Done flags according to the function specified by **F**. The format of the specified accumulator is as follows:



Bits	Name	Contents
0-1	Drive	Number (0-3) of the selected drive.
2	Format	When 1, Indicates that the controller is in FORMAT mode.
3-5	---	Reserved for future use.*
6-7	Surface	Surface number (0-3) of the selected head on the drive.
8-11	Sector	Number of the sector (0-13_8) immediately following the last sector read or written. If a read or write operation ends at the last sector (13_8) of a surface, this field contains the value 14_8.
12-15	- Sector Count	Two's complement of the number of sectors remaining to be read or written.

Bits 3-5 are the high-order bits for the head address field; they are ignored in all operations. Iif these bits are loaded with a value during a **DOC** *instruction, that value will appear in the specified accumulator when a* **DIC** *instruction is issued. Upon End of Cylinder Error, the contents of these bits is incremented by 1.*



REAR VIEW OF A DISC DRIVE MOUNTED IN A SWING CABINET. DRIVE IS SHOWN PARTIALLY EXTENDED ON THE SLIDE RAILS. NOTE DISC CABLE INTERFACE ASSEMBLY FASTENED TO THE REAR CABINET RAIL; SLACK IN I/O AND POWER CABLES IS TAKEN UP BY A SPRING-LOADED SWING ARM.

DG-04105

CHAPTER III
INTERFACE OVERVIEW

INTRODUCTION

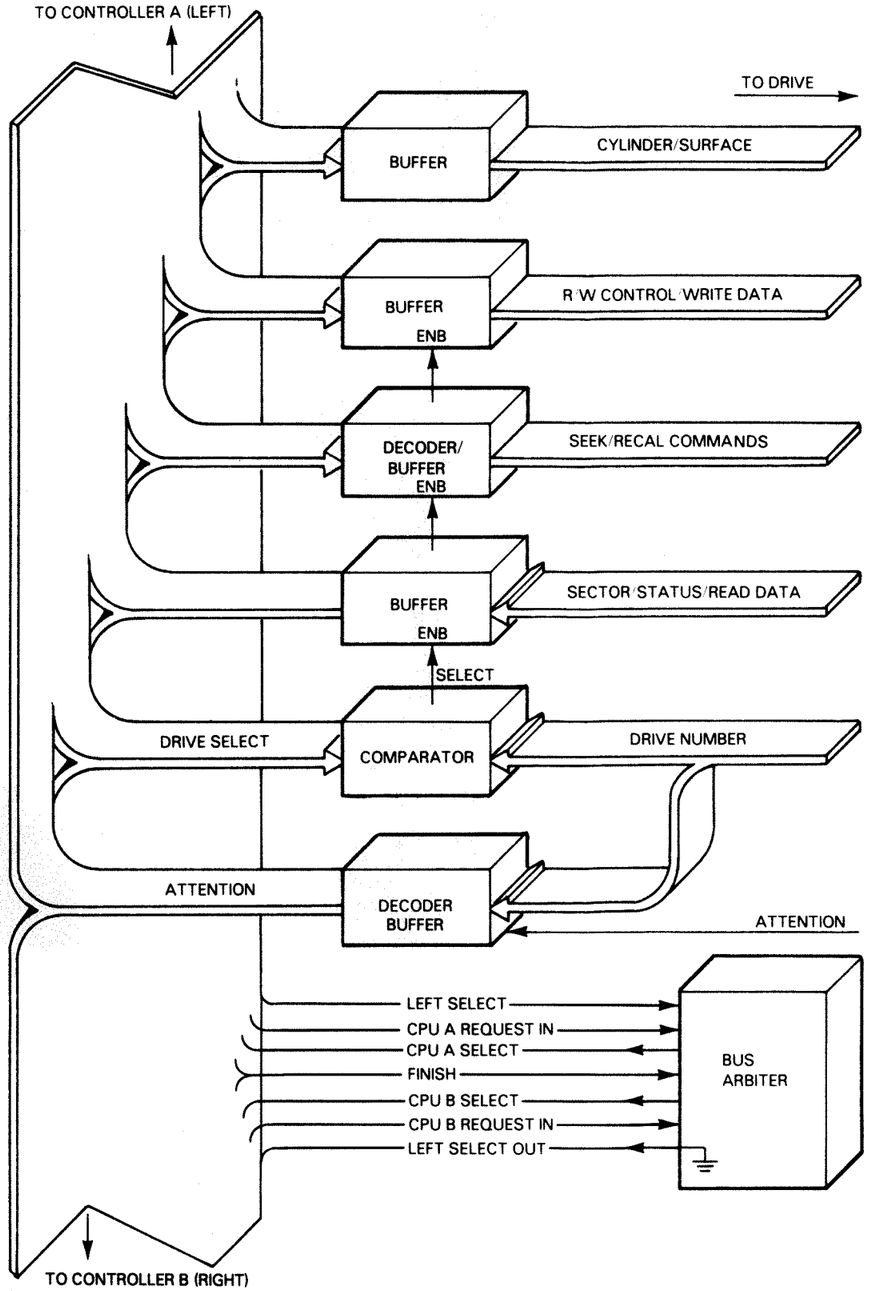
Each drive communicates with subsystem controller(s) through a separate interface board. The board is covered by a protective metal enclosure which mounts on rails behind the drive. (The rear protective cover can be removed for service access.) The interface connects to the drive through a flexible ribbon cable, and a swing arm retracts the cable to prevent damage as the drive slides into the rack. Edge connectors accept controller cables or terminators.

The interface logic is summarized in the block diagram to the right. Once the processor is granted access to the bus (in single processor systems the arbiter is disabled and access is always available), each interface compares the drive number sent out by the controller with the drive number on its select switch on the front panel of the drive. The selected interface connects its drive to the bus. The interface buffers all the signals on the bi-directional controller bus and decodes drive attention requests and position commands.

The Bus Arbiter

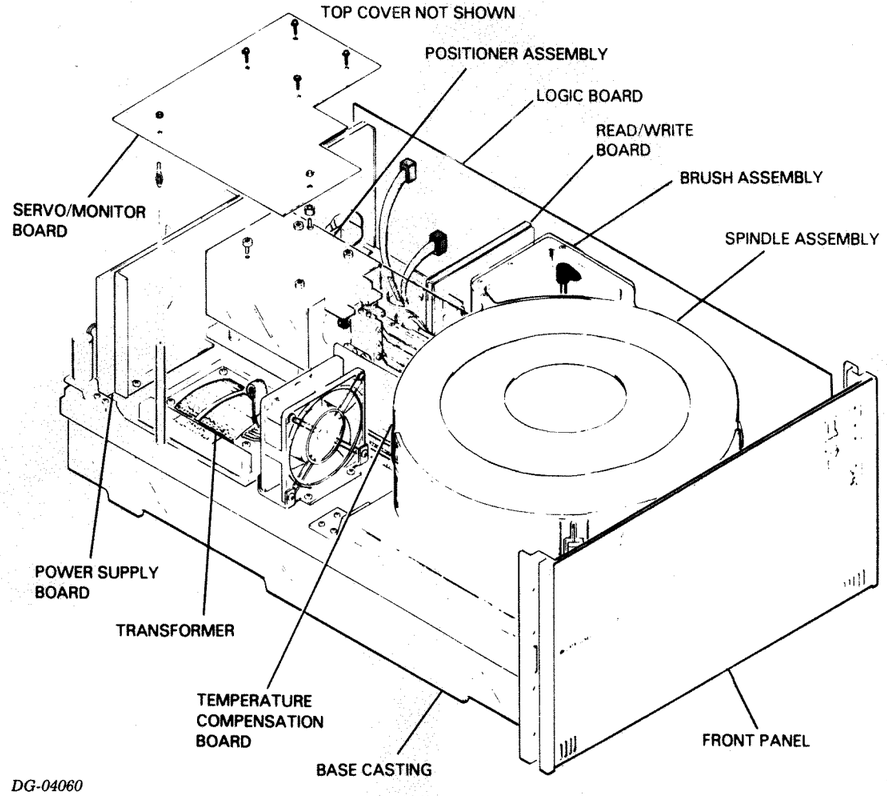
The leftmost interface controls access in a dual processor system. The left controller enables the leftmost bus arbiter (**Left Select**) which in turn disables the remaining arbiters in the chain (**Left Select Out**). Controllers compete for access on a first come, first served basis. Usually the first controller that issues a request (**CPU Request In**) gets the bus (**CPU Select**). The controller releases the arbiter (**Finish**) when the transfer is complete. If the controller tries to hold the bus for more than three seconds, a timer automatically releases it. This constrains the time the controller has to issue a seek, preventing a controller from locking up the subsystem. (In a single processor system, the controller ignores the arbiter and permanently connects to the bus.)

CABLE INTERFACE BLOCK DIAGRAM

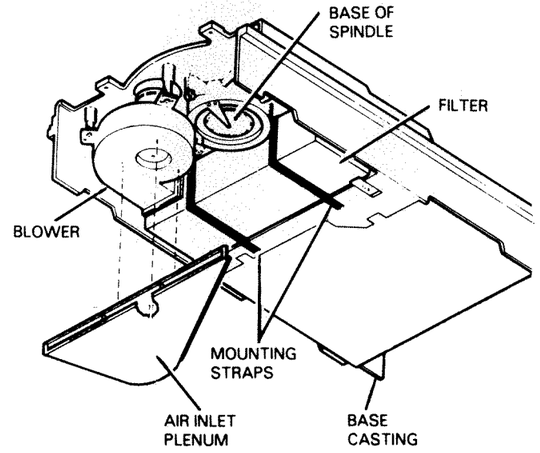


DG-04054

DRIVE INTERNAL VIEW



DG-04060



DG-04063

ROTATED 180° FOR CLARITY

CHAPTER IV
DRIVE OVERVIEW

INTRODUCTION

The cartridge disc subsystem employs rack mountable moving head disc data storage units. Each drive contains a non-removable disc and a removable top loading cartridge disc, and has a total storage capacity of 10 Mbytes of data. Both discs are mounted on a vertical splindle which is directly driven by a motor. A brush assembly cleans the surfaces during disc startup.

Each disc has two recording surfaces and the drive contains four recording heads which move in unison on the servo controlled positioner assembly. Position and velocity transducers provide feedback signals to the positioner servo to support rapid and accurate head positioning.

A velocity tachometer controls large positioner movements. An optical position sensor locates the data track zone, defines the data track centerlines, and controls small positioner movements in the vicinity of a selected track. A temperature compensation circuit reduces position errors caused by different drive and cartridge temperatures, and reduces startup time when the cartridge disc is changed.

The positioner control circuits locate the heads over selected tracks in response to commands from the drive console and the subsystem controller. The data transcription circuits write encoded data and recover binary data and a clock from the encoded read data. Logical and switched interlocks maintain data integrity in the event of component failure or operator error.

The drive is fully self contained and includes a power supply, blower, filter, and cooling fan. It requires a minimum of maintenance, and can operate in a wide range of environments. In the event of failure, the subassemblies can be easily adjusted or replaced in the field.

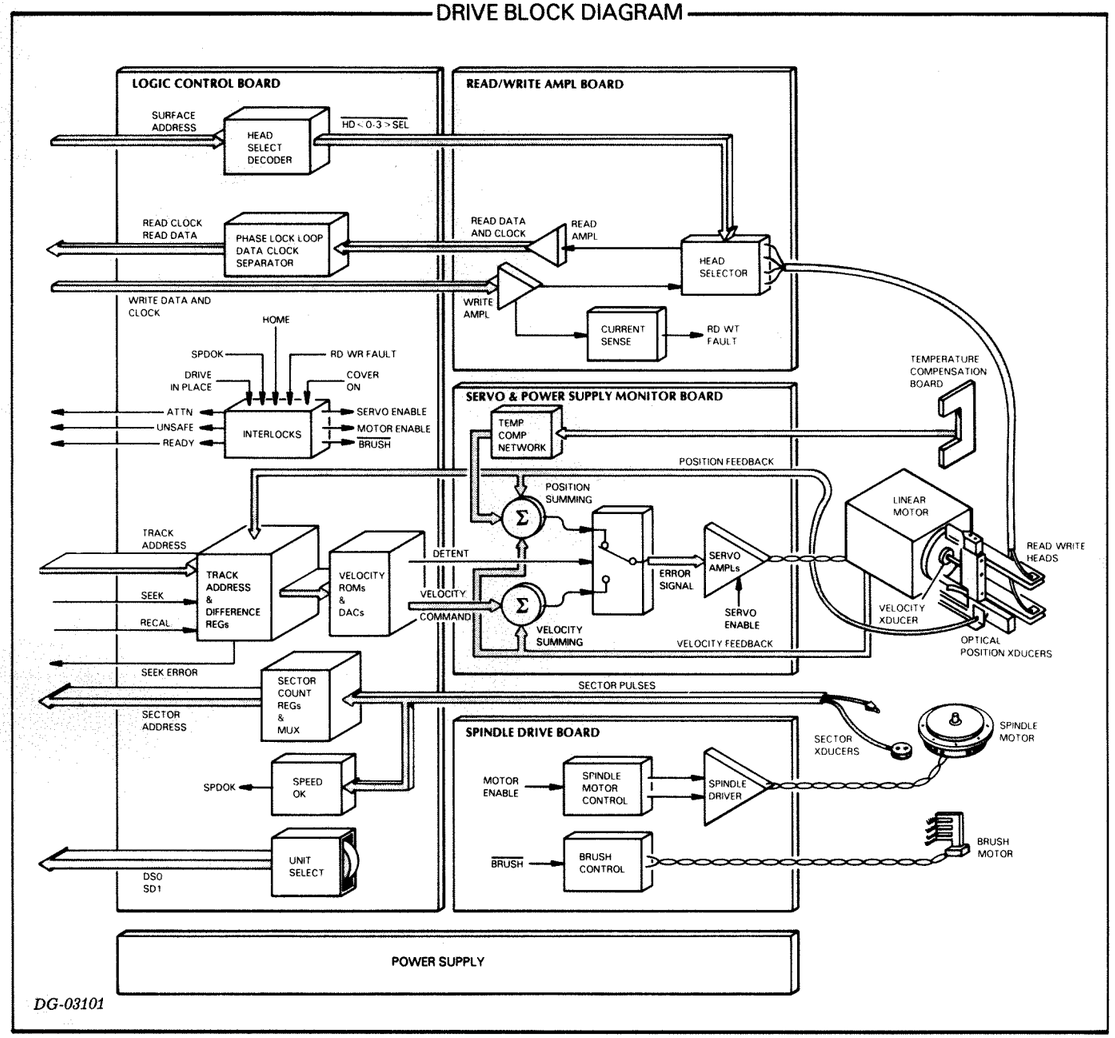
The disc drive incorporates a system of interlocks which monitor the drive to insure safe operation and data reliability. If an interlock is violated, the drive may lockout data transfers or unload the heads and prevent further access until the fault is cleared.

The major subassemblies are;

- *Spindle drive and monitors*
- *Head positioner and servo*
- *Data transcription*
- *Power supply*

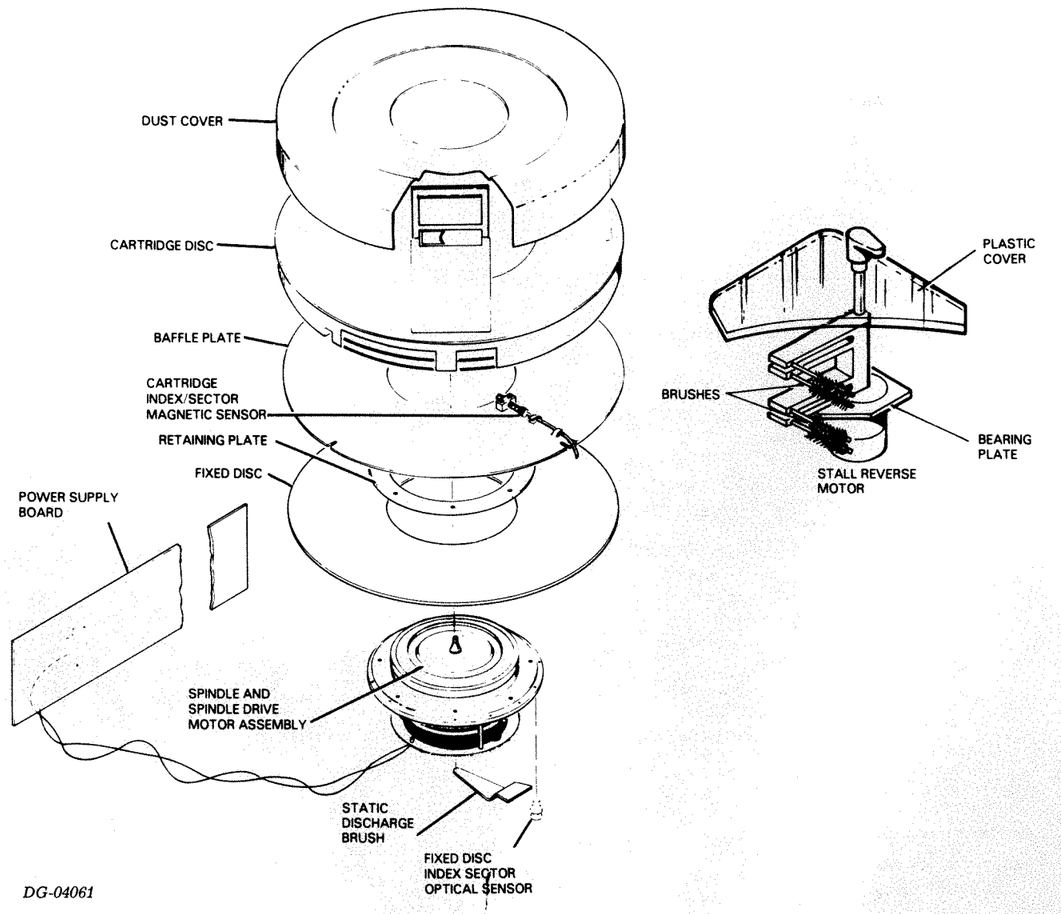
The figure on the opposite page shows all the major subassemblies. They are supported by the base casting and enclosed by a removable top cover. The front panel contains the operator controls. The drive unit mounts on roller slides in a standard 19" equipment cabinet.

DRIVE BLOCK DIAGRAM



DG-03101

SPINDLE ASSEMBLY



DG-04061

Spindle Drive and Monitors

The spindle assembly supports and rotates the recording discs, and a brush assembly sweeps the surfaces during startup. A blower cools the discs and purges the disc cavity with finely filtered air. If the drive is extended on the slides or the protective dust cover is not in place, interlock devices disable spindle operation. These same interlocks also prevent the operator from extending the drive if the spindle is turning.

The spindle runs in precision ball bearings and is rotated by an integral synchronous drive motor. It supports the fixed disc and the cartridge disc on a common axis. The fixed disc bolts directly to a ring at the base of the spindle. The ring also has holes drilled around its periphery to provide sector marks for the optical sector pickup. A magnet at the top of the spindle clamps the removable cartridge disc. A second ring at the base of the cartridge disc has slots around its periphery to provide sector marks for the magnetic sector pickup (the spindle mounted magnet provides the field).

A baffle plate divides the cavity into an upper and lower chamber and prevents contamination of the fixed disc. The cartridge includes a protective bottom cover which is removed before the cartridge is inserted, and placed on top of the mounted cartridge to keep contaminants out of the spindle cavity.

The drive motor rotates the discs at 2400rpm. Circuits on the power supply board divide a precision crystal clock and provide two phase drive current for the two motor poles. These circuits reverse the phase relationship during an unload cycle to provide dynamic braking, and then apply direct current to stop spindle rotation.

The sector pickups send clock pulses to the spindle speed monitor and the sector counters. The spindle speed monitor checks that the frequency of the fixed sector pickup signal is within acceptable limits and that the cartridge pickup signal is present (the drive will not load the heads if the cartridge disc is not installed.) Each disc has a separate sector counter. (The cartridge disc is not keyed to mechanically align with the fixed disc.) The sector counters increment when the pickups detect sector pulses, and reset when the pickups detect index pulses.

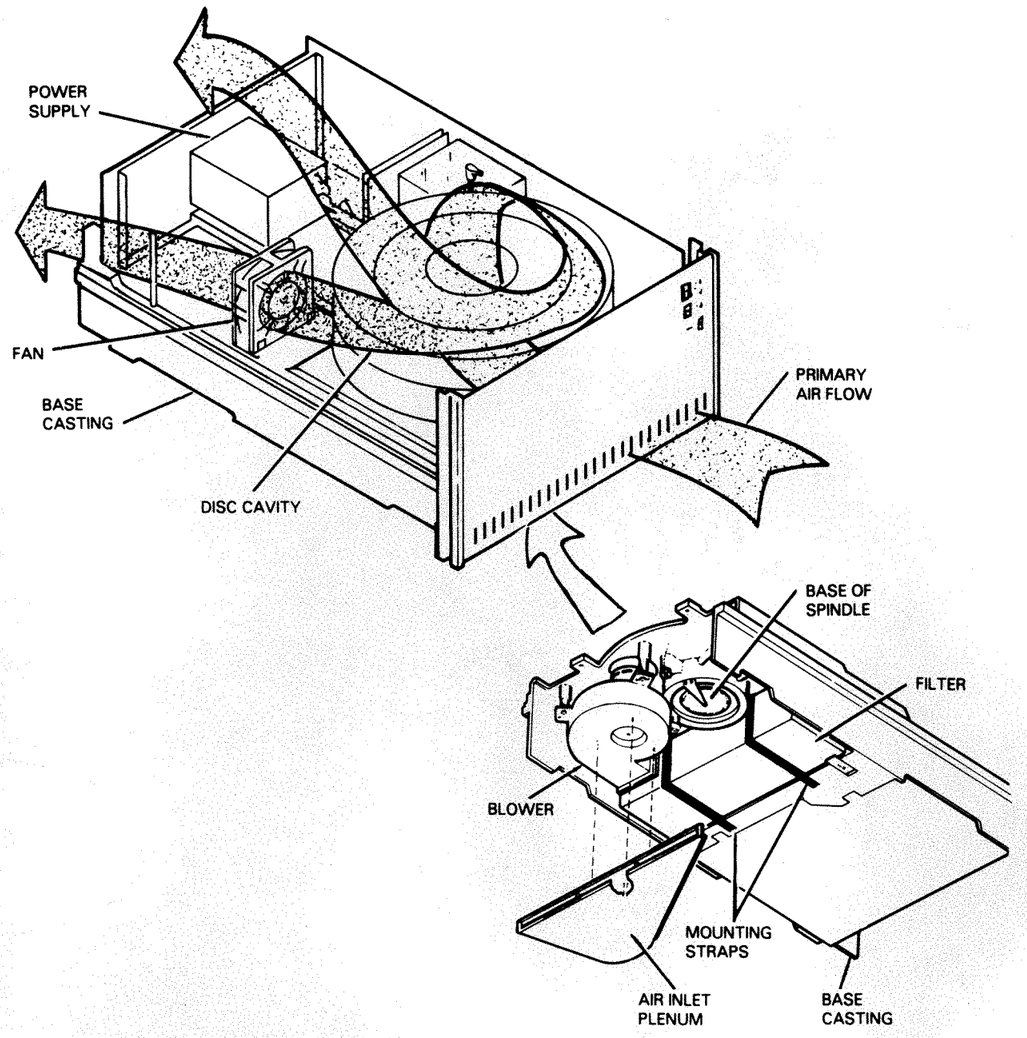
The brush assembly sweeps contaminants off the disc surfaces after the spindle comes up to speed but before the drive loads the heads. It employs a stall reverse motor that automatically reverses and retracts the brushes when they hit the extension stop.

A blower mounted under the spindle assembly forces air through a fine filter and into the disc cavity to clean and cool the disc surfaces. The positive air pressure within the cavity expels any foreign matter. The air exhaust from the rear of the cavity cools the remainder of the drive components. No external cooling is required when the drive is operated within the environmental limits; however, it is necessary that the airflow remain unobstructed. It is important to replace the filter at periodic intervals (about 1000 operating hours or six months) to prevent contamination of the disc cavity and provide unrestricted airflow.

Several mechanical interlocks protect the discs and heads. The drawer latch locks the drive in the cabinet when the drive is powered down or running. This prevents anyone from extending the drive and removing the cartridge disc while the spindle is running. (The latch may be manually operated from the rear of the drive if neccessary.) If the drive is extended or the dust cover is not in place, the drive in place switch and cover on switch disable the spindle. (Field service personnel can disable the drive in place switch by pulling out on the switch button. It is not recommended that the drive be normally operated in the extended position.) These three interlock switches are closely associated with the operator procedures discussed in Appendix A.

There are also logical interlocks such as **Speed OK** which inhibit drive operation and these are discussed in the following chapters.

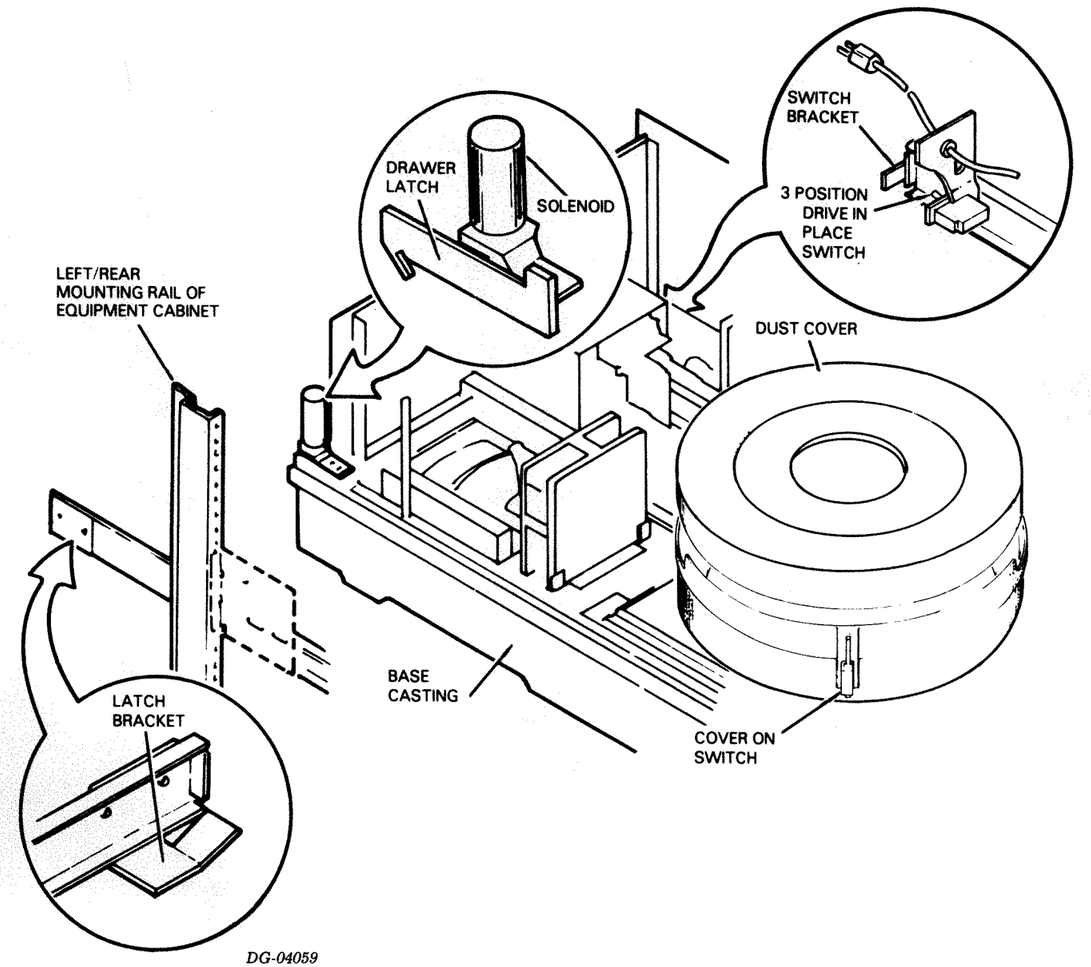
AIR FLOW



DG-04063

ROTATED 180°FOR CLARITY

INTERLOCK LOCATIONS



DG-04059

Head Positioner and Servo

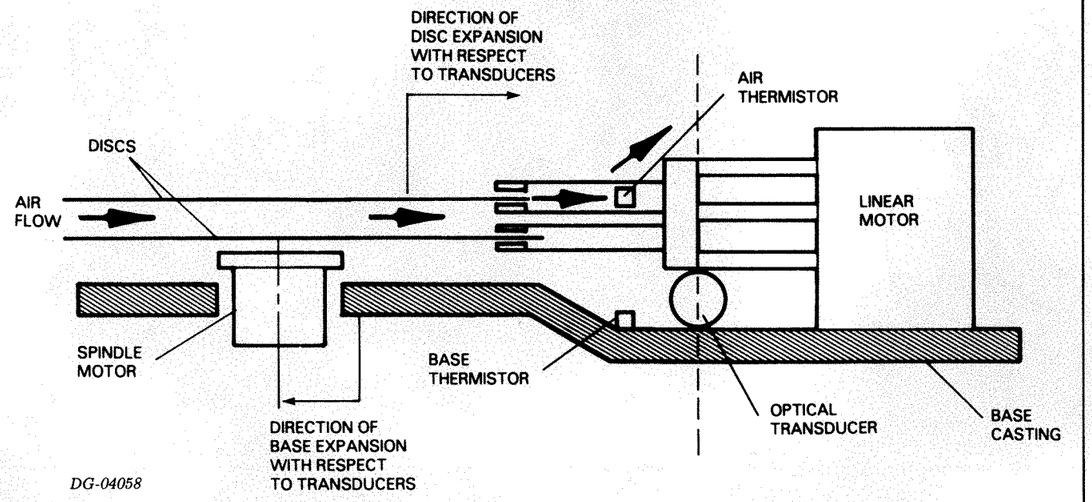
The head positioner shown to the right loads the heads onto the disc surface, locates the heads over selected data tracks, and unloads the heads to allow powerdown or cartridge interchange. A linear motor moves the carriage along precision ways, and a cam assembly lifts the heads away from the disc surfaces as they approach the outer edge. (The positioner and its associated control circuits are designed to prevent contact between the heads and the disc surfaces.)

A feedback servo system controls the positioner. Circuits on the servo/monitor board accept signals from the optical position transducer and the linear motor tachometer. The servo has two modes of operation: *velocity* and *detent*. Feedback from the tachometer controls positioner speed in velocity mode as the heads move to the desired track. The position signal indicates data track crossings and updates the present track address register. Read only memories dictate a reduction in velocity as the positioner approaches the destination track.

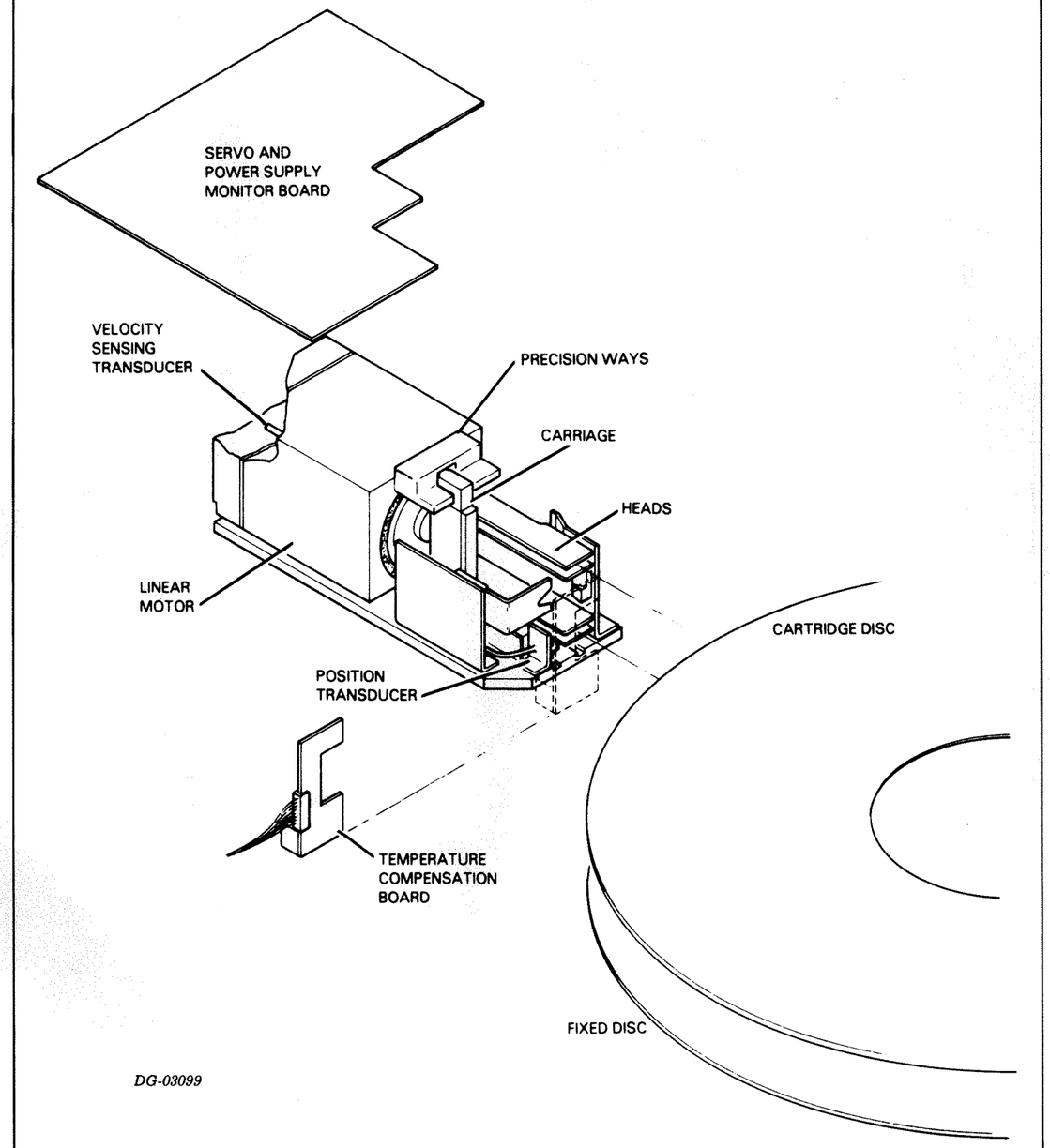
A signal from the position transducer controls the positioner in detent mode as the heads move over the desired track. The position signal feeds a closed loop servo that detects offset errors and drives the positioner back on track.

A temperature difference between the disc surfaces and the drive can cause misalignment between the heads and the data tracks. A temperature compensation network offsets this error and reduces the wait time after a cold cartridge is placed in a hot drive. Thermistors measure the temperature of the drive and the exhaust from the disc cavity, and offset the positioner in detent mode to counteract the mechanical error.

TEMPERATURE SENSORS



HEAD POSITIONER ASSEMBLY

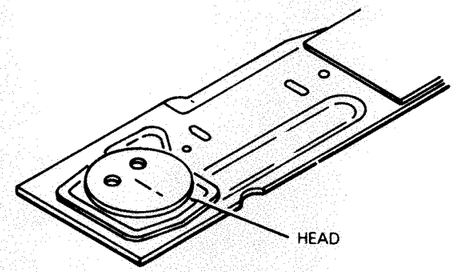


Data Transcription

Four read/write heads record and read data on the disc surfaces. The heads float on a cushion of air above the surfaces and small read/write coils define the physical location of the data tracks. Data is recorded serially as a series of flux transitions that polarize the magnetic oxide coating on the disc surfaces. The data encoding scheme, called two frequency (2F), records a flux transition at the beginning of each bit cell, and in the center of each cell containing a one.

The head select circuits activate one head at a time for reading or writing. The write circuits receive 2F encoded data from the controller and induce a regulated current in the selected head. A tunnel erase coil then trims the track to prevent crosstalk into adjacent tracks. The selected read head detects flux reversals on the recording surface and uses a phase locked loop to recover the binary data stream and clock.

READ/WRITE HEAD

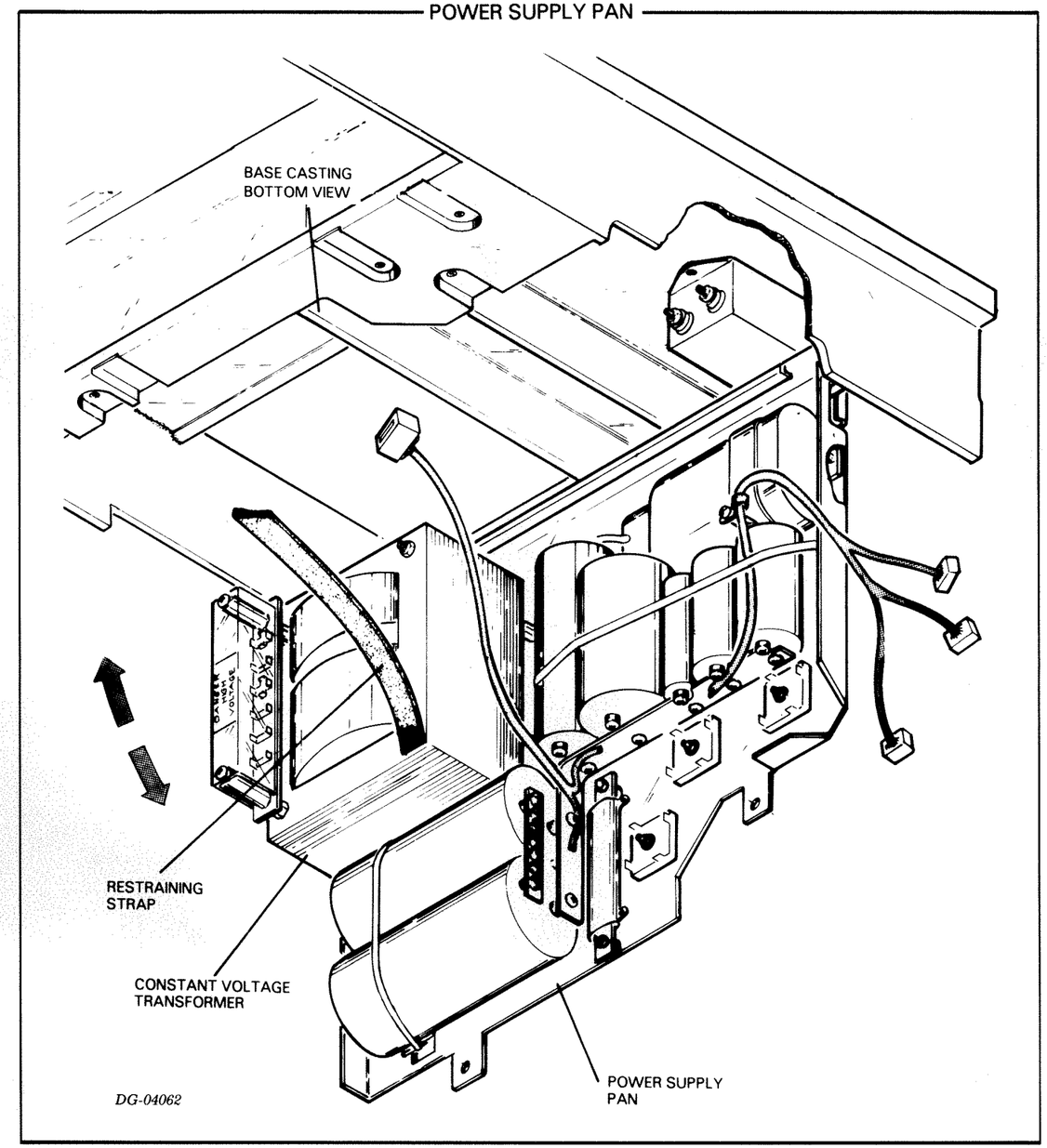


DG-04106

Power Supply

A self contained dc power supply energizes the spindle, brush and linear motors as well as the associated control and data transcription circuits. A constant voltage transformer *(CVT,* also called *ferroresonant)* provides coarsely regulated voltages for six series pass regulators that provide the drive operating voltages. The transformer, rectifiers and filters mount on a pan that swings down below the base of the drive for easy service access. The regulators are located on the power supply board at the rear of the drive and the voltage monitors appear on the servo monitor board above the positioner.

POWER SUPPLY PAN



DG-04062

PART II

CHAPTER V
CONTROLLER

INTRODUCTION

The controller directs the activities of the cartridge disc subsystem. It decodes instructions received from the processor, selects a drive, issues seek or recalibrate commands and supports data transfers.

The controller can be divided into four logical blocks;

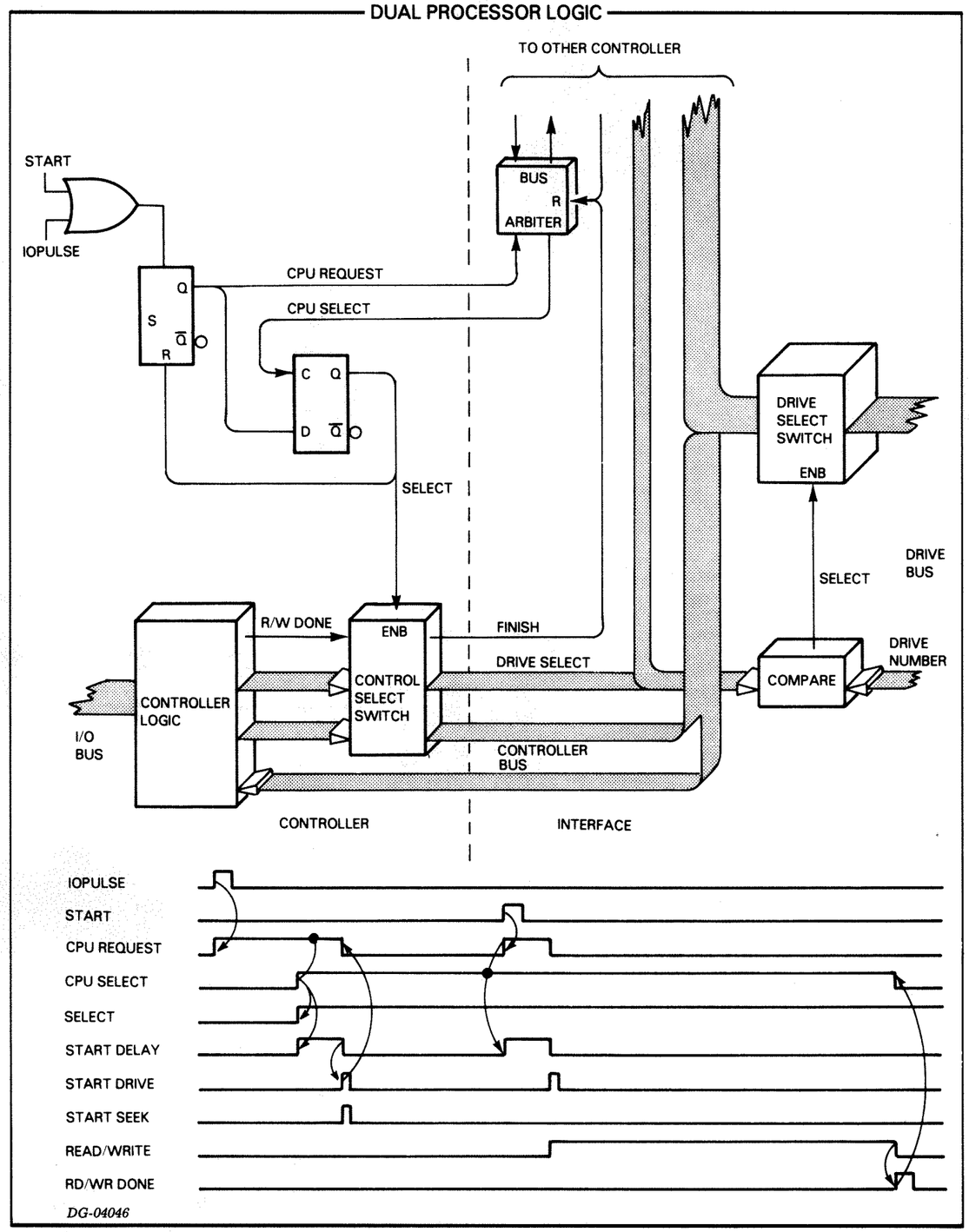
- *The Dual Processor logic requests the bus arbiter to open the channel between the controller and the drives when the processor initiates a command or data transfer.*
- *The Drive Command logic sends seek and recalibrate commands to selected drives.*
- *The Read/Write Control logic sets up and times data transfers on selected drives.*
- *The Data Transfer logic buffers data words and supports data conversion.*

Dual Processor Logic

A bus arbiter, located in the Interface, controls access to a common set of drives in a dual processor system. The controllers compete for access on a first come, first serve basis. The winner retains control until it completes a data transfer or is released by a three second timer. When the processor issues a *start* (S) or *pulse* (P) to initiate a transfer, the controller requests the bus arbiter to open the channel. When the arbiter indicates that the channel is available, the controller connects to the bus. The controller releases the bus when it terminates a data transfer, but it remains connected until the arbiter opens the channel to the other controller. (In single processor subsystems, the controller is permanently connected to the bus.)

Drive Command Logic

The controller transfers position commands as soon as the channel opens. It sends a **track address strobe** to clock the command into the selected drive, and specifies a seek or recalibrate operation. The nine bit track address register indicates the destination track for a seek operation.

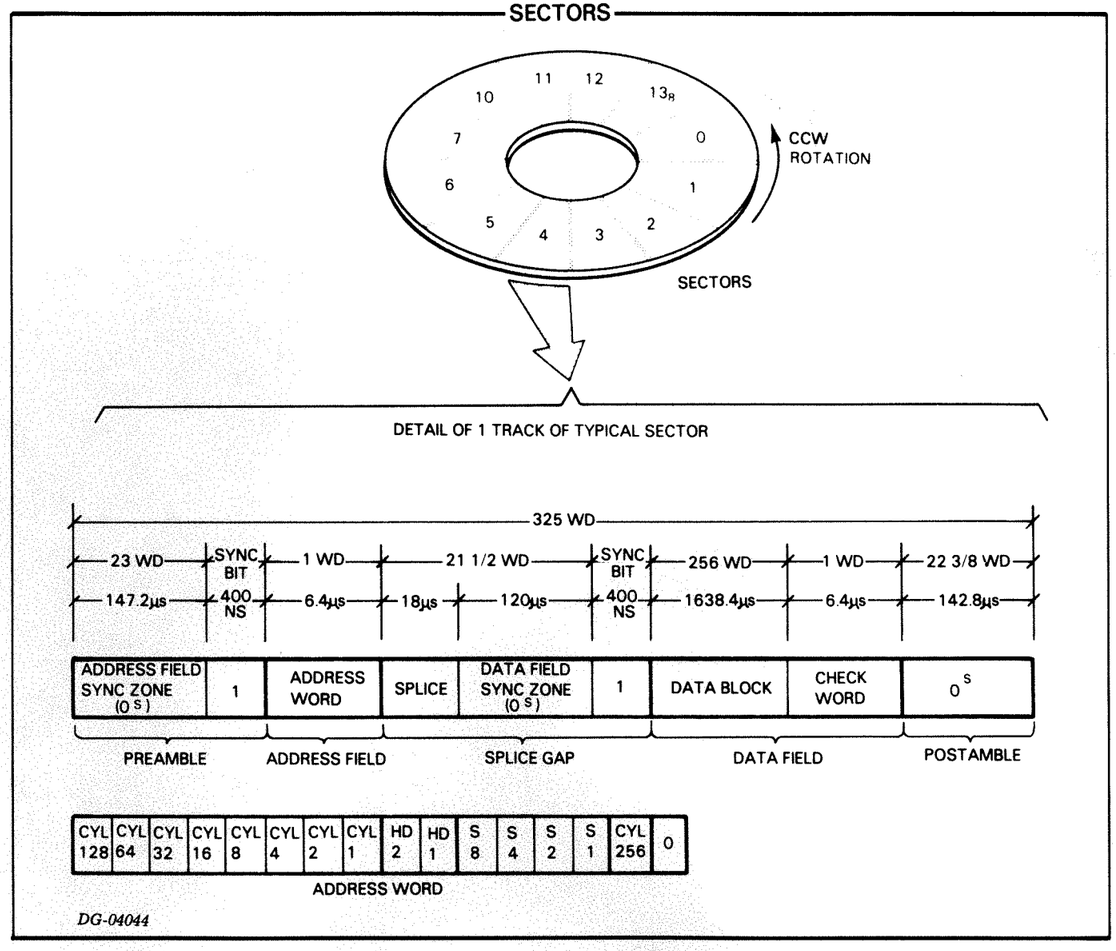


Read/Write Control Logic

The controller directs and times all data transfers. It commands the drive to read or write at the proper times so that a specific sector format is maintained. Each surface is divided into twelve equal sectors shown in the figure at right.

All new discs must be formatted before write operations can executed. The DOC command with the format bit(2) set puts the controller in FORMAT mode, and specifies the sector or consecutive sectors to be formatted. Under certain circumstances an individual sector of a heavily used disc may require reformatting; a sector may be reformatted at any time. The format for each track in a sector has five parts:

- *The Preamble gives the drive time to setup an address transfer. It also allows for some variation in the position of the sector pulse in relation to the beginning of the recorded sector (variations may occur when cartridges are interchanged between drives with differing alignments).*
- *The Address Header indicates the current surface, cylinder and sector. The controller uses this information to check for surface select errors, seek errors and sector address errors. The begining of this field is signalled by a sync bit.*
- *The Splice Gap is the transition area between the address information recorded by a format command and the data field recorded by a write command. These operations are not generally synchronized, especially if the cartridge has been interchanged, so there are usually a number of spurious pulses recorded in this zone. This field is divided into two parts. The Splice Zone contains the splice between pulses written during a write and those written during a format. The Stabilization Zone permits the heads to synchronize with the data recorded on the disc.*
- *The Data Field includes the 256 word data block and a Cyclic Redundancy Checkword. The begining of this field is also signalled by a sync bit.*
- *The postamble allows for variation in the position of the sector pulse, and contains the second splice.*



The timing diagram on the opposite page shows the major signals that control a sector read or write transfer. The preamble and address header timing are the same for both read and write operations. A sector pulse triggers the controller to examine the current sector address received from the drive. If it is the desired sector for a data transfer, the controller sets **Sector Equal** and enters address check mode. It commands the drive to read, and waits 60us for the read circuits to stabilize. The Controller then begins examining the data stream for the sync bit that signals the beginning of the Address Header.

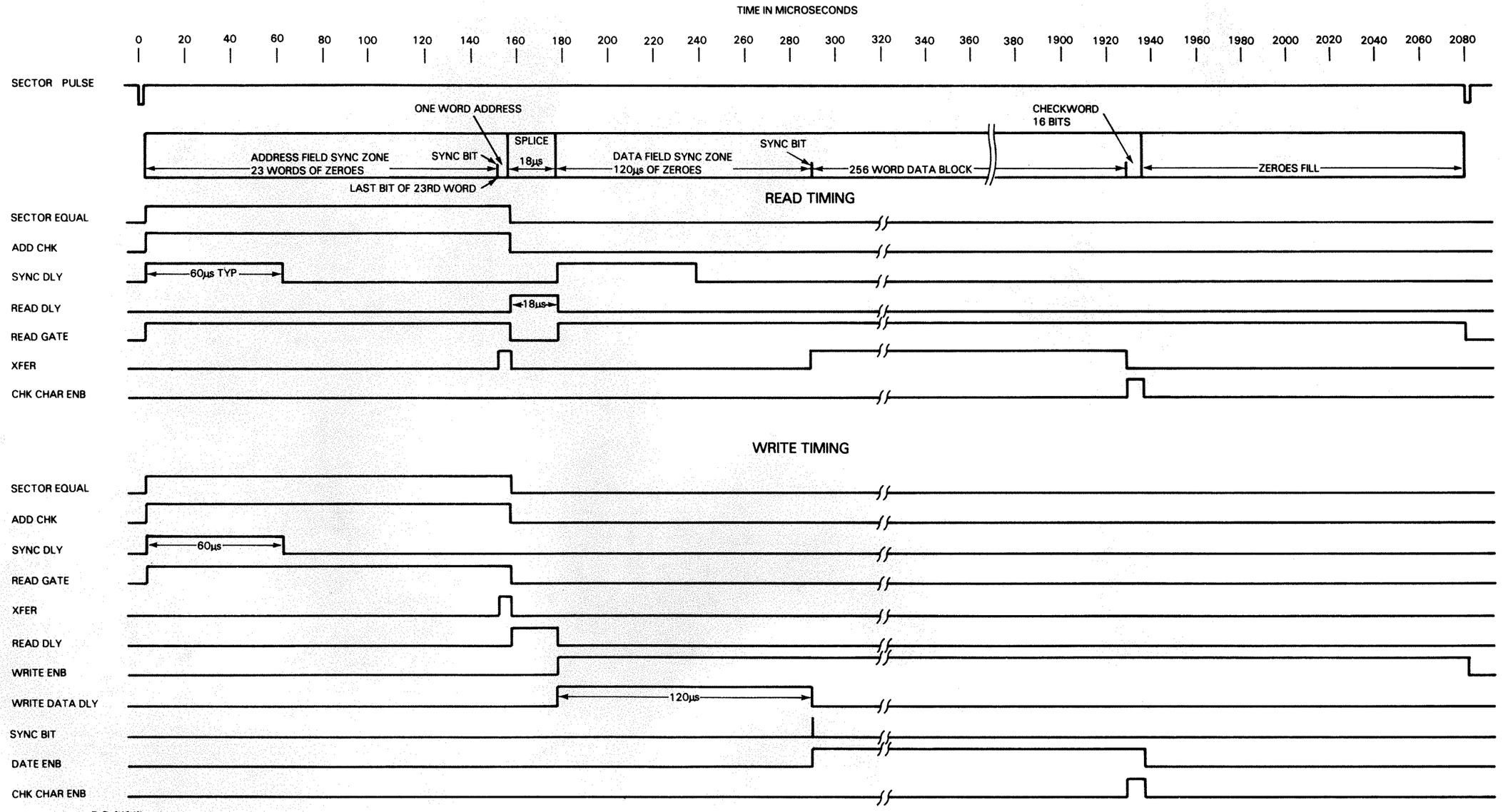
When the sync bit is received the controller reads the one word address and compares it to the address requested by the processor. If the address words differ, the data transfer terminates immediately.

A splice gap follows the Address Header. The next step depends on the type of operation specified.

For a read transfer the controller pauses 60us to allow the read circuits to restabilise (in the Splice Zone the read circuits are turned off to prevent clock discontinuities from affecting the phase locked loop read clock in the drive). A sync bit at the end of the Splice Gap signals the start of the data field. The controller then transfers 256 data words followed by the Cyclic Redundancy Checkword. The read circuits are then shut off for the remainder of the sector.

For a write transfer the controller waits 120us while the heads pause 18us in the Splice Zone then write 0s through the Stabilization Zone. The write circuits record a sync bit to signal the beginning of the Data Field. The 256 data words followed by the checkword are then written to the disc. The write circuits shut down at the beginning of the postamble. (The read circuits are always turned off in the postamble; they ignore the second splice.) Timing diagrams at the back of this chapter show these processes in greater detail.

READ/WRITE TIMING



DG-04047

V

Data Transfer Logic

The following diagram shows the basic controller structure; the upper half shows the data transfer paths and the lower half shows the transfer control logic. To setup a data transfer, the processor specifies a command string (usually a seek followed by a read or write). A seek specifies a drive number, and a cylinder (track) number. A read or write instruction includes a starting surface and sector address, and a sector count. After the drive completes the seek, the controller begins searching for the starting sector. The **Sector Equal** signal initiates the data transfer. The controller then transfers the 256 words of data between the drive and processor memory. Diagrams at the end of the chapter detail data flow timing.

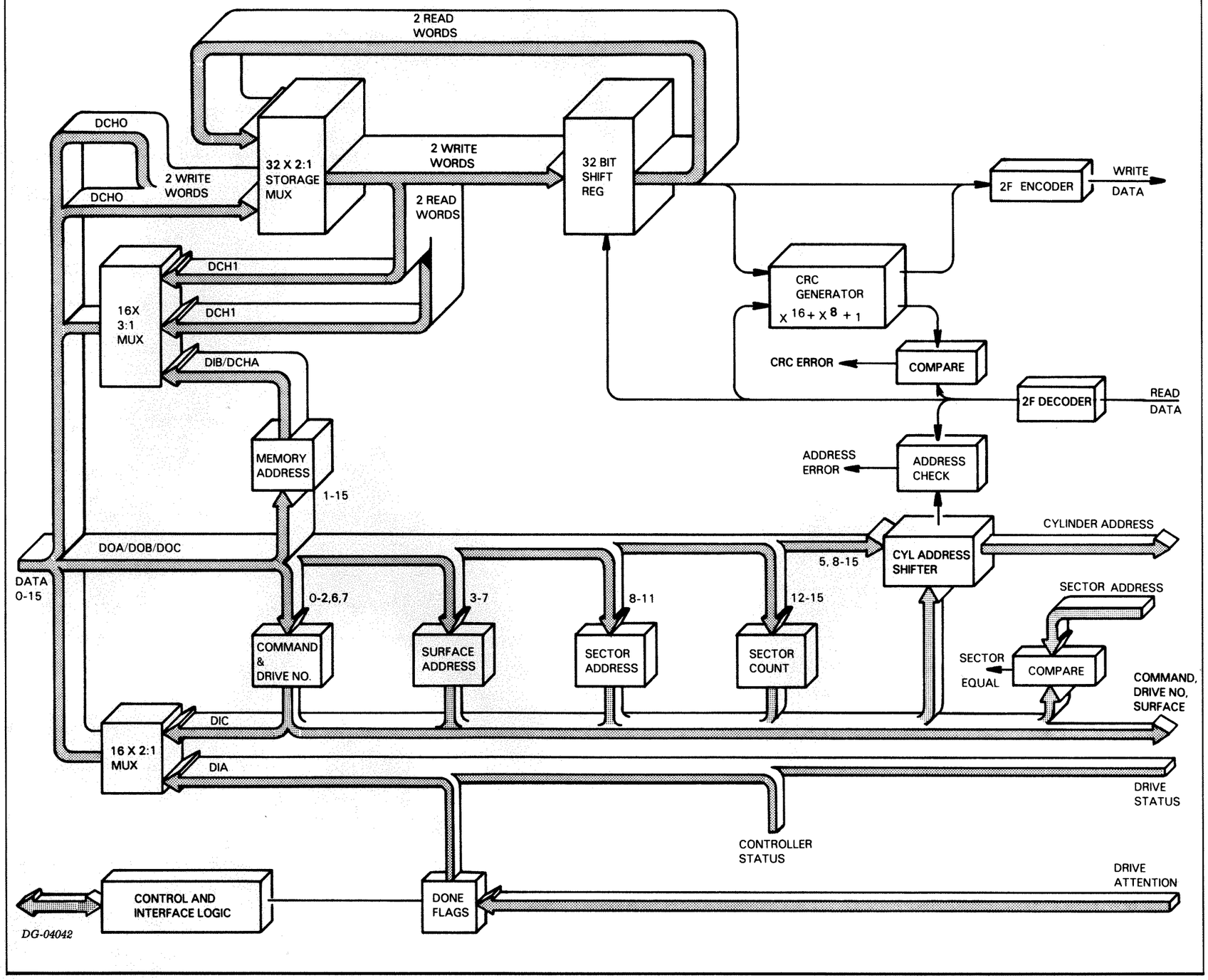
Read

A 32-bit shift register accepts the read data stream. When the register becomes full, it immediately transfers the two words to a 32-bit holding register which buffers the data for a data channel transfer. If the controller shifts in another 32 bits before the holding register is emptied, Data Late sets.

Write

During a write transfer, this system works in reverse. The data channel loads two words into the 32-bit holding register. When the 32-bit shift register becomes empty, it immediately accepts the new data words and begins shifting them to the the data encoder. This frees the holding register to receive two more words. Data Late sets if the controller shifts out all 32 bits before the holding register is refilled.

CONTROLLER BLOCK DIAGRAM



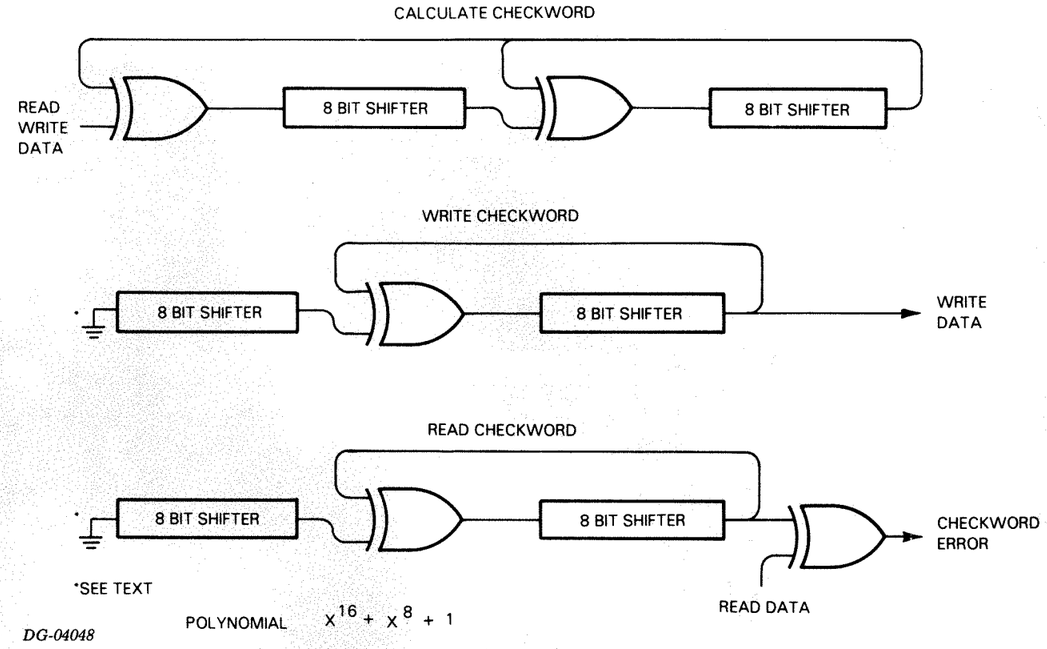
Cyclic Redundancy Check

The controller employs a Cyclic Redundancy Check generator to detect transcription errors. A CRC generator divides the 256 word data stream by a fixed generator polynomial. During a write the final remainder (the checkword) is appended to the data block. When the controller reads, if no transcription errors occur, the remainders will match. This method of error detection catches multiple bit errors that simpler parity check circuits often miss.

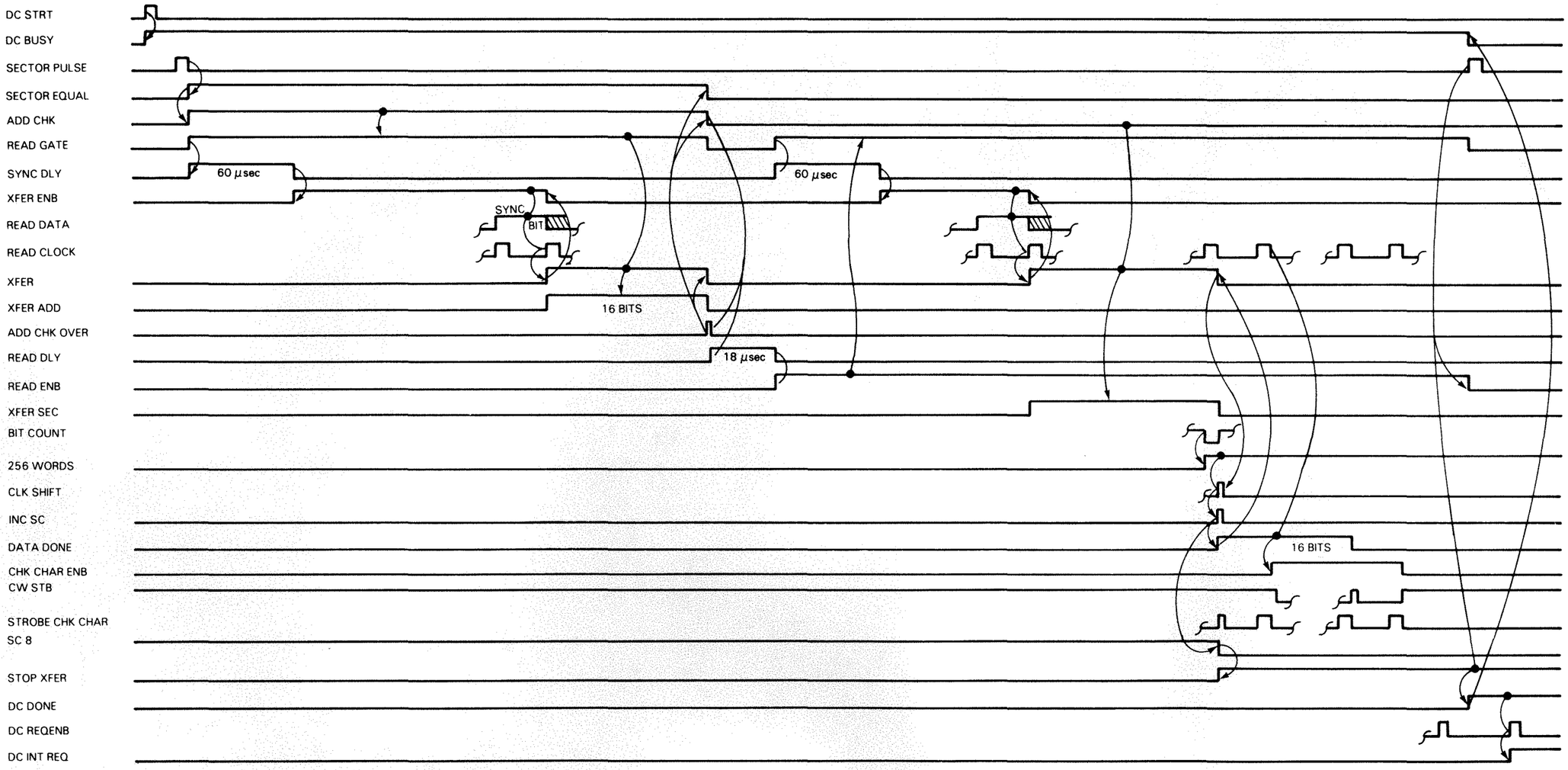
The diagram to the right shows the CRC generator. Feedback to the input and midpoint of a 16-bit shift register conforms to the generator polynomial. During data transfer, the generator processes the serial data stream as it passes to or from the drive. When all 256 words have been transferred, the controller writes the final checkword. When the check word is removed from the CRC generator the contents of the first byte loop back to the midpoint to be xored with the second byte. The second byte is effectively zeroed.

The CRC generator performs the same operation during a read data transfer. When all 256 words have been read, the controller serially compares the output of the generator with the incoming checkword. As the check word is removed from the CRC generator the first byte again loops back to the midpoint to be xored with the second byte. See Appendix F for a more detailed discussion.

CYCLIC REDUNDANCY CHECK

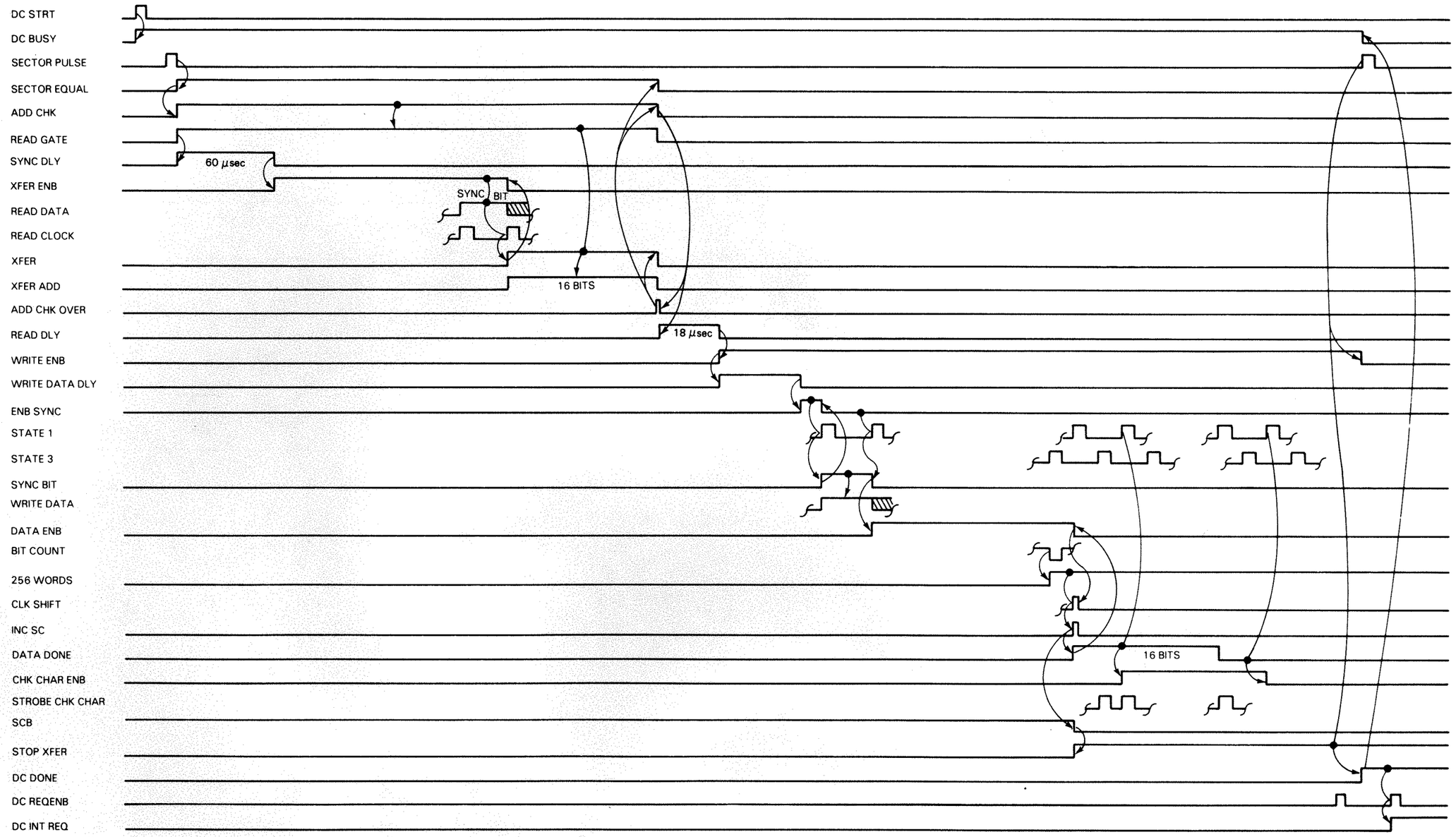


READ CONTROL TIMING



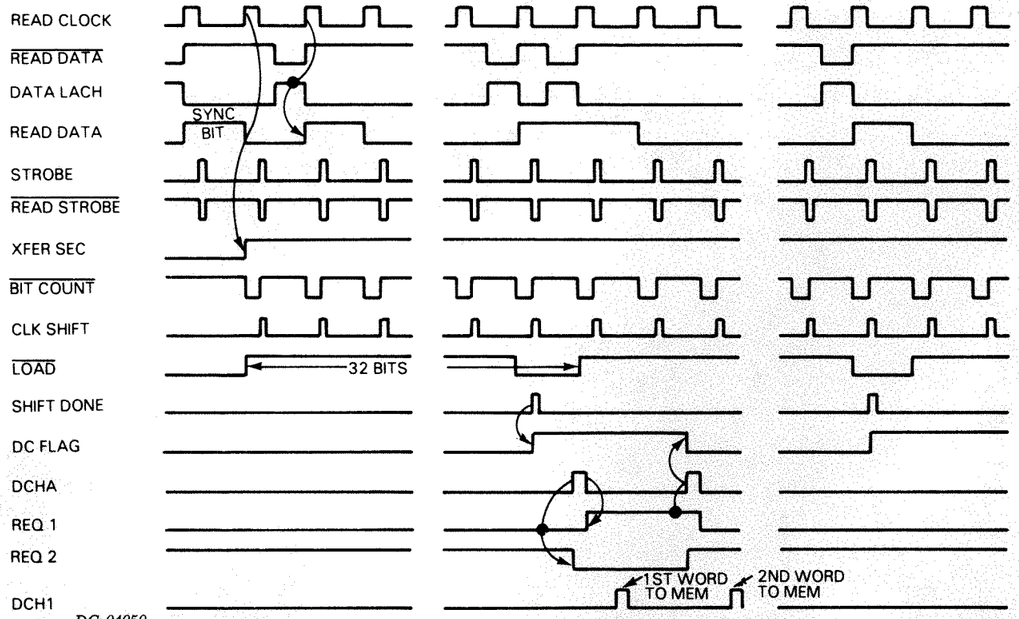
DG-04051

WRITE CONTROL TIMING



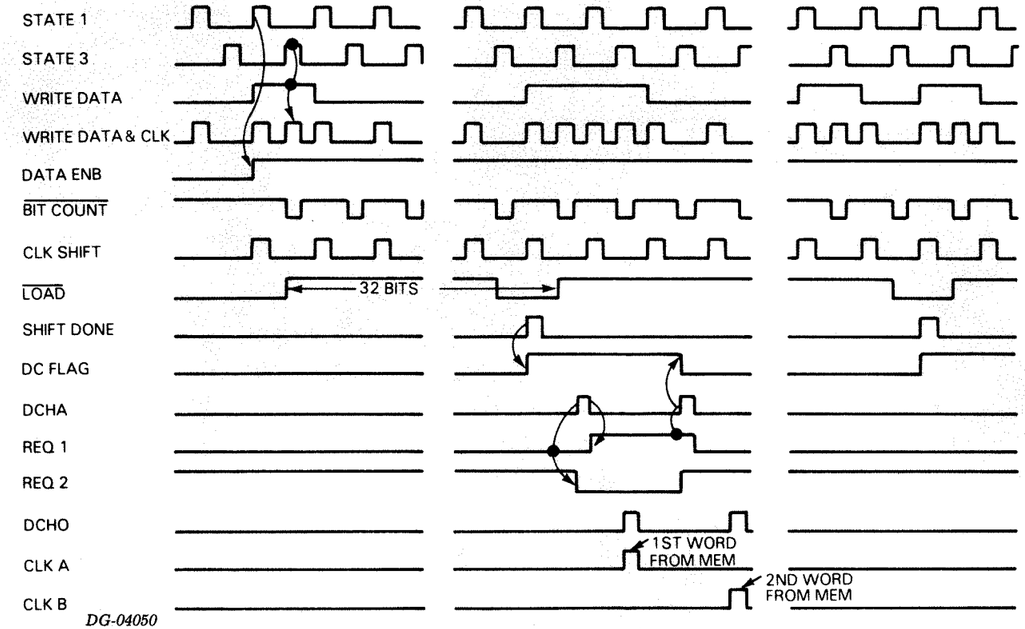
DG-04052

READ DATA TIMING



DG-04050

WRITE DATA TIMING



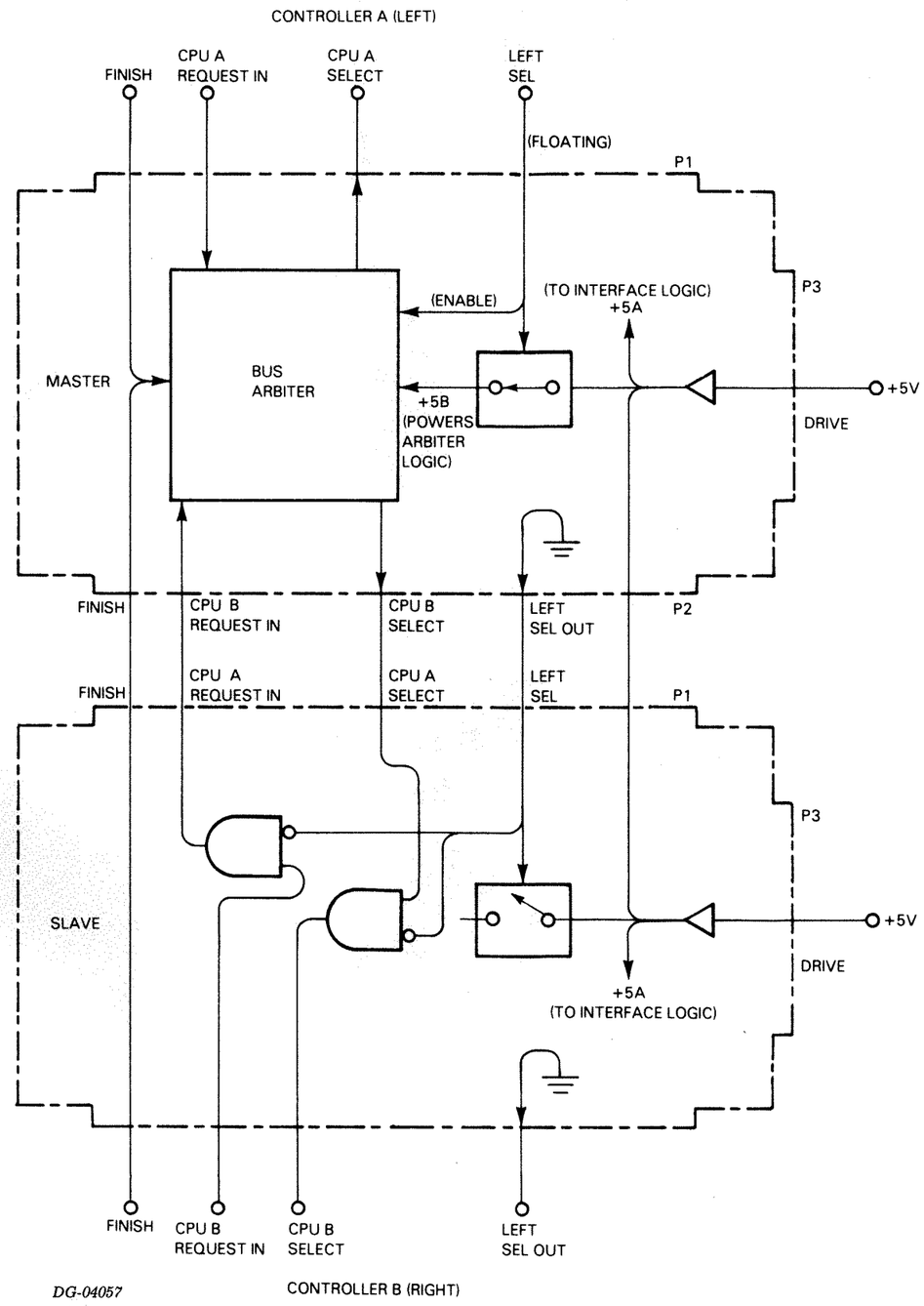
DG-04050

CHAPTER VI
INTERFACE

INTRODUCTION

The diagram to the right shows a simple case of two interfaces interconnected in a dual drive subsystem. You may extrapolate more complex subsystems by adding interfaces similar to the slave at the bottom of the diagram. The interfaces receive power from the drives and are both energized if either drive is powered up (+ 5A). The left select line applies power (+ 5B) to the arbiter logic in the leftmost interface. The left select line switches the remaining arbiter to repeater mode and it passes the request and select signals directly through.

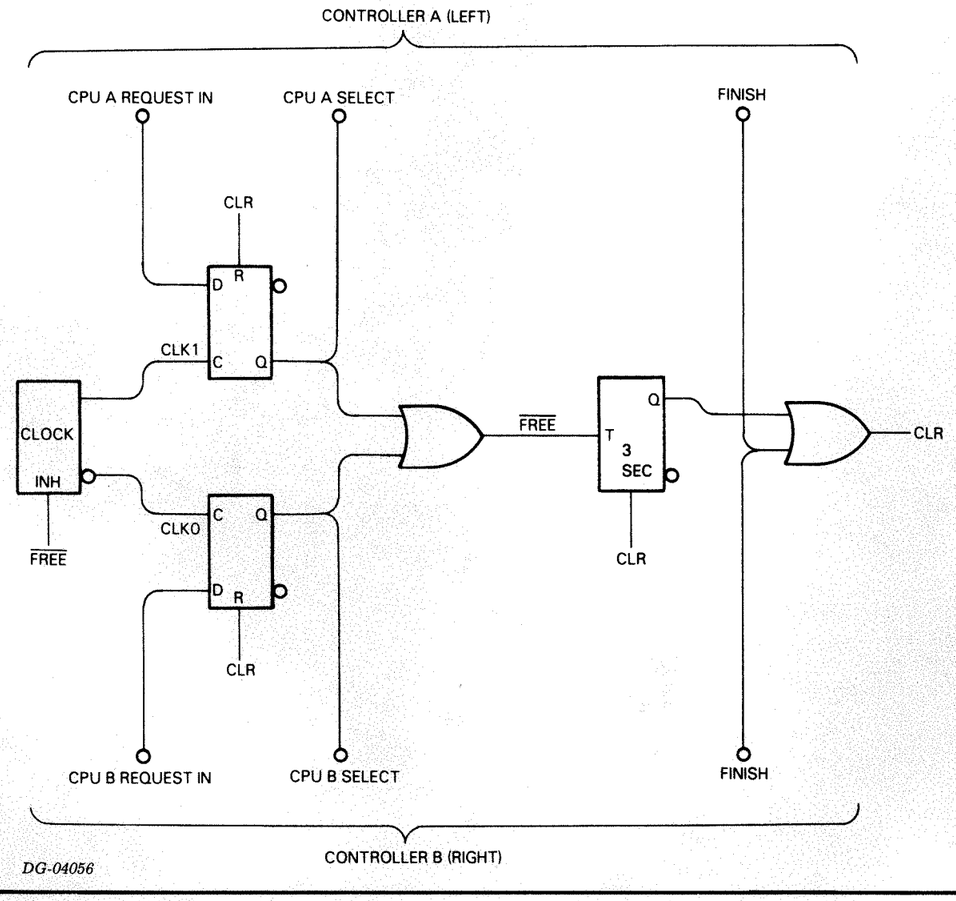
INTERCONNECTION & PRIORITY LOGIC



Bus Arbiter

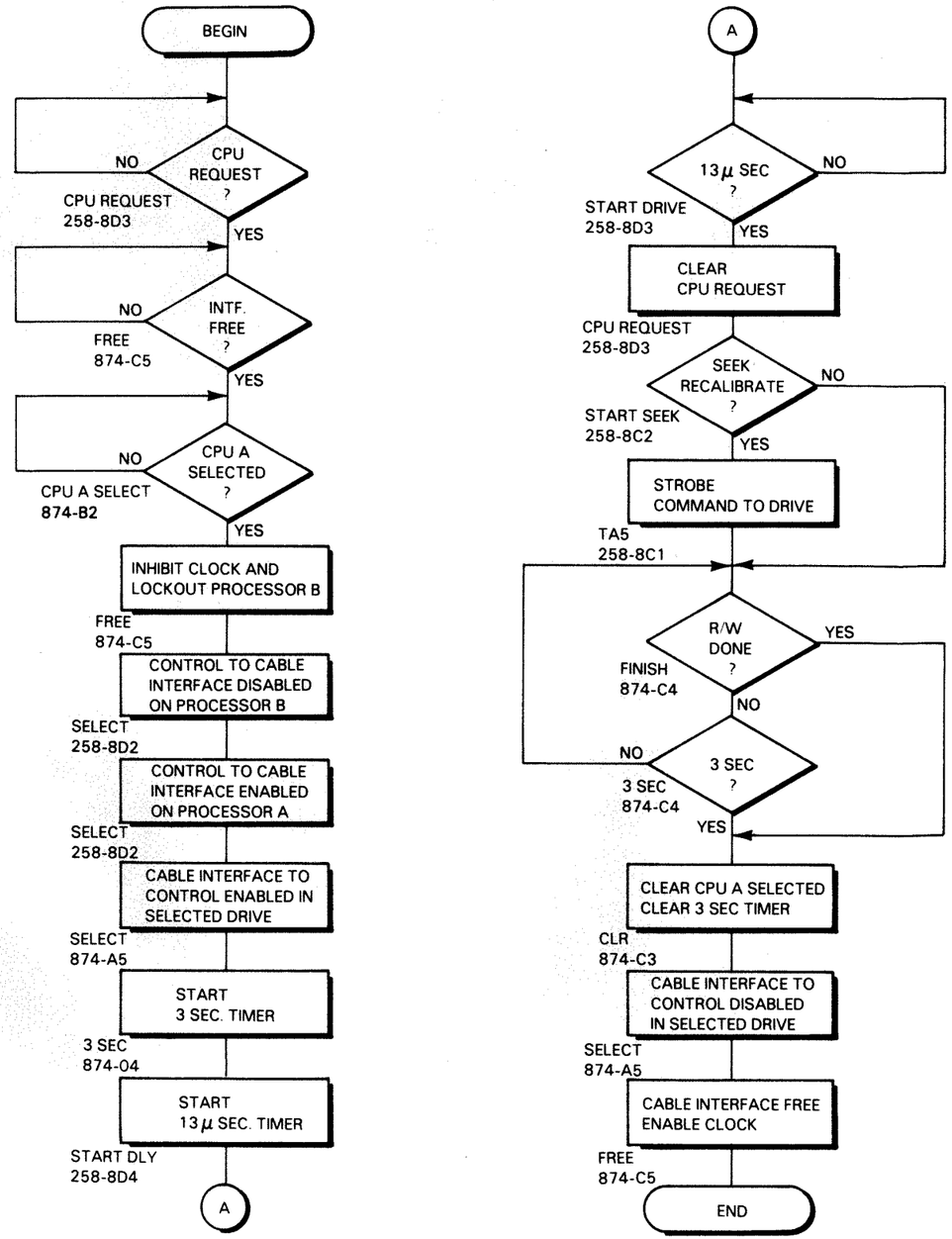
The arbiter logic appears below. Let us assume the left processor (CPU A) requests access first. Output from the arbiter clock alternately strobes the two request flops. When the request arrives (**CPU A Request In**) the select flop sets (**CPU A Select**) This disables the clock (**Free**), locks out CPU B, and starts the three second timer. When the controller finishes the operation, or the three second time period elapses, the select flop is reset (**Clear**), which in turn enables the clock. The flow chart at right covers this process in detail.

BUS ARBITER LOGIC



DG-04056

DUAL PROCESSOR ACCESS FLOW DIAGRAM*



REF PRINTS
DGC NO.001-000874 & 001-000258

DG-04055

*ASSUMES PROCESSOR A (LEFT) REQUEST. IF PROCESSOR B, INTERCHANGE A & B

CHAPTER VII
DRIVE: SPINDLE AND MONITORS

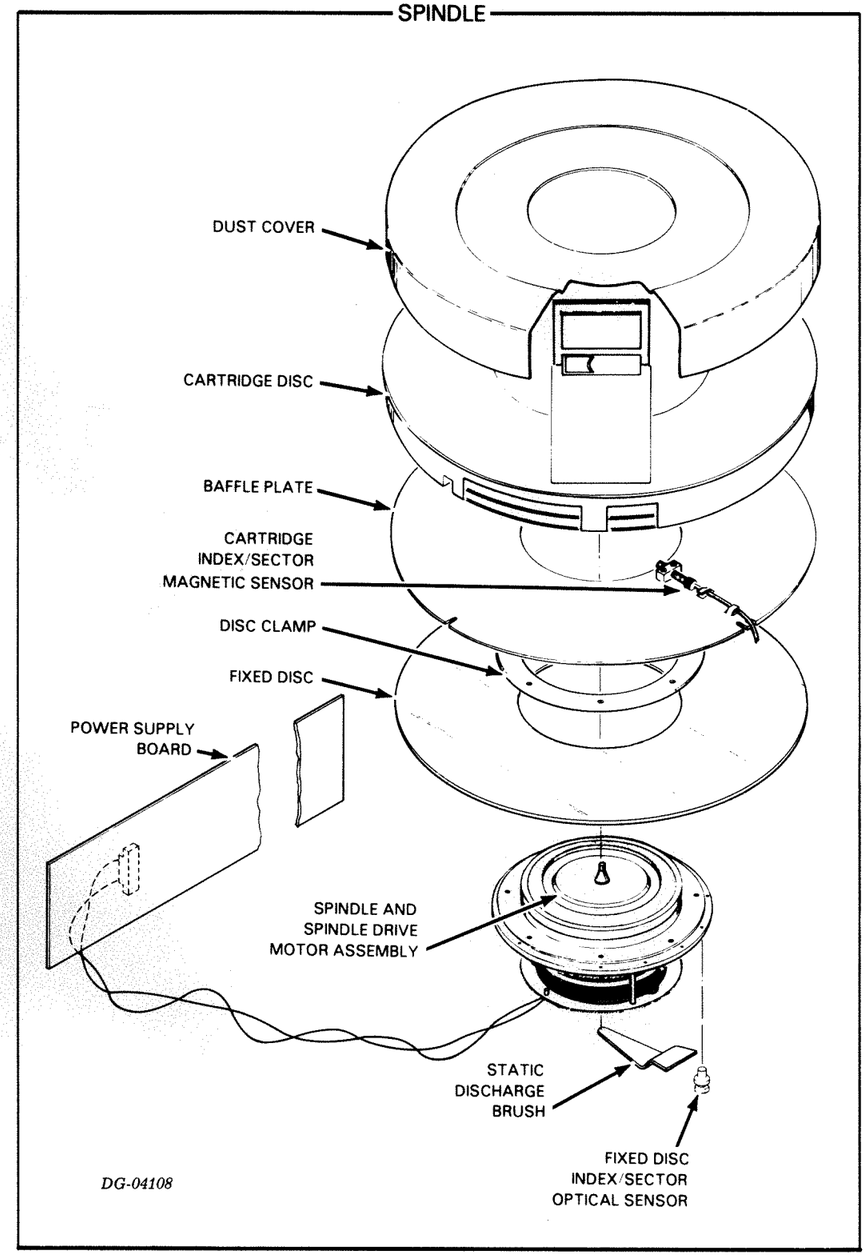
SPINDLE ASSEMBLY

The spindle assembly shown to the right includes a spindle and drive motor to support the recording discs and rotate them at 2400 rpm. The motor is mounted directly on the spindle shaft; the entire assembly is mounted in a protective cavity.

The upper end of the spindle has a flange and a ring-shaped permanent magnet. The fixed disc is held to the flange by four retaining screws. The cartridge disc has a metal hub which clamps to the permanent magnet and becomes a temporary magnet. A tapered pin centers the disc, and a handle on the top of the cartridge is used to lift it free of the magnet.

Any static charge collected on the discs will discharge to ground through the static discharge brush. A steel strap, fastened to the base plate presses against a graphite button on the lower end of the spindle thus providing an electrical ground.

The spindle and motor assembly is serviced as a unit, and should not be disassembled. It is keyed to the baseplate precisely so that no adjustment is necessary during replacement.

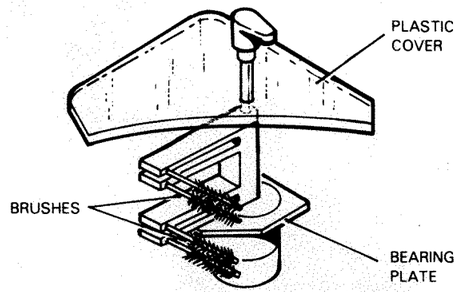


BRUSH MECHANISM

The brush assembly cleans loose particles from the disc surfaces during spindle runup. It is activated after the blower has developed full air flow and the spindle has nearly reached operating speed, but before the heads are loaded. Nylon brushes sweep across the disc surfaces and then retract. The air stream from the blower picks up any debris dislodged during the brush cycle and carries it out of the disc cavity.

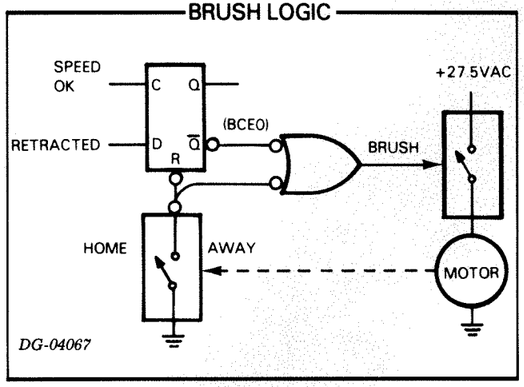
The brush assembly consists of four nylon brushes (one for each disc surface), supported as shown on a vertical shaft which is rotated by a stall/reverse motor. The brush control logic activates the motor which rotates the shaft so that the brushes swing into the disc cavity and sweep across the discs. After the shaft has rotated approximately 90 degrees, the assembly strikes a solid stop. This stalls the motor, and it automatically reverses and retracts the brushes. When fully retracted, the brushes activate the brush home microswitch.

BRUSH ASSEMBLY

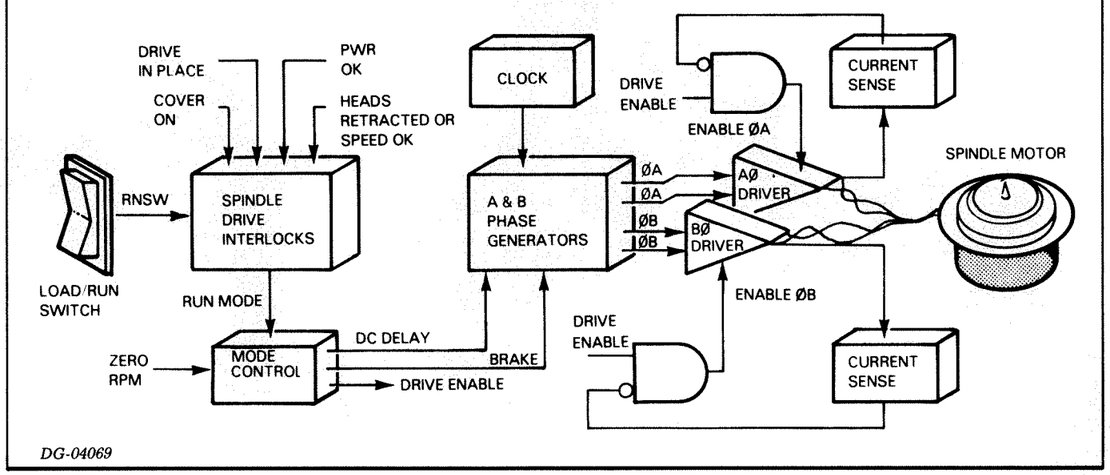


The diagram below shows the brush control circuits. The cycle starts when the spindle comes up to speed at the beginning of a run cycle. The Brush Cycle Execute (**BCE0**) signal activates a triac that connects 27.5Vac to the brush motor. When the brushes swing out of the retract position, the brush home switch clears **BCE0** but maintains the cycle. When the brushes complete the cycle, the home switch opens, deactivating the brush motor.

BRUSH LOGIC



SPINDLE CONTROL BLOCK DIAGRAM



Spindle Drive

The spindle motor control circuits, shown above, generate analog signals to operate the spindle motor. They include the spindle drive interlocks, the A and B phase generators, the spindle motor drivers and the current limiters.

The **Run Mode** signal is asserted, thus activating the spindle when the drive interlocks are in either of two states. Prior to **Speed OK** the spindle will start when the run switch is depressed, if both the drive and its protective dust cover are in place, power is ok, and the heads are retracted. Once **Speed OK** is asserted, the heads need not be retracted to maintain **Run Mode.** The run signal enables the phase generators, which provide a two phase drive signal to power the hysteresis synchronous motor. The phase generators divide the master clock and produce two 80hz waveforms called **Phase A** and **Phase B.** The two signals control drivers that switch current in the two motor poles.

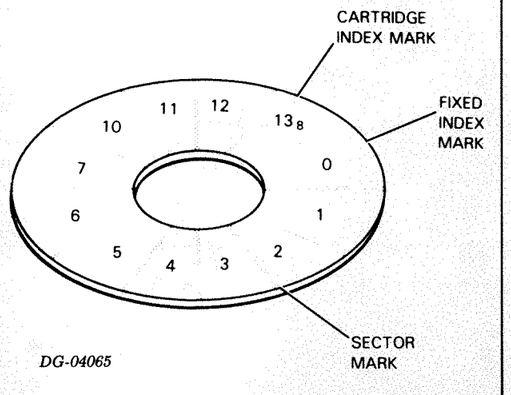
Each motor driver alternates the voltage polarity across the associated motor pole, and the motor inductance causes triangular current waveforms. If current exceeds a preset maximum, current limiters momentarily disable the drivers to prevent damage to both them and the motor.

The drive interlocks disable spindle operation when the run switch is returned to the load position or an interlock is violated. The **BRAKE** signal reverses the phase relationship between **Phase A** and **Phase B,** dynamically braking the motor. When the **Zero RPM** signal indicates that the spindle has nearly stopped, the **DC Delay** signal resets the phase generators, and direct current flows through the motor windings to complete the braking cycle. The **Drive Enable** signal disconnects the motor drivers after the spindle stops.

Sector Counter

Each disc surface is divided into twelve sectors shown in the figure below. There is a sector mark that indicates the beginning of each sector, and an index mark to locate sector zero. The index mark for the cartridge disc appears in sector 13_8, and the mark for the fixed disc is in sector zero. Since there is no set mechanical relationship between the fixed disc and cartridge disc, the drive contains two sector counters.

SECTOR ALLOCATION



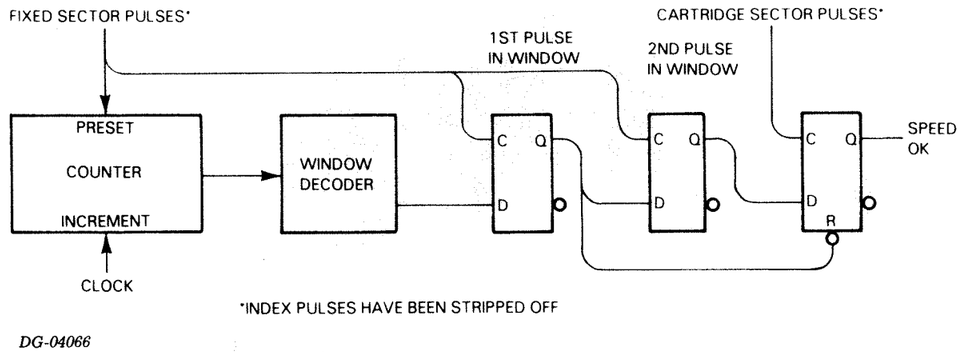
DG-04065

The block diagram to the right shows the sector mark detectors and sector counters. A reluctance pickup senses slots in the temporarily magnetized hub on the cartridge disc, and an optical pickup senses holes in a plate below the fixed disc. Pulse shapers deliver the recovered signals to timing logic which separates the sector and index marks and checks the spindle speed. Each sector pulse increments its respective sector counter, and index pulses initialize the counters (the drive employs divide by 12 counters, so the index pulses are not needed once the spindle is up and running). The most significant bit of the head address selects the appropriate counter during a data transfer.

Speed Detector

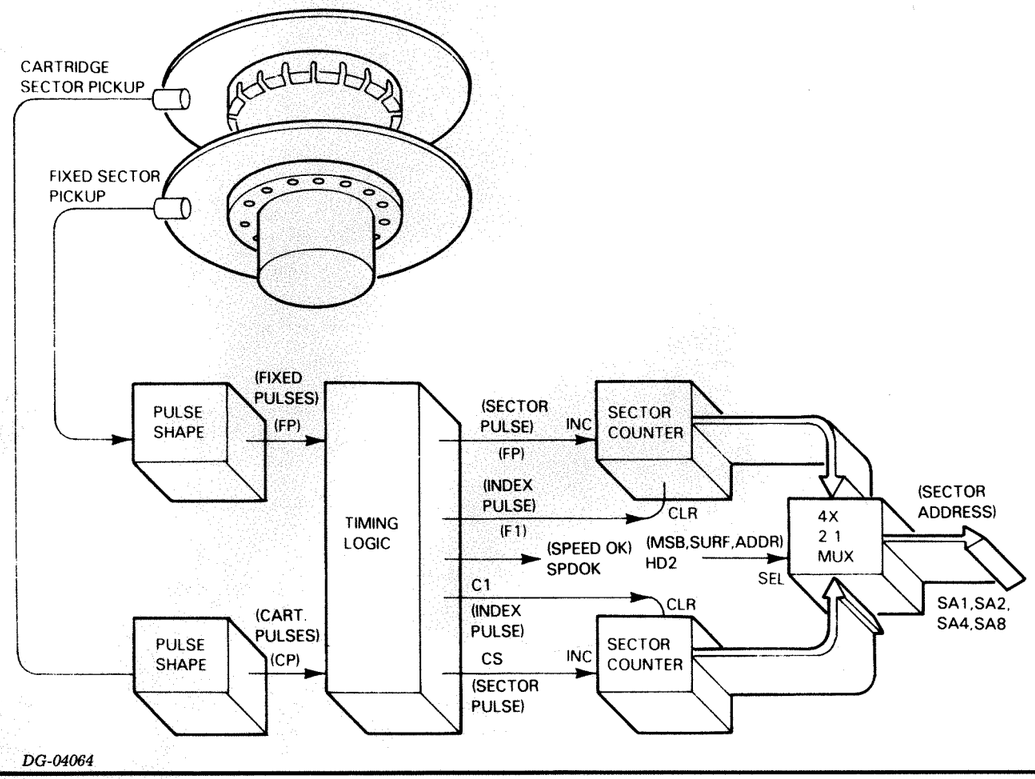
The spindle speed detector compares the rate of sector pulses from the fixed disc to a precision clock. A window circuit checks for a rate between 1.64 and 2.46msec per pulse. This corresponds to a speed range between 3060 and 2040rpm. The speed detector asserts **Speed OK** when two consecutive fixed sector pulses fall in this window and sector pulses for the cartridge are also present. (If a cartridge is not installed, **Speed OK** will not assert and the drive will not load the heads.)

SPEED DETECTOR BLOCK DIAGRAM



DG-04066

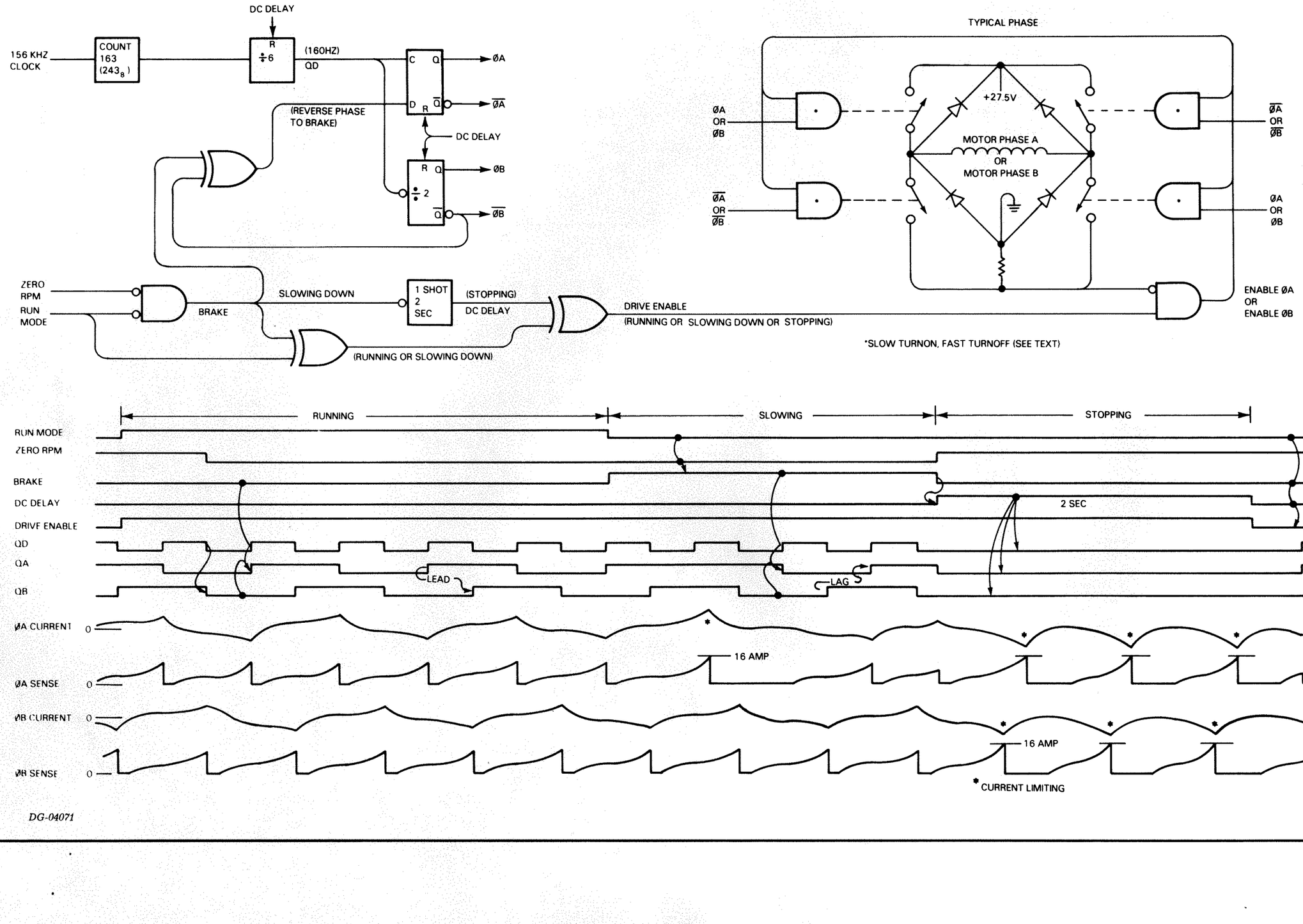
SECTOR COUNTER BLOCK DIAGRAM



DG-04064

VII

SPINDLE CONTROL & TIMING



Spindle Drive - some details

The spindle drive circuits include the control logic, phase generators and motor drivers shown in the figure to the left. The timing diagram shows four operational states: run, brake, stop, and disable. The control logic decodes these states from the **Run Mode** and the **Zero RPM** signals.

The phase generators control the motor in run mode. In this mode **phase A** leads **phase B** by 90 degrees. The frequency and phase relationship of these two signals causes synchronous counter-clockwise rotation. The phase generators also control the motor in brake mode, but the phase relationship is reversed (**phase B** leads **phase A** by 90 degrees). This brakes the motor by accelerating it in a clockwise direction. When the spindle speed falls below 47.5rpm, the **Zero RPM** detector triggers a 2 second **DC Delay** signal that resets the phase generators. This causes a direct rather than alternating current flow through the motor windings and brings the spindle to a halt. The control logic disables the motor drivers when the delay times out.

The phase generators accept a 156.25KHz clock signal derived from the drive's master clock. Two counters divide this signal by 163 x 6 = 978 to produce a 160Hz clock. An additional counter divides the 160Hz clock by two to produce the 80Hz **phase B** signal. Feedback from **phase B**, along with the **brake** signal, establishes the relationship of **phase A**. If the **brake** signal is low, phase A sets after phase B clears (A leads B). If the brake signal is high, the polarity of the feedback signal is inverted and the phase relationship reverses.

Each motor phase is driven by an H-bridge, so called because the current paths resemble the letter H. The H-bridge alternates the direction of current flow in the motor winding. When the phase signal is high, current flows from the +27.5 volt supply, through the upper left branch of the H, across through the motor winding, down through the lower right branch of the H and through the current sensing resistor to ground. When the phase signal is low, current follows the opposite path and therefore flows in the opposite direction through the coil. The coil is inductive, so the current waveform is triangular. If we arbitrarily assume the left side of the coil to be positive, then current steadily increases in the positive direction when the phase signal is high, and in the negative direction when the phase signal is low, and the average current is zero. Current always returns to ground in the same direction through the current sensing resistor, so the resulting current sense voltage is rectified.

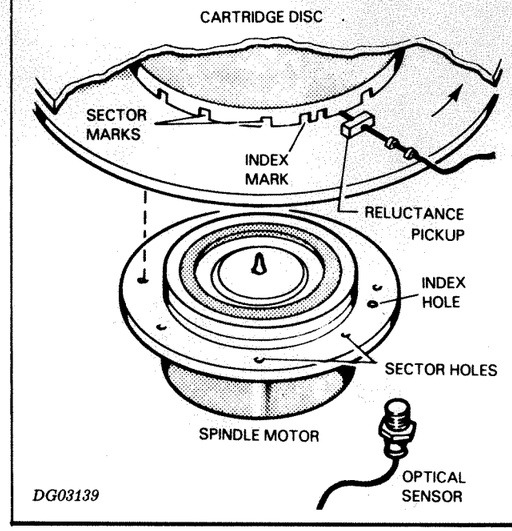
An H-bridge can cause a direct short circuit to ground when it switches. Consider the case where the phase signal goes low. If the lower left leg turns on before the upper left leg turns off, the bridge closes a current path directly through the sense resistor to ground. The switches are therefore designed to turn off faster than they turn on. Because this interrupts the coil current, flyback diodes connect the coil to the supply and ground during commutation. This prevents dangerously high back emf voltages that could damage the switches. (Note that this causes flat spots in the current sense waveform.)

A current limiter turns the H-bridge off if the current level becomes too high. If the current level exceeds 16 amps, a one shot disables the drivers for 2.25 msec, and current decays through the flyback diodes.

Spindle Monitor - some details

Sector transducers - The diagram below shows a cutaway view of the sector mark transducers which generate signals used for hard sensing of sector boundaries and rotational speed. One transducer is an optical sensor mounted in the baseplate. It senses holes in the spindle flange which supports the fixed disc. Twelve holes are evenly spaced to correspond to sector positions; an extra hole indicates the index position. The second transducer is a magnetic sensor mounted on the baffle plate and triggered by the magnetic field radiating from slots in the hub of the cartridge disc. (The source of the magnetic field is the permanent magnet used to clamp the cartridge disc to the spindle). These slots, like the holes in the spindle flange, indicate the sector and index positions.

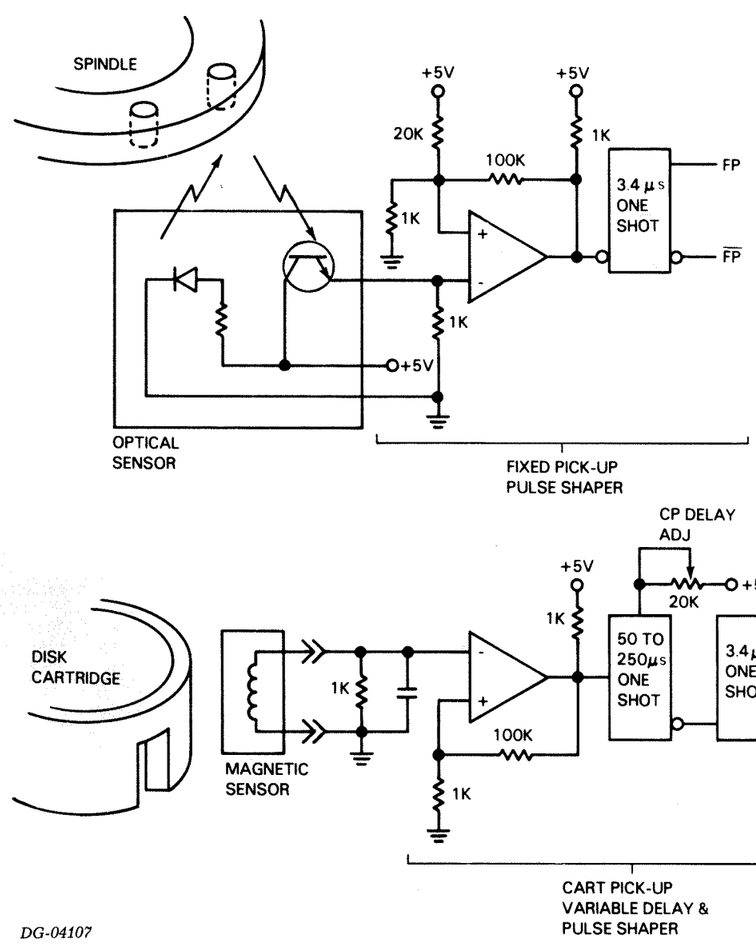
SECTOR TRANSDUCERS



The diagram below shows the circuits that recover and amplify the sector pulses. An amplifier receives current pulses from the optical pickup transistor and triggers a 3.4us one shot. The resulting fixed pulses clock the spindle speed detector, the spindle speed low detector and the fixed sector counter.

Another amplifier receives current pulses from the magnetic pickup coil. The amplified pulses trigger a delay oneshot which can be adjusted to maintain pack interchangeability. (Different drives have varying transducer sensitivity; therefore, the pulse position tends to move. The delay oneshot cancels these variations to prevent a sector transfer from starting too late or ending too early.) When the delay oneshot times out, it triggers a 3.4us one shot. The resulting cartridge pulses enable the spindle speed detector and clock the cartridge sector counter.

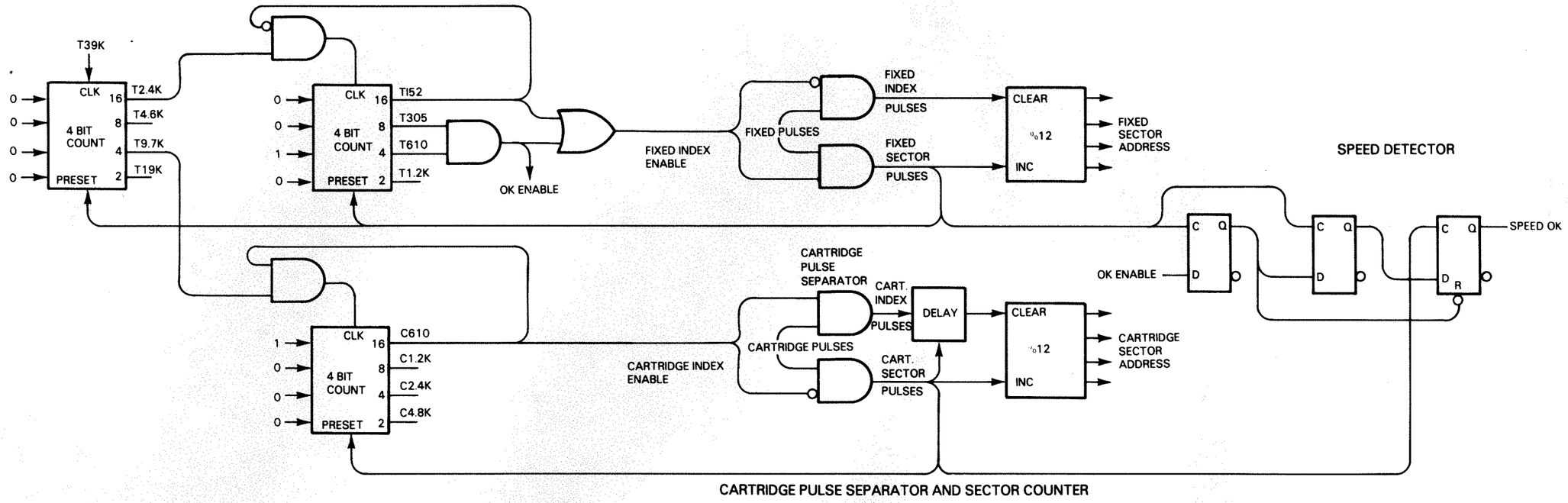
SECTOR DETECTORS BLOCK DIAGRAM



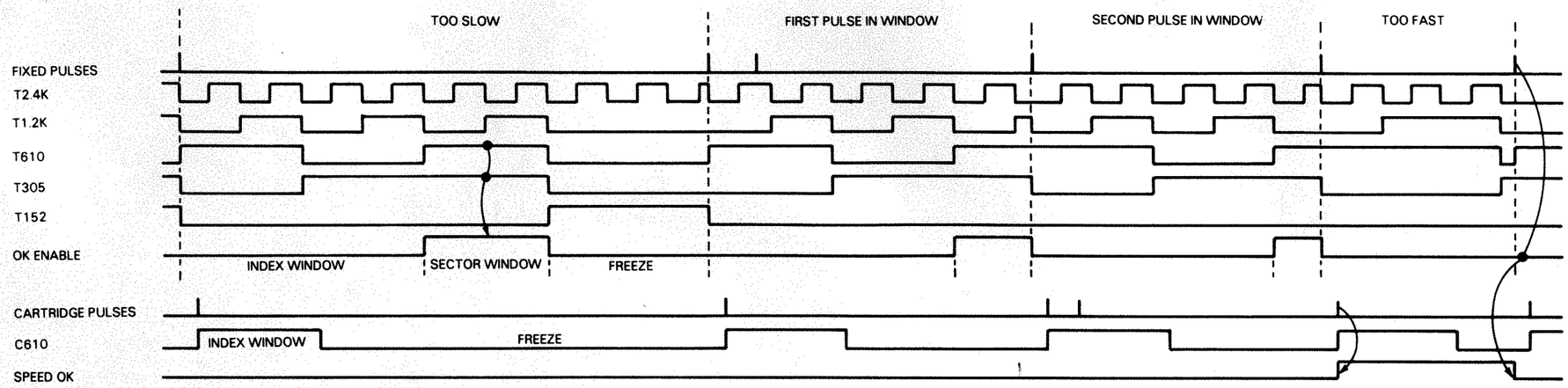
VII

SPINDLE SPEED MONITOR AND SECTOR COUNTERS

FIXED PULSE SEPARATOR AND SECTOR COUNTER



CARTRIDGE PULSE SEPARATOR AND SECTOR COUNTER



DG-04070

Spindle Speed Monitor and Sector Counters - The spindle monitor circuits are detailed in the figure on the opposite page. The fixed disc circuits appear at the top and include the speed monitor, the index and sector pulse separator, and the fixed sector counter. The cartridge circuits at the middle of the page include the index and sector pulse separator, and the cartridge sector counter. Signals from both sections combine in the spindle speed detector at the right.

The fixed pulse separator isolates index and sector pulses. The spindle speed monitor checks that frequency of sector pulses (and thus the spindle speed) falls within an acceptable range. The speed monitor uses an eight bit counter to define time windows. If the spindle speed is in the normal operating range, the index and sector pulses will fall within these windows.

The timing process starts when a sector pulse presets the counter, and a 39khz clock increments the counter. The four least significant bits define the seven states shown below. If it reaches the seventh state before a sector pulse appears, the counter freezes, to prevent it from cycling through the states again. Each state represents a time lapse of 409.6us.

SIGNAL NAMES	INDEX PULSE WINDOW				SECTOR PULSE WINDOW		
T152	0	0	0	0	0	0	1
T305	0	0	1	1	1	1	0
T610	1	1	0	0	1	1	0
T1.2	0	1	0	1	0	1	0
		PRESET				FREEZE	

The sector pulse window defines a time lapse between 1638.4us and 2457.6us, and this corresponds to a speed range between 3050rpm and 2033rpm. If the speed is too low, the freeze count is reached, and T152 goes high and locks out the clock. The count recycles when the next sector pulse appears and presets the counter.

Decoders detect the count states and control the fixed sector counter. If an index pulse falls in the index window, the fixed index (**FI**) signal clears the sector counter. Similarly, if a sector pulse falls in the sector window, the fixed sector (**FS**) signal increments the counter.

Cartridge sector pulses trigger the cartridge pulse separator. A four bit counter accepts a 9.7kHz clock which is derived from the drive's master clock. The counter defines a time window for the index pulse, and then freezes until a sector pulse presets it and restarts the cycle. The counter defines the nine states shown below. Each state represents an elapsed time of 102.4us.

SIGNAL NAMES	INDEX PULSE WINDOW								SECTOR PULSE WINDOW
C610	1	1	1	1	1	1	1	1	0
C1.2	0	0	0	0	1	1	1	1	0
C2.4	0	0	1	1	0	0	1	1	0
C4.8	0	1	0	1	0	1	0	1	0
		PRESET						FREEZE	

The freeze count is always reached during normal operation, and **C610** goes low and locks out the clock. The count recycles when the next sector pulse appears. A decoder detects the count states to control the cartridge sector counter. If an index pulse falls in the index window, the Cartridge Index signal (**CI**) arms a delay circuit and enables the next sector pulse to clear the counter (recall that the cartridge index pulse falls in sector 13_9) Subsequent Cartridge Sector (**CS**) pulses increment the counter.

Fixed and cartridge sector pulses combine in the spindle speed detector. A three stage shift register stores two consecutive fixed pulses that fall in the speed range, and shift the result to the third stage when a cartridge pulse appears. The register clears if any subsequent fixed pulse falls outside the speed range. Note that **Speed OK** cannot set if a cartridge disc is not installed.

Zero RPM Timer

A separate timer checks the spindle speed during a braking cycle. It is constructed around a counter that is clocked by the 305Hz output from the fixed sector timer (**T305**), and cleared by fixed sector pulses. The counter indicates **zero rpm** when the frequency of sector pulses drops to the point where it is allowed to overflow.

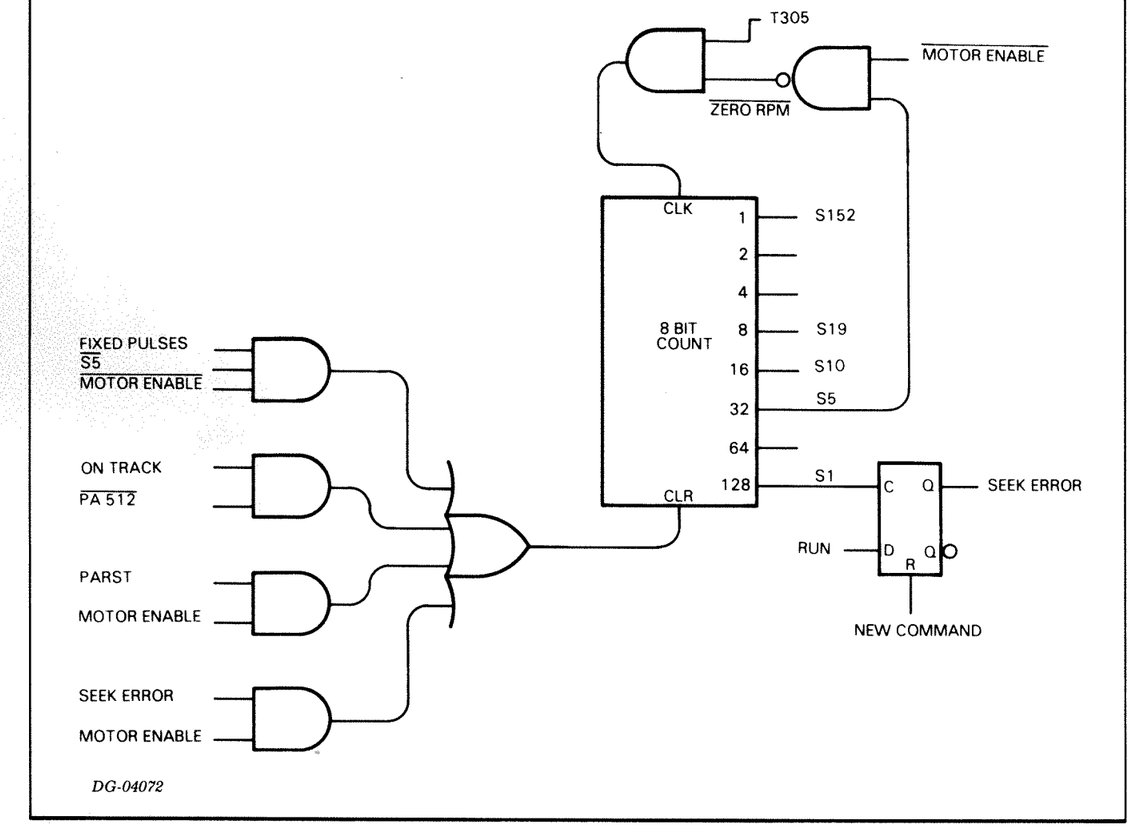
When Motor Enable goes low to initiate a braking cycle, the clock lockup and preset on the fixed sector timer are released. This allows **T305** to free run at 305Hz (it normally runs at 480Hz, due to preset). The zero rpm counter divides **T305** by 64 to yield a signal called **S5**. As the spindle slows down, the time interval between sector pulses increases. When the interval becomes long enough to allow the timer to reach a count of 32, feedback from **S5** locks out clock and clear pulses. The counter therefore freezes and signals zero rpm at a threshold speed of:

305/32 x 1/12 x 60 = 47.5rpm

The timer also monitors positioner operations. The counter divides **T305** by 256 to yield a signal called **S1** which has a half cycle period of 264ms (remember that while the spindle is running, the frequency of **T305** is 480Hz). When a seek operation begins, the **On Track** signal goes low and releases the counter. If the counter asserts **S1** before the positioner detents on the new track, **Seek Error** sets and locks the counter until the drive receives a new command or is shut down.

When a load or recalibrate operation begins, the present track address reset signal (**PARST**) clears the counter. When the heads reach the outside edge of the data zone, **PARST** goes low and the counter starts. **Seek Error** sets if the counter asserts **S1** before the positioner goes on track.

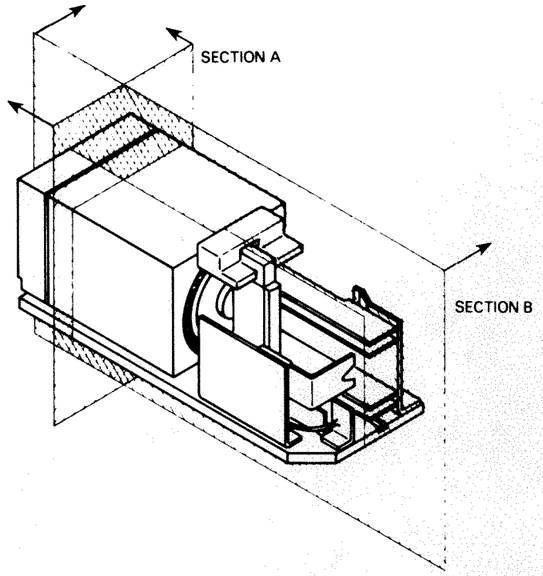
ZERO RPM AND SEEK TIMER

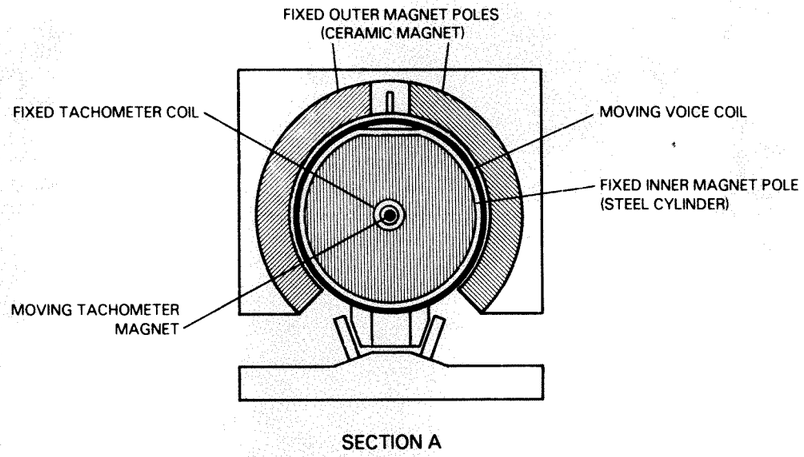


DG-04072

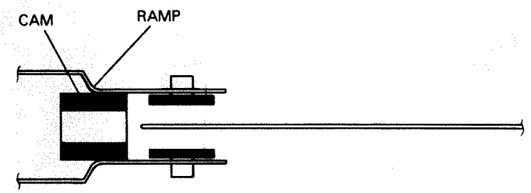
VII

HEAD POSITIONER

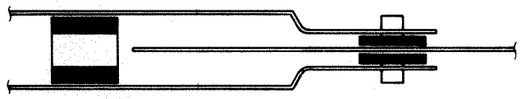




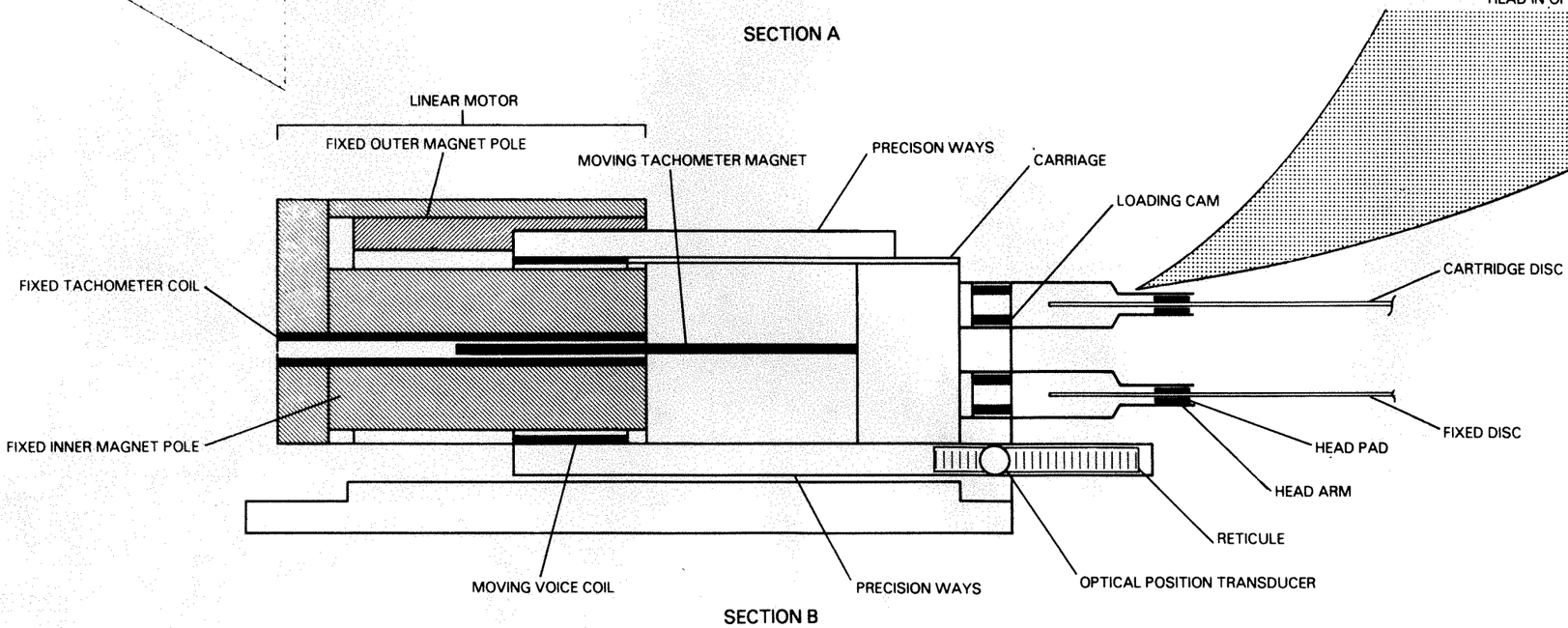
SECTION A



HEAD IN RAISED POSITION



HEAD IN OPERATING POSITION



SECTION B

DG-04074

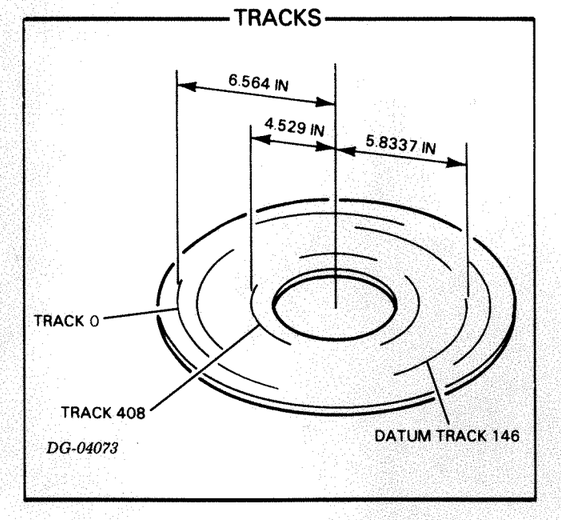
CHAPTER VIII
DRIVE: HEAD POSITIONER AND SERVO

INTRODUCTION

The cartridge disc head positioner incorporates a linear motor actuator to locate the heads over selected tracks. The head positioner assembly is an integral unit and mounts on a doweled plate that bolts to the base casting. The following components are included in the positioner assembly shown on the opposite page:

- *linear motor*
- *head carriage and precision ways*
- *heads*
- *loading cams*
- *tachometer (motor velocity sensor)*
- *optical position transducer and lamp*
- *full retract sensing microswitch (not shown)*

The linear motor drives the head carriage along the precision ways under servo control. The head arms attached to the carriage ride down and off the loading cams as the heads move out over the disc surface. The tachometer senses positioner velocity and provides a servo feedback signal to control large positioner movements. The position sensing transducer provides a servo feedback signal to hold the positioner in selected cylinders (detent). It also provides track pulses for the track counter, and indicates when the heads are in the data track zone. The retract microswitch senses that the heads are fully retracted, and combines with other signals to allow load or run operations.



Linear Motor

The linear motor contains a moving cylindrical voice coil enclosed by two concentric fixed magnet poles. The rear plate connects the poles and links flux from the outer ceramic magnet to the inner steel cylinder. The voice coil provides a motive force to the carriage as a function of the direction and magnitude of the coil current.

Carriage

The carriage is integral with the voice coil. Upper and lower support beams ride in precision ways and connect the coil to the head mounting block. The ways are aligned to prevent contact between the coil and the magnet poles, and the bearings are spring loaded to prevent lateral head movements. A notch in the upper beam aligns with one of the bearings in the retract position to provide a retract detent. A spring limits uncontrolled forward carriage travel, and a soft stop limits reverse travel.

Heads and Cams

The four head arms attach to the carriage with mounting clamps and are individually adjustable in the disc-radial direction to provide initial head alignment. Machined slots in the carriage permanently locate the heads in the vertical and circumferential directions. The loading cams hold the heads away from the disc surfaces during load and unload operations. As the heads move out over the surfaces, ramps allow the head arms to ride off the cams, and the heads float freely.

Tachometer

A magnetic rod attached to the carriage moves in and out of the tachometer pickup coil mounted within the linear motor. The changing flux linkage induces a current in the coil with a magnitude and polarity determined by the velocity and direction of movement. The servo uses the resulting signal to control positioner velocity as it moves the heads to selected tracks.

Position Transducer

The optical position transducer assembly includes a lamp, a photoelectric pickup, and a glass reticule (mounted on the carriage) that moves between them. Lines ruled on the reticule and on the photoelectric pickup form a diffraction grating which varies the light intensity on the photocells as the reticule moves. (Diffraction gratings form wave-like patterns of light with alternating bright and dark areas. As the grating moves, the bright and dark areas move also. Appendix G contains a detailed discussion of one and two dimensional diffraction gratings.)

The transducer produces two signals which locate the data track zone and two more that define the data track centerlines. The positioner servo uses these signals to determine head position during load, unload, seek, and recalibrate operations. It is important to note that the position transducer is mechanically separate from the disc surfaces. It cannot actually look at the surfaces and find the tracks, it can only indicate where they should be. If the transducer assembly moves relative to the surfaces, it will give incorrect position information. This actually happens when thermal expansion and contraction occur, and a special temperature compensation circuit adjusts the position signal to counteract the deviation.

Position Transducer - some details

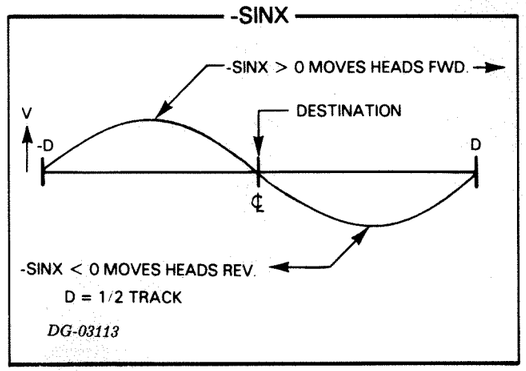
The following diagrams show the transducer, amplifiers, and resulting waveforms. There are six signals; **Sinx**, **Cosx**, (which are analog signals) **Dsinx**, **Dcosx** (which are digital versions of **Sinx** and **Cosx**), **Dindex** and **Dhu**.

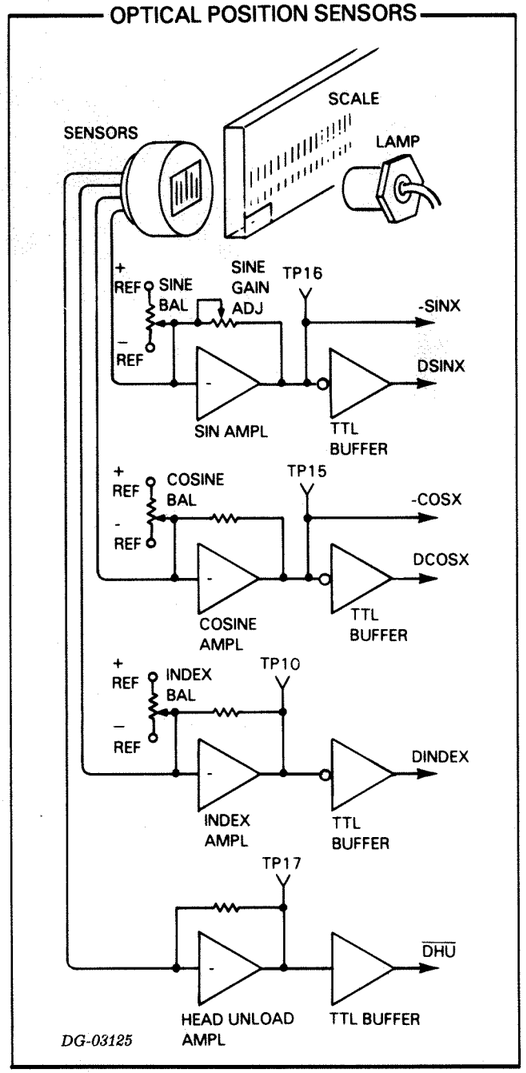
Sinx is the actual position signal. It has one full cycle per track and has zero crossings at the track centerlines and at the track boundaries. The current track address register counts boundary crossings during seek operations. When the heads move to within a half track of the destination, the servo switches to detent mode and feeds **Sinx** directly to the positioner. If the heads are reverse of the centerline, **Sinx** is positive and drives the motor forward. Conversely, if the heads are forward of the centerline, **Sinx** is negative and drives the positioner backward. The positioner therefore reaches equilibrium at the zero crossing. The detent servo loop gain is a function of the amplitude of **Sinx**, and is adjusted with a potentiometer. Another potentiometer biases the signal to adjust the locations of the zero crossings.

Cosx locates the zero crossings of **Sinx** and allows the drive to determine which zero crossings correspond to track centerlines (**Cosx** is positive) and which correspond to track boundaries (**Cosx** is negative). The drive cannot determine this simply by examining the slope of **Sinx**, because **Sinx** is negative going as the positioner moves forward through a centerline, but positive going as it moves backwards.

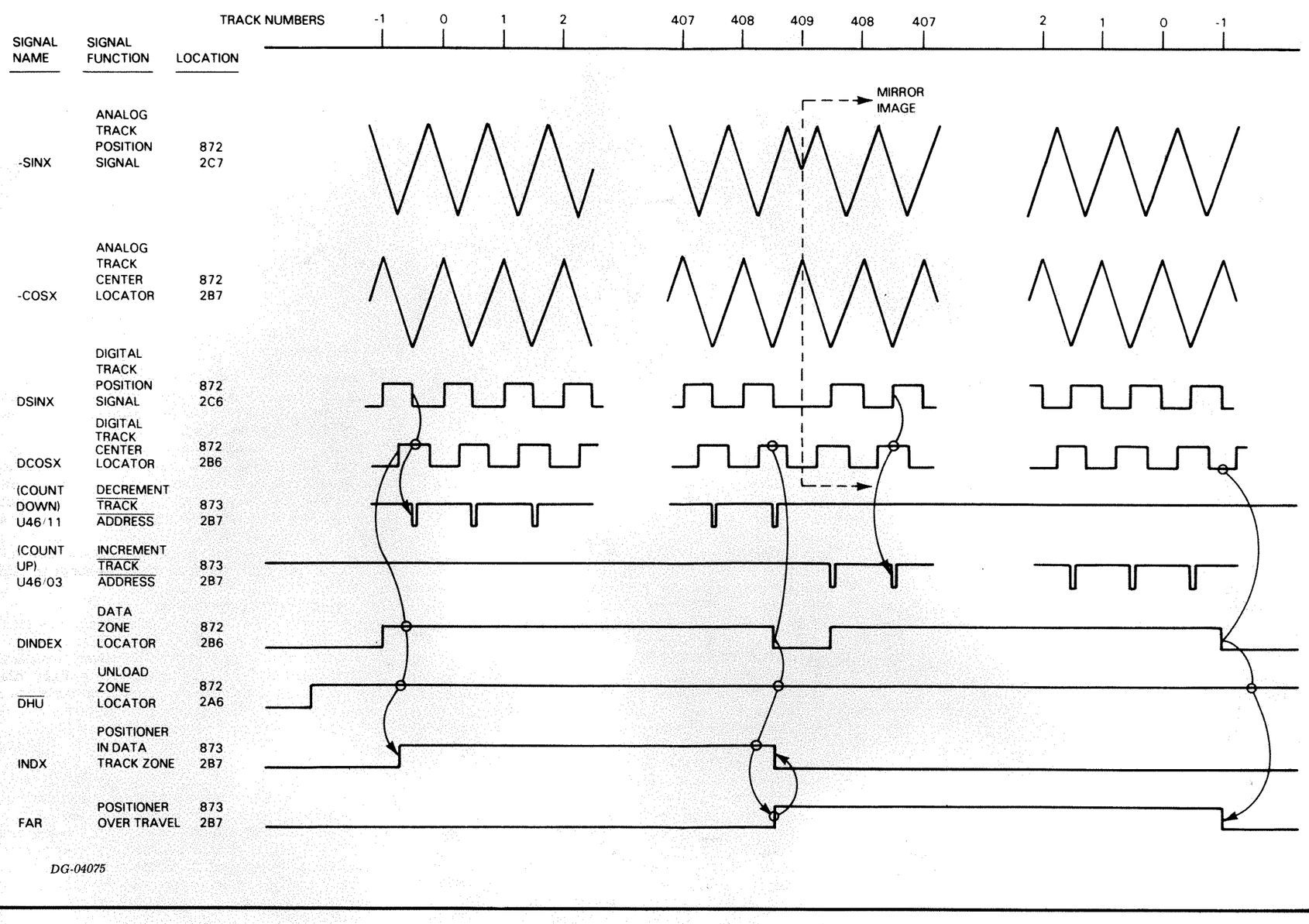
Dsinx and **Dcosx** combine to decrement the track address register (which holds the one's complement of the present track address) as the positioner moves forward, and increment the address as the positioner moves backward.

Dindex is high when the heads are between tracks -1 and 409, and **Dhu** is high when the heads are outside the retract zone. They combine to form a signal called **Indx** that goes high when the heads move into a data track zone, and low when they move out. Another signal called **Far** indicates that the heads have moved too far forward, and automatically initiates a recalibrate operation.





POSITION WAVEFORMS



DG-04075

VIII

SERVO OPERATION

The servo circuits support four basic operations: load, unload, seek, and recalibrate. An auxiliary emergency retract system overrides the servo and unloads the heads if a fault occurs which could endanger the heads and discs (such as a power failure). The following diagram shows the the three main circuits that drive the positioner:

- *the velocity servo controls large positioner movements*
- *the detent servo controls movements within the boundaries of destination tracks*
- *the servo drive circuits select either the velocity servo or the detent servo and power the linear motor*

Velocity Servo

The velocity servo moves the heads at constant velocity during load, unload and recalibrate operations. During seek operations, however, the heads move with a decreasing velocity as they approach the destination track. This method minimizes seek times and prevents overshoot that could occur, if the heads approached the destination too quickly.

The drive contains two track address registers. The present track address register indicates the current position of the heads, and the new track address register indicates the destination track for a seek operation. The present track address is subtracted from the new address to derive a difference count.

Read only memories (ROM) store a specific velocity for each difference. The greater the difference, the greater the velocity. The ROM output drives a digital to analog converter (DAC) that provides a voltage proportional to the required velocity. An atenuator divides the voltage when the heads move within two tracks of the destination to provide a more accurate velocity reference at this critical point.

A summing node subtracts the actual positioner velocity (measured by the tachometer) from the required velocity (computed by the DAC) and produces an error signal to accelerate or decelerate the motor. As the positioner moves, feedback from the position transducer updates the current track address register. The servo switches to detent mode when the heads reach the track address.

Detent Servo

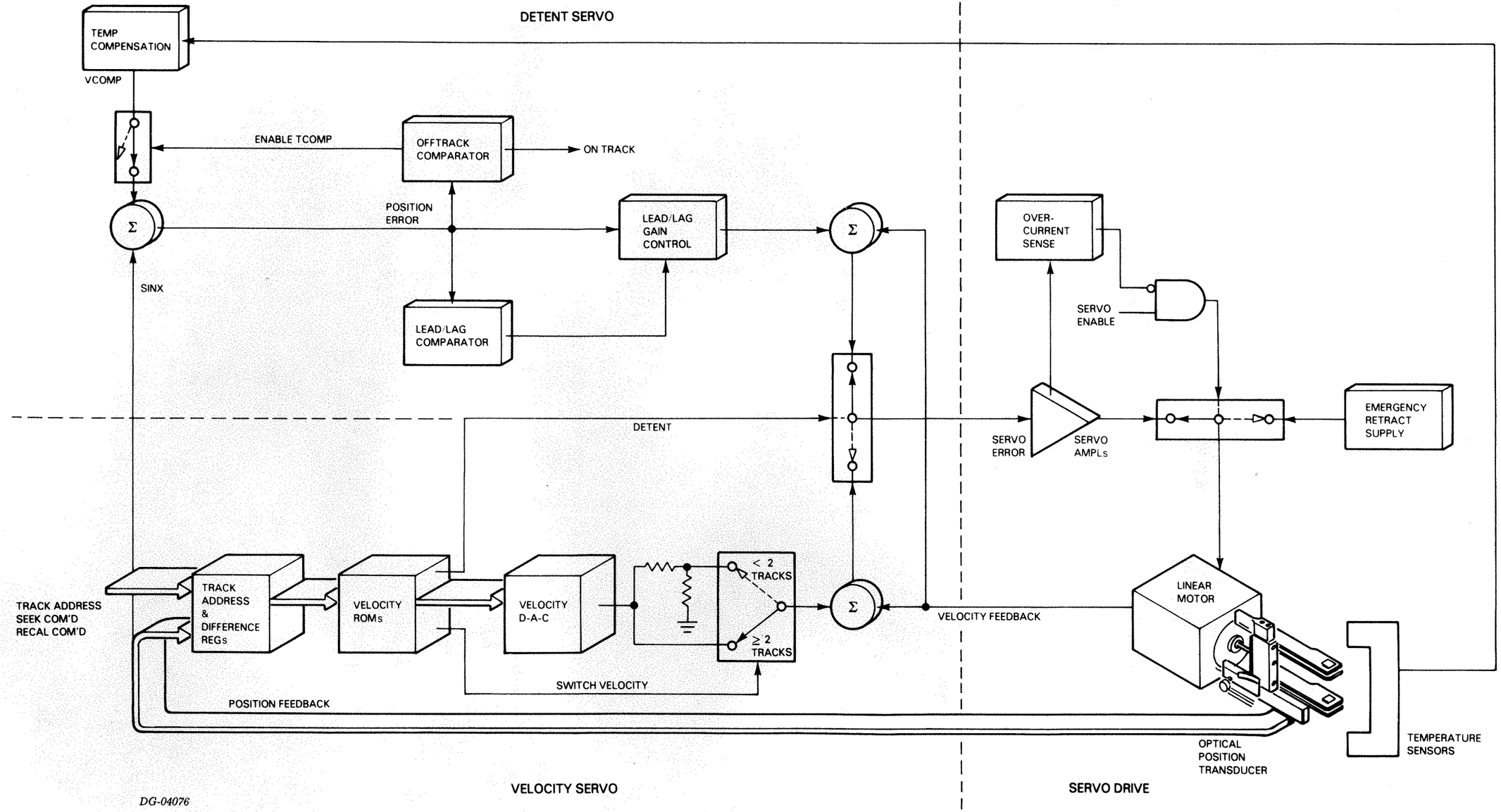
The detent servo feeds the analog position signal (**Sinx**) directly back to the positioner, which moves to null the signal and detent on the destination track. As the positioner approaches track center, a lead/lag comparator enables additional amplification to improve the accuracy of the detent operation. As the positioner moves even closer, the off track comparator enables the temperature compensation circuit to counteract errors in the position signal that may arise due to thermal differences. The position signal combines with velocity signal to increase loop gain as a function of the error, and drives the servo amplifier.

Temperature compensation applies only to the cartridge disc; the thermistor does not measure the temperature of the fixed disc, which always remains near the drive temperature. However, temperature compensation is not shut off if the fixed disc is supporting a data transfer. So a cold cartridge may cause a true offset on the fixed disc. The drive tolerances are designed to allow for this.

Servo Drive

The servo converts the drive signal to a current which powers the linear motor. Current sensors monitor the current level. If the motor heats up and starts to saturate, the drive delays subsequent seek operations to reduce the duty cycle. If the current continues to climb, or **Servo Enable** is lost, the emergency retract circuits take over and unload the heads.

HEAD POSITIONER BLOCK DIAGRAM



VIII

Velocity Servo - some details

The block diagram below details the velocity servo. We will concentrate on three major parts; the track difference computation, the velocity ROMs, and the DAC.

The logic subtracts the present track address from the new address to determine the track difference. It does this using two's compliment arithmetic.

DIFFERENCE = NEW ADDRESS + PRESENT ADDRESS + 1

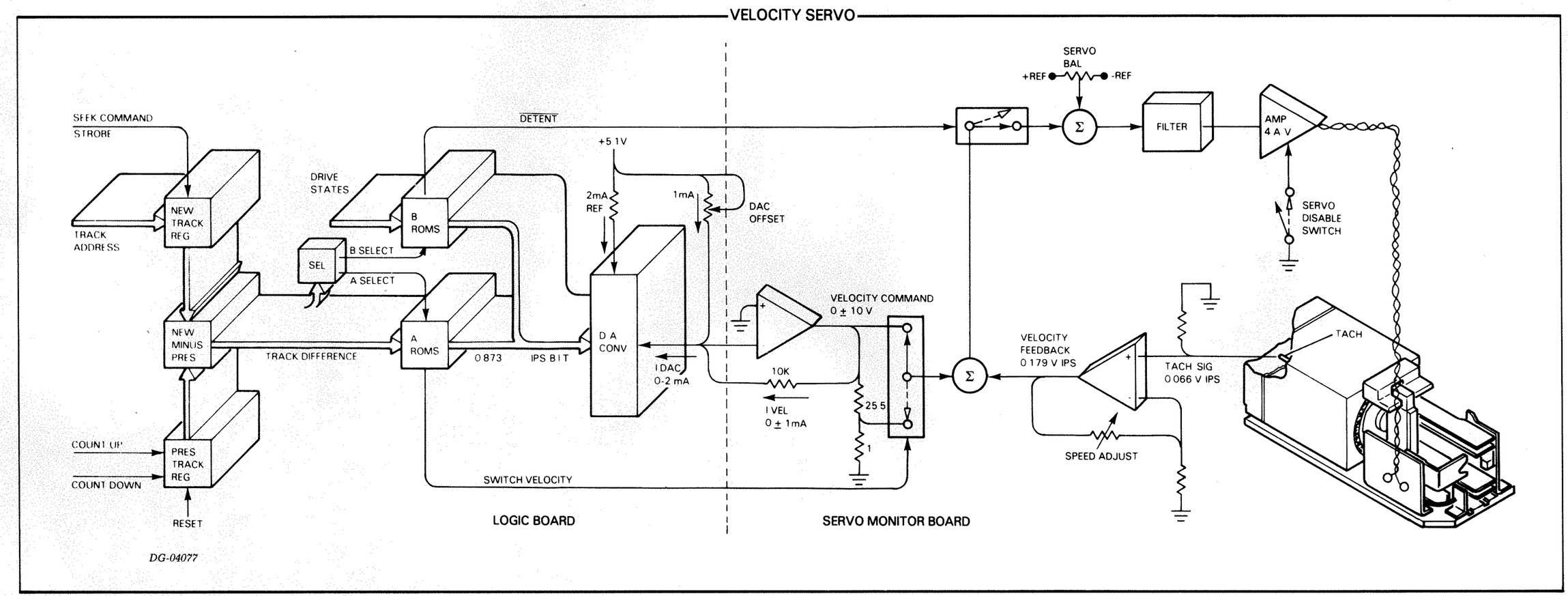
A selector examines the carry bit and most significant bits of the difference, and enables the A ROMs if the absolute value of the difference is less than 128 tracks. The selector enables the B ROMs, if the absolute value of the difference is greater than or equal to 128 tracks, or if the difference is zero. The A ROM and B ROM outputs are connected together (they have open collector outputs) and drive the DAC.

The B ROMs control positioner movements during load, unload, and recalibrate operations. They also control movement during the initial phase of a long seek. The B ROMs decode drive states that indicate the operation to be performed. They program positioner velocity; 1.7ips to load, 7ips to unload the heads or to return the heads to track zero, and 55ips to move the heads to within 128 tracks of the seek destination.

The A ROMs control short seeks of less than 128 tracks and dictate a velocity profile that decreases positioner velocity as the heads approach the destination track. They also provide a signal (switch velocity) that attenuates the velocity reference when the heads are one track away. This more accurately controls the velocity.

When the difference reaches zero, the B ROMs are re-enabled program a velocity of 0 ips, and switch the servo to detent mode. (Note that the A ROMs remain enabled, but are programmed to float their outputs when the difference equals zero.)

The DAC converts the ROM outputs to a current which the velocity command amplifer converts to a voltage. The resulting signal provides the analog reference for the velocity servo.



Differencer

The diagram to the right shows the address difference computation circuit. It uses an integrated eight bit full adder plus a discrete one bit full adder to subtract the nine bit present address from the nine bit new address. The present track address register sources the nes complement of the current address. For example, if the address is 3, the output is 111111100_2. The one bit full adder is internally wired to add one to the sum, so the result is a two's complement add.

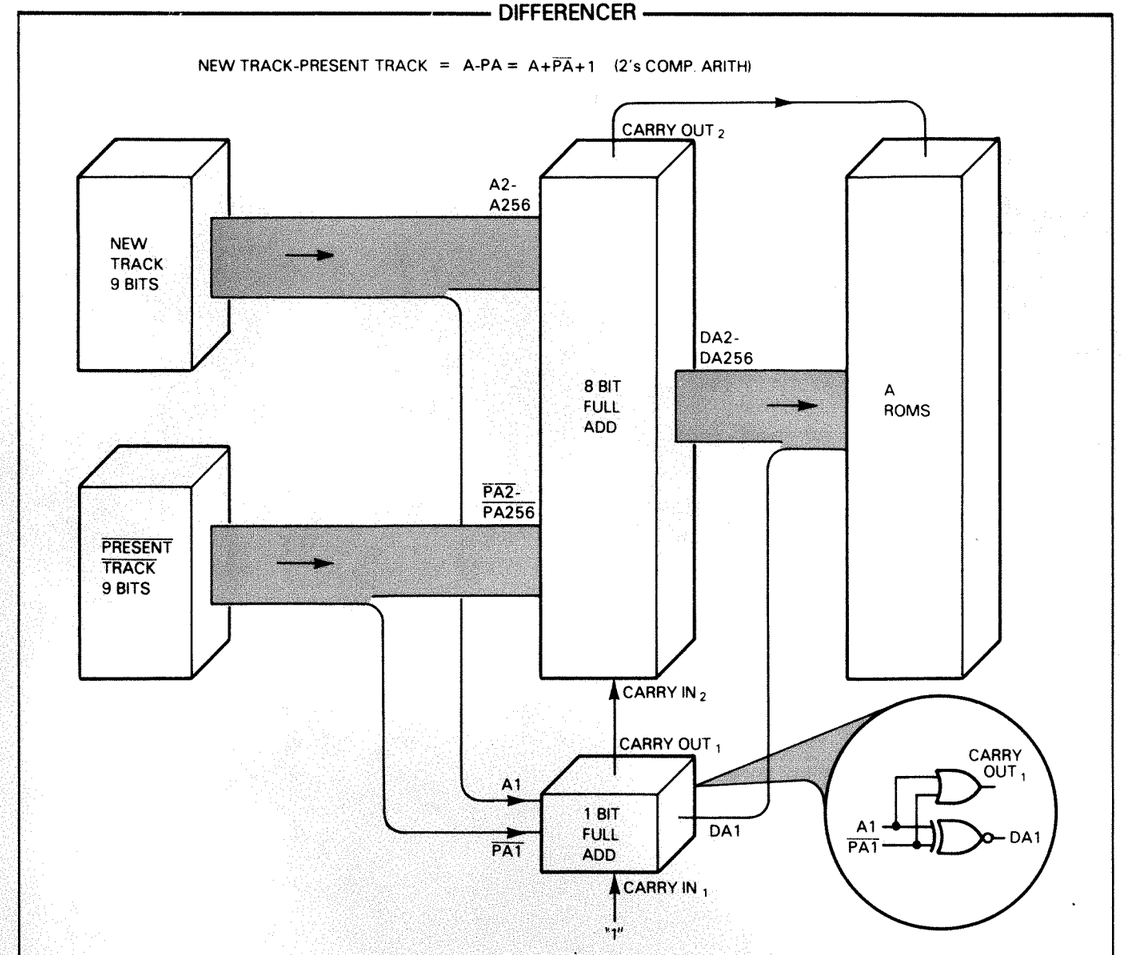
If the present address is 3 and the new address is 4, the result is:

```
0000000100  NEW ADDRESS
0111111100  ADD PRESENT ADDRESS
0000000001  ADD 1
----------
1000000001  RESULT
```

The difference is one and carry out is one to indicate forward displacement. Conversely, if the present address is 4 and the new address is 3, the result is:

```
0000000011  NEW ADDRESS
0111111011  ADD PRESENT ADDRESS
0000000001  ADD 1
----------
0111111111  RESULT
```

The difference is -1 (two's complement notation) and carry out is zero to indicate reverse displacement.

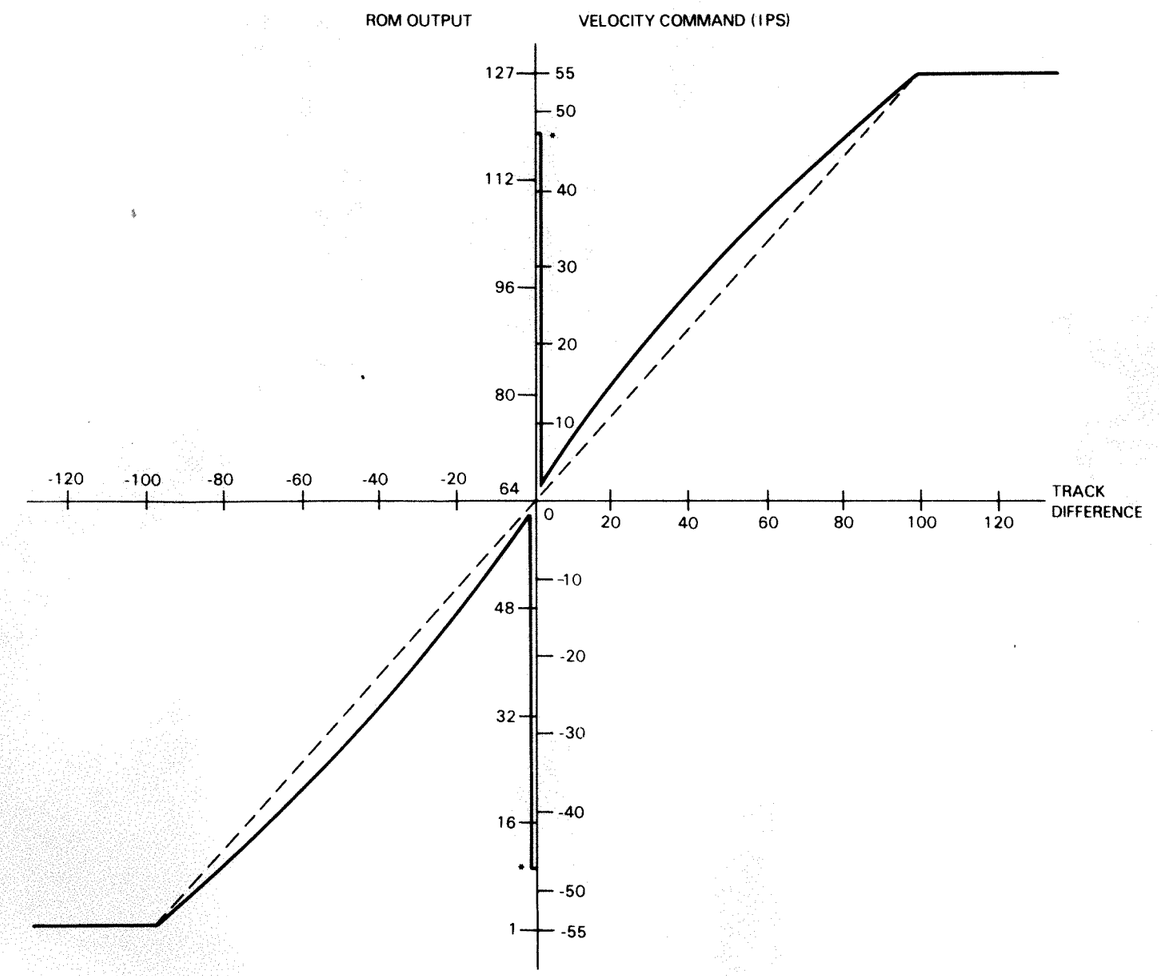


VELOCITY PROFILE

A ROM MAP (PARTIAL)

TRACK DIFFERENCE (NEW ADDRS MINUS PRES ADDRS)	DIFFERENCE (ROM ADDRESS) C9	DA 64	DA 32	DA 16	DA 8	DA 4	DA 2	$\overline{DA\ 1}$	ROM OUTPUT DACSGN	DAC 64	DAC 32	DAC 16	DAC 8	DAC 4	DAC 2	SW VEL	DAC OUTPUT MA	VOLTS = (MA-1) X 10K	EQUIVALENT VELOCITY VOLTS TIMES 5.587 IPS/V
127	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1.984	9.84	55.00
126	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.984	9.84	55.00
99	1	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1.984	9.84	55.00
98	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1.969	9.69	54.12
80	1	1	0	1	0	0	0	1	1	1	1	0	1	0	1	1	1.828	8.28	46.26
60	1	0	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1.656	6.56	36.66
40	1	0	1	0	1	0	0	1	1	0	1	1	1	1	1	1	1.484	4.84	27.06
20	1	0	0	1	0	1	0	1	1	0	1	0	0	1	0	1	1.281	2.81	15.71
3	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1.078	0.78	4.36
2	1	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1.047	0.47	2.62
1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	1.859	8.59	1.81 *
0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	•	•	•
-1	0	1	1	1	1	1	1	0	0	0	0	1	0	0	1	0	0.141	-8.59	-1.81 *
-2	0	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	0.953	-0.47	-2.62
-3	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	0.922	-0.78	-4.36
-20	0	1	1	0	1	1	0	1	0	1	0	1	1	1	0	1	0.719	-2.81	-15.71
-40	0	1	0	1	1	0	0	1	0	1	0	0	0	0	1	1	0.516	-4.84	-27.06
-60	0	1	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0.344	-6.56	-36.66
-80	0	0	1	1	0	0	0	1	0	0	0	1	0	1	1	1	0.172	-8.28	-46.26
-98	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1	0.031	-9.69	-54.12
-99	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0.016	-9.84	-55.00
-127	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0.016	-9.84	-55.00
-128	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0.016	-9.84	-55.00

• A ROM FLOATS, B ROM OVERLAYS



* VELOCITY SWITCH ATTENUATES DAC OUTPUT BY 1/26.5

DG-04079

A ROMs

The A ROMs convert the carry and the seven least significant bits of the difference (which represent a number between 128 and -128) to a seven bit digital velocity reference for the DAC. They dictate an optimum velocity profile that matches positioner response to minimize seek times. The maximum ROM output (1111111_2) corresponds to full forward velocity (55ips), and the minimum output (0000001_2) corresponds to full reverse velocity. The number half way in between (1000000_2), therefore corresponds to zero velocity.

The ROM map shows velocities for selected difference counts. Note that the least significant bit of the difference count (DA 1) is inverted. The ROM takes that into account. The ROM dictates maximum velocity until the difference falls below 99, and programs decreasing velocity from there.

When the difference between the current track and new track address becomes one, additional measures must be taken to provide an optimum velocity reference. Velocity must be precisely controlled as the positioner enters detent phase, to prevent overshoot. The DAC does not have enough resolution to provide the required velocity at this critical point. To overcome this the ROM prescribes a very large velocity while activating an attenuator that reduces the DAC output to the appropriate level.

As mentioned previously, a zero difference floats the ROM outputs (with the exception of the velocity switch) to allow the B ROM overlay.

B ROMs

The following input signals control the B ROM:

FAR Far limit sets when the heads move beyond track 407 and clears when they move back behind track zero. It initiates a recalibrate operation following a seek overtravel.

RNENAB Run enable Sets after the spindle has come up to speed and the brushes have completed a sweep (load). It clears when the spindle shuts off (unload).

PA512 Present address bit 512 is the most significant bit of the present track address. It sets if the heads are in the data track zone. (Recall that the address register holds the one's complement of the present track address, so an address between 0 and 511 corresponds to a binary number between 1111111111_2 and 1000000000_2.)

HSWB Home switch sets if the carriage is home.

C9 The carry bit sets for forward motion.

DA=0 DAC input equals zero when the difference is zero (detent mode).

DCOSX, DSINX Not used.

The ROM map shows ten states. The first nine specify specific drive operations which the ROMS initiate by releasing **Detent** and specifying a velocity. The tenth state is illegal and will never occur when the drive is functioning properly.

The mapping function becomes clear when the input control signals are examined. For example, consider the first entry in the map table. In this case the spindle is stopped, but the carriage is not home. This state might occur if vibration causes the carriage to roll forward while the drive is powered down. The B ROMs prescribe a velocity of -7ips to retract the heads. Note that the remaining control signals are insignificant; however, the drive will initialize them to the states shown if it is functioning properly.

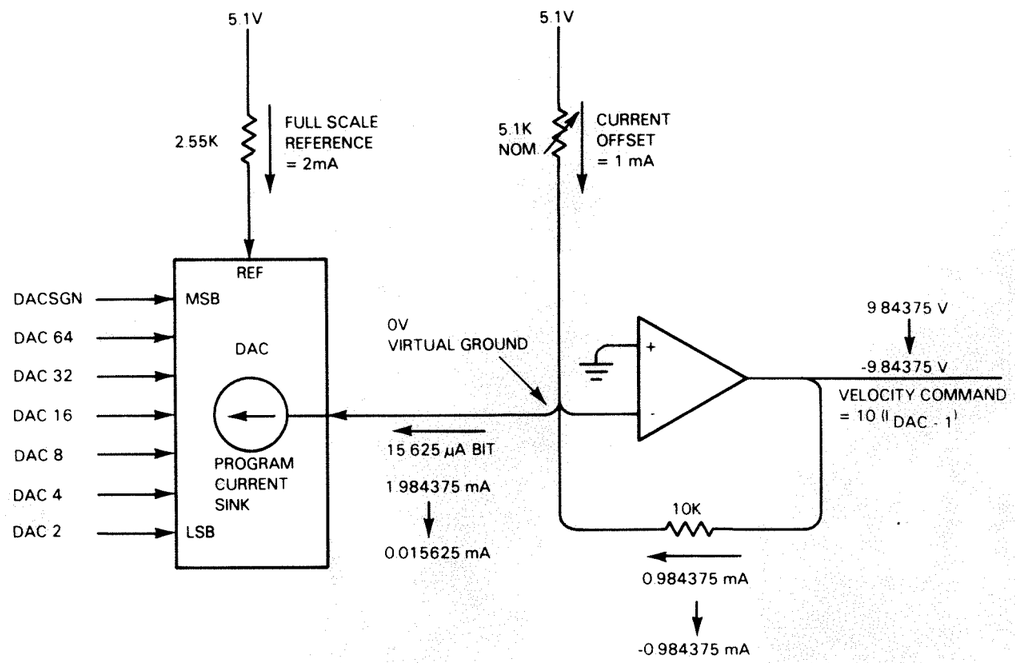
B ROM MAP

CURRENT STATE	ROM INPUT								ROM OUTPUT								NEXT STATE	EQUIV. VELOCITY (IPS)
	FAR	RNENAB	$\overline{P4512}$	HSWB	C9	DA = 0	$\overline{DCOSX}$	$\overline{DSINX}$	DACSGN	DAC64	DAC32	DAC16	DAC 8	DAC 4	DAC 2	$\overline{DETENT}$		
DRIVE INACTIVE IN UNLOAD ZONE BUT NOT HOME	0	0	0	0	0	1	X	X	0	1	1	1	0	0	0	1	DRIVE POSITIONER HOME AFTER POWER UP	-7
POSITIONER HOME AND DRIVE INACTIVE	0	0	0	1	0	1	X	X	1	0	0	0	0	0	0	1	POSITIONER HOME	0
POSITIONER HOME AND DRIVE ACTIVE	0	1	0	X	0	1	X	X	1	0	0	0	0	1	0	1	LOAD HEADS (FORWARD RECAL)	+1.7
INNER LIMIT HIT	1	1	0	0	0	1	X	X	0	1	1	1	0	0	0	1	REVERSE RECAL	-7
DIFFERENCE = 0	0	1	1	0	1	0	X	X	1	0	0	0	0	0	0	0	DETENT	0
FORWARD	0	1	1	0	1	1	X	X	1	1	1	1	1	1	1	1	FULL FORWARD SPEED	55
REVERSE	0	1	1	0	0	1	X	X	0	0	0	0	0	0	1	1	FULL REVERSE SPEED	-55
HEADS LOADED AND DRIVE INACTIVE	0	0	1	0	0	1	X	X	0	1	1	1	0	0	0	1	UNLOAD	-7
POSITIONER MOVING FORWARD AND DRIVE INACTIVE	0	0	1	0	1	1	X	X	0	1	1	1	0	0	0	1	UNLOAD	-7
ILLEGAL CONDITION	ALL OTHER ADDRESSES								0	1	1	1	0	0	0	1	UNLOAD	-7

DG-04080

X = "DON'T CARE"

DAC OPERATION



DAC INPUT	CURRENT WEIGHT (mA)	VELOCITY WEIGHT (IPS*)
DACSGN	1	55.872
DAC 64	0.5	27.936
DAC 32	0.25	13.698
DAC 16	0.125	6.984
DAC 8	0.0625	3.492
DAC 4	0.03125	1.746
DAC 2	0.015625	0.873

* TO COMPUTE VELOCITY
IF DACSGN = 1 SUM THE WEIGHTS OF DAC 64 THROUGH DAC 2
IF DACSGN = 0 SUM THE WEIGHTS OF DAC 64 THROUGH DAC 2 AND SUBTRACT 55.872

DG-04081

DAC

The DAC is a programmable current source. The seven bit input from the ROMs determines the current level. An external resistor sets the maximum current to 2ma. This current corresponds to a DAC input of 10000000_2. However, the maximum number the DAC can accept is 1111111_2 so the peak current output falls one bit short of 2ma. The current weight per bit is 15.625ua. To provide a symmetric output, the ROMs specify a minimum DAC input of 0000001_2.

The DAC output is unipolar (it can only sink current). But the velocity servo requires a bipolar voltage to produce forward and reverse velocities. An external resistor provides an exact 1mA offset current, and exactly cancels the DAC current at the midpoint (1000000_2 = zero track difference). This causes a net current flow *into* the DAC if the track difference is greater than zero (forward), and an apparent net current flow *out of* the DAC, if the difference is less than zero (reverse). An operational amplifier converts the net current to a voltage and provides the analog velocity reference. The resulting velocity weight is 0.873 ips per bit (55 ips divided by 63).

For example: Assume the current track address is 32 and the new address is 34, so the difference is 2 (forward). The difference is:

```
0000100010
0111011111 +
0000000001 +
----------
1000000010 RESULT
```

The differencer inverts the the least significant bit, so the input to the A ROM is 10000011_2, and the output is 1000011_2. The DAC current is then

```
1.000000
0.031250 +
0.015625 +
---------
1.046875mA RESULT
```

Subtract 1ma and multiply by 10 (the current-to-voltage conversion ratio) to get 0.46875 volts as the velocity reference. The resulting velocity is:

0.873/0.15625 x 0.46875 = 2.62 ips.

Detent Servo - some details

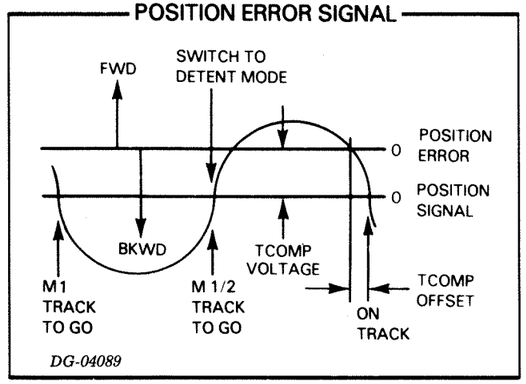
The diagram on the opposite page shows the detent servo in detail. The servo signal flows from left to right across the top of the picture. The position signal **(Sinx)** is amplified and balanced to form the position error signal. The position error is further amplified and combined with the tachometer signal to improve settling time. The result is balanced again and amplified to drive the positioner.

Two window detectors monitor the absolute value of the position error voltage as the heads move on track. When the position error is reduced to 0.5 volts the lead/lag amplifier gain increases by four to improve the error sensitivity (and therefore the detenting accuracy). When the error is further reduced to 0.37 volts, the temperature compensation circuit is activated, and offsets errors in the position signal that arise due to thermal expansion. The **on track** signal also asserts at this point, and 3ms later the positioner control logic assumes the heads are on track.

To better understand the need for switching temperature compensation on and off, let us examine servo operations with compensation conditions continuously applied. The figure below shows that temperature compensation alters the apparent zero crossing of the error signal, SINX. The case shown will degrade settling time because the error signal will try to reverse the positioner as it enters detent mode and drive it back to the previous track. Even though the positioner will have enough inertia to get above the zero crossing of the error signal, the reduced apparent amplitude of the signal beyond that point would further degrade settling.

Even though the compensation voltage is switched, the offset could still be enough to degrade the detent servo. Consider again the case shown and notice that the offset is so severe that the slope of the position signal in the vicinity of the zero crossing of the position signal is markedly reduced. This reduces the gain of the servo loop. A window detector monitors the compensation voltage and negates the **Temperature OK** signal, if the temperature difference is excessive. This causes the drive to inhibit **Ready** until equilibrium is achieved (which could be as much as 10min).

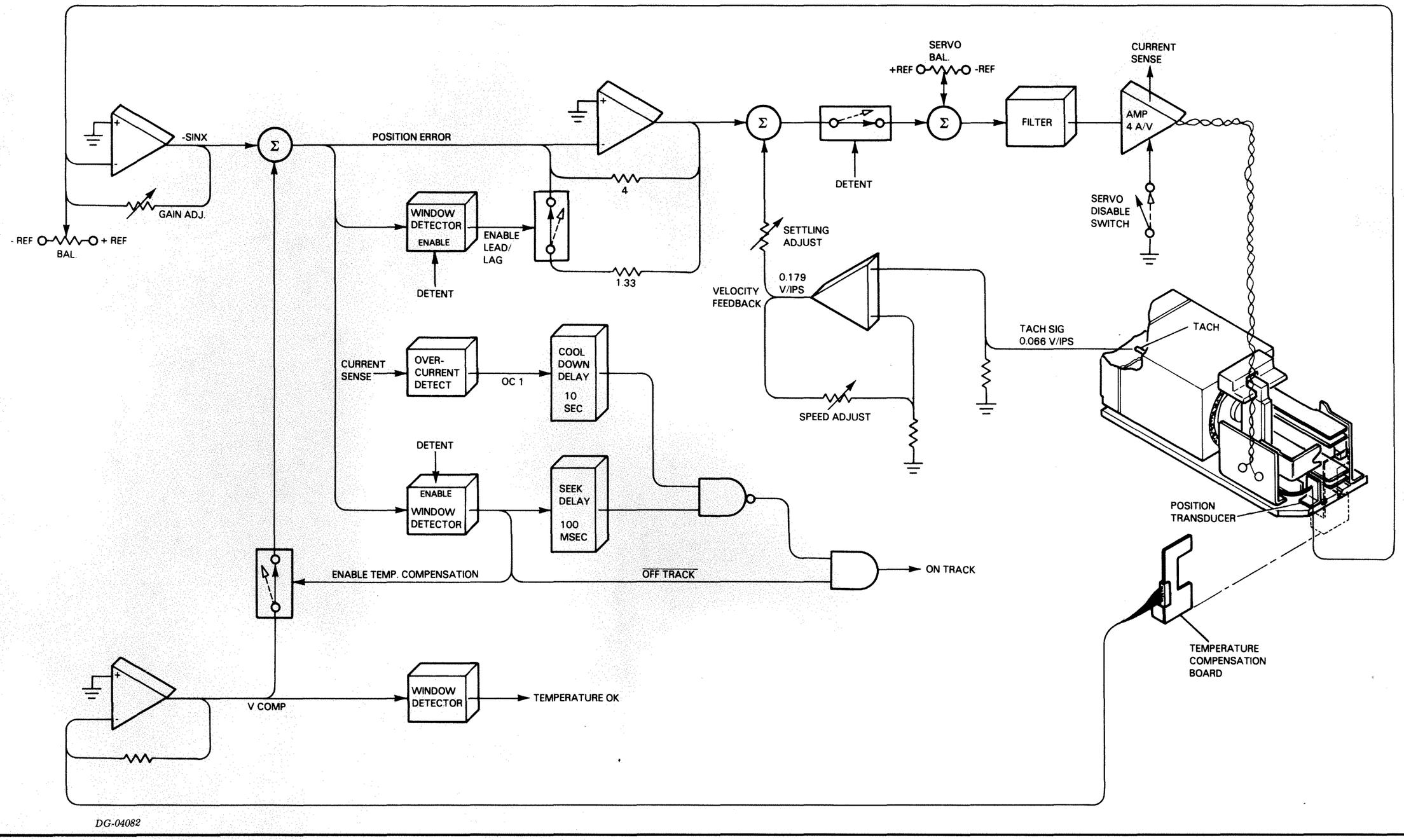
POSITION ERROR SIGNAL



DG-04089

The detent operation is delayed if the linear motor current becomes excessive. This forces a reduction in the seek duty cycle and allows the motor to cool down. If an over current occurs, a 10 second cool down delay begins. During that time, all detent operations are delayed an additional 100ms.

DETENT SERVO



DG-04082

VIII

Servo Drive--Some Details

The diagram on the opposite page shows the positioner drive amplifier and emergency retract circuits. The amplifier accepts signals from the velocity and detent servo loops, and converts them to a current to drive the linear motor. Feedback from a current sensing resistor in the return leg of the motor controls the amplifier gain. A servo disable switch can short circuit the amplifier and effectively disconnect the linear motor to allow service personnel to operate the positioner by hand.

Several fault detectors monitor the condition of the drive. If a condition which could endanger the discs or the heads occurs, they cause an emergency retract.

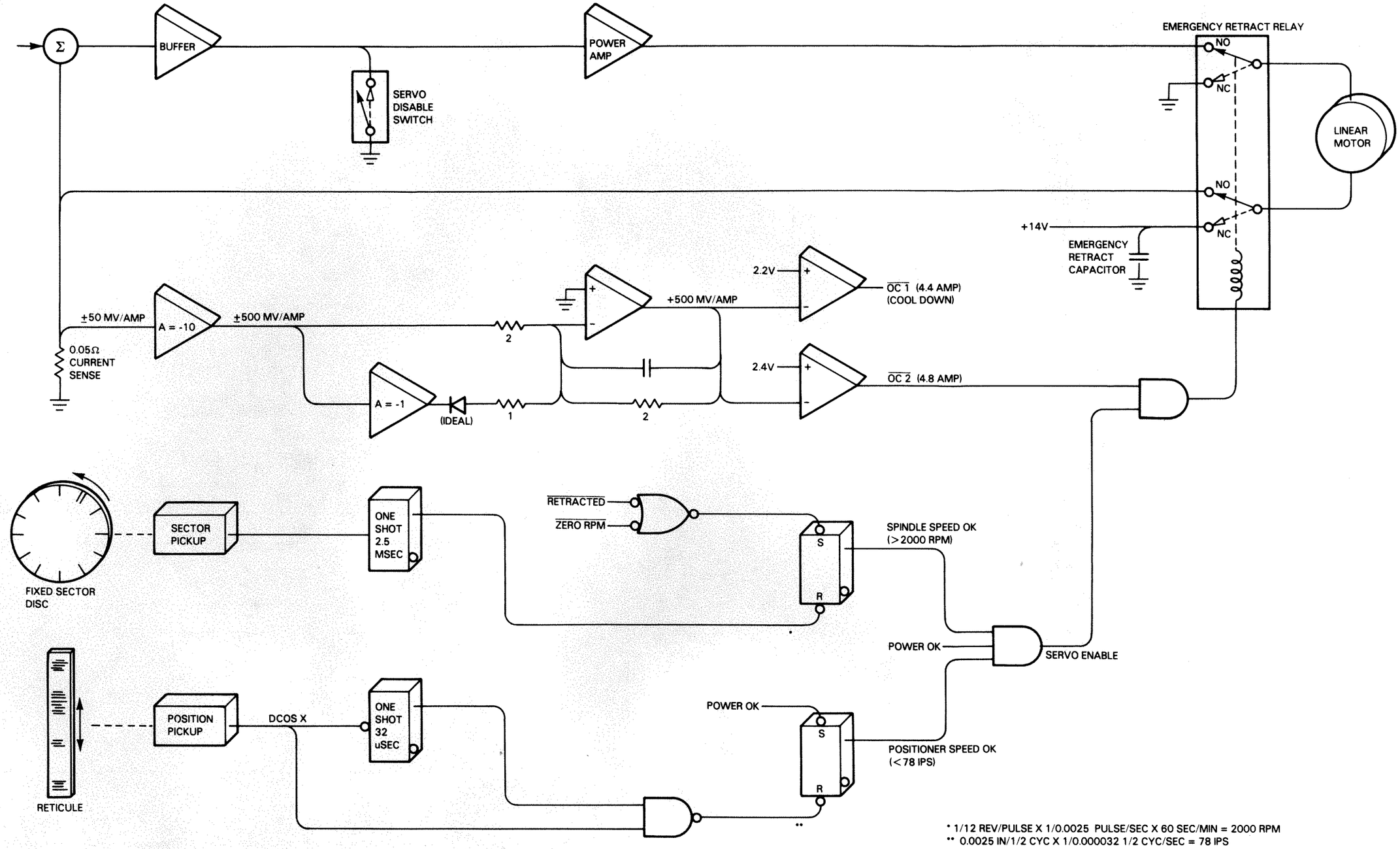
A monitor checks that the motor current does not rise to levels which might endanger the motor or drive amplifier. If the average current level exceeds 4.8amps, it requests an emergency retract.

A velocity in excess of 78ips would indicate a failure in the velocity servo, and could result in extensive damage to the positioner mechanism. A timer monitors the 1/2 cycle period of the Cosx, signal. This corresponds to the amount of time to move 1/2 track(0.0025in). It requests an emergency retract, if period of one half cycle falls below 32us.

Another timer checks that the spindle speed does not fall below 2000rpm while the heads are loaded. A lower velocity could cause a head crash. The timer monitors the period of sector pulses from the fixed disc, and requests an emergency retract if the period exceeds 2.5 msec. (Note that the timer gets an extra trigger from the index pulse, and will not accurately time the spindle speed in that sector.)

Finally, an emergency retract occurs in the event of a power failure. All four signals combine to drive the emergency retract relay. If a failure occurs, the relay de-energizes and mechanically defaults to the retract state. This reverses the polarity of the motor drive, and connects the previously charged retract capacitor, which drives the motor in reverse to the retract position. This mechanism guarantees a retract even in the presence of a total power failure. (The **power ok** monitor checks the voltage that charges the retract capacitor and prevents head load if it is below acceptable limits.)

EMERGENCY RETRACT SYSTEM



DG-04083

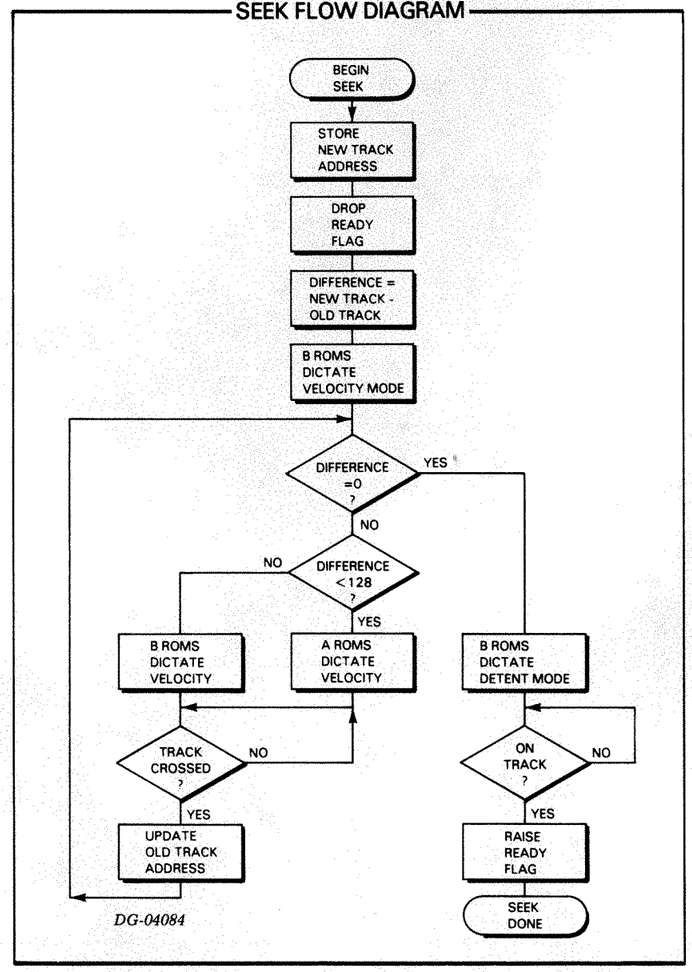
SEEK COMMMAND EXECUTION

The following flow chart and timing diagram show the sequence of a long forward seek. It starts when the controller strobes a new address to the new track register. If a non-zero difference results, the drive drops out of detent mode, releases lead/lag amplification and temperature compensation, and clears **Ready**. In the case shown, the initial difference is greater than 127 tracks so the B ROMs are activated and command maximum velocity. As the positioner moves forward, track boundary crossings detected by the **Sinx** signal decrement the present track address counter.

The A ROMs are activated when the difference falls below 128. They begin to reduce the velocity when the difference falls below 99. When the difference falls below two, the A ROMs command a large velocity, but negate the **Switch Velocity** signal to attenuate the DAC output. The heads move at low speed to the destination track where the B ROMs take over and initiate detenting. As the heads approach the track centerline, threshold detectors monitor the position signal and enable lead/lag amplification followed by temperature compensation. The **on track** signal asserts **Ready** 3ms later and the operation is complete.

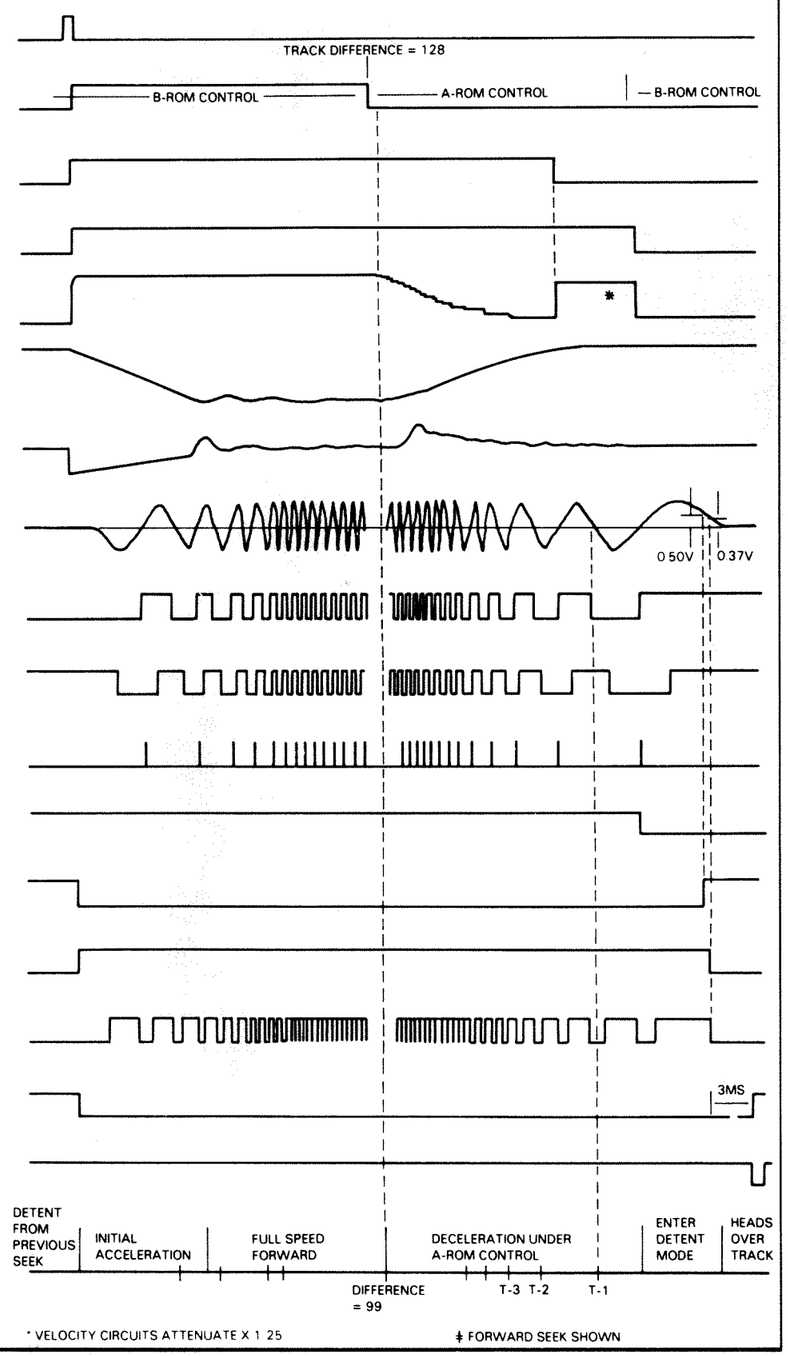
The remaining flowcharts detail load, unload and recalibrate operations and include spindle operations discussed in previous chapters. Finally, a master timing diagram shows a random sequence of drive operations.

SEEK FLOW DIAGRAM



SERVO SEEK WAVEFORMS ‡

SIGNAL NAME	SIGNAL FUNCTION	LOCATION
STROBE	SEEK COMMAND	873 2C8
$\overline{\text{TRACK}}$ $\overline{\text{ENABLE}}$	DIFFERENCE >128	873 2D5
SWITCH VELOCITY	DO NOT ATTENUATE DAC OUTPUT	873 2D4
$\overline{\text{DETENT}}$	VELOCITY MODE	873 2D3
VELOCITY COMMAND	DAC OUTPUT	872 2C2
VELOCITY FEEDBACK	TACHOMETER	872 2D6
TP 30 (SERVO ERROR)	TACH - DAC	872 1D5
-SIN X	ANALOG TRACK POSITION SIGNAL	872 2C7
$\overline{\text{D SIN X}}$	DIGITAL TRACK POSITION SIGNAL	872 2C6
$\overline{\text{D COS X}}$	DIGITAL TRACK CENTER LOCATER	872 2B6
U46 11 (COUNT DOWN)	DECREMENT $\overline{\text{TRACK}}$ $\overline{\text{ADDRESS}}$	873 2B7
$\overline{\text{DA = 0}}$	COMING ON TRACK 0	873 2D3
ENB L L	LEAD LAG LOOP GAIN BOOST	872 2B4
$\overline{\text{ENAB}}$ $\overline{\text{TCOMP}}$	THERMAL OFFSET COMPENSATION	872 2B3
$\overline{\text{ON TRACK}}$	NEAR TRACK CENTER	872 1B4
DUR	DISC UNIT READY	873 2B3
$\overline{\text{ATTEN}}$	SEEK COMPLETE	873 2A4

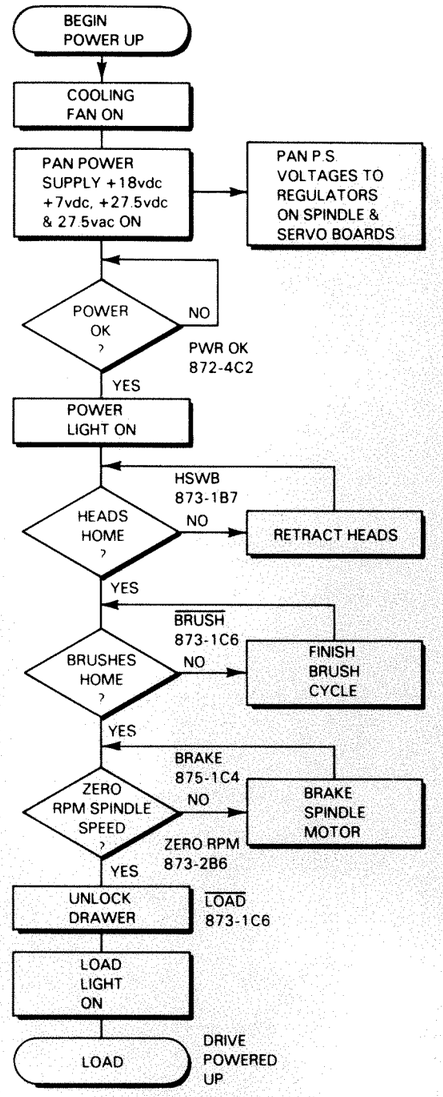


DG-04085

* VELOCITY CIRCUITS ATTENUATE X 1 25

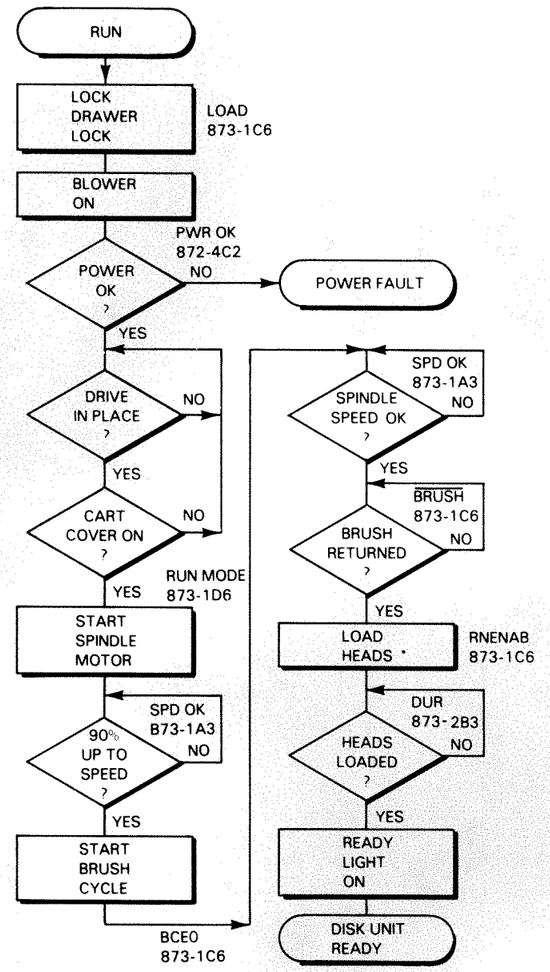
‡ FORWARD SEEK SHOWN

POWER UP FLOWCHART



DG-04087

START UP FLOWCHART

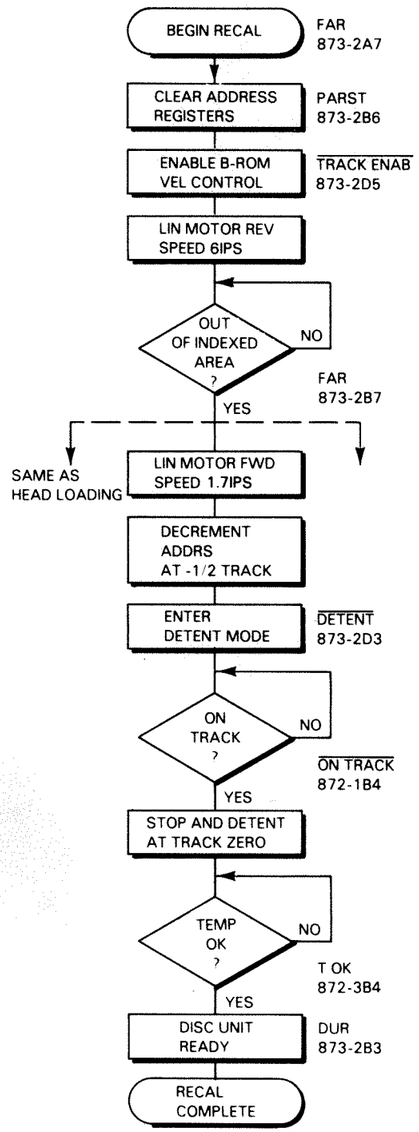


DISK DRIVE IS READY TO EXECUTE I/O COMMANDS FROM CONTROLLER

• SEE RECAL/LOAD FLOWCHART

DG-04087

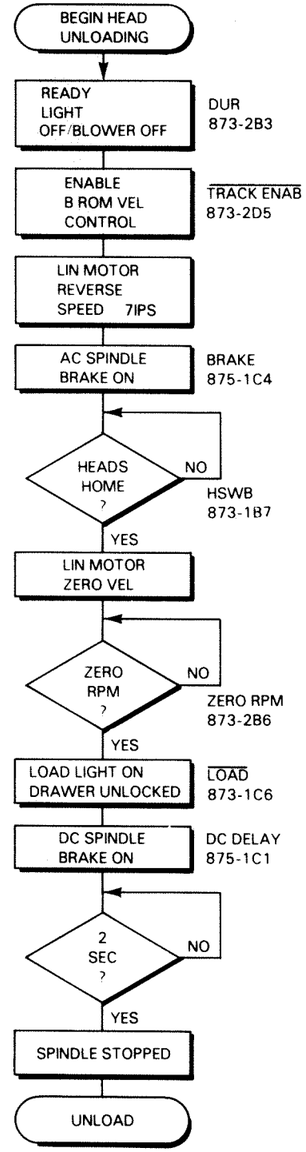
RECALIBRATE/LOAD FLOWCHART



DISC DRIVE IS READY TO EXECUTE I/O COMMANDS FROM THE CONTROLLER

DG-04087

UNLOAD FLOWCHART

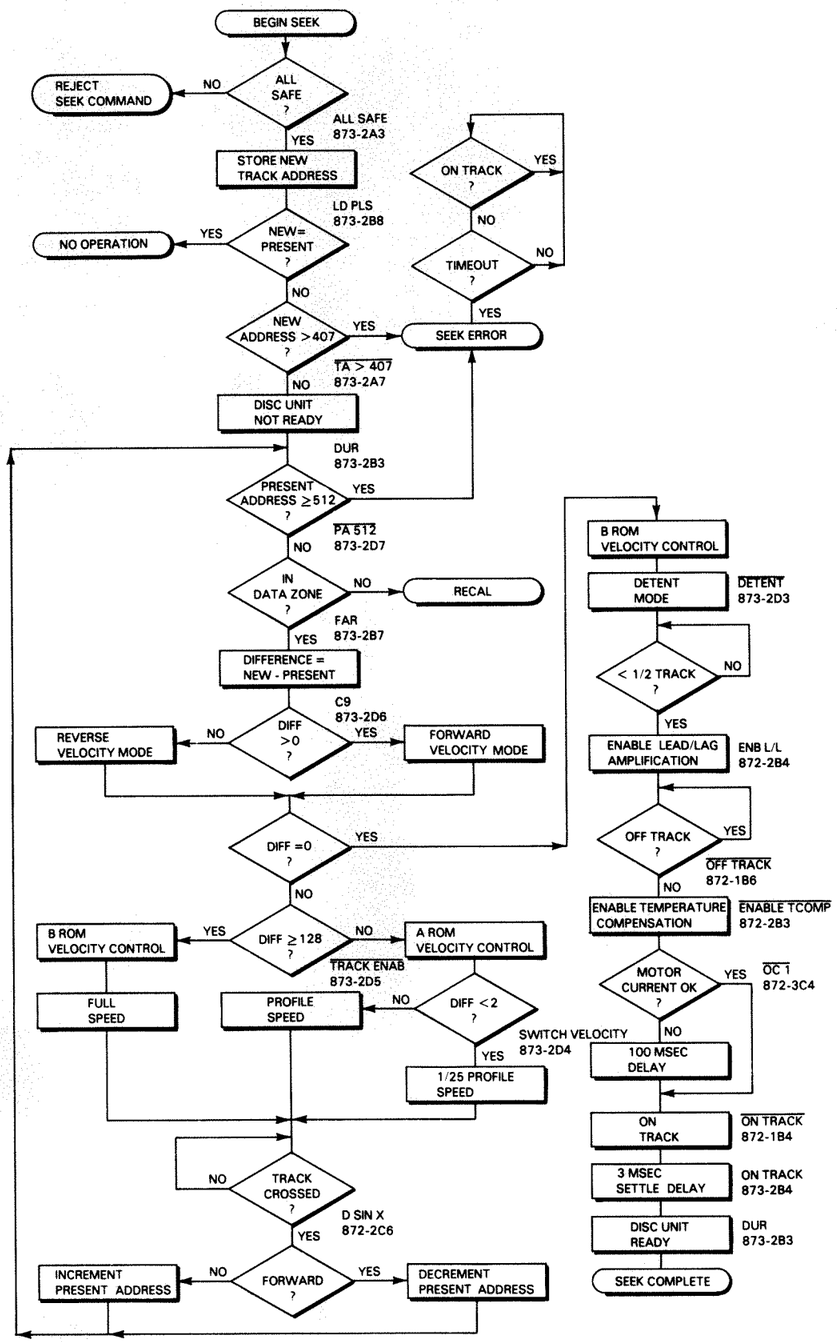


DISC DRIVE MAY BE PULLED OUT FROM CABINET FOR DISC CARTRIDGE UNLOADING

DG-04087

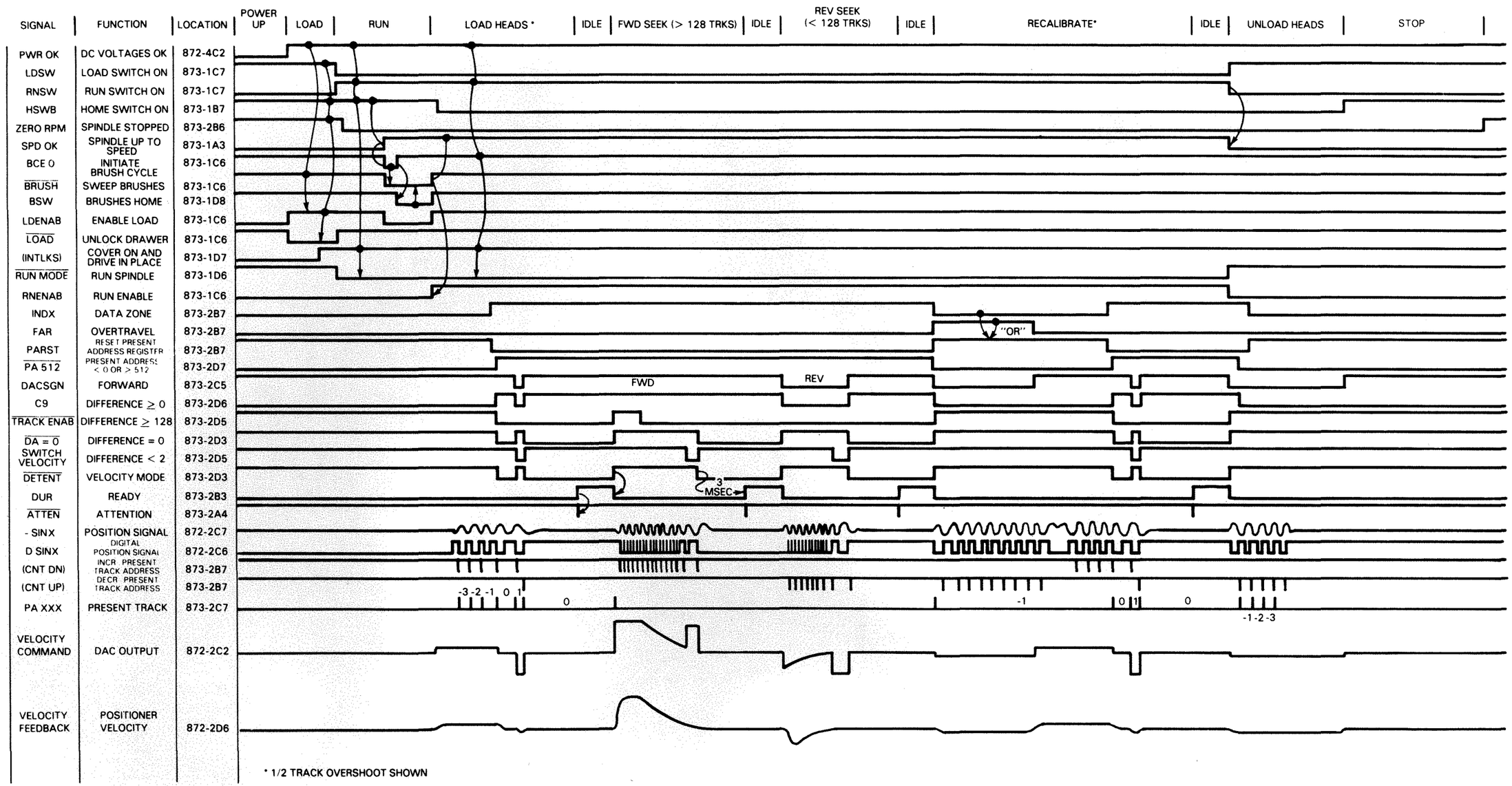
VIII

SEEK FLOWCHART



DG-04086

MASTER TIMING DIAGRAM

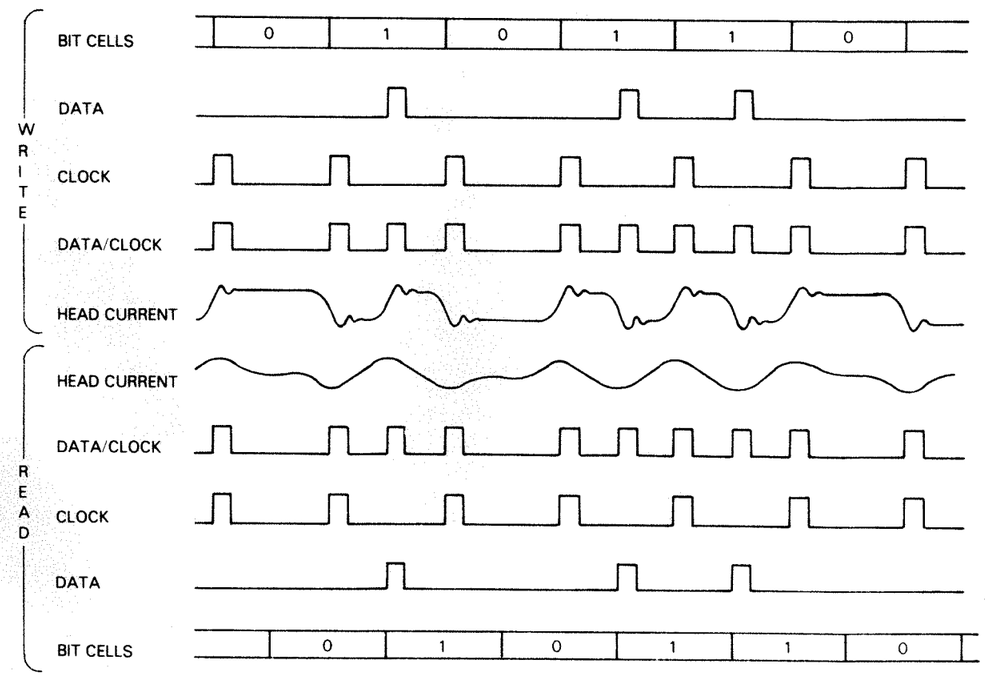


* 1/2 TRACK OVERSHOOT SHOWN

DG-04088

VIII

READ/WRITE TIMING



DG-04094

CHAPTER IX
DRIVE: DATA TRANSCRIPTION

TWO FREQUENCY RECORDING

The drive uses a data encoding scheme which records a clock along with the data. The read circuits use the recorder clock to recover the data, which allows data recovery over a range of spindle speeds. The diagram on the opposite page illustrates this encoding scheme. It is called two frequency (2F).

Consider the binary data stream as a series of evenly spaced bit cells. The 2F encoding scheme records a clock pulse at the beginning of each bit cell. The center of each cell contains the data (a pulse signifies a 1, and an empty cell represents a 0). One can clearly see the two frequencies. The fundamental frequency is the data rate (frequency of clock pulses) and for this drive is 2.5MHz. The second harmonic (5MHz) occurs when ones are recorded.

The timing diagram shows that data pulses and clock pulses combine to form a data/clock signal. Each pulse in the data/clock stream causes the drive to reverse the direction of current flow in the selected head. This "writes" a series of magnetic reversals in the ferrous oxide coating on the disc surface. The head can then read the data back by sensing the flux reversals at the magnet boundaries. (Remember that the current induced in an inductor by a magnetic field is proportional to the rate of change of flux, so each flux reversal induces a current pulse in the head.) The read circuits amplify these current pulses to recover the data/clock signal. A phase locked loop then locks onto the clock pulses, which allows the data separator to isolate the data pulses.

Note that the read data rate is a function of spindle speed. If the spindle was turning faster when data was recorded than it is when data is read, the rate is reduced. Of course, the opposite is also true. This is one reason the spindle speed is precisely regulated.

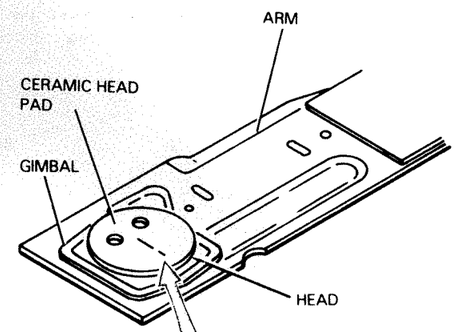
READ/WRITE MECHANISM

Heads

A head consists of a ceramic pad connected by a gimbal to a spring loaded suspension arm. The spring action of the arm pushes the pad toward the disc surface and the aerodynamic lift counters this force and causes the head to fly above the surface at a minimum height of 85 μinch.

The ceramic pad contains a coil assembly with four poles and three windings. The three windings join at a common point which the head select circuits ground to enable the head (this point otherwise floats). Two windings form a center-tapped read/write coil and the third is the erase coil. A gap between the read/write poles locates the zone where flux reversals are recorded. As the surface moves by the head, this gap defines a circular track. A gap on either side of the trailing read/write pole locates the tunnel erase zone. The erase head trims the written track down to 0.0035 inches to prevent crosstalk from adjacent tracks, during read operations.

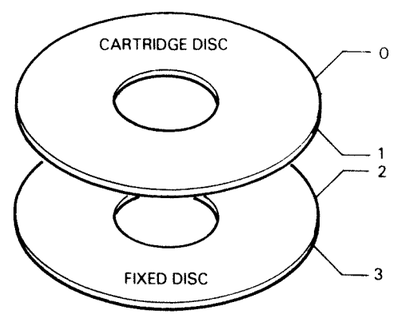
READ/WRITE HEAD



DG-04120

Each of the four heads has a unique address which selects the associated surface, as shown in the following figure. The controller specifies a surface address when it sets up a data transfer, and the head select circuits in the drive enable the head and check that no more than one head is selected.

SURFACES



DG-04095

IX

READ/WRITE CIRCUITS

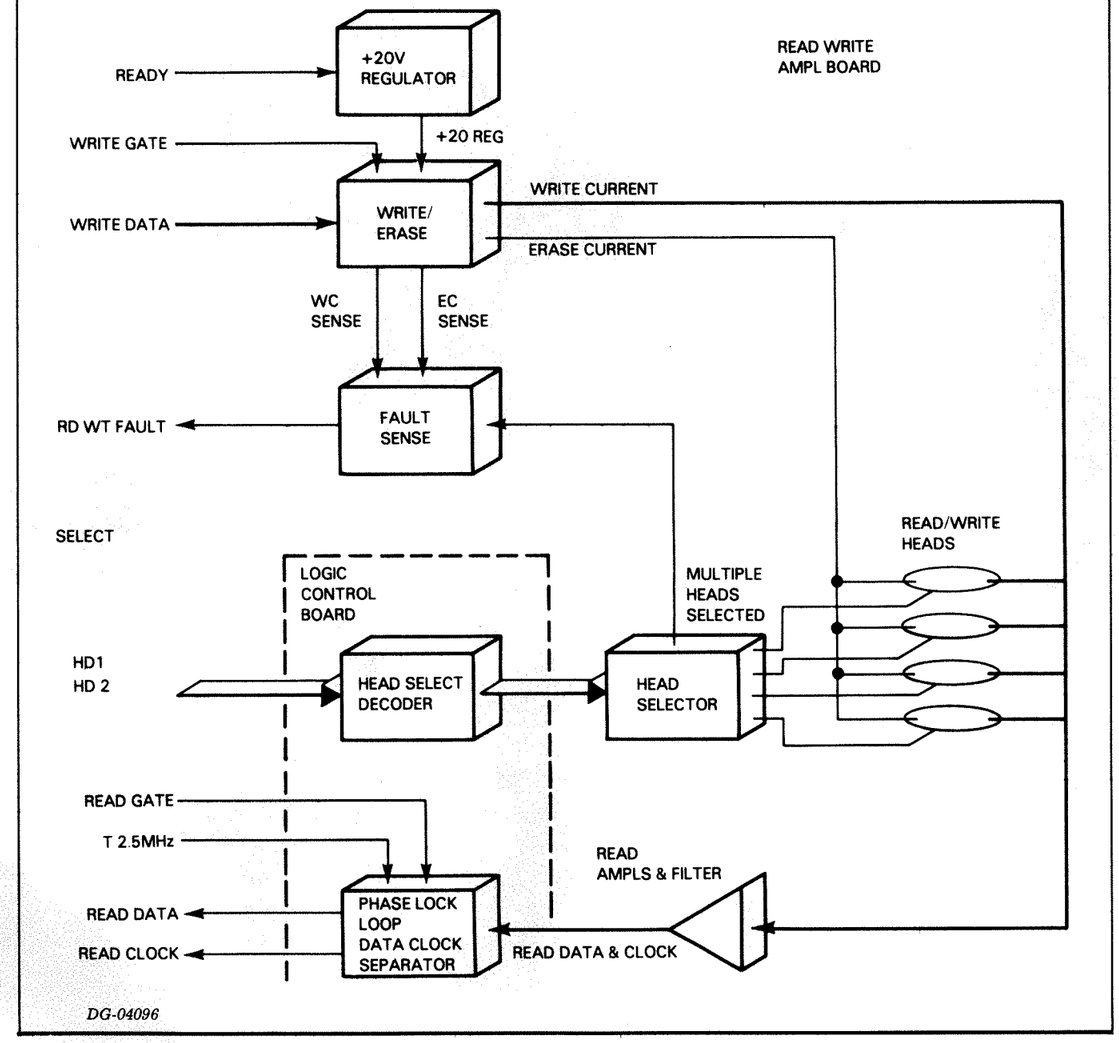
The block diagram to the right shows the circuits that support data transcription. It is divided into three sections; head select, read, and write.

The head select decoder accepts a two bit address from the controller and enables one of the four heads via the head selector. The head selector checks that no more than one head is selected at a given time, and signals a read/write fault if the circuits malfunction.

The write current driver accepts 2F encoded data and alternates the current in the selected head. Current flows continuously in the associated erase coil, which trims the written track. A 20 volt regulator supplies both currents and is disabled if the drive is not ready to execute data transfers. The fault sensor checks for two sources of error. If write and erase currents are not present during a write operation, or if write current is present during other operations, the sensor signals a read/write fault.

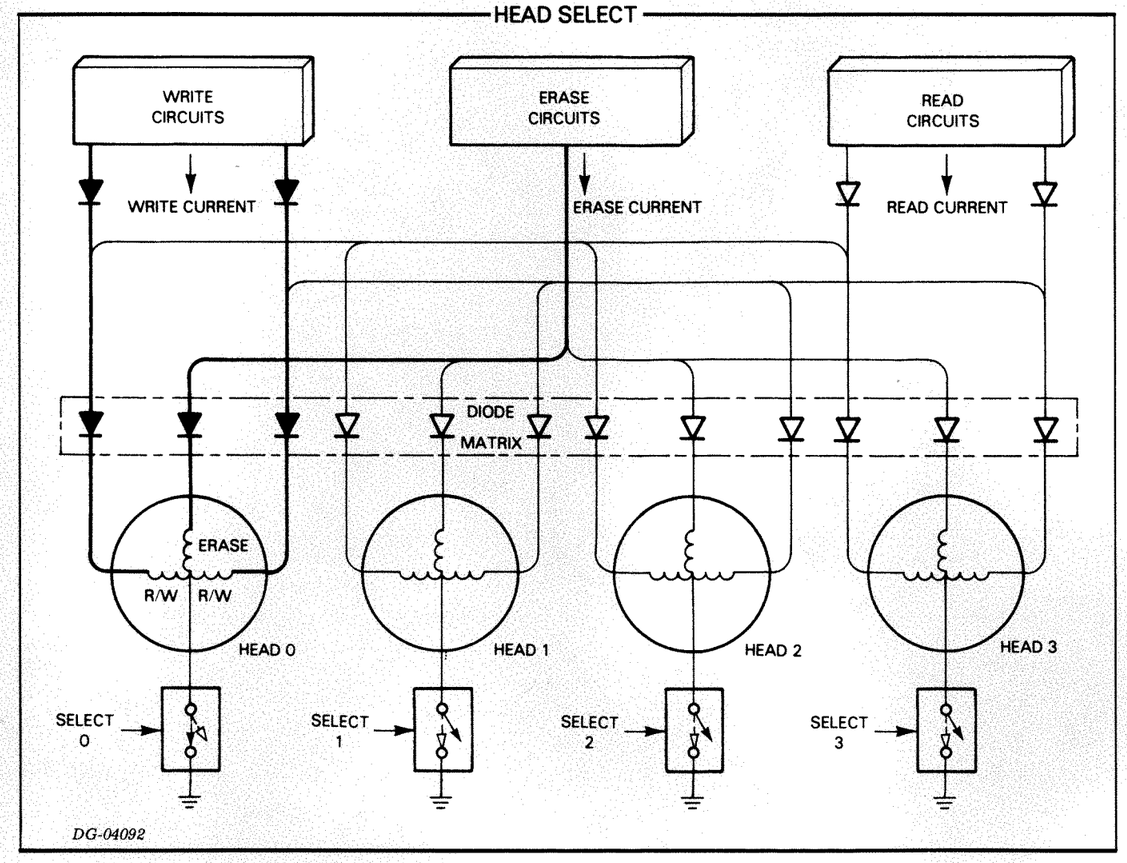
The read amplifier detects and amplifies read current pulses and sends the recovered 2F encoded data to the phase locked loop. When the read circuits are idle, a precision 2.5MHz clock trains the phase locked loop and keeps it running at the expected data rate. When a read operation begins, the actual data stream replaces the clock as the reference input to the loop. Normally, the loop need only make a phase adjustment to lock to the clock pulses in the data stream and this reduces the time that the read circuits need to synchronize with the data (phase locked loops take time to shift to a new frequency because they employ feedback and must therefore have a limited frequency response for stability). The output from the loop provides a synchronous data clock. This allows the data separator to identify the centers of the bit cells and look for ones. The separator then clocks the recovered binary bit stream to the controller.

READ/WRITE LOGIC BLOCK DIAGRAM



Head Selection - some details

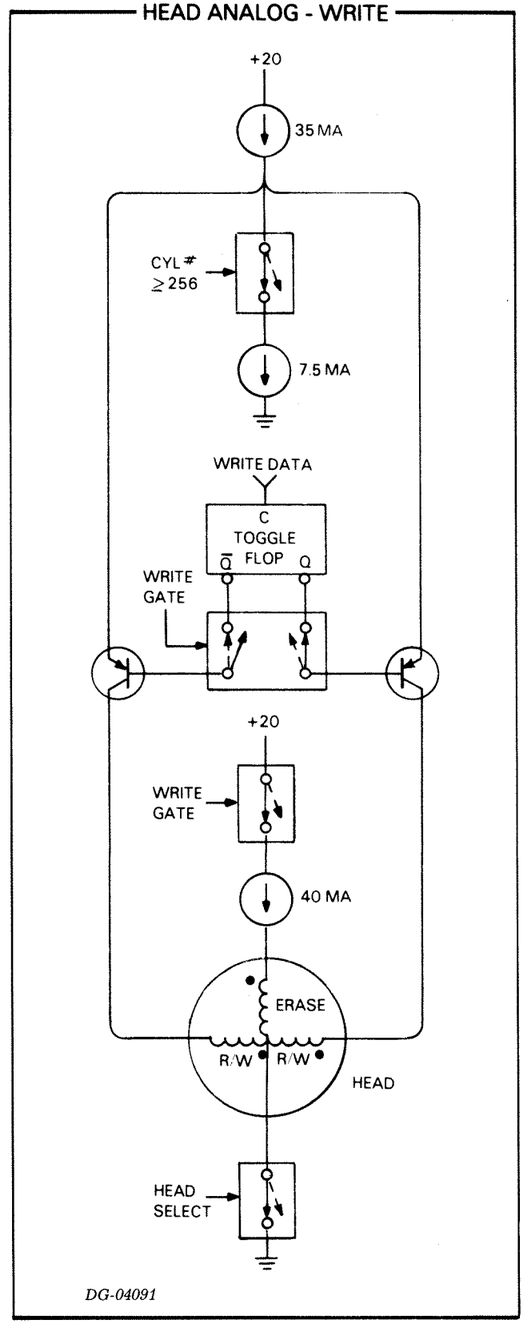
The heads connect to the read and write circuits through a diode matrix. Read, write and erase currents flow through this matrix to the selected head and return to ground through the head select switch. No current flows in the remaining heads and the associated matrix diodes isolate them from the read and write circuits.



Write Circuits - some details

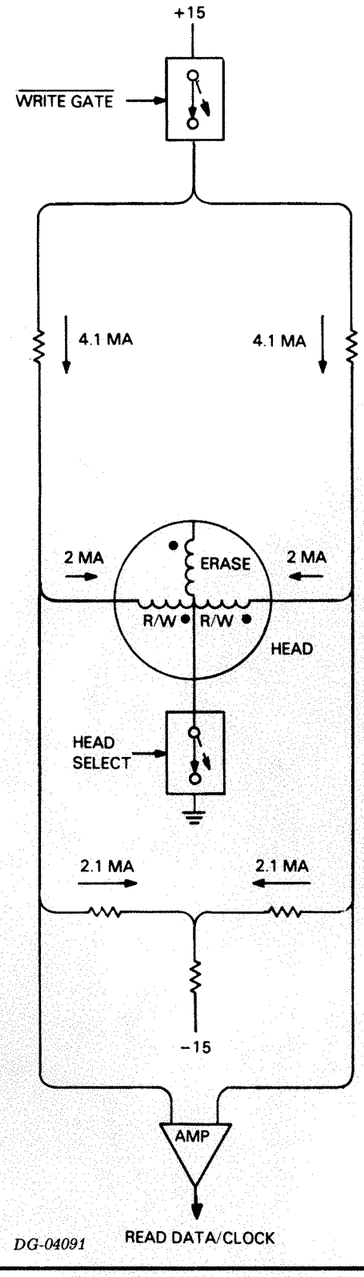
The diagram to the right shows a selected head in the write configuration. The matrix diodes have been omitted for clarity. The write flip/flop receives **2F** encoded data pulses from the controller. Each pulse toggles the flop and its complementary outputs drive a differential switch which alternates current flow in each half of the read/write coil. The coil halves are wound with opposite polarities so the current alternations cause flux reversals in the head to be recorded on the disc.

The write current varies with head position. As the head moves forward (toward the center of the disc) it sees decreasing surface velocity. This lowers the aerodynamic lift. The write circuits reduce the write current from 35ma at the outer tracks to 27.5ma at the inner tracks (256 through 407) to prevent field fringing and poor resolution at the flux boundaries that would otherwise occur as the head flies closer to the disc surface. During the entire write cycle, 40ma of current flows in the erase head. The write and erase current return through the head select switch to ground.



IX

HEAD ANALOG - READ



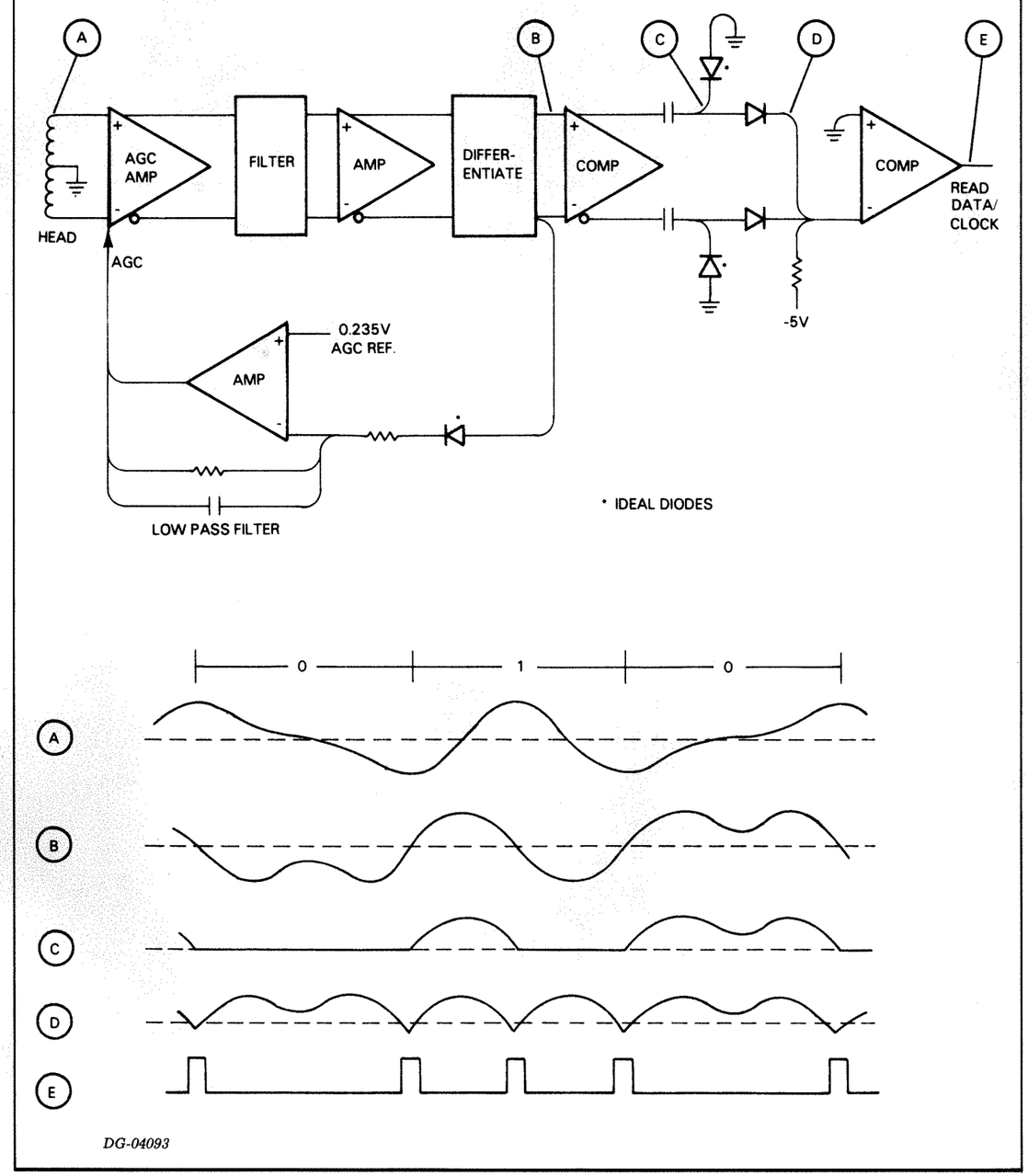
DG-04091

Read Circuits - some details

The diagram to the left shows a selected head in the read configuration. The matrix diodes have again been omitted for clarity. During a read operation, 2ma of current flows continuously in each half of the read/write coil. This current forward biases the matrix diodes and improves the sensitivity and linearity of the head. When a flux roversal occurs, the head current varies differentially due to the opposing polarities of the coils. That is, as the current increases in one coil, it decreases an equal amount in the other coil. A resistive terminator converts the head current to a differential voltage and this signal drives the read amplifier.

The data/clock recovery circuits shown to the right amplify the differential read signal and detect the signal peaks that correspond to flux transitions. The read signal is amplified, filtered to reduce the harmonic content, amplified again and finally differentiated. The result is a waveform that has zero crossings at the corresponding flux transitions. This signal is fed back to control the gain of the amplifier (automatic gain control, AGC). When the average amplitude of the signal envelope exceeds the AGC threshold, the feedback polarity reverses and decreases the gain of the amplifier. The differentiator also drives a peak detector that rectifies the signal and detects the minima to produce a pulse for each corresponding flux transition.

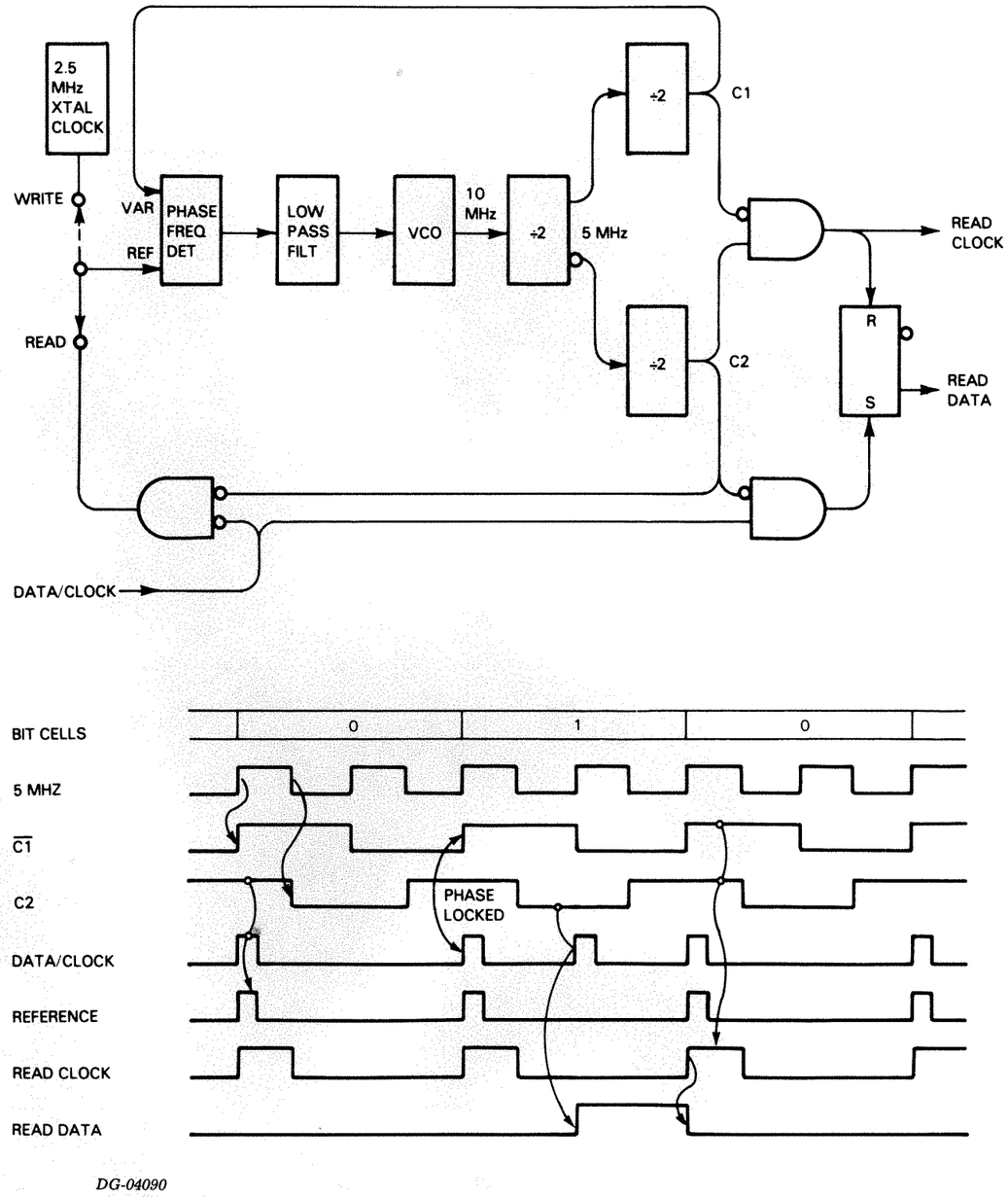
READ ANALOG CIRCUITS



DG-04093

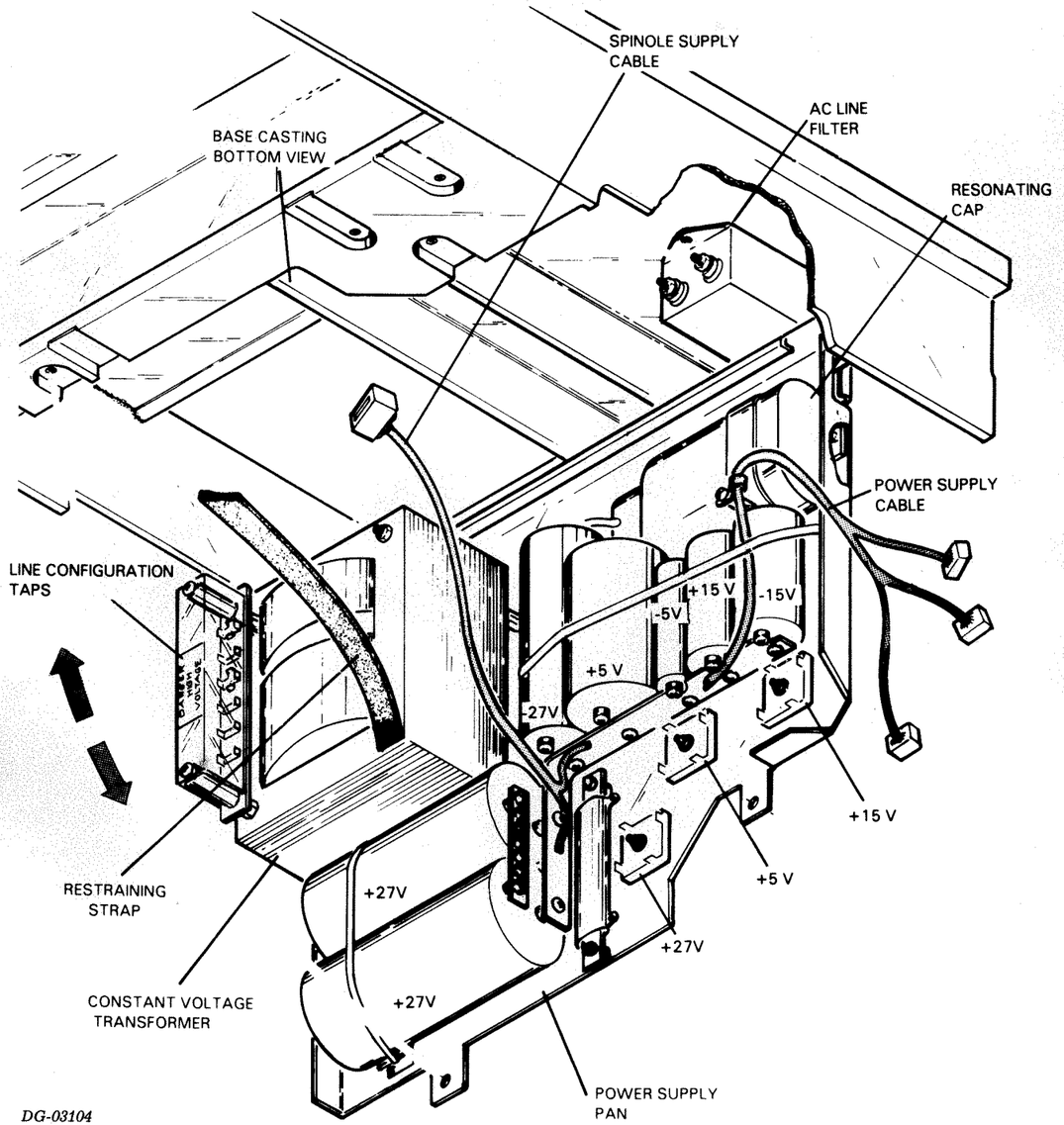
The phase locked loop shown to the right separates the data and clock pulses. The sector format guarantees that the data stream is a string of zeros (clock pulses) when a read operation begins. The phase locked loop locks onto this read signal in frequency and phase and produces a clock (**C1**) that has positive transitions at the bit cell boundaries, and negative transitions at the centers. An additional clock (**C2**) leads **C1** 90 degrees in phase and is therefore positive in the vicinity of the bit cell boundaries, and negative in the vicinity of the centers (where ones pulses appear). **C2** is used to separate clock and data pulses. When **C2** is high, it lets clock pulses through to the phase locked loop. When **C2** is low, it lets data pulses through to the data recovery flip flop. **C1** and **C2** combine to form a clock signal that strobes the output of the data recovery flip flop to the controller.

DATA/CLOCK SEPARATION



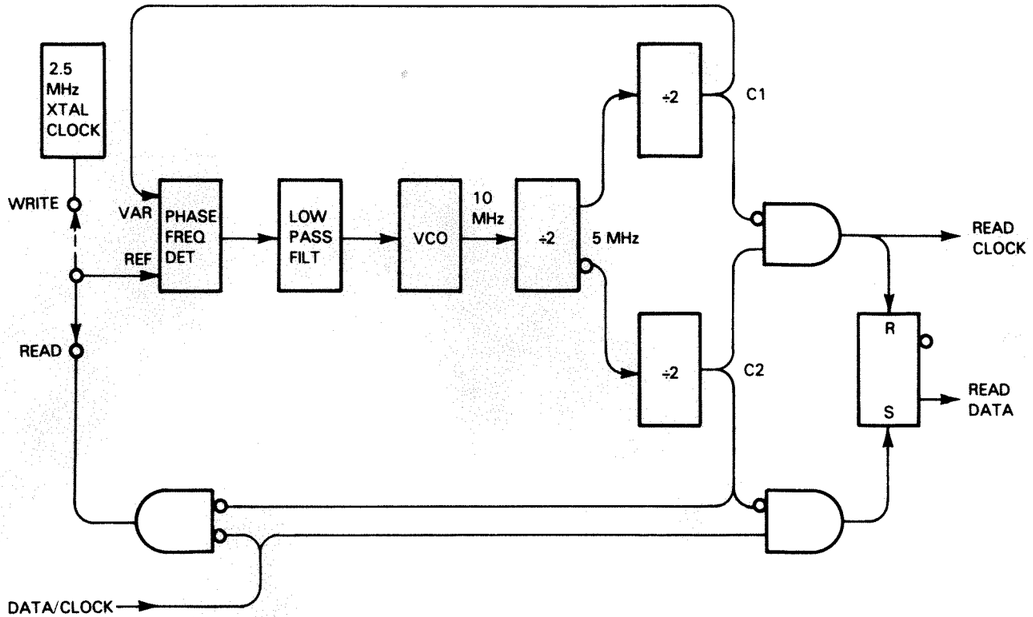
DG-04090

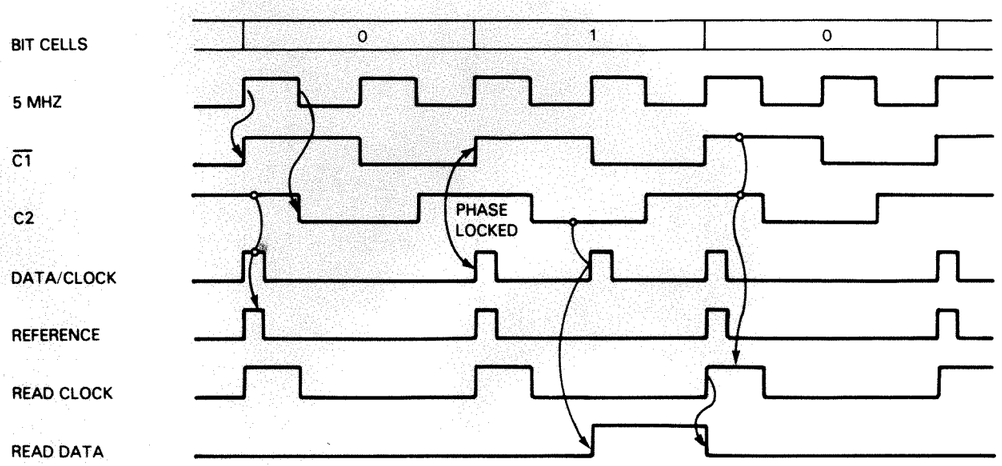
POWER SUPPLY PAN



The phase locked loop shown to the right separates the data and clock pulses. The sector format guarantees that the data stream is a string of zeros (clock pulses) when a read operation begins. The phase locked loop locks onto this read signal in frequency and phase and produces a clock (**C1**) that has positive transitions at the bit cell boundaries, and negative transitions at the centers. An additional clock (**C2**) leads **C1** 90 degrees in phase and is therefore positive in the vicinity of the bit cell boundaries, and negative in the vicinity of the centers (where ones pulses appear). **C2** is used to separate clock and data pulses. When **C2** is high, it lets clock pulses through to the phase locked loop. When **C2** is low, it lets data pulses through to the data recovery flip flop. **C1** and **C2** combine to form a clock signal that strobes the output of the data recovery flip flop to the controller.

DATA/CLOCK SEPARATION

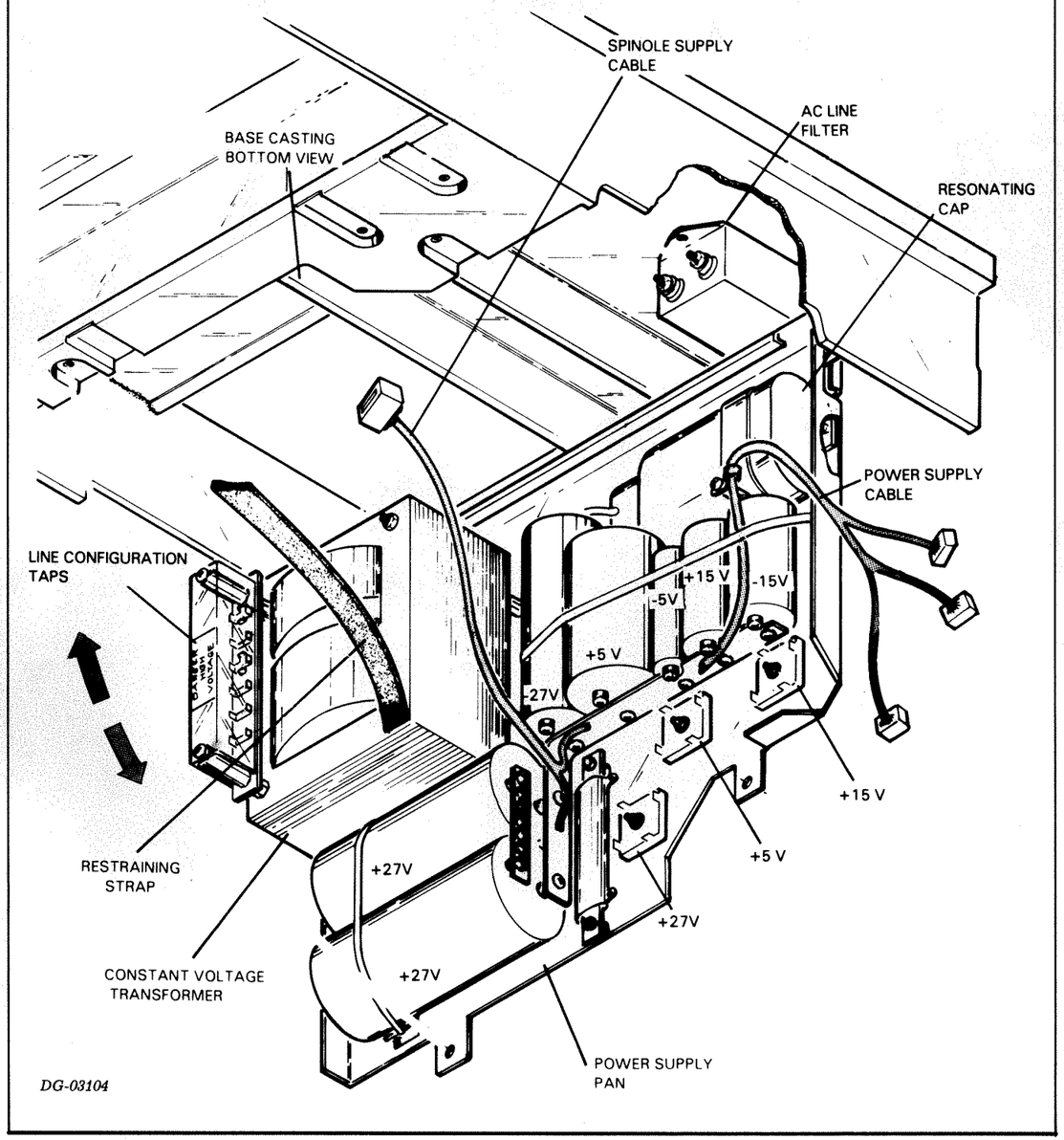




DG-04090

IX

POWER SUPPLY PAN

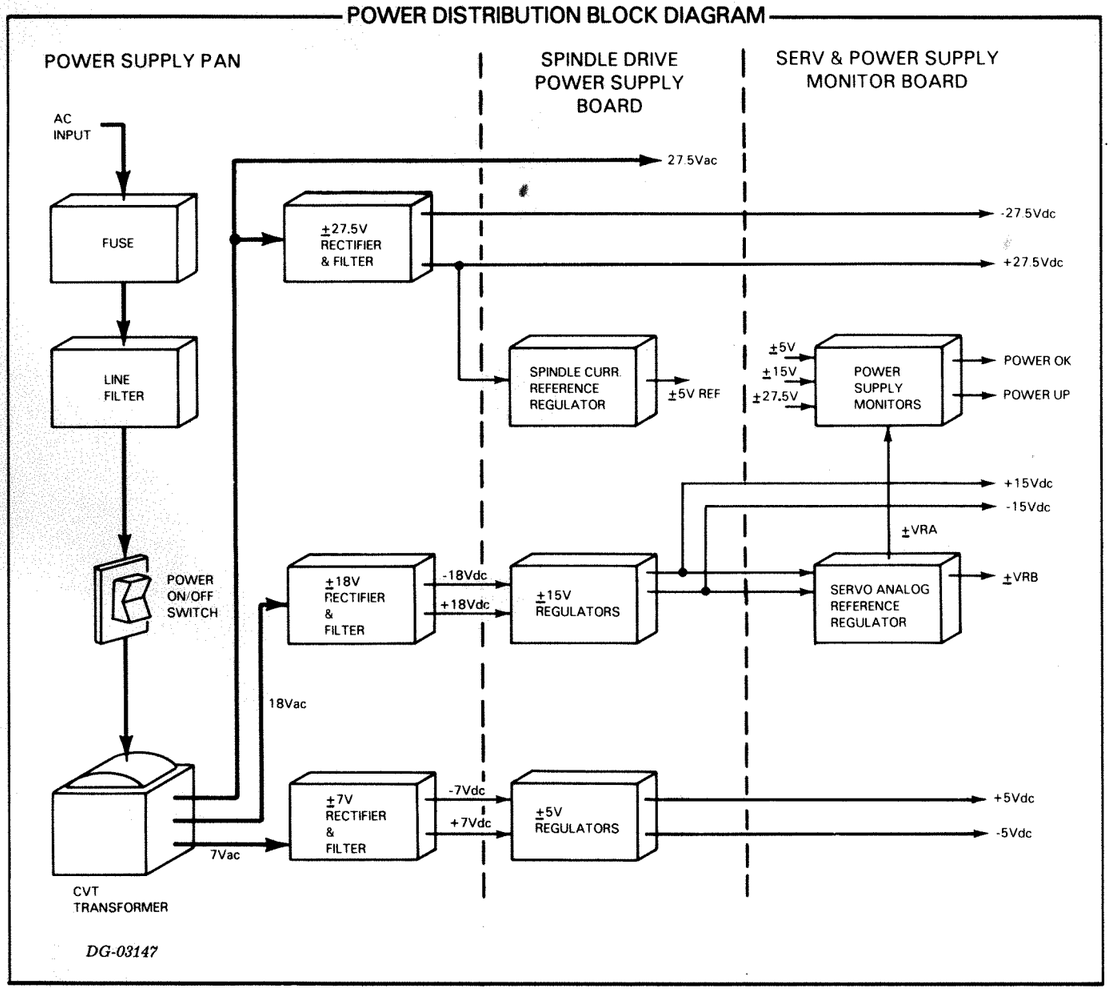


CHAPTER X
DRIVE: POWER SUPPLY

INTRODUCTION

The power supply circuits are distributed throughout the drive and include the bulk dc supply mounted on the power supply pan, the main dc regulators on the spindle board, the power monitors on the servo board, and several auxiliary regulators mounted on the spindle, servo and read/write boards. The block diagram shows the central power distribution system.

POWER DISTRIBUTION BLOCK DIAGRAM



DG-03147

X

AC SUPPLY

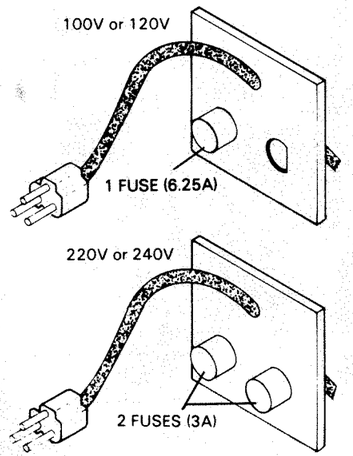
The drive can operate from one of five nominal ac line voltages tabulated below. The single phase voltages (100 and 120) require one 6.25 amp line fuse, and the two phase voltages require two 3 amp fuses. A filter removes high frequency noise on the AC line that might otherwise degrade drive operation. The on/off switch connects the output of the filter to the ferroresonant (CVT) power transformer, the blower, and the power supply cooling fan.

NOMINAL AC INPUT REQUIREMENTS

LINE VOLTAGE +10%,-15%	LINE FREQUENCY ±1Hz	LOAD AMPS	READY AMPS	SEEKING AMPS	BRAKING AMPS
100	50	1.6	3.10	4.15	3.6
100	60	1.18	2.6	3.50	3.3
120	60	1.03	2.33	3.16	2.75
220	50	0.77	1.49	2.0	1.7
240	50	0.64	1.45	1.9	1.6

DG-04097

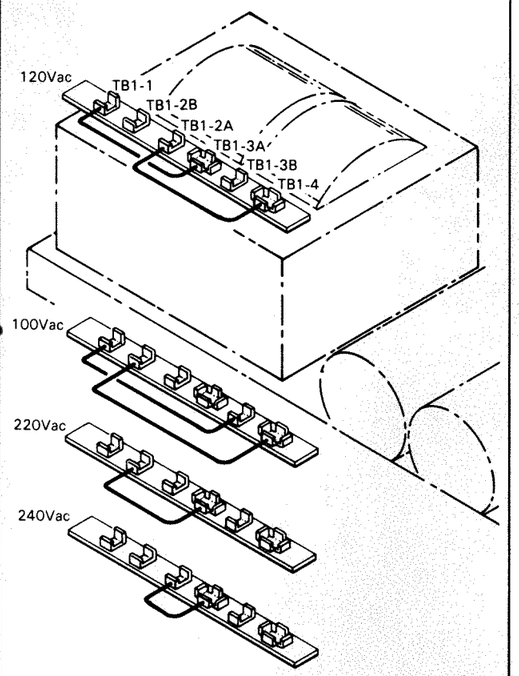
FUSING



DG-03105

The transformer has two primary windings. They can be connected in parallel for 100 or 120 volt operation, or in series for 220 or 240 volts. The figure below shows the jumper configurations for the different input voltages. The blower and ventilation fan connect across one of the primary windings and always operate at 100 to 120 volts (at 220 or 240 volts, the series connected windings act as an autotransformer to half the line voltage). Different transformers accomodate 50 and 60Hz operation.

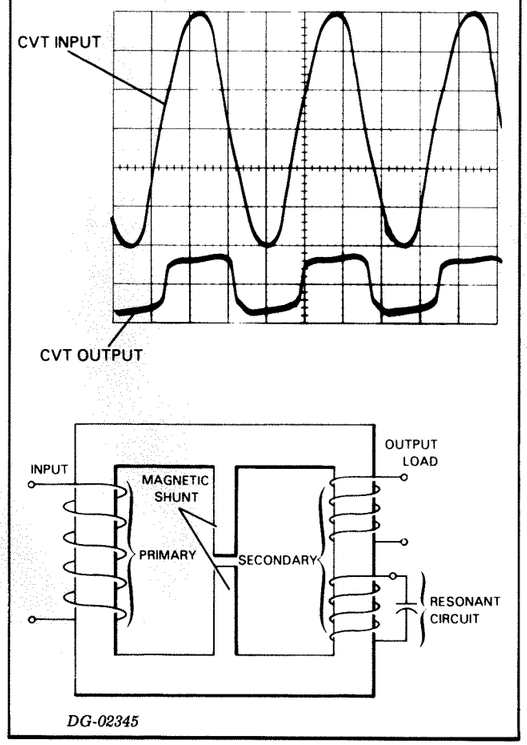
JUMPER SELECTION



DG-04097

The structure of a constant voltage transformer differs from that of a conventional transformer. A magnetic shunt and resonant winding are added to control flux linkage between the primary and secondary winding. When the primary voltage (and therefore the primary flux density) exceeds a minimum value, the resonant winding saturates the secondary half of the transformer core. This happens irrespective of the amount of current flow in the secondary windings. As the primary current rises, the additional flux is short circuited through the magnetic shunt, and does not link the secondary windings. This mechanism maintains a fixed secondary flux density, regulating the secondary voltages. Because the secondary half of the core is saturated, the transformer inherently limits current in the secondary windings. As the secondary core saturates at the onset of each half cycle of the primary voltage, the transformer provides square wave outputs.

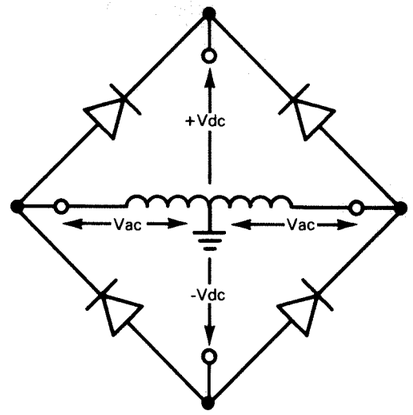
CUT OPERATION SUMMARY



DG-02345

The secondary windings provide six coarsely regulated ac voltages. Three rectifier modules convert the transformer outputs to six bulk dc voltages, tabulated below. The three center taps are connected together to form a common dc ground return that connects to the drive case along with the ground conductor in the ac power cord.

RECTIFIER



DG-04099

NON-REGULATED DC POWER SUPPLY OUTPUT VOLTAGES

VOLTAGE	CURRENT	RIPPLE	PROTECTION	
			OVERCURRENT	OVERVOLTAGE
+7	5a	350mV	LIMITED	LIMITED
-7	100mA	160mV	TO	TO
+18	320mA	400mV	+100%	+20%
-18	180mA	300mV	BY CVT	BY CVT
+27.5	24A(PEAK)	N/A	TRANSFORMER	TRANSFORMER
-27.5	10A(PEAK)	N/A		

The drive uses some of the bulk voltages to power the spindle and positioner motors and the drawer lock solenoid. The brush motor runs directly off the 27.5 volt ac winding. The bulk supply also drives several regulators distributed throughout the drive that power the drive circuits.

REGULATORS

Four series pass regulators on the spindle board provide the major dc operating voltages tabulated below. The + 5 volt regulator is implimented with an integrated circuit and discrete components. The remaining regulators are fixed three-terminal devices that can only be serviced as a unit.

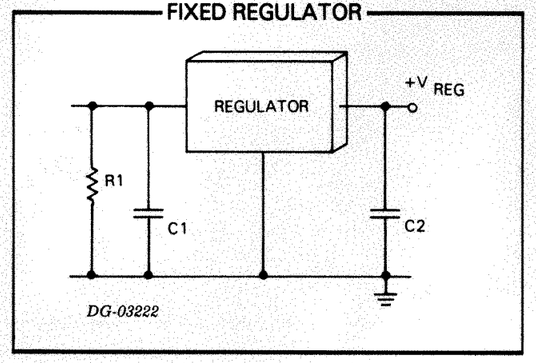
STEADY STATE DC POWER SUPPLY OUTPUT VOLTAGES

VOLTAGE	LOAD REGULATION	RIPPLE	PROTECTION		
			OVERCURRENT	OVERVOLTAGE	THERMAL
+5	+100mV	40mV	4 8 Amps	Function of CVT Transformer	NA
-5	+300mV	25mV	Internal		Internal
+15	+500mV	30mV	Internal		Internal
-15	+500mV	30mV	Internal		Internal

86-03225

Fixed Voltage Regulators

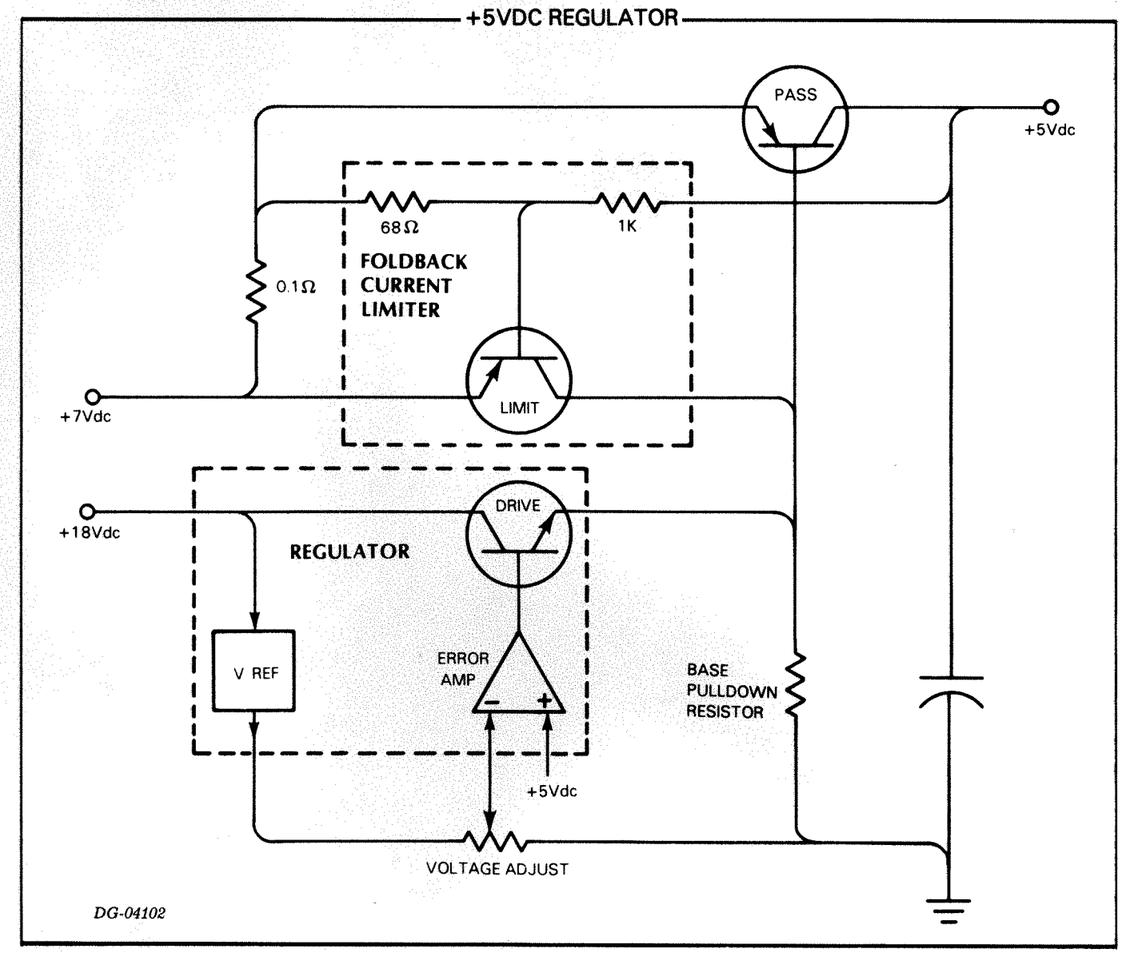
The followiing schematic shows the external components attached to a fixed voltage regulator. Capacitor C1 filters the bulk supply and resistor R1 is a bleeder. Capacitor C2 supports high frequency current demands and therefore improves the transient response. The regulator cannot be adjusted and is internally current limited.



+5 Volt Regulator

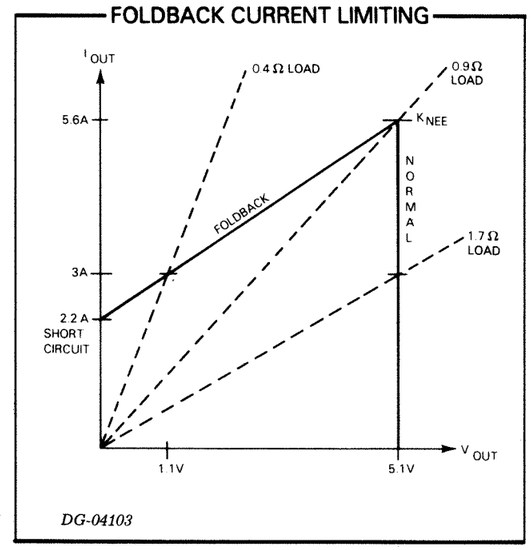
The +5 volt regulator shown below includes an integrated circuit voltage regulator and several discrete components to adjust and amplify the output and provide current limiting. The regulator uses negative feedback to lock its output voltage to an adjustable reference. A comparator detects differences between the output and reference voltages, and adjusts the output to track the reference.

To illustrate the operating principle, let us examine the responce to a transient output change. Assume the load current suddenly increases and the output sags. This causes a negative error and the error amplifier biases the drive transistor toward cutoff. There is now more base drive available for the pass transistor (the drive transistor diverts less current around the pass transistor and into the base pulldown resistor) and the output voltage rises until the loop again balances. An output capacitor absorbs high frequency current transients that the regulator cannot handle due to its limited frequency response.



The regulator includes a foldback current limiter to prevent excessive current flow and power dissipation in the pass transistor. The limiter reduces current flow as the output sags and so holds the dissipation in the pass transistor (which senses an increasing voltage drop) to a preset maximum. The limit transistor receives negative feedback from the 0.1 ohm current sensing resistor, and shunts base drive around the pass transistor if the current threshold is exceeded. As the voltage begins to sag, positive feedback from the output (via the 1 K resistor) further depresses the current flow until it is sufficiently reduced and the positive and negative feedback components balance.

The following curve shows the limiting action. It depicts load lines and resulting current flows for three load resistances.

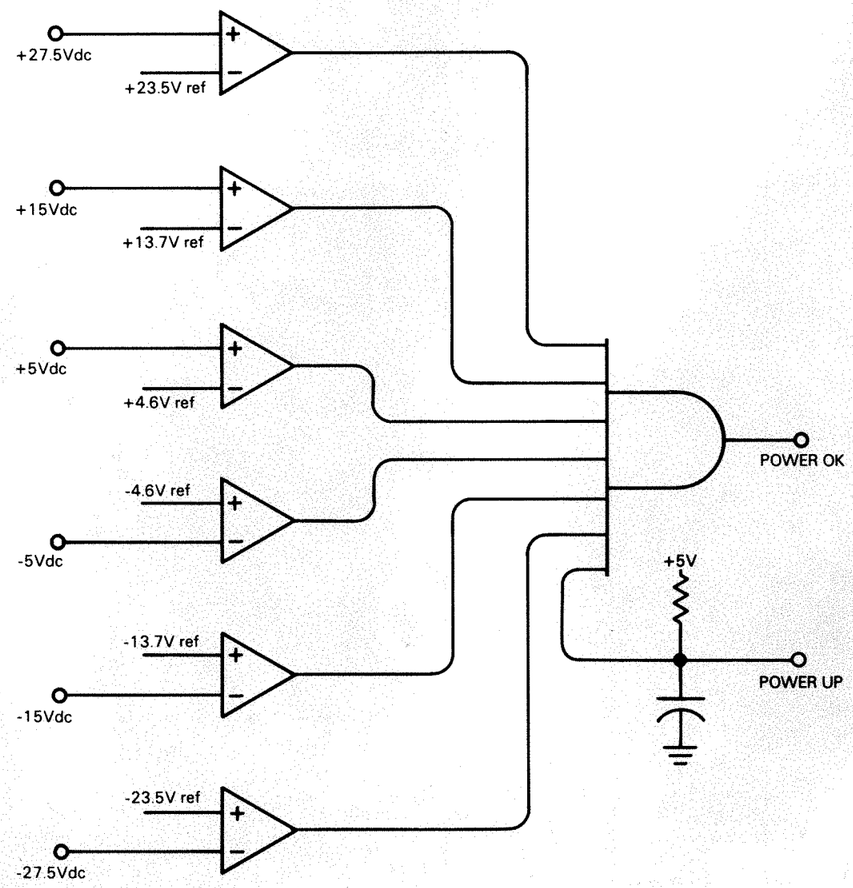


X

POWER CHECK

The servo board contains six comparators that look for undervoltage conditions on ±27.5, ±15, and ±5 volts. An undervoltage causes an emergency retract and disables the spindle. An additional signal called **Power Up** maintains the fault indication, during very low voltage conditions.

POWER CHECK LOGIC



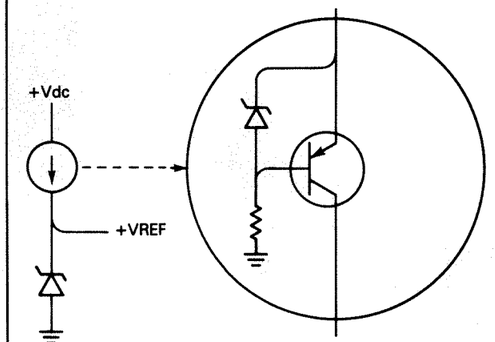
DG-04100

AUXILIARY REGULATORS

Some of the boards contain additional regulators that supply write and erase current, power the position sensor lamp, and provide precision references for level sensing circuits. They are all shunt regulators of different phase. The simple ones drive a zener directly from a series resistor. Where greater accuracy is required, a second shunt stage is added. In this configuration, the first stage drives a constant current source which supplies the zener current for the second stage. This reduces variations in output voltage that would otherwise occur as changes in supply voltage alter the zener current (zeners have internal resistance, so their voltage drop varies with current).

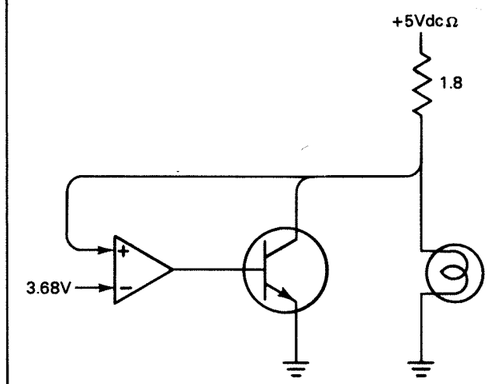
The power for the position transducer lamp driver uses one of the precision zener references to regulate the lamp current. Variations in lamp intensity change the amplitude of the position signal **Sinx**, which alters the position loop gain. It is very important to control the lamp intensity to prevent oscillation or variations in settling time. As the lamp reaches the end of its life, drive operation can degrade.

REFERENCE REGULATOR



DG-04104

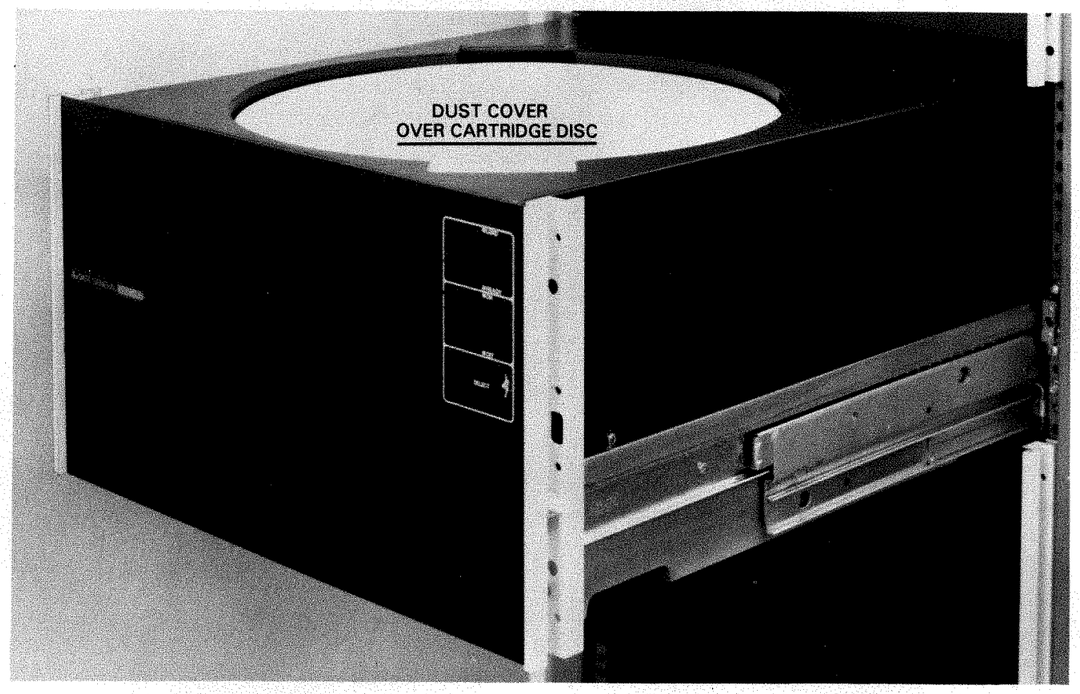
LAMP REGULATOR



DG-04101

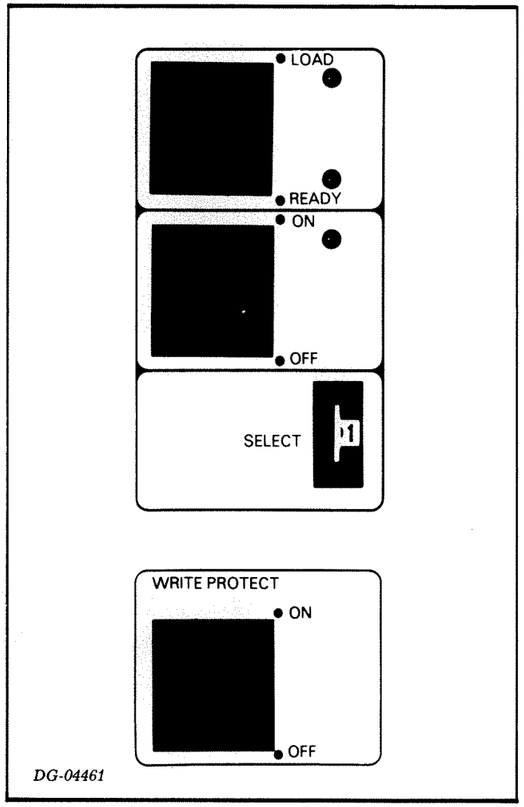
APPENDICES

APPENDIX A
OPERATORS GUIDE



OPERATOR CONTROLS

The operator controls are located on the front panel of the disc drive, and consist of three two-position rocker switches, a thumbwheel switch, and three indicator lights.

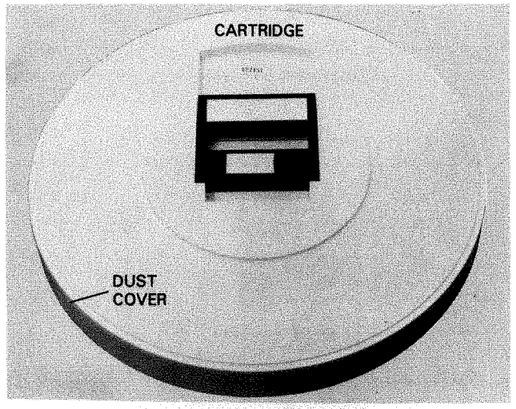


Operation is as follows:

Control	Function
ON/OFF *rocker switch*	Turns power on or off to the disc drive. Set this switch to ON as the first step to bring the disc drive on-line with the computer. The drive cannot slide out of the cabinet to load the cartridge disc unless this switch is ON. Set this switch to OFF to completely shut down the disc drive. The LOAD indicator light should be illuminated before turning this switch OFF. NOTE: LOAD/RUN switch should be in LOAD position and LOAD light should be lit before trying the switch.
ON *indicator light*	When ON, indicates that power is supplied to the drive at proper levels. When OFF, indicates that the drive is completely shut down or power at Low Level.
LOAD/READY *rocker switch*	Starts and stops the disc drive, permits loading and unloading the cartridge disc by unlocking the drive from the cabinet. Set to LOAD to stop the disc drive, and to unlock the drive to slide out of the cabinet and thereby permit a cartridge disc to be loaded. This switch should be in the LOAD position before turning off the power to the drive. Set to READY to start the disc drive. Do NOT set to READY unless the cartridge disc is loaded and the drive is slid back into the cabinet.
LOAD *indicator light*	When ON, indicates that the drive is stopped; the drive can be extended on the slides, and the cartridge disc may be interchanged. The discs may continue rotating for up to 1 second after the load light illuminates. If the drive is operated in the extended position, wait for pack rotation to stop! When OFF, indicates that the drive is locked in the cabinet.
READY *indicator light*	When ON, indicates that the drive is on-line with the computer, has not faults or interlocked to inhibit operation, and is ready to accept and execute program commands. When OFF, indicates that the drive is not on-line, or that a fault is set to inhibit operation. This light is OFF during load operations. NOTE: The READY light may blink on and off during normal operation. This is no cause for concern unless the light remains extinguished for more than one second. The READY light is OFF during the time when the drive is seeking to a cylinder.
SELECT *thumbwheel switch*	Selects the logical unit number for the drive. This switch is used to assign logical unit number 0, 1, 2 or 3 to the disc drive, as indicated by the number displayed. Normally, this number is set at installation and need not be changed. **NEVER** change the switch setting when the disc drive is on-line, or data may be lost; if necessary to change the setting, ensure that the drive is off-line.

Notes on Removable Disc Cartridges

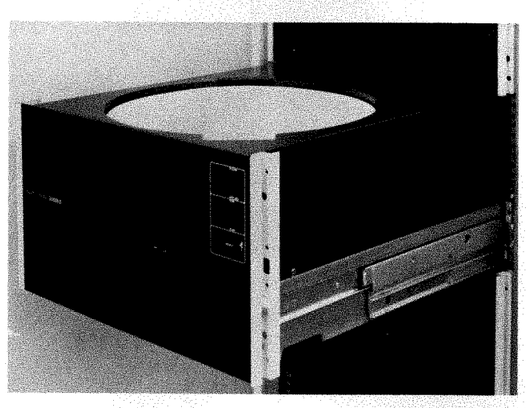
The removable disc cartridge and its dust cover are shown in the figure. The removable disc is permanently sealed inside the cartridge, and the read/write heads gain access to the disc through an opening in the side of the cartridge. When properly loaded in the disc drive, two horizontal arms, each supporting a read/write head, are positioned to straddle the disc. When the LOAD/READY switch is set to READY, the disc accelerates to operating speed and the heads are positioned to read or write on their corresponding disc surfaces. As soon as this is condition is met, the READY light illuminates, if no faults or interlocks are set to inhibit operation.



NOTE *The READY light may not illuminate immediately if there is a substantial temperature difference between the cartridge disc and the drive.*

The Model 6050 Cartridge Disc Drive accepts a unique cartridge disc, which may be ordered from Data General and is specifically tailored for this unit. Do NOT attempt to use a cartridge disc intended for another drive, even if the cartridge appears similar to the Model 6050 cartridge.

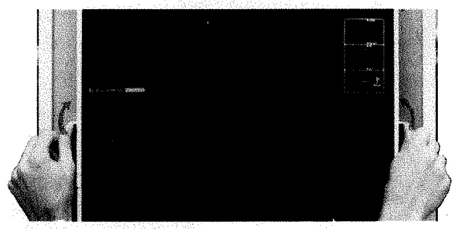
The disc is a delicate, precision device which requires particular care during handling and storage to ensure the integrity of the data stored within it. Use the handle on top of the cartridge when transporting the disc, and always install the dust cover on the cartridge as soon as it is removed from the drive.

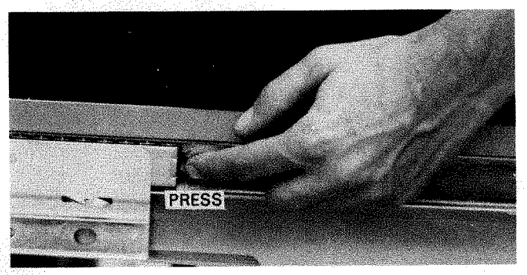


OPERATING PROCEDURES

Loading

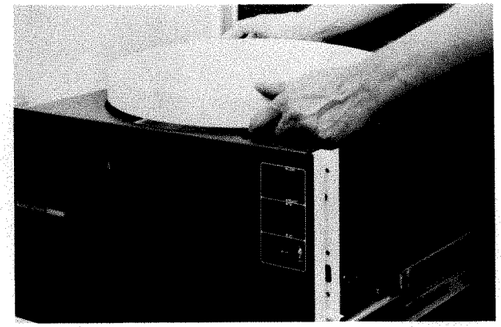
1. Ensure that the power switch is ON.
2. Ensure that the disc drive is released from the computer system.
3. Turn the LOAD/READY switch to LOAD.
4. Wait for the LOAD light to illuminate.
5. Release the front panel latches, and slide the drive out of the cabinet until it stops. Do NOT release any slide detents.





NOTE *If the drive is inadvertently moved beyond the operator's position by releasing the detents, it can be moved back by releasing the detents as shown.*

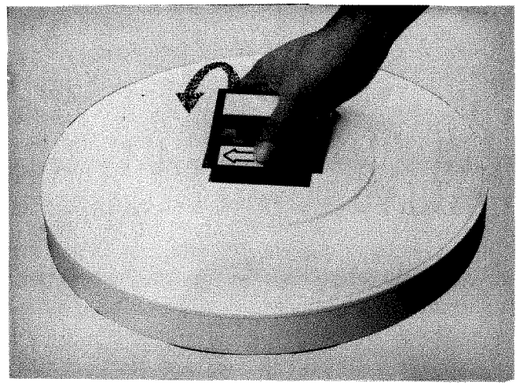
6. Remove the dust cover, if present, from the top of the drive.



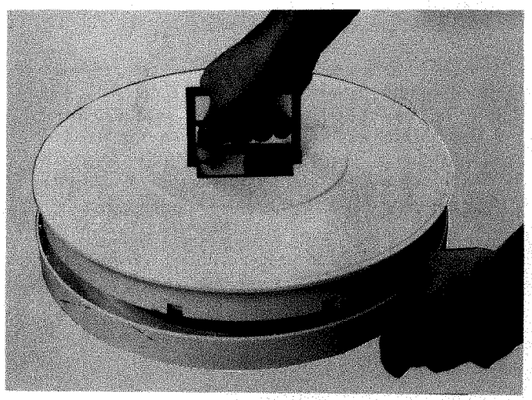
NOTE *It is good practice to ensure that the cavity and spindle are clean and free of dust and contaminants. Use a lint-free tissue to clean the cavity and spindle if necessary.*

7. Remove the dust cover from the bottom of the cartridge to be installed as follows:

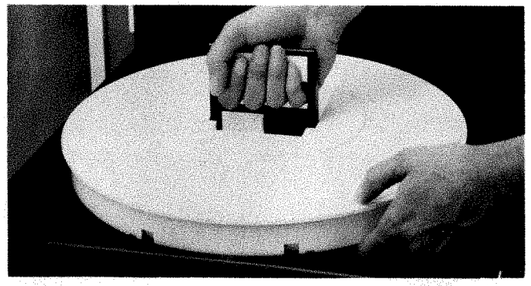
   Slide the latch plate to the left as shown.



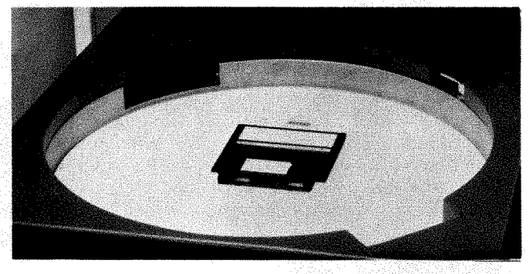
   Lift the handle straight up, and lift the cartridge up and out of the dust cover.



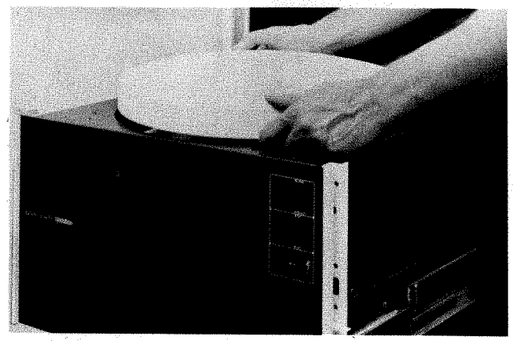
8. Hold the cartridge by the handle, and place it into the cavity on top of the drive as shown. The cartridge will fit into locating lugs when properly positioned, and slide smoothly into the cavity and seat on the spindle.



9. Lower the cartridge handle until it is flat on the cartridge.



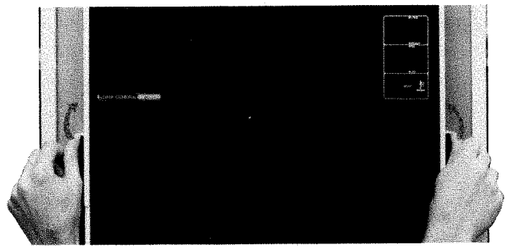
10. Place the dust cover over the cartridge. Ensure that it seats in the cavity.

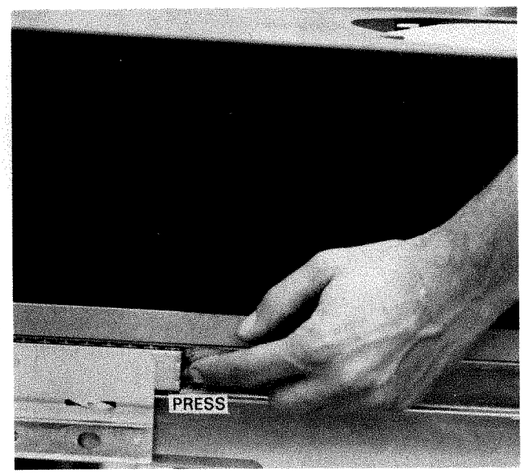


11. Slide the drive into the cabinet until the front panel latches engage and latch the drive in place.

Unloading

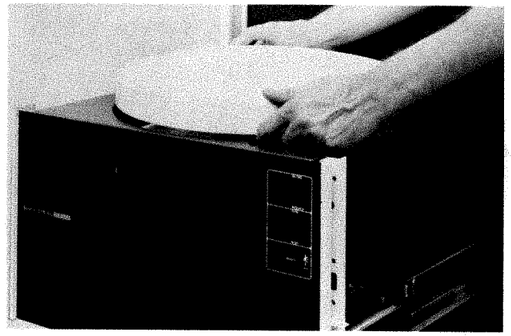
1. Ensure that the power switch is ON.
2. Ensure that the disc drive is released from the computer system.
3. Turn the LOAD/READY switch to LOAD.
4. Wait for the LOAD light to illuminate.
5. Release the front panel latches, and slide the drive out of the cabinet until it stops. Do NOT release any slide detents.





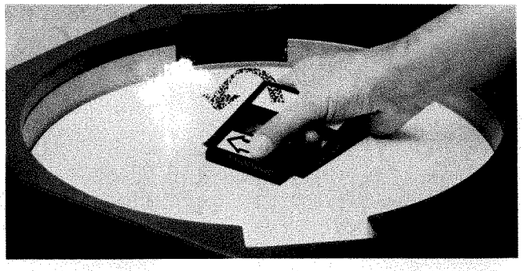
NOTE *If the drive is inadvertently moved beyond the operator's position by releasing the detents, it can be moved back by releasing the detents as shown.*

6. Remove the dust cover from the top of the drive, exposing the disc cartridge to be removed.

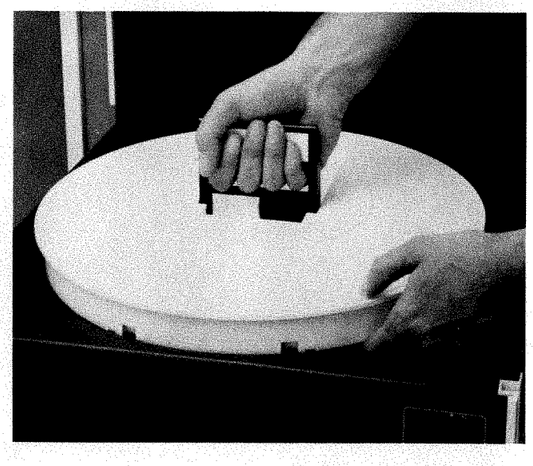


7. Remove the disc cartridge as follows:

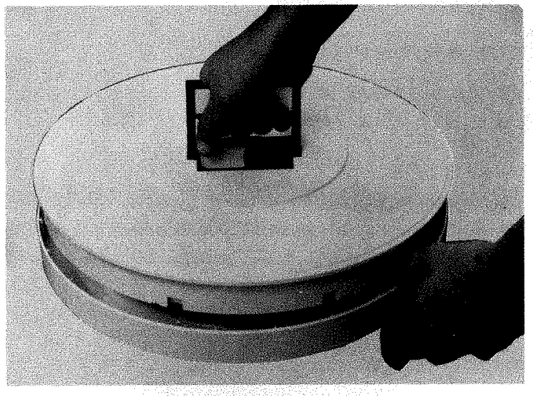
   Slide the latch plate to the left as shown.



   Lift the handle straight up, and carefully lift the disc cartridge straight up and out of the drive.



8. Place the cartridge into the dust cover, and lower the cartridge handle until it is flat on the cartridge. The dust cover will magnetically latch to the cartridge. The cartridge may now be stored in a controlled environment, in accordance with the requirements given under "Disc Cartridge Care and Handling".



9. If another disc cartridge is to be installed, load it following the procedure under "Loading", steps 7-10. If no cartridge is to be installed, place a spare dust cover in the cavity in the disc drive, to minimize contamination in this area.

10. Slide the drive into the cabinet until the front panel latches engage and latch the drive in place.

Starting the Disc Drive

To start the disc drive and place it on-line with the computer system, proceed as follows:

1. Turn the power switch to ON. The ON indicator light will illuminate.

2. If there is no disc cartridge installed in the drive, load a cartridge following the procedure given under "Loading". If a disc cartridge is already installed, proceed to the next step.

3. Turn the LOAD/READY switch to READY.

4. Wait for the READY light to illuminate.

   If the READY light does not illuminate after one minute, turn the LOAD/READY switch to LOAD, wait for the LOAD light to illuminate, and then turn the LOAD/READY switch to READY again. If the READY light remains extinguished again, turn the LOAD/READY switch to LOAD and contact technical personnel for assistance.

   NOTE *If there is a substantial temperature difference between the cartridge disc and the drive, the READY light may not illuminate for 5 to 10 minutes. This is no cause for concern, but will merely increase start-up-time. To expedite the start-up procedure, it is good practive to store the cartridge in the computer room.*

5. When the READY light is illuminated, the disc drive is ready to accept and execute program commands.

Interchanging the Cartridge Disc

To interchange a cartridge disc with another one, proceed as follows:

1. Ensure that the disc drive is released from the computer system; the power ON light must be illuminated.

2. Unload the cartridge disc following the procedure given under "Unloading". Load the new cartridge following the procedure given under "Loading".

3. Ensure that the disc drive is latched back into the cabinet, and turn the LOAD/READY switch to READY.

4. Wait for the READY light to illuminate.

   If the READY light does not illuminate after one minute, turn the LOAD/READY switch to LOAD, wait for the LOAD light to illuminate, and then turn the LOAD/READY switch to READY again. If the READY light remains extinguished again, turn the LOAD/READY switch to LOAD and contact technical personnel for assistance.

   NOTE *If there is a substantial temperature difference between the cartridge disc and the drive, the READY light may not illuminate for 5 to 10 minutes. This is no cause for concern, but will merely increase the interchange time. To expedite interchanging cartridges, it is good practice to store them in the computer room.*

5. When the READY light is illuminated, the disc drive is ready to accept and execute program commands.

Shutting Down the Disc Drive

To completely shut down the disc drive, proceed as follows:

1. Ensure that the disc drive is released from the computer system.
2. Turn the LOAD/READY switch to LOAD.
3. Wait for the LOAD light to illuminate.
4. When the LOAD light is illuminated, turn the power switch to OFF.

NOTE *If desired, remove the cartridge disc when the LOAD light is illuminated, prior to turning the power OFF. Follow the procedure given under "Loading".*

DISC CARTRIDGE CARE AND HANDLING

Disc cartridges should be stored in the same environment as the computer room, to minimize temperature differences when a cartridge is placed in the drive. If a substantial temperature difference exists, the READY light on the drive will not illuminate until a reasonable temperature equilibrium is reached after the cartridge is installed.

NOTE *The cartridges may be safely stored over a temperature range of -40 to 150 deg. F. and 0% to 80% relative humidity. The cartridge may be instaled in the drive immediately after removal from this environment, but the drive will not be on-line until the READY light illuminates, which may take up to 10 minutes as the temperatures equilibrate.*

All disc cartridges must have the dust cover installed when not in the disc drive. The dust cover prevents contaminants from entering the cartridge during storage.

Store the disc cartridges, with dust cover attached, on a flat surface or vertically in a storage rack. NEVER stack cartridges on top of one another, nor stack other material on top of a cartridge.

Before storing disc cartridges, ensure that each cartridge is properly identified. Apply a pressure sensitive label to the top of the cartridge, and mark it with a felt tip pen or other insrument which will not deposit flakes or loose material. Do not use a graphite pencil.

The disc can be damaged by excessive pressure, abrasion, moisture or impact. Ensure that hands, pencils, liquids or other foreign objects do not touch the disc surface. Do not attempt to blow foreign material from a disc, as moisture contamination may result. If a disc cartridge is suspected of damage, do not use the disc until it is inspected by technically qualified personnel.

KEEP THE DISC CARTRIDGE AWAY FROM STRONG MAGNETIC FIELDS.

OPERATING NOTES

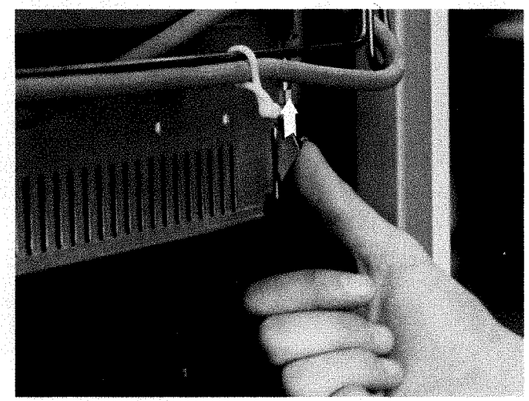
The following guidelines are provided as an aid to the operator in the maintenance and operation of the cartridge disc drives.

1. Never shut down the disc drive when the READY light is illuminated, or data may be lost.
2. Never unload or interchange a disc cartridge until the drive has been released from the computer system, or data may be lost. The system engineer can provide the procedure to release the disc for the particular operating system in use.
3. Keep a dust cover in place over the cartridge disc cavity to minimize entrance of contaminants.
4. Exercise care when the cavity is exposed, to prevent the entrance of smoke, dust or other contaminants into this area.
5. Never try to force the drive out of the cabinet; an interlock prevents the drive from moving unless power is turned ON.

   If necessary, the interlock may be overridden manually through the rear of the cabinet. This is an emergency procedure only, and is accomplished as follows:

   Unplug the power cord to the disc drive.
   Open the cabinet rear door.
   Raise the latch at the rear of the disc drive as shown, and push the drive forward.

6. Do not remove the disc cartridge for at least 1 second after the LOAD light comes on.



7. If the cartridge disc does not slide easily into the cavity in the drive, ensure that it is positioned correctly and engaged on the locating lugs. If difficulty is still encountered, examine the cavity and the underside of the cartridge for obstructions, such as paper clips, staples, or excess contamination. Clean the areas using a lint-free tissue and isopropyl alcohol, if necessary. If interference still persists, do not operate the drive, and contact technical personnel for assistance.
8. A sustained audible "tinging" or scratching sound during operation may be caused by head-to-disc contact (head crash). If this condition persists, unload the cartridge disc and shut down the disc drive. Do not operate the drive or use the cartridge disc until both have been inspected by qualified technical personnel.
9. A three position drive in place switch, located at the rear of the drive prevents the drive from operating in the extended position. Service personnel may override this feature by pulling out on the switch button.

MAINTENANCE

Operator Maintenance

The cartridge disc drive is designed to require no operator maintenance. Periodically, wipe the front panel of the drive using a lint-free tissue.

Environmental cleanliness is important for reliable operation of the cartridge disc drive. The drive is equipped with filters to remove air-borne contaminants, but excessive smoke or dust will reduce filter life. The computer room should be maintained as clean as possible.

It is very poor practice to use the drive as a counter-top for beverages, ashtrays, and the like, when it is slid out of the cabinet for operator procedures. Ensure that objects such as paper clips and staples do not fall into the disc cavity. If an object does fall in, do NOT operate the drive until the object has been removed and the cavity has been wiped clean.

Preventive Maintenance

After 1000 hours of operation or six months, whichever comes first, contact the nearest Data General Field Service office to arrange for preventive maintenance procedures by qualified technical personnel. These procedures consist of cleaning the filters and read/write heads, and should be performed on a regular schedule to ensure trouble-free operation.

APPENDIX B
DOCUMENTATION

RELATED DOCUMENTS

The following is a list of Data General publications and drawings dealing with the 6045/50/51 Cartridge Disc Subsystem.

PUBLICATIONS

015-000021 PROGRAMMER'S REFERENCE, PERIPHERALS
015-000057 TECHNICAL MANUAL, 6045 6050 6051 DISC DRIVES
015-000058 FIELD SERVICE PROCEDURES, 6045 6050 6051 DISC DRIVES

LOGIC SCHEMATICS

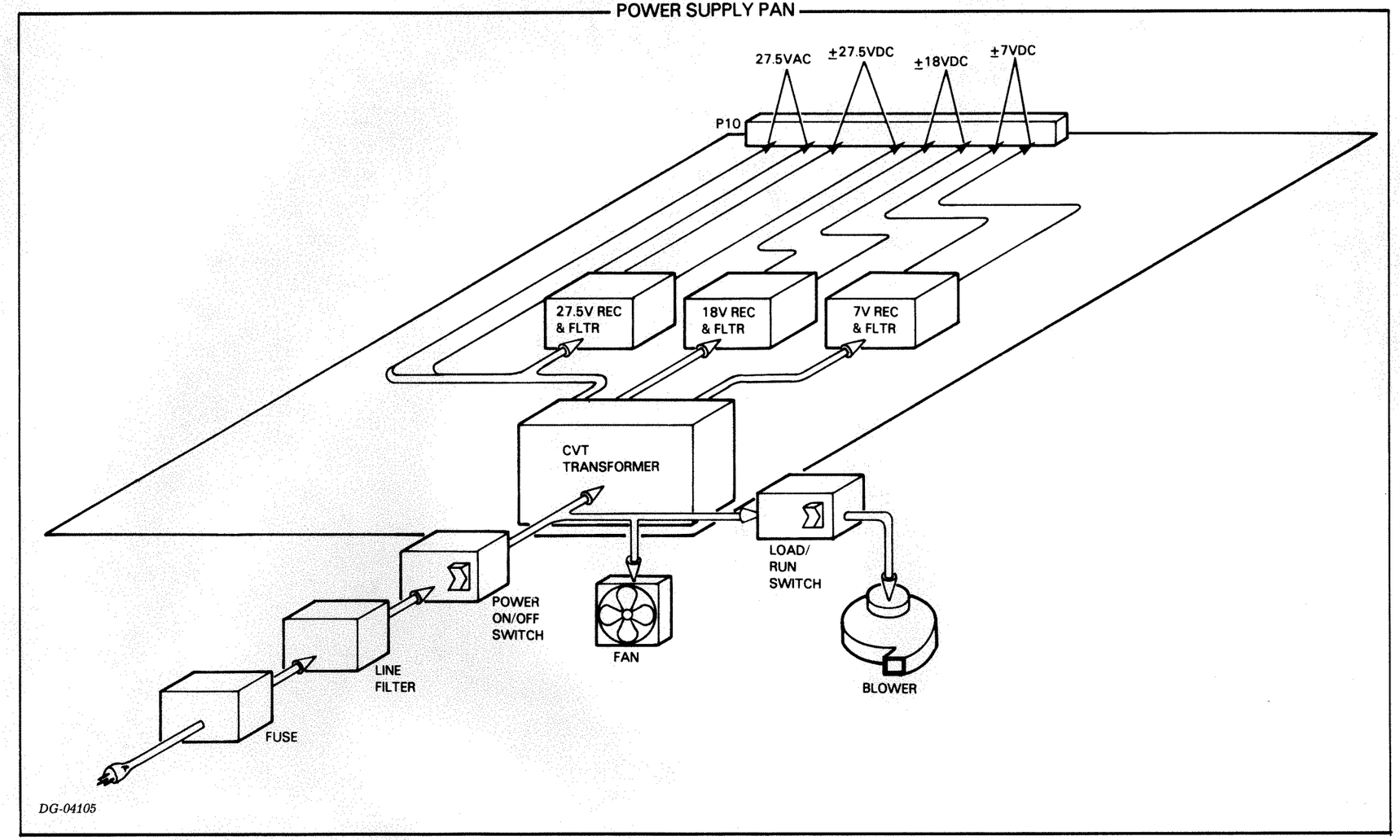
001-000870 SCHEMATIC, TERMINATOR PCB
001-000871 SCHEMATIC, READ/WRITE AMP PCB
001-000872 SCHEMATIC, SERVO & POWER SUPPLY MONITOR PCB
001-000873 SCHEMATIC, LOGIC CONTROL PCB
001-000874 SCHEMATIC, DISC CABLE INTERFACE PCB
001-000875 SCHEMATIC, SPINDLE DRIVE POWER SUPPLY PCB
001-000906 SCHEMATIC, PAN POWER SUPPLY
001-000978 SCHEMATIC, TEMPERATURE COMPENSATOR BOARD
001-000258 SCHEMATIC, DISC CARTRIDGE CONTROL

ILLUSTRATED PARTS LISTS

016-000260 IPL, READ/WRITE PCB
016-000265 IPL, SERVO & SERVO POWER SUPPLY MONITOR PCB
016-000266 IPL, LOGIC CONTROL PCB
016-000259 IPL, DISC CABLE INTERFACE PCB
016-000267 IPL, SPINDLE DRIVE POWER SUPPLY PCB
016-000297 IPL, TEMPERATURE COMPENSATOR BOARD
000-000000 IPL, DISC CARTRIDGE CONTROL

CABLE SPECIFICATIONS

008-000835 RIBBON CABLE WIRING LIST
008-000836 RIBBON CABLE READ/WRITE WIRING LIST
008-000837 CABLE POWER SUPPLY GND WIRING LIST
008-000838 SOLENOID CABLE ASSEMBLY WIRING LIST
008-000840 CABLE POWER SUPPLY MAIN WIRING LIST
008-000841 PREP TRANSFORMER 60HZ
008-000843 HARNESS SERVO 100TPI CART DISC WIRING LIST
008-000844 CABLE CARTRIDGE SPINDLE LOGIC WIRING LIST
008-000845 CABLE BRUSH MOTOR WIRING LIST
008-000849 DC JUMPER KIT, POWER SUPPLY
008-000850 POWER CORD 50HZ WIRING LIST
008-000851 POWER CORD 60HZ WIRING LIST
008-000852 POWER SUPPLY JUMPER KIT 50/60HZ WIRING LIST
008-000853 AC JUMPER 60HZ WIRING LIST
008-000854 AC JUMPER 50HZ WIRING LIST
008-000855 AC CONTROL CABLE WIRING LIST
008-000857 CABLE SENSOR WIRING LIST
008-000871 I/O CABLE SHORT WIRING LIST
008-000889 CABLE THERMISTOR PCB WIRING LIST
008-000892 FAN CABLE WIRING LIST
008-000924 CONN TERMINATOR PCB WIRING LIST
008-000978 SPINDLE MOTOR CABLE WIRING LIST
000-000000 I/O CABLE LONG/EDGE
000-000000 I/O CABLE LONG/CANNON



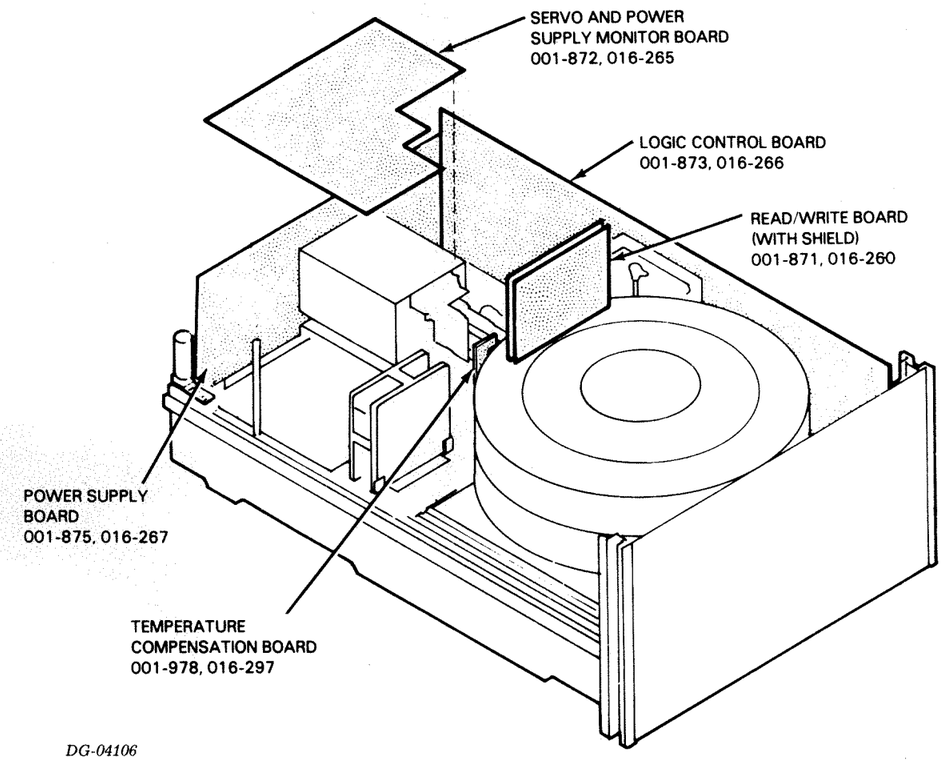
APPENDIX C
DRIVE PRINTED CIRCUIT BOARDS

This supplement describes the function of each board in the drive and includes pictorial representations that may help you isolate problems to the board level. The five boards are;

- *Logic control*
- *Servo control and power monitor*
- *Power supply and spindle drive*
- *Read/write*
- *Temperature compensation*

The pan power supply is an additional electrical subassembly, and mounts in the base of the drive. The PAN POWER SUPPLY steps down, rectifies, and filters the ac line voltage, and supplies +7, +18, +27.5 volts DC and 27.5volts AC to the disk drive. The output voltages are also regulated by the PAN due to the operating characteristics of the CVT transformer.

CIRCUIT BOARDS



DG-04106

LOGIC CONTROL

The logic board is the control center of the drive. It controls the following operations:

- *cycle up and cycle down sequences*
- *monitors the spindle speed*
- *counts sectors*
- *directs the activities of the positioner*
- *provides a velocity reference during positioner movements*
- *recovers data and a clock from the read signal*

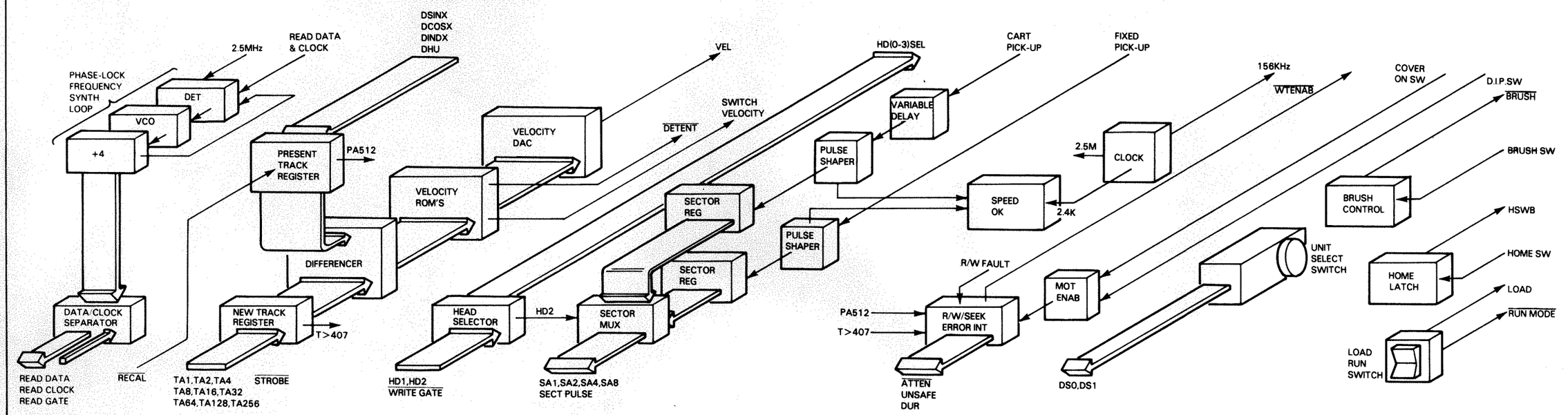
The spindle control section activates the spindle and brush drivers, controls the drawer lock, and monitors the sector pickup transducers. The sector pulses clock the spindle speed monitor and the sector counters.

The servo control section receives commands from the controller, the console, and fault detectors in the drive itself. It provides a velocity reference to control load, unload, seek and recalibrate operations. Track address registers store the current address and the destination address. An adder calculates the difference and maps through read only memories to control the velocity profile. An on track monitor provides a settling delay following a positioner movement and indicates that the drive is ready to support data transfers. An additional monitor watches for positioner movements across the data zone boundaries and controls load, unload and recalibrate operations.

The read/write control section decodes the head address and includes a phase locked loop and data separator to recover data and clock pulses from the read signal.

Miscellaneous circuits monitor the condition of the drive and include the seek timer, seek error detector, and positioner overspeed detector.

LOGIC CONTROL BLOCK DIAGRAM

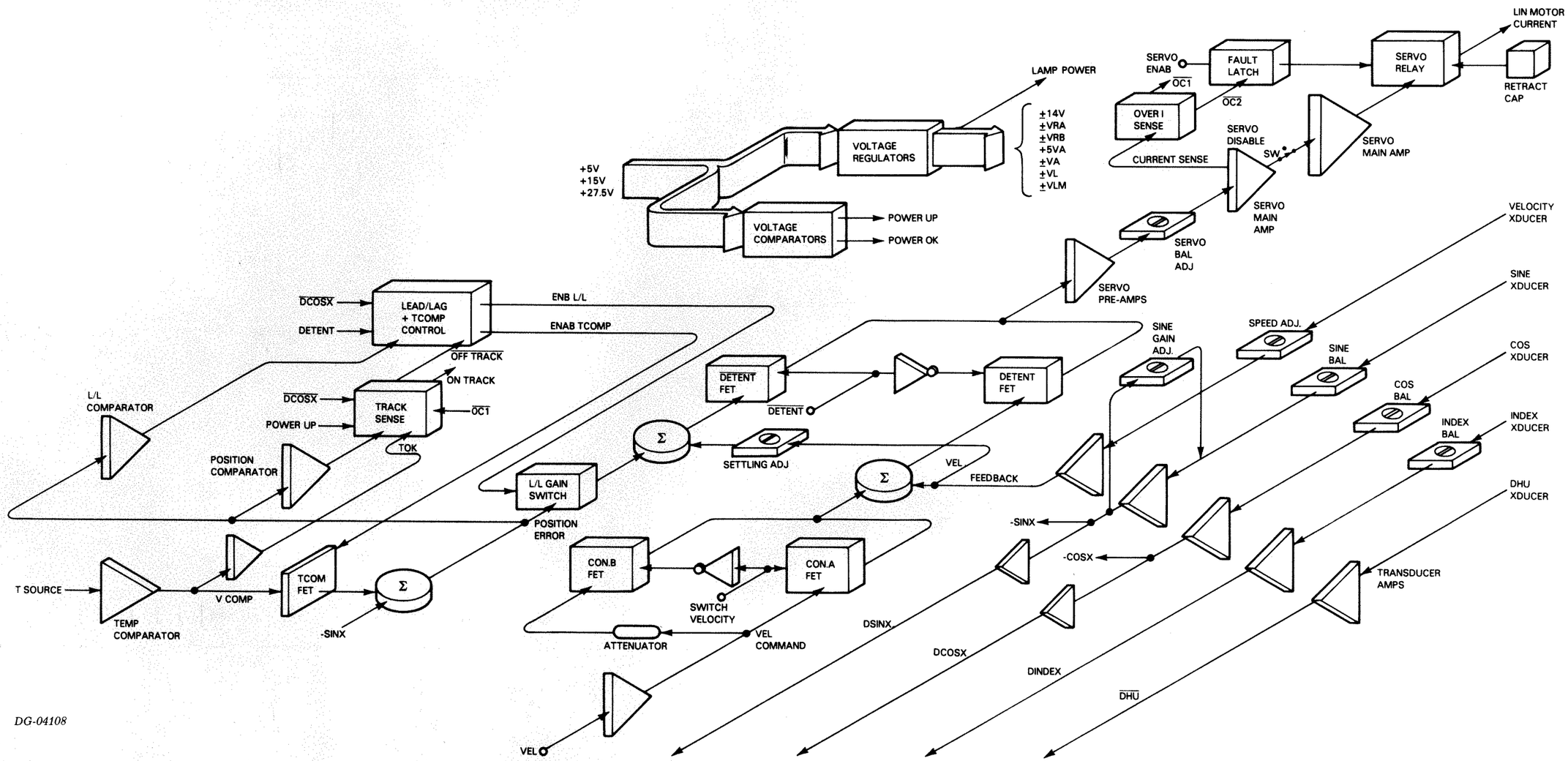


DG-04109

SERVO CONTROL AND POWER MONITOR

This board contains all the analog circuits that control and monitor the positioner. It also includes the monitors for the main dc supply voltages, and additional regulators to power the servo circuits and the lamp in the position sensor. The servo circuits include the velocity and position sensors, the velocity and position feedback loops, and the power amplifier that drives the linear motor. Position monitors indicate that the heads are on track, and enable lead lag amplification and temperature compensation. Motor current monitors detect overcurrents serious enough to require seek delays or an emergency retract. The emergency retract system unloads the heads if a failure or power outage occurs.

SERVO CONTROL AND POWER MONITOR



DG-04108

POWER SUPPLY AND SPINDLE DRIVE

This board contains the spindle drive circuits, and voltage regulators for the main dc supply. The regulators provide ± 5 V and ± 15 V for the drive electronics. They receive bulk power from the power supply pan, which hinges down below the base of the drive for service access. (Note that the pan is also a removable module.)

The spindle circuits divide a precision clock and provide two phase drive current for the spindle motor. Control logic reverses the phases to provide dynamic braking, switches to direct current drive to stop rotation, and momentarily disconnects the motor if an overcurrent occurs. The board also contains the brush motor and drawer lock solenoid drive circuits.

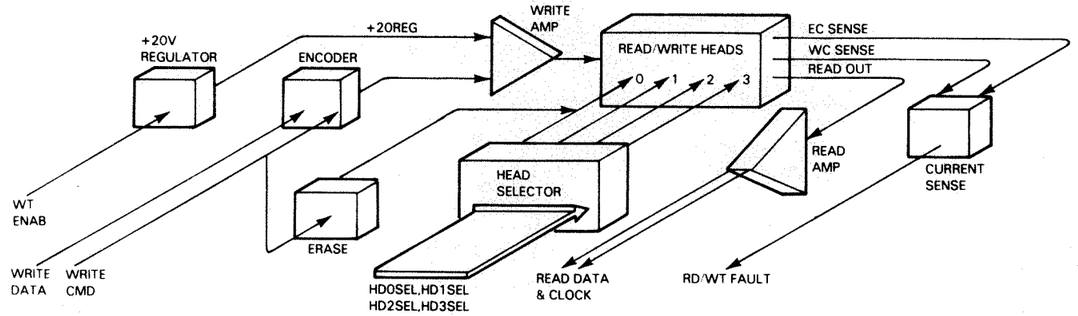
READ/WRITE

The read/write board contains all the analog read/write circuits including the head selector, write driver, read preamplifier and peak detector, and fault detection logic.

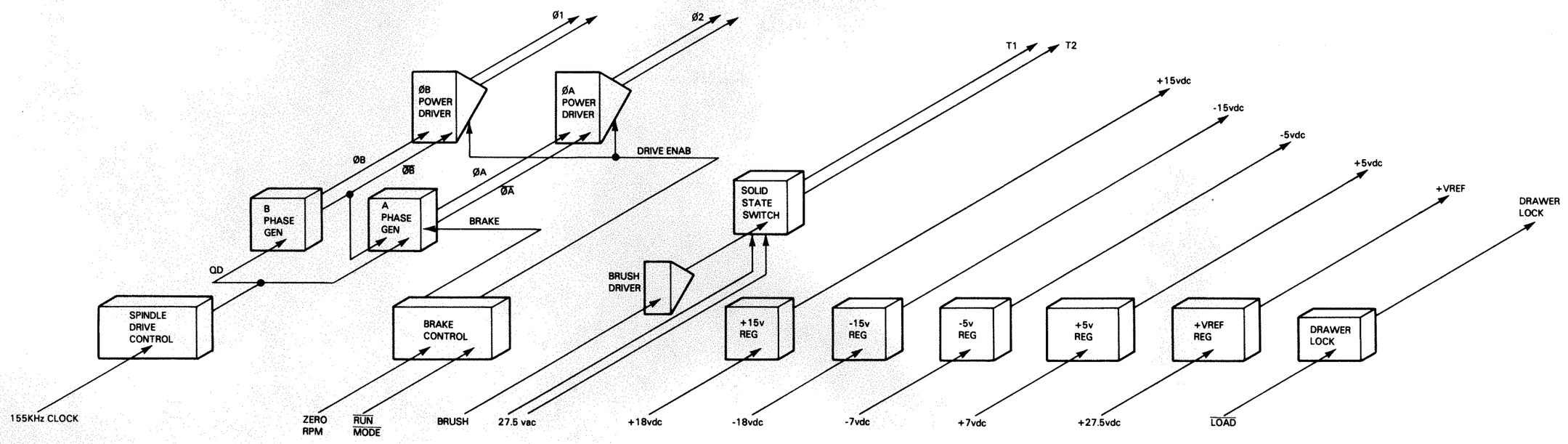
TEMPERATURE COMPENSATION

The temperature compensation board contains the temperature sensing thermistors and precision resistors for the temperature compensation circuits.

READ/WRITE BLOCK DIAGRAM

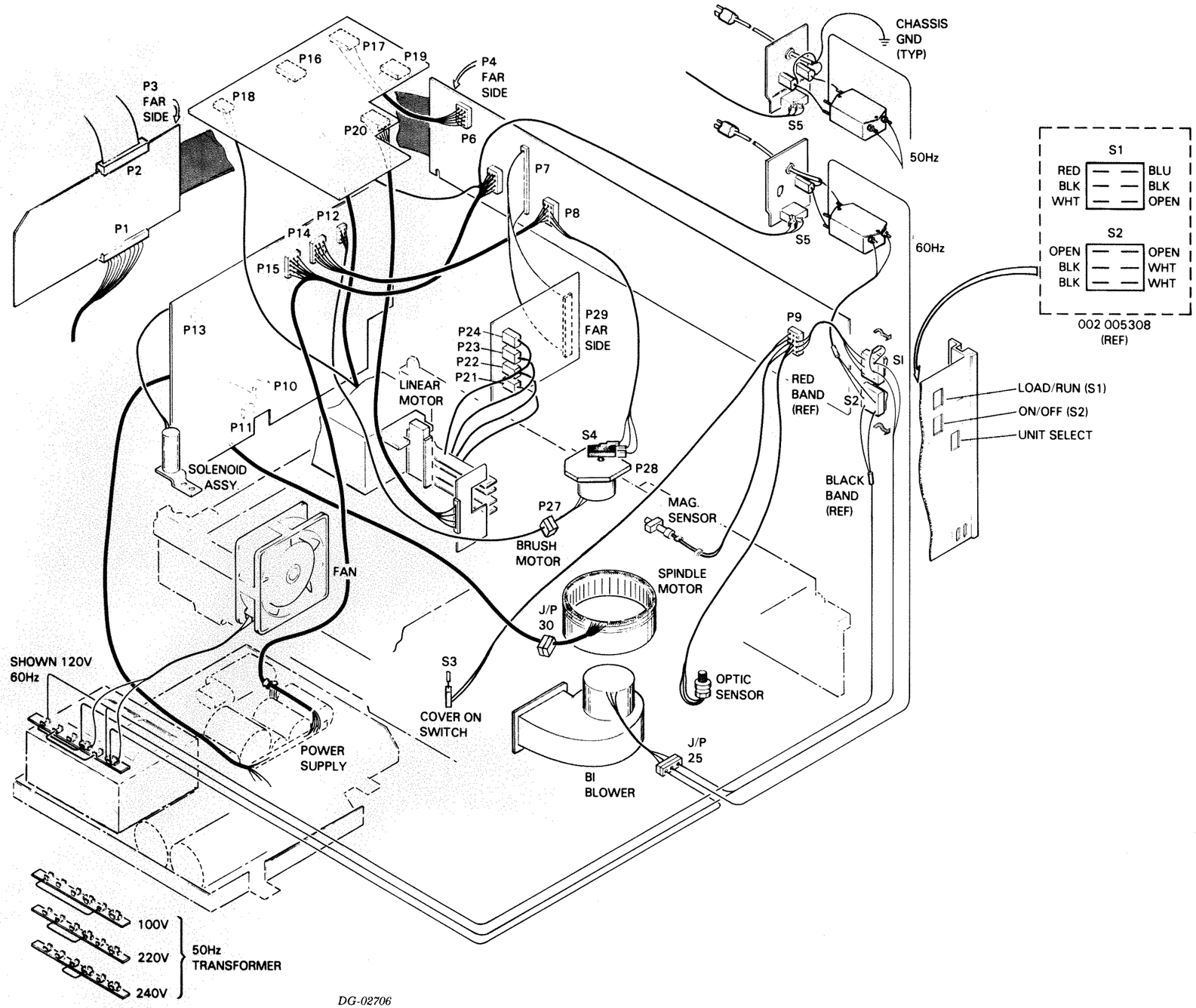


POWER SUPPLY AND SPINDLE DRIVE



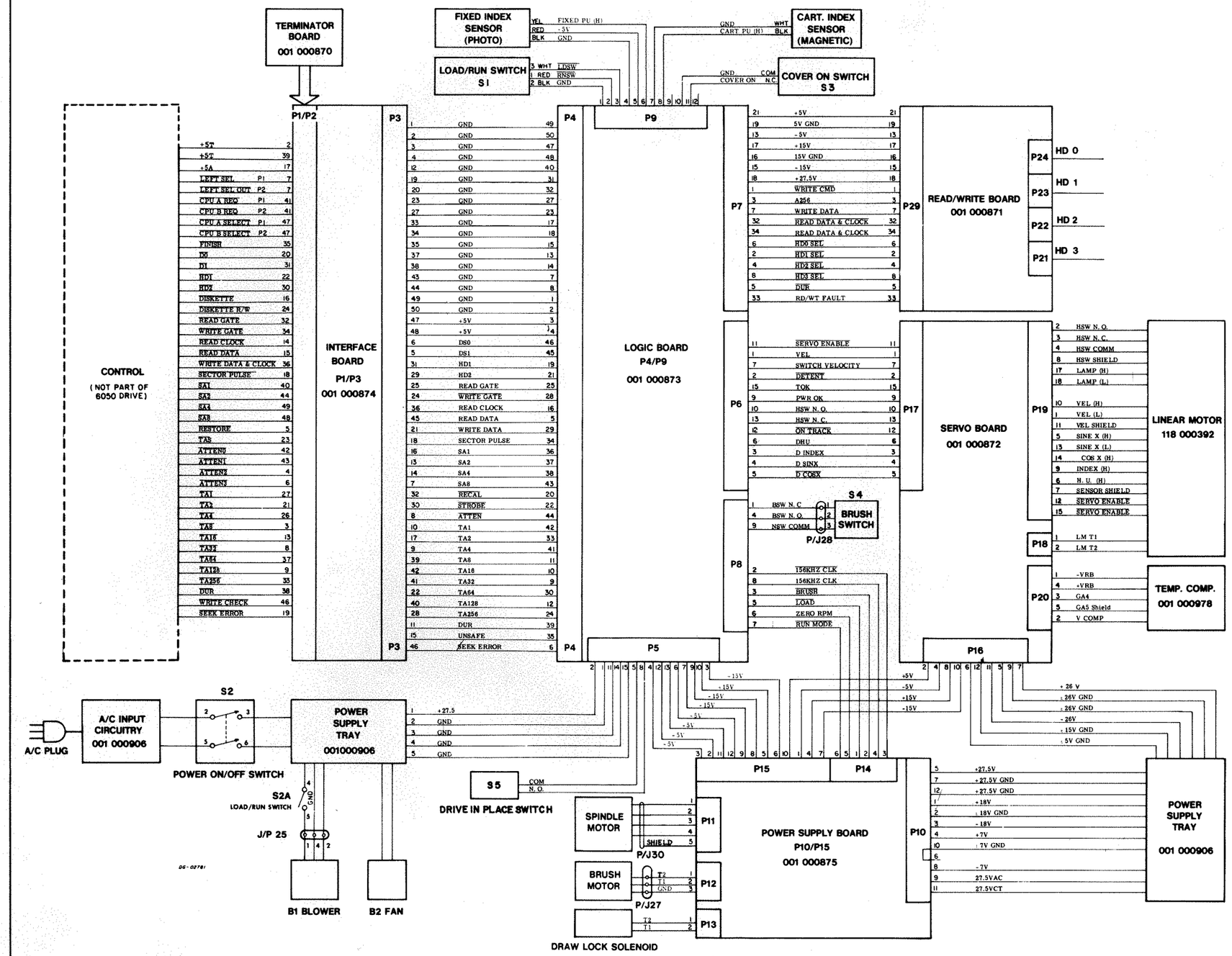
APPENDIX D
INTERNAL CABLES

DRIVE INTERNAL CABLING



DG-02706

DRIVE PCB INTERCONNECTION



APPENDIX E
FAULT FLAGS

FAULT		DESCRIPTION	CLEARED BY	• EMERGENCY RETRACT • STOP DATA TRANSFER
SET	SUBSET			
DRIVE FAULTS				
UNSAFE	TEMPERATURE NOT OK	THE TEMPERATURE DIFFERENCE BETWEEN THE DRIVE AND CARTRIDGE IS OUTSIDE THE COMPENSATION RANGE	WAITING FOR STABILIZATION	
	SPEED NOT OK	THE SPINDLE SPEED IS >3060 RPM OR <2040 RPM OR A CARTRIDGE IS NOT IN PLACE	WAITING FOR SPEED UP OR INSTALLING CARTRIDGE	
	READ/WRITE FAULT	MULTIPLE HEADS SELECTED, OR WRITE COMMAND/NO CURRENT, OR WRITE OR ERASE CURRENT/NO COMMAND	REPAIRING DRIVE	
SEEK ERROR	TRACK ADDRESS >407	A SEEK COMMAND ISSUED A TRACK ADDRESS >407	ISSUING A RECAL COMMAND OR ISSUING A SEEK COMMAND OR POWERING THE DRIVE DOWN	
	SEEK TIMEOUT	THE DRIVE DID NOT COMPLETE A SEEK OPERATION WITHIN 267 MSEC.		
	TRACK ADDRESS >511 OR <0	A COUNT ERROR OR AUTOMATIC RECALIBRATE (SEEK OVERTRAVEL) OCCURRED		
SERVO DISABLE	DISK UNDERSPEED	THE DISC SPEED FELL BELOW 2000 RPM WHILE THE HEADS WERE LOADED	COMPLETION OF RETRACT	
	SERVO OVERSPEED	THE POSITIONER VELOCITY EXCEEDED 78 IPS	POWERING THE DRIVE DOWN	•
	POWER NOT OK	5 VOLTS FELL BELOW 4.6V, 15 VOLTS FELL BELOW 13.7V, 27.5 VOLTS FELL BELOW 23.5, OR POWERING UP	REPAIR OR RESTORATION OF LINE VOLTAGE	
OVERCURRENT 1		MILD LINEAR MOTOR OVERCURRENT. EXTENDS SEEKS BY 100 MSEC. FOR 10 SEC.	MOTOR COOLDOWN	
OVERCURRENT 2		SEVERE LINEAR MOTOR OVERCURRENT	POWERING THE DRIVE DOWN	•
INTERFACE FAULTS				
3 SECONDS		THE CONTROLLER DID NOT FINISH A DATA TRANSFER WITHIN 3 SEC OF DRIVE SELECTION OR SEEK COMMAND		•
CONTROLLER FAULTS				
ERROR	UNSAFE (WRITE CHECK)	SEE DRIVE FAULTS	START/CLEAR/IOPULSE/IORESET/DOA · DATA 0 (DOES NOT CLEAR FAULT IN DRIVE)	•
	SEEK ERROR	SEE DRIVE FAULTS	SEE DRIVE FAULTS	
	ADDRESS ERROR	THE ADDRESS READ FROM THE DISC DISAGREED WITH THE ADDRESS STORED BY THE CONTROLLER	START/CLEAR/IOPULSE/IORESET/DOA · DATA 0	•
	CHECKWORD	THE CHECKWORD ACCUMULATED DURING A READ OPERATION DISAGREED WITH THE RECORDED CHECKWORD	START/CLEAR/IOPULSE/IORESET/DOA · DATA 0	•
	DATA LATE	SHIFTER AND BUFFER FULL DURING A READ OR SHIFTER AND BUFFER EMPTY DURING A WRITE	START/CLEAR/IOPULSE/IORESET	
	END OF CYLINDER	THE SURFACE ADDRESS WAS INCREMENTED BEYOND 3 DURING A MULTI-SECTOR TRANSFER	START/CLEAR/IOPULSE/IORESET/DOA · DATA 0	•

DG-04273

APPENDIX F
CYCLIC REDUNDANCY CHECK GENERATOR

The following example may help you to understand the CRC generator. We'll pick a simple polynomial to demonstrate the principle.

GENERATOR POLYNOMIAL = X4 + X1 + X0 = 10011 (FIFTH ORDER)
DATA = X4 + X3 + X0 = 11001 (FIFTH ORDER)
DATA * X5 = X9 + X8 + X5 = 1101100000 (TENTH ORDER)

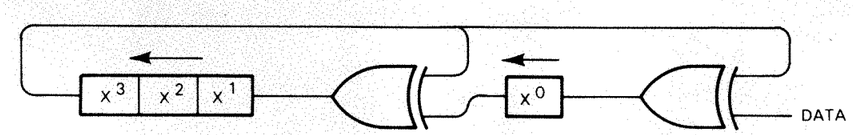
We will now divide the premultiplied data by the generator polynomial using modulo two (add with no carry, i.e. exclusive-or) arithmetic.

```
          110111
10011 ) 1100100000
        10011
        10100
        10011
        01110      __ most significant bit of partial remainder
        00000         is 0, so shift the remainder unaltered
         11100     __ most significant bit of partial remainder
         10011        is 1, so shift the remainder and invert the
         11110        bits that correspond to 1's in the
         10011        polynomial (i.e. exclusive-or the remainder
         11010        with the polynomial)
         10011
          1001     __ remainder (order 4)
```

The method for calculating the checkword becomes obvious when we examine the steps laid out in the example above. We need a four-bit shift register to store the partial remainder, with exclusive or gates at the inputs to the first and second stages. Feedback from the output of the shift register programs the exclusive or gates to invert when the most significant bit of the partial remainder is a 1. The content of the register after 10 shifts will be:

	X3	X2	X1	X0	
1 -	1	0	0	0	
2 -	1	1	0	0	
3 -	0	1	1	0	
4 -	0	0	1	1	
5 -	0	1	0	1	
6 -	1	1	1	0	
7 -	0	1	1	1	
8 -	1	1	1	1	
9 -	1	0	1	1	
10 -	1	0	0	1	__ FINAL REMAINDER

CRC GENERATOR EXAMPLE



POLYNOMIAL $X^4 + X^1 + X^0 = X^4 + X + 1$

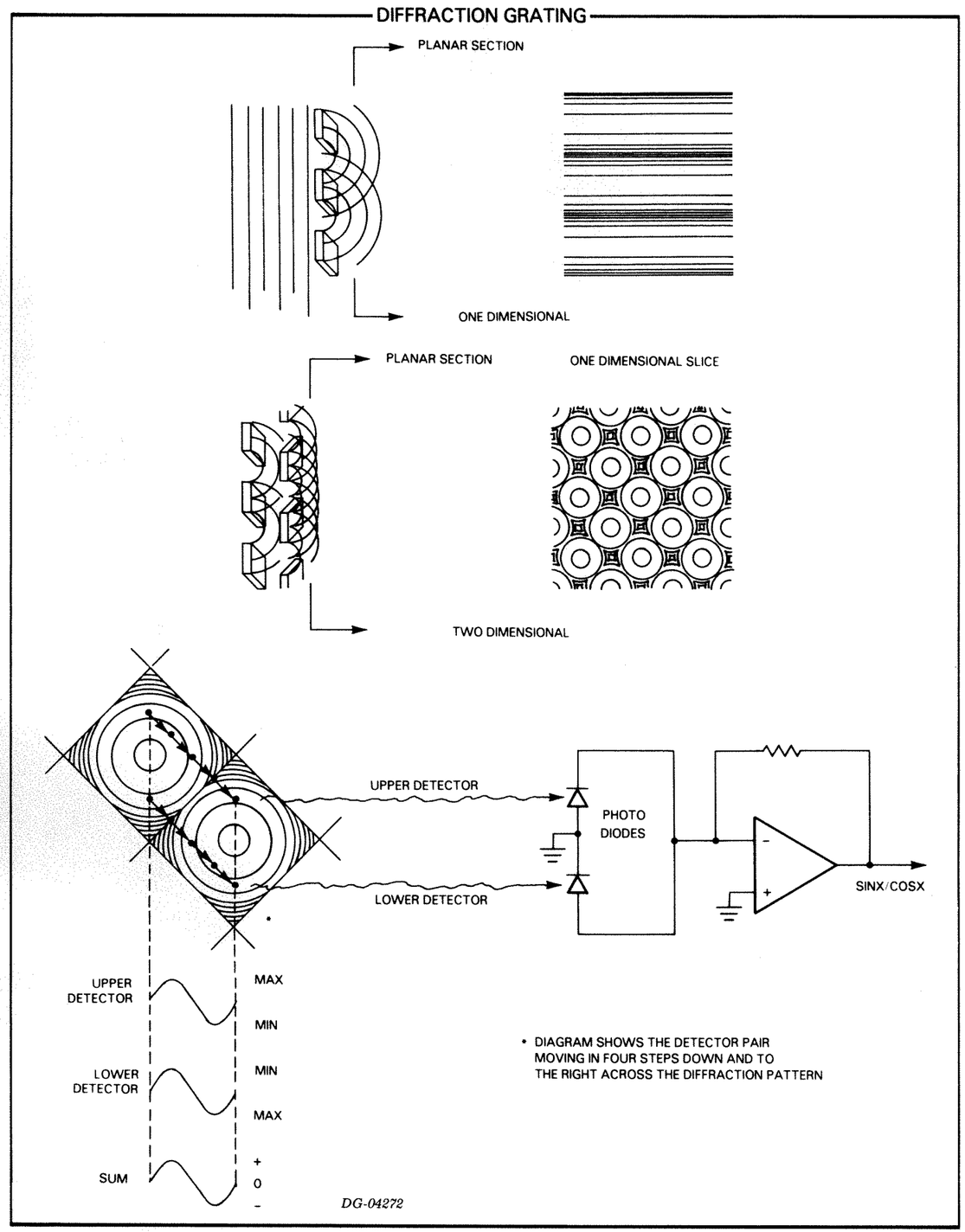
DG-04049

APPENDIX G
DIFFRACTION GRATING

The optical position sensor uses a two dimensional diffraction grating to diffract light from a precision lamp. The two dimensional grating consists of two single gratings that are closely spaced and set at angles to each other. One grating moves with the positioner, and the other is fixed on the optical pickup. As the positioner moves, the gratings combine to form a light pattern with varying intensity that moves in front of sets of photo detectors. Amplifiers recover the signal and produce a sinusoidal waveform that has one cycle per track.

The figure to the right graphically depicts the diffraction phenomenion and shows a typical position detection circuit. To understand how diffraction works, we will first examine a one dimensional grating. Think of a diffraction grating as an array of slits, somewhat liike a pickett fence. The width and spacing of the slits must be of the same order as the wavelength of the light. The grating breaks up light waves such that the light passing through appears as a series point sources that radiate concentric waves. The waves interact such that they superimpose at some points, and cancel at others. This produces alternating areas of light and dark when the pattern is observed in a planar section.

A two dimensional grating produces a vertical diffraction pattern superimposed on a horizontal pattern. The pattern moves vertically as one grating moves horizontally. Photo diodes located as shown in the drawing sense the intensity variations as the pattern moves, and combine to provide a sinusoidal signal (for simplicity, the drawing shows the photo diodes moving across a stationary pattern.)



CUT ALONG DOTTED LINE

DataGeneral

Engineering Publications Comment Form

Please help us improve our future publications by answering the questions below. Use the space provided for your comments.

Title: _____

Document No. _____

Yes	No			
☐	☐	Is this manual easy to read?	○ You (can, cannot) find things easily. ○ Language (is, is not) appropriate. ○ Technical terms (are, are not) defined as needed.	○ Other:
		In what ways do you find this manual useful?	○ Learning to use the equipment ○ As a reference ○ As an introduction to the product	○ To instruct a class. ○ Other:
☐	☐	Do the illustrations help you?	○ Visuals (are,are not) well designed. ○ Labels and captions (are,are not) clear. ○ Other:	
☐	☐	Does the manual tell you all you need to know? What additional information would you like?		
☐	☐	Is the information accurate? (If not please specify with page number and paragraph.)		

Name: _____ Title: _____

Company: _____ Division: _____

Address: _____ City: _____

State: _____ Zip: _____ Telephone: _____ Date: _____

DG-06895

DataGeneral
Data General Corporation, Westboro, Massachusetts 01580