DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-001059-00

PROGRAM

MICRONOVA ANALOG CONVERSION
SYSTEM EXERCISER

TEXT TAPE

097-001059-00

ABSTRACT

THIS IS THE SYSTEM EXERCISER FOR THE 4223 A/D CONVERTER AND 4224 D/A CONVERTER INTERFACE SUB-SYSTEMS FOR MICRONOVA COMPUTERS. IT CONTAINS TWO INDIVIDUAL PROGRAMS; A MULTIPLEXER ANALOG INPUT TEST (A/D ONLY) AND A D/A TO A/D LOOP AROUND TEST (A/D & D/A). THESE PROGRAMS TEST BOTH ANALOG AND DIGITAL SECTIONS OF THE INTERFACES FOR PROPER FUNCTIONING, AND REQUIRE A MODEL 1125A ANALOG VOLTAGE TEST ADAPTER.

```
 0001 .MAIN    MACRO REV 06.30          09:53:08 05/05/79
01
02
03
04              ;*****************************************************************
05              ;
06              ; NAME: MNACSE.TX                PART NUMBER: 097-001059
07              ;
08              ;
09              ; DESCRIPTION: MICRO NOVA ANALOG CONVERSION SYSTEM EXERCISER
10              ;
11              ;
12              ; REVISION HISTORY:
13              ;
14              ;       REV.            DATE
15              ;
16              ;       00              01/05/79
17              ;
18              ;
19              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1979
20              ; ALL RIGHTS RESERVED.
21              ;*****************************************************************
```

```
10002 .MAIN
01              ;1.     PROGRAM NAME:
02              ;       ------------
03              ;       MNACSE   -   MICRO NOVA ANALOG CONVERSION SYSTEM
04              ;                                EXERCISER
05              ;
06              ;2.     REVISION HISTORY:
07              ;       ----------------
08              ;       REV 00   -   01/05/79   FIRST RELEASE
09              ;
10              ;3.     MACHINE REQUIREMENTS:
11              ;       --------------------
12              ;       1.  MICRO NOVA CENTRAL PROCESSOR WITH AT LEAST
13              ;           8K READ/WRITE (RAM) MEMORY
14              ;           (16K IF USING CATS/KITTEN DCH EXERCISER)
15              ;       2.  MICRO NOVA ASYNCHRONOUS INTERFACE
16              ;       3.  TELETYPE OR CRT TERMINAL
17              ;       4.  PAPER TAPE READER AND/OR DISKETTE DRIVE
18              ;
19              ;4.     TEST REQUIREMENTS:
20              ;       -----------------
21              ;       FOR "MUX ANALOG INPUT" AND "LOOP AROUND" TESTS:
22              ;       1.  MICRO NOVA ANALOG TO DIGITAL INTERFACE MODEL 4223
23              ;       2.  MICRO NOVA ANALOG TO DIGITAL INTERFACE DIAGNOSTIC
24              ;           SHOULD BE RUN FIRST TO DETECT AND CORRECT ANY
25              ;           LOGIC LEVEL FAULTS ON THE A/D INTERFACE.
26              ;           - PROGRAM NAME IS "MNADC"
27              ;             AB TAPE PART # 095 - 000539
28              ;             LISTING PART # 096 - 000539
29              ;       3.  VOLTAGE ANALOG TEST ADAPTER MODEL 1125A.
30              ;       4.  CABLE: 1125A ADAPTER TO 4223 A/D CONVERTER
31              ;                  PART # 005 - 12431; WIRE LIST 008 - 2184.
32              ;
33              ;       FOR "D/A TO A/D LOOP AROUND" TEST ONLY:
34              ;       5.  MICRO NOVA DIGITAL TO ANALOG INTERFACE MODEL 4224
35              ;       6.  MICRO NOVA DIGITAL TO ANALOG INTERFACE DIAGNOSTIC
36              ;           SHOULD BE RUN FIRST TO DETECT AND CORRECT ANY
37              ;           LOGIC LEVEL FAULTS ON THE D/A INTERFACE.
38              ;           - PROGRAM NAME IS "MNDAC"
39              ;             AB TAPE PART # 095 - 000540
40              ;             LISTING PART # 096 - 000540
41              ;       7.  CABLE: 4224 D/A CONVERTER TO 1125A ADAPTER
42              ;                  PART # 005 - 12425; WIRE LIST 008 - 2185.
43              ;       8.  ONE OF THE FOLLOWING D/A INTERFACE JUMPERS MUST
44              ;           BE INSERTED TO ALLOW Z-AXIS PULSE TRIGGERING:
45              ;           - CLOCK X (JUMPER W22) OR
46              ;             CLOCK Y (JUMPER W21)
47              ;       9.  W33 MUST BE INSERTED FOR Z-AXIS DC COUPLING.
48              ;
49              ;       AN EXTERNAL DC VOLTAGE SOURCE IS ALSO NEEDED FOR THE
50              ;       MUX ANALOG INPUT TEST (+/- 10 VDC MAXIMUM). SEE TEST
51              ;       DESCRIPTION IN SECTION 7.2.1 FOR MORE INFORMATION.
```

```
10003 .MAIN
01              ;       IN ADDITION, THE A/D CONVERTER AND THE D/A CONVERTER
02              ;       (LOOP AROUND ONLY) MUST BE PROPERLY CALIBRATED TO
03              ;       INSURE DATA VALIDITY BEFORE RUNNING THIS EXERCISER.
04              ;       THIS CAN BE ACCOMPLISHED USING THE FOLLOWING PROGRAMS
05              ;       AND CALIBRATION EQUIPMENT:
06              ;
07              ;       10. MICRO NOVA ANALOG TO DIGITAL INTERFACE EXERCISER
08              ;           - PROGRAM NAME IS "MNADE"
09              ;             AB TAPE PART # 095 - 000637
10              ;             LISTING PART # 096 - 000637
11              ;       11. MICRO NOVA DIGITAL TO ANALOG INTERFACE EXERCISER
12              ;           - PROGRAM NAME IS "MNDAE"
13              ;             AB TAPE PART # 095 - 000638
14              ;             LISTING PART # 096 - 000638
15              ;       12. FOR ACCURATE CONVERTER CALIBRATION, A PRECISION
16              ;           VOLTAGE SOURCE AND A 3 1/2 - 4 1/2 DIGIT DIGITAL
17              ;           MULTIMETER (OR VOLTMETER) WILL BE NECESSARY.
18              ;       13. IF YOU ARE RUNNING THIS PROGRAM WITH THE "KITTEN"
19              ;           DATA CHANNEL EXERCISER, A MICRO NOVA I/O TESTER
20              ;           BOARD IS REQUIRED TO BE IN THE MICRO NOVA CHASSIS.
21              ;           THE BOARDS MUST HAVE THE PROPER DATA CHANNEL PRIOR-
22              ;           ITY IN THE MICRO NOVA CHASSIS. THE A/D CONVERTER,
23              ;           D/A CONVERTER (IF LOOP AROUND) AND I/O TESTER BOARD
24              ;           SHOULD BE PLACED IN CONTIGUOUS I/O SLOTS AVALIABLE
25              ;           AFTER THE ASYNCRONOUS INTERFACE BOARD. NOTE THAT ANY
26              ;           SKIPPED I/O SLOT WILL BREAK BOTH /INTR/ AND /DCHP/
27              ;           I/O LINES. THESE SHOULD BE JUMPERED IN THIS CASE.
28              ;
29              ;           THE I/O BUS (B SIDE) PRIORITY PIN #'S ARE:
30              ;           INTP IN:  B20
31              ;           INTP OUT: B19
32              ;           DCHP IN:  B22
33              ;           DCHP OUT: B21
34              ;
35              ;5.     SUMMARY:
36              ;       --------
37              ;       THIS IS A SYSTEM EXERCISER FOR THE 4223 A/D CONVERTER
38              ;       AND 4224 D/A CONVERTER INTERFACE SUB-SYSTEMS FOR MICRO-
39              ;       NOVA COMPUTERS. IT CONTAINS TWO INDIVIDUAL PROGRAMS;
40              ;       A MULTIPLEXER ANALOG INPUT TEST (A/D ONLY) AND A
41              ;       D/A TO A/D LOOP AROUND TEST (A/D & D/A). THESE PROGRAMS
42              ;       TEST BOTH ANALOG AND DIGITAL SECTIONS OF THE INTERFACES
43              ;       FOR PROPER FUNCTIONING, AND REQUIRE A MODEL 1125A ANALOG
44              ;       VOLTAGE TEST ADAPTER.
```

```
10004 .MAIN
01              ;6.     RESTRICTIONS:
02              ;       -------------
03              ;       1) INSERTION OF, AND CONNECTIONS TO ANY BOARD SHOULD
04              ;          ALWAYS BE DONE WITH POWER OFF.
05              ;       2) THE A/D (AND D/A FOR LOOP TEST) MUST BE CAILIBRATED
06              ;          (SEE SECTION 4 ABOVE).
07              ;       3) ONE A/D CONVERTER (MUX ANALOG INPUT TEST) OR ONE
08              ;          A/D - D/A PAIR (LOOP AROUND TEST) MAY BE TESTED AT
09              ;          A TIME.
10              ;       4) FOR THE LOOP AROUND TEST, THE TEST CONFIGURATION IS
11              ;          SUCH THAT NO MUX CHANNEL INTERACTION CAN BE DETECTED
12              ;          BETWEEN CHANNELS 7 AND 8. ALSO, THE LOOP AROUND TEST
13              ;          PEFORMS WITH "SINGLE-ENDED" MUX MODE SELECTED ONLY.
14              ;       5) THE FOLLOWING A/D HANDSHAKING AND TEST SIGNALS ARE
15              ;          NOT TESTED: ADC READY, ADC CR PLT TEST, ADC CLOCK,
16              ;          ADC SERIAL DATA. (ALL ARE OUTPUT ONLY).
17              ;       6) THE FOLLOWING D/A HANDSHAKING SIGNALS ARE NOT TEST-
18              ;          ED: ERASE, EXTERNAL ERASE INPUT, WRITE-THROUGH,
19              ;          NON-STORE (SCOPE CONTROL SIGNALS), DAC DATA READY,
20              ;          DAC DATA VALID, BRTXMSB, BRTXLSB, BRTYMSB, BRTYLSB.
21              ;          IN ADDITION, THE DC BASE LEVEL VOLTAGE OF "Z-AXIS"
22              ;          CAN BE ANYWHERE IN ITS NOMINAL ADJUSTMENT RANGE
23              ;          (+/- 5 VDC). IT IS USED ONLY TO TEST MUX CHANNEL
24              ;          INDEPENDENCE ON THE A/D INTERFACE. THE PROGRAM
25              ;          DOES NOT EXPECT ANY SPECIFIED VALUE FROM IT. IT
26              ;          WILL, HOWEVER, REPORT AN ERROR IF THE Z-AXIS LEVEL
27              ;          IS INCONSISTENT.
28              ;       7) ALTHOUGH THE ANALOG FUNCTIONS ARE TESTED FOR BASIC
29              ;          OPERATION IN THIS EXERCISER, IT IS NOT AN ANALOG
30              ;          ACCURACY TEST.
31              ;       8) THIS PROGRAM WILL NOT RUN IN CONJUNCTION WITH "CATS",
32              ;          WHICH IS A DISK BASED DATA CHANNEL EXERCISER PROGRAM.
33              ;          IF ATTEMPTED, "I/O ADDR ERRORS" WILL BE REPORTED BY
34              ;          THE "CATS" DCH EXERICSER PROGRAM. IT WILL, HOWEVER,
35              ;          RUN IN CONJUNCTION WITH "KITTEN", WHICH IS A DATA
36              ;          CHANNEL EXERCISER THAT USES A SPECIAL I/O TESTER
37              ;          BOARD (SEE SECTION 4 - TEST REQUIREMENTS).
```

```
10005 .MAIN
01              ;7.     PROGRAM DESCRIPTION/THEORY OF OPERATION:
02              ;       ---------------------------------------
03              ;NOTE: THE FOLLOWING CONVENTION IS USED IN THE
04              ;       DESCRIPTION TO INDICATE LOW ACTIVE SIGNALS:
05              ;
06              ;                       ----------
07              ;         /SIGNALNAME/ = SIGNALNAME
08              ;
09              ;7.1.1  4223 ANALOG TO DIGITAL CONVERTER OPERATION:
10              ;
11              ;THE A/D BOARD FOR THE MICRONOVA CONSISTS OF A TWO HYBRID
12              ;PACKAGE DATA ACQUISITION SYSTEM (DAS) ALONG WITH INTERFACE
13              ;AND LOGIC CIRCUITRY.  AN ON-BOARD DC-DC CONVERTER
14              ;PROVIDES +/- 15 VOLTS REQUIRED BY THE ANALOG CIRCUITRY.
15              ;ONE HYBRID PACKAGE OF THE DAS CONSISTS OF TWO EIGHT-TO-ONE
16              ;ANALOG MULTIPLEXERS, ANALOG SWITCH TO SELECT SINGLE ENDED
17              ;OR DIFFERENTIAL CHANNELS, INSTRUMENTATION AMPLIFIER, AND
18              ;SAMPLE AND HOLD.  THE OTHER PACKAGE CONTAINS A 12-BIT A/D
19              ;CONVERTER WITH INTERNAL CLOCK.  THE DAS CAN BE USED EITHER
20              ;WITH 16. SINGLE-ENDED OR, FOR HIGHER COMMON-MODE REJECTION
21              ;RATIO, WITH 8. DIFFERENTIAL ANALOG INPUTS.  THE SELECTION
22              ;OF SINGLE-ENDED OR DIFFERENTIAL CHANNELS IS PROGRAM SELECT-
23              ;ABLE.  VOLTAGE RANGES, WHICH ARE JUMPER SELECTABLE, ARE 0-5,
24              ;0-10, +/- 5, +/- 10 VOLTS.  CONVERSION TIME IS 25 US MAXIMUM
25              ;WITH A THROUGHPUT RATE OF 30 KHZ.  LINEARITY AND DIFFERENTIAL
26              ;NONLINEARITY ERRORS ARE EACH TYPICALLY 1/2 LSB, CONVERSION
27              ;IS MONOTONIC, AND OVERALL RELATIVE ACCURACY AT 25 DEGREES C
28              ;IS 0.025% OF FULL SCALE READING.
29              ;
30              ;THERE ARE SEVEN DIFFERENT CLOCK SOURCES FOR STARTING A/D
31              ;CONVERSIONS.  FOR PROGRAMMED I/O THESE ARE /STRT/, NO
32              ;CLOCK SYNCHRONIZATION; /STRT/, INTERNAL CLOCK SYNC;
33              ;/STRT/, EXTERNAL CLOCK SYNC.  FOR DATA CHANNEL TRANSFERS
34              ;THESE ARE:  /IOPLS/ (ONE CONVERSION FOR EVERY /IOPLS/
35              ;COMMAND - THE TIME BETWEEN /IOPLS/ COMMANDS SHALL BE
36              ;GREATER THAN THE MAXIMUM DATA CHANNEL LATENCY OR 33 US,
37              ;WHICHEVER IS GREATER); /DCHI/, NO CLOCK SYNC (MAXIMUM
38              ;TRANSFER RATE); INTERNAL CLOCK SYNC; EXTERNAL CLOCK SYNC.
39              ;THE EXTERNAL CLOCK SHOULD HAVE A PERIOD GREATER THAN
40              ;33 US.  ALL DATA CHANNEL TRANSFER SEQUENCES BEGIN WITH
41              ;A /STRT/ COMMAND. THE CLOCK SOURCE IS SELECTED BY THREE
42              ;STATUS BITS IN A DOA INSTRUCTION.  THIS INSTRUCTION MUST
43              ;ALSO CONTAIN AN INITIAL AND FINAL MULTIPLEXER ADDRESS.
44              ;A MUX CHANNEL COUNTER FIRST ADDRESSES THE INITIAL CHANNEL
45              ;AND IS INCREMENTED ONCE FOR EVERY CONVERSION.  AFTER
46              ;THE VOLTAGE ON THE FINAL CHANNEL IS CONVERTED, THE
47              ;INITIAL CHANNEL IS AGAIN ADDRESSED.  THIS SEQUENCE THEN
48              ;REPEATS ITSELF. HENCE, FOR CONVERSIONS ON ONLY ONE CHANNEL
49              ;THE FINAL AND INITIAL CHANNELS ARE SET EQUAL TO THE
50              ;DESIRED CHANNEL.
```

```
10006 .MAIN
01              ;CHANNEL NUMBERING IS AS FOLLOWS:
02              ;
03              ;CHANNEL ADDRESS  ------- CHANNEL SELECTED ----------
04              ;   (OCTAL)       SINGLE-ENDED           DIFFERENTIAL
05              ;---------------  ------------           ------------
06              ;       0       ANA0 (A49) HI          ANA0 (A49) HI
07              ;               ANA0 SE RET (A47) LO   ANA8 (A50) LO
08              ;
09              ;       1       ANA1 (A45) HI          ANA1 (A45) HI
10              ;               ANA1 SE RET (A43) LO   ANA9 (A46) LO
11              ;
12              ;       2       ANA2 (A41) HI          ANA2 (A41) HI
13              ;               ANA2 SE RET (A39) LO   ANA10 (A42) LO
14              ;
15              ;       3       ANA3 (A37) HI          ANA3 (A37) HI
16              ;               ANA3 SE SET (A35) LO   ANA11 (A38) LO
17              ;
18              ;       4       ANA4 (A33) HI          ANA4 (A33) HI
19              ;               ANA4 SE RET (A31) LO   ANA12 (A34) LO
20              ;
21              ;       5       ANA5 (A29) HI          ANA5 (A29) HI
22              ;               ANA5 SE RET (A27) LO   ANA13 (A30) LO
23              ;
24              ;       6       ANA6 (A25) HI          ANA6 (A25) HI
25              ;               ANA6 SE RET (A23) LO   ANA14 (A26) LO
26              ;
27              ;       7       ANA7 (A21) HI          ANA7 (A21) HI
28              ;               ANA7 SE RET (A19) LO   ANA15 (A22) LO
29              ;
30              ;       10      ANA8 (A50) HI          SAME AS CHANNEL 0
31              ;               ANA8 SE RET (A48) LO
32              ;
33              ;       11      ANA9 (A46) HI          SAME AS CHANNEL 1
34              ;               ANA9 SE RET (A44) LO
35              ;
36              ;       12      ANA10 (A42) HI         SAME AS CHANNEL 2
37              ;               ANA10 SE RET (A40) LO
38              ;
39              ;       13      ANA11 (A38) HI         SAME AS CHANNEL 3
40              ;               ANA11 SE RET (A36) LO
41              ;
42              ;       14      ANA12 (A34) HI         SAME AS CHANNEL 4
43              ;               ANA12 SE RET (A32) LO
44              ;
45              ;       15      ANA13 (A30) HI         SAME AS CHANNEL 5
46              ;               ANA13 SE RET (A28) LO
47              ;
48              ;       16      ANA14 (A26) HI         SAME AS CHANNEL 6
49              ;               ANA14 SE RET (A24) LO
50              ;
51              ;       17      ANA15 (A22) HI         SAME AS CHANNEL 7
52              ;               ANA15 SE RET (A20) LO
53              ;
54              ;       CODING JUMPERS:
55              ;
56              ;       DAS 0 LO = W7
57              ;       DAS 0 HI = W6
```

```
10007 .MAIN
01              ;AN INTERESTING FEATURE OF THE CHANNEL ADDRESSING LOGIC IS
02              ;ITS ABILITY TO "WRAP AROUND" ADDRESS 17 OCTAL.  THUS, THE
03              ;FINAL CHANNEL MAY BE LESS THAN THE INITIAL CHANNEL.  FOR
04              ;EXAMPLE, IF THE INITIAL CHANNEL IS 12 OCTAL AND THE FINAL
05              ;CHANNEL IS 3 OCTAL, CONVERSIONS OCCUR FOR CHANNELS 12,13,
06              ;14,15,16,17,0,1,2,3,12,13,....  THE EIGHT DIFFERENTIAL
07              ;CHANNELS WOULD NORMALLY BE NUMBERED 0-7.  IF IT IS
08              ;DESIRED TO USE THE WRAP-AROUND FEATURE TO CONVERT DIFFERENTIAL
09              ;CHANNELS 6,7,0,1,2, HOWEVER, THE INITIAL CHANNEL MUST
10              ;BE GIVEN AS 16 OCTAL AND THE FINAL AS 2 OCTAL, SINCE THE
11              ;WRAP-AROUND OCCURS AROUND 17 OCTAL.
12
13              ;THE DOA INSTRUCTION SHOULD NOT BE GIVEN IF BUSY IS SET.
14              ;ALL STATUS BITS SET UP BY THE DOA INSTRUCTION REMAIN
15              ;THE SAME UNITL THE NEXT DOA INSTRUCTION FOR /IORST/,
16              ;WHICH CLEARS ALL STATUS BITS.
17
18              ;AN END-OF-CONVERSION SIGNAL FROM THE DAS WHEN CONVERTING
19              ;IN PROGRAMMED I/O MODE, OR A /WCEZ/ SIGNAL FROM THE
20              ;MN603 I/O CONTROLLER CHIP IN DATA CHANNEL MODE SETS
21              ;DONE AND WILL REQUEST AN INTERRUPT IF INTERRUPTS
22              ;ARE ENABLED.
23
24              ;A CLOCK OVERRUN WILL OCCUR IF AN END-OF-CONVERSION
25              ;SIGNAL (EOC) OCCURS BEFORE DATA FROM THE PREVIOUS
26              ;CONVERSION IS READ INTO THE CPU.  THIS CAUSES THE CURRENT
27              ;DATA TO BE LOST.  THE CLOCK OVERRUN SIGNAL SETS
28              ;A STATUS BIT WHICH CAN BE READ BY A DIA INSTRUCTION
29              ;AND CAN ALSO, BY SETTING A JUMPER, SET DONE.  THE DIA
30              ;INSTRUCTION ALSO READS IN THE CURRENT MUX CHANNEL, EOC
31              ;AND A BIT INDICATING AN EXTERNAL INTERRUPT REQUEST.
32              ;SUCH A REQUEST, WHICH OCCURS BY PULLING THE /EXTERNAL
33              ;INTERRUPT REQUEST/ LINE LOW, DIRECTLY REQUESTS AN
34              ;INTERRUPT WITHOUT SETTING DONE.  EOC IS LOW DURING AN
35              ;A/D CONVERSION AND OTHERWISE IS HIGH.  READING IN EOC
36              ;BY A DIA INSTRUCTION IS USEFUL IN THE IOPLS DATA CHANNEL
37              ;MODE TO INDICATE THAT NEW DATA IS READY AND THAT,
38              ;AFTER THE APPROPRIATE DATA CHANNEL LATENCY, WILL BE
39              ;READ TO THE CPU.
40
41              ;AN ADC READY SIGNAL (TRUE HIGH OR LOW, JUMPER SELECT-
42              ;ABLE) IS A HANDSHAKING SIGNAL THAT INDICATES TO THE
43              ;USER THAT THE DAS HAS FINISHED THE CURRENT CONVERSION
44              ;AND IS READY TO DO ANOTHER CONVERSION.  AS SOON AS A
45              ;NEW CONVERSION BEGINS, THIS SIGNAL CHANGES STATE UNTIL
46              ;THE NEXT END-OF-CONVERSION SIGNAL.
47
48              ;THE NOMINAL INTERNAL CLOCK RANGE (PERIOD) IS:
49              ;30 US - 500 US (ADJUSTABLE BY POTENTIOMETER R26).
50
51              ;OTHER SIGNALS ARE:
52
53              ;INTERNAL CLOCK OUTPUT = A1,     RETURN = A2
54              ;EXTERNAL CLOCK INPUT  = A3,     RETURN = A4
```

```
10008 .MAIN
01              ;       NOTE: THE FOLLOWING CONVENTION IS USED IN THE
02              ;             DESCRIPTION TO INDICATE LOW ACTIVE SIGNALS:
03
04              ;                                 ----------
05              ;                    /SIGNALNAME/ = SIGNALNAME
06
07              ;7.1.2  4224 DIGITAL TO ANALOG CONVERTER OPERATION:
08              ;       THE D/A INTERFACE FOR THE MICRO NOVA CONSISTS OF
09              ;       TWO 12-BIT HYBRID D/A CONVERTERS WITH SCOPE CONTROL,
10              ;       LOGIC AND INTERFACE CIRCUITRY. VOLTAGE RANGES FOR
11              ;       THE DACS (JUMPER SELECTABLE) ARE 0-5, 0-10,
12              ;       +/- 5, +/- 10 VOLTS DC. THE VOLTAGE RANGES OF THE TWO
13              ;       DACS ARE INDEPENDENT OF EACH OTHER. MAXIMUM SETTLING
14              ;       TIME TO 0.01% OF FULL SCALE READING IS TYPICALLY 7 US.
15              ;       LINEARITY AND DIFFERENTIAL LINEARITY ARE EACH +/-
16              ;       1/2 LSB AND CONVERSION IS MONOTONIC. EACH DAC HAS
17              ;       AN OUTPUT AMPLIFIER ENABLING IT TO DRIVE 5 MA LOADS.
18              ;       AN ON BOARD DC-DC CONVERTER PROVIDES THE +/- 15 VDC
19              ;       NECESSARY FOR THE ANALOG CIRCUITRY. CODING FOR THE
20              ;       CONVERTERS (JUMPER SELECTABLE) IS EITHER OFFSET BINARY
21              ;       OR TWO'S COMPLEMENT.
22
23              ;       A DOUBLE BUFFERING SCHEME ALLOWS SYNCHRONIZATION OF
24              ;       OUTPUT DATA TO THE D/A CONVERTERS WITH EITHER AN
25              ;       INTERNAL OR EXTERNAL CLOCK. THE FIRST BUFFER IS LOADED
26              ;       BY A DOC INSTRUCTION FOR PROGRAMMED I/O (PIO) OR
27              ;       /DCHO/ FOR DATA CHANNEL (DCH) CONVERSIONS. AT THIS
28              ;       POINT, BOTH THE DAC DATA READY STATUS BIT
29              ;       (READABLE BY A DIA INSTRUCTION) AND OUTPUT SIGNAL
30              ;       (JUMPER SELECTABLE ACTIVE HIGH OR LOW) BECOME ACTIVE.
31              ;       THEY REMAIN ACTIVE UNTIL A CLOCK SIGNAL OCCURS TO
32              ;       LOAD THE SECOND BUFFER WHICH SENDS THE DATA TO
33              ;       ONE OF THE DACS FOR CONVERSION TO ITS EQUIVALENT
34              ;       ANALOG VOLTAGE OUTPUT. APPROXIMATELY 7 US LATER,
35              ;       AFTER THE DAC HAS SETTLED TO ITS NEW VALUE, THE DAC
36              ;       DATA VALID OUTPUT SIGNAL BECOMES ACTIVE (ALSO JUMPER
37              ;       SELECTABLE ACTIVE HIGH OR LOW) AND REMAINS ACTIVE
38              ;       UNTIL THE NEXT CONVERSION IS STARTED.
39
40              ;       THERE ARE SEVEN DIFFERENT CLOCK SOURCES FOR SENDING
41              ;       DATA TO THE DACS. FOR PROGRAMMED I/O (PIO) THEY ARE:
42              ;       /STRT/ - NO CLOCK SYNCRONIZATION, INTERNAL CLOCK
43              ;       SYNCHRONIZATION, EXTERNAL CLOCK SYNCHRONIZATION.
44              ;       FOR DATA CHANNEL (DCH) TRANSFERS THEY ARE: /IOPLS/
45              ;       (ONE CONVERSION FOR EVERY /IOPLS/ ISSUED TO THE D/A),
46              ;       DATA READY (OCCURS ONE FSTROBE AFTER /DCHO/ AND
47              ;       REPRESENTS THE MAXIMUM TRANSFER RATE), INTERNAL
48              ;       CLOCK SYNCRONIZATION, EXTERNAL SYNCHRONIZATION.
49              ;       FOR /IOPLS/ DCH TRANSFERS, THE TIME BETWEEN
50              ;       SUBSEQUENT IOPLS'S SHOULD BE GREATER THAN THE
51              ;       MAXIMUM DATA CHANNEL LATENCY. ALSO, AN I/O
52              ;       INSTRUCTION WITH AN IOPLS APPENDED (I.E. NIOP)
53              ;       SHOULD NOT BE GIVEN TO THE D/A UNTIL DATA READY
54              ;       IS ACTIVE (DATA LOADED INTO FIRST BUFFER). THIS
55              ;       CAN BE CHECKED BY READING THE D/A STATUS (DIA).
```

```
10009 .MAIN
01              ;       IF AN EXTERNAL CLOCK IS USED, THE CLOCK SIGNAL
02              ;       MUST BE HIGH FOR AT LEAST 2 US AND LOW FOR AT
03              ;       LEAST 2 US AND HAVE A PERIOD GREATER THAN THE
04              ;       SETTLING TIME OF THE DACS (7 US TYPICAL),
05              ;       AND FOR DATA CHANNEL TRANSFERS, HAVE A PERIOD
06              ;       GREATER THAN THE MAXIMUM DATA CHANNEL LATENCY.
07              ;
08              ;       THE CLOCK SOURCE IS SELECTED BY THREE STATUS BITS
09              ;       IN A DOA INSTRUCTION. THE DOA INSTRUCTION ALSO
10              ;       CONTAINS AN ALTERNATE BIT, WHICH IS SET TO INDICATE
11              ;       ALTERNATING CONVERSIONS BETWEEN THE TWO DACS, A DAC
12              ;       SELECT BIT TO SELECT WHICH DAC RECEIVES THE FIRST
13              ;       DATA AND FOUR SELECTABLE SCOPE FUNTION BITS. THEY
14              ;       ARE /SCOPE MODE/, /NON-STORE/, /WRITE-THROUGH/
15              ;       AND /ERASE/. THE ERASE STATUS BIT CAUSES A PULSE
16              ;       OF DURATION APPROXIMATELY 2 MS ON THE /ERASE/ LINE
17              ;       (A13, LOW ACTIVE OPEN COLLECTOR SIGNAL), WHICH CAN BE
18              ;       USED TO ERASE A SCOPE. THE DOA COMMAND SHOULD NOT
19              ;       BE GIVEN IF BUSY IS SET AND MUST APPEAR FIRST BEFORE
20              ;       DOB AND DOC IN A DATA CHANNEL SETUP SEQUENCE. ALL
21              ;       STATUS BITS REMAIN THE SAME UNTIL THE NEXT DOA
22              ;       INSTRUCTION OR /IORST/, WHICH CLEARS ALL STATUS BITS.
23              ;       SYNCHRONIZTION TO A CLOCK OCCURS ON THE FALLING
24              ;       EDGE OF THE CLOCK.
25              ;
26              ;       WHEN POWER IS FIRST APPLIED TO THE DAC BOARD
27              ;       THE DIGITAL CODE FOR 0 VOLTS IS APPLIED TO EACH DAC
28              ;       UNTIL THE FIRST CONVERSION. /IORST/ AGAIN CAUSES 0
29              ;       VOLTS TO BE OUTPUTTED FROM EACH DAC. OTHERWISE, THE
30              ;       VOLTAGE OUTPUT OF EACH DAC IS THAT OF THE LAST
31              ;       CONVERSION.
32              ;
33              ;       IF THE /SCOPE MODE/ IN A DOA INSTRUCTION (D4) IS 0
34              ;       (ACTIVE LOW SIGNAL), A Z-AXIS PULSE WILL OCCUR EVERY
35              ;       TIME A NEW DIGITAL CODE IS SENT TO EITHER DAC X
36              ;       OR DAC Y (JUMPER SELECTABLE). THE Z PULSE,
37              ;       WHICH IS AN INTENSIFICATION PULSE, ACTUALLY OCCURS
38              ;       AFTER A 7 US DELAY TO ALLOW DAC SETTLING.
39              ;       THE Z PULSE MAY BE AC OR DC COUPLED (JUMPER
40              ;       SELECTABLE). THE DC LEVEL OF THE Z-AXIS SIGNAL
41              ;       SHOULD BE ADJUSTED BY THE POT PROVIDED SO THAT
42              ;       THE CRT OR OSCILLOSCOPE TRACE IS JUST BARELY
43              ;       BLANKED. THE Z PULSE CAN BE UP TO THREE 0.5
44              ;       VOLT LEVELS ABOVE OR BELOW THIS DC LEVEL (UP-DOWN
45              ;       IS JUMPER SELECTABLE). THE AMPLITUDE OF THE Z
46              ;       PULSE CAN BE INCREASED TO THREE 2 VOLT LEVELS
47              ;       BY CHANGING THE 3.3K RESISTOR TO 680 OHMS AND
48              ;       THE 8.2K TO 3.3K. THE BRIGHTNESS OF THE Z PULSE
49              ;       IS DETERMINED BY BITS 14 AND 15 OF THE DATA WORD
50              ;       WHICH CAUSES THE Z PULSE (NOTE THAT BITS 0-11
51              ;       CONTAIN D/A DATA). THE FOLLOWING CODES DETERMINE
52              ;       THE BRIGHTNESS:
53              ;
54              ;       D14     D15             BRIGHTNESS LEVEL
55              ;       0       0       1.5 VOLTS +/- DC LEVEL
56              ;       0       1       1.0 VOLTS +/- DC LEVEL
57              ;       1       0       0.5 VOLTS +/- DC LEVEL
58              ;       1       1       NO CHANGE IN DC LEVEL DURING Z PULSE
```

```
10010 .MAIN
01              ;       ALL PROGRAMMED I/O DIGITAL-TO-ANALOG CONVERSIONS
02              ;       SHOULD NORMALLY BEGIN WITH A DOCS INSTRUCTION. THE
03              ;       DOC INSTRUCTION WILL LOAD THE FIRST BUFFER WITH DATA.
04              ;       PIO CONVERSIONS THAT ARE SYNCHRONIZED TO AN INTERNAL
05              ;       OR EXTERNAL CLOCK WILL OCCUR WITHOUT THE START COMMAND,
06              ;       ON THE FIRST FALLING EDGE OF THE CLOCK PULSE AFTER
07              ;       THE DOC COMMAND HAS BEEN ISSUED. HENCE, IF IT IS
08              ;       DESIRED TO DO PROGRAMMED, SYNCHRONIZED CONVERSIONS
09              ;       WITHOUT SETTING DONE, THE DOC COMMAND ALONE MAY BE
10              ;       GIVEN. FOR NON-SYNCHRONIZED PROGRAMMED I/O CONVERSIONS,
11              ;       THE I/O START COMMAND MUST BE GIVEN TO SEND THE DATA
12              ;       FROM THE FIRST BUFFER TO THE SECOND BUFFER AND OUT
13              ;       TO THE DACS FOR CONVERSION.
14              ;
15              ;       FOR DATA CHANNEL TRANSFERS, THE I/O START COMMAND CAUSES
16              ;       THE FIRST DATA CHANNEL TRANSFER TO THE FIRST BUFFER.
17              ;       SUBSEQUENTLY, THE CLOCK SOURCE SELECTED BY THE
18              ;       DOA INSTRUCTION OUTPUTS THE DATA TO THE APPROPRIATE
19              ;       DAC AND REQUESTS ANOTHER DATA CHANNEL TRANSFER.
20              ;
21              ;       THE EVENT WHICH CAUSES DONE TO BE SET VARIES, DEPENDING
22              ;       ON THE MODE IN WHICH INTERFACE IS BEING USED. FOR
23              ;       UNSYNCHRONIZED CONVERSIONS IN WHICH THE SCOPE MODE IS
24              ;       NOT BEING USED (NO Z-AXIS PULSES TRIGGERED AFTER THE
25              ;       CONVERSION), THE DOCS COMMAND TO START A CONVERSION
26              ;       WILL, OF COURSE, SET BUSY BUT DONE WILL NEVER BE SET
27              ;       IN THIS MODE BECAUSE OF THE FAST SPEED OF THE CON-
28              ;       VERSION (BUSY WILL REMAIN SET). BEFORE NEW STATUS BITS
29              ;       ARE SELECTED (VIA A DOA INSTRUCTION), BUSY SHOULD BE
30              ;       CLEARED (VIA AN I/O CLEAR). DONE IS SET AS FOLLOWS:
31
```

```
10011 .MAIN
01              ;       DOA INSTRUCTION STATUS BITS     DONE SETTING SOURCE
02              ;       ===========================     ===================
03              ;       MODE    CLOCK   /SCOPE
04              ;       DCH     SYNC    MODE/
05              ;       --      --      --
06              ;       D0      D1      D4
07              ;       --      --      --
08
09              ;       0       0       0               END OF Z PULSE
10
11              ;       0       0       1               NONE
12
13              ;       0       1       0               END OF Z PULSE
14
15              ;       0       1       1               2ND BUFFER CLOCK PULSE
16              ;                                       (FALLING EDGE OF
17              ;                                       EXTERNAL/INTERNAL CLK
18              ;                                       INDICATES DATA SENT
19              ;                                       TO DAC)
20
21              ;       1       0       0               END OF Z PULSE AFTER
22              ;                                       /WCEZ/ (NOTE: LAST
23              ;                                       DATA CHANNEL WORD MUST
24              ;                                       CAUSE Z PULSE OR ELSE
25              ;                                       DONE WILL NOT SET)
26
27              ;       1       0       1               2ND BUFFER CLOCK PULSE
28              ;                                       AFTER /WCEZ/(SYCHRONIZED
29              ;                                       TO FALLING EDGE OF
30              ;                                       /IOPLS/ OR /DATA READY/
31              ;                                       = INDICATES LAST DATA
32              ;                                       IN DCH TRANSFER HAS
33              ;                                       BEEN SENT TO DAC
34
35              ;       1       1       0               END OF Z PULSE AFTER
36              ;                                       /WCEZ/ (SEE NOTE ABOVE)
37
38              ;       1       1       1               2ND BUFFER CLOCK PULSE
39              ;                                       AFTER /WCEZ/. SYNCHRO-
40              ;                                       NIZED TO FALLING EDGE
41              ;                                       OF INTERNAL/EXTERNAL
42              ;                                       CLOCK = INDICATES LAST
43              ;                                       DATA IN DCH TRANSFER HAS
44              ;                                       BEEN SENT TO DAC
45
46              ;       NOTE = IN THE DATA CHANNEL MODES ABOVE, DONE MAY
47              ;       ALSO BE SET BY THE LATE CONVERSION SIGNAL, IF THE
48              ;       APPROPRIATE JUMPER CONNECTION IS MADE.
```

```
10012 .MAIN
01              ;       IF THE PERIOD OF THE SYNCHRONIZING CLOCK IN DATA
02              ;       CHANNEL MODE IS LESS THAN THE DATA CHANNEL LATENCY
03              ;       TIME, DATA WILL NOT BE LOST, BUT IT WILL NOT APPEAR
04              ;       AT THE DAC AT THE CORRECT SYNCHRONIZING CLOCK EDGE.
05              ;       RATHER, IT WILL APPEAR AT THE APPROPRIATE DAC AT THE
06              ;       TIME OF THE FIRST TRAILING EDGE OF THE CLOCK AFTER
07              ;       THE FIRST BUFFER HAS BEEN LOADED WITH NEW DATA. THE
08              ;       DATA APPEARING AT THE DACS IS LATE FOR SYN-
09              ;       CHRONIZATION, HOWEVER, AND THE LATE CONVERSION SIGNAL
10              ;       IS SET. THIS SIGNAL MAY BE READ IN AS A STATUS
11              ;       BIT BY A DIA INSTRUCTION AND MAY, BY
12              ;       SETTING A JUMPER, SET DONE. THE LATE CONVERSION
13              ;       SIGNAL IS CLEARED BY AN I/O CLEAR OR DOA INSTRUCTION.
14
15              ;       IF THIS INTERFACE IS BEING USED TO DISPLAY ON A SCOPE
16              ;       AN ARRAY OF POINTS LOCATED IN MEMORY, DATA CHANNEL
17              ;       MODE SHOULD BE USED WITH THE ALTERNATE BIT SET, THE
18              ;       /SCOPE MODE/ BIT RESET (THIS IS AN ACTIVE-LOW SIGNAL)
19              ;       AND DATA ARRAYED IN MEMORY XYXYXYXY...OR YXYXYXYX...
20              ;       IN THE FORMER CASE, DAC X IS SELECTED AS THE FIRST
21              ;       DAC TO RECEIVE DATA AND THE SCOPE CIRCUITRY IS JUMPED
22              ;       SO THAT A Z PULSE OCCURS AFTER CLOCK Y, AND THE
23              ;       BRIGHTNESS CIRCUIT IS JUMPERED FOR BRTYMSB AND
24              ;       BRTYLSB. FOR THE YXYXYXYX... ORIENTATION, SET UP
25              ;       IS REVERSED. THE Z DELAY (7 US) + THE Z PULSE
26              ;       WIDTH MAY NOT EXCEED THE CLOCK PERIOD. HENCE,
27              ;       THE Z INTENSIFICATION PULSE IS DONE BEFORE ANY DAC IS
28              ;       UPDATED WITH NEW DATA.
29
30              ;       AN EXTERNAL INTERRUPT MAY BE REQUESTED BY PULLING THE
31              ;       /EXTERNAL INTERRUPT/ LINE LOW, WHICH WILL REQUEST AN
32              ;       INTERRUPT WITHOUT SETTING DONE. THE EXTERNAL
33              ;       INTERRUPT REQUEST IS CLEARED BY AN I/O CLEAR OR DOA
34              ;       INSTRUCTION.
35
36              ;       A DIA INSTRUCTION INPUTS FOUR STATUS BITS TO THE CPU:
37              ;       AN EXTERNAL ERASE INPUT BIT WHICH IS SET BY PULLING
38              ;       THE /EXTERNAL ERASE INPUT/ LINE LOW; A DATA READY BIT
39              ;       TO INDICATE THAT NEW DATA HAS BEEN LOADED INTO THE
40              ;       FIRST BUFFER (USEFUL FOR THE IOPLS DATA CHANNEL MODE)
41              ;       A LATE CONVERSION ERROR BIT; AND A BIT INDICATING
42              ;       THE PRESENCE OF AN EXTERNAL INTERRUPT.
43
44              ;       THE FOLLOWING ARE THE NOMINAL RANGES (PERIODS) FOR
45              ;       THE INTERNAL CLOCK AND THE ZPULSE (ADJUSTABLE BY
46              ;       POTENTIOMETERS ON THE D/A BOARD):
47
48              ;       WHAT            MIN     MAX     POT.
49              ;       ====            ===     ===     ====
50              ;       INTERNAL CLOCK  16 US   190 US  R43
51              ;       ZPULSE          4 US    150 US  R32
52
53              ;       PERTINENT SIGNALS & I/O PIN DESIGNATIONS ARE:
54
55              ;       DAC X OUTPUT = A49,     RETURN = A50
56              ;       DAC Y OUTPUT = A29,     RETURN = A30
57              ;       Z-AXIS OUTPUT = A25,    RETURN = A26
58              ;       INT CLK OUTPUT = A17,   RETURN = A18
59              ;       EXT CLK INPUT = A1,     RETURN = A2
```

```
10013 .MAIN
01                ;7.2    PROGRAM OPERATION:
02
03                ;7.2.0  GENERAL DESCRIPTIONS & INFORMATION:
04
05                ;       THIS SYSTEM EXERCISER CONSISTS OF TWO DIFFERENT
06                ;       PROGRAMS. THE FIRST IS A MULTIPLEXER ANALOG INPUT
07                ;       TEST, WHICH TESTS ANALOG AND DIGITAL FUNCTIONS ON
08                ;       THE 4223 ANALOG TO DIGITAL CONVERTER INTERFACE BOARD.
09                ;       THE SECOND IS A CLOSED LOOP SYSTEM TEST DESIGNED TO
10                ;       TEST ANALOG AND DIGITIAL FUNCTIONS ON BOTH THE 4223
11                ;       A/D INTERFACE AND THE 4224 DIGITAL TO ANALOG INTERFACE
12                ;       BOARDS. BOTH OF THESE TESTS REQUIRE AN 1125A VOLTAGE
13                ;       ANALOG TEST ADAPTER WITH ACCOMPANYING CABLES FOR THE
14                ;       THE TEST CONFIGURATION. THE PROGRAMS ARE DESIGNED TO
15                ;       BE EASY TO SET-UP AND USE. THEY CONTAIN MANY SPECIAL
16                ;       FEATURES SUCH AS THE SELECTION OF BOTH TESTS FROM ONE
17                ;       STARTING ADDRESS, THE ABILITY TO ENTER AN INTERNAL
18                ;       DEBUGGER FOR ERROR ISOLATION, AUTOMATIC TEST PARAMETER
19                ;       SELECTION TO TEST THE DIFFERENT OPERATING MODES OF THE
20                ;       BOARDS AND THE ABILITY TO DISPLAY VARIOUS INFORMATION
21                ;       DURING TEST OPERATION. THERE ARE SEVERAL OPERATOR/PRO-
22                ;       GRAM INTERACTIONS THAT ARE POSSIBLE (BUT NOT NECESSARY)
23                ;       SUCH AS DETAILED ERROR, TEST PARAMETER AND TEST CONFIG-
24                ;       URATION SUMMARY REPORTS. DIFFERENT ACTIONS ARE POSSIBLE
25                ;       WHEN AND IF ERRORS OCCUR DURING PROGRAM OPERATION.
26
27                ;       THIS EXERCISER CONTAINS THE FOLLOWING ROUTINES, WHICH
28                ;       WILL BE DESCRIBED IN FULL:
29
30                ;       - MULTIPLEXER ANALOG INPUT TEST
31                ;       - MULTIPLEXER ANALOG INPUT TEST W/DATA CHANNEL EXERCISER
32                ;       - D/A TO A/D LOOP AROUND TEST
33                ;       - D/A TO A/D LOOP AROUND TEST W/DATA CHANNEL EXERCISER
34
35                ;       THE MUX ANALOG INPUT TEST WILL CHECK THE ANALOG/DIGITAL
36                ;       SECTIONS OF A 4223 A/D CONVERTER. THE ANALOG SECTIONS
37                ;       ARE TESTED BY THE USE OF AN 1125A TEST ADAPTER AND AN
38                ;       EXTERNAL VOLTAGE SOURCE. WHEN PROPERLY SET UP, THE
39                ;       ADAPTER ACTS AS A "LADDER NETWORK" THAT APPLIES DIFFER-
40                ;       ENT VOLTAGES TO THE MUX INPUT CHANNELS. THIS IS USED
41                ;       TO TEST THESE CHANNELS AND A/D MODULES (SAMPLE & HOLD,
42                ;       A/D CONVERTER) FOR CONTINUITY, INDEPENDENCE AND PROPER
43                ;       FUNCTIONING. THIS TEST NEED NOT BE RUN IF THE "D/A TO
44                ;       D/A LOOP AROUND TEST" IS RUN FIRST, WITHOUT ERROR.
45
46                ;       THE D/A TO A/D LOOP AROUND TEST PUTS THE 4223 A/D
47                ;       INTERFACE AND THE 4224 D/A INTERFACE BOARDS IN A
48                ;       CLOSED ANALOG LOOP TEST CONFIGURATION VIA THE 1125A
49                ;       TEST ADAPTER AND CABLES. THIS CONFIGURATION CONNECTS
50                ;       THE D/A CHANNELS TO THE MUX CHANNELS SO THAT DATA
51                ;       CAN BE SENT TO THE D/A AND CONVERTED TO A VOLTAGE WHICH
52                ;       IS RECEIVED BY THE A/D AND CONVERTED BACK TO DIGITAL
53                ;       DATA. VARIOUS SUB-TESTS USE DIFFERENT TYPES OF DATA TO
54                ;       CHECK THE ANALOG SECTIONS FOR OPEN/SHORT MUX CHANNELS,
55                ;       CHANNEL OR LOOP INDEPENDENCE (NO D/A OR MUX CHANNEL
56                ;       INTERACTION) AND CONVERTER LINEARITY. IN ADDITION, MOST
57                ;       OPERATING MODES ON BOTH INTERFACES ARE EXERCISED.
```

```
10014 .MAIN
01                ;       OVERALL SYSTEM PERFOMANCE IS BASED ON INSPECTION AND
02                ;       ANALYSIS OF THE TRANSFER/ERROR INFORMATION FOR ANALOG
03                ;       SECTIONS AND THE ABSENCE OF FUNCTIONAL ERROR REPORTS
04                ;       (SECTION 10) FOR DIGITIAL SECTIONS. SEE INDIVIDUAL TEST
05                ;       DESCRIPTIONS FOR DETAILED INFORMATION ON POSSIBLE ERRORS.
06
07                ;       IT SHOULD BE NOTED THAT NEITHER TEST CAN BE CONSIDERED
08                ;       AS AN ANALOG CONVERTER ACCURACY TEST, ALTHOUGH PROPER
09                ;       ANALOG FUNCTIONING CAN BE ASSUMED IF THE APPROPRIATE
10                ;       TEST RUNS WITHOUT ERROR.
11
12                ;       SPECIAL NOTE: RUNNING TESTS WITH DCH EXERCISER (KITTEN).
13
14                ;       BOTH ANALOG TESTS WILL RUN IN CONJUNCTION WITH THE DATA
15                ;       CHANNEL (DCH) EXERCISER PROGRAM "KITTEN". A SPECIAL I/O
16                ;       TESTER BOARD IS REQUIRED TO BE IN THE MICRO NOVA CHASSIS
17                ;       IF THIS OPTION IS DESIRED. THE DCH EXERCISER SIMPLY SENDS
18                ;       AND RECEIVES DATA TO AND FROM THE I/O TESTER BOARD VIA
19                ;       THE DATA CHANNEL. THE PURPOSE IS TO DETERMINE HOW THE A/D
20                ;       AND/OR D/A BEHAVE IN THE PRESENCE OF OTHER BUS ACTIVITY.
21                ;       THESE PROGRAMS WILL NOT RUN WITH THE "CATS" VERSION OF
22                ;       THE DCH EXERCISER. THIS PROGRAM IS THE SAME AS "KITTEN"
23                ;       EXCEPT THAT IT USES A DISKETTE DRIVE INSTEAD OF THE I/O
24                ;       TESTER BOARD. IF "CATS" IS USED, I/O ADDRESS ERRORS WILL
25                ;       OCCUR, DUE TO THE FACT THAT THE PROGRAM HOLDS OFF DISK
26                ;       INTERRUPTS FOR MORE THAT 200 MILLISECONDS DURING DATA
27                ;       HANDLING, CALCULATIONS ETC. SEE SECTIONS 4 AND 9.1 FOR
28                ;       MORE DCH EXERCISER INFORMATION.
```

```
10015 .MAIN
01              ;7.2.1  PROGRAM DESCRIPTION: MULTIPLEXER ANALOG INPUT TEST
02              ;                            MULTIPLEXER ANALOG INPUT TEST
03              ;                            WITH DATA CHANNEL EXERCISER
04
05              ;       INTRODUCTION:
06
07              ;       THIS PROGRAM IS A STATIC (DC) TEST USED TO AUTOMATICALLY
08              ;       TEST THE 16. SINGLE-ENDED MODE AND 8. DIFFERENTIAL MODE
09              ;       MULTIPLEXER ANALOG INPUT CHANNELS, AS WELL AS THE A/D
10              ;       MODULES (SAMPLE/HOLD, INSTRUMENTATION AMPLIFIER, A/D
11              ;       CONVERTER) OF THE MODEL 4223 ANALOG TO DIGITAL INTER-
12              ;       FACE. THE ANALOG SECTIONS ARE TESTED USING A VOLTAGE
13              ;       TEST ADAPTER AND EXTERNAL VOLTAGE SOURCE. THE ADAPTER
14              ;       ACTS AS A "LADDER NETWORK" THAT APPLIES STATIC VOLTAGES
15              ;       TO THE MULTIPLEXER CHANNELS IN A CONFIGURATION THAT
16              ;       ALLOWS THE PROGRAM TO EXERCISE AND CHECK THEM FOR
17              ;       CONTINUITY AND INDEPENDENCE AND PROPER CONVERTER SECTION
18              ;       PERFORMANCE. IN ADDITION, THE DIFFERENT OPERATING
19              ;       CONDITIONS (MODES, TRIGGERING, STATUS) ARE EXERCISED
20              ;       TO INSURE THAT THE DIGITAL AND CONTROL FUNCTIONS WORK.
21
22              ;       REQUIRED TEST HARDWARE:
23
24              ;       1) MODEL 1125A VOLTAGE ANALOG TEST ADAPTER
25              ;       2) CABLE: 1125A ADAPTER TO 4223 A/D CONVERTER;
26              ;                 PART # 005 - 12431; WIRE LIST # 008 - 2184
27              ;       3) EXTERNAL DC VOLTAGE SOURCE (+/- 10 VDC MAXIMUM)
28
29              ;       TEST PROCEDURES:
30
31              ;       THE MICRO-NOVA CHASSIS AND ANY EXTERNAL VOLTAGE
32              ;       SOURCES SHOULD BE POWERED DOWN WHILE INSERTING OR
33              ;       MAKING ANY CONNECTIONS TO/FROM THE BOARDS. THE TEST
34              ;       IS SET UP AS FOLLOWS:
35
36              ;       1) MAKE SURE THAT THE 4223 A/D INTERFACE IS IN
37              ;          THE MICRO NOVA CHASSIS (SEE SECTION 9.1). IN
38              ;          ADDITION, THE A/D SHOULD SUCCESSFULLY RUN
39              ;          THE DIAGNOSTIC PROGRAM, AND MUST BE PROPERLY
40              ;          CALIBRATED (SEE SECTION 4).
41              ;       2) INSURE THAT NO CONNECTIONS ARE MADE TO THE "D/A"
42              ;          CONNECTOR (J1) OF THE 1125A TEST ADAPTER.
43              ;       3) CONNECT ONE END OF THE ADAPTER CABLE (SEE ABOVE)
44              ;          TO THE KEYED I/O CONNECTOR OF THE A/D, AND THE
45              ;          OTHER TO THE "MUX" CONNECTOR (J2) ON THE TEST
46              ;          ADAPTER. (THE CONNECTORS ONLY FIT ONE WAY).
47              ;       4) WITH THE POWER OFF, CONNECT THE EXTERNAL VOLTAGE
48              ;          SOURCE TO THE "V+" AND "RET" TERMINALS OF THE
49              ;          TEST ADAPTER. THIS VOLTAGE MUST BE +/- 10 VDC
50              ;          MAXIMUM AND MUST BE IN THE RANGE OF THE A/D.
51              ;          FOR EXAMPLE, A -10 VDC VOLTAGE CANNOT BE USED
52              ;          WITH A 0 - 5 VOLT A/D CONVERTER. THIS VOLTAGE
53              ;          IS THE LADDER SOURCE VOLTAGE OR "V.IN".
54              ;       5) SET THE SWITCHES ON THE 1125A ADAPTER AS FOLLOWS:
55              ;          SWITCHES 1,2,3,4,8 = ON (ALL OTHERS OFF).
56              ;       6) POWER UP THE MICRO NOVA CHASSIS AND TURN ON THE
57              ;          EXTERNAL VOLTAGE SOURCE.
58              ;       7) LOAD THE EXERCISER, SELECT AND INITIALIZE THE
59              ;          "MULTIPLEXER ANLOG INPUT TEST". SEE SECTION 9.1
60              ;          FOR LOADING AND INITIALIZATION INFORMATION.
```

```
 0016 .MAIN
01              ;       NOTES ON TEST INITIALIZATION:
02
03              ;       THE RESPONSE TO THE LADDER SOURCE VOLTAGE QUESTION
04              ;       CAN BE EITHER THE SIGNED, DECIMAL, MILLIVOLT VALUE
05              ;       OF THE EXTERNAL VOLTAGE SOURCE (V.IN), OR "A". IF THE
06              ;       RESPONSE IS "A", THE PROGRAM WILL TRY TO DETERMINE IT
07              ;       FOR YOU AUTOMATICALLY. IN THE FIRST CASE, THE VALUE
08              ;       ENTERED MUST BE < = THE A/D CONVERTER FULL SCALE RANGE.
09              ;       FOR EXAMPLE, IT MUST BE WITHIN THE RANGE OF +/- 5 VDC
10              ;       FOR A BIPOLAR, LOW RANGE A/D INTERFACE. IN THE SECOND
11              ;       CASE, THE PROGRAM TRIES TO DETERMINE "V.IN" BY SAMPLING
12              ;       MUX CHANNEL 0 IN SINGLE-ENDED MUX TYPE OPERATING MODE.
13              ;       IT THEN PRINTS THIS VALUE TO THE OPERATOR AS FOLLOWS:
14
15              ;       LADDER SOURCE VOLTAGE = (X)      MV
16
17              ;       (THE VALUE PRINTED (X) IS SIGNED DECIMAL MILLIVOLTS).
18              ;       THIS CHANNEL NORMALLY SEES 100% OF THE LADDER VOLTAGE,
19              ;       OR THE ACTUAL EXTERNAL VOLTAGE BEING APPLIED WHEN THE
20              ;       MUX TYPE IS SINGLE-ENDED. HOWEVER, THE PROGRAM ASSUMES
21              ;       THAT THE CONVERTER DOES IN FACT PERFORM CORRECT ANALOG
22              ;       CONVERSIONS, AND THAT THE VOLTAGE VALUE RECEIVED FROM
23              ;       THIS CHANNEL IS CORRECT. IF THEY ARE NOT, DATA ERRORS
24              ;       WILL BE REPORTED ON OTHER MUX CHANNELS. IF THIS OCCURS,
25              ;       RE-START THE TEST AND ENTER THE MILLIVOLT VALUE INSTEAD,
26              ;       TO DETERMINE THE CAUSE OF THE FAILURE.
27
28              ;       TEST OPERATION:
29
30              ;       AFTER THE INITIALIZATION SEQUENCE (INCLUDING AUTO-
31              ;       FINDING OF THE LADDER SOURCE VOLTAGE IF SELECTED), THE
32              ;       TEST PARAMETERS AND A/D CONVERTER ARE INITIALIZED AND
33              ;       THE TEST IS STARTED. INITIALLY, THE TEST PARAMETERS ARE
34              ;
35              ;       - PIO MODE
36              ;       - STRT PULSE TRIGGERING, NO SYNCHRONIZATION
37              ;       - MUX TYPE IS DIFFERENTIAL
38              ;         (8. DIFFERENTIAL CHANNELS)
39
40              ;       THE ACTUAL TEST IS DIVIDED INTO 3 SECTIONS: 1) THE MUX
41              ;       CHANNELS ARE SCANNED SUCH THAT EACH CHANNEL TO BE
42              ;       TESTED IS SAMPLED 8. TIMES. THEREFORE, 128. CONVERSIONS
43              ;       ARE PERFORMED FOR SINGLE-ENDED MUX TYPE (16. CHANNELS
44              ;       X 8. SAMPLES EACH) OR 64. CONVERSIONS ARE PERFORMED
45              ;       FOR DIFFERENTIAL MUX TYPE (8. CHANNELS X 8. SAMPLES);
46              ;       2) THE MUX CHANNEL RECEIVE (ACTUAL) AVERAGES ARE THEN
47              ;       CALCULATED FROM THE SAMPLES TAKEN; 3) THE MUX CHANNEL
48              ;       RECEIVE AVERAGES ARE THEN COMPARED AGAINST THE MAXIMUM
49              ;       AND MINIMUM DATA VALUES EXPECTED FROM THEM. THESE WERE
50              ;       PREVIOUSLY DETERMINED DURING TEST PARAMETER INITIAL-
51              ;       IZATION. A DATA ERROR (SEE ERROR DESCRIPTIONS) IS
52              ;       REPORTED FOR ANY AND ALL CHANNELS WHOSE RECEIVE AVERAGES
53              ;       ARE NOT WITHIN THE EXPECTED RANGE. IF THE RECEIVE
54              ;       AVERAGE IS WITHIN THE EXPECTED RANGE FOR A PARTICULAR
55              ;       MUX CHANNEL, THEN THE TRANSFER COUNT FOR THAT CHANNEL
```

```
10017 .MAIN
01              ;       IS INCREMENTED (ONCE FOR EACH SUCCESSFUL TEST). IF THE
02              ;       RECEIVE AVERAGE IS NOT WITHIN THE EXPECTED RANGE, THEN
03              ;       BOTH TRANSFER AND ERROR COUNTS ARE INCREMENTED FOR THE
04              ;       MUX CHANNEL IN ERROR. THIS TABULATED INFORMATION CAN
05              ;       BE PRINTED AT ANY TIME BY HITTING THE "SPACE" BAR ON
06              ;       THE TTY CONSOLE (SEE SECTION 10). AFTER ALL CHANNELS
07              ;       HAVE BEEN SCANNED, AVERAGED AND CHECKED, AND IF THE
08              ;       PROGRAM IS NOT LOOPING ON A DETECTED ERROR, THE TEST
09              ;       PARAMETERS WILL BE CHANGED TO THE NEXT TEST STATE, AND
10              ;       THE MUX CHANNELS WILL BE TESTED AGAIN. THE SEQUENCE
11              ;       OF A/D - MUX PARAMETERS TESTED ARE AS FOLLOWS:
12              ;
13              ;       MUX TYPE  MODE   TRIGGERING
14              ;       --------  ----   ----------
15              ;       DIFF.     PIO    STRT
16              ;       DIFF.     PIO    INT CLK
17              ;       DIFF.     PIO    EXT CLK
18              ;       DIFF.     DCH    IOPLS
19              ;       DIFF.     DCH    DCHI
20              ;       DIFF.     DCH    INT CLK
21              ;       DIFF.     DCH    EXT CLK
22              ;       S.E.      PIO    STRT
23              ;       S.E.      PIO    INT CLK
24              ;       S.E.      PIO    EXT CLK
25              ;       S.E.      DCH    IOPLS
26              ;       S.E.      DCH    DCHI
27              ;       S.E.      DCH    INT CLK
28              ;       S.E.      DCH    EXT CLK
29              ;
30              ;       WHERE: DIFF. = DIFFERENTIAL
31              ;              S.E. = SINGLE-ENDED
32              ;              PIO = PROGRAMMED INPUT/OUTPUT (I/O)
33              ;              DCH = DATA CHANNEL
34              ;              INT/EXT CLK = INTERNAL/EXTERNAL CLOCK SYNC
35              ;              STRT = START PULSE (I.E. "NIOS" INSTRUCTION)
36              ;              IOPLS = I/O PULSE (I.E. "NIOP" INSTRUCTION)
37              ;              DCHI = DATA CHANNEL INPUT (A CONTROL SIGNAL)
38              ;
39              ;       AFTER ALL OF THE ABOVE MODES ARE TESTED, THE SEQUENCE
40              ;       STARTS OVER AGAIN AND WILL CONTINUE UNTIL OPERATOR
41              ;       TERMINATED. IF A/D ERRORS EXIST, THIS PROGRAM CAN BE
42              ;       USED TO DETECT AND TRACE THE CAUSE OF THE ERROR(S).
43              ;       THIS IS EXPLAINED IN THE FOLLOWING SECTION. REFER TO
44              ;       SECTION 10 FOR INFORMATION ON SPECIAL PROGRAM FEATURES
45              ;       SUCH AS TEST PARAMETER SUMMARY AND ERROR SUMMARY
46              ;       REPORTS. THEY WILL BE HELPFUL DURING PROGRAM OPERATION.
47              ;
48              ;       ERROR DESCRIPTIONS:
49              ;
50              ;       THERE ARE TWO CATAGORIES OR CLASSES OF ERRORS THAT
51              ;       ARE DETECTED AND REPORTED. THE FIRST ARE A/D
52              ;       FUNCTIONAL ERRORS AND ARE ASSOCIATED WITH FAILURES
53              ;       IN THE A/D LOGIC AND CONTROL FUNCTIONS (I.E. IN
54              ;       CONVERSION TRIGGERING, DATA TRANSFER MODES (PIO, DCH),
55              ;       A/D STATUS INFORMATION ETC.). THESE ERRORS ARE DETECTED
56              ;       AND REPORTED FROM THE A/D DRIVER ROUTINE "SCAN". SEE
57              ;       SECTION 10 FOR INFORMATION REGARDING THESE ERRORS.
58              ;       IF THEY OCCUR, RUN THE A/D INTERFACE DIAGNOSTIC
59              ;       PROGRAM (SECTION 4).
```

```
10018 .MAIN
01              ;       THE SECOND CLASS OF ERRORS DETECTED AND REPORTED ARE
02              ;       DATA ERRORS. THESE FAILURES, IF THEY OCCUR, INDICATE
03              ;       A MALFUNCTION IN THE ANALOG SECTIONS OF THE A/D OR
04              ;       IN THE TEST HARDWARE (ADAPTER, CABLES, CONNECTORS).
05              ;
06              ;       IF A RECEIVE AVERAGE FROM A MUX CHANNEL IS NOT WITHIN
07              ;       ITS EXPECTED RANGE AND "SWREG" SWITCH D = 0 (SECTION 8),
08              ;       THE FOLLOWING ERROR IS REPORTED:
09              ;
10              ;       *** DATA ERROR ***
11              ;       DETECTED IN ROUTINE "CHECK" CALLED AT: (OCTAL ADDRESS)
12              ;       CHANNEL:MUX     SOURCE  MUX TYPE
13              ;               (M)     (S)     (TYPE)
14              ;       DATA: EXPECTED  RECEIVED        MAX EXP MIN EXP
15              ;             EEEEEE    RRRRRR          XXXXXX  NNNNNN
16              ;
17              ;       WHERE:  (M) = MUX CHANNEL # (DECIMAL)
18              ;                     (0 - 7 IF DIFF., 0 - 15 IF S.E. MUX TYPES)
19              ;               (S) = 1125A ADAPTER SOURCE CHANNEL # (0 - 3)
20              ;               (TYPE) = MUX TYPE (SINGLE-ENDED OR DIFFERENTIAL)
21              ;               EEEEEE = EXPECTED CENTER VALUE FOR MUX CHANNEL
22              ;                        (M) = CORRECT VALUE
23              ;               RRRRRR = ACTUAL RECEIVE AVERAGE FROM MUX CHANNEL
24              ;                        (M) = ERROR VALUE
25              ;               XXXXXX = EXPECTED MAXIMUM FOR MUX CHANNEL (M)
26              ;               NNNNNN = EXPECTED MINIMUM FOR MUX CHANNEL (M)
27              ;               (OCTAL ADDRESS) = THE ADDRESS IN THE PROGRAM
28              ;                                 LISTING WHERE THE "CHECK"
29              ;                                 SUBROUTINE IS CALLED FROM.
30              ;
31              ;               DATA VALUES (EEEEEE, RRRRRR, XXXXXX, NNNNNN) ARE
32              ;               AS FOLLOWS:
33              ;               - SWITCH C = 0  DATA IS 12-BIT OCTAL A/D DATA,
34              ;                               LEFT-JUSTIFIED, UNUSED BITS = 0
35              ;               - SWITCH C = 1  VALUE IS THE SIGNED, DECIMAL
36              ;                               MILLIVOLT EQUIVALENT OF THE
37              ;                               THE OCTAL A/D DATA.
38              ;
39              ;       DATA ERROR REPORTS ARE SUPPRESSED BY SETTING SWITCH
40              ;       D = 1 (SEE SECTION 8 FOR SWITCH INFORMATION).
41              ;
42              ;       ERROR HANDLING AND INTERPRETATION OF ERROR INFORMATION:
43              ;
44              ;       IF DATA ERRORS ARE OCCURING, THE FIRST THING TO
45              ;       CHECK IS THE TEST HARDWARE SET-UP. MAKE SURE THAT
46              ;       THE CONNECTOR PINS ARE NOT BROKEN OR MISSING, THAT
47              ;       THE CABLES ARE CONNECTED PROPERLY AND THAT THE ADAPTER
48              ;       SWITCHES ARE CORRECTLY SET. ALSO BE SURE THAT THE
49              ;       EXTERNAL VOLTAGE SOURCE IS CONNECTED AND IS ON.
50              ;       IF EVERYTHING APPEARS TO BE IN ORDER, THEN ONE
51              ;       OR MORE MUX CHANNELS, OR THE A/D CONVERTER MODULES
52              ;       AND CIRCUITRY MAY BE FAILING. IN THIS CASE, USE
53              ;       THE TEST DATA TO DETERMINE WHAT IS CAUSING THE
54              ;       DATA ERRORS. INSURE THAT THE TEST WAS PROPERLY
55              ;       INITIALIZED, AS DATA ERRORS WILL BE REPORTED IF
56              ;       MISTAKES ARE MADE IN THE INITIALIZATION SEQUENCE.
```

```
10019 .MAIN
01              ;       IF DATA ERRORS STILL EXIST AFTER CHECKING THE
02              ;       ABOVE ITEMS, AN ERROR EXISTS SOMEWHERE IN THE
03              ;       ANALOG SECTIONS OF THE A/D INTERFACE OR ON THE TEST
04              ;       ADAPTER. THE AREA OF FAILURE CAN BE DETERMINED BY
05              ;       ANALYSIS OF THE INFORMATION CONTAINED IN THE DATA
06              ;       ERROR MESSAGES (SEE ABOVE) AND BY THE TRANSFER/ERROR
07              ;       SUMMARY REPORT. IF AND WHEN DATA ERRORS OCCUR DO THE
08              ;       FOLLOWING:
09              ;
10              ;       1) IF POSSIBLE, OBTAIN A HARD-COPY OF THE DATA ERRORS
11              ;          BEING REPORTED (I.E. OUTPUT TO A LINE PRINTER OR
12              ;          PRINTING TERMINAL). OTHERWISE MAKE A NOTE OF THE
13              ;          PERTINENT ERROR INFORMATION INCLUDING SOURCE
14              ;          CHANNEL, MUX CHANNEL, EXPECTED AND RECEIVED DATA
15              ;          VALUES. DO THIS FOR ALL FAILING MUX CHANNELS.
16              ;       2) SELECT "LOOP ON ERROR" (SWITCH 1 = 0) WHICH IS
17              ;          THE DEFAULT CONDITION. THIS WILL FREEZE THE TEST
18              ;          PARAMETERS IN CASE THEY ARE THE CAUSE OF THE DATA
19              ;          ERRORS.
20              ;       3) SUPPRESS DATA ERROR REPORTS (SWITCH D = 1) AND
21              ;          OBTAIN A TRANSFER/ERROR SUMMARY REPORT AFTER A
22              ;          FEW MINUTES OF PROGRAM OPERATION (3 - 5 MINUTES).
23              ;          (SEE SECTION 10 FOR MORE INFORMATION). AGAIN, A
24              ;          HARD-COPY IS PREFERABLE.
25              ;       4) IF THE A/D OPERATING MODES ARE SUSPECTED AS A CAUSE
26              ;          OF THE DATA ERRORS, A TEST PARAMETER SUMMARY REPORT
27              ;          CAN BE OBTAINED BY TYPING CNTRL-S (SEE SECTION 10).
28              ;
29              ;       FROM THE INFORMATION RECEIVED FROM THESE STEPS, YOU
30              ;       ARE READY TO MAKE AN ANALYSIS. THE FOLLOWING IS SOME
31              ;       HELPFUL INFORMATION REGARDING POSSIBLE FAILURES.
32              ;
33              ;       POSSIBLE FAILURES INCLUDE:
34              ;
35              ;       1) BAD MUX CHANNEL(S)
36              ;       2) BAD SOURCE CHANNEL(S) (INCORRECT VOLTAGE PRESENT)
37              ;       3) NON-INDEPENDENT MUX OR SOURCE CHANNELS (CROSSTALK)
38              ;       4) A/D MODULE FAILURE (SAMPLE/HOLD, A/D CONVERTER ETC.)
39              ;       5) NON-CALIBRATED A/D SUB-SYSTEM.
40              ;       6) POWER SUPPLY FLUCTUATIONS (EXCESSIVE NOISE)
41              ;
42              ;       MORE DETAILED INFORMATION ABOUT THE ABOVE POSSIBLE
43              ;       FAILURES FOLLOWS.
44              ;
45              ;       *** IMPORTANT NOTE ***
46              ;
47              ;       IF USING AN OSCILLOSCOPE OR VOLTMETER/MULTIMETER,
48              ;       ALL MEASUREMENTS MADE ON THE A/D INTERFACE MUST BE DONE
49              ;       VERY CAREFULLY TO INSURE THAT NO OTHER DAMAGE IS CAUSED
50              ;       BY SHORTING SIGNALS TOGETHER. THE INTERFACE SHOULD BE
51              ;       ON AN EXTENDER CARD FOR EASIER ACCESS TO THE BOARD.
52              ;
53              ;       ALSO, IT IS IMPORTANT TO ELIMINATE THE ADAPTER CARD
54              ;       (CONNECTOR, ETCH, RESISTORS AND SWITCHES) AND THE
55              ;       CABLE (ESPECIALLY THE CONNECTORS) AS THE POSSIBLE
56              ;       SOURCES OF FAILURE BEFORE AN ATTEMPT IS MADE TO
57              ;       REPLACE ANY OF THE A/D CONVERTER SUB-SYSTEM MODULES.
58              ;       THESE MODULES SHOULD BE SUSPECTED ONLY AFTER ALL OTHER
59              ;       POSSIBILITIES HAVE BEEN ELIMINATED.
```

```
10020 .MAIN
01              ;       DETAILED FAILURE ANALYSIS:
02              ;
03              ;       1) BAD MUX CHANNEL(S)
04              ;
05              ;          THIS IS ONE OF THE MOST COMMON ANALOG SECTION
06              ;          FAILURES. DATA ERRORS WILL BE REPORTED ON ONE OR
07              ;          MORE MUX CHANNELS, NOT NECESSARILY CONNECTED TO THE
08              ;          SAME ADAPTER SOURCE CHANNEL. IT USUALLY INDICATES
09              ;          A FAILURE (OPEN, SHORTED OR INTERMITTENT) IN THE
10              ;          A/D SUB-SYSTEM MODULE THAT CONTAINS THE ANALOG
11              ;          MULTIPLEXER (M1), OR THE ETCH RUNS CONNECTING
12              ;          THE I/O EDGE PINS AND THE MODULE INPUTS.
13              ;
14              ;          IF A MUX CHANNEL IS OPEN, THE DATA RETURNED
15              ;          SHOULD INDICATE A FLOATING CHANNEL (GENERALLY,
16              ;          BUT NOT NECESSARILY IN THE RANGE OF 1 TO 2
17              ;          VOLTS). 0 VOLTS SHOULD BE RETURNED IF A CHANNEL
18              ;          IS SHORTED TO GROUND. IT COULD ALSO BE SHORTED
19              ;          TO THE ON-BOARD A/D +/- 15 VOLT SUPPLY, TO THE
20              ;          BOARD +5 V ETC. IT IS POSSIBLE TO CHECK THE
21              ;          VOLTAGE LEVEL AT THE SUSPECTED FAILING MUX INPUT
22              ;          WITH A VOLTMETER AND COMPARING IT TO THE EXPECTED
23              ;          RECEIVE VALUE FROM THE DATA ERROR REPORT. (IF
24              ;          SWITCH C = 1, THE ERROR DATA WILL BE PRINTED IN
25              ;          DECIMAL MILLIVOLTS.) IF THE ETCH RUNS ARE O.K.
26              ;          (NO OPEN, SHORTS, COLD-SOLDER JOINTS ETC. EXIST),
27              ;          THEN THE A/D MODULES (M1 FIRST, M2 SECOND) ARE
28              ;          THE PROBABLE FAILING MODULES. INSURE THAT THE
29              ;          MODULE +/- 15 VOLTS SUPPLY IS FUNCTIONING.
30              ;
31              ;       2) BAD SOURCE CHANNEL(S)
32              ;
33              ;          IF THE LADDER VOLTAGE PRESENT AT ONE OR MORE OF
34              ;          SOURCE CHANNELS IS INCORRECT (ALLOWED ERROR
35              ;          RANGE IS +/- 5 %) THEN DATA ERRORS WILL PROBABLY
36              ;          BE REPORTED FROM ALL MUX CHANNELS CONNECTED TO
37              ;          THEM. SEE THE THEORY OF OPERATION SECTION FOR THE
38              ;          CONNECTION SCHEME. THIS INFOMATION CAN ALSO BE
39              ;          RECEIVED FROM THE PROGRAM BY TYPING A CNTRL-C.
40              ;          MEASURE THE VALUE PRESENT ON THE SUSPECTED FAILING
41              ;          SOURCE CHANNEL AND COMPARE AGAINST THE EXPECTED
42              ;          VALUE. THE MOST PROBABLE FAILING MODULES ARE 1)
43              ;          THE 1125A ADAPTER CARD (CHECK RESISTOR VALUES AND
44              ;          SWITCHES FIRST) 2) BAD CABLE AND/OR CONNECTORS.
45              ;          THE A/D MODULES AND ETCH ARE NOT LIKELY TO BE THE
46              ;          CAUSE OF THE FAILURE UNLESS A SHORT TO GROUND OR
47              ;          A POWER SUPPLY ETCH EXISTS SOMEWHERE.
48              ;
49              ;       3) NON-INDEPENDENT MUX OR SOURCE CHANNEL(S)
50              ;
51              ;          IF AN INTER-CONNECTION OR CROSSTALK EXISTS BETWEEN
52              ;          TWO OR MORE MUX CHANNNELS, DATA ERRORS SHOULD BE
53              ;          REPORTED ON THEM. THE PROBLEM WILL APPEAR AS
54              ;          IN PROBLEM # 1) ABOVE, EXCEPT THAT DATA ERRORS
55              ;          ARE REPORTED FROM TWO OR MORE CHANNELS (PROBABLY
56              ;          ADJACENT). IF TWO OR MORE SOURCE CHANNELS ARE
57              ;          CONNECTED, SEVERAL MUX CHANNELS WILL REPORT DATA
58              ;          ERRORS (SEE PROBLEM # 2) ABOVE). LOOK FOR ETCH
59              ;          SHORTS ON THE TEST ADAPTER AND THE A/D INTERFACE.
```

```
!0021 .MAIN
01                ;       4) A/D SUB-SYSTEM MODULE MALFUNCTION
02
03                ;          IF AN INTERNAL HARDWARE ERROR EXISTS IN ONE OR BOTH
04                ;          OF THE A/D MODULES, IT IS LIKELY THAT DATA ERRORS
05                ;          WILL APPEAR ON MOST OR ALL OF THE MUX CHANNELS.
06                ;          MODULE "M1" CONTAINS THE ANALOG MULTIPLEXER LINES,
07                ;          CHANNEL SELECT LOGIC, SINGLE-ENDED/DIFFERENTIAL MUX
08                ;          SELECT LOGIC, THE SAMPLE AND HOLD AND AN AMPLIFIER.
09                ;          MODULE "M2" CONTAINS THE A/D CONVERTER, A CLOCK
10                ;          AND CONTROL LOGIC. MAKE SURE THAT THE A/D MODULE
11                ;          ON-BOARD +/- 15 VOLT SUPPLY IS FUNCTIONING. IF
12                ;          IT IS O.K., THEN CHECK THE DATA ERROR INFORMATION.
13                ;          IF THE ERRORS ARE OCCURING IN BOTH SINGLE-ENDED
14                ;          AND DIFFERENTIAL MUX TYPE MODES, THE MOST PROBABLE
15                ;          FAILING MODULES ARE "M2" OR "M1". IF THE ERRORS
16                ;          ARE OCCURING IN ONLY ONE OF THE MULTIPLEXER MODES
17                ;          THEN EITHER THE MUX MODE SELECT LINE FROM "M2"
18                ;          OR MODULE "M1" SHOULD BE SUSPECTED. MAKE SURE
19                ;          THAT THE CONVERTER SUB-SYSTEM IS CALIBRATED
20                ;          (SEE PROBLEM # 5) BELOW).
21
22                ;       5) A/D CONVERTER SUB-SYSTEM NOT CALIBRATED
23
24                ;          IF DATA ERRORS ARE BEING REPORTED ON ONE OR MORE
25                ;          MUX CHANNELS, AND THE ACTUAL (RECEIVE) AVERAGES ARE
26                ;          CONSISTANTLY OFFSET ABOVE OR BELOW THE EXPECTED
27                ;          VALUES, THEN THE A/D CONVERTER MAY NOT BE PROPERLY
28                ;          CALIBRATED. SINCE THE ALLOWED DATA ERROR IS +/-
29                ;          5%, THE CONVERTER WOULD HAVE TO BE GROSSLY OUT
30                ;          OF CALIBRATION, AND THIS SHOULD AFFECT MOST OR ALL
31                ;          OF THE MUX CHANNELS. SEE SECTION 4 FOR CALIBRATION
32                ;          INFORMATION.
33
34                ;       6) POWER SUPPLY FLUCTUATIONS
35
36                ;          SPURIOUS OR INTERMITTENT DATA ERRORS MAY INDICATE
37                ;          A FAILURE IN THE A/D SUB-SYSTEM (STABILITY, NOISE)
38                ;          OR THERE MAY BE EXCESSIVE NOISE IN THE EXTERNAL
39                ;          VOLTAGE SOURCE BEING USE. ALSO, THE POWER SUPPLY
40                ;          VOLTAGE MAY DRIFT SLOWLY.
```

```
!0022 .MAIN
01                ;       THEORY OF OPERATION:
02
03                ;       THE 1125A ANALOG TEST ADAPTER AND ITS EXTERNAL VOLTAGE
04                ;       SOURCE ACT AS A VOLTAGE LADDER NETWORK. WHEN THE ADAP-
05                ;       TER IS PROPERLY CONFIGURED AND CONNECTED TO THE MUX
06                ;       (AND A/D) AND THE EXTERNAL VOLTAGE SOURCE (V.IN) IS
07                ;       APPLIED TO THE ADAPTER CARD, EACH MUX CHANNEL WILL
08                ;       SEE 1 OF 4 DIFFERENT VOLTAGES. THE MUX CHANNELS ARE
09                ;       CONNECTED TO THE ADAPTER SOURCE CHANNELS IN THE
10                ;       FOLLOWING SCHEME, ALONG WITH THE % OF V.IN THAT
11                ;       APPEARS AT THE SOURCE CHANNELS:
12
13                ;               SINGLE-ENDED MUX          DIFFERENTIAL MUX
14                ;               ----------------          ----------------
15                ;       ADAPTER MUX                       MUX
16                ;       CHANNEL CHANNELS    %V.IN         CHANNELS    %V.IN
17                ;       ------- --------    -----         --------    -----
18                ;       0       0,7,10,13   100.          0,7         30.
19                ;       1       1,4,11,14   90.           1,4         50.
20                ;       2       2,5,8,15    70.          2,5         -30.
21                ;       3       3,6,9,12    40.          3,6         -50.
22
23                ;       MUX TYPE = DIFFERENTIAL:
24                ;       # OF CHANNELS = 8.
25                ;       CONVERSION COUNT = 64.
26                ;       (8. CHANNELS X 8. SAMPLES EACH)
27                ;       IF UNIPOLAR A/D: NEGATIVE %
28                ;       CHANNELS WILL REPORT 0 VALUES.
29
30                ;       MUX TYPE = SINGLE-ENDED:
31                ;       # OF CHANNELS = 16.
32                ;       CONVERSION COUNT = 128.
33                ;       (16. CHANNELS X 8. SAMPLES EACH)
```

```
10023 .MAIN
01              ;       THE EXPECTED CENTER, MAXIMUM AND MINIMUM DATA
02              ;       VALUES FOR THE SOURCE CHANNELS ARE CALCULATED IN
03              ;       THE SUBROUTINE "CLADR" (CALL = JSR @ICLAD). THE
04              ;       ESTIMATED CENTER VALUE IS OBTAINED BY MULTIPLYING
05              ;       THE % OF V.IN, BY V.IN AND DIVIDING THE PRODUCT BY
06              ;       100. THIS IS THE EXPECTED CENTER VALUE. USING AN
07              ;       ALLOWED DATA ERROR = +/- 5% (THE MINIMUM ALLOWED DATA
08              ;       ERROR IS +/- 8 LSB'S), THE CENTER VALUE DEVIATION
09              ;       CAN BE CALCULATED. THE MAXIMUM EXPECTED VALUE IS
10              ;       THE CENTER + DEVIATION AND THE MINIMUM EXPECTED
11              ;       VALUE IS THE CENTER - DEVIATION. FINALLY, THESE
12              ;       VALUES ARE CONVERTED TO THEIR EQUIVALENT 12-BIT
13              ;       A/D DATA WHICH DEPENDS ON THE A/D RANGE, POLARITY
14              ;       AND CODING TYPE INFORMATION. THIS PROCEDURE IS
15              ;       DONE FOR ALL FOUR SOURCE CHANNELS. NEW VALUES
16              ;       ARE CALCULATED EVERY TIME THAT THE MUX TYPE UNDER
17              ;       TEST IS CHANGED. EACH MUX CHANNEL BEING TESTED IS
18              ;       IS CONNECTED TO ONE OF THE SOURCE CHANNELS AND
19              ;       THEREFORE USES THE EXPECTED CENTER, MAXIMUM AND
20              ;       MINIMUM VALUES FOR THE SOURCE CHANNEL THAT IT IS
21              ;       CONNECTED TO. THE MUX CHANNELS ARE SAMMPLED  8.
22              ;       TIMES EACH AND CHANNEL RECEIVE AVERAGES ARE FORMED FROM
23              ;       THEM. FOR EVERY CHANNEL SAMPLED, THE CHANNEL AVERAGE
24              ;       RECEIVED BY THE A/D MUST BE IN THE FOLLOWING RANGE:
25
26              ;       MIN EXPECTED < = CHANNEL AVERAGE < = MAX EXPECTED
27
28              ;       IF THE CHANNEL AVERAGE FALLS OUTSIDE OF THE ABOVE
29              ;       RANGE, A DATA ERROR HAS RESULTED.
30
31              ;       MISCELLANEOUS:
32
33              ;       THIS PROGRAM SHOULD BE RUN, WITHOUT ERROR, FOR 15 -
34              ;       30 MINUTES OR MORE. A TRUE "PASS" SITUATION WILL
35              ;       EXIST IF NO A/D FUNCTIONAL ERRORS ARE REPORTED
36              ;       (SECTION 10) AND NO MUX CHANNELS ARE REPORTING
37              ;       ANY DATA ERRORS. A LONGER TERM TEST IS DESIRABLE
38              ;       TO INSURE THAT THE INTERFACE STILL WORKS AFTER
39              ;       THE BOARD HAS COMPLETELY WARMED-UP, AND IS STABLE.
```

```
10024 .MAIN
01              ;7.2.2  PROGRAM DESCRIPTION: D/A TO A/D LOOP AROUND TEST
02              ;                            D/A TO A/D LOOP AROUND TEST
03              ;                            WITH DATA CHANNEL EXERCISER
04
05              ;       INTRODUCTION:
06
07              ;       THIS PROGRAM IS A SYSTEM TEST EXERCISER FOR THE 4223 A/D
08              ;       CONVERTER AND 4224 D/A CONVERTER INTERFACE BOARDS FOR
09              ;       MICRO NOVA COMPUTERS. IT IS A CLOSED LOOP ANALOG TEST
10              ;       THAT MANIPULATES AND TESTS THE VARIOUS ANALOG CONVERSION
11              ;       MODULES, CIRCUITS AND ANALOG PATHS ON THESE BOARDS.
12              ;       IN ADDITION, MOST LOGIC FUNCTIONS AND OPERATING MODES
13              ;       ARE CHECKED DURING THE ANALOG TESTING. THE LOOP CONSISTS
14              ;       OF THE D/A CONVERTER (2 ANALOG CHANNELS, "X" AND "Y",
15              ;       AND A DC LEVEL, Z-AXIS) LOOPED AROUND TO 16. INPUT
16              ;       MULTIPLEXER CHANNELS AND THE A/D CONVERTER VIA A MODEL
17              ;       1125A ANALOG VOLTAGE TEST ADAPTER.
18
19              ;       A PARTIAL LIST OF SECTIONS TESTED FOLLOWS:
20
21              ;       D/A CONVERTER: D/A ANALOG CHANNELS "X" AND "Y" INCLUDING
22              ;                      DATA HOLDING REGISTERS, CONVERTER MODULES,
23              ;                      UNITY GAIN OP-AMPS; Z-AXIS PULSE DC BASE
24              ;                      VOLTAGE (USED TO TEST MUX CHANNELS ON THE
25              ;                      A/D); ALL TRANSFER MODES (PIO/DCH) AND
26              ;                      TRIGGER SELECTS (STRT, IOPLS, DTA RDY AND
27              ;                      INTERNAL/EXTERNAL CLOCK); D/A STATUS
28              ;                      (DATA READY, LATE CONVERSION); INTERRUPTS;
29              ;                      D/A ALTERNATE; OTHER FUNCTIONS. NOT
30              ;                      TESTED ARE THE SCOPE CONTROL BITS (BITS
31              ;                      4-7 OF A DOA COMMAND).
32
33              ;       A/D CONVERTER: A/D CONVERTER SUB-SYSTEM (SAMPLE/HOLD AND
34              ;                      CONVERTER HYBRID MODULES) INCLUDING THE
35              ;                      16. ANALOG INPUT MULTIPLEXER CHANNELS AND
36              ;                      ASSOCIATED CIRCUITRY; ALL TRANSFER MODES
37              ;                      (PIO/DCH) & TRIGGER SELECTS (STRT, IOPLS
38              ;                      DCHI AND INTERNAL/EXTERNAL CLOCK); A/D
39              ;                      STATUS (EOC, CLOCK OVERRUN); INTERRUPTS;
40              ;                      MISC. FUNCTIONS. ALL ANALOG TESTS ARE
41              ;                      PERFORMED WITH SINGLE-ENDED MULTIPLEXER
42              ;                      MODE SELECTED.
43
44              ;       REQUIRED TEST HARDWARE:
45
46              ;       1) MODEL 1125A VOLTAGE ANALOG TEST ADAPTER
47              ;       2) CABLE: 4224 D/A CONVERTER TO 1125A ADAPTER;
48              ;                 PART # 005 - 12425; WIRE LIST # 008 - 2185
49              ;       3) CABLE: 1125A ADAPTER TO 4223 A/D CONVERTER;
50              ;                 PART # 005 - 12431; WIRE LIST # 008 - 2184
```

```
10025 .MAIN
01                ;       TEST PROCEDURES:
02                ;
03                ;       THE MICRO-NOVA CHASSIS SHOULD BE POWERED DOWN WHILE
04                ;       INSERTING OR MAKING ANY CONNECTIONS TO/FROM THE BOARDS.
05                ;       THE LOOP AROUND TEST IS SET UP AS FOLLOWS:
06                ;
07                ;       1) MAKE SURE THAT THE 4223 A/D INTERFACE AND 4224 D/A
08                ;          INTERFACE BOARDS ARE PROPERLY IN THE MICRO NOVA
09                ;          CHASSIS. IN ADDITION, THEIR RESPECTIVE DIAGNOSTIC
10                ;          PROGRAMS SHOULD SUCCESSFULLY RUN AND BOTH OF THE
11                ;          SUB-SYSTEMS MUST BE CALIBRATED (SEE SECTION 4).
12                ;          YOU WILL HAVE TO KNOW THE POLARITY/RANGE INFORMATION
13                ;          FOR BOTH CHANNELS OF THE D/A, "X" AND "Y", (THEY ARE
14                ;          GENERALLY THE SAME) AND THE A/D. YOU WILL ALSO NEED
15                ;          TO KNOW THE DATA CODING TYPE FOR THE "X" AND "Y"
16                ;          D/A CHANNELS. REFER TO SECTIONS 11.5 & 11.6 FOR RANGE
17                ;          POLARITY AND CODING INFORMATION. THE D/A MUST HAVE
18                ;          A JUMPER IN TO ALLOW Z-AXIS PULSE TRIGGERING (W22 OR
19                ;          W21) AND THE Z-AXIS OUTPUT MUST BE DC COUPLED BY
20                ;          INSERTING JUMPER W33. SEE SECTION 11.5.2 FOR MORE INFO.
21                ;       2) DISCONNECT ANY EXTERNAL VOLTAGE SOURCE FROM THE
22                ;          "V+" AND "RET" TERMINALS OF THE ADAPTER CARD.
23                ;       3) TAKE THE D/A TO ADAPTER CABLE (ITEM 2) IN REQUIRED
24                ;          HARDWARE) AND CONNECT ONE END TO THE KEYED I/O
25                ;          CONNECTOR OF THE D/A AND THE OTHER TO THE "D/A"
26                ;          CONNECTOR (J1) ON THE TEST ADAPTER. THEY WILL ONLY
27                ;          FIT ONE WAY.
28                ;       4) TAKE THE ADPATER TO A/D CABLE (ITEM 3) IN REQUIRED
29                ;          HARDWARE) AND CONNECT ONE END TO THE KEYED I/O
30                ;          CONNECTOR OF THE A/D AND THE OTHER TO THE "MUX"
31                ;          CONNECTOR (J2) ON THE TEST ADAPTER. AGAIN, THEY WILL
32                ;          ONLY FIT ONE WAY.
33                ;       5) SET THE SWITCHES ON THE 1125A ADAPTER AS FOLLOWS:
34                ;          SWITCHES 1 - 8 = OFF.
35                ;       6) POWER UP THE MICRO NOVA CHASSIS.
36                ;       7) LOAD THE EXERCISER, SELECT AND INITIALIZE THE "D/A
37                ;          TO A/D LOOP AROUND TEST". SEE SECTION 9.1 FOR LOAD-
38                ;          ING AND INITIALIZATION INFORMATION.
39                ;
40                ;       TEST OPERATION:
41                ;
42                ;       AFTER THE PROGRAM IS STARTED AND INITIALIZED, A TABLE
43                ;       OF VOLTAGE RANGES TESTED FOR THE D/A CHANNELS AND A/D
44                ;       IS PRINTED AS FOLLOWS:
45                ;
46                ;       LOOP TEST VOLTAGE RANGES (SINGLE-ENDED MUX):
47                ;       ------- D/A -------      --- A/D ---
48                ;       CHANNEL MAX     MIN     MAX     MIX
49                ;       X       XXXX    YYYY    XXXX    YYYY
50                ;       Y       XXXX    YYYY    XXXX    YYYY
51                ;
52                ;       WHERE:  XXXX = MAXIMUM VOLTAGE TESTED FOR D/A OR A/D
53                ;               YYYY = MINIMUM VOLTAGE TESTED FOR D/A OR A/D
54                ;                      (0 FOR UNIPOLAR TEST, NEGATIVE FOR
55                ;                       BIPOLAR TEST)
56                ;       ALL VALUES ARE IN SIGNED, DECIMAL MILLIVOLTS.
```

```
10026 .MAIN
01                ;       ALTHOUGH THERE IS NO RESTRICTION ON THE A/D CONVERTER
02                ;       OR THE "X" AND "Y" D/A CONVERTER'S RANGE AND POLARITY,
03                ;       THEY SHOULD BE THE SAME IF FULL RANGE ANALOG TESTING
04                ;       IS DESIRED. FOR EXAMPLE, YOU SHOULD LOOP A +/- 5 VOLT
05                ;       D/A (BOTH CHANNELS) TO A +/- 5 VOLT A/D CONVERTER.
06                ;       SEE THEORY OF OPERATION SECTION FOR A DESCRIPTION ON
07                ;       HOW THE TEST RANGES ARE DETERMINED.
08                ;
09                ;       AFTER THE ABOVE TABLE IS PRINTED, THE PROGRAM WILL
10                ;       ATTEMPT TO CORRECTLY ESTABLISH (READ) THE Z-AXIS
11                ;       BASE LEVEL VOLTAGE (DC), BY SAMPLING MUX CHANNEL 3
12                ;       IN SINGLE-ENDED MUX MODE. IT THEN PRINTS THIS VALUE
13                ;       TO THE OPERATOR AS FOLLOWS:
14                ;
15                ;       Z-AXIS BASE LEVEL VOLTAGE = (X) MV
16                ;
17                ;       (THE VALUE PRINTED (X) IS SIGNED DECIMAL MILLIVOLTS).
18                ;       THE Z-AXIS LEVEL CAN BE ANYWHERE IN ITS ADJUSTMENT
19                ;       RANGE (NOMINALLY +/- 5 VOLTS). NO SPECIFIC VALUE IS
20                ;       EXPECTED, AS THE PROGRAM USES IT ONLY FOR MUX CHANNEL
21                ;       INDEPENDENCE TESTING. HOWEVER, FOR THE MOST EFFECTIVE
22                ;       TESTING, THE Z-AXIS LEVEL SHOULD BE ADJUSTED TO A
23                ;       LEVEL IN THE RANGE OF +/- 2 TO 3 VOLTS. SEE SECTION
24                ;       11.5.2 FOR ADJUSTMENT INFORMATION. ALSO, THE PROGRAM
25                ;       ASSUMES THAT THE A/D PERFORMS CONVERSIONS PROPERLY,
26                ;       AND THAT THE Z-AXIS LEVEL READ IS CORRECT. IF IT
27                ;       IS NOT, DATA ERRORS WILL OCCUR ON OTHER CHANNELS
28                ;       CONNECTED TO THE Z-AXIS OUTPUT. THIS WILL BE DESCRIBED
29                ;       LATER.
30                ;
31                ;       NEXT, THE TEST PARAMETERS, A/D CONVERTER AND D/A
32                ;       CONVERTER ARE INITIALIZED AND THE TEST IS STARTED.
33                ;       INITIAL TEST PARAMETERS ARE:
34                ;
35                ;       - A/D MODE = D/A MODE = PIO
36                ;       - A/D TRIGGERING = D/A TRIGGERING = STRT PUSE, NO SYNC
37                ;       - MUX TYPE = SINGLE-ENDED (16. CHANNELS)
38                ;
39                ;       THE ANALOG SECTIONS ARE TESTED BY SENDING DIFFERENT
40                ;       DATA PATTERNS TO THE D/A CONVERTER CHANNELS, WHICH
41                ;       ARE CONVERTED TO ANALOG VOLTAGES IN THE LOOPS FORMED
42                ;       BY THE TEST ADAPTER AND CABLES (ALONG WITH THE Z-AXIS
43                ;       VOLTAGE). THESE VOLTAGES ARE RECEIVED BY THE MUX INPUT
44                ;       CHANNELS AND CAN BE SELECTIVELY READ BY THE A/D
45                ;       CONVERTER WHICH CONVERTS THEM BACK TO DIGITAL DATA.
46                ;       THE A/D CONVERTER SCANS THE 16 MUX CHANNELS 8 TIMES
47                ;       EACH (128. SAMPLES) AFTER THE DATA IS SENT TO THE D/A
48                ;       CHANNELS. THE MUX CHANNEL RECEIVE (ACTUAL) AVERAGES
49                ;       ARE CALCULATED FROM THE SAMPLES TAKEN. THEN THE
50                ;       EXPECTED CENTER, MAXIMUM AND MINIMUM RECEIVE DATA
51                ;       VALUES ARE CALCULATED. THE CALCULATIONS DEPEND ON
52                ;       THE DATA SENT TO THE D/A CHANNELS, ALONG WITH THE RANGE,
53                ;       POLARITY AND CODING INFORMATION OF THE A/D AND D/A.
54                ;       FINALLY, THE MUX CHANNEL RECEIVE AVERAGES ARE COMPARED
55                ;       AGAINST THE MAXIMUM AND MINIMUM DATA VALUES EXPECTED
56                ;       FROM THEM. A DATA ERROR (SEE ERROR DESCRIPTIONS) IS
57                ;       REPORTED FOR ANY AND ALL CHANNELS WHOSE RECEIVE AVERAGES
58                ;       ARE NOT WITHIN THE EXPECTED RANGE. IF THE RECEIVE
```

```
01              ;       AVERAGE IS WITHIN THE EXPECTED RANGE FOR A PARTICULAR
02              ;       MUX CHANNEL, THEN THE TRANSFER COUNT FOR THAT CHANNEL
03              ;       IS INCREMENTED (ONCE FOR EACH SUCCESSFUL TEST). IF THE
04              ;       RECEIVE AVERAGE IS NOT WITHIN THE EXPECTED RANGE, THEN
05              ;       BOTH TRANSFER AND ERROR COUNTS ARE INCREMENTED FOR THE
06              ;       MUX CHANNEL IN ERROR. THIS TABULATED INFORMATION CAN
07              ;       BE PRINTED AT ANY TIME BY HITTING THE "SPACE" BAR ON
08              ;       THE TTY CONSOLE (SEE SECTION 10). AFTER ALL CHANNELS
09              ;       HAVE BEEN SCANNED, AVERAGED AND CHECKED, AND IF THE
10              ;       PROGRAM IS NOT LOOPING ON A DETECTED ERROR, THE TEST
11              ;       PARAMETERS WILL BE CHANGED TO THE NEXT TEST STATE, AND
12              ;       THE MUX CHANNELS WILL BE TESTED AGAIN. THE SEQUENCE
13              ;       OF A/D, MUX AND D/A PARAMETERS TESTED ARE AS FOLLOWS:
14              ;
15              ;       ------ A/D ------        ---------- D/A ----------
16              ;       MODE    TRIGGERING      MODE    TRIGGERING  SCOPE MODE
17              ;       ----    ----------      ----    ----------  ----------
18              ;       PIO     STRT            PIO     STRT            ON
19              ;       PIO     INT CLK         DCH     IOPLS           OFF
20              ;       PIO     EXT CLK         DCH     DTA RDY         OFF
21              ;       DCH     IOPLS           DCH     INT CLK         OFF
22              ;       DCH     DCHI            DCH     EXT CLK         OFF
23              ;       DCH     INT CLK         (REPEAT ABOVE SEQUENCE)
24              ;       DCH     EXT CLK
25              ;       (REPEAT ABOVE SEQUENCE)
26              ;
27              ;       WHERE: DIFF. = DIFFERENTIAL
28              ;              S.E. = SINGLE-ENDED
29              ;              PIO = PROGRAMMED INPUT/OUTPUT (I/O)
30              ;              DCH = DATA CHANNEL
31              ;              INT/EXT CLK = INTERNAL/EXTERNAL CLOCK SYNC
32              ;              STRT = START PULSE (I.E. "NIOS" INSTRUCTION)
33              ;              IOPLS = I/O PULSE (I.E. "NIOP" INSTRUCTION)
34              ;              DCHI = DATA CHANNEL INPUT (A CONTROL SIGNAL)
35              ;              DTA RDY = DATA READY (FROM DCHO CONTROL SIGNAL)
36              ;
37              ;       AFTER ALL OF THE ABOVE MODES ARE TESTED, THE SEQUENCE
38              ;       STARTS OVER AGAIN AND WILL CONTINUE UNTIL OPERATOR
39              ;       TERMINATED. IF ANY ERRORS EXIST, THIS PROGRAM CAN BE
40              ;       USED TO DETECT AND TRACE THE CAUSE OF THE ERROR(S).
41              ;       THIS IS EXPLAINED IN THE FOLLOWING SECTION. REFER TO
42              ;       SECTION 10 FOR INFORMATION ON SPECIAL PROGRAM FEATURES
43              ;       SUCH AS TEST PARAMETER SUMMARY AND ERROR SUMMARY
44              ;       REPORTS. THEY WILL BE HELPFUL DURING PROGRAM OPERATION.
45              ;
46              ;       THE PROGRAM WILL PRINT "END OF PASS # (#)" EACH TIME
47              ;       ALL A/D AND D/A MODES HAVE BEEN TESTED IF THE PROGRAM
48              ;       IS NOT LOOPING ON AN ERROR. THIS IS ONLY AN INDICATION
49              ;       THAT THE PROGRAM HAS COMPLETED THE ABOVE MODE/TRIGGER
50              ;       SELECTION SEQUENCE AND GIVES AN INDICATION TO THE
51              ;       OPERATOR THAT THE PROGRAM IS RUNNING. IT DOES NOT
52              ;       INDICATE THAT THE BOARDS HAVE "PASSED" ANY TEST.
```



```
01              ;       ERROR DESCRIPTIONS:
02              ;
03              ;       THERE ARE TWO CATAGORIES OR CLASSES OF ERRORS THAT
04              ;       ARE DETECTED AND REPORTED. THE FIRST ARE A/D AND D/A
05              ;       FUNCTIONAL ERRORS AND ARE ASSOCIATED WITH FAILURES
06              ;       IN THE A/D - D/A LOGIC AND CONTROL FUNCTIONS (I.E. IN
07              ;       CONVERSION TRIGGERING, DATA TRANSFER MODES (PIO, DCH)
08              ;       STATUS INFORMATION ETC.). A/D ERRORS ARE DETECTED
09              ;       AND REPORTED FROM THE A/D DRIVER ROUTINE "SCAN". D/A
10              ;       ERRORS ARE DETECTED AND REPORTED FROM THE D/A DRIVER
11              ;       ROUTINE "SEND". SEE SECTION 10 FOR INFORMATION REGARD-
12              ;       ING THESE ERRORS. IF THEY OCCUR, RUN THE APPROPRIATE
13              ;       INTERFACE DIAGNOSTIC PROGRAM TO FURTHER ISOLATE THE
14              ;       FUNCTIONAL FAILURE(S) (SEE SECTION 4).
15              ;
16              ;       THE SECOND CLASS OF ERRORS DETECTED AND REPORTED ARE
17              ;       DATA ERRORS. THESE FAILURES, IF THEY OCCUR, INDICATE
18              ;       A MALFUNCTION IN THE ANALOG SECTIONS OF THE A/D, D/A
19              ;       OR IN THE TEST HARDWARE (ADAPTER, CABLES, CONNECTORS).
20              ;
21              ;       IF A RECEIVE AVERAGE FROM A MUX CHANNEL THAT IS CONNECT-
22              ;       ED TO EITHER THE "X" OR "Y" D/A CHANNELS IS NOT WITHIN
23              ;       ITS EXPECTED RANGE AND "SWREG" SWITCH D = 0 (SECTION 8),
24              ;       THE FOLLOWING ERROR IS REPORTED:
25              ;
26              ;       *** DATA ERROR ***
27              ;       DETECTED IN ROUTINE "CHECK" CALLED AT: (OCTAL ADDRESS)
28              ;       D/A CHANNEL = (D)
29              ;       MUX CHANNEL = (M)
30              ;       D/A     A/D     A/D
31              ;       SEND    RECEIVE EXPECTED
32              ;       SSSSSS  RRRRRR  EEEEEE
33              ;
34              ;       WHERE:  (D) = D/A SOURCE CHANNEL "X" OR "Y"
35              ;               (M) = MUX CHANNEL # (DECIMAL)
36              ;                     (0 - 15 FOR SINGLE-ENDED MUX TYPE ONLY)
37              ;               SSSSSS = DATA SENT TO THE D/A CHANNEL (D)
38              ;               RRRRRR = ACTUAL RECEIVE AVERAGE FROM MUX CHANNEL
39              ;                        (M) = ERROR VALUE
40              ;               EEEEEE = EXPECTED CENTER VALUE FOR MUX CHANNEL
41              ;                        (M) = CORRECT VALUE
42              ;               (OCTAL ADDRESS) = THE ADDRESS IN THE PROGRAM
43              ;                                 LISTING WHERE THE "CHECK"
44              ;                                 SUBROUTINE IS CALLED FROM.
45              ;                                 TELLS OPERATOR WHICH DATA
46              ;                                 TEST FAILED.
47              ;
48              ;               DATA VALUES (SSSSSS, RRRRRR, EEEEEE) ARE
49              ;               AS FOLLOWS:
50              ;               - SWITCH C = 0  DATA IS 12-BIT OCTAL DATA,
51              ;                               LEFT-JUSTIFIED, UNUSED BITS = 0
52              ;               - SWITCH C = 1  VALUE IS THE SIGNED, DECIMAL
53              ;                               MILLIVOLT EQUIVALENT OF THE
54              ;                               THE OCTAL DATA FOR A/D OR D/A.
55              ;
56              ;       IF A RECEIVE AVERAGE FROM A MUX CHANNEL THAT IS CONNECT-
57              ;       ED TO THE Z-AXIS VOLTAGE OUTPUT CHANNEL IS NOT WITHIN
58              ;       ITS EXPECTED RANGE AND "SWREG" SWITCH D = 0 (SECTION 8),
59              ;       THE FOLLOWING ERROR IS REPORTED:
```

```
10029 .MAIN
01              ;       *** DATA ERROR ***
02              ;       DETECTED IN ROUTINE "CHECK" CALLED AT: (OCTAL ADDRESS)
03              ;       Z-AXIS VOLTAGE LEVEL INCONSISTENCY
04              ;       MUX     Z-AXIS DC
05              ;       CHANNEL VOLTAGE (MV)
06              ;       ======= ===========
07              ;       3.      MMMM
08              ;       6.      MMMM
09              ;       9.      MMMM
10              ;       12.     MMMM
11              ;       EXPECTED Z-AXIS DC LEVEL IS: (ZZZZ)     MV
12              ;
13              ;       WHERE: MMMM AND ZZZZ ARE SIGNED, DECIMAL MILLIVOLTS.
14              ;
15              ;       DATA ERROR REPORTS ARE SUPPRESSED BY SETTING SWITCH
16              ;       D = 1 (SEE SECTION 8 FOR SWITCH INFORMATION).
17              ;
18              ;       ERROR HANDLING AND INTERPRETATION OF ERROR INFORMATION:
19              ;
20              ;       IF DATA ERRORS ARE OCCURING, THE FIRST THING TO
21              ;       CHECK IS THE TEST HARDWARE SET-UP. MAKE SURE THAT
22              ;       THE CONNECTOR PINS ARE NOT BROKEN OR MISSING, THAT
23              ;       THE CABLES ARE CONNECTED PROPERLY AND THAT THE ADAPTER
24              ;       SWITCHES ARE CORRECTLY SET. IF EVERYTHING APPEARS TO
25              ;       BE IN ORDER, THEN ONE OR MORE MUX CHANNELS, THE D/A
26              ;       CONVERTER (WHICH CONSISTS OF THE "X" AND "Y" CHANNELS
27              ;       AS WELL AS THE Z-AXIS OUTPUT) OR THE A/D CONVERTER
28              ;       MODULES AND CIRCUITRY MAY BE FAILING. IN THIS CASE,
29              ;       USE THE TEST DATA TO DETERMINE WHAT IS CAUSING THE
30              ;       DATA ERRORS. INSURE THAT THE TEST WAS PROPERLY
31              ;       INITIALIZED, AS DATA ERRORS WILL BE REPORTED IF
32              ;       MISTAKES ARE MADE IN THE INITIALIZATION SEQUENCE.
33              ;
34              ;       IF DATA ERRORS STILL EXIST AFTER CHECKING THE
35              ;       ABOVE ITEMS, AN ERROR EXISTS SOMEWHERE IN THE ANALOG
36              ;       SECTIONS OF THE A/D OR D/A INTERFACES, OR IN THE TEST
37              ;       ADAPTER. THE AREA OF FAILURE CAN BE DETERMINED BY
38              ;       ANALYSIS OF THE INFORMATION CONTAINED IN THE DATA
39              ;       ERROR MESSAGES (SEE ABOVE) AND BY THE TRANSFER/ERROR
40              ;       SUMMARY REPORT. IF AND WHEN DATA ERRORS OCCUR DO THE
41              ;       FOLLOWING:
42              ;
43              ;       1) IF POSSIBLE, OBTAIN A HARD-COPY OF THE DATA ERRORS
44              ;          BEING REPORTED (I.E. OUTPUT TO A LINE PRINTER OR
45              ;          PRINTING TERMINAL). OTHERWISE MAKE A NOTE OF THE
46              ;          PERTINENT ERROR INFORMATION INCLUDING D/A CHANNEL,
47              ;          MUX CHANNEL, SEND, EXPECTED AND RECEIVED DATA ETC.
48              ;          VALUES. DO THIS FOR ALL FAILING MUX CHANNELS.
49              ;       2) SELECT "LOOP ON ERROR" (SWITCH 1 = 0) WHICH IS
50              ;          THE DEFAULT CONDITION. THIS WILL FREEZE THE TEST
51              ;          PARAMETERS. IT WILL ALSO CYCLE ON THE FAILING DATA
52              ;          TEST AND FREEZE THE TEST DATA WHEREVER APPLICABLE.
53              ;       3) SUPPRESS DATA ERROR REPORTS (SWITCH D = 1) AND
54              ;          OBTAIN A TRANSFER/ERROR SUMMARY REPORT AFTER A
55              ;          FEW MINUTES OF PROGRAM OPERATION (3 - 5 MINUTES).
56              ;          (SEE SECTION 10 FOR MORE INFORMATION). AGAIN, A
57              ;          HARD-COPY IS PREFERABLE.
```

```
10030 .MAIN
01              ;       4) IF A/D - D/A OPERATING MODES ARE SUSPECTED AS A CAUSE
02              ;          OF THE DATA ERRORS, A TEST PARAMETER SUMMARY REPORT
03              ;          CAN BE OBTAINED BY TYPING CNTRL-S (SEE SECTION 10).
04              ;
05              ;       FROM THE INFORMATION RECEIVED FROM THESE STEPS, YOU
06              ;       ARE READY TO MAKE AN ANALYSIS. THE FOLLOWING IS SOME
07              ;       HELPFUL INFORMATION REGARDING POSSIBLE FAILURES.
08              ;
09              ;       POSSIBLE FAILURES INCLUDE:
10              ;
11              ;       1) BAD MUX CHANNEL(S)
12              ;       2) D/A MODULE FAILURE(S) ("X" AND/OR "Y" CONVERTERS)
13              ;       3) NON-INDEPENDENT MUX OR D/A CHANNELS (CROSSTALK)
14              ;       4) A/D MODULE FAILURE (SAMPLE/HOLD, A/D CONVERTER ETC.)
15              ;       5) NON-CALIBRATED D/A SUB-SYSTEM ("X" AND/OR "Y")
16              ;       6) NON-CALIBRATED A/D SUB-SYSTEM.
17              ;       7) INCONSISTENT Z-AXIS DC LEVEL (INCLUDING NOISE)
18              ;
19              ;       MORE DETAILED INFORMATION ABOUT THE ABOVE POSSIBLE
20              ;       FAILURES FOLLOWS.
21              ;
22              ;       *** IMPORTANT NOTE ***
23              ;
24              ;       IF USING AN OSCILLOSCOPE OR VOLTMETER/MULTIMETER,
25              ;       ALL MEASUREMENTS MADE ON THE INTERFACES MUST BE DONE
26              ;       VERY CAREFULLY TO INSURE THAT NO OTHER DAMAGE IS CAUSED
27              ;       BY SHORTING SIGNALS TOGETHER. THE INTERFACES SHOULD BE
28              ;       ON EXTENDER CARDS FOR EASIER ACCESS TO THE BOARDS.
29              ;
30              ;       ALSO, IT IS IMPORTANT TO ELIMINATE THE ADAPTER CARD
31              ;       (CONNECTOR, ETCH, RESISTORS AND SWITCHES) AND THE
32              ;       CABLES (ESPECIALLY THE CONNECTORS) AS THE POSSIBLE
33              ;       SOURCES OF FAILURE BEFORE AN ATTEMPT IS MADE TO
34              ;       REPLACE ANY INTERFACE CONVERTER SUB-SYSTEM MODULES.
35              ;       CHECK THE ADAPTER FOR SHORTED, OPEN OR OTHERWISE
36              ;       FAULTY ETCHES AND CONNECTIONS. A/D AND/OR D/A MODULES
37              ;       SHOULD BE SUSPECTED ONLY AFTER ALL OTHER POSSIBILITIES
38              ;       HAVE BEEN ELIMINATED.
```

```
10031 .MAIN
01                ;       DETAILED FAILURE ANALYSIS:
02
03                ;       1) BAD MUX CHANNEL(S)
04
05                ;          THIS IS ONE OF THE MOST COMMON ANALOG SECTION
06                ;          FAILURES. DATA ERRORS WILL BE REPORTED ON ONE OR
07                ;          MORE MUX CHANNELS, NOT NECESSARILY CONNECTED TO THE
08                ;          SAME D/A OR Z-AXIS CHANNEL. IT USUALLY INDICATES
09                ;          A FAILURE (OPEN, SHORTED OR INTERMITTENT) IN THE
10                ;          A/D SUB-SYSTEM MODULE THAT CONTAINS THE ANALOG
11                ;          MULTIPLEXER (M1), OR THE ETCH RUNS CONNECTING
12                ;          THE I/O EDGE PINS AND THE MODULE INPUTS.
13
14                ;          IF A MUX CHANNEL IS OPEN, THE DATA RETURNED
15                ;          SHOULD INDICATE A FLOATING CHANNEL (GENERALLY,
16                ;          BUT NOT NECESSARILY IN THE RANGE OF 1 TO 2
17                ;          VOLTS). 0 VOLTS SHOULD BE RETURNED IF A CHANNEL
18                ;          IS SHORTED TO GROUND. IT COULD ALSO BE SHORTED
19                ;          TO THE ON-BOARD A/D +/- 15 VOLT SUPPLY, TO THE
20                ;          BOARD +5 V ETC. IT IS POSSIBLE TO CHECK THE
21                ;          VOLTAGE LEVEL AT THE SUSPECTED FAILING MUX INPUT
22                ;          WITH A VOLTMETER AND COMPARING IT TO THE EXPECTED
23                ;          RECEIVE VALUE FROM THE DATA ERROR REPORT. (IF
24                ;          SWITCH C = 1, THE ERROR DATA WILL BE PRINTED IN
25                ;          DECIMAL MILLIVOLTS.) IF THE ETCH RUNS ARE O.K.
26                ;          (NO OPEN, SHORTS, COLD-SOLDER JOINTS ETC. EXIST),
27                ;          THEN THE A/D MODULES (M1 FIRST, M2 SECOND) ARE
28                ;          THE PROBABLE FAILING MODULES.
29
30                ;       2) "X", "Y" D/A SUB-SYSTEM MODULE FAILURE
31
32                ;          IF A D/A CONVERTER MODULE FAILS TO PROPERLY CONVERT
33                ;          THE DIGITAL DATA WORD TO ITS EQUIVALENT VOLTAGE OUT-
34                ;          OUTPUT, THEN DATA ERRORS SHOULD BE REPORTED FROM ALL
35                ;          MUX CHANNELS CONNECTED TO IT. SEE THE THEORY OF
36                ;          OPERATION SECTION FOR THE CONNECTION SCHEME BETWEEN
37                ;          D/A AND MUX CHANNELS. THIS INFORMATION CAN ALSO BE
38                ;          OBTAINED FROM THE PROGRAM BY TYPING A CNTRL-C.
39                ;          MEASURE THE VALUE PRESENT AT THE SUSPECTED FAILING
40                ;          D/A CHANNEL OUTPUT AND COMPARE AGAINST THE EXPECTED
41                ;          VALUE. IF THE ADAPTER AND CONNECTING CABLES HAVE
42                ;          BEEN ELIMINATED AS POSSIBLE ERROR SOURCES, THEN THE
43                ;          D/A CONVERTER IS THE MOST PROBABLE FAILING MODULE.
44                ;          MAKE SURE THAT THE D/A CONVERTER +/- 15 VOLT SUPPLY
45                ;          VOLTAGE IS WITHIN ACCEPTED LIMITS OF OPERATION.
46                ;          THE A/D MODULES AND ETCH ARE NOT LIKELY TO BE THE
47                ;          CAUSE OF THE FAILURE UNLESS A SHORT TO GROUND OR
48                ;          A POWER SUPPLY ETCH EXISTS SOMEWHERE.
49
50                ;       3) NON-INDEPENDENT MUX OR CHANNEL(S)
51
52                ;          IF AN INTER-CONNECTION OR CROSSTALK EXISTS BETWEEN
53                ;          TWO OR MORE MUX CHANNNELS, DATA ERRORS SHOULD BE
54                ;          REPORTED ON THEM. THE PROBLEM WILL APPEAR AS
55                ;          IN PROBLEM # 1) ABOVE, EXCEPT THAT DATA ERRORS
56                ;          ARE REPORTED FROM TWO OR MORE CHANNELS (PROBABLY
57                ;          ADJACENT). IF BOTH D/A CONVERTER-CHANNEL OUTPUTS
58                ;          ARE INTER-CONNECTED THEN SEVERAL OR ALL MUX CHANNELS
59                ;          SHOULD REPORT DATA ERRORS. LOOK FOR ETCH SHORTS ON
60                ;          THE TEST ADAPTER AND THE D/A (AND A/D) INTERFACES.
```

```
 0032 .MAIN
01                ;       4) A/D SUB-SYSTEM MODULE MALFUNCTION
02
03                ;          IF AN INTERNAL HARDWARE ERROR EXISTS IN ONE OR BOTH
04                ;          OF THE A/D MODULES, IT IS LIKELY THAT DATA ERRORS
05                ;          WILL APPEAR ON MOST OR ALL OF THE MUX CHANNELS.
06                ;          MODULE "M1" CONTAINS THE ANALOG MULTIPLEXER LINES,
07                ;          CHANNEL SELECT LOGIC, SINGLE-ENDED/DIFFERENTIAL MUX
08                ;          SELECT LOGIC, THE SAMPLE AND HOLD AND AN AMPLIFIER.
09                ;          MODULE "M2" CONTAINS THE A/D CONVERTER, A CLOCK
10                ;          AND CONTROL LOGIC. MAKE SURE THAT THE A/D MODULE
11                ;          ON-BOARD +/- 15 VOLT SUPPLY IS FUNCTIONING. IF
12                ;          IT IS O.K., THEN CHECK THE DATA ERROR INFORMATION.
13                ;          IF THE ERRORS ARE OCCURING IN BOTH SINGLE-ENDED
14                ;          AND DIFFERENTIAL MUX TYPE MODES, THE MOST PROBABLE
15                ;          FAILING MODULES ARE "M2" AND "M1". IF THE ERRORS
16                ;          ARE OCCURING IN ONLY ONE OF THE MULTIPLEXER MODES
17                ;          THEN EITHER THE MUX MODE SELECT LINE FROM "M2"
18                ;          OR MODULE "M1" SHOULD BE SUSPECTED. MAKE SURE
19                ;          THAT THE CONVERTER SUB-SYSTEM IS CALIBRATED
20                ;          (SEE PROBLEM # 6) BELOW).
21
22                ;       5) "X", "Y" D/A CONVERTER SUB-SYSTEM NOT CALIBRATED
23
24                ;          IF DATA ERRORS ARE BEING REPORTED ON ONE OR MORE
25                ;          MUX CHANNELS CONNECTED TO A D/A CHANNEL AND THE
26                ;          ACTUAL (RECEIVE) AVERAGES ARE CONSISTANTLY OFFSET
27                ;          ABOVE OR BELOW THE EXPECTED VALUES, THEN THE D/A
28                ;          CONVERTER (FAILING) MAY NOT BE PROPERLY CALIBRATED.
29                ;          THE CONVERTER WOULD HAVE TO BE OFFSET BY MORE THAN
30                ;          5 LSB'S IN ORDER FOR THIS ERROR TO OCCUR. SEE
31                ;          SECTION 4 FOR CALIBRATION INFORMATION.
32
33                ;       6) A/D CONVERTER SUB-SYSTEM NOT CALIBRATED
34
35                ;          IF DATA ERRORS ARE BEING REPORTED ON ONE OR MORE
36                ;          MUX CHANNELS, AND THE ACTUAL (RECEIVE) AVERAGES
37                ;          APPEAR TO BE OFFSET ABOVE OR BELOW THE EXPECTED
38                ;          VALUES, THEN THE A/D CONVERTER MAY NOT BE PROPERLY
39                ;          CALIBRATED. THE CONVERTER HAS TO BE OFFSET BY MORE
40                ;          THAN 5 LSB'S SINCE THIS IS THE +/- ALLOWED DATA
41                ;          ERROR. IF IT IS INCORRECTLY CALIBRATED, MOST MUX
42                ;          CHANNELS (IF NOT ALL) SHOULD BE AFFECTED. SEE
43                ;          SECTION 4 FOR MORE INFORMATION.
```

7) Z-AXIS LEVEL INCONSISTENCY

AS PREVIOUSLY MENTIONED, THE Z-AXIS DC BASE LEVEL VOLTAGE IS READ FROM MUX CHANNEL 3 AT THE BEGINING OF THE PROGRAM. IT ASSUMES THAT THE VOLTAGE IT READS FROM THIS CHANNEL WILL BE PRESENT AT THE OTHER 3 MUX CHANNELS (6,9,12) THAT IT IS CONNECTED TO. IF, DURING "X" AND "Y" D/A CHANNEL TESTING, A VALUE IS READ FROM A MUX CHANNEL CONNECTED TO THE Z-AXIS OUTPUT AND IS MORE THAN +/- 100 MILLIVOLTS FROM THE THE INITIAL READING, THEN A Z-AXIS INCONSISTENCY ERROR IS REPORTED. ALL 4 CHANNELS AND THEIR RESPECTIVE RECEIVE VALUES ARE PRINTED (IN MILLIVOLTS) TO ASSIST THE OPERATOR IN DETERMINING THE PROBLEM. IF CHANNELS 6, 9 & 12 ARE THE SAME AND CHANNEL 3'S VALUE IS DIFFERENT, THEN CHANNEL 3 IS PROBABLY BAD. IF THE ARE ALL THE SAME, BUT DIFFERENT THAN THE INITIAL VALUE READ, THEN THE Z-AXIS LEVEL MAY HAVE DRIFTED, OR THERE MAY BE EXCESSIVE NOISE PRESENT. IF ONLY ONE CHANNEL IS DIFFERENT, THAT MUX CHANNEL MUST BE SUSPECTED AS THE SOURCE OF ERROR. NOTE THAT THE ALLOWED DATA ERROR IS DOUBLE THAT OF THE D/A CHANNELS BECAUSE OF ADDED NOISE PRESENT AT THE Z-AXIS OUTPUT. NO SPECIFIC VALUE IS EXPECTED FROM Z-AXIS, BUT FOR BEST MUX CHANNEL INDEPENDENCE TESING, IT SHOULD BE ADJUSTED TO 2 OR 3 VOLTS. IF ERRORS OF THIS TYPE OCCUR, FIRST INSURE THAT JUMPER W33 IS INSERTED FOR Z-AXIS DC COUPLING.

NOTE: THIS SIGNAL TENDS TO HAVE A SUBSTANTIAL AMOUNT OF NOISE (UP TO 200 MV TOTAL RIPPLE). THIS IS DUE TO THE FACT THAT THE OPERATIONAL AMPLIFIER IS BEING DRIVEN BY A TTL OUTPUT. THIS IS NOT HIGH ENOUGH TO AFFECT THE INTENSITY CONTROL (Z-AXIS) ON A SCOPE. A TYPICAL INPUT RANGE FOR THIS SIGNAL ON A STORGAE SCOPE IS +/- 10 VDC OR MORE.

THEORY OF OPERATION:

THIS SECTION CONTAINS DETAILED DESCRIPTIONS OF VARIOUS ASPECTS OF THE LOOP AROUND TEST.

THE 1125A VOLTAGE TEST ADAPTER AND CABLES, WHEN USED IN LOOP AROUND MODE, CONNECT THE "X" & "Y" D/A CHANNELS AND Z-AXIS AMPLIFIER (VOLTAGE) OUTPUTS TO THE A/D CONVERTER VIA THE 16 SINGLE-ENDED MODE CHANNELS OF THE ANALOG MULTIPLEXER. WHEN THE TEST ADAPTER IS PROPERLY SET AND CONNECTED BETWEEN THE D/A AND A/D (VIA THE MUX CHANNELS) 16 INDIVIDUAL ANALOG LOOPS ARE FORMED. THE D/A CHANNELS AND Z-AXIS OUTPUT ARE CONNECTED TO THE MUX INPUTS AS FOLLOWS:

FOR THE 1125A VOLTAGE ADAPTER:

SOURCE CHANNEL	CONNECTED TO	MUX CHANNELS (S.E. MUX)
0	"X" D/A	0,7,10,13
1	"Y" D/A	1,4,11,14
2	"X" D/A	2,5,8,15
3	"Z-AXIS"	3,6,9,12

THE ABOVE TEST CONFIGURATION IS USED TO TEST ANALOG SYSTEM FUNCTIONS. IT ALSO TESTS THE ANALOG PATHS (LOOPS) FOR CONTINUITY AND CHANNEL (D/A, MUX) INDEPENDENCE.

AFTER THE PROGRAM IS LOADED, STARTED AND INITIALIZED, THE TEST RANGES FOR THE D/A AND A/D ARE DETERMINED. THE TEST RANGES ARE THE MAXIMUM AND MINIMUM DATA VALUES THAT CAN BE SENT TO THE "X" AND "Y" D/A CHANNELS THAT WILL NOT CAUSE AN A/D DATA OVERFLOW (VOLTAGES PRODUCED BY D/A CHANNELS THAT ARE OUT OF THE A/D'S VOLTAGE RANGE). THIS WILL NOT HAPPEN IF BOTH A/D AND D/A ARE OF THE SAME POLARITY AND RANGE (I.E. BOTH 0 - 10 VOLTS). HOWEVER, NO RESTRICTION IS PLACED ON THE A/D OR D/A POLARITY/RANGE TYPES. IF THEY ARE DIFFERENT, A LIMITATION WILL EXIST IN THE FULL RANGE ANALOG TESTING OF EITHER THE A/D OR D/A SUB-SYSTEMS. FOR EXAMPLE IF A UNIPOLAR, LOW RANGE D/A (0 - 5 V) IS TESTED IN A LOOP WITH A UNIPOLAR, HIGH RANGE A/D (0 - 10 V), THEN THE RANGE FROM 5 - 10V ON THE A/D CAN NOT BE TESTED. LIKEWISE, IF ONE MODULE IS UNIPOLAR AND THE OTHER IS BIPOLAR (+/- VOLTAGES), THE NEGATIVE VOLTAGE RANGE CANNOT BE TESTED. PROGRAM SUBROUTINE "LCALC" CALCULATES THE MAXIMUM AND THE MINIMUM OCTAL D/A SEND DATA TO BE USED IN THE LOOP AROUND TESTS. MAX/MIN VALUES ARE DETERMINED FROM THE D/A RANGE, POLARITY/CODING TYPE PLUS THE A/D RANGE, POLARITY INFORMATION. THE VALUES ARE CHOSEN SUCH THAT ANY VALUES USED WITHIN THE SEND RANGE (END POINTS INCLUSIVE) WILL NOT CAUSE AN A/D OVERFLOW.

D/A DATA WORDS ARE 12-BITS. THE FIRST STEP IS TO DETERMIN THE "TEST RANGE" AND THE "TEST POLARITY" FOR EACH SOURCE CHANNEL'S D/A (SEE ABOVE) AND THE A/D. THEY ARE AS FOLLOWS:

```
10035 .MAIN
01              ;       D/A     A/D     TEST        D/A         A/D         TEST
02              ;       RANGE   RANGE   RANGE       POLARITY    POLARITY    POLARITY
03              ;       -----   -----   -----       --------    --------    --------
04              ;       LOW     LOW     LOW         UNIPOLAR    UNIPOLAR    UNIPOLAR
05              ;       LOW     HIGH    LOW         UNIPOLAR    BIPOLAR     UNIPOLAR
06              ;       HIGH    LOW     LOW         BIPOLAR     UNIPOLAR    UNIPOLAR
07              ;       HIGH    HIGH    HIGH        BIPOLAR     BIPOLAR     BIPOLAR
08
09              ;       IT IS APPARENT THAT LOW RANGE, AND UNIPOLAR MODE ARE THE
10              ;       LIMITING FACTURS.
11
12              ;       THE VOLTAGE RANGES THEN TESTED ARE AS FOLLOWS:
13
14              ;       TEST        TEST        TEST
15              ;       POLARITY    RANGE       VOLTAGE RANGE (VDC)
16              ;       --------    -----       -------------------
17              ;       UNIPOLAR    LOW         0 - 5
18              ;       UNIPOLAR    HIGH        0 - 10
19              ;       BIPOLAR     LOW         -5 - +5
20              ;       BIPOLAR     HIGH        -10 - +10
21
22              ;       THE TEST VOLTAGE RANGES ARE CONVERTED TO MAXIMUM/MINIMUM
23              ;       D/A SEND OCTAL DATA VALUES AS FOLLOWS:
24
25              ;       THE POSSIBLE MINIMUN D/A SEND DATA VALUES ARE:
26
27              ;       UNIPOLAR TEST: MINIMUM = 000 000 000 000  (000000)
28              ;       BIPOLAR TEST:  D/A RANGE = TEST RANGE
29              ;                      MINIMUM = 100 000 000 000  (100000)
30              ;                      D/A RANGE > TEST RANGE
31              ;                      MINIMUM = 110 000 000 000  (140000)
32
33              ;       THE POSSIBLE MAXIMUM D/A SEND DATA VALUES ARE:
34
35              ;       D/A       TEST      D/A   TEST MAXIMUM
36              ;       PLR       PLR       RNG   RNG  VALUE - BINARY  OCTAL
37              ;       ---       ---       ---   ---  ----------------------
38              ;       UNIPOLAR  UNIPOLAR  LOW   LOW  111 111 111 111 (177760)
39              ;       UNIPOLAR  UNIPOLAR  HIGH  HIGH 111 111 111 111 (177760)
40              ;       UNIPOLAR  UNIPOLAR  HIGH  LOW  100 000 000 000 (100000)
41              ;       BIPOLAR   BIPOLAR   LOW   LOW  011 111 111 111 (077760)
42              ;       BIPOLAR   BIPOLAR   HIGH  HIGH 011 111 111 111 (077760)
43              ;       BIPOLAR   BIPOLAR   HIGH  LOW  010 000 000 000 (040000)
44              ;       BIPOLAR   UNIPOLAR  LOW   LOW  011 111 111 111 (077760)
45              ;       BIPOLAR   UNIPOLAR  HIGH  HIGH 011 111 111 111 (077760)
46              ;       BIPOLAR   UNIPOLAR  HIGH  LOW  010 000 000 000 (040000)
47
48              ;       (ALL OCTAL VALUES ARE 12-BIT LEFT JUSTIFIED)
49
50              ;       FOR MINIMUM VALUES:
51              ;       000000 = TRUE ZERO
52              ;       100000 = BIPOLAR (-) FULL SCALE
53              ;       140000 = BIPOLAR (-) HALF SCALE
54
55              ;       FOR MAXIMUM VALUES:
56              ;       177760 = UNIPOLAR FULL SCALE
57              ;       077760 = BIPOLAR (+) FULL SCALE
58              ;       100000 = UNIPOLAR HALF SCALE
59              ;       040000 = BIPOLAR (+) HALF SCALE
```

```
10036 .MAIN
01              ;       THE ABOVE MAXIMUM/MINIMUM DATA VALUES ARE ADJUSTED
02              ;       ACCORDING TO THE D/A CODING TYPE AS FOLLOWS:
03
04              ;       D/A             D/A             D/A SEND DATA
05              ;       POLARITY        CODING TYPE     MSB (BIT 0)
06              ;       --------        -----------     -----------
07              ;       UNIPOLAR        OFFSET BINARY   NO CHANGE
08              ;       UNIPOLAR        2'S COMPLEMENT  COMPLEMENT MSB
09              ;       BIPOLAR         OFFSET BINARY   COMPLEMENT MSB
10              ;       BIPOLAR         2'S COMPLEMENT  NO CHANGE
11
12              ;       METHOD OF TESTING:
13
14              ;       THIS PROGARM IS DESIGNED TO TEST SEVERAL AREAS
15              ;       OF OPERATION ON THE A/D (MUX) AND D/A INTERFACES. IT
16              ;       IS PRIMARILY AN ANALOG SECTIONS TEST. HOWEVER, MOST
17              ;       LOGIC FUNCTIONS ON THESE MODULES ARE CHECKED IN THE
18              ;       COURSE OF PROGRAM OPERATION. THE PURPOSE OF THIS
19              ;       PROGRAM IS TO EVALUATE, ON A FAIRLY DETAILED BASIS,
20              ;       THE OVERALL FUNCTIONING OF THE MODULES THAT MAKE UP
21              ;       THE SINGLE LOOP ANALOG SYSTEM.
22
23              ;       THE ANALOG SECTIONS ARE TESTED THROUGH A SERIES OF
24              ;       DATA TESTS. THESE TESTS ARE DESIGNED TO DETECT OPEN,
25              ;       SHORTED OR INTERMITTENT ANALOG PATHS AS WELL AS ANALOG
26              ;       CONVERTER LINEARITY. ALL DATA D/A SEND, A/D SCAN,
27              ;       CALCULATIONS AND DATA CHECKS ARE PERFORMED IN THE
28              ;       INDIVIDUAL SUB-TESTS. FEATURES ARE BUILT IN TO ALLOW
29              ;       LOOPING ON ERROR IF ANY DATA ERRORS OCCUR. THE
30              ;       TESTS ARE RUN UNDER MOST OF THE A/D AND D/A OPERATING
31              ;       MODES AND CONDITIONS TO INSURE THAT THEY DO NOT AFFECT
32              ;       DATA CONVERSION INTEGRITY. DATA TESTS ARE AS FOLLOWS:
33
34              ;       ZERO DATA       "X" AND "Y" D/A CHANNELS SET
35              ;       TEST            TO 0 VOLTS (DC) TO TEST OPEN
36              ;                       MULTIPLEXER CHANNELS.
37
38              ;       MAXIMUM DATA    "X" AND "Y" D/A CHANNELS SET
39              ;       TEST            TO THEIR RESPECTIVE MAXIMUM
40              ;                       (POSITIVE VOLTAGE) DATA VALUES
41              ;                       TO TEST GROUNDED MUX CHANNELS.
42
43              ;       MINIMUM DATA    "X" AND "Y" D/A CHANNELS SET
44              ;       TEST            TO THEIR RESPECTIVE MINIMUM
45              ;                       DATA VALUES. (0 VDC IF UNIPOLAR,
46              ;                       NEGATIVE VOLTAGES IF BIPOLAR).
47
48              ;       MAXIMUM/MINIMUM "X" SET TO MAXIMUM DATA VALUE
49              ;       DATA TEST # 1   AND "Y" SET TO MINIMUM DATA
50              ;                       VALUE TO TEST MULTIPLEXER &
51              ;                       D/A CHANNEL INDEPENDENCE.
```

```
10037 .MAIN
01              ;       MAXIMUM/MINIMUM "X" SET TO MINIMUM DATA VALUE
02              ;       DATA TEST # 2   AND "Y" SET TO MAXIMUM DATA
03              ;                       VALUE TO TEST MULTIPLEXER &
04              ;                       D/A CHANNEL INDEPENDENCE.
05              ;
06              ;       SHIFT A "1"     A "1" IS SHIFTED FROM THE LSB
07              ;       DATA TEST # 1   TO THE MSB (OR UNTIL DATA
08              ;                       BECOMES > MAXIMUM DATA VALUE)
09              ;                       OF THE "X" D/A CHANNEL SEND
10              ;                       WORD. TESTS VARIOUS LOOP
11              ;                       VOLTAGES AND DATA BITS.
12              ;                       ("Y" D/A = 0 VDC).
13              ;
14              ;       SHIFT A "1"     A "1" IS SHIFTED FROM THE LSB
15              ;       DATA TEST # 2   TO THE MSB (OR UNTIL DATA
16              ;                       BECOMES > MAXIMUM DATA VALUE)
17              ;                       OF THE "Y" D/A CHANNEL SEND
18              ;                       WORD. TESTS VARIOUS LOOP
19              ;                       VOLTAGES AND DATA BITS.
20              ;                       ("X" D/A = 0 VDC).
21              ;
22              ;       LINEARITY TEST  TEST "X" D/A CHANNEL AND ITS
23              ;       # 1             CORRESPONDING ANALOG LOOPS
24              ;                       (VIA THE A/D AND MULTIPLEXER
25              ;                       CHANNELS) FOR LINEARITY BY
26              ;                       COUNTING FROM THE MINIMUM
27              ;                       DATA VALUE TO THE MAXIMUM
28              ;                       DATA VALUE IN 16. LEAST
29              ;                       SIGNIFICANT BIT (LSB)
30              ;                       INCREMENTS. ("Y" D/A = 0 VDC).
31              ;
32              ;       LINEARITY TEST  TEST "Y" D/A CHANNEL AND ITS
33              ;       # 2             CORRESPONDING ANALOG LOOPS
34              ;                       (VIA THE A/D AND MULTIPLEXER
35              ;                       CHANNELS) FOR LINEARITY BY
36              ;                       COUNTING FROM THE MINIMUM
37              ;                       DATA VALUE TO THE MAXIMUM
38              ;                       DATA VALUE IN 16. LEAST
39              ;                       SIGNIFICANT BIT (LSB)
40              ;                       INCREMENTS. ("X" D/A = 0 VDC).
41              ;
42              ;       REGARDLESS OF THE DATA USED, ALL SUB-TESTS HAVE THE
43              ;       SAME STRUCTURE. ONCE THE DATA HAS BEEN DETERMINED (AS
44              ;       WELL AS THE A/D AND D/A OPERATING CONDITIONS), THE
45              ;       FOLLOWING SEQUENCE OF EVENTS (SUBROUTINES)) WILL BE
46              ;       USED TO IMPLEMENT THE TEST:
47              ;
48              ;       SUBROUTINE NAME         FUNCTION/PURPOSE
49              ;       ~~~~~~~~~~~~~~~         ~~~~~~~~~~~~~~~~
50              ;       SEND                    SEND SPECIFIED # OF DATA WORDS
51              ;                               FROM DATA BLOCK TO D/A IN THE
52              ;                               SELECTED MODES/TRIGGERING.
53              ;
54              ;       SCAN                    PERFORM SPECIFIED # OF A/D
55              ;                               CONVERSIONS IN SELECTED MODE/
56              ;                               TRIGGER & STORE IN DATA BLOCK.
```

```
10038 .MAIN
01              ;       AVERAGE                 CALCULATE THE RECEIVE (ACTUAL)
02              ;                               AVERAGE VALUES PRESENT AT THE
03              ;                               MUX CHANNELS UNDER TEST FROM
04              ;                               THE DATA JUST TAKEN.
05              ;
06              ;       CONVERT                 CONVERT "X" AND "Y" D/A SEND
07              ;                               DATA TO A/D EXPECTED RECEIVE
08              ;                               CENTER/MAXIMUM/MINIMUM DATA.
09              ;
10              ;       CHECK                   CHECK THE RECEIVE (ACTUAL) MUX
11              ;                               CHANNEL AVERAGE VALUES AGAINST
12              ;                               THE MAXIMUM AND MINIMUM DATA
13              ;                               VALUES EXPECTED FROM THEM.
14              ;                               REPORT A DATA ERROR (IF SW D=0)
15              ;                               FOR ANY AND ALL CHANNELS WHOSE
16              ;                               RECEIVE VALUES ARE OUT OF THE
17              ;                               EXPECTED RANGE.
18              ;
19              ;       JMP     (ERROR)         DATA ERROR(S) OCCURED AND/OR
20              ;                               LOOP ON ERROR (SW 1=0). NO
21              ;                               CHANGE IN PREVIOUS TEST PARA-
22              ;                               METERS. REPEAT LAST ANALOG TEST.
23              ;
24              ;       (ERROR) IS AN ADDRESS THAT THE PROGRAM JUMPS TO IF
25              ;       DATA ERRORS OCCURED DURING THE SUBTEST AND LOOP ON ERROR
26              ;       IS INDICATED (ADDRESS DEPENDS ON THE TEST). THE EFFECT
27              ;       IS TO CYCLE ON A FAILING TEST AND "FREEZE" THE TEST
28              ;       (ERROR) DATA PATTERNS WITHIN A SUB-TEST (I.E. FOR
29              ;       SHIFT A "1" AND LINEARITY TESTS). THE OCTAL ADDRESS
30              ;       THAT IS REPORTED IN A DATA ERROR IS THE ADDRESS OF
31              ;       THE CALL TO SUB-ROUTINE "CHECK" IN THE FAILING DATA
32              ;       TEST. THIS IS THE SUB-ROUTINE THAT COMPARES THE
33              ;       RECEIVED DATA TO THE EXPECTED DATA VALUES THAT WERE
34              ;       PREVIOUSLY CALCULATED IN SUB-ROUTINE "CONVERT". IT
35              ;       IS INCLUDED SO THAT THE OPERATOR CAN DETERMINE THE
36              ;       DATA TYPE THAT CAUSED THE FAILURE.
37              ;
38              ;       THE ALLOWED DATA VALUE TOLERANCE BEFORE A DATA ERROR
39              ;       IS REPORTED IS +/- 5 LSB'S FROM THE EXPECTED CENTER
40              ;       RECEIVE VALUE FOR LOOPS CONNECTED TO EITHER THE "X"
41              ;       OR "Y" D/A CONVERTERS. IT IS +/- 100 MV FOR CHAN-
42              ;       NELS CONNECTED TO THE Z-AXIS DC BASE LEVEL VOLTAGE.
43              ;
44              ;       THERFORE, THE ACTUAL RANGE IS AS FOLLOWS:
45              ;       MAXIMUM EXPECTED = EXPECTED CENTER + 5 (OR 10) LSB'S
46              ;       MINIMUM EXPECTED = EXPECTED CENTER - 5 (OR 10) LSB'S.
47              ;
48              ;       THE MAXIMUM EXPECTED IS ALWAYS < = (+) FULL SCALE.
49              ;       THE MINIMUM EXPECTED IS ALWAYS > = 0 FOR UNIPOLAR
50              ;       A/D'S AND ALWAYS > = (-) FULL SCALE FOR BIPOLAR
51              ;       A/D'S. MAXIMUM VALUES ARE ALWAYS MORE POSITIVE
52              ;       THAN MINIMUM VALUES.
53              ;
54              ;       THEREFORE IN ORDER FOR A RECEIVED DATA VALUE
55              ;       TO BE CORRECT THE FOLLOWING MUST BE TRUE:
56              ;
57              ;       MIN EXPECTED < = RECEIVE DATA < = MAX EXPECTED
```

```
10039 .MAIN
01                  ;       MISCELLANEOUS:
02                  ;
03                  ;       EXTERNAL INTERRUPT REQUEST IS NOT TESTED ON EITHER
04                  ;       BOARD. BECAUSE OF THE TESTING CONFIGURATION USING THE
05                  ;       1125A ANALOG TEST ADAPTER, NO MUX CHANNEL INDEPENDENCE
06                  ;       CAN BE DETECTED BETWEEN CHANNLES 7 AND 8.
07                  ;
08                  ;       THIS PROGRAM SHOULD BE RUN FOR 15 - 30 MINUTES OR MORE.
09                  ;       A "PASS" CONDITION EXISTS IF NO A/D OR D/A FUNCTIONAL
10                  ;       ERRORS ARE REPORTED, AND IF NO MUX CHANNELS ARE REPORT-
11                  ;       ING DATA ERRORS. A LONG TERM TEST (1 HOUR +) WILL CHECK
12                  ;       THE CONVERTER SUB-SYSTEMS FOR STABILITY.
```

```
10040 .MAIN
01                  ;8.     OPERATING MODES/SWITCH COMMANDS:
02                  ;       ================================
03                  ;       LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS
04                  ;       (AND SPECIAL OPTIONS). WHILE RUNNING UNDER DTOS,
05                  ;       THIS LOCATION WILL BE LOADED BY THE MONITOR.
06                  ;       HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS
07                  ;       LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED
08                  ;       BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED
09                  ;       OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC.
10                  ;       8.2
11                  ;
12                  ;8.1.0  SWITCH OPTIONS - STANDARD (DTOS) SWITCHES:
13                  ;       DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION
14                  ;       "SWREG" IS AS FOLLOWS:
15                  ;
16                  ;       BIT     OCTAL   BINARY  INTERPRETATION
17                  ;               VALUE   VALUE
18                  ;
19                  ;       1               0       LOOP ON ERROR
20                  ;               40000   1       DO NOT LOOP ON ERROR
21                  ;
22                  ;       2               0       PRINT TO CONSOLE
23                  ;               20000   1       DO NOT PRINT OUT TO CONSOLE
24                  ;
25                  ;       5               0       DO NOT PRINT ON THE LINE PRINTER
26                  ;               02000   1       PRINT ON THE LINE PRINTER
27                  ;
28                  ;       6               0       DO NOT HALT ON ERROR
29                  ;               01000   1       HALT ON ERROR
30                  ;
31                  ;       7               0       DO NOT PRINT ERROR SUMMARY
32                  ;               00400   1       PRINT ERROR SUMMARY
33
34                  ;8.1.1  SWITCH OPTIONS - SPECIAL EXERCISER FUNCTIONS
35
36                  ;       BIT     OCTAL   BINARY  INTERPRETATION
37                  ;               VALUE   VALUE
38
39                  ;       C               0       PRINT ALL ERROR DATA IN OCTAL
40                  ;               00010   1       PRINT ALL ERROR DATA IN SIGNED
41                  ;                               DECIMAL MILLIVOLTS
42
43                  ;       D               0       REPORT DATA ERRORS
44                  ;               00004   1       DO NOT REPORT DATA ERRORS
```

```
10041 .MAIN
01              ;8.2    SWITCH COMMANDS
02              ;       ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
03              ;       THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
04              ;       PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS.
05              ;       EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
06              ;       ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
07              ;       SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
08              ;       (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0)
09              ;       THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE
10              ;       BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE
11              ;       CHANGED BEFORE  CONTROL IS ALLOWED TO RETURN TO THE
12              ;       MAIN PROGRAM.
13              ;
14              ;8.2.1  OTHER COMMANDS
15              ;       "CR"    A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM
16              ;               AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE
17              ;
18              ;       ^D      THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG"
19              ;               TO DEFAULT MODE AND RESTART THE PROGRAM.
20              ;
21              ;       ^R      THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE
22              ;               PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY
23              ;               HAD BEFORE THE COMMAND WAS ISSUED.
24
25              ;       ^O      THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE
26              ;               PROGRAM TO GO TO THE OCTAL DEBUG TOOL (ODT).
27
28              ;       M       THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE
29              ;               CURRENT VALUE OF THE SWITCHES (OPERATING MODES).
30
31              ;       SEE ALSO SECTION 9.
```

```
10042 .MAIN
01              ;9.     OPERATING PROCEDURE/OPERATOR INPUTS:
02              ;       ------------------------------------
03              ;       NOTE: THE POWER SHOULD ALWAYS BE OFF DURING INSERTION
04              ;       AND REMOVAL OF THE A/D - D/A INTERFACES (OR ANY BOARD)
05              ;       INTO MICRO NOVA CHASSIS.
06
07              ;9.1    TO RUN THIS EXERCISER:
08
09              ;       1.  INSERT A/D INTERFACE INTO AN I/O SLOT
10              ;           AND THE D/A INTERFACE (IF LOOP AROUND TEST)
11              ;           WITH THE INTERRUPT PRIORITY (/INTP/) AND
12              ;           DATA CHANNEL PRIORITY (/DCHP/) I/O LINES
13              ;           PROPERLY JUMPERED. ALSO INSERT THE I/O
14              ;           TESTER BOARD IF RUNNING A TEST WITH THE DCH
15              ;           EXERCISER (TESTS 8 & D). SEE SECTION 4 FOR
16              ;           PRIORITY INFORMATION.
17              ;       2.  MAKE ALL NECESSARY CONNECTIONS TO THE 1125A
18              ;           TEST ADAPTER. SEE INDIVIDUAL TEST DESCRIPTIONS
19              ;           IN SECTION 7.2 FOR PROPER SET-UP INSTRUCTIONS.
20              ;           WHEN FINISHED, TURN CPU POWER ON.
21              ;       3.  LOAD THE EXERCISER VIA PAPER TAPE OR
22              ;           DOS DISKETTE. FOR DOS: "LOAD MNACSE" OR
23              ;           "CLOAD MNACSE" (TO LOAD DCH EXERCISER ALSO).
24              ;       4.  STARTING ADDRESS IS 200 (OR 500) OCTAL
25              ;       5.  AFTER THE PROGRAM HAS BEEN STARTED, THE
26              ;           MEMORY WILL BE SIZED AND THE MESSAGE
27
28              ;               "TOP OF MEMORY = XXXXXX"
29              ;
30              ;               WILL BE PRINTED WHERE XXXXXX IS THE
31              ;               HIGHEST LOGICAL MEMORY ADDRESS IN
32              ;               OCTAL.
33              ;       6.  THE TEST TITLE IS PRINTED, FOLLOWED BY:
34
35              ;               "TYPE "?" FOR LIST OF VALID RESPONSES TO ANY
36              ;                QUESTION, "CR" SKIPS."
37
38              ;       7.  "A/D CONVERTER INITIALIZATION FOLLOWS:" IS
39              ;           PRINTED, AND THE INITIALIZATION SEQUENCE FOR
40              ;           THE A/D CONVERTER STARTS.
41
42              ;               "DEVICE CODE = "
43
44              ;               ENTER THE 6-BIT DEVICE CODE OF THE
45              ;               A/D INTERFACE IN OCTAL.
46              ;               (MUST BE < 77 OCTAL).
47
48              ;       "RANGE? "
49
50              ;       THIS IS THE VOLTAGE RANGE OF THE A/D. ENTER:
51              ;       = L FOR 5 VOLT RANGE (0-5 OR +/- 5)
52              ;       = H FOR 10 VOLT RANGE (0-10 OR +/- 10)
53
54              ;       "POLARITY? "
55              ;
56              ;       THIS IS THE POLARITY OF THE A/D. ENTER:
57              ;       = U FOR UNIPOLAR (0-5 OR 0-10)
58              ;       = B FOR BIPOLAR (+/- 5 OR +/- 10)
```

```
10043 .MAIN
01              ;       "TEST? "
02              ;
03              ;       THIS IS THE DESIRED TEST TO BE RUN. ENTER:
04              ;       - A FOR MULTIPLEXER ANALOG INPUT TEST
05              ;       - B FOR MUX INPUT TEST WITH DCH EXERCISER
06              ;       - C FOR D/A TO A/D LOOP AROUND TEST
07              ;       - D FOR LOOP AROUND TEST WITH DCH EXERCISER
08              ;
09              ;       THE INDIVIDUAL PROGRAM TITLE IS PRINTED AFTER THE
10              ;       TEST IS SELECTED AND THE INITIALIZATION SEQUENCE
11              ;       CONTINUES AS FOLLOWS:
12              ;
13              ;       FOR MULTIPLEXER ANALOG INPUT TEST (TESTS A & B):
14              ;
15              ;       "LADDER SOURCE VOLTAGE?"
16              ;
17              ;       THIS IS THE VALUE OF THE EXTERNAL POWER (DC VOLTAGE)
18              ;       SUPPLY THAT IS CONNECTED TO THE 1125A TEST ADAPTER
19              ;       (SEE SECTION 7.2.1 FOR MORE INFORMATION). THE RESPONSE
20              ;       SHOULD BE:
21              ;       - A SIGNED, DECIMAL MILLIVOLT EQUIVALENT VALUE OF
22              ;         THE POWER SUPPLY VOLTAGE. THE MAXIMUM RANGE IS
23              ;         +/- 10 VDC. ALSO, THE VOLTAGE APPLIED MUST BE
24              ;         WITHIN THE OPERATING RANGE OF THE A/D (I.E. -5 VDC
25              ;         CANNOT BE USED ON A 0 - 5 VOLT A/D CONVERTER).
26              ;       - IF ASCII "A" IS THE RESPONSE, THE PROGRAM WILL
27              ;         DETERMINE IT FOR YOU.
28              ;
29              ;       FOR D/A TO A/D LOOP AROUND TEST (TESTS C & D):
30              ;
31              ;       "D/A CONVERTER INITIALIZATION FOLLOWS:" IS PRINTED
32              ;       AND THE D/A CONVERTER INITIALIZATION SEQUENCE STARTS.
33              ;
34              ;       "DEVICE CODE - "
35              ;
36              ;       ENTER THE OCTAL D/A DEVICE CODE. IT MUST BE < 77 AND
37              ;       NOT EQUAL TO THE A/D'S DEVICE CODE.
38              ;
39              ;       "RANGE?"
40              ;
41              ;       THIS IS THE VOLTAGE RANGE OF D/A CONVERTER CHANNELS
42              ;       "X" AND "Y" (TOGETHER). ENTER:
43              ;       - L FOR 5 VOLT RANGE (0-5 OR +/- 5)
44              ;       - H FOR 10 VOLT RANGE (0-10 OR +/-10)
45              ;       - S TO SELECT "X" AND "Y" RANGES SEPERATELY, IN WHICH
46              ;           CASE "RANGE X" AND "RANGE Y" WILL BE ASKED. THE
47              ;           VALID RESPONSES TO THESE ARE "L" OR "H" ONLY. ANY
48              ;           MISTAKE WILL RETURN YOU TO THE PARENT QUESTION.
49              ;
50              ;       "POLARITY?"
51              ;
52              ;       THIS IS THE POLARITY OF D/A CONVERTER CHANNELS "X"
53              ;       AND "Y" (TOGETHER). ENTER:
54              ;       - U FOR UNIPOLAR (0-5 OR 0-10)
55              ;       - B FOR BIPOLAR (+/-5 OR +/-10)
56              ;       - S TO SELECT "X" AND "Y" POLARITIES SEPERATELY, IN
57              ;           WHICH CASE "POLARITY X" AND POLARITY Y" WILL BE
58              ;           ASKED. THE VALID RESPONSES TO THESE ARE "U" OR
59              ;           "B" ONLY. ANY MISTAKE WILL RETURN YOU TO THE
60              ;           PARENT QUESTION.
```

```
 0044 .MAIN
01              ;       "CODING?"
02              ;
03              ;       THIS IS THE DATA CODING TYPE OF D/A CONVERTER CHANNELS
04              ;       "X" AND "Y" (TOGETHER). ENTER:
05              ;       - O FOR OFFSET BINARY CODING (JUMPERS OB1, OB2 IN)
06              ;       - T FOR 2'S COMPLEMENT CODING (JUMPERS TC1, TC2 IN)
07              ;       - S TO SELECT "X" AND "Y" CODING TYPES SEPERATELY, IN
08              ;           WHICH CASE "CODING X" AND "CODING Y" WILL BE ASKED.
09              ;           THE VALID RESPONSES TO THESE ARE "O" OR "T" ONLY.
10              ;           ANY MISTAKE WILL RETURN YOU TO THE PARENT QUESTION.
11              ;       (SEE SECTIONS 11.5 AND 11.6 FOR CODING INFORMATION).
12              ;
13              ;       "TYPE ? FOR HELP" IS PRINTED FOLLOWING THE ABOVE
14              ;       INITIALIZATION SEQUENCES AND THE SELECTED TEST IS
15              ;       THEN STARTED. REFER TO THE INDIVIDUAL TEST DESCRIPTIONS
16              ;       IN SECTION 7.2 FOR TEST OPERATION INFORMATION.
17              ;
18              ;       AN INVALID RESPONSE TO ANY QUESTION WILL CAUSE
19              ;       A LIST OF VALID RESPONSES FOR THE QUESTION
20              ;       TO BE TYPED AND THE QUESTION IS ASKED AGAIN. IF
21              ;       THE RESPONSE IS A "CARRIAGE RETURN" (CR) ONLY, THE
22              ;       QUESTION IS SKIPPED, AND THE PARAMETER THAT
23              ;       WAS PREVIOUSLY ENTERED WILL REMAIN. NOTE THAT ON
24              ;       INITIAL PROGRAM LOADING, THE DEFAULT PARAMETERS WILL
25              ;       BE USED. THEY ARE:
26              ;       - A/D OR D/A RANGE = L (5V)
27              ;       - A/D OR D/A POLARITY = U (UNIPOLAR)
28              ;       - TEST = A (MUX ANALOG INPUT TEST)
29              ;       - LADDER SOURCE VOLTAGE = 0 VDC (ANALOG INPUT TEST ONLY)
30              ;       - CODING = OFFSET BINARY (FOR D/A & LOOP TEST ONLY)
31              ;
32              ;       ALSO NOTE THAT IF TESTS "B" OR "D" (TESTS THAT RUN WITH
33              ;       DCH EXERCISER) IS SELECTED, THE "KITTEN" DATA CHANNEL
34              ;       EXERCISER MUST BE LOADED WITH THIS PROGRAM
35              ;       (I.E. A "CLOAD" IF RUNNING UNDER DTOS DISKETTE).
36              ;
37              ;9.2    OPERATOR INPUTS DURING PROGRAM OPERATION:
38              ;
39              ;       THERE ARE SEVERAL OPERATOR INPUTS THAT CAN BE
40              ;       ENTERED DURING THE OPERATION OF EITHER OF THE TESTS
41              ;       INCLUDED IN THIS EXERCISER. THEY ARE USED TO
42              ;       PERFORM DIFFERENT FUNCTIONS AND FALL INTO ONE
43              ;       OF THE FOLLOWING CLASSES:
44              ;       - INPUTS THAT CHANGE OR DISPLAY THE "SWREG" SWITCHES
45              ;       - INPUTS THAT ALTER PROGRAM OR TEST FLOW
46              ;       - INPUTS THAT CONTROL PROGRAM OUTPUT
47              ;       - INPUTS THAT DISPLAY INFORMATION TO THE OPERATOR
48              ;
49              ;       WHEN RUNNING A TEST, THE FOLLOWING COMMANDS CAN
50              ;       BE ENTERED TO PERFORM THEIR CORRESPONDING ACTIONS:
```

```
10045 .MAIN
01              ;               ENTER:          TO PERFORM FUNCTION:
02              ;               ======          ====================
03              ;               0 - 9, A - F    SET/CLEAR SELECTED "SWREG" SWITCH
04              ;                               (SEE SECTION 8)
05              ;               M               DISPLAY "SWREG" SWITCHES
06              ;               CNTRL - O       ENTER OCTAL DEBUG TOOL (ODT)
07              ;                               (SEE SECTION 11)
08              ;               CNTRL - R       RESTART PROGRAM (NO SWREG CHANGE)
09              ;               CNTRL - D       RESTART PROGRAM (DEFAULT SWREG)
10              ;                               (SEE SECTION 8)
11              ;               CNTRL - T       SELECT A NEW TEST
12              ;                               (SEE SECTION 9.1)
13              ;               CNTRL - S       PRINT SUMMARY OF TEST PARAMETERS
14              ;                               (SEE SECTION 10)
15              ;               CNTRL - C       PRINT THE TEST CONFIGURATION
16              ;                               (SEE SECTION 10)
17              ;               CNTRL - W       PRINT SWITCH FUNCTION SUMMARY
18              ;                               (SEE SECTIONS 8 & 10)
19              ;               SPACE           PRINT TRANSFER/ERROR TABLE
20              ;                               (SEE SECTION 10)
21              ;               ?               PRINT A LIST OF POSSIBLE COMMANDS
22              ;                               (PRINT THIS TABLE)
23
24              ;       ALL INPUTS ARE ECHOED. ANY INVALID INPUT CAUSES THE
25              ;       MESSAGE "TYPE ? FOR HELP" TO BE PRINTED.
```

```
10046 .MAIN
01              ;10.    PROGRAM OUTPUT/ERROR DESCRIPTION:
02              ;       ================================
03              ;       ALL PROGRAM OUTPUTS, BOTH MESSAGES AND ERROR
04              ;       REPORTS, ARE CONTROLLED BY THE VALUE OF "SWREG"
05              ;       (SEE SECTION 8) SWITCHES 2 AND 5 AS FOLLOWS:
06
07              ;       SWITCH          PRINTOUT TO
08              ;       2    5          TTY/CRT  LPT
09              ;       ======          ==========
10              ;       0    0          YES      NO
11              ;       0    1          YES      YES
12              ;       1    0          NO       NO
13              ;       1    1          NO       YES
14
15              ;10.1   FUNCTIONAL ERROR DESCRIPTIONS:
16
17              ;       FUNCTIONAL OR LOGIC ERRORS THAT DETECTED AND REPORTED
18              ;       FOR THE A/D AND D/A INTERFACES ARE AS FOLLOWS:
19              ;       (SEE BELOW FOR MORE DETAILED ERROR DESCRIPTIONS)
20
21              ;       1) A/D CONVERSION TIME OUT
22              ;          D/A CONVERSION TIME OUT
23              ;          - OCCURS IF AN END OF CONVERSION (OR CYCLE) INTERRUPT
24              ;            IS NOT REQUESTED AT THE END OF THE CONVERSION CYCLE.
25              ;       2) A/D DCH CONVERSION ERROR
26              ;          D/A DCH CONVERSION ERROR
27              ;          - OCCURS IF THE DCH FINAL ADDRESS DOES NOT AGREE WITH
28              ;            THE EXPECTED FINAL ADDRESS (CALCULATED FROM THE DCH
29              ;            STARTING ADRRESS AND WORD COUNT LOADED).
30              ;       3) A/D DCH DATA ERROR
31              ;          - OCCURS IF A WORD(S) IN THE CONTIGIOUS DATA BLOCK WAS
32              ;            SKIPPED (NOT WRITTEN INTO) DURING A DCH OPERATION.
33              ;       4) A/D STATUS ERROR
34              ;          D/A STATUS ERROR
35              ;          - OCCURS IF THE STATUS REGISTER CONTENTS DO NOT
36              ;            AGREE WITH THE EXPECTED STATUS (CHECKED AT THE START,
37              ;            DURING AND END OF EACH CONVERSION CYCLE).
38
39              ;       ERRORS 2) AND 3) ABOVE ARE REPORTED IN DCH MODE ONLY.
40              ;       D/A ERRORS ONLY REPORTED DURING LOOP AROUND TEST.
41
42              ;10.2   FUNCTIONAL ERROR FORMATS:
43              ;
44              ;       1)      "(A/D OR D/A) CONVERSION TIME OUT
45              ;               DIA = (STATUS REG)      (MODE/TRIGGER SELECT)
46              ;               CONVERSIONS: EXPECTED = (X)  RECEIVED = (Y)"
47              ;
48              ;       2)      "(A/D OR D/A) DCH CONVERSION ERROR
49              ;               DIB = (DCH ADDRESS REGISTER)
50              ;               CONVERSIONS: EXPECTED = (X)  RECEIVED = (Y)"
51              ;
52              ;       3)      "A/D DCH DATA ERROR AT (ADDR)"
53
54              ;       4)      "(A/D OR D/A) STATUS ERROR"
55              ;               GOOD/BAD
56              ;               GGGGGG BBBBBB"
```

```
10047 .MAIN
01              ;10.3   FUNCTIONAL ERROR DESCRIPTIONS (DETAILED):
02              ;
03              ;       1)      A CONVERSION TIME OUT IS REPORTED IN THE EVENT
04              ;               THAT AN INTERRUPT IS NOT REQUESTED WITHIN A
05              ;               SPECIFIED AMOUNT OF TIME AFTER THE STARTING OF
06              ;               A CONVERSION OR DCH CONVERSION CYCE. THIS
07              ;               INTERRUPT RESULTS FROM "END OF CONVERSION" (EOC)
08              ;               (FOR THE A/D) OR "CLK DONE"/"DDONE" (FOR D/A)
09              ;               IN PIO MODE OR "WORD COUNT=0" (AS A RESULT OF
10              ;               THE LAST CONVERSION OF A DCH CYCLE) IN DCH MODE.
11              ;               THE MODE (PIO OR DCH) AND THE TRIGGER SELECT
12              ;               (STRT, IOPLS, INT/EXT CLK, DCHI, DTA RDY) ARE
13              ;               PRINTED, AS WELL AS THE STATUS WORD (DIA).
14              ;               SEE SECTION 11.4 FOR STATUS WORD INFORMATION.
15              ;               THE # OF CONVERSIONS EXPECTED AND RECEIVED ARE
16              ;               ALSO REPORTED AS FOLLOWS:
17              ;
18              ;               PIO MODE: (1) EXPECTED, (0) RECEIVED
19              ;
20              ;               DCH MODE: (2 IF D/A, 64 OR 128 IF A/D) EXPECTED,
21              ;                         (Y) RECEIVED. (Y) IS CALCULATED BY
22              ;                         READING THE DCH ADDRESS REGISTER AND
23              ;                         SUBTRACTING THE DCH STARTING ADDRESS TO
24              ;                         DETERMINE THE ACTUAL # OF CONVERSIONS
25              ;                         PERFORMED.
26              ;
27              ;               THE AMOUNT OF TIME THAT THE PROGRAM WAITS FOR
28              ;               THE "EOC" INTERRUPT DEPENDS ON THE MODE AND
29              ;               TRIGGERING OF THE A/D (D/A). THEY ARE AS FOLLOWS:
30              ;
31              ;                                         = A/D OR D/A =
32              ;               MODE    TRIGGERING        INTERRUPT WAIT
33              ;               ====    ==========        ==============
34              ;               PIO     STRT, INT OR      600 US
35              ;                       EXT CLK
36              ;               DCH     DCHI OR DCHO      180 MS
37              ;                       (DTA RDY),
38              ;                       INT/EXT CLK
39              ;               DCH     IOPLS             60 US
40              ;
41              ;               IN PIO MODE, THERE IS ONE INTERRUPT PER
42              ;               SINGLE CONVERSION. FOR DCH (DCHI FOR A/D
43              ;               DTA RDY FOR D/A, INTERNAL OR EXTERNAL CLOCK)
44              ;               THE WAIT TIME IS FOR THE ENTIRE DCH CYCLE
45              ;               (ALWAYS < = 400 OCTAL CONVERSIONS). FOR
46              ;               DCH (IOPLS) THE ENTIRE WAIT TIME IS THE
47              ;               TOTAL # OF CONVERSIONS TIMES 60 US.
48              ;
49              ;               THE 1125A ANALOG TEST ADAPTER CABLES (SEE
50              ;               SECTION 4) CONNECT THE INTERNAL CLOCK OUTPUT
51              ;               TO THE EXTERNAL CLOCK INPUT FOR BOTH THE A/D
52              ;               AND D/A INTERFACES. THIS ALLOWS TESTING OF
53              ;               THE CLOCK CIRCUITRY AND CONVERSIONS TO BE
54              ;               PERFORMED IN ALL MODES. NOTE THAT FOR THE
55              ;               D/A (LOOP AROUND TEST), INTERNAL AND EXTERNAL
56              ;               CLOCK MODES ARE TESTED IN DATA CHANNEL (DCH)
57              ;               MODE ONLY.
58              ;
59              ;               IF A TIME OUT OCCURS, FIRST CHECK IF THE
60              ;               TEST CONFIGURATION IS AS SPECIFIED.
```

```
0048 .MAIN
01              ;       2)      A CONVERTER DATA CHANNEL (DCH) ADDRESS CHECK IS
02              ;               PERFORMED ON ALL ROUTINES WHEN OPERATING
03              ;               IN DCH MODE TO INSURE THAT THE # OF CONVERSIONS
04              ;               ACTUALLY RECEIVED IS EQUAL TO THE # THAT ARE
05              ;               EXPECTED AT THE END OF THE CONVERSION CYCLE.
06              ;               THE DCH ADDRESS REGISTER IS READ AND CHECKED
07              ;               TO INSURE THAT THE FINAL DCH ADDRESS IS THE
08              ;               SAME AS THAT CALCULATED FROM THE DCH STARTING
09              ;               ADDRESS AND WORD COUNT (FINAL = STARTING ADDRESS
10              ;               + WORD COUNT). IF THEY ARE NOT EQUAL, A DCH
11              ;               CONVERSION ERROR IS REPORTED, ALONG WITH
12              ;               THE DCH ADDRESS REGISTER CONTENTS (DIB),
13              ;               THE EXPECTED # OF CONVERSIONS AND THE #
14              ;               OF CONVERSIONS ACTUALLY RECEIVED. THE "DIB"
15              ;               WORD IS PRINTED IN OCTAL.
16              ;
17              ;       3)      IN ADDITION TO AN ADDRESS CHECK (SEE ABOVE)
18              ;               AFTER A DCH CYCLE, THE DCH DATA BLOCK IS
19              ;               ALSO CHECKED TO MAKE SURE THAT ALL ADDRESSES
20              ;               WERE ACTUALLY WRITTEN INTO WITH A/D DATA.
21              ;               BEFORE A DCH CYCLE, THE DCH DATA BLOCK IS
22              ;               INITIALIZED WITH -1'S (177777). IF AFTER THE
23              ;               DCH CYCLE ANY LOCATION WITHIN THE DEFINED
24              ;               DCH BLOCK (SPECIFIED BY THE DCH STARTING
25              ;               ADDRESS AND WORD COUNT) IS STILL = -1 THEN
26              ;               A DCH DATA ERROR IS REPORTED. (ADDR) IS THE
27              ;               DATA WORD ERROR LOCATION. *** NOTE ***: THIS
28              ;               APPLIES ONLY TO THE A/D CONVERTER. NO SUCH
29              ;               TEST IS PEFORMED ON THE D/A INTERFACE.
30              ;
31              ;       4)      THE STATUS REGISTER IS CHECKED AT THE
32              ;               BEGINNING AND END OF EACH CONVERSION CYCLE
33              ;               (AND SOMETIMES DURING THE CONVERSION CYCLE)
34              ;               TO INSURE PROPER A/D AND D/A FUNCTIONING. IF A
35              ;               STATUS ERROR IS DETECTED DURING PROGRAM
36              ;               OPERATION, A STATUS ERROR IS REPORTED
37              ;               ALONG WITH THE GOOD (GGGGGG) AND THE BAD
38              ;               (BBBBBB) STATUS REGISTER CONTENTS (DIA).
39              ;               SEE SECTION 11.4 FOR STATUS INFORMATION.
40              ;               IF THE WRONG DEVICE CODE WAS ENTERED FOR AN
41              ;               INTERFACE, OR IF THE MICRO NOVA CANNOT
42              ;               COMMUNICATE WITH AN INTERFACE BECAUSE IT
43              ;               IS NOT INSERTED PROPERLY OR A HARDWARE ERROR
44              ;               EXISTS, A STATUS ERROR WILL BE THE FIRST ERROR
45              ;               REPORTED.
46              ;
47              ;       ERRORS 2) AND 3) ARE ONLY DETECTED AND REPORTED DURING
48              ;       DATA CHANNEL OPERATIONS ON THE INTERFACES. ERROR 3)
49              ;       IS REPORTED FOR THE A/D INTERFACE ONLY. IF EITHER
50              ;       OR BOTH OF THESE ERRORS ARE REPORTED DURING PROGRAM
51              ;       OPERATION, IT GENERALLY INDICATES A PROBLEM WITH THE
52              ;       DCH PRIORITY. THERE COULD ALSO BE A DCH LOGIC OR TIMING
53              ;       PROBLEM. IN MOST CASES, THE FAILURE WILL EXIST IN THE
54              ;       MN603 I/O CONTROLLER CHIP ITSELF (SINCE ALL DCH LOGIC IS
55              ;       CONTAINED IN THIS DEVICE).
```

```
10049 .MAIN
01              ;10.4   OTHER ERRORS:
02
03              ;       1.  "FATAL STACK BOUNDARY VIOLATION, SP = (XXXXXX)"
04              ;           IS REPORTED, FOLLOWED BY A HALT, IF A
05              ;           STACK BOUNDARY IS CROSSED (256 WDS). XXXXXX
06              ;           IS THE VALUE OF THE STACK POINTER (OCTAL).
07              ;           IF CONTINUED, THE PROGRAM WILL RESTART (200).
08              ;
09              ;       2.  "*** RTC FAILURE ****" IS REPORTED, FOLLOWED
10              ;           BY A HALT IF THE REAL-TIME CLOCK FAILS TO
11              ;           CAUSE INTERRUPTS DURING TIMER VALUE CALCULATIONS.
12              ;
13              ;       3.  "UNIDENTIFIED INTERRUPT - (DVC)"
14              ;           IS REPORTED IF ANY DEVICE OTHER THAN THE EXPECTED
15              ;           DEVICE (A/D OR D/A) REQUESTS AN INTERRUPT DURING
16              ;           EXERCISER OPERATION. DVC = THE OCTAL DEVICE CODE
17              ;           OF THE DEVICE REQUESTING THE INTERRUPT. ALSO,
18              ;           THE PROGRAM WILL ATTEMPT TO CLEAR THE INTERRUPT
19              ;           BY ISSUING AN 'NIOC' INSTRUCTION TO THE DEVICE.
20              ;           (SEE BELOW FOR ACTION TAKEN AFTER THIS ERROR).
21              ;
22              ;       4.  "EXTERNAL INTERRUPT - (DVC)"
23              ;           IS REPORTED IF AN UNEXPECTED EXTERNAL INTERRUPT
24              ;           (CAUSED BY GROUNDING THE /EXT INT REQ/ LINE)
25              ;           DURING EXERCISER OPERATION. THE INTERRUPT
26              ;           IS NOT CLEARED BY THE INTERRUPT SERVICE ROUTINE.
27              ;           DVC IS THE EXPECTED INTERRUPTING DEVICE CODE (OCTAL).
28              ;           THIS IS EITHER THE A/D OR D/A DEPENDING ON THE
29              ;           OPERATION BEING PERFORMED AT THE TIME. NOTE THAT
30              ;           IF AN EXTERNAL INTERRUPT IS REQUESTED ON AN INTERFACE
31              ;           WHEN IT IS NOT THE EXPECTED DEVICE, AN UNIDENTIFIED
32              ;           INTERRUPT WILL BE REPORTED INSTEAD (SEE ABOVE).
33              ;           (SEE BELOW FOR ACTION TAKEN AFTER THIS ERROR).
34              ;
35              ;       A/D ERRORS ARE DETECTED AND REPORTED IN THE PROGRAM
36              ;       SUBROUTINE "SCAN". D/A ERRORS ARE DETECTED AND REPORTED
37              ;       IN THE PROGRAM SUBROUTINE "SEND". THESE ERRORS ARE
38              ;       OF THE INTERFACE FUNCTIONAL (LOGIC) TYPE, AND NOT
39              ;       PROGRAM DATA ERRORS. DATA ERRORS ARE REPORTED FROM THE
40              ;       INDIVIDUAL TESTS. SEE THE DESCRIPTIONS IN SECTION 7.2
41              ;       FOR FORMATS, INFORMATION AND INTERPRETATIONS OF THESE
42              ;       ERRORS. ALL TELETYPE (TTY) INPUTS ARE PROCESSED IN THE
43              ;       PROGRAM SUBROUTINE "CHKTTY" ON A NON-INTERRUPT BASSIS.
```

```
10050 .MAIN
01              ;10.5   FUNCTIONAL ERROR HANDLING:
02
03              ;       THE ACTION TAKEN FOLLOWING ERROR MESSAGE PRINTOUT
04              ;       (EXECPT FOR EXTERNAL OR UNIDENTIFIED INTERRUPTS)
05              ;       DEPENDS ON THE VALUE OF "SWREG" (SEE SECTION 8).
06              ;       IF SWITCH 6 = 1 THEN THE PROGRAM WILL HALT AFTER THE
07              ;       MESSAGE "HALTED ON ERROR" IS PRINTED. IF SWITCH
08              ;       1 = 0 THEN THE PROGRAM WILL LOOP ON THE ERROR
09              ;       AFTER THE MESSAGE "LOOPING ON ERROR" IS PRINTED.
10              ;       IN ADDITION, THE PROGRAM WILL REPORT WHERE (IN WHICH
11              ;       SUBROUTINE - "SCAN" OR "SEND) THE ERROR WAS DETECTED.
12              ;       THIS FORMS A TEST SCOPE LOOP FOR FAILURE TRACING
13              ;       WITH AN OSCILLOSCOPE. IF SWITCH 1 = 0 & SWITCH 6 = 1
14              ;       THE PROGRAM WILL FIRST HALT, THEN LOOP ON THE
15              ;       ERROR IF THE PROGRAM IS CONTINUED. TO ESTABLISH
16              ;       A HIGH SPEED LOOP (WHEN LOOPING ON ERROR), INHIBIT
17              ;       TTY/LPT OUTPUTS. THIS PROVIDES A CONVIENIENT METHOD
18              ;       OF ERROR TRACING WITH AN OSCILLOSCOPE OR LOGIC
19              ;       ANALYSER. ALL A/D INPUT/OUTPUT IS PERFORMED IN THE
20              ;       SUBROUTINE "SCAN". ALL D/A INPUT/OUTPUT IS PERFORMED
21              ;       IN THE SUBROUTINE "SEND". REFER TO THESE SUBROUTINES
22              ;       FOR INFORMATION IF YOU ARE TRACING A FUNCTIONAL ERROR.
23              ;       OTHER HELPFUL ITEMS ARE BOARD SCHEMATICS AND PHYSICAL
24              ;       DIAGRAMS.
25              ;
26              ;       IN THE CASE OF AN A/D OR D/A EXTERNAL INTERRUPT, OR AN
27              ;       UNIDENTIFIED INTERRUPT, THE PROGRAM WILL TRY TO
28              ;       CLEAR THE INTERRUPT FIRST, THEN RESTART THE PROGRAM.
29              ;       (FOR AN EXTERNAL INTERRUPT, THE CLEAR IS TO THE A/D OR
30              ;       D/A CONVERTER'S DEVICE CODE. FOR AN UNIDENTIFIED
31              ;       INTERRUPT, AN "NIOC" IS ISSUED TO THE INTERRUPTING
32              ;       DEVICE). IT IS POSSIBLE TO HALT ON ERROR WHEN EITHER
33              ;       OF THESE SITUATIONS OCCUR. HOWEVER IF THE INTERRUPT
34              ;       WILL NOT CLEAR, THE PROGRAM WILL REMAIN IN THE LOOP
35              ;       (FATAL EXERCISER ERRORS). AN EXTERNAL INTERRUPT
36              ;       IS COUNTED AS A STATUS ERROR (ALTHOUGH NOT REPORTED
37              ;       AS ONE) FOR THE A/D OR D/A. AN UNIDENTIFIED
38              ;       INTERRUPT IS NOT.
39              ;
40              ;       IF ANY OF THE ABOVE FUNCTIONAL ERRORS ARE REPORTED
41              ;       FOR THE A/D AND/OR D/A INTERFACES BY THIS EXERCISER,
42              ;       IT IS SUGGESTED THAT THE APPROPRIATE INTERFACE DIAG-
43              ;       NOSTIC BE RUN TO DETECT AND ISOLATE THE EXACT CAUSE
44              ;       OF THE FAILURE, AS THE DIAGNOSTICS ARE MORE SUITABLE
45              ;       FOR "SCOPE LOOP" ERROR TRACING. SEE SECTION 4 FOR THE
46              ;       PART NUMBERS OF THE A/D AND D/A INTERFACE DIAGNOSTIC
47              ;       PROGRAMS.
```

```
10051 .MAIN
01              ;10.6   MISCELLANEOUS PROGRAM OUTPUTS:
02
03              ;       THERE ARE FIVE TYPES OF SUMMARY REPORTS THAT ARE
04              ;       POSSIBLE. THE FIRST IS AN ERROR SUMMARY REPORT. THIS IS
05              ;       OBTAINED WHEN "SWREG" SWITCH 7 GOES FROM A 0 TO A 1.
06              ;       THE REPORT FORMAT IS:
07
08              ;       A/D CONVERSION TIMES OUTS: (#)
09              ;       A/D DCH CONVERSION ERRORS: (#)
10              ;       A/D DCH DATA ERRORS:       (#)
11              ;       A/D STATUS ERRORS:     (#)
12
13              ;       D/A CONVERSION TIMES OUTS: (#)
14              ;       D/A DCH CONVERSION ERRORS: (#)
15              ;       D/A STATUS ERRORS:     (#)
16
17              ;       ALL COUNTS ARE DECIMAL.
18              ;       THE D/A ERRORS ARE REPORTED DURING THE LOOP AROUND
19              ;       TEST OPERATION ONLY.
20
21              ;       THE SECOND IS AN A/D - MULTIPLEXER, D/A TEST PARAMETER
22              ;       SUMMARY REPORT. THIS CAN BE OBTAINED ANY TIME BY ENTER-
23              ;       ING A ^S (CNTRL S). ITS FORMAT IS:
24
25              ;       - A/D CONVERTER & MULTIPLEXER -
26              ;       POLARITY: (UNIPOLAR OR BIPOLAR)
27              ;       RANGE: (5V OR 10V)
28              ;       MODE: (PIO OR DCH)
29              ;       TRIGGERING: (FOR PIO: STRT, INT CLK OR EXT CLK)
30              ;                   (FOR DCH: IOPLS, DCHI, INT CLK OR EXT CLK)
31              ;       CODING: (OFFSET BINARY OR TWO'S COMPLEMENT)
32              ;       MUX TYPE: (DIFFERENTIAL OR SINGLE-ENDED)
33              ;       INITIAL CHANNEL: (0-15. DECIMAL)
34              ;       FINAL CHANNEL: (0-15. DECIMAL)
35              ;       LADDER SOURCE VOLTAGE: (#) MV (SIGNED DECIMAL MILLIVOLTS)
36
37              ;       - D/A CONVERTER -
38              ;       MODE: (PIO OR DCH)
39              ;       TRIGGERING: (FOR PIO: STRT ONLY)
40              ;                   (FOR DCH: IOPLS, DTA RDY, INT CLK, EXT CLK)
41              ;       POLARITY: X = , Y = , (UNIPOLAR OR BIPOLAR)
42              ;       RANGE: X = , Y = , (5V OR 10V)
43              ;       CODING: X = , Y = , (OFFSET BINARY OR TWO'S COMPLEMENT)
44              ;       ALTERNATE: ON
45              ;       SCOPE MODE: (ON IF PIO, OFF IF DCH)
46              ;       CHANNEL SELECT: X (SELECTS WHO GETS DATA FIRST)
47              ;       Z-AXIS DC LEVEL: (#) MV (# IS SIGNED DECIMAL MILLIVOLTS)
48
49              ;       LADDER SOURCE VOLTAGE IS REPORTED FOR ANALOG INPUT TEST
50              ;       ONLY. D/A CONVERTER SUMMARY IS REPORTED FOR THE LOOP
51              ;       AROUND TEST ONLY.
52
53              ;       THIS SUMMARY IS HELPFUL IN DETERMINING IF THE A/D AND/OR
54              ;       D/A TEST PARAMETERS (OPERATING CONDITIONS) ARE CAUSING
55              ;       OR CONTRIBUTING TO DATA ERRORS AND ALSO GIVES THE EXACT
56              ;       STATE OF THE SYSTEM WHEN FUNCTIONAL ERRORS ARE OCCURING.
57              ;       IF THIS SUMMARY IS BEING USED FOR ADDITIONAL INFORMATION
58              ;       DURING ERROR ANALYSIS, THE PROGRAM SHOULD BE IN "LOOP
59              ;       ON ERROR MODE" (SWITCH 1 = 0).
```

```
10052 .MAIN
01              ;       THE THIRD IS A TEST CONFIGURATION SUMMARY, AND CAN BE
02              ;       OBTAINED BY ENTERING A CNTRL-C ON THE TTY CONSOLE.
03              ;       THIS REPORT GIVES A SUMMARY OF PERTINENT INFORMATION
04              ;       ON WHAT YOU NEED TO RUN THE TEST PROPERLY AND HOW
05              ;       THE TEST HARWARE IN CONNECTED TO THE A/D AND D/A
06              ;       INTERFACES.
07
08              ;       IF THIS SUMMARY IS REQUESTED DURING THE MUX ANALOG
09              ;       INPUT TEST, THE FOLLOWING SUMMARY IS REPORTED:
10
11              ;       *** MULTIPLEXER ANALOG INPUT TEST CONFIGURATION ***
12
13              ;       REQUIRED HARDWARE:
14              ;       ANALOG TO DIGITAL INTERFACE BOARD MODEL 4223
15              ;       ANALOG VOLTAGE TEST ADAPTER MODEL 1125A
16              ;       ADAPTER (CONNECTOR J2) TO A/D CABLE PART # 005 - 12431
17              ;       ADAPTER SWITCH SETTINGS: 1,2,3,4,8 = ON
18              ;       EXTERNAL VOLTAGE SOURCE (+/- 10 VDC MAX) = "V.IN"
19
20              ;       INTERCONNECTION SCHEME AND MUX CHANNEL VALUES ARE:
21
22              ;               SINGLE-ENDED MUX          DIFFERENTIAL MUX
23              ;               ================          ================
24              ;       ADAPTER MUX                       MUX
25              ;       CHANNEL CHANNELS    %V.IN         CHANNELS    %V.IN
26              ;       ======= ========    =====         ========    =====
27              ;       0       0,7,10,13   100.          0,7         30.
28              ;       1       1,4,11,14   90.           1,4         50.
29              ;       2       2,5,8,15    70.           2,5         -30.
30              ;       3       3,6,9,12    40.           3,6         -50.
31
32              ;       IF THE SUMMARY IS REQUESTED FROM THE D/A TO A/D
33              ;       LOOP AROUND TEST, THE FOLLOWING IS REPORTED:
34
35              ;       *** D/A TO A/D LOOP AROUND TEST CONFIGURATION ***
36
37              ;       REQUIRED HARDWARE:
38              ;       ANALOG TO DIGITAL INTERFACE BOARD MODEL 4223
39              ;       DIGITAL TO ANALOG INTERFACE BOARD MODEL 4224
40              ;       ANALOG VOLTAGE TEST ADAPTER MODEL 1125A
41              ;       D/A TO ADAPTER (CONNECTOR J1) CABLE PART # 005 - 12425
42              ;       ADAPTER (CONNECTOR J2) TO A/D CABLE PART # 005 - 12431
43              ;       ADAPTER SWITCH SETTINGS: 1-8 = OFF
44
45              ;       INTERCONNECTION SCHEME FOR SINGLE-ENDED
46              ;       MULTIPLEXER TYPE IS:
47
48              ;       FROM            VIA ADAPTER     TO
49              ;       SOURCE:         SOURCE CHANNEL: MUX CHANNEL:
50              ;       ======          ==============  ===========
51              ;       X D/A           0               0,7,10,13
52              ;       Y D/A           1               1,4,11,14
53              ;       X D/A           2               2,5,8,15
54              ;       Z-AXIS          3               3,6,9,12
```

```
10053 .MAIN
01              ;       THE FOURTH SUMMARY REPORT, OBTAINED BY ENTERING
02              ;       CNTRL-W, IS THE SWITCH FUNCTION SUMMARY AS FOLLOWS:
03              ;
04              ;       *** SWITCH (SWREG) FUNCTION SUMMARY ***
05              ;
06              ;       SWITCH 1 = 0 LOOP ON ERROR
07              ;                = 1 DO NOT LOOP ON ERROR
08              ;       SWITCH 2 = 0 PRINT TO TTY CONSOLE
09              ;                = 1 DO NOT PRINT TO TTY CONSOLE
10              ;       SWITCH 5 = 0 DO NOT PRINT TO LPT
11              ;                = 1 PRINT TO LPT
12              ;       SWITCH 6 = 0 DO NOT HALT ON ERROR
13              ;                = 1 HALT ON ERROR
14              ;       SWITCH 7 = 0 DO NOT PRINT ERROR SUMMARY
15              ;                = 1 PRINT ERROR SUMMARY REPORT
16              ;       SWITCH C = 0 PRINT ERROR DATA IN OCTAL
17              ;                = 1 PRINT ERROR DATA IN DECIMAL MILLIVOLTS
18              ;       SWITCH D = 0 PRINT DATA ERRORS
19              ;                = 1 DO NOT PRINT DATA ERRORS
20              ;
21              ;       THE FIFTH AND LAST SUMMARY REPURT POSSIBLE IS THE
22              ;       PRINTING OF THE TRANSFER AND ERROR COUNT TABLE.
23              ;       IS IMPORTANT, AS THE INFORMATION CONTAINED IN THIS
24              ;       TABLE IS USED TO DETERMINE THE PERFORMANCE OF THE
25              ;       MUX AND/OR D/A CHANNELS UNDER TEST. THE PASS/FAIL
26              ;       INFORMATION IS DETERMINED BY EVALUATING THE NUMBER
27              ;       OF TRANSFERS AND ERRORS REPORTED FOR THE MUX CHANNELS
28              ;       OVER A SPECIFIED PERIOD OF TIME. OBVIOUSLY THE BEST
29              ;       SITUATION IS TO HAVE NO ERRORS REPORTED FOR ANY
30              ;       AND ALL CHANNELS TESTED. THE SUMMARY FORMAT IS:
31              ;
32              ;                               SINGLE-ENDED MUX        DIFFERENTIAL MUX
33              ;       MUX CHANNEL             TRANSFERS/ERRORS        TRANSFERS/ERRORS
34              ;       0.                      STTTTT  SEEEEE          DTTTTT  DEEEEE
35              ;       1.                      STTTTT  SEEEEE          DTTTTT  DEEEEE
36              ;       .                         .       .               .       .
37              ;       .                         .       .               .       .
38              ;       7.                      STTTTT  SEEEEE          DTTTTT  DEEEEE
39              ;       8.                      STTTTT  SEEEEE
40              ;       .                         .       .
41              ;       .                         .       .
42              ;       14.                     STTTTT  SEEEEE
43              ;       15.                     STTTTT  SEEEEE
44              ;
45              ;       WHERE:  STTTTT = TRANSFER COUNT FOR THE RESPECTIVE
46              ;                        SINGLE-ENDED MUX CHANNEL
47              ;               SEEEEE = ERROR COUNT FOR THE RESPECTIVE
48              ;                        SINGLE-ENDED MUX CHANNEL
49              ;               DTTTTT = TRANSFER COUNT FOR THE RESPECTIVE
50              ;                        DIFFERENTIAL MUX CHANNEL
51              ;               DEEEEE = ERROR COUNT FOR THE RESPECTIVE
52              ;                        DIFFERENTIAL MUX CHANNEL
53              ;
54              ;       NOTES:  1) ALL COUNTS ARE DECIMAL.
55              ;               2) MAXIMUM ERROR COUNT IS 65,536.
56              ;               3) MUX CHANNEL #'S ARE DECIMAL
57              ;               4) DIFFERENTIAL MUX MODE IS NOT TESTED IN THE
58              ;                  D/A TO A/D LOOP AROUND TEST. BOTH TRANSFER
59              ;                  AND ERROR COUNTS SHOULD BE = 0.
```

```
10054 .MAIN
01              ;11.    DEBUG HELP:
02              ;       ----------
03              ;       *** OCTAL DEBUG TOOL (ODT) ***
04              ;
05              ;       THE DIAGNOSTIC IS EQUIPED WITH A BUILT IN ODT WHICH CAN
06              ;       BE ACCESSED BY HITTING CONTROL O (^O) AT ANY TIME DURING
07              ;       THE EXECUTION OF THE PROGRAM (AFTER SETTING THE PARA-
08              ;       METERS).
09              ;
10              ;       ON ENTERING ODT THE ADDRESS OF THE LOCATION HAVING THE
11              ;       NEXT INSTRUCTION TO BE EXECUTED WILL BE TYPED-OUT.
12              ;
13              ;11.1   CONVENTIONS AND SYMBOLS
14              ;       THE FOLLOWING CONVENTIONS ARE USED BY THE ODT:
15              ;       ?       PRESSING ANY ILLEGAL KEY CAUSES THE ODT TO RES-
16              ;               POND WITH A "?".
17              ;       @       ODT IS READY AND AT YOUR SERVICE.
18              ;
19              ;11.2   COMMAND STRUCTURE
20              ;       AN ODT COMMAND HAS THE FOLLOWING FORMAT:
21              ;               [ARGUMENT][COMMAND]
22              ;       AN ARGUMENT MAY BE ONE OF THE FOLLOWING:
23              ;       "EXP"   AN OCTAL EXPRESSION CONSISTING OF OCTAL NUMBERS
24              ;               SEPARATED BY PLUS (+) OR MINUS (-) SIGNS. LEAD-
25              ;               ING ZEROS NEED NOT BE TYPED.
26              ;       "ADR"   AN ADDRESS IS THE SAME AS AN EXPRESSION EXCEPT
27              ;               THAT BIT 0 IS NEGLECTED.
28              ;       A COMMAND IS A SINGLE TELETYPE CHARACTER
29              ;
30              ;11.3   ODT COMMANDS
31              ;       THE LOCATIONS THAT CAN BE EXAMINED AND MODIFIED BY THE
32              ;       USER ARE CALLED CELLS. THESE CELLS ARE OF TWO TYPES:
33              ;       INTERNAL CPU CELLS AND MEMORY LOCATIONS.
34              ;
35              ;11.3.1 OPENING INTERNAL CELLS
36              ;       THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF
37              ;       THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN
38              ;       0 AND 7
39              ;       0-3     FOR ACCUMULATORS 0-3
40              ;       4       FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN
41              ;               THE EVENT OF A "P" COMMAND.
42              ;       5       CPU AND TTO STATUS
43              ;               BIT     INTERPRETATION
44              ;               15      STATUS OF TTO DONE FLAG
45              ;               14      STATUS OF INTERRUPTS (ION FLAG)
46              ;               13      STATUS OF CARRY BIT
47              ;       6       ADDRESS OF THE LOCATION HAVING THE BREAK POINT (IF
48              ;               ANY)
49              ;       7       INSTRUCTION AT THE BREAK POINT LOCATION
50
```

```
10055 .MAIN
01              ;       OTHER COMMANDS TO OPEN CELLS ARE:
02              ;
03              ;       "ADR"/  OPEN THE CELL AND PRINT ITS CONTENTS
04              ;       ./      OPEN THE CELL CURRENTLY POINTED TO BY THE POINTER
05              ;               AND PRINT ITS CONTENTS.
06              ;       .+"ADR"/        ADD "ADR" TO THE POINTER, OPEN THE CELL AND PRIN
07              ;               ITS CONTENTS.
08              ;       .-"ADR"/        SUBTRACT "ADR" FROM THE POINTER, OPEN THE CELL A
09              ;               PRINT ITS CONTENTS.
10              ;       "CR"    THE RETURN KEY IS USED TO CLOSE THE OPEN CELL
11              ;               WITH OR WITHOUT MODIFICATION.
12              ;       "LF"    LINE FEED IS USED TO CLOSE THE OPEN CELL WITH OR
13              ;               WITHOUT MODIFICATION AND TO OPEN THE SUCCEEDING
14              ;               CELL.
15              ;       ^       CLOSE THE OPEN CELL WITH OR WITHOUT MODIFICATION
16              ;               AND OPEN THE PRECEDING CELL
17              ;       /       CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
18              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS.
19              ;       +"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
20              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS +"ADDR".
21              ;       -"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
22              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS - "ADR".
23              ;
24              ;11.3.2 MODIFICATION OF A CELL
25              ;       ONCE A CELL HAS BEEN OPENED ITS CONTENTS CAN BE MODIFIED
26              ;       BY TYPING THE NEW VALUE THE CELL IS TO CONTAIN IN THE
27              ;       FORM OF AN OCTAL EXPRESSION FOLLOWED BY "CR" OR "LF".
28              ;       IF A + OR - IS TYPED AS THE FIRST CHARACTER OF THE EX-
29              ;       PRESSION THEN THE VALUE OF THE EXPRESSION IS ADDED TO OR
30              ;       SUBTRACTED FROM THE OLD CONTENTS OF THE CELL. THE
31              ;       ADDRESS ITSELF OR AN EXPRESION RELATIVE TO THE ADDRESS
32              ;       CAN BE DEPOSITED BY TYPING A "." OR ".+/-OCTAL EXPRESS-
33              ;       ION". A RUBOUT COMMAND GIVEN RIGHT AFTER OPENING A CELL
34              ;       ALLOWS THE MODIFICATION OF ITS CONTENTS AS IF THEY WERE
35              ;       TYPED IN JUST BEFORE THE COMMAND WAS ISSUED.
36              ;
```

```
10056 .MAIN
01              ;11.3.3 OTHER ODT COMMANDS
02              ;       RUBOUT  THIS KEY IS USED TO DELETE ERRONEOUSLY TYPED
03              ;               DIGITS. EACH TIME THE KEY IS PRESSED THE RIGHT MOST
04              ;               DIGIT IS DELETED AND ECHOED ON THE TERMINAL. IF
05              ;               THE RUBOUT KEY IS PRESSED RIGHT AFTER OPENING A
06              ;               CELL THEN IT DELETES THE RIGHT MOST DIGIT OF THE CELL'S
07              ;               CONTENTS. THIS ALLOWS THE MODIFICATION OF THE CELL
08              ;               AS IF ITS CONTENTS WERE TYPED IN JUST BEFORE THE
09              ;               KEY WAS PRESSED.
10              ;       "ADR"B  INSERT A BREAK POINT AT LOCATION "ADR".
11              ;               ONLY ONE BREAK POINT CAN BE INSERTED AND ANY
12              ;               ENTRY TO ODT AFTER EXECUTING A BREAK POINT WILL
13              ;               CAUSE IT TO BE DELETED.
14              ;       D       DELETE THE BREAK POINT IF ANY.
15              ;       P       RESTART THE EXECUTION OF THE PROGRAM AT LOCATION
16              ;               POINTED BY 4A.
17              ;       "ADR"R  START EXECUTING THE PROGRAM AT "ADR" AFTER AN
18              ;               IO-RESET.
19              ;       K       KILL THE STRING TYPED SO FAR. THE ODT RESPONDS
20              ;               WITH A "?" AND THE OPEN CELL IS CLOSED WITHOUT
21              ;               MODIFICATION.
22              ;       =       PRINT THE OCTAL VALUE OF THE INPUT ONLY.
23              ;               THIS WILL CLOSE ANY OPEN CELLS WITHOUT
24              ;               MODIFICATION AND WILL NOT OPEN A CELL
25              ;
26              ;
27              ;       NOTE:   IN PROGRAMS WHICH RELOCATE THEMSELVES THE
28              ;               THE USER SHOULD PLACE BREAK POINTS ONLY IN THE
29              ;               THE ORIGINAL PROGRAM AREA. IF A BREAK POINT IS
30              ;               PLACED OUTSIDE THIS AREA THE RESULTS WILL
31              ;               BE UNPREDICTABLE.
```

```
!0057 .MAIN
01              ;11.4   INSTRUCTION SET SUMMARY:
02
03              ;11.4.1 4223 A/D CONVERTER INSTRUCTION SET:
04
05              ;DOA:   OUTPUTS INITIAL DOA MUX CHANNEL, FINAL MUX
06              ;       CHANNEL, AND STATUS BITS TO THE INTERFACE.
07
08              ;       D0, D1, D2 ARE THE CLOCK SOURCE SELECT BITS:
09
10              ;           D0  D1  D2  CLOCK SOURCE TO START A/D CONVERSIONS
11              ;           --  --  --  ------------------------------------
12
13              ;            0   0   0   /STRT/, NO SYNC
14
15              ;PROGRAMMED 0   0   1   NO CONVERSIONS
16
17              ;   I/O      0   1   0   /STRT/, INTERNAL CLOCK SYNC
18              ;                        (FALLING EDGE)
19
20              ;            0   1   1   /STRT/, EXTERNAL CLOCK SYNC
21              ;                        (FALLING EDGE)
22
23
24              ;            1   0   0   /IOPLS/, (1 DATA CHANNEL CONVERSION
25              ;                        FOR EVERY /IOPLS/, NO SYNC
26
27              ;DATA        1   0   1   /DCHI/, NO SYNC
28              ;                        (MAXIMUM TRANSFER RATE)
29
30              ;CHANNEL     1   1   0   INTERNAL CLOCK SYNC
31              ;                        (FALLING EDGE)
32
33              ;            1   1   1   EXTERNAL CLOCK SYNC
34              ;                        (FALLING EDGE)
35
36              ;ALL DATA CHANNEL SEQUENCES BEGIN WITH THE NEXT CLOCK
37              ;SOURCE SIGNAL AFTER STRT.  SYNCHRONIZATION OCCURS ON
38              ;THE FALLING EDGE OF THE INTERNAL OR EXTERNAL CLOCK.
39
40              ;           D3          SINGLE-ENDED/DIFFERENTIAL
41              ;                       CHANNEL SELECT
42              ;                       0 =  DIFFERENTIAL
43              ;                       1 =  SINGLE-ENDED
44
45              ;           D4-D7       FINAL MUX CHANNEL, BIT 4 MSB
46
47              ;           D12-D15     INITIAL MUX CHANNEL, BIT 12 MSB
48
49              ;TO READ DATA ON ONLY ONE CHANNEL, BOTH THE FINAL AND
50              ;INITIAL CHANNELS SHOULD EQUAL THE DESIRED CHANNEL.
51              ;/IORST/ CLEARS ALL STATUS BITS.  THE DOA INSTRUCTION
52              ;SHOULD NOT BE GIVEN IF BUSY IS SET.
```

```
!0058 .MAIN
01              ;DOB:   OUTPUTS TO ADDRESS REGISTER FOR DATA CHANNEL
02              ;       TRANSFERS
03
04              ;DOC:   OUTPUTS TO WORD-COUNT REGISTER FOR DATA CHANNEL
05              ;       TRANSFERS
06
07              ;DIA:   INPUTS CURRENT MUX CHANNEL AND STATUS BITS:
08
09              ;           D0          1 IF EXTERNAL INTERRUPT REQUEST
10              ;                       HAS OCCURRED, 0 OTHERWISE
11
12              ;           D1          1 IF EOC IS HIGH (CONVERSION
13              ;                       IS FINISHED), 0 OTHERWISE
14
15              ;           D8          1 IF CLOCK OVERRUN HAS OCCURRED,
16              ;                       0 OTHERWISE.
17
18              ;           D12-D15     CURRENT MUX CHANNEL
19
20              ;       ALL OTHER BITS ARE CLEARED.  EXTERNAL INTERRUPT
21              ;       REQUEST BIT AND CLOCK OVERRUN BIT ARE CLEARED
22              ;       BY I/O CLEAR INSTRUCTION OR IORST.
23
24              ;DIB:   INPUTS DCH ADDRESS REGISTER
25
26              ;DIC:   INPUTS DATA FROM A/D CONVERTER.  DATA IS LEFT
27              ;       JUSTIFIED IN BITS 0-11, WITH BIT 0 THE MSB.
```

```
10059 .MAIN
01              ;11.4.2 4224 D/A CONVERTER INSTRUCTION SET:
02
03              ;       DOA:  OUTPUT STATUS BITS TO THE INTERFACE, CLEARS
04              ;       EXTERNAL INTERRUPT REQUEST AND LATE CONVERSION.
05              ;       SHOULD NOT BE GIVEN IF BUSY IS SET AND MUST APPEAR
06              ;       BEFORE DOB AND DOC IN DATA CHANNEL SETUP SEQUENCE.
07
08              ;       D0, D1, D2 ARE THE CLOCK SOURCE BITS FOR SENDING
09              ;       DIGITAL DATA TO THE D/A CONVERTERS:
10
11              ;       D0      D1      D2      CLOCK SOURCE TO SEND DAC DATA
12              ;       --      --      --      ----------------------------
13              ;       0       0       0       /STRT/, NO SYNC
14              ;       0       0       1       NO CONVERSIONS
15              ;       0       1       0       INTERNAL CLOCK SYNC *
16              ;       0       1       1       EXTERNAL CLOCK SYNC *
17              ;       1       0       0       /IOPLS/ (1 DATA CONVERSION
18              ;                               FOR EVERY /IOPLS/ FOLLOWING
19              ;                               /STRT/, NO SYNC) **
20              ;       1       0       1       /DATA READY/ (OCCURS 1
21              ;                               FSTROBE CYCLE AFTER /DCHO/
22              ;                               & IS MAXIMUM TRANSFER RATE)
23              ;       1       1       0       INTERNAL CLOCK SYNC
24              ;       1       1       1       EXTERNAL CLOCK SYNC
25
26              ;       * FIRST FALLING EDGE AFTER DOC COMMAND
27              ;       ** DATA SHOULD BE READY IN THE FIRST BUFFER BEFORE
28              ;          /IOPLS/ IS ISSUED
29
30              ;D3     ALTERNATE BIT       0       DO NOT ALTERNATE BETWEEN
31              ;                                   DAC X AND DAC Y.
32
33              ;                           1       ALTERNATE BETWEEN DAC X AND
34              ;                                   DAC Y, STARTING WITH DAC
35              ;                                   SELECTED BY D15
36
37              ;D4     /SCOPE MODE/ BIT    0       Z-AXIS PULSE GIVEN EVERY TIME
38              ;                                   DAC X OR DAC Y (JUMPER
39              ;                                   SELECTABLE) IS WRITTEN TO
40
41
42              ;                           1       NO Z-AXIS PULSES OUTPUTTED
43
44              ;D5     /NON-STORE/         1       FOR NON-STORE, OC TRUE-LOW
45              ;                                   OUTPUT (PINS A9 AND A10)
46
47              ;D6     /WRITE-THROUGH/     1       FOR WRITE-THROUGH, OC TRUE-LOW
48              ;                                   OUTPUT (PINS A11 AND A12)
49
50              ;D7     /ERASE/             1       FOR 2 MS PULSE TO SCOPE,
51              ;                                   OC TRUE-LOW OUTPUT
52              ;                                   (PINS A13 AND A14)
53
54              ;D15    DAC SELECT BIT      0       SELECTS DAC X
55              ;                           1       SELECTS DAC Y
56
57              ;       THE DEFAULT STATE OF ALL THESE STATUS BITS
58              ;       UPON POWER-UP OR IORST IS 0.
```

```
10060 .MAIN
01              ;DOB:   OUTPUTS TO ADDRESS REGISTER FOR DATA CHANNEL
02              ;       TRANSFERS.
03
04              ;DOC:   OUTPUTS TO WORD-COUNT REGISTER FOR DATA CHANNEL
05              ;       TRANSFERS. IN PROGRAMMED I/O MODE (D0=0 IN
06              ;       DOA INSTRUCTION) THIS INSTRUCTION CAUSES THE
07              ;       FIRST BUFFER TO BE LOADED WITH THE DATA IN
08              ;       THE ACCUMULATOR BITS 0-11, 14 AND 15.
09              ;       BITS 0-11 ARE THE D/A DATA, WITH BIT 0 THE MSB.
10              ;       BITS 14 AND 15 CONTAIN BRIGHTNESS INFORMATION
11              ;       FOR Z-AXIS PULSES. A CLOCK SIGNAL AS SELECTED BY
12              ;       THE DOA INSTRUCTION THEN OUTPUTS THE DATA TO THE
13              ;       SECOND BUFFER AND THE APPROPRIATE DAC.
14
15              ;DIA:   INPUTS STATUS BITS FROM THE INTERFACE
16
17              ;D0     1  IF EXTERNAL INTERRUPT REQUEST HAS OCCURRED,
18              ;       0  OTHERWISE
19              ;D1     1  IF DATA READY=1, 0 OTHERWISE.  THIS INDICATES
20              ;          THE PRESENCE OF DIGITAL DATA IN THE FIRST BUFFER.
21
22              ;D8     1  IF LATE CONVERSION=1, 0 OTHERWISE.  THIS INDICATES
23              ;          A LOSS OF SYCHRONIZATION WITH THE INTERNAL OR
24              ;          EXTERNAL CLOCK IN DATA CHANNEL MODE.
25
26              ;D15    1  IF /EXTERNAL ERASE INPUT/ LINE IS PULLED LOW,
27              ;       0  OTHERWISE.
28
29              ;DIB:   INPUTS CURRENT DATA CHANNEL ADDRESS REGISTER
30
31              ;DIC:   NOT USED
```

```
10061 .MAIN
01              ;11.5   JUMPER/RESISTOR INFORMATION:
02
03              ;11.5.1 A/D CONVERTER SYSTEM MODEL 4223
04              ;       JUMPER CONFIGURATION INFORMATION:
05
06              ;       JUMPER(S)       FUNCTION(S)/NOTES
07              ;       ---------       -----------------
08
09              ;       W1              IF INSERTED, A13 CONTAINS THE
10              ;                       "Y" INFORMATION FOR ADC CROSS PLOT
11              ;                       TEST. IT SHOULD NOT BE INSERTED
12              ;                       NORMALLY.
13
14              ;       W2, W3          A/D CONVERTER RANGE/POLARITY SELECT
15              ;                       AS FOLLOWS:
16
17              ;                       RANGE/POLARITY  JUMPERS (INSERTED)
18              ;                       --------------  ------------------
19              ;                       +/- 10 VDC      W3, W4
20              ;                       +/- 5 VDC       W2, W4
21              ;                       0 - 5 VDC       W2, W5
22              ;                       0 - 10 VDC      W2
23
24              ;       W6, W7          A/D CODING TYPE SELECT AS FOLLOWS:
25
26              ;                       W6 IN = TWO'S COMPLEMENT CODING
27              ;                       W7 IN = OFFSET BINARY CODING
28              ;                       (ONLY ONE MAY BE INSERTED).
29
30              ;       W8 - W13        A/D DEVICE CODE SELECT AS FOLLOWS:
31
32              ;                       -------- DATA BIT ---------
33              ;                       10   11   12   13   14   15
34              ;                       -------------------------
35              ;                       W10  W11  W9   W12  W13  W8
36              ;                       DS0 (MSB)             DS5 (LSB)
37
38              ;                       INSERT CORRESPONDING JUMPER FOR
39              ;                       A "1" IN ANY OF ABOVE DEVICE CODE
40              ;                       SELECT ("DS") BITS.
41
42              ;       W14, W15        "ADC READY" HANDSHAKING SIGNAL SELECT
43              ;                       AS FOLLOWS:
44
45              ;                       W14 IN = TRUE LOW
46              ;                       W15 IN = TRUE HIGH
47              ;                       (ONLY ONE MAY BE INSERTED).
48
49              ;       W16             IF INSERTED, A "CLOCK OVERRUN" ERROR
50              ;                       STATUS SIGNAL WILL SET DONE.
51
52              ;       A/D CONVERTER POTENTIOMETER INFORMATION:
53
54              ;       POTENTIOMETER           FUNTION
55              ;       -------------           -------
56
57              ;       R26                     INTERNAL CLOCK FREQUENCY
58              ;                               (NOMINAL RANGE: 30 US - 500 US)
59              ;       R21                     A/D CONVERTER GAIN ADJUST
60              ;       R20                     A/D CONVERTER OFFSET ADJUST
```

```
 0062 .MAIN
01              ;11.5.2 D/A CONVERTER SYSTEM MODEL 4224
02              ;       JUMPER CONFIGURATION INFORMATION:
03
04              ;       JUMPER(S)       FUNCTION/NOTES
05              ;       ---------       --------------
06
07              ;       W1 - W10        D/A CONVERTER RANGE/POLARITY SELECT
08              ;                       FOR CHANNELS "X" & "Y" AS FOLLOWS:
09
10              ;                                       JUMPERS (INSERTED)
11              ;                       RANGE/POLARITY  DAC "X" DAC "Y"
12              ;                       --------------  ------- -------
13              ;                       +/- 10 VDC      W2,W4   W7,W9
14              ;                       +/- 5 VDC       W2,W5   W7,W10
15              ;                       0 - 5 VDC    W1,W3,W5   W6,W8,W10
16              ;                       0 - 10 VDC      W1,W5   W6,W10
17
18              ;       W11 - W14       D/A CODING TYPE SELECT AS FOLLOWS:
19
20              ;                       W11 IN = OFFSET BINARY FOR DAC X
21              ;                       W12 IN = 2'S COMPLEMENT FOR DAC X
22
23              ;                       W13 IN = OFFSET BINARY FOR DAC Y
24              ;                       W14 IN = 2'S COMPLEMENT FOR DAC Y
25              ;                       (ONLY ONE MAY BE INSERTED FOR EACH).
26
27              ;       W15 - W20       D/A DEVICE CODE SELECT AS FOLLOWS:
28
29              ;                       -------- DATA BIT ---------
30              ;                       10   11   12   13   14   15
31              ;                       -------------------------
32              ;                       W19  W20  W15   W16  W17  W18
33              ;                       DS0 (MSB)             DS5 (LSB)
34
35              ;                       INSERT CORRESPONDING JUMPER FOR
36              ;                       A "1" IN ANY OF ABOVE DEVICE CODE
37              ;                       SELECT ("DS") BITS.
38
39              ;       W21, W22      * Z-AXIS PULSE TRIGGERING WHEN DATA
40              ;                       IS LOADED IN CHANNEL "X" OR "Y":
41
42              ;                       W21 IN = TRIGGER ON DAC "Y" LOAD
43              ;                       W22 IN = TRIGGER ON DAC "X" LOAD
44              ;                       (ONLY ONE MAY BE INSERTED).
45              ;                     * NOTE: D/A MUST BE IN SCOPE MODE.
46
47              ;       W23 - W26       BRIGHTNESS INFORMATION SELECT FOR
48              ;                       Z-AXIS PULSE AS FOLLOWS:
49
50              ;                       W23, W24 IN = BRIGHTNESS INFO IN BITS
51              ;                                     14-15 OF DAC X DATA WORD.
52
53              ;                       W25, W26 IN = BRIGHTNESS INFO IN BITS
54              ;                                     14-15 OF DAC Y DATA WORD.
55              ;                       (ONLY ONE PAIR MAY BE INSERTED).
```

```
10063 .MAIN
01              ;       W27             SELECT WHETHER Z-AXIS PULSE IS
02              ;                       POSITIVE OR NEGATIVE GOING. NO
03              ;                       JUMPER SELECTS NEGATIVE GOING.
04              ;                       W27 IN = POSITIVE GOING. QUIESCENT
05              ;                       DC LEVEL OF Z-AXIS SIGNAL IS SET
06              ;                       BY R27 (SEE BELOW).
07              ;
08              ;       W28, W29        "DAC DATA VALID" HANDSHAKING SIGNAL
09              ;                       SELECT AS FOLLWS:
10              ;
11              ;                       W28 IN = TRUE HIGH
12              ;                       W29 IN = TRUE LOW
13              ;                       (ONLY ONE MAY BE INSERTED).
14              ;
15              ;       W30, W31        "DAC DATA READY" HANDSHAKING SIGNAL
16              ;                       SELECT AS FOLLOWS:
17              ;
18              ;                       W30 IN = TRUE HIGH
19              ;                       W31 IN = TRUE LOW
20              ;                       (ONLY ONE MAY BE INSERTED).
21              ;
22              ;       W32             IF INSERTED, A "LATE CONVERSION"
23              ;                       STATUS SIGNAL WILL SET DONE.
24              ;
25              ;       W33             Z-AXIS COUPLING SELECT AS FOLLOWS:
26              ;
27              ;                       W33 IN = DC COUPLING ON Z-AXIS
28              ;                       W33 OUT = AC COUPLING ON Z-AXIS
29              ;
30              ;       D/A CONVERTER POTENTIOMETER INFORMATION:
31              ;
32              ;       POTENTIOMETER           FUNTION
33              ;       -------------           -------
34              ;
35              ;       R43                     INTERNAL CLOCK FREQUENCY
36              ;                               (NOMINAL RANGE: 16 US - 190 US)
37              ;       R32                     Z-AXIS PULSE LENGTH
38              ;                               (NOMINAL RANGE: 4 US - 150 US)
39              ;       R27                     Z-AXIS DC BASE LEVEL ADJUST
40              ;                               (NOMINAL RANGE +/- 5 VDC)
41              ;       R1                      "X" D/A GAIN ADJUST
42              ;       R2                      "X" D/A OFFSET ADJUST
43              ;       R7                      "Y" D/A GAIN ADJUST
44              ;       R8                      "Y" D/A OFFSET ADJUST
```

```
10064 .MAIN
01              ;11.6   GENERAL INFORMATION:
02              ;
03              ;       THE FOLLOWING FORMAT IS ALWAYS USED IN THIS PROGRAM FOR
04              ;       OCTAL VALUES THAT ARE USED AS DATA, EITHER INPUT TO THE
05              ;       D/A CONVERTER OR OUTPUT FROM THE A/D CONVERTER.
06              ;
07              ;       DATA VALUES = XXXXXX - ONE FULL OCTAL WORD (16 BITS)
08              ;       DATA LEFT JUSTIFIED TO BIT 0 WITH ALL UNUSED BITS = 0.
09              ;
10              ;       ANALOG CONVERTER VALUE/DATA CORRESPONDANCE
11              ;       LEFT JUSTIFIED OCTAL DATA:
12              ;
13              ;                               OCTAL DATA EQUIVALENTS **
14              ;                               12-BIT A/D OR D/A CONVERTER
15              ;                              -------------------------
16              ;       ANALOG VALUE    UNIPOLAR            BIPOLAR
17              ;       ------------------------------------------------
18              ;       + FS - 1 LSB    177760              077760
19              ;       + 1/2 FS        100000              040000
20              ;       + 1 LSB         000020              000020
21              ;       0 (TRUE ZERO)   000000              000000
22              ;       - 1 LSB         ------              177760
23              ;       - 1/2 FS        ------              140000
24              ;       - FS + 1 LSB    ------              100020
25              ;       - FS            ------              100000
26              ;
27              ;       WHERE: FS = FULL SCALE VOLTAGE OF CONVERTER
28              ;              LSB = LEAST SIGNIFICANT BIT
29              ;
30              ;       ** THE ABOVE OCTAL DATA VALUES ARE FOR THE FOLLOWING:
31              ;       - UNIPOLAR VALUES: CODING = OFFSET BINARY
32              ;       - BIPOLAR VALUES: CODING = TWO'S COMPLEMENT
```

```
10065 .MAIN
01                ;       CODING CONVENTIONS (FOR OCTAL DATA VALUES):
02                ;
03                ;       OFFSET BINARY IS DEFINED AS CONVERTER DATA BIT 0
04                ;       (MOST SIGINIFICANT BIT OR MSB) = 0 AS A RESET VALUE.
05                ;       IN OFFSET BINARY, DATA VALUES SENT/RECEIVED ARE ABSOLUTE
06                ;       VALUES (MAGNITUDES ONLY). IN OTHER WORDS, THE LOWER
07                ;       VOLTAGES HAVE LOWER OCTAL CODES, AND THE HIGHER
08                ;       VOLTAGES HAVE HIGHER CODES WHERE 000000 = LOWEST CODE
09                ;       AND 177760 = HIGHEST CODE. (BIT 0 IS NOT A SIGN BIT).
10                ;       0 VDC (UNIPOLAR), -5 VDC (LOW RANGE BIPOLAR) OR -10 VDC
11                ;       (HIGH RANGE BIPOLAR) = LOWEST VOLTAGES AND +5 VDC (LOW
12                ;       RANGE UNIPOLAR/BIPOLAR) OR +10 (HIGH RANGE UNIPOLAR/BI-
13                ;       POLAR) = HIGHEST VOLTAGES.
14                ;
15                ;       TWO'S COMPLEMENT IS DEFINED AS CONVERTER DATA BIT
16                ;       0 (MSB) = 1 AS A RESET VALUE. IN TWO'S COMPLEMENT
17                ;       CODING, THE VALUES ARE "SIGNED", WITH BIT 0 = SIGN BIT.
18                ;       BIT 0 = 0 INDICATES "POSITIVE" VALUES, AND BIT 0 = 1
19                ;       INDICATES "NEGATIVE" VALUES. IN THE CASE OF UNIPOLAR
20                ;       CONVERTER VALUES (0-5 OR 0-10 VDC), HALF FULL
21                ;       SCALE (2.5 OR 5.0 VDC) BECOMES THE "000000" DATA POINT.
22                ;       VALUES BETWEEN 0 AND 2.5 (OR 5.0) HAVE BIT 0 = 1,
23                ;       AND VALUES BETWEEN 2.5 (OR 5.0) AND 5.0 (OR 10.0)
24                ;       HAVE BIT 0 = 0.
25                ;
26                ;       (I.E. 100000 = 0 VDC, 177760 = 1/2 FULL SCALE - 1
27                ;       LSB, 000000 = 1/2 FULL SCALE, 000020 = 1/2 FULL SCALE
28                ;       + 1 LSB AND 077760 = FULL SCALE; WHERE FULL SCALE =
29                ;       +5 VDC LOW RANGE OR +10 VDC HIGH RANGE UNIPOLAR).
30                ;
31                ;       FOR THE BIPOLAR CASE, 0 VDC = 000000 IS THE TRUE
32                ;       ZERO POINT. VOLTAGES IN THE RANGE OF 0 TO +5 (OR +10)
33                ;       VDC HAVE POSITVE OCTAL CODES (BIT 0 = 0 WITH 077760 =
34                ;       + FULL SCALE) AND VOLTAGES IN THE RANGE OF -5 (OR -10)
35                ;       TO 0 VDC HAVE NEGATIVE OCTAL CODES (BIT 0 = 1 WITH
36                ;       100000 = - FULL SCALE). THEY ARE TRUE SIGNED NUMBERS.
37                ;
38                ;       THEREFORE, WHEN EITHER ONE OF THE FOLLOWING CASES
39                ;       OCCUR, FOR THE DATA VALUES SHOWN, SIMPLY COMPLEMENT
40                ;       BIT 0 (THE MSB) TO GET THE TRUE DATA VALUES:
41                ;       - UNIPOLAR W/TWO'S COMPLEMENT CODING (MSB=1)
42                ;       - BIPOLAR W/OFFSET BINARY CODING (MSB=0)
43                ;
44                ;       NOTE THAT EACH OF THE D/A CHANNELS, "X" AND "Y", AND
45                ;       THE A/D CONVERTER HAVE THEIR OWN CODING TYPES.
46                ;       THEY WILL NOT NECESSARILY BE THE SAME. SEE SECTIONS
47                ;       11.5.1 AND 11.5.2 FOR INFORMATION ON SELECTION OF
48                ;       CODING TYPES FOR THE A/D AND D/A CONVERTERS. IN THE
49                ;       CASE OF THE A/D, THE PROGRAM DETERMINES THE CODING
50                ;       TYPE BY RESETING THE A/D DATA REGISTER AND READING
51                ;       THE STATE OF A/D DATA BIT 0, WHICH IS THE CODING BIT.
52                ;       THE INFORMATION MUST BE INPUT BY THE OPERATOR IN THE
53                ;       CASE OF THE D/A.
```

```
10066 .MAIN
01                ;       THE FOLLOWING IS A TABLE OF DATA WORD FORMATS FOR THE
02                ;       A/D AND D/A CONVERTERS:
03                ;
04                ;       TYPE            #BITS   SIGN BIT  MSB   LSB     RES
05                ;       ----            -----   --------  ---   ---     ---
06                ;       UNIPOLAR         12       NONE     0     11      12
07                ;       BIPOLAR          12        0       1     11      12
08                ;
09                ;       MSB/LSB = MOST/LEAST SIGNIFICANT BITS.
10                ;       RES = RESOLUTION = THE # OF ACTUAL DATA BITS PER DATA
11                ;       WORD (NOT INCLUDING THE SIGN BIT). 2**RES IS THE TOTAL
12                ;       # OF INCREMENTS THAT THE FULL SCALE VALUE CAN BE BROKEN
13                ;       DOWN INTO. FOR EXAMPLE, A 12-BIT A/D HAS 2**12. = 4096.
14                ;       POSSIBLE DATA VAULES.
15                ;
16                ;       THE FOLLOWING IS A TABLE OF ACTUAL RESOLUTION VALUES
17                ;       FOR THE A/D AND D/A CONVERTERS:
18                ;
19                ;       MODE            FULL SCALE      RESOLUTION      RANGE
20                ;       ----            ----------      ----------      -----
21                ;       UNIPOLAR          5V            1.22 MV/BIT     0 - 5
22                ;       UNIPOLAR          10V           2.44 MV/BIT     0 - 10
23                ;       BIPOLAR           5V            2.44 MV/BIT     +/- 5
24                ;       BIPOLAR           10V           4.88 MV/BIT     +/- 10
```

```
!0067 .MAIN
01                ;12.    SPECIAL NOTES/SPECIAL FEATURES:
02                ;         ~~~~~~~~~~~~~~~~~~~~~~~~~~~~
03
04                ;         SEE INDIVIDUAL TEST DESCRIPTIONS IN SECTION 7.2.
05                ;         SEE ALSO SECTION 10.
06
07                ;13.    RUN TIME:
08                ;         ~~~~~~~
09
10                ;         MINIMUM RUN TIME FOR BOTH PROGRAMS SHOULD BE 15 -
11                ;         30 MINUTES WITHOUT ERROR. THE D/A TO A/D LOOP AROUND
12                ;         TEST PRINTS AN "END OF PASS" MESSAGE EVERY 2 - 3
13                ;         MINUTES DEPENDING ON A/D AND D/A CLOCK FREQUENCIES
14                ;         AND IF NOT LOOPING ON AN ERROR.
```

```
!0068 .MAIN
01

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```