

TEXT LISTING

068-001113-01

PROGRAM

LP2 UNOVA BOARD & PRINTER
DIAGNOSTIC

TEXT TAPE

097-001113-01

ABSTRACT

THIS PROGRAM PROVIDES THE USER WITH THE TESTS NECESSARY FOR CHECKING OUT THE DASHER LP2 MICRONOVA CPU, 2K RAM, FIRMWARE, INTERRUPT STRUCTURE, AND MECHANISM.

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/ NAME1 DLP2.TX          PART NUMBER: 097-001113
/
/ DESCRIPTION: LP2 UNOVA BOARD & PRINTER DIAGNOSTIC
/
/ REVISION HISTORY:
/
/ REV.          DATE
/ 00          XX/XX/XX
/ 01          09/01/78
/
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/*****

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      .DD #
      PROGRAM NAME:
      -----
      CLP2.TX
      CASHIER LP2 DIAGNOSTIC PACKAGE

      REVISION HISTORY:
      -----
      REV 1

      MACHINE REQUIREMENTS:
      -----
      TO RUN THE DLP2 TESTS THE
      USER SHOULD HAVE ALL OF THE
      FOLLOWING:

      1) DASHIER LP2 TERMINAL
      2) HOST CPU (ANY DCC TYPE)
      WITH AT LEAST 8K OF MEMORY
      3) HOST TERMINAL ON DEVICE CODE
      10 AND 11 (CRT, TTY, DASHIER ETC.)

      FOR THE PURPOSES OF ERROR REPORTING,
      ONE OF THE FOLLOWING MUST BE AVAILABLE.

      1) MICRONOVA HAND HELD CONSOLE
      2) TERMINAL WITH DEVICE CODES
      10 AND 11 (CRT, TTY, DASHIER) WITH
      SPECIAL LP2 INTERFACE

      IN SPECIAL CASES WHERE A
      HOST CPU IS NOT AVAILABLE, OR IT
      IS DESIRED NOT TO DISTURB THE
      HOST, THE TESTS MAY BE LOADED
      DIRECTLY INTO THE LP2 VIA THE
      FIELD SERVICE CASSETTE. EITHER
      A HAND HELD CONSOLE OR A TERMINAL
      ON DEVICE CODES 10 & 11 (CRT, TTY,
      DASHIER ETC.) IS STILL REQUIRED.

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TEST REQUIREMENTS

THE PROGRAM WILL BE THOROUGHLY EXERCISED BY ANY CONFIGURATION LISTED IN THE MACHINE REQUIREMENTS.

WHILE IT IS NOT REQUIRED TO RUN THE TESTS IN ANY SPECIFIC ORDER, THE FOLLOWING SEQUENCE IS SUGGESTED.

THE USER SHOULD RUN THE ROM TEST FIRST. NEXT, THE MICRONOVA TESTS (LOGIC, ARITHMETIC, AND MEMORY) SHOULD BE RUN. THE FINAL TEST SHOULD BE CAUTO. COPER2 SHOULD ONLY BE RUN IF CAUTO FAILS, OR IF A SCOPE LOOP WITH DIAGNOSTIC CAPABILITIES IS DESIRED.

FOR CHECKING PRINT QUALITY AND SPECIAL FUNCTIONS, THE USER SHOULD RUN THE LP2 RELIABILITY PROGRAM (NOT INCLUDED IN DLP2).

SUMMARY:

THIS PROGRAM PROVIDES THE USER WITH THE TESTS NECESSARY FOR CHECKING OUT THE DASHER LP2 MICRONOVA CPU, 2K RAM, FIRMWARE INTERRUPT STRUCTURE, AND MECHANISM.

THE TESTS INCLUDED ARE:

- 0) LP2 ROM TEST
- 1) MICRO NOVA LOGIC TEST
- 2) MICRO NOVA ARITHMETIC TEST
- 3) MICRO NOVA MEMORY TEST
- 4) RUNS 1, 2, & 3
- 5) CAUTO (LP2 MECHANISM DIAGNOSTIC)
- 6) COPER2 (LP2 SCOPE LOOP DIAGNOSTIC)

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RESTRICTIONS

IN THE ROM TEST, CAUTO AND COPER2, THE LP2 RAM IS USED TO STORE MACHINE STATUS. IF THE LP2 WAS RESET UNDER PROGRAM CONTROL AT THE END OF THESE TESTS, MEMORY WOULD BE DESTROYED BEFORE THE USER HAD A CHANCE TO EXAMINE THE STATUS LOCATIONS. THEREFORE, AFTER RUNNING ANY OF THE PREVIOUSLY MENTIONED TESTS, THE LP2 MUST BE RESET BEFORE SELECTING ANOTHER TEST TO BE DOWN LINE LOADED. IF CAUTO IS BEING RUN, THE HOST PROCESSOR MUST BE STOPPED BEFORE RESETTING THE LP2. OTHERWISE, ERRONEOUS "CAUTO-END OF PASS" MESSAGES WILL BE PRINTED ON THE HOST TERMINAL.

ALTHOUGH BOTH CAUTO AND COPER2 ARE LABELED AS DIAGNOSTIC PROGRAMS, IT SHOULD BE NOTED THAT THESE TESTS DO NOT PERFORM A CHIP BY CHIP TEST ON THE LP2 BOARDS. ONLY THAT HARDWARE PERTAINING TO THE LP2 INTERRUPT STRUCTURE IS THOROUGHLY CHECKED. THE PRIMARY REASON FOR THIS IS THAT ANY PROGRAM RUNNING IN THE LP2 MICRONOVA CPU HAS AVAILABLE AS IT'S LINKS TO THE LP2 HARDWARE, ONLY THOSE SIGNALS WHICH CAN BE READ IN BY EXECUTING ONE OF THE LP2'S IN FUNCTIONS (SEE SECTION 12).

THERE ARE NO SPECIAL RESTRICTIONS REGARDING THE MICRO NOVA TESTS 1, 2, 3 OR 4. IN ALL CASES THE PRINTER MUST BE ON LINE AND READY.

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7) PROGRAM DESCRIPTION/THEORY OF OPERATION

ROM TEST

THE LP2 FIRMWARE IS CONTAINED IN

SIX 512X8 ROMS GIVING A TOTAL

CAPABILITY OF 1 1/2K 16 BIT WORDS.

THE FIRMWARE IS RESPONSIBLE FOR

INTERPRETING ALL INFORMATION COMING

FROM THE HOST. IF A ROM LOCATION

IS BURNED INCORRECTLY, IT IS QUITE

LIKELY THAT THE LP2 WILL MALFUNCTION.

IF THE BAD LOCATION(S)

HAPPENS TO BE IN AN AREA OF

CODE WHICH IS USED TO ACCEPT

A DOWN LINE LOADED PROGRAM,

THEN IT IS PROBABLE THAT THE

ROM TEST ITSELF WILL BE UNABLE

TO EXECUTE. HOWEVER, THE BAD

LOCATION MAY BE IN AN AREA

OF CODE WHICH IS RESPONSIBLE FOR

SELDON USED FEATURES. IN

THIS SITUATION THE ROM TEST PERFORMS

A VALUABLE SERVICE IN THAT IT

CAN VERIFY THE ROMS BEFORE

A BAD LOCATION IS EXECUTED.

THE TEST COMPUTES A STRAIGHT

CHECKSUM FOR EACH ROM AND

STORES THE RESULTS IN LOCATIONS 72-77

IN RAM. THE CHECKSUMS ARE THEN AVAILABLE

FOR USER INSPECTION.

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THE MICRO NOVA TESTS 1,2,3 OR 4
ARE BASICALLY THE SAME AS THE CORRESPONDING
TESTS THAT EXIST FOR A MICRO NOVA
CPU HOST. VARIOUS MINOR ALTERATIONS HAVE
BEEN MADE TO ADAPT THESE TESTS
TO THEIR NEW EXECUTION ENVIRONMENT.

TESTS 1 AND 2 WERE FIRST
ASSEMBLED SEPARATELY. IN FACT, TEST
1 WAS DIVIDED INTO 2 SEGMENTS, EACH OF
WHICH WAS ASSEMBLED SEPARATELY, SO THAT
EACH SEGMENT OCCUPIES LESS THAN
2K OF MEMORY. (WHEN TEST 1 IS
EXECUTED 2 DOWNLINE LOADS ARE
PERFORMED.) THE LISTING FILES
FOR EACH OF THESE SEPARATE
ASSEMBLIES WAS THEN EDITED BY
AN INSPED EDIT PROGRAM THAT DID
THE FOLLOWING:

- 1) FIRST LINE ON EVERY PAGE
AND ALL LINE NUMBERS WERE ERASED.
- 2) MEMORY LOCATIONS (ALL ASSEMBLIES
BEGIN AT LOCATION 5) WERE MOVED TO
FOLLOW MEMORY CONTENTS ON EACH
LISTING LINE.
- 3) A COMMENT CHARACTER (J) WAS
PLACED BETWEEN THE MEMORY
CONTENTS AND THE MEMORY LOCATION
ON EACH LISTING LINE.

THE EDITED LISTING FILES WERE
THEN INSERTED INTO THE DLP2 DIAGNOSTIC
SOURCE FILE. THEREFORE, WHEN DLP2.SR IS ASSEM-
BLED THE ABOVE MENTIONED INSERTS
ARE TREATED AS CONSTANTS (ACTUALLY
THEY ARE THE MEMORY CONTENTS FROM THE LISTING
FILE) WITH EVERYTHING ELSE BEING COMMENTS.
THIS EXPLAINS THE UNIQUE FORMAT OF
TESTS 1 AND 2 IN THE DLP2 DIAGNOSTIC
LISTING. THE FIRST FIELD FOLLOWING THE (J) IS THE
LOCATION IN MICRONOVA MEMORY OF THE INSTRUCTION
OR DATA WORD PRECEDING THE (J).

TEST 3 HAS A STANDARD LISTING FORMAT IN THE
DLP2 DIAGNOSTIC LISTING EXCEPT THAT EVERY
INSTRUCTION OR DATA WORD LINE HAS A (J)
FOLLOWED BY THE LOCATION IN MICRONOVA
MEMORY INTO WHICH THAT INSTRUCTION OR
DATA WORD GETS DOWNLINE LOADED. THIS LOCATION
FIELD IS FOLLOWED BY A (*).

TEST 1 (LOGIC TEST):
THIS IS A FUNCTIONAL TEST OF THE LOGIC
USED TO IMPLEMENT THE MICRO-NOVA
INSTRUCTION SET. ALSO INCLUDED IS A
MINIMUM LEVEL TEST OF THE CPU I/O

LOCATION	CHECKSUM	CHIP #	CG PART
72	LOW ORDER 1/2K, LOWER BYTE	U44	100-1539
73	LOW ORDER 1/2K, UPPER BYTE	U61	100-1542
74	MIDDLE 1/2K, LOWER BYTE	U45	100-1540
75	MIDDLE 1/2K, UPPER BYTE	U62	100-1543
76	UPPER 1/2K, LOWER BYTE	U46	100-1541
77	UPPER 1/2K, UPPER BYTE	U63	100-1544

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INSTRUCTIONS AND PROGRAM INTERRUPT.

TEST 2 (ARITHMETIC TEST):
THIS IS A PROGRAM DESIGNED TO EXERCISE THE
ARITHMETIC AND LOGICAL INSTRUCTIONS OF
THE MICRO NOVA CPU. THE PROGRAM CONSISTS
OF A NUMBER OF SUBROUTINES PERFORMING
VARIOUS OPERATIONS ON SETS OF PSEUDO RANDOM
NUMBERS. SOME ROUTINES PERFORM MORE THAN
ONE OPERATION, SUCH AS TAKING THE SQUARE
ROOT OF A SQUARED NUMBER. WHEN THE OP-
ERATOR QUESTIONS WHICH RESULT IS CORRECT
THE OPERATIONS MAY BE PERFORMED WITH PENCIL
AND PAPER ON THE ORIGINAL NUMBERS.
BECAUSE THIS PROGRAM IS USED AS A FINAL
TEST OF THE ARITHMETIC AND LOGICAL OP-
ERATIONS IT IS COMPLEX AND DIFFICULT TO
TROUBLE-SHOOT. IT IS, THEREFORE, SUGGESTED
THAT THIS PROGRAM BE RUN AFTER TEST
1 (LOGIC TEST).

TEST 3 (MEMORY TEST):
THIS TEST WILL CHECKOUT MEMORIES
OF MICRO NOVA BOARDS CONSISTING
OF 2K OR 4K MOS RAMS.
THE DIAGNOSTIC IS DESIGNED TO TEST
1 AND 4K MOS RAMS AND THE CIRCUITRY
AROUND THEM. 4K RAMS MANUFACTURED
BY DATA GENERAL ARE TREATED AS FOUR
1K RAMS. THE TEST STARTS BY CHECKING
SIMPLE HARDWARE AND AS IT PROGRESSES
MORE COMPLEX TESTING IS DONE. IF
RELOCATION IS ALLOWED THEN THE PRO-
GRAM CANNOT BE STOPPED IN THE
MIDDLE AND RESTARTED AT LOCATION 5.

TEST 4:
THIS TEST WILL CAUSE THE CONTINUOUS
EXECUTION OF THE SEQUENCE: TEST 1,
TEST 2 AND TEST 3.

CAUTION:
CAUTION IS A MECHANISM DIAGNOSTIC
DESIGNED TO CHECK THE LP2
INTERRUPT STRUCTURE AND WORSE CASE
MOVEMENT PATTERNS.

THE PROGRAM FIRST TESTS
SIMPLE HORIZONTAL & VERTICAL MOVEMENTS.
AS THE TEST PROCEEDS THE MOVEMENTS
GROW PROGRESSIVELY MORE COMPLEX.
DURING THE TESTING, THE PROGRAM
MONITORS LP2 INTERRUPT TIMING,
SEQUENCE, AND RESETTING FOR
BOTH HORIZONTAL AND VERTICAL MOVEMENTS.
SINCE THE PROGRAM IS DESIGNED TO
LOOP, IT CAN BE USED AS A
MECHANISM RELIABILITY TEST. IF
AT ANY TIME, AN INTERRUPT DOES
NOT COME AT THE RIGHT TIME, OR

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DOES NOT GET RESET, OR IF AN ILLEGAL
INTERRUPT OCCURS, THE TEST WILL
TERMINATE, AND ALL MOTOR MOVEMENT
WILL CEASE.

COPER2:
IF THE LP2 MOTOR MOVEMENTS ARE
NOT FUNCTIONING CORRECTLY, IT MAY BE
NECESSARY TO MAKE ADJUSTMENTS TO
THE TRANSDUCERS WHICH GENERATE
THE INTERRUPTS TO THE LP2 MICRONOVA
CPU. IN SUCH CASE, THE TECHNICIAN
DESIRES A MEANS OF PRECLUDING
MOTOR MOVEMENT. SPECIFICALLY
HE WOULD LIKE THE ABILITY TO SET
UP ANY SCOPE LOOP HE WISHES.
HORIZONTAL OR VERTICAL. COPER2
PROVIDES THE MEANS OF SETTING
UP THESE SCOPE LOOPS. IN ADDITION,
COPER2 IS CAPABLE OF MAKING
DIAGNOSTIC ERROR REPORTS ON THE
INTERRUPT SECTION OF THE LP2 HARDWARE.
BY USING THE COPER2 MAEMONICS
THE TECHNICIAN CAN SET UP
THESE DIAGNOSTIC SCOPE LOOPS
QUICKLY AND EASILY.

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OPERATING MODES/SWITCH SETTINGS
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THE ROM TEST, AUTO,
AND COPER2 REQUIRE NO EXTRA
SWITCH SETTINGS.
TEST 1 HAS NO SWITCH SETTINGS.
TEST 2 HAS A SREG SWITCH
WHICH THE PROGRAM REQUESTS THE
USER TO SET AS FOLLOWS:

USER INPUT      INTERPRETATION
-----
0 OR CR        LOOP ON ERROR
4000          HALT ON ERROR

TEST 3 HAS THE SAME SREG SWITCH
AS ABOVE AND ALSO THE FOLLOWING
USREG SWITCH:

BIT(S)  OCTAL  BINARY  INTERPRETATION
        VALUE  VALUE
0       100000  1      CHECK THE ENTIRE MEMORY
        MEMORY BOUNDARIES WILL BE DEFINED
        BY THE OPERATOR.
2       020000  0      ALLOW THE RELOCATION OF THE PROG
        TO THE HIGHEST AVAILABLE MEMORY.
        THIS DOUBLES TEST EXECUTION TIME
        SUPPRESS RELOCATION
3       010000  1      ONLY ROW/COLUMN GALLOPING TEST
        IS TO BE PERFORMED, WITH NO RELO
        EXECUTION TIME IS 1.5 MINUTES.
        ENABLE LONG GALLOPING TEST.
        WITH NO RELOC. EXECUTION TIME
        IS 6 MINUTES.
11      000020  1      DO NOT LOOP ON A TEST
        LOOP ON THE TEST SPECIFIED BY
        BITS 12-15
        TEST NUMBER.
        ONLY TEST DEFINED BY BITS 12-15
        THROUGH THE LAST TEST WILL BE
        EXECUTED.

OPERATING PROCEDURE/OPERATOR INPUTS
-----
1) RUNNING WITH A HOST CPU

DLP2 STARTS AT 200. IF THERE
IS NO REAL TIME CLOCK IN THE CPU,
THE USER WILL HAVE TO ANSWER THE
"HTO BAUD RATE =" QUESTION
BEFORE PROCEEDING. THE USER SHOULD
TYPE IN THE BAUD RATE OF THE HOST TERMINAL
(110 FOR A TTY) FOLLOWED BY A CARRIAGE
RETURN. THE ANSWER TO THIS QUESTION
IS USED TO DETERMINE THE LENGTH OF
INTERNAL PROGRAM DELAYS.

IF THERE IS A REAL TIME CLOCK IN
THE CPU, THIS QUESTION WILL NOT APPEAR.

AFTER ANSWERING THE QUESTION, OR IF
THERE IS REAL TIME CLOCK PRESENT
IN THE CPU, THE HOST TERMINAL WILL
PRINT OUT THE AVAILABLE TESTS FOLLOWED
BY THE QUESTION "WHICH TEST NUMBER?".

THIS QUESTION SHOULD BE ANSWERED
WITH THE SELECTED TEST NUMBER
FOLLOWED BY A CARRIAGE RETURN.
AN ANSWER OTHER THAN 0-7 (THE
AVAILABLE TEST NUMBERS) WILL RESULT
IN THE QUESTION BEING REPEATED.

WHEN THE QUESTION IS ANSWERED WITH
A VALID TEST NUMBER, THE SELECTED TEST
WILL BE DOWN LOADED INTO THE
LP2 MEMORY AND EXECUTED.

THE FOLLOWING DESCRIBES THE ACTION
THE USER SHOULD TAKE AFTER SELECTING
EACH TEST:

        0) ROM TEST

UPON SELECTION,
THE ROM TEST IS DOWN LOADED
INTO THE LP2 MEMORY AND
EXECUTED. THERE IS NO OPERATOR INPUT
REQUIRED.

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TEST 1 (LOGIC TEST):

THE LP2 MUST BE RESET IN ORDER FOR TEST 1 TO DOWNLINE LOAD. IF TESTS 1,2 OR 3 HAVE BEEN EXECUTED SUCCESSFULLY JUST PREVIOUS TO THIS SELECTION THEN THE USER NEED NOT RESET THE LP2 BECAUSE THESE TESTS DO A RESET UPON THEIR SUCCESSFUL CONCLUSION. AFTER TEST 1 IS SELECTED IT IDENTIFIES ITSELF, THEN OUT AND A SPECIAL LOADER ARE DOWNLINE LOADED TO THE LP2 AND THE SPECIAL LOADER PROGRAM IS EXECUTED AND THE HOST STARTS DOWNLINE LOADING TEST1, BEGINNING AT LOCATION 5 IN THE LP2 MEMORY. THIS IS ALSO THE STARTING ADDRESS OF TEST 1. WHEN THE DOWNLINE LOADING IS COMPLETED THE HOST SETS THE LP2 BUSY LINE BY DOWNLINE ENTERING A WAIT LOOP. WHILE THIS IS HAPPENING IN THE HOST THE SPECIAL LOADER PROGRAM TRANSFERS CONTROL TO LOCATION 5 (STARTING ADDRESS OF TEST 1) AND EXECUTION OF THE TEST BEGINS. IF NO ERROR CONDITION OCCURS THE TEST CONCLUDES BY DOING AN "IN2" (THEREBY RESETTING THE LPT BUSY LINE,) AND A RESET OF THE PRINTER.

THE HOST PROGRAM FINISHES ITS WAIT LOOP (UNIQUE FOR EACH OF TESTS 1,2 AND 3) AND CHECKS THE LP2 BUSY LINE. IF IT IS RESET IT DISPLAYS "PASSED" ON THE HOST TERMINAL FOLLOWED BY THE QUESTION "WHICH TEST NUMBER?".

THE ABOVE DESCRIPTION APPLIES ALSO TO TESTS 2 AND 3.

BECAUSE TEST 1 OCCUPIES MORE THAN 2K, IT IS DOWNLINE LOADED IN 2 SEGMENTS. AFTER THE FIRST SEGMENT RUNS SUCCESSFULLY (I.E. THE HOST SENSES A RESET BUSY LINE) THE SECOND SEGMENT IS DOWNLINE LOADED AND EXECUTED. THIS IS DONE AUTOMATICALLY AND REQUIRES NO OPERATOR ACTION.

TEST 2 (ARITHMETIC TEST):

SEE PROCEDURE FOR TEST 1 ABOVE. FOR TEST 2 THE USER MUST SUPPLY THE "SREG" AS DESCRIBED IN SECTION 8 ABOVE.

TEST 3 (MEMORY TEST):

SEE PROCEDURE FOR TEST 1 ABOVE. FOR TEST 3 THE USER MUST SUPPLY THE "SREG" AND "USREG" AS

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DESCRIBED IN SECTION 8 ABOVE.

TEST 4:

SEE PROCEDURES DESCRIBED ABOVE. AFTER THE FIRST PASS THIS TEST WILL LOOP INDEFINITELY DISPLAYING "END" ON THE HOST TERMINAL AFTER EVERY PASS.

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CAUTO:

UPON SELECTION, CAUTO IS
DOWN LINE LOADED INTO THE LP2 MEMORY
AND EXECUTED. THERE IS NO OPERATOR
INPUT REQUIRED.

COPER2:

4) MONITOR MODE

ONCE STARTED COPER2 WILL RESPOND WITH A CARRIAGE RETU
LINE FEED AND THEN THE CHARACTER "A". THE "A" INFORM
THE OPERATOR THAT COPER2 IS IN THE MONITOR.

THE MONITOR ALLOWS THE USER TO ENTER SIMPLE MNEMONIC STR
WHICH INSTRUCT THE LP2 TO MOVE IN CERTAIN WAYS. AN EX-
PLANATION OF THE MONITOR COMMANDS FOLLOWS.

A) SPEED

- 1) 24 CHAR/SEC = INCREMENTAL = I
- 2) 110 CHAR/SEC = SLOW = S
- 3) 180 CHAR/SEC = FAST = F

DEFAULT IS NO MOTION

B) DIRECTION

- 1) RIGHT = R
- 2) LEFT = L

DEFAULT IS TO THE RIGHT

VERTICAL MOTION

VERTICAL MOTION = V

BY TYPING A "V" THE USER INSTRUCTS THE LP2 TO STOP
THE LINE FEED MOTOR THE NUMBER OF TIMES REQUIRED
TO PRODUCE N LINE FEEDS, WHERE N IS A NUMERICAL ARGU-
MENT SET BY THE USER.

NUMERICAL ARGUMENT

IN ANY TEST, A NUMERICAL ARGUMENT (N) FROM
0 TO 255 MAY BE ENTERED ALONG WITH THE COM-
MAND. IN THE HORIZONTAL CASE, N IS THE NUM-
BER OF CHARACTERS MOVED, IN THE VERTICAL
CASE, N IS THE NUMBER OF LINE FEEDS. IF 0
IS ENTERED, OR IF NO NUMERICAL ARGUMENT IS
ENTERED, N WILL BE INFINITY.

ALTERNATE FLAG

IF THE LETTER A IS ENTERED, THE ALTERNATE
FLAG WILL BE SET. IN THE HORIZONTAL CASE,
THIS INSTRUCTS THE LP2 TO MOVE THE PRINT

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HEAD BACK TO ITS ORIGINAL POSITION AFTER
A TEST HAS BEEN COMPLETED, AND, TO THEN
LOOP ON THE TEST. THE ALTERNATING MOTION
WILL PROCEED INDEFINITELY. IN THE ALTERNATE
MODE, THE PRINT HEAD WILL MOVE FIRST IN THE
DIRECTION GIVEN IN THE INSTRUCTION.

DON'T CHECK 10 PRINT INTERRUPTS PER START CHARACTER

BY TYPING AN "X" THE USER CAN CANCEL THE
CHECKING OF 10 PRINT INTERRUPTS FOR EACH
START CHARACTER.

NOTE: IN THIS MODE, THE PRINT HEAD MAY
NOT STOP TRYING TO MOVE IF IT HITS EITHER
END OF THE CARRIAGE.

TERMINATING COMMAND STREAM - A CARRIAGE RETURN WILL
TERMINATE THE COMMAND STREAM & START ITS EXECUTION

10015 .MAIN

10016 .MAIN

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01 ORDER OF MNEMONICS =
02
03 ORDER DOES NOT MATTER WHEN ENTERING MNEMONICS. EVEN
04 NUMERICAL ARGUMENTS DO NOT HAVE TO BE ENTERED SE-
05 QUENTIALLY.
06
07 STOP ANY TEST:
08
09 ANY TEST CAN BE TERMINATED BY HITTING ANY KEY OF THE
10 KEYBOARD.
11
12 SUMMARY OF MONITOR COMMANDS
13
14 I = INCREMENTAL = 24 CHAR/SEC
15 S = SLOW = 110 CHAR/SEC
16 F = FAST = 180 CHAR/SEC
17
18 R = RIGHT
19 L = LEFT
20
21 V = VERTICAL
22
23 A = ALTERNATE
24
25 X = DON'T CHECK TO PRINT INTERRUPTS/START CHAR
26
27 EXAMPLES:
28
29 100 RIGHT AT INCREMENTAL SPEED
30
31 100RI (CR)
32
33 100 RIGHT AT SLOW SPEED
34
35 100RS (CR)
36
37 100 RIGHT AT FAST SPEED
38
39 100RF
40
41 100 TO THE RIGHT AT FAST SPEED AND ALTERNATE
42
43 100RFA
44
45 100 TO THE RIGHT AT FAST SPEED AND ALTERNATE=DON'T CHECK
46
47 100RFAX
48
49 INFINITE VERTICAL
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51 V (CR)
52
53 100 LINE FEEDS
54
55 100V (CR)
56
57

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01 PROGRAM OUTPUT/ERROR DESCRIPTION
02 -----
03 ROM TEST
04
05 THE TEST TAKES LESS THAN 1 SECOND
06 TO EXECUTE. UPON COMPLETION, THE
07 STARTING ADDRESS OF THE CHECKSUM
08 STORAGE AREA (72) IS STORED IN THE HAND
09 HELD CONSOLE DISPLAY, AND A COMPLETION
10 MESSAGE IS PRINTED ON THE POST
11 TERMINAL.
12
13 THE "WHICH TEST NUMBER?"
14 QUESTION IS THEN PRINTED OUT ON THE
15 HOST TERMINAL, BEFORE SELECTING
16 AND DOWN LINE LOADING THE NEXT
17 TEST, THE LP2 MUST BE RESET (SEE
18 SECTION 12)
19
20 AT THE SAME TIME, ODT IS STARTED
21 ON THE LP2 TTY. IF THE TTY
22 DOES NOT EXIST, THE PROGRAM
23 WAITS FOR THE USER TO HIT
24 THE "RESET" KEY ON THE HAND HELD
25 CONSOLE. THIS WILL RESULT IN THE PROGRAM
26 ENTERING THE HAND HELD CONSOLE SOFTWARE,
27 EITHER WAY, THE CHECKSUMS CAN NOW BE
28 READ FROM THE LP2 MEMORY AND CHECKED AGAINST
29 THE CIRCULATED ONES.
30
31 TEST 1:
32 IF AN ERROR CONDITION IS FOUND
33 THE MESSAGE "FAILED. TO DOWNLINE LOAD RESET
34 THE PRINTER." WILL BE DISPLAYED ON THE
35 HOST TERMINAL. IF A TTY IS CONNECTED
36 TO THE LP2 MICRO NOVA BOARD "ODT"
37 WILL BE GIVEN CONTROL AND THE
38 OPERATOR CAN DETERMINE THE PC OF
39 THE INSTRUCTION THAT DETECTED THE
40 ERROR BY EXAMINING AL3. CONSULT
41 THE LISTING AT THIS ADDRESS
42 (THE ADDRESS FOLLOWS THE "I"
43 ON EVERY LINE IN THE LISTING) FOR
44 PROBABLE CAUSES OF THE FAILURE. CONSTRUCT
45 A LOOP THAT WILL REPEAT THE FAILURE
46 AND SCOPE AS REQUIRED. BECAUSE TEST
47 1 CONSISTS OF 2 CONNLINE LOADED
48 SEGMENTS THE OPERATOR MUST LISTEN
49 FOR THE LP2 RESET BELL TO DETERMINE
50 IF THE FAILURE OCCURRED IN SEGMENT
51 1 (MNL1) OR SEGMENT 2 (MNL2).
52
53 IF A TTY IS NOT CONNECTED
54 TO THE LP2 TEST 1 WILL ENABLE
55 MCC INTERRUPTS AND ENTER AN INDEFINITE
56 LOOP. THE USER CAN HIT STOP KEY ON THE
57 HHC AND USE THE HHC INSTEAD OF
58 A TTY TO INVESTIGATE THE ERROR
59 AS DESCRIBED ABOVE.
60

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10)

0017 .MAIN

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TEST 2:
SAME AS TEST 1, IN TEST
2 IF 0 OR CR ARE USED FOR
"SRG" THE TEST WILL LOOP FROM
THE BEGINNING OF THE TEST (LOC.5)
TO THE LOCATION WHERE THE ERROR
OCCURS, REGARDLESS OF "SRG" THE
PC, AC0, AC1, AC2 AND THE SUBTEST
NUMBER WHERE THE ERROR OCCURRED (TSN?)
ARE STORED IN LOCATIONS 28 THRU 24.

TEST 3:
THE PROGRAM IS DESIGNED TO
ENCOUNTER 2 TYPES OF ERRORS.

FATAL ERROR - THIS ERROR IS CAUSED
WHEN PROGRAM FLOW IS OUT OF SEQUENCE.
THIS ERROR OVERRIDES THE "SRG" SWITCH
SETTING AND THE MICRONOVA PROGRAM WAITS
FOR A MHC INTERRUPT. AC0, AC1, AC2 AND THE
PC ARE SAVED IN MICRONOVA MEMORY LOCATIONS
21 THRU 24 RESPECTIVELY.

SOFT ERROR - THIS ERROR IS CAUSED
UPON ENCOUNTERING A FAULT IN THE
MEMORY. THE PROGRAM WILL ACT AS
IN TEST 2 EXCEPT THAT LOOPING
WILL BE DONE ONLY ON THE SUBTEST
THAT DETECTED THE ERROR. AC0, AC1,
AC2, SUBTEST NUMBER AND PC
ARE SAVED IN LOCATIONS 28 THRU 24.
AC0= THE DATA FOUND. AC1= THE EXPECTED
DATA AND AC2= THE FAILING MEMORY
LOCATION. THE MICRONOVA PROGRAM WAITS FOR A MHC INTERRUPT

TEST 4:
SEE WRITEUP PERTAINING TO
THE TEST THAT FAILED. DETERMINATION
OF THE FAILING TEST IS BY THE LPT
RESET BELL. THIS BELL IS SOUNDED FOUR TIMES
PER TEST 4 PASS: TWICE FOR TEST 1, ONCE FOR TEST
2 AND ONCE FOR TEST 3.

0018 .MAIN

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CAUTO:
THE ERROR REPORTING FOR CAUTO
IS IDENTICAL TO THAT OF COPER2
COPER2:
WHEN COPER2 FLAGS AN ERROR,
IF, DURING ANY TEST, AN ERROR IS DETECTED, THE PROGRAM
WILL LOAD THE ERROR CODE INTO ERRNM (LOCATION 2124) AND
ALSO INTO THE HAND HELD CONSOLE DISPLAY. THEN THE
PROGRAM WILL TRAP TO CDT.

THE FIRST THING THAT SHOULD BE DONE IS TO EXAMINE THE
ERRNM LOCATION. THE INFORMATION STORED HERE DESCRIBES
THE TYPE OF ERROR. (SEE ERROR CODES)

ERROR CODE	MEANING
000000	HORIZONTAL TEST PASSED
000001	VERTICAL TEST PASSED
020000	VERTICAL REAL TIME CLOCK INTERRU
10000	TICK INTERRUPT NOT RESET
4000	ILLEGAL INTERRUPT IN LINE FEED T
1000	VERTICAL INTERRUPT NOT RESET
400	START CHARACTER INTERRUPT NOT RE
200	PRINT INTERRUPT NOT RESET
100	HORIZONTAL REAL TIME CLOCK INTER
40	ILLEGAL HORIZONTAL INTERRUPT
20	DIDNIT GET 10 PRINT INTERRUPTS /

10019 .MAIN

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DEBUG HELP

ROM TEST-

NO DEBUG TOOLS ARE AVAILABLE FOR THIS TEST

TEST 1
SEE SECTION 10 ABOVE, ODT
IS CONTAINED IN "DLPT". IT RESIDES
AT LABEL "ENTER" IN THE HOST AND
AT ADDRESS 3333 IN THE MICRO NOVA
MEMORY WHEN EITHER SECTION OF TEST
1 IS DOWNLINE LOADED.

TEST 2
SEE SECTION 10 AND WRITEUP FOR
TEST 1 IN THIS SECTION.

TEST 3
SEE SECTION 10. ODT IN MICRONOVA MEMORY IS DESTROYED BY
EXECUTION OF TEST 3 AND THEREFORE ONLY
THE HHC IS OF ANY USE IN DEBUGGING.

TEST 4
SEE SECTION 10 AND WRITEUP
FOR TEST 1 IN THIS SECTION.

CAUTO

THE DEBUG TOOLS FOR CAUTO ARE IDENTICAL TO
THAT OF COPER2.

COPER2

THERE ARE SEVERAL KEY STATUS LOCATIONS TO EXAMINE AFTER
LOOKING AT ERRNH.

WHILE THE PROGRAM IS EXECUTING, DLP2 STATUS IS CONSTANTLY
BEING MONITORED & STORED. WHEN AN ERROR CONDITION ARISE
ODT WILL BE CALLED. FROM THE ODT, THESE KEY LOCATIONS C
BE EXAMINED AND INTERPRETTED.

LOUT6 - THIS LOCATION STORES THE LAST OUT6 INSTRUCTION I
BY THE PROGRAM. THE USER CAN TELL WHICH DEVICE WAS THE
TO BE RESET AFTER AN INTERRUPT.

LOUT5 - THIS LOCATION STORES THE LAST OUT5 ISSUED BY THE
PROGRAM. THE USER CAN EXAMINE THE STATUS OF SEVERAL BIT
TO OBTAIN INFORMATION ABOUT SPEED, DECELERATING, DIRECTI
& VERTICAL MOTION.

LFcnt - THIS LOCATION STORES THE NUMBER OF LINE FEEDS TH
NEED TO BE PERFORMED TO COMPLETE THE VERTICAL TEST.

LFsct - THIS LOCATION STORES THE LAST OUT5 ISSUED TO STE
THE LINE FEED MOTOR.

LFfct - THIS LOCATION STORES THE NUMBER OF VERTICAL INTE

0020 .MAIN

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RECEIVED BETWEEN. EACH LINE FEED SEQUENCE START

LFspt - THIS LOCATION POINTS TO THE LAST OUT5 INSTRUCTIO
WHICH WAS SENT OUT DURING THE VERTICAL TEST.

PICnt - THIS LOCATION STORES THE NUMBER OF PRINT INTERRU
RECEIVED. AFTER EACH START CHARACTER

SCnt - THIS LOCATION STORES THE NUMBER OF START CHARACT
WHICH MUST BE RECEIVED TO COMPLETE THE HORIZONTAL TEST.

SCIEZ - THIS FLAG WILL EQUAL 1 WHEN THE NUMBER OF START
CHARACTERS RECEIVES IS EQUAL TO THE NUMERICAL ARGUMENT N

PICEP - THIS LOCATION WILL EQUAL ONE EVERY TIME FOUR OR
MORE PRINT INTERRUPTS HAVE BEEN RECEIVED AFTER THE LAST
START CHAR.

LN1 - THIS LOCATION STORES THE DATA RECEIVED BY EXECUTI
THE LAST IN 1 INSTRUCTION. FROM THIS DATA, THE USER CAN
DETERMINE THE SOURCE OF THE LAST INTERRUPT RECEIVED BEFO
THE ERROR

LIRst - THIS LOCATION STORES THE LAST IN 1 PERFORMED AFT
AND INTERRUPT HAS BEEN RESET. WHEN AN INTERRUPT OCCURS,
IT IS RESET. THEN THE PROGRAM DOES ANOTHER IN1 TO CHECK
AND SEE IF THE INTERRUPT WAS ACTUALLY RESET. IF NOT, AN
ERROR IS FLAGGED. THIS LOCATION CAN BE EXAMINED IF THE
ERROR CODE IN ERRNH IS ONE WHICH SIGNIFIES AN INTERRUPT
BEING RESET. THE USER CAN VERIFY THIS FACT BY LOOKING A
LN1 AND LIRst.

10021 .MAIN

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1) TIME DELAY ARGUMENT

IN ALTERNATING MODE, THE PRINT HEAD MUST COME TO A STOP FOR A CERTAIN AMOUNT OF TIME BEFORE CHANGING DIRECTION. SINCE EVERY MECHANISM IS SLIGHTLY DIFFERENT THE AMOUNT OF TIME THE PRINT HEAD MUST BE STOPPED MAY VARY BETWEEN MACHINES. LOCATION 1336 CONTAINS THE TIME DELAY ARGUMENT FOR THIS ALTERNATING SETTLING TIME. THE ARGUMENT IS OCTAL AND REPRESENTS THE NUMBER OF MILLISECONDS THE PRINT HEAD WILL WAIT BEFORE CHANGING DIRECTION THE ARGUMENT MAY BE BETWEEN 1 AND 17777. THE ARGUMENT IS ORIGINALLY SET AT 62 WHICH IS DECIMAL 50 AND THIS GIVES A 50 MILLISECOND DELAY.

1A)

DURING THE EXECUTION OF CAUTO, THE LP2 MOTOR MOVEMENT MAY REVERSE ITS DIRECTION IN SUCCESSIVE TESTS. TO MAKE SURE THE MOTOR MOVEMENT HAS THE PROPER SETTLING TIME NEEDED FOR DIRECTION CHANGE, A TIME DELAY HAS BEEN INTRODUCED BETWEEN EACH SUCCESSIVE CAUTO TEST. THIS DELAY IS INITIALLY SET MILLISECONDS AND CAN BE CHANGED BY THE OPERATOR. IF THE BECOMES TOO SMALL, THE LP2 MOTOR MOVEMENT MAY NOT BE ABLE TO SETTLE BEFORE THE NEXT TEST. THEREFORE, THE TIME DELAY ARGUMENT (FOUND AT LOCATION 2) MUST NOT BE MADE SMALLER THAN 25 MILLISECONDS (FOR MOST MACHINES). THERE IS NO LIMIT ON THE AMOUNT THE DELAY CAN BE INCREASED. THE USER SHOULD NOTE THAT USING A SMALLER DELAY WILL RESULT IN CAUTO BEING EXECUTED AT A FASTER RATE, WHILE A LARGER DELAY WILL INCREASE EXECUTION TIME.

2) DURING THE LINEFEED TESTS THE DLP2 STEPS THE VERTICAL MOTOR BY ISSUING THE VERTICAL STEPS CONTAINED IN THE OUTS INSTRUCTIONS IN THE LFSBEG TABLE. THESE STEPS MAY BE CHANGED. THE PROGRAM WILL ISSUE THE EIGHT STEPS FOR EVERY LINEFEED EVEN IF THEY ARE IN INCORRECT ORDER. FOR EXAMPLE, TO RUN THE LINEFEED MOTOR AT HALF SPEED, THE STEPS CAN BE DOUBLED. SO THAT THE MOTOR ONLY MOVES EVERY OTHER STEP.

LFSBEG: 64820
64820
64800
64800
64840
64840
64800
64800

IT IS NOT NECESSARY THAT EIGHT STEPS BE ISSUED FOR EVERY LINEFEED. FOR EXAMPLE, IF THE USER WANTED TO CAREFULLY EXAMINE THE VERTICAL MOTOR HARDWARE, IT WOULD BE DESIRABLE TO GO ONE STEP AT A TIME. TO ACCOMPLISH THIS, THE ARGUMENT IN LOCATION 1106 CAN BE CHANGED TO 21000. THIS WILL RESULT IN THE PROGRAM EXECUTING ONLY 1 STEP AND THE TERMINATING. THE STEP EXECUTED IS THE FIRST ONE IN THE

0022 .MAIN

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LINE FEED SEQUENCE TABLE (LOCATION 2211). THE FOLLOWING IS AN EXAMPLE OF GOING THROUGH THE STEPS ON AT A TIME.

0 1106/21055 21000 (CR)
0 503R
0 1V (CR)
0 2211/64020 64000 (CR)
0 503R (CR)
0 1V (CR)
0 2211/64000 64040 (CR)
0 503R (CR)
0 1V (CR)
0 2211/64040 64000 (CR)
0 503R
0 1V (CR)

AT THIS TIME, EVERY STEP HAS BEEN EXECUTED ONE TIME.

NOTE: UPON ENTERING THE ODT, THE HORIZONTAL MOTOR IS STOPPED AND THE VERTICAL MOTOR IS RESET TO STEP 00.

10023 .MAIN

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0024 .MAIN

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2.1 IN'S AND OUT'S

IN ORDER TO SIMPLIFY THE HARDWARE LP2 DO
SUPPORT THE I/O FUNCTIONS. ALL THE INPUT
OUTPUTS ARE DONE USING LOAD AND STORE IN
WITH ADDRESSES OVER 37770.

2.1.1

IN FUNCTIONS

THERE ARE EIGHT IN FUNCTIONS (IN0 THRU I
ABLE TO INPUT INFORMATION FROM THE LP2 H
THEIR ADDRESSES ARE 37770 THRU 37777. TH
OF AN ACCUMULATOR FROM LOCATION 37770 HI
FERED TO AS IN0 AND THE ACCUMULATOR WILL
WITH 16 BITS OF INFORMATION FROM THE LP2

2.1.2

OUT FUNCTIONS

THERE ARE EIGHT OUT FUNCTIONS (OUT0 THRU
ABLE TO OUTPUT INFORMATION TO THE LP2 MA
THESE FUNCTIONS ARE ADDRESSED BY ADDRESS
THAN 40000 - ADDRESS BITS 2,3, AND 4 ARE
SELECT ONE OF THE EIGHT OUT FUNCTIONS AN
MATION ON BITS 5 THRU 15 IS TRANSFERED T
THUS STORING OF ANY ACCUMULATOR AT THE A
40177 WILL PERFORM AN OUT 0 AND SEND 177

2.1.3

LIST OF IN FUNCTIONS

IN0 USED TO READ DATA FROM CHAR GEN.

BDATA 6-15

IN1 BIT 0 HOME STATUS EQUAL TO ZERO MH
HOME
BIT 10 SELF TEST INT. EQUAL TO ZERO FO
BIT 11 VERT INTERRUPT EQUAL TO ZERO FO
BIT 12 KEYBOARD INT. EQUAL TO ZERO KE
BIT 13 TICK INTERRUPT EQUAL TO ZERO CL
BIT 14 PRINT INTERRUPT EQUAL TO ZERO PR
BIT 15 START CHAR INT. EQUAL TO ONE FOR

IN2

BIT 7 ERROR EQUAL TO ONE FOR
BITS 8-15 DATA FROM UART

IN3

BIT 8 PAPER FAULT EQUAL TO ZERO FO
BITS 8-15 FORM FEED EQUAL TO
COUNT OF LINES

IN4

BIT 0 VIEW ENABLE EQUAL TO ONE VIE
BIT 1 ON LINE EQUAL TO ONE FOR
BIT 2 DATA AVAILABLE EQUAL TO ONE FOR
BIT 3 TBE EQUAL TO ZERO BU
BIT 4 CARRIER DETECT ZERO FOR CARRIER
BIT 5 CLEAR TO SEND EQUAL TO ONE FOR

BIT 6 1/2 DUPLEX EQUAL TO ONE FOR
BIT 7 NOT USED
BIT 8 LINE FEED EQUAL TO ZERO FO
BIT 9 FORM FEED. EQUAL TO ZERO FO
BIT 10 DATA SET READY EQUAL TO ZERO FO
BIT 11 NOT USED
BIT 12 NOT USED
BIT 13 NOT USED
BIT 14 BUSY
BIT 15 EQUAL 11 CLEAR T
10 DEVICE
01 BREAK

INS RESET KEYBOARD INT.
9-15 KEYBOARD DATA

IN6 START TIME TASK

IN7 BIT0 FORM FEED INIT ONE TO INIT. THE
BIT1 PLOTTING MODE ONE IF THE JUMPE
JUMPER
BIT2 COMPRESSED ONE IF THE JUMPE
BIT3 ELONGATED MODE ONE IF THE JUMPE
JUMPER
BIT4 APL JUMPER ONE IF THE JUMPE
BITS NOT USED
BIT6 NOT USED
BIT7 NOT USED
BIT8 6/8 LINES PER 6-ZERO
INCH 8*ONE
BIT9 NOT USED
BIT10 NOT USED
BIT11 COMPRESSED ONE TO SELECT CO
SELECT PRINTING MODE
BIT13 NOT USED ONE TO SELECT AP
BIT14 NOT USED
BIT15 AUTO SKIP ONE TO ENABLE AU

18825 .MAIN

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2.1.4 LIST OF OUT FUNCTIONS

OUT0 RESET POWER UP INIT
OUT1 TRANSFER DATA TO HOST

DATA 9-15

OUT2 BIT11 DATA TERMINAL ONE WHEN THE DEV
READY
BIT12 ON LINE ONE WHEN THE DEV
BIT13 READY LIGHT ON ONE TO TURN ON T
KEYBOARD
BIT14 REQUEST TO SEND EQUAL TO ONE WHE
BIT15 BREAK ONE TO SEND THE

OUT3 BIT12 SELECT APL ONE TO SELECT AP
BIT13 PRINT MASK ZERO TO MASK OUT
BIT14 PRINT SELECT 0 REG
BIT15 BELL 1 COMPRESSED

OUT4 FIRE THE PRINT WIRES
BITS 7-15

OUT5 MOTION CONTROL
BIT 10
8 PAPER FEED COMMANDS
BIT 11
HORIZONTAL MOTION COMMANDS
BIT 12 INC/SLOW SPEED
BIT 13 DIRECTION OF
BIT 14 STOP BIT 0 TO MOVE TO THE
BIT 15 110/180 SPEED 1 TO MOVE TO THE
0 TO STOP THE HD

OUT6 INTERRUPT RESET ONE TO RESET SEL
BIT10 SELF TEST ONE TO RESET VER
BIT11 VER INT
BIT12 NOT USED
BIT13 TICK
BIT14 PRINT
BIT15 START CHAR INTERRUPT

OUT7 ADDRESS FOR CHAR GEN CHAR
BITS 6-12
BITS 13-15 COUNT FOR POS

18826 .MAIN

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2.5 OCTAL DEBUG TOOL (ODT)

THIS FIRMWARE IS EQUIPPED WITH AN OCTAL D
RE ACCESSED BY HITTING ANY KEY ON THE TE
A TEMPORARY FEATURE WHICH WILL BE TAKEN
FIRMWARE IS RELEASED). WHEN THE PROGRAM
ING A KEY, A STOP TO THE HORIZONTAL PHOTO

ODT OFFERS THE FOLLOWING FEATURES:

ON ENTERING ODT THE ADDRESS OF THE LOCAL
NEXT INSTRUCTION TO BE EXECUTED WILL BE

CONVENTIONS AND SYMBOLS

THE FOLLOWING CONVENTIONS ARE USED BY TH
? PRESSING ANY ILLEGAL KEY CAUSES
0 ODT IS READY AND AT YOUR SERVICE

COMMAND STRUCTURE

AN OCT COMMAND HAS THE FOLLOWING FORMAT:
(ARGUMENT) (COMMAND)
AN ARGUMENT MAY BE ONE OF THE FOLLOWING:
EXP AN OCTAL EXPRESSION CONSISTING O
SEPARATED BY PLUS (+) OR MINUS (-)
ADR AN ADDRESS IS THE SAME AS AN EXP
ING ZEROS NEED NOT BE TYPED.
THAT BIT 0 IS NEGLECTED.
A COMMAND IS A SINGLE TELETYPE CHARACTER

ODT COMMANDS

THE LOCATIONS THAT CAN BE EXAMINED AND M
USER ARE CALLED CELLS. THESE CELLS ARE O
INTERNAL CPU CELLS AND MEMORY LOCATIONS.

2.5.3.1

OPENING INTERNAL CELLS
THE COMMAND TO OPEN ONE OF THE INTERNAL
THE FORM "NA" WHERE N IS ANY OCTAL EXPRE

0016 CDEBA

WHERE N IS THE NUMBER OF REGISTER TO BE SEEN
0-3 TO LOOK AT ACCUMULATORS 0-3
4 PC+1 BEFORE PROGRAM ENTERED ODT, BIT 0 I
5 STACK POINTER
6 FRAME POINTER
7 CPU AND I/O STATUS
BIT INTERPERTATION
15 1 IF I/O DONE WAS SET, 0 OTHERWISE
14 1 IF INTERRUPTS WERE ENABLED, 0
13 STATUS OF THE CARRY BIT
12 ADDRESS OF A LOCATION IN PAGE 0 (0-377)
11 BREAK POINT.
10 ADDRESS OF THE LOCATION WHERE BREAK POIN
INSTRUCTION THAT WAS STORED AT BREAK POI

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OTHER COMMANDS TO OPEN CELLS ARE:

ADR/ OPEN THE CELL AND PRINT ITS CONT
./ AND PRINT ITS CURRENTLY POINTED
AND PRINT ITS CONTENTS.
+ADR/ ADD ADR TO THE POINTER, OPEN THE
ITS CONTENTS.
-ADR/ SUBTRACT ADR FROM THE POINTER, O
PRINT ITS CONTENTS.
"CR" THE RETURN KEY IS USED TO CLOSE
WITH OR WITHOUT MODIFICATION.
"LF" LINE FEED IS USED TO CLOSE THE O
WITHOUT MODIFICATION AND TO OPEN
CELL.
/ CLOSE THE OPEN CELL WITHOUT MODI
OPEN THE CELL POINTED BY ITS CON
CLOSE THE OPEN CELL WITHOUT MODI
OPEN THE CELL POINTED BY ITS CON
CLOSE THE OPEN CELL WITHOUT MODI
OPEN THE CELL POINTED BY ITS CON

2.5.3.2 MODIFICATION OF A CELL

ONCE A CELL HAS BEEN OPENED ITS CONTENTS
BY TYPING THE NEW VALUE THE CELL IS TO C
FORM OF AN OCIAL EXPRESSION FOLLOWED BY
IF A + OR IS TYPED AS THE FIRST CHARAC
PRESSION THEN THE VALUE OF THE EXPRESSIO
SUBTRACTED FROM THE OLD CONTENTS OF THE
ADDRESS ITSELF OR AN EXPRESSION RELATIVE
CAN BE DEPOSITED BY TYPING A " " OR "+/
ION". A RUBOUT COMMAND GIVEN RIGHT AFTER
DELETES THE RIGHT MOST DIGIT OF THE OPEN
ALLOWS THE MODIFICATION OF ITS CONTENTS
TYPED IN JUST BEFORE THE RUBOUT WAS ISSU

2.5.3.3 OTHER ODT COMMANDS

RUBOUT THIS KEY IS USED TO DELETE ERRON
DIGITS. EACH TIME THIS KEY IS PR
MOST DIGIT IS DELETED AND ECHOED
IF THE RUBOUT KEY IS HIT IMMEDIA
ING A CELL THE RIGHT MOST DIGIT
DELETED THIS CELL CAN NOW BE MO
CONTENTS WERE TYPED-IN BY THE US
THE RUBOUT KEY WAS PRESSED.
ADRB INSERT A BREAK POINT AT LOCATION
ONLY ONE BREAK POINT CAN BE INSE
ENTRY TO ODT AFTER EXECUTING A B
CAUSE IT TO BE DELETED.
D DELETE THE BREAK POINT IF ANY.
P RESTART THE EXECUTION OF THE PRO
POINTED BY AA
ADRR START EXECUTING THE PROGRAM AT "
IO=RESET.
K KILL THE STRING TYPED SO FAR, TH
WITH A "?" AND THE OPEN CELL IS
MODIFICATION.

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10020 .MAIN

12) SPECIAL NOTES/SPECIAL FEATURES

1) RESETTNG THE LP2

THE LP2 CAN BE RESET BY STARTING
EXECUTION AT 40000 IN THE LP2 MICRONOVA
CPU. THIS CAN BE ACCOMPLISHED
BY HITTING 40000 START ON THE
HAND HELD CONSOLE, OR 40000R IN
ODT.

13) RUN TIME

RON TEST 1 SECOND
TEST 1 2 SECONDS (10 SECONDS MOST WAIT)
TEST 2 1 SECOND (5 SECOND MOST WAIT)
TEST 3 45 SECONDS FOR USREG=20000
1.5 MINUTES FOR USRES=0
3.0 MINUTES FOR USRES=30000
6.0 MINUTES FOR USREG=10000
TEST 4 SUM OF TESTS 1,2 AND 3
FOR 1 PASS.
CAUTO 7.0 MINUTES (ONE PASS, ALL PASSES
TAKE THE SAME TIME)
COPER2 NA
.ENDC

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS