MODEL 422
FLOPPY DISK SYSTEM
OPERATION
AND
MAINTENANCE MANUAL
PART II

dicom INDUSTRIES

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FOREWORD

This manual provides operating and service instructions for the FD400/500 Flexible Disk Drives, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

The content includes a detailed description, specifications, installation instructions and checkout of the disk drive. Also included are theory of operation and prventive maintenance instructions.

All graphic symbols used in logic diagrams conform to the requirements of ANSI Y32.14 and all symbols used in schematic diagrams are as specified in MIL-STD-15.

SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact the following conveniently located regional service centers — our trained service staff will be pleased to assist you.

WESTERN REGION

PERTEC Service Center
17835 Ventura Blvd,
Encino, California 91316
Phone (213) 996-1333
TWX (910) 493-2075

EASTERN REGION

PERTEC Service Center
235 Bear Hill Road
Waltham, Massachusetts 02154
Phone (617) 890-6230
TWX (710) 324-1154

CENTRAL REGION

PERTEC Service Center
6300 North River Road
O'Hare International Transportation Center
Rosemont, Illinois 60018
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TWX (910) 253-5918

EUROPEAN REGION

PERTEC Service Center
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10 Portman Road
Reading, Berkshire RG3 1DU, England
Phone Reading (734) 582-115
TWX (851) 847-101

AUTHORIZED REPAIR CENTER

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9600 Irondale Avenue
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Phone (213) 882-0030
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PROPRIETARY NOTICE

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the FD400/FD500 Flexible Disk Drives, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

1.2 MODEL IDENTIFICATION

The following paragraphs provide descriptions of the unique functional features offered within the PERTEC family of flexible disk drives. In addition to the unique features described, the following features may be included in all models.

- Write Protect Sensor. This option is used to disable the disk drive write electronics, thus prevents overwriting the protected diskettes.
- Trim erase timing circuits internal to the disk drive.
- Negative Voltage Option. When properly configured, this option allows use of operation on —5 or —12/—15v dc.
- Power Save Circuitry. Provides reduction of the + 24v current during periods of disk drive inactivity.

(1) FD400. The FD400 is the basic model configuration of the PERTEC family of flexible disk drives. The unit utilizes a dc drive motor which operates from user supplied + 24v dc. The FD400 front door is spring-loaded and is activated by a bar-switch located on the front of the machine.

(2) FD5X0. The FD5X0 Series of flexible disk drives are dependent on ac voltage and current for drive motor operation. The front door of the FD5X0 has an interlock feature which disables the door mechanism via an interface line. In addition, an indicator located in the bar-switch will become illuminated whenever the interface line is true. The drive can also be used to provide double density recording.

(3) FD5X1. The FD5X1 Series of flexible disk drives provide capabilities similar to those provided by the FD5X0 Series. In addition to those features, the following capabilities are offered.

- Internal Daisy Chain
- Basic Data Separator Circuit (Double Frequency Operation)
- Index-Sector Separation Circuit
- Sector Divider
- Ready Information
- Busy Seeking Status
- Power Save Feature Selectable with Head Load or Select Logic
- Step Logic Offering Step-In/Step-Out Control or Direction-Step Control

1.2.1 OPTIONAL INTERFACE (MODELS FD400 AND FD5X0 ONLY)

Provision for certain optional interfacing has been included in the design of the PERTEC family of flexible disk drives. These interfaces are implemented on a 3.5- by 8.5-inch PCBA which is electrically connected to the drive via a 44-pin edge connector mounted to the PCBA and mechanically secured to the disk drive via captive hardware. It should be noted that use of this PCBA extends the required mounting depth for the drive by 1.5 inches.

A description of the interface supplied with the disk drive is presented in Section III of this manual.

1.2.2 DISKETTES

The standard IBM diskette is designed for use with a format in which sector mark information is pre-recorded on the diskette. In this case, a single index hole is provided for reference purposes. Detection of this hole is accomplished by an Index Transducer/LED combination.

Other diskettes are available which are designed with multiple holes which themselves provide sector mark information via the same transducer that is used in the single hole configuration.

1.3 PURPOSE OF EQUIPMENT

The PERTEC flexible disk drive is a compact disk memory device designed for random access data storage, data entry, and data output applications. These applications typically are intelligent terminal controllers, mini-computers, word processing systems, data communications systems, error logging and micro-program logging, and point of sale terminals.

The flexible disk family has the capability of recording and reading digital data using a double frequency technique. Data recorded on a diskette by the flexible disk drive can be recovered when the diskette is played back by an IBM 3540 or 3740 system. Conversely, data recorded on a diskette by an IBM 3540 or 3740 system can be recovered when the diskette is played back by the PERTEC flexible disk drive.

The FD400 operates directly from customer-supplied +24v dc, +5v dc, and —5v dc; an optional feature is available which allows the use of a negative power supply up to —15v dc in lieu of —5v. No ac power is required for the FD400 Series.

The FD5XX Series require both dc and ac power. The ac power is required to operate the drive motor. The ac voltage and frequency must be specified at the time of ordering. The FD5XX electronics operate directly from customer-supplied +24v dc, +5v dc, and —5v dc.

1.4 PHYSICAL DESCRIPTION OF EQUIPMENT

The FD400 and FD5XX flexible disk drives are shown in Figure 1-1. The drives can be mounted in any vertical or horizontal plane; however, when mounted horizontally, the non-recording surface of the diskette must be uppermost.

Figure 1-2 is a simplified drawing of the diskette used with the flexible disk drive. It can be seen that this recording medium is a flexible magnetic disk enclosed in a protective jacket. The protected disk, free to rotate within the jacket, is continuously cleaned by the soft fabric inner lining of the jacket during normal operation.

The basic chassis centers around a precision stamped steel plate which provides a single reference surface to which all critical mechanical components are attached. This reference surface is held to a high degree of flatness. The steel material provides an optimum overall temperature compensation which ensures a high degree of track location accuracy over the specified temperature range.

The mechanical components of the drive, depending on the model, include a direct drive brushless dc motor, or belt-driven ac motor, and a stepper motor/lead screw combination for positioning the magnetic read/write/erase head assembly.

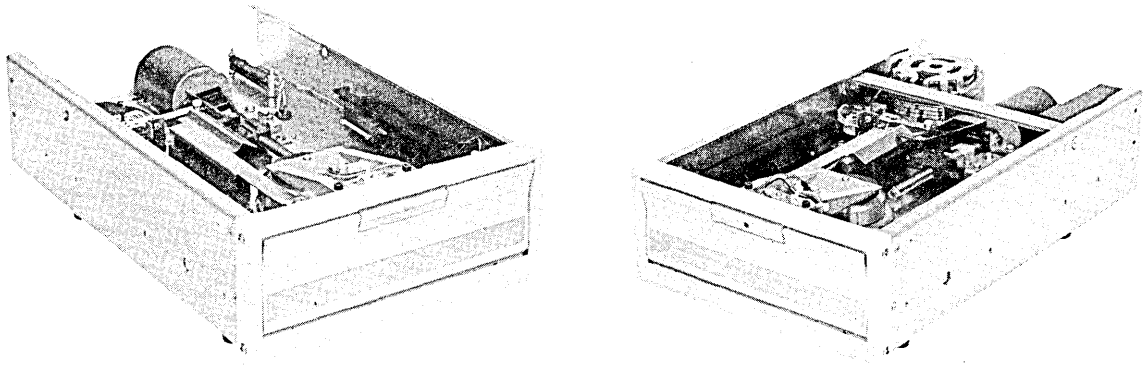


Figure 1-1. FD400 and FD5XX Flexible Disk Drives

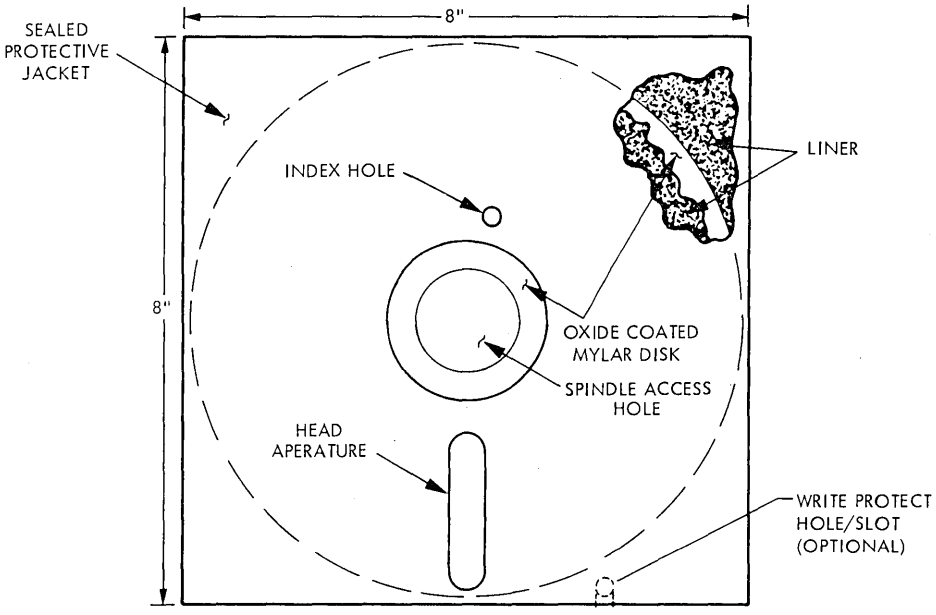


Figure 1-2. Recording Medium

The read/write/erase head assembly is a glass-bonded ferrite/ceramic structure which has a life in excess of 20,000 hours.

Operator access for diskette loading is provided via a door located at the front of the unit.

The electronic components of the drive are mounted on a single PCBA which is located beneath the chassis. Power and interface signals are routed through connectors which plug directly into the PCBA.

The PERTEC flexible disk family provides the mechanical and magnetic characteristics necessary to achieve diskette interchangeability with an IBM 3540 or 3740 system. Diskettes thus employed are pre-initialized.

NOTE

Further information regarding format and control of PERTEC flexible disk drives is contained in a series of Application Notes, PERTEC document numbers 75605, 75607, and 76601.

1.5 FUNCTIONAL DESCRIPTION

The flexible disk drive is fully automatic and requires no operator intervention during normal operation. The drive consists of a spindle drive system, head load and positioning system, and read/write and erase system.

When the front door is opened, access is provided for the insertion of a diskette. The diskette is positioned in a lateral and up/down direction by cartridge guides. In/out location is provided by ensuring that the diskette is inserted until a back stop is encountered.

With the disk located as described, closure of the front door activates the cone/clamp system resulting in (first) centering of the recording medium and (second) clamping of the medium to the drive hub. The drive hub is driven at a constant speed of 360 rpm in dc models by a brushless dc motor; in ac models the hub is driven at a constant 360 rpm by an ac motor.

In operation, the magnetic head is loaded into contact with the recording medium by the head load system. For reliable operation it is important that the head/medium relationship is controlled. This is accomplished by:

(1) Referencing the diskette to a platten surface.

(2) Referencing the head crown to the same platten surface as the diskette, thus minimizing errors due to the absolute relationship of platten and stepper motor shaft.

(3) Providing a pressure pad which is loaded on the opposite side of the recording medium from the head with a force of 12 to 15 grams.

In the standby mode, the head load solenoid is de-energized and both the head and pressure pad are retracted, thereby minimizing head and media wear.

The magnetic head is positioned over the desired track by means of a 3-phase stepper motor/lead screw assembly and its associated electronics. This positioner employs a 3-step movement to cause a one-track linear movement. Thus, a superior track location accuracy is provided by combining the increased basic movement accuracy with a reduced hysteresis error caused by system friction.

In drives equipped with the Write Protect option, the write electronics are disabled if a hole is provided in the diskette jacket as shown in Figure 1-2. When a write protected diskette is inserted into the drive, light from a LED passes through the hole and activates a photo-transistor circuit which, in turn, disables the write electronics of the drive.

A double frequency recording system is typically employed in the PERTEC family of flexible disk drives.

When performing a write operation, a 0.013-inch (nominal) data track is recorded. This 0.013-inch (nominal) track is tunnel erased to 0.012-inch (nominal).

The recording area is divided into two zones: Tracks 0 through 42 (outer), and Tracks 43 through 76 (inner). These two zones correspond to those in the standard IBM format. It should be noted that the write current is higher in the outer zone tracks than in those tracks located in the inner zone. The two-level write current source and erase current source are provided by the write electronics portion of the disk drive.

Data recovery electronics include a low-level read amplifier, differentiator, zero-crossing detector, and digitizing circuits. No data decoding facilities are provided in the basic drive but are provided as an option on the FD5X1 Series.

Although the drive is primarily intended for operation in a double frequency recording mode, the basic electronics design does not preclude the use of other recording code systems. Changes in values to the electronics may be necessary when other coding systems are employed.

The drive is also supplied with the following sensor systems.

(1) A door switch which detects the position of the door, i.e., open or closed.

(2) A Track 0 switch which senses when the Head/Carriage assembly is positioned at track zero.

(3) An index sensor/LED light source is positioned so that when the index hole (located at an inner radius of the recording medium) is detected, a digital signal is generated.

(4) In the case when a 'hard sectored' (multi-hole) diskette is used, the index sensor used is a high resolution device which can distinguish holes placed close together, i.e., index-sector holes.

1.6 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications for the flexible disk drive family are given in Table 1-1.

1.7 INTERFACE SPECIFICATIONS

Levels: True = +0.2v (±0.2v) (approximately)

False = +3.0v (approximately)

Pulses: Levels as above.

The interface circuits are designed so that a disconnected wire results in a false signal.

Figure 1-3 illustrates the configuration for which transmitters and receivers have been designed for FD400 and FD5X0 models. Transmitters and receivers for Models FD5X1 are shown in Figure 3-6.

Table 1-1
Mechanical and Electrical Specifications

Removable Recording Media	IBM Diskette (or equivalent)	
Maximum Storage Capacity (Unformatted)	3.2 megabits	
Tracks per inch	48	
Tracks per diskette	77	
Maximum bits per track (Unformatted)	41,665	
Recording Mode	Double Frequency	
Recording Density	6631 bits per radian	
Transfer Rate	250,000 bits per second	
Disk Speed	360 rpm	
Long Term Speed Variation	±1.5%	
Instantaneous Speed Variation (ISV)	±1.5%	
Latency Time (average)	83.3 milliseconds	
	FD400	FD5XX
Start Time	5 seconds (maximum)	2 seconds (maximum)
Stop Time (with diskette)	5 seconds (maximum)	2 seconds (maximum)
Adjacent Track Seek Time	10 milliseconds (minimum)	
Head Settling Time	20 milliseconds (at last track addressed)	
Head Load Time	40 milliseconds (maximum)	
Head Positioner	Stepper Motor with Lead Screw Driven Carriage	
Head Life	20,000 hours	
Dimensions	FD400/FD5X0	FD5X1
Height	3.45 inches (8.99 cm)	3.45 inches (8.99 cm)
Width	8.60 inches (21.84 cm)	8.60 inches (21.84 cm)
Length	14.2 inches (36.07 cm)	14.91 inches (37.87 cm)
Weight	Less than 14 pounds (6.35 kg)	Less than 14 pounds (6.35 kg)
Operating Temperature	+10° to +42°C (+50° to 110°F)	
Non-Operating Temperature	—40° to +71°C (—40° to +160°F)	
Operating Humidity	20 to 80% (without condensation)	
Non-Operating Humidity	5 to 95% (without condensation)	
Operating Altitude	500 ft (152.4 m) below sea level to 10,000 ft (3,048 m) above sea level	
Non-Operating Altitude	1,000 ft (304.8 m) below sea level to 50,000 ft (15,240 m) above sea level	
Cooling	53 Watts (177 Btu/Hr) nominal; 70 Watts (235 Btu/Hr) maximum	
Vibration and Shock (Operating)	6 to 600 Hz, 0.5g; 11 milliseconds duration, 1.5g	
	FD400	FD5XX
Power*	+24v dc, +5v dc, —5v dc	115v ac 60 Hz/230v ac 50 Hz/ 115v ac 50 Hz +24v dc, +5v dc, —5v dc
Electronics	All Silicon	

*Refer to Section III for details.

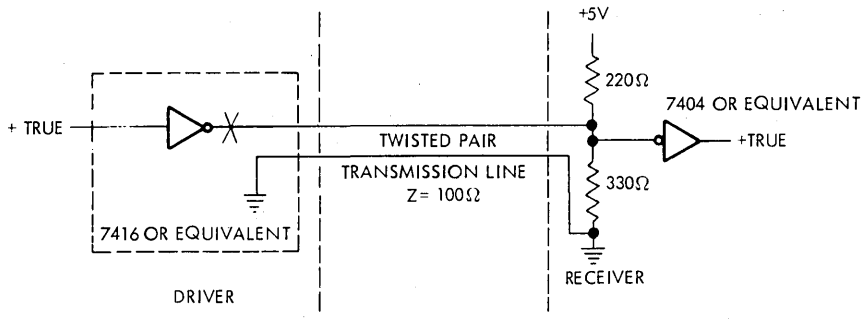


Figure 1-3. Interface Configuration, FD400 and FD5X0

1.8 UNCRATING THE DISK DRIVE

The disk drive is shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment. The following procedure describes the recommended method for uncrating the disk drive.

(1) Place the shipping container on a flat work surface. Ensure that the carton is positioned as indicated on the carton.

(2) Remove or cut the tape from one end of the carton; open the carton flaps.

(3) Remove the schematic package from the carton.

(4) Remove the Operating and Service Manual from the carton (if supplied).

(5) Slide the disk drive and packing material out of the shipping carton.

(6) Remove the packing material from around the disk drive.

(7) Check the contents of the shipping container against the packing slip; investigate the contents for possible damage — notify the carrier immediately if any damage is noted.

1.9 PHYSICAL CHECKOUT

Before applying power to the unit and prior to integrating it into a system, the following inspection should be performed.

(1) Diskette Loading Door

- FD400 Models:

  Check that the front access door opens and closes. Note that when the door is opened the head-load arm raises.

- FD500 Models:

  Check that the front access door opens and closes. To accomplish this operation with power removed, the door locking solenoid must be manually actuated.

CAUTION

THE HEAD-LOAD SPRING AND THE DISKETTE-LOAD SPRING ARE DELICATE, PRECISION SPRINGS AND MUST NOT BE STRESSED OR OTHERWISE DISTURBED.

(2) Inspect the bezel for security.

(3) Manually rotate the drive hub. This hub should rotate freely.

(4) Manually rotate the stepper motor shaft. The shaft should rotate without hindrance and should cause the head carriage to advance and retract as the shaft is rotated alternately clockwise and counterclockwise.

(5) Check that the Printed Circuit Board Assembly (PCBA) is secure. Access to the PCBA is from the bottom of the drive. Check that the connectors are firmly seated.

CAUTION

OPERATION OF THE DISK DRIVE WITH THE UNIT SITTING HORIZONTALLY ON A FLAT SURFACE WITH NO PROVISION FOR AIR FLOW BENEATH THE UNIT MAY CAUSE OVERHEATING. DO NOT OPERATE THE DRIVE IN THIS CONFIGURATION FOR AN EXTENDED PERIOD.

1.10 INTERFACE CONNECTIONS

1.10.1 FD400 AND FD5X0

Both signal and dc power connection is made to the FD400 and FD5X0 via a user-supplied 44-pin edge connector. This connector mates directly with the FD400 and FD5X0 PCBA at the rear of the drive as shown in Figure 1-4 (A and B) and must be keyed between pins 5 and 6. Two tapped (4-40 UNC) holes are provided to accommodate strain-relief screws.

CAUTION

THE USER-SUPPLIED 44-PIN EDGE CONNECTOR MUST BE PROPERLY KEYED. REVERSAL OF CONNECTOR WILL CAUSE SERIOUS DAMAGE TO THE DRIVE.

In addition to the 44-pin edge connector, FD5X0 drives require that ac power connection be made via a three-pin socket located at the rear of the drive. Refer to Figure 1-4(B).

The signal connector harness should be made of individual twisted pairs, each with the following characteristics:

(1) Maximum length 30 feet (9.14m).

(2) Not less than one twist per inch.

(3) 22 - 24 gauge conductor.

It is important that one side of each twisted pair be grounded within a few inches of the circuit component with which it is associated.

Power connections to the FD400 and FD5X0 should be made with 18 AWG cable (minimum).

1.10.2 FD5X1

Signal connections for the FD5X1 are made via a user-supplied 50-pin flat ribbon connector (3M Part No. 3425-3000, or equivalent). This connector mates directly with the PCBA connector at the rear of the drive as shown in Figure 1-4. Power connections are divided for ac and dc requirements. The dc connector is a seven pin connector which mates with PCBA mounted connector at the rear of the drive (see Figure 1-4). The FD5X1 Series is similar to the FD5X0 Series in that ac power connection is made via a three pin socket at the rear of the drive. Refer to Figure 1-4 (C).

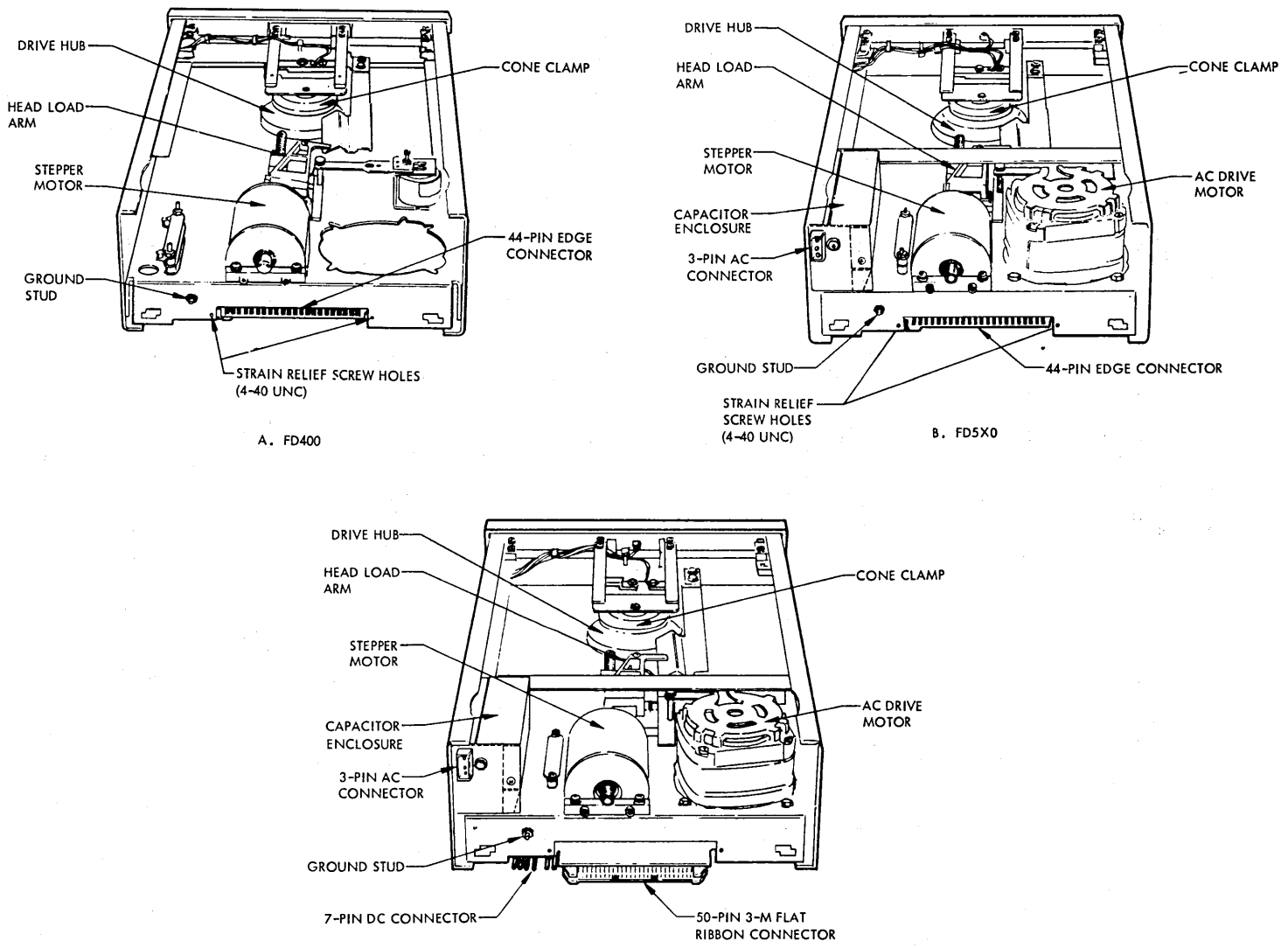


Figure 1-4. Physical Orientation

The signal connector harness should be of the flat ribbon type with the following characteristics.

(1) Maximum length of 30 feet (9.14m).

(2) 22 - 24 gauge conductor compatible with connector to be used.

Power connections should be made with 18 AWG cable (minimum). In addition, the PCBA mounted dc power connector is keyed at pin location No. 5; the corresponding connector should be keyed accordingly.

1.10.3 CHASSIS GROUND

To ensure proper operation of the drive, the chassis should be connected to earth ground. A stud, shown in Figure 1-4, is provided at the rear of the chassis to facilitate this connection.

1.11 MOUNTING THE DISK DRIVE

The drive has been designed such that it can be mounted in any plane, i.e., upright, horizontal, or vertical. The only restriction in mounting is that when mounted horizontally, the non-recording side of the diskette must be the uppermost side. Tapped holes are provided in various locations for the attachment of user-supplied hardware. Figure 1-5 shows the location of the recommended mounting holes.

The user should comply with the guidelines contained in the following paragraphs when designing an enclosure for the flexible disk drive. Outline dimensions are shown in Figure 1-5.

1.11.1 HARDWARE

The flexible disk drive is a precision device in which certain critical internal alignments must be maintained. Therefore, in keeping with rigid disk requirements, it is important that the mounting hardware does not introduce significant stress on the drive.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted.

Since the disk drive cannot be subjected to significant stress when it is slide mounted, this type of mounting generally satisfies the above requirement.

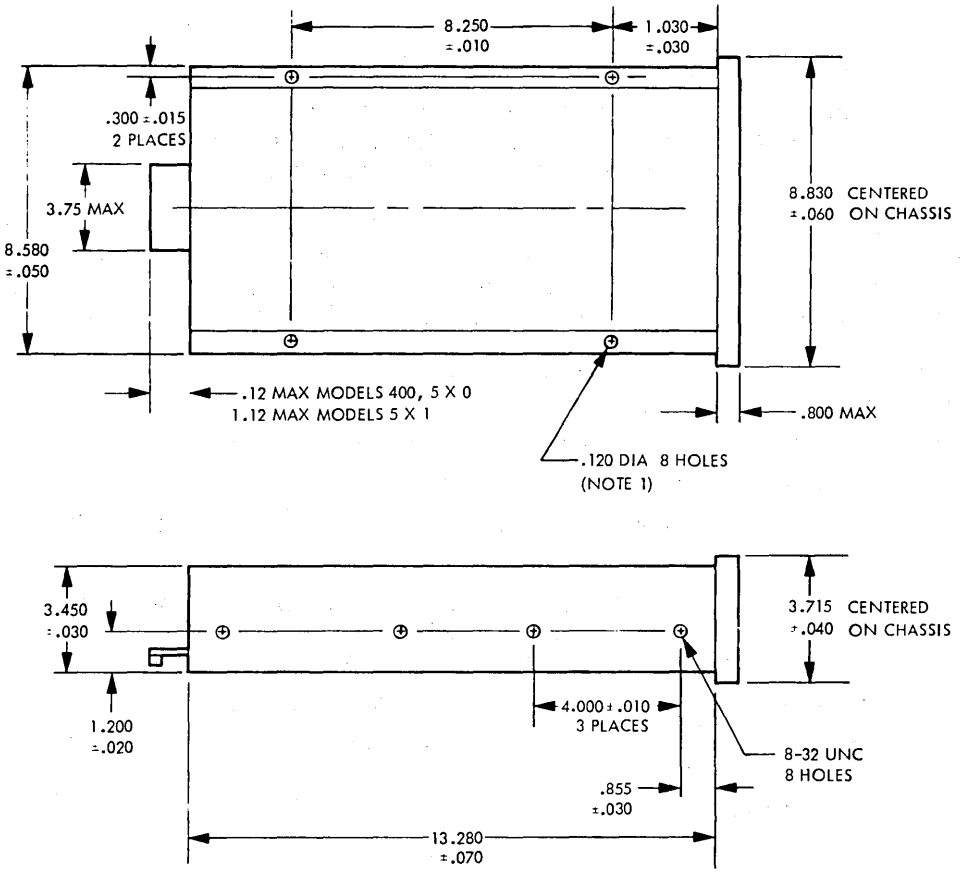
Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

Mounting schemes involving more than two hard mounting points and a third point should be avoided.

1.11.2 DUST COVER

Since the flexible disk drive is not provided with a dust cover, the design of an enclosure should incorporate a means to prevent direct ingress of loose items, e.g., dust, paper punch waste, etc.

The chassis provides additional holes if the user elects to mount his own dust cover.



NOTES: 1. THESE HOLES NOT RECOMMENDED FOR MOUNTING THE UNIT.
2. DIMENSIONS SHOWN DO NOT INCLUDE MATING CONNECTORS OR ADAPTER PCB ASSEMBLIES.

Figure 1-5. Mounting the Disk Drive

1.11.3 COOLING

Heat dissipation from a single disk drive is normally 53 watts (177 Btu/hr), and a maximum of 70 watts (235 Btu/Hr) under high line conditions. When the drive is mounted so that the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range.

When the drive is mounted in a confined environment, air flow may have to be provided to maintain specified air temperatures in the vicinity of the motors, PCBA, and diskette. An air supply of approximately 15 cfm per drive is recommended.

1.11.4 DRIVE SEPARATION

In addition to the cooling requirements specified in Paragraph 1.10.3, a minimum separation of 1 inch between drives is recommended. This is required to avoid electrical interference between the motors of one drive and the magnetic head of another drive. Closer mounting is allowable if a grounded sheet of steel of at least 0.060-inch thickness is interposed between units. However, use of this steel sheet may increase the cooling requirements.

1.12 DISKETTE HANDLING AND STORAGE

It is important that the diskette be properly handled and stored so that the integrity of the recorded data is maintained. A damaged or contaminated diskette can impair or prevent recovery of data and can result in damage to the read/write head.

Figure 1-6 illustrates the physical configuration of the diskette. The diskette is made up of an oxide coated, flexible mylar disk, 7.88 inches in diameter, and is enclosed in an 8- X 8-inch protective jacket. Read/write/erase head access is made through an aperture in the jacket. Openings for the driving hub and diskette index hole are also provided.

To assure trouble-free operation and enhance the service life of the diskette, the following handling procedures should be observed.

- Return the diskette to the protective jacket when not in use.
- Store the diskette vertically — do not stack.
- Avoid exposure of the diskette to any magnetizing force in excess of 50 oersted.

NOTE

The 50 oersted level of magnetizing force is reached at a distance of approximately 3 inches from a typical source e.g., motors, generators, transformers.

- Do not store the diskette in direct sunlight — warping could result.
- Do not use a lead pencil or ballpoint pen to write on the label — use a felt tip pen and mark lightly on the label.

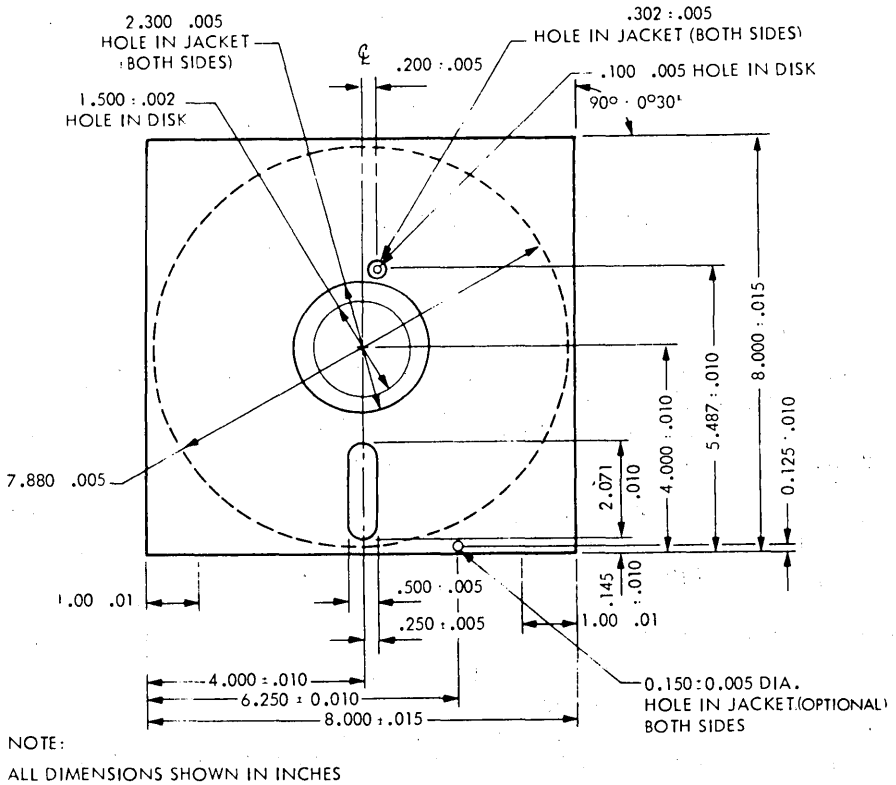


Figure 1-6. Typical Diskette

- Do not smoke when handling the diskette — ashes and other contaminants can cause serious damage to the recording surface.
- Avoid physical contact with the disk surface; do not attempt to clean or wipe the surface of the disk.

1.13 LOADING THE DISKETTE

Diskette loading is accomplished by inserting the properly oriented diskette into the *mail box* type slot provided. Access to the diskette loading slot is obtained by opening the front loading door.

NOTE

Power must be applied to the FD5XX Series drives to enable actuation of the door lock solenoid.

The diskette should be carefully inserted until the diskette jacket is solidly against the stops.

CAUTION

DAMAGE TO THE DRIVE HUB HOLE IN THE DISKETTE MAY RESULT IF THE DOOR IS CLOSED WHEN THE DISKETTE IS NOT PROPERLY INSERTED.

PERTEC flexible disk drives are equipped with a *card eject* feature which, when the diskette is inserted into the receiving slot and does not latch behind the bezel stop, a spring-loaded ejector causes the diskette to be ejected approximately 1 inch from the home position. This feature gives a clear visual indication to the operator when the diskette is not properly inserted. There is no tendency to skew the diskette since the line of action of the spring passes through the bezel stop.

Figure 1-7A illustrates the correct method of diskette loading and unloading. When loading a diskette into the drive a light force is required on the right portion of the diskette to overcome the spring-loaded ejector mechanism. When the diskette is fully inserted and encounters the stops, a slight downward pressure at the right side of the diskette will allow it to seat behind the diskette retaining stop. The loading door can now be closed; thus engaging the cone/clamp assembly.

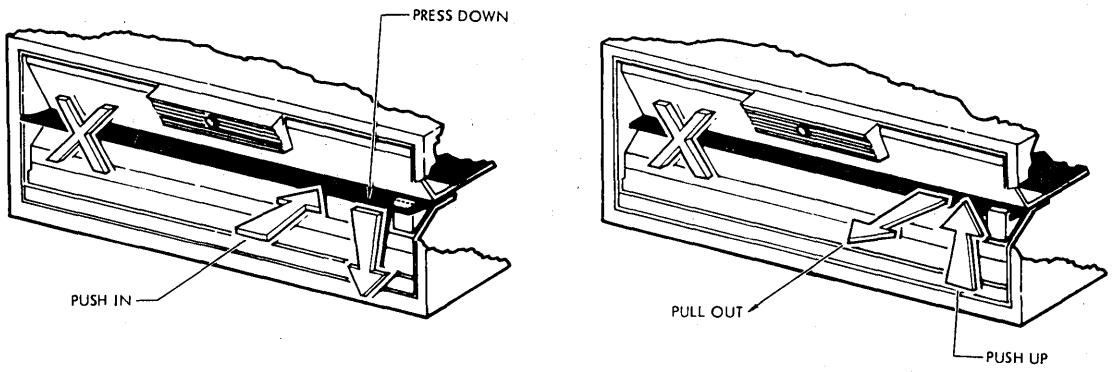


Figure 1-7. Diskette Loading and Unloading

It should be noted that, on dc models, closing the loading door when the DRIVE MOTOR ON (IDEN) interface line is true will cause the drive motor to operate. On ac models, the drive motor operates continuously.

1.14 UNLOADING THE DISKETTE

When the diskette loading door is opened, the Door Open switch is actuated; in dc models the drive motor stops regardless of the state of the DRIVE MOTOR ON interface line; in ac models, the drive motor operates continuously, regardless of the state of the loading door, i.e., open or closed.

Additionally, when the loading door is opened the cone/clamp assembly is disengaged, allowing the diskette to be withdrawn.

CAUTION

IF THE DOOR IS NOT FULLY OPENED TO THE DETENT, DAMAGE TO THE DISKETTE MAY OCCUR CAUSED BY PARTIAL ENGAGEMENT OF THE CONE.

Referring to Figure 1-7(B), it can be seen that the diskette is disengaged from the diskette retaining stop by exerting a slight upward pressure on the diskette in the vicinity of the stop. This will release the diskette which will be ejected by the spring. The diskette can then be fully withdrawn. Close the door to the drive and place the diskette in a protective jacket.

1.15 WRITE PROTECT (OPTION)

When the Write Protect feature is included, the flexible disk drive is equipped with a write protect sensor assembly. This sensor operates in conjunction with a diskette having a hole located as shown in Figure 1-6 (IBM diskettes are not manufactured with such a hole).

When the hole is not covered, the diskette is write protected. The hole must be covered to write on the diskette. Figure 1-8 illustrates how to install a tab to cover the hole. (A write protect tab may be fabricated from an adhesive-backed label such as Avery #DGF-K1-D12.)

1.16 PRIMARY POWER REQUIREMENTS

1.16.1 FD400 Series

+24 ±1v dc: 2.0 amp (maximum average)

+5 ±0.25v dc: 1.1 amp (maximum), 100 mv ripple

—5 ±0.25v dc: 0.3 amp (maximum), 100 mv ripple

In operation, the current load on the 24v line is pulsating in nature. It consists of an approximate saw-tooth which oscillates between 1.1 amp and 2.2 amp at a frequency of approximately 430 Hertz. The current profile peaks to 2.4 amps under certain conditions of positioner operation. During the drive motor start sequence, current is as follows.

t = 0 → t = 0.6 sec = 1.2 amp

t = 0.6 sec = 3.0 amp

t = 1.2 sec = 3.0 amp

t = 1.4 sec = 2.4 amp

t = 1.6 sec = 2.2 amp

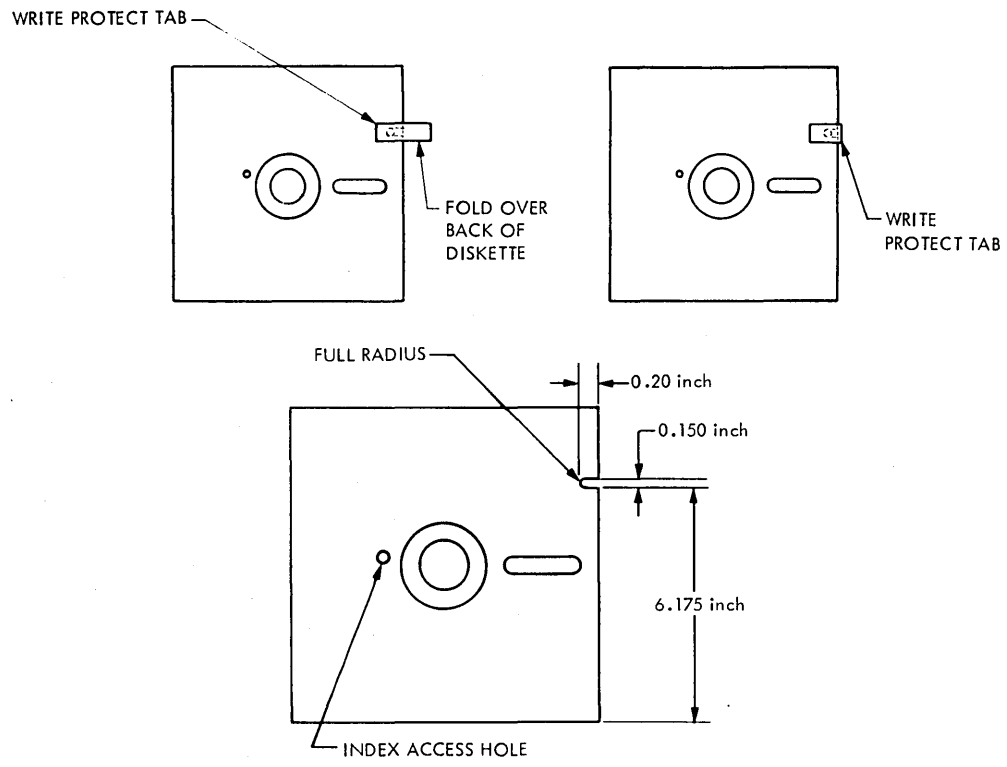


Figure 1-8. Write Protect Tab Installation

1.16.2 FD5XX Series

+24 ±1v dc: 1.4 amps

+5 ±0.25v dc: 1.4 amps (maximum), 100 mv ripple

—5 ±0.25v dc: 0.3 amps (maximum), 100 mv ripple

In operation, the current load on the 24v line is pulsating in nature and is dependent on the operational condition of the drive.

1.16.3 POWER SAVE

A power save feature is available in both FD400 and FD5XX Series disk drives. In this configuration the +24v power consumption is reduced. Also, a reduced stepper motor power dissipation in the standby mode is achieved.

1.16.4 NEGATIVE VOLTAGE

The —5v line can be changed to —12v to —15v at 0.3 amp (maximum) and 500 mv ripple (maximum). This must be specified at the time of order.

SECTION II
THEORY OF OPERATION

2.1 INTRODUCTION

This section provides a basic description of the operation of the PERTEC family of flexible disk drives.

The flexible disk drive consists of the mechanical and electrical components necessary to record and read digital data recorded on a diskette. User provided dc power at +24v, +5v, and —5v/—12v/—15v is required for operation of the disk drive.

2.2 ORGANIZATION OF THE DISK DRIVE

All electrical subassemblies in the disk drive, except the magnetic head, are constructed with leads which terminate in AMP push-in pins. These leads are merged and inserted in the single 30-pin PCB edge connector body which interfaces with the single electronics PCBA in the drive. Thus, the individual assemblies can be removed without providing individual connectors with their associated space requirements on the PCBA.

The magnetic head is connected to the PCBA via a shielded, twisted cable terminated in a 5-pin female connector and its associated male socket which is located in close proximity to the data electronics.

Interface signals and power are provided via connector or connectors at the rear of the drive dependent on drive version. Detailed description of these signals are presented in Section III of this document.

2.3 FUNCTIONAL DESCRIPTION

Figure 2-1 is a functional block diagram of the PERTEC family of disk drives and should be referred to in conjunction with the following discussion.

NOTE

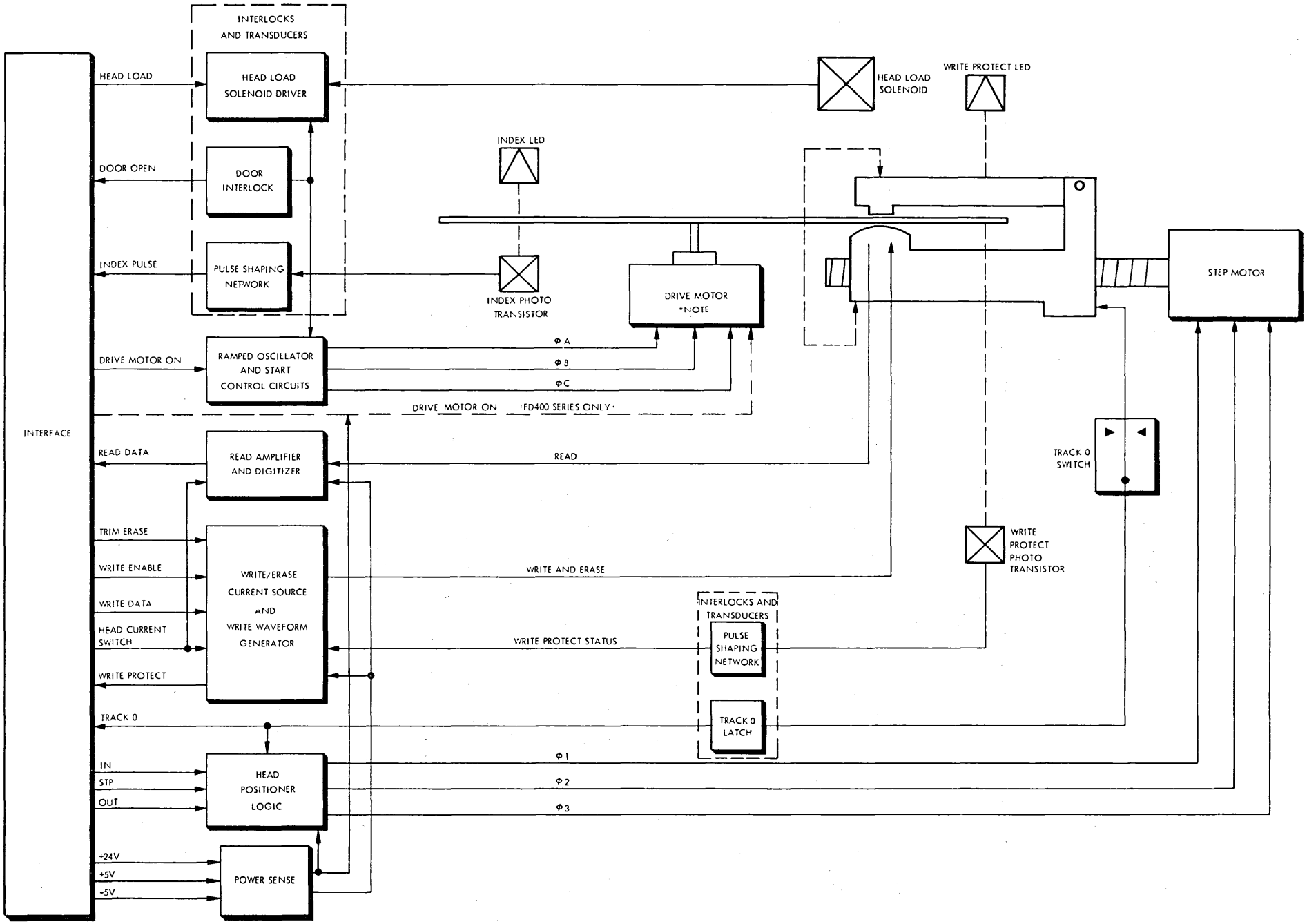
The identification of the elements in this discussion and associated figures although related to the actual schematic are not exact. Total correspondence is not possible since the schematic contains functions which are only represented in simplified form in this section.

The flexible disk drive consists of the following functional groups.

(1) Head Positioner Logic
(2) Power Sense Circuitry
(3) Interlocks and Transducers
(4) Data Electronics
    - Write/Erase Logic
    - Read Logic
(5) Spindle Drive
(6) Interface Control

2.4 HEAD POSITIONER LOGIC

A simplified diagram of the head positioner system is shown in Figure 2-2. The associated timing diagram is presented in Figure 2-3.



NOTE: *FD400 EMPLOYS DC MOTOR. FD500 EMPLOYS AC MOTOR.

Figure 2-1. Block Diagram

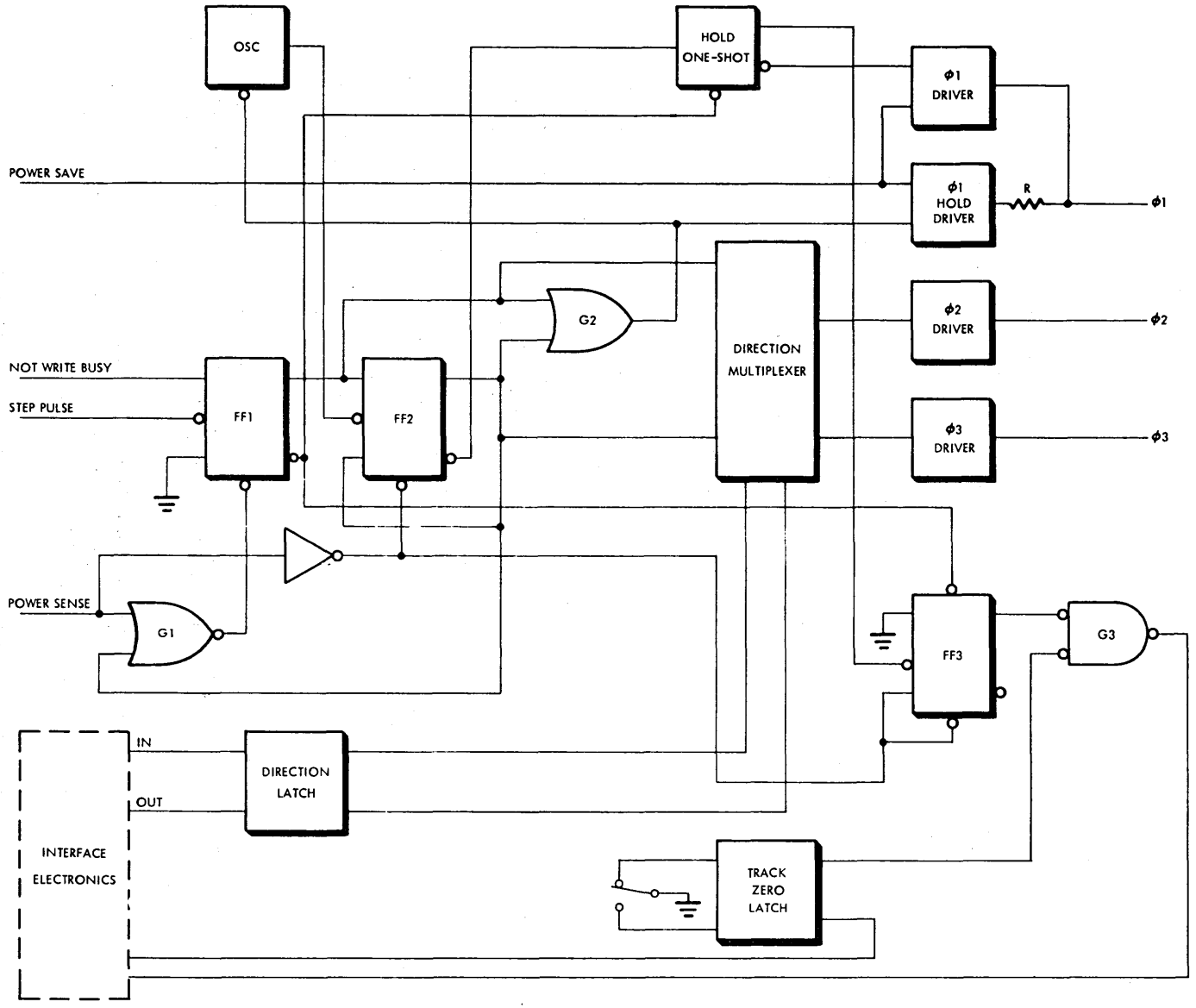


Figure 2-2. Head Positioner Control System, Simplified Block Diagram

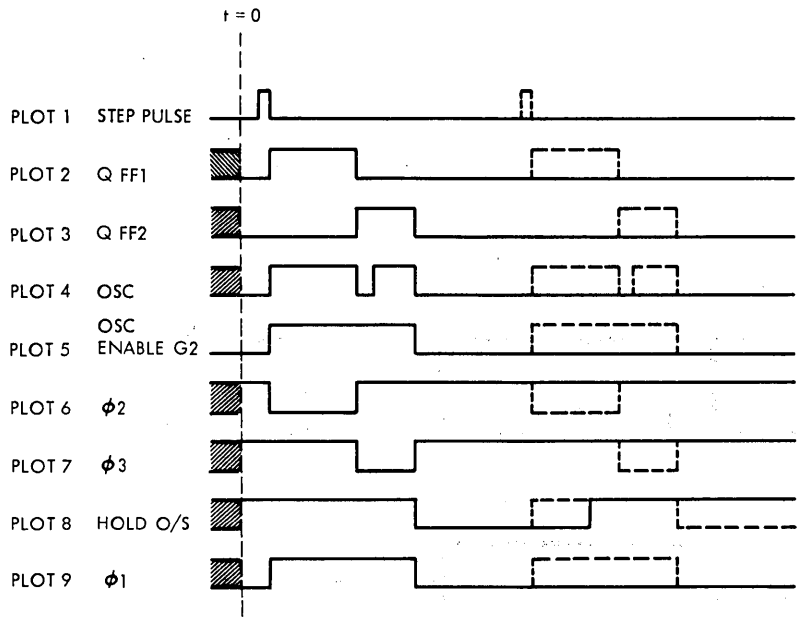


Figure 2-3. Head Positioner Control Timing

The Head Positioner Logic of the drive is controlled by the user system and causes the magnetic head to be positioned at the desired track. The circuitry centers around a phase state generator counter and oscillator. A Step Pulse initiates a series of actions which results in a sequence of 3 pulses which drive the 3 phases of the variable reluctance step motor in sequence. This, in turn, causes three successive steps of the motor shaft which constitute a 1-track movement (approximately 0.021-inch). The last step of this series energizes $\phi 1$ which is the holding phase. In $\phi 1$, the current is reduced following a 40-millisecond (approximately) delay after the last step pulse. This reduced current is sufficient to maintain accurate positioning while reducing power dissapation during long periods of stepper motor inactivity.

To perform a step out function, the required phase sequence is $\phi 2$, $\phi 3$, $\phi 1$; to step in, the sequence is $\phi 3$, $\phi 2$, $\phi 1$. It is important to note that in each case the sequence ends in $\phi 1$, the holding phase.

Referring to Figure 2-2, after power is established, the Head Positioner Logic is initialized with the power sense circuitry. With FF1 and FF2 in the reset state, gate G2 disables the oscillator and enables the $\phi 1$ Hold Driver. The $\phi 1$ Hold Driver provides reduced hold current to $\phi 1$ via resistor R.

In the case when the drive receives a motion command from the interface, the Direction Latch stores direction information and the command is initiated by the Step pulse. The timing for a STEP IN or STEP OUT sequence is shown in Plots 1, 2, and 3 of Figure 2-3.

NOTE

When a Write operation is in progress the Not Write Busy line will be low, inhibiting FF1.

Flip-Flop FF1 sets on the trailing edge of the Step Pulse and allows gate G2 to enable the oscillator and disable the ϕ1 Hold Driver. The output of the oscillator, shown in Plot 4, causes the phase counter Flip-Flop FF2 to increment on each low-going edge. Plots 2 and 3 show the states of FF1 and FF2 at initialization, after the Step Pulse and counting as a result of the oscillator.

At the termination of ϕ3, the output of gate G2 goes low, disabling the oscillator and enabling the ϕ1 Hold Driver. The Hold One-Shot is triggered and the ϕ1 drive is enabled for a period of approximately 40 milliseconds. When the ϕ1 drive is de-energized, the current in the ϕ1 coil reverts to the hold level defined by the ϕ1 Hold Driver and resistor R. This sequence is shown by Plots 6, 7, 8, 9 of Figure 2-3. If a subsequent Step Pulse is received before the Hold One-Shot has finished timing out, the Hold One-Shot is cleared by FF1 going true and the sequence is repeated.

Direction control is provided via the interface and stored in the Direction Latch. The outputs of the Direction Latch are used to drive the Direction Multiplexer which causes the phase sequence of ϕ2 and ϕ3 to reverse in the appropriate manner.

If the read/write head is positioned at track 0, the interface logic is disabled to prevent acceptance of further STEP OUT commands. It should be noted the durations of ϕ2 and ϕ3 are not equal; this is shown in Plots 6 and 7 of Figure 2-3. This imbalance is intentional and results in an improved stepping characteristic.

2.5 POWER SENSE CIRCUITRY

The power sense circuitry monitors the user supplied +24v dc, +5v dc, —5/—12/—15v dc. The circuitry provides an initialization signal to the Head Positioning Logic and status signal to the Write/Erase Current Sources.

2.6 INTERLOCKS AND TRANSDUCERS

2.6.1 INDEX

An Index pulse is provided to the user system via the INDEX PULSE interface line. The index circuitry shown in Figure 2-1 consists of an Index LED, an Index Photo-Transistor, and a Pulse Shaping Network. As the index hole in the disk passes the Index LED, light from the LED strikes the Index Photo-Transistor causing it to conduct. The signal from the Index Photo-Transistor is passed to the Pulse Shaping Network which produces a pulse for each revolution of the diskette. This pulse is presented to the user on the INDEX PULSE interface line.

2.6.2 WRITE PROTECT (OPTION)

A Write Protect signal is provided to the user system via the WRITE PROTECT interface line. The write protect circuitry, shown in Figure 2-1, consists of the Write Protect LED, Write Protect Photo-Transistor assembly, and a Pulse Shaping Network.

When a write-protected diskette is inserted in the drive, light from the LED passing through the write protect hole of the diskette activates the photo-transistor. The photo-transistor output is then passed through a pulse shaping network which provides a logic level used to disable the write electronics. Additionally, the write protect status is presented to the interface.

2.6.3 TRACK 0 SWITCH

The level on the TRACK 0 interface line is a function of the position of the magnetic head assembly. When the head is positioned at Track 0, a true level is generated and is sent to the user system. The Track 0 Latch is activated by the Track 0 Switch and inhibits response to any STEP OUT commands issued by the user.

Two special interlocks are provided to compensate for possible false signals during operation. Refer to Figures 2-2, 2-4, and 2-5 in conjunction with the following paragraphs.

2.6.3.1 Case 1

Consider the head approaching Track 1 as shown schematically in Figure 2-2 and Figure 2-4. Recall that each track movement consists of 3 steps. At the end of the third step, it can be seen that it is possible for the head carriage to overshoot and momentarily activate the Track 0 Switch. However, note that Flip-Flop FF1 presets FF3 and disables gate G3 until FF3 is clocked by the falling edge of the output waveform from the Hold One-Shot. Thus, false indications on the TRACK 0 interface line are inhibited until 40 milliseconds after the last phase step.

2.6.3.2 Case 2

Consider the head carriage during motion from Track 1 to Track 0 as shown schematically in Figure 2-5. In this case, it is possible to have false indications throughout the motion period. False indications are inhibited during this period by presetting FF3 during $\phi 2$ and clocking the flip-flop on the trailing edge of the output waveform from the Hold One-Shot.

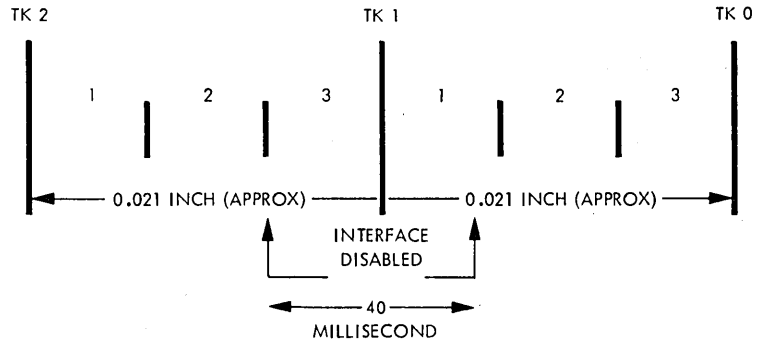


Figure 2-4. Track 0 Operation, Case 1

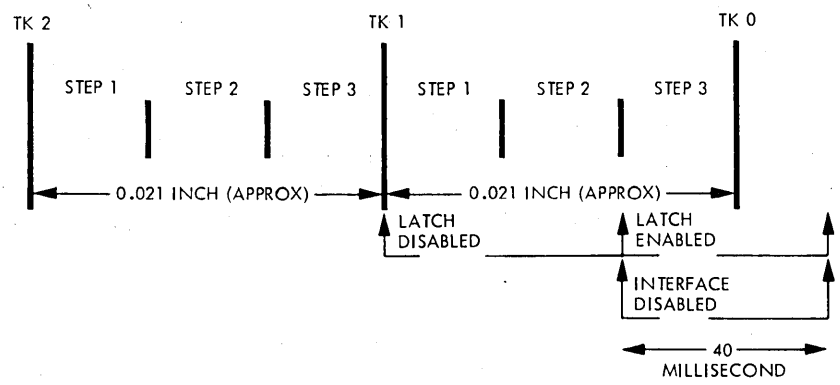


Figure 2-5. Track 0 Operation, Case 2

2.6.4 HEAD LOAD

The head load circuitry consists of a Head Load Solenoid Driver and a Head Load Solenoid as shown in Figure 2-1. A true level on the HEAD LOAD interface line causes the Head Load Solenoid to energize. This action loads the magnetic head and pressure pad assembly against the recording surface of the disk drive. The solenoid will remain energized and the head loaded until the true level is removed from the HEAD LOAD interface line or the disk drive door is opened. The door interlock circuitry detects a door-open condition and disables Head Load Solenoid and the drive motor circuitry on Model FD400. The DOOR OPEN signal is available at the interface for FD400 and FD5X0 models; on model FD5X1 the Door Open signal is part of the Ready Status signal.

2.7 DATA ELECTRONICS

Information is normally recorded on the diskette in a double frequency code. Figure 2-6 illustrates the magnetization profiles in each bit cell for the number sequence shown.

The recording area of the diskette is divided into two zones in accordance with the requirements of the IBM format. Tracks decimal 0 throuh 42 comprise the outer recording zone; tracks decimal 43 through 76 make up the inner recording zone.

A higher write current (10 mA peak-to-peak) is used in the outer zone in order to guarantee good overwrite characteristics.

Since the recording density is higher in the inner zone, good overwrite characteristics can be achieved with a lower write current (8 mA peak-to-peak). This lower write current also enhances the resolution at the higher recording density. A single magnetic head structure is employed in the drive which combines a read/write gap with two tunnel-type trim erase gaps located nominally 0.036-inch behind the read/write gap.

The erase gaps serve to trim the recorded track from 0.013-inch to 0.012-inch and also provide an erased guard band on either side of the recorded track. This provides for tolerances in track positioning.

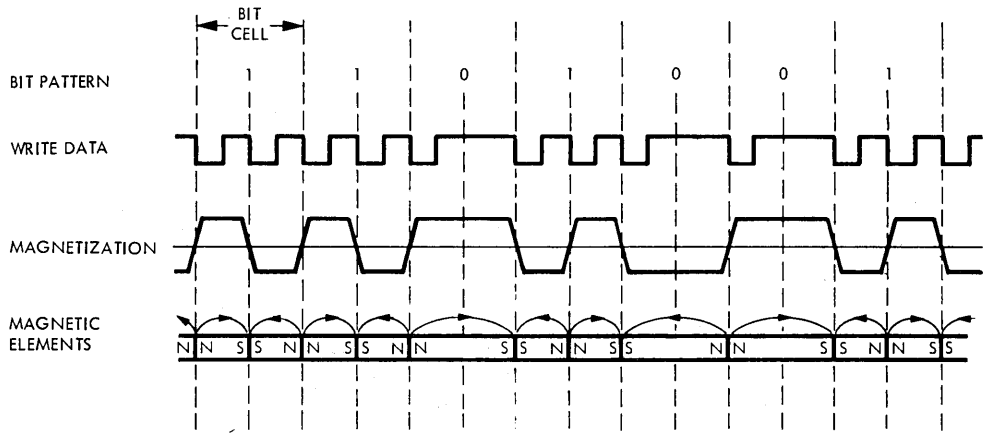


Figure 2-6. Double Frequency Recording

All signals required to control the data electronics are provided by the user system and are shown in the block diagram of Figure 2-7. These control signals are:

- Write Enable
- Trim Erase (External Trim Erase Optional)
- Write Data
- Head Current Switch

The following signals are sent to the user system via the interface and are also shown in Figure 2-7.

- Read Data (Composite)
- Write Busy

2.7.1 DATA RECORDING

Referring to Figure 2-7, it can be seen that the Write electronics consists of a two-value Write Current Source, a Write Waveform Generator, Erase Current Source, and Trim Erase Control Logic.

The write/read winding on the magnetic head is center-tapped; during a write operation, current from the Write Current Source flows in alternate halves of the winding under the control of the Write Waveform Generator.

Before recording can begin, certain conditions must be satisfied. The conditions required for recording (i.e., unit ready) must be established by the user system as follows.

(1) Drive speed stabilization. This condition will exist 5 seconds after starting the drive motor FD400, 2 seconds for FD5XX.

(2) Subsequent to any step operation, the positioner must be allowed to *settle.* This requires 30 msec after the last step pulse is initiated, i.e., 10 msec for the step motion and 20 msec for settling.

(3) Subsequent to a Head Load operation, 40 msec is required for the head-media relationship to stabilize.

(4) The HEAD CURRENT SWITCH line must be appropriately set according to the track position at which recording is required.

NOTE

All of the foregoing operations can be overlapped, if required.

Figure 2-8 shows the relevant timing diagram for a write operation. At t = 0 when the unit is ready, the WRITE ENABLE interface line goes true (Plot 1); this enables the Write Current Source at the value set by the Head Current Switch signal.

Since the trim erase gaps are behind the read/write gap, the TRIM ERASE control goes true (Plot 2) 200 μsec after the WRITE ENABLE interface line. It should be noted that this value is optimized between the requirements at Track 0 and Track 76 so that the encroachment by the trim erase gaps on previous information is minimized.

Plot 4 shows the information on the WRITE DATA interface line; Plot 5 shows the output of the Write Waveform Generator which toggles on the leading edge of every WRITE DATA pulse.

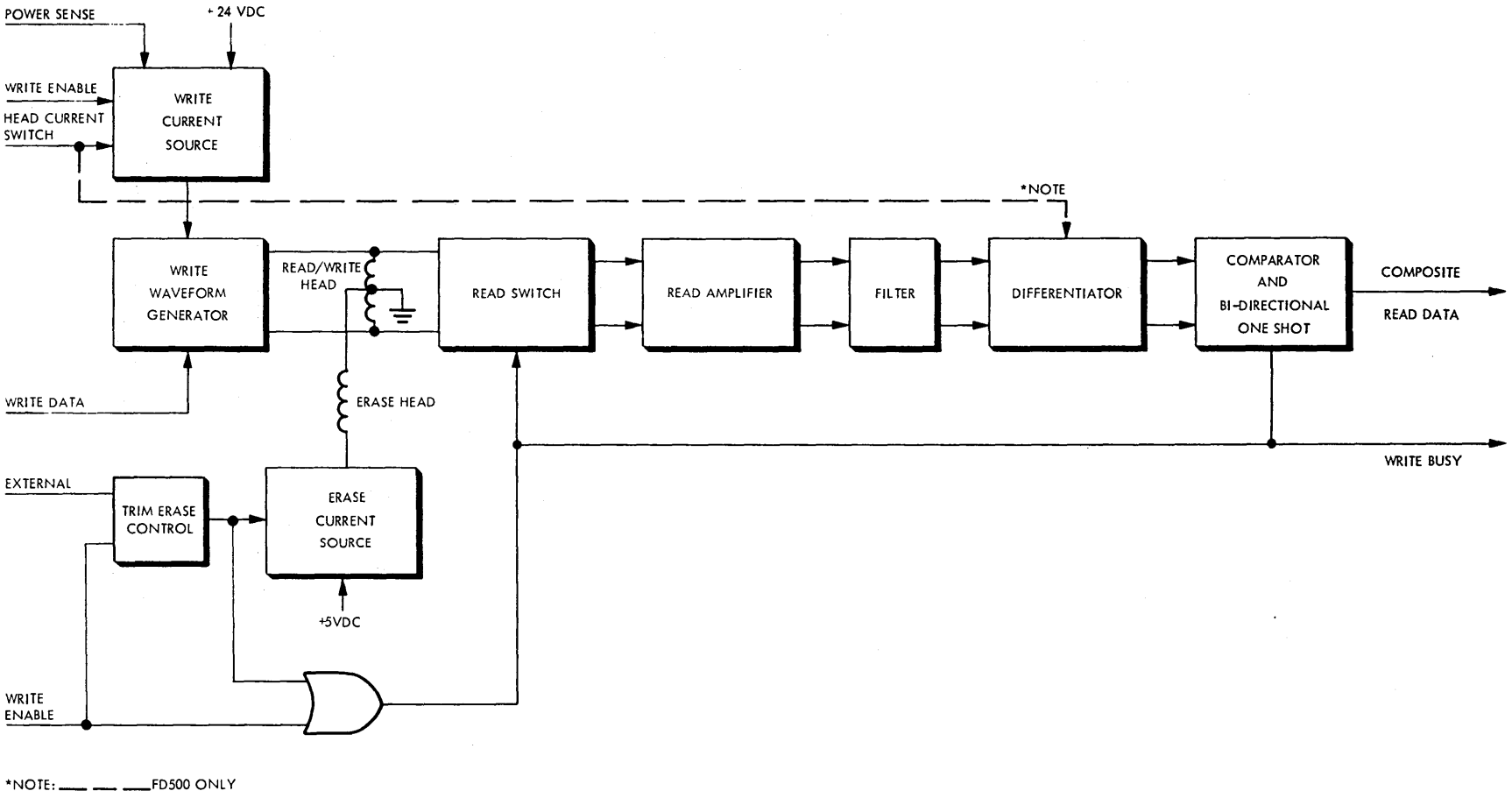
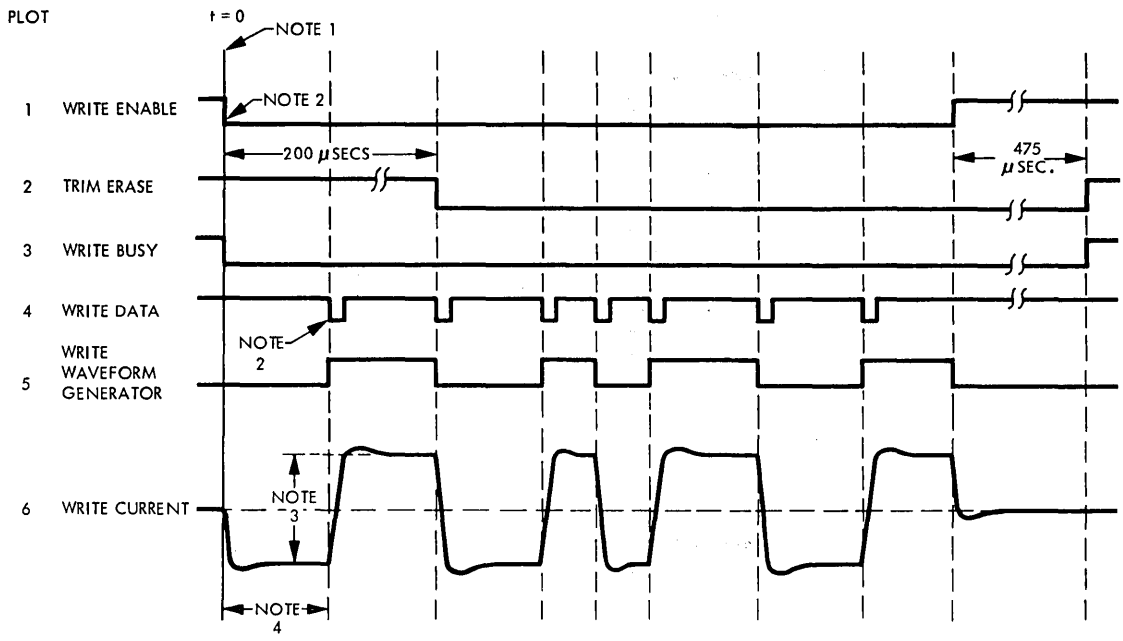


Figure 2-7. Data Electronics Block Diagram



NOTES:
1. t = 0 = 5 SECONDS AFTER DRIVE MOTOR STARTS, OR 40 MILLISECONDS AFTER HEAD LOAD COMMAND, OR 30 MILLISECONDS AFTER LAST STEP PULSE; (WHICHEVER IS THE LATEST TIME)
2. UNSYNCHRONIZED
3. 10 MA PEAK TO PEAK TRACKS 0 - 42, 8 MA PEAK TO PEAK TRACKS 43 - 76
4. 2 μSECONDS MINIMUM, 4 μSECONDS MAXIMUM

Figure 2-8. Write Timing Diagram

Note that Plot 4 indicates a minimum of 2 μsec and a maximum of 4 μsec between WRITE ENABLE going true and the first WRITE DATA pulse. This period is only required if faithful reproduction of the first WRITE DATA transition is significant.

At the end of recording, at least one additional pulse on the WRITE DATA line must be inserted after the last significant WRITE DATA to avoid excessive peak shift effects.

The TRIM ERASE signal (Plot 2) must remain true for 475 μsec after the termination of WRITE ENABLE to ensure that all recorded data are trim erased. This value is again optimized between the requirements at Tracks 0 and 76.

The duration of a write operation is from the true-going edge of WRITE ENABLE to the false-going edge of TRIM ERASE. This is indicated by the WRITE BUSY waveform shown in Plot 3.

NOTE

Further information regarding format and control of the flexible disk is contained in a series of Application Notes, PERTEC Document Nos. 75605, 75607, and 76601.

2.7.2 DATA REPRODUCTION

The Read Electronics are shown in Figure 2-7 and consist of

- Read Switch
- Read Amplifier
- Filter
- Differentiator
- Comparator and Bi-Directional One-Shot

The Read Switch is used to isolate the Read Amplifier from the voltage excursions across the magnetic head during a write operation. The switch is operated by the WRITE ENABLE signal.

Before reading can begin, the drive must be in a ready condition. As with the data recording operation, this ready condition must be established by the user's system. In addition to the requirements established in Paragraph 2.7.1, a 100 μsec delay must exist from the trailing edge of the TRIM ERASE (and therefore of the WRITE BUSY) signal to allow the Read Amplifier to settle after the transient caused by the Read Switch returning to the Read mode.

Referring to Figure 2-9, the output signal from the read/write head is amplified by a *balanced-in/balanced-out* read amplifier and filtered to remove noise by a linear phase Filter. The linear output from the Filter (Plot 1) is passed to the Differentiator which generates a waveform (Plot 2) whose zero crossovers correspond to the peaks of the read signal (Plot 1). This signal is then fed to the Comparator and Bi-Directional One-Shot circuit.

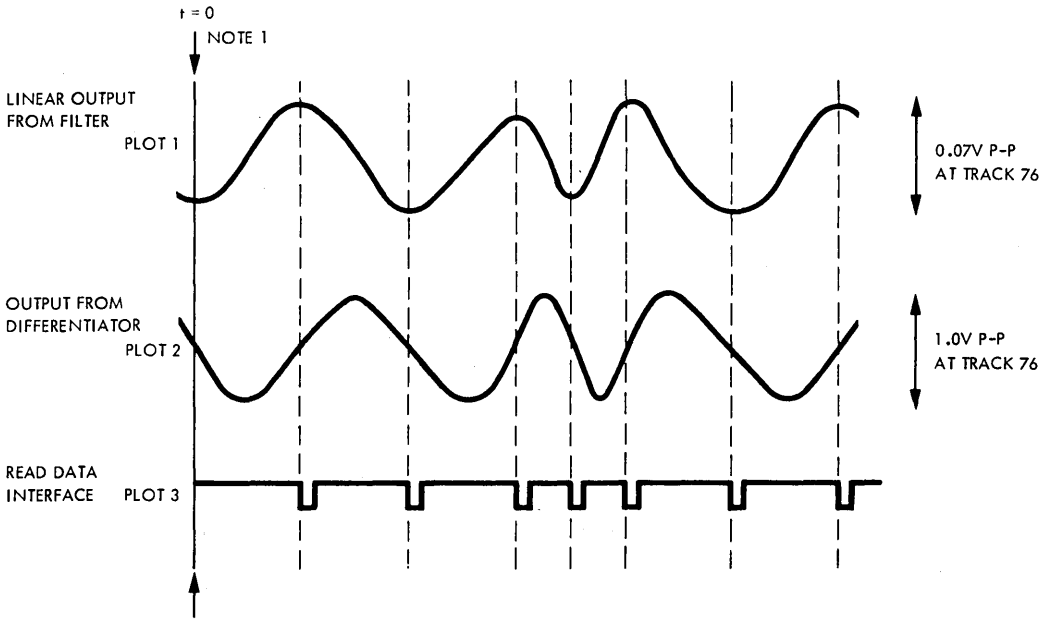


Figure 2-9 Read Timing Diagram

The Comparator and Bi-Directional One-Shot circuit generates a 200-nanosecond READ DATA pulse (Plot 3) corresponding to each peak of the read signal. AC hysteresis is provided in the comparator to eliminate the possibility of multiple detections of the zero crossovers.

This Composite Read Data signal is then sent to the user system via the READ DATA interface line.

During a write operation the Comparator and Bi-Directional One-Shot are disabled by the Write Busy signal.

2.8 SPINDLE DRIVE

2.8.1 FD400 MODELS

The spindle drive system consists of a single stack, 3-phase variable reluctance stepper motor operated in the Slew mode. The motor is directly coupled to the drive hub.

Associated with the spindle drive motor are the electronics required for control. These electronics are shown in Figure 2-10 and consist of the following.

- Drive Motor Oscillator
- Ramp Generator
- 3-Phase Counter
- Control Circuitry
- Current Limit

Initially, when the loading door is open and/or the DRIVE MOTOR ON interface line is false (High) the drive is in the Standby mode, i.e., the motor is stationary.

The 3-Phase Counter is disabled by the high output of gate G1 and the low output of the Detent Gate G3. Thus, drive is removed from three of the motor drivers. The Detent Single-Shot is also reset, disabling the Detent Driver. In this condition the output of G2 is high and the Ramp Generator output causes the Drive Motor Oscillator to operate at 432 Hz.

Refer to the timing diagram shown in Figure 2-11. Closing the door and placing the DRIVE MOTOR ON line true initiates the start-up sequence. The output of G1 goes low (Plot 2) which triggers the 0.6-second Detent Single Shot (Plot 3). This energizes the Detent Driver via G4 (Plot 8) which causes the rotor of the drive motor to be positioned at a reference from which the direction of rotation can be predicted. Also, during the 0.6-second timeout period, the output of G2 is low, and the Ramp Generator output (Plot 4) establishes the Drive Motor Oscillator at the start frequency of approximately 105 Hz. Since the output of G3 (Plot 5) is still low the counter remains disabled.

At the end of the 0.6-second detent period, the outputs of G2 and G3 go high and the 3-Phase Counter generates a sequence of pulses. These pulses energize the ϕA, ϕB, and ϕC drivers as shown in Plots 9, 10, and 11, respectively. In addition, the Detent Driver is de-energized via G4 (Plot 8).

As the motor begins to rotate, the output of the Ramp Generator starts to rise (Plot 4), the oscillator frequency increases approximately exponentially, and the motor speed increases. At the end of the ramp-up period the oscillator is operating at 432 Hz $\pm$1.5%.

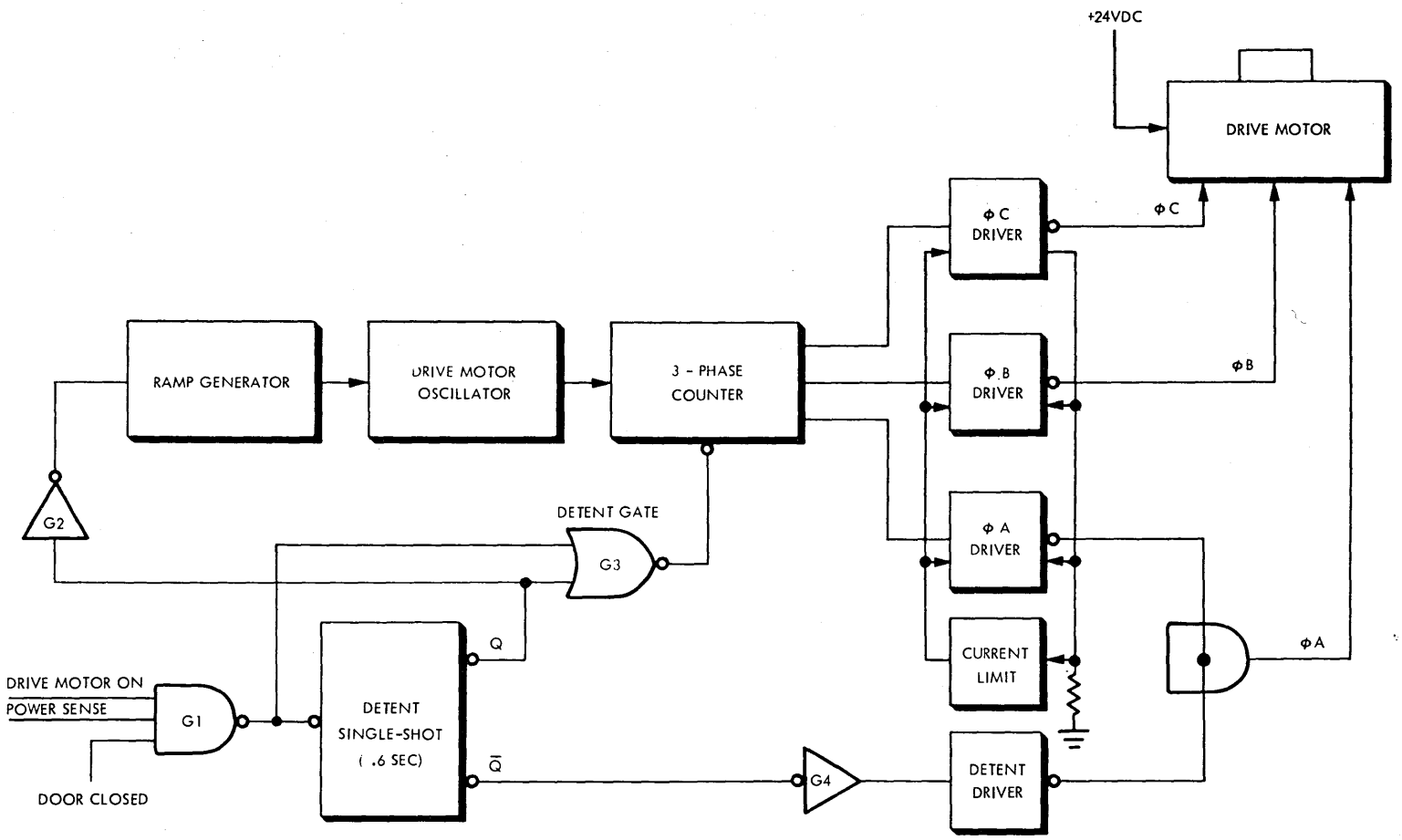


Figure 2-10. Drive Motor System Block Diagram

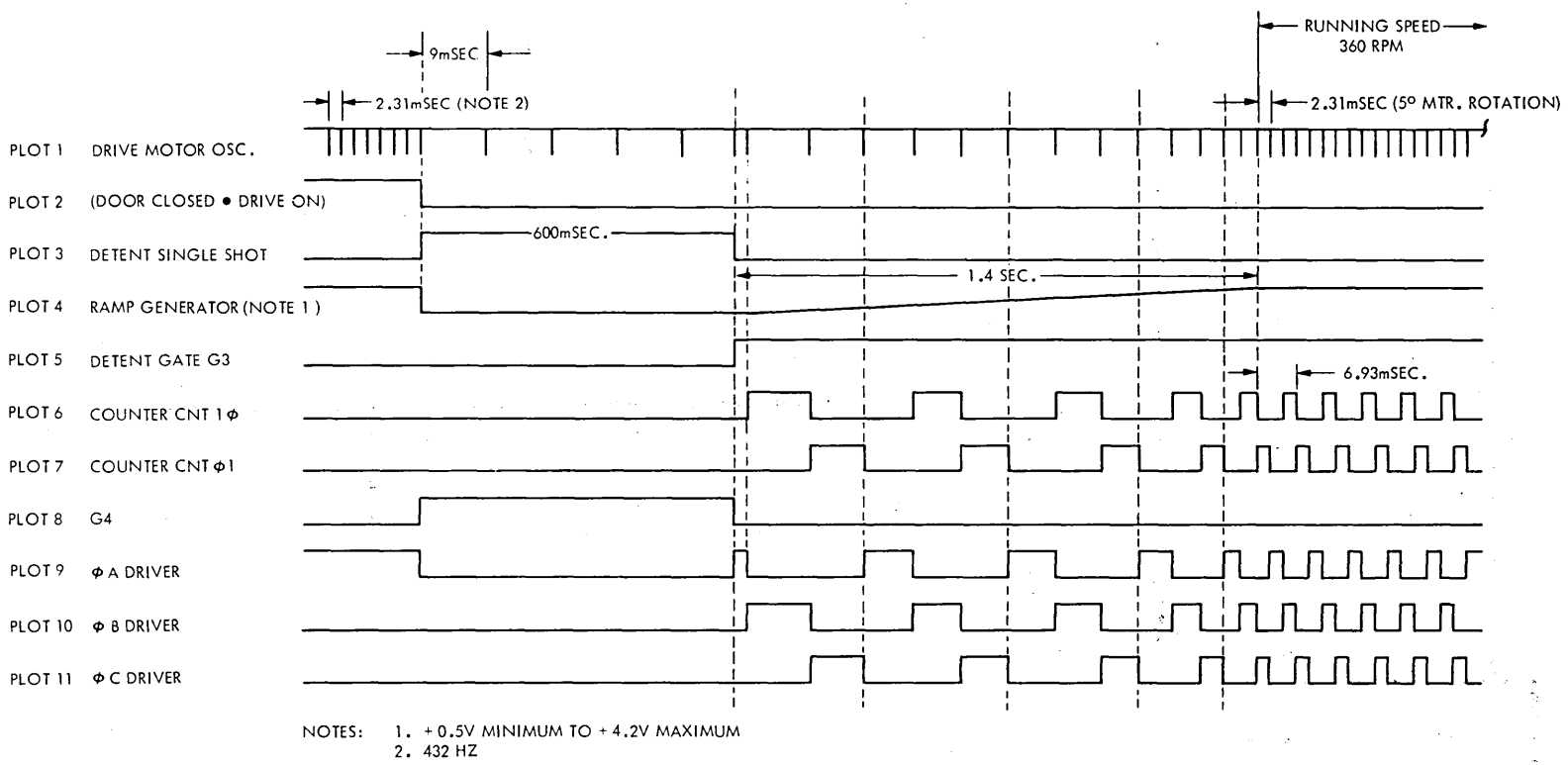


Figure 2-11. Drive Motor Start Sequence

The Drive Motor Oscillator is designed so that the Ramp Generator voltage has no influence on the speed of the motor at the end of the ramp-up period.

The current limit circuitry prevents high starting currents in the dc motor, disabling the output drivers when current greater than 2.7 amps is sensed.

2.8.2 FD5XX MODELS

The FD5XX models are flexible disk drives that operate the spindle motor from user-supplied ac power.

The spindle drive system consist of a permanent split capacitor ac synchronous motor, belt coupled to the drive hub. The voltage and frequency must be specified at the time of ordering. When the drive is energized, the motor is in constant rotation and is not dependent on the condition of the door; i.e., open or closed.

SECTION III
DETAILED ELECTRICAL DESCRIPTION

3.1 INTRODUCTION

This section contains the interface description and the theory of operation for the Printed Circuit Board Assembly (PCBA). Mechanical and electrical adjustments are contained in Section IV. Schematics and assembly drawings are contained at the end of this manual.

3.2 PHYSICAL DESCRIPTION, PCBA NO. 600321, FD400 DISK DRIVES

The PCBA is approximately 10 inches (25.40 cm) long by 7.50 inches (19.05 cm) wide. Figure 3-1 illustrates the placement of test points and connectors.

There are three connectors on the PCBA. J1 is the interface connector and is slotted to mate with a key in the mating plug; J2 is a 30-pin edge connector into which the subassembly connector plugs; and J3 is the connector into which the read/write head plugs.

3.3 INTERFACE DESCRIPTION, PCBA NO. 600321

Table 3-1 lists the input/output and power pin assignments for interfacing the FD400 series disk drive. These signals are described in detail in the following paragraphs.

3.3.1 GENERAL

All interface signals are TTL compatible. The logic true (low) state is represented by +0.4v (maximum); the logic false (high) state is represented by +2.4v (minimum).

Cable used to interface with the disk drive must be 100-ohm twisted pair (or equivalent) with a maximum length of 30 feet.

Figure 3-2 shows the configuration for which the drivers and receivers have been designed.

3.3.2 INTERFACE INPUT

3.3.2.1 Step In/Step Out (2 lines) (ISTI, ISTO)

The Step In/Step Out (ISTI, ISTO) interface lines are used to move the read/write head by one track position. The trailing edge of this pulse initiates the access motion.

A true (low) pulse with a time duration greater than 200 nsec but less than 2 msec on the ISTI line moves the read/write head by one track position toward the center of the disk.

A true (low) pulse with a time duration greater than 200 nsec but less than 2 msec on the ISTO line moves the read/write head by one track position away from the center of the disk.

The repetition rate for the ISTI and ISTO pulses must be such that the time interval between two consecutive pulses is between 10 and 11 msec. If this condition is not satisfied, then two consecutive ISTI or ISTO pulses must be separated by a time interval greater than 30 msec.

When attempting a multi-track seek operation, optimum access time is realized by issuing ISTI or ISTO pulses at intervals between 10 and 11 msec.

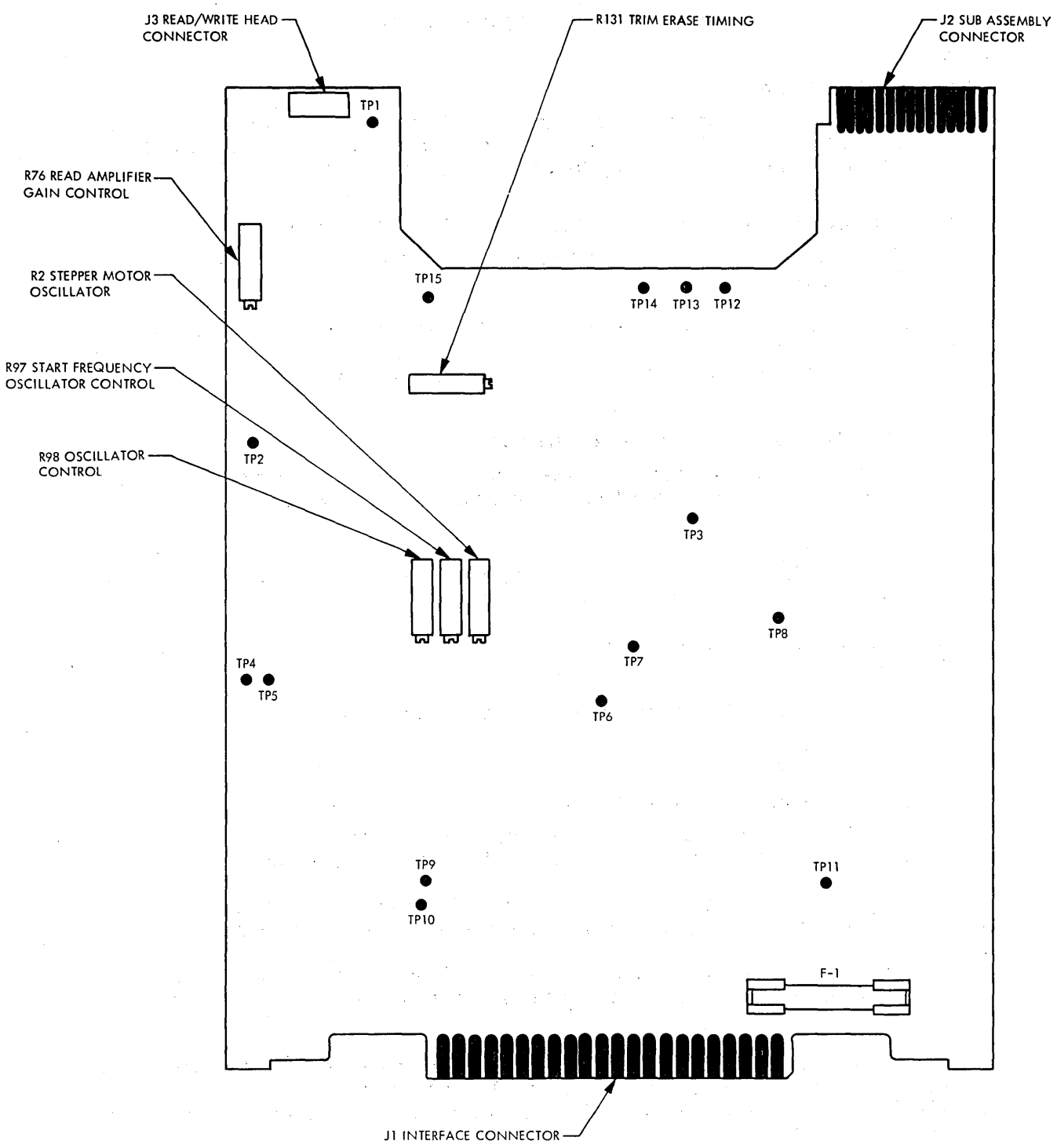


Figure 3-1. Placement of Test Points and Connectors for PCBA No. 600321

Table 3-1
Standard Interface Pin Assignment

	Signal	Line	Ground
Input Control	STEP IN (ISTI)	11	M
	STEP OUT (ISTO)	15	S
	DRIVE MOTOR ON (IDEN)	18	V
	HEAD LOAD (IHLD)	16	T
	HEAD CURRENT SWITCH (IHCS)	7	H
	WRITE ENABLE (IWEN)	9	K
	EXTERNAL TRIM ERASE (Option) (IEEN)	8	J
	Not Applicable	2	4
Output Status	TRACK 0 (ITRK0)	19	W
	INDEX (IINXP)	17	U
	DOOR OPEN (IDOP)	6	F
	WRITE PROTECT (IWPT)	13	P
	WRITE BUSY (IWBSY)	1	3
Data	WRITE DATA INPUT (IWDA)	10	L
	READ DATA OUTPUT (IRDA)	20	X
Power	+ 24V DC	A,B	C,D,E
	+ 5V DC	21	Y
	—5V DC (—15V DC)(Option)	22	Z

- Interface Connector Body AMP Inc. No. 583859-3 Contacts 1-583853-1, or equivalent.
- Keying slot located between pins 5 and 6.

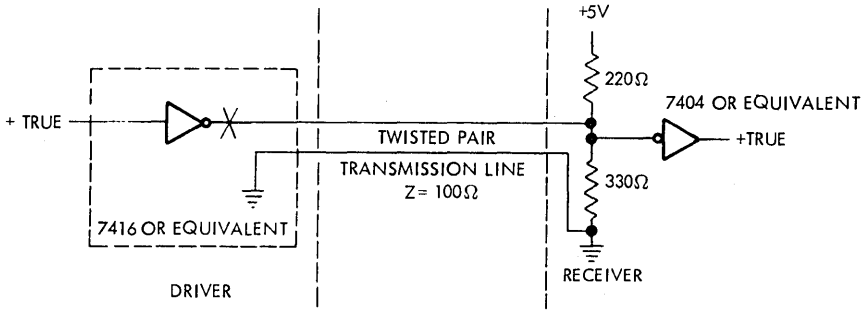


Figure 3-2. Typical Driver/Receiver Configuration

Two consecutive pulses on these lines, involving a change in the direction of motion, must be separated by a time interval not less than 30 msec.

When the read/write head is positioned on track 0, an ISTO pulse requiring motion away from the center of the disk is ignored. The head motion is inhibited if either the Write Enable or the Erase Enable signal line is true (low). A Read/Write command must not be attempted within 30 msec after issuing a Step In or Step Out pulse which results in head motion.

3.3.2.2 Drive Motor Enable (IDEN)

When the Drive Motor Enable (IDEN) line goes true (low), the drive motor accelerates to a nominal speed of 360 rpm and stabilizes in less than 5 seconds. When IDEN goes false (high), the drive decelerates to a stop in less than 5 seconds.

3.3.2.3 Head Load (IHLD)

The Head Load (IHLD) interface signal activates the Head Load actuator to move the read/write head and pressure pad into contact with the disk. When IHLD is true (low), the read/write head remains in contact with the disk. When IHLD is false (high), the head load actuator is deactivated; this moves the read/write head and pressure pad away from the disk. A Read/Write command must not be attempted within 40 msec after the IHLD line goes true (low).

3.3.2.4 Head Current Switch (IHCS)

The Head Current Switch (IHCS) interface line must be true (low) for a write operation on tracks 43 through 76. A true (low) on this line selects the lower of two write current values. The interface line must be false (high) for a write operation on tracks 0 through 42. A false (high) on this line selects the higher of two write current values.

3.3.2.5 Write Enable (IWEN)

When the Write Enable (IWEN) interface line is true (low), the write electronics are prepared for writing data (the read electronics are disabled). This signal turns on write current in the read/write head. Data are written under the control of the Write Data Input line. It is generally recommended that changes of state on the Write Enable line occur before the first Write Data pulse. However, the separation between the leading edge of Write Enable and the first significant Write Data pulse should not be less than 2 μsec or greater than 4 μsec. The same restrictions exist on the relationship between the last significant Write Data pulse and the termination of the Write Enable signal. When the Write Enable line is false (high), all write electronics are disabled.

If a FD400 disk drive is installed with the Write Protect Option, and if the diskette is write protected, the Write electronics are disabled irrespective of the state of the Write Enable line.

3.3.2.6 External Trim Erase (Option) (IEEN)

When the External Trim Erase option is incorporated in the disk drive, the IEEN interface signal provides independent control of the trim erasure of data recorded in the track.

When IEEN is true (low), the erase current is allowed to flow in the erase head; when IEEN is false (high), the erase current is disabled.

If a FD400 disk drive with the Write Protect option is installed, and if the diskette is write protected, the Trim Erase electronics are disabled irrespective of the state on the Trim Erase line.

When the Write Enable line goes false (high), the erase current must remain enabled for a period of time thereafter to ensure that all the recorded data is trim erased. The gap between the read/write head and the erase head is 0.036 ±0.002 inch. Minimum time is defined as the minimum erase gap time and results from tolerances arising from the head, track position, and diskette speed. The value is 475 μsec.

When the Write Enable line goes true (low), a delay must be incorporated before the External Trim Erase line is allowed to go true. This is to avoid erasure of previously recorded information, which can occur when fixed header formats are utilized.

The value of this delay must be calculated with respect to tolerances in the head, track location, and diskette speed, and with respect to the format used.

3.3.2.7 Write Data Input (IWDA)

The Write Data Input (IWDA) interface line provides the bit-serial write-data pulses that control the switching of the Write current in the head.

When the Write electronics have been conditioned for writing by a true (low) state on the Write Enable line, each high-to-low transition on the Write Data line, a flux change is produced at the (write) head gap. This causes a flux change to be stored on the medium.

The double-frequency type encoding technique is normally used in which data and clock form the combined Write Data signal. It is generally recommended that the repetition rate of the high-to-low transitions when writing all zeros be equal to the nominal data rate ±0.1 percent. The repetition rate of the high-to-low transitions when writing all ones should be equal to twice the nominal data rate ±0.1 percent.

3.3.3 INTERFACE OUTPUT

3.3.3.1 Index (IINXP)

The Index signal is provided once each revolution (166.67 msec nominal) for the duration of 2.5 ±1 msec to indicate to the controller the beginning of a track. The Index line remains in the true (low) state for the duration of the Index pulse.

The leading edge of the Index pulse must always be used to guarantee diskette interchangeability for the FD400 series disk drive.

3.3.3.2 Door Open (IDOP)

The Door Open (IDOP) line goes true (low) when the loading door of a disk drive is opened. IDOP goes false (high) when the door is closed.

It is important to note that the head load solenoid is de-energized when the door is opened, irrespective of the state of the Head Load interface line.

3.3.3.3 Write Protect (IWPT) (Optional)

The Write Protect (IWPT) line goes true (low) when the diskette is write protected. The write electronics in the FD400 disk drive are disabled internally when the diskette is write protected.

When IWPT is false (high), the write electronics are enabled and the write operation can be performed. It is generally recommended that the controller not issue a Write command when the Write Protect signal is true (low).

3.3.3.4 Read Data Output (IRDA)

The Read Data Output (IRDA) interface line transmits readback data to the controller. It provides a pulse for each flux transition recorded on the medium. The IRDA line goes true (low) for a duration of 200 ± 50 nsec for each flux change recorded on the medium.

During a Write operation, Read Data pulses are inhibited for the duration of the true (low) state on the Write Busy line (see Paragraph 3.3.3.6).

Read Data pulses are invalid for a period of 100 μsecs after the Write Busy line goes false (high) (see Paragraph 3.3.3.6).

If the Write Enable line is false (high) and the head is unloaded, spurious pulses of random frequency will be present on this interface line.

It is recommended that the Write Data Input line be disabled in addition to the Write Enable line during the Read operation.

3.3.3.5 Track 0 (ITRK0)

The Track 0 (ITRK0) interface signal alerts the controller that the read/write head is positioned on track 0. ITRK0 remains true (low) until the head is moved away from track 0.

ITRK0 goes true (low) approximately 50 msec after the trailing edge of the Step Out command pulse that positions the read/write head on track 0. Step Out command pulses issued after the 9 msec period from the trailing edge of the Step Out command pulse that positions the read/write head on track 0 are ignored.

3.3.3.6 Write Busy (IWBSY)

The Trim Erase function in the FD400 disk drive is provided internally. Since a Write operation starts when the Write Enable line goes true (low) and terminates when the Trim Erase current is turned off, it is necessary to signal the controller when the (internal) Trim Erase function is complete.

This information is provided on the Write Busy interface line, which is true (low) whenever the Write Enable or the (internal) Trim Erase functions are energized. In particular, the line goes true (low) when Write Enable goes true (low) and false (high) at the completion of the (internal) Trim Erase function.

When the External Trim Erase option is installed, the Write Busy interface line still goes true (low) whenever the Write Enable or the External Trim Erase functions are energized.

3.4 CIRCUIT DESCRIPTION, PCBA NO. 600321

3.4.1 HEAD POSITIONER LOGIC

The Head Positioner Logic, including the Track 0 circuits, are shown on Schematic No. 600320, sheet 2. Refer to the functional description given in Paragraph 2.4 in conjunction with this description.

Positioner control is a function of gated oscillator U13 (zone G7), phase state generator U14 (zone E5), and the requested motion direction pulse (ISTI or ISTO) from the interface.

The Step pulses are received and terminated by gates U29 (zone F7) pin 5 (ISTI) and U23 pin 9 (ISTO). The respective outputs of U29 and U23 are used to set the Direction Control Latch 23 (zone D5) pins 2 and 6 and to initiate the motion sequence through U23 pins 11, 12, and 13 (which can be observed at TP11) and U29 (zone E6) pins 9 and 8.

Initial conditions are established by the Power Sense circuitry (NPSEN) through U22 and U29. NPSEN places both flip-flops of U14 (zone E6, E5) in the reset state. Oscillator U13 is held inactive by U20 (zone F4) pin 6 and will remain inactive until U14 pin 15 or pin 11 is high.

Upon receipt of a Step pulse, U14 pin 15 will go high if Not Write Busy (NWBSY) is high and is not cleared by U22 pin 4. U14 pin 15 sets on the trailing edge of the Step pulse. When U14 pin 15 goes high, the oscillator is enabled via U22 and U20; additionally, $\phi 1$ of the stepper motor drive is disabled by U30 (zone F2) pin 2.

The output of Oscillator U13 pin 3, which can be observed at TP7, goes high for a period of time determined by the time for capacitor C2 to charge to the high internal threshold of U13 pin 6 through R1 + R2 + R3. When the sense threshold of U13 pin 6 is reached, U13 pin 3 goes low for a period of time determined by the time for C2 to discharge to the low threshold through R3. At this time U13 pin 3 goes high again (if U13 pin 4 is still enabled) then the oscillation process repeats itself. Oscillator U13 typically generates two consecutive positive periods of unequal duration for each Step pulse. The unequal durations are a result of the first charging cycle that occurs each time U13 is enabled; C2 initially charges from a voltage level lower than the threshold level achieved during sustained oscillator operation. The output of the oscillator is shaped by U20 pins 3 and 4 then inverted for proper polarity by U15 pins 9 and 8.

The oscillator clocks U14 pins 6 on the high-to-low transition. U14 pin 11 is initially reset but goes high on the trailing edge of the first internal clock pulse initiated by a Step command. This change causes U14 pin 3 to reset through U22 pin 4 and continues to enable oscillator U13. The output states of U14 are directed via the Direction Multiplexer U28 (zone F4) to the $\phi 2$ or $\phi 3$ pre-driver dependent on the state of the Direction Latch U23. If a Step In command (ISTI) had been issued, U23 pin 4 would be high enabling $\phi 3$ pre-driver for the state of U14 pin 15 and $\phi 2$ pre-driver for the state of U14 pin 11. The sequence established allows first $\phi 3$ to be active, then $\phi 2$. The second clock pulse causes U14 pin 10 to go high; this transition triggers single-shot U17 (zone G4) for approximately 40 msec. U17 pin 12 energizes the $\phi 1$ Driver transistor Q1 (zone G2). Additionally, the reset states of U14 causes the $\phi 1$ hold driver (transistor Q2) to be energized via U22, U20, and U30. If the disk drive incorporates the Power Save feature, the positioner $\phi 1$ will be disabled if the head is unloaded (IHLD false) through U24, U9, W5 and W6.

The output drive circuitry for $\phi 1$ consists of transistors Q1 and Q2. Transistor Q1 is used as the Phase Driver, allowing full current through $\phi 1$. Transistor Q2 is used as a hold or detent driver operating at a reduced current through a 33-ohm resistor (across pins 10 and 12 on P2) mounted external to the PCBA. Transistors Q3 and Q4 provide the drive for phases $\phi 2$ and $\phi 3$, respectively.

The Track 0 circuitry relies on a *form-C* switch that is de-bounced by a cross-coupled latch formed by U15 (zone C4) pins 3 and 5. When active, the Track 0 Latch disables the interface receiver U23 (zone E7) pin 8 from receiving any additional Step-Out commands. The output of the Track-0 Latch is also provided to the interface via U22 and U9 (zone D2). The status is only allowed to propagate through the interface (J1-19) after the time-out associated with the $\phi 1$ one-shot, U17. The high-to-low transition of U17 pin 5 clocks U4 (zone D3) pin 11 and enables U22 pin 9.

3.4.2 POWER SENSE CIRCUITRY

The Power Sense circuit, shown on Schematic No. 600320, sheet 2 (zones B7-D7), consists of the under-voltage monitors of +24v dc, +5v dc and —5v dc. The +24v dc supply distribution is fused by F1 at 3 amps.

Initial conditions assume that all supplies are at their zero value and all components are inactive, i.e., capacitors discharged.

Application of dc power can be sequential or simultaneous. In either case, initialization of the drive electronics is dependent on the last of the three dc voltages that achieves its minimum sense value. The control elements are the charged state of capacitor C6, and the logic threshold of U20 (zone D6) pin 9. Capacitor C6 is not allowed to charge until the three dc sense voltages have been reached. For the +24v dc supply, the sense circuitry consists of transistor Q5, VR1, R16 and R18. The base of Q5 is controlled by the conduction of VR1 through R16 and R18 and will not conduct until the +24v dc has exceeded 17.6v dc. If the other voltages have been established, capacitor C6 is allowed to charge; if not, resistor R20 diverts the charge current to transistor Q7 or Q28.

Transistors Q6, Q7, zener diode VR2 and resistors R21, R22 and R23 sense the +5v dc supply. Transistor Q7 relies on the state of Q6 and the +24v dc supply. Transistor Q6 will not turn on until the +5v dc supply has reached +4.3v dc or greater; at that time zener diode VR2 will conduct and establish a turn-on voltage for Q6 via R21 and R23.

The negative voltage supply is sensed off the common tie of jumpers W1 and W2. If the —5v dc operation is required, W1 is installed and W2 is omitted. If the Negative Voltage option (—12v dc/—15v dc) is required, W1 is omitted and W2 is installed. Resistors R24, R121, and zener diode VR3 form a —5v dc regulator. Resistors R119, R120, zener diode VR5, and transistor Q28 sense the —5v dc supply.

The signals supplied from the power sense circuitry are NPSEN which is used for the positioner logic and enables the Drive Motor Enable receiver U8 pin 9 (sheet 6, zone E7), and APSEN which is used for the analog write circuitry.

3.4.3 INTERLOCKS AND TRANSDUCERS

The Interlocks and Transducers circuitry are shown on Schematic No. 600320, sheet 3.

The terminating amplifiers for the Index pulse and Write Protect transducers are similar. Operational amplifiers U21 and U27 (zones F, G-6) compare the conduction of their respective photo-transistors with a reference level set by R27, R29, R31, and R33. Diodes CR4 and CR5 clamp the outputs from any negative excursions.

The Index signal (IINXP) consists of a pulse for each rotation of the index hole in the diskette. It is important that the transition edges of each pulse be sharp. Schmitt trigger gate U20 (zone G6) provides controlled hysteresis to ensure these sharp transitions (which can be observed at TP10). U6 is the driver for the IINXP interface signal (J1-17).

In the Write Protect circuitry, it is important only to detect the presence of a Write Protected diskette hole. Therefore it is sufficient to route the output of the sense amplifier through a conventional gate, U9 (zone F6) for level changes, then to the interface as IWPT on pin 13 of connector J1.

The Door-Open Indication switch is conditioned by a cross-coupled latch formed by U15 (zone G3) pins 1 and 13. This signal provides status to the interface through U6 (zone G2) pin 1, a control signal to the Drive Motor logic U11 pin 2 (sheet 6, zone D6), and disables the Head Load gate U8 (zone F3) pin 5. The Head Load signal (IHLD) on pin 16 of connector J1 activates the Head Load Solenoid Driver consisting of U24 (zone F3) pin 6, resistors R38, R39, and transistor Q9.

3.4.4 WRITE/ERASE LOGIC

The Write/Erase Logic circuitry is shown on Schematic No. 600320, sheet 4.*

3.4.4.1 Write Waveform Generator

At the beginning of a Write operation, the Write Enable interface signal (IWEN) on connector J1-9 goes true. If the disk drive has the Write Protect option and the diskette is not write protected, the output of U8 (zone E7) pin 1 goes high; this can be observed at TP14. The high output of U8 pin 1 removes the clear signal to pin 3 of the Write Data flip-flop U4. The Write Data flip-flop is now in a reset state conditioned to respond to write data information. The Write Enable Interface signal enables gate U5 (zone E6) pin 5 and 6 and gate U8 (zone D4) pin 12. This action enables the write current source (U7 pins 1 and 2) and provides a Write Busy status signal to the interface.

The composite write clock and data signals (double frequency encoding) are received through connector J1-10 (Write Data Input). These signals are inverted twice by U29 pin 11 and U15 pin 11, then presented to the clock input of the Write Data flip-flop U4 pin 1. The Write Data flip-flop is toggled on the high-to-low transition of each pulse, changing the direction of the current flowing in the magnetic head.

The outputs of Write Data flip-flop U4 pins 15 and 14 are processed by the level-changing circuit comprised of U6 pins 3 and 5, and resistors R55, R56, R57, and R58. The outputs of the level-changing circuits, node of R55 and R56, node of R57 and R58, are fed to Write Drive Switch transistors Q17 and Q18 (zones E, F-5). The emitters of these transistors are tied together to the collector of Q14 (zone G5), the Write Current Source. The collectors of Q17 and Q18 are routed to the center-tapped magnetic head through diodes CR10 and CR11, which results in the required write current waveform. Resistor R61 dampens the Read/Write head and its value is chosen for an optimum current waveform.

The basic current source of voltage reference components VR4, CR8, R53 and R54 (zone G6). These components establish a voltage differential across R47 and the base-emitter junction of Q14. Thus, transistor Q14 and R47 forms the basic current source of approximately 4 ma. An additional current source is formed by U7 pin 5, R49, R50, R129, and Q16. This source is energized via U11 (zone D6) pin 6 whenever the Head Current Switch (IHCS) interface signal on connector J1-7 is high. This causes an additional 1 ma (totaling 5 ma) to flow into switch transistors Q17 and Q18.

During system power-up or loss of one of the dc voltages, the write current source is disabled by circuitry consisting of R125, R126, R127, Q29, and Q30 (zone H6). When control signal APSEN goes low, transistor Q29 turns off, thereby turning Q30 (zone H5) off. This action prevents erroneous information from being recorded during system power up or loss of one of the dc voltages.

Diodes CR10, CR11 and resistors R59 and R60 are not functionally required for the write circuitry but provide isolation of the sensitive read circuits from the write circuitry. During a read operation, the head windings are approximately at ground potential; diodes CR10 and CR11 are cut off by the —5v dc return through R59 and R60.

3.4.4.2 Erase Current Driver

The Erase Current Driver circuitry consists of U9 (zone B4) pin 4, C47, R64, R65, R66, R67, R68, R132 and Q19 (zone B2). These components control and form an erase current source of approximately 85 ma. The circuit is disabled by signal APSEN via R133, Q31 and enabled by either the Internal Trim Erase components, or (as an option) the External Erase (IEEN) interface line on connector J1-8. Jumpers W3 and W4 are exclusive and configure the circuit to respond to the Internal or External Erase commands.

The Internal Trim Erase timing is controlled by a dual single-shot U10, C15, C16, R62, R63, and R131. Upon receipt of Write Enable going high, U10 pin 12 is active and provides a pulse of approximately 200 μsec in duration. This pulse provides a *pre-delay* to turn on of the erase driver via U11 pin 8 and U11 pins 12 and 11. At the completion of the write operation, Write Enable (IWEN) goes false and causes the second half of U10 (zone B4) pin 4 to go active. The pulse from the second single-shot provides a *post-delay* to turn off of the erase driver for approximately 475 μsec via U11 pins 13 and 11. The value of this delay can be adjusted by R131 and optimized to tolerances arising from head, track position, and diskette speed.

The Write Enable and Trim Erase signals are ORed through U8 pin 13 and provides a Write Busy status through U29 pins 1 and 2 and U30 pins 9 and 8 to the interface on pin 1 of connector J1. The Write Busy signals of appropriate polarity are routed to the positioner logic and the read logic.

3.4.5 READ AMPLIFIER

The Read Amplifier and associated digital circuitry is shown on Schematic No. 600320, sheet 5.

3.4.5.1 Read Switch

The Read Switch circuitry consists of components CR12, CR13, CR14, CR15, CR16, CR17,CR18, CR19, R69, R70, R71, R72, R73, R74, R75, Q20 (zone G7) and non-inverting gate U6 (zone G6) pins 9 and 8. This switch isolates the Read Amplifier from the considerable voltage excursions across the magnetic head that occur during a write operation. During a write operation, the Write Enable interface line is low. This signal is inverted by U5 pins 5 and 6 (Write Logic, sheet 4, zone E6), the output of U5 pin 4 (NWRT) is low causing the output of U6 pin 8 to go low. U6 pin 8 turns on the Read Switch transistor Q20 (zone G7) via R69 and R70. The collector of Q20 is now at approximately + 24v dc so that the anodes of CR12 and CR13 are *pulled* positive. The junctions of CR12 and R74, CR13 and R75 are pulled positive thereby cutting off CR14, CR15, CR17, and CR18. Diodes CR16, CR19 and resistors R72, R73 clamp the inputs of U1 (zone D6) so that U1 never goes higher than a diode voltage drop.

During a read operation, Write Enable is high; therefore Q20 is cut off and CR12, CR13 are back biased. The anodes of CR14 and CR17 are at approximately zero volts because they are connected through the low impedance head windings to ground. Approximately 0.20 ma of current is available through resistors R72 and R73. Additionally, 0.40 ma is demanded by R74 and R75 so that each of the four diodes (CR14, CR15, CR17, CR18) have approximately 0.20 ma of current flowing.

In this condition the diode bridge provides a low impedance path for the head signal to preamplifier U1. Capacitor C18 decouples any read switch noise to ground.

3.4.5.2 Preamplifier

The Preamplifier is a balanced-in/balanced-out high-pass circuit whose gain is controlled by resistors R76, and R77. Capacitor C19 is the reactive component that establishes the high pass characteristic of the amplifier. Potentiometer R76 is provided to allow gain adjustment, compensating for different read head sensitivities thus reducing the dynamic range requirements of the system.

A gain of approximately 20 is used to avoid problems encountered by amplification of the small dc offset introduced by Read Switch. The signal level, measured differentially between pins 7 and 8 of U1, is approximately 250 mv for an all-ones pattern at track 0.

3.4.5.3 Filter

The balanced output from U1 is fed via the linear phase filter L1, L2, L3, L4, C30 to a terminating network consisting of C21, C23, R78, and R80. This filter has a linear phase response over the frequency of operation and attenuates the high frequency noise from the signal.

3.4.5.4 Differentiator

The output of the filter is fed to the differentiator circuit U2 (zone D4). Capacitors C21 and C23 are used to couple the filter to amplifier U2 and to isolate any dc offset voltage at the output of U1. Amplifier U2 is similar in operation to preamplifier U1 with the exception that the gain network is fixed and provides a 6 db-per-octave gain rise characteristic over the frequency range of operation, thus providing the required differentiator characteristics. The gain components are R79 and C24.

3.4.5.5 Zero-Crossing Detector

The output of U2 is fed to emitter followers Q21 and Q22 to prevent the output from being improperly loaded. The emitters are ac coupled to inputs of the Zero-Crossing Detector, U3, whose inputs can be observed at TP4 and TP5.

U3 (zone D3) is a bi-directional one-shot that accepts the differential read signal. The output of U3 pin 11, which can be observed at TP9, is a single 200 nsec ±50 nsec pulse from each and every zero crossover. The pulse width is determined by capacitor C26 and resistor R86. Ac hysteresis is provided by C29 and R91 to eliminate the possibility of multiple detection of zero crossover.

U3 pin 3 is disabled by the Write Busy (WBSY) signal. The output of U3 pin 11 is fed to interface driver U9 pin 5, then to connector J1-20 Read Data (IRDA).

3.4.6 SPINDLE MOTOR LOGIC/DRIVE

The Spindle Motor Logic /Drive circuitry is shown on Schematic 600320, sheet 6. Refer to the functional description given in paragraph 2.8 and the corresponding timing diagram (Figure 2-11) in conjunction with this description.

The Drive Motor Enable interface line, (IDEN, connector J1-18, zone E7) is terminated at gate U8 pin 8. When IDEN is low and there are no power supply faults (NPSEN low), U8 pin 10 goes high. If the loading door of the disk drive is closed (NDOP high), U11 pin 3 goes low causing the detent single-shot U17 (zone E6) to time out. The single-shot timing is controlled by capacitor C37 and resistor R101 which results in a nominal time out of 0.6 seconds. During the active period of the single-shot, U17 pin 4 is low and energizes the detent driver, Q24, through U30 pin 13 and 12. The detent driver energizes ϕA of the spindle motor at a reduced current level through resistors R104 and R105 (zone 3). Also during this time U17 pin 13 goes high which (a) resets phase counters U16 thru U5 pin 13, (b) disables ϕA driver Q25 through U24 pin 8, and, (c) causes U9 (zone H5) pin 12 to go low. With U9 pin 12 low, CR20 is forward biased allowing C33 (zone H4) to discharge, thus turning off FET Q23 (zone H4).

FET Q23 controls the frequency of Drive Motor Oscillator U12 (zone G3). With Q23 off, the oscillator will oscillate at the start frequency of approximately 105 Hz. This frequency is determined by capacitor C35 and resistors R96, R97, R98, R99 and R100. Potentiometer R97 provides independent adjustment of the start frequency.

At the end of the 0.6 second single-shot timeout, detent drive Q24 is switched off; ϕA driver is enabled and the clear is removed from phase counter U16. The output of drive motor oscillator U12 pin 3, which can be observed at TP3, is shaped and inverted by U20

(zone G3) pins 13 and 12, then fed to the phase-counter clock inputs U16 pins 6 and 1. Additionally, at the end of the detent period, the output of U9 (zone H5) pin 12 goes high and capacitor C33 charges exponentially through R95 towards +5v. The FET characteristics are such that the oscillator freuency changes in an approximately linear fashion from 105 Hz (Start Frequency) to the required 432 Hz (Run Frequency) in about 1.5 seconds. This matches the torque/inertia characteristics of the drive motor allowing it to ramp up to speed synchronously with the oscillator output. At this time the drain-to-source resistance of Q23 (zone H4) is approximately 100 ohms thereby by passing R96 and R97. The frequency of the oscillator in this condition is the run frequency of 432 Hz (nominal) and is determined by R98, R99, R100 and C35. Potentiometer R98 is provided to adjust the run frequency.

Phase Counter U16 (zone G2) is clocked on the high-to-low transition of each clock pulse from U20 pin 12. Outputs CNT10, CNT01 are anded by U5 (zone D5) pin 1 to provide the ϕA drive signal to U25 pin 6. CNT10 is used for the ϕB drive signal through U19 pin 6 and CNT01 is used for the ϕC drive signal through U19 pin 1. The pre-drive gates are enabled by U20 pin 2 if the value of current sensed through the current-limit circuit is within the operating range. The drive to ϕA is controlled by the output of U25 pin 5, R106, R107 and Q25; The drive to ϕB is controlled by the output of U19 pin 5, R112, R113 and Q26; and the drive to ϕC is controlled by the output of U19 pin 3, R115, R116 and Q27.

U26 (zone B6) is used as the current-sense amplifier and compares the voltage across R118 (the composite motor current) to a level determined by R108 and R109. When the composite current through R118 (zone A3) exceeds approximately 2.7A, gates U25 pin 7, U19 pin 7 and U19 pin 2 disable the respective phase drivers. During motor startup, the current-sense amplifier (U26) tends to limit the start current by *chopping* the drive signal. As the motor starts, it requires high starting currents; this is sensed causing the driver to turn off. As the current is reduced, the driver is enabled. This switching action continues until the composite motor current is below the sense level.

3.5 PHYSICAL DESCRIPTION, PCBA NO. 600251, FD5X0 DISK DRIVES

The PCBA is approximately 10 inches (25.40 cm) long by 7.50 inches (19.04 cm) wide. Figure 3-3 illustrates the placement of test points and connectors.

There are four connectors on the PCBA. J1 at the rear of the PCBA is the interface connector and is slotted to mate with a key in the mating plug. J2 is a 30-pin edge connector into which the subassembly connectors plug; J3 is the connector into which the Read/Write head plugs, and J4 is the connector into which the Door-Open-Request Switch and Door-Open Solenoid plug.

In addition, P5 is routed through P2 to connect to the Busy Indicator mounted in the Door-Open Switch; J6 (not visible in Figure 3-3) is mounted in the capacitor housing and allows for ac power connections.

3.6 INTERFACE DESCRIPTION, PCBA NO. 600251

Table 3-2 lists the input/output and power pin assignments for interfacing the FD5X0 series disk drive. These signals are described in detail in the following paragraphs. Table 3-3 lists the ac power pin assignments for J6/P6.

3.6.1 GENERAL

All interface signals are TTL compatible. The logic true (low) state is represented by +0.4v (maximum); the logic false (high) state is represented by +2.4v (minimum).

Cable used to interface with the disk drive must be 100-ohm twisted pair (or equivalent) with a maximum length of 30 feet.

Figure 3-4 shows the configuration for which the drivers and receivers have been designed.

3.6.2 INTERFACE INPUT

3.6.2.1 Step In/Step Out (2 lines) (ISTI,ISTO)

The Step In/Step Out (ISTI, ISTO) interface signals are used to move the read/write head by one track position. The trailing edge of this pulse initiates the access motion.

A true (low) pulse with a time duration greater than 200 nsec but less than 2 msec on the ISTO line causes the read/write head to move one track position toward the center of the disk.

A true (low) pulse with a time duration greater than 200 nsec but less than 2 msec on the ISTO line causes the read/write head to move one track position away from the center of the disk.

The repetition rate of the ISTI and ISTO pulses must be such that the time interval between two consecutive pulses is between 10 and 11 msec. If this condition is not satisfied, two consecutive ISTI or ISTO pulses must be separated by greater than 30 msec.

When attempting a multi-track seek operation, optimum access time is realized by issuing ISTI or ISTO pulses at intervals between 10 and 11 msec.

Two consecutive pulses on these lines, involving a change in the direction of motion, must be separated by a time interval not less than 30 msec.

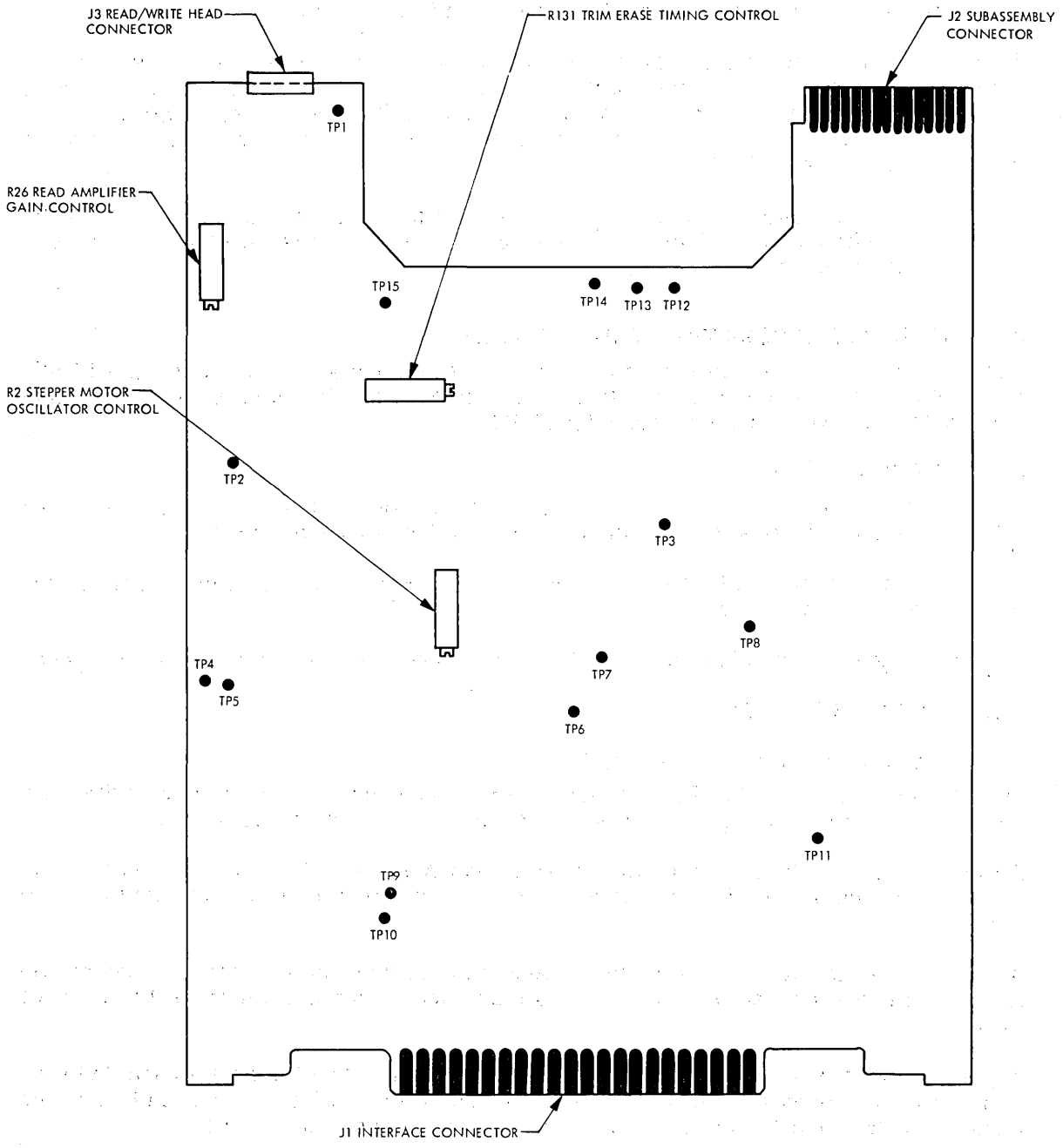


Figure 3-3. Placement of Test Points and Connectors for PCBA No. 600251

Table 3-2
Standard Interface Pin Assignment

	Signal	Line	Ground
Input Control	STEP IN (ISTI)	11	M
	STEP OUT (ISTO)	15	S
	Not Applicable	18	V
	HEAD LOAD (IHLD)	16	T
	HEAD CURRENT SWITCH (IHCS)	7	H
	WRITE ENABLE (IWEN)	9	K
	TRIM ERASE EXTERNAL (Option) (IEEN)	8	J
	DOOR LOCK ENABLE (IINLK)	2	4
Output Status	TRACK 0 (ITRK0)	19	W
	INDEX (IINXP)	17	U
	DOOR OPEN (IDOP)	6	F
	WRITE PROTECT (IWPT)	13	P
	WRITE BUSY (IWBSY)	1	3
Data	WRITE DATA INPUT (IWDA)	10	L
	READ DATA OUTPUT (IRDA)	20	X
Power	+24V DC	A,B	C,D,E
	+5V DC	21	Y
	—5V DC (—15V DC, Option)	22	Z

- Interface Connector Body AMP Inc. No. 583859-3 Contacts 1-583853-1, or equivalent.
- Keying slot located between pins 5 and 6.

Table 3-3
AC Power Pin Assignment

Connector Components - AMP, Inc.	AMP P/N
Pin Housing (used on Drive)	1-480305-0
Male Pins 1, 3	61118-4
Male Pin 2 (Ground)	61527-2
Socket Housing (attached to power cord)	1-480303-0
Female Pins	61117-4

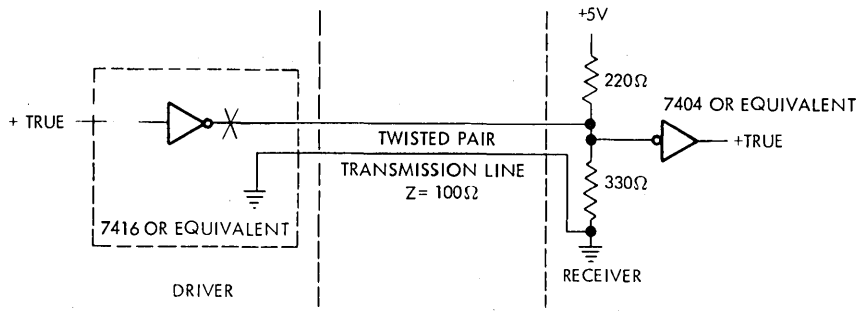


Figure 3-4. Typical Driver/Receiver Configuration

When the read/write head is positioned at Track 0, an ISTO pulse is ignored. Also, head motion is inhibited if either the Write Enable or the Erase Enable signal is true (low).

The Read/Write command must not be attempted within 30 msec of issuing a Step In or Step Out pulse that results in head motion.

3.6.2.2 Head Load (IHLD)

The Head Load (IHLD) signal activates the head load actuator to move the read/write head and pressure pad into contact with the disk. When IHLD is true (low), the read/write head remains in contact with the disk. When IHLD is false (high), the head load actuator is deactivated; this moves the read/write head and pressure pad away from the disk. A read/write command must not be attempted in less than 40 msec after the IHLD line goes true (low).

3.6.2.3 Head Current Switch (IHCS)

The Head Current Switch (IHCS) interface line must be true (low) for a write operation on tracks 43 through 76. A true (low) level selects the lower of two write current values. The level on IHCS must be false (high) for a write operation on tracks 0 through 42. A false (high) level selects the higher of two write current values.

In single/double density models such as the FD510, it is mandatory that during a read operation on tracks 43 through 76, the level on the IHCS line be true (low). It is also mandatory that when performing a read operation on tracks 0 through 42, the level on the IHCS line be false (high).

When performing a read operation with single density models such as the FD500, the preceding operation of the IHCS line is allowable, but is not mandatory.

3.6.2.4 Write Enable (IWEN)

A true (low) level on the Write Enable (IWEN) interface line prepares the write electronics for writing data and causes the read electronics to be disabled. Although data are written under control of the Write Data Input (IWDA) line, it is recommended that changes of state on the IWEN line occur before the first Write Data pulse. However, the separation between the leading edge of IWEN and the first significant Write Data pulse should not be less than 2 μsec, nor greater than 4 μsec. The same restrictions exist on the relationship between the last significant Write Data pulse and the termination of the IWEN signal. When IWEN is false (high), the write electronics are disabled.

When a Model FD5X0 is installed with the Write Protect option, and if the diskette is write protected, the write electronics are disabled irrespective of the state of the Write Enable line.

3.6.2.5 Trim Erase External (Option) (IEEN)

When the Trim Erase External (IEEN) option is incorporated in the disk drive, the IEEN interface signal provides independent control of the trim erasure of data recorded in the track.

When IEEN is true (low), erase current is allowed to flow in the erase head; when IEEN is false (high), the erase current is disabled.

When a Model FD5X0 is installed with the Write Protect option, and if the diskette is protected, the trim erase electronics are disabled irrespective of the state on the IEEN line.

When the Write Enable (IWEN) line goes false (high), the erase current must remain enabled for a minimum of 475 μsec thereafter to ensure that all of the recorded data are trim erased. The 475 μsec minimum time is defined as the minimum erase gap time and results from tolerances arising from the head, track position, and diskette speed.

When the Write Enable (IWEN) line goes true (low), a delay must be incorporated before allowing the IEEN line to go true (low). This is to preclude erasing previously recorded information, which can occur when fixed header formats are utilized. The value of the delay must be calculated with respect to tolerances in the head, track location, diskette speed, and format used.

3.6.2.6 Write Data Input (IWDA)

The Write Data Input (IWDA) interface line provides the bit-serial write-data pulses that control the switching of the write current in the head.

When the write electronics have been conditioned for writing by a true (low) state on the Write Enable (IWEN) interface line, each high-to-low transition on the IWDA line causes a flux change to be produced at the (write) head gap. This flux change at the (write) head gap causes a flux change to be stored on the medium.

The double-frequency-encoding technique is normally used with the FD5X0. In this technique, the data and clock form the combined Write Data Input signal. It is recommended that the repetition rate of the high-to-low transitions when writing all zeros be equal to the nominal data rate ±0.1 percent. The repetition rate of the high-to-low transitions when writing all ones should be equal to twice the nominal data rate ±0.1 percent.

3.6.2.7 Door Lock Enable (IINLK)

A false (high) signal or an open circuit condition on the Door Lock Enable (IINLK) line allows the operator to open the loading door by activating the Door-Open Bar-Switch. The LED indicator in the Door-Open Bar-Switch is extinguished when IINLK is false (high). When IINLK is true (low), the release action of the bar-switch is inhibited and prevents the loading door from being opened. The LED indicator is illuminated.

3.6.3 INTERFACE OUTPUT

3.6.3.1 Index (IINXP)

The Index (IINXP) signal is provided once each revolution (166.67 msec nominal) for a duration of 2.5 ± 1 msec and is used to indicate to the controller the beginning of a track. The IINXP line remains true (low) for the duration of Index pulse.

The leading edge of IINXP must always be used to guarantee diskette interchangeability for the PERTEC FD5X0 Series Flexible Disk Drive.

3.6.3.2 Door Open (IDOP)

The Door Open (IDOP) signal goes true (low) when the loading door of the disk drive is opened. IDOP goes false (high) when the door is closed.

The head-load solenoid is de-energized when the loading door is opened, irrespective of the state on the Head Load (IHLD) interface line.

3.6.3.3 Write Protect (IWPT)

The Write Protect (IWPT) level goes true (low) when the installed diskette is write protected. The write electronics in the FD5X0 series disk drives are internally disabled when the diskette is write protected.

When the IWPT line is false (high), the write electronics are enabled and a write operation can be performed. It is recommended that the controller not issue a Write command when the Write Protect signal is true (low).

3.6.3.4 Read Data Output (IRDA)

The Read Data Output (IRDA) interface line transmits a readback data pulse to the controller for each flux transition recorded on the medium. IRDA goes true (low) for a duration of 200 ± 50 nsec for each flux change recorded on the medium.

During a write operation, Read Data pulses are inhibited for the duration of the true (low) state on the Write Busy line. Read Data pulses are invalid for a period of 100 μsec after the Write Busy line goes false (high). (Refer to Paragraph 3.6.3.6.)

If the Write Enable line is false (high) and the head is unloaded, spurious pulses of random frequency will be present on this interface line.

It is recommended that the Write Data Input line be disabled in addition to the Write Enable line during the read operation.

3.6.3.5 Track 0 (ITRK0)

The Track 0 (ITRK0) interface signal is used to alert the controller that the read/write head is positioned on track 0. The ITRK0 signal remains true (low) until the head is moved away from track 0.

ITRK0 goes true (low) approximately 50 msec after the trailing edge of the Step Out command pulse that positions the read/write head on track 0. Step Out command pulses issued after the 9 msec period from the trailing edge of the Step Out command pulse that positions the read/write head on track 0 are ignored.

3.6.3.6 Write Busy (IWBSY)

The Trim Erase function in the FD5X0 series disk drives is provided internally. Since a write operation starts when the Write Enable line goes true (low) and terminates when the Trim Erase current is turned off, it is necessary to signal the controller when the (internal) Trim Erase function is complete. This information is provided on the Write Busy (IWBSY) interface line, which is true (low) whenever the Write Enable or the (internal) Trim Erase functions are energized. In particular, the line goes true when Write Enable goes true (low), then goes false (high) at the completion of the (internal) Trim Erase function.

When the (external) Trim Erase option is installed, the Write Busy interface line still goes true (low) whenever the Write Enable or the (external) Trim Erase functions are energized.

3.7 CIRCUIT DESCRIPTION, PCBA NO. 600251

3.7.1 HEAD POSITIONER LOGIC

The Head Positioner Logic, including the Track 0 circuits, are shown on Schematic No. 600250, sheet 2. Refer to the functional description given in Paragraph 2.4 in conjunction with this description.

Positioner control is a function of gated oscillator U13 (zone G7), phase state generator U14 (zone E5), and the requested motion direction pulse (ISTI or ISTO) from the interface.

The Step pulses are received and terminated by gates U29 (zone F7) pin 5 (ISTI) and U23 (zone E7) pin 9 (ISTO). The respective outputs of U29 and U23 are used to set Direction Control Latch U23 (zone D5) pins 2 and 6, and to initiate the motion sequence through U23 (zone E6) pins 11, 12, 13 (TP11) and U29 (zone E6) pins 9 and 8.

Initial conditions are established by the Power Sense circuitry (NPSEN) through U22 (zone E6) and U29 (zone 5). NPSEN places both flip-flops of U14 (zone E6, E5) in the reset state. Oscillator U13 is held inactive by U20 (zone F4) pin 6 and will remain inactive until U14 pin 15 or pin 11 is high.

Upon receipt of a Step pulse, U14 pin 15 will go high if Not Write Busy (NWBSY) is high and is not cleared by U22 pin 4. U14 pin 15 sets on the trailing edge of the Step pulse. U14 pin 15 going high enables the oscillator via U22 and U20 (zone F4). Additionally, $\phi 1$ of the stepper motor drive is disabled by U30 (zone F2) pin 2.

The output of Oscillator U13 pin 3 (which can be observed at TP7) goes high for a period of time determined by the time for capacitor C2 to charge to the high internal threshold of U13 pin 6 through R1 + R2 + R3. When the sense threshold of U13 pin 6 is reached, U13 pin 3 goes low for a period of time determined by the time for C2 to discharge to the low threshold through R3. At this time U13 pin 3 goes high again (if U13 pin 4 is still enabled) then the oscillation process repeats itself. Oscillator U13 typically generates two consecutive positive periods of unequal duration for each Step pulse. The unequal durations are a result of the first charging cycle that occurs each time U13 is enabled; C2 initially charges from a voltage level lower than the threshold level achieved during sustained oscillator operation. The output of the oscillator is shaped by U20 pins 3 and 4 then inverted for proper polarity by U15 pins 9 and 8.

The oscillator clocks U14 pin 6 on the high-to-low transition. U14 pin 11 is initially reset but goes high on the trailing edge of the first internal clock pulse initiated by a Step command. This change causes U14 pin 3 to reset through U22 pin 4 and continues to enable Oscillator U13. The output states of U14 are directed via the Direction Multiplexer U28 (zone F4) to the $\phi 2$ or $\phi 3$ pre-driver dependent on the state of Direction Latch U23. If a

Step-In command (ISTI) had been issued, U23 pin 4 would be high, enabling $\phi 3$ pre-driver for the state of U14 pin 15 and $\phi 2$ pre-driver for the state of U14 pin 11. The sequence established allows first $\phi 3$ to be active, then $\phi 2$. The second clock pulse causes U14 pin 10 to go high; this transition triggers single-shot U17 (zone G4) for a period of approximately 40 msec. U17 pin 12 energizes the $\phi 1$ Driver, transistor Q1 (zone G20). Additionally, the reset states of U14 causes the $\phi 1$ hold driver (transistor Q2) to be energized via U22, U20, and U30. If the disk drive incorporates the Power Save feature, the positioner $\phi 1$ will be disabled if the head is unloaded (IHLD false) through U24, U9, W5 and W6.

The output drive circuitry for $\phi 1$ consists of transistors Q1 and Q2. Transistor Q1 is used as the Phase Driver, allowing full current through $\phi 1$. Transistor Q2 is used as a hold or detent driver, operating at a reduced current through a 33-ohm resistor (across pins 10 and 12 on P2) mounted external to the PCBA. Transistors Q3 and Q4 provide the drive for $\phi 2$ and $\phi 3$, respectively.

The Track-0 Latch circuitry relies on a microswitch that is de-bounced by a cross-coupled latch formed by U15 (zone C4) pins 3 and 5. When active, the Track-0 Latch disables interface receiver U23 (zone E7) pin 8 from receiving any additional Step Out commands. The output of the Track-0 Latch is also provided to the interface via U22 and U9 (zone D2). The status is only allowed to propagate through the interface (connector J1-19) after the time-out associated with the $\phi 1$ one-shot, U17. The high-to-low transition of U17 pin 5 clocks U4 (zone D3) pin 11 and enables U22 pin 9.

3.7.2 POWER SENSE CIRCUITRY

The Power Sense circuit, shown on Schematic No. 600250 sheet 2 (zones B7 to D7), consists of the under-voltage monitors of +24v dc, +5v dc and —5v dc.

Initial conditions assume that all supplies are at their zero value and all components are inactive, i.e., capacitors discharged.

Application of dc power can be sequential or simultaneous. In either case, the initialization of the drive electronics is dependent on the last of the three dc voltages that achieves its minimum sense value. The control elements are the charged state of capacitor C6 and the logic threshold of U20 (zone D6) pin 9. Capacitor C6 is not allowed to charge until the three dc sense voltages have been reached. For the +24v dc supply, the sense circuitry consists of transistor Q5, VR1, R16, and R18. The base of Q5 is controlled by the conduction of VR1 through R16 and R18 and will not conduct until the +24v dc has exceeded 17.6v dc. If the other voltages have been established, capacitor C6 is allowed to charge; if not, resistor R20 diverts the charge current to transistor Q7 or Q28.

Transistors Q6, Q7, zener diode VR2 and resistors R21, R23 and R22 sense the +5v dc supply. Transistor Q7 relies on the state of Q6 and the +24v dc supply. Transistor Q6 will not turn on until the +5v dc supply has reached +4.3v dc or greater. At that time zener diode VR2 will conduct and establish a turn-on voltage for Q6 via R21 and R23.

The negative voltage supply is sensed off the common tie of jumpers W1 and W2. If the —5v dc operation is required, W1 is installed and W2 is omitted. If the Negative Voltage option (—12v dc/—15v dc) is required, W1 is omitted and W2 is installed. Resistors R24, R121, and zener diode VR3 form a —5v dc regulator. Resistors R119, R120, zener diode VR5, and transistor Q28 sense the —5v dc supply.

The signals supplied from the power sense circuitry are NPSEN which is used for the positioner logic, and APSEN which is used for the analog write circuitry.

3.7.3 INTERLOCKS AND TRANSDUCERS

The Interlocks and Transducer circuitry are shown on Schematic No. 600250 sheet 3.

The terminating amplifiers for the Index pulse and Write Protect transducers are similar. Operational amplifiers U21 and U27 (zones F, G-6) compare the conduction of their respective photo-transistors with a reference level set by R27, R29, R31, and R33. Diodes CR4 and CR5 clamp the outputs from any negative excursions.

The Index signal (IINXP) consists of a pulse for each rotation of the index hole in the diskette. It is important that the transition edges of each pulse be sharp. Schmitt trigger gate U20 (zone G6) provides controlled hysteresis to ensure these sharp transitions (which can be observed at TP10). U6 is the driver for IINXP pin 17 of connector J1.

In the Write Protect circuitry, it is important only to detect the presence of a Write Protected diskette hole. Therefore, it is sufficient to route the output of the sense amplifier through a conventional gate (U9, zone F6) for level changes, then to the interface as IWPT on pin 13 of connector J1.

The solenoid-operated door on the FD5X0 family of disk drives is inhibited from opening when interface line IINLK is low. When this line is low, U25 (zone E7) pin 3 goes low and enables the LED indicator located on the Door-Open Bar-Switch assembly. Additionally, U6 (zone C7) pin 12 disables the door-open solenoid driver composed of resistors R36, R37, and transistor Q8. When IINLK is high, the LED indicator is extinguished and the solenoid driver is conditioned to respond to the Door Open Request switch unless the door is already open as indicated through U24 pin 2 (zone C7).

The Door-Open Indication switch is conditioned by a cross-coupled latch formed by U15 (zone G3) pins 1 and 13. This signal provides status to the interface through U6 (zone G2) pin 1 and disables the Head Load gate U8 (zone F3) pin 5. The Head Load signal (IHLD) on pin 16 of connector J1 activates the Head Load Solenoid driver consisting of U24 (zone F3) pin 6, resistors R38, R39, and transistor Q9.

Schematic No. 600250 sheet 3 also provides the ac distribution circuitry for two configurations of the ac Drive Motor (zone B5). This wiring is accomplished via fast-on terminals located within the capacitor box structure and is not a part of the PCBA.

3.7.4 WRITE/ERASE LOGIC

The Write/Erase Logic circuitry is shown on Schematic No. 600250 sheet 4.

3.7.4.1 Write Waveform Generator

At the beginning of a write operation, the Write Enable Interface signal (IWEN) on connector J1-9 goes low. If the disk drive has the Write Protect option and the diskette is not write protected, the output of U8 (zone E7) pin 1 goes high; this can be observed at TP14. The high output of U8 pin 1 removes the clear signal to pin 3 of the Write Data flip-flop U4. The Write Data flip-flop is now in a reset state, conditioned to respond to write data information. The Write Enable Interface signal enables gate U5 (zone E6) pin 5 and 6 and gate U8 (zone D4) pin 12. This action enables the write current source (U7 pins 1 and 2) and provides a Write Busy status signal to the interface.

The composite write clock and data signals (double frequency encoding) are received through connector J1-10 (Write Data Input). These signals are inverted twice by U29 pin 11 and U15 pin 11, then presented to the clock input of the Write Data flip-flop U4 pin 1. The Write Data flip-flop is toggled on the high-to-low transition of each pulse, changing the direction of the current flowing in the magnetic head.

The outputs of Write Data flip-flop U4 pins 15 and 14 are processed by the level-changing circuit comprised of U6 pins 3 and 5, and resistors R55, R56, R57, and R58. The outputs of the level changing circuits, node of R55 and R56 and node of R57 and R58, are fed to Write Drive Switch transistors Q17 and Q18 (zones E, F-5). The emitters of these transistors are tied together to the collector of Q14 (zone G5) the write current source. The collectors of Q17 and Q18 are routed to the center-tapped magnetic head through diodes CR10 and CR11, which results in the required write current waveform. Resistor R61 dampens the Read/Write head and its value is chosen for an optimum current waveform.

The basic current source consists of voltage reference components VR4, CR8, R53 and R54 (zone G6). These components establish a voltage differential across R47 and the base-emitter junction of Q14. Thus, transistor Q14 and R47 forms the basic current source of approximately 4 ma. An additional current source is formed by U7 pin 5, R49, R50, R129, and Q16. This source is energized via U11 (zone D6) pin 6 whenever the Head Current Switch (IHCS) interface signal on connector J1-7 is high. This causes an additional 1 ma (totaling 5 ma) to flow into switch transistors Q17 and Q18.

During system power-up, or loss of one of the dc voltages, the write current source is disabled by circuitry consisting of R125, R126, R127, Q29, and Q30 (zone H6). When control signal APSEN goes low, transistor Q29 turns off thereby turning Q30 (zone H5) off. This action prevents erroneous information from being recorded during system power-up or loss of one of the dc voltages.

Diodes CR10, CR11 and resistors R59 and R60 are not functionally required for the write circuitry but provide isolation of the sensitive read circuits from the write circuitry. During a read operation, the head windings are approximately at ground potential; diodes CR10 and CR11 are cut off by the —5v dc return through R59 and R60.

3.7.4.2 Erase Current Driver

The Erase Current Driver circuitry consists of U9 (zone B4) pin 4, C47, R64, R65, R66, R67, R68, R132 and Q19 (zone B2). These components control and form an erase current source of approximately 85 ma. The circuit is disabled by signal APSEN via R133, Q31 and enabled by either the Internal Trim components, or (as an option) the External Erase interface (IEEN) line on connector J1-8. Jumpers W3 and W4 are exclusive and configure the circuit to respond to the Internal or External Erase commands.

The Internal Trim Erase timing is controlled by a dual single-shot U10, C15, C16, R62, R63, and R131. Upon receipt of Write Enable going high, U10 pin 12 is active and provides a pulse approximately 200 μsec in duration. This pulse provides a *pre-delay* to turn on of the erase driver via U11 pin 8 and U11 pins 12 and 11. At the completion of the write operation, Write Enable (IWEN) goes high and causes the second half of U10 (zone B4) pin 4 to go active. The pulse from the second single-shot provides a *post-delay* to turn off of the erase driver for approximately 475 μsec via U11 pins 13 and 11. The value of this delay can be adjusted by R131 and optimized to tolerances arising from head, track position, and diskette speed.

The Write Enable and Trim Erase signals are Ored through U8 pin 13 and provides a Write Busy status through U29 pins 1 and 2 and U30 pins 9 and 8 to the interface on pin 1 of connector J1. The Write Busy signals of appropriate polarity are routed to the positioner logic and the read logic.

3.7.5 READ AMPLIFIER

The Read Amplifier and associated digital circuitry is shown on Schematic No. 600250, sheet 5.

3.7.5.1 Read Switch

The Read Switch circuitry consists of components CR12, CR13, CR14, CR15, CR16, CR17, CR18, CR19, R69, R70, R71, R72, R73, R74, R75, Q20 (zone G7) and non-inverting gate U6 (zone G6) pins 9 and 8. The Read Switch isolates the Read Amplifier from the considerable voltage excursions across the magnetic head that occur during a write operation. During a write operation, the Write Enable interface line is low. This signal is inverted by U5 pins 5 and 6 (Write Logic, sheet 4, zone E6), the output of U5 pin 4 (NWRT) is low causing the output of U6 pin 8 to go low. U6 pin 8 turns on Read Switch transistor Q20 (zone G7) via R69 and R70. The collector of Q20 is now at approimately +24v dc so that the anodes of CR12 and CR13 are *pulled* positive. The junctions of CR12 and R74, CR13 and R75 are pulled positive thereby cutting off CR14, CR15, CR17, and CR18. Diodes CR16, CR19 and resistors R72, R73 clamp the inputs of U1 (zone D6) so that U1 never goes higher than a diode voltage drop.

During a read operation, NWRT is high, therefore, Q20 is cut off and CR12, CR13 are back biased. The anodes of CR14 and CR17 are at approximately zero volts because they are connected through the low impedance head windings to ground. Approximately 0.20 ma of current is available through resistors R72 and R73. Additionally, 0.40 ma is demanded by R74 and R75 so that each of the four diodes (CR14, CR15, CR17, CR18) have approximately 0.20 ma of current flowing.

In this condition, the diode bridge provides a low impedance path for the head signal to preamplifier U1. Capacitor C18 decouples any Read Switch noise to ground.

3.7.5.2 Preamplifier

The Preamplifier is a balanced-in/balanced-out high-pass circuit whose gain is controlled by R76, R77. Capacitor C19 is the reactive component that establishes the high pass characteristic of the amplifier. Potentiometer R76 is provided to allow gain adjustment compensating for different read head sensitivities thus reducing the dynamic range requirements of the system.

A gain of approximately 20 is used to avoid problems encountered by amplification of the small dc offset introduced by Read Switch. The signal level, measured differentially between pins 7 and 8 of U1, is approximately 250 mv for an all-ones pattern at track 0.

3.7.5.3 Filter

The balanced output from U1 is fed via the linear phase filter L1, L2, L3, L4, C30 to a terminating network consisting of C21, C23, R78, and R80. This filter has a linear phase response over the frequency of operation and attenuates the high frequency noise from the signal.

3.7.5.4 Differentiator

The output of the filter is fed to the differentiator circuit U2 (zone D4). Capacitors C21 and C23 are used to couple the filter to amplifier U2 and to isolate any dc offset voltage at the output of U1. Amplifier U2 is similar in operation to preamplifier U1 with the exception that the gain network is fixed and provides a 6 db-per-octave gain rise characteristic over the frequency range of operation, thus providing the required differentiator characteristics. The gain components are R79 and C24.

3.7.5.5 Bandwidth Control (Single/Double Density Units)

Two bandwidth values are required to accommodate the range of head resolution for double density operation.

The Bandwidth Control circuitry consists of U24 pin 4, R134, R135, R136, R137, and FET Q32 (zone F5). The Head Current Switch (IHCS) interface signal must be used during a read operation. When IHCS is low, U11 pin 6 goes high (sheet 4 zone D6); this forces U24 pin 4 to go low causing Q32 to turn on. With FET Q32 on, resistor R137 is placed in parallel with R79, thereby increasing the bandwidth of amplifier U2 so it can read the denser inner tracks (Tracks 43—76). When IHCS is high, the bandwidth switch is off, hence, reducing the bandwidth and improving the differentiator response.

3.7.5.6 Zero-Crossing Detector

The output of U2 is fed to emitter followers Q21 and Q22 to prevent the output from being improperly loaded. The emitters outputs (which can be observed at TP4 and TP5) are ac coupled to inputs of the Zero-Crossing Detector, U3.

U3 (zone D3) is a bi-directional one-shot that accepts the differential Read signal. The output of U3 pin 11 (which can be observed at TP9) is a single 200 ±50 nsec pulse from each and every zero-crossover. The pulse width is determined by capacitor C26 and resistor R86. Ac hysteresis is provided by C29 and R91 to eliminate the possibility of multiple detection of zero crossover.

U3 pin 3 is disabled by the Write Busy (WBSY) signal. The output of U3 pin 11 is fed to interface driver U9 pin 5, then to connector J1-20, Read Data (IRDA).

3.8 PHYSICAL DESCRIPTION, PCBA NO. 600266, FD5X1 DISK DRIVES

The PCBA is approximately 10.85 inches (27.56 cm) long by 7.85 inches (19.94 cm) wide. Figure 3-5 illustrates the placement of test points and connectors.

There are six connectors on the PCBA; J1 is the interface connector, a 50-pin flat ribbon type 3M connector; J2 is a 30-pin edge connector into which the subassemblies plug; J3 is the connector into which the read/write head plugs; and J4 is the connector into which the Door Open Request Switch and Door Open Solenoid are connected. In addition, P5 is routed through P2 to connect to the Busy Indicator mounted in the Door-Open Bar Switch; J6 (not visible in Figure 3-5) is mounted to the capacitor housing and provides for ac power connections. J7 is mounted on the PCBA adjacent to J1 and allows for dc power connections.

3.9 INTERFACE DESCRIPTION, PCBA NO. 600266

Table 3-4 lists the input/output and power pin assignments for interfacing the FD5X1 series disk drive. These signals are described in detail in the following paragraphs.

Table 3-5 lists the ac power pin assignments for J6/P6. Table 3-6 lists the dc power pin assignments for J7/P7.

3.9.1 GENERAL

All interface signals are TTL compatible. The logic true (low) state is represented by +0.4v (maximum); the logic false (high) state is represented by +2.4v (minimum).

Cable used to interface with the disk drive must be 3M 100-ohm flat ribbon (or equivalent) with a maximum length of 30 feet.

Figure 3-6 shows the configuration for which the drivers and receivers have been designed.

3.9.2 INTERFACE INPUT

3.9.2.1 Select Lines (4 Lines) (ISLT0 — ISLT3)

The Select lines provide a means of selecting and de-selecting a disk drive. These four lines select one of the four disk drives attached to the controller. When the Select line logic level is true (low), the disk drive electronics are activated to execute any Step or Read/Write commands that are issued. When the Select line logic level is false (high), all input/output interface lines (with exception of the four Head Load Enable lines and four Ready lines) are de-selected. When the FD5X1 series disk drive includes the Power Save feature, these lines provide a means of exercising this feature.

A Select line must go true (low) at least 100 nsec before any command is issued to the disk drive. A Select line may go false (high) in no less than 100 nsec after the trailing edge of the Step command pulse. A Select line must remain stable in the true (low) state until the any Read/Write command is completed.

The disk drive address is determined by a jumper option on the PCBA. Select lines 0 through 3 provide a means of daisy-chaining a maximum of four disk drives to a single controller. Only one line can be true at a time.

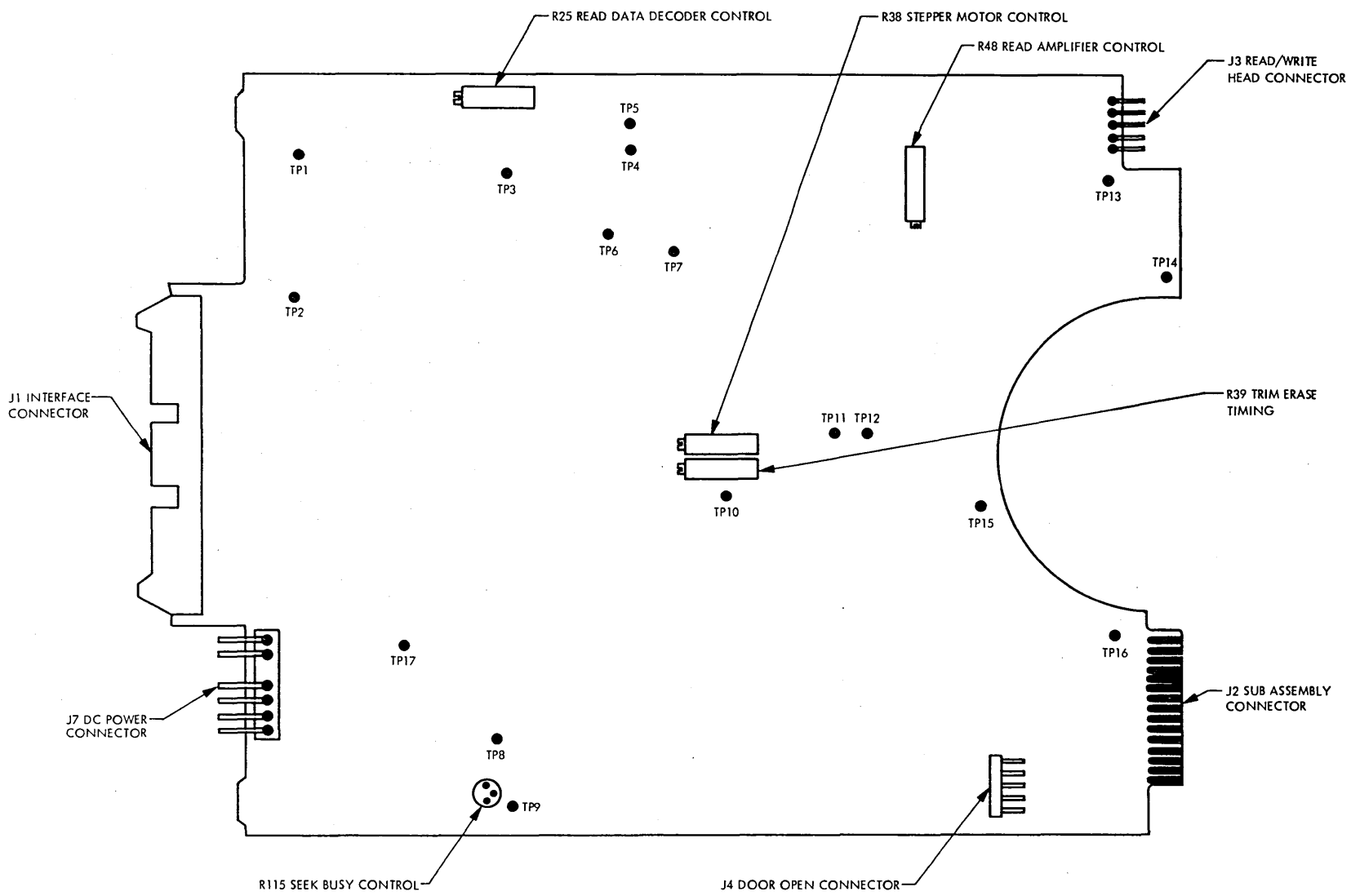


Figure 3-5. Placement of Test Points and Connectors for PCBA No. 600266

Table 3-4
Standard Interface Pin Assignment

Controller to Disk Drive		
Signal	Ground	Description
1	4	SELECT 0 (ISLT0)
2	4	SELECT 1 (ISLT1)
3	4	SELECT 2 (ISLT2)
5	4	SELECT 3 (ISLT3)
6	10	HEAD LOAD ENABLE 0 (IHLD0)
7	10	HEAD LOAD ENABLE 1 (IHLD1)
8	10	HEAD LOAD ENABLE 2 (IHLD2)
9	10	HEAD LOAD ENABLE 3 (IHLD3)
11	12	WRITE ENABLE (IWEN)
13	14	ERASE ENABLE (IEEN)
15	16	HEAD CURRENT SWITCH (IHCS)
17	18	WRITE DATA (IWDA)
19	20	DIRECTION/STEP IN (IDIR/STI)
21	22	STEP/STEP OUT (IST/STO)
23	24	HEAD LOAD (IHLD)
35	34	DOOR LOCK ENABLE (IDLEN)
Disk Drive to Controller		
Signal	Ground	Description
29	30	READ DATA (IRDA)
31	34	SELECTED AND READY (ISRDY)
32	34	TRACK 0 (ITRK0)
33	34	WRITE PROTECT (IWPT)
36	40	READY 0 (IRDY0)
37	40	READY 1 (IRDY1)
38	40	READY 2 (IRDY2)
39	40	READY 3 (IRDY3)
45	46	INDEX (IINXP)
47	46	SECTOR (ISECP)
25	26	READ DATA (SEPARATED) (IRDA/S)
27	28	READ CLOCK (SEPARATED) (IRCLK/S)
41	40	SEEK BUSY (ISBSY)
50	46	WRITE BUSY (IWBSY)

Table 3-5

AC Power Pin Assignment, J6/P6
(Connector Components are AMP, Inc.)

Description	AMP Part No.
Pin Housing (Used on Drive)	1-480305-0
Pins 1 and 3	61118-4
Pin 2 (Ground)	61527-2
Socket Housing (Attached to Power Cord)	1-480303-0
Sockets	61117-4

Table 3-6

Power Connector Pin Assignment, J7/P7

Pin No.	Supply Voltage
1	—5V DC (—12V/—15V)
2	Return (—5V, —12V/—15V)
3	+ 5V DC
4	Return (+ 5V)
5	Key
6	Return (+ 24V)
7	+ 24V DC

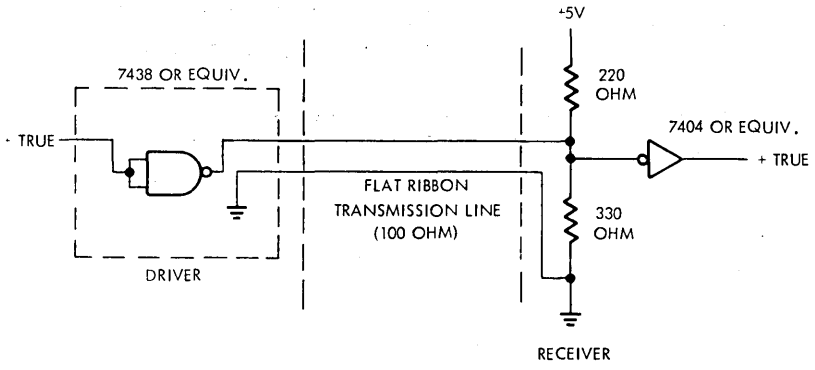


Figure 3-6. Typical Driver/Receiver Interface Configuration

An undefined operation may result if two of more units are assigned the same address on the daisy-chain, or if two or more Select lines are true (low) simultaneously.

3.9.2.2 Head Load Enable Lines (4 Lines) (IHLD0—IHLD3)

The Head Load Enable lines (IHLD0—IHLD3) are not gated by Select lines; this allows independent control of head load in each disk drive. When a FD5X1 series disk drive includes the Power Save feature, these lines provide a means of exercising this feature.

The Head Load Enable line, when true, activates the head load actuator to move the read/write head and pressure pad into contact with the disk in the drive with the corresponding unit address. When the signal is false (high), the head load actuator is deactivated to move the read/write head and pressure pad away from the disk.

A Read/Write command must not be attempted within 40 msec after a Head Load Enable signal goes true (low).

3.9.2.3 Write Enable (IWEN)

When IWEN is true (low), the write electronics are prepared for writing data (the read electronics are disabled). This signal turns on write current in the read/write head. Data are written under the control of the Write Data (IWDA) input line. It is generally recommended that changes of state on the Write Enable line occur before the first write data pulse. However, the separation between the leading edge of IWEN and the first significant IWDA pulse should not be less than 2 μsec and not greater than 4 μsec. The same restrictions exist on the relationship between the last significant IWDA pulse and the termination of the IWEN signal. When the IWEN line is false (high), all write electronics are disabled.

If a FD5X1 series disk drive with the Write Protect option is installed, and if the diskette is write protected, the write electronics are disabled irrespective of the state of the IWEN line.

3.9.2.4 Erase Enable External (Option) (IEEN)

When the External Trim Erase option is incorporated in the drive, the IEEN interface signal provides independent control of the trim erasure of data recorded in the track.

When IEEN is true (low), the erase current is allowed to flow in the erase head. When IEEN is false (high), the erase current is disabled.

If a FD5X1 series disk drive with the Write Protect option is installed, and if the diskette is write protected, the trim erase electronics are disabled irrespective of the state on the IEEN line.

When the IEEN signal is placed in the false (high) state, the erase current must remain enabled for a period of time thereafter to ensure that all recorded data is trim erased. The gap between the read/write head and the erase head is 0.036 ±0.002 inch. The minimum time is defined as the minimum erase gap time and results from tolerances arising from the head, track position, and diskette speed. The value is 475 μsec, nominal.

When the Write Enable (IWEN) line goes true (low), a delay must be incorporated before IEEN is allowed to go true. This is to avoid erasure of previously recorded information. This can occur when ...ved header formats are used.

The value of this delay must be calculated with respect to tolerances in the head, track location, and diskette speed, and with respect to the format used.

3.9.2.5 Head Current Switch (IHCS)

When the Head Current Switch (IHCS) interface signal is true (low), and the disk drive is selected, the lower value of the write current is selected for a write operation on tracks 43 through 76. When IHCS is false (high) and the disk drive is selected, the higher value of the write current is selected for a write operation on tracks 0 through 42.

When the drive is configured for single density as well as for double density operation, IHCS is used for switching the read channel bandwidth during a read operation in the two track zones. This optimizes the read channel bandwidth with respect to the differentiator droop (shouldering effect) and data decoder margins for a read operation. IHCS must remain active during a read operation.

3.9.2.6 Write Data Input (IWDA)

The Write Data Input (IWDA) interface line provides the bit-serial write data pulses that control the switching of the write current in the head. The write electronics must be conditioned for writing.

A flux change is produced at the write head gap for each high-to-low transition on the IWDA line. This causes a flux change to be stored on the medium.

The double frequency type encoding technique is normally used in which data and clock form the combined Write Data signal. It is generally recommended that the repetition rate of the high-to-low transition when writing all zeros be equal to the nominal data rate of ±0.1 percent. The repetition rate of the high-to-low transitions when writing all ones should be equal to twice the nominal ±0.1 percent data rate.

It is recommended that during a read operation, the Write Data Input line be disabled in addition to the Write Enable line.

3.9.2.7 Step In/Step Out (2 Lines) (IDIR/STI) (IST/STO)

The Step In/Step Out (ISTI, ISTO) interface lines are used to move the read/write head by one track position. The trailing edge of this pulse initiates the access motion.

A true (low) pulse, with a time duration greater than 200 nsec but less than 2 msec, on the Step In line moves the read/write head by one track position toward the center of the disk.

A true (low) pulse, with a time duration greater than 200 nsec but less than 2 msec, on the Step Out line moves the read/write head by one track position away from the center of the disk.

The repetition rate for the Step In or Step Out pulses must be such that the time interval between two consecutive pulses is between 10 and 11 msec. If this condition is not satisfied, then two consecutive ISTI or ISTO pulses must be separated by a time interval greater than 30 msec.

When attempting a multi-track seek operation, optimum access time is realized by issuing ISTI or ISTO pulses at the interval which is between 10 and 11 msec.

Two single-track seek operations must not occur within 30 msec of each other. The two consecutive pulses on these lines involving a change in the direction of motion must be separated by a time interval not less than 30 msec.

When the read/write head is positioned on track 0, a Step Out pulse requiring motion away from the center of the disk is ignored. The head motion is inhibited if either the Write Enable or Erase Enable signal is true (low). A Read/Write command must not be attempted within 30 msec after issuing a Step In or Step Out pulse which results in head motion.

The access motion is initiated on the trailing edge of a Step In or Step Out pulse. For other restrictions, refer to Paragraph 3.9.3.10 when motion commands are used in conjunction with the Seek Busy interface line.

3.9.2.8 Direction/Step (Option) (2 Lines) (IDIR/STI) (IST/STO)

When the Direction/Step option is incorporated, the Step line is used in conjunction with the Direction line to position the read/write head on a given track.

A true (low) pulse, with a time duration greater than 200 nsec but less than 2 msec, on the Step line initiates the access motion. The direction of motion is determined by the state on the Direction line when the Step pulse is issued. If the Direction line is true (low) when a Step pulse is issued, the motion is towards the center of the disk; if the Direction line is false (high), motion is away from the center of the disk. To ensure proper positioning, the Direction line should be stable a minimum of 0.1 μsec prior to issuing a corresponding Step pulse, and remain stable during the time of the Step pulse. All other constraints for control of head motion, as described for the Step In/Step Out lines, still apply to the Direction/Step lines.

The access motion is initiated on the trailing edge of a Step pulse. For other restrictions, refer to Paragraph 3.9.3.10 when motion commands are used in conjunction with the Seek Busy interface line.

3.9.2.9 Head Load (IHLD)

When the disk drive is selected, IHLD activates the head load actuator to move the read/write head and pressure pad into contact with the disk. When IHLD is true (low), the read/write head remains in contact with the disk. When IHLD is false (high), the head load actuator is deactivated to move the read/write head and pressure pad away from the disk.

A Read/Write command must not be attempted within 40 msec after IHLD goes true (low).

3.9.2.10 Door Lock Enable (IDLEN)

The IDLEN interface line, when false (high) or open circuit, activates the Door-Open Bar Switch which allows the operator to open the loading door. The indicator in the Door-Open Bar Switch is extinguished. When IDLEN is true (low), the Door-Open Bar Switch action is inhibited and the operator cannot open the door; the indicator is then illuminated.

The IDLEN interface line may be used to indicate a Busy status of the drive under conditions determined by the user.

3.9.3 INTERFACE OUTPUT

3.9.3.1 Unseparated Read Data Output (IRDA)

The unseparated Read Data Output line (IRDA) transmits readback data to the controller. It provides a pulse for each flux transition recorded on the medium. IRDA goes true (low) for 200 ±50 nsec for each flux change recorded on the medium.

During a write operation, read data pulses are inhibited for the duration of the Write Busy signal (see Paragraph 3.9.3.11).

Read data pulses are invalid for 100 μsec after the termination of the Write Busy signal (see Paragraph 3.9.3.11).

If the Write Enable line is false (high) and the head unloaded, spurious pulses of random frequency will be present on the Write Enable interface line.

Since a data separation circuit is not normally provided in the FD5X1 series disk drives, there is no restriction on the type of encoding technique as long as certain read amplifier bandwidth limitations are not exceeded.

When data separation circuitry is provided, IRDA still provides the composite read data information in addition to Separated Read Data (see Paragraph 3.9.3.8) and Separated Read Clock (see Paragraph 3.9.3.9).

It is recommended that during the read operation, the Write Data input line be disabled in addition to the Write Enable line.

When the disk drive is configured for single as well as double density operation, the Head Current Switch (IHCS) interface signal must remain active during a read operation (see Paragraph 3.9.2.5).

3.9.3.2 Selected and Ready (ISRDY)

When the disk drive is selected, a true (low) signal on ISRDY indicates to the controller that the diskette is inserted, the loading door is closed, and the drive motor is stabliized at the nominal speed of 360 rpm.

When the ISRDY signal is false (high), any read/write operation is disabled in the disk drive. A Read/Write command issued when the ISRDY signal is false (high) is ignored.

3.9.3.3 Track 0 (ITRK0)

When the disk drive is selected, the Track 0 interface signal indicates to the controller that the read/write head is positioned on track 0. The Track 0 signal remains true (low) until the head is moved away from track 0.

The Track 0 signal goes true (low) within 40 $\pm$10 msec after the trailing edge of the Step Out command pulse that positions the read/write head on track 0. Step Out command pulses issued after the 9 msec period from the trailing edge of the Step Out command pulse that positions the read/write head on track 0 are ignored.

3.9.3.4 Write Protect (IWPT)

When the disk drive is selected, the Write Protect (IWPT) line goes true (low) when the diskette is write protected. The write electronics in the FD5X1 series disk drives are internally disabled when the diskette is write protected.

When IWPT is false (high), the write electronics are enabled and the write operation can be performed. It is generally recommended that the controller not issue a Write command when the Write Protect signal is true (low).

3.9.3.5 Ready (4 Lines) (IRDY0-IRDY3)

The Ready interface lines (IRDY0—IRDY3) indicate to the controller the Ready status of each individual disk drive on the daisy-chain. These lines are not gated by Select lines.

When a Ready line is true (low), it indicates to the controller that the diskette is inserted, the door is closed, and the drive motor has stabilized at the nominal speed of 360 rpm. The IRDY0—IRDY3 interface lines report the Ready status for the disk drives on the daisy-chain with addresses 0 through 3, respectively.

3.9.3.6 Index (IINXP)

The Index signal is provided once each revolution (166.67 msec, nominal) to indicate to the controller the beginning of a track. The Index line remains in the true (low) state for the duration of the index pulse. The duration of an Index pulse is 0.4 ±0.1 msec.

The leading edge of an Index pulse must always be used to guarantee diskette interchangeability for the PERTEC FD5X1 series disk drives.

3.9.3.7 Sector (ISECP) (Option)

The Sector signal is provided (for each sector) to indicate to the controller the beginning of a sector when using a hand-sectored diskette. The Sector signal goes true (low) for the duration of a sector pulse. The duration of a sector pulse is 0.4 ±0.1 msec. A Sector pulse is provided 32 times each revolution at the time interval of 5.2 msec, nominal, for a diskette with 32 sectors and one index hole. The leading edge of a sector pulse must always be used to guarantee diskette interchangeability for the FD5X1 series disk drives. As an option, the Sector signal may be divided by 2 or 4 on the PCBA to divide the recording surface into 16 or 8 sectors, respectively.

3.9.3.8 Separated Read Data (Option) (IRDA/S)

The Separated Read Data line (IRDA/S) provides the signal which defines the content of the data read during a read operation. IRDA/S will be a pulse for each *logic-one* bit read from the disk. The line will be true (low) during the time of the pulse, and false (low) for each *logic-zero*.

The timing of the IRDA/S pulses is relative to the Read Clock line. The relative timing is such that a *logic-one* should be interpreted if the Read Data line is true (low) at any time when the Read Clock line is false (high) between consecutive pulses on the Read Clock line. Read Data pulses are invalid for a period of 100 μsec after the termination of the Write Enable or Erase Enable signal, whichever is last.

During a write operation, Read Data pulses are inhibited for the duration of the Write Busy signal (see Paragraph 3.9.3.11).

If the Write Enable line is false (high) and the head unloaded, pulses of random frequency will be present on this interface line. The IRDA/S line is not relevant when using other than double frequency encoding techniques.

3.9.3.9 Separated Read Clock (Option) (IRCLK/S)

The Separated Read Clock (IRCLK/S) line provides the signal which defines the bit-cell time of the information read during a read operation.

The leading edge of the IRCLK/S pulse defines the beginning of a new (next) bit-cell. The line is at the true (low) logic level during the time of the pulse.

During a portion of each bit-cell time, the Read Clock line goes false (high) and remains high until the next bit-cell time is to be defined by a pulse leading edge. This line is used to establish a timing reference for interpreting pulses on the Read Data line. Read Clock pulses are invalid for 100 μsec after termination of the Write Enable or Erase Enable signal, whichever is last.

During a write operation, Read Clock pulses are inhibited for the duration of the Write Busy signal (see Paragraph 3.9.3.11).

If the Write Enable line is false (high) and the head unloaded, pulses of random frequency will be present on this interface line. The IRCLK/S line is not relevant when using other than double frequency encoding techniques.

3.9.3.10 Seek Busy (ISBSY)

When the disk drive is selected, the Seek Busy (ISBSY) signal indicates to the controller that the disk drive is seeking a track. ISBSY goes true (low) within 500 nsec after the leading edge of a Step pulse and remains true (low) for a period of 10 msec after the trailing edge of the Step pulse. After this 10 msec period, the Seek Busy signal goes false (high) for approximately 1 msec. During this time, a next Step pulse true-to-false transition must occur if a multi-track seek operation is desired. This requirement restricts the width of the Step pulse to a nominal value less than 1 msec. If during this 1 msec period a Step pulse is not received, ISBSY goes true (low) for an additional 20 msec, during which time a Step pulse must not be issued. The next seek operation must wait until after the 20 msec period.

A Step pulse must never be issued when the Seek Busy (ISBSY) signal is true (low). ISBSY is provided as a status signal to the user and does not provide a logical lockout for Step commands not issued in accordance with previously defined constraints. (See Paragraph 3.9.2.7.)

3.9.3.11 Write Busy (IWBSY)

The Trim Erase function is provided internally in the FD5X1 series of disk drives. Since a write operation starts when the Write Enable line goes true (low) and terminates when the Trim Erase current is turned off, it is necessary to signal the controller when the internal Trim Erase function is complete.

This information is provided on the Write Busy interface line, which is true (low) whenever the Write Enable or the (internal) Trim Erase functions are energized. In particular, the line goes true (low) when Write Enable goes true (low) and then goes false (high) at the completion of the (internal) Trim Erase function.

When the (external) Trim Erase option is installed, the Write Busy interface line still goes true (low) whenever the Write Enable or the (external) Trim Erase functions are energized.

3.10 CIRCUIT DESCRIPTION, PCBA NO. 600266

3.10.1 INTERFACE CONTROL AND OUTPUT STATUS

Refer to Schematic No. 600265 sheet 2 in connection with the following discussion on signal input/output lines.

Each active signal input/output line can be terminated via resistor networks U2, U3, and U4. In a typical daisy-chain system, the last drive sharing the signal bus terminates the signal line. For this reason, sockets are provided for the terminating network since system configuration and drive position are determined by the user.

3.10.1.1 Select Control

The Select lines provide a means of selecting and de-selecting a disk drive. The four Select lines, ISLT0 through ISLT3, are routed to their respective terminator networks and then to jumpers W6, W5, W4, and W3 (zone G7). The standard configuration enables the drive to respond to ISLT0 commands where W6 is installed with W3, W4, and W5 omitted. The four jumpers are bussed together and use gate U15 pin 5 as the receiver. Only one jumper must be installed at a time, corresponding to the drive position shown below.

ISLT0 = W6
ISLT1 = W5
ISLT2 = W4
ISLT3 = W3

U15 pin 6 (SEL) is inverted via U15 (zone G2) pin 3 (NSEL). The SEL signal is used to gate

(1) the Head Load command U8 (zone G6) pin 1
(2) the Ready Status at U19 (sheet 4 zone E4) pin 1
(3) the Write Protect signal at U8 (sheet 4 zone B2) pin 10
(4) the Track Zero Status U8 (sheet 5 zone H2) pin 5
(5) and gates the SLT/DF12 signal at U16 pin 10.

NSEL at U15 (zone G2) pin 4 enables receiver U10 (sheet 3 zone C7) pins 8 and 11 for positioner commands and may be used to control the Power Save option via W30 (sheet 5 zone F7).

3.10.1.2 Head-Load Select

Loading the head on a FD5X1 series disk drive is accomplished two ways: (1) the head may be loaded by first selecting the disk drive, then issuing a Head-Load command; or (2) by issuing a separate Head-Load command independent of Select. Interface signal IHLD (J1-23) is terminated by U3 (zone F8) pin 12 and receiver U15 pin 9. This signal is gated with Select at U8 pin 2 and routed to the Head Load driver via U10 (zone F5) pin 1. The head will load only if the drive has been selected and the IHLD command has been issued.

An alternate method of loading the head can be accomplished by issuing a command via one of the Head load lines (IHLD0—IHLD3). These four Head Load lines are routed through jumpers W7, W8, W9, and W10. Signal lines IHLD1 and IHLD3 are routed directly to terminators, lines IHLD0 and IHLD2 are routed to jumpers W12 and W11 that select terminators U3 and U4, respectively. The standard configuration enables the drive to respond to Head Load 0 commands when jumpers W7, W11, W12 are installed and W8,

W9, and W10 are omitted. Jumpers W7, W8, W9, and W10 are bussed together and use pin 3 of gate U10 as a receiver gate. The output of U10 pin 1 is the logic form of the Head Load signal and is inverted by U14 pin 5 which provides NHLD to the Head Load driver (sheet 3, zone G8) and also controls the Power Save option via W31 (sheet 5, zone F7).

IHLD0 (J1-6) and IHLD2 (J1-8) may be used to supply to the interface either +5v dc or approximately 3v dc by omitting W7, W9, W11, W12 and installing (1) W15, W16 for the 3v dc or (2) W17, W18 for the +5v. This configuration will disable the use of these lines for their normally intended usage. Diodes CR3, CR4 (zone E6) and resistor R17 provide the coarse +3v. Additionally, the terminators may be powered from interface lines IHLD0 (J1-6) and IHLD2 (J1-8) by omitting W7, W9, W11, W12, W15, W16, W17, W18, W36. The terminator supply voltage will then depend on W37 and W38. In the standard configuration, the terminator supply voltage is supplied from the +5v distribution on the PCBA via W36.

Jumper W13, when installed, is used to disable the Sector Separator circuitry. With jumper W13 omitted, the NDSSEP signal (sheet 4 zone F8) is allowed to go high through resistor R2, thus enabling the Sector Separator circuitry of U5, U6, U7, and U20.

Jumper W14, when installed, causes U16 pin 8 to go high, U15 pin 10 to go low, and also disables interface drivers U1 pins 6 and 11, and U9 pins 8 and 11; when omitted, U16 pin 9 goes high through R20. In this condition, the output at U16 pin 8 is dependent on the Select status. If the drive has been selected, U16 pin 8 goes low enabling the previously mentioned drivers via U15 pin 10. In addition, the SLT/DF12 signal (sheet 3 zone D7; sheet 4 zone D7) enables U10 pin 5 and U32 pin 9.

3.10.1.3 Seek Busy Status

The Seek Busy interface signal is issued in response to a Step command. This signal indicates to the user the activity of the positioner and when it is allowable to request another seek operation.

Seek Busy circuitry is shown on sheet 2 of Schematic No. 600265, zones E and D. The circuit is initialized by the Power Sense (NPSEN) signal and inhibited during a write operation (WBSY). Timing for the Status signal is controlled by gated oscillator U29, counter U21 and single-shot U13. Initially, U22 pin 15 is set, U22 pin 11 and U23 pin 5 reset. With U22 pin 15 high, the oscillator is disabled by U12 pin 10. Operation is initiated by a Step pulse (STP). This Step pulse resets U22 pin 15, U22 pin 11, and U23 pin 5 at the same instant U13 pin 13 goes active for a period of approximately 2.5 msec. The oscillator remains disabled and counter U21 is loaded to a count of 10 by single-shot U13 pin 4. The Seek Busy signal (TP3) goes high and the interface line J1-41 goes low. At the end of the single-shot timeout, the oscillator is enabled and the load input to counter U21 pin 11 is removed. The frequency of oscillation of U29 pin 3 is established by capacitor C12 and resistors R23, R24, and the frequency is controlled by potentiometer R115. The output of U29 pin 3 is inverted and shaped by U28 and U19 to provide clocking inputs to U21 pin 5 and U23 pin 9. Counter U21 is preset to count from 10 (decimal) and will issue a Carry pulse (U21 pin 12) on the fifth high-to-low transition of the clock input. This Carry pulse is inverted by U30 and clocked into U23 pin 8 causing U23 pin 5 to go high and U12 pin 13 to go low. This action signifies the first available window for a seek operation and is presented to the interface. If no subsequent Step pulse has been issued, U23 pin 5 clocks U22 pin 6. Oscillator U29 pin 3 continues to function and allows U21 to count until a second Carry pulse is generated. The second Carry pulse *clocks* U23 and subsequently U22 pin 6. The second clocking of U22 causes U22 pin 15 to go low and disables oscillator U29. If a subsequent Step pulse is received, the counter loads to 10, then counts as previously described.

3.10.1.4 Read Data Separator

A single-shot data decoder is provided for double frequency applications. This circuitry is shown in Schematic No. 600265, sheet 2 (zones F and G).

The Read Data pulse (RDA) originates from sheet 7, zone D1. Initially, single-shot U5 (sheet 2, zone F4) pin 4 is high causing U6 pin 9 to be reset via U19 pin 6. The RDA pulse is is fed to U7 pins 4 and 10 (zone F3). Unseparated RDA pulses are presented to the interface through U9 pin 3. Since U6 pin 8 is high, the RDA pulse causes U7 pin 8 to go low and single-shot U5 pin 4 to time out. The single-shot is set to time out in approximately 3 μsec, adjustable via R25, and enables U6 pin 11 to be clocked on the subsequent RDA pulse. This action allows the clock pulse to be separated from the data pulse. The separated Read Data and Read Clock are inverted through U14 pins 1 and 9 and then presented to interface drivers U9 pins 9 and 12.

3.10.1.5 Write Interface

The Write interface receivers are shown on Schematic No. 600265 sheet 3 (zone E-F-6). Gate U16 (zone E7) pin 11 disables each interface signal receiver of IWEN, IEEN, IWDA when the drive is Selected and Ready (SRDY, low) or the diskette is Write Protected (NWPT, low).

Write Enable (IWEN, J1-11) is received by U11 pin 8; Erase Enable (IEEN, J1-13) is received by U11 pin 11 and Write Data (IWDA, J1-17) is received by U11 pin 5. Head Current Switch (IHCS, J1-15) is received by U11 pin 2 but is enabled only if the drive is selected and ready (NSRDY, low). The output of each interface receiver is routed to the Read/Write logic as required.

3.10.1.6 Door Lock Enable

The Door Lock Enable (IDLEN, J1-35) interface line is received by U10 pin 6. When pin 6 is low and SLT/DF12 is low, U10 pin 4 goes high causing U30 pin 3 to go low, thereby energizing the LED in the Door-Open Bar Switch. Additionally, U35 (zone D4) pin 10 goes low inhibiting operation of the Door-Open Solenoid. When IDLEN is high, the LED is extingished and the Door-Open solenoid driver enabled. The loading door may now be opened by pushing the Door-Open bar switch. The Door-Open solenoid driver, resistors R101, R102, and transistor Q17, energize the solenoid and allow the door to spring open. When the loading door is open, the Door-Open solenoid driver is disabled via the DOP signal and gate U35 pin 12.

3.10.1.7 Head Load Solenoid Driver

The Head Load Solenoid Driver is shown on Schematic No. 600265 sheet 3 (zone G1). The logic form of the Head Load signal (NHLD), when low, causes U35 (zone G6) pin 6 to go high; this allows R103, and R104 to energize Q22 which energizes the Head Load Solenoid. The output of Q22 can be observed at TP16.

3.10.1.8 Direction-Step/Step In-Step Out Control Logic

The logic that controls the disk drive response to positioner commands is shown on Schematic No. 600265 sheet 3 (zone D6). The drive may be configured to respond to two different forms of interface commands for positioner control.

Jumpers W23 and W24 are used to select the drive response to either the Step In-Step Out form or the Direction-Step form of command. When the jumpers are omitted, the response of the drive is to Step In-Step Out pulses as defined by Paragraph 3.3.2.7. Gate U10 pins 9 and 12 are the receivers for interface lines IST/ST0 and IDIR/STI, respectively. If the drive has been selected (NSEL, low) these receivers are enabled. If the required motion is to

position the head carriage toward the hub, a pulse on the IDIR/STI is received. U10 (zone D6) pin 13 goes high for the duration of the pulse and U16 pin 3 inverts this signal and supplies NSTI to the positioner logic (sheet 5 zone D7). Additionally, this signal is routed to OR gate U16 (zone C4) pin 4 to form the Step Pulse (STP) at U16 pin 6 (TP8). The STP signal intiates the positioner sequence (sheet 5 zone E7). For a Step Out pulse, the IST/STO is active causing U10 (zone C6) pin 10 to go high for the duration of the pulse. U20 pin 8 supplies the logic signal NSTO, and OR gate U16 pin 6 supplies the logic signal STP.

When jumpers W23 and W24 are installed, the IDIR/STI line controls the direction of motion. U15 (zone C6) pins 13 and 12 invert the direction signal for proper polarity to steer the Step pulse to form the appropriate control signal. When the positioner is at Track 0 (NS/TRK0 low), the logic will not respond to subsequent Step-Out commands.

3.10.1.9 Index/Sector Separator

The Index/Sector Separator is shown on Schematic No. 600265 sheet 4 (zones F4, F5). When the disk drive is configured for Hard Sector operation, W13 (sheet 2, zone C6) is omitted causing NDSSEP to go high and thus enabling the Index/Sector Separator.

The Index pulse from U18 (sheet 4, zone H5) pin 13 is routed to U7 pins 2 and 13. Assuming U6 is reset, U7 pin 3 goes low for the duration of the pulse, triggers single-shot U5 pin 9, and clocks U6 pin 3. Single-shot U5 pin 12 *times out* for approximately 4.3 msec and removes the *clear* from U6 pin 1 via U20. U6 pin 5 goes high on the low-to-high transition of U7 pin 3, enables U7 pin 12, and disables U7 pin 1. If the next Index pulse occurs within the single-shot time, this pulse causes U7 pin 11 to go low for the duration of the pulse and is identified as the separated Index pulse, which can be observed at TP9. U1 pins 8 and 3 are the Interface drivers for the Index and Sector pulses.

Additional flip-flop circuitry, U24 and U23 (zone D3), is provided to divide the Sector pulse information and present it to the Interface driver U1 (zone F2) pin 1 via U32 (zone D3) pin 10 (TP2). Jumper W27 allows the full 32-sector decode to be presented to the interface; jumper W28 provides 16 sectors and jumper W29 provides 8 sectors.

3.10.1.10 Ready Status

The Ready Status circuit is shown on Schematic No. 600265 sheet 4 (zone D5). The Ready single-shot U13 pin 9 is triggered on the high-to-low transition of each Index pulse. This single-shot is re-triggerable and *times out* in approximately 220 msec. The period of the Index pulse is 166.67 msec and will re-trigger the single-shot when the disk drive with the diskette inserted is up to speed. J-K flip-flop U24 stores the condition of the Ready single-shot and is cleared if there is a power fault or if the loading door is open. If the disk drive has been selected and is Ready, U19 (zone D4) pin 3 goes low. U14 pins 13 and 12 invert the signal and provide the Selected and Ready status (SRDY) to the interface drivers U9 pins 2 and 6 (sheet 2 zone E2), U1 pins 2 and 10. The Ready signal from U24 pin 3 is also routed through jumper W39 to interface driver U8. The output of U8 pin 11 is routed to jumpers W19, W20,W21, W22 and is selected with respect to disk drive position and provides the Ready Status, independent of Select. The disk drive may be configured to provide the Seek Busy signal via W40 (zone D4) to interface driver U8 (zone C2).

3.10.2 INTERLOCKS AND TRANSDUCERS

The Interlocks and Transducer circuitry are shown on Schematic No. 600265, sheet 4.

The terminating amplifiers for the Index pulse and Write Protect transducers are similar. Dual operational amplifier U41 (zones B7, G7) compares the conduction of the respective photo-transistors with a reference level set by R95, R97, R99, and R100. Diodes CR5 and CR6 clamp the outputs from any negative excursions.

The Index signal consists of a pulse for each rotation of the index hole in the diskette. It is important that the transition edges of each pulse be sharp. The Schmitt trigger input of single-shot U18 pin 2 provides controlled hysteresis and this single-shot also *times* a controlled pulse width of 0.4 msec.

In the Write Protect circuitry, it is important only to detect the presence of a Write Protected diskette hole. Therefore, it is sufficient to route the output of the sense amplifier through a conventional gate, U14 (zone B3) pins 3 and 4, for internal use, and to route the interface driver, U8 pin 9, as the IWPT signal from U8 pin 8 to pin 33 on connector J1.

The Door-Open Indication switch is conditioned by a cross-coupled latch formed by U31 (zone A5) pin 1 and 3. The two logic signals from this latch, NDOP and DOP, are used to (1) gate the head-load logic, U10 pin 2 (sheet 2, zone F5); (2) inhibit the Door-Open Solenoid Driver via U35 pin 13 (sheet 3, zone B6), and (3) gate the Ready Status, U20 pin 13 (sheet 4, zone C6).

3.10.3 HEAD POSITIONER LOGIC

The Head Positioner Logic, including the Track ircuits, are shown on Schematic No. 600265, sheet 5. Refer to the functional description in Paragraph 2.7 in conjunction with this description.

Positioner control is a function of gated oscillator U27 (zone G6) and logic signals NSTO, NSTI, and STP from the Control logic (Paragraph 3.10.1.7). Control signals NSTO and NSTI are used to set the Direction Control Latch U38 (zone E5) pins 13 and 5. Control signal STP is used to initiate the motion sequence by clocking U33 (pin 9).

Initial conditions are established by the Power Sense circuitry (NPSEN) through U32 pin 13 and U31 pin 8. NPSEN places both flip-flops of U33 (zone E6, E5) into their reset state. Oscillator U27 is held inactive by U38 (zone F5) pin 3 and will remain inactive until U33 pin 6 or pin 2 goes low. The pulse at U38 pin 3 can be observed at TP12 (zone F4).

Upon receipt of a Step pulse, U33 pin 5 will go high if Not Write Busy (NWBSY) is high and pin 10 is not cleared by U32 pin 13. U33 pin 5 sets on the trailing edge of the Step pulse. When U33 pin 6 goes low, it enables Oscillator U27 via U38 pin 3 (TP12); additionally, $\phi 1$ of the Stepper Motor Drive is disabled by U40 pin 2 (zone F3).

The output of Oscillator U27 pin 3 (TP10) goes high for a period of time determined by the time it takes for capacitor C23 to charge to the high internal threshold of U27 pin 6 through R36 + R37 + R38. When the sense threshold of U27 pin 6 is reached, U27 pin 3 goes low for a period of time determined by the time C23 discharges to the low threshold through R37. At this time U27 pin 3 goes high again (if U27 pin 4 is still enabled) and then the oscillation process repeats itself. Oscillator U27 typically generates two consecutive positive periods of unequal duration for each Step pulse. The unequal durations are a result of the first charging cycle that occurs each time U27 is enabled; C23 initially charges from a voltage level lower than the threshold level that is achieved during sustained Oscillator operation. The output of the Oscillator is shaped by U28 (zone G6) pins 3 and 4 then inverted for proper polarity by U31 pins 5 and 6.

The oscillator *clocks* U33 (zone 5) pin 12 on the high-to-low transitions. U33 pin 3 is initially reset but goes high on the trailing edge of the first internal clock pulse initiated by a Step command. This change causes U33 (zone E6) pin 10 to reset through U32 pin 13 and continues to enable Oscillator U27. The output states of U33 are directed via the Direction Multiplexer U39 (zone E4) to the $\phi 2$ or $\phi 3$ pre-driver, dependent on the state of the Direction Latch U38 (zone B5). If a Step-In command (NSTI) had been issued, U38 pin 6 would be high, enabling $\phi 3$ pre-driver for the state of U33 pin 5 and $\phi 2$ pre-driver for the

state of U33 pin 3. The phase sequence established allows first $\phi 3$ to be active, then $\phi 2$. The second internal clock pulse causes U33 pin 2 to go high; this transition triggers a single-shot U18 (zone G4) for a period of approximately 40 msec. U18 pin 12 energizes the $\phi 1$ Driver transistor Q21 (zone F2). Additionally, the reset states of U33 cause the $\phi 1$ Hold driver, transistor Q20 (zone E2), to be energized via U38 pin 3 (TP12) and U40 pins 1 and 2. If the disk drive incorporates the Power Save feature, the positioner $\phi 1$ will be disabled if the head is unloaded (NHLD, high) or the drive is not Selected (NSEL, high) depending on whether W30 or W31, W32 and W33 are installed. Gates U40 pins 9 and 8, and 13 and 12, will disable the $\phi 1$ drivers.

The output drive circuitry for $\phi 1$ consists of transistors Q20 and Q21. Transistor Q21 is used as the phase driver, allowing full current through $\phi 1$. Transistor Q20 is used as a hold or detent driver, operating at a reduced current through a 33-ohm resistor (across pins 10 and 12 on P2) mounted external to the PCBA. Transistors Q19 and Q18 provide the drive for phases $\phi 2$ and $\phi 3$, respectively.

The Track-0 circuitry relies on a *Form-C* switch that is de-bounced by a cross-coupled latch formed by U31 (zone H7) pins 11 and 13. When active, the Track-0 latch (NS/TRK0) disables the control logic gate U20 pin 11 (sheet 3 zone C5) and prevents it from propagating any additional Step-Out commands. The output of the Track-0 latch is also provided to an interface driver through U32 pin 5. The status is allowed only to propagate through to the interface (J1-32) after the time out associated with the $\phi 1$ single-shot, U18. The high-to-low transition of U18 pin 5 clocks U26 pin 1 and enables U32 pin 6 to allow the Track 0 signal to reach interface drive U8 (zone H2) pin 4.

3.10.4 POWER SENSE CIRCUITRY

The Power Sense circuit shown on Schematic No. 600265, sheet 5 (zones A through D), consists of the undervoltage monitors of the +24v dc, +5v dc, and —5v dc supplies. As an option, circuitry is provided to regulate a —12/—15v dc input to approximately —5v dc.

Initial conditions assume that all supplies are at their zero value and all components are inactive, i.e., capacitors discharged.

Application of dc power can be sequential or simultaneous. In either case, the initialization of the drive electronics is dependent on the last of the three dc voltages that achieves its minimum sense value. The control elements are the charge state of capacitor C5, and the logic threshold of U28 (zone C4) pin 9. Capacitor C5 is not allowed to charge until the three dc-sense voltages have been reached. For the +24v dc supply, the sense circuitry consists of transistor Q1, VR1, R7, R8, R9, and R19. The base of Q1 is controlled by the conduction of VR1 through R8 and R9 and will not conduct until the +24v dc (J7-7) has exceeded 17.6v dc. If the other voltages have been established, capacitor C5 is allowed to charge; if not, resistor R10 diverts the charge current to transistor Q2 or Q3.

Transistors Q2, Q4, zener diode VR4, and resistors R15, R16, and R18 sense the +5v dc supply (J7-3). Transistor Q2 relies on the state of Q4 and the +24v dc supply. Transistor Q4 will not turn on until the +5v dc supply has reached +4.3v dc or greater; at that time, zener diode VR4 will conduct and establish a turn-on voltage for Q4 via R15 and R16.

The negative voltage supply is sensed off the common tie point of jumpers W1 and W2. If —5v dc operation is required, W1 is installed and W2 is omitted. If the Negative Voltage option (—12v dc/—15v dc) is required, W1 is omitted and W2 installed. Resistors R11, R12, and zener diode VR2 form a —5v dc regulator. Resistors R13, R14, zener diode VR3, and transistor Q3 sense the —5v dc supply.

The signals supplied from the Power Sense circuitry are NPSEN, PSEN, and APSEN.

3.10.5 WRITE/ERASE LOGIC

The Write/Erase logic circuitry is shown on Schematic No. 600265, sheet 6.

3.10.5.1 Write Waveform Generator

At the beginning of a write operation, the Write Enable signal (WEN, zone D8) goes high (TP11). WEN going high removes the clear signal to pin 8 of the Write Data flip-flop U26 (zone E7). The Write Data flip-flop is now in a reset state, conditioned to respond to Write Data information. The Write Enable signal enables the write current source through U28 pins 13 and 12 (NWEN) and to initiate the erase timing.

The composite Write Clock and Data signal, WDA, (double frequency encoding) is inverted by U28 (zone B8) pins 5 and 6, then presented to the clock input of Write Data flip-flop U26 pin 6. The Write Data flip-flop is toggled on the high-to-low transition of each pulse thereby changing the direction of the current flowing in the magnetic head.

The outputs of Write Data flip-flop U26 pins 10 and 11 are processed by the level-changing circuit comprised of U36 pins 1 and 3, and resistors R84, R85, R86, and R87. The outputs of the level-changing circut (node of resistors R84 and R85, node of resistors R86 and R87) are fed to the Write Drive Switch, transistors Q13 and Q14 (zone F6). The emitters of these transistors are tied together to the collector of Q12 (zone F6) which is the write current source. The collectors of Q13 and Q14 are routed to the center-tapped magnetic head through diodes CR16 and CR17. This results in the required write current waveform. Resistor R67, whose value is chosen for an optimum current waveform, dampens the read/write head.

The basic current source consists of voltage reference components VR5, CR7, R93, and R94 (zones F6 and 7). These components establish a voltage differential across R92 and the base-emitter junction of Q12. Thus, transistor Q12 and resistor R92 form the basic current source of approximately 4 ma. An additional current source is formed by U36 pin 8, R55, R83, R89, and Q10. This source is energized whenever the Head Current Switch (HCS) is high and causes an additional 1 ma (5 ma total) to flow into switch transistors Q13 and Q14.

During system power-up or loss of one of the dc voltages, the write current source is disabled by circuitry consisting of R77, R78, R79, Q9 and Q11 (zone H6 and 7). When the control signal APSEN goes low, transistor Q11 turns off, thereby turning off Q9. This action prevents erroneous information from being recorded during system power-up or loss of one of the three dc voltages described in Paragraph 3.10.4.

Diodes CR16 and CR17 (zone D5) and resistors R70 and R71 are not functionally required for the write circuitry but provide isolation of the sensitive read circuits from the write circuitry. During a read operation, the head windings are approximately at ground potential, diodes CR16 and CR17 are cut off by the —5v dc return through R70 and R71.

3.10.5.2 Erase Current Driver

The Erase Current Driver circuitry consists of U35 pin 2 (zone B4), C43, R73, R74, R75, R76, R81, R82, and Q16. These components form and control erase current source of approximately 85 ma. The circuit is disabled by signal APSEN via R80, Q15 and enabled by either the Internal Trim Erase components (connected via jumper W25) or as an option, the External Erase signal EXT/EEN (jumper W26 installed).

The Internal Trim Erase timing is controlled by a dual single-shot, U37 (zone C6), plus C29, C38, R39, R56, and R91. When Write Enable (WEN) goes high, U37 pin 12 is active and provides a pulse approximately 200 μsec in duration. This pulse provides a *pre-delay* to the turn on of the Erase Current Driver via U38 pin 8 and U19 pin 13 and 11.

At the completion of the write operation, WEN goes low causing the second half of U37 pin 4 to go active. The pulse from this single-shot provides a *post-delay* to turn off of the Erase Current Driver for approximately 475 μsec via U19 pins 12 and 11. The value of this delay is adjustable with R39 and optimized to tolerances arising from head, track position, and diskette speed.

The Write Enable and Trim Erase signals are ORed through U32 (zone A4) pin 1, which provides a Write Busy Status (NWBSY) and also provides the inverted signal WBSY via inverter U28 pin 10.

3.10.6 READ AMPLIFIER

The Read Amplifier and associated digital circuitry is shown on Schematic No. 600265, sheet 7.

3.10.6.1 Read Switch

The Read Switch circuitry consists of components CR8 through CR15, R50, R54, R63, R64, R65, R66, R69, Q8, and non-inverting gate U36 pins 10 and 11. The purpose of this switch is to isolate the Read Amplifier from the considerable voltage excursions across the magnetic head that occur during a write operation. During a write operation, NWEN is low causing the output of U36 pin 10 to go low. U36 pin 10 turns on the Read switch transistor Q8 (zone F7) via R54 and R50. At this point, the collector of Q8 is approximately + 24v dc so that the anodes of CR8 and CR9 are *pulled* positive. The junctions of CR8 and R65, CR9 and R66 are then pulled positive, thereby cutting off CR10, CR11, CR12, and CR13. Diodes CR14, CR15 and resistors R63, R64 clamp the inputs of U34 (zone D6) so that the voltage input to U34 never gets higher than a diode voltage drop.

During a read operation, NWEN is high, therefore Q8 is cut off and CR8, CR9 are both back biased. The anodes of CR12 and CR13 are at approximately zero volts because they are connected through low impedance head windings to ground. Approximately 0.20 ma of current is available through resistor R63 and R64. Additionally, 0.40 ma is demanded by R65 and R66 so that each of the four diodes (CR10, CR11, CR12, and CR13) have approximately 0.20 ma of current flowing through them.

In this condition, the diode bridge provides a low impedance path for the head signal to Preamplifier U34. Capacitor C42 decouples any Read switch noise to ground.

3.10.6.2 Preamplifier

Preamplifier U34 (zone D6) is a balanced-in/balanced-out high-pass circuit whose gain is controlled by resistors R48, R68. Capacitor C39 is the reactive component that establishes the high-pass characteristic of this amplifier. Potentiometer R48 is provided to allow gain adjustment, compensating for different read head sensitivities thus reducing the dynamic range of U34.

A gain of approximately 20 is used to avoid problems encountered by amplification of the small dc offset voltage introduced by Read switch. The level of the signal measured differentially between pins 7 and 8 of U34 is approximately 250 mv for an all-ones pattern at track 0.

3.10.6.3 Filter

The balanced output from U34 is fed via the linear phase filter L3, L4, L5, L6, C34 to a terminating network consisting of C32, C33, R47, and R49. This filter has a linear phase response over the frequency of operation and attenuates the high frequency noise from the signal.

3.10.6.4 Differentiator

The output of the filter is fed to the Differentiator circuit U25 (zone D4). Capacitors C32 and C33 are used to couple the filter to amplifier U25 and to isolate any dc offset voltage at the output of U34. Amplifier U25 is similar in operation to Preamplifier U34 with the exception that the gain network is fixed and provides a 6 db-per-octave gain rise characteristic over the frequency range of operation, thus providing the required differentiator characteristics. The gain components are R45 and C27.

For bandwidth control (Single/Double Density Units), two values of bandwidth are required to accommodate the range of head resolution values for double density operation.

The Bandwidth Control circuitry consists of U35 (zone G5) pin 4, R46, R51, R52, R53, and FET Q7 (zone E4). The Head Current Switch (HCS) signal must be used during a Read operation. When HCS is high, U35 pin 4 goes low causing Q7 to turn on. With FET Q7 on, resistor R46 is placed in parallel with R45 thereby increasing the bandwidth of amplifier U25 (zone D4) so it can read the denser inner tracks (Tracks 43 through 76). When HCS is low, bandwidth switch Q7 is off. This reduces the bandwidth and improves the response of differentiator U25.

3.10.6.5 Zero-Crossing Detector

The output of U25 is fed to emitter followers Q5 and Q6 to prevent the U25 output from being improperly loaded. The emitters are ac coupled to inputs of the Zero-Crossing Detector, U17 (zone D2), which can be observed at TP4 and TP5.

U17 is a bi-directional single-shot that accepts the differential Read signal. The output of U17 pin 11 (TP6) is a single 200 $\pm$50 nsec pulse for each and every zero-crossover. The pulse width is determined by capacitor C19 and resistor R34. Ac hysteresis is provided by C16 and R29 to eliminate the possibility of multiple detection of the zero-crossover point.

U17 pin 3 is disabled by the Write Busy (WBSY) signal during a Write operation. The output of U17 pin 11 is routed to the Data Decoder (RDA signal) and then fed to the interface driver U9 (sheet 2 zone E2).

SECTION IV
MAINTENANCE AND ADJUSTMENTS

4.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments. Parts replacement is contained in Section V. Section III contains the theory of circuit operation for reference.

4.2 SCHEDULED MAINTENANCE

PERTEC Flexible Disk Drives are designed to operate with a minimum of maintenance and adjustments and replacement of parts is designed to be as simple as possible.

Repair equipment is kept to a minimum and only common tools are required in most cases.

4.2.1 MAINTENANCE PHILOSOPHY

To ensure that the disk drive operates at its optimum design potential, a scheduled preventive maintenance program is recommended.

The objective of any maintenance program is to provide maximum machine readiness, with a minimum of downtime. To provide this type of reliability, it is necessary to perform preventive maintenance on the disk drive at the intervals specified in Table 4-1.

In general, it is unnecessary to alter any adjustment on equipment that is performing in a satisfactory manner.

Table 4-1
Preventive Maintenance Schedule

Maintenance Operation	Frequency (Months)	Time Required (Minutes	Manual Paragraph Reference
Stepper Motor Lead Screw Lubrication	12*	5	4.3.2
Head Cleaning	1*	2	4.3.1
Head-Load Pad Replacement	12*	5	4.7.11.1
CE Alignment Check	12	10	4.6.3
*Minimum may be required more frequently dependent upon usage and environment.			

4.3 CLEANING AND LUBRICATION

The only part of the disk drive that requires regular cleaning is the magnetic recording head.

4.3.1 CLEANING THE HEAD

To clean the magnetic head, use a lint-free cloth or cotton swab moistened with isopropyl alcohol or DuPont Freon TF. Wipe the head carefully to remove all accumulated oxide and dirt. Dry the head using a lint-free cloth.

NOTE

The magnetic head must be cleaned after head load pad replacement.

CAUTION

ROUGH OR ABRASIVE CLOTH SHOULD NOT BE USED TO CLEAN THE MAGNETIC RECORDING HEAD. USE ONLY ISOPROPYL ALCOHOL OR DU PONT FREON TF. USE OF OTHER CLEANING SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY DAMAGE THE HEAD LAMINATION ADHESIVE.

4.3.2 LUBRICATION OF THE STEPPER MOTOR

Prior to lubrication, the stepper motor shaft (lead screw) should be cleaned. This is accomplished by wiping the shaft with a lint-free cloth lightly moistened with isopropyl alcohol. Lubricate the shaft by applying four drops of Lubricant, PERTEC Part No. 665-0008.

CAUTION

DO NOT CONTAMINATE MAGNETIC RECORDING HEAD OR HEAD PAD WITH LUBRICANT. DAMAGE TO THE RECORDING SURFACE CAN BE CAUSED BY LUBRICANT DEPOSITED ON THE MAGNETIC HEAD OR LOAD PAD BEING TRANSFERRED TO THE DISK.

4.4 PART REPLACEMENT ADJUSTMENTS

Table 4-2 lists the adjustments required when a part or subassembly in the disk drive is replaced.

4.5 ELECTRICAL ADJUSTMENTS

The following paragraphs describe the test configurations, test procedures, adjustment procedures, and related adjustments to the electrical functional portions of the disk drive.

The following test equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 465 (vertical and horizontal sensitivity ±3 percent specified accuracy) with three X10 probes each with individual ground leads.

(2) Counter Timer, Monsanto Model 100B (±0.1 percent specified accuracy).

(3) Work diskette.

Table 4-2
Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	Time Required (Minutes)	Manual Paragraph Reference
Stepper Motor Assembly	Head Load Time CE Alignment index Sensor Alignment	25	4.5.4 4.5.5 4.5.6
Head Carriage Assembly	Head Load Time CE Alignment Index Sensor Alignment Read Amplifier Gain Track-0 Switch	25	4.5.4 4.5.5 4.5.6 4.5.2 4.5.7
Head Load Arm/Head Load Solenoid	Head Load Time Compliance Check	5	4.5.4 5.1.11.2
Head Load Pad	Head Load Time Compliance Check	2	4.5.4 5.1.11.2
Track-0 Switch Assembly	Index Sensor Track-0 Switch	15	4.5.6 4.5.7
LED Assembly	CE Alignment	10	4.5.5
Photo-Transistor Assembly	CE Alignment	10	4.5.5
Write Protect Assembly	None	10	-
Door Open/Close Switch	None	10	-
PCBA	Stepper Motor Timing Read Amplifier Gain	2	4.5.3 4.5.2
Auxiliary PCBA	None	3	-
Bezel	Diskette Stop	2	5.1.10.2
Cartridge Eject Assembly	None	4	-
AC Motor	None	10	-
Belt	None	4	
Cone Clamp Assembly	None		5.1.15
Door Open Stop	None	2	5.1.17

4.5.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure taking into consideration the assumed accuracy of the test equipment specified in Paragraph 4.5.

When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure.

NOTE

Some adjustments may require corresponding adjustment in other parameters. Ensure adjustments are made as specified in the individual procedures. The user-supplied +5, —5, and +24 voltages must be checked prior to attempting any electrical adjustment.

4.5.1.1 FD400 and FD5X0 Test Point Grounds

The only ground reference test point to be used for digital measurements is TP6. For Write Analog signals the ground reference is TP1, for Read Analog signals the ground reference is TP2. All test points referred to are located on the single PCBA unless otherwise noted.

4.5.1.2 FD5X1 Test Point Grounds

The only ground reference test points to be used for digital measurements are TP15 and TP17. For Write Analog signals the ground reference is TP13, for Read Analog signals the ground reference is TP7. All test points referred to are located on the single PCBA unless otherwise noted.

4.5.2 READ AMPLIFIER GAIN

When either the PCBA or the magnetic read/write head is replaced, the read amplifier gain must be checked and, if necessary, adjusted.

4.5.2.1 Test Configuration

(1) Apply power to the drive.

(2) Install a work diskette in the disk drive.

(3) Close the diskette loading door.

(4) Load the magnetic head.

(5) Perform a track 0 seek operation.

4.5.2.2 Test Procedure

(1) Write an all-ones pattern on the diskette.

(2) Set horizontal time base on the oscilloscope to 20 msec per division.

(3) Using the oscilloscope signal probes, observe the signal at the output of the differentiator amplifier at TP4 and TP5 on the PCBA; place ground clips of signal probes as established in Paragraph 4.5.1.1 or 4.5.1.2. This reading is made differentially, i.e., A + B with B inverted.

(4) Acceptable Limits

- 3.5v peak-to-peak (maximum)
- 2.5v peak-to-peak (minimum)

4.5.2.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 4.5.2.1.

(2) Write an all-ones pattern on the diskette at track 0.

(3) Using the oscilloscope signal probes differentially (A + B with B inverted), observe the output of the differentiator amplifier at TP4 and TP5 on the PCBA. Place ground clips of signal probes as established in Paragraph 4.5.1.1 or 4.5.1.2. Adjust R76 (for FD400 and FD5X0) or R48 (for FD5X1) to 3.0v peak-to-peak.

4.5.2.4 Related Adjustments

- None.

4.5.3 STEPPER MOTOR TIMING

The pulsewidth of the stepper motor internal oscillator U13 (for FD400 and FD5X0) or U27 (for FD5X1) is set by adjusting potentiometer R2 (for FD400 and FD5X0) or R38 (for FD5X1) on the PCBA.

4.5.3.1 Test Configuration

(1) Apply power to the drive.

(2) Install a work diskette in the drive.

(3) Close the diskette loading door.

(4) Load the magnetic head.

(5) Connect Monsanto Counter Timer (Model 100B, or equivalent) as an interval timer to TP8 (for FD400 and FD5X0) or TP12 (for FD5X1) on the PCBA.

4.5.3.2 Test Procedure

(1) Perform a repetitive Step-In operation followed by a repetitive Step-Out operation at not less than 30 msec interval between steps.

(2) Note duration of the positive-going waveform measured at the test point in Paragraph 4.5.3.1 Step (4).

(3) Acceptable Limits

- 7.0 msec (maximum)
- 6.8 msec (minimum)

4.5.3.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustment is performed.

(1) Establish test configuration described in Paragraph 4.5.3.1.

(2) Adjust potentiometer R2 (for FD400 and FD5X0) or R38 (for FD5X1) until the positive-going portion of the signal measured at TP8 (for FD400 and FD5X0) or TP12 (for FD5X1) is 6.9 msec.

4.5.3.4 Related Adjustments

- None.

4.5.4 HEAD LOAD SOLENOID/HEAD LOAD ARM ADJUSTMENT

Proper head retraction distance and correct load time for the magnetic head is assured by performing the following adjustment procedure. Refer to Figure 4-1 in conjunction with this procedure.

4.5.4.1 Test Configuration

(1) Perform the Compliance Check, Paragraph 5.1.11.2.

(2) Bend the upper tab on the relay frame upwards and clear of any armature motion (Figure 4-1), if not already clear.

(3) Back off the Allen-head adjustment screw to allow maximum armature travel (Figure 4-1).

4.5.4.2 Mechanical Test Procedure and Adjustment

(1) With disk drive in a horizontal position, apply power to the disk drive and install a work diskette.

(2) Perform a track-0 seek and activate the head load solenoid.

(3) Insert a 0.005-inch-thick feeler gauge between the plastic slot-head adjustment screw on the end of the armature and the ledge of the head carriage (Figure 4-1).

(4) Loosen the locknut and rotate plastic slot-head adjustment screw until it contacts feeler gauge.

(5) Secure plastic adjustment screw with locknut and remove feeler-gauge blade. Recheck gap.

(6) Perform a seek to track 76 and observe gap between the end of the plastic screw on the armature and the head ledge on carriage. Maintain minimum gap of 0.003 inch.

(7) Readjust plastic slot-head adjustment screw on armature, if necessary, to maintain minimum gap of 0.003 inch (Figure 4-1).

(8) With the head at track 76, insert a 0.010 feeler gauge between the end of the extension on the head-load arm and the ramp on the platen load spring (Figure 4-2).

(9) Move platen load spring horizontally until tip of the load arm extension contacts the feeler gauge.

(10) Remove feeler gauge; recheck the gap by re-inserting the feeler gauge and adjusting the platen load spring, if necessary.

(11) Perform a seek to track 0. Ensure that the gap between the head-load arm extension and the ramp on the platen load spring is never less than 0.010 inch at any time during the seek operation.

(12) Reset gap for 0.010 inch clearance at that point, if necessary.

(13) Ensure that a gap of 0.010 to 0.020 inch is maintained throughout carriage travel. Secure platen load spring mounting screws.

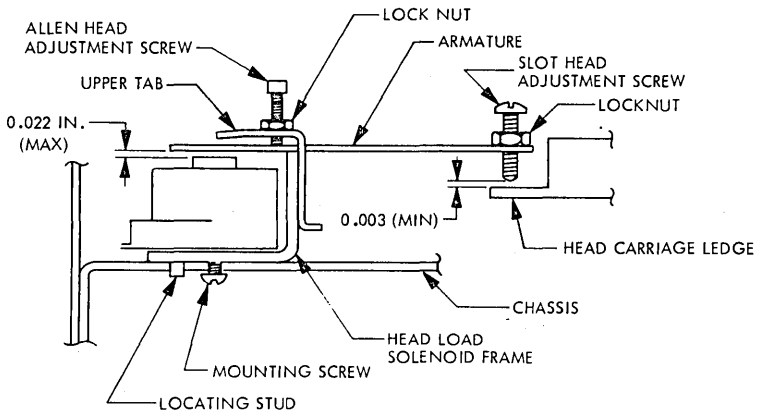


Figure 4-1. Head Load Solenoid Adjustment

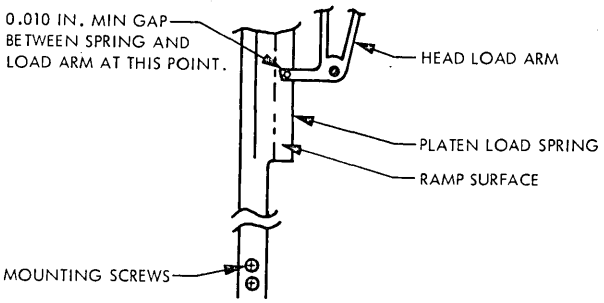


Figure 4-2. Head Load Arm Adjustment

4.5.4.3 Electrical Test and Adjustment Procedure

Refer to Figure 3-1 for appropriate test points.

The electrical operational test is accomplished by measuring the time from the Head Load command to the availability of a usable data envelope. Usable data is defined as at least 83 percent of the peak amplitude available without subsequent dropouts. Figure 4-3 shows that the usable data is available 35 msec after the Head Load command is given. It should be noted that the data envelope waveform may be modulated due to media variations.

(1) Attach oscilloscope probes to the output of the read amplifier differentiator at TP4 and TP5; place ground clips of signal probes as established in Paragraph 4.5.1.1 or 4.5.1.2. Adjust oscilloscope to read differentially (A + B with B inverted). Trigger the oscilloscope on the falling edge of the Head Load signal at TP13 (for FD400 and FD5X0) or TP1 (for FD5X1); place ground clips of signal probes as established in Paragraph 4.5.1.1 or 4.5.1.2.

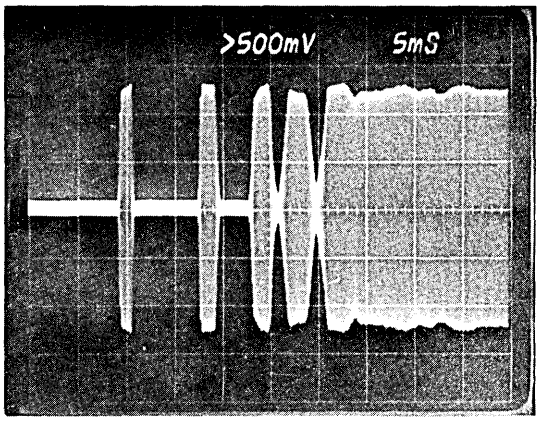


Figure 4-3. Usable Data Envelope

(2) Install a diskette known to have usable recorded data in the drive. Perform a seek to track 0.

(3) Toggle the Head Load signal and measure the time from the start of the trace to the usable data envelope.

(4) Adjust the Allen-head adjustment screw on the head load solenoid frame until the 83 percent peak amplitude (Figure 4-2) point is met at 40 msec after the Head Load command is given. Secure the Allen-head screw with the locknut.

(5) Check gap between armature and solenoid coil post (gap must not exceed 0.022 inch).

(6) Perform a seek to track 76 and assure that head load time is 40 msec or better.

(7) Unload the head and ensure that the head load pad leaves the diskette surface for any portion of a revolution.

(8) Perform a seek to track 0 and ensure that the head load pad does not touch the disk surface for any portion of a revolution.

4.5.5 CE ALIGNMENT

The CE alignment procedure locates the magnetic read/write head gap at the proper radial distance from the hub center line, thus assuring accurate track location. The drive must be CE aligned after replacement of the stepper motor or head carriage assembly. The CE diskette is also used to set Index sensor adjustments.

4.5.5.1 Preliminary Preparation of the Disk Drive

(1) Loosen the four stepper motor retaining screws.

(2) Manually rotate the stepper motor shaft until the carriage is positioned at approximately track 0. Ensure that the carriage does not rest on the track 0 stop.

(3) Apply the necessary power and control to turn the drive on.

(4) Insert a CE Alignment Diskette (PERTEC Part No. 600202) into the drive and close the loading door.

(5) Load the magnetic head.

(6) Attach oscilloscope signal probes to test points TP4 and TP5; place ground clips of signal probes as established in Paragraphs 4.5.1.1 or 4.5.1.2. Adjust the oscilloscope to read differentially (A + B with B inverted). Sync the oscilloscope on the leading edge of the Index pulse at TP10 (for FD400 and FD5X0) or TP9 (for FD5X1); place ground clip of signal probe as established in Paragraph 4.5.1.1 or 4.5.1.2.

CAUTION

DO NOT ENABLE THE WRITE OR ERASE MODE OF OPERATION WHILE A CE DISKETTE IS INSTALLED IN THE DRIVE. ALIGNMENT DATA RECORDED ON THE DISKETTE CAN BE DESTROYED.

4.5.5.2 Track Alignment

(1) Perform Preliminary Preparation of the Disk Drive, Paragraph 4.5.5.1.

(2) Manually slide stepper motor toward rear of chassis; secure lightly with retaining screws.

(3) Perform 38 Step-In commands. The carriage will move to track 38 (approximately).

(4) Manually turn stepper motor shaft until a *cats-eye* pattern (see Figure 4-4) is observed on the oscilloscope.

NOTE

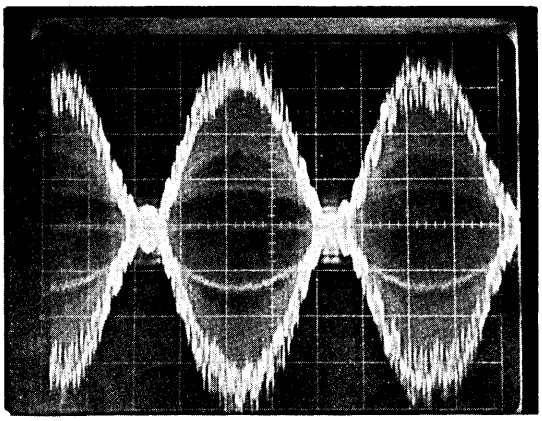
Only a slight movement of the stepper motor shaft should be necessary to observe cats-eye pattern.

(5) Note the direction of movement (toward or away from track 0) required to observe the *cats-eye* pattern. The direction noted indicates the direction that the stepper motor must be moved to be in alignment.

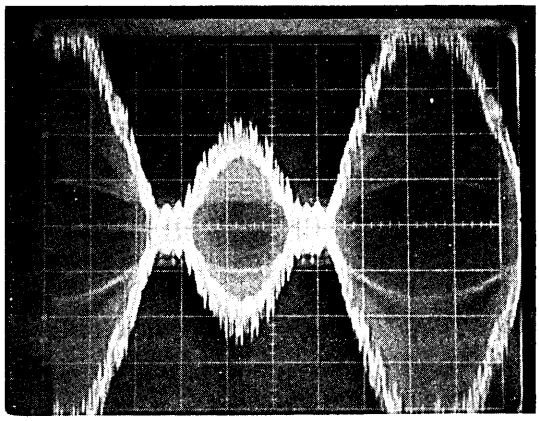
(6) Lightly tap the stepper motor in the direction noted until the *cats-eye* pattern observed has equal amplitudes (one lobe being 80 percent of the other). Refer to Figure 4-4.

(7) Secure stepper motor by tightening the four retaining screws. Torque the two front screws to 16 in-lb and the two rear screws to 6 in-lb.

(8) Verify Step (6) after securing stepper motor mounting screws. Repeat Steps (4) through (6) as required.



Head Properly Aligned



Head Improperly Aligned

Figure 4-4. CE Alignment Oscilloscope Patterns

4.5.6 INDEX SENSOR AND SKEW ALIGNMENT

(1) Apply the necessary power and control to turn the drive motor on.

(2) Insert a CE Alignment Diskette (PERTEC Part No. 600202-02) into the drive and close the loading door.

(3) Load the magnetic head.

(4) Attach the oscilloscope signal probes to test points TP4 and TP5 on the PCBA; place ground clips of signal probes as established in Paragraphs 4.5.1.1 or 4.5.1.2. Adjust the oscilloscope to read differentially (A + B with B inverted). Sync the scope on the leading edge of the Index pulse; TP10 (for FD400 and FD5X0) or TP9 (for FD5X1); place ground clip of signal probe as established in Paragraph 4.5.1.1 or 4.5.1.2.

CAUTION

DO NOT ENABLE THE WRITE OR ERASE MODES OF OPERATION WHILE A CE DISKETTE IS INSTALLED IN THE DISK DRIVE. ALIGNMENT DATA RECORDED ON THE DISKETTE CAN BE DESTROYED.

(5) Perform CE alignment as required to locate the *cats-eye* pattern at track 38 (refer to Paragraph 4.5.5).

(6) Perform 37 repetitive Step-Out commands to arrive at track 1.

(7) Set oscilloscope horizontal time base to 20 μsec per division.

(8) Loosen screws retaining the photo-transistor bracket.

(9) Referring to Figure 4-5, adjust photo-transistor bracket until first bit of the 40 sec burst recorded on track 1 occurs 40 ± 40 μsec after the Index pulse.

(10) Secure retaining screws on the photo-transistor bracket.

(11) Perform 75 repetitive Step-In commands and observe the burst on track 76. The burst must be within ± 20 μsec of the position of the burst observed in Step (7), i.e., track 1.

(12) If the bursts are not within ±20 μsec of each other, position the stepper motor horizontally (sideways) to bring the burst into alignment. To position the stepper motor, insert a flat-bladed screwdriver between the stepper motor frame and chassis. The screwdriver may be used as a lever to move the stepper motor in the direction desired.

(13) Return to track 1 and ascertain that the bursts are within 20 μsec of each other; if not, repeat Step (11).

(14) Step to track 76 and verify burst alignment.

(15) Perform a track 1 seek and adjust the index sensor bracket in accordance with Steps (1) through (9) as required to obtain index-to-data time of 40 ± 40 μsec.

(16) Perform a track 38 seek and ascertain that *cats-eye* pattern is to specification (one lobe of the *cats-eye* being 80 percent of the other, minimum). Repeat Paragraph 4.5.5.2, if necessary.

4.5.7 TRACK-ZERO SWITCH ADJUSTMENT

(1) Apply the necessary power and control to turn the drive motor on.

(2) Insert a CE Alignment Diskette (PERTEC Part No. 600202-01) into the drive and close the loading door.

(3) Load the magnetic head.

(4) Position the carriage to track 1. Confirm the track 1 position by observing the index bursts recorded on track 1 (see Figure 4-5). Position carriage to track 0.

CAUTION

DO NOT ENABLE THE WRITE OR ERASE MODES OF OPERATION WHILE A CE DISKETTE IS INSTALLED IN THE DRIVE. ALIGNMENT DATA RECORDED ON THE DISKETTE CAN BE DESTROYED.

(5) Loosen the two hex-head track-0 switch mounting screws.

(6) Adjust the track-0 switch so that it is closed when the carriage is positioned at track 0 and open when the carriage is at track 1. Secure the two hex-head retaining screws.

NOTE

The stepper motor shaft may be slightly and slowly rotated to a null-holding position midway between track 0 and track 1. The switch should be adjusted to just close at this point.

(7) Perform several repetitive Step-In commands to move the carriage away from track 0. Refer to Figure 4-6.

(8) Open the loading door and remove the CE Alignment Diskette.

(9) Remove power.

4.5.8 TRACK-0 STOP ADJUSTMENT

(1) With power removed from the drive and the loading door open, rotate the stepper motor shaft until carriage is positioned at approximately track 0.

(2) Rotate the track-0 stop on the stepper motor shaft until the tabs on the stop and the carriage are approximately 10 to 15 degrees apart. Refer to Figure 4-7.

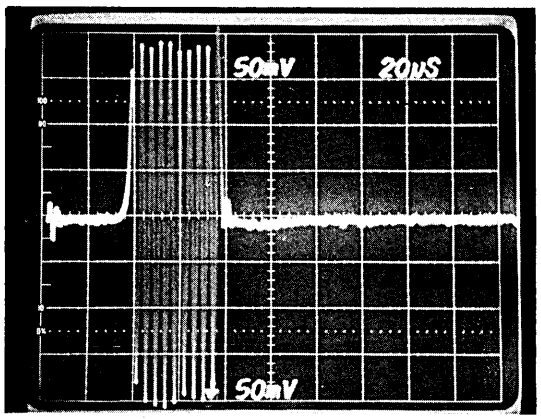


Figure 4-5. Index Sensor Alignment Oscilloscope Pattern

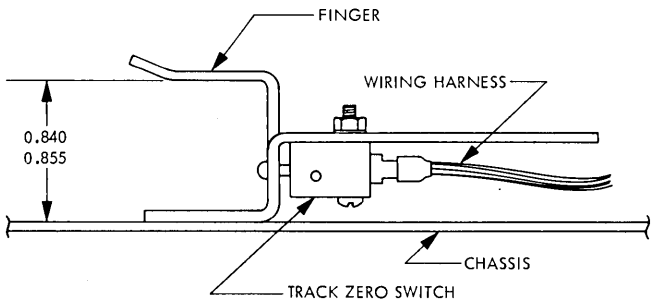


Figure 4-6. Track 0 Switch Adjustment

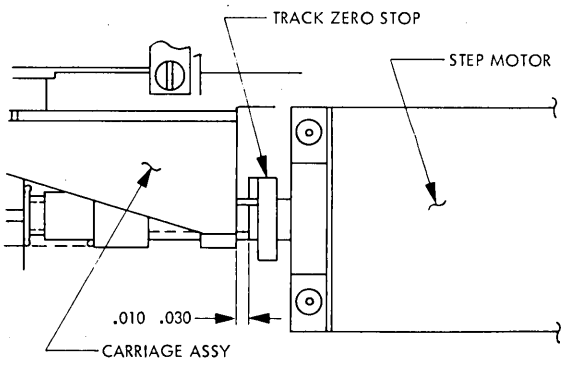


Figure 4-7. Track 0 Stop Adjustment

(3) Insert a 0.020-inch feeler gauge between the tab on the track-0 stop on the stepper motor shaft and the back surface of the carriage.

NOTE
Clearance of 0.020 ± 0.010 inch is acceptable.

(4) If adjustment is required, loosen the Allen-head retaining screw in the track-0 stop. Hold stepper motor shaft and rotate track-0 stop in the appropriate direction.

(5) Tighten Allen-head retaining screw on the track-0 stop to approximately 2 in-lb.

CAUTION
DO NOT OVER TORQUE THE RETAINING SCREW.

4.5.9 BEAM CLAMP ADJUSTMENT

The beam clamp adjustment controls the amount of clamping force applied to the diskette at the hub.

(1) Loosen the four socket-head cap screws securing the beam clamp to the tension shaft.

(2) Open the diskette loading door and insert a 5/8-inch-thick spacer between the top of the door and the bezel; hold door slightly open thereby trapping the spacer between the door and bezel.

(3) Push the cone clamp assembly down into the hub. Center beam clamp sideways to the support plate making the support plate side parallel and equal to sides of the beam clamp.

(4) Secure the socket-head cap screws and torque each of them to 16 ± 2 in-lbs.

4.5.10 ERASE DELAY TIMING

The post-delay to turn off of the Erase driver Q19 (for a FD400 and FD5X1) or Q16 (for 5X1) is set by adjusting potentiometer R131 (for FD400 and FD5X1) or R39 (for 5X1) on the PCBA.

4.5.10.1 Test Configuration

(1) Apply the necessary power and control to position the carriage at track 0.

(2) Insert a work diskette into the drive and close the loading door.

(3) Load the magnetic head.

(4) Write an all-ones pattern on the diskette.

(5) Set the horizontal time base on the oscilloscope to 0.1 msec per division.

(6) Using the test probes oscilloscope, observe the signal at TP15 (for FD400 and FD5X0) or TP14 (for FD5X1) (collector of Erase Driver). Place the ground clip of the signal probe as established in Paragraph 4.5.1.1 or 4.5.1.2.

(7) Sync the oscilloscope on the trailing edge of the Write Enable Signal (WEN) at TP14 (for FD400 and FD5X0) or TP15 (for FD5X1). Place the ground clip of the signal probe as established in Paragraph 4.5.1.1 or 4.5.1.2.

4.5.10.2 Test Procedure

(1) For FD400 and FD5X0, measure the delay time from the Write Enable signal going low (at TP14) to the Erase Driver signal going low (at TP15).

(2) For FD5X1, measure the delay time from the Write Enable signal going low (at TP11), to the Erase Driver signal going low (at TP14).

(3) Acceptable Limits

- 470 μsec (minimum)
- 480 μsec (maximum)

4.5.10.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 4.5.10.1.

(2) Measure the delay time from the Write Enable signal going low to the Erase Driver signal going low in Paragraph 4.5.10.2 Step (1) or (2).

(3) Adjust R131 (for FD400 and FD5X0) or R39 (for FD5X1) for a delay time of 475 μsec at the 50 percent point.

4.5.10.4 Related Adjustments

- None.

4.5.11 DOOR-OPEN SOLENOID ADJUSTMENT (FD5X0 AND FD5X1 ONLY)

(1) Perform the Beam Clamp Adjustment, Paragraph 4.5.9.

(2) Remove dc power from disk drive; loosen two hex-head solenoid-mounting screws and close the loading door.

(3) Hold loading door shut with its front surface grooves flush with the door-open bar switch.

(4) Pivot door-open solenoid until solenoid armature seats securely in notch in cam surface of the pivot bracket on the rear surface of the loading door.

(5) Secure the two solenoid mounting screws.

NOTE

The grooved surface of the loading door must be flush or ±0.015 inches from the surface of the door-open bar switch when the door-open solenoid is properly adjusted.

4.5.12 DOOR-OPEN REQUEST SWITCH (FD5X0 AND FD5X1 ONLY)

(1) Perform the Beam Clamp Adjustment, Paragraph 4.5.9, and the Door-Open Solenoid Adjustment, Paragraph 4.5.11.

(2) Close loading door and loosen screws securing the switch to the beam clamp.

(3) Remove dc power from the disk drive.

(4) Manually raise the door-open bar 0.065 inch.

(5) Hold door-open bar in this position and adjust the door-open request switch until it *mates* at the same time the switch-actuating mechanism contacts the rear edge of the door-open bar.

(6) Secure switch mounting screws.

NOTE

The door-open request switch must activate when door-open bar is raised between 0.040 to 0.090 inch.

4.5.13 SEEK BUSY TIMING (FD5X1 ONLY)

The Seek Busy Timing signal is controlled by adjusting potentiometer R115.

4.5.13.1 Test Configuration

(1) Apply the necessary power and control to position the carriage at track 0.

(2) Insert a work diskette into the drive and close the loading door.

(3) Load the magnetic head.

(4) Perform a repetitive Step-In operation followed by a repetitive Step-Out operation with an interval of not less than 30 msec between steps.

(5) Set horizontal time base on the oscilloscope to 2 msec per division.

(6) Using the oscilloscope test probes, observe the signal at TP3 (Seek Busy). Place the ground clip of the signal probe at TP17. Sync the oscilloscope on the trailing edge of the Step Pulse (STP) signal (at TP8). Retain the ground clip of the signal probe at TP17.

4.5.13.2 Test Procedure

(1) Observe the time between the STP signal going low (at TP8) to the Seek Busy signal going low (at TP3).

(2) Elapsed time should be 10 msec.

4.5.13.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 4.5.13.1.

(2) Measure the time from the STP signal going low (at TP8) to the Seek Busy signal going low (at TP3). Adjust R115 for elapsed time of 10 msec.

4.5.13.4 Related Adjustments

- None.

4.5.14 READ DATA SEPARATOR (SINGLE DENSITY OPERATION ONLY) (FD5X1 ONLY)

The Read Data Separator Single-Shot timing signal is set by adjusting potentiometer R25.

4.5.14.1 Test Configuration

(1) Apply the necessary power and control to position the carriage at track 0.

(2) Insert a work diskette into the drive and close the loading door.

(3) Load the magnetic head.

(4) Write an all-ones pattern on the diskette, then Read the pattern.

(5) Set the horizontal time base on the oscilloscope to 1 μsec per division.

(6) Using the test probes of the oscilloscope, observe the signal at the Read Data Separator Single-Shot, U5, at TP1. Place the ground clip of the signal probe at TP17. Sync the oscilloscope on the leading edge of Read Data (RDA) signal (at TP6). Place the ground clip of the signal probe at TP17.

4.5.14.2 Test Procedure

(1) Measure the time from the Read Data Signal going high (at TP6) to the Read Data Separator Single-Shot signal going low (at TP1).

(2) Time elapsed should be 3 μsec.

4.5.14.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 4.5.14.1.

(2) Measure the time from Read Data signal going high (at TP6) to Read Data Separator Single-Shot going low (at TP1). Adjust potentiometer R25 for an elapsed time of 3 μsec.

4.5.14.4 Related Adjustments

- None.

4.5.15 DRIVE MOTOR SPEED ADJUSTMENTS (FOR FD400 ONLY)

The running speed and starting speed of the drive motor are adjusted by potentiometers R97 and R98, respectively. The drive motor running speed must be adjusted first because it affects the drive motor starting speed. Correct setting of the starting speed is required to ensure proper motor starting.

4.5.15.1 Test Configuration

(1) Install a work diskette in the drive and close the loading door.

(2) Apply the necessary power and control to turn the drive motor on. Load the magnetic head.

(3) Connect a timer (Monsanto Counter Timer Model 100B, or equivalent) to the output of the Drive Motor Oscillator, U12, at TP3 on the PCBA. Place the ground clip of the signal probe as established in Paragraph 4.5.1.1.

4.5.15.2 Test Procedure

(1) Using the counter-timer, observe the period of the Drive Motor Oscillator, U12, at TP3 on the PCBA.

NOTE

The measurement can be performed with the DRIVE MOTOR ON interface line either true or false.

(2) Acceptable Limits (Run Speed, DRIVE MOTOR ON Interface Line, True)

- 2.34 milliseconds (maximum)
- 2.28 milliseconds (minimum)

(3) With the counter-timer connected as in Step (1), rapidly cycle the DRIVE MOTOR ON interface line from true to false, approximately twice per second. Measure the period of the oscillator.

(4) Acceptable Limits (Start Speed)

- 9.7 milliseconds (maximum)
- 9.3 milliseconds (minimum)

4.5.15.3 Adjustment Procedure

If the acceptable limits are exceeded, the following adjustments must be performed.

(1) Establish the test configuration described in Paragraph 4.5.10.1.

(2) With the DRIVE MOTOR ON interface line false (or door open), adjust R98 on the PCBA until the period of the oscillator waveform measured at TP3 is 2.31 milliseconds.

(3) Ensure that the drive loading door is closed. Cycle the DRIVE MOTOR ON interface line rapidly from true to false, approximately twice per second.

(4) Adjust R97 for an oscillator period of 9.50 milliseconds.

4.5.15.4 Related Adjustments

- None.

SECTION V
PARTS REPLACEMENT

5.1 INTRODUCTION

Replacement of mechanical and electrical components in the Flexible Disk Drive is relatively simple and requires only common hand tools and a minimum number of special tools. Details for replacement of all electrical and mechanical assemblies are addressed in the following paragraphs.

5.1.1 The Printed Circuit Board Assembly (PCBA)

The single PCBA is held in the chassis by two tabs (on the PCBA) which mount through slots at the rear of the chassis, and two ¼-inch hex-head self-tapping screws which mount through the PCBA near the drive motor.

5.1.1.1 PCBA Removal

NOTE

Some models are equipped with an Auxiliary PCBA. The Auxiliary PCBA must be removed before removal of the PCBA is attempted. Refer to Paragraph 5.1.2 for details relating to removal of the Auxiliary PCBA.

(1) Remove the interface connector (P1), the 30-pin AMP connector (P2), and the head connector (P3). For the FD511 also remove the power cable (P7). For the FD5XX series, remove the door interconnect plug (P4) and the ac power cable plug (P6).

(2) Remove the two ¼-inch hex-head screws located adjacent to the drive motor.

(3) Remove the PCBA from the chassis.

5.1.1.2 PCBA Installation

(1) Locate the PCBA tabs in the slots provided at the rear of the chassis and lower the PCBA into the drive.

(2) Install relevant connectors (P2, P3, P4, P6, and P7).

(3) Align the PCBA; replace and tighten the two mounting screws.

5.1.1.3 Related Adjustments

The following adjustments must be made subsequent to replacing the PCBA.

(1) Read Amplifier Gain (Paragraph 4.5.2.2).

(2) Drive Motor Speed (Paragraph 4.5.1.5) (FD400 only).

(3) Step Motor Timing (Paragraph 4.5.3).

(4) Erase Delay (Paragraph 4.5.12 for FD5X0 and FD5X1; Paragraph 4.5.11 for FD400).

(5) For Basic IIA PCBA (FD5XX only)

- Seek Busy (Paragraph 4.5.13)
- Read Data Separator One-Shot (Paragraph 4.5.14)

5.1.2 AUXILIARY PCBA

The Auxiliary PCBA is an option and not included with every drive. This PCBA is secured to the chassis with captive hardware located on either side of the interface connector J1, and with a bracket which attaches to one side of the chassis. A view of this PCBA is shown in Figure 5-1. It should be noted that some versions of Auxiliary PCBAs have 50-wire flat interface cables attached.

5.1.2.1 Removal

(1) If the Auxiliary PCBA is equipped with a 50-wire flat interface cable, loosen the two captive screws which secure the cable strain relief bar (and insulator) to the PCBA. These captive screws also secure the Auxiliary PCBA to the mounting bracket.

(2) Free the interface cable from the strain relief bar. Note that the relief bar is slotted at one end and can be pivoted.

(3) Remove the 50-wire interface cable (if so equipped) and the power cable from the Auxiliary PCBA.

(4) Loosen the two captive mounting screws located on each side of the drive interface connector J1.

(5) When the two captive screws which were loosened in Step (1) are totally disengaged, the Auxiliary PCBA can be freed from its mounting bracket.

(6) Disengage the Auxiliary PCBA from J1 on the chassis.

5.1.2.2 Installation

(1) Engage the Auxiliary PCBA and interface connector J1 at the rear of the chassis.

(2) Tighten the two mounting screws on either side of interface connector J1.

(3) Install the power cable connector and the 50-pin flat cable connector, if so equipped. Observe proper connector keying.

(4) Fold the 50-wire flat cable over the insulator on the strain relief. Swing the clamp bar up under the upper retaining screw, if so equipped.

(5) Tighten the two screws on the side of the Auxiliary PCBA into the mounting bracket behind this PCBA. This will also tighten the strain relief clamps onto the 50-wire flat cable.

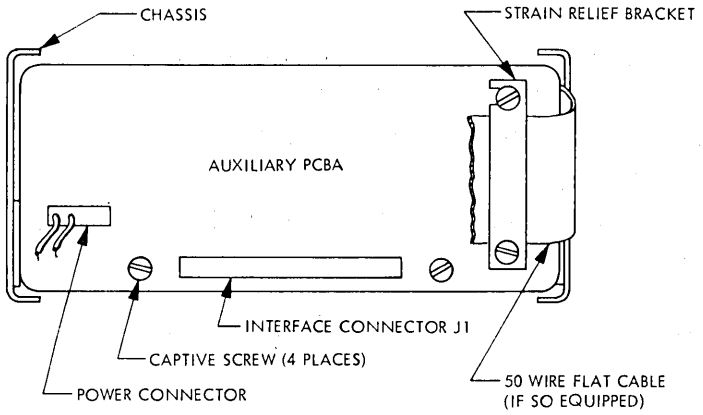


Figure 5-1. Auxiliary PCBA Installation

5.1.3 TRACK-0 SWITCH ASSEMBLY

The track-0 switch is located on the top surface of the chassis beside the stepper motor. In the event that the switch fails, both the switch and the bracket should be replaced as a unit and the switch adjusted to activate between tracks 0 and 1.

5.1.3.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the plastic tie wraps from the harness which connects the three wires from the track-0 switch assembly to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps and the wire routing.

(3) Using an AMP extractor tool, remove the track-0 switch pins from connector P2. Note color code and pin numbers.

(4) Remove the track-0 switch, bracket, and associated hardware by removing the two hex-head retaining screws. Retain this hardware.

5.1.3.2 Installation

(1) Position the replacement switch assembly and secure lightly with the hardware retained in Paragraph 5.1.3.1 Step (4). Route the wires through the grommet in the chassis adjacent to the track-0 switch assembly.

(2) Insert wire terminating pins in P2 according to pin numbers and color code noted during removal of the assembly.

(3) Route the wires, replace the tie wraps.

(4) Install the PCBA as described in Paragraph 5.1.1.

(5) Perform the adjustment procedure detailed in Paragraph 4.5.7.

5.1.4 HEAD LOAD SOLENOID

The head load solenoid is located on the top surface of the chassis adjacent to the platen.

5.1.4.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the plastic tie wraps on the wiring harness which connect the two wires from the head load solenoid to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps and wire routing.

(3) Using an AMP extractor tool, remove the head load solenoid pins from connector P2. Note color code and pin numbers.

(4) Remove the Phillips head screw and washer which secures the solenoid to the chassis on the underside of the machine. Refer to Figure 4-1 for location. Retain the mounting hardware.

(5) Remove the solenoid. Carefully pull the connecting wiring through the grommet in the chassis.

5.1.4.2 Installation

(1) Carefully route the connecting wires of the replacement head load solenoid down through the grommet in the chassis and locate the solenoid in the alignment hole. Refer to Figure 4-1 for location.

(2) Position the replacement solenoid and insert the Phillips head mounting screw and washer; tighten to 16 +2 in-lb. Ensure that the solenoid remains properly seated in the alignment hole during this operation.

(3) Insert the wire terminating pins in P2 according to pin numbers and color code noted during removal of the solenoid.

(4) Route the wires and replace the tie wraps.

(5) Install the PCBA as detailed in Paragraph 5.1.1.

(6) Perform the Head Load Solenoid adjustment procedure as described in Paragraph 4.5.4.

5.1.5 WRITE PROTECT ASSEMBLY (OPTIONAL)

The optional write protect assembly is located adjacent to the head load solenoid. Failure of the device requires that the complete assembly be replaced.

5.1.5.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the tie wraps on the harness connecting the write protect assembly to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps and wire routing.

(3) Using an AMP extractor tool, remove the write protect pins from connector P2. Note color code and pin numbers.

(4) Remove the two hex-head write protect assembly mounting screws. Retain this hardware. Note the position of the disk acceptance slot on the assembly.

(5) Carefully pull the connecting wiring through the grommet in the chassis.

(6) Remove the write protect assembly.

5.1.5.2 Installation

(1) Carefully route connecting wires of the replacement write protect assembly down through the grommet in the chassis.

(2) Mount the replacement write protect assembly on the chassis with the disk acceptance slot facing forward, i.e., towards the door.

(3) Carefully tighten the hex-head retaining screws while holding the write protect assembly with the disk acceptance slot parallel to the door.

(4) Reroute the wires and replace the tie wraps.

(5) Insert wire terminating pins in P2 according to pin numbers and color code noted during removal of the assembly.

(6) Install the PCBA as detailed in Paragraph 5.1.1.

5.1.6 LED ASSEMBLY

The LED assembly is mounted to the underside of the beam clamp assembly directly in front of the drive hub.

5.1.6.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the plastic tie wraps from the cable harness connecting the LED assembly to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps and wire routing.

(3) Remove the LED terminals from connector P2. Note color code and pin numbers.

(4) Remove tie wraps on beam clamp and shaft noting the approximate locations. Carefully pull the connecting wires up through the chassis grommet and through hole in card guide.

(5) Remove and retain the two LED mounting block screws. Remove the assembly.

5.1.6.2 Installation

(1) Mount the replacement LED assembly from the underside of the beam clamp with the chamfer on the mounting block facing the door. Refer to Figure 5-2.

(2) Secure the two mounting screws to 4 to 6 in-lb.

(3) Route the connecting wires across the shaft and down the outside of the card guide, i.e., between the chassis side and the card guide and through the hole in the card guide.

(4) Route the connecting wires through the grommet in the chassis. Ensure that the wires do not interfere with the diskette when a diskette is installed in the drive.

(5) Insert wire terminating pins in connector P2 according to pin numbers and color code noted during removal of the assembly.

(6) Replace the tie wraps.

(7) Install the PCBA as detailed in Paragraph 5.1.1.

(8) Check the Index Sensor alignment and adjust if required (see Paragraph 4.5.6).

5.1.7 PHOTO-TRANSISTOR ASSEMBLY

The photo-transistor assembly is located on a bracket on the front of the chassis base plate (directly beneath the LED assembly). In the event of a failure, the photo-transistor must be replaced. Reference Figure 5-2.

5.1.7.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the plastic tie wraps on the wiring harness connecting the photo-transistor assembly to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps.

(3) Using an AMP extractor tool, remove the photo-transistor pins from P2. Note color code and pin numbers.

(4) Remove the bracket mounting screws. Remove the photo-transistor bracket from the base plate. Refer to Figure 5-1 for location of the mounting screws. Retain the mounting hardware.

(5) Carefully pull the photo-transistor wires up through the grommet in the chassis.

(6) Remove photo-transistor assembly from mounting bracket; retain hardware.

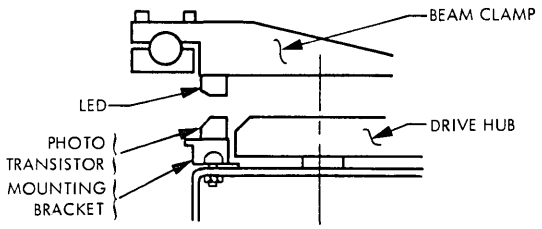


Figure 5-2. LED Assembly Placement (Side View)

5.1.7.2 Installation

(1) Mount photo-transistor assembly to bracket with chamfer towards the loading door.

(2) Carefully route the connecting wires of the replacement photo-transistor assembly down through the grommet.

(3) Install the photo-transistor bracket on the chassis as shown in Figure 5-2. Tighten the bracket mounting screws finger tight.

(4) Insert wire terminating pins in connector P2 according to pin number and color code noted during removal of the assembly.

(5) Route the wires and replace the tie wraps. Ensure that the wires clear the loading door mechanism during opening and closing.

(6) Install the PCBA as detailed in Paragraph 5.1.1.

(7) Perform the Index Sensor alignment procedure detailed in Paragraph 4.5.6.

5.1.8 DOOR OPEN/CLOSED SWITCH

The switch which senses the condition of the loading door, i.e., open or closed, is located on a bracket secured to the door pivot bracket.

5.1.8.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) Remove the plastic tie wraps on the wiring harness which connects the door open/closed switch to the 30-pin AMP connector (P2). Note approximate locations of the tie wraps.

(3) Using an AMP extractor tool, remove the door open/closed pins from connector P2. Note color code and pin numbers.

(4) Remove and retain the two mounting screws located on the switch. Refer to Figure 5-3 for location.

(5) Remove the switch assembly by carefully pulling wires through grommets on the bracket and chassis.

5.1.8.2 Replacement

(1) Install the replacement switch on the bracket. (See Figure 5-3.)

(2) Secure the switch with the two mounting screws, assuring that the switch lever is under the lip on the bezel.

(3) Carefully route the connecting wires down through the grommets in the chassis and bracket.

(4) Insert wire terminating pins in connector P2 according to pin numbers and color code noted during removal of the assembly.

(5) Replace the tie wraps.

(6) Check the operation of the switch by opening and closing the door and observing that the lever operates against the bezel.

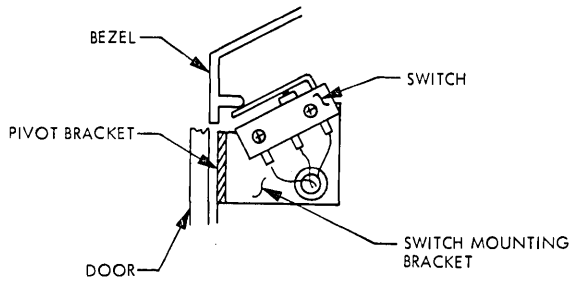


Figure 5-3. Door Open/Closed Switch Placement

5.1.9 BEZEL

The standard flexible disk drive is equipped with a cartridge eject system. If it is necessary to replace the bezel on a machine, the card stop (located on the front of the bezel) must be adjusted after bezel replacement.

5.1.9.1 Removal

(1) Open the diskette loading door.

(2) Remove the four bezel mounting screws (2 each side) located on the bezel sides.

(3) Pull the bezel outward, at the same time tilting it upward, around the door.

5.1.9.2 Installation

(1) With the loading door open, rotate the replacement bezel around the door and push the bezel onto the chassis, being careful not to damage the door open/close switch.

(2) Secure the bezel with the four mounting screws (2 each side) located on the bezel sides.

NOTE

It may be necessary to re-attach the door bottom spring in the event it becomes detached while replacing the bezel.

NOTE

Align the diskette stop as detailed in Paragraph 5.1.10.3.

5.1.10 CARTRIDGE-EJECT SYSTEM

The disk drive is supplied with either a cartridge-ejection-block type system or torsional cartridge-ejection-spring type system. Paragraph 5.1.10.1 describes the cartridge-ejection-block spring replacement; Paragraph 5.1.10.2 describes the torsional cartridge-ejection-spring replacement.

5.1.10.1 Cartridge-Ejection-Block Spring Replacement

The cartridge-ejection-block system is located on the right side of the chassis attached to the right cartridge guide rail. The system consists of a fixed mounting block, movable cartridge-ejection block, ejection spring, guide shaft, and an adjustable cartridge stop on the front of the bezel.

One end of the ejection spring is attached to a screw located on the mounting block (attached to the right cartridge guide rail); the other end is hooked to a screw in the movable cartridge eject block. Replacement of the spring is as follows.

(1) Remove each end of the ejection spring from its mounting point.

(2) Install the replacement spring by attaching one end to the screw located on the mounting block and the other end to the screw in the cartridge-eject block.

5.1.10.2 Torsional Cartridge-Ejection Spring Replacement

The torsional cartridge-ejection spring is located on the left side of the chassis adjacent to the left cartridge guide rail. The ejection system consists of a vertical spring mounted on a keyed, two-part plastic retainer. This system is held to the top surface of the chassis by a ¼-inch hex-head self-tapping screw.

The ejection spring is held captive between each end of the two spring retainers which mate and are *keyed together* to assemble in only one position. A pin projects from the bottom of the lower spring retainer and mates with a locating hole in the chassis. Replacement of the spring and spring retainers is as follows:

(1) Note the relative positions of the upper and lower spring retainers.

(2) Remove the ¼-inch hex-head mounting screw and pull the eject system free of the chassis. The spring retainers can now be pulled apart, releasing the ejection spring.

(3) Install the new spring between the spring retainers (making sure the longer spring arm will be furthest from the chassis) and ensure that the spring retainers key and mate together properly.

(4) Hold the spring retainers (with the spring in between them) together between the thumb and forefinger of one hand. With the other hand, hold both ends of the ejection spring together and force them over the stop pins projecting inward from the spring retainers.

(5) Release the ends of the ejection spring. The ends should exert pressure outwards against the pins that project from the spring retainers. Pressure from the ejection spring should now hold the spring retainers lightly together as a unit.

(6) Mount the ejection spring and spring retainers unit on the chassis. Ensure that the locating pin on the lower spring retainer mates with the proper hole in the chassis as the hex-head mounting screw is tightened.

5.1.10.3 Diskette-Stop Replacement

(1) Close loading door and turn disk drive upside down.

(2) Remove the Allen-head retaining screw (with a ball-type Allen wrench) from the diskette stop on back of the bezel.

(3) Open loading door and remove the diskette stop from the bezel; retain the screw.

(4) Attach the new diskette stop to the bezel and secure lightly with the screw.

(5) Install the diskette-stop alignment tool (PERTEC Part No. 601060-01) through the top of the drive. Ensure that the circular projection fits into the drive hub.

(6) Push the diskette stop until it contacts the edge of the adjustment tool. Hold the stop firmly and squarely against the tool. Tighten the holding screw. Refer to Figure 5-4.

(7) Remove the alignment tool.

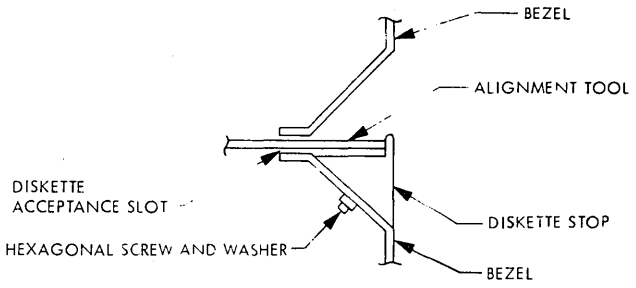


Figure 5-4. Diskette Stop Placement (Side View)

5.1.11 HEAD LOAD PAD

5.1.11.1 Head Load Pad Replacement

The head load pad must be replaced when it loses its nap, or becomes impregnated with an excessive amount of iron oxide from the disk.

NOTE

The magnetic head must be cleaned after the head pad is replaced.

(1) Remove the plastic screw which holds the pad button to the load arm. Raise the spring-loaded head-load arm, and remove button.

CAUTION

DO NOT TOUCH THE NAP SURFACE OF THE PAD WITH YOUR FINGERS. ACIDS EMITTED FROM SKIN CAN BE TRANSFERRED TO THE LOAD PAD, THEN TO THE MAGNETIC HEAD, CAUSING PERMANENT DAMAGE TO THE HEAD.

(2) Place the replacement load pad button in the recess in the load arm; the button is keyed to the load arm. Replace the plastic screw.

(3) Clean the magnetic head as detailed in Paragraph 4.3.1.

(4) Perform the Compliance Check as detailed in Paragraph 5.1.11.2.

5.1.11.2 Compliance Check

(1) Load a work diskette in the drive, apply power, and load the magnetic head.

(2) Write an all-ones pattern at track 0.

(3) Set the oscilloscope time base to 20 msec per division.

(4) Attach the signal probes of the oscilloscope to TP4 and TP5 on the PCBA. Ajust the oscilloscope to read differentially (A + B with B inverted).

(5) Apply a 15 gm load with an appropriate gram gauge to the load arm directly over the load pad. Should the signal level observed on the oscilloscope increase by more than 10 percent, the disk drive is said to have poor compliance.

(6) Should the results of Step (5) indicate poor compliance, replace the pad as described in Paragraph 5.1.11.1.

5.1.12 STEPPER MOTOR ASSEMBLY

When the stepper motor is replaced, the head carriage assembly must also be removed and reinstalled.

5.1.12.1 Removal

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) From beneath the chassis, remove the stepper motor wires from the cable clamps — note wire routing.

(3) Remove the plastic tie wraps from the cable harness connecting the stepper motor to the 30-pin AMP connector (P2). Note the approximate locations of the tie wraps.

(4) Remove the stepper motor wire terminals from connector P2. Note the color code and pin numbers.

(5) Remove and retain the four stepper motor mounting screws — note hex-heads are front mounted and Phillips-head screws, with fiber washers, are rear mounted.

(6) Remove the head carriage assembly from the stepper motor shaft as detailed in Paragraph 5.1.13.1.

(7) Remove the stepper motor assembly from the chassis.

5.1.12.2 Installation

(1) Install the head carriage assembly onto the shaft of the replacement stepper motor as detailed in Paragraph 5.1.13.2.

(2) Route the wires from the stepper motor through the stepper motor mounting hole in the chassis and install the stepper motor in its guide slot.

(3) Install the stepper motor mounting screws and washers; tighten to finger tight.

CAUTION

TAKE CARE TO GUIDE HEAD CARRIAGE ASSEMBLY AROUND THE PLATEN, TRACK-0 SWITCH, AND SOLENOID LOAD SCREW. ENSURE THAT THE HEAD LOAD ARM IS ON TOP OF THE PLATEN LOAD SPRING.

(4) Insert the stepper motor terminating pins in P2 according to pin numbers and color code noted during removal of the assembly.

(5) Replace the tie wraps and route the wire through the cable clamps.

(6) Route the head cable in front of the head load solenoid and attach the tie wrap and route wires under cable clamp.

(7) Route the head cable down through the opening in the chassis. Assure that cable does not interfere with the drive pulley.

(8) Install the PCBA as detailed in Paragraph 5.1.1.

(9) Plug the 30-pin AMP connector and head cable to J2 and J3, respectively, on the PCBA.

(10) Perform the CE Alignment procedure described in Paragraph 4.5.5.

(11) Check the Track-0 Switch adjustment (Paragraph 4.5.7) and set the Track-0 Stop Paragraph 4.5.8).

5.1.13 HEAD CARRIAGE ASSEMBLY

When it is necessary to replace the head carriage assembly, the stepper motor must be removed from the chassis and both front and rear stops on the stepper motor shaft adjusted.

5.1.13.1 Removal

(1) Remove the head cable tie located on the chassis top.

(2) Unplug the head from the PCBA (J3) and push the cable and plug up through the hole in the chassis; slide the cable out from under the cable clamp.

(3) Remove the stepper motor from the chassis as detailed in Paragraph 5.1.12.1 but do not disconnect the stepper motor wires.

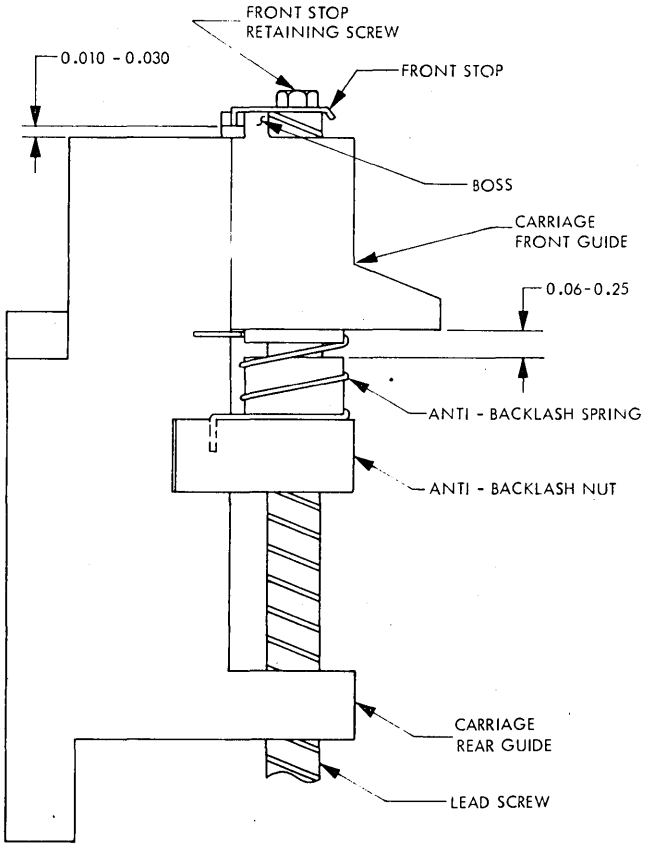
(4) Rotate the stepper motor so that the stepper motor shaft and the head carriage assembly are perpendicular to the chassis, i.e., vertical.

(5) Protect the short end of the stepper motor shaft (rear of the stepper motor) with a soft cloth.

(6) Fit a suitable wrench on the hex-head front stop retaining screw. See Figure 5-5.

(7) Grip the cloth-protected shaft with pliers and remove the front stop by rotating the hex-head retaining screw while holding the shaft.

(8) Rotate the shaft and remove the head carriage, anti-backlash nut and spring.



NOTES: 1. ALL DIMENSIONS IN INCHES
2. VIEW FROM BOTTOM OF DEVICE

Figure 5-5. Head Carriage Assembly Placement

5.1.13.2 Installation

(1) With the stepper motor shaft perpendicular to the chassis, rotate the shaft and thread the rear guide of the replacement carriage onto the stepper motor shaft.

(2) Thread the anti-backlash nut onto the shaft and install the anti-backlash spring. Carefully thread the carriage front guide onto the shaft and set the distance between the anti-backlash nut and carriage to 0.06- to 0.25-inch as shown in Figure 5-5. Rotate the shaft until the carriage assembly has moved well down the shaft.

(3) Orient and install the front stop as shown in Figure 5-5 using the hex-head retaining screw. Use Loctite Grade C adhesive on the screw.

(4) Install the stepper motor to the chassis as detailed in Paragraph 5.1.12.2.

(5) Route head cable, replace the tie wrap, plug the cable into J3.

(6) Perform the Read Amplifier Gain procedure detailed in Paragraph 4.5.2.

(7) Set the head load time per Paragraph 4.5.4.

5.1.14 CARTRIDGE GUIDE

The cartridge guides are used to support the outer edges of the diskette when the diskette is installed in the machine. The following procedure is used to replace the cartridge guides.

(1) Remove the PCBA as detailed in Paragraph 5.1.1.

(2) When removing the cartridge guide opposite the head load solenoid, it is necessary to remove the door-return spring lug and a portion of the LED wiring. Remove the nut holding the door-return spring lug and pull the lug from the screw. The wires to the LED must be removed from connector P2 as detailed in Paragraph 5.1.6.1; however, it is not necessary to remove the tie wraps on the top side of the machine.

(3) From beneath the chassis, remove the cartridge guide mounting screws (2 each guide). Retain hardware.

(4) Remove guide.

(5) Replace guide and secure with hardware. Replace door spring lug and LED wiring as required.

(6) Install the PCBA as detailed in Paragraph 5.1.1.

5.1.15 CONE CLAMP ASSEMBLY

When the door is closed, the cone-clamp assembly locates and secures the diskette to the drive spindle.

(1) Open the loading door.

(2) Remove hardware which secures the cone clamp assembly to the support clamp. Retain hardware and crowned shaft.

(3) Install cone clamp assembly to underside of support plate with crowned shaft in top of bearing; secure hardware.

(4) Check to determine that cone clamp rotates freely and enters the hub properly.

5.1.16 DOOR PIVOTS/LINKS/LEVERS/PIVOT BRACKET

Should any of the pivots, links, levers, or bracket fail, the complete door mechanism can be removed and replaced as follows with the defective component replaced.

(1) Remove bezel according to the steps in Paragraph 5.1.9.

(2) Remove door-open springs — note location of springs.

(3) Loosen socket head cap screws which secure the levers to the shaft.

(4) Reach inside chassis with an appropriate open-end wrench and grip onto pivots which secure the shaft. Remove Phillips-head screws in pivots — discard screws.

NOTE

Phillips-head screws are secured in place with Loctite Grade C adhesive.

(5) Remove the lower pivots in the same manner as in Step (4) — discard screws.

(6) Slide the shaft and door assembly forward and be careful not to damage any of the wires attached to the assembly.

(7) Disassemble the assembly to the point at which the defective part needs replacement.

(8) Replace the defective component and assemble the loading door mechanism loosely.

(9) Slide assembly back into chassis with pivots installed on shaft and into door pivot bracket; be careful not to damage wires.

(10) Replace Phillips-head screws in pivots using Loctite Grade C adhesive.

(11) Replace bezel according to the steps in Paragraph 5.1.9.

(12) Firmly push levers towards each side of the chassis and secure the socket head cap screws. Torque to 16 ±2 in-lb. No side play of shaft/level/beam clamp system is permitted.

(13) Replace springs on loading door mechanism.

(14) Adjust beam clamp assembly according to the steps in Paragraph 4.5.9.

(15) On FD5XX only, adjust door open solenoid according to Paragraph 4.5.11.

5.1.17 DOOR-OPEN STOP

The door-open stop is a rubber grommet located on a standoff attached to the front flange of the chassis base plate. Use the following steps to remove and replace the door-open stop.

(1) Close loading door and reach from underside of chassis and remove the grommet from the standoff.

(2) Replace by firmly pushing grommet onto standoff.

5.1.18 DOOR LATCH SOLENOID ASSEMBLY REPLACEMENT

The Door Latch Solenoid Assembly is mounted behind the loading door and is attached to the chassis. It is accessed from the underside of the drive.

5.1.18.1 Removal

(1) Observe wire routing and locations of tie wraps for the door latch wiring.

(2) Remove tie wraps on door latch wiring. Remove the pins to the door latch wiring from connector P4. Carefully draw the wires through the grommet in the chassis.

(3) Remove the two ¼-inch hex-head screws which secure the door latch assembly to the chassis. Remove the assembly.

5.1.18.2 Installation

(1) Attach the replacement door latch assembly to the chassis. Tighten the attachment hardware finger tight. Ensure that the shield is in its original position.

(2) Adjust the door latch solenoid according to the steps in Paragraph 4.5.10.

(3) Route the door latch solenoid wires to P4. Replace the tie wraps. Ensure that no wiring interferes with door movement.

5.1.19 BEAM CLAMP REPLACEMENT

The beam clamp is mounted on the horizontal shaft immediately behind the top of the bezel and is accessed from the top of the drive.

5.1.19.1 Removal

(1) Loosen the 4 socket-head set screws which hold the beam clamp to the shaft. Loosen the ¼-inch hex-head screws which hold the platen spring to the left side of the beam clamp.

(2) Move the platen spring horizontally from under the load arm. Rotate the beam clamp, and its attached components, into a vertical position.

(3) All components attached to the beam clamp (LED Assembly, platen load spring, photo-transistor assembly, support plate, cone assembly, and door-open switch) can now be removed, after noting their positions.

(4) The beam clamp can now be freed from the shaft by further loosening and moving the four socket-head set screws mentioned in Step (1). Retain all beam clamp attachment hardware.

5.1.19.2 Installation

(1) Assemble the support plate, cone assembly, and platen load spring to the beam clamp. Do not fully tighten the platen spring screws. Ensure that the support plate slides freely on the underside of the beam clamp.

(2) Assemble the beam clamp to the shaft using the cap clamps, square nuts and socket head set screws. Tighten the socket head set screws finger tight.

(3) Replace the components removed in 5.1.19.1 Step (3). Ensure that the wiring does not interfere with diskette insertion.

(4) Lower the beam clamp into operating position, i.e., insert the cone assembly into the drive hub. Ensure that the platen spring rests under the load arm.

(5) Perform the beam clamp adjustment according to the steps in Paragraph 4.5.9.

(6) Adjust the platen load spring according to Steps (8) through (13) in Paragraph 4.5.4.2.

(7) Adjust the index sensor, according to the steps in Paragraph 4.5.6.

5.1.20 DRIVE MOTOR ASSEMBLY REPLACEMENT (FD400)

The drive motor assembly is located at the front of the disk drive. The mounting nuts are accessed from the top of the chassis and the assembly is removed from the underside of the chassis.

5.1.20.1 Removal

(1) Remove all power from the disk drive.

(2) Remove the PCBA according to the steps in Paragraph 5.1.1.

(3) Note the color coding, wire routing, location of cable clamps and tie wraps on the drive motor wiring. Remove the tie wraps restraining these wires.

(4) Remove the drive motor wire pins from connector P2.

(5) Place the disk drive on its side, remove the four hex nuts and washers from the mounting bolts that hold the motor to the chassis. (The front two bolts also hold the sensor assembly to the chassis.)

(6) Carefully pull the drive motor assembly and four mounting bolts off the chassis. Note the position of the two flat metal motor spacers as the drive motor is removed. Also note that the sensor assembly bracket will remain in place as the motor and mounting bolts are removed.

5.1.20.2 Installation

(1) Position the replacement motor assembly so that the motor leads are in their original positions (as noted in Paragraph 5.1.20.1 Step (3)). Insert mounting bolts through the bottom of the motor assembly and install the two flat metal spacers. Carefully guide the assembly into the four mounting holes provided on the chassis.

(2) Position the motor firmly against the spacers.

CAUTION

ENSURE THAT NONE OF THE MOTOR LEADS ARE PINCHED BETWEEN THE MOTOR AND SPACERS, OR BETWEEN THE SPACERS AND CHASSIS.

(3) Replace the four mounting nuts removed in Paragraph 5.1.20.1 Step (5). Make these finger tight. Inspect the installation for proper wire routing.

(4) Fully tighten the four motor mounting bolts from the underside of the disk drive.

(5) Route the motor leads, replace the cable clamps and tie wraps.

(6) Replace the PCBA according to the steps in Paragraph 5.11.2.

(7) Perform the beam clamp adjustment according to the steps in Paragraph 4.5.9.

(8) Perform the CE Alignment and Index Sensor Alignment according to the steps in Paragraphs 4.5.5 and 4.5.6, respectively.

5.1.21 DRIVE MOTOR ASSEMBLY REPLACEMENT (FD5XX)

There are nine ac motor assembly variations composed of three basic motor frame styles. Replacement of any of the nine variations with another variation requires that the complete motor assembly, capacitor, and related hardware be replaced. See Figure 5-6 A,B,C for mounting variations between the different frame styles, and Table 5-1 for the applicable motor and its associated components.

5.1.21.1 Removal

(1) Remove power from the disk drive.

(2) Remove the PCBA as detailed in Paragraph 5.1.1.

(3) Remove the capacitor housing located on the top side of the chassis opposite the drive motor. Note wire routing, color code, and the location of cable clamps and tie wraps.

(4) Remove the drive belt by first slipping if off of the large pulley and then off of the small pulley, on the underside of the disk drive.

(5) Remove the tie wraps holding the motor wires. Disconnect these wires from the terminals on connector J2 and carefully thread them through the grommet(s) in the chassis.

(6) The drive motor, pulley, and adaptor plate can now be removed as a unit.

5.1.21.2 Installation

(1) Note the name plate and/or part number of the replacement drive motor assembly to ensure that the assembly is correct for the voltage and frequency to be used (refer to Table 5-1).

(2) Study the appropriate illustration (Figure 5-6A,B,C) to establish the mounting adaptor plate and pulley for the replacement motor assembly.

(3) Assemble the adaptor plate and pulley to the motor. See Figure 5-6A,B,C, as necessary.

(4) Install the motor assembly onto the chassis. Ensure that the motor is properly oriented (in the chassis) for the frame style used, as depicted in Figure 5-6A,B,C. Check motor mounting screws and pulley setscrew for tightness.

(5) Route the motor wires through the grommet(s) in the chassis.

(6) Refer to the schematics in Figure 5-6A,C,B for the motor type used and its associated capacitor(s), when reconnecting the wires to connector J2. Note that some motors (see Table 5-1) do not require capacitors.

(7) Replace cable clamps and tie wraps as required.

(8) Select and install the proper capacitor (see Table 5-1). Replace the capacitor housing removed in Step (3).

(9) Install the drive belt by first looping it around the small pulley and then slipping it around the large pulley.

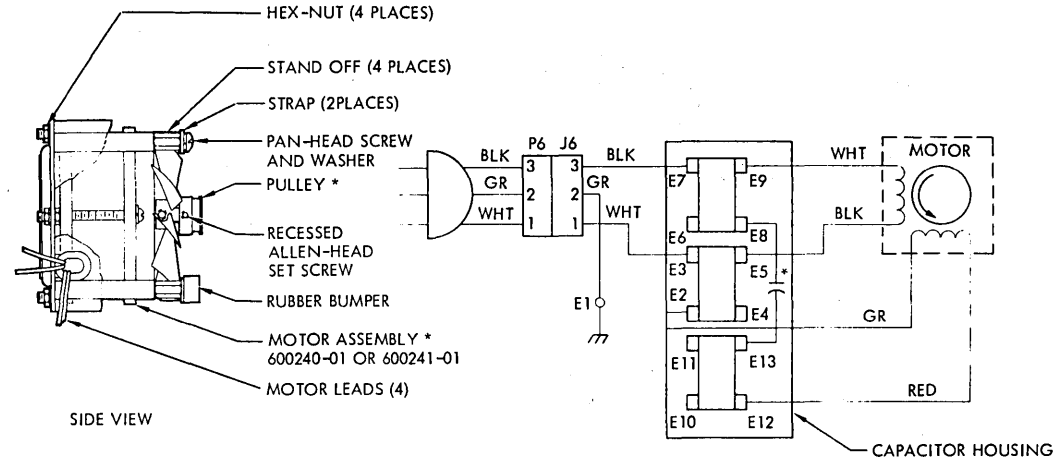
(10) Ensure that the motor spindle rotates freely in either direction. Also ensure that all wires are clear of the belt while the motor is running, and that the motor pulley does not rub against the motor housing.

(11) Replace the PCBA according to the steps in Paragraph 5.1.1.2. Note that a rubber tipped standoff is used to prevent the PCBA from hitting the motor pulley.

(12) Ensure that the motor pulley and drive belt run clear of the PCBA.

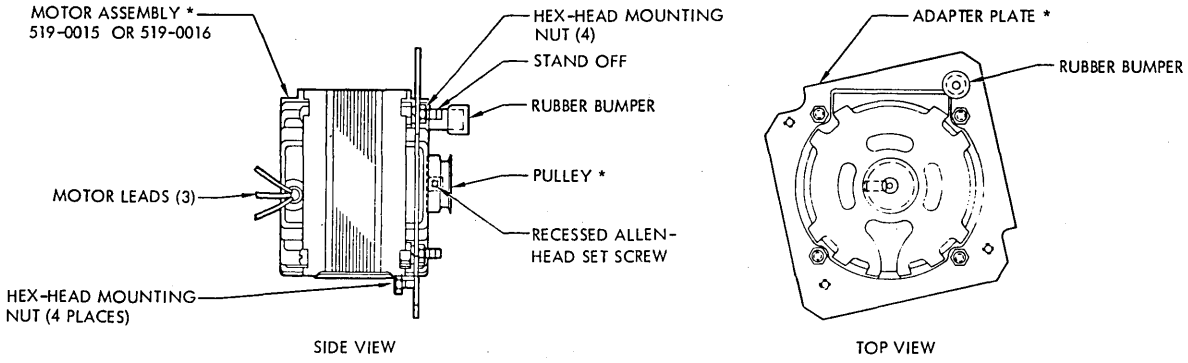
5.1.22 PLATEN LOAD SPRING REPLACEMENT

Replacement of the platen load spring is accomplished in accordance with the steps in Paragraph 5.1.19, beam clamp replacement.



* REFER TO TABLE 5-1 FOR COMPONENT VALUES

Figure 5-6A. AC Drive Motor, IMC Type



* REFER TO TABLE 5-1 FOR COMPONENT VALUES

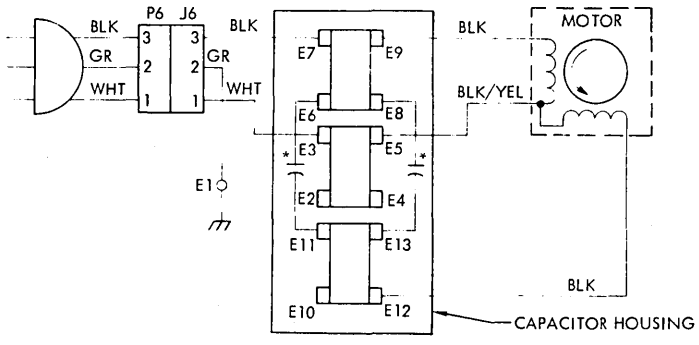
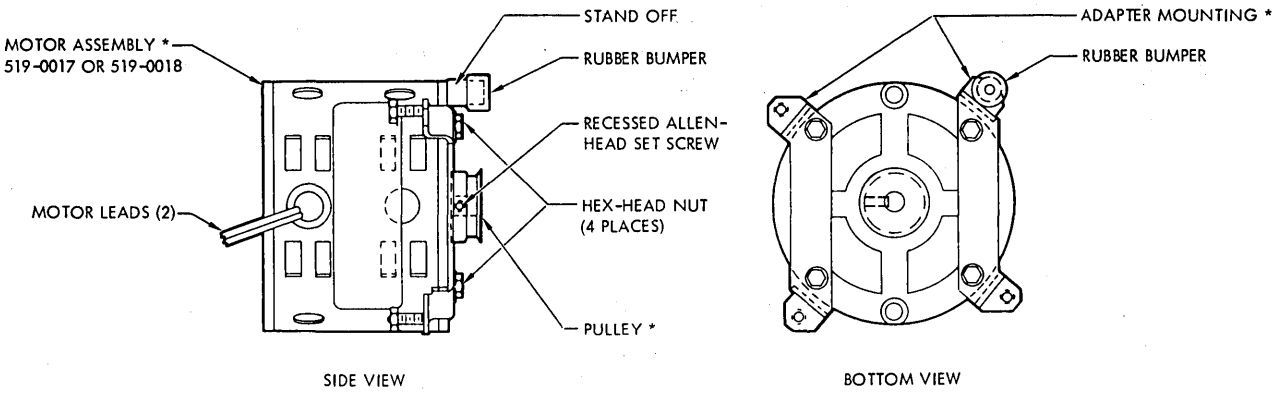


Figure 5-6B. AC Drive Motor, Bodine Type



* REFER TO TABLE 5-1 FOR COMPONENT VALUES

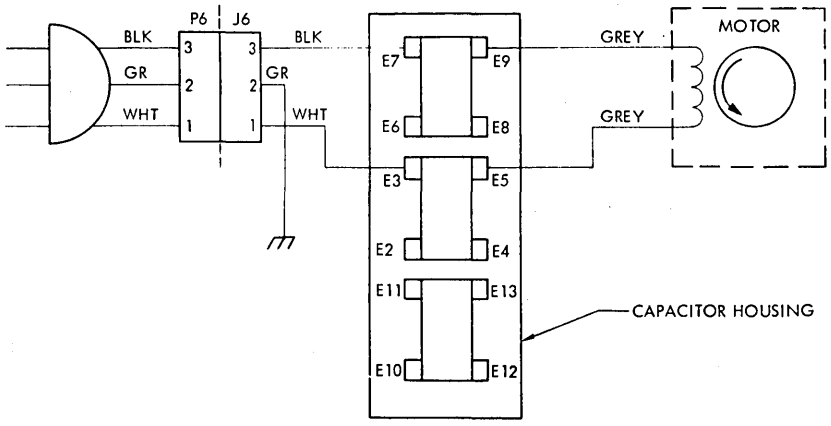


Figure 5-6C. AC Drive Motor, Robbins and Myers Type

Table 5-1
Drive Motor Replacement Matrix

AC Drive Motor	Source Voltage	Hz	Pulley	Capacitor Assembly	Adaptor Mounting Plate	Wiring Schematic on Figure
600240-01	115v	50/60	600325-01	2.0 µfd (1) 131-2050	None	5-6A
600241 -01	230v	50	600356-01	0.56 µfd (1) 131-5641	None	5-6A
600240-01	115v	50/60	600356-01	2.5 µfd (1) 131-2550	None	5-6A
519-0015	115v	50/60	600325-01	2.5 µfd (2) 131-2550	600004-01	5-6B
519-0016	230v	50	600356-01	2.5 µfd (1) 131-2551	600004-01	5-6B
519-0015	115v	50/60	600356-01	2.5 µfd (2) 131-2550	600004-01	5-6B
519-0017	115v	50/60	600045-01	None	600043-01	5-6C
519-0017	115v	50/60	600046-01	None	600043-01	5-6C
519-0018	230v	50	600046-01	None	600043-01	5-6C

TABLE I (1)

PART NUMBER	REFERENCE DESIGNATION
100-1015	R66, 84, 90
100-1025	R1, 16, 34, 46, 50 65, 85, 70
100-1035	R29, 33, 127 74, 75
100-1045	R59, 60
100-1055	R25
100-1215	R21
100-1515	R8, 10, 12, 14, 23, 36 38
100-1815	R120, 35
100-1825	R17,
100-2215	R26, 30, 78, 80, 83, 89
100-2225	R56, 57, 125, 132, 133
100-2235	R71, 72, 73
100-2715	R19,
100-2725	R86, 4, 122
100-2735	R61
100-4705	R20, 77
100-4715	R7, 64, 82, 88, 81, 87
100-4725	R91
100-4735	R27, 31
100-6805	R9, 11, 13, 15, 37, 39
100-6815	R58, 55
100-6825	R126, 129, 89, 49
100-8215	R18, 123
100-8225	R28, 32
101-1015	R68
101-1215	R5, 6, 67
101-1825	R53, 54
101-2225	R22
101-1525	R128
101-2725	R119
103-1015	R24, 121
104-1621	R47
104-2152	R3
120-0001	U18
121-2020	R76
121-2030	R2
130-1015	C26, 33
130-4705	C29
130-4715	C18
130-7515	C30
130-3315	C24

PART NUMBER	REFERENCE DESIGNATION
131-1030	C11, 12, 13, 14
131-1520	C 49
139-1020	C2
139-1055	C3, 25, 28, 47
139-2244	C1, 7, 8, 9, 20, 22, 27 31, 32
139-2262	C4
139-4751	C5, 34
139-4755	C21, 23, 19
139-4762	C6
200-1100	Q3, 4
200-1120	Q1, 2
200-4123	Q5, 6, 7, 28, 29, 31, 21, 22
200-4125	Q14, 16, 17, 18, 19, 20, 30
200-5321	Q8, 9
300-4002	CR1, 2, 3, 6, 7
300-4446	CR4, 5, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19
330-0515	VR3
330-0685	VR4
331-0335	VR2, 5
331-1605	VR1
400-0555	U13
400-0592	U1, 2
400-2741	U21, 27
515-1015	L1, 3, 5, 6
515-2405	L2, 4
700-4221	U17
700-7545	U25, 7
700-7400	U11
700-7402	U5, 8, 22, 23
700-7404	U15, 29
700-7406	U9, 24
700-7407	U6
700-7414	U20
700-7416	U30
700-7450	U28
700-7476	U4, 14
700-8020	U3

TABLE II (2)

			VERSION CHARACTERISTIC	C15, C16, R62, R63, U110, R131		WI	W2	W3	W4	W5	W6		W8	W9	R134, R135 R136, R137 Q32, C48	R79	
ASSEMBLY VERSION NO.				USAGE (3)		100-0005	100-0005	100-0005	100-0005	100-0005	100-0005		100-0005	100-0005	USAGE (3)	VALUE	PART NO.
SINGLE DENSITY	INTERNAL TRIM ERASE	-5V	-01	SINGLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	USE		USE	OMIT	USE	OMIT	OMIT	OMIT		USE	USE	OMIT	1K	100-1025
			-02	SINGLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE IN	USE		USE	OMIT	USE	OMIT	USE	USE		USE	USE	OMIT	1K	100-1025
		-12/-15V	-03	SINGLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	USE		OMIT	USE	USE	OMIT	OMIT	OMIT		USE	USE	OMIT	1K	100-1025
			-04	SINGLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	USE		OMIT	USE	USE	OMIT	USE	USE		USE	USE	OMIT	1K	100-1025
	EXTERNAL TRIM ERASE OPTION	-5V	-05	SINGLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	OMIT		USE	OMIT	OMIT	USE	OMIT	OMIT		USE	USE	OMIT	1K	100-1025
			-06	SINGLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE IN	OMIT		USE	OMIT	OMIT	USE	USE	USE		USE	USE	OMIT	1K	100-1025
		-12/-15V	-07	SINGLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	OMIT		OMIT	USE	OMIT	USE	OMIT	OMIT		USE	USE	OMIT	1K	100-1025
			-08	SINGLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	OMIT		OMIT	USE	OMIT	USE	USE	USE		USE	USE	OMIT	1K	100-1025
SINGLE/DOUBLE DENSITY	INTERNAL TRIM ERASE	-5V	-09	DOUBLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	USE		USE	OMIT	USE	OMIT	OMIT	OMIT		USE	USE	USE	2.2K	100-2225
			-10	DOUBLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE IN	USE		USE	OMIT	USE	OMIT	USE	USE		USE	USE	USE	2.2K	100-2225
		-12/-15V	-11	DOUBLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	USE		OMIT	USE	USE	OMIT	OMIT	OMIT		USE	USE	USE	2.2K	100-2225
			-12	DOUBLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	USE		OMIT	USE	USE	OMIT	USE	USE		USE	USE	USE	2.2K	100-2225
	EXTERNAL TRIM ERASE OPTION	-5V	-13	DOUBLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	OMIT		USE	OMIT	OMIT	USE	OMIT	OMIT		USE	USE	USE	2.2K	100-2225
			-14	DOUBLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE IN	OMIT		USE	OMIT	OMIT	USE	USE	USE		USE	USE	USE	2.2K	100-2225
		-12/-15V	-15	DOUBLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	OMIT		OMIT	USE	OMIT	USE	OMIT	OMIT		USE	USE	USE	2.2K	100-2225
			-16	DOUBLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	OMIT		OMIT	USE	OMIT	USE	USE	USE		USE	USE	USE	2.2K	100-2225

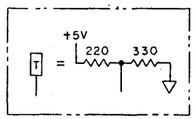


TABLE V
SPARES:

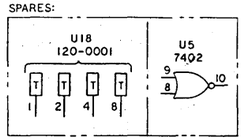


TABLE III (3)

PART NUMBER	REFERENCE DESIGNATION
104-2871	R62
139-1020	C15, 16
700-4221	U10
100-1525	R63
121-1830	R131
100-4725	R134
100-2745	R135
100-4745	R136
100-2225	R137
130-5615	C48
204-3993	Q32

REFERENCE DESIGNATIONS

LAST USED	NOT USED	DELETED
C49	C35 THRU C46	C10, 17
CR19		CR9
		F1
L6		
Q32	Q23 THRU Q27	Q10, 11, 12, 13, 15
R137	R92 THRU 118, 130, 124	R40, 41, 42, 43, 44, 45, 48, 51, 52
TP15		
U30	U12, 16, 19, 26	
VR5		
W9		W7

(12) VERSIONS OF THIS ASSEMBLY FOR INTERNAL/EXTERNAL TRIM ERASE MAY BE CREATED BY INSTALLING C15, C16, R62, R63, R131 AND SELECTING W3 OR W4 AS APPLICABLE.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.
10. DIODES ARE 1N4446.
9. PNP TRANSISTORS ARE 2N4125.
8. NPN TRANSISTORS ARE 2N4123.
7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.
6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
5. FOR SPARE LOGIC ELEMENTS, SEE TABLE V.
4. PIN 7 OF ALL I.C.s IS 0V. 7476 PIN 13 IS 0V 74221 PIN 8 is 0V
PIN 14 OF ALL I.C.s IS +5V. PIN 5 IS +5V PIN 16 IS +5V

(3) FOR PART NUMBER SEE TABLE III.

(2) FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

(1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS:
ASSEMBLY NO. 600251

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 200-FA PRE-PROD RELEASE	4/1/75	SOL		
B	ECN 30352A	11/5/75	RM		
C	ECN 30380	12/9/75	FFP		
	ECN 30530	1-2-76			
C1	ERN 200-GP PROD REL	2/19/76	RS		
D	ECN 30467	3-12-76	RJ		
E	ECN 30477	3-26-76	RJ		
F	ECN 30595	8-4-76	RJ		

600250 F

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± ANGULAR
.XXX ± 1/2°
X ±
X ±
BREAK ALL SHARP CORNERS APPROX. .010

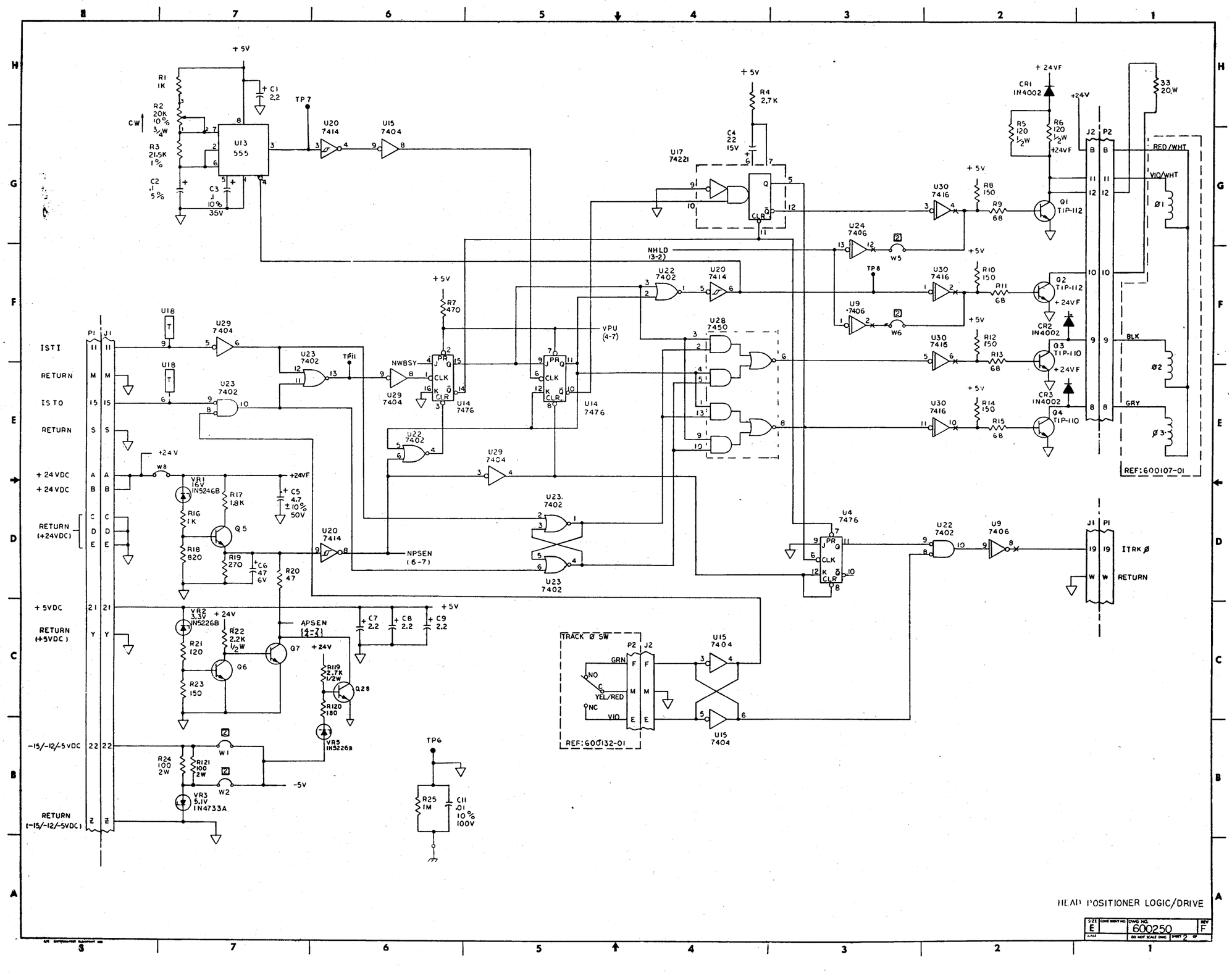
FINISH:
MATL:
NEXT ASSY | 1PT USED ON
APPLICATION

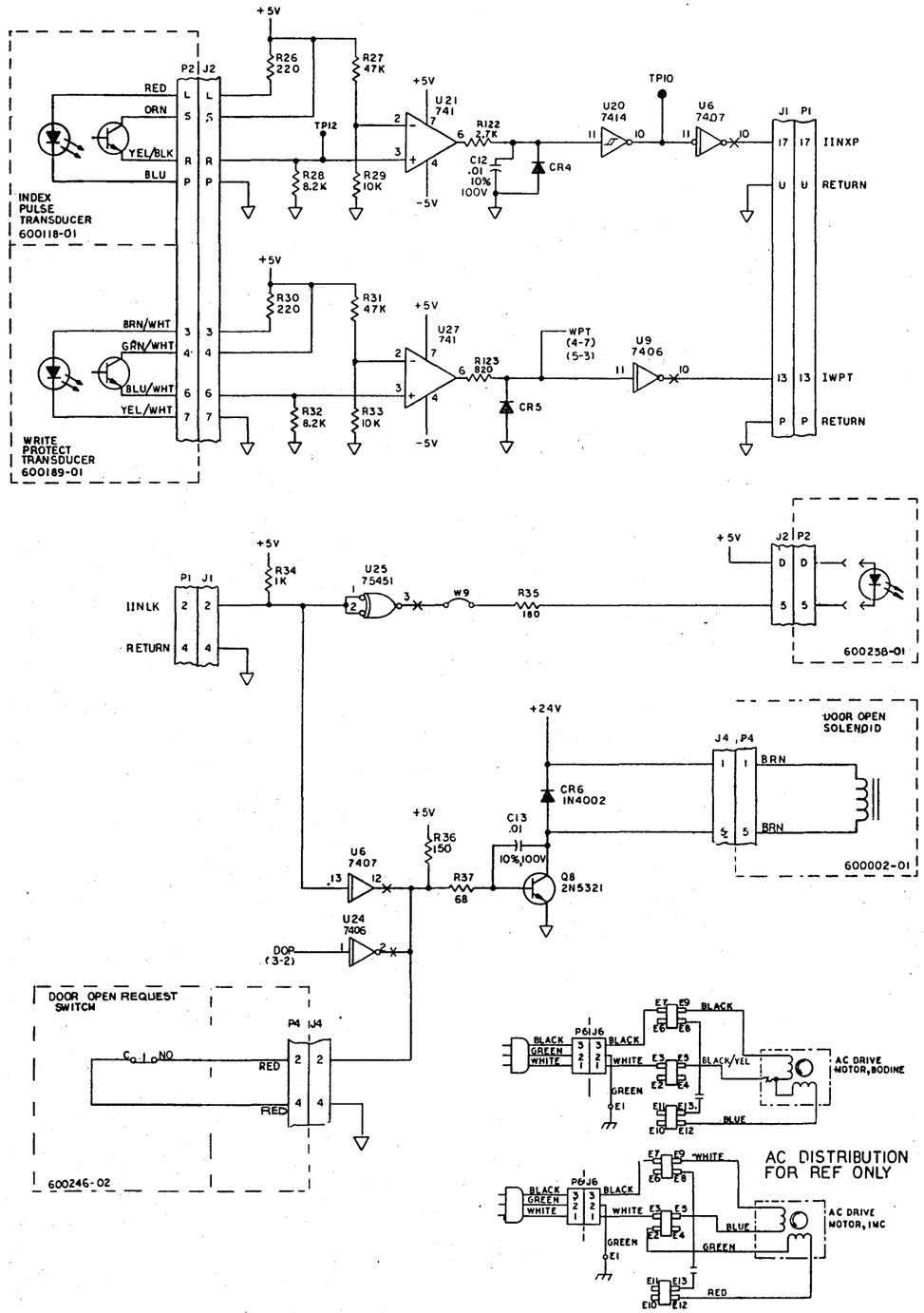
SIGNATURES	DATE
DR	12-15-75
CHK	
ENG	
SHOP SUP	
PROD. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE
SCHEMATIC,
FD, BASIC II, AC

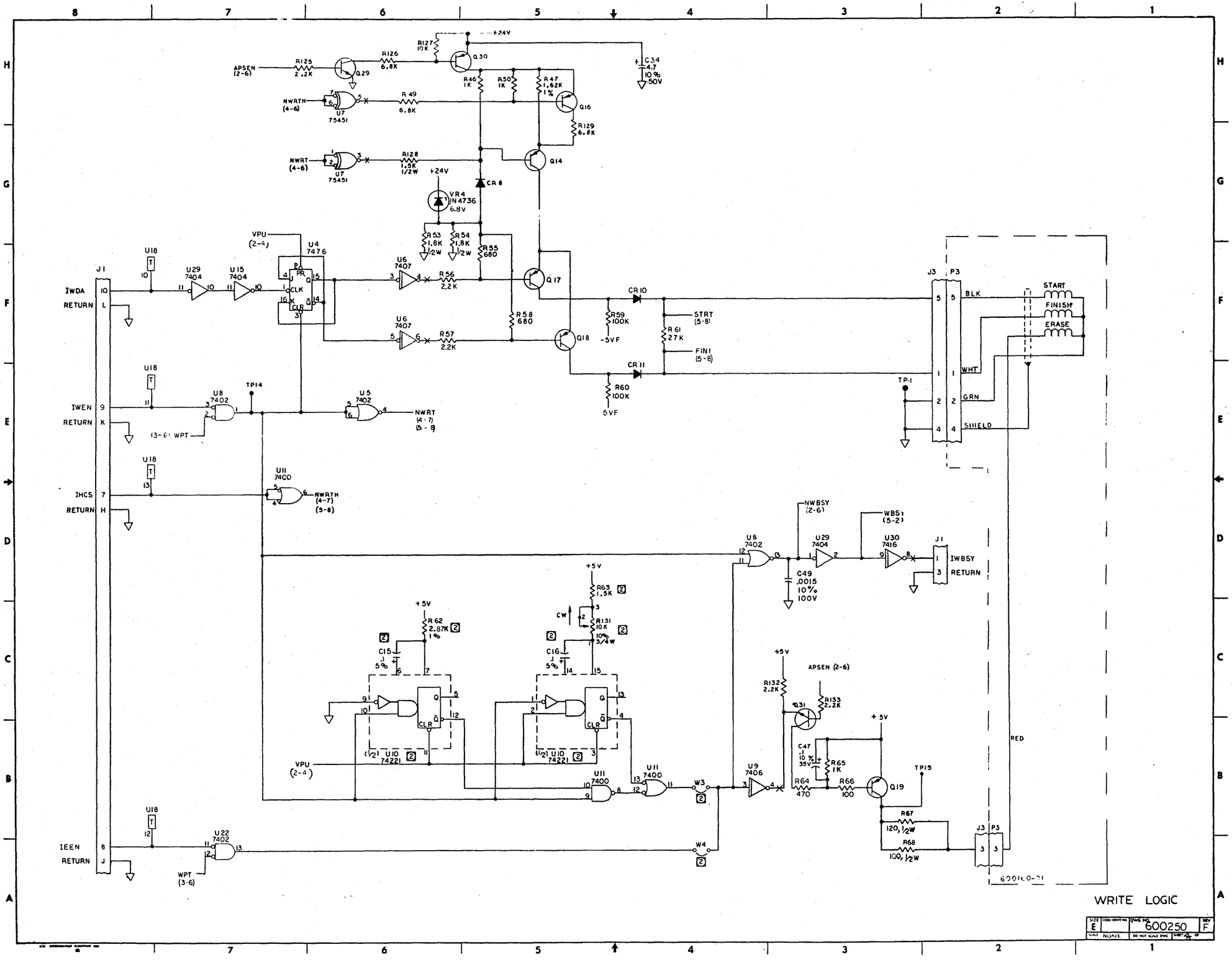
SIZE E | CODE IDENT NO. | DWG NO. 600250 | REV F
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 5

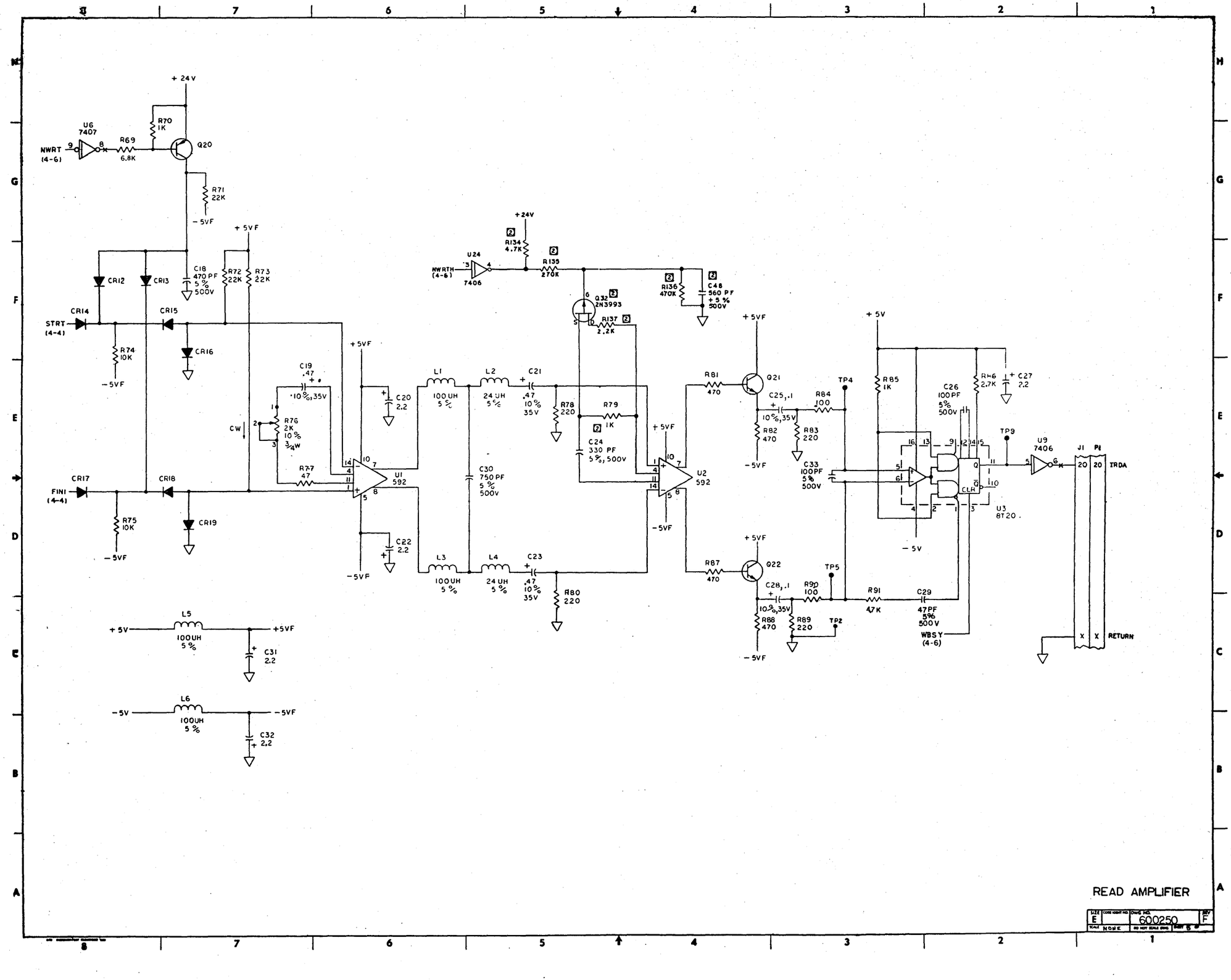

+5V
R1 1K
R2 20K 10% 3/4W
CW
R3 21.5K 1%
C2 .1 5%
C3 .1 10% 35V
C1 2.2
TP7
U13 555
U20 7414
U15 7404
R4 2.7K
C4 22 15V
U17 74221
+24VF
CR1 IN4002
R5 120 1/2W
R6 120 1/2W
+24VF
J2 P2
33 20W
RED/WHT
VIO/WHT
Ø1
U30 7416
R8 150
R9 68
Q1 TIP-112
U24 7406
W5
NHLD (3-2)
TP8
R10 150
R11 68
Q2 TIP-112
+24VF
CR2 IN4002
U9 7406
W6
R12 150
R13 68
Q3 TIP-110
+24VF
CR3 IN4002
BLK
Ø2
R14 150
R15 68
Q4 TIP-110
GRY
Ø3
REF:600107-01
U22 7402
U20 7414
U28 7450
R7 470
VPU (4-7)
U18
U29 7404
U23 7402
TP11
NWBSY
U14 7476
U22 7402
U29 7404
U23 7402
U14 7476
U23 7402
U4 7476
U22 7402
U9 7406
J1 P1
ITRKØ
RETURN
P1 J1
ISTI
RETURN
IS TO
RETURN
+24 VDC
+24 VDC
RETURN (+24VDC)
+24 V
W8
VR1 16V IN5246B
R17 1.8K
C5 4.7 ±10% 50V
R16 1K
Q5
R18 820
R19 270
C6 47 6V
R20 47
U20 7414
NPSEN (6-7)
+5VDC
RETURN (+5VDC)
VR2 3.3V IN5226B
+24V
R22 2.2K 1/2W
R21 120
Q6
R23 150
APSEN (4-3)
Q7
+24V
C7 2.2
C8 2.2
C9 2.2
+5V
R119 2.7K 1/2W
Q28
R120 180
VR5 IN5226B
-15/-12/-5VDC
W1
W2
R24 100 2W
R121 100 2W
-5V
VR3 5.1V 1N4733A
RETURN (-15/-12/-5VDC)
TRACK Ø SW
P2 J2
GRN
NO
C
YEL/RED
NC
VIO
REF:600132-01
U15 7404
U15 7404
TP6
R25 1M
C11 .01 10% 100V
HEAD POSITIONER LOGIC/DRIVE
SIZE E
CODE IDENT NO
DWG NO. 600250
REV F
DO NOT SCALE DWG
SHEET 2 OF



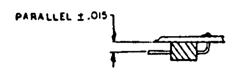
INTERLOCKS/TRANSDUCERS

SIZE	CODE IDENT NO	DWG NO.	REV
E		600250	F
SCALE NONE	DO NOT SCALE DWG	SHEET 3 OF	

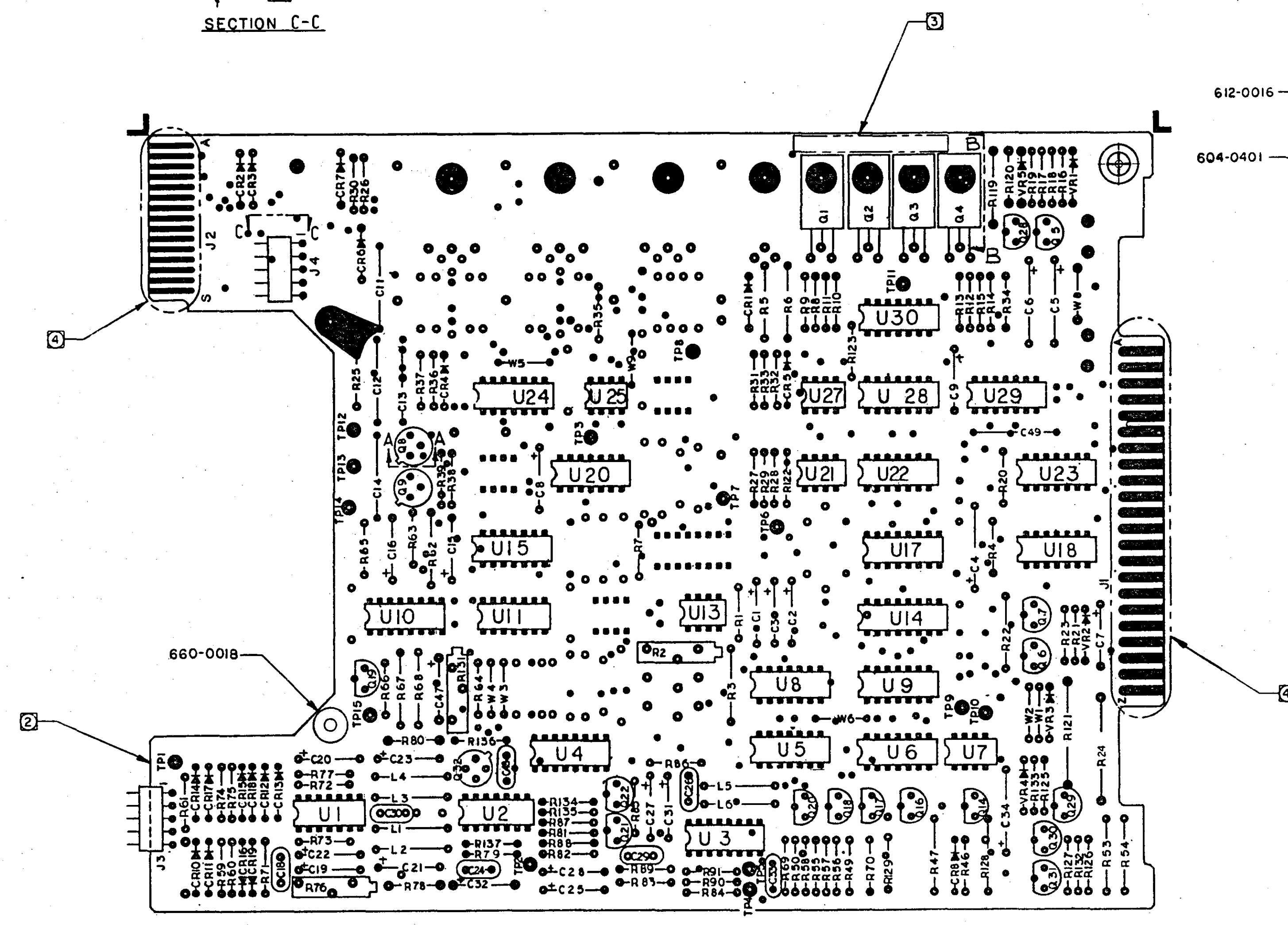

+24V
R127 10K
Q30
C34 47 10% 50V
APSEN (2-6)
R125 2.2K
Q29
R126 6.8K
R46 1K
R50 1K
R47 1.62K 1%
Q16
NWRTH (4-6)
U7 75451
R49 6.8K
R129 6.8K
NWRT (4-6)
R128 1.5K 1/2W
Q14
CR8
VR4 1N4736 6.8V
R53 1.8K 1/2W
R54 1.8K 1/2W
R55 680
VPU (2-4)
U4 7476
U18
J1
IWDA
RETURN
U29 7404
U15 7404
U6 7407
R56 2.2K
Q17
CR10
R59 100K
-5VF
STRT (5-8)
R61 27K
FINI (5-8)
R58 680
U6 7407
R57 2.2K
Q18
CR11
R60 100K
5VF
J3
P3
BLK
WHT
GRN
SHIELD
START
FINISH
ERASE
TP-1
IWEN
RETURN
U8 7402
TP14
U5 7402
NWRT (4-7) (5-8)
(3-6) WPT
IHCS
RETURN
U11 74C00
NWRTH (4-7) (5-8)
NWBSY (2-6)
WBSY (5-2)
U30 7416
IWBSY
RETURN
C49 .0015 10% 100V
+5V
R63 1.5K
R62 2.87K 1%
R131 10K 10% 3/4W
CW
C15 1 5%
C16 1 5%
U10 7422
U11 7400
U9 7406
APSEN (2-6)
R132 2.2K
Q31
R133 2.2K
C47 1 10% 35V
R65 1K
R64 470
R66 100
Q19
TP15
R67 120, 1/2W
R68 100, 1/2W
RED
IEEN
RETURN
U22 7402
WPT (3-6)
W3
W4
600250-21
WRITE LOGIC
SIZE E
DWG NO 600250
REV F
SCALE NONE
DO NOT SCALE DWG
SHEET 4 OF 6

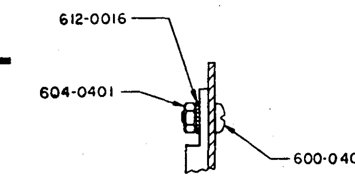

+24V
U6
7407
NWRT
(4-6)
R69
6.8K
R70
1K
Q20
R71
22K
-5VF
+5VF
CR12
CR13
C18
470 PF
5%
500V
R72
22K
R73
22K
CR14
CR15
STRT
(4-4)
R74
10K
CR16
C19
.47
+ -
10%,35V
CW
R76
2K
10%
3/4W
R77
47
U1
592
C20
2.2
L1
100UH
5%
L2
24UH
5%
C21
.47
10%
35V
R78
220
R79
1K
C24
330 PF
5%,500V
C30
750PF
5%
500V
U2
592
C22
2.2
L3
100UH
5%
L4
24UH
5%
C23
.47
10%
35V
R80
220
CR17
CR18
FINI
(4-4)
R75
10K
CR19
U24
NWRTH
(4-6)
7406
R134
4.7K
R135
270K
Q23
2N3993
R137
2.2K
R136
470K
C48
560 PF
+5%
500V
R81
470
Q21
C25,.1
10%,35V
R82
470
R83
220
R84
100
TP4
C33
100PF
5%
500V
R85
1K
R86
2.7K
C27
2.2
C26
100PF
5%
500V
TP9
U9
7406
U3
8T20.
J1
P1
20
20
TRDA
RETURN
WBSY
(4-6)
R87
470
Q22
C28,.1
10%,35V
R88
470
R89
220
TP2
R90
100
TP5
R91
4.7K
C29
47PF
5%
500V
L5
100UH
5%
C31
2.2
L6
100UH
5%
C32
2.2
READ AMPLIFIER
E
600250
F

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 200-FA PRE-PROD REL		SOL		
B	ECN 30352A				
B1	ECN 30400		RE		
	ERN 200-GP PROD REL		RE		
C	ECN 30467	5-13-76	RJ	JBL	

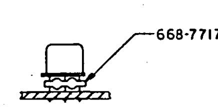


SECTION C-C





SECTION B-B
4 PLACES



SECTION A-A
(TYPICAL TO-5 MTG)

4 MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.

3 MARK PART NUMBER 600251 VERSION NUMBER AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 600252-01 REV D AND SUBSEQENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC 600250
SPECIFICATION
REF DWGS:

PART NO. 600251- REV

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR.	
CHK	
DES	
ENGR	
PROJ. ENGR	

NEXT ASSY | 1ST USED ON
APPLICATION

FINISH:

MATL: SEE LM

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA, FD,
BASIC II, AC

SIZE E | CODE IDENT NO. | DWG NO. 600251 | REV C

SCALE 2 1 | DO NOT SCALE DWG | SHEET 1 OF 1

600251 C

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 200 FB PRE-PROD RELEASE				
B	ECN 30367A				
B1	ECN 30397				
	ERN 200-GP PROD RELEASE		R.E.		
C	ECN 30462A		C.J.		
D	ECN 30467	5-12-76	RJ		
E	ECN 30477	5-26-76	RJ		
F	ECN 30505	8-4-76	RJ		

TABLE I [1]

PART NUMBER	REFERENCE DESIGNATION
100-1015	R66, 84, 90, 111
100-1025	R1, 16, 46, 50, , 65, 85, 110, 70, 79
100-1035	R29, 33, 93, 74, 75, 127
100-1045	R59, 60
100-1055	R25
100-1215	R21
100-1515	R8, 10, 12, 14, 23, 102, 112, 38, 115, 106
100-1235	R94
100-1825	R17, 100
100-2215	R26, 30, 78, 80, , 83, , 89
100-2225	R92, 56, 57, 125, 132, 133
100-2235	R71, 72, 73
100-2715	R19,
100-2725	R86, 4, 122.
100-2735	R61
100-1835	R101
100-4705	R20, 77
100-4715	R7, 64, 82, 88, 81, 87
100-4725	R91
100-4735	R27, 31
100-6805	R9, 11, 13, 15, 39, 103, 107, 113, 116
100-6815	R58, 55
100-6825	R126, 129, 69, 49
100-6835	R96
100-8215	R18, R123
100-8225	R28, 32
100-2745	R95
100-1815	R120
101-1015	R68
101-1215	R5, 6, 67
101-1825	R53, 54
101-2225	R22
101-1525	R128
101-2725	R119
103-1015	R24, 121
104-1331	R109
104-1621	R47
104-2152	R3
104-2372	R108
104-2612	R99
109-0003	R118
109-0008	R104, 105, 114, 117
120-0001	U18
121-1030	R98
121-1040	R97
121-2020	R76
121-2030	R2
130-1015	C26, 45
130-4705	C29
130-4715	C18
130-7515	C30
130-3315	C24
131-1030	C11, 12, 14, , 40
131-1520	C48
135-5061	C38, 39, 44
139-1020	C2, 35
139-1055	C3, 47, 36, 25, 28
139-2244	C1, 7, 8, 9, , 20, 22, 27, 34, 41, 42, 31, 32
139-2262	C4
139-2710	C33
139-4751	C5, 46
139-4755	C21, 23, 19 43
139-4762	C6, 37
200-1100	Q3, 4, 25, 26, 27
200-1120	Q1, 2, 24
200-4123	Q5, 6, 7, 28, 29, 31, , 21, 22
200-4125	Q14, 16, 17, 18, 19, 20, 30
200-5321	Q9
204-4393	Q23
300-4002	CR1, 2, 3, 7, 21, 22, 25
300-4446	CR4, 5, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 23, 24
330-0515	VR3
330-0475	VR6
330-0685	VR4
331-0335	VR2, 5
331-1605	VR1
400-0555	U13, 12
400-0592	U1, 2
400-2741	U21, 26, 27
515-1015	L1, 3, 5, 6
515-2405	L2, 4
700-4221	U17
700-7545	U25, 19, 7
700-7400	U11
700-7402	U5, 8, 22, 23
700-7404	U15, 29
700-7406	U9, 24
700-7407	U6
700-7414	U20
700-7416	U30,
700-7450	U28
700-7476	U4 14, 16
700-8020	U3

TABLE II [2]

	ASSEMBLY VERSION NO.			VERSION CHARACTERISTIC	[12] C15, C16, R62, R63, U10, R131		W1	W2	[12] W3	[12] W4	W5	W6	
					USAGE [3]		100-0005	100-0005	100-0005	100-0005	100-0005	100-0005	
SINGLE DENSITY	INTERNAL TRIM ERASE	-5V	-01	SINGLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	USE		USE	OMIT	USE	OMIT	OMIT	OMIT	
			-02	SINGLE DENSITY, INTERNAL ERASE, -5V, POWER SAVE FEATURE IN	USE		USE	OMIT	USE	OMIT	USE	USE	
		-12/-15V	-03	SINGLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	USE		OMIT	USE	USE	OMIT	OMIT	OMIT	
			-04	SINGLE DENSITY, INTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	USE		OMIT	USE	USE	OMIT	USE	USE	
	EXTERNAL TRIM ERASE OPTION	-5V	-05	SINGLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE OUT	OMIT		USE	OMIT	OMIT	USE	OMIT	OMIT	
			-06	SINGLE DENSITY, EXTERNAL ERASE, -5V, POWER SAVE FEATURE IN	OMIT		USE	OMIT	OMIT	USE	USE	USE	
		-12/-15V	-07	SINGLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE OUT	OMIT		OMIT	USE	OMIT	USE	OMIT	OMIT	
			-08	SINGLE DENSITY, EXTERNAL ERASE, -12/-15V, POWER SAVE FEATURE IN	OMIT		OMIT	USE	OMIT	USE	USE	USE	

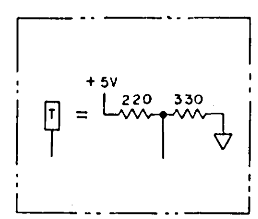


TABLE V
SPARES:

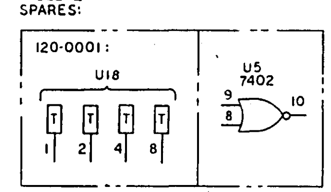


TABLE III [3]

PART NUMBER	REFERENCE DESIGNATION
104-2871	R62
100-1525	R63
139-1020	C15, 16
700-4221	U10
121-1030	R131

REFERENCE DESIGNATIONS

LAST USED	NOT USED	DELETED
C48	C13	C10, 17
CR25	CR6	CR9
F1		
L6		
Q31	Q8	Q10, 11, 12, 13, 15
R133	R34 THRU 37, 52, 124, 130	R40, 41, 43, 44, 45, 48, 51, 42
TP15		
U30		
VR6		
W6	W7, 8	

[12] VERSIONS OF THIS ASSEMBLY FOR INTERNAL/EXTERNAL TRIM ERASE MAY BE CREATED BY INSTALLING C15, C16, R62, R63, R131, U10 AND SELECTING W3 OR W4 AS APPLICABLE.

11. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

10. DIODES ARE 1N4446.

9. PNP TRANSISTORS ARE 2N4125.

8. NPN TRANSISTORS ARE 2N4123.

7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

5. FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

4. PIN 7 OF ALL I.C.s IS 0V. 7476 PIN 13 IS 0V 74221 PIN 8 IS 0V
PIN 14 OF ALL I.C.s IS +5V. PIN 5 IS +5V PIN 16 IS +5V

[3] FOR PART NUMBER SEE TABLE III.

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS:
ASSEMBLY NO. 600321

600320 F

PERTEC PERIPHERAL EQUIPMENT

TITLE SCHEMATIC, FD, BASIC II, DC

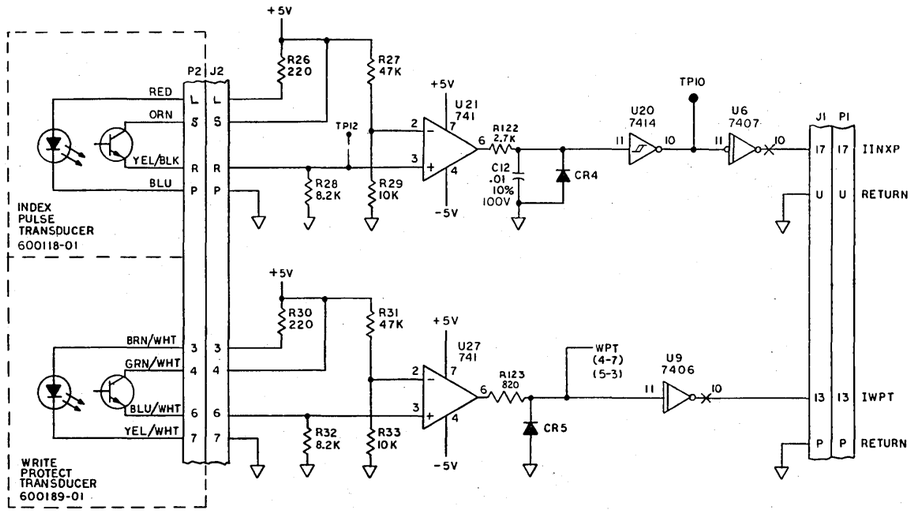
SIZE E | DWG NO. 600320 | REV F | SCALE NONE | DO NOT SCALE DWG | SHEET OF 6

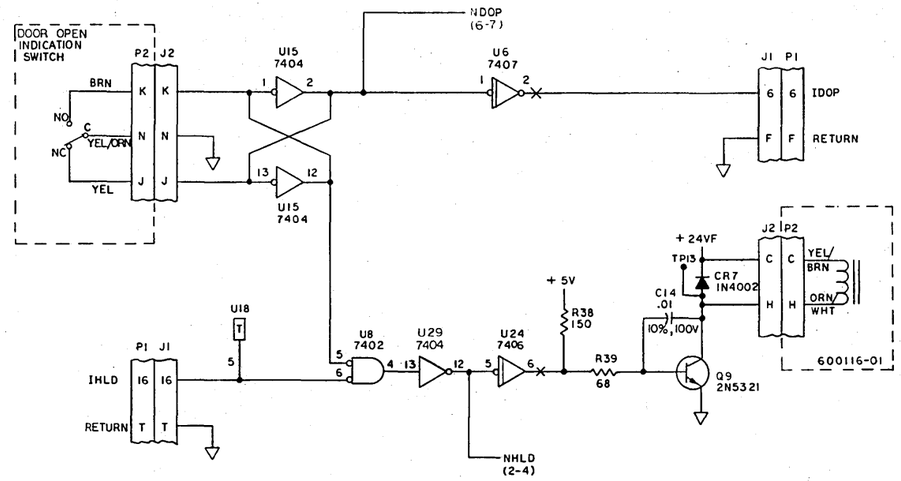
NEXT ASSY | USED ON | APPLICATION | FINISH: | MATL: | SIGNATURES | DATE

HEAD POSITIONER LOGIC/DRIVE

SIZE	CODE IDENT NO.	DWG NO.	REV
E		600320	F

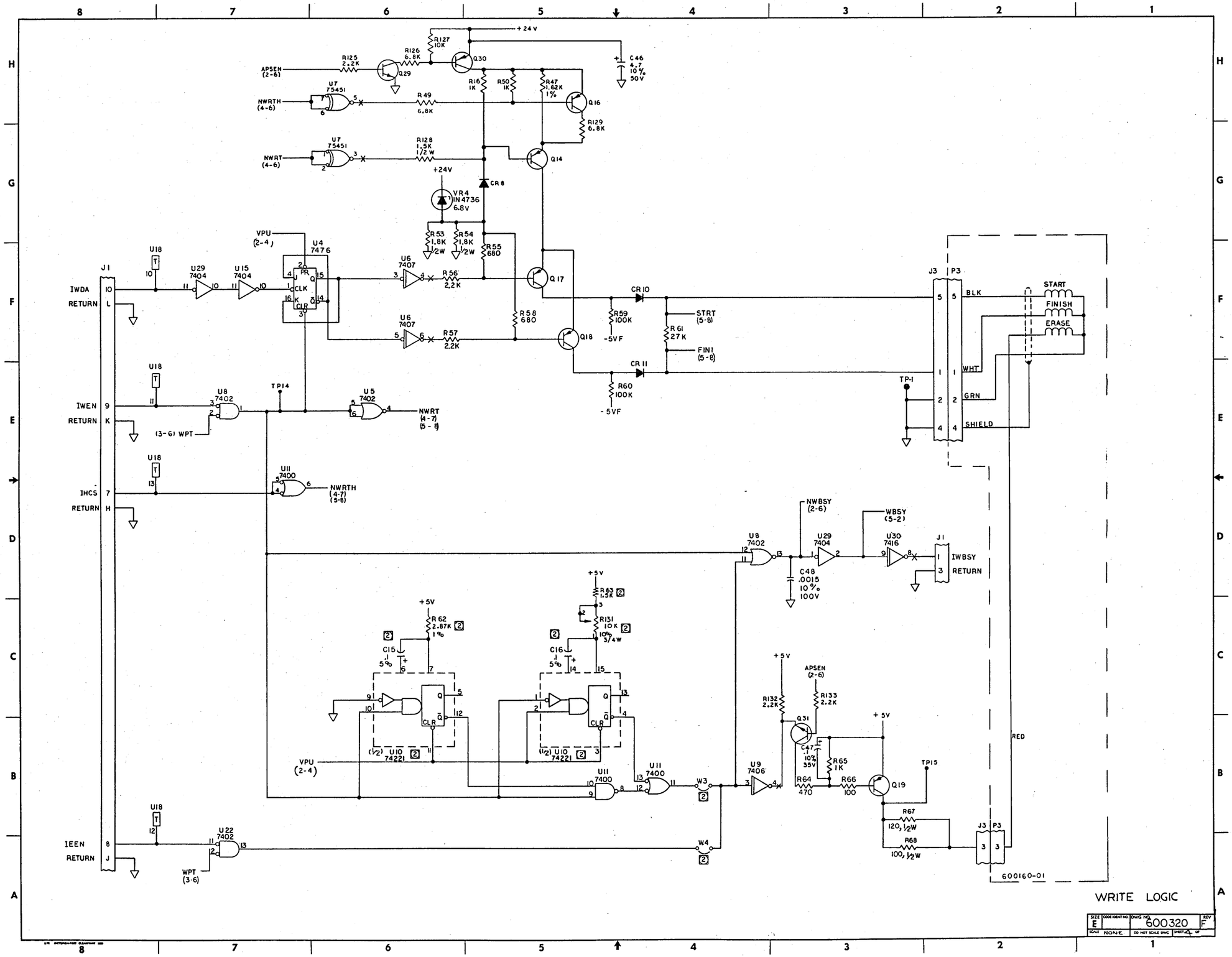
SCALE — DO NOT SCALE DWG — SHEET 2 OF

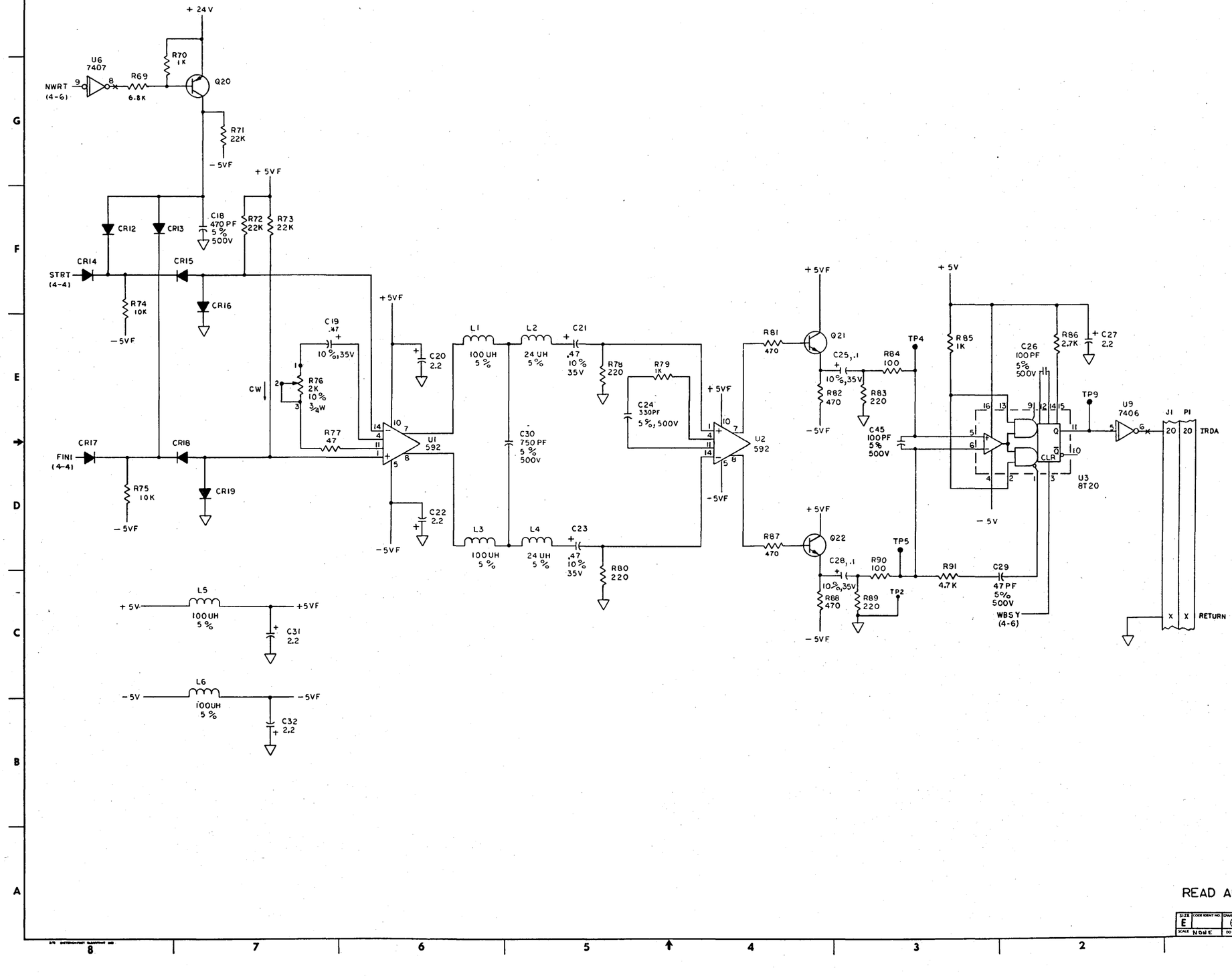




INTERLOCKS/TRANSDUCERS

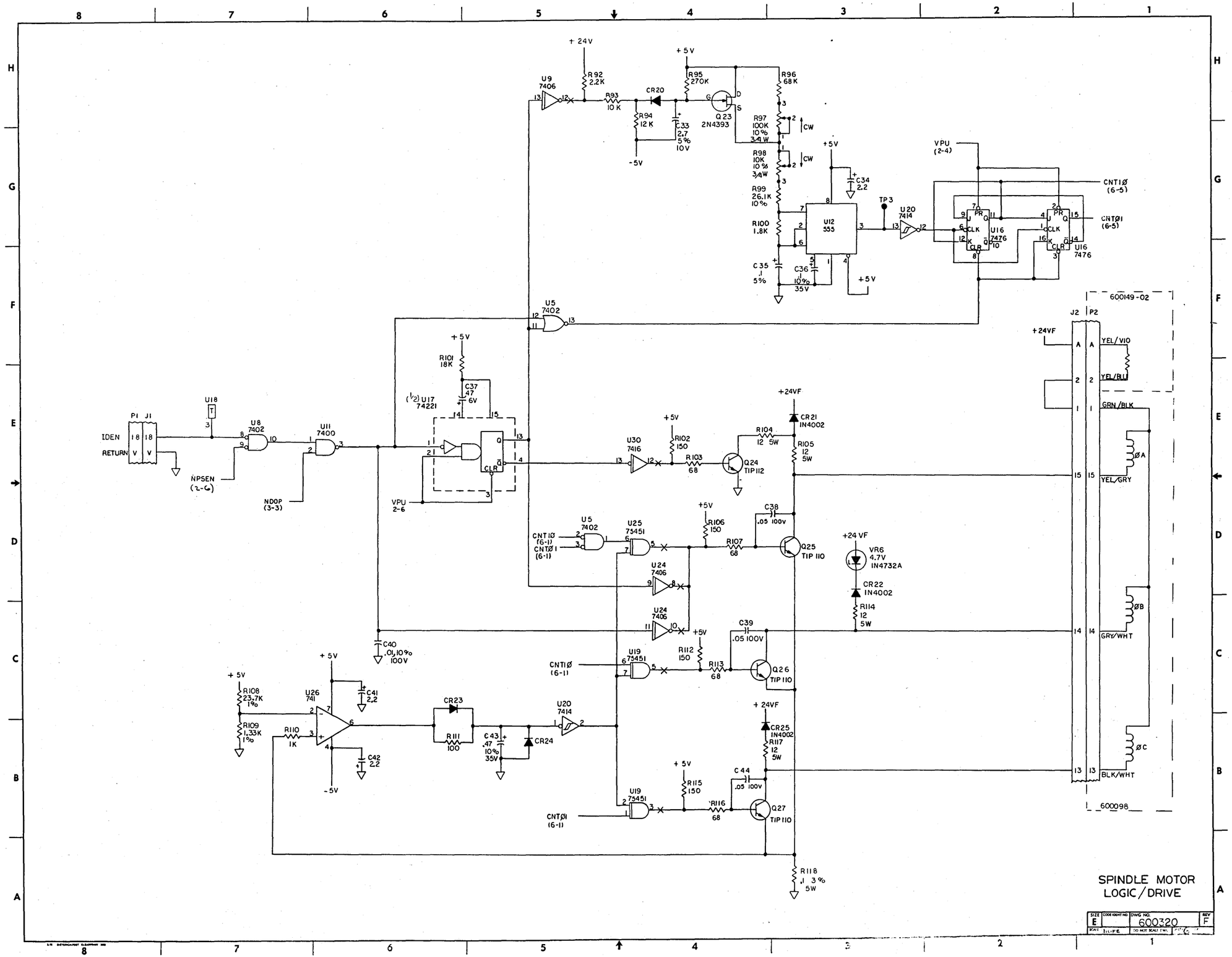
SIZE	CODE IDENT NO	DWG NO	REV
E		600320	F
SCALE NONE	DO NOT SCALE DWG	SHEET 3 OF	


+24V
R127 10K
R126 6.8K
R125 2.2K
APSEN (2-6)
Q29
Q30
C46 4.7 10% 50V
R16 1K
R50 1K
R47 1.62K 1%
Q16
R129 6.8K
U7 75451
NWRTH (4-6)
R49 6.8K
NWRT (4-6)
R128 1.5K 1/2W
Q14
CR8
VR4 IN4736 6.8V
R53 1.8K 1/2W
R54 1.8K 1/2W
R55 680
VPU (2-4)
U4 7476
U6 7407
R56 2.2K
Q17
CR10
R59 100K
-5VF
STRT (5-8)
R61 27K
FINI (5-8)
R58 680
R57 2.2K
Q18
CR11
R60 100K
J1
IWDA
RETURN
U18
U29 7404
U15 7404
U8 7402
TP14
U5 7402
IWEN
(3-6) WPT
NWRT (4-7) (5-8)
IHCS
NWRTH (4-7) (5-8)
U11 7400
IEEN
WPT (3-6)
U22 7402
J3 P3
BLK
WHT
GRN
SHIELD
TP1
START
FINISH
ERASE
RED
600160-01
NWBSY (2-6)
WBSY (5-2)
U30 7416
IWBSY
C48 .0015 10% 100V
+5V
R62 2.87K 1%
R63 1.5K
R131 10K 10% 3/4W
C15 .1 5%
C16 .1 5%
U10 74221
W3
W4
U9 7406
APSEN (2-6)
R132 2.2K
R133 2.2K
Q31
C47 .1 10% 35V
R64 470
R65 1K
R66 100
Q19
TP15
R67 120, 1/2W
R68 100, 1/2W
WRITE LOGIC
SIZE E
CODE IDENT NO
DWG NO 600320
REV F
SCALE NONE
DO NOT SCALE DWG
SHEET 4 OF

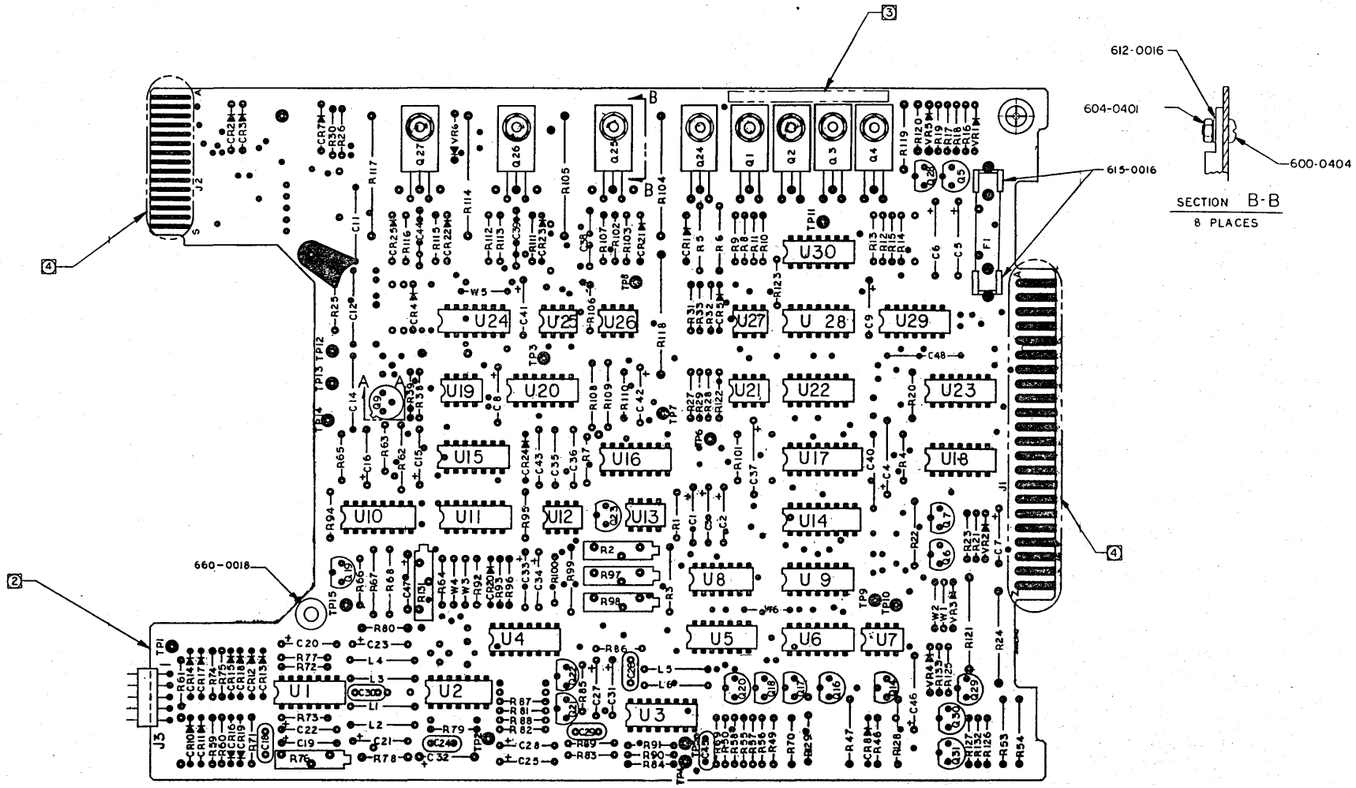


READ AMPLIFIER

SIZE	CODE IDENT NO	DWG NO	REV
E		600320	F
SCALE NONE		DO NOT SCALE DWG	SHEET 5 OF


+24V
+5V
U9 7406
R92 2.2K
R93 10K
CR20
R94 12K
-5V
C33 2.7 5% 10V
R95 270K
R96 68K
Q23 2N4393
R97 100K 10% 3/4W
CW
R98 10K 10% 3/4W
R99 26.1K 10%
R100 1.8K
C35 5%
C36 10% 35V
U12 555
C34 2.2
TP3
U20 7414
VPU (2-4)
CNTIØ (6-5)
CNTØI (6-5)
U16 7476
U5 7402
R101 18K
C37 47 6V
(1/2) U17 74221
VPU 2-6
U18
P1 J1
IDEN 18 18
RETURN V V
U8 7402
U11 7400
NPSEN (2-6)
NDOP (3-3)
U30 7416
R102 150
R103 68
Q24 TIP112
R104 12 5W
R105 12 5W
CR21 IN4002
U5 7402
U25 75451
CNTIØ (6-1)
CNTØI (6-1)
R106 150
R107 68
C38 .05 100V
Q25 TIP 110
U24 7406
+24 VF
VR6 4.7V IN4732A
CR22 IN4002
R114 12 5W
C40 .01, 10% 100V
U19 75451
CNTIØ (6-1)
R112 150
R113 68
C39 .05 100V
Q26 TIP 110
R108 23.7K 1%
R109 1.33K 1%
U26 741
R110 1K
C41 2.2
C42 2.2
CR23
R111 100
C43 .47 10% 35V
CR24
U20 7414
CR25 IN4002
R117 12 5W
C44 .05 100V
U19 75451
CNTØI (6-1)
R115 150
R116 68
Q27 TIP 110
R118 .1 3% 5W
600149-02
J2 P2
YEL/VIO
YEL/BLU
GRN/BLK
ØA
YEL/GRY
ØB
GRY/WHT
ØC
BLK/WHT
600098
SPINDLE MOTOR LOGIC/DRIVE
SIZE E
DWG NO. 600320
REV F

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 200-FB PRE-PROD. RELEASE	3/17	[illegible]	[illegible]	[illegible]
B	ECN 30376A	4/24	[illegible]	[illegible]	[illegible]
B	ERN 200-GP PROD REL	10/26	[illegible]	[illegible]	[illegible]
C	ECN 30462A	11/24	C.J.	[illegible]	[illegible]
D	ECN 30467	5-12-86	F.J.	[illegible]	[illegible]



5. MAINTAIN MIN. AIR GAP OF .10 BETWEEN CONPONENT BODY & BOARD FOR R104, R105, R114 R117 & R118

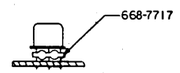
4 MASK AREAS SHOWN DURING FLOW SOLDER OPERATION.

3 MARK PART NUMBER 600321, VERSION NUMBER AND VERSION ISSUE LETTER IN AREA SHOWN.

2 THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 600252-01 REV D AND SUBSEQENT.

1. ASSEMBLE PER STANDARD MANUFATURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED



SECTION A-A
(TYPICAL TO-5 MTG.)

SCHEMATIC 600320

REF DWGS:

PART NO. 600321- REV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .03 ANGULAR ± 1/2°
.XXX ± .010
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR LUIS P	4/87
CHK [illegible]	4/87
APP [illegible]	4/87
MGR [illegible]	4/87
PROD [illegible]	4/87

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA, FD, BASIC II, DC

NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL: SEE LM

SIZE	CODE IDENT NO.	DWG NO.	REV
E		600321	D

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1

600321 D