APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

DATA TECHNOLOGY CORPORATION

DTC510 CONTROLLER SPECIFICATION

PRELIMINARY

June 5, 1981

PROMS WD11*

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN	DATE	DTC510
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO. / REV.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET

DTC510 SPEC REVISION RECORD

Revision	Description
1/16/81	Chg Shugart Tech. to Seagate Tech.; correct section 7.0; add Appendices B & C
1/21/81	Changes or corrections to pages 8, 11, 12, 13, 15, 17, 18
6/5/81	Revision to section 4.4.2

DRAWN	SIZE A	FSCM NO.	DWG. NO.	REV.
ISSUED	SCALE		SHEET	

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ISSUED	SCALE		SHEET 1	

1.0 INTRODUCTION

The DTC510 Controller consists of a microprocessor-based controller with on-board data separator logic, and is able to control a maximum of two Seagate Technology ST506 fixed disk drives, or equivalent.

Commands are issued to the controller over a bidirectional bus connected to the host computer. The data separator/"serdes" logic serializes bytes and converts to MFM data, and deserializes MFM data into 8-bit bytes.

Due to the microprogrammed approach utilized in the controller, extensive diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media imperfections up to 4-bit burst errors.

2.0 DTC510 Controller

2.1 Features

2.1.1 The capabilities supplied as standard with the DTC510 are listed below:

AUTOMATIC SEEK AND VERIFY	A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.
FAULT DETECTION	Two classes of faults are flagged to improve error handling: * Controller faults * Disk faults

AUTOMATIC HEAD AND CYLINDER SWITCHING	If during a multi-block data transfer the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.
DATA ERROR SENSING AND CORRECTION	If a data error is detected during a disk data transfer, the controller indicates whether or not it is correctable. If correctable, either a pointer and mask can be requested by the host for applying the correction or the error can be automatically corrected.
LOGICAL TO PHYSICAL DRIVE CORRELATION	Logical unit numbers (LUN's) are independent of physical port numbers. All accesses specify LUN's.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.
EFFICIENT HOST INTERFACE PROTOCOL	A bidirectional bus between the controller and host provides a simple yet efficient communication path. In addition, a high level command set permits effective command initiation.
SECTOR INTERLEAVE	Sector interleaving is programmable with up to 16 way interleave.
ODD PARITY	The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
FIXED SECTOR SIZE	The sector size is fixed at 256 bytes of data.
NUMBER OF DRIVES	The controller will connect to a maximum of two (2) ST506 drives.

2.2 System Configuration

The controller and data separator comprise a single PCB. A maximum of two (2) drives may be connected as shown in Fig. 2.1.

2.3 Theory of Operation

Disk commands are issued to the DTC510 via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (Command structure is described in Section 4.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send completion status to the host. (Further delineation of the completion status may be requested by issuing the appropriate sense commands.)

Odd parity is generated by the DTC510 for all information that it puts on the I/O bus. If enabled, the DTC510 flags all information that it receives with bad parity.

2.3.1 Electrical Interface

The electrical interface to the ST506 will conform to the requirements described in the ST506 interface specification. The electrical interface to the DTC510 Host Bus is shown in Fig. 2.2.

NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

SH

DWG. NO.

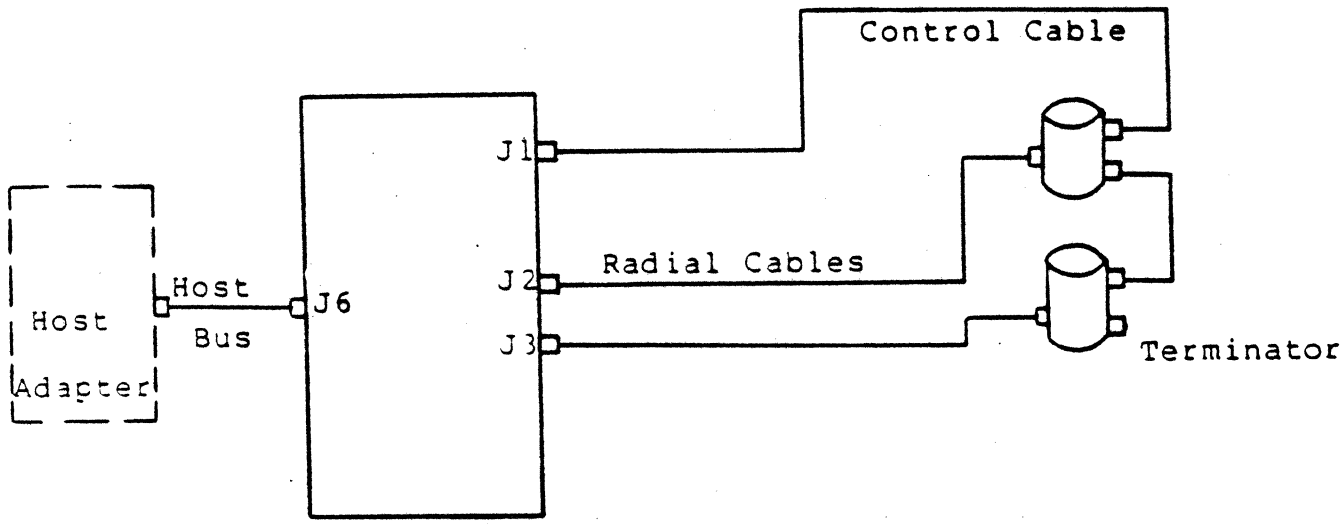


Figure 2.1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO. DTC510	DTC Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN	DATE	SYSTEM CONFIGURATION
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

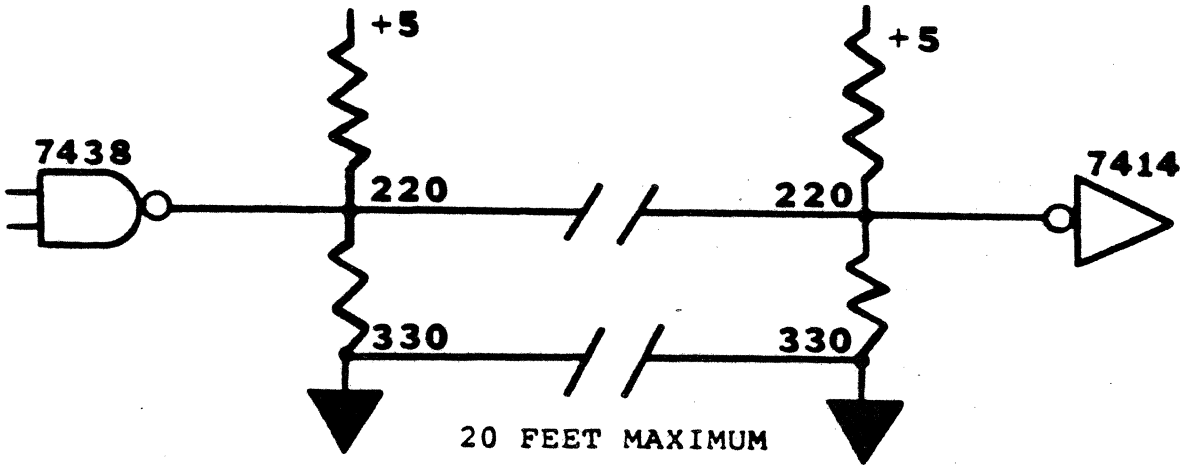


Figure 2.2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	DTC Data Technology Corporation	
	APPROVALS / DATE	ELECTRICAL INTERFACE	
MATERIAL	DRAWN		
FINISH	CHECKED	SIZE A / FSCM NO. / DWG. NO. / REV.	
DO NOT SCALE DRAWING	ISSUED	SCALE / SHEET 6	

3.0 DTC510 HOST BUS

The DTC510 Host Bus is a negative-logic, bidirectional 8-bit data bus utilizing odd parity. The electrical interface consists of an open collector bus terminated on each end by a 220/330 ohm resistor network. The controller regulates transfers across the bus which eliminates data overruns that could occur during data transfers.

The term "asserted" means that the signal on the host bus is between 0V and 0.8V. The term "deasserted" means that the signal on the host bus is between 2.5V and 3.5V (Negative or Low True logic).

3.1 Signal Definition

3.1.1 Unidirectonal Signals Driven By Controller

I/O — Input/Output
When asserted, the data on the bus is driven by the controller. When deasserted, the data on the bus is driven by the host adapter. The host adapter will use this line to enable its drivers onto the data bus.

C/D — Command/Data
When asserted, the data transmitted across the bus will be the command bytes. When deasserted, the data will be the disk data bytes.

BUSY — This bit is asserted as a response to the SEL line from the host adapter and to indicate that the host bus is currently in use.

MSG — Message
When asserted, indicates that the command is completed. This bit is always followed with the assertion of I/O, and the assertion of REQ.

REQ — Request
This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the host adapter (H/A).

I/O	C/D	MSG	Meaning
d	a	d	Get command from H/A
d	d	d	Get data from H/A
a	d	d	Send data to H/A
a	a	d	Send status byte to H/A
a	a	a	Command done to H/A

a = asserted, d = deasserted

3.1.2 Unidirectional Signals Driven By Host Adapter

ACK — Acknowledge
This bit is asserted as a response to REQ from the controller. The timing requirements on this signal with respect to the data is described in REQuest section. ACK must be returned for each REQ assertion.

RST — Reset
When asserted, this bit forces the controller to the beginning of its microcode. Any error status request will result in invalid information after RST has been asserted. All signals to the drives are deasserted. RST must be asserted for a minimum of 250ns and a maximum of 10us.

SEL — Select
When asserted, indicates the beginning of the command transaction. The H/A asserts SEL to gain the attention of the controller. A data bit on the host host bus must also be asserted during SEL time to determine which controller is selected. SEL must not be asserted on the host bus before the data bit. The controller will return BUSY within lus. After the assertion of BUSY, the H/A will deassert SEL.

3.1.3 Bidirectional Data

DB(7-0,P) - Data lines 7 thru 0 represent the eight data bits (DB0=lsb). Parity is represented by P. The controller utilizes odd parity (the number of asserted bits on the host bus is always odd).

3.2 Theory of Operation

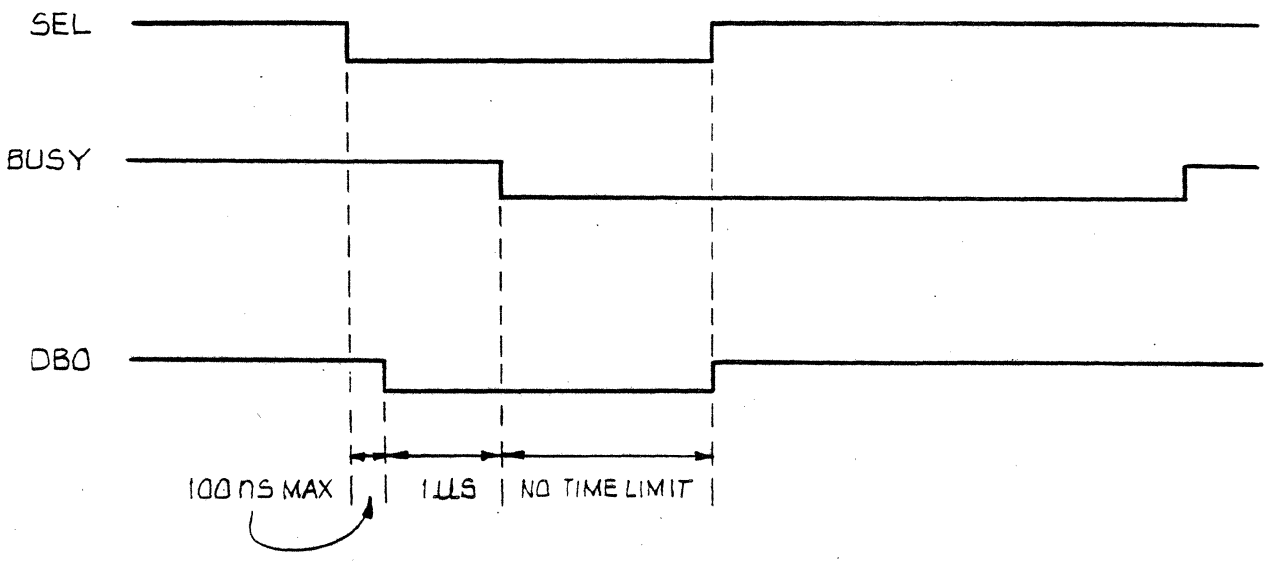
Whenever the host adapter has a command for the controller, it performs a selection sequence to gain the attention of the controller. The sequence is as follows:

The host adapter asserts SEL and DB0 (controller address bit) on the host bus. It then waits for the controller to respond with BUSY. Upon reception of BUSY, the H/A deasserts SEL. The controller now has control of the host bus.

After the controller asserts BUSY, it then asserts C/D (to indicate command mode transfer), and deasserts I/O (to indicate output from the host adapter) to fetch the command bytes from the H/A. The command bytes are transferred over the host bus with the REQ/ACK handshake protocol until all command bytes are transferred to the controller. (The command byte fetch mode ends after the last REQ pulse from the controller is deasserted.)

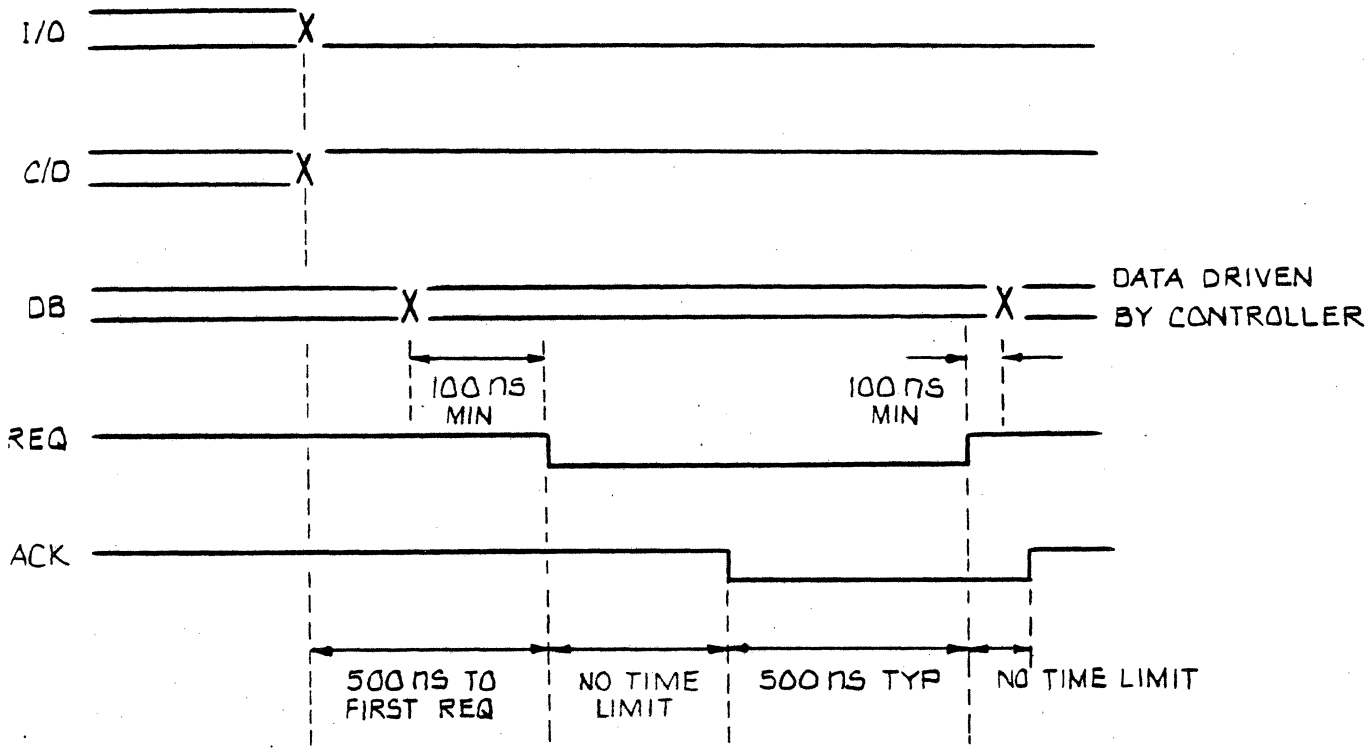
For data transfer, the controller deasserts the C/D line to indicate data mode. Depending on the command type (read/write disk), the I/O bit on the host bus is asserted or deasserted by the controller, and the data is transferred (one byte at a time) with the same REQ/ACK handshake protocol. After all the data bytes have been transferred, a completion status is placed on the data bus by the controller - C/D and I/O are asserted. REQ is asserted and the controller waits for ACK from the host adapter. After the status byte transfer, the controller places zeros on the data bus and asserts C/D, I/O and MSG along with REQ to indicate to the host that the command is complete (this action can be used to generate an interrupt on the host system). After the H/A responds with ACK, the controller deasserts REQ, BUSY and all other lines. This completes the command execution and the controller is now ready to be selected for the next command.

3.2.1 TIMING REQUIREMENTS FOR CONTROLLER SELECTION



NOTE: SEL must be deasserted before the controller will assert REQ.

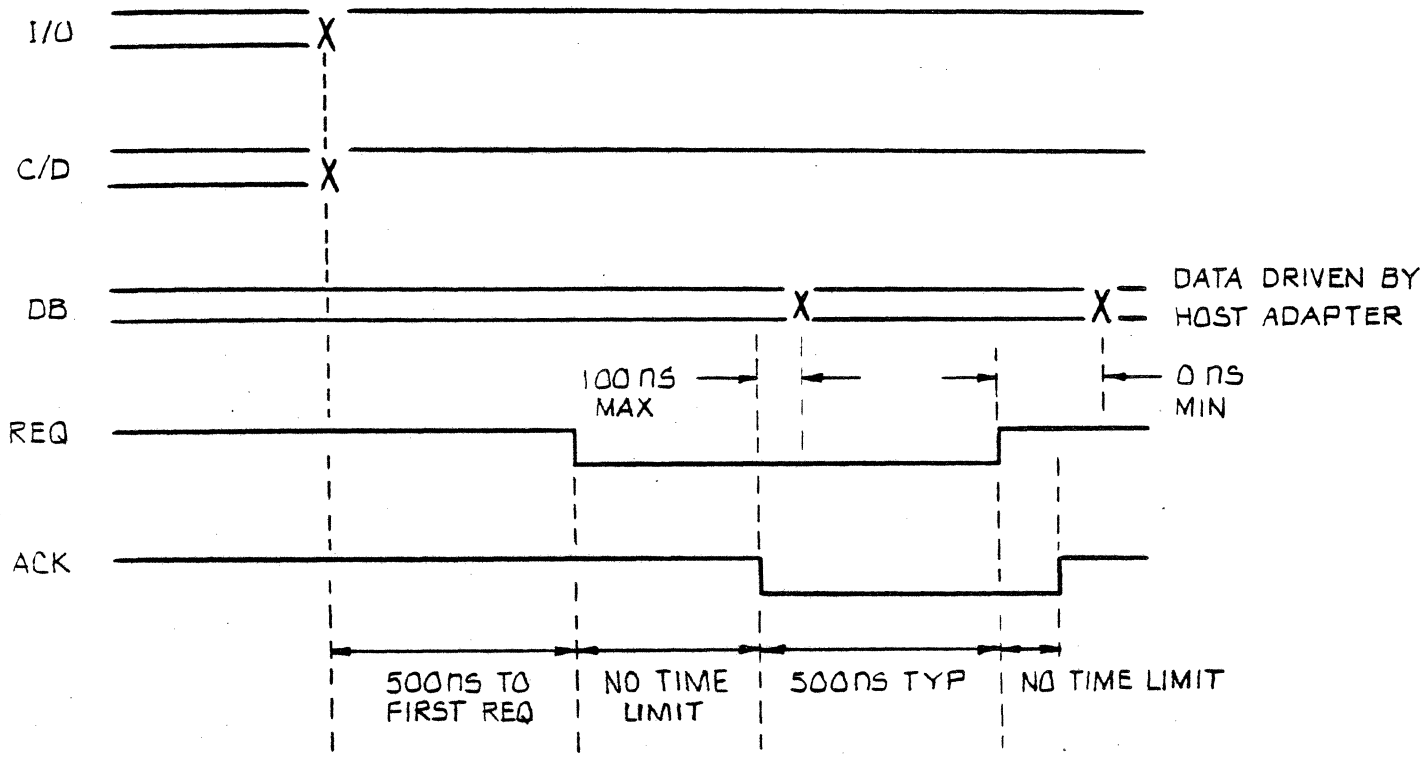
3.2.2 TIMING REQUIREMENTS FOR DATA TRANSFER
To Host Adapter - Typical Byte



NOTE: 1. For Status Byte Transfer (I/O, C/D asserted & MSG deasserted), or Interrupt Byte Transfer (MSG, I/O, C/D asserted), REQ is asserted 500ns (typical) after the assertion of any of the above bits.

2. Data driven by the controller is stable 100ns min at the host adapter end before REQ is asserted, and 100ns min after REQ is deasserted.

3.2.3 TIMING REQUIREMENTS FOR DATA TRANSFER
From Host Adapter - One Byte



NOTE: 1. Data driven by the host adapter must be stable 100ns (max) at the controller after ACK is asserted, and 0ns (min) after REQ is deasserted.

2. For command mode transfers, SEL must be deasserted before ACK is asserted. This sequence follows the selection protocol.

4.0 COMMANDS

An I/O request to a disk drive is performed by passing a command descriptor block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, number of blocks to transfer or the destination device ID. The controller performs an implied seek and verify when required to access a block.

Commands are categorized into three classes as indicated:

Class 0	-	Non-data Transfer, Data Transfer and Status Commands
Class 1	-	Disk Copy Commands
Class 2-6	-	Reserved
Class 7	-	Diagnostic Commands

The command descriptor blocks in Command Class 0 and 7 are 6 bytes long. and those in Class 1 are 10 bytes long.

Command Description (Class 0)

Opcode (Hex) — Description

00 — Test drive ready. Selects the drive and verifies drive ready.

01 — Recalibrate. Positions the R/W arm to Track00, clears possible error status in the drive.

02 — Request Syndrome. Returns the offset and syndrome for data field error correction. The two bytes are as follows:

Byte	7	6	5	4	3	2	1	0
0	M.S. BIT OFFSET (8)							
1	L.S. BIT OFFSET				SYNDROME			

The bit offset is relative from the first data bit, i.e., Bit 7 of Byte 0.

03 — Request Sense. This command must be issued immediately after an error. It returns 4 bytes of drive and controller sense for the specified LUN (see copy block for exception).

04 — Format Drive. Formats all blocks with ID field according to interleave factor and data fields. The data field contains 6C Hex.

05 Check Track Format. Checks format on the specified track for correct ID and interleave. Does not read the data field.

06 Format Track. Formats the specified track with bad block flag cleared in all blocks of that track. Writes 6C Hex in the data fields.

07 Format Bad Track (bad block flag). Formats the specified track with bad block flag set in the ID fields. Writes 6C Hex in the data fields.

08 Read. Reads the specified number of blocks starting from initial block address given in the CDB.

0A Write. Writes the specified number of blocks starting from initial block address given in the CDB.

0B Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drives capable of overlap seek.

Command Description (Class7)

Opcode (Hex)	Description
00	RAM Diagnostic. Performs a data pattern test on the RAM buffer.
01	Write ECC. Displaces data on the disk by three bytes so that the ECC bytes can be written from the data specified. Used to verify the ECC logic.
02	Read ID. Transfers the cylinder, head, sector and 3 ECC bytes for the specified block ID field.
03	Drive Diagnostic 0. Performs a drive diagnostic. Reads Sector 0 on all cylinders sequentially. Reads Sector 0 on 256 random cylinders.

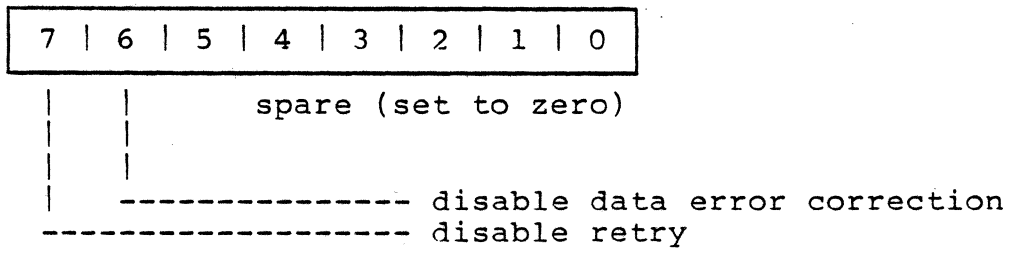
4.1 Command Format

4.1.1 Class 0 & 7 Commands

Byte	7	6	5	4	3	2	1	0
0	0 or 7			opcode				
1	LUN			logical adr2**				
2	logical adr1**							
3	logical adr0**							
4	number of blocks*							
5	control field							

*Interleave factor for Format, Check Track, and Read ID commands.
**Refer to section 4.3 Logical Address.

The control field is defined as follows:



Commands in this group

a) NOP
b) Format Drive
c) Check Format
d) Request Sense
e) Request Syndrome
f) Recalibrate
g) Read Block(s)
h) Read ID
i) Write Block(s)
j) Format Track
k) Format Track (bad track flag)
l) Seek
m) Ram Diagnostic
n) Drive Diagnostic
o) Write ECC

4.1.2 Class 1 Commands

Byte	7	6	5	4	3	2	1	0
0	0	0	1	opcode				
1	LUN/s			logical adr2/s*				
2	logical adr1/s*							
3	logical adr0/s*							
4	number of blocks							
5	LUN/d			logical adr2/d*				
6	logical adr1/d*							
7	logical adr0/d*							
8	spare							
9	control							

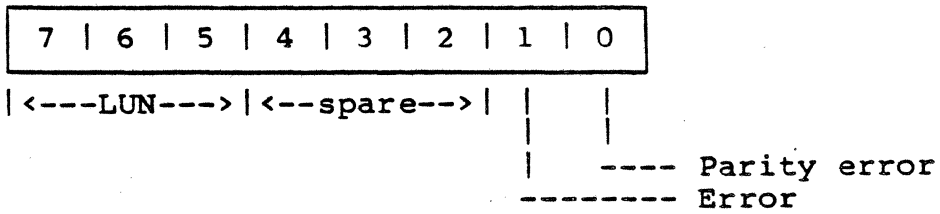
"s" = the source device, "d" = the destination device

*Refer to section 4.3 Logical Address

Commands in this group: Copy Block

4.2 Status Format

4.2.1 Completion Status Byte



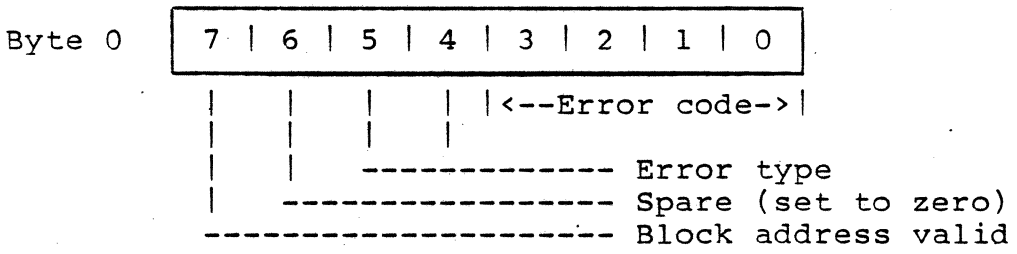
0	Parity error occurred during transfer from host to controller.
Bit 1	Error occurred during command execution.
Bit 2-4	Spare (set to zero).
Bit 5-7	Logical unit number of the drive.

4.2.2 Drive and Controller Sense Bytes

Byte	7	6	5	4	3	2	1	0
0	Sense Byte**							
1	LUN			logical adr2*				
2	logical adr1*							
3	logical adr0*							

*Refer to section 4.3 for Logical Address Computation

**Sense Byte is defined as follows:



Block Address Valid - Indicates that the Logical Sector Address in bytes 1 thru 3 contain the block at which the error occurred.

Error Type - Indicates the general type of error.

Error Code - The actual error interpretation.

LUN The Logical Unit Number of the erring drive.

4.3 Logical Address Computation

The logical address is computed as follows:

Logical adr = (CYADR * HDCYL + HDADR) * SETRK + SEADR

Where: CYADR = cylinder adress
HDADR = head address
SEADR = sector address
HDCY = number of heads per cylinder
SETRK = number of sectors per track

Bit 0 of Logical adr0 = the least significant bit.
Bit 4 of Logical adr2 = the most significant bit.

4.4 Error Code Descriptions

4.4.1 Sense Command Results

Type 0 (Drive) Error codes.

0	No status
1	No Index signal.
2	No Seek Complete.
3	Write fault
4	Drive not ready
5	Drive not selected.
6	No Track00
7	Multiple drives selected.

Type 1 (Controller) Error codes.

0	ID read error. ECC error in the ID field.
1	Uncorrectable data error during a read.
2	ID Address Mark not found.
3	Data Address Mark not found.
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	Unused.
7	Write protected.
8	Correctable data field error.
9	Bad block found.
A	Format Error. The controller detected that during the Check Track command, the format on the drive was not expected.

Type 2 (Command) Error codes.

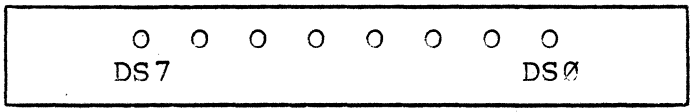
0	Invalid Command received from the host.
1	Illegal disk address. Address is beyond the maximum address.

Type 3 (Misc) Error codes.

0	RAM error. Data error detected during Sector buffer RAM diagnostic.

4.4.2 Error Display in LED's

The table below lists the error indications as displayed by the controller.



Error Code (HEX, DSØ is LSB)	Interpretation
ØØ	No Error
Ø1	No Index from drive
Ø2	No Track ØØ from drive
Ø3	Sector Address Out of Bounds
Ø4	ST5Ø6 not selected
Ø5	No Seek Complete from ST5Ø6
Ø6	No ID Address Mark
Ø7	No Data Address Mark
Ø8	Seek Error (Cylinder or Head not correct)
Ø9	Sector not found
ØA	ID ECC error
ØB	No ACK from Host Adaptor
ØC	Invalid Command
ØD	Incorrect DATA MARK
ØE	Incorrect ID MARK
ØF	Incorrect cylinder address from drive
1Ø	Incorrect sector address from drive
11	Incorrect head address from drive
12	Uncorrectable Data Error
13	Correctable Data Error
14	Drive not READY
15	Write fault
16	not used
17	Drive write protected
18	RAM diagnostic error
19 - 1F	not used
2Ø	Parity Error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad Block detected from drive
22	Invalid function for this type
81	Multiple ST5Ø6's selected. Fatal error.

5.0 ELECTRICAL/MECHANICAL SPECIFICATIONS

Physical Parameters

Width	8.0	inches
Length	12.0	inches
Height	0.49	inches
Weight	1.12	lbs.

Environmental Parameters

	Operating:	Storage:
Temperatureegree (degrees F/C)	32/0 to 131/55	-40/-10 to 167/75
Relative Humidity (@ 40 degrees F, wet bulb temp., no condensation)	10% to 95%	10% to 95%
Altitude	sea level to 10K feet	sea level to 15K feet

Power Requirement

Voltage @ current	+5 VDC @ 4.6A (max) +12 VDC @ 100 mA (max)

6.0 DIAGNOSTIC PHILOSOPHY

6.1 Error Indicators

The controller contains 8 diagnostic LED error indicators. Each time an error occurs the controller deposits a value in the LED's and returns a failure status to the host adapter. The LED value can be decoded, but the error it indicates will always be available to the host software. The errors that are returned by the controller are very detailed. As a result, preliminary fault isolation is made fairly easily, narrowing the failure to the particular interface portion of the controller. In addition, two diagnostic commands can be invoked via the host software interface. One is the RAM Diagnostic Command, and the other is the Drive Diagnostic Command.

6.2 Fault Isolation Microdiagnostics (Optional)

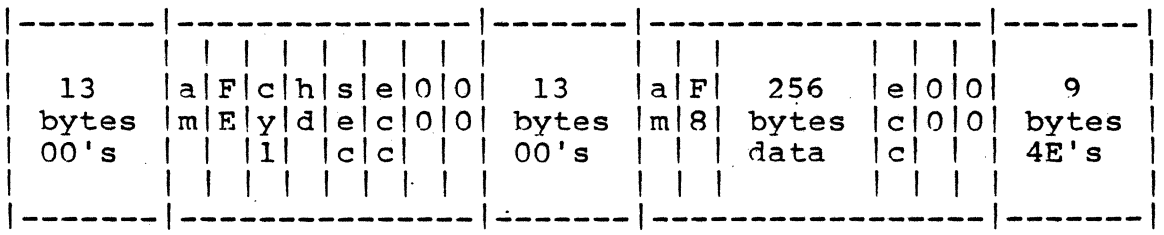
The controller can be further checked out off-line by initiating explicit microdiagnostic routines via optional firmware diagnostic sets. The routines are initiated by a set of control switches. Errors will be displayed in a set of LED's. Each microdiagnostic checks the functionality of a particular section of the controller and is able to isolate failures in the following major categories:

- ALU
- Registers
- Sector Buffer
- ECC Logic

Fault-isolation techniques can be concentrated on the failing section.

7.0 ST506 SECTOR FORMAT

The track layout for the ST506 (typical for 33 sectors) is shown below.



am, FE, cyl, hd, sec, 00, F8 = 1 byte
ecc = 3 bytes

Track Capacity = 10416 ± 1% (i.e., ± 104 bytes)

10164	= 308 x 33
16	= Index Gap (4E)
236	= Speed Tolerance Gap (4E)
10416	

308 bytes/sector including ID and overhead

Appendix A

Host I/O Connector Pin Assignment.

The Host I/O Bus uses a 50-pin connector (AMP P/N 2-87227-5 or equivalent). The unused signal pins are considered to be spares for future use. The pin assignments are as follows:

Signal	Pin Number	
DATA0	2	
DATA1	4	
DATA2	6	
DATA3	8	
DATA4	10	
DATA5	12	
DATA6	14	
DATA7	16	
PARITY	18	
--	20	-----
--	22	|
--	24	|
--	26	Future
--	28	Usage
--	30	|
--	32	|
--	34	-----
BUSY	36	
ACK	38	
RST	40	
MSG	42	
SEL	44	
C/D	46	
REQ	48	
I/O	50	

NOTE: All signals are negative true and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5V and 330 ohms to ground.

SH

DWG. NO.

APPENDIX B DTC-510 Controller Power Connections

1) +12V @ 500mA

2) GND

3) GND

4) +5V @ 4.0A

APPENDIX C Parity Jumper Setting

Jumper near connector J6:

A - B = enable parity

B - C = disable parity

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DATA TECHNOLOGY CORPORATION

CABLE CONNECTIONS FOR DTC510

1. Controller Board to Host Adapter Board

   Connector to Controller Board
   a. Type - 50 Pin Socket
   b. Location - J6

   Connector to Host Adapter Board
   a. Type - 50 Pin Socket
   b. Location - J3

2. Controller Board to HDD (B Cable)

   Connector to Controller Board
   a. Type - 20 Pin Socket
   b. Location - J2 or J3

   Connector to HDD
   a. Type - 20 Pin Cardedge
   b. Location - rear of unit

3. Controller Board to HDD (A Cable)

   Connector to Controller Board
   a. Type - 34 Pin Cardedge
   b. Location - J1

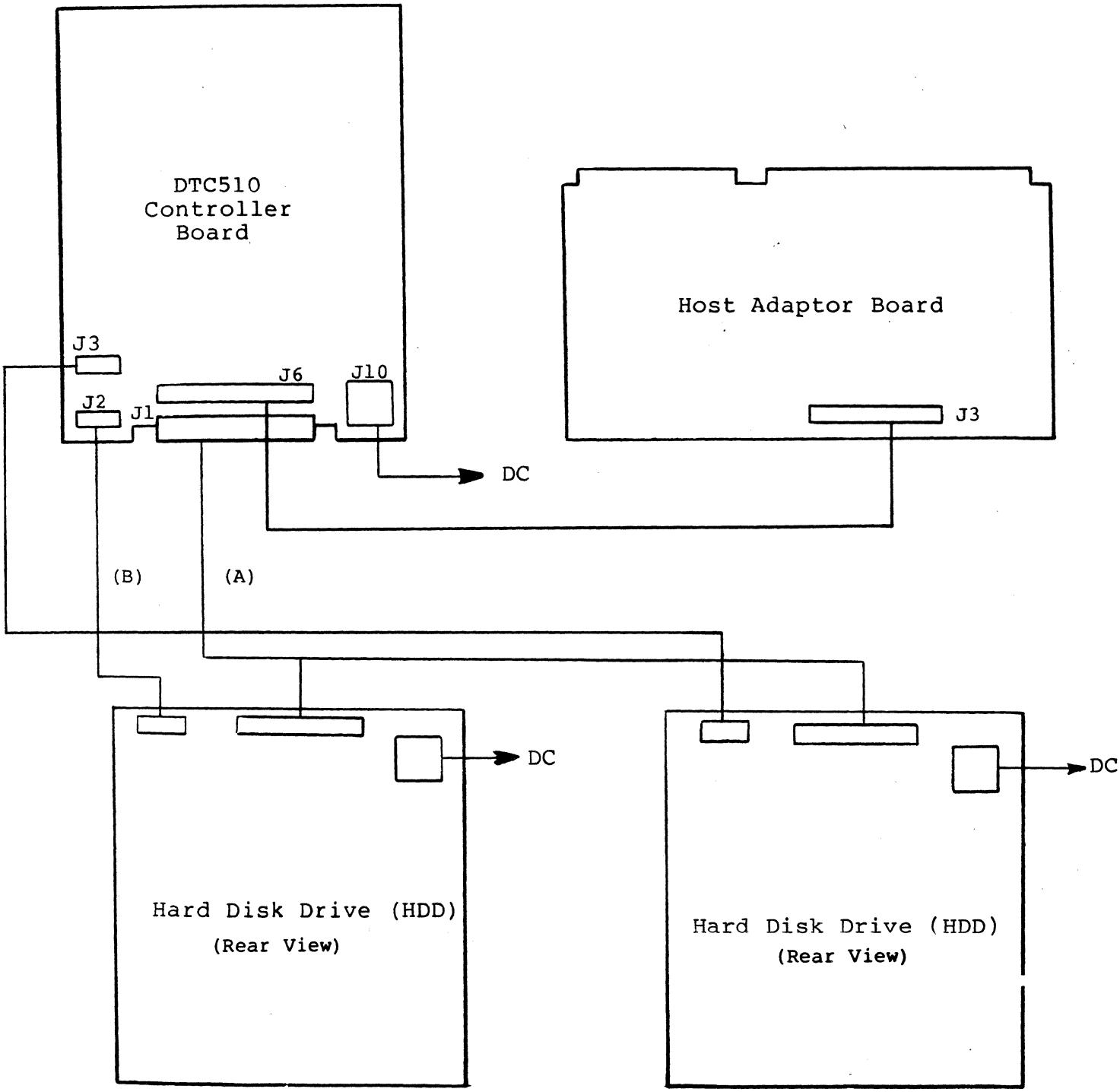
   Connector to HDD
   a. Type - 34 Pin Cardedge
   b. Location - rear of unit

4. DC Power (Controller, HDD)

   Connector to Controller Board
   a. Type - 4 Pin Plug
   b. Location - J10

   Connector to HDD
   a. Type - 4 Pin Plug
   b. Location - rear of unit

   Pin Assignments
   Pin 1: +12
       2: GND
       3: GND
       4: +5



CABLE CONNECTIONS

J2 — READ/WRITE CABLE

J3 — READ/WRITE CABLE

J1 — DISK DRIVE BUS CONTROL CABLE

J1			J2		J3	
2	RED WR CUR		17	MFMRD 0	17	MFMRD 1
6	WR GATE		18	MFMRD 0	18	MFMRD 1
18	HD SEL 1		1	SELECTED 0	1	SELECTED 1
14	HD SEL 0		15	MFM WR 0	15	MFM WR 1
32	DRV SEL 4		14	MFM WR 0	14	MFM WR 1
30	DRV SEL 3					
28	DRV SEL 2					
26	DRV SEL 1					
34	DIR IN					
24	STEP					
4	HD SEL 2					
8	SEEK COMPLETE IT					
20	INDEX					
22	READY					
10	TRACK 00					
12	WRITE FAULT					

TERMINATED WITH 220/330Ω

DATA SEPARATOR LOGIC

SERVO & READ CLOCK

17.36 MHZ CLOCK

WRITE CLK

READ, WRITE, CLOCK

RD DATA

WR DATA

2 BYTE CLR

VOC

DATA SEPARATOR

MFM GENERATOR W/ WRITE PRECOMP

CLOCK CONTROL LOGIC

BYTE & AM DET

SERIAL-IZER & ECC

SHR

DIP SWITCH

INPUT MATRIX

INST DECODE

BRANCH DECISION

2911

12 BITS

ROM

16 BITS

IR

OUTPUT MATRIX

ADRS

IRAM

ACC

F ALU

OUTPUT

8 BITS

OUTPUT BUS

OHR

DATA BUS

ADRS SECTOR BUFFER

D I/O

BUFFER

LEDS

DATA TRANSFER CONTROL LOGIC

DB 0	2
DB 1	4
DB 2	6
DB 3	8
DB 4	10
DB 5	12
DB 6	14
DB 7	16
PAR	18
I/O	50
DB 0	2
DB 1	4
DB 2	6
DB 3	8
DB 4	10
DB 5	12
DB 6	14
DB 7	16
PAR	18
I/O	50
REQ	48
C/D	46
MSG	42
BUSY	36
SELECT	44
ACK	38
BUSY	36
RESET	40

DATA BUS — HOST BUS

TERMINATED WITH 220/330Ω

ZONE	REV	DESCRIPTION	DATE	APPROVED

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN C. THEIN	12-18-86
CHECKED	
ISSUED	

SCALE

Data Technology Corporation

DTC 510
FUNCTIONAL BLOCK DIAGRAM

SIZE D | FSCM NO. | DWG. NO. 031-00001 | REV. B