# DZ80-80 CPU MANUAL 



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> THE DZ80-80 CPU

## INTRODUCTION

The DZ80-80 is a 4-inch square "Piggyback" PC card designed to upgrade an $8080 / 8080 \mathrm{~A}$ CPU microprocessor based system to a $\mathrm{Z}-80$ CPU system without requiring replacement of the system processor card. The Z-80 CPU is NOT electrically interchangeable with the 8080 CPU and has meant, until the DZ80-80, that to obtain the power of the nearly 690 instruction variations of the $\mathrm{Z}-80$, the 8080 processor card had to be discarded.

Nine integrated circuits and a bevy of passive components provide a network which interface the Z-80 CPU to the system's existing 8080 socket. An umbilical cord connects from the DZ80-80 to the system's existing 8212 status latch socket. Thereby providing Z-80 power by replacing only two ICs.

It is recommended that all included reference material be read prior to the installation of the DZ80-80. Since the Z-80 IC included is an MOS device, improper handling or installation can become an expensive education.

## THE Z-80 CPU

Included is the 'Z80 Technical Manual' written by the Z-80 design team. A thorough study and understanding of this Manual is a must to obtain full benefit of $\mathrm{Z}-80$ POWER.

## COMPATABILITY

As a subset of the $\mathrm{Z}-80$ instruction set is the 8080 instruction set. Therefore, programs written for the 8080 will execute identically on the DZ80-80 system with one minor exception.

The Parity flag of the 8080 is shared by a new Overflow flag on the Z-80 (see 'Z80 Technical Manual' for description). Some sophisticated software writers have been known to store information in the Parity flag and certain arithmetic instructions cause the Parity flag to react differently on the $\mathrm{Z}-80$ than the 8080. Therefore, in one or two rare instances, where the Parity flag is used for other than Parity, a minor incompatibility could exist (ALTAIR Basic is one rare instance). This is the only inconsistency found after extensive research.

Another difference between the DZ80-80 and the 8080 is that there is no provision for STACK status. As of this writing, no known hardware is available that would be inoperative without STACK status.

As a consolation the DZ80-80 provides the user an option to connect the STACK status line to the Z-80 Refresh signal, thereby allowing the DZ80-80 to perform all necessary refreshing of the system's dynamic memory.

One final note on compatability is when operating the DZ80-80 in an IMSAI, ALTAIR or other systems with a hardware front panel that is supposed to stop (when STOP is pressed) on an M1 cycle only, the DZ80-80 may stop on any random machine cycle. This occurs when the front panel samples the data lines during SYNC to decode M1 status rather than using the STATUS lines themselves. The DZ80-80 does not place STATUS on the data lines.

Panel switches EXAMINE, EXAMINE NEXT, DEPOSIT and DEPOSIT NEXT do not operate correctly unless the processor is in an M1 cycle. It is thus required to single step the processor to an Ml cycle before operating the previously mentioned panel switches after a STOP. (RESET while STOP will always generate an Ml cycle.)

This idiosyncrasy has been found not to be a problem once the operator becomes used to checking for Ml before pressing EXAMINE. It was felt that the extra cost that would have been incurred by the end user did not warrant the addition of hardware to eliminate this inconvenience.

DZ80-80

## THEORY OF OPERATION

As noted in the 'Technical Manual' the $\mathrm{Z}-80$ does not provide many of the signals required for the operation of an 8080 system. Namely SYNC, INTE, DBIN, INTA, OUT, INP and MEMR had to be generated from the Z-80 System Control Signals IORQ, MREQ, RD and M1.

The system $\$ 2$ clock was chosen to generate the $\Phi$ clock for the $\mathrm{Z}-80$ since the specification for $\$ 2$ is compatible with the $\Phi$ clock specification and no system timing change occurs for this choice. $\Phi 2$ is a 12 v clock, unlike the 8080 the $\mathrm{Z}-80$ requires a single 5 V supply and no high voltage clocking. Diode CR1 and resistor R1 shift the $\Phi 2$ clock to a 5 V signal which is double inverted by IC5 and derives $\Phi$ with pull-up resistor R2. R2 is included to insure that $\Phi$ has a High of 5 V as required by the $\mathrm{Z}-80$.

System SYNC (beginning of each machine cycle) is created as one $\Phi$ period beginning when both IORQ and MREQ are False by NAND gate IC3, inverter IC5 and JK flip flop IC6 clocked by $\Phi$. IC5 output, SYNC, is used to gate $\overline{W R}$ and $\overline{W O}$ to insure that time is available for the system to decode OUT status before WR becomes active during a write operation.

Status INP is the AND of RD and IORQ implemented by NOR gate IC7. Status OUT is IORQ ANDED with WR using NOR gate IC4. The status signal INTA is M1 AND IORQ with NOR gate IC4 acting as the AND function.

Status MEMR is formed with NOR gate IC7 as RD AND MREQ. The remaining two implemented status signals, Ml and HLTA, are merely the inversion of $\mathrm{z}-80$ outputs $\overline{M T}$ and HALT by IC2 and IC3, respectively.

The Z-80 does not provide any indication when it is performing a STACK operation, therefore, the STK status has not been provided. The DZ80-80 is assembled with a jumper from the STACK status input to ground. At the user's option this jumper may be connected to the Z-80 RFSH output thus providing the system with automatic dynamic memory refresh. See 'Z80 Technical Manual' for a discussion of this subject.

No external indicator is provided by the $\mathrm{Z}-80$ as to the state of the internal Interrupt Flip-Flop. Thus NAND gate IC1, Inverters (2) IC2 and NORs (2) IC4 decode each EI and DI instruction on the falling edge of M1 and store this information in Flip-Flop IC6 providing the INTE signal. System

RESET or Status INTA will set IC6 through NOR gate IC7 indicating INTE False. IC7 then parrots the state of the internal Z-80 Interrupt Flip-Flop.

DBIN is implemented as RD OR INTA by NAND gate IC3 and NOR gate IC7. Notice that DBIN is True also during System RESET. This is not a system requirement but included only to save an IC package. It was determined that DBIN True at RESET time would not degrade performance and create a physically smaller DZ80-80 assembly.

A potentially powerful feature of the $\mathrm{Z}-80$ is its handling of the high order address lines during I/O operations, refer to the 'Technical Manual' for a discussion. Most existing 8080 systems, however, have used A8 through Al5 for I/O addressing and this feature could not be included in the DZ80-80. (If this feature is desired IC8 and IC9 can be removed and A3 through Al5 strapped straight through.)

Multiplexers IC8 and IC9 are connected between the Z-80 and 8080 system address lines such that during status INP or OUT NOR Gate IC7 causes A8 through Al5 to contain the same data as AO through A7.

The Z-30 $\overline{\mathrm{NMI}}$ (Non-Maskable Interrupt) line has been brought to a solder pad on the DZ80-80 so the user may connect this to, say VIO. This connection would mean VIO is the ultimately highest priority interrupt.

As noted on the DZ80-80 schematic the remainder of the Z-80 to 8080 system interface is either by straight connection or by simple inversion and need not be dwelled upon.

With tho oxcoption of the right status lines (and NMT) all DZ80-80 connections are made through the system's 8080 socket. Connector J2 provides the connection of the status to the system via Plug P2, 8 conductor flat cable, 24 -pin connector, connector J3 to the system 8212 status latch socket ( 8212 is removed). The flat cable is permanently attached and wired to J3 pins $4,6,8,10,15,17,19$, and 21 , the output pins of the 8212 .

Marked on J2 are two different positions
P2 can be plugged in, POSition A and POSition B,

J2 Pins 9 and 10 unconnected,
J2 Pins 1 and 2 unconnected,
respectively.

There is no conformed to standard which sets the status signal to 8212 pin relationship. However, two different and often used pin-outs have been observed and those are included as POSition $A$ and POSition $B$ :

> POS A - ALTAIR Position
> POS B - IMSAI Position

In the event another pin-out is required, the pins of plug P2 maybe removed and scrambled to fit the user's requirements (see INSTALLATION and CHECKOUT section).

$$
\backsim
$$

$$
\cup
$$

THE Z-80 CPU IN THE DZ80-80 IS AN MOS DEVICE AND IT IS IMPERATIVE THAT THE MOS PRECAUTIONS ON THE REVERSE SIDE OF THE PARTS LIST BE FOLLOWED. THE DEVICE WARRANTY WILL BECOME VOID IF THESE ARE NOT ADHERED TO.

1. If the DZ80-80 was obtained as a semi-kit (integrated circuits not installed in their sockets and shipped in separate containers) remove J3 from IC10 socket (shipped there to protect the pins) by carefully prying it up with a small screwdriver or pen knife. DO NOT remove the conductive foam from Jl until ready to install the DZ80-80 on the processer card. Skip to Step 4 if the IC's are already installed.
2. Install ICl through IC9 in their sockets as directed by the DZ80-80 PC card legend silk screen, the dot indicates Pin 1. Refer to DIP INSERTION on the reverse side of the Parts List.
3. Install IC10, the Z-80 CPU, observing MOS PRECAUTIONS.
4. Turn the Process System Power Switch to OFF and remove the Processor Card.
5. From the Processor Card remove the 8080 CPU If (etoxs in a otatio froo sarixiox) and tho gate IC. If tho 8212 is soldered-in, cut off each pin at the IC and unsolder the pins one at a time. (It is NOT recommended that the 8212 be saved by desoldering it. There is too big a change of board damage unless the proper desoldering tools are available.) Install a 24 -pin socket if required.
6. Orient the DZ80-80 connector Jl over the processor card CPU socket (Observe Pin 1 orientation) and check for any bypass capactiors that may interfere with the DZ80-80 installation. Bend these over on the processor card as required.
7. Attach P2 to J2 with top of P2 showing (no holes) as follows: (Pins 9 and 10 of J2 not connected) POS A - ALTAIR configuration; (Pins 1 and 2 of J2 not connected) POS B - IMSAI configuration. Skip to Step 8 if interfacing to ALTAIR or IMSAI.

When it is required to interface to other than the two systems shown, it will be necessary to reconfigure P2 by removing its pins and re-inserting them in the dictated order. Refer to the Processor Card documentation and check the signal name to 8212 output pin relationship and compare to the table below.

| J2 Pin Number | Status <br> Signal | Flat Cable Wire Color | J3 Pin Number (8212 Output Pin) |
| :---: | :---: | :---: | :---: |
| 1 | INTA | GRY | 15 |
| 2 | WO | PUR | 17 |
| 3 | OUT | BLU | 10 |
| 4 | MI | GRN | 8 |
| 5 | HLTA | YEL | 21 |
| 6 | STACK | ORG | 19 |
| 7 | MEMB | RED | 4 |
| 8 | INP | BRN | 6 |
| 9 | INTA |  |  |
| 10 | $\overline{\text { WO }}$ |  |  |

The P2 pins are removed by pressing on the locking tab and sliding them out. (Not an easy operation, but possible.) Re-insert the P2 Pins such that the order matches the 1 to 8 order of J2 as seen in Table left, above. Connect P2 in POS A.
8. Remove the conductive foam from the DZ80-80 Jl canve and reinstall any time the unit is not connectod to the processor card) and observing MOS PRECAUTIONS install the DZ80-80 in the 8080 socket.
9. Connect J3 to the 8212 socket, insure proper Pin 1 orientation, pin numbers are molded into J3.
10. Recheck all previous steps, any error could result in $Z-80$ damage.
11. Install the Processor Card in the system and dress the flat cable. It may be necessary to leave one blank card slot in front of the Processor Card if there is interference.

## CHECKOUT

A quick check of operation can be made by testing the front panel functions DEPOSIT and EXAMINE. With these operational the

DUTZ MONITOR can be loaded and the system given a workout.
In the event the system does not perform as indicated on initial start-up, power down immediately and recheck methodically every step of the installation procedure. Performance will be unpredictable if the status cable or ICs are installed incorrectly.

If all attempts at curing a problem fail, contact the supplier or the Factory for assistance.

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THE DUTZ MONITOR

## GENERAL

V1.0 of DUTZ MONITOR is a 1 K page relocatable (able to be loaded at the beginning of any 1 K memory page) program to be used for initial DZ80-80 check out and as a system and program debug and evaluation tool. DUTZ V1.0 executes thirteen commands and is capable of expansion limited only to memory availability and the users desires and ingenuity.

It has been assumed that the minimum user I/O configuration will be a Teletype with paper tape option. Two sets of I/O drives are included to allow for a Command Console I/O and File $\mathrm{I} / \mathrm{O}$.

The Command I/O is the Input-Output device from which the user issues and receives response from the instruction Command Set. This device is a keyboard input $I / O$ such as a Teletype or CRT with keyboard.

The File I/O is a serial Input-Output device such as a paper tape reader and punch or a tape recorder. The I and $O$ Commands use the File drivers and the remainder use the console drivers. The MONITOR as received is, as indicated in the MONITOR LOADING section, for Console and File I/O to be the same device, but may be changed to the users configuration.

## COMMAND SET

Tho following 13 onc or two character commands direct the DUTZ Vl.0 Monitor to perform the described operations.

Definitions: TR - Terminator any of CR (carriage return)
or SP (space bar) or , (comma) or $\uparrow(\wedge)$.
(A1) or (A2) or (A3) - *4 Hexidecimal (Hex) digit memory address, will default to zero if none entered, if more than four digits are entered the last four will be used.
(OA) - Same as above except optional (need not be entered). When option is not taken the preceeding $T R$ must be replaced with a CR.

[^0](H) - *2 Hex digit number, if one entered a preceding zero is assumed, if more than one is entered the last 2 will be used.

COMMAND

## DESCRIPTION

Abort present directive and return control to Monitor, a ? will be output to the console indicating an abort and on a new line the prompter Z will be displayed to indicate the monitor is ready for a new command.
Note: $Z$ is not effective during an I (Input) operation (command I/O could be the same as File $I / O$ ) an abort is automatically entered if there is no File data received for about 3 seconds.

D (A1) TR (A2) TR
DUMP memory locations (A1) through (A2) on the command device. Each location is presented as two Hex digits 16 per line with each line beginning with the Hex address of the first location in that line.

E(Al)CR
EXECUTE starting at memory location (A1), if the program that is executed ends with a RET instruction control will be returned to the Monitor.
$\mathrm{H}(\mathrm{A} 1) \mathrm{TR}(\mathrm{A} 2) \mathrm{TR}$
HEX arithmetic, the following will be display:

$$
[(\mathrm{A} 1)+(\mathrm{A} 2)], \quad[(\mathrm{A} 1)-(\mathrm{A} 2)]
$$

$\operatorname{IB}(\mathrm{Al}) \mathrm{TR}(\mathrm{OA}) \mathrm{CR}$
INPUT BINARY file starting at memory location (Al) and Abort if location greater than ( $O A$ ) is reached. If the Optional (OA) is not used $C R$ must replace $T R$.

Place the Binary File (Paper tape etc.) in the File Input device starting with the NULL leader, input the command and start the device. The BELL will sound once to indicate the file is loading. (See Appendix for Binary File format.)

[^1]IL

IL( OA ) CR
INPUT LOADER file (also called HEX file or Intel format file, see Appendix for format). If the Optional Address (OA) is included (OA) will be added to the address indicated on the file to compute the load address of the data as it is loaded, thus allowing the user to load a file anywhere in memory.
This command will load either check summed or non check summed Loader files. An abort is executed if a check summed file contains a check sum error or a non Hex character other than a: Record cue in the correct position. Use the IB load procedure for IL.
Command will return to the Monitor when an EOF is found. (See Appendix).

M (Al) TR
MODIFY memory location (A1). The Monitor will respond with the address (Al) followed by the two Hex digit value stored at (Al) and wait for the users next entry.
To modify the displayed location enter
(H) SP
and the Monitor will respond with a * to indicate the location has been altered and display the address and value of the next sequential location and wait. If only $S P$ is entered the next location will be displayed without altering the first.
Return to Monitor can be accomplished at any time by entering $C R$ or $Z$. To display the location one less than the one displayed enter $\uparrow$ (^). No alteration of memory will occur on a $\uparrow$ command.

OB (A1) TR(A2)CR
OUTPUT BINARY format to the File I/O from memory address (A1) thru (A2). (See Appendix for format)
Command may be aborted by entering $Z$.
Enter the command except for the CR, turn on the File Output device (punch etc.) and enter CR.

OL

R

S

T

V

OL(A1)TR(A2)TR(OA)CR
OUTPUT LOADER format to File I/O device from memory location (A1) through (A2), if (OA) is included output an EOF containing (OA) (for ID or starting address), if (OA) is not included no EOF or Null Trailer will be output. (More records to come.)
Command may be Aborted by entering Z.
Follow the OB procedure.

V(A1)TR(A2)CR
VERIFY memory locations (A1) through (A2) for hardware errors. Upon finding an error the $M$ (modify) routine is entered and the error location is displayed with all functions of the $M$ routine active; the user can then

V (continued) evaluate the nature of the error. To complete verification enter CR, to return to the Monitor before address (A2) is reached enter $Z$.

This command is not intended to be used as a comprehensive memory test, it may be used to locate gross memory errors such as a stuck bit, protect on, or no memory at an address.
DO NOT Verify the memory containing the Verify routine as it can modify itself.

The Monitor has been punched on paper tape in a modified Hexidecimal Format preceded by a Binary Format Relocating Load Routine. The Loader is bootstrapped in using the following 21 word Binary Loader.

| 0000 | 2.1 | AF | 01 | LXI H,OIAFH | REVERSE LOAD ADDR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0003 | DR | 00 | INCH | IN STP | STATUS PORT |
| 0005 | EE | FF |  | XRI PMK | FF FOR RDAV TRUE |
| 0007 | E6 | 40 |  | ANI BMK | BIT MASK |
| 0009 | 20 | F8 |  | JRNZ INCH | JMP NONE AVAILABLE |
| 0008 | DB | 01 |  | IN IPT | INPUT PORT |
| 000 D | BD |  |  | CMP L | TEST FOR CUE |
| OOOE | 28 | F3 |  | JRZ INCH | JMP STILL CUE |
| 0010 | 2 D |  |  | DCR L |  |
| 0011 | 77 |  |  | MOV M, A | STORE IT |
| 001 ? | 20 | EF |  | JRNZ INCH | JMP NOT DONE |
| 0014 | E9 |  |  | PCHL | EXECUTE REL LOADER |

The preceeding BOOT must be manually loaded at 0000. The uoor muat oupply tha propor statuc part (STD). Polarity Mask (PMK) (FF for Data Available-True, Oo for Data Available-False), Bit Mask (BMK) and Input Port (IPT) for the loading device.

Once the BOOT is entered and verified:

1. Select the desired load address on the processor panel sense switches. (Only SSAlO through SSAl5 are sampled to obtain a 1 K page boundry.) The Monitor was designed to be located at the highest available memory location, but maybe located at any 1 K boundary except 0000 ( 0000 contains the Relocating Load Routine).
2. Press Processor RESET.
3. Place the DUTZ MONITOR tape in the Reader with the Hex AF record cue under the read head.
4. Start Reader.
5. Press processor RUN.

The section of tape following the Hex AF record cue is the Relocating Loader which is read in at location 0100 and self-relocates to 0000 around the input routine manually loaded.

Once the Loader relocates to 0000 the INTE LED on the processor panel will light indicating that the Loader has entered correctly. If the INTE LED does not light at the section of NULLS on the Monitor tape (about 2 feet in) the Loader did not get in correctly and the whole Load Procedure must be repeated.

Once the tape has read to the NULLS and the INTE LED is lighted a checksumed Relocatable Hex File is being read. At this time an error is indicated by the flashing of the INTE LED (about 2 cycles per second). This can occur for the following reasons:

1. The Sense Switches are set at zero (remember SSA8 and SSA9 are not used). REMEDY: Stop Reader, set switches to a nonzero value, back tape to NULL, restart reader and press RESET while reader is still reading NULLS.
2. Due to a read error, a non-Hex or wrong character is read indicated by a checksum or non-Hex character error. REMEDY: Stop Reader, back tape 2-3 feet (a guess of where the record before the error occurred is located), restart Reader and press RESET.

A properly loading program is indicated (not positively) by a non-flash lighted INTE LED.

Chances are quite good that DUTZ MONITOR as received will not have the Command Console and File I/O configuration required by the user's Processor System. Each user will have made assignments to fit system needs that may follow no universal standard (even if there were one).

With this in mind the EOF (End Of File) indicator on the DUTZ MONITOR tape has been separated from the end of the last record by about 6 inches of NULLS. The EOF causes the Loader to branch to the beginning of the MONITOR for automatic start-up.

When the tape reaches these NULLS the reader may be stopped and a patch tape inserted to patch the four I/O drives to match the user's system assignments. If the user doesn't stop the tape before EOF is read and the system is set for different $I / O$ and Status Ports, Polarity and Bit Masks the program will be in a waiting loop. At this point the I/O drivers may be modified via the Front Panel Switches or the patch tape maybe put in the reader and with NULLS being read followed a press RESET. If the patch contains an EOF the MONITOR will sign on with a ? followed by the MONITOR name and version number.

See Appendix for patch tape preparation.

The following table defines the I/O assignments of the DUTZ MONITOR as received and the addresses and values to be changed when reconfiguring the MONITOR to fit the user's system.

| FUNCTION | ADDRESS* | VALUE | CHANGE TO |
| :---: | :---: | :---: | :---: |
| Console Input |  |  |  |
| Status Port | 0004 | 00 | Desired Port |
| Console Data |  |  |  |
| Available | 0006 | FF | FF for True High |
| Polarity Mask |  |  | 00 for True Low |
| Console Data |  |  |  |
| Available | 0008 | 40 | Set to zero all |
| Status Bit |  |  | bits but the de- |
| Mask |  |  | sired (uses an ANI instruction) |
| Console Input |  |  |  |
| Port | 000B | 01 | Desired Port |
| Console Output |  |  |  |
| Status Port | 002E | 00 | Desired Port |
| Console Output | 0030 | FF | FF for True High |
| Not Busy Polar- 00 for True Low |  |  |  |
| ity Mask |  |  |  |
| Console Output |  |  |  |
| Status Bit Mask | 0032 | 80 | Set to zero all |
|  |  |  | bits but the deoired (uses an |
|  |  |  | ANI instruction) |
| Console Output |  |  |  |
| Port | 0037 | 01 | Desired Port |
| File Input |  |  |  |
| Status Port | 003E | 00 | Desired Port |
| File Data |  |  |  |
| Available | 0040 | FF | FF for True High |
| Polarity Mask 00 for True Low |  |  |  |
| File Data | 0042 | 40 | Set to zero all |
| Available |  |  | bits but the de- |
| Status Bit Mask |  |  | sired (uses an |

VALUE
FUNCTION ADDRESS* AS RECEIVED CHANGE TO

File Input
Port 005401 Desired Port

File Output Status Port

0019
00
Desired Port
File Output

| Not Busy | OO1B | FF | FF for True High <br> Polarity Mask |
| :--- | :--- | :--- | :--- |

File Output
Status Bit Mask 001D
80
Set to zero all bits but the desired (uses an ANI instruction)

File Output Port

0022
01
Desired Port

[^2]
## PATCH TAPE PREPARATION

A patch tape is prepared by punching a tape with one or more of the following:

PATCH NUMBER
(Don't punch reference only)

| 1 | $: 01000403 X X Y Y$ |
| :--- | :--- |
| 2 | $: 01000603 X X Y Y$ |
| 3 | $: 01000803 X X Y Y$ |
| 4 | $: 01000 B 03 X X Y Y$ |


| NOTES |  |
| :--- | :---: |
| Replace XX <br> in HEX by | Replace YY <br> in HEX by |
| Console Input <br> Status Port <br> Number | $-(08+X X)$ |
| Console Input <br> Polarity | $-(0 A+X X)$ |
| Console Input <br> Status Bit Mask | $-(0 C+X X)$ |
| Console Input <br> Port Number | $-(O F+X X)$ |

:01002E03XXYY

6 :01003003XXYY
:01003203XXYY
:01003703XXYY

9

| 10 | $: 01004003 X X Y Y$ |
| :--- | :--- |
| 11 | $: 01004203 X X Y Y$ |
| 12 | $: 01005403 X X Y Y$ |

13
:01001903XXYY
File Output
Status Port Number
$-(1 D+X X)$

PATCH NUMBER
(Don't punch

| NOTES |  |
| :--- | :--- |
| Replace XX <br> in HEX by | Replace YY <br> in HEX by |
| File Output <br> Polarity | $-(1 F+X X)$ |
| File Output |  |
| Status Bit Mask | $-(21+X X)$ |
| File Output <br> Port Number | $-(26+X X)$ |

Only those $I / O$ assignments that differ from the MONITOR Tape as received need be patched. As an example suppose that a particular system with Teletype I/O only requires the following I/O configuration:
A. Input and Output Status Port : Port 00
B. Input and Output Port : Port 01
C. Read Data Available : Bit 4, Low
D. Transmit Buffer Empty : Bit 5, Low

A check of the I/O Assignment Section of this Appendix shows that the MONITOR is now set for

| A. | Port 00 |
| :--- | :--- |
| S. Port 01 |  |
| C. | Bit 6, High |
| D. | Bit 7, High |

Therefore only C and D need be changed. Scanning the Patch List it is seen that this requires Patch Nos. 2, 3, 6, 7, 10, 11, and $14,15$.

Patches 2 and 10 set the Status Bit Polarity, the MONITOR requires an active low indicator thus the status word is exclusive OR'd with either 00 or $F F$ to achieve this. Therefore both Patches 2 and 10 require an 00 substituted for the XX in the list. Next the check sum YY must be calculated, this is defined as the negative (ignoring carry outs, i.e. maintain an 8 -bit word) of the sum of the HEX digit pairs (l Byte) in the record.

The Patch List shows the sum of the bytes with the exception of XX, i.e. for Patch 2:

$$
\begin{aligned}
& 01 \\
& 00 \\
& 06 \\
& 03 \\
& \mathrm{XX} \\
& \hline 0 \mathrm{~A}+\mathrm{XX}
\end{aligned}
$$

thus $Y Y=-(0 A+X X)=-(0 A+00)$, for $X X=00$ and $Y Y=$ $-(O A)=F 6$ and Patch 2 becomes
:0100060300F6
and likewise Patches 3, 6, 7, 10, 11 and 14,15 are

| Patch 3 | $: 0100080310 \mathrm{E} 4$ |
| :--- | :--- |
| Patch 6 | $: 0100300300 C C$ |
| Patch 7 | $: 0100320320 \mathrm{AA}$ |
| Patch 10 | $: 0100400300 \mathrm{BC}$ |
| Patch 11 | $: 0100420310 A A$ |
| Patch 14 | $: 01001 \mathrm{B0300E} 1$ |
| Patch 15 | $: 01001$ D0320BF |
| EOF | $: 000000$ |

In the preparation of the above example the DUTZ MONITOR H command was used to calculate the checksum, we cheated!

The foregoing procedure is tedious and time consuming, nowever, once completed and verified it need not be repeated until the system configuration is changed and the MONITOR will automatically start after loading.

One way to limit the amount of work required is to calculate by hand the Console Patches and get the MONITOR on line and use it to aid in the calculation of the File Patches.

## FILE RECORD FORMATS

1. Binary Record read by DUTZ IB command or Output by OB command:

Record Cue (identify beginning of record) - 4 or more FF (all 8 bits 1 words as single binary 8-bit word per FF.

Record Data - Single binary 8-bit word per data word, a direct copy of the binary data word.

EOF (End of File, in this case Record) - Exactly 8 binary FF words as in Cue.
2. HEX or Loader Record read by DUTZ IL command or Output
by OL command:
Record Cue -:(single word 3 A in binary)
Header - NN (2-ASCII HEX characters defining the number of Data Bytes in the record in Hexidecimal)

AAAA (4-ASCII HEX characters defining the 2-byte starting address the data is to be stored.)

Record Type - 00 (2-ASCII zeros, absolute record type 0)

Data - HH (2-ASCII HEX characters per byte of data)
Checksum - CC (2-ASCII HEX characters equal to the negative of the binary sum of all of the Data bytes the Record Type bytes and the three Header bytes during the summation all carry outs are ignored, i.e. modulo 256.)
3. DUTZ Sense Switch Relocatable Record read by relocating BOOT STRAP LOADER.

Record Cue -:(single word 3 A in binary)
Header - Same as Loader Record
Record Type - 00 or 03 (In ASCII)
Data - Same as Loader Record except an ASCII R is the first character of a Data byte that is to be relocated (the value of the 6-MSB Sense Switches are added to the Data bytes before storing.)

```
Checksum - Same as Loader Record with R taken as 0 .
```

4. End of File (EOF)Record indicating EOF of a string of Loader or Relocatable Records.

Record Cue - Same as Loader Record
Header - 00 (2-ASCII zeros, no-data)
AAAA (4-ASCII HEX characters indicating program entry address or program identification, most often zeros).

## STATEMENT OF WARRANTY

DUTRONICS, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by Dutronics are obtained through recognized factory distribution channels and any part which fails due to defects in manufacture or material will be replaced on an exchange basis, free of charge, for a period of 90 days following the date of purchase.

Any malfunctioning module returned to Dutronics within the warranty period, which in the judgement of Dutronics has been installed and used with care and not subjected to electrical or mechanical absue, will be restored or replaced at Dutronics discretion and returned, with a minimal charge to cover packaging and shipping.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to repair or replacement of the module involved.

## DZ80-80 SEMI-KIT PARTS LIST

| 1 each | DZ80-80 Manual |
| :---: | :---: |
| 1 each | Assembled (No ICs installed) DZ80-80 PC Card |
| 1 each | IC1 - 74LS30 IC |
| 1 each | IC2 - 74LS04 IC |
| 1 each | IC3 - 74LSOO IC |
| 2 each | IC4, IC7 - 74LS02 IC |
| 1 each | IC5 - 7404 IC |
| 1 each | IC6 - 74LSI12 IC |
| 2 each | IC8, IC9 - 74LS157 IC |
| 1 each | IC10 - Z80 CPU (MOS) |
| 1 each | Z02 Status Cable Assembly |
| 1 each | 1-1/2 inch Binder |

## DZ80-80 SPECIFICATIONS

Size: $\quad 4$ inches x 4 inches ( $10.16 \mathrm{~cm} \times 10.16 \mathrm{~cm}$ )
Weight: $\quad 3 \mathrm{oz}$ ( 85.05 gm )
Operating Temperature: 0 to $70^{\circ} \mathrm{C}$.
Power Requirements: $\quad \mathrm{VCC}=5 \mathrm{~V} \pm 5 \%$
ICC $=190 \mathrm{~mA}$ TYP, 280 mA MAX, Net increase when replacing 3080A and $8212=50 \mathrm{~mA}$ TYP
Interface: Jl - 8080/8080A Pin-Out
J3 - 8212 Pin-Out

## CONSTRUCTION HINTS

## SOLDER DO'S AND DON'TS

1. MOST IMPORTANT: The solder supplied with your kit is the highest quality $60 / 40$, resin-core solder. DO NOT under any circumstances use acid core solder or paste or liquid flux. Any of these will cause unrepairable damage to your PC board and components.
2. DO use a small diameter, low wattage soldering iron, 18 watts is sufficient--no greater than 25 watts. DO NOT use a soldering gun, they are too hot and clumsy!
3. DO keep your soldering iron clean. A damp sponge is a handy cleaning aid.
4. DO NOT PRESS a hot iron on a PC board land or trace. If you do you will watch the copper peel off the board!
5. DO keep the working part of the iron tip well tinned. Touch tip of iron to parts to be soldered while applying solder to combination, solder will flow and heat joint. Use enough solder to just cover the contour of the joint, remove solder and leave iron until resin boils out, about $2-3$ seconds. ICs are speced at a max soldering time of 10 seconds.
6. DO be careful of solder bridges between traces -- bridges are the most frequent problem when the initial equipment test fails -- even with professionals! After every step in assembly, carefully inspect for bridges and missed solder points -- the second most frequent problem. Use a solder wick or vacuum bulb to remove bridges and blobs.

## DIP INSERTION

1. Dual In-line Packages are uniquely embossed or marked to indicate $P$ in No. 1. This marking can take the form of a small dot over $P$ in 1, elongated half circle or full circle at the end of the package containing Pin I. Whatever the marking, it will be over Pin No. I when the DIP is oriented such that the marking is on the left. Pin count then increases counterclockwise around the DIP.
2. Most DIP packages are manufactured with the pin spacing greater than the board lay-out spacing to facilitate automatic machine insertion and soldering. If you have access to an insertion tool, use it; if not, insert the pins on one side about $1 / 3$ and exert pressure on the opposite side until the pins align with the holes, then press down. Use a strip of masking tape to hold several packages down while soldering from the bottom of the board. All components are inserted from the top of the board and soldered from the bottom unless specifically stated otherwise.
3. BE SURE to check DIP orientation and location before soldering. If one is soldered in the incorrect position, it is tedious to remove. If this happens, it is usually best to remove the IC by cutting off the pins and unsoldering the cut pins one at a time. Unless you have had experience unsoldering DIPs you will probably destroy the PC board as well as the DIP anyway. The DIP is inexpensively replaced comipared to the whole circuit.

## MOS PRECAUTIONS

All MOS devices, so indicated on the parts list as (MOS), are more or less susceptible to destruction by static electric discharge. The following precautions should be taken:

1. Wear cotton rather than synthetic clothing while handling MOS devices.
2. DO NOT allow household pets in the vicinity while working with MOS devices.
3. Insure that your body, the PC board and the MOS device are at the same potential before removing the device from the (shipping) carrier and inserting it into the PC board. This is easily accomplished by simultaneously bringing your working hand (and tool if used), the IC carrier and the PC board in contact immediately before removal and insertion.
4. Use a grounded soldering iron (3-wire) to solder MOS devices, if not available, connect the metal part of the iron to the ground bus on the PC. card with aligator clips and flexible wire while soldering.


## DUTRONICS P. о. вох 9160 - STOскTON, CALIFORNIA 95208







| 0191 | 04 |  |  |
| :---: | :---: | :---: | :---: |
| 0192 | CD | 2C | 00" |
| 0195 | 18 | EE |  |
| 0197 | 3 E | 07 |  |
| 0199 | 18 | F7 |  |
| 0198 | 04 |  |  |
| 019 C | 05 |  |  |
| 0190 | C1 |  |  |
| 019E | C9 |  |  |
| 019 F | 00 |  |  |
| 0140 | 06 | 07 |  |
| O1A2 | 18 | 02 |  |
| 0144 | 06 | 12 |  |
| 0146 | AF |  |  |
| 01 A7 | ED | 47 |  |
| 0149 | FB |  |  |
| 01 AA | 31 | 00 | 00 |
| 01 AD | DD | E 1 |  |
| 01 AF | CD | E8 | $00^{\prime \prime}$ |
| 0182 | DD | E5 |  |
| 0184 | 23 |  |  |
| 0185 | F9 |  |  |
| 0186 | 21 | A 0 | 01" |
| 0189 | E5 |  |  |
| 01 BA | 21 | BE | $00^{\prime \prime}$ |
| 01 BD | CD | DO | $00^{\prime \prime}$ |
| 01 C | 21 | CO | $01^{\prime \prime}$ |
| 01 C 3 | E5 |  |  |
| 01 C | CD | 31 | $01^{\prime \prime}$ |
| $01 C 7$ | 3 E | 5 A |  |
| $01 C 9$ | CD | 2 C | 00" |
| 01 C | CD | 14 | 01" |
| 01CF | FE | 45 |  |
| 0101 | 20 | 05 |  |
| 0103 | CD | 6A | $01^{\prime \prime}$ |
| 0106 | EB |  |  |
| 0107 | E9 |  |  |
| 0108 | FE | 4D |  |
| 01 A | 20 | 2C |  |
| 01 C | CD | 80 | 01" |
| 01 DF | EB |  |  |
| $01 E 0$ | CD | 31 | 011" |
| 0153 | CD | 18 | $01^{\prime \prime}$ |
| 01.6 | CD | 54 | $01^{\prime \prime}$ |
| $01 E 9$ | 7E |  |  |
| 01EA | CD | 24 | $01^{\prime \prime}$ |
| 01ED | CD | 4F | $01^{\prime \prime}$ |
| 01F0 | CD | 80 | $01^{\prime \prime}$ |
| 01F3 | D8 |  |  |
| 01F4 | 06 | 00 |  |

INR B B NON ZERO FOR ANY ENTERED
PAR2 CALL OCC ECHO IT
JR PARI AGAIN
PBAD MVI A.7H BELL
JR PAR2 OUTPUT DING AND DO AGAIN
POUT INR B
DCR B SET ZERO IF NONE ENTERED
POP B
RET
NOP ROOM
*ABORT ROUTINE
ABRT MVI B,7H
JR ENT1 SKIP OVER SIGN ON MESSAGE
*PRINT MLSSAGE AND SET STK POINTER
ENTR LXI B.12H
ENT1 XRA A
MOV I.A SET INT MODE 0
EI
LXI SP, 0
POP $X$ SAVE 0000 AND 0001
CALL TOPM GET TOP OF MEMORY
PUSH X
INX H
SPHL STK POINTER SET
LXI H.ABRT
PUSH H ABORT ON TOO MANY RETURNS
LXI H.MESG
CALL PRNT OUTPUT ABORT OR SIGN ON MESSAGE
*MAIN COMMAND READ LOOP
MAIN LXI H.MAIN HERE ON A RETURN
PUSH H
MAN1 CALL CRLF
MVI $A 0^{\circ} Z^{\circ}$
CALL OCC OUTPUT PROMPTER
CALL GICC GET COMMAND LHARACTEK *EXECUTE ROUTINE
E CPI 'E.
JRN $\angle$ MT
CALL PARG GET EXEC ADDRESS
XCHG
PCHL GO
*MODIFY ROUTINE
MT CPI •M
JRNZ DT
M CALL PARA GET START ADDRESS
XCHG
ME1 CALL CRLF
CALL OCHL OUTPUT ADDRESS
CALL OC1S
MOV A.M
CALL OCA OUTPUT ADDRESS CONTENTS
CALL OC2S
CALL PARA ANY CHANGE?
RC RETURN TO MONITOR ON CR
MVI B.O




?

| 0397 | D1 |  |  |
| :---: | :---: | :---: | :---: |
| 0398 | CD | A7 | $00^{\prime \prime}$ |
| 0398 | 30 | E9 |  |
| 0390 | C9 |  |  |
| 039 E | FE | 53 |  |
| 03 A0 | 20 | 16 |  |
| O3A2 | CD | 62 | $01^{\prime \prime}$ |
| 03A5 | CD | 70 | $01^{\prime \prime}$ |
| 03 A8 | 01 | 00 | 00 |
| $03 A B$ | 7B |  |  |
| $03 A C$ | ED | 81 |  |
| O3AE | EO |  |  |
| O3AF | 2B |  |  |
| 0380 | D5 |  |  |
| $03 \mathrm{B1}$ | CD | EO | 01" |
| 0384 | D1 |  |  |
| 0385 | 23 |  |  |
| 0386 | 18 | F0 |  |
| 0388 | FE | 48 |  |
| 03BA | 20 | 18 |  |
| 03 BC | CD | 5A | 01" |
| 03 BF | E5 |  |  |
| 03 CO | 09 |  |  |
| $03 C 1$ | CD | 4 F | $01^{\prime \prime}$ |
| $03 C 4$ | CD | 1 B | 01" |
| 03 C 7 | C5 |  |  |
| 03 C 8 | E1 |  |  |
| $03 C 9$ | C1 |  |  |
| $03 C A$ | B7 |  |  |
| 03 CB | ED | 42 |  |
| $03 C D$ | CD | 4B | $01^{\prime \prime}$ |
| 0300 | CD | 1B | $01^{\prime \prime}$ |
| 0303 | C9 |  |  |
| 0304 | FE | 52 |  |
| 0306 | 20 | 22 |  |
| 0308 | CD | 5 A | 01" |
| 03DB | DA | A 0 | 01" |
| O3DE | CD | 67 | 01" |
| O3E1 | 87 |  |  |
| 03E2 | ED | 42 |  |
| OJE4 | 38 | F5 |  |
| $03 E 6$ | C5 |  |  |
| O3E7 | E3 |  |  |
| 03 E8 | C1 |  |  |
| 03E9 | CD | A6 | $00^{\prime \prime}$ |
| O3EC | 38 | 08 |  |
| 03 EE | 09 |  |  |
| O3EF | EB |  |  |
| 03F0 | 09 |  |  |
| 03F1 | EB |  |  |
| 03F2 | 03 |  |  |
| $03 F 3$ | ED | B8 |  |

```
    POP D
    V2 CALL HGTD
        JRNC VI JMP NOT DONE
        RET
```

    *SEARCH ROUTINE
    SERT CPI 'S'
        JRNZ HEXT
    S CALL PARH GET FROM
    CALL PARC GET TO
    SE1 LXI B,O B USED BY M ROUTINE
    MOV A,E SEARCH IN E
    CPIR LOOK FOR IT
    RPO RET NONE FOUND
    DCX H STOPS ONE HIGHER
    PUSH D SAVE D
    CALL MEI M ROUTINE ENTRY
    POP D UNSAVE D
    INX H SET HL FOR NEXT
    JR SEI AGAIN
    *HEXIDECIMAL ROUTINE
    HEXT CPI 'H'
JRN $\angle$ RELT
H CALL PAFT GET TWO NUMBERS
PUSH H SAVE FIRST
DAD B AUD THEM
CALL OC2S
CALL OCHL OUTPUT SUM
PUSH B
POP H
POP B
ORA A ZERO CY
SBC B SUGTRACT THEM
CALL OCIC
CALL OCHL OUTPUT DIFFERENCE
RET
*RELOCATE ROUTINE
RELT CPI 'R'
JRNZ TOPT
$R$ CALL PAFT GET FROM THRU
RE1 JC ABORT NO TO
CALL PARD GET TO
ORA A ZERO CY
SBC B NO. LOCATIONS
JRC REI ABORT ON FROM GT TO
PUSH B
XTHL
POP B
CALL HDVD
JRC RE2 MOVE FORWARD
DAD B
XCHG
DAD B
XCHG
INX B
LDDR MOVE REVERSE

```
03F5 C9
03F6 03
03F7 ED B0
03F9 C9
O3FA FE 54
O3FC CA F5 00"
03FF C9
```

```
    RET
```

    RET
    RE2 INX B FORWARD
    RE2 INX B FORWARD
        LDIK
        LDIK
        RET
        RET
    *TOP MEMORY JUMP OFF
*TOP MEMORY JUMP OFF
TOPT CPI 'T'
TOPT CPI 'T'
JZ TOPP
JZ TOPP
RET ILLEGAL COMMAND
RET ILLEGAL COMMAND
*REPLACE ABOVE RET WITH NEXT ROUTINE
*REPLACE ABOVE RET WITH NEXT ROUTINE
*WHEN EXPANDING

```
*WHEN EXPANDING
```


[^0]:    *If other than Hex digits are entered, a BELL is output to the Command Console and the character is ignored.

[^1]:    *If other than Hex digits are entered, a BELL is output to the Command Console and the character is ignored.

[^2]:    * Add to these addresses the relocation factor (Sense Switch Value) when modifying by hand. When modifying with a Patch Tape, the Loader will add the relocation, so punch the address shown.

