EAI®

580

ANALOG/HYBRID COMPUTING SYSTEM

REFERENCE HANDBOOK

EAI® 580

ANALOG/HYBRID COMPUTING SYSTEM

REFERENCE HANDBOOK

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RELATED PUBLICATIONS

The table below lists other publications which may be of interest to the readers of this manual. Unless otherwise indicated by title or footnote, all are maintenance handbooks. Note that maintenance handbooks directly applicable to a particular system are normally supplied with the system.

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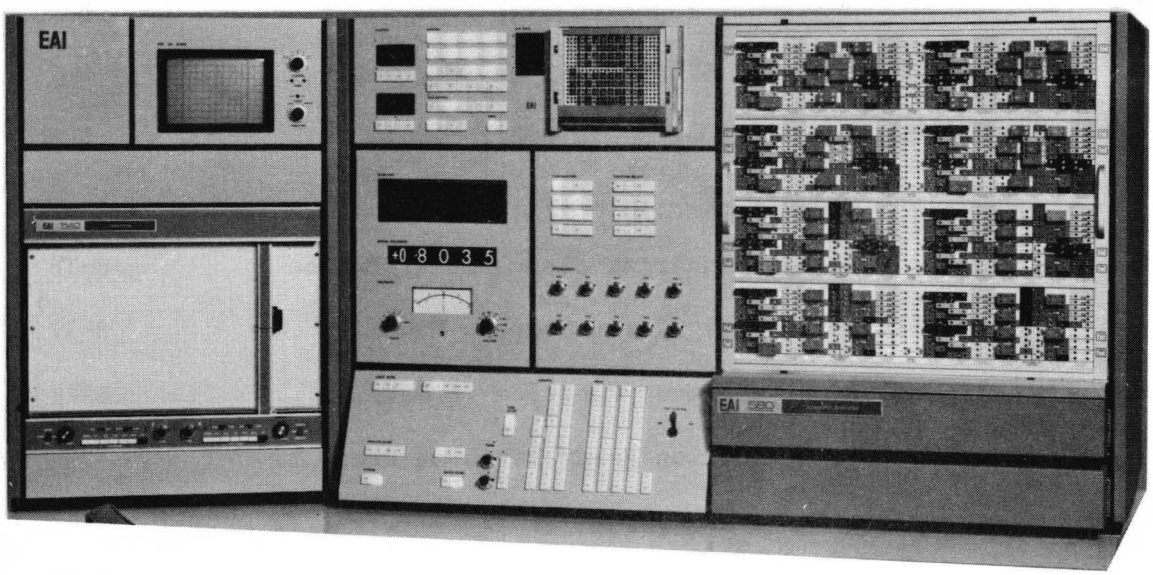


Figure 1.1. 580 Analog/Hybrid Computing System

CHAPTER 1

GENERAL DESCRIPTION AND OPERATION OF THE 580 ANALOG/HYBRID COMPUTING SYSTEM

1.1 GENERAL DESCRIPTION

The EAI 580 Analog/Hybrid Computing System (Figure 1.1) is composed of solid state computing components. The 580 (categorized as a desk-top computer) is compact in size and operates with stability and precision in a normal office or classroom environment as well as a computer laboratory. Each component has input and output terminations on the computer pre-patch panel for interconnection by bottle plugs and patch cords. The pre-patch panel is arranged in a series of 8 similar patching fields (Figure 1.2), with each field separated horizontally by either a control or trunk trays. The modular design tends to eliminate patching clutter caused by long across-the-panel patching.

The main control panel is located to the lower left of the analog patch panel (Figure 1.3). This area contains a majority of the operating controls.

The analog readout panel, located to the far left of the analog patch panel, contains the overload indicators, DVM readout (an expansion) and a multirange voltmeter.

The Auxiliary Control Panel, immediately to the left of the analog patch panel, includes 10 handset potentiometers, and override controls for both the comparators and the function relays.

The area below the analog patch panel contains two manual diode function generator (MDFG) drawers. The lower drawer contains the set-up amplifier and controls, and up to four, 10-segment MDFGs. The upper drawer is used to house additional segments as required.

The logic package, located at the upper left of the analog patch panel, contains the logic patch panel and various indicators and controls for the logic components.

1.2 OPERATING CONSIDERATIONS

1.2.1 General

The 580 is completely tested and calibrated at the time of manufacture and is shipped with all components in place. After performing the installation checkout procedure outlined in the 580 Maintenance Manual, the computer is ready for operation.

It should be noted that the low voltage levels used in the 580 eliminate any shock hazard when patching with the pre-patch panel in the computer. Current-limiting circuits protect the reference supplies from damage when they are in-

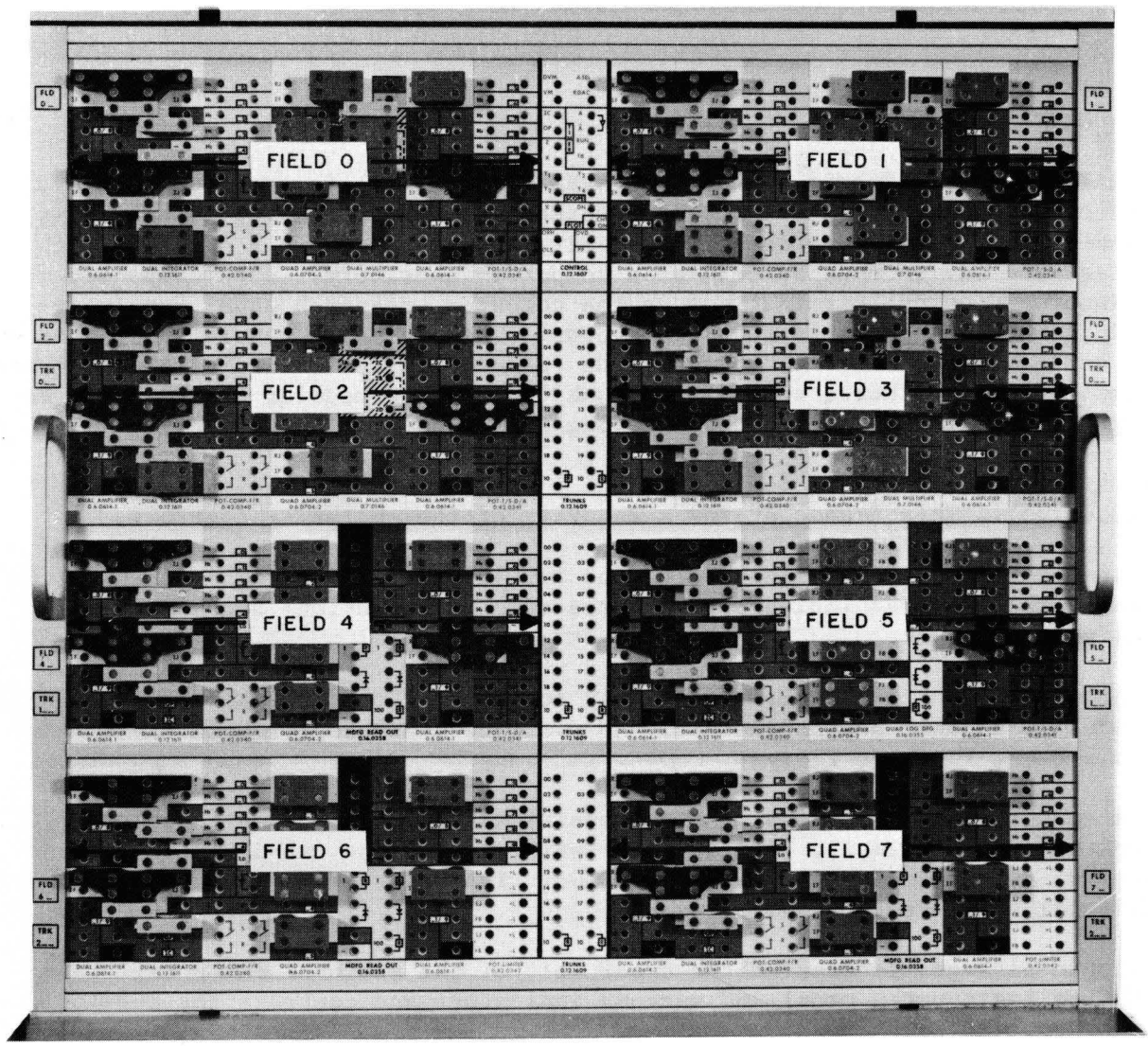


Figure 1.2. Typical Pre-Patch Panel Field Layout

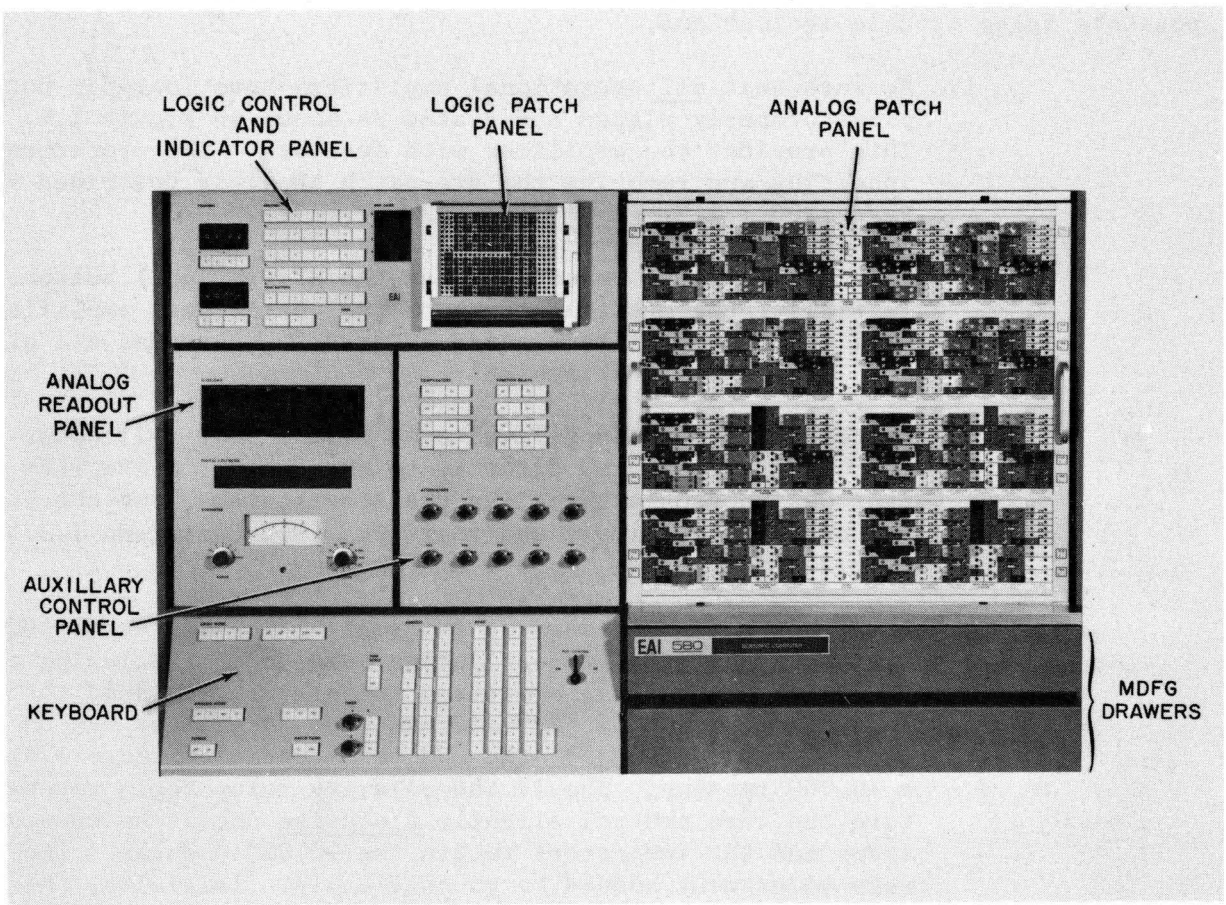


Figure 1.3. Physical Layout of the 580 Computer

advertantly patched to ground or to each other. (Dangling patch cords rarely short to ground because of the plastic patching blocks and because the metal strips between the patching block are covered with a scratch-resistant, non-conductive paint.)

1.2.2 Preliminary Operating Considerations

The following steps are recommended prior to operating the 580 to prevent possible false trouble indications.

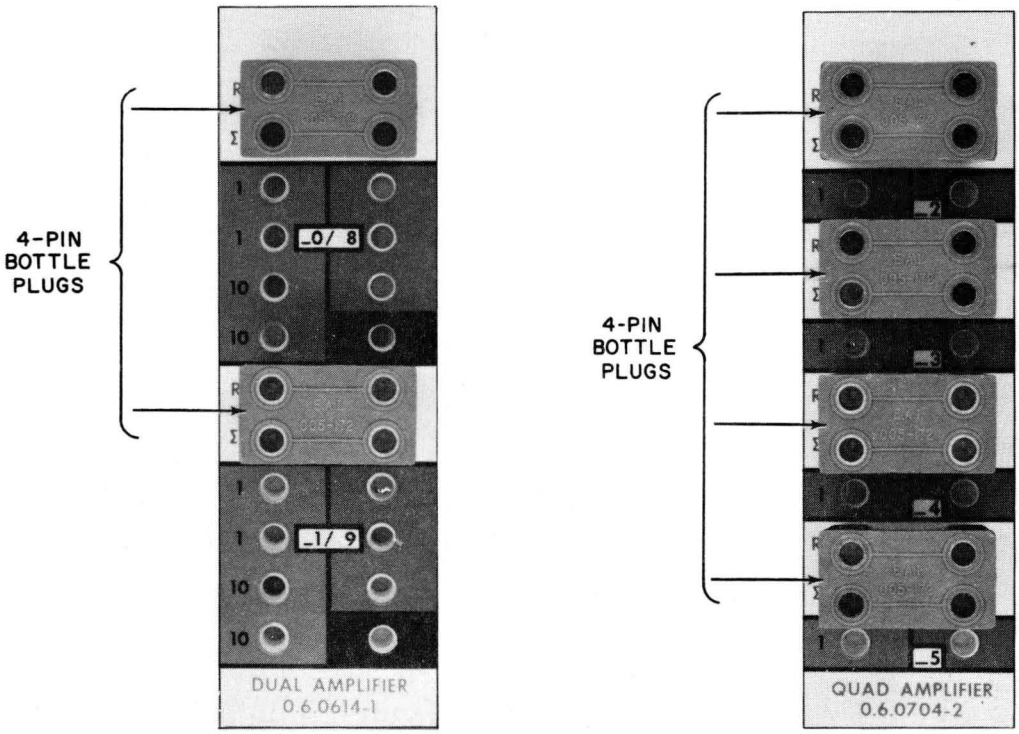
1. Be sure that all operational amplifiers have four-pin bottle plugs properly placed and seated as shown in Figure 1.4. This provides the amplifier with feedback. The procedure for inserting and removing the pre-patch panel is described in Paragraph 1.2.3.

2. Turn the computer on and depress the SP (set pot) button. Initially, the overload lamps of the operational amplifiers will light due to transients; after a few seconds, all of the lamps should extinguish.

3. Check the various supply voltages of the 580. All power supply outputs are connected directly to the voltmeter FUNCTION switch (through appropriate scaling resistors); thus, the check may be accomplished simply and rapidly. (See Paragraph 1.3.5 of this section.)

4. Allow a few minutes warm-up (at least 1/2 hour for the DVM) time to assure that the computing components (including the DVM) are up to normal operating temperature. Ground the input termination in "PP" address mode designated DVM on the control tray and adjust the DVM zero control (Figure 1.5) for a +0.000 reading. Should the polarity relay begin to chatter, turn the zero control slightly clockwise until the chatter stops and the indicators retain the +0.000 display. The DVM zero adjustment should be checked daily. Initially, this adjustment may be required more frequently due to aging of the components.

5. Closed relay contacts provide a 100Ω feedback resistor for the operational amplifiers when in the set pot mode of the computer (SP button on the control panel depressed). (This feature permits pre-patch panel removal without overloading the amplifiers.) However, when the computer is switched from set pot to another mode, the relay contacts open and the amplifier feedback loop is determined by the patching on the pre-patch panel. The amplifier overload indicators may be triggered momentarily during the switching time. This is of no consequence since the computer should always be placed in the initial condition mode before going to the operate mode.



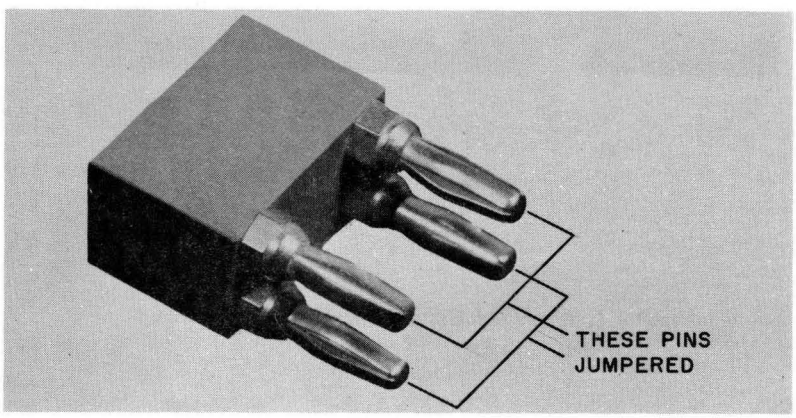


Figure 1.4. Amplifiers with Four-Pin Bottle Plugs Providing Feedback

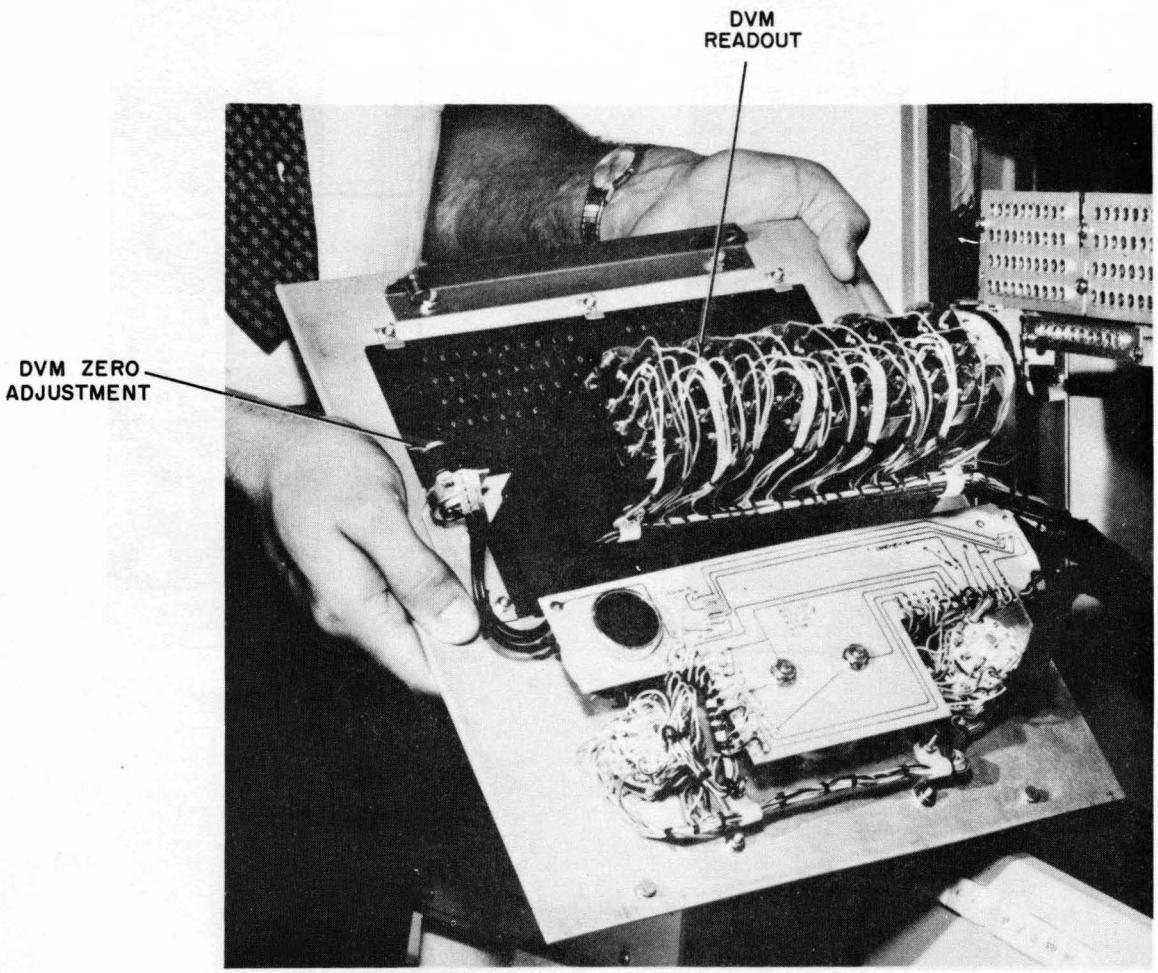


Figure 1.5. DVM Zero Adjustment Location

1.2.3 Pre-Patch Panel Insertion and Removal

To insert the pre-patch panel, align the lugs on the bottom of the pre-patch panel frame with the slots in the bottom rail of the patch bay (Figure 1.6). Push the pre-patch panel forward until the lugs on the top of the frame mate with the slots on the top rail of the patch bay. Gently slide the pre-patch panel slightly to the right. Depress the ENG switch. (The computer automatically goes into the set pot mode when the ENG switch is depressed.) The patch panel drive system faces the pre-patch panel to the right into the locked position.

Depressing the DIS pushbutton disengages the locking system and forces the pre-patch panel to the left for removal.

1.2.4 Amplifier Balance

For accurate computation, the operational amplifier must remain balanced. The amplifier must produce a zero output voltage when the combined effects of the input voltages or the absence of input voltages demand it. With this requirement in mind, the amplifiers contain chopper stabilization circuits to minimize the effect of component drift. Under normal circumstances, the amplifiers do not require balancing for several weeks. However, it is desirable to check this condition periodically; if an amplifier is found to be unbalanced, an adjustment is required. The amplifier balance is checked as follows:

1. Allow a warm-up of 15 to 30 minutes. Place the voltmeter FUNCTION switch in the ABAL position and depress the SP pushbutton of the MODE switch.

2. Use the signal selector system to connect the stabilizer output of each amplifier to the voltmeter. Select A00 and proceed in order. In each case, the voltmeter should register a deflection that is less than 1/2 division on the meter scale.

3. If an amplifier causes a larger deflection, the amplifier should be balanced. The balance controls for amplifiers are located behind the pre-patch panel on the front block of the amplifiers (Figure 1.7). Adjust these controls for a zero reading on the voltmeter.

1.2.5 Changing Computational Components

In the solution of some problems, it may be necessary to add a computing component to the existing complement. Since some of the module positions are designed to handle more than one type of computing component, a component not required in the problem investigation may be removed and another unit inserted in its place. Figure 1.8 illustrates the various positions of the computing component in the 580 field area. The diagram shows which type of computing component is compatible with each position. The procedure for replacing a computing component and changing the pre-patch panel patching block is described in the following paragraphs.

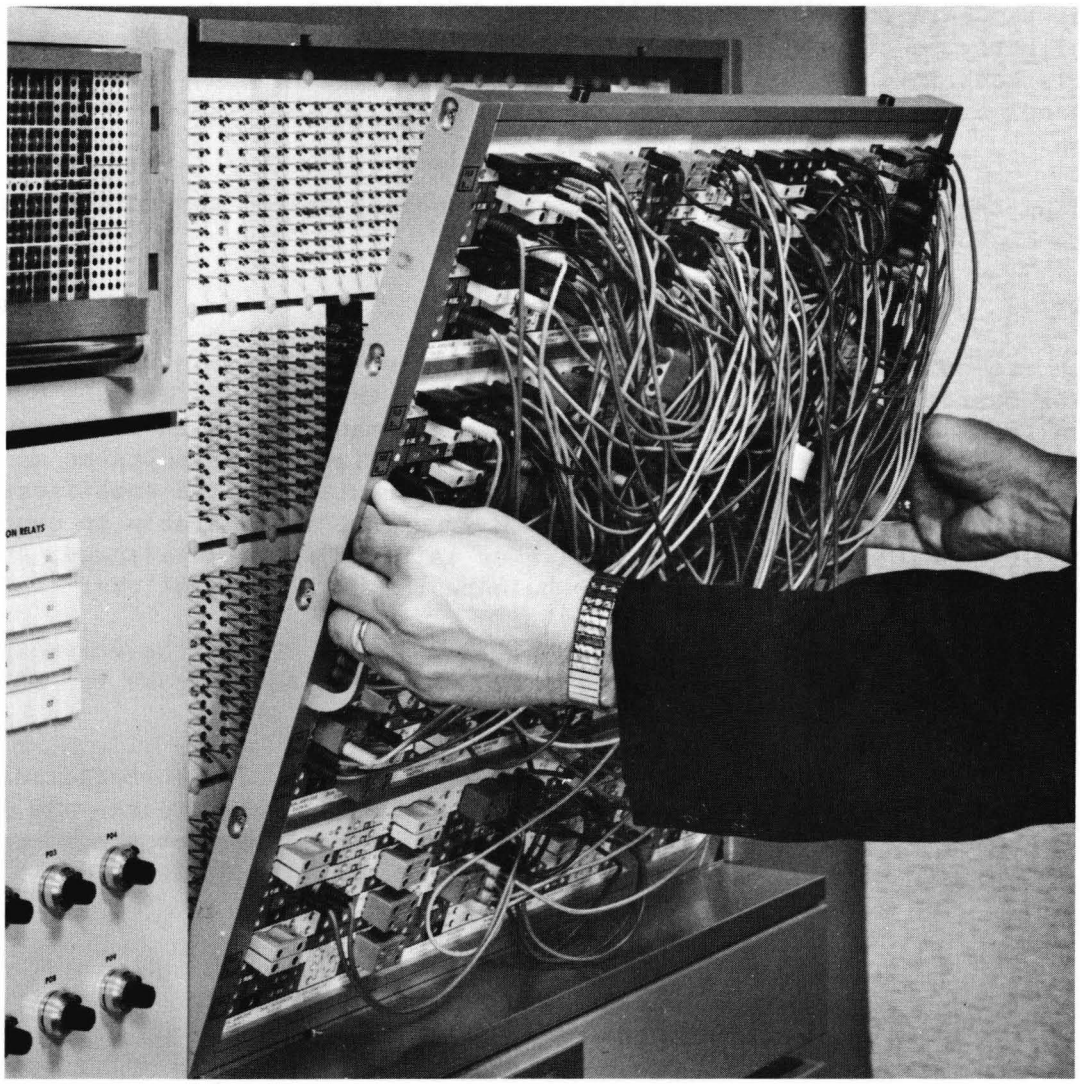
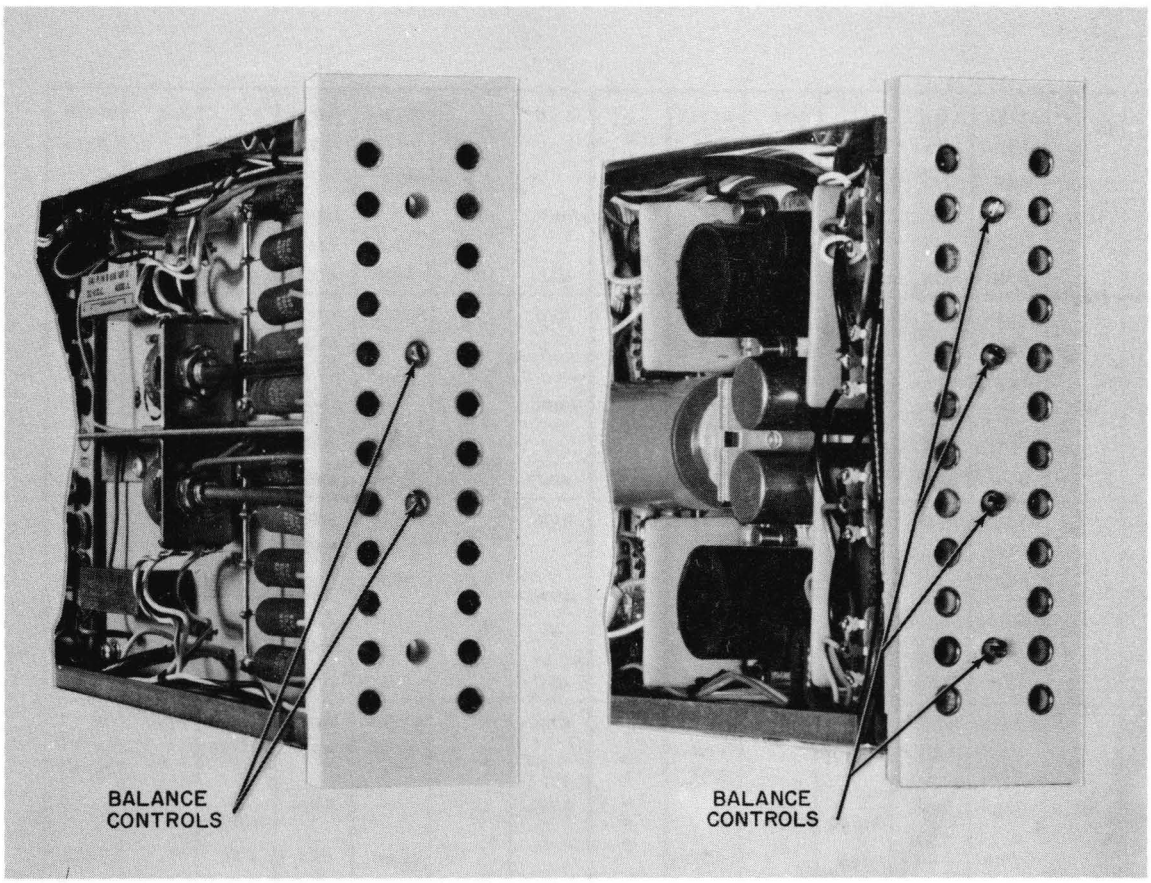


Figure 1.6. Pre-Patch Panel Insertion



(a) 0.6.0614 Dual DC Amplifier

(b) 0.6.0704-2 Quad DC Amplifier

Figure 1.7. Amplifier Balance Control Locations

A00 AMPL A01	INT	ATTEN P00- P04 ---- COMP. F/R	A02 A03 AMPL A04 A05	MULT	A08 AMPL A09	ATTEN P05- P09 ---- T/S D/A	CONTROL TRAY	A10 AMPL A11	INT	ATTEN P10- P14 ---- COMP. F/R	A12 A13 AMPL A14 A15	MULT	A18 AMPL A19	ATTEN P15- P19 ---- T/S D/A
A20 AMPL A21	INT	ATTEN P20- P24 ---- COMP F/R	A22 A23 AMPL A24 A25	MULT	A28 AMPL A29	ATTEN P25- P29 ---- T/S D/A	TRUNKS	A30 AMPL A31	INT	ATTEN P30- P34 ---- COMP. F/R	A32 A33 AMPL A34 A35	MULT	A38 AMPL A39	ATTEN P35- P39 ---- T/S D/A
A40 AMPL A41	INT	ATTEN P40- P44 ---- COMP F/R	A42 A43 AMPL A44 A45	QUAD LOG DFG ---- MDFG A46 A47	A48 AMPL A49	ATTEN P45- P49 ---- T/S D/A	TRUNKS	A50 AMPL A51	INT	ATTEN P50- P54 ---- COMP. F/R	A52 A53 AMPL A54 A55	QUAD LOG DFG ---- MDFG A56 A57	A58 AMPL A59	ATTEN P55 P59 ---- T/S D/A
A60 AMPL A61	INT	ATTEN P60- P64 ---- COMP F/R	A62 A63 AMPL A64 A65	SINE/ COSINE ---- MDFG A66 A67	A68 AMPL A69	ATTEN P65- P69 ---- LIMITER	TRUNKS	A70 AMPL A71	INT	ATTEN P70- P74 ---- COMP. F/R	A72 A73 AMPL A74 A75	SINE/ COSINE ---- MDFG A76 A77	A78 AMPL A79	ATTEN P75 P79 ---- LIMITER

Figure 1.8. Computer Component - Field Assignment Areas

1.2.5.1 Computing Module Replacement

1. Remove the pre-patch panel to expose the computing component modules. Remove the two Phillips head retaining screws from the top and bottom of the module to be removed (Figure 1.9a).

2. Insert the special module extraction tool on the ends of the tray (Figure 1.9b). Pull the tray forward, removing it from the computer.

3. Place the new component in place; be sure the guide pins are properly seated in the guide-pin holes before mating the connectors to the rear of the module.

4. Check that the module is properly installed (connector firmly mated, etc.,) and replace the two retaining screws.

1.2.5.2 Patching Block Replacement

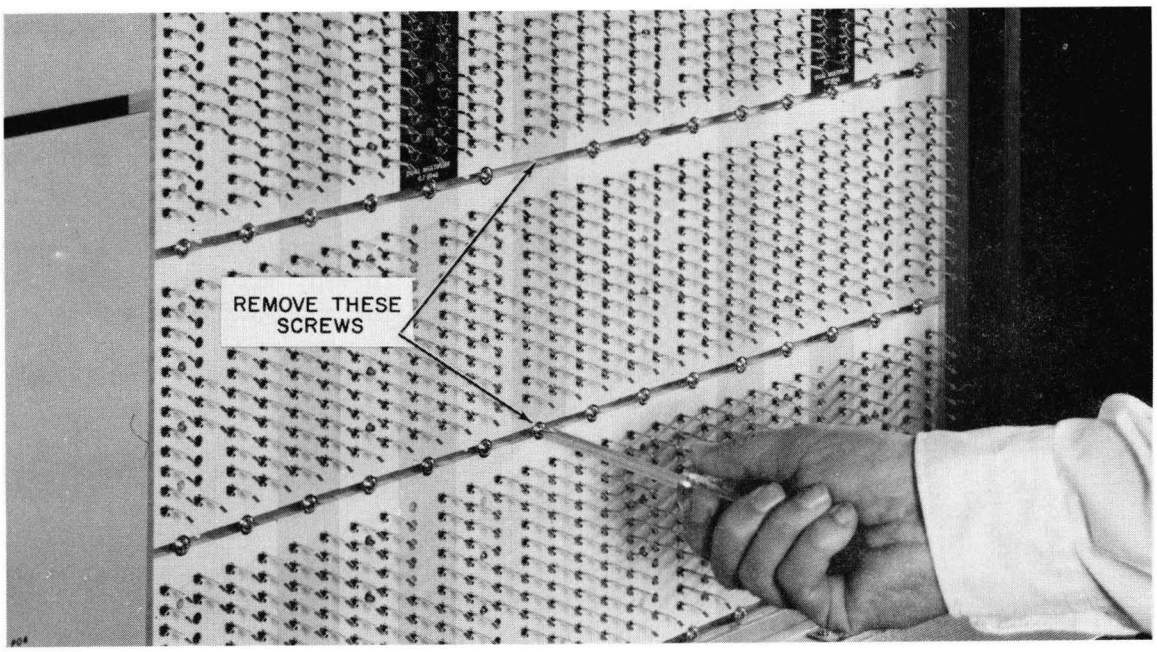
1. The patching blocks of the computing components are held securely in place by the retaining strips on the front of the pre-patch panel (Figure 1.10a).

2. The retaining strip above or below the patching block may be removed to change blocks. The retaining strip is released by removing the four screws directly behind the strip on the rear of the pre-patch panel (Figure 1.10b). If blocks on two adjacent horizontal rows are to be replaced, remove only the retaining strip between the two rows. The patching blocks can then be removed from the rows above and below the strip.

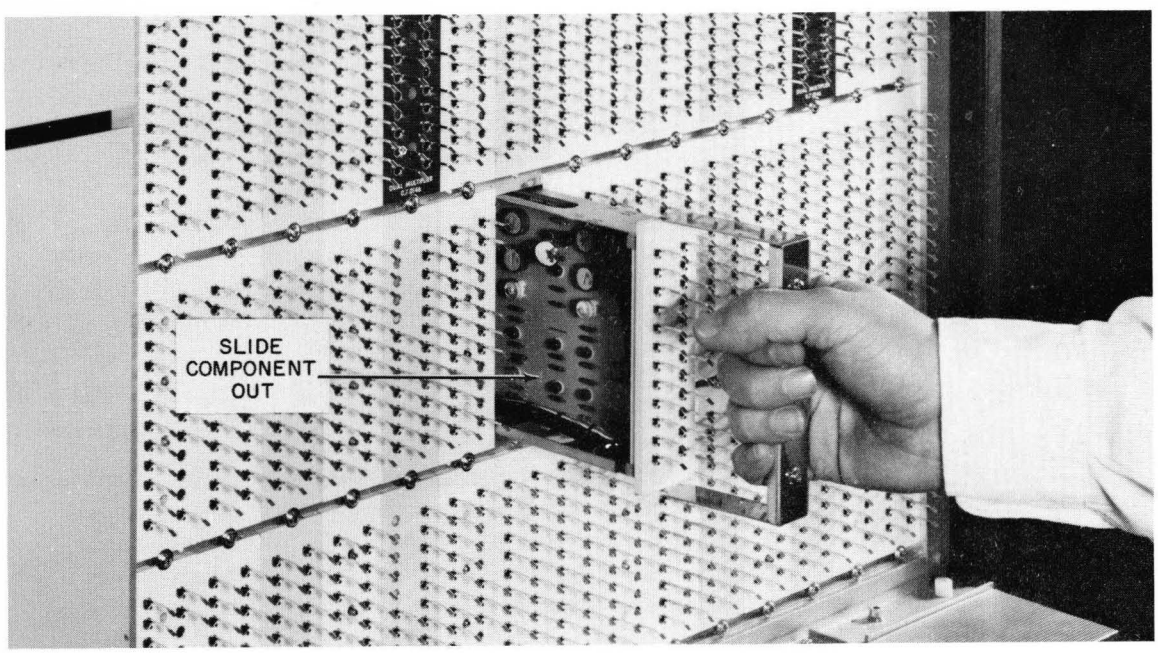
3. Once the retaining strip is free, remove the original patching block and replace it with the new block (Figure 1.10b). Secure the retaining strip with the four screws. The pre-patch panel is now ready for problem patching.

NOTE

Failure to change the patching block when computing components are changed may prevent proper operation because of the arrangement of the jumpers on the rear of the patching block.

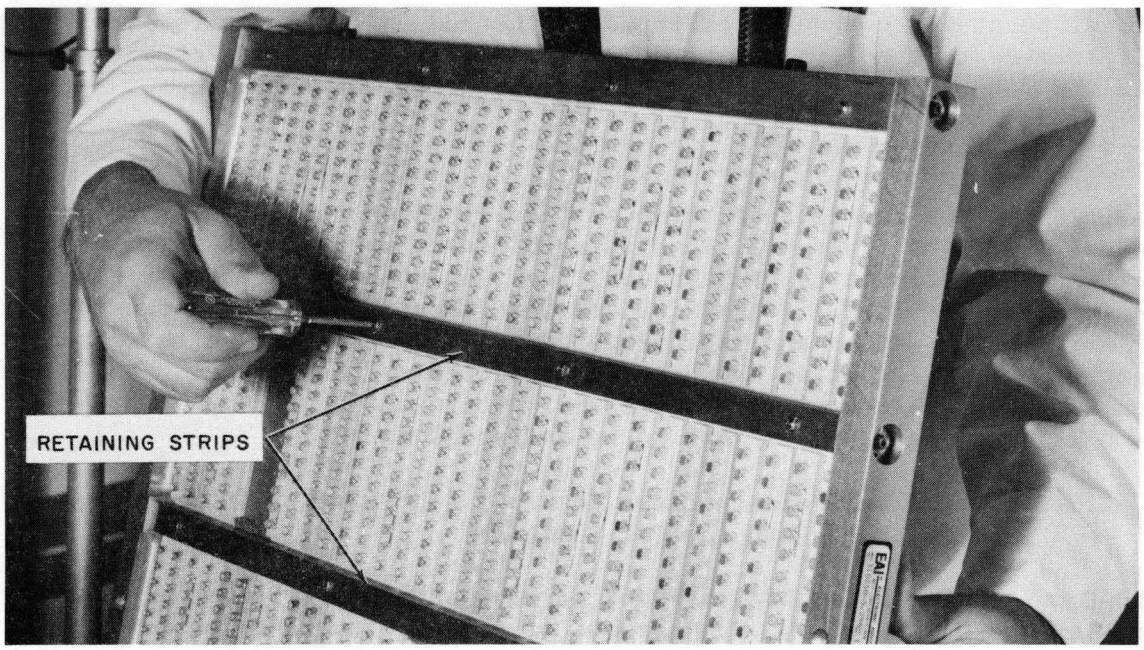


(a) Retaining Screw Location

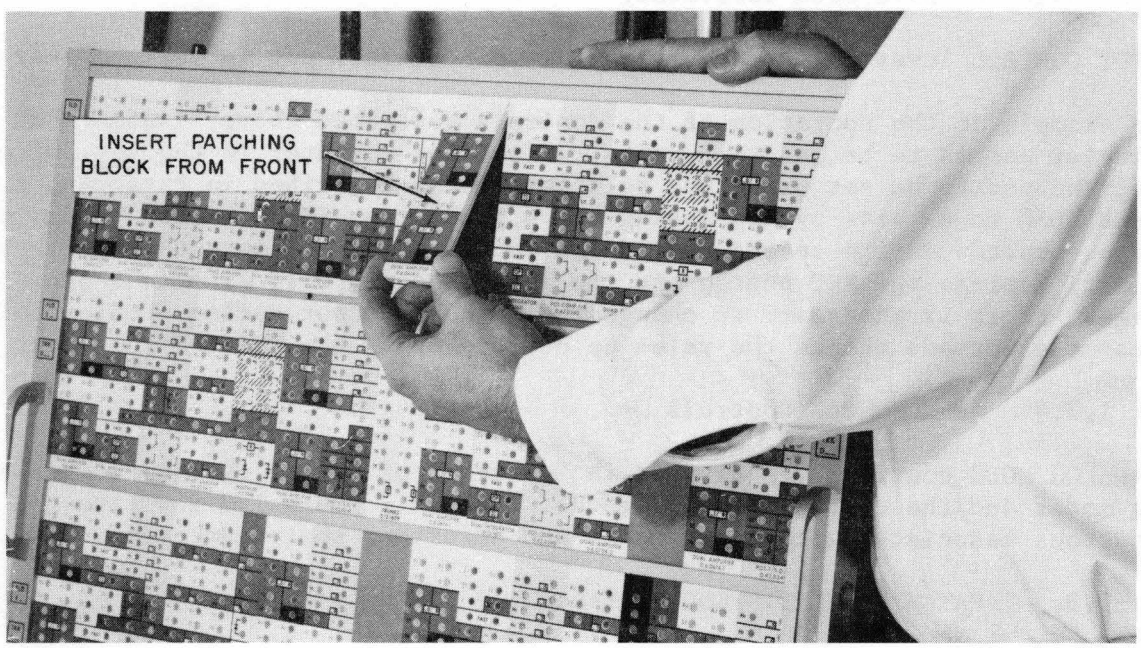


(b) Using Extraction Tool

Figure 1.9. Removal of Computing Component



(a) Removal



(b) Replacement

Figure 1.10. Patching Block Replacement

1.3 KEYBOARD PANEL

1.3.1 General

The focal point for control facilities of the 580 is the keyboard panel (Figure 1.11), located to the left of the MDFG drawers. The following paragraphs describe the function and use of the various controls and components.

1.3.2 ADDRESS Switch

The ADDRESS switch consists of three vertical rows of pushbutton switches (Figure 1.11). The first row, consisting of seven pushbuttons, is used to select the type of unit to be read out, i.e., A equals Amplifier, P equals Potentiometer. Table 1.1 identifies and describes the function of each switch in this row. The second and third rows contain the tens and units switches respectively. Note that if the position selected is less than 10, the 0 pushbutton in the 10 column must be depressed. For example, if amplifier 4 in field 0 is to be read out, it has to be addressed as A04.

1.3.3 Servo Set Potentiometer Controls (Including RDAC Switches, CL/SET Switches, and the POT CONTROL)

The RDAC switches consist of 4 columns of 10 pushbutton switches with each column labeled 0 through 9. The purpose of these switches is to provide a precise voltage for automatic setting of the servo set potentiometers.

The CL/SET pushbuttons are used to <u>clear</u> or to <u>set</u> an addressed pot once the RDAC pushbuttons have been activated.

The POT CONTROL lever allows adjustment of an addressed pot in any computer mode.

As an example of the operation of the controls described above, assume that a particular pot is to be set to 8 volts. Place the computer in the <u>set pot</u> mode. Select the pot to be set using the selector system described in Paragraph 1.3.1. Set the RDAC to 8 volts by depressing the 8 pushbutton in the first column and the 0 pushbutton in the second, third and fourth columns. Once the RDAC has been set, depress the SET button and the addressed pot will slew to the proper voltage. If it is necessary to change the value of a pot during problem solution, address the pot and change the value up or down using the POT CONTROL lever.

1.3.4 ANALOG MODE Controls

The ANALOG MODE controls are divided in two types of modes; the computer operating modes and the computer set-up modes. Tables 1.2 and 1.3 indicate the pushbuttons associated with these modes and describes their functions.

1.3.5 PATCH PANEL DIS/ENG Switches

The PATCH PANEL DIS/ENG switches provide control of the patch panel drive system when inserting or removing the pre-patch panel (see Paragraph 1.2.3).

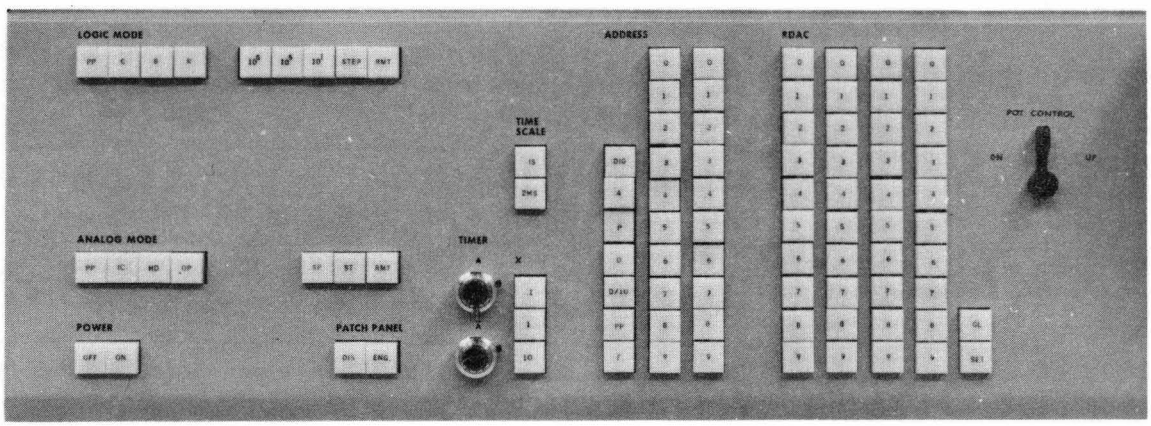


Figure 1.11. Keyboard

Table 1.1

Pushbutton	Function
DIG I/O	Depressing this pushbutton transfers control of the readout selection system to a digital computer when the 580 is installed in a hybrid configuration.
PP	This pushbutton is used to connect the DVM patch terminal on the 0.12.1607 Control Tray to the DVM input.
F	Depressing this pushbutton and the appropriate pushbutton on the Amplifier Balance Panel, located in the lower MDFG drawer, allows the amplifiers, located in the 0.12.1345 MDFG Amplifier Network, to be balanced on the DVM.
D	This pushbutton is used for a derivative readout from the summing junctions of the integrators and track/store units.
D/10	Same as the D (derivative) pushbutton except that in voltage readout is divided by a factor of 10.
P	The P (potentiometer) pushbutton connects the arm of the potentiometer addressed to the DVM.
A	The A (amplifier) pushbutton when depressed switches the output of the selected amplifier or MDFG setup amplifier to the DVM input.

Table 1.2. Definitions of Computer Operating Modes

Mode	Function
OPERATE (OP)	Integrators operate; computer produces a dynamic solution to a patched problem.
HOLD (HD)	Integrators do not operate; all values present at the time the hold mode is selected are returned.
INITIAL CONDITION (IC)	Integrators are set to initial values.
REMOTE (RMT)	Parallels mode control of computer to external devices.

Table 1.3. Definition of Computer Set-Up Modes

Mode	Function
STATIC TEST (ST)	Similar to initial condition. Static test voltages can be applied to integrators not normally provided with initial condition voltages, to permit checking computed levels at other parts of the program via Function Relays. All INT and T/S are forced to IC mode.
SET POT (SP)	All amplifiers provided with low impedance feedback to provide correct attenuator loading. Reference voltage applied to high end of any pot selected for readout, so that the pot coefficient may be read out. The servo amplifier is connected to the motor of an addressed pot, permitting the pot to be set.
PROGRAM PANEL (PP)	When this button is depressed the IC, HOLD, and OPERATE modes may be controlled by logic signals applied to the 0.12.1607 Control Tray patch block. This mode also causes the internal timer to automatically start operation.

1.3.6 TIME SCALE Switches and Controls

The TIME SCALE and X switches along with the TIMER controls are used to control the analog timer (repetitive operation) circuit. The timer circuit generates the precise time intervals necessary to control the analog modes of the computer for iterative or repetitive operation. The TIME SCALE pushbuttons provide a 500 to 1 speed-up of the entire computer.

The repetitive operation (Rep-Op) circuit allows both high-speed, and low-speed repetitive operation. Any OPERATE or IC period from 100 μsec to 100 sec may be selected by the pushbuttons and Vernier controls provided to "bridge the gap" between pushbutton settings. Separate Vernier controls are provided for adjustment of the A (IC) and $\overline{A}$ (OP) periods.

The timer has the following inputs, outputs, and controls:

1.3.6.1 Input. The "RUN" terminal on the analog patch panel terminates in the control tray in the center of the first row. This input starts and stops the timer, and allows rep-op runs to be terminated by some condition other than elapsed time. For example, if it is desired to operate the analog simulation until some analog variable crosses zero, the RUN input may be patched from a comparator.

When RUN = 0, the timer does not run; its output remains in the A (IC) state. When RUN becomes high (logic ONE) the timer starts to run, starting with a full A (IC) period, followed by an $\overline{A}$ (OP) period. It continues to cycle between A and $\overline{A}$ as long as RUN = 1.

In ordinary repetitive operation, where the OPERATE period is fixed in advance by the operator, there is no need to patch the RUN input. It is internally connected to the "PP" signal, which is controlled by the ANALOG MODE button labeled "PP" (Paragraph 1.3.3). Thus, ordinary repetitive operation requires no special patching; the operator simply selects the desired A (IC) and $\overline{A}$ (OP) periods, and depresses the "PP" button. However, if the operator desired to control the timer from an arbitrary logic signal, local patching at the RUN terminal overrides the internal connection.

1.3.6.2 Outputs. The timer has two logic outputs (A and $\overline{A}$) and an analog output TB (Time Base). The terminals are connected to the 0.12.1607 Control Tray. The A and $\overline{A}$ outputs normally control the IC and OP buses respectively. The IC and OP patch terminals, connected internally to the A and $\overline{A}$ terminals, act as inputs to the IC and OP buses. Logic signals at these terminals override the internally generated signals and provide external control of the IC and OP buses.

The TB output is an analog ramp generated by an internal integrator and provides a voltage proportional to time. The ramp output may be used to drive the horizontal axis of readout devices (Plotting Board, Oscilloscope, etc.,) or may be used as an analog signal for problems requiring a signal proportional to time. The ramp integrates from zero to plus reference voltage during a given operate cycle. Thus, the scaled output is (t/t_{max}), where t_{max} is the length of the operate cycle. (This is a unit scaled notation; the run terminates when $t = t_{max}$, which means $(t/t_{max}) = 1.0$ unit, or 10 volts.)

1.3.6.3 Controls. The period of the timer is determined by three sets of controls: a pair of dials (one for A, one for $\overline{A}$), a group of three X (multiplier) pushbuttons (.1, 1, 10), and two TIME SCALE pushbuttons (2 msec, 1 sec). Note that the dials and the multiplier pushbuttons affect the rep-op timer only, while the TIME SCALE pushbuttons control the timer integrator as well as the capacitors in the computer integrators.

The A and $\overline{A}$ controls utilize ten-turn Vernier dials with a built-in turn counter. A window at the top of each dial displays an integer representing the number of complete revolutions of the dial. The graduations around the dial allows a fractional part of a revolution to be set to two figures. Thus, the dial can be set for 5.20 turns, 8.75 turns, etc. The dial has been offset by 0.50 turns. Consequently the minimum position is 0.50 turns while the maximum position is 10.5 turns.

The multiplier pushbuttons are a series of momentary contact switches connected in such a manner that when one is depressed it electrically clears any previously selected pushbutton.

The length of the A and $\overline{A}$ periods is the product of three factors: the number of turns on the Vernier dial, the multiplier setting, and the TIME SCALE selected. A simple equation for determining the lengths of either the A or $\overline{A}$ periods is TIME SCALE X Multiplier X Vernier = Length of Period. The following table gives the minimum and maximum time periods for each range.

A 500 to 1 speedup of the entire computer is also provided by the TIME SCALE pushbuttons. The TIME SCALE pushbuttons control the time scale relays located in each integrator tray through the time scale bus system. The 500 to 1 speed-up controls both integrators in a dual integrator tray. In the 2 ms range, the time scale bus is at a logic ZERO level energizing the time scale relay. Energizing this relay switches capacitance from 10 μf to 0.02 μf, speeding up the problem by a factor of 500. (The problem is automatically rescaled when speeded up by a factor of 500.) The 1 SEC pushbutton switches the time scale bus to a high (+5v) logic level, the relays are de-energized and the computer resumes normal problem speed.

Note that the TIME SCALE pushbuttons only affect the normally patched integrators. By local patching, it is possible to control the time scale input of the integrators, located in a particular tray, independent of the master time scale selection system. In addition, it is possible, by local patching, to speed up a factor of 10 to 1 individual integrators.

Table 1.4. Time Periods

TIME SCALE	X (Multiplier)	Vernier	Time
2 MS	X0.1	0.5 to 10.5	100 μS to 2 MS
2 MS	X1.0	0.5 to 10.5	1 MS to 20 MS
2 MS	X10.0	0.5 to 10.5	10 MS to 200 MS
1 SEC	X0.1	0.5 to 10.5	50 MS to 1.0 SEC
1 SEC	X1.0	0.5 to 10.5	0.5 Sec to 10.0 SEC
1 SEC	X10.0	0.5 to 10.5	5.0 Sec to 100.0 SEC

1.3.7 POWER Pushbuttons

The POWER pushbuttons control the power for the entire computer. To activate the computer, depress the ON pushbutton. To turn the computer off, depress the OFF pushbutton. The ON pushbutton contains an indicator lamp which lights to indicate that the computer is "ON".

1.3.8 LOGIC MODE Pushbuttons

The LOGIC MODE pushbuttons consist of four momentary pushbutton switches used to control the 580 Logic Package. These switches are connected in such a manner that when one is depressed it electrically clears any previously selected modes. An indicator lamp in each pushbutton indicates, when lit, which mode is selected. The LOGIC MODE pushbuttons are included only when a logic package is installed in the computer. Table 1.5 lists the description and function of each LOGIC MODE pushbutton.

Table 1.5. LOGIC MODES

LOGIC MODE	Function
PP (Patch Panel)	Transfers control of logic mode to the logic patch panel.
C (Clear)	Clears all flip-flops in the logic package including those in the counters and registers. (Clear line remains high preventing initialization.)
S (Stop)	Stops the logic clock preventing flip-flops and registers from reacting to patched inputs. (Clocked devices may still set and reset manually.)
R (Run)	Normally used for computation. Clocked devices (flip-flops, registers) respond to patch panel inputs.

1.3.9 Logic Clock Rate Pushbuttons

The four clock rate pushbuttons (10^6, 10^5, 10, and STEP) select the clock rate for the synchronized logic elements in the logic package. The pushbuttons are momentary contact switches which, when depressed, select a new clock rate and electrically clear the previously selected clock rate. The 10^6, 10^5, and 10 pushbuttons include lamps which indicate which clock rate has been selected. Table 1.6 lists the function of each clock rate pushbutton.

Table 1.6. Clock Rate Pushbutton Functions

Clock Rate	Function
10^6	Considered normal clock rate. One clock pulse every microsecond.
10^5	One clock pulse every 10 microseconds.
10	Ten clock pulses every second.
STEP	Inhibits all clock pulses when initially depressed. Provides one clock pulse when subsequently depressed.

1.3.10 Logic RMT (Remote) Pushbutton

The RMT (remote) pushbutton is a latching type pushbutton which parallels both logic mode control and clock rate control with a remote source. The remote source may be a digital computer in a hybrid configuration or another 580 Computer when two or more are connected in a slaved configuration.

1.4 THE ANALOG READOUT PANEL

The analog readout panel (Figure 1.12) consists of amplifier OVERLOAD indicators, a multi-range VOLTMETER. A DIGITAL VOLTMETER readout display is also located on this panel if a digital voltmeter (DVM) is provided with the computer. The following paragraphs describe the function and use of the various controls and components.

1.4.1 Amplifier OVERLOAD Indicators

The amplifier OVERLOAD indicators provide a graphic overload display for each individual amplifier. The indicators are numbered (A00 to A79) to correspond with each amplifier position in the computer. The overload indicators are normally extinguished. A lit position indicates that the corresponding amplifier is in an overload condition. During warm-up periods, various overload lamps may light but should be extinguished once the corresponding amplifiers have settled down.

1.4.2 The DIGITAL VOLTMETER (DVM) Readout

The DVM readout displays four digits, a polarity sign, and a fifth digit for overrange. The output of any selected amplifier in the coefficient of any selected potentiometer can be displayed on the DVM. The reading may range from $\pm$0.0000 to $\pm$1.1999 which, when multiplied with the reference voltage, represents the voltage into the DVM. As an example a reading of 1.1999 is equivalent to 11.999 volts (UNITS DISPLAYED X REFERENCE VOLTAGE).

1.4.3 The VOLTMETER

The VOLTMETER is controlled by the RANGE and FUNCTION rotary switches located directly below the meter.

The RANGE switch selects the voltage range of the meter. The ranges provided are: 30, 10, 3, 1, 3, and 0.1 volt for full scale meter deflection. A NULL position is also provided on this switch to convert the VOLTMETER to a null meter.

The FUNCTION switch determines the source of the input signal. Note that many positions on the switch are primarily used for maintenance purposes. However, these positions enable the operator to quickly check all power supply voltages to ensure proper computer operation. Table 1.7 describes the function of each RANGE switch position.

1.5 THE AUXILIARY CONTROL PANEL

The auxiliary control panel (Figure 1.13) contains the pushbutton controls and indicators for the interface components (comparator and function relays), and the ten handset pots (P0 through P9).

1.5.1 The COMPARATOR Controls

A pair of pushbuttons (one numbered, one blank) is provided for each of the eight comparators in the computer. These pushbuttons are used to force the

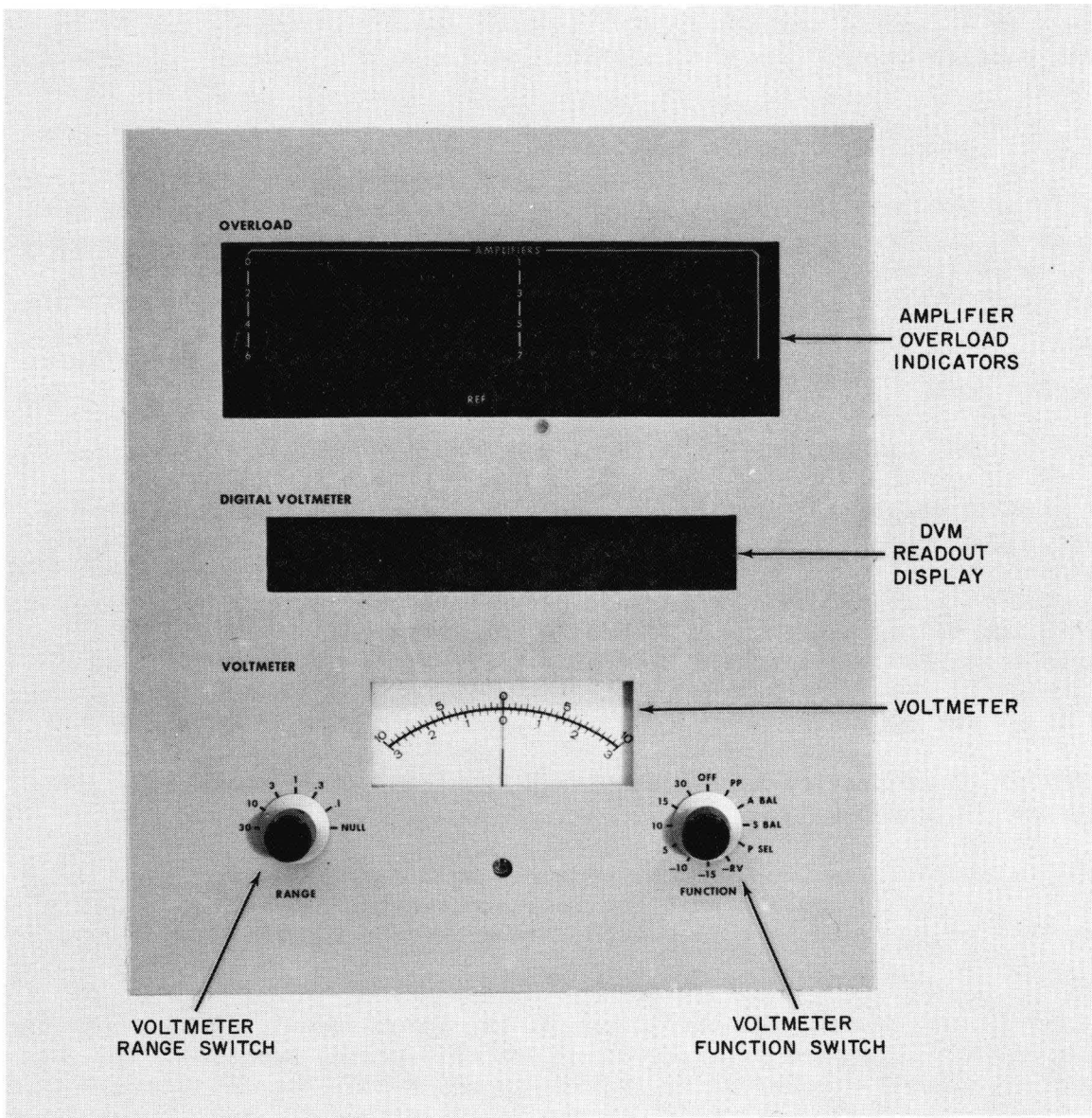


Figure 1.12. Analog Readout Panel

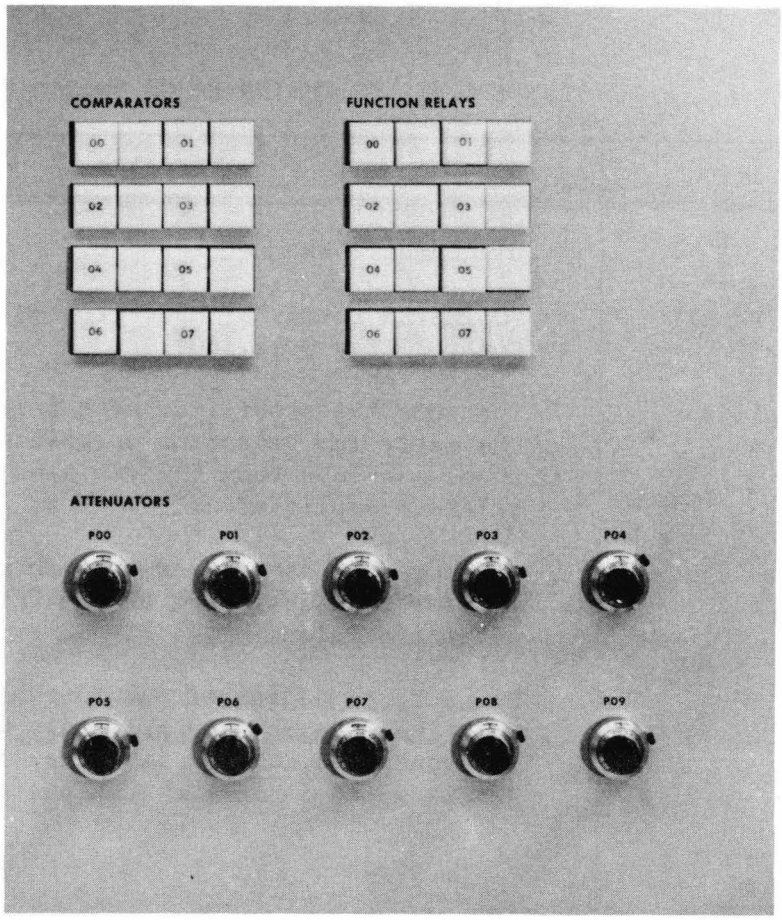


Figure 1.13. Auxiliary Control Panel

comparator output to a particular state regardless of its analog inputs. When the pushbutton is released, the corresponding comparator returns to the state dictated by the patch panel inputs. The numbered pushbutton, when depressed, forces the patch panel output of the corresponding comparator high. Similiarly depressing the blank pushbutton forces the comparator output low.

The numbered pushbutton contains an indicator lamp that lights when the comparator output is high. When the comparator has a low output the lamp is extinguished.

Table 1.7. VOLTMETER RANGE Switch Functions

Switch Position	Function
OFF	Disconnects the meter input.
PP (Patch Panel)	VOLTMETER receives input from VM patch terminal on Control Tray 0.12.1607.
A BAL (Amplifier Balance)*	Connects the stabilizer of a selected amplifier to the meter for balancing purposes. Meter deflection should be less than 1/2 division deflection for balanced amplifier.
S BAL (Stabilizer Balance)*	Connects the stabilizer of either the servo amplifier or the amplifiers on the DFG setup panel to the meter for balancing.
P SEL	Connects an addressed pot to the meter for setting. This position is used primarily when computer does not contain a DVM and is operable only when the RANGE switch is in the NULL position.
30 (Volts)* 15 (Volts)* 10 (Volts)* 5 (Volts)* -10 (Volts)* -15 (Volts)* -RV (Relay Volts)*	These switch positions connect the various dc voltages in the computer directly to the meter.

*When balancing amplifiers or reading power supply voltages the RANGE switch is inoperative; the appropriate meter ranges are selected automatically.

1.5.2 The FUNCTION RELAY Controls

The pushbutton controls for the eight function relays operate in a manner similiar to the comparator controls. Two pushbuttons (one numbered, one blank) are associated with each function relay. The numbered pushbutton, when depressed, forces the relay to the set condition regardless of the patched logic inputs. The blank

pushbutton, when depressed, resets the relay. When the pushbutton is released, the function relay returns to the state dictated by the patch panel inputs. If the patch panel inputs are not patched they remain in the state selected by the pushbuttons. Consequently, with no logic signals patched to its inputs, the function relay can be used as a manual function switch controlled by its associated pushbuttons.

1.5.3 The Handset ATTENUATORS

Ten handset ATTENUATORS (P00 to P09) are provided on the auxiliary control panel. Each ATTENUATOR is addressable on the signal selector system and is set in a manner similar to the servo set attenuators except that they are manually adjusted. Set each ATTENUATOR to the desired value using the DVM as a readout device. If the computer does not contain a DVM, the ATTENUATORS have to be set using the nulling method on the VOLTMETER.

1.6 THE LOGIC CONTROL AND INDICATOR PANEL

The logic control and indicator panel (Figure 1.14) is located at the upper left of the analog patch panel. The panel contains the digital patch panel, AND gate indicators, the REGISTER indicators and pushbutton controls, the indicators and thumbwheel controls for the COUNTERS, the general purpose PUSHBUTTONS and repetitive operation TIME controls (A and $\overline{A}$). The operation of the various controls and indicators mentioned above are described in the following paragraphs.

1.6.1 The Digital Patch Panel

The digital patch panel (Figure 1.15) is used to provide access to the inputs and outputs of the logic devices in the logic package. Physically the logic patch panel is divided into four fields (0 through 3) and three trunk areas (0 through 2). Each of the fields and trunk areas are similar in layout. The particular patching areas and the patch termination functions are described with their associated units.

1.6.2 The AND Gate Display

The AND gate display is provided to indicate the output state of each individual AND gate. When the indicator is lit, the output of the gate is high. The indicator is numbered and lettered to correspond to the gates, and in addition, is laid out in the same configuration as the terminations on the patch panel.

1.6.3 The REGISTER Controls and Indicators

A fully expanded 580 Computer logic package contains four registers of four bits each for a total of 16 flip-flops. A numbered pushbutton and the adjacent blank pushbutton are provided as manual controls and indicator for each flip-flop. The numbered pushbutton lights when the flip-flop is set and is extinguished when cleared. The numbered pushbutton also serves as a manual control; depressing it sets the flip-flop. The blank pushbutton is not used as an indicator but serves as a manual clear control for its associated flip-flop.

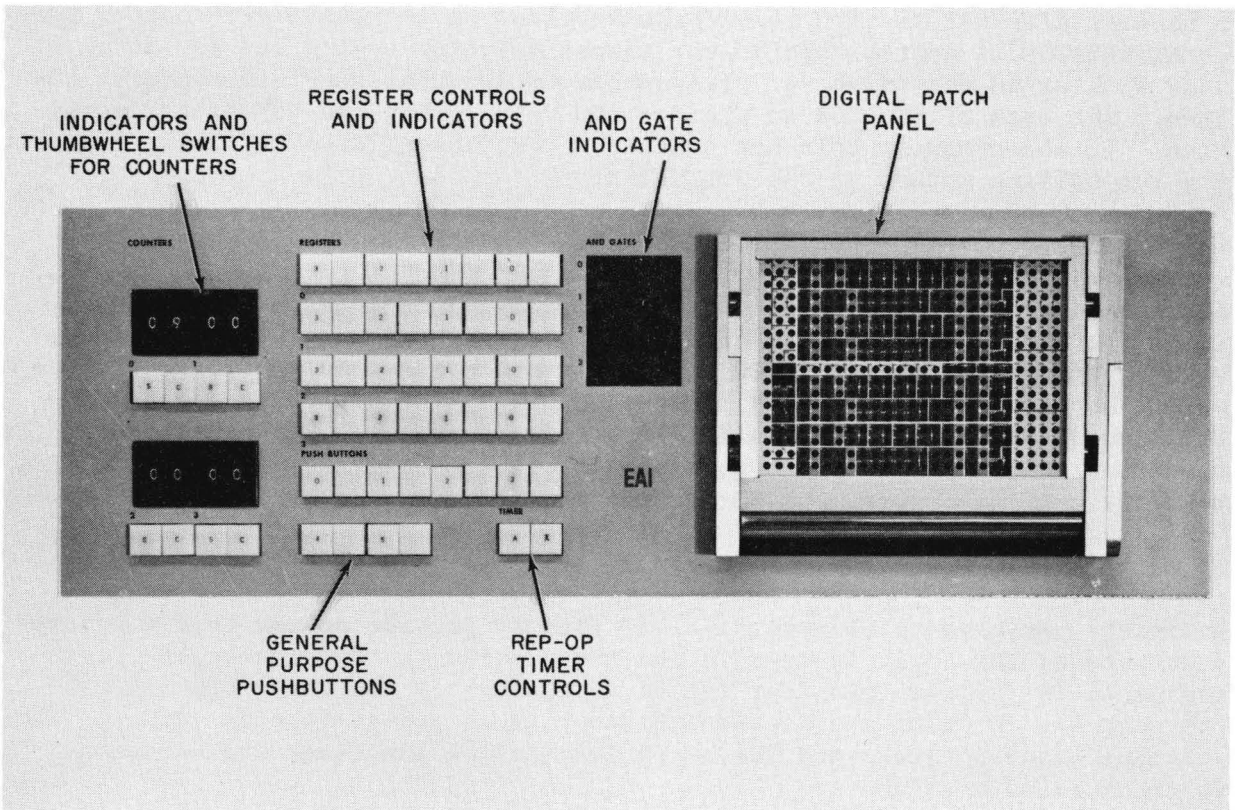


Figure 1.14. Logic Control and Indicator Panel

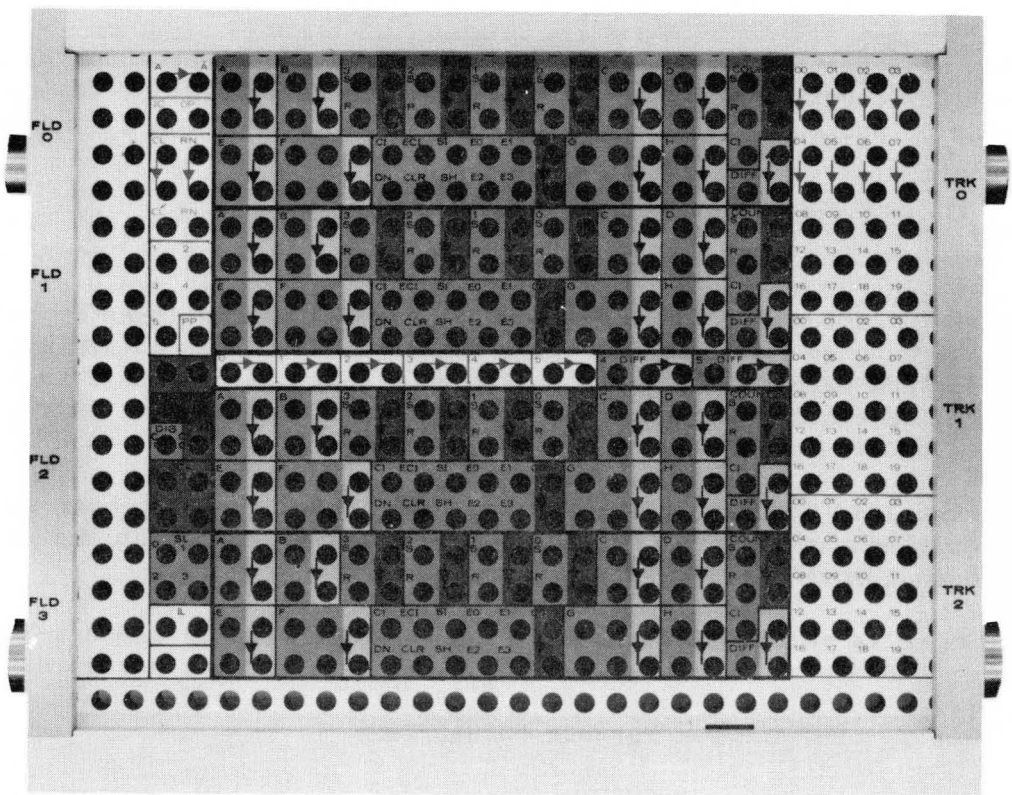


Figure 1.15. Digital Patch Panel

The registers are numbered 0, 1, 2 and 3 while the flip-flops within the registers are numbered in the reverse order. The reverse order of the flip-flops is necessary since, by convention, the most significant bit of a counter is considered to be on the left.

1.6.4 The COUNTER Controls and Indicators

A fully expanded 580 Computer logic package contains four counters which may be used for counting or timing functions. Manual control of the counter is provided by pushbuttons S (set) and R (reset). Pushbutton S contains an indicator lamp; it lights whenever the counter output is high.

Depressing pushbutton S sets the output flip-flop and loads the counter. When the count reaches 00, the output flip-flop is reset, and the counter output goes low. The output stays low until the output flip-flop is again set (the counter is loaded). Automatic loading of the counter is accomplished by patching the output through an AND gate (for time delay) to the S patch terminal. The second input for the patched AND gates serves as a controlling input; that is the AND gates can be patched to make the counter operation dependent on two or more separate output functions.

The preset load value is simply a matter of selecting the proper count while the left thumbwheel represents the tens count. In the event the count is less than 10 (0 through 9) the left thumbwheel is set to zero.

The counter is reset by patching a high to the R (reset) patch terminal or depressing the manual reset (R) pushbutton on the computer keyboard.

1.6.5 The General Purpose PUSHBUTTONS

The six general purpose PUSHBUTTONS provided in the 580 Computer logic package are latching-type switches whose outputs are terminated on the patch panel. Two pushbutton controls are provided for each switch. The numbered pushbutton is used to set the switch (output is high), and the adjacent pushbutton (blank) is used to reset the switch (output low). The numbered pushbutton also contains an indicator which, when lit, indicates that the associated output is high. When the output of a PUSHBUTTON is zero, depressing the blank pushbutton associated with that output, generates a synchronized pulse (one clock period in length) available at the output terminal.

1.6.6 The TIMER Controls

The rep-op TIMER controls (A and $\overline{A}$) are used to manually force the timer into the corresponding modes (A = IC, $\overline{A}$ = OP). The A pushbutton contains an indicator circuit which lights when the timer is in the IC mode.

1.7 READOUT DEVICES

The problem solution obtained with the 580 may be permanently recorded or temporarily displayed on several types of readout devices. The DVM or VOLTMETER, discussed previously, may be used to measure steady-state computational voltages. In repetitive operation, the computer solution is displayed on an

oscilloscope and a permanent record can be obtained by photographing the oscilloscope trace. X-Y plotters, such as the EAI 1110 VARIPLOTTER®, or strip chart recorders, such as the EAI 8875 RECORDER, can also be used to display problem variables. These readout devices are connected to the 580 Computer by means of the connectors provided on the connector panel (Figure 1.16) located at the rear of the computer.

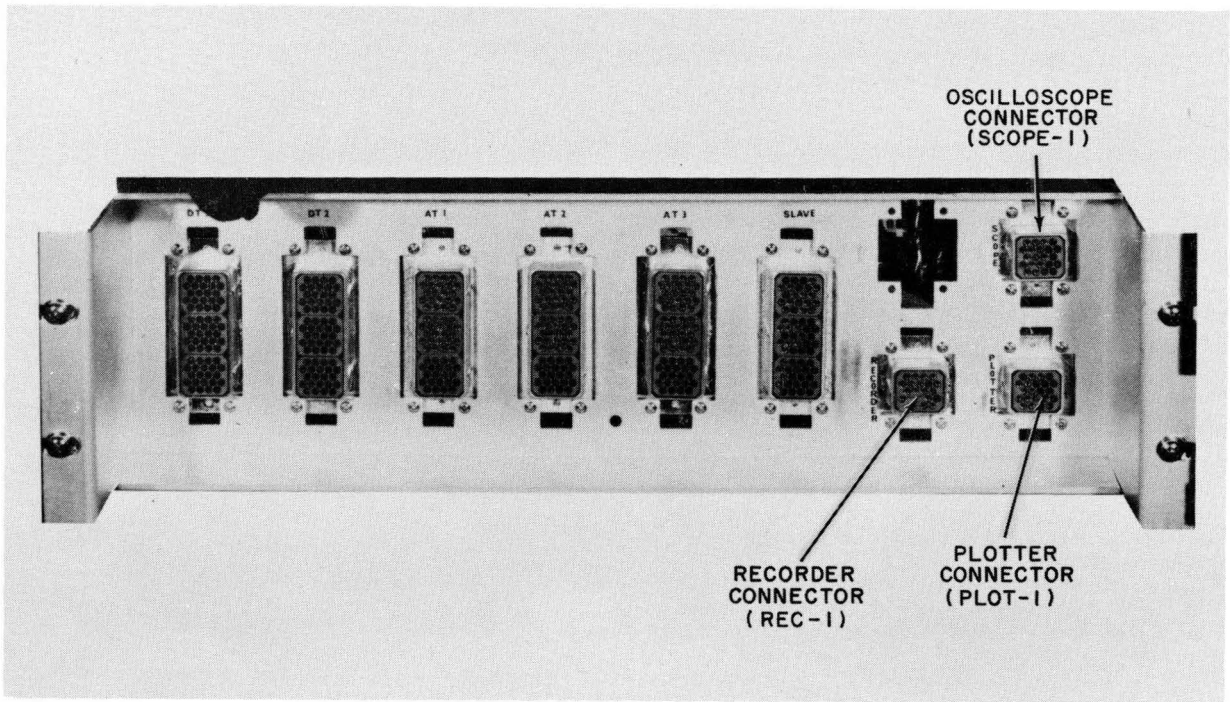


Figure 1.16. Readout Device Connectors

CHAPTER 2

OPERATIONAL AMPLIFIERS

2.1. INTRODUCTION

The operational amplifier is the basic computing element in an analog computer. The amplifier may be used in conjunction with appropriate networks to perform linear computations such as summation, integration, multiplication by a constant, and inversion. Accessory components permit use of the amplifier for nonlinear operations such as multiplication and division of variables, and the generation or analytic or arbitrary functions.

There are two amplifiers used in the 580. These are:Dual DC Amplifier, Model 0.6.614-1 and Quad DC Amplifier, Model 6.704-2. Figure 2.1 shows the patch block layout and simplified schematic of each amplifier type and the associated resistor network.

2.2 DUAL DC AMPLIFIER PATCHING

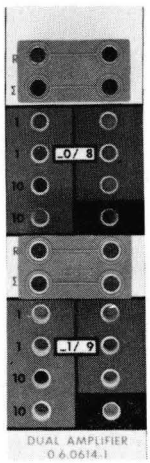
The input and output terminations of the dual amplifier and dual resistor networks are terminated at the pre-patch panel and are arranged for ease of patching. The nonlinear components are also located in close proximity to the amplifiers for ease of patching and short patch cord runs.

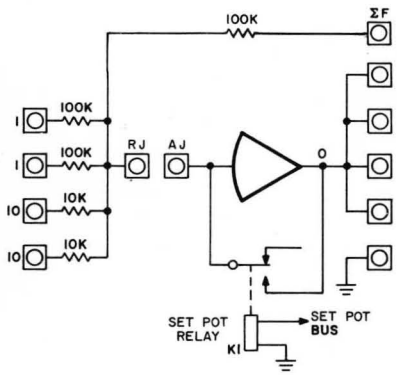
Patching an amplifier for use with an integrator network, or one of the nonlinear components, is covered in the separate sections of this manual pertaining to the particular component. This section is limited to the description of the amplifier used in conjunction with a resistor network.

Figure 2.2 illustrates two of the more common patching arrangements for the Model 0.6.614-1 Amplifier. The patching shown for the upper amplifier (Figure 2.2a) makes use of the standard 4-pin bottle plug and provides the summing circuit shown schematically in Figure 2.2b. This configuration has two gain-of-one and two gain-of-ten inputs. The basic programming symbol for this circuit is shown in Figure 2.2c. Note that the amplifier address number is normally placed in the triangle. Normally, only those inputs to be used are shown.

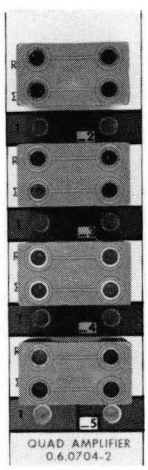
The lower amplifier (Figure 2.2a) is patched for one gain-of-one and three gain-of-one-tenth inputs using two 2-pin bottle plugs. The simplified schematic and programming symbol for this configuration are illustrated in Figures 2.2d and e. Additional input resistors can be made available by connecting the RJ terminations of different resistor networks together as shown in Figure 2.2f.

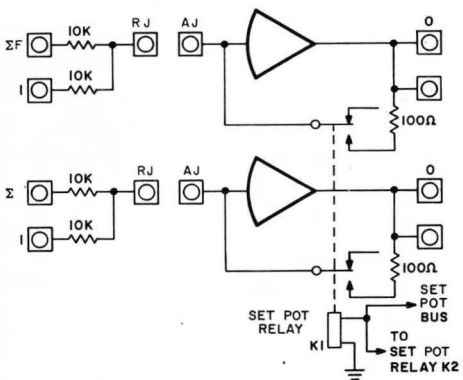
Resistors may be patched in series or parallel in the input or feedback circuit to obtain desired gains. Some of these configurations are summarized in Appendix 1.





(a) 6.614-1 Dual DC Amplifier Patch Block and Simplified Schematic (One Channel)





(b) 6.704-2 Quad DC Amplifier Patch Block and Simplified Schematic

NOTES:

1. SET POT RELAYS SHOWN IN DE-ENERGIZED CONDITION.
2. DUAL AMPLIFIERS HAVE 1 SET POT RELAY EACH. QUAD AMPLIFIERS HAVE 2 SET POT RELAYS EACH.

Figure 2.1. 580 Operational Amplifiers

(Patch Block Layout and Simplified Schematics)

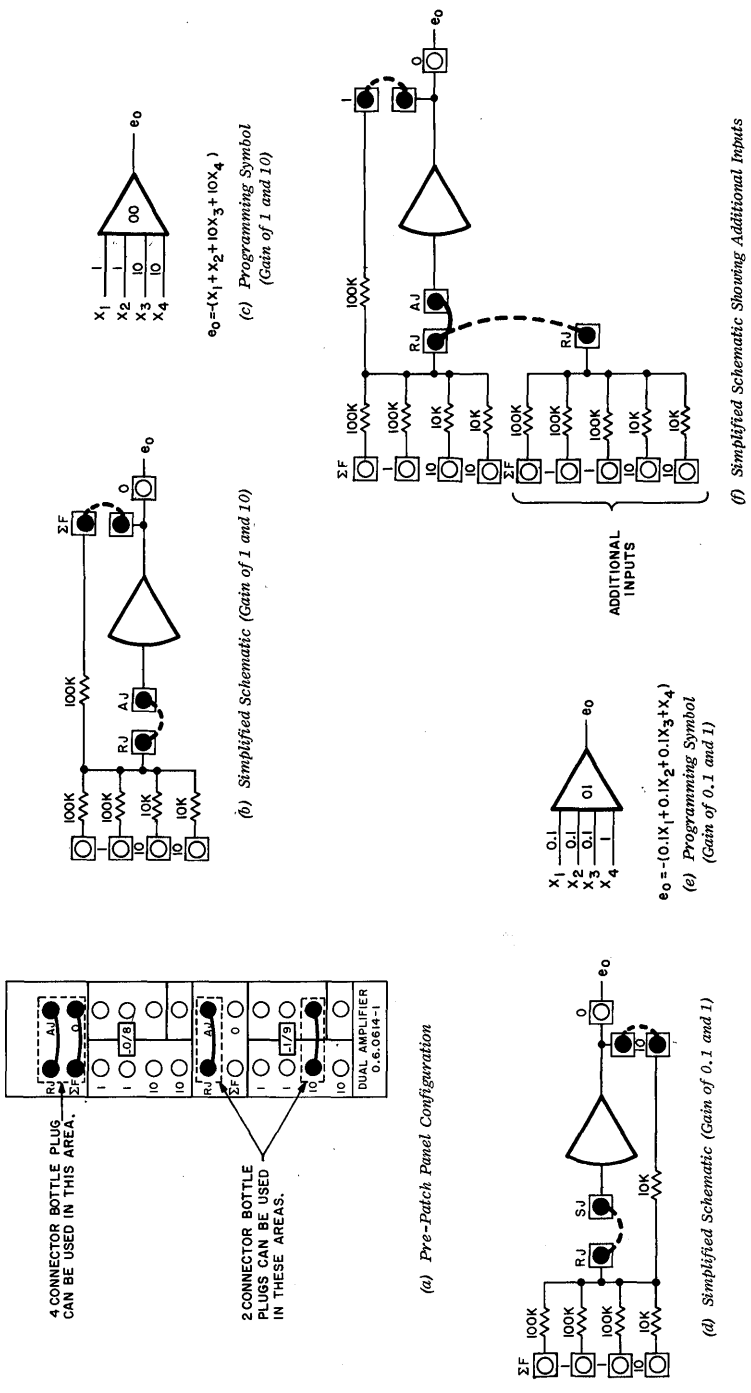


Figure 2.2. Dual Amplifier, Typical Patching Configurations

2.3 QUAD DC AMPLIFIER PATCHING

The 580 Computer has provisions for up to eight Quad DC Amplifiers, Model 0.6.704-2 installed in the patch bay. The quad amplifiers have 10K ohm input and feedback resistors for each amplifier circuit. This permits wide bandwidth, low offset, inversion. The 10K ohm resistors are accurately matched to ensure true unity gain inversion. Figure 2.3 shows the normal patch configuration for one amplifier of a quad.

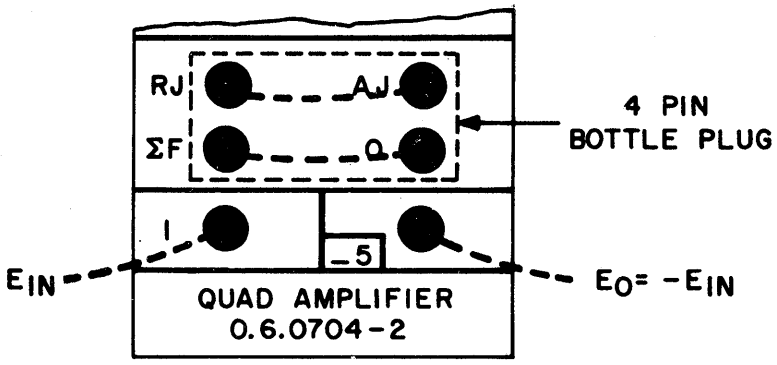


Figure 2.3. Quad Amplifier Patching Configuration

CHAPTER 3

ATTENUATORS AND FEEDBACK LIMITERS

3.1 ATTENUATORS

3.1.1 Introduction

The 580 Computers have provisions for 10 handset attenuators (Figure 3.1a) and 70 servo set attenuators (Figure 3.1b) when fully expanded. Each row of attenuators (one row of handset attenuators and seven rows of servo set attenuators) is terminated in a particular field on the patch panel. The first digit in the attenuator address indicates the field number. For example, the handset attenuators are all terminated in FIELD 0 and are numbered 00 through 09. Each row of the seven rows of servo set attenuators is terminated in a particular field. With the exception of the ungrounded attenuator in each _4 position, all attenuators in a particular field have one end internally grounded with the ungrounded end and the wiper terminated on the patch panel. The ungrounded pot in each field has both ends and the wiper terminated on the patch panel.

The standard potentiometers are ten-turn, wirewound, 5000 ohm units. The handset attenuators are equipped with vernier dials that have a locking mechanism.

3.1.2 Grounded Attenuators

Figure 3.2a shows the circuits used in the 580 for setting grounded attenuators under load. Relay K1 is energized when the computer is placed in <u>set pot</u> mode and applies reference voltage to the high end of all grounded attenuators. Relay K2 is energized when the attenuator is addressed by the signal selector system. The wiper voltage is connected to the input of the DVM. The wiper is still connected to the patch panel and is patched to the load it sees when in use. The wiper of the attenuator is adjusted until the desired coefficient is obtained on the DVM.

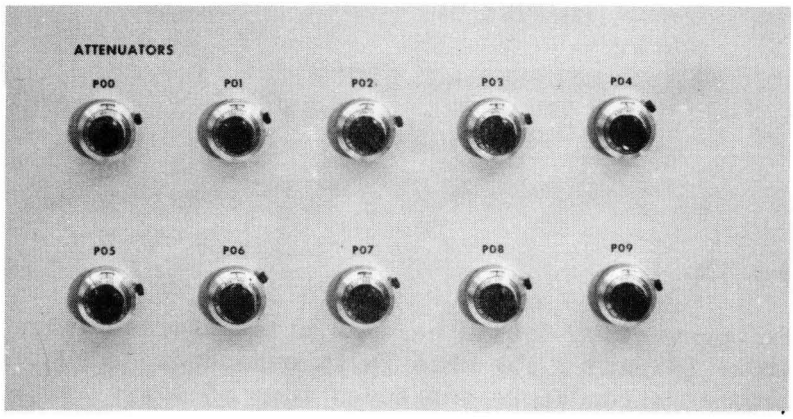
3.1.3 Ungrounded Attenuators

The operation of the ungrounded attenuators (Figure 3.2b) is similar to the grounded attenuators except that the lower terminal is not internally grounded. <u>Prior to setting an ungrounded attenuator, the lower terminal must be patched to ground.</u> If setting is attempted without the ground connection, the servo drives the attenuator to its highest resistance. The attenuator is held in this position until the CLR pushbutton is depressed and the attenuator is grounded. The ground can be removed from the attenuator once it is set and its address removed.

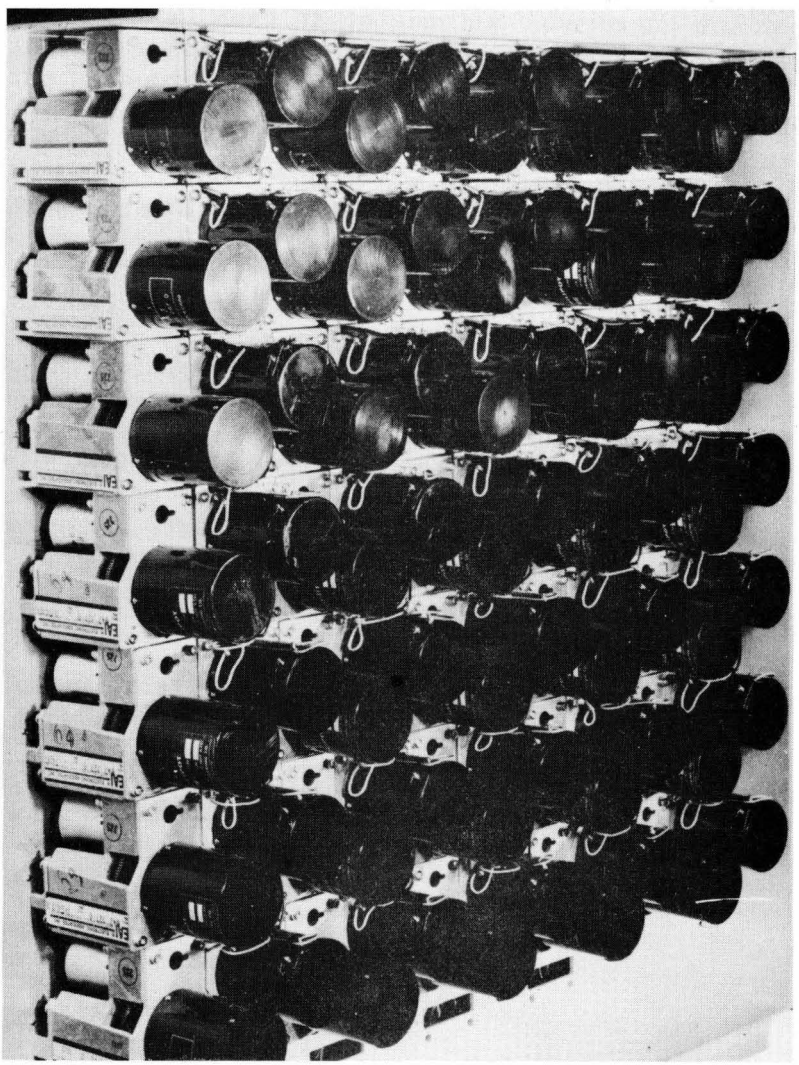
3.2 FEEDBACK LIMITER

3.2.1 General

Feedback Limiter, Model 0.42.0342 provides three variable and accurate feedback limiters capable of limiting either or both the positive and negative amplifier outputs.

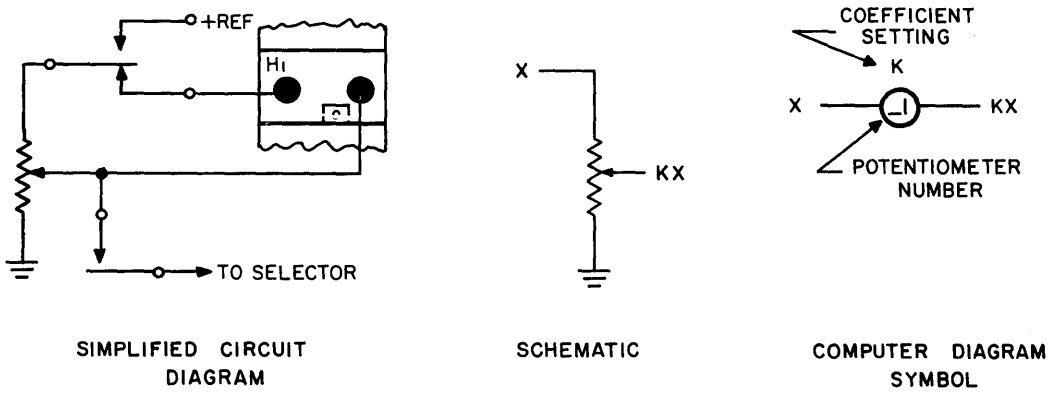


(a) Handset Attenuators

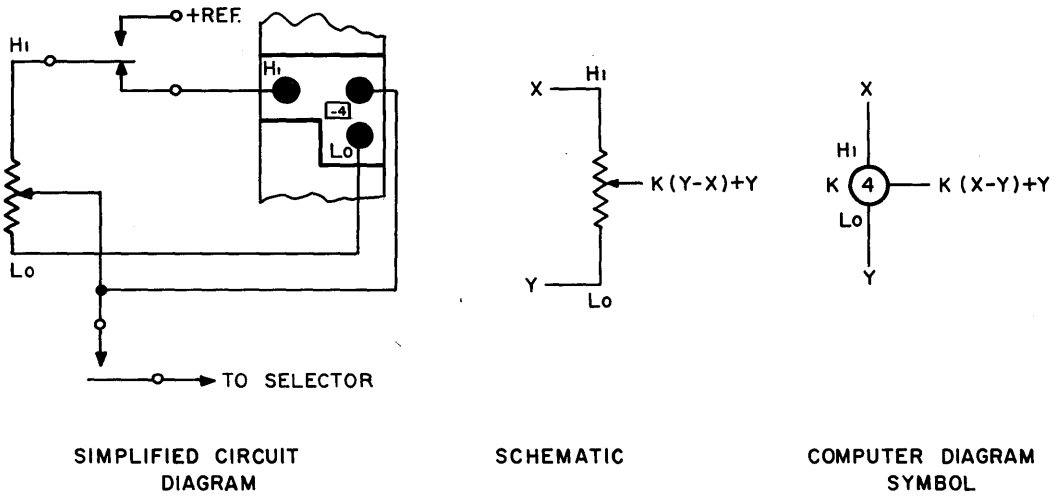


(b) Servo Set Attenuators

Figure 3.1. Attenuators



(a) Grounded Potentiometer



(b) Ungrounded Potentiometer

Figure 3.2. Potentiometer Configurations

The 0.42.0342 Module may be installed in any Track/Store potentiometer module slot in the pre-patch panel area. In addition to the limiter terminations, this module retains the patching terminations for the potentiometer group normally terminated in the area used. The patch block configuration is illustrated in Figure 3.3. The five potentiometers are all available for standard potentiometer use when the limiters are not in use. When the limiters are in use, the potentiometers become the limit adjustment controls. When all limiters are used for ± limiting a sixth attenuator has to be patched from another position.

3.2.2 Patching Configuration

Whether used in conjunction with the limiter or not, the five potentiometers can be selected for readout and/or setup using the standard procedure.

Figure 3.4 illustrates a typical patching configuration for the upper limiter of the network. The amplifier to be limited is patched in its normal circuit configuration. The limiter is then patched around the amplifier with the LJ to AJ and FB to 0 connections as shown. The patching is completed by connecting the Hi-side (top) of two potentiometers to the appropriate reference levels and the wipers to the proper limiter inputs.

3.2.3 Setting the Limit Value

The diode action of the base-emitter junction causes a small amount of "rounding" (or knee) in the amplifier limited output waveform as shown in Figure 3.5. The procedure for setting the limiter depends on whether the programmer prefers the knee to fall above or below the limit value. To set the knee below the limit value proceed as follows: Apply reference as the input to the amplifier (opposite in polarity to the output voltage to be limited). Adjust the limit pot to the desired limit value. The knee will start before the limit value is reached, and the amplifier output will not exceed the set value. To set the knee above the limit value proceed as follows: Apply an input that provides the amplifier with an unlimited output equal to the desired limit value. Adjust the limit pot to the point where the limiter just starts to function and then "back-off" the control slightly. The knee will start at the set limit value.

If it is desired to limit the amplifier output at ± reference, the ±L potentiometers can be eliminated from the circuit by patching + reference directly to -L (- reference output limit) or - reference directly to +L (+ reference output limit).

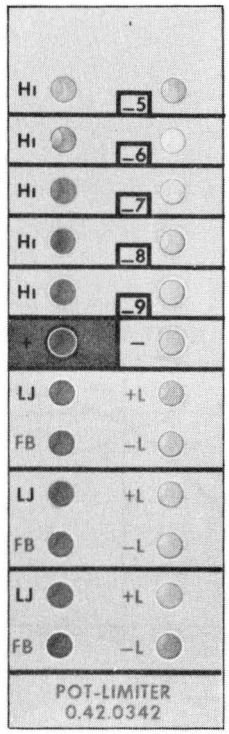
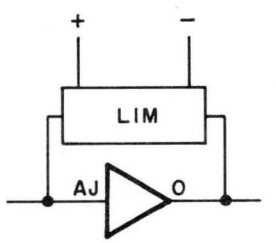
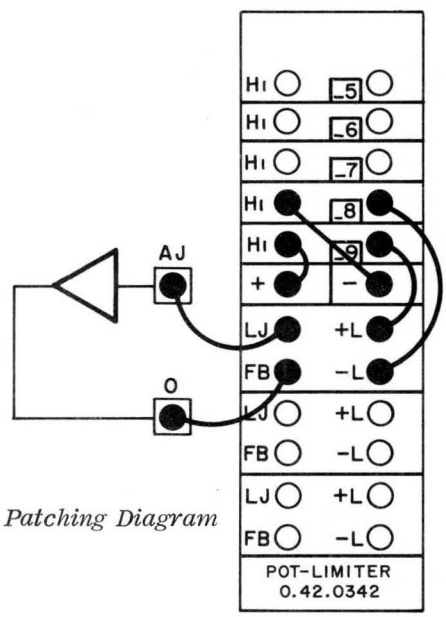


Figure 3.3. Feedback Limiter Patching Block



(a) Computer Diagram



(b) Patching Diagram

Figure 3.4. Typical Limiter Patching

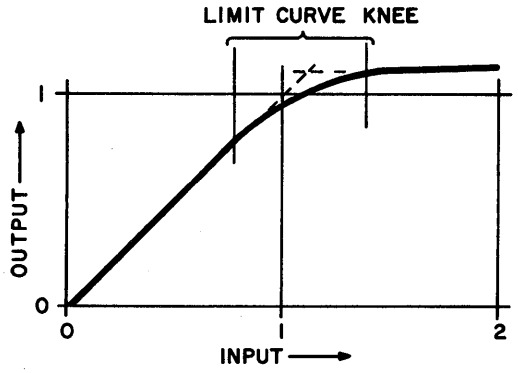


Figure 3.5. Limit Curve

CHAPTER 4

INTEGRATORS

4.1 INTRODUCTION

This chapter includes operating information for the 0.12.1611 Dual Integrator Tray and the 0.12.1675 Potentiometer, Integrator Tray. The patching blocks for these integrators are shown in Figure 4.1. This chapter also includes operation of the repetitive operation group, which controls the integrators when the computer is in the rep-op mode.

4.2 INTEGRATOR TRAYS

The 0.12.1611 Dual Integrator Tray and the 0.12.1675 Potentiometer, Integrator Tray are similar except that the 0.12.1675 contains only one integrator while the 0.12.1611 contains two. The operation of each integrator section of each tray is identical. Consequently only the dual integrator is discussed in this chapter.

The integrators are typically patched as shown in Figure 4.2. Note that in each field, the integrator trays are physically located adjacent to a dual dc amplifier to facilitate the usage of bottle plugs for patching.

4.2.1 Integrator Mode Control

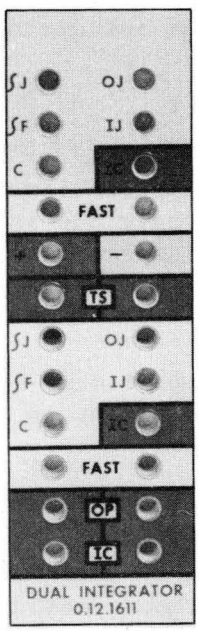
The initial condition (IC), operate (OP), and hold (HD) integrator modes are controlled by logic signals. The table below gives the necessary logic levels at the various control terminals to establish the control modes.

Table 4.1. Integrator Control Modes

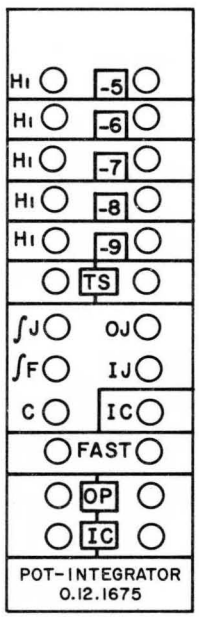
IC Input	OP Input	Resulting Mode
0	1	OP
1	0	IC
0	0	HD
1	1	IC

These modes can be controlled either automatically or manually. The typical patching diagram (Figure 4.2) indicates automatic control utilizing bottle plugs. In this method, bottling the OP and IC terminals with a four prong bottle plug connects the OP and IC terminals to their respective buses. Control of these buses is established at the main control panel and is discussed in Paragraph 1.3.5 of Chapter 1.

Controlling these modes manually requires the removal of the four prong bottle plug and patching externally generated logic signals to the OP and IC input



(a) Dual Integrator



(b) Single Integrator (With Attenuator Terminations)

Figure 4.1. Integrator Patching Blocks

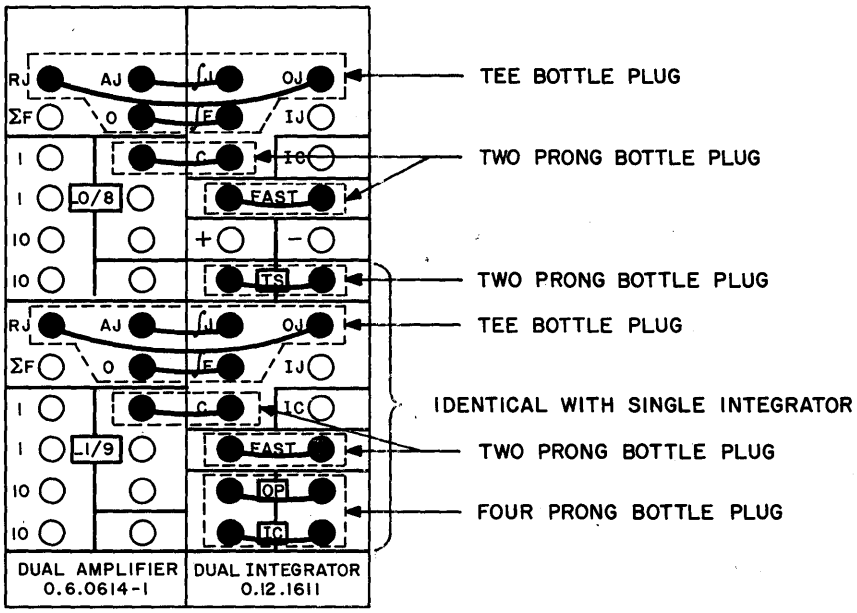


Figure 4.2. Typical Integrator Patching

(green) patch terminals. Refer to Table 4.1 for the proper logic signals for the desired mode.

4.2.2 Integrator Capacitor Selection

Each integrator is provided with four capacitors (10 μf, 1 μf, 0.02 μf, and 0.002 μf) which provide time constants of 1 second, 0.1 second, 2 milliseconds, and 0.2 millisecond respectively when used with a standard gain-of-one (100K) resistor. Capacitor selection is determined by logic levels on the TS (time scale) and the proper patching of the FAST input terminals.

Bottling the TS patch terminals connects the TS input to a master time scale bus. The logic levels in this bus are: controlled by the TIME SCALE push-buttons on the main control panel. The operation of the TIME SCALE pushbutton is described in Paragraph 1.3.5 of Chapter 1. Removal of the TS bottle plug provides access to the TS input (green) terminal. Externally generated logic levels can be patched to this terminal to provide manual control of the TS relay. A low (grd) patched to the TS terminal energizes the TS relay placing it in the 2 ms state while a high (+ voltage or no connection) patched to the terminal de-energizes the TS relay placing it in the 1S state.

The FAST terminals, when bottled, effectively slow down computer operation by increasing the value of the integrator feedback capacity. This is accomplished by paralleling the 1 μf capacitor with a 9 μf capacitor in the 1S mode and paralleling the 0.002 μf capacitor with a 0.018 μf capacitor in the 2 ns mode. Table 4.2 gives the necessary patching and time scale selection for different time constants.

Table 4.2. Time Constant Selection

TIME SCALE Switch	FAST Terminals	Feedback Capacitor	Time Constant (with 100K Input)
1 SEC	Bottled	10 μf	1.0 SEC
1 SEC	Not Bottled	1 μf	0.1 SEC
2 MS	Bottled	0.02 μf	2.0 MS
2 MS	Not Bottled	0.002 μf	0.2 MS

4.2.3 Additional Integrator Uses

Any integrator not used for a particular problem can, by proper patching, be used as 1) an extra D/A switch, and 2) as a differentiator. The paragraphs below describes these additional uses for the integrator.

4.2.3.1 D/A Switch. To use the integrator as a D/A switch, remove the bottle plug between the C terminal and the amplifier output. Connect a two prong bottle plug between an amplifier gain-of-one input and the amplifier output. Patch the signals to be switched in the IC patch terminal and the remaining gain-of-one amplifier inputs. The resulting circuit is shown on Figure 4.3. If the four prong bottle plug is left in the OP and IC patch terminals,

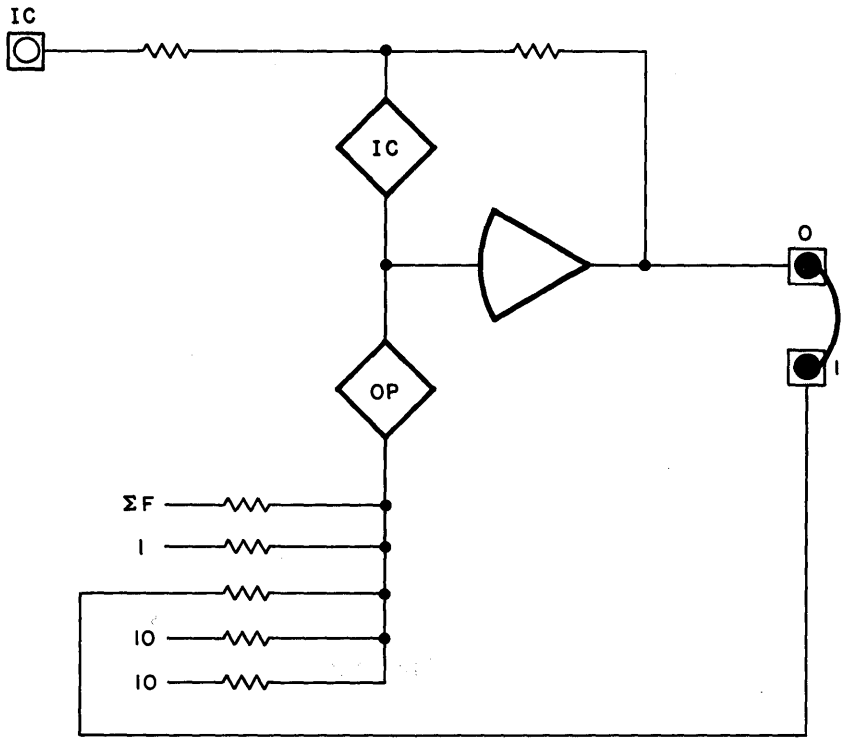


Figure 4.3. Integrator Used as a D/A Switch

the D/A switches operate at the REP-OP rate. The D/A switches can be operated independently of the REP-OP rate by removing the four prong bottle plug and patching external logic signals to the OP and IC input (green) patch terminals.

4.2.3.2 Differentiator. To operate the integrator as a differentiator remove the bottle plug from the C patch terminal. Connect two prong bottle plug between a gain-of-one amplifier input and the amplifier output. Select the desired capacitor value (see Paragraph 4.2.2, this chapter). Patch the signal to be differentiated to the C patch terminal. The resultant differentiated signal appears at the output of the amplifier.

CHAPTER 5

QUARTER-SQUARE MULTIPLIERS

5.1 INTRODUCTION

This chapter provides information on the operation of the quarter-square multipliers used in the 580 Computer. The multipliers available in the 580 Computer include the 0.7.0146 High Accuracy Quarter-Square Multiplier, the 0.7.0148 Quarter-Square Multiplier, and the 0.7.0150 Quarter-Square Multiplier (Figure 5.1). Each of these multipliers are used in conjunction with dc amplifiers to produce a four quadrant product of two variables, X and Y. In addition to multiplication, each of the multipliers is also capable of division. The upper multipliers in the 0.7.0146 and 0.7.0148 Trays are provided with extra patching terminals to permit patching each squaring circuit separately (Figure 5.2a). This provision allows the upper multipliers in these trays to be utilized, additionally, for squaring and square root functions.

5.2 MODEL 0.7.0146 AND 0.7.0148 QUARTER-SQUARE MULTIPLIERS

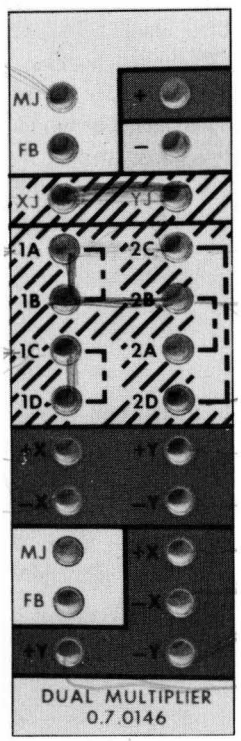
Since the patch blocks and patching procedures for the 0.7.0146 and 0.7.0148 Quarter-Square Multipliers are identical, only the 0.7.0146 is described below.

Figure 5.2 is a simplified diagram of the multiplier. Note that the multiplier is patched to an amplifier in a typical configuration. The inputs are not shown patched to simplify the diagram. The function of each input terminal is given in Table 5.1.

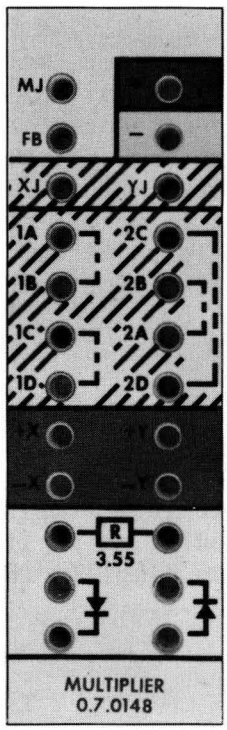
Table 5.1. Multiplier Input Functions

Patch Terminal	Function	Destination
1A	+X	+ squaring card in upper multiplier
1B	+Y	
1C	-X	- squaring card in upper multiplier
1D	-Y	
2C	+X	+ squaring card in lower multiplier
2B	+Y	
2A	-X	- squaring card in lower multiplier
2D	-Y	

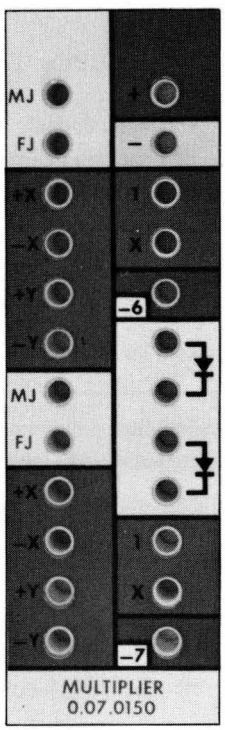
Figures 5.3 through 5.6 show multiplier patching for multiplication, division, squaring, and square root functions respectively. Note that each multiplier (upper and lower) has only one feedback resistor. For squaring and square roots functions (Figures 5.5 and 5.6) the upper squaring cards are patched separately. The output amplifiers patched to YJ in the 0.7.0146 Multiplier must have an external feedback resistor patched. A feedback resistor (3.55K ohms) is provided for this purpose in the 0.7.0148 Multiplier.



(a) 0.7.0146 Dual Multiplier

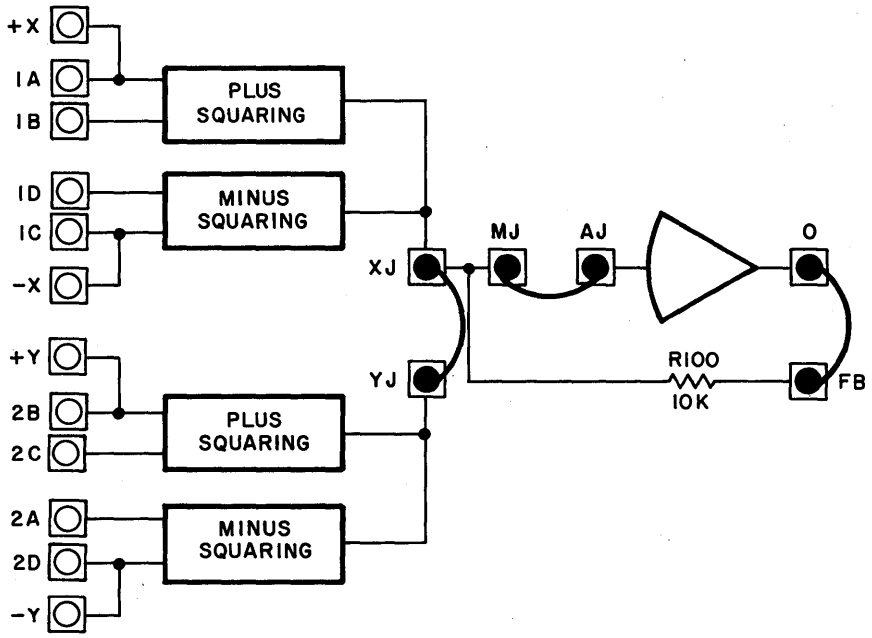


(b) 0.7.0148 Multiplier

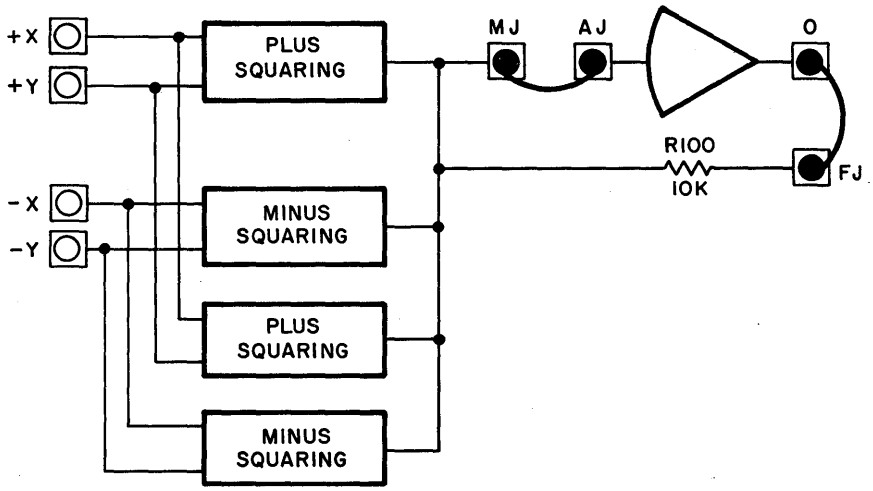


(c) 0.07.0150 Multiplier

Figure 5.1. Quarter-Square Multiplier Patch Blocks



(a) Upper Multiplier



(b) Lower Multiplier

Figure 5.2. Quarter-Square Multiplier, Simplified Diagram

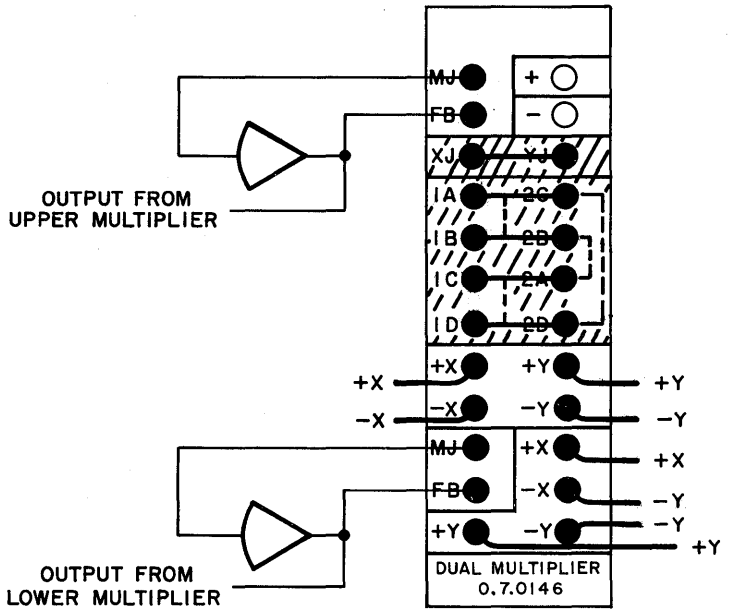


Figure 5.3. Multiplier Patching for Multiplication

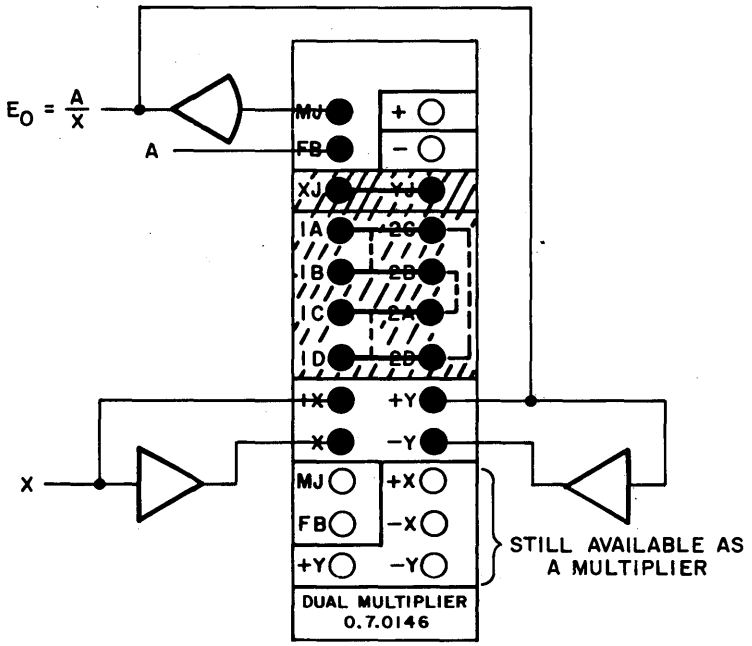


Figure 5.4. Multiplier Patching for Division

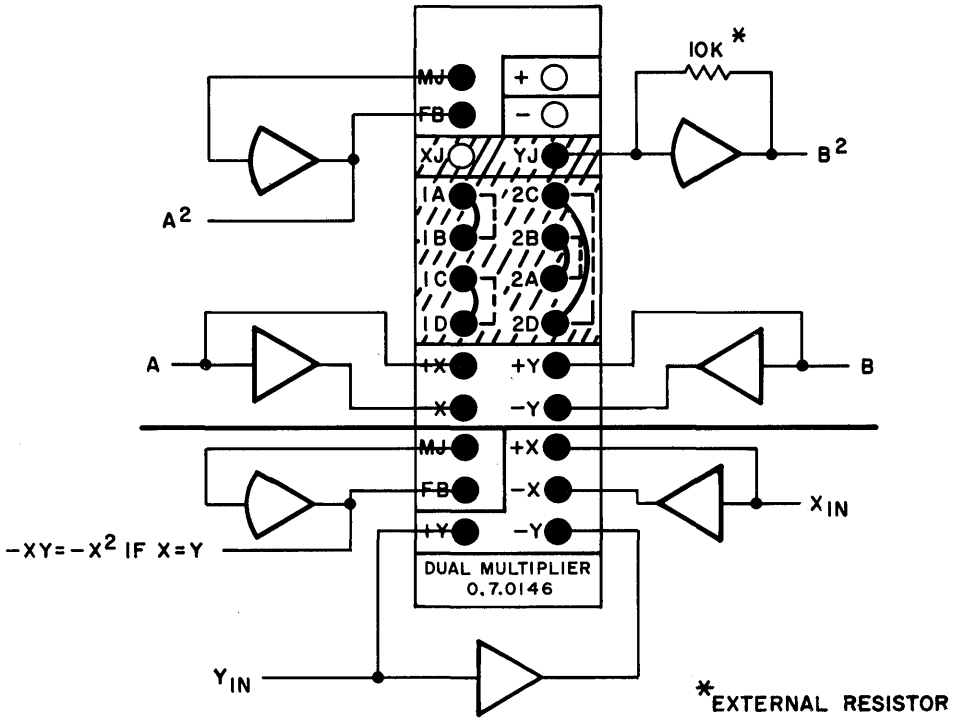


Figure 5.5. Multiplier Patching for Squaring (Two Squaring Circuits Shown)

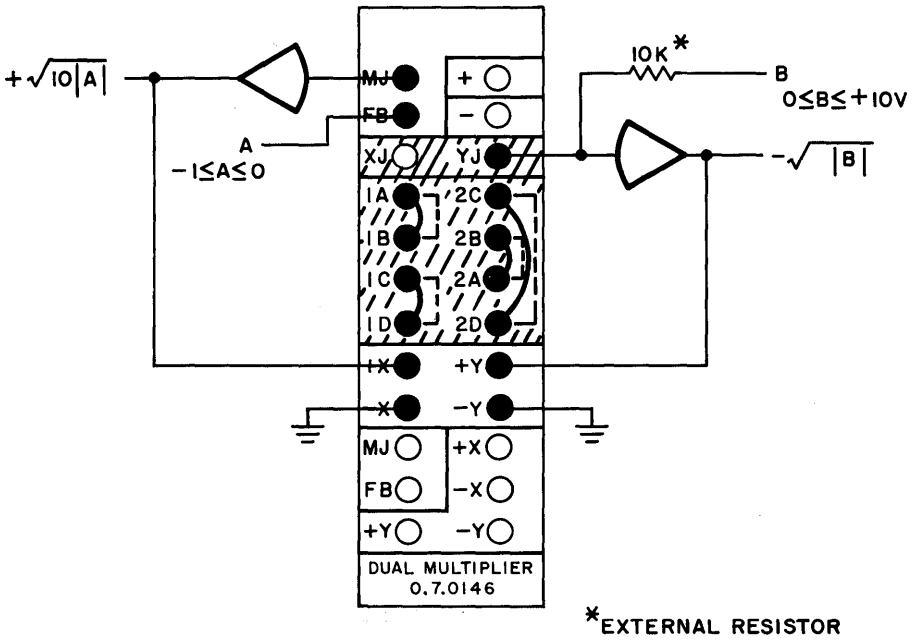


Figure 5.6. Multiplier Patching for Square Root

5.3 MODEL 0.7.0150 QUARTER-SQUARE MULTIPLIER

The 0.7.0150 Quarter-Square Multiplier (Figure 5.1c) includes two multiplier circuits, patching for two MDFG units and two free diodes for use as required by any particular problem. The MDFG readout patch terminals are described in Chapter 8.

Operationally, each of the multipliers in this tray are identical to the lower multipliers in the 0.7.0146 and 0.7.0148 Trays (Figure 5.2b). Physically, the feedback resistor patch terminal is identified as FJ instead of FB, and the patch holes have been relocated. These multipliers are capable of performing multiplication and division functions. Patching for these functions is shown in Figures 5.7 and 5.8.

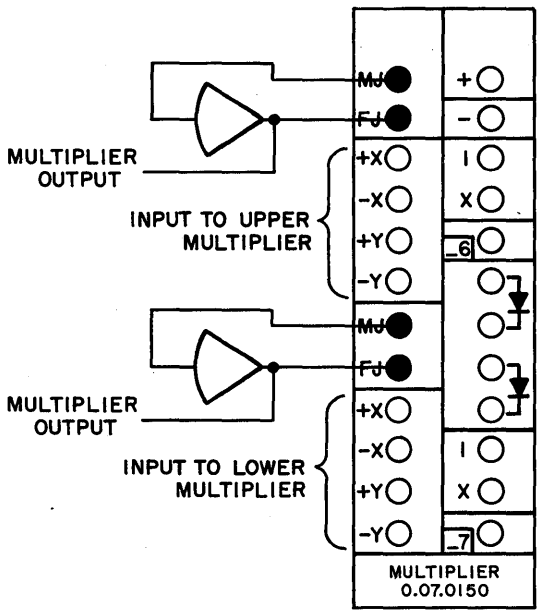


Figure 5.7. Multiplier Patching for Multiplication

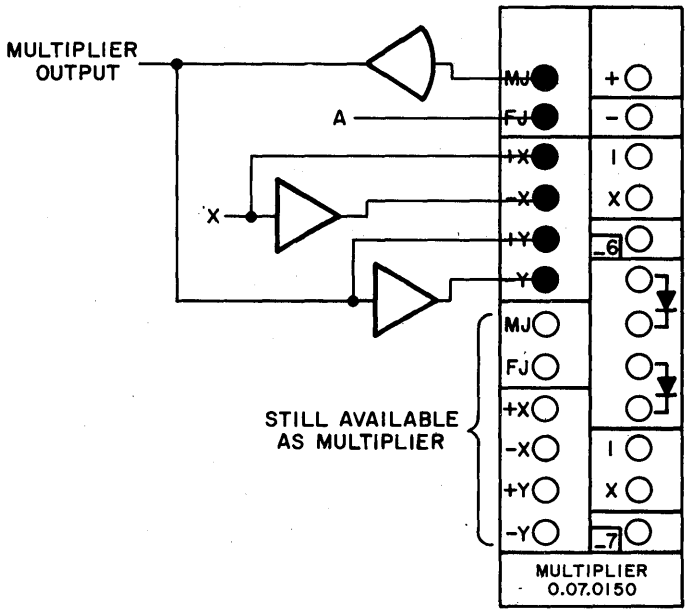


Figure 5.8. Multiplier Patching for Division

CHAPTER 6

LOG X DIODE FUNCTION GENERATORS

6.1 INTRODUCTION

The Log X DFG's operate in conjunction with an operational amplifier to produce an output voltage that is proportional to the logarithm of the input voltage. Common and natural logarithms and antilogarithms can be generated.

The inputs and outputs for the circuit configurations described in the following paragraphs are given on a unit-scaled basis. Computer reference is taken as basic unit of measurement so that all properly scaled voltages are ≤ 1.0 unit in magnitude. A description of unit-scaling and a tabulation of outputs for both unit-scaling and voltage-scaling is given in Appendix 4.

6.2 OPERATING CONSIDERATIONS

The Log X DFG, Model 0.16.0355, consists of four independent logarithmic function generators. Two of the generators accept a positive input voltage X and produce an output voltage of $-1/2 \log_{10} (-100X)$. The other two generators accept a negative input voltage X and produce an output voltage of $1/2 \log_{10} (-100X)$.

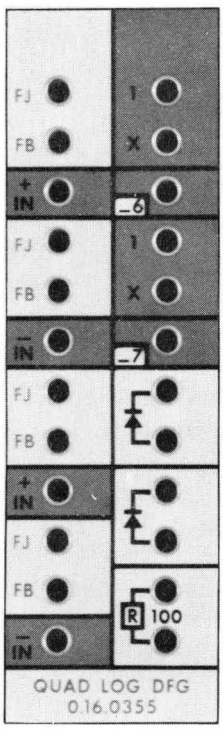
NOTE

The abbreviation log indicates the logarithm to the base 10. The abbreviation ln is used for natural logarithms (to the base e).

A simplified schematic of the log X DFG is shown in Figure 6.1. The four DFG's are independent and each has a resistor associated with it. The log X DFG patching terminations occupy the left side of the patch block. The right side is occupied by two MDFG amplifier patch terminations and two diodes and a 100 ohm resistor used as free components. The MDFG amplifier patch terminations are described in Chapter 8.

6.3 OPERATING INSTRUCTIONS

The patching for the DFG's is illustrated in Figure 6.2. Note that the input voltage is restricted to a range of 0.01 to 1.0 (reference). Since the DFG has a variable input impedance, input voltages should <u>never</u> be obtained from potentiometers. Care should be taken not to apply an input voltage of the wrong polarity. Although doing so will not harm the DFG, it can constitute a severe overload on the associated amplifiers in certain circuits.



PATCHING BLOCK

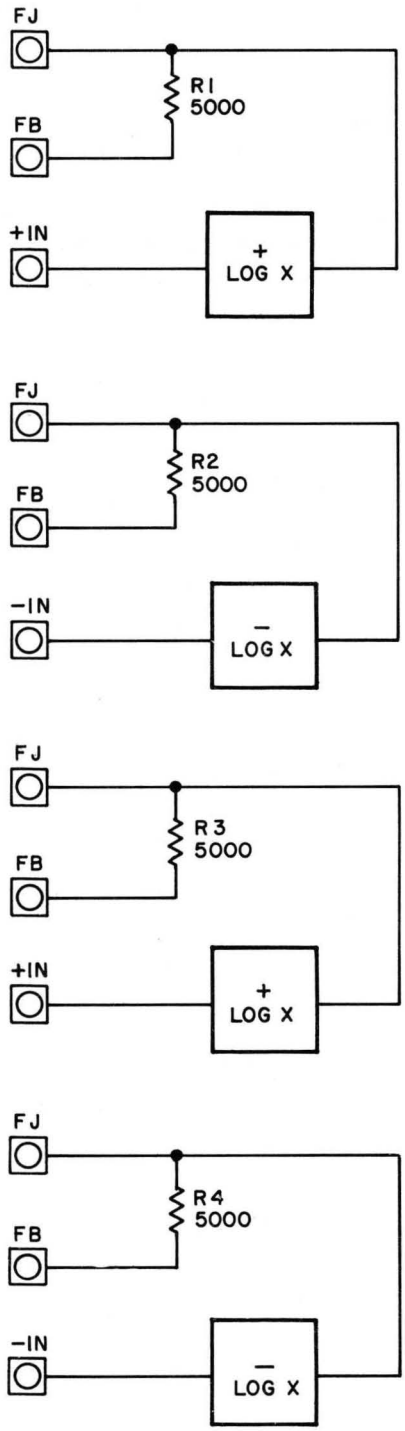


Figure 6.1. Log X DFG, Simplified Schematic and Patch Block

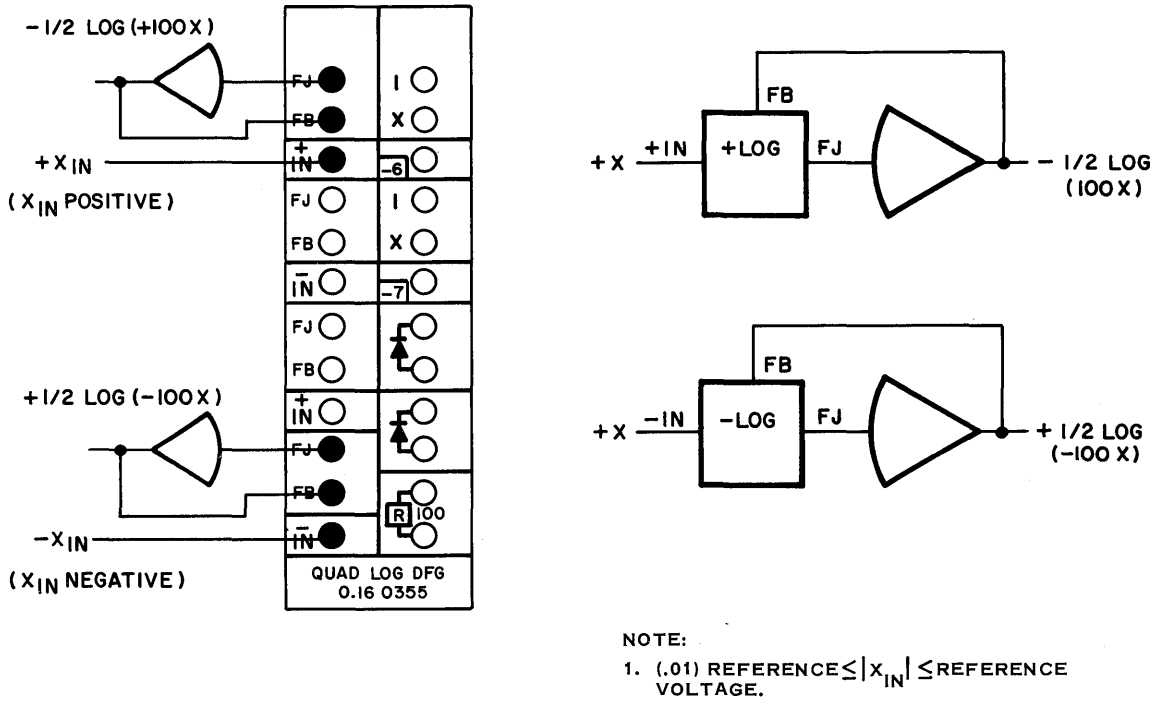


Figure 6.2. Log X DFG Patching

CHAPTER 7

THE TRACK-STORE, D/A SWITCH TRAY

7.1 INTRODUCTION

The Model 0.42.0341 Potentiometer, Track-Store, D/A Tray (Figure 7.1) has patching terminations for three different types of circuits. These include patching for five attenuators (-5 through -9), one track-store (T/S) unit and two D/A switches. A description of the attenuator operation is included in Chapter 3 of this manual, and is not discussed in this chapter. The remaining circuits (T/S and D/A) are described in the following paragraphs.

7.2 THE TRACK-STORE CIRCUIT

The track-store (T/S) circuit (Figure 7.2) consists of storage capacitors, three electronic switches (track, long store, and short store), an IC network, and a control circuitry.

Figure 7.3 gives typical T/S patching. The resistor junction (RJ) of an amplifier is patched to terminal TJ. The switch junction (SWJ) terminal and terminal TF are patched to amplifier terminals AJ and 0 respectively. Terminal T (track) is patched to a logic signal which controls the mode of the unit. The lower IC terminal (track IC input on Figure 7.2) is patched to a logic signal which places the unit in the IC mode. It overrides the T logic control signal. The upper IC terminal provides an input for the analog initial condition voltage for the store capacitors.

When the track (T) input is high, the track electronic switch is closed connecting the TJ terminal with SWJ, and the store electronic switches are open. A low at the T terminal causes the track switch to open and the store switch to close. Consequently, the unit is in the track mode when the T input is high and in the store mode when the T input goes low.

A high at the (track) IC terminal energizes a relay which connects the TJ terminal to the D/10 selector switch on the main control panel, permitting a derivative readout. A second set of relay contacts permits charging the store capacitors to the IC analog voltage through the IC terminal.

7.3 THE D/A SWITCH

The D/A switch and its control input are terminated at the SW, 10, and SWJ patching terminals (Figure 7.4). The SW terminal provides a control input. A logic signal at this point turns the switch on or off depending on its voltage level. A high (+5v) causes the switch to conduct while a low (0 volt) holds the switch in a non-conducting state.

The 10 terminal is 10X (10K) times input of the switch. Any analog input to be switched is patched at this terminal.

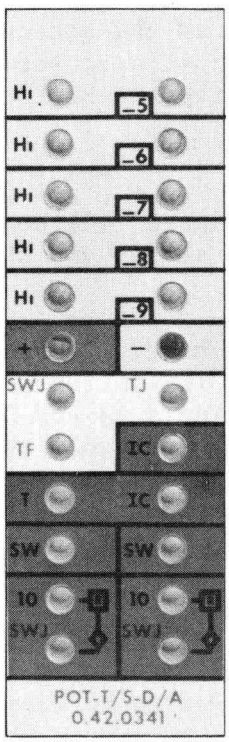


Figure 7.1. Track/Store, D/A Switch Patch Block

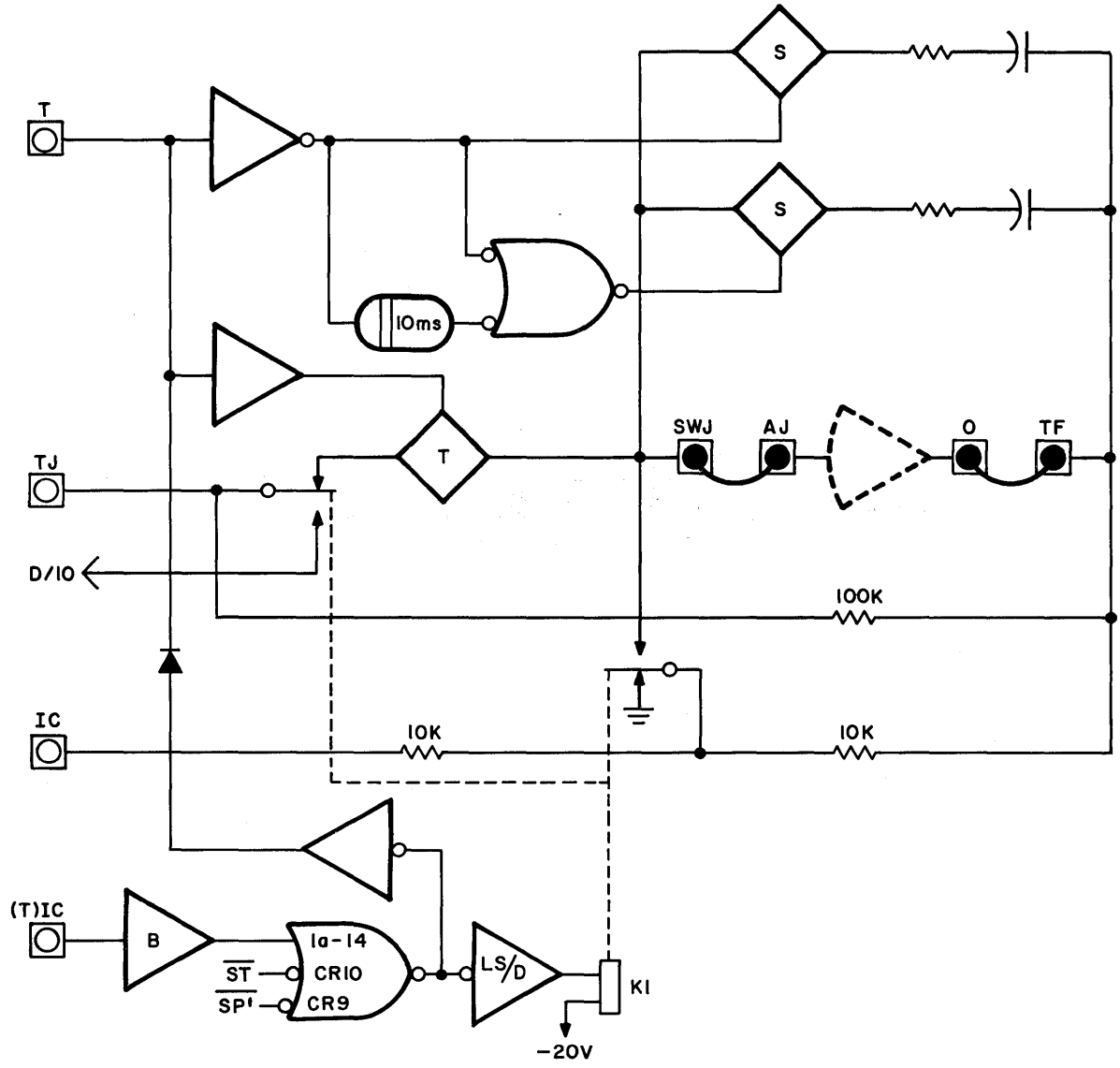


Figure 7.2. Track/Store Circuit, Simplified Diagram

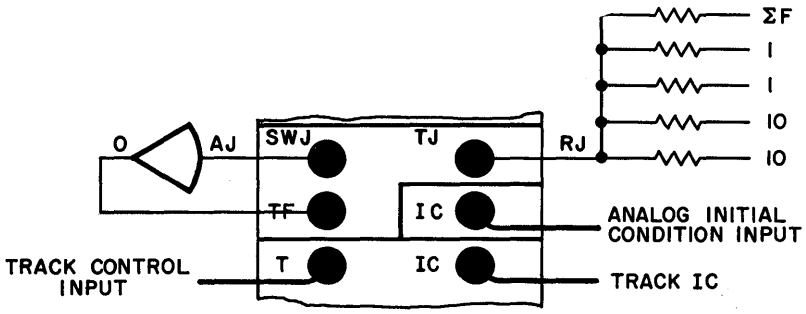


Figure 7.3. T/S Patching (Typical)

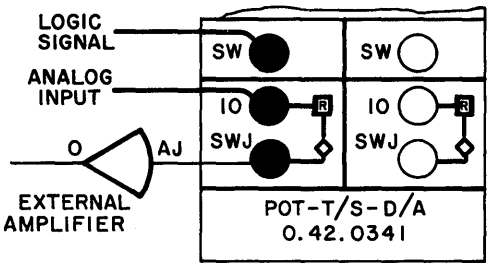


Figure 7.4. D/A Switch Patching (Typical)

The SWJ (switch junction) terminal is the output of the switch. The input of the device (the amplifier in Figure 7.3) recovering the switched analog voltage is patched to this terminal.

CHAPTER 8

THE MDFG

8.1 INTRODUCTION

The MDFG allows the generation of arbitrary continuous non-linear functions by means of straight-line segment approximation. Both ten and twenty segment operations are possible.

8.2 LOCATION AND ADDRESSING

A fully expanded 580 contains 8 ten-segment DFG's. The DFG's are arranged in pairs, and each pair may be used as a twenty-segment DFG or as two ten-segment DFG's. The DFG's are located in slideout drawers directly below the analog patch panel.

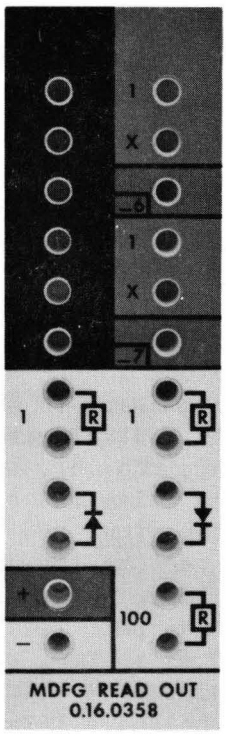
Each pair of DFG's are terminated on a single patch block in the analog patching area. To address a DFG for readout, it is necessary to depress the F pushbutton and the numerical address on the main control panel. The address for each of the MDFG pairs is F46, 47, F56, 57, F66, 67, and F76, 77. In a ten-segment operation each MDFG is addressed using one of the addresses given above. In a twenty-segment operation the <u>first</u> DFG in each pair (the one ending in -6) uses all twenty segments leaving the output amplifier of the second DFG (the one ending in -7) available as an inverter. In a standard computer configuration, the first DFG in a pair is the +DFG, capable of accepting positive inputs. The second DFG is a -DFG, capable of accepting negative inputs. Either type of DFG can produce either positive or negative outputs. Figure 8.1 shows the MDFG patching terminations on a separate tray (8.1a) and the patching terminations on a multi-purpose tray (8.1b).

8.3 APPLICATIONS

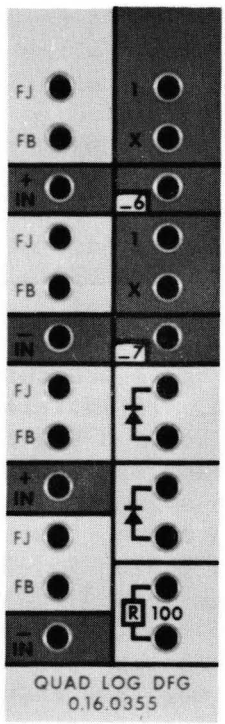
The main application for a DFG is function generation; however, the inclusion of an additional input resistor for each DFG allows some alternate applications such as the use of the unused output amplifier as an inverter, and combined summation and function generation.

8.4 SETUP PROCEDURE

Since the diode function generator approximates a given curve by a series of straight-line segments, the first step in the setup of any DFG is to determine the location of the breakpoints ("corners") in order to fit the curve as smoothly as possible. Usually the desired curve is given in graphical form, and the programmer must determine, by inspection of the graph, a table of values of x and f(x) for setup. Sometimes the function is given in tabular form - a table of values of x and f(x). Such a table of values is usually the result of experimental measurements, although it may represent the result of a series of calculations.



(a) Separate Patch Block



(b) MDFG Patching Terminations on a Typical Multipurpose Tray

Figure 8.1. MDFG Patching Terminations

If the function is given in tabular form it is tempting to simply set up the DFG to the values of x and f(x) from the table, especially if the number of data points in the table happens to coincide with the number of segments available in the DFG. The difficulty with this approach is that the distribution of the data points that define the function will probably not be the best distribution of breakpoints for straight-line approximation. For example, the original data may have been obtained for equally-spaced values of the input variable x, whereas it is generally not a good idea to use equally-spaced breakpoints for segment approximation. It is better to plot the data points, pass a smooth curve through them, and determine a good breakpoint location from this smooth graph. In any case, it is desirable to know "what the function looks like" before trying to set it up, which means it should be plotted before setup.

Hence, setup procedure in this chapter assumes from the start that the function is defined graphically. The procedure consists of determining good breakpoint locations, tabulating the values of x and f(x) at these points, and setting up the function from this table of values. The 580 DFG's have a setup panel that permits the direct setup for values of x and f(x), both the input x and output f(x) may be read directly on the DVM during setup.

An alternate procedure, illustrated in Paragraph 8.4.4, skips the table and consists of setting up the function of an X-Y plotter. The procedure is exactly the same, but the operator looks at the plotter, instead of the DVM.

Even if the function is set up from a table of discrete values read out in the DVM, it is a good idea to obtain a continuous plot of f(x) versus x to make sure that the function has been set up correctly. Such a plot should be a part of the problem documentation, along with the circuit diagram, listing of pot-settings, assignment sheets, etc. The 580 setup panel includes an integrator capable of generating a ramp input to the DFG for convenient plotting without patching changes. In fact, the DFG can be completely set up and the resulting curve plotted with the patch panel off.

8.4.1 Breakpoint Location

Although there exist analytical methods for dealing with breakpoint location, they generally require too much computation to be of practical use. With a bit of experience, a good programmer can come very close to the optimum breakpoint location simply by inspection of the curve. The following general rules may serve as a rough guide to the techniques.

1. Keep in mind the total number of breakpoints available on the DFG. Most functions of practical interest may be adequately represented with 10 segments; a few require 20 segments. Most computers (including the 580) have ten-segment DFG's capable of being "paired" to handle the occasional twenty-segment function.

2. Start out by locating the areas where the function is nearly straight; the individual segments in such areas may be relatively long. In between these areas will be the areas of rapid slope change; the breakpoints should be concentrated here.

3. As a general rule, it does not pay to locate two breakpoints closer together than about 4% of full scale (i.e., 0.04 unit, or 0.4 volt on a ten-volt computer). If two breakpoints are spaced more closely than this, they tend to "blend" into one because of the characteristics of diodes, which are not perfect switches. This effect, which "rounds off the corners" of the function, gives a smoother output and is beneficial, provided it is used to advantage in determining breakpoint locations. In case of very sharply curved functions, it may be necessary to space breakpoints as close as 2% of full scale (0.02 unit).

   As an example, consider Figure 8.2. This curve represents an arbitrary function, scaled on a unit basis, so that both input x and output f(x) vary from zero to unity. The procedure starts by noting the two areas where the function is almost straight, namely $0 \leq x \leq 0.2$ and $0.6 \leq x \leq 0.8$. There would be little point in putting any breakpoint here, so the process starts by drawing two fairly long segments to approximate the function over these intervals.

   The intervals from 0.2 to 0.6 and from 0.8 to 1.0 are the intervals where the function curves noticably. Since this is a relatively "mild" function, it may be easily approximated by ten segments. Hence, there are nine breakpoints to be determined. (Note that the number of breakpoints is one less than the number of segments. For example, a two-segment function would have one breakpoint - where the two segment joined; a three-segment function would have two breakpoints, and so on. The endpoints of the interval are fixed, and are not counted as breakpoints.)

We have nine breakpoints to divide between the two intervals of rapid slope-change. Since the first interval is longer, and the slope changes somewhat more in this interval, more breakpoints should be put in this interval.

Based on a 6-3 split, the breakpoint location in Figure 8.2 was determined. The above rules and example are intended only as a general guide.

8.4.2 DFG Setup Theory

In order to understand the DFG setup procedure, one particular aspect of the electrical theory of DFG's should be explained. Mistakes are less likely to occur if the operator has some knowledge of why various steps are taken, hence, this summary.

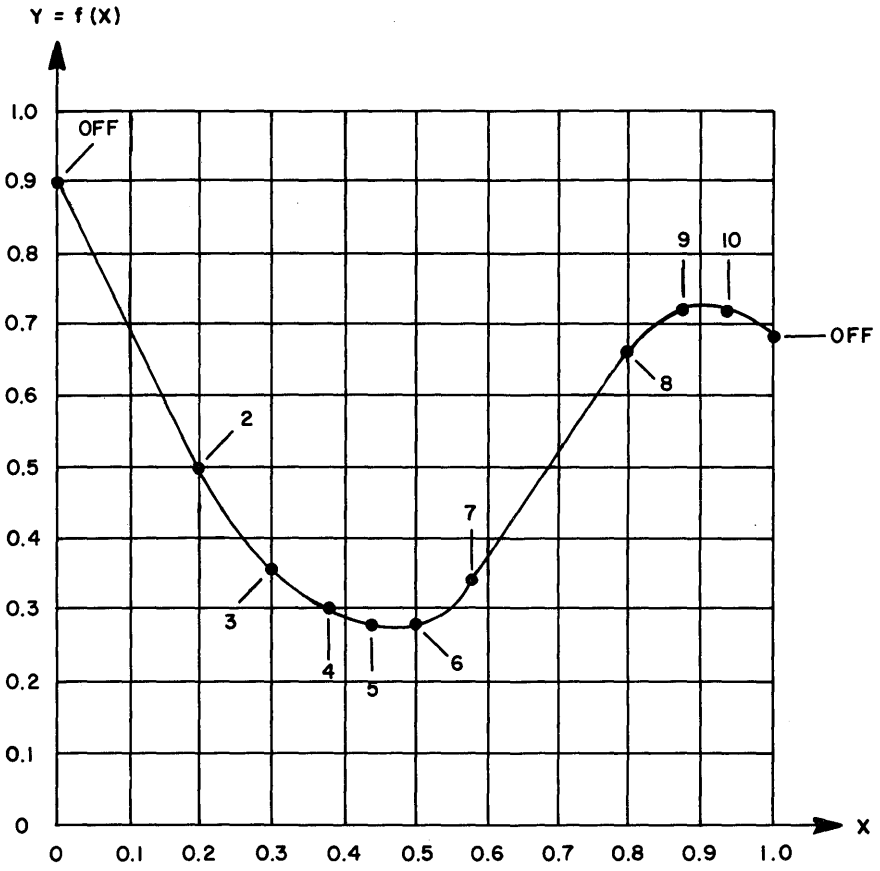


Figure 8.2. Typical Ten-Segment Function

Each breakpoint, or "corner" in a DFG curve represents a diode that is changing state; as the input voltage moves away from the origin, in either the positive or the negative direction, more and more diodes start to conduct. Each diode, when it starts to conduct, increases or decreases the slope of the curve. The change in slope for a given segment is determined by adjusting a potentiometer (the slope pot). The change in slope introduced at a given point has no affect on the value of the function at that point, but does affect the value at subsequent points. For example, Figure 8.3 shows the affect of changing the slope pot for segment 5 on a partially setup function. The incremental slope introduced at x_5 does not affect the function value at that point, but does affect the value at the next breakpoint x_6. The tangent line represents the output with the SLOPE switch OFF.

The DFG setup procedure is arranged so that the operator does not observe slopes, but rather values of x and f(x). Hence, the function value at the sixth breakpoint is adjusted by means of the slope pot at the fifth and similarly for the other breakpoints. This fact is the key to understanding the setup procedure.

In practice, the slope pot for a given segment does have an effect on the value of the function at that point, due to the fact that the diode is not a perfect switch. The "corner" at x_5 (Figure 8.3) is somewhat rounded, and a slight shift in $f(x_5)$ will occur when setting $f(x_6)$. In many cases, this shift is negligible, but in a few cases, it necessitates a later "trimming" adjustment.

8.4.3 Setting a Ten-Segment Function

Once the values of x and f(x) are tabulated, the function setup is quite straight forward. The 580 variable DFG has potentiometers for adjusting slope and breakpoint for each segment. The DFG setup panel allows direct setting from a table of values; first adjust the breakpoint x (which may be read directly on the DVM), and then set f(x).

As an example, consider the function in Table 8.1. This is the same function that was given graphically in Figure 8.2. Note that since 10 segments are to be used, the function is tabulated at 11 points, including the 2 endpoints and 9 breakpoints. A "+" DFG is assumed, and the endpoints are fixed at 0 and 1.

In setting such a function, most computer operators will find it easiest to set all breakpoints (x values) first, and then, set the function values f(x). However, it is also possible to set the first breakpoint x, then set the corresponding f(x), and continue alternating in this manner. In either case, the procedure for setting a slope or a breakpoint is the same. The procedure makes use of the DVM and signal selector, and the setup panel (Figure 8.4), which is in the right half of the lower DFG drawer. The unit is marked TIME BASE AND MDFG INPUT.

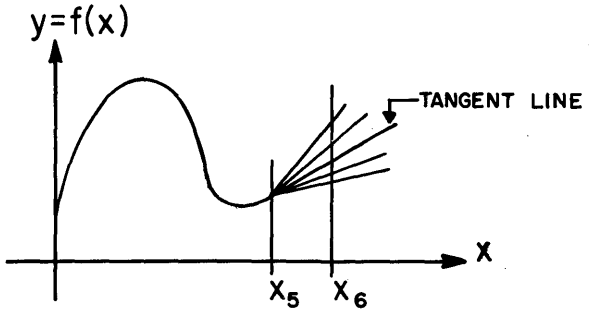


Figure 8.3. Effect of Changing Slope Pot 5 on DFG Output

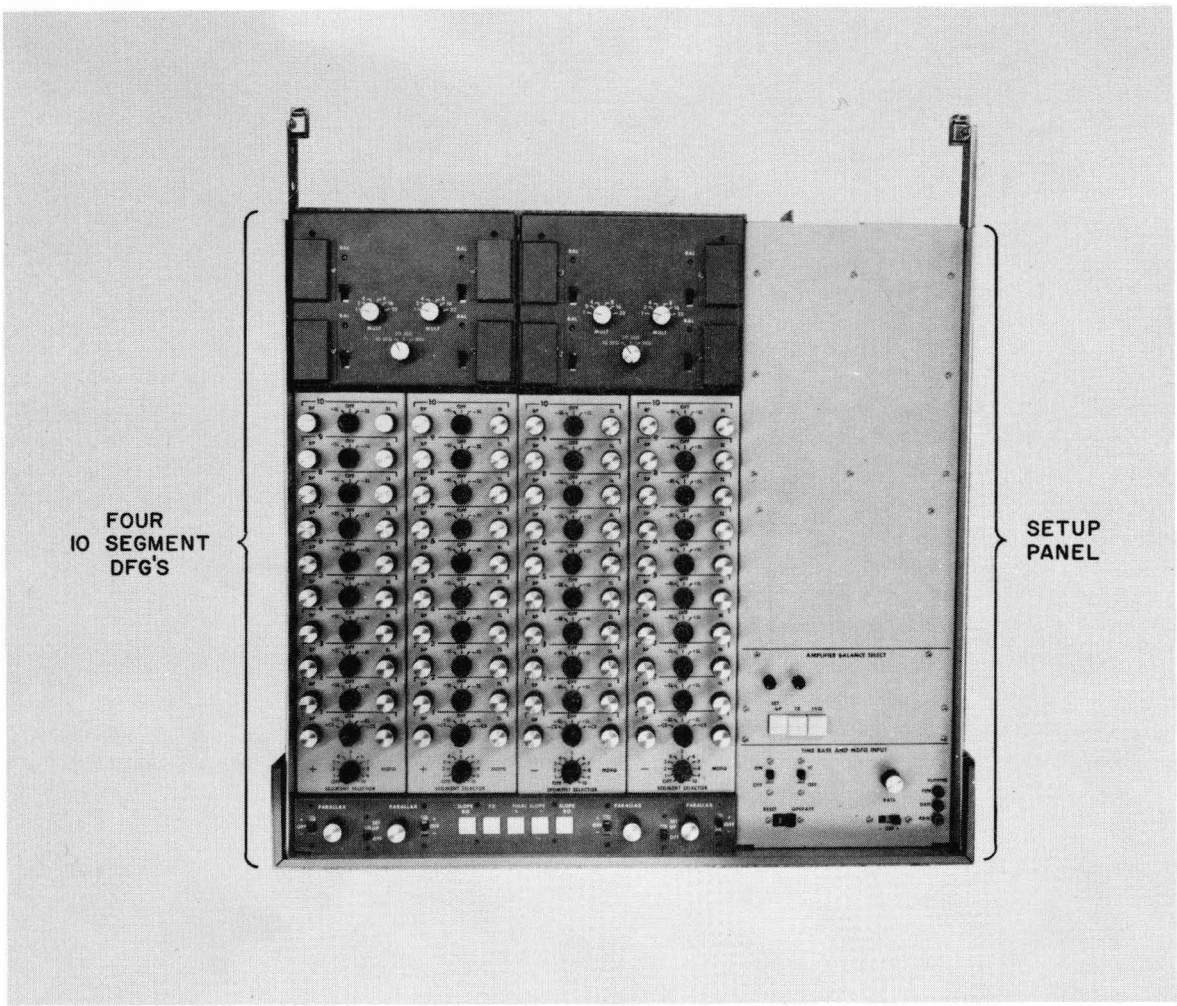


Figure 8.4. DFG Setup Panel (Lower DFG Drawer)

8.4.3.1 Computer Mode. Select the SP mode. Although the unit may be set up in any mode, the SP mode prevents overloads of other components during setup. No patch panel need be inserted; however, if there is one on the computer, it does no harm.

8.4.3.2 Setup Panel Switches. Open the drawer containing the setup panel and make sure that all switches are in the OFF position; this includes the switches marked SETUP, TB, SVO, ON/OFF, IC/OFF, and RATE. The switch marked RESET/OPERATE should be in the RESET position. Close the drawer.

8.4.3.3 Selecting the DFG. Address the DFG to be set on the signal selector. Its output should be near zero, since the computer is in the SP mode. Now open the drawer containing the DFG (Figure 8.5), and turn on the SETUP switch near the front of the drawer. There is one switch for each pair of ten-segment DFG's. When the SETUP switch for any DFG is turned on, the "F" button on the signal selector keyboard will light. This button is also lit whenever the AMP BAL switch is in the ON position. Hence, after setting up DFG's or balancing DFG amplifiers, the operator has a visual warning reminding him to turn off the setup panel before proceeding with computation.

Table 8.1

X	Y = f(x)
0.00	0.90
0.20	0.50
0.30	0.36
0.38	0.30
0.44	0.28
0.50	0.28
0.58	0.34
0.80	0.66
0.88	0.72
0.94	0.72
1.00	0.68

8.4.3.4 Checking other DFG's. The operator should now check all other DFG's to make sure that their setup switches and their SEGMENT SELECTOR switches are all in the OFF position. Only one DFG can be set up at a time, and if several are turned on at once, they will be interconnected through the setup panel, making accurate setup impossible.

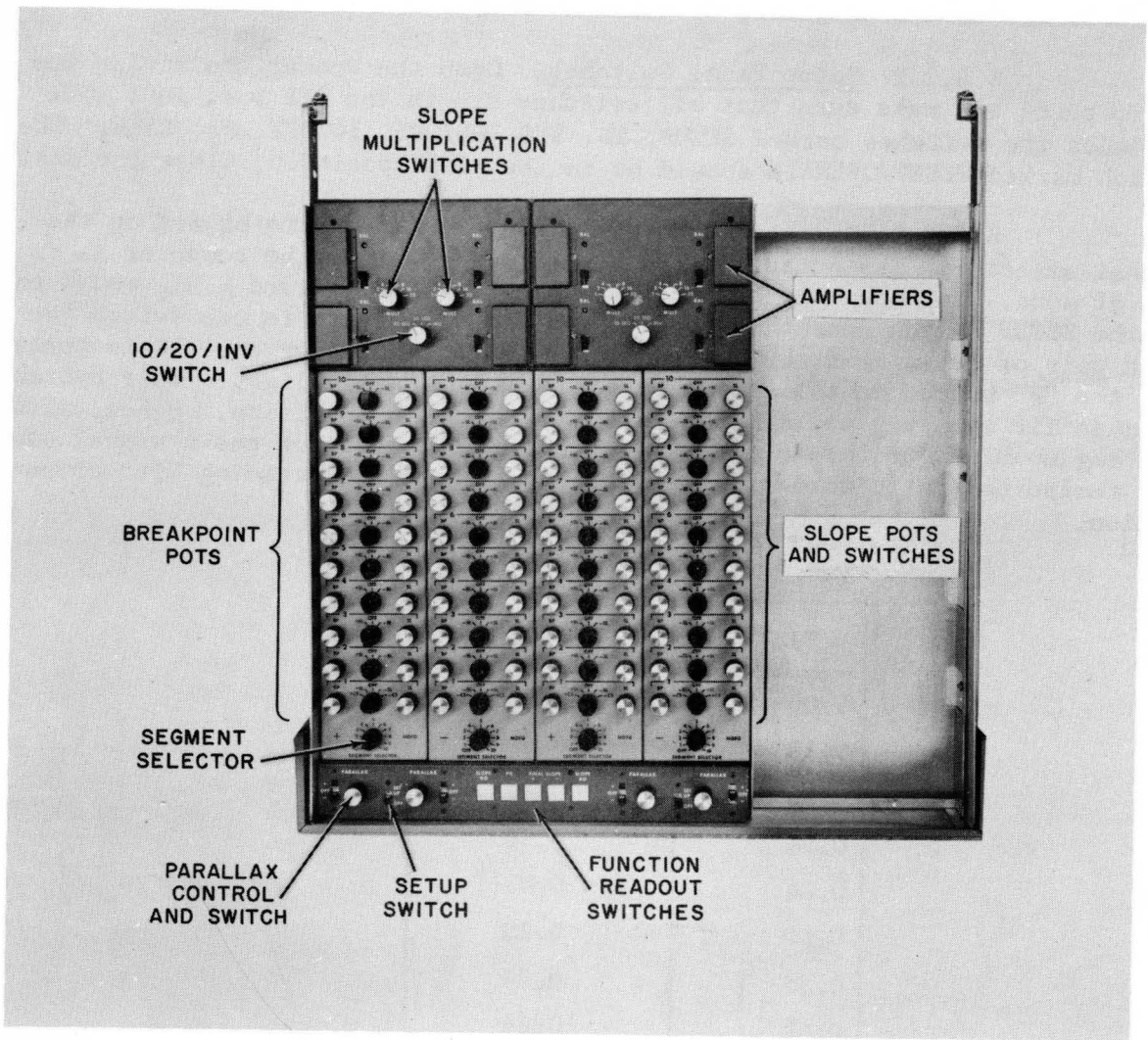


Figure 8.5. Upper DFG Drawer

8.4.3.5 Preliminary Steps. Once the DFG SETUP switch is turned on, select the proper setting on the rotary switches at the rear of the drawer. The "10 SEG/20 SEG/INV" switch should be in the "10 SEG" position, which separates the unit into two independent 10-segment DFG's. The switch marked "MULT" determines the maximum slope change per segment; rules for determining the best setting are covered in Paragraph 8.4.4. For the function such as the one in Figure 8.2, a setting of "1" is adequate.

8.4.3.6 Slope Switches. Turn all slope switches off for the DFG being set up.

8.4.3.7 Setting x and f(x). Now set up the values of x and f(x), starting from x = 0 and proceeding out from the origin toward the maximum x. The breakpoint value is read directly on the DVM; to read the corresponding function value, depress the appropriate switch. Each switch is momentary; it must be held down while setting f(x). When the switch is released, the breakpoint value x is again displayed.

Table 8.2 gives detailed information on which switch to depress at any given time. The table applies to any ten-segment function with positive inputs; the values of x and f(x) have been left blank, except for the initial and final values of x, which must be zero and one.

Table 8.2

Segment Selector	X Value	Set X on This Point	Then Hold Down this Button While Setting Y	Set Y on This Pot and Switch	Y Value
OFF	0.0000	None	PX	PARALLAX	
2		BP2	SLOPE RO	SL1*	
3		BP3	SLOPE RO	SL2	
4		BP4	SLOPE RO	SL3	
5		BP5	SLOPE RO	SL4	
6		BP6	SLOPE RO	SL5	
7		BP7	SLOPE RO	SL6	
8		BP8	SLOPE RO	SL7	
9		BP9	SLOPE RO	SL8	
10		BP10	SLOPE RO	SL9	
OFF	1.0000	None	+FINAL SLOPE	SL10	

*Use ±CS position, not ±SL position.

8.4.3.8 The Pattern of Settings. Notice that except for the first and last setting, the value of y at any point is determined by the setting on the previous slope pot. The reason for this is explained in Paragraph 8.4.2. Note also that BP pot 1 is not set; it is not used in ten-segment operation. This means that position 1 on the SEGMENT SELECTOR is skipped (see left-hand column in Table 8.2).

8.4.3.9 Slope Switch Position. The table says to "set y on a pot and switch". Each slope pot has a slope switch immediately to its left; when setting the function value, the operator first turns on the switch to the +SL or -SL position, and then adjusts the pot to obtain the correct f(x) value. If the switch is in the OFF (center) position, the pot has no affect.

To determine whether to use the + or - position, leave the switch off while depressing the readout button. This displays the function value with the segment turned off. This value will not be equal to the desired value at this point. Turning the segment on will increase or decrease this value. If the desired function value is more positive than the value with the segment off, then the switch should be turned to the +SL position. Conversely, if it is desired to decrease the function value (make it more negative), then the -SL position should be used. Some computer operators prefer not to memorize this rule, but simply turn the switch on in either direction; if the output moves in the wrong direction, the switch should be reversed. In any case, it is the direction of change that is important; the function value should change in the right direction when the switch is turned on. If the switch has no effect on the function value, the slope pot is probably set to zero; give it a few turns and repeat the ON/OFF process.

8.4.3.10 Trimming Adjustments. Having set up the entire function, from the origin outward, the operator should now go through the table again, checking the funtion values f(x). The breakpoints, once set, should remain essentially constant, but the function values may have changed slightly. This is because the value at a given breakpoint is set by changing the slope at the previously set breakpoint, causing a small shift in the previously set function value.

The amount of this shift depends upon the nature of the function and the spacing of breakpoints, but it is generally about 0.0010 to 0.0020 unit (10 to 20 millivolts), and rarely greater than 0.0050. In many cases, this shift is negligible. However, if desired, most of this effect may be removed by a series of trimming adjustments. These adjustments should be made in the same order as the original setup - starting at the origin and working outward. The trimming process goes much faster than the original setup, since the breakpoints do not have to be set again, and only small changes in function values are required. After trimming, most function values will be correct to within 0.0002 to 0.0005 unit; rarely is a second set of trimming adjustments needed.

8.4.3.11 Plotting. Once the function is set, a continuous plot of output versus input should be made, which serves as part of the problem documentation. Such a plot may be made on the 580 without repatching. The 580 DFG setup panel contains a built-in ramp integrator to provide a smooth sweep for the input. Slide out the upper DFG drawer, and make the appropriate plotter connections at the terminals on the right. Turn on the OFF/ON switch ON, and set the IC and RATE switches appropriately. To sweep from -Reference upwards, turn the RATE switch to "+". To sweep from +Reference downwards, put the RATE switch to "-"; this reverses both the rate and the IC. To start the sweep at x = 0, turn the IC switch OFF.

To make a plot, put the switch marked RESET/OPERATE to the OPERATE position. The rate of the sweep is determined by the RATE pot; a little experimenting will produce a setting that does not overdrive the plotter. When the plot is completed, put the RESET/OPERATE switch to the RESET position and turn the OFF/ON switch OFF.

8.4.4 Insufficient Slope

During the above procedure, it may happen that a particular function value cannot be obtained. If the slope pot is rotated to the end of its travel (ten times) and the function value still has not been reached, the first thing to do is to check Table 8.2 and make sure you are setting the right pot. Also, make sure the slope polarity switch is in the right position. Assuming that no such error has been made, the problem is probably one of insufficient slope.

For each segment there is an upper limit to the amount of slope change that it can introduce; this is the amount produced with the slope pot fully clockwise. On the 580, a maximum slope change of 1.0 may be obtained with one segment, assuming the slope multiplication switch is in the "1" position (see Paragraph 8.4.3.5). Other positions of this switch allow for slope changes as great as 32.

The slope multiplication switch works by changing the effective feedback resistance on the output amplifier, thus providing greater gain. For every steep or sharply curving functions, a position other than "1" may be necessary. There is also a limitation on the initial slope f'(0). This limitation is 3.0 if the MULT switch is in the "1" position, and it goes up in proportion to the setting on this switch, so that the maximum value is 96 (3 x 32).

The effective resolution of the slope pots decreases with higher gain; at high settings a small motion of the pot produces a large change in the output, making accurate setup difficult. Also, electrical characteristics such as bandwidth are degraded at high gain setting. For this reason, it is not desirable to use any more gain than necessary in generating a particular function.

A conservative procedure is to set the switch initially at "1", and proceed to set the function until insufficient slope is encountered, then try a setting of 2 and try again. However, this procedure may lead to a number of false starts, and some methods of estimating the maximum slope requirement prior to setup is desirable.

Such an estimate may be easily obtained from a graph of the function once the breakpoint locations have been determined. The procedure is as follows:

1. Locate visually the points where the slope is steepest (in either the positive or negative direction).

2. Estimate the slope of the curve at these points by drawing triangles or counting squares on the graph.

3. Form the difference between the maximum positive slope and the maximum negative slope. This is the total slope change required between the two points where maximum slope occurs. Note that in subtracting two slopes of opposite sign, the magnitudes are added. If there are several points of maximum positive and negative slopes, choose a pair of such points near each other where the slope difference is large.

4. Divide the total slope change between these two points by the number of breakpoints in this interval. This gives the average slope change per breakpoint in the "worst case" region. The slope actually required may be somewhat greater, since not all segments will have the same slope change. However, this estimate is a good one to use as a starting point.

8.4.5 Example of Slope Amplification

As an example of a function requiring slope amplification, see Figure 8.6. This curve was initially drawn free-hand on a sheet of graph paper and inserted in the X-Y plotter. Breakpoints and function values were set directly by observing the plotter, not the DVM. Hence there was no need to tabulate the function. Thus the curve offers a good example of graphical setup procedure as well as of slope amplification.

Breakpoint location was determined by following the rules in Paragraph 8.4.1. There are 4 relatively straight portions and 3 relatively "curvy" portions. Since the function appears to curve about the same amount in each curve region, the nine available breakpoints were equally distributed - three per region. Note that the breakpoints have been marked according to the SEGMENT SELECTOR position that will be used in setting them. The pattern goes: OFF, 2, 3, 4, ..., 9, 10, OFF. As mentioned previously, position 1 is skipped.

The greatest positive slope occurs at the left side; the greatest negative slope occurs just past the first peak; these facts are obvious by inspection of the graph.

Graphical determination of the slopes indicates that the positive slope is about 5.5, and the negative slope about -6. The difference in slopes is 11.5. Since there are three breakpoints between these two points, the average slope change per segment is 11.5/3 or 3.9. It is somewhat questionable whether a slope multiplier of 4 will be adequate, since some of these breakpoints will require greater slope change than others. However, it may

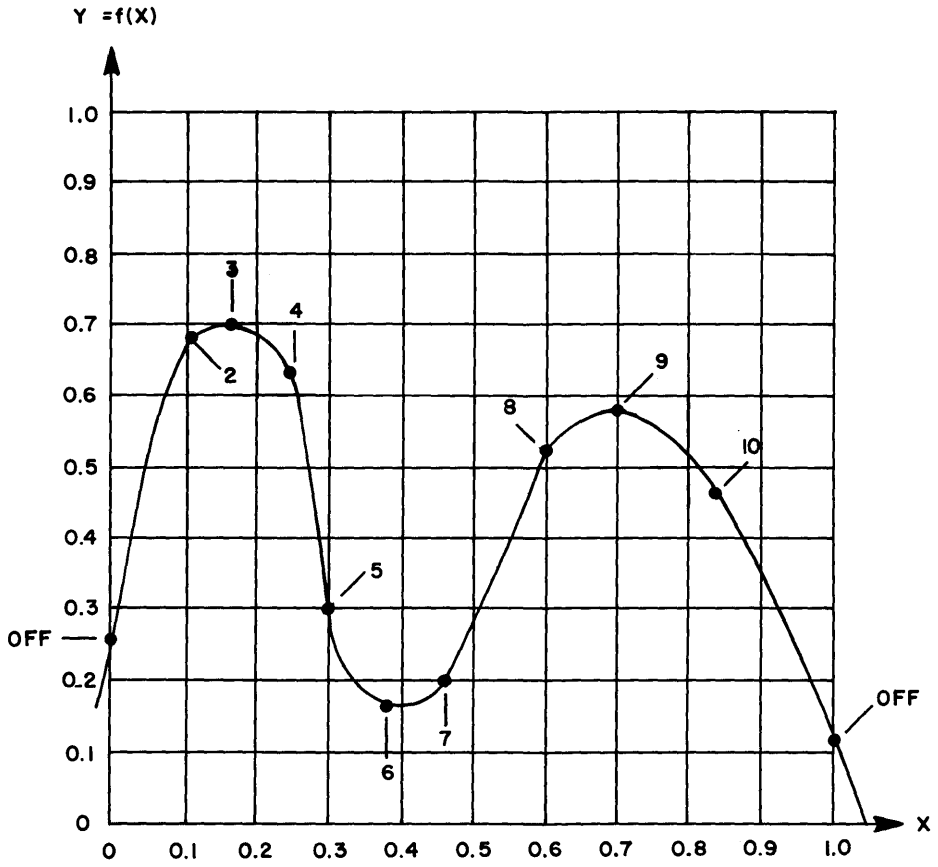


Figure 8.6 Typical Function Requiring Slope Amplification

be possible to get by with 4, especially since the slope rating is somewhat conservatively specified on most DFG's. Hence a setting of 4 was tried.

As might be expected, there was difficulty in setting the value at point 5. The smallest value obtainable was about a quarter-inch above the curve. (About 0.025 unit.) The slope multiplier switch was set to the next higher value (8) and the setup was repeated. Note that when the slope amplification is changed, it is necessary to go back to the beginning and reset every previously set function value, starting with the PARALLAX setting, since doubling the gain will double the entire function up to that point. However, the breakpoint settings do not have to be reset; they are unaffected by the slope amplification switch.

With a slope setting of 8, the setup proceeded smoothly. No difficulty was observed in setting function values. A continuous plot made after the setup was completed indicated that the plotted function was virtually indistinguishable from the original hand-drawn curve over most of its length, and that the maximum deviation was about 0.3%. No trimming adjustments were necessary.

8.4.6 Eleven-Segment Functions

At this point, the reader may be wondering what "Breakpoint 1" is for. The setup procedure calls for ignoring this breakpoint pot and its corresponding position on the segment selector. This breakpoint is usable for twenty-segment functions (see Paragraph 8.4.6) and, under certain conditions, for eleven-segment functions.

Whenever the function to be generated is initially horizontal (that is, $f'(0) = 0$), then the function may be generated with eleven segments instead of ten. The additional segment is horizontal. An example of such a curve is given in Figure 8.7, and a corresponding table of values is given in Table 8.3.

Note that since the first segment is horizontal, the value at the first breakpoint is the value at the origin. In fact, since the value at a given breakpoint is set by adjusting the slope at the previous breakpoint, there is no control for adjusting the function value at breakpoint number one.

Table 8.3

Segment Selector	x	f(x)	Segment Selector	x	f(x)
OFF	0.00	0.33	6	0.46	0.84
1	0.06	0.33	7	0.52	0.84
2	0.12	0.36	8	0.60	0.82
3	0.18	0.42	9	0.70	0.76
4	0.34	0.72	10	0.84	0.60
5	0.40	0.80	OFF	1.00	0.32

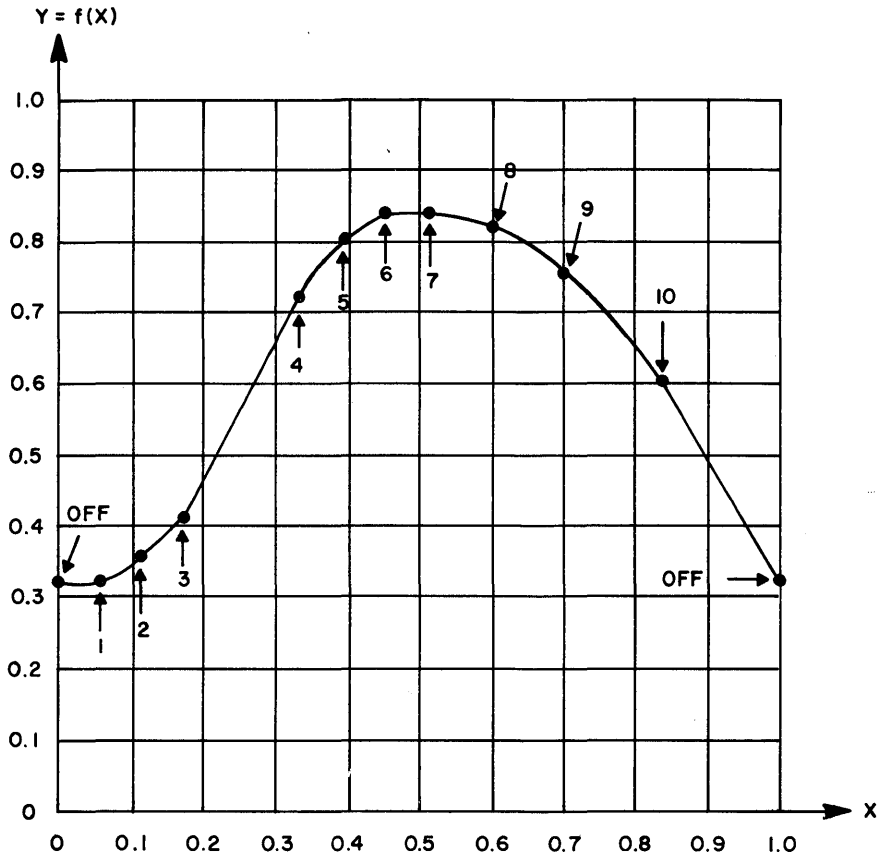


Figure 8.7 Initially Horizontal Eleven-Segment Function

The setup procedure is similar as for any other function, with the two following exceptions:

1. Position 1 on the SEGMENT SELECTOR is not skipped. It is used for setting breakpoint 1. Once the breakpoint has been set, the function value can be read out by depressing the SLOPE RO button, but there is no way to adjust this value without disturbing the rest of the function. The value should be equal to the value of x = 0 (previously set by the PARALLAX control), plus or minus a small increment due to interaction with the next setting.

2. The slope switch for BP1 is put in the ±SL position, rather than the ±CS position.

The reason for this feature is that the slope pot for segment 1 is actually a CENTER SLOPE pot; it is this pot that sets the slope at x = 0. When the pot is used in this manner, there is no diode and hence no breakpoint associated with it. Electrically, the pot simply provides linear gain from the input to the output. If f'(0) = 0, then there is no need for a pot to set the initial slope. Hence, by adding one more pot, (breakpoint pot 1) an additional segment becomes available. The CENTER SLOPE pot can now be used as a slope pot for the extra segment. The setting of this pot determines the value of the function at the next breakpoint.

8.4.7 Negative Inputs

The above procedure applies to the +DFG; this type of DFG accepts positive inputs only. The output values, however, may be of either polarity. For generating functions with negative inputs, the -DFG is used. Most computers are equipped with an equal number of either type; however, they may be installed in any proportions.

The setup procedure for the -DFG is essentially the same as for the + type; starting from zero, work away from the origin toward the final value of -1.0000. The value at this last endpoint is ready by depressing the -FINAL SLOPE button, rather than +FINAL SLOPE. The rule given in Paragraph 8.4.3.9 for determining the polarity of the slope switch should be reversed.

8.4.8 Twenty-Segment Functions

Provision is made for operating a pair of ten-segment DFG's as a single twenty-segment unit. The unused output amplifier of the second DFG is then available for independent use as an inverter. Twenty-segment operation can serve either of two purposes: increased accuracy through the use of more segments, or the generation of functions from an input that ranges over both polarities. For the former purpose, two DFG's of the same type (both "+" or both "-") are used together; for the latter, one "+" and one "-" are used together. In most common arrangement, the first DFG in a pair is the "+" type and the second is the "-" type. However, either type may be put in any position, so that it is possible to obtain (for example) twenty breakpoints in the interval $0 \leq x \leq 1$.

The PARALLAX controls on two connected DFG's perform the same function, each of them is simply a bias adding a constant (positive or negative) voltage to the output. In twenty-segment operation, only one of these controls is needed, the other should be turned off.

Similarly, the controls marked CENTER SLOPE (i.e., the $\pm$CS position on slope switch 1) determine the slope at x = 0. This slope is determined by a pot and input resistor; like the PARALLAX controls, one of these is redundant in twenty-segment operation. However, unlike the PARALLAX control, the CENTER SLOPE control may be used as an ordinary segment when not needed for central slope. This capability is described in Paragraph 8.4.6,"Eleven-Segment Functions".

In the case of a DFG with positive and negative inputs, some thought should be given to the problem of setting the values in the interval around zero. What is desired is a straight-forward method of setting the values of x and f(x) at all breakpoints. If there is no breakpoint at x = 0, then the function values of the two breakpoints nearest zero (one positive, one negative) cannot be set directly and independently. Over the interval containing zero, no diodes are conducting, and the output is simply a linear function of the input. The PARALLAX pot allows setting the y-intercept of this function, i.e., the value when x = 0. The CENTRAL SLOPE pot, which is Slope Pot 1 on either the + or the -DFG, allows setting the slope of this line. Since these two parameters completely characterize the line, they can be set to pass the line through any two points; i.e., they can be set to give the correct values at the two breakpoints (one positive, one negative).

However, the relation between these two pot-settings has a relatively large interaction; each pot-setting affects both values. This interaction does not exist anywhere except at this one interval. Setting any other function value does not disturb previous settings, except for the small secondary effect of the "diode curvature" which is easily taken care of by "trimming" if necessary.

To set the values at the two breakpoints containing zero, first calculate and tabulate f(0), even though this is not a breakpoint. The value of f(0) should be calculated by linear interpolation between the values at the breakpoints on either side of zero, since the curve is straight over this interval. Of course, the interpolation can be done graphically simply by drawing a line connecting these points. Once the values have been set at x = 0 and at one of the two breakpoints, they should automatically be corrected for the other breakpoint.

Since there is no need for two CENTRAL SLOPE pots in twenty-segment operation, one of the two pots can be used for a regular breakpoint. This allows 9 breakpoints to be used on one side of zero, and 10 on the other. The operator may put this tenth breakpoint on either side, depending upon where it is needed most.

As an example, consider the function in Figure 8.8. This function has three regions where it curves rather sharply, separated by regions where it is relatively straight. One of the curved regions lies in the negative half of the graph and another in the positive half. Since the third curved region lies mostly on the positive side, it appears advisable to put the "extra" breakpoint on the +DFG. Hence, BP1 on the -DFG is used for the CENTRAL SLOPE, and BP1 on the +DFG is used as a regular breakpoint. The resulting breakpoint tabulation is given in Table 8.4. Note that the SEGMENT SELECTOR positions for each segment are given on the figure, as well as in the table.

In setting the function, first turn all slope switches off for both DFG's and put the rotary switch at the rear of the drawer to the "20 SEG" position. Address the appropriate output amplifier on the SIGNAL SELECTOR. Since both DFG's are connected to the first amplifier, it is this amplifier (the one whose address ends in -6) that should be addressed. The other output amplifier (the one ending in -7) disconnected from the DFG, and is available for use as an inverter. Its slope multiplier switch (the one on the right) should be set to 1. A quick calculation based on the techniques of Paragraph 8.4.4 indicates that a slope multiplier of unity is probably adequate for this function; hence, the slope multiplier switch on the left should also be set to 1. Set all breakpoints (positive and negative), but do not set function values at this time.

NOTE

Only one SEGMENT SELECTOR should be on at a time. When setting either breakpoints or function values on one of the DFG's, ensure that the SEGMENT SELECTOR on the other one is in the "OFF" position.

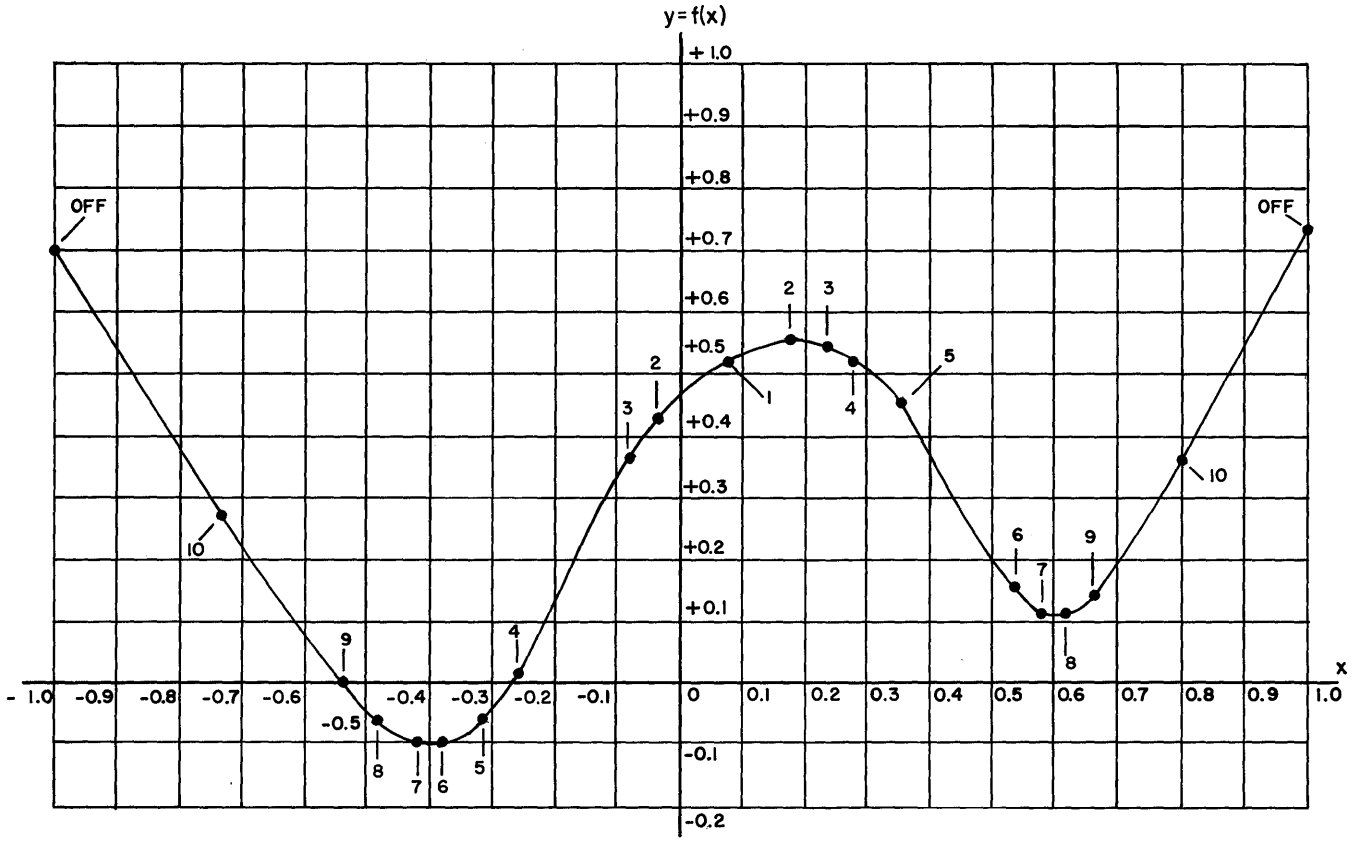


Figure 8.8. A Typical Twenty-Segment Function

Table 8.4

x	f(x)	SEGMENT SELECTOR Position	
-1.00	+0.70	OFF	
-0.74	+0.28	10	
-0.54	0.00	9	
-0.48	-0.06	8	
-0.42	-0.10	7	-DFG
-0.38	-0.10	6	
-0.32	-0.06	5	
-0.26	+0.02	4	
-0.08	+0.38	3	
-0.04	+0.44	2	
0.00	+0.47	OFF	(Both SEGMENT SELECTORS Off)
+0.08	+0.53	1	
+0.18	+0.56	2	
+0.24	+0.55	3	
+0.28	+0.52	4	
+0.36	+0.46	5	+DFG
+0.54	+0.16	6	
+0.58	+0.12	7	
+0.62	+0.12	8	
+0.66	+0.14	9	
+0.80	+0.36	10	
+1.00	+0.74	OFF	

Set both SEGMENT SELECTOR switches to the "OFF" position and set f(0). Then put the +DFG SEGMENT SELECTOR in position 1, and set the value at the first positive breakpoint. Turn this SEGMENT SELECTOR off and put the other SEGMENT SELECTOR in position 2 to read the value at the first negative breakpoint. (Note the switch positions, as tabulated in Table 8.4.) When the SLOPE RO button is depressed, the function value at this breakpoint should be correct.

If it is not, then the three tabulated values are not collinear; if this happens, determine the correct f(0). Once proper values have been obtained at these breakpoints, set the function values on the -DFG, working outward from the origin, and then do the same for the +DFG. Remember to turn off the SEGMENT SELECTOR for one DFG when setting either breakpoints or function values on the other.

Trimming adjustments may or may not be necessary, depending upon the nature of the function and the accuracy required. As with a ten-segment unit, trimming should be done from the origin outward. Remember there is one function value that cannot be trimmed: the PX and CS pots allow the function to be set properly at x = 0 and at one of the two breakpoints nearest the origin; the value at the other breakpoint will be close to the desired value, but it cannot be changed without disturbing previous settings.

If it is necessary to trim the function values at the two breakpoints near the origin accurately, an iterative procedure may be used. Trim the function value nearest to zero by means of the PARALLAX pot, trim the other value by means of the CENTRAL SLOPE pot, and alternate until both function values are correct. The value of f(0) is, of course, no longer equal to the tabulated value, but the values at the two breakpoints are correct. The interaction between settings means that after setup, the value of f(0) may no longer be exactly collinear with the adjacent values. Now proceed to trim the other function values, working from the origin outward, as before.

After the last function value is set, be sure both SEGMENT SELECTOR switches are off, and plot the function using the time-base integrator in the MDFG setup drawer. A sweep from -reference to +reference should be used to cover the entire range of the function.

If one of the breakpoints occurs at x = 0, then the procedure is somewhat simplified. The zero breakpoint can be set on BP1 for either the + or the -DFG; the BP1 pot on the other DFG is not used, since this segment is used for CENTER SLOPE. The value f(0) is set by a PARALLAX pot as usual; the value at "breakpoint 1" on the DFG being used to give the zero breakpoint should agree with the PARALLAX setting.

CHAPTER 9

COMPARATORS AND FUNCTION RELAYS

9.1 INTRODUCTION

This chapter provides operating information for the comparator and function relay portions of the Model 0.42.0340 Potentiometer-Comparator-Function Relay Tray (Figure 9.1) used in the 580 Computer. Operating information for the potentiometer portion of the tray is included in Chapter 3 of this manual.

9.2 THE COMPARATOR

The comparator used in the 580 is a completely self-contained device that algebraically compares two analog input voltages and provides a logic signal and its complement as an output. If the algebraic sum of the input voltages is positive, the comparator output is high. The comparator output is low when the algebraic sum of the input voltages is negative. In each case the output complement is the inverse of the output.

The L (latch) patch terminal is used to inhibit the output logic circuits and hold the comparator output at a particular state regardless of the inputs. For example, if the algebraic sum of the voltages being compared is positive, the output of the comparator is high. A high patched to the L terminal holds the output high even if the algebraic sum of the input voltages goes negative. The L terminal can be used to inhibit the comparator output at a particular point in a sequence of events, or after a predetermined number of clock periods utilizing the digital counters. The L terminal can also be patched to the comparator output (or its complement) terminal to inhibit the comparator output when the algebraic sum of the input voltages change polarity. Figure 9.2 is a typical comparator patching configuration.

9.3 FUNCTION RELAYS

The function relays are included on the Model 0.42.0340 POT-COMP-F/R tray (Figure 9.1). Each tray contains one 2 Form C relay with the contacts and wipers of the relay terminated on the patch panel (Figure 9.1). One relay is terminated in each patch panel field, i.e., function relay 0 is located in FIELD 0, function relay 1 is located in FIELD 1, etc.

The patch panel is graphically worked with the relay shown in the set (S) position. Utilizing this diagram makes patching the various functions to be switched a relatively easy task.

The FUNCTION RELAY pushbuttons, located on the auxiliary control panel, are used to switch the relays. Depressing a numbered pushbutton sets the relay in the field that the pushbutton number coincides with. The adjacent blank pushbutton causes the relay to be reset. The numbered pushbutton contains a lamp circuit which, when lit, indicates the state of the relay.

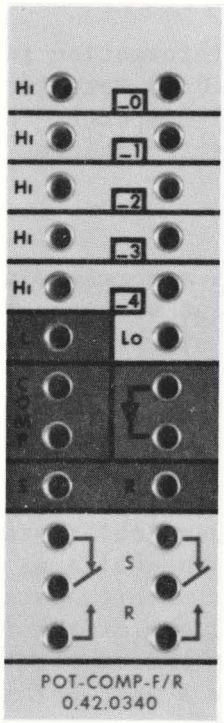


Figure 9.1. Comparator and Function Relay Patching Area

Patch terminals S (set) and R (reset) can also be used to control the relays. A high at either of these inputs forces the function relay to the state patched. The relay is retained in the selected state until a high is patched to the alternate state, at which time it will change states.

CAUTION

Damage to the relay will result if reference voltage is grounded through the relay contacts.

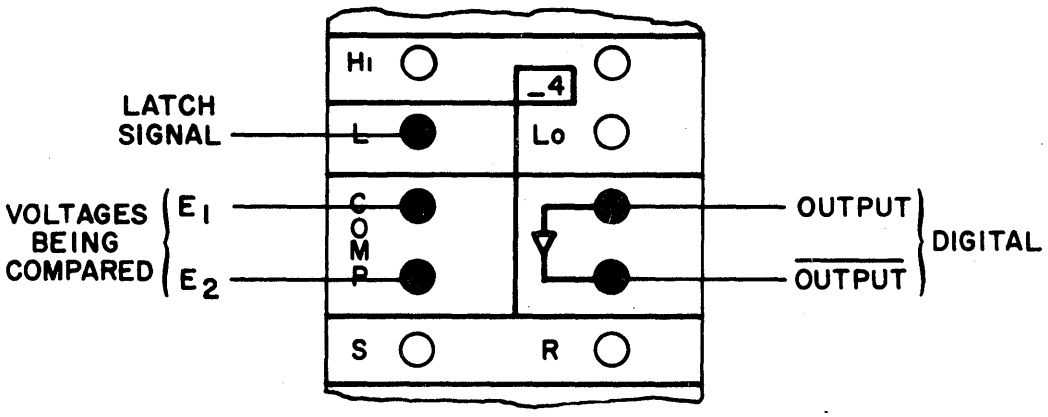


Figure 9.2. Typical Comparator Patching

CHAPTER 10

CONTROL TRAY

10.1 INTRODUCTION

The 0.12.1607 Control Tray (Figure 10.1) provides patch terminals for various inputs, outputs and control functions. Since the functions of the patch terminals (or groups of patch terminals) are not related, each is described separately.

10.2 DVM PATCH TERMINAL

The DVM patch terminal provides an input to the DVM when the PP pushbutton on the ADDRESS switch is depressed. This provision permits the DVM to readout any voltage not capable of being addressed.

10.3 VM PATCH TERMINAL

The VM patch terminal is used primarily when the computer is not equipped with a DVM. This patch terminal provides an input to the VM when the VM FUNCTION switch is placed in the PP position. The RANGE switch selects the proper meter range for the input voltage.

10.4 IC AND OP PATCH TERMINALS

The IC and OP patch terminals provide inputs to their respective bus bars through a series of gates and inverters. To utilize these inputs, it is necessary to depress the analog mode PP pushbutton on the main control panel. Once this is done, control of the IC and OP bus bars is assumed by these inputs. A high in either patch terminal forces the respective bus bars high. A low input forces the bus bars low. Table 10.1 defines the computer modes resulting from the possible IC and OP inputs.

Table 10.1. Computer Modes

Input Terminals	Mode OP	Mode IC	Mode HD
OP	1	0 1	0
IC	0	1 1	0

Note from the table that the IC signal overrides the OP signal, i.e., if the OP patch terminal is held high, the integrators may be switched between the OP and IC modes by switching the IC signal.

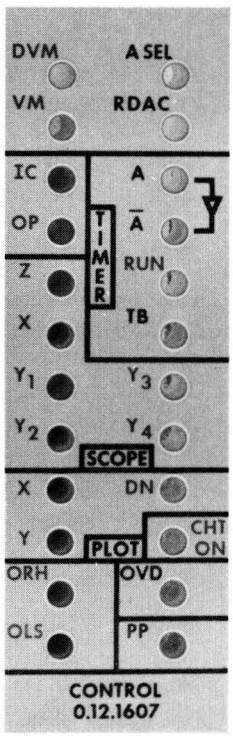


Figure 11.1. Control Tray Patch Panel

10.5 SCOPE PATCH TERMINALS

The six patch terminals enclosed within a solid black line and labeled SCOPE are used as inputs to the Rep-Op Display Scope available with the 580 Computer. The Z patch terminal is the blanking input to the Rep-Op scope. The sweep voltage is patched to the X terminal. Patch terminals Y_1, Y_2, Y_3, and Y_4 connect the patched signals to the respective Y channels. Operating instructions for the Rep-Op scope are provided in the manual for the 34.034 and 34.035 Repetitive Operation Display Scope (EAI Publication Number 00 800.2024-1).

10.6 PLOTTER PATCH TERMINALS

The three patch terminals enclosed within a solid black line and labeled PLOT are the inputs to the EAI 1110 Plotting Board available with the 580 Computers. The X and Y patch terminals are connected to the X and Y inputs on the plotter. The patch terminal labeled DN is used for remote control of the pen lift circuit. A high patched to this terminal causes the pen to be lowered to the plotting surface. A low causes the pen to return to the up position.

10.7 CHT ON PATCH TERMINAL

The CHT (chart) ON patch terminal is used for remote control of the strip chart recorder available for use with the 580 Computer. A high patched at this terminal turns on the recorder. A low returns the recorder to the OFF state.

10.8 RDAC PATCH TERMINAL

The RDAC terminal is connected to the output of the RDAC. This terminal can be utilized to monitor the RDAC output. Using this terminal, the RDAC can also be used as a digitally set attenuator. In a hybird configuration this terminal becomes the high speed DAC output.

10.9 A SEL PATCH TERMINAL

The A SEL patch terminal is used as an output terminal for any addressed amplifier. This terminal is used primarily to externally monitor the output of any addressable amplifier.

10.10 TIMER PATCH TERMINALS

The four patch terminals enclosed by a black line and labeled TIMER are used as timer output and control functions. The A and $\overline{A}$ terminals provide the IC (A) and OP ($\overline{A}$) functions at the patch panel for problem usage. The RUN patch terminal is a control input used to start and stop timer operation and overrides the PP mode pushbutton. When this terminal is high the timer starts operation. When it is low the timer operation ceases. (This terminal performs the same timer function as the PP pushbutton on the main control panel. If the computer is in the PP mode it is not necessary to patch this terminal.) The TB patch terminal provides the output of the time base generator.

10.11 OVD, ORH, AND OLS PATCH TERMINALS

The OVD (overload) patch terminal, connected to the output of the overload system, provides a logic output voltage indicating the state of the overload circuit. A high at OVD terminal indicates that an overload has occurred, while a low indicates no overload.

The ORH (override hold) patch terminal is an input used to force the integrators into the hold mode should an overload occur in the system. This feature requires patching the OVD terminal to the ORH terminal and is usually used to stop the program solution at the instant an overload occurs.

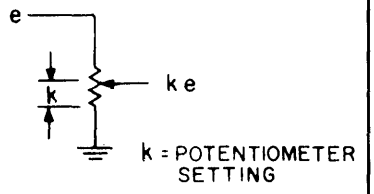
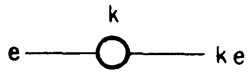
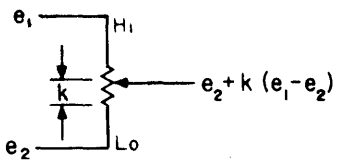
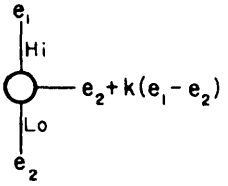
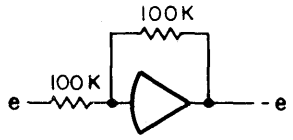
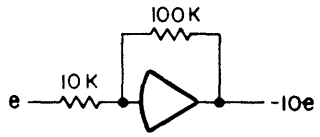
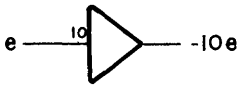
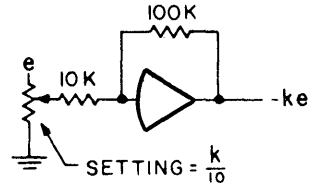
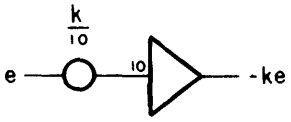
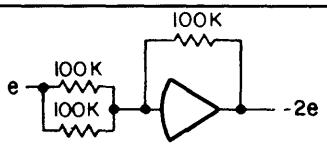
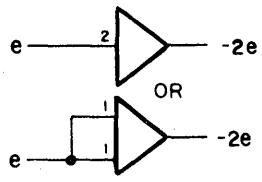
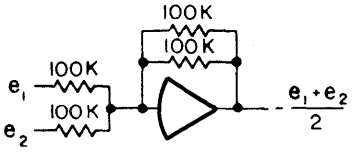
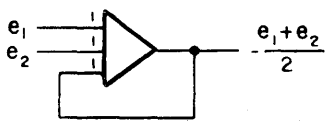
The OLS (overload stores) patch terminal is used to detect and locate short term, intermittent overload conditions. During normal operations, the overload indicators light as overloads occur and automatically clear themselves when the overload is cleared. Patching the OLS terminal to the OVD terminal forces the overload indicator to remain lit even after the overload condition is removed. To reset, the patch cord from OVD to OHS must momentarily be removed.

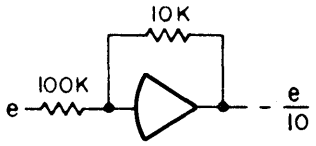
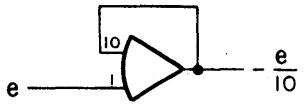
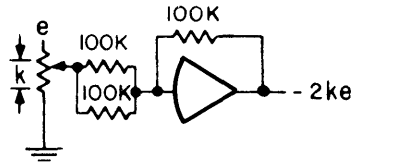
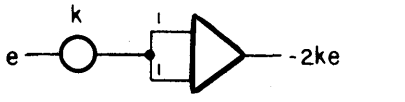
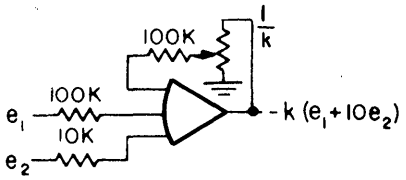
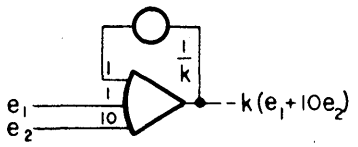
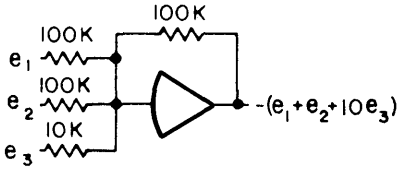
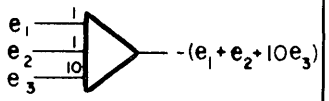
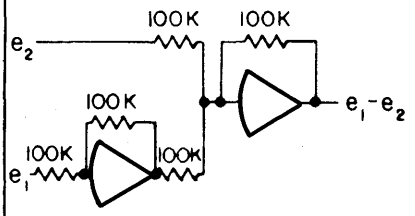
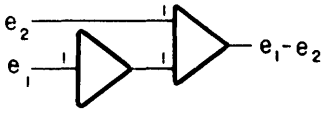
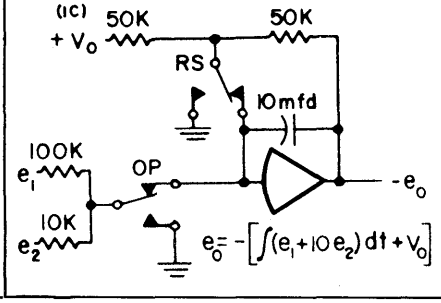
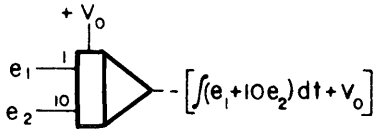
10.12 PP PATCH TERMINAL

The PP patch terminal provides a buffered output of the analog PP mode. When the analog PP pushbutton is depressed (computer in PP mode) the PP patch terminal goes high. The output from this terminal can be used for control functions as required by particular problems.

APPENDIX 1

SIMPLE CIRCUITS USING AMPLIFIERS AND POTENTIOMETERS

CIRCUIT DESCRIPTION	CIRCUIT	PROGRAMMING SYMBOL
1. GROUNDED POTENTIOMETER		
2. UNGROUNDED POTENTIOMETER		
3. INVERTER		
4. MULTIPLICATION BY -10		
5. MULTIPLICATION BY -k for $1 \leq k \leq 10$ (for $k < 1$ use circuit 1 feeding circuit 3)		
6. MULTIPLICATION BY 2		
7. MULTIPLICATION BY $\frac{1}{2}$		

CIRCUIT DESCRIPTION	CIRCUIT	PROGRAMMING
8. MULTIPLICATION BY $\frac{1}{10}$		
9. MULTIPLICATION BY AN ARBITRARY VALUE		 $0<k<1.0$
		 $1<k$
10. ADDITION		
11. SUBTRACTION		
12. INTEGRATION		

APPENDIX 2

UNIT SCALING

The process of scaling an analog computer circuit is simplified if the reference voltage of the computer is used as a unit for measuring amplifier outputs. On a ten-volt computer, such as the 580, this means that one unit is defined to be equal to ten volts; all signals, when measured in units, will be ≤ 1.0000 in magnitude.

There are a number of advantages to such an approach. One of the most obvious (but not the most important) is the fact that the DVM reads in units (when reference voltage is measured on the DVM, the result is +1.0000). This location of the decimal point is determined by the fact that the DVM is used for pot-setting as well as amplifier readout, and pot-setting must be ≤ 1.0000 in magnitude. If reference voltage is used as the unit of measurement, then amplifier outputs are also ≤ 1.0000 in magnitude. Hence the decimal point is correctly located in all cases.

The relation between a problem variable and the corresponding computer variable becomes somewhat simpler in terms of unit scaling. For example, if a problem variable P has a maximum value of 50 lbs, then the corresponding computer variable is simply [P/50], which has a maximum value of one. In unit scaling, every computer variable is simply *the ratio of the corresponding problem variable to its maximum value.*

If the scaling is done in volts, then the computer variable is ten times the ratio of the problem variable to its maximum value. Thus, if $P \leq 50$ lbs, then the computer variable would be [P/5]. On a hundred-volt computer, the computer variable would be [2P]. This points out another advantage of the "unit scaling" technique - it is machine-independent: the scaled variable would be [P/50] on *either* machine.

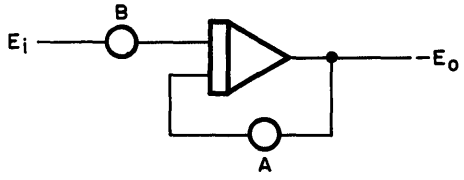
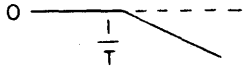
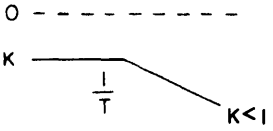
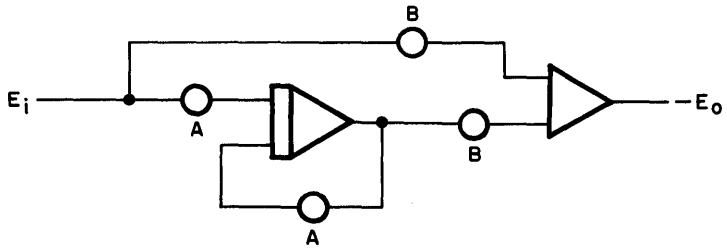
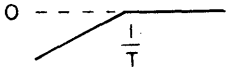
Probably the greatest advantage of unit scaling is the way it simplifies the scaling of non-linear circuits. For example, the product of two variables that are ≤ 1 in magnitude will also be ≤ 1 in magnitude. If a multiplier has scale inputs X and Y ($-1 \leq X \leq 1$, $-1 \leq Y \leq 1$) then the output will simply be the product XY ($-1 \leq XY \leq 1$). If scaled in volts, the output would be XY/10 or XY/100, depending on the reference voltage of the machine. Similarly, expressions for square, square root, log exponential, and trigonometric functions are generally simpler when expressed in terms of units.

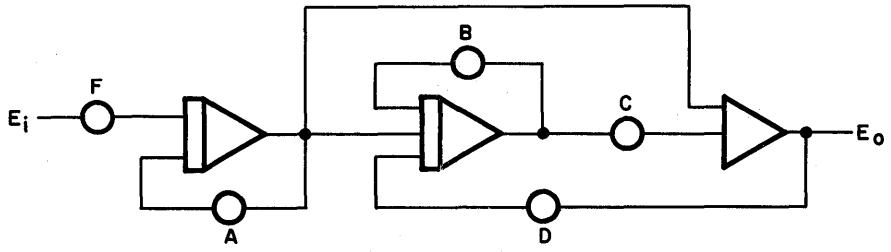
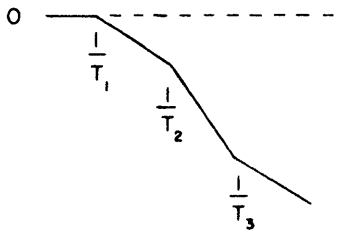
A more complete description of the unit scaling technique is given in Chapter 3 of the Handbook of Analog Computation, available from EAI.

APPENDIX 3

TRANSFER FUNCTION SIMULATION

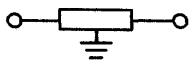
(1) The following table contains examples of amplifier circuits for simulating transfer functions . A more complete listing may be found in Jackson, A.S., "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960.

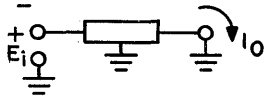
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
1		$\frac{1}{1+Tp}$	$T = \frac{1}{A}$	$A = B = \frac{1}{T}$
2		$\frac{K}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$
				
3		$\frac{Tp}{1+Tp}$	$T = \frac{1}{A}$	$A = \frac{1}{T}$ $B = 1$
4		$\frac{Kp}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$

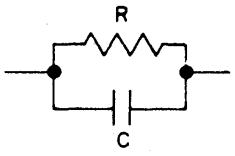
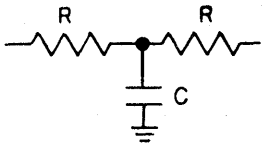
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
5.		$\frac{1+T_3P}{(1+T_1P)\,(1+T_2P)}$	$T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$	$A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ C = Arbitrary >0 $D = \frac{1}{C}\left(\frac{1}{T_3} - \frac{1}{T_2}\right) + 1$ $F = \frac{T_3}{T_1 T_2}$

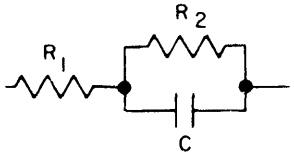
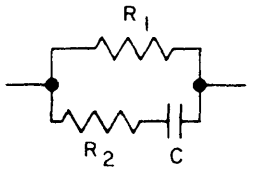
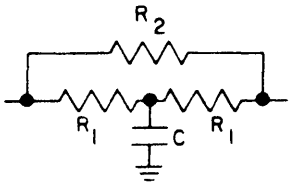
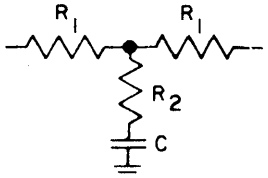
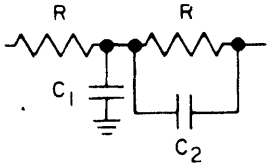
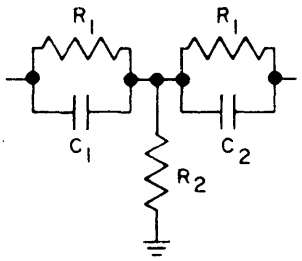
(2) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S., "Analog Computation", and Fifer, S. "Analog Computation". (See Bibliography.)

NOTE

The short-circuit admittance of a two or three terminal network represented by 

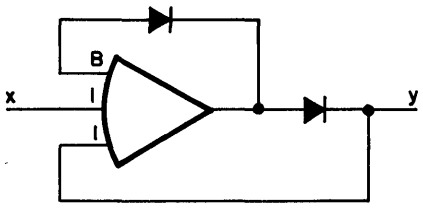
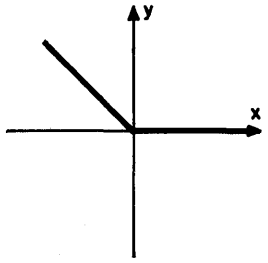
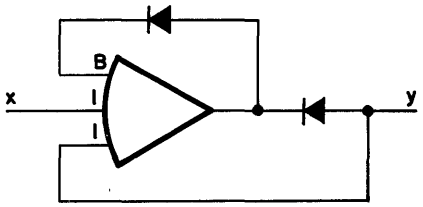
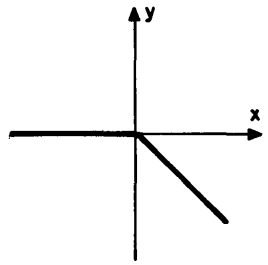
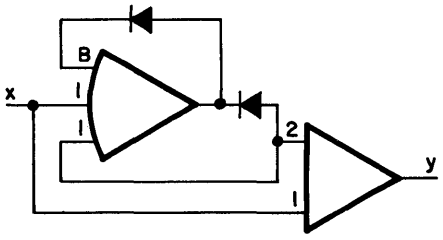
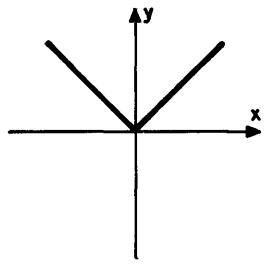
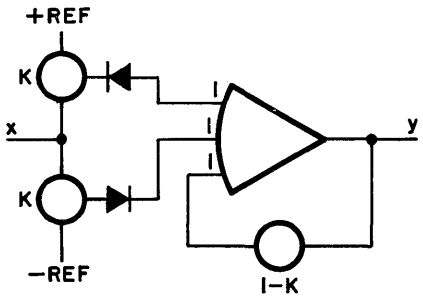
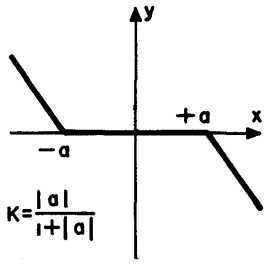
is given by the ratio of $I_o(P)/E_i(P)$ *from* 

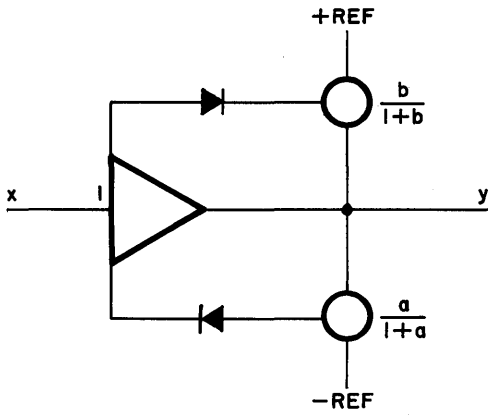
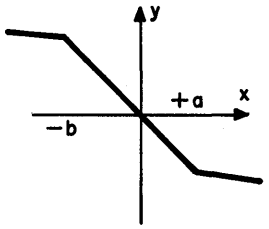
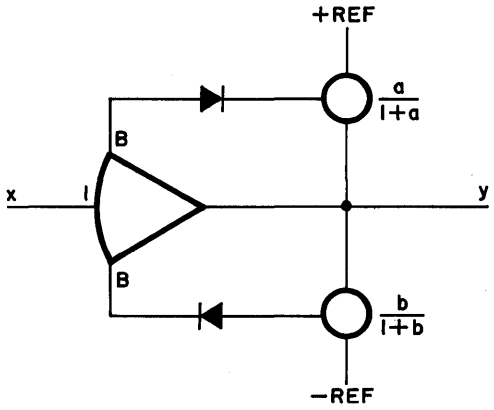
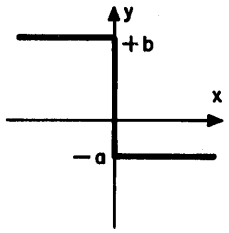
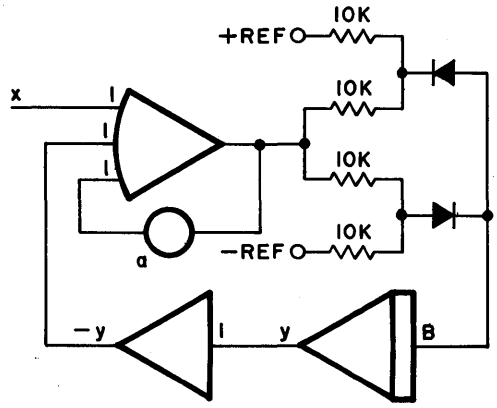
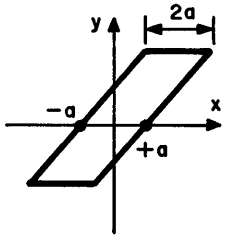
NO.	SHORT-CKT ADMITTANCE	NETWORK	PARAMETERS
1.	$\frac{1}{A}$		A = R
2.	$\frac{1 + pT}{A}$		A = R T = RC
3.	$\frac{1}{A\,(1 + pT)}$		A = 2R $T = \frac{RC}{2}$

NO.	SHORT-CKT ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1$ $T = (R_1 + R_2)\, C$ $\theta = \frac{R_2}{R_1 + R_2}$
6.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = \frac{2R_1 R_2}{2R_1 + R_2}$ $T = \frac{R_1 C}{2}$ $\quad \theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R_1$ $T = \left[R_2 + \frac{R_1}{2}\right] C$ $\theta = \frac{2R_2}{2R_2 + R_1}$
8.	$\frac{1}{A}\,\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left[\frac{(1+pT_1)(1+pT_3)}{(1+pT_2)}\right]$ $T_1 > T_2 > T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T_2 = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right] (C_1 + C_2)$ $T_3 = R_1 C_2$

APPENDIX 4

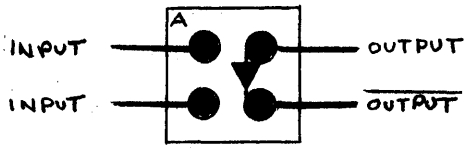
REPRESENTATION OF CONSTRAINTS AND NONLINEARITIES

1. HARD ZERO LIMIT		
2. HARD ZERO LIMIT		
3. ABSOLUTE VALUE	 FOR $-\|x\|$, REVERSE THE DIODES	
4. DEAD SPACE		

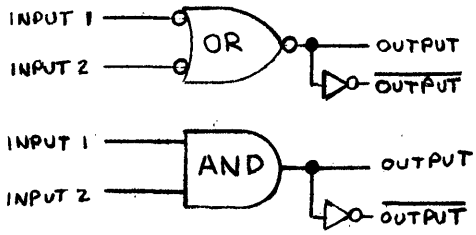
5. LIMITER		
6. BANG−BANG CIRCUIT (CAN BE USED AS COMPARATOR		
7. BACKLASH (HYSTERESIS)		

APPENDIX 5

LOGIC PATCHING



PATCHING

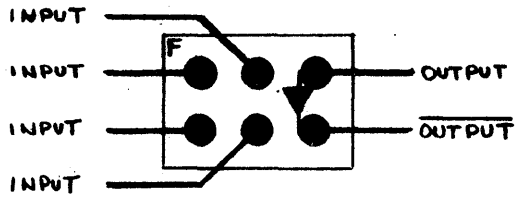


PROGRAMMER'S SYMBOLS

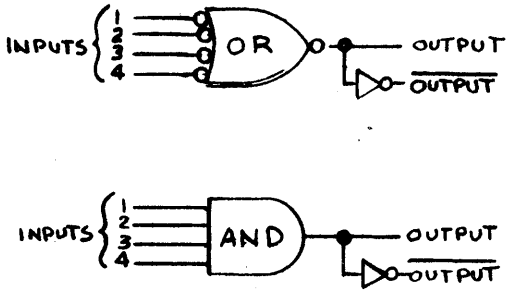
INPUTS		OUTPUT
1	2	
L	L	L
L	H	L
H	L	L
H	H	H

TRUTH TABLE

TWO INPUT AND GATE PATCHING



PATCHING



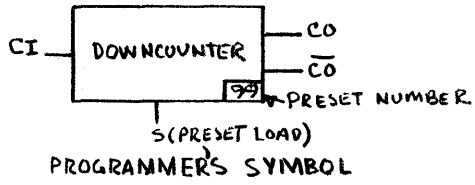
PROGRAMMER'S SYMBOLS

INPUTS				OUTPUT
1	2	3	4	
L	L	L	L	L
H	L	L	L	L
H	H	L	L	L
H	H	H	L	L
H	H	H	H	H

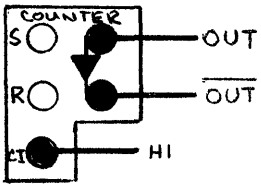
TRUTH TABLE

FOUR INPUT AND GATE PATCHING

DOWNCOUNTER PATCHING



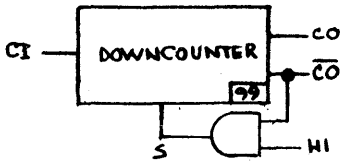
PROGRAMMER'S SYMBOL



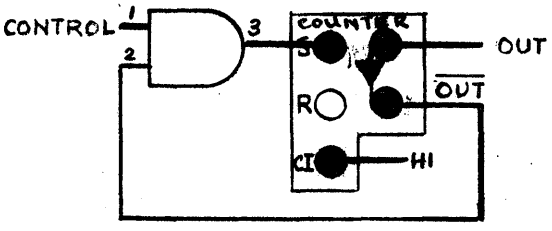
PATCHING

NOTES: 1. SELECT NUMBER OF COUNTS USING THUMBWHEEL SWITCHES ON LOGIC CONTROL PANEL.
2. PATCH CI INPUT HIGH.
3. DEPRESS S PUSHBUTTON ASSOCIATED WITH THE COUNTER, TO LOAD PRESET VALUE. LOADING CAN ALSO BE ACCOMPLISHED USING THE S PATCH TERMINAL WHICH PARALLELS THE S PUSHBUTTON
4. COUNTER COUNTS TO ZERO AT CLOCK RATE. A ZERO, COUNTER OUTPUT IS INHIBITED AND CARRY OUT (CO) GOES LOW AND $\overline{CO}$ GOES HIGH.
5. THE CARRY IN (CI) HOLE MAY BE PATCHED TO OTHER INPUTS (PATCH PANEL CLOCK OUTPUTS) AND USED AS A COUNTER.

TIMER MODE



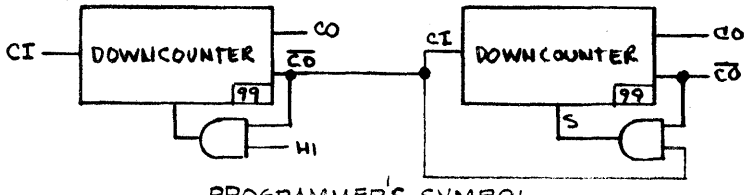
PROGRAMMER'S SYMBOL



PATCHING

NOTES: 1. OPERATION OF RING COUNTER IS THE SAME AS THE COUNTER ABOVE, EXCEPT FOR AND GATE. PATCHED AS SHOWN, COUNTER IS RELOADED TO THE PRESET VALUE EACH TIME COUNT REACHES ZERO.
2. INPUT 1 OF AND GATE IS USED AS A CONTROL INPUT.

TIMER MODE



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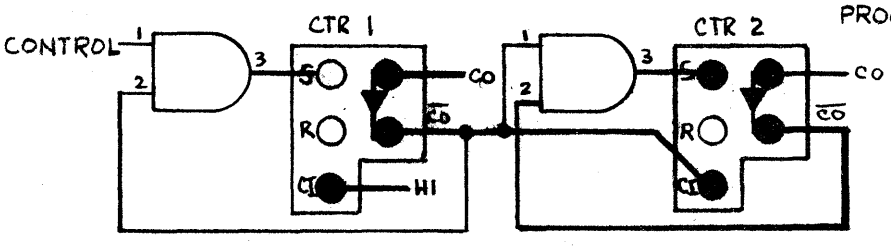
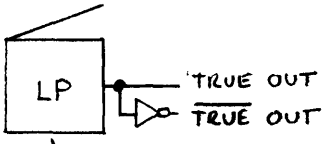


PATCHING

NOTE: WHEN CTR 1 REACHES ZERO $\overline{CO}$ GOES HIGH RELOADING CTR 1 AND LOADING CTR 2. CTR 1 $\overline{CO}$ GOES LOW INHIBITING CTR 2 AFTER ONE CLOCK PERIOD.

CASCADED COUNTERS



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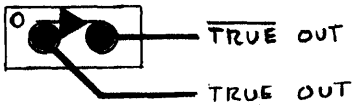
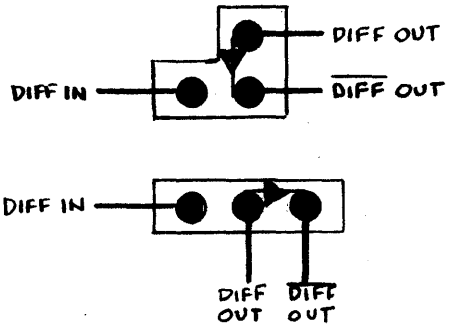


PATCHING

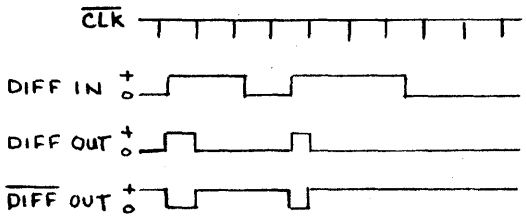
NOTES: 1. PUSHBUTTON IS A SYNCHRONOUS LATCHING SWITCH.
2. TRUE OUTPUT HIGH WHEN ASSOCIATED LETTERED PUSHBUTTON ON LOGIC CONTROL PANEL IS DEPRESSED.
3. TRUE OUTPUT LO WHEN ASSOCIATED UNLETTERED PUSHBUTTON IS DEPRESSED.
4. PUSHING UNLETTERED PUSHBUTTON AGAIN PRODUCES 1 μSEC PULSES FOR PROGRAM CHECKOUT.

DIGITAL PUSHBUTTON PATCHING

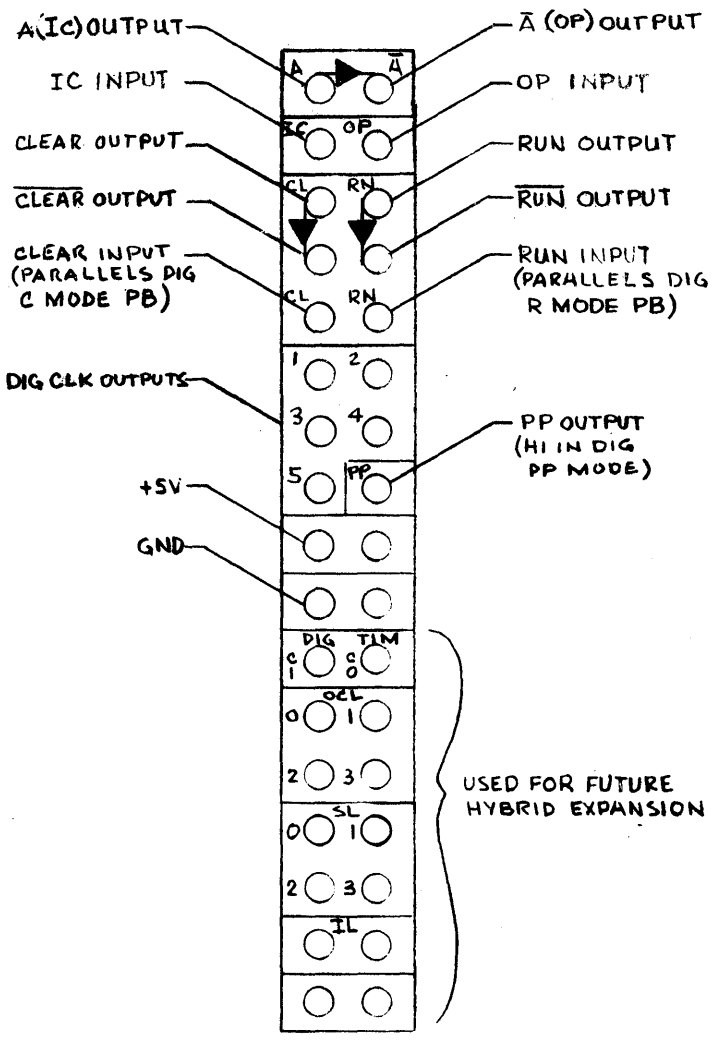
PROGRAMMER'S SYMBOL



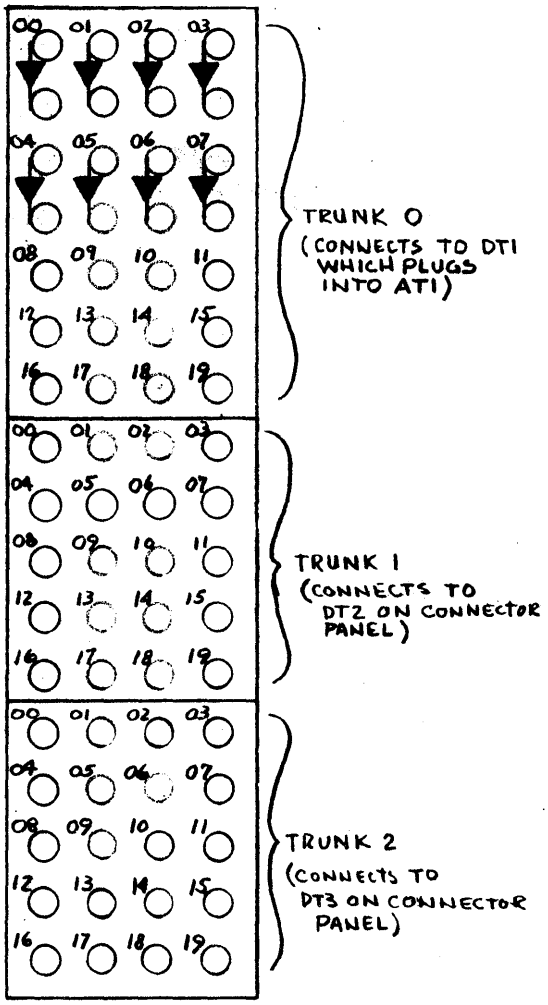
PATCHING



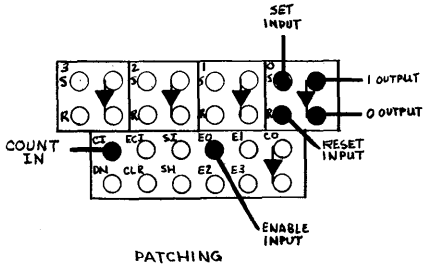
DIFFERENTIATOR PATCHING



MISCELLANEOUS PATCHING TERMINATIONS

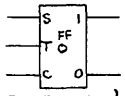


DIGITAL TRUNK PATCHING TERMINATIONS



PATCHING

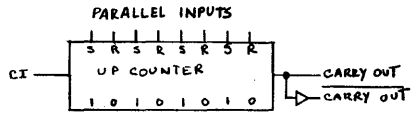
NOTE: OPERATION OF FF1, 2, & 3 IS IDENTICAL TO FF0.

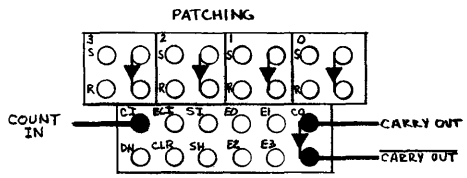


PROGRAMMER'S SYMBOL

E IN	S	R	DESCRIPTION
0	ANY	ANY	NO CHANGE OF STATE
1	1	0	FF IS SET (1=HI-O=LO) ON NEXT CLK
1	0	1	FF IS RESET (1=LO-O=HI) ON NEXT CLK
1	0	0	NO CHANGE
1	1	1	FF TOGGLES ON EACK CLK.

(a.) INDIVIDUAL FLIP-FLOP MODE

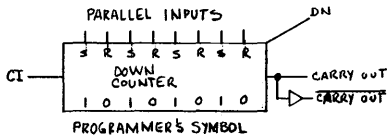




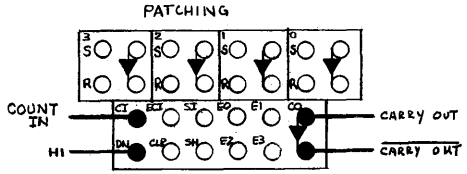
NOTES: 1. COUNTER IS PRESET USING REGISTER PB ON LOGIC CONTROL PANEL (i.e. PB 0 PRESETS FF1, PB1 PRESETS FF2, PB2 PRESETS FF4, PB3 PRESETS FF8). PRESET FF IS INDICATED WHEN THE LAMP BEHIND LETTERED PB IS LIT. FF NOT USED IN PRESET OPERATION, ARE RESET USING THE UNLETTERED PB ON THE RIGHT OF THE LETTERED PB.
2. UP COUNT OF 16 COUNTS (0 TO 15) IS POSSIBLE.
3. CO GOES HI ONLY WHEN COUNTER REACHES 0.

EXAMPLE: FOR A COUNT OF 9, PRESET 7 (16-7=9) [PRESET FF 1, 2 & 4]. START CLK., COUNT INCREASES BY 1 BIT PER CLK PULSE. CO REMAINS LO UNTIL 16 COUNT (0) IS REACHED.

(b) UP COUNTER MODE



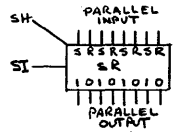
PROGRAMMER'S SYMBOL



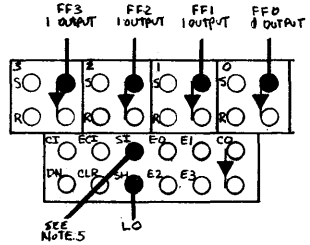
NOTES: 1. COUNTER IS PRESET USING REGISTER PB ON LOGIC CONTROL (i.e. PB 0 PRESETS FF1; PB 1 PRESETS FF 2; PB2 PRESETS FF4; PB 3 PRESETS FF8). PRESET FF IS INDICATED WHEN LAMP BEHIND LETTERED PB IS LIT. FF NOT USED IN PRESET OPERATION, ARE RESET USING THE UNLETTERED PB ON THE RIGHT OF THE LETTERED PB.
2. DOWN COUNT OF 16 COUNTS (15 TO 0) IS POSSIBLE.
3 CO GOES HI ONLY WHEN COUNTER REACHES 0.

EXAMPLE: PRESET 7 (PRESET FF 1, 2 & 4). START CLOCK. COUNT DECREASES BY 1 BIT PER CLK PULSE, CO REMAINS LO FOR 6 COUNTS, GOES HI ON 7 COUNT (0).

(c) DOWN COUNTER MODE



PROGRAMMERS SYMBOL



PATCHING

NOTES: 1. FOR SHIFT REGISTER (SR) OPERATION-PATCH SH HI (+V). RESET ALL FLIP FLOPS.
2. EACH SR IS CAPABLE OF SHIFTING A BIT THROUGH 4 REGISTERS.
3. A BIT IS LOADED INTO THE SR BY MEANS OF THE PRESET PB.
4. THE BIT IS THEN SHIFTED TO EACH SUCCESSIVE REGISTER AT THE RATE OF ONE SHIFT PER CLK PULSE.
5. THE SR MAY BE USED AS A RING COUNTER BY PATCHING THE 1 OUTPUT OF FFS TO THE SI TERMINAL.

(d) SHIFT REGISTER MODE

GENERAL PURPOSE REGISTER PATCHING

APPENDIX 6

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