EMULEX

EMULEX STORAGE TECHNOLOGY

EMULEX SCSI PROCESSOR ESP 216*

FEATURES

- Oriented to host applications and 16-bit applications
- Supports ANSI X3.131 1986 SCSI standard
- Provides on-chip single-ended receivers and 48mA drivers from SCSI bus
- SCSI parity generation with optional checking
- Parity pass through on FIFO data
- Functions as initiator or target
- Supports asynchronous SCSI bus transfers up to 6MB/sec
- Supports synchronous SCSI bus transfers up to 5MB/sec
  -Programmable synchronous transfer period
  -Programmable synchronous transfers offsets, up to 15 bytes
- Provides 16-byte data FIFO between the microprocessor DMA and SCSI bus channels
- Up to 20MB/sec DMA burst transfer rate (10 megatransfers per second)
- Utilizes pipelined command structure
- Implements common SCSI sequences without microprocessor intervention
  -Selection sequence, from arbitration through command
  -Reselection sequence, from arbitration through message
  -Bus-initiated selection through received command
  -Bus-initiated reselection through received message
  -Command complete sequences
  -Terminate and disconnect sequences

*ESP 216 will refer to ESP 226 and ESP 236 as well, except as noted

- Four bus configurations
  -Separate microprocessor address control:
  . Single bus to 8-bit microprocessor and 8-bit DMA
  . Single bus to 8-bit microprocessor and 16-bit DMA
  . Separate 8-bit microprocessor bus and 16-bit DMA bus
  -Separate 8-bit multiplexed address/data microprocessor bus and 16-bit byte-controlled DMA bus
- DMA interface options
  -Threshold-8 option
  -Alternate DMA Mode
  -Save Residual Byte option
  -FIFO preload
- Interrupts microprocessor only when service is required
  -Disconnect or bus reset
  -Selection/reselection sequence complete
  -Target mode command complete or ATN detected
  -Initiator mode command complete or phase change and REQ detected
- Supports clock rates of up to 25MHz
- Interfaces to 8-bit microprocessor data bus with no support logic
- Low power requirements
- Packaging
  -216 - 84 PLCC
  -226 - 84 PLCC
  -236 - 100 PQFP

DESCRIPTION

The ESP 216, ESP 226 and ESP 236 chips are new versions of the ESP 200 Emulex SCSI Processor chip. They all add a 16-bit split-bus architecture to the ESP design. The ESP 216 operates in SCSI single-ended mode only; the ESP 226 operates in SCSI differential mode only; and the ESP 236 combines the features of both into a single package, supporting both single-ended and differential operations. All three versions are designed to maximize transfer rates over the SCSI bus. Operating in both the Target and Initiator roles, the ESP 216 can be used in both host adapter and peripheral applications.

The ESP 216 performs such functions as bus arbitration, selection of a target, or reselection of an initiator. It handles message, command, status, and data transfer between the SCSI bus and the chip's 16-byte internal FIFO, or a buffer memory. These functions are internal processes that the ESP 216 chip performs **without microprocessor intervention.**

The chip maximizes protocol efficiency by utilizing a first-in, first-out command pipeline and combination commands to minimize host intervention. The ESP 216 also maximizes transfer rates by sustaining asynchronous data rates up to 6.0MB/sec and synchronous data rates of 5.0MB/sec (at 25MHz). With its on-chip 48mA, single-ended drivers and receivers, the ESP 216 can be directly connected to the SCSI bus, thus minimizing board space requirements.

The ESP 216 SCSI processor controller systems support three main busses: the 8-bit SCSI bus, the 8-bit or 16-bit Data Bus (DB), and the 8-bit Processor Address Data (PAD) bus. The versatile ESP 216 architecture supports four different DB/PAD bus configurations. This split-bus architecture separates the two high-traffic information flows of the system, providing maximum efficiency and throughput.

Figure 1 shows the internal architecture of the ESP 216.

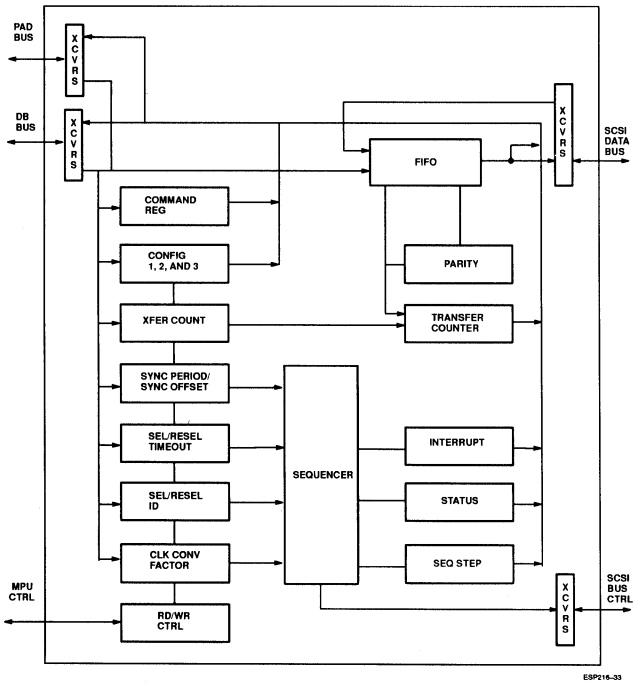


Figure 1. ESP 216 Block Diagram

The ESP 216 replaces existing SCSI interface circuitry which typically consists of discrete devices, external drivers, and a low performance SCSI interface chip. The ESP 216 contains a fast DMA interface, a 16-byte FIFO, and fast asynchronous and synchronous data interface to the SCSI bus, including drivers.

The ESP 216 has been optimized for interaction with the controller microprocessor. Common SCSI bus sequences that would typically require significant amounts of processing and interaction have been reduced to single commands.

The commands are:

Sequence	Description
Selection	Arbitration, target selection, transmission of an optional one-byte or 3-byte message followed by a multiple-byte command
Reselection	Arbitration, initiator reselection and transmission of a one-byte message
Bus-initiated selection	Selection detection, receipt of a one-byte or a 3-byte message, command length decode, and receipt of a command (if the message was IDENTIFY)
Bus-initiated reselection	Reselection detection and receipt of a one-byte message
Target command complete	Transmission of a status byte and a one-byte message followed by disconnection from the SCSI bus
Target disconnection	Transmission of two one-byte messages followed by disconnection from SCSI bus
Initiator command complete	Receipt of a status byte and a one-byte message

To reduce overhead further, the ESP 216 Transfer Counter contains a double-ranked Command Register which provides a transfer-command pipeline, allowing command stacking. The double ranked Transfer Counter with memory controllers such as Emulex's Buffer Controller 2, which supports buffer setup overlap, removes time lost in interbuffer overhead.

SYSTEM ORGANIZATION

The ESP 216 versatile bus architecture supports various microprocessor DMA bus configurations, such as those listed below.

- Microprocessor interface via the PAD bus or the DB bus
- Concurrent microprocessor access and DMA data transfer
- Single-bus or split-bus operation
- PAD bus selectable as a data-only bus or as a multiplexed address and data bus
- DB bus selectable for 8-bit transfers, or 16-bit transfers with byte control option

ESP 216 bus configuration is selected by pulling the MODE1 and MODE0 signals up or down, as below.

Table 1. Bus Configuration

Mode No.	MODE Register 1	0	Addr	Data	Configuration
0	0	0	A3-0	DB Bus	Single-bus, 8-bit DMA
1	0	1	A3-0	DB Bus	Single-bus, 16-bit DMA
2	1	0	PAD3-0	PAD Bus	Split-bus, 16-bit DMA, byte control option
3	1	1	A3-0	PAD Bus	Split-bus, 16-bit DMA

PROCESSOR INTERFACE

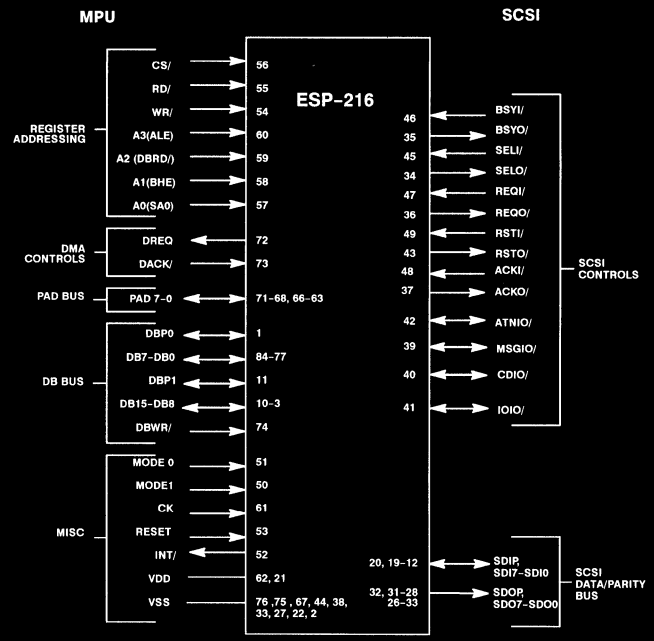
The processor can interface to the ESP 216, ESP 226, or ESP 236 using either the PAD bus or the DB bus (see Figures 2 and 3). Both interfaces allow the processor to read and write to all chip registers (including the FIFO). The PAD bus allows the processor an interface to the chip registers independent of DMA activity on the DB bus. All register accesses are 8 bits wide.

DMA INTERFACE

All ESP 216 DMA activity occurs over the DB bus. The DB bus may be configured as either an 8-bit or 16-bit data bus, with a parity bit for each byte on the bus. If byte control is enabled, the DMA controller can control how the bytes are placed on the bus (MODE2 only).

SIGNALS

The ESP 216 acts as the interface between the microprocessor and the SCSI bus, in either a target or initiator mode. Refer to Figure 2 (ESP 216/ESP 226 Functional Signal Grouping) and Figure 3 (ESP 236 Functional Signal Grouping) which group the chip pins into those that interface with the microprocessor and those that interface with the SCSI bus.



*Sec pin description

Fig. 2. ESP 216/226 Functional Signal Grouping

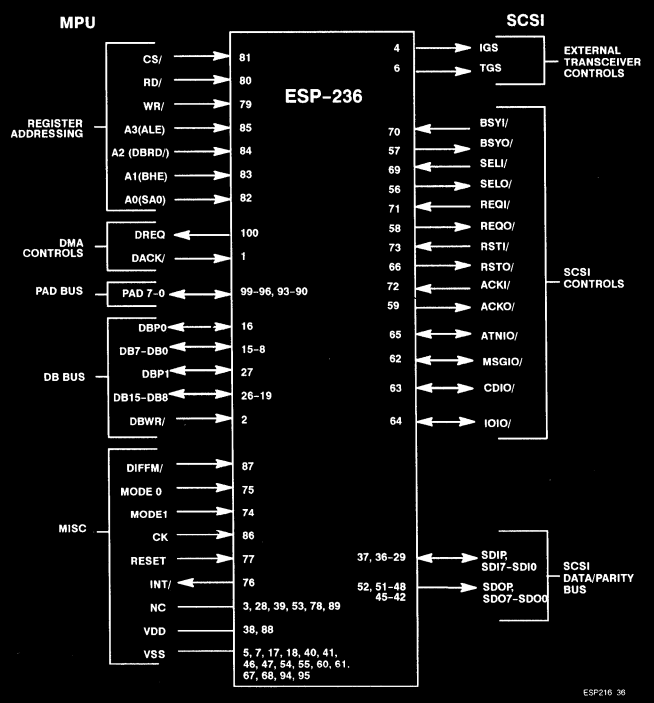


Fig. 3. ESP 236 Functional Signal Grouping

SCSI INTERFACE

The ESP 216 operates in single-ended SCSI mode only. The ESP 226 operates in differential SCSI mode only. The ESP 236 interface can be configured in either differential mode or single-ended mode using the differential mode enable (DFFM/) pin. When DIFFM/ is high, the ESP 236 operates in single-ended mode; when it is held low, the ESP 236 operates in differential mode.

PACKAGING

The ESP 216 and ESP 226 chips are available in a 84-pin PLCC for surface or socket mounting. The ESP 236 is available in a 100-pin plastic quad flat pack (PQFP). Part numbers are:

	84pPLCC	100pPQFP
ESP 216	2400008	
ESP 226	2400009	
ESP 236		2400039

PIN DESCRIPTION

Figure 4 shows the signal names associated with each pin of the ESP 216/226 84-pin PLCC. The diagram is viewed from the top of the chip, with the pins facing away from the reader. The pins for the ESP 216 and ESP 226 are identical, with the exception of pins 75 and 76. Pins 75 and 76 in the ESP 216 are VSS; in the ESP 226, pin 75 is IGS and pin 76 is TGS.

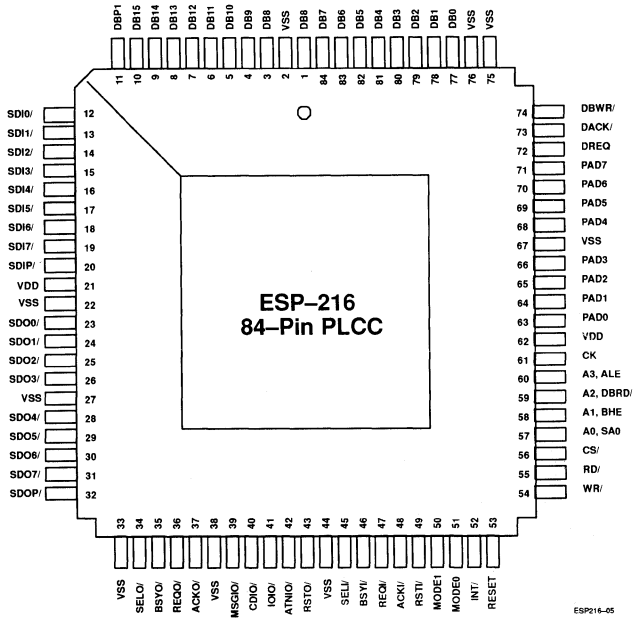


Figure 4 ESP 216 84-Pin PLCC Pin Diagram

Figure 5 shows the signal names associated with each pin of the ESP 236 100-pin PQFP. The diagram is viewed from the top of the chip, with the pins facing away from the reader.

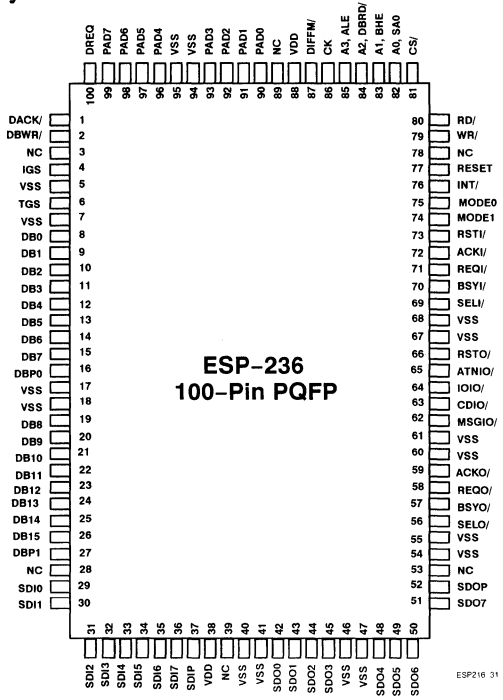


Figure 5. ESP 236 100-pin PQFP Pin Diagram

REGISTERS and COUNTERS

The ESP 216 registers are used by the microprocessor to control the operation of the SCSI bus. Through these registers, the microprocessor can configure, command, monitor, and pass data through the chip to the SCSI bus. These registers are listed in Tables 2 and 3.

Table 2. ESP216 Registers

Addr (h)	Read Registers	Write Registers
00	Transfer Counter Low	Transfer Count Low
01	Transfer Counter High	Transfer Count High
02	FIFO	FIFO
03	Command	Command
04	Status	Select/Reselect Bus ID
05	Interrupt	Select/Reselect Timeout
06	Sequence Step	Synch Transfer Period
07	FIFO Flags	Synchronous Offset
08	Configuration #1	Configuration #1
09	Reserved	Clock Conversion Factor
0A	Reserved	Test
0B	Configuration #2	Configuration #2
0C	Configuration #3	Configuration #3
0D	Reserved	Reserved
0F	Reserved	FIFO Preload

Fig. 6. ESP 216 Register Illustrations

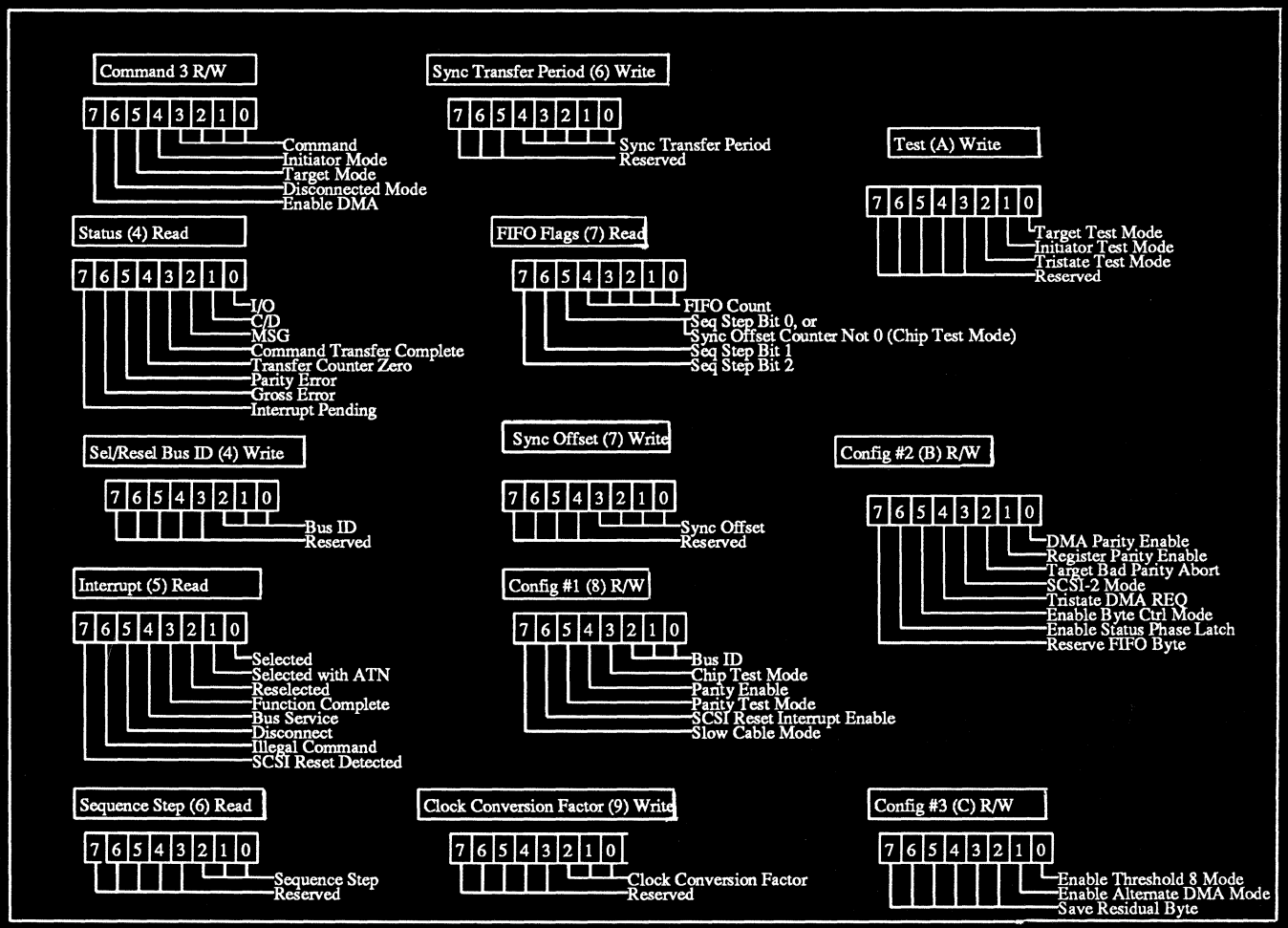


Table 3. ESP 216 Command Set

Codes(h) Non-DMA	Codes(h) DMA	Command	Interrupt[1]
		Disconnected	
40	C0	Reselect Sequence	Y
41	C1	Select w/o ATN Sequence	Y
42	C2	Select with ATN Sequence	Y
43	C3	Select with ATN and Stop	Y
44	C4	Enable Select/Reselect	N
45	--[2]	Disable Select/Reselect	Y
46	C6	Select w/ATN3 Sequence	Y
		Target	
20	A0	Send Message	Y
21	A1	Send Status	Y
22	A2	Send Data	Y
23	A3	Disconnect Sequence	Y
24	A4	Terminate Sequence	Y
25	A5	Target Command Complete Sequence	Y
27	--2	Disconnect	N
28	A8	Receive Message Sequence	Y
29	A9	Receive Command	Y
2A	AA	Receive Data	Y
2B	AB	Receive Command Sequence	Y
04	--[2]	Stop DMA	N
		Initiator	
10	90	Transfer Information	Y
11	91	Initiator Command Complete Sequence	Y
12	--[2]	Message Accepted	Y
--	98	Transfer Pad	Y
1A	--[2]	Set ATN	N
1B	--[2]	Reset ATN	N
		Miscellaneous	
00	--[2]	NOP	N
01	--[2]	Flush FIFO	N
02	--[2]	Reset Chip	N
03	--[2]	Reset SCSI Bus	N

[1]"Y" value indicates interrupt generated after command completion

[2]Transfer Counter is loaded at beginning of this command, but no DMA occurs

Command Register - Address 03h (Read/Write)

The Command Register is an 8-bit, read/write register that is actually a two-byte deep FIFO, enabling the microprocessor to stack commands to the ESP 216. This register is read from the bottom of the FIFO, and returns the value of the last executed, or executing command. Reading the Command Register has no effect upon the contents of the register.

The bottom command begins executing within six clock cycles after dropping to the bottom of the Command Register. If applicable, an interrupt is generated at command completion. (Refer to Table 3 for commands that generate interrupts.)

Once the bottom command has completed, the top command, if present, falls to the bottom and executes. If both the bottom command and the top command generate interrupts, and the first interrupt has not been serviced, the second interrupt is stacked behind the first. The Microprocessor must service the first interrupt (by reading the Status Register, Sequence Step Register, and Interrupt Register) prior to issuing a third command. After servicing the first interrupt, the Status Register, Sequence Step Register, and Interrupt Register are updated to apply to the second interrupt.

Note that the Reset Chip, Reset SCSI Bus, and Target Stop DMA commands execute within four clock cycles of being loaded into the top of the Command Register.

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