M2321K/2322K

Disk Drives
Customer Engineering Manual

FUJITSU

B03P-4740-0111A-02C

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Note 1: A revision of each page except "A" is indicated by the Revision Letter with the specification number of this manual in the bottom of the page.

Note 2: A bar by the page number in this page indicates pagination rather than content has changed.

Preface

This manual explains how to operate, handle, and maintain the M2321K/M2322K micro-disk drives.

The information is provided in 10 sections:

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Illustrations

Tables

Section 1

General Description

1. GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

1.1.1 General Description

This manual describes the Fujitsu 8-inch rigid disk drives M2321/M2322. These units contain non-removable disks in a sealed module. A rotary actuator using a closed loop servo performs head positioning.

These drives have floppy disk drive dimensions and can be mounted horizontally two drives wide in a 19-inch rack (with 3 pitch) or mounted vertically in a system cabinet.

The contact start/stop (CSS) type heads and media are of the whitney technology type. These units feature high performance, high reliability and low cost.

The maximum unformatted storage capacities of the M2321 and M2322 units are 84MB and 168MB , respectively.

The M2321 and M2322 utilize the industry standard SMD interface, thereby allowing the drives to be added to an existing disk configuration.

By standardizing on the SMD interface, development time for controllers and software will be substantially reduced. Fixed and variable sector length formats are internally selectable.

To power the drives only DC voltages of +24, +5 and −12 volts are required. This allows for international use. Total nominal power consumption is less than 150 watts.

1.1.2 Features

(1) High reliability
   (a) Whitney type technology contact-start/stop (CSS) heads and media are used.
   (b) Each head has an LSI circuit on its arm to amplify the small signal thereby reducing read errors by increasing the signal to noise ratio.
   (c) The heads, media and positioning mechanism are sealed in a closed-loop air filtration system.
   (d) The electrical components located within the sealed disk area are minimized.

(2) Maintainability
   No scheduled maintenance is required.
   The use of a completely sealed DE, a belt-eliminating built-in DC spindle motor, as well as highly reliable printed circuit assemblies, the necessity of maintenance is greatly reduced.

(3) Compact, Lightweight
   This unit can be mounted, two drives across in a standard 19-inch rack. The dimensions are almost floppy disk drive compatible. The weight of the unit is approximately 30 pounds (13.6 kg). Mounting equipment for the 19-inch rack can be provided as an option.

(4) Vertical/horizontal Mount Capability
   These units are available to vertical-mount and horizontal-mount by setting the ON-END switch to OFF, and ON-END mount by setting the ON-END switch to ON.

(5) Low accoustical noise level and low vibration allow for installation in an office environment.

(6) Uses only DC voltages. No internal changes are necessary for changes in frequency or power.

1.2 SPECIFICATIONS

1.2.1 Unit Specifications

The basic specifications of the disk drive are as follows:

Table 1-2-1 Basic Specifications

Model	Specification	Storage capacity
M2321K	B03B-4745-B001A	84M bytes
M2322K	B03B-4745-B002A	168M bytes

1.2.2 Physical Specifications

Table 1-2-2 Physical Specifications

Item	Conditions	Specifications
Dimension	Height	127mm (5.0")
	Width	216mm (8.5")
	Depth	380mm (15.0")
Weight*		13.6 kg (30 lbs)
Temperature	Operating	41°F to 104°F (5°C to 40°C)
Relative Humidity	Operating	20% to 80% (no condensation)
Temperature Variation	Operating	< 27°F/hr (15°C/hr) (no condensation)
Altitude	Operating	10,000 feet (3,000 m)
Vibration	Operating	0.2G max. (3 Hz to 60 Hz)
		Both ways 2 minutes x 30 cycle (sine wave)
Shock	Operating	< 2.0G, 10 ms
Temperature	Non-operating	-40°F to 140°F (-40°C to 60°C)
Relative Humidity	Non-operating	5% to 95% (no condensation)
Altitude	Non-operating	40,000 feet (12,000 m)
Vibration	Non-operating	0.4G max. (3 Hz to 60 Hz)
		Both ways 2 minutes x 30 cycle (sine wave)
Shock	Non-operating	<15G, 10 ms
Dust		Less than 0.168 mg/m^3 (Stearic acid standard)

1.2.3 Power Requirements

The M2321K and M2322K requires +5V, -12V and +24V DC voltages from an optional power supply or system power supply. Each load current required by the drive is shown in Table 1-2-3.

Table 1-2-3 DC Power Requirement

DC Voltage	Load Current (Basic)	Load Current (With Dual Port)
+5V ± 5%	3.5A	4.5A
−12V ± 5%	3.0A	4.0A
+24V ± 10%	4.0 Arms (Effective, typical) 7.2 Ao-p (Maximum) 4.6 Arms (POW ON; Effective typical)	

Important Note: The D. C. return lines must be made electrically common at the Power Supply when using other then the optional Fujitsu Power Supply. Failure to commonize these lines will result in premature failure of the spindle motor circuit.

The load currents of +5V DC and −12V DC will be stable regardless of operation being performed within the disk drive, however, the load current of +24V DC will be varied during a power up sequence or DC motor acceleration and/or seek operation.

The +24V DC load current profile during power up sequence is shown in Figure 1-2-1.

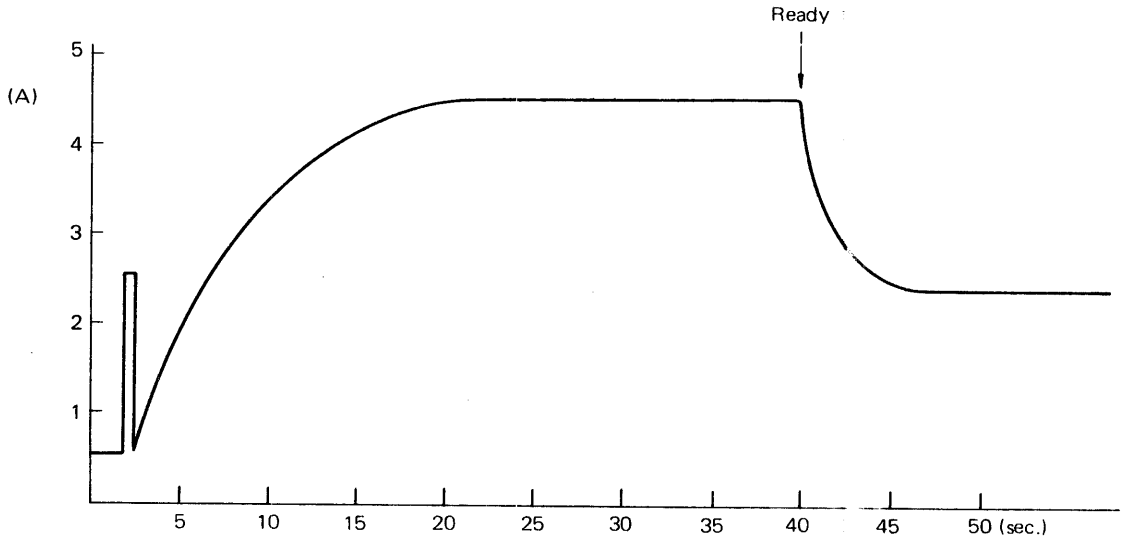


Figure 1-2-1 +24V DC Load Current on Power Up Sequence

The +24 DC load current profile during the repeated acceleration/inertia modes of DC motor and/or seek operation after Ready status is shown in Figure 1-2-2.

1.2.3.1 U.L./CSA

The M232XK disk drive is a U.L. recognized and CSA listed component. The appropriate file numbers are as follows:

U.L. 478 file #E62049 Vol. 3 Sec. 7
CSA 22.2 file #LR51352-3

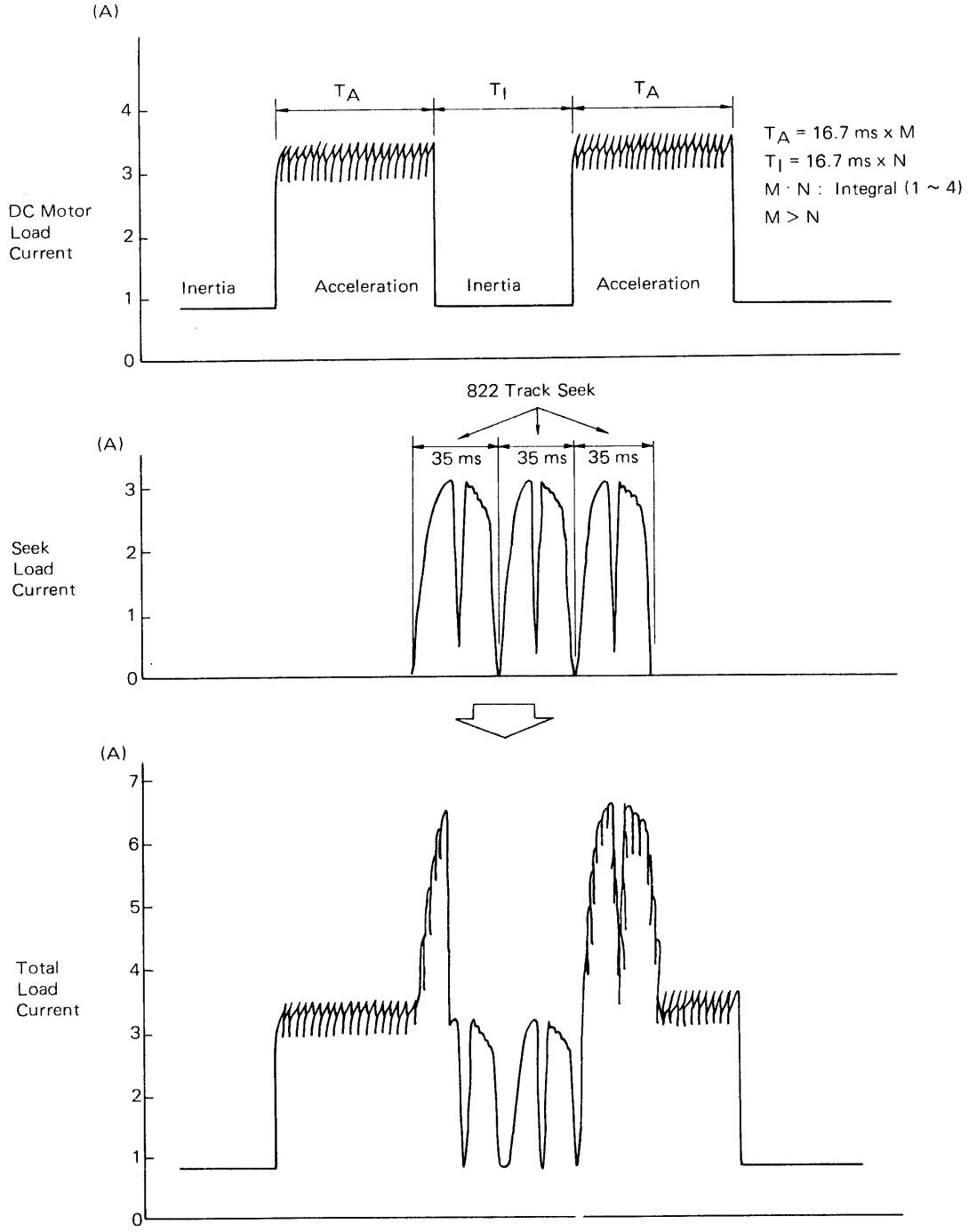


Figure 1-2-2 Total +24V DC Load Current (Ready)

1.2.4 Data Recording Specifications

Data recording specifications are presented in Table 1-2-4.

Table 1-2-4 Data Recording Specifications

Item	Specifications	
	M2321	M2322
Storage capacity (unformatted)	84,275,200 bytes	168,550,400 bytes
Number of cylinders	823	823
Tracks per cylinder	5	10
Cylinder capacity	102,400 bytes	204,800 bytes
Track capacity	20,480 bytes	
Average rotational latency	8.3 ms	
Positioning time: Track to track	5 ms	
Average	20 ms	
Maximum	40 ms	
Rotational speed	3,600 rpm ± 1%	
Transfer rate	1.229 MB/sec	
Encoding method	MFM	
Interface data	NRZ	
Recording density	9,867 BPI	
Track density	683 TPI	
Start/Stop time	<50/ <40 sec	
Interface	SMD	
Number of sectors	128 (maximum)	

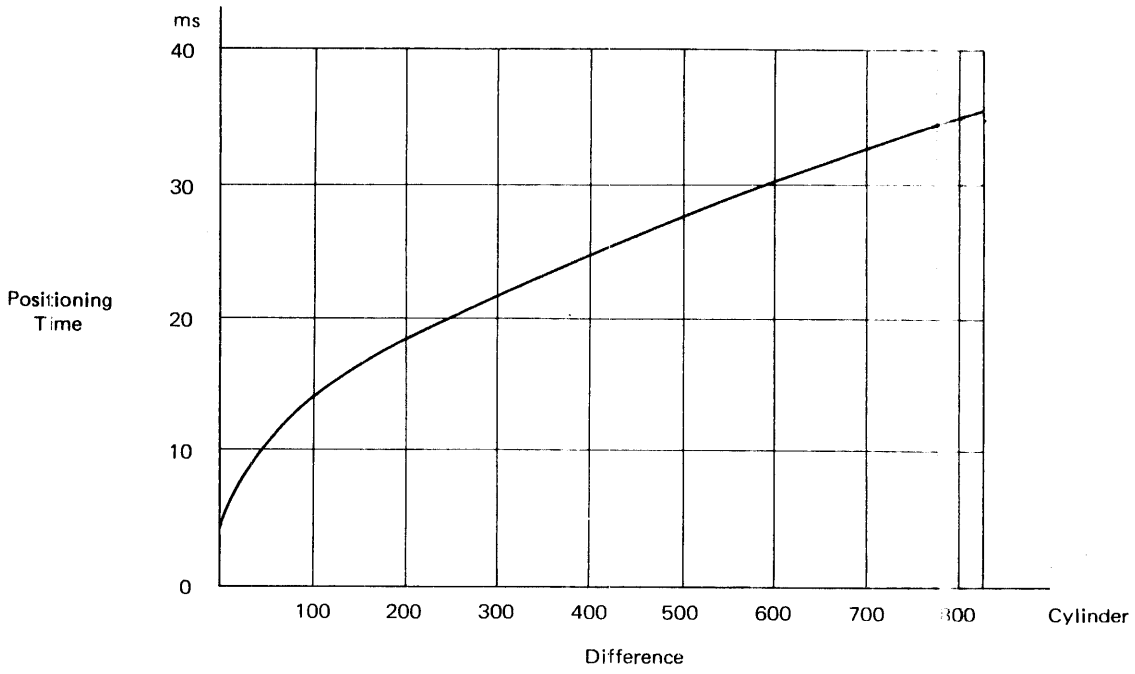


Figure 1-2-3 Positioning Time Profile

1.2.5 Reliability

(1) Mean Time between Failure (MTBF)
The MTBF is defined as follows:

$$MTBF = \frac{\text{Estimated Operating Hours}}{\text{Number of Equipment Failures}}$$

The MTBF shall exceed 20,000 hours (design value). Estimated operating hours should not include any maintenance time. Equipment failures means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding that caused by operator error, cable failure, or other failure not due to the equipment. To establish a meaningful MTBF, operating hours must be greater than 6,000 hours and shall include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repair or replacement on an unscheduled basis.

(2) Mean Time to Repair (MTTR)
The mean time to repair shall not exceed 1.0 hour. It is defined as the time for an adequately trained and competent service technician to diagnose and correct a malfunction.

(3) Preventive Maintenance Time
No scheduled maintenance is required.

(4) Service Life
The M2321/M2322 drive is designed to provide a useful life of five (5) years before factory overhaul or replacement is required.

(5) DC Power Loss
Data integrity is assured in the event of a power loss (data is not assured during write operation).

1.2.6 Data Integrity

The following error rates assume that the M2321/M2322 is being operated within specification. Errors caused by media defects or equipment failures are excluded.

1.2.6.1 Read Errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

(1) Recoverable Error Rate
A recoverable read error is one which can be read correctly within fifteen retries when reading on track, and should not exceed ten per 10^{11} bits.

(2) Unrecoverable Error Rate
An unrecoverable read error is one which cannot be read correctly within sixteen retries and should not exceed ten per 10^{14} bits.

1.2.6.2 Positioning Error Rate

The positioning error which can be corrected within one retry should not exceed ten per 10^{8} seeks.

1.2.6.3 Media Defects

A media defect is defined as a repetitive read error that occurs on a properly adjusted drive within specific operating conditions.

Valid data must not be written over known media defects, therefore, sector/track deallocation or skip displacement techniques must be utilized.

(1) Media Defect Characteristics
a) The maximum number of defects per drive is as follows:
M2321K (84MB): 100
M2322K (168MB): 200
b) The maximum number of defective tracks per drive is as follows:
M2321K (84MB): 14
M2322K (168MB): 28

A defective track is defined as a track having any of the following:

1. Two or three defects.
2. Defective logging areas

Note: No track shall have more than three defects.

(2) Media defect free areas are defined as follows:

1. Cylinder 0, Head 0 through 2
2. Any error in logging area to extent defined in the Media Defect Format

1.2.6.4 Media Defect Information

Each drive will have a Media Defect List which will list the following information.

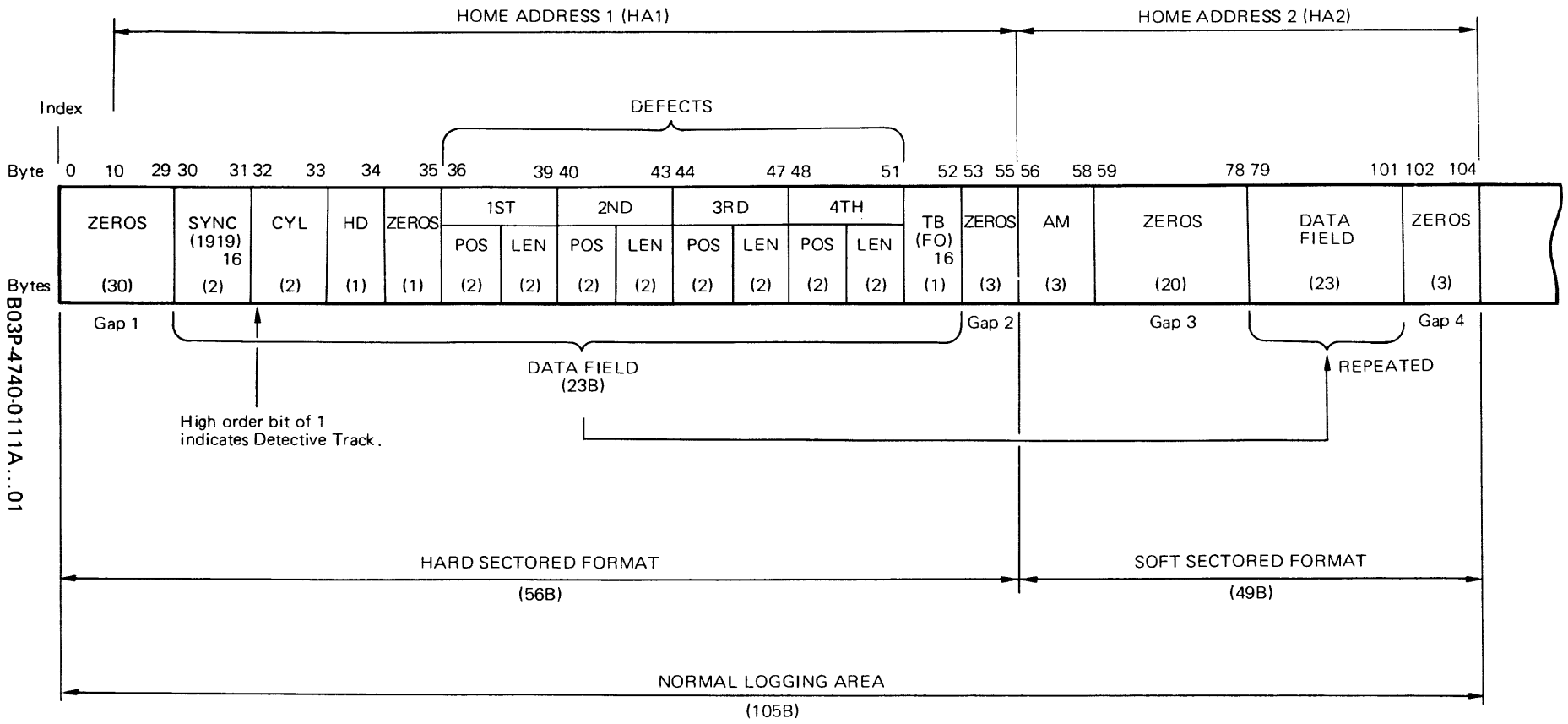
1. Cylinder Address
2. Head Address
3. Position (bytes from Index ±1 byte)
4. Length (bits ±1 bit)

The above information will be listed by hexadecimal code. The maximum media defect length at a defect is 64 bytes (512 bits).

1.2.6.5 Media Defect Format

The drive will be formatted at the factory with standard Media Defect Format. The Media Defect Format is divided into two parts. The first part is a hard-sectored format and is normally included in the first 56 bytes following Index signal. The second part is a soft-sectored format and is normally included in the next 49 bytes following Index signal as shown in Figure 1-2-4 Format 1. The format rules are as follows:

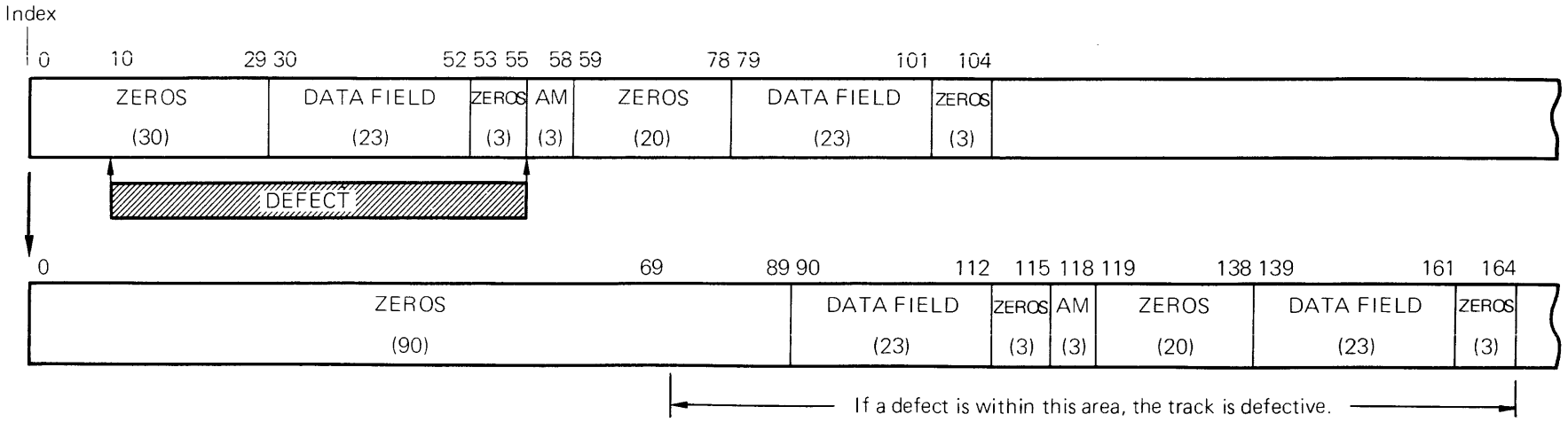
1. A track which has more than one defect is defined and flagged as a defective track. The first four media defects are logged.
2. If the beginning of a defect is located between Byte 10 to Byte 55 (HA1) after Index, 60 bytes of zeros are added to gap 1 (90 bytes total).
   In this case, if any part of a defect is located between Byte 69 and Byte 164 (HA1' and HA2'), the track is flagged as defective. Refer to Figure 1-2-5 Format 2.
3. If the beginning of a defect is located between Byte 56 and Byte 104 (HA2) after Index, 60 bytes of zeros are added before Address Mark (AM). In this case, if any of a defect is located between Byte 116 and Byte 164 (HA2''), the track is flagged as defective. Refer to Figure 1-2-5 Formats.
4. If the track is defined as a defective track according to above-mentioned rule 1, 2 or 3, the high order bit of the first cylinder address byte is set to 1. Remaining information may or may not be valid.



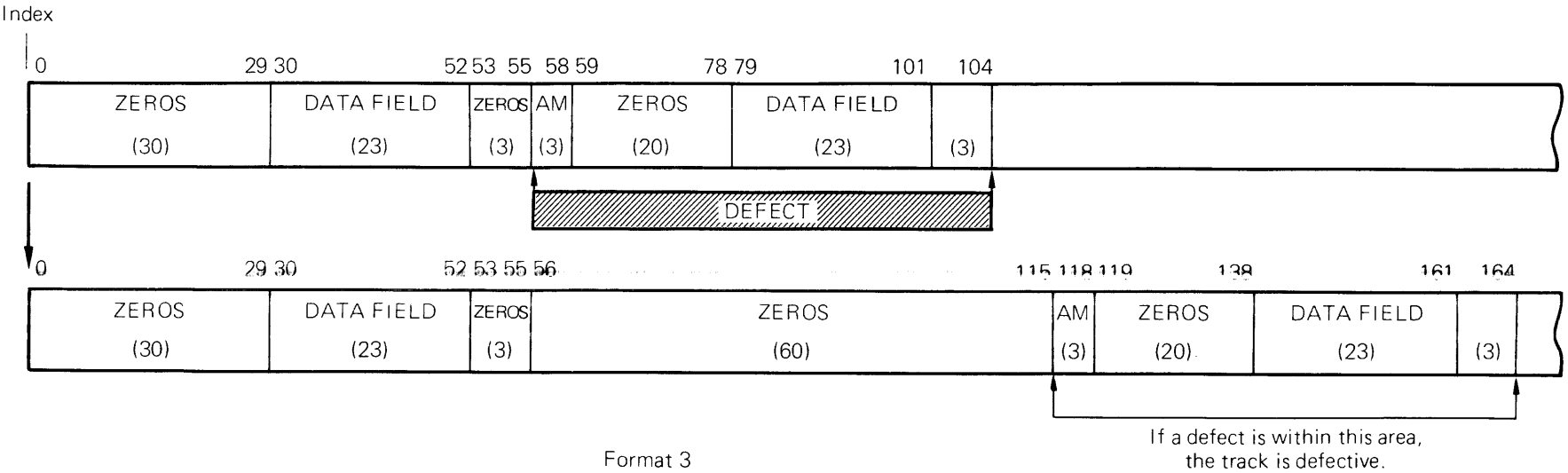
B03P-4740-0111A...01

Note 1) Position (POS) of defect is in bytes after Index ±1 byte.
2) Length (LEN) of defect is in bits ±1 bit.
3) Unused defect locations are all zeros.

Figure 1-2-4 Media Defect Format 1



Format 2



Format 3

Figure 1-2-5 Skip Displaced Format

1.3 CONFIGURATION

1.3.1 Fundamental Unit Configuration

Figure 1-3-1 shows the fundamental configuration of the unit; Figure 1-3-2 shows the block diagram.

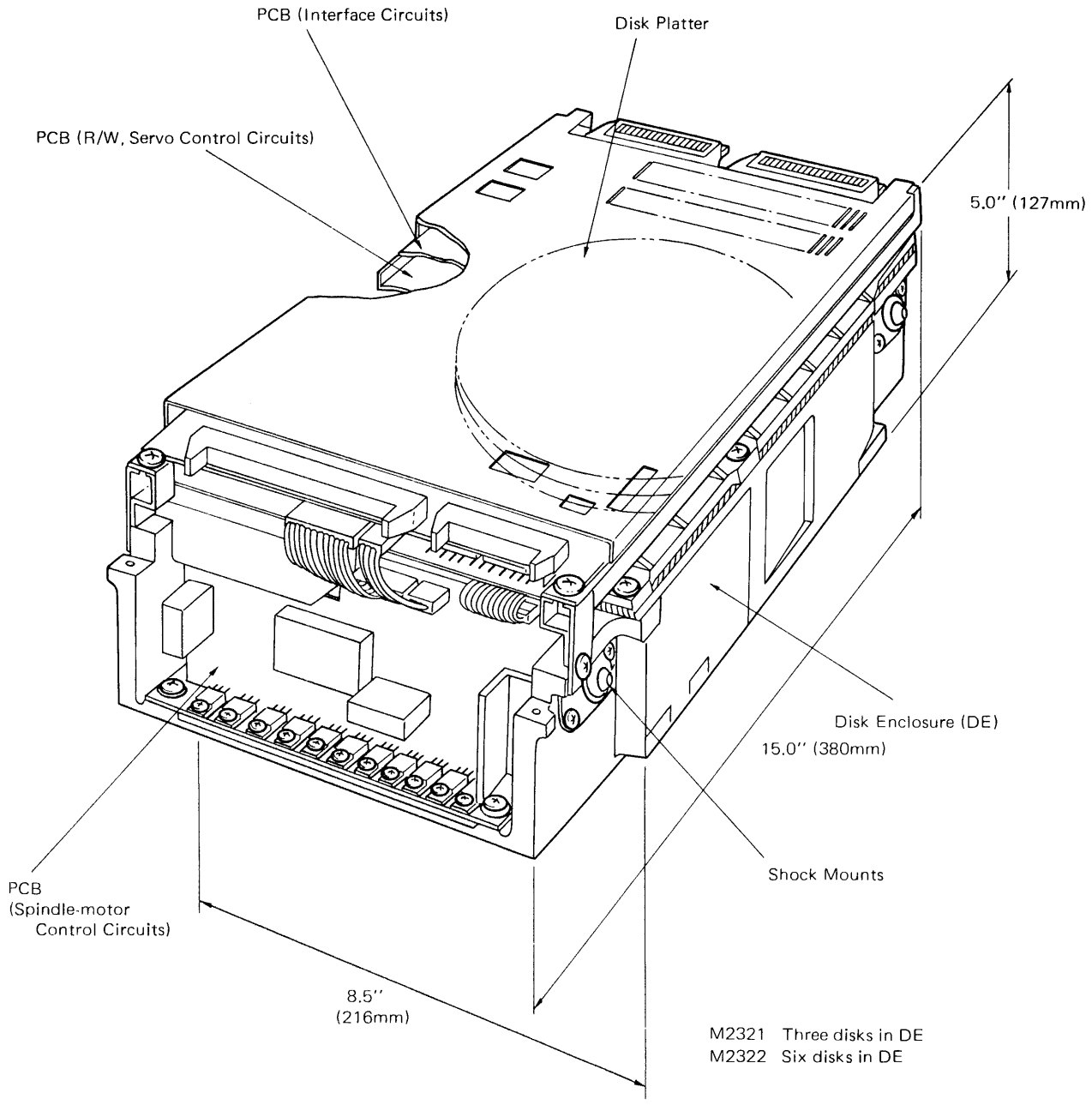


Figure 1-3-1 Fundamental Configuration

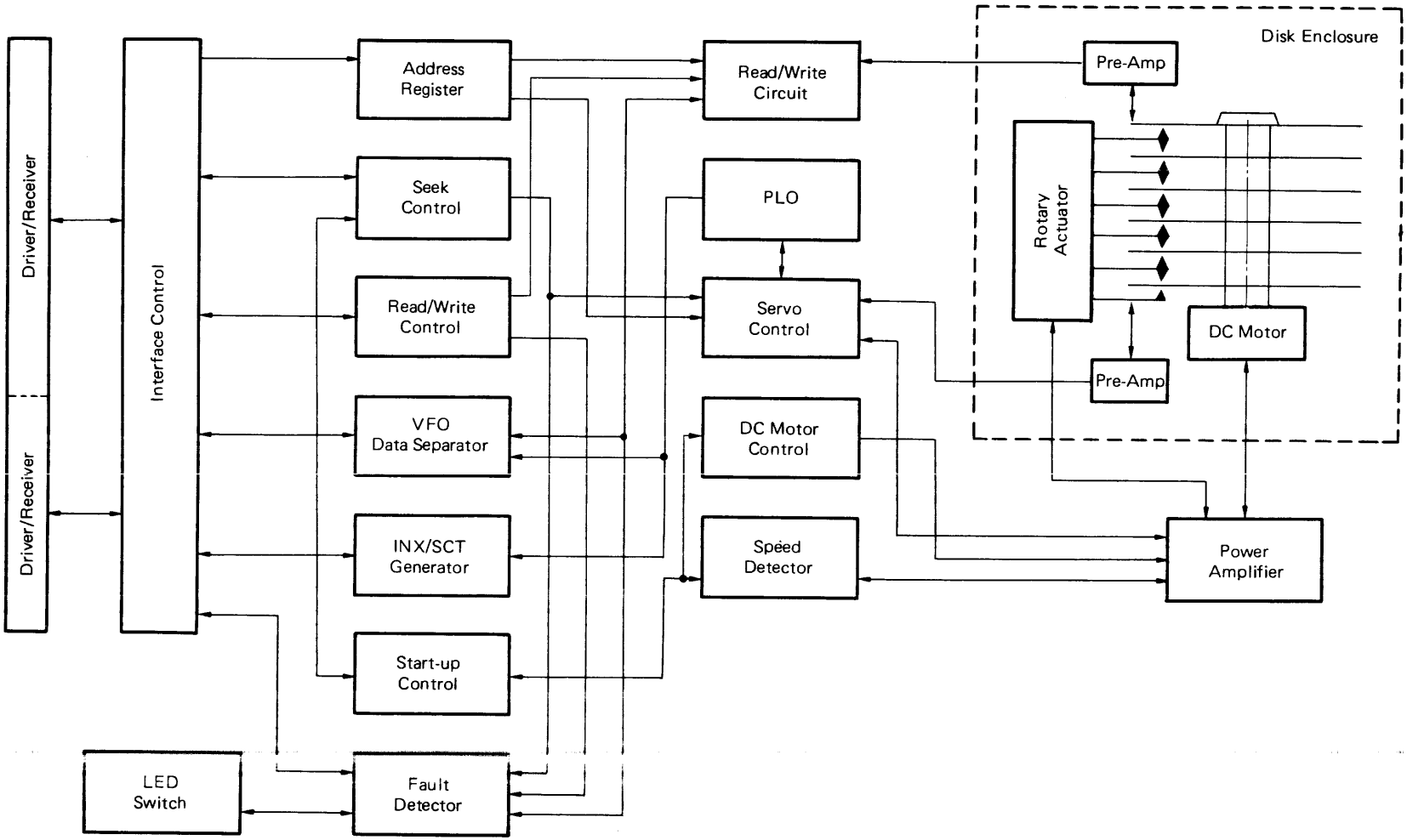


Figure 1-3-2 Block Diagram

1.3.2 Options

Optional items are presented in Table 1-3-1.

Table 1-3-1 Options

Item No.	Component name	Specification (Drawing No.)	Remarks
1-1	Fan unit	B03B-4740-E002A	100/115/120V AC; 50/60 Hz
1-3	Fan unit	B03B-4740-E005A	+24V DC
2-1	Power supply unit	B14L-5105-0100A	· 100/115/120/220/240V AC. · With connectors for feeding power to fan units and dual channel printed board unit.
3-1	Cable	B660-1065-T006A	Interface cable (A) 60P flat cable
3-2	Cable	B660-1065-T008A	Interface cable (B) 26P flat cable
4-1	Panel unit	B03B-4590-E501A	Flat key type control panel board
5	Mounting tray	B21L-1810-0002A	For mounting two units of 19-inch rack with 3 pitches (inside frame), and the front panel has the windows for operating the panel unit.
6-1	Dual Channel	B03B-4740-E401A	To be mounted on optional PSU.
6-2	Dual Channel	B03B-4740-E402A	To be mounted on drive unit.
7-1	Power cable	B660-0625-T327A	Drive unit – power supply unit connecting
7-2	Power cable	B660-1995-T041A	Drive unit and DC (+24V) Fan unit-power supply unit connecting Cable.
8-1	Cable	B660-0625-T328A	E002A fan unit — power supply unit connecting
9-1	Cable	B660-1995-T003A	E501A panel unit — drive unit connecting
10-1	Cable	B660-0625-T329A	Dual channel PCB assy. — Power supply unit connecting

Note: Items in the above table are optional and not fundamental components of this unit. These items must be ordered separately conforming to the above specifications as occasion demands.

1.3.2.1 Fan Unit

The M2321K/M2322K requires some means of cooling, since there is no internal blower motor. For this purpose, optional fan units are available in the event that adequate cooling is not provided within the mounting cabinet. This fan unit is directly mountable onto the rear of the device using the existing screws and taps.

The fan unit may be ordered in the following voltage ratings: 100/115/120V AC or +24V DC. When the input power of the fan unit is supplied from the optional power supply unit, the 100/115/120V AC (B03B-4740-E002A) fan unit should be specified regardless of system AC Voltage.

The DC fan unit (B03B-4740-E005A) may be used with the optional power supply unit. In this case, order power cable specification: B660-1995-T041A.

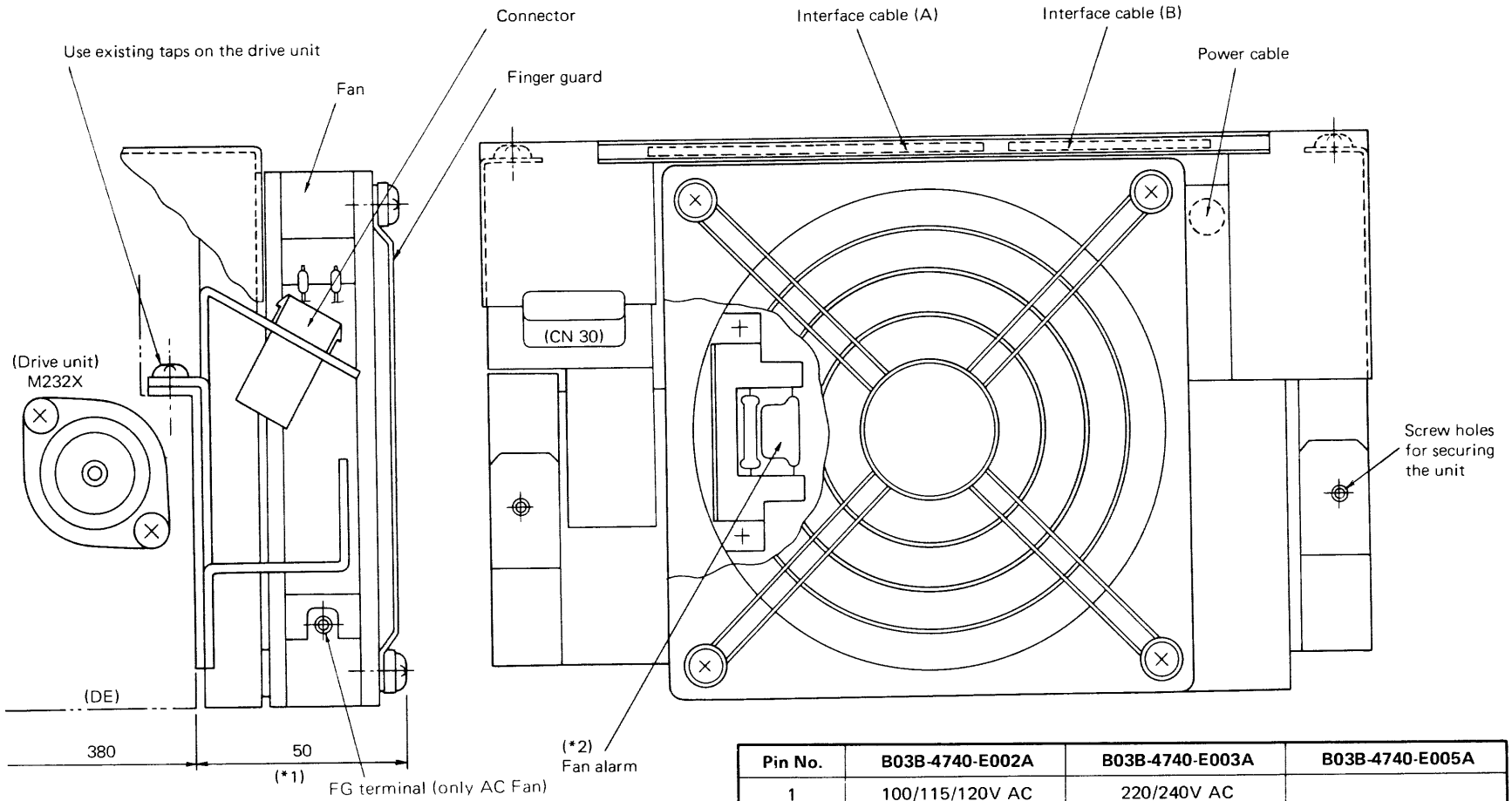
The Table 1-3-2 shows the specifications of fan units.

The Figure 1-3-3 shows the mounting status, of the fan unit.

Table 1-3-2 Specifications of fan units

	B03B-4740-E002A	B03B-4740-E005A
Rated voltage	AC 115V	DC 24V
Frequency	50/60 Hz	–
Ready current		0.5 A or less
50 Hz	0.26A or less (standard : 0.18A)	
60 Hz	0.20A or less (standard: 0.12A)	
Starting current		0.72 A or less
50 Hz	0.27A or less	
60 Hz	0.21A or less	
Consumption		15W or less
50 Hz	27W or less	
60 Hz	19W or less	
Phase/Pole	Single/2P	–
Environmental condition	Same as of unit	Same as left
Thermal alarm	Blow-value detecting method alarm	Blow-value detecting method alarm
Motor protection	Impedance protect	–
Weight	1 kg or less	1 kg or less

Note: Values of voltage and current show in case of no-load state.



*1: The overall length after mounting the fan unit is 430 mm (380 mm + 50 mm).

*2: Fan alarm specification

Type of contact point:	Normal open
Contact capacity:	0.5A DC max. 200V DC max. * However, I (A) x E (V) < 10W DC
Consumption:	4.2W (at 100V AC or 24V-DC)
Responce time:	5 – 300 sec.
Circuit:	See Figure 1-3-4

Pin No.	B03B-4740-E002A	B03B-4740-E003A	B03B-4740-E005A
1	100/115/120V AC	220/240V AC	
2	100/115/120V AC		
3	FG	FG	+24V Return
4		220/240V AC	+ 24V DC
5	ALARM (*2)		ALARM (*2)
6	ALARM (*2)		ALARM (*2)

Figure 1-3-3 Fan Unit

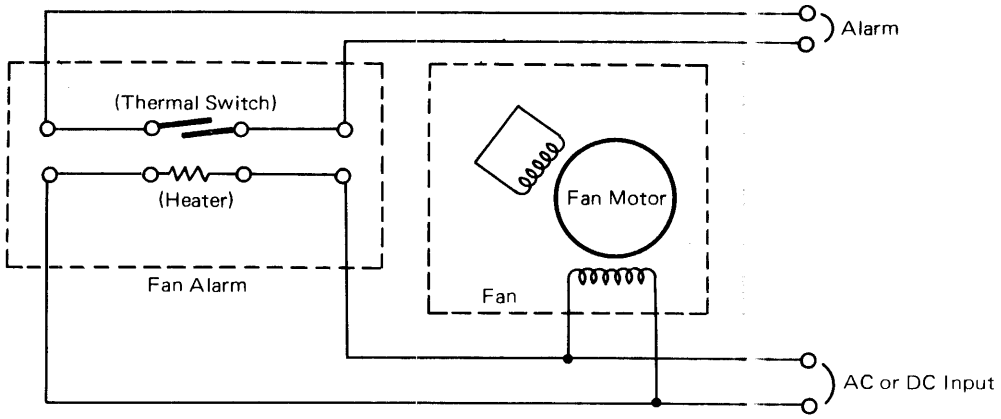


Figure 1-3-4 Optional Fan Unit Alarm

1.3.2.2 Power Supply Unit

A power supply unit may either be mounted horizontally behind the disk drive or may be mounted vertically. Figure 1-3-5 shows the details of I/O terminals and the external dimensions of the power supply unit.

Specification: B14L-5105-0100A

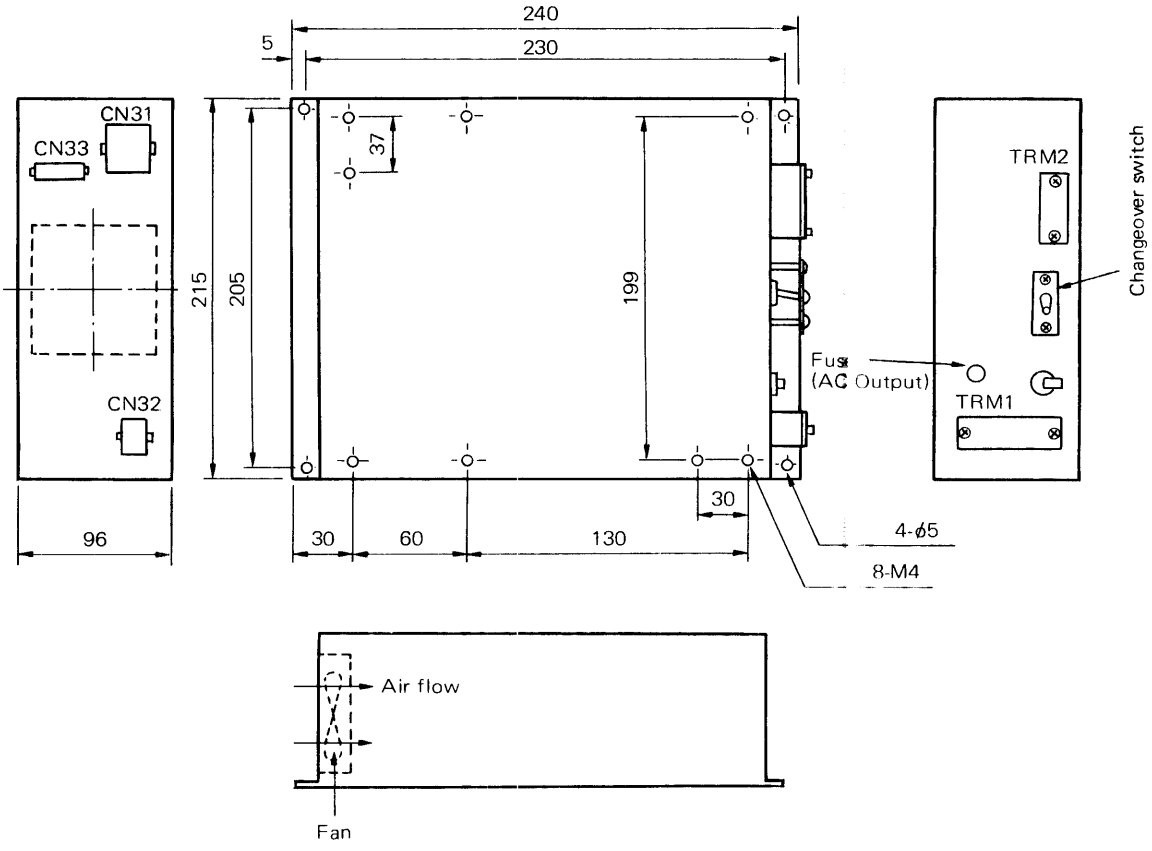


Figure 1-3-5 Power Supply Unit

TRM1: AC power input and alarm sending.
TRM2: FG-SG coupling terminal. (Normally open)
CN31: Drive unit power feeding connector
(for cable B660-0625-T327A (Option))
CN32: Fan unit power feeding connector
(for cable B660-0625-T328A/T355A (Option))
CN33: Dual channel PCB unit power feeding connector
(for cable B660-0625-T329A (Option))

AC input voltage selection from 100/115/120V AC to 220/240V AC is switch selectable.

Regardless of AC input voltage, AC output voltage from CN2 (AC fan unit power supplying connector) is kept 115V $^{+15\%}_{-24\%}$ AC.

Therefore when using the optional power supply only the 115V AC fan is required.

1.3.2.3 Panel Unit

The panel unit includes function lights which indicate power on, ready, write protect, check, and also includes a write protect switch and a check clear switch.

Figure 1-3-6 shows the mounting dimensions and mounting status of panel unit B03B-4590-E501A.

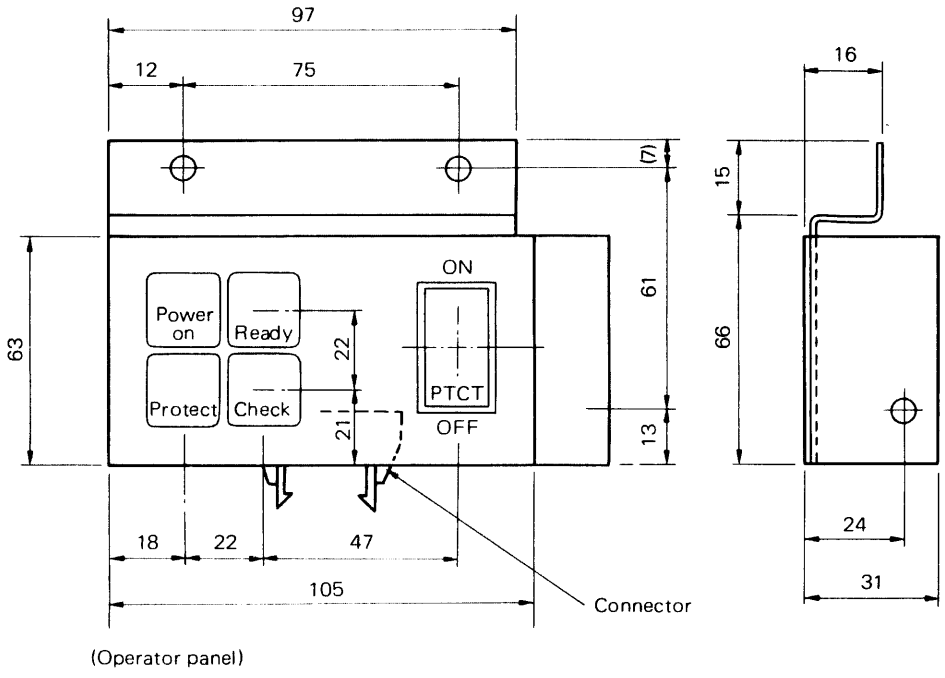


Figure 1-3-6 Panel Unit

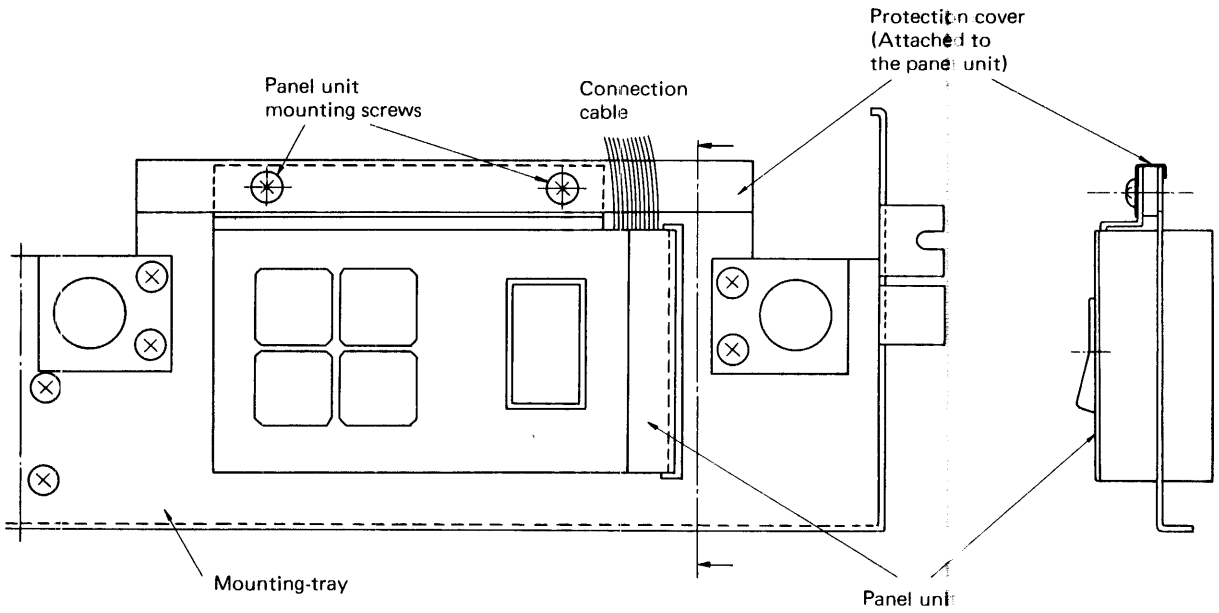


Figure 1-3-7 Mounting of Panel Unit on Optional Rack Mount Kit

1.3.2.4 19'' Rack Mount Installation

A mounting-tray with brackets is available to install two drives, side by side in a 19'' rack, three pitches. It can also accommodate the optional fan units and/or power supply units for each of the two drives.

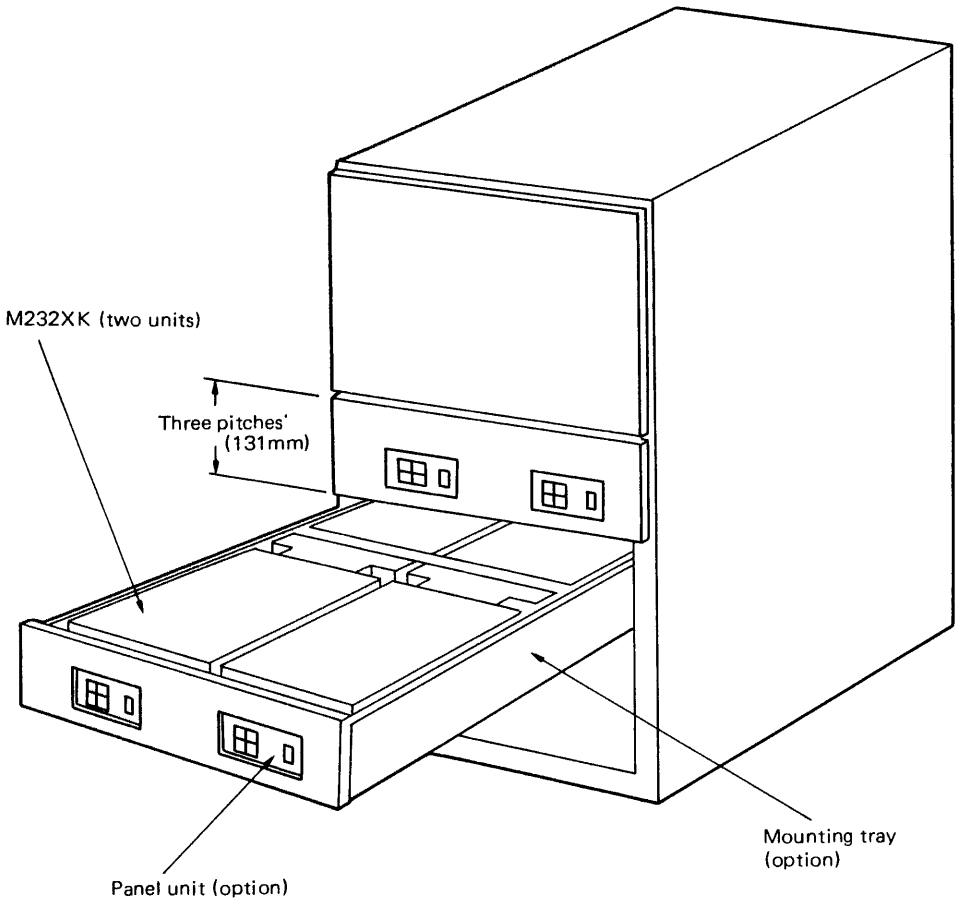
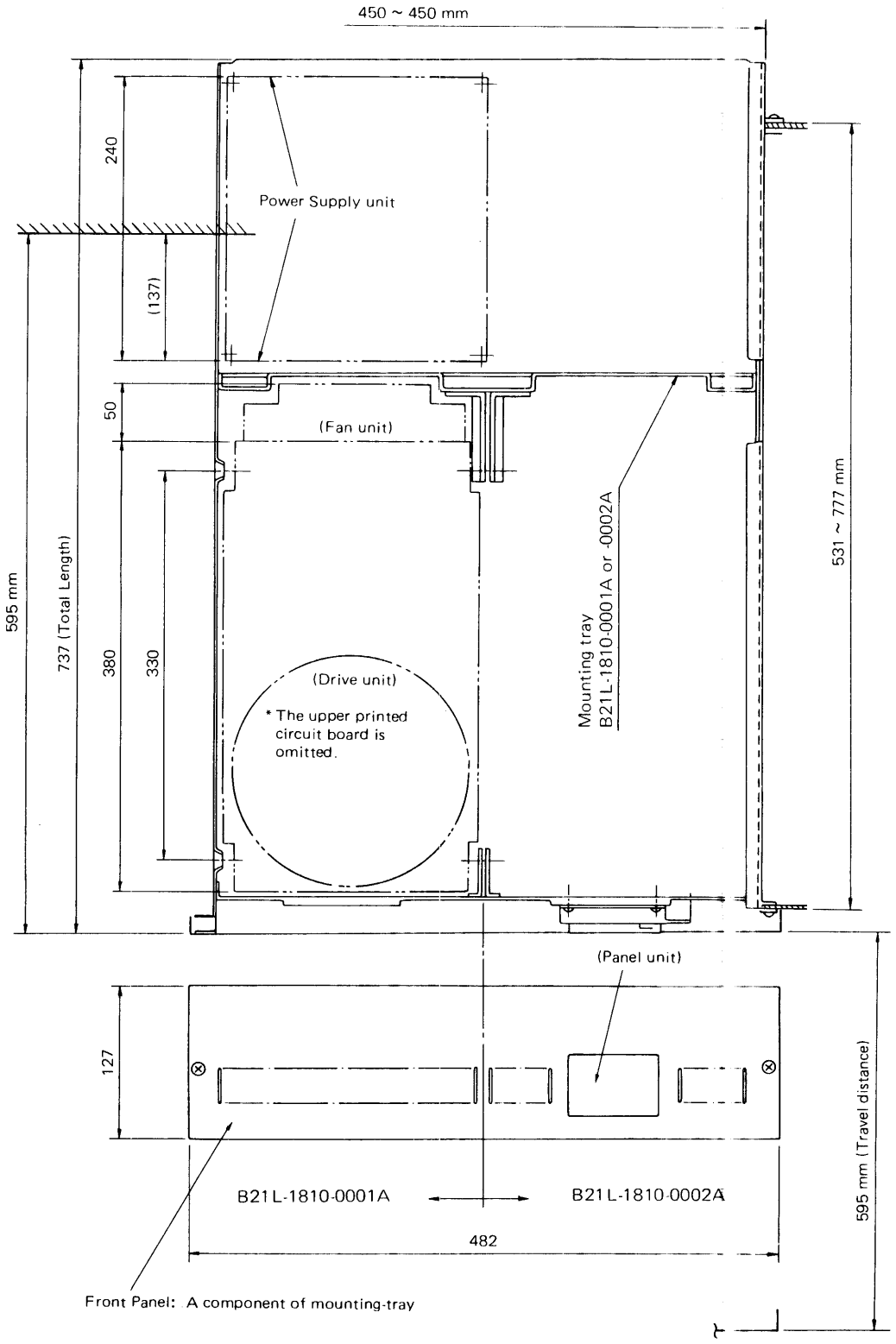


Figure 1-3-8 19'' Rack Mount Installation

The mounting-tray (inner frame) guided by brackets (outer frame) can be drawn out forward. (Travel distance is approximately 24'').
The 19'' rack mounting method is illustrated in Figure 1-3-8. And Figure 1-3-9 shows the appearance when the units are mounted using the mounting-tray and brackets.



Note: Mounting-tray (0001A) cannot accommodate the drive unit with Panel unit. In that case, 0002-type must be specified.

Figure 1-3-9 Mounting-Tray and Brackets

1.3.2.5 Cables

The inteface cable (A) may be up to 30 m long (to the final unit in case of daisy chain mode).

The interface cable (B) may be up to 15 m long.

NOTE: Contact local FAI Sales Office for Cable lengths.

How to specify cable lengths

(For 3.5m: Example 1)

B660-1065-T008A #L3R503
Cable specification 3.5×10^3 (mm)

(For 50cm: Example 2)

B660-0625-T327A #L500R0
Cable specification 500×10^0 (mm)

The lengths of cables at Items 7, 8, 9 and 10 in Table 1-3-1 must also be specified.

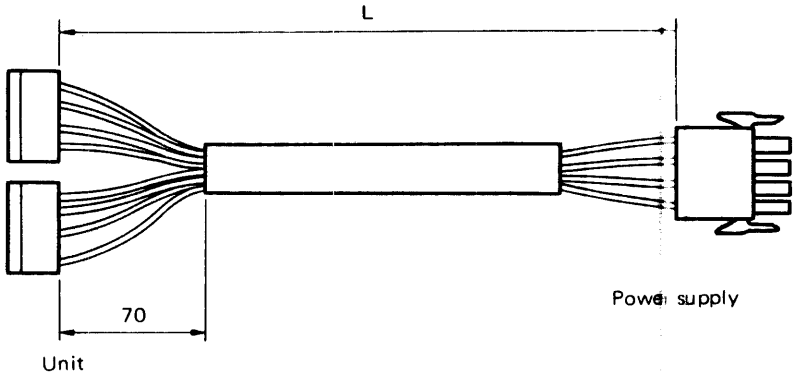


Figure 1-3-11 Power Cable (When A.C. fan or no fan is used) B660-0625-T327A

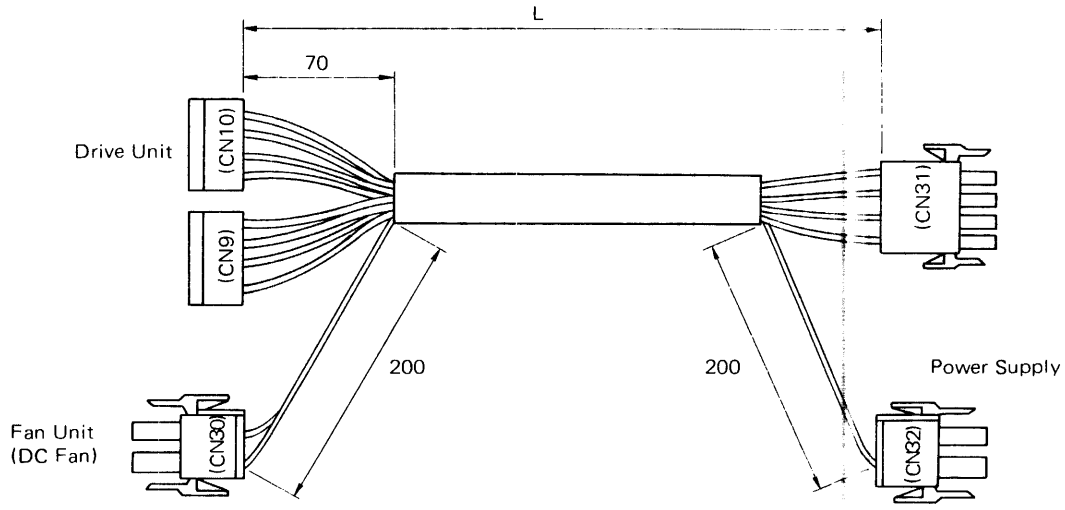


Figure 1-3-12 Power Cable (When using D.C. fan option) B660-1995-T001A

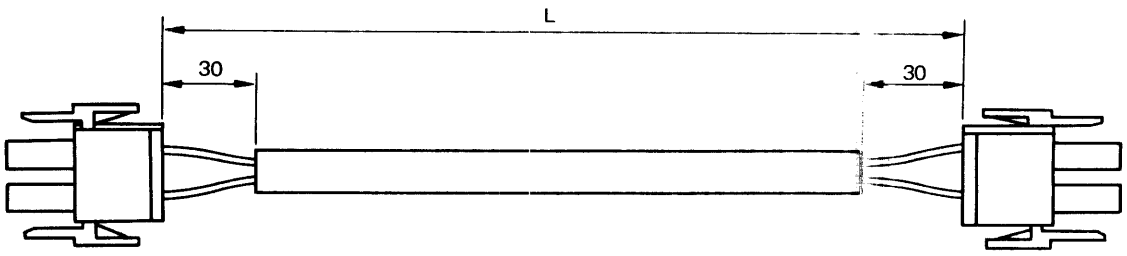


Figure 1-3-13 Cable B660-0625-T328A, T355A
(A.C. Fan unit - Power supply unit)

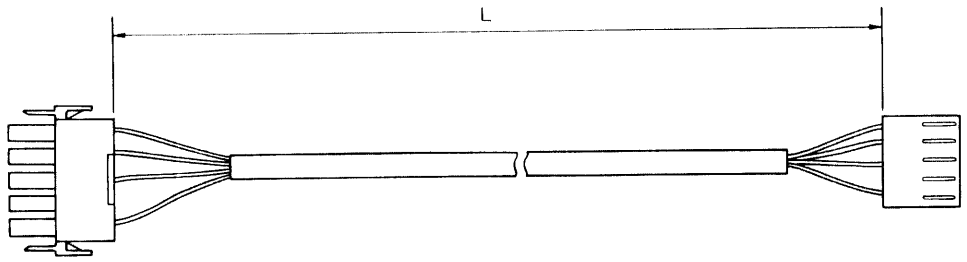


Figure 1-3-14 Cable B660-0625-T329A
(Dual Channel PCB assy. – Power supply unit)

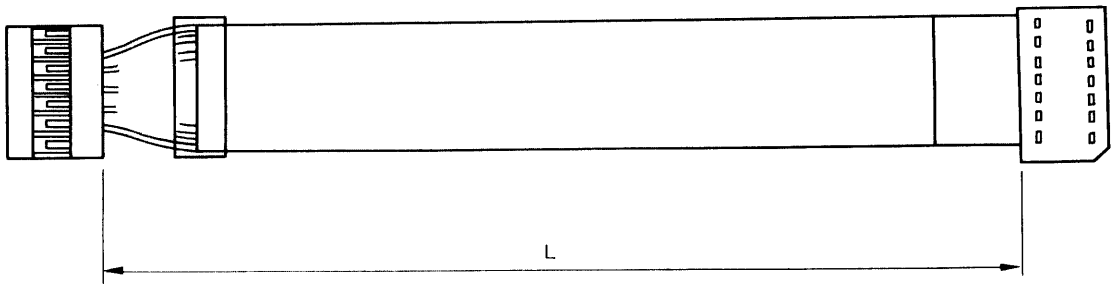


Figure 1-3-15 Cable B660-1995-T003A
(E501A Panel unit – Drive unit connecting)

The length of this cable can be specified in 60 mm increments (Minimum length is 90 mm.)

Operator Panel Connection

The CZFM PCB allows for connection of an optional control panel. At location B30 on this PCB, there is a 14 pin DIP socket for the control panel connection. Following is pin-out for this DIP socket.

PIN NUMBER	SIGNAL MNEMONIC	DEFINITION
1	+5V	+5 Volt
2	*FPTK	File Protect Switch
3	*CKCLR	Check Clear Switch
4	*LRDY	Ready LED
5	0V	Signal Ground
6	*LUSLD	Unit Selected LED
7	0V	Signal Ground
8	0V	Signal Ground
9	*PWRDY	Power Ready LED
10	*LFPT	File Protect LED
11	*LDVCK	Device Check LED
12	0V	Signal Ground
13	0V	Signal Ground
14	+5V	+5 Volt

"*" Indicates a low active signal.

1.3.2.6 Dual Channel PCB Assembly

This unit can be provided with a dual channel option to add the crosscall function. Versions are available which permit the mounting of this option on the drive or the power supply.

Drive's height is:

- In case of mounting on the unit; 154mm
- In case of mounting on the power supply; 123 mm
  It is possible to be mounted in the 19-inch rack with 3-pitch by using the optional power supply (B14L-5105-0100A), the mounting-tray (B21L-1810-0001A or 0002A).

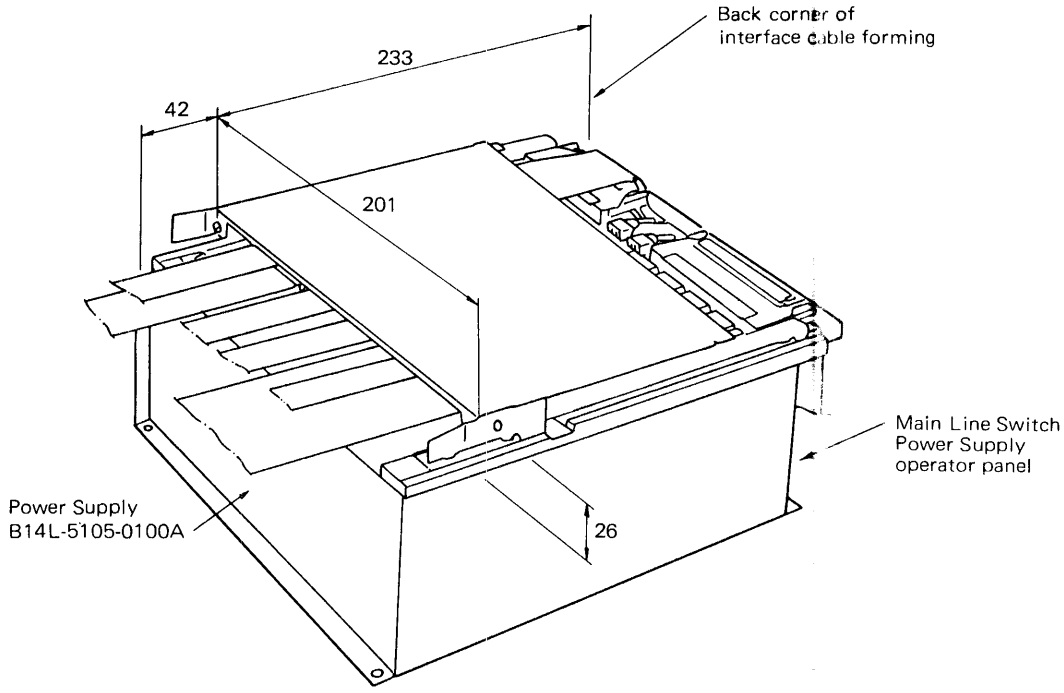
The specifications and the rating of dual channel option are shown in Table 1-3-3.

Table 1-3-3 Dual Channel Option

Specifications	B03B-4740-E401A	B03B-4740-E402A
Mounting location	On the power supply	On the unit
Input condition	+5V, 4.5A −12V, 4.0A (Including the basic drive)	

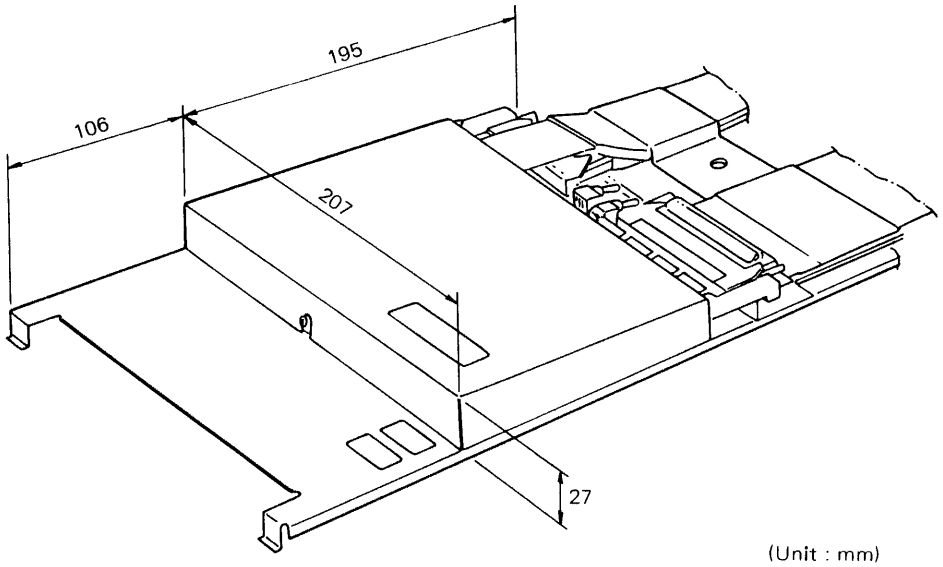
Note: The dual channel option is connected with optional power supply by using the connecting cable. (See Item 1.3.2.5)

Dimensions after mounting of Dual channel PCB Assembly are shown in Figure 1-3-16 (E401A) or Figure 1-3-17 (E402A).



Note: In case of mounting on the power supply, fix Brackets with screws on the power supply.

Figure 1-3-16 Dual Channel Option (E401A)



(Unit : mm)

Note: In case of mounting on the unit, change the usual unit cover to the cover for this option.

Figure 1-3-17 Dual Channel Option (E402A)

Connector location on the PCB are shown in Figure 1-3-18.

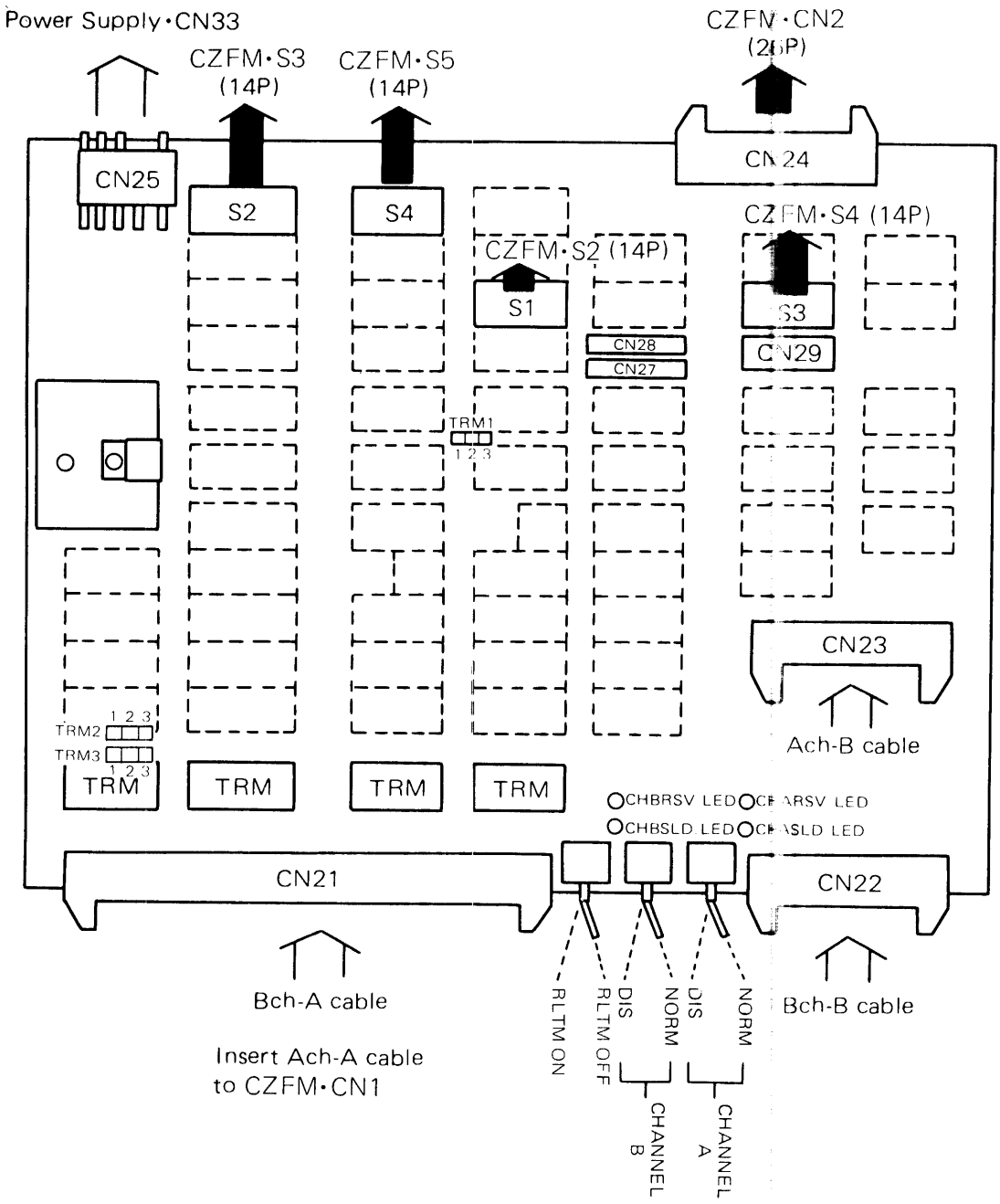


Figure 1-3-18 Dual Channel PCB Assembly Connector Location

Section 2

Operation

2. OPERATION

2.1 GENERAL DESCRIPTION

Two M232X Micro disk Drives can be horizontally mounted in a 19 inch rack with the optional mounting tray. The M232X may also be built into a system cabinet and mounted horizontally, vertically or on-end.

The CZFM Printed-Circuit-Board Assembly in the M232X Micro Disk Drive is equipped with Maintenance Aid LED's and a File Protect switch.

Powering up/down and the functions of the internal indicators (LED) and switches will be described in this section. The functions of the LED's and switches on the optional operator panel will also be described.

2.2 POWERING UP/DOWN

The M232X Micro Disk Drive is not equipped with a power ON/OFF switch. Powering up/down of the M232XK typically performed by powering up/down the system.

When the disk unit is equipped with an optional power supply, powering up/down may be performed by turning the power switch ON and OFF at the power supply.

2.3 CONTROL AND INDICATORS

2.3.1 Operator Panel (option)

The functions of the LED's and switches or optional operator panel (front panel) is described below.

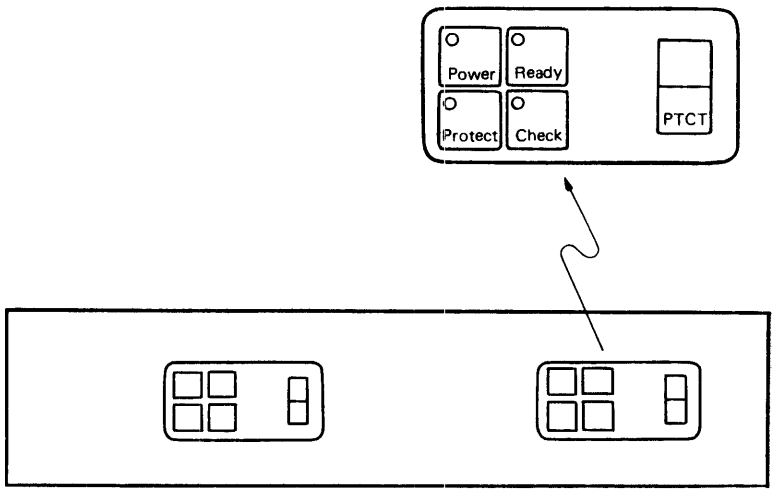


Fig. 2-3-1 Operator Panel (Optional)

(1) Power indicator: Red
This LED lights when the power is turned on.
(2) Ready indicator: Red
This LED indicates that the initial seek has performed or indicates the termination of a Seek or RTZ operation.
(3) Check indicator: Red
This LED indicates any fault condition.
(4) Protect indicator: Red
This LED indicates that writing is inhibited.
(5) Protect (PTCT) switch: White
This key inhibits the write operation.
(6) Check clear switch: Gray (flat key)
This key resets a Device Check status.

2.3.2 PCB Assembly

The unit contains fault display indicators (LED's) as shown in Figure 2-3-2. these are location on CZFM PCB.

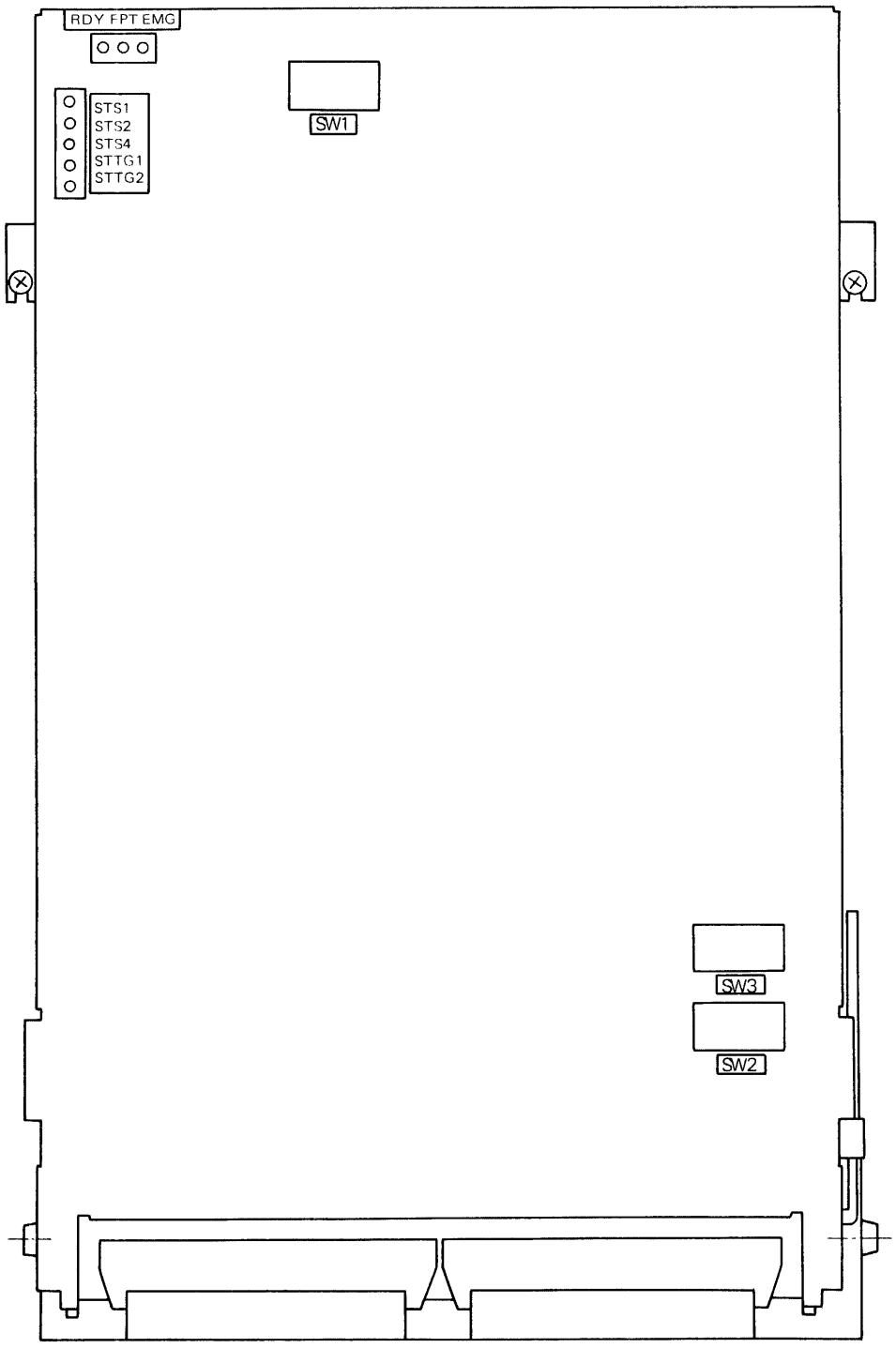


Figure 2-3-2 Fault Display Location on CZFM PCB

(1) RDY (Ready) indicator: Green
This RDY LED indicated that the initial seek has been performed or indicates the termination of a Seek or RTZ operation.
(2) FPT (File Protect) indicator: Orange
This LED indicates that writing is inhibited.
(3) EMG (Emergency Retract) indicator : Red
This LED indicates DC Motor Fault (DMFT) or VCM Heat (VCMHT) condition.
DMFT condition ——— This LED is blinks on and off
VCMHT condition ——— This LED is turned on
(4) STS1 to 4, STTG1 and STTG2 (Status and Status Tag): Red
The two-bit binary coded Status Tag 1 and 2 LED's have the following conditions.

Status Tag 2	Status Tag 1		Condition
0	0	:	Not Ready (Under the power-up sequence)
0	0 ⇄ 1	:	Not Ready (Power-up Sequence Check)
0	1	:	Fault
1	0	:	Seek Error
1	1	:	Normal Status

The Status Tag 00 has the highest priority and Status Tag 11 has the lowest priority.

Status 1, 2 and 4 LED's are defined by the above Status Tag LED's as shown in Table 2-3-1.

Table 2-3-1 Fault Indicator

Status	Status Tag		Status Bit			Code (Hex)	Fault or Normal Status	
	2	1	4	2	1		Designation	Condition
Not Ready	0	0	0	0	0	00	State 0	Power-on Reset Sequence.
			0	0	1	01	State 1	+24V Supply Sequence.
			0	1	1	03	State 3	Auto-lock Release Sequence.
			0	1	0	02	State 2	DC Motor Accelerate Sequence.
			1	1	0	06	State 6	Accelerate Complete Sequence.
			1	1	1	07	State 7	Initial Seek Sequence.
			1	0	1	05	State 5	Ready state but this state is not indicated.
Not Ready (Powerup Sequence Check)	0	0 ↓↑ 1	0	0	1	0X	State 1	Indicates the condition to power up is not correct.
			0	1	1	0X	State 3	Indicates the actuator lock is not released.
			0	1	0	0X	State 2	Indicates the rotational speed is not to 94% (nominal) within the specified time.
			1	1	0	0X	State 6	Indicates the accelertion mode is not terminated within the specified time.
			1	1	1	0X	State 7	Indicates the intial seek is not terminated within the specified time or is terminated incompletely.
			1	0	1	0X	State 5	Indicates an abnormal current flows to winding of VCM or DC motor.

Table 2-3-1 Fault Indicator (Continued)

Status	Status Tag		Status Bit			Code (Hex)	Fault or Normal Status	
	2	1	4	2	1		Designation	Condition
Fault	0	1	0	0	1	09	Control Check 1	Indicates a read/write command is issued during a busy condition.
			0	1	0	0A	Control Check 2	Indicates a write command is issued during a fault/check condition.
			0	1	1	0B	Write off-track	Indicates an off-track condition occurs during write operation.
			1	0	0	0C	Write Unsafe	Indicates a write operation cannot be performed due to a write circuit fault.
			1	0	1	0D	Write Protected	Indicates a write command is issued during File-protected status.
			1	1	0	0E	Read/Write Multi	Indicates multiple heads are selected during a read or write operation.
			1	1	1	0F	Emergency	Indicates over-load current flows on VCM or DC Motor.
Seek Error	1	0	0	0	1	11	RTZ Time-out	Indicates an RTZ operation is not terminated within the specified time.
			0	1	0	12	Seek Time-out	Indicates a Seek operation is not terminated within the specified time.
			0	1	1	13	Over-shoot	Indicates the head Over-shoots the target cylinder during settling time, or the head moves out during track following sequence in linear mode.
			1	0	0	14	Seek Guard Band	Indicates the guard band is detected during seek operation.
			1	0	1	15	Linear Mode Guard Band	Indicates the guard band is detected during linear mode.
			1	1	0	16	RTZ Outer Guard Band	Indicates the outer guard band is detected during RTZ operation.
			1	1	1	17	Illegal Cylinder	Indicates an illegal cylinder address (>822) is issued by the controller.
Normal Status	1	1	0	0	1	19	Selected	Indicates the drive is selected by the controller.
			0	1	0	1A	Tag 4/5 Enabled	Indicates the optional tag 4/5 function is enabled by the key on the drive.
			1	0	0	1C	Hard Sector Mode	Indicates the sector mode is set to Hard Sector by the key on the drive.

2.4 Dual Channel PCB Assembly (Option)

Dual channel PCB assembly is shown in Figure 2-4-1.

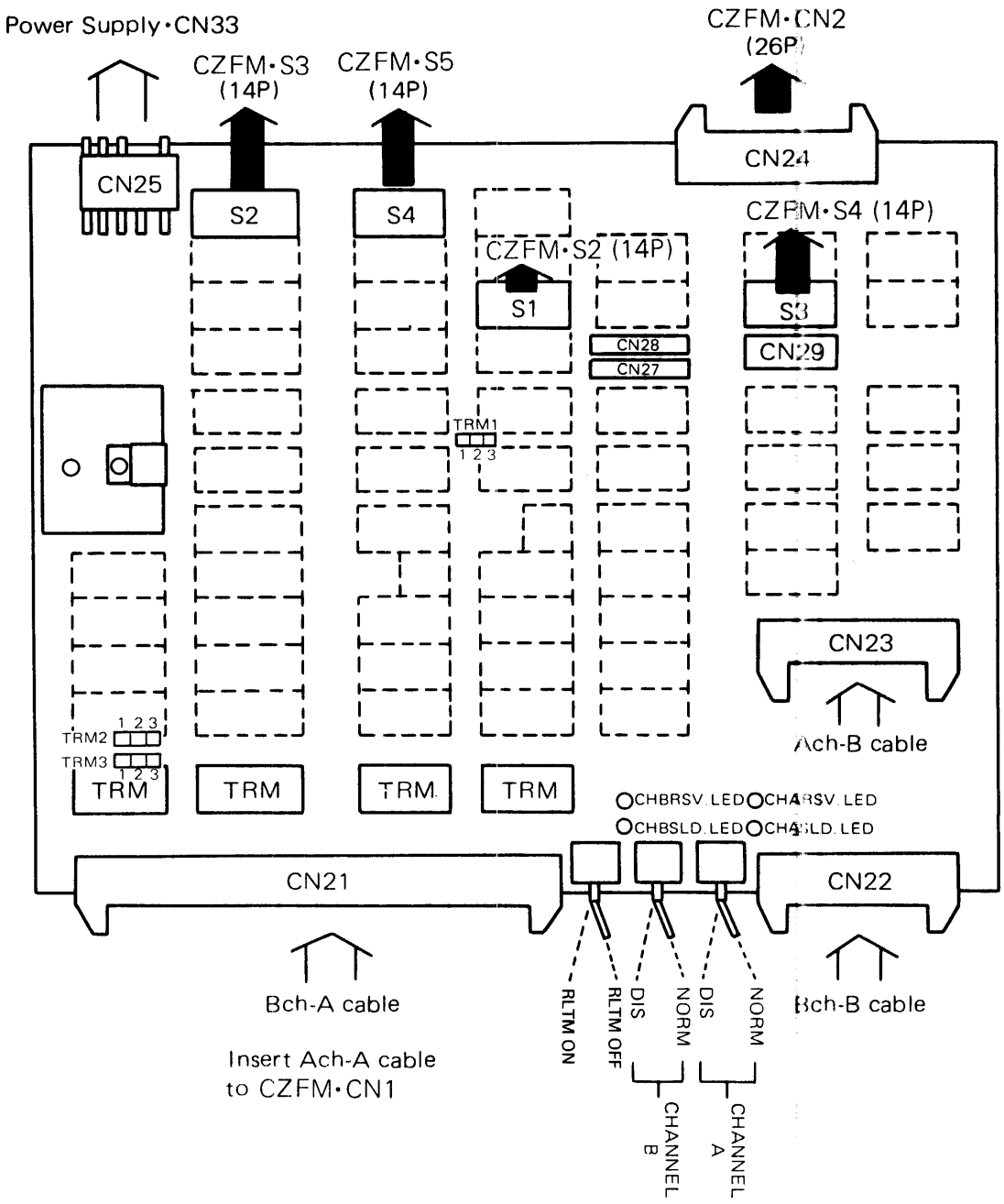


Figure 2-4-1 Dual Channel PCB Assembly

(1) CHASLD LED (green)
Indicates that this unit is Selected by the Channel-A controller.

(2) CHARSV LED (orange)
Indicates that this unit is Reserved by the Channel-A controller.

(3) CHBSLD LED (green)
Indicates that this unit is Selected by the Channel-B controller.

(4) CHBRSV LED (orange)
Indicates that this unit is Reserved by the Channel-B controller.

(5) CH-A Switch

DIS (Disable A): Disconnects the unit from the Channel-A controller and disables it from sending and recieving all interface signals.

NORM (Normal A): Connects the unit to the Channel-A controller and enables it to send and receive interface signals.

(6) CH-B Switch

DIS (Disable B): Disconnects the unit from the Channel-B controller and disables it from sending and receiving all interface signals.

NORM (Normal B): Connects the unit to the Channel-B controller and enables it to send and receive interface signals.

(7) RLTM Switch

RLTM ON: When in "Release Timer On", Reserved and Priority Select are released 500 ms (nominal) after the unit is deselected.

Note: Reserved and Priority Select can also be released by the Release Command (TAG 3, BUS 9).

RLTM OFF: When in "Release Timer Off", the Reserved condition is released from the controller by the Release Command (TAG 3, BUS 9).

2.5 POWER SUPPLY

2.5.1 General

This manual describes the installation, operation and maintenance of the optional Power Supply. The power supply is designed to provide the power required by the Model M231XK/M232XK Microdisk Drives. Circuit configuration and component values were selected to accomodate the dynamic load presented by these drives. Adequate derating of components and quality workmanship have been used throughout the design and manufacture of this power supply to gain maximum reliability and operating life. Reliability and long life are also assured through the use of an internal cooling fan.

The power supply operates from a primary power source of 100V AC at 50/60 Hz, 115V AC at 60Hz, 120V AC at 60 Hz, 220V AC at 50 Hz, and 240V AC at 50 Hz. Line voltage and frequency variations of $^{+10\%}_{-12\%}$ respectively, can be tolerated without degradation of power supply performance.

All output voltages are available on the back of the power supply at connectors CN31, CN32 and CN33 as described in Table 3.1.

Combined static and dynamic output voltage variation on all regulated outputs does not exceed ±5% under worst case conditions of temperature, input voltage, frequency and load. The AC input line is protected by a circuit breaker (NFB1).

The +5V DC circuit has an over-voltage protection feature which operates if the output voltage exceeds 25% of nominal. The +5V, +24V and —12V DC circuits have over current protection which will reduce the output voltages. The 115V AC circuit for the power supply and disk drive fan is protected by a 250V AC, 1.25A Fuse. Alarm circuits are provided to indicate power supply or device malfunction. These alarm circuits are described in Sections 2.3, 2.4, 4.6 and 4.7.

2.5.2 Power Supply Specifications

Table 1.1 shows the specifications for the Power Supply. The specifications are for operation at rated load unless otherwise indicated.

Table 2.5.1 Power Supply Specifications

Parameter	Specifications
Input Voltage	100V AC $^{+10\%}_{-12\%}$ 50/60 Hz $^{+2\%}_{-4\%}$, 115V AC $^{+10\%}_{-12\%}$ 60 Hz $^{+2\%}_{-4\%}$
	120V AC $^{+10\%}_{-12\%}$ 60 Hz $^{+2\%}_{-4\%}$, 220V AC $^{+10\%}_{-12\%}$ 50 Hz $^{+2\%}_{-4\%}$
	240V AC $^{+10\%}_{-12\%}$ 50 Hz $^{+2\%}_{-4\%}$,
Input Current	3.5A (100V AC), 3.3A (115V AC)
	3.2A (120V AC), 1.8A (220V AC)
	1.7A (240V AC)
Rated Output	+5V DC ±5%, 4.8A
Current	+24V DC ±10% (when +5V DC is nominal), 4.2A
	—12V DC ±5% (when +5V DC is nominal), 4.0A
	115V AC $^{+15\%}_{-24\%}$ 0.3A
Output:	
Nominal Output/	+5V DC/Adj ±10% (When the Input Voltage is more than 95V)
Adjustment Range	+24 Unregulated or
	—12V Unregulated
Ripple Voltage	+5V 50mV P-P
	+24V Unregulated 1.8V P-P, or
	—12V Unregulated 400mV P-P
Peak Current	+5V DC 4.8A —24V DC 7.7A —12V DC 4A
Protection:	
AC Input Lines	7.5A Circuit Breaker
DC Output Lines	+5V, +24V, —12V Over-current protection circuit
AC Output Lines	115V 1.25A Fuse
Environment:	
Operating Ambient	0 °C to 50 °C
Relative Humidity	20% to 85% (Operating)
	8% to 90% (Storage)
Physical:	
Height	96 mm
Width	215 mm
Depth	240 mm
Weight	5.5 Kg

2.5.3 Outer View

The outer view of this power supply unit is shown in Figure 2.5.1

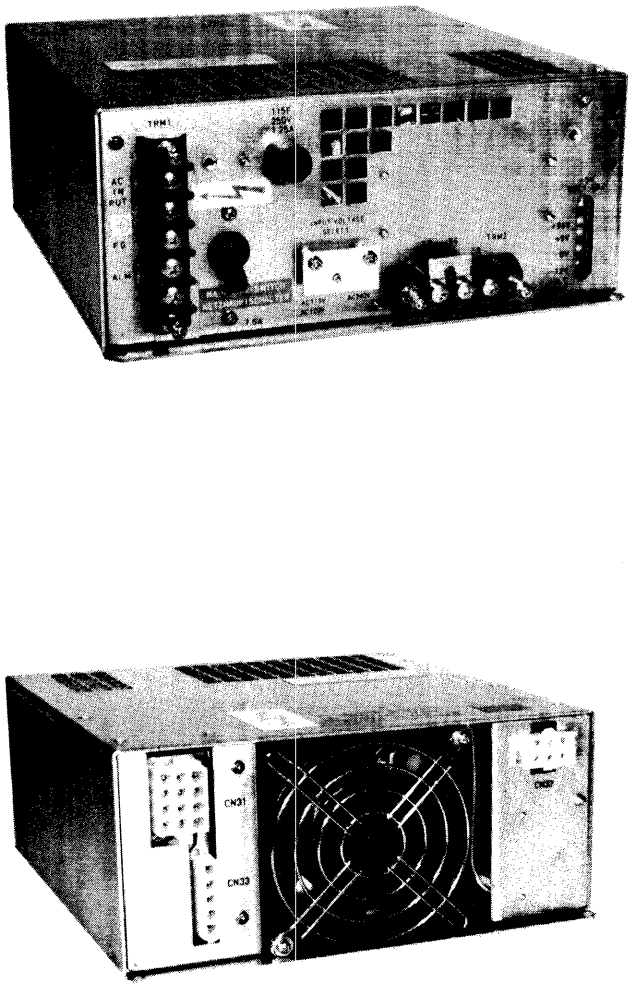


Figure 2.5.1 Outer View

2.5.4 OPERATION

2.5.4.1 General

The switches, alarm lamp, and the device alarm lamp of the power supply unit are described in this section.

2.5.4.2 Main Line Switch (NFB1)

This switch controls application of AC power to the power supply unit. It also serves as the AC input circuit breaker and is located at the front of the power supply.

2.5.4.3 Power Alarm Lamp

Power Alarm Lamp indicates one of the following power malfunctions has occured on the power supply unit.

(a) +5V DC; Over-current, High-voltage and Low-voltage, No voltage.

(b) −12V DC; Over-current and Low voltage.

(c) +24V; Over-current and Low-voltage.

(d) AC input; Over-current and Circuit Protector.

(e) AC output; Fuse blown.

2.5.4.4 Device Alarm Lamp

Device Alarm Lamp indicates that the Thermal-switch on the M2311/12 fan has closed due to over-heating. The Device Alarm circuitry shuts off the DC voltage to the disk drive to prevent possible damage.

Section 3

Installation

3. INSTALLATION

3.1 GENERAL DESCRIPTION

This section describes unpacking, installation, and cabling of the M232XK when shipped separately, and shipping precautions when the unit is delivered as a system.

3.2 UNPACKING

The M232XK is wrapped in a polyethylene bag, surrounded by cushions, and packed in a carton. An exterior view of the carton is shown in Figure. 3-2-1.

(1) Store and open the carton on a flat surface. Ensure that the top of the box, indicated by a "This Side Up" signs, is oriented correctly, and take out options.
Note: Don't store the disk drive in the upside-down position.

(2) Take out the top cushion.

(3) Pull the M232XK out of the box by grasping its base.
Move the unit slowly and carefully, to prevent unnecessary shock.

(4) Store packing material for possible future use.
Note: When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for more than 3 hours prior to unpacking to avoid condensation.

Caution: To avoid handling damage due to shock when unpacking, don't place the M232XK directly on a bare floor. Place it on a suitable cushioning material.

3.3 VISUAL INSPECTION

After unpacking, check the following.

(1) There should be no cracks, rust or other damage that mars appearance and integrity.

(2) All parts should be firmly fixed, there should be no loose screws, etc.

(3) The attachments and options should be as ordered.

3.4 INSTALLATION

This unit may be mounted in a 19-inch rack or built into a system cabinet.
If mounting the M232XK in a standard 19-inch rack, the mounting tray and its brackets are provided (as options). When the M232XK is built into a system cabinet, it can be mounted horizontally, vertically or on-end. (Refer to Figure 3-4-1.)

3.4.1 Mounting Dimensions

Figure 3-4-2 shows the M232XK dimensions and the structure of its frame.

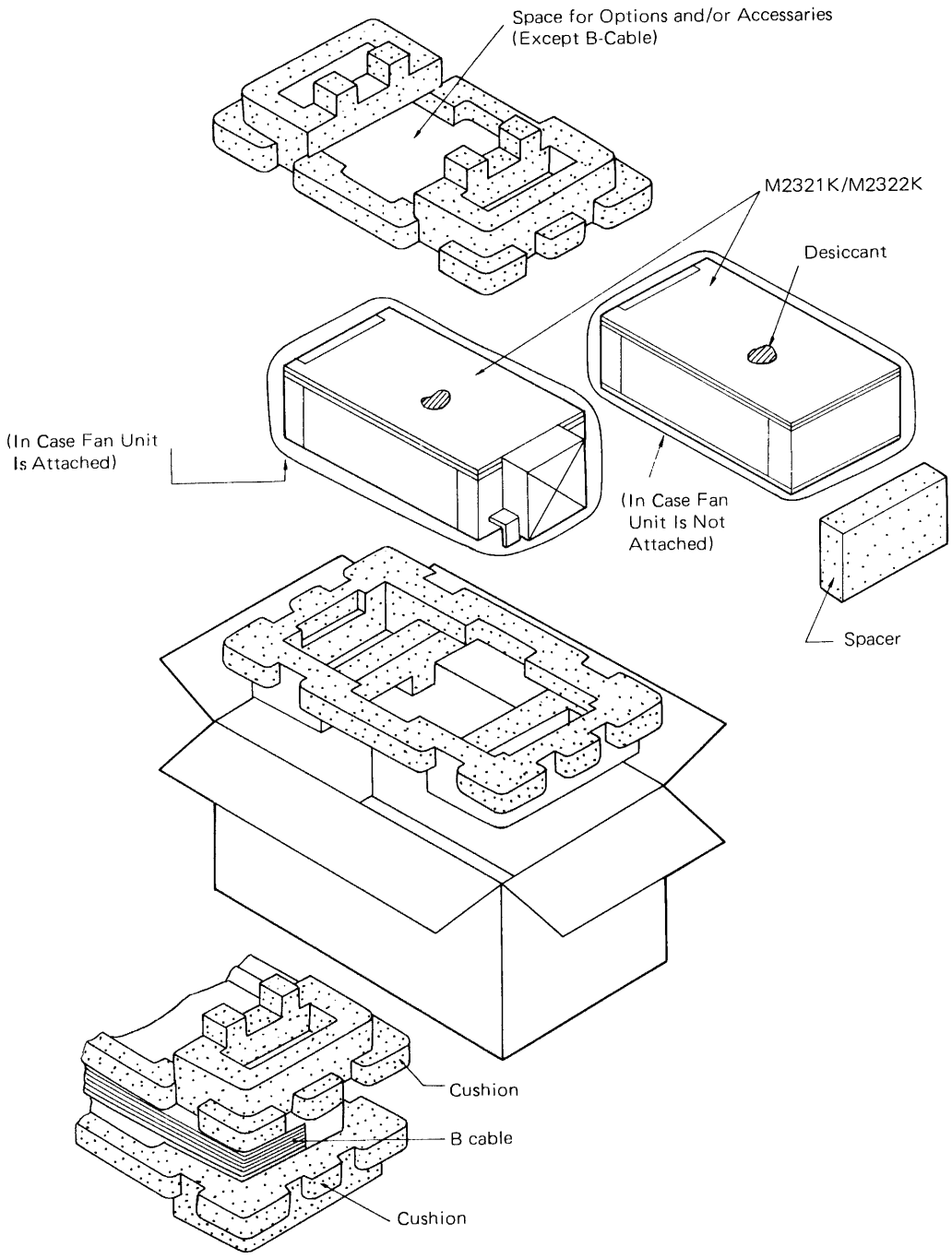
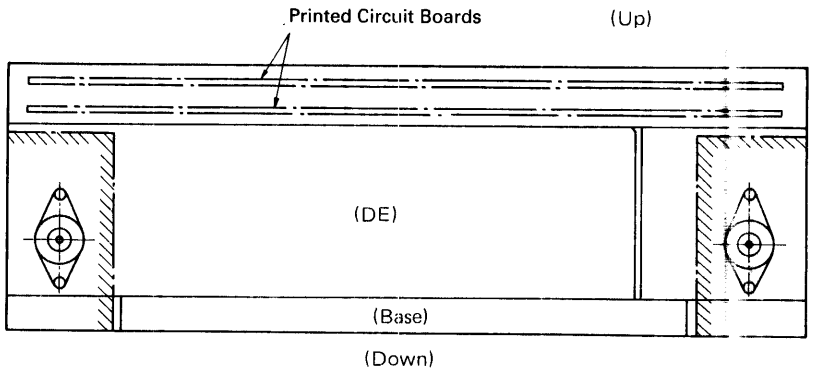
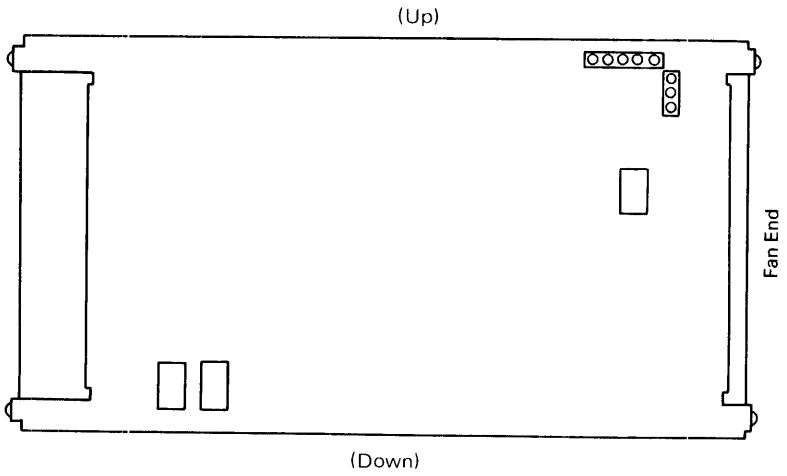


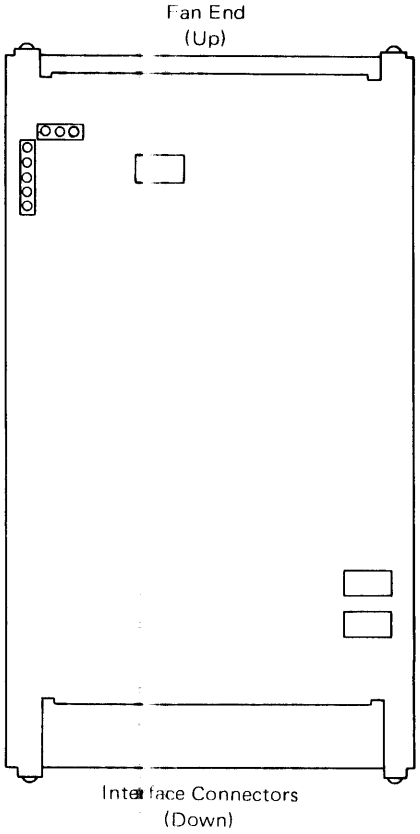
Figure 3-2-1 External View of Carton



(a) HORIZONTAL MOUNTING



(b) VERTICAL MOUNTING



(c) ON-END MOUNTING

NOTE:
This drive maybe mounted in the following orientations only:

1. Horizontally (a) — PCA boards up.
   Key 8 of SW1 in the 'OFF' position
2. Vertically (b) — On the left side of the unit as viewed from the fan end of the drive. Key 8 of SW1 in the 'OFF' position.
3. ON-END (c) — The front of the drive down and the fan (TVQM) end up. Key 8 of SW1 in the 'ON' position.

Any position other than these is not acceptable and may cause unreliable drive operation.

Figure 3-4-1 Mounting direction

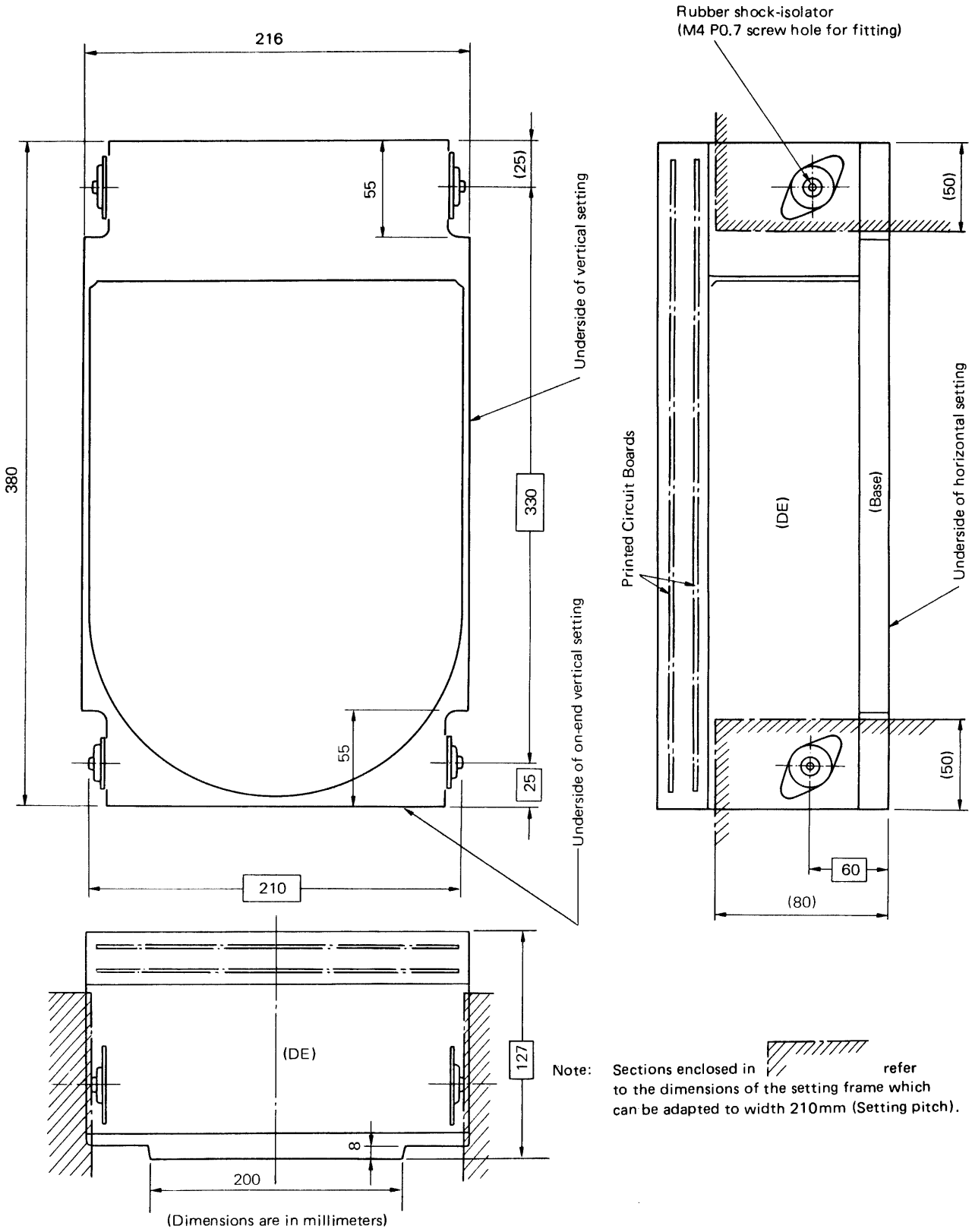
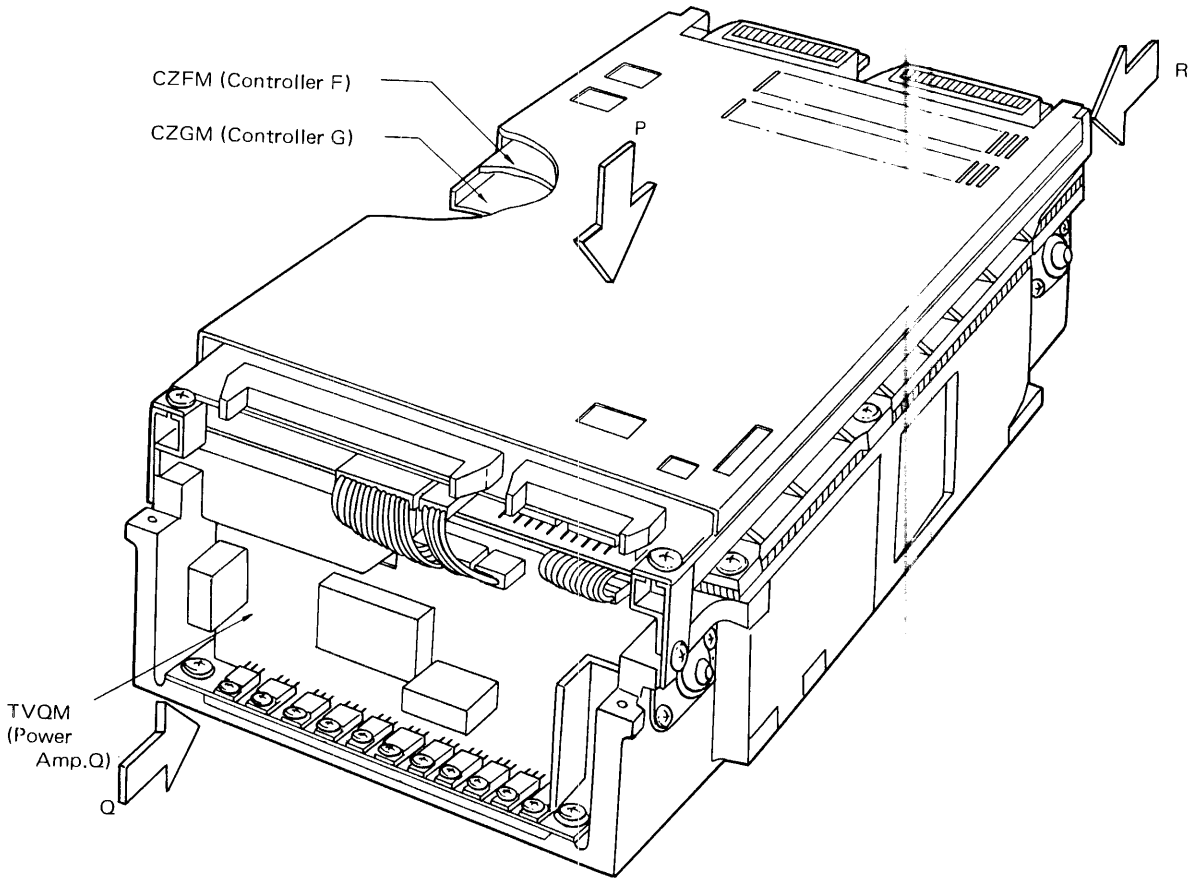


Figure 3-4-2 Mounting Dimensions of the Unit

3.4.2 Service Area

Maintenance, securing for transportation, cable connection, are accessed as shown below.

When determining the service area and where to install the locker, make sure that there is enough room for maintenance work.



P side: Maintenance operation on PCB (CZFM, CZGM)
Q side: Maintenance operation on PCB (TVQM)
Cable connections
Securing the unit. (Refer to 3.4.4)
R side: Securing the unit. (Refer to 3.4.4)
Operating the panel unit (Optional)

Figure 3-4-3 Maintenance Access on the Unit

3.4.3 Securing the Unit

When installing the unit, it is important that suitable clearance be maintained between the drive and any other hard parts such as mounting plate even during extreme excursions of the shock isolators, operating as well as non-operating (both storage and shipping).

For this purpose, the unit is provided with screw holes on Q side and S side (refer to Figure 3-4-3).

The holes are used to secure the unit to the mounting frame during shipment. Examples of securing the unit are shown in Figure 3-4-4 and Figure 3-4-5.

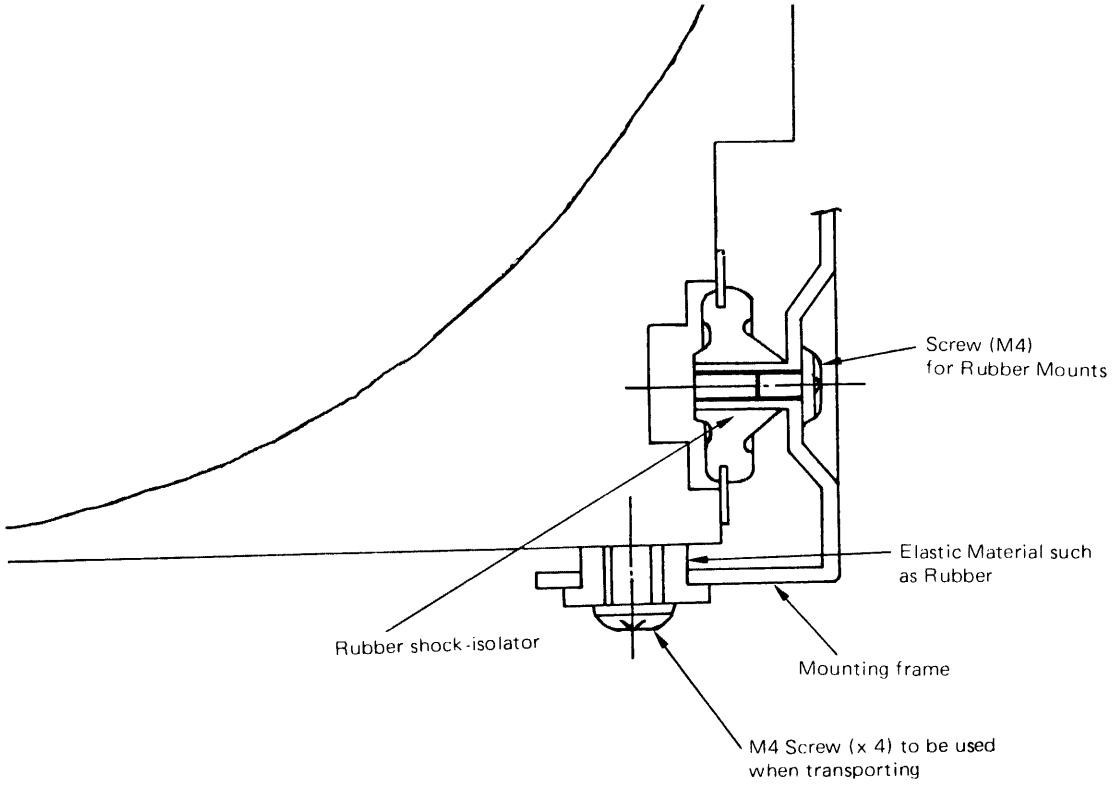
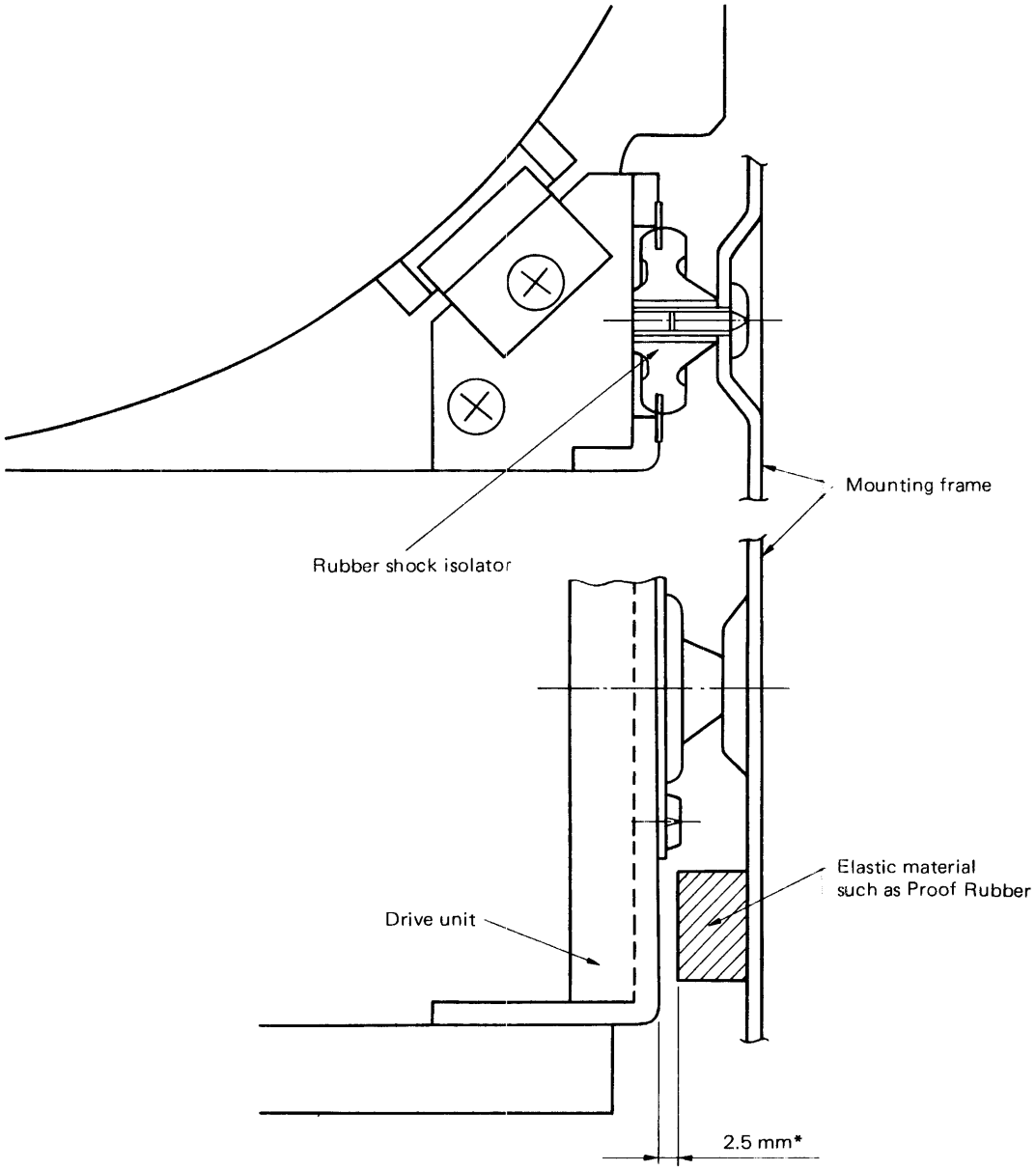


Figure 3-4-4 Securing the Unit (Example 1)



* Maintain this gap so there is no contact with the drive unit in case of shock or vibration.

Figure 3-4-5 Securing the Unit (Example 2)

A more effective use of these holes is to attach some elastic materials as stoppers. The stopper acts as a shock absorber, keeping a suitable clearance. The stopper protects not only the device but also rubber shockisolators from damage. Figure 3-4-6 shows recommended form of the stopper. This stopper is effective when operating as well as non-operating, and it is unnecessary to remove after shipping.

The screw hole dimensions on the unit are shown in Figure 3-4-7.

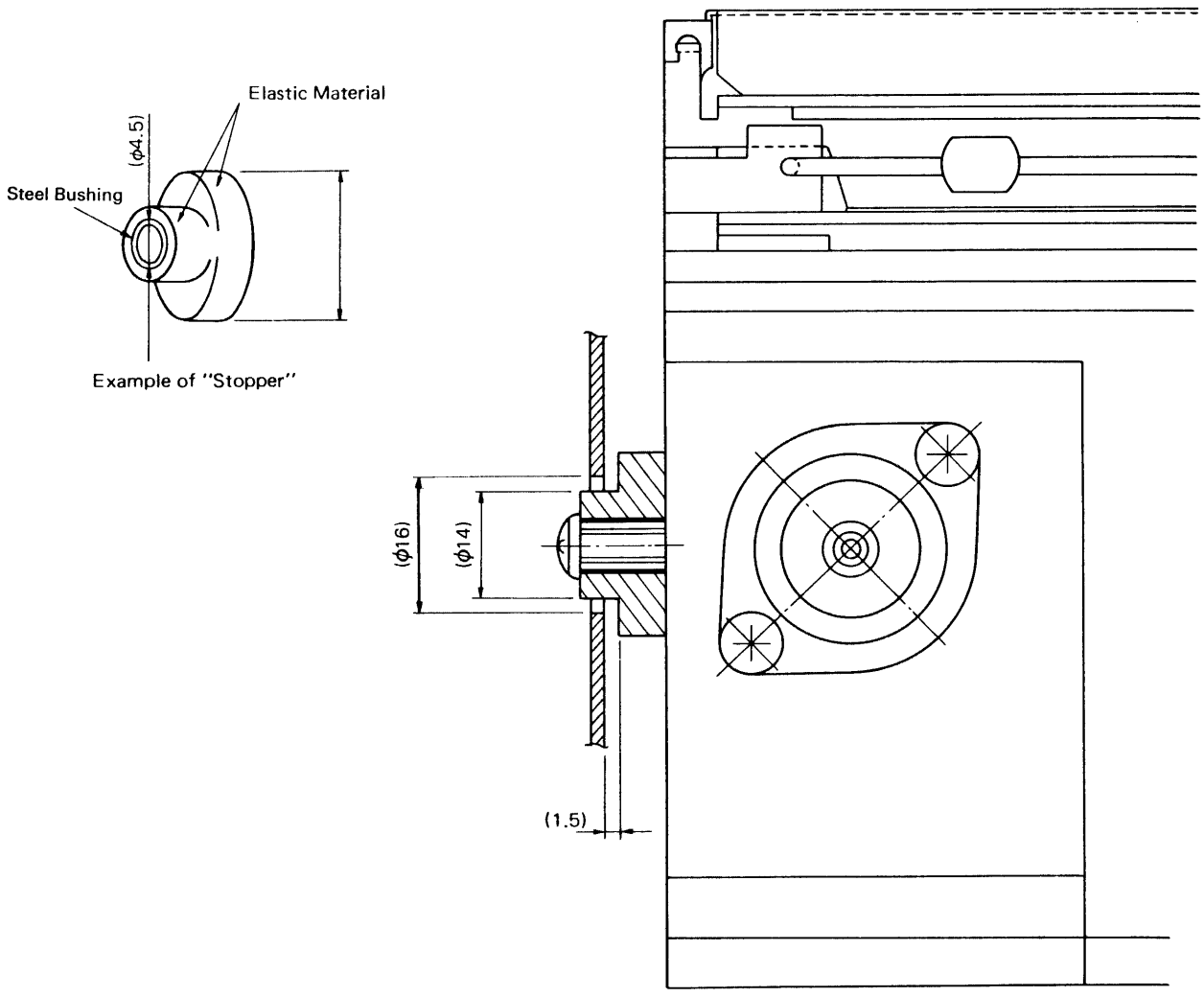
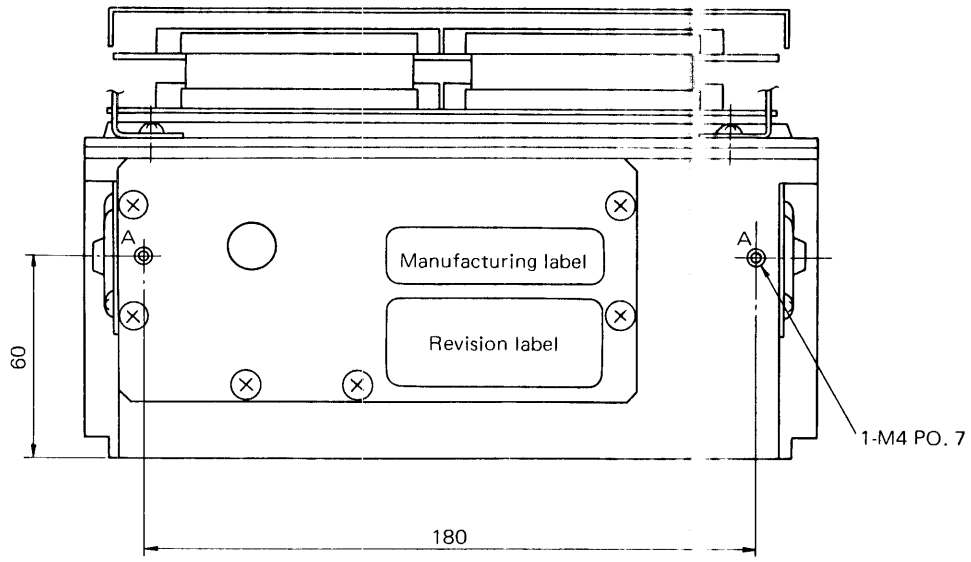
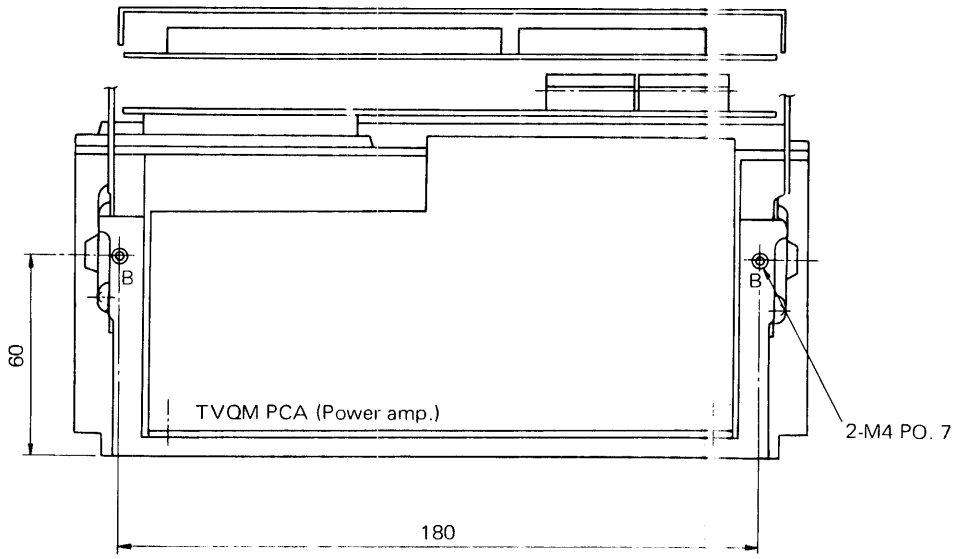


Figure 3-4-6 Form of the Stopper

(1) R side



(2) Q side



(3) Q side
(with Fan Unit)

Pitch
A-B: 380mm
A-C: 415mm

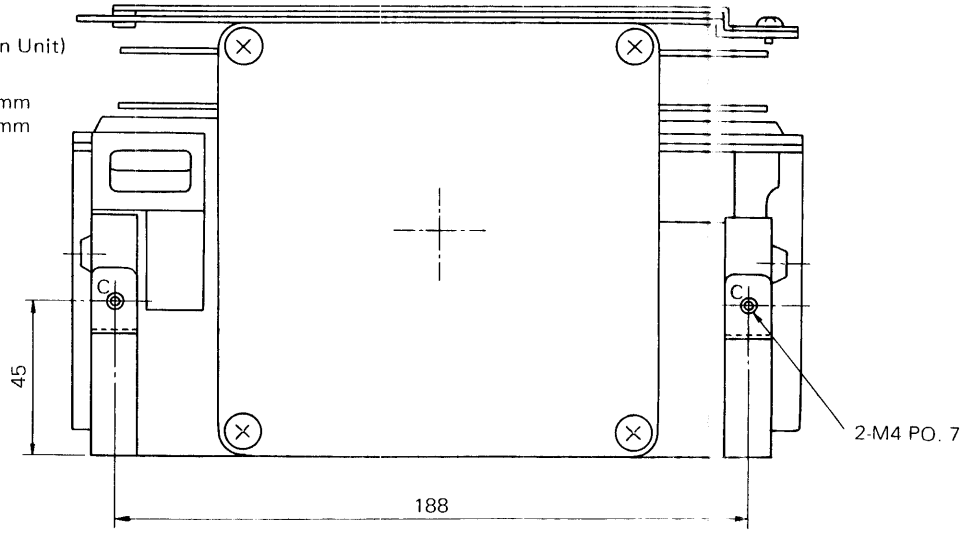


Figure 3-4-7 Dimensions of the Screw Holes

3.4.4 Cooling*

This unit requires some means of cooling, since there is no internal blower motor.

Figure 3-4-8 shows the recommended air flow posture.

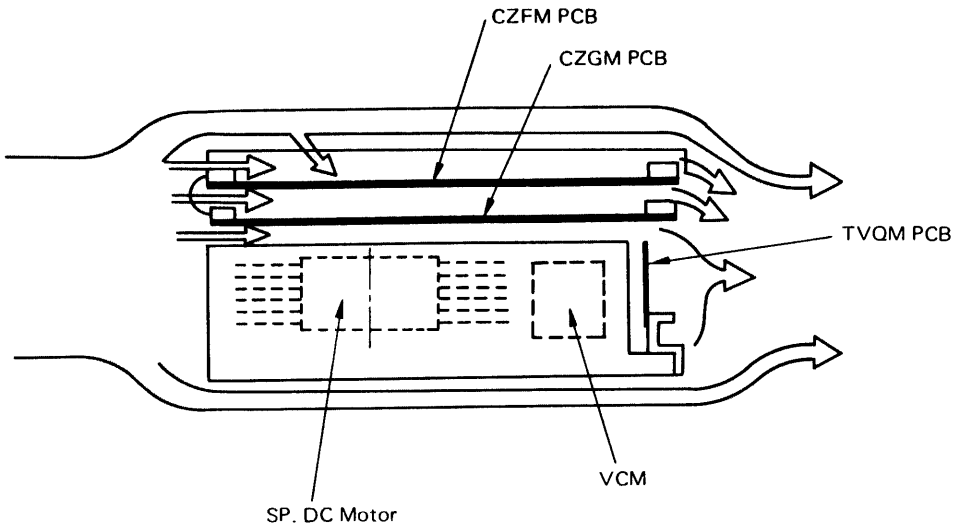


Figure 3-4-8 Recommended Air Flow Posture

* For this purpose, an optional fan unit is available. This fan unit will remove the generated heat most effectively. (Refer to 1.3.2.1)

The cooling condition can be confirmed by taking the surface temperature of some ICs and heat sinks.

The following IC's surface temperature must be kept under the temperature listed on the Table 3-4-1.

Table 3-4-1 Thermal Check Points

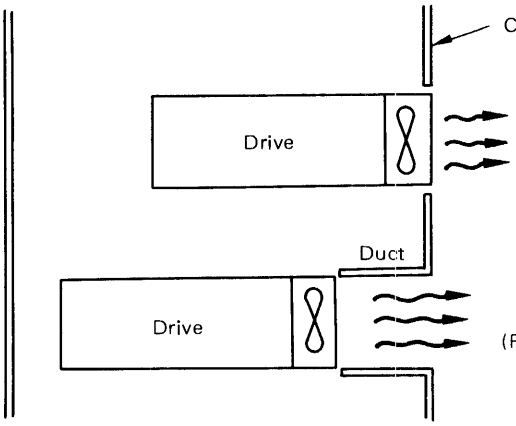
Part No.	On Board	Maximum surface Temperature (Tc)
Q20	CZFM PCB	85°C
Q17	"	85°C
Q38	CZGM PCB	85°C
Q35	"	85°C
Q8	TVQM PCB	80°C
Aluminum base (Bottom side)	DE	65°C

* Random seeking
* Even at max. environment temperature (40°C)

Note: Please refer to section 10 for check point location.

Figure 3-4-9 shows some examples of cooling installation.

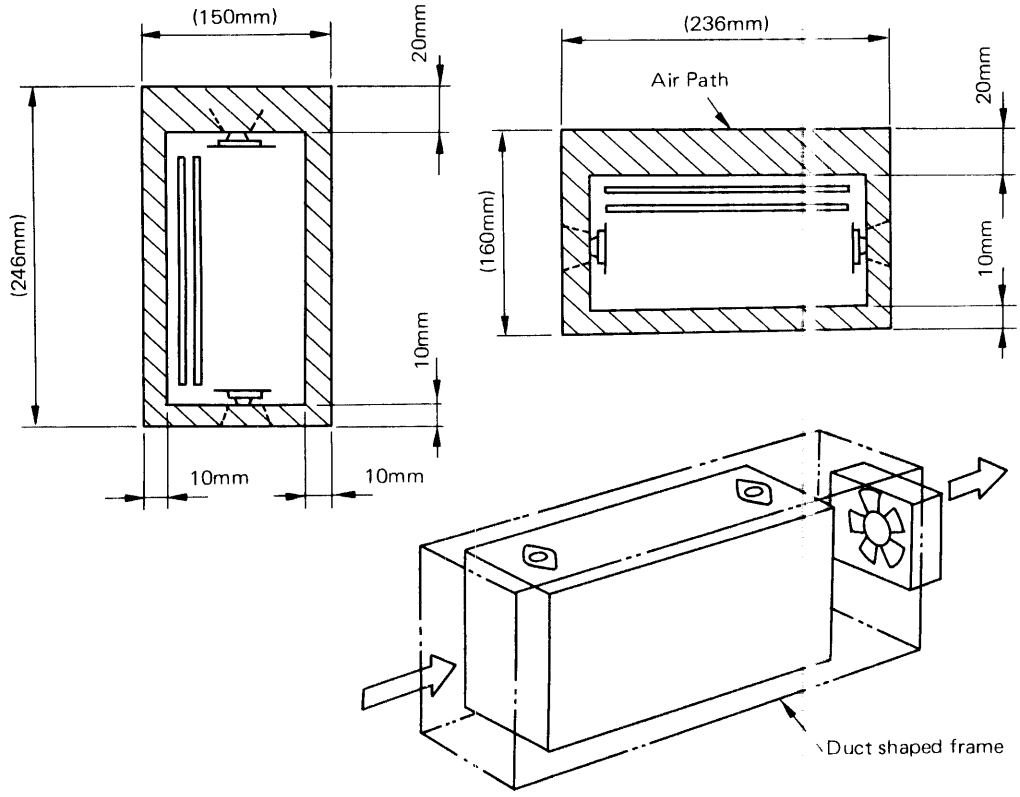
(a) Using optional fan unit



* Warmed air must be exhausted directly out of the cabinet.

(b) Without optional fan unit

We recommend that the installation frame is shaped like a duct and the cooling air flow path as follows:



* Air flow rate of more than $1m^3$/min through the duct must be maintained.

Figure 3-4-9 Examples of Installation Cooling

3.5 MOUNTING OF OPTIONS

3.5.1 Mounting the fan unit

The optional fan unit can be mounted or replaced in the field. See Subsection 1.3.2.1 for the specifications, shape, and connector pin assignments of the fan unit. The mounting procedures of an optional fan are as follows:

(1) Remove the protection cover of the power amplifier PC board (TVQM) at the rear of the equipment. (The screws are used to attach the fan. The cover is not used when the fan unit is used.)
(2) Mount the fan unit and attach it with the screws from the protection cover.
(3) Place the interface cables at the top of the fan unit.
(4) Connect the power supply cable to the fan unit. Refer to Figure 3-5-1.

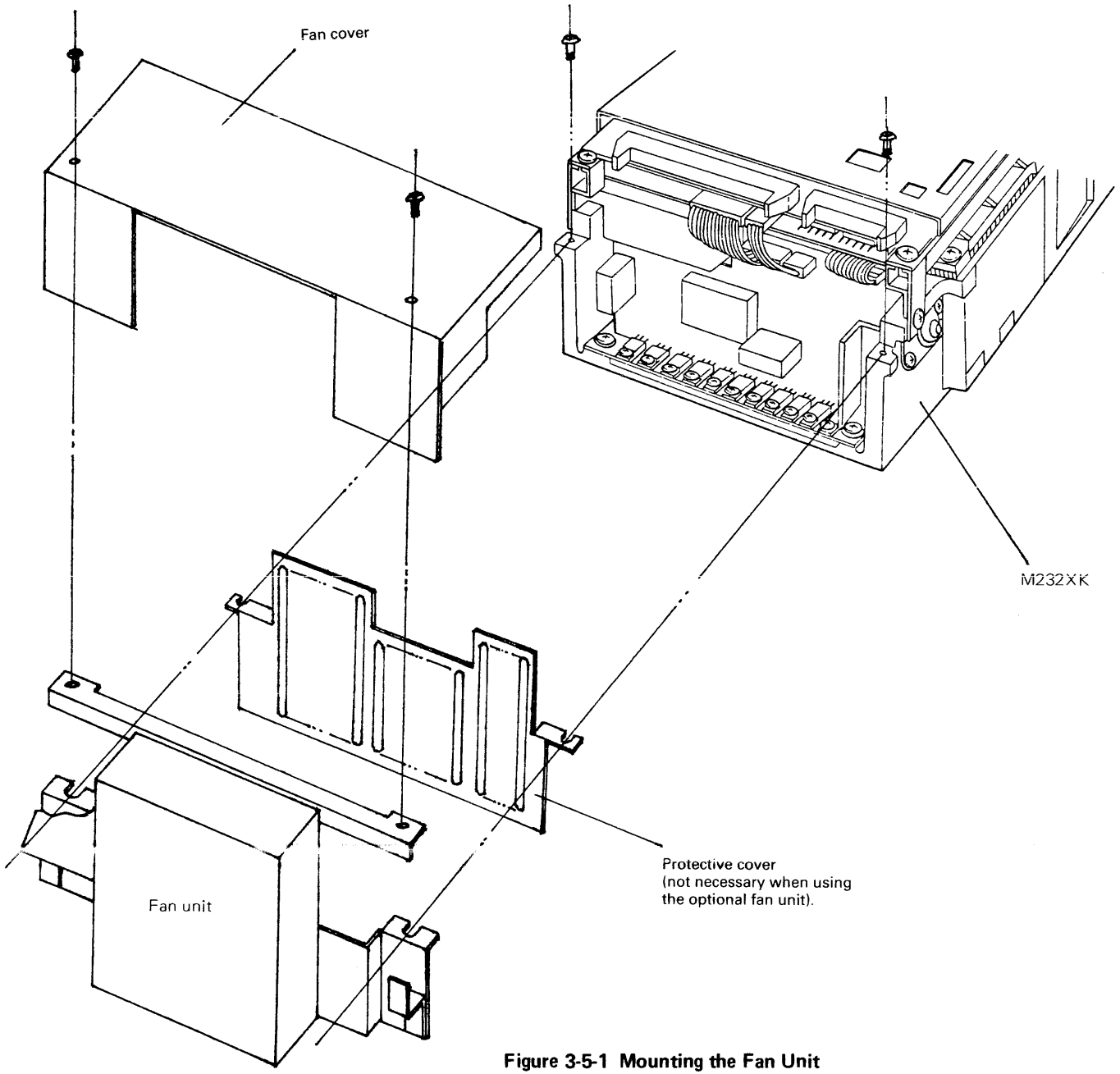
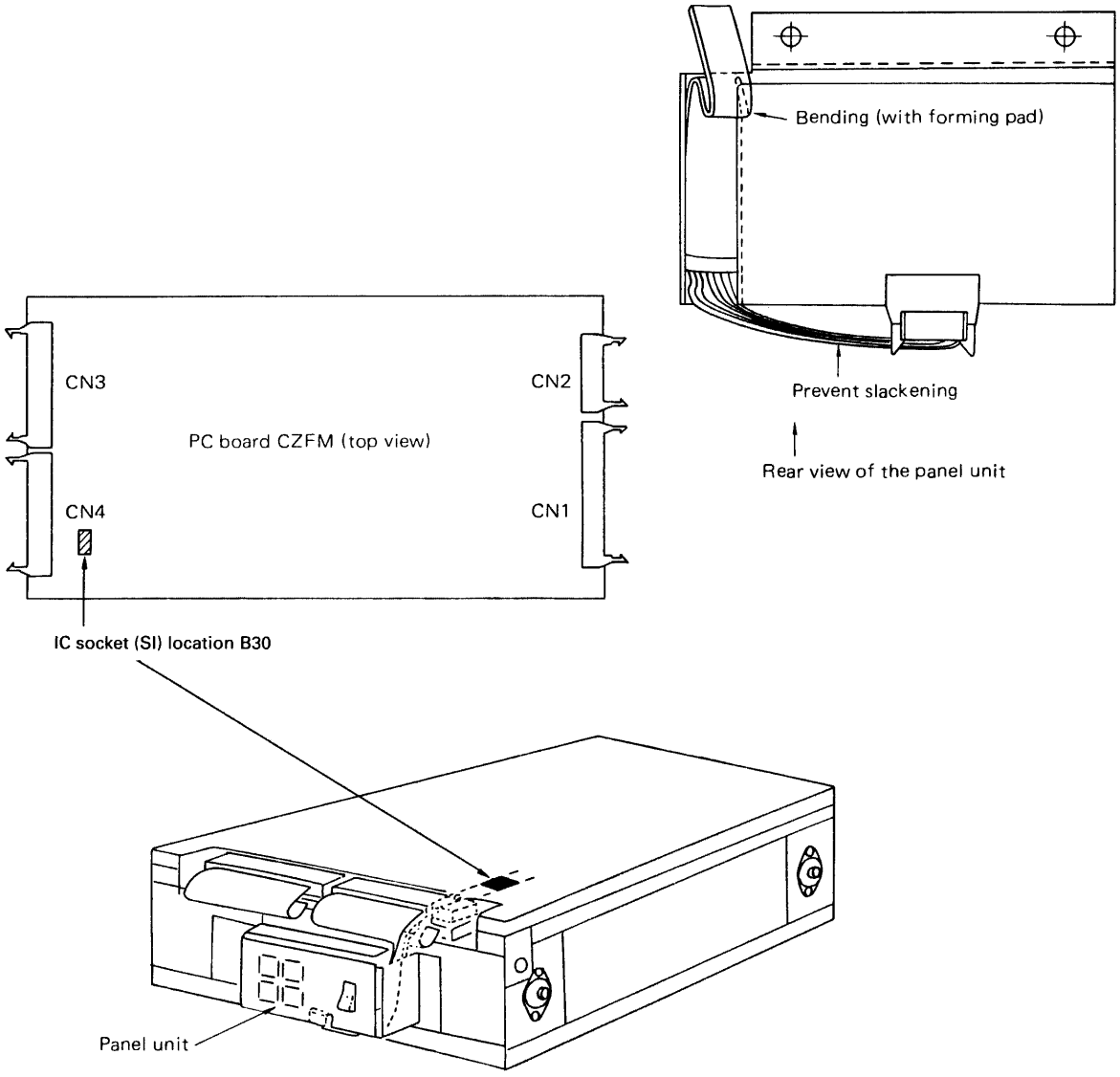


Figure 3-5-1 Mounting the Fan Unit

3.5.2 Mounting the Panel Unit

Figure 3-5-2 shows panel unit mounting diagrams.

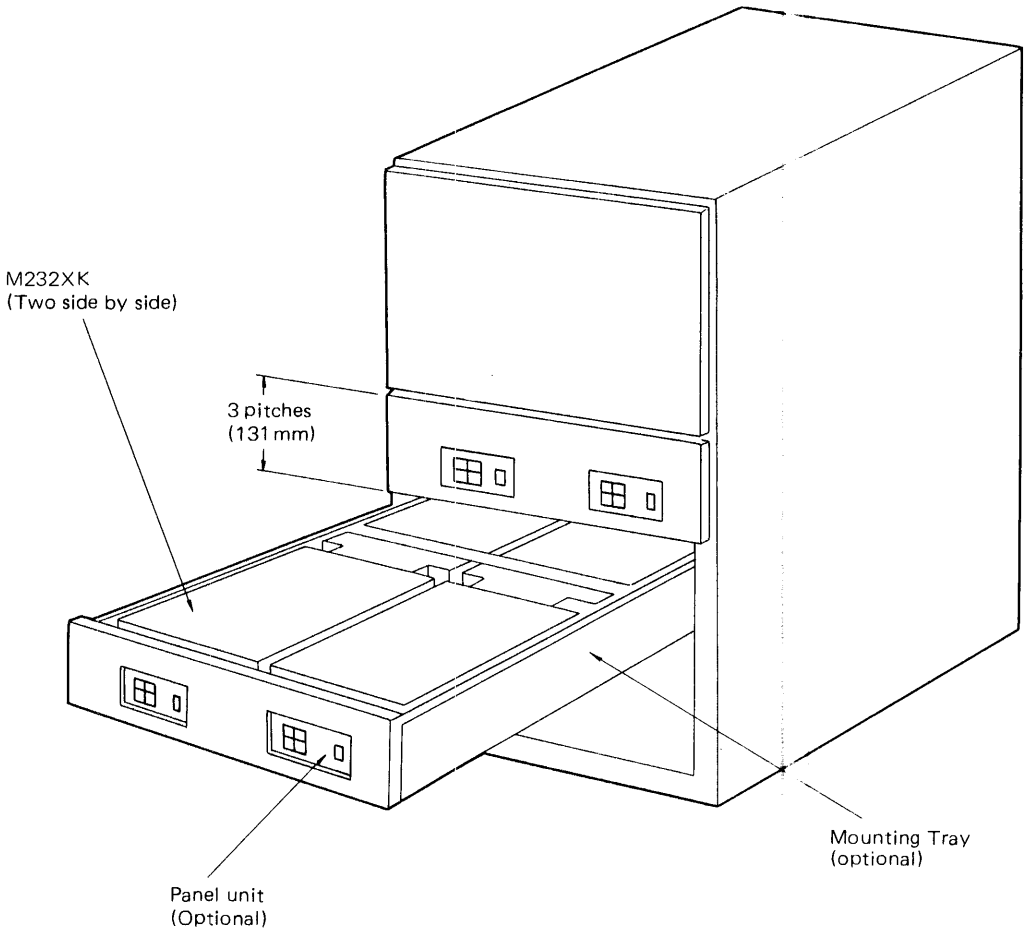


Note: To prevent the connection cable from slackening under the panel unit or on the equipment top (PC board), loop the cable at the rear of the panel unit as shown in the figure above.

Figure 3-5-2 Mounting the Panel Unit

3.5.3 Installation Mounting Tray

Two disk drive units can be installed side by side, in 3 pitches (131mm) of height, in a 19-inch rack using the optional mounting tray as shown in Figure 3-5-3.



Note: Refer to Section 1-3-2-4.

Figure 3-5-3 Installation in the 19-inch Rack

3.5.3.1 Installation Mounting Tray in the 19-inch Rack

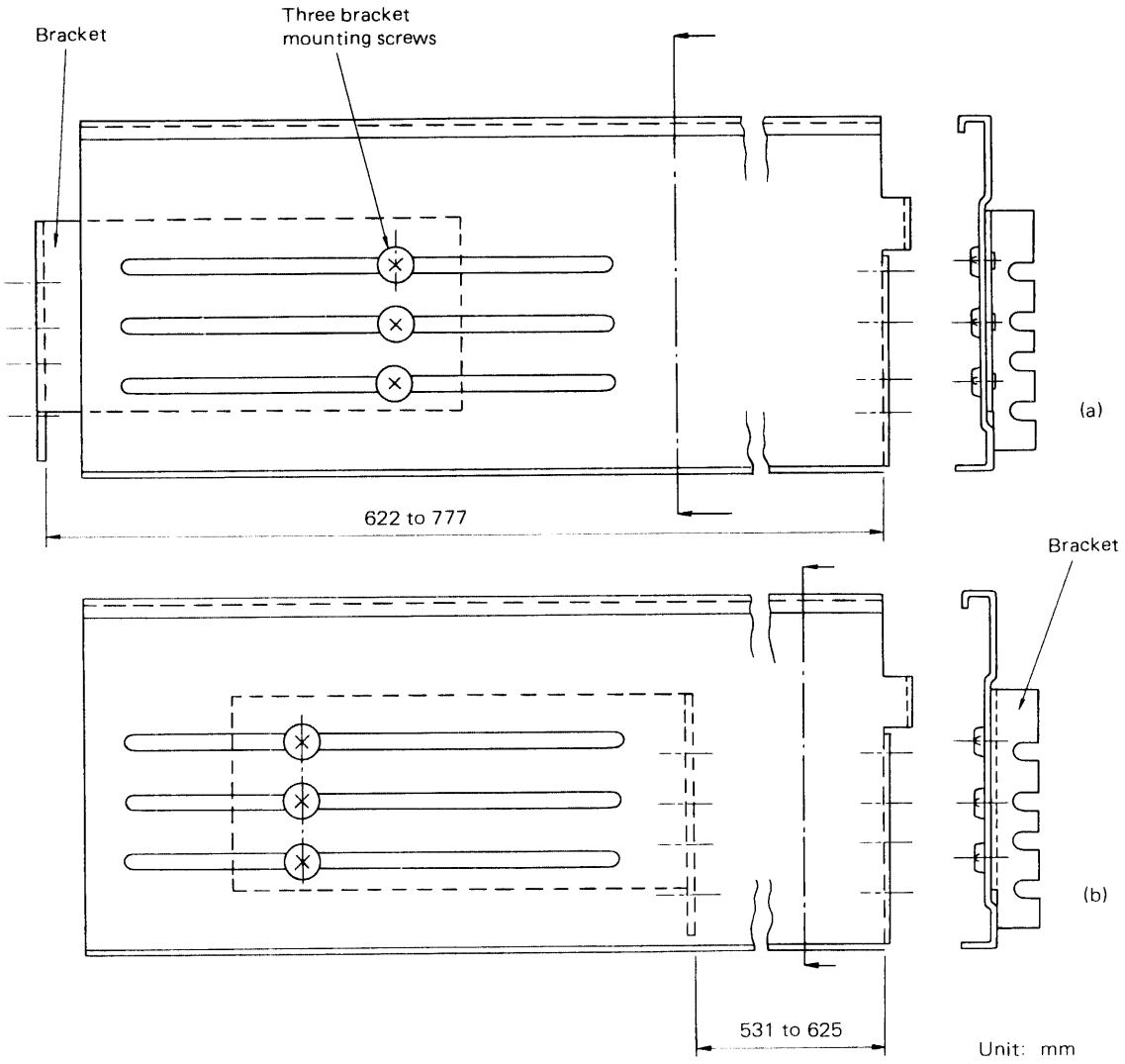
First, mount the bracket assembly on the 19 inch rack as follows. The bracket assembly consists of a pair of right and left slide guides (outer rails).

(1) Loosen 3 screws which hold the bracket in the back, so that it moves back and forth. (See Figure 3-5-4.)
The installation frame can be mounted in the 19 inch rack with a depth of mounting pitch ranging from 531 mm to 777 mm by adjusting the brackets. When mounting the installation frame in the rack with a depth of 622 mm to 777 mm, secure the brackets as shown in Figure 3-5-4 (a).
For racks other than the above, secure the brakets as shown in Figure 3-5-4, (b). The brackets are symmetrical, so a pair can be used for either (a) or (b).

(2) Remove tapped plates and hold them on the 19-inch rack post as shown in Figure 3-5-5, (a).

(3) Install left and right outer rails (bracket assembly) in the 19-inch rack. Tighten the bracket mounting screws after adjusting bracket location to fit it to the depth of the mounting pitch. (See Figure 3-5-5, (b).)

(4) Mount the outer rails using tapped plates with the bracket U-slots (in the back and front) pressed against the tapped plate fixing screws. (See Figure 3-5-5, (c).)



Note: The above figure ((a) and (b)) shows only the right slide guide (see from the front). The brackets in (a) and (b) are symmetrical to each other.

Figure 3-5-4 Bracket Assembly

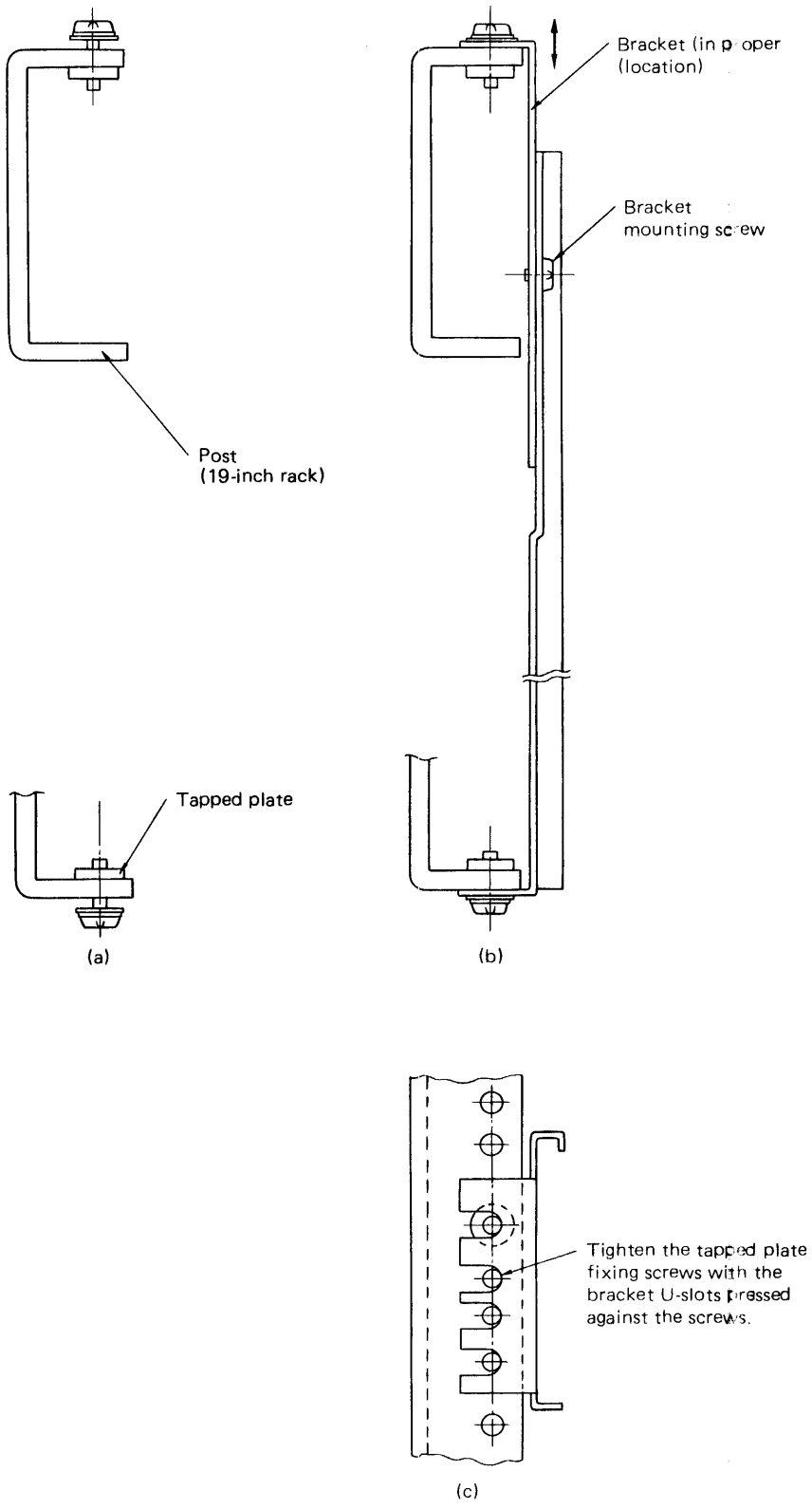


Figure 3-5-5 Bracket Assembly Mounting on the 19-inch Rack

(5) Insert the mounting tray (inner rail) and check its movement. If it does not slide freely, loosen the tapped plate holding screws and adjust outer rail locations for their relative width.
Confirm that the inner rail stops against the stopper when it is pulled out. (The installation frame can be pulled out approximately 595 mm.)
(6) Insert the mounting tray and fix it to the outer rails at the front left and right. (See Figure 3-5-6).
(7) Mount the front panel.

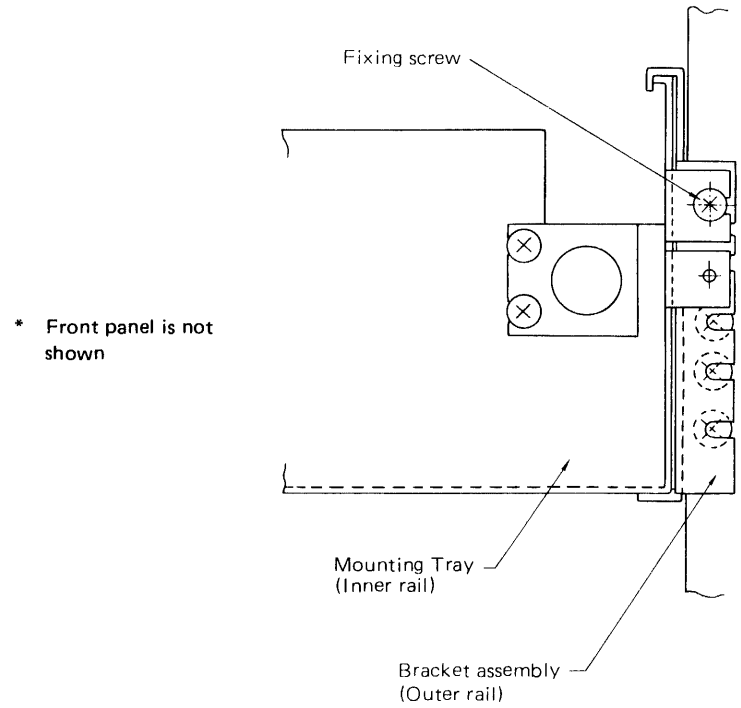


Figure 3-5-6 Mounting Tray to the Outer Rails

3.5.3.2 Each Unit Installation on the Mounting Tray

(1) Fan unit installation
Disk drive units installed on the Mounting Tray must have a fan unit. Refer to Section 3.5.1.
(2) Disk drive unit (with fan) installation
(A) Mount the rubber stoppers, attached to the Mounting Tray, using taps in the front and back of the drive unit as shown in Figure 3-5-7.

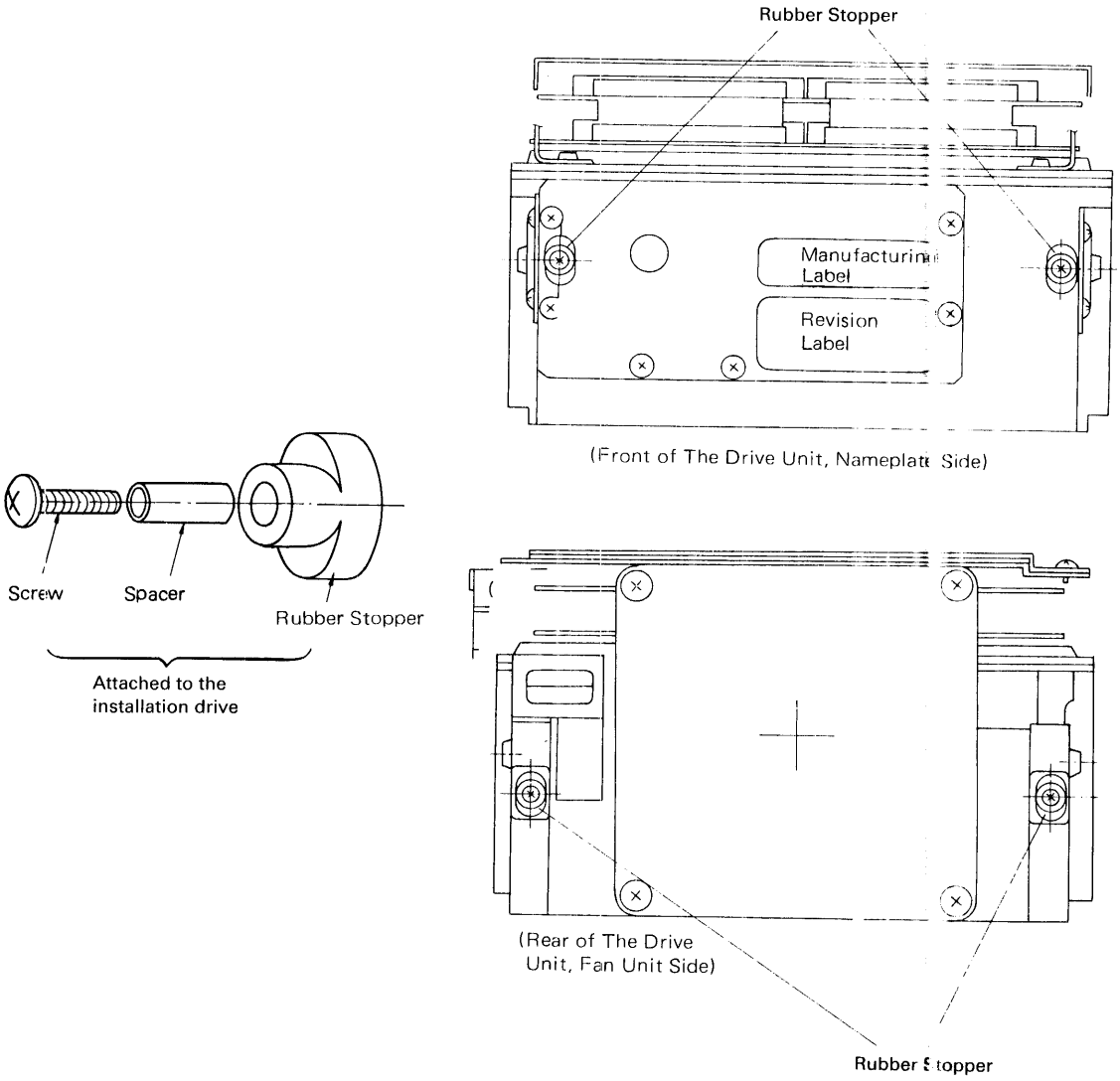
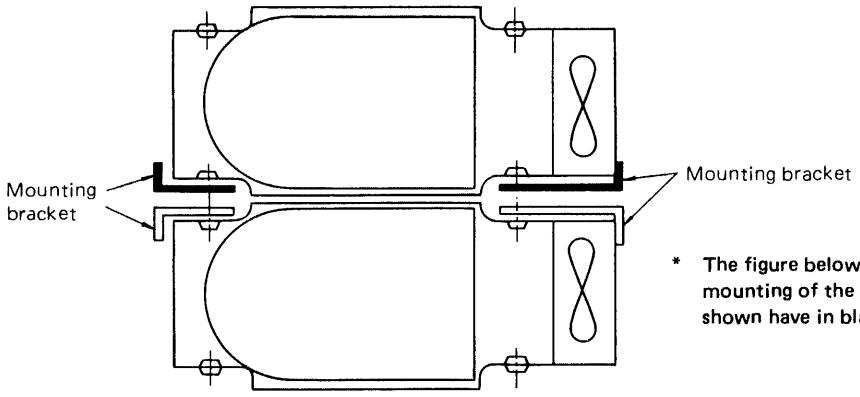


Figure 3-5-7 Rubber Stopper Mounting

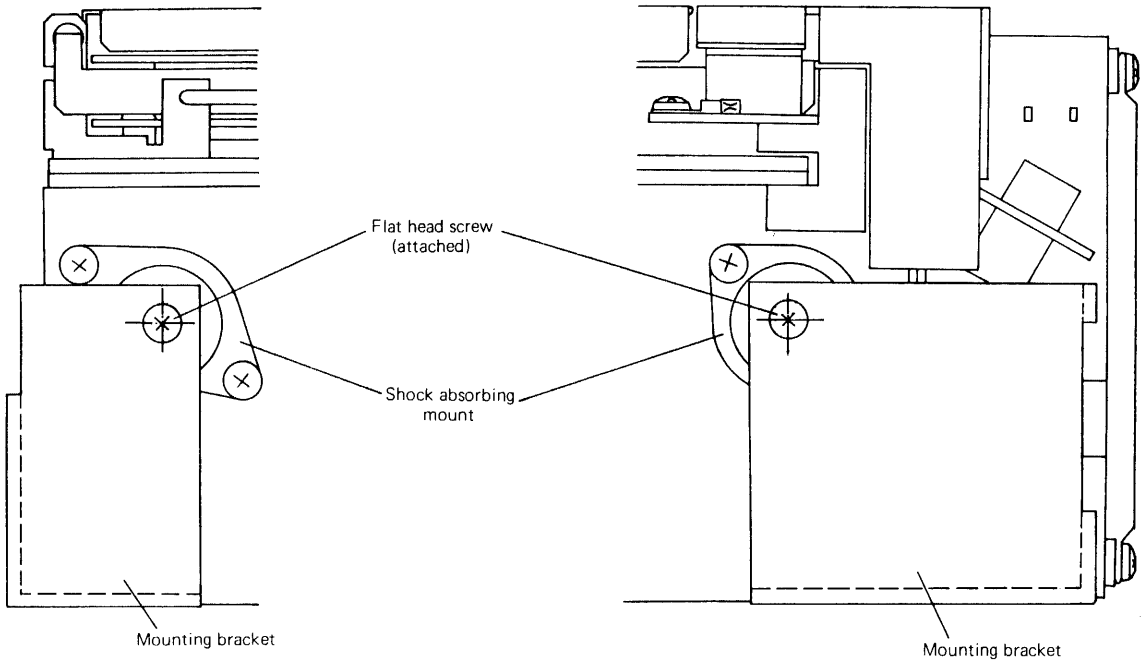
(B) Attach the mounting brackets using taps (M4) for shock absorbing mounts after setting the mounting brackets to disk drive unit location. Note that the front and back brackets are different. Refer to Figure 3-5-8.

(C) Remove the stopper supports from the Mounting Tray. (4 per installation frame (See Figure 3-5-9.))

(D) Set the disk drive on the Mounting Tray. The disk drive unit can temporarily ride on the front and back beams of the installation frame (inner rail) without manual support using the mounting brackets and 4 cushion supports in the front and back. (See Figure 3-5-10.) Therefore, even one person can install the drive unit in the Mounting Tray either removed or in the rack (pulled-out).
In this state, attach each shock absorbing mount (for the inside shock absorbing mount section, attach the mounting brackets to the inside shock absorbers first). See Figure 3-5-10.



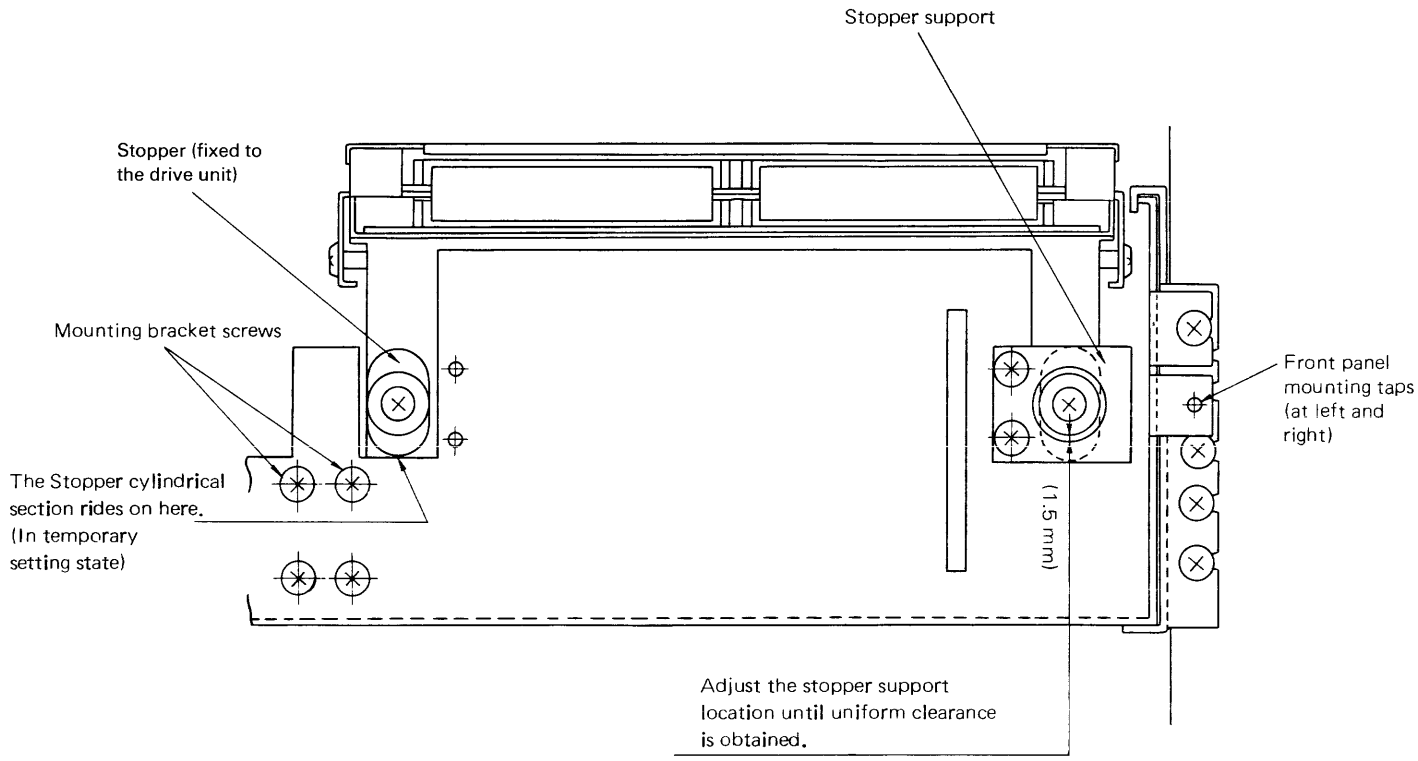
* The figure below shows mounting of the brackets shown have in black.



(a) Mounting in the front of the drive unit

(b) Mounting in the back of the drive unit

Figure 3-5-8 Bracket Mounting



* The figure shows the right drive unit (seen from the front). The stopper supports of the left drive unit and the back (fan side) are the same.

Figure 3-5-9 Stopper Support

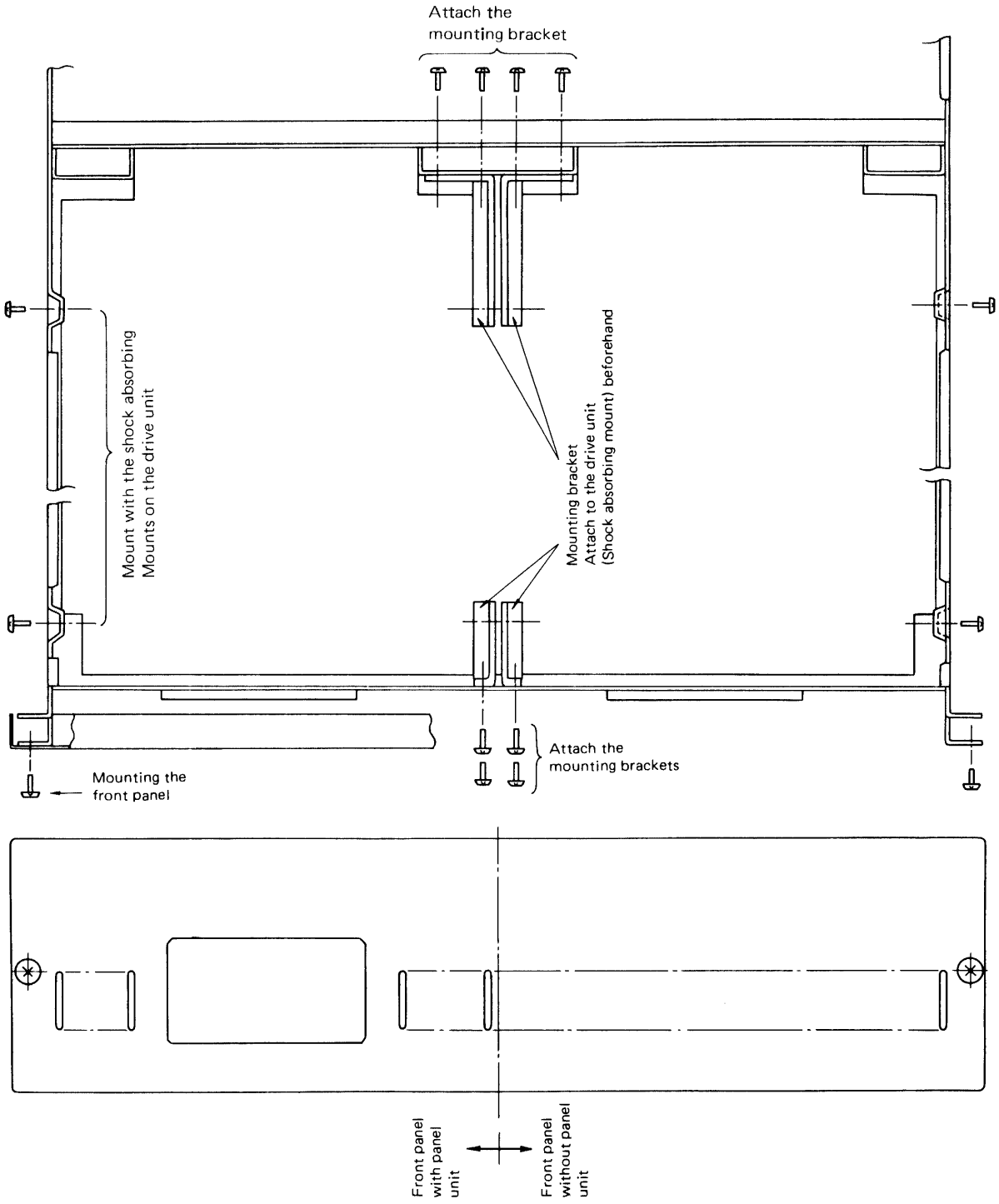


Figure 3-5-10 Mounting the Unit

(E) Mount the Stopper supports that were removed in procedure (C), so that clearances around the stopper including those in its front and back are 1.5 mm. See Figure 3-5-9.
(F) If the panel unit is required, mount it. See Item (3).
(G) Mount the front panel.

(3) Mounting the panel unit

The panel unit (optional) is mounted as shown in Section 3.5.2. When the panel unit is used in the Mounting Tray, mount it as shown in the following figure.

When the panel unit is mounted, use the Mounting Tray (B030-1810-0001A) as the inner rail. (Refer to Section 1.3.2.4.) This type of Mounting Tray has a blank panel on one side. When installing 2 drive units, this blank panel is not used. When installing 1 drive unit, mount this blank panel in the unused window.

Notes: 1. The protection cover on the installation frame edge protects cables from damage. Mount it together with the panel unit as shown in the following figure.
2. For cable forming, see Figure 3-5-2.

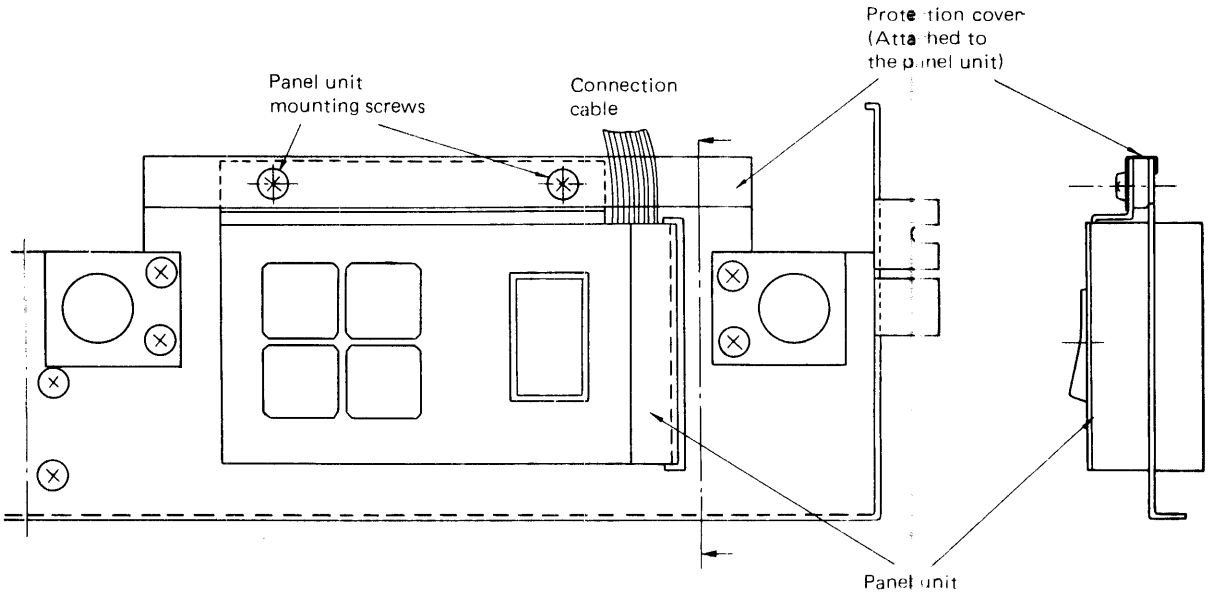
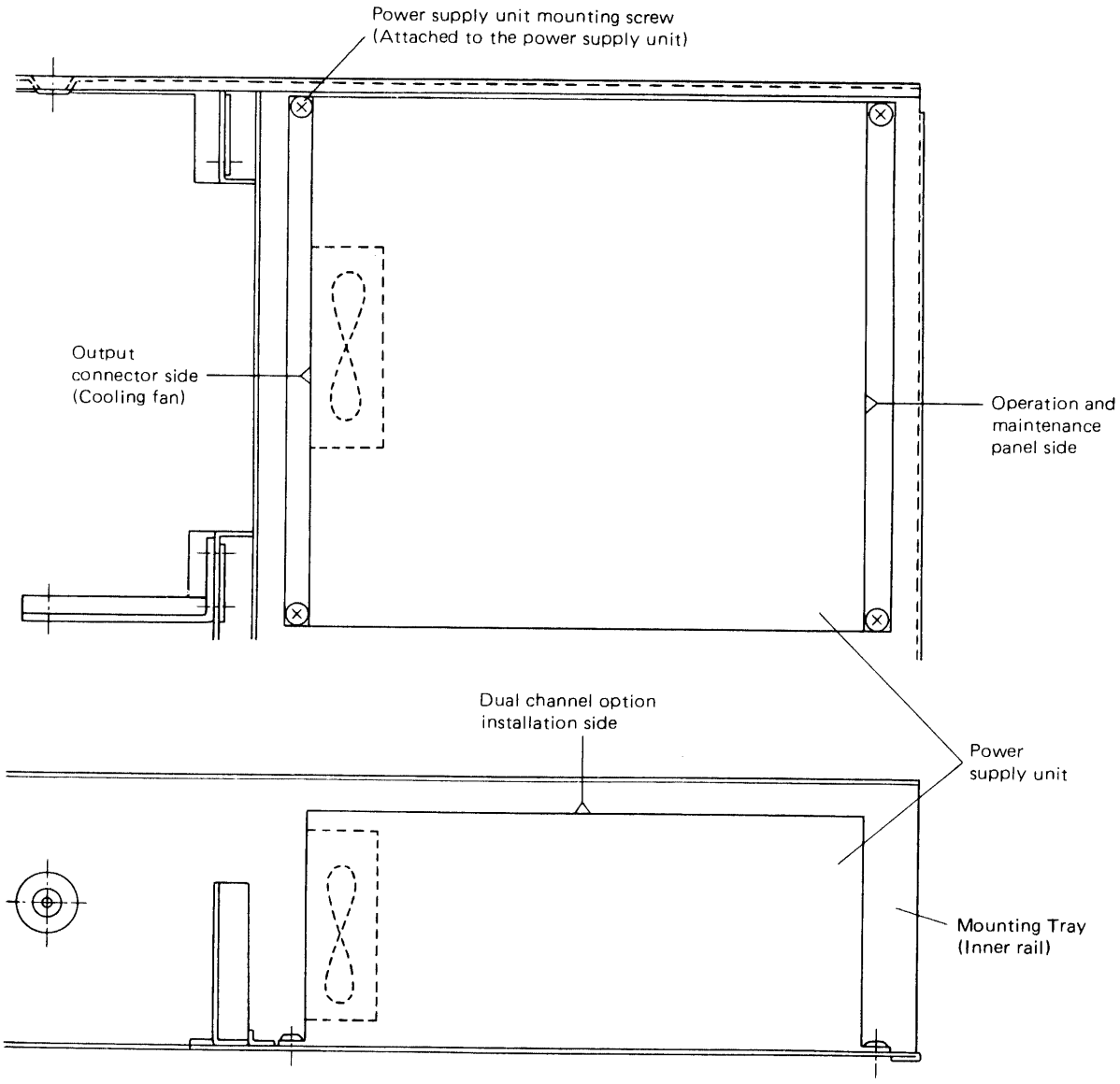


Figure 3-5-11 Mounting the Panel Unit



Note: Refer to Section 1.3.2.5 for optimum cable lengths when the optional power supply unit is installed.

Figure 3-5-12 Power Supply Unit Installation

(4) Dual channel option installation

The dual channel option can be mounted on the power supply unit. (Tap locations for mounting are shown in Figure 1-3-5.)

(A) Mount the bracket (2a) on the rail (1a) using screws SBD M3x5. The left and right brackets and rails are symmetrically mounted.

(B) Mount the spring (3a) on the rail (1a) using screws SBD M2x5. The left and right brackets and rails are symmetrically mounted.

(C) Mount the rails (1a) on the power supply unit using screws SSA M4x8.

(D) Mount the guide (4a) at the back (operating section) of the power supply unit using screws SBD M4x8.

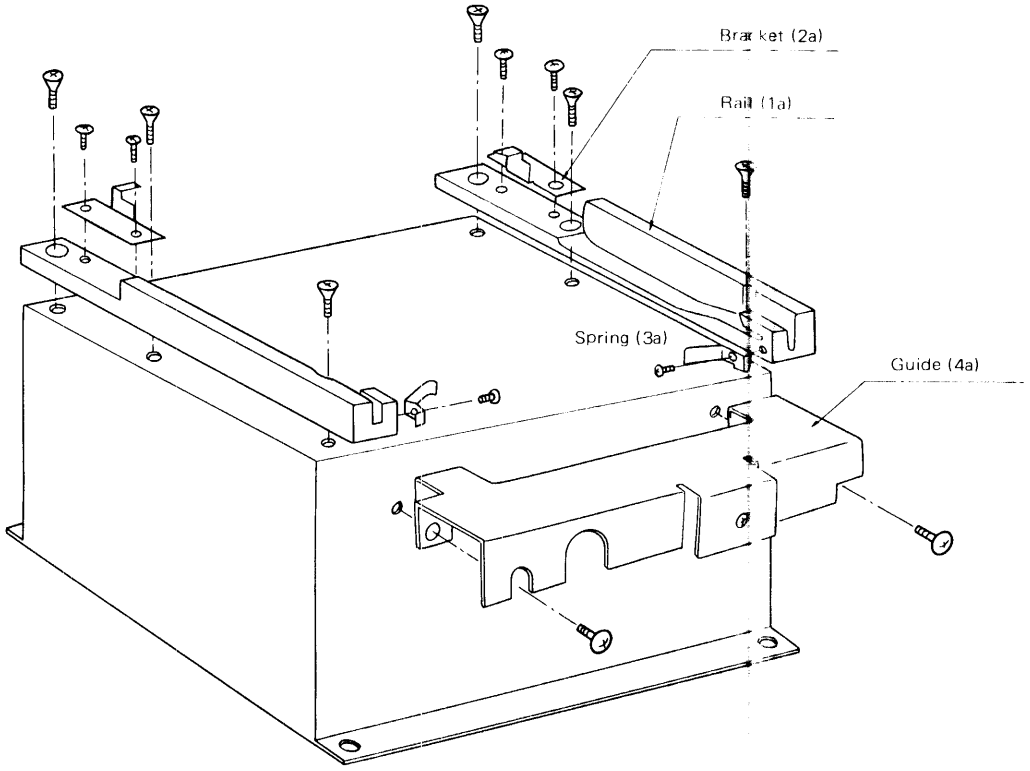


Figure 3-5-13 Dual Channel Option Installation 1

(E) Mount the dual channel PC board on the frame (6a) using screws SBD M3x5. (See Figure 3-5-14.)

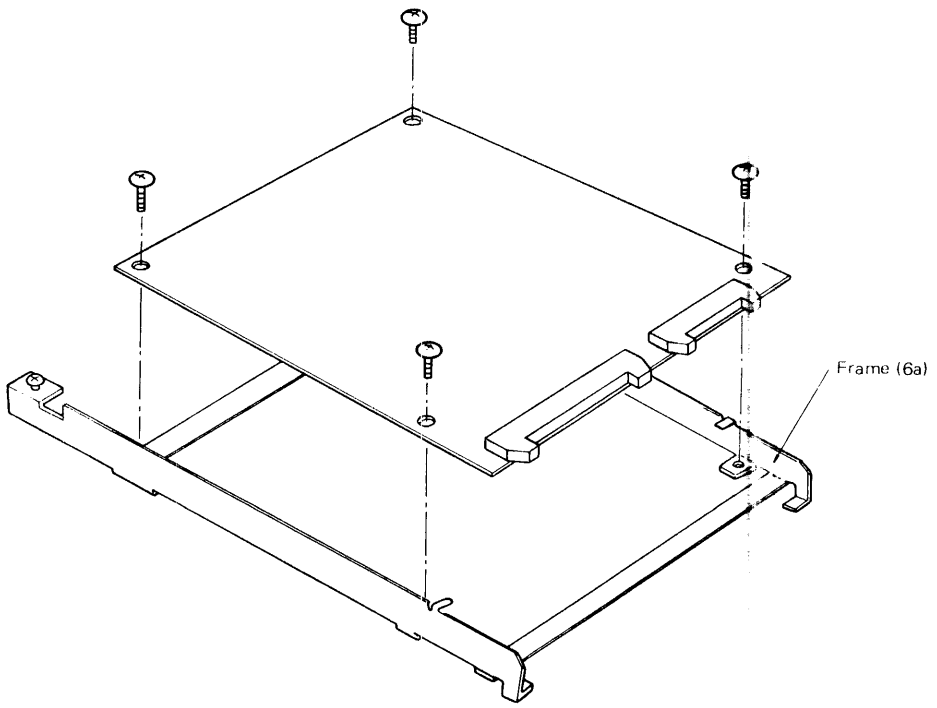


Figure 3-5-14 Dual Channel Option Installation 2

(F) Pressing PC board unit (PC board and frame assembly) (12a) downward, insert it until the springs deflect slightly. The PC board unit frame is automatically latched at lugs of the brackets (2a) and locked. (See Figure 3-5-15.)

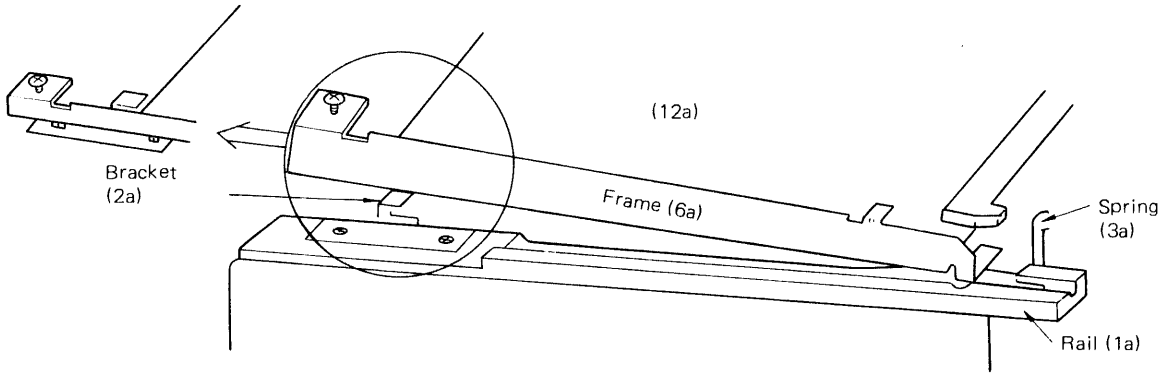


Figure 3-5-15 Dual Channel Frame Mount

(G) Connect CN25 on the PC board and CN33 on the power supply unit with the connection cable (B660-0625-T329A). (See Figure 3-5-16.)
(H) Connect interface cables (8a and 9a) between the drive unit (CZFM) and the dual channel PC board.
(I) Connect the A-channel cable B to the PC board, and pull the cable out behind the power supply unit.
(J) Remove the dual channel PC board from the rails and connect the A-channel cable A to the drive unit (CZFM), and pull the cable out under the dual channel PC board and behind the power supply unit.
(K) Connect B-channel cables A and B to the back of the PC board (CN21 and CN22) and pull them out behind the power supply unit.

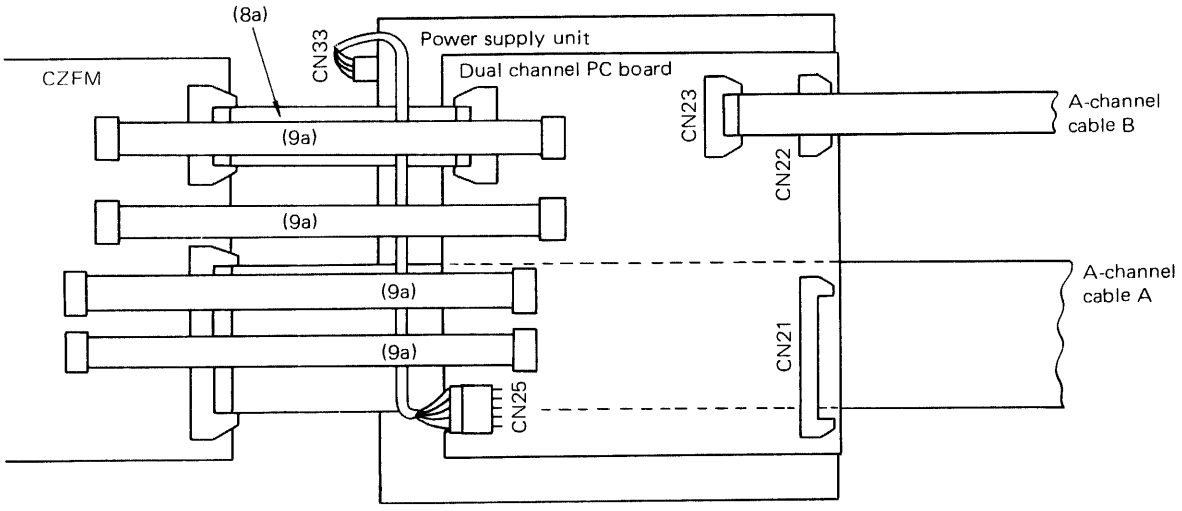


Figure 3-5-16 Dual Channel Cabling

(L) Attach the cover (11a) on the frame (6a) using screws SBD M3x5.

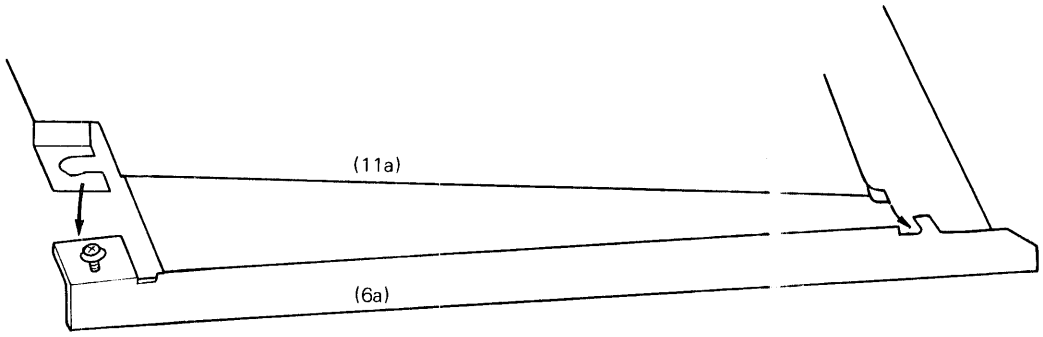


Figure 3-5-17 Dual Channel Top Cover Fixing

(M) Form the A- and B-channel interface cables along the guide (4a) and hold them with the cable retainer (13a).

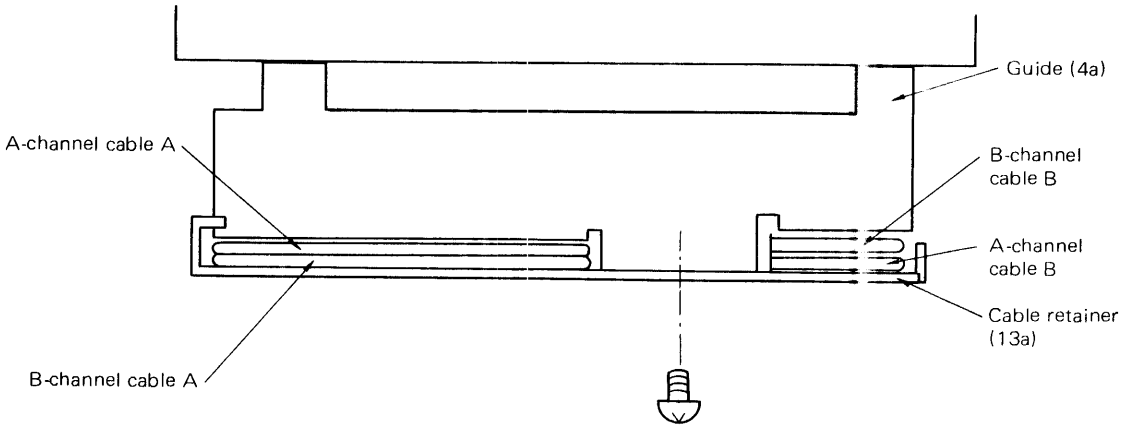


Figure 3-5-18 Dual Channel Interface Cables Holding

* Part number of the dual channel option is B03B-4740-E401A.

3.5.4 Mounting the Dual Channel Option

The procedure for mounting the dual channel option on the power supply (procedure B03B-4740-E401A) was previously described in Subsection 3.5.3.2. This section describes the procedure for mounting the option on the drive unit (procedure B03B-4740-E402A).

(1) Mount the dual channel PCB on frame as shown in Figure 3-5-14.
(2) Connect the drive unit (CZFM) to the PC board via the cable as shown in Figure 3-5-16.
(3) Insert cover between frame and the equipment from the front of the equipment, and fix cover.
(4) Fix the frame with PCB with two screws (SBD M3 x 5).
(5) Connect A-channel cable B (CN23).
(6) Attach cover 3b in the frame and fix with screw (SBD M4 x 6).
(7) Connect all other interface cable to channels A and B.
(8) When mounting the optional fan unit to the drive unit, fix the interface cable with the attached cable clamp.

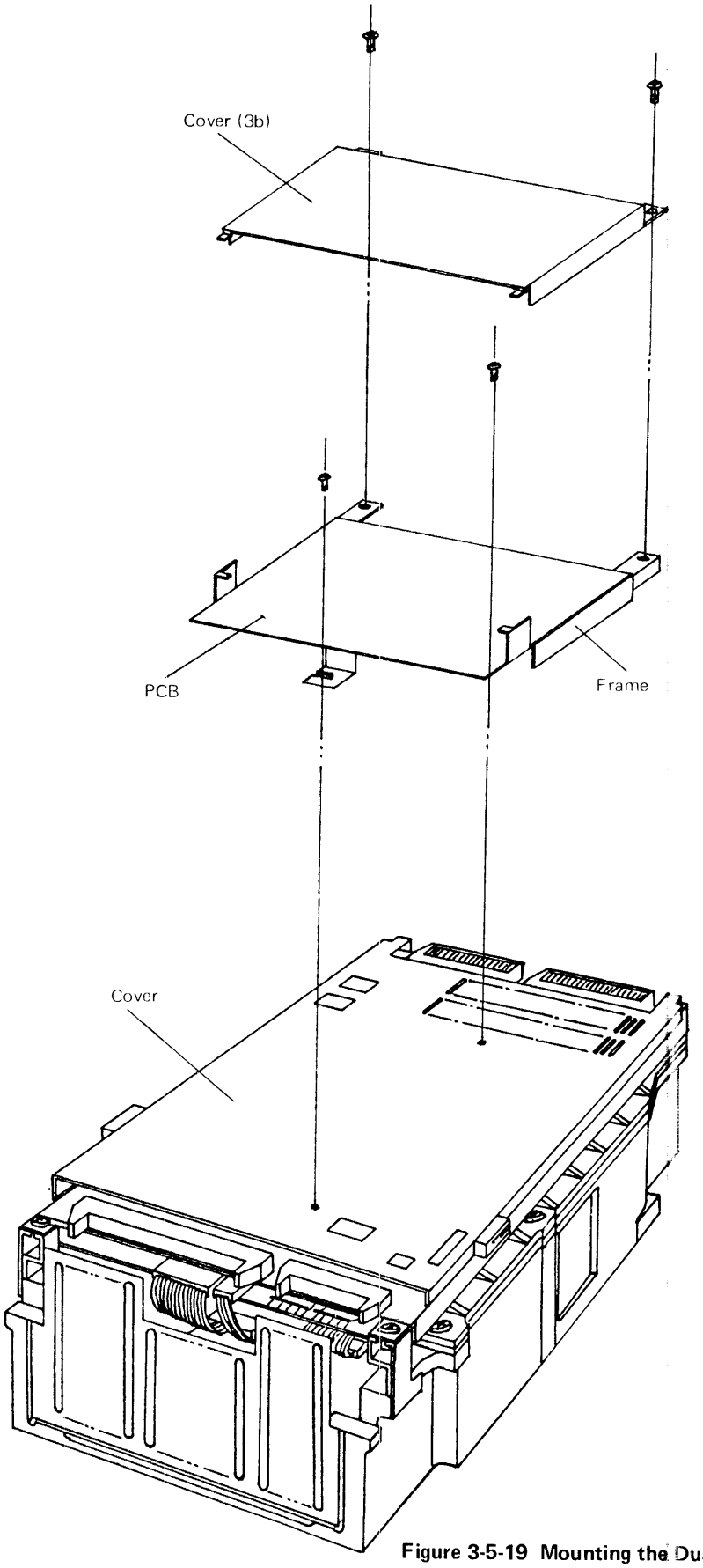


Figure 3-5-19 Mounting the Dual Channel Option

3.5.5 INSTALLATION OF THE POWER SUPPLY

3.1 Unpacking

Use normal care when opening the reusable shipping container for the Power Supply. After unpacking the unit, visually inspect it as follows:

(a) Check for scratches, rust and soiling.

(b) Check for loose or missing parts and screws.

3.2 Mounting

Do not insert mounting screws more than 6 mm into the Power Supply.

CAUTION:

Longer screws could cause an electrical short in the Power Supply.

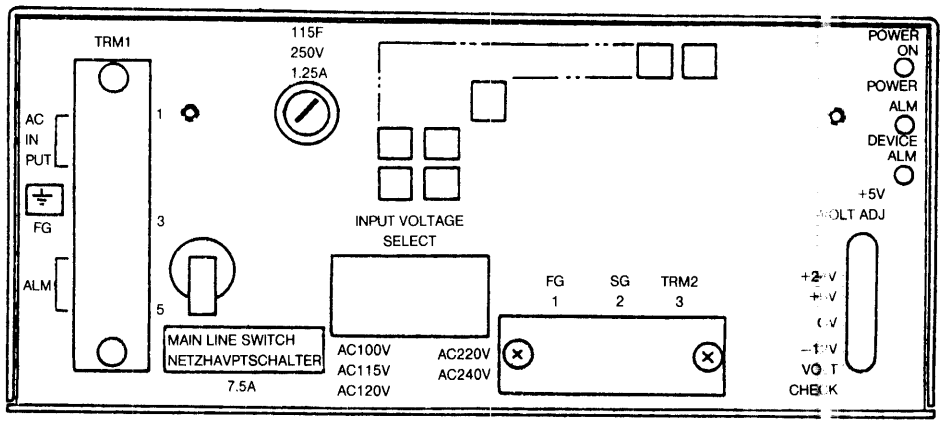
3.3 Input AC

The Power Supply can be selected to operate from one of two input groups, 100V AC at 50/60 Hz, 115V AC at 60 Hz, 120V AC at 60 Hz or 220V AC at 50 Hz, 240V AC at 50 Hz, by changing the Voltage Select switch, SW1. Input-voltage is provided between TRM1-1 to 2 at the front of the Power Supply. TRM1 Pin 3 is provided for frame ground (FG).

3.4 Output Voltages

All output voltages are provided on connectors CN31, CN32 and CN33 at the back of the Power Supply. The connectors are clearly marked by numbers. (Figure 3.1) The connection diagram is shown in Table 3.1.

FRONT VIEW



REAR VIEW

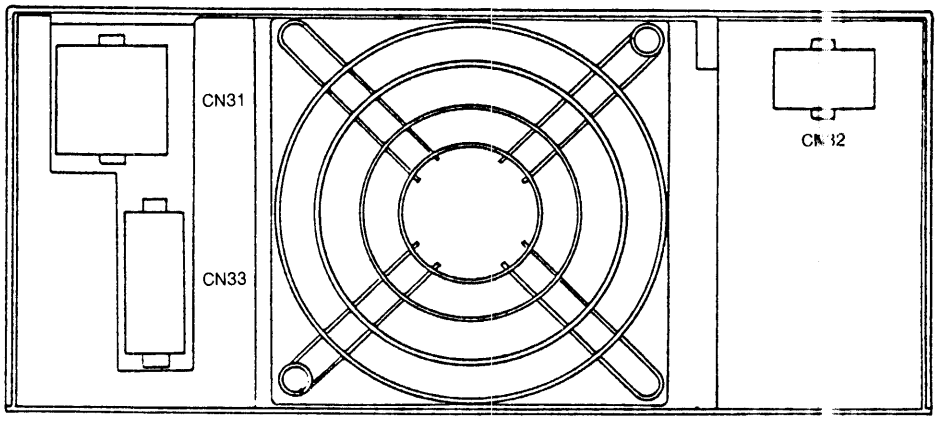


Figure 3.5.20 Power Supply Front and Rear View

Table 3.5.1 Power Supply Connection Diagram

Connector	No.	Voltage
CN31	1	0V
	2	0V
	3	−12V
	4	−12V
	5	0V
	6	0V
	7	+5V
	8	+5V
	9	0V
	10	0V
	11	+24V
	12	+24V
CN32	1	115V AC
	2	115V AC
	3	FG
	4	NC
	5	ALM (Receive)
	6	
CN33	1	+5V
*	2	0V
	3	−12V
	4	
	5	0V

*Used For Dual Port Only

3.6 CABLING

3.6.1 Connectors On Unit Side

Figure 3-6-1 shows the mounting positions of the interface connectors on the drive side.

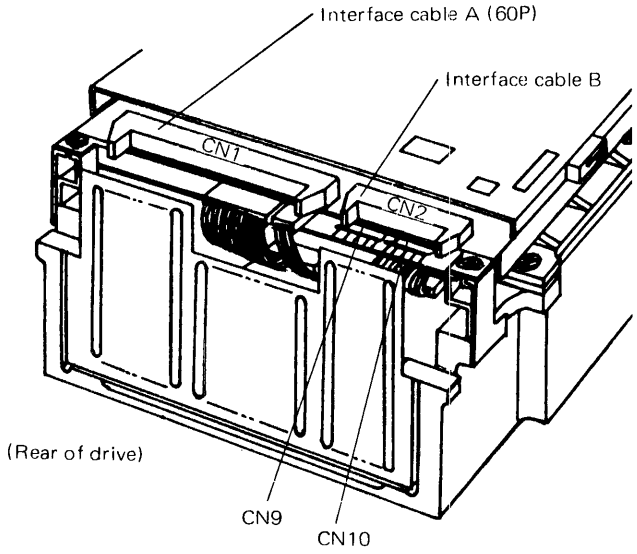


Figure 3-6-1 Mounting Positions of Connectors

Cables include an interface (A) cable 60P, an interface (B) cable 26P, and a power cable.

Refer to Section 3.6.2 for additional information on the power cable.

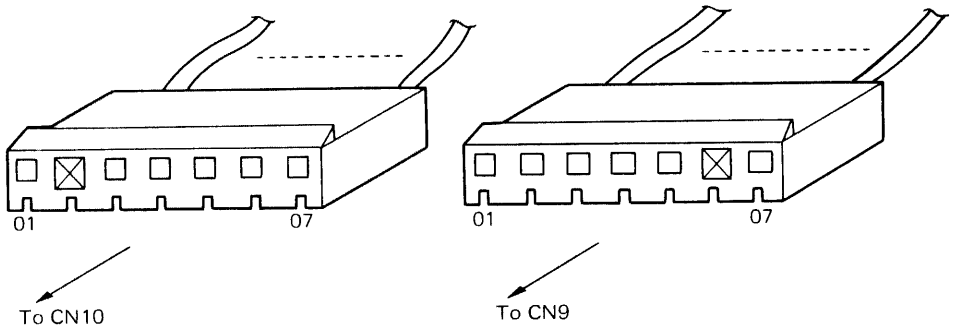
3.6.2 Power Cable Connection

The M232XK uses only DC power, Connector specification for the unit, recommended specifications for the cable, and pin assignment and voltages follows.

(1) Specification on the unit side
Header C63L-0820-0008 (2420-07A-G manufactured by Molex Japan Co., Ltd.)
(7P) x 2 pieces

(2) Recommended specifications on the cable side
- Housing C63L-0820-0007 (2139-7 manufactured by Molex Japan Co., Ltd.)
(7P) x 2 pieces
- Contact C63L-0820-0002 (2478-GL manufactured by Molex Japan Co., Ltd.)
(12 pieces)
- Key C63L-0820-0001 (2560-1 manufactured by Molex Japan Co., Ltd.)
(2 pieces)

(3) Pin assignment and voltages
Refer to Figure 3-6-2.



(CN10)			(CN9)		
1	0 V	(−12 V RTN)	1	+5 V	
2	(Key)		2	+5 V	
3	0 V	(−12 V RTN)	3	0 V	(+24 V RTN)
4	−12 V		4	0 V	(+24 V RTN)
5	−12 V		5	+24 V	
6	0 V	(+5 V RTN)	6	(Key)	
7	0 V	(+5 V RTN)	7	+24 V	

Note: 1 Use AWG18 as the cable material.
2 The cable length must be less than 1.5m.
3 All "0V" must be connected together at power supply outputs.

Figure 3-6-2 Pin Assignment and Voltages

If the power supply (option: B14L-5105-0100A) is used, the following power cable is provided. (refer to Figure 3-6-3)

Specification: B660-0625-T327A or
B660-1995-T041A (with DC Fan Unit)

Specify the length of the power cable as follows [for 50 cm (example)] :

B660-0625-T327A	#L500R0
Cable specification	500 x 10^0 (mm)

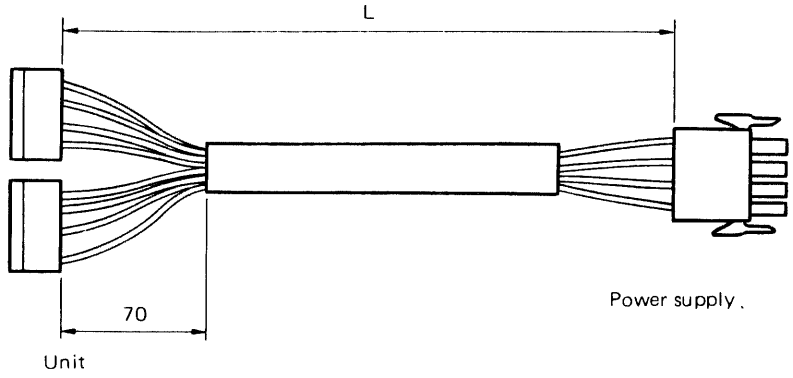


Figure 3-6-3 Power Cable (Specification: B660-0625-T327A)

Note: To ease the installation of the D.C. Power Cable at CN9 and CN10; loosen the two CZFM hold-down screws (screws 'B' in figure 6-5-3).

3.6.3 Interface Cabling

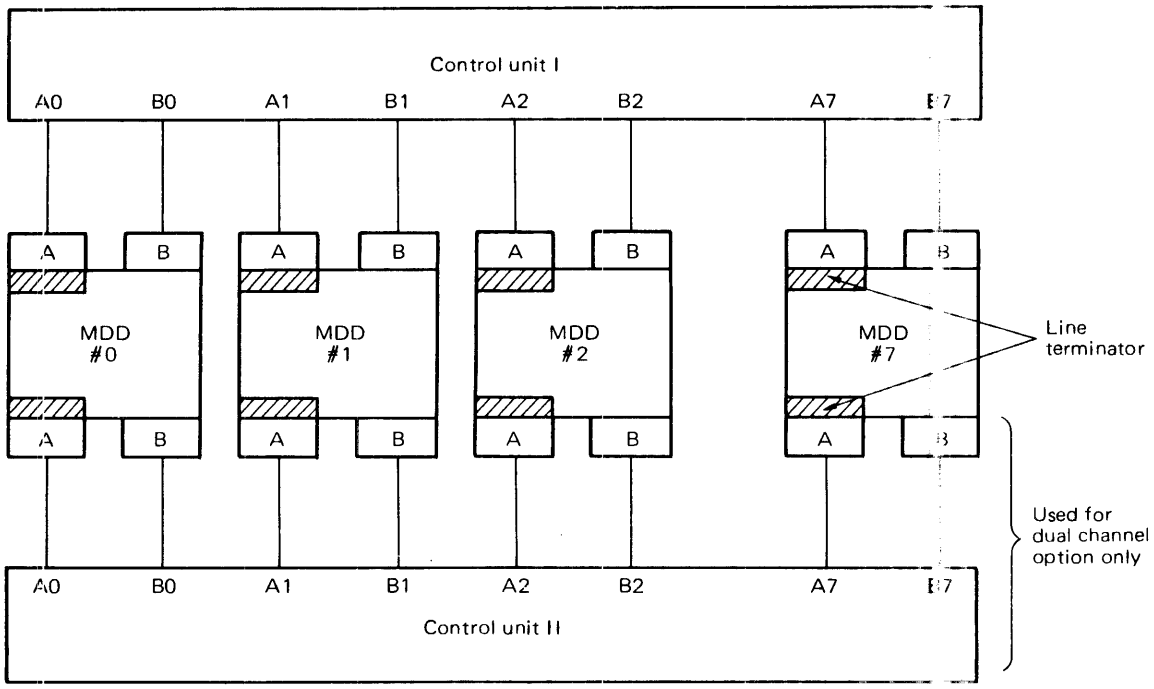
Interface cables include cable (A) (60P) for control signals and cable (B) (26P) for data signals.

(1) Cabling

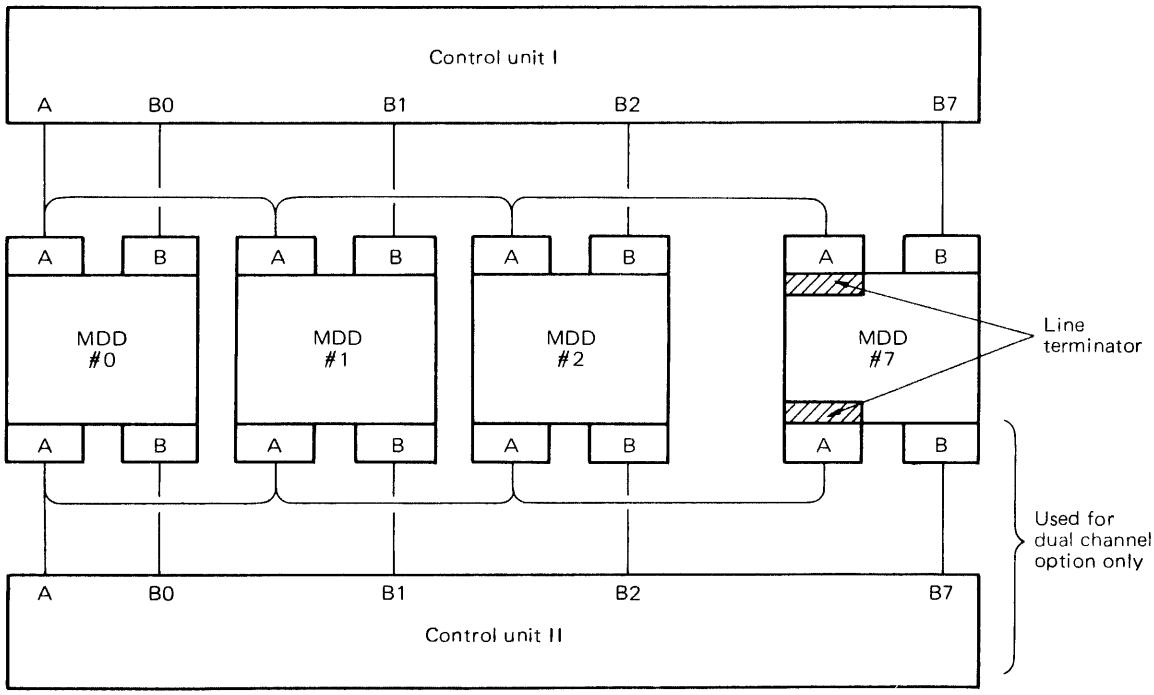
Cables are connected with the system in the star (radial) mode or the daisy-chain mode, as shown in Figure 3-6-4. For the star mode, the line terminator for cable (A) is necessary for every device. For the daisy chain mode only the last device requires a line terminator.

The unit side of cables (A) and (B) use right angled connectors which have no malinsertion preventive keys. Insert the cable to match the triangular marks on the connectors, (at the number one) shown in Figure 3-6-5. Then lock them from both sides with the locking lever.

If an optional fan unit is used, fix cables (A) and (B) at the upper section of the fan unit, (as shown in Figure 3-5-18) using the fan cover/strain relief.



a) Star-chain cabling



b) Daisy-chain cabling

Figure 3-6-4 System Interface Cabling

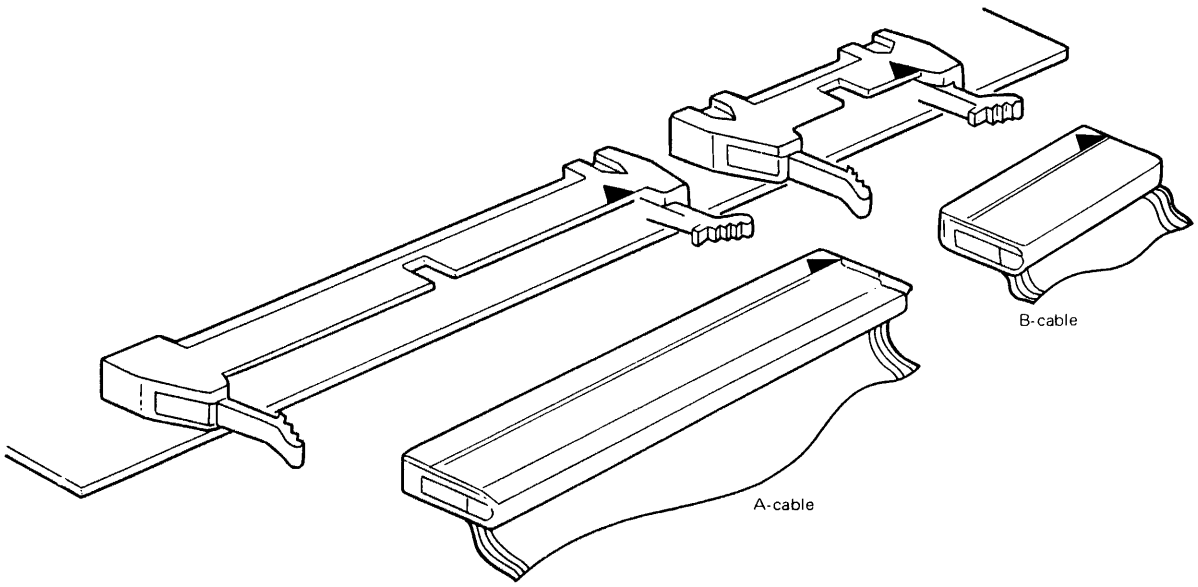


Figure 3-6-5 Interface Cabling

(2) Cable Termination

In the daisy-chain configuration, (A) cable signals must be terminated at the last disk drive with four IC module-resistors packs as shown in Figure 3-6-6. The four IC module resistors packs are installed in all disk drives; therefore they must be removed from the disk drives on which the line termination is unnecessary.

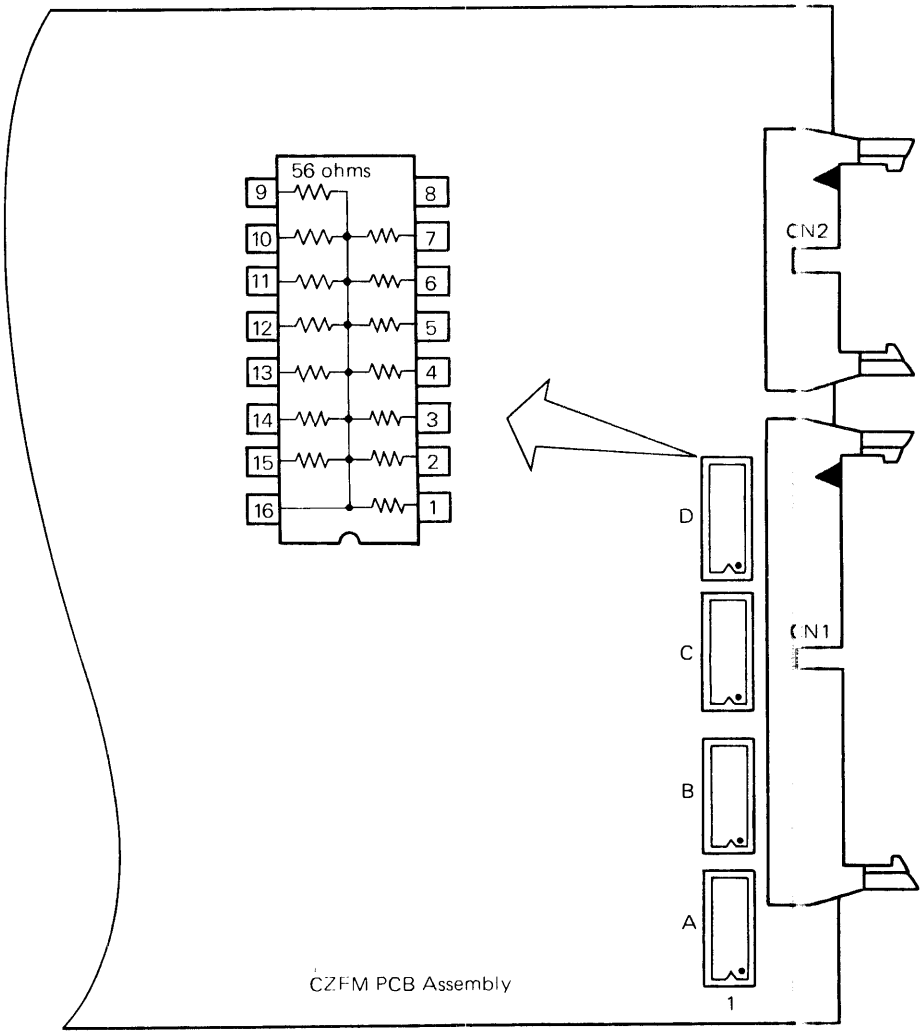


Figure 3-6-6 Cable Termination

3.6.4 System Grounding

(1) This drive unit is uniformly grounded at the signal ground (SG) connector. If FG and SG connection is required on the system, use the SG tap at the back of the unit, shown in Figure 3-6-7.

The optional AC fan unit (B03B-4740-E002A, -E003A) is grounded at the FG (Frame ground) connector, the SG (Signal ground) is separated from the FG (Frame ground) with insulating bushings.

A grounding cable may be connected as shown in Figure 3-6-8, if it is required.

(2) The FG and SG terminals are provided with the optional power supply unit. Connecting or disconnecting FG and SG on the power supply unit can be performed according to system power distribution and system ground requirements.

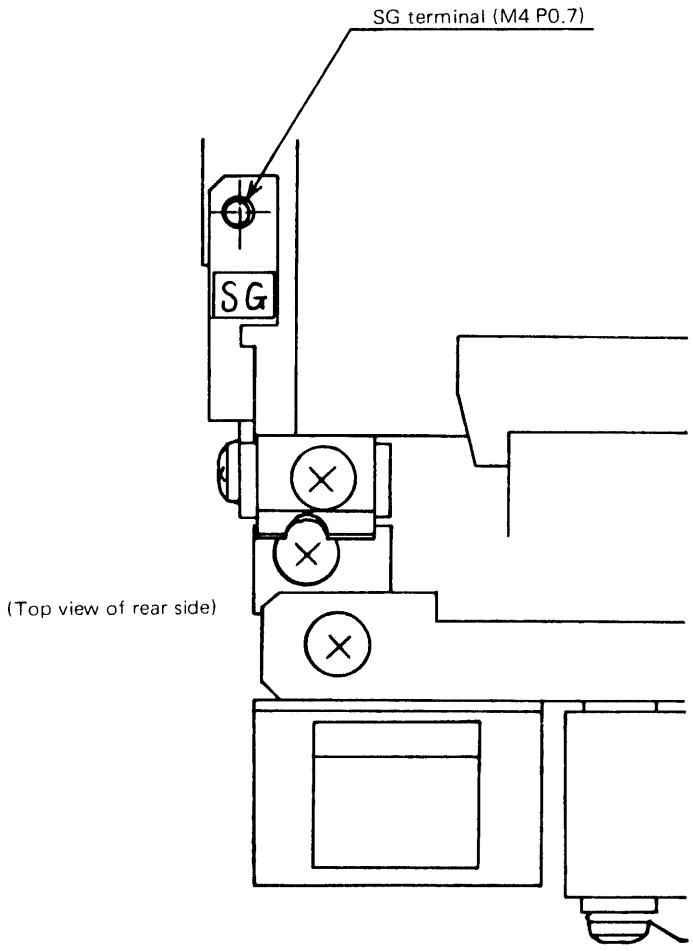


Figure 3-6-7 SG Terminal

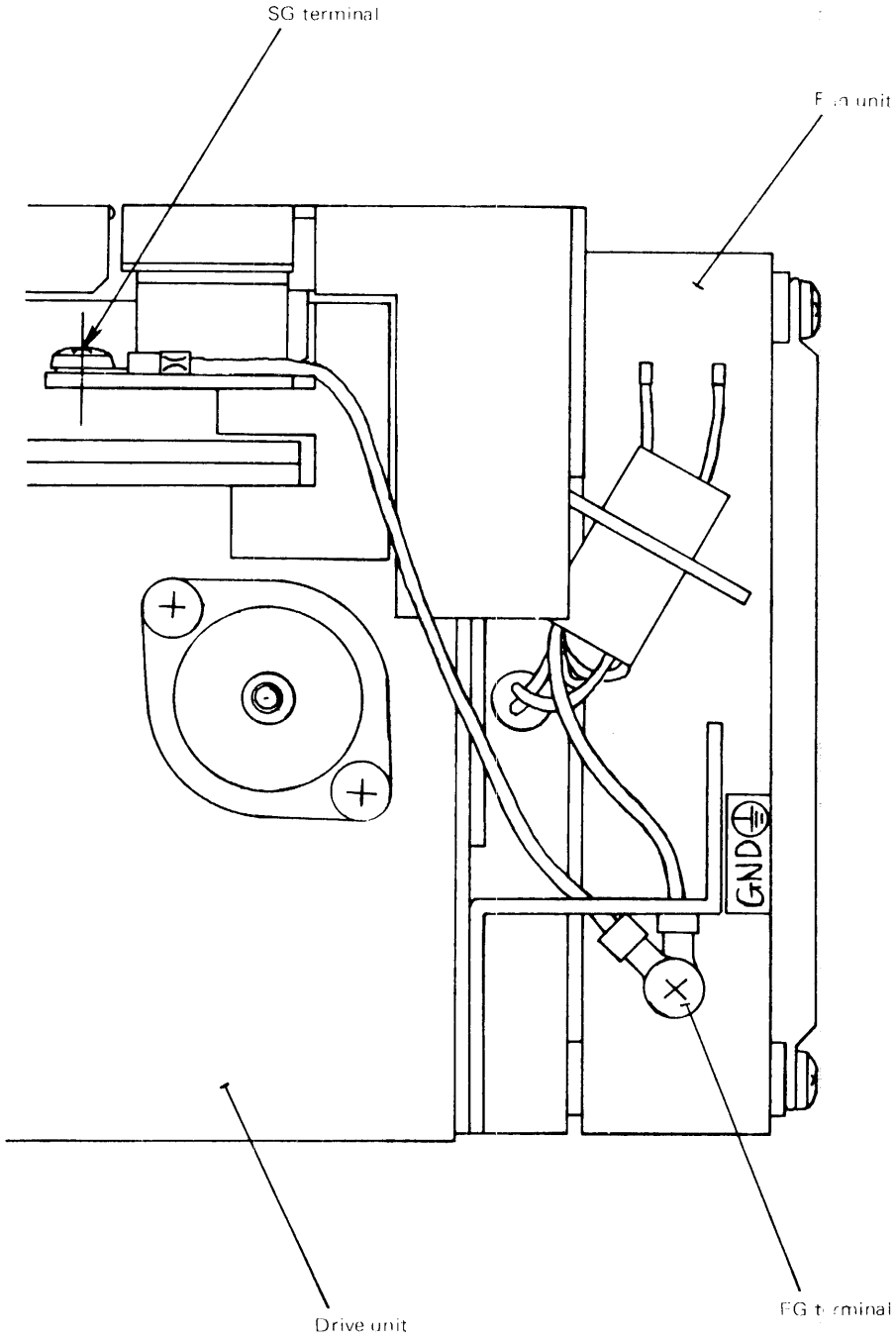


Figure 3-6-8 FG/SG Connection

3.7 MODE SELECT SETTING

When the M232X Micro Disk Drive is installed in the system, the customer must set switch 1 through 3 according to system requirements; these switches determine, Disk Logical Unit Number, Sector Mode, Tag 4/5 Enable, File Protect and Sector Counting, Switch 1 through Switch 3 are located on the CZFM PCB Assembly, as shown in Figure 3-7-1.

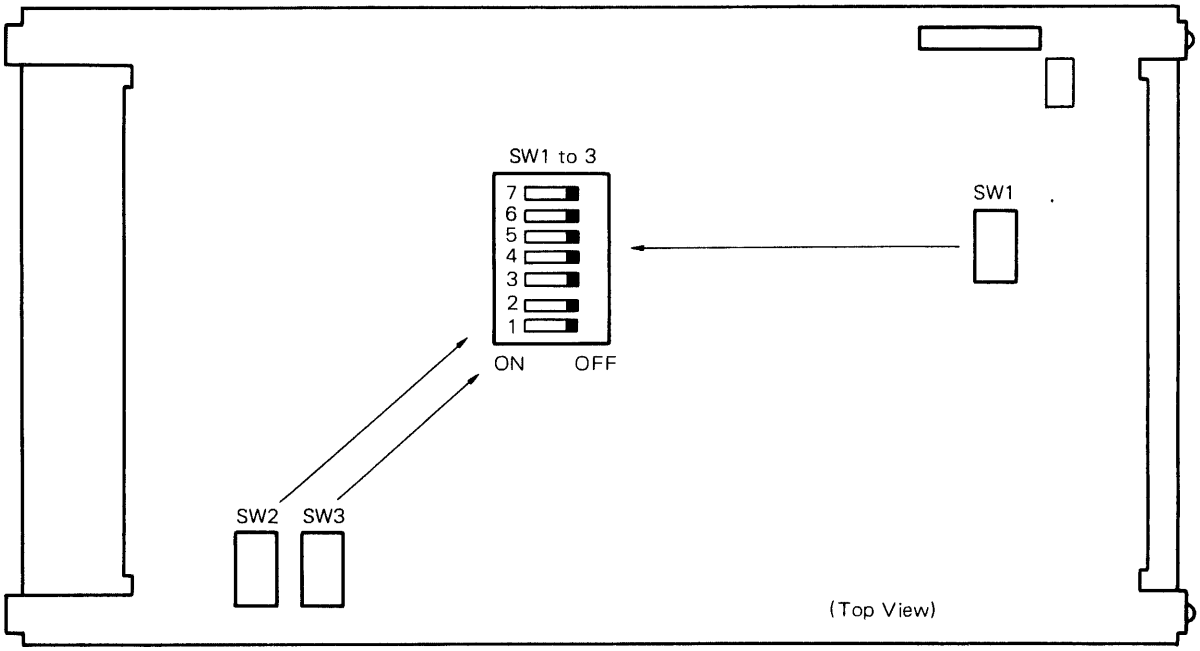


Figure 3-7-1 Mode Select Switch Location

3.7.1 Disk Addressing

Disk Logical Unit Number 0 to 7 is selected by SW1 at location E3 on the CZFM PCB assembly. Set the desired disk address with the three keys on SW1 using the binary code as shown in Table 3-7-1.

Table 3-7-1 Disk Addressing

Disk Address	Key 1	Key 2	Key 3
	2^1	2^2	2^3
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

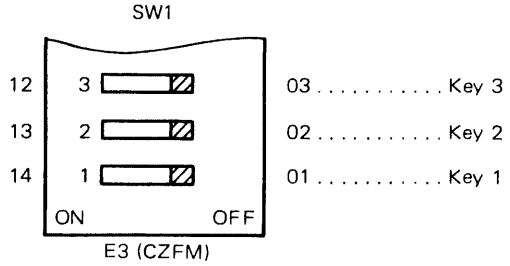


Figure 3-7-2 Disk Addressing

3.7.2 Sector Mode

The customer can select Hard Sector mode (1 to 128 sectors) or Variable Soft Sector mode, using Key 6 on SW1 at location E3 on the CZFM PCB assembly according to Table 3-7-2 as shown in Figure 3-7-3.

In the case of Hard Sector, the customer must set the number of sectors per disk revolution as described in Section 3.7.7. Setting the number of sectors per revolution is also available in the Variable Soft Sector mode.

Table 3-7-2 Sector Mode

Sector Mode	Key 6
Hard Sector	OFF
Variable Soft Sector	ON

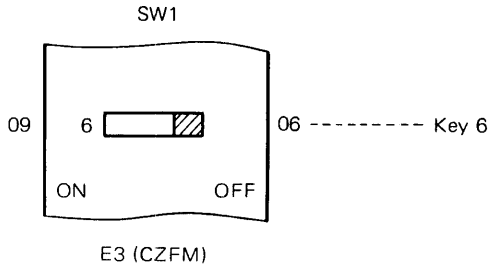


Figure 3-7-3 Sector Mode

3.7.3 Tag 4/5 Enable

The M232X provides optional Tag 4 and Tag 5 functions. The customer may disable or enable these optional functions using Key 5 on SW1 at location E3 on the CZFM PCB assembly. Refer to Figure 3-7-4. Disabling the Tag 4 and Tag 5 functions inhibits the receivers of Tag 4 and Tag 5 on the interface.

Table 3-7-3 Tag 4/5 Enable

Tag 4/5	Key 5
Disable	OFF
Enable	ON

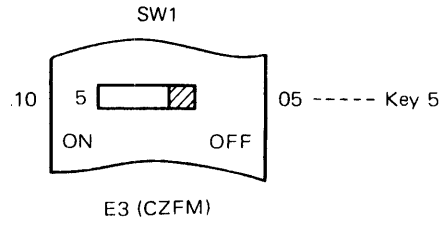


Figure 3-7-4 Tag 4/5 Enable

3.7.4 File Protect

When the customer desires to inhibit the write operation, the File Protect key may be set to the On position, using Key 7 on SW1 at location E3 on CZFM PCB assembly. Refer to Figure 3-7-5.

Table 3-7-4 File Protect

File Protect	Key 7
Enable writing	OFF
Disable writing	ON

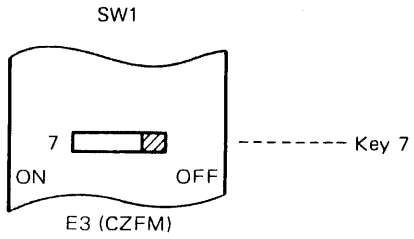


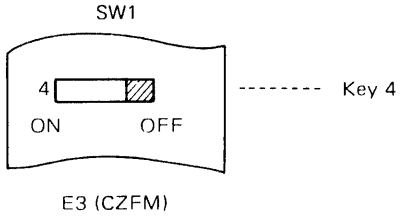
Figure 3-7-5 File Protect

3.7.5 Device Type (optional)

The device type, M2321K or M2322K, can be selected by setting key 4 on SW1.

Table 3-7-5 Device Type

Device Type	Key 4
M2321	OFF
M2322	ON



Note) Tag 4/5 feature must be enabled to obtain device type code.

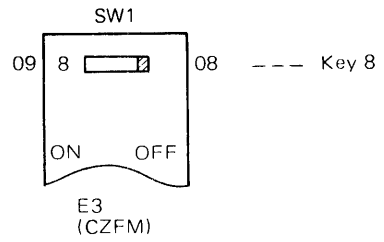
Figure 3-7-6 Device Type

3.7.6 ON END Switch

The customer can select on-end mode or other mode (Horizonal or Vertical), using Key 8 on SW1 at location E3 on the CZFM PCB assembly according to Table 3-7-6.

Table 3-7-6 On-end Switch

Mount Mode	Key 8
On-end	ON
Other	OFF



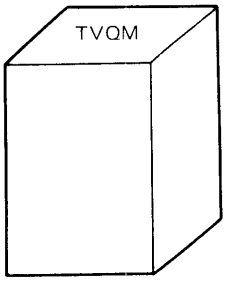


Figure 3-7-7 On End Installation

3.7.7 Sector Counting

Sector count configuration switches SW2 and SW3 are located at A26 and A24 respectively on the CZFM PCB assembly. Each key of SW2 and SW3 represents the binary powers of the Byte Clock as shown in Table 3-7-7.

Table 3-7-7 Sector Counting Keys

SW2 Key No.	Value	SW3 Key No.	Value
1	1	1	128
2	2	2	256
3	4	3	512
4	8	4	1024
5	16	5	2048
6	32	6	4096
7	64	7	8192

SW2 and SW3 keys must be set according to the number of bytes per sector. Knowing that the number of bytes possible on a track equals 20,480, any sectoring requirement from 1 to 128 sectors per track can be configured using the following formulas:

(1) Calculation based on Sectors/Track

$$1)\ \frac{20{,}480}{\text{Number of sectors}} = \text{Number of bytes per sector}$$

EXAMPLE
(Calculations for 9 Sectors)

$$\frac{20{,}480}{9} = 2{,}275.555$$

2) If the above calculation results in a remainder, truncate the remainder and add one to the integer portion of "number of bytes per sector".

2,275 + 1 = 2,276

EXAMPLE
(Calculations for 9 Sectors)

3) Configure SW2 and SW3 to "number of bytes per sector" minus one to allow for sector counter reset clock.

2,276 − 1 = 2,275

2,275 = 2,048 + 128 + 64 + 32 + 2 + 1

Keys must be "ON": Key # 5 1 7 6 2 1

SW3 SW2

4) To determine how many bytes (if any) the last sector of each track will be short, multiply "number of bytes per sector" by "number of sectors" and subtract 20,480.

2,276 x 9 = 20,484
−20,480

Last sector short 4 bytes

(2) Calculation based on Bytes/Sector

Example: 583 Bytes/Sector

1) Calculate the value to be set. = 16,384 − (Byte/Sector)
(Particular Value)
= 16,384 − 583
= 15,801

2) Select the keys must be OFF position referring to Table 3-7-7 after the following calculation.

15,801=8,192+4,096+2,048+1,024+256+128+32+16+8+1

Keys must be "OFF": 7 6 5 4 2 1 6 5 4 1

SW3 SW2

3) Calculate the Sectors/Track

$$\text{Sectors/Track} = \frac{\text{Bytes/Track}}{\text{Bytes/Sector}}$$

$$= \frac{20{,}480}{583}$$

= 35,129

4) If the above calculation results in a remainder, truncate the remainder. The integer portion means actual sectors per track.

Actual Sectors/Track = 35

5) Calculate the number of the last sector (remainder).

Last Sector Length = 20,480 − (Bytes/Sector) x (Sectors/Track)
= 20,480 − 583 x 35
= 75

Table 3-7-8 Commonly Used Sector Counting

Sector	SW2							SW3							Byte Sector	Last Sector Shorter
	1	2	3	4	5	6	7	1	2	3	4	5	6	7		
1															20,480	0
2	1	1	1	1	1	1	1	1	1	1	1	0	0	1	10,240	0
3	0	1	0	1	0	1	0	1	0	1	0	1	1	0	6,827	—1
4	1	1	1	1	1	1	1	1	1	1	0	0	1	0	5,120	0
5	1	1	1	1	1	1	1	1	1	1	1	1	0	0	4,096	0
6	1	0	1	0	1	0	1	0	1	0	1	1	0	0	3,414	—4
7	1	0	1	1	0	1	1	0	1	1	0	1	0	0	2,926	—2
8	1	1	1	1	1	1	1	1	1	0	0	1	0	0	2,560	0
9	1	1	0	0	0	1	1	1	0	0	0	1	0	0	2,276	—4
10	1	1	1	1	1	1	1	1	1	1	1	0	0	0	2,048	0
11	1	0	1	0	0	0	1	0	1	1	1	0	0	0	1,862	—2
12	0	1	0	1	0	1	0	1	0	1	1	0	0	0	1,707	—4
13	1	1	1	0	0	1	0	0	0	1	1	0	0	0	1,576	—8
14	0	1	1	0	1	1	0	1	1	0	1	0	0	0	1,463	—2
15	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1,366	—10
16	1	1	1	1	1	1	1	1	0	0	1	0	0	0	1,280	0
17	0	0	1	0	1	1	0	1	0	0	1	0	0	0	1,205	—5
18	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1,138	—4
19	1	0	1	0	1	1	0	0	0	0	1	0	0	0	1,078	—2
20	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1,024	0
21	1	1	1	1	0	0	1	1	1	1	0	0	0	0	976	—16
22	0	1	0	0	0	1	0	1	1	1	0	0	0	0	931	—2
23	0	1	0	1	1	1	1	0	1	1	0	0	0	0	891	—13
24	1	0	1	0	1	0	1	0	1	1	0	0	0	0	854	—16
25	1	1	0	0	1	1	0	0	1	1	0	0	0	0	820	—20
26	1	1	0	0	1	0	0	0	1	1	0	0	0	0	788	—8
27	0	1	1	0	1	1	1	1	0	1	0	0	0	0	759	—13
28	1	1	0	1	1	0	1	1	0	1	0	0	0	0	732	—16
29	0	1	0	0	0	0	1	1	0	1	0	0	0	0	707	—23
30	0	1	0	1	0	1	0	1	0	1	0	0	0	0	683	—10
31	0	0	1	0	1	0	0	1	0	1	0	0	0	0	661	—11
32	1	1	1	1	1	1	1	0	0	1	0	0	0	0	640	0
33	0	0	1	1	0	1	1	0	0	1	0	0	0	0	621	—13
34	0	1	0	1	1	0	1	0	0	1	0	0	0	0	603	—22
35	1	0	0	1	0	0	1	0	0	1	0	0	0	0	586	—30
36	0	0	0	1	1	1	0	0	0	1	0	0	0	0	569	—4
37	1	0	0	1	0	1	0	0	0	1	0	0	0	0	554	—18
38	0	1	0	1	1	0	0	0	0	1	0	0	0	0	539	—2
39	1	0	1	1	0	0	0	0	0	1	0	0	0	0	526	—34
40	1	1	1	1	1	1	1	1	1	0	0	0	0	0	512	0
41	1	1	0	0	1	1	1	1	1	0	0	0	0	0	500	—20
42	1	1	1	0	0	1	1	1	1	0	0	0	0	0	488	—16
43	0	0	1	1	1	0	1	1	1	0	0	0	0	0	477	—31
44	1	0	0	0	1	0	1	1	1	0	0	0	0	0	466	—24
45	1	1	1	0	0	0	1	1	1	0	0	0	0	0	456	—40
46	1	0	1	1	1	1	0	1	1	0	0	0	0	0	446	—36

Table 3-7-8 (Continued)

Sector	SW2							SW3							Byte Sector	Last Sector Shorter
	1	2	3	4	5	6	7	1	2	3	4	5	6	7		
47	1	1	0	0	1	1	0	1	1	0	0	0	0	0	436	—12
48	0	1	0	1	0	1	0	1	1	0	0	0	0	0	427	—16
49	1	0	0	0	0	1	0	1	1	0	0	0	0	0	418	—2
50	1	0	0	1	1	0	0	1	1	0	0	0	0	0	410	—20
51	1	0	0	0	1	0	0	1	1	0	0	0	0	0	402	—16
52	1	0	0	1	0	0	0	1	1	0	0	0	0	0	394	—8
53	0	1	0	0	0	0	0	1	1	0	0	0	0	0	387	—31
54	1	1	0	1	1	1	1	0	1	0	0	0	0	0	380	—40
55	0	0	1	0	1	1	1	0	1	0	0	0	0	0	373	—35
56	1	0	1	1	0	1	1	0	1	0	0	0	0	0	366	—16
57	1	1	1	0	0	1	1	0	1	0	0	0	0	0	360	—40
58	1	0	0	0	0	1	1	0	1	0	0	0	0	0	354	—52
59	1	1	0	1	1	0	1	0	1	0	0	0	0	0	348	—52
60	1	0	1	0	1	0	1	0	1	0	0	0	0	0	342	—40
61	1	1	1	1	0	0	1	0	1	0	0	0	0	0	336	—16
62	0	1	0	1	0	0	1	0	1	0	0	0	0	0	331	—42
63	1	0	1	0	0	0	1	0	1	0	0	0	0	0	326	—58
64	1	1	1	1	1	1	0	0	1	0	0	0	0	0	320	0
65	1	1	0	1	1	1	0	0	1	0	0	0	0	0	316	—60
66	0	1	1	0	1	1	0	0	1	0	0	0	0	0	311	—46
67	1	0	0	0	1	1	0	0	1	0	0	0	0	0	306	—22
68	1	0	1	1	0	1	0	0	1	0	0	0	0	0	302	—56
69	0	0	0	1	0	1	0	0	1	0	0	0	0	0	297	—13
70	0	0	1	0	0	1	0	0	1	0	0	0	0	0	293	—30
71	0	0	0	0	0	1	0	0	1	0	0	0	0	0	289	—39
72	0	0	1	1	1	0	0	0	1	0	0	0	0	0	285	—40
80	1	1	1	1	1	1	1	1	0	0	0	0	0	0	256	0
128	1	1	1	1	1	0	0	1	0	0	0	0	0	0	160	0

Notes: (1) "1" indicates that the key is set to ON side.
(2) "0" indicates that the key is set to OFF side.
(3) The last sector is equal or shorter than nominal sector.

3.8 SHIPPING

Perform the following operations when the M232XK is to be shipped mounted in a 19-inch rack.

(1) Secure the unit:
We recommend to attach a elastic material to the mounting-frame side near the rubber shock-isolator, so that excessive force is not applied to the isolators.
Refer to 3.4.4 for securing the unit.

(2) This process is required so that the shock applied to the unit during shipment does not exceed 5G.

3.9 STORAGE AND REPACKING

When reshipping the unit, repack it in the original carton or a carton having equivalent functions.

When the environmental conditions are severe and the unit is to be stored for an extended period of time, it should be packed in its box.

Units can be stacked three cartons high.

When storing unpacked units, avoid locations that are dusty or subject to extreme environmental changes.

Section 4

Theory of Operation

4. THEORY OF OPERATION

4.1 GENERAL DESCRIPTION

The operation of the M232XK is divided into three parts. The first part (Section 4.2) describes the mechanical assemblies of the unit. The second part (Section 4.3 and 4.4) describes the magnetic heads and magnetic disks. The third part (Section 4.5 and 4.6) describes the interface, servo circuit, R/W control, and other electronic controls.

4.2 MECHANICAL ASSEMBLIES

4.2.1 Disk Enclosure

The Disk Enclosure (DE) is a completely sealed unit containing the disks, spindle, actuator, and heads.

The DE is sealed at the factory and must not be opened in the field.

4.2.2 Air Circulation in DE

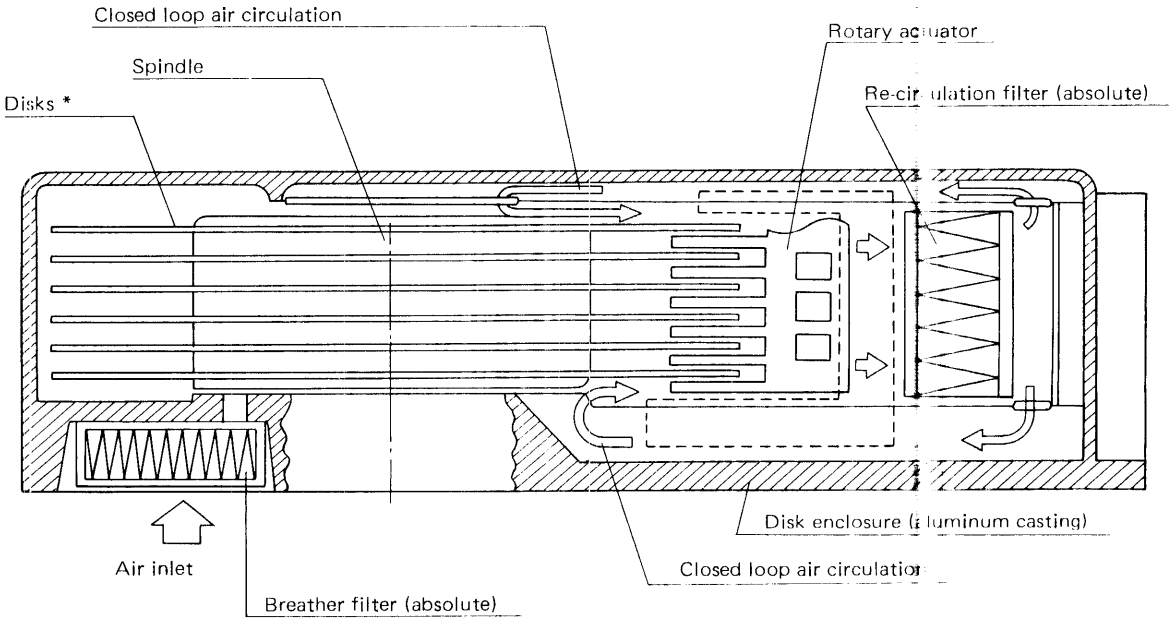
As the Contact stop/start (CSS) head used in this disk unit has a very low flying height (approximately 0.35μm), head crashes can be caused by microscopic foreign particles. To keep the inside of the DE clean, the enclosure is completely sealed and clean air is supplied through two fileters. A breather filter is used for external air intake, while a re-circulation filter keeps the air inside the DE clean. Refer to Figure 4.2.1.

The breather filter is used for the following purposes:

(a) Prevention of negative pressure in the vicinity of the spindle when the disk begins to rotate.

(b) Prevention of dust intake when the air in the DE contracts due to a temperature difference between the DE and its environment.

The re-circulation filter, attached to the closed loop duct in the DE, is used to keep the air free of foreign particles. When a pressure difference is caused in the DE by the rotation of the spindle, the air in the DE circulates through the closed loop. Because it continually passes through this filter, the air is always kept clean. These two filters can remove 99.97% of the dust particles (0.3μm min.).



M2321 contains 3 disks in DE
M2322 contains 6 disks in DE

Figure 4-2-1 Air Circulation Inside DE

4.2.3 Spindle Drive Motor

The spindle/drive motor is an integral part of the chassis. It consists of seven major components: Shaft, Hub, Bearings, Stator, Rotor, Antistatic Brush, and Speed Sensor. Refer to Figure 4.2.2. The motor shaft is fixed within the motor housing by upper and lower bearings which are sealed to prevent contamination of the disk platter environment. The stator is fixed to the outer radius of the cast motor housing. The hub is fixed to the top of the motor shaft. The rotor and disk platters are fixed to the hub. The antistatic brush contacts the bottom of the motor shaft and dissipates any electrostatic noise to the chassis. Hall-effect sensors detects hub movement. The signal produced by this sensor is compared with an oscillator clock on the PCB in order to maintain the normal RPM rotational speed of 3,600 RPM, the special range.

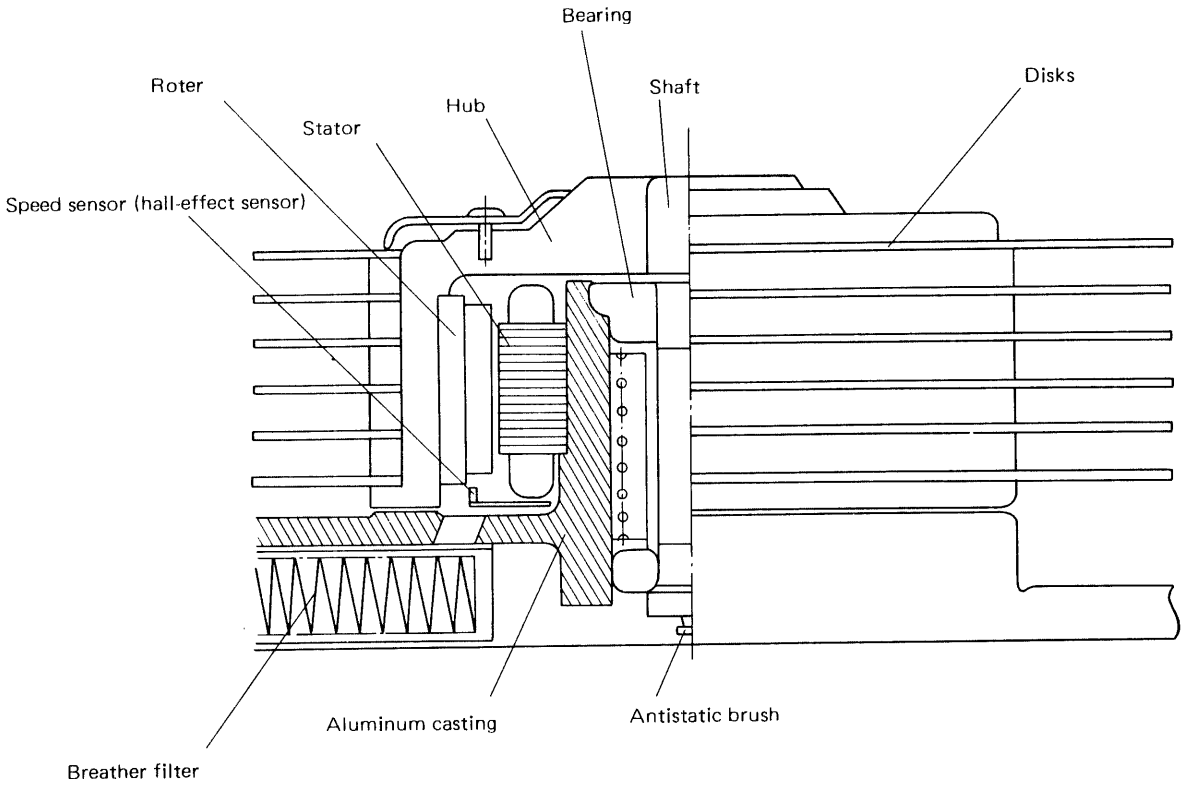


Figure 4-2-2 Spindle Drive Motor

4.2.4 Actuator Arm Assembly

A low-power-consumption, rotary-type actuator is used to move the data heads and servo head along a circular arc to the specified cylinder. A moving coil is attached to the other end of the actuator arm and moves freely between fixed permanent magnets without contact. When current is applied to the coil, the coil and magnets interface and the actuator moves around the pivot. Refer to Figure 4.2.3.

The actuator performs the following types of motion, which are controlled by servo feed-back current from the servo head.

(1) Seek
Heads are moved to the specified cylinder while counting track-crossing signals.

(2) On Cylinder
Heads follow the specified tracks. The servo system prevents mispositioning due to disturbances such as shock, vibration, or temperature changes.

The servo head is located on the lower surface of the bottom disk, where servo information is pre-written at the factory.

This servo information is used as a control signal for the actuator; that is, it provides track-crossing signals during a seek operation, track following signals during On Cylinder operation, and timing information such as index and servo clock.

The heads are in contact with the disk surfaces during start and stop (CSS) at a fixed position called the landing zone. This zone is on the innermost area of the disk, separate from the recording zone. A spring force holds or fixes the actuator at this position. If no current is applied to the moving coil, the heads are fixed at the landing zone to prevent CSS in the recording zones.

Once the disks attain the required rotational speed, an initial seek function occurs. Current then flows in the coil and the heads are released from the landing zone and moved to Cylinder 0.

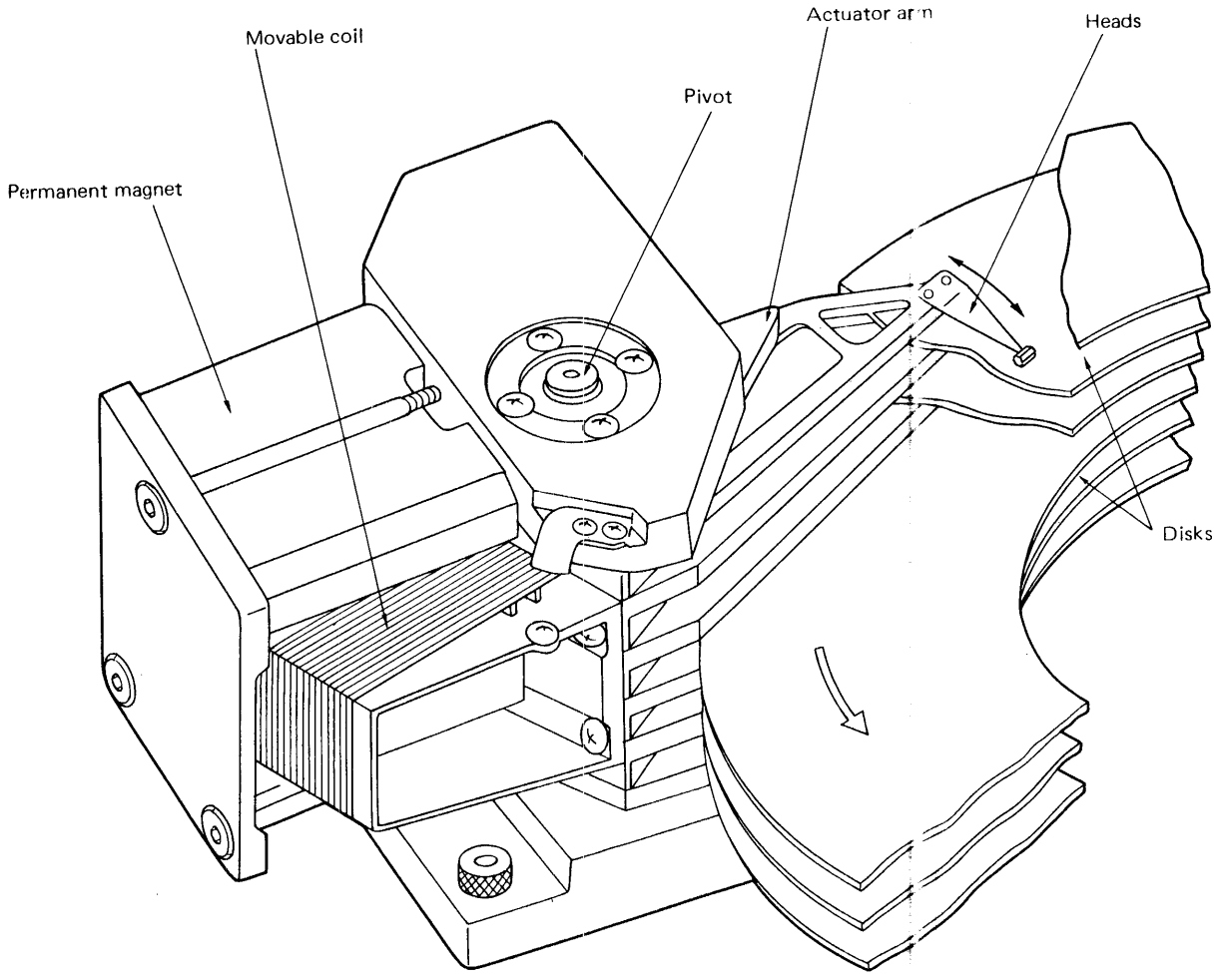


Figure 4-2-3 Actuator Arm Assembly

4.3 MAGNETIC HEADS AND RECORDING MEDIA

4.3.1 Magnetic Heads

To accomplish high density recording, Contact Start/Stop (CSS) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The CSS system differs from the conventional ramp-load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Since, the head and disk make contact, the wear caused by this contact must be minimized. Therefore, the CSS heads are lightly loaded and surface pressure is reduced by using a tapered flat slider such as that shown in Figure 4-3-2. The slider has three rails. The air intake end of the slider is tapered to obtain lift from the air flowing over the disk surface. Read and write are performed by a ferrite core at the rear of the head, the minimum flying height position.

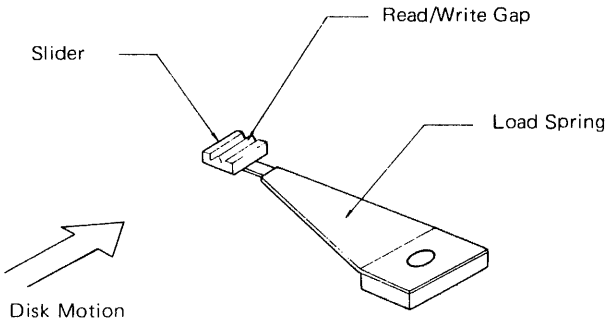


Figure 4-3-1 Read/Write Head

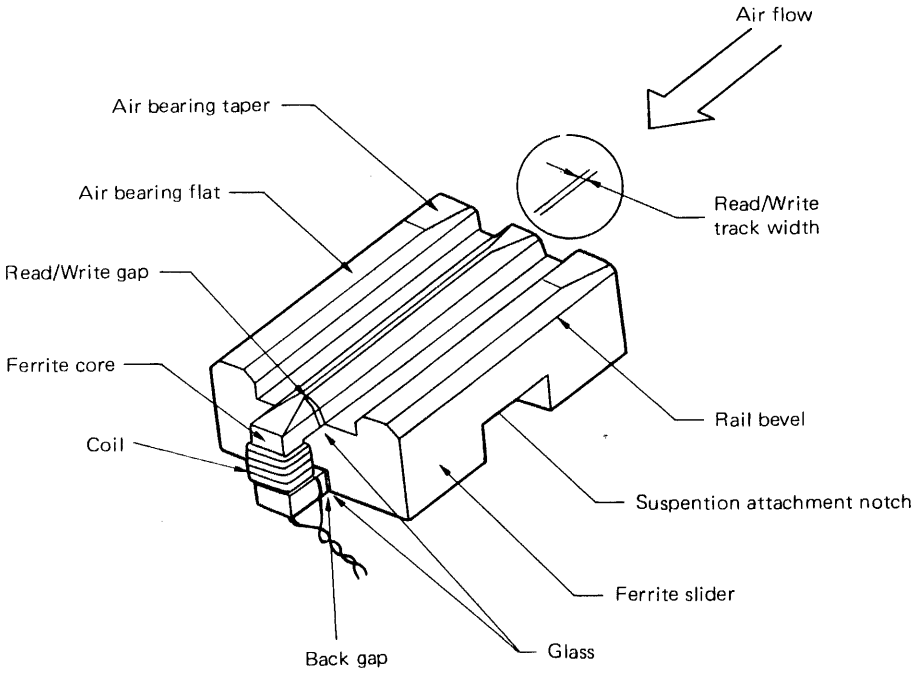


Figure 4-3-2 Tapered Flat Slider

4.3.2 Recording Media (Magnetic Disk)

The data recording media are aluminum disks approximately 210 mm (8 1/4 inches) in diameter and approximately 2 mm (75 mil) thick, and are coated with a magnetic material. Since the M232XK employs CSS heads, to prevent wear the surface is coated with a special material. Up to six disks can be installed for a maximum storage capacity of 168.8 MB. The bottom surface of the lowest disk is for the servo area, on which the positioning data and clock signals are recorded.

4.3.3 Servo Track Format

4.3.3.1 Servo track configuration

The servo area is used to store the unique data patterns which generate the Track Positioning, Index, Guard Band, and Clock signals. This data is recorded on the disk before the unit is shipped from the factory.

The servo area consists of a combination of ODD1, ODD2 EVEN1 and EVEN2 tracks. The physical placement of servo tracks is shown in Figure 4-3-3. The servo tracks are divided into the following five parts:

(1) Dead Space (DS or Landing Zone)
Dead Space is used for head contact during start and stop. DS consists of five DC-erased tracks and is recognized as Head Unloaded through the servo circuit.

(2) Inner Guard Band 2 (IGB2)
Inner Guard Band 2 is used for speed control during RTZ or Initial seek sequence. IGB2 consists of six EVEN1–EVEN2 tracks, six ODD1–EVEN2 tracks, six ODD1 – ODD2 tracks and six EVEN1 – ODD2 tracks (24 tracks total).

(3) Inner Guard Band 1 (IGB1)
Inner Guard Band 1 is located between IGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence. IGB1 consists of four EVEN1–EVEN2 tracks, four ODD1–EVEN2 tracks, four ODD1–ODD2 tracks and four EVEN1–ODD2 tracks (16 tracks total).

(4) Servo Band
Servo Band is used for tracking to determine the center of each cylinder. The Servo Band consists of 207 EVEN1 – EVEN2 tracks, 206 ODD1 – EVEN2 tracks, 206 ODD1 – ODD2 tracks, and 207 EVEN1 – ODD2 tracks (826 track total). However, 1-½ inner tracks of Cylinder 0 and 1-½ outer tracks of Cylinder 822 are not utilized for corresponding data tracks.

(5) Outer Guard Band (OGB)
The Outer guard Band is used to recognize that the head has passed through the servo zone in an outward direction. OGB consists of three EVEN1 – EVEN2 tracks, three ODD1 – EVEN2 tracks, three ODD1 – ODD2 tracks and three EVEN1 – ODD2 track minimum (12 tracks minimum total).

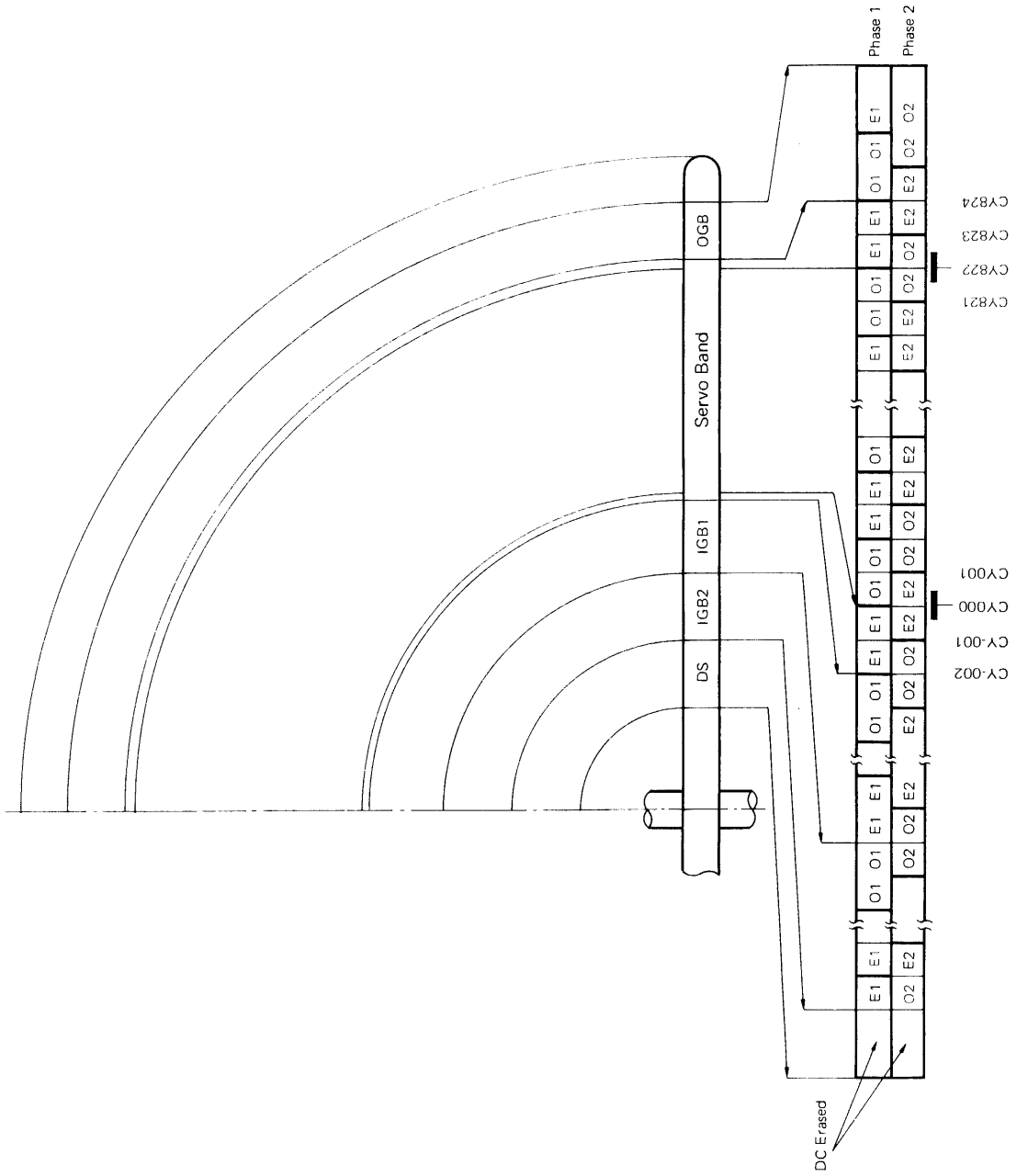


Figure 4-3-3 Servo Track Configuration

4.3.3.2 Servo pattern

The servo signal is a unique "Dual-phase composite servo signal" which creates a high-performance positioning system. It is used to achieve angular positioning (location with reference to the circumference of the disk) and radial positioning (location with reference to the radius of the disk).

Angular positioning is determined by a series of sync bits which are written on each track. Through a combination of Index Bit and Normal Bit; the "sync pattern" is developed. A series of unique sync patterns is written at the factory and used in the identification of specific disk regions. Refer to Figure 4-3-4 and Figure 4-3-5. Index mark, OGB, IGB1, and IGB2 patterns are described in paragraph 4.3.3.3.

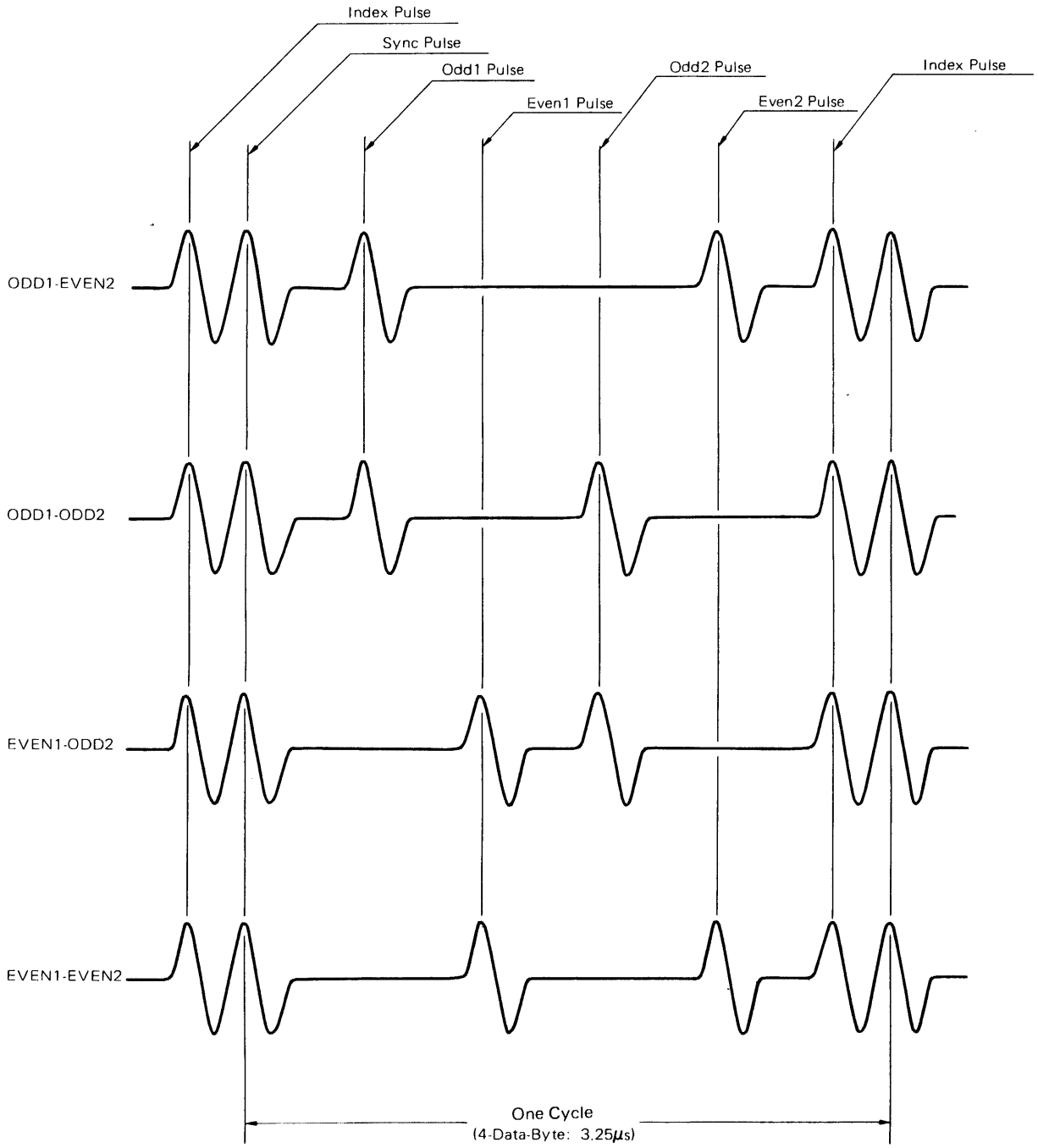


Figure 4-3-4 Normal Bit Pattern

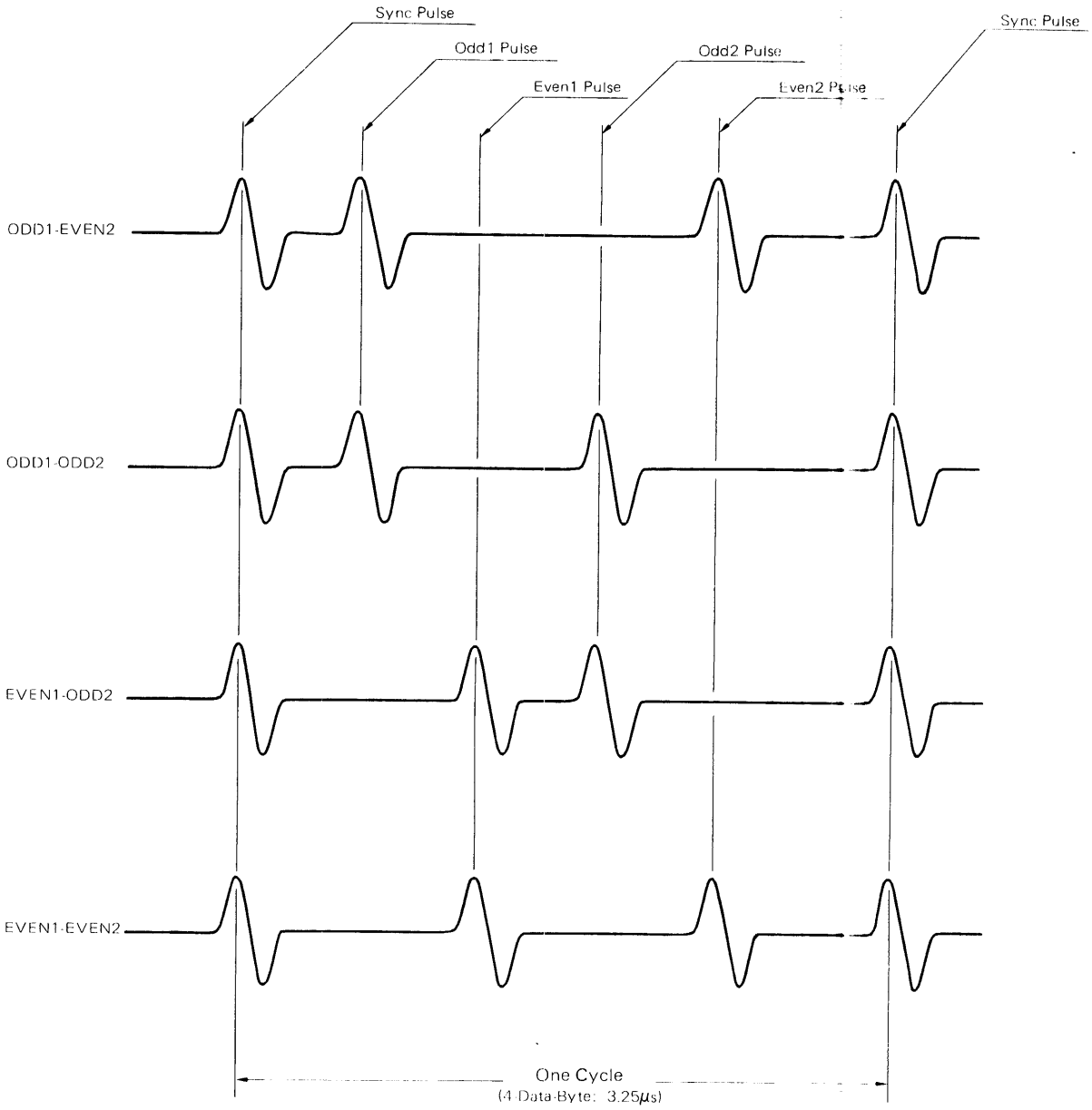


Figure 4-3-5 Index Bit Pattern

Radial positioning information is provided by writing ODD1–EVEN2, ODD1–ODD2, EVEN1–ODD2, and EVEN1–EVEN2 patterns, in that order, on the servo surface.

During head movement, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase 1), and between ODD2 and EVEN2 peaks (phase 2), and then converts them into two position signals (phase 1: Normal, phase 2: Quadruture) through the position sensing.

After head movement, the servo head, which has double the core width of the data head, settles on the border of two types of servo patterns controlled by the two least-significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN1 (or EVEN 2) peak by positioning the servo head on the center of the servo track. Refer to Figure 4-3-6.

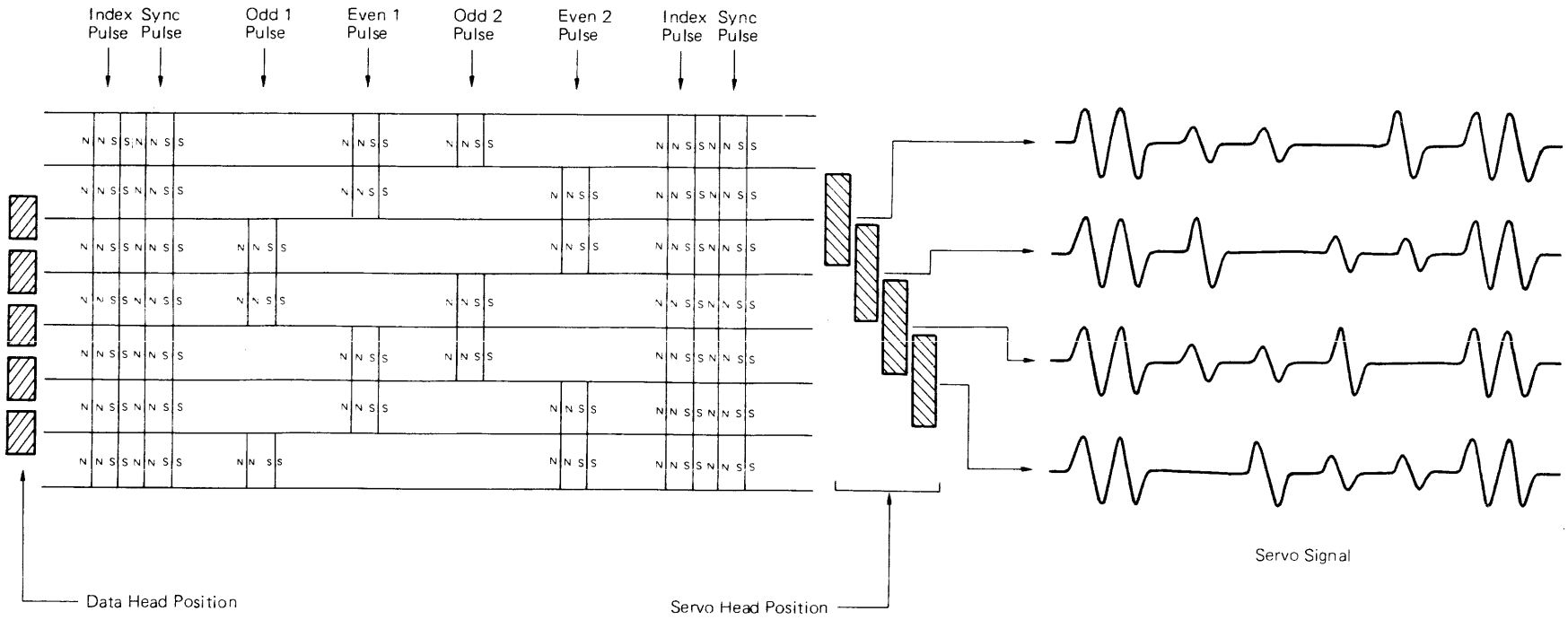


Figure 4-3-6 Dual-Phase Composite Servo Signal

4.3.3.3 Index, IGB2, IGB1 and OGB patterns

Index, IGB2, IGB1, and OGB patterns are detected by decoding the combination of Index bits and Normal bits. Each of the patterns are shown in Table 4-3-1.

Table 4-3-1 Index, IGB2, IGB1, and OGB Patterns

Signal	Pattern	Pattern interval
Index	01011	20,480 B (5,120-sync)
IGB2	01110	256 B (64-sync)
IGB1	01010	256 B (64-sync)
OGB	10011	256 B (64-sync)

Note: 0 — Normal bit
1 — Missing bit

4.3.4 Data Surface Format

The data surface consists of all the disk surfaces except the servo surface and is composed of three basic parts as follows:

(1) Landing Zone (LZ)
The Landing Zone is included in the area described as Behind Home (BH), but is specifically the area the heads contact during start and stop sequence. The Landing Zone corresponds to Dead Space (DS) on the servo surface.

(2) Behind Home (BH)
Behind Home (BH) is the transition area on both sides of the data tracks. It corresponds to IGB2, IGB1, or OGB on the servo surface.

(3) Data Track
The data track area consists of 823 cylinders for data recording, with Cylinder 0 being the inner-most track and Cylinder 822 being the outer-most track.

4.3.5 Head and Surface Configuration

The head and surface configuration for the M2321K and M2322K are given in Figures 4-3-7 and 4-3-8, respectively.

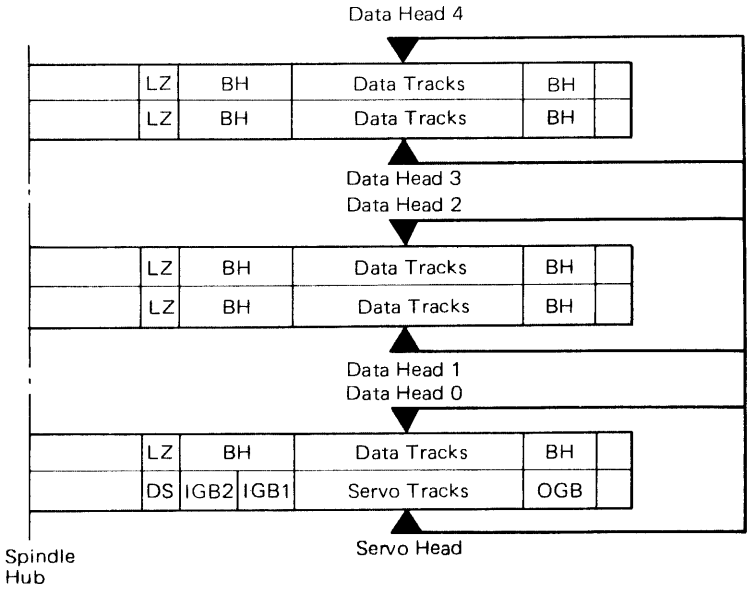


Figure 4-3-7 M2321 Surface Configuration

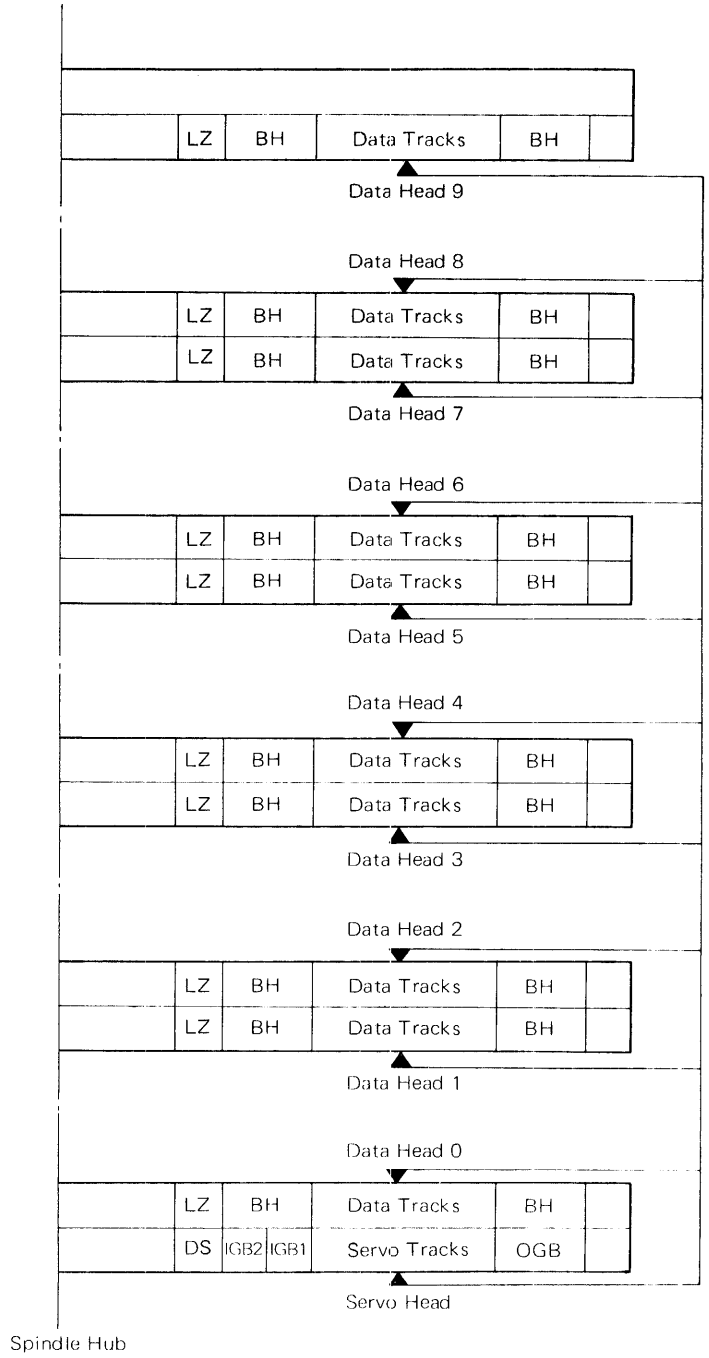


Figure 4-3-8 M2322 Surface Configuration

4.4 FORMAT

4.4.1 Description

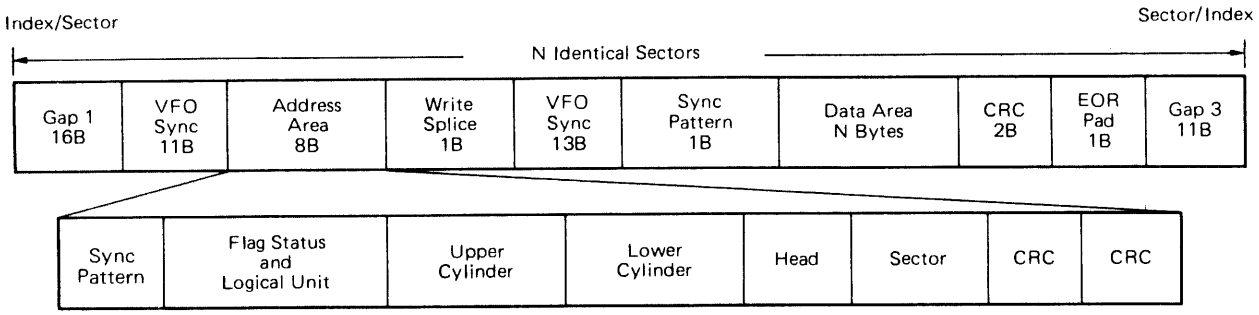
A "sector" is an area assigned an address on the disk. Each sector consists of an Address Area (AA) to confirm that the correct sector has been read, and a Data Area (DA) on which the actual data is recorded.

Index and sector pulses are used by the controller to find the beginning of the track and sector. Sector format is determined by the controller. Fixed Sector format or Variable Sector format can be used with the M232XK.

The recommended Fixed Sector format and Variable Sector format is as follows.

4.4.2 Fixed Sector Format

Refer to Figure 4-4-1.



Example: 64 Sectors/Track

$$\text{Data Area} = \frac{\text{Total Bytes/Track}}{\text{Sector/Track}} - (\text{Gap loss} + \text{Check Bytes})$$

$$= \frac{20480}{64} - 64 = 256 \text{ Bytes/Sector}$$

$$\text{Track Efficiency} = \frac{256 \times 64}{20480} \times 100 = 80\%$$

Notes: 1) This format is an example only and may be structured to suit individual requirements.

2) Sync Byte patterns for address and data areas may be different. It is recommended that Sync Byte patterns are $0E_{(Hex)}$ for address areas and $09_{(Hex)}$ for data areas.

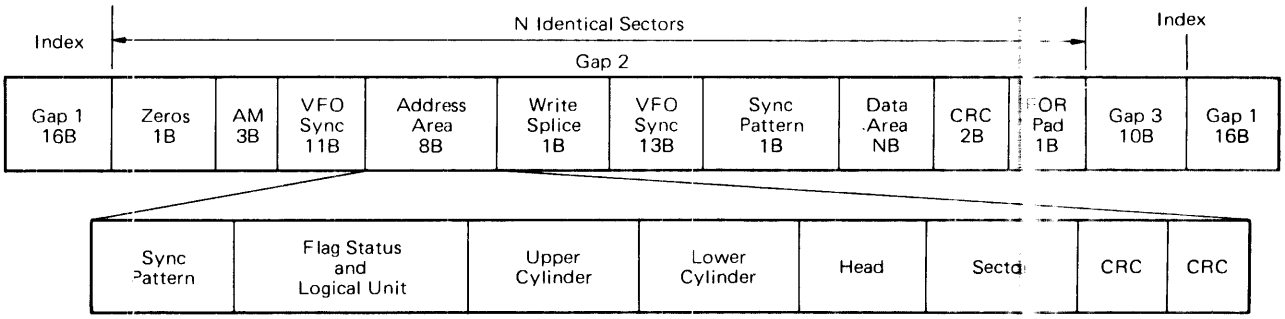
3) Data patterns for Gap 1, PLO sync, Write Splice, EOR Pad and Gap 3 are all "0".

4) Fixed sectors per track may be any number from 1 through 128 and can be selected by setting the configurator switches on the PCB assembly.

Figure 4-4-1 Fixed Sector Format

4.4.3 Variable Sector Format

Refer to Figure 4-4-2.



$$\text{Data Area} = \frac{\text{Total Bytes/Track} - \text{Index Loss}}{\text{Sectors/Track}} - (\text{Sync} + \text{Address Area})$$

Example 1: 64 Sectors/Track

$$\text{Data Area: } \frac{20480 - 26}{64} - 41 = 278 \text{ Bytes/Sector}$$

$$\text{Track Efficiency} = \frac{278 \times 64}{20480} \times 100 = 87\%$$

Example 2: 256 Bytes/Sector

$$\text{Sector Count} = \frac{20480 - 26}{256 + 41} = 68 \text{ Sectors/Track}$$

$$\text{Track Efficiency} = \frac{256 \times 68}{20480} = 85\%$$

Note: This format is an example only and may be structured to suit individual requirements.

Figure 4-4-2 Variable Sector Format

4.4.4 Description of Format Parameters

4.4.4.1 Fixed Sector Format

(1) Gap 1
Gap 1 allows for displacement of the head and circuit tolerances under worst case conditions. This gap must be a minimum of 16 bytes.

(2) VFO Sync
All "0" 's are written and used to synchronize the data from the disk and the read/write clock from the VFO circuits. This field must be 11 bytes.

(3) Sync Pattern Byte
The Sync pattern byte represents the start of the address area. It's function is the same as that before the data area, but the address area sync and data area sync byte may be different. The recommended patterns is "$0E_{(Hex)}$".

(4) Flag Status and Logical Unit Byte
Flag status and logical unit indicates the status of the disk on the sector. Normal record, primary record, or secondary record condition may be indicated. The specifications for this field is a function of the control unit.

(5) Upper Cylinder, Lower Cylinder
Upper/Lower cylinder indicates the cylinder address of the track.

(6) Head Address
Head address indicates the head address of the track.

(7) Sector Address
Sector address indicates the sector address.

(8) CRC (Cyclic Redundancy Check)
CRC is a check byte used to determine whether the data was read correctly.

(9) Write Splice
When the address and data areas are written separately, write splice is the location of the read/write head transitions.

(10) VFO Sync
All "0" 's are written and used to synchronize the data from the disk and the read/write clock from the VFO circuits.

(11) Sync Pattern
Sync pattern indicates the beginning of the data area. The recommended pattern is "$09_{(Hex)}$". Refer to (3) above.

(12) Data Area
Data area is where data is actually recorded.

(13) CRC
Same as (8) above for the data field.

(14) EOR Pad
EOR pad eliminates the possibility of destroying the end of a record written with a late displacement head.

(15) Gap 3
Gap 3 is a delay allowance for the control unit. It should be written all "0" 's.

4.4.4.2 Variable Sector Format

This format is written in the Variable Sector Mode. Refer to Figure 4-4-2. Address Mark (AM) is written, prior to the Address Area, to indicate the beginning of a sector, and the data field is written in whatever length necessary to accommodate the system. The Address Mark (AM) is a three-byte DC-erase area at the beginning of the sector format.

4.5 INTERFACE

4.5.1 Introduction

4.5.1.1 Purpose

This section describes the logical and physical specifications for signal transfer between the M232XK and the control unit.

4.5.1.2 Application

These specifications are applicable to both the M2321K (84 MB storage) and the M2322K (168 MB storage).

4.5.1.3 Connection

The external connection (for transmitting and/or receiving interface signals) consists of connectors, "A" and "B" which connect, respectively, to cables "A" and "B". "A" cables may be connected in a daisy-chain configuration. Therefore, a line terminator must be inserted for the "A" connector of the last device. "B" cables are connected in a star configuration. Therefore, the control unit requires "B" cables and connectors to match the number of units to be connected. Refer to Figure 4-5-1.

4.5.1.4 Time Specification

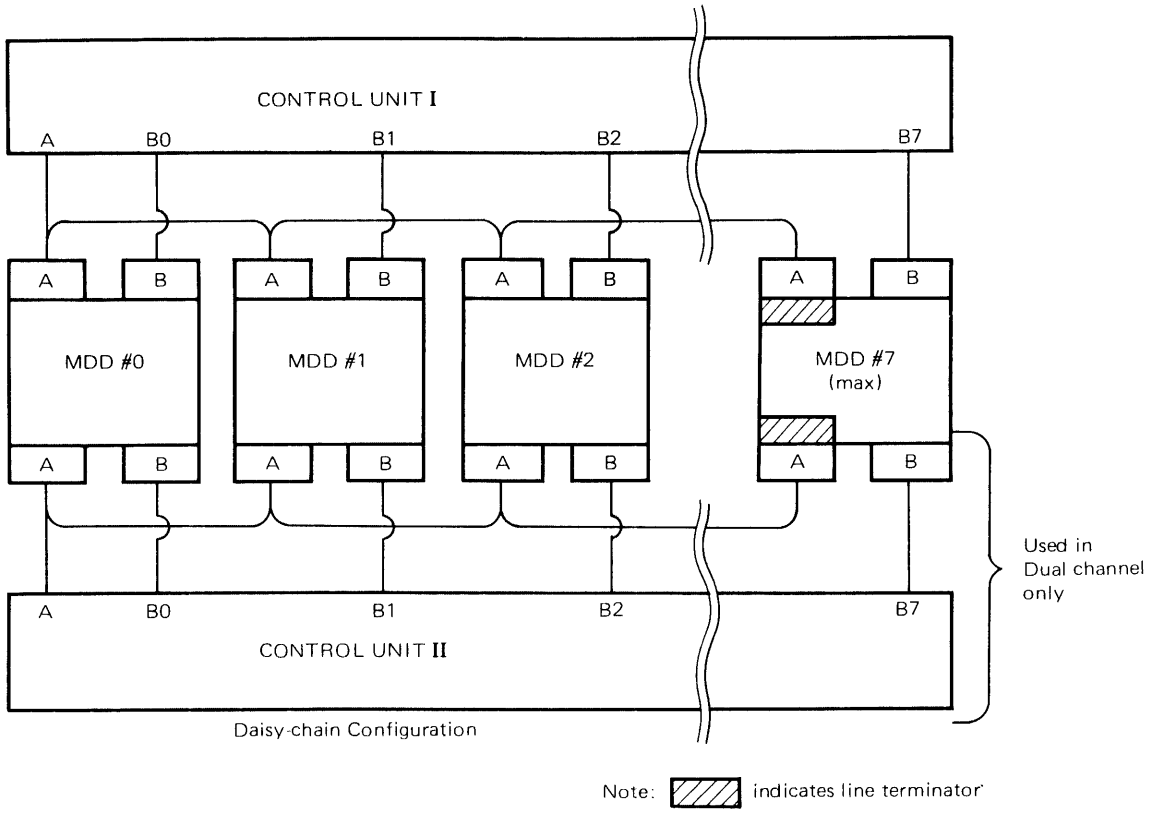
Timings are specified at the connector position of the M2322XK. Accordingly, it is necessary for signal timings to consider both the delay time of the interface cable and the circuits of the disk control unit.

4.5.1.5 Interface Transmitter/Receiver

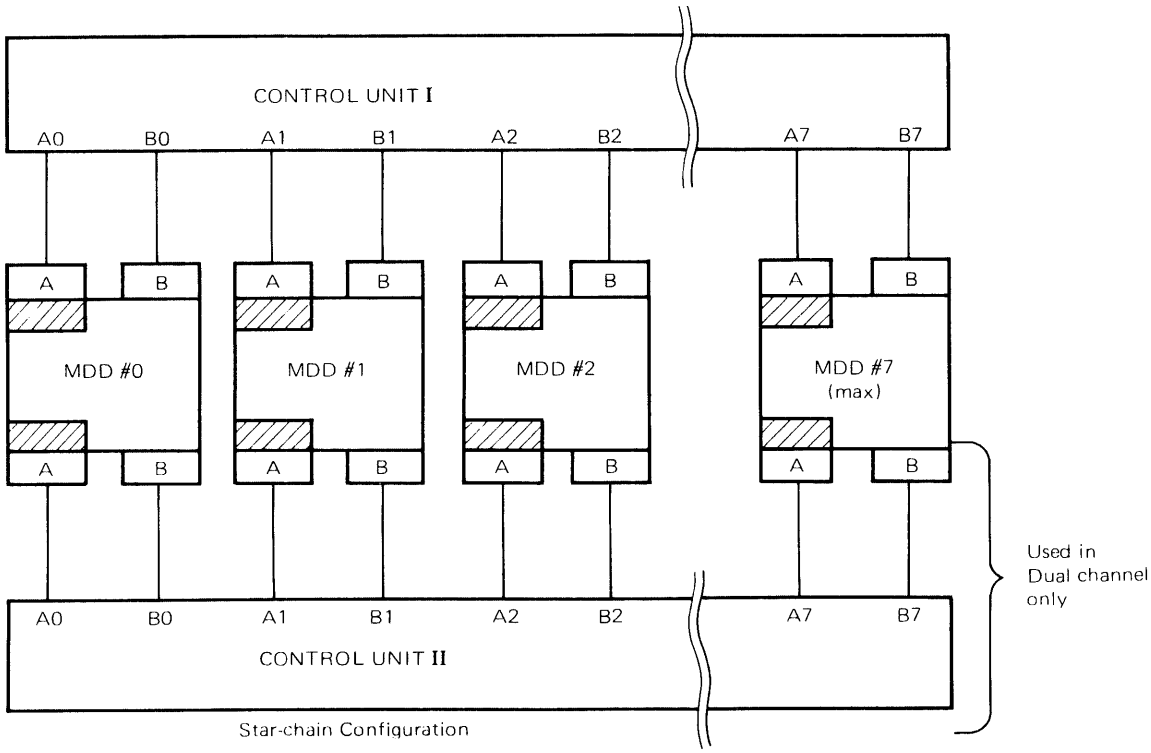
Transmitters and receivers (SN75110 and SN75107 or equivalent) are used to provide a terminated, balanced-line transmission system. Refer to Section 4.5.7.1.

4.5.2 Interface Cabling

Refer to Figure 4-5-1.



a) Daisy-Chain Configuration



b) Star-Chain Configuration

Figure 4-5-1 Interface Cabling

Notes: 1) Line terminators (LTN) are required on the control unit and each unit in a star cable configuration.

2) Line terminators are required on the control unit and last drive in a daisy-chain cable configuration.

Figure 4-5-1 Interface Cabling

4.5.3 Type and Name of Signal Lines

4.5.3.1 "A" Cable Lines for Balanced Transmission

Refer to Figure 4-5-2.

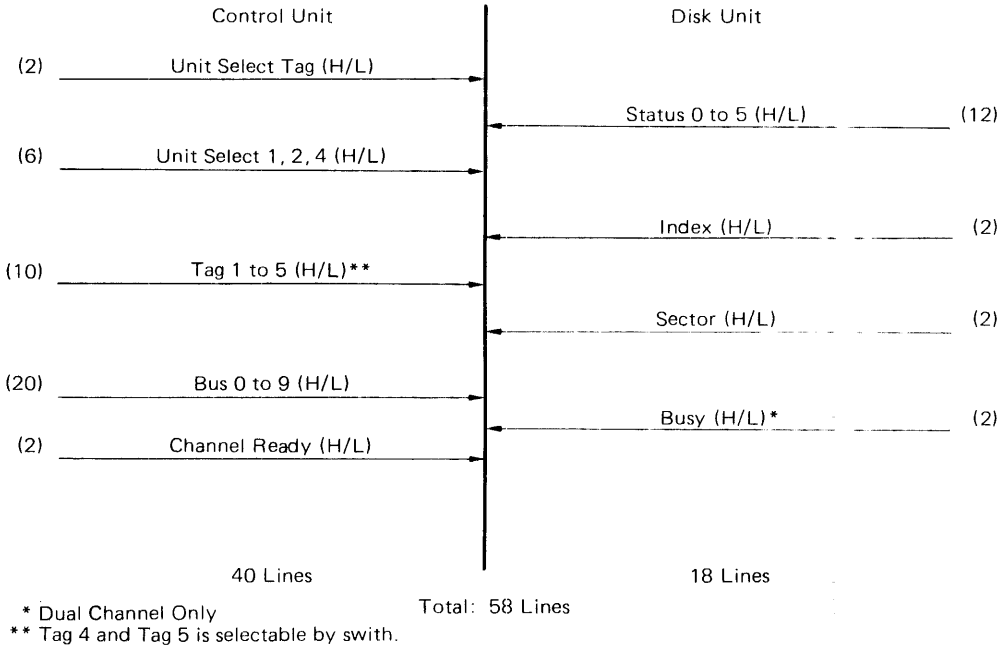


Figure 4-5-2 "A" Cable Signals

4.5.3.2 "B" Cable Lines for Balanced-line Transmission

Refer to Figure 4-5-3.

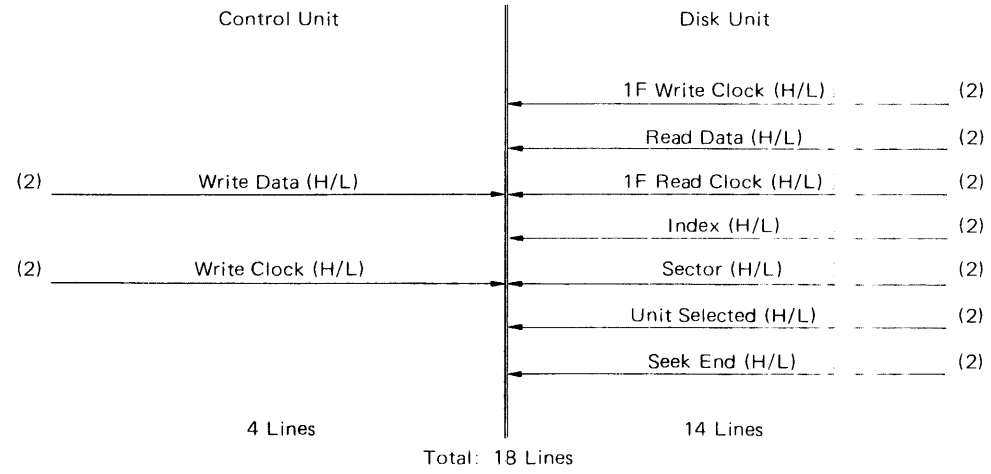


Figure 4-5-3 "B" Cable Signals

4.5.4 Description of Signal Lines

4.5.4.1 "A" Cable Input Signals

(1) Unit Select Tag
This signal gates Unit Select 1, 2, and 4 to select the desired disk. Refer to timing of Unit Select 1, 2, and 4 (Figure 4-5-6).

(2) Unit Select 1, 2, and 4
These three signals are binary-coded to select the desired disk and are validated by the leading edge of Unit Select Tag. The logical disk number (0 through 7) is selectable by means of a switch located on the PCB card.

(3) Tag 1 to 3 and Bus 0 to 9
Refer to Table 4-5-1 which shows the relationship of Tag 1, 2, and 3 and Bus 0 to 9.

Table 4-5-1 Tag/Bus Lines

Bus	Tag 1	Tag 2	Tag 3	Unit Select Tag *2
	Cylinder Address	Head Address	Control Select	
0	1	1	Write Gate	–
1	2	2	Read Gate	–
2	4	4	Servo Offset Plus	–
3	8	8	Servo Offset Minus	–
4	16	–	Fault Clear	–
5	32	–	AM Enable	–
6	64	–	RTZ	–
7	128	–	——	–
8	256	–	——	–
9	512	–	Release *1	Priority Select *1

Note 1: Dual Channel Only.
2: Validates (or gates) the Unit Select 1, 2, and 4 lines in addition to the dual channel priority select line.

(4) Cylinder Address (Tag 1)
Cylinder address is set with Tag 1 and bus lines (Bus 0 to 9) on the M232XK interface. However, throughout Tag 1, the bus lines must be stable. Refer to Figures 4-5-8 and 4-5-9.

The M232XK must indicate On Cylinder Status prior to Tag 1.

(5) Head Address (Tag 2)
The head address is set by Tag 2 and Bus 0 to 3 on the unit. However, throughout Tag 2, Bus 0 to 3 must be stable. Refer to Figure 4-5-10.

Note: Cylinder address and Head address information for the M232XK is shown in Figures 4-5-4 and Figure 4-5-5.

(a) M2321K

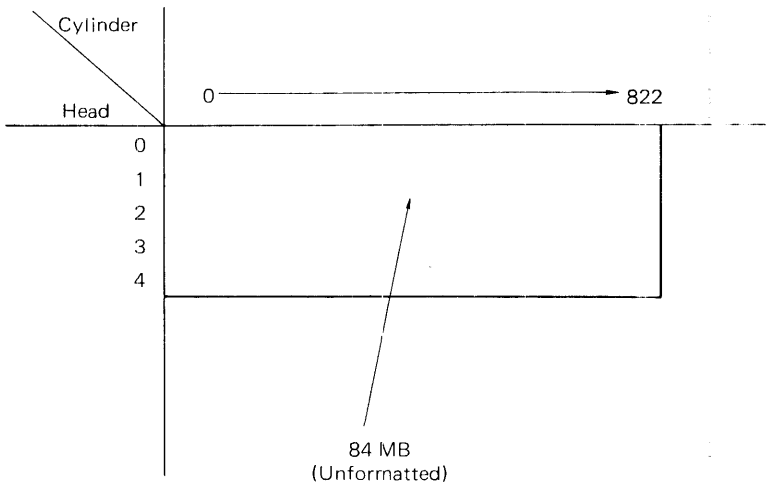


Figure 4-5-4 Storage Addressing M2321K

(b) M2322K

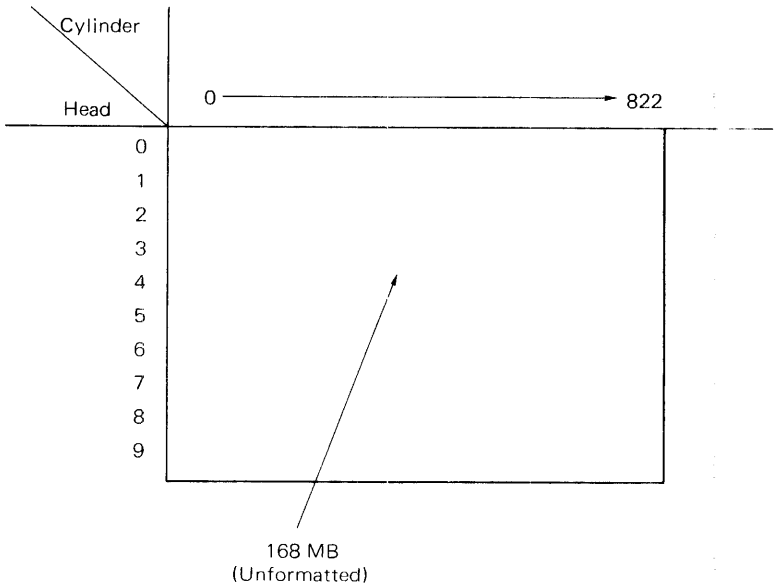


Figure 4-5-5 Storage Addressing M2322K

(6) Control Select

Bus lines 0 to 9 specified by Tag 3 have a different meaning in each bit. All signals are defined as control signals.

(A) Write Gate (Bus 0)

Write Gate signal enables the write operation on the specified track. This signal is validated under the following conditions:

i. Unit Ready — True
ii. On Cylinder — True
iii. Seek End — True
iv. Seek Error — False
v. Fault — False
vi. Channel Ready — True
vii. File Protect — False
viii. Offset — False

If Write Gate is turned on in cases other than the above-mentioned conditions, Fault occurs and writing is inhibited. Refer to the difinition of a Fault.

(B) Read Gate (Bus 1)
Read gate signal is used to read data from the specified track/record. Refer to the definition of Read Gate, Read Data and 1F Read Clock in Figure 4-5-18 and Figure 4-5-21.

(C) Servo Offset Plus (Bus 2)
When Servo Offset Plus signal is true on the unit, the head is offset 3.0 μm from nominal On Cylinder position away from the spindle. Refer to Figure 4-5-11. When going false of Servo Offset Plus, a 4ms delay is required before writing.

(D) Servo Offset Minus (Bus 3)
When Servo Offset Minus signal is true on the unit, the head is offset 3.0 μm from nominal On Cylinder position towards the spindle. Refer to Figure 4-5-11. When going false of Servo Offset Minus, a 4ms delay is required before writing.

(E) Fault Clear (Bus 4)
Fault Clear signal resets the Fault status; however, if any source of a fault still exist (refer to Fault), this status is not cleard.

(F) AM Enable (Bus 5)
The AM (Address Mark) Enable signal, in conjunction with Write Gate or Read Gate, is used in a variable sector format. When AM Enable is true while Write Gate is true, an AM of 3-bytes is written on the desired track. When AM Enable is true while Read Gate is true, the disk read circuit searches for an AM of three bytes. When the AM is found, the unit will issue an Address Mark Found signal to the control unit. Refer to Figures 4-5-22 and Figure 4-5-23.

(G) RTZ (Return to Zero) (Bus 6)
No matter where the access heads are located on the media, they are returned to cylinder zero and head zero by the RTZ signal. This signal also clears the Seek Error flip-flop.

(H) Release (Bus 9) [Dual Channel Only]
The Release command releases Channel Reserve and Unconditionally Reserve in the drive, making alternate channel access possible after selection by the other channel ceases.
If the customer desires the Release Timer feature using the Release Time switch on the optional Dual Channel PCB assembly, release will occur 500 ms (nominal) after the deselection of the drive. Refer to Figure 4-5-7.

(7) Channel Ready
The Channel ready signal is used to prevent lost of information or damage to the file caused by random interface disturbance when the control unit power is lost. This signal must be stable when the control unit is available, and must be disabled before logic levels decay at the interface lines when a power failure of the control unit occurs. Refer to Figure 4-5-14.

(8) Tag 4 and Tag 5 (selectable)
When Tag 4 goes true, the unit issues Sector Address Status signals on the Status 0 to 5 lines.
When Tag 5 goes true, the unit issues Device Check Status signals on the Status 0 to 5 lines.
When both Tag 4 and Tag 5 are true, the Device Type Code will be issued in BCD on the status 0 to 5 lines. Refer to Table 4-5-2 and Figure 4-5-15.

(9) Pick and Hold
Pick and Hold are not used in M232X Micro Disk Drive.

(10) Priority Select (Dual Channel Only)

When the control unit issues Unit Select Tag and Bus Bit 9 with a specified disk address, the disk drive will be unconditionally selected and absolutely reserved by the channel issuing the command, providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the drive is uncodnitionally reserved by a Priority Select command, the respective channel has exclusive access to the drive. The oppositie channel can access it only after Release command has been issued by the selected channel. Refer to Figure 4-5-7. When a dual port drive is unconditionally reserved, all interface signal are inhibited on the other channel, including unit selected and Busy signals.

4.5.4.2 "A" Cable Output Signals

(1) Status 0 to 5

The status 0 to 5 lines contain status information determined by a combinations of Tag 4 and Tag 5 signals. Information available on status lines 0 to 5 with the various combinations of Tag 4 and 5 signals is specified in Table 4-5-2.

Table 4-5-2 Status Lines Determined by Tag 4/5

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Count* Status	Fault/Seek Error* Status	Device Type*
0	Unit Ready	Sector Address 1	Fault 1	Device Type 1
1	On Cylinder	" 2	" 2	" 2
2	Seek Error	" 4	" 4	" 4
3	Fault	" 8	Seek Error 1	" 8
4	File Protected	" 16	" 2	" 16
5	AM Found	" 32	" 4	" 32

* Note: These status signals are available if Tag 4/5 function is enabled. When Tag 4/5 switch is set to Disable, only Unit Status is available.

(A) Unit Status

i Unit Ready

When Unit Ready signal is true, and the unit is selected, this signal indicates the unit is up to speed, and no fault condition exists within the unit.

ii On Cylinder

On cylinder line indicates that the heads are located on the specified cylinder (track).

iii Seek Error

Seek Error signal indicates that a seek error has occurred. In this case, the On Cylinder signal does not always go true. The Seek Error is cleared by issuing RTZ command. Seek Error occurs in the condition described in (c) Fault/Seek Error Status.

iv Fault

Fault signal indicates that a fault condition exists in the unit, and details of this signal describes in (c) Fault/Seek Error Status

The fault status is cleared by a fault clear on tag 3 and bus 4; or by an active fault clear on the operator panel (if operator panel is employed.)

Fault Status turns on the check lamp on the operator panel as well as Fault Indicator LEDs on PCB assembly.

v File Protected
File Protected signal indicates that the selected M232XK is in a write-protected status. The File Protect function is enabled by the following switches:
a. File Protect Switch on the operator panel (option)
b. File Protect Switch on the PCB assembly.
Attempting to write while protected will cause a Fault (Read/Write Check 3) to be issued to the control unit.

vi Address Mark Found
Address Mark Found is an eight-byte pulse which is sent to the control unit at least two bytes after the recognition of three-byte DC-erased area.

(B) Sector Address 1 to 32 (Status Lines 0 to 5)
Six bits of binary-coded Sector Address indicate the current sector address in the unit. They are transferred from the Sector Counter, reset by the trailing edge of Index, and clocked by the trailing edge of Sector. Sector Address (Status Lines 0 to 5) is issued to the control unit by activating Tag 4.
Refer to Figure 4-5-16 for timing of Sector Address (status lines 0 to 5).

(C) Fault/Seek Error
Three-bit binary coded Status 0 to 2 indicate the seven types of Fault, and also three-bit binary coded Status 3 to 5 indicate the six types of Seek Error as shown in Table 4-5-3.

Table 4-5-3 Fault/Seek Error Status

Status	Status Bit							Seek Error
	5	4	3	2	1	0	Designation	Condition
Seek Error	0	0	1	x	x	x	RTZ Time-out	Indicates an RTZ operation is not terminated within the specified time.
	0	1	0	x	x	x	Seek Time-out	Indicates a Seek operation is not terminated within the specified time.
	0	1	1	x	x	x	Over-Shoot	Indicates the head over-shoots the target cylinder during setting time, or the head moves out during track following sequence in linear mode.
	1	0	0	x	x	x	Seek Guard Band	Indicates the guard band is detected during seek operation.
	1	0	1	x	x	x	Linear Mode Guard Band	Indicates the guard band is detected during linear mode.
	1	1	0	x	x	x	RTZ Outer Guard Band	Indicates the Outer guard band is detected during GTZ operation.
	1	1	1	x	x	x	Illegal Cylinder	Indicates an illegal cylinder address (> 822) is issued by the controller.

(D) Device Type 1 to 32 (Status lines 0 to 5)
Enabling Tag 4 and Tag 5 lines causes Device Type Status to be issued to the control unit as Status 0 to 5 signals. Binary-coded Device Type signals are specified as show in Table 4-5-4.

Table 4-5-4 Device Type Code

	Status 5	Status 4	Status 3	Status 2	Status 1	Status 0	
	2^5	2^4	2^3	2^2	2^1	2^0	
M2321	1	0	0	1	0	0	84 MB
M2322	1	0	0	1	0	1	168 MB

Notes: 0—False; 1—True

(2) Index

The Index signal occurs once per revolution and is used for reference in read/write operation to indicate the beginning of a track.

Refer to Figure 4-5-16 for the timing of Index and Sector.

(3) Sector

The Sector Mark, a 1-½ pulse which occurs 1 to 128 times per track, is derived from the Index signal and Byte Clock of the servo surface. The number of bytes per track is selected by DIP switches. Refer to 3.7.6.

(4) Busy (Dual Channel Only)

If the drive is already selected and/or reserved, a Busy signal will be issued to the "A" cable and the Unit Selected signal will be issued to the "B" cable of the channel attempting the select function. The Busy signal will remain until the Unit Select Tag is negated or the drive is no longer busy. Unit Selected signal should be used to enable Busy in the control unit. Refer to Figure 4-5-6.

4.5.4.3 "B" Cable Input Signals

(1) Write Data

This line carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 4-5-17.

(2) Write Clock

Write Clock is a return signal of 1F Write Clock issued from the unit. Refer to Figure 4-5-17.

4.5.4.4 "B" Cable Output Signals

(1) 1F Write Clock

This signal is used by the control unit to synchronize Write Data Clock. 1F Write Clock is available during Unit Ready Status except during read operations. However, a fluctuation of 32 bits ±3 bits could occur in the last 4 bytes of Invalid Data. Refer to Figure 4.5.17.

(2) Read Data

This line transmits the recovered data in the form of NRZ data synchronized with 1F Read Clock. Refer to Figure 4-5-18.

(3) 1F Read Clock

This line transmits 1F Read Clock. The Read Data is synchronized with 1F Read Clock. Refer to Figure 4-5-18. This line is valid only during a read operation.

(4) Unit Selected

When the three unit select signals (gated by the Unit Select Tag) and the logical address of the unit compare, the status signals are issued from the MDD. The Unit Selected signal activates the drivers/receivers on A—cable.

(5) Seek End

Seek End signal indicates that a Seek, RTZ or Offset operation has terminated. This signal may be used as an interrupt to the control unit.

In dual channel mode, the Seek End signal sent the unselected channel will normally be constant-true. However, if while the drive is selected on a channel, and the opposite channel receives a select command, and then the selected channel resets the Select and Reserve latches on the drive, the Seek End signal sent to the Waiting channel will go false for 30 μs.

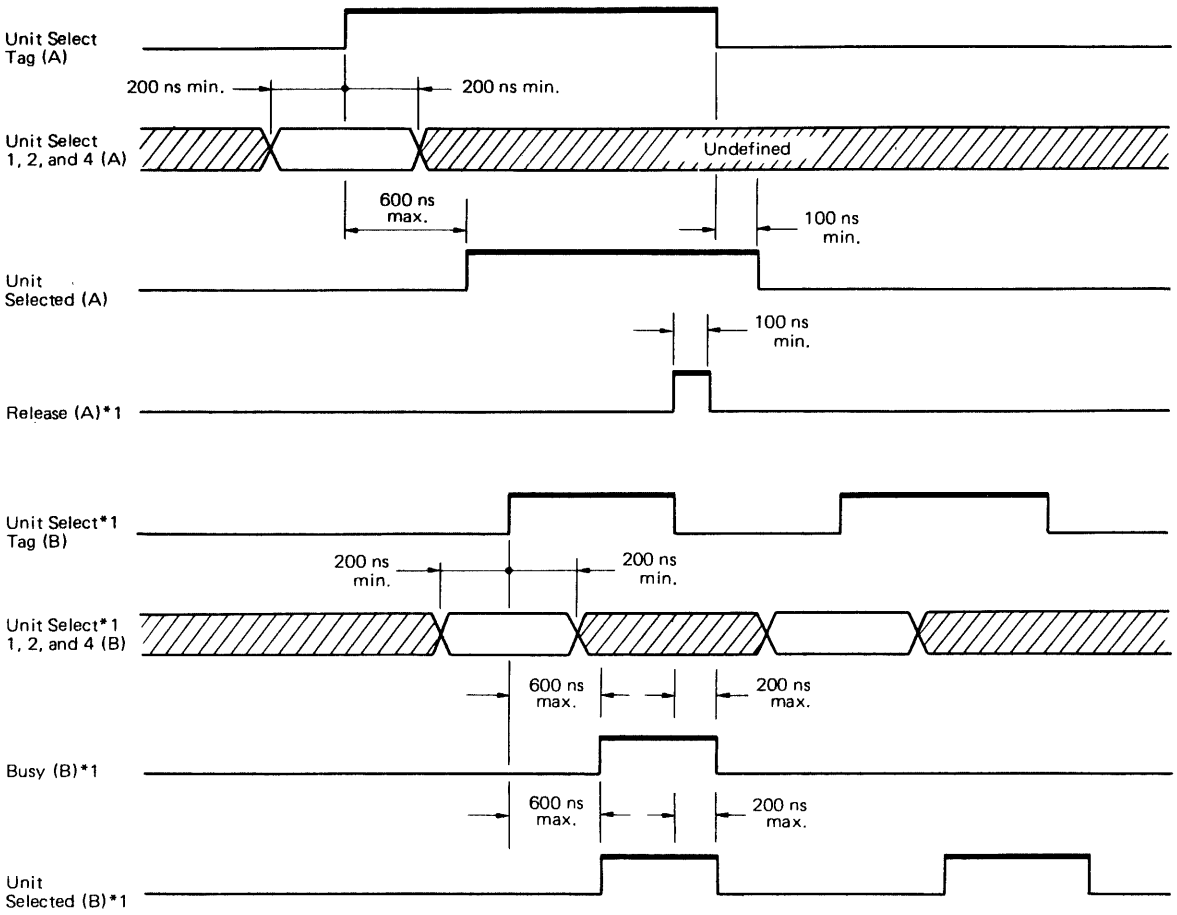
(6) Index/Sector

Exactly the same as A Cable Signals.

4.5.5 Timing

Polarities are defined in positive logic. The shaded area is undefined.

4.5.5.1 Unit Selection

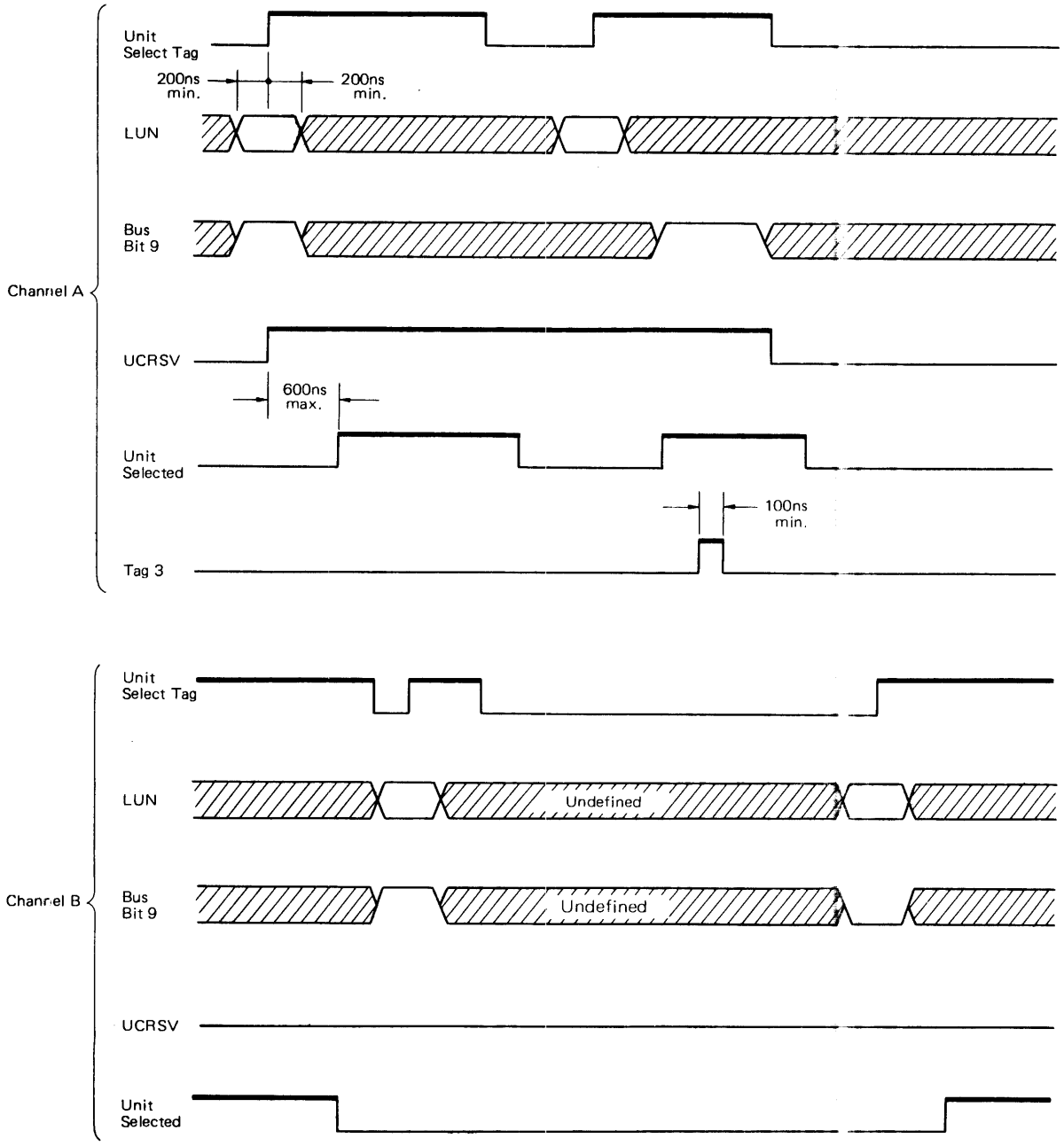


Note: * 1—Dual Channel only.

Figure 4-5-6 Unit Select Timing

4.5.5.2 Priority Select Timing (sample)

Refer to Figure 4.5.7.



Notes: 1) LUN: Logical Unit Number (Unit Select 1, 2 and 4).

2) UCRSV: Unconditionally Reserved (Priority Selected).

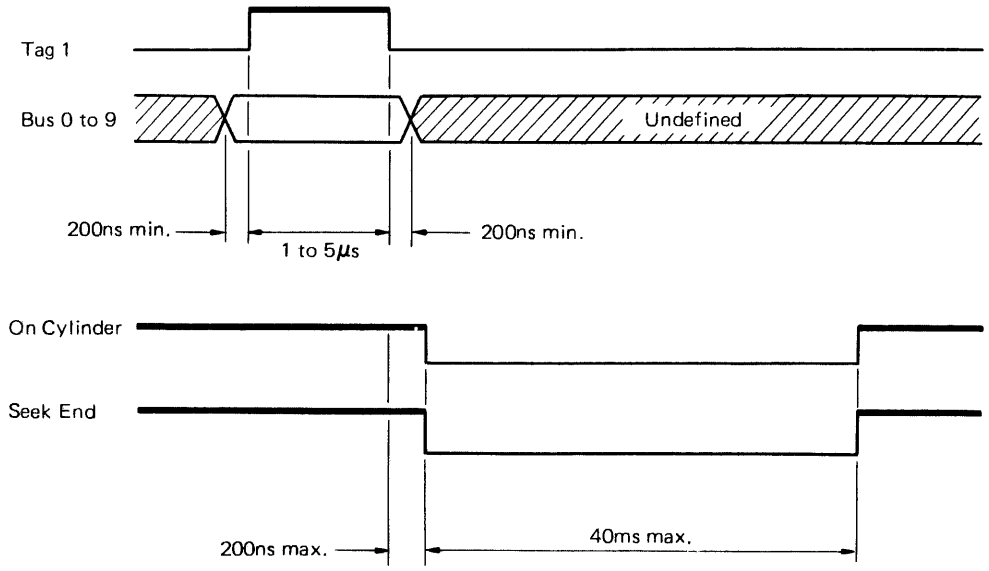
3) Sample Sequence is as follows;

CHB Selected → CHA Priority Select → CHB Priority Select → CHA Release → CHB Select

Figure 4-5-7 Priority Select Timing

4.5.5.3 Direct Seek Timing (Tag 1)

Refer to Figure 4-5-8.



Note: Cylinder Address must be less than 822.

Figure 4-5-8 Direct Seek Timing

4.5.5.4 Same Cylinder Address

Refer to Figure 4-5-9.

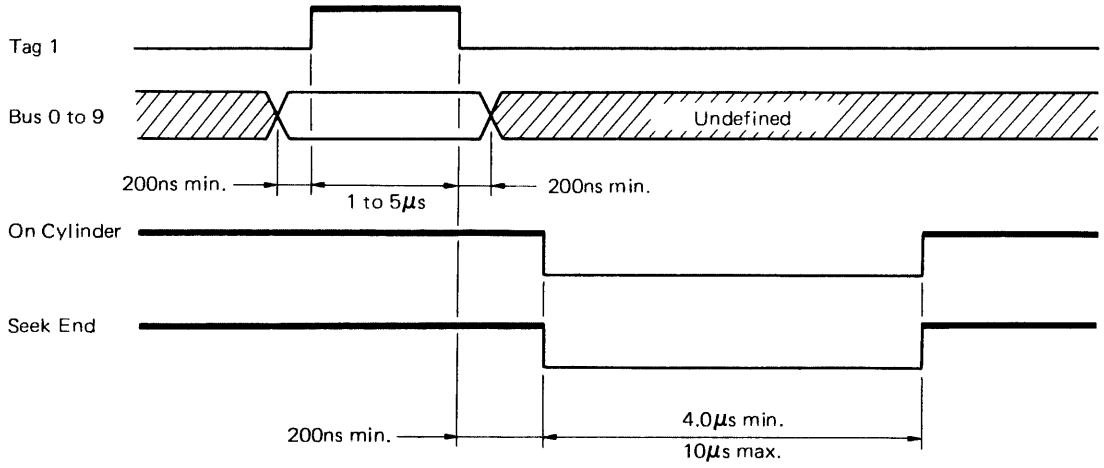


Figure 4-5-9 Same Cylinder Address

4.5.5.5 Tag 1 to Tag 2 Timing

Refer to Figure 4-5-10.

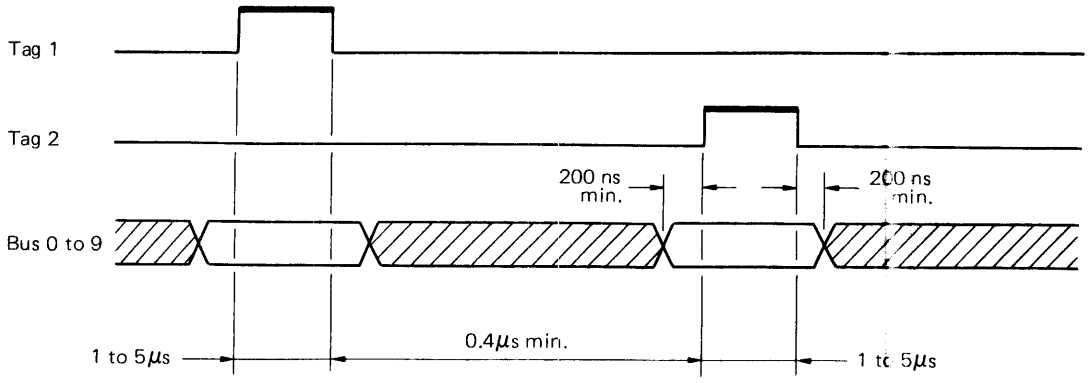


Figure 4-5-10 Tag 1 to Tag 2 Timing

4.5.5.6 Offset Timing

Refer to Figure 4-5-11.

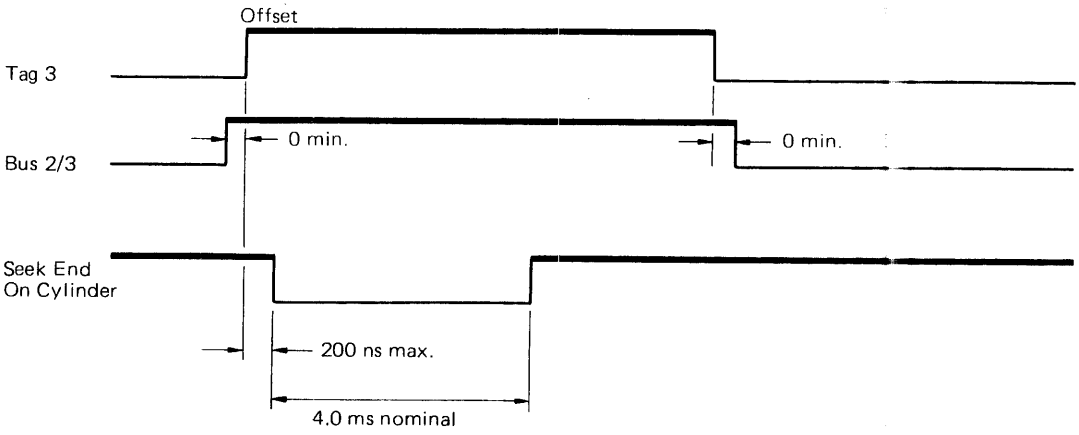


Figure 4-5-11 Offset Plus/Minus Timing

4.5.5.7 Fault Clear Timing

Refer to Figure 4-5-12.

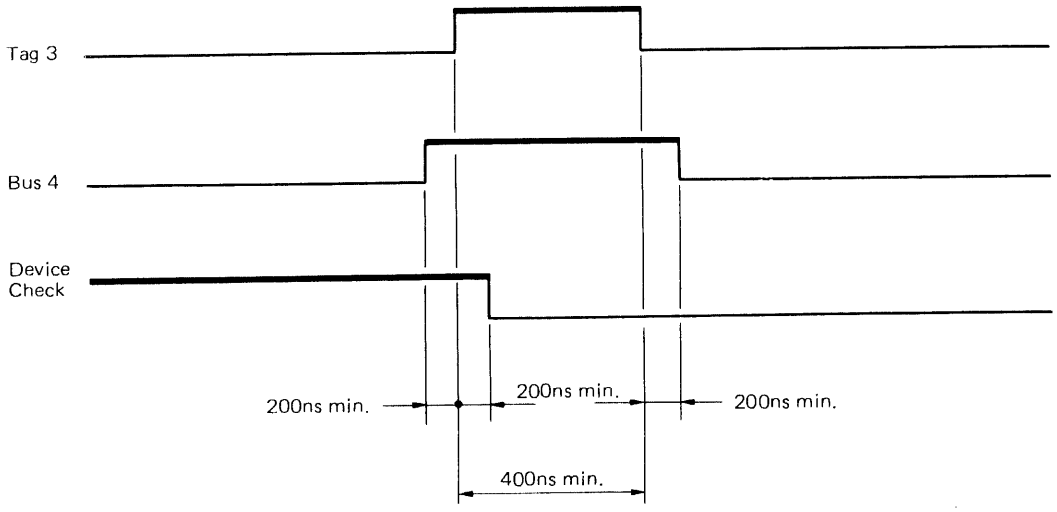
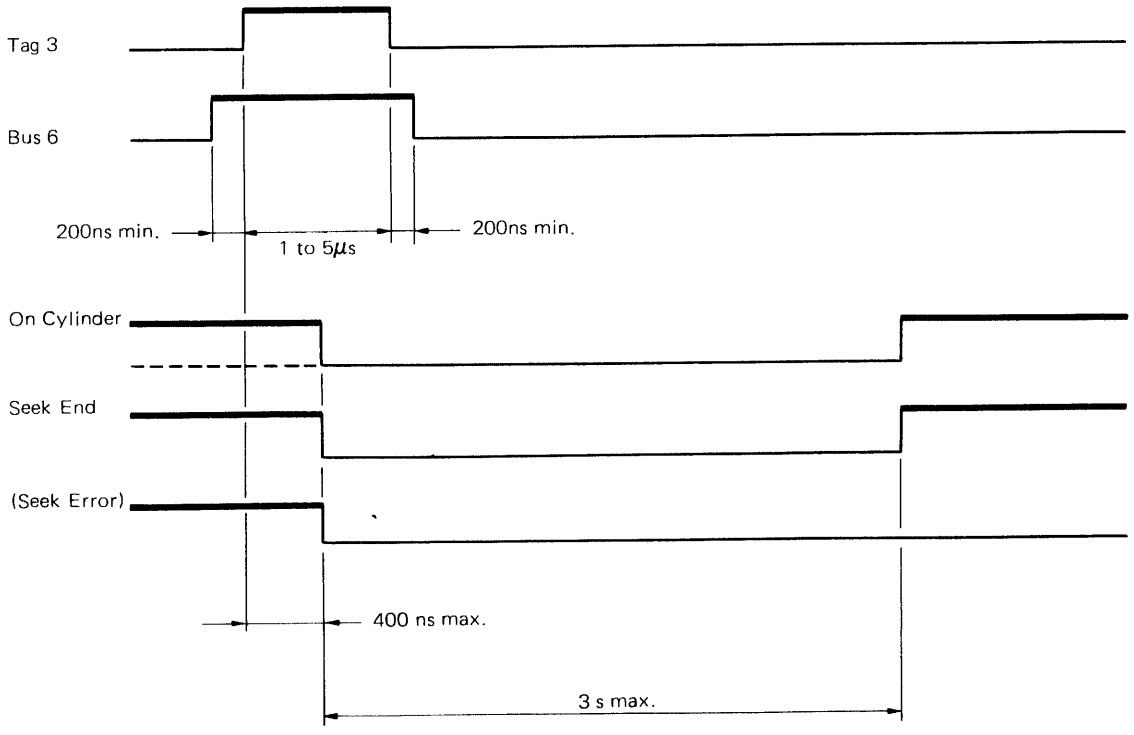


Figure 4-5-12 Fault Clear Timing

4.5.5.8 RTZ Timing

Refer to Figure 4-5-13.



Note: On Cylinder is not always set if a Seek Error occurs.

Figure 4-5-13 RTZ Timing

4.5.5.9 Channel Ready Timing

Refer to Figure 4-5-14.

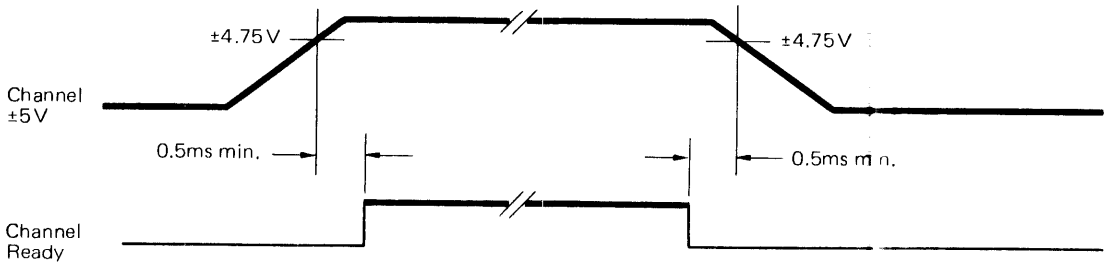


Figure 4-5-14 Channel Ready Timing

4.5.5.10 Tag 4/5 and Status 0 to 5 (optional) Timing

Refer to Figure 4.5.15.

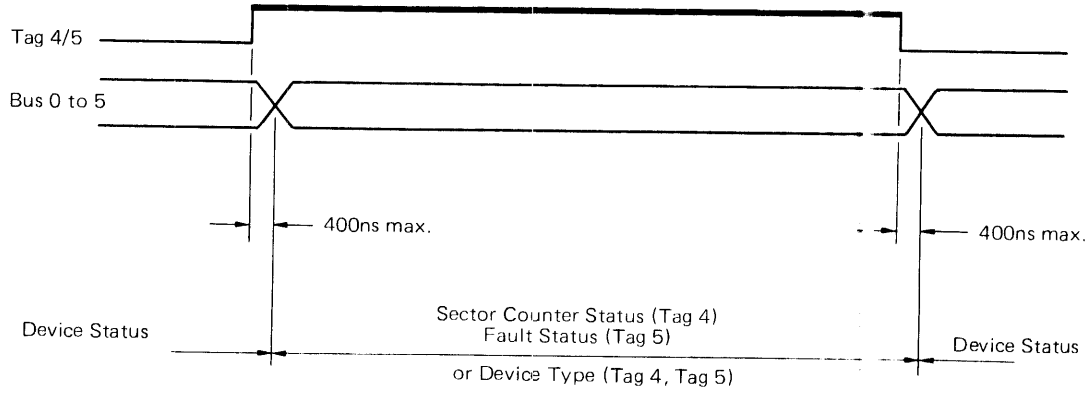


Figure 4-5-15 Tag 4/5 Timing

4.5.5.11 Index/Sector Timing

Refer to Figure 4-5-16.

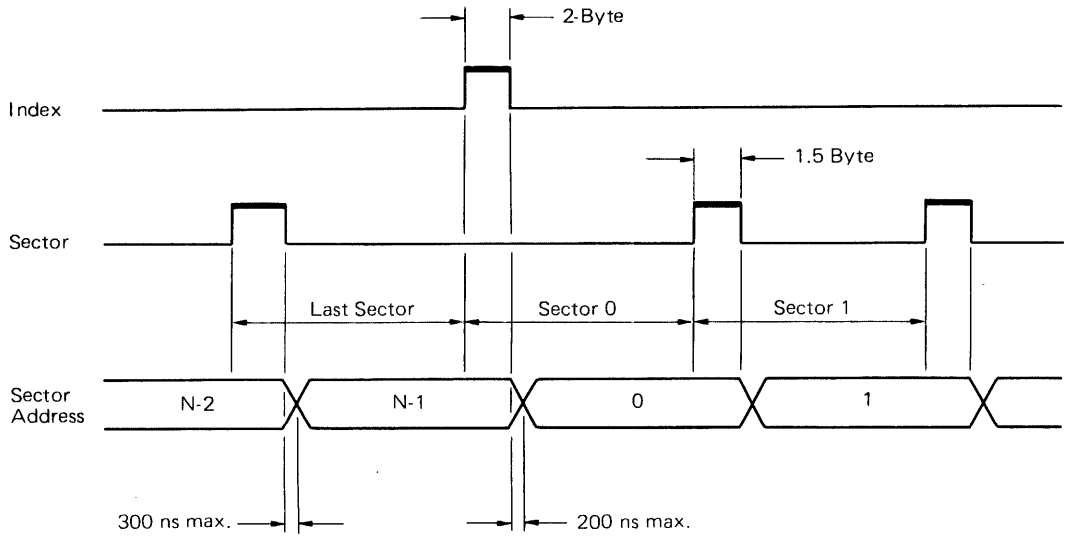
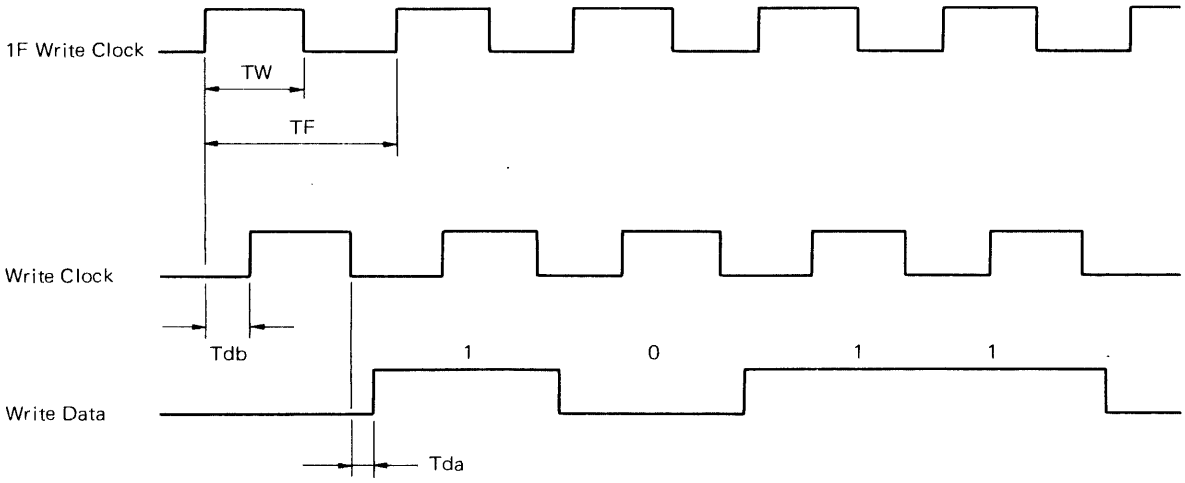


Figure 4-5-16 Index and Sector Timing

4.5.5.12 1F Write Clock, Write Data/Write Clock Timing

Refer to Figure 4-5-17.



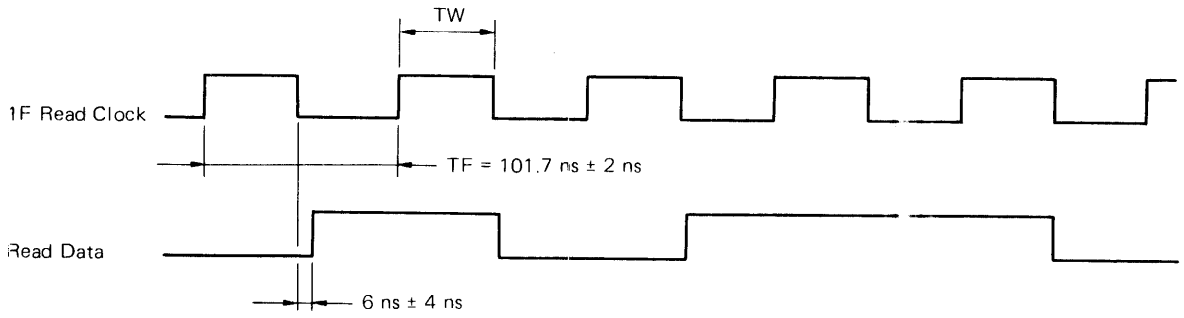
Tw = TF/2
TF = 101.7 ns ± 2 ns
Tdb = 2 bits max.
Tda = 0 ± 10ns

Notes:
1. Write Data and Write Clock timing shall be specified at the output connector of the control unit.
2. The permissible value of TF=101.7ns ± 2ns is about 2%, which includes the rotational speed tolerance, 1% and the servo jitter, ±1%.
3. NRZ Write Data issued from the control unit is write-compensated and then MFM-modulated for writing on the disk surface.

Figure 4-5-17 Write Data and Write Clock Timing

4.5.5.13 Read Clock/Read Data Timing

Refer to Figure 4-5-18.



Tw = TF/2

Notes: 1. 1F Read Clock and Read Data timing shall be specified at the output connector of the disk unit.

2. Read Data signal should be clocked at the positive-going edge of 1F Read Clock on the control unit.

Figure 4-5-18 1F Read Clock and Read Data Timing

4.5.6 Read/Write Timing

4.5.6.1 Format Write

Refer to Figure 4-5-19.

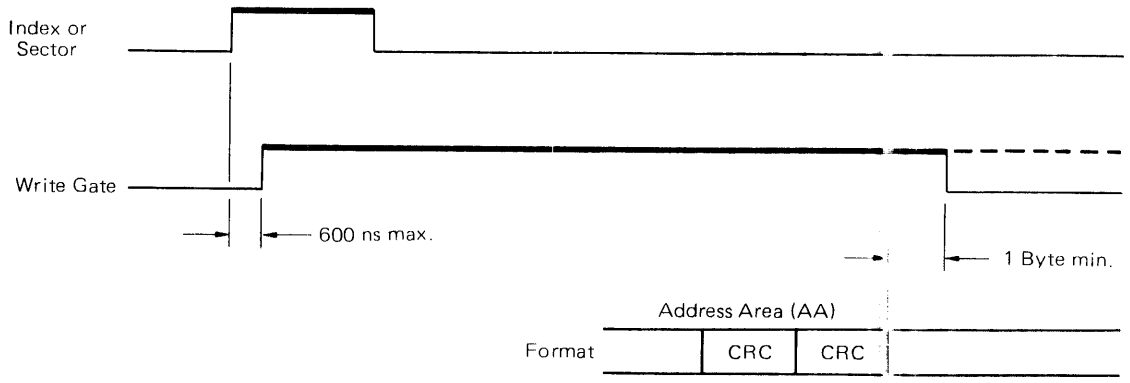


Figure 4-5-19 Format Write Timing

4.5.6.2 Data Write

Refer to Figure 4-5-20.

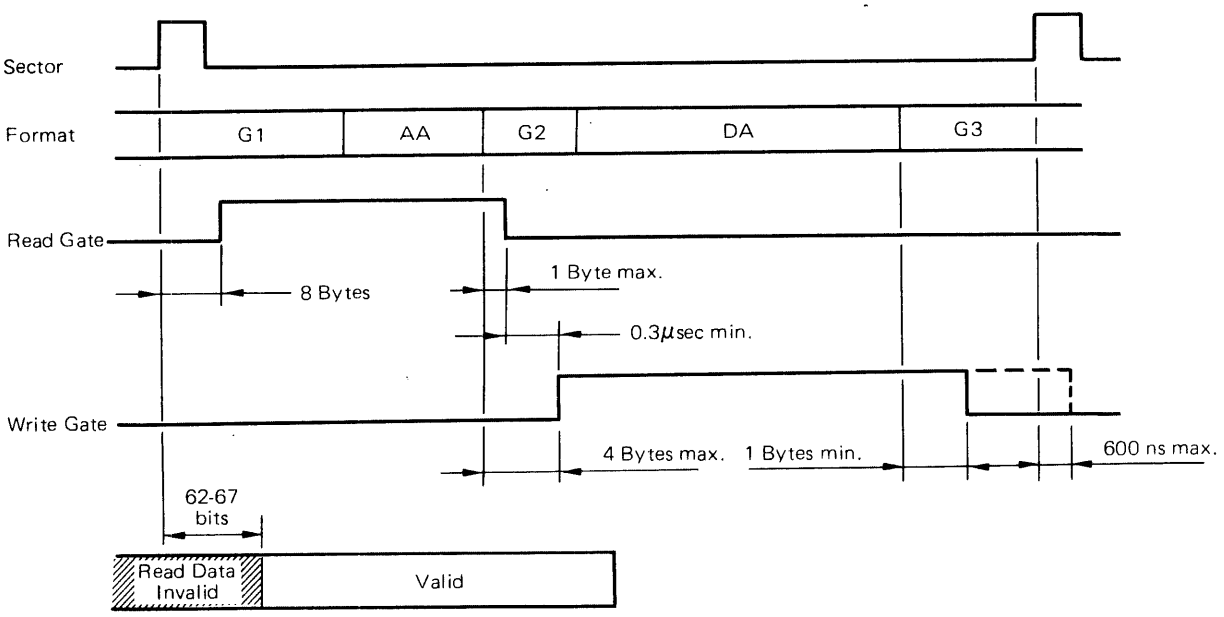
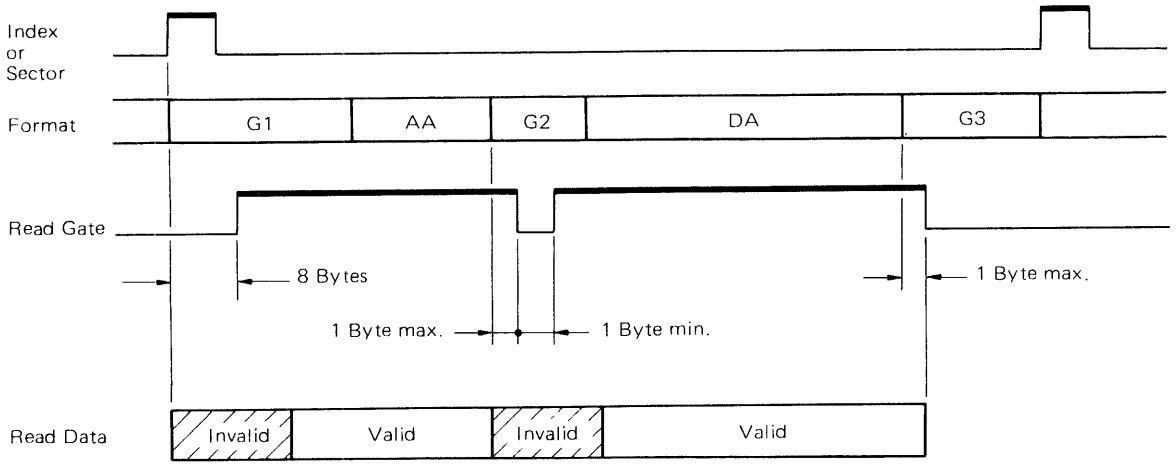


Figure 4-5-20 Write Data Timing

4.5.6.3 Data Read

Refer to Figure 4-5-21.



Notes: 1. The invalid data in the above figure is inhibited in the unit; therefore, it may be disregarded in the control unit.

2. The timing for switching to 1F Read Clock should be performed after the invalid data. In this case, a phase adjustment is required for 1 or 2 bits.

Figure 4-5-21 Read Data Timing

4.5.6.4 AM Write (Variable Soft Sector Only)

Refer to Figure 4-5-22.

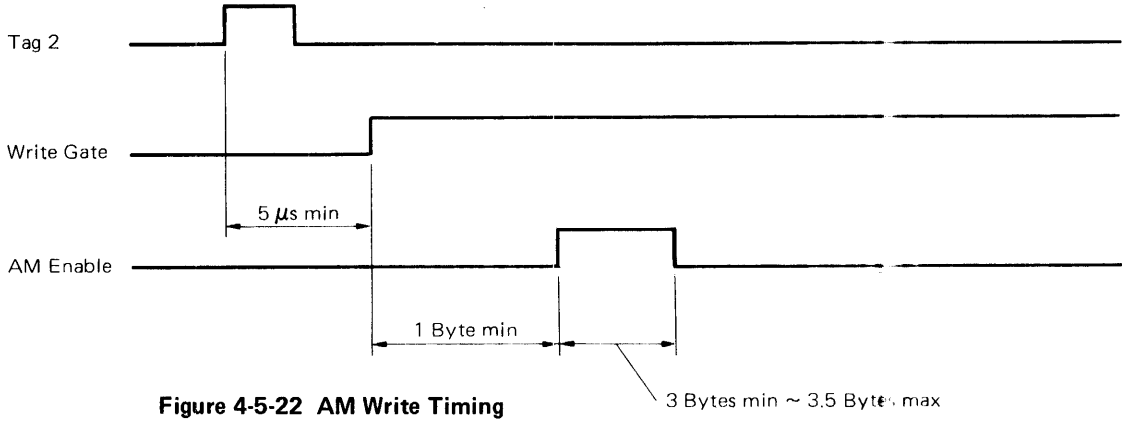


Figure 4-5-22 AM Write Timing

4.5.6.5 AM Read (Variable Soft Sector Only)

Refer to Figure 4-5-23.

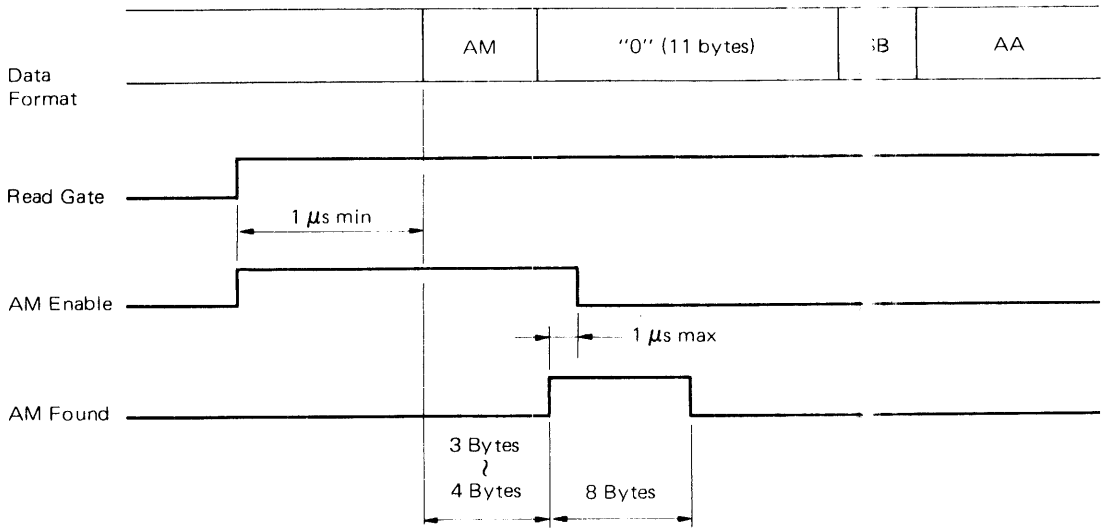


Figure 4-5-23 AM Read Timing

4.5.6.6 Write-To-Read Recovery Time

Refer to Figure 4-5-24. When head selection has been stabilized, the recovery time before Read Gate can be enabled after Write Gate goes false is 10 μs minimum.

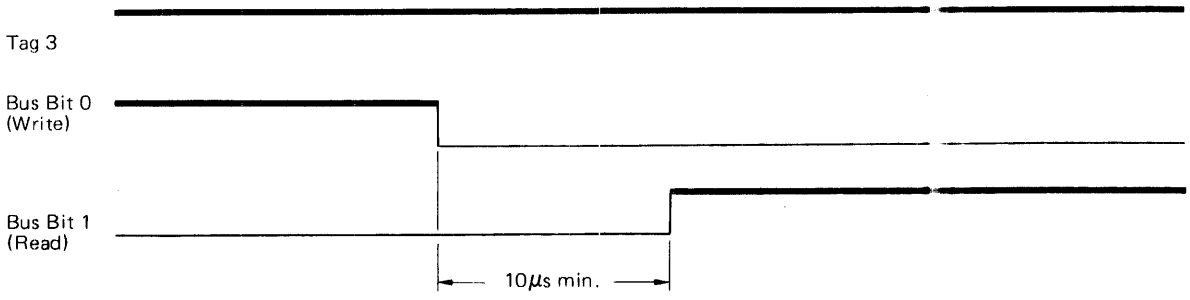


Figure 4-5-24 Write-To-Read Recovery Time

4.5.6.7 Head Select Transient

Refer to Figure 4-5-25. There is a 5 μs delay within the disk drive due to circuit characteristics between the deselection of one head and the selection of another head.

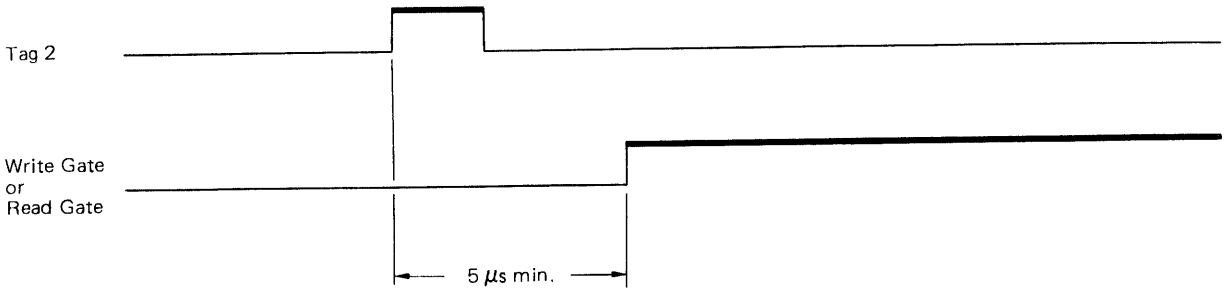
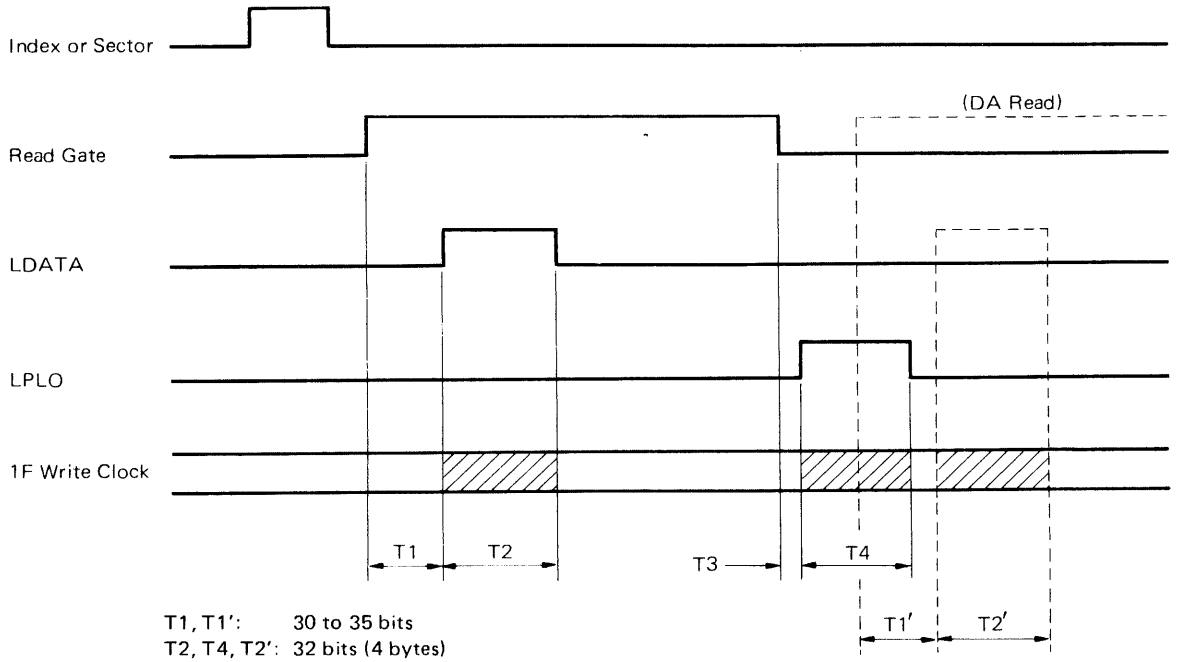


Figure 4-5-25 Head Select Transient

4.5.6.8 1F Write Clock in Reading

In the read operation, the 1F Write Clock signal fluctuates slightly within the Lock-To-Data or Lock-To-PLO signal (internal signal of Variable Frequency Oscillator circuit), as shown in Figure 4-5-26.



T1, T1': 30 to 35 bits
T2, T4, T2': 32 bits (4 bytes)
T3: 2 to 11 bits

Note: Shaded area (4 bytes) is equal to 32 ± 3 bits of clock count.

Figure 4-5-26 1F Write Clock in Reading

4.5.7 Interface Transmission

4.5.7.1 Driver and Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission. The Driver is SN75110 or equivalent, and the Receiver is SN75107/SN75108 or equivalent.

(1) Driver

Refer to Figure 4-5-27 and Table 4-5-5.

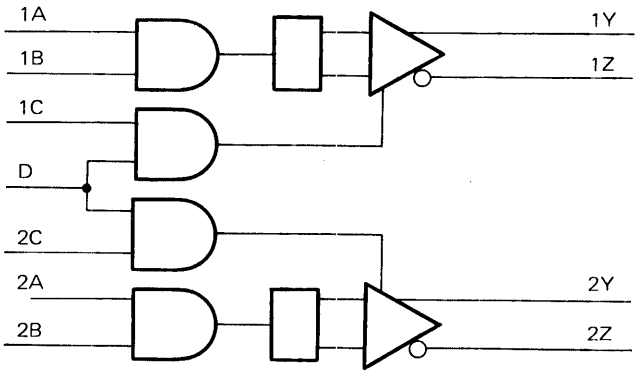


Figure 4-5-27 Driver Logic Diagram (SN75110)

Table 4-5-5 SN75110 Function Table

Logic Inputs		Inhibit Input		Outputs	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

Note: H—High Level, L—Low Level, X—Irrelevant.

(2) Receiver

Refer to Figure 4-5-28 and Table 4-5-6.

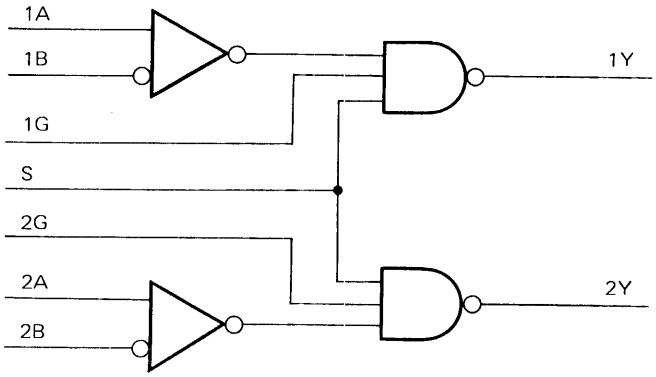


Figure 4-5-28 Receiver Logic Diagram (SN75107/75108)

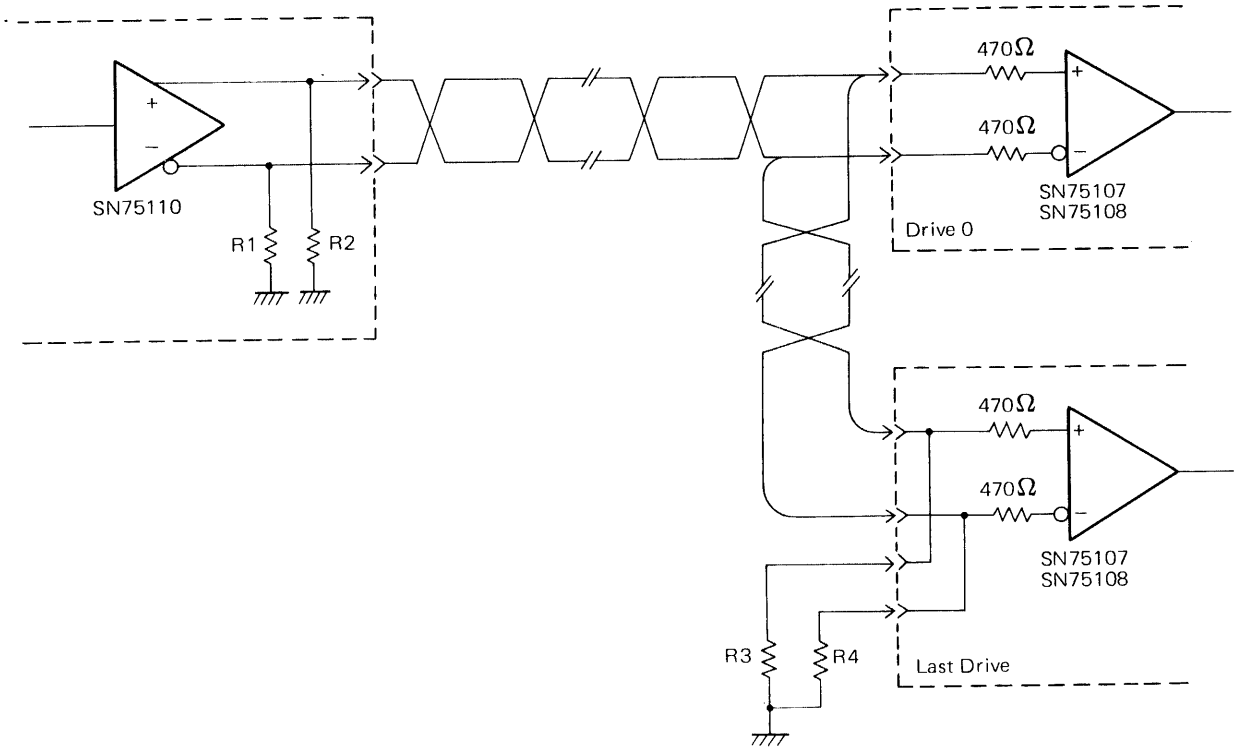
Table 4-5-6 SN75107/75108 Function Table

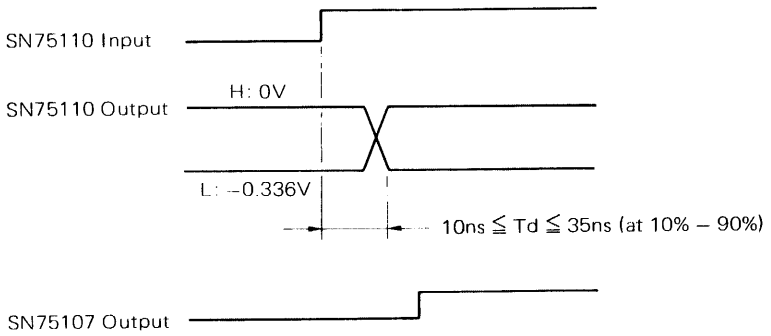
Differential Inputs	Strobes		Output
	G	S	Y
A−B ≥ 25 mV	X	X	H
−25 mV<A−B<25 mV	X	L	H
	L	X	H
	H	H	Indeterminate
A−B ≤ −25 mV	X	L	H
	L	X	H
	H	H	L

Note: H—High Level; L—Low Level; X—Irrelevant.

4.5.7.2 "A" Cable (Control Cable) Transmission

Refer to Figure 4-5-29.





Notes: 1. Line terminators are located on the unit and the controller. R1 to R4: 56 Ω ± 5 %, 1/10W.

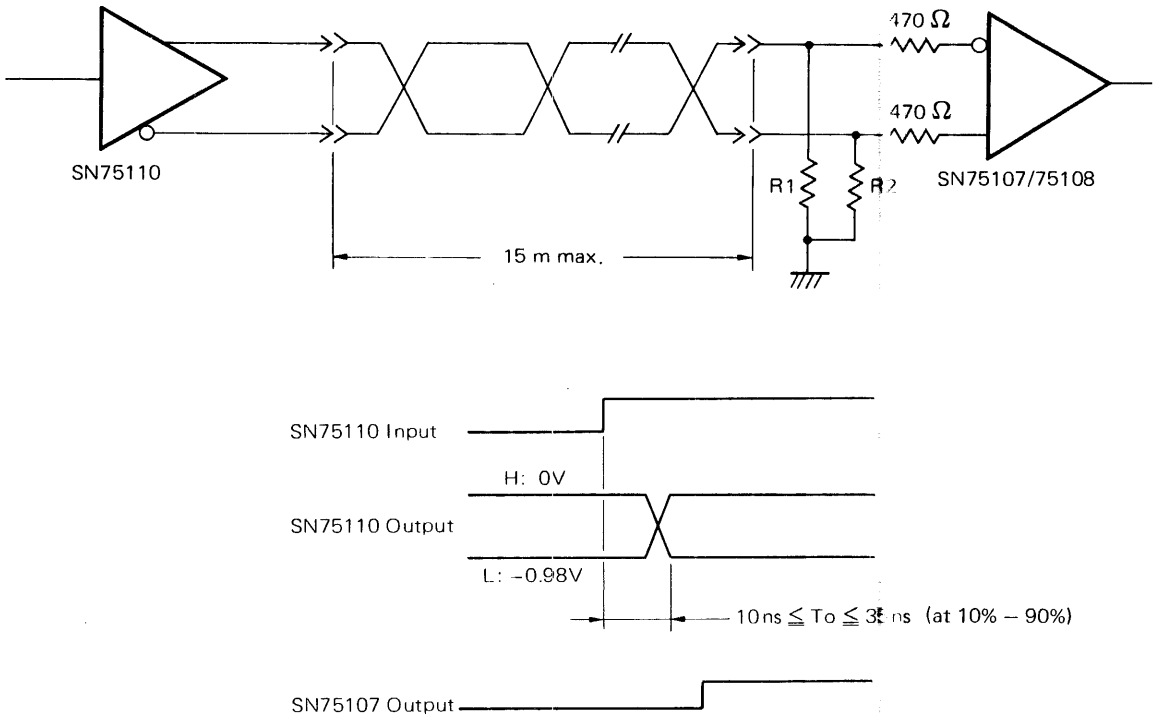
2. A line terminator is located on the terminator assembly of the last unit in the daisy chain configuration.

3. The maximum cable length is 30 meters.

Figure 4-5-29 Balanced Transmission of "A" Cable

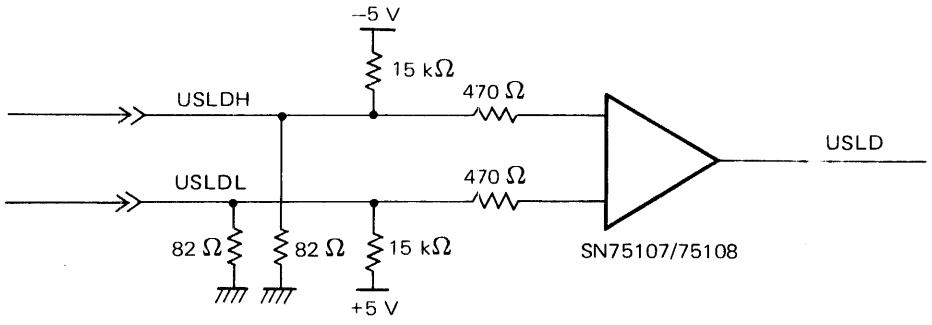
4.5.7.3 "B" Cable (Data Cable) Transmission

Refer to Figure 4-5-30.



a) Balanced Transmission of "B" cable

Note:
1. Cable shall be flat with characteristic impedance of 100 ± 10 ohms.
2. Line terminators are located on the receivers at the drive or control unit. R1 and R2 are 82 ohms ± 5%, 1/10W.
3. The protect resistors (470 ohms) should be located on the receiver side. 470 Ω ± 5 %, 1/10W.
4. A bias network should be used to prevent disturbance conditions by power failure at the control unit end of Unit Selected and Seek End signals as in b).



b) Bias Network to Prevent Power Failure Disturbance

Figure 4-5-30 Balanced Transmission "B" Cable

4.5.7.4 Channel Ready Driver

The Channel Ready signal must be issued so that data is protected during a power failure of the control unit. Relay logic and passive terminations sometimes aid this requirement. If SN75110A drivers are used to drive the Channel Ready signal from the control unit, dual drivers should be connected in parallel, and no 56 ohm termination to ground should be used at the control unit.

4.5.8 Connectors and Cables

4.5.8.1 Connectors

(1) "A" Cable connectors (60 positions)
Refer to Table 4-5-7.

Table 4-5-7 "A" Cable Connectors

Connector	Fujitsu Specification	
Drive Side	FCN-702P060-AU/M	(Wire Wrapping)
	FCN-704P060-AU/M	(Straight)
	FCN-705P060-AU/M	(Right Angle)
Cable Side	FCN-707J060-AU/B	(Closed End)
	FCN-707J060-AU/O	(Through End)

(2) "B" Cable connectors (26 positions)
Refer to Table 4-5-8.

Table 4-5-8 "B" Cable Connectors

Connector	Fujitsu Specification	
Drive Side	FCN-702P026-AU/M	(Wire Wrapping)
	FCN-704P026-AU/M	(Straight)
	FCN-705P026-AU/M	(Right Angle)
Cable Side	FCN-707J026-AU/B	(Closed End)
	FCN-707J026-AU/O	(Through End)

4.5.8.2 Cable

Refer to Table 4-5-9.

Table 4-5-9 Cable

Cable	Specification
A	455-248-60 Spectra Strip Zo = 100 ohms ± 10 ohms 28 AWG, 7 strands
B	174-26 Ansley / 3476-26 3M Zo = 100 ohms ± 10 ohms / Zo = 130 ohms ± 15 ohms 28 AWG, 7 strands / 28 AWG, 7 strands

4.5.9 Connector Pin Assignment

4.5.9.1 "A" Cable Connector 60 Pin

Refer to Table 4-5-10.

Table 4-5-10 "A" Cable Pin Assignment

Pin	Function	Pin	Function
1	Tag 1 L	31	Tag 1 H
2	Tag 2 L	32	Tag 2 H
3	Tag 3 L	33	Tag 3 H
4	Bus 0 L	34	Bus 0 H
5	Bus 1 L	35	Bus 1 H
6	Bus 2 L	36	Bus 2 H
7	Bus 3 L	37	Bus 3 H
8	Bus 4 L	38	Bus 4 H
9	Bus 5 L	39	Bus 5 H
10	Bus 6 L	40	Bus 6 H
11	Bus 7 L	41	Bus 7 H
12	Bus 8 L	42	Bus 8 H
13	Bus 9 L	43	Bus 9 H
14	Channel 1 Ready L	44	Channel Ready H
15	Status 3 L	45	Status 3 H
16	Status 2 L	46	Status 2 H
17	Status 1 L	47	Status 1 H
18	Index L	48	Index H
19	Status 0 L	49	Status 0 H
20	Status 5 L	50	Status 5 H
21	Busy L (Dual Channel Only)	51	Busy H (Dual Channel Only)
22	Unit Select Tag L	52	Unit Select Tag H
23	Unit Select 1 L	53	Unit Select 1 H
24	Unit Select 2 L	54	Unit Select 2 H
25	Sector L	55	Sector H
26	Unit Select 4 L	56	Unit Select 4 H
27	Tag 5 L (Selectable)	57	Tag 5 H (Selectable)
28	Status 4 L	58	Status 4 H
29	(Pick): Not used	59	(Hold): Not used
30	Tag 4 L (Selectable)	60	Tag 4 H (Selectable)

4.5.9.2 "B" Cable Connector 26 Pin

Refer to Table 4-5-11.

Table 4-5-11 "B" Cable Pin Assingment

Pin	Function	Pin	Function
1	GND	14	1F Write Clock H
2	1F Write Clock L	15	GND
3	Read Data L	16	Read Data H
4	GND	17	1F Read Clock H
5	1F Read Clock L	18	GND
6	Write Clock L	19	Write Clock H
7	GND	20	Write Data H
8	Write Data L	21	GND
9	Unit Selected H	22	Unit Selected L
10	Seek End L	23	Seek End H
11	GND	24	Index H
12	Index L	25	GND
13	Sector L	26	Sector H

4.6 ELECTRICAL CIRCUIT FUNCTION

4.6.1 Start/Stop Control

DC powers of +5V, −12V and +24V are applied to the drive from the optional power supply unit or system power. +12V required for servo circuit is regulated from +24V on TVQM PCB assembly.

The DC voltage monitor circuit (which monitors +5V, −12V, +24V and internal +12V) issues Power Ready (PWRDY) signal through the delay circuit when these voltages are within the specified range.

When +5V is supplied to the drive, the Crystal Oscillator circuit issues 15,728,640 Hz clock signal, this clock signal is divided by eight and converted into Control Clock 1 (CTCL1) at 1,966,080 Hz frequency which controls DC Motor Control circuit function. Then the CTCL1 signal is divided by thirty-two (32) and converted into Oscillator Clock (OSCLK) at 61,440 Hz (16.3μs interval) which controls Power-up Sequence Control circuit function.

Disabling of PWRDY signal resets all registers and latches on the drive, and also resets three latches at Power-up Sequence Control circuit, that is, Start Sequence Latch 1, 2 and 4 (SSL1, 2 and 4) signals which result in State 0.

The PWRDY signal is applied to a delay circuit (45 μs) and consequently Delayed Power Ready (DPWRDY) signal is issued to the Power-up Sequence Latch circuit. The leading edge of DPWRDY signal sets SSL1 latch and results State 1.

One hundred thirty milliseconds after enabling state 1, Emergency Retract (EMRT) signal is reset, and the relays RL1 and RL2 are activated on the TVQM PCB assembly. The contacts rℓ11 to rℓ13 of RL1 connect the DC Motor Power-amplifier and DC motor windings, the DC Motor Power-amplifier, however, is not activated by disabling the later-mentioned ACDME signal at this state. The contact Rℓ14 of RL1 applys +5V to the solenoid of auto-lock, the auto-lock, however, is not released at this state.

The contact rℓ21 of RL2 applys +24V power to the VCM power amplifier.

One second after resetting EMRT signal, the circuit checks whether Accelerate DC Motor (ACDM) signal which must be set at State 0 is true or false. If ACDM is true at this state, SSL2 latch is set and then the state moves to State 3. If not true, the Sequence inhibit (SQINH) latch is set.

One second after enabling State 3, Lock Release (LKRLS) signal is set and holds for two seconds. The LKRLS signal activates relay RL3 and then +24V power is supplied to the autolock solenoid which releases the actuator lock of VCM. One second after releasing the actuator lock, the circuit checks whether the current flows through the solenoid coil or not. If correct, SSL1 latch is reset and the state moves to State 2. If not, SQINH latch is set.

One hundred-thirty milliseconds after enabling State 2, Accelerate DC Motor Enable (ACDME) which enables the acceleration at DC motor is set. DC motor is accelerated according to the phase of Speed Sensor outputs (three Hall-effect elements), which is then converted into a Set Speed (STSPD) signal once per revolution. When the rotational speed is up to 3,366 rpm (−6%), Speed Good (SPGD) signal is issued. Going-true of SPGD signal during State 2 sets the SSL4 latch, and the state moves to State 6. If the rotational speed is not up to 3,366 rpm within fifty-two seconds, SQINH latch is set.

When the DC motor is further accelerated (up to 3,600 rpm), the DC Motor Control circuit changes to inertia mode from accelerate mode. Simultaneously a Start Pulse (STARTP) signal is issued, which initiates the internal initial seek sequence. Going-true of STARTP signal during State 6 sets SSL1 latch, and then the state moves to State 7. If STARTP signal does not go true within sixteen seconds, SQINH latch is set.

The internal initial seek is performed in State 7. The detail of initial seek sequence is described in paragraph 4.6.4.1. The completion of the initial seek sequence resets SSL2 latch, and then the state moves to State 5. The incompletion of the initial seek sequence sets SQINH latch.

State 5 indicates that all power-up sequences are completed.

When DC Motor Fault (DMFL) or VCM Heat (VCMHT) malfunction occurs during any state, or a specific malfunction has occurred during each power-up sequence, the SQINH latch and Device Check (DVCK) latch are set on the drive and the condition is frozen at that state. Going-true of SQINH latch sets EMRT signal and all relays are deactivated on TVQM PCB assembly.

When check clear (CKCLR) signal which is issued from the controller or the optional operator panel during SQINH State, SSL1, 2 and 4 are reset; and the Power-up Sequence is initiated again.

The Start/Stop Control block diagram is shown in Figure 4-6-1, Power-up Sequence Control block diagram in Figure 4-6-2, Power-up Sequence flow chart in Figure 4-6-3 and Power-up Sequence timing chart in Figure 4-6-4.

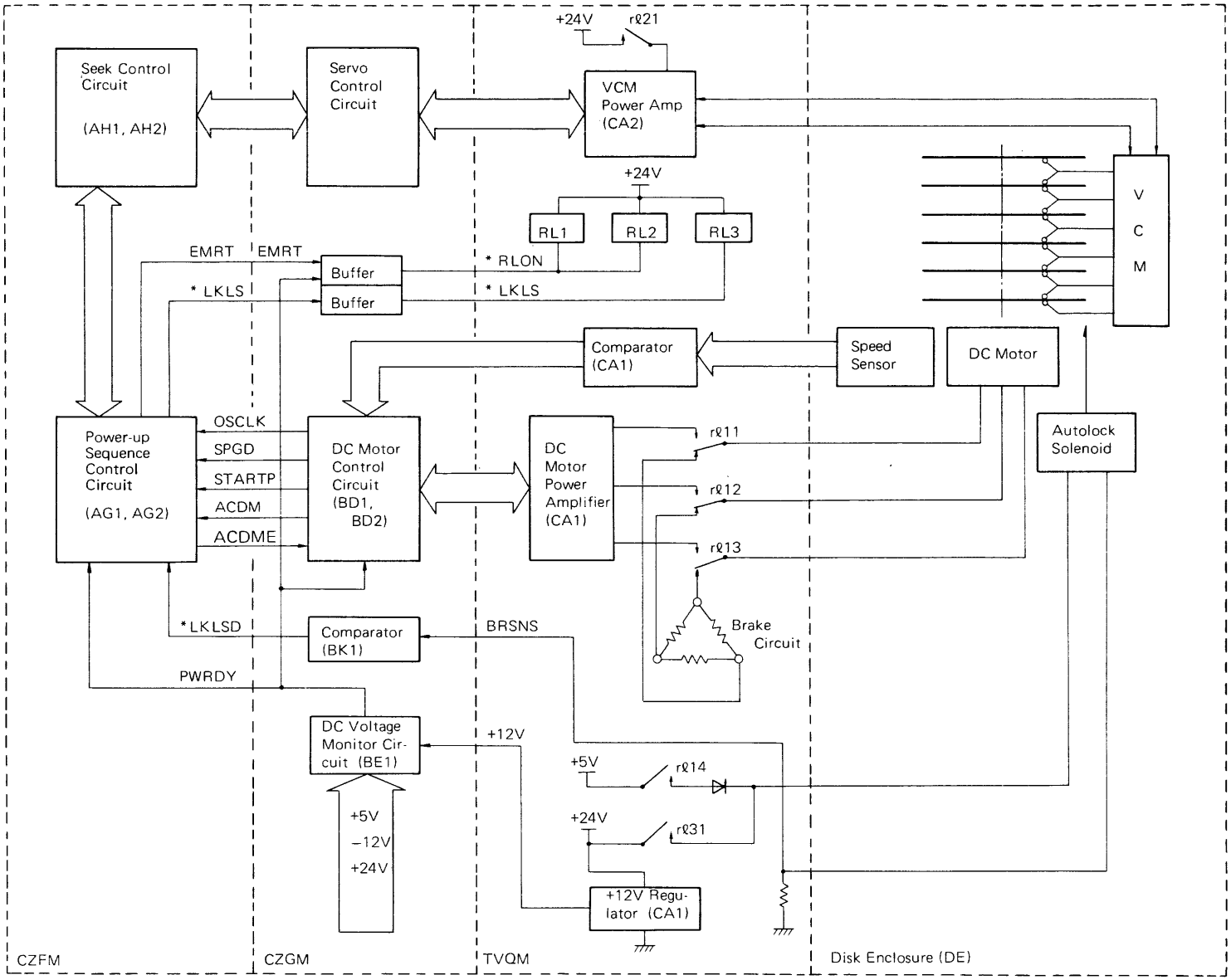


Figure 4-6-1 Start/Stop Control Block Diagram

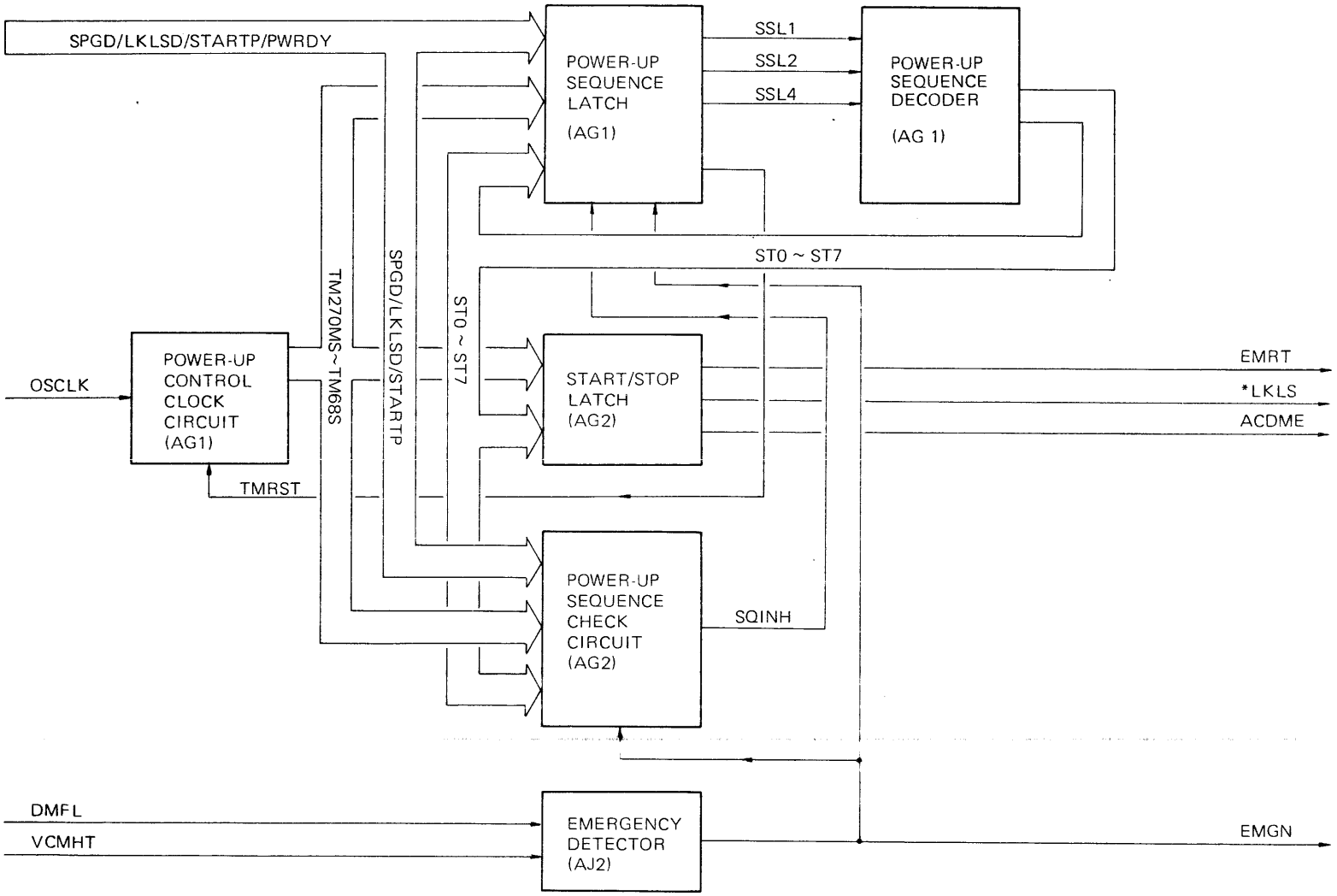


Figure 4-6-2 Power-up Sequence Control Block Diagram

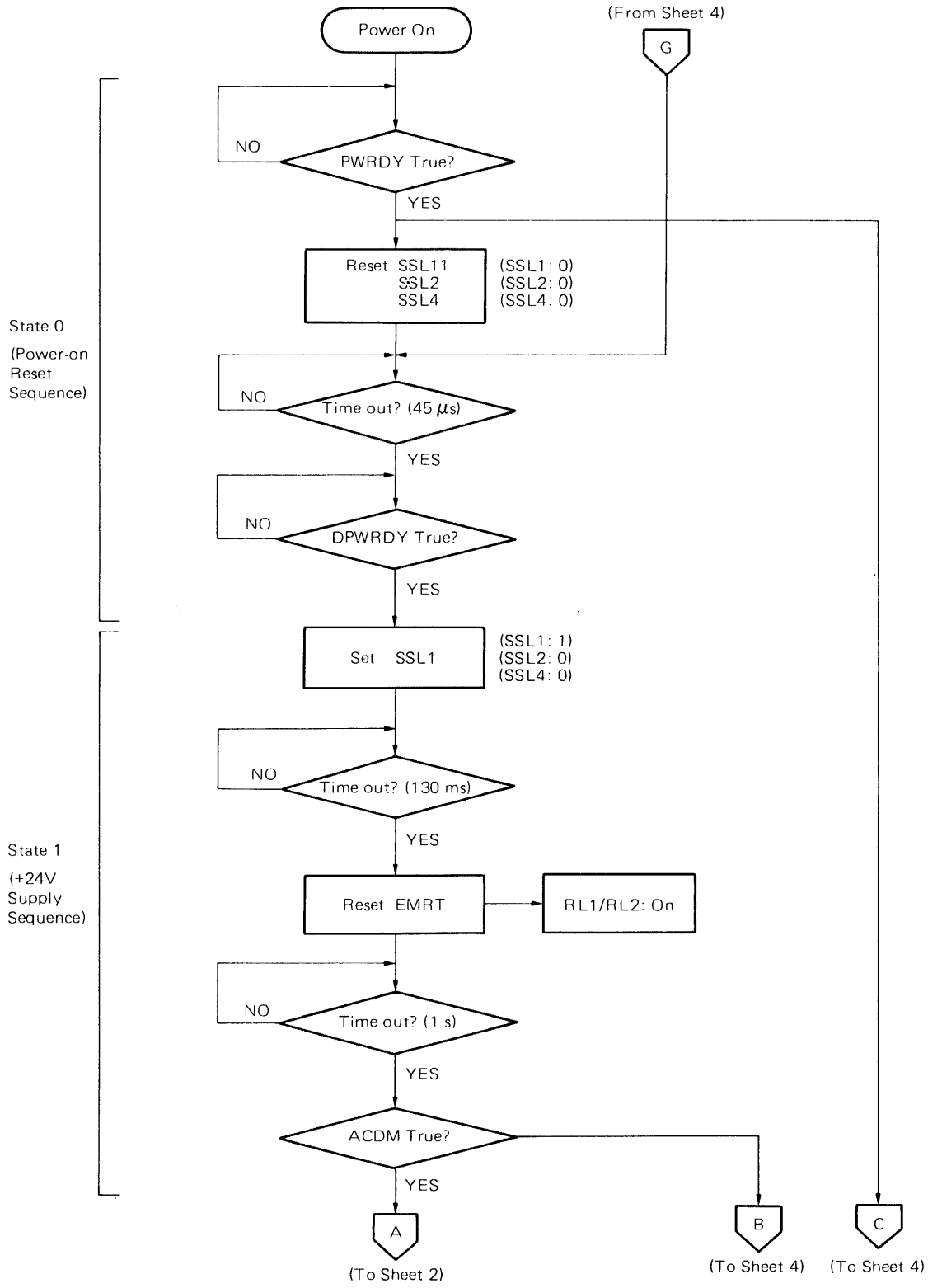


Figure 4-6-3 Power-up Sequence Flow Chart (Sheet 1 of 4)

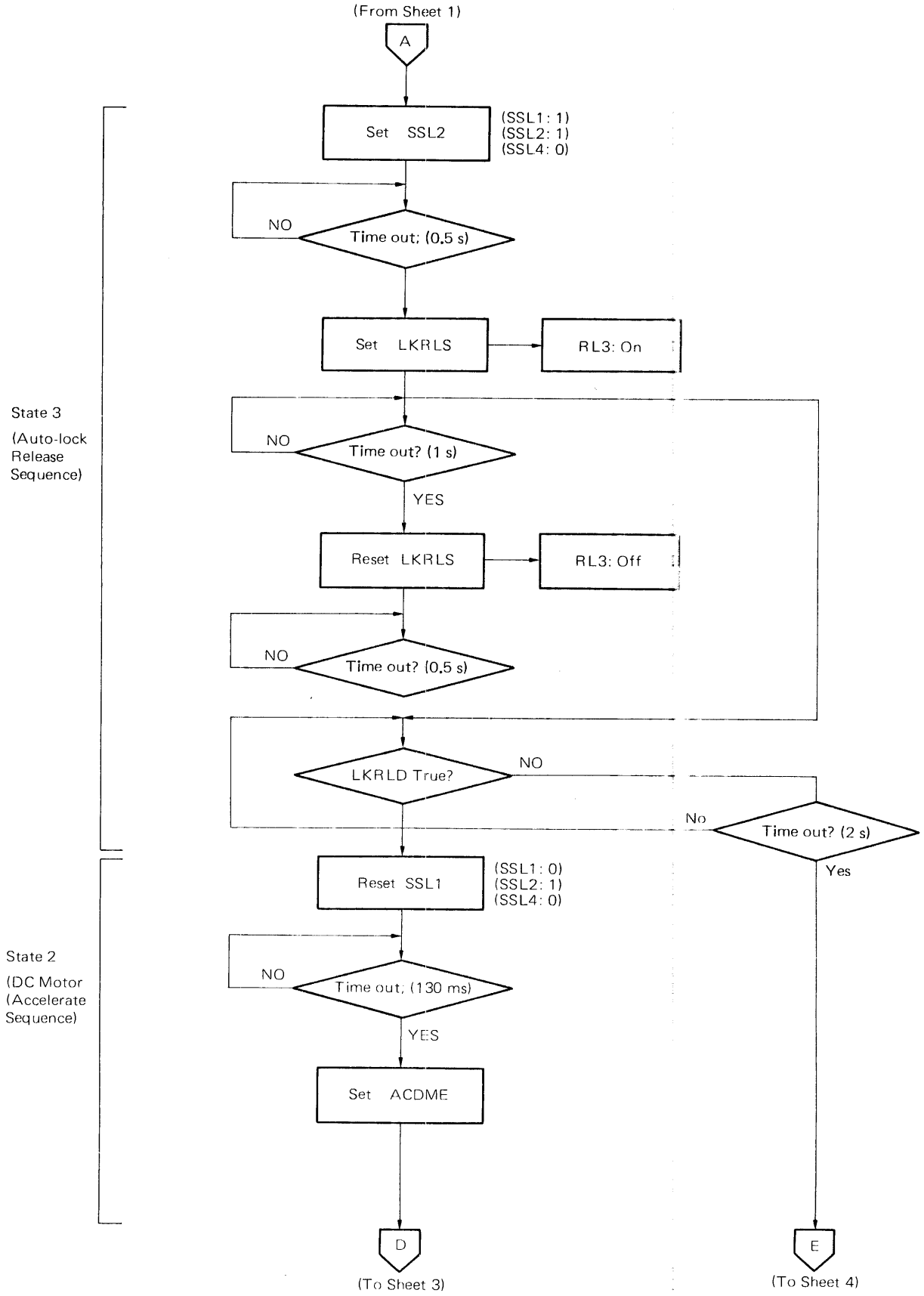


Figure 4-6-3 Power-up Sequence Flow Chart (Sheet 2 of 4)

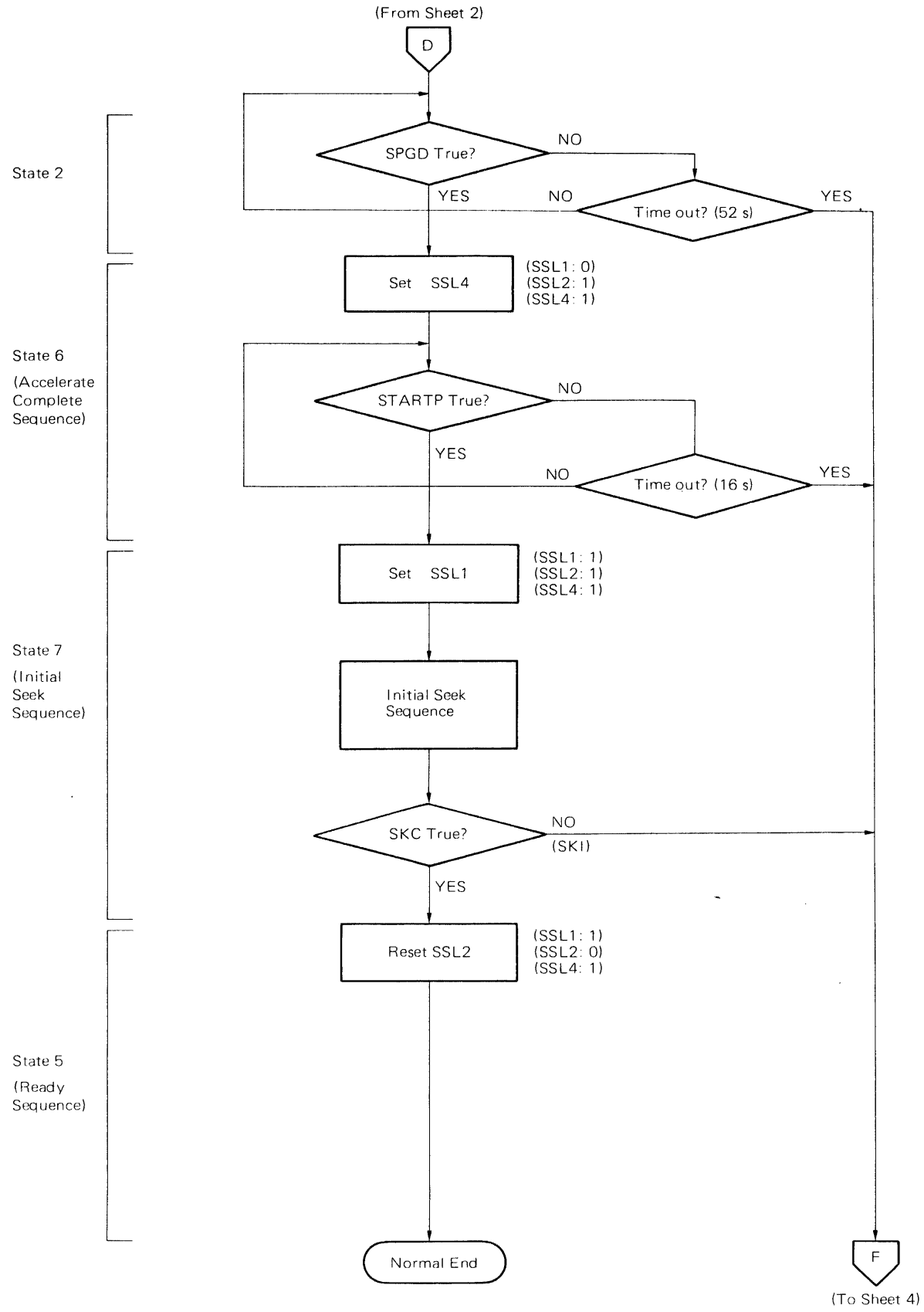


Figure 4-6-3 Power-up Sequence Flow Chart (Sheet 3 of 4)

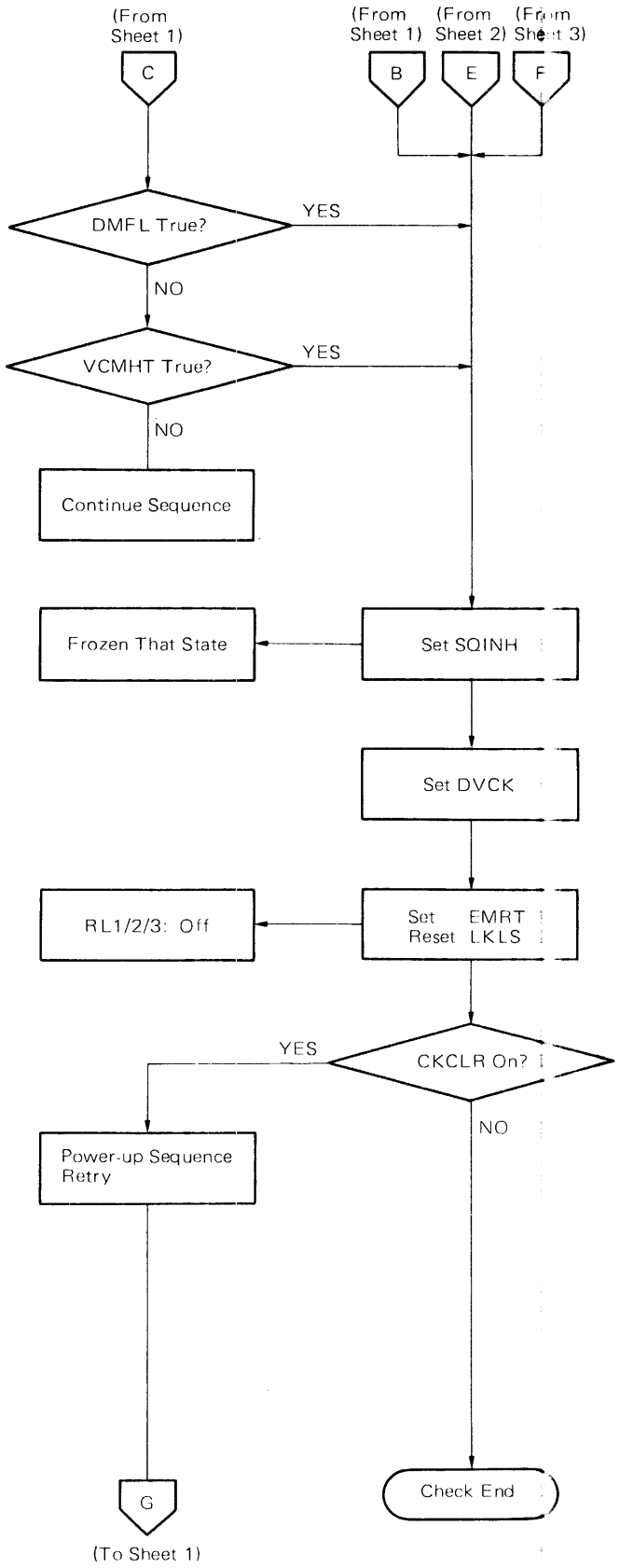


Figure 4-6-3 Power-up Sequence Flow Chart (Sheet 4 of 4)

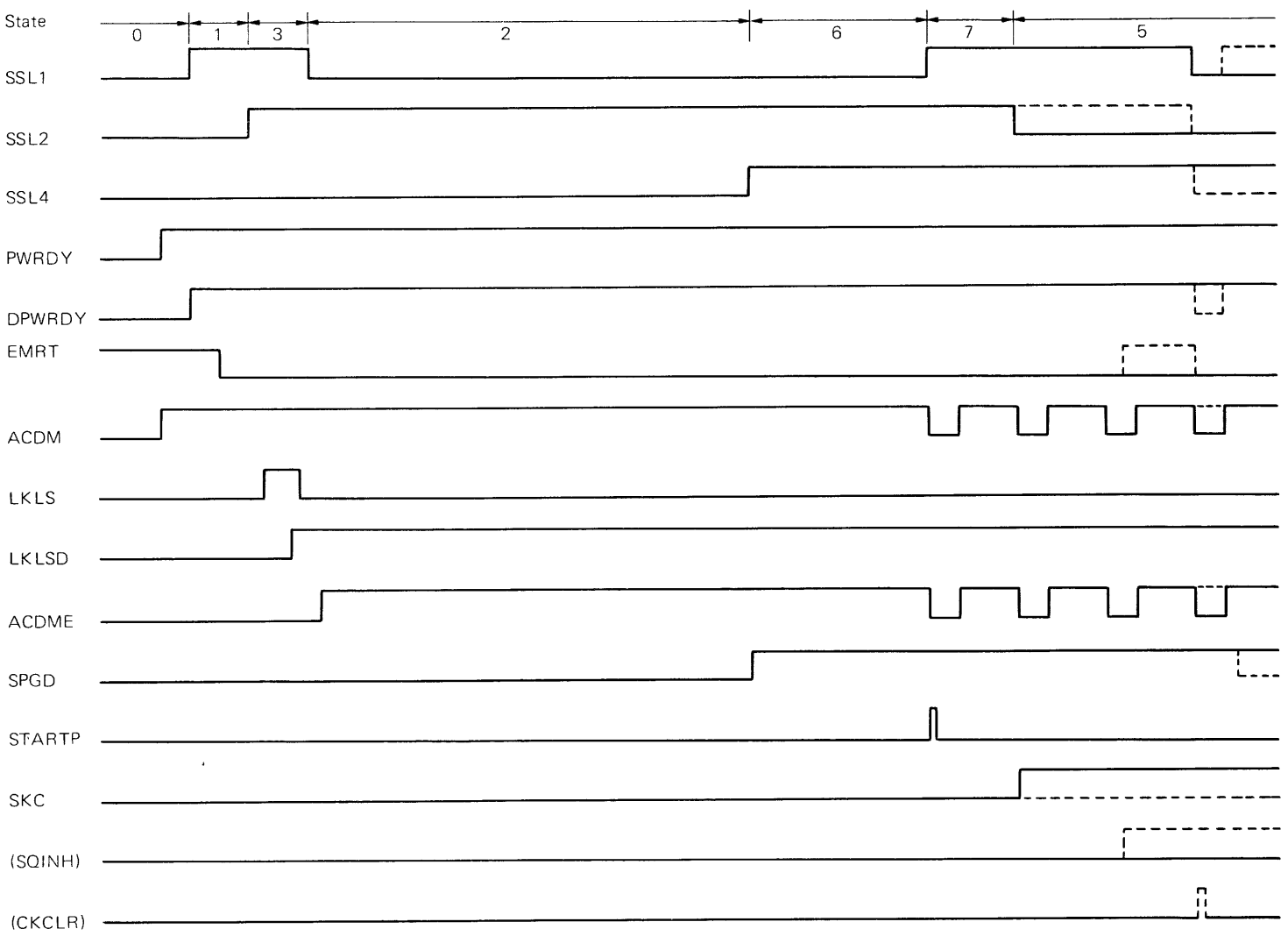


Figure 4-6-4 Power-up Sequence Timing Chart

4.6.2 DC Motor Control

The block diagram of DC Motor Control is shown in Figure 4 6-5.

As mentioned in Section 4.6.1 (Start/Stop Control), the ACDME signal initiates the acceleration of the DC Motor according to the phase outputs of the Speed Sensor. During the start-up sequence, the Current Limiter limits the winding-flow current to 4.0A nominal by detecting the voltage level at the bleeder resistor.

When the spindle rotation is initiated by initial stage, the Speed Sensor output is converted into TTL level signals (Phase A, B and C: PHA, PHB and PHC), are then applied to Speed Detect and DC Motor Fault Detect circuits. The PHA, PHB, and PHC signals have two cycles per revolution.

The positive-going edge of PHA signal sets the next latch and the negative-going edge of *PHB signal resets this latch; the latch output signal is then applied to the Clock Synchronize and Divider circuits which generate Set Speed (STSPD) and Timer Clock (TMCLK) signals once per revolution. The TMCLK signal resets the Divide Counter at the leading edge, and is also applied to the Time-out Counter. The STSPD signal is applied to the Speed Detect and Accelerate Latch circuits.

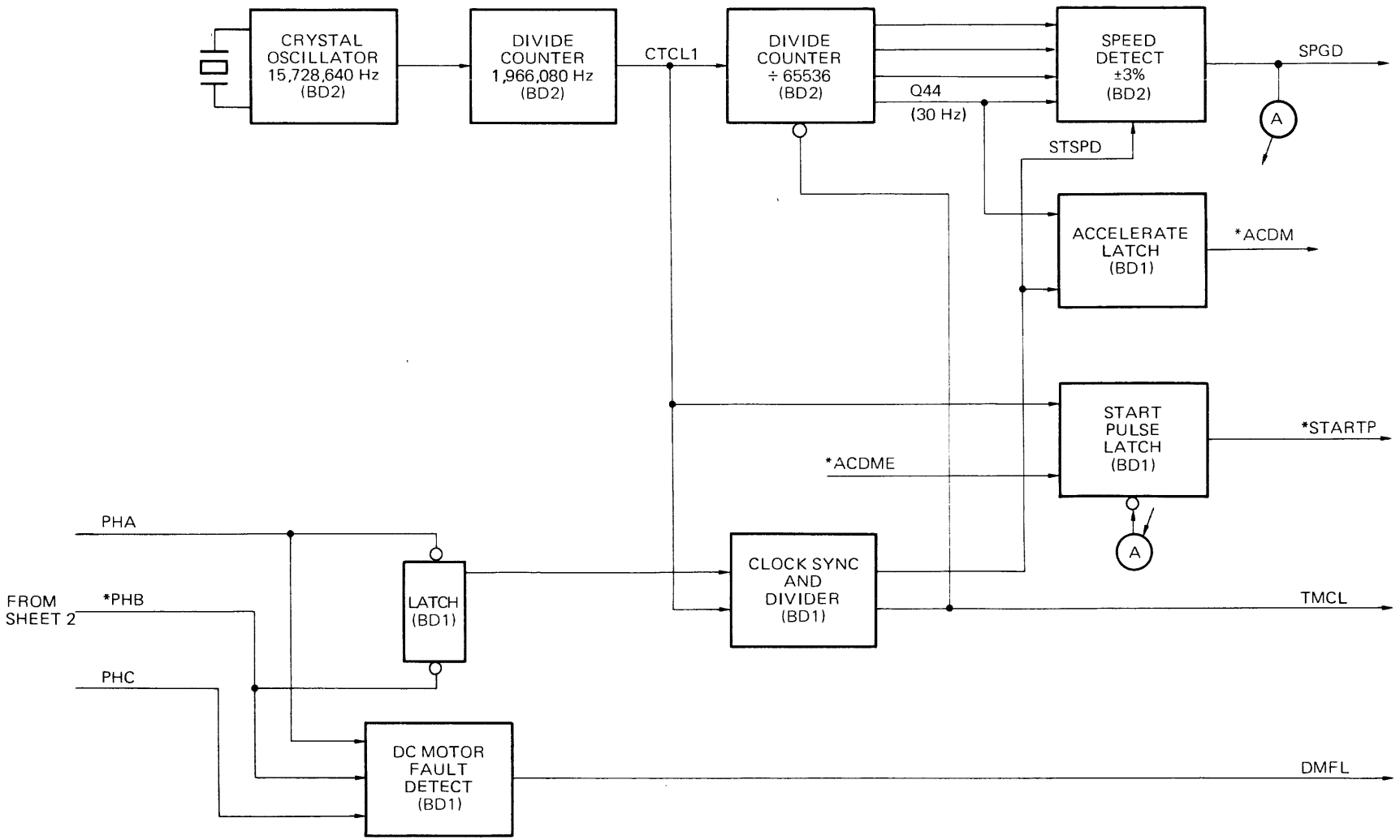


Figure 4-6-5 DC Motor Control Block Diagram (Sheet 1 of 2)

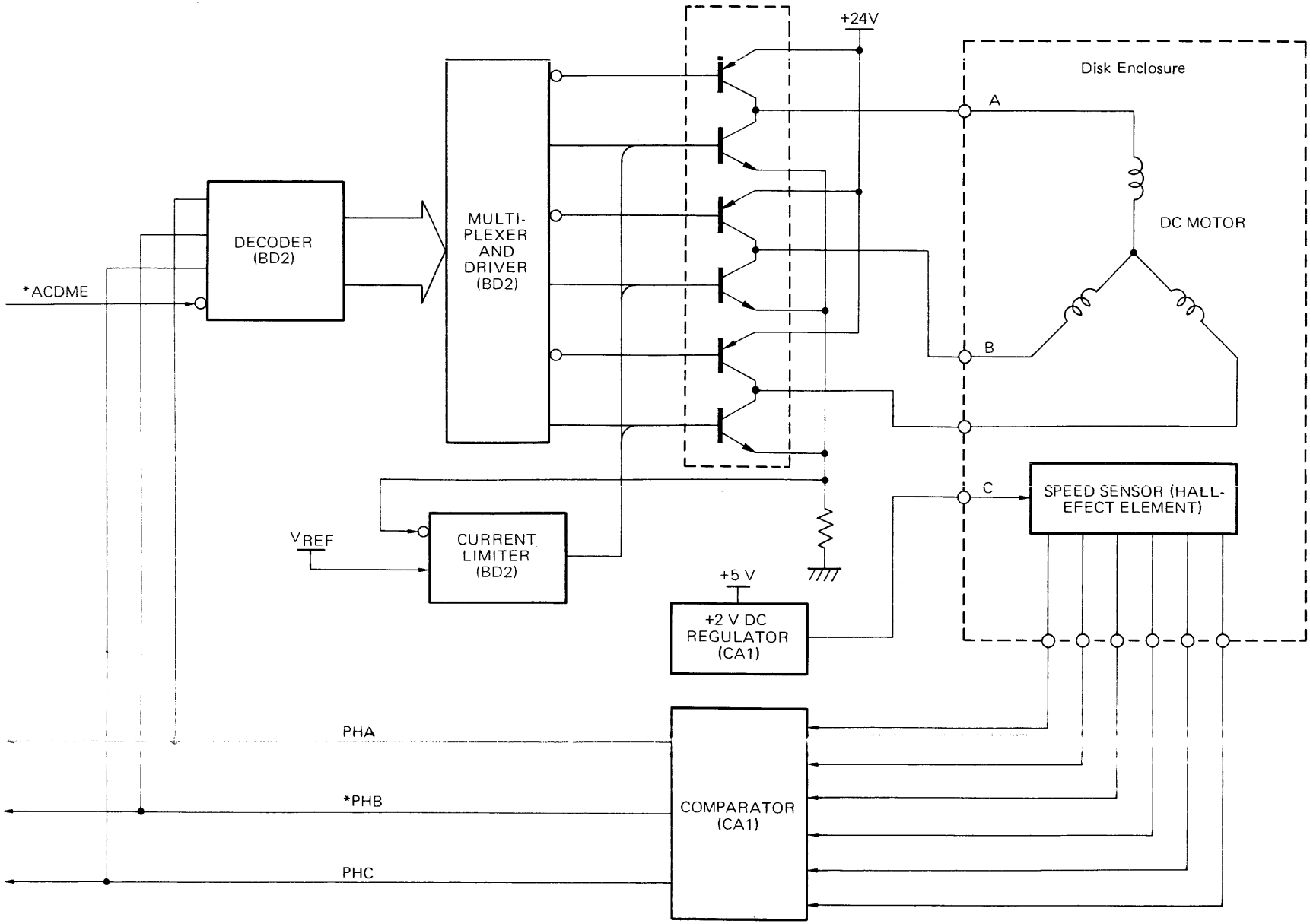


Figure 4-6-5 DC Motor Control Block Diagram (Sheet 2 of 2)

During the power-up sequence, the leading edge of the PWRDY signal sets the Q44 signal which is final stage output of the Divide Counter (Divided by 65536). The Q44 signal inhibits the count-up function of the Divide Counter until the counter is reset by the leading edge of the TMCLK signal, and also is clocked by the leading edge of the STSPD signal. When the Q44 signal goes true, this indicates that the rotational speed is slower than nominal speed. When the rotational speed is within ±6% of nominal speed, the Speed Good (SPGD) signal goes true.

About thirty-five seconds after power on, when the Q44 signal is false at the leading edge of the STSPD signal, DC Motor control mode is changed to inertial mode from accelerate mode. Simultaneously, the STARTP signal, which starts the initial seek sequence, is issued at the first negative going-edge of the ACDM signal. The DC Motor control then repeats the accelerate mode and inertia mode and maintains the rotational speed at 3,600 rpm ±1%.

The timing chart of the DC Motor power-up sequence is shown in Figure 4-6-6.

In accelerate mode the ACDM signal is set by the leading edge of the STSPD which clocks the Q44 signal, and the PHA, *PHB and PHC signals are decoded into binary signals. By combining of these decoder outputs, the power amplifier drives the DC Motor windings as shown in Figure 4-6-7.

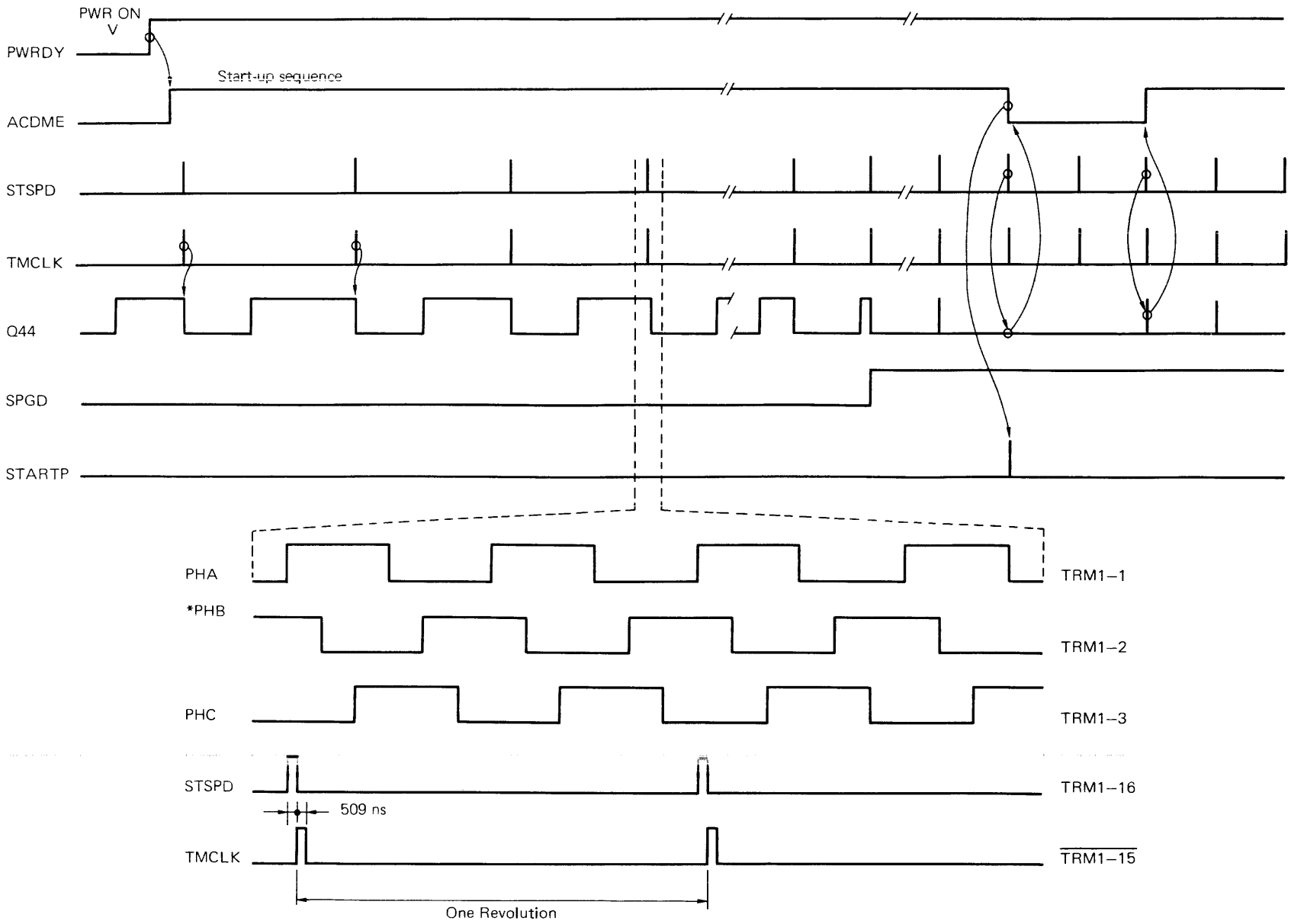
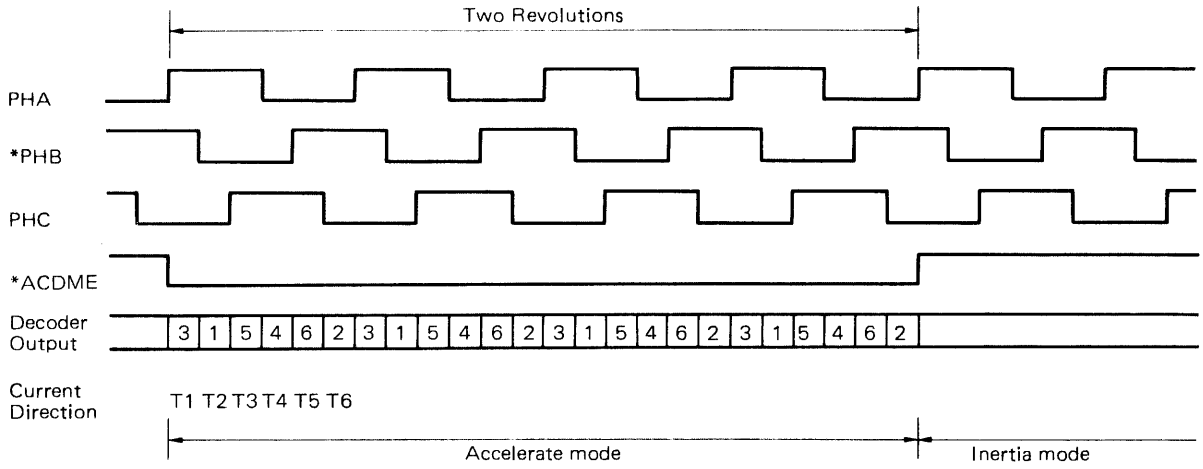


Figure 4-6-6 Power Up DC Motor Control



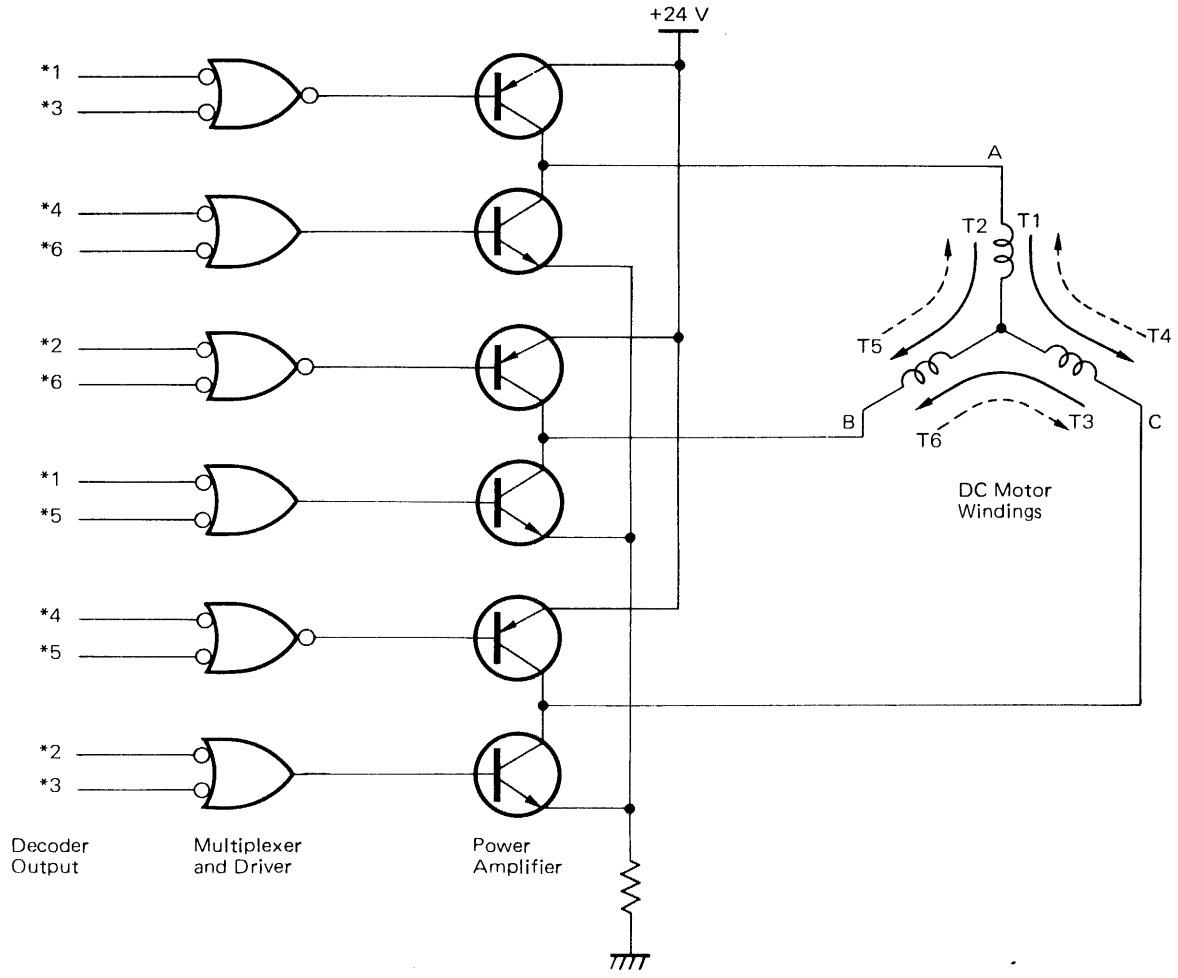


Figure 4-6-7 DC Motor Accelerate/Inertia Mode Control

4.6.3 Unit Selection

The Micro Disk Drive must be selected before it will respond to any commands from the control unit. Tag and Bus receivers are not enabled until the unit is selected.

This describes the dual channel functions related to selection. They are as follows:

- Unit address select
- Reserve
- Release
- Priority select (unconditional reserve)
- Disable with a maintenance switch

The functional block diagram of dual port is shown in Figure 4-6-8.

4.6.3.1 Unit Address Select and Reserve

A unit is selected or reserved in an identical sequence which is initiated by Unit Select Tag (USLTG) and a unit address signal (Unit select 1, 2, 4: USL 1, 2, 4). However, this sequence cannot start when:

- The unit is selected and reserved by the opposite channel.
- The unit is not selected, but reserved by the opposite channel.
- The channel which has attempted to select the unit is disabled by the maintenance switch on the unit or because the unit is placed in the Priority Select state by the opposite channel.

The select/reserve sequence is as follows:

Suppose that the unit is ready to be selected that is, none of the above three conditions exists. A controller sends USLTG and USL 1, 2, 4 to the unit. If the unit address from the channel-A controller agrees with the logical unit number (LUN), the unit sends Unit Selected to the channel-A controller through cable B when Channel-A Compare (CHACMP) is sent to the XCDM printed circuit board. This sequence is the same as with the single-port configuration.

Unless the unit is selected or reserved by channel-B and, as a result, is Busy, CHACMP causes the Channel A Selected signal (CHASLD) to be sent in synchronization with Clock 1 (CLK1) from the oscillator. CHASLD turns on the Channel-A Enable (CHAENB) signal to make the driver/receiver for Channel-A ready for transmission/reception, drive the LED to indicate CHASLD, switch the WDAT/WCLK multiplexer to Channel-A, set Busy to indicate that the unit is selected or reserved by the Channel-A controller, and trigger the Set Reserve (STRSV) one-shot multivibrator to set the reserve latch.

If channel-A and B attempt to select a unit at the same time, CLK1 and CLK2 (clocks with the same frequency and different phases) determine which channel is to access the unit. As a result, Busy is set.

The STRSV one-shot multivibrator output sets the Channel A Reserved (CHARSV) latch about 300 ns after CHASLD. This CHARSV signal turns on the LED on the XCDM printed circuit board, sets BUSY A, and sets Seek End B (SKENDB) to "1" before its transmission to Channel-B. SKEND to Channel-B is kept "1" as long as the unit is reserved by Channel-A.

The unit is kept selected/reserved by Channel-A until Channel-A is disabled by the maintenance switch or until USLTG becomes false. When Channel-B attempts to select the unit, the unit sends BUSYA as a busy signal to Channel-B, and sends also Unit Selected B (USLDB) to indicate that it is selected/reserved by Channel-A.

Even when USLTG from Channel-A goes false after the select/reserve sequence, the unit remains reserved by Channel-A. This reserved state is not reset until a Release command comes from Channel-A, Channel-A is disabled by the main-

tenance switch, Channel-B performs Priority Select, or the power is turned on/off.

If the opposite channel control unit attempts to select a channel while it is selected or reserved by the other channel control unit (i.e. in Busy state), Tried Latch in the dual channel is set. Thus, at the time when the one channel becomes neither selected nor reserved, Seek End goes faise for 30 μs so that the opposite channel, having been waiting, can interrupt.

If the unit is in Disabled state (realized by Priority Select from the opposite channel or by Disable switch) and the other channel attempts to select the unit, no signal response is activated.

The block diagram of the select/reserve circuit is shown in Figure 4-6-9, and the related flowchart and timing chart are shown in Figures 4-6-10 and 4-6-11, respectively.

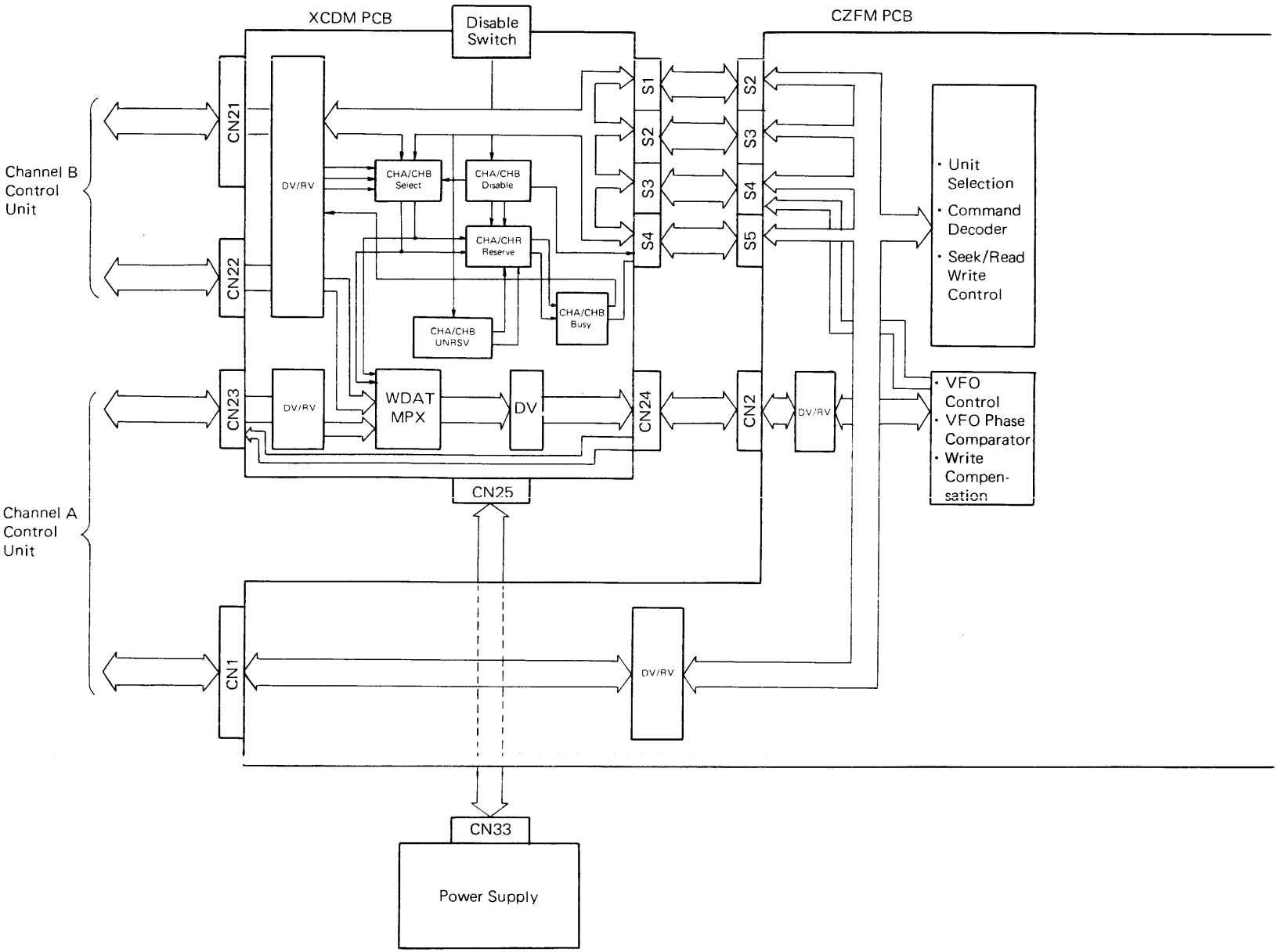


Figure 4-6-8 Functional Block Diagram of Dual Channel

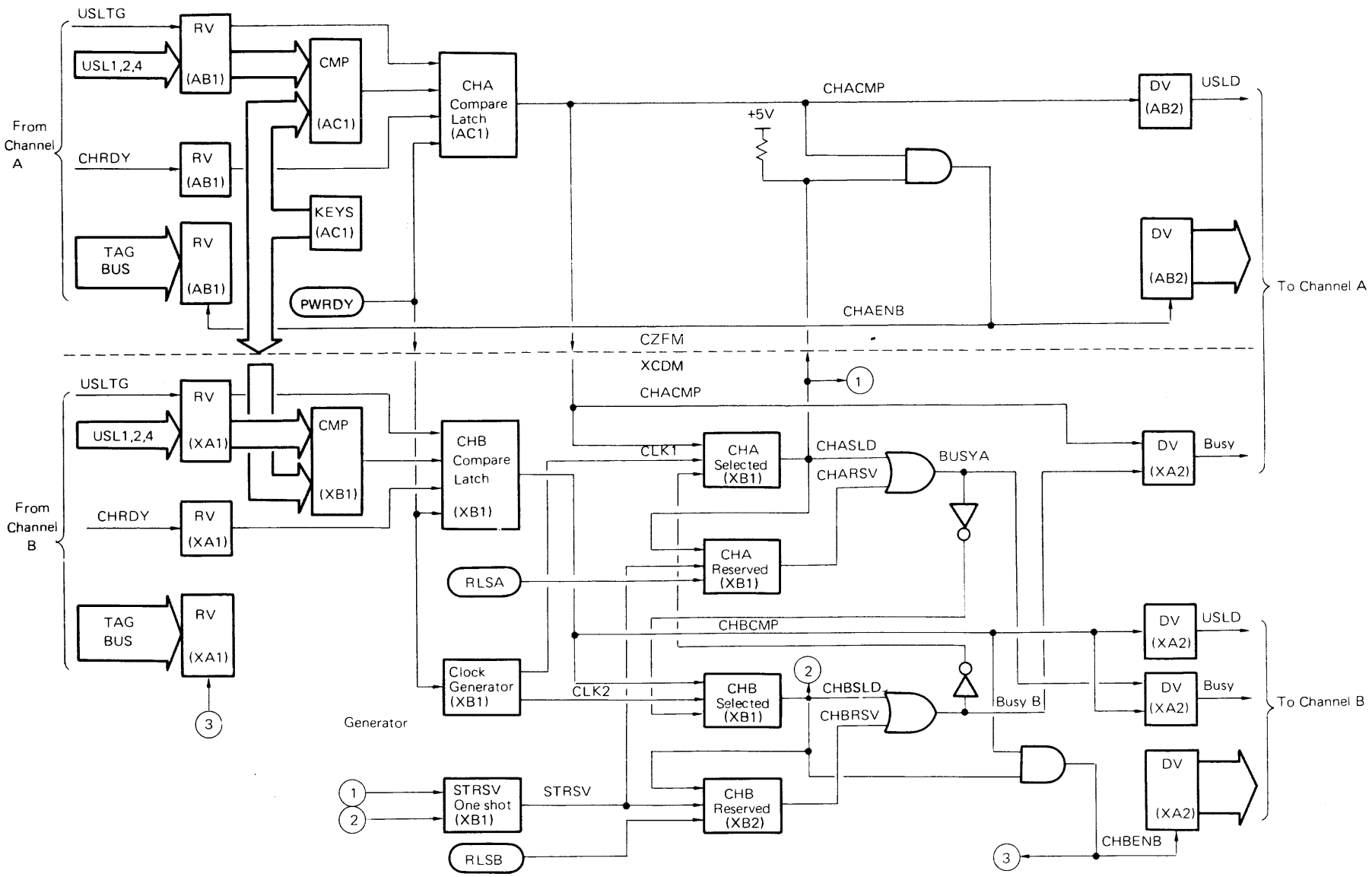


Figure 4-6-9 Functional Block Diagram of Select/Reserve

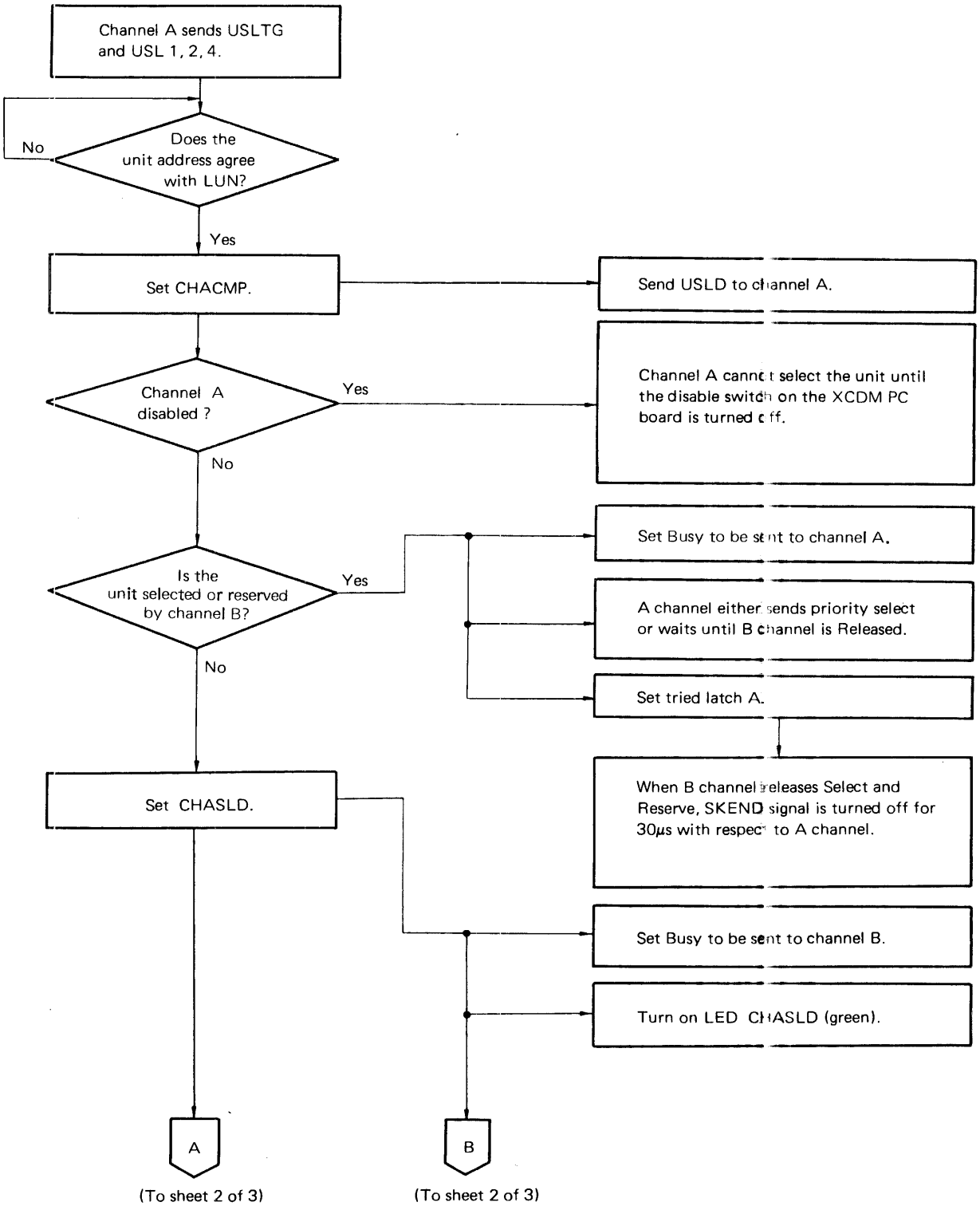


Figure 4-6-10 Select/Reserve Flow Chart (Sheet 1 of 3)

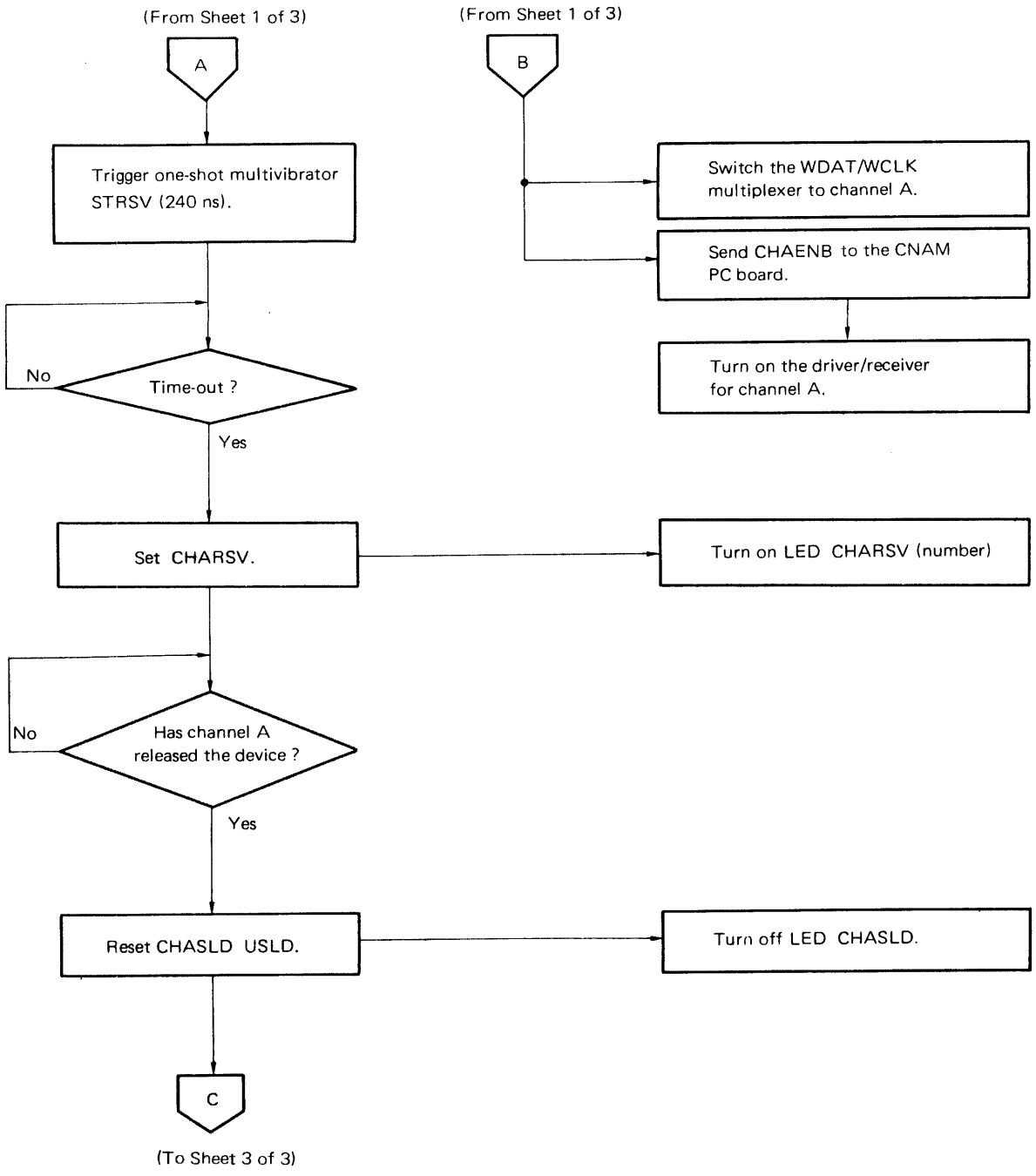


Figure 4-6-10 Select/Reserve Flow Chart (Sheet 2 of 3)

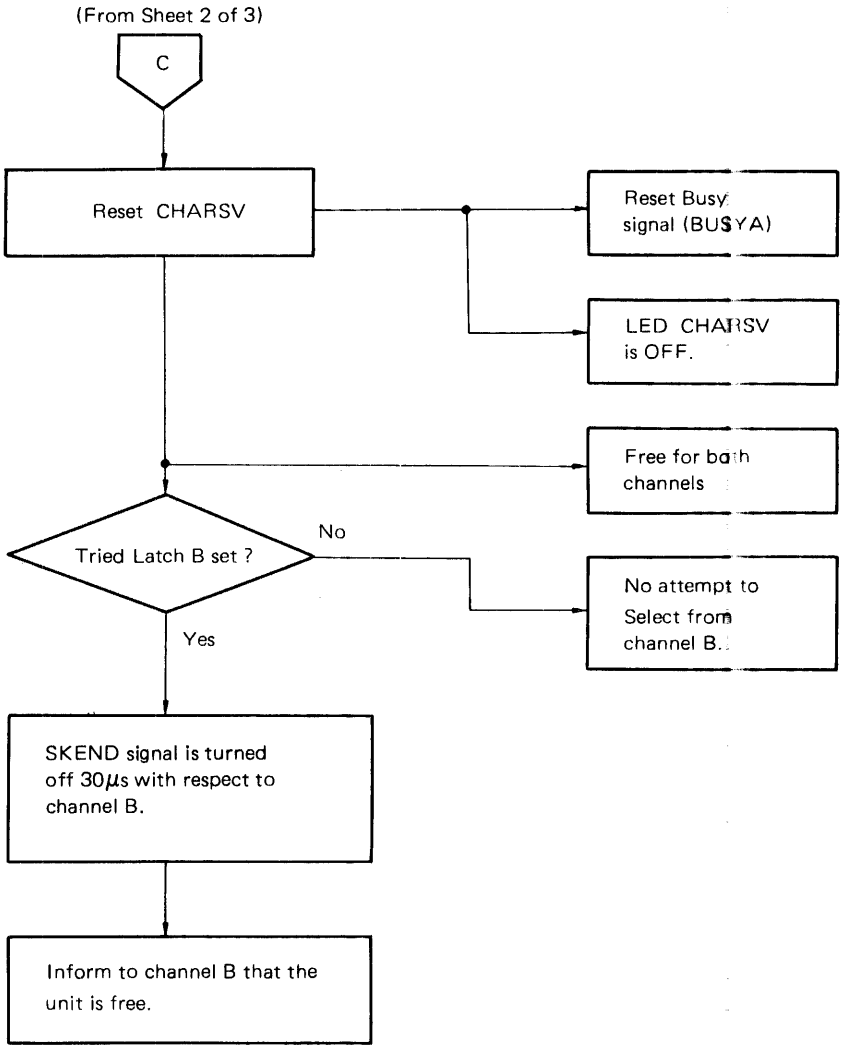


Figure 4-6-10 Select/Reserve Flow Chart (Sheet 3 of 3)

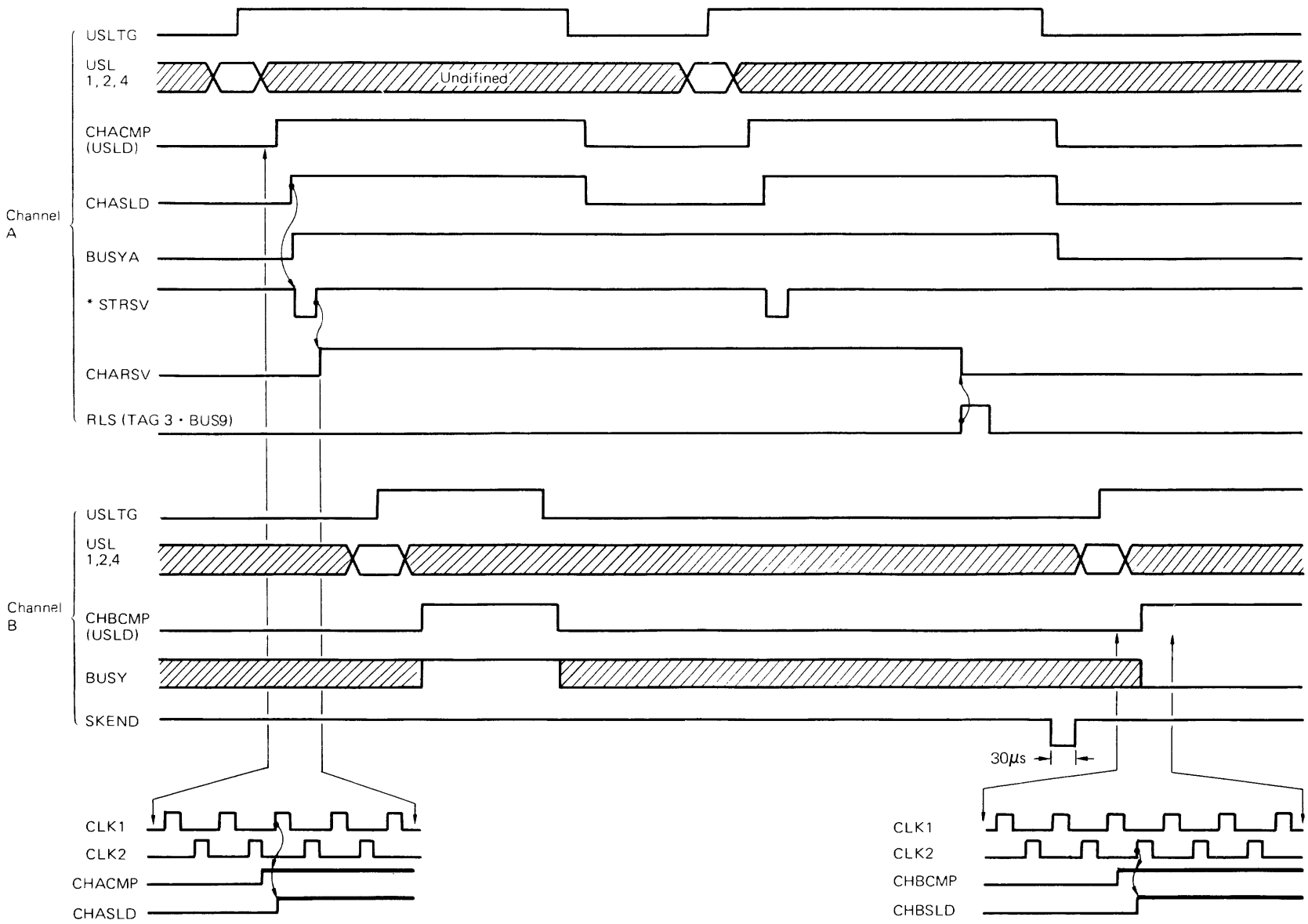


Figure 4-6-11 Select/Reserve Timing Chart

4.6.3.2 Release

The release command resets the reserved and priority select (unconditional reserve) states. Release is executed by two functions described in the following. One is a release command from a control unit (Tag 3 Bus bit 9) and the other is Release Timer of the dual channel option.

(1) Release command (Tag 3, Bus bit 9)
Reserve and Priority Select (unconditional reserve) are reset by the leading edge of Tag 3 and Bus Bit 9 sent from the control unit. Thus, it is possible to be accessed from the control unit of the opposite channel.

(2) Release Timer
If the switch on the dual channel is set to the RLTM position. The Release function is enabled by the unit itself. If unit Select Tag signal goes false when the switch is being set to the RLTM position, the Release Timer one-shot (500 ms) is triggered. The Reserve Latch is reset by the trailing edge of the Release Pulse.
If the switch is set the ABSL (Absolute Reserve) side, the one-shot is disabled.

4.6.3.3 Priority Select (Unconditional Reserve)

Even if a unit is selected or reserved (except unconditional reserve) by a channel, the opposite channel can switch the unit to its channel by issuing a Priority Select (Unit Select Tag, unit address and Bus Bit 9) command.

This command sets the Unconditionally Reserved (UCRSV) latch to inhibit all signals, Select/Reserve is given to the channel and, at the same time, the channel which was previously connected is disconnected. Once it is set in an unconditional reserve state, all signals are disabled to the opposite channel.

The Unconditionally Reserve is released only by the release command given by the channel with exclusive connection.

4.6.3.4 Disable Switch

During maintenance the interface functions released to channels A and B can be inhibited by using the maintenance switch on the XCDM printed circuit board. This disable function can be done for the two channels separately.

4.6.4 Seek Control Logic Function

The M232X has four types of seek modes: Initial Seek, Return To Zero (RTZ), Direct Seek by Tag 1, and Linear Mode.

(1) Initial Seek Mode
The Initial Seek Mode positions the heads at Cylinder 0 during power-up sequence.

(2) Return To Zero Mode
The Return To Zero (RTZ) mode moves the heads to Cylinder 0, regardless of where they are when the RTZ command is received. Return To Zero mode is essentially equivalent to the Initial Seek mode; therefore, they are both referred to as the Go To Zero (GTZ) mode.

(3) Direct Seek Mode
The Direct Seek mode causes a seek to the cylinder address specified by Bus bit 0 to 9, Tag 1 signals from the control unit.

(4) Linear Mode

Linear mode causes the heads to track the center of the specified cylinder after the seek operation has been completed. An Offset operation is available in the Linear mode.

When a power failure or seek malfunction has occurred on the unit, each seek mode is reset and the heads are returned to the Landing Zone by the retract spring in the actuator assembly.

The Seek Control Logic block diagram is shown in Figure 4-6-12.

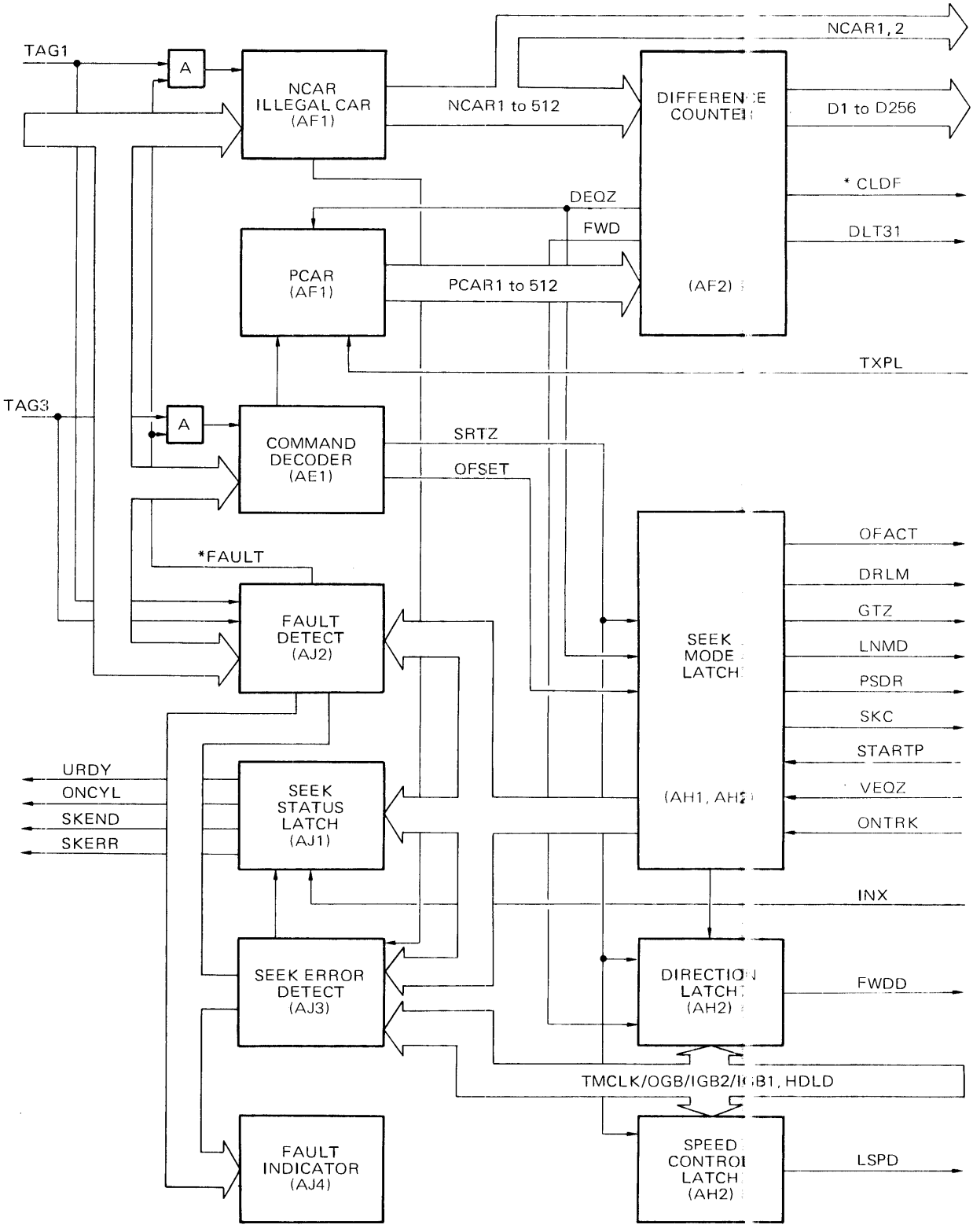


Figure 4-6-12 Seek Control Logic Block Diagram

4.6.4.1 Initial Seek Mode

The Start Pulse (STARTP) is issued to the Seek Control circuit when the spindle rotational speed has reached its nominal value. The STARTP signal sets State 7, Go To Zero Mode (GTZM), Under Sequence (UNSQ), Drive Linear Motor (DRLM), and Forward Drive (FWDD) latches, and resets the Low Speed (LSPD) latch.

At the start of Initial Seek, the heads move toward the outside of the disk (forward) at high speed by enabling FWDD and disabling Low Speed (LSPD).

When the heads have passed through the IGB2 zone and enter the IGB1 zone, the heads are driven toward the outside of the disk at low speed by enabling the FWDD and LSPD signals.

When the heads have passed through IGB1 zone, the Position Drive (PSDR) goes true, which changes the target velocity to the Position signal. When the velocity reaches the capture range, Velocity Equal to Zero (VEQZ) signal goes true which then resets the DRLM and PSDR latches and set the Linear Mode (LNMD) latch. When the LNMD signal goes true, it keeps the heads precisely on the center of Cylinder 0, that is, the first ODD1—EVEN1 and EVEN1—EVEN2 servo track.

The first Index signal under the linear mode triggers the Settling 1 one-shot (STL1:2.0 ms). The trailing edge of the STL1 signal sets the Seek End (SKEND), On Cylinder (ONCYL), and Unit Ready (URDY) latches, and also resets the GTZM, and UNSQ latches.

If the initial seek has not been performed within 4 seconds after STARTP, the Device Check goes true, Not Ready status is true. The Device Check Clear signal under the not ready status, which is commanded from the control unit or the Check Clear key, will cause a retry of the Initial Seek sequence.

The Return To Zero (RTZ) command, with a complete servo-off sequence and during the Ready status, initiates the Initial Seek sequence.

The Go To Zero flow chart is shown in Figure 4-6-13, and the timing chart for Initial Seek is shown in Figure 4-6-14.

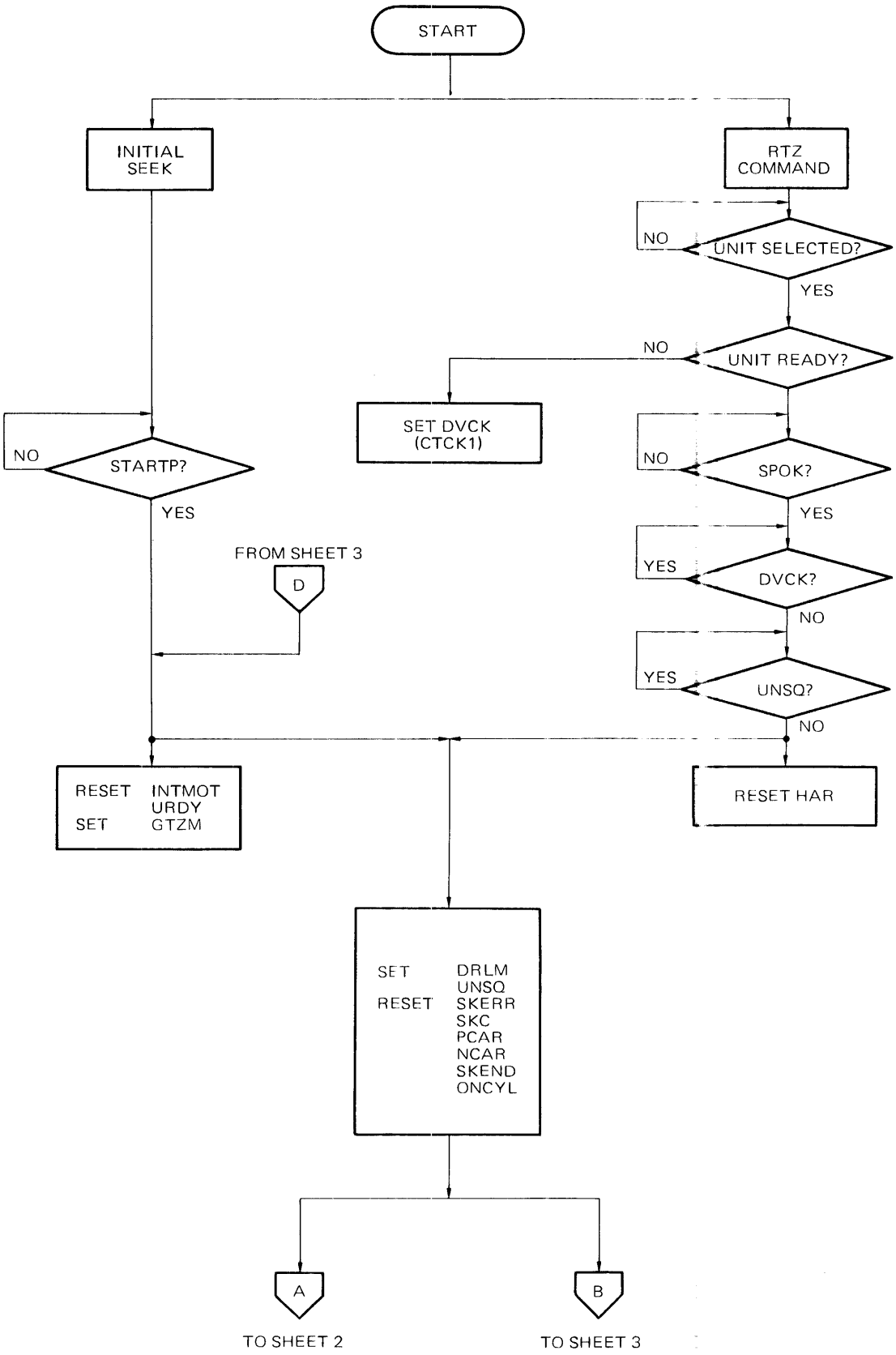


Figure 4-6-13 Go To Zero Flow Chart (Sheet 1 of 3)

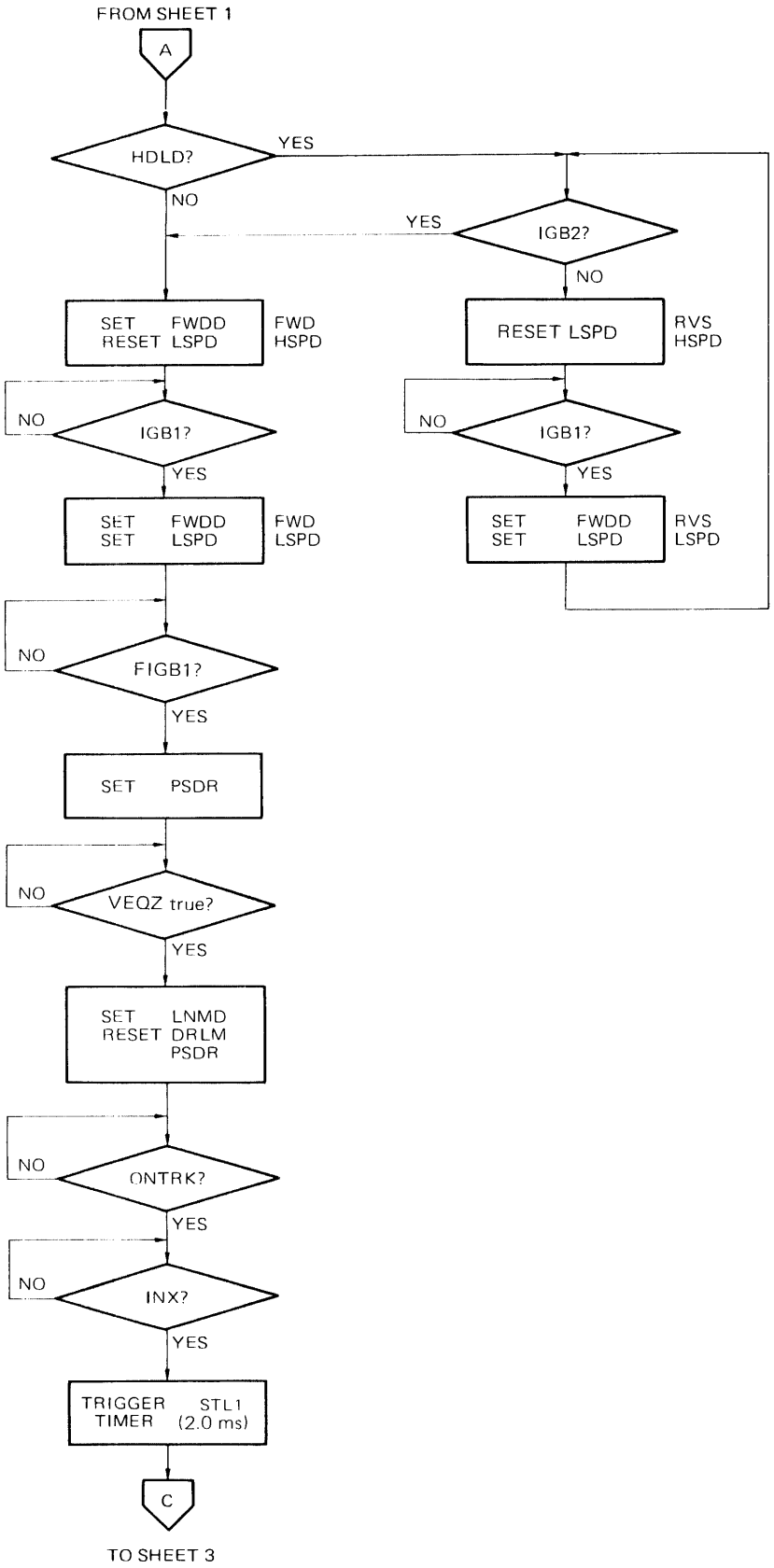


Figure 4-6-13 Go To Zero Flow Chart (Sheet 2 of 3)

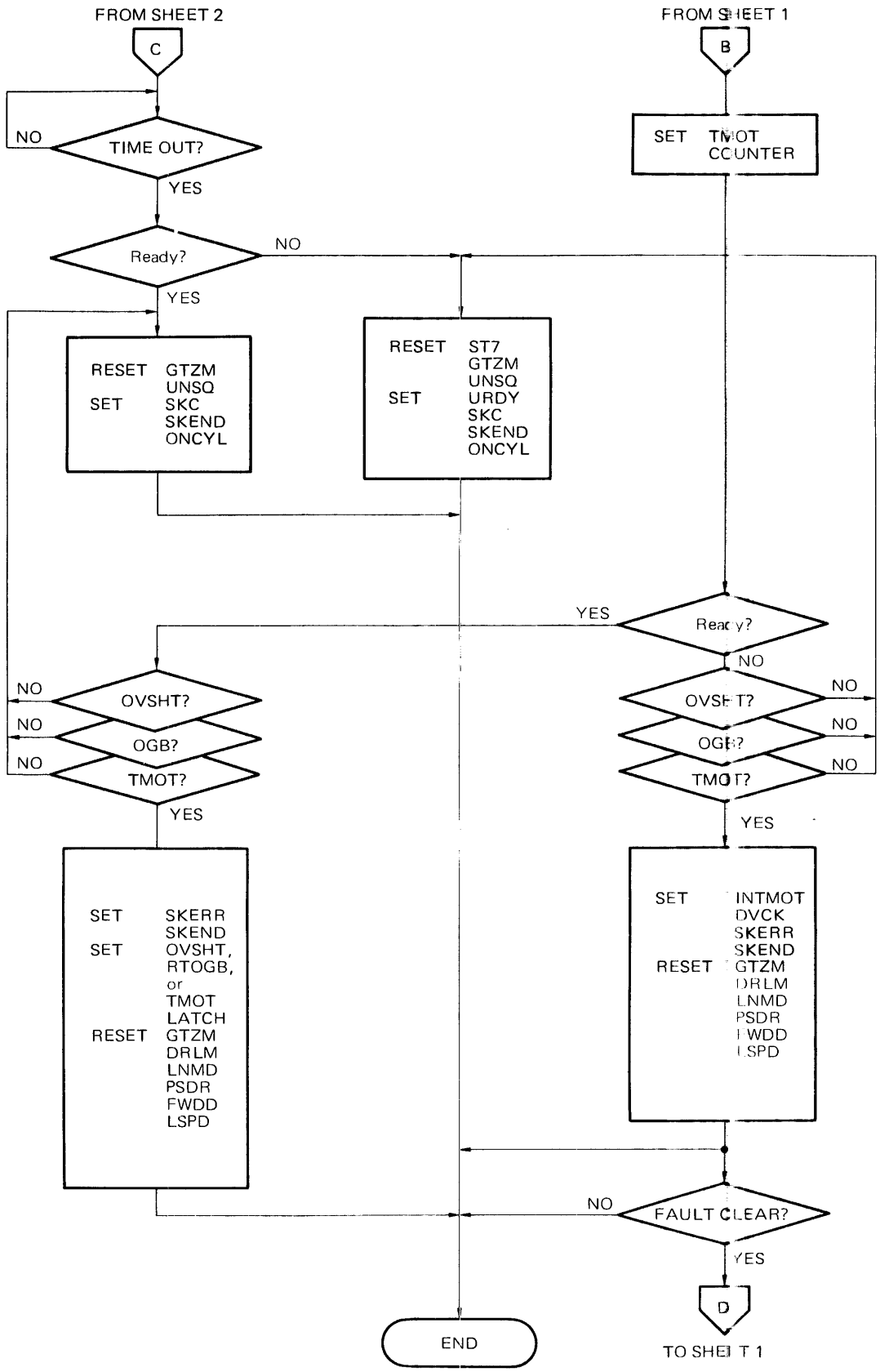


Figure 4-6-13 Go To Zero Flow Chart (Sheet 3 of 3)

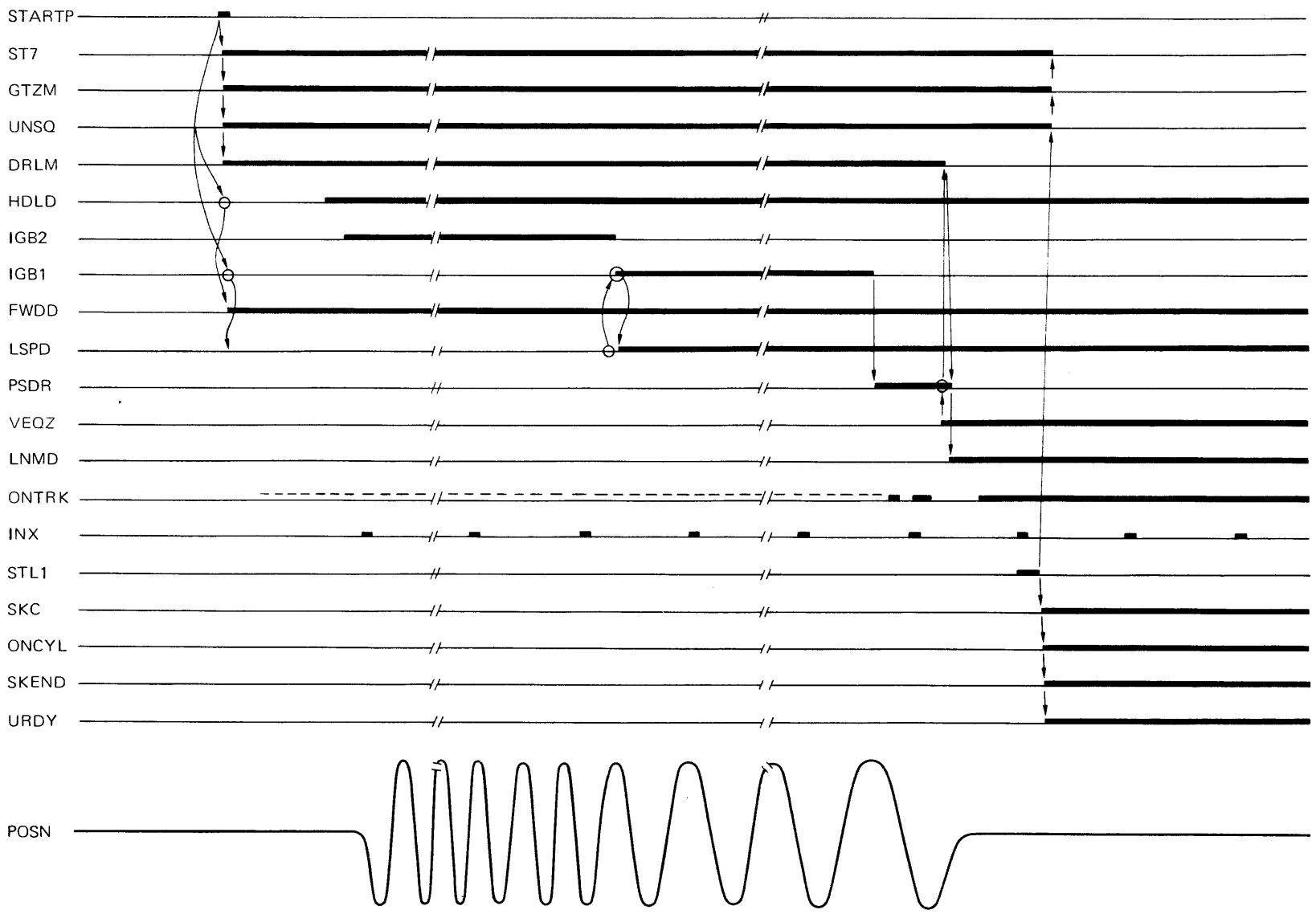


Figure 4-6-14 Initial Seek Timing Chart

4.6.4.2 Return To Zero Mode

The Return To Zero mode is initiated by a Return To Zero (RTZ) command from the control unit during Ready status and linear mode.

The RTZ command sets GTZM, DRLM, and UNSQ latches; resets SKEND, ONCYL, and Seek Error (SKERR) latches; and resets Present Cylinder Address Register (PCAR), Next Cylinder Address Register (NCAR), and Head Address Register (HAR).

At the start of GTZM, the heads move toward the center of the disk (reverse) at high speed by disabling the FWDD and LSPD signals.

When the heads have passed through the Servo Zone and enter the IGB1 zone, they are driven toward the center of the disk at low speed.

When the heads enter the IGB2 zone, they are driven toward the perimeter forward) at high speed. Upon entering the IGB1 zone again, they are driven forward at low speed.

The subsequent sequence is equivalent to the Initial Seek Mode.

The RTZ timing chart is shown in Figure 4-6-15.

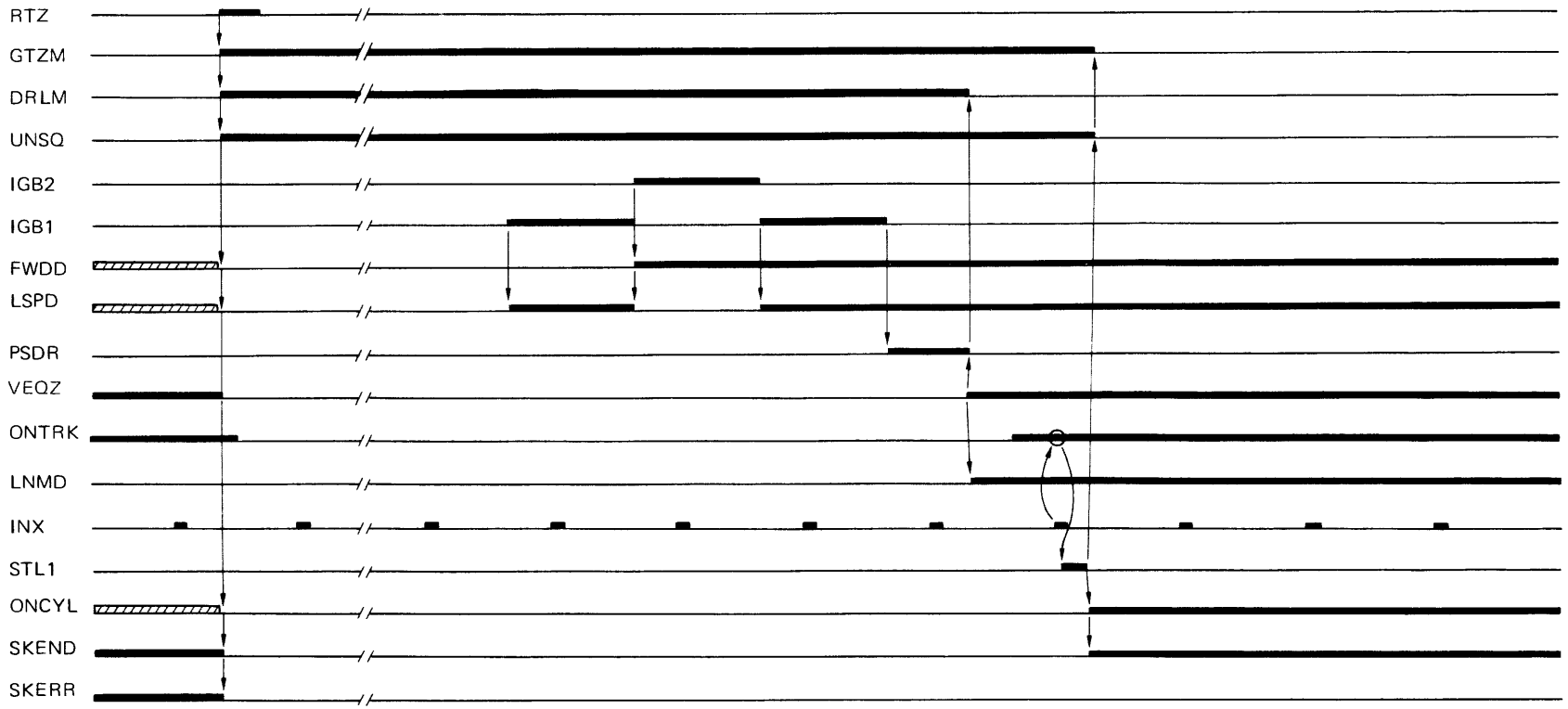


Figure 4-6-15 Return To Zero Timing Chart

4.6.4.3 Direct Seek Mode

Direct Seek mode is initiated by activating the Tag 1 signal.

The leading edge of Tag 1 sets the bus bits 0 to 9 into the Next Cylinder Address Register (NCAR) when the bus contains an address of less than 822.

When the NCAR output is not equal to the Present Cylinder Address Register (PCAR) output at the trailing edge of the Tag 1 signal (Seek Start : SEKST), a Direct Seek is initiated.

The SEKST signal resets the ONCYL, SKEND, LNMD, latches, and also sets the SEKM, DRLM, UNSQ, and direction latches.

NCAR1 and 2 signals are applied to the Servo Control circuit to determine the phase of target cylinder.

The difference between NCAR and PCAR is equal to the number of cylinders to be moved to the desired address. The difference counter outputs D1 to D256, Clamp Difference (CLDF) and Difference Less Than 31 (DLT31), is sent to the servo control circuit to generate the target velocity.

When the NCAR is greater than PCAR, the forward direction is set, and when the NCAR is less than the PCAR, the reverse direction is set using the FWDD signal.

When the heads start to move to the desired address, the Track Crossing Pulse (TXPL) is sent from the servo circuit to the PCAR counter every time the servo head crosses a cylinder. The PCAR counter is increased by the trailing edge of the TXPL signal in the forward direction, and is decreased in the reverse direction.

When the difference is equal to zero, the Position Drive (PSDR) signal is activated and the velocity follows the position signal. When the VEQZ signal goes true, LNMD latch is set, and DRLM and PSDR latches are reset. The successive ONTR signal triggers the Settling 1 (STL1) one-shot (2.0 ms). The trailing edge of STL1 signal sets the ONCYL and SKEND latches and reset the SEKM and UNSQ latches.

If NCAR is equal to PCAR at the leading edge of Tag 1, a No Motion Seek (NOSEK) signal is activated and triggers Settling 2 (STL2: 5μs) one-shot. The ONCYL and SKEND signals are reset by the trailing edge of the TAG1 signal and then ONCYL and SKEND signals go true at the trailing edge of STL2 signal.

If an illegal cylinder address (CAR > 822) is issued from the control unit, the trailing edge of the TAG1 signal resets the ONCYL and SKEND signals and then sets the Seek Error (SKERR) and SKEND signals immediately. The LNMD latch is also reset and the heads move to the Landing Zone.

The Direct Seek flow chart is shown in Figure 4-6-16 and the timing chart is shown in Figure 4-6-17.

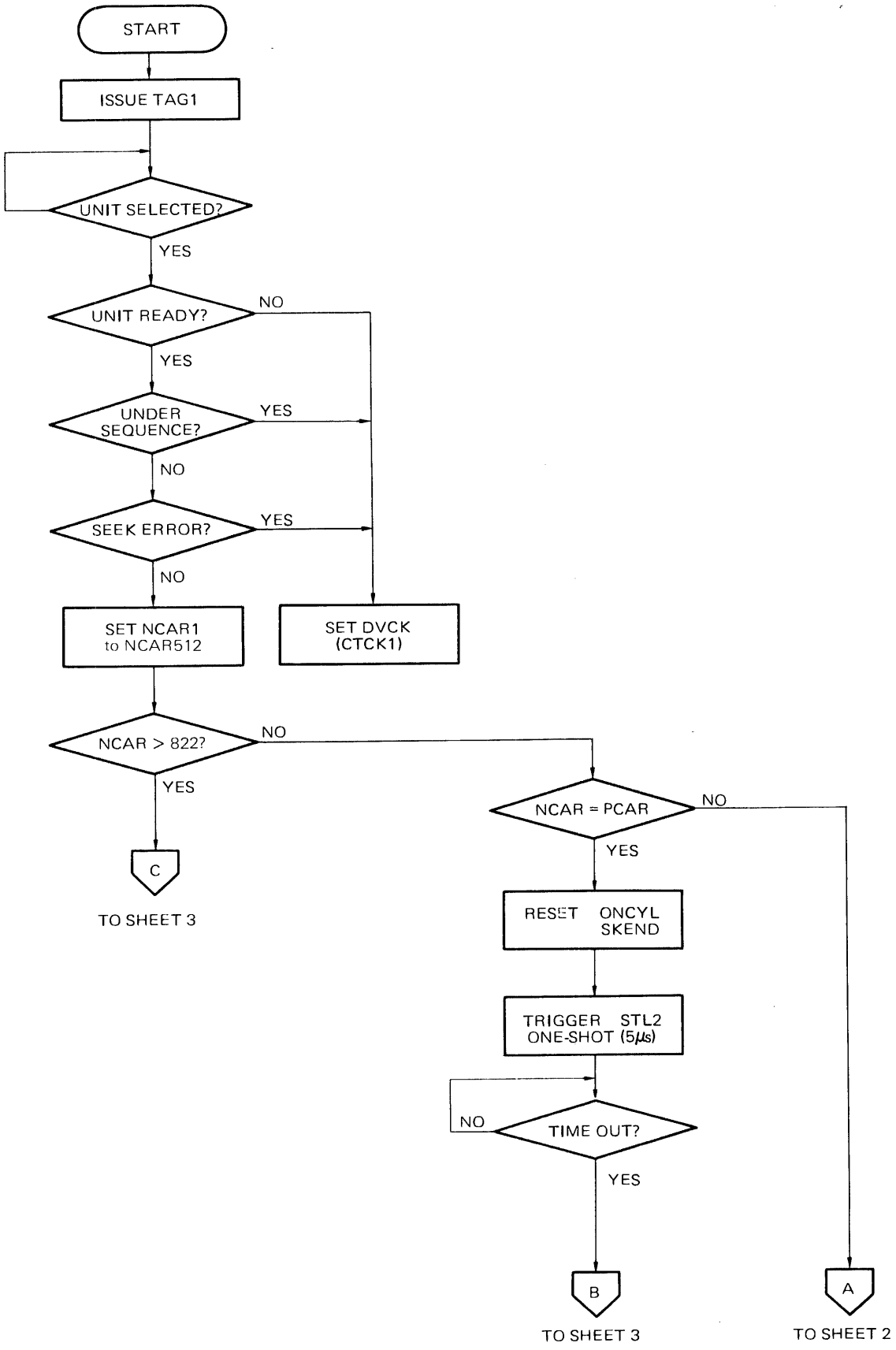


Figure 4-6-16 Direct Seek Flow Chart (Sheet 1 of 3)

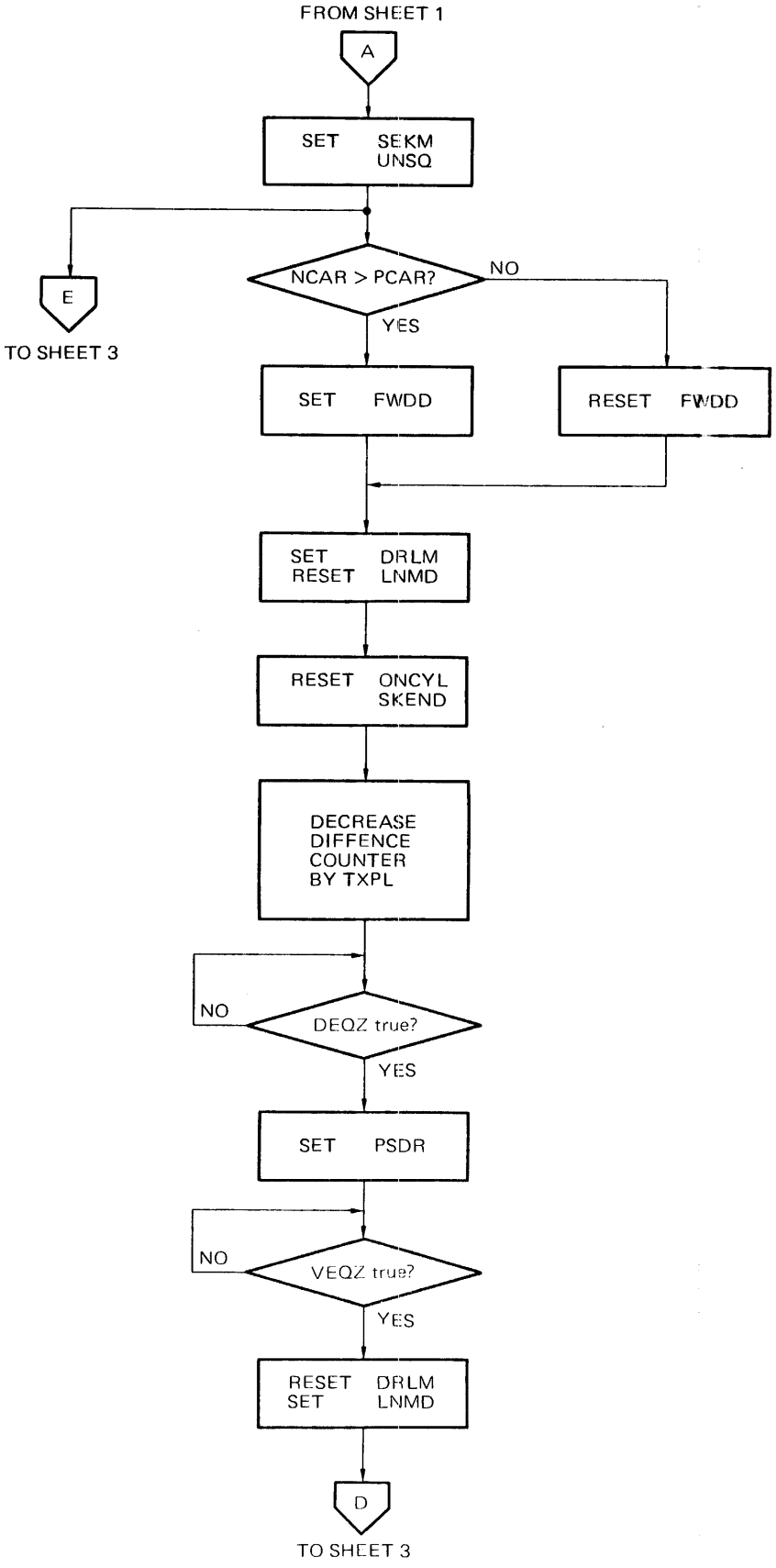


Figure 4-6-16 Direct Seek Flow Chart (Sheet 2 of 3)

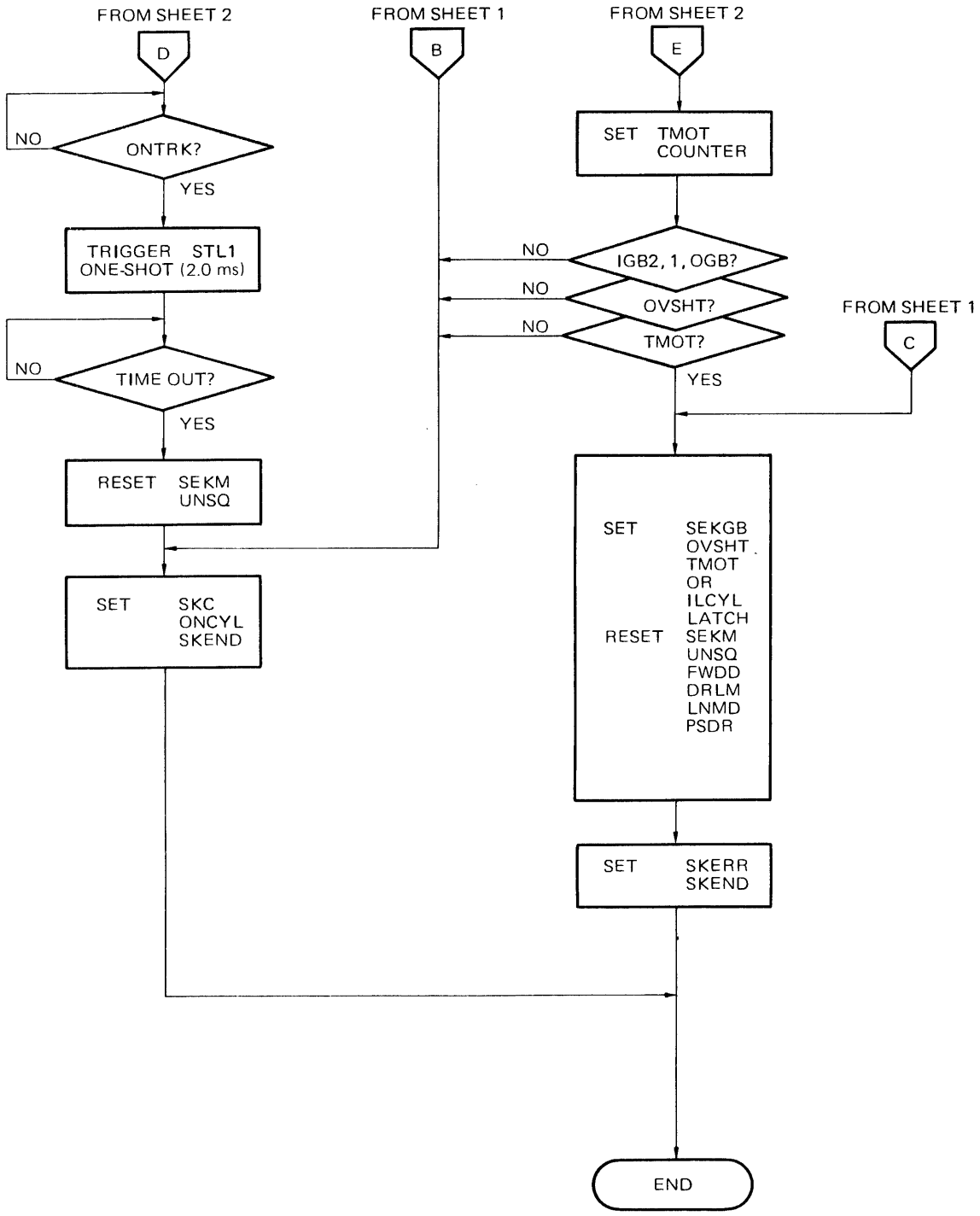


Figure 4-6-16 Direct Seek Flow Chart (Sheet 3 of 3)

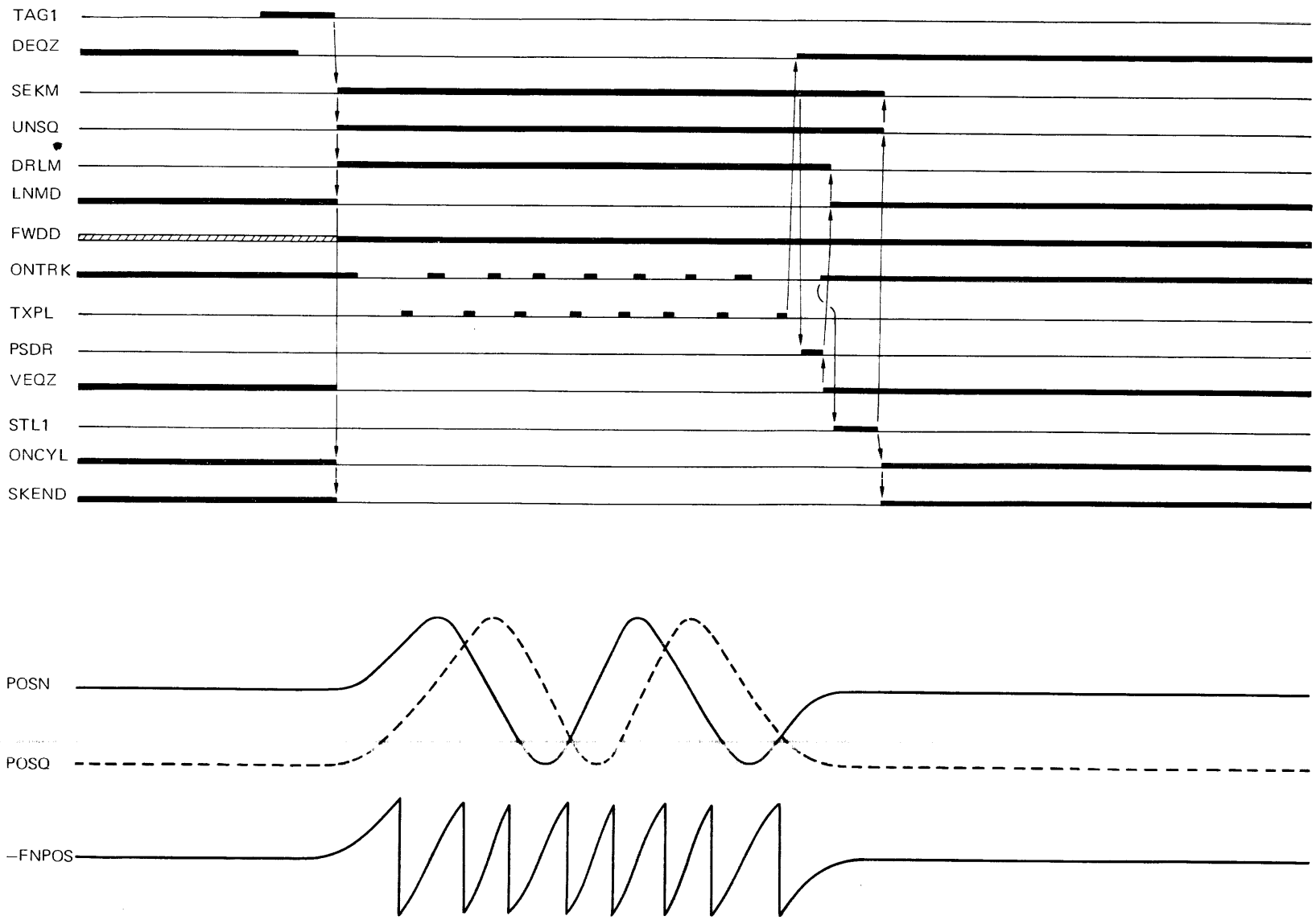


Figure 4-6-17 Direct Seek Timing Chart

4.6.4.4 Servo Off Mode

If a seek malfunction shown in Table 4-6-1 occurrs in the drive, all servo modes (INSKM, GTZM, SEKM, and LNMD) are reset and the heads move to the Landing Zone by the mechanical force of the retract spring in the actuator assembly.

Table 4-6-1 Seek Malfunctions

ERROR	UNIT STATUS
Initial Seek Time Out	Not Ready
Rotational Speed High or Low	Not Ready
DC voltage fault	Not Ready
Time Out in Any Seek Mode	Seek Error
Over-shoot in Linear Mode	Seek Error
Any Guard Band in Seek Mode	Seek Error
OGB in Go To Zero Mode	Seek Error
Any Guard Band in Linear Mode	Seek Error
Illegal Cylinder (CY > 822)	Seek Error

4.6.5 Servo Circuit Function

4.6.5.1 Position Sensing

This section describes the Position Sensing functions from the output of the servo head to generating the position signal. The Position Sensing block diagram is shown in Figure 4-6-18.

The servo data written on the servo surface is read by the servo head, amplified through the Head-Preamplifier (with a nominal gain of 35), and applied to the Automatic Gain Control (AGC) amplifier on CZGM PCB. The AGC amplifier keeps the output constant with an AGC voltage from the Summing Amplifier, even if the AGC input varies. The AGC output is applied to a Low Pass Filter (LPF), which attenuates the unused high frequencies, and then is amplified by the Carrier Amplifier. The Carrier Amplifier issues the Servo (SERVO) signal of four-byte interval to the Level Slice and Peak Hold circuits.

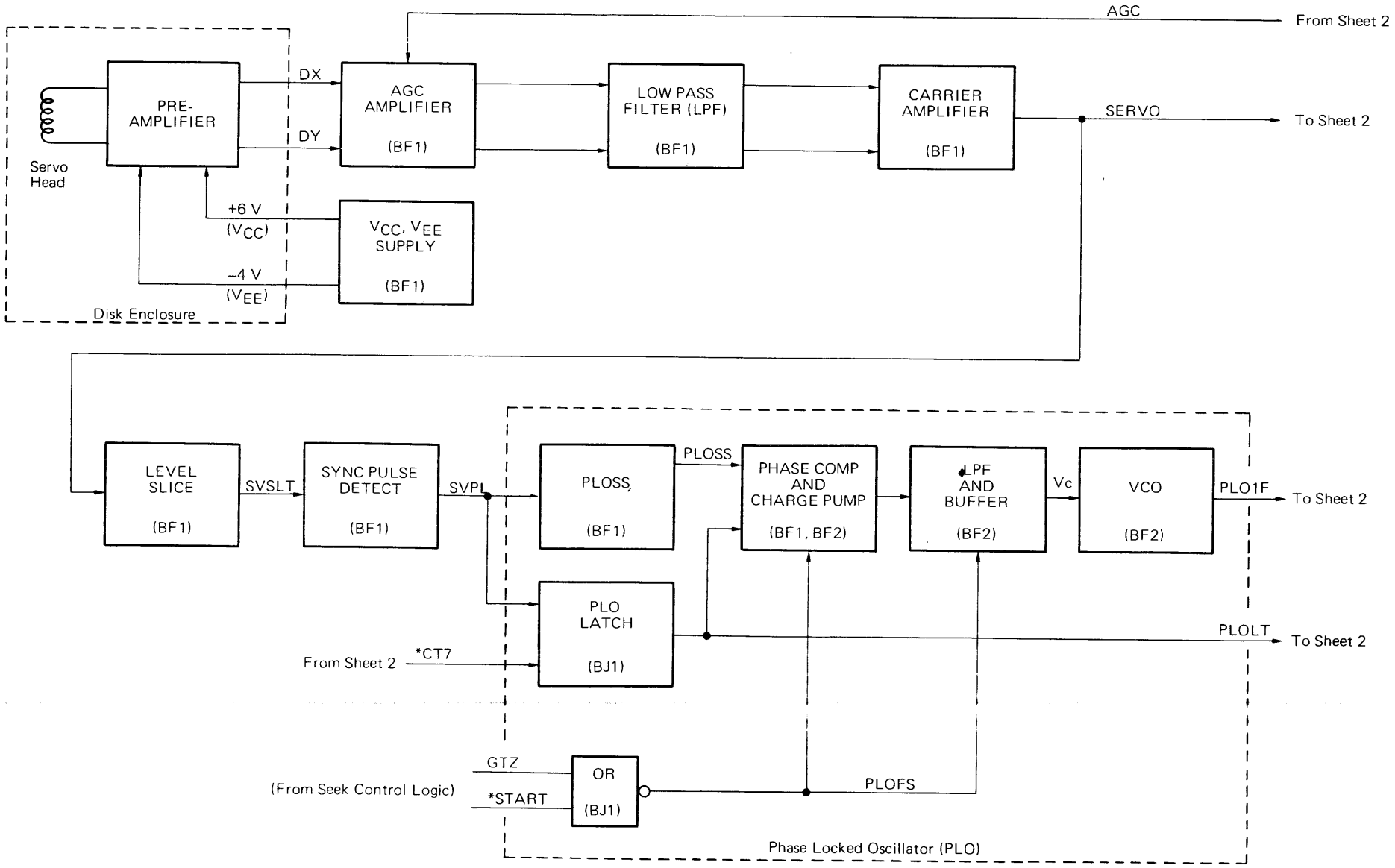


Figure 4-6-18 Position Sensing Block Diagram (Sheet 1 of 2)

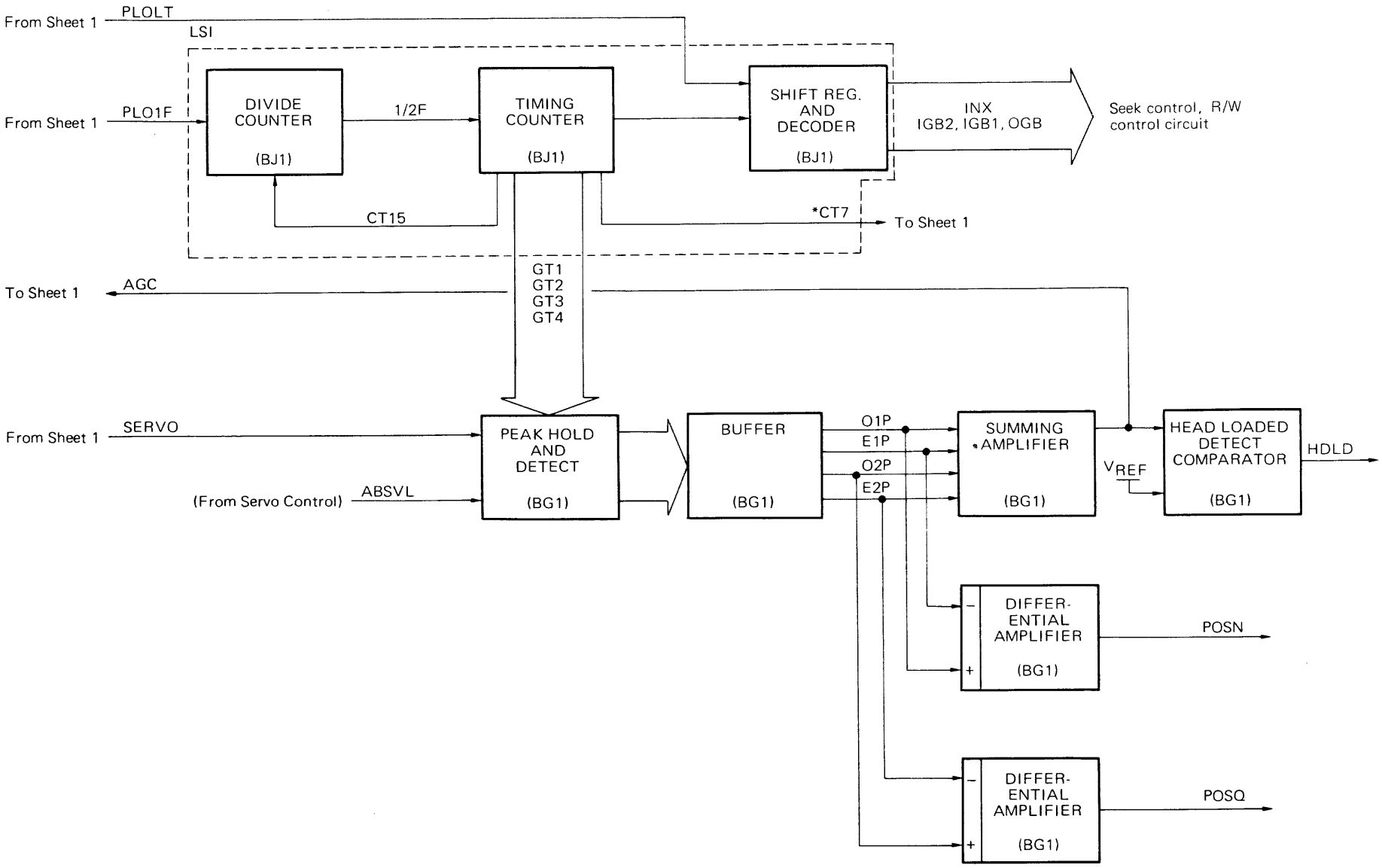


Figure 4-6-18 Position Sensing Block Diagram (Sheet 2 of 2)

The SERVO signal is converted into the Servo Slice Output (SVSLT) signal at a TTL level. The SVSLT signal triggers a 100 ns pulse at its trailing edge and the trailing edge of this 100 ns pulse triggers the 320-ns-long Servo Pulse Window (SVPWD) one-shot. The SVPWD signal separates only the Sync Pulse, that is, it separates the Servo Pulse (SVPLS) signal from the SVSLT signal. The SVPLS Signal is applied to the Phase Locked Oscillator (PLO).

The leading edge of the SVPLS Signal triggers PLOSS one shot (1.5 μs) and sets the PLO Latch circuit. The PLO Latch is reset by the leading edge of the Count 7 (CT7) signal, which is the output signal of the Timing Counter, and issues the PLO Latch (PLOLT) signal to the Phase Comparator circuit and the Index Guard Bands sense circuit.

The PLOSS and PLOLT signals are applied to the Phase Comparator circuit of PLO. The Phase Comparator issues an Increase (INC) signal when phase-lead has occurred on the VCO output, or a Decrease (DEC) signal when phase-lead has occurred on the VCO output. The INC and DEC signals are applied to the Charge Pump circuit which converts the phase difference into a DC-levle signal. The Charge Pump circuit issues a control voltage to the Voltage Controlled Oscillator (VCO) through the Low Pass Filter (LPF). Thus, the PLO circuit synchronizes with the SVPLS signal and generates a one bit cell clock, that is, the PLO1F signal. The PLO1F signal is applied to the VFO circuit and the Timing Counter circuit.

The Timing Counter circuit divides the PLO1F signal by two into 1/2F signal. The 1/2F signal generates the Gate 1, 2, 3, and 4 (GT1 to GT4) signals Count 15 (CT15) and the CT7 signal, which resets the PLOLT signal.

The Peak Hold circuit holds the peak of the signals (Odd 1, Even 1, Odd 2 and Even 2) enabled by the GT1 to GT4 timing signals. The Peak-hold outputs (Odd 1 peak, Even 1 peak, Odd 2 peak, and Even 2 peak) are applied to the Summing Amplifier and two Differential Amplifier circuits.

The Differential Amplifiers issue the Position Normal (POSN) signal from Odd 1 peak and Even 1 peak signals, and the Position Quadrature (POSQ) signal from Odd 2 peak and Even 2 peak signals. The Summing Amplifier issues the AGC Control Voltage (AGC) signal for the AGC amplifier. When the AGC signal exceeds the reference level, the Head Loaded (HDLD) signal is issued to the seek control circuit. The timing chart for PLO and Peak Hold is shown in Figure 4-6-19. The conversion waveform from Servo signal to dual-phase position signal is shown in Figure 4-6-20, which is valid when the servo head is moving.

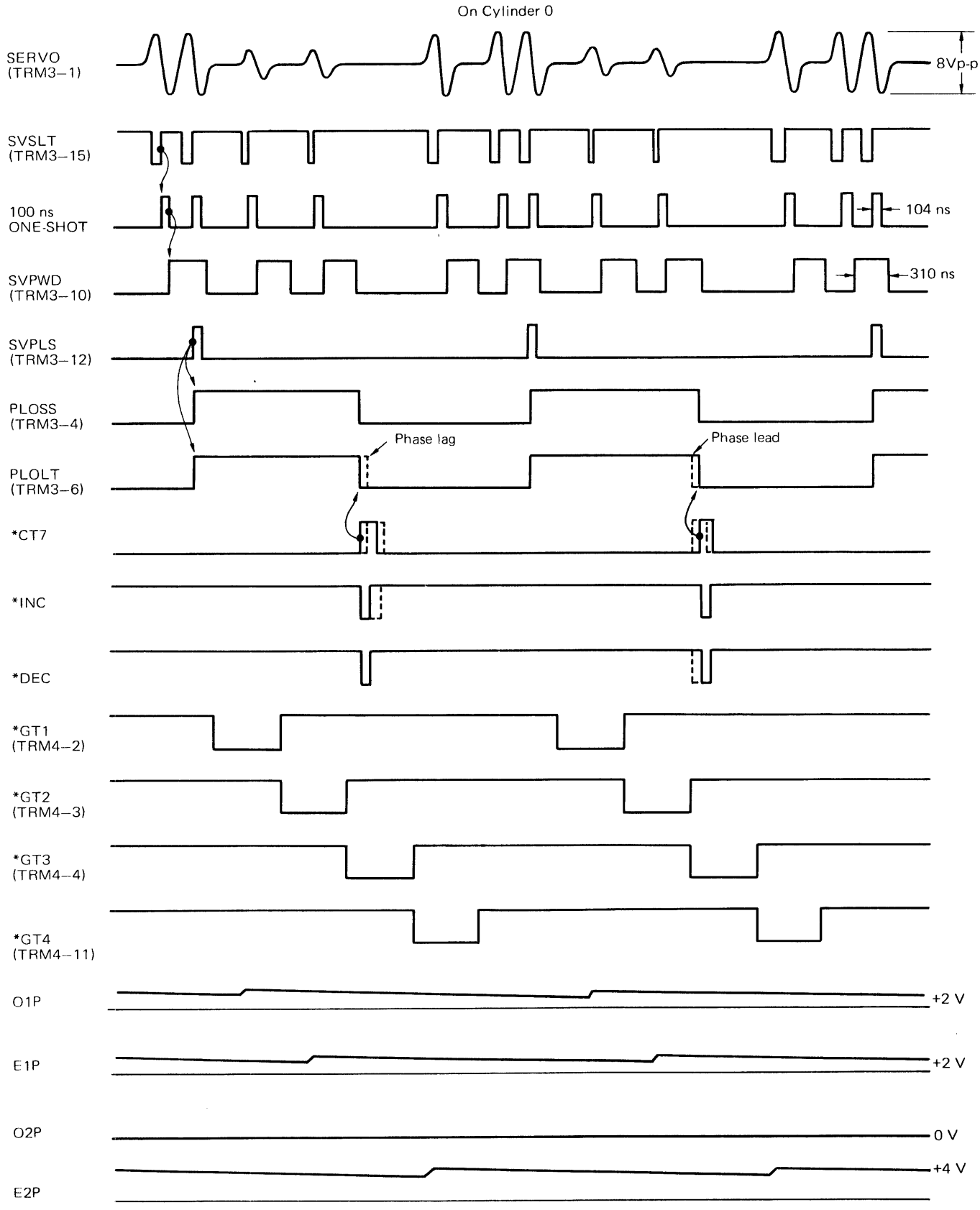


Figure 4-6-19 PLO and Peak Hold Timing Chart

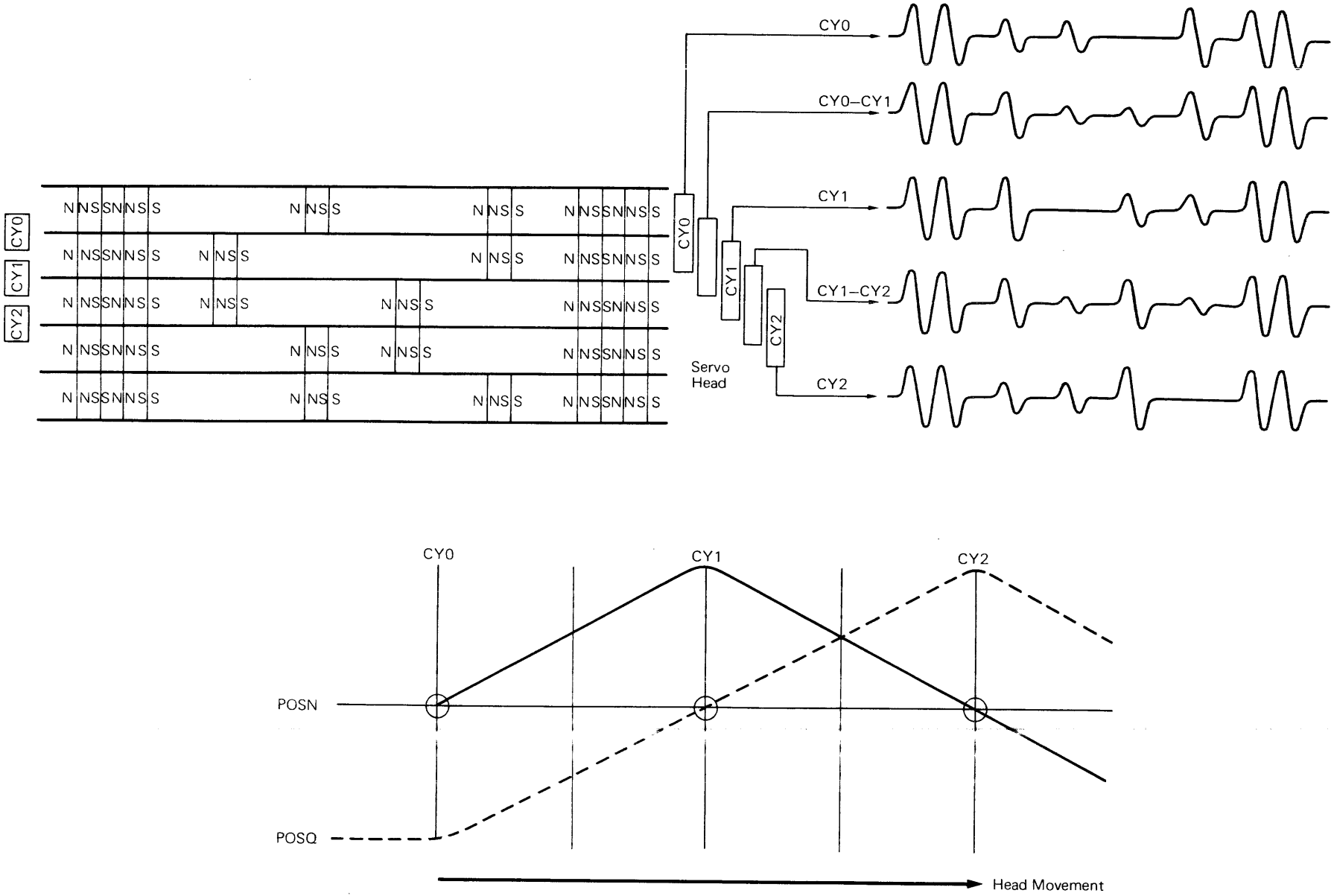


Figure 4-6-20 Servo Signal to Position Signal Conversion

4.6.5.2 Servo Control

The block diagram of the Servo Control circuit after Position Sensing is shown in Figure 4-6-21.

(1) Block Description

a) Position Signal Slice

The dual-phase position signals, POSN and POSQ which are demodulated through Position Sensing circuitry, are applied to a level slice circuit. The Position Signal Slice circuit then issues NGTQ and NQGTZ signals which are applied to Position Decoder, also issues an Off-track (OFTRK) signal which indicates that the servo head positions off from the center of each cylinder by ±9 μm.

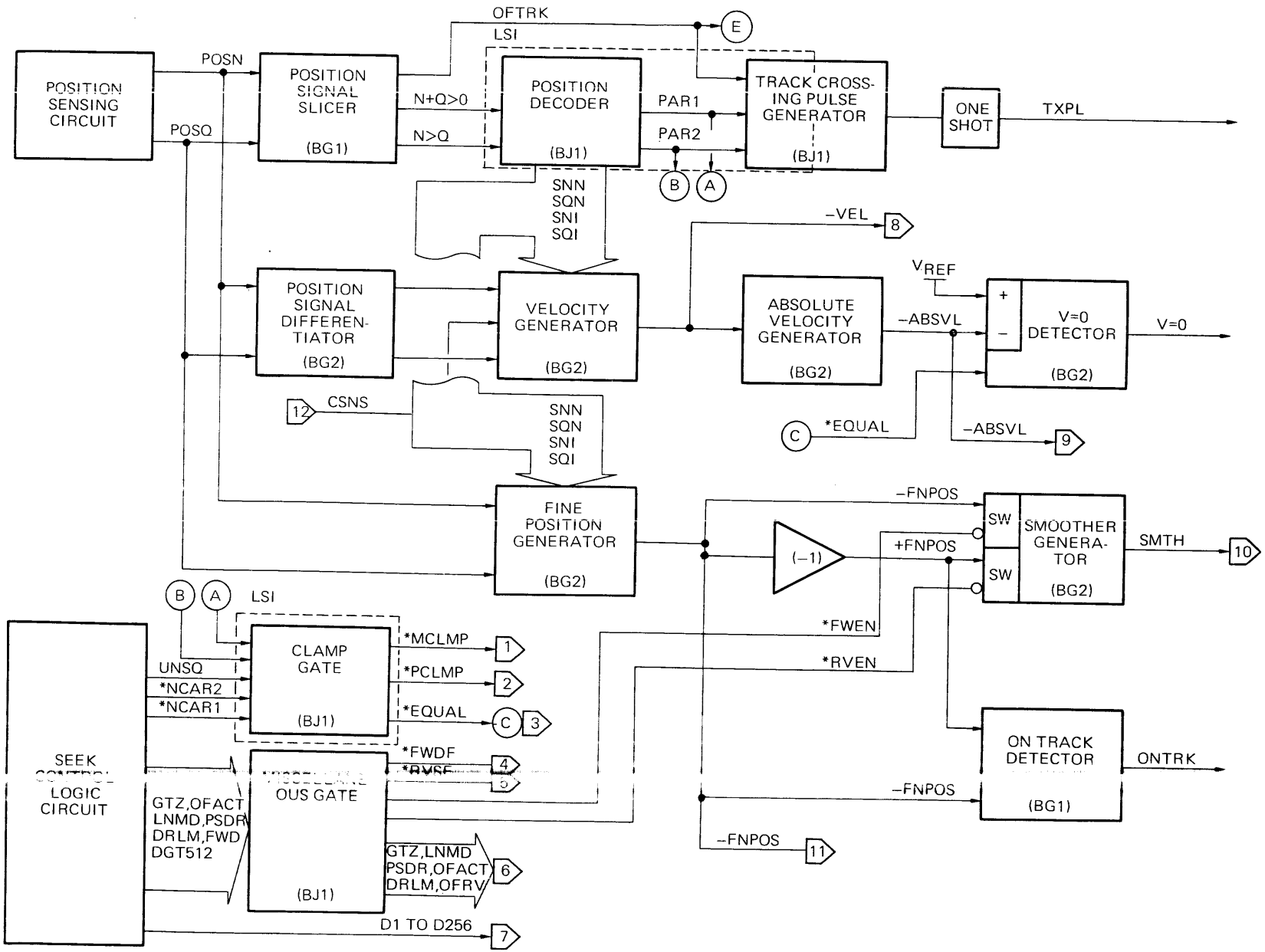


Figure 4-6-21 Servo Control Block Diagram (Sheet 1 of 2)

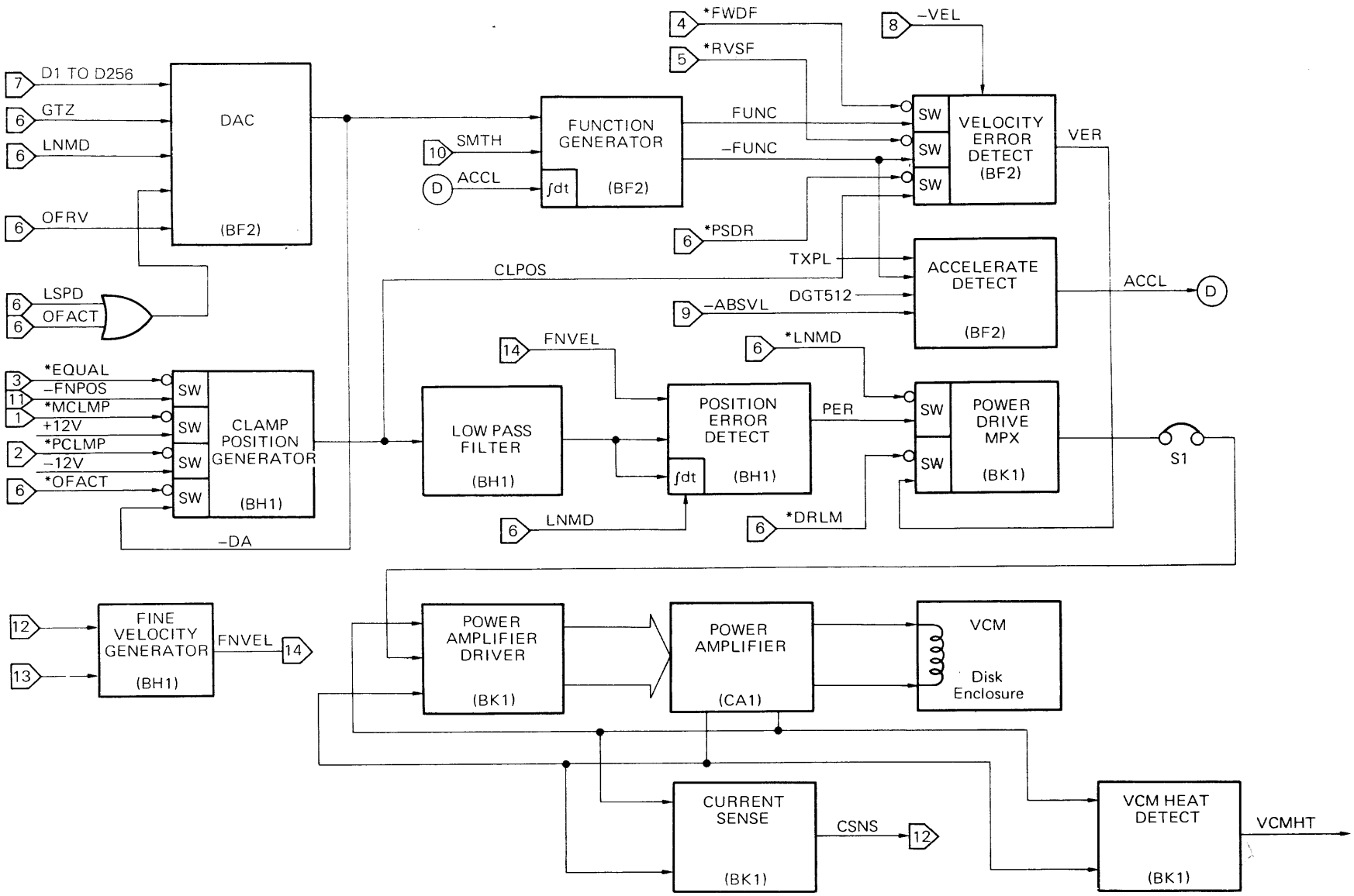


Figure 4-6-21 Servo Control Block Diagram (Sheet 2 of 2)

b) Position Decoder

The Position Decoder circuit issues the two least-significant bits of the current cylinder address, Present Address 2 and 1 (PAR2 and PAR1), which are decoded by the NGTQ and NQGTZ signals. The Position Decoder circuit also issues Select N Non-invert (SNN), Select Q Non-invert (SQN), Select N Invert (SNI), and Select Q Invert (SQI) signals, which control the Velocity Generator circuit and Fine Position Generator circuit.

c) Track Crossing Pulse Generator

The Track Crossing Pulse Generator circuit issues a 5-μs-wide Track Crossing Pulse (TXPLS), which is generated by PAR2, PAR1, and OFTRK signals, and which is applied to the Present Cylinder Address Register (PCAR). The PCAR counts up the TXPLS signal when Forward Drive (FWDD) signal is true, and counts down when FWDD signal is false.

The timing chart for items (a) through (c) is shown in Figure 4-6-22.

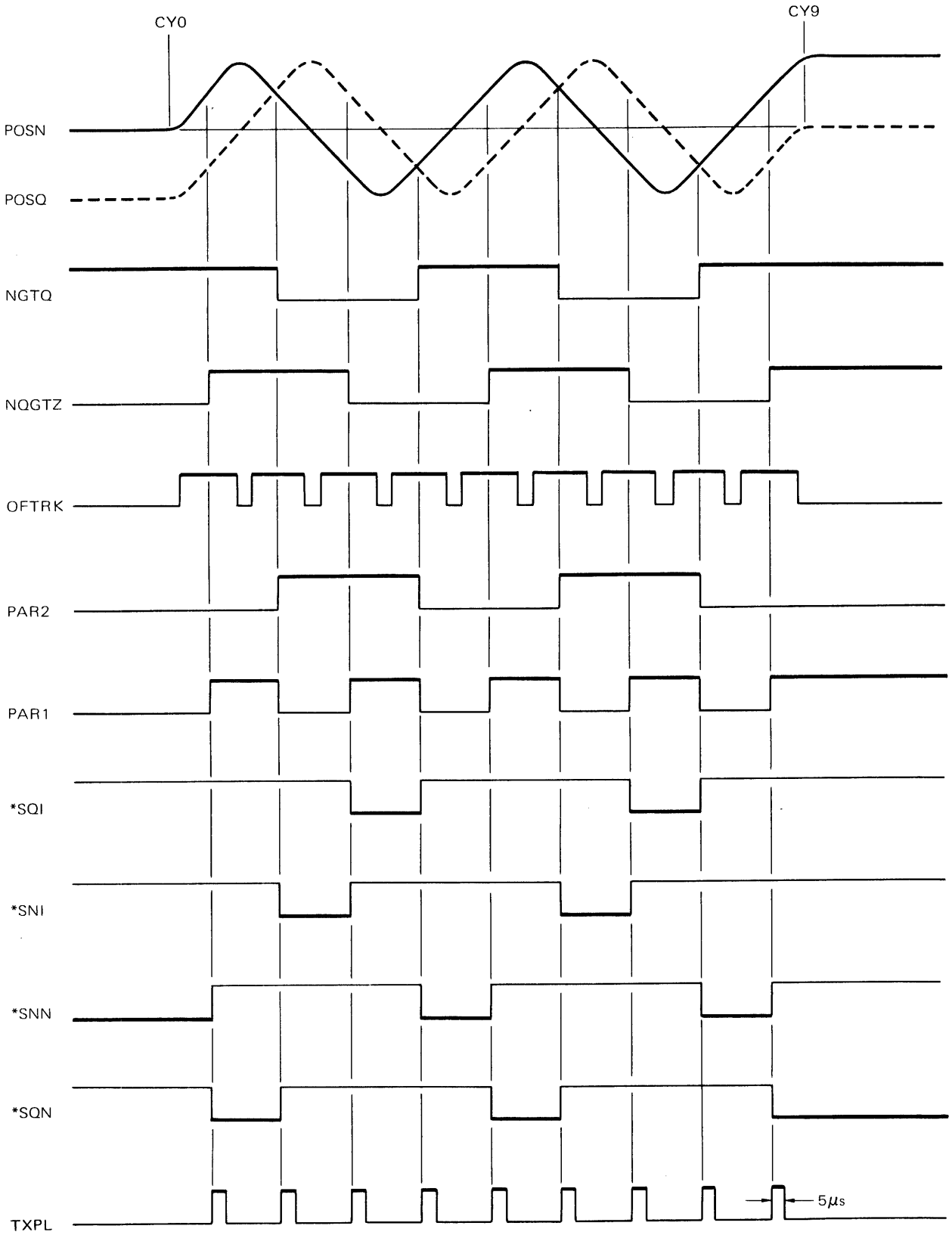


Figure 4-6-22 Position Detect Timing Chart

d) Position Signal Differentiator

The Position Signal Differentiator circuit differentiates the dual-phase position signals, POSN and POSQ, to generate the actual velocity from the linear portion of the position signal.

e) Velocity Generator

The SQI, SNI, SNN, and SQN signals, which are issued from the Position Decoder circuit, pull out the linear portion of the position signals; the composed signal and Current Sense (CSNS) signal are then converted into the Velocity (VEL) signal.

f) Absolute Velocity Generator

The Absolute Velocity Generator converts the velocity signal, with polarity, into the Absolute Velocity (ABSVL) signal.

g) V = 0 Detector

When the Equal signal on the Clamp Gate circuit goes true, and OFTRK signal goes false, and when the velocity is within 1 cm/second, the Velocity Equal to Zero (V = 0) signal is issued to the Seek Control circuit and then the Seek mode is changed to Linear mode by terminating Seek operation.

The timing chart of the Velocity Generator is shown in Figure 4-6-23.

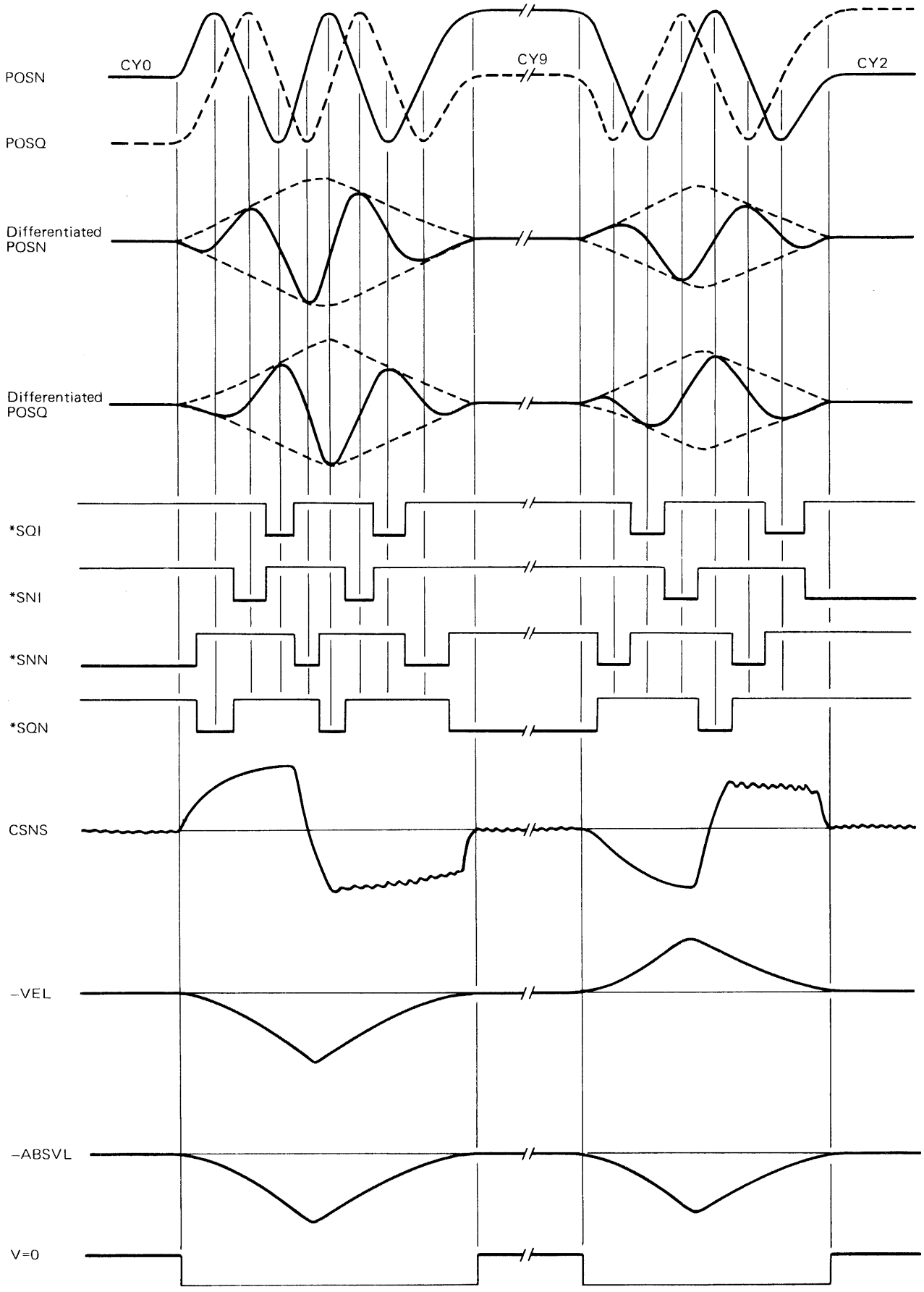


Figure 4-6-23 Velocity Generator Timing Chart

h) Fine Position Generator

The Fine Position Generator circuit pulls out the linear portion, that is, the Fine Position (FNPOS) signal from the POSN and POSQ signals controlled by SQI, SNI, SNN, and SQN signals. The FNPOS signal is applied to the Smoother, On Track Detector, and Clamp Position Detector circuits.

i) Smoother Generator

The Smoother Generator circuit polarizes the FNPOS (the polarity of signal which is in accord with the head movement direction) and issues the Smoother (SMTH) signal. The SMTH signal makes the DA signal smooth through the Function Generator circuit (see item (l), below). When the difference between NCAR and PCAR, however, is greater than 512 during Direct Seek mode, or GTZ mode is activated then the SMTH signal is deactivated.

j) On Track Detector

The On Track Detector senses the servo head positions on the center of each cylinder within $\pm 5\,\mu m$ and issues an On Track (ONTRK) signal to seek control and fault detect logics.

The timing chart of Fine Position Generator is shown in Figure 4-6-24.

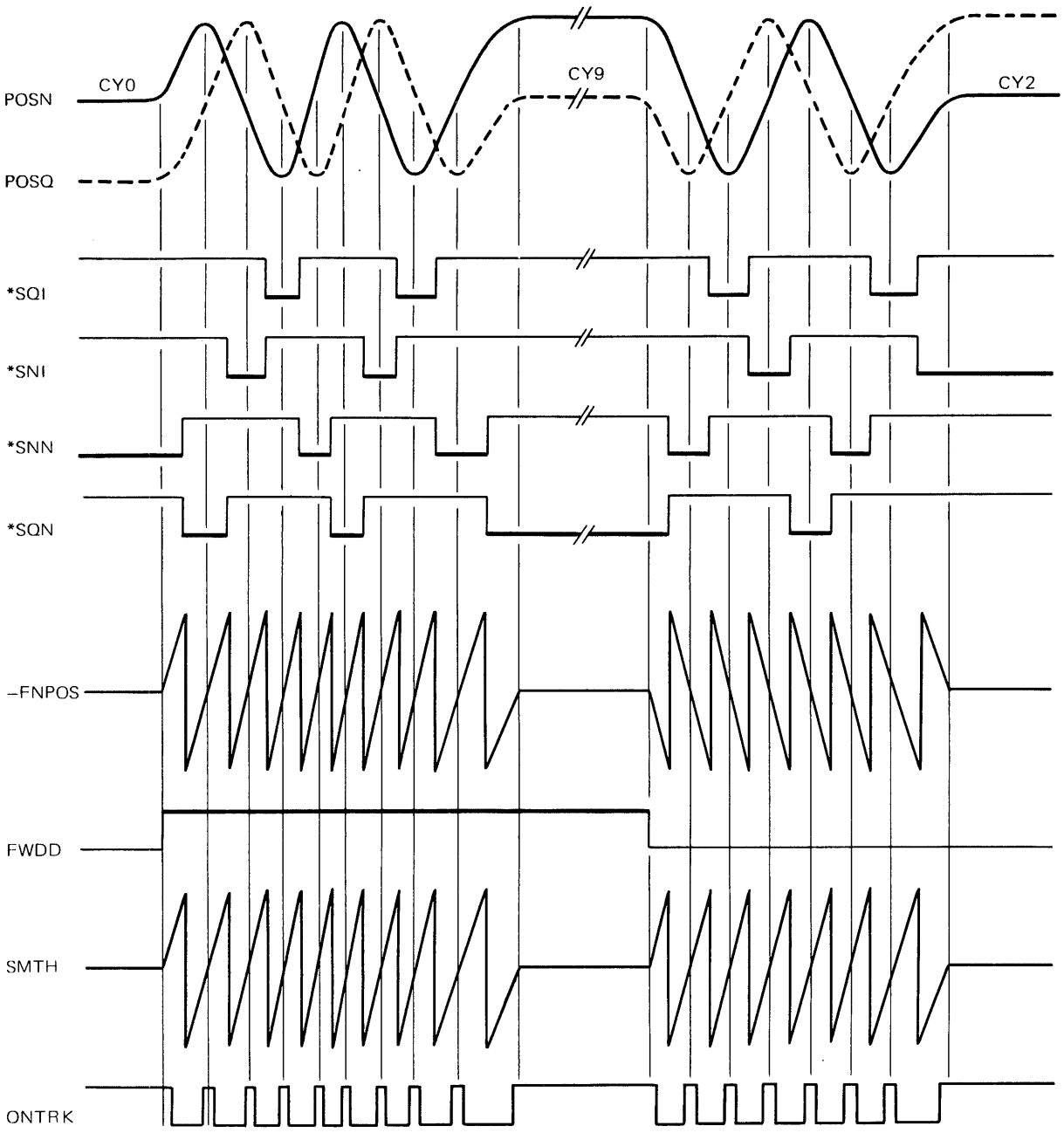


Figure 4-6-24 Fine Position Generator Timing Chart

k) DA Converter

The DA Converter DAC circuit generates the target velocity during Direct Seek or GTZ operations. When the Direct Seek operation is performed, the Difference Counter bits D1 to D256 are applied to the DAC at the beginning of the seek operation. When the servo head passes through a cylinder, the TXPLS signal is issued and it decreases the Difference Counter. When the Difference Counter output is equal to or greater than 512, the D1 to D256 signal is clamped to 511 and the DAC output is adjusted to be -7.3V.

When the GTZ operation is performed, GTZ and LSPD signals set a target velocity through the DAC.

When the Offset operation is performed, OFACT and OFRVS signals set the offset voltage to a value equivalent to ±3 μm from the center of cylinder. The DAC output, -DA signal, is applied to the Function Generator and Clamp Position circuits.

l) Function Generator

When the Difference Counter output is less than 511 the Function Generator circuit converts the DAC output into a smooth waveform by adding the SMTH signal. The Function Generator issues a Function (FUNC) signal which is the optimum deceleration curve for positioning time and the deceleration current profile.

When the servo control is changed to deceleration from acceleration, the Function Generator adds the integrated ACCL signal to the FUNC signal to avoid an excessive force to the actuator.

m) Velocity Error Detector

The Velocity Error Detector circuit issues the Velocity Error (VER) signal, which is applied to the Power Amplifier, after comparing a target velocity (FUNC) signal and actual velocity (VEL) signal. At the termination of Seek operation, the Clamped Position (CLPOS) signal is applied to the Velocity Error Detector instead of the FUNC signal, which is activated by the PSDR signal.

n) Accelerate Detector

The Accelerate Detector output, that is, the Accelerate (ACCL) signal, is set when the TXPL signal is equal to the DGT512 signal. The ACCL signal is applied to the Function Generator circuit.

The timing chart of the Target Velocity Generator, for a Direct Seek operation, is shown in Figure 4-6-25, and the timing chart for a GTZ operation is shown in Figure 4-6-26.

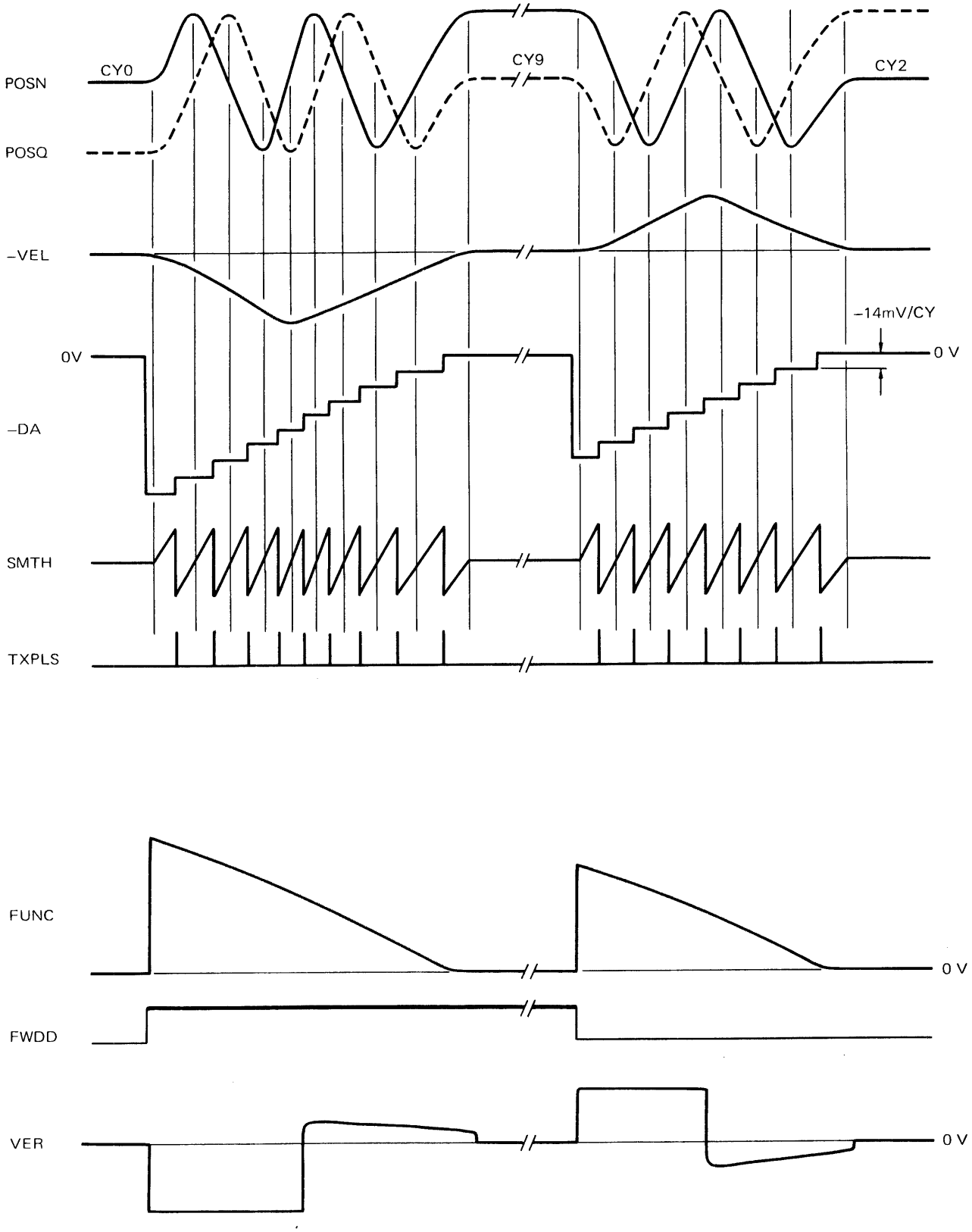


Figure 4-6-25 Direct Seek Target Velocity Generator

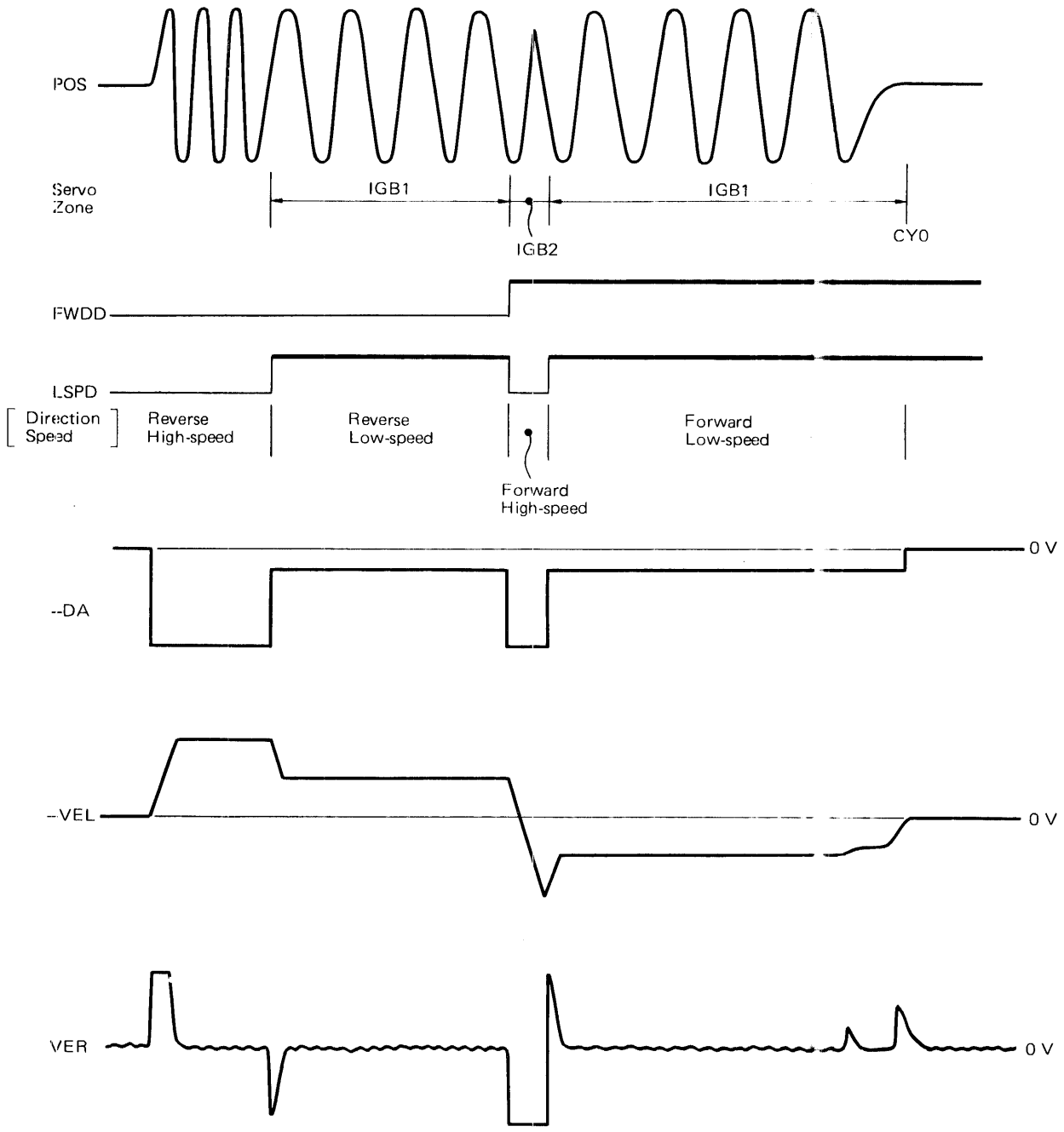


Figure 4-6-26 GTZ Target Velocity Generator

p) Clamp Gate

The Clamp Gate circuit issues Minus Clamp Position (MCLMP), Plus Clamp Position (PCLMP) and Equal (EQUAL) signals through the adder circuit, which compares the two least-significant bits (NCAR2 and 1) of the target cylinder (NCAR2 and NCAR1) with PAR2 and PAR1 signals from the Position Decoder circuit.

q) Clamp Position Generator

The Clamp Position Generator holds the position signal at specified levels when the servo head is positioned within three cylinders of the target cylinder address specified by the two least-significant bits of NCAR and PAR. This extends the area controlled by the servo circuit.

The PCLMP signal sets the Calmped Position Signal (CLPOS) to +2 V, the MCLMP is set to −2 V, and the EQUAL signal enables the FNPOS signal on the CLPOS signal.

The CLPOS signal is applied to the Velocity Error Detector circuit when the PSDR signal goes true at the termination of Seek operation, and is then applied to Low Pass Filter (LPF) when the servo head settles on the specified cylinder.

The timing chart of Clamp Position is shown in Figure 4-6-27.

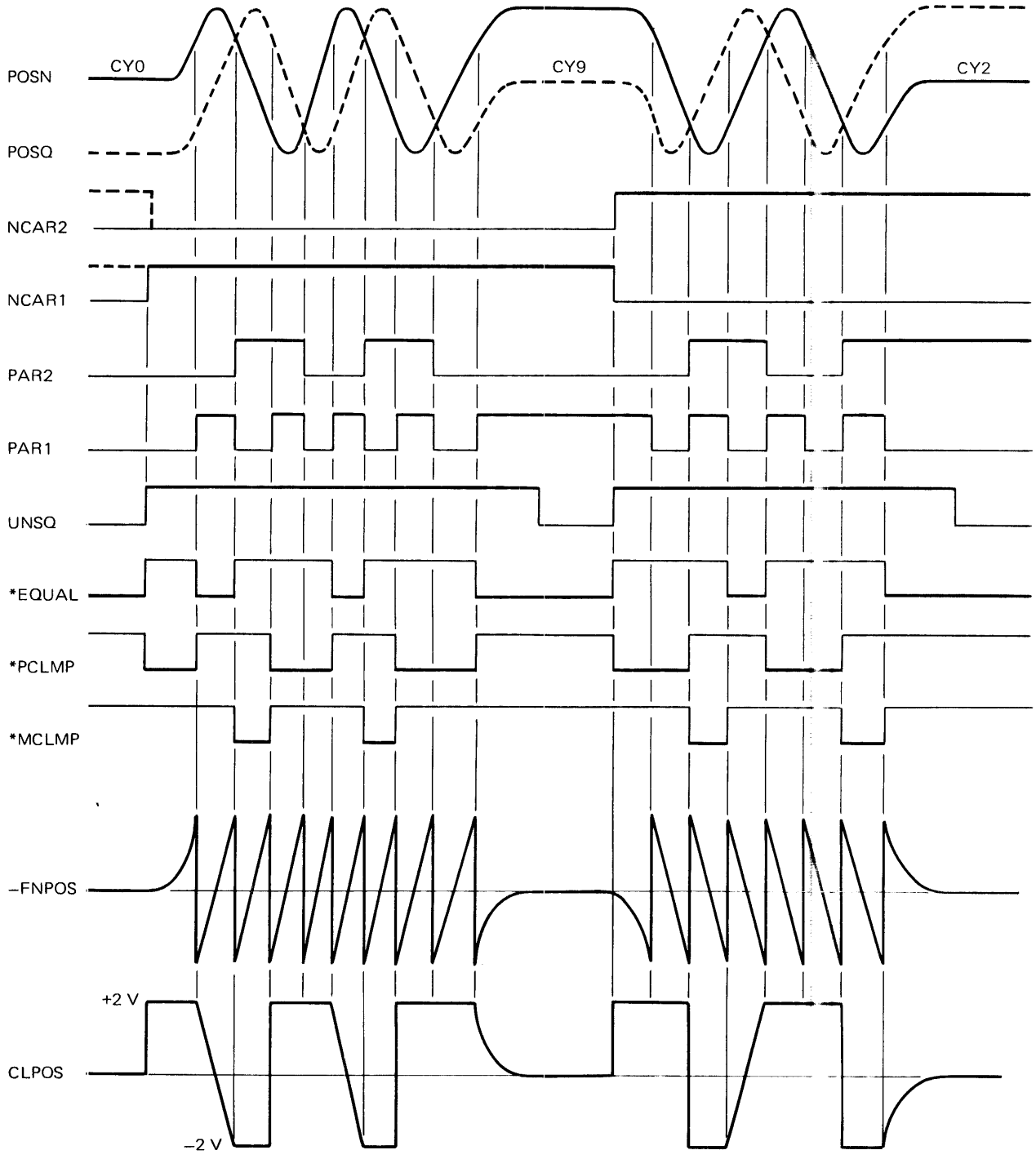


Figure 4-6-27 Clamp Position Timing Chart

r) Low Pass Filter (LPF)
The servo circuits form a feed-back loop during track following after a Seek operation using the position signal recovered from the servo head.

The LPF circuit attenuates unused high frequencies.

s) Position Error Detector
The Position Error Detector pulls out the phase-compensated Position Error (PER) signal required for the feed-back loop during track following.

The PER signal is composed of FNVEL (phase-compensating) signal, and an integrated position signal; improves stiffness and track following characteristics of lower frequencies.

t) Power Drive Multiplexer
The Power Drive Multiplexer circuit passes through either the VER signal, by activating DRLM signal during Direct seek or GTZ operation, or the PER signal, by activating the LNMD signal during track following sequence.

u) Power Amplifier Driver
The Power Amplifier Driver circuit drives the last stage of the power amplifier. This circuit controls the base current to the power transistors by comparing the input signal with the feed-back signal from the last-stage transistor current.

v) Power Amplifier
The Power Amplifier circuit is a current amplifier which drives the coil of the Voice Coil Motor (VCM). Four transistors compose H-type circuit.

w) Current Sense
The Current Sense circuit detects the VCM coil current through the voltage bleeder resistors. The coil current is amplified by the differential mode, and then the Current Sense (CSNS) signal is issued.

x) VCM Heat Detect
The VCM Heat Detect circuit senses an abnormal current flowing through the VCM coil or DC Motor windings.

The coil current of the DC Motor windings current is integrated and converted into the VCM Heat Detect (VCMHT) signal.

(2) Direct Seek Servo Control
During a Direct Seek with servo control, the servo head is driven high speed, so that the actual velocity pulled out from the position signal through the servo head is equal to the target velocity controlled by the Difference Counter. Whenever the servo head has passed through each cylinder, the target velocity is decreased for optimum speed control. The Direct Seek signal flow is shown in Figure 4-6-28.

(3) GTZ Servo Control
Wherever the head is positioned, GTZ Servo Control returns the head to Cylinder 0. The target velocity is given by the specified velocity, that is, high speed is 7 cm/second and low speed is 2 cm/second.

The GTZ signal flow is shown in Figure 4-6-29.

(4) Linear Mode Servo Control
When the servo head is positioned within capture distance from the specified cylinder, the Servo Control mode is changed to Linear mode. During Linear mode (track following), the feed-back loop is formed to minimize the Position Error Signal.

When an Offset operation is performed, the offset voltage is applied to the Position Error signal through the DAC.
The Linear mode signal flow is shown in Figure 4-6-30.

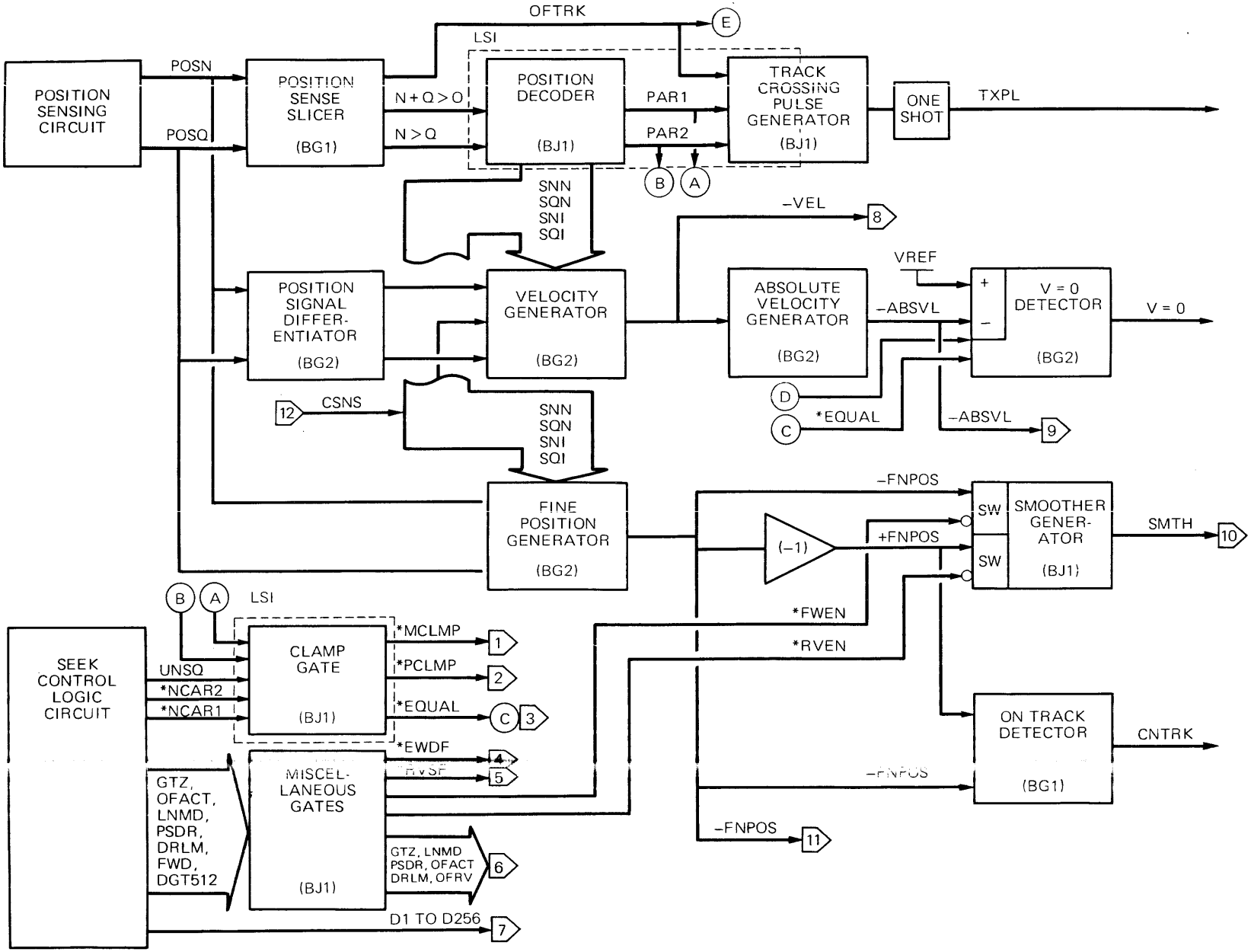


Figure 4-6-28 Direct Seek Signal Flow (Sheet 1 of 2)

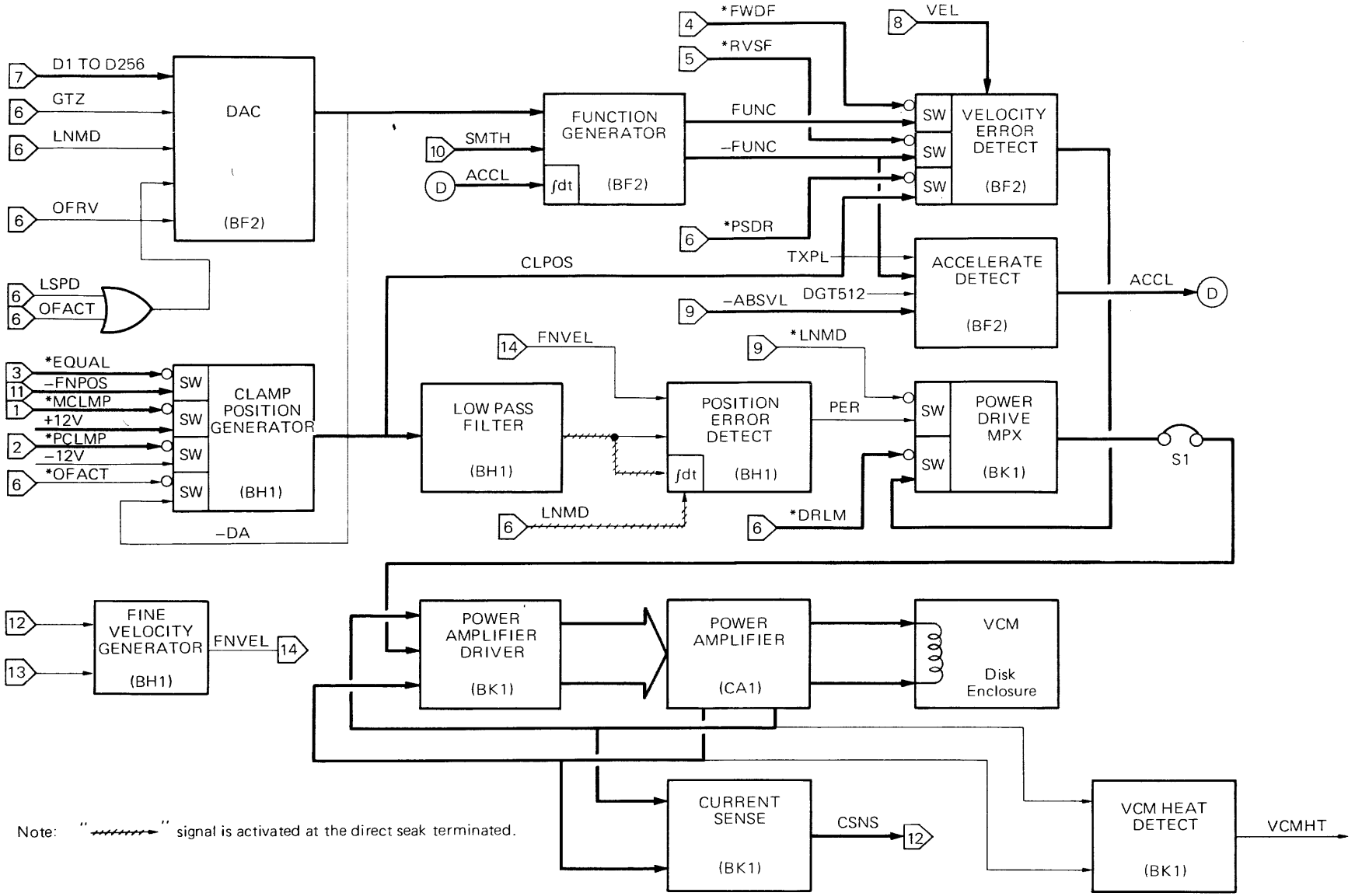


Figure 4-6-28 Direct Seek Signal Flow (Sheet 2 of 2)

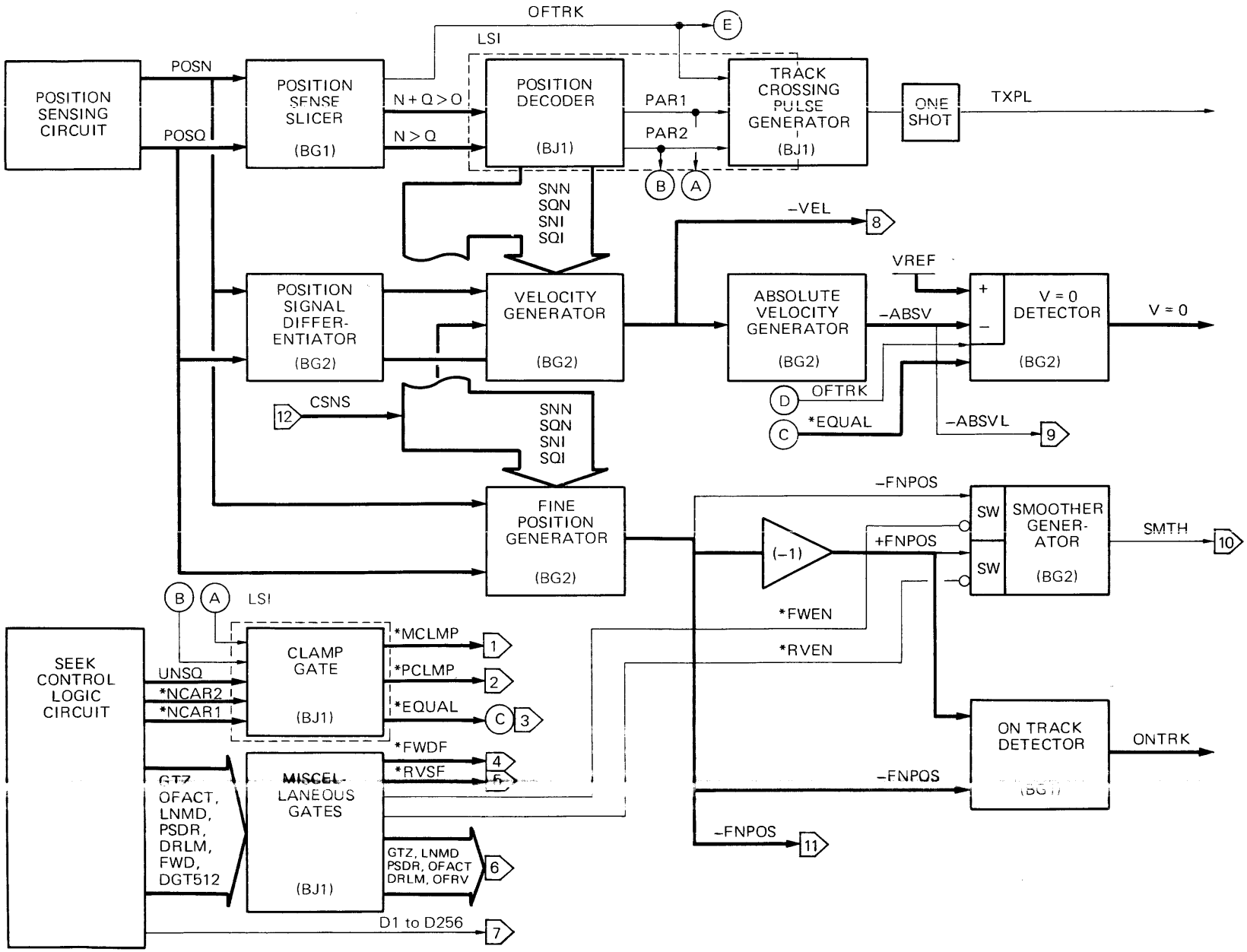


Figure 4-6-29 GTZ Signal Flow (Sheet 1 of 2)

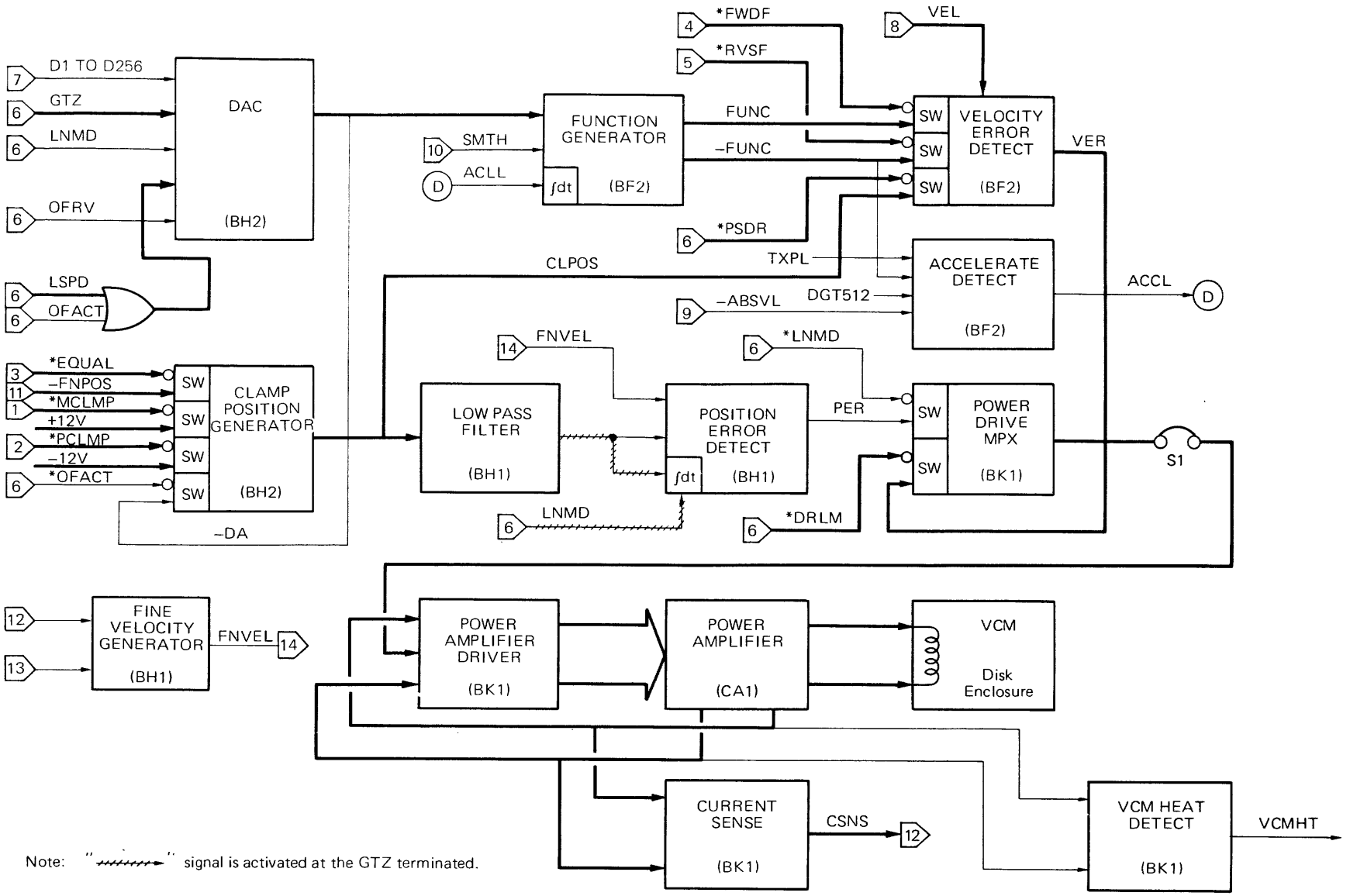


Figure 4-6-29 GTZ Signal Flow (Sheet 2 of 2)

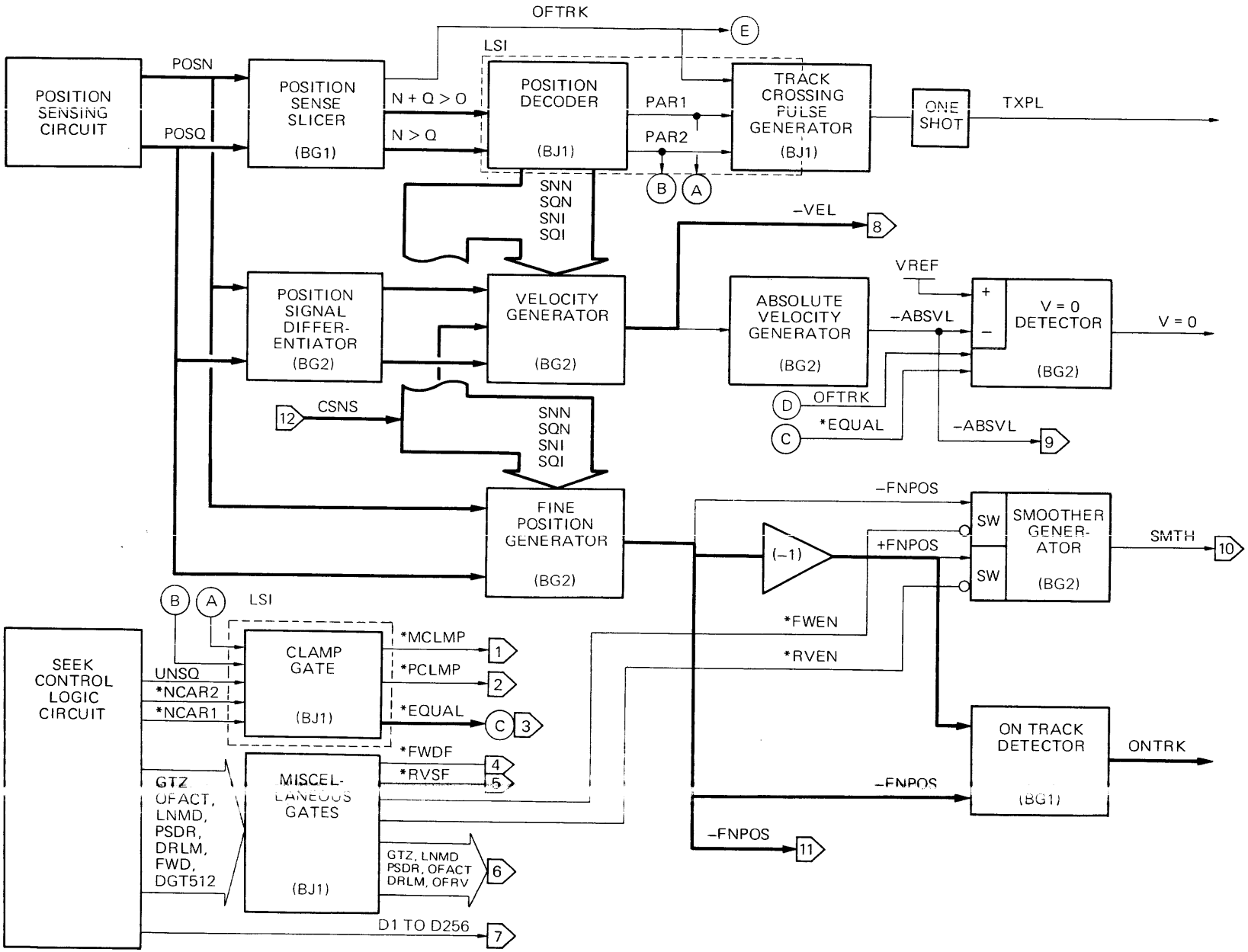


Figure 4-6-30 Linear Mode Signal Flow (Sheet 1 of 2)

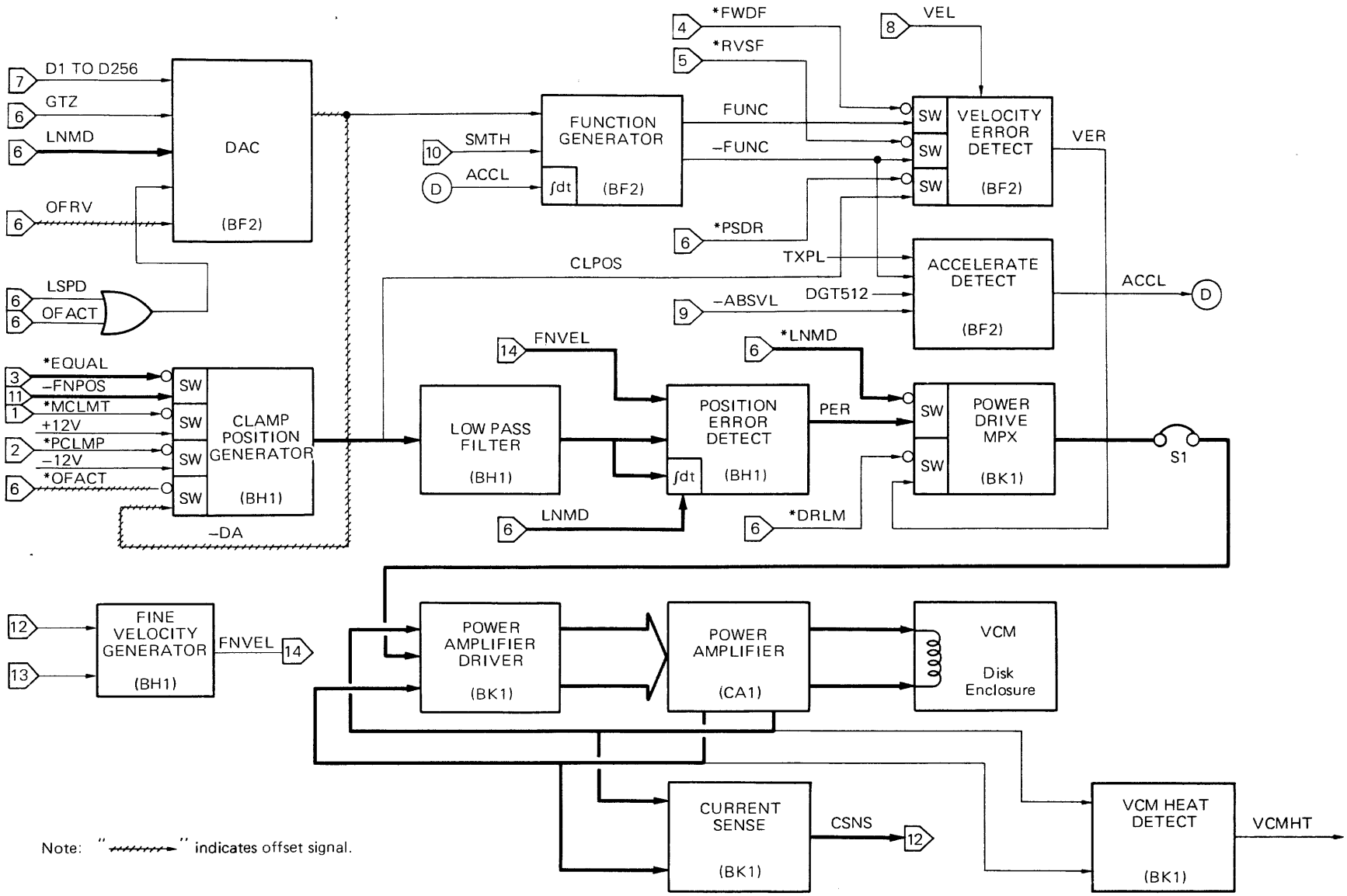


Figure 4-6-30 Linear Mode Signal Flow (Sheet 2 of 2)

4.6.6 Index/Sector/Guard Band Generate Function

4.6.6.1 Index Detect

As described in the position sensing discussion, the servo signal contains missing Index Bits. The servo pulse (SVPL) is applied to the PLO which outputs a one-bit cell clock (PLO1F).

The PLO latch (PLOLT) signal is set by the leading edge of the SVPL signal and reset by the leading edge of Count 7 (CT7). It is applied to a shift register in the LSI (MB15238) and clocked by the positive-going edge of the CT7 signal.

The shift register outputs are decoded, and then the Index (INX) signal, two Inner Guard Band pulse (IGB2P and IGB1P) signals, and the Outer Guard Band pulse (OGBP) signals are detected by the combination of the decoder outputs. The block diagram of Index and Guard Band pattern detect is shown in Figure 4-6-31. The timing chart of the Index signal processing is shown in Figure 4-6-32.

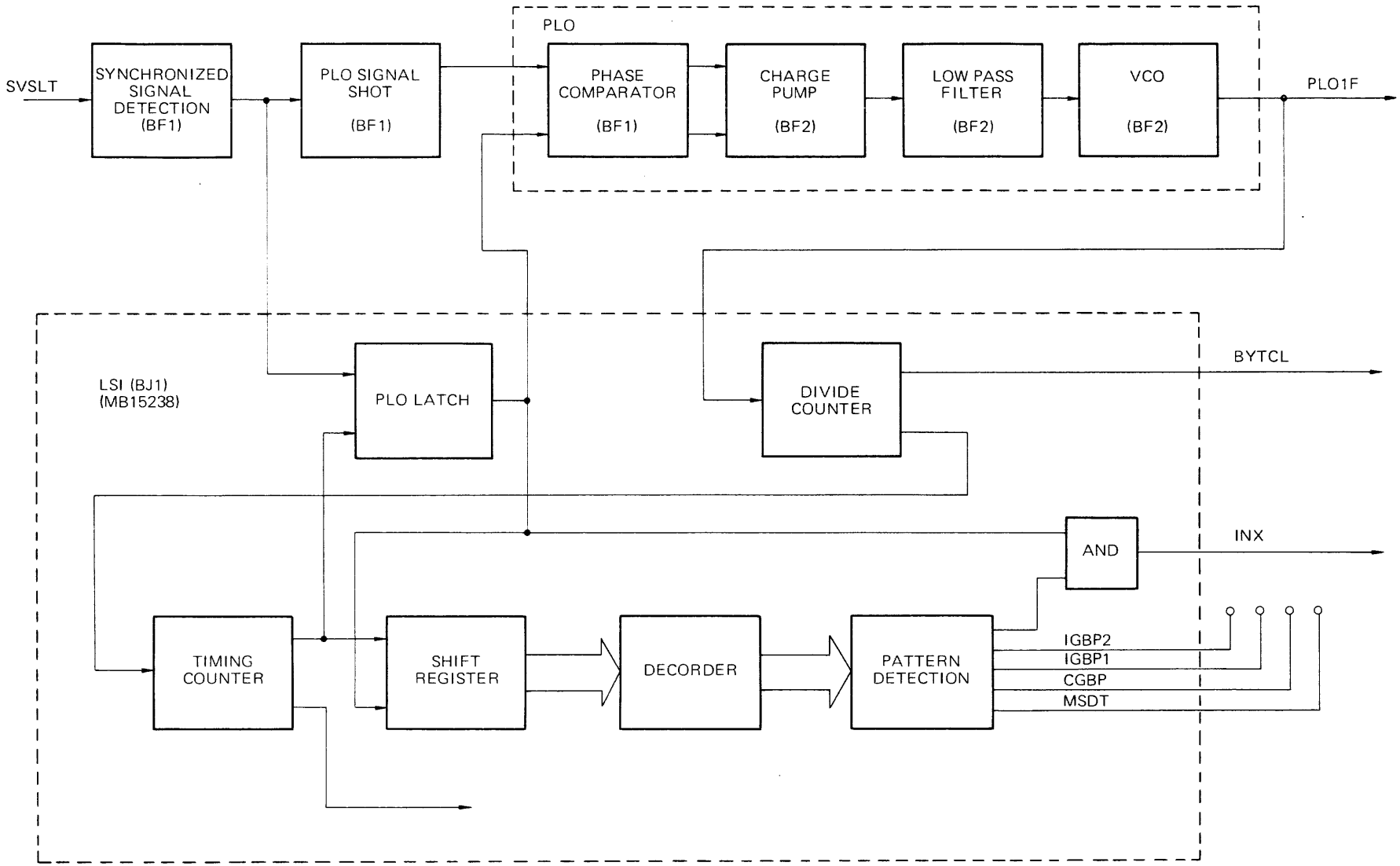


Figure 4-6-31 Index/Guard Band Patterns Detect Block Diagram

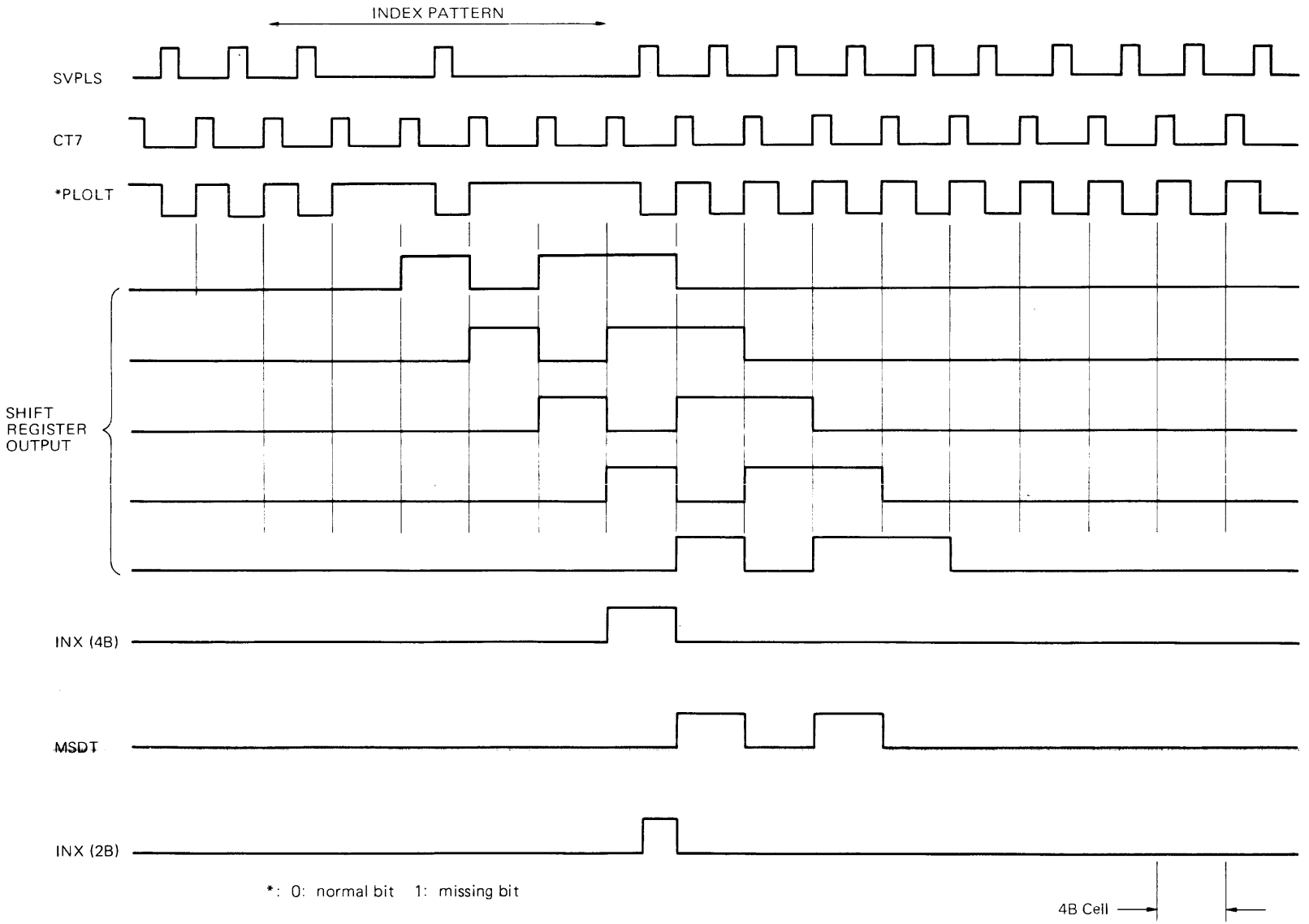


Figure 4-6-32 Index Detect Timing Chart

4.6.6.2 Guard Band Detect

As described in Section 4.3.3, each guard band has a missing Index bit. When the servo head is located on any guard band track, the servo PLO circuit develops IGB2P, IGB1P, or OGBP and missing detect (MSDT) signals as shown in Figure 4-6-33.

The first pulse of the Guard Band Pulse sets the first flip-flop, and simultaneously the MSDT signal loads 187 (decimal) on the Guard Band Reset counter clocked by the four-byte interval Count 15 (CT15) signal. When the second pulse is applied before the Guard Reset Counter issue the Reset Guard Band (RSTGB) signal, the second pulse sets the second flip-flop; Guard Band signal (IGB2, IGB1 or OGB) is then issued to the seek control logic.

The output of each Guard Band latch is reset by a RSTGB signal, when the servo head is not located over a guard band track and the Guard Band Reset counter counts up to 255 (decimal).

The two stages of the flip-flop prevent the Guard Band signal from improper detection of the Guard Band signals caused by media flaws.

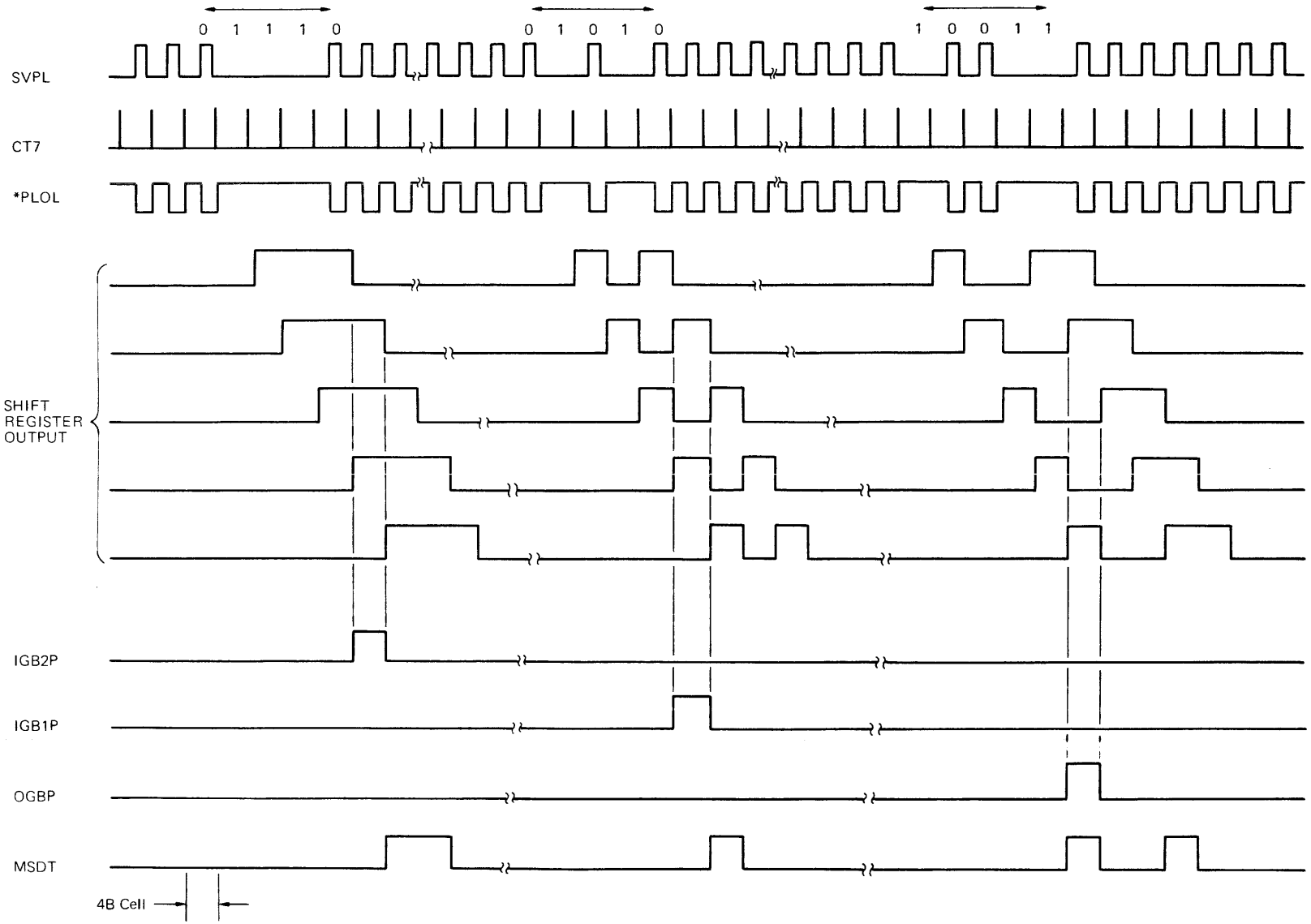


Figure 4-6-33 Guard Band Pulse Detect Timing Chart

4.6.6.3 Sector Generator

A Sector pulse is not written on the servo surface. The sector pulses are derived from a Byte counter counting Byte clocks, which are generated by the PLO circuit synchronized with servo pulse. One disk revolution has 20,480 Byte clocks, and the sector length is determined by selectable keys on the CZFM PCB.

The Index signal (Two Bytes) from the PLO circuit enables the preset input to the Byte Counter. An example of 256-byte sector length is described as follows; The value loaded into the Byte Counter is specified by turning on SW2 keys one to seven and SW3 key one. The binary value of the keys not turned on (SW3 keys two to seven) equals 65,280. The Index signal causes the Byte counter to be preset to 65,280. The Counter is then clocked by the positive going edge of the Byte Clock (BYTCL) signal until it reaches 65,535 (255 byte clocks). Then a carry signal which is used as a new preset enable to the Byte Counter is issued. The carry signal is applied to next flip-flop and then converted into 12-bit pulse of the Sector signal. The block diagram is shown in Figure 4-6-34, and the timing chart is shown in Figure 4-6-35.

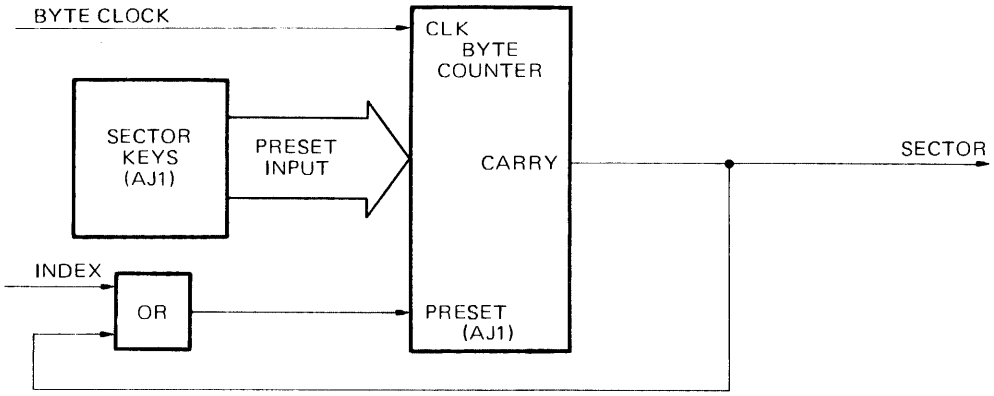


Figure 4-6-34 Sector Generator Block Diagram

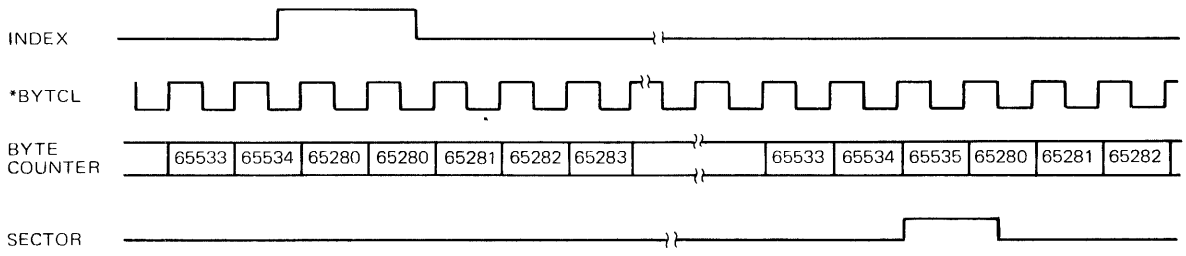


Figure 4-6-35 Sector Generator Timing Chart

4.6.7 Head Selection

A head must be selected before a read or write operation can be performed. (However, head switching during format write is available.) The head address is set by positive-going edge of Tag 2 signal with Bus bit 0 to 3 at Head Address Register (HAR). The HAR outputs, HAR1, 2, 4 and 8 signals, are applied to the Driver circuit on the CZGM PCB.

HA1 and HA2 signals are converted from TTL level to ECL level, and applied to head ICs (HIC). Then HIC selects one read/write pre-amplifier and one head in the decode circuit. At this time, Chip Select (CS) signal corresponding to that HIC must be ON.

HA4 and HA8 signals are converted from TTL level to +6V/0V (0V:ON) level in the CZGM PCB. CS0, CS1 and CS2 signals enable HD0 to HD3, H4 to H6 and H7 to H9 signals respectively, and these signal are applied to each HIC.

The DC regulators in the CZGM PCB supply +6V DC (V_{cc}) and −4V DC (V_{EE}) to the head ICs within the Disk Enclosure. When the power supply becomes abnormal condition (PWRDY signal becomes OFF), V_{EE} supply stops immediately. The multiple-chip select or head-short condition is detected by an overload current of V_{cc} supply.

The block diagram of head selection is shown in Figure 4-6 36.

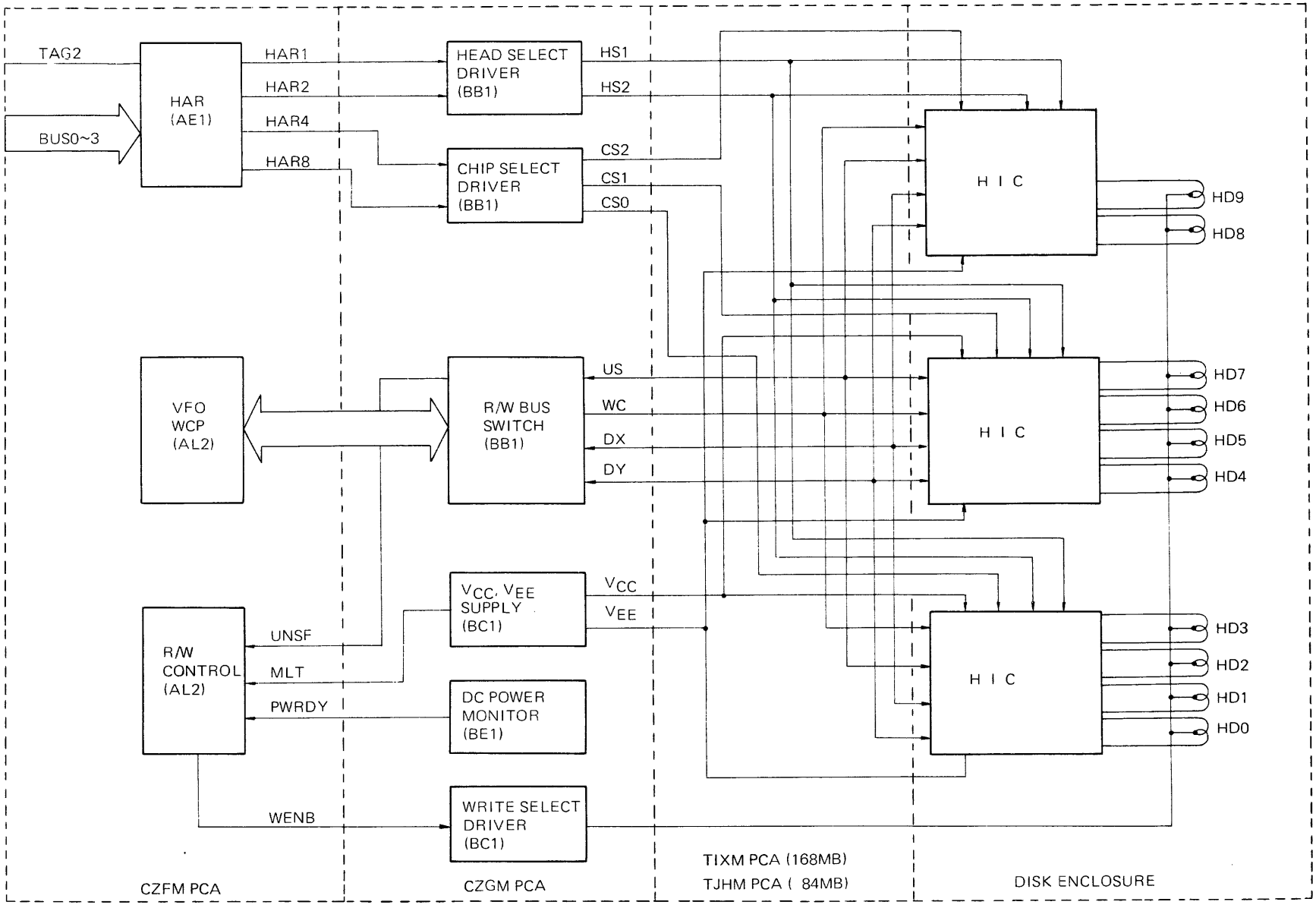


Figure 4-6-36 Head Selection Block Diagram

4.6.8 Read/Write Function

4.6.8.1 Read/Write Basic Principles

When the disk is rotating at a nominal 3,600 rpm, a read or write may be performed. The basic principles of the read/write function are as follows:

(1) Data Write

During a write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is revered. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

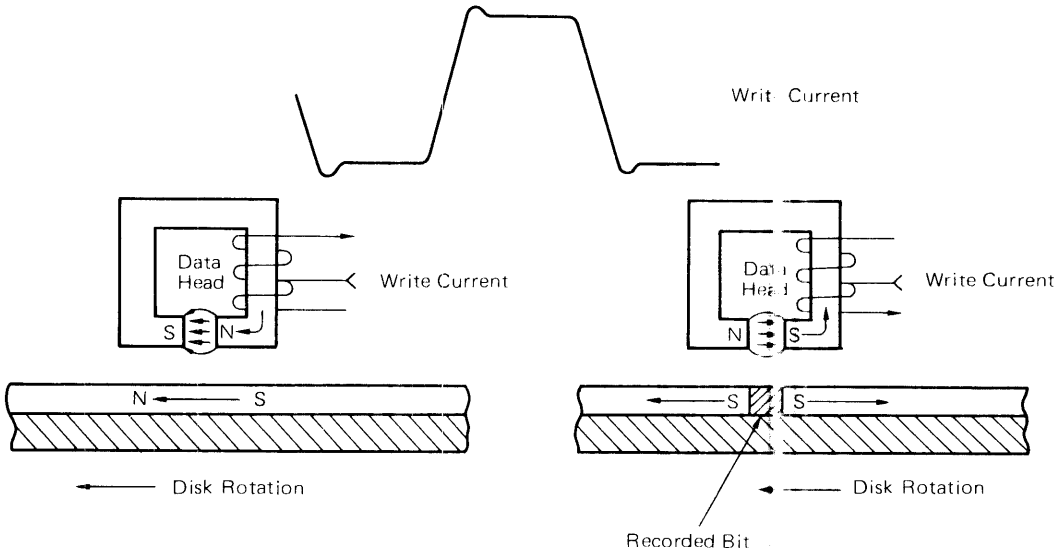


Figure 4-6-37 Data Write

(2) Data Read

During a read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180-degree flux reversal in the horizontal direction) passes under the head gap, the magnetic flux flowing in the ring and coil is reversed and an output pulse is obtained.

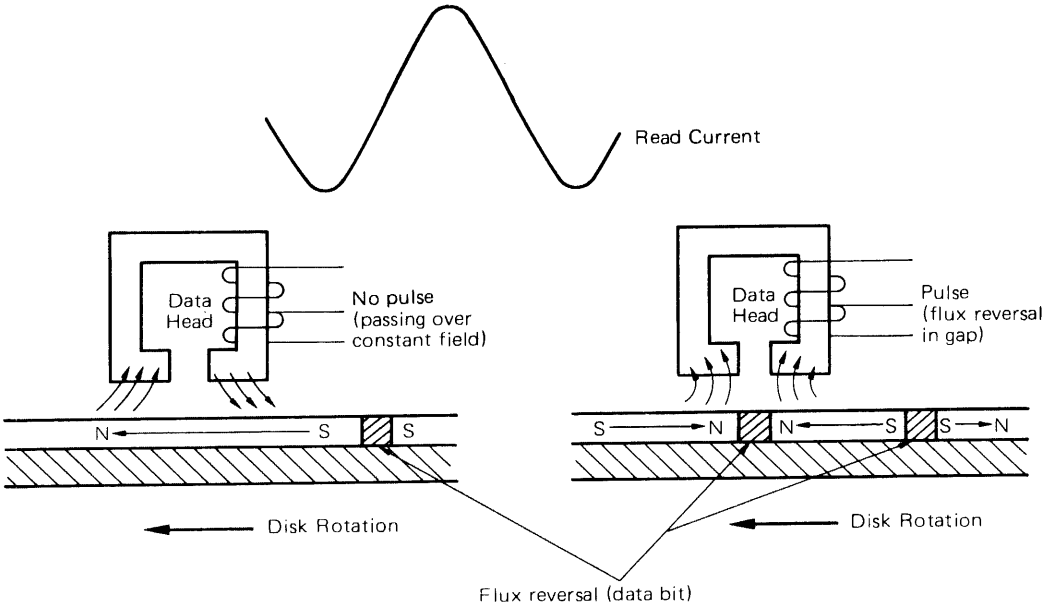


Figure 4-6-38 Data Read

(3) Principles of MFM Recording

This unit uses the modified frequency modulation (MFM) recording technique. The length of time required to define one bit of information is the cell. Each cell is nominally 102 ns in width.

MFM defines a "1" by writing a pulse at the half-cell time. A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is clock. However, clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell. See Figure 4-6-39.

The rule for MFM recording is summarized:

(A) There is a flux transition for each "1" bit at the time of the "1".
(B) There is a flux transition between each pair of "0" bits.
(C) There is no flux transition between the bits of a "10" or "01" combination.

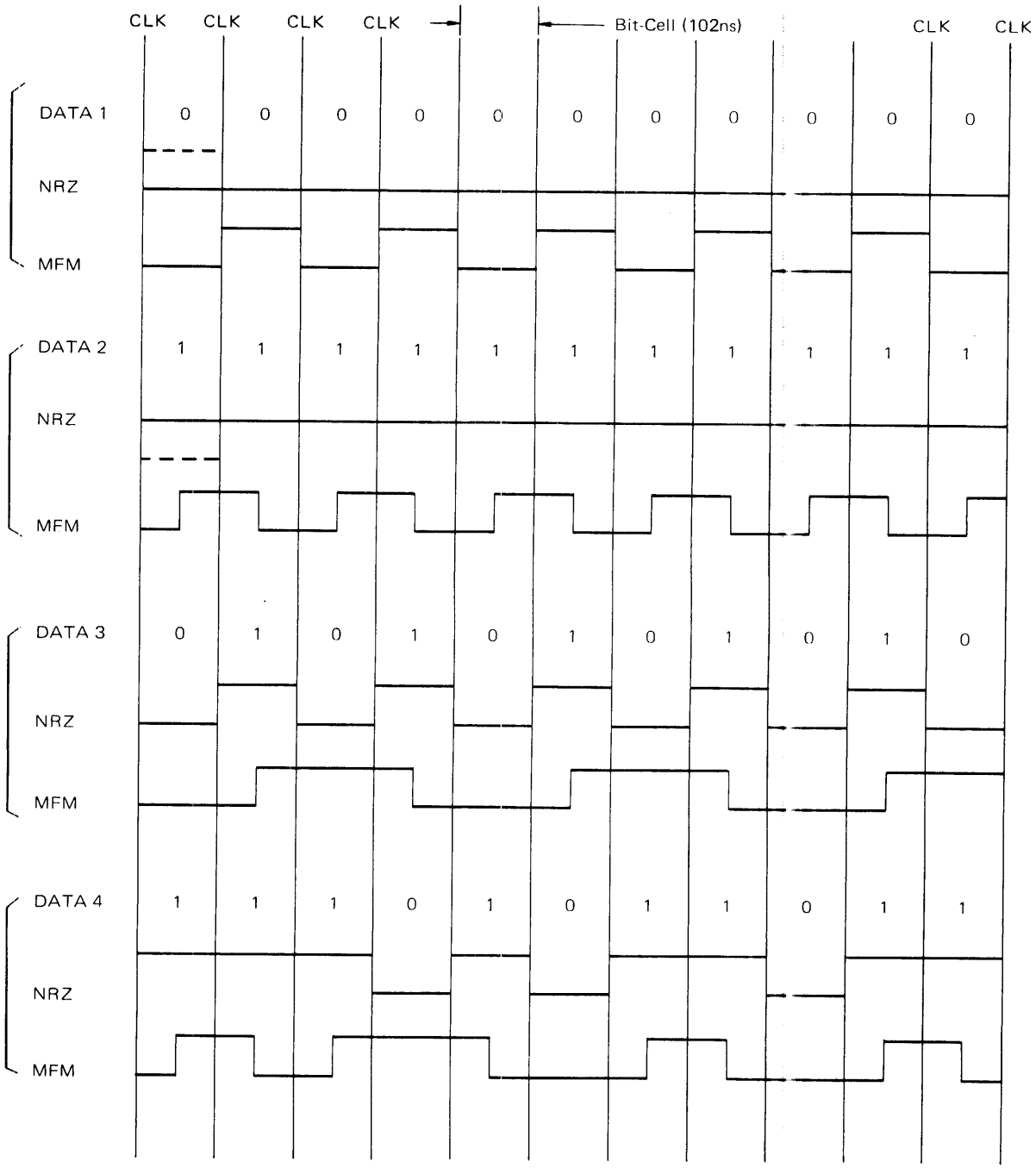


Figure 4-6-39 MFM Coding

4.6.8.2 Write Operation

The write circuit block diagram is shown in Figure 4-6-40. The servo data written on the disk are read by the servo head, and the PLO circuit generates one bit cell PLO1F signal. The PLO1F signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the PLO1F signal and generates a frequency twice the PLO1F frequency; it then generates VFO1F and VFO2F signal. VFO1F and VFO2F signals are applied to the Write Compensation circuit; VFO1F is also sent to the control unit as the 1F Write Clock signal. The control unit must use this 1F Write Clock signal during Write Clock (WCLK) and Write Data (WDAT) generating.

When a write command is issued from the control unit after head selection, the WDAT and WCLK signals are sent the disk drive, and the WDAT signal is clocked by the positive-going edge of WCLK signal.

The clocked WDAT signal is applied to Write Compensation (WCP) circuit, and then is compensated according to the theory of write compensation. Through the Write Compensation circuit, WDAT of NRZ code is converted into Write Data Pulse (WDP) of MFM code.

When the Write Gate signal goes true, the WDP signal is toggled by a flip-flop and passes through the Read/Write Bus Switch IC. It is then applied to the Head IC (HIC) chips as Data X (DX) and Data Y (DY) signals. The write current is supplied to the selected HIC chip through a Write Current (WC) line.

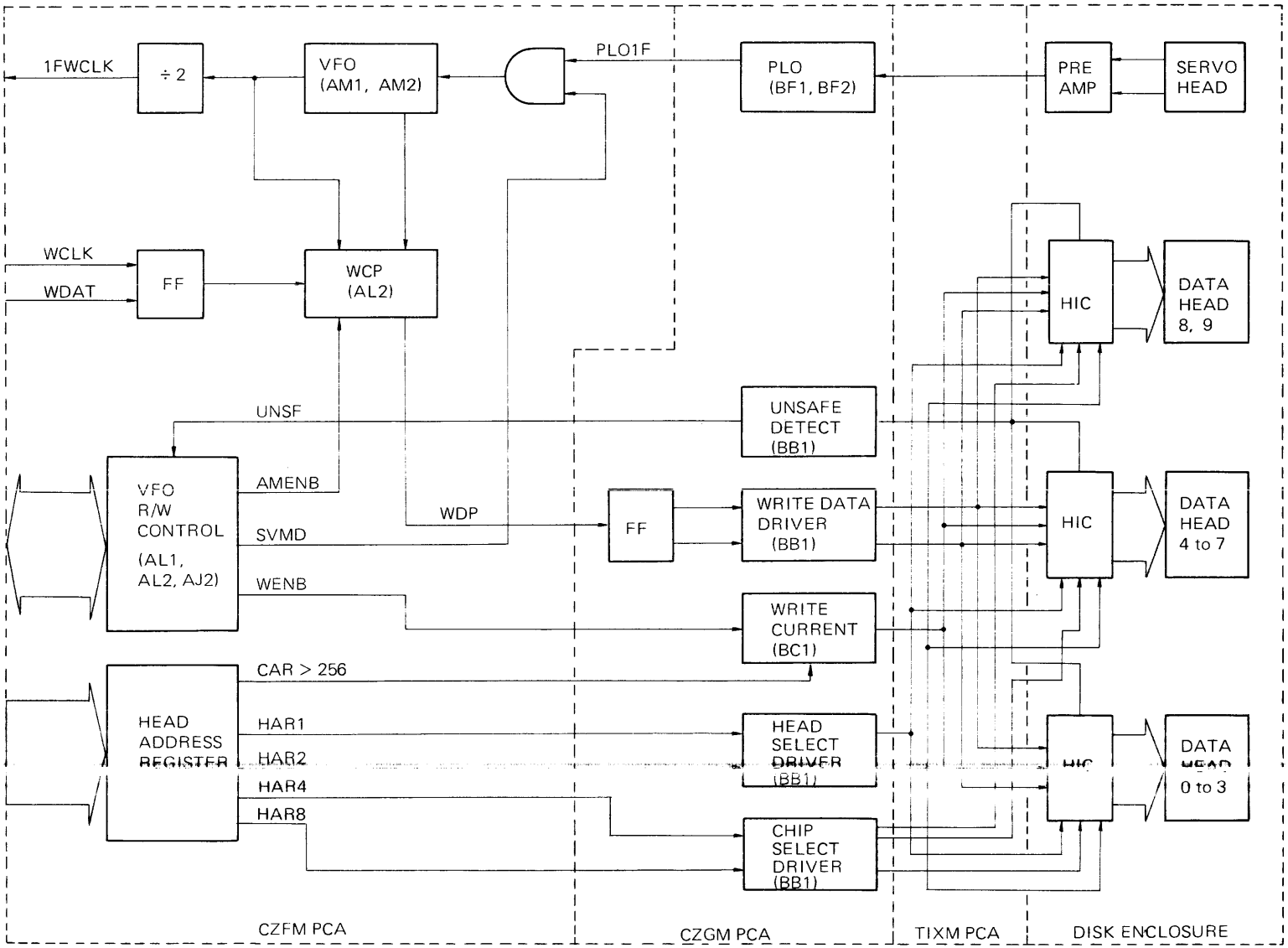


Figure 4-6-40 Write Operation Block Diagram

4.6.8.3 Write Compensation and MFM Coding

When the bit density (BPI) is high on a disk surface, and a read operation is performed, a peak shift phenomenon appears, which tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits. When such a phenomenon appears, reading of the data will deviate from the correct bit spacing, causing errors. The write compensation circuit measures this peak shift beforehand so the data is written by shifting the peak in the opposte direction of the peak shift appearing during the read operation.

The NRZ write data (WDAT) sent from the control unit is clocked by the positive-going edge of the WCLK signal. It is then synchronized with the internal one-bit cell clock whose phase is specified by a sync decision window circuit at the positive-going edge of the Write Enable (WENB) signal.

The NRZ data synchronized with the internal clock is applied to four-bit shift register. Each output of the four-bit shift register is applied to a write compensation decoder and a multiplexer and then converted into a MFM data pulse train with write compensation according to the truth table (as shown in Table 4-6-2). The preshift timing of write compensation is defined by 2F Early (2FEY), 2F On-Time (2FOT) and 2F Late (2FLT) signals.

The block diagram and timing chart are given in Figure 4-6-41 and Figure 4-6-42.

Table 4-6-2 Write Compensation and MFM Truth Table

SHIFT REGISTER STATUS				WRITE COMP			MFM	
SR 3	SR 2	SR 1	SR 0	EYP	OTP	LTP	CLP	DTP
1	0	0	*	1	0	0	1	0
0	0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	1	0
0	1	*	*	1	0	0	0	1
1	1	1	*	0	1	0	0	1
1	1	0	*	0	0	1	0	1

Note: EYP: Early Pulse
OTP: On-Time Pulse
LTP: Late Pulse
CLP: Clock Pulse
DTP: Data Pulse
*: Irelevant

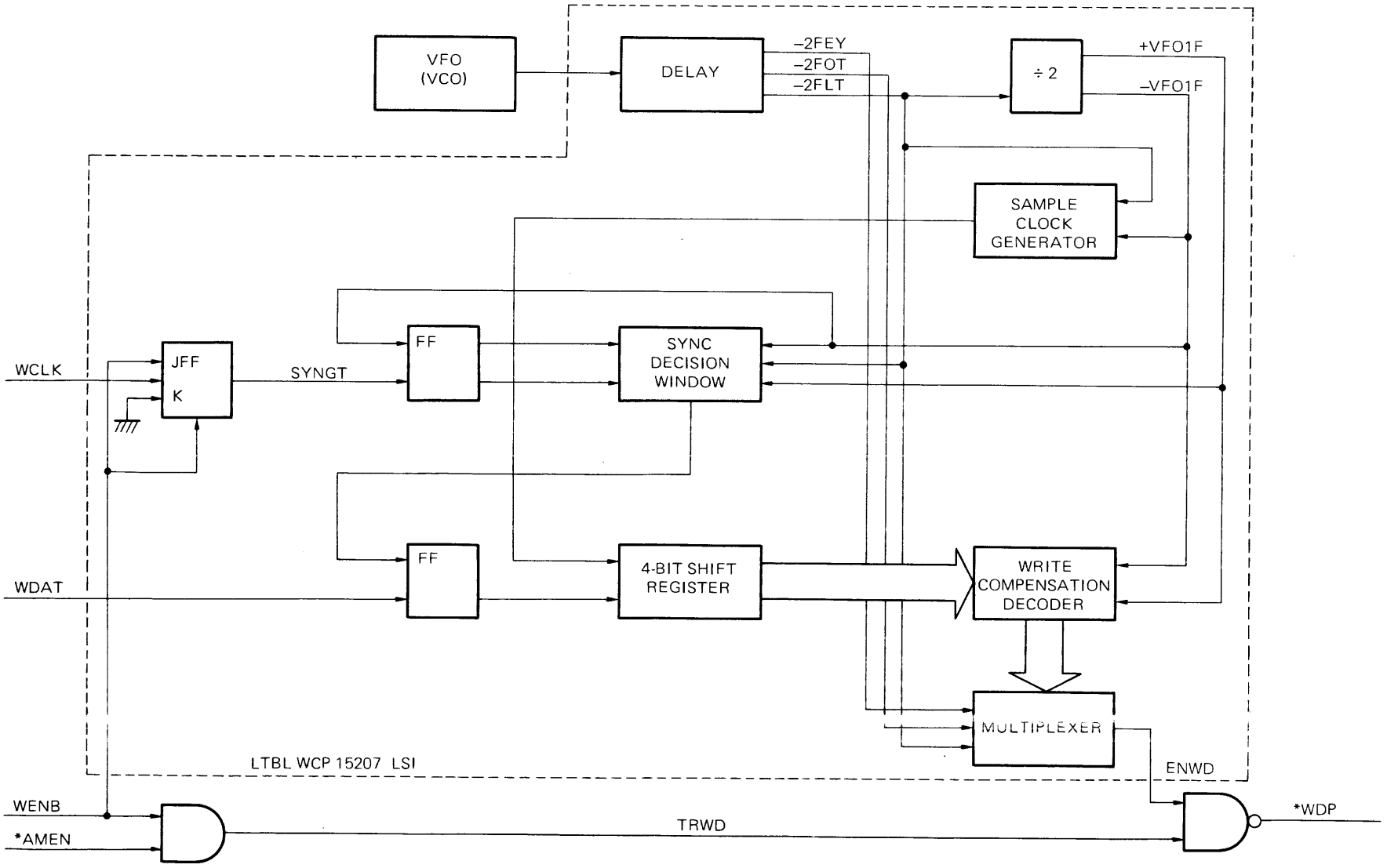
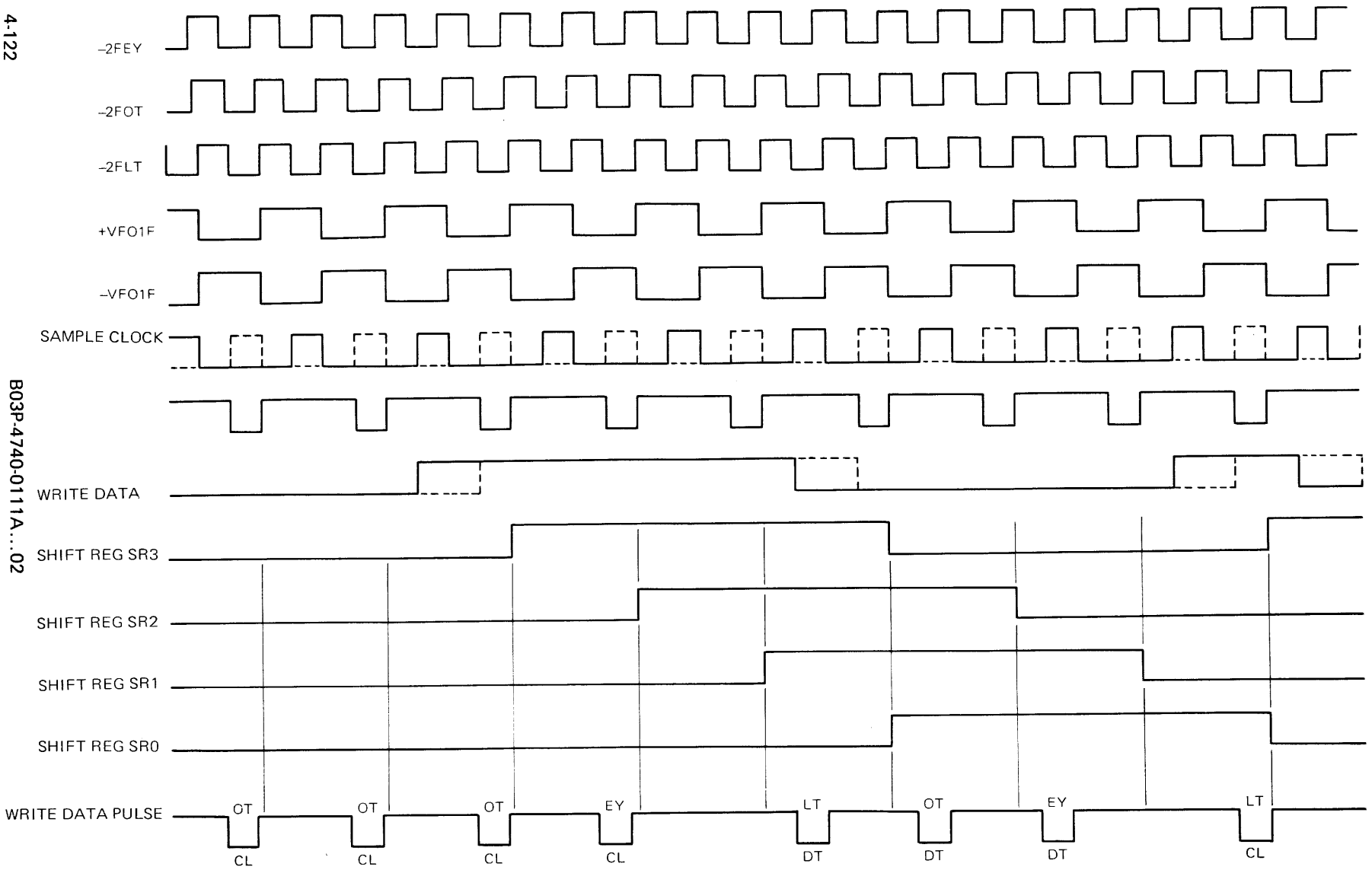


Figure 4-6-41 Write Compensation and MFM Coding Block Diagram



B03P-4740-0111A...02

Figure 4-6-42 Write Compensation and MFM Coding Timing Chart

4.6.8.4 Read Operation

A read operation is initiated by enabling Tag 3 and Bus 1 (Read Gate: RG). The analog read circuitry is enabled by disabling Write Enable (WENB).

The DX, DY HIC (Head IC) outputs are applied to the Read/Write Bus Switch IC (MB4316), amplified, and then sent to LPF (Low Pass Filter) circuit as shown in Figure 4-6-43.

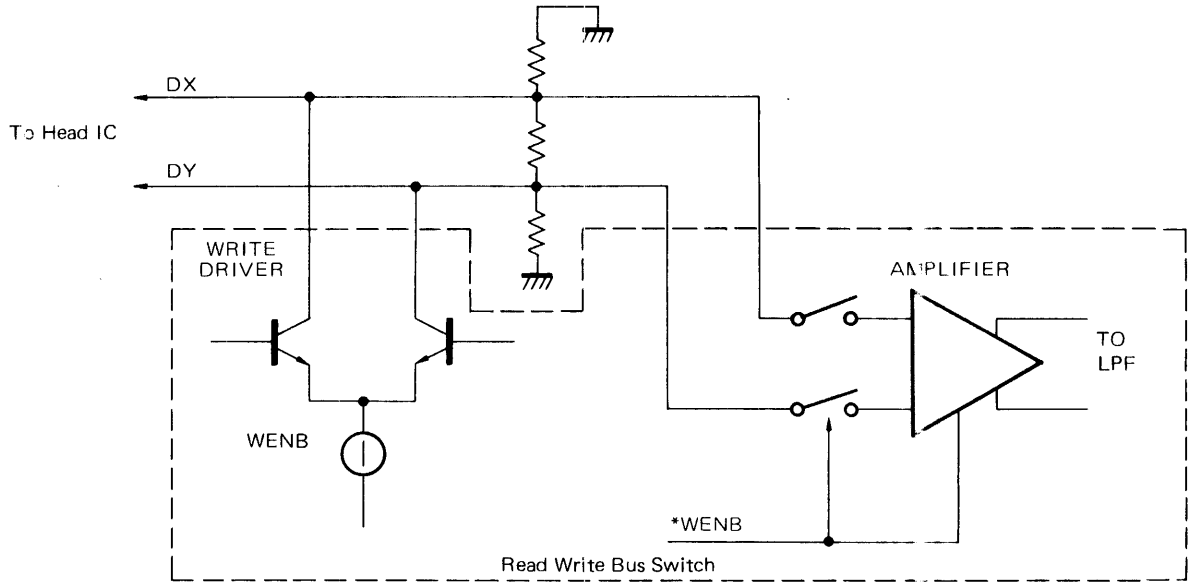


Figure 4-6-43 Read Write Bus Switch

The LPF attenuates the high-frequency noise; its output is then applied to the Automatic Gain Control (AGC) circuit.

The AGC circuit develops the control voltage to the AGC amplifier and holds AGC output amplitude (300 mVp-p) at a constant level. The output of the AGC amplifier is amplified to 3.0 Vp-p, and sent to the Pulse Shaper circuit.

After going false at WENB, the read circuit is activated; however, a read-transient which is caused by the DC unbalance of the read pre-amplifier will occur. WENB signal squelches this read transient (refer to Figure 4-6-44).

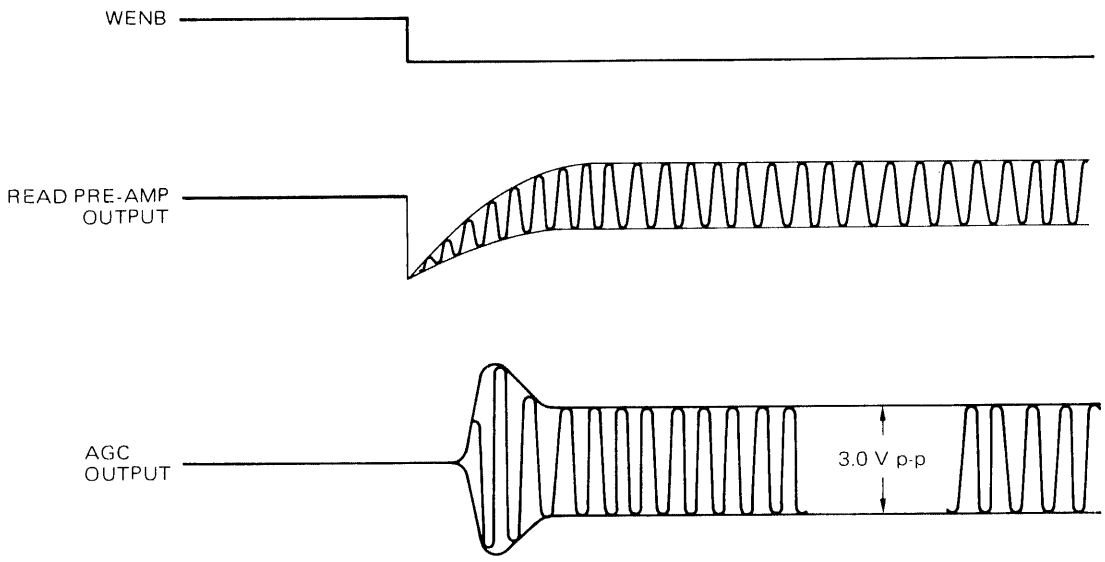


Figure 4-6-44 AGC Squelch Function

In the variable Soft Sector mode, the Address Mark (AM) which is a DC-erased three-Byte area is used for indicating the beginning of sector. When the control unit issues an AM-Read (Tag 3·Bus 1·Bus 5) command, the AM-Search (AMSH) signal goes true and suppresses the AGC output amplitude to avoid misdetection of an AM caused by external or media noise in the DC-erased area (refer to Figure 4-6-45).

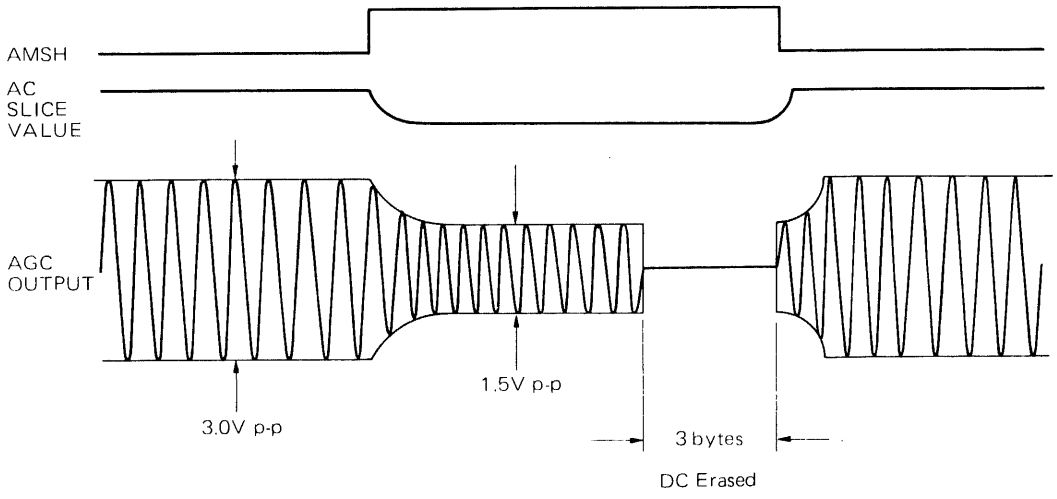


Figure 4-6-45 AM Search on Read Signal

The AGC output signal is applied to Pulse Shaper which is the analog-to-digital convertor circuit. Pulse shaper has following three fundamental circuits:

Differentiator circuit	:	Differentiates the AGC output signal and then converts the peaks into zero-crossing signals.
Integrator circuit	:	Integrates the AGC output signal and then generates the data window.
Fixed slice circuit	:	Slices the AGC output signal and then generates the data window.

The block diagram is shown in Figure 4-6-46 and the timing chart is shown in Figure 4-6-47.

The output of Pulse Shaper which is Raw Data (RAWDT), is sent to the VFO circuit and then is converted from MFM into NRZ data.

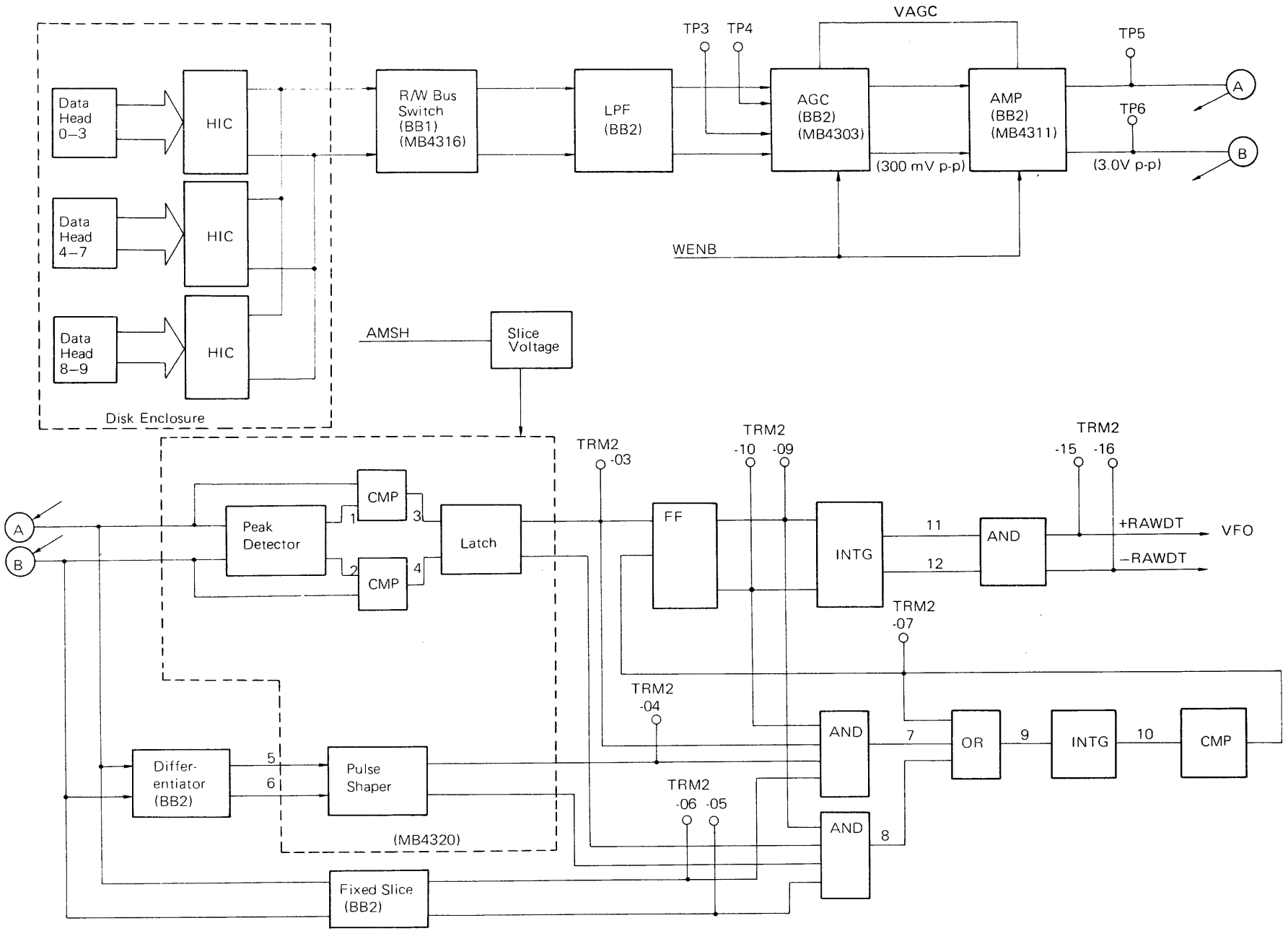


Figure 4-6-46 Read Operation Block Diagram

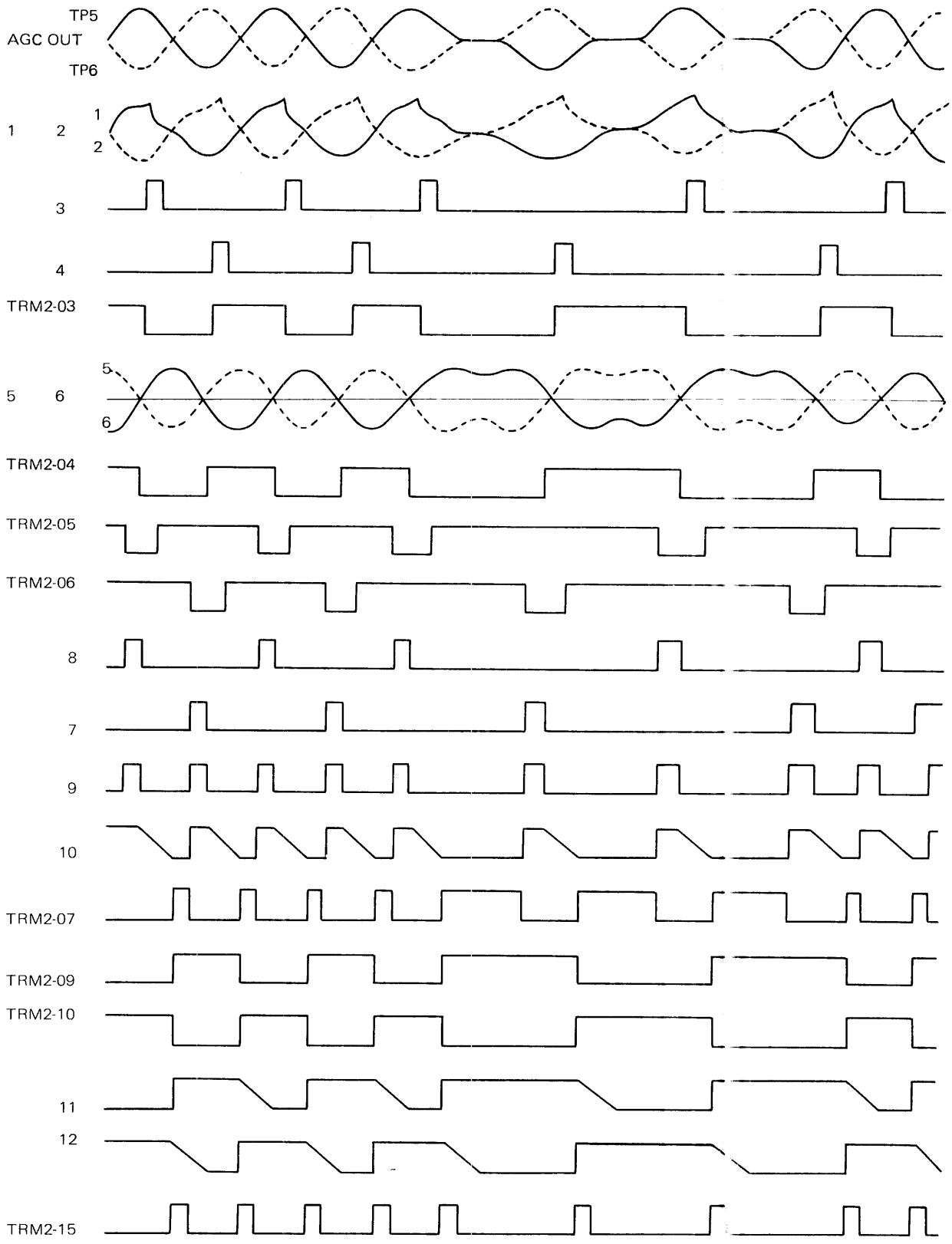


Figure 4-6-47 Read Data Analog to Digital Timing

4.6.9 VFO

4.6.9.1 VFO and Data Separator

The Variable Frequency Oscillator (VFO) circuit synchronizes with a PLO1F signal from the servo track during Not-Read operation and with the Raw Data (RAWDT) signal, from the data track, during a read operation. The block diagram of the VFO and Data Separator circuits is shown in Figure 4-6-48.

The VFO and Data Separator are composed of the following circuit.

(1) VFO Input Multiplexer
(2) Time-Margin Measurement (TMG) One-Short
(3) Reference One-Shot
(4) Phase-compare Latch
(5) Phase Comparator and Charge Pump
(6) Low-Pass Filter and Buffer
(7) Voltage-Controlled Oscillator (VCO)
(8) Data Separator

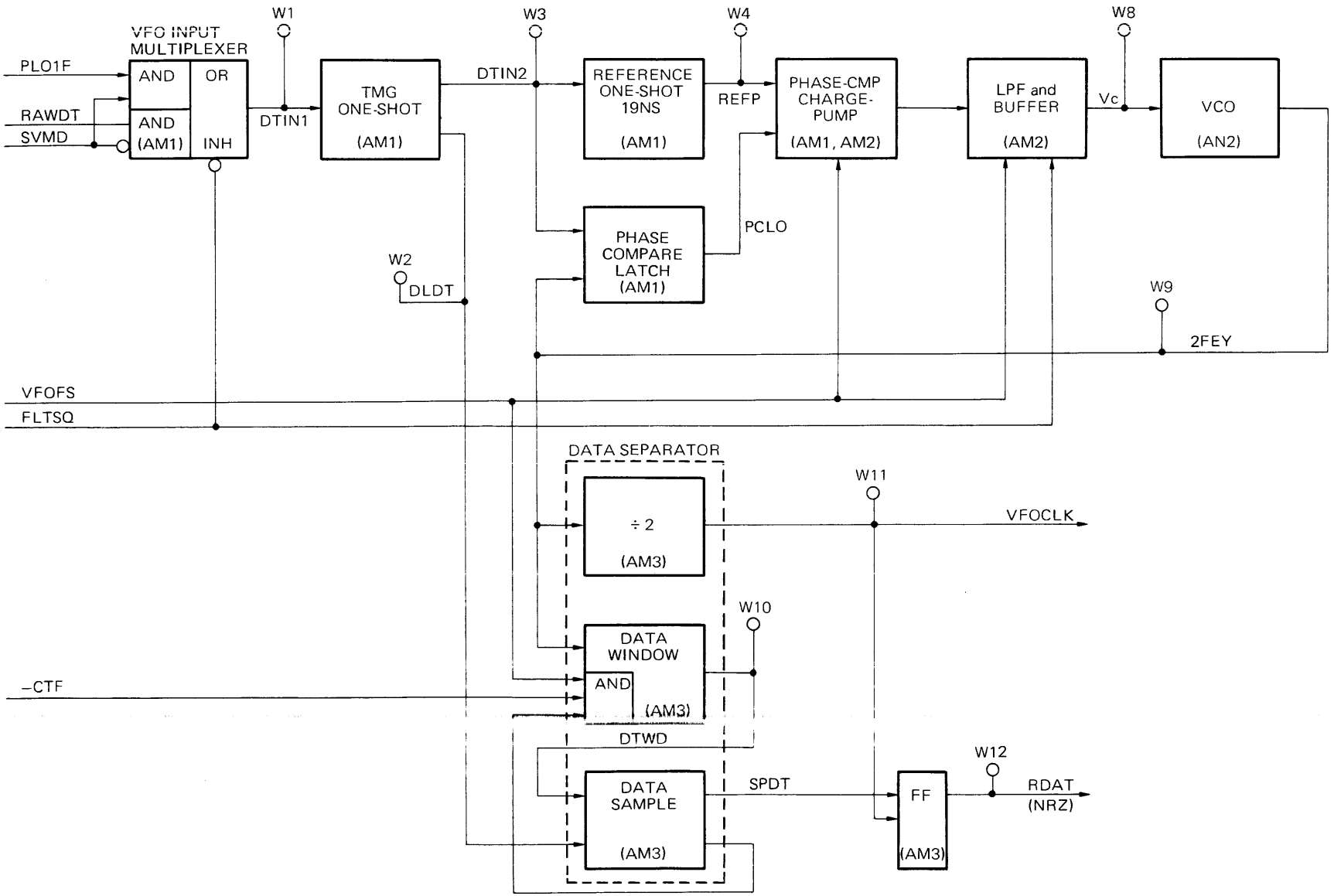


Figure 4-6-48 VFO/Read Data Separator Block Diagram

(1) VFO Input Multiplexer

The VFO input multiplexer controls the VFO input. During an initial seek operation or a RTZ operation, this circuit inhibits an input of Data into the VFO circuit by enabling the filter squelch (FLTSQ) signal. This causes the VCO to oscillate at a free-running frequency. After an initial seek operation or RTZ operation, the VFO Input multiplexer controls the transmission of the PLO1F or RAWDT signals into the VFO circuit.

During a Not-Read operation, the PLO1F signal is applied to the VFO circuits by the enabling of the servo mode (SVMD) signal. During a Read operation, the RAWDT signal is applied to the VFO circuits by disabling the SVMD signal. The VFO input multiplexer output, Data In 1 (DTIN1), is applied to the TMG One-shot circuit.

(2) TMG One-shot

The TMG One-shot circuit issues a Data Input 2 (DTIN2) signal to the Phase Comparator, and Reference One Shot. It also issues Delayed Data (DLDT) signal to the Data Separator. The timing relation between DTIN2 and DLDT signals is adjusted by potentiometer RV2 determines the read margin within the VFO circuit.

(3) Reference One-shot

The leading edge of the DTIN2 signal triggers the Reference One-shot, which issues a 19 ns Reference Pulse (REFP) signal to the Phase Comparator Charge Pump circuit.

(4) Phase-compare Latch

The leading edge of the DTIN2 signal sets the Phase-compare Latch and the negative-going edge of –2F Early A (–2FEYA) resets it. The Phase-compare Latch issues a Phase-compare Latch Output (PCLO) signal to the Phase Comparator Charge Pump Circuit.

(5) Phase Comparator and Charge Pump

The Phase Comparator circuit issues a decrease frequency (DEC) signal when the VFO input phase is leading, and an increase frequency (INC) signal when the VFO input phase is lagging, comparing the phases between a DTIN2 signal and a PCLO signal.

The INC or DEC signal drives the constant-current circuit in the Charge Pump circuit.

(6) LPF and Buffer

The charge pump output is applied to a Low Pass Filter (LPF) and converted into DC voltage to control the VCO. During an initial seek operation or RTZ operation, the FLTSQ signal clamps the charge pump output to 0 V to recalibrate the VFO function.

During an initial data read operation, a VFO fast-sync (VFOFS) signal is issued to the VFO circuit which increases the loop gain of the VFO circuit to widen the capture range, and to shorten the capturing time for synchronization to the RAWDT signal. At termination of the Data read operation, the same function is activated for synchronization with the PLO1F signal.

The LPF and Buffer output is applied to two stages of an emitter-follower circuit. It controls the VCO frequency as a control voltage (Vc) signal.

(7) VCO

The VCO circuit is an emitter-coupled multivibrator in which cross-coupled transistors, Q8 and Q9, form a positive-feedback gain stage. At any time either Q8 or Q9 and the timing capacitor, is alternately charged and discharged by the voltage-controlled current sources according to Vc signal.

The VCO circuit issues a 2F Early (2FEY) signal to the Data Separator and Write Compensation circuit. The 2FEY signal frequency increases when the Vc signal goes high, and decreases when Vc signal goes low.

(8) Data Separator

Through the before-mentioned process, the VFO circuit is synchronized with the RAWDT signal. The VCO output, 2FEY, is delayed to a 2FERLYB (—2FEYB) signal. The —2FEYB signal is applied to the data window circuit and Data Sample circuit. The —2FEYB signal is applied to two flip-flop in the Data window circuit, and then toggled at its positive-going edge. The VFO circuit can be synchronized with a normal phase relation or a 180 degree shifted phase relation. Therefore, the VFOFS and count F (—CTF) signals function as a "0" during the VFO fast mode.

The data window circuit issues a VFO clock (VFOCLK) signal to the interface circuit and a data window (DTWD) signal to the Data Sample circuit.

The positive-going edge of the DLDT signal clocks the DTWD signal, and then issues a —separated data (—SPDT) signal. When VFOFS, —CTF and SPDT signals go true, the DTWD signal phase is changed to a "0" on the SPDT signal during VFO fast mode. The SPDT signal is clocked by the positive-going edge of the VFOCLK signal.

The timing chart of the VFO is shown in Figure 4-6-49, and the timing chart of the Data Separator is shown in Figure 4-6-50.

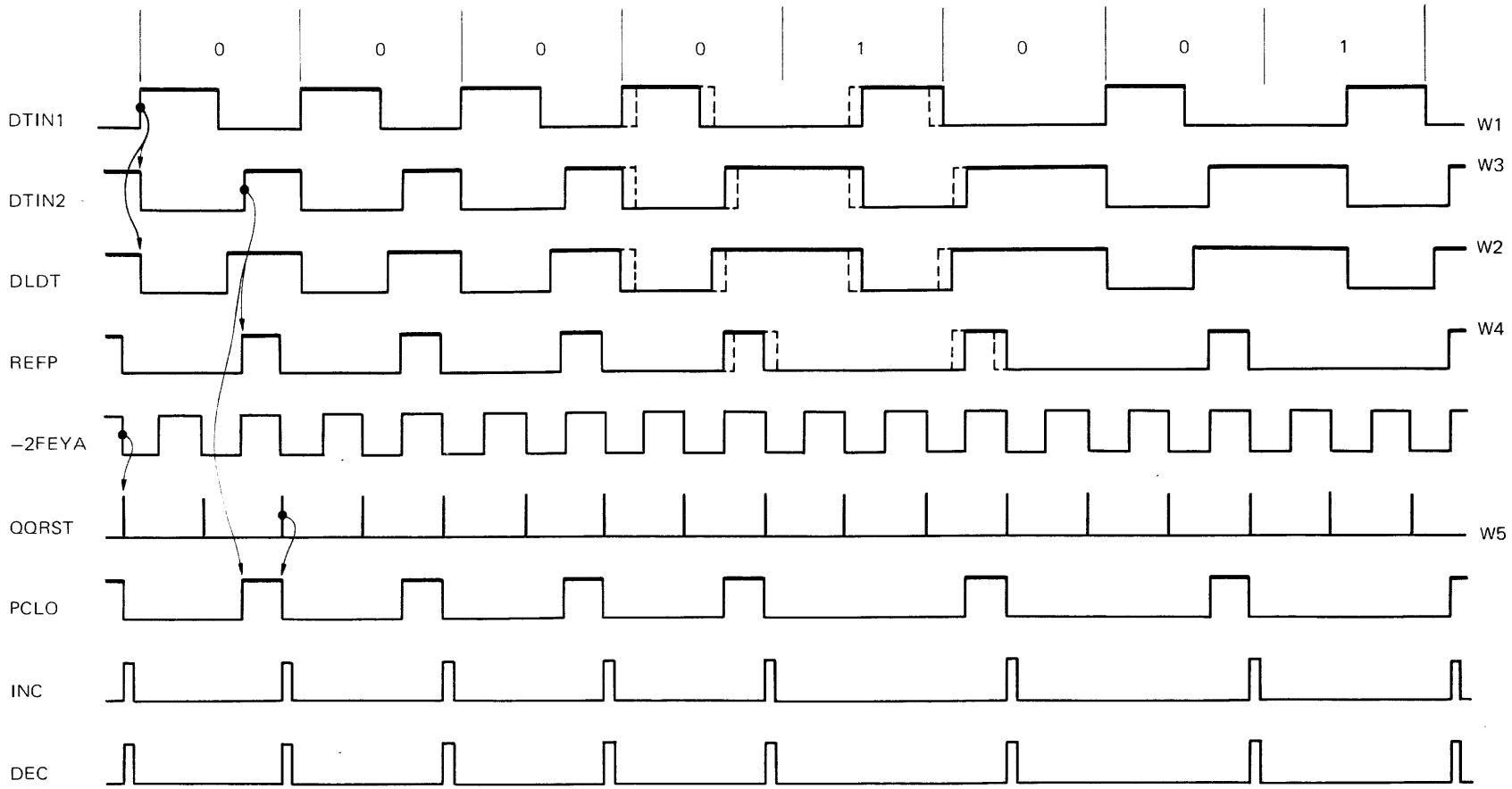


Figure 4-6-49 VFO Timing Chart

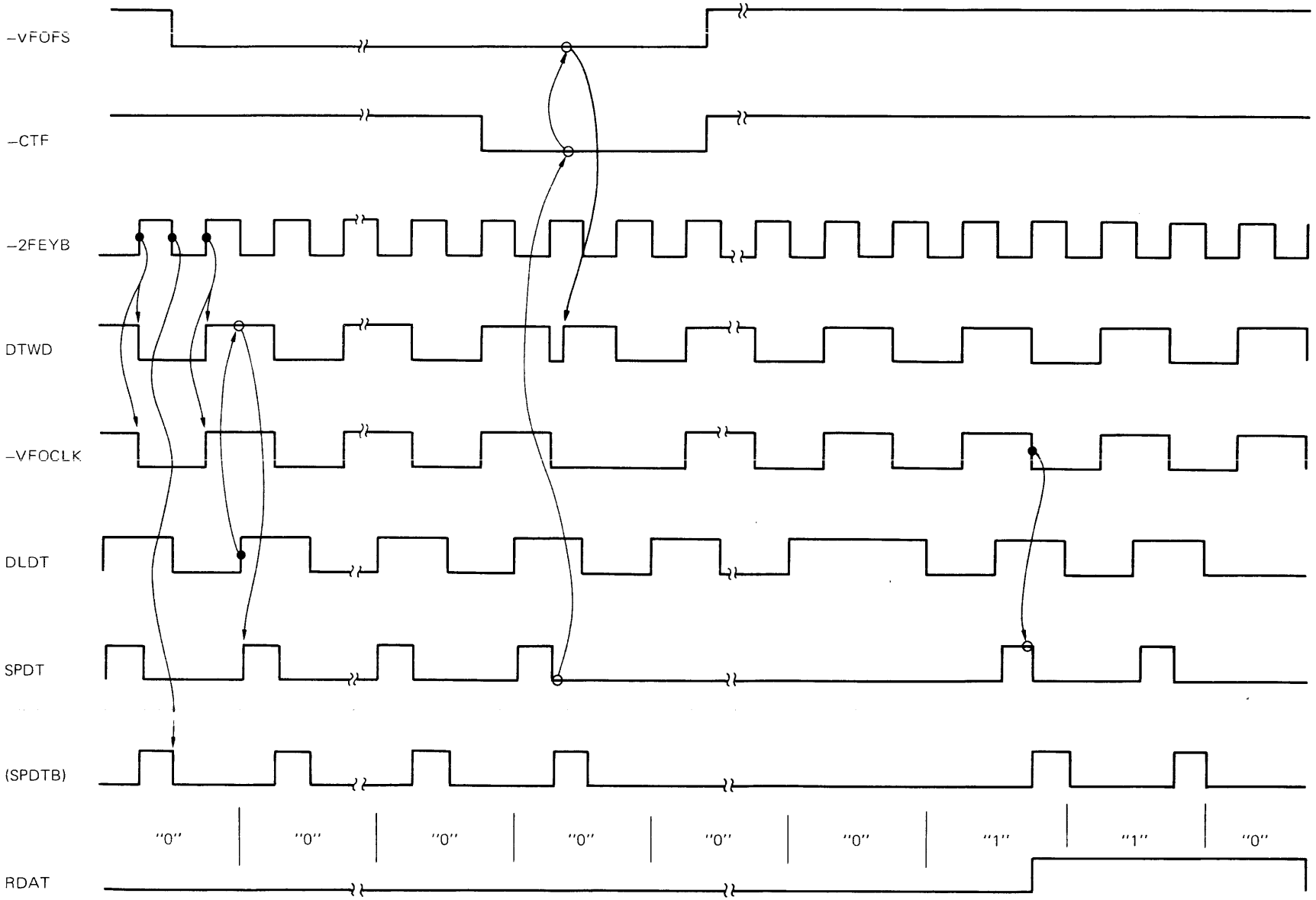


Figure 4-6-50 Data Separator Timing

4.6.9.2 VFO Control Logic

The VFO control circuit controls the input to the VFO circuit; that is, the PLO output PLO1F or recovered read data, RAWDT, it also generates a VFO fast synchronization (VFOFS) signal for faster VFO synchronization with the input signals RAWDT or PLO1F.

In a start-up sequence, the leading edge of the PWRDY signal sets the FLTSQ signal to inhibit the input to the VFO circuit. The initial seek completion sets a Linear Mode (LNMD) signal, and then resets the FLTSQ signal to enable the synchronization of the VFO circuit. The leading edge of the FLTSQ signal clocks the initial VFO fast-sync (IVFOFS) counter which issues a 12-byte pulse of the VFOFS1 signal and a 1-byte pulse of the Count F (CTF) signal at the last of the VFOFS1 signal.

The leading edge of the VFOFS1 signal sets the Servo Mode (SVMD) latch. The SVMD signal is applied to the VFO input multiplexer so that the PLO1F signal is applied to the VFO. Simultaneously, the VFOFS signal (12-byte) activates the fast synchronization of the VFO circuit.

When either PWRDY or SPGD signal, go false or when a seek error has occurred, or when a RTZ command is issued to the drive, the FLTSQ signal will go true. A block diagram of VFO control is shown in Figure 4-6-51, and the timing chart of an initial VFO control is shown in Figure 4-6-52.

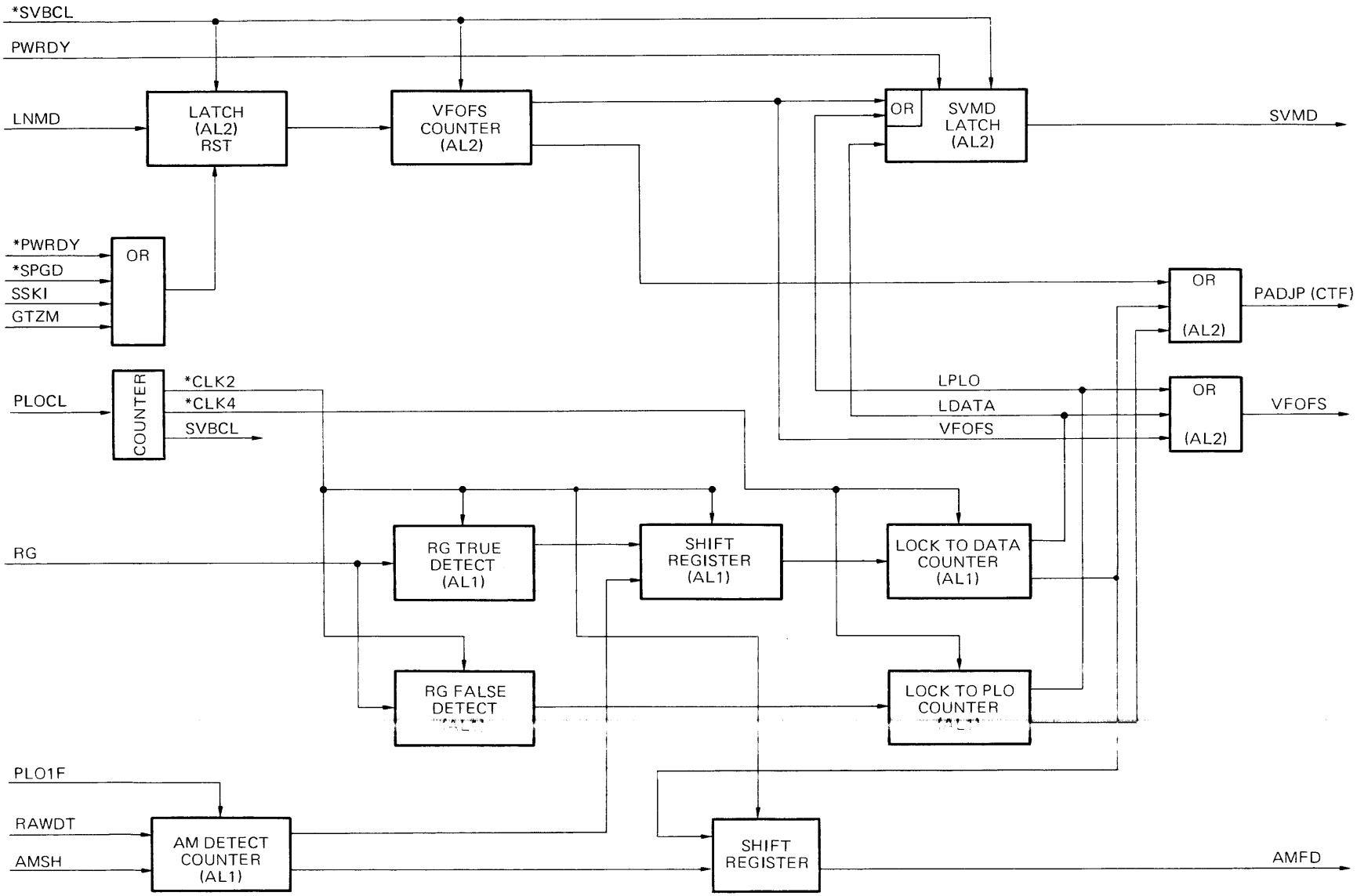


Figure 4-6-51 VFO Control Logic Block Diagram

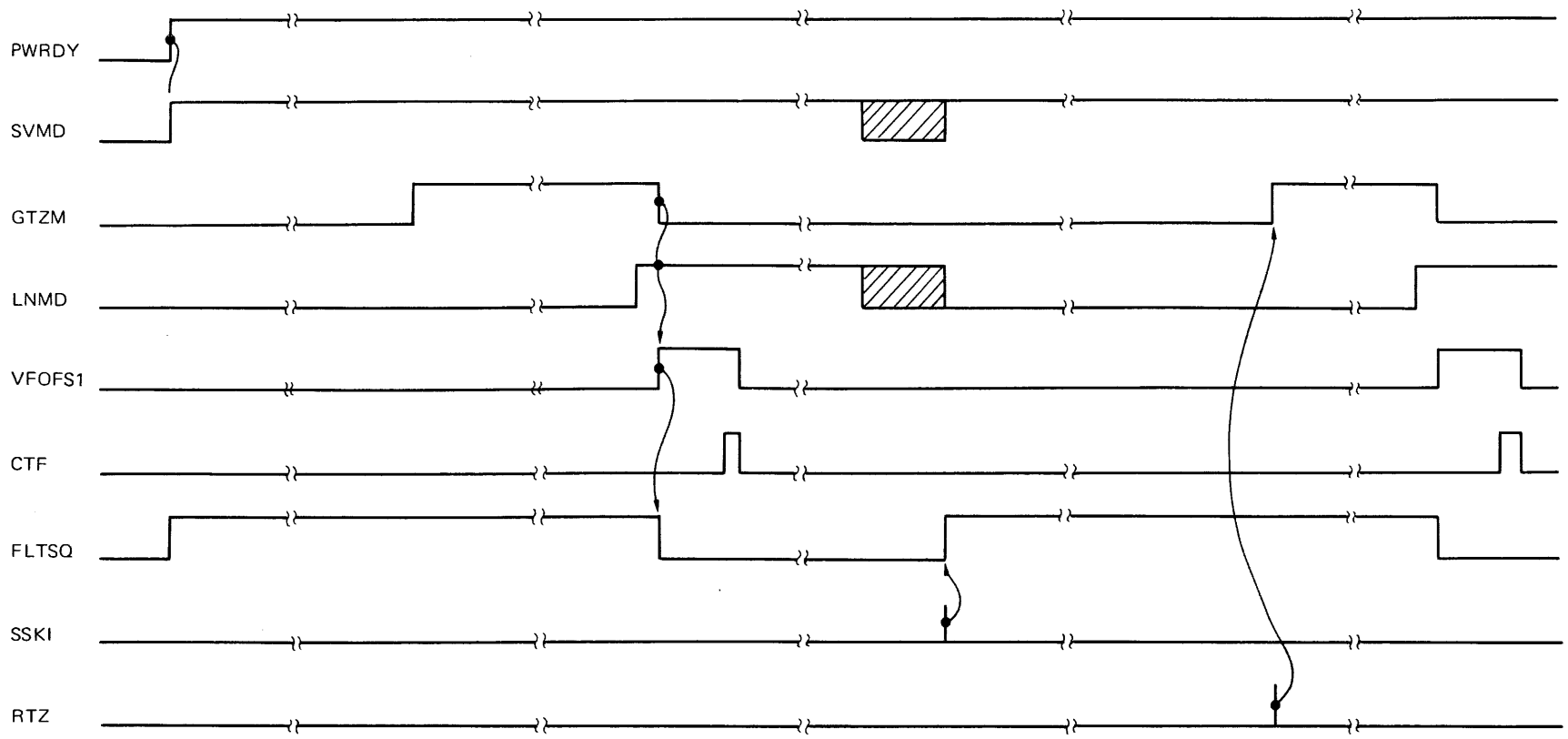


Figure 4-6-52 Initial VFO Control Timing Chart

During a Non-read operation, the VFO circuit synchronizes with the PLO output, PLO1F, and generates a VFO clock (VFOCLK). In Hard Sector mode, at the beginning of a read operation, Read Gate is applied to the RG True Detect circuit and is clocked by the positive-going edge of the *CLK2 signal.

A rise read gate (RRG) signal, which is an output of the RG True Detect circuit, is applied to 4 byte shift register. Its output then Load 8 on the lock-to-data counter to generate a 4-byte lock-to-data (LDATA) signal, and phase Adjust Pulse (DCTF). The leading edge of the LDATA signal resets Servo Mode (SVMD) so that the VFO circuit synchronizes with RAWDT.

In Variable Soft Sector Mode, the Rise AM Found (RAMF) signal sets the lock-to-data counter to generate the LDATA signal. (Refer to Figure 4-6-53).

At the end of the Read Gate signal, a half byte Set Lock-To-PLO (SLPLO) signal is issued and applied to the Lock-To-PLO Counter to generate a 4-byte Lock To PLO (LPLO) signal. The LPLO signal sets Servo Mode (SVMD) so that the VFO circuit synchronizes with PLO1F.

The LDATA and LPLO signals are converted into the VFO Fast-sync (VOFS) signal and applied to the VFO LPF circuit to decrease the time constant of the LPF. This promotes faster synchronization of the VFO circuit with RAWDT or PLO1F.

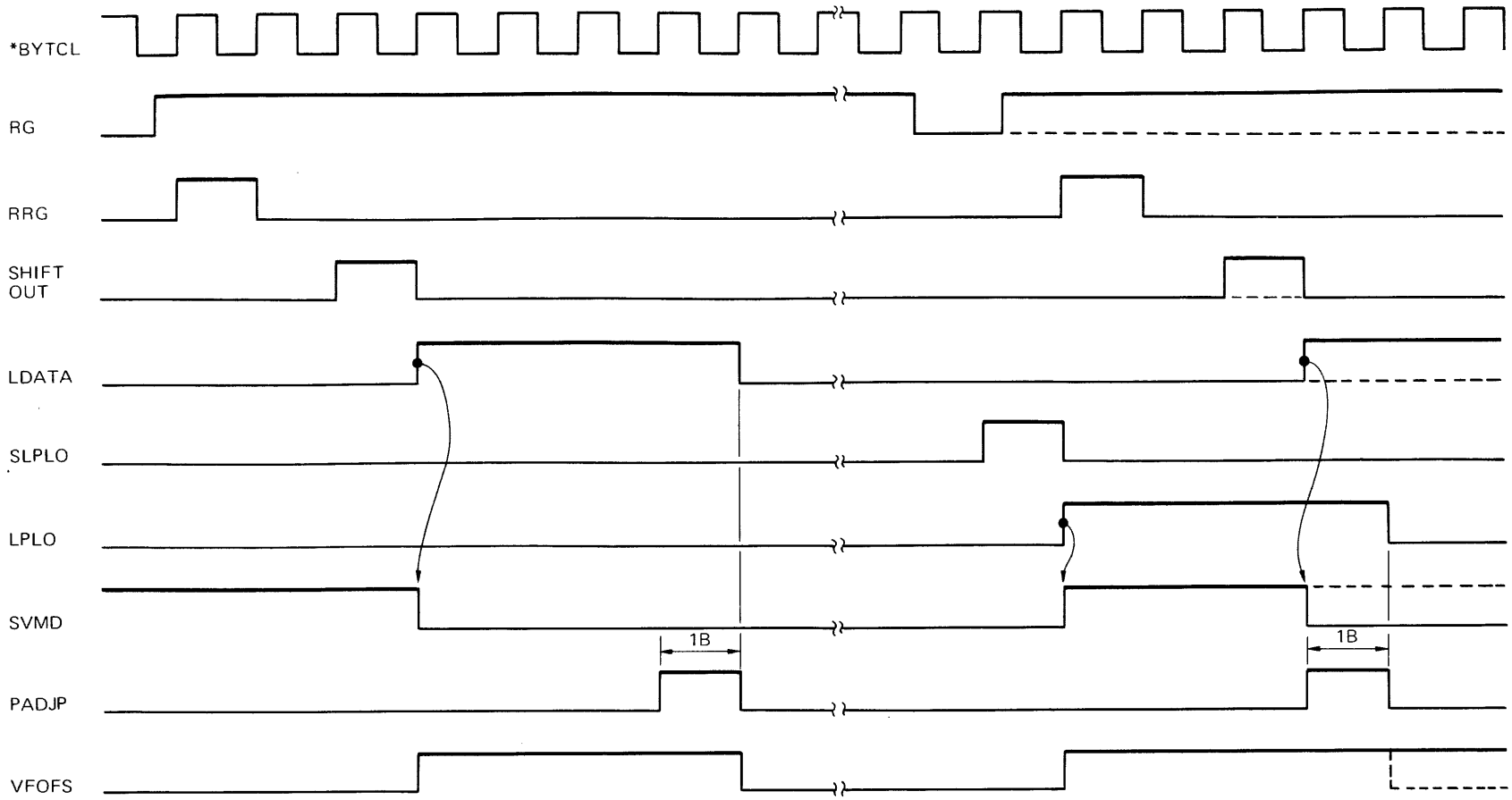


Figure 4-6-53 VFO Control Timing Chart

4.7 POWER SUPPLY THEORY OF OPERATION

4.7.1 General

This section contains circuit descriptions of the features within the Power Supply.

This power supply is a switching regulator of the inverter control type. The output voltage of the inverter is controlled by changing the pulse width. The regulated output voltage is obtained by transforming the input voltage according to the turn ratio of the primary and secondary inverter transformer. The output is then rectified and smoothed.

The theory of regulation is output voltages are controlled by the inverter input pulse width which is modified according to the input and output voltages.

The inverter transformer isolates the primary lines from the secondary lines. By raising the working frequency of the inverter, its physical size is reduced to a minimum. The smoothing circuit, after the inverter, is of the choke input type and provides the mean value of the rectifier output voltage.

The output voltage of the +5V circuit controls the inverter. The +24V DC and −12V DC output voltages are provided from separate windings of the transformer.

These features are shown in block diagram in Figure 4.1. A wave form which can be observed on each line is shown in Figure 4.2.

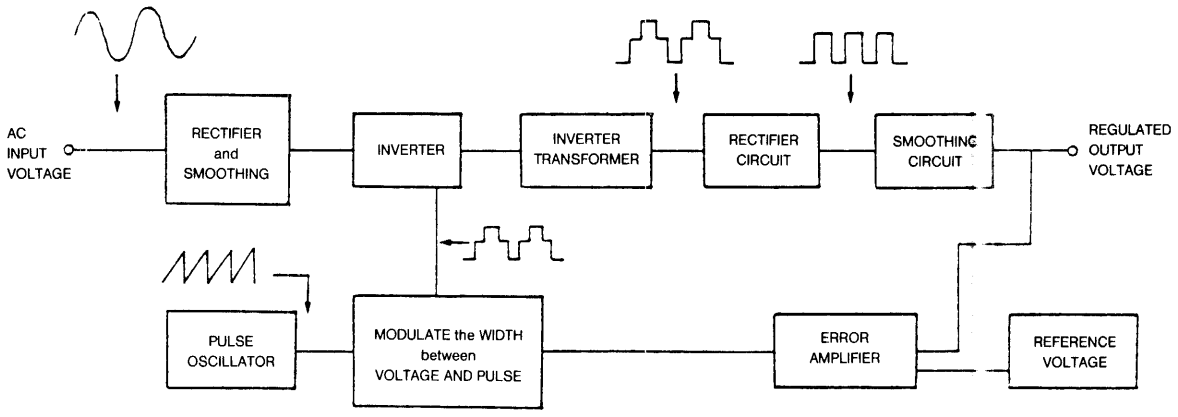
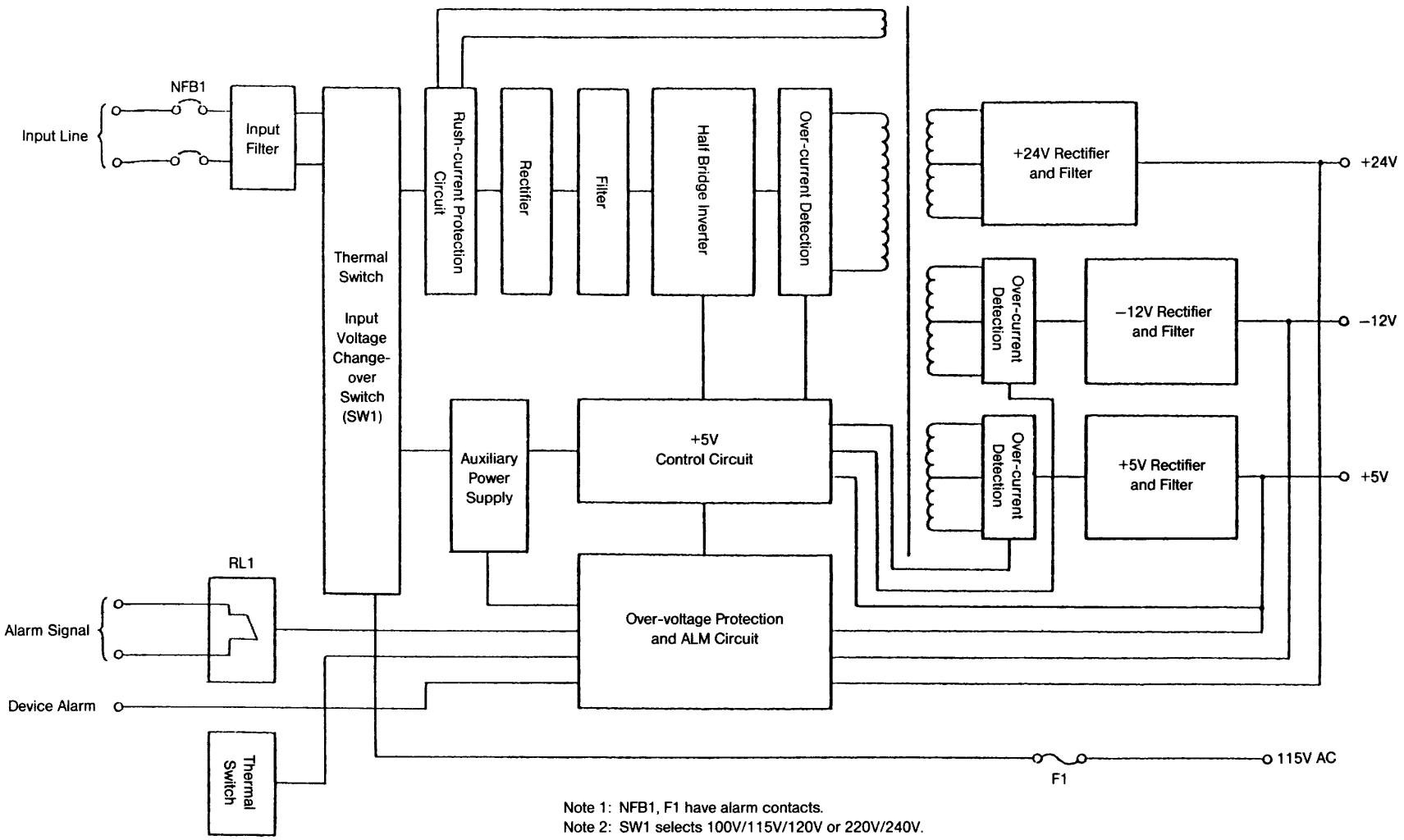


Figure 4.7.1 Block Diagram and Waveform



Note 1: NFB1, F1 have alarm contacts.
Note 2: SW1 selects 100V/115V/120V or 220V/240V.

Figure 4.7.2 Power Supply Block Diagram

4.7.2 AC Input

AC line input voltage is applied to circuit breaker (NFB1) through the terminal number 1 and 2 of TRM1. The filtered AC line input from NFB1 is applied to the voltage select switch (SW1). SW1 is the switch which selects the input voltage group, 100, 115, 120V or 220, 240V. The primary rectifier form is changed by selecting SW1. The auxiliary power supply transformer changes the input voltage by selecting the tap.

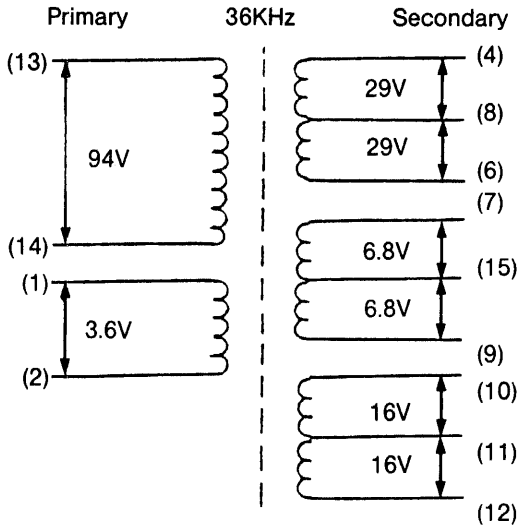
SW1 has a lock mechanism to prevent accidental switching. Rectified input voltage is smoothed by the capacitor and is applied to the half-bridge type inverter. The output voltage of the inverter, which drives the secondary main transformer, is rectified, filtered and becomes the output voltage.

4.7.3 Voltage Regulation

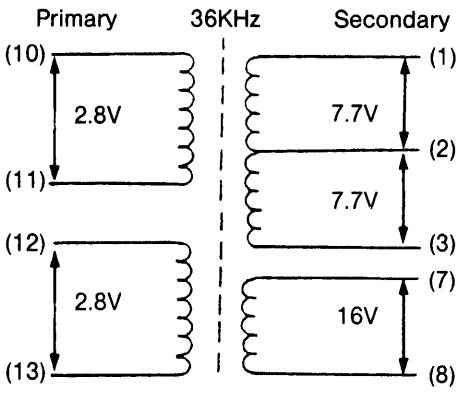
DC output voltage regulation of ±5% is achieved on all DC outputs even under worst case conditions of temperature, input voltage, frequency and load. Line voltage and frequency variations of +10/−12%, respectively, can be tolerated without degradation of the power supply performance.

4.7.4 Over-voltage Protection Circuit

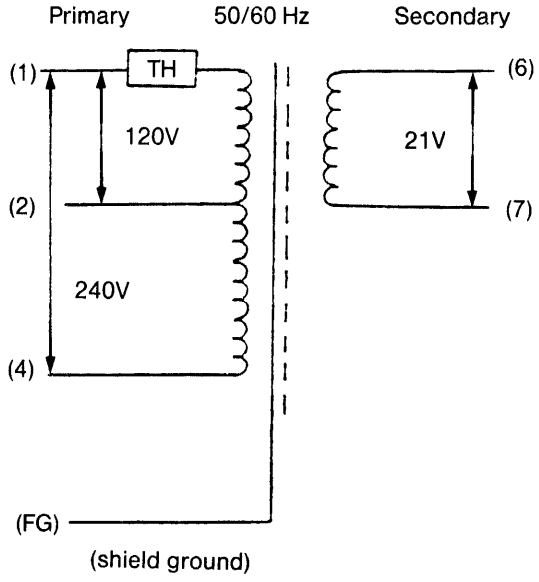
Over-voltage protection circuits are used to insure that the output voltage level will not damage the disk drives if the power supply circuits should malfunction. If the +5V supply circuit exceeds about 6.5V, all DC output voltage will be turned off and the power alarm lamp will be set.



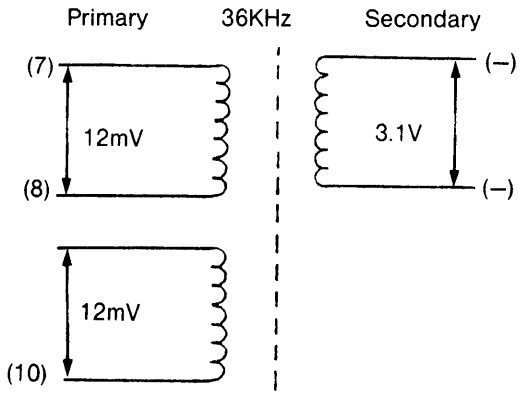
Transformer T1
(on the PWB "AD1")



Transformer T3
(on the PWB "AD3")



Transformer T2
(on the PWB "AD1")



Transformer CT1
(on the PWB "AD3")

Note: Numbers in ( ) show the markings which are marked around wires.

Figure 4.7.3 Input/Output Voltages of Transformers

4.5 Over-current Protection Circuit

The DC output voltage circuit is provided with the over-current protection circuit. This circuit protects the power supply when the output voltage is shorted and improper current begins to flow. The circuit decreases the voltage if the output current of +5, +24 or −12V DC exceeds the established limit value.

4.6 Alarm Circuit

This power supply is provided with an alarm circuit. This circuit detects improper voltage, temperature rise, fan stopped, device alarm, etc., and turns off the DC output, lights the alarm lamp, and outputs the alarm signal. The alarm lamp is on the front panel. To clear the alarm condition, turn off the main line switch (NFB1) and power up again.

4.7 Device Alarm Circuit

When the device alarm signal is received from the disk drive, the device alarm circuit turns off the DC output, lights the device alarm lamp, and outputs the alarm signal.

4.8 Alarm Signal

The Alarm Signal is a signal output on TRM1-4 and 5. This signal is supplied when either the Power Alarm or Device Alarm circuits are activated and is for customer use only.

4.9 Transformer Voltages

The input/output voltages of transformers are shown in Figure 4.3.

Section 5

Troubleshooting Guide

5. TROUBLESHOOTING GUIDE

5.1 INTRODUCTION

This section will contain troubleshooting flow charts arranged according to the error status on the disk unit and control unit.

Note: Before any operation is attempted, maintenance personnel should read carefully Section 6 (Maintenance) and fully understand the details of the procedures and tools required.

Check the following items in list before applying power to the unit after installation.

(1) Ensure that the AC line conditions satisfy the power supply requirements.
(2) Ensure that the DC voltages satisfy the unit requirements.
(3) Inspect the interface cables to ensure pin 1 on the cable goes to pin 1 of the connector at both the unit and at the control unit.
(4) If the unit is in a daisy chain mode with one or more units, make sure that only the last unit has a line terminator (LTN) installed.
(5) Ensure that the desired logical unit number (LUN) of the unit is selected on the CZFM PCB, see Section 3.7.1 and that each LUN in the system is unique.
(6) Ensure that Hard/Soft sector mode is selected, see Section 3.7.2, per the system configuration.
(7) In the case of Hard Sector (fixed sector length), ensure that the correct sector count is set on CZFM PCB, see Section 3.7.7.
(8) Ensure that Tag 4/5 Enable or Disable is set, per the system configuration. See Section 3.7.3.
(9) Ensure that File Protect key is in the proper position to meet the system requirement, see Section 3.7.4.
(10) Ensure that Disable/Normal keys are correctly set to the Normal position. (Dual Channel option)
(11) Ensure the Release Timer key is set to the desired position. (Dual channel option)
(12) Ensure that all PCB assemblies and cables are firmly seated.

5.2 ERROR STATUS

The disk unit, optional power supply unit (PSU), and/or the control unit will issue the following statuses as shown in Table 5-2-1.

Table 5-2-1 Error Status

Error Status	Definition	Information Source
Alarm	Power malfunction has occurred on the disk unit or optional PSU.	Optional PSU
Not Selected	The control unit cannot select the specified disk unit.	Disk Unit Control Unit
Not Power Ready (*PWRDY)	DC power is not sufficient for the specified voltage.	Disk Unit (CZFM)
Power-up Sequence Check	Power-up sequence is not completed.	Disk Unit (CZFM)
Device Check (DVCK)	DVCK indicates a fault condition has occurred in the disk unit.	Disk Unit (CZFM)
Seek Error (SKERR)	SKERR status indicates that a seek malfunction has occurred in the disk unit.	Disk Unit (CZFM) Control Unit
Read Error	READ ERROR status result if a data error has occurred in read operation.	Control Unit
AM Missing	AM MISSING status indicates the Address Mark (AM) has not been found in a AM read operation. (Soft sector mode)	Control Unit
Dual Channel	DUAL CHANNEL malfunction concerns Select/Reserve functions.	Control Unit

Maintenance personnel can see the Power-up Sequence Check, Device Check (Fault) or Seek Error status at Fault Indicator LEDs on CZFM PCB assembly. These LEDs are defined as shown in Table 5-2-2.

Table 5-2-2 Fault Indicator Definition

Error Status	Status Tag		Status Bit			Error Code	Description
	2	1	4	2	1		
Power-up Sequence Check	0	0 ↑↓ 1	0	1	1	03/0B	Actuator Lock check (State 3)
			0	1	0	02/0A	DC Motor Accelerate check (State 2)
			1	1	0	06/0E	Accelerate complete check (State 6)
			1	1	1	07/0F	Initial seek check (State 7)
			1	0	1	05/0D	Emergency on Ready check
Device Check (Fault)	0	1	0	0	1	09	Control Check 1
			0	1	0	0A	Control Check 2
			0	1	1	0B	Write Off-track Check
			1	0	0	0C	Write Unsafe Check
			1	0	1	0D	Write Protect Check
			1	1	0	0E	Maltiple Head Check
			1	1	1	0F	Emergency (Consequently 05/0D)
Seek Error	1	0	0	0	1	11	RTZ Time-out Check
			0	1	0	12	Seek Time-out Check
			0	1	1	13	Over-shoot Check
			1	0	0	14	Seek Guard Band Ckeck
			1	0	1	15	Linear Mode Guard Band Check
			1	1	0	16	RTZ outer Guard Band check
			1	1	1	17	Illegal Cylinder Check

5.3 FAULT ISOLATION LIST

To isolate the fault, the possible faults defined by fault code and assembly to be replaced are listed in Table 5-3-1.

Table 5-3-1 Fault Isolation List

Code	Definition	Description
03/0B	Actuator Lock Check (State 3)	Description : indicates that the actuator was not released during State 2, which was detected by no current flowing through the solenoid. Possible Fault: ① Disconnection of CN12 on TVQM ② Actuator auto-lock fault (Drive) ③ Relay RL1/RL3 fault (TVQM PCB) ④ Relay driver fault (CZGM PCB) ⑤ Release detection fault (CZGM PCB) ⑥ Power-up sequence control fault (CZFM)
02/0A	DC motor Accelerate check (State 2)	Description : indicates that the rotational speed did not come up to 94% speed within 50 seconds of State 2. Possible Fault: ① Disconnection of CN11 of TVQM PCB. ② Power amplifier fault (TVQM PCB) ③ DC motor control fault (CZGM PCB) ④ +24V DC too low (Power Supply) ⑤ DC motor itself fault (Drive) ⑥ Power-up sequence control fault (CZFM)
06/0E	Accelerate complete check (State 6)	Description : indicates that the first acceleration of spindle motor was not terminated within 16 seconds of State 6. Possible Fault: ① Power amplifier fault (TVQM PCB) ② DC motor control fault (CZGM PCB) ③ +24V DC too low (Power Supply) ④ DC motor itself fault (Drive) ⑤ Power-up sequence control fault (CZFM) ⑥ Power supply fault.
07/0F	Initial Seek Check (State 7)	Description : indicates that initial seek was not completed or not terminated within 4 seconds of State 7. Possible Fault: ① Power amplifier fault (TVQM PCB) ② Actuator auto-lock fault (Drive) ③ Position sensing fault including PLO (CZGM PCB) ④ Servo control fault (CZGM) ⑤ Power-up sequence or seek control logics fault (CZFM) ⑥ Servo surface malfunction (Drive) ⑦ VCM fault (Drive) ⑧ Power supply fault.
05/0D	Emergency on Ready Check	Description : indicates that VCM/DC motor over-heat or DC motor fault (sensor fault) occurred during Ready Status (State 4), and consequently goes to not-ready status. Possible Fault: ① Power amplifier fault (TVQM PCB) ② Servo control fault (CZGM PCB) ③ Seek control logic fault (CZFM PCB) ④ VCM itself fault (Drive) ⑤ DC motor control fault (CZGM PCB) ⑥ DC motor phase detection fault (TVQM PCB) ⑦ DC motor phase decoder fault (CZGM) ⑧ Disconnection of CN11 of TVQM PCB

Table 5-3-1 Fault Isolation List (Continued)

Code	Definition	Description
09	Control Check 1	Description : indicates that illegal command was issued from the control unit during not-ready status, head's moving or seek error status. Possible fault: ① Illegal command from the control unit. ② Driver/receiver fault (CZFM PCB) ③ Cabling fault to the control unit.
0A	Control Check 2	Description: indicates that illegal write command sequence has occurred within the drive. Possible fault: ① Illegal command from the control unit ② Driver/receiver fault (CZFM PCB) ③ Cabling fault to the control unit
0B	Write Off-track Check	Description : indicates that Off-track condition has occurred during write operation. The Off-track condition is detected by exceeding ±0.65 V0-p on FNPOS signal. Possible fault: ① Servo control fault including adjustments (CZGM) ② Position sensing fault (CZGM) ③ Servo surface malfunction (Drive)
0C	Write Unsafe Check	Description : indicates that write operation was not completed caused by write driver. Possible fault: ① Write circuit fault for any head (CZGM) ② Specific head assembly fault (Drive) ③ Specific head group at HD0 to 3, HD4 to 7, or HD8/9 • HIC/chip select fault (CZFM) • HIC itself fault (Drive) ④ Head select fault (CZGM) ⑤ Illegal head address by the control unit ⑥ MFM Encoder fault (CZFM) ⑦ Head Address Register Fault (CZFM)
0D	Write Protect Check	Description : indicates that write operation was attempted during write-protect condition which was enabled by File-protect switch on CZFM or optional front panel. Possible fault: ① Illegal write command from the control unit. ② Mis-operation of the switch. ③ Write Control Logic Fault (CZFM)
0E	Multiple Head Check	Description : indicates that multiple heads or HICs were selected during write operation. Possible fault: ① HIC chip-select driver fault (CZGM) (excluding the specific head group) ② HIC itself fault (Drive) ③ Multiple head detection fault (CZGM)
0F	Emergency on Ready Check	Refer to Code 05/0D
11	RTZ Time-out Check	Description : indicates that RTZ operation was not terminated within 4 seconds. Possible fault: ① Servo control fault (CZGM) ② Seek control logic fault (CZFM) ③ Servo surface malfunction (Drive)

Table 5-3-1 Fault Isolation List (Continued)

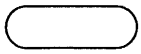
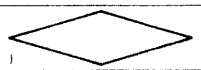
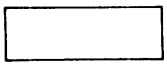
Code	Definition	Description
12	Seek Time-out Check	Description : indicates that seek operation was not terminated within 67ms. Possible fault: ① Servo control fault (CZGM) ② Seek control logic fault (CZFM) ③ Servo surface malfunction (Drive)
13	Over-shoot Check	Description : indicates that the head over-shoot on to the unspecified new cylinder. Possible fault: ① Servo control fault including adjustment (CZGM) ② Actuator auto-lock fault (Drive) ③ DC Voltage too high or low (Power Supply) ④ Servo surface malfunction (Drive) ⑤ Position sensing fault (CZGM) ⑥ Seek control logic fault (CZFM)
14	Seek Guard Band Check	Description : indicates that any Guard Band patterns were detected during seek operation. Possible fault: ① Servo control fault including adjustment (CZGM) ② Position sensing fault (CZGM) ③ Servo surface malfunction (Drive) ④ Seek control logic fault (CZFM)
15	Linear Mode Guard Band Check	Description : indicates that any Guard Band patterns were detected during linear mode (track following). Possible fault: ① Servo control fault including adjustment (CZGM) ② Position sensing fault (CZGM) ③ Servo surface malfunction (Drive) ④ Seek control logic fault (CZFM)
16	RTZ Outer Guard Band Check	Description : indicates that Outer Guard Band Patterns were detected during RTZ operation. Possible fault: ① Servo control fault (CZGM) ② Seek control logic fault (CZFM)
17	Illegal Cylinder Check	Description : indicates that illegal cylinder address (CAR >822) were set on the drive. Possible fault: ① Illegal command from the control unit. ② Cylinder address register fault (CZFM) ③ Line receiver fault (CZFM)

5.4 TROUBLESHOOTING SYMBOL

The troubleshooting flow charts contain the procedures beginning with an error status, to pursue trouble sources.

The following conventions are provided to aid understanding the symbols used in this trouble shooting flow charts as shown in Table 5-4-1.

Table 5-4-1 Symbol of Flow Chart

Symbol	Description
	Terminals. Starting point of the trouble.
	Decision, go ahead according with YES or NO. (Reference test point.) ○: possible fault (Refer to 5.3)
	Connector, go ahead same-numbered symbol in same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process, perform activity given.

5.5 TROUBLESHOOTING FLOW CHART

In this paragraph, the following flow charts are provided.

Figure 5-5-1 Alarm
Figure 5-5-2 Not Selected
Figure 5-5-3 Not Power Ready
Figure 5-5-4 Power-up Sequence Check
Figure 5-5-5 Device Check
Figure 5-5-6 Seek Error
Figure 5-5-7 Read Error
Figure 5-5 8 AM Missing
Figure 5-5-9 Dual Channel

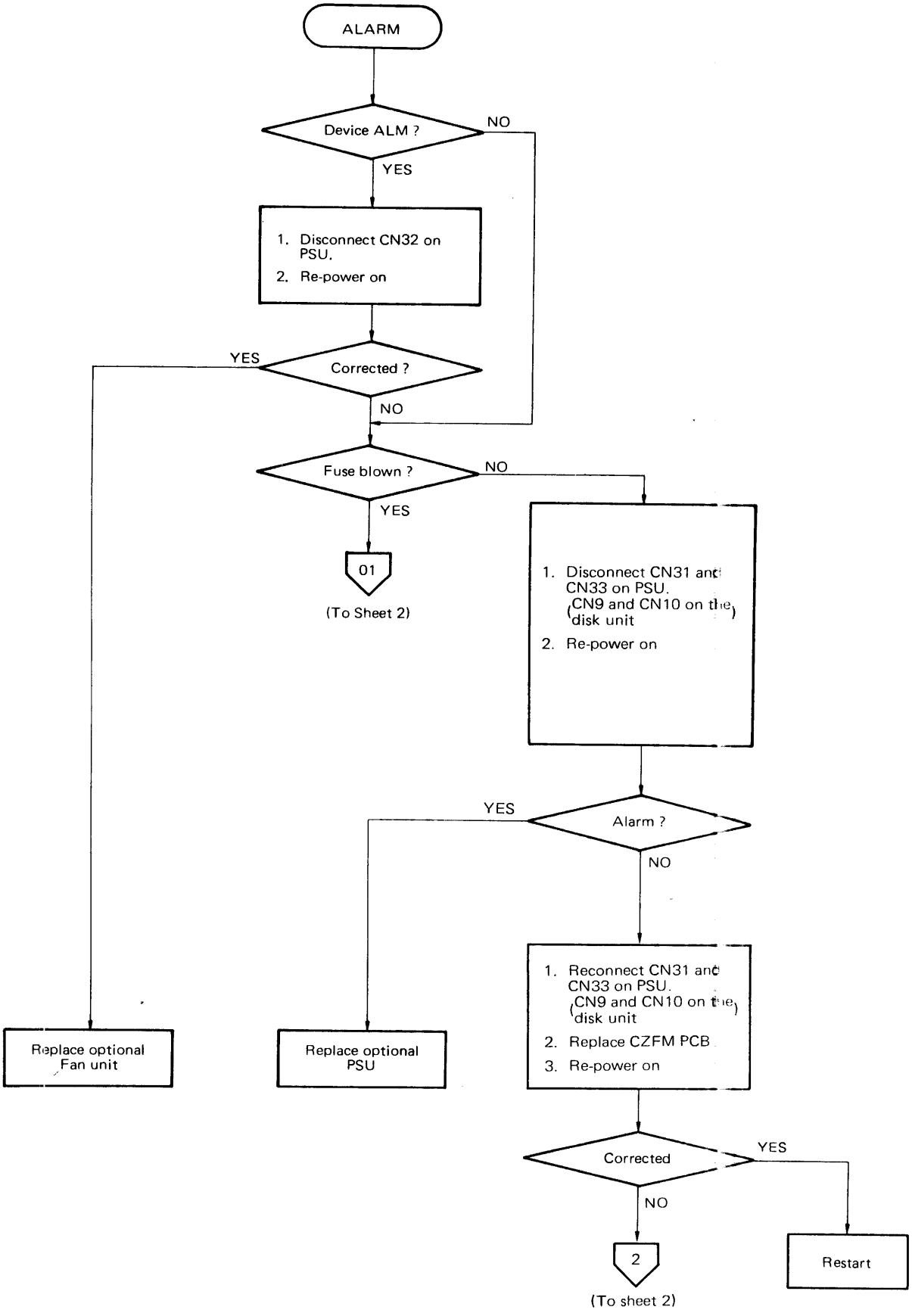


Figure 5-5-1 Alarm Flow Chart (Sheet 1 of 2)

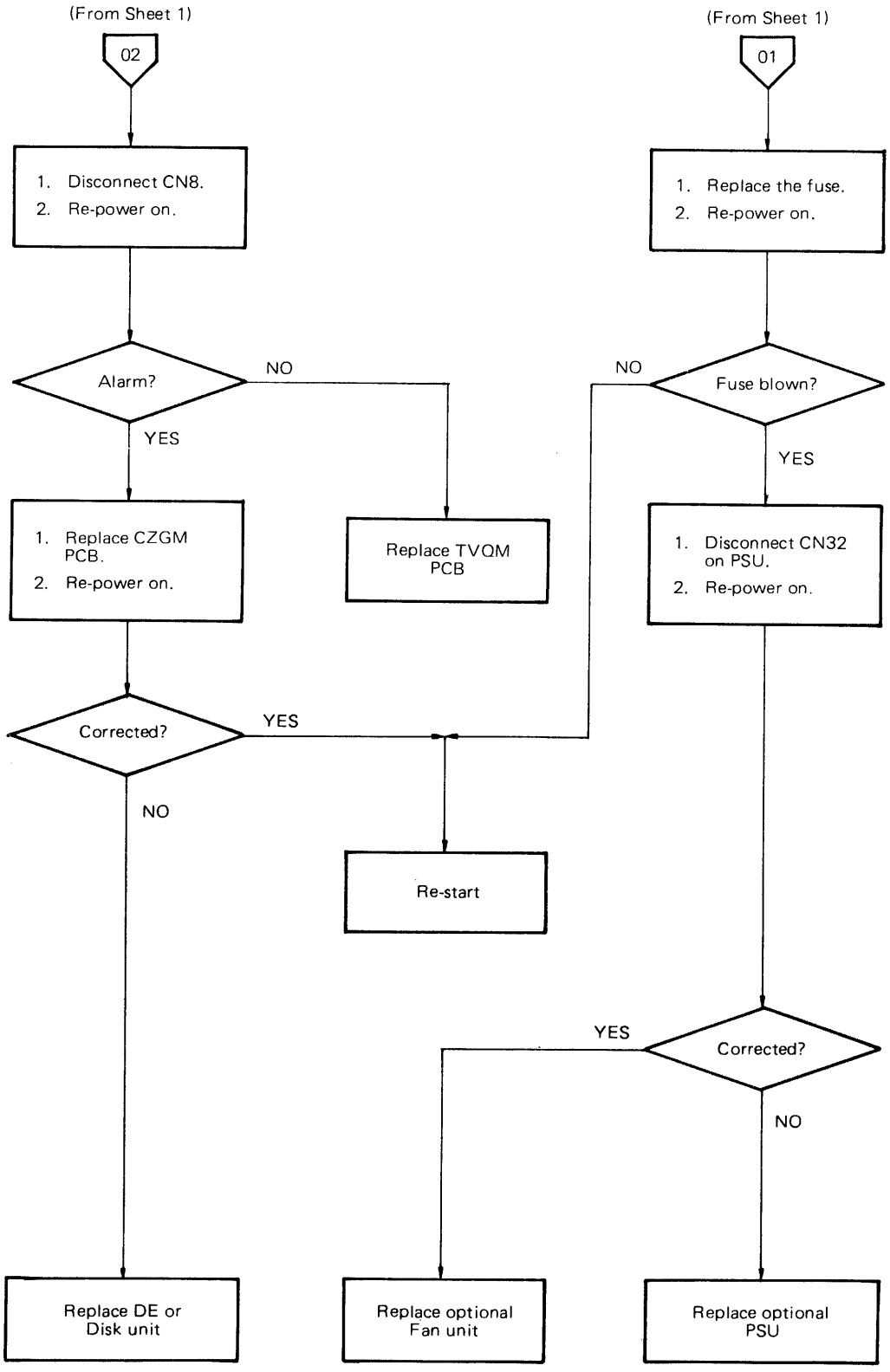


Figure 5-5-1 Alarm Flow Chart (Sheet 2 of 2)

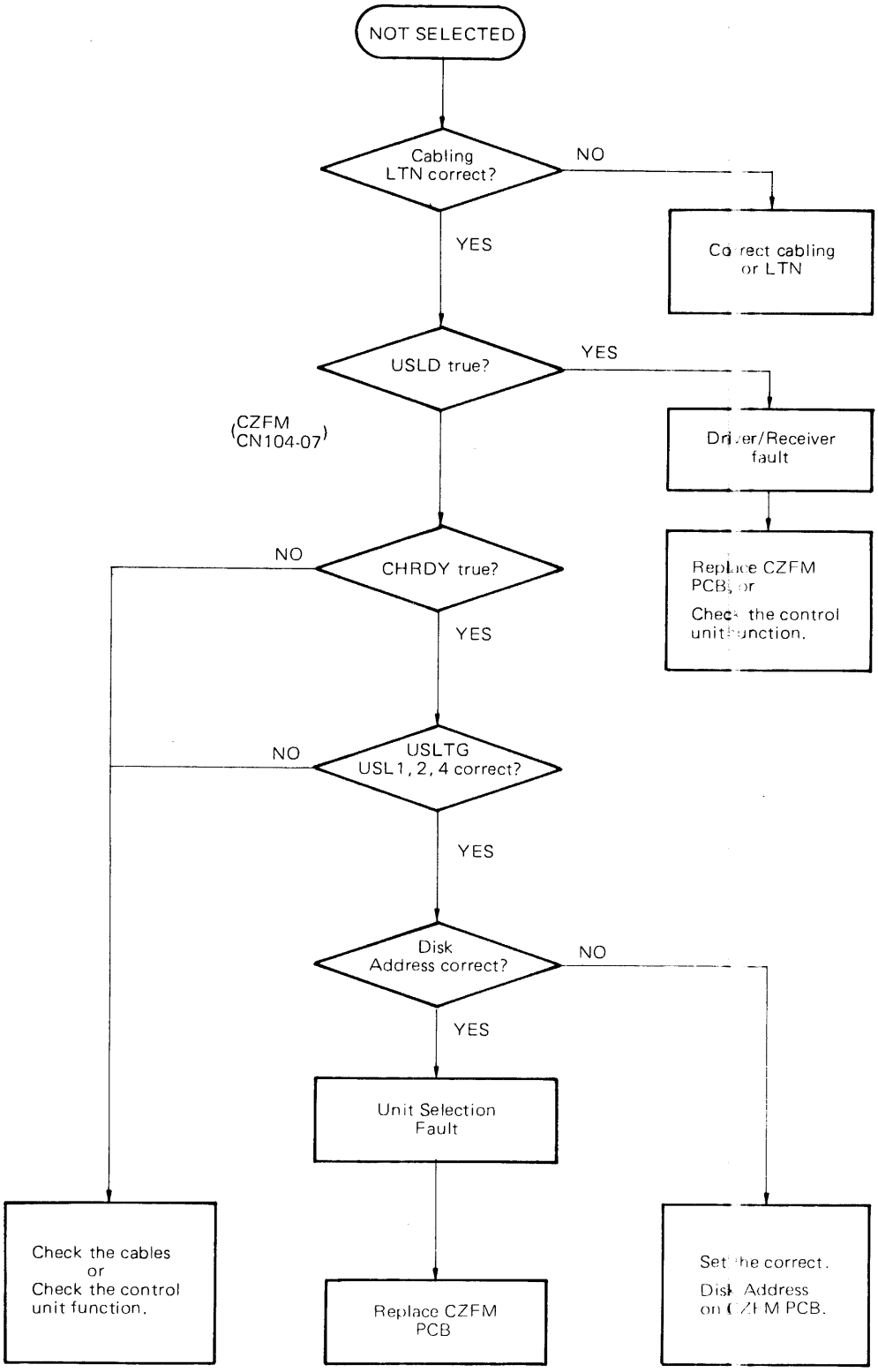


Figure 5-5-2 Not Selected Flow Chart

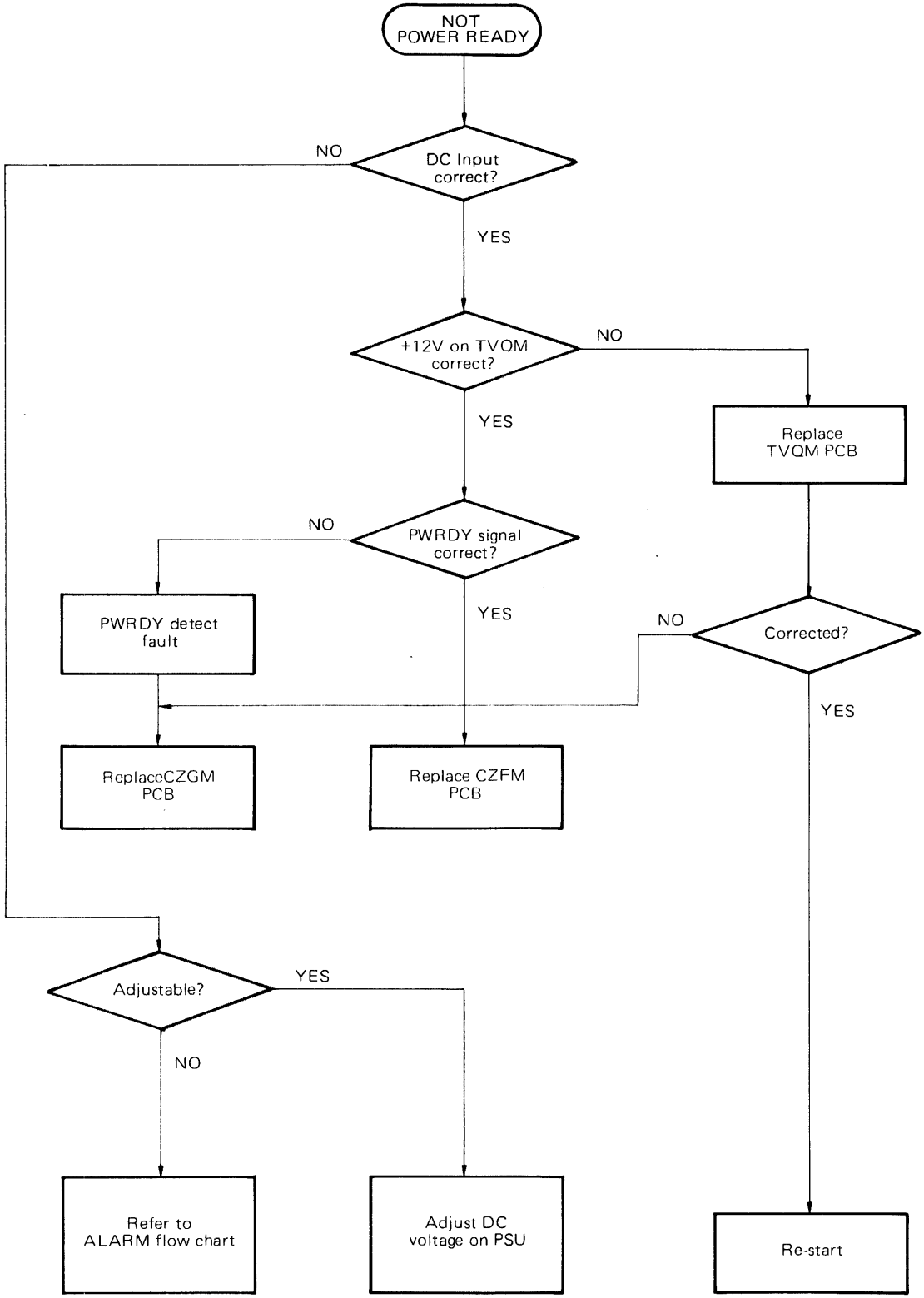


Figure 5-5-3 Not Power Ready Flow Chart

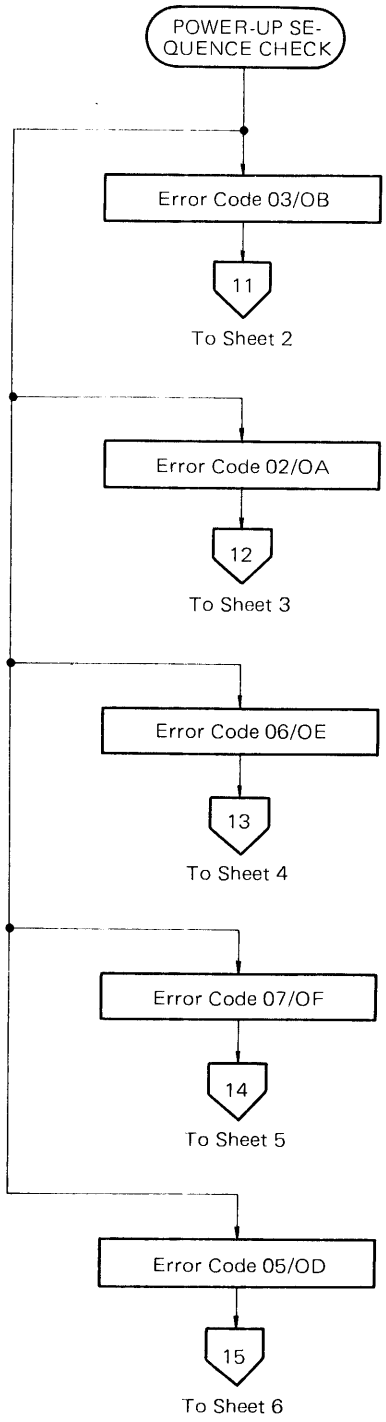


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 1 of 6)

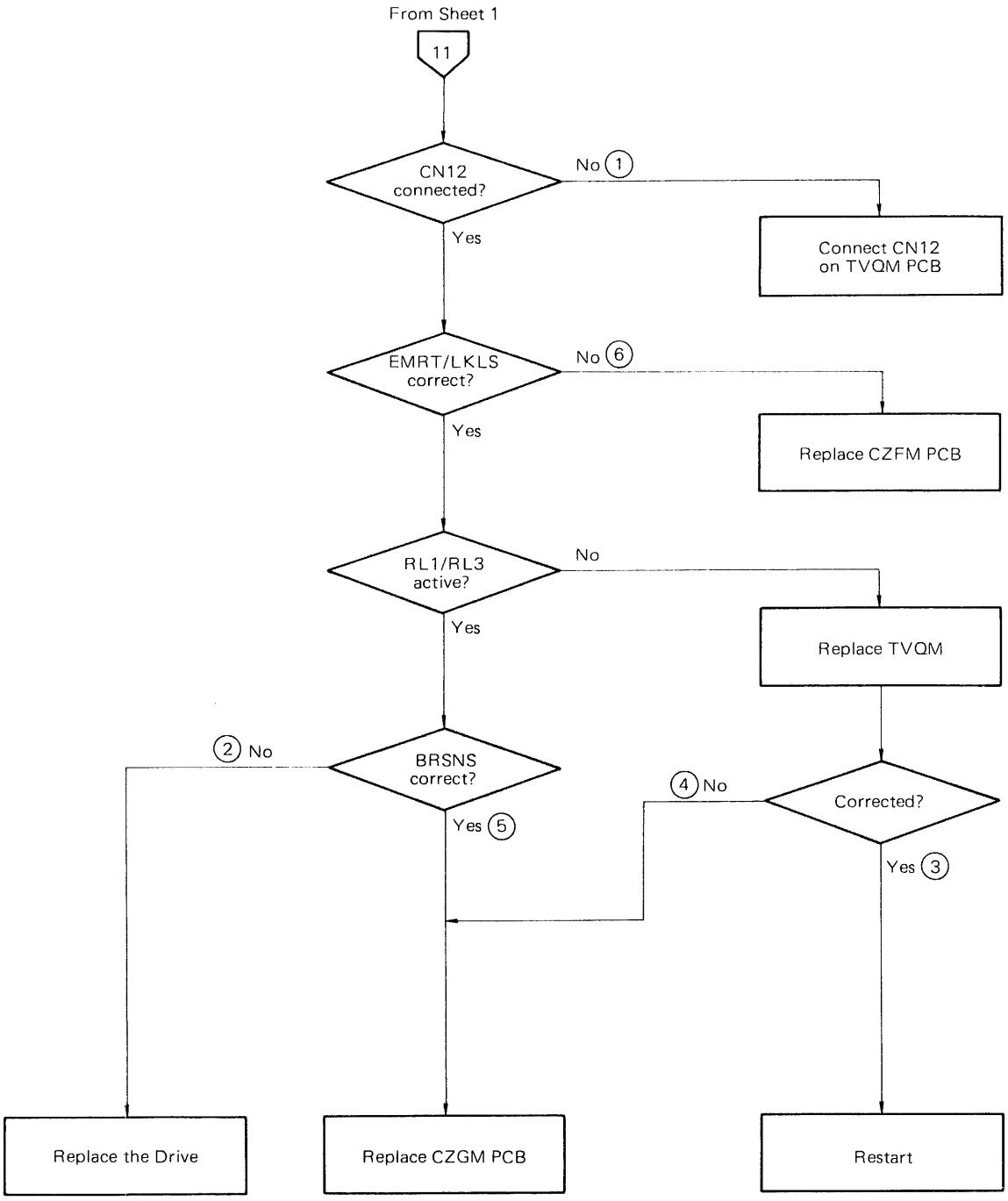


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 2 of 6)

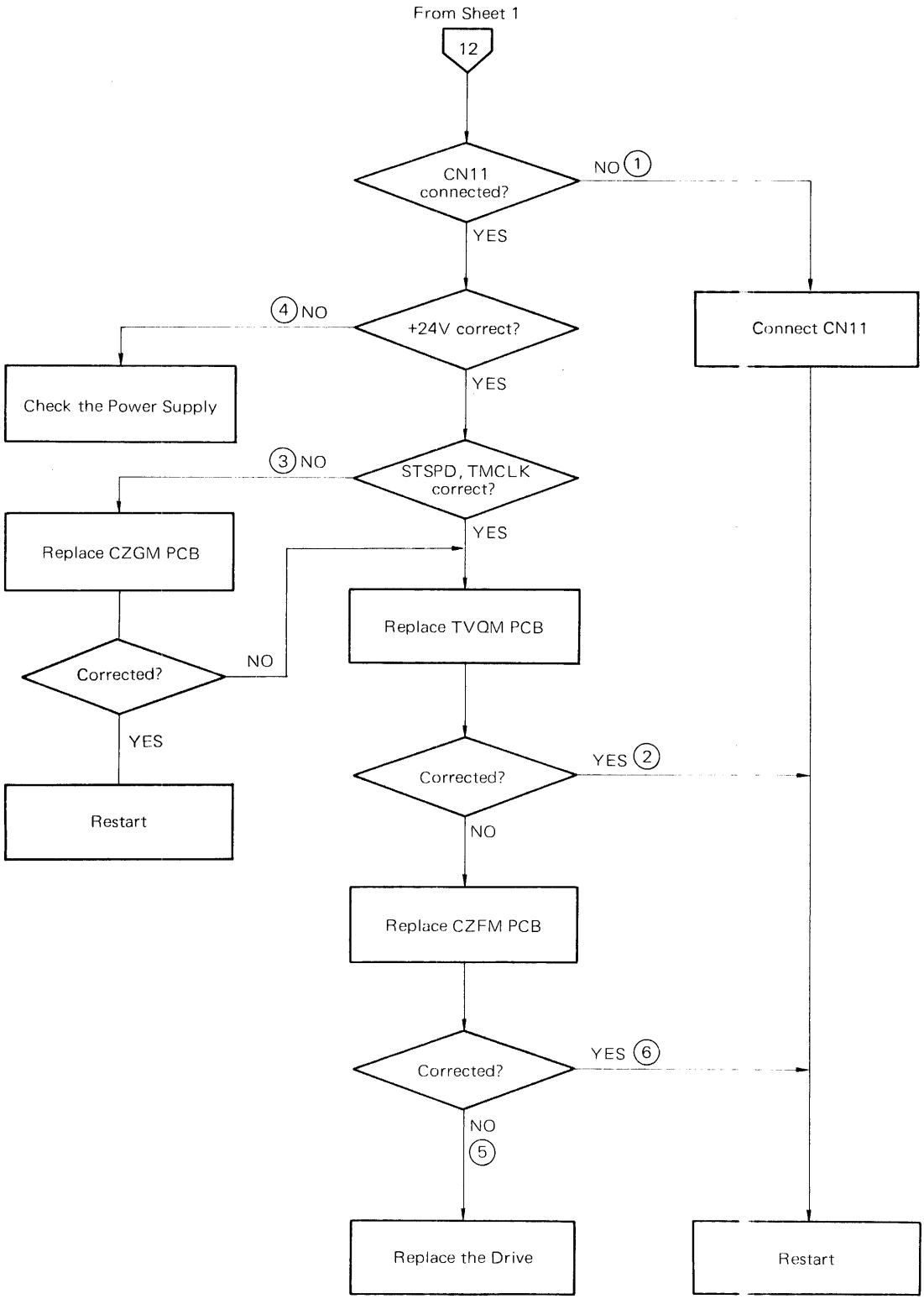


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 3 of 6)

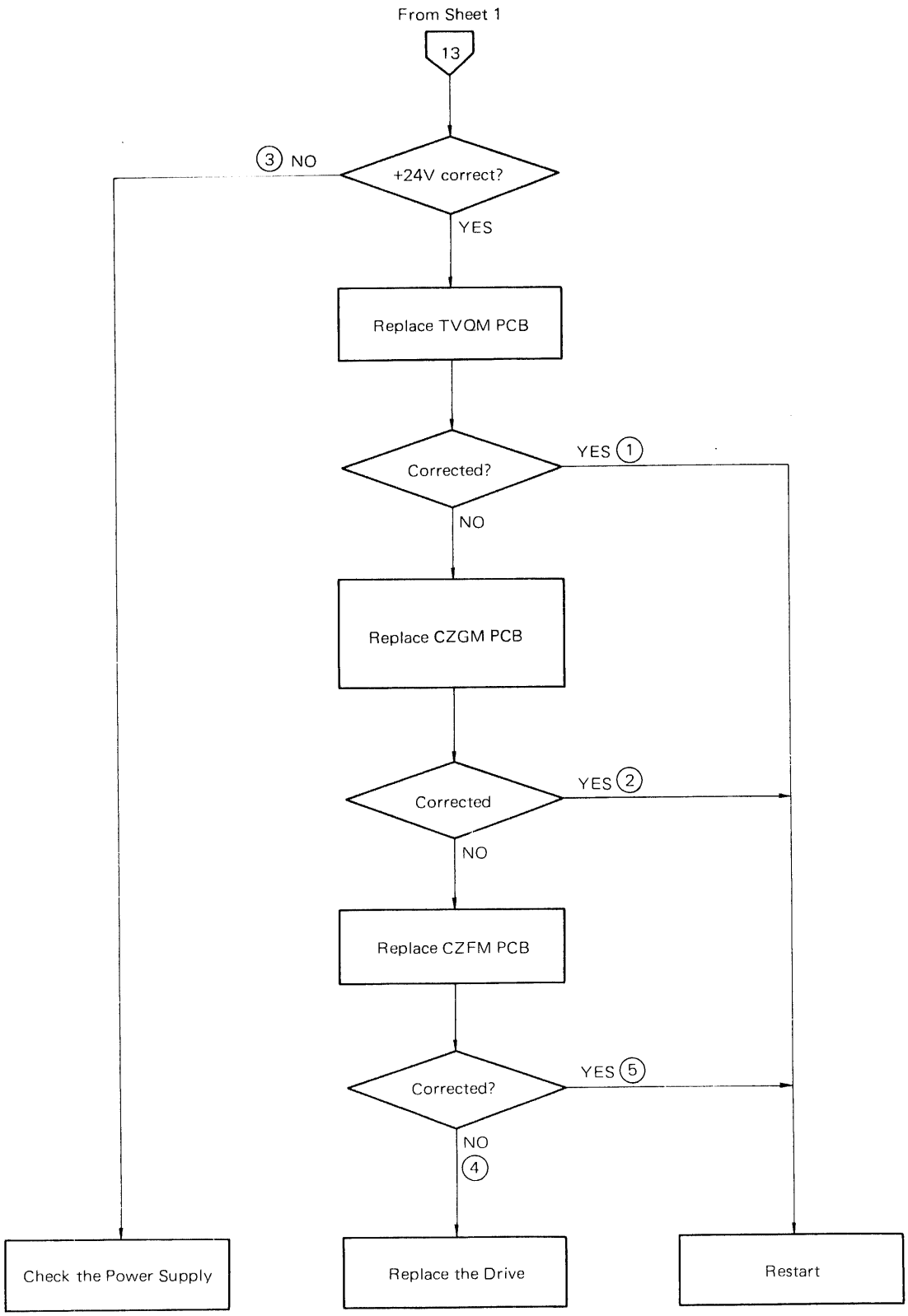


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 4 of 6)

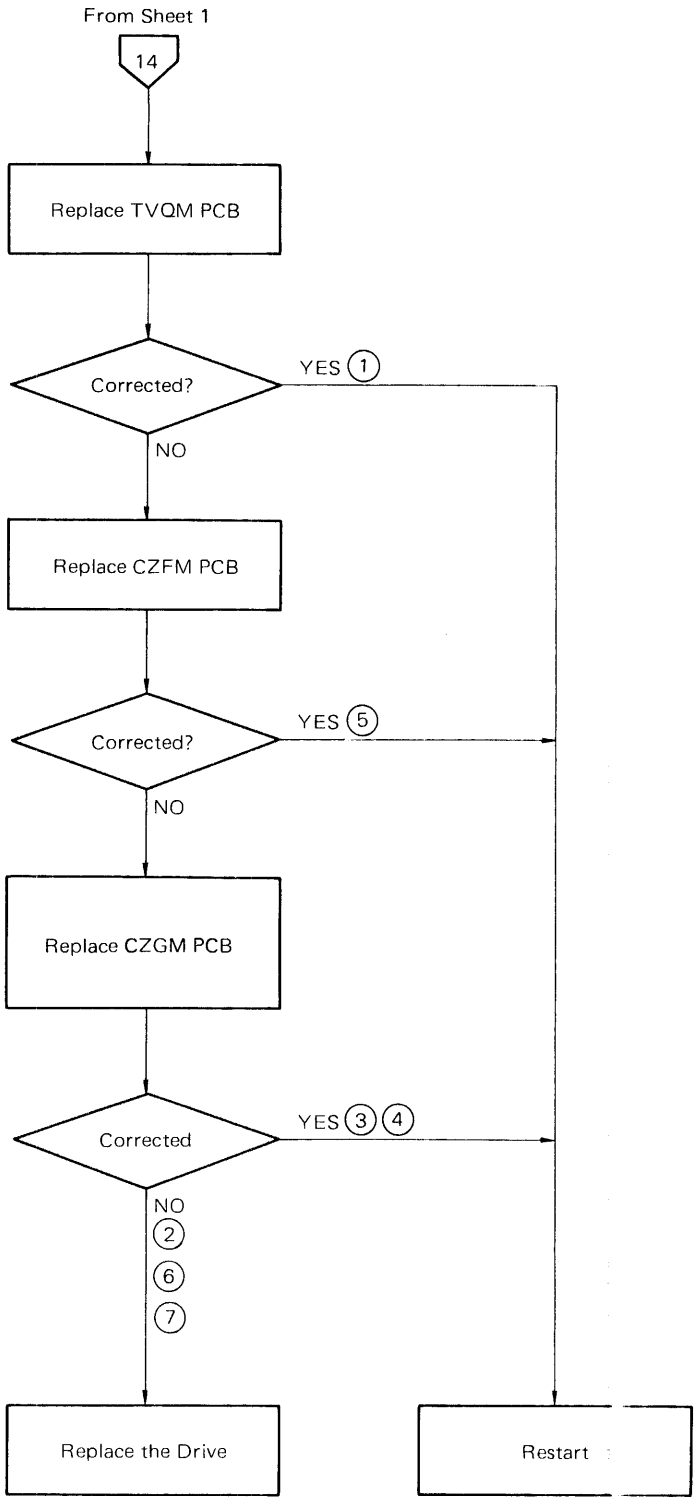


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 5 of 6)

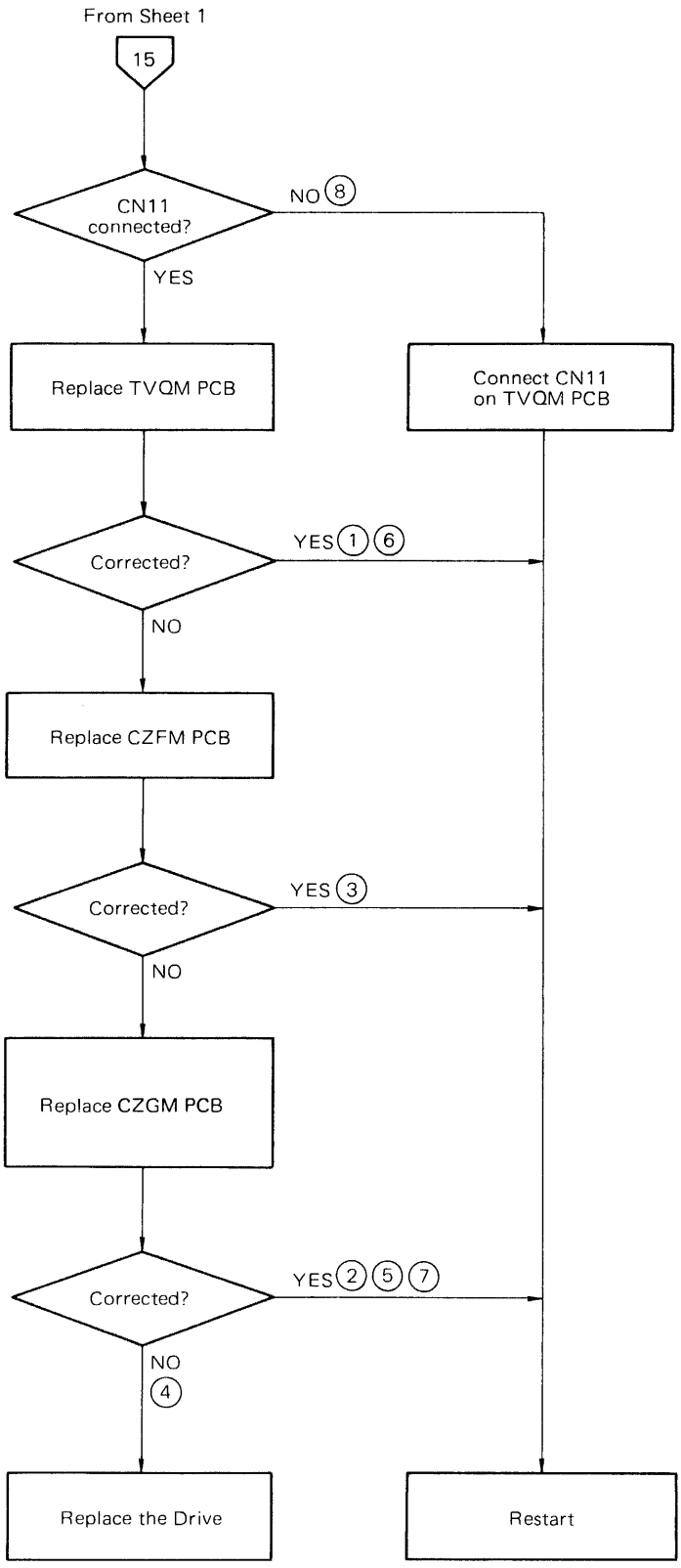


Figure 5-5-4 Power-up Sequence Check Flow Chart (Sheet 6 of 6)

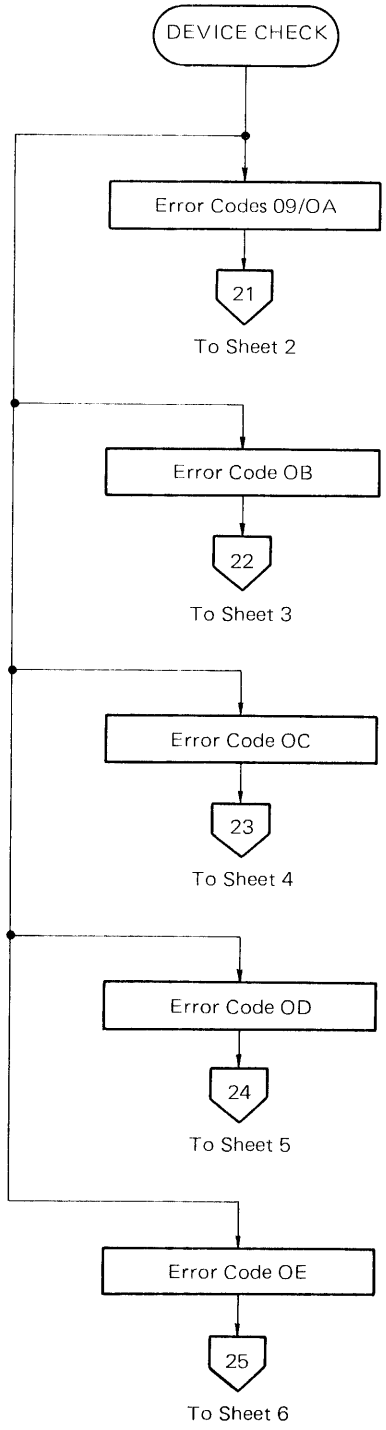


Figure 5-5-5 Device Check Flow Chart (Sheet 1 of 6)

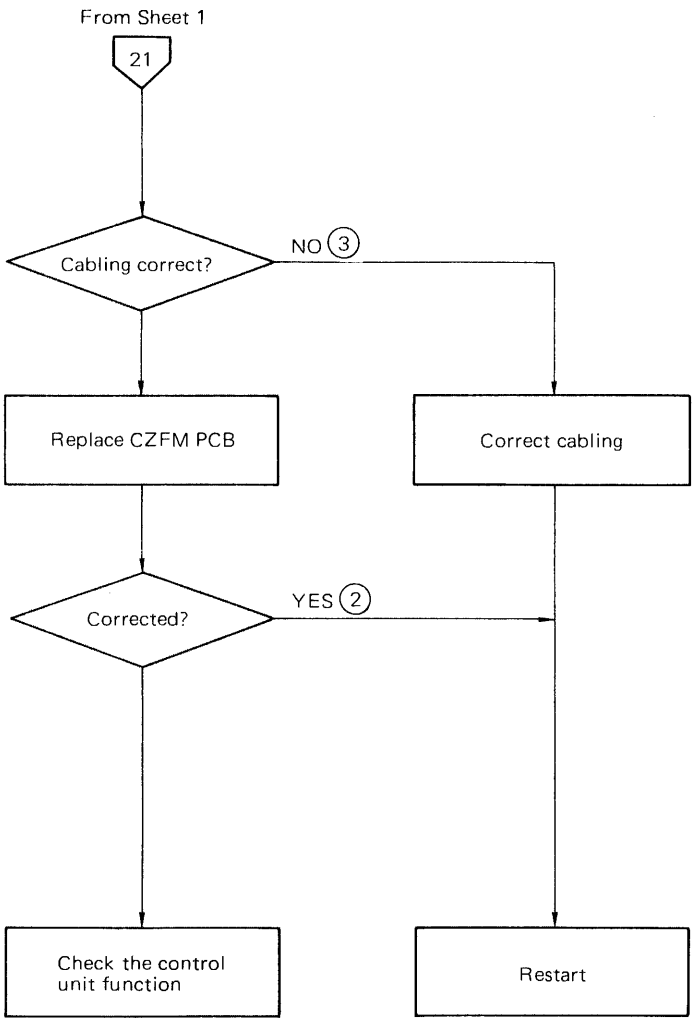


Figure 5-5-5 Device Check Flow Chart (Sheet 2 of 6)

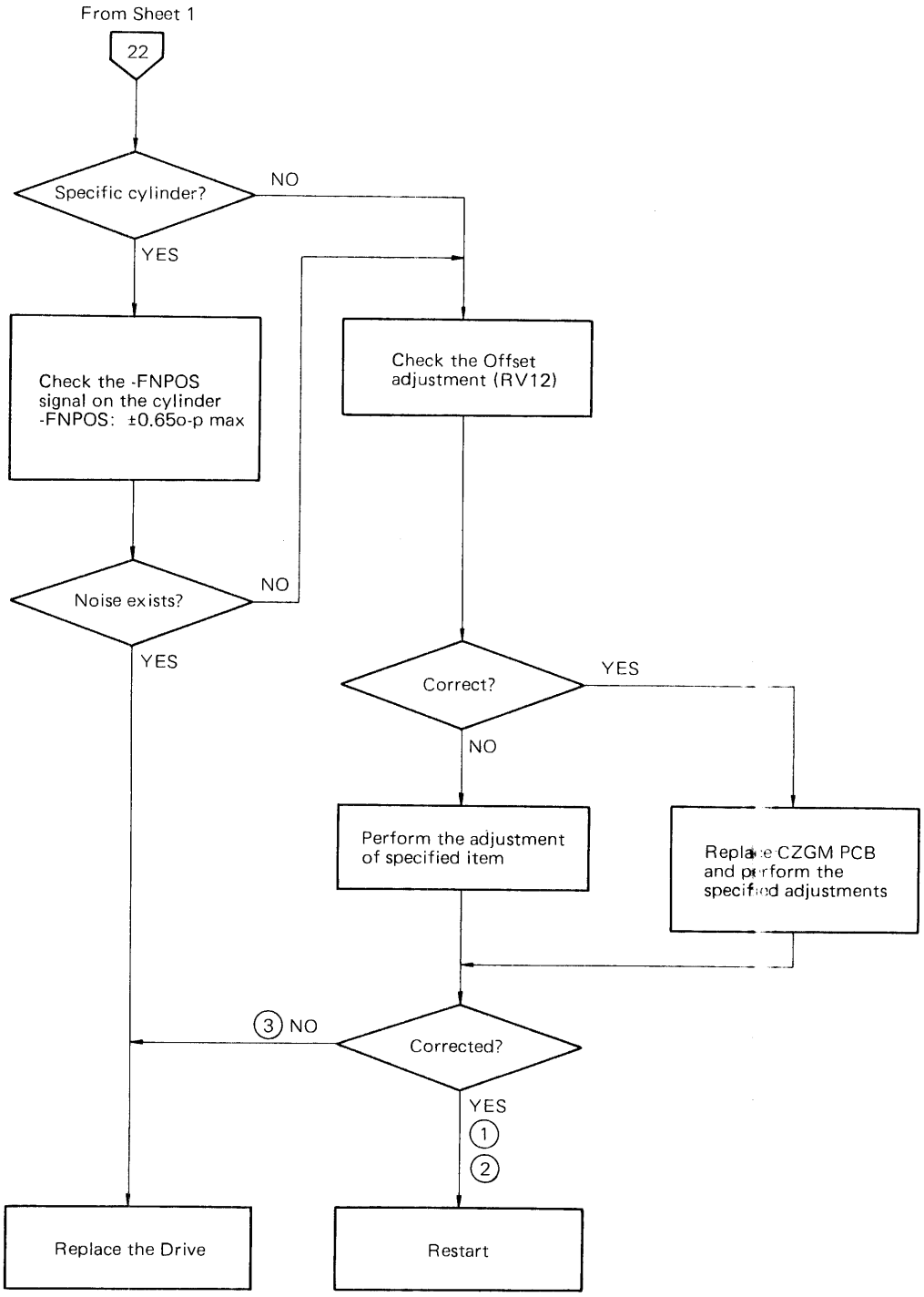


Figure 5-5-5 Device Check Flow Chart (Sheet 3 of 6)

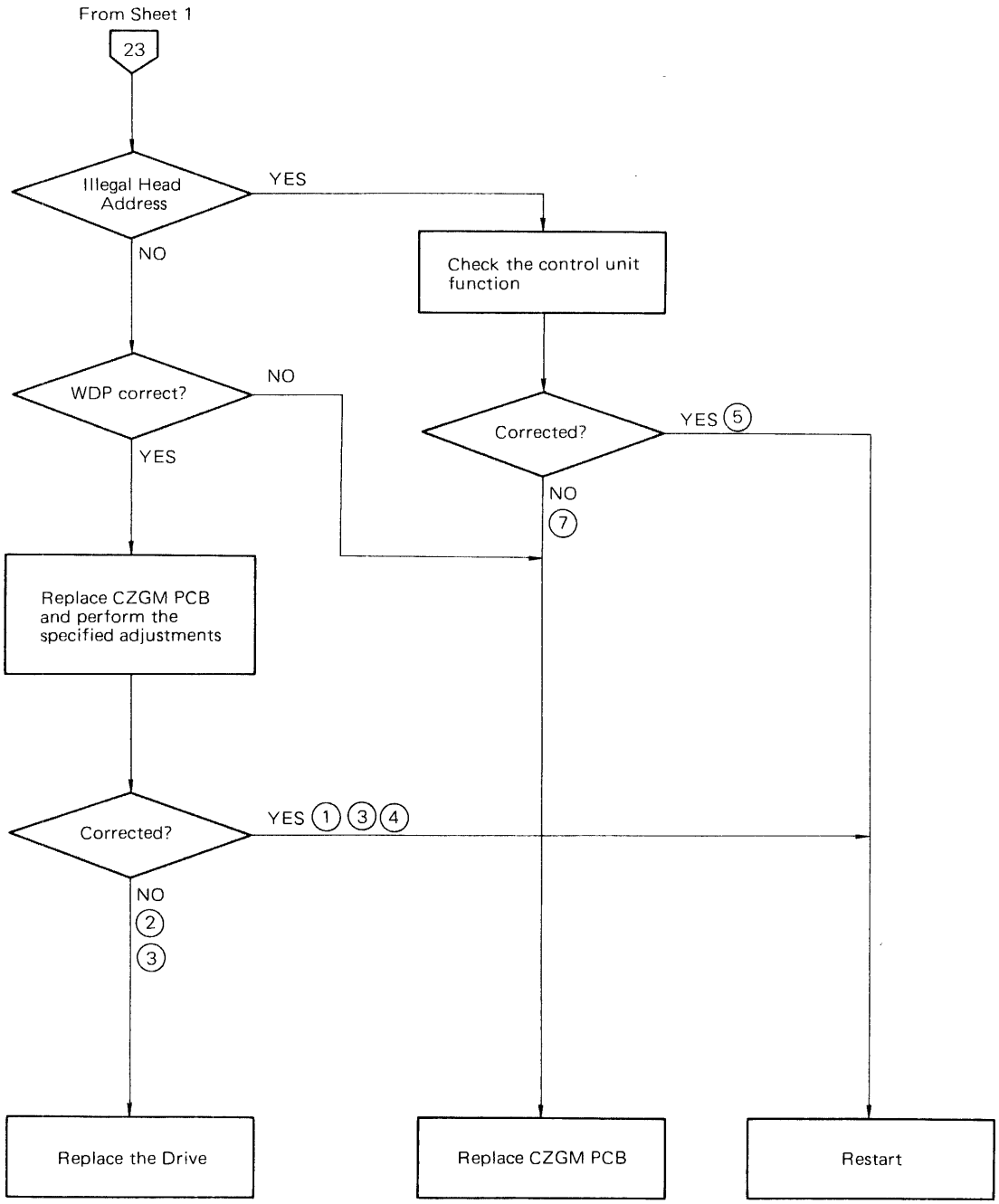
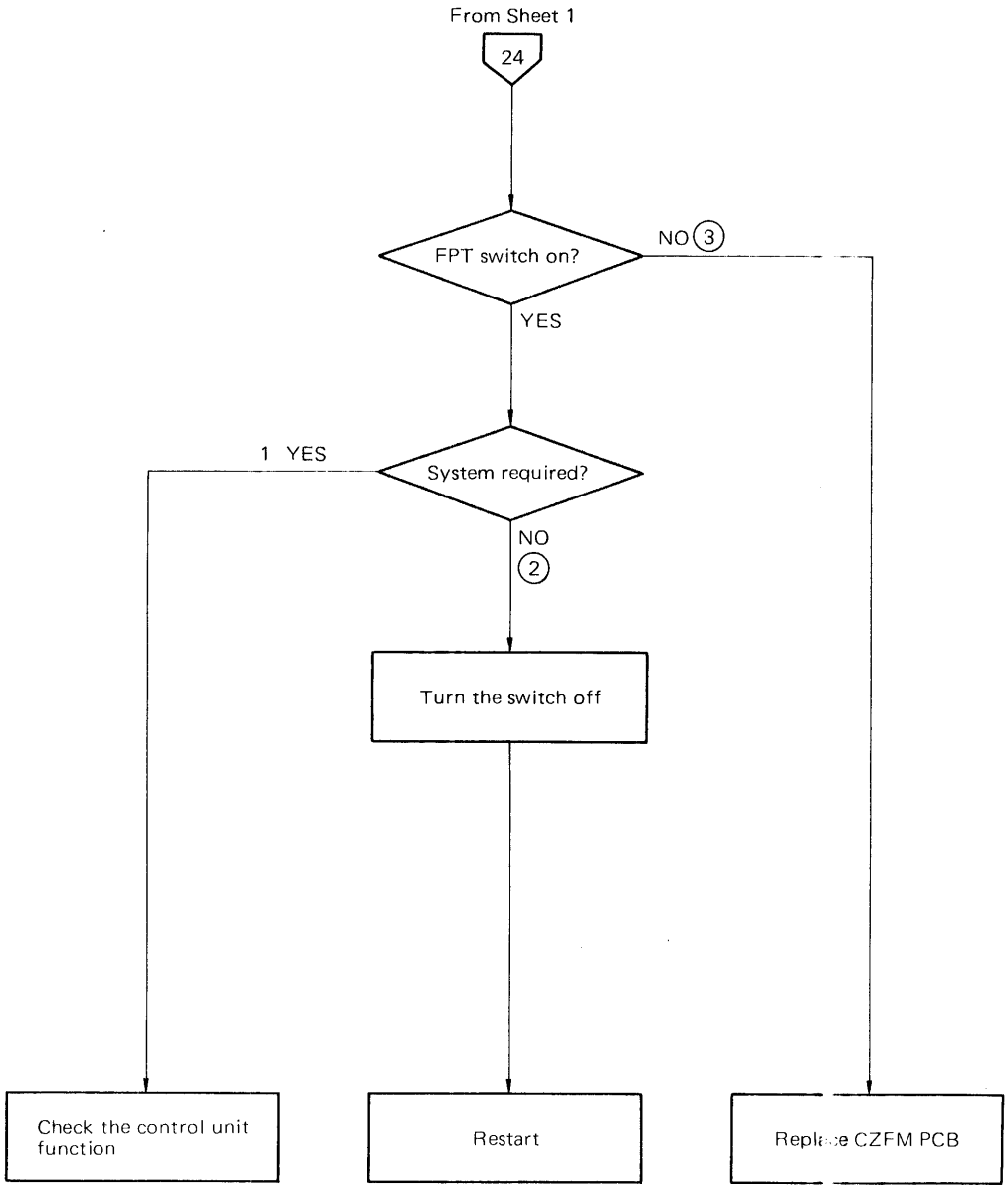


Figure 5-5-5 Device Check Flow Chart (Sheet 4 of 6)



Note) FPT (File Protect) switches are located on CZFM PCB assembly (SW1-Key 7) and an optional operator panel.

Figure 5-5-5 Device Check Flow Chart (Sheet 5 of 6)

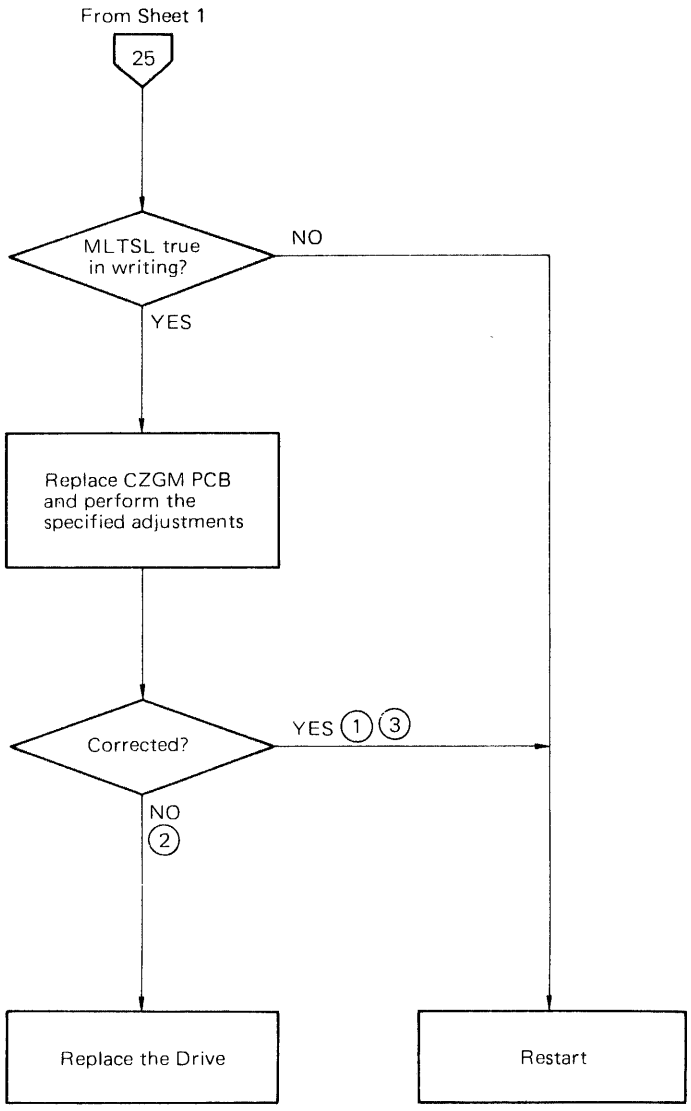


Figure 5-5-5 Device Check Flow Chart (Sheet 6 of 6)

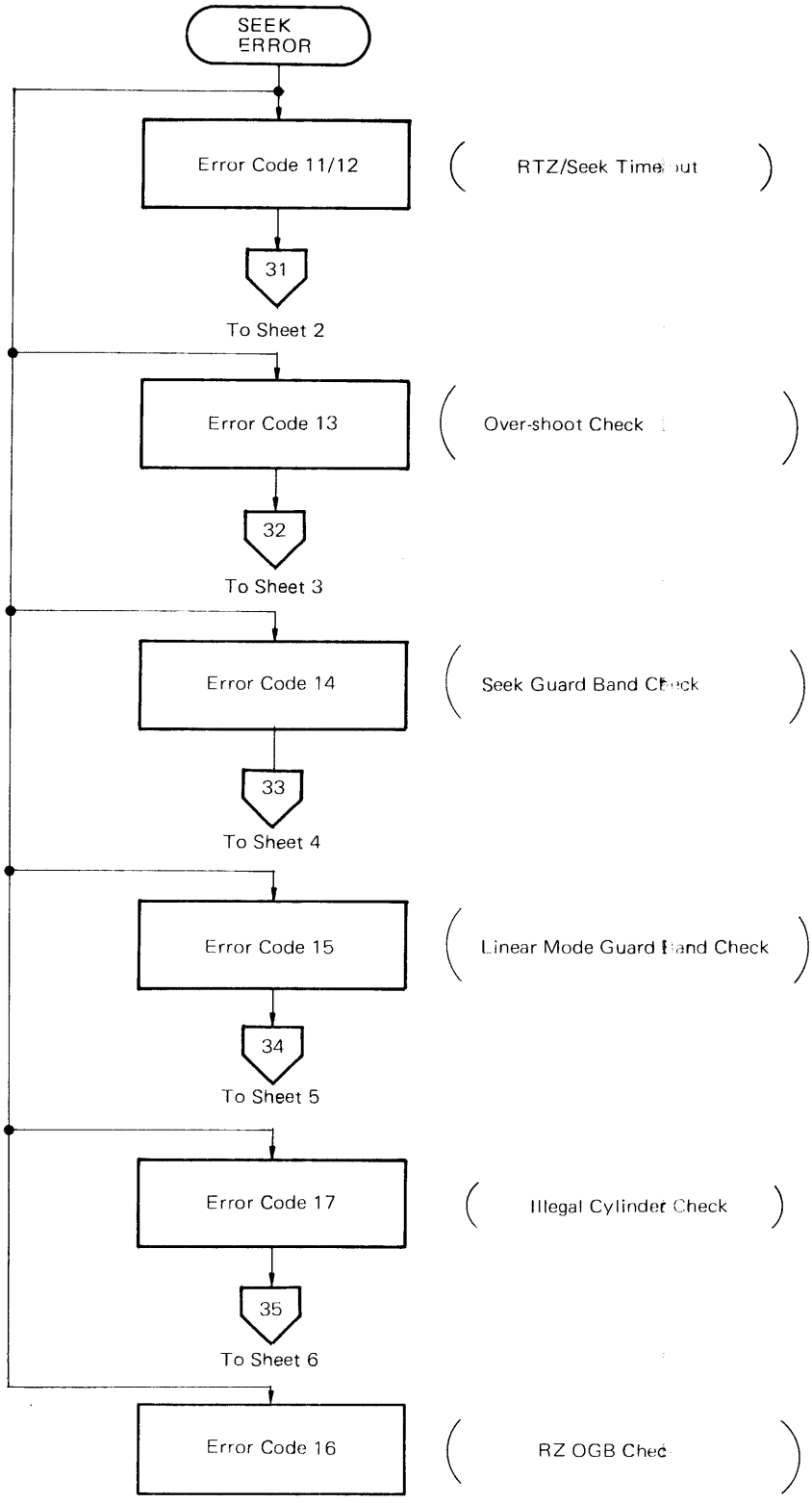


Figure 5-5-6 Seek Error Flow Chart (Sheet 1 of 6)

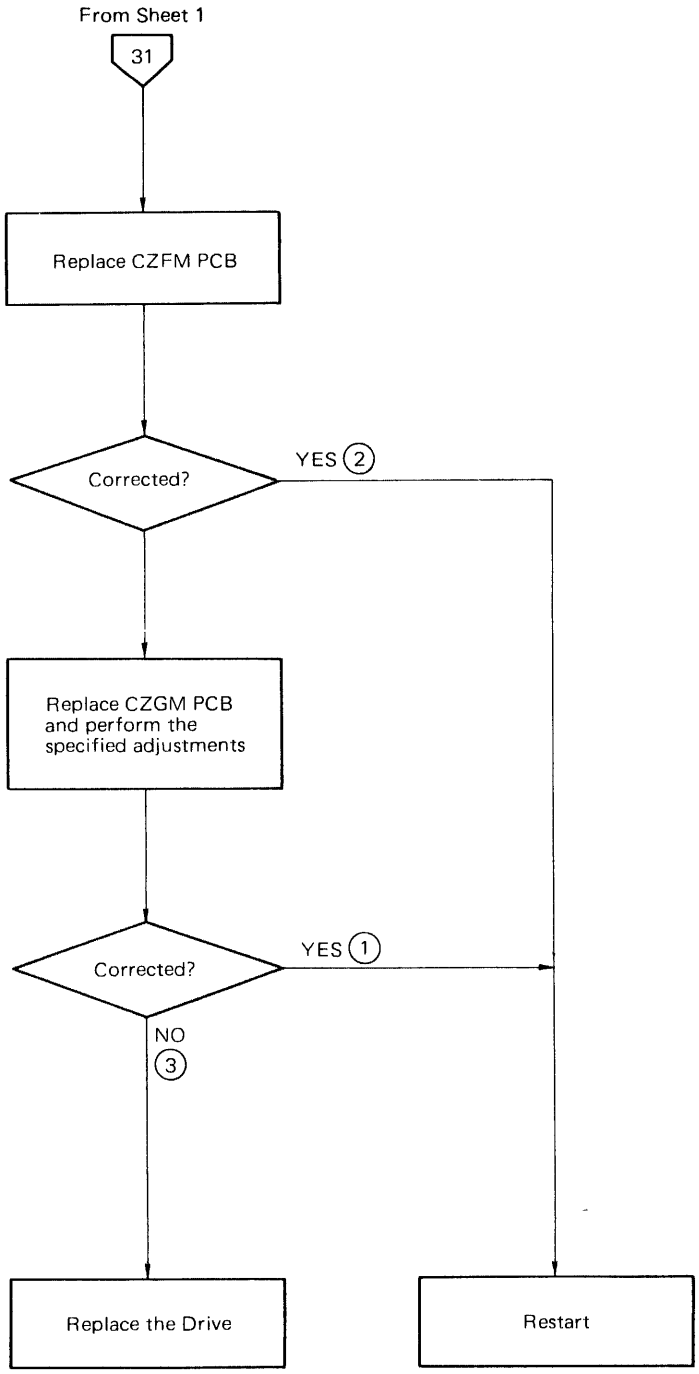


Figure 5-5-6 Seek Error Flow Chart (Sheet 2 of 6)

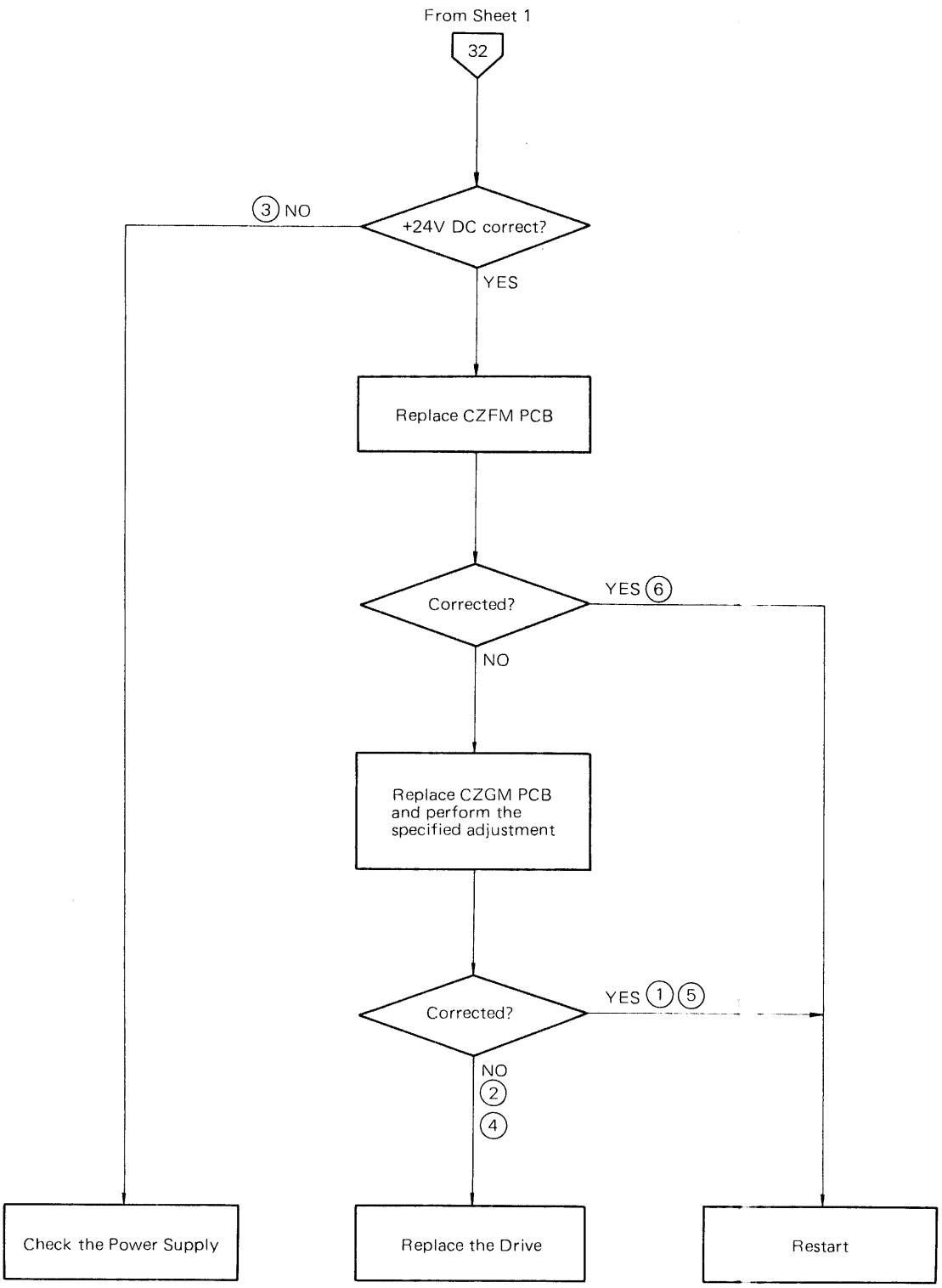


Figure 5-5-6 Seek Error Flow Chart (Sheet 3 of 6)

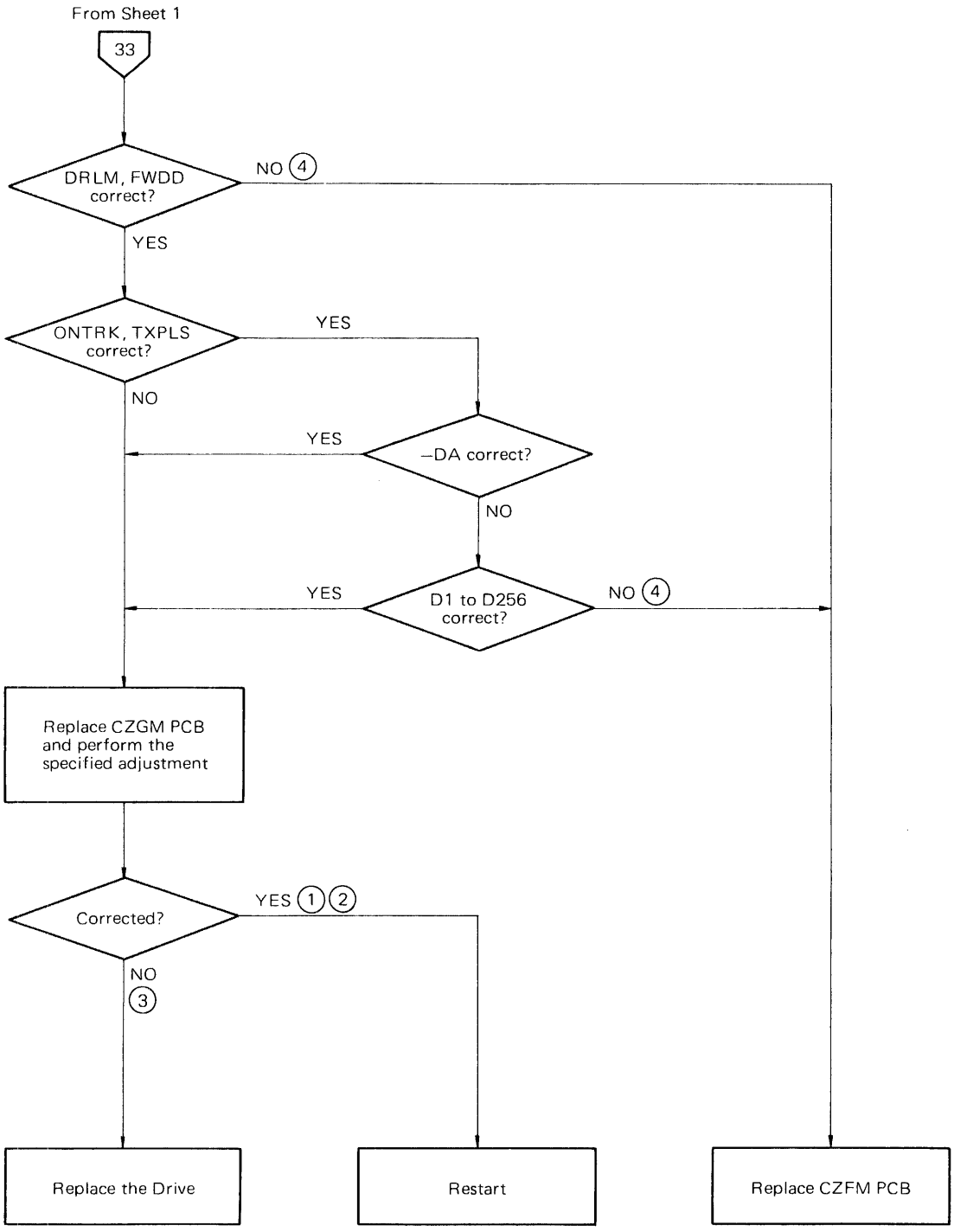


Figure 5-5-6 Seek Error Flow Chart (Sheet 4 of 6)

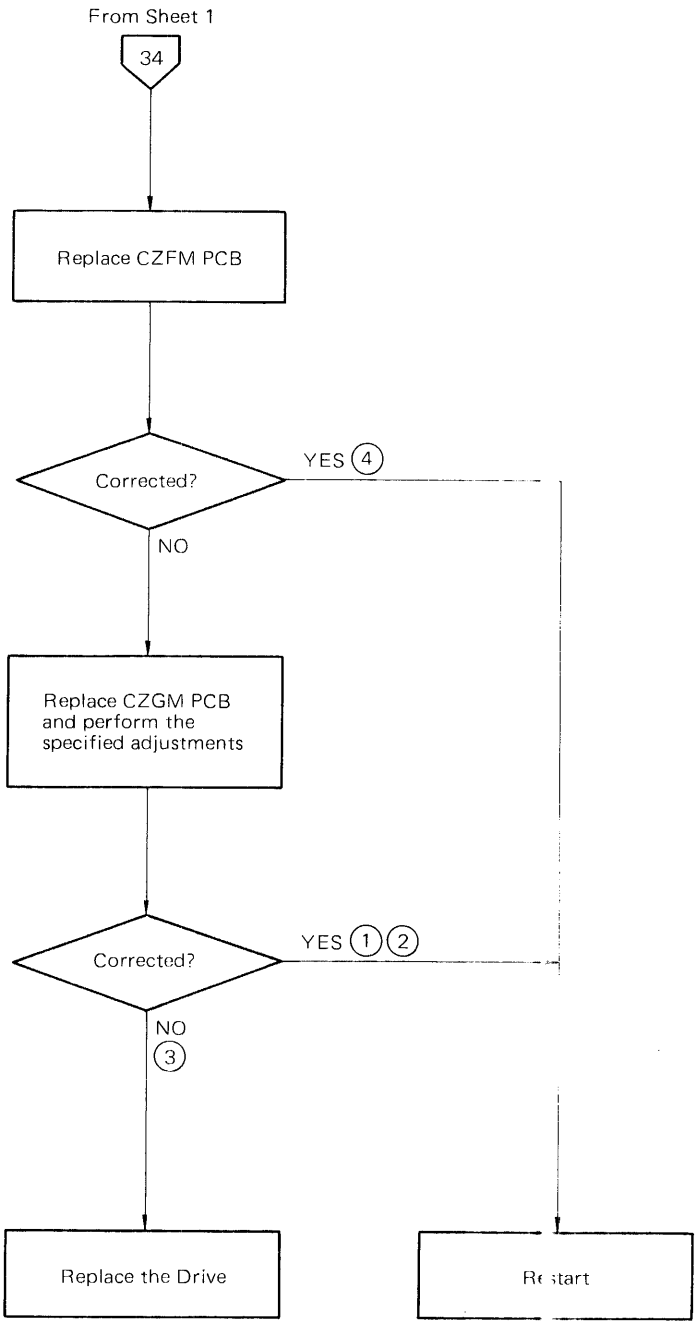


Figure 5-5-6 Seek Error Flow Chart (Sheet 5 of 6)

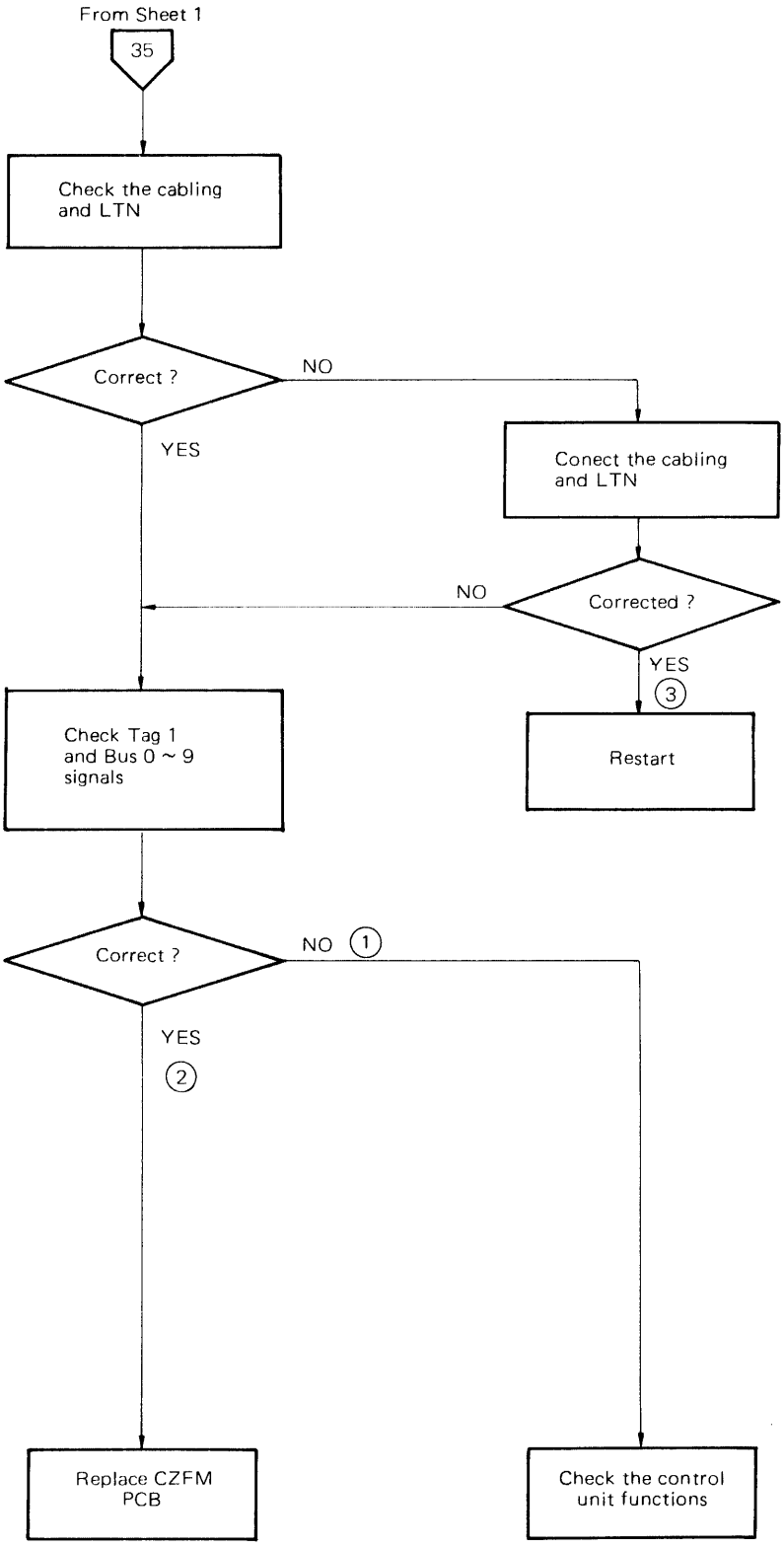
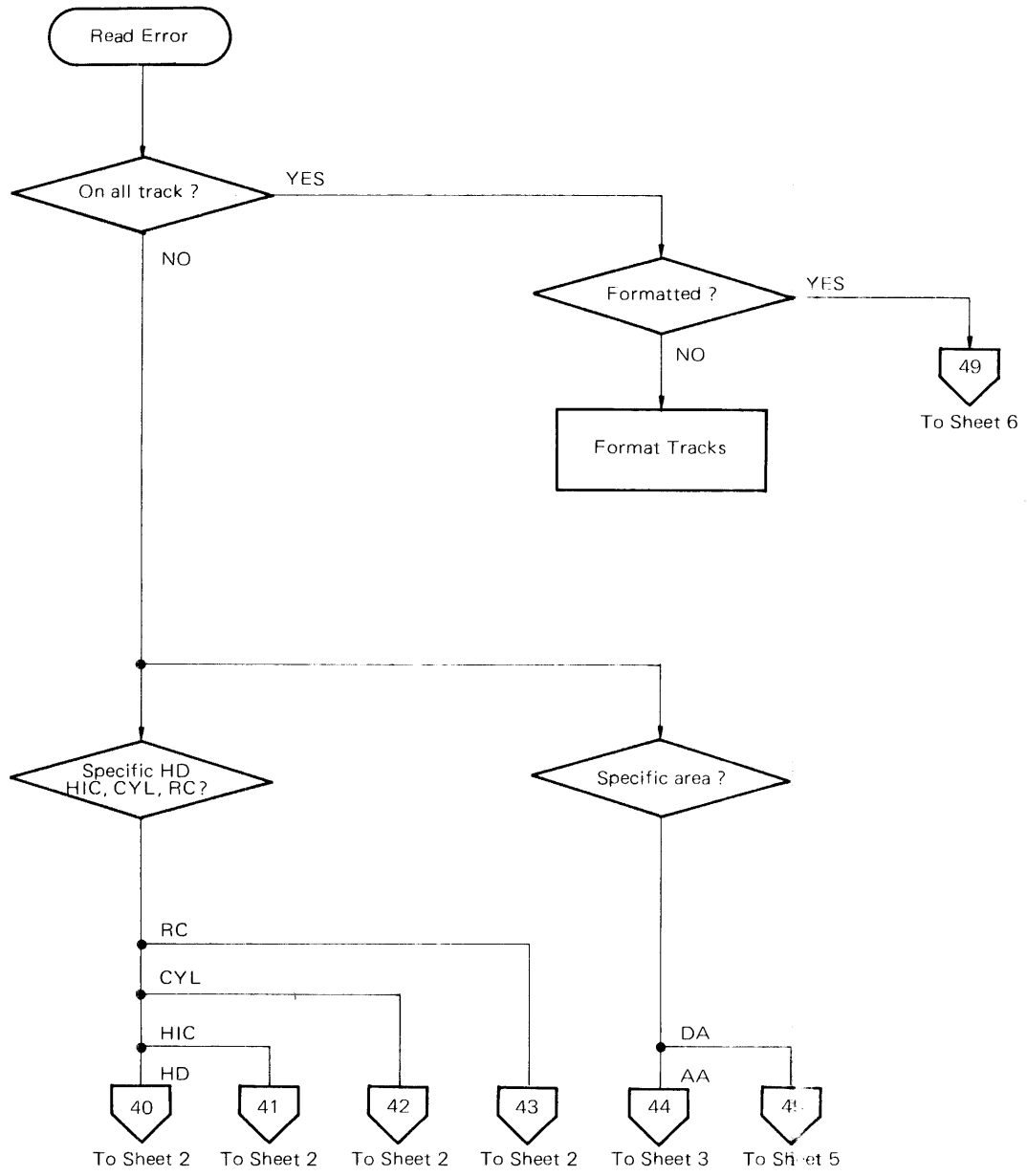
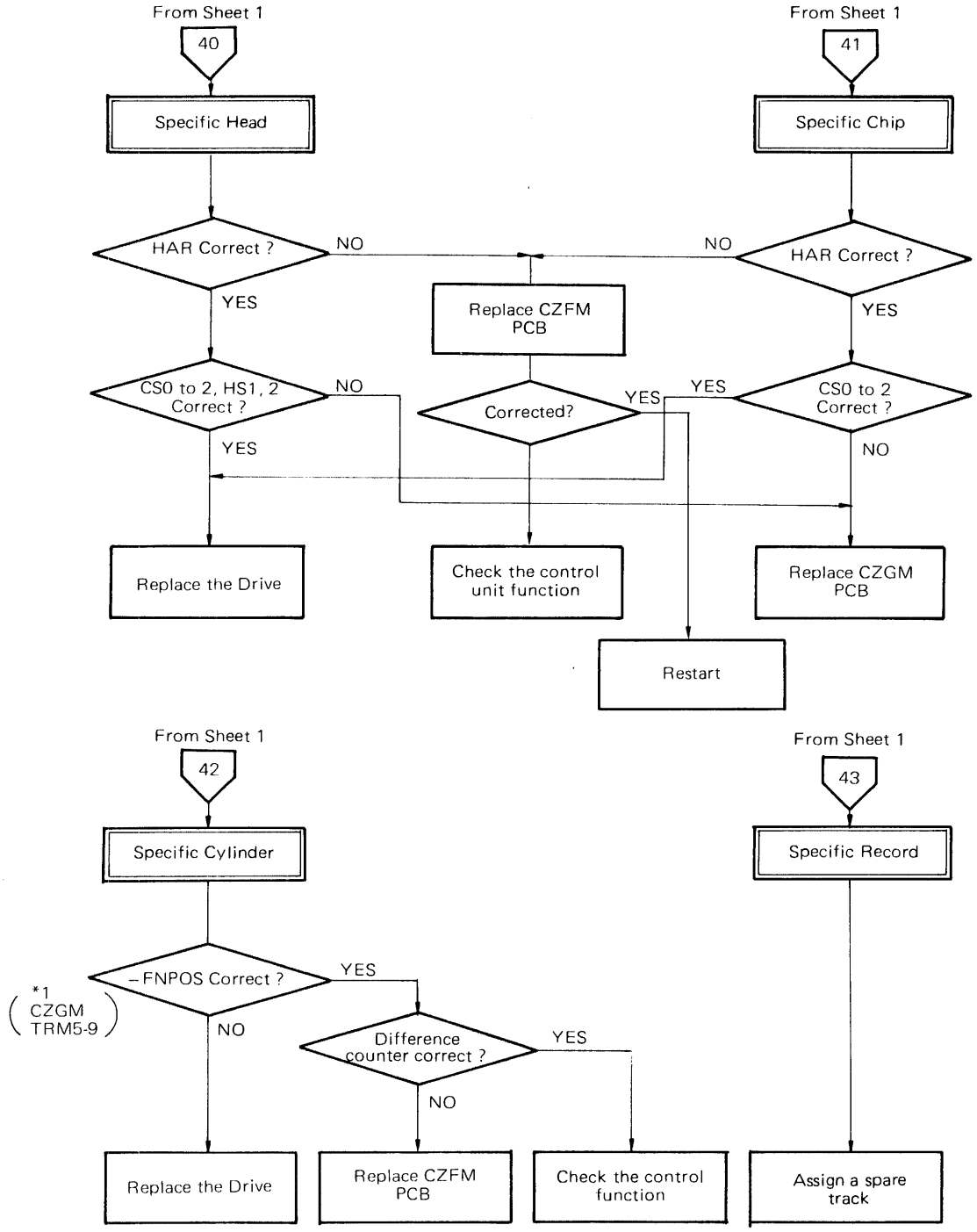


Figure 5-5-6 Seek Error Flow Chart (Sheet 6 of 6)



Note: 1) AA is Address Area
2) DA is Data Area.

Figure 5-5-7 Read Error Flow Chart (Sheet 1 of 6)



Note: 1) If the noise exceeding 1.0Vo-p appears on –FNPOS signal during Linear Mode, it is incorrect.

2) One HIC chip has four/two heads.
CS0: HD0 to 3
CS1: HD4 to 7
CS2: HD8 and 9

Figure 5-5-7 Read Error Flow Chart (Sheet 2 of 6)

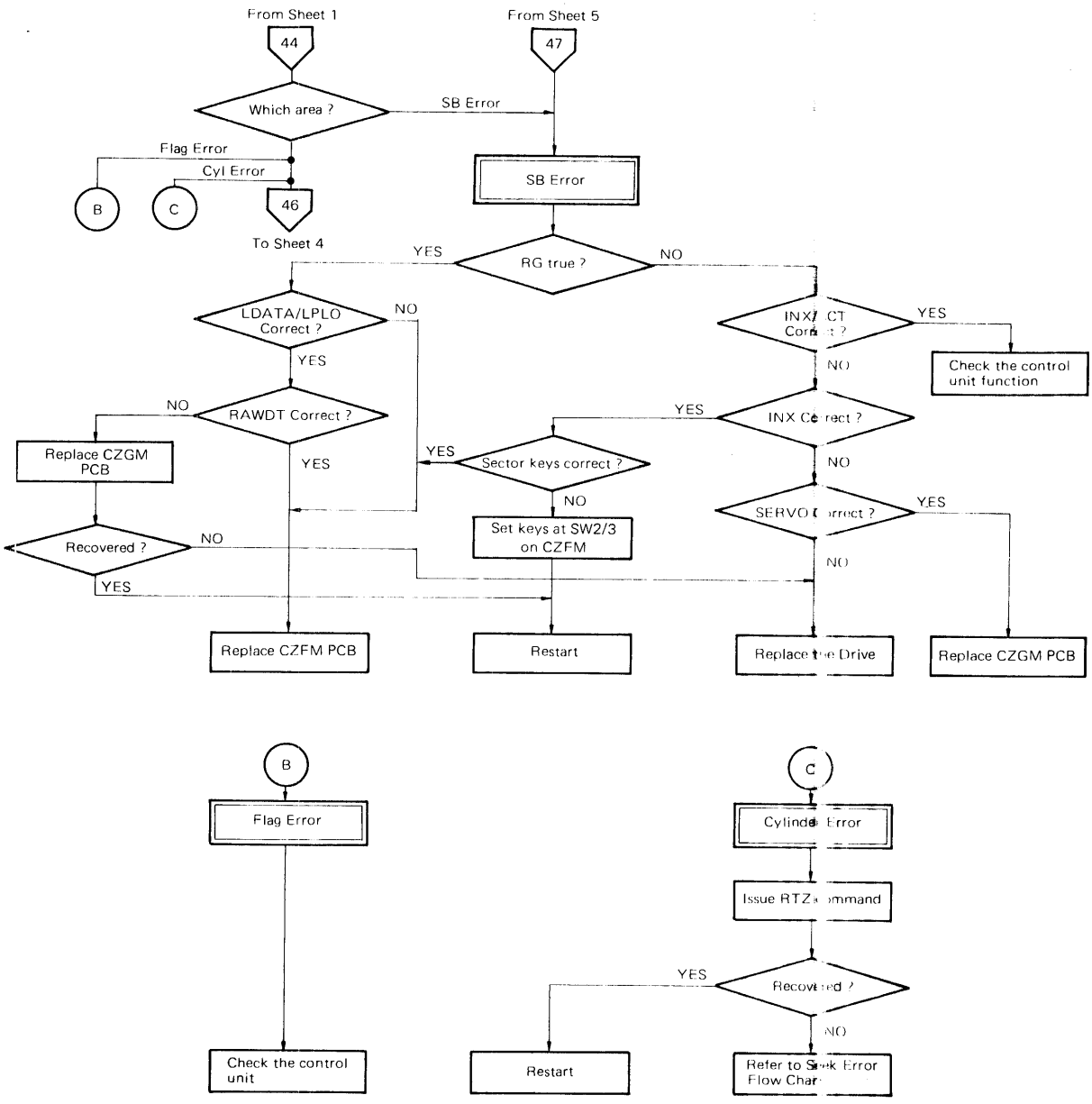


Figure 5-5-7 Read Error Flow Chart (Sheet 3 of 6)

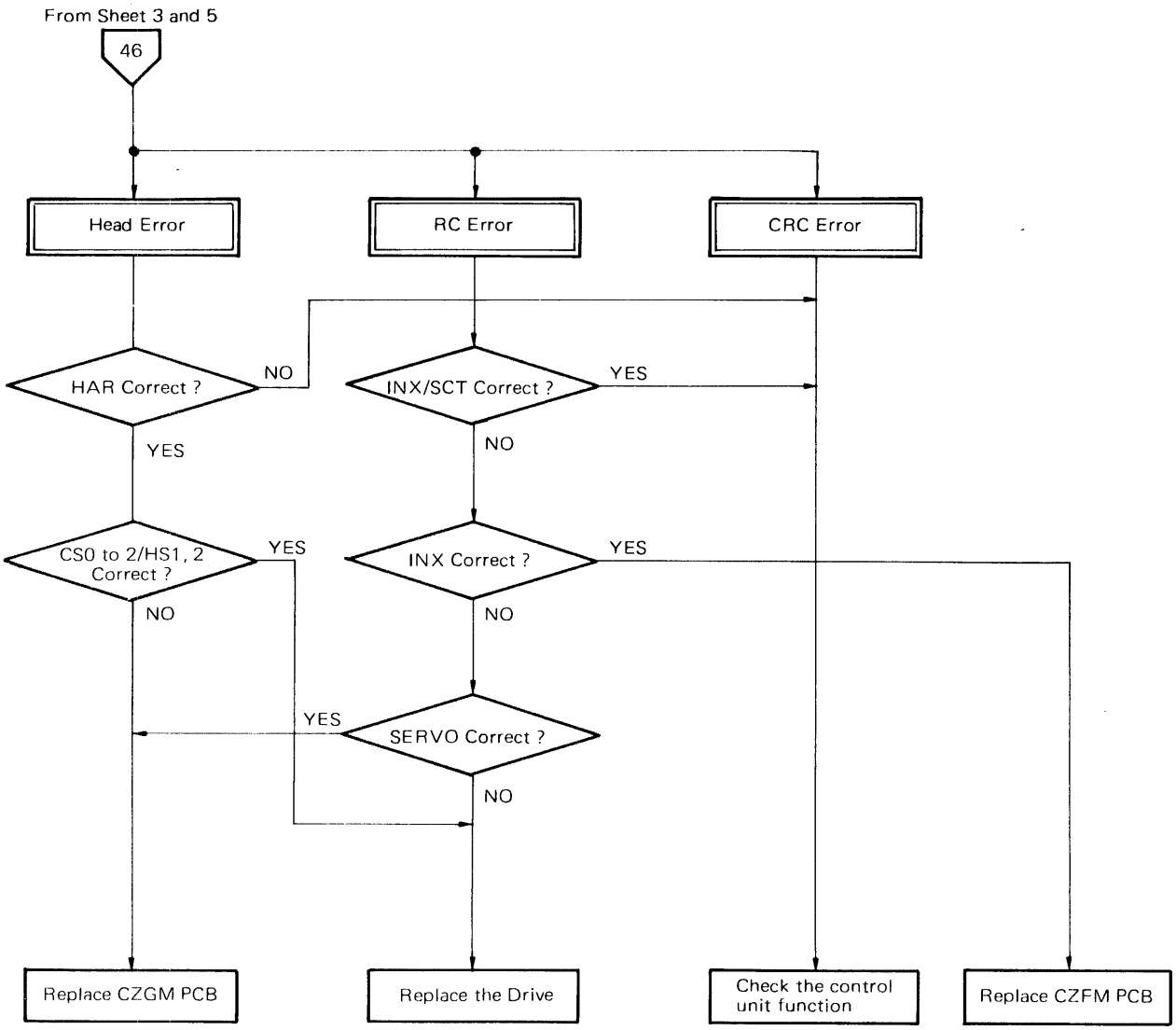


Figure 5-5-7 Read Error Flow Chart (Sheet 4 of 6)

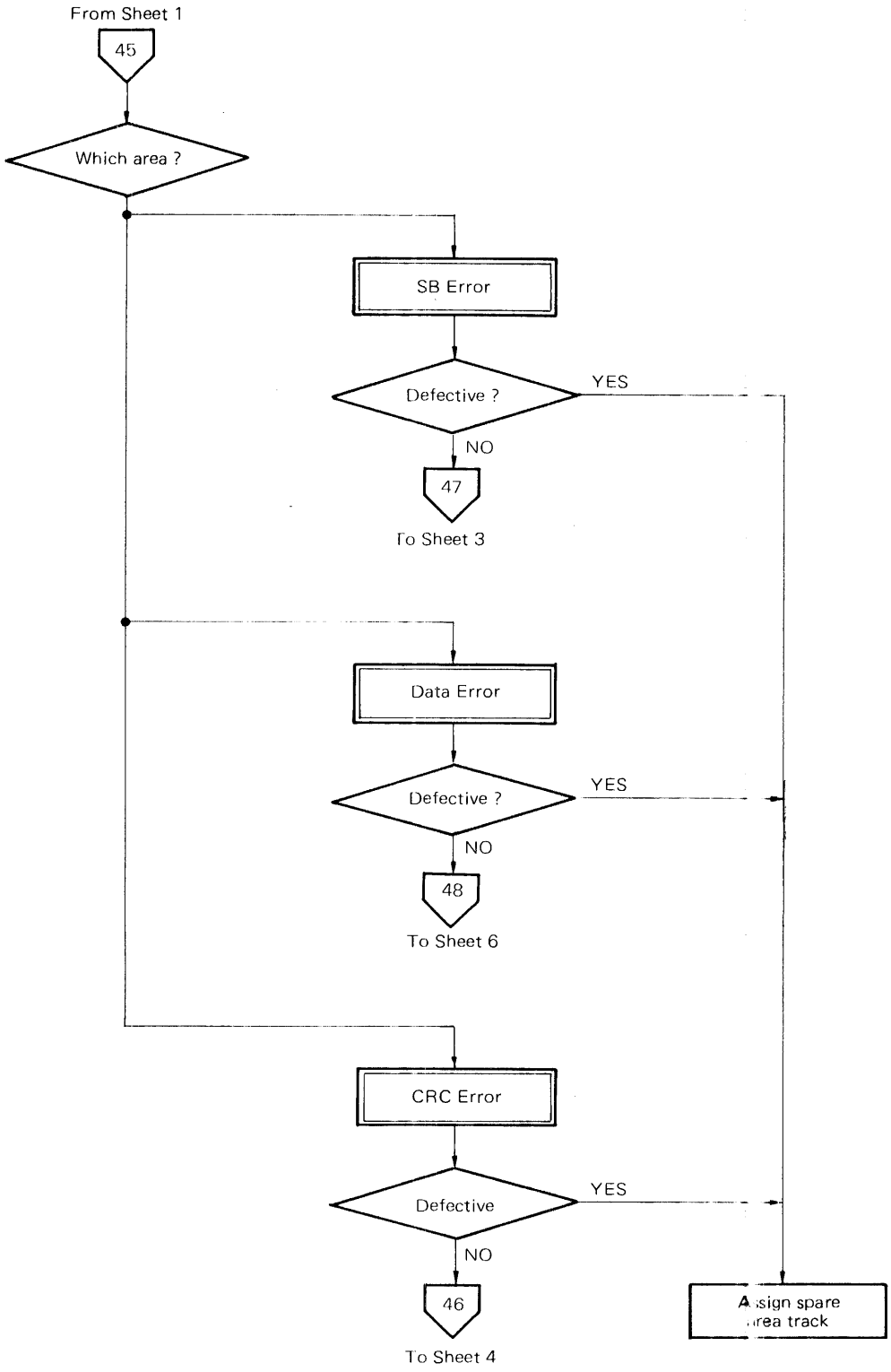


Figure 5-5 7 Read Error Flow Chart (Sheet 5 of 6)

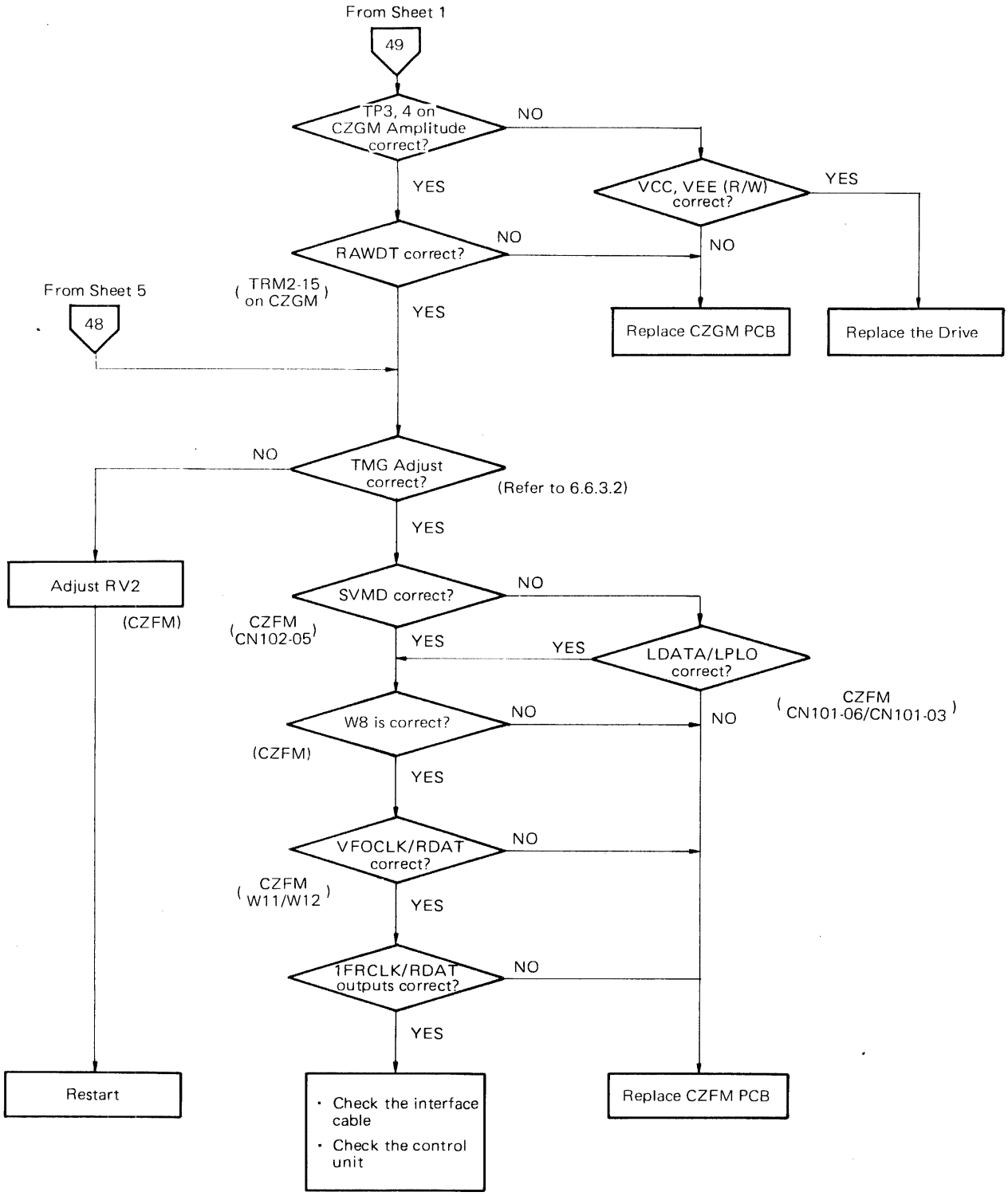


Figure 5-5-7 Read Error Flow Chart (Sheet 6 of 6)

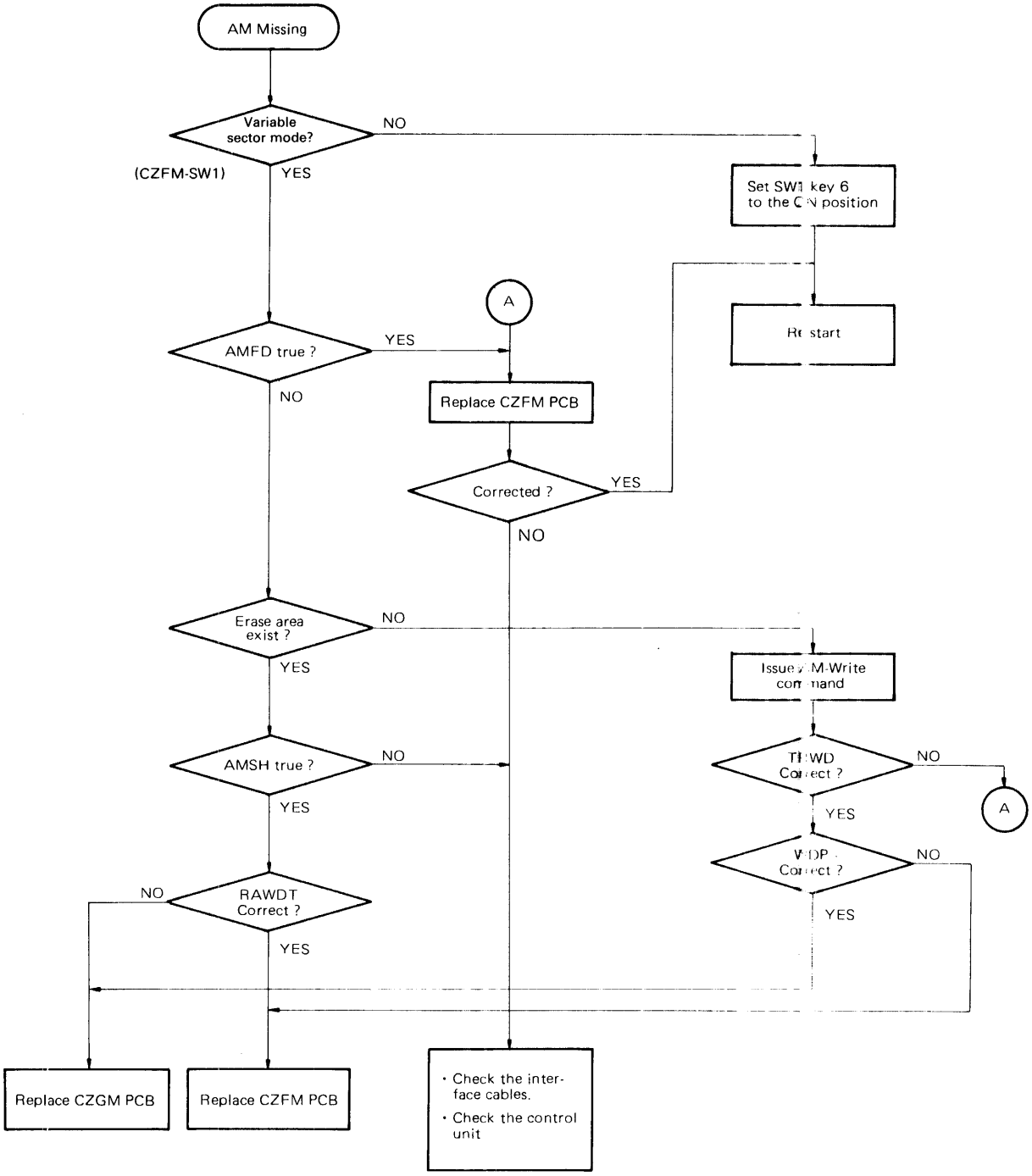


Figure 5-5-8 AM Missing Flow Chart

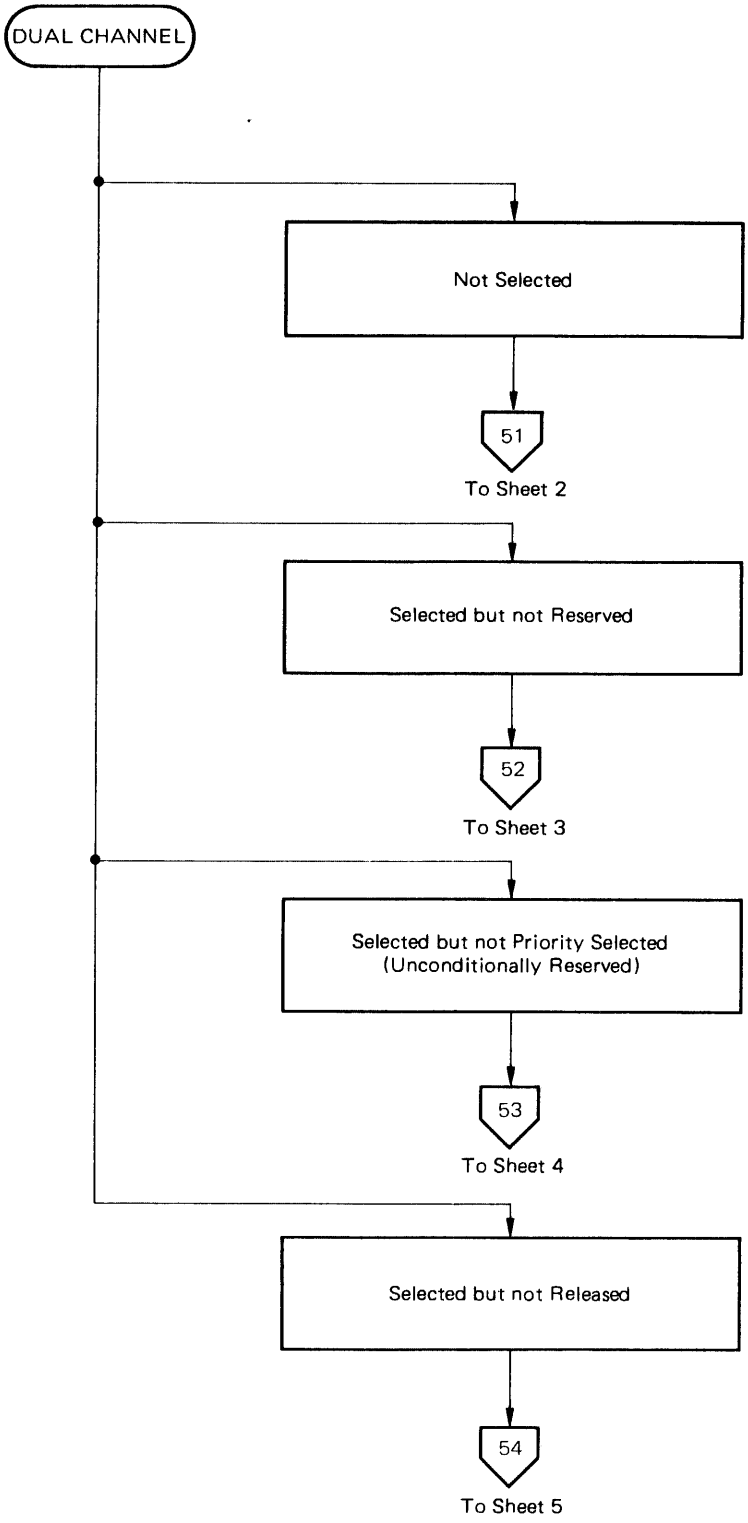


Figure 5-5-9 Dual Channel Malfunction Flow Chart (Sheet 1 of 5)

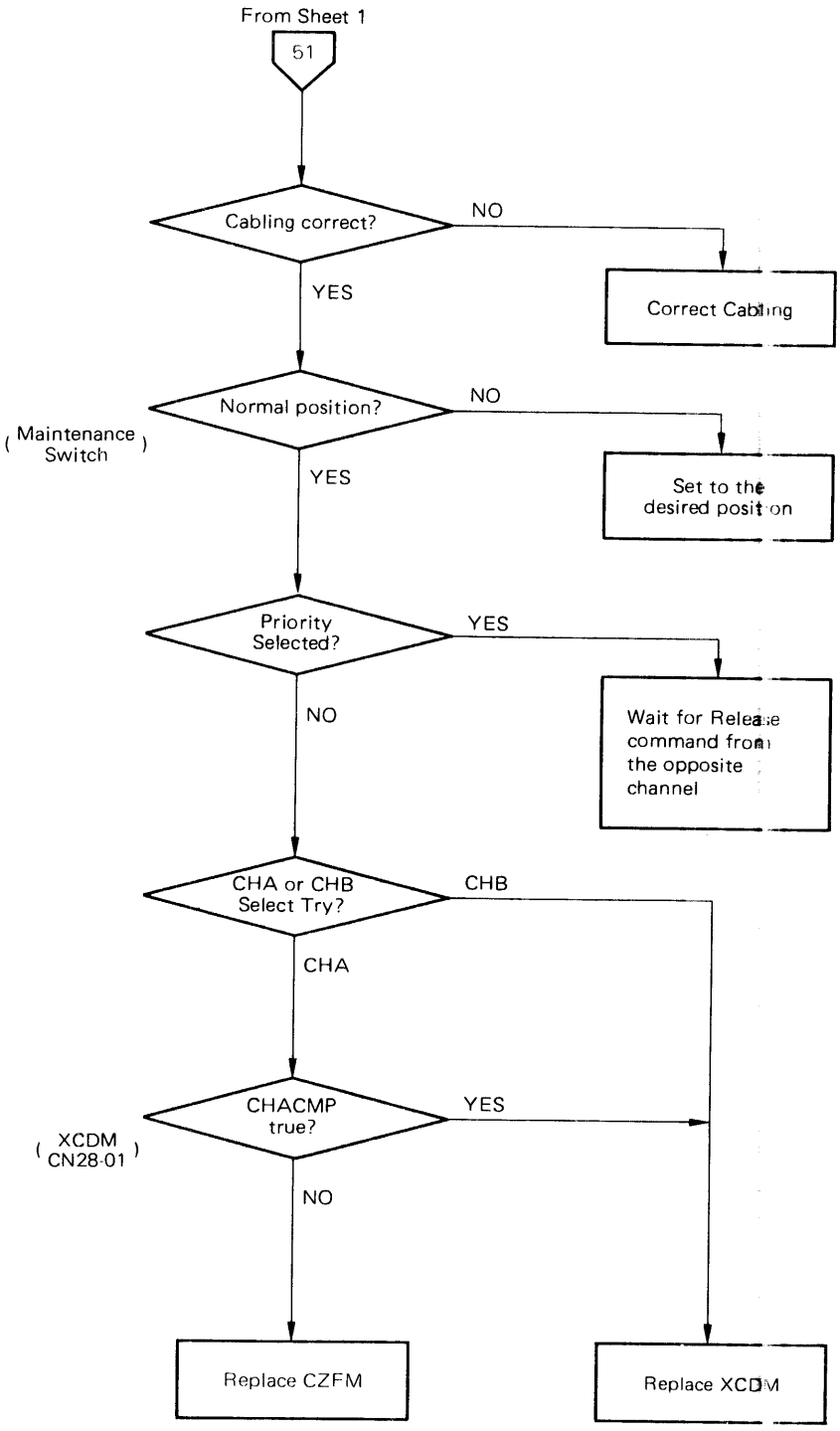


Figure 5-5-9 Dual Channel Malfunction Flow Chart (Sheet 2 of 5)

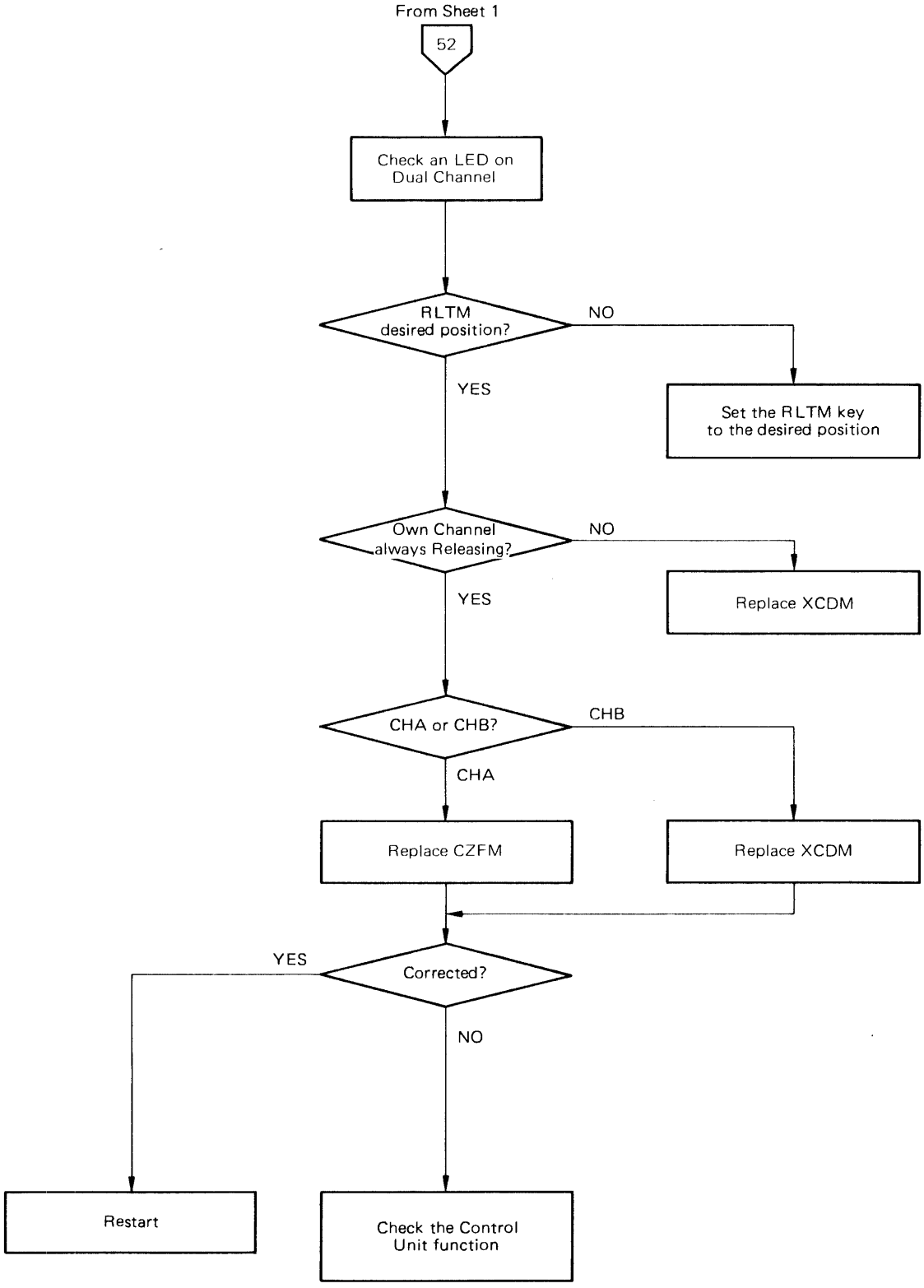


Figure 5-5-9 Dual Channel Malfunction Flow Chart (Sheet 3 of 5)

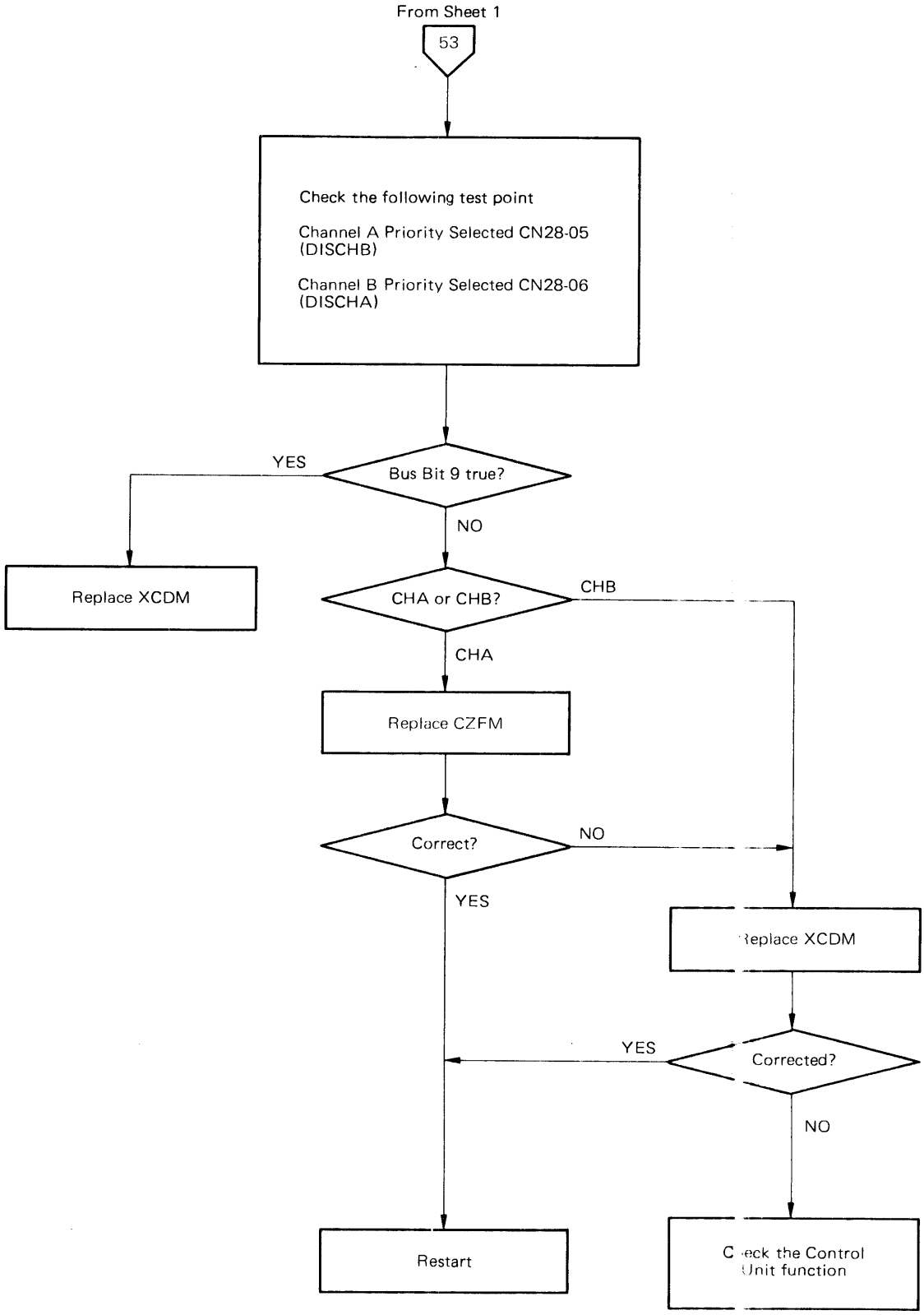


Figure 5-5-9 Dual Channel Malfunction Flow Chart (Sheet 4 of 5)

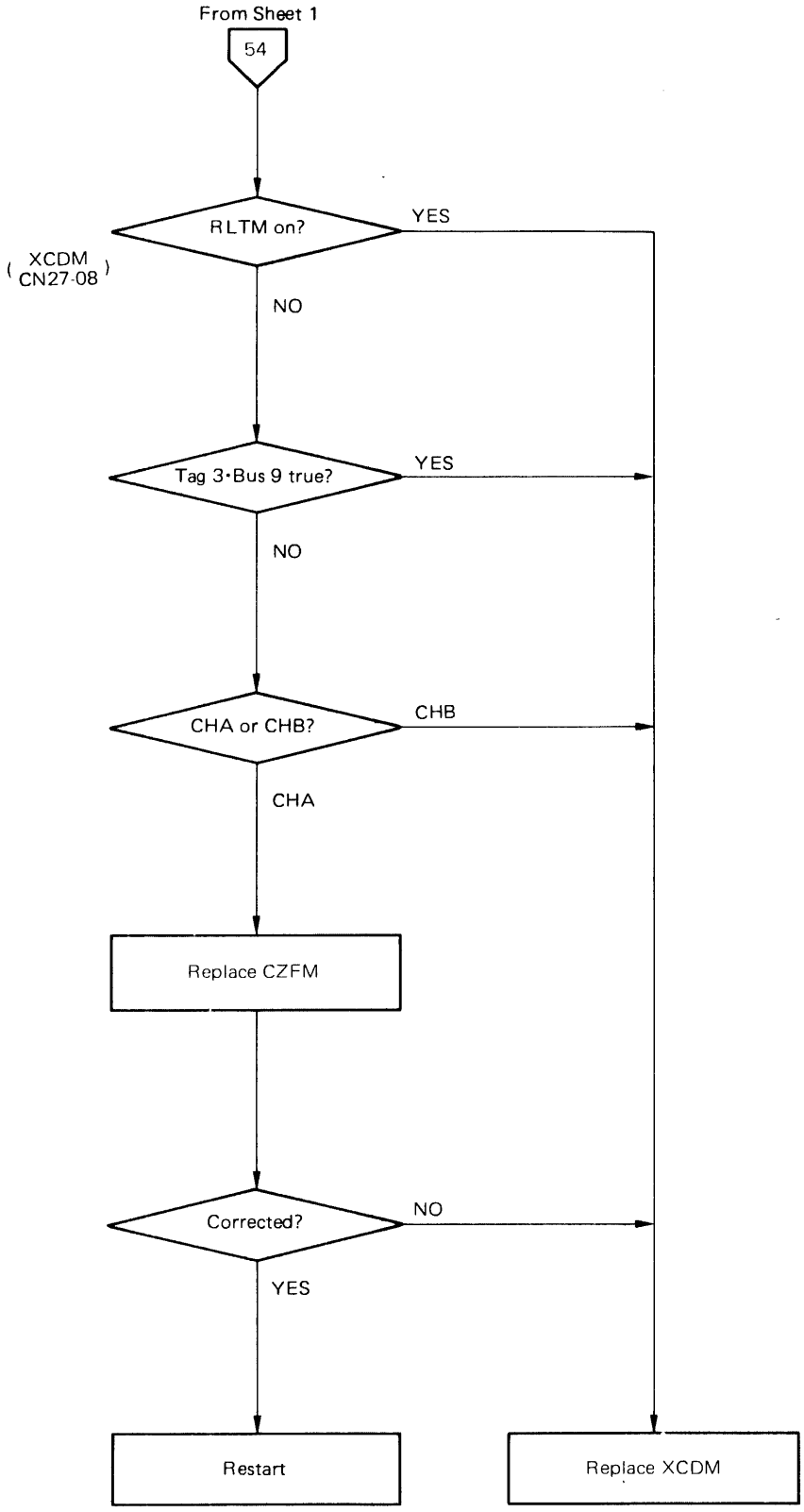


Figure 5-5-9 Dual Channel Malfunction Flow Chart (Sheet 5 of 5)

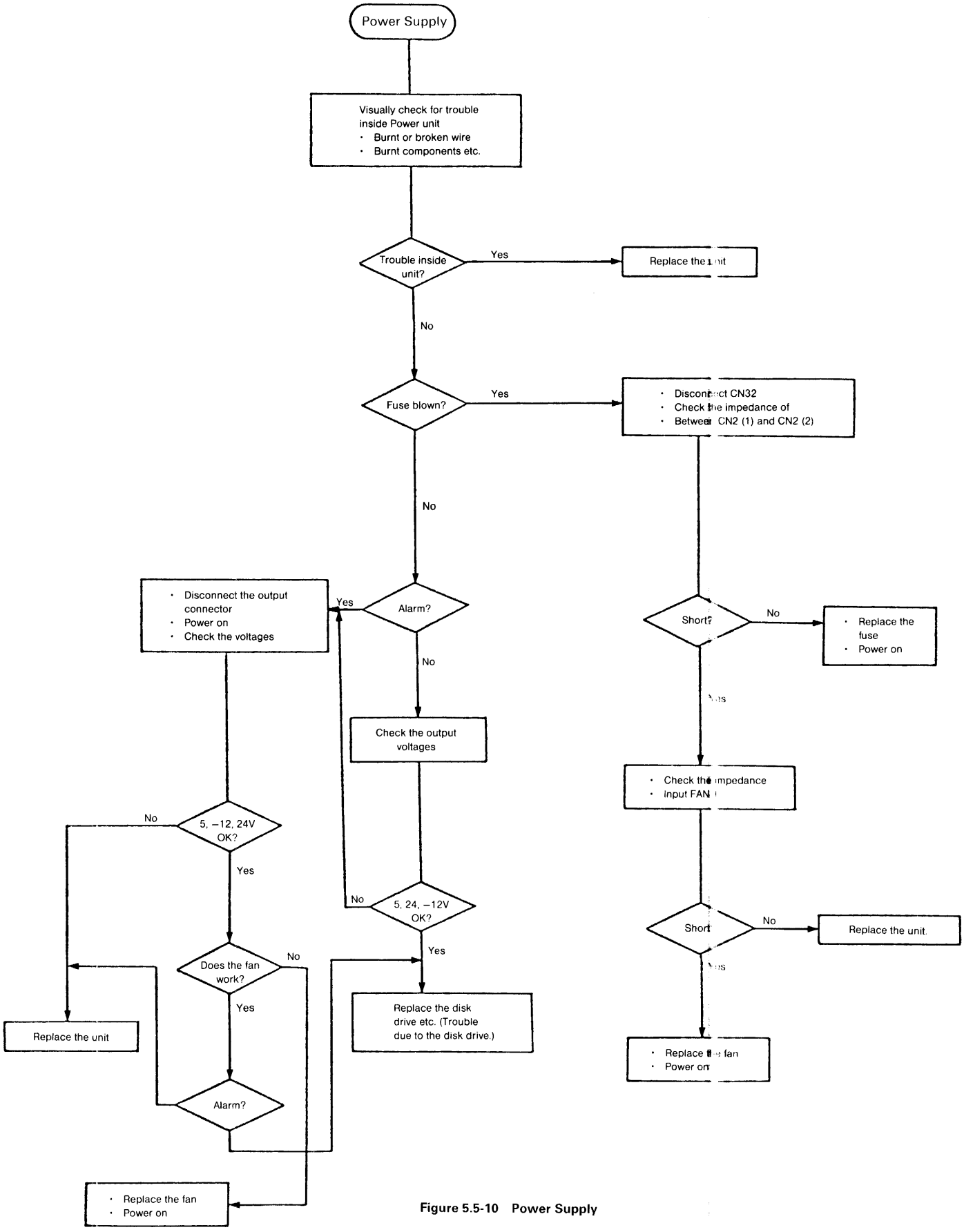


Figure 5.5-10 Power Supply

Section 6
Maintenance

6. MAINTENANCE

6.1 INTRODUCTION

This section covers maintenance of the unit, and is divided into General Precautions, Preventive Maintenance, Maintenance Equipment, Parts Replacement, and Electrical Checks and Adjustment items.

6.2 GENERAL PRECAUTIONS

6.2.1 Power On/Off

(1) Visually check the condition of the device before turning the power on.

(2) Always turn the power off before removing or inserting printed circuit boards or connectors.

(3) After maintenance, before turning the power on, ensure that all printed circuit boards and connectors correctly seated and installed in the correct position.

6.2.2 Parts Replacement

(1) Use screwdrivers that match the size of the screws.

(2) Do not leave removed screws in the drive.

Caution: Never loosen the retaining clamps for the DE aluminum cover. The DE must not be opened in the field. Screws marked with paint on their heads must not be loosened.

6.2.3 Dual Channel Switches

(1) Turn the switches to the desired position according to system configuration.

(2) After maintenance, turn the maintenance switch to the Normal A/B (NRA/NRB) position.

6.2.4 Other

(1) Use test equipment that has been correctly calibrated.

(2) Always record failure symptoms and remedies employed for later reference.

(3) To ease the installation of the D.C. power cable at CN9 and CN10; loosen the two CZFM screws (screws 'B' in figure 6-5-3).

6.3 MAINTENANCE TOOLS AND EQUIPMENT

Table 6-3-1 Maintenance Tools and Equipment

Tool and equipment	Model
Oscilloscope	TEKTRONIX 475, or equivalent
Oscilloscope probe (x 10)	TEKTRONIX P6053B, or equivalent
Digital multimeter	
Screwdriver	

6.4 PREVENTIVE MAINTENANCE

No preventive maintenance is required.

6.5 PCB ASSEMBLY REPLACEMENT

The parts required for maintenance are the three printed circuit board assemblies. (in case that dual channel option is not mounted). (Refer to Section 7. Spare Parts.) This section describes the removal of bad PCB.

6.5.1 PCB Assembly Arrangement

Three PCB assemblies are mounted on the DE as shown in Figure 6-5-1.

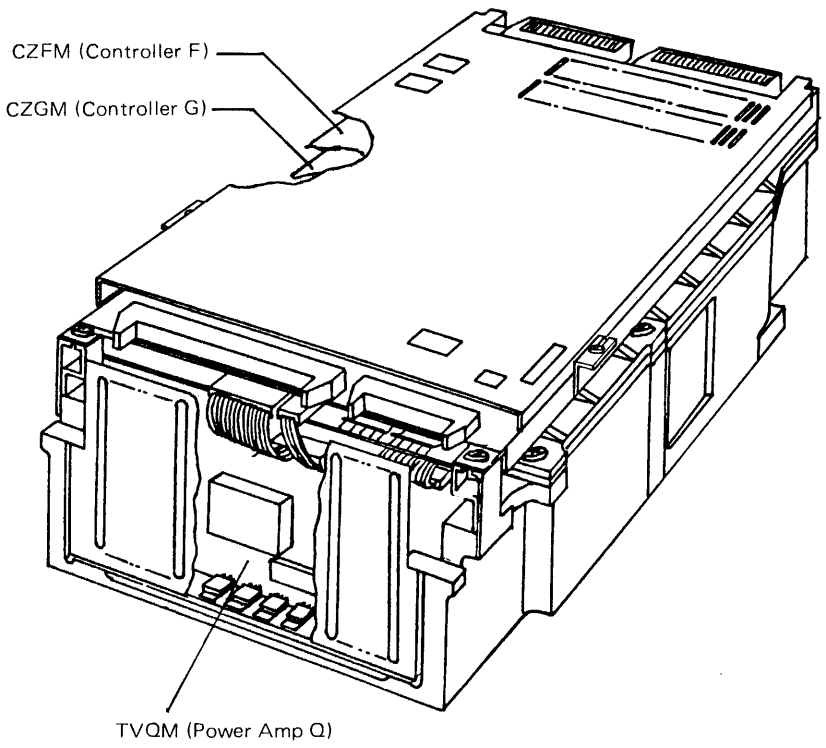


Figure 6-5-1 PCB Assy. Arrangement

6.5.2 CZFM PCB Assembly Replacement Procedure

Refer to Figure 6-5-2.

To replace the CZFM PCB Assembly, proceed as follows:

(1) Removal
   (A) Loosen screws "A" and remove the top cover.
   (B) Disconnect wiring (CN3 and CN4) from the CZFM PCB assembly.
   (C) Remove the six screws indicates in Figure 6-5-2.
   (D) Remove the CZFM PCB assembly by lifting it.

(2) Installation
   (A) Fasten the CZFM PCB Assembly to the side frame, six screws.
   (B) Fasten connectors (CN3 and CN4).
   (C) Install the top cover and tighten screws "A".

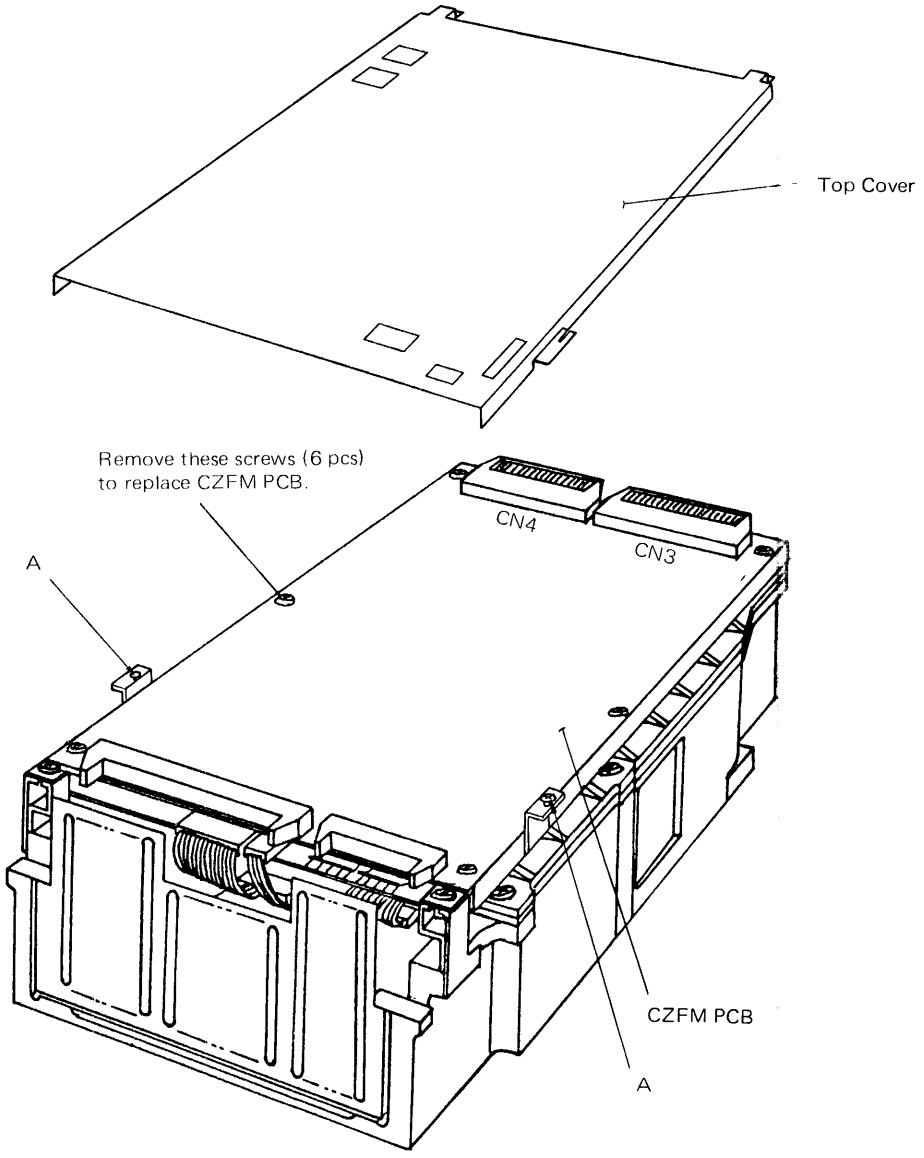


Figure 6-5-2 CZFM PCB Assembly Replacement

6.5.3 CZGM PCB Assy. Replacement Procedure

To replace the CZGM PCB Assembly, proceed as follows:
Refer to Figure 6-5-3.

(1) Removal
  (A) Loosen screws "B".
  (B) Raise the CZFM PCB Assy. by lifting up the upper side-frame.
  (C) Disconnect wiring (CN5, CN6, CN7, CN8, CN9, and CN10).

(D) Remove six screws, and lift out the CZGM PCB Assembly. Be careful not to damage CN15 on the TIXM (Through Connector).
The TIXM is connected to the CZGM PCB assembly at the back of the board. Refer to Figure 6-5-4. CN15 will be disconnected by lifting the CZGM PCB assembly.

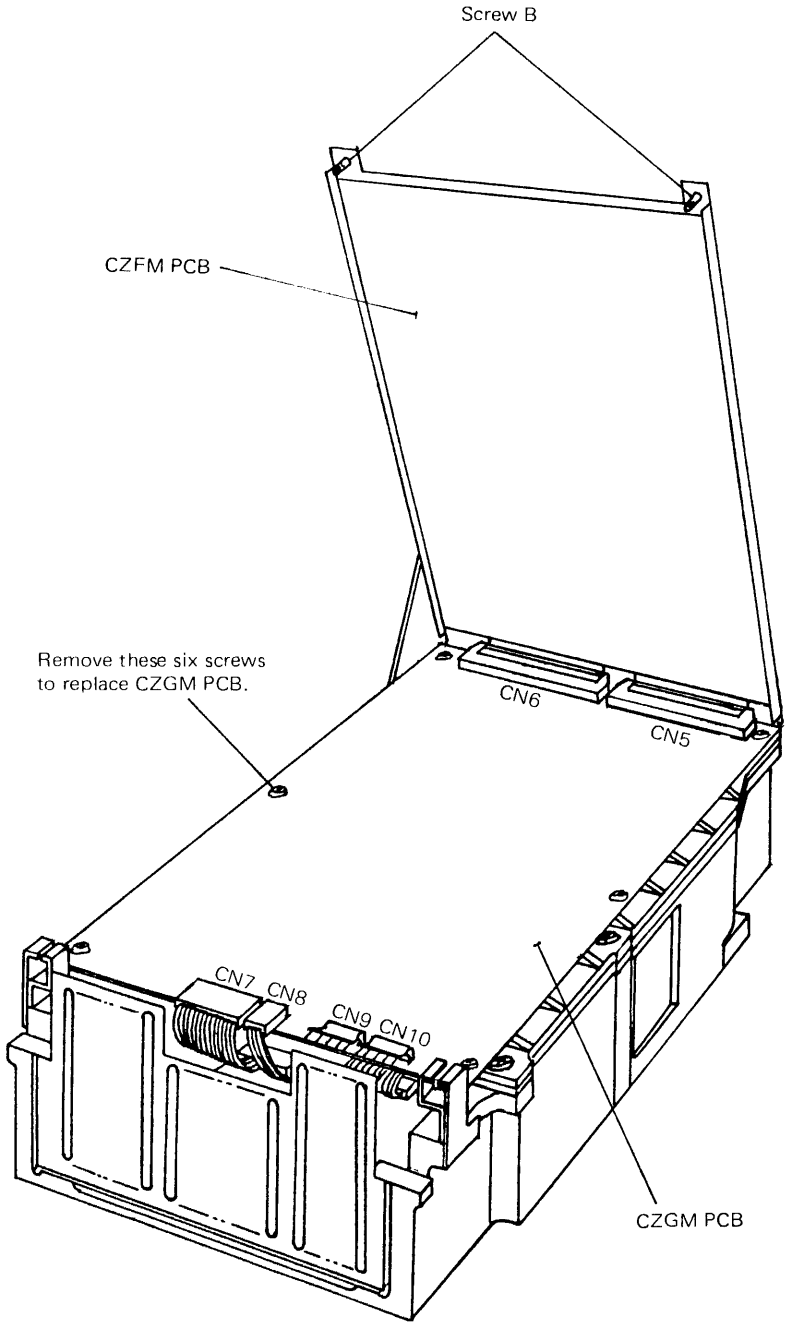


Figure 6-5-3 CZGM PCB Replacement

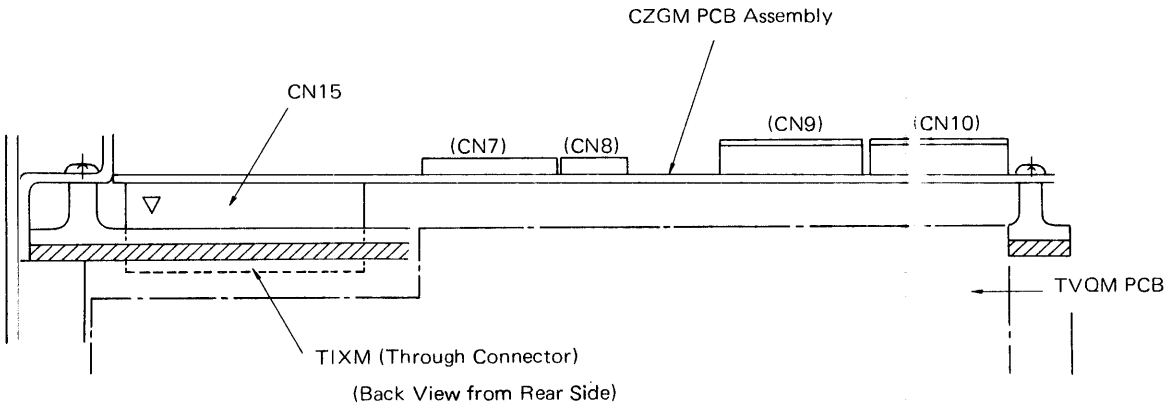


Figure 6-5-4 TIXM Connection

(2) Installation
  (A) Set the CZGM PCB assembly on the lower side-frame. Then, check that CN15 is connected correctly.
  (B) Fasten the six screws, and fasten other connectors.
  (C) Tighten screws "B".

6.5.4 TVQM PCB Assembly Replacement

The TVQM PCB assembly is mounted on the rear side of DE. Refer to Figure 6.5.5.

(1) Removal
  (A) Remove the Fan Unit (which is optional) or the cover by loosening the the screws "E".
  (B) Disconnect wiring (CN11, CN12, CN13, and CN14) from the DE and the CZGM PCB assembly.
  (C) Remove screws "F".

  Note: Be careful not to lose the isolating bushings, which fit around the threaded portion of the screws "F". When replacing the TVQM PCB assembly.

(2) Installation
  (A) Fasten the TVQM PCB assembly to the DE with screws "F". At this time, do not forget to fit the isolating bushings.
  (B) Fasten connectors coming from the DE and the CZGM PCB assembly.
  (C) Install the optional Fan Unit or the cover with screws "E".

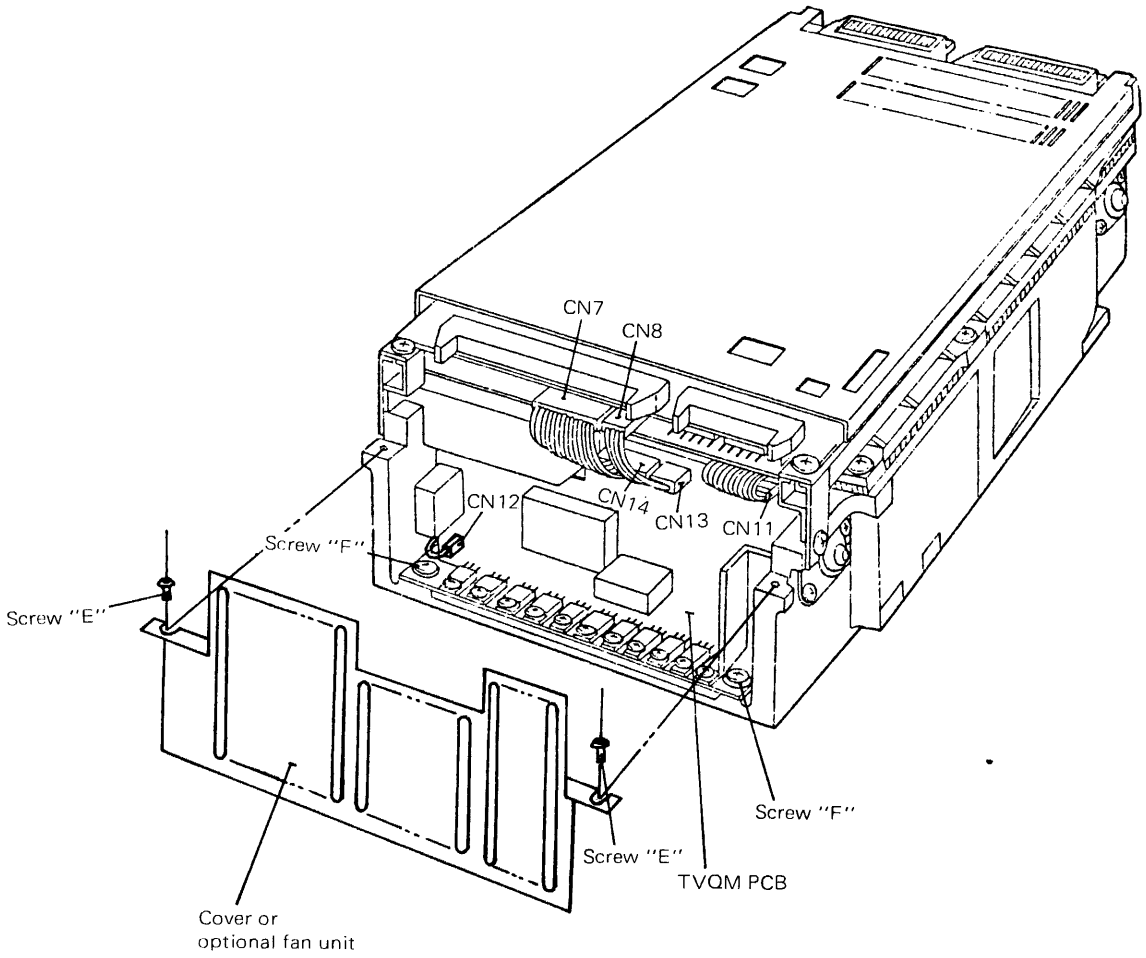


Figure 6-5-5 TVQM PCB Assembly Replacement

6.6 PCB CHECK AND ADJUSTMENT

6.6.1 Test Point Arrangement on PCB

Each PCB assembly is provided with test points and potentiometers to check and/or adjust circuit functions.

(1) CZFM PCB assembly

The test points and potentiometers are located on the CZFM PCB assembly as shown in Figure 6-6-1. Test points are listed in Table 6-6-1, check terminals in Table 6-6-2, potentiometers in Table 6-6-3, and switch keys in Table 6-6-4.

Caution: The short plugs listed in Table 6-6-2 must not be removed during PCB replacement.

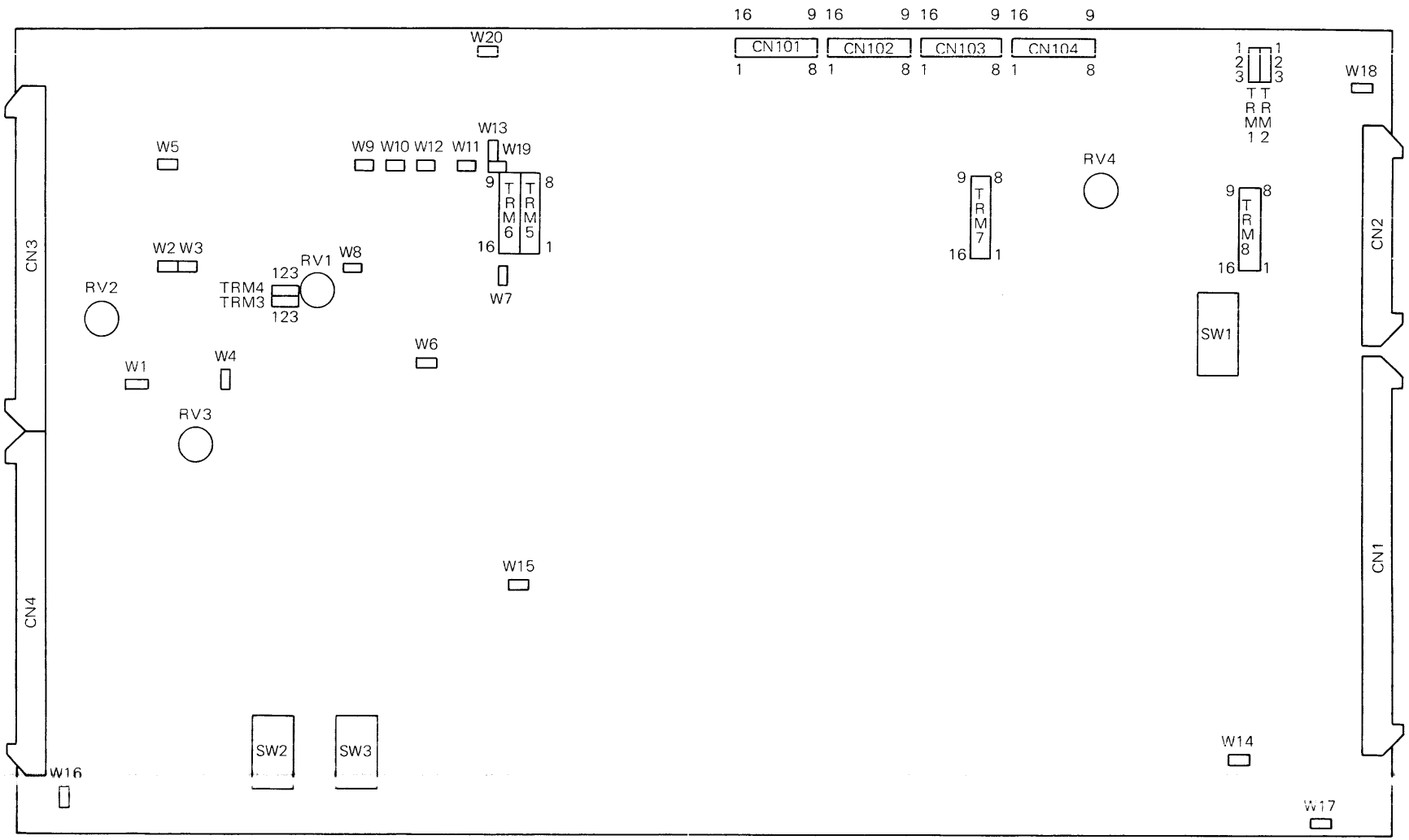


Figure 6-6-1 CZFM PCB Assembly Test Points

Table 6-6-1 CZFM Test Points

Test Point		Abbreviation	Signal Name	Signal Level	Schematic Code
Connector	Pin No.				
CN101	01	SQINH			AG2
	02	CLRG	Clock Read Gate	TTL	AL1
	03	LPLO	Lock to PLO	TTL	AL1
	04	WCPS (NCAR $\geq$ 512)			AF1
	05	VCMHTL	VCM Heat Latch	TTL	AJ2
	06	LDATA	Lock to Data	TTL	AL1
	07	INX	Index	TTL	AK1
	08				
	09	SEKM	Seek Mode	TTL	AH1
	10	SCT	Sector	TTL	AK1
	11	AMFD			AL1
	12	*VFOFS	VFO Fast Sync.	TTL	AL2
	13	*CTF	Count F	TTL	AL2
	14	WCS (NCAR $\geq$ 256)			AF1
	15	DMFLL			AJ2
	16	OV	Ground		
CN102	01	SKEND	Seek End	TTL	AJ1
	02	GTZM	Go To Zero Mode	TTL	AH1
	03	OFSET			AE1
	04	SLD	Selected	TTL	AC1
	05	RDMD	Read Mode	TTL	AL2
	06	FLT	Fault	TTL	AJ2
	07	SKERR			AJ1
	08				
	09	ONCYL			AJ1
	10	DEQZ			AF2
	11	DRLM	Drive Liner Motor	TTL	AH1
	12	*ACDME	Accelerate DC Motor	TTL	AG2
	13	UNSQ	Under Sequence	TTL	AH1
	14	*RLDR			AG2
	15	RGC	Read Gate Control	TTL	AE1
	16	OV	Ground		
CN103	01	RTZC	Return to Zero Control	TTL	AE1
	02	PWRDY1			AG1
	03	PWRDY2			AG1
	04	DFWD	Drive Forward	TTL	AH2
	05	DLSPD			AH2
	06	STCARD			AE1
	07				
	08				
	09	LNMD	Linear Mode	TTL	AH2
	10				
	11				
	12	PSDR	Position Drive	TTL	AH2

Table 6-6-1 CZFM Test Points (continued)

Test Point		Abbreviation	Signal Name	Signal Level	Schematic Code
Connector	Pin No.				
	13	*BRLS			AG2
	14	*OSCLK			AG1
	15	WGC	Write Gate Control	TTL	AE1
	16	OV	Ground		
CN104	01				
	02	*CKCLRK			AD1
	03	SKI	Seek In Complete	TTL	AJ3
	04				
	05	RDY	Ready	TTL	AJ1
	06	*AMRD			AL1
	07	CHACMP			AC1
	08				
	09	*PLOCL			AL1
	10				
	11				
	12				
	13				
	14				
	15				
	16	OV	Ground		
—	W1	DTIN1	Data In 1	ECL	AM1
	W2	DLDT	Delayed Data	ECL	AM1
	W3	DTIN2	Data In 2	ECL	AM1
	W4	REF	Reference Pulse	ECL	AM1
	W5	QQRST	QQ Reset	ECL	AM1
	W6	FLTSQ	Filter Squelch	Analog	AM2
	W7	VFOFS	VFO Fast Sync.	Analog	AM2
	W8	VFOVC	VFO Control Voltage	Analog	AM2
	W9	-2FEYB	2F Early B	ECL	AM2
	W10	DTWD	Data Window	ECL	AM3
	W11	RCLK	Read Clock	ECL	AM3
	W12	RDAT	Read Data	ECL	AM3
	W13	-5.2V	-5.2V DC (VFO)	DC	AM3
	W14	-5V	-5V DC	DC	AB2
	W15	*ENWDP	Write Data Pulse	TTL	AL2
	W16	OV	Ground		
	W17	OV	Ground		
	W18	OV	Ground		
	W19	PHRST	Phase Reset	ECL	AM3
	W20	OV	Ground		

Table 6-6-2 CZFM Check Terminals

TRM5					
Pin	**Abbreviation**	**Signal Name**	**Pin**	**Abbreviation**	**Signal Name**
09	OV	Ground	08	OV	Ground
10	(*FLTSQ)	→	07	(*FLTSQ)	←
11	OV	Ground	06	OV	Ground
12	(*VFOFS)	→	05	(*VFOFS)	←
13	OV	Ground	04	OV	Ground
14	(*CTF)	→	03	(*CTF)	←
15	OV	Ground	02	OV	Ground
16	(SVMD)	→	01	(SVMD)	←
TRM6					
Pin	**Abbreviation**	**Signal Name**	**Pin**	**Abbreviation**	**Signal Name**
09	(RAWDT)	→	08	(RAWDT)	←
10	OV	Ground	07	OV	Ground
11	(VFOCLK)	→	06	(VFOCLK)	←
12	OV	Ground	05	OV	Ground
13	(RDAT)	→	04	(RDAT)	←
14	OV	Ground	03	OV	Ground
15	(VFO2F)	→	02	(VFO2F)	←
16	OV	Ground	01	OV	Ground
TRM7					
Pin	**Abbreviation**	**Signal Name**	**Pin**	**Abbreviation**	**Signal Name**
09	STLTRE (O)	→	08	STLTRE (I)	←
10	OFSTS (O)	→	07	OFSTS (I)	←
11	*SKSTL (I)	→	06	*SKSTL (O)	←
12	OFINT (I)	→	05	OFINT (O)	←
13	*SKIINH (I)	→	04	*SKIINH (O)	←
14	NMINT (I)	→	03	NMINT (O)	←
15	ILCYTR (O)	→	02	ILCYTR (I)	←
16	NMSEK (O)	→	01	NMSEK (I)	←
TRM8					
Pin	**Abbreviation**	**Signal Name**	**Pin**	**Abbreviation**	**Signal Name**
09	STG2		08	OV	
10	STG1		07	RDY	
11	STS4		06	FPT	
12	STS2		05	EMGN	
13	STS1		04		
14			03		
15			02		
16	+5V		01		

Note) The pins shown by "→←" must be connected with short-plug (C63L-0790-0001).

Table 6-6-3 CZFM Potentiometer Function

Pot. No.	Function/Adjustment	Reference TP
RV1	VFO Free-run Frequency	W8, W9
2	Time-margin Measurement	W2, W10
3	Reference Pulse Width Adjustment	W4
4	Settling 1 (2.0 ms)	F7-05

Note: No adjustment is required when the CZFM PCB is replaced.

Table 6-6-4 CZFM Switch Function

No.	Function	Reference TP
SW1	Disk Addressing Device Type (when Tag 4/5 enabled) Tag 4/5 Enable Hard/Soft Sector mode File Protect On-End	None
SW2 SW3	Sector Counting	CN101-07, 10
TRM1 TRM2	Busy signal terminator	None
TRM3 TRM4	VCO (VFO) select	W8, W9

(2) CZGM PCB assembly

The test points and potentiometers located on the CZGM PCB assembly are shown in Figure 6-6-2. Test points are listed in Table 6-6-5, potentiometers in Table 6-6-6 switches in Table 6-6-7.

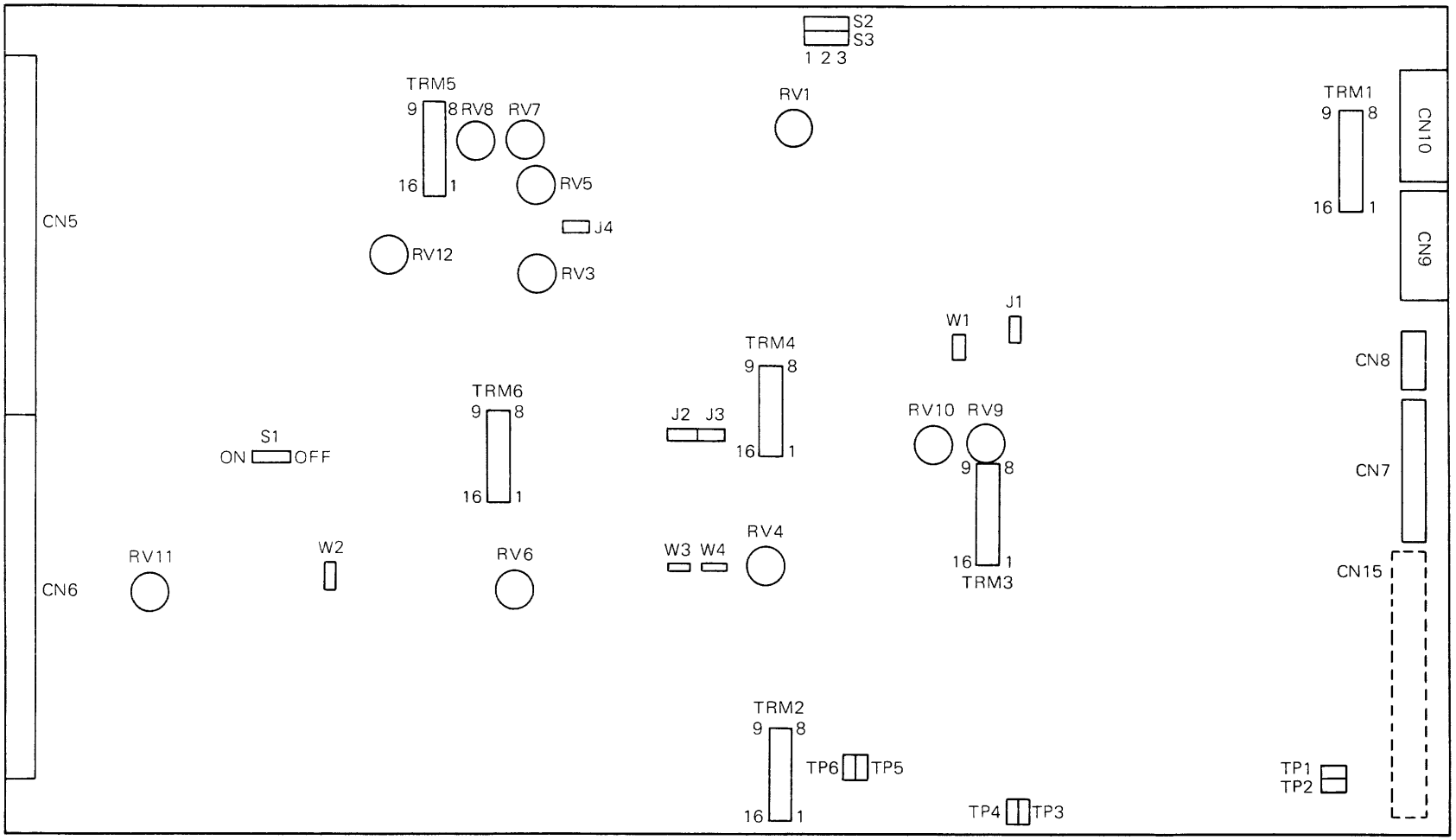


Figure 6-6-2 CZGM PCB Assembly Test Points

Table 6-6-5 CZGM Test Points

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TP1	WCA	Write Current A	Analog	BB1
2	WCB	Write Current B	Analog	BB1
3	PROT1	Pre-amplifier Output 1	Analog	BB2
4	PROT2	Pre-amplifier Output 2	Analog	BB2
5	AGOT1 SIG	Signal (AGC Output 1)	Analog	BB2
6	AGOT2 *SIG	Signal (AGC Output 2)	Analog	BB2
TRM1-1	PHA	Phase A	TTL	BD1
2	* PHB	Phase B	TTL	BD1
3	PHC	Phase C	TTL	BD1
4	–			
5	–			
6	*PWRDY1	Pow Ready 1	TTL	BE1
7	–			
8	OV	Ground		
9	–			
10	* CTCL1	Control Clock 1	TTL	BD2
11	TEST	Test (test purpose only)	TTL	BE1
12	SPDGD	Speed Good	TTL	BD2
13	Q44	Q44	TTL	BD2
14	* STARTP	Start Pulse	TTL	BD1
15	*TMCL	Timer Clock	TTL	BD1
16	STSPD	Set Speed	TTL	BD1
TRM2-1	* DIGLT	Diag Latch (test purpose only)	TTL	BB1
2	–			
3	INTLT1	Integrator Latch 1	ECL	BB2
4	DIFDT1	Differentiator Output 1	ECL	BB2
5	FSOT1	Fixed Slice Output 1	ECL	BB2
6	FSOT2	Fixed Slice Output 2	ECL	BB2
7	SMPCK	Sample Clock	ECL	BB2
8	OV	Ground		
9	PLSH1	Pulse Shaper 1	ECL	BB2
10	PLSH2	Pulse Shaper 2	ECL	BB2
11	–			
12	–			
13	–			
14	–			
15	+RAWDT	Raw Data	ECL	BB2
16	–RAWDT	Raw Data	ECL	BB2

Table 6-6-5 CZGM Test Points (Continued)

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TRM3- 1	SERVO	Servo Signal	Analog	BF1
2	AGC	AGC Voltage	Analog	BG1
3	CSNS	Current Sense	Analog	BK1
4	PLOSS	PLO Single-shot	TTL	BF1
5	*HDLD	Head Loaded	TTL	BG1
6	PLOLT	PLO Latch	TTL	BF1
7	POSN	Position Normal	Analog	BG1
8	0 V	Ground		
9	POSQ	Position Quadruture	Analog	BG1
10	SVPWD	Servo Pulse Window	TTL	BF1
11	TESTP	Test Point (test Purpose only)	TTL	BF1
12	SVPLS	Servo Pulse	TTL	BF1
13	* PLOLT	PLO Latch	TTL	BF1
14	–ABSVL	Absolute Velocity	Analog	BG2
15	SVSLT	Servo Slice Out	TTL	BF1
16	CLP	Clamp (test purpose only)	TTL	BF1
TRM4- 1	PLO1F	PLO 1 Frequency	TTL	BF2
2	*GT1	Gate 1	TTL	BJ1
3	*GT2	Gate 2	TTL	BJ1
4	*GT3	Gate 3	TTL	BJ1
5	BYTCLK	Byte Clock	TTL	BJ1
6	–			
7	PLOVC	PLO Control Voltage	TTL	BF2
8	0 V	Ground		
9	*MSDT	Missing Detect	TTL	BJ1
10	–			
11	*GT4	Gate 4	TTL	BJ1
12	*IGB2P	IGB2 Pulse	TTL	BJ1
13	–			
14	*OGBP	OGB Pulse	TTL	BJ1
15	*IGB1P	IGB1 Pulse	TTL	BJ1
16	–			

Table 6-6-5 CZGM Test Points (Continued)

No.	Abbreviation	Signal Name	Signal Level	Schematic Code
TRM5- 1	PADR	Power Amplifier Drive	Analog	BK1
2	–VEL	Velocity	Analog	BG2
3	FNVEL	Fine Velocity	Analog	BH1
4	*ACCL	Accelerate	TTL	BF2
5	–DA	Digital To Analog Output	Analog	BF2
6	–			
7	CLPOS	Clamp Position	Analog	BH1
8	0 V	Ground		
9	–FNPOS	Fine Position	Analog	BG2
10	–			
11	–			
12	–			
13	PER	Position Error	Analog	BH1
14	VER	Velocity Error	Analog	BF2
15	–			
16	FUNC	Function	Analog	BF2
TRM6- 1	*OFTRK	Off Track	TTL	BG1
2	NQGTZ	POSN + POSQ > 0	TTL	BG1
3	NGTQ	POSN > POSQ	TTL	BG1
4	*PSDR	Position Drive	TTL	BJ1
5	*OGB	OGB	TTL	BJ1
6	–			
7	DRLM	Drive Linear Motor	TTL	BJ1
8	0 V	Ground		
9	FWDD	Forward Drive	TTL	BJ1
10	TXPL	Track Crossing Pulse	TTL	BJ1
11	*INX	Index	TTL	BJ1
12	*IGB2	IGB2	TTL	BJ1
13	*IGB1	IGB1	TTL	BJ1
14	–			
15	V=0	Velocity Equal to Zero	TTL	BG2
16	ONTRK	On Track	TTL	BG1

Table 6-6-6 CZGM Potentiometer Function

Pot. No	Function/Adjustment	Reference TP
RV1	VCO (PLO) Adjustment	TRM4-7/TRM4-5
3	Positioning Time Adjustment*	TRM5-4/TRM6-7
4	Position Signal Gain Adjustment*	TRM3-7/TRM6-7
5	Velocity Offset Adjustment	TRM5-2
6	Write Current Adjustment	TP1/TP2
7	Velocity Balance Adjustment	TRM5-2
8	Velocity Balance Adjustment	TRM5-2
9	Servo Pulse Window Adjustment	TRM3-10
10	PLOSS Adjustment	TRM3-4
11	DAC Output Adjustment	TRM5-5/TRM6-7
12	Fine Velocity Adjustment	TRM5-3

Note) Adjust potentiometers RV3 and RV4 when the CZGM PCB assembly is replaced.

Table 6-6-7 CZGM Switch Function

No.	Function	Reference TP
S1	Power Amplifier Drive Cut	
S2 S3	VCO (PLO) Adjustment	TRM4-7/TRM4-5

(3) XCDM PCB Assembly

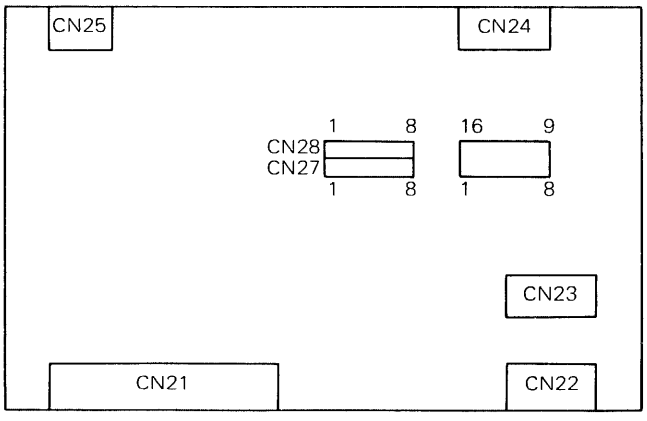


Figure 6-6-3 XCDM PCB Assembly Test Points

Table 6-6-8 XCDM Test Points

CN27 (E9)			CN28 (E9)		
Pin	**ABBR**	**Signal Name**	**Pin**	**ABBR**	**Signal Name**
1	CHAENB	Channel A Enable	1	CHACMP	Channel A Compare
2	DISAK	Disable A Key	2	*DISCHB2	Disable Channel B2
3	DISAB	Disable B Key	3	BUSYB	Busy B
4	*CHASLD	Channel A Selected	4	PWRDY	Power Ready
5	CHBENB	Channel B Enable	5	DISCHB	Disable Channel B
6	*CHBSLD	Channel B Selected	6	DISCHA	Disable Channel A
7	*DISCHA2	Disable Channel A2	7	SKENDA	Seek End A
8	RSTMK	Release Timer Key	8	SKENDB	Seek End B
CN29 (F9)					
Pin	**ABBR**	**Signal Name**	**Pin**	**ABBR**	**Signal Name**
1	*INTR	Interrupt	16	*INTR	←
2	*RSTMP	Release Timer Pulse	15	*RSTMP	←
3	CHBCMP	Channel B Compare	14	BUSYA	Busy A
4	CLK1	Clock 1	13	CLK1	←
5	*RSVCL	Reserve Clock	12	*RSVCL	←
6	CHARSV	Channel A Reserved	11	CHBRSV	Channel B Reserved
7	CLK2	Clock 2	10	CLK2	←
8	RSTMP	Release Timer Pulse	9	RSTMP	←

6.6.2 PCB Adjustment and Selection after PCB Replacement

Refer to Table 6-6-9 for the required adjustments and selections when a PCB assembly is replaced.

Table 6-6-9 Adjustments and Selections after PCB Replacement

Item	Spare Part	Adjustment/Selection
1	TVQM (B16B-9250-0010A)	None
2	CZGM (B16B-9240-0010A)	(1) Position Signal Gain Adjustment (RF4) (2) Positioning Time Adjustment (RV3)
3	CZFM (B16B-9230-0010A)	(1) Disk Addressing (SW1) (2) Sector Mode (SW1) (3) Tag 4/5 Enable (SW1) (4) File Protect (SW1) (5) Device Type (SW1) (6) Sector Counting (SW2/SW3) (7) On-End (SW1)

6.6.2.1 Position Signal Gain Adjustment

(1) Confirm that the drive has normal status.
(2) Repeatedly issue an RTZ command from Cylinder 0.
(3) Connect the test point TRM6-7 (DRLM) to one vertical input channel of an oscilloscope and trigger with the positive-going edge of the signal on the CZGM PCB (DC coupled).
(4) Connect test point TRM3-7 (POSN) to the other vertical input channel of the oscilloscope (DC coupled).
(5) Adjust potentiometer RV4 so that the POSN signal amplitude is 8.0 V ±0.4 V (peak-to-peak). Refer to Figure 6-6-4.

Note: On the occasion that the RTZ is not completed, rotate the potentiometer RV3 a little.

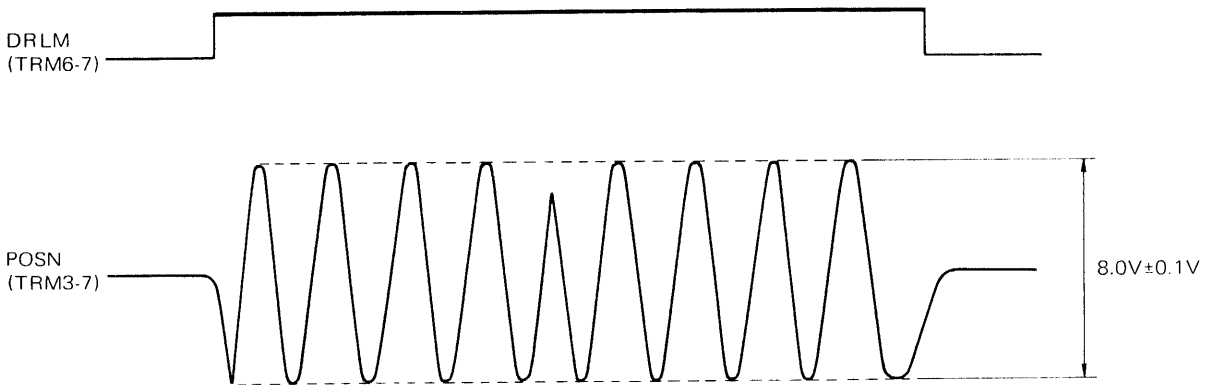


Figure 6-6-4 Position Signal Gain Adjustment

6.6.2.2 Positioning Time Adjustment

(1) Repeatedly issue an alternate seek command between Cylinder 0 and Cylinder 822 (decimal).
(2) Connect the test point TRM5-4 (*ACCL) to one vertical input channel of an oscilloscope and trigger with the positive-going edge of the signal on CZGM PCB (DC coupled).
(3) Connect the test point TRM6-7 (DRLM) to the other vertical input channel of the oscilloscope (DC coupled).
(4) Adjust potentiometer RV3 so that the decelerate time (Tdc) is 17.3 ms ± 1 ms.

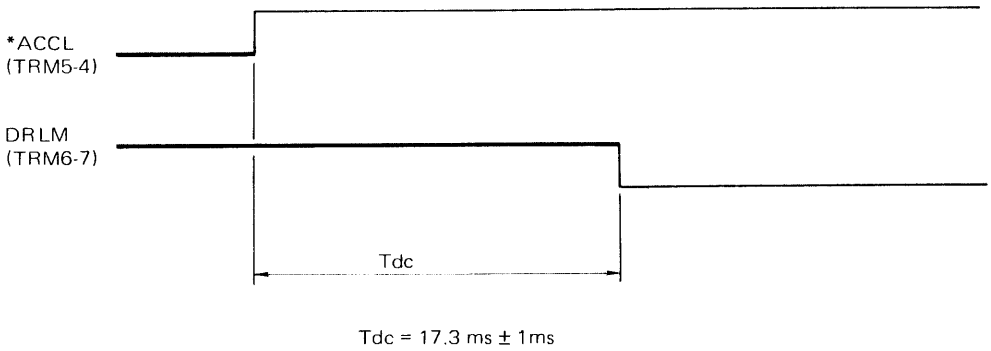


Figure 6-6-5 Positioning Time Adjustment

6.6.3 Electrical Measurement

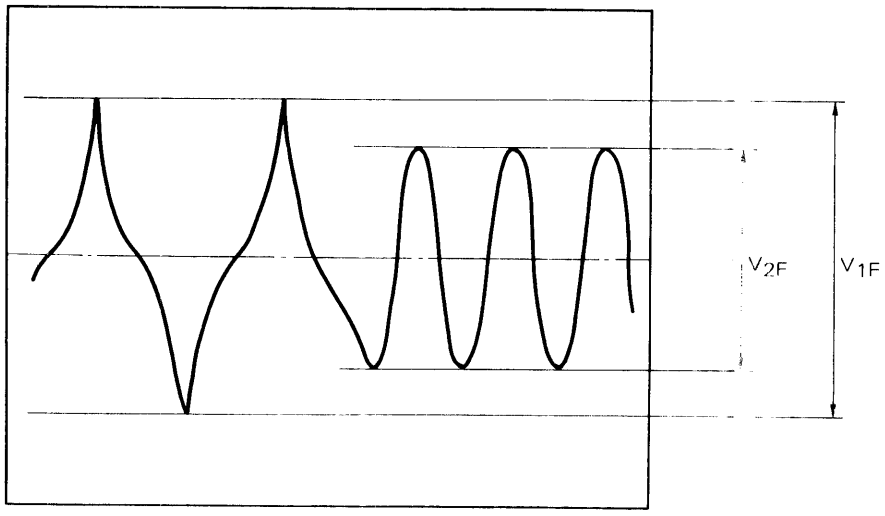
This section describes electrical measurements.

6.6.3.1 Read Output Measurement

Caution

Use the 0 V terminals near test points TP3 and TP4 on the CZGM PCB, and use a 200 MHz wide band pass oscilloscope. Measurement error may occur if these precautions are not followed.

(1) Confirm that the specific track can be rewritten for the Read Output measurement.
(2) Write repetitive "10" and "00" pattern ("AAAA000C$_{16}$") to all records on the specific track, e.g. CE track or Cylinder 0 track.
(3) Connect test points TP3 and TP4 on the CZGM PCB with differential mode (inverted CH2 and add with CH1).
(4) After writing, measure the peak-to-peak level V_{2F} and V_{1F} as shown in Figure 6-6-6.



$V_{2F} \geq 200$ mVp-p

Resolution Ratio = $\frac{V_{2F}}{V_{1F}} \times 100(\%) \geq 55\%$

Figure 6-6-6 Read Output Measurement

6.6.3.2 Timing Margin Measurement

Caution

Use the 0 V terminal or signal ground near check terminals CH1 and CH3 for measurement, and a 200 MHz, wide band pass oscilloscope. Otherwise some measurement error may occur.

(1) Record this worst-case data pattern "$EB6DB6DB_{16}$" on all records of the specific track, e.g. CE track or Cylinder 0 track.
(2) Connect terminal W10 on the CZFM PCB to one vertical input of the oscilloscope (DC coupled).
(3) Connect terminal W2 to the other vertical input channel of the oscilloscope (DC coupled).
(4) Trigger with the positive-going edge of the W10 signal (DTWD).
(5) Adjust the W2 (DLDT) signal by the potentiometer RV2 to the minimum width of the critical state, so that no errors occur for 20 seconds. See TW1 in Figure 6-6-7.
(6) Similarly, adjust the maximum width as mentioned above. See TW2 in Figure 6-6-7.
(7) Perform the steps (5) and (6) using each Head on the specific cylinder.
(8) The timing margin will be specified as follows:

$$T_{TMG} = TW2\ (max) - TW1\ (min) \geq 8\ ns$$

(9) Adjust the W2 signal as follows:

$$T_{ADJ} = \frac{TW2\ (max) + TW1\ (min)}{2} = 25\ ns$$

Refer to Figure 6-6-7.

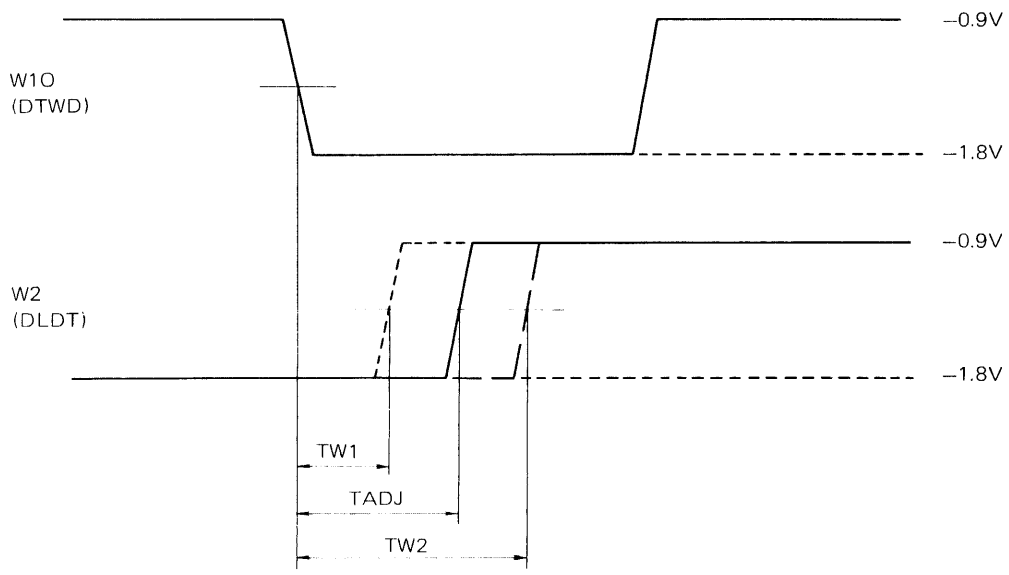


Figure 6-6-7 Timing Margin Measurement

6.6.4 Electrical Check and Adjustment

This section describes electrical checks and adjustments when an error and/or fault has occurred in the unit, or when a repair action has been performed.

Caution

Do not perform the following adjustments when the PCB is replaced.

6.6.4.1 CZFM PCB

(1) Settling 1 (STL1) Adjustment (RV4)

1. Confirm that unit has a normal status.
2. Connect test point F7-05 (STL1) signal one channel of the oscilloscope (DC coupled).
3. Issue a repetitive RTZ command to the drive.
4. Trigger the oscilloscope with the positive-going edge of the test point signal.
5. Adjust potentiometer RV4 so that the following T_{STL1} is 2.0 ms ±0.1 ms (Refer to Figure 6-6-8).

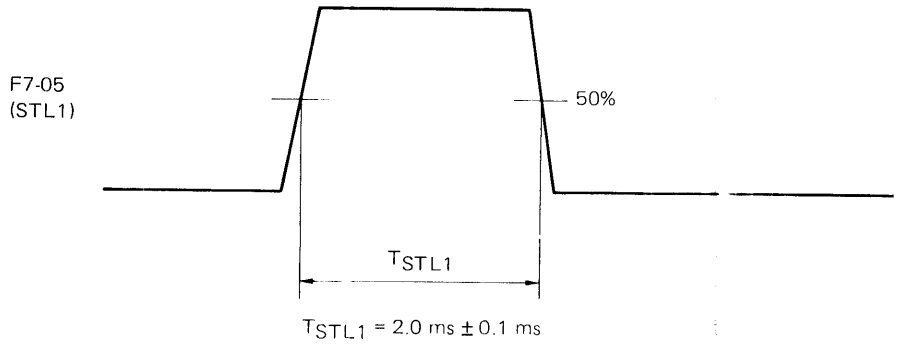


Figure 6-6-8 Settling 1 Adjustment

(2) Reference Pulse Adjustment (RV3)

1. Confirm that unit has a normal status.
2. Connect test point W4 (REFP) signal to one channel of the oscilloscope (DC coupled).
3. Trigger the oscilloscope with the positive-going edge of the test point signal.
4. Adjust potentiometer RV3 so that the following T_{REF} is 19 ns ±1 ns.

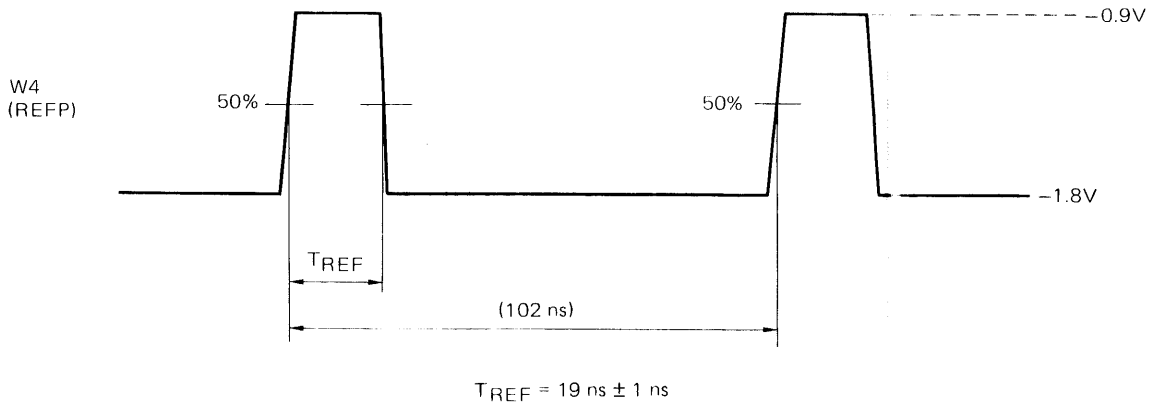


Figure 6-6-9 Reference Pulse Adjustment

(3) VFO Free-run Frequency Adjustment (RV1)

1. Turn power off.
2. Remove the short plug between TRM5-10 and TRM5-7.
3. Clamp the TRM5-7 signal (*FLTSQ) to 0 V.
4. Turn power on and wait 40 seconds.
5. Adjust potentiometer RV1 to the center position.
6. Connect W9 (–2FEYB: ECL level) to a frequency counter.
7. Select the proper capacitance as shown in Figure 6-6-9 so that the frequency of W9 is closest to 19.664 MHz.
8. Adjust potentiometer RV1 so that the frequency of W9 is 19.664 MHz ± 0.1 MHz, and connect TRM5-10 and TRM5-7 with the short-plug.

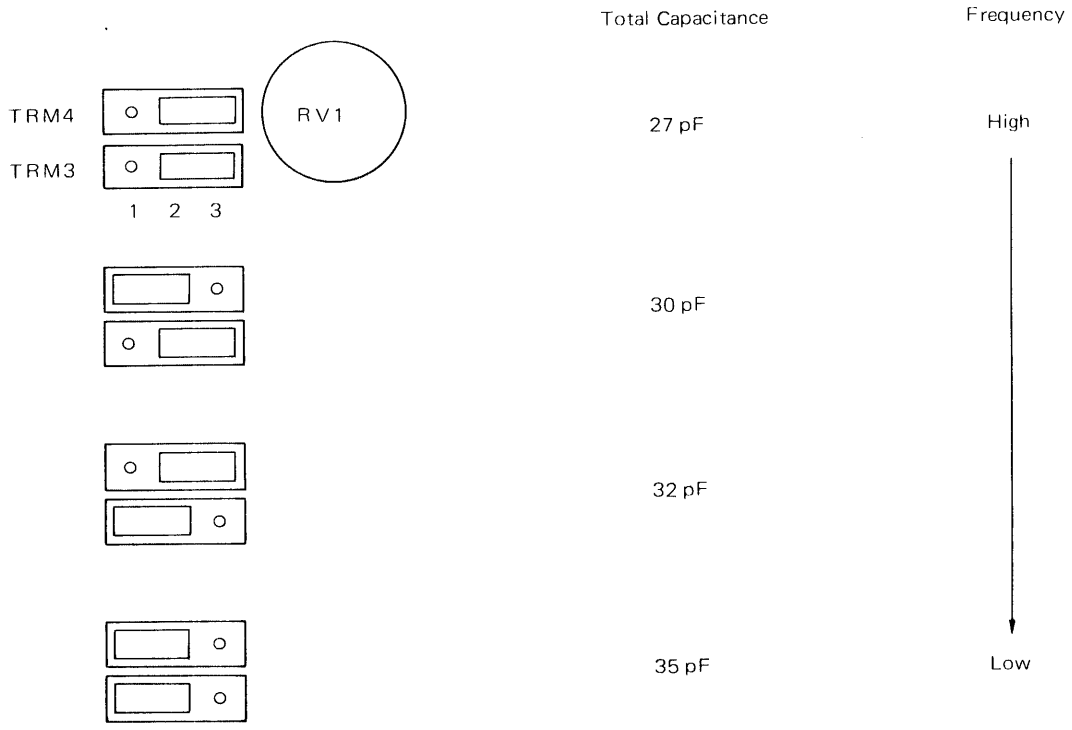


Figure 6-6-10 VFO Free-run Frequency Adjustment

(4) Timing Margin Adjustment (RV2)
Refer to Section 6.6.3.2.

6.6.4.2 CZGM PCB

(1) Write Current Adjustment (RV6)

1. Confirm that unit has a normal status.
2. Connect TP1 (WCA) to channel of oscilloscope and connect TP2 (WCB) to the other vertical input channel with invert mode set.
3. Add the two channels (differential mode).
4. Issue a write command on Cylinder 0 and Head 0.
5. Adjust potentiometer RV6 so that the difference is 400 mV ± 10 mV.

(2) Servo Pulse Window Adjustment (RV9)

1. Confirm that unit has normal status.
2. Connect the test point TRM3-10 to an oscilloscope.
3. Trigger by itself at the positive-going edge.
4. Adjust the potentiometer RV9 so that the following T_{SVP} is 320 ns ±10 ns.

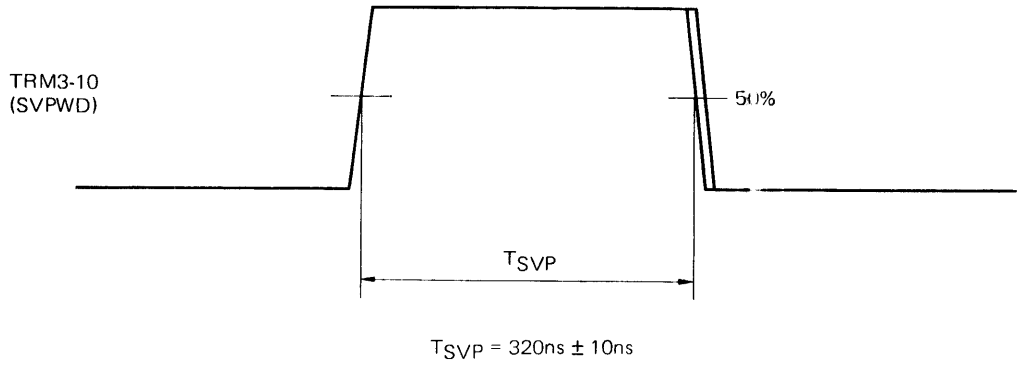


Figure 6-6-11 Servo Pulse Window Adjustment

(3) PLOSS Adjustment (RV10)

1. Confirm that unit has normal status.
2. Connect the test point TRM3-4 (PLOSS) to an oscilloscope.
3. Trigger by itself at the positive-going edge.
4. Adjust potentiometer RV10 so that the following T_{SS} is 1.5 μs ± 0.1 μs.

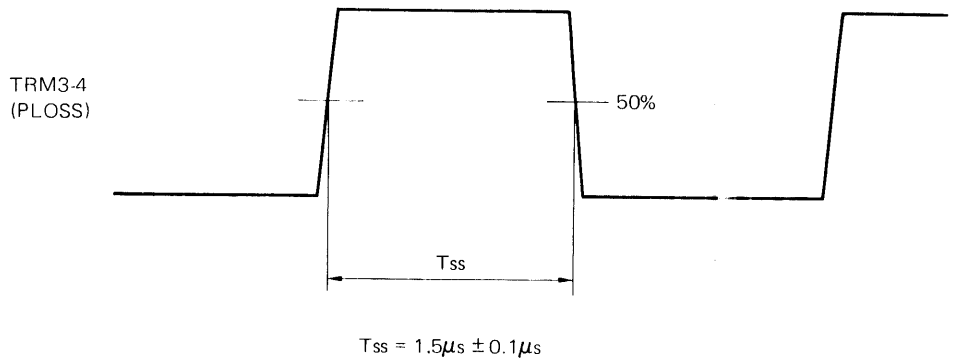


Figure 6-6-12 PLOSS Adjustment

(4) PLO Free-run Frequency Adjustment (S2, S3, RV1)

1. Turn the power off.
2. Set S1 to the off position.
3. Clamp TRM3-16 to 0V.
4. Turn the power on, and wait 40 seconds.
5. Connect test point TRM4-7 (PLOVC) to an oscilloscope (DC coupled).
6. Adjust potentiometer RV1 so that TRM4-7 signal is +2.5 V ±0.1 V.
7. Connect test point TRM4-5 (BYTCLK) to a frequency counter.
8. Select the proper capacitance as shown in Figure 6-6-13 so that the frequency of TRM4-5 is closest to 1.229 MHz as possible.

9. Finally adjust the potentiometer RV1 so that the frequency of TRM4-5 is 1.229 MHz ±2%.

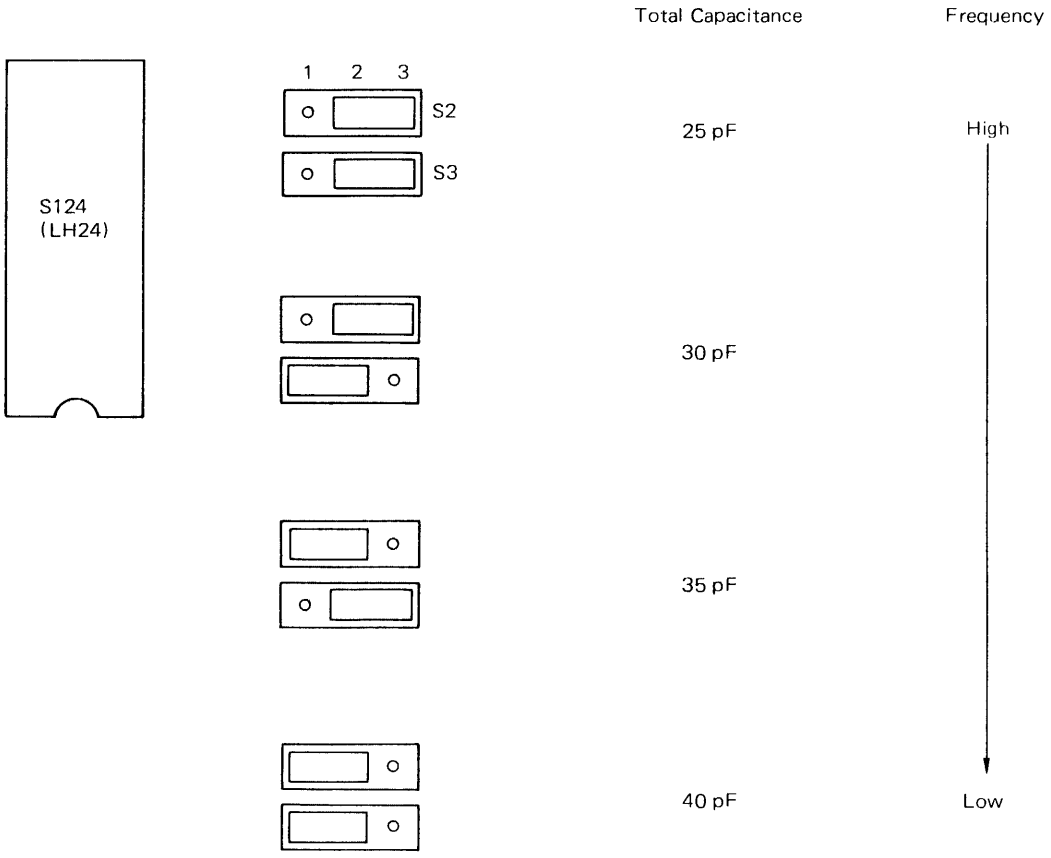


Figure 6-6-13 PLO Free-run Frequency Adjustment

(5) Velocity Offset Adjustment (RV5)
1. Confirm that unit has a normal status.
2. Connect test point TRM5-2 (–VEL) to an oscilloscope.
3. Adjust potentiometer RV5 so that TRM5-2 signal is 0 V ±50 mV with linear mode and without seek command on 0 Cylinder.

(6) DAC Output Adjustment (RV11)
1. Confirm that unit has a normal status.
2. Issue the alternate seek command between Cylinder 0 and Cylinder 822 (decimal) repeatedly.
3. Connect the test point TRM6-7 (DRLM) to an oscilloscope and trigger with positive-going edge of the signal. (DC coupled)
4. Connect the test point TRM5-5 (–DA) to the other channel at the oscilloscope. (DC coupled)
5. Adjust a potentiometer RV11 so that V_{DA} is 7.3V ± 0.3V as shown in Figure 6-6-14.

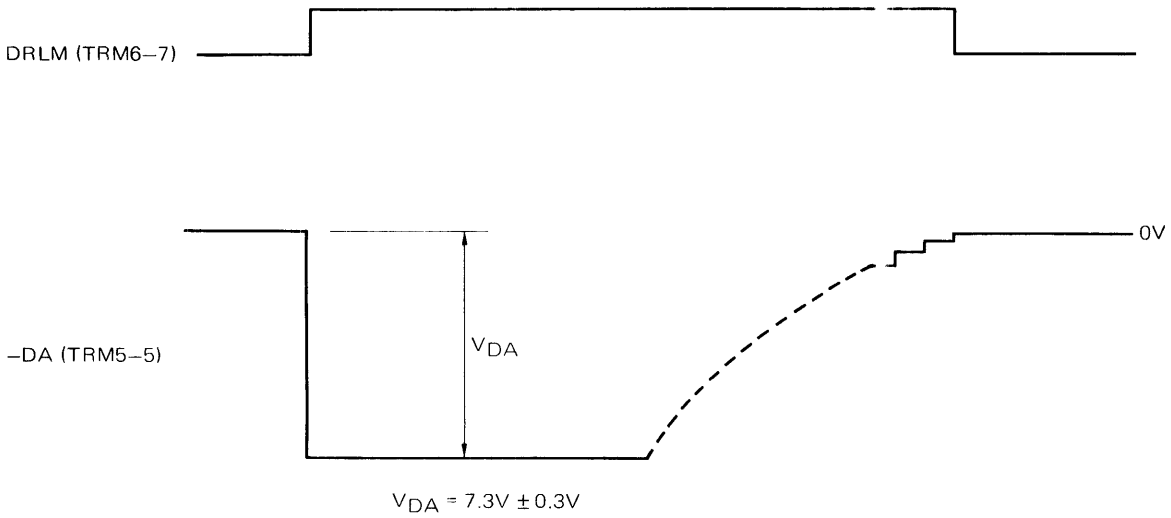


Figure 6-6-14 DAC Output Adjustment

(7) Fine Velocity Offset Adjustment (RV12)
1. Confirm that unit has a normal status.
2. Connect test point TRM5-3 (FNVEL) to an oscilloscope.
3. Adjust potentiometer RV12 so that TRM5-3 signal is 0V ± 50 mV with linear mode and without seek command on 0 cylinder.

(8) Velocity Balance Adjustment (RV7. RV8)
1. Confirm that unit has a normal status.
2. Connect test point TRM5-2 (-VEL) to an oscilloscope and check the voltage on cylinder 0 (V_0), cylinder 1 (V_1), cylinder 2 (V_2) and cylinder 3 (V_3) without seek command.
3. Adjust potentiometers RV7 and RV8 as described below.
   RV7: $V_1 - V_3 = 0mV \pm 10mV$
   RV8: $V_0 - V_2 = 0mV \pm 10mV$

6.7 Power Supply

6.7.1 General

This power supply unit needs no preventive maintenance. The only field replaceable parts are the fan and fuse. This section describes the replacement procedure for the fan and fuse.

6.7.2 General Precautions

6.7.2.1 Power On/Off

(1) Check carefully the operating condition of the unit and the drive before turning the power on and off.

(2) Always turn the power off before servicing the power supply.

6.7.2.2 Parts Replacement

(1) Always use the proper tools.

(2) Do not leave removed screws or nuts, etc. in the unit.

(3) Tighten all the screws securely.

6.7.2.3 Others

(1) Use test equipment that has been correctly calibrated.

(2) Record observed data for future reference.

6.7.3 Power Supply Spare Parts Replacement

6.7.3.1 Fuse replacement

Refer to the Figure 6.1.

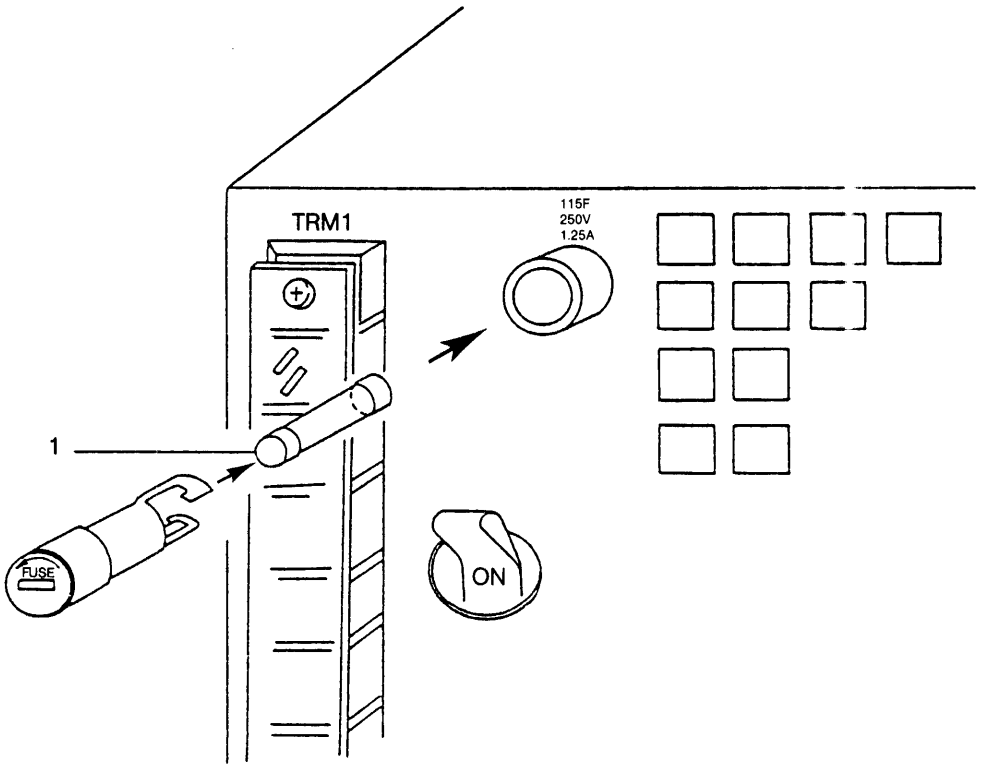


Figure 6.7.1 Fuse Replacement

6.7.3.2 Fan Replacement

(Refer to Figure 6.2.)

(1) Unfasten screws (#2) to remove the fan and the side cover.

(2) Unfasten screw (#7) to remove the grounding line.

(3) Disconnect the connector from the fan.

(4) Replace in opposite order.

6.7.3.3 Unit Test

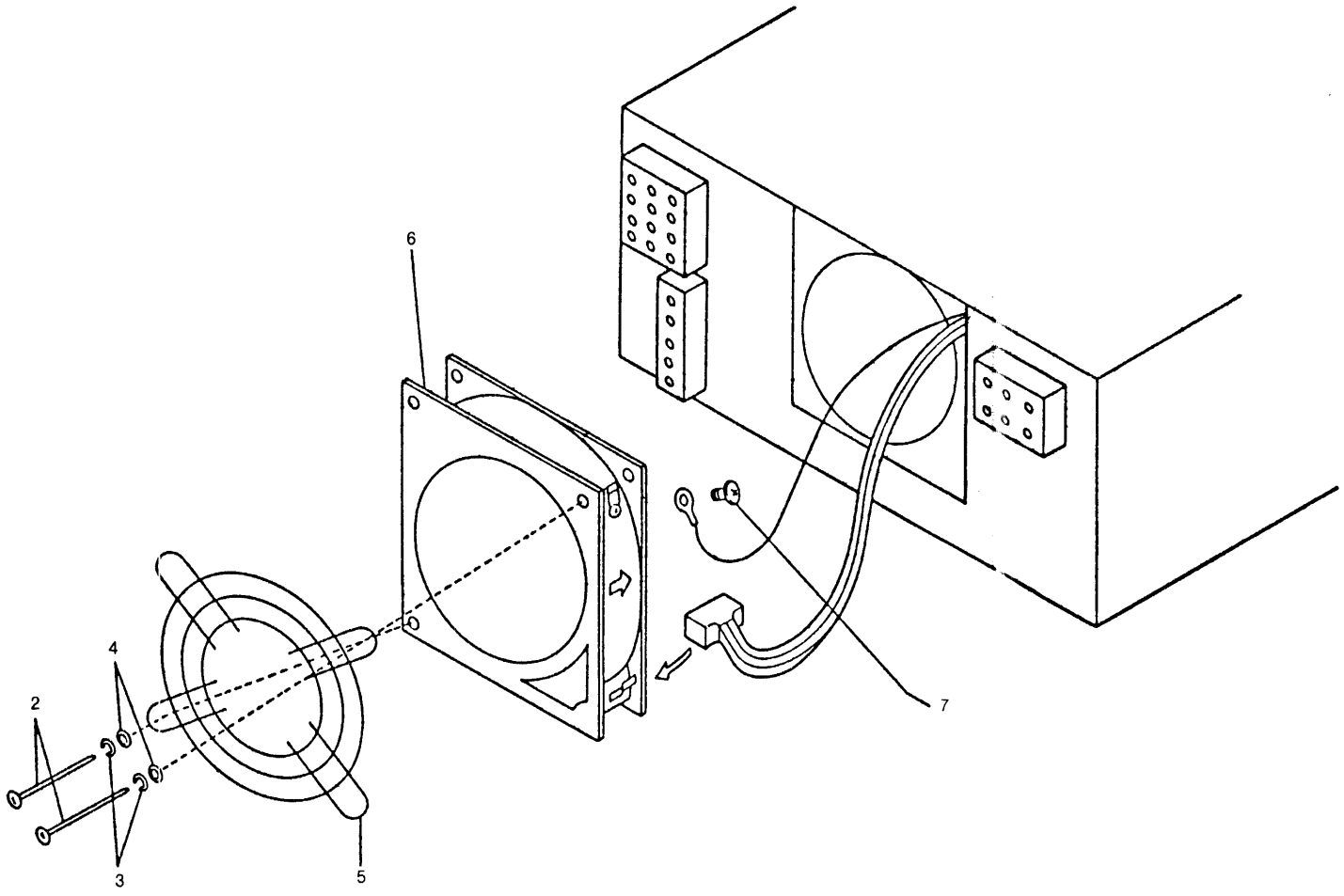
When the parts are replaced, the following checks are required.

Note: Before the checks, make sure that:
- All internal connectors are properly inserted at specified place.
- There is no foreign matter in the power unit.
- The screws and nuts are tightened securely.

(1) Measure the insulation resistance
   (a) Open the in/output connectors.
   (b) Measure the insulation resistance between the primary winding and the frame:
   500V DC (more than 10M Ohms)
   (c) Measure the insulation resistance between the secondary winding and the frame:
   100V DC (more than 5M Ohms)

(2) Power ON/OFF output voltage check
   (a) Open the output connectors.
   (b) Switch power on.
   (c) Check the output voltage from the check terminal. (Because of the no-load condition, output voltages except +5V DC will indicate a little lower than the specified.)
   (d) Confirm the rotation of the fan.

Note: Recommended test equipment
Instrument Manufacturer Spec. No.
- 500V megger Yokogawa Electric 3213-13
- 100V megger Yokogawa Electric 3213-11



NOTE: Confirm that air flows into the unit

Figure 6.7.2 Fan Replacement

6.7.4 Input Voltage Select

Remove the nameplate and select in accordance with the Figure 6.7.3.

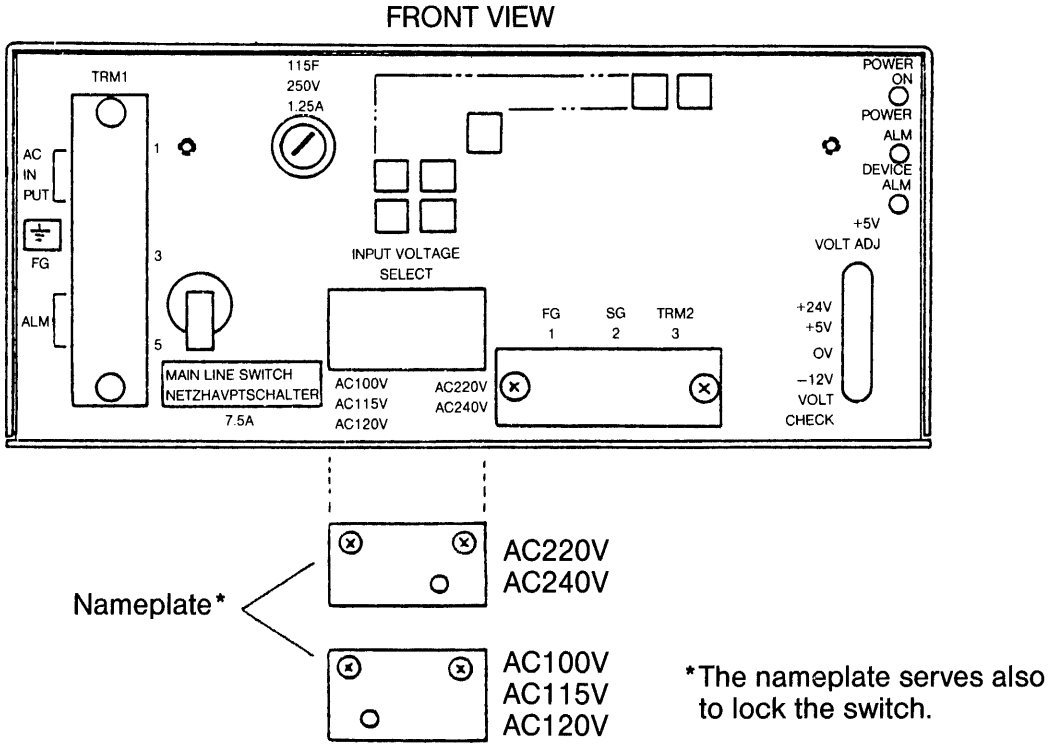


Figure 6.7.3 Input Voltage Select

Section 7

Spare Parts List

7. SPARE PARTS LIST

7.1 SPARE PARTS LIST

Refer to Table 7-1.

Table 7-1 Spare Parts List

Item	Designation	Specification
1	Controller F(CZFM) PCB Assembly	B16I 9230-0010A#U
2	Controller G(CZGM)PCM Assembly	B16I 9240-0010A#U
3	Power Amp Q(TVQM) PCB Assembly	B16I 9250-0010A#U
4	M232X C.E. Manual	B03I 4640-0111A
5	M232X Engineering Specs	B03I 4740-0101A
6	Interface Cable, Dual Port (26cm)	B66I 1060-T096
7	Interface Cable, Dual Port (16cm)	B66I 1060-T097
8	Filler Panel, Rack Mount	B03I 4590-Y514A
9	Fan Cover (TVQM)	B03I 4740-X047A
10	Vibration Stopper	B03I 4590-Y518A
11	Stopper Screw	F6-S 3D-4X16S-MNI1A
12	Stopper Bushing	F6-S K-4X12S
13	Shock Absorber	B30I 2670-0001A
14	Fan, Power Supply	CT-I N9301BW (UL)

7.2 Power Supply Spare Parts List

Table 7.2 Power Supply Spare Parts List

Item	Specifications	Description	Nickname	Quantity
1	ST4-250V-1.25A	Fuse	F1	1
2	UN3901 BW	Fan	Fan 1	1

Section 8
IC Details

8. IC DETAILS

8.1 INTRODUCTION

This section describes functions of TTL, ECL, Linear and FUJITSU Proprietary IC's.

8.2 LOGIC CONVENTIONS AND SYMBOLOGY

8.2.1 TTL Logic

M232XK Micro Disk Drive uses +5V Transistor-Transistor Logic. TTL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High = Logical "1"
Low = Logical "0"

The input/output logic of TTL are defined as follows:

(A) TTL Low Power Schottky IC Level

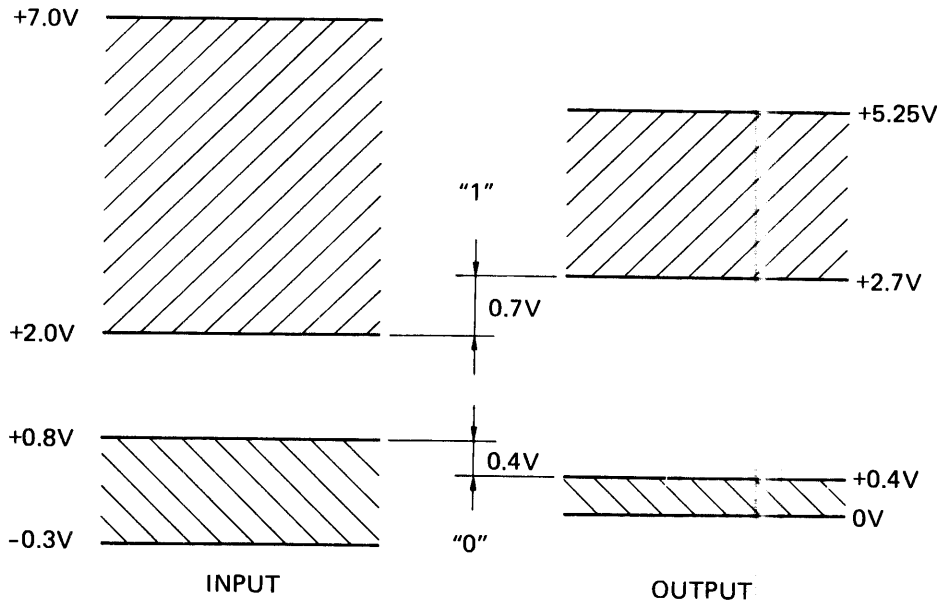


Figure 8-2-1 Low Power Schottky IC Level

(B) TTL Schottley IC Level

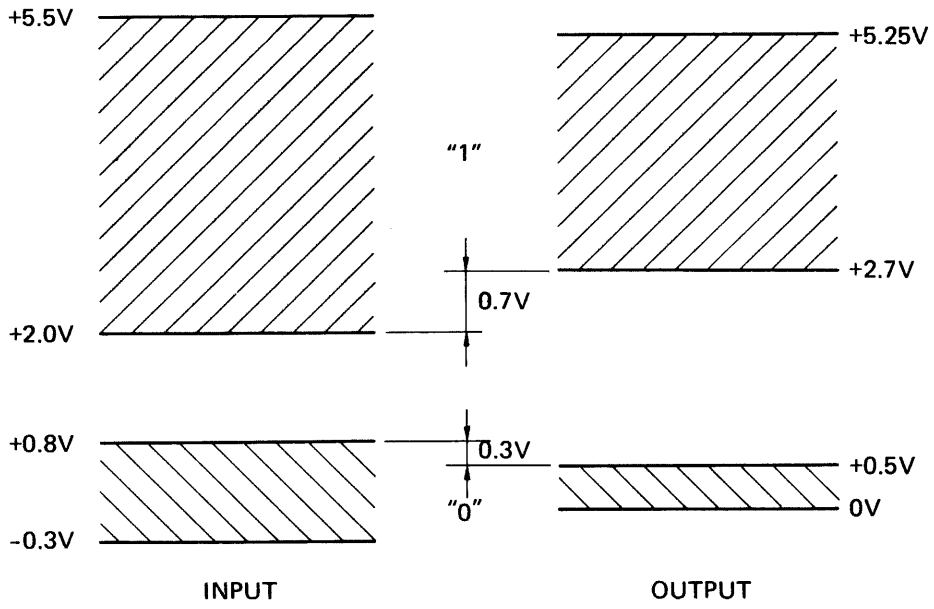


Figure 8-2-2 TTL Schottky IC Level

8.2.2 ECL Logic

M232XK Mirco Disk Drive uses −5.2V ECL (Emitter-Coupled-Logic). The high impedance of the logic (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high DC fan-out.

High-speed operation and high fan-out is possible because all circuits are designed to operate in a 50 ohm system. Complementary outputs cause a function and its complement to appear simultaneously at the device output, without the use of external inverters. In a M232X each output is terminated by resistors. ECL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High = Logical "1"
Low = Logical "0"

The input/output logic levels of ECL are defined as follows:

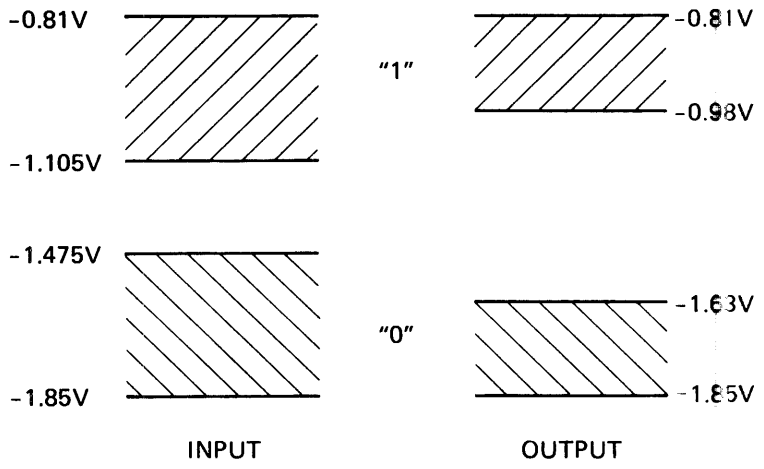
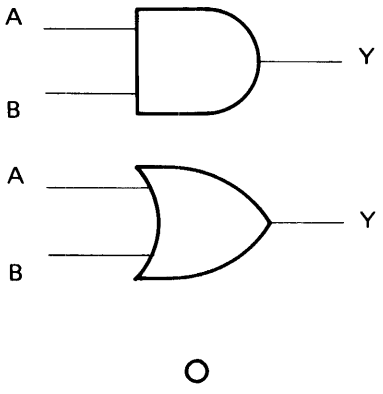


Figure 8-2-3 ECL Logic Level

8.2.3 Logic Symbology

The following conventions are provided to aid in understanding the symbology used in this manual.

1) TTL



This indicates AND gate.

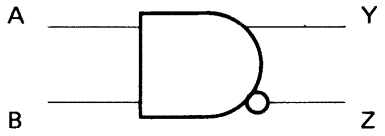
$Y = A \cdot B$

This indicates OR gate.

$Y = A+B$

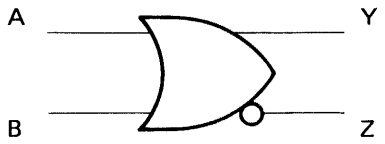
A circle placed on any input line or on the output line indicates that logical "0" is the significant state.
The absence of a circle, "1" is the significant state.

2) ECL



This indicates AND/NAND Gate.

$Y = A \cdot B = \overline{Z}$



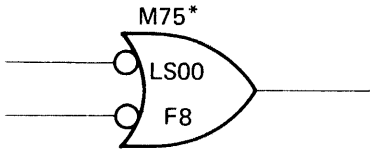
This indicates OR/NOR gate.

$Y = A + B = \overline{Z}$

This is equivalent to TTL.

3) All logic symbols on each logic diagram are identified by a sequential numbering and element type code.

For example:



M75* : Sequential part number ON the parts list.
LS00 : Abbreviation (marking) of the element code.
F8 : Physical location of element on P.C.B. assembly.

8.3 IC INTERCHANGEABILITY GUIDE

8.3.1 TTL IC Interchangeability

Table 8-3-1 TTL Interchangeability

FUJITSU		Direct Replacement	Functions	Q'ty	Page
Part Number	Code				
MB74LS00M	LS00	SN74LS00N	Quad 2-input NAND	12	
MB74LS02M	LS02	SN74LS02N	Quad 2-input NOR	8	
MB74LS04M	LS04	SN74LS04N	Hex Inverter	16	
MB74LS05M	LS05	SN74LS05N	Hex Inverter with Open Collector	1	
MB74LS08M	LS08	SN74LS08N	Quad 2-input AND	9	
MB74LS10M	LS10	SN74LS10N	Triple 3-input NAND	5	
MB74LS11M	LS11	SN74LS11N	Triple 3-input AND	3	
MB74LS14M	LS14	SN74LS14N	Hex Schmitt-Triggered Inverter	1	
MB74LS20M	LS20	SN74LS20N	Dual 4-input NAND	1	
MB74LS27M	LS27	SN74LS27N	Triple 3-input NOR	4	
MB74LS32M	LS32	SN74LS32N	Quad 2-input OR	4	

Table 8-3-1 TTL Interchangeability (Continued)

FUJITSU		Direct Replacement	Functions	Q'ty	Remark
Part Number	Code				
MB74LS37M	LS37	SN74LS37N	Quad 2-input NAND Buffer	8	
MB74LS42M	LS42	SN74LS42N	4-line-to-10-line Decoder	3	
MB74LS51M	LS51	SN74LS51N	Dual 2-wide 2-input AND-OR-INVERT	2	
MB74LS54M	LS54	SN74LS54N	4-wide AND-OR-INVERT	4	
MB74LS74AM	LS74	SN74LS74AN	Dual D-type Positive-Edge-Trigger d Flip-Flop	9	
MB74LS85M	LS85	SN74LS85N	4-bit Magnitude Comparator	4	
MB74LS86M	LS86	SN74LS86N	Quad 2-input EOR	3	
–	LS123	SN74LS123N	Dual Retrigerable Monostable Multivibrator with Clear	1	
MB74LS148M	LS148	SN74LS148N	8-to-3 Priority Encoder	3	
MB74LS153M	LS153	SN74LS153N	Dual 4-line-to-1-line Data Selector/Multiplexer	5	
MB74LS161AM	LS161	SN74LS161AN	4-bit Binary Counter	15	
MB74LS164M	LS164	SN74LS164N	8-bit Shift Register	1	
MB74LS174M	LS174	SN74LS174N	Hex D-type Flip-Flop	2	
MB74LS175M	LS175	SN74LS175N	Quad D-type Flip-Flop	7	
MB74LS191M	LS191	SN74LS191N	4-bit Binary Up/Down Counter	3	
–	LS221	SN74LS221N	Dual Monostable Multivibrator with Clear	4	
–	LS279	SN74LS279N	Quad S-R Latch	5	
MB74LS283M	LS283	SN74LS283N	4-bit Full Adder	3	
–	LS393	SN74LS393N	Dual 4-bit Binary Counters	3	
MB434M	434	SN75451BP	Dual 2-input AND Buffer with Open-collector	7	
MB436M	436	SN75453BP	Dual 2-input OR Buffer with Open-collector	1	
MB463M	463	–	Quad 2-input NAND with Open-collector	1	
–	LX16	SN75452BP	Dual 2-input NAND Buffer with Open-collector	5	
MB84020BM	4020	MC14020BCP	14-Bit Binary Counter	1	
MB74S00M	LH01	SN74S00N	Quad 2-input NAND	2	
MB74S04M	LH04	SN74S04N	Hex Inverter	7	
MB74S08M	S08	SN74S08N	Quad 2-input AND	1	
–	LH10	SN74S112N	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear	1	
–	LH24	SN74S124N	Dual VCO	1	

Note 1) Direct Replacement is a device from Texam Instruments Inc. except 4020.
2) Direct Replacement of 4020 is a device from MOTOROLA Semiconductor P oduct Inc.

8.3.2 ECL IC Interchangeability

Table 8-3-2 ECL Interchangeability

FUJITSU		Direct Replacement	Functions	Q'ty	Remark
Part Number	Code				
MB10102C	102	MC10102L	Quadruple 2-input NOR	3	
MB10105C	105	MC10105L	Triple 2-3-2 Input OR/NOR	4	
MB10109C	109	MC10109L		1	
MB10115C	115	NC10115L	Quad Receiver	1	
MB10116C	116	MC10116L	Triple Receiver	5	
MB10124C	124	MC10124L	Quadruple TTL to ECL Translator	3	
MB10125C	125	MC10125L	Quadruple ECL to TTL Translator	1	
MB10131C	131	MC10131L	Dual D-type Master-Slave Flip-Flop	6	

Note: Direct replacement is a device from MOTOROLA Semiconductor Product Inc.

8.3.3 Linear IC Interchangeability

Table 8-3-3 Linear IC Interchangeability

FUJITSU		Direct Replacement	Functions	Q'ty	Remark
Part Number	Code				
MB3607M	A1458	μPC251C (NEC)	Dual 741-type Operational Amplifier	15	
MB4002M	A4002		High Speed Voltage Comparator	1	
	A311	μPC271C (NEC)	311-type Voltage Comparator	20	
	A082	HA17082PS (HITACHI)	082-type-J-FET Dual Operational Amplifier	5	
	A399	μPC177C (NEC)	339-type Voltage Comparator	1	
	A610	μPC610D (NEC)	8-bit D/A Converter	1	
	A201	DG201BK (Siliconix)	Quad SPST Analog Switch	7	
	A7812	μPC14312H (NEC)	7812-type +12V Regulator	1	
	A7952	μPC16352H (NEC)	7952-type −5.2V Regulator	1	
	3450	MC3450L (MOTOROLA)	Quad Line Receiver	5	
	75108A	SN75108AN (T1)	Dual Line Receiver with Open-collector	2	
	75110	SN75110AN (T1)	Dual Line Driver	8	

8.3.4 FUJITSU Proprietary IC

Table 8-3-4 FUJITSU Proprietary IC List

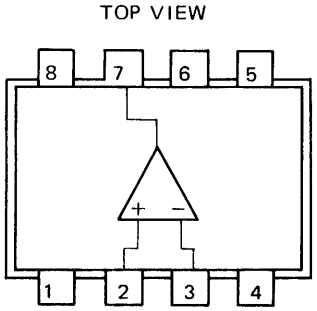
FUJITSU		Classification	Functions	Q'ty	Remark
Part Number	Code				
MB4303C	A4303	Analog Master-Slice	AGC Amplifier	2	
MB4311C	A4311	Analog Master-Slice	Peak Detector	1	
MB4316C	A4316	Analog Master-Slice	Read/Write Bus Switch	1	
MB4319C	A4319	Analog Master-Slice	Peak Hold	1	
MB4320C	A4320	Analog Master-Slice	Pulse Shaper	1	
MB15207C	15207	Bipolar 500-gate	MFM Encoder/Decoder	1	
MB15238C	15238	Bipolar 500-gate	Servo Control Logic	1	
	DV18	Hybrid IC	Clock Driver	1	

8.4 FUJITSU PROPRIETARY IC DETAIL

(1) MB4002M

High Speed Differential Comparator

The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

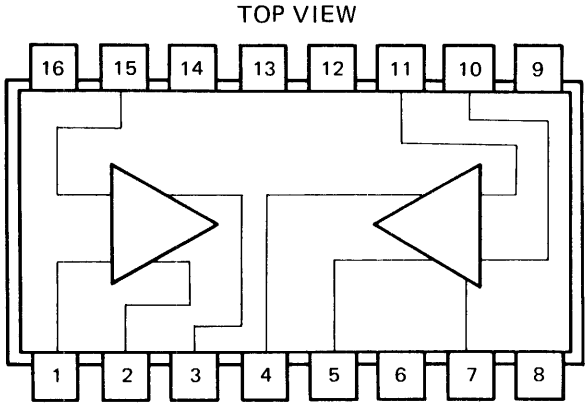


1: GND
2: INPUT (+)
3: INPUT (−)
4: V^-
5: NC
6: NC
7: OUTPUT
8: V^+

(2) MB4303C

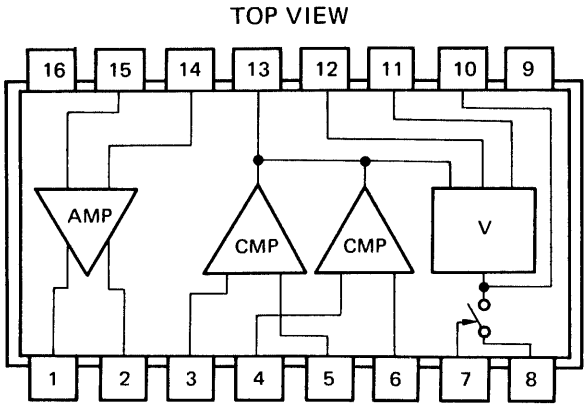
AGC Amplifier

The MB4303C is a Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.



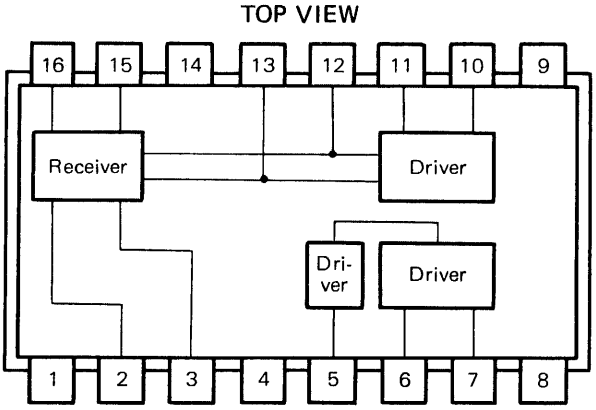
1: INPUT2
2: OUTPUT2
3: OUTPUT2
4: OUTPUT1
5: OUTPUT1
6: VR
7: VAGC
8: VG (GND)
9: Vee
10: INPUT1
11: INPUT1
12: GA
13: GB
14: VBB
15: INPUT2
16: Vcc

(3) MB4311C
Peak Detector



1: OUT1
2: OUT1
3: IN2
4: IN2
5: VH
6: VL
7: SQ
8: GND
9: Vee
10: AGCG
11: CLA
12: CAP
13: VAGC
14: IN1
15: IN1
16: Vcc

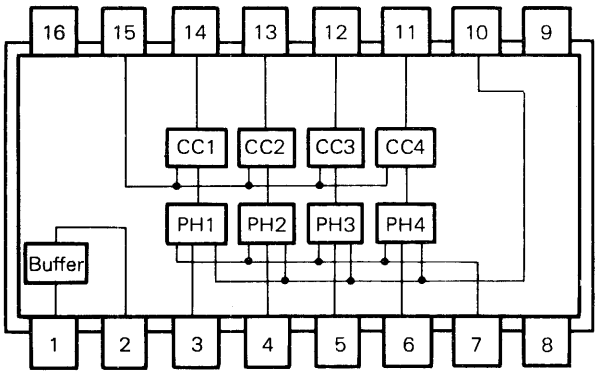
(4) MB4316C
Read/Write Bus Switch



1: Vee2
2: GAN2
3: GAN1
4: IN5
5: IN4
6: OUT5
7: OUT6
8: GND
9: Vee1
10: IN2
11: IN3
12: OUT4
13: OUT3
14: IN1
15: OUT2
16: OUT1

(5) MB4319C
Peak Hold

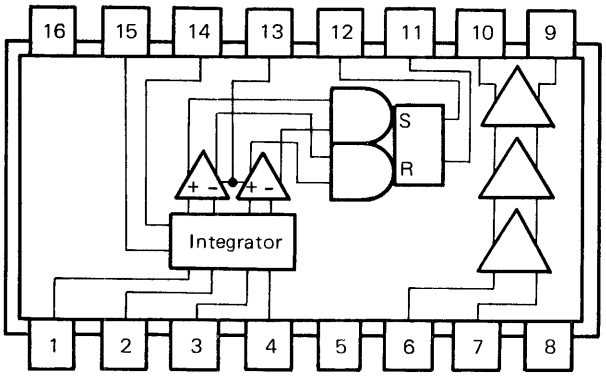
TOP VIEW



1: REG1
2: VELOCITY
3: *GATE1
4: *GATE2
5: *GATE3
6: *GATE4
7: CARIE
8: GND
9: VEE
10: REG3
11: EVEN2
12: ODD2
13: EVEN1
14: ODD1
15: REG2
16: Vcc

PH: Peak Hold
CC: Constant Current

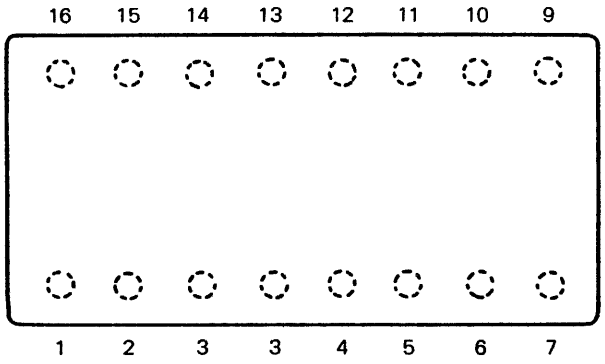
(6) MB4320C
Pulse Shaper



1: RDX1
2: RDX2
3: RDY1
4: RDY2
5: VEE
6: RDA
7: RDB
8: GND
9: OUT4
10: OUT3
11: OUT2
12: OUT1
13: VDX
14: CEY
15: CEX
16: Vcc

(7) DV18

Clock Driver



1: N.C.
2: ENB
3: X_{E1}
4: N.C.
5: N.C.
6: N.C.
7: X_{EZ}
8: GND
9: N.C.
10: N.C.
11: N.C.
12: N.C.
13: OUT
14: N.C.
15: Vcc
16: N.C.

(8) MB15207C (Bipolar 500 Gates LSI)

This LSI has the following functions.

- NRZ to MFM Encoder with Write Compensation
- MFM to NRZ Decoder (not used)
- PLO/VFO Phase Comparator (not used)
- Physical Index Detector (not used)
- Fault Detector

The package of B500 LSI is shown in Figure 8-4-1, the pin assignment is shown in Table 8-4-1, and the block diagram is shown in Figure 8-4-2.

(RIT 64)

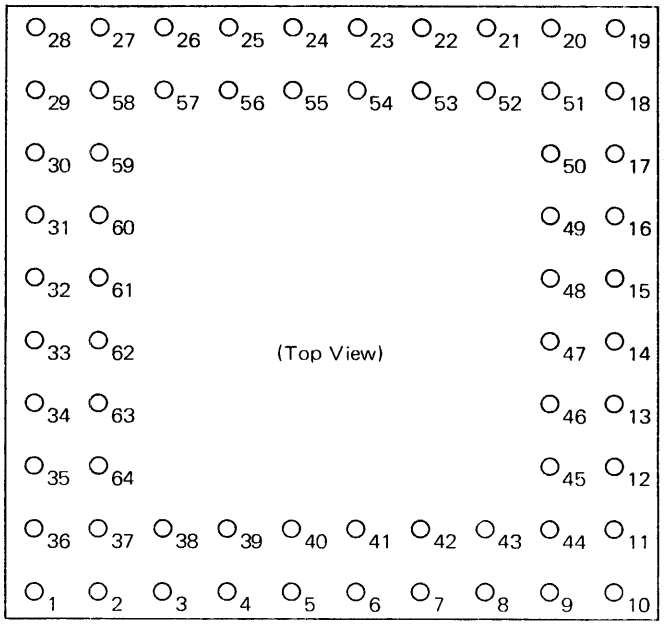


Figure 8-4-1 B500 LSI Package

Table 8-4-1 MB15207C Pin Assignment

Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal
1	NC		17	I	PWRDY1 (RTRY2)	33	I	VF02F (ONT)	49	O	NC (GATES)
2	O	NC (*PDEC)	18	I	SVCLK (CLK11)	34	I	WDAT (WDT)	50	O	*USFCL (RTRY1)
3	O	NC (1P8)	19	I	OSCLK (DLYCL)	35	I	GND (PSWCL)	51	I	GND (CLK10)
4	NC		20	I	GND (FMD)	36	O	NC (PSWDT)	52	I	*TRWD (INX)
5	I	TUP (RDYIN)	21	O	NC (PCL)	37	I	GND (*DIAG)	53	O	NC (RDDT)
6	I	GND (CPL)	22	O	NC (WIN)	38	O	NC (PINC)	54	VDD	GND
7	I	GND (1P16I)	23	I	GND (*GAP00)	39	O	NC (1P16)	55	I	TUP (V2F)
8	I	TUP (*CLPLS)	24	I	GND (*DTCL)	40	VDD	GND	56	I	TUP (VF02F)
9	O	NC (PINX)	25	I	GND (*RDMSK)	41	I	GND (*CPL)	57	I	TUP (*VFOD1)
10	I	*RGC (SKCT)	26	I	TUP (*VFOD2)	42	I	PWRDY1 (*CLR)	58	I	GND (RGT)
11	O	SCTCK2 (ERROR)	27	I	GND (RAWDT)	43	I	TUP (1P16F)	59	O	NC (LOCK)
12	I	SKERR (MLTSL)	28	I	GND (PLOSW)	44	NC		60	O	NC (*VFODO)
13	I	RG.SKER (UNS)	29	O	NC (VINC)	45	O	NC (*FAULT)	61	VSS	+5V
14	I	*OFACT (RLCT)	30	O	NC (*VDEC)	46	I	VF02F (P2F)	62	I	VFO2F (LTT)
15	I	WGC (WGT)	31	I	OTZN (DLYSW)	47	VSS	+5V	63	I	*WCL (WCL)
16	O	DPWRDY1 (READY)	32	I	VF02F (ELT)	48	I	GND (FCLR)	64	O	ECWD (WDTP)

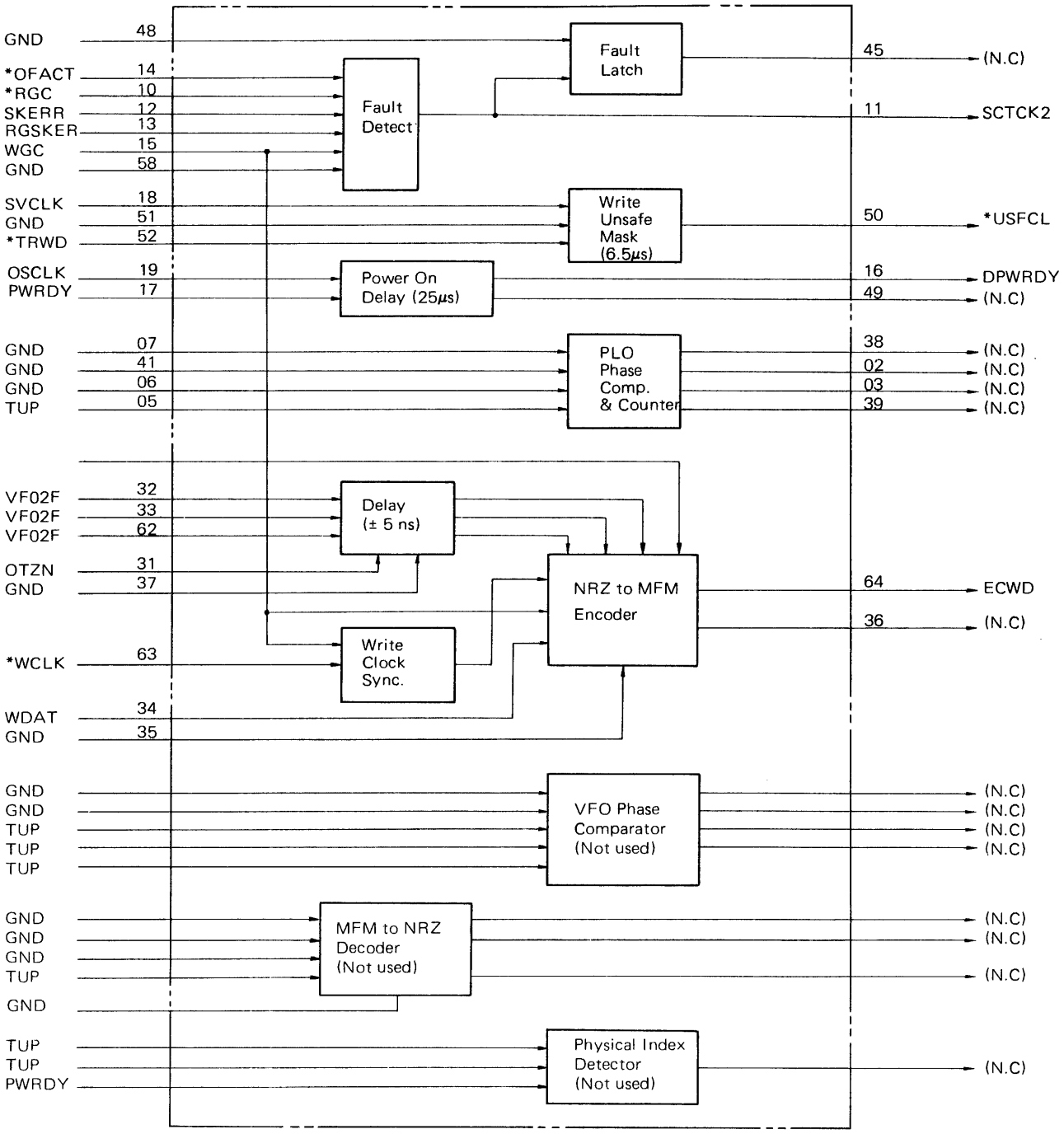


Figure 8-4-2 MB15207C Block Diagram

(9) MB15238C (Bipolar 500 Gates LSI)

This LSI has the following functions.

- PLO Latch
- Divide and Timing Counter
- Peak Hold Gate Decoder
- Index/Guard Band Pattern Decoder
- Guard Band Detector with Counter
- Polarity Control Gates Decoder
- 2-bit Full Adder

The package of B500 LSI is shown in Figure 8-4-1, the pin assignment is shown in Table 8-4-2, and the block diagram is shown in Figure 8-4-3.

Table 8-4-2 MB15238C Pin Assignment

Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal
1	NC		17	O	* SQN	33	O	* CNT15	49	O	* SQI
2	O	PLOCLK	18	O	* INX	34	I	*OGBQ	50	O	* FIGB1
3	O	* GT1	19	I	* CAR1	35	O	CT7	51	I	NGTQ
4	O	* CT15	20	O	* OINX	36	I	VCO2	52	O	* MSDT
5	O	* GT4	21	O	* SNI	37	NC		53	O	* EINX
6	O	* GT3	22	O	* RSTGB	38	I	PWRDY	54	V	GND
7	O	PLOLT	23	O	CNT4	39	O	CT8F	55	O	* SNN
8	O	* OGBP	24	O	* EQUAL	40		GND	56	O	XPL
9	O	SFRGA	25	O	* PCLMP	41	O	* GT2	57	I	* OFTRK
10	I	* SEL1F	26	O	* MCLMP	42	O	* PLOLT	58	I	* SVPMS
11	O	SFRGE	27	O	* PAR1	43	O	* IGBIP	59	O	* IGB1
12	O	CNT1	28	I	* SKC	44	NC		60	I	* IGB2Q
13	I	* RSTGB	29	O	* OGB	45	O	* IGB2P	61	VSS	+5V
14	I	* HDLD	30	O	* IGB2	46	I	CNT7	62	I	VCO1
15	I	NQGTZ	31	I	* IGB1Q	47	V	+5V	63	O	CNT64
16	I	* CAR2	32	I	* MSDT	48	I	* PLOLT	64	I	PLOLT

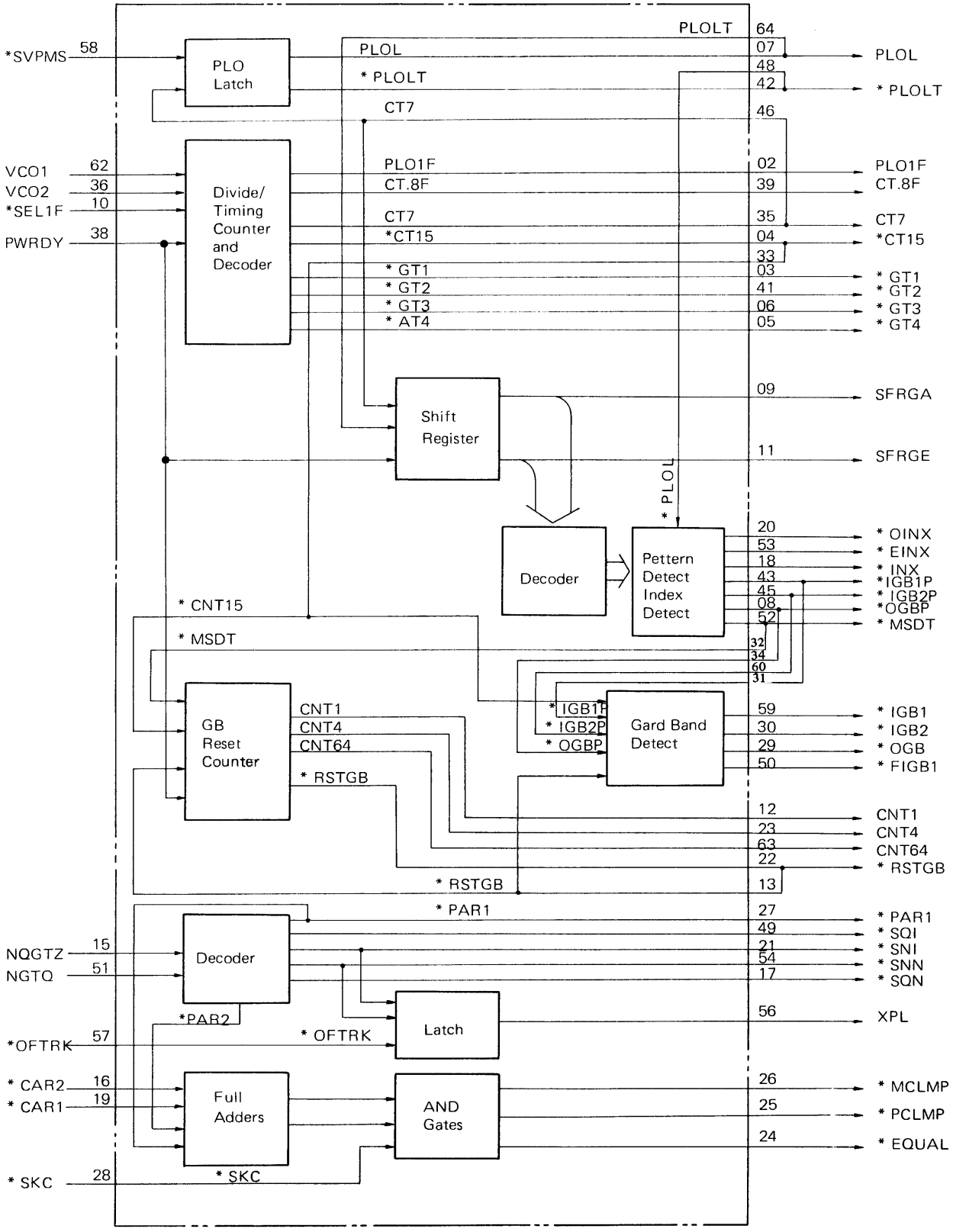


Figure 8-4-3 MB15238C Block Diagram

Section 9

Parts List

9. PARTS LIST

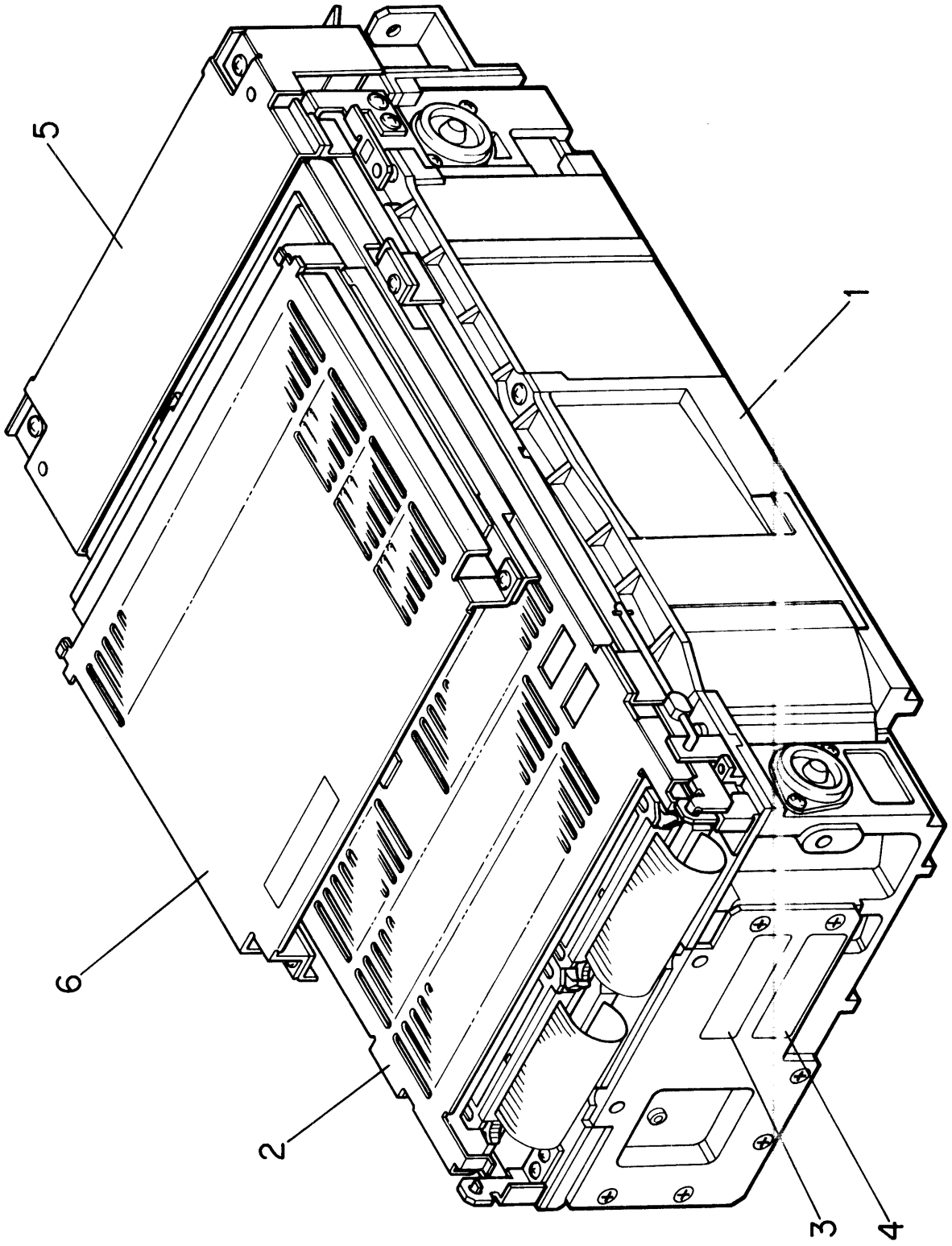


Figure 9-1 M2321K/M2322K Micro Disk Drive

Table 9-1 M2321K/M2322K Micro Disk Drive

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B–4745–B001A	M2321K Micro-Disk Drive			
	1	B03B–4745–B002A	M2322K Micro-Disk Drive			
1	1	B030–4740–T001A	M2321K Disk Drive Unit			
1	1	B030–4740–T002A	M2322K Disk Drive Unit			
2	1	B030–4740–V301A	Frame Unit			
3	1	C370–1270–0002	Manufacturing Name Label			
4	1	C370–1270–0003	Revision Label			
5	1	B03B–4740–E002A	Fan Unit (AC 115V) Option			
5	1	B030–4740–E005A	(DC 24V) Option			
6	1	B03B–4740–E402A	Dual Channel Option			

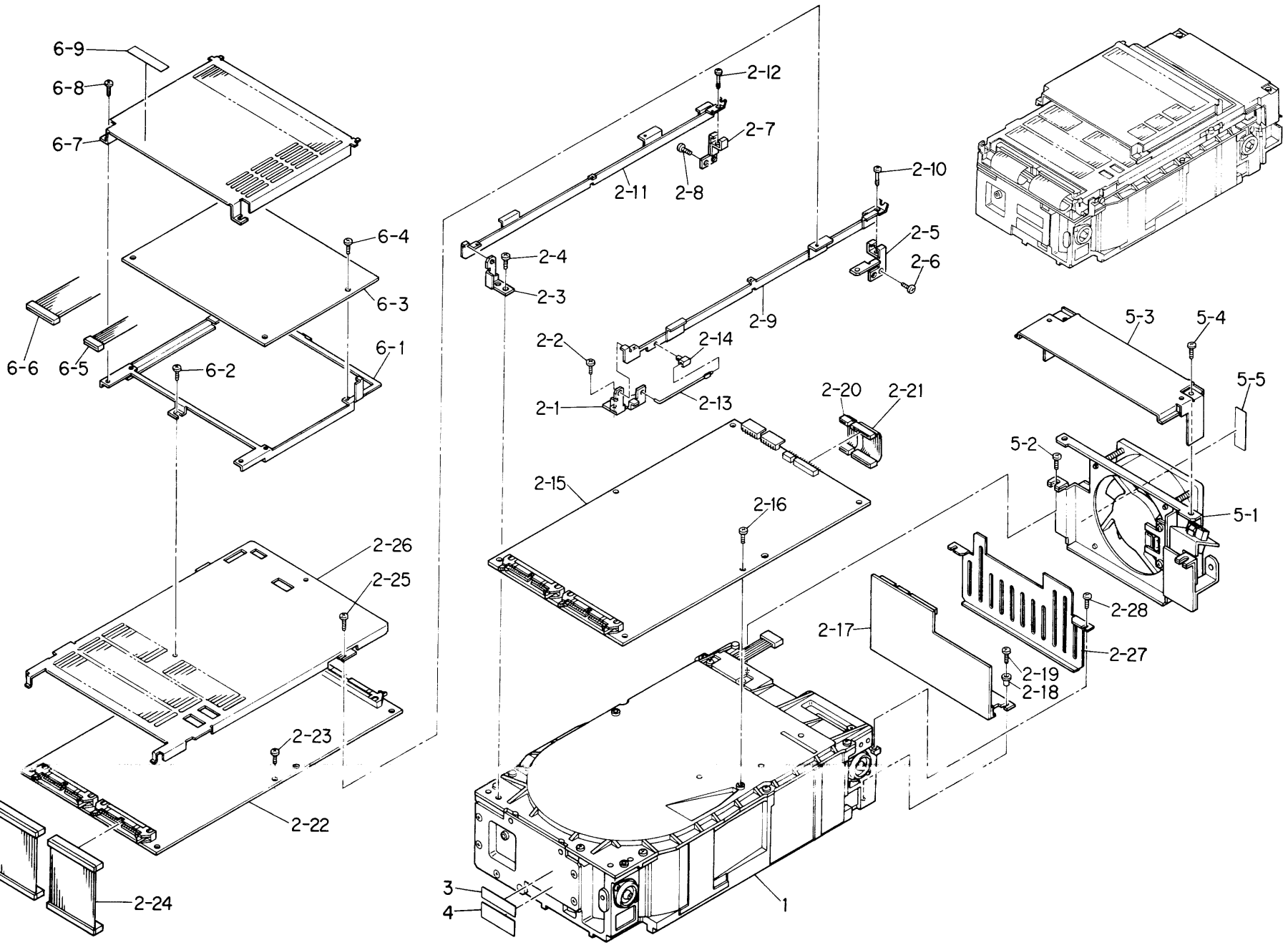


Figure 9-2 Frame Unit (1/2)

Table 9-2 Frame Unit (Basic)

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
1	1	B030–4740–T001A	M2321K Disk Drive Unit			
1	1	B030–4740–T002A	M2322K Disk Drive Unit			
2	1	B030–4740–V301A	Frame Unit			
2-1	1	B030–4740–X310A	Plate			
2-2	2	F6–SBD–4x6S–M–NI1A	Screw			
2-3	1	B030–4740–X309A	Plate			
2-4	2	F6–SBD–4x6S–M–NI1A	Screw			
2-5	1	B030–4740–W304A	Stopper			
2-6	2	F6–SBD–4x8S–M–NI1A	Screw			
2-7	1	B030–4740–W305A	Stopper			
2-8	2	F6–SBD–4x8S–M–NI1A	Screw			
2-9	1	B030–4740–W308A	Frame Assy.			
2-10	1	C300–0010–X176	Screw			
2-11	1	B030–4740–W309A	Frame Assy.			
2-12	1	C300–0010–X176	Screw			
2-13	1	B030–4740–X312A	Hinge			
2-14	1	B030–4740–X311A	Stopper			
2-15	1	B16B–9240–0010A#U	Controller G			
2-16	6	F6–SBD–4x6S–M–NI1A	Screw			
2-17	1	B16B–9250–0010A#U	Power Amplifier Q			
2-18	2	B030–4740–X046A	Bushing			
2-19	2	F6–SBD–3x8S–M–NI1A	Screw			
2-20	1	B660–0625–T318A	Cable			
2-21	1	B660–0625–T319A	Cable			
2-22	1	B16B–9230–0010A#U	Controller F			
2-23	6	F6–SBD–3x6S–M–NI1A	Screw			
2-24	2	B660–1990–T036A#L70R00	Cable			
2-25	2	F6–SBD–3x6S–M–NI1A	Screw			
2-26	1	B030–4740–X313A	Cover			
2-27	1	B030–4740–X047A	Cover			
2-28	2	F6–SBD–4x6S–M–MI1A	Screw			
3	1	C370–1270–0002A	Nameplate			
4	1	C370–1270–0003A	Revision Label			

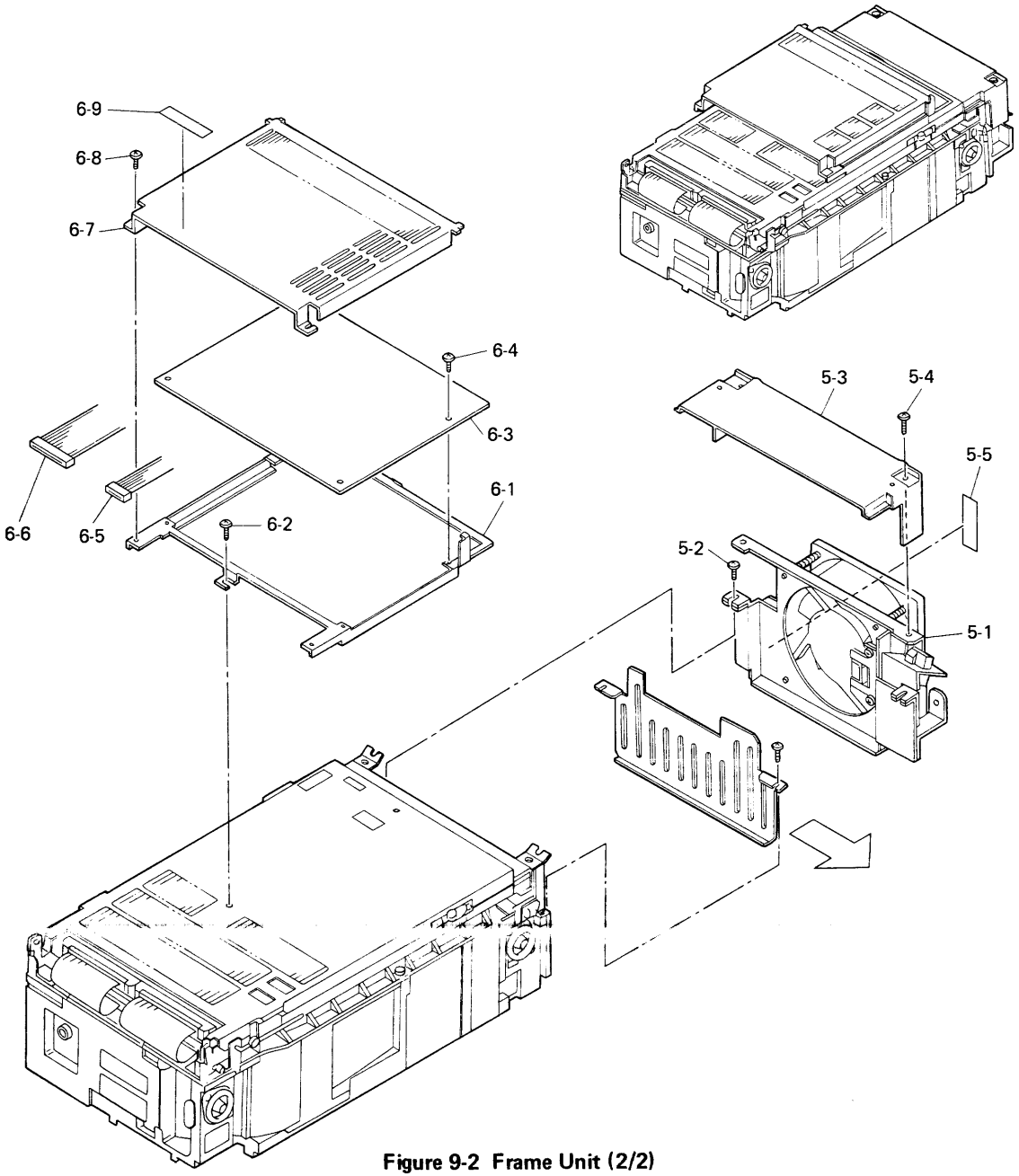


Figure 9-2 Frame Unit (2/2)

Table 9-2 Frame Unit (Option)

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
5	1 1	B03B–4740–E002A	Fan Unit			
5	1 1	B03B–4740–E004A	Fan Unit			
5-1	1	B030–4740–T201A	Fan Assy.			
5-2	1	F6–SBD–4x8S–M–NI1A	Screw			
5-3	1	B030–4740–W204A	Retainer			
5-4		F6–SBD–4x10S–M–NI1A	Screw			
5-5		B370–0950–0409A	Label			
	1					
6	1 1	B03B–4740–E402A	Dual Channel			
6-1	1	B030–4740–X401A	Frame			
6-2	1	F6–SBD–3x6S–M–NI1A	Screw			
6-3	4	B16B–7990–0060A#U	Crosscall D			
6-4	1	F6–SBD–3x5S–M–NI1A	Screw			
6-5	1	B660–1060–T096A#L280R0	Cable			
6-6	1	B660–1060–T097A#L300R0	Cable			
6-7	1	B030–4740–X404A	Cover			
6-8		F6–SBD–3x6S–M–NI1A	Screw			
6-9		B370–0950–0414A	Label			

Section10
Schematics

10. SCHEMATICS

10.1 BASIC SCHEMATICS

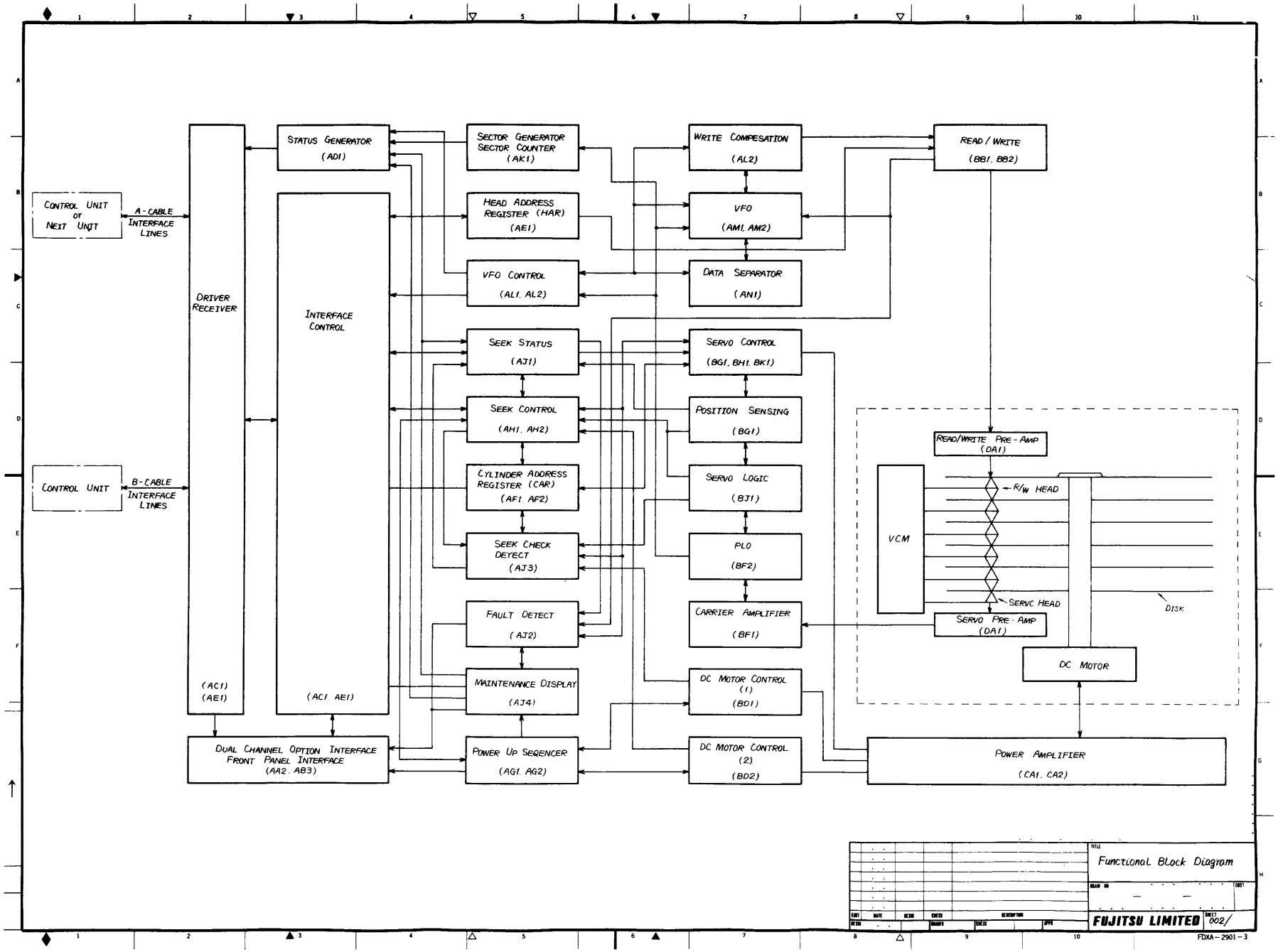
SHEET	ABBR	TITLE
001		Schematics/Drawings List
002		Functional Block Diagram
003	AA1	Interface Connection/Line Termination
004	AA2	Connection With CZGM PCA/ Dual Channel Connection
005	AB1	A-Cable Signal Receivers
006	AB2	A/B-Cable Signal Drivers
007	AB3	Wired-AND With Dual Channel Option
008	AC1	Unit Selection
009	AD1	Status Multiplexer
010	AE1	Command Decoder/ Head Address Register
011	AF1	Next/Present Cylinder Address Register
012	AF2	Difference Counter
013	AG1	Power Up Sequencer (1)
014	AG2	Power Up Sequencer (2)
015	AH1	Seek Control Latches (1)
016	AH2	Seek Control Latches (2)
017	AJ1	Seek Status Generator
018	AJ2	Fault Detect
019	AJ3	Seek Check Detect
020	AJ4	Maintenance Display
021	AK1	Sector Generator/ Sector Counter
022	AL1	VFO Control
023	AL2	VFO Control
024	AM1	VFO Phase Comparator
025	AM2	VFO Charge Pump and VCO
026	AM3	VFO Data Separator
027	AN1	IC Power Supply
028	BA1	Connection With CZFM PCA/ TIXM and TVQMPCA's
029	BB1	R/W Bus Switch/ Head and Chip Secection
030	BB2	AGC Amplifier/Pulse Shaper
031	BC1	HIC Power Supply
032	BD1	DC Motor Control (1)
033	BD2	DC Motor Control (2)
034	BE1	Power Ready Detector
035	BF1	~~Carrier Amplifier~~ PLO Phase Comparator
036	BF2	PLO Charge Pump and VCO/DAC
037	BG1	Position Sensing
038	BG2	Velocity Generator/ Fine Position Detect
039	BH1	Error Amplifier
040	BJ1	Servo Control Logic
041	BK1	Servo Power Amplifier Drive
042	CA1	DC Motor Power Amplifier
043	CA2	Servo Power Amplifier
044	DA1	Connection With CZGM and Head IC Data Servo Head IC
045	EA1	I/O Connectors of Acc PCA's
046		CZFM PCB Assembly
047		CZGM PCB Assembly
048		TVQM PCB Assembly
049		Power Supply

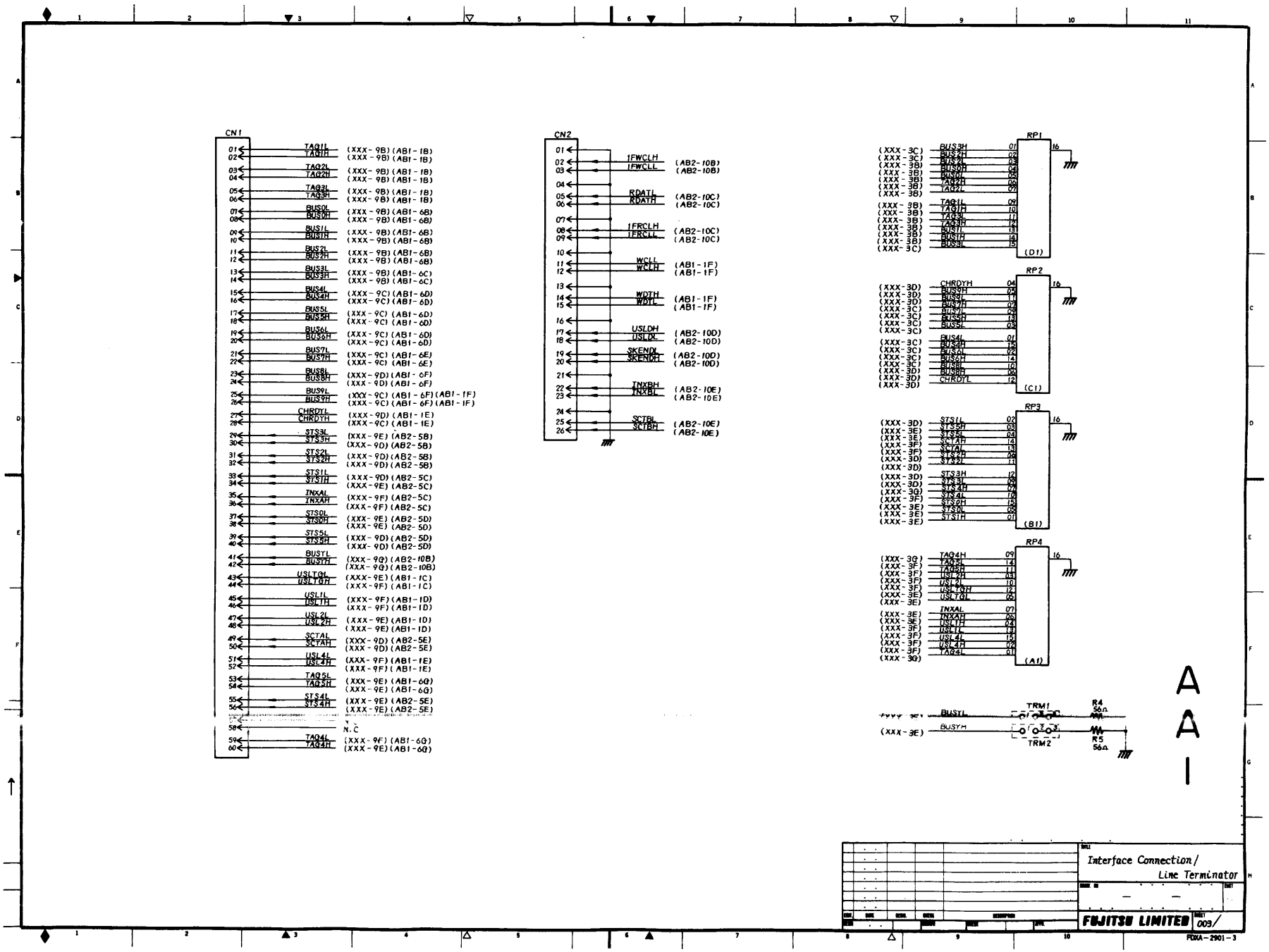
TITLE: Schematics/Drawings List

FUJITSU LIMITED

SHEET 001/45

FDXA-2901-3


CONTROL UNIT or NEXT UNIT
A-CABLE INTERFACE LINES
CONTROL UNIT
B-CABLE INTERFACE LINES
DRIVER RECEIVER
(AC1) (AE1)
INTERFACE CONTROL
(AC1, AE1)
DUAL CHANNEL OPTION INTERFACE FRONT PANEL INTERFACE (AA2, AB3)
STATUS GENERATOR (AD1)
SECTOR GENERATOR SECTOR COUNTER (AK1)
HEAD ADDRESS REGISTER (HAR) (AE1)
VFO CONTROL (AL1, AL2)
SEEK STATUS (AJ1)
SEEK CONTROL (AH1, AH2)
CYLINDER ADDRESS REGISTER (CAR) (AF1, AF2)
SEEK CHECK DEYECT (AJ3)
FAULT DETECT (AJ2)
MAINTENANCE DISPLAY (AJ4)
POWER UP SEQENCER (AG1, AG2)
WRITE COMPESATION (AL2)
VFO (AM1, AM2)
DATA SEPARATOR (AN1)
SERVO CONTROL (BG1, BH1, BK1)
POSITION SENSING (BG1)
SERVO LOGIC (BJ1)
PLO (BF2)
CARRIER AMPLIFIER (BF1)
DC MOTOR CONTROL (1) (BD1)
DC MOTOR CONTROL (2) (BD2)
READ / WRITE (BB1, BB2)
READ/WRITE PRE-AMP (DA1)
VCM
R/W HEAD
SERVO HEAD
SERVO PRE-AMP (DA1)
DISK
DC MOTOR
POWER AMPLIFIER (CA1, CA2)
TITLE
Functional Block Diagram
FUJITSU LIMITED
SHEET 002/
FDXA-2901-3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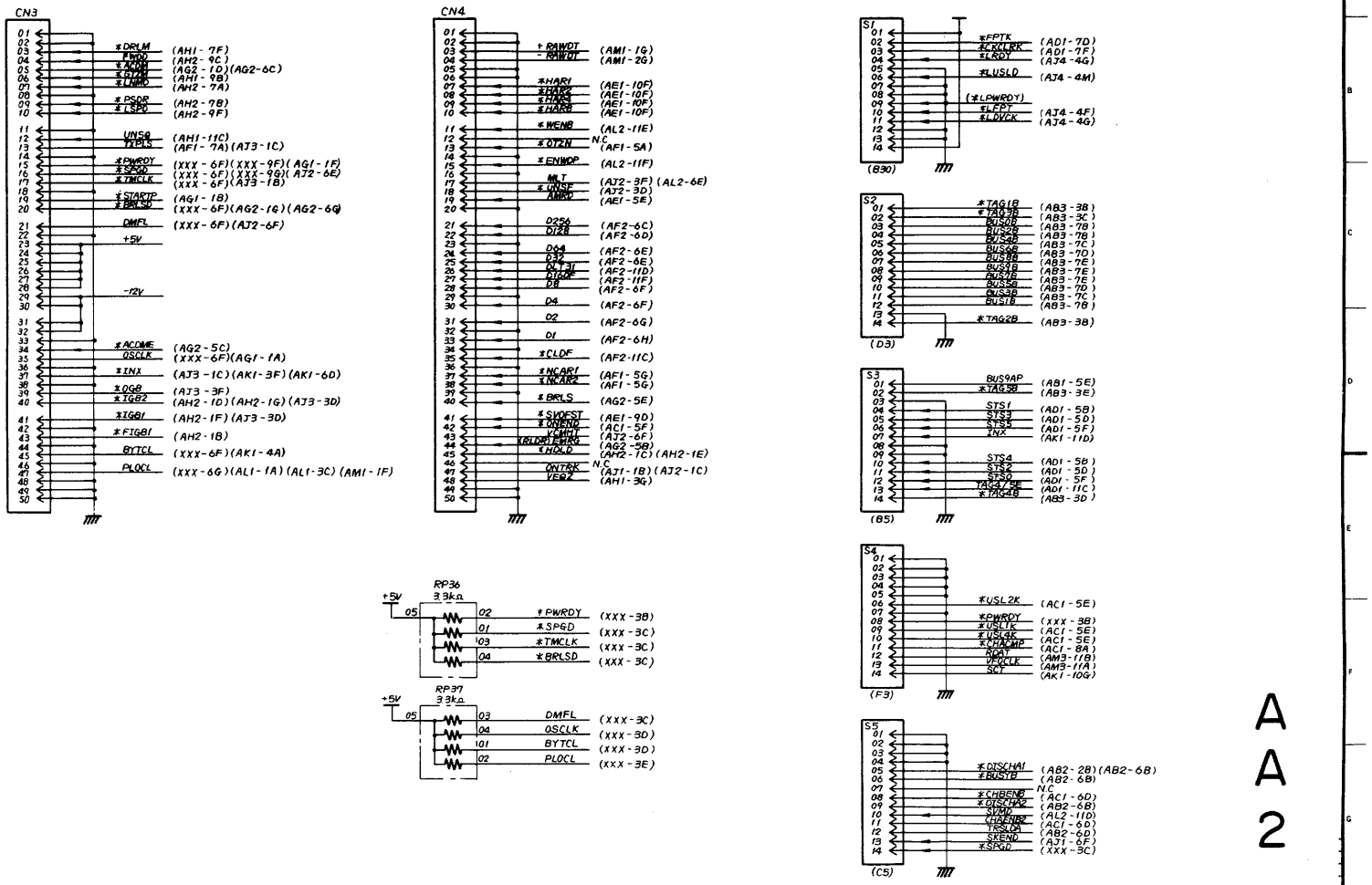
CN2
RP1
RP2
RP3
RP4
TRM1
TRM2
R4 56Ω
R5 56Ω
Interface Connection / Line Terminator
FUJITSU LIMITED
FOXA-2901-3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PWRD (AH2-9C)
*ACOM (AG2-1D)(AG2-6C)
*GTAM (AH1-9B)
*LWRD (AH2-7A)
*PSDR (AH2-7B)
*LSPD (AH2-9F)
UNSA (AH1-11C)
TXPLS (AF1-7A)(AJ3-1C)
*PWRDY (XXX-6F)(XXX-9F)(AG1-1F)
*SPGD (XXX-6F)(XXX-9G)(AJ2-6E)
*TMCLK (XXX-6F)(AJ3-1B)
*STARTP (AG1-1B)
*BRLSD (XXX-6F)(AG2-1G)(AG2-6G)
DMFL (XXX-6F)(AJ2-6F)
+5V
-12V
*ACOME (AG2-5C)
OSCLK (XXX-6F)(AG1-1A)
*INX (AJ3-1C)(AK1-3F)(AK1-6D)
*QGB (AJ3-3F)
*IGB2 (AH2-1D)(AH2-1G)(AJ3-3D)
*IGB1 (AH2-1F)(AJ3-3D)
*FIGB1 (AH2-1B)
BYTCL (XXX-6F)(AK1-4A)
PLOCL (XXX-6G)(AL1-1A)(AL1-3C)(AM1-1F)
CN4
*RAWDT (AM1-1G)
-RAWDT (AM1-2G)
*HAR1 (AE1-10F)
*HAR2 (AE1-10F)
*HAR4 (AE1-10F)
*HAR8 (AE1-10F)
*WENB (AL2-11E)
*QTZN N.C
*ENWDP (AL2-11F)
MLT (AJ2-3F)(AL2-6E)
*UNSF (AJ2-3D)
AMRD (AE1-5E)
D256 (AF2-6C)
D128 (AF2-6D)
D64 (AF2-6E)
D32 (AF2-6E)
D16F (AF2-11D)
D16OF (AF2-11F)
D8 (AF2-6F)
D4 (AF2-6F)
D2 (AF2-6G)
D1 (AF2-6H)
*CLDF (AF2-11C)
*NCAR1 (AF1-5G)
*NCAR2 (AF1-5G)
*BRLS (AG2-5E)
*SWDEST (AE1-9D)
*DNENG (AC1-5F)
*CMIT (AJ2-6F)
(RLDAT,EMRG) (AG2-5B)
*HOLD (AH2-7C)(AH2-1E)
N.C
ONTRK (AJ1-1B)(AJ2-1C)
VERZ (AH1-3G)
RP36
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+5V
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*SPGD (XXX-3C)
*TMCLK (XXX-3C)
*BRLSD (XXX-3C)
RP37
3.3kΩ
+5V
DMFL (XXX-3C)
OSCLK (XXX-3D)
BYTCL (XXX-3D)
PLOCL (XXX-3E)
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*CKLERR (AD1-7F)
*LRDY (AJ4-4G)
*LUSLD (AJ4-4M)
(*LPWRDY)
*LFCT (AJ4-4F)
*LDVCK (AJ4-4G)
(B30)
S2
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*TAG3B (AB3-3C)
BUS2B (AB3-7B)
BUS6B (AB3-7B)
BUS4B (AB3-7C)
BUS9B (AB3-7D)
BUS8B (AB3-7E)
BUS9B (AB3-7E)
BUS1B (AB3-7E)
BUS5B (AB3-7D)
BUS3B (AB3-7C)
BUS1B (AB3-7B)
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(D3)
S3
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STS3 (AD1-5D)
STS5 (AD1-5F)
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STS4 (AD1-5B)
STS6 (AD1-5D)
STS0 (AD1-5F)
TAG4/5E (AD1-11C)
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(B5)
S4
*USL2K (AC1-5E)
*PWRDY (XXX-3B)
*USLTK (AC1-5E)
*USL4K (AC1-5E)
*CHCLAMP (AC1-8A)
ROAT (AM3-11B)
*DPCCLK (AM3-11A)
SCT (AK1-10G)
(F3)
S5
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*BUS1B (AB2-6B)
N.C
*CHBEND (AC1-6D)
*DTSCHA2 (AB2-6B)
SYMD (AL2-11D)
*CHBENB2 (AC1-6D)
*FSLOA (AB2-6D)
SKEND (AJ1-6F)
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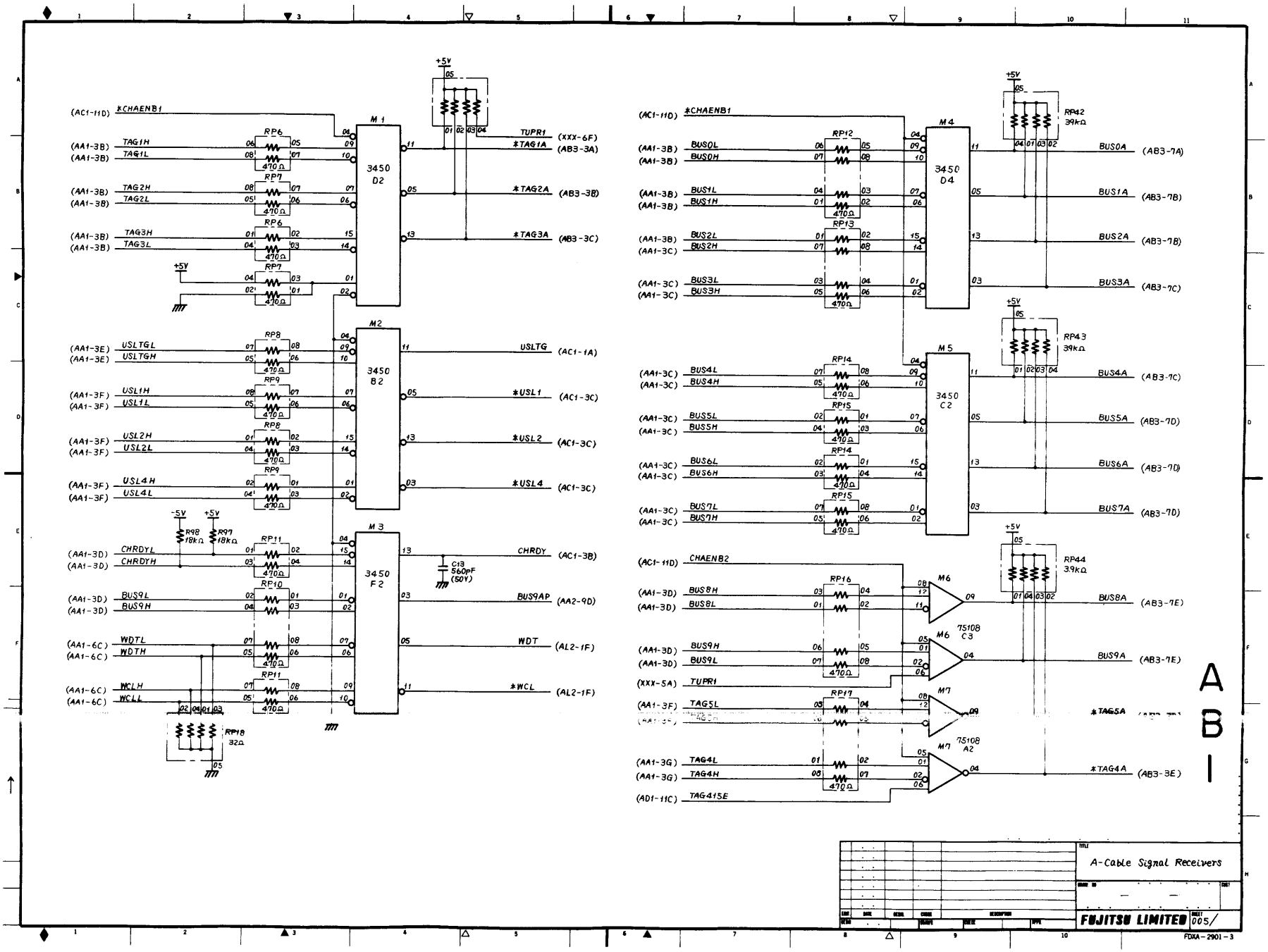
Connection with CZGM PCA/
Dual Channel Connection
FUJITSU LIMITED
004/
FDXA-2901-3


A
B
I
A-Cable Signal Receivers
FUJITSU LIMITED
005/
FDXA-2901-3
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M2
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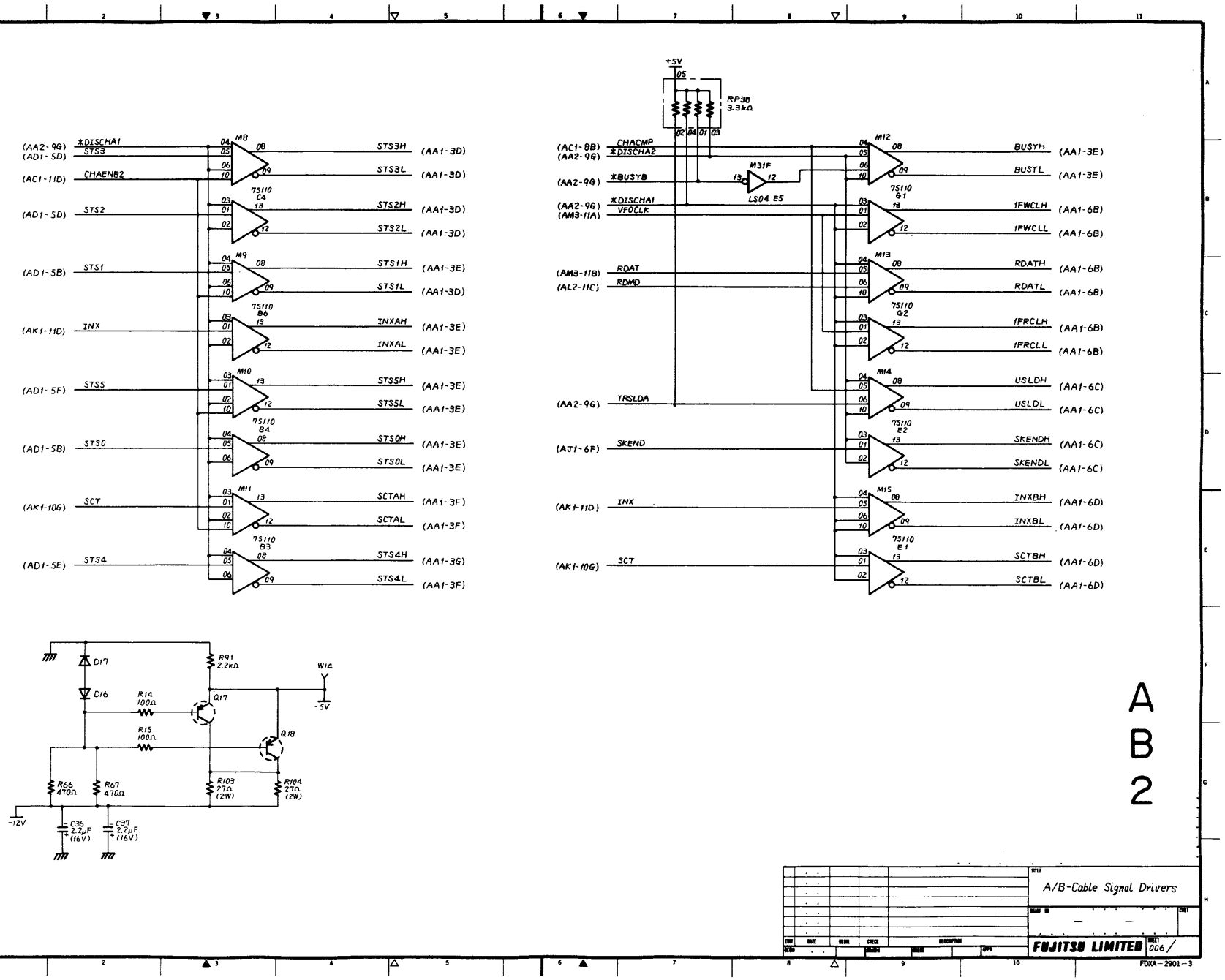
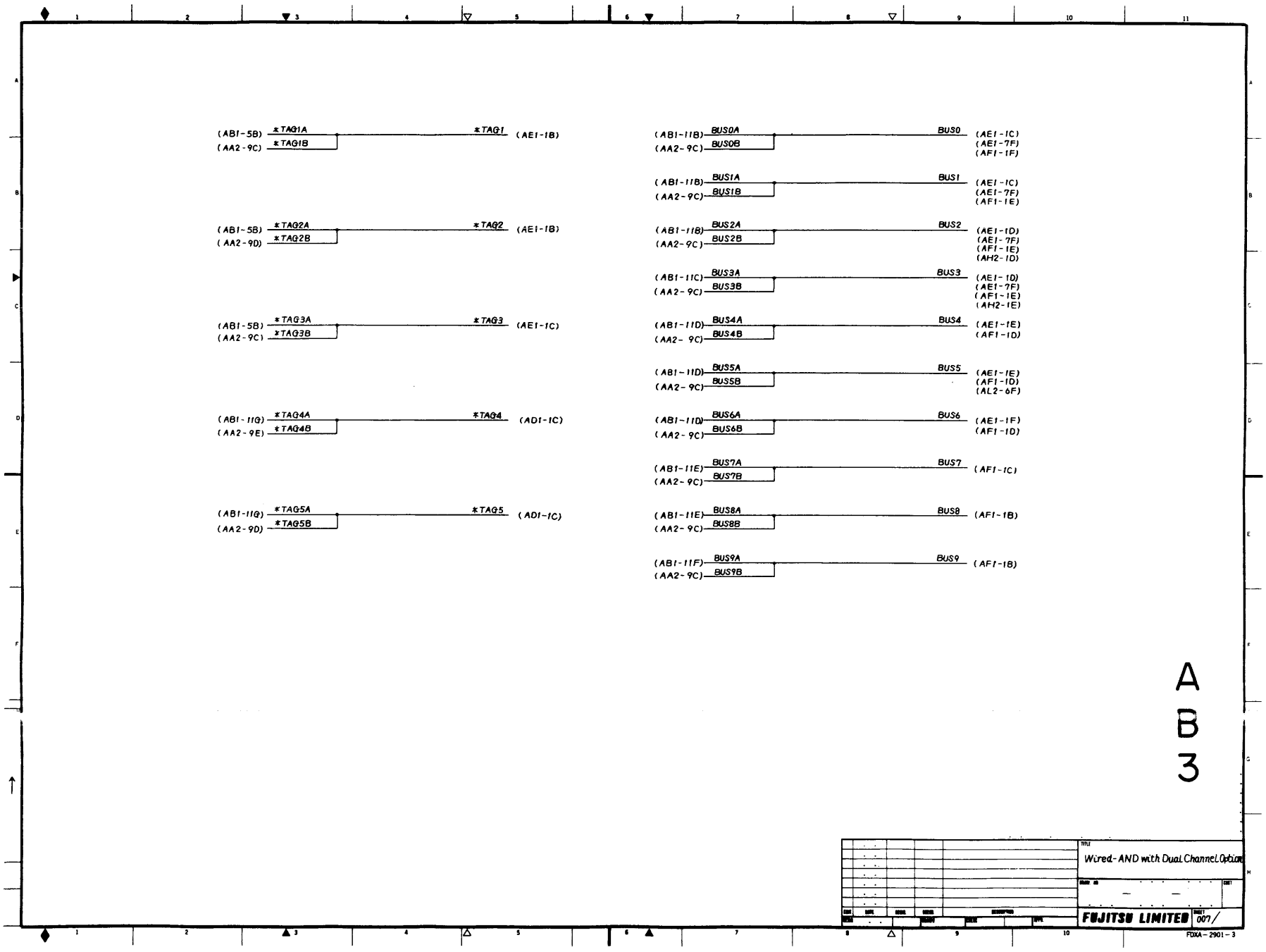
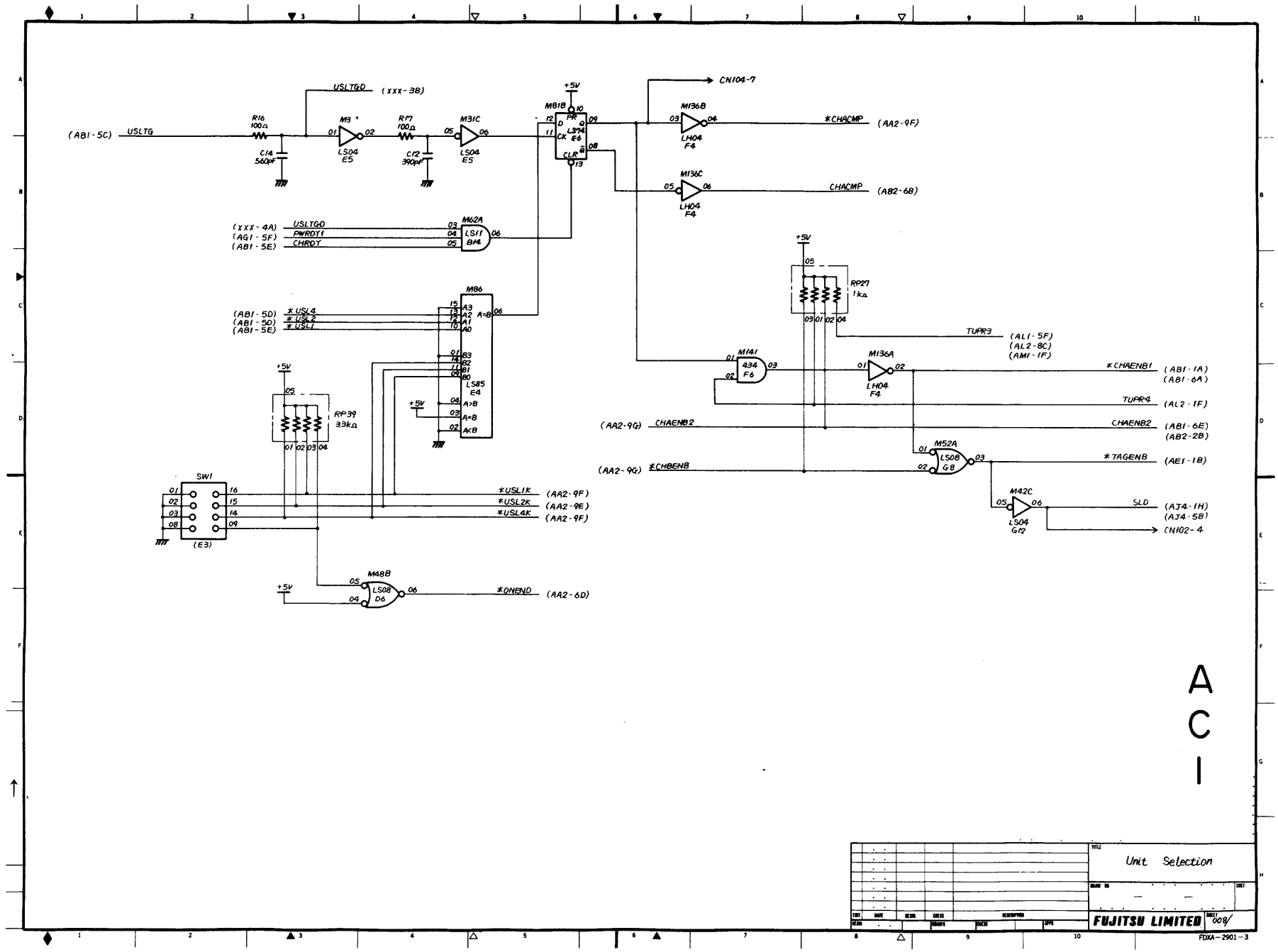
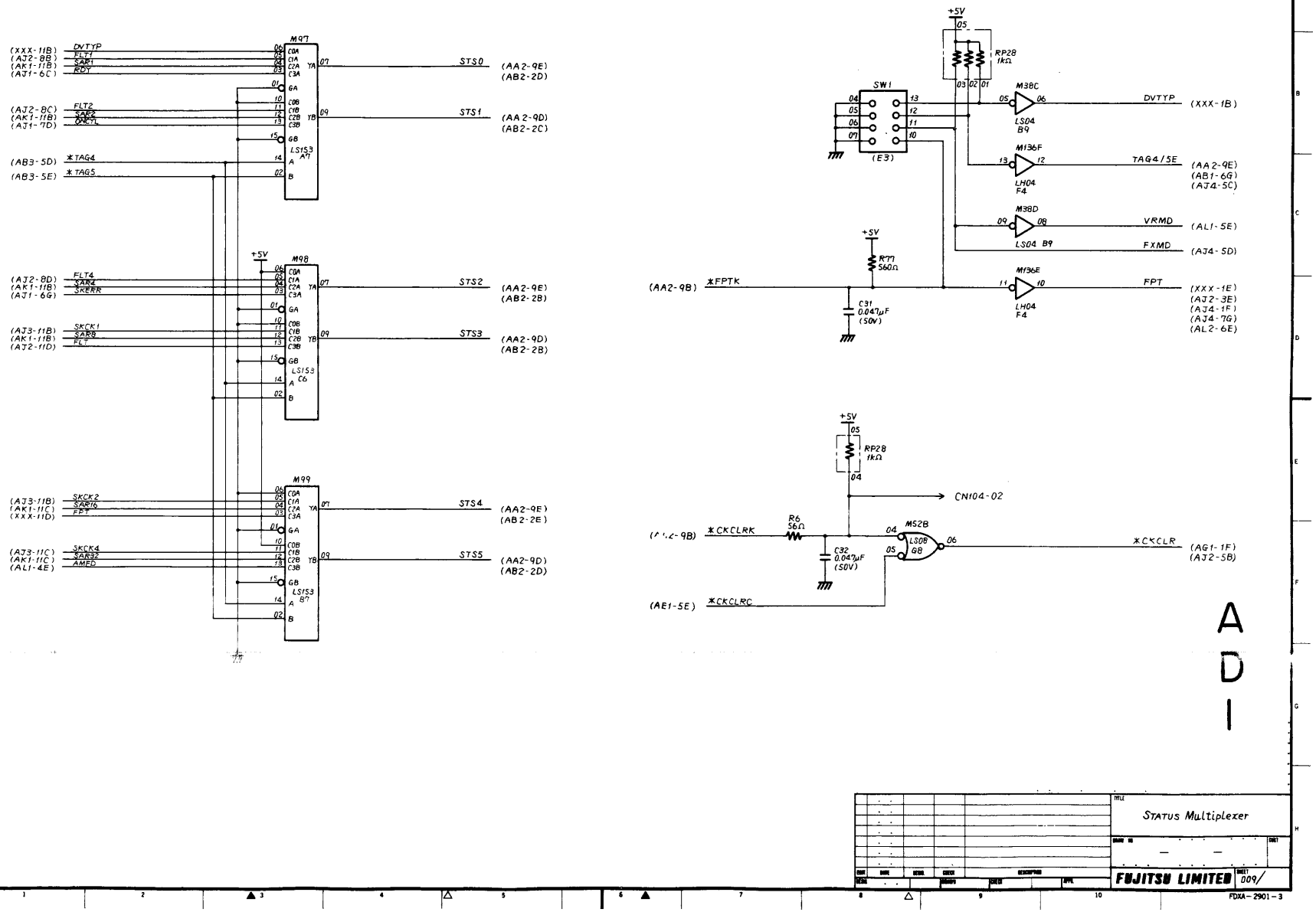
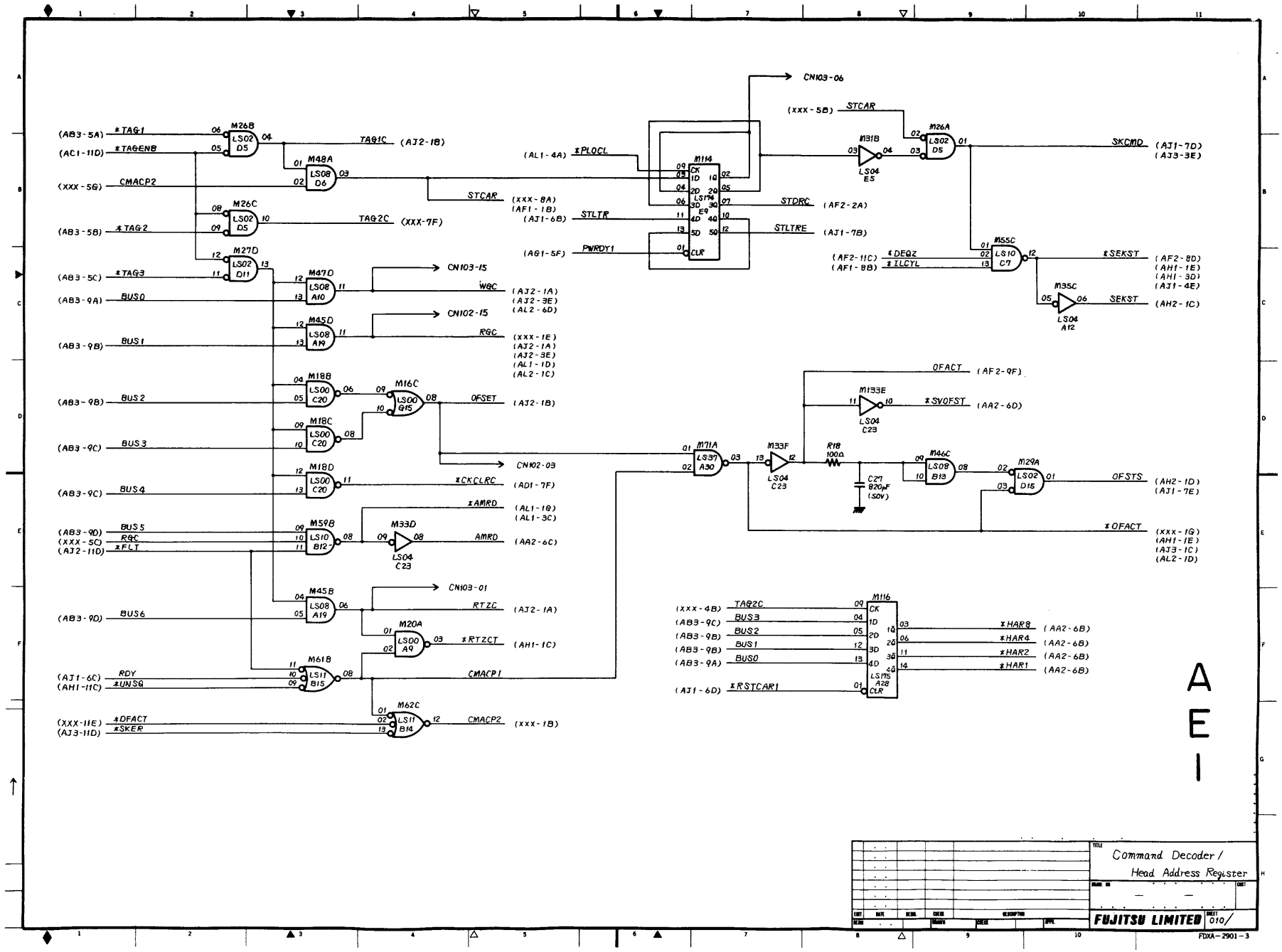
M3
3450 F2
M4
3450 D4
M5
3450 C2
M6
75108 C3
M7
75108 A2
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
RP14
RP15
RP16
RP17
RP18 32Ω
RP42 39kΩ
RP43 39kΩ
RP44 3.9kΩ
R98 18kΩ
R97 18kΩ
C13 560PF (50V)
470Ω
+5V
-5V
(AC1-11D) *CHAENB1
(AA1-3B) TAG1H
(AA1-3B) TAG1L
(AA1-3B) TAG2H
(AA1-3B) TAG2L
(AA1-3B) TAG3H
(AA1-3B) TAG3L
TUPR1 (XXX-6F)
*TAG1A (AB3-3A)
*TAG2A (AB3-3B)
*TAG3A (AB3-3C)
(AA1-3E) USLTGL
(AA1-3E) USLTGH
(AA1-3F) USL1H
(AA1-3F) USL1L
(AA1-3F) USL2H
(AA1-3F) USL2L
(AA1-3F) USL4H
(AA1-3F) USL4L
USLTG (AC1-1A)
*USL1 (AC1-3C)
*USL2 (AC1-3C)
*USL4 (AC1-3C)
(AA1-3D) CHRDYL
(AA1-3D) CHRDYH
(AA1-3D) BUS9L
(AA1-3D) BUS9H
(AA1-6C) WDTL
(AA1-6C) WDTH
(AA1-6C) WCLH
(AA1-6C) WCLL
CHRDY (AC1-3B)
BUS9AP (AA2-9D)
WDT (AL2-1F)
*WCL (AL2-1F)
(AA1-3B) BUS0L
(AA1-3B) BUS0H
(AA1-3B) BUS1L
(AA1-3B) BUS1H
(AA1-3B) BUS2L
(AA1-3C) BUS2H
(AA1-3C) BUS3L
(AA1-3C) BUS3H
BUS0A (AB3-7A)
BUS1A (AB3-7B)
BUS2A (AB3-7B)
BUS3A (AB3-7C)
(AA1-3C) BUS4L
(AA1-3C) BUS4H
(AA1-3C) BUS5L
(AA1-3C) BUS5H
(AA1-3C) BUS6L
(AA1-3C) BUS6H
(AA1-3C) BUS7L
(AA1-3C) BUS7H
BUS4A (AB3-7C)
BUS5A (AB3-7D)
BUS6A (AB3-7D)
BUS7A (AB3-7D)
(AC1-11D) CHAENB2
(AA1-3D) BUS8H
(AA1-3D) BUS8L
(AA1-3D) BUS9H
(AA1-3D) BUS9L
(XXX-5A) TUPR1
(AA1-3F) TAG5L
(AA1-3G) TAG4L
(AA1-3G) TAG4H
(AD1-11C) TAG415E
BUS8A (AB3-7E)
BUS9A (AB3-7E)
*TAG5A
*TAG4A (AB3-3E)

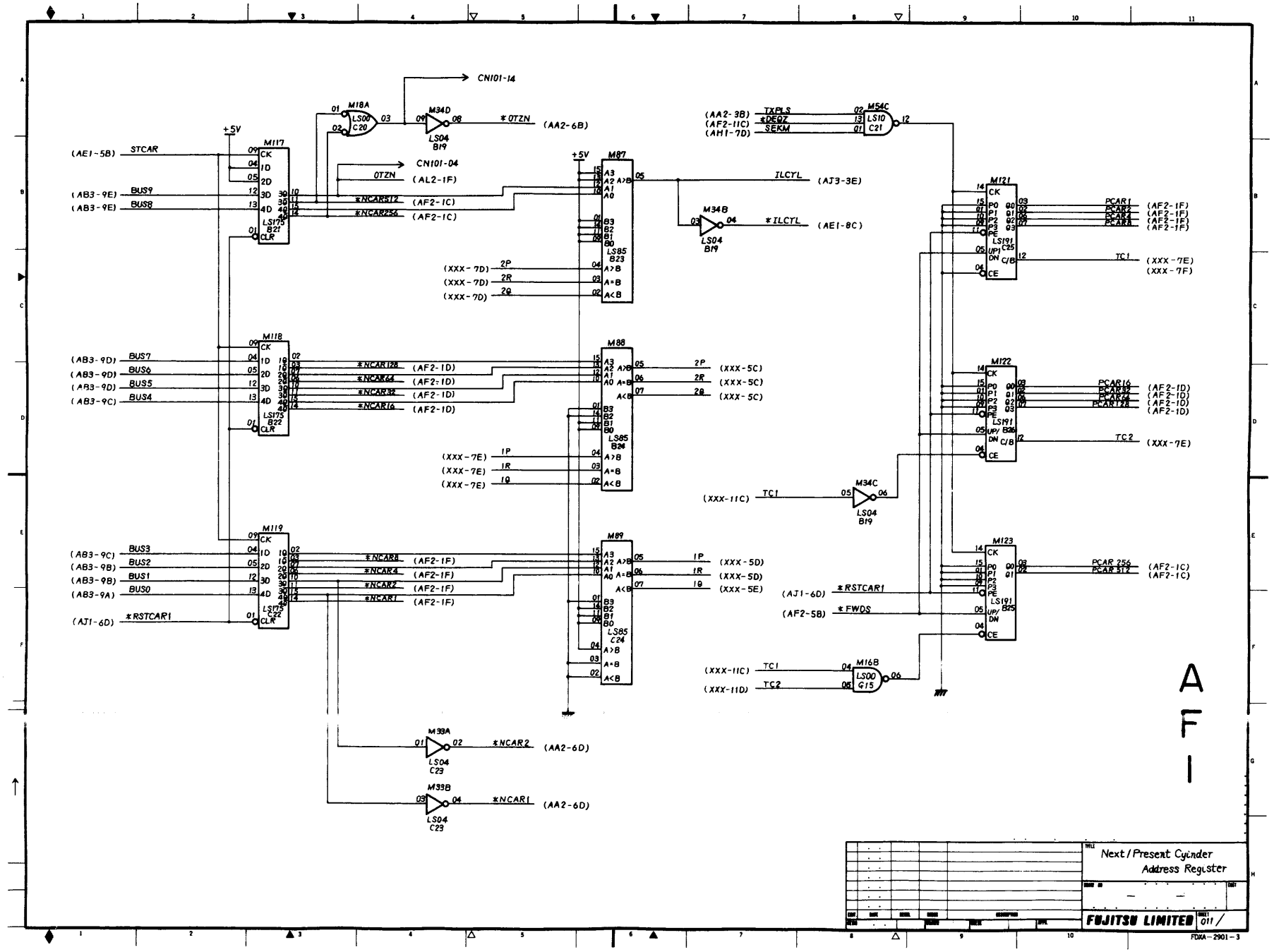

(AA2-9G) *DISCHA1
(AD1-5D) STS3
(AC1-11D) CHAENB2
(AD1-5D) STS2
(AD1-5B) STS1
(AK1-11D) INX
(AD1-5F) STS5
(AD1-5B) STS0
(AK1-10G) SCT
(AD1-5E) STS4
M8
M9
M10
M11
75110 C4
75110 B6
75110 B4
75110 B3
STS3H (AA1-3D)
STS3L (AA1-3D)
STS2H (AA1-3D)
STS2L (AA1-3D)
STS1H (AA1-3E)
STS1L (AA1-3D)
INXAH (AA1-3E)
INXAL (AA1-3E)
STS5H (AA1-3E)
STS5L (AA1-3E)
STS0H (AA1-3E)
STS0L (AA1-3E)
SCTAH (AA1-3F)
SCTAL (AA1-3F)
STS4H (AA1-3G)
STS4L (AA1-3F)
+5V
RP38 3.3kΩ
(AC1-8B) CHACMP
(AA2-9G) *DISCHA2
(AA2-9G) *BUSYB
(AA2-9G) *DISCHA1
(AM3-11A) VFOCLK
(AM3-11B) RDAT
(AL2-11C) RDMD
(AA2-9G) TRSLDA
(AJ1-6F) SKEND
(AK1-11D) INX
(AK1-10G) SCT
M31F LS04 E5
M12
M13
M14
M15
75110 G1
75110 G2
75110 E2
75110 E1
BUSYH (AA1-3E)
BUSYL (AA1-3E)
1FWCLH (AA1-6B)
1FWCLL (AA1-6B)
RDATH (AA1-6B)
RDATL (AA1-6B)
1FRCLH (AA1-6B)
1FRCLL (AA1-6B)
USLDH (AA1-6C)
USLDL (AA1-6C)
SKENDH (AA1-6C)
SKENDL (AA1-6C)
INXBH (AA1-6D)
INXBL (AA1-6D)
SCTBH (AA1-6D)
SCTBL (AA1-6D)
D17
D16
R91 2.2kΩ
R14 100Ω
R15 100Ω
Q17
Q18
W14
-5V
R66 470Ω
R67 470Ω
R103 27Ω (2W)
R104 27Ω (2W)
-12V
C36 2.2μF (16V)
C37 2.2μF (16V)
A
B
2
A/B-Cable Signal Drivers
FUJITSU LIMITED
FDXA-2901-3

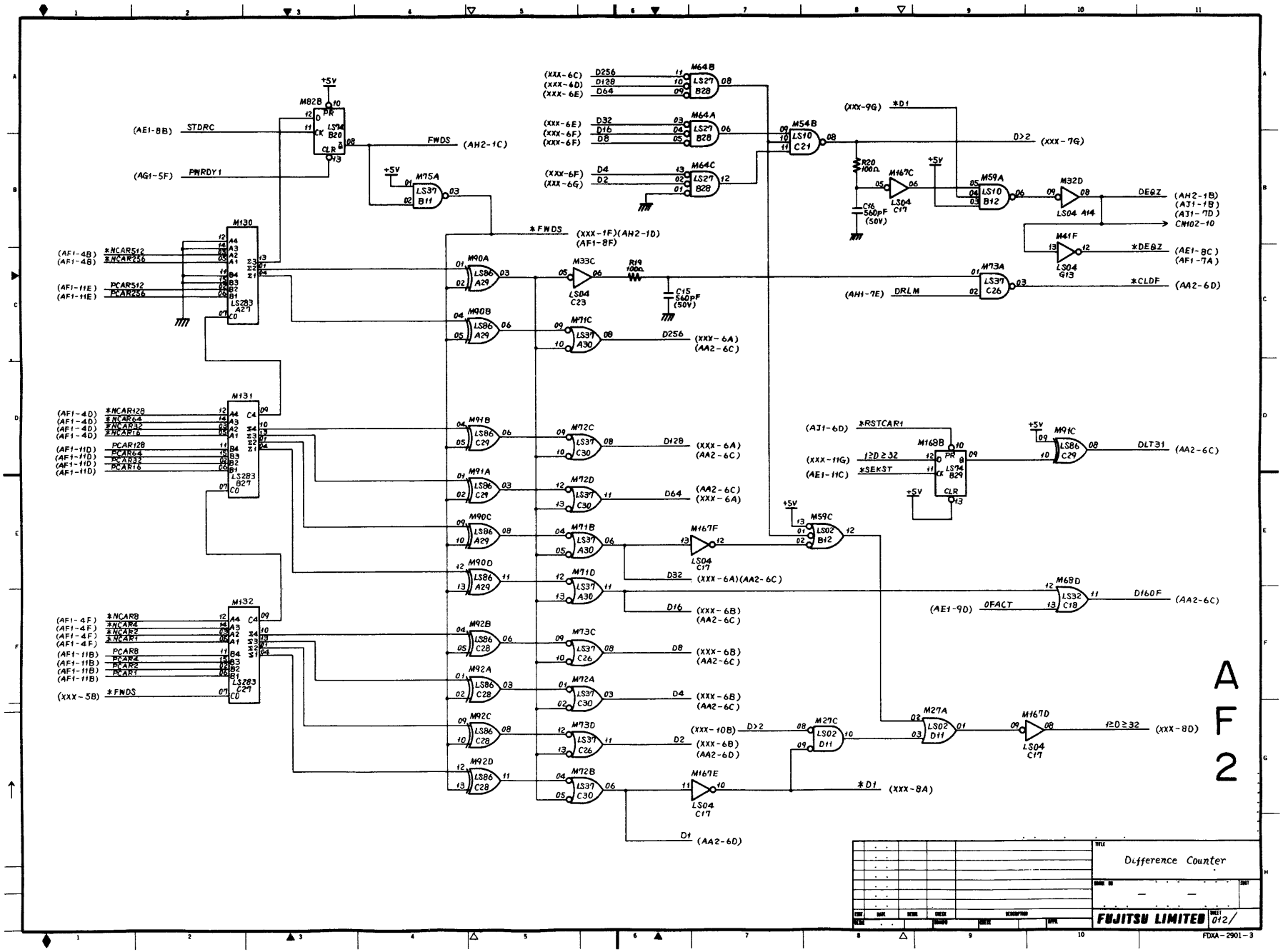

(AB1-5B) *TAG1A
(AA2-9C) *TAG1B
*TAG1 (AE1-1B)
(AB1-5B) *TAG2A
(AA2-9D) *TAG2B
*TAG2 (AE1-1B)
(AB1-5B) *TAG3A
(AA2-9C) *TAG3B
*TAG3 (AE1-1C)
(AB1-11G) *TAG4A
(AA2-9E) *TAG4B
*TAG4 (AD1-1C)
(AB1-11G) *TAG5A
(AA2-9D) *TAG5B
*TAG5 (AD1-1C)
(AB1-11B) BUS0A
(AA2-9C) BUS0B
BUS0 (AE1-1C) (AE1-7F) (AF1-1F)
(AB1-11B) BUS1A
(AA2-9C) BUS1B
BUS1 (AE1-1C) (AE1-7F) (AF1-1E)
(AB1-11B) BUS2A
(AA2-9C) BUS2B
BUS2 (AE1-1D) (AE1-7F) (AF1-1E) (AH2-1D)
(AB1-11C) BUS3A
(AA2-9C) BUS3B
BUS3 (AE1-1D) (AE1-7F) (AF1-1E) (AH2-1E)
(AB1-11D) BUS4A
(AA2-9C) BUS4B
BUS4 (AE1-1E) (AF1-1D)
(AB1-11D) BUS5A
(AA2-9C) BUS5B
BUS5 (AE1-1E) (AF1-1D) (AL2-6F)
(AB1-11D) BUS6A
(AA2-9C) BUS6B
BUS6 (AE1-1F) (AF1-1D)
(AB1-11E) BUS7A
(AA2-9C) BUS7B
BUS7 (AF1-1C)
(AB1-11E) BUS8A
(AA2-9C) BUS8B
BUS8 (AF1-1B)
(AB1-11F) BUS9A
(AA2-9C) BUS9B
BUS9 (AF1-1B)
A
B
3
Wired-AND with Dual Channel Option
FUJITSU LIMITED
007/
FOXA-2901-3

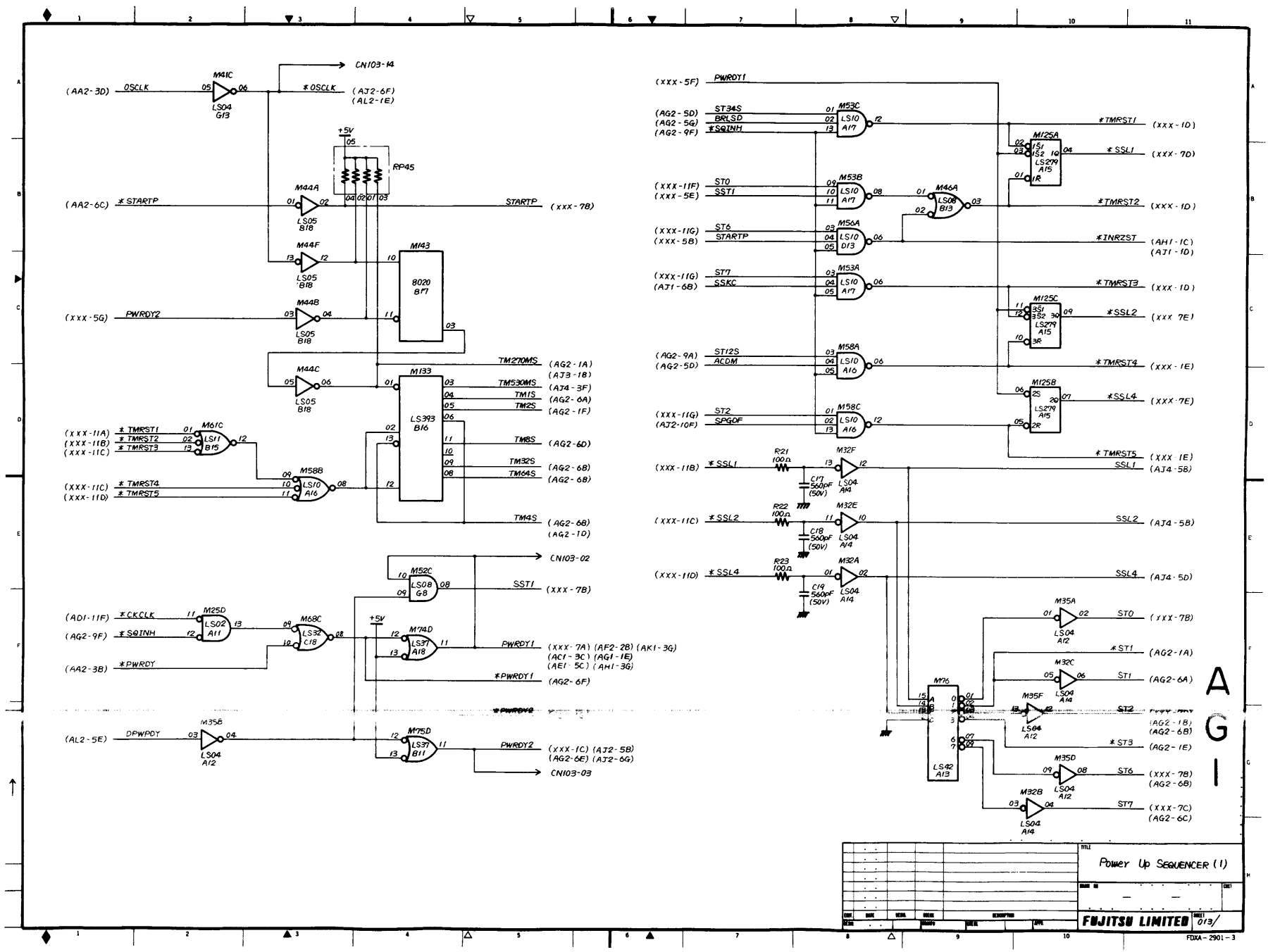

USLTGD (XXX-3B)
(AB1-5C) USLTG
R16 100Ω
C14 560PF
M3 LS04 E5
R17 100Ω
C12 390PF
M31C LS04 E5
M81B LS74 E6
+5V
CN104-7
M136B LH04 F4
*CHACMP (AA2-9F)
M136C LH04 F4
CHACMP (AB2-6B)
(XXX-4A) USLTGD
(AG1-5F) PWRDY1
(AB1-5E) CHRDY
M62A LS11 B14
M86 LS85 E4
(AB1-5D) *USL4
(AB1-5D) *USL2
(AB1-5E) *USL1
RP39 33kΩ
SW1 (E3)
*USL1K (AA2-9F)
*USL2K (AA2-9E)
*USL4K (AA2-9F)
M48B LS08 D6
*ONEND (AA2-6D)
RP27 1kΩ
TUPR3 (AL1-5F) (AL2-8C) (AM1-1F)
M141 434 F6
M136A LH04 F4
*CHAENB1 (AB1-1A) (AB1-6A)
TUPR4 (AL2-1F)
(AA2-9G) CHAENB2
CHAENB2 (AB1-6E) (AB2-2B)
M52A LS08 G8
(AA2-9G) *CHBENB
*TAGENB (AE1-1B)
M42C LS04 G12
SLD (AJ4-1H) (AJ4-5B)
CN102-4
A
C
I
Unit Selection
FUJITSU LIMITED
FDXA-2901-3


M97
(XXX-11B) DVTYP
(AJ2-8B) FLT1
(AK1-11B) SAR1
(AJ1-6C) RDY
(AJ2-8C) FLT2
(AK1-11B) SAR2
(AJ1-7D) OVCYL
(AB3-5D) *TAG4
(AB3-5E) *TAG5
LS153 A7
STS0 (AA2-9E) (AB2-2D)
STS1 (AA2-9D) (AB2-2C)
M98
(AJ2-8D) FLT4
(AK1-11B) SAR4
(AJ1-6G) SKERR
(AJ3-11B) SKCK1
(AK1-11B) SAR8
(AJ2-11D) FLT
LS153 C6
STS2 (AA2-9E) (AB2-2B)
STS3 (AA2-9D) (AB2-2B)
M99
(AJ3-11B) SKCK2
(AK1-11C) SAR16
(XXX-11D) FPT
(AJ3-11C) SKCK4
(AK1-11C) SAR32
(AL1-4E) AMED
LS153 B7
STS4 (AA2-9E) (AB2-2E)
STS5 (AA2-9D) (AB2-2D)
+5V
RP28 1kΩ
SW1
(E3)
M38C
LS04 B9
DVTYP (XXX-1B)
M136F
LH04 F4
TAG4/5E (AA2-9E) (AB1-6G) (AJ4-5C)
M38D
LS04 B9
VRMD (AL1-5E)
FXMD (AJ4-5D)
R77 560Ω
(AA2-9B) *FPTK
C31 0.047μF (50V)
M136E
LH04 F4
FPT (XXX-1E) (AJ2-3E) (AJ4-1F) (AJ4-7G) (AL2-6E)
CN104-02
R6 56Ω
(AA2-9B) *CKCLRK
C32 0.047μF (50V)
M52B
LS08 G8
*CKCLR (AG1-1F) (AJ2-5B)
(AE1-5E) *CKCLRC
A
D
I
TITLE
STATUS Multiplexer
FUJITSU LIMITED
009/
FDXA-2901-3


(AB3-5A) *TAG1
(AC1-11D) *TAGENB
(XXX-5G) CMACP2
(AB3-5B) *TAG2
(AB3-5C) *TAG3
(AB3-9A) BUS0
(AB3-9B) BUS1
(AB3-9B) BUS2
(AB3-9C) BUS3
(AB3-9C) BUS4
(AB3-9D) BUS5
(XXX-5C) RGC
(AJ2-11D) *FLT
(AB3-9D) BUS6
(AJ1-6C) RDY
(AH1-11C) *UNSC
(XXX-11E) *DFACT
(AJ3-11D) *SKER
M26B LS02 D5
M48A LS08 D6
M26C LS02 D5
M27D LS02 D11
M47D LS08 A10
M45D LS08 A19
M18B LS00 C20
M16C LS00 G15
M18C LS00 C20
M18D LS00 C20
M59B LS10 B12
M33D LS04 C23
M45B LS08 A19
M20A LS00 A9
M61B LS11 B15
M62C LS11 B14
TAG1C (AJ2-1B)
TAG2C (XXX-7F)
STCAR (XXX-8A) (AF1-1B)
CN103-15
WGC (AJ2-1A) (AJ2-3E) (AL2-6D)
CN102-15
RGC (XXX-1E) (AJ2-1A) (AJ2-3E) (AL1-1D) (AL2-1C)
OFSET (AJ2-1B)
CN102-03
*CKCLRC (AD1-7F)
*AMRD (AL1-1B) (AL1-3C)
AMRD (AA2-6C)
CN103-01
RTZC (AJ2-1A)
*RTZCT (AH1-1C)
CMACP1
CMACP2 (XXX-1B)
(AL1-4A) *PLOCL
(AG1-5F) PWRDY1
M114 LS175 A9 E9
STLTR (AJ1-6B)
STDRC (AF2-2A)
STLTRE (AJ1-7B)
CN103-06
(XXX-5B) STCAR
M131B LS04 E5
M26A LS02 D5
SKCMD (AJ1-7D) (AJ3-3E)
(AF2-11C) *DEQZ
(AF1-8B) *ILCYL
M55C LS10 C7
*SEKST (AF2-8D) (AH1-1E) (AH1-3D) (AJ1-4E)
M35C LS04 A12
SEKST (AH2-1C)
OFACT (AF2-9F)
M133E LS04 C23
*SVOFST (AA2-6D)
M71A LS37 A30
M33F LS04 C23
R18 100Ω
C27 820pF (50V)
M46C LS08 B13
M29A LS02 D15
OFSTS (AH2-1D) (AJ1-7E)
*OFACT (XXX-1G) (AH1-1E) (AJ3-1C) (AL2-1D)
(XXX-4B) TAG2C
(AB3-9C) BUS3
(AB3-9B) BUS2
(AB3-9B) BUS1
(AB3-9A) BUS0
(AJ1-6D) *RSTCAR1
M116 LS175 A28
*HAR8 (AA2-6B)
*HAR4 (AA2-6B)
*HAR2 (AA2-6B)
*HAR1 (AA2-6B)
A
E
I
Command Decoder / Head Address Register
FUJITSU LIMITED
FDXA-2901-3


CN101-14
M18A
LS00
C20
M34D
LS04
B19
*OTZN
(AA2-6B)
+5V
M117
STCAR
(AE1-5B)
CN101-04
OTZN
(AL2-1F)
BUS9
BUS8
(AB3-9E)
*NCAR512
*NCAR256
(AF2-1C)
LS175
B21
CLR
M87
ILCYL
(AJ3-3E)
M34B
*ILCYL
(AE1-8C)
LS85
B23
(XXX-7D)
2P
2R
2Q
A>B
A=B
A<B
M118
BUS7
BUS6
BUS5
BUS4
(AB3-9D)
(AB3-9C)
*NCAR128
*NCAR64
*NCAR32
*NCAR16
(AF2-1D)
LS175
B22
M88
LS85
B24
(XXX-7E)
1P
1R
1Q
2P
2R
2Q
(XXX-5C)
M119
BUS3
BUS2
BUS1
BUS0
(AB3-9C)
(AB3-9B)
(AB3-9A)
*NCAR8
*NCAR4
*NCAR2
*NCAR1
(AF2-1F)
*RSTCAR1
(AJ1-6D)
LS175
C22
M89
LS85
C24
(XXX-5D)
(XXX-5E)
M33A
LS04
C23
*NCAR2
(AA2-6D)
M33B
*NCAR1
(AA2-6D)
(AA2-3B)
TXPLS
(AF2-11C)
*DEQZ
(AH1-7D)
SEKM
M54C
LS10
C21
M121
LS191
C25
PCAR1
PCAR2
PCAR4
PCAR8
(AF2-1F)
TC1
(XXX-7E)
(XXX-7F)
M122
LS191
B26
PCAR16
PCAR32
PCAR64
PCAR128
(AF2-1D)
TC2
(XXX-7E)
M34C
(XXX-11C)
TC1
M123
LS191
B25
PCAR 256
PCAR 512
(AF2-1C)
*RSTCAR1
(AJ1-6D)
*FWDS
(AF2-5B)
M16B
LS00
G15
TC2
(XXX-11D)
A
F
I
Next / Present Cylinder
Address Register
FUJITSU LIMITED
FDXA-2901-3


Difference Counter
FUJITSU LIMITED
FDXA-2901-3
A F 2
STDRC
PWRDY1
FWDS
*FWDS
*NCAR512
*NCAR256
PCAR512
PCAR256
*NCAR128
*NCAR64
*NCAR32
*NCAR16
PCAR128
PCAR64
PCAR32
PCAR16
*NCAR8
*NCAR4
*NCAR2
*NCAR1
PCAR8
PCAR4
PCAR2
PCAR1
DRLM
*RSTCAR1
*SEKST
0FACT
*CLDF
*DEQZ
DEQZ
DLT31
D0F
D1
D2
D4
D8
D16
D32
D64
D128
D256
D>2
I≥D≥32
M130
M131
M132
M828
M75A
M64B
M64A
M64C
M54B
M90A
M90B
M90C
M90D
M91B
M91A
M91C
M92B
M92A
M92C
M92D
M33C
M71C
M72C
M72D
M71B
M71D
M73C
M72A
M73D
M72B
M167F
M167E
M59C
M27C
M27A
M167D
M168B
M91C
M69D
M73A
M59A
M32D
M41F
M167C


CN103-14
M41C
(AA2-3D) OSCLK
LS04 G13
*OSCLK
(AJ2-6F)
(AL2-1E)
+5V
RP45
M44A
(AA2-6C) *STARTP
LS05 B18
STARTP (xxx-7B)
M44F
LS05 B18
M143
8020 BF1
M44B
(xxx-5G) PWRDY2
LS05 B18
TM270MS (AG2-1A) (AJ3-1B)
M44C
LS05 B18
M133
LS393 B16
TM530MS (AJ4-3F)
TM1S (AG2-6A)
TM2S (AG2-1F)
TM8S (AG2-6D)
TM32S (AG2-6B)
TM64S (AG2-6B)
TM4S (AG2-6B) (AG2-1D)
M61C
(xxx-11A) *TMRST1
(xxx-11B) *TMRST2
(xxx-11C) *TMRST3
LS11 B15
M58B
(xxx-11C) *TMRST4
(xxx-11D) *TMRST5
LS10 A16
CN103-02
M52C
LS08 G8
SST1 (xxx-7B)
(AD1-11E) *CKCLK
(AG2-9F) *SQINH
(AA2-3B) *PWRDY
M25D
LS02 A11
M68C
LS32 C18
+5V
M74D
LS37 A18
PWRDY1 (xxx-7A) (AF2-2B) (AK1-3G) (AC1-3C) (AG1-1E) (AE1-5C) (AH1-3G)
*PWRDY1 (AG2-6F)
(AL2-5E) DPWPDY
M35B
LS04 A12
M75D
LS37 B11
PWRDY2 (xxx-1C) (AJ2-5B) (AG2-6E) (AJ2-6G)
CN103-03
(xxx-5F) PWRDY1
(AG2-5D) ST34S
(AG2-5G) BRLSD
(AG2-9F) *SQINH
M53C
LS10 A17
(xxx-11F) ST0
(xxx-5E) SST1
M53B
LS10 A17
M46A
LS08 B13
(xxx-11G) ST6
(xxx-5B) STARTP
M50A
LS10 D13
(xxx-11G) ST7
(AJ1-6B) SSKC
M53A
LS10 A17
(AG2-9A) ST12S
(AG2-5D) ACDM
M58A
LS10 A16
(xxx-11G) ST2
(AJ2-10F) SPGOF
M58C
LS10 A16
M125A
LS279 A15
*TMRST1 (xxx-1D)
*SSL1 (xxx-7D)
*TMRST2 (xxx-1D)
M125C
LS279 A15
*INRZST (AH1-1C) (AJ1-1D)
*TMRST3 (xxx-1D)
*SSL2 (xxx 7E)
*TMRST4 (xxx-1E)
M125B
LS279 A15
*SSL4 (xxx-7E)
*TMRST5 (xxx 1E)
(xxx-11B) *SSL1
R21 100Ω
C17 560pF (50V)
M32F
LS04 A14
SSL1 (AJ4-5B)
(xxx-11C) *SSL2
R22 100Ω
C18 560pF (50V)
M32E
LS04 A14
SSL2 (AJ4-5B)
(xxx-11D) *SSL4
R23 100Ω
C19 560pF (50V)
M32A
LS04 A14
SSL4 (AJ4-5D)
M35A
LS04 A12
STO (xxx-7B)
*ST1 (AG2-1A)
M32C
LS04 A14
ST1 (AG2-6A)
M76
LS42 A13
M35F
LS04 A12
ST2 (AG2-1B) (AG2-6B)
*ST3 (AG2-1E)
M35D
LS04 A12
ST6 (xxx-7B) (AG2-6B)
M32B
LS04 A14
ST7 (xxx-7C) (AG2-6C)
A
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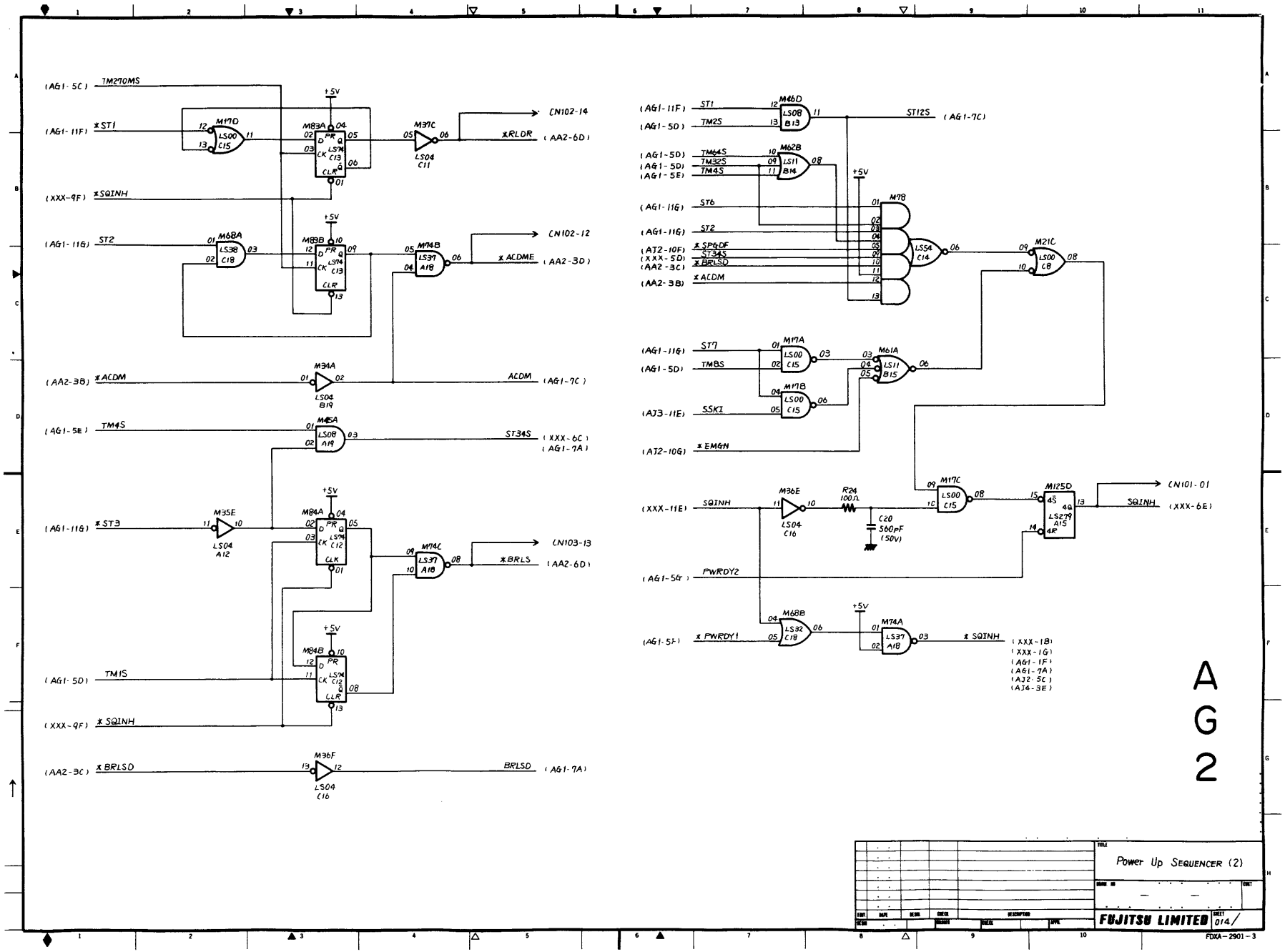
I
Power Up Sequencer (1)
FUJITSU LIMITED
FDXA-2901-3


(AG1-5C) TM270MS
(AG1-11F) *ST1
M17D LS00 C15
M83A LS74 C13
M37C LS04 C11
CN102-14
*RLDR (AA2-6D)
(XXX-9F) *SQINH
(AG1-11G) ST2
M68A LS38 C18
M83B LS74 C13
M74B LS37 A18
CN102-12
*ACDME (AA2-3D)
(AA2-3B) *ACDM
M34A LS04 B19
ACDM (AG1-7C)
(AG1-5E) TM4S
M45A LS08 A19
ST34S (XXX-6C) (AG1-7A)
(AG1-11G) *ST3
M35E LS04 A12
M84A LS74 C12
M74L LS37 A18
CN103-13
*BRLS (AA2-6D)
(AG1-5D) TM1S
M84B LS74 C12
(XXX-9F) *SQINH
(AA2-3C) *BRLSD
M36F LS04 C16
BRLSD (AG1-7A)
(AG1-11F) ST1
(AG1-5D) TM2S
M46D LS08 B13
ST12S (AG1-7C)
(AG1-5D) TM64S
(AG1-5D) TM32S
(AG1-5E) TM4S
M62B LS11 B14
(AG1-11G) ST6
(AG1-11G) ST2
(AT2-10F) *SP&DF
(XXX-5D) ST34S
(AA2-3C) *BRLSD
(AA2-3B) *ACDM
M78 LS54 C14
M21C LS00 C8
(AG1-11G) ST7
(AG1-5D) TM8S
M17A LS00 C15
M17B LS00 C15
M61A LS11 B15
(AJ3-11E) SSKI
(AJ2-10G) *EMGN
M17C LS00 C15
M125D LS279 A15
CN101-01
SQINH (XXX-6E)
(XXX-11E) SQINH
M36E LS04 C16
R24 100Ω
C20 560pF (50V)
(AG1-5G) PWRDY2
M68B LS32 C18
M74A LS37 A18
(AG1-5F) *PWRDY1
*SQINH (XXX-1B) (XXX-1G) (AG1-1F) (AG1-7A) (AJ2-5C) (AJ4-3E)
A
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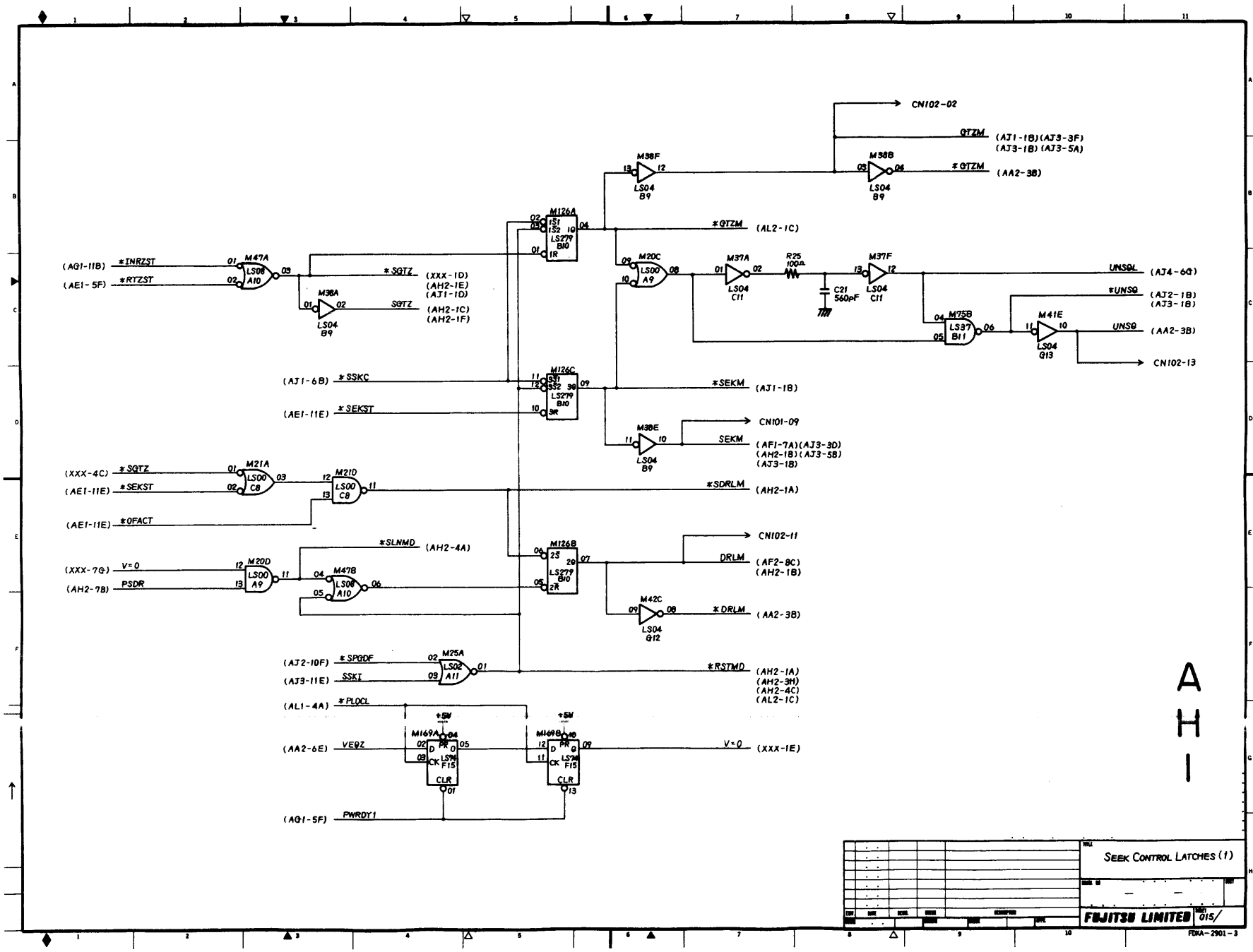
2
Power Up Sequencer (2)
FUJITSU LIMITED
FDXA-2901-3


CN102-02
QTZM
(AJ1-1B)(AJ3-3F)
(AJ3-1B)(AJ3-5A)
*QTZM
(AA2-3B)
*QTZM
(AL2-1C)
(AG1-11B) *INRZST
(AE1-5F) *RTZST
*SQTZ
(XXX-1D)
(AH2-1E)
(AJ1-1D)
SQTZ
(AH2-1C)
(AH2-1F)
UNSQL
(AJ4-6C)
*UNSQ
(AJ2-1B)
(AJ3-1B)
UNSQ
(AA2-3B)
CN102-13
(AJ1-6B) *SSKC
(AE1-11E) *SEKST
*SEKM
(AJ1-1B)
CN101-09
SEKM
(AF1-7A)(AJ3-3D)
(AH2-1B)(AJ3-5B)
(AJ3-1B)
(XXX-4C) *SQTZ
(AE1-11E) *SEKST
(AE1-11E) *OFACT
*SDRLM
(AH2-1A)
*SLNMD
(AH2-4A)
(XXX-7G) V=0
(AH2-7B) PSDR
CN102-11
DRLM
(AF2-8C)
(AH2-1B)
*DRLM
(AA2-3B)
(AJ2-10F) *SPGDF
(AJ3-11E) SSKI
*RSTMD
(AH2-1A)
(AH2-3H)
(AH2-4C)
(AL2-1C)
(AL1-4A) *PLOCL
(AA2-6E) VEQZ
V=0
(XXX-1E)
(AG1-5F) PWRDY1
M47A
M38A
M126A
M38F
M38B
M20C
M37A
M37F
M75B
M41E
M126C
M38E
M21A
M21D
M20D
M47B
M126B
M42C
M25A
M169A
M169B
R25
100Ω
C21
560pF
A
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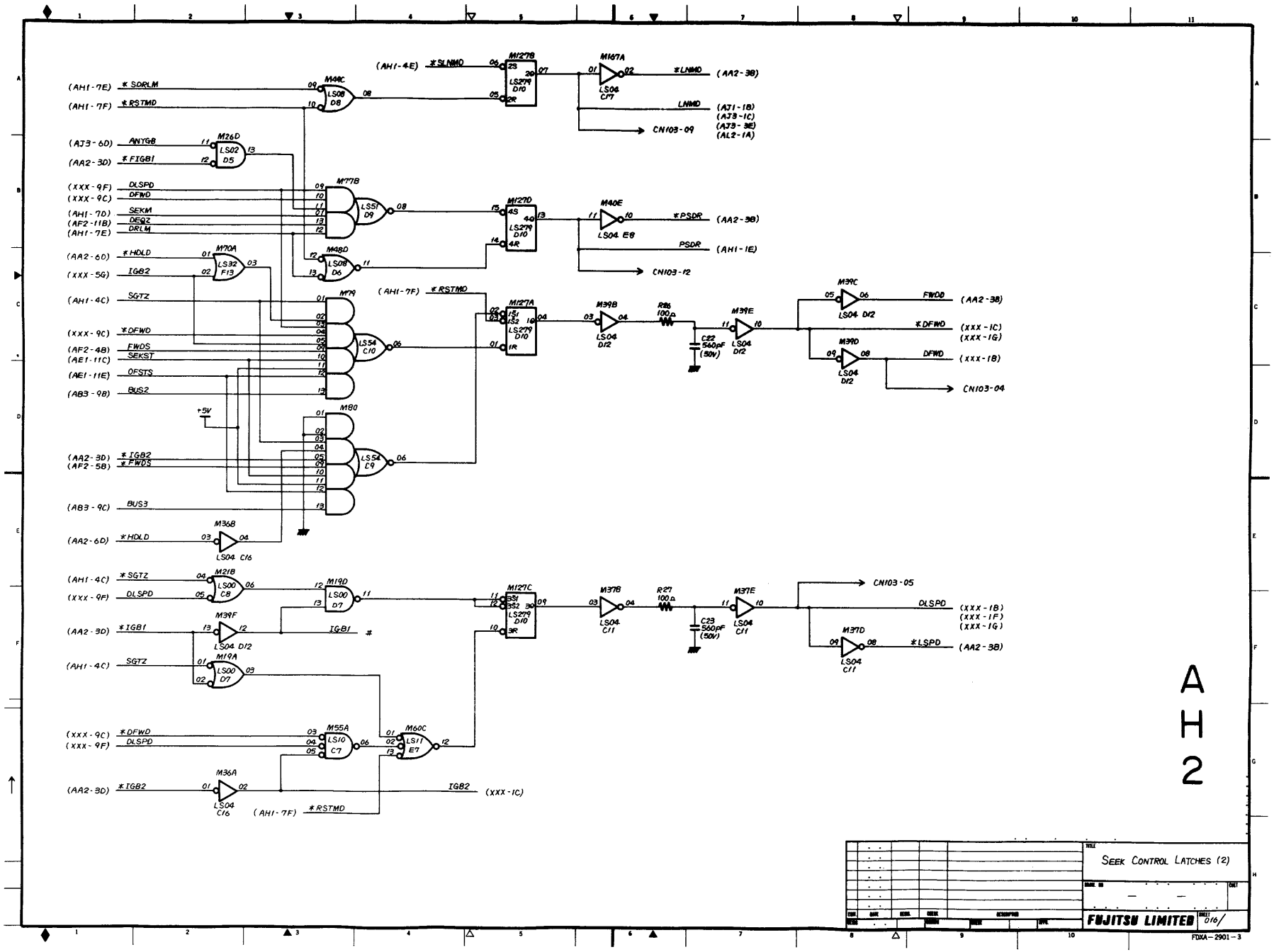
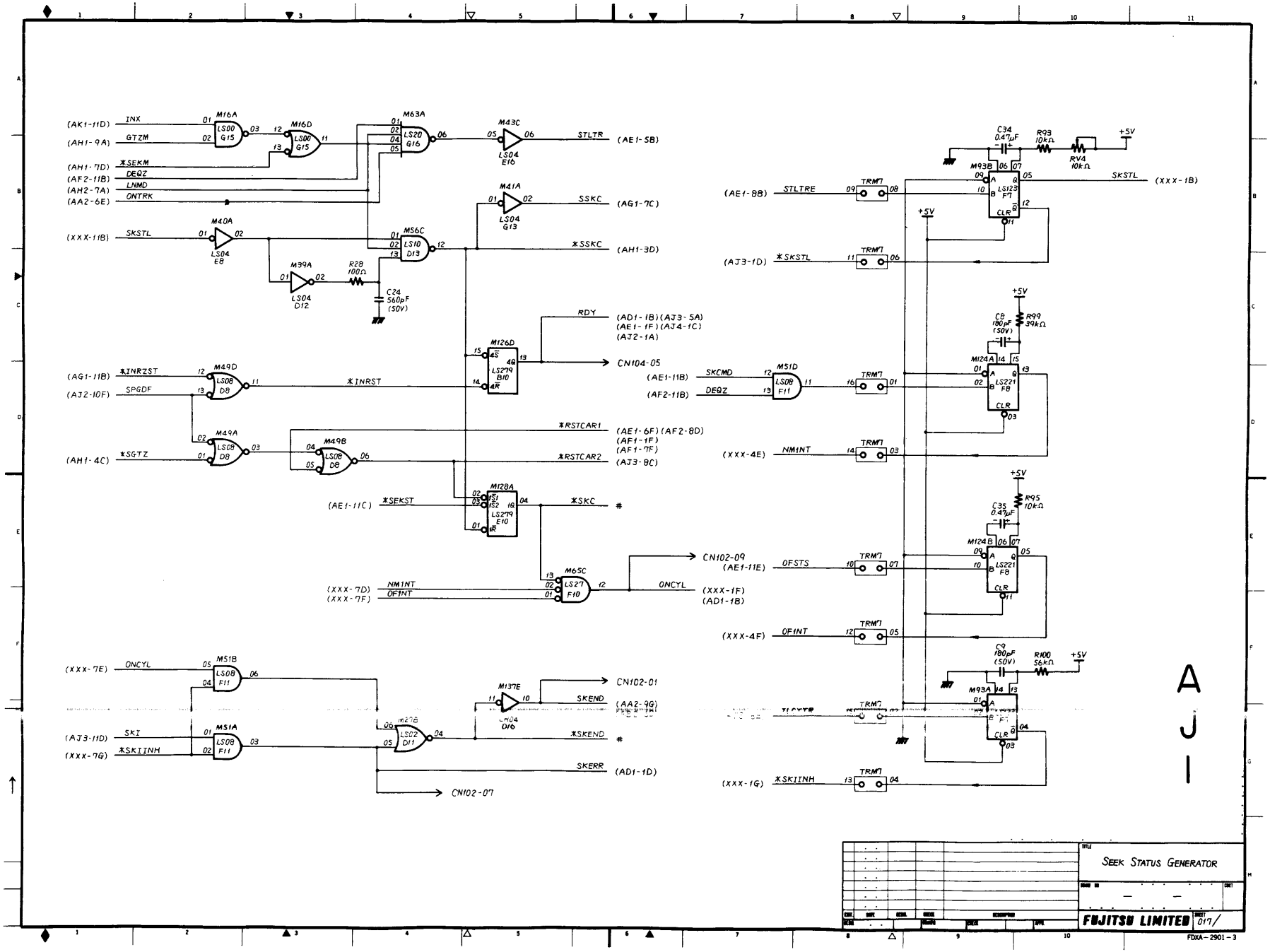
SEEK CONTROL LATCHES (1)
FUJITSU LIMITED
FDKA-2901-3


(AH1-7E) *SDRLM
(AH1-7F) *RSTMD
M44C LS08 D8
(AH1-4E) *SLNMD
M127B LS279 D10 2R
M167A LS04 C17
*LNMD (AA2-3B)
LNMD (AJ1-1B) (AJ3-1C) (AJ3-3E) (AL2-1A)
CN103-09
(AJ3-6D) ANYGB
(AA2-3D) *FIGB1
M26D LS02 D5
(XXX-9F) DLSPD
(XXX-9C) DFWD
(AH1-7D) SEKM
(AF2-11B) DEQZ
(AH1-7E) DRLM
M77B LS51 D9
M127D LS279 D10 4R
M140E LS04 E8
*PSDR (AA2-3B)
PSDR (AH1-1E)
CN103-12
(AA2-6D) *HDLD
(XXX-5G) IGB2
M70A LS32 F13
M48D LS08 D6
(AH1-4C) SGTZ
M79 LS54 C10
(AH1-7F) *RSTMD
M127A LS279 D10 1R
M139B LS04 D12
R86 100Ω
C22 560pF (50V)
M139E LS04 D12
M139C LS04 D12
FWDD (AA2-3B)
*DFWD (XXX-1C) (XXX-1G)
M139D LS04 D12
DFWD (XXX-1B)
CN103-04
(XXX-9C) *DFWD
(AF2-4B) FWDS
(AE1-11C) SEKST
(AE1-11E) OFSTS
(AB3-9B) BUS2
+5V
M80 LS54 C9
(AA2-3D) *IGB2
(AF2-5B) *FWDS
(AB3-9C) BUS3
(AA2-6D) *HDLD
M36B LS04 C16
(AH1-4C) *SGTZ
(XXX-9F) DLSPD
M21B LS00 C8
M19D LS00 D7
M127C LS279 D10 3R
M137B LS04 C11
R27 100Ω
C23 560pF (50V)
M137E LS04 C11
CN103-05
DLSPD (XXX-1B) (XXX-1F) (XXX-1G)
M137D LS04 C11
*LSPD (AA2-3B)
(AA2-3D) *IGB1
M38F LS04 D12
IGB1
M19A LS00 D7
(XXX-9C) *DFWD
(XXX-9F) DLSPD
M55A LS10 C7
M60C LS11 E7
(AA2-3D) *IGB2
M36A LS04 C16
IGB2 (XXX-1C)
(AH1-7F) *RSTMD
A H 2
SEEK CONTROL LATCHES (2)
FUJITSU LIMITED
FDXA-2901-3


(AK1-11D) INX
(AH1-9A) GTZM
(AH1-7D) *SEKM
(AF2-11B) DEQZ
(AH2-7A) LNMD
(AA2-6E) ONTRK
M16A LS00 G15
M16D LS00 G15
M63A LS20 G16
M43C LS04 E16
STLTR (AE1-5B)
M41A LS04 G13
SSKC (AG1-7C)
*SSKC (AH1-3D)
(XXX-11B) SKSTL
M40A LS04 E8
M56C LS10 D13
M39A LS04 D12
R28 100Ω
C24 560pF (50V)
RDY
(AD1-1B)(AJ3-5A)
(AE1-1F)(AJ4-1C)
(AJ2-1A)
M126D LS279 B10
CN104-05
(AG1-11B) *INRZST
(AJ2-10F) SPGDF
M49D LS08 D8
*INRST
M49A LS08 D8
M49B LS08 D8
(AH1-4C) *SGTZ
*RSTCAR1
(AE1-6F)(AF2-8D)
(AF1-1F)
(AF1-7F)
*RSTCAR2
(AJ3-8C)
M128A LS279 E10
(AE1-11C) *SEKST
*SKC #
M65C LS27 F10
(XXX-7D) NM1NT
(XXX-7F) OF1NT
ONCYL
CN102-09
(AE1-11E)
(XXX-1F)
(AD1-1B)
(XXX-7E) ONCYL
M51B LS08 F11
M137E LS04 D16
CN102-01
SKEND (AA2-9G)
(AJ3-11D) SKI
(XXX-7G) *SKIINH
M51A LS08 F11
M137B LS02 D11
*SKEND #
SKERR (AD1-1D)
CN102-07
+5V
C34 0.47μF
R93 10kΩ
RV4 10kΩ
M93B LS123 F7
SKSTL (XXX-1B)
(AE1-8B) STLTRE
TRM7
(AJ3-1D) *SKSTL
C8 180pF (50V)
R99 39kΩ
M124A LS221 F8
(AE1-11B) SKCMD
(AF2-11B) DEQZ
M51D LS08 F11
(XXX-4E) NM1NT
C35 0.47μF
R95 10kΩ
M124B LS221 F8
(XXX-4F) OF1NT
C9 180pF (50V)
R100 56kΩ
M93A LS123 F7
(XXX-1G) *SKIINH
A
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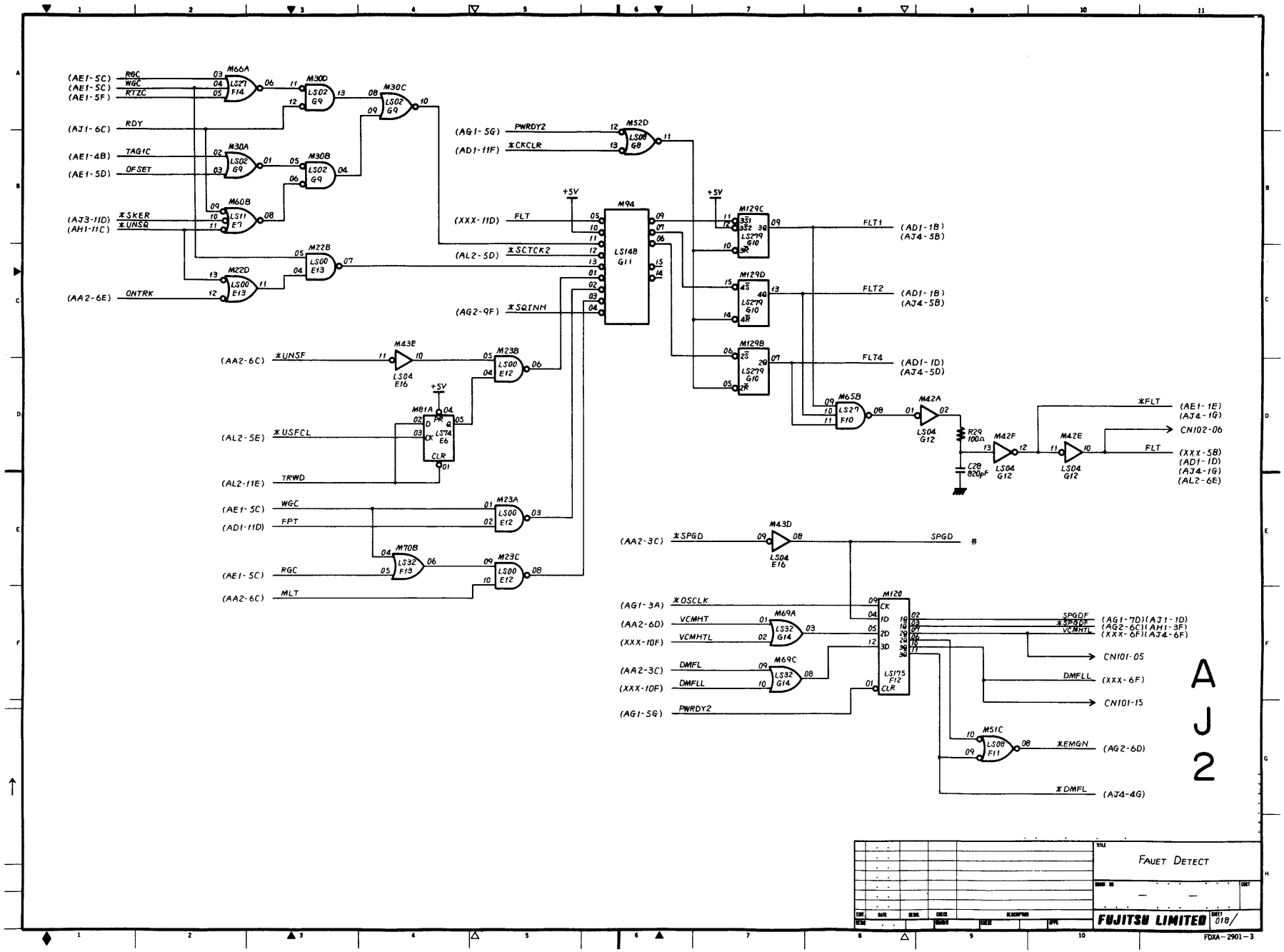
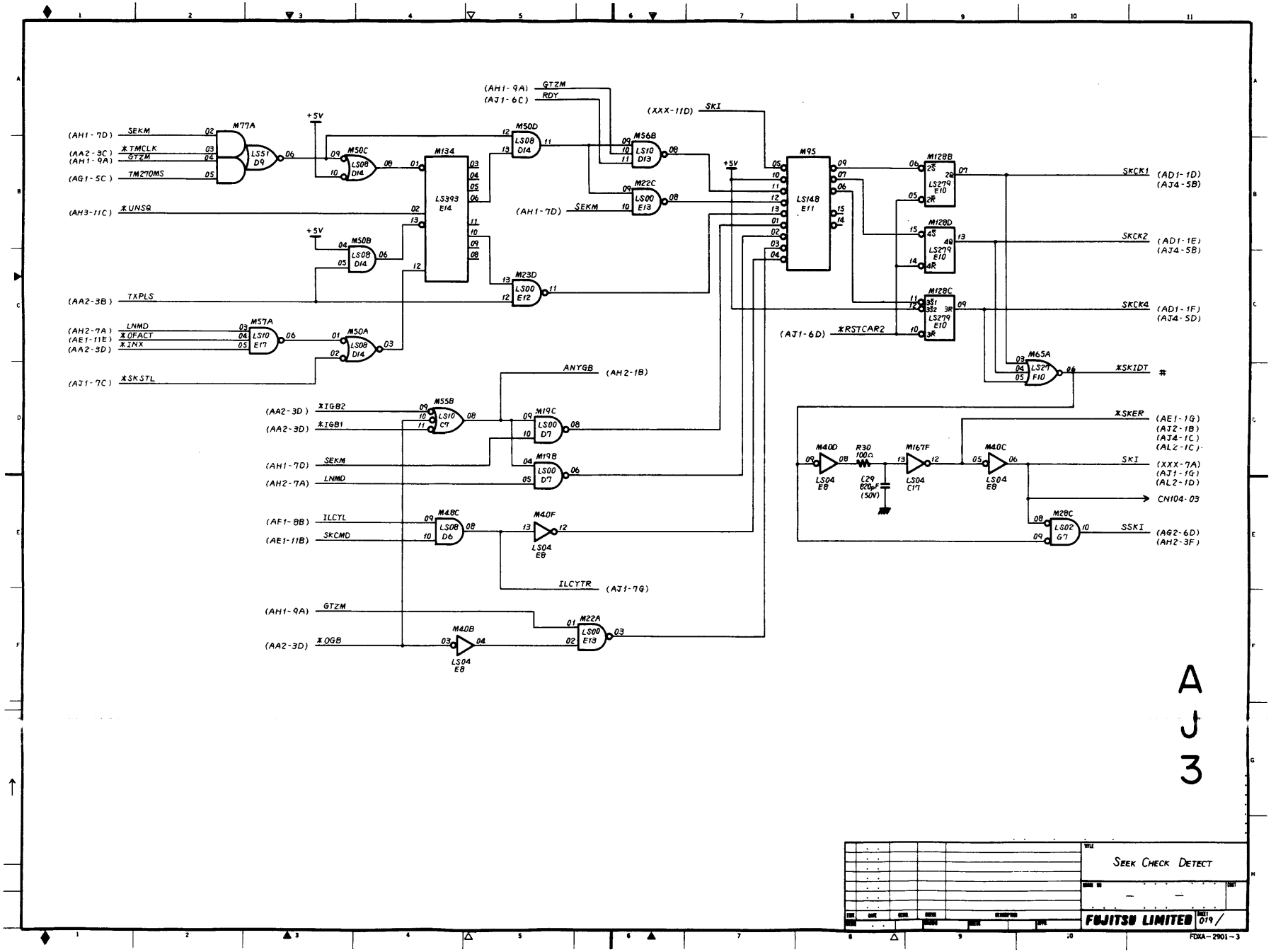
SEEK STATUS GENERATOR
FUJITSU LIMITED
FDXA-2901-3


(AE1-5C) RGC
(AE1-5C) WGC
(AE1-5F) RTZC
(AJ1-6C) RDY
(AE1-4B) TAG1C
(AE1-5D) OFSET
(AJ3-11D) *SKER
(AH1-11C) *UNSQ
(AA2-6E) ONTRK
M66A LS27 F14
M30D LS02 G9
M30C LS02 G9
M30A LS02 G9
M30B LS02 G9
M60B LS11 E7
M22B LS00 E13
M22D LS00 E13
(AG1-5G) PWRDY2
(AD1-11F) *CKCLR
M52D LS08 G8
(XXX-11D) FLT
(AL2-5D) *SCTCK2
(AG2-9F) *SQINH
M94 LS148 G11
+5V
M129C LS279 G10
M129D LS279 G10
M129B LS279 G10
FLT1
FLT2
FLT4
(AD1-1B) (AJ4-5B)
(AD1-1B) (AJ4-5B)
(AD1-1D) (AJ4-5D)
M65B LS27 F10
M42A LS04 G12
R29 100Ω
C28 820pF
M42F LS04 G12
M42E LS04 G12
*FLT
(AE1-1E) (AJ4-1G)
CN102-06
FLT
(XXX-5B) (AD1-1D) (AJ4-1G) (AL2-6E)
(AA2-6C) *UNSF
M43E LS04 E16
M23B LS00 E12
M81A LS74 E6
(AL2-5E) *USFCL
(AL2-11E) TRWD
(AE1-5C) WGC
(AD1-11D) FPT
M23A LS00 E12
M70B LS32 F13
(AE1-5C) RGC
(AA2-6C) MLT
M23C LS00 E12
(AA2-3C) *SPGD
M43D LS04 E16
SPGD #
(AG1-3A) *OSCLK
(AA2-6D) VCMHT
(XXX-10F) VCMHTL
M69A LS32 G14
(AA2-3C) DMFL
(XXX-10F) DMFLL
M69C LS32 G14
(AG1-5G) PWRDY2
M120 LS175 F12
SPGDF (AG1-7D)(AJ1-1D)
*SPGDF (AG2-6C)(AH1-3F)
VCMHTL (XXX-6F)(AJ4-6F)
CN101-05
DMFLL (XXX-6F)
CN101-15
M51C LS08 F11
*EMGN (AG2-6D)
*DMFL (AJ4-4G)
A J 2
FAUET DETECT
FUJITSU LIMITED
FDXA-2901-3


(AH1-7D) SEKM
(AA2-3C) *TMCLK
(AH1-9A) GTZM
(AG1-5C) TM270MS
(AH3-11C) *UNSQ
(AA2-3B) TXPLS
(AH2-7A) LNMD
(AE1-11E) *OFACT
(AA2-3D) *INX
(AJ1-7C) *SKSTL
(AA2-3D) *IGB2
(AA2-3D) *IGB1
(AH1-7D) SEKM
(AH2-7A) LNMD
(AF1-8B) ILCYL
(AE1-11B) SKCMD
(AH1-9A) GTZM
(AA2-3D) *OGB
(AH1-9A) GTZM
(AJ1-6C) RDY
(XXX-11D) SKI
(AH1-7D) SEKM
(AJ1-6D) *RSTCAR2
ANYGB (AH2-1B)
ILCYTR (AJ1-7G)
SKCK1 (AD1-1D) (AJ4-5B)
SKCK2 (AD1-1E) (AJ4-5B)
SKCK4 (AD1-1F) (AJ4-5D)
*SKIDT #
*SKER (AE1-1G) (AJ2-1B) (AJ4-1C) (AL2-1C)
SKI (XXX-7A) (AJ1-1G) (AL2-1D)
CN104-03
SSKI (AG2-6D) (AH2-3F)
M77A LS51 D9
M50C LS08 D14
M50D LS08 D14
M50B LS08 D14
M134 LS393 E14
M56B LS10 D13
M22C LS00 E13
M23D LS00 E12
M57A LS10 E17
M50A LS08 D14
M55B LS10 C7
M19C LS00 D7
M19B LS00 D7
M48C LS08 D6
M40F LS04 E8
M40B LS04 E8
M22A LS00 E13
M95 LS148 E11
M128B LS279 E10
M128D LS279 E10
M128C LS279 E10
M65A LS21 F10
M40D LS04 E8
R30 100Ω
C29 820pF (50V)
M167F LS04 C17
M40C LS04 E8
M28C LS02 G7
+5V
A
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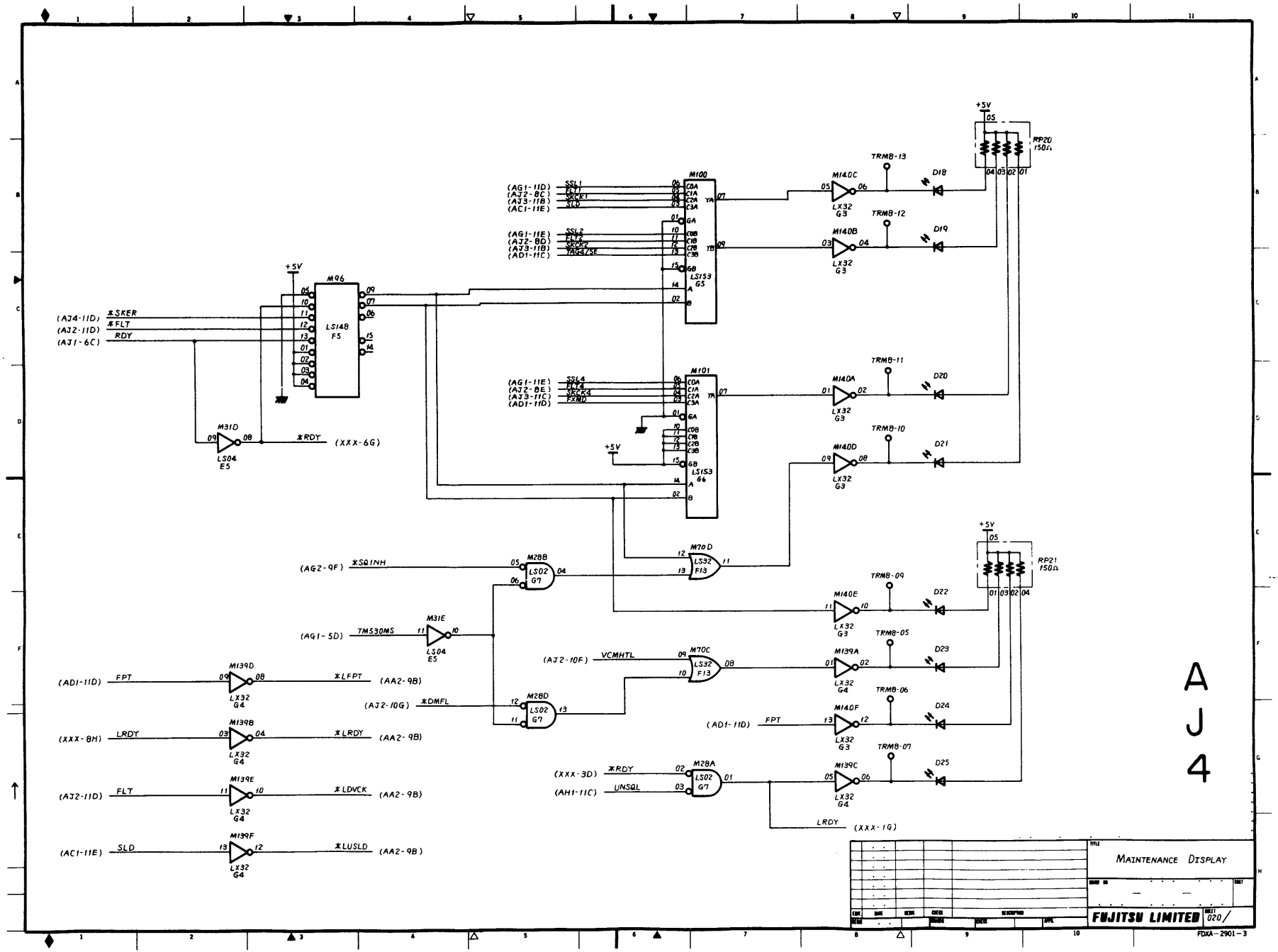
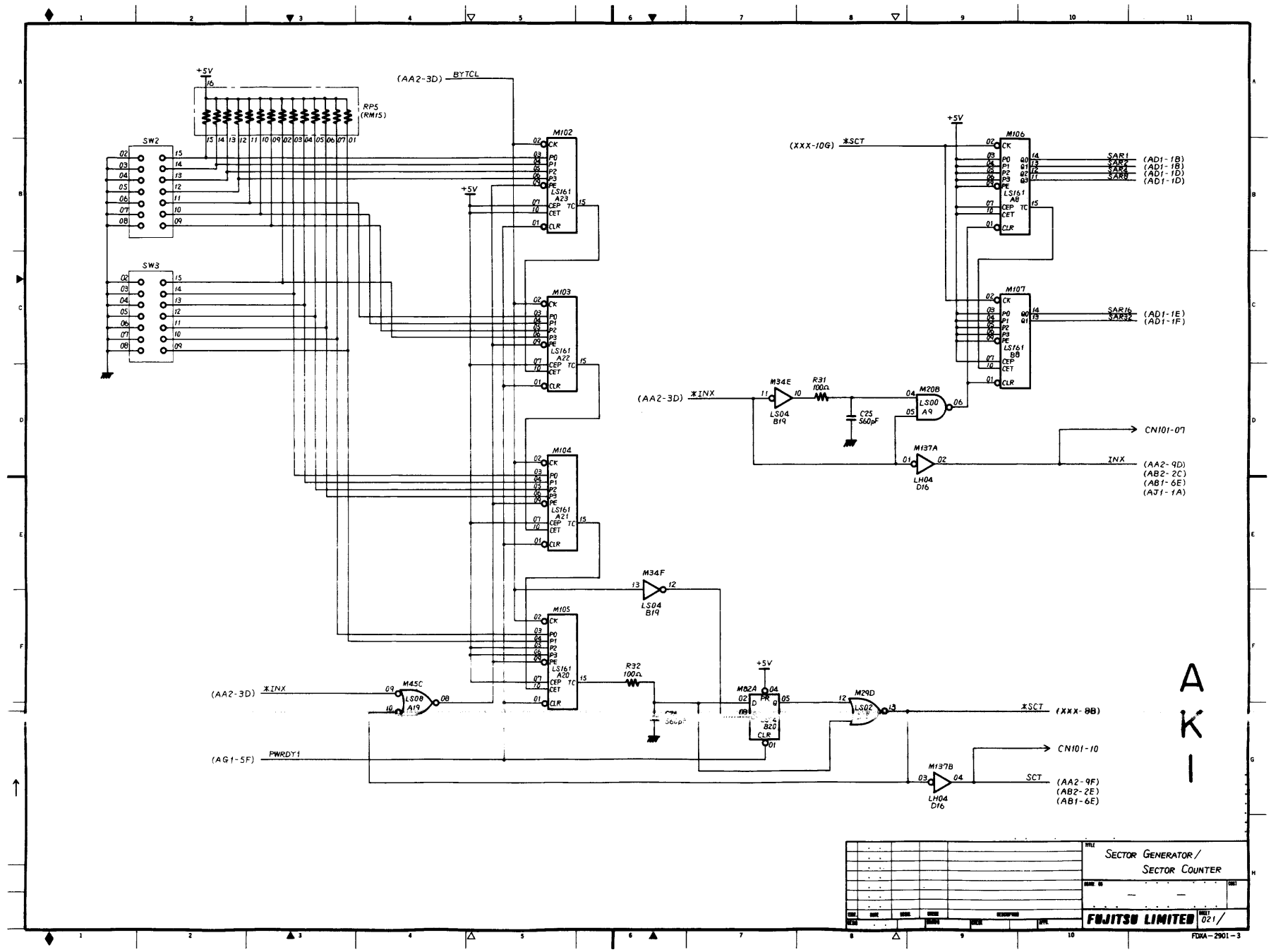
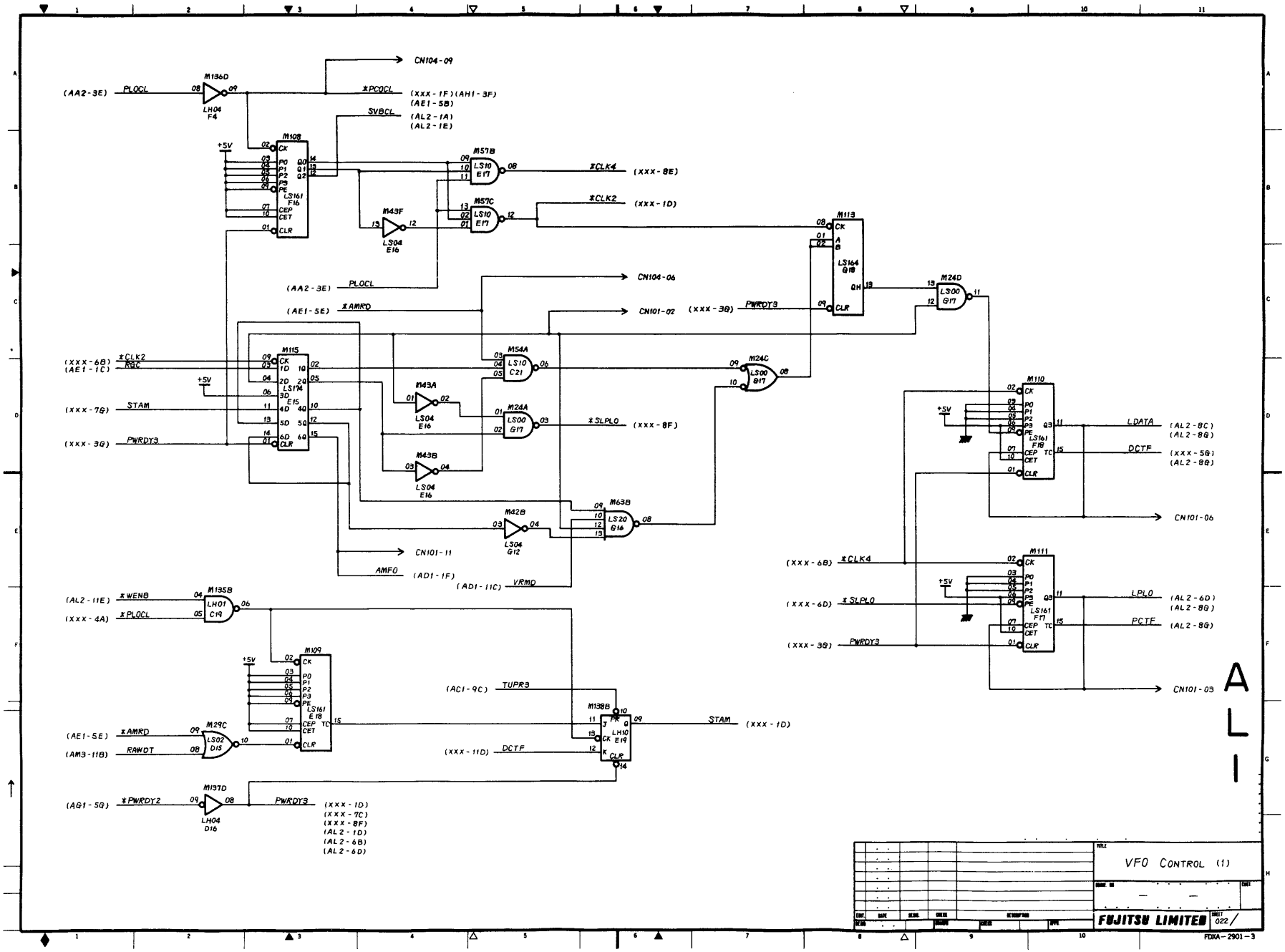
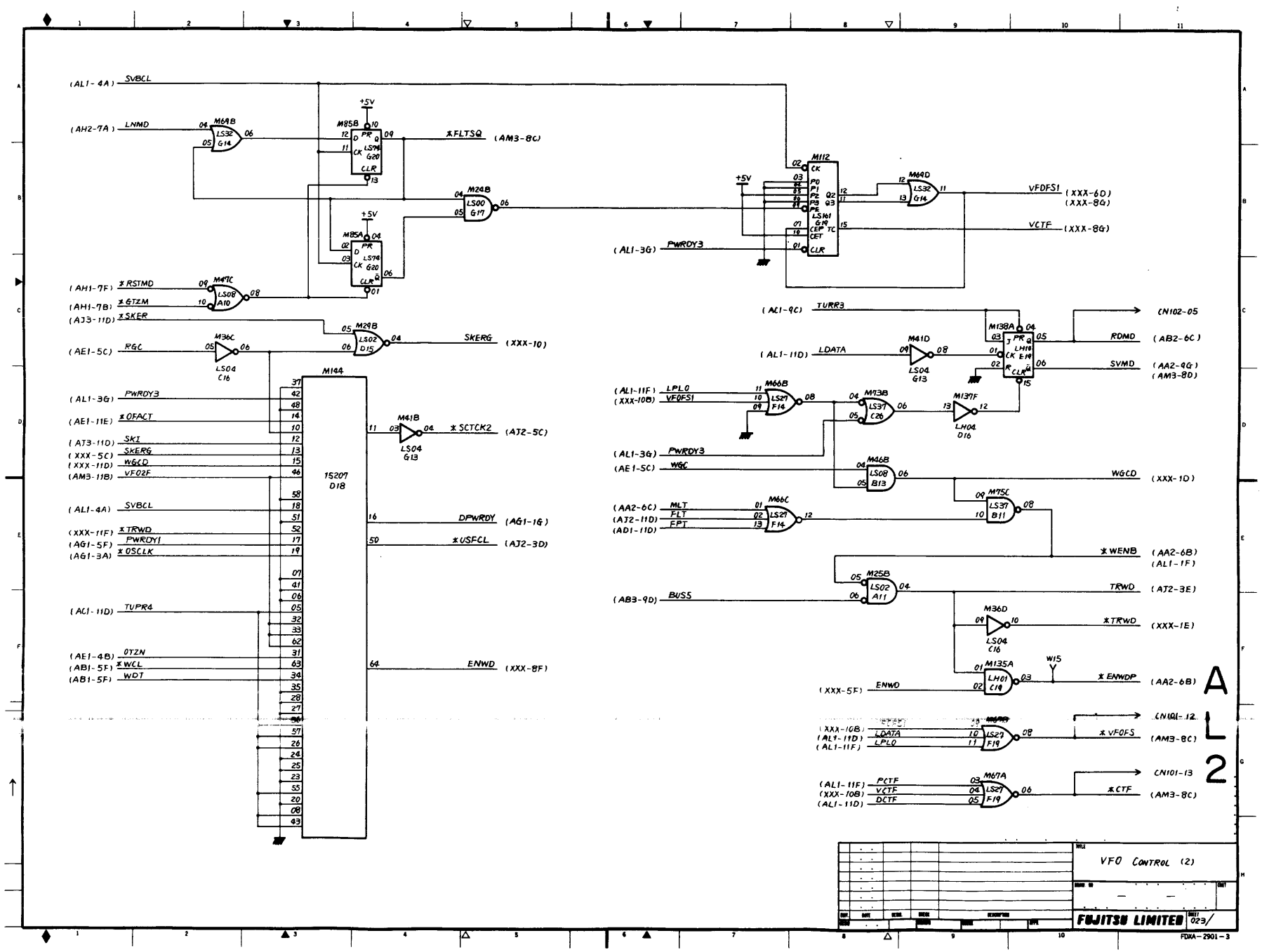
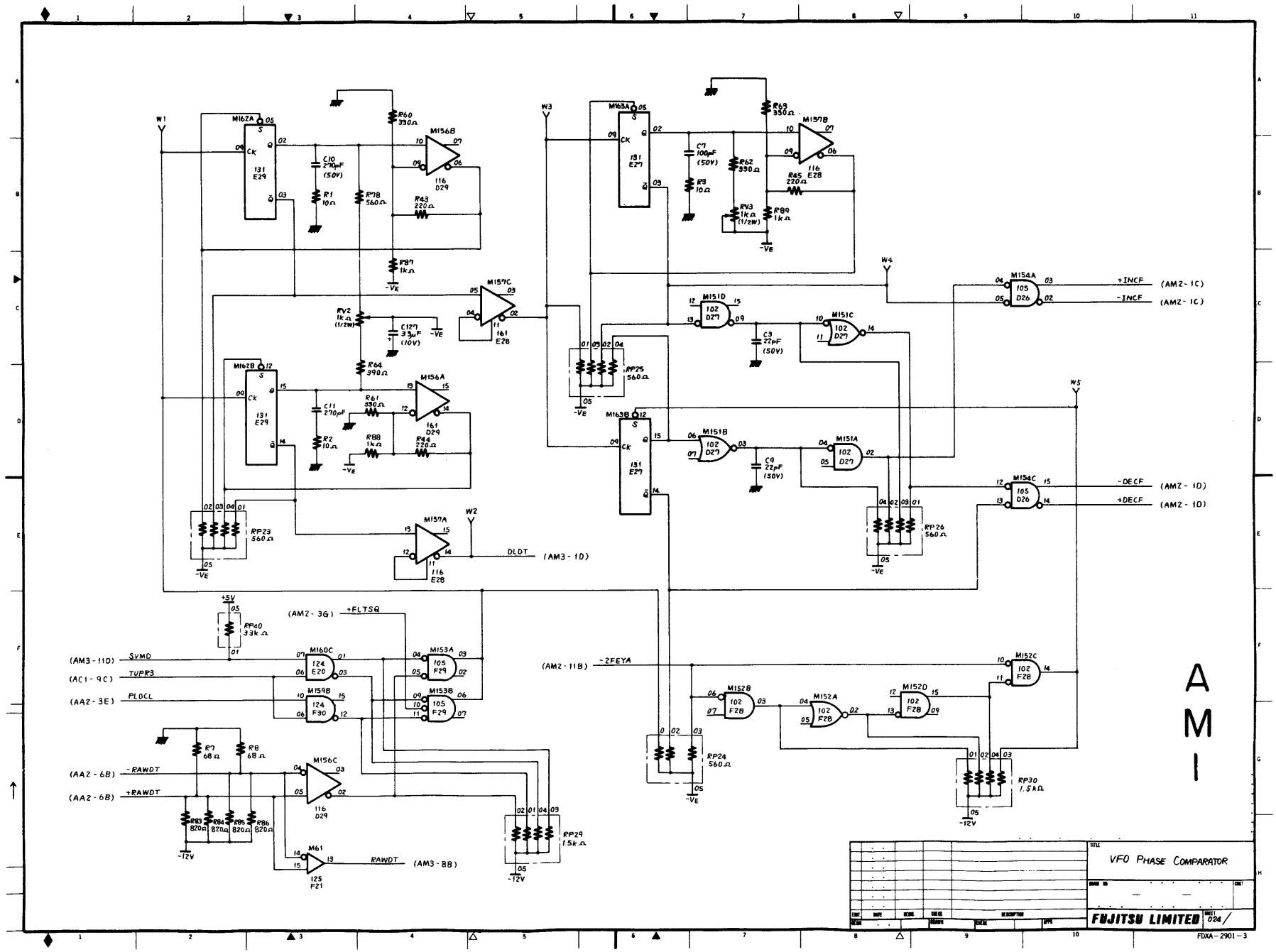
SEEK CHECK DETECT
FUJITSU LIMITED
FDXA-2901-3

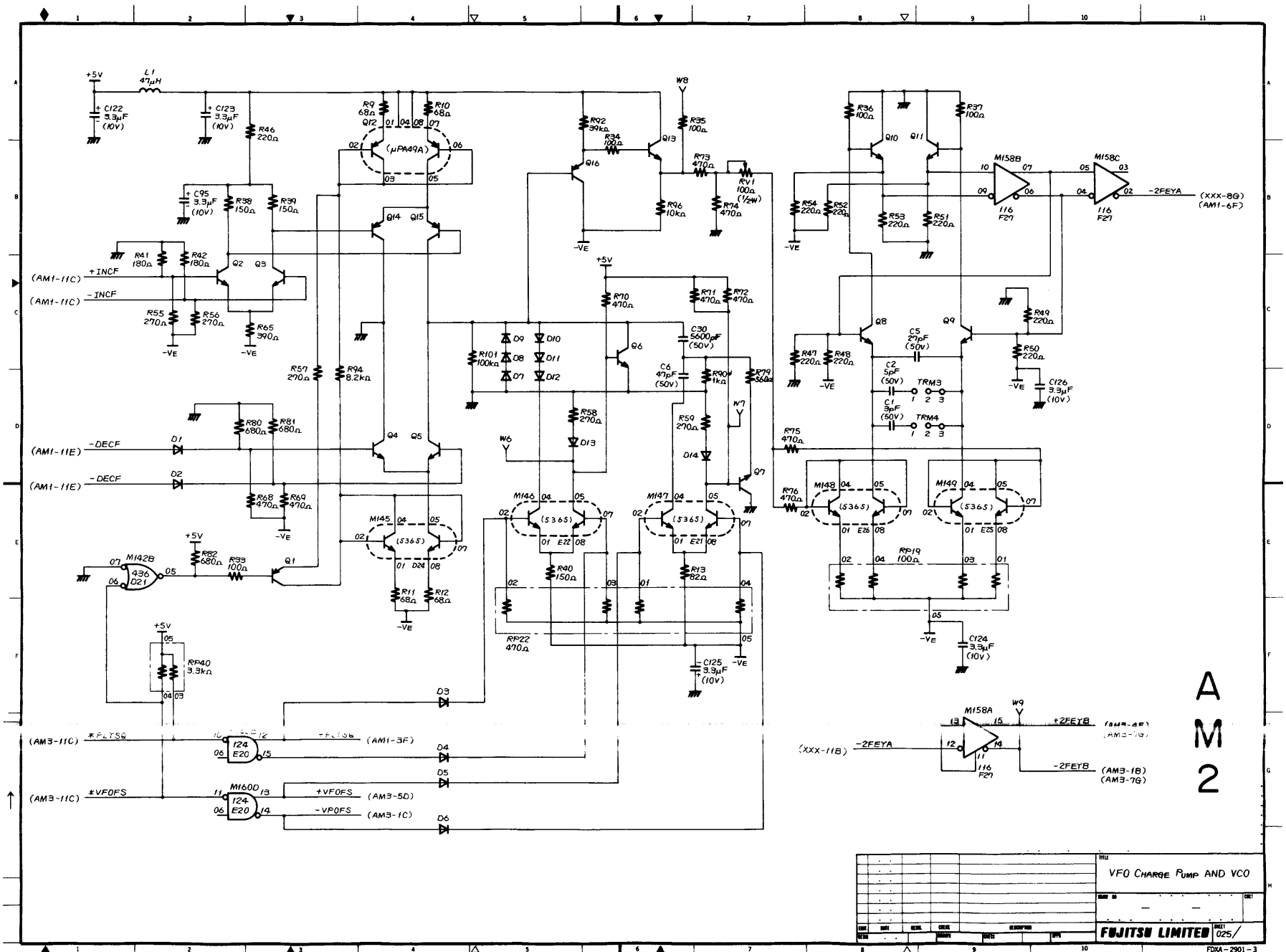

A
J
4
MAINTENANCE DISPLAY
FUJITSU LIMITED
FDXA-2901-3
M100
M101
M96
M31D
M31E
M28B
M28D
M28A
M70D
M70C
M140C
M140B
M140A
M140D
M140E
M140F
M139C
M139A
M139B
M139D
M139E
M139F
LS153 G5
LS153 G6
LS148 F5
LS04 E5
LS02 G7
LS32 F13
LX32 G3
LX32 G4
RP20 150Ω
RP21 150Ω
+5V
TRM8-13
TRM8-12
TRM8-11
TRM8-10
TRM8-09
TRM8-05
TRM8-06
TRM8-07
D18
D19
D20
D21
D22
D23
D24
D25
(AG1-11D) SSL1
(AJ2-8C) FLT1
(AJ3-11B) SRCRT
(AC1-11E) SLD
(AG1-11E) SSL2
(AJ2-8D) FLT2
(AJ3-11B) SRCRT2
(AD1-11C) TAG475E
(AG1-11E) SSL4
(AJ2-8E) FLT4
(AJ3-11C) SRCRT4
(AD1-11D) TXMD
(AJ4-11D) *SKER
(AJ2-11D) *FLT
(AJ1-6C) RDY
*RDY (XXX-6G)
(AG2-9F) *SQINH
(AG1-5D) TM530MS
(AJ2-10F) VCMHTL
(AJ2-10G) *DMFL
(AD1-11D) FPT
*LFPT (AA2-9B)
(XXX-8H) LRDY
*LRDY (AA2-9B)
(AJ2-11D) FLT
*LDVCK (AA2-9B)
(AC1-11E) SLD
*LUSLD (AA2-9B)
(XXX-3D) *RDY
(AH1-11C) UNSQL
LRDY (XXX-1G)

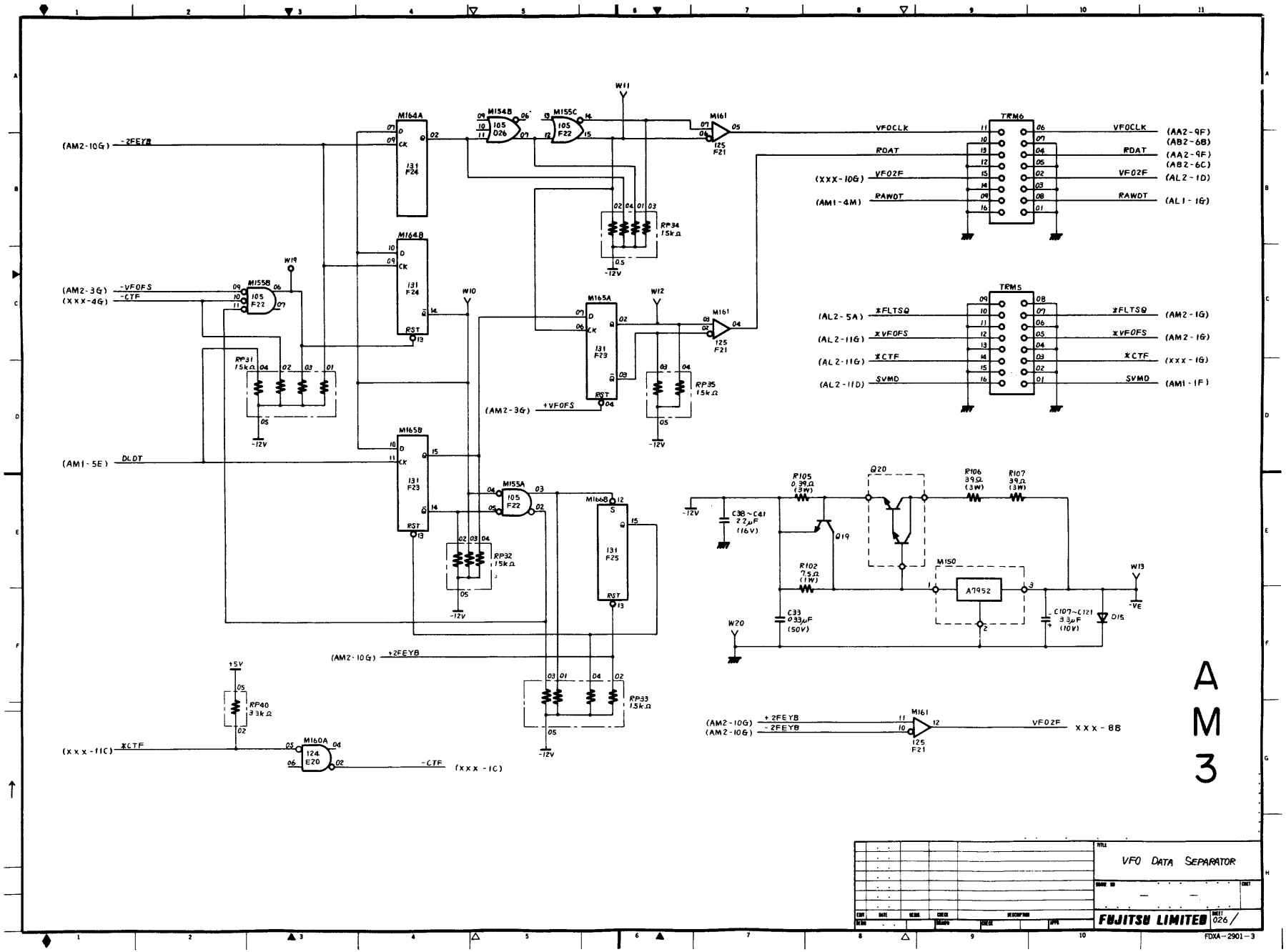

+5V
RP5 (RM15)
SW2
SW3
(AA2-3D) BYTCL
M102
M103
M104
M105
M106
M107
LS161
(XXX-10G) *SCT
SAR1 (AD1-1B)
SAR2 (AD1-1B)
SAR4 (AD1-1D)
SAR8 (AD1-1D)
SAR16 (AD1-1E)
SAR32 (AD1-1F)
(AA2-3D) *INX
M34E
LS04 B19
R31 100Ω
C25 560pF
M20B
LS00 A9
CN101-07
M137A
LH04 D16
INX
(AA2-9D)
(AB2-2C)
(AB1-6E)
(AJ1-1A)
M34F
R32 100Ω
M45C
LS08 A19
M82A
LS02
M29D
*SCT (XXX-8B)
CN101-10
(AG1-5F) PWRDY1
M137B
SCT
(AA2-9F)
(AB2-2E)
(AB1-6E)
SECTOR GENERATOR / SECTOR COUNTER
FUJITSU LIMITED
FDXA-2901-3

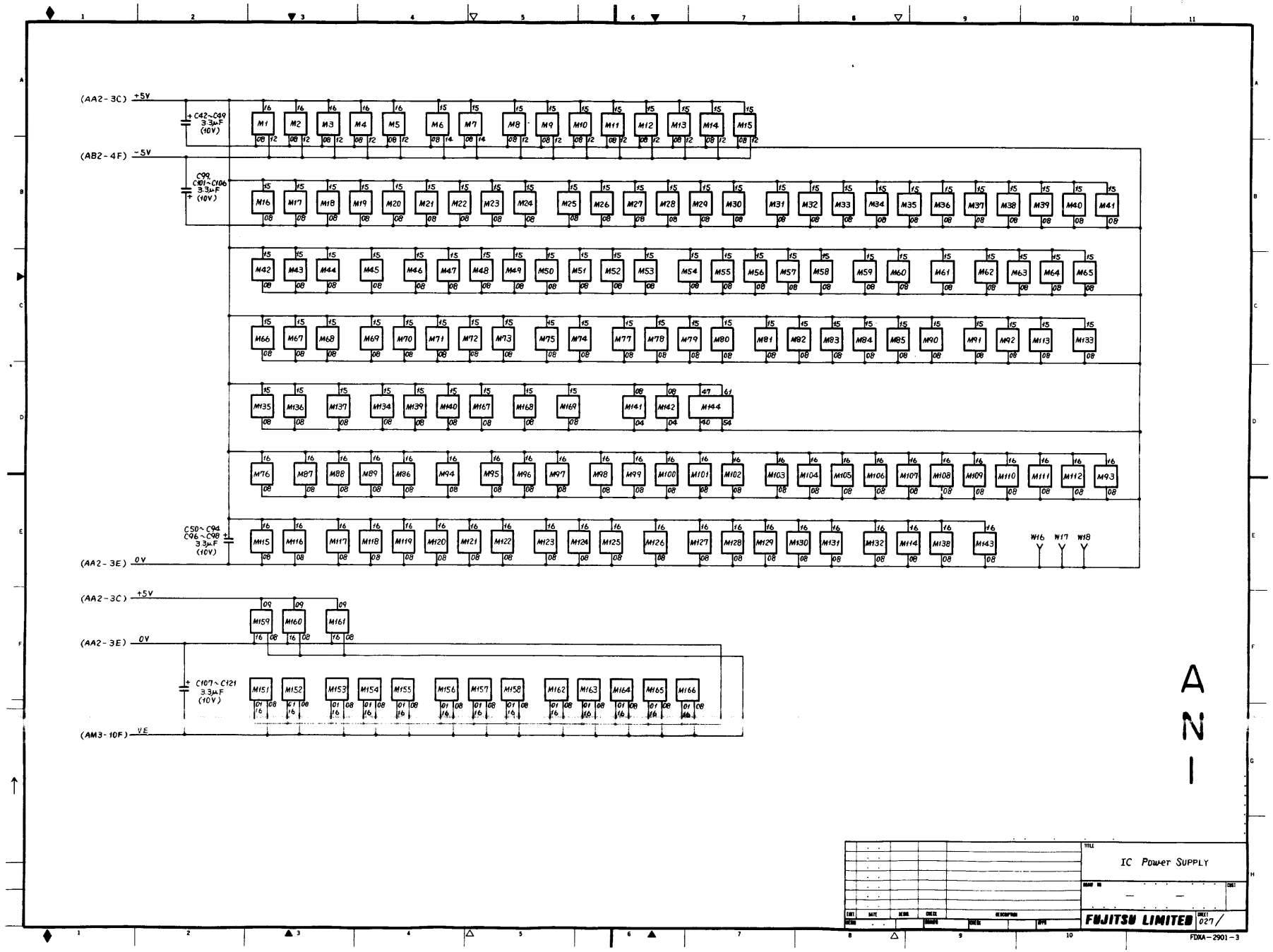

CN104-09
(AA2-3E) PLOCL
M136D LH04 F4
*PCOCL
(xxx-1F)(AH1-3F) (AE1-5B)
SVBCL
(AL2-1A) (AL2-1E)
M108 LS161 F16
M57B LS10 E17
*CLK4 (xxx-8E)
M57C LS10 E17
*CLK2 (xxx-1D)
M43F LS04 E16
M113 LS164 G18
(AA2-3E) PLOCL
CN104-06
(AE1-5E) *AMRD
CN101-02
(xxx-3B) PWRDY3
M24D LS00 G17
M115 LS174 E15
(xxx-6B) *CLK2
(AE1-1C) RSC
(xxx-7G) STAM
(xxx-3G) PWRDY3
M54A LS10 C21
M24C LS00 B17
M43A LS04 E16
M24A LS00 G17
*SLPLO (xxx-8F)
M43B LS04 E16
M42B LS04 G12
M63B LS20 G16
CN101-11
AMF0 (AD1-1F)
(AD1-11C) VRMD
M110 LS161 F18
LDATA (AL2-8C) (AL2-8G)
DCTF (xxx-5G) (AL2-8B)
CN101-06
M111 LS161 F17
(xxx-6B) *CLK4
(xxx-6D) *SLPLO
(xxx-3B) PWRDY3
LPLO (AL2-6D) (AL2-8B)
PCTF (AL2-8G)
CN101-03
M135B LH01 C19
(AL2-11E) *WENB
(xxx-4A) *PLOCL
M109 LS161 E18
(AE1-5E) *AMRD
(AM3-11B) RAWDT
M29C LS02 D15
(AC1-9C) TUPR3
M138B LH10 E19
STAM (xxx-1D)
(xxx-11D) DCTF
M137D LH04 D16
(AG1-5G) *PWRDY2
PWRDY3
(xxx-1D) (xxx-7C) (xxx-8F) (AL2-1D) (AL2-6B) (AL2-6D)
A L I
VFO CONTROL (1)
FUJITSU LIMITED
FDXA-2901-3


VFO CONTROL (2)
FUJITSU LIMITED
FDXA-2901-3
A L 2
15207 D18
M144
SVBCL
LNMD
*FLTSQ
PWRDY3
*RSTMD
*GTZM
*SKER
RGC
SKERG
*OFACT
SKI
WGCD
VF02F
TRWD
PWRDY1
*OSCLK
TUPR4
OTZN
*WCL
WDT
*SCTCK2
DPWRDY
*USFCL
ENWD
TURR3
LDATA
LPLO
VFOFS1
WGC
MLT
FLT
EPT
BUSS
*WENB
TRWD
*TRWD
*ENWDP
*VFOFS
*CTF
PCTF
VCTF
OCTF
RDMD
SVMD
WI5


W1
W2
W3
W4
W5
M162A
M156B
M157C
M162B
M156A
M163A
M157B
M154A
M151D
M151C
M163B
M151B
M151A
M154C
M157A
M160C
M153A
M159B
M153B
M156C
M61
M152C
M152B
M152A
M152D
R60 330Ω
R78 560Ω
R43 220Ω
R87 1kΩ
R64 390Ω
R61 330Ω
R88 1kΩ
R44 220Ω
R69 330Ω
R62 330Ω
R45 220Ω
R89 1kΩ
C10 270pF (50V)
C11 270pF
C7 100pF (50V)
C127 3.3μF (10V)
C3 22pF (50V)
C9 22pF (50V)
RV2 1kΩ (1/2W)
RV3 1kΩ (1/2W)
R1 10Ω
R2 10Ω
R3 10Ω
RP23 560Ω
RP25 560Ω
RP26 560Ω
RP24 560Ω
RP40 33kΩ
RP30 1.5kΩ
RP29 15kΩ
R7 68Ω
R8 68Ω
R83 820Ω
R84 820Ω
R85 820Ω
R86 820Ω
+5V
-12V
-Ve
+INCF (AM2-1C)
-INCF (AM2-1C)
-DECF (AM2-1D)
+DECF (AM2-1D)
DLDT (AM3-1D)
(AM2-3G) +FLTSQ
(AM3-11D) SVMD
(AC1-9C) TUPR3
(AA2-3E) PLOCL
(AM2-11B) -2FEYA
(AA2-6B) -RAWDT
(AA2-6B) +RAWDT
RAWDT (AM3-8B)
A
M
I
VFO PHASE COMPARATOR
FUJITSU LIMITED
FDXA-2901-3


VFO CHARGE PUMP AND VCO
FUJITSU LIMITED
FDXA-2901-3
AM2
+5V
L1 47μH
C122 3.3μF (10V)
C123 3.3μF (10V)
C95 3.3μF (10V)
C124 3.3μF (10V)
C125 3.3μF (10V)
C126 3.3μF (10V)
R46 220Ω
R38 150Ω
R39 150Ω
R41 180Ω
R42 180Ω
R55 270Ω
R56 270Ω
R65 390Ω
R57 270Ω
R94 8.2kΩ
R80 680Ω
R81 680Ω
R68 470Ω
R69 470Ω
R82 680Ω
R83 100Ω
R9 68Ω
R10 68Ω
R11 68Ω
R12 68Ω
R92 39kΩ
R34 100Ω
R35 100Ω
R73 470Ω
R96 10kΩ
R74 470Ω
RV1 100Ω (1/2W)
R70 470Ω
R71 470Ω
R72 470Ω
R101 100kΩ
C30 5600pF (50V)
C6 47pF (50V)
R90 1kΩ
R79 560Ω
R58 270Ω
R59 270Ω
R40 150Ω
R13 82Ω
RP22 470Ω
RP40 3.3kΩ
R36 100Ω
R37 100Ω
R54 220Ω
R52 220Ω
R53 220Ω
R51 220Ω
R49 220Ω
R50 220Ω
R47 220Ω
R48 220Ω
C5 27pF (50V)
C2 5pF (50V)
C1 3pF (50V)
TRM3
TRM4
R75 470Ω
R76 470Ω
RP19 100Ω
M142B
M145
M146
M147
M148
M149
M158A
M158B
M158C
M160D
(5365)
(μPA49A)
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
W6 W7 W8 W9
+INCF (AM1-11C)
-INCF (AM1-11C)
-DECF (AM1-11E)
-DECF (AM1-11E)
*PLTSQ (AM3-11C)
*VFOFS (AM3-11C)
+PLTSQ (AM1-3F)
+VFOFS (AM3-5D)
-VFOFS (AM3-1C)
-2FEYA (XXX-8G) (AM1-6F)
(XXX-11B) -2FEYA
+2FEYB (AM3-6F) (AM3-1G)
-2FEYB (AM3-1B) (AM3-7G)
-VE


(AM2-10G) -2FEYB
M164A
131 F24
M154B 105 D26
M155C 105 F22
W11
M161 125 F21
VFOCLK
RDAT
(XXX-10G) VF02F
(AM1-4M) RAWDT
TRM6
VFOCLK (AA2-9F) (AB2-6B)
RDAT (AA2-9F) (AB2-6C)
VF02F (AL2-1D)
RAWDT (AL1-1G)
RP34 15kΩ
M164B
W9
(AM2-3G) -VFOFS
(XXX-4G) -CTF
M155B 105 F22
W10
RP31 15kΩ
-12V
M165A
W12
M161 125 F21
(AM2-3G) +VFOFS
RP35 15kΩ
TRM5
(AL2-5A) *FLTSQ
(AL2-11G) *VFOFS
(AL2-11G) *CTF
(AL2-11D) SVMD
*FLTSQ (AM2-1G)
*VFOFS (AM2-1G)
*CTF (XXX-1G)
SVMD (AM1-1F)
(AM1-5E) DLDT
M165B
131 F23
M155A 105 F22
M166B
131 F25
RP32 15kΩ
R105 0.39Ω (3W)
Q20
R106 39Ω (3W)
R107 39Ω (3W)
C38~C41 22μF (16V)
Q19
R102 7.5Ω (1W)
M150
A7952
W13
-VE
C107~C121 3.3μF (10V)
D15
C33 0.33μF (50V)
W20
(AM2-10G) +2FEYB
RP33 15kΩ
+5V
RP40 33kΩ
(XXX-11C) XCTF
M160A 124 E20
-CTF (XXX-1C)
(AM2-10G) +2FEYB
(AM2-10G) -2FEYB
M161 125 F21
VF02F XXX-8B
A M 3
VFO DATA SEPARATOR
FUJITSU LIMITED
FDXA-2901-3


(AA2-3C) +5V
(AB2-4F) -5V
(AA2-3E) 0V
(AA2-3C) +5V
(AA2-3E) 0V
(AM3-10F) VE
C42~C49 3.3μF (10V)
C99, C101~C106 3.3μF (10V)
C50~C94, C96~C98 3.3μF (10V)
C107~C121 3.3μF (10V)
M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15
M16 M17 M18 M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 M29 M30 M31 M32 M33 M34 M35 M36 M37 M38 M39 M40 M41
M42 M43 M44 M45 M46 M47 M48 M49 M50 M51 M52 M53 M54 M55 M56 M57 M58 M59 M60 M61 M62 M63 M64 M65
M66 M67 M68 M69 M70 M71 M72 M73 M75 M74 M77 M78 M79 M80 M81 M82 M83 M84 M85 M90 M91 M92 M113 M133
M135 M136 M137 M134 M139 M140 M167 M168 M169 M141 M142 M144
M76 M87 M88 M89 M86 M94 M95 M96 M97 M98 M99 M100 M101 M102 M103 M104 M105 M106 M107 M108 M109 M110 M111 M112 M93
M115 M116 M117 M118 M119 M120 M121 M122 M123 M124 M125 M126 M127 M128 M129 M130 M131 M132 M114 M138 M143
W16 W17 W18
M159 M160 M161
M151 M152 M153 M154 M155 M156 M157 M158 M162 M163 M164 M165 M166
IC Power Supply
FUJITSU LIMITED
FDXA-2901-3

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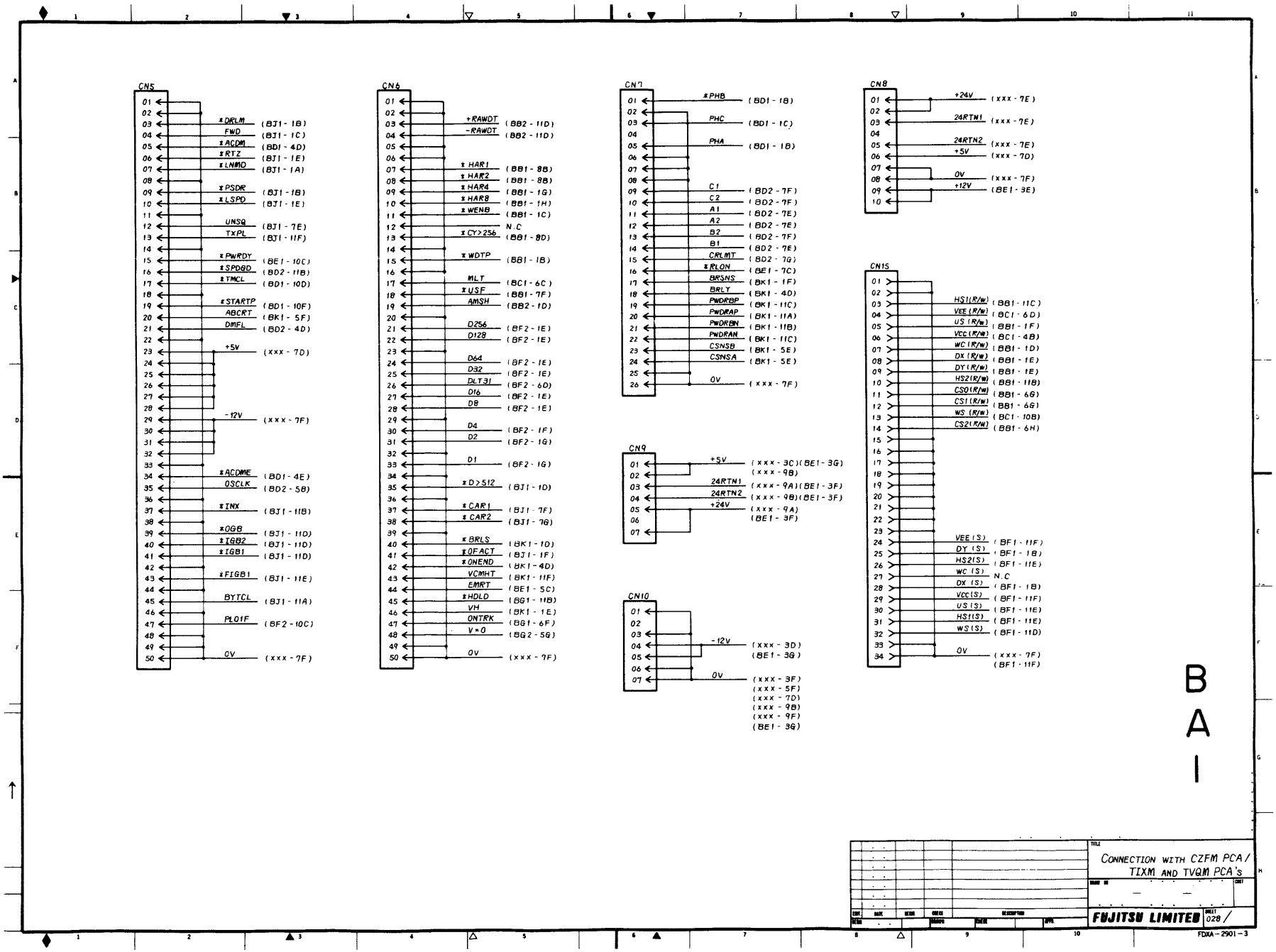
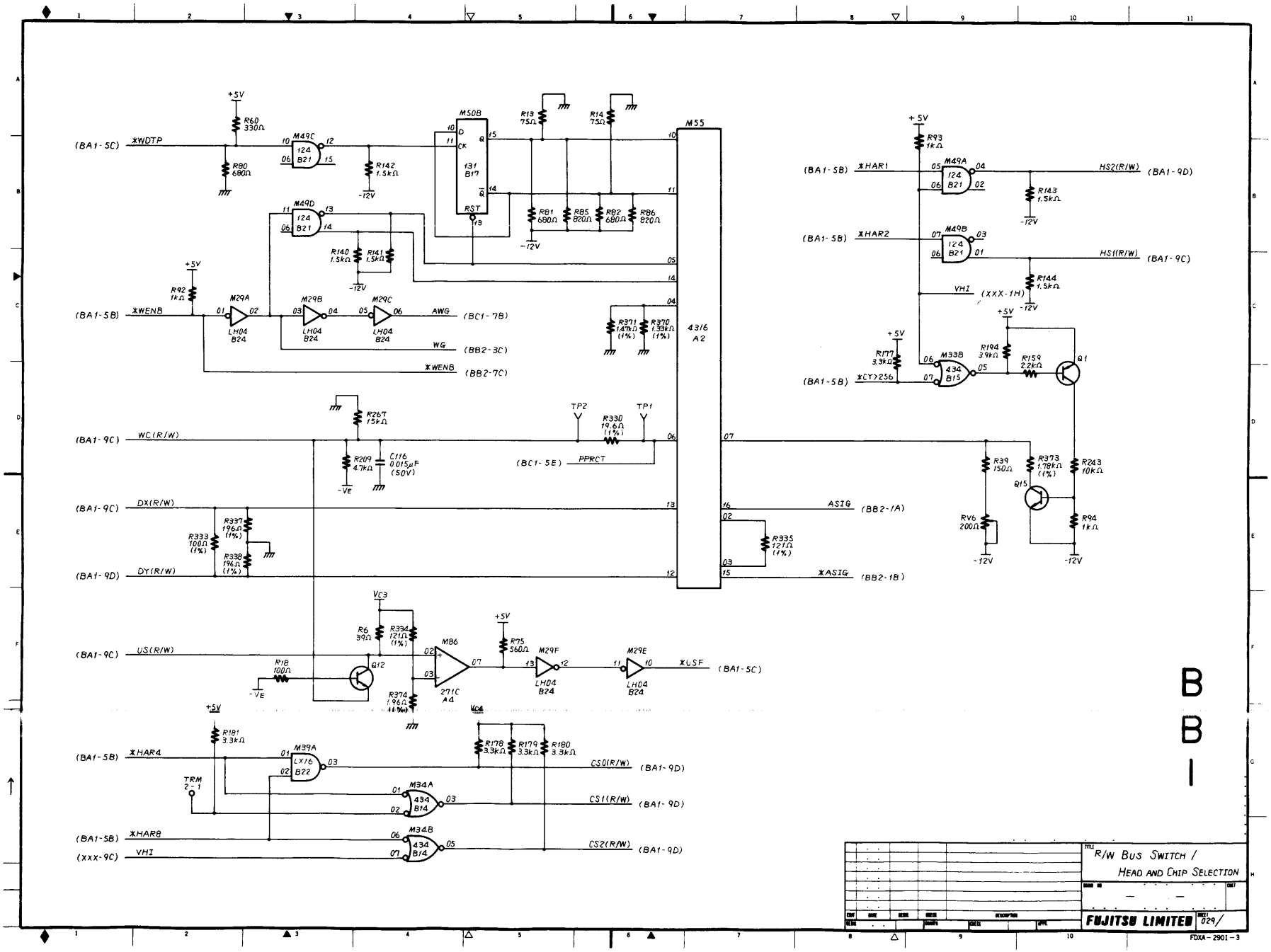
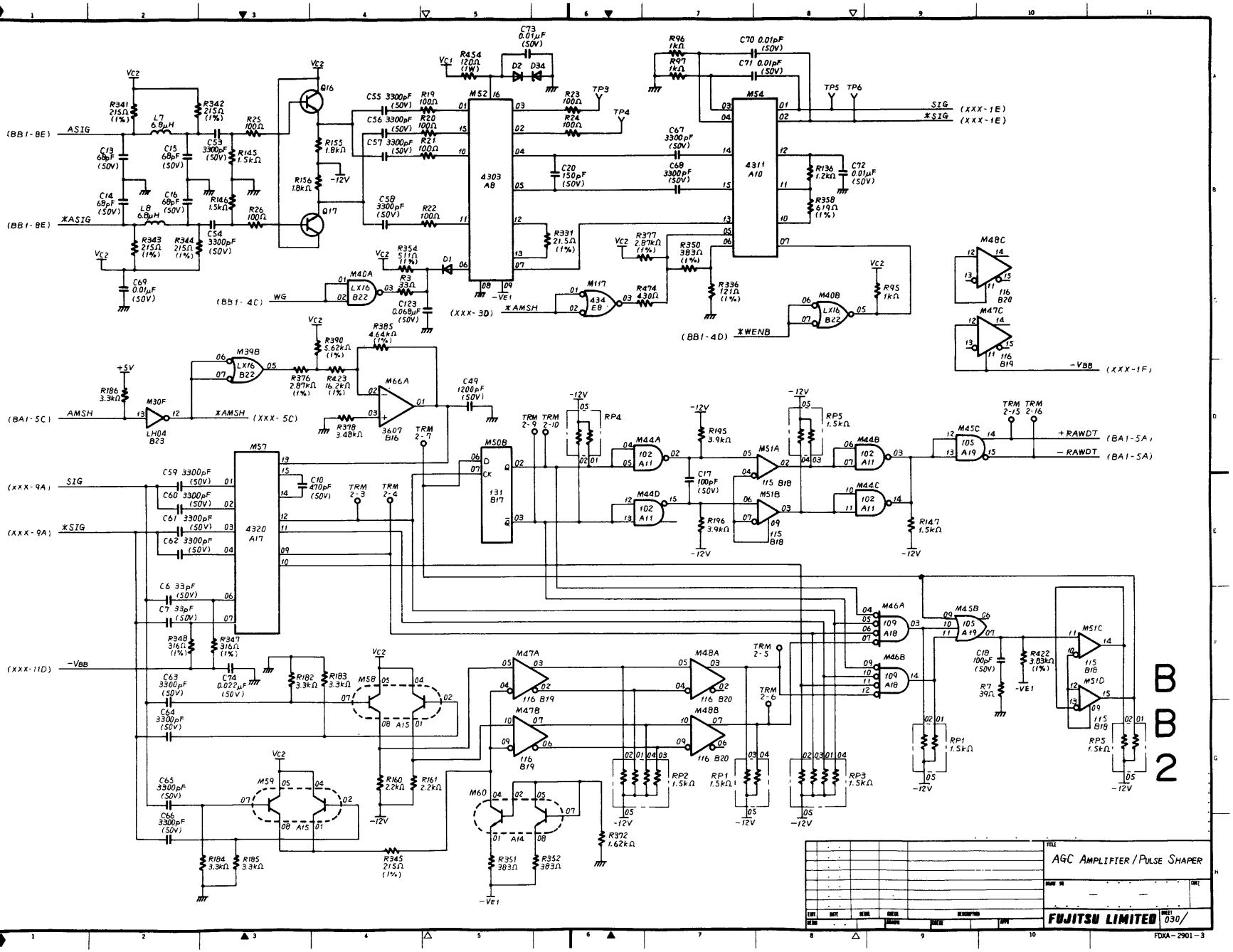
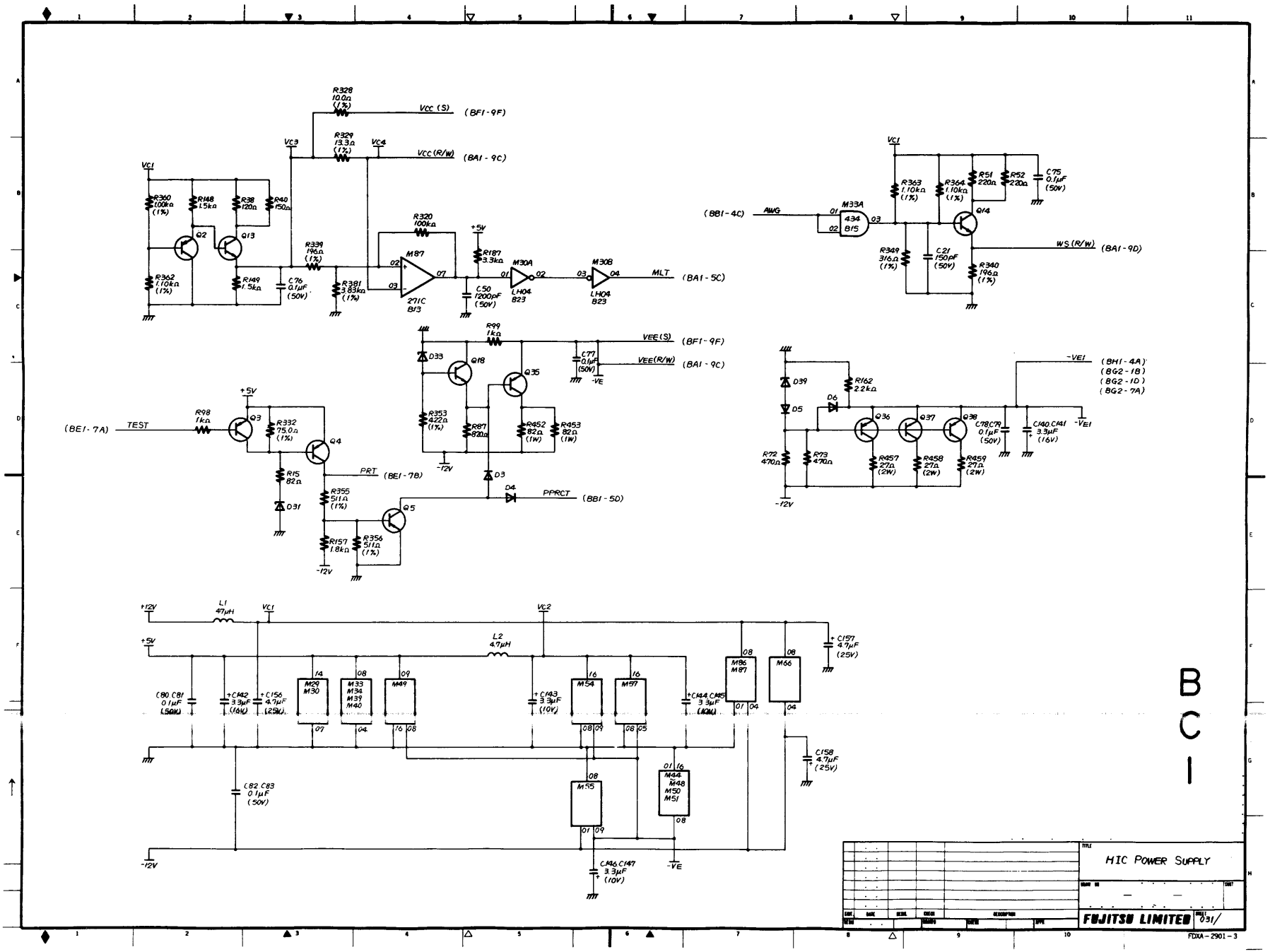
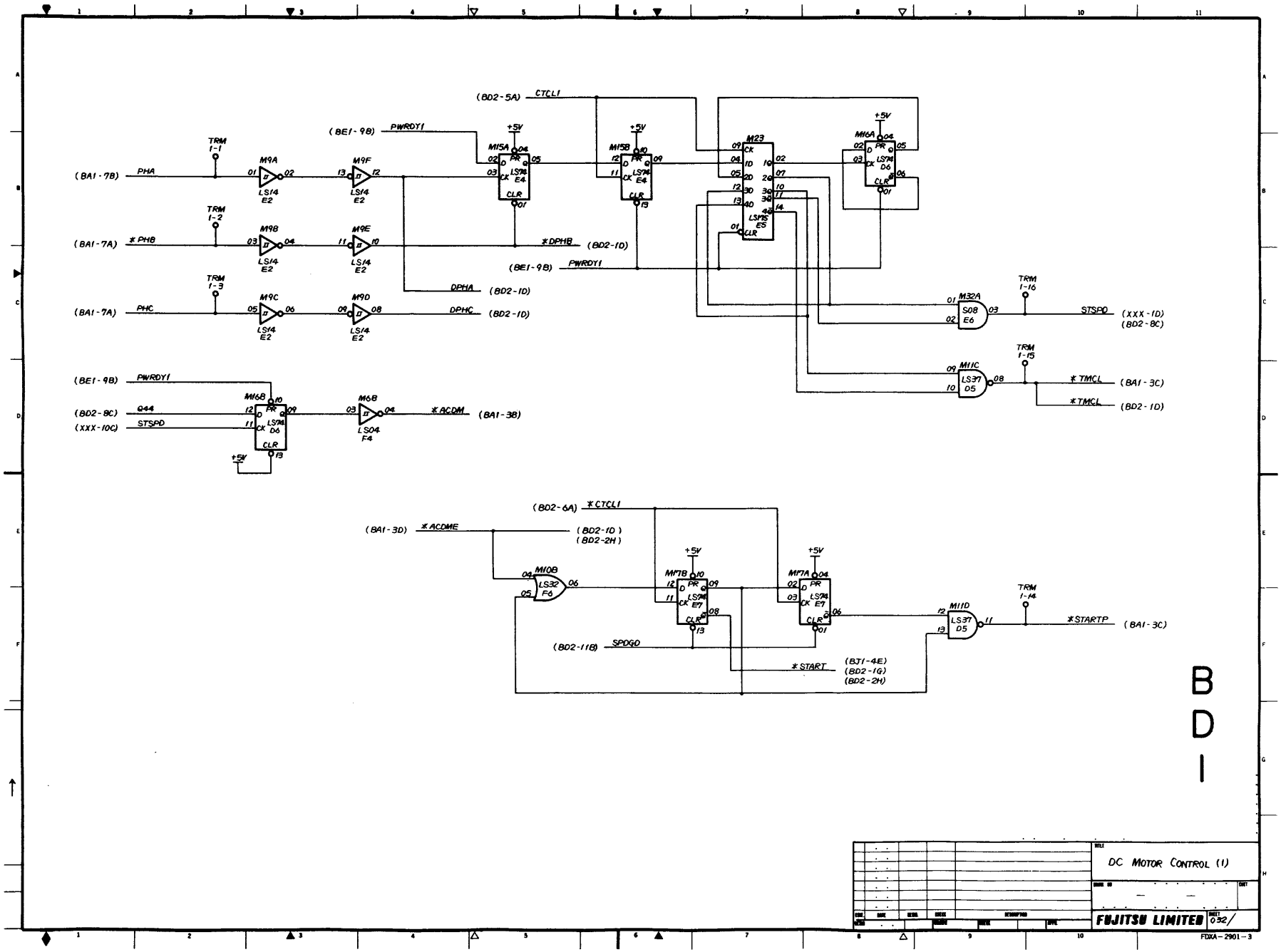

CN5
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
*DRLM (BJ1 - 1B)
FWD (BJ1 - 1C)
*ACOM (BD1 - 4D)
*RTZ (BJ1 - 1E)
*LNMO (BJ1 - 1A)
*PSDR (BJ1 - 1B)
*LSPD (BJ1 - 1E)
UNSQ (BJ1 - 7E)
TXPL (BJ1 - 11F)
*PWRDY (BE1 - 10C)
*SPDGD (BD2 - 11B)
*TMCL (BD1 - 10D)
*STARTP (BD1 - 10F)
ABORT (BK1 - 5F)
DMFL (BD2 - 4D)
+5V (xxx - 7D)
-12V (xxx - 7F)
*ACOME (BD1 - 4E)
OSCLK (BD2 - 5B)
*INX (BJ1 - 11B)
*OGB (BJ1 - 11D)
*IGB2 (BJ1 - 11D)
*IGB1 (BJ1 - 11D)
*FIGB1 (BJ1 - 11E)
BYTCL (BJ1 - 11A)
PLO1F (BF2 - 10C)
0V (xxx - 7F)
CN6
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
+RAWDT (BB2 - 11D)
-RAWDT (BB2 - 11D)
*HAR1 (BB1 - 8B)
*HAR2 (BB1 - 8B)
*HAR4 (BB1 - 1G)
*HAR8 (BB1 - 1H)
*WENB (BB1 - 1C)
N.C
*CY>256 (BB1 - 8D)
*WDTP (BB1 - 1B)
MLT (BC1 - 6C)
*USF (BB1 - 7F)
AMSH (BB2 - 1D)
D256 (BF2 - 1E)
D128 (BF2 - 1E)
D64 (BF2 - 1E)
D32 (BF2 - 1E)
DLT31 (BF2 - 6D)
D16 (BF2 - 1E)
D8 (BF2 - 1E)
D4 (BF2 - 1F)
D2 (BF2 - 1G)
D1 (BF2 - 1G)
*D>512 (BJ1 - 1D)
*CAR1 (BJ1 - 7F)
*CAR2 (BJ1 - 7G)
*BRLS (BK1 - 1D)
*OFACT (BJ1 - 1F)
*ONEND (BK1 - 4D)
VCMHT (BK1 - 11F)
EMRT (BE1 - 5C)
*HDLD (BG1 - 11B)
VH (BK1 - 1E)
ONTRK (BG1 - 6F)
V=0 (BG2 - 5G)
0V (xxx - 7F)
CN7
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
*PHB (BD1 - 1B)
PHC (BD1 - 1C)
PHA (BD1 - 1B)
C1 (BD2 - 7F)
C2 (BD2 - 7F)
A1 (BD2 - 7E)
A2 (BD2 - 7E)
B2 (BD2 - 7F)
B1 (BD2 - 7E)
CRLMT (BD2 - 7G)
*RLON (BE1 - 7C)
BRSNS (BK1 - 1F)
BRLY (BK1 - 4D)
PWDRBP (BK1 - 11C)
PWDRAP (BK1 - 11A)
PWDRBN (BK1 - 11B)
PWDRAN (BK1 - 11C)
CSNSB (BK1 - 5E)
CSNSA (BK1 - 5E)
0V (xxx - 7F)
CN8
01 02 03 04 05 06 07 08 09 10
+24V (xxx - 7E)
24RTN1 (xxx - 7E)
24RTN2 (xxx - 7E)
+5V (xxx - 7D)
0V (xxx - 7F)
+12V (BE1 - 3E)
CN9
01 02 03 04 05 06 07
+5V (xxx - 3C)(BE1 - 3G) (xxx - 9B)
24RTN1 (xxx - 9A)(BE1 - 3F)
24RTN2 (xxx - 9B)(BE1 - 3F)
+24V (xxx - 9A) (BE1 - 3F)
CN10
01 02 03 04 05 06 07
-12V (xxx - 3D) (BE1 - 3G)
0V (xxx - 3F) (xxx - 5F) (xxx - 7D) (xxx - 9B) (xxx - 9F) (BE1 - 3G)
CN15
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34
HS1(R/W) (BB1 - 11C)
VEE(R/W) (BC1 - 6D)
US(R/W) (BB1 - 1F)
VCC(R/W) (BC1 - 4B)
WC(R/W) (BB1 - 1D)
DX(R/W) (BB1 - 1E)
DY(R/W) (BB1 - 1E)
HS2(R/W) (BB1 - 11B)
CS0(R/W) (BB1 - 6G)
CS1(R/W) (BB1 - 6G)
WS(R/W) (BC1 - 10B)
CS2(R/W) (BB1 - 6H)
VEE(S) (BF1 - 11F)
DY(S) (BF1 - 1B)
HS2(S) (BF1 - 11E)
WC(S) N.C
DX(S) (BF1 - 1B)
VCC(S) (BF1 - 11F)
US(S) (BF1 - 11E)
HS1(S) (BF1 - 11E)
WS(S) (BF1 - 11D)
0V (xxx - 7F) (BF1 - 11F)
B
A
I
CONNECTION WITH CZFM PCA / TIXM AND TVQM PCA'S
FUJITSU LIMITED
FDXA-2901-3

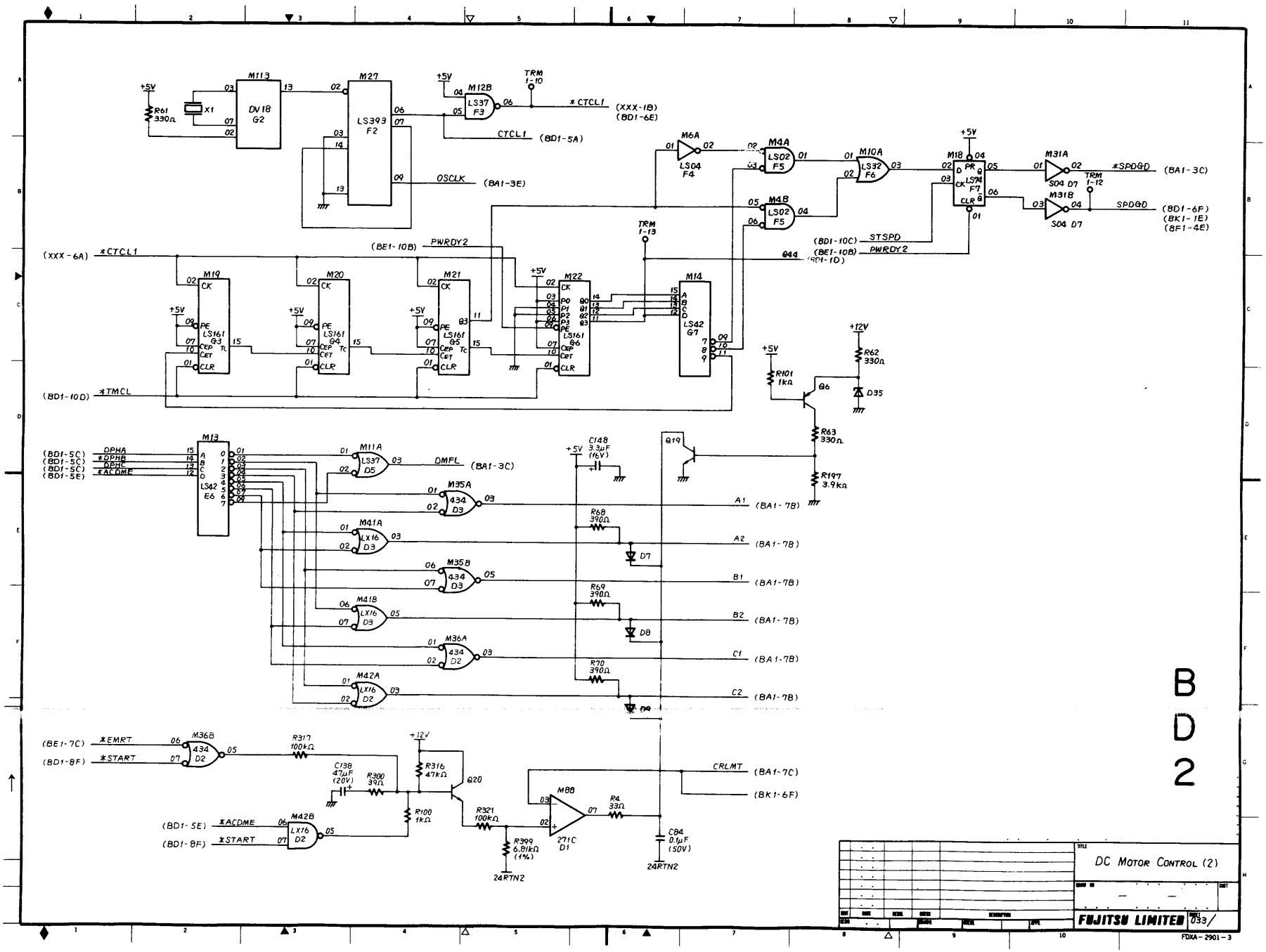

(BA1-5C) *WDTP
(BA1-5B) *WENB
(BA1-9C) WC(R/W)
(BA1-9C) DX(R/W)
(BA1-9D) DY(R/W)
(BA1-9C) US(R/W)
(BA1-5B) *HAR4
TRM 2-1
(BA1-5B) *HAR8
(xxx-9C) VHI
(BA1-5B) *HAR1
(BA1-5B) *HAR2
(BA1-5B) *CY>256
(BC1-5E) PPRCT
AWG (BC1-7B)
WG (BB2-3C)
*WENB (BB2-7C)
ASIG (BB2-1A)
*ASIG (BB2-1B)
*USF (BA1-5C)
HS2(R/W) (BA1-9D)
HS1(R/W) (BA1-9C)
CS0(R/W) (BA1-9D)
CS1(R/W) (BA1-9D)
CS2(R/W) (BA1-9D)
M55 43/6 A2
R/W BUS SWITCH / HEAD AND CHIP SELECTION
FUJITSU LIMITED
FDXA-2901-3

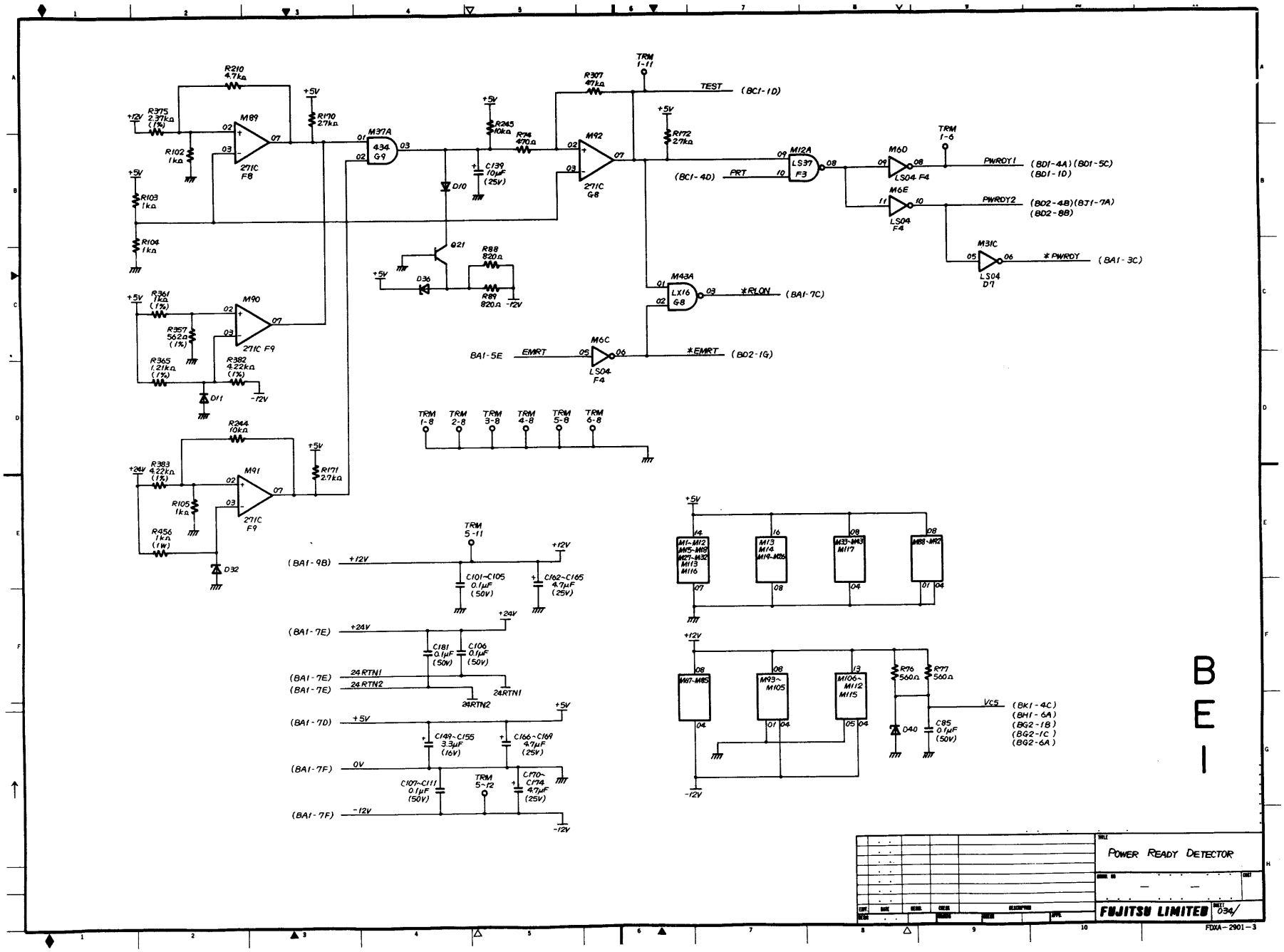
B
B
I

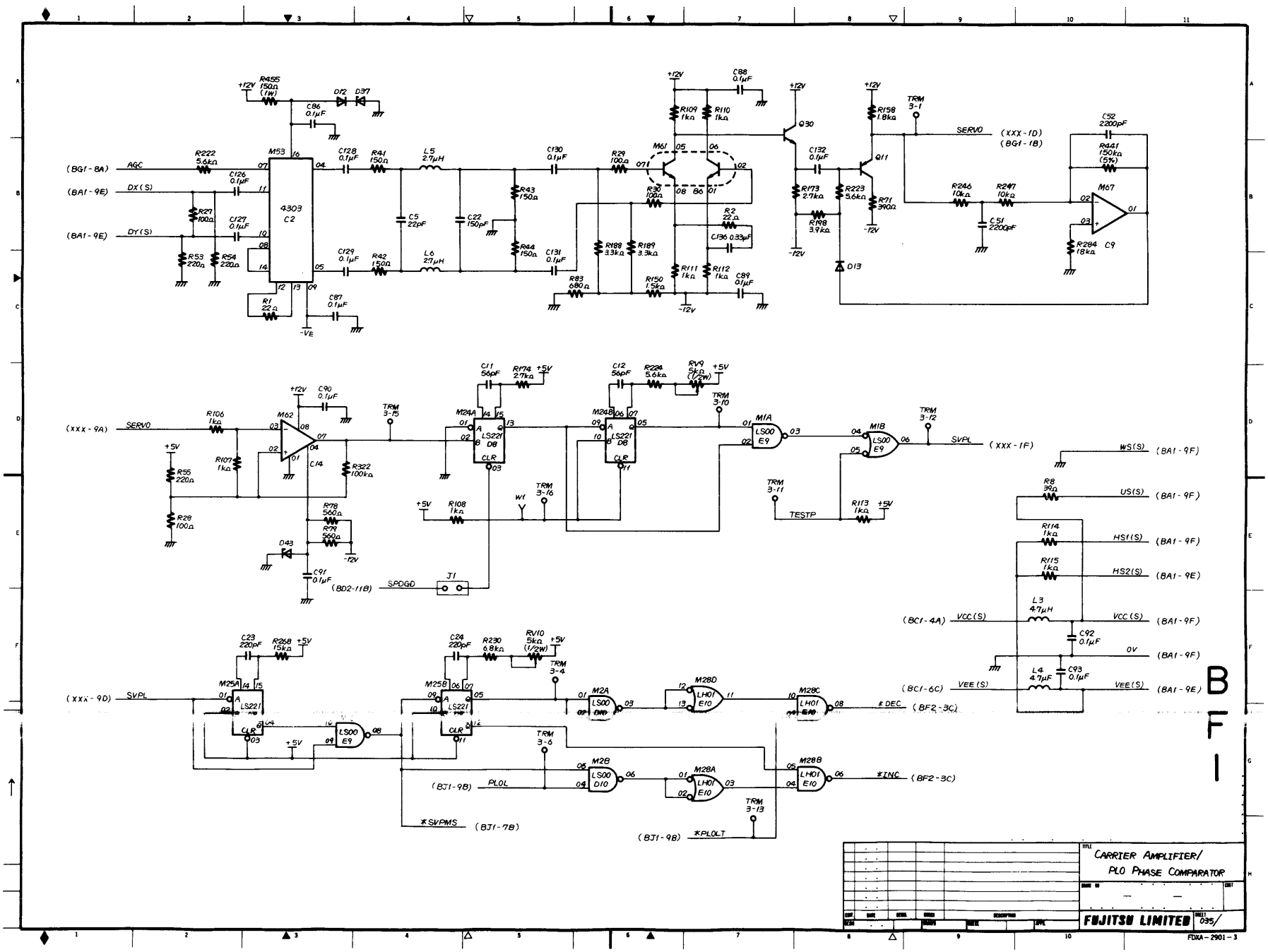

AGC AMPLIFIER / PULSE SHAPER
FUJITSU LIMITED
FDXA-2901-3
B B 2

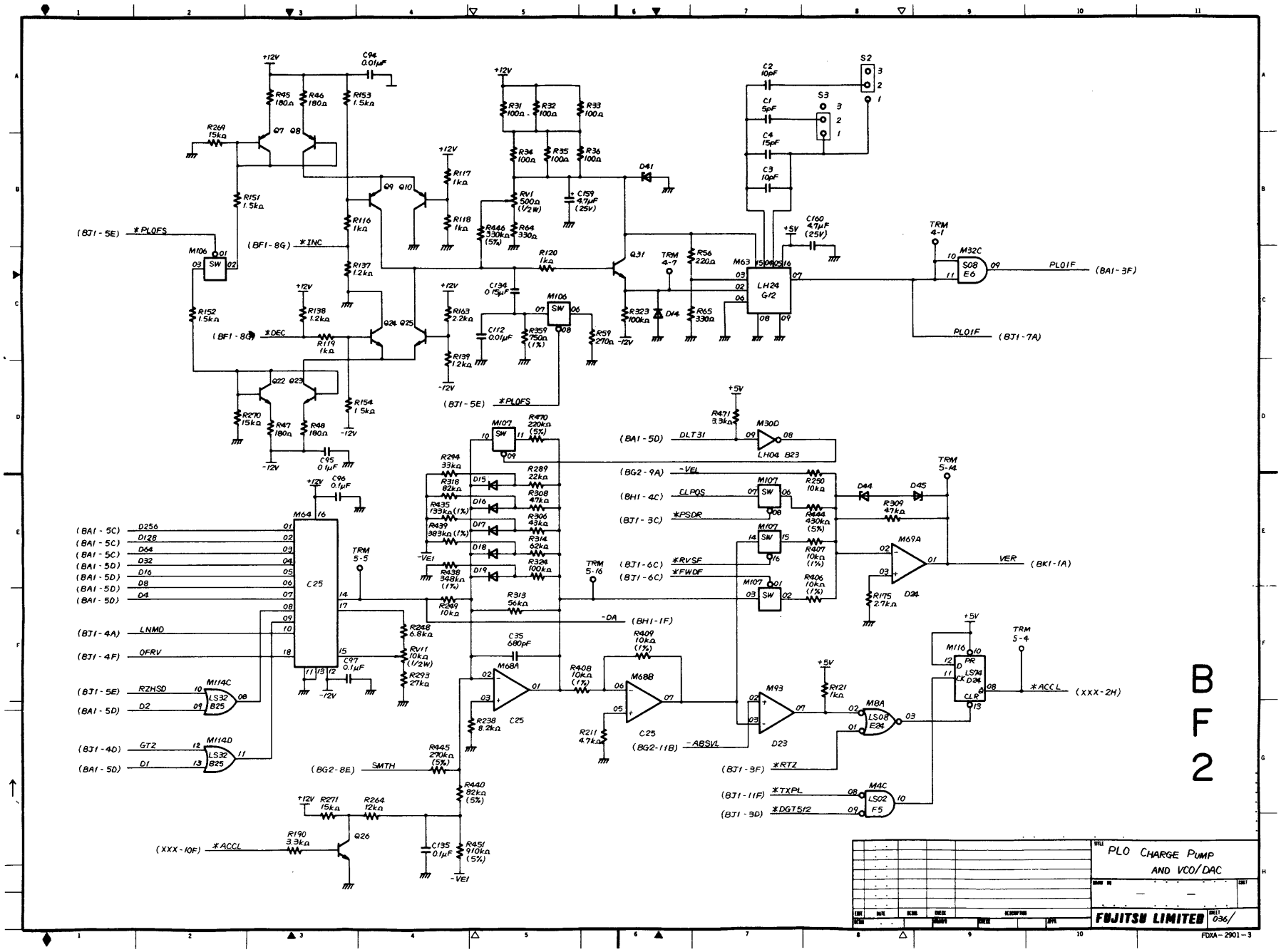

R328 10.0Ω (1%)
VCC (S)
(BF1-9F)
R329 13.3Ω (1%)
VCC(R/W)
(BA1-9C)
VC3
VC4
VC1
R360 100kΩ (1%)
R148 1.5kΩ
R38 120Ω
R40 150Ω
Q2
Q13
R362 1.10kΩ (1%)
R149 1.5kΩ
C76 0.1μF (50V)
R339 196Ω (1%)
R381 3.83kΩ (1%)
R320 100kΩ
M87
271C 8B3
+5V
R187 3.3kΩ
C50 1200pF (50V)
M30A
LH04 823
M30B
LH04 823
MLT
(BA1-5C)
R99 1kΩ
VEE(S)
(BF1-9F)
VEE(R/W)
(BA1-9C)
C77 0.1μF (50V)
-VE
D33
Q18
Q35
R353 422Ω (1%)
R87 820Ω
R452 82Ω (1W)
R453 82Ω (1W)
-12V
D3
D4
PPRCT
(BB1-5D)
+5V
(BE1-7A)
TEST
R98 1kΩ
Q3
R332 75.0Ω (1%)
Q4
PRT
(BE1-7B)
R15 82Ω
D31
R355 511Ω (1%)
Q5
R157 1.8kΩ
R356 511Ω (1%)
-12V
(BB1-4C)
AWG
M33A
434
8f5
VC1
R363 1.10kΩ (1%)
R364 1.10kΩ (1%)
R51 220Ω
R52 220Ω
C75 0.1μF (50V)
Q14
WS(R/W)
(BA1-9D)
R349 316Ω (1%)
C21 150pF (50V)
R340 196Ω (1%)
-VE1
(BH1-4A)
(BG2-1B)
(BG2-1D)
(BG2-7A)
D39
R162 2.2kΩ
D6
D5
Q36
Q37
Q38
C78,C79 0.1μF (50V)
C140,C141 3.3μF (16V)
R72 470Ω
R73 470Ω
R457 27Ω (2W)
R458 27Ω (2W)
R459 27Ω (2W)
-12V
+12V
L1 47μH
VC1
VC2
+5V
L2 4.7μH
+C157 4.7μF (25V)
C80,C81 0.1μF (50V)
+C142 3.3μF (16V)
+C156 4.7μF (25V)
M29 M30
M33 M34 M39 M40
M49
+C143 3.3μF (10V)
M54
M57
+C144,C145 3.3μF (10V)
M86 M87
M66
C82,C83 0.1μF (50V)
M55
M44 M48 M50 M51
C158 4.7μF (25V)
C146,C147 3.3μF (10V)
-12V
-VE
B
C
I
HIC POWER SUPPLY
FUJITSU LIMITED
FDXA-2901-3

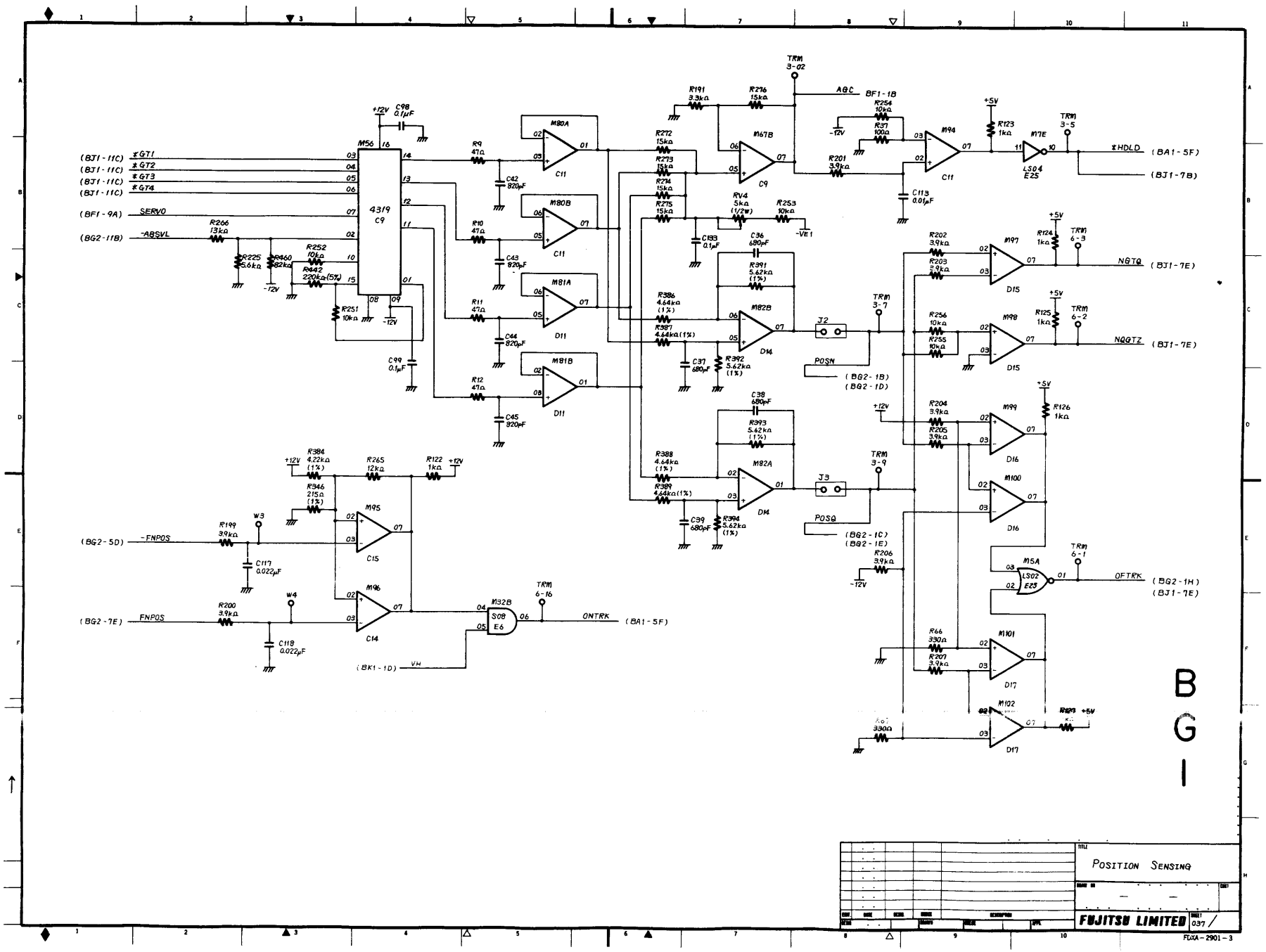

(BD2-5A) CTCL1
(BE1-9B) PWRDY1
(BA1-7B) PHA
(BA1-7A) *PHB
(BA1-7A) PHC
DPHA (BD2-1D)
*DPHB (BD2-1D)
DPHC (BD2-1D)
(BE1-9B) PWRDY1
(BD2-8C) Q44
(XXX-10C) STSPD
*ACDM (BA1-3B)
STSPD (XXX-1D) (BD2-8C)
*TMCL (BA1-3C)
*TMCL (BD2-1D)
(BD2-6A) *CTCL1
(BA1-3D) *ACDME (BD2-1D) (BD2-2H)
(BD2-11B) SPDGO
*START (BJ1-4E) (BD2-1G) (BD2-2H)
*STARTP (BA1-3C)
B D I
DC MOTOR CONTROL (1)
FUJITSU LIMITED
FDXA-2901-3

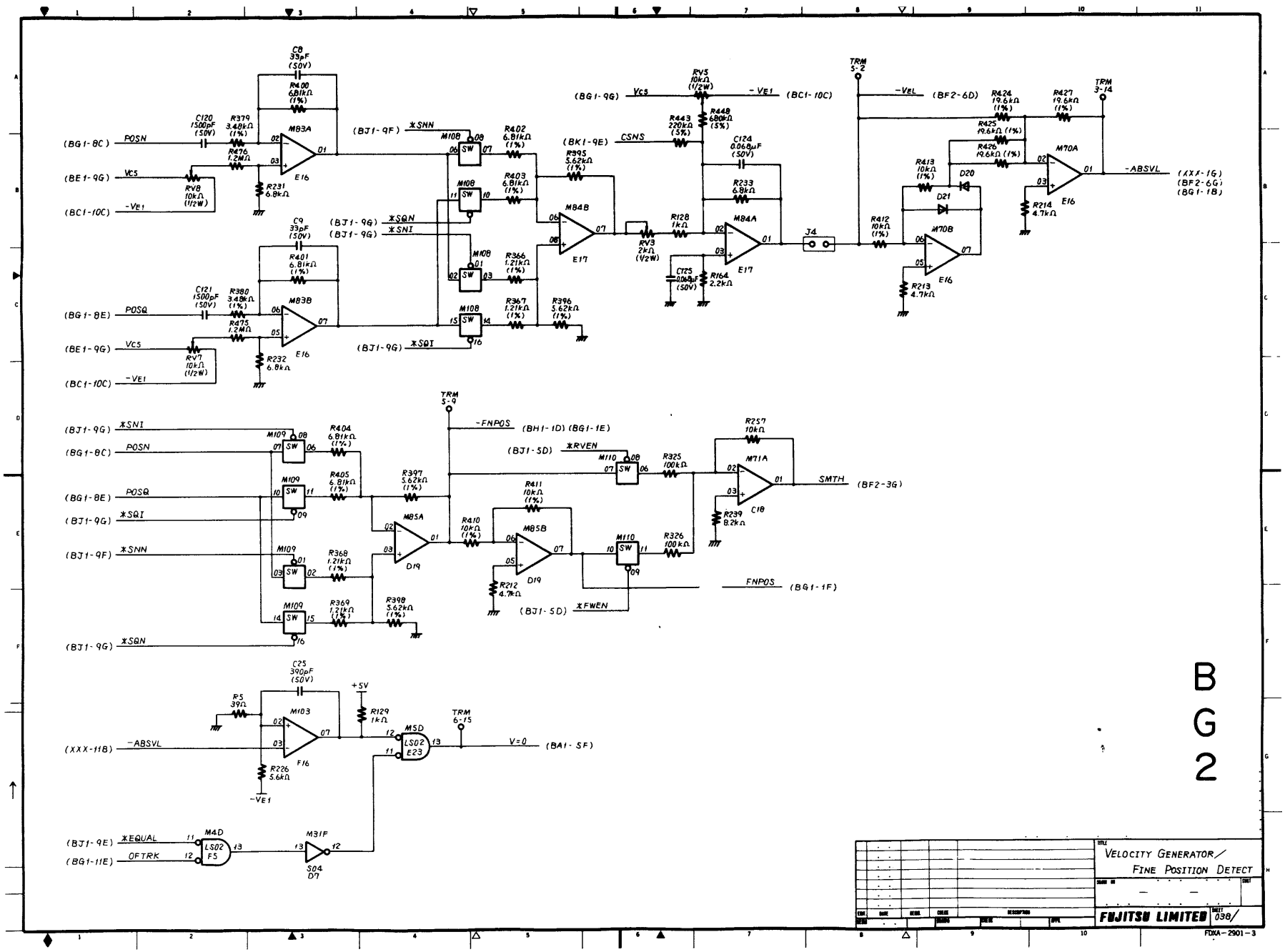

B D 2
DC MOTOR CONTROL (2)
FUJITSU LIMITED
FDXA-2901-3
M113
DV18 G2
M27
LS393 F2
M12B
LS37 F3
M6A
LS04 F4
M4A
LS02 F5
M4B
LS02 F5
M10A
LS32 F6
M18
LS74 F7
M31A
S04 D7
M31B
S04 D7
M19
LS161 G3
M20
LS161 G4
M21
LS161 G5
M22
LS161 G6
M14
LS42 G7
M13
LS42 E6
M11A
LS37 D5
M35A
434 D3
M41A
LX16 D3
M35B
434 D3
M41B
LX16 D3
M36A
434 D2
M42A
LX16 D2
M36B
434 D2
M42B
LX16 D2
M88
271C D1
Q6
Q19
Q20
R61 330Ω
X1
R101 1kΩ
R62 330Ω
R63 330Ω
R197 3.9kΩ
R68 390Ω
R69 390Ω
R70 390Ω
R317 100kΩ
R316 47kΩ
R300 39Ω
R100 1kΩ
R321 100kΩ
R399 6.81kΩ (1%)
R4 33Ω
C148 3.3μF (16V)
C138 47μF (20V)
C84 0.1μF (50V)
D7
D8
D9
D35
+5V
+12V
24RTN2
TRM 1-10
TRM 1-12
TRM 1-13
*CTCL1 (XXX-18) (BD1-6E)
CTCL1 (BD1-5A)
OSCLK (BA1-3E)
*SPDGD (BA1-3C)
SPDGD (BD1-6F) (BK1-1E) (8F1-4E)
STSPD (BD1-10C)
PWRDY2 (BE1-10B) (8F1-10D)
*CTCL1 (XXX-6A)
*TMCL (BD1-10D)
DPHA (BD1-5C)
*DPHB (BD1-5C)
DPHC (BD1-5C)
*ACDME (BD1-5E)
DMFL (BA1-3C)
A1 (BA1-7B)
A2 (BA1-7B)
B1 (BA1-7B)
B2 (BA1-7B)
C1 (BA1-7B)
C2 (BA1-7B)
*EMRT (BE1-7C)
*START (BD1-8F)
CRLMT (BA1-7C) (BK1-6F)

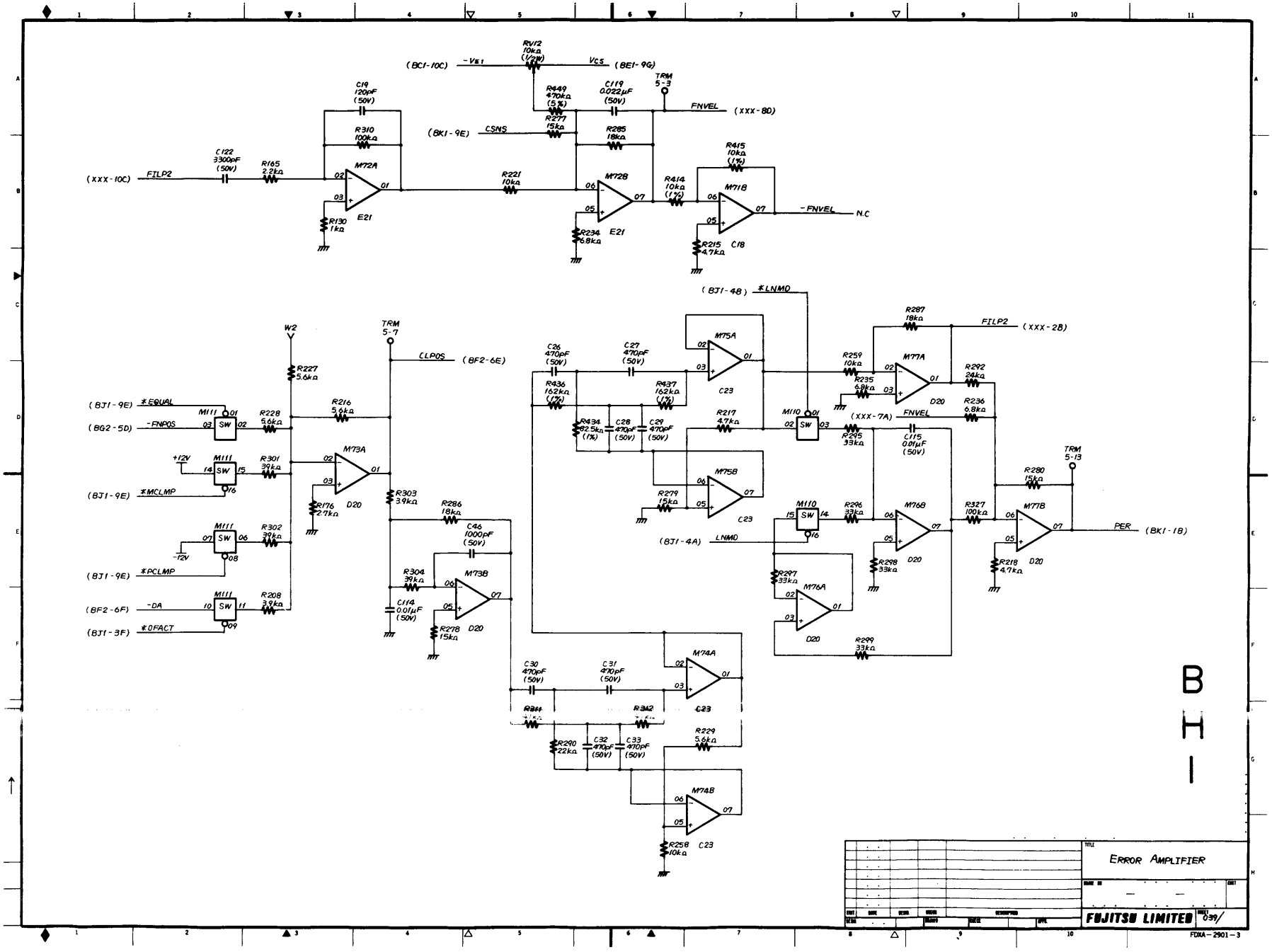

R210 4.7kΩ
R375 2.37kΩ (1%)
R102 1kΩ
R103 1kΩ
R104 1kΩ
M89
271C F8
R170 2.7kΩ
M37A 434 G9
R245 10kΩ
C139 10μF (25V)
D10
R74 470Ω
R307 47kΩ
TRM 1-11
TEST (BC1-1D)
M92
271C G8
R172 2.7kΩ
(BC1-4D) PRT
M12A LS37 F3
M6D LS04 F4
TRM 1-5
PWRDY1 (BD1-4A)(BD1-5C) (BD1-1D)
M6E LS04 F4
PWRDY2 (BD2-4B)(BJ1-7A) (BD2-8B)
M31C LS04 D7
*PWRDY (BA1-3C)
Q21
R88 820Ω
D36
R89 820Ω -12V
M43A LX16 G8
*RLON (BA1-7C)
BA1-5E EMRT
M6C LS04 F4
*EMRT (BD2-1G)
R361 1kΩ (1%)
R357 562Ω (1%)
R365 1.21kΩ (1%)
R382 4.22kΩ (1%)
M90
271C F9
D11
R244 10kΩ
R383 4.22kΩ (1%)
R105 1kΩ
R456 1kΩ (1W)
M91
271C F9
R171 2.7kΩ
D32
TRM 1-8 TRM 2-8 TRM 3-8 TRM 4-8 TRM 5-8 TRM 6-8
TRM 5-11
(BA1-9B) +12V
C101~C105 0.1μF (50V)
C162~C165 4.7μF (25V)
(BA1-7E) +24V
C181 0.1μF (50V)
C106 0.1μF (50V)
24RTN1
24RTN2
(BA1-7D) +5V
C149~C155 3.3μF (16V)
C166~C169 4.7μF (25V)
(BA1-7F) 0V
C107~C111 0.1μF (50V)
TRM 5~12
C170~C174 4.7μF (25V)
-12V
M1~M12 M15~M19 M27~M32 M113 M116
M13 M14 M19~M26
M33~M43 M117
M88~M92
M67~M85
M93~M105
M106~M112 M115
R76 560Ω
R77 560Ω
VCS (BK1-4C) (BH1-5A) (BG2-1B) (BG2-1C) (BG2-6A)
C85 0.1μF (50V)
D40
B
E
I
POWER READY DETECTOR
FUJITSU LIMITED
034/
FDXA-2901-3

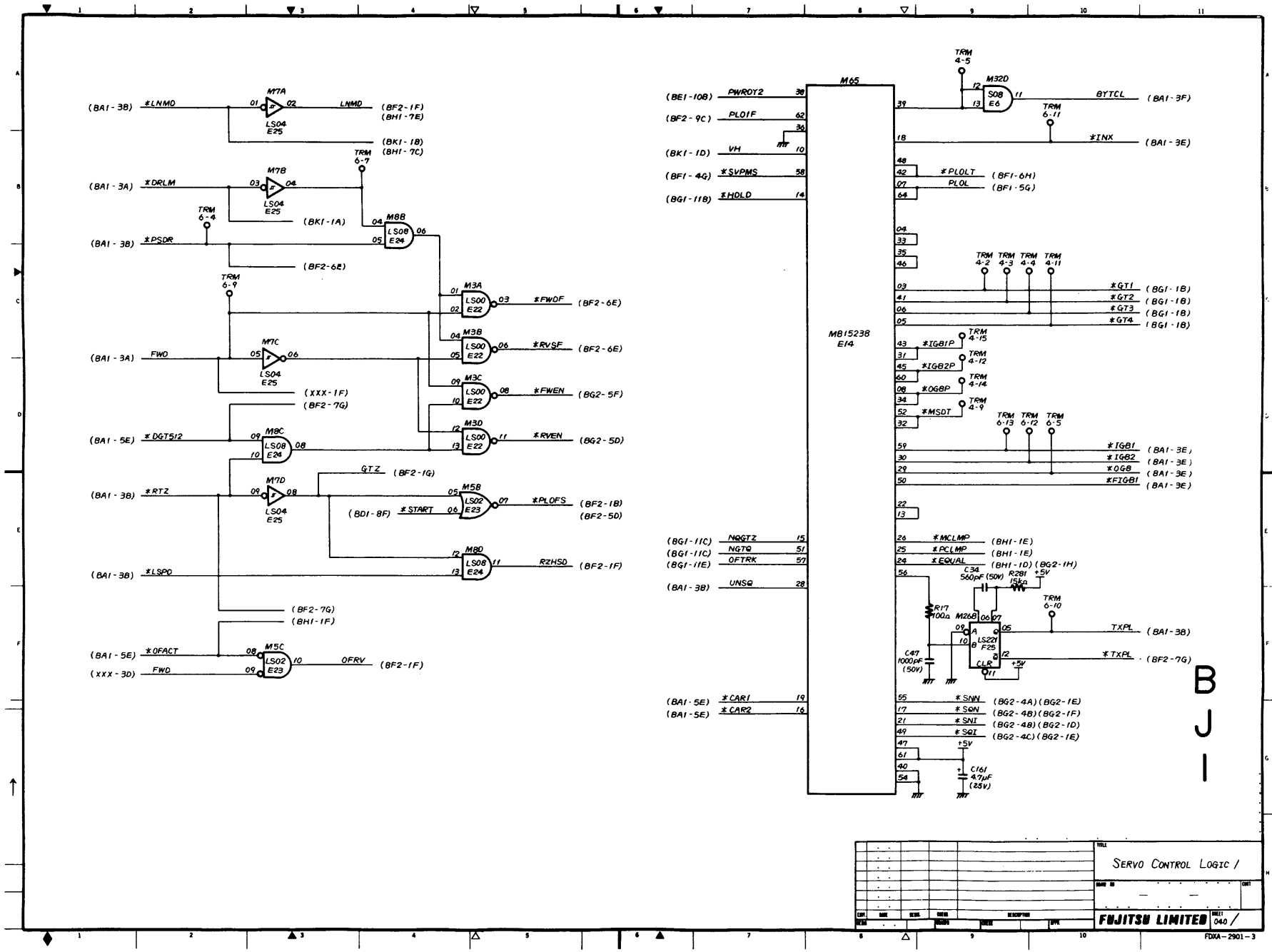

CARRIER AMPLIFIER/
PLO PHASE COMPARATOR
FUJITSU LIMITED
FDXA-2901-3
B
F
I

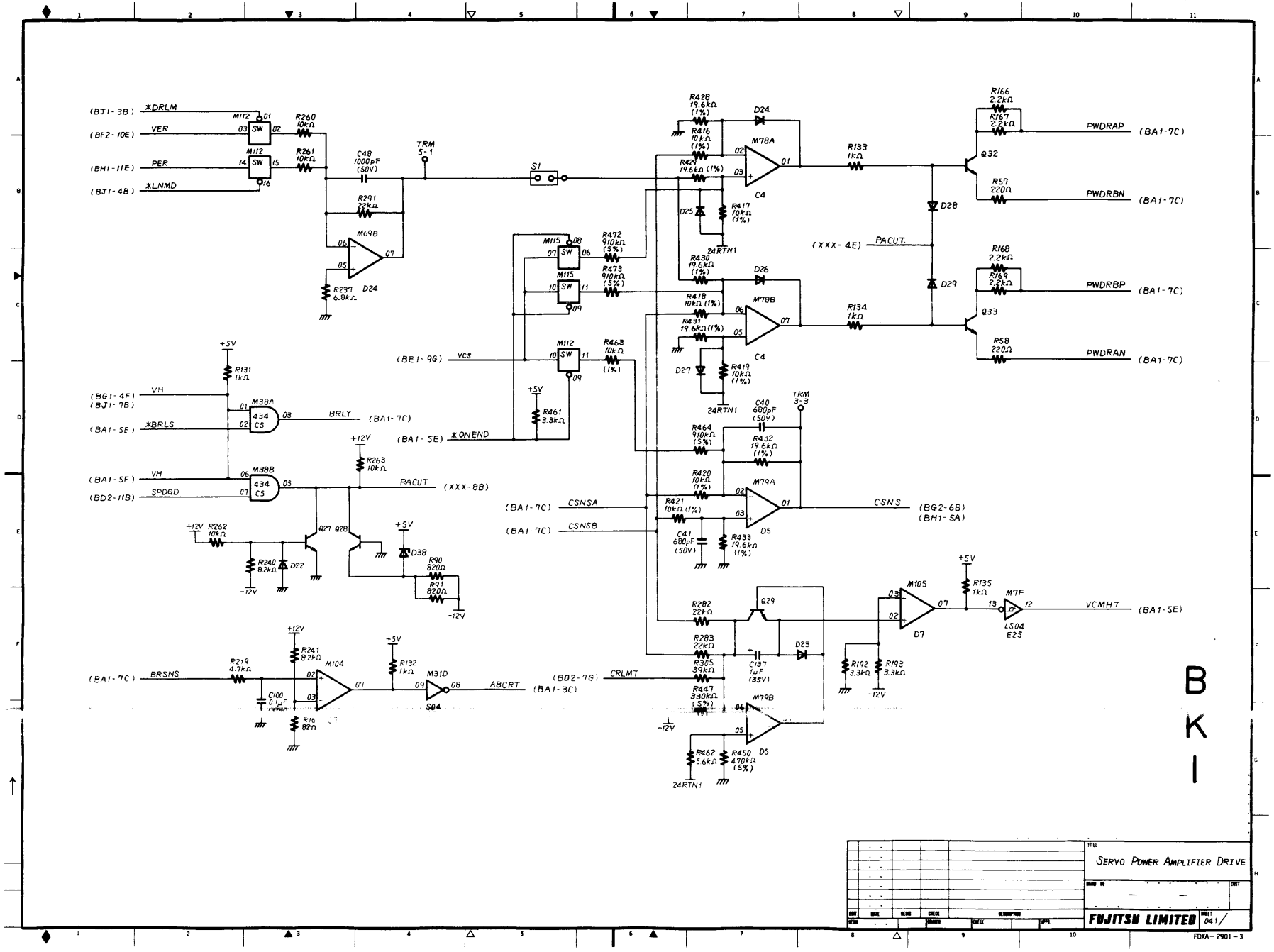

PLO CHARGE PUMP AND VCO/DAC
FUJITSU LIMITED
B F 2

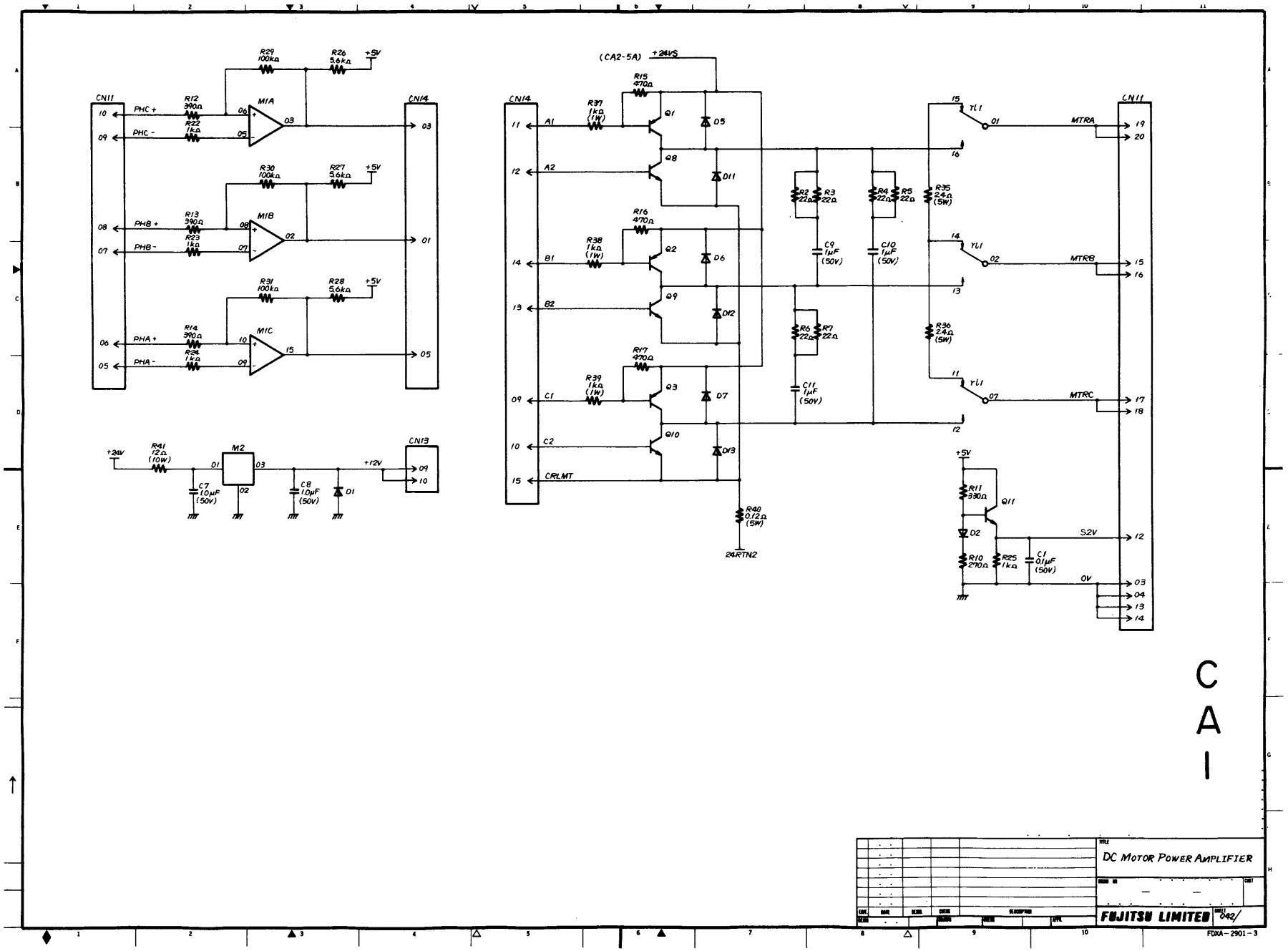

(BJ1-11C) *GT1
(BJ1-11C) *GT2
(BJ1-11C) *GT3
(BJ1-11C) *GT4
(BF1-9A) SERVO
(BG2-11B) -ABSVL
M56
4319
C9
+12V C98 0.1μF
R9 47Ω
R10 47Ω
R11 47Ω
R12 47Ω
C42 820pF
C43 820pF
C44 820pF
C45 820pF
M80A
M80B
M81A
M81B
C11
D11
R266 13kΩ
R225 5.6kΩ
R460 82kΩ
R252 10kΩ
R442 220kΩ(5%)
R251 10kΩ
C99 0.1μF
R191 3.3kΩ
R276 15kΩ
R272 15kΩ
R273 15kΩ
R274 15kΩ
R275 15kΩ
C133 0.1μF
RV4 5kΩ (1/2W)
R253 10kΩ
-VE1
M67B
C9
TRM 3-02
AGC
BF1-1B
R254 10kΩ
R37 100Ω
R201 3.9kΩ
C113 0.01μF
M94
C11
+5V
R123 1kΩ
M17E
LS04 E25
TRM 3-5
*HDLD
(BA1-5F)
(BJ1-7B)
C36 680pF
R391 5.62kΩ (1%)
R386 4.64kΩ (1%)
R387 4.64kΩ(1%)
C37 680pF
R392 5.62kΩ (1%)
M82B
D14
J2
POSN
(BG2-1B)
(BG2-1D)
TRM 3-7
C38 680pF
R393 5.62kΩ (1%)
R388 4.64kΩ (1%)
R389 4.64kΩ(1%)
C39 680pF
R394 5.62kΩ (1%)
M82A
D14
J3
POSQ
(BG2-1C)
(BG2-1E)
TRM 3-9
R202 3.9kΩ
R203 3.9kΩ
M97
D15
R124 1kΩ
TRM 6-3
NGTQ
(BJ1-7E)
R256 10kΩ
R255 10kΩ
M98
D15
R125 1kΩ
TRM 6-2
NQGTZ
(BJ1-7E)
R204 3.9kΩ
R205 3.9kΩ
M99
D16
R126 1kΩ
M100
D16
R206 3.9kΩ
M15A
LS02 E23
TRM 6-1
OFTRK
(BG2-1H)
(BJ1-7E)
R66 330Ω
R207 3.9kΩ
M101
D17
M102
D17
330Ω
+5V
R384 4.22kΩ (1%)
R265 12kΩ
R122 1kΩ
R346 215Ω (1%)
M95
C15
R199 3.9kΩ
W3
(BG2-5D) -FNPOS
C117 0.022μF
M96
C14
R200 3.9kΩ
W4
(BG2-7E) FNPOS
C118 0.022μF
M132B
S08 E6
TRM 6-16
ONTRK
(BA1-5F)
(BK1-1D) VH
B
G
I
TRM
Position Sensing
FUJITSU LIMITED
037
FLXA-2901-3


B G 2
VELOCITY GENERATOR/ FINE POSITION DETECT
FUJITSU LIMITED
FDXA-2901-3
(BG1-8C) POSN
(BE1-9G) VCS
(BC1-10C) -VE1
(BG1-8E) POSQ
(BJ1-9F) *SNN
(BJ1-9G) *SNI
(BJ1-9G) *SQN
(BJ1-9G) *SQI
(BK1-9E) CSNS
(BG1-9G) VCS
(BC1-10C) -VE1
(BF2-6D) -VEL
(XXX-16) (BF2-6G) (BG1-1B) -ABSVL
(BH1-1D) (BG1-1E) -FNPOS
(BJ1-5D) *RVEN
(BF2-3G) SMTH
(BG1-1F) FNPOS
(BJ1-5D) *FWEN
(XXX-11B) -ABSVL
(BA1-5F) V=0
(BJ1-9E) *EQUAL
(BG1-11E) OFTRK
J4
TRM 5-2
TRM 3-14
TRM 5-9
TRM 6-15


ERROR AMPLIFIER
FUJITSU LIMITED
FDXA-2901-3
B
H
I


(BA1-3B) *LNMO
LNMD (BF2-1F) (BH1-7E)
(BK1-1B) (BH1-7C)
(BA1-3A) *DRLM
(BK1-1A)
(BA1-3B) *PSDR
(BF2-6E)
(BA1-3A) FWD
(XXX-1F)
(BF2-7G)
(BA1-5E) *DGTS12
(BA1-3B) *RTZ
GTZ (BF2-1G)
(BD1-8F) *START
*PLOFS (BF2-1B) (BF2-5D)
(BA1-3B) *LSPD
RZHSD (BF2-1F)
(BF2-7G)
(BH1-1F)
(BA1-5E) *OFACT
(XXX-3D) FWD
OFRV (BF2-1F)
*FWDF (BF2-6E)
*RVSF (BF2-6E)
*FWEN (BG2-5F)
*RVEN (BG2-5D)
(BE1-10B) PWROY2
(BF2-9C) PLOIF
(BK1-1D) VH
(BF1-4G) *SVPMS
(BG1-11B) *HOLD
(BG1-11C) NQGTZ
(BG1-11C) NGTQ
(BG1-11E) OFTRK
(BA1-3B) UNSQ
(BA1-5E) *CAR1
(BA1-5E) *CAR2
M8152 38 E14
BYTCL (BA1-3F)
*INX (BA1-3E)
*PLOLT (BF1-6H)
PLOL (BF1-5G)
*GT1 (BG1-1B)
*GT2 (BG1-1B)
*GT3 (BG1-1B)
*GT4 (BG1-1B)
*IGB1P
*IGB2P
*OGBP
*MSDT
*IGB1 (BA1-3E)
*IGB2 (BA1-3E)
*OGB (BA1-3E)
*FIGB1 (BA1-3E)
*MCLMP (BH1-1E)
*PCLMP (BH1-1E)
*EQVAL (BH1-1D) (BG2-1H)
C34 560pF (50V)
R281 15kΩ
+5V
R17 100Ω
C47 1000pF (50V)
TXPL (BA1-3B)
*TXPL (BF2-7G)
*SNN (BG2-4A) (BG2-1E)
*SQN (BG2-4B) (BG2-1F)
*SNI (BG2-4B) (BG2-1D)
*SQI (BG2-4C) (BG2-1E)
C161 4.7μF (25V)
B
J
I
SERVO CONTROL LOGIC /
FUJITSU LIMITED
FDXA-2901-3


(BJ1-3B) *DRLM
(BF2-10E) VER
(BH1-11E) PER
(BJ1-4B) *LNMD
M112
R260 10kΩ
R261 10kΩ
C48 1000pF (50V)
TRM 5-1
S1
R291 22kΩ
M69B
R297 6.8kΩ
D24
R428 19.6kΩ (1%)
R416 10kΩ (1%)
R429 19.6kΩ (1%)
M78A
C4
D25
R417 10kΩ (1%)
24RTN1
D24
R133 1kΩ
R166 2.2kΩ
R167 2.2kΩ
Q32
R57 220Ω
PWDRAP (BA1-7C)
PWDRBN (BA1-7C)
D28
(XXX-4E) PACUT
M115
R472 910kΩ (5%)
R473 910kΩ (5%)
R430 19.6kΩ (1%)
D26
R418 10kΩ (1%)
R431 19.6kΩ (1%)
M78B
C4
D27
R419 10kΩ (1%)
24RTN1
D29
R134 1kΩ
R168 2.2kΩ
R169 2.2kΩ
Q33
R58 220Ω
PWDRBP (BA1-7C)
PWDRAN (BA1-7C)
(BE1-9G) Vcs
M112
R463 10kΩ (1%)
+5V
R461 3.3kΩ
(BA1-5E) *ONEND
TRM 3-3
C40 680pF (50V)
R464 910kΩ (5%)
R432 19.6kΩ (1%)
R420 10kΩ (1%)
M79A
R421 10kΩ (1%)
C41 680pF (50V)
R433 19.6kΩ (1%)
D5
(BA1-7C) CSNSA
(BA1-7C) CSNSB
CSNS (BG2-6B) (BH1-5A)
+5V
R131 1kΩ
(BG1-4F) (BJ1-7B) VH
(BA1-5E) *BRLS
M38A
434 C5
BRLY (BA1-7C)
+12V
R263 10kΩ
(BA1-5F) VH
(BD2-11B) SPDGD
M38B
434 C5
PACUT (XXX-8B)
+12V R262 10kΩ
Q27 Q28
R240 8.2kΩ
D22
-12V
+5V
D38
R90 820Ω
R91 820Ω
-12V
R282 22kΩ
Q29
R283 22kΩ
R305 39kΩ
C137 1μF (35V)
D23
R447 330kΩ (5%)
M79B
R462 5.6kΩ
R450 470kΩ (5%)
D5
24RTN1
-12V
R192 3.3kΩ
R193 3.3kΩ
-12V
+5V
R135 1kΩ
M105
D7
M7F
LS04 E25
VCMHT (BA1-5E)
+12V
R241 8.2kΩ
R219 4.7kΩ
(BA1-7C) BRSNS
M104
C100 0.1μF
R15 82Ω
+5V
R132 1kΩ
M31D
S04
ABCRT (BA1-3C)
(BD2-7G) CRLMT
B
K
I
TITLE
SERVO POWER AMPLIFIER DRIVE
FUJITSU LIMITED
FDXA-2901-3

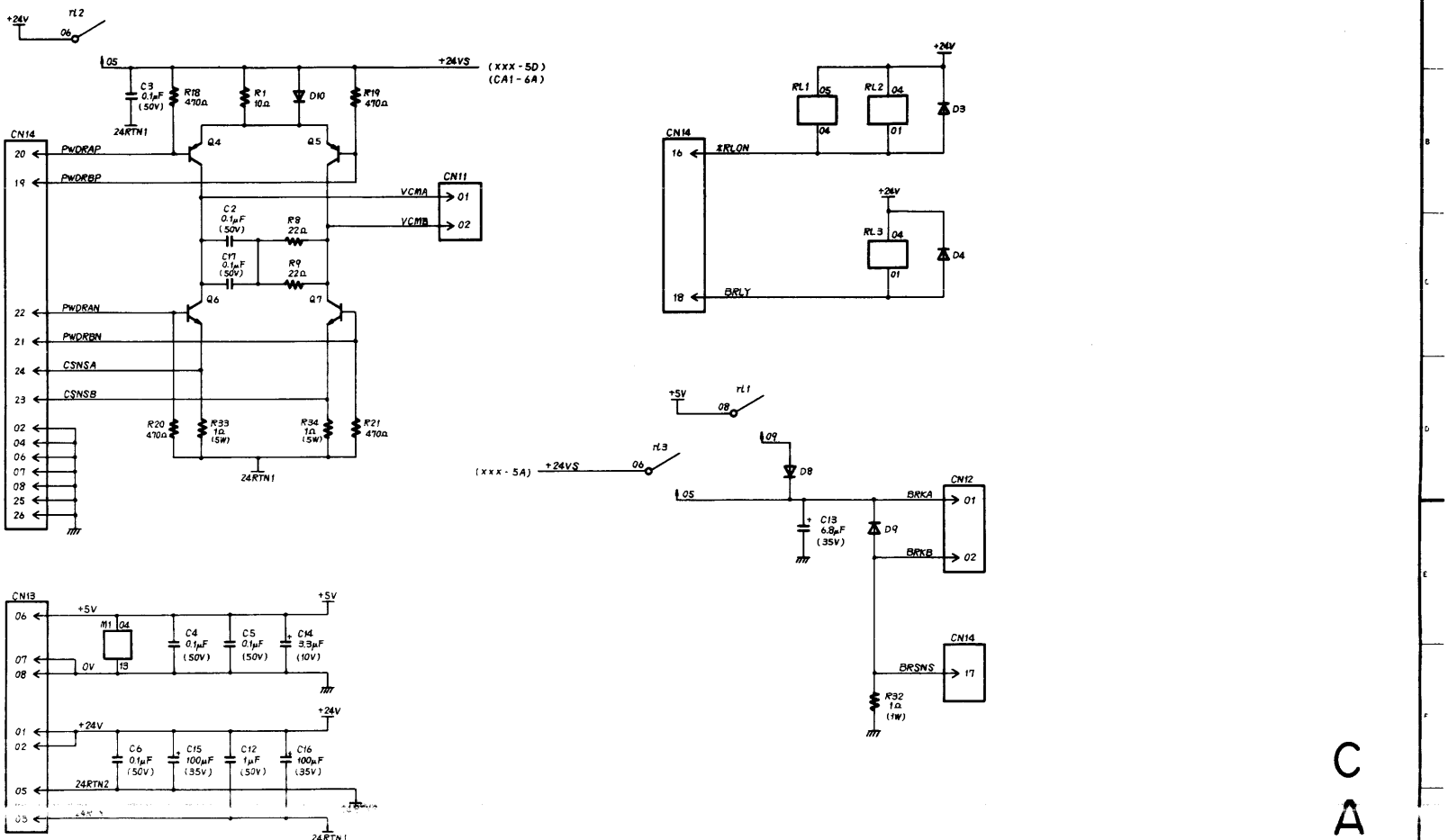


C
A
I

DC MOTOR POWER AMPLIFIER

FUJITSU LIMITED

FDXA-2901-3

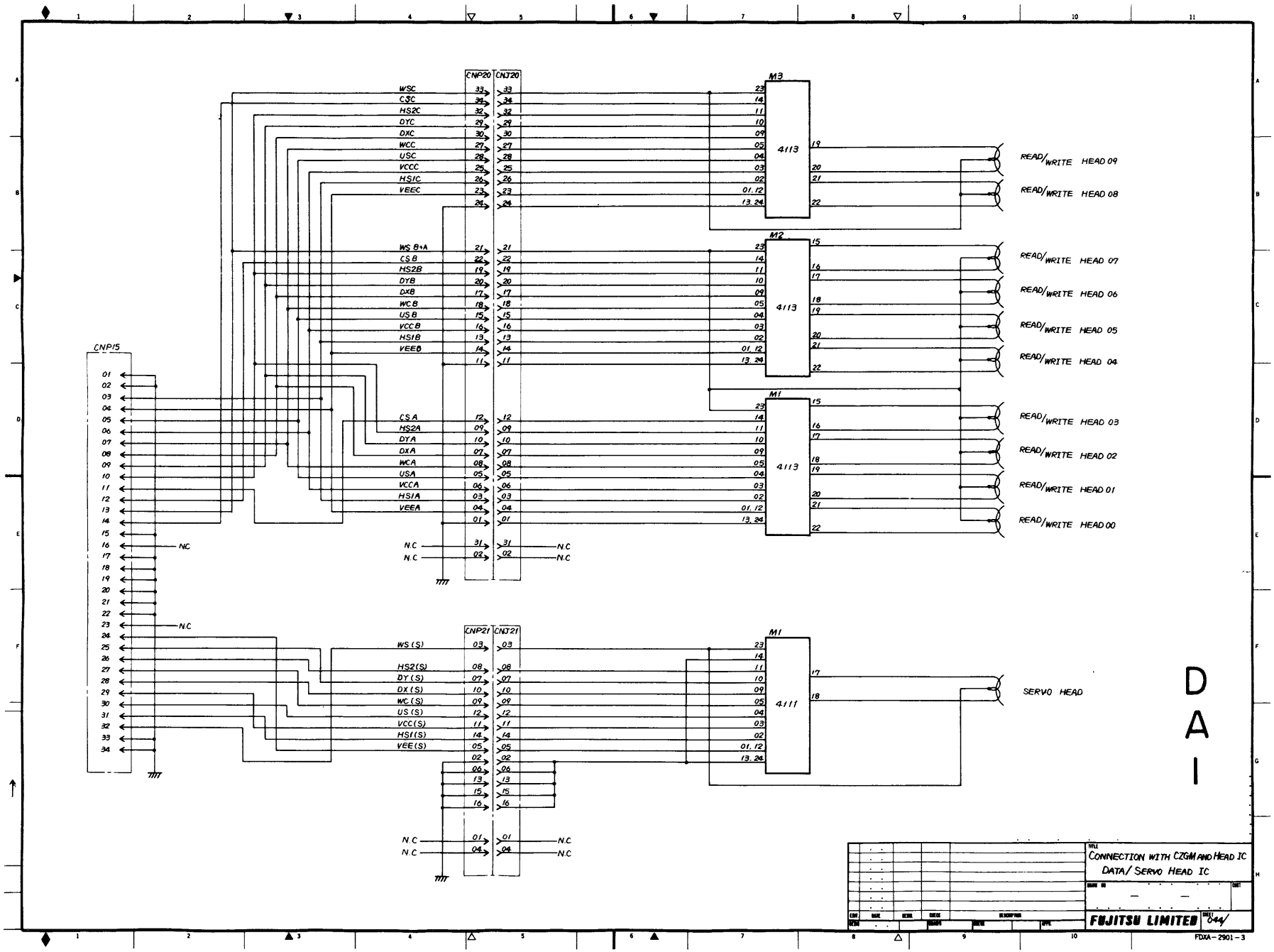


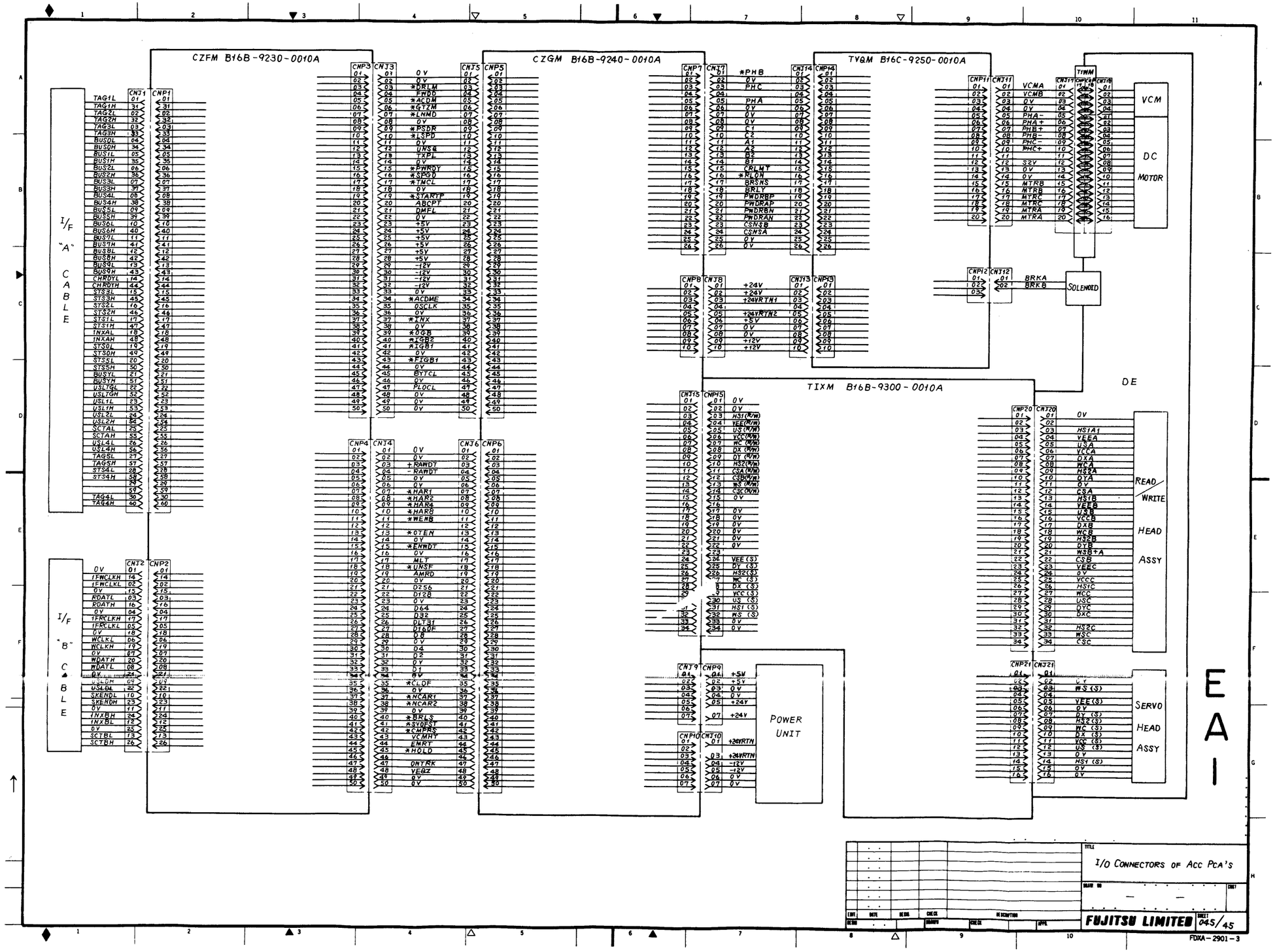
C
A
2

						TITLE	SERVO POWER AMPLIFIER
						SIZE —	DWG NO —
						FUJITSU LIMITED	SHEET 043

FDXA-2901-3

B03P-4740-0111A...02


CNP20
CNJ20
WSC
CSC
HS2C
DYC
DXC
WCC
USC
VCCC
HS1C
VEEC
WS B+A
CS B
HS2B
DYB
DXB
WCB
USB
VCCB
HS1B
VEEB
CS A
HS2A
DYA
DXA
WCA
USA
VCCA
HS1A
VEEA
N.C
M3
M2
M1
4113
READ/WRITE HEAD 09
READ/WRITE HEAD 08
READ/WRITE HEAD 07
READ/WRITE HEAD 06
READ/WRITE HEAD 05
READ/WRITE HEAD 04
READ/WRITE HEAD 03
READ/WRITE HEAD 02
READ/WRITE HEAD 01
READ/WRITE HEAD 00
CNP15
CNP21
CNJ21
WS(S)
HS2(S)
DY(S)
DX(S)
WC(S)
US(S)
VCC(S)
HS1(S)
VEE(S)
4111
SERVO HEAD
D
A
I
CONNECTION WITH CZGM AND HEAD IC
DATA/SERVO HEAD IC
FUJITSU LIMITED
FDXA-2901-3



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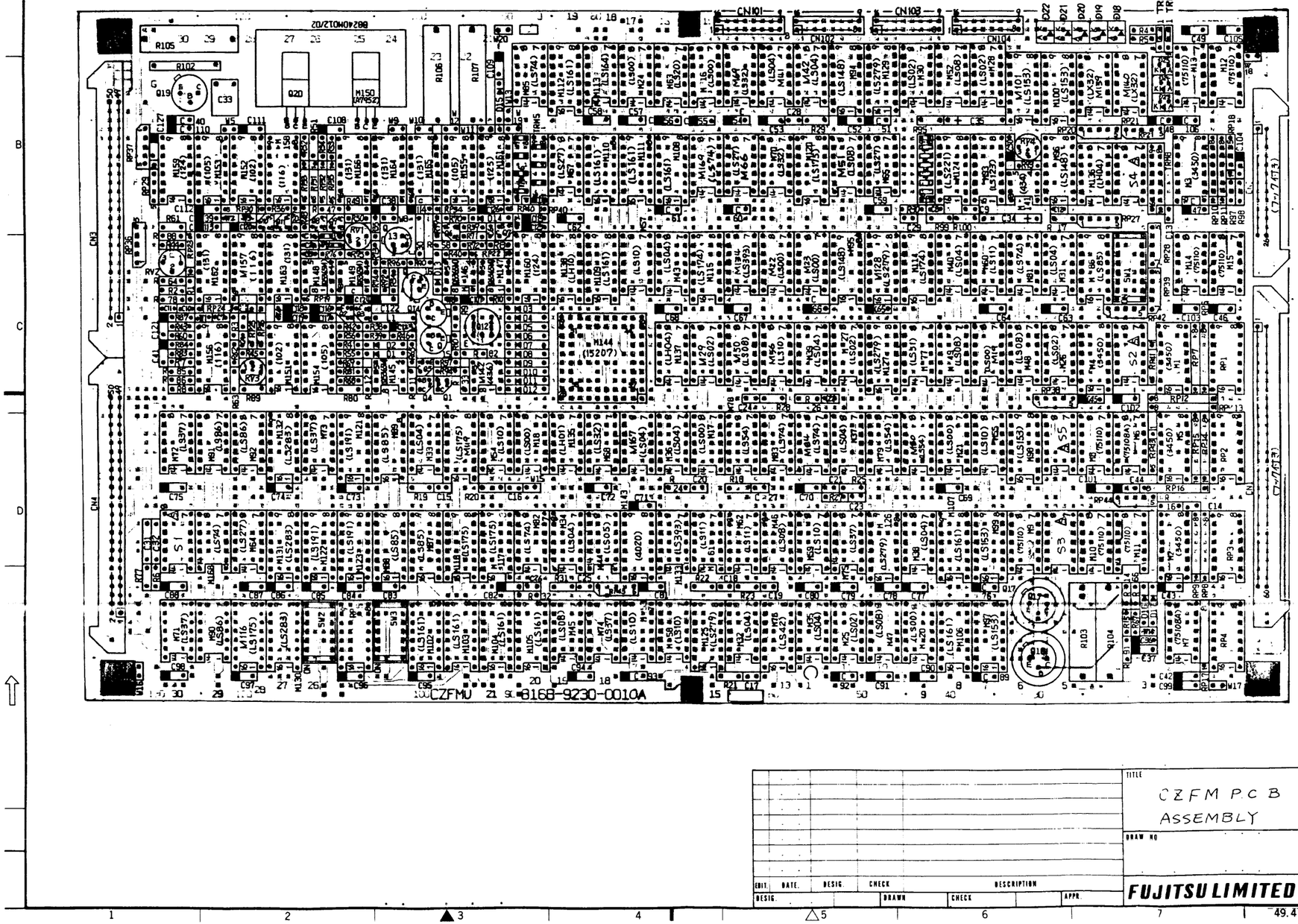
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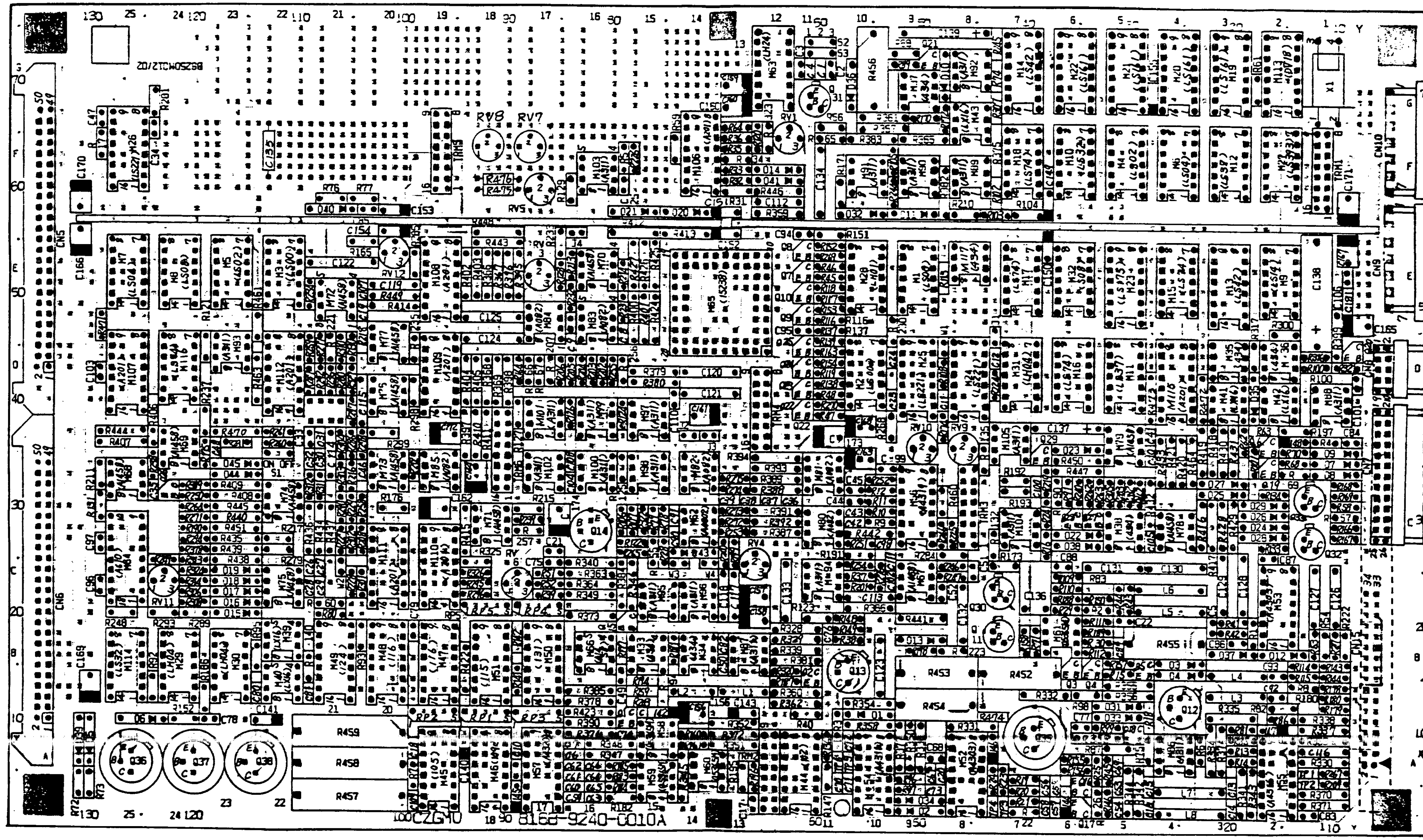
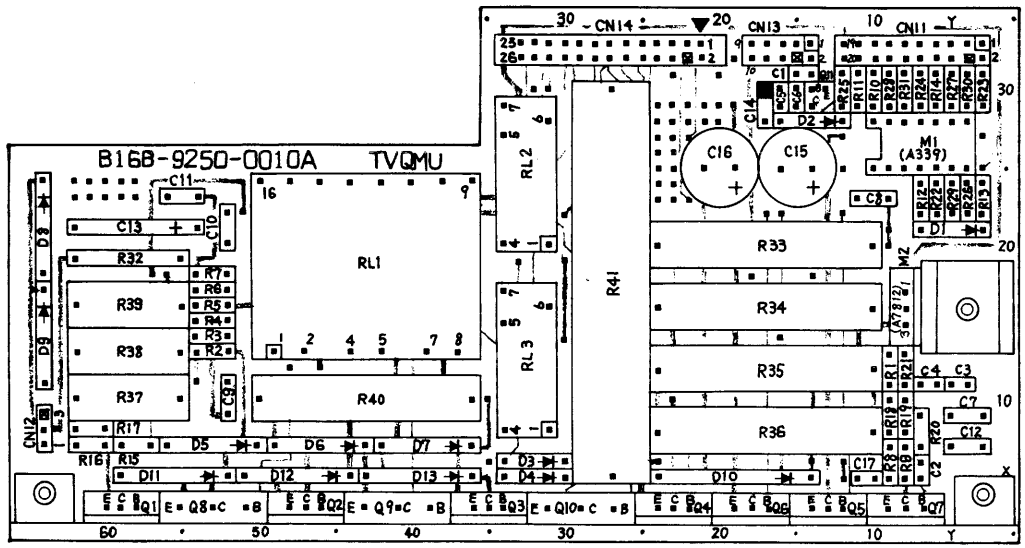
CZFM P.C.B
ASSEMBLY
DRAW NO
CUST.
FUJITSU LIMITED
SHEET 46/
49.4 FDXA-3001-3



CZGM P.C.B
ASSEMBLY

FUJITSU LIMITED 47/

FDXA-2901-3



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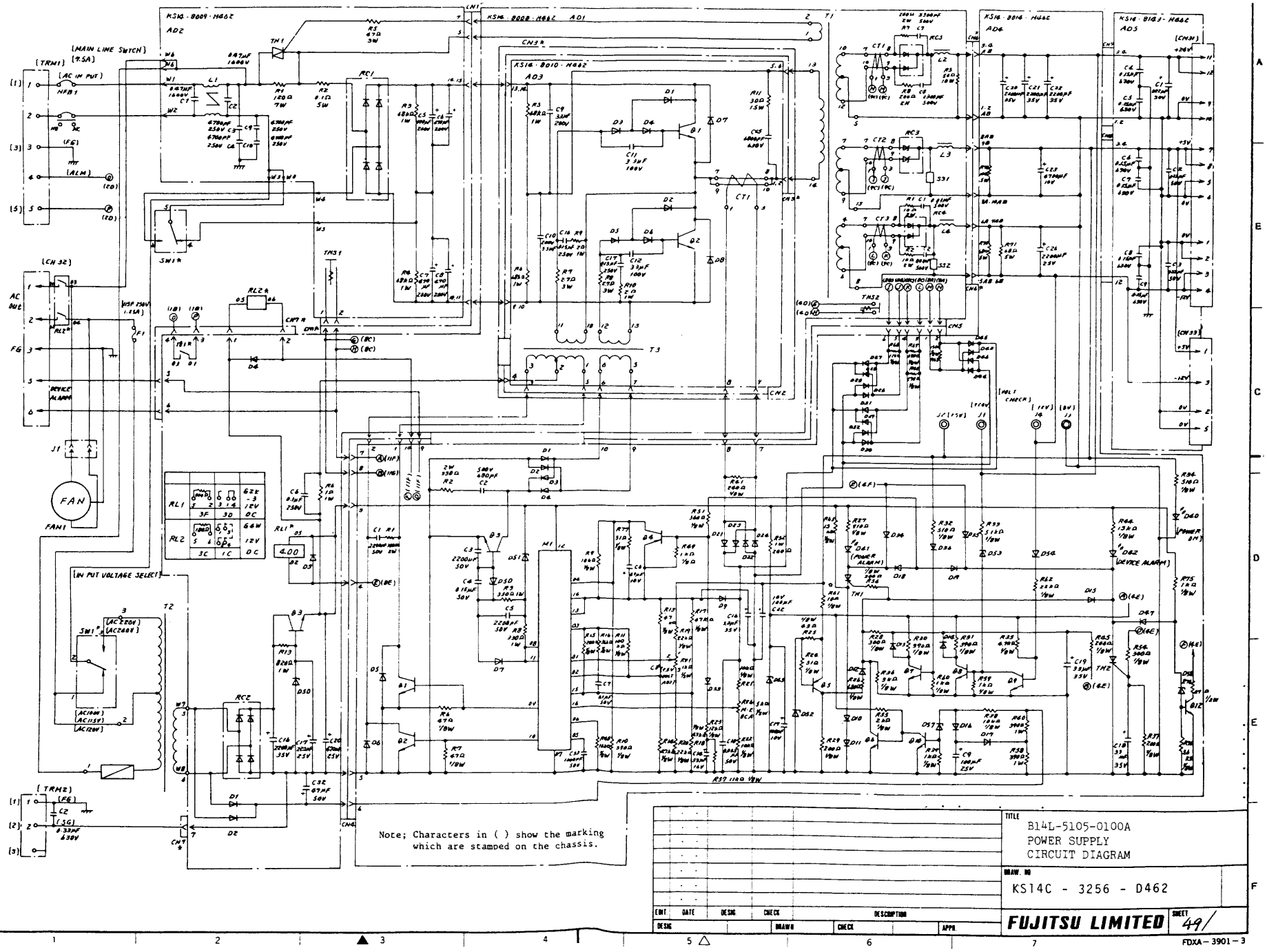
DESN			DRAWN	CHCK	APPR	

494 FDXA 3001 3

B03P-4740-0111A...02C



TITLE
B14L-5105-0100A
POWER SUPPLY
CIRCUIT DIAGRAM

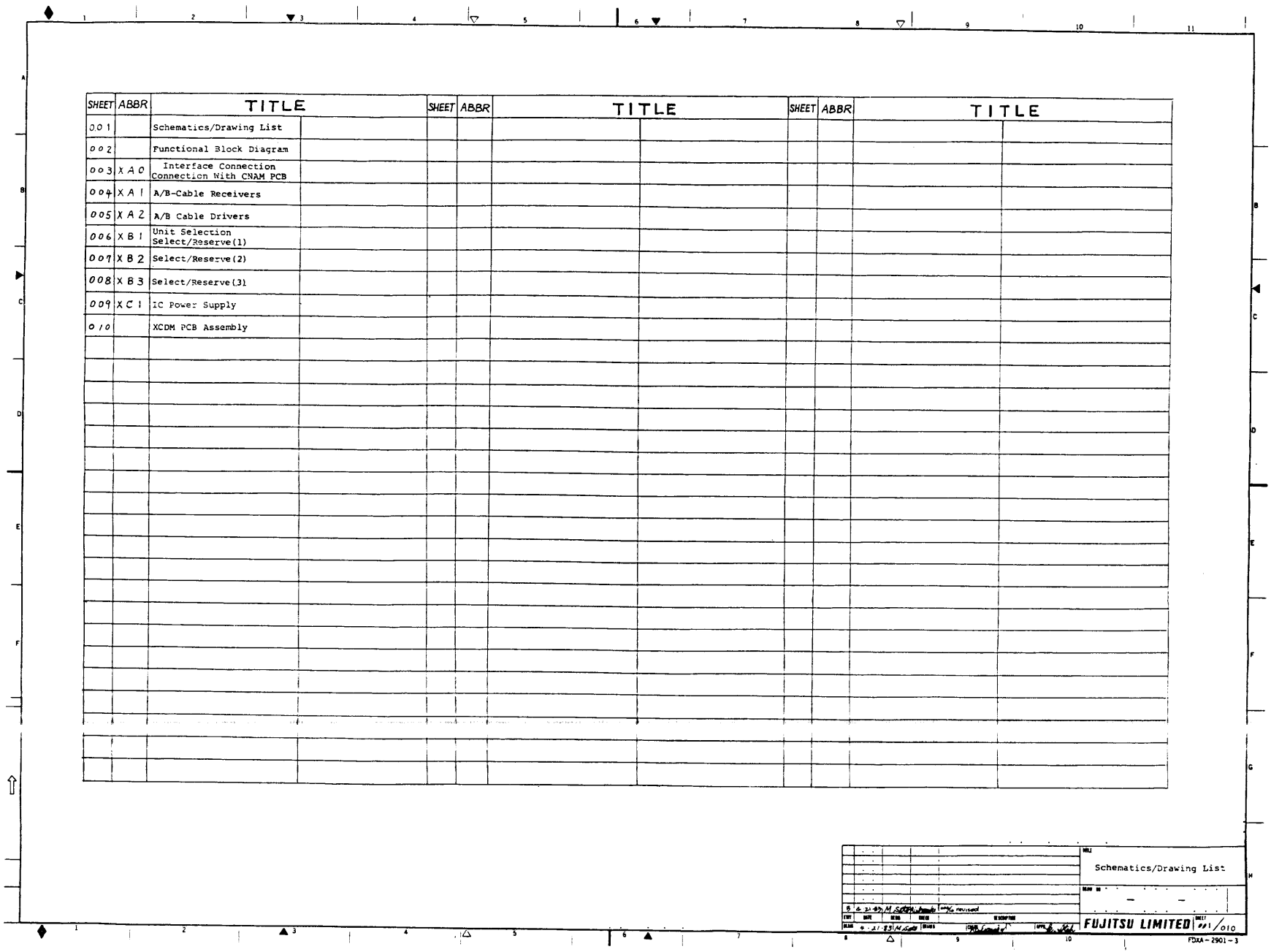
DRAW. NO
KS14C - 3256 - D462

FUJITSU LIMITED

SHEET 49

FDXA-3901-3

B03P-4740-0111A...02C



SHEET	ABBR	TITLE
001		Schematics/Drawing List
002		Functional Block Diagram
003	XA0	Interface Connection Connection With CNAM PCB
004	XA1	A/B-Cable Receivers
005	XA2	A/B Cable Drivers
006	XB1	Unit Selection Select/Reserve(1)
007	XB2	Select/Reserve(2)
008	XB3	Select/Reserve(3)
009	XC1	IC Power Supply
010		XCDM PCB Assembly

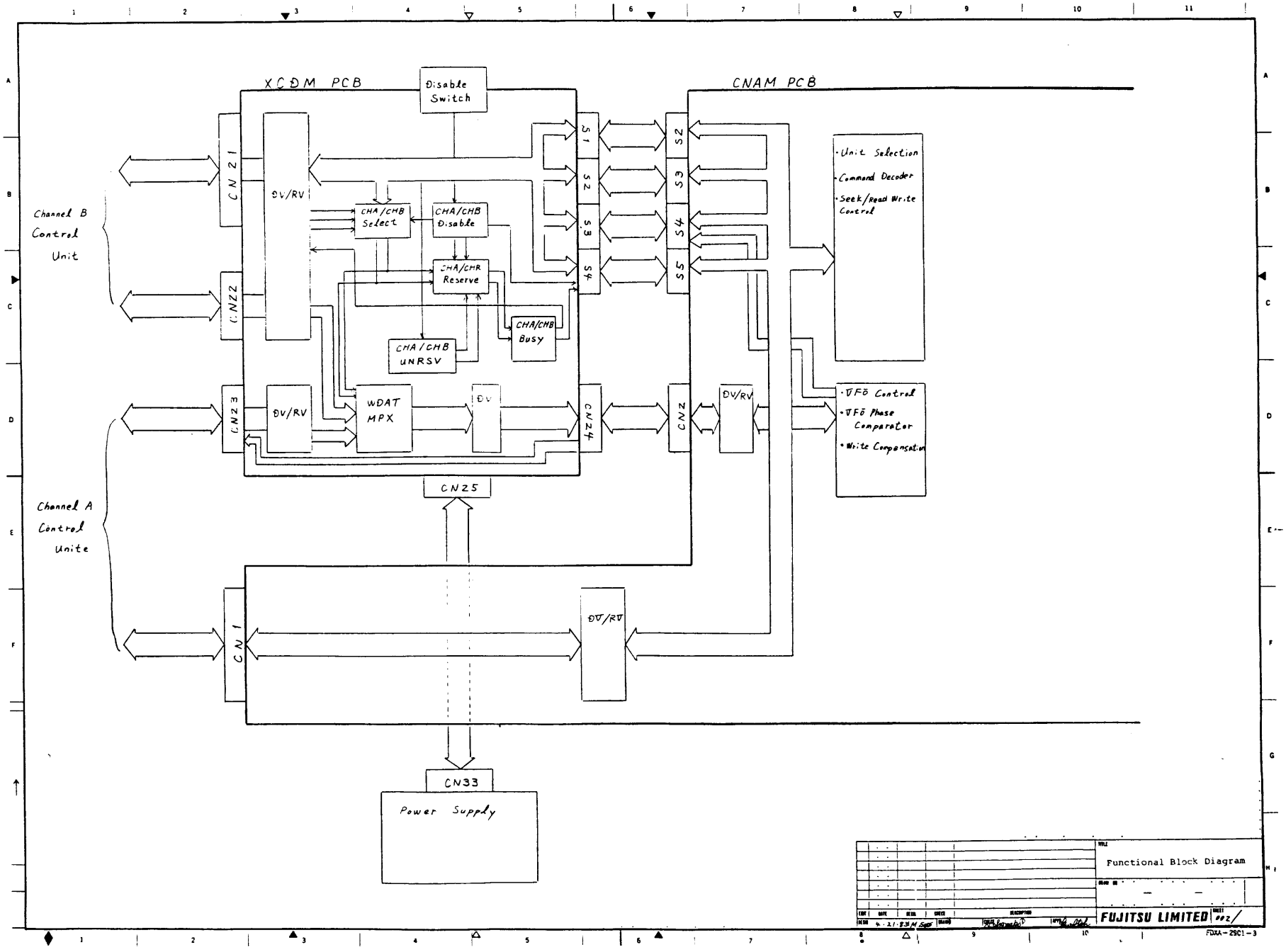
SHEET	ABBR	TITLE

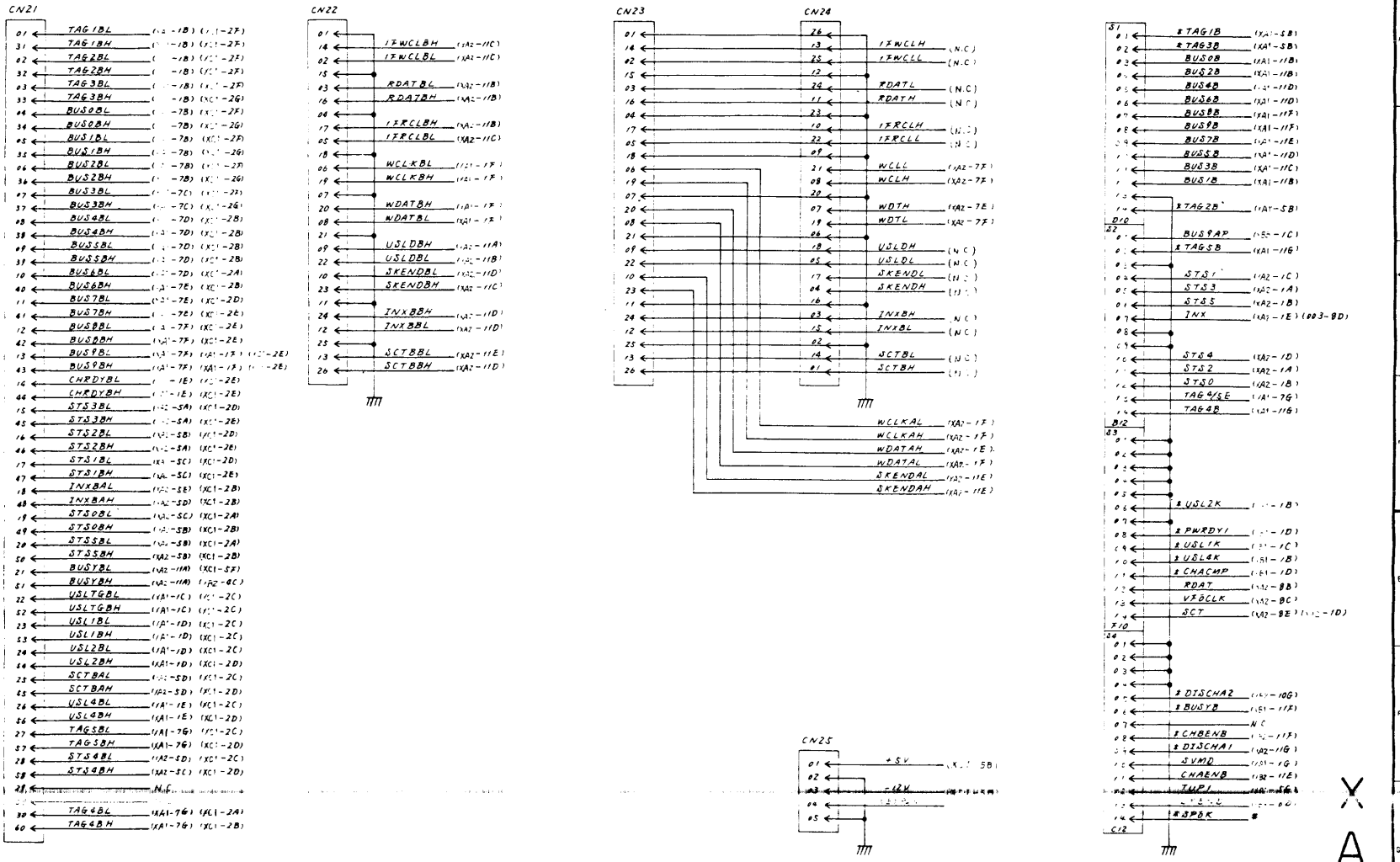
SHEET	ABBR	TITLE

Schematics/Drawing List

FUJITSU LIMITED 001/010

FDXA-2901-3

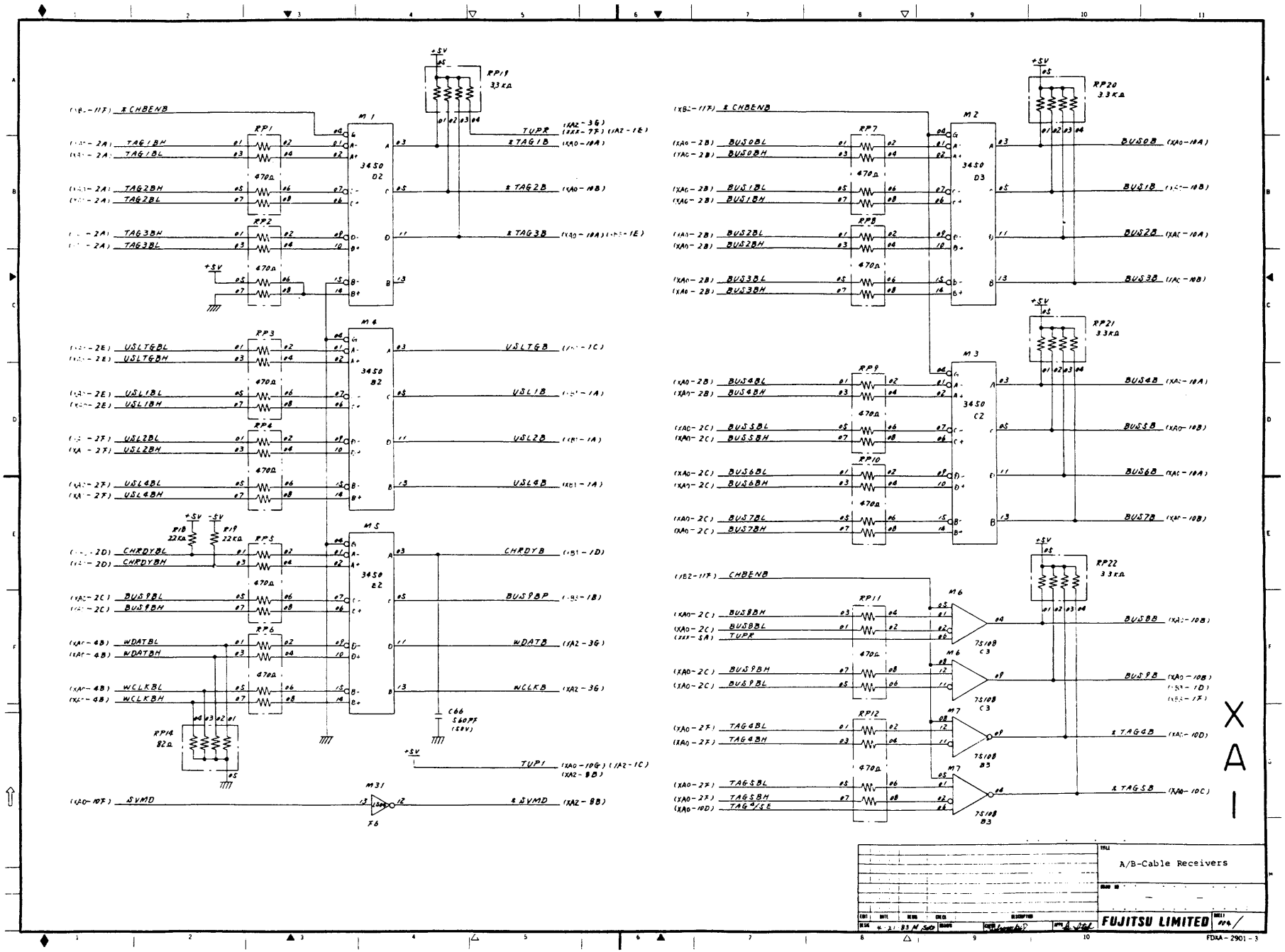

XCDM PCB
Disable Switch
CNAM PCB
CN21
CN22
CN23
CN24
CN25
CN1
CN2
CN33
DV/RV
CHA/CHB Select
CHA/CHB Disable
CHA/CHB Reserve
CHA/CHB Busy
CHA/CHB UNRSV
WDAT MPX
DV
DV/RV
S1
S2
S3
S4
S5
Channel B Control Unit
Channel A Control Unite
· Unit Selection
· Command Decoder
· Seek/Read Write Control
· VFO Control
· VFO Phase Comparator
· Write Compensation
Power Supply
Functional Block Diagram
FUJITSU LIMITED
FDXA-2901-3

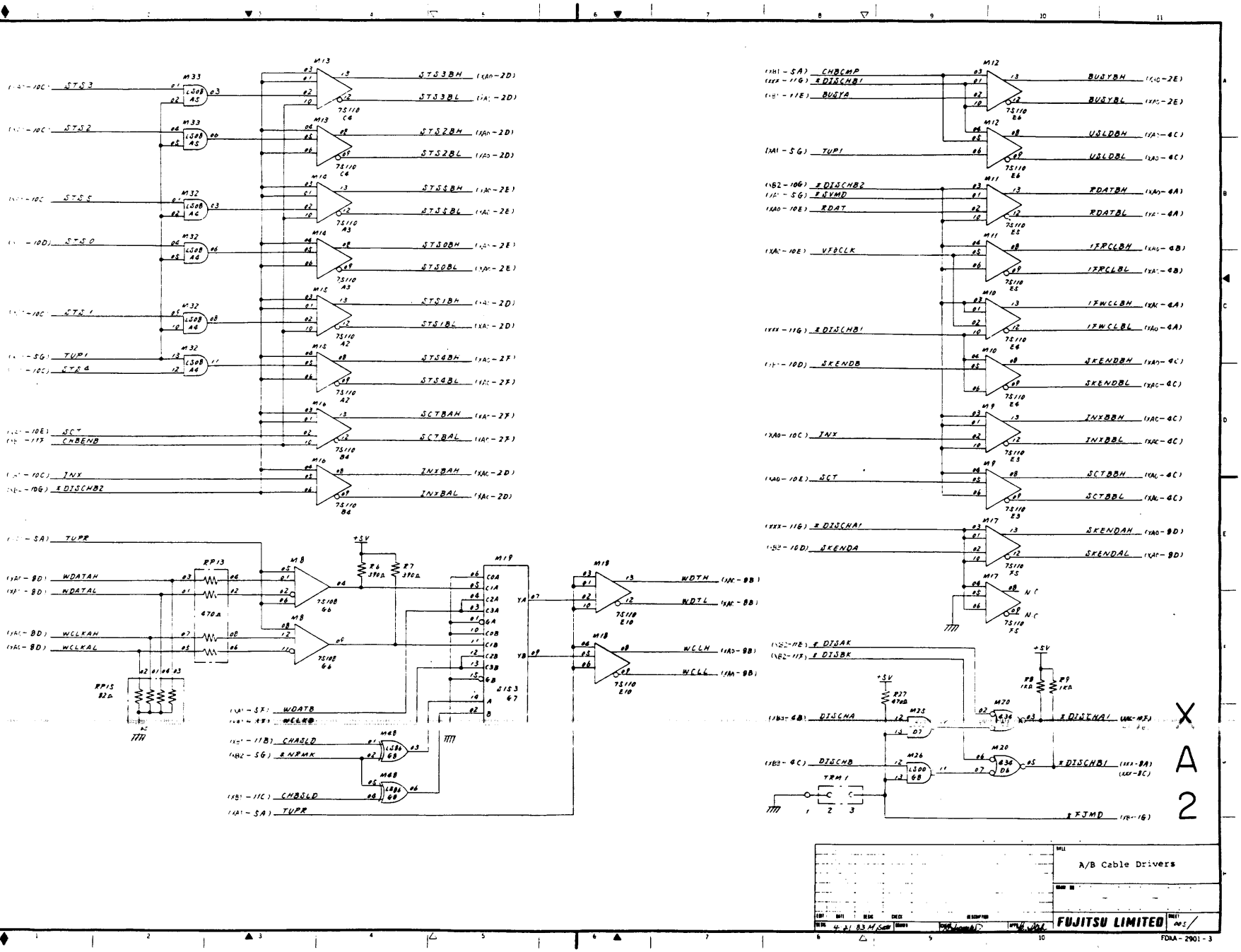


Interface Connection
Connection With CNAM PCB

FUJITSU LIMITED

FDXA-2901-3


A/B-Cable Receivers
FUJITSU LIMITED
FDRA-2901-3
X
A
I



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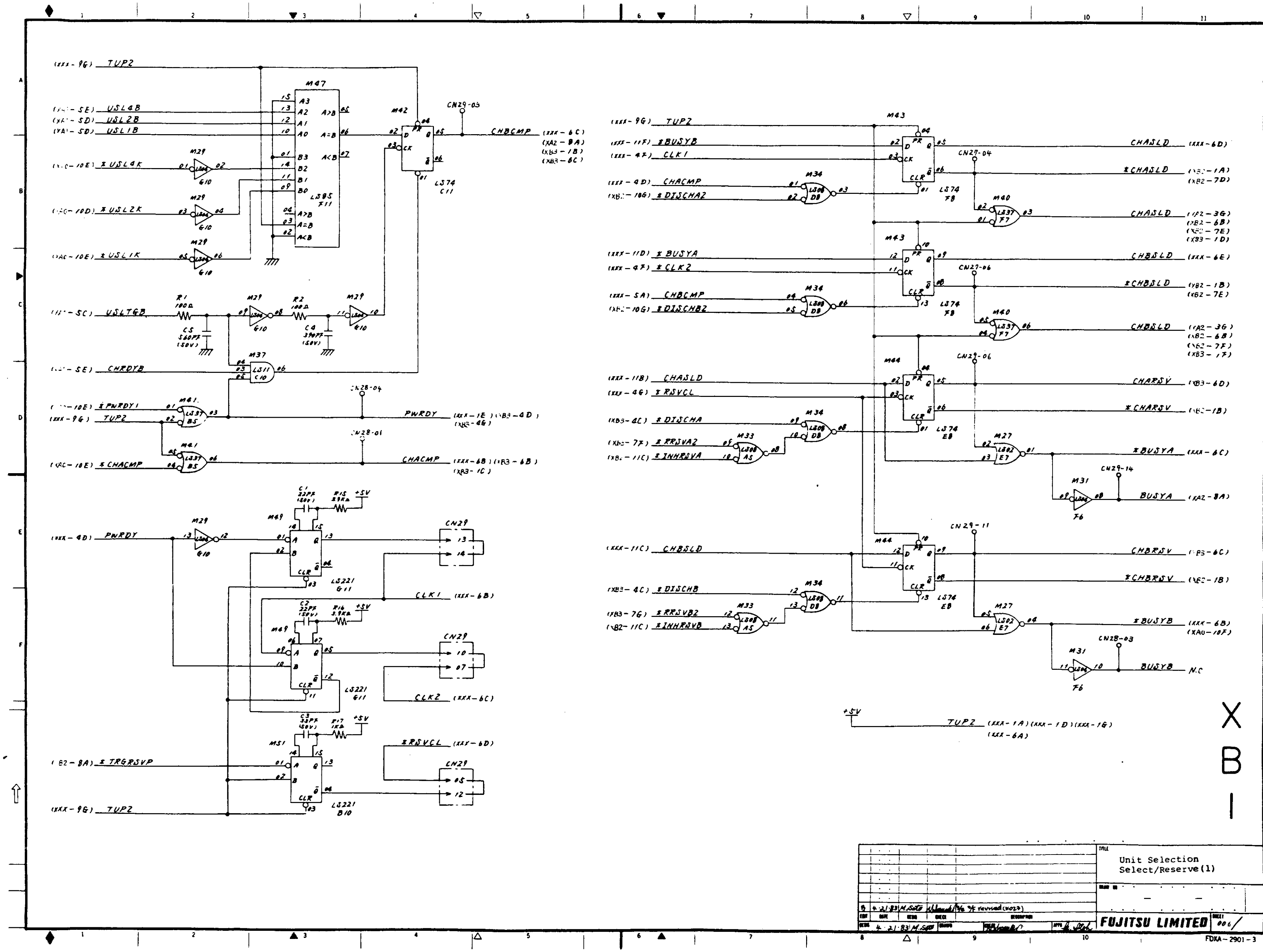
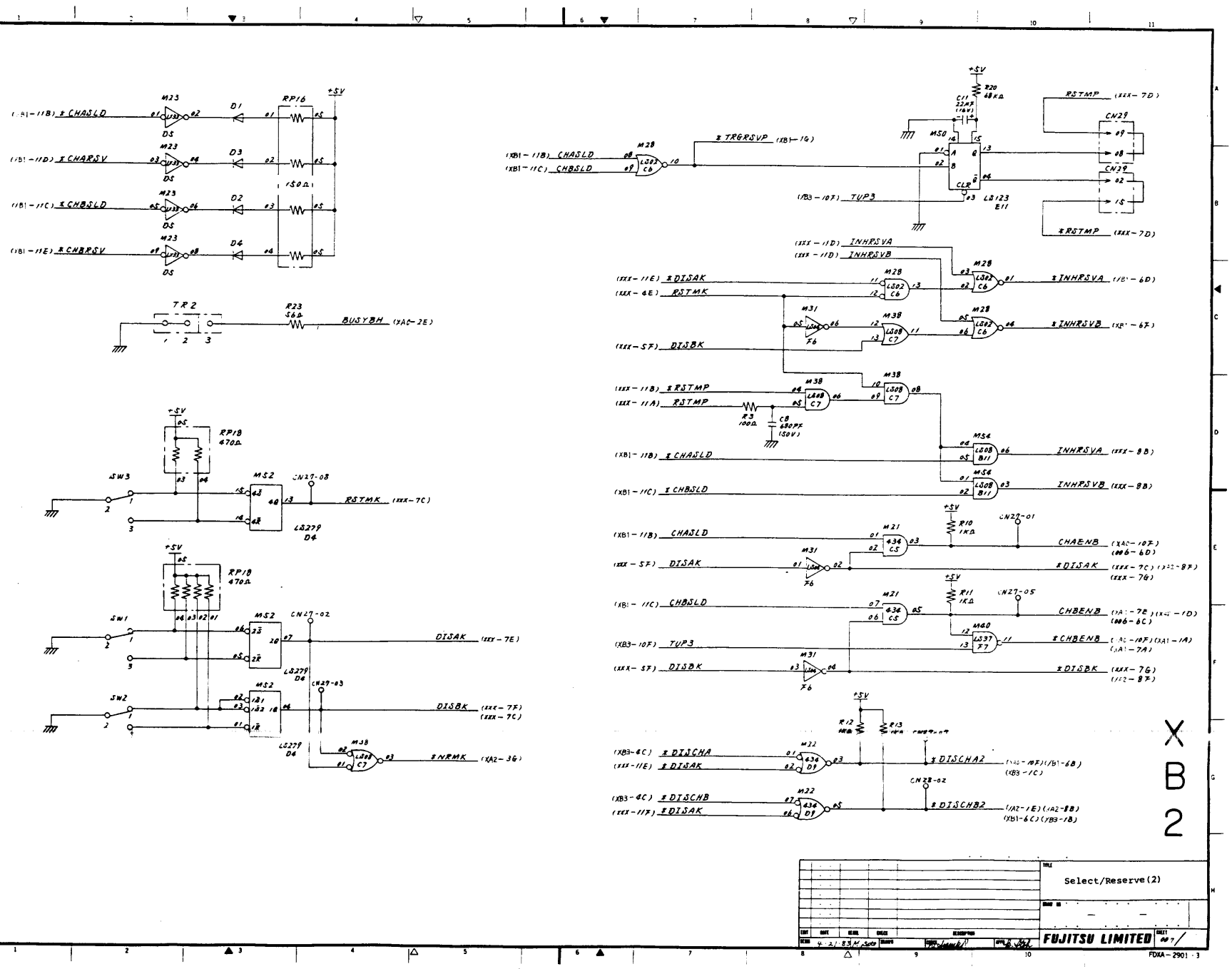
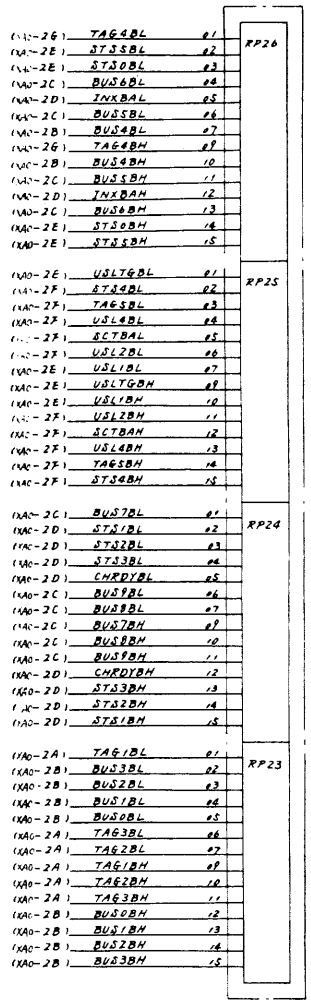
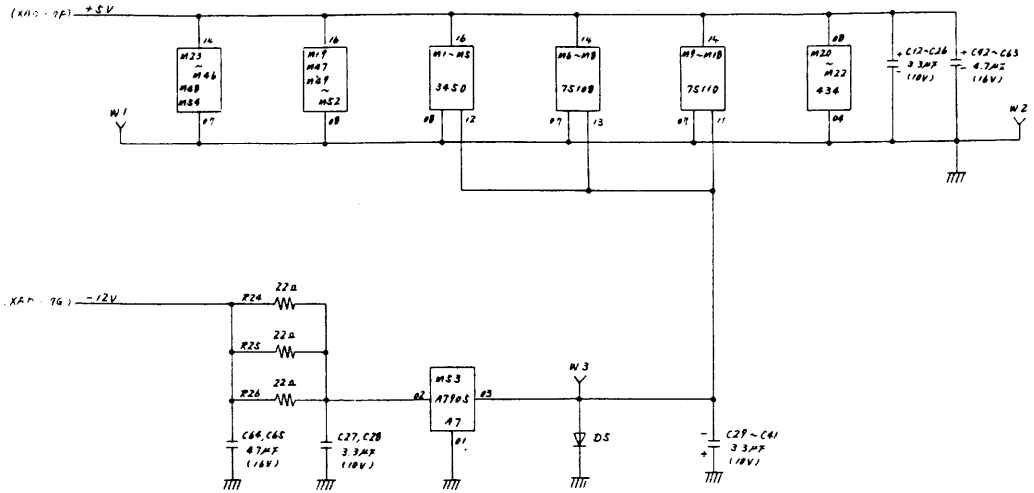
10-56

X A 2


TUP2
USL4B
USL2B
USL1B
*USL4K
*USL2K
*USL1K
M47
LS85
F11
M42
LS74
C11
CN29-03
CHBCMP
USLTGB
CHRDYB
*PWRDY1
*CHACMP
PWRDY
CHACMP
CN28-04
CN28-01
M29
M37
M41
M49
LS221
G11
CLK1
CLK2
M51
B10
*TRGRSVP
*RSVCL
CN29
M43
*BUSYB
*DISCHA2
CHASLD
*CHASLD
CN29-04
M40
LS37
F7
*BUSYA
*CLK2
CHBSLD
*CHBSLD
*DISCHB2
M44
LS74
E8
*DISCHA
*RRSVA2
*INHRSVA
CHARSV
*CHARSV
M27
LS02
E7
M31
F6
BUSYA
CN29-14
CN29-11
*DISCHB
*RRSVB2
*INHRSVB
CHBRSV
*CHBRSV
BUSYB
CN28-03
N.C
+5V
X
B
I
Unit Selection
Select/Reserve(1)
FUJITSU LIMITED
FDXA-2901-3


Select/Reserve(2)
FUJITSU LIMITED
FDXA-2901-3
X B 2

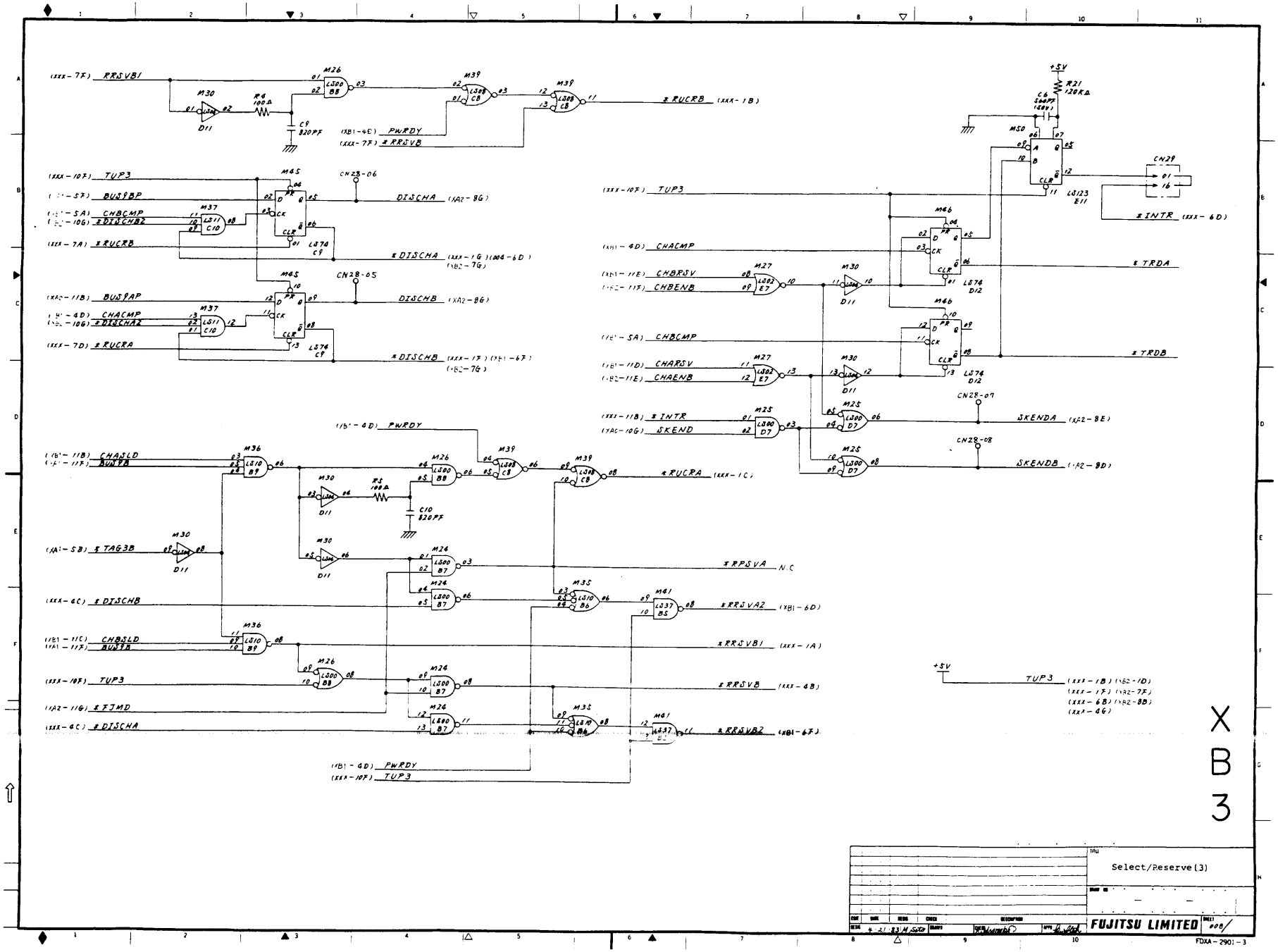




XCI

TITLE	IC Power Supply
SIZE	—
DRAWN	FUJITSU LIMITED

FDXA-2901-3



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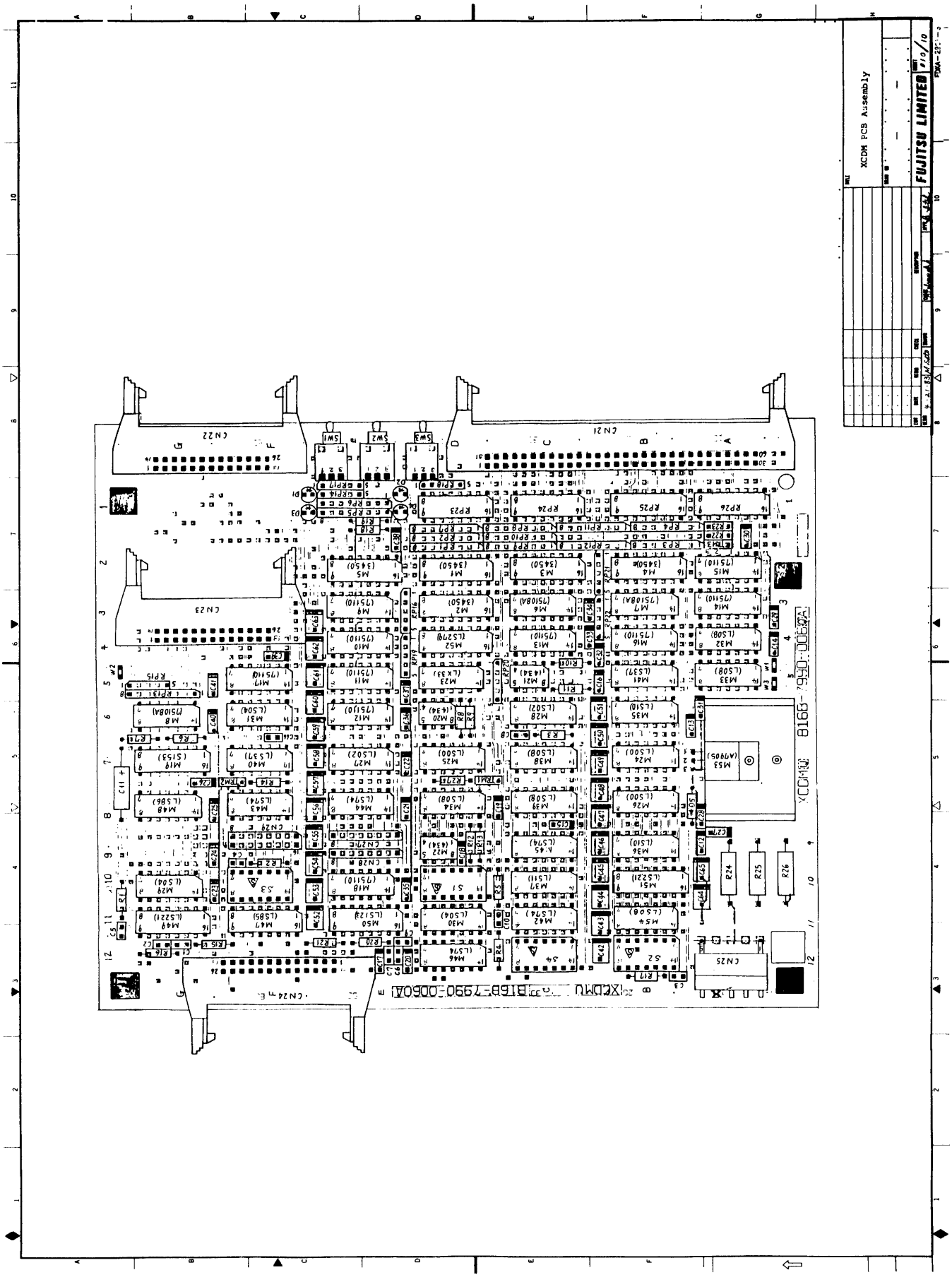
XCDM PCB Assembly
FUJITSU LIMITED
CN22
CN21
CN23
CN25
CN24
SW1
SW2
SW3
R24
R25
R26

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