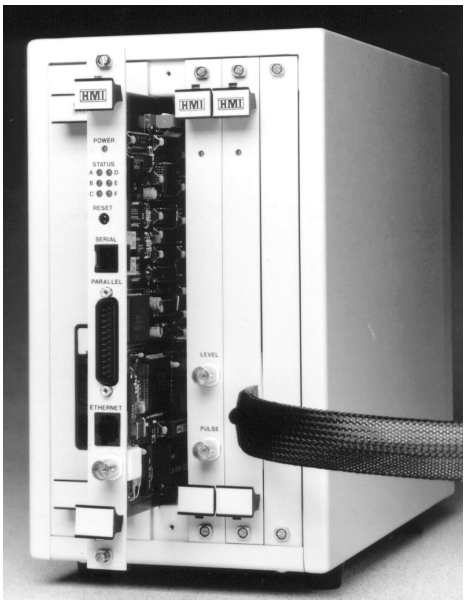
# HMI SPS 2000 PowerPC Development System

HMI announces the latest innovation in development tools for PowerPC processsors with the new SPS 2000 Series. The SPS (Smart Pod System) provides support for numerous PowerPC variants simply by changing pods. A new enhanced feature set will insure that you have the most powerful development tool available for the PowerPC. Of course, you would expect nothing less from HMI, the leader in microprocessor development tools!


*The SPS 2000 PowerPC emulator is a high performance development system which combines the control of an in-circuit emulator with the power of a logic analyzer to provide a complete debugging environment for hardware and software.*

- Real-time emulation up to 40MHz*
- 512K of emulation overlay memory std. (1, 2, or 4 MB optional). 512K Shadow RAM for real-time data monitoring.
- Time based delays for break and trigger points
- Eight levels of trigger and break sequencing logic
- Up to 8192 separate trace buffers for windowing code of interest. User defined trace buffer size of up to 128K.
- Trace qualification to allow selective tracing. Freeze trace allows viewing of trace buffers and changing of events during emulation.
- High-speed host communications via 115.2KB RS-232 serial port or Ethernet. Parallel port for fast code downloads.
- Hardware based Performance Analysis provides analysis of up to 8 test modules, minimum/maximum/average execution time displays, histograms, code coverage displays, and trace data time stamping.




*Backplane based design results in high reliability and allows for easy expandability and in-field service. 3' emulation cable for those tough to reach target systems.*

## SPS 2000 PRODUCT INFORMATION

HMI SPS 2000 Series in-circuit emulators represent the best in emulation technology and provide the most accurate and complete microprocessor development systems available.

Primary communication with the host computer is provided using a high speed serial port or standard Ethernet port. A parallel port is provided for high speed code downloads.

Overlay RAM may be mapped in small blocks throughout the memory address space of the target system. Shadow RAM blocks may be mapped to allow real-time monitoring of critical memory variables.

Breakpoint, trigger point, timing, and other emulator functions are activated by flexible user-defined conditions of up to eight levels deep with time delays.

Trace buffers capture addresses, data, control signals, and external trace bits. Source code information can also be shown. A Freeze Trace command allows trace buffers to be viewed without stopping emulation. User defines number and size of trace buffers shown.

A hardware based non-statistical software Performance Analysis system is standard. This premium system provides 50 nanosecond resolution timing information and displays results in easy to read histogram or raw data formats.

***Source-Level Debugger Support***

SourceGate II, HMI's acclaimed source-level debugger software, is supplied with all SPS 2000 Series emulators and provides full native GUI environment support for Windows 3.1/NT/95, SUN/SPARC, and HP platforms. Please see the back of this page for additional information on SourceGate II features.

***PowerPC Processor Support***

The HMI SPS 2000 PowerPC has pods available to support the Motorola MPC5xx, MPC8xx, and IBM4xx families. Future versions will be supported via new pods.

*1 wait state to emulation memory required for speeds >33MHz

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MOTOROLA EMBEDDED PLATINUM DEVELOPER