Mass Storage Unit

0402/0451

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION

THIS DOCUMENT AND THE INFORMATION CONTAINED THEREIN IS CONFIDENTIAL AND PROPRIETARY TO AND THE EXCLUSIVE PROPERTY OF HONEYWELL INFORMATION SYSTEMS INC. IT IS MADE AVAILABLE ONLY TO HONEYWELL FIELD ENGINEERING DIVISION PERSONNEL FOR THEIR USE SOLELY IN THE MAINTENANCE AND OPERATION OF HONEYWELL PRODUCTS. THIS DOCUMENT AND INFORMATION MUST BE MAINTAINED IN STRICTEST CONFIDENCE; IT MUST NOT BE REPRODUCED, IN WHOLE OR IN PART; AND IT SHALL NOT BE DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF HONEYWELL.

Honeywell

THIS DOCUMENT AND THE INFORMATION CONTAINED THEREIN IS CONFIDENTIAL AND PROPRIETARY TO AND THE EXCLUSIVE PROPERTY OF HONEYWELL INFORMATION SYSTEMS INC. IT IS MADE AVAILABLE ONLY TO HONEYWELL FIELD ENGINEERING DIVISION PERSONNEL FOR THEIR USE SOLELY IN THE MAINTENANCE AND OPERATION OF HONEYWELL PRODUCTS. THIS DOCUMENT AND INFORMATION MUST BE MAINTAINED IN STRICTEST CONFIDENCE; IT MUST NOT BE REPRODUCED, IN WHOLE OR IN PART; AND IT SHALL NOT BE DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF HONEYWELL.

83318200

MAGNETIC
PERIPHERALS INC.

MAGNETIC PERIPHERALS®
DISK STORAGE UNIT
BR3C9
BR3E4
BR3E5

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION

HARDWARE REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual Released
(10-1-75)	
B	Manual updated with technical and editorial changes.
(2-16-76)	
C	Revised to document models BR3E4, BR3E5 with Engineering Change Order 39617 plus
(9-30-76)	up dates with technical and editorial changes.
D	Revised to incorporate technical and editorial changes.
(6-20-78)	
E	Incorporate ECO 39882C changing CSAV to JSAV and add Power Sequence feature.
(9-25-80)	

Revision letters I,O,Q, and X are not used.

Address comments concerning this manual to:

Magnetic Peripherals Incorporated
Technical Publications Department
7801 Computer Avenue
Minneapolis, MN 55435

© 1975 , 1976 , 1978, 1980
By Magnetic Peripherals Incorporated
Printed in the United States of America

LIST OF EFFECTIVE PAGES

Sheet 1 of 2

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Cover	-
Proprietary Information	-
Title P	-
ii	E
iii	E
iv	B
v	E
Blank	-
vii	E
viii	E
ix	E
Blank	-
S-1 Div	-
Blank	-
1-1	A
1-2	C
1-3	D
1-4	A
1-5	B
Blank	-
S-2 Div	-
Blank	-
2-1	A
2-2	B
2-3	A
2-4	E
2-4.1	E

PAGE	REV
Blank	-
2-5	E
2-6	D
2-7	C
2-8	C
2-9	C
2-10	C
2-11	C
2-12	C
2-13	C
2-14	C
2-15	C
Blank	-
S-3 Div	-
Blank	-
3-1	A
3-2	A
3-3	A
3-4	A
3-4.1	E
3-4.2	E
3-5	E
3-6	A
3-7	E
3-8	E
3-9	E
3-10	E
3-11	A

PAGE	REV
3-12	A
3-13	A
3-14	A
3-15	A
3-16	A
3-17	A
3-18	A
3-19	A
3-20	A
3-21	A
3-22	E
3-23	A
3-24	A
3-25	A
3-26	E
3-26.1	E
Blank	-
3-27	C
3-28	A
3-29	B
3-30	A
3-31	A
3-32	C
3-33	C
3-34	A
3-35	A

PAGE	REV
3-36	A
3-37	D
3-38	A
3-39	A
3-40	A
3-41	A
3-42	A
3-43	C
3-44	A
3-45	D
3-46	D
3-47	A
3-48	A
3-49	E
3-50	E
3-51	E
3-52	E
3-53	A
3-54	A
3-55	D
3-56	C
3-57	D
3-58	A
3-59	C

PAGE	REV
3-60	A
3-61	A
3-62	A
3-63	C
3-64	A
3-65	A
3-66	A
3-67	A
3-68	C
3-69	A
3-70	A
3-71	A
3-72	A
3-73	A
3-74	A
3-75	A
3-76	A
3-77	A
3-78	A
3-79	A
3-80	A
3-81	A
3-82	A
3-83	A

LIST OF EFFECTIVE PAGES

Sheet 2 of 2

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
3-84	A
3-85	A
3-86	A
3-87	A
3-88	A
3-89	A
3-90	A
3-91	A
3-92	A
3-93	A
3-94	A
3-95	A
3-96	A
3-97	A
3-98	A
3-99	A
3-100	A
3-101	A
3-102	A
3-103	A
3-104	D
3-105	A
3-106	A
3-107	A

PAGE	REV
3-108	A
Blank	-
Cover	-

PREFACE

This manual contains reference information applicable to the BR3C9/BR3E4/BR3E5 disk storage unit. It has been prepared for customer engineers and other technical personnel directly involved with maintaining this equipment.

Information in this manual is applicable to the BR3C9 models A/B/C/D/J/K and BR3E4/BR3E5 A/B/E.

Reference information is divided into three sections. These sections and a brief description of their contents are listed below.

Section 1 - General Description: Describes equipment functions, specifications and equipment number identification.

Section 2 - Operation: Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation: Describes basic logic and mechanical functions.

For further information concerning the BR3C9 refer to the following manuals.

Publication No.	Title
83318100	BR3C9/BR3E4/BR3E5 - Installation and Checkout, Preventive Maintenance, Corrective Maintenance, Diagrams, Wire Lists.
83318300	BR3C9/BR3E4/BR3E5 - Parts Data
83318600	BR3D5/BR3D6/BR3C9/BR3E2/BR3E3/BR3E4/BR3E5 - Key to Logic, Integrated Circuits, Discrete Circuits, Card Schematics, Card Component Layout Diagrams.

CONTENTS

1. GENERAL DESCRIPTION

General 1-1
Assembly Location 1-1
Introduction 1-1
Top Cover Assembly 1-4
Deck Assembly 1-4
AC Power Supply 1-4
Logic Chassis 1-4
Equipment Identification 1-5

2. OPERATION

Introduction 2-1
Operating Instructions 2-4.1
Power Application 2-4.1
Power Down 2-6
Disk Pack Handling 2-6
Disk Pack Installation 2-6
Disk Pack Removal 2-7
Head Alignment Card 2-7
Off Line Tester
Preparation for Use 2-7
Operating Procedures 2-11
Error Detection 2-11
Seek Operations 2-11
Head Selection 2-13
Read Operations 2-13
Write Operations 2-14

3. THEORY OF OPERATION

Introduction

3A. ELECTROMECHANICAL FUNCTIONS

Introduction 3-1
Power Supply 3-4
General 3-4
AC/DC Distribution 3-4
Local/Remote Control 3-4
General 3-4
Local Control 3-4.1
Remote Control 3-4.1
Power On Sequence 3-4.1
Emergency Retract and Data Protection 3-8
Loss of AC Power 3-9
Control Interlock Opening 3-9
Loss of Speed 3-9
Loss of DC Power 3-9
Power Off Sequence 3-11
Logic Chassis Assembly 3-11
Deck Assembly 3-11
General 3-11
Drive Motor 3-11
Hysteresis Brake 3-11
Spindle Assembly 3-13
Actuator 3-13
Transducers 3-17
First Seek Interlock 3-17
Blower System 3-17
Disk Pack 3-19

3B. LOGIC FUNCTIONS

Introduction 3-20
Device Level Interface 3-20
Commands 3-20
Command Execution 3-20
Seek Operations 3-41
General 3-41
Servo Circuit Operation 3-43
Basic Seek Operations 3-45
Introduction 3-45
Accelerate Phase 3-45
Coast Phase 3-48
Decelerate Phase 3-48
Stop Phase 3-48
Short Seeks 3-49
Types of Seeks 3-49
Introduction 3-49
First Seek (Load) 3-49
Direct (forward/reverse)Seek 3-52
Return to Zero Seek 3-59
End of Travel Detection 3-59
Seek Status and Error Conditions 3-63
General 3-63
Normal Status Conditions 3-63
Device Level Interface Errors 3-63
Device Fault Conditions 3-64
Track Servo Circuit 3-64
General 3-64
Dibit Gating 3-66
Track Servo Signal Generation 3-66
Cylinder Pulse Generation 3-68
Machine Clock Circuits 3-68
General 3-68

Clock Generation 3-68
Write Clock 3-71
Index Detection Circuit 3-72
Sector Circuit 3-72
Read/Write Operations 3-72
General 3-72
Head Selection 3-72
Basic Read/Write Principles 3-76
General 3-76
Track Format 3-76
Principles of MFM Recording 3-78
Disk Surface Recording 3-79
Write Operations 3-79
General 3-79
Basic Write Sequence 3-79
Serdes Serializer 3-82
Write Compensation 3-84
Write Driver Circuits 3-88
Writing Address Marks 3-88
Write Fault Detection 3-88
Read Operations 3-90
General 3-90
Basic Read Sequence 3-90
Read Circuits 3-92
Sense Operations 3-103
General 3-103
Summary Status Request 3-103
Fault Detection 3-104
Diagnostic Operations 3-104
General 3-104
Diagnostic Commands 3-104
Write Test Diagnostics 3-104

FIGURES

1-1 Assembly Locations 1-1
2-1 Controls and Indicators 2-5
2-2 Off Line Tester 2-8
3-1 Simplified Logic Symbology 3-2
3-1.1 Local/Remote Power Sequencing Control Circuits 3-4.2
3-1.2 Remote Mode Power Sequencing 3-4.2
3-2 Power Distribution 3-5
3-3 Power Sequencing 3-6
3-4 Power Interlocks 3-7
3-5 Power Off Timing 3-10
3-6 Deck Assembly 3-12
3-7 Spindle Assembly 3-13
3-8 Actuator Assembly Elements 3-14
3-9 Head Loading 3-15
3-10 Head/Arm Assembly Motion 3-16
3-11 Speed Detection 3-17
3-12 Velocity Detection 3-18
3-13 Blower System 3-18
3-14 Drive Block Diagram 3-21
3-15 Device Level Interface Lines 3-22
3-16 Command Decode and Abbreviations 3-23
3-17 Command Decoding Logic 3-24
3-18 SRI Timing 3-42
3-19 Servo Circuits Simplified Schematic 3-46
3-20 Servo Circuit Simplified Signals 3-47
3-21 First Seek Flow Chart 3-50
3-22 First Seek Timing 3-51
3-23 Direct Seek Flow Chart 3-53
3-24 Direct Seek Timing 3-55
3-25 RCB Flow Chart 3-60
3-26 RCB Timing 3-61
3-27 Track Servo Circuit Simplified Schematic 3-62
3-28 Disk Surface Layout 3-65
3-29 Track Servo Circuit Simplified Signals 3-69
3-30 Dibits Detect 3-69
3-31 Cylinder Pulses Generation 3-70
3-32 Machine Clock Circuit 3-71
3-33 Index Detection Circuit 3-73
3-34 Sector Circuit 3-74
3-35 Read/Write Circuits Block Diagram 3-75
3-36 Head Selection Circuit 3-77
3-37 MFM Recording 3-78
3-38 Magnetic Recoding 3-80
3-39 Read Current 3-80
3-40 Write Circuits 3-81
3-41 Write Timing 3-83
3-42 Write Irregularity 3-85
3-43 Read Shift 3-86

3-44	Write Compensation Circuit	3-87	3-51	Phase Lock Oscillator Circuit	3-97
3-45	Write Driver Circuits Timing	3-89	3-52	Data Separator Circuit	3-98
3-46	Read Circuits	3-91	3-53	Serdes Read Circuit	3-101
3-47	AGC Amplifier Stage	3-92	3-54	Read Timing	3-102
3-48	Level Detection Circuit	3-94	3-55	Device Fault Logic	3-106
3-49	Time Constant Control Circuit	3-95	3-56	DLI Fault Logic	3-107
3-50	Data Latch Circuit	3-96	3-57	Diagnostic Mode Logic	3-108

TABLES

1-1	Electrical Specifications	1-2	3-2	Signal Lines	3-25
2-1	Controls and Indicators	2-1	3-3	Commands	3-26.1
2-2	Off Line Tester Switch Functions	2-8	3-4	Servo Circuit Functions	3-43
3-1	Abbreviations	3-3			

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The BR3C9 is a high speed, random access, data storage device that records and recovers data using portable disk packs.

The equipment specifications for this unit are listed in Table 1-1.

ASSEMBLY LOCATIONS

General

Figure 1-1 illustrates the major drive assemblies. Detailed information on the construction and function of these assemblies is provided in section 2 of this manual.

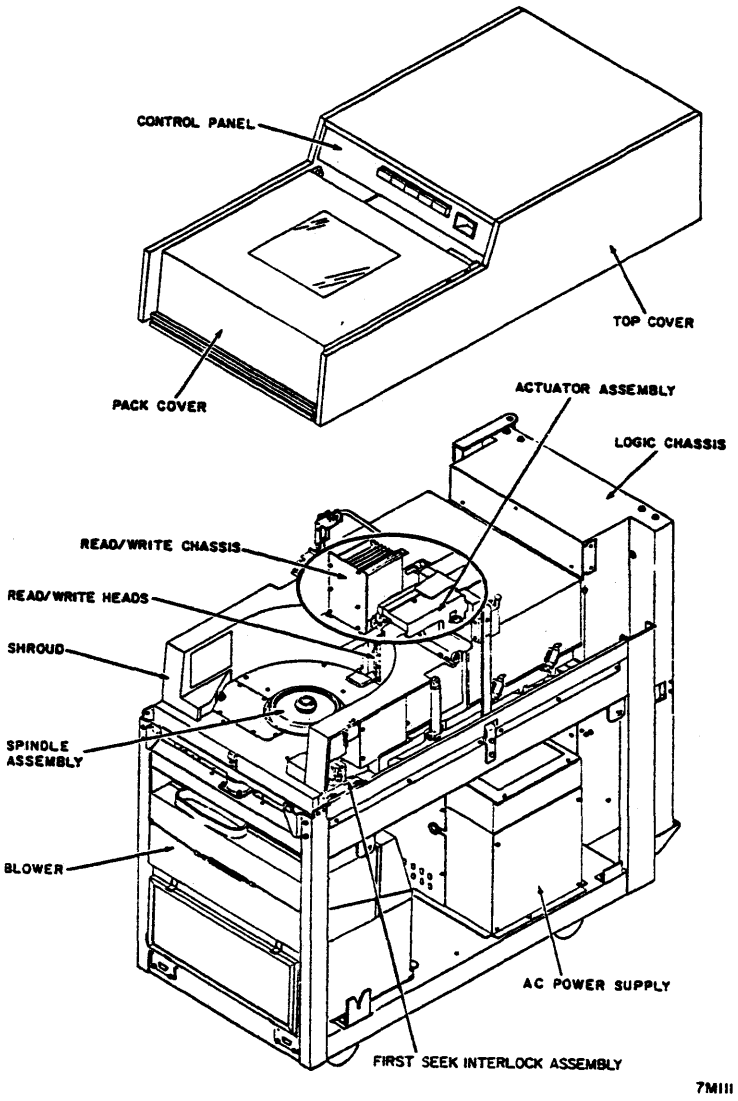


Figure 1-1. Assembly Locations

TABLE 1-1. EQUIPMENT SPECIFICATION

Specification	Value			
Size				
Height	39.25 in (997 mm)			
Width (Front)	22 in (559 mm)			
Depth	44.5 in (1130 mm)			
Weight	680 lbs (309 kg)			
Temperature				
Operating	60°F (15.5°C) to 90°F (32°C)			
Gradient	12°F (6.6°C) per hour			
Non-Operating	-30°F (-34°C) to +150°F (66°C)			
Gradient	36°F (20°C) per hour			
Humidity				
Operating	20% to 80% (providing there is no condensation)			
Non-Operating	5% to 90%			
Altitude				
Operating	-1000 ft (305 m) to +7000 ft (2134 m)			
Non-Operating	-1000 ft (305 m) to +16000 ft (4877 m)			
Input Voltage				
BR3C9A,B	208v (+10%,-15%), 60 (±1%) Hz			
BR3C9C,D	220v (+10%,-15%), 50 (±1%) Hz			
BR3E4,A	208v (+10%,-15%), 60 (±1%) Hz			
BR3E4,B	220v (+10%,-15%), 50 (±1%) Hz			
BR3E5,A	208v (+10%,-15%), 60 (±1%) Hz			
BR3E5,B	220v (+10%,-15%), 50 (±1%) Hz			
Power Consumption	**Standby**		**Accessing**	
	60 Hz	**50 Hz**	**60 Hz**	**50 Hz**
Current	2.0 Amps	2.5 Amps	8.0 Amps	8.5 Amps
True Power	0.4 KW	0.5 KW	1.2 KW	1.3 KW
Power Factor	0.9	0.9	0.7	0.6
Heat Dissipation	1400 BTU	1750 BTU	4200 BTU	4500 BTU
Starting Current	**Time**		**208v**	**220v**
	0-6 sec		38	40
	6-8 sec		38	25
	8-10 sec		20	12
	10-12 sec		12	8
	12-14 sec		8	8

TABLE 1-1. EQUIPMENT SPECIFICATION (CONT'D)

Specification	Value
Channel Configuration	
BR3C9A/C, BR3E4A, BR3E4B	Single
BR3C9B/D, BR3E5A, BR3E5B	Dual
Data Capacity	
BR3C9A/B/C/D	200 megabytes
BR3E4/BR3E5 A/B	100 megabytes
Disk Pack	
Packs/Drive	1
Recording Surfaces/Pack	19
Usable Tracks/Surface	823 (808 plus 15 spares) 411 (404 plus 7 spares) BR3E4/3E5
Tracks/inch	384
Tracks Spacing	0.0026 inch
Rotation Speed	3600 (±2%) rpm (16.7 ms/rev)
Recommended Pack	M4451
Seek Timing	
823 tracks	55 ms (maximum)
411 tracks BR3E4/3E5	40 ms (maximum)
1 track	8 ms (maximum)
Average	30 ms 25 ms BR3E4/3E5
Latency Time	
Average	8.33 ms (@ 3600 rpm)
Maximum	17 ms (@ 3528 rpm)

TABLE 1-1. EQUIPMENT SPECIFICATION (CONT'D)

Specification	Value
Recording	
Mode	Modified frequency modulation (MFM)
Bit Density	4040 bpi (inner track nominal)
Rate	6.45 MHz (nominal)
Recording Heads	
Quantity	20
Read/Write Width	0.0021 in (nominal) units

TOP COVER ASSEMBLY

The top cover assembly protects the drive assemblies during customer operations.

The pack cover is opened by means of a latch under the cover. An electrical switch senses the cover is opened, and disables spindle motor power.

DECK ASSEMBLY

The deck assembly has the following major subassemblies:

- A spindle assembly to mount the disk pack. Its associated drive motor runs continuously whenever a pack is installed, the pack cover is closed, the START switch is on, and sequence power (either from the controller or with the LOCAL/REMOTE switch on the power supply in the LOCAL position) are available.
- An actuator assembly that mounts the read/write heads for processing data. The actuator contains a voice coil positioner controlled by a closed-loop, continuous-feedback servo system
- A shroud to surround the disk pack. The shroud: protects the pack, aids in directing air from the blower to the pack; and prevents the operator from damaging the read/write heads with the pack.
- A read/write chassis to mount logic cards that contain logic directly affecting head selection and operation.
- A first seek interlock assembly to provide a heads load command delay.

AC POWER SUPPLY

The ac power supply provides ac power required by the drive. The ac voltages generated are distributed to the dc power supply located in the logic chassis assembly.

The line filter filters the ac power input to the power supply.

LOGIC CHASSIS

The logic chassis serves as the mounting point for the main complement of the logic cards and dc power supply. The chassis is hinge-mounted for easy access to the cards (which plug in at the inner side of the chassis) or to the backpanel terminals (at the outer side). The backpanel terminals provide ready access to all signals entering and leaving each card. In addition, the cards have test points for monitoring critical signals within the cards.

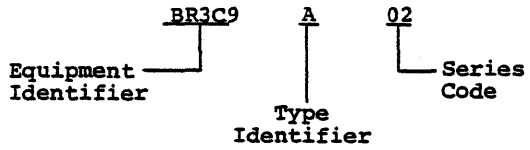
The logic chassis also contains a test point panel that provides a location for status monitoring of the dc voltages generated by the dc power panel.

Located in the lower half of the logic chassis is the dc power panel. The dc power panel provides dc power required by the drive. It also contains relays and solid state logic used for power sequencing.

EQUIPMENT IDENTIFICATION

An equipment number is assigned to each drive to identify its configuration. This provides a systematic method of identifying, accounting, and controlling changes that affect drive logic and mechanical components.

The equipment configuration is identified by a nameplate attached to the frame at the back of the drive. The nameplate is visible with the logic chassis open. The Equipment Identification Number will be similar to the following:



The Equipment Identifier indicates the basic function of the unit. This number will be BR3C9 on all units for which this series of manuals have been prepared.

The Type Identifier indicates a non-interchangeable difference in equipments that affects the interface. The term "Mod" is sometimes used interchangeably with "Type Identifier".

The Series Code Changes with each non-interchangeable change within the equipment.

Drives with different series codes are fully interchangeable at the system level; however, not all of their electrical or mechanical components may be interchangeable. Series codes are changed by Engineering Change Order (ECO) only at the factory.

Other changes are accomplished by Field Change Order (FCO). These changes may be installed either at the factory or by field personnel. FCO changes are indicated by an entry on the FCO Log that accompanies each machine. It is important that this log be kept current by the person installing each FCO.

Unless otherwise specified, all theory, procedures, and diagrams in these manuals apply to all units. Exceptions are noted where applicable.

Manuals accompanying unit shipments from the manufacturer match the configuration of those units. Subsequent manual changes are controlled by the Revision Record sheet behind the title page of every manual. This sheet identifies the Series Code and FCO effectivity of manual changes. If maintenance will be performed using a manual other than the manual supplied with each drive, verify that the manual and drive configurations match.

SECTION 2

OPERATION

OPERATION 2

INTRODUCTION

The drive contains several panels and indicators.

Figure 2-1 locates the panels and indicators on a cabinet. Table 2-1 describes the various panel controls and indicators.

TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
	Operator Panel
START/STOP Switch/indicator	Controls power on and off sequences. If the indicator is not lighted (indicating drive is in a power down condition) depressing the switch does the following: • Lights the indicator • Energizes the spindle drive motor • Initiates the first seek sequence This happens only if the disk pack is in place with canister removed, the pack cover is closed, and the circuit breakers are on. If the indicator is lighted (indicating the unit is powered up) depressing the switch extinguishes the indicator and causes a power off sequence.
READY indicator	Lights when the heads are loaded and the unit is ready to accept commands.
PROTECT switch/indicator	Depressing this switch lights the indicator and inhibits the drive from writing on the pack.
OFFLINE indicator	Lights when the drive has experienced any of the following conditions: • Controller issued a Set Local State command • ONLINE switch on maintenance panel set to an offline position.
Logic Plug	Determines the device number of the drive. Each plug has a fixed number which is changed by replacing the present plug with one having a different number. The controller determines the device number via a Device Number Request command (Tag 26).

TABLE 2-1. CONTROLS AND INDICATORS (CONT'D)

Control or Indicator	Function
Operator Panel (Cont'd)	
CHECK switch/indicator	Lights when one or more of the following fault conditions occur. • Read or Write is commanded without an On Cylinder signal. • Low voltage (±5v, ±20v, or -16v) condition • Read and Write commanded at the same time • Servo dibits lost for more than 200 ms • More than one head selected • Air flow has decreased below an acceptable limit • Head register contains number exceeding 18 (no head select) • Write command without write current • Write Current without Write command
Logic Chassis Maintenance Panel	
	NOTE The POSITIONER OFFSET and READ CLOCK switches are designed for use during a maintenance situation. Functions of the two switches are enabled only when the ONLINE switch is set to either OFF LINE position.
POSITIONER OFFSET switch	NORMAL position allows servo logic to position positioner to the nominal center of the disk pack servo recording track. OUT position injects a fixed bias so that positioner is positioned 400 microinches off nominal center of servo track in the direction away from the spindle. IN position injects a fixed bias so that carriage is positioned 400 microinches off nominal center of servo track in the direction toward the spindle.
READ CLOCK switch	NORMAL position allows read data strobe to occur in the nominal center of the allowable margin of the data window (time period in which a recovered data "1" must appear in order to be recognized as a "1"). ADV position causes data strobe to be moved to the advanced (early) margin position of the data window. (Data strobe occurs about 8 nanoseconds earlier than nominal). RET position causes data strobe to be moved to the retarded (late) margin position of the data window. (Data strobe occurs about 8 nanoseconds later than nominal.)

TABLE 2-1. CONTROLS AND INDICATORS (CONT'D)

Control or Indicator	Function
Logic Chassis Maintenance Panel (Cont'd)	
ONLINE/NORMAL/ WRITE PROTECT switch (Cont'd)	OFFLINE-WRITE PROTECT position causes same occurrences as for OFFLINE-NORMAL position and additionally disables the write circuits. Switching from OFFLINE to ONLINE causes an internal General Reset (equivalent to DIN).
CHECK switch/indicator	Indicator lights in response to one or more of the same conditions as listed for the operator panel CHECK switch/indicator. Pressing the logic chassis maintenance panel CHECK switch clears the Pack Unsafe FF and all bits of DSB1, DSB2, and DSB3.
+5, -5, +20, -20, and GND test jacks	Provide a point at which dc voltages in logic chassis can be measured. They must not be used as a power source.
Bidirectional Data Line bit indicators	Display information is selected by DISPLAY SELECT switch when in Offline mode. Indicator lights if selected signal is true.
DISPLAY SELECT switch	Ten position rotary switch that allows selection and display of machine status and register contents. Switch positions function as follows: 1. ADDRESS VERIFY is used only in conjunction with Off Line Tester. Tester operation stops if it detects difference between cylinder byte read from disk and contents of Cylinder Address register. Indicators display address read from disk. Error may be verified by setting switch to DSB4. Bit 2^6 (Tester Address Error) will be on.
ONLINE/NORMAL/ WRITE PROTECT switch	ONLINE position places unit under control of control unit. OFFLINE - NORMAL position causes the following: 1. Prevents control unit from initiating a seek or read/write operation. 2. Enables control of drive functions by Off Line Tester. 3. Lights LOCAL indicator. 4. Clears reserved status of drive, inhibiting gating of status signals (including OPI to controller.

TABLE 2-1. CONTROLS AND INDICATORS (CONT'D)

Control or Indicator	Function
Logic Chassis Maintenance Panel (Cont'd)	
DISPLAY SELECT switch (Cont'd)	2. CYLINDER causes contents of Cylinder Address register to be displayed. 3. DIFFERENCE causes contents of Difference Counter to be displayed. This value is complement of number tracks to go. 4. HEAD causes contents of Head Register to be displayed. 5. SUMMARY STATUS causes Summary Status (SSR) byte to be displayed. Refer to Table 2-2 for bit significance. 6. DSB2-DSB7 causes applicable Detailed Status byte to be displayed. Refer to Table 2-2 for bit significance. The meanings of the Summary Status and Detailed Status bytes are explained in Section 4.
	AC Power Supply
Elapsed Time Meter	Indicates cumulative hours that logic dc power is on.
DRIVE MOTOR circuit breaker	Controls application of ac voltage to spindle drive motor.
+20Y Fuses	Protects 20 volt power supply transformer used to derive +20Y sequence and lamp voltages.
	DC Power Supply
+20Y indicator	Lights to indicate presence of +20Y voltage used by lamps and power up sequence circuit.
±46, ±20, and ±10 volt circuit breakers	Control application of related dc voltages throughout drive.
Local/Remote Switch (Applies only to drives with Power Sequence feature)	Determines whether the power on sequences of the drives in a particular string are controlled independent of one another by the START switches or by the START switches working in conjunction with a power sequence signal received from either the controller or the first drive in the string. In the local mode, the power on sequences are controlled independently. However, in the remote mode, pressing the START switch starts a power on only if the drive is receiving the Pick signal. In remote, the drive receives the Pick signal only if all previous drives in the strinf have completed their power on, are in local, or are completely deenerigized (all circuit breakers off). The purpose of remote mode is to allow a sequential power up of all drives in the string. A sequential power up is accomplished by: 1. Closing all circuit breakers and setting the LOCAL/REMOTE switch of each drive to the REMOTE position. 2. Pressing the START switches to light the indicators of each drive except the first in the string. 3. Press the START switch to light the indicator of the first drive. The drives will now power up sequentially (see Local/Remote Control discussion for more information
	Main Breaker Box
UNIT Power circuit breaker	Controls application of main ac power.

OPERATING INSTRUCTIONS

POWER APPLICATION

The following procedure prepares the drive to go on-line.

1. Install a disk pack (refer to disk pack installation.
2. Set main breaker box UNIT POWER circuit breaker to ON. Blower motor will start.
3. Open cabinet logic chassis gate located at the rear of the drive cabinet.
4. Position logic chassis maintenance panel switches as follows:
   - POSITIONER OFFSET switch to NORMAL.
   - READ CLOCK switch to NORMAL
   - ON LINE switch to ON LINE
5. Close all dc power supply circuit breakers. The +20Y indicator (on the dc power supply) lights.
6. Close cabinet logic chassis gate.
7. Press operator panel START/STOP switch/indicator. This lights the indicator, starts the spindle drive motor and initiates the first seek sequence.
8. Completion of the first seek operation lights the operator panel READY indicator. The heads are now positioned at track 000 and the unit is ready to receive a command.

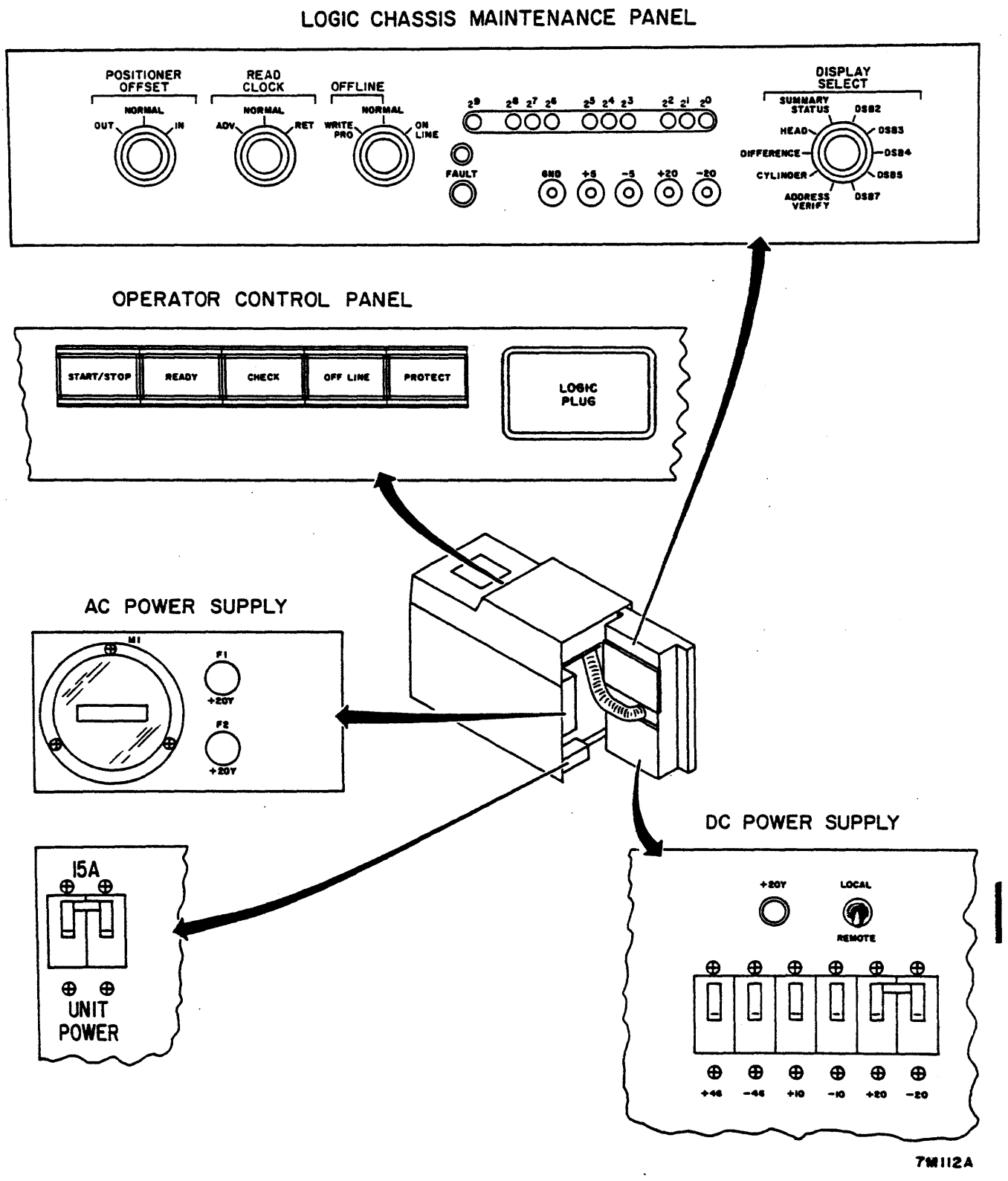


Figure 2-1. Controls and Indicators

POWER DOWN

The following procedure powers down the drive.

1. Stop the spindle motor and unload heads by either issuing a Set Standby State (Tag 13) from the controller or pressing the START/STOP indicator/switch on the operator panel.

WARNING

If pressing the START/STOP switch does not cause the heads to unload and the spindle motor to stop the following procedures must be followed to avoid personal injury or damage to the heads and disk pack.

1. Manually retract heads as follows:

   a. Open top cover from rear

   b. Disconnect yellow lead from voice coil

   c. Manually retract heads following precaution given in Section 5 of this manual under Maintenance Preliminary conditions

2. Remove main ac power from drive by opening UNIT POWER circuit breaker.

3. Determine cause of failure (normally an open lead to voice coil.

2. Remove main ac power to drive by opening UNIT POWER circuit breaker.

DISK PACK HANDLING

To ensure maximum disk pack life and reliability, observe the following precautions:

1. Store disk packs in a machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).

2. If a disk pack must be stored in a different environment, allow two hours for adjustment to the computer environment before use.

3. Never store a disk pack in sunlight, in a dirty environment, or on top of another disk pack.

4. Store the disk packs flat, not on edge.

5. Always be sure that both the top and bottom plastic cannister covers are on a disk pack whenever is is not actually installed in a drive.

6. When marking packs, use a pen or felt-tip marker that does not produce a loose residue. Never use a lead pencil. Write on the label before it is applied to the disk pack cannister.

7. Always close the disk drive pack access cover after loading or removing the disk pack. This will allow the disk drives positive air pressure system to keep the pack area free of any foreign particles.

8. Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack cannister if required.

DISK PACK INSTALLATION

Make certain that the disk pack to be installed has been properly maintained.

1. Raise drive front cover.

2. Lift the disk pack by the plastic canister handle.

3. Disengage the bottom dust cover from the disk pack by squeezing the levers of the releasing mechanism in the center of the cover and lifting the cover off. Set the cover aside to an uncontaminated storage area.

CAUTION

Make certain the heads are fully retracted.

4. Place the disk pack onto the spindle

NOTE

A spindle lock mechanism (ratchet brake) is actuated when the disk pack canister cover is on the spindle. A "click" may be heard as the lock mechanism engages. The machanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist the canister handle clockwise until pack is locked in place.

6. Lift the canister clear of the disk pack and set it aside to an uncontaminated storage area.

7. Close the front cover immediately to prevent the entry of dust and the contamination of the disk surfaces.

DISK PACK REMOVAL

1. Press (to extinguish) to operator panel START switch.
2. Check that disk pack rotation has stopped completely.
3. Raise the front cover.

CAUTION

During maintenance procedures the read/write heads are sometimes manually positioned. Make certain that the heads are fully retracted.

4. Place the plastic canister over the mounted disk pack so that the post protruding from the center of the disk pack is received into the canister handle.
5. Twist the canister handle counterclockwise until the disk pack is free of the spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly

6. Lift the canister and the disk pack clear of the spindle.
7. Close the front cover.
8. Place the bottom dust cover in position on the disk pack and tighten it.
9. Store the disk pack in a clean cabinet or on a clean shelf.

HEAD ALIGNMENT CARD (DSFV)

Four LED indicators are provided as monitors to ensure accurate alignment data is taken. Their functions are:

Power - When lighted indicates power is applied to card (card is fully inserted in card slot).

Input - When lighted idnciates amplitude of alignment signal is below minimum threshold required to allow alignment card to operate.

Bad Track - When lighted indicates short duration loss of alignment signal. Indicator lights when polarity (S1) is operated. A one-shot maintains light for four seconds.

Mode - When lighted indicates switches S2 (servo-R/W select) or S3 (meter sensitivity) are not in correct position to measure data head alignment error.

NOTE

Measurement of data head alignment error can be taken only when the power indicator is on and the other indicators are off.

Three toggle switches are provided on the card edge which perform the following functions:

S1 - Switch changes the polarity of the alignment signal and is used in taking measurements of both servo and data heads as follows:

a) note null meter reading in P (normal) position

b) note null meter reading in N (reverse) position

then P-N = alignment position, i.e., P=+30 mv, N=-40 mv(+30)-(-40)=+70 mv alignment error.

S2 - Switch selects the servo head (S) as an input to the card on the data head (R/W) as an input to the card. When switch is in S position, mode indicator will light.

S3 - Switch changes the sensitivity of the meter circuit (TPX and TPY). In X1 position, meter readings are multiplied by 1, in X.1 multiply meter readings by 10. With switch in X1 position, mode indicator lights.

Test points TP-X and TP-Z are connected to the null meter. TP-Y is connected to an oscilloscope to observe the dibit pattern.

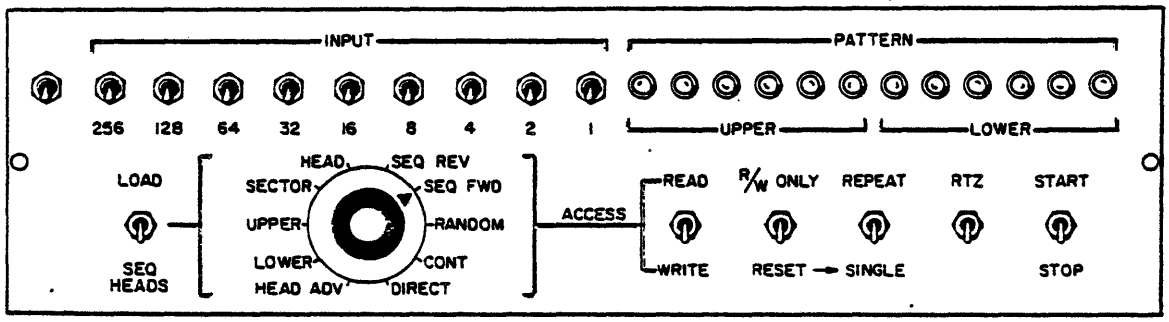
OFF LINE TESTER

The Off Line Tester PN 86073404 permits full control of the drive seek and read/write logic without computer intervention.

The tester front panel is illustrated in Figure 2-2. Switch functions are defined in Table 2-2.

PREPARATION FOR USE

1. Verify that the CPU operating system permits the drive to be removed from computer control.
2. Open cabinet rear door.



NOTES: 1. DATA SYNC JACK IS ON REAR PANEL OF TESTER.

9A18

TABLE 2-2. OFF LINE TESTER SWITCH FUNCTIONS

Switch/Indicator	Mode Select Switch Position	Function
Bits Used		
INPUT All	DIRECT	Loads destination cylinder of seek.
All	CONT	
All	SEQ FWD	Loads length of each forward or reverse incremental seek.
All	SEQ REV	
1-16	HEAD	Loads head to be selected for read/write operations.
1-16	SECTOR	Loads sector to be selected for read operations.
1-32	UPPER	Loads upper six bits of data pattern to be written.
1-32	LOWER	Loads lower six bits of data pattern to be written.
PATTERN Lamps	--	Indicates 12-bit data pattern that has been loaded into tester for write operations.
Mode Select	--	Controls tester mode of operation.
	HEAD ADV	N/A
	LOWER	Loads write data pattern selected by INPUT switches 32 through 1 when LOAD switch is actuated. Pattern is displayed by LOWER PATTERN indicators.

TABLE 2-2. OFF LINE TESTER SWITCH FUNCTIONS (CONT'D)

Switch/Indicator	Mode Select Switch Position	Function
Mode Select (Cont'd)	UPPER	Loads data pattern selected by INPUT swit ches 32 through 1 when LOAD switch is actuated. Pattern is displayed by UPPER PATTERN indicators.
	SECTOR	N/A
	HEAD	Selects head to be used for read/write operations (determined by INPUT switches 16 through 1) when LOAD switch is actuated. NOTE The following switch positions, except DIRECT, are under further control of REPEAT/SINGLE switch. For sequential forward or reverse seeks, do not exceed lengths greater than 255 tracks.
	SEQ REV	Drive seeks in reverse until it reaches cylinder 000; operation then stops. Decrement length selected by INPUT switches.
	SEQ FWD	Drive seeks forward until it reaches cylinder 822 (or address is generated that would exceed 822), then performs direct seek to cylinder 000. Sequence repeats. Increment length selected by INPUT switches.
	RANDOM	Drive continuously seeks forward or reverse to random cylinder. INPUT switches have no effect.
	CONT	Drive continuously seeks from starting cylinder to cylinder selected by INPUT switches.
	DIRECT	Drive seeks once to cylinder selected by INPUT switches.
LOAD/SEQ HEADS SWITCH	LOAD	Data selected by INPUT switches is loaded in tester. When mode select switch is in UPPER or LOWER position. Data selected by INPUT switches is loaded into drive when mode select switch is in HEAD position. Data selected by INPUT switches is loaded into drive.
	NEUTRAL	No data loaded.
	SEQ HEADS	N/A
READ/ACCESS/WRITE SWITCH	READ	Drive reads selected track with selected head after each seek. Cylinder address read from disk is displayed on logic chassis maintenance panel if its DISPLAY SELECT switch is in ADDRESS VERIFY position. If error occurs on compare between address read from disk and current cylinder address, accessing stops. This may be verified by setting DISPLAY SELECT to DSB4: if Bit 8 is lit, (Address Error Fault) has been detected by tester.
	ACCESS (NEUTRAL)	Reading and writing inhibited. Only seeks are enabled.

TABLE 2-2. OFF LINE TESTER SWITCH FUNCTIONS (CONT'D)

Switch/Indicator	Mode Select Switch Position	Function
READ/ACCESS/WRITE SWITCH (Cont'd)	WRITE	NOTE Do not perform write operation with drive's TAG LINE SELECT switch in ADDRESS VERIFY position. Write operation begins at Index and ends at next Index. Drive writes following pattern: 1. Delay of 630 µsec after leading edge of index mark, before Address Segment of track is written. 2. Bit pattern that was leaded into PATTERN display from end of Address Segment to leading edge of index.
R/W ONLY/RESET SWITCH	R/W ONLY	Seeks are inhibited. Refer to REPEAT/SINGLE switch for further information.
	NEUTRAL	Seeks enabled. Refer to READ/WRITE.
	RESET	Resets starting address of single-access continuous seeks (SINGLE and CONT).
REPEAT/SINGLE SWITCH	SINGLE	One operation will take palce each time START/STOP switch is actuated to START. If writing, one seek/write operation is performed. If reading, one seek/read operation is performed. In R/W ONLY mode the following occurs: 1. While reading, selected track is read once per START/STOP switch actuation. 2. While writing, one track is written per START/STOP switch actuation.
	REPEAT	Operation continues until START/STOP switch is actuated to STOP (except, DIRECT mode has only one operation). In READ or WRITE mode, one read or write operation is performed per each seek. In R/W ONLY mode the following occurs: 1. While reading, select track address is continuously read and compared. 2. While writing, track is continuously rewritten.
RTZ Switch	RTZ	Drive performs a return to zero seek operation when RTZ switch is actuated.
START/STOP SWITCH	START	Initiates selected operation. If in SINGLE mode, switch must be actuated for each execution.
	STOPS	Stops operation.

TABLE 2-2. OFF LINE TESTER SWITCH FUNCTIONS (CONT'D)

Switch/Indicator	Mode Select Switch Position	Function
DATA SYNC JACK (Rear of Tester)		Provides scope sync point during read operations. Signal is positive-going at beginning of data pattern (which follows cylinder byte) and drops at end of data field. Because of timing variations and propagation delays between tester, drive, and scope, the first bit of the data pattern may not actuaally be displayed.

3. Set ON LINE/NORMAL/WRITE DISABLE switch to OFF LINE (normal). Tester will not work in ON LINE mode. If operated in WRITE PROTECT mode, accessing and reading are normal, but data cannot be written.

4. Open tester bottom panel and remove cable assembly. If tester has not been used, verify that 12.88 MHz crystal is installed. The 13.60 MHz crystal should be in the dummy jack. Replace cover.

NOTE

DC power supply voltage must be removed when tester is being installed or removed.

5. Connect cable assembly between connectors on rear of tester and C27 on logic rack. Tester receives power from drive. Set START/STOP switch to STOP.

6. Apply DC power.

OPERATING PROCEDURES

Error Detection

The DISPLAY SELECT switch on the logic rack maintenance panel is a valuable accessory in using the tester. A thorough knowledge of this switch and its functions will assist greatly in isolating malfunctions. Functions of each switch position are specified in Table 2-1.

When the DISPLAY SELECT switch is set to ADDRESS VERIFY position, the ADDRESS & CONTROL BUS indicators display the cylinder address read from the disk. This function is enabled only during tester read operations. If any error occurs, all accessing stops and the last address read will be displayed. Proceed as follows:

1. Set DISPLAY SELECT switch to following posiiton to verify the type of error. DSB4, Bit 2^6 displayed indicates that the tester detected an address error: DSB3, Bit 2^7 indicates a seek error; etc. (refer to Table 3-3).

2. Set switch to CYLINDER position to determine the address that the drive should be at.

3. Set switch to DIFFERENCE position to check the contents of the difference counter. When the seek is completed, all bits should be on (which is the complement of zero).

4. If the cylinder and difference are correct, but an address error is indicated, proceed as follows:

   a. Press FAULT switch. Address Error DSB4 2^6 is stored in drive's Fault register. FAULT switch must be pressed to clear that bit.

   b. Select R/W ONLY.

   c. Reread cylinder address.

   d. If ADDRESS VERIFY display matches CYLINDER display, the error is not a positioning error; a read error caused the previous "address error".

5. If CYLINDER and ADDRESS VERIFY cannot be matched, cause of the address error was a positioning error.

While performing sequential forward seeks, and with the DISPLAY SELECT switch set to CYLINDER, the display will increment with each seek.

Seek Operations

The tester is capable of performing the following seek operations:

- Single seek to any cylinder
- Repeated seek between any two cylinders
- Sequential seeks at selectable seek lengths

NOTE

Do not exceed seek lengths greater than 255 tracks.

- Random cylinder seeks

Single Seek

This procedure causes a single direct access to desired cylinder. Precondition tester by setting START/STOP switch to STOP and actuating RTZ switch.

1. Set INPUT switches to desired cylinder number.
2. Set LOAD/SEQ HEADS switch to neutral position.
3. Set mode select switch to DIRECT.
4. Set READ/ACCESS/WRITE switch to ACCESS.
5. Set R/W ONLY/RESET switch to neutral position.
6. Set REPEAT/SINGLE switch to SINGLE.
7. Set START/STOP switch to START.
8. When move is complete, return START/STOP switch to STOP.

Repeated Seek Between Two Cylinders

This procedure causes drive to access between two cylinders. Precondition tester by setting START/STOP switch to STOP and actuating RTZ switch.

1. Perform single seek procedure to desired first cylinder if it is other than track 000.
2. Set INPUT switches to new desired cylinder.
3. Set LOAD/SEQ HEADS switch to neutral.
4. Set mode select switch to CONT.
5. Set READ/ACCESS/WRITE switch to ACCESS.
6. Set R/W ONLY/RESET switch to neutral position.
7. Set REPEAT/SINGLE switch to REPEAT.
8. Set START/STOP switch to START.
9. To stop repeated seeking, place START/STOP switch to STOP.

Sequential Seeks

This procedure causes drive to access sequentially forward, or reverse. The direction is determined by the Mode Select switch, and the incremental cylinder seek length is determined by the setting of the INPUT switches. Precondition tester by setting STOP/START switch to STOP and actuating RTZ switch. If actuator is not at cylinder 000 and a seqential forward seek is initiated, the actuator seeks forward one seek length at a time from current cylinder position until reaching last cylinder or an illegal address. It then returns to cylinder 000 in one movement and continues forward sequential seeks starting at track 000 and at the seek length set by the INPUT switches.

If a sequential reverse seek is initiated, actuator seeks in reverse at the cylinder increment selected by INPUT switches until reaching track 000. The operation is then stopped. A direct seek to a cylinder other than 000 must precede a sequential reverse seek.

For sequential forward or reverse seeks, do not exceed seek lengths greater than 255 tracks. Otherwise seek lengths different from that desired will be obtained. For example, if a seek of 256 is commanded, actuator will seek to: 0, 256, 1, 257, 2, 258, 3, 259, and so on.

If CONT and SINGLE are both selected, actuate RESET if the starting seek address is to be changed. This permits the tester to gate internally the new address selected by INPUT switches. Otherwise, tester will command a return seek to original starting cylinder (stored when operation first started).

Procedure for Sequential Forward Seek:

1. Perform single seek procedure if desired starting position is other than track 000.
2. Set INPUT switches to desired seek length.
3. Set LOAD/SEQ HEADS switch to neutral.
4. Set mode select switch to SEQ FWD.
5. Set READ/ACCESS/WRITE switch to ACCESS.
6. Set R/W ONLY/RESET switch to neutral.
7. Set REPEAT/SINGLE switch to desired mode.
8. Set START/STOP switch to START.
9. If REPEAT/SINGLE switch is set to SINGLE, one seek is made for each START/STOP switch actuation. Return START/STOP switch to STOP when move is complete. If REPEAT/SINGLE switch is set to REPEAT, selected seek operation is continuous until START/STOP is set to STOP.

Procedure for Sequential Reverse Seek:

1. Perform single seek to desired starting track.
2. Set INPUT switches to desired seek length.
3. Set LOAD/SEQ HEADS switch to neutral.
4. Set mode select switch to SEQ REV.

5. Set READ/ACCESS/WRITE switch to ACCESS.

6. Set R/W ONLY RESET switch to neutral.

7. Set REPEAT/SINGLE switch to desired mode.

8. Set START/STOP switch to START.

9. If REPEAT/SINGLE switch is set to SINGLE, one seek is made for each START/STOP switch actuation. Return START/STOP switch to STOP when move is completed. If REPEAT/SINGLE switch is set to REPEAT, actuator will sequentially move to cylinder 000 and stop.

10. Set START/STOP switch to STOP.

Head Selection

1. Select a specific head as follows:

   a. Set mode select switch to HEAD.

   b. Set INPUT switches (16 through 1) to desired head number.

   c. Actuate LOAD/SEQ HEADS switch to LOAD and let return to neutral position. The selected head will be used for all operations.

NOTE

Head register will be cleared automatically after a RTZ step.

Read Operations

Read operations are primarily address-oriented. The tester compares the cylinder address read from the disk with the current cylinder address. If an error occurs, execution stops. Read Gate stays up for the remainder of the track. When comparing cylinder addresses set DISPLAY SELECT switch on maintenance panel to ADDRESS VERIFY.

Panel indicators then display cylinder address read by tester. If performing a repeat read without accessing (R/W ONLY) indicators may appear to be blank. This is because the lamp drivers cannot react fast enough to display data inputs. Display may be obtained by setting START/STOP switch to STOP or performing a single access/read operation.

The data pattern read from the disk is NOT compared with the loaded pattern in the tester. Pattern read errors will therefore not be detected by the tester. If it is necessary to observe read waveforms within drive, connect oscilloscope vertical inputs to desired test points. Sync positive on DATA SYNC jack on tester rear panel. Display is initiated at leading edge of first data bit. Because of timing variations and propagation delays, first bit may be missed so that display starts at second bit.

A read operation can be performed in conjunction with a seek operation or separately. If performed with a seek operation, the seek is completed first, then the track is read.

Read One Track

To read one track perform the following steps:

1. Set READ/ACCESS/WRITE switch to READ.

2. Set REPEAT/SINGLE switch to SINGLE.

3. Set R/W ONLY/RESET switch to NEUTRAL.

4. Select desired head as described in Head Selection procedure.

5. Access to desired track as described in Seek Operations.

6. To read track again, actuate START/STOP switch. Repeat START/STOP step for each read operation.

To select new head on same track without accessing perform the following steps:

7. Set R/W ONLY /RESET switch to R/W ONLY.

8. Select desired head as described in Head Selection procedure.

9. Set START/STOP switch to START. To read that track again, actuate START/STOP switch. Repeat START/STOP step for each read operation.

To read continuous with one head without accessing perform the following steps:

10. Set REPEAT/SINGLE switch to REPEAT.

11. Set START/STOP switch to START. Track will be continuously read until START/STOP switch is set to STOP.

Read More Than One Track

To read more than one track perform the following steps:

1. Set READ/ACCESS/WRITE switch to READ.

2. Set REPEAT/SINGLE switch to REPEAT.

3. Set R/W ONLY/RESET switch to NEUTRAL.

4. Select desired head as described in Head Selection procedure.

5. Select desired seek as described in Seek Operations.

6. Tracks will be continuously read until START/STOP switch is set to STOP.

Read All Cylinders With All Heads

To read all cylinders with all heads use the following procedure:

1. Set READ/ACCESS/WRITE switch to READ.
2. Set REPEAT/SINGLE switch to REPEAT.
3. Set R/W ONLY/RESET switch to NEUTRAL.
4. Select head 00 as described in Head Selection procedure.
5. Set Mode Select switch to SEQ FWD.
6. Set INPUT switches for one track seek.
7. Set START/STOP switch to START. Address will be read on track 000 by head 00, etc. When last track is read switch START/STOP switch to STOP. Repeat test selecting next higher order head and read all tracks. Continue until all heads have read all tracks.

Write Operations

A write operation can be performed in conjunction with a seek operation or separately. If performed with a seek operation, the seek is completed first, then the track is written. The write operation begins at Index and ends at the next Index. The bit pattern loaded into the PATTERN display is written on the track (after a delay of 630 µsec from the leading edge of Index.

Write One Track

To write one track perform the following steps:

1. Set READ/ACCESS/WRITE switch to write.
2. Set REPEAT/SINGLE switch to SINGLE.
3. Set R/W ONLY/RESET switch to NEUTRAL.
4. Load bit pattern as follows:
   a. Set Mode Select switch to UPPER.
   b. Set INPUT switches (32 through 1) to upper six bits of bit pattern.
   c. Actuate LOAD/SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by LOWER PATTERN indicators.
   d. Set Mode Select switch to LOWER.
   e. Set INPUT switches (32 through 1) to lower six bits or bit pattern.
   f. Actuate LOAD/SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by LOWER PATTERN indicators.
5. Select desired head as described in Head Selection procedure.
6. Access to desired track as described in Seek Operations.
7. To write track again, actuate START/STOP switch. Repeat START/STOP step for each write operation.

To select new head on same track without accessing perform the following steps:

8. Set R/W ONLY/RESET switch to R/W ONLY.
9. Select desired head as described in Head Selection procedure.
10. Set START/STOP switch to START. To write that track again, actuate START/STOP switch. Repeat START/STOP step for each write operation.

To write continuous with one head without accessing perform the following steps:

11. Set REPEAT/SINGLE switch to REPEAT.
12. Set START/STOP switch to START Track will be continuously written until START/STOP switch is set to STOP.

Write More Than One Track

To write more than one track perform the following steps:

1. Set READ/ACCESS/WRITE switch to write.
2. Set REPEAT/SINGLE switch to REPEAT.
3. Set R/W ONLY/RESET swi-ch to NEUTRAL.
4. Load bit pattern as follows:
   a. Set Mode Select switch to UPPER.
   b. Set INPUT switches (32 through 1) to upper six bits of bit pattern.
   c. Actuate LOAD/SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by UPPER PATTERN indicators.
   d. Set Mode Select switch to LOWER.
   e. Set INPUT switches (32 through 1) to lower six bits of bit pattern.

f. Actuate LOAD/SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by LOWER PATTERN indicators.

5. Select desired head as described in Head Selection procedure.

6. Select desired Seek as described in Seek Operations.

7. Tracks will be continuously written until START/STOP switch is set to STOP.

Write All Cylinders With All Heads

To write all cylinders with all heads use the following procedure:

1. Set READ/ACCESS/WRITE switch to write.

2. Set REPEAT/SINGLE switch to REPEAT.

3. Set R/W ONLY/RESET switch to NEUTRAL.

4. Load bit pattern as follows:

   a. Set Mode Select switch to UPPER.

   b. Set INPUT switch (32 through 1) to upper six bits of bit pattern.

   c. Actuate LOAD SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by UPPER PATTERN indicators.

   d. Set Mode Select switch to LOWER.

   e. Set INPUT switches (32 through 1) to lower six bits of bit pattern.

   f. Actuate LOAD/SEQ HEADS switch to LOAD and let switch return to neutral. Verify that pattern is displayed by LOWER PATTERN indicators.

5. Select head 00 as described in Head Selection procedure.

6. Set Mode Select switch to SEQ FWD.

7. Set INPUT switches for one track seek.

8. Set START/STOP switch to START. Pattern will be written on track 000 by head 00, then track 001 is written by head 00, etc. When last track is written switch START/STOP switch to STOP. Repeat test selecting next higher order head and write all tracks. Continue until all heads have written all tracks.

SECTION 3

THEORY OF OPERATION

THEORY OF OPERATION 3

INTRODUCTION

The theory of operation is organized into the following 2 parts.

- Subsection 1A - Describes the operation of the power supply and major mechanical assemblies.
- Subsection 1B - Describes the logical functions and the signals exchanged within the Controller.

Functional descriptions are frequently accompanied by simplified logic diagrams. These diagrams are useful both for instructional purposes and as an aid in troubleshooting. Figure 3-1 illustrates the logic symbology used by the illustrations in this manual. The diagrams have been simplified to illustrate the principles of operation; therefore, other elements may be omitted. The logic diagrams in the Maintenance manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The descriptions are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals), and track format (i.e., data records and field organization).

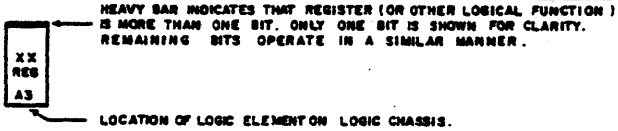
The text will make liberal use of system and drive abbreviations. These abbreviations are listed in Table 3-1.

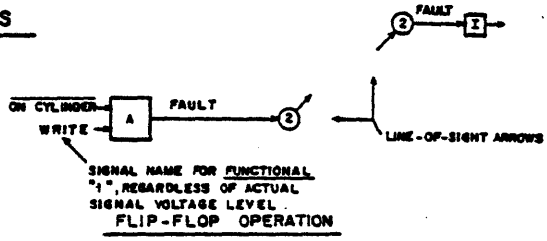
GENERAL INFORMATION

SIMPLIFIED DIAGRAMS IN THIS MANUAL SHOW THE FUNCTIONAL FLOW OF SIGNALS THROUGH THE DRIVE. THE DIAGRAMS HAVE BEEN SIMPLIFIED TO SERVE AS A GUIDE IN TROUBLESHOOTING AND IN UNDERSTANDING DRIVE OPERATIONS. REFER TO THE COMPLETE LOGIC DIAGRAMS FOR ACTUAL TEST POINTS AND SIGNAL LEVELS.

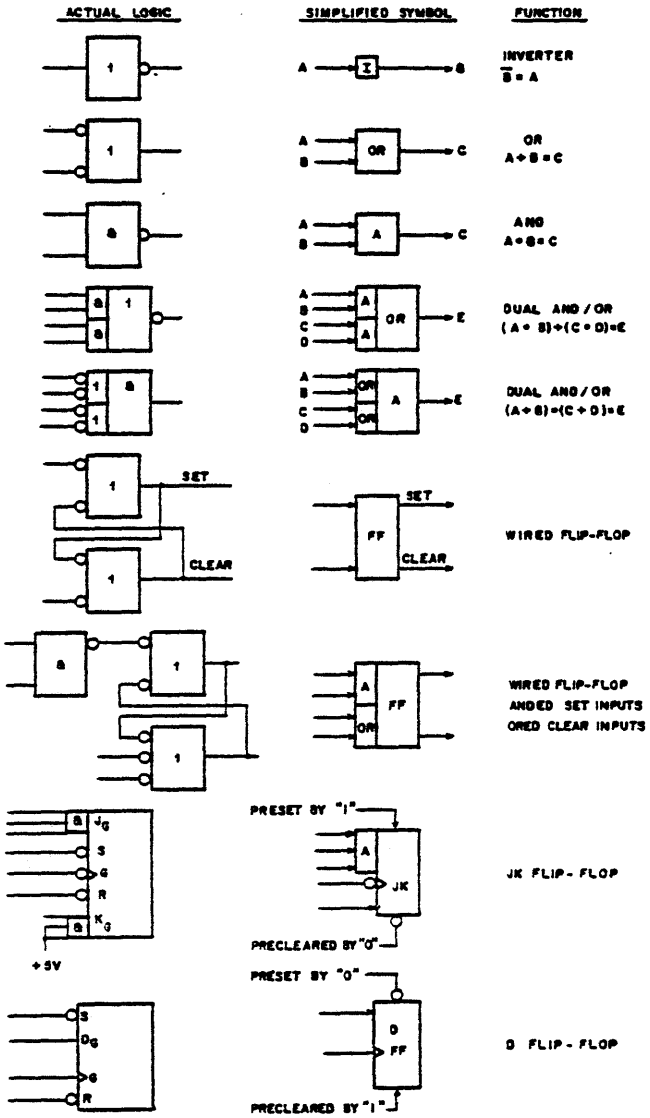
ALL LOGIC IS SHOWN ON POSITIVE LOGIC REPRESENTATION. SIGNAL LEVELS ARE DISREGARDED. ALL SIGNALS ARE NAMED WHEN THE FUNCTION TO BE ACCOMPLISHED REQUIRES A LOGICAL 1, REGARDLESS OF ACTUAL SIGNAL VOLTAGE LEVEL.

SYMBOLS





LOGIC SYMBOLOGY CONVERSION



FLIP-FLOP OPERATION

WIRED FF

FF OUTPUTS ARE COMPLEMENTARY UNLESS BOTH INPUTS RECEIVE SIMULTANEOUS ENABLES. IF SO, BOTH OUTPUTS ARE HIGH ("1").

JK FF

JK FF IS ENABLED (TO CHANGE STATE) BY DYNAMIC TOGGLE. IF CIRCLE IS SHOWN AT TOGGLE, CIRCUIT IS ENABLED BY NEGATIVE-GOING TOGGLE ("1" → "0"). PRESETS AND PRECLEARS DO NOT REQUIRE TOGGLE TO CHANGE STATE.

JK TRUTH TABLE

J	K	BEFORE TOGGLE		AFTER TOGGLE	
		SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

D FF

SAME AS JK, EXCEPT THAT THERE IS NO DATA INPUT TO CLEAR SIDE. FF SETS ONLY IF D INPUT IS "1" WHEN TOGGLE GOES TO "1". IF D INPUT IS "0" AT TOGGLE, FF CLEARS.

7H7

Figure 3-1. Simplified Logic Symbology

TABLE 3-1. ABBREVIATIONS

Abbreviation	Full Name	Abbreviation	Full Name
API	Angular Position In	MSD	Mass Storage Device
ARC	Advance Read Clock	OPI	Operational In
CA	Control Adapter (Controller)	OPO	Operational Out
CIL	Cylinder Address In (Lower)	RCB	Recalibrate
CIU	Cylinder Address In (Upper)	RDH	Read Header
COL	Cylinder Address Out (Lower)	RDM	Reset Diagnostic Mode
COU	Cylinder Address Out (Upper)	RDX	Read
*CYL	Cylinder	*REV	Reverse
DC-	Command Code Lines (0-5,P)	RLS	Release
DCS	Device Command Strobe	RPS	Rotational Position Sensing (error)
DEN	Device Event Notification	RRC	Retard Read Clock
*DIFF	Difference	RTC	Return to Track Centerline
DIN	Device Initialize	*RTZS	Return to Zero Seek
D1-	Bidirectional Data Lines (D10-17,DIP)	SDE	Set Diagnostic Escape
DLI	Device Level Interface	SDM	Set Diagnostic Mode
DM1	Data Modifier Line	SFL	Seek Forward (Lower)
DNR	Device Number Request	SFU	Seek Forward (Upper)
DSB	Detailed Status Byte (Bytes DS1-DS8)	SLS	Set Local State
DTR	Device Type Request	SPI	Shift Position In
*EOT	End of Travel	SPO	Shift Position Out
*FF	Flip-Flop	SRI	Serial Read In
FLT	Fault	SRL	Seek Reverse (Lower)
*FWD	Forward	SRU	Seek Reverse (Upper)
HIL	Head Address In (Lower)	SSR	Summary Status Request
HIU	Head Address In (Upper)	SSS	Set Standby State
HOL	Head Address Out (Lower)	SWO	Serial Write Out
HOU	Head Address Out (Upper)	SZE	Seize Device
IDX	Index Mark	*T	Track
MB	Megabyte	*VEL	Velocity
*MP	Maintenance Panel	WRT	Write
*OP	Operator (Control) Panel		

*NOTE: These are abbreviations for device functions. They are not applicable to the I/O.

INTRODUCTION

This subsection provides physical and function descriptions of the power supply and the major mechanical assemblies. It is divided into the following major areas:

- Power Supply
- Logic Chassis Assembly
- Deck Assemblies
- Blower System
- Disk Pack

POWER SUPPLY

GENERAL

Each drive cabinet has a self-contained power supply accessible by swinging open the logic chassis. The power supply is contained in two locations. The ac portion of the supply, consisting of transformers, rectifiers, triacs, and line filters, is mounted in the lower rear of the drive cabinet. The dc portion of the supply, consisting of rectifiers and filters and the relays for power sequencing, is mounted in the lower portion of the logic chassis. Power supply cooling is accomplished by room air for the ac portion; for the dc portion, cooling air is blown over the chassis from a blower at the front of the drive cabinet.

The power supply has the following onputs:

1. +20Y for power sequencing control.
2. ±20 vdc used by the logic.
3. ±9.7 vdc which, in turn, is regulated to ±5 vdc at the logic chassis.
4. ±46 vdc for use by the voice coil positioner.
5. -16 vdc used to retract the carriage under emergency conditions.

Power distribution and sequencing control are illustrated in Figures 3-2 through 3-4.

AC/DC DISTRIBUTION

Input power is made available to the power supply via the closed contacts of the UNIT POWER circuit breaker. With this breaker closed, the blower motor operates. AC power is available to the remainder of the circuit breakers.

The remainder of the ac distribution occurs when the input voltage is applied to transformer A1T3. An ac voltage of about 24 volts is picked off the secondary and applied to the first seek interlock motor, but application of the voltage to the motor does not occur until the spindle motor is started. Another T3 output is rectified to +20Y volts, which is used as a control voltage within the power system.

With +20Y volts available, A1Q1 is enabled. Solid state switches A1Q1 through A1Q4 effectively operate as relays.

The input applied to pin 1 of these devices is transferred to output pin 2 only if pin 3 has +20 volts on it while pin 4 is grounded. These enables are described in detail in the Power Up Sequence discussion.

With A1Q1 enabled, ac is applied to transformers A1T1 and T2. In the case of T2, four distributative voltages developed across the secondary windings are applied to receiver/filter circuits. The four circuits.(+9.7, -9.7, +20, and -20 vdc) are not adjustable and incorporate no switching device other than circuit breakers for circuit protection. Both polarities of the 9.7v circuit are voltage level regulated and made adjustable to ±5 vdc at the logic chassis.

The voltages developed across A1T1 are applied to rectifier and filter circuits. None of the voltages are adjustable. The actuator power (±46 vdc) incorporates no switching devices other than circuit breakers for protection. The emergency retract power (-16 vdc) uses retract relay K5 to connect or disconnect the emergency retract capacitor to the voice coil. This function is explained further in the Emergency Retract discussion.

LOCAL/REMOTE CONTROL

This applies only to units with power sequence feature.

General

The power on and off sequence of drives having the power sequence feature can be controlled either locally or remotely depending on the setting of the drive LOCAL/REMOTE switch. When this switch is set to LOCAL, the sequences are inititated at each drive. When the switch is set to REMOTE, the sequences are initiated only at the first drive in the power sequence cable daisy chain. This daisy chain consists of I/O cables (in addition to the A and B cables) that sequentially route the Pick and Hold power sequence signals to each drive in the subsystem.

The LOCAL/REMOTE switch is located on the power supply control panel and controls the mode of operation by determining how the drive remote start relay (K1) is energized and deenergized. This relay works in conjunction with the drive START switch to control the power on and off sequences.

Figure 3-1.1 shows the LOCAL/REMOTE power sequencing control circuits. The operation of these circuits in both local and remote modes is explained in the following paragraphs.

Local Control

When the drive is in local mode, the remote start relay (K1) energizes whenever +20 volts is available. In this mode, the power on sequence (see figure 3-1.2) begins when the START switch is pressed to light the indicator (providing all circuit breakers and interlocks are closed). The power off sequence is initiated by pressing the START switch to turn off the indicator.

Remote Control

In the remote mode, the start of the power on sequence is controlled by the Sequence Power (K5) and Remote Start relays as well as the START switch. Here, even of the START switch is pressed (to light the indicator), the sequence does not begin until both relays are energized. The Sequence Power relay (K5) energizes when all circuit breakers are closed. With K5 energized, the Remote Start relay (K1) energizes to start the power on whenever the Pick signal goes low (see figure 3-1.1).

Therefore, if the START switch is on and the circuit breakers are closed, the Pick signal determines when the power on sequence begins. In a system where the Pick lines are connected in a daisy chain, the drives power up sequentially, starting with the first drive. A sequential power up occurs because each drive waits until its spindle is up to speed (K2 energizes) before passing the Pick signal to the next drive in the chain.

Only the drives in the remote mode with their START switches on (lighted) are involved in the power up. Drives in local or with their START switches off (not lighted) are not involved in the power up. A drive that is not involved passes the Pick signal to the next drive without delay providing its circuit breakers are open thus deenergizing K5.

The Pick signal originates either at the controller or a plug connecting to the I/O panel of the first drive in the daisy chain. (the plug keeps the Pick signal permanently low) with the Pick signal low, the first drive begins ite power up sequence whenever its START switch is pressed)providing all

breakers and interlocks are closed). When the spindle of the first drive gets up to speed and the Speed relay (K2) energizes, the Pick signlas go to the next drive. This sequence is repeated until all drives in the remore mode with their START switches on are powered up.

Once the Remote Start relay (K1) has been energized, the Hold signal keeps it energized even if the Pick signal goes inactive, (Hold like Pick, may orginiate wither at the controller or the first drive). This allows powering down drives in the chain without affecting other drives.

POWER ON SEQUENCE

Power application to the unit is sequenced by logic and by relays within the power supply. Refer to Figures 3-2 through 3-4.

When the circuit breakers are closed, ac and dc power is enabled. As the +5V power comes up, Power Up Blanking acts as a master clear to the logic. Controller issuance of an SSR command will result in a Device in Standby and Positioner Busy status response. OPI is available if Online mode is selected by the switch on the maintenance panel.

With a pack installed and all interlocks closed, the unit may be powered up. (on units with power sequence feature K1 must also be energized) Pressing the START switch on the control panel has the following effects:

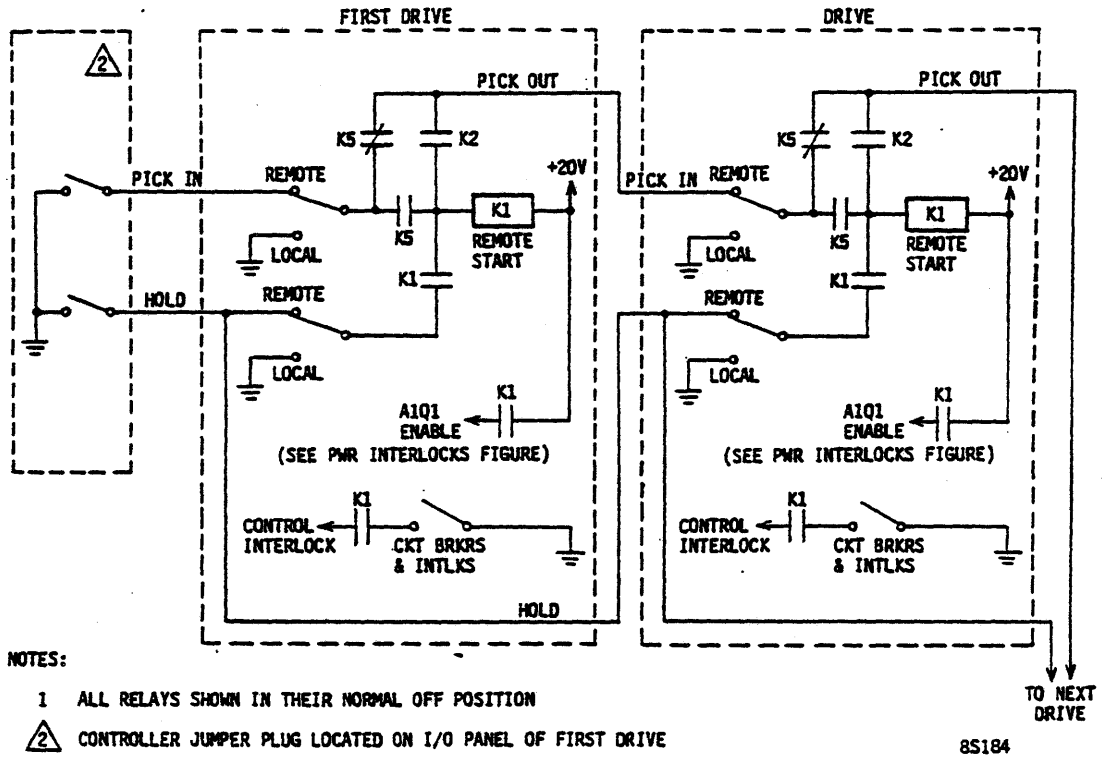


Figure 3-1.1 Local/Remote Power Sequencing Control Circuits

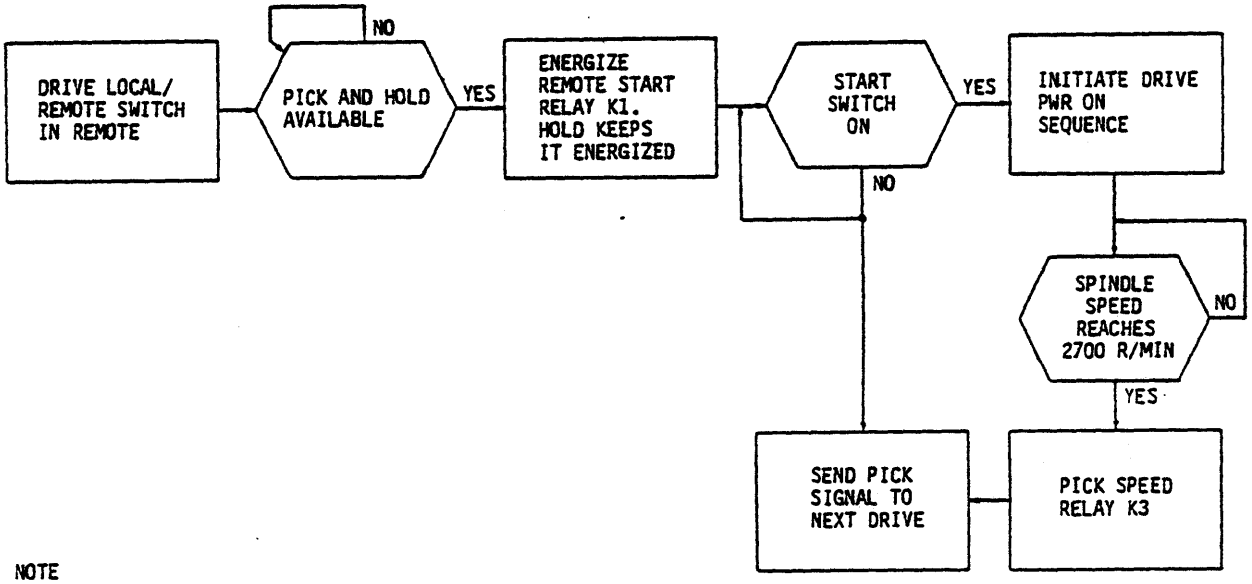


Figure 3-1.2 Remote Mode Power Sequencing

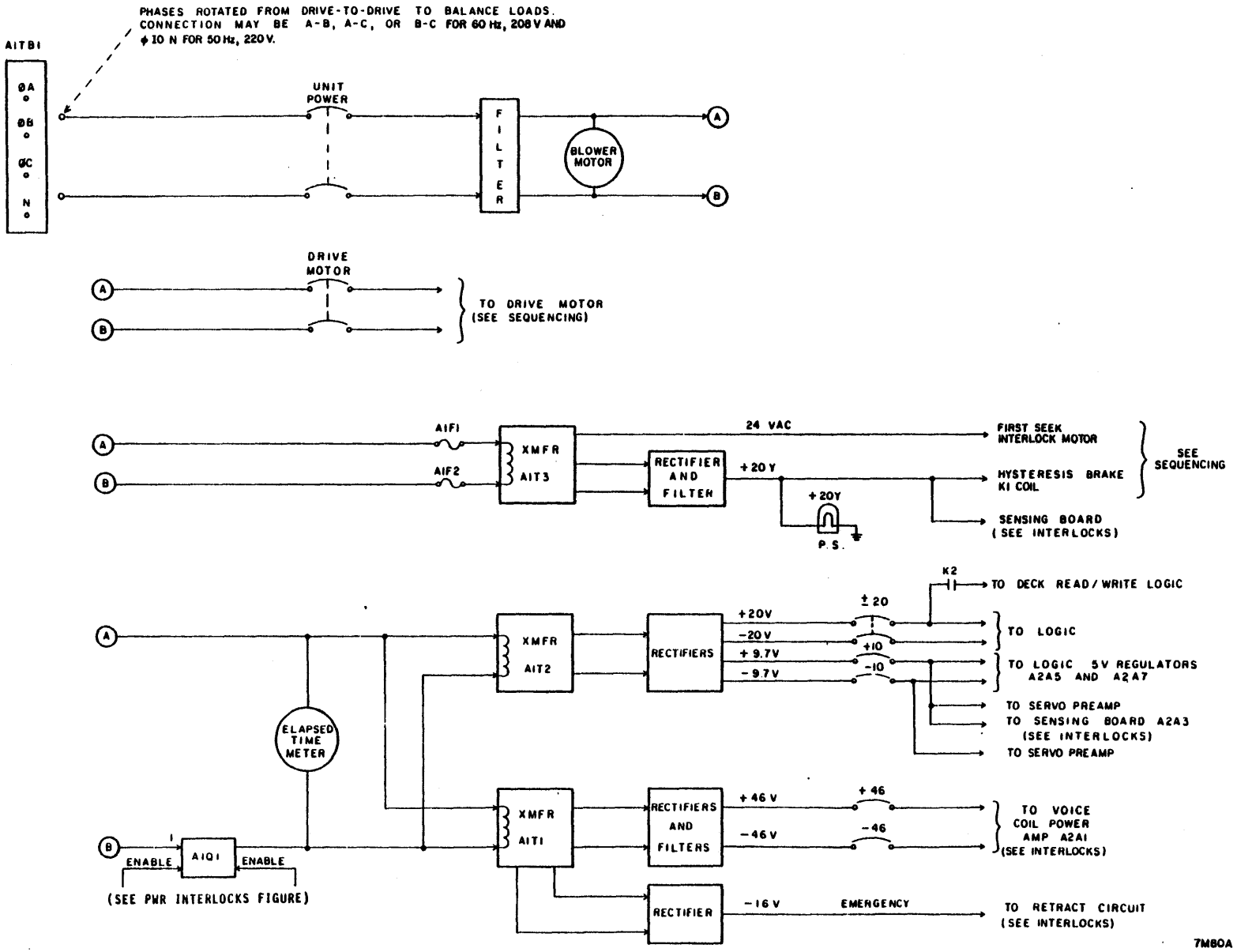


Figure 3-2. Power Distribution

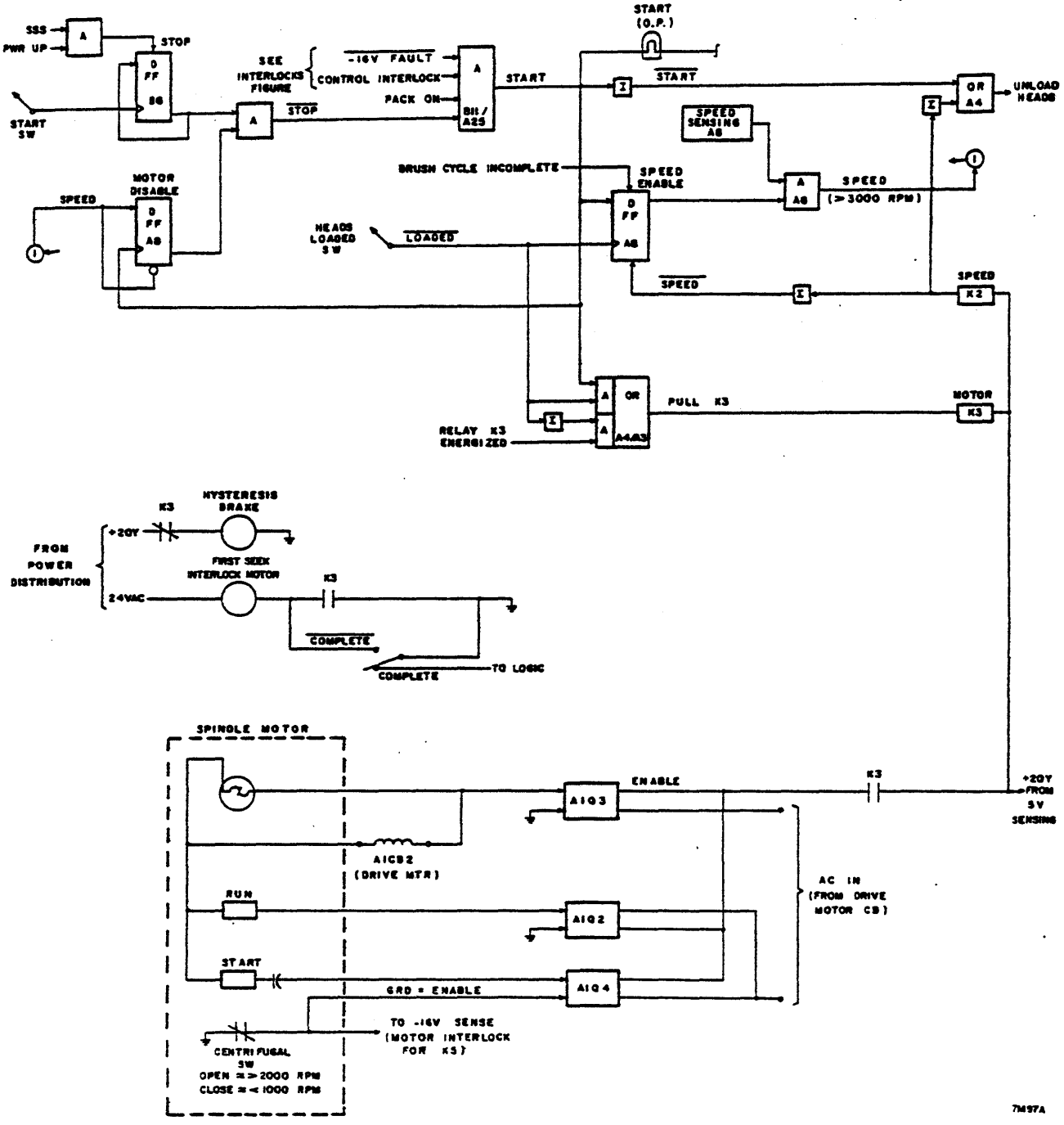


Figure 3-3. Power Sequencing

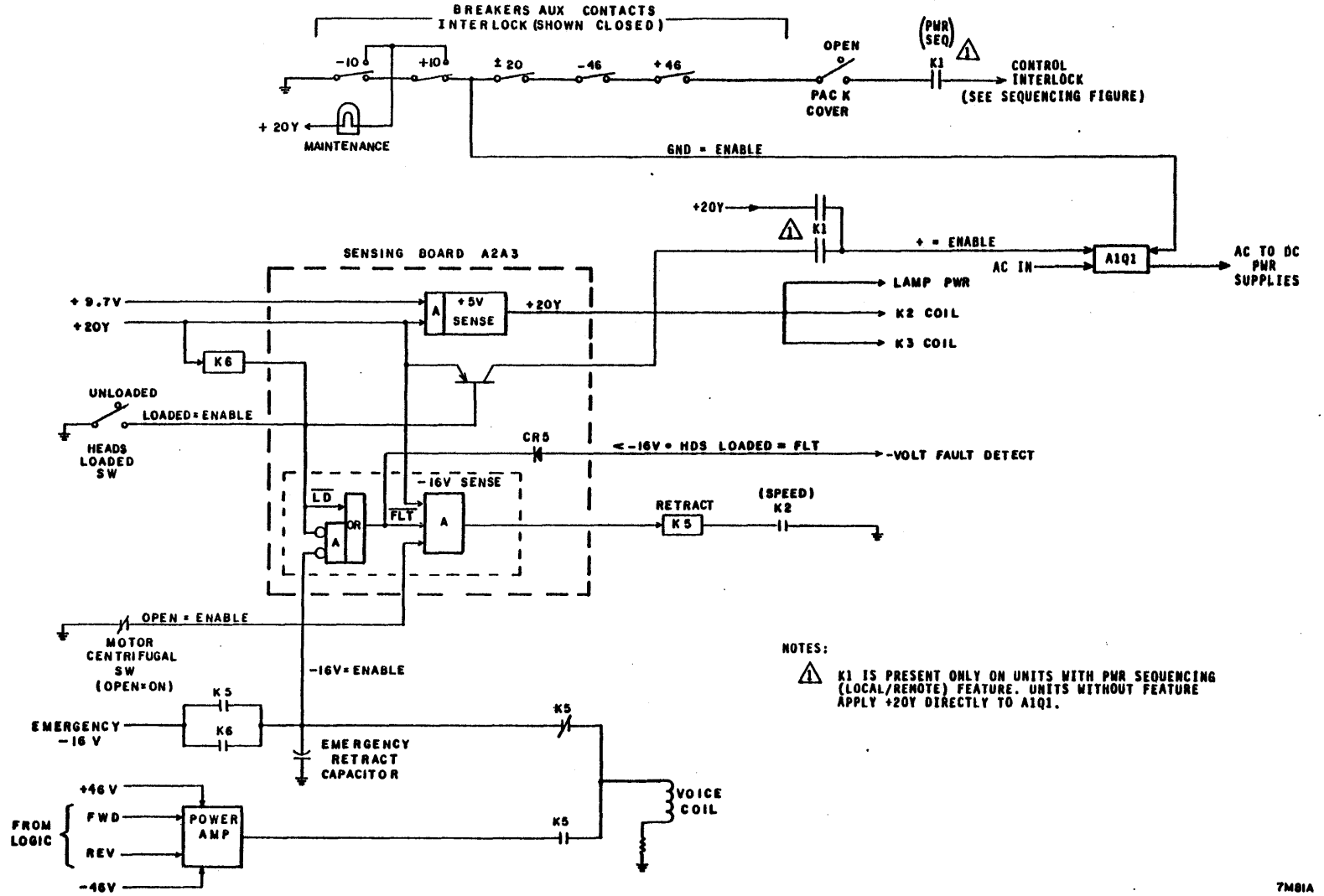


Figure 3-4. Power Interlocks

1. The Stop FF (Figure 3-3) is cleared. It was set previously by dc power up, a Set Standby State command, or by a previous pressing (to extinguish) to START switch/indicator.

2. The logic provides an enable (Figure 3-3) to energize Motor relay K3.

3. The closed contacts of K3 cause the following:

   a. +20 volts enables solid state switches A1Q2, A1Q3, and Q1Q4. These switches can now conduct ac power to the spindle motor.

   b. Because the motor is stopped, the centrifugal switch inside the motor is closed. This provides a ground enable to A1Q4 to connect the start winding and capacitor to ac power. At 2000 rpm the switch transfers to open, disconnecting the start winding and enabling the run winding.

   c. Apply GND to the first seek interlock motor. The first seek interlock switch transfers to the not complete (in progress) position.

   d. Removes power from the hysteresis brake.

4. When the logic determines that the spindle speed exceeds 3000 rpm and the first seek interlock delay is complete, relay K2 energizes.

5. With relay K2 closed

   a. +20 vdc distributed to the read/write logic

   b. Retract relay K5 energized (Figure 3-4).

6. The transferring contacts of K5 cause the following:

   a. Disconnects the emergency retract capacitor from the voice coil while connecting it to the -16v power supply to allow it to charge to -16 volts.

   b. Connects the power amplifier A2A1 to the positioner so that the logic may control the positioner.

7. The first seek interlock switch mechanically transfers to the complete position upon completion of the interlock motor revolution (15 seconds for first seek delay). This removes the remaining ground to the interlock motor to disable it. It also signals load heads to the logic.

8. Completion of the first seek delay allows the start of the First Seek (load heads) function. The logic commands the positioner to move the carriage forward. Refer to the First Seek discussion for further information.

9. When the heads move into the pack, the heads loaded switch closes. This causes the following:

   a. Provides a control signal to the logic for further loading/unloading sequencing.

   b. Maintains a motor relay K3 enable so that the motor continues to operate if the control interlock opens. This prevents the motor from being shut down until the heads are unloaded.

   c. Energizes relay K6. If any condition occurs where Retract relay K5 opens, K6 continues to apply -16v retract voltage to the voice coil until the heads unload.

   d. Enables the -16v Sense circuit. If the -16v power becomes insufficient (loss of power), fault is set and Retract relay K5 opens. Relay K5 connects the retract voltage to the voice coil while removing logic control of the voice coil.

EMERGENCY RETRACT AND DATA PROTECTION

Certain emergency conditions could occur which require immediate disabling of the write circuits and full retraction of the heads. These conditions are:

1. Loss of ac power, either site power or UNIT POWER circuit breaker.

2. Opening of any of the control interlocks (Figure 3-4).

3. Overheating of spindle motor, If this occurs, the spindle motor thermostat (Figure 3-3) opens: this applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. Loss of speed (step 4) occurs.

4. Loss of spindle motor speed.

5. Loss of any of the following ac voltages: +20Y, ±9.7, or -16.

If any of these conditions occur, the read/write logic is disabled and the heads are unloaded. Refer to Figure 3-5 for timing of these conditions.

LOSS OF AC POWER

The following events occur upon catastrophic loss of the ac power or opening of either 5v circuit breaker.

1. All dc power supplies drop their outputs to zero and the logic is disabled.
2. All relays open.
3. With K5 open, the normally-closed contacts of K5 (Figure 3-4) provide a path from the emergency retract capacitor A2C2 to the voice coil. This negative voltage pulls the carriage back to its retracted stop.
4. With K2 open, +20 vdc is removed from the read/write logic.

When power is restored, drives without the power sequence feature and drives with this feature and in local mode are restarted by pressing the START switch. Drives with the power sequence feature and in remote mode, automatically restart when power is restored.

CONTROL INTERLOCK OPENING

If the control interlock (Figure 3-4) opens, the heads unload normally as explained in Power Off Sequence. Pressing START to extinguish the indicator opens the interlock to initiate the normal unload heads sequence. There are certain special emergency sensing conditions:

1. If either the +10 or -10 circuit breaker opens, A1Q1 (Figure 3-2) is disabled. The effect is the same as if all ac power were lost. All ac power input to the dc power supplies is opened except to +20Y.
2. Opening a 20v circuit breaker generates an undervoltage condition to light the CHECK indicator.
3. Opening of any other circuit breaker or interlock breaks the control interlock.

All of these conditions extinguish the START indicator and unload the heads. Any undervoltage condition (±20v or ±5v) sets the Pack Unsafe FF and lights the CHECK indicator.

LOSS OF SPEED

If the spindle motor speed drops below 2700 rpm, the following events occur:

1. The speed detection circuit in the logic detects the speed loss and opens Speed relay K2. As a backup circuit, when the speed is less than about 2000 rpm, the motor centrifugal switch closes. This breaks the gate in the -16v sense circuit (Figure 3-4) to open K5 and energizes K4 to start a new first seek interlock time delay.
2. With K2 open:
   a. K5 opens to apply -16v retract voltage to the voice coil.
   b. +20 vdc power is removed from the read/write logic.
3. Relay K3 is de-energized when speed drops below 2700 rpm.
4. Relay K6 remains energized to continue to apply -16v retract voltage until the heads retract sufficiently to open the heads loaded switch.

LOSS OF DC POWER

If +20Y power is lost, all relays open and the ac input to the dc power supplies is opened. The effect is the same as if all ac power were lost.

If +9.7v is insufficient, the following occur:

1. Relays K2 and K3 are opened by the +5v Sense circuit.
2. With K2 open:
   a. K5 opens to apply -16v retract power.
   b. +20v power removed from read/write chassis. With the heads still loaded, the write circuit generates a Current Fault.
3. With K3 open:
   a. The spindle motor is disabled.
   b. The hysteresis brake is energized.
4. In addition the undervoltage condition will light the CHECK indicator and raise DSB2 bit 2^0. The condition must be cleared to load heads again.

If -16v power is lost, the following occur:

1. The -16v Sense circuit opens K5. It also generates an undervoltage fault condition to set the PACK UNSAFE FF and open One Start Interlock (Figure 3-3).
2. With K5 open, retract power is applied to the voice coil. Since the undervoltage fault has disabled the read/write logic, the circuit is disabled prior to carriage retraction.
3. Relay K5 remains energized, so the drive motor continues to run. Heads cannot load until the CHECK indicator is cleared.

POWER OFF SEQUENCE

The normal power off sequence begins when the controller issues an SSS command, the START switch is pressed, or in units with the power sequence feature of the Pick and Hold signals go inactive. Sequencing is then as follows (see Figures 3-3 and 3-5):

1. The Stop FF sets. This raises an Unload Heads command within the logic. This sets the RTZ Latch which, in turn, causes the carriage to retract at 7 ips.
2. When the heads unload:
   a. Relay K3 de-energizes.
   b. The speed detection circuit is disabled to de-energize relay K2.
3. With K3 open:
   a. The spindle motor is disabled.
   b. Power is applied to the hysteresis brake.
4. With K2 open:
   a. +20v removed from read/write logic.
   b. Relay K5 opens. The emergency retract capacitor discharges through the voice coil to pull it back against its retracted stop.

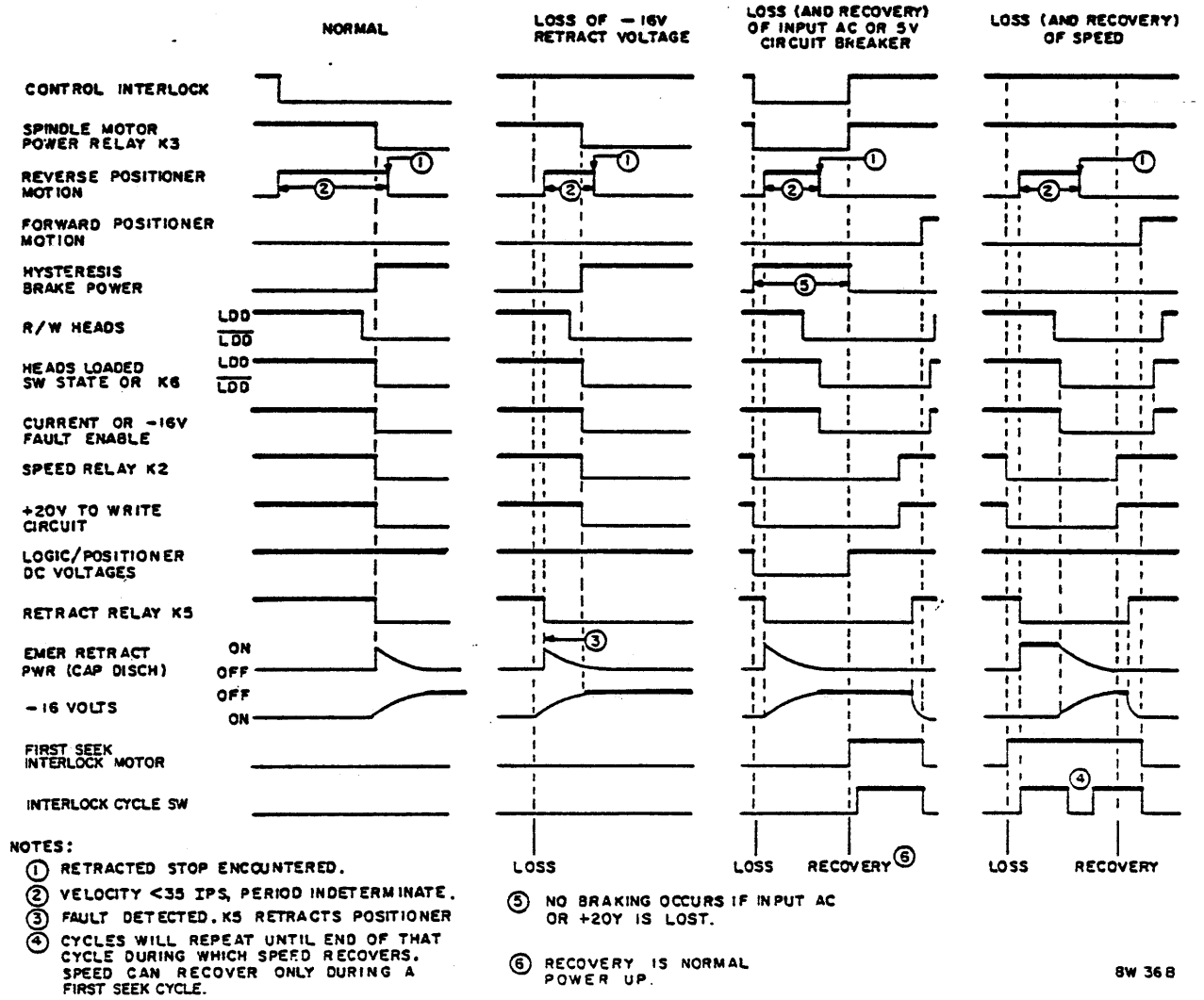


Figure 3-5. Power Off Timing

LOGIC CHASSIS ASSEMBLY

The logic chassis assembly consists of a wire wrap board, logic cards, Maintenance panel, air plenum and dc power supply. The entire assembly forms the rear door to the cabinet. Flexible tubing from the blower assembly connects to the air plenum and provides air to cool the logic cards and the dc power supply.

The logic cards are installed on the protruding pins of one side of the wire wrap board. Wiring between cards and to and from the logic chassis occurs at the protruding pins on the opposite side of the wire wrap board. Access to this wiring is gained by releasing two 1/4-turn fasteners at the top of the door and removing the outer surface of the rear door.

The logic card section contains the bulk of the logic cards used in the cabinet (five cards are located on the deck assembly). The vertically mounted cards are installed in four rows (A top row and D bottom row) at numerically identified locations.

Some cards span two rows and are referred to as full-size cards. Others span a single row and are called half-size cards. Refer to the Diagrams section of the Maintenance manual for a description of the logical functions performed by the cards. The Logic Card manual provides a physical description of the cards. The Wire Lists section of the Maintenance manual contains a tabulation of the wire wrap connections made in the chassis.

The test point panel at the top of the logic chassis provides a convenient point to measure the dc voltages. At the bottom of the logic chassis assembly, and on the front panel of the dc voltage section of the power supply, are located the LOCAL/REMOTE switch, the indicator for +20Y power and the circuit breakers for ±46v, ±20v, and ±10v. Specific information on each control or indicator on the test point and dc power panel is provided in the Operation section of this manual.

ME Maintenance panel contains a set of test point jacks, switches and indicators that relate to the operational status of the drive. These components function primarily in the maintenance mode as a troubleshooting aid. Specific information on each control or indicator is provided in Section 2 of this manual.

DECK ASSEMBLY

GENERAL

The deck assembly mechanism (Figure 3-6) drives the disk pack and loads and positions the read/write and servo heads. The deck assembly consists of a drive motor, hysteresis brake, spindle, actuator, two transducers, and a first seek interlock assembly.

DRIVE MOTOR

The drive motor drives the spindle assembly. The motor is a 3/4-hp unit of the induction type. The motor is secured to a mounting plate. The motor mounting plate is secured to the underside of the deck plate in such a manner as to allow control of belt tension. Power is transferred to the spindle via a flat, smooth-surfaced belt that threads over the pulleys of the spindle and drive motor. Two idler springs maintain a constant tension on the motor mounting plate to keep the belt tight.

A second pulley on the drive motor shaft links the motor (via a V-belt) to the hysteresis brake.

The temperature of the drive motor is monitored by an internal thermostat. If the motor overheats, the thermostat opens. This applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. The result is a speed loss (refer to Power Supplies). The DRIVE MOTOR circuit breaker must be reset to ON to restore operation.

HYSTERESIS BRAKE

The hysteresis brake decelerates the drive motor during a Power-Off sequence (refer to Power-Off sequence paragraph). The brake is energized whenever Motor relay K3 is de-energized. The brake mounts on a plate which, in turn, is mounted on the motor mounting plate. The brake and motor shafts are linked via a V-belt and a pulley on each shaft.

The brake consists of two concentric permeable bodies. These cylinders are assembled, one inside the other, with a uniform gap separating the outer diameter of one from the inner diameter of the other. These adjacent surfaces are machined to contain a series of pole faces. A permanent magnet, in the shape of a cup, fits in the gap to separate the cylinders. This cup is connected to the brake shaft. As long as spindle motor power is applied, brake power is not available and the cup is driven at the speed of the motor. When spindle motor power is removed, braking power is applied.

A flux field is created between the inner and outer cylinder pole faces as braking voltage (+20 volts) is applied to the inner cylinder. The flux field sets up what is in effect magnetic friction between the inner cylinder and the cup, causing the cup (and brake shaft) to decelerate. Brake deceleration in turn causes spindle motor deceleration.

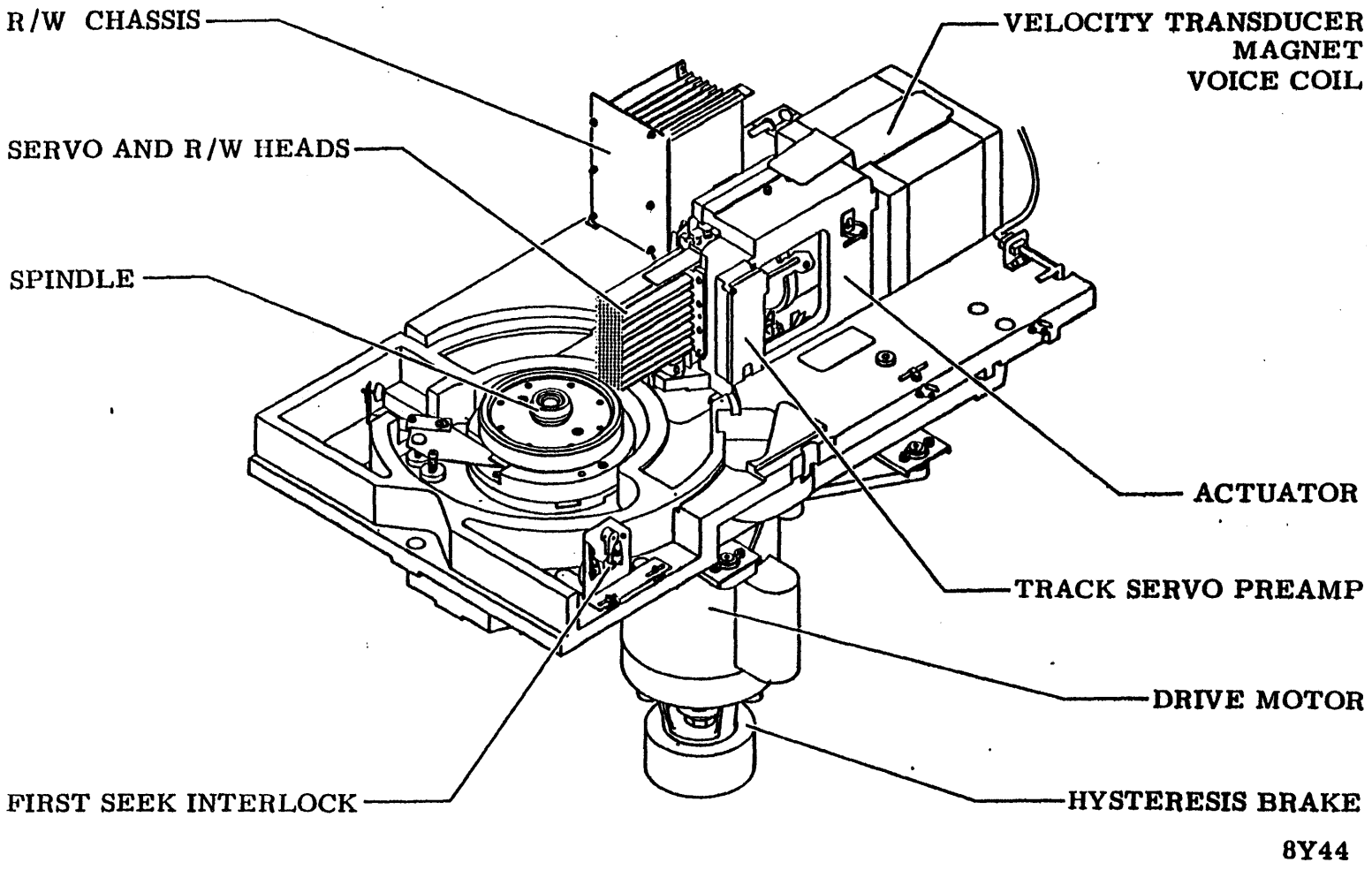


Figure 3-6. Deck Assembly

SPINDLE ASSEMBLY

The spindle assembly is the physical interface between a drive and a disk pack. The surface of the pack mounting plate (Figure 3-7) mates directly with the center of the disk pack.

A vertically free-floating lockshaft runs through the center of the spindle assembly. The upper end of the lockshaft contains internal threads that engage the external threads of a stud projecting from the disk pack. When the disk pack canister cover handle is rotated clockwise, the spring-loaded lockshaft is pulled upward and the disk pack is pulled down. As a result, the mating surfaces of the disk pack and spindle are engaged by a force of approximately 325 pounds. When the disk pack is fully engaged, a release mechanism in the canister handle frees the canister from the disk pack.

The spindle is locked by the pack canister when installing or removing a disk pack. This makes it easier to install or remove a disk pack by preventing spindle rotation.

The pack on switch and ground spring (Figure 3-7) are mounted at the lower end of the spindle assembly. The ground spring is mounted so that it is always in contact with the lockshaft to bleed off any accumulation of static electricity on the spindle to the deck through a ground strap. The pack on switch contacts transfer in response to the vertical movement of the lockshaft. When the shaft is up (disk pack mounted), the contacts are closed. When a pack is not installed, the shaft moves downward to deflect the switch actuator and transfer the contacts. The switch is part of the interlock that inhibits spindle motor power to an improperly configured unit.

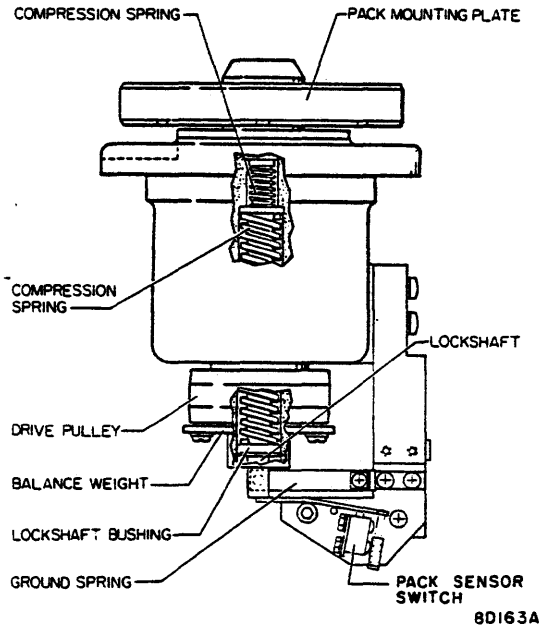


Figure 3-7. Spindle Assembly

ACTUATOR

The actuator consists of the carriage, actuator housing, and magnet assembly. The actuator (Figure 3-8) is the device that supports and moves the read/write and track servo heads. The forward and reverse moves of the carriage on the carriage track are controlled by a servo signal. The basic signal is developed in the logic section and processed by a power amplifying stage in the power supply. The power amplifier output is applied to the voice coil positioner (part of carriage). The signal causes a magnetic field about the voice coil positioner. This magnetic field reacts with the permanent magnetic field existing around the magnet assembly. The reaction either draws the voice coil into the permanent magnet field or forces it away. Signal polarity determines the direction of motion, while signal amplitude controls the acceleration of the motion.

The voice coil positioner is a bobbin-wound coil that is free to slide in and out of the forward face of the magnet assembly. Fastened to the positioner is a head/arm receiver which holds the 19 read/write heads and the single track servo head. The head/arm receiver mounts on the carriage and bearing assembly that moves along the carriage track on eight bearing type rollers. Movement of the positioner in or out of the magnet causes the same motion to be imparted to the entire carriage assembly. This linear motion is the basis for positioning the read/write and track servo heads to a particular track of data on the disk pack. (Refer to Head Loading paragraph for detailed information on read/write head loading and unloading.)

The positioning signal is derived in the logic chassis and power supply. The signal is applied to the voice coil positioner via two flexible, insulated, metal straps, the ends of which are secured to the cam mount and the carriage and bearing assembly.

During any Seek operation, the logic must be informed of the current location and velocity of the carriage. This information is provided by the velocity transducer in the magnet assembly and the lone track servo head installed on the head/arm receiver. The transducer is a two-piece device, one piece stationary and the other movable. Refer to the Transducers paragraph for a complete description.

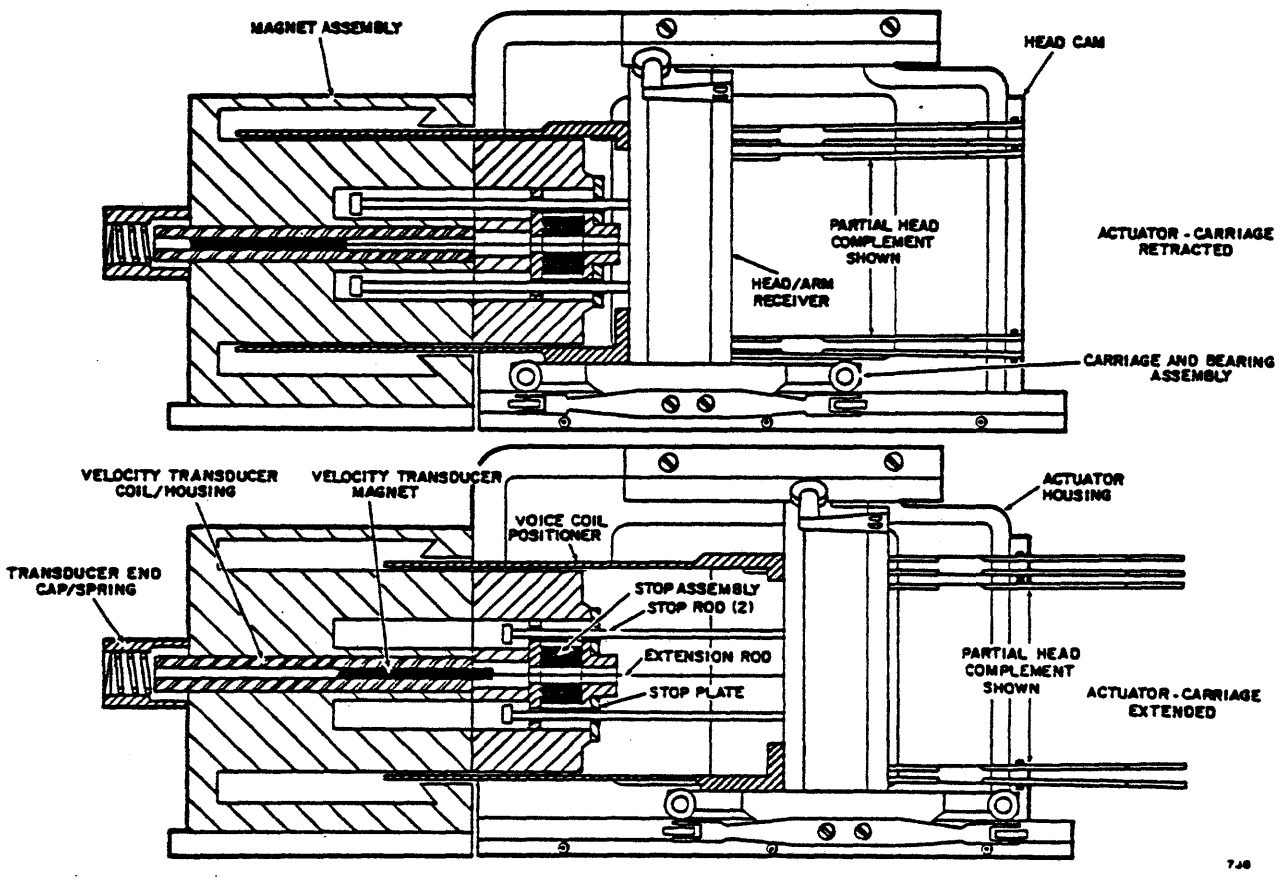


Figure 3-8. Actuator Assembly Elements

The actuator contains a stop mechanism to limit extremes in forward and reverse movement. The stop assembly is a rubber cylinder sandwiched between two metal plates. If the carriage moves too far toward the disk pack, the stop rod heads contact the plate on the magnet-side of the rubber cylinder. If the carriage is retracted far enough away from the disk pack, the rear of the head/arm receiver contacts the stop assembly stud protruding through the stop plate.

Head Loading

The read/write heads must be loaded to the disk surfaces before exchanging data with the controller. The heads must be removed (unloaded) from this position and driven clear of the disk pack either when power is removed from the unit or when the disk pack velocity falls below about 2700 rpm. The actuator components involved in these operations are identified in Figure 3-9.

Head loading amounts to allowing spring pressure of the floating arm (part of head/arm assembly) to move the aerodynamically shaped head face toward the related disk surface. When the cushion of air that exists on the surface of the spinning disk is encountered, it resists any further approach by the head. Spring pressure is designed to just equal the opposing cushion pressure (function of disk pack rpm) at the required height. As a result, the head flies. However, if the spring pressure exceeds the cushion pressure (as would happen if the disk pack lost enough speed), the head stops flying and contacts the disk surface. This could cause damage to the head as well as the disk surface.

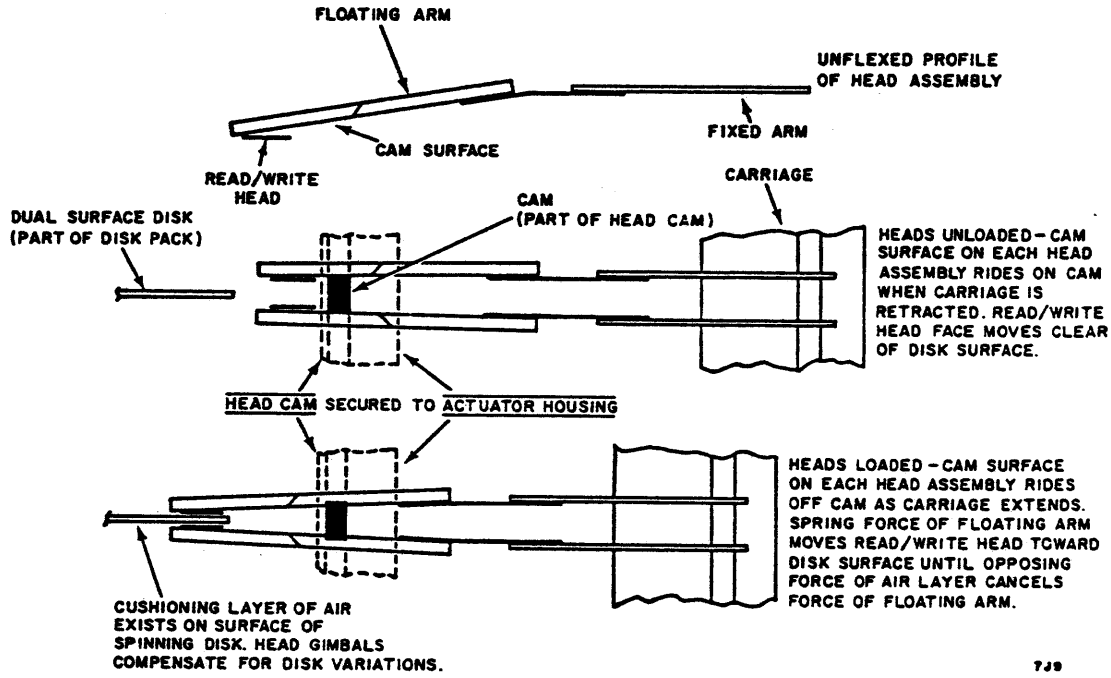


Figure 3-9. Head Loading

To prevent damage to the heads and/or the disk pack during automatic operation, loading occurs only after the disk pack is up to speed and the heads are over the disk surfaces. For the same reason, the heads unload automatically and are retracted if the disk pack rpm drops out of tolerance. During manual operations, heads should never be loaded on a disk pack that is not rotating. Head loading is part of the Power On/First Seek function. As power to the deck is sequenced up, the drive motor starts. This initiates disk pack rotation and a first seek interlock delay. Actual delay is approximately 15 seconds.

When the disk pack rpm reaches 3000, the power supply speed relay energizes to establish the ability to continue the operation. Upon completion of the first seek interlock delay, the logic specifies a forward seek and the carriage moves forward toward track 0. Head loading occurs during this forward motion. The carriage continues toward the spindle until the servo detects track 0.

The floating arm (Figure 3-9) is designed to maintain a constant loading force. While the heads are retracted, head cams on the actuator housing bear against the floating arm cam surfaces. The cams support the loading force and hold the heads in unloaded position. As the carriage moves forward, the floating arm cam surface rides off the head cam just after the read/write heads move out over the disk surface. The loading force moves the head face toward the air layer on the surface of the spinning disk until the opposing forces balance.

The heads loaded switch status reflects the state of the read/write heads (loaded or unloaded). This status is used in the logic chassis and power supply. The switch mounts on the carriage track and is transferred by carriage motion. Whenever the carriage is fully retracted, the switch state reflects the unloaded status of the heads. As the carriage moves forward during a Power On/First Seek, the switch transfers at a point within about 0.1 to 0.2 inch forward of the retracted stop. This switch status remains unchanged until the carriage is retracted to the same position and, as such, does not precisely indicate the loaded/unloaded status of the heads. Precise status is determined by the logic when the servo track head senses dibits.

Head unloading occurs whenever power to the unit is removed or disk pack rpm drops below tolerance. Either event drops a speed enable signal to the logic. This causes the voice coil to drive the carriage in reverse from its current location toward the retracted

stop. (Either normal or emergency methods can be used. Refer to Power Off Sequence paragraph for additional information.) As the carriage retracts, the cam surfaces encounter the head arms and each head rides vertically away from the related disk surface. The carriage continues back to the retracted position and stops.

Head/Arm Assemblies

Twenty head/arm assemblies are mounted on the carriage. A read/write head/arm assembly consists of a read/write head assembly mounted at the end of a supporting arm structure. A track servo head/arm assembly consists of a read coil head assembly mounted at the end of a supporting arm structure.

The head assembly (Figure 3-10), which includes a cable and plug, is mounted on a gimbal ring which, in turn, is mounted on a floating arm. This method of mounting allows the head assembly to pivot (independent of the arm) tangentially and radially relative to a data track on the disk surface. Such motion is required to compensate for possible irregularities in the disk surface.

The arm structure consists of a floating arm secured to a heavier fixed arm. The end of the fixed arm opposite the head mounts in the carriage receiver. The floating arm is the mounting point for the head and is necessarily flexible so that it can flex during load and unload motions, onto and off of the cam surfaces.

Freedom and mobility of the head are necessary elements to being able to function with interchangeable disk packs. During head loading, each floating arm is driven off the related cam and unflexes to force a head toward the air cushion on the spinning disk surface. The force applied by the floating arm causes the heads to fly or float on the air cushion. Vertical motion by a disk surface (due to warpage or imperfection) is countered by a move in the opposite direction by the gimballed head and/or floating arm. As a result, flight height remains nearly constant.

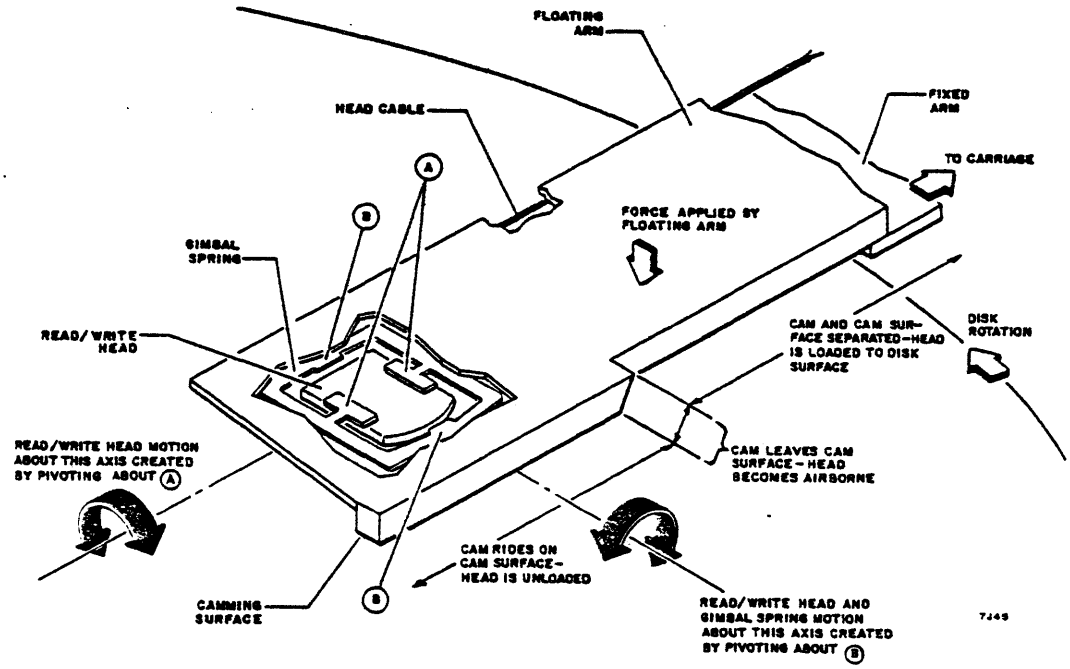


Figure 3-10. Head/Arm Assembly Motion

TRANSDUCERS

The deck assembly contains two transducers: speed sensing transducer and velocity transducer. These transducers provide signals that are used by the logic chassis and the controller to generally control the progression of most machine operations.

Speed Sensing Transducer

The speed sensor (Figure 3-6 and 3-11) generates a voltage output whenever a ferrous material (steel pin set in spindle pulley) enters the magnetic field surrounding the pole piece at the pickup end of the transducer. The logic then shapes this signal into a 55 microsecond pulse. As long as the speed exceeds 3000 rpm, one of these pulses will be sensed at least once each 20 ms. A sensing circuit within the logic monitors the pulse repetition rate and provides an enable to Speed relay K2.

If speed is insufficient, the pulse repetition rate is reduced accordingly. This has either of two effects:

1. If the heads are not loaded, K2 cannot energize and the logic will not initiate the load sequence.

2. If the heads are already loaded, K2 opens, thereby opening the coil of Retract relay K5. The voice coil is disconnected from the logic power amplifier and connected to the -16v emergency retract capacitor. The heads immediately are unloaded to the retracted stop.

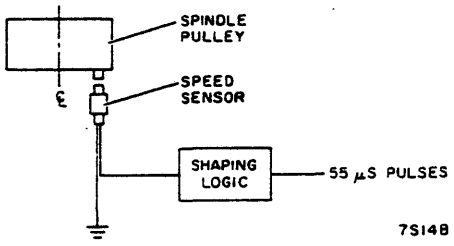


Figure 3-11. Speed Detection

Velocity Transducer

The velocity transducer (Figure 3-12) is a two-piece device consisting of a stationary tubular coil/housing and a movable magnetic core.

The magnetic core is connected via the extension rod to the rear surface of the head/arm receiver. All motion of the carriage is therefore duplicated by the magnetic core. As the core moves, an emf is induced in the coil. The amplitude of this emf is directly related to the velocity of the core (and carriage). The polarity of the emf is an indication of the direction of movement by the core (and carriage). The transducer output drives an operational amplifier located in the logic chassis. This signal is used by the servo logic to control acceleration/deceleration of the carriage during Seek operations.

FIRST SEEK INTERLOCK ASSEMBLY

The First Seek Interlock assembly provides a fixed time delay from the completion of the Start interlocks until heads can be loaded during the Power On/First Seek sequence.

The assembly consists of a motor, reset switch, cam linkage, and a mounting base. The base mounts on the deck assembly. The motor is energized during the Power On sequence and starts a 15-second (approximate) first seek interlock delay cycle. The cam revolves until the reset switch is encountered. The switch then transfers and removes power to the motor and signals completion of the delay cycle to the logic.

If power is lost or dropped during the cycle, the cam completes the initial cycle upon reapplication of power. At this time, a new cycle is initiated if Speed relay K2 has not been energized. Refer to Power On paragraph for a complete description of conditions that apply power to the first seek interlock motor.

BLOWER SYSTEM

The blower system (Figure 3-13) provides positive pressure in the pack area. The presence of this elevated pressure results in an outward dispersion of air preventing ingestion of contaminated air. This air flow greatly reduces possible contamination and resulting damage to the disk surfaces and the read/write heads.

Power to the blower drive motor is available whenever the UNIT POWER circuit breaker is on.

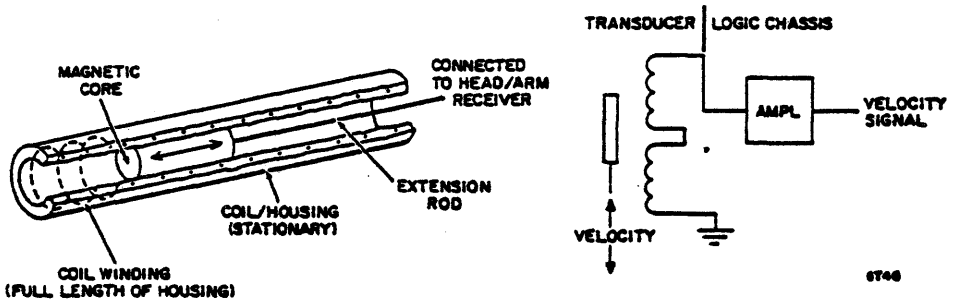


Figure 3-12. Velocity Detection

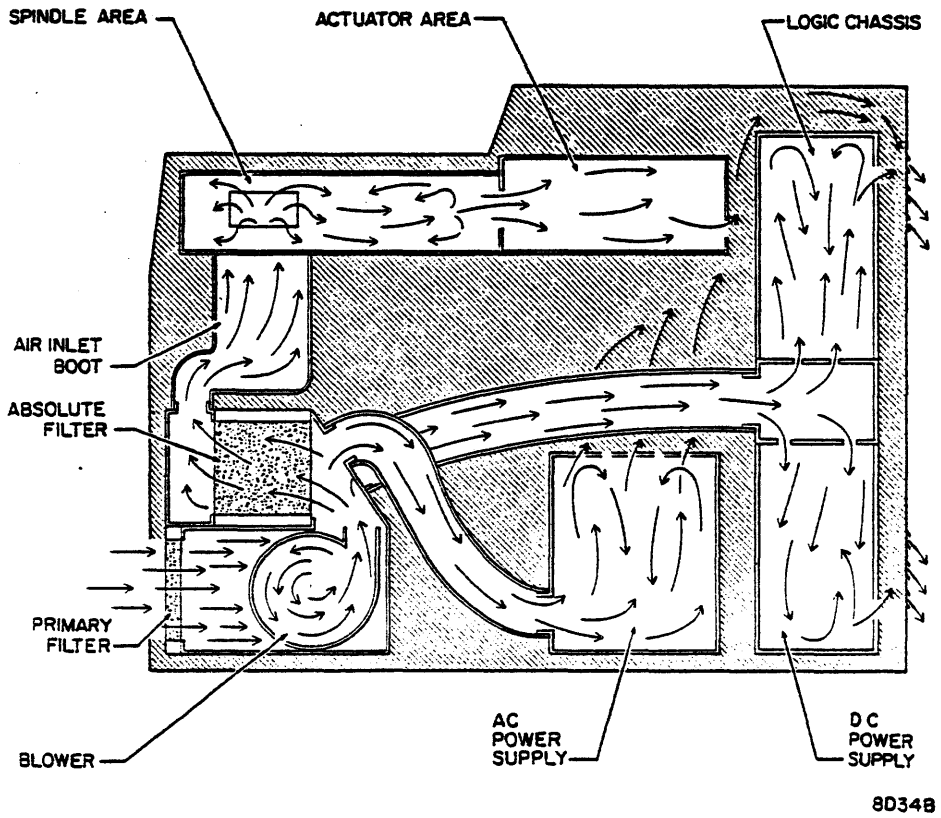


Figure 3-13. Blower System

DISK PACK

The disk pack is the recording medium for the drive. The disk pack consists of 12 14-inch disks, center-mounted on a hub. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders and adhesives. The top and bottom disks are protective non-recording disks.

There are 19 recording surfaces and one track servo surface. The servo disk contains pre-recorded information that is used by the servo logic to position the heads to the desired track.

The recording tracks are grouped in a 2 inch band near the outer edge of the disk. The disk has 823 tracks. The diameter of the outer track (823) is approximately 13 inches, while track 0 is about 3 inches. The tracks are spaced about 0.0026 inches apart.

The disk pack has a two-piece container. The bottom cover can be removed simply by grasping and rotating the center hub. The top cover is designed so that it can be removed only by installing the disk pack on the spindle. The disk pack can be removed from the spindle only by using the top cover (see Operation section). This design protects the disk pack from physical damage and greatly reduces the possibility of contamination of the disk pack recording surfaces.

INTRODUCTION

This subsection describes the logic functions performed by the drive and divides them into the following areas.

- Device Level Interface - Describes the signal lines connecting the drive to controller.
- Commands - Defines the commands issued to the drive and the drive responses to them.
- Command Execution - Describes how the drive logic processes commands received from the controller.
- Seek Operations - Explains how the drive logic controls the positioning of the read/write heads on the disk pack.
- Track Servo Circuit - Describes how this circuit derives, from the disk pack, timing pulses used by the Servo and Machine Clock circuits.
- Machine Clock Circuit - Explains how the Machine Clock generates the timing signals used by the index, sector and read/write circuits.
- Index Detection - Describes how the drive detects the index pattern which indicates the logical beginning of each track.
- Sector Detection - Explains how the drive derives the Sector pulses which are used to determine the angular position, with respect to Index of the read/write heads.
- Read/Write Operation - Explains how the drive processes the data that it reads from and writes on the disk pack.
- Sense Operations - Describes the drive logic used to monitor the status of the drive.
- Diagnostic Operations - Explains how the controller checks certain areas of drive operations by use of diagnostic commands.

Figure 3-14 is a block diagram illustrating basic signals within the drive. The functions of these signals are described in the applicable description of logic functions.

Most operations require the transfer of data between the controller and drive. Descriptions of these signal interchanges will emphasize drive functions. Controller functions are described only where necessary to clarify drive operations. Unless otherwise specified, controller signal timing is for illustrative purposes only. Refer to the applicable controller manual for details of controller operations and actual I/O timing.

DEVICE LEVEL INTERFACE

Signals are exchanged between the controller and drive by means of a set of signal conductors known as the Device Level Interface (DLI). The functions of these signals are described in Table 3-2 and shown on Figure 3-15.

The basic unit of information is the byte. A byte consists of eight information bits (logical 1 or 0) plus a parity bit. Data is transferred between the drive and controller one byte at a time. This information is transmitted in parallel: eight data lines plus one parity line to make odd parity.

COMMANDS

Commands may be classified as follows:

- Control Commands - Cause the drive to execute the instruction without any data transfer via the bidirectional data lines.
- Input Information Transfer Commands - Cause the drive to transfer data to the controller via the bidirectional data lines.
- Output Information Transfer Commands - These transfer data to the drive via the bidirectional data lines.
- Test and Diagnostic Commands - Controls drive operations for test purposes.

Table 3-3 describes the commands and classifies them according to the above categories. Figure 3-16 is a quick reference table showing all command abbreviations and hex decodes.

COMMAND EXECUTION

Before the drive will execute any commands, certain prior conditions must be met: the Controller must have Operational Out up and the drive must be online. Otherwise, commands are not recognized.

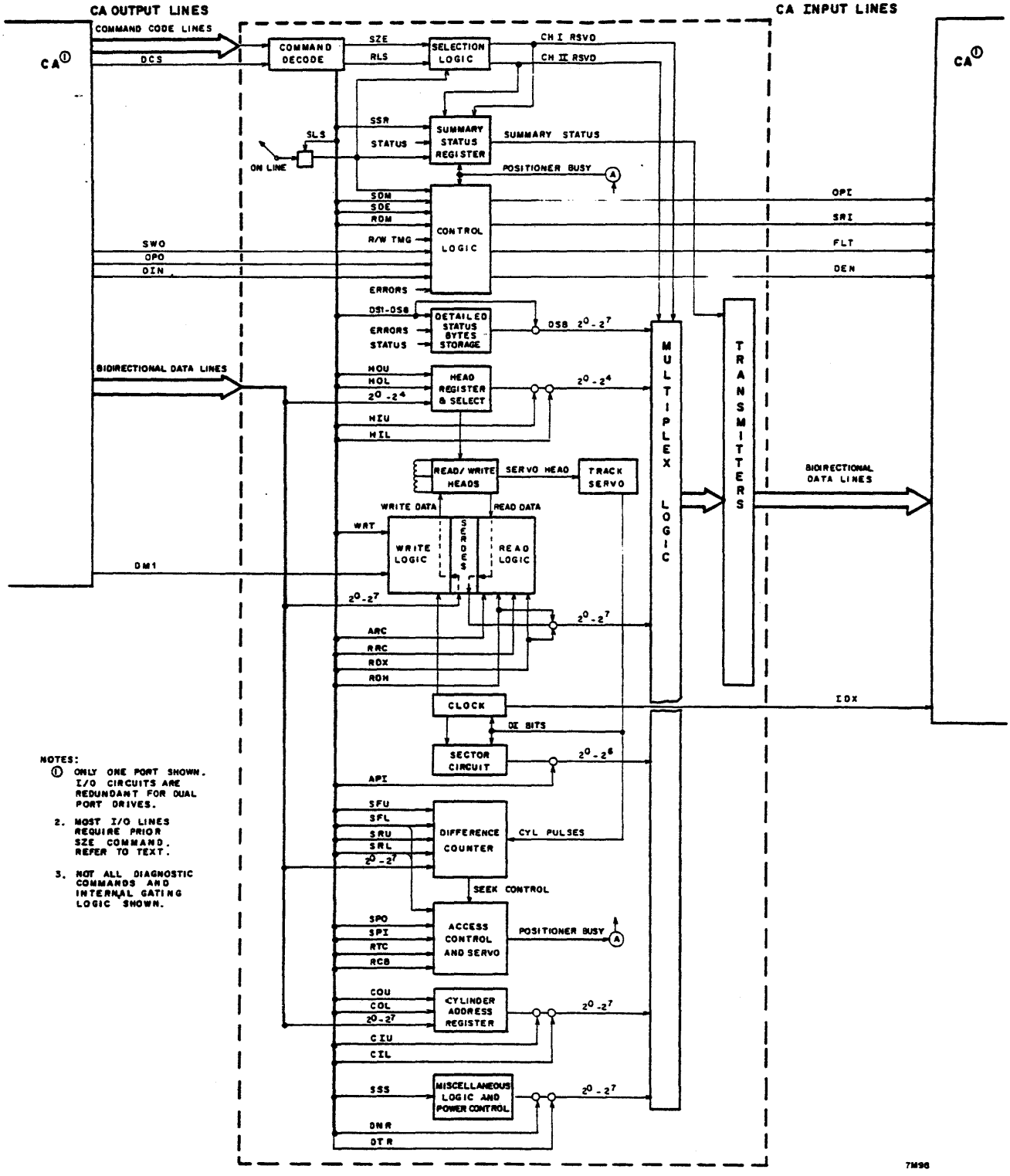


Figure 3-14. Drive Block Diagram

Figure 3-17 illustrates the logic used to decode commands from Channel I. With the exception of Seize and Summary Status Request the controller must first have successfully seized the drive. Regular commands without a prior Seize will cause a Select Fault; this raises FLT and sets bit 2^3 of the Summary Status Register. A subsequent Summary Status Request or Fault Reset (Device or Initialize power up) is required to reset the FLT. (For single channel drives, Seize will be accepted, but need not precede any other valid command. The CHI Reserved FF is held in the continuous set state.)

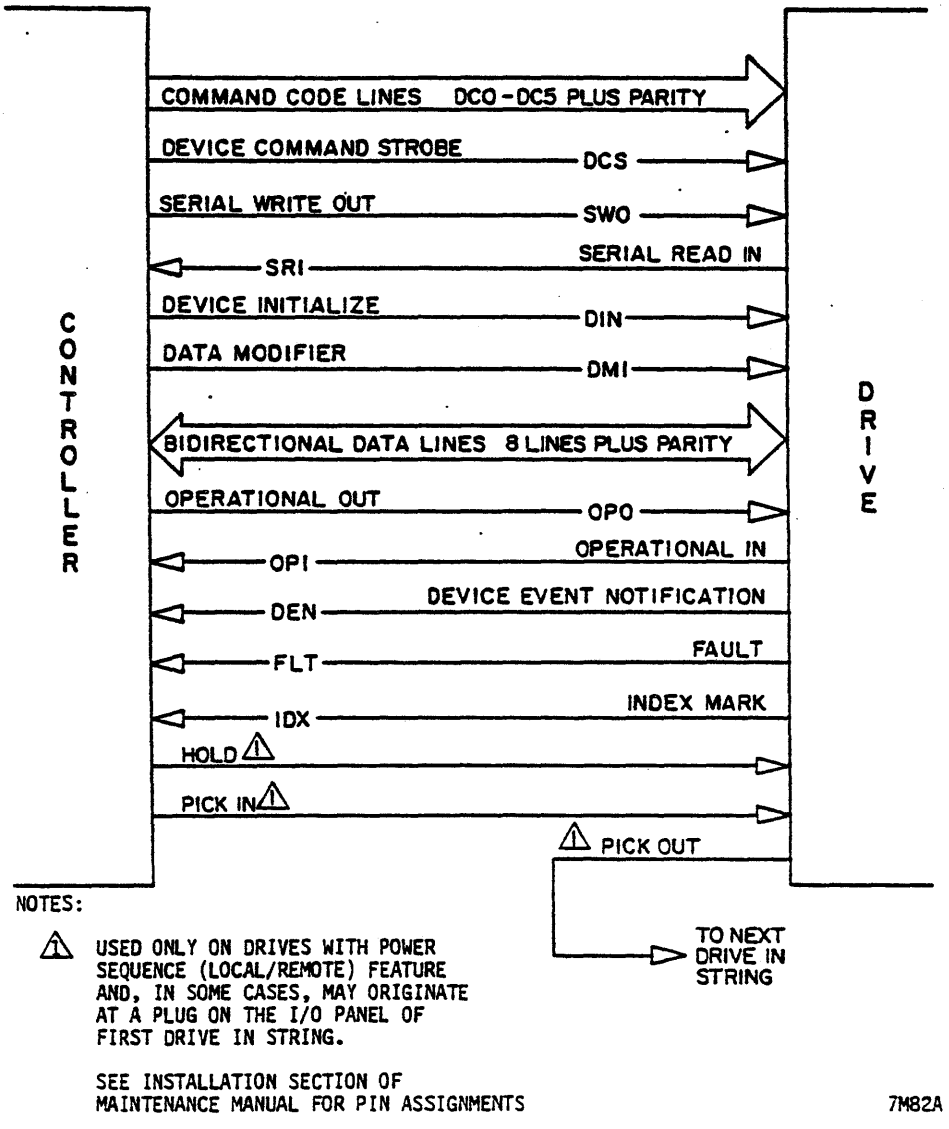
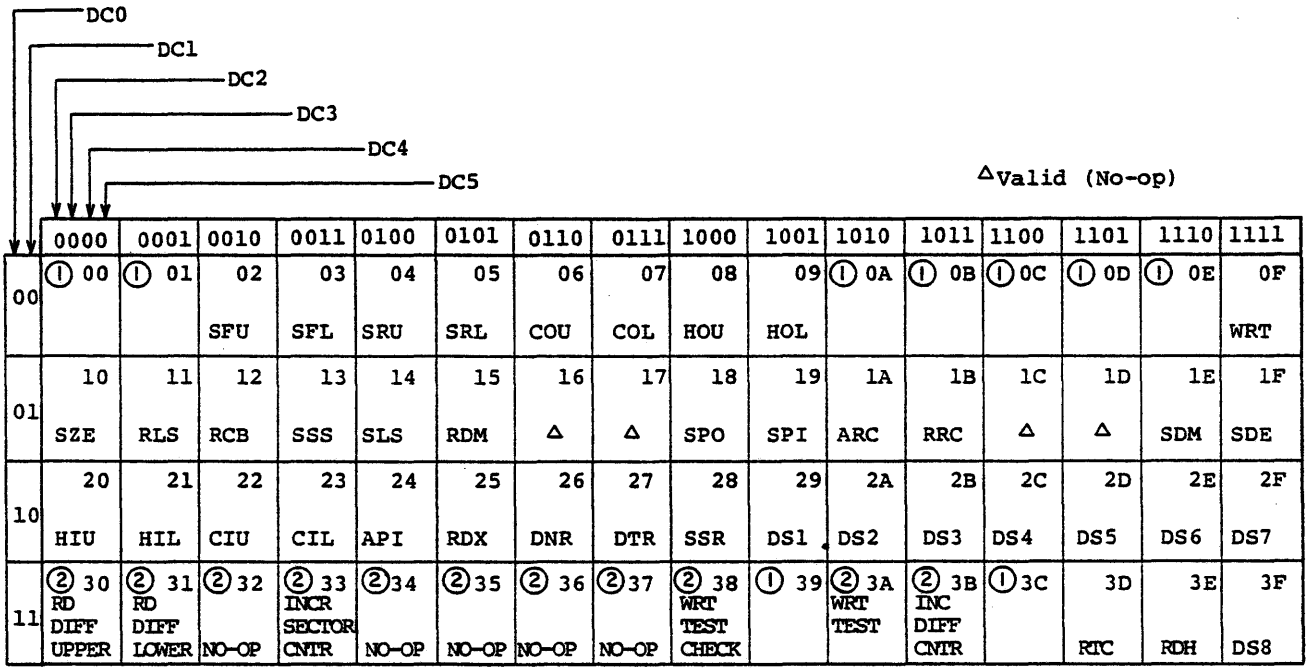


Figure 3-15. Device Level Interface Lines



	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
00	① 00	① 01	02 SFU	03 SFL	04 SRU	05 SRL	06 COU	07 COL	08 HOU	09 HOL	① 0A	① 0B	① 0C	① 0D	① 0E	0F WRT
01	10 SZE	11 RLS	12 RCB	13 SSS	14 SLS	15 RDM	16 △	17 △	18 SPO	19 SPI	1A ARC	1B RRC	1C △	1D △	1E SDM	1F SDE
10	20 HIU	21 HIL	22 CIU	23 CIL	24 API	25 RDX	26 DNR	27 DTR	28 SSR	29 DS1	2A DS2	2B DS3	2C DS4	2D DS5	2E DS6	2F DS7
11	② 30 RD DIFF UPPER	② 31 RD DIFF LOWER	② 32 NO-OP	② 33 INCR SECTOR CNTR	② 34 NO-OP	② 35 NO-OP	② 36 NO-OP	② 37 NO-OP	② 38 WRT TEST CHECK	① 39	② 3A WRT TEST	② 3B INC DIFF CNTR	① 3C	3D RTC	3E RDH	3F DS8

Output Info Xfer

SFU - Seek Forward-Upper

SFL - Seek Forward-Lower

SRU - Seek Reverse-Upper

SRL - Seek Reverse-Lower

COU - Cyl. Out-Upper

COL - Cyl. Out-Lower

HOU - Hd Addr Out-Upper

HOL - Hd Addr Out-Lower

WRT - Write

Control

SZE - Seize Device

RLS - Release Device

RCB - Recalibrate

SSS - Set Standby State

SLS - Set Local State

RDM - Reset Diag. Mode

RTC - Return to Track Centerline

SPO - Shift Posit. Out

SPI - Shift Posit. In

ARC - Adv. Read Clock

RRC - Ret. Read Clock

SDM - Set Diagnostic Mode

SDE - Set Diagnostic Escape

Input Info Xfer

HIU - Hd Addr-Upper

HIL - Hd Addr-Lower

CIU - Cyl. Addr In-Upper

CIL - Cyl. Addr In-Lower

API - Ang. Pos. In

RDX - Read

DNR - Device Number Request

DTR - Device Type Request

SSR - Sum. Stat. Req.

DS1 - Det. Stat. Req.-Byte 1

DS2 - Det. Stat. Req.-Byte 2

DS3 - Det. Stat. Req.-Byte 3

DS4 - Det. Stat. Req.-Byte 4

DS5 - Det. Stat. Req.-Byte 5

DS6 - Det. Stat. Req.-Byte 6

DS7 - Det. Stat. Req.-Byte 7

DS8 - Det. Stat. Req.-Byte 8

RDH - Read Header

NOTES:

① Invalid commands.

② Valid only during set diagnostic escape mode

7M83

Figure 3-16. Command Decodes & Abbreviations

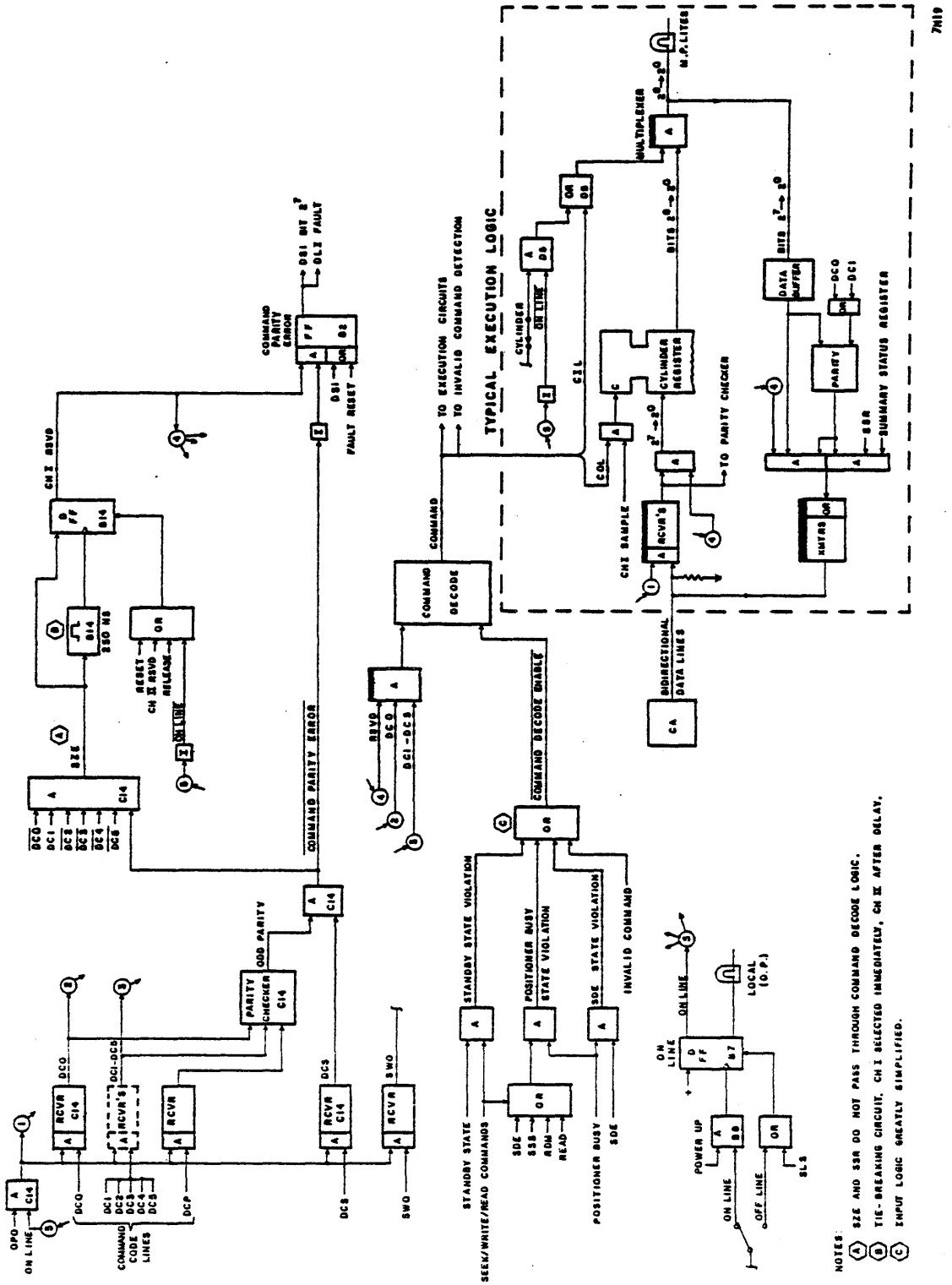


Figure 3-17. Command Decoding Logic

TABLE 3-2. SIGNAL LINES

Line	Function
	Lines From Controller To Drive
Command Code DCO-5	Six lines plus parity which carry encoded commands from controller to drive.
Device Command Strobe (DCS)	Indicates that the Command Decode lines are valid and the command may be decoded.
Operational Out (OPO)	When true it indicates the controller is operational. Unless this line is true the drive will ignore all signals from the controller.
Device Initialize (DIN)	Acts as a general reset to the drive: All drive status and control functions are reset and the positioner returns to cylinder 000. Before the drive will react to this signal the following conditions must be met. • Controller issuing command must have Operational Out true. • Controller issuing command must have seized the drive. This signal releases the seized status. • Drive must be On Line
Data Modifier (CM1)	Used during a write operation it causes the drive to ignore the data on the bidirectional data lines thereby creating an address mark.
Serial Write Out (SWO)	Signal from Controller to drive that is used in conjunction with Serial Write In (SRI) to syncronize transfer of data on the bidirectional data lines.
	Lines From Drive To Controller
Device Event Notification (DEN)	This line indicates that an event has occurred which is reflected in the Summary Status byte. The controller obtains this byte via Summary Status Request (Tag 28).
Fault	Indicates the drive has detected an error. The controller can determine the specific error by examining the Detailed Status bytes via the Detailed Status Request Commands (Tags 29 through 3D). All fault conditions, except pack unsafe, are cleared when the Detailed Status byte identifying the fault is requested or by a Device Initialize signal. Pack unsafe must be cleared by pushing the CHECK switch/indicator on the maintenance panel. The pack unsafe signal is caused by any of the following: • Low DC Voltage • No Servo Tracks Detected • Write Current Fault • Read or Write and Not On Cylinder
Serial Read In (SRI)	Signal from drive to controller that is used in conjunction with Serial Write Out to syncronize transfer of data on the bidirectional data lines.

TABLE 3-2. SIGNAL LINES (CONT'D)

Line	Function
Lines From Drive To Controller	
Index Mark (IDX)	A 2ms pulse indicating the drive has sensed the beginning of a logical track and occurs once each revolution of the disk pack. The leading edge defines the beginning of the track.
Operational In (OPI)	When true it indicates the drive is powered up, on line and capable of communicating with the controller.
Bidirectional Data Lines	
	Nine lines carrying data, address, control and status information between the controller and drive. The specific information transferred depends on the command being executed.
Power Sequence Lines (used only on units with Power sequence feature)	
Pick In	Used for power sequencing. A low on this line powers up drive if LOCAL/REMOTE switch is in REMOTE and START indicator if lighted. The drive receives the signal either from the controller or the previous drive in the string. Depending on the system, this signal may originate either at the controller or a jumper plug attached to the I/O panel of the first drive in the string. With the jumper plug, the signal is held low at the input to the first drive. See Local/Remote Control discussion for more information.
Hold	Used for power sequencing. This line must be low for drive to remain in a power up condition after completing a remote power up. Like Pick In, this signal may originate either at the controller or the first drive in the string.
Pick Out	Goes to next drive in string as Pick In. If this drive is in local, the signal is low thereby allowing the next drive to power up. If LOCAL/REMOTE switch is in REMOTE, the signal goes low when the drive completes its power on sequence.

TABLE 3-3. COMMANDS

<table>
<tr><th>Command</th><th>Definition/Function</th></tr>
<tr><td>Seek Forward Upper (SFU) Tag 02</td><td>
1. An output information tag.
2. Loads Upper 2 bits of seek difference information (512,256) into temporary storage for gating into the Difference Counter during a subsequent Seek Forward Lower (Tag 03). The data is received via the bidirectional data lines.
3. This tag must precede the Seek Forward Lower Command.
4. Bidirectional data lines are decoded as follows:
<table>
<tr><th>Bit</th><th>Decode</th></tr>
<tr><td>2^0</td><td>DIFF 256</td></tr>
<tr><td>2^1</td><td>DIFF 512 (BR3C9 only)</td></tr>
<tr><td>2^2-2^7</td><td>Not Used</td></tr>
</table>
</td></tr>
<tr><td>Seek Forward Lower (SFL) Tag 03</td><td>
1. An output information tag.
2. Loads lower 8 bits of seek difference information (tracks to go) from bidirectional data lines into the Difference counter.
3. This tag must be preceded by a Seek Forward Upper (Tag 03) or the fault line is raised along with Bit 2^4 of the Detailed Status Byte.
4. This command causes the drive to seek forward the number of cylinders indicated by the difference count.
5. The Bidirectional data lines decode as follows:
<table>
<tr><th>Bit</th><th>Decode</th><th>Bit</th><th>Decode</th></tr>
<tr><td>2^0</td><td>DIFF 1</td><td>2^4</td><td>DIFF 16</td></tr>
<tr><td>2^1</td><td>DIFF 2</td><td>2^5</td><td>DIFF 32</td></tr>
<tr><td>2^2</td><td>DIFF 4</td><td>2^6</td><td>DIFF 64</td></tr>
<tr><td>2^3</td><td>DIFF 8</td><td>2^7</td><td>DIFF 128</td></tr>
</table>
</td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function
Seek Reverse Upper (SRU) Tag 04	Same as Seek Forward Upper except that seek is in reverse direction.
Seek Reverse Lower (SRL) Tag 05	Same as Seek Forward Lower except that seek is in reverse direction.
Cylinder Out Upper (COU) Tag 06	1. An output information tag. 2. Cause the drive to set the high order bits (512 and 256) in the Cylinder Address register (CAR) according to the information on the bidirectional data lines. 3. This command must precede the Cylinder Out Lower (Tag 07) command. 4. The bidirectional data lines send the following information to the drive. Bit: 2^0 — Decode: CAR 256 Bit: 2^1 — Decode: CAR 512 (BR3C9 only) Bit: 2^2-2^7 — Decode: Not Used
Cylinder Out Lower (COL) Tag 07	1. An output information tag. 2. Causes the drive to load the 8 low order bits of the new cylinder address into the Cylinder Address Register (CAR). 3. The bidirectional data lines are decoded as follows: Bit: 2^0 — Decode: CAR 1 Bit: 2^1 — Decode: CAR 2 Bit: 2^2 — Decode: CAR 4 Bit: 2^3 — Decode: CAR 8 Bit: 2^4 — Decode: CAR 16 Bit: 2^5 — Decode: CAR 32 Bit: 2^6 — Decode: CAR 64 Bit: 2^7 — Decode: CAR 128
Head Address Out Upper (HOU) Tag 08	Has no effect in the drive.
Head Address Out Lower (HOL) Tag 09	1. An output information tag. 2. Transfers head address information to the drive via the bidirectional data lines. The drive stores the data in the Head Address Register (HAR). The drive will now read and write data using the head identified by this head address.

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function
(HOL) (Cont'd)	3. The bidirectional data lines decode as follows: Bit: Decode 2^0: HAR 1 2^1: HAR 2 2^2: HAR 3 2^3: HAR 8 2^4: HAR 16 2^5-2^7: Not Used
Tags OA-OE	Invalid commands
Write (WRT) Tag OF	1. An output information command. 2. This command causes the drive to Write data on the disk pack. See the discussion on Write operations for more information.
Recalibrate (RCB) Tag 12	1. A control command. 2. Causes the Head register and Cylinder Address register to be set to zero and the heads to return to track 000 (RTZ).
Set Standby State (SSS) Tag 13	1. A control command. 2. Causes the drive to turn off the pack motor, unload the heads and extinguish the START indicator. 3. To return to the ready state the operator must push the START button.
Set Local State (SLS) Tag 14	1. A control command. 2. Removes drive from on line status. It breaks I/O communication between drive and controller and lights the LOCAL indicator. 3. Drive is returned to On Line status by moving the ON LINE/OFF LINE switch from ON LINE to OFF LINE and then back to ON LINE.
Seize Device (SZE) Tag 10	1. A control command. 2. When 2 controllers are connected to a drive (dual channel) this signal is used to seize (select) the drive. For dual channel operation the drive must be seized before it will respond to other instructions (other than Summary Status Byte Request). However the seize is not required for single channel operation. 3. The drive responds to the command only if it has not been previously seized by the other controller.
Release Device (RLS) Tag 11	1. A control command. 2. Issued by the controller having the drive seized, it releases the drive from the seized condition thus making it available to both controllers. 3. The drive sends a Device Event Notification (DEN) to the other controller telling it the drive is now available.

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function
Reset Diagnostic Mode (RDM) Tag 15	1. A control command. 2. Resets diagnostic operations (Tags 1E or 1F) and places drive in normal mode. 3. The drive performs an RTZS (refer to Recalibrate Tag 12).
Tag 16, 17	These tags are recognized and acknowledged by the drive but initiate no operations.
Shift Positioner Out (SPO) Tag 18	1. A control command. 2. This is used for data retry and error recovery. 3. It causes the positioner to move the read/write heads 400 µin away from the spindle unless Shift Positioner In (Tag 19) was active in which case it would cause the heads to return to the track centerline. In either case the drive generates a 10 ms Positioner Busy signal. 4. The Offset condition is reset and the positioner returned to the track centerline by any of the following: • Device Initialize Signal (DIN) • Return to Centerline (Tag 30) • Shift Positioner In (Tag 19) • Any Seek Command (however the seek is not performed) • Loss of On Cylinder
Shift Positioner In (SPI) Tag 19	1. A control command. 2. Same as Shift Positioner OUt (Tag 20) except that the heads are offset 400 µin towards the spindle and Shift Position Out replaces Shift Position In as a reset condition.
Advance Read Clock (ARC) Tag 1A	1. A control command. 2. Used during data recovery it moves the Read Data strobe to the early position of the data window (about 8 ns earlier than normal). 3. The function is reset by a Recalibrate (Tag 12) or Retard Read Clock (Tag 1B).
Retard Read Clock RRC Tag 1B	1. A control command. 2. The same as Advance Read Clock (Tag 1A) except that it retards the Read Data strobe by about 8 ns. 3. Reset by a Recalibrate (Tag 12) or an Advance Read Clock (Tag 1A).
Set Diagnostic Mode (SDM) Tag 1E	1. A control command. 2. Places drive in diagnostic mode and sets bit 7 (Device in Diagnostic Mode) of Summary Status Byte. 3. This command initiates no function in drive unless Set Diagnostic Escape (Tag 1F) is also received. 4. Drive returned to normal operation by a Reset Diagnostic Mode (Tag 15) or by the Device Initialize line going true.

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function
Set Diagnostic Escape (SDE) Tag 1F	1. A control command. 2. Enables the drive logic to perform special diagnostic functions by disabling the normal command repertoire (except for Tag 15) and conditioning the logic to receive to test and diagnostic commands (Tags 30 through 37). 3. This command inhibits the Sector Counter and sets Bit 7 (Device in Diagnostic Mode) of the Summary Status byte. 4. Drive is returned to normal operation by a Reset Diagnostic Mode (Tag 15) or by the Device Initialize line going true.
Head Address In Upper (HIV) Tag 20	1. An input information command. 2. Causes the drive to return a byte of zeros on the bidirectional data lines.
Head Address In Lower (HIL) Tag 21	1. An input information command. 2. Drive transfers its current head address to the controller via the bidirectional data lines. 3. The bidirectional data lines decode as follows: Bit — Decode 2^0 — HAR 1 2^1 — HAR 2 2^2 — HAR 4 2^3 — HAR 8 2^4 — HAR 16 2^5-2^7 — Not Used
Cylinder Address In Upper (CIU) Tag 22	1. An input information command. 2. Causes drive to place high order bits of current positioner location on bidirectional data lines. 3. Bidirectional data lines are decoded as follows: Bit — Decode 2^0 — CAR 256 2^1 — CAR 512 2^2-2^7 — Not Used
Cylinder Address In Lower (CIL) Tag 23	1. An input information command. 2. Causes drive to place 8 low order bits of current positioner location on bidirectional data lines.

TABLE 3-3. COMMANDS (CONT'D)

<table>
<tr><th>Command</th><th>Definition/Function</th></tr>
<tr><td>CIL (Cont'd)</td><td>3. Bidirectional data lines are decoded as follows:

<table>
<tr><th>Bit</th><th>Decode</th></tr>
<tr><td>2^0</td><td>CAR 1</td></tr>
<tr><td>2^1</td><td>CAR 2</td></tr>
<tr><td>2^2</td><td>CAR 4</td></tr>
<tr><td>2^3</td><td>CAR 8</td></tr>
<tr><td>2^4</td><td>CAR 16</td></tr>
<tr><td>2^5</td><td>CAR 32</td></tr>
<tr><td>2^6</td><td>CAR 64</td></tr>
<tr><td>2^7</td><td>CAR 128</td></tr>
</table></td></tr>
<tr><td>Angular Position In (API)
Tag 24</td><td>1. An input information command.

2. Gates current angular position (sector to the controller. This is the value the Sector Counter was at when the API Tag was received.

3. Bidirectional data lines decode as follows:

<table>
<tr><th>Bit</th><th>Decode</th></tr>
<tr><td>2^0</td><td>1</td></tr>
<tr><td>2^1</td><td>2</td></tr>
<tr><td>2^2</td><td>4</td></tr>
<tr><td>2^3</td><td>8</td></tr>
<tr><td>2^4</td><td>16</td></tr>
<tr><td>2^5</td><td>32</td></tr>
<tr><td>2^6</td><td>64</td></tr>
<tr><td>2^7</td><td>Not Used</td></tr>
</table></td></tr>
<tr><td>Read (RDX)
Tag 25</td><td>1. An input information tag.

2. Enables the drive to read data from the disk pack. See discussion on read operations for more information.</td></tr>
<tr><td>Device Number Request (DNR)
Tag 26</td><td>1. An input information command.

2. Causes the drive to place the 8 bit physical identifier number on the bidirectional data lines.</td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

<table>
<tr><th>Command</th><th>Definition/Function</th></tr>
<tr><td>DNR (Cont'd)</td><td>3. Bidirectional data lines decode as follows:

<table>
<tr><th>Bit</th><th>Decode</th></tr>
<tr><td>2^0</td><td>1</td></tr>
<tr><td>2^1</td><td>2</td></tr>
<tr><td>2^2</td><td>4</td></tr>
<tr><td>2^3</td><td>8</td></tr>
<tr><td>2^4</td><td>16</td></tr>
<tr><td>2^5</td><td>32</td></tr>
<tr><td>2^6</td><td>64</td></tr>
<tr><td>2^7</td><td>128</td></tr>
</table></td></tr>
<tr><td>Device Type Request (DTR) Tag 27</td><td>1. An input information command.

2. Causes drive to return prewired type identifier code on bidirectional data lines.

3. Bidirectional data lines are decoded as follows:

<table>
<tr><th>Bit</th><th>Decode (200MB)</th><th>Decode (100MB)</th></tr>
<tr><td>2^0</td><td>1</td><td>1</td></tr>
<tr><td>2^1</td><td>0</td><td>0</td></tr>
<tr><td>2^2</td><td>0</td><td>1</td></tr>
<tr><td>2^3</td><td>1</td><td>1</td></tr>
<tr><td>2^4</td><td>1</td><td>1</td></tr>
<tr><td>2^5</td><td>0</td><td>0</td></tr>
<tr><td>2^6</td><td>1</td><td>1</td></tr>
<tr><td>2^7</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>Summary Status Request (SSR) Tag 28</td><td>1. An input information command.

2. Causes the drive to transfer 8 bits of summary status information to the controller via the bidirectional data lines. The unit need not be seized or have a pack installed (refer to Sense Operations for more information).

3. The bidirectional data lines are interpreted as follows:

<table>
<tr><th>Bit</th><th>Name</th><th>Meaning</th></tr>
<tr><td>2^0</td><td>Device In Diagnostic Mode</td><td>Drive has received a Set Diagnostic Mode (Tag 1E) or Set Diagnostic Escape (Tag 1F).</td></tr>
</table></td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function		
SSR (Cont'd)	Bit	Name	Meaning
	2^1	Device Failure	Error has been detected in drive. One of the following occurred: 1. Any error of DS2 (see Table 4-7). 2. Bits 2^3 and 2^7 of DS3. 3. Bit 2^0 of DS5. 4. Pack Unsafe FF set. This lights the CHECK indicator. This condition is set by any of the following: a. Read or Write while not On Cylinder. b. Voltage fault of ±5v, ±20v, or -16v power. c. Dibits lost for more than 200 milliseconds. d. Simultaneous Read and Write. e. Current Fault (see DS2, bits 2^4 thru 2^7). Any of the above conditions will raise the FLT line.
	2^2	Device Protected	WRITE PROTECT indicator is on.
	2^3	DLI Error	Interface error has been detected by drive. One of the following has occurred: 1. Any error of DS1. 2. Bit 2^6 of DS3. 3. Select Fault has occurred. Controller attempted any command other than Summary Status Request or Seize before first successfully seizing the drive. Any of the above conditions will raise the FLT line.
	2^4	Positioner Busy	Positioner is in motion. One of the following conditions exist: 1. Not Unit Ready and Not Stop (typically a First Seek sequence).

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function		
SSR (Cont'd)	Bit	Name	Meaning
	2^4	Positioner Busy (Cont'd)	2. Stop with heads loaded (typically a power off sequence). 3. Zero-length Seek Forward Lower or Seek Reverse Lower command. 4. Seek in progress (not On Cylinder). 5. Up for 10 milliseconds following receipt of Start Positioner In or Start Positioner Out or, if one of these is already set, Return to Centerline or Recliabrate. When the Positioner Busy status drops, DEN is returned to the controller.
	2^5	Device in Standby	Drive is in Standby Mode, that is, Unit Ready (First Seek to On Cylinder) is not available yet. Status is cleared by Stop (Set Standby State or press START to extinguish indicator).
	2^6	Device Seized	Drive has accepted a Seize command and is reserved to controller issuing the Summary Status Request. If drive is single-port device, this signal is always available without requiring a Seize command.
	2^7	Device Reserved	Drive has already been seized by the other channel.
Detailed Status Byte 1 (DSB1) Tag 29	1. This is an input information command. 2. This command causes the drive to present a byte of data concerning various drive error conditions. These conditions are identified on the bidirectional data lines. 3. The FF's corresponding to the status bits are reset by the Detailed Status Byte 1 command, a Device Initialize signal or by pushing the CHECK indicator/switch on the maintenance panel. 4. All errors identified in Detailed Status Byte 1 set Summary Status Byte Bit 2^3 (DLI error). 5. The bidirectional data lines are interpreted as follows:		
	Bit	Name	Meaning
	2^0	Data Parity Error	On Output Information Transfer Commands (DC0,DC1 = 00), parity was not odd during time that SWO is down while SRI is up.

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function		
DSB1 (Cont'd)	Bit	Name	Meaning
	2^1	Transfer Timing Error	During read or write operations, Serial Write Out and Serial Read In timing relationships were incorrect.
	2^2	Protect Violation	WRT or Write Test command was issued with WRITE PROTECT indicator on. Also sets DS1, bit 2^3.
	2^3	State Violation	Any one of the following errors occurred: 1. Same condition that set DS1, bit 2^2. 2. WRT or Write Test command with Positioner Busy. 3. Write or Write Test command while offset (Shift Positioner Out or In) is active if not in Set Diagnostic Escape Mode (Tag 1F). 4. Standby State Violation -- one of the following commands was decoded with drive in Standby: RCB SFL SPO WRT RDH SFU SRL RDX SPI SRU 5. Positioner Busy State Violation -- one of the following commands was decoded with Positioner Busy up. RCB RDX SFU SRL RDH SDE SPI SRU RDM SFL SPO SSS WRT
	2^4	Invalid Command Sequence	One of the following invalid sequences occurred: 1. COL preceded COU. 2. SFL preceded SFU. 3. SRL preceded SRU.

TABLE 3-3. COMMANDS (CONT'D)

<table>
<tr><th>Command</th><th colspan="3">Definition/Function</th></tr>
<tr><td>DSB1 (Cont'd)</td><td>Bit</td><td>Name</td><td>Meaning</td></tr>
<tr><td></td><td>2^5</td><td>Invalid Command</td><td>1. A diagnostic command was issued prior to a Set Diagnostic Escape (Tag 1F).

2. A no-op command (other than codes 32,34,35,36, or 37 during Set Diagnostic Escape) was received while in any mode.</td></tr>
<tr><td></td><td>2^6</td><td>Not Used</td><td></td></tr>
<tr><td></td><td>2^7</td><td>Command Parity Error</td><td>Command did not have odd parity at rise of Device Command Strobe.</td></tr>
<tr><td>Detailed Status Byte 2 (DSB2) Tag 2A</td><td colspan="3">1. An input information command.

2. This command causes the same function as DSB1 except for the following:

• All errors in this status byte set Summary Status Byte bit 2^1.

• All errors in this status byte are reset by the DSB2 command, the Device Initialize signal or the CHECK switch/indicator.

• The bidirectional data line decode is different.

3. The bidirectional data line decode is as follows:</td></tr>
<tr><td></td><td>Bit</td><td>Name</td><td>Meaning</td></tr>
<tr><td></td><td>2^0</td><td>Loss of Voltage</td><td>Any one of the following dc voltage errors occurred:

1. +5v less than +4.825v.

2. -5v more positive than -4.825v.

3. +20v less than +18v.

4. -20v more positive than -18v.

5. -16v more positive than -12v.

Any of these errors will set Pack Unsafe FF and light indicator. In addition, insufficient -16v power will cause automatic emergency retract of positioner.</td></tr>
<tr><td></td><td>2^1</td><td>Not Used</td><td></td></tr>
<tr><td></td><td>2^2</td><td>Spindle Speed Loss</td><td>Spindle speed dropped below 2700 rpm after heads were loaded. Heads unload.</td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

<table>
<tr><th>Command</th><th>Definition/Function</th></tr>
<tr><td>DSB2 (Cont'd)</td><td>
<table>
<tr><th>Bit</th><th>Name</th><th>Meaning</th></tr>
<tr><td>2^3</td><td>Not Used</td><td></td></tr>
<tr><td>2^4</td><td>No or Multiple Head Selection</td><td>Head number 19 or greater (non-existent) is selected or more than two heads have been selected.

NOTE

The remaining DS2 bits apply only while writing with DM1 down.</td></tr>
<tr><td>2^5</td><td>Loss of AC Write Current</td><td>No write driver output current transitions were detected for 900 nanoseconds.</td></tr>
<tr><td>2^6</td><td>Write Current without Write Command</td><td>Write current is sensed but Write Enable is down.</td></tr>
<tr><td>2^7</td><td>Write Command without Write Current</td><td>Write Enable is up, but there is no write current.</td></tr>
</table>
</td></tr>
<tr><td>Detailed Status Byte 3 (DSB 3) Tag 2B</td><td>
1. An input information command.

2. Sends a byte of status to the controller concerning the error condition identified on the bidirectional data lines.

3. The error conditions are reset by any of the following:

• Device Initialize (DIN) signal.

• Pushing CHECK switch/indicator

• By the DSB 3 command

4. The bidirectional data lines are interpreted as follows:

<table>
<tr><th>Bit</th><th>Name</th><th>Meaning</th></tr>
<tr><td>2^0-2^2</td><td>Not Used</td><td></td></tr>
<tr><td>2^3</td><td>Rotational Position Sensing Fault</td><td>While not in Set Diagnostic Escape Mode, sector counter did not reach a count of 127 before Index was sensed. Also sets Device Failure (SSR bit 2^1).</td></tr>
<tr><td>2^4-2^5</td><td>Not Used</td><td></td></tr>
<tr><td>2^6</td><td>Positioner Overtravel</td><td>Positioner went forward past cylinder 822 (Forward EOT) or reverse past cylinder 000 (Reverse EOT) if not performing an RTZS. Also sets DLI Error (SSR bit 2^3).</td></tr>
</table>
</td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function		
DSB 3 (Cont'd)	Bit	Name	Meaning
	2^7	Seek Incomplete	Positioner could not attain On Cylinder status with 500 milliseconds after start of a controller-initiated seek (SFL, SRL, RCB, or RDM). Also sets Device Failure (SSR bit 2^1).
Detailed Status Byte 4 (DSB4)	1. An input information command. 2. This command causes the drive to present a byte of data concerning the status of the drive at the time the command was received. 3. The bidirectional data lines are interpreted as follows:		
	Bit	Name	Meaning
	2^0	Reverse FF Set	Status bit indicating that Seek Reverse Lower was last seek command. Not affected by Recalibrate or Reset Diagnostic Mode.
	2^1	Forward FF Set	Status bit indicating that SFL was last seek command. Not affected by Recalibrate or Reset Diagnostic Mode.
	2^2	Restricted Air Flow	Cooling air was of inadequate volume. CHECK indicator lights.
	2^3	Not Used	
	2^4	First Seek Interlock Cycle Incomplete	Status bit indicating that First Seek Interlock motor is operating.
	2^5	Not Used	
	2^6	Tester Address Error (Offline Only)	Not used while Online. When Offline, Off Line Tester has detected a difference between the current cylinder address and the address byte read from the pack. Device Failure (SSR 2^1) is set, but not returned to controller since drive is Offline. In addition, error may be displayed by setting DISPLAY SELECT switch on maintenance panel to DSB4. Bit 2^6 indicator will be on. Error is cleared by pressing CHECK or by returning unit to Online mode.
	2^7	Fine Servo Status	Fine FF is set: less than one-half cylinder remains of seek, positioner is On Cylinder, or positioner is in LOAD or RTZ sequence.

TABLE 3-3. COMMANDS (CONT'D)

<table>
<tr><th>Command</th><th>Definition/Function</th></tr>
<tr><td>Detailed Status Byte 5 (DSB5) Tag 2D</td><td>1. An input information command.

2. This command causes the drive to present a byte of data that, except for bit 2; concerns the status of the drive at the time the command was executed. The status is returned on the bi-directional data lines.

3. The bidirectional data lines are interpreted as follows:

<table>
<tr><th>Bit</th><th>Name</th><th>Meaning</th></tr>
<tr><td>2^0</td><td>Write and Read</td><td>Both Write Enable and Read Enable were up simultaneously. This sets Pack Unsafe FF to light the CHECK indicator and to set Device Failure (SSR bit 2^1).</td></tr>
<tr><td>2^1</td><td>Read Clock Offset</td><td>Status bit indicating that read circuit is under influence of ARC or RCC command.</td></tr>
<tr><td>2^2</td><td>Positioner Offset</td><td>Status bit indicating that positioner is under influence of a Shift Positioner Out or In command.</td></tr>
<tr><td>2^3</td><td>Heads Retracted</td><td>Status bit indicating that heads are unloaded as sensed by heads loaded switch.</td></tr>
<tr><td>2^4-2^7</td><td>Not Used</td><td></td></tr>
</table>
</td></tr>
<tr><td>Detailed Status Bytes 6,7 (DSB6,7) Tags 2E,2F</td><td>These tags are recognized and acknowledged by the drive but initiate no drive functions.</td></tr>
<tr><td>Read Difference Counter Upper Tag 30</td><td>1. A test and diagnostic command requiring prior acceptance of a Tag 1F.

2. Causes the drive to gate bits 2^8 and 2^9 of Difference Counter onto bits $2^0$and 2^1 of bidirectional data lines.</td></tr>
<tr><td>Read Difference Counter Lower Tag 31</td><td>1. A test and diagnostic command requiring prior acceptance of a Tag 1F.

2. Causes the drive to gate bits 2^0 through 2^7 of Difference counter onto bidirectional data lines.</td></tr>
<tr><td>Tag 32</td><td>This tag is recognized and replied to by the drive but initiates no drive operations.</td></tr>
<tr><td>Increment Sector Counter Tag 33</td><td>1. A test and diagnostic command requiring prior acceptance of a Tag 1F.

2. Causes the drive to increment its Sector counter by 1. The counter and its register are reset by Set Diagnostic Escape (Tag 1F). With Tag 1F up the index and dibits input to the counter is disabled. The counter value is read by an Angular Position In Command (Tag 24).</td></tr>
</table>

TABLE 3-3. COMMANDS (CONT'D)

Command	Definition/Function
Tags 34,35,36, 37	These tags are recognized and replied to by the drive but initiate no drive operations.
Write Test Check Tag 38	1. A test and diagnostic command requiring prior acceptance of a Tag 1F. 2. Issued after Write Test (Tag 3A). If NRZ fault occurred (error condition), bit 2^0 of bidirectional data lines will be true. If Current fault occurred (normal condition Write Test), bit 2^1 will be true. Error conditions are cleared when command drops.
Write Test (Tag 3A)	1. A test and diagnostic command requiring prior acceptance of a Tag 1F. 2. Causes drive to write special pattern transferred via bidirectional data lines. It then checks the following: • Toggling of NRZ data as it leaves the Serdes Shift Register. If toggles are absent for more than 800 nsec NRZ fault sets (refer to Write Test Check Tag 38). • The AC Write Fault Detector is checked when the controller raises the Data modifier line causing a period without byte transitions. This should set Write Test Current Fault.
Tag 3B	This tag is recognized and replied to by the drive but initiates no drive operation.
Tag 3C	Invalid command.
Return To Track Centerline (RTC) Tag 3D	1. A control command. 2. Causes positioner to return to track centerline by resetting either Shaft Positioner Out (Tag 18) or Shift Positioner In (Tag 19). 3. This causes a 10 ms Positioner Busy status followed by Device Event Notification (DEN).
Read Header (RDH) Tag 3E	1. An input information command. 2. Some function as Read (Tag 25) except that the drive searches for and must find the address mark before any data transfer can occur (see discussion on read operations).
Detailed Status Byte 8 (DSB8) Tag 3F	This command is recognized and replied to by the drive but initiates no drive functions.

Note that the drive may be in the standby state and still execute commands not involving seeks, reads, or writes. To complete a Summary Status Request for example, the drive must be powered up but need not even have a pack installed.

As an example of execution sequence assume that the unit is seized and that a cylinder Out Lower (COL) command has been issued. See Figure 3-18. Sequencing is then as follows:

1. Controller places the command byte on the Command Code Lines.
2. Drive decodes the command (000 111) as Cylinder Out Lower. Since DC0=0, Enable Serial Read In is generated internally.
3. Controller raises Device Command Strobe. The following occur if the command byte plus parity is not odd:
   a. Command Parity Error is generated.
   b. Bit 2^7 of DS1 sets.
   c. DLI Fault comes up.
   d. FLT returned to controller.
4. Controller raises Serial Write Out.
5. SRI Out FF (Figure 3-18) sets to raise Serial Read In.
6. Controller drops Serial Write Out.
7. With Serial Write Out down, single-shot DCØ1 triggers and remains up for one microsecond. This raises CH I Sample, causing the following:
   a. Logic verifies that Cylinder Out Upper preceded Cylinder Out Lower. If not, Invalid Command Sequence (bit 2^4 of DS1) and DLI Fault are set.
   b. Data on bidirectional lines loaded into Cylinder Address Register. See Figure 3-17. (In the case of Cylinder Out Lower, bit 2^8 was stored by a flip-flop during the preceding Cylinder Out Upper and is also gated in at this time.)
8. After one microsecond, DCØ1 returns to its untriggered state to trigger DCØ2 for one microsecond. This causes the following:
   a. Data parity is checked. If not odd, bit 2^0 of DS1 is set along with DLI Fault.
   b. Seek Enable comes up. If the command is a seek (SFL, SRL, or RCB), it is executed at this time.
   c. SRI Out FF clears to drop SRI.

On an input command (Cylinder In Lower in Figure 3-18), Serial Write Out is raised in response to Serial Read In, Execution sequence is as follows:

1. Command byte raised by controller.
2. Drive decodes command as Cylinder In Lower (100 011). This gates the contents of the Cylinder Address Register (Figure 3-17) onto the multiplexer.
3. Device Command Strobe is raised by the controller, triggering single-shot DCØ3 for 500 nanoseconds. The multiplexer data is loaded into the Data Buffer which serves both channels.
4. The data is immediately applied to the I/O transmitters (and also to the receivers).
5. If both DC0 and DC1 are not down, the drive will add a parity bit (DIP) if required. Correct parity is not, however, checked.
6. After DCØ3 times out, it triggers single-shot DCØ4 for 500 nanoseconds. When it times out, SRI In FF sets to raise Serial Read In to the controller.
7. When the controller raises Serial Write Out, Serial Read In, SRI drops.
8. When the controller drops Device Command Strobe, the Data Buffer is reset.

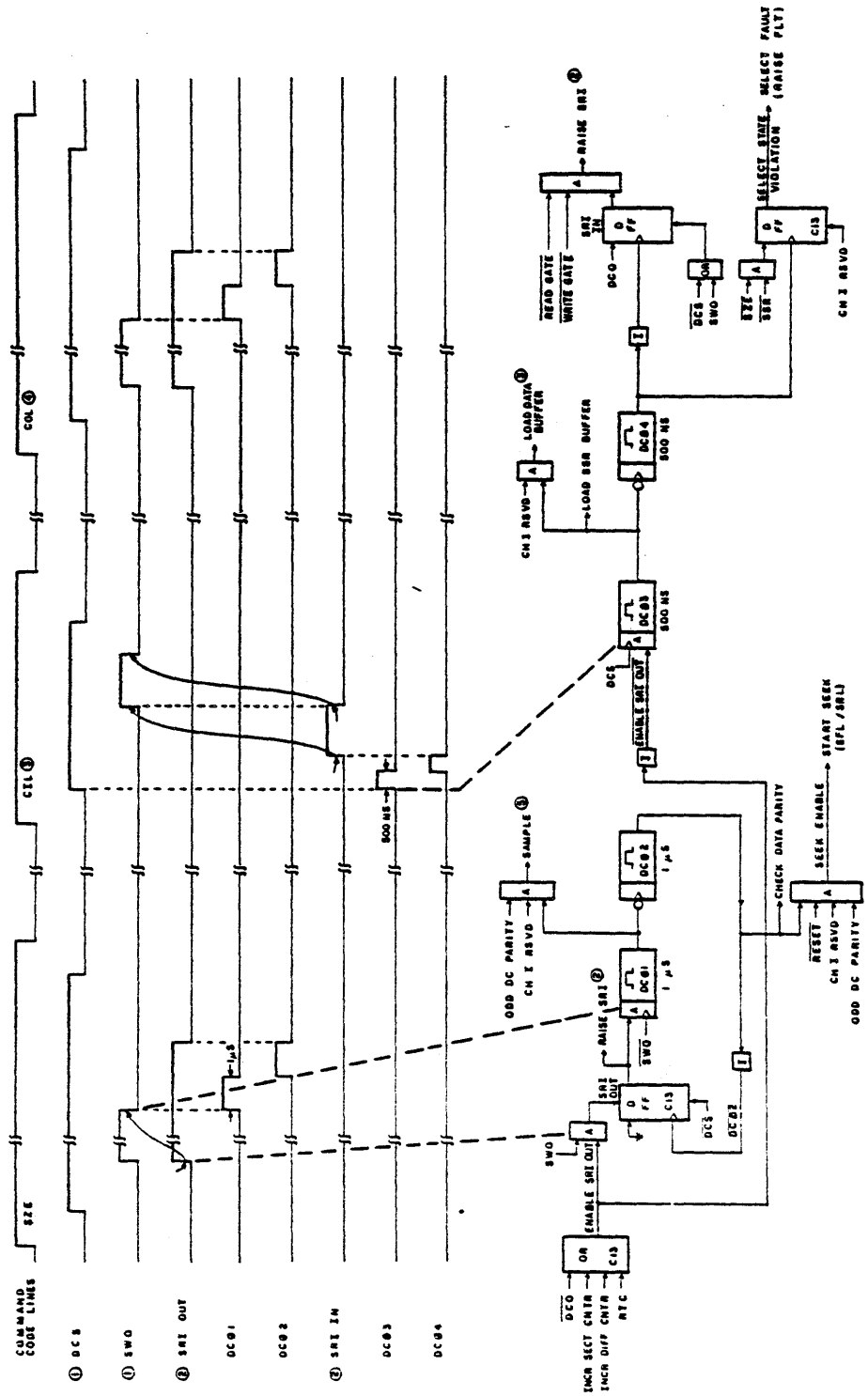
Read or Write operations have a similar, but not identical, Serial Read In/Serial Write Out exchange. Refer to the applicable theory. discussion for further information.

For commands where data is not exchanged (Control Commands), the bidirectional data lines are not sampled for data or parity.

SEEK OPERATIONS

GENERAL

Seek operations are those drive functions that cause a repositioning of the read/write heads. The heads are attached to the actuator which in turn, is moved in a voice coil positioner. The mechanical elements involved in the mechanism are described in the assembly portion of subsection 1A.



NOTES

① CHANNEL TIMING NOT TO SCALE (FOR REFERENCE ONLY). COMMAND SEQUENCE IS FICTIONAL.

② EITHER SRI OUT/IN WILL RAISE SRI. READ/WRITE SRI CONTROL NOT SHOWN.

③ DATA FROM DRIVE → CA. DATA PLACED ON BIDIRECTIONAL LINES AT DC03.

④ DATA FROM CA → DRIVE. DATA PARITY MUST BE ODD AT DC02 OR DO1, ϕ^0 AND DLI FAULT SET.

⑤ EXECUTION FOR MANY COMMANDS STARTS AT SAMPLE TIME.

Figure 3-18. SRI Timing

The discussion on Seek operations is divided into the following areas:

- Servo Circuit Operation - Describes the Servo circuit, which controls the voice coil positioner.
- Basic Seek Operation - Provides a general description of how the drive functions during a seek operation.
- Types of Seeks - Describes the different types of seeks performed by the drive.
- End of Travel Detection - Describes what happens when the drive positions the heads beyond the normal area of travel.
- Seek Status and Error Conditions - Defines certain error conditions related to seek operations.

SERVO CIRCUIT OPERATION

The servo circuit is a closed loop servomechanism used to position the read/write heads. Figure 3-19 is a simplified schematic of the servo circuit. Functions of the major elements of the system are explained in Table 3-4.

A servo loop sums all of the error voltages imposed on it. The loop always attempts to maintain itself at a null. If not nulled, the loop will adjust the correctable device (in this case, the voice coil positioner) to achieve this null. Signals applied to the loop are called error voltages. Two major error voltages are used.

1. A position error: this is the departure of the positioner from the desired position.
2. A feedback signal to modify (or oppose) the position error to cause a smooth motion of the positioner.

The position error signal is provided by the position converter and its allied elements. The amplitude of the signal is proportional to the distance from the present position to the desired position (tracks-to-go). The major feedback signal is the output of the velocity transducer. The amplitude of this signal is proportional to the velocity of the positioner while the phase indicates the direction of motion, forward or reverse.

The loop applies its position and feedback signals to one summing point, the summing amplifier. If the summation of these signals is not equal to zero, the summing amplifier outputs a signal proportional to the amplitude of the error voltage (which signifies the amount of displacement from the desired position) and the phase of the error voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the actuator assembly. The actuator contains a voice coil positioner that supports and moves the read/write heads. In turn, the voice coil is located within a powerful magnet. Whenever a current passes through the voice coil windings, the interaction of the induced emf and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.

TABLE 3-4. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Difference Counter	Holds the complement of the number of tracks yet to be crossed before reaching the desired track or cylinder. When On Cylinder the counter indicates 1023 or 511 for BR3E4/3E5. An associated decoding network provides outputs representative of the current general content of the counter.
Digital To Analog Converter	Monitors the 7 lowest order bits of Difference counter to provide an analog indication of position error the amplitude of which is proportional to the number of tracks to go. The amplitude decreases in discrete steps as last 127 tracks of a seek are crossed.
Desired Velocity Function Generator	Processes Position Error signal at gain levels that vary as position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control of deceleration. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems.

TABLE 3-4. SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Function
Position Converter	Uses the output of the digital to analog converter to develop the coarse position error signal.
Summing Amplifier	Generates a control signal to drive the power amplifier. Control signal based on algebraic summation of Position Error and Velocity Amplifier signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity of 7 ips.
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity of 7 ips.
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement of the retracted position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 127 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Fine Enable and Fine FF	Fine enable monitors integrated velocity. When difference counter is 1022 and fine enable (Velocity integrator output) exceeds 1.28v, it indicates that there is one-half track to go. Fine FF sets to enable fine gate and clear coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine servo (fine gate). Fine also has the following effects: a. Turn on integrator clamp to switch off velocity integrator. b. Enables on cylinder detection. During load or RTZ sequences, both the fine and coarse latches are cleared. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Bit 0 Address Register and FF Slope	Used to select proper track servo signal phase for use as Fine Servo signal (signal controlling servo loop as last track is approached and carriage is stopped). If bit 0 is not set, the seek destination is an even numbered track and the track servo signal will be inverted for use in stopping the carriage. If bit 0 is set, an odd track is identified and track servo is not inverted. Register bit content is placed in Slope FF which performs actual gating.

TABLE 3-4. SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Function
Fine Servo Amplifier	Provides the Fine Servo signal to the On Cylinder Detector. This signal amplitude is proportional to distance that heads are displaced from track centerline. Scale factor is one millivolt per microinch displacement. If heads drift off slightly after seek is completed, track servo signal is no longer null. This becomes fine servo signal to drive heads back into position. Provides the Position Error signal, via the fine gate, to the summing amplifier during the last one-half track of the seek. Amplitude of this signal is proportional to distance-to-go. Phase is selected by Slope FF to be opposite in phase to velocity signal. The combination of the position error and velocity signals controls voice coil current to bring positioner into On Cylinder position.
On Cylinder Detector	Monitors fine servo signal when T<1. When signal is less than about 0.3v, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is generated. If heads overshoot at end of seek so that voltage exceeds 0.7v, delay is reinitiated. Delay permits carriage to settle out before controller may attempt any read/write operations. The On Cylinder Detector is inhibited from triggering for 4.75 ms from the initiation of a Seek Start.

BASIC SEEK OPERATION

Introduction

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see Figure 3-20):

1. Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.

2. Coast Phase: velocity is at its maximum and the positioner velocity is constant.

3. Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.

4. Stop Phase: the positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Accelerate Phase

This phase is controlled largely by the position error signal. The controller loads the difference counter with the complement of the seek length. For example, if the heads are presently on cylinder 10 and must go to cylinder 160, the seek length is 150 cylinders. In binary representation, decimal 150 is 00 1001 0110. The complement of this number is 11 0110 1001, or decimal 873. At each cylinder pulse, the counter is incremented; therefore, the greater the number in the difference counter, the fewer tracks-to-go. The counter is at its maximum value when tracks to go equal zero. This maximum value is 1023 (11 1111 1111) and 511 (01 1111 1111) for the BR3E4/3E5.

The 7 low-order bits of the difference counter are applied to the Digital to Analog (D/A) converter. The value of these bits indicates the position error (or tracks-to-go) from 0 to 128. That is, the amplitude of the D/A converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 128, the D/A converter output is at its maximum value.

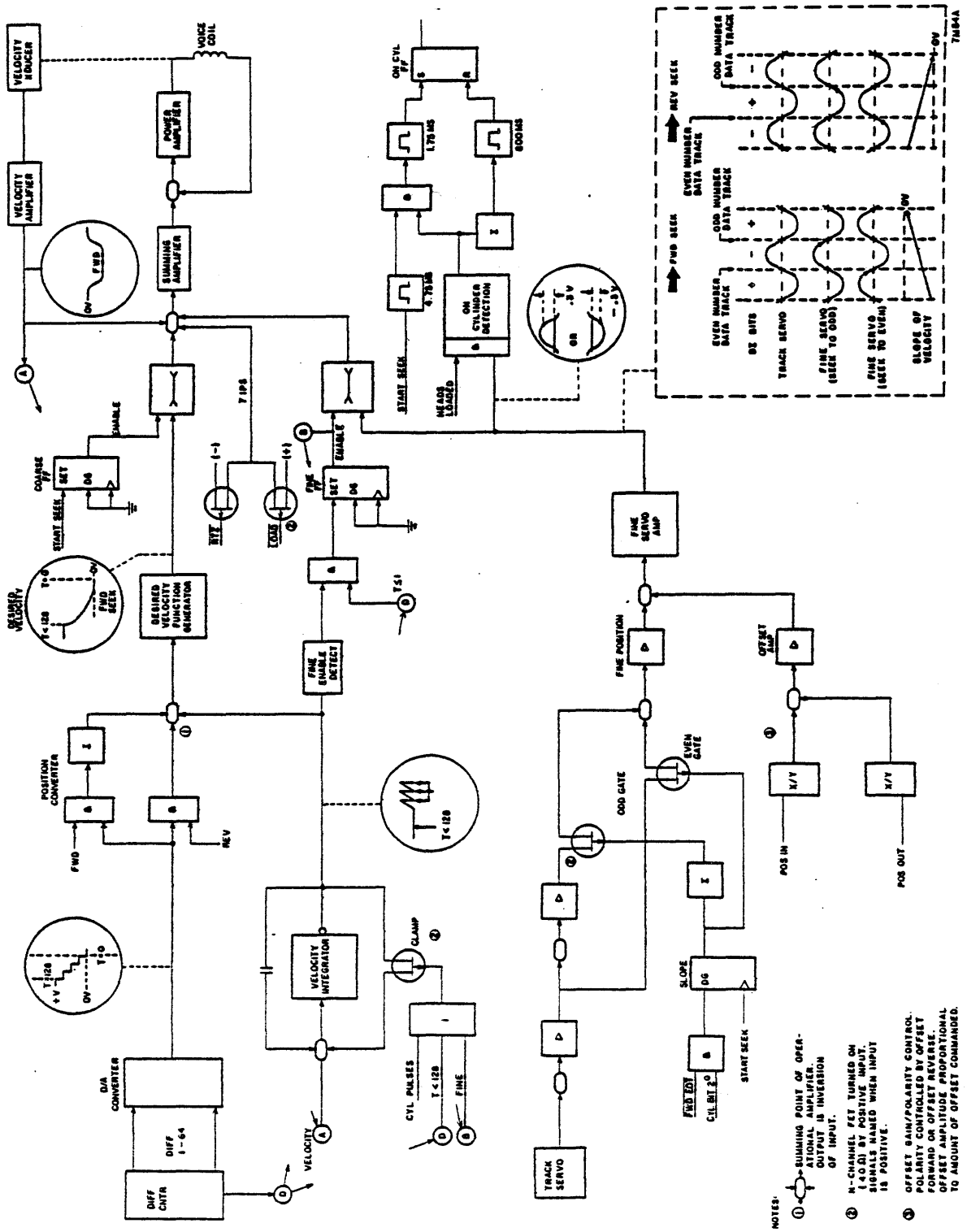
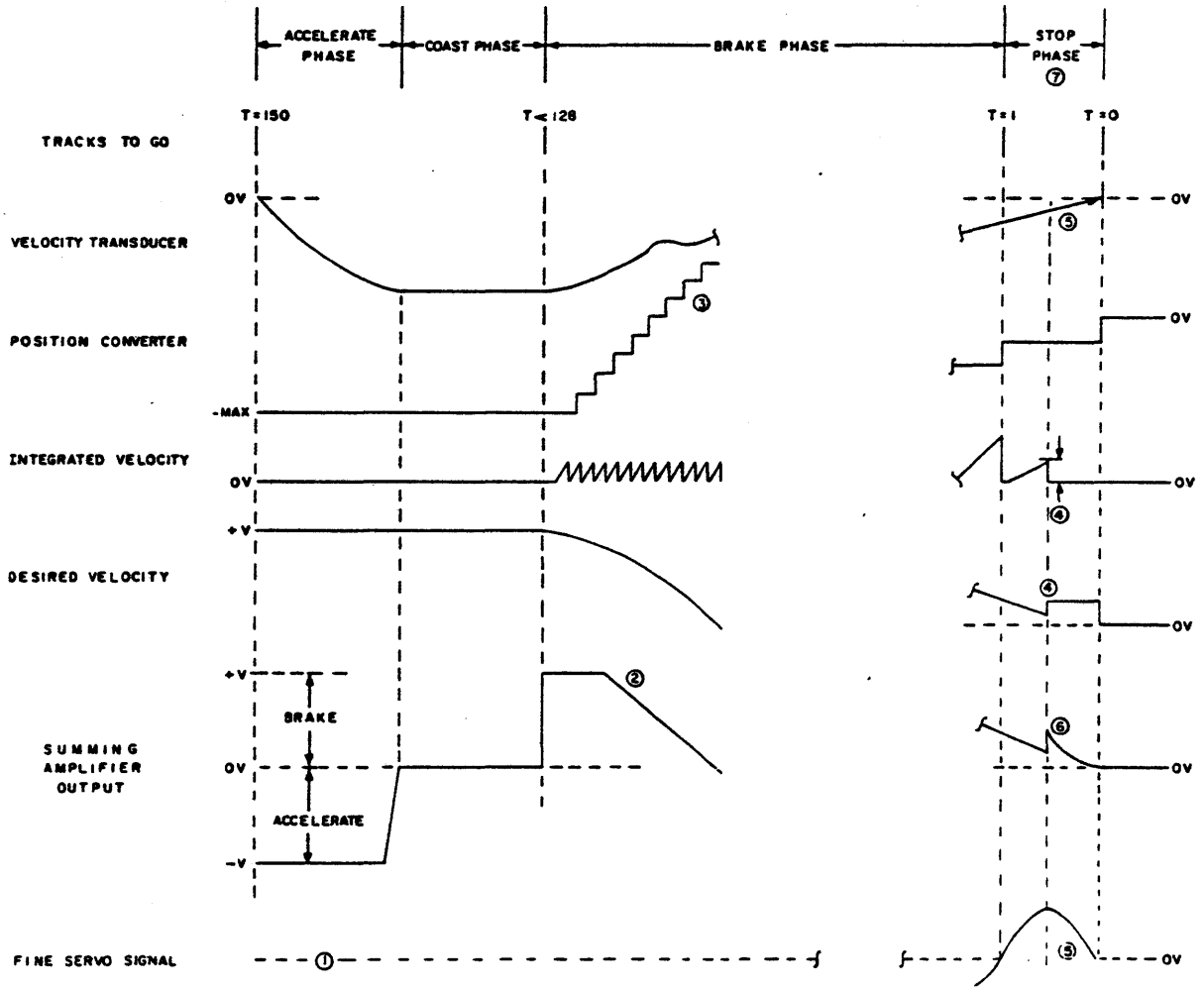


Figure 3-19. Circuit Simplified Schematic



NOTES

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS

② SLOPE DETERMINED BY LOOP GAINS TO PERMIT SERVO CONTROL ALONG DESIRED CURVE.

③ OUTPUT DECREASES WITH EACH CYLINDER PULSE.

④ FINE LATCH SETS WHEN $T \leq 1$ AND INTEGRATED VELOCITY $> 1.28V$. DESIRED VELOCITY HAS NO FURTHER EFFECT.

⑤ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER

⑥ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑦ SCALE CHANGED AT T=1 FOR CLARITY.

8. DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

7M85

Figure 3-20. Servo Circuit Simplified Signals

The output of the D/A converter is applied to the position converter which used it to develop one coarse position error signal. This signal is directly proportional to the D/A converter output and serves as the input to the summing amplifier.

At the beginning of this seek the coarse position signal is maximum so the input to the summing amplifier is a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration. As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less and acceleration continues.

Coast Phase

Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses will tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.

Decelerate Phase

Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each cylinder is passed. These pulses are used to increment the difference counter. When T=64, the position error signal, from the desired velocity function generator is reduced. This causes the velocity signal to dominate and, since it is opposite in phase to the position error, the summing amplifier output switches polarity. Opposing current passes through the voice coil. The carriage decelerates. Both the desired velocity and velocity signals are decreasing simultaneously. Voice coil current decreases proportionately.

The loop maintains speed along an ideal velocity curve. This curve is the analog version of the number of tracks-to-go. The velocity curve is generated by the desired velocity function generator, Its output is compared with velocity to achieve maximum deceleration under all conditions without overshoot. The position signal is the sum of the following:

1. The position error signal from the position converter. Its output is a signal whose amplitude is proportional to the number of tracks-to-go.

2. Integrated velocity from the velocity integrator. Integrating a velocity signal provides a signal proportional to distance. This signal is a sawtooth waveform: it is pulled back to zero by each cylinder pulse and increases in proportion to velocity and time (distance). The combination of the stepping-down output from the position converter with the ramp integrated velocity signal results in a smooth curve of constantly-decreasing magnitude.

3. The function provided by the nonlinear feedback around the desired velocity function generator.

Stop Phase

Stop Phase begins when the difference counter indicates that there is one track-to-go. When T=1, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the Fine FF. Desired velocity is disabled since the coarse gate is opened by Fine being set.

The last half-track of motion is controlled by the fine servo signal. There is a slight increase in position error gain in switching from coarse to fine. Fine servo and velocity are applied to the summing amplifier through the fine gate. The summation of these two signals controls the braking current.

At the start of the seek, the Slope FF is set if the seek is to an odd-numbered cylinder. The slope signal controls the phase of the track servo signal applied to the fine position amplifier. This adjustment is required since track servo signal phasing is a function of the servo head position: the signal is negative when over negative dibits and positive when over positive dibits. Therefore, on forward seeks, the signal is decreasing from a negative value toward zero when approaching a data track with an odd number; it it increasing from a positive value toward zero when approaching a data track with an even number. The opposite is true during a reverse seek.

Phasing of the track servo signal is selected so that the fine servo signal opposes the velocity signal during the last half-track of the seek. Both signals are decreasing. If

either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the fine position signal is less than about 0.3 volt, the positioner is, for all practical purposes, positioned over the data track. This initiates the On Cylinder delay. After 1.75 milliseconds, On Cylinder is generated.

The fine servo signal remains active even though On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move, one dibit signal will increase in amplitude. This results in a slight track servo signal which is translated into the fine servo signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause the fine position signal greater than 0.7 volt for more than 800 microseconds, the On Cylinder signal is lost. This sets Seek Incomplete, Fault, and deselects the heads. If the unit is reading or writing at the time, Pack Unsafe is also set.

The loop also permits positioner offset if the program requires it for error recovery. Shift Position In (Tag 19) command will provide a positive bias input to the fine position amplifier. This is now an error signal to the summing amplifier to cause a motion forward of 400 microinches. The motion stops when the bias voltage and track servo voltage cancel. Shift Position Out (Tag 18) causes a 400-microinch reverse offset. Either offset may also be provided by switches on the maintenance panel. Positioner Busy status is up for 100 milliseconds following receipt of Shift Position Out or Shift Position In. DEN is then generated.

Short Seeks

The preceding explanation of the basic seek operation presumed long seeks that permitted the positioner to attain maximum velocity.

Maximum velocity of about 66 ips requires 70 tracks acceleration time. During short seeks, gating is identical although relative phasing of the error signals will vary. During seeks less than 128 tracks certain signals are available immediately: integrated velocity, non-linear feedback to the desired velocity function generator, and a position converter output not clamped at its maximum value. These signals generate a position error voltage to accelerate the positioner.

The voice coil saturates for a shorter time but the primary function remains unchanged: acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

TYPES OF SEEKS

Introduction

The drive performs 3 basic types of seeks:

- First Seek - Initiated by pressing the START switch, it causes the heads to load and position themselves at cylinder 000.
- Direct (Forward/Reverse) Seek - Performed when the controller commands the drive to move the heads from one location to another.
- Return to Zero Seek - Initiated by the controller it causes the drive to position the heads at cylinder 000.

First Seek(Load)

This function, also known as the Load sequence, involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the unit's logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs. Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlocks are closed. Successful completion of a First Seek is signified by the occurrence of DEN and the lighting of the Unit Number indicator. Standby status (SSR bit 2^5) drops.

Initiation of the function occurs when the START switch is pressed (Figures 3-21 and 3-22). Refer to the power supply discussion in this section for additional sequencing information. Positioner Busy status is available. The logic enables motor relay K3. This causes release of the hysteresis brake and starts the spindle motor. At the same time, the First Seek Interlock is energized to initiate a First Seek Interlock Delay. In S/C 33 and above, the first seek interlock is replaced by circuitry located on the _SAV card.

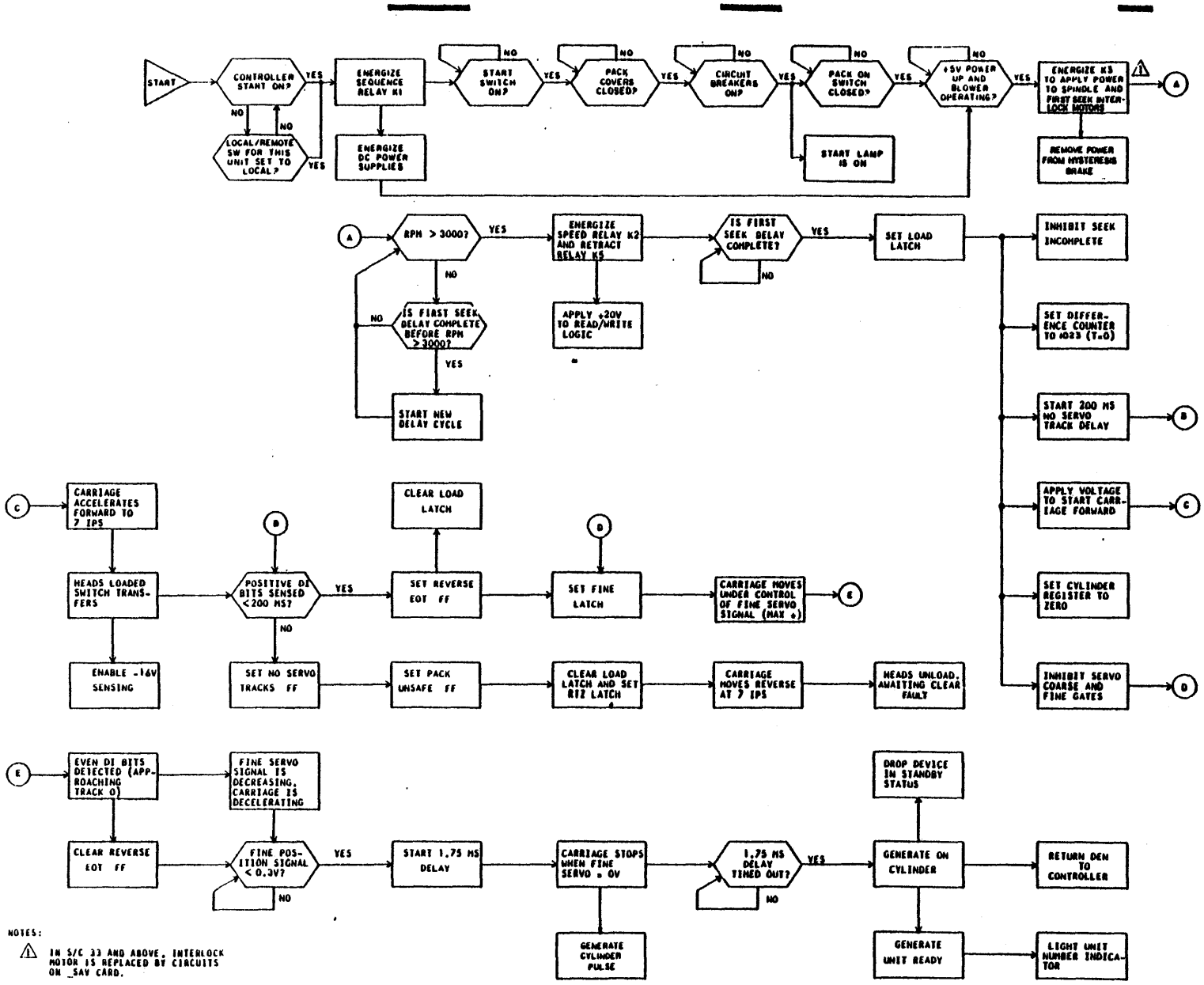
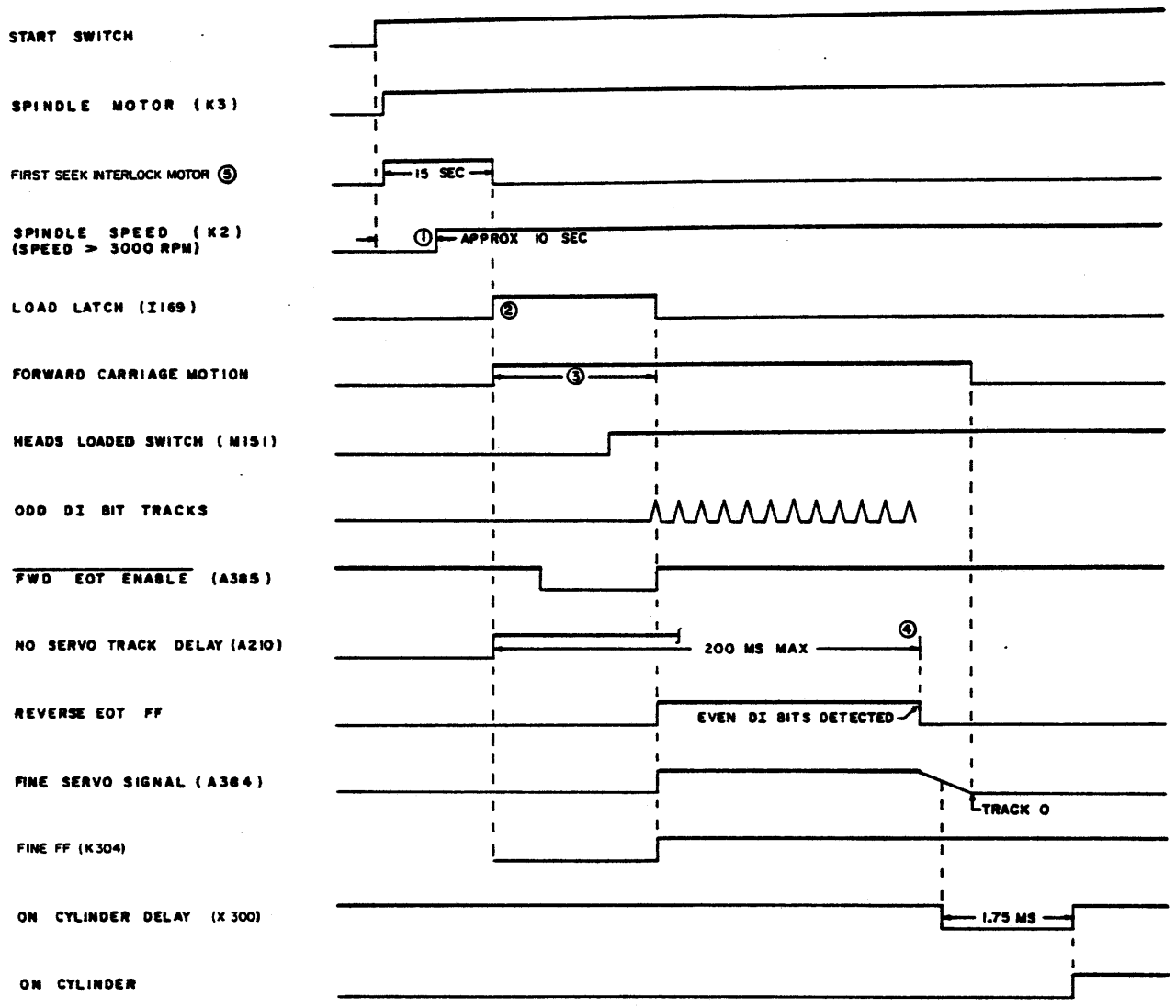


Figure 3-21. First Seek Flow Chart



NOTES:

① RETRACT RELAY K5 PICKED WHEN K2 PICKS.

② LOAD FF CAUSES LOAD GATE (A2903) TO APPLY + (SEEK FWD) VOLTAGE TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (1023).

③ MOTION TO 7 IPS PROVIDED BY LOAD GATE UNTIL ODD DI BITS SET REVERSE EOT FF. MOTION CONTROL THEN PROVIDED BY FINE POSITION SIGNAL.

④ DI BITS MUST BE DETECTED WITHIN 200 MS OR PACK UNSAFE IS SET. HEADS UNLOAD. SELECT LOCK MUST BE CLEARED BEFORE ANOTHER LOAD ATTEMPT CAN BE MADE.

⑤ IN S/C 33 AND ABOVE, INTERLOCK MOTOR IS REPLACED BY CIRCUIT ON _SAV CARD

7M100A

Figure 3-22. First Seek Timing Diagram

When the disk pack speed reaches 3,000 rpm, the power supply relay K2 energizes to apply +20v power to the read/write logic and to energize retract relay K5 (the heads are unloaded) to connect the positioner voice coil to the power amplifier driven by the servo logic.

At the end of the 15 second (approximately) First Seek Interlock Cycle the First Seek Interlock switch transfers and activates the first seek operation by setting the Load latch. In S/C 33 and above, first seek delay circuit on the _SAV card provides the signalthat sets the Load latch. The Load latch drives the Load gate; this bias voltage forces an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibits signals on the track servo or positive, dibits) is sensed, the Load latch is cleared and the Fine gate is enabled. The carriage now servoes into cylinder 000 under control of the fine servo signal.

When the positioner reaches cylinder 000, On Cylinder is generated. This causes the following sequence of events:

1. Unit Ready comes up within the drive.
2. Standby status drops.
3. Positioner Busy status drops.
4. DEN is returned to the controller.
5. With EOT down, Index is available.
6. The drive may respond to any operational command if preceded by a normal seize sequence. However, Seize and Summary Status Request (Tag 28) do not require a prior Unit Ready.

If, for any reason, the dibit signals are not detected by the track servo logic within 200 milliseconds after the Load Latch is set, the RTZ latch will be set. The positioner will retract to the heads unloaded position. In this case, a Pack Unsafe (Device Fault and CHECK indicator on) condition exists to prevent reloading until the CHECK is cleared. The same conditions exist if the dibits are lost for 200 milliseconds after Unit Ready is available. Refer to Seek Status and Error Conditions for other First Seek Errors.

Direct (Forward/Reverse) Seek

Introduction

The Direct Seek function involves those operations that must be performed to move the read/write heads from their present track or cylinder location to the one specified by the controller. This function must be preceded by a Seize command unless the unit is already seized or if it is a single channel device.

The basic principles of the seek operation are explained in the Servo Circuit discussion.

I/O Sequencing

Controller/drive signal interchanges during a seek function from cylinder 10 to cylinder 160 would be as follows (see Figures 3-23 and 3-24):

NOTE

Except as specified below, the actual sequence may be varied without affecting drive operations. This is a typical sequence.

1. Controller raises Cylinder Address in Upper (Tag 22) command.
   a. Drive decodes command.
   b. Bit 2^8 and 2^9 of Cylinder Address Register is placed on bit 2^0 and 2^1 of bidirectional data lines. This bit is on if the positioner is currently at cylinder 256 or above. Since the current address is 10, bit 2^0 and 2^1 are zero.
   c. Drive raises Serial Read In one microsecond after rise of Device Command Strobe. Delays DCØ3 and DCØ4 must time out before Serial Read In is raised. It drops in response to Serial Write Out from the controller.
2. Controller raises Cylinder in Lower (Tag 23) command.
   a. Drive decodes command.
   b. Bits 2^7 through 2^0 of Cylinder Address Register are placed on bidirectional data lines. With current address equal to decimal 10, this byte is 0000 1010.
   c. Drive raises Serial Read In. It drops in response to Serial Write Out.
3. Controller places bit 2^8 and 2^9 of new address on bit 2^0 and 2^1 of bidirectional data lines. Since new address (160) is less than 256, this bit is zero. Controller also raises Cylinder Out Upper (Tag 06) and Serial Write Out.
   a. Drive decodes command.
   b. Drive raises Serial Read In.

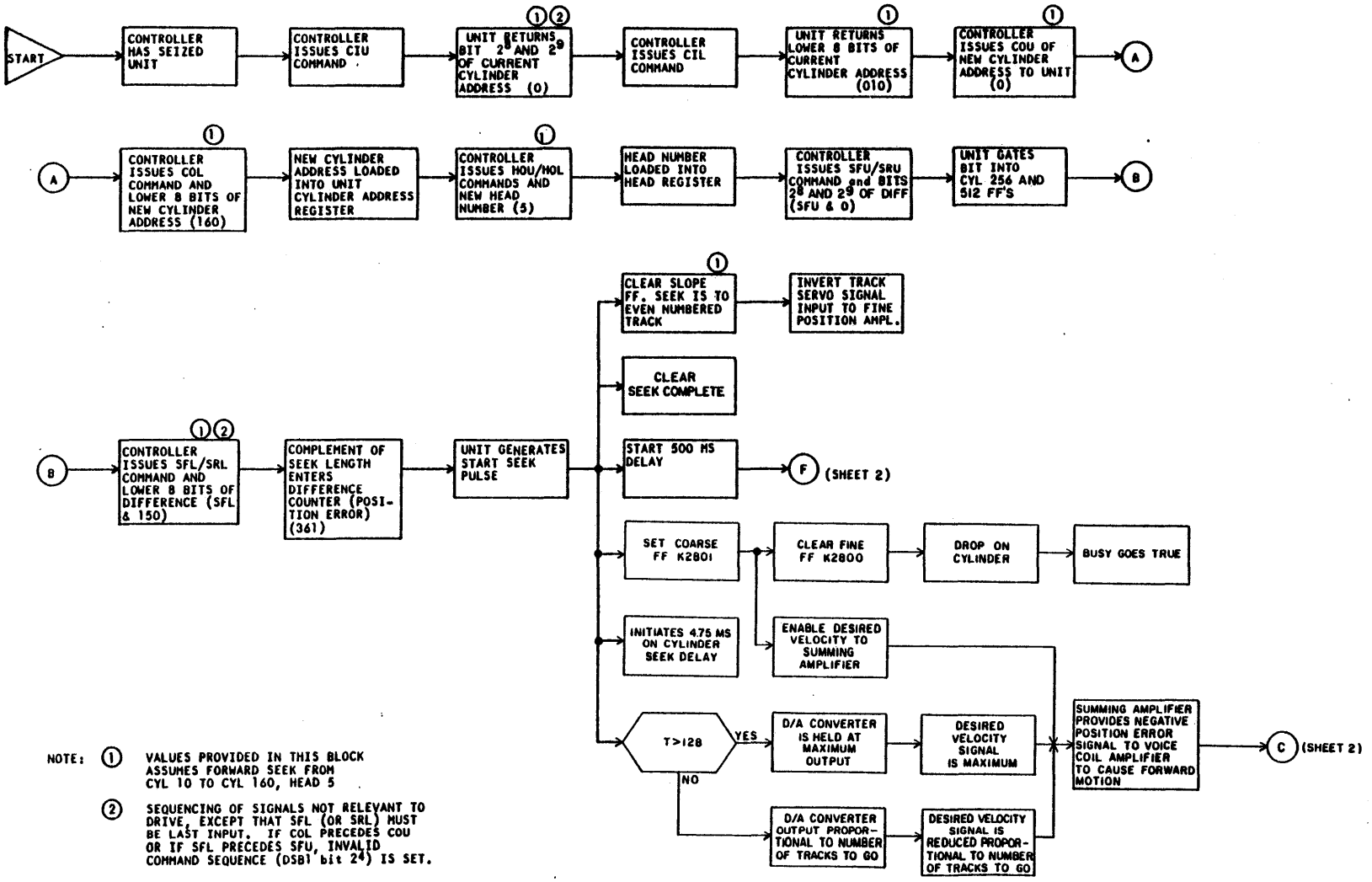


Figure 3-23. Direct Seek Flow Chart (Sheet 1 of 2)

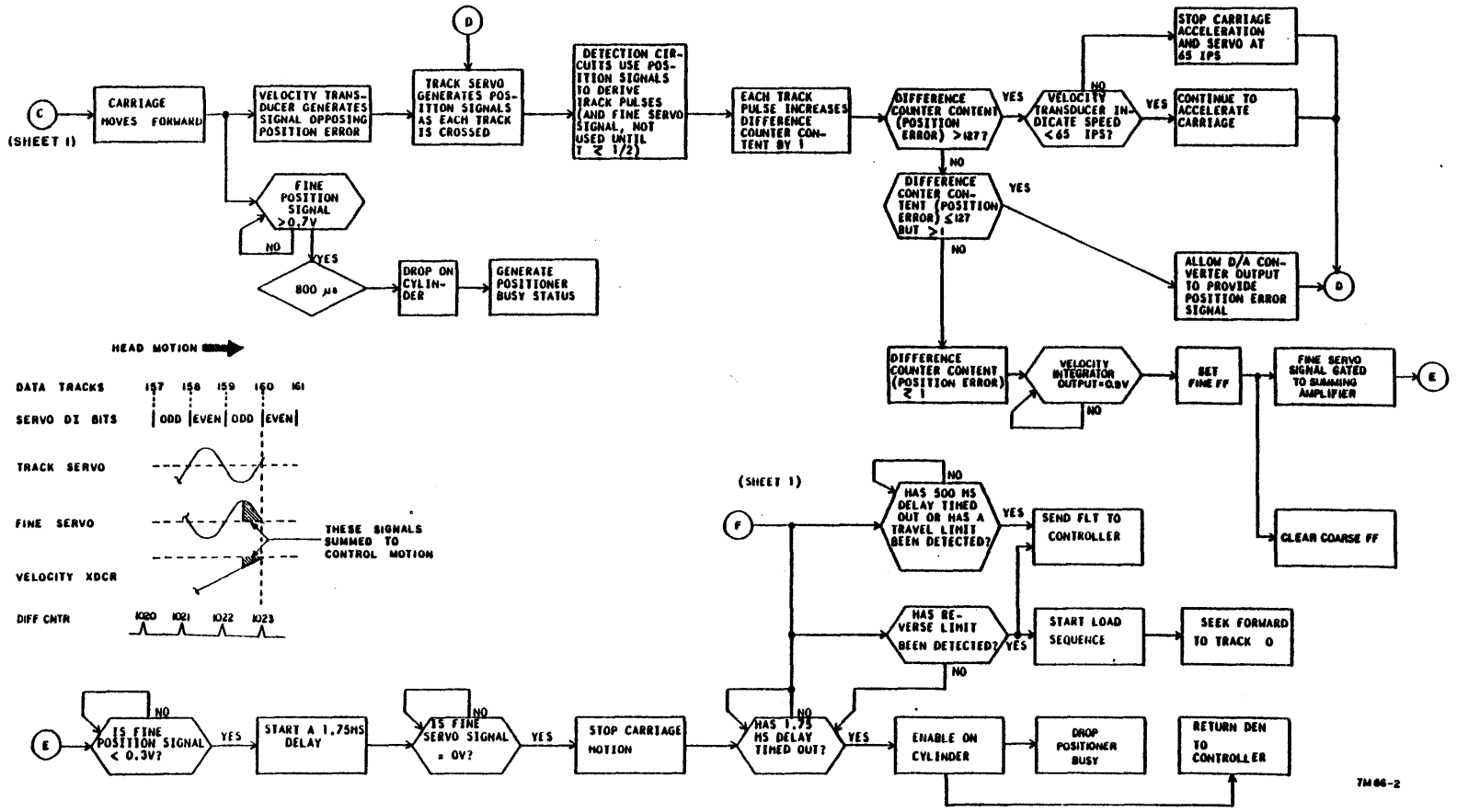
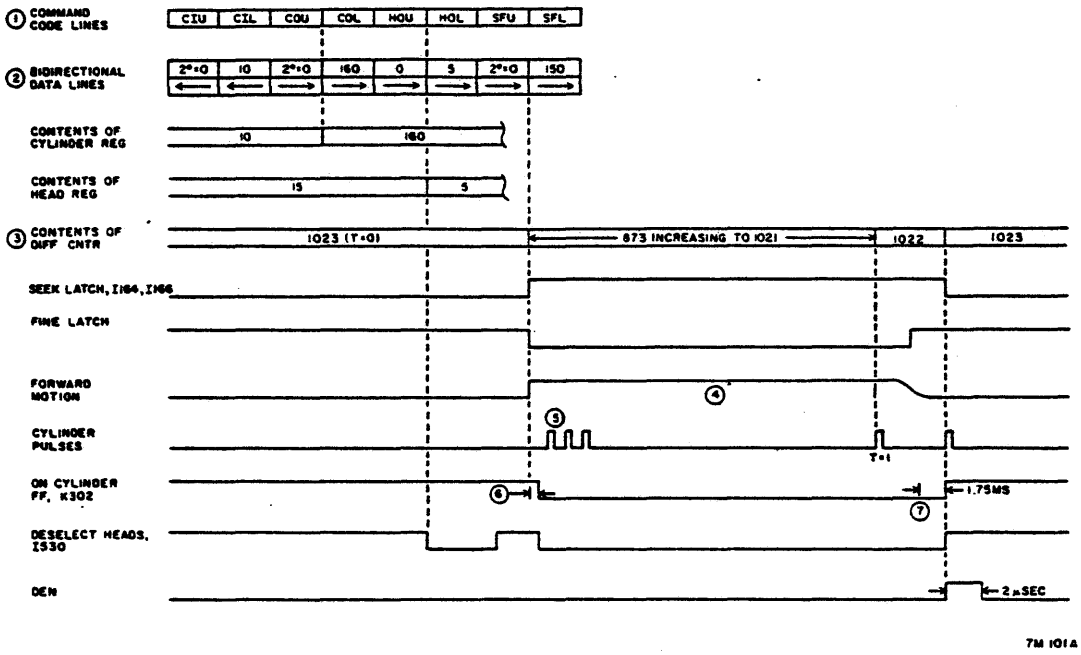


Figure 3-23. Direct Seek Flow Chart (Sheet 2 of 2)

DIRECT FORWARD SEEK FROM TRACK 10 TO TRACK 160, HEAD 05



NOTES:

(1) DCS/SWO/SRI timing not shown. Command loaded at sample time.

(2) Decimal values shown. ← indicates drive to controller → indicates controller to drive.

(3) Difference counter is loaded with complement of seek length. Complement of 150 is 873 it increments with each gated cylinder pulse.

(4) Positioner moves forward under control of position converter. This signal is maximum until number of tracks to go is less than 128. At this point it is stepped down under control of the D/A converter. When approximately 1/2 track remains the Fine FF sets and the position is guided On Cylinder by the Fine Servo signal.

(5) 10 μs cylinder pulse generated with each track crossing. First pulse cannot start sooner than .7 ms from seek start.

(6) On Cylinder drops when Fine FF is cleared.

(7) On Cylinder Delay starts when fine position becomes less than 0.3v (assuming that 4.75 ms delay has timed out).

Figure 3-24. Direct Seek timing

c. Data is entered into the Cyl 256 FF and Cyl 512 FF* when controller drops Serial Write Out (Sample time - DCØ1).

d. FF K1200 is set. Refer to step 4 for this function.

e. Drive drops Serial Read In two microseconds after fall of Serial Write Out.

4. Controller places bits 2^7 through 2^0 of new address on bidirectional data lines. Since new address is decimal 160, this byte is 1010 0000. Controller also raises Cylinder Out Lower (Tag 07) and Serial Write Out.

a. Drive decodes command.

b. Drive raises Serial Read In.

c. FF K1200 clears when controller drops SWO. If Cylinder Out Lower had preceded Cylinder Out Upper or if Cylinder Out Upper were never issued, this FF would set Invalid Command Sequence (bit 2^4 of Detailed Status Byte 1 (Tag 29) and raise DLI Fault. Refer to Seek Status and Error Conditions for additional information.

d. At the same time (DCØ1), contents of bidirectional data lines plus the Cyl 256 FF and Cyl 512 FF * are loaded into drive's Cylinder Address Register. This register is automatically reset to zero by an RTZS function (Recalibrate or Device Initialize) or First Seek.

e. Drive drops Serial Read In two microseconds after fall of Serial Write Out.

5. Controller raises Head Address In Upper (Tag 20) command.

a. Drive decodes command. However, for HIU, the output of the command decoder has no output. Therefore, no data is placed on bidirectional data lines except for parity.

b. Drive raises Serial Read In. It drops in response to Serial Write Out.

6. Controller raises Head Address In Lower (Tag 21) command.

a. Drive decodes command.

b. Bits 2^4 through 2^0 of Head Register are placed on bidirectional data lines. Bits 2^7 through 2^5 are automatically zero.

c. Drive raises Serial Read In. It drops in response to Serial Write Out.

d. There are no restrictions on Head Address In Upper/Head Address In Lower: they may be in any sequence or omitted.

7. Controller raises Head Address Out Upper (Tag 08) command and raises Serial Write Out.

a. Drive decodes command. However, for Head Address Out Upper the output of the command decoder has no output. Therefore, no data is accepted from bidirectional data lines.

b. Drive raises Serial Read In then drops it two microseconds after controller drops Serial Write Out.

8. Controller places new head address on bidirectional data lines and raises Head Address Out Lower and Serial Write Out.

a. Drive decodes command.

b. Drive raises Serial Read In.

c. When controller drops Serial Write Out (Sample time), drive performs steps d and e.

d. Bits 2^4 through 2^0 of bidirectional data lines are loaded into Head Register. High-order bits, if any, are ignored. Head Register is automatically reset to zero by either an RTZS or First Seek function.

f. Drive drops Serial Read In two microseconds after fall of Serial Write Out.

9. Controller computes difference between current address (obtained from Tag 22 and 23) and new address. On a seek from cylinder 10 to 160, the difference (tracks-to-go) is 150. Controller also determines if seek should be forward or reverse.

10. If difference is 256 or more cylinders controller turns on bit 2^0 of bidirectional data lines and will also turn on bit 2^1 if difference is 512* or more cylinders. In this case, the bit is zero. Controller also raises Seek Forward Upper (Tag 02) and Serial Write Out.

a. Drive decodes command.

b. Drive raises Serial Read In.

* Not applicable to BR3E4/3E5.

c. Data bit is entered into the Diff 256 FF and Diff 512 FF*when controller drops Serial Write Out. (Sample time).

d. FF K1200 is set. It functions in this command as it did during steps 3 and 4 to ensure correct command sequencing.

e. Drive drops Serial Read In two microseconds after fall of Serial Write Out.

11. Controller places difference byte on bidirectional data lines. Since the difference is 150, the byte is 1001 0110. Controller also raises Seek Forward Lower (Tag 03) and Serial Write Out.

a. Drive decodes command.

b. Drive raises Serial Read In.

c. Data from bidirectional data lines, Diff 256 FF and Diff 512 FF*is applied to inputs of Difference Counter. It is not gated in until step d. These inputs are complemented by inverting the inputs to the counter. Including bit 2^8 and 2^9, decimal 150 (1001 0110) becomes 873 (11 0110 1001). The Difference Counter increments with each cylinder pulse during the seek; seek length is zero (T=0) when counter is at its maximum count of 1023 or 511 for BR3E4/3E5.

d. When controller drops Serial Write Out Sample time (DCØ1) is up for one microsecond. FF K1200 checks command sequencing and, at the same time, the Difference Counter common enable line gates 873 into the counter.

e. When DCØ1 times out, DCØ2 is up for one microsecond. This is Seek Enable time. The remaining events occur in sequence.

f. Seek Initiate is generated. As long as there is not a Pack Unsafe condition and Unit Ready is up, the Forward FF sets.

g. If the seek length is not zero, the Seek FF sets. On the other hand, with a zero-length seek, Seek FF does not set; Positioner Busy is up for DCØ2 time, followed by DEN.

h. When DCØ2 times out, drive drops Serial Read In. No further controller/drive communications are needed to complete the seek.

*Not applicable to BR3E4/3E5.

12. The following drive events occur with the Seek FF set:

a. The output of the position converter is gated to the desired velocity function generator to generate the Position Error signal. This initiates voice coil amplifier current.

b. A 1.2 microsecond Seek Start pulse is generated.

13. Seek Start initiates the following events:

a. A .500 millisecond delay is triggered. If On Cylinder is not obtained before the delay times out, Seek Incomplete (bit 2^7 of DS3), Device Fault, and FLT are generated.

b. Bit 2^0 of Cylinder Address Register is gated to Slope FF. If this bit is up, seek is to an odd-numbered cylinder. The FF will then be set. The track servo signal is, therefore, inverted before becoming the fine servo signal (position error signal when T < 1) during even seeks.

c. Fine FF is cleared. The position error signal is obtained via the coarse gate.

14. The positioner starts its seek. Refer to Positioner Motion.

15. As the positioner begins to move, the track servo signal increases. This signal functions as the fine position signal in the servo circuit. When it exceeds about 0.7 volt, On Cylinder Enable drops. The following events occur:

a. If On Cylinder Enable is down for more than 800 microseconds, the On Cylinder FF clears. This causes steps b and c.

b. Positioner Busy status is raised.

c. The heads are deselected.

d. The Schmitt triggers driving On Cylinder Enable have hysteresis. Fine position must exceed 0.7 volt to initiate Not On Cylinder while it must be less than 0.3 volt to enable the On Cylinder delay.

16. When the seek is completed and On Cylinder is generated, Positioner Busy status drops. This raises DEN to the controller.

Positioner Motion

The Forward Latch (I156 and I160) ANDed with the Seek Latch (I164, I166) gates the inverted output of the D/A converter (position error signal) into the desired velocity function generator. (A Reverse FF enable would have gated an uninverted position error signal.) Since the seek length is greater than 127 tracks, the D/A converter output is held at a fixed level by the T>128 signal from the Difference counter. Receipt of the Seek Start signal also caused a Start Seek signal to occur. Start Seek clears the Fine FF, so the output of the desired velocity function generator is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no velocity signal exists to balance the position error, and forward motion of the positioner begins.

With the position error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the positioner will continue to accelerate. As the positioner moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse increases the content of the difference counter by one. As accelaration continues, the velocity signal opposes the position error signal by an increasing amount. The input to the summing amplifier drops off, finally becoming zero when these opposing signals are equal. With a nulled input to the summing amplifier, voice coil current is zero. During this phase, the positioner coasts along the 60 ips plateau with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the seek become less than 128 tracks to go, the D/A clamp is disabled for the remainder of the seek (except the last track). As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the position error provided at the desired velocity function generator input is not also stepped, the integrator clamp gates the velocity integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output. This removes the step and provides a nearly smooth curve. As the position error decreases, the summing amplifier control signal decelerates the positioner to keep the velocity signal/position error signal difference to zero.

When the counter indicates one track to go to the desired destination counter = 1023, the integrated velocity signal is reset by the regular cylinder pulse. The integrated velocity, which indicates distance, brings up fine enable when about one-half track of travel remains. This sets the Fine FF which, in turn, clears the Coarse FF.

Desired velocity no longer has an effect; the position error is supplied by the fine servo signal. This signal is the track servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between the present head position and the desired cylinder.

Since the desired destination is track 160, bit 2^0 of the Cylinder Address register is "0". This caused the Slope FF to be cleared at the start of the seek. As a result, the track servo signal is inverted to form the fine servo signal. In all seeks, the fine servo signal is phased to be opposite to the velocity signal. Since, for forward seeks, the velocity signal is positive-going from a negative value toward zero, fine servo must be negative-going toward zero so that these two signals can oppose each other.

The dibit pattern causes a track servo signal to have a positive slope while approaching an even-numbered cylinder. Therefore, the track servo signal must be inverted to serve as a usable fine servo (position error) signal. If the seek had been to an odd cylinder, the Slope FF would have been set and the track servo signal would not have been inverted. As the positioner approaches track 160, the fine servo signal approaches 0v. The summing amplifier responds to this decrease in amplitude by decelerating the positioner so that the sum of the velocity and position error equal zero and all motion stops with the servo circuit at null.

With the Fine FF set, the On Cylinder detection circuit is enabled. It receives the analog signal from the fine servo amplifier. When fine servo is less than about 0.3v, the read/write heads are about 0.0003-inch from nominal data track centerline and On Cylinder Enable comes up. If the 4.75 ms delay initiated at the start of the seek has timed out, the 1.75 ms On Cylinder delay is triggered. When it times out, the On Cylinder FF sets and the heads are selected again to permit Read/Write operations. This causes Positioner Busy to drop, which in turn, forces a DEN to the controller.

Since the positioner is not locked by a mechanical mechanism, the servo circuit continues to be enabled following the seek. If the positioner should drift slightly, the track servo signal decreases. This signal (fine servo), becomes a position error input to the summing amplifier. This drives the positioner back into place.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward and reverse seeks are identical for seeks of equivalent lengths.

Return to Zero Seek (RTZS)

The RTZS function is a Seek where the heads are repositioned to cylinder 000. This function is commanded when the controller issues Recalibrate (Tag 12), Reset Diagnostic Mode (Tag 15), or a DIN. One of these commands is required to clear a Seek Incomplete condition (DS3, bit 2^7). This bit is set if On Cylinder is not generated within 500 milliseconds from the start of the seek, or if On Cylinder is lost. It is also required to clear Positioner Overtravel (Detailed Status Byte 3, bit 2^6). However, the error is cleared only by DIN if a Pack Unsafe (CHECK indicator lighted) condition exists. See Figures 3-25 and 3-26 for Recalibrate (RCB) timing.

The Recalibrate pulse sets the RTZ latch and clears the EOT Seek Error Latch. This enables the RTZ gate; this bias voltage forces an average 7 ips reverse motion of the positioner.

When the positioner passes cylinder 000, no more even dibits are detected. This is the Reverse EOT area. The lack of even dibits inhibits cylinder pulses, allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.28 volts. This sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.28 volts. The RTZ latch is cleared while the Load latch sets. The logic now functions in a manner equivalent to the First Seek sequence.

With the Load latch set, the Load gate supplies a voltage to command a 7 ips forward motion. The velocity integrator, this time indicating forward distance, clears the Load latch to permit continued motion under control of the fine servo signal. The positioner then servoes into cylinder 000.

On Cylinder is available 1.75 milliseconds after the RTZS is completed. The sequence must be completed within 500 milliseconds after RTZS initiation, or else Seek Error is set. On Cylinder drops Positioner Busy. This raises DEN.

The RTZS function is also used during normal power off sequencing. If the controller issues a Set Standby State (Tag 13) command, or if the START switch is pressed by the operator, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 7 ips reverse seek.

This time, however, the EOT Enable circuit is disabled so that the velocity integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload.

The RTZS function occurs automatically to the heads unloaded condition if dibits are lost for more than 200 milliseconds. The Pack Unsafe FF is set to prevent another First Seek until the CHECK indicator has been cleared.

END OF TRAVEL DETECTION

The End of Travel (EOT) circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek to an illegal cylinder past cylinder 822 or 410 for BR3E4/3E5. Sequencing is a follows (See Figure 3-27).

1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The output, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 822 or 410 for BR3E4/3E5 is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.25 volts (4-8 tracks) Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard band, sets the Forward EOT FF.

3. With the Forward EOT FF set:

   a. Seek FF (set the start of the seek) is cleared. This stops the seek function. The output of the position converter in the servo circuit is blocked to indicate a zero position error.

   b. The difference counter is set to 1023 (T=0), or 511 for BR3E4/3E5.

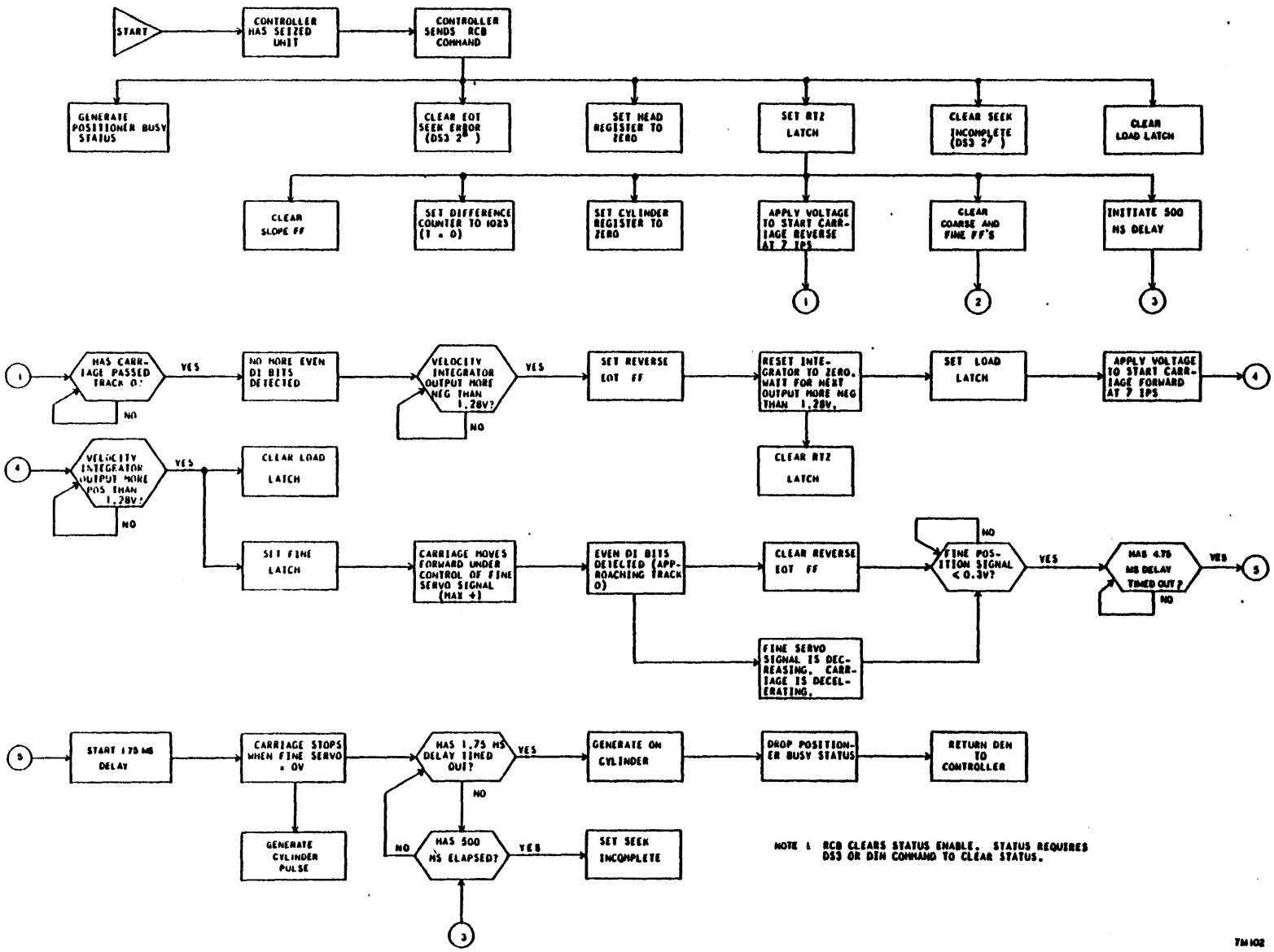
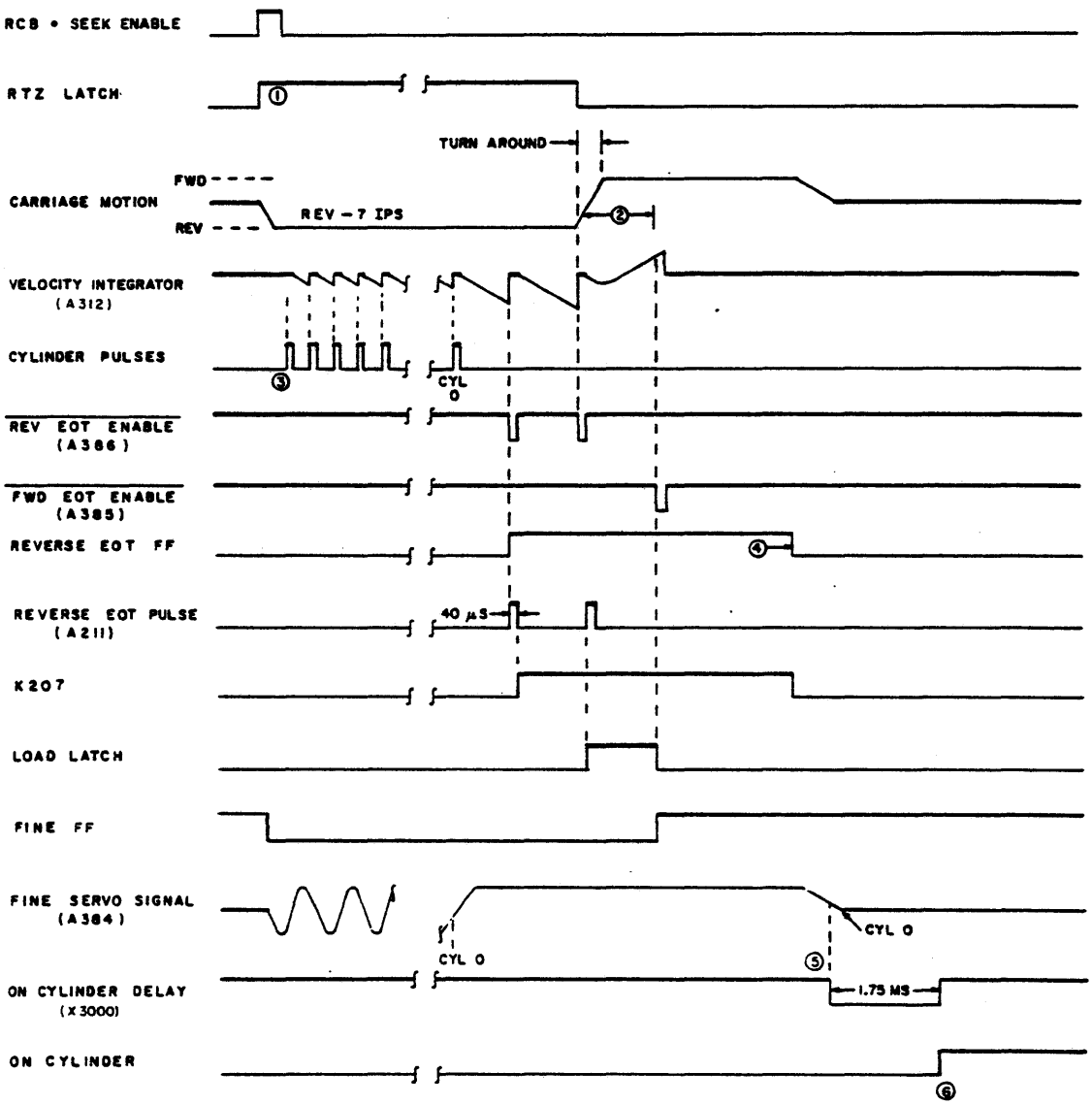


Figure 3-25. RCB Flow Chart



NOTES:

① RTZ LATCH CAUSES RTZ GATE (A29Q) TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (1023)

② FWD MOTION TO 7 IPS PROVIDED BY LOAD GATE (A29Q) _ IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN 01 BITS. (APPROACHING TRACK 0).

⑤ ASSUMES 4.75 MS DELAY HAS TIMED OUT.

⑥ ON CYLINDER DROPS POSITIONER BUSY AND INITIATES DEN.

7MI03

Figure 3-26. RCB Timing Diagram

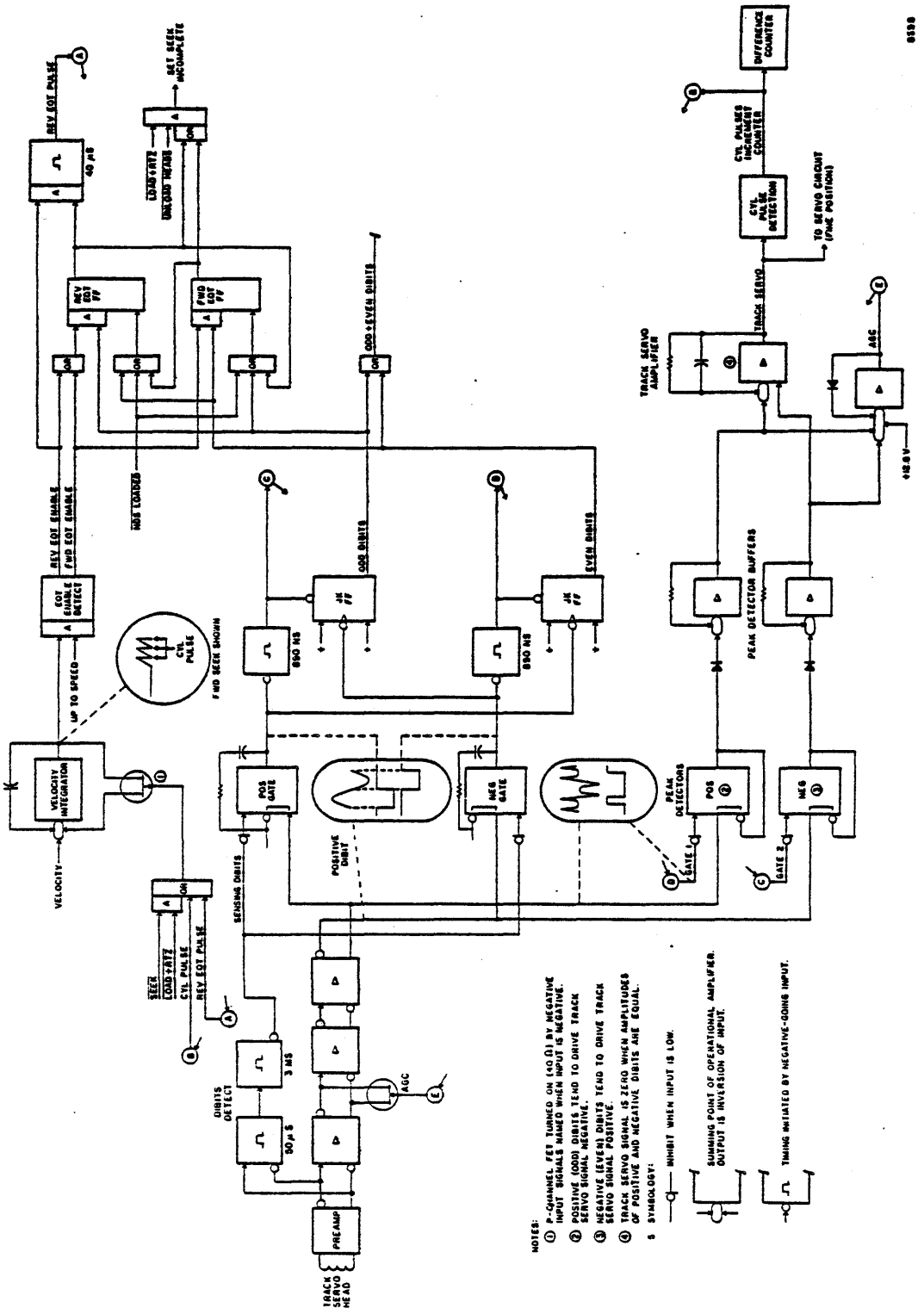


Figure 3-27. Track Servo Circuit Simplified Schematic

c. Fine Enable is raised within the servo circuit.

d. Because of b and c, the Fine gate in the servo circuit is enabled.

e. The Slope FF is cleared to indicate a seek to an even-numbered cylinder.

f. Index counter is reset to zero and held there until the Forward EOT FF is cleared.

g. EOT Seek Error FF sets. This results in steps h through k.

h. Read and Write Gates are disabled.

i. DS3 bit 2^6 (Positioner Overtravel) is set.

j. DLI Fault is generated. Note that Device Fault is not generated.

k. FLT is returned to the controller.

4. The track servo, functioning as the fine servo signal in the servo circuit, is gated to the servo summing amplifier via the Fine Gate. The signal is at a maximum amplitude because only even dibits are being sensed. This error voltage causes the positioner to drift in reverse until the servo signal drops to zero: the heads are then positioned at cylinder 822 or 410 for BR3E4/3E5. The EOT FF is cleared by the odd dibits.

5. The positioner has 500 milliseconds to generate On Cylinder at cylinder 822 or 410, for BR3E4/3E5, for the time that the Forward EOT FF set. If not, Seek Incomplete (DS3 bit 2^7) and Device Fault are also generated.

6. When On Cylinder is generated, Positioner Busy status drops and DEN is returned to the controller.

7. To clear the fault, the controller must issue a Recalibrate or Device Initialize. Status clearing requires a DS3 command.

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to cylinder 000. The same error condition exists, however, as if a forward EOT occurred.

SEEK STATUS AND ERROR CONDITIONS

General

Many of the status bits available for the Summary Status Request (SSR) or Detailed Status (DS) commands are related to the seek functions. These conditions are listed in the following paragraphs. For further information on their effects, refer to Sense Operations.

Normal Status Conditions

The following status conditions are not, in themselves, considered as error conditions. They may, however, shake up the system if there is an element of surprise in them.

Positioner Busy (SSR bit 2^4) is up under any one or more of the following conditions:

1. Unit is not Ready but Stop is down (generally a First Seek sequence).

2. Stop up with heads still loaded (generally a shutdown sequence).

3. Zero length seek in Seek Forward or Seek Reverse Lower.

4. Not On Cylinder.

5. Shift Positioner Out. Shift Positioner In or Return to Centerline command: status is up for 10 milliseconds. Device Event Notification is generated when Position Busy drops.

Device in Standby (SSR, bit 2^5) means that Unit Ready is not up (First Seek completed to On Cylinder) and that stop (SSS or press START switch to turn it off) is up. Unit Ready is not affected by error conditions. This FF remains set until the heads unload.

Forward FF Set (DS4, bit 2^1) is up following and Seek Forward Lower. It remains up until an Seek Reverse Lower is issued. Note that the FF remains up and is not cleared by Recalibrate or other commands. Reverse FF Set (DS4, bit 2^0) is actually the output of the reset side of the Forward FF.

Fine Servo Status (DS4, bit 2^7) indicates that the Fine FF is set. This indicates that the heads are within one-half track of On Cylinder (or already there) or that the unit is in a First Seek or RTZS sequence. Status drops at Start Seek.

Positioner Offset (DS5, bit 2^2) indicates that the unit is still under the influence of Shift Positioner Out or Shift Positioner In.

Device Level Interface Errors (DLI)

The following conditions are considered as DLI Faults (SSR, bit 2^3). FLT is also generated.

Invalid Command Sequence (DS1, bit 2^4) is the result of Seek Forward Lower preceding Seek

Forward Upper, Seek Reverse Lower preceding Seek Reverse Upper or Cylinder Out Lower preceding Cylinder Out Upper.

State Violation (DS1, bit 2^3) results from any of the following:

1. WRT or WRT TEST while not On Cylinder.
2. Set Diagnostic Escape with Positioner Busy.
3. Positioner Busy and any one of several commands (seeks, WRT, etc.)
4. Standby mode (Not Unit Ready) and any one of several commands.
5. Positioner Overtravel (DS3, bit 2^6) occurs if the positioner moved into the forward or reverse End of Travel area. This may be considered as a DLI Fault since this most likely occurs if the Seek Forward Lower or Seek Reverse Lower command called for an excessive seek length.

Device Fault Conditions

The following conditions are considered as Device Failures (SSR, bit 2^1). FLT is also generated.

Loss of Voltage (DS2, bit 2^0) can occur if -16 volt emergency retract voltage is insufficient with the heads loaded. This also causes retract relay K5 to open, retracting the positioner to unload the heads. The Pack Unsafe FF sets; the CHECK Indicator Lights.

Spindle Speed Loss (DS2, bit 2^2) indicates that speed dropped below 3000 rpm with the heads loaded. This opens speed relay K2 which, in turn, opens retract relay K5 to retract the heads. If speed recovers, the heads reload. Insufficient speed prior to heads loading prevents K2 from setting: First Seek Interlock cycles are continuous and the heads never load.

If no head is selected (Head Address Register contains head 19 or greater), Current Fault is generated. This causes the following:

1. Pack Unsafe FF sets the light the CHECK indicator. Heads do not unload.
2. No or Multiple Head Selection (DS2, bit 2^4) is on.

Read or Write Gate up while not On Cylinder sets the Pack Unsafe FF and lights the CHECK indicator.

Seek Incomplete (DS3, bit 2^0) sets if On Cylinder is not obtained within 500 milliseconds after the initiation of a seek or RTZ function. It also sets if On Cylinder is lost without seek initiation.

If dibits are not sensed within 200 milliseconds after the Load latch sets, or if they are lost for 200 milliseconds after the heads are loaded, the No Servo Track FF sets. This causes the following:

1. Pack Unsafe FF sets to light the CHECK indicator.
2. RTZ latch sets to start an RTZS.
3. With the Pack Unsafe condition, the Load latch cannot set. (It normally sets during an RTZ in the reverse EOT area, causing a seek forward to cylinder 000). Therefore, the heads just keep going at 7 ips until they unload.

With a Pack Unsafe condition, the drive will not initiate a First Seek condition (pressing START). Nor will it accept a Seek Forward Lower, Seek Reverse Lower, Recalibrate or Reset Diagnostic command. The unsafe must be cleared by pressing the CHECK indicator or by a Device Initialize. Note that a Pack Unsafe unloads the heads only if dibits are lost or if -16 volt emergency retract power becomes insufficient. All other CHECK conditions will effectively freeze the positioner and lock out any further reads or writes.

TRACK SERVO CIRCUIT

GENERAL

The track servo circuit (Figure 3-27) provides head positioning information. The signals generated by this circuit:

1. Generate a track servo signal that indicates the displacement of the heads from their nominal track centerline.
2. Generate indications that the heads are positioned outside of the normal data cylinders.
3. Generate cylinder pulses during seeks to indicate each cylinder crossing.
4. Provides signals used as the basic 806 kHz clock.

Information for this circuit is derived from the track servo head (Figure 3-28). This head is physically similar to the read/write heads, except that it does not write. The

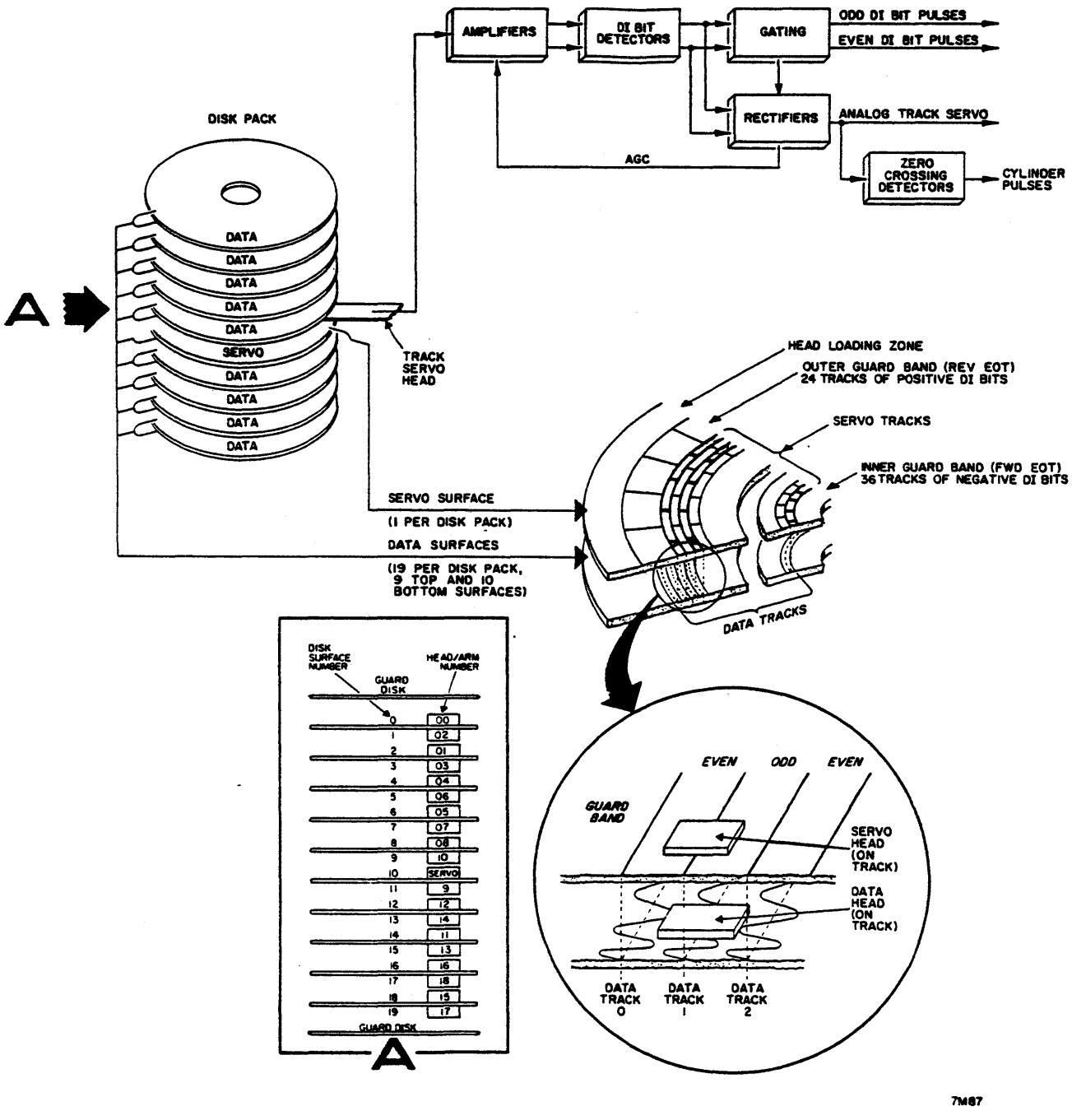


Figure 3-28. Disk Surface Layout

head reads information from the servo track surface of the disk pack. This information is known as dibits: dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the other 19 disk pack recording surfaces.

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

At the outer edge of the servo surface is a band of positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. Then, there are servo tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

The basic elements of the track servo circuit are illustrated in Figure 3-27. Table 3-5 explains the track servo circuit functions.

DIBIT GATING

After being differentially amplified, the servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (Figure 3-29). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform.

The dibits are analyzed by the positive and negative gates. Each gate output switches to the low state when it senses its respective dibit. The negative-going pulses control single-shots and JK FF's to generate the odd/even dibits.

The even/odd dibits are used to enable the EOT detection circuit and to generate the basic machine clock signal.

TRACK SERVO SIGNAL GENERATION

The servo signal is generated by peak detectors that monitor their respective dibits. The positive peak detector (Figure 3-29) provides an output proportional to the amplitude of the positive dibits. It senses only the positive waveform of positive dibits: Gate 1 low inhibits it from reacting to either the negative waveform of positive dibits or the entire negative dibit. An RC network integrates the peak detector output to provide a smooth output. The resulting signal output is greatest, therefore, when the servo head is centered over an odd dibit track.

The negative gate works in a similar manner.

The servo signal is provided by a summing amplifier. It receives inputs from the peak detectors. (The positive peak detector output is first inverted.) Therefore, the output represents the difference between the two peak detector outputs.

The track servo signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine servo signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

Circuit gain control is achieved by applying the outputs from the peak detector buffers to the AGC summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the AGC voltage. This signal is fed back to the AGC amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the AGC, the less the resistance; therefore, more of the signal from the track servo head is shunted by the FET to reduce circuit gain.

The Dibits Detect One Shots (A336 and A337) prevent the circuit from being turned on by random noise spikes while the heads are unloaded or being loaded. When the preamp

TABLE 3-5. TRACK SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Track Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This triggers the Odd Dibit FF. The positive gate also serves as an inhibit to the positive peak detector during the negative portion of the positive dibit and the entire negative dibit. The negative delay functions in the reverse condition.
Even Dibits and Odd Dibits Flips-Flops	Provides 600-nsec pulses indicating dibits. Frequency of each one-shot is 403 kHz.
Dibits Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibits amplifiers: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - peak detector are equal. As head moves from center position, output from one peak detector increases negatively while output from the other peak detector becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportiol to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Track Servo Amplifier	Provides signal proportional to sum of + and - dibit peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.
Cylinder Pulse Detection	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).
Velocity Integrator	Provides ramp signal proportional to distance travelled (velocity integrated with time). Output is positive-going during forward seek; negative-going during reverse seek. Output is pulled back to zero to re-initiate integrator function by each cylinder pulse, or during certain conditions of RTZ or Load sequences.

TABLE 3-4. TRACK SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Function
Dibits Detect	50 µsec and 3 ms delays used to prevent the track servo circuit from being turned on by random noise spikes during a heads unloaded condition or a load heads operation.
End of Travel (EOT)	Monitors integrated velocity to enable EOT circuit. When velocity integrator output exceeds about 1.2v, heads have moved a distance of approximately two tracks without sensing any cylinder pulses.
Reverse EOT FF	Indicates that heads are positioned over outer guard band. Refer to First Seek and RTZS discussions for further details.
Forward EOT FF	Indicates that heads are positioned over inner guard band. This is an error condition.

output is zero, as in a heads unloaded condition, A336 is not triggered and its output is high. This holds A337 at a logic zero. The positive and negative gates and cylinder detect circuits are now inhibited.

When the heads are loaded and dibits are outputed from the preamp, A336 is triggered and retriggered, keeping its output at a logic zero. This releases the timing components of A337 and after 3 ms its output goes to one turning on the Track Servo circuit. If dibits are lost for more than 50 µsec, A336 times out and resets A337 to a logic zero, disabling the Track Servo circuit (See Figure 3-30).

CYLINDER PULSE GENERATION

As the servo head crosses the interface of the even/odd dibit tracks (Figure 3-31), the servo signal decreases toward null. Two operational amplifiers connected as Schmitt triggers switch state. The hysteresis designed into the circuit causes both triggers to be up only while the servo signal is between 0v and 0.4v. These signals are applied to two level shifters (A364/A365). Their outputs are ANDed together to provide a 10 microsecond cylinder pulse. Each cylinder pulse:

1. Increments the difference counter.
2. Switches the two velocity integrators (one each in the servo circuit and track servo circuit) to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 1022 or 510 for BR3E4/3E5. The On Cylinder signal provides a pulse to increase the difference counter to 1023 or 511 for BR3E4/3E5. With the difference counter at 1023 or 511 for BR3E4/3E5 tracks to go equal zero and On Cylinder is available so Positioner Busy status drops.

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine servo signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

MACHINE CLOCK CIRCUIT

GENERAL

The machine clock circuit uses dibits generated by the track servo circuit to generate the basic 806 kHz clock signal. This signal is applied to the following circuits:

1. Index detection
2. Write clock generator
3. Sector counter

CLOCK GENERATION

The circuits (Figure 3-32) most important portion is a phase locked loop (PLL). The loop compares the frequency of input data (dibits) with feedback data. A comparator circuit generates a square wave input to a GJK circuit in the voltage controlled oscillator. (Refer to Section 6 for an explanation of the GJK circuit.) The GJK generates a voltage proportional to the difference in frequency between input data and feedback data. The output of the GJK is applied to the voltage controlled oscillator to control its frequency. The PLL is satisfied when the input and feedback frequencies are identical. Note that data and feedback are 90 degrees out of phase.

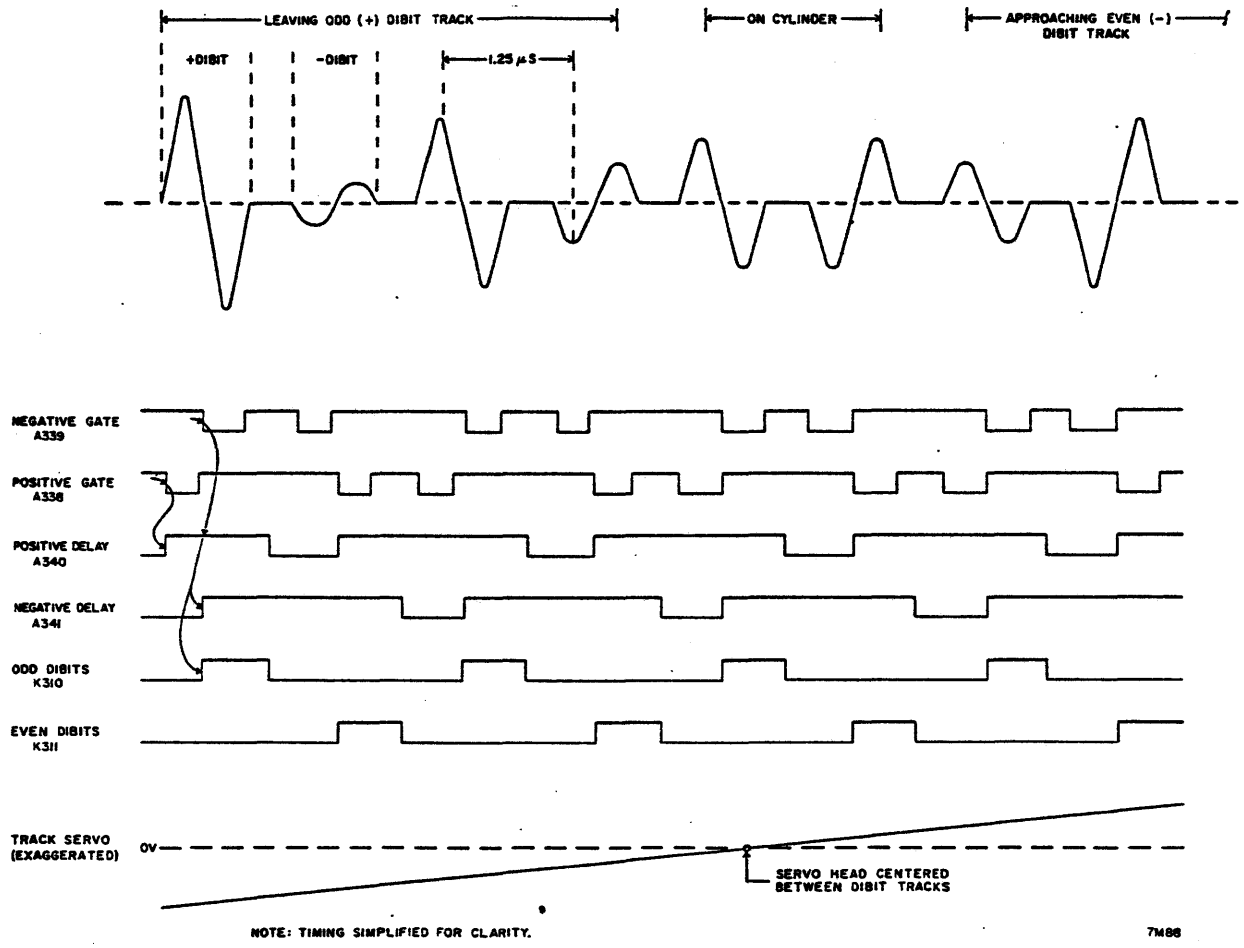


Figure 3-29. Track Servo and Dibits Detect Circuit Simplified Signals

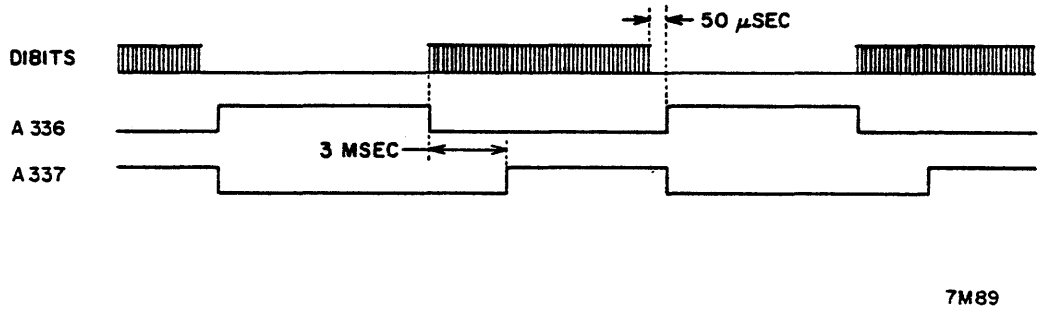
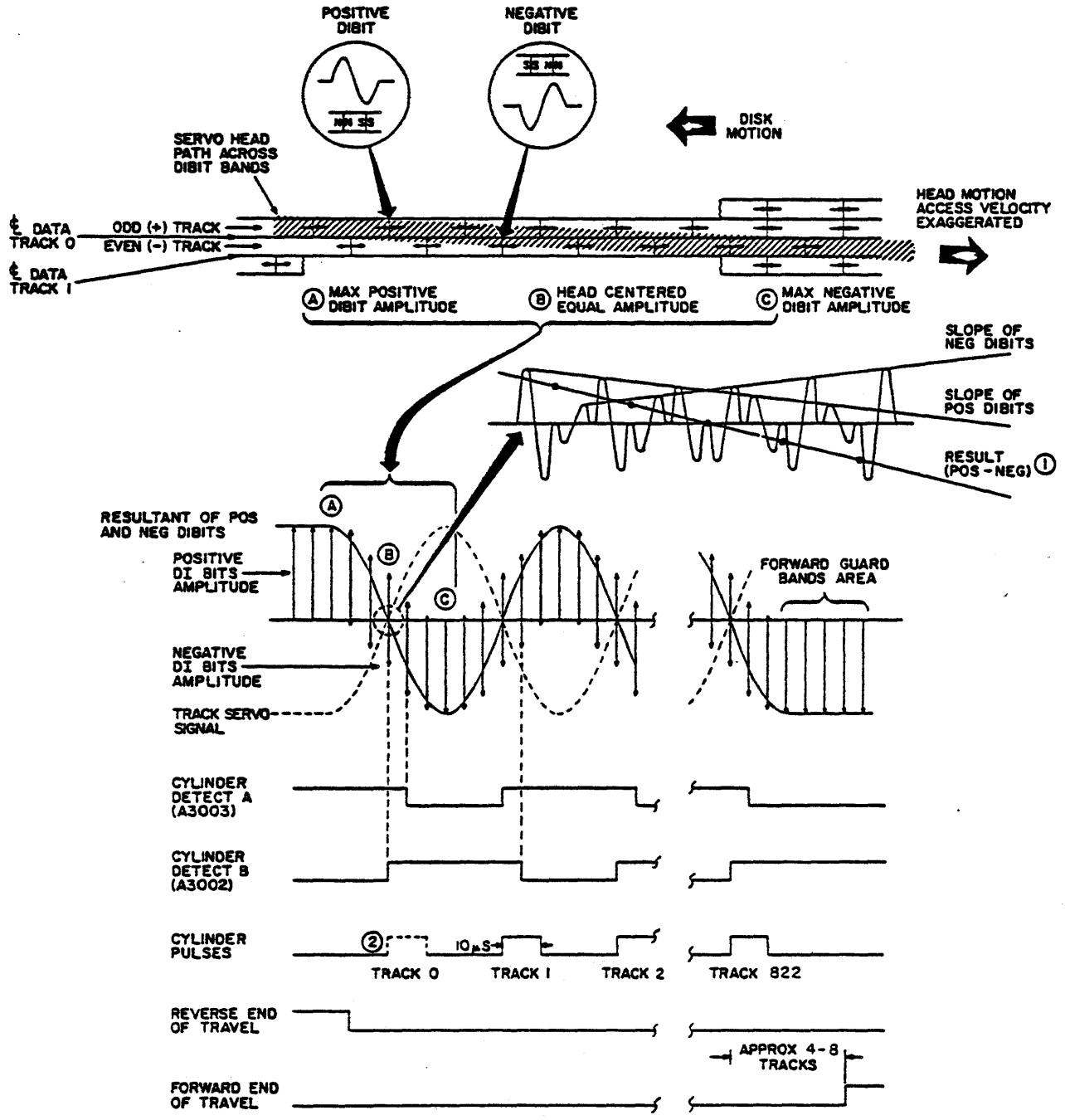


Figure 3-30. Dibits Detect



NOTES: (1) TRACK SERVO SIGNAL (A2503) IS 180° OUT-OF-PHASE WITH THIS WAVEFORM.
(2) CYL PULSE DOES NOT AFFECT DIFFERENCE COUNTER AT TRACK 0 FOR FIRST SEEK.

7M90

Figure 3-31. Cylinder Pulses Generation

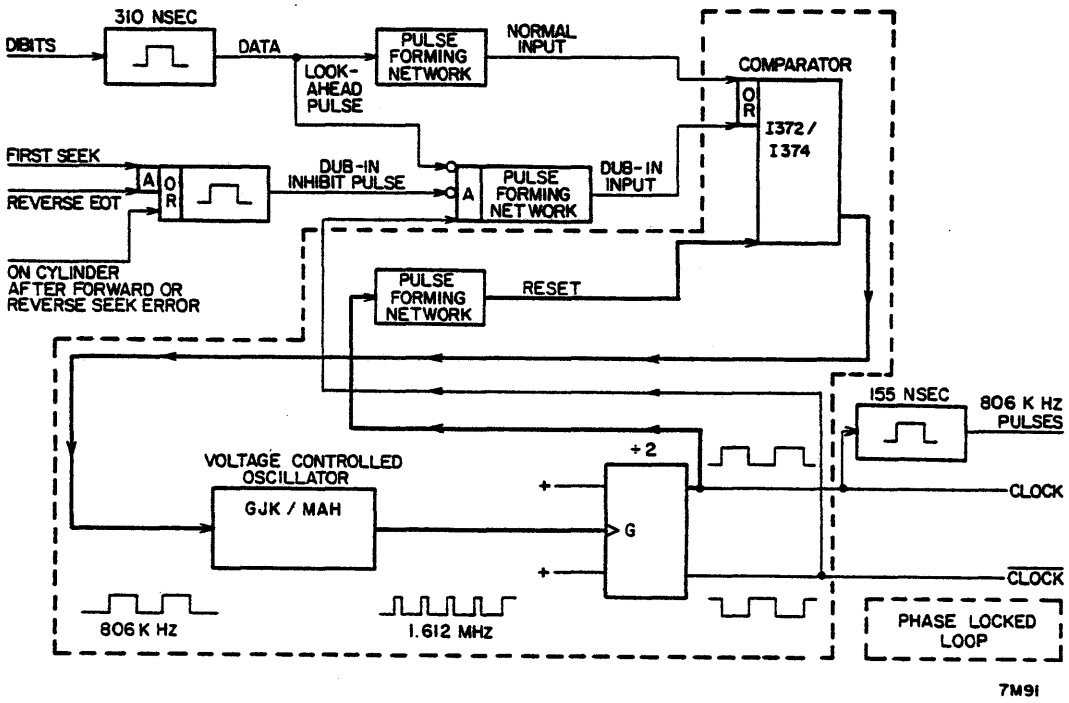


Figure 3-32. Machine Clock Circuit

There are three inputs to the comparator. One is the normal input from dibits delayed approximately 1/4 cell and shaped to 30 nsec (approximate) pulses. The second input is a dub-in input. This is a 30 nsec pulse coming up at the same time as the normal input but from the clock output. The third input is the reset pulse. It is the normal and the reset input which provide the basis for normal comparator operation.

During normal operation, a look-ahead pulse blocks the dub-in input to the comparator. This insures that the comparator and therefore the clock, tracks with the real input data from dibits. However, if dibits are missing, as they are during the index mark (for two cells) or during a seek (every other cell), there must be a pseudo-dibit or dub-in pulse to keep the clock in phase. Therefore, the circuit is self-ringing when data is not present at the input.

A problem with the self-ringing feature of the circuit is that, if the first input to the comparator is not data but a dub-in pulse, the circuit may not be in synchronization with real data when it is received. It would then take some time before synchronization could be attained. The 5 ms dub-in inhibit pulse fires to block dub-in pulses in three situations: 1) when the latch is cleared by reverse EOT at the end of a first seek, or 2) and 3) when On Cylinder is received after a forward or reverse seek error.

After the heads are loaded, even/odd dibits are available. Their nominal frequency is 806 kHz. The actual frequency is a function of spindle motor speed. The PLL quickly synchronizes itself to the actual dibit rate. This permits the clock to react to variations in spindle speed between drives. Signals derived from this circuit, such as sectors, are a function of actual spindle speed rather than functions of an absolute time base.

FF K351 is connected as a divide-by-two circuit. This circuit arrangement permits the PLL feedback to be a function of negative-going edges of the PLL output. Therefore, PLL unsymetrical outputs are ignored and the basic frequency is the controlling factor. The PLL output frequency is nominally 1.612 MHz.

WRITE CLOCK

Write Clock is derived directly from the basic 806 kHz clock. Three phase lock oscillators and a divide by two flip-flop generate the basic 6.44 MHz clock signal to the write circuitry. The frequency is gradually increased to permit the generation of stable pulses.

INDEX DETECTION CIRCUIT

The Index detection circuit (Figure 3-33) generates a 2-microsecond pulse at the start of each new logical track. This signal is returned to the controller as Index Mark and also resets the sector counter to zero.

Prior to reaching the Index area, both even and odd dibits are available. Dibits Present FF (K705) is held in the preset state. Gate I707 is held at a continuous low state: this causes the counter to be continually loaded with zero with each clock pulse from A708.

The Index pattern is the special pattern of missing dibits illustrated in Figure 3-33. Flip-flop K705 clears, allowing the counter to increment with each 806 kHz pulse via A708. The counter can continue to increment only if the precise pattern continues to be sensed. Any other combination of missing dibits (such as when tracks are crossed during seeks) will cause the counter to be reset to zero.

When the counter reaches a decoded value of 5, two of the three input gates to Index Set FF K706 are available. The next even dibit triggers A708 to set the FF. In turn, A707 provides a 2-microsecond Index pulse.

Note that Index is inhibited while the heads are over either a forward or reverse EOT area.

SECTOR CIRCUIT

The sector circuit (Figure 3-34) permits the controller to determine the current angular position (sector) of the read/write heads with respect to Index. The number may be obtained by an Angular Position In (Tag 24) command. This command is one of the few commands that may be issued during either diagnostic or regular operations. Note that this command cannot be used to generate an interrupt when a select sector is reached; it can only determine the sector available at the time that Angular Position In is issued. The count transmitted on the DLI remains frozen until Angular Position In drops.

Each track may be considered as subdivided into 128 segments of equal size. They are numbered from 000 to 127. Sector 000 is the first sector following Index.

The 806 kHz clock signal is used to generate the sector count. Each positive-going clock pulse increments a divide by 104 counter. When the counter reaches 104, the sector counter is incremented by one. The divide by 104 counter restarts from zero; the process continues so that every 104 odd/even dibits increases the sector counter by one.

When the sector counter equals 127, the divide by 104 counter can no longer increment the sector counter. Index should occur at this time to reset both counters.

If Index occurs before the sector counter reaches 127, the counter is malfunctioning. This sets Rotational Position Sensing (RPS) Error, which is bit 2^3 of DS3.

The sector register is unaffected during sector counter operations. The contents of the sector counter are gated into the sector register when API is issued. Angular Position In (Tag 24). The register remains at the same value until the next Angular Position In. The sector counter continues to operate normally.

During diagnostic operations (Set Diagnostic Escape Latch set), the sector counter continues to operate but it cannot be gated into the sector register. The register is reset by Set Diagnostic Escape (Tag 1F) and incremented by an Incr Sector Counter command (Tag 33). Its value may then be determined by Angular Position In.

READ/WRITE OPERATIONS

GENERAL

The drive processes the read/write data transferred between the disk pack and controller.

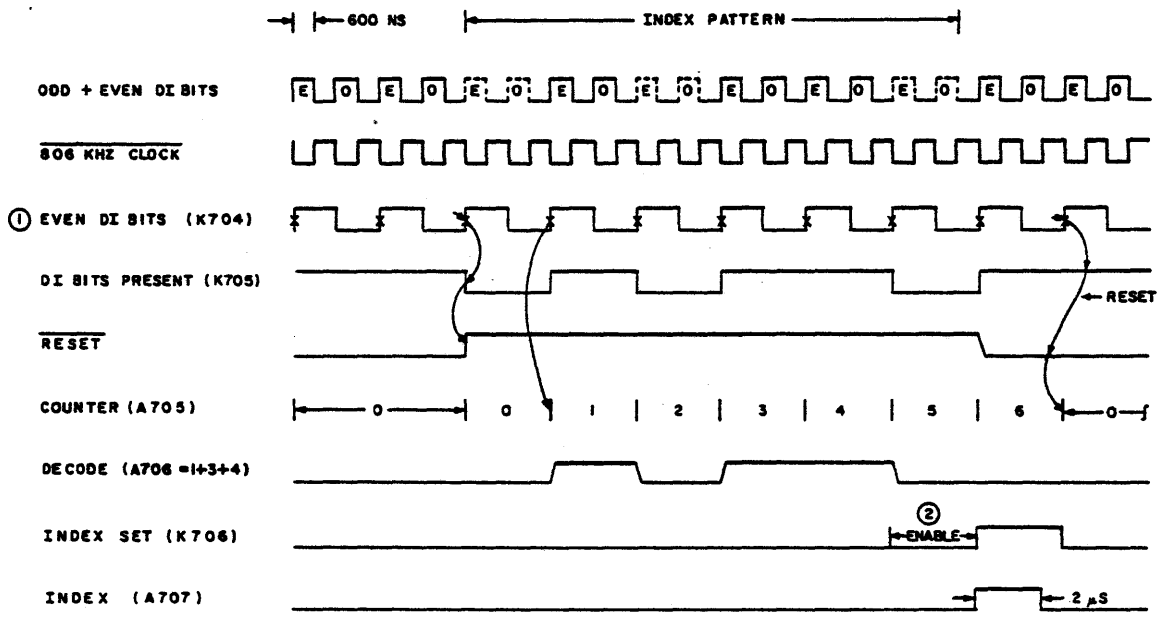
The controller and disk pack each handle different types of data. The controller transmits and receives only 8 bit parallel bytes of NRZ data. The disk pack requires serial MFM data. Therefore the drive must convert the data to the proper format before transferring it between the two.

During Write operations the drive receives parallel data from the controller, converts it to serial data (serialization) and writes it on the disk pack. During read operations it reads serial data from the disk pack, converts it to parallel (deserialization) and transmits it to the controller.

The read/write circuits (Figure 3-35) perform this conversion and the heart of these circuits is the serializer/deserializer (SERDES). It is used during both read and write operations to make the proper data conversions. The remainder of this section describes SERDES along with the other circuits involved in processing read/write data.

HEAD SELECTION

The head select circuit must select the desired head before a read or write operation



NOTES:

① X INDICATES LEADING EDGE OF SINGLE SHOT A708.

② NEXT LEADING EDGE REQUIRED TO SET FF BECAUSE OF PROPAGATION TIME THRU A705 / A706.

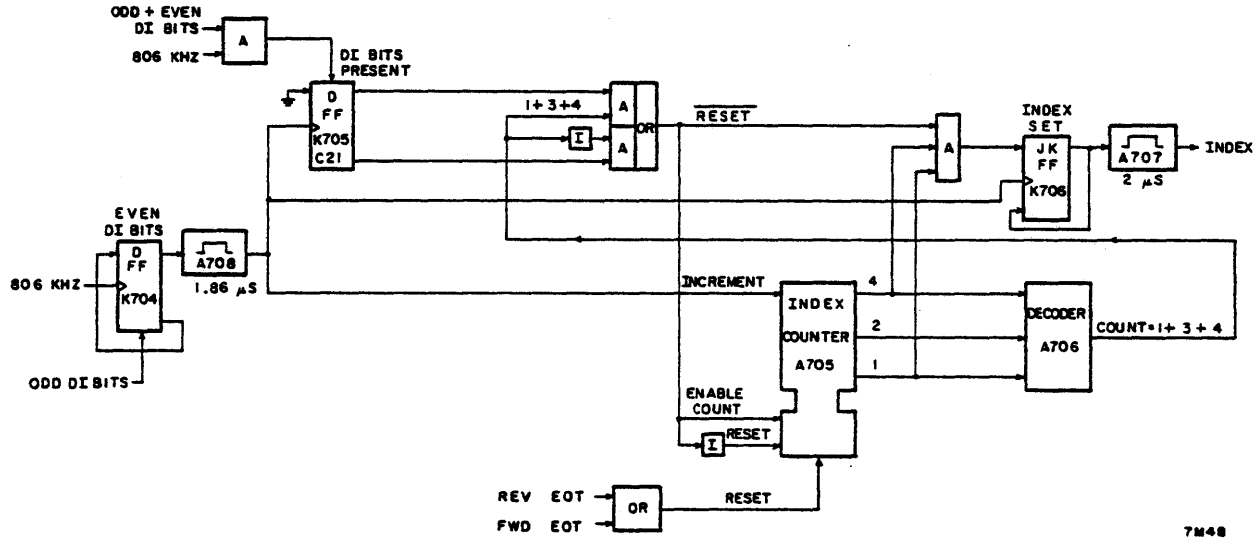


Figure 3-33. Index Detection Circuit

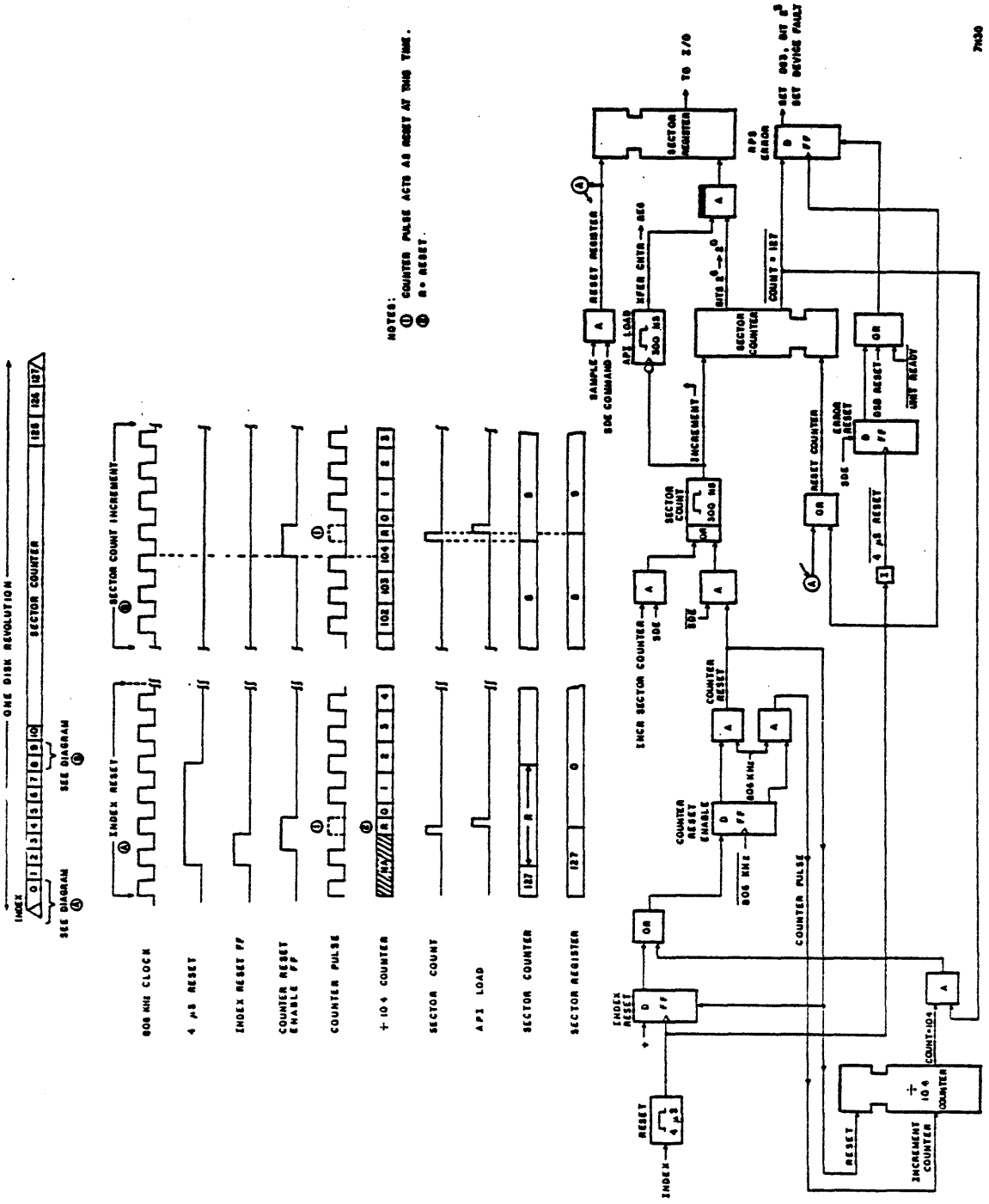


Figure 3-34. Sector Circuit

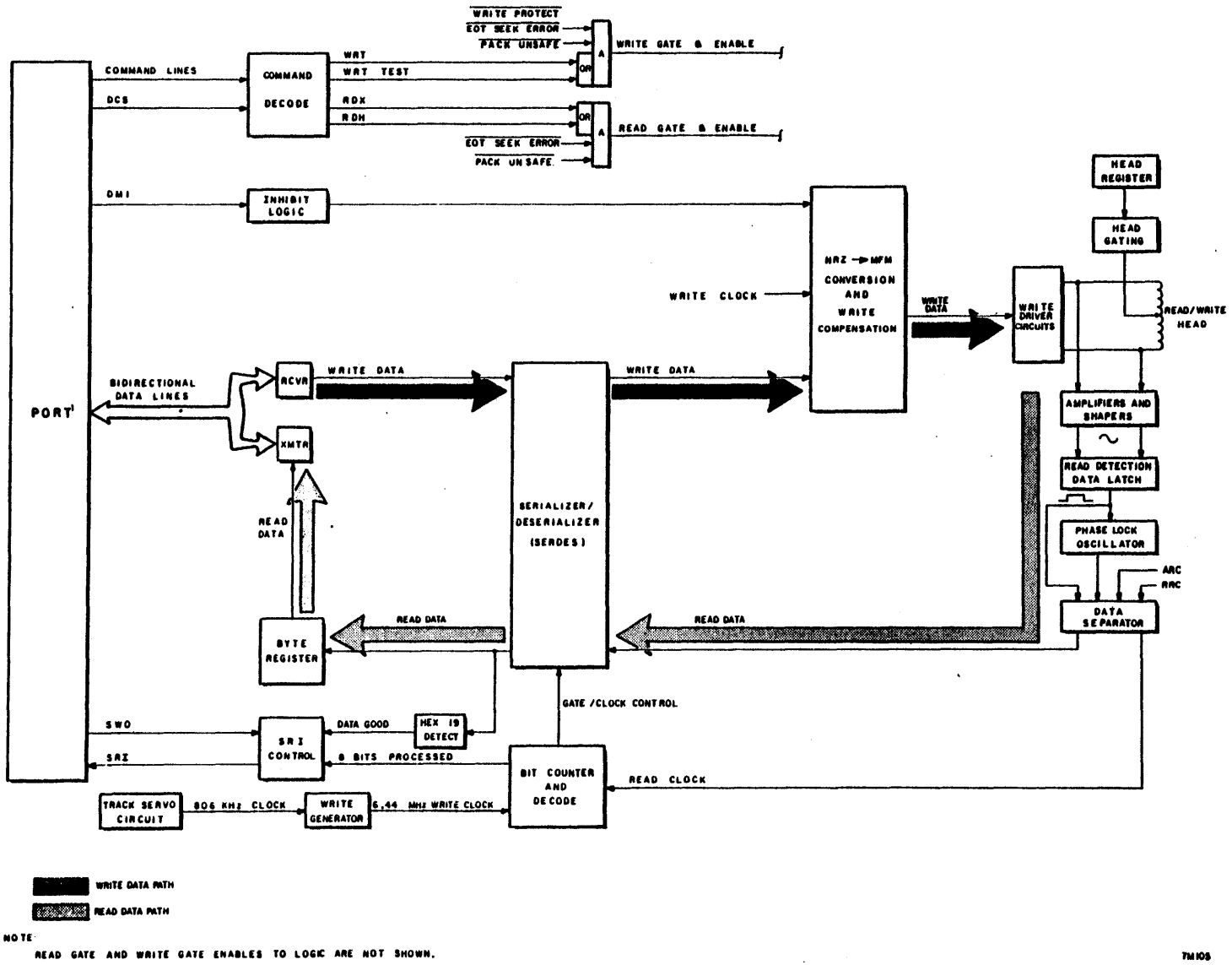


Figure 3-35. Read/Write Circuits Block Diagram

can be performed. See Figure 3-36 for the head 02 circuit.

The Head Address Register is set by a Head Address Out Lower (Tag 09) command from the controller. It is automatically reset to zero by any RTZS function. Bit 2^0 of the register is examined to determine if the head will have an odd or even number. Since (in this example) bit 2^0 is off, the even head decoder is enabled. The head is enabled by applying a ground to the read/write head center tap.

Note that all heads are automatically deselected while not On Cylinder or for 6 microseconds following a Head Address Out Lower command.

Two head select errors may occur at any time:

1. No Head Select is generated if the register is set to 19 or greater. Since these head numbers are nonexistent, there has been an equipment malfunction.

2. Multiple Head Select is sensed by the SCE/SCD circuit. If only one ground (or no ground) is sensed, the SCD voltage comparator output is +5 volts (no error). Two or more grounds puts more resistors in parallel, causing the voltage comparator to indicate a Multiple Head Select error.

As Figure 3-36 illustrates, any one of four head select or write errors can generate a current fault. With the Current Fault FF set:

1. Pack Unsafe FF sets.

   a. CHECK indicator lights.

   b. Read and Write Gates are disabled.

   c. Seek Forward Lower, Seek Reverse Lower or Recalibrate commands are not executed.

   d. This error status can be cleared only by pressing the CHECK switch or by a DIN from the controller.

2. Bits 2^4 through 2^7 of DS2 are enabled. Refer to Sense Operations.

The Current Fault FF cannot set to indicate an error while Data Modifier Line is up. Since there are no flux transitions while writing the address mark, AC Write Fault will occur. This is not an error condition at this time.

BASIC READ/WRITE PRINCIPLES

General

Read/Write data is transferred between the controller and drive in bytes. Each byte consists of eight bits. The parity bit is not written on the pack.

Information is recorded on, and read from, the disk by means of 19 read/write heads. Data is written by injecting a large current through a coil within the selected head. This generates a flux field that magnetizes the iron oxide particles bound to the disk pack surface. Each particle is then the equivalent of a miniature bar magnet with a North and South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes under the head. In turn, the direction of the flux field is a function of write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

Reading is an equivalent process. As the oxide particles pass beneath the head, the stored flux field intersects the coil within the head. This induces a current which, when amplified and analyzed, defines the written data.

In order to define the binary digits stored on the pack, the frequency of the flux reversale must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. The drive uses the Modified Frequency Modulation (MFM) recording technique. Refer to Principles of MFM Recording. The main advantage of MFM is that it permits higher recording densities without increasing the number of recorded flux reversals per inch.

The length of time required to define one bit of information is the cell. Each cell is nominally 155 nsec in width. Since there are eight bits per byte, each byte requires 1.24 usec to write or read. Although data is transferred in parallel (by byte), it is written or read serially (by bit).

Track Format

Each track has Index as its starting point. Information is then recorded in groups of related data in the form of records. In turn, records may be subdivided into fields. A gap of zeros separates each field within each record and, in addition, another gap

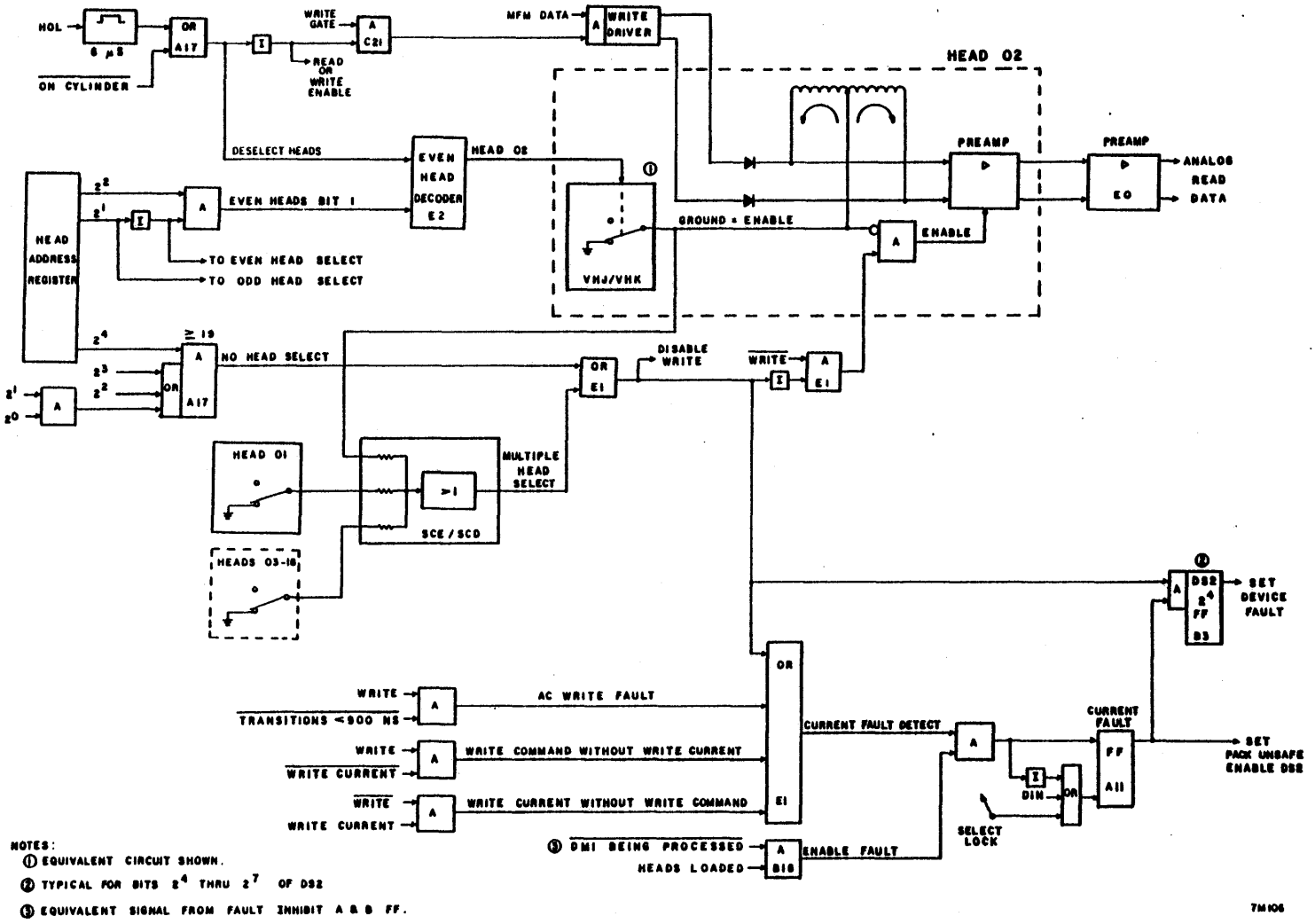


Figure 3-36. Head Selection Circuit

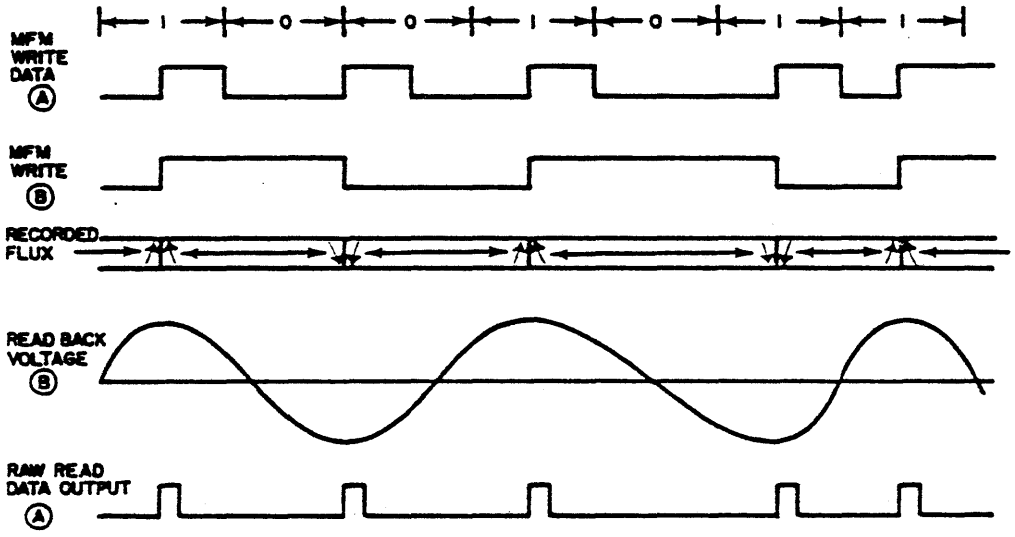
separates records. These gaps are used to permit the read circuit to synchronize itself so that it can reliably define logical ones and zeros. Gap length is variable in accorcance with the nature of the following field or record.

Track format, gap lengths, and record format are a function of the operating system. Refer to the applicable controller manual for further information. Because of the drive logic operations, however, the following rules apply.

- Each gap (field-to-field) or record-to-record) has variations in the number of zeros. The last two bytes of each gap contain hexadecimal 19. The first byte is called the Sync Byte; the second, the ID Byte. Read data cannot be returned to the controller until these bytes are found.
- For all records following Record Zero (or its equivalent), an address mark is written between the zeros gap and the hex 19 bytes. An address mark (AM) contains bytes without any flux transitions ("0" or "1") whatsoever. Although the address mark is typically three bytes of missing flux reversals, the actual AM length is determined by Data Modifier Line. As long as Data Modifier Line is up -- one byte or sixty bytes -- all writing is inhibited. Twelve bytes of zeros typically separated the AM bytes from the Sync Byte.

Principles of MFM Recording

This unit uses the MFM recording technique. This system defines a "1" by a positive transition occurring at the half-cell time (Figure 3-37). A "0" is defined by a positive transition occurring at the start of the cell time, except when preceded by a "1". In this case, no transition occurs during the cell time for a "0".



NOTES:

A. TIMING RELATIVE TO DRIVE AT I/O CONNECTOR.
B. SIGNAL AS IT WOULD APPEAR AT HEAD COIL.

7S168

Figure 3-37. Modified Frequency Modulation Recording

The rules for MFM recording may be summarized as follows:

1. There is a flux transition for each "1" bit at the time of the "1".

2. There is a flux transition between each pair of "0" bits.

3. There is no flux transition between the bits of a "10" or "01" combination.

Sorting data is accomplished by synchronizing an oscillator with the read data during the first continuous gap of zeros after read is enabled. The analog data can be decoded to binary "1's" and "0's" once the oscillator is synchronized.

A write function is similar to a read, except the incoming binary "1's" and "0's" are changed to the proper write current levels and then written on the disks.

The advantages and disadvantages of MFM recording are listed as follows:

1. Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries. This achieves higher recording densities of data without increasing the number of flux reversals per inch.

2. Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

3. Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

Erase before writing is not required when using MFM recording. The data being written is recorded over any data which may already be on the disk (this technique is referred to as a hard write).

Disk Surface Recording

Surface recording involves the magnetization of minute areas on the surface of a highly retentive magnet material. In order to reproduce the recorded information, the magnetic state of the material is read back by using the retained or residual flux to induce voltages in the Read circuits.

The relationship of a fixed recording head with a magnetic recording surface is shown in Figure 3-38. Also shown is one cycle of alternating current and the resulting current flow through the coil and the flux changes on the disk surface. The current flow through the coil reverses with a change from a positive to a negative direction, causing the polarity of the recorded flux to also reverse. Data is written by this flux reversal that is, it is the change in flux that will be read back as data. This reversal generates a readback pulse. Constant current (no flux reversals) does not generate a pulse; therefore, it does not represent meaningful data. This constant current state occurs while Data Modifier Line is up.

Figure 3-39 shows the phase difference between the induced magnetic force (flux) and the resulting current while reading data off the disk.

WRITE OPERATIONS

General

The controller sends the Write data to the drive via the bidirectional data lines. The data passes through the receivers and is input to SERDES. SERDES converts the parallel data into the necessary serial format. Next the data goes to the Write Compensation circuits which adjusts for problems caused by variations in read data frequency. The Write Driver circuits then process the data and send it to the head for writing on the disk. Figure 3-40 shows the Write circuits

Basic Write Sequence

The basic write operation sequencing is as follows:

1. Controller places command on the Command Code Lines and raises Device Command Strobe and Serial Write Out.

2. The drive decodes the command and verifies that it is safe to write (not Pack Unsafe and heads are On Cylinder). If it is safe, the write logic is enabled.

3. The drive raises Serial Read In. The controller drops Serial Write Out, but data must remain stable on the bidirectional data lines until the drive drops Serial Read In.

4. Data is loaded from the bidirectional data lines into SERDES.

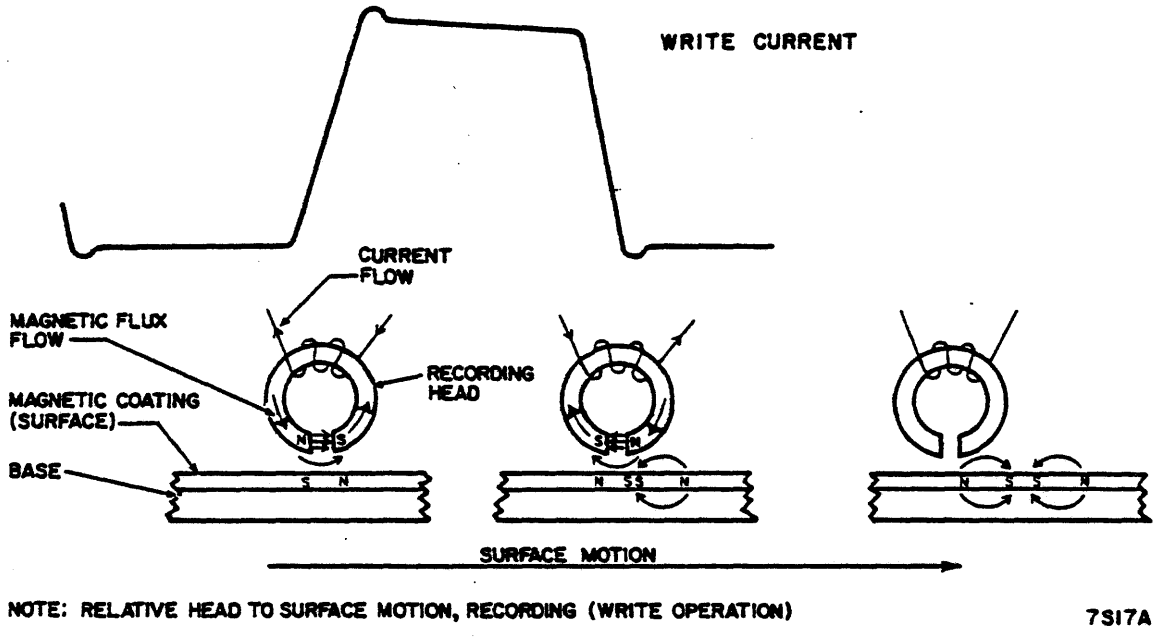


Figure 3-38. Magnetic Recording

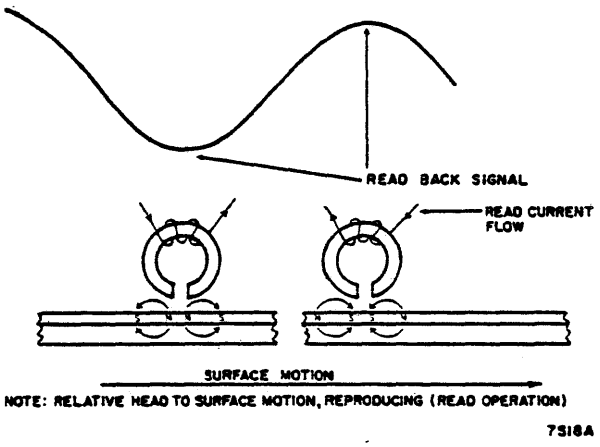
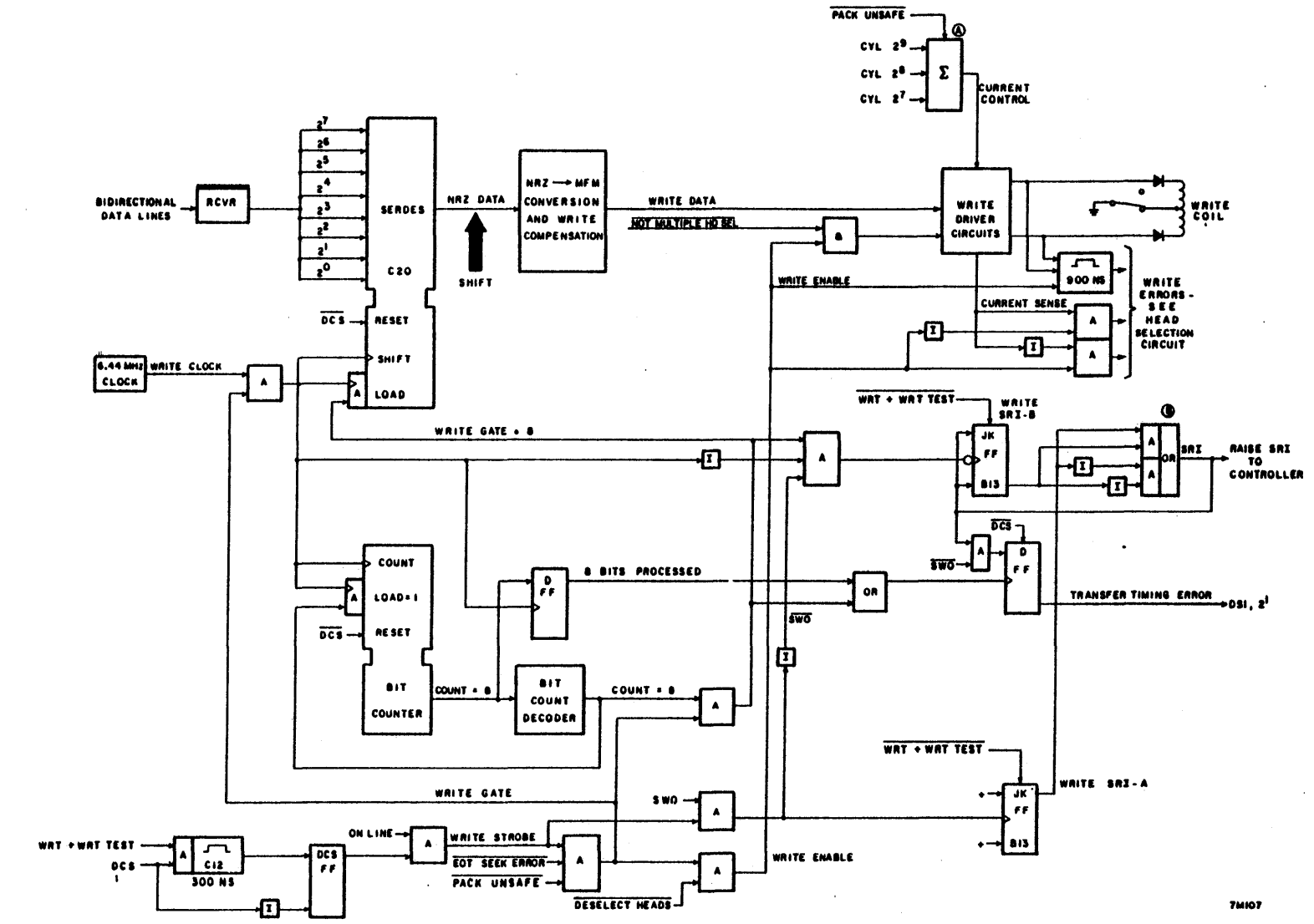


Figure 3-39. Read Current



NOTES

Ⓐ DECREASES WRITE CURRENT AS POSITIONER IS CLOSER TO SPINDLE.

Ⓑ EQUIVALENT CIRCUIT FOR EXCLUSIVE —OR GATE.

Figure 3-40. Write Circuit

5. The track servo circuit is generating the 806 kHz machine clock. This clock is generated by dibits read from the servo track; therefore, variations in spindle motor speeds do not affect recording density. This basic clock is used to form the 6.44 MHz write clock.

6. The write clock controls a counter which, in turn, controls the shift register function of SERDES. Data is shifted out of SERDES (deserialized) with each write clock so that the information on Bidirectional Data Line 2^7 is written first and 2^0 written last.

7. Data shifted from SERDES, which is NRZ (Non-Return to Zero), is converted to MFM. Actual phasing to compensate for peak shifting during subsequent read operations is controlled by a write compensation circuit.

8. If the controller has raised the Data Modifier Line, SERDES is ignored and all writing is inhibited.

9. The MFM pulses are sent to the write driver circuits which supply the necessary current to the write coil.

10. When a byte has been written, 8 Bits Processed comes up to load the next byte from the bidirectional data lines and to drop Serial Read In.

The Serial Write Out/Serial Read In sequencing continues for each byte written. Device Command Strobe and the command must remain up until the write operation is to be terminated.

Serdes Serializer

In order to understand the operation of this circuit, assume that the drive is in the process of writing byte "N". Serial Read In is up, Serial Write Out is down, and data for byte "N+1" is on the bidirectional data lines. See Figure 3-41. Sequencing is then as follows:

- Data is shifted from SERDES to the write compensation circuit with the leading edge of each write clock. Refer to Write Compensation for information on the NRZ/MFM conversion process.

- As data is shifted, the bit counter is also incrementing with write clock. It normally begins counting from a count of one; however, it starts from zero when Write is first enabled (writing the zeros gap).

- The bit counter contains a value of 8 as the last bit from byte "N" (originating from D17 of the bidirectional data lines) is being shifted out.

- If SRI had already dropped, or if Serial Write Out was still up, Transfer Timing Error (bit 2^1 of DS1) raises FLT to the controller.

- At the trailing edge of the next write clock:

  a. Data for byte "N+1" is loaded into SERDES from the bidirectional data lines.

  b. The Write SRI-B FF toggles to the cleared state. Two flip-flops, Write SRI-A and Write SRI-B, are connected to an exclusive-OR gate. They raise Serial Read In whenever they are in opposite states. As each byte is processed, toggling SRI-A raise Serial Read In while toggling SRI-B drops Serial Read In. In this case, with Write SRI-A and Write SRI-B both down, Serial Read In is dropped to the controller. This signifies to the controller that it may remove data from the bidirectional datalines.

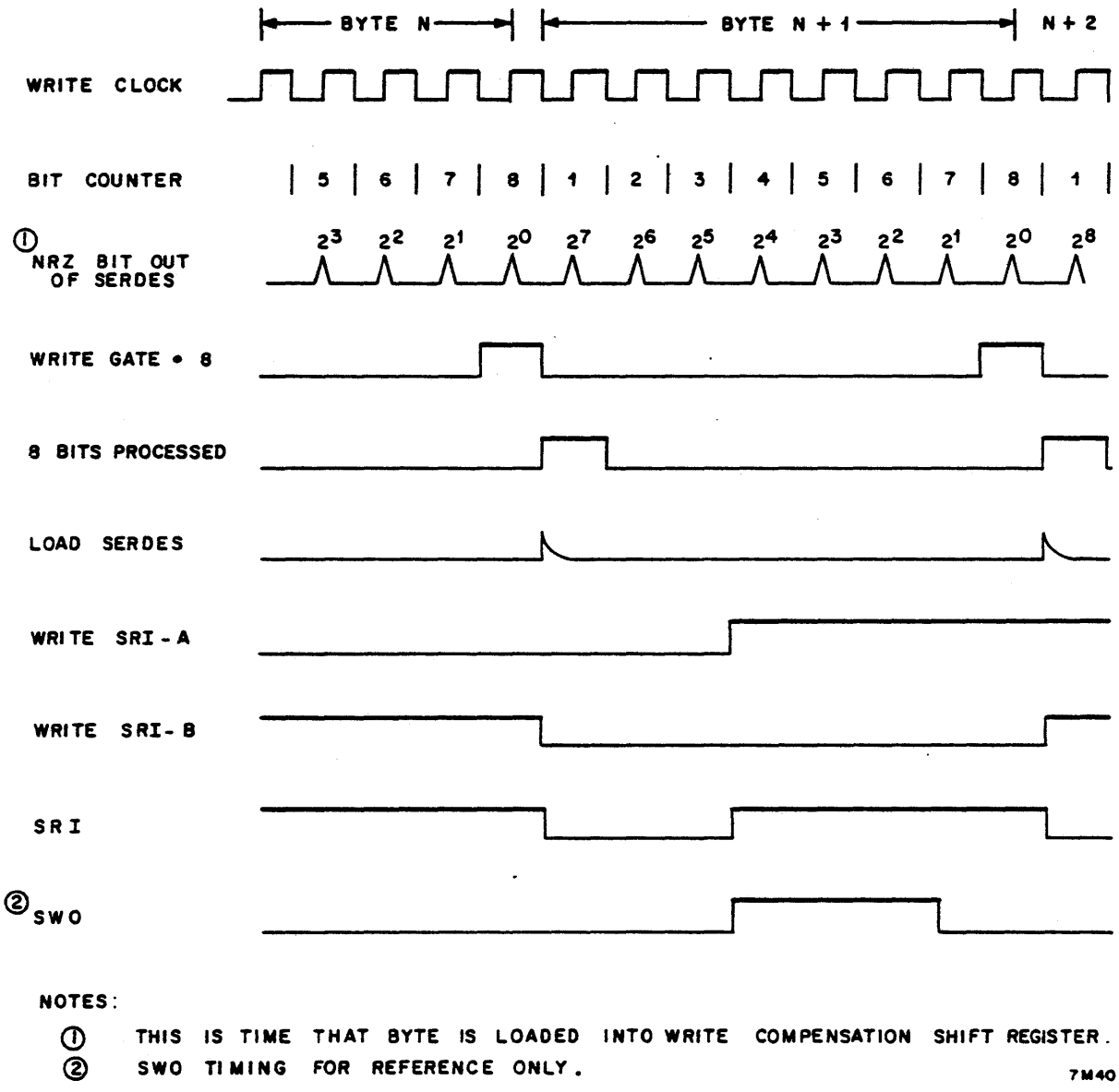
  c. The bit counter is reset to one.

- The data in SERDES is shifted out, one at a time, with each clock.

- While byte "N+1" is being written, the controller places data for byte "N+2" on the bidirectional data lines. It then raises Serial Write Out.

- With Serial Write Out up, Write SRI-A FF toggles to the set state. The requirements of the exclusive-OR gate are again met to raise Serial Read In. If Serial Write Out is late (8 Bits Processed generated before the controller gets around to raising Serial Write Out. Transfer Timing Error is generated.

- The controller drops Serial Write Out in response to the rise of Serial Read In. Parity of the data on the bidirectional data lines is checked at this time. If parity is not odd, Data Parity Error (bit 2^0 of DS1) is generated to raise FLT to the controller. This error does not directly stop the writing process. The drive logic will continue to write garbage until the controller drops Device Command Strobe. Parity bits, although checked by the I/O, are not written on the pack.



NOTES:

① THIS IS TIME THAT BYTE IS LOADED INTO WRITE COMPENSATION SHIFT REGISTER.

② SWO TIMING FOR REFERENCE ONLY.

7M40

Figure 3-41. Write Timing

- The writing process continues uninterrupted until the controller drops Device Command Strobe to terminate the operation. This drops Write Enable within the drive to prevent the write driver chain from writing flux transitions on the pack. SERDES and the bit counter are forcibly reset to zero.

Write Compensation

General

The write compensation circuit converts the NRZ data from SERDES into MFM data while compensating for a read condition known as peak shift.

Peak Shift

Peak shift is an effect that degrades read accuracy by distorting the waveform. This condition exists because no electromechanical device can be perfect.

In an ideal world, the flux reversal command by the write toggle would be instantaneous as shown in the Ideal Recording portion of Figure 3-42. Current would immediately switch from one polarity to the other. As a result, the distance required to complete the magnetic flux reversal on the disk would be so narrow as to be insignificant; the readback pulse would then also be extremely narrow. To carry the principle one step further, the heads would be an infinitesimal distance from the disk surface. Therefore, the head gap itself could be made very small for two reasons:

- The magnetic field strength increases as the head moves closer to the disk.
- The head gap must be wide enough to intersect sufficient lines of force from the magnetic flux field to generate a signal. The weaker the signal, the wider the gap must be. With the substantial flux amplitude gained by having the head very close to the disk surface, a very small head gap can generate a reliable readback voltage.

But in the real world, it takes time for the current to reverse; the flux change is not instantaneous. Furthermore, heads must fly a finite distance from the disk. The greater the distance between the head and the oxide, the wider the head gap must be. The resulting readback voltage is more or less sinusoidal with peaks less easily defined in time or amplitude.

With modern high frequency recording techniques, adjacent clock/data pulses are close enough to interact with each other. This is shown in Figure 3-43. Peak shift is the result of the interaction of the pulses. Because two pulses tend to have a portion of their individual signals superimpose themselves on each other, the actual readback voltage is the algebraic summation of the pulses.

When all "1's" or all "0's" are being recorded, the data frequency is constant: pulses are spaced apart by one cell (155 nanoseconds). As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative-going and positive-going errors cancel each other. This is the "zero peak shift" condition of the "...111..." pattern in Figure 3-43.

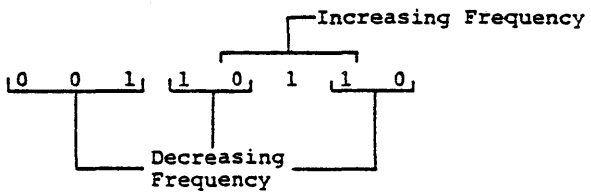
Peak shift occurs when there is a change in frequency. A "011" pattern represents a frequency increase since there is a delay of about 1.5 cell between the "01" and only 1.0 cell between the "11". As a result, the squeezing of the cells causes the mathematical average (the actual readback voltage) to shift the apparent peak to the left. This is early peak shift.

On the other hand, a "10" pattern represents a frequency decrease since a pulse is not written at all in the second cell. In addition, a "001" pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two bits.

The examples listed above examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



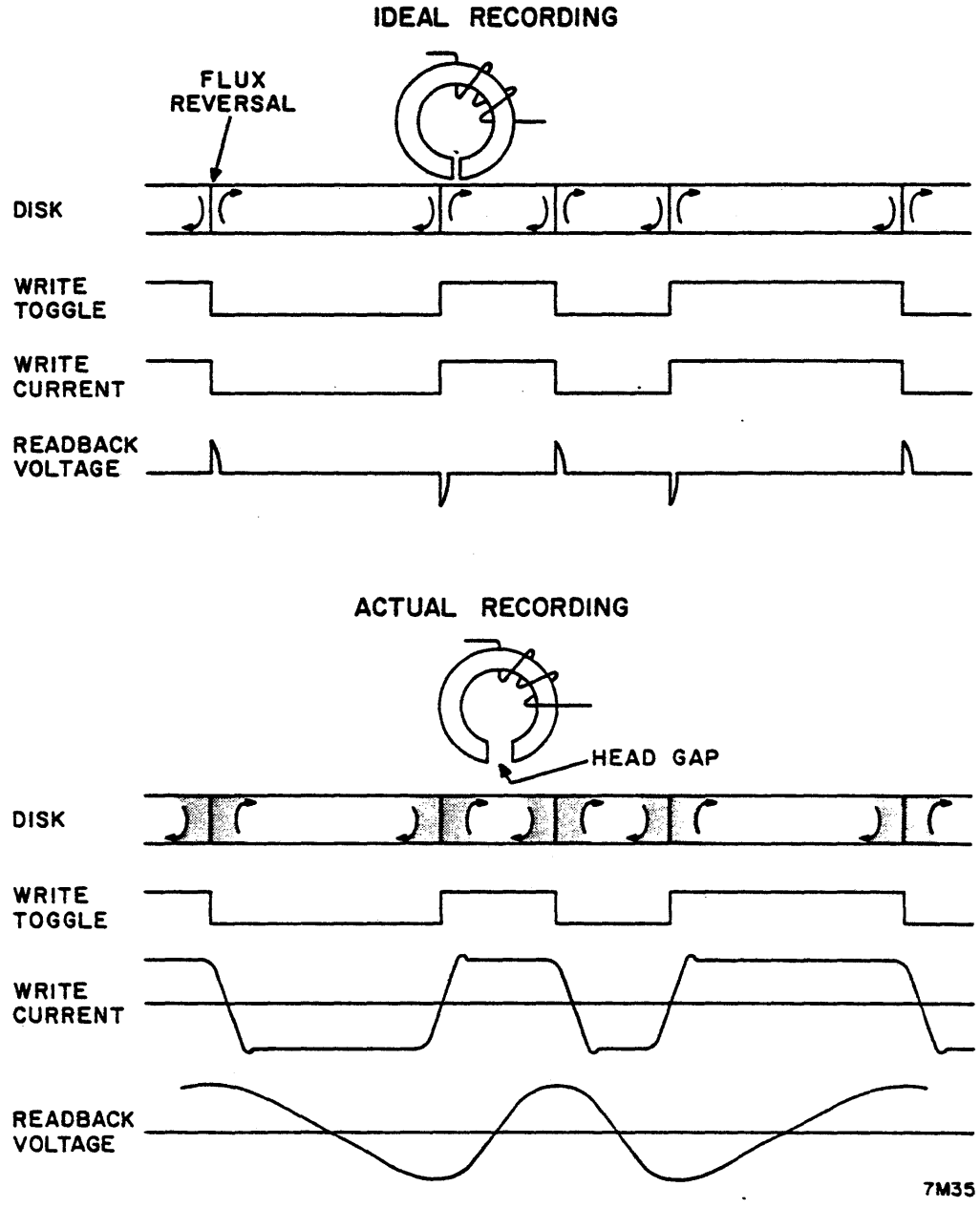


Figure 3-42. Write Irregularity

Any of these peak shift conditions can cause errors during subsequent read operations. The drive compensates for these known errors by intentionally writing a pulse earlier or later than nominal. This function is accomplished by the write compensation circuit.

Write Compensation Circuit

The write compensation circuit (Figure 3-44) converts NRZ data into MFM data while intentionally shifting the pulses in the data cell to compensate for peak shift.

Data from SERDES enters a decode shift register (K756 through K750) in NRZ format. It is shifted through the register by a two-phase clock signal consisting of Write Clock and its inversion, Not Write Clock. As the data shifts through the register, the register contents are examined by a series of gates to analyze the bit pattern. These gates determine if the incoming data frequency is constant (00000 or 11111), increasing (011 or 1000), or decreasing (10 or 001). The timing of the write data pulses applied to the write Driver Circuits (Figure 3-40) are adjusted to compensate for the frequency shift:

- If frequency is constant, there will be no peak shift. An MFM Clock pulse (pulse at beginning of a cell) is generated while Write Clock is down; MFM Datapulse (pulse at middle of a cell) is generated while Write Clock is up. The pulse, clock or data, is intentionally delayed by 10 nanoseconds and is applied to the On Time Gate. This pulse is the write data pulse applied to the write toggle.
- If frequency is decreasing, the apparent readback peak (Figure 3-43) would occur later than normal. To compensate for this, the data is written earlier than nominal. Early Gate is enabled. This causes clock/data to be written concurrently with Write Clock or Not Write Clock; the 10 nanosecond delay is bypassed.
- If frequency is increasing, apparent readback peak would occur earlier than normal. Therefore, data is intentionally written later than nominal. Late Gate is enabled. This causes the write data to be written 20 nanoseconds after the beginning of the cell.

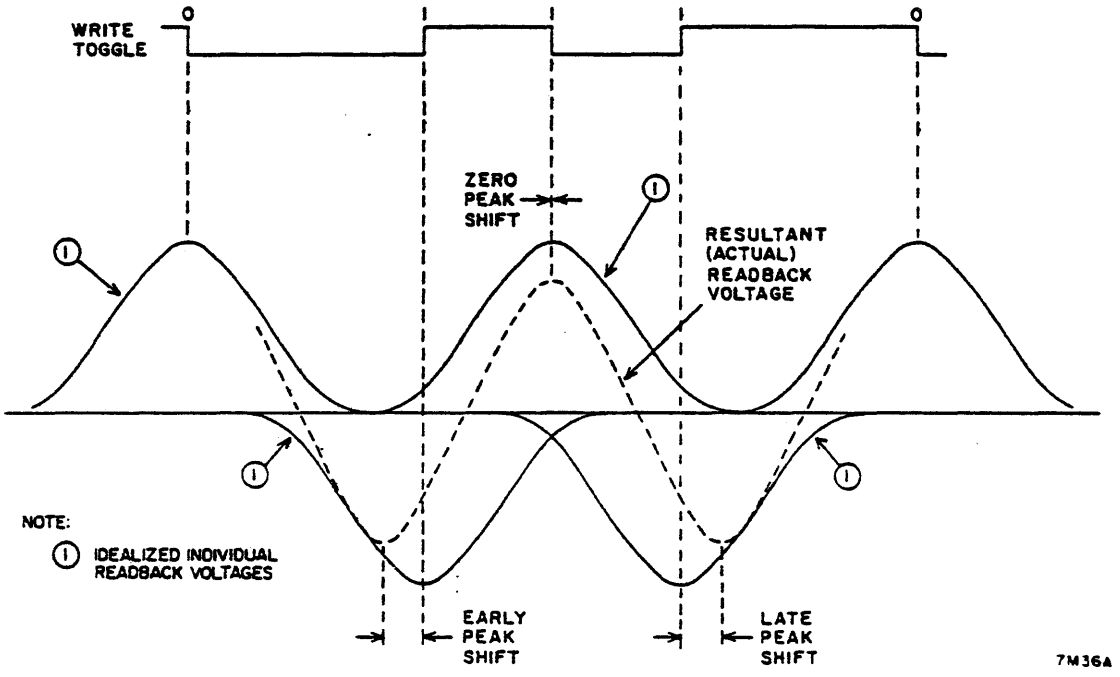


Figure 3-43. Peak Shift

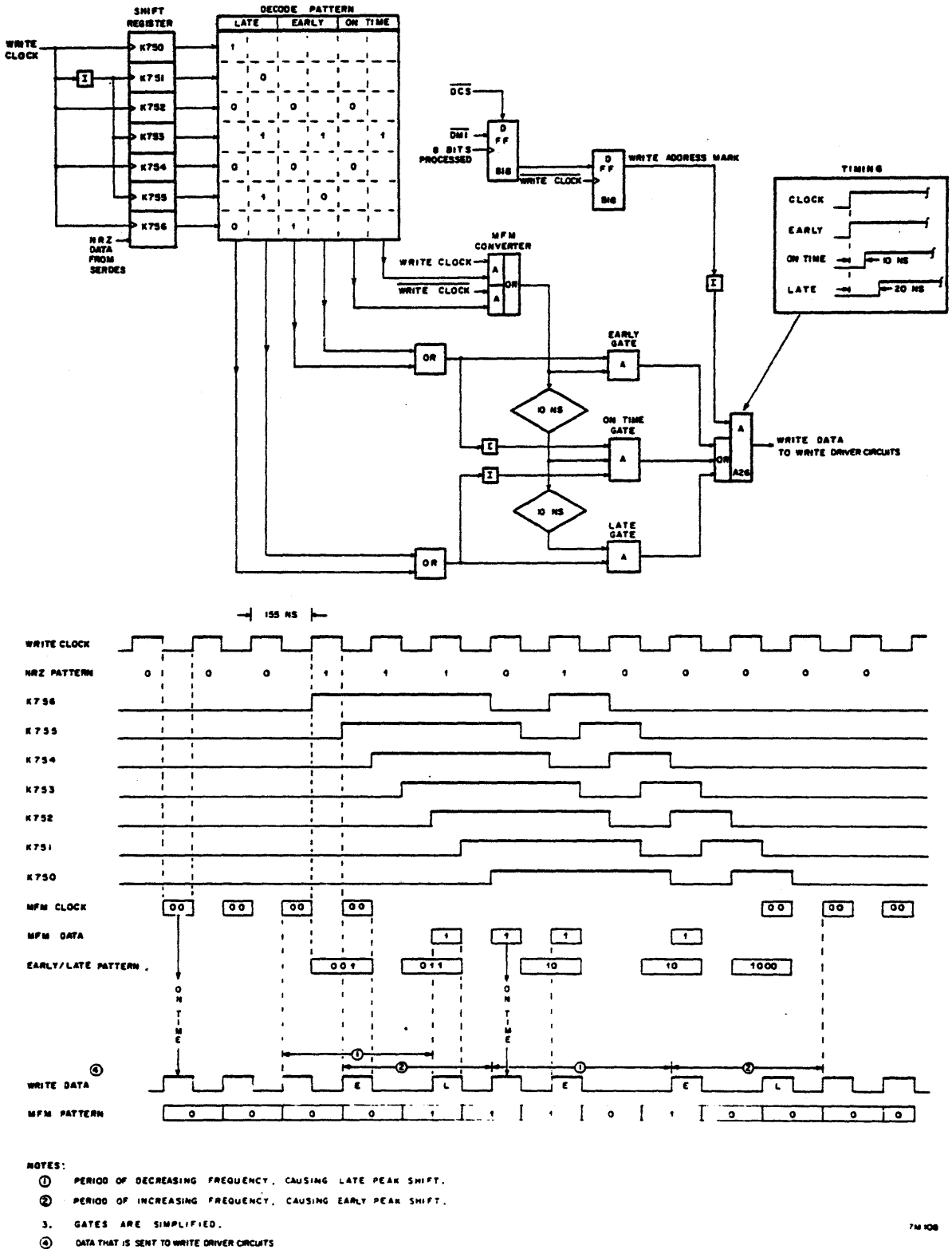


Figure 3-44. Write Compensation Circuit

As Figure 3-44 indicates, MFM Clock is written whenever there is a decode of 00 along with Not Write Clock. The clock is advanced or retarded if there is a simultaneous early or late decode (1000, etc.). The MFM Data signal is written whenever there is a decode of "1" along with Write Clock being true. Data may also be on time, advanced, or retarded.

Write Driver Circuits

The compensated Write data is sent to the Write Drive Circuits where it is applied to a differential receiver. The receiver is enabled by the Write Enable signal which is true only when the drive logic indicates a safe write condition. If this signal is true the data passes through the receiver to the Write Toggle FF.

The output of the Write Toggle FF is processed by a symetry restore circuit. This discrete circuit (QEL) restores symetry that may have been lost when the data was transmitted from the Write Compensation circuits (located in the logic chassis) to the driver circuits (located on the check). Refer to section 5 of this manual (Discrete Circuits) for a description of this circuit.

The magnitude of the Write current flowing in the heads is controlled as a function of cylinder address (this is referred to as Write Current Zoning). These zones are as follows:

- 0-127
- 128-255
- 256-511
- 512-1022

Write current amplitude is reduced at each zone boundary from outer to inner tracks.

Figure 3-45 shows the Write Driver circuits and its associated timing.

Writing Address Marks

The drive writes an address mark (AM) while Data Modifier Line is up. This prevents the output of the write compensation circuit (Figure 3-44) from being applied to the write driver chain (Figure 3-40). Current continues to flow through the write coil but, since there is no current reversal, no flux transitions occur. Therefore, the read circuit cannot recognize the constant flux as usable information.

The controller raises Data Modifier Line while the drive is writing the zeros gap. At the next 8 Bits Processed (a byte has just been written):

1. Not Address Mark Enable FF clears (Figure 3-44). All MFM clock/data pulses are unconditionally inhibited.

2. Fault Enable A FF sets, inhibiting Enable Fault (Figure 3-36). During normal write operations, a lack of write driver transitions will set Current Fault. This condition is occurring during Data Modifier Line but it is normal. The fault detection must, therefore, be disabled.

Data continues to be inhibited as long as Data Modifier Line remains up. The Serial Read In/Serial Write Out dialog continues, data is "accepted" into SERDES, but it is not gated to the write driver.

After the first AM byte is written, 8 Bits Processed sets Fault Inhibit B FF. Then, Fault Inhibit A FF clears at the next 8 Bits Processed; Not Address Mark Enable FF sets to again permit data to be written. Fault Inhibit B FF waits for one more byte; therefore, a Current Fault cannot be generated during the first byte (zeros) following the AM bytes. Current Fault is generated if Data Modifier Line is up for more than three bytes.

Write Fault Detection

Extensive monitoring circuits warn the controller of data transfer errors or hardware failures. Either condition will raise FLT to the controller. Hardware failures will set the Pack Unsafe FF: the CHECK indicator lights and writing is terminated.

Refer to Table 3-3 (Commands) for an explanation of these error conditions. Events that can be considered as related to write errors are:

Byte	Bit	Name
DS1	2^0	Data Parity Error
DS1	2^1	Transfer Timing Error
DS1	2^2	Protect Violation
DS1	2^4	State Violation
DS1	2^7	Command Parity Error
DS2	2^4	No or Multiple Head Selection
DS2	2^5	Loss of AC Write Current
DS2	2^6	Write Current Without Write Command
DS2	2^7	Write Command Without Write Current
DS5	2^0	Write and Read

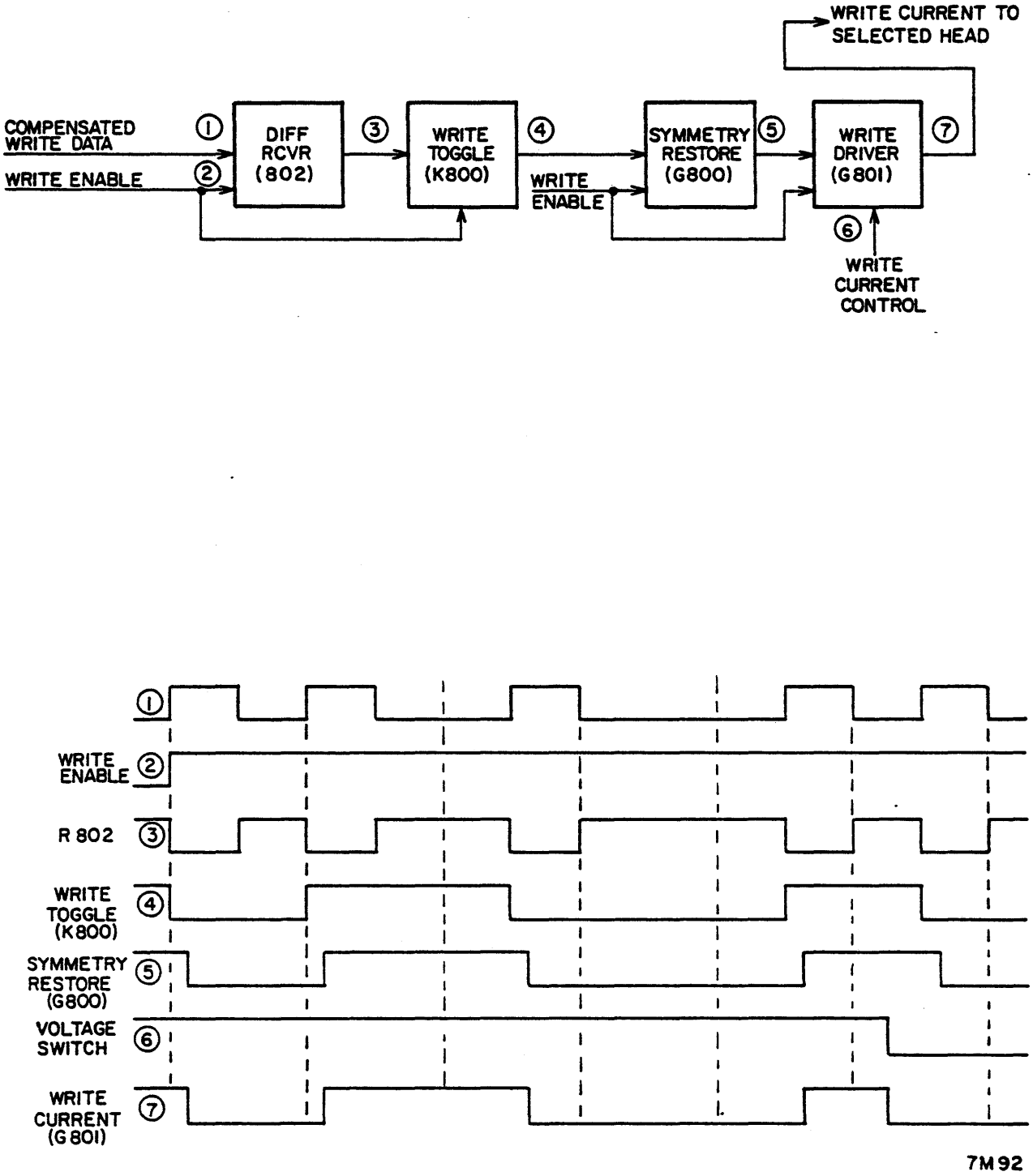


Figure 3-45. Write Driver Circuits Block Diagram & Timing

READ OPERATIONS

General

The read mode of operation is initiated when the drive receives a read command and the desired head is selected. The head then detects any flux transitions on the pack and converts them into an analog voltage. This analog signal (representing written data on the pack) is amplified and applied to the AGC amplifier. This output is applied to the Data Latch where it is converted to MFM data. It is then sent to the Phase Lock Oscillator which syncronizes itself to the data frequency and provides sync information to the Data Seperator. The Data seperator converts the data pulses from the Data latch into clock and data signals. The Serdes assembles the serial (bit) information into parallel (byte) information for transfer to the controller. A maximum of 30 ms is required from the application of read data for the read circuits (Figure 3-46) to stabilize to a steady state condition.

Basic Read Sequence

The basic read operation for a Read command is as follows:

1. Controller places command on the Command Code Lines and raises Device Command Strobe.

2. The drive decodes the command and verifies that it is safe to read (not Pack Unsafe and heads are On Cylinder). If it is safe, the read logic is enabled.

3. Analog data read by the head is amplified and shaped. The signal is then analyzed by the read detection data latch to find flux transitions. Each transition generates a data pulse. In this context, however, data pulse means only that there was a transition: whether it is a data ("1") or clock pulse is not yet defined.

4. A phase lock oscillator synchronizes itself with the data pulses frequency and phase. During the first 5 microseconds following the rise of Read Gate, a signal called Fast Start acts as a booster pulse to help the oscillator to quickly attain synchronization.

5. The data separator receives inputs from the phase lock oscillator and the data pulses. It separates the clock "data" pulses from the true data "data" pulses. The clock pulses are used as the internal read clock. The data pulses are applied to SERDES.

6. Data is loaded into SERDES and shifted through SERDES by the read clock. The bit counter is disabled and no data is transferred to the controller. When SERDES contains hex 19 (0001 1001) of the Sync Byte, Data Good is generated. This means that a valid field is approaching. The bit counter starts counting. Data Good cannot come up during Fast Start.

7. With Data Good up, the bit counter starts counting.

8. When the bit counter equals 8, SERDES contains the hex 19 of the ID Byte. This byte is loaded into the Byte Register and the drive raises Serial Read In. The Byte Register acts as a buffer to hold the assembled byte for the controller since the first bits of the next byte are already entering SERDES. The output of the Byte Register is applied to the multiplexer for transmission to the controller via the bidirectional data lines.

9. Serial Read In drops when the controller raises Serial Write Out.

The Serial Read In/Serial Write Out sequencing continues for each byte read. Device Command Strobe and the command must remain up until the read operation is terminated.

The Read Header functions identically to Read except that hex 19 cannot set Data Good prior to the sensing of an address mark. Most steps of the basic Read function apply; however, Fast Start does not rise with Read Gate (step 4). In addition, replace step 6 with the following:

1. Data is loaded into SERDES and shifted through SERDES by the read clock. The bit counter is disabled and no data is transferred to the controller.

2. When at least 2.5 microseconds of missing flux transitions have passed (this will occur only during the AM bytes of missing clock/data), and when the first pulse of the "0" bit is sensed (this is the first bit of the 12 bytes of zeros separating the AM bytes from the Sync Byte), a 5-usec Fast Start timeout is initiated. Data Good cannot come up during Fast Start.

3. After Fast Start times out, the read logic begins looking for hex 19 in SERDES. When the Sync Byte is detected, Data Good comes up.

4. The remaining Read steps apply without change.

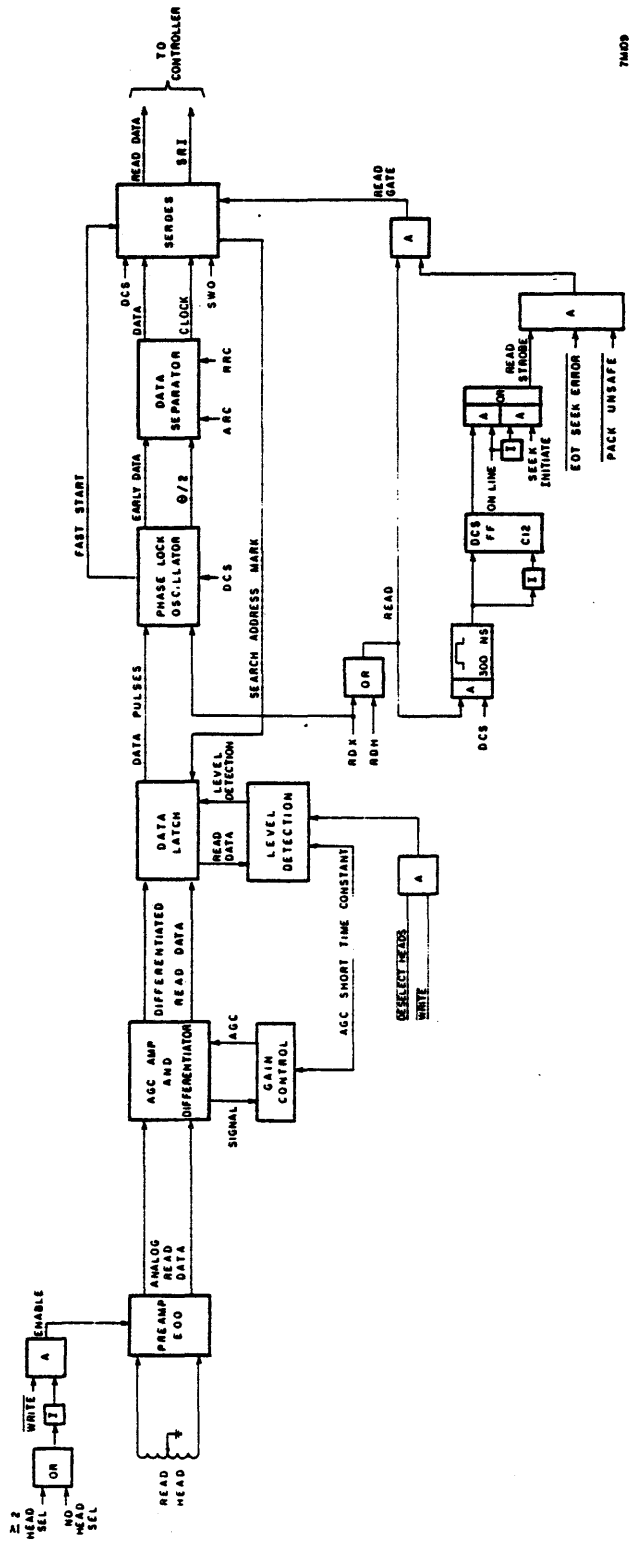


Figure 3-46. Read Circuit

General

The read circuits (Figure 3-46) process the read data and are described in the following discussion.

Preamplifier

A read preamplifier provides preliminary amplification of the voltage induced in the read coil. This voltage is induced in the read head by the magnetic field stored in the disk oxide. The frequency of the analog voltage is proportional to the magnetic field flux transitions generated while writing. The preamplifier is enabled whenever the positioner is On Cylinder (applicable head is selected) and the unit is not writing. Note that a Read or Read Header command is not needed at this point.

AGC Amplitude Stage

The analog read data is applied to a low pass filter in the AGC amplifier stage (Figure 3-47). This filter attenuates the high unwanted frequencies (noise) in the read data signal and provides a linear phase response over the read data frequencies.

The output of the filter is applied to the AGC amplifier (A851). The AGC amplifier provides a relatively constant output from a wide amplifier range on the input. This is accomplished by the AGC Control circuit which varies the gain of the AGC amplifier as the output varies.

The output of the AGC amplifier is amplified and differentiated and then applied to the Data Latch and Level Detection circuits.

Level Detector and Time Constant Control

The Level Detector and Time Constant Control circuit contains an Amplitude Enable pulse generator, a data detector to detect the address mark gap, and a circuit to control the time constants of the AGC amplifier and level detector.

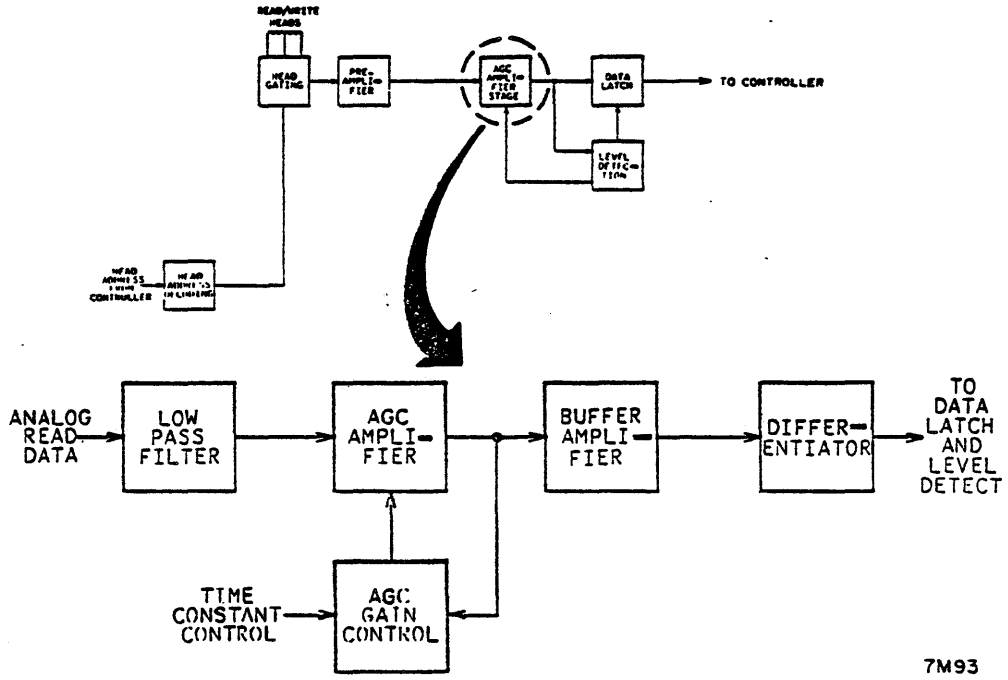


Figure 3-47. AGC Amplified Storage (Simplified Logic)

The output of the differentiator (Figure 3-48), is applied to a filter (A878) which attenuates the third harmonic of the low frequency Read signal. This effectively lowers the resolution of the signal.

The output of the filter is amplified and then rectified. A capacitor is charged to the average dc level of the rectified signal. This voltage is then applied to the reference input of a comparator (A886) and the rectified signal to the other input. When the rectified signal becomes more positive than the reference signal, the comparator switches. This produces a squarewave output that is used as an Amplitude Enable signal to reject noise and spurious pulses in the address gap area. The only time this output is used is during a Search Address Mark operation.

The Data Detector consists of a comparator (A883) and a retriggerable single shot delay (X884). The reference voltage on the comparator is a fixed dc voltage of about -0.46v. Each time the single voltage crosses the reference, the single shot is retriggered. The single shot will not time out as long as data above the fixed reference is being read. When a gap is reached, the single shot is retriggered by the last bit preceding the gap, times out for 670 nsec, then changes state to indicate an absence of data (Figure 3-48). The single shot is retriggered by the first data bit following the gap and by each succeeding bit, indicating that data is again present.

The Time Constant Control circuit switches the time constants of the AGC Amplifier and Level Detection circuits. Switching from a short time constant to a long time constant avoids responding to the loss of amplitude in the address mark gap area. Figure 3-49 shows block and timing diagrams of the Time Constant Control circuit with the address mark gap in three different positions.

The Level Detector circuit is normally in a short time constant of 5 µsec in order to rapidly respond to changes in signal amplitude to maintain adequate margin in the amplitude enable function. The 5 µsec time is long enough so that the level detector does not respond to drop outs caused by disk surface bad spots. During the address mark gap, the level detector is switched to a time constant of 100 µsec. This prevents a shift in the comparator reference level so noise in the gap area does not produce false enable pulses.

The AGC amplifier is allowed 25 µsec to stabilize from the Head Select and Read Gate transients. A head may be selected and Read Gate can come up any time during a revolution of the disk, so it is possible that the address mark gap could occur during the 25 µsec stabilizing period. The AGC time constant is held in the short condition for the first 10 µsec following Read Gate. If a gap occurs between 10 and 25 µsec, the AGC amplifier is switched to a long time constant of 200 µsec to maintain a relatively constant gain level through the gap area.

Data Latch Circuit

The Data Latch circuit (Figure 3-50) consists of a low pass filter for the low resolution channel and zero-cross detectors and pulse generators for both the high and low resolution channels.

The Read Data from the differentiator is applied directly to the zero-cross detector in the high resolution channel and through the low pass filter to the zero-cross detector in the low resolution channel. As mentioned before, the filter lowers the resolution of the Read signal by attenuating the third harmonic of the signal.

The pulse generators (N882 and N877) produce pulses for each zero-crossing of the data. By appropriate delays, the low channel pulse (IN882) enables the K input to the output FF (K873) in time for the high channel pulse (N877) to clear it. A 50 nsec output pulse is formed when the delayed feedback resets the FF. The leading edge of the output pulse retains the timing of the high resolution channel. Note that the propagation time of the various gates must be considered to enable the K input at the proper time. Whenever the frequency of the read back data is decreasing, there is a camels hump in the differentiated output. (See Figure 3-48). With sufficient frequency change and high resolution heads, the differentiated signal may actually pass through zero. The high resolution channel can react to these extraneous zero-crossing pulses; the low cannot because of the low pass filter. Therefore, they are ignored by the output FF because it cannot be cleared unless the low channel K enable is present.

The rejection of spurious pulses in the address mark gap is accomplished by ANDing the high channel pulses with an enable pulse. During the search mode, the Amplitude Enable pulses are passed through and ANDed with the high channel zero crossover pulses. When a zero crossover pulse corresponds to an enable pulse, it is passed through to reset the Output FF. There are noise created zero-crossover pulses in the address mark gap area. However, there are no enable pulses, so the reset input to the Output FF is disabled. Noise pulses in the low resolution channel are present at the set input of the FF, but are ignored because the FF is not reset during the gap period.

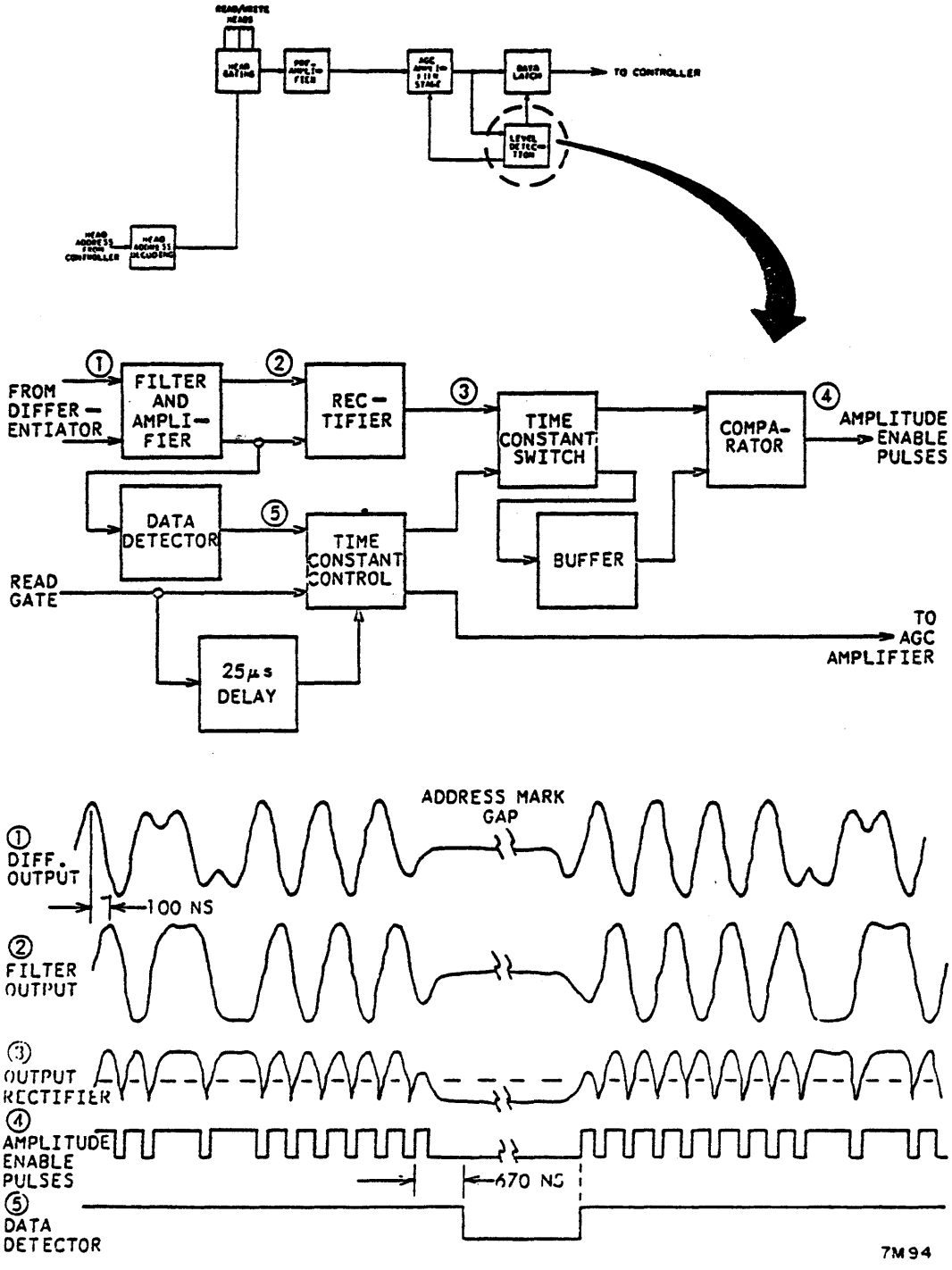


Figure 3-48. Level Detection Circuit

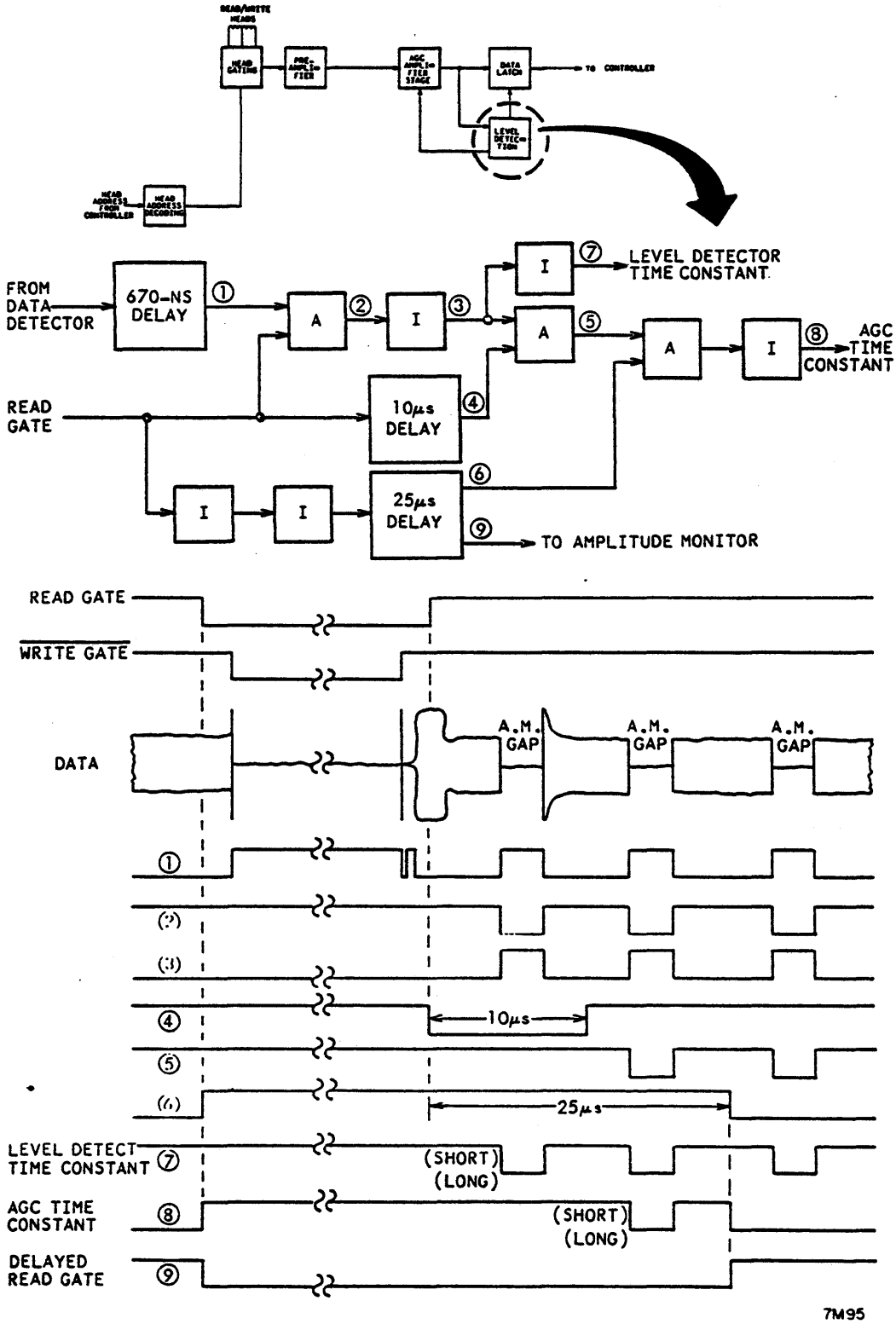


Figure 3-49. Time Constant Control Circuit

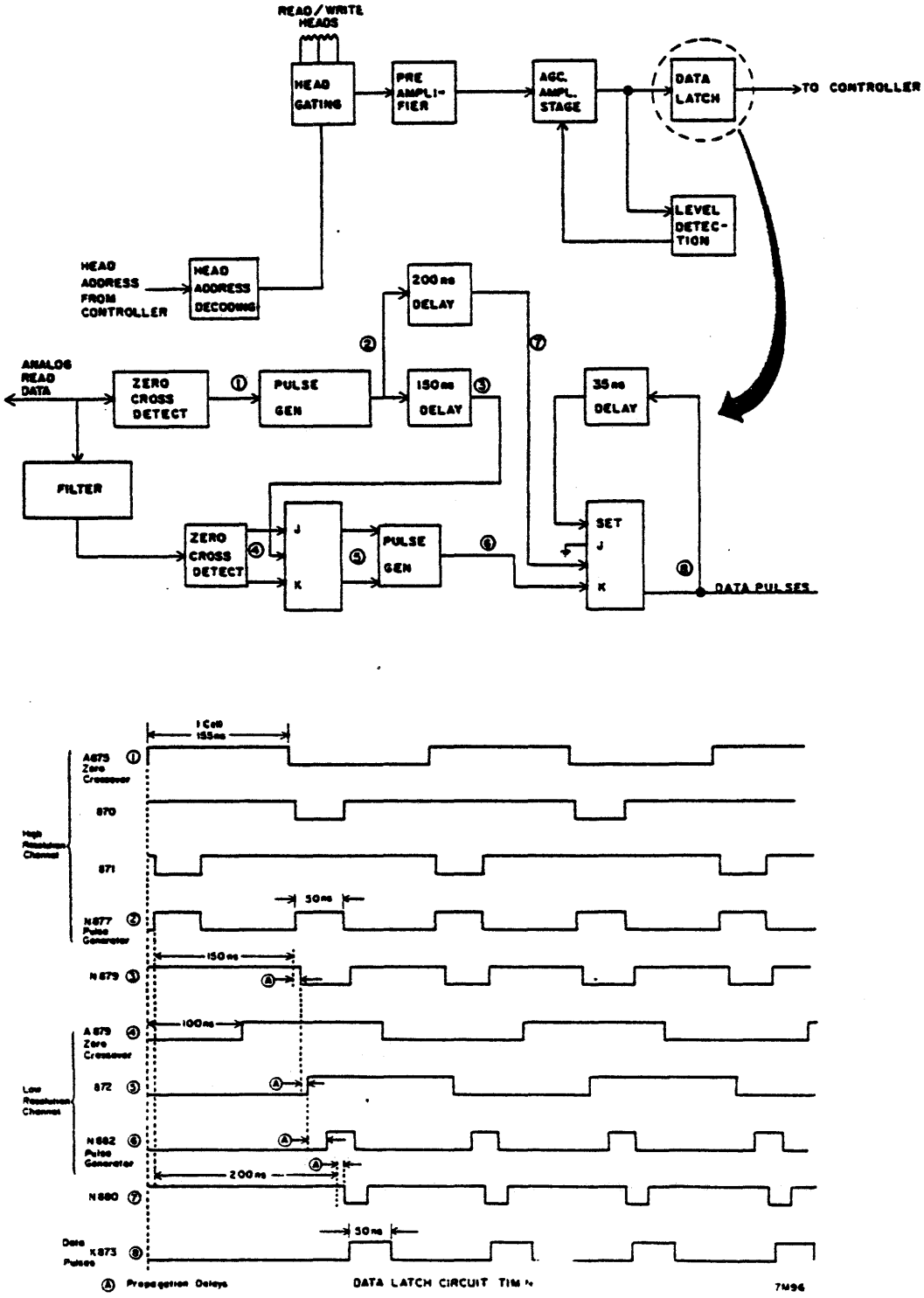


Figure 3-50. Data Latch Circuit

The Search Address Mark signal drops at the end of the gap. This applies a constant enable to the high resolution channel and all zero-cross pulses get through to the FF. This terminates the Amplitude Enable function and removes the Level Detector as a possible source of error during the actual reading of data.

Phase Lock Oscillator Circuit

The phase lock oscillator (PLO) circuit (Figure 3-51) provides a clock signal to the data separator so that it may determine if the data pulses from the data latch are MFM Clock or MFM Data. To do this, the PLO must synchronize its frequency to the frequency of the data coming from the disk.

PLO frequency is controlled by the Comparator FF. Basically, the FF is set by data and cleared by the oscillator pulses. Therefore, if the oscillator is too slow, the FF will be set more than it is cleared because data frequency exceeds oscillator frequency. Frequency synchronization is attained when data and oscillator frequencies are identical. The FF is then set 50% of the time. The nominal data frequency is 6.44 MHz with the oscillator running at twice the data frequency (12.88 MHz).

The FF is set by one of three signals:

1. DS, which is Early Data.
2. X, which is delayed DS.
3. Y Enable, which is used when data will not be available in time to set the Comparator FF.

The oscillator output is divided into four 1/4-cell phases: P1, P2, P3, and P4. The X or DS pulses can set the FF only if they occur in the P1, P2, or P3 periods. Except in cases of abnormal peak shift, the Comparator FF is set during P1 or P2. The FF is unconditionally cleared at P4 time.

In a pattern of all "1's", DS sets the FF. An all "0's" pattern causes it to be set by X pulses. Synchronization shifts between DS and X pulses depending upon the data pattern being read. During a data pattern in which DS or X will not occur during P1 or P2 time (for example, in a "10" pattern) Y Enable acts as a fake data pulse to set the FF to maintain reasonable frequency control.

The Comparator FF output is integrated and used as a control voltage to the voltage-controlled oscillator in the PLO. With the FF set, the oscillator tends to speed up; with the FF cleared, it slows down. The multivibrator output is, therefore, not completely symmetrical. A divide-by-two flip-flop (θ/2) provides the required symmetrical output by triggering off of the negative-going edge of the PLO output.

Note that the PLO functions as long as the data latch is operational. Only the Read Enable signal need be up.

Fast Start

Fast start increases loop gain to assist in rapid frequency synchronization. This function is enabled by a Read command. Note that Read Header does not directly provide Fast Start. With delay Y806 timing out for 5 microseconds, the following events occur:

1. Greater current is provided to a circuit internal to the control voltage generator. The control voltage to the multivibrator, which is normally 0.65v peak-to-peak, is doubled.
2. DS and Y Enable pulses are inhibited. Only X pulses are presented to the Comparator FF. This ensures correct phase synchronization. Fast Start must be enabled only during a sync pattern of zeros.
3. P4 pulses are narrowed to about 1/8-cell time to permit incoming data to dominate the Comparator FF.
4. Fast Start is applied to SERDES control to control Data Good.

Delay Y808 is used for address mark operations. With Read Enable up, this single-shot remains in the continuously-triggered condition. A Read command cannot generate a Resync Pulse to initiate Fast Start. As explained in the SERDES discussion, data cannot be recognized until the trailing edge of Fast Start. However, no flux transitions occur during the address mark gap; therefore, there are no X or DS pulses. Y808 times out if about two bytes (each byte equals about 1.24 microseconds) occur without X or DS pulses. The first "0" of the first zeros byte retriggers Y808; Y806 fires to initiate Fast Start.

Data Separator Circuit

The Data Separator circuit (Figure 3-52) separates the data "1's" from the clock. The circuit consists of the Data Window FF, Data Sense FF, Data and Clock register FFs, the Data Strobe circuit, and various delays and gates.

The data window, Shift pulses, and Reset pulses are derived from the θ/2 output of the Phase Lock Oscillator circuit. The data window width is adjustable for maximum data discrimination by means of a tapped delay

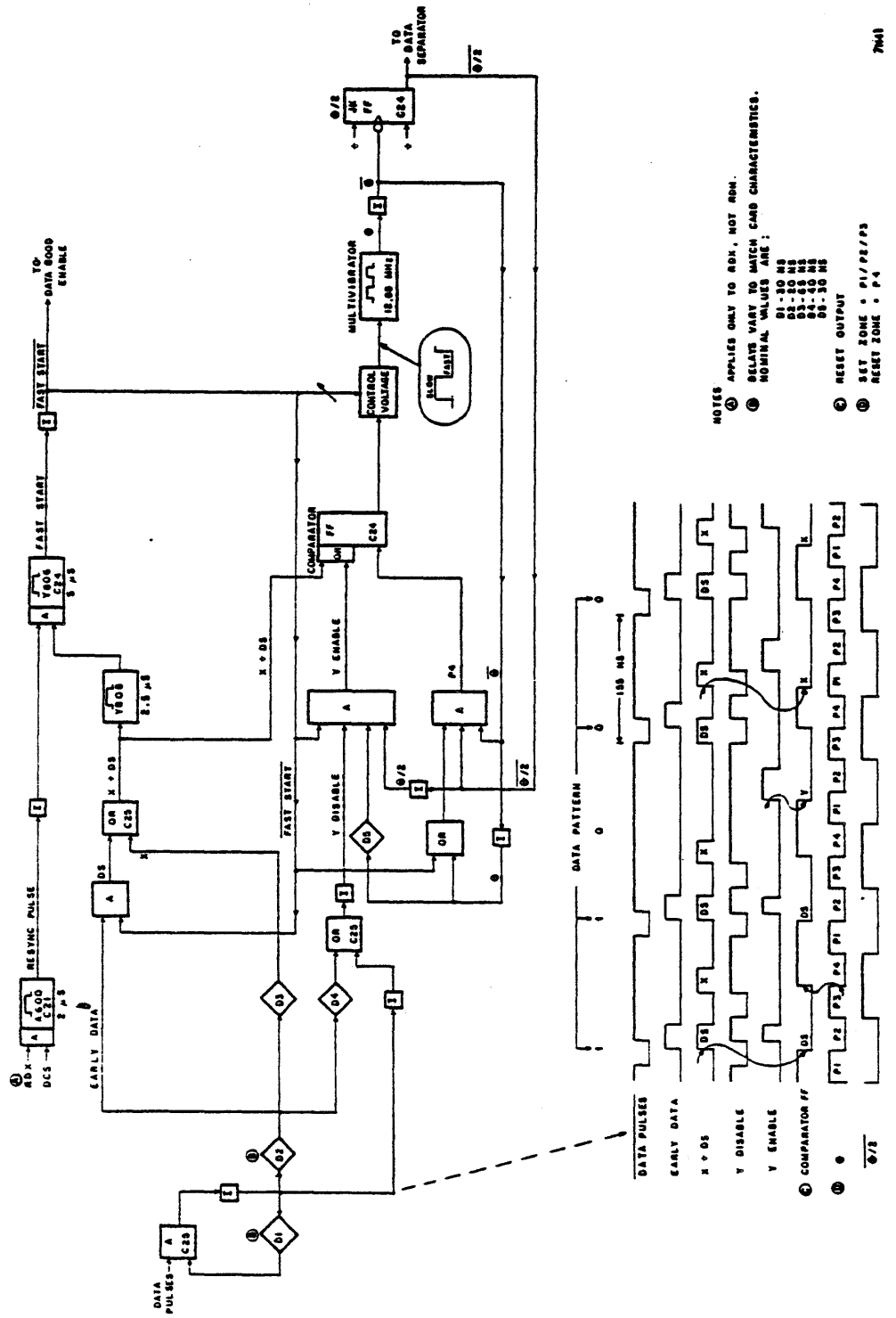


Figure 3-51. Phase Lock Oscillator Circuit

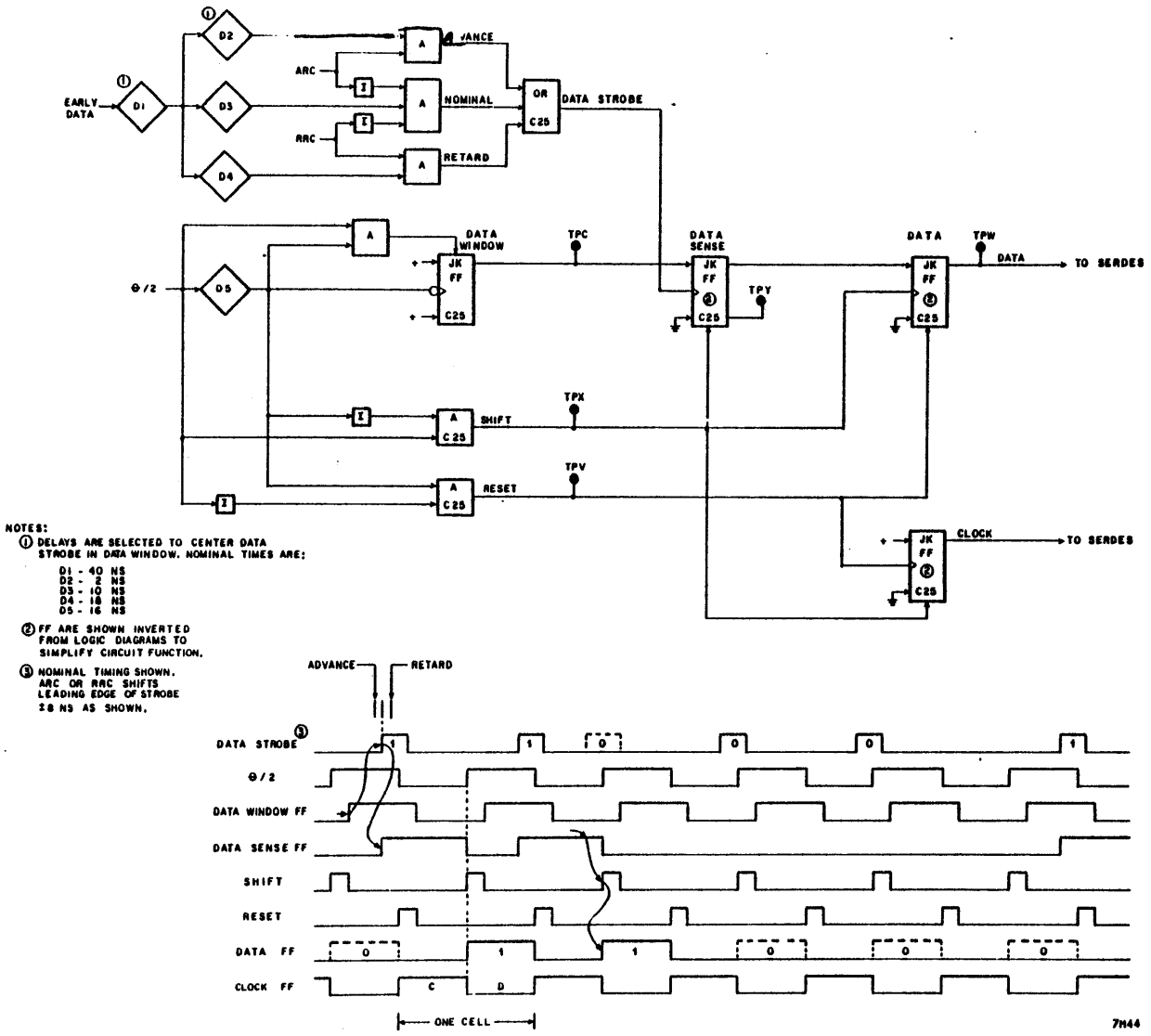


Figure 3-52. Data Separator Circuit

line. The Data Strobe pulses are used to toggle the Data Sense FF. The nominal strobe is a delayed data pulse. The strobe's relative position with respect to the data window is adjusted for maximum data recovery. A "1" is recognized if strobe occurs while the Data Window FF is set. Early or late strobes may be varied from the nominal strobe time by a command from the controller (Advance or Retard Read Check) or the setting of a switch on the logic chassis maintenance panel. This feature allows recovery of data which may be out of position on the disk relative to the average data position.

The shift pulses are narrow pulses which occur once each cell time. These pulses initialize the Data Sense FF and shift the contents of the Data Sense FF into the Data Register FF. The Shift pulses also initialize the Clock register FF.

The Reset pulses also occur once per cell period. They initialize the Data Register FF and toggle the Clock Register FF. As shown in Figure 3-52), the Shift and Reset pulses control the timing of the output waveforms of the data separator circuit. Note that the window is delayed beyond the Shift pulse so that the Data Sense FF is always ready to accept a Data Strobe pulse.

The Data Sense FF is toggled whenever a Data Strobe occurs during the data window time (Data Window FF set) of a cell period. The next Shift pulse would then transfer the data "1" from the Data Sense FF to the Data register FF. Note in Figure 3-52 that the data "1" is actually transmitted to SERDES almost one cell time after it is detected.

SERDES Deserializer

SERDES (figure 3-53) is used during Read operations to convert serial information read from the disk into parallel (byte) information for transmission to the controller.

Serdes During Read (RDX)

In order to understand the operation of this circuit, assume that Read Enable is up (On Cylinder and Not Write) and that the drive/controller interface is not yet communicating. The earlier stages of the read circuit are operational: data pulses are available from the data latch circuit and the PLO is providing read clock. SERDES itself is inhibited because Read Gate is down. The bit counter contains a count of zero.

The heads are sensing the bytes of zeros in the inter-record gap and the controller raises Read and Device Command Strobe Sequencing is then as follows:

1. Read Gate is generated.
2. The rise of Device Command Strobe drops the bit counter reset. The bit counter counts to one. Then, because of Count Inhibit, it is frozen.
3. Data from the data separator circuit triggers single shot A625. Data is loaded into SERDES at the trailing edge of each read clock from the data separator circuit.

NOTE

The remaining steps cannot occur for at least 5 microseconds following the rise of Read. This is the Fast Start timeout to allow full frequency/phase synchronization.

4. After 5 microseconds, Fast Start drops and the Data Good Enable FF sets. Note that Search Address Mark is NOT enabled.
5. The zeros pattern continues to be loaded into SERDES.
6. Eventually, the sync byte of hexadecimal 19 (0001 1001) begins to enter SERDES. See Figure 3-54 for timing.
7. When the sync byte is fully loaded, the Hex 19 Detect FF sets.
8. The Data Good FF sets. Count Inhibit drops.
9. The bit counter starts counting from one as the sync byte is shifted out of SERDES. This byte cannot enter the byte register. The ID byte (also hex 19) begins to enter SERDES.
10. When the counter reaches a count of eight, and at the trailing edge of read clock:
    a. The ID byte is transferred from SERDES to the byte register.
    b. The first bit of the first data byte is loaded into SERDES. (This does not affect the byte transferred to the byte register because SERDES contains edge-triggered devices. The ID byte is transferred out before the next incoming data bit can be reflected in the SERDES 2^0 output.)
    c. The bit counter is reset to one.
    d. The output of the byte register is applied to the bidirectional data lines via the multiplexer as long as Read Gate is up. The data on these lines has no validity with Serial

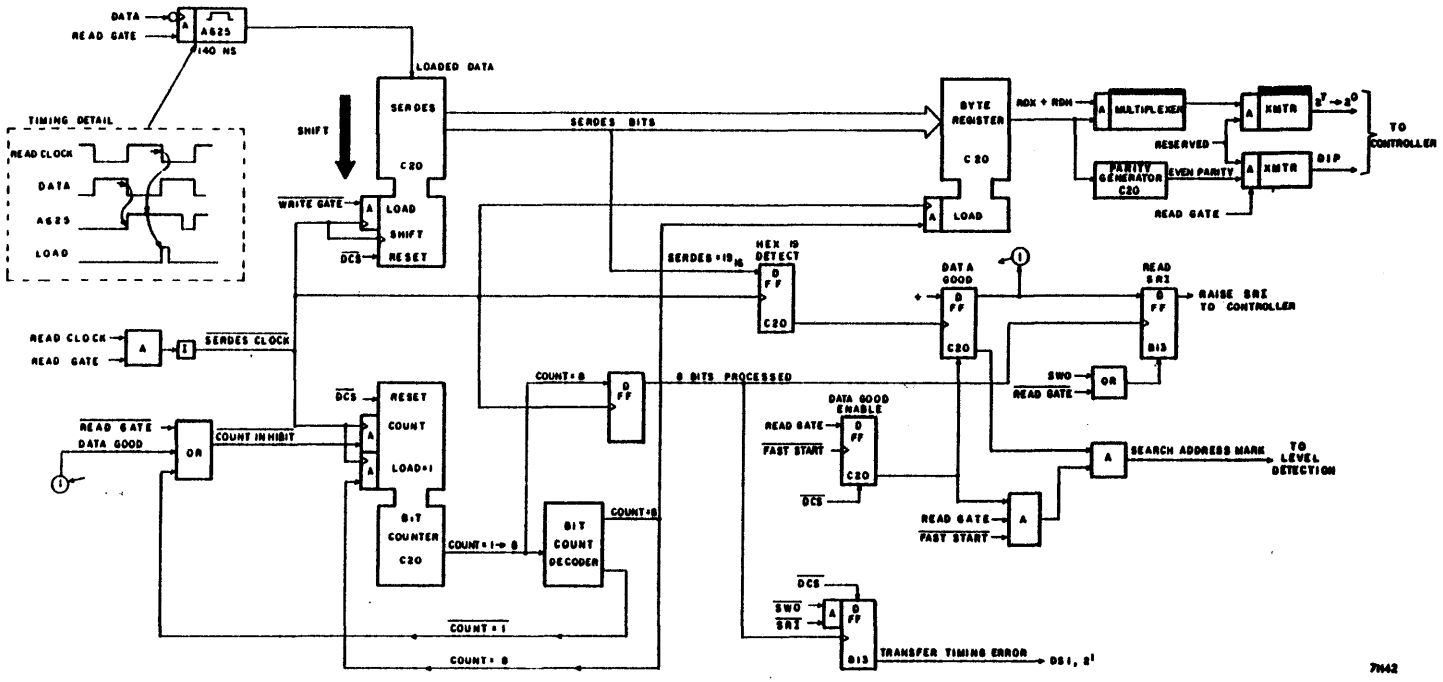
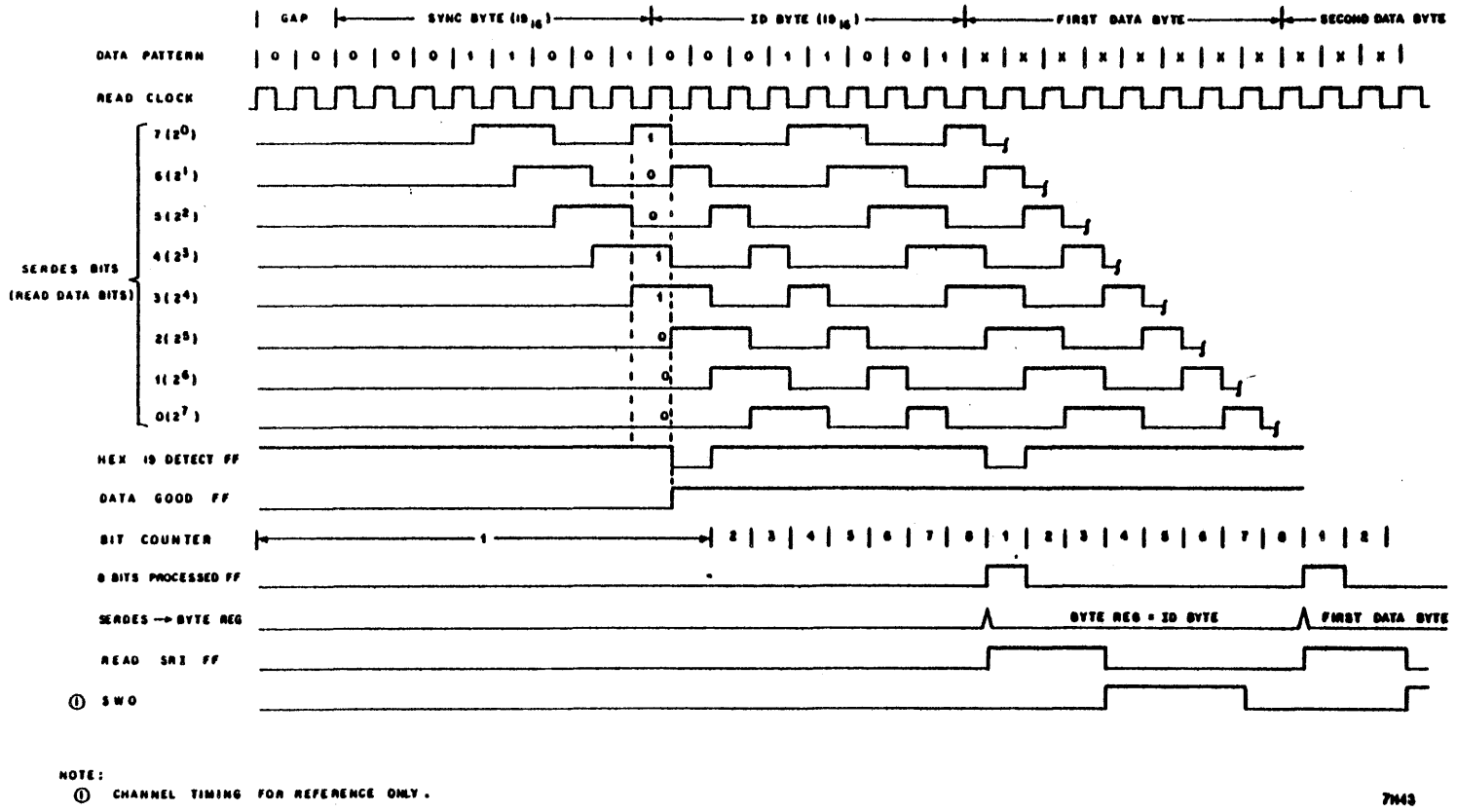


Figure 3-53. SERDES Read Circuit



NOTE:
① CHANNEL TIMING FOR REFERENCE ONLY.

7143

Figure 3-54. Read Timing

Read In down. Whenever the byte register contains an even number of "1" data bits, a parity generator automatically turns on DlP. Odd parity is, therefore, checked. Parity is not checked at the drive to ensure that there is not a Data Parity Error.

e. The 8 Bits Processed FF sets. This sets the Read SRI FF.

f. Serial Read In is raised to the controller to indicate that data (ID byte) on the bidirectional data lines is valid.

11. When the controller accepts the information, it raises Serial Write Out.

12. The drive drops Serial Read In until the next 8 Bits Processed.

13. The Serial Read In/Serial Write Out dialog continues without interruption until the controller drops DCS.

Note that the first byte, the sync byte, is recognized by SERDES but does not generate SRI. Only the ID byte and all subsequent data bytes are transferred.

If the controller is late in raising Serial Write Out another data byte could be loaded into the byte register before the resident byte is accepted. If this happens, Transfer Timing Error (bit 2^1 of DS1) is generated to raise FLT. This FLT does not, in itself, terminate the read operation.

Serdes During A Read Header (RDH)

A Read Header (RDH) command is identical to Read, except that data cannot be returned to the controller until an address mark is detected prior to the sync byte.

Except as specified herein, SERDES works in the identical manner for both Read and Read Header.

Assume that the read head is reading the inter-record gap of zeros. The controller raises Read Header and Device Command Strobe. Sequencing is as follows:

1. Because Read Header does not generate the Resync Pulse used to initiate Fast Start (Figure 3-51) that signal is not available. (It timed out following the last Read Enable).

2. The Data Good Enable FF remains reset since there is no Not Fast Start edge to toggle the FF. Data Good cannot set if the controller inadvertently raised RDH preceding a record field without an address mark.

3. With both the Data Good FF and Data Good Enable FF cleared. Search Address Mark is raised to the level Time Constant Control circuit (Figure 3-49).

4. Nothing of further consequence happens until the address mark gap (transitionless area) is sensed. Delay Y808 (Figure 3-51) can then time out.

5. When the first MFM Clock of the sync field is sensed, the resulting X pulse retriggers Y808 which, in turn, triggers Fast Start single shot Y806. Fast Start is up for 5 microseconds.

6. With Fast Start up, Search Address Mark is disabled.

7. After about 4 bytes of the 12 byte sync field (all zeros), Fast Start drops.

8. The Data Good Enable FF sets to permit the Data Good FF to set when the hex 19 of the sync byte is loaded into SERDES.

The remaining operation of Read Header is identical to the Read operation already explained.

SENSE OPERATIONS

GENERAL

Sense operations permit the controller to determine drive status.

SUMMING STATUS REQUEST (SSR)

The SSR command causes the transfer of one byte of data from the drive to the controller. This command does not require a previous Seize command. It is decoded directly off of the command lines without passing through the normal command decode logic. The only requirement is that the drive be online. The meanings of each bit in the SSR dialog are explained in Table 3-4 (Commands).

Two separate Summary Status Registers are provided within the drive: one for each controller. Current status is loaded from the logic into the applicable register when the SSR command is decoded. The register is gated to the DLI transmitters followed by a Serial Read In to indicate that the data is valid.

SSR status may also be determined during maintenance by setting the DISPLAY SELECT switch on the maintenance panel to SSR. This gates the status information (while bypassing the Summary Status Register) to the display indicators. Bit 2^8 (not used), bit 2^7 (Device Reserved), and bit 2^6 (Device Seized) indicators are always off. Data placed on the bidirectional data lines is applied to

the maintenance panel indicators and is theoretically available. However, except during maintenance, the signals are not up long enough for the LED indicators to react.

FAULT DETECTION

The drive contains extensive logic to monitor its internal operations and the DLI dialog. If any critical component or functions operate outside of their required parameters, the malfunction is defined as a fault. This raises the FLT line to the controller.

There are two types of fault. Device Fault (SSR bit 2^4) indicates an internal hardware failure. A simplified illustration of circuits used to generate this fault is provided by Figure 3-55. Refer to the applicable detailed operation theory (seeks, etc.) for further information. DLI Error (SSR bit 2^3) indicates that the normal controller/drive data transfer is erroneous. See Figure 3-56 for the simplified logic; refer to Command Operations for additional information.

Detailed Status Bytes (DSB)

Up to five bytes of additional status information may be obtained by means of the DS1 through DS5 commands (tags 29 through 20). These bytes further define status to indicate the cause of a fault or other status data. These commands require a successful Seize sequence. Status bytes and their bit meanings are defined in Table 3-4.

When an error occurs, the corresponding DSB flip-flop is set to raise FLT and to store the information. Even through the cause of the fault may be removed, the status will continue to be stored until it is cleared by either the specific DS- command or by a Device Initialize signal.

Certain errors require that the cause of the error be removed. For example, Seek Incomplete (DS3 bit 2) requires a DS3 command to drop the status. However, the internal malfunction must be cleared by prior Recalibrate command. In this case, DS3 will not fully reset the DS3 status bit: it is immediately set again by Seek Incomplete if there has not been a Recalibrate or its equivalent command.

DSB bits specified as status, (Heads Retracted, etc.), do not set DSB flip-flops. Current status is examined only while the command is being executed. The status itself remains unaffected.

DIAGNOSTIC OPERATIONS

GENERAL

Diagnostic operations permit the controller to check certain elements of the seek, angular position, and write circuits. See Figure 3-57.

DIAGNOSTIC COMMANDS

The drive enters the diagnostic mode when it is Online, seized, and has received a Set Diagnostic Mode (SDM) or Set Diagnostic Escape (SDE) command. Either command sets bit 2^0 of the Summary Status Register, SDM itself has no further effect on drive operations. The SDE command conditions the drive so that it can accept an additional command set not available during normal operations. SDM need not precede SDE. For further information on diagnostic operations, refer to the following discussions earlier in this section.

- Command functions are listed in Table 3-3.
- A list of Test and Diagnostic Commands is provided in the Device Level Interface portion.
- Angular Position In and Increment Sector Counter commands are in the Sector Circuit explanation.
- Fault conditions generated by invalid commands are explained in Sense Operations.
- Write Operations portion provides theory on the write driver logic.

The drive is released from the diagnostic mode if the controller issues a Reset Diagnostic Mode (RDM) or Device Initialize (DIN). Either command also initiates an automatic RTZS sequence.

WRITE TEST DIAGNOSTICS

The write test diagnostics (Write Test and Write Test Check) check the write portion of SERDES and the write toggle. A typical sequence of operations would be as follows:

NOTE

Sequencing is for reference only. Actual sequencing or data patterns may differ from this explanation.

1. Controller issues Set Diagnostic Escape.

2. Controller issues Write Test command. This enables the normal write circuitry. The normal Serial Read In/Serial Write Out dialog explained in Write Operations begins.

3. Controller writes a selected number of bytes with a 10101010 pattern.

   a. Data is processed by SERDES as it does during a normal Write command. As the NRZ data leaves SERDES, the bit toggling is checked by one-shot A676. It must receive a "1" at least once each 800 nanoseconds. Since the data pattern (10101010) normally creates toggles, SERDES is malfunctioning if the one-shot times out. This sets Not NRZ Toggle FF which, in turn, sets the NRZ Fault FF. See step 5.

4. Controller raises Data Modifier Line to inhibit MFM clock/data writing.

   a. Fault Inhibit A and Fault Inhibit B flip-flops set. They inhibit Current Fault FF (DS2 bit 2^5) as they do during regular address mark operations.

   b. Lack of write driver transitions generates a Current Fault. Although the Current Fault FF is inhibited, the fault is still indicated internally. If the fault is not generated (hardware error), Write $\overline{\text{Test}}$ Current Fault FF sets.

5. Controller drops Write Test and raises Write Test Check.

   a. If NRZ Fault (error condition) occurred in step 5, bit 2^0 of the bidirectional data lines is true.

   b. If a Current Fault did not occur in step 4, bit 2^1 of the bidirectional data lines is true.

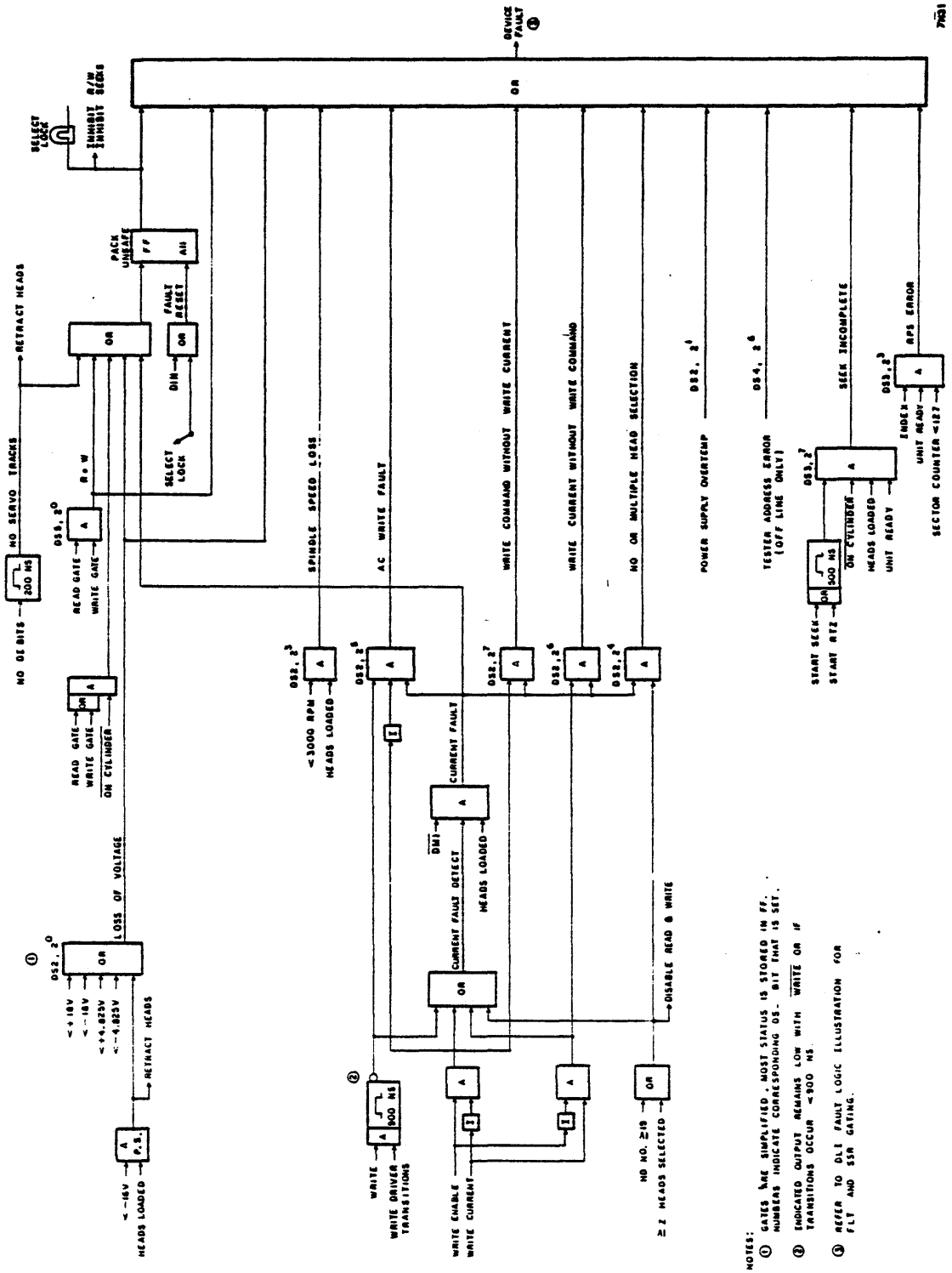


Figure 3-55. Device Fault Logic

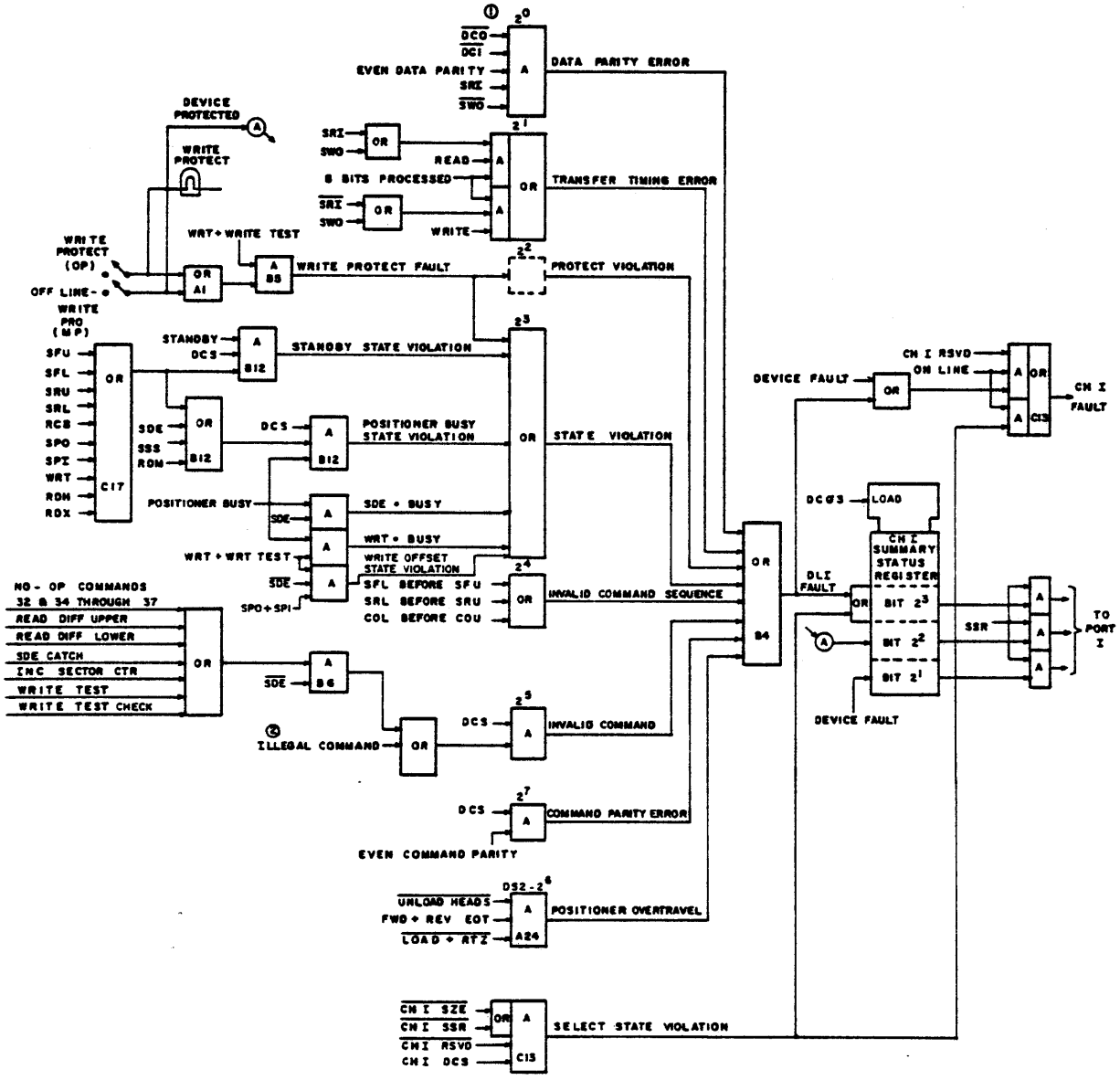
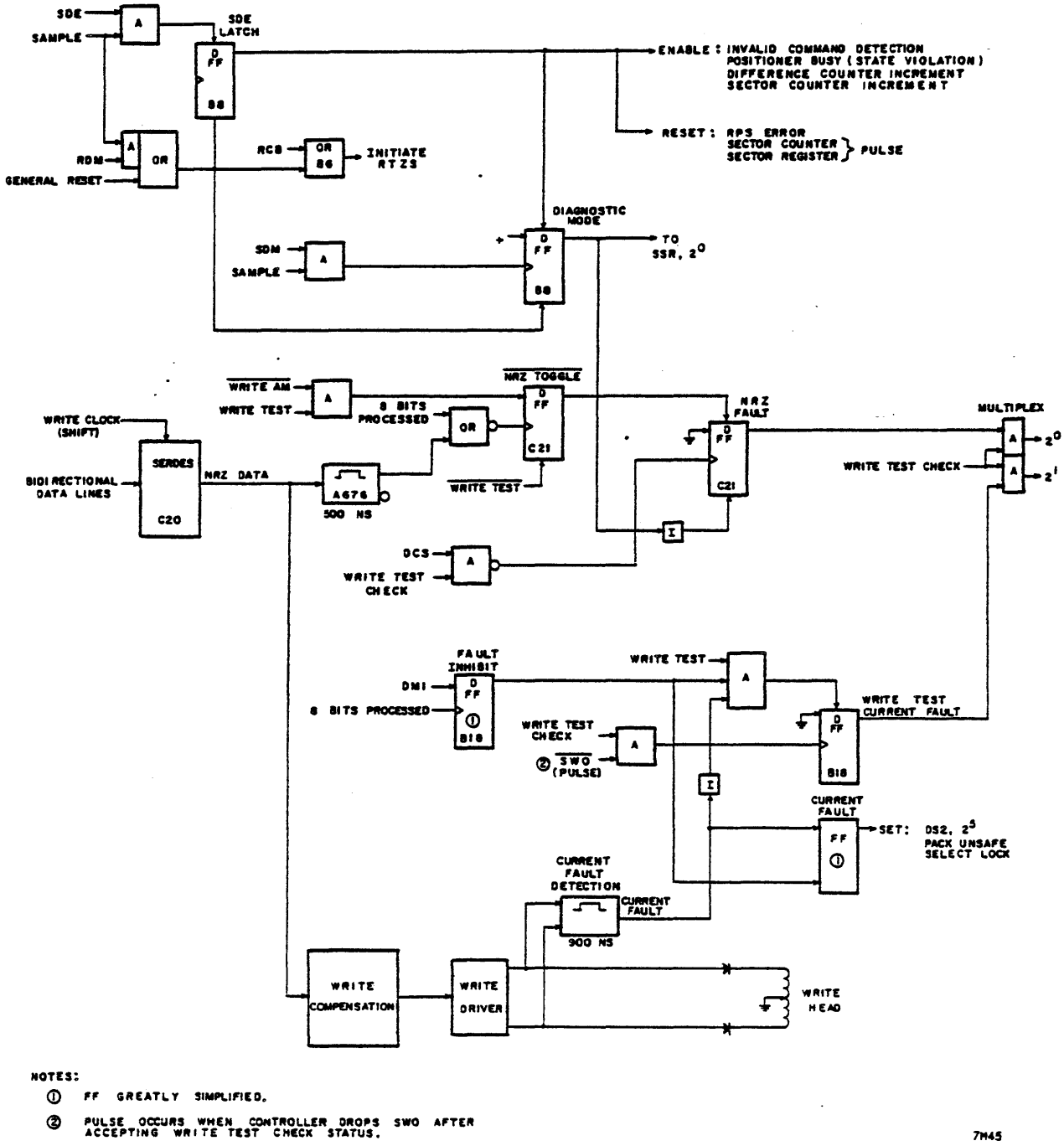


Figure 3-56. DLI Fault Logic



NOTES:

① FF GREATLY SIMPLIFIED.

② PULSE OCCURS WHEN CONTROLLER DROPS SWO AFTER ACCEPTING WRITE TEST CHECK STATUS.

7M45

Figure 3-57. Diagnostic Mode Logic

Mass Storage Unit

0402/0451

PARTS DATA

THIS DOCUMENT AND THE INFORMATION CONTAINED THEREIN IS CONFIDENTIAL AND PROPRIETARY TO AND THE EXCLUSIVE PROPERTY OF HONEYWELL INFORMATION SYSTEMS INC. IT IS MADE AVAILABLE ONLY TO HONEYWELL FIELD ENGINEERING DIVISION PERSONNEL FOR THEIR USE SOLELY IN THE MAINTENANCE AND OPERATION OF HONEYWELL PRODUCTS. THIS DOCUMENT AND INFORMATION MUST BE MAINTAINED IN STRICTEST CONFIDENCE; IT MUST NOT BE REPRODUCED, IN WHOLE OR IN PART; AND IT SHALL NOT BE DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF HONEYWELL.

Honeywell

THIS DOCUMENT AND THE INFORMATION CONTAINED THEREIN IS CONFIDENTIAL AND PROPRIETARY TO AND THE EXCLUSIVE PROPERTY OF HONEYWELL INFORMATION SYSTEMS INC. IT IS MADE AVAILABLE ONLY TO HONEYWELL FIELD ENGINEERING DIVISION PERSONNEL FOR THEIR USE SOLELY IN THE MAINTENANCE AND OPERATION OF HONEYWELL PRODUCTS. THIS DOCUMENT AND INFORMATION MUST BE MAINTAINED IN STRICTEST CONFIDENCE; IT MUST NOT BE REPRODUCED, IN WHOLE OR IN PART; AND IT SHALL NOT BE DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN CONSENT OF HONEYWELL.

83318300

MAGNETIC
PERIPHERALS, INC.

MAGNETIC PERIPHERALS®
DISK STORAGE UNIT
BR3C9
BR3E4
BR3E5

PARTS DATA

Volume 2 of 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released. Engineering Change Orders incorporated in manual: PE35322B,
(8-22-75)	PE35745B, PE35674A, PE35871, PE39278B, PE39306, PE39309, PE39312, PE39319, PE39324,
	PE39339, PE39351, PE39354, PE39358, PE39365C, PE39367, PE39368, PE39369, PE39406A.
B	Manual updated to incorporate Engineering Change Orders: 35816A, 35856C, 39336,
(11-4-75)	39411, 39412, 39436; Field Change Orders: 39411, 39436. This edition obsoletes
	all previous editions.
C	Manual updated to incorporate Engineering Change Orders: 35970, 35981, 39504.
(2-16-76)	Technical and editorial changes. This edition obsoletes all previous editions.
D	Incorporate Engineering Change Orders 39588, 47029. Document BR3E4/BR3E5.
(8-30-76)	Editorial changes.
E	Updated to incorporate technical and editorial changes.
(1-14-77)	
F	Manual revised to incorporate technical and editorial changes.
(5-24-77)	
G	Manual revised to incorporate technical and editorial changes.
(10-17-77)	
H	Manual revised to incorporate Engineering Change 47412B and editorial changes.
(12-2-77)	
J	Manual revised to incorporate technical and editorial changes. This edition
(6-20-78)	obsoletes all previous editions.
K	Manual updated to incorporate Engineering Change Orders: 47509D, 47624, 39875,
(1-29-79)	39869A, 39836. Technical and editorial changes. This edition obsoletes all
	previous editions.
L	Manual revised to incorporate Engineering Change Orders: 39860D, 39882D, 39948A,
(11-29-79)	39949, 47785A, 47782A. Technical and editorial changes. This edition obsoletes
	all previous editions.
M	Incorporate Engineering Change Orders PE39955, PE39957, PE47830,
(9-2-80)	PE47855, PE47859, PE47897, PE47898 and Technical changes.
N	Incorporate Engineering Change Orders PE47857, PE47956, PE47985, PE63002 and
(4-29-81)	Technical Changes.
P	Incorporate Engineering Change Orders PE63134, DH01043, DH01060 and Technical
(12-7-81)	Changes.

Revision letters I,O,Q and X are not used.

Address comments concerning this manual to:

Magnetic Peripherals Incorporated
Technical Publications Dept.
7801 Computer Avenue
Minneapolis, Mn 55435

©1975, 1976, 1977, 1978, 1979, 1980, 1981
Magnetic Peripherals, Inc.
Printed in the United States of America

MANUAL TO EQUIPMENT LEVEL CORRELATION

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

This correlation sheet also applies to the following related manuals:

Publication No._____ Rev._____ Publication No._____ Rev._____

Publication No. 83318100 Rev. L Publication No._____ Rev._____

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
BR3C9A/B/C/D BE3E4/3E5A/B			
	11	39365	
		39367	
		39406	BR3C9A/B ONLY
		39423	BR3C9B S/C 11 ONLY
		39435	BR3C9A/B ONLY
	12	39411	BR3C9A/B ONLY
		39436	BR3C9A/B ONLY
		39451	BR3C9A/B ONLY
	13	NONE	
	14	47185	BR3C9A/B ONLY
		47228	BR3C9D ONLY
	15	NONE	
	16	NONE	
	17	39688	
	18 thru 48	None	
	49		

LIST OF EFFECTIVE PAGES

Sheet 1 of 1

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Cover	-
Blank	-
Title P	-
ii	P
iii	P
Blank	-
v	P
Blank	-
vii	L
Blank	-
ix	L
Blank	-
1	D
2	L
3	L
Blank	-
5	M
6	P
7	P
Blank	-
9	P
10	P
11	P
12	P
13	P
14	L
15	L
16	L
17	L
18	L
19	M
20	L
21	L
22	L
23	M
24	P
25	N
Blank	-
27	P
28	N
29	M
30	L

PAGE	REV
31	M
32	M
33	P
34	L
35	L
36	L
37	M
38	L
39	L
40	L
41	L
42	L
43	L
44	N
45	N
46	L
47	M
Blank	-
49	L
50	N
51	L
Blank	-
53	N
54	M
55	P
Blank	-
57	L
58	L
59	L
60	L
61	L
62	L
63	L
64	L
65	L
Blank	-
67	P
Blank	-
Cmt Sh	-
Rtn Env	-
Blank	-
Cover	-

PAGE	REV

PAGE	REV

PAGE	REV

PREFACE

This manual contains illustrations and part number information. It has been prepared for customer engineers and other technical personnel directly involved with maintaining the disk storage unit (drive).

Information in this manual is applicable to all BR3C9 and BR3E4/5 disk storage units. For further information concerning the above units refer to the following manuals:

Publication No.	Title
83318100	Hardware Maintenance manual, Volume 1: Installation and Checkout, Preventive Maintenance, Corrective Maintenance, Diagrams, Wire Lists.
83318200	Hardware Reference Manual - General Description, Operation, Theory of Operation.
83318600	Logic Cards Manual: Key to Logic, Integrated Circuits, Discrete Circuits, Unique Card Schematics, Card Component Layout Diagrams.

CONTENTS

Figure	Title	Page	Figure	Title	Page
	Introduction	1	11	Actuator Assembly	36
1	Final Assembly	2	12	Pack Sensor Assembly	40
2	Main Frame Assembly	12	13	Air Supply Assembly	44
3	I/O Panel Assembly	14	14	Power Supply Assembly	46
4	Circuit Breaker Box Assembly	18	15	Logic Chassis Assembly	50
5	Top Cover Assembly	20	16	Component Assembly, Type 3ZCN	58
6	Control Panel Assembly	22	17	Plus Voltage Regulator Assembly	60
7	Main Deck Assembly	24	18	Minus Voltage Regulator Assembly	62
8	Pack Access Cover Assembly	30	19	Sensing Board Assembly	64
9	Drive Motor and Brake Assembly	32		Card Complement	67
10	Read/Write Pin and Guide Assembly	34			

INTRODUCTION

This manual provides the information needed to order field replaceable parts for BR3C9, BR3E4, BR3E5 Disk Storage Unit (DSU).

Information within this manual is provided by representative illustrations and their companion parts lists. The parts shown on the illustrations are assigned index numbers. These numbers cross reference the illustrations to the associated parts lists. The first illustration in the manual shows the complete DSU. Subsequent illustrations progressively break the unit down into its component parts and assemblies.

The parts lists associated with each illustration are organized in four columns:

- The Index Number column cross references the applicable entry to the associated illustration. When more than one entry is given for a particular index number, the use of the particular part is defined in the Notes column.

- The Part Number column provides the eight digit number by which a part may be ordered. In some cases the last two digits (referred to as Tab numbers) may be shown as "xx". This situation exists when an assembly (which is not normally considered field replaceable) changes tab numbers rapidly in the course of normal factory build. If if is necessary to order an assembly which is catalogued in this manner, the actual part number can usually be found on the part number label attached to the assembly. If the actual part number cannot be determined, be sure to include on the order the series code of the machine, and a listing of all the change orders installed.

- The Description column provides the part nomenclature. This column also provides information on the relationship of parts and assemblies. This is accomplished by means of indentation within the column . An indented item is part of a previous assembly which is indented to a lesser degree.

- The Notes column is used to show differences in configuration when more than one configuration of a machine is covered in the manual. This is shown by identifying a Model Level (Mod A), by identifying a machine series code and change order number (S/C 10 with PE35537), or by identifying the last two digits of the eight digit assembly part number to which the particular part applies (Tab 17).

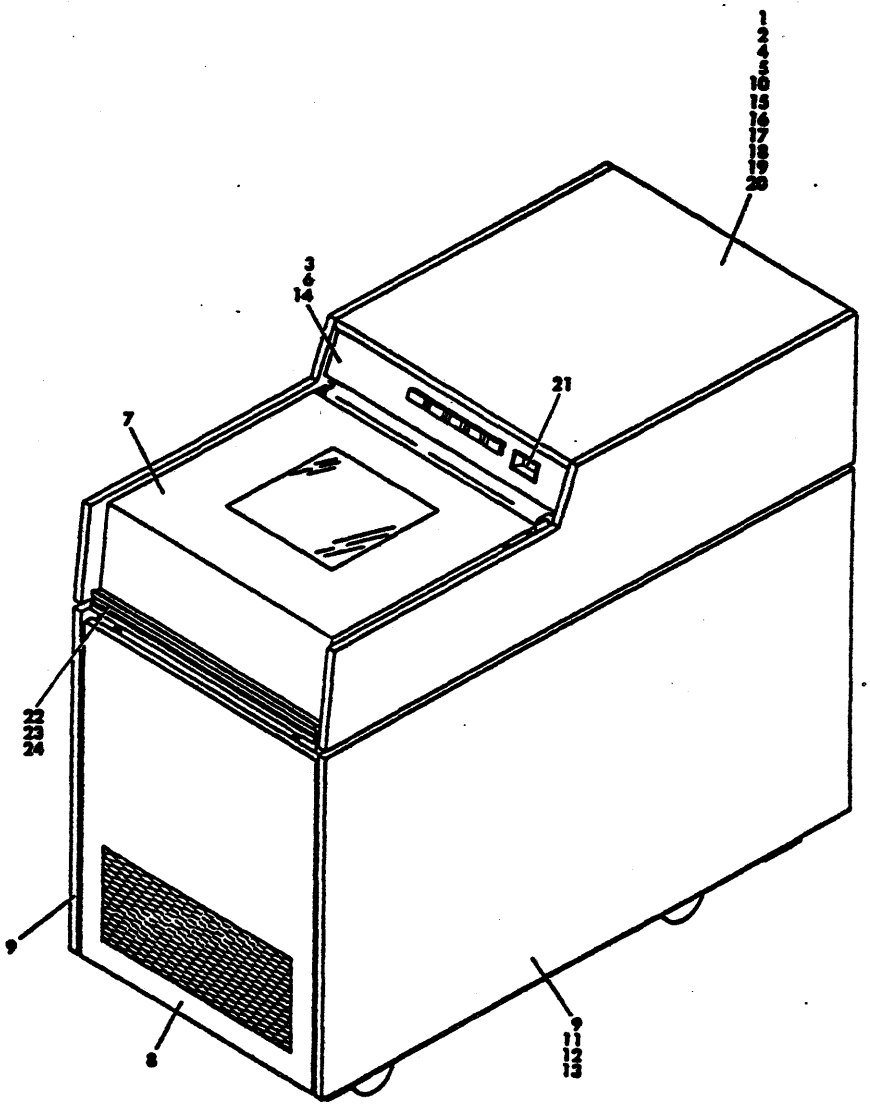


FIGURE 1. FINAL ASSEMBLY (SHEET 1 OF 3)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
1-	752100xx	FINAL ASSEMBLY (SHEET 1 OF 2)	
1		TOP COVER ASSEMBLY (SEE FIGURE 5)	
2	10125607	WASHER, FLAT, 10	
3	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
4	10125108	NUT, HEX, 10-32	
5	10127144	SCREW, MACHINE, PAN HEAD, PHILLIPS,10-32 x 5/8	
6	10127141	SCREW, MACHINE, PAN HEAD, PHILLIPS,10-32 x 5/16	
7		PACK ACCESS COVER ASSEMBLY (SEE FIGURE 8)	
8	736710xx	FRONT PANEL ASSEMBLY	S/C 25 & BELOW
8	472672xx	FRONT PANEL ASSEMBLY	S/C 26 & ABOVE
	75029946	PANEL, FRONT, REBEL RED	
	75029929	PANEL, FRONT, WHITE	
	75029927	PANEL, FRONT, BLUE	
	75029990	PANEL, FRONT, HUNTER RED	
	75029992	PANEL, FRONT, AZTEC YELLOW	
	75029986	PANEL, FRONT, MARITIME	
	75029957	PANEL, FRONT, MARINE	
	75029988	PANEL, FRONT, LOBSTER	
	75029987	PANEL, FRONT, SCARAB	
	75029946	PANEL, FRONT, HORIZON	
	75029966	PANEL, FRONT, BERMUDA TAN	
	75029968	PANEL, FRONT, MIST	
	92628323	TAPE, FOAM	
	75045200	HOOK, PANEL	
	93592458	SCREW, MACHINE, HEX HEAD, STP, 10-24 x 3/8	
	93573006	STUD ASSEMBLY	S/C 25 & BELOW
	93573014	STUD ASSEMBLY	S/C 26 & ABOVE
	93572001	RING	
	93571003	GROMMET	
	75031901	PANEL, ACOUSTICAL	
	94276602	TAPE, FOAM	
	94281432	CABLE, GROUND	
	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
	09040204	WASHER, LOCK, DISHED TYPE	
9	750036xx	SIDE PANEL ASSEMBLY	
	75007528	PANEL, SIDE, BLACK	
	75007570	PANEL, SIDE, INDIGO	
	75007599	PANEL, SIDE, BRIAR	
	75007569	PANEL, SIDE, MINT	
	75007568	PANEL, SIDE, MIST	
	75007545	PANEL, SIDE, DARK GOLD	
	75040409	PANEL, FOAM, ACOUSTICAL	
	40029800	BRACKET, RECEPTACLE	
	94303500	RECEPTACLE, CLIP-IN	
	93592428	SCREW, TPG, 10-32 x 3/8	
	75194501	BRACKET, SUPPORT	
	75194500	BRACKET, SUPPORT	
	75040408	PANEL, FOAM, ACOUSTICAL	
	10127120	SCREW, MACHINE, PAN HEAD,PHILLIPS,8-32 x 1/4	
	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
	76429347	SEAL, ACOUSTICAL (TOP AND BOTTOM)	
	76429348	SEAL, ACOUSTICAL (SIDES)	

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
1-	752100XX	FINAL ASSEMBLY (SHEET 2) (Contd)	
10	72818101	PLATE, NUT	
11	10126500	SCREW, MACHINE, HEX HEAD, PLAIN, 1/4-20 x 1/2	
12	10126404	WASHER, LOCK, EXTERNAL TOOTH, 1/4	
13	10125301	NUT, HEXAGON, 1/4-20	
14		CONTROL PANEL ASSEMBLY (SEE FIGURE 6)	
15		NOT USED	
16	72959300	LABEL, FIELD CHANGE ORDER	
17	73229609	LABEL, COMMON TEST POINT	
18	24547508	PLATE, WARNING	
19	94060004	CHANNEL, RUBBER	
20	75040411	PANEL, FOAM, ACOUSTICAL	
21	77549300	LOGIC PLUG KIT	
22	75029401	HANDLE, COVER	
23	10127142	SCREW, MACHINE, PANHEAD, 10-32 x 3/8	
24	09040204	WASHER, LOCK, DISHED TYPE	
	76533906	STRIP, DECORATIVE, BLACK	

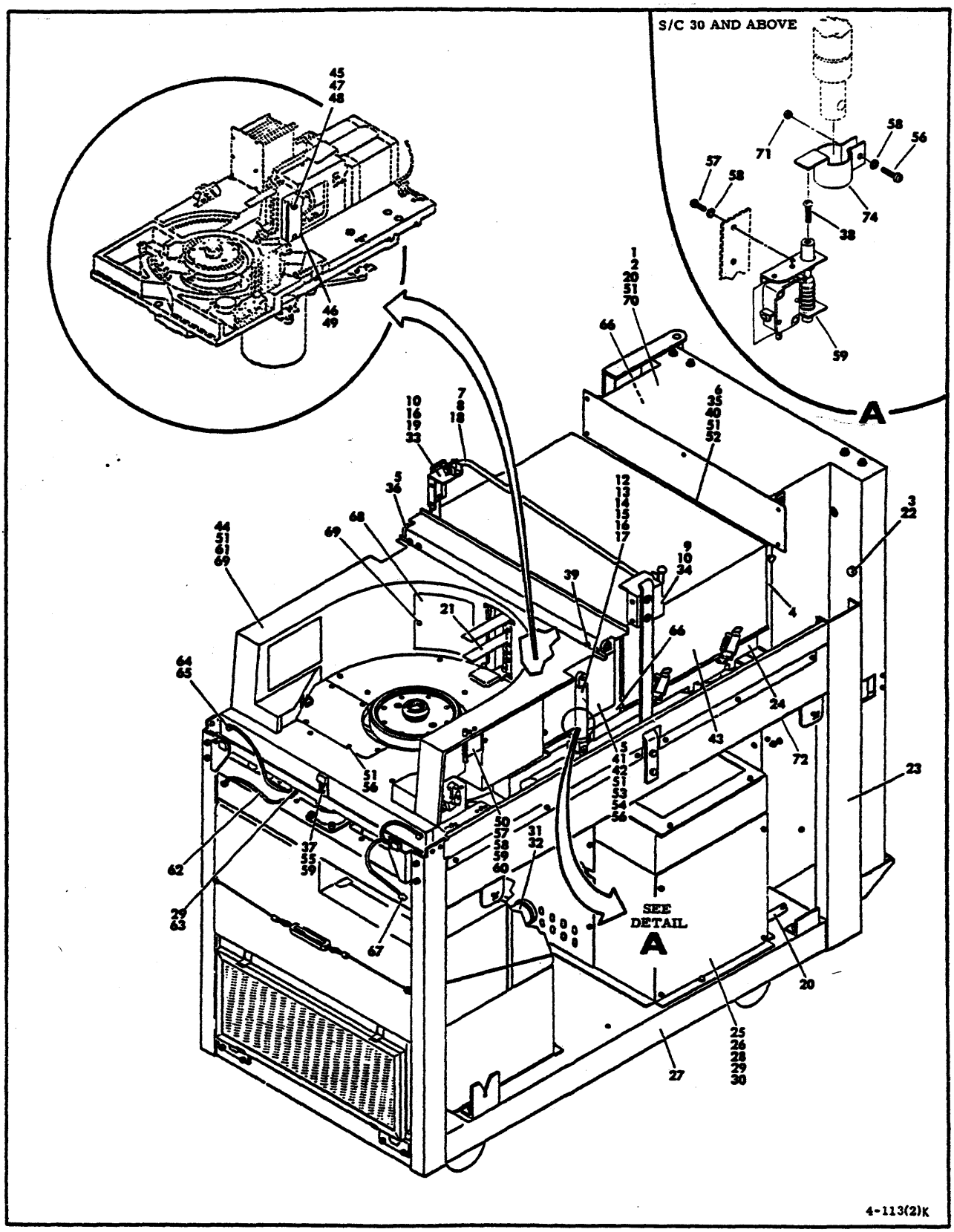


FIGURE 1. FINAL ASSEMBLY (SHEET 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
1-		FINAL ASSEMBLY (SHEET 2)	
1		LOGIC CHASSIS ASSEMBLY (SEE FIGURE 15)	
2	75003509	LOGIC CHASSIS REAR COVER ASSEMBLY	S/C 25 & BELOW
2	47259609	LOGIC CHASSIS REAR COVER ASSEMBLY	S/C 26 & ABOVE
	75026228	COVER, REAR, LOGIC CHASSIS	S/C 25 & BELOW
	47257928	COVER, REAR, LOGIC CHASSIS	S/C 26 & ABOVE
	10127120	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 1/4	
	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
	94281432	CABLE, GROUND (LOGIC REAR COVER TO LOGIC CHASSIS)	
3	10125108	NUT, HEXAGON, 10-32	
4	75032803	CARD COVER ASSEMBLY	
	75028300	COVER, CARD	
	00855701	GROMMET, PUSH-PULL	
	94281473	CABLE, GROUND (FROM CARD COVER)	
	10125804	WASHER, SPRING LOCK, 8	
	10125106	NUT, HEXAGON, 8-32	
	10127121	SCREW, MACHINE, PAN HEAD, PHILLIPS,8-32x5/16	
	93783102	FASTENER, PUSH-PULL, BLACK	
5	94276600	TAPE, FOAM	
6	93590164	SCREW, PAN HEAD, PHILLIPS, TPG, 6-32 x 1/2	
7	75030000	ROD, SUPPORT, TOP COVER	
8	92649009	PIN, COTTER, 1/16 x 1/2 x 6	
9	92953329	SCREW, MACHINE, FLAT HEAD,PHILLIPS,1/4-20 x 5/8	
10	75029500	PLATE, NUT, CONTROL PANEL	
11	93592238	SCREW, HEX HEAD, STP, 10-24 x 3/8	
12	94354901	SPRING, GAS	
13	92033221	RING, RETAINING	
14	73229002	STUD	
15	76374201	BRACKET, SPRING, BOTTOM, LEFT & RIGHT	S/C 29 & BELOW
15	76374201	BRACKET, SPRING, BOTTOM, LEFT ONLY	S/C 30 & ABOVE
15	82379200	BRACKET, SPRING, BOTTOM, RIGHT	S/C 30 & ABOVE ONLY
16	93592238	SCREW,SELF-TAPPING, 10-24 x 3/8	
17	94217702	NUT, SELF-LOCKING	
18	10125609	WASHER, FLAT, 5/16	
19	93592240	SCREW, MACHINE, WASHER HEAD, 10-24 x 1/2	
20	40016108	CABLE ASSEMBLY, W1	BR3C9 MOD A,B BR3E4/5 MOD A
20	40016126	CABLE ASSEMBLY, W1	BR3C9 MOD C,D BR3E4/5 MOD B
21		HEAD ARM COMPLIMENT (SEE FIG. 7, SHEET 1)	
22	94193401	BUMPER, RUBBER	
23	78816905	DECK, FRAME, AND POWER SUPPLY ASSEMBLY	BR3C9 MOD A,B BR3E4/5 MOD A
23	78816906	DECK, FRAME, AND POWER SUPPLY ASSEMBLY	BR3C9 MOD C,D BR3E4/5 MOD B
24		DECK ASSEMBLY (SEE FIG. 7)	
25	75214607	FRAME AND POWER SUPPLY ASSEMBLY	BR3C9 MOD A,B BR3E4/5 MOD A
25	75214608	FRAME AND POWER SUPPLY ASSEMBLY	BR3C9 MOD C,D BR3E4/5 MOD B
26		POWER SUPPLY ASSEMBLY (SEE FIG. 14)	
27		FRAME ASSEMBLY (SEE FIG. 2)	
28	10126500	SCREW, MACHINE, HEX HEAD, PLAIN, 1/4-20 x 1/2	
29	10126404	WASHER, LOCK, EXTERNAL TOOTH, 1/4	
30	10125608	WASHER, FLAT, 1/4	
31	94311619	HOSE, FLEXIBLE	
32	94279412	BUTTON, PLUG	
33	76381700	BRACKET, CONTROL PANEL, LEFT HAND	
34	76538300	BRACKET, CONTROL PANEL, RIGHT HAND	
35	75085100	PANEL, DECK, SEAL, REAR	
36	72873000	BLOCK, HINGE	
	94281477	CABLE, GROUND (CONTROL PANEL TO BLOCK HINGE)	
	73485034	COMPONENT ASSEMBLY, TYPE 3ZQN (SEE FIG. 16)	

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
1-		FINAL ASSEMBLY (SHEET 2 CONT)	
37	75080100	CATCH, COVER PACK	
38	82376500	CLAMP, SWITCH	S/C 30 & ABOVE ONLY
39	93187314	SCREW , MACHINE, HEX SOCKET,BUTTON HEAD,10-32 x 3/8	
40	94001102	TAPE, FOAM (BETWEEN DECK REAR SEAL AND DECK ASSEMBLY)	
41	76470701	PANEL, SHROUD, SIDE, RIGHT	S/C 29 & BELOW
41	47341901	PANEL, SHROUD, SIDE, RIGHT	S/C 30 & ABOVE
42	76470700	PANEL, SHROUD, SIDE, LEFT	S/C 29 & BELOW
42	47341900	PANEL, SHROUD, SIDE, LEFT	S/C 30 & ABOVE
43	73627702	DECK COVER ASSEMBLY	
	77418000	COVER, DECK	
	94356900	LATCH, SPRING	
	95037600	GASKET, RUBBER	
44	76405700	PACK SHROUD ASSEMBLY	S/C 12 W/O 35856C & BLW
44	77541400	PACK SHROUD ASSEMBLY	S/C 12 W/35856 & ABV
45		SERVO PREAMP ASSEMBLY (SEE CARD COMPLEMENT)	
46	73479900	COVER, PREAMPLIFIER	
47	73479800	HOUSING, PREAMPLIFIER	
48	93115247	SCREW,MACHINE, HEX SOCKET, CAP HEAD, 6-32 x 5/8	
49	93592084	SCREW, HEXAGON, WASHER HEAD, 4-40 x 5/16	
50	93342098	SCREW, NYLON, 4-40 x 3/8	
51	10125605	WASHER, PLAIN, 6	
52	93590162	SCREW, MACHINE, 6-32 x 3/8	
53	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
54	10127112	SCREW, MACHINE, PAN HEAD, 6-32 x 5/16	
55	10127114	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/2	
56	10127113	SCREW, MACHINE, PAN HEAD, 6-32 x 1/4	
57	92723196	SCREW, BUTTON HEAD, 6-32 x 1/4	
58	10126103	INTERNAL LOCK WASHER, 6	
59	93560001	SWITCH, INTERLOCK	LOCATED ON ARM OF SHROUD FOR S/C 29 & BELOW LOCATED AS SHOWN IN DETAIL A FOR S/C 30 & ABOVE
60	93154109	TUBING, HEAT SHRINKABLE	S/C 29 & BELOW
61	93749162	SCREW, PHILLIPS, 6-32 x 3/8	
62	94369514	CABLE, GROUND(DECK TO SHROUD AND FRONT PANEL)	
63	10127153	SCREW, MACHINE, PAN HEAD, 1/4-20 x 1/2	
64	10127363	SCREW, MACHINE, PAN HEAD, 10-32 x 3/8	
65	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
66	09040204	WASHER, LOCK, DISH TYPE	
67	94274140	TERMINAL, QUICK CONNECT	
68	76371000	COVER, SHROUD	
69	93343158	SCREW, NYLON, 6-32 x 1/4	
70	10127141	SCREW, Phillips, 10-32 x 5/16	
71	10125105	NUT, MACHINE, HEXAGON, 6-32	S/C 30 & ABOVE ONLY
72	94237703	TRIM, SAFETY	

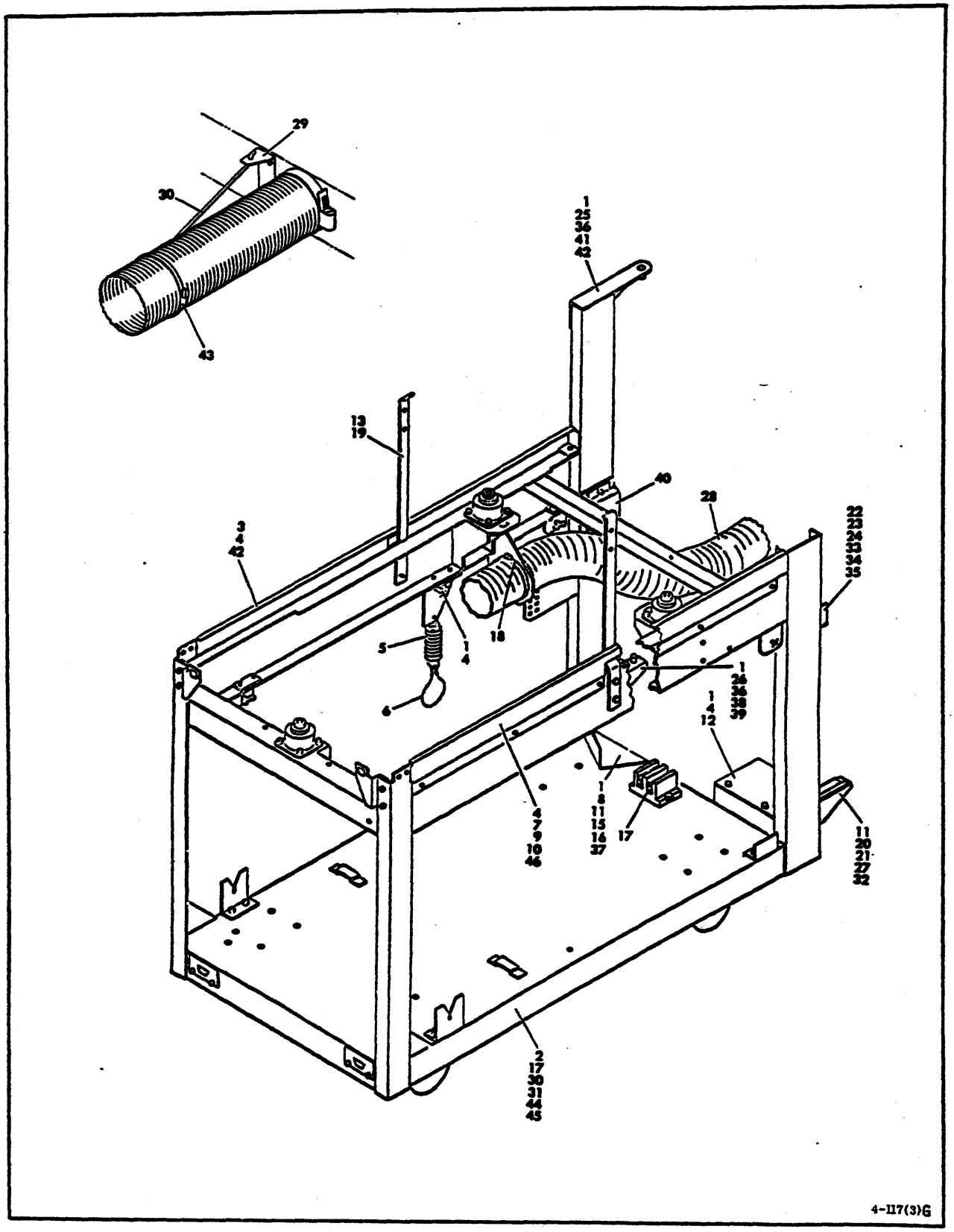


FIGURE 1. FINAL ASSEMBLY (SHEET 3)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
1-		FINAL ASSEMBLY (SHEET 3)	
1	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
2	93697020	LEVELER	S/C 39 W/047857 & BLW
2	94402800	LEVELER	S/C 39-40 W/ 47857
2	94402801	LEVELER	S/C 40 W/47956 & ABV
3	82390401	BELTLINE, SIDE, LEFT	
4	93592428	SCREW, MACHINE, HEX HEAD, PLAIN, 10-32 x 3/8	
5	94204269	SPRING, EXTENSION	
6	73559903	CABLE, BRAKE ACTUATOR	
7	76506200	BELTLINE, SIDE, RIGHT	S/C 25 & BLW
7	82390601	BELTLINE, SIDE, RIGHT	S/C 26 & ABV
8		I.O. PANEL ASSEMBLY (SEE FIGURE 3)	
9	76522100	CATCH, TOP COVER	S/C 26 thru 35
9	47402700	CATCH, TOP COVER	S/C 36 & ABV
10	93994003	RIVET, OPEN END, POP TYPE	S/C 26 thru 35
10	93994002	RIVET, OPEN END, POP TYPE	S/C 36 & ABV
11	10125607	WASHER, PLAIN, 10	
12		CIRCUIT BREAKER BOX (SEE FIGURE 4)	
13	10126502	SCREW, MACHINE, HEX HEAD, 1/4-20 x 3/4	
14	10127141	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 5/16	
15	10125031	SCREW, MACHINE, HEX HEAD, 8-32 x 5/8	
16	94277406	STRAP, CABLE TIE	
17	75081611	FINAL GROUNDING ASSEMBLY	
	53714400	TERMINAL BLOCK, GROUNDING	
	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
	94297000	CABLE, GROUND (GROUND BLOCK TO FRAME)	
	94297011	CABLE, GROUND (GROUND BLOCK TO FINAL GROUNDING)	
	93592202	SCREW, MACHINE, HEX HEAD, 8-32 x 1/2	
18	94275213	CLAMP, HOSE	
19	76373000	BAR, MOUNTING, CONTROL PANEL	
20	47278201	LOGIC SUPPORT ASSEMBLY	
	72822800	BLOCK, SUPPORT	
	10127131	SCREW, PAN HEAD, MACHINE, 10-24 x 3/8	
	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
	75084600	SUPPORT, LOGIC FRAME	
21	10126245	SCREW, SOCKET HEAD, 10-32 x 5/8	
22	76398400	PLATE, NUT, KEEPER	
23	76398300	CATCH, KEEPER	S/C 25 & BLW
23	82353100	CATCH, KEEPER	S/C 26 & ABV
24	75027500	KEEPER, BRACKET, MOUNTING	
25	75024900	HINGE, PIVOT, UPPER	
26	75024800	HINGE, PIVOT, LOWER	
27	10126500	SCREW, HEXAGON HEAD, 1/4-20 x 1/2	
28	94311607	HOSE, FLEXIBLE	
29	92033316	RING, RETAINING	
30	76535100	HINGE, HOSE SUPPORT	
31	94277503	BASE, MOUNTING	
32	10125301	NUT, HEXAGON, 1/4-20	
33	10125605	WASHER, FLAT, 6	
34	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
35	10127114	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/2	
36	10125062	SCREW, MACHINE, HEX HEAD, 10-32 x 1/2	
37	10127142	SCREW, PHILLIPS, 10-32 x 3/8	
38	10126501	SCREW, MACHINE, HEX HEAD, PLAIN, 1/4-20 x 5/8	
39	10125806	WASHER, LOCK, SPRING, 1/4	
40	47431200	SHROUD, CABLE GUIDE	
41	70738306	INSULATOR, MOTOR MOUNT	
42	72875100	CHANNEL, RUBBER	
43	94277418	STRAP, CABLE TIE	
44	73068801	LEVER, EXTENSION	S/C 39 W/ 47857 & ABV
45	93006035	NUT	S/C 39 W/ 47857 & ABV
	72920801	CABLE, EPO (PACKAGED W/44 & 45)	S/C 41 W/ 47985 & ABV. Used in BR3C9-J, K, BR3E4/5-E only
46	72875101	CHANNEL, RUBBER	

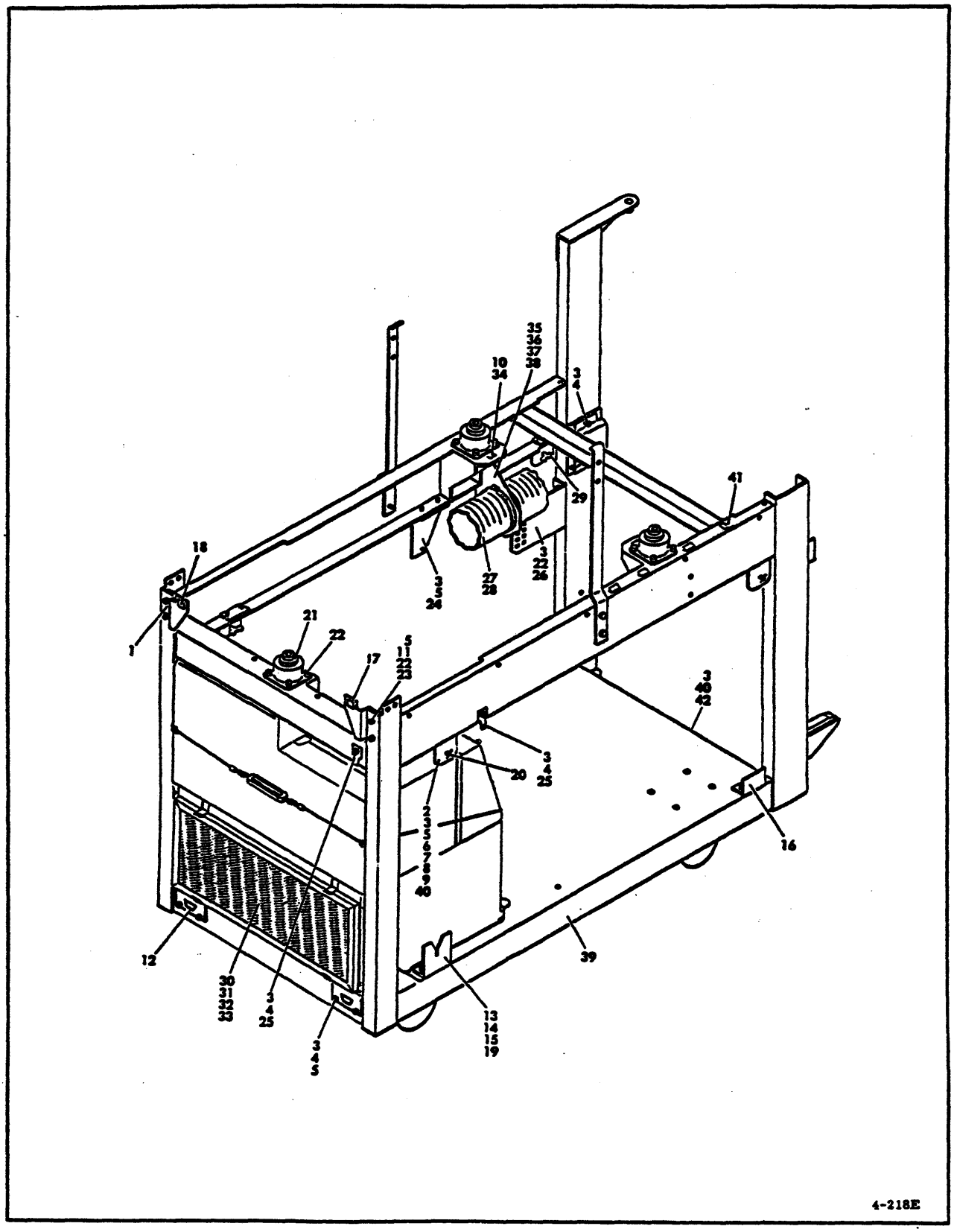


FIGURE 2. MAIN FRAME ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
2-	750968xx	MAIN FRAME ASSEMBLY	
1	75029300	BRACKET, FRONT PANEL	
2	10125062	SCREW, MACHINE, HEX HEAD, 10-32 x 1/2	
3	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
4	10127142	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 3/8	
5	10125607	WASHER, FLAT, 10	
6	40029500	BRACKET, STUD	
7	93571002	GROMMET	
8	93572001	RING, SNAP	
9	75031800	PLATE, NUT, SIDE PANEL	
10	93592240	SCREW, HEX HEAD, PNL, 10-24 x 1/2	
11	75030200	PLATE, NUT, FRONT PANEL	
12	76507400	PLATE, FRONT PANEL	
13	10126501	SCREW, MACHINE, HEX HEAD, PLAIN, 1/4-20 x 5/8	
14	10125608	WASHER, FLAT, 1/4	
15	10125806	WASHER, LOCK, SPRING, 1/4	
16	75007300	BRACKET, REAR PANEL	
17	75029301	BRACKET, FRONT PANEL	
18	94303500	RECEPTACLE, CLIP-IN	
19	75007400	BRACKET, SIDE PANEL	
20	93573017	STUD ASSEMBLY	
21	94245302	ISOLATOR, VIBRATION	
22	10127143	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 1/2	
23	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
24	75040600	BRACKET, MOUNTING, SPRING	
25	94274140	TERMINAL, QUICK CONNECT	
26	47181700	ANGLE, CABLE CLAMP	
27	94359401	HOSE, AIR, FLEXIBLE	
28	94275213	CLAMP, HOSE	
29	93573018	STUD ASSEMBLY	
30		AIR SUPPLY ASSEMBLY (SEE FIGURE 13)	
31	10126513	SCREW, MACHINE, HEX HEAD, PLAIN, 5/16-18 x 1/2	
32	10125609	WASHER, PLAIN, 5/16	
33	10126405	WASHER, LOCK, EXTERNAL TOOTH, 5/16	
34	93602322	NUT, HEX, 1/4-20	
35	75007000	SUPPORT, AIR HOSE	
36	10127123	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 1/2	
37	10125106	NUT, HEX, 8-32	
38	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
39	760258xx	FRAME, MAIN	
40	09040204	WASHER, LOCK, DISH TYPE	
41	94312902	CLIP, CABLE	
42	10125108	NUT, HEXAGON, 10-32	W/ CABLE GROUND - S/C 44 W/ 63134 & ABOVE

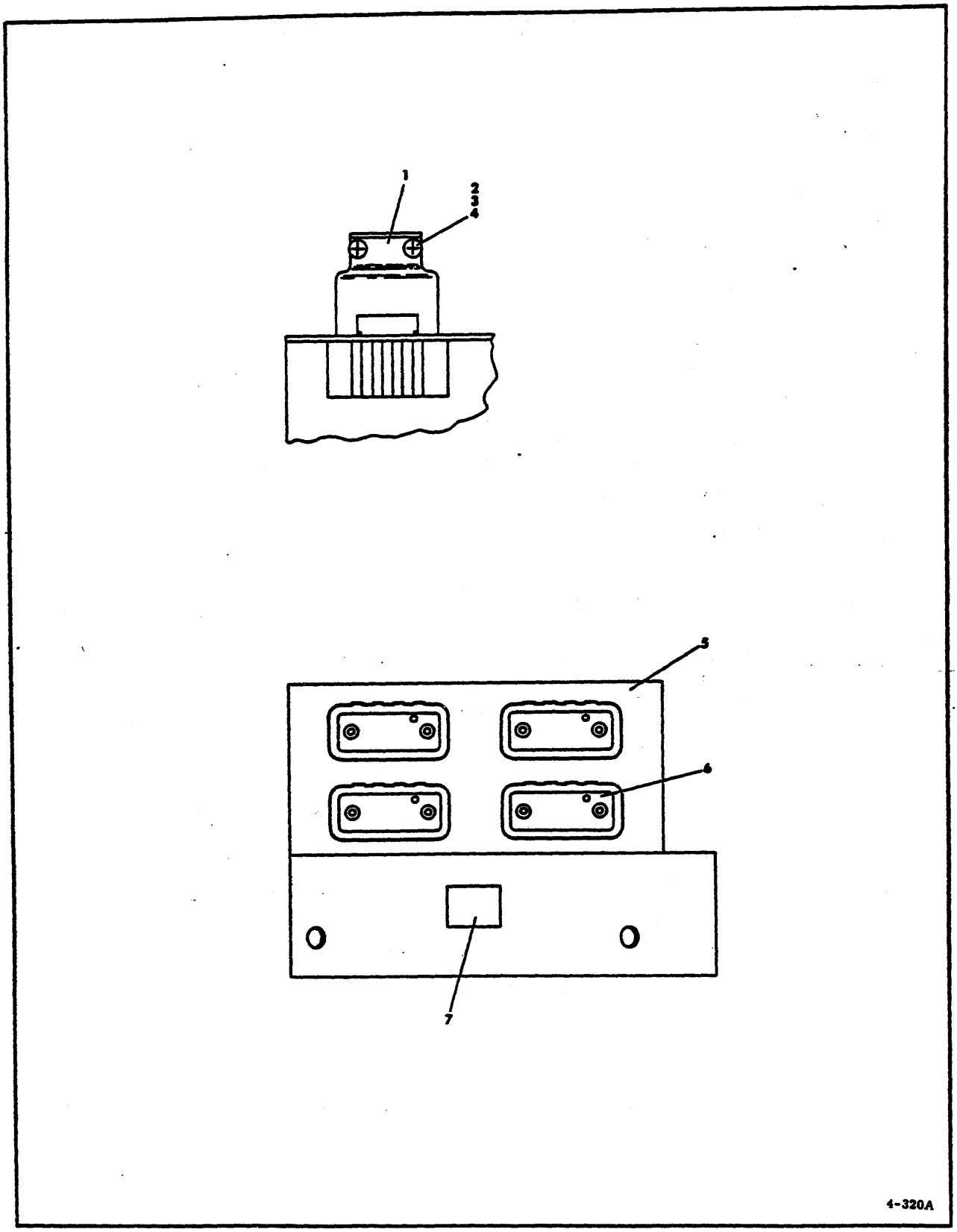


FIGURE 3. I/O PANEL ASSEMBLY (SHEET 1 OF 2)
ALL EXCEPT BR3C9J/K AND BR3E4/5E

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
3-	77538500	I/O PANEL ASSEMBLY	S/C 13 W/O 39412 & BLW
3-	77479400	I/O PANEL ASSEMBLY	S/C 13 W/ 39412 & ABV, ALL EXCEPT BR3C9J/K & BR3E4/5E
1	75080000	STRAIN RELIEF AND CLAMP	
2	10127106	SCREW, PAN HEAD, MACHINE, 4-40 x 5/8	
3	94168016	SLEEVING, INSULATION	
4	75080001	STRAIN RELIEF AND CLAMP	
5	77538200	PANEL, I/O	S/C 13 W/O 39412 & BLW
5	77473400	PANEL, I/O	S/C 13 W/39412 & ABV
6	94352508	CONNECTOR, RECEPTACLE	
7	94208501	LABEL	
	75008901	CABLE ASSEMBLY	

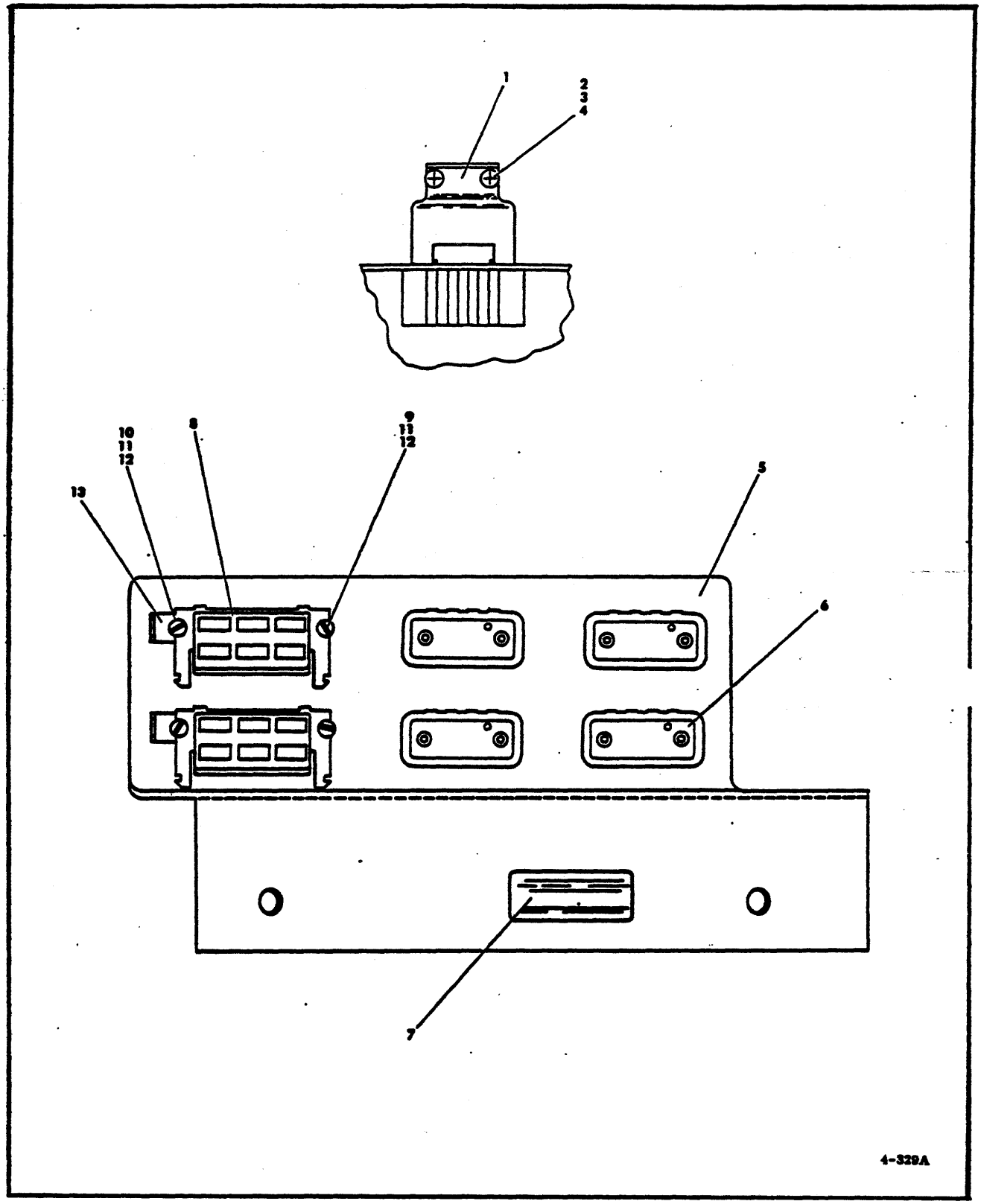


FIGURE 3. I/O PANEL ASSEMBLY (SHEET 2)
BR3C9J/K AND BR3E4/5E

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
3-	82385300	I/O PANEL ASSEMBLY	BR3C9J/K, BR3E4/5E
1	75080000	STRAIN RELIEF AND CLAMP	
2	10127106	SCREW, PAN HEAD, MACHINE, 4-40 x 5/8	
3	94168016	SLEEVING, INSULATION	
4	75080001	STRAIN RELIEF AND CLAMP	
5	77473400	PANEL, I/O	
6	94352508	CONNECTOR, RECEPTACLE	
7	94208501	LABEL	
8	94254700	HOUSING, RECEPTACLE	
9	10127113	SCREW, PAN HEAD, MACHINE, 6-32 x 3/8	
10	10127114	SCREW, PAN HEAD, MACHINE, 6-32 x 1/2	
11	10126401	WASHERS, EXTERNAL TOOTH, LOCK, 6	
12	10125105	NUT, HEXAGON, MACHINE, 6-32	
13	94274107	TERMINAL, QUICK CONNECT	
	75008901	CABLE ASSEMBLY	

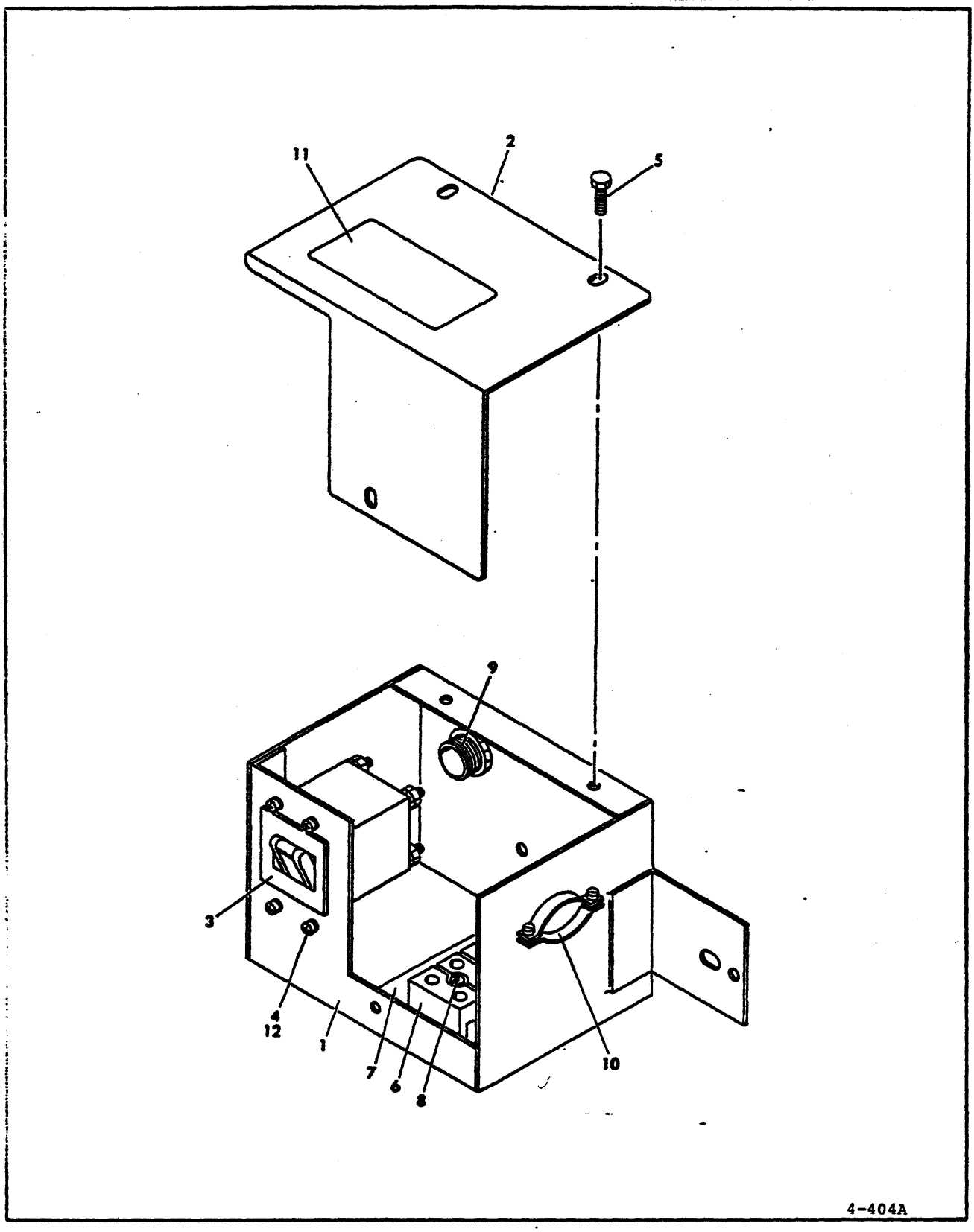


FIGURE 4. CIRCUIT BREAKER BOX ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
4-	75032904	CIRCUIT BREAKER BOX ASSEMBLY, 60HZ	SC 38 W/O 47897 & BLW
4-	75032933	CIRCUIT BREAKER BOX ASSEMBLY, 60HZ	SC 38 W/47897 & ABV
4-	75032931	CIRCUIT BREAKER BOX ASSEMBLY, 50HZ	SC 38 W/O 47897 & BLW
4-	75032934	CIRCUIT BREAKER BOX ASSEMBLY, 50HZ	SC 38 W/47897 & ABV
1	73594801	BOX, CIRCUIT BREAKER	
2	73594903	COVER, BOX, CIRCUIT BREAKER	
3	94245217	CIRCUIT BREAKER, LONG DELAY	
4	10127111	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/4	
5	93592196	SCREW, MACHINE, HEX HEAD, STP, 8-32 x 1/4	
6	18946007	TERMINAL BLOCK	
7	75032100	PLATE, TERMINAL MARKING	
8	94208666	SCREW, MACHINE, PAN HEAD, PHILLIPS,8-32 x 1-1/4	
9	92801001	CLAMP, CABLE	
10	92801002	CLAMP, CABLE	
11	46068603	PLATE, WARNING	
12	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	
	75043900	CIRCUIT BREAKER BOX HARNESS ASSEMBLY	

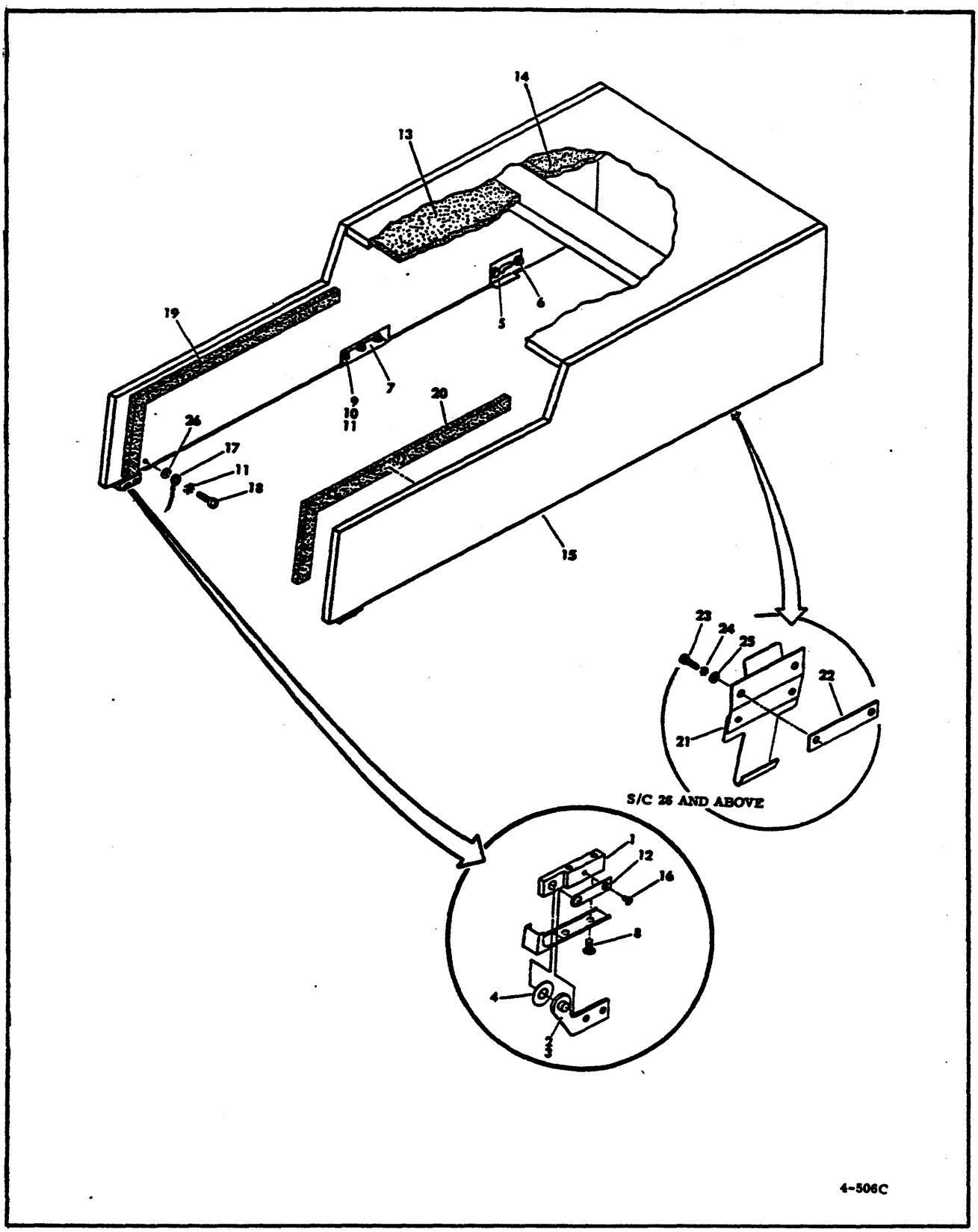


FIGURE 5. TOP COVER ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
5-	750032xx	TOP COVER ASSEMBLY	S/C 25 & BELOW
5-	472645xx	TOP COVER ASSEMBLY	S/C 26 & ABOVE
1	76533100	BASE, HINGE, TOP COVER	
2	76372900	SHAFT, HINGE BEARING	
3	76533401	HINGE, TOP COVER, LEFT	
	76533400	HINGE, TOP COVER, RIGHT	
4	93564028	WASHER, NYLON	
5	73628300	PLATE, SUPPORT ROD	
6	93994011	RIVETS, POP TYPE	
7	75026900	GUIDE, TOP COVER	
8	93187314	SCREW, BUTTON HEAD, SOCKET DRIVE, NYLOCK	
9	10125108	NUT, HEXAGON, 10-32	
10	10125607	WASHER, FLAT, 10	
11	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
12	76533300	PLATE, WEAR	
13	75040425	PANEL, ACOUSTICAL	
14	75040413	PANEL, ACOUSTICAL	
15	75008744	COVER, TOP, CHAMOIS	S/C 25 & BELOW
	75008729	COVER, TOP, WHITE	S/C 25 & BELOW
	75008771	COVER, TOP, HORIZON	S/C 25 & BELOW
	75008766	COVER, TOP, BERMUDA TAN	S/C 25 & BELOW
	75008768	COVER, TOP, MIST	S/C 25 & BELOW
	75008769	COVER, TOP, MINT	S/C 25 & BELOW
15	47263544	COVER, TOP, CHAMOIS	S/C 26 & ABOVE
	47263529	COVER, TOP, WHITE	S/C 26 & ABOVE
	47263571	COVER, TOP, HORIZON	S/C 26 & ABOVE
	47263566	COVER, TOP, BERMUDA TAN	S/C 26 & ABOVE
	47263568	COVER, TOP, MIST	S/C 26 & ABOVE
	47263569	COVER, TOP, MINT	S/C 26 & ABOVE
16	10125711	SCREW, FLAT HEAD, PHILLIPS, 6-32 x 3/16	
17	94281431	CABLE, GROUND	
18	10127142	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 3/8	
19	94389800	FOAM, STRIP	
20	94389801	FOAM, STRIP	
21	82379500	LATCH BRACKET ASSEMBLY	S/C 26 & ABOVE ONLY
22	94376715	NUT, PLATE	S/C 26 & ABOVE ONLY
23	17901509	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 3/8	S/C 26 & ABOVE ONLY
24	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	S/C 26 & ABOVE ONLY
25	10125605	WASHER, FLAT, 6	S/C 26 & ABOVE ONLY
26	09040204	WASHER, LOCK, DISHED TYPE	

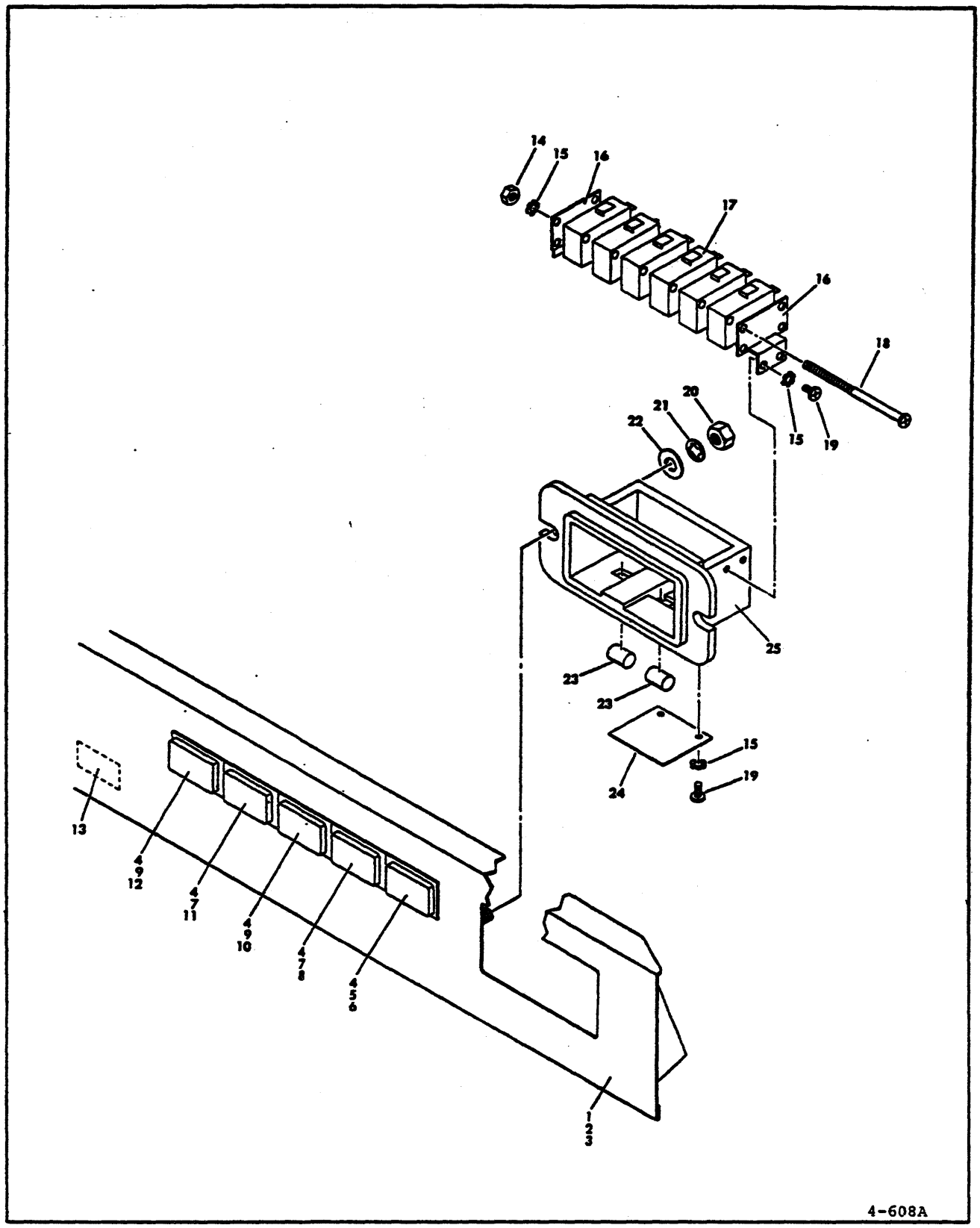


FIGURE 6. CONTROL PANEL ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
6-	77431902	CONTROL PANEL ASSEMBLY	S/C 36 W/39955, S/C 35 & BLW
6-	77431903	CONTROL PANEL ASSEMBLY	S/C 36 W/39955, S/C 37 & ABV
1	77544728	PANEL, CONTROL	
2	94277503	BASE, MOUNTING	
3	94277400	STRAP, CABLE TIE	
4	94380402	LAMP, INCANDESCENT	
5	94380078	SWITCH, P.B. PANEL	
6	94380838	LENS, YELLOW, PROTECT	
7	94380202	INDICATOR, ILLUMINATE PANEL	
8	94380839	LENS, WHITE, OFF-LINE	
9	94380076	SWITCH, P.B. PANEL	
10	94380840	LENS, RED, CHECK	
11	94380841	LENS, READY	
12	94380842	LENS, START/STOP	
13	94208501	LABEL	
14	10125103	NUT, HEX, MACHINE, SCREW, 4-40	
15	10126400	WASHERS, EXTERNAL TOOTH, LOCK, 4	
16	73228700	BRACKET, SWITCH MOUNTING	
17	93984000	SWITCH, MINIATURE	
18	92834116	SCREW, ROUND HEAD, MACHINE, 4-40 x 3/4	
19	10127101	SCREW, PAN HEAD, MACHINE, 4-40 x 3/16	
20	10125108	NUT, HEX, 10-32	
21	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
22	10125607	WASHER, PLAIN, 10	
23	76398500	ROLLER, DETENT	
24	73228300	SPRING, DETENT	
25	75212700	SOCKET, LOGIC	
	76465202	W8 HARNESS ASSEMBLY	TAB 02
	76465203	W8 HARNESS ASSEMBLY	TAB 03

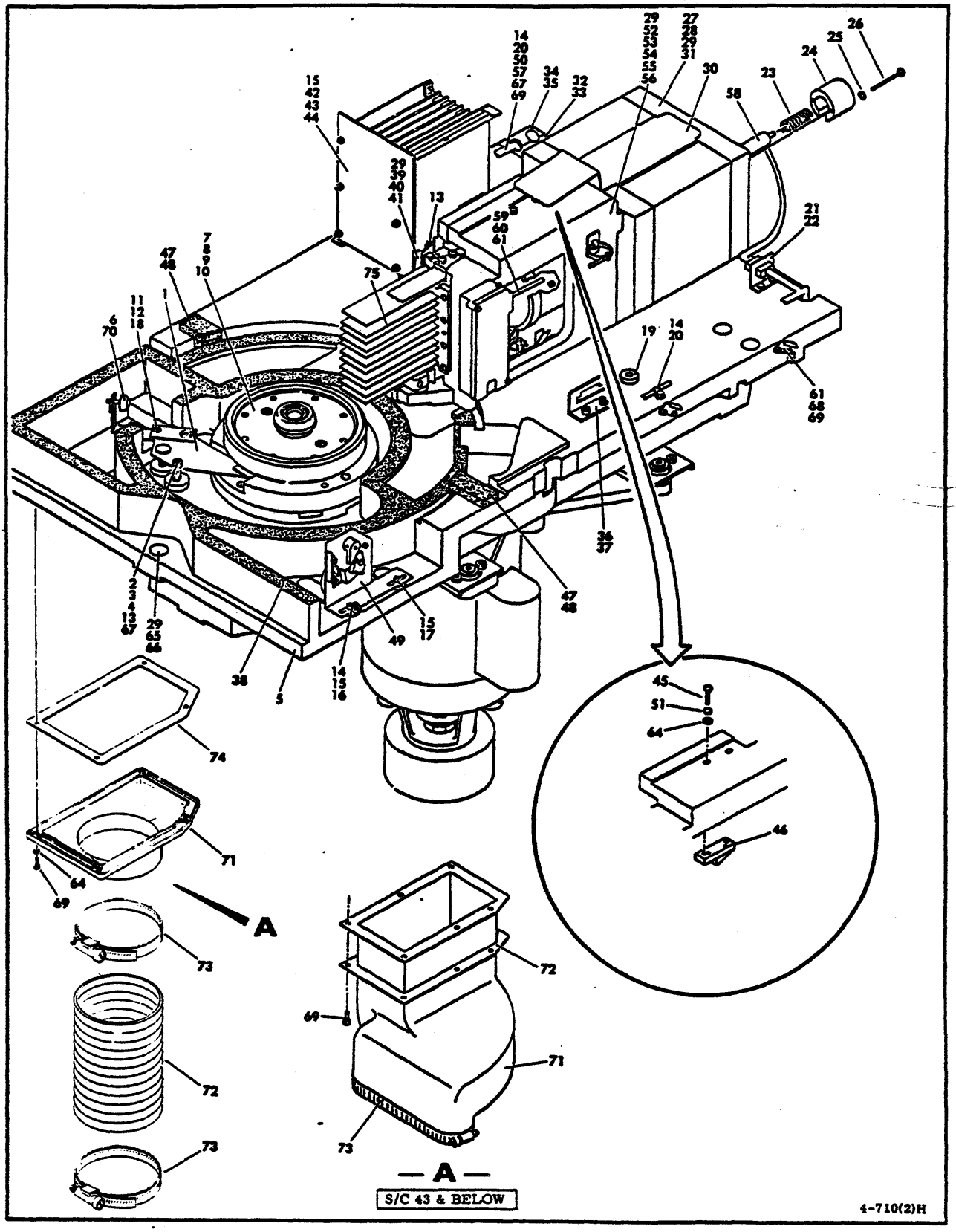


FIGURE 7. MAIN DECK ASSEMBLY (SHEET 1 OF 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
7-		MAIN DECK ASSEMBLY (SHEET 1 OF 2)	
1	76405000	PLATE, BRAKE	
2	93707005	SCREW, MACHINE, HEX SOCKET, 1/4 x 1	S/C 14 & ABOVE. NOTE 1
3	94205793	SPRING, COMPRESSION	
4	94347111	WASHER, SHOULDER	
5	76038300	DECK	
6	75006600	BUTTON, BRAKE	
7	73586003	SPINDLE AND LOCKSHAFT ASSEMBLY	
	76538500	LOCKSHAFT SPINDLE	
	92033301	RING, RETAINING	
8	10126533	SCREW, MACHINE, PLAIN, HEX HEAD, 3/8-16 x 1-3/4	
9	10125808	WASHER, LOCK, SPRING, 3/8	
10	10125610	WASHER, FLAT, 3/8	
11	93073250	SCREW, SET, SOCKET HEAD, 6-32 x 1/2	
12	94001104	TAPE, FOAM	
13	73485304	COMPONENT ASSEMBLY, 3ZQN	
14	94277406	STRAP, CABLE TIE	
15	10125607	WASHER, FLAT, 10	
16	10126245	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 10-32 x 5/8	
17	10126244	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 10-32 x 1/2	
18	47181300	BRACKET, BRAKE ADJUSTMENT	S/C 14 & ABOVE. NOTE 1
19	72837700	BUSHING, INSULATOR	
20	93592202	SCREW, MACHINE, PLAIN, HEX HEAD, STP, 8-32 x 1/2	
21	72823900	BRACKET, CONNECTOR, 3 PIN	
22	93592196	SCREW, MACHINE, PLAIN, HEX HEAD, STP, 8-32 x 1/4	
23	94206431	SPRING, COMPRESSION	
24	70726001	CAP, END, TRANSDUCER	
25	10126104	WASHER, LOCK, INTERNAL TOOTH, 8	
26	10127353	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 1-1/4	
27	76472701	MAGNET ASSEMBLY	
28	10126262	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 2-20 x 1/4	
29	10125608	WASHER, FLAT, 1/4	
30	46484000	COVER, MAGNET	
31	95027403	TAPE, FOAM	
32	93532207	PIN, ROLL	
33	72826001	BLOCK, CLAMP, HARNESS, RIGHT	
34	72825900	BLOCK, CLAMP, HARNESS, LEFT	
35	93592160	SCREW, SELF-TAPPING, 6-32 x 5/16	
36	10127142	SCREW, PHILLIPS, 10-32 x 3/8	
37	72823902	BRACKET, CONNECTOR, 3 PIN	
38	94001102	TAPE, FOAM, 1/8 x 1/2	S/C 13 W/ 35856C & ABOVE
39	10126253	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 1/4-20 x 3/8	
40	93530081	PIN, ROLL	
41	47278500	HEAD CLAMP ASSEMBLY	
	73632100	BRACKET, MOUNTING, HEAD CLAMP	
	73566400	CLAMP, CABLE, HEAD	
	10125801	WASHER, SPRING LOCK, 4	
	10126213	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 4-40 x 3/8	
42	10127142	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 3/8	

NOTE:

1. S/C 13 & BELOW, ORDER PARKING BRAKE BRACKET KIT #95046400.

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
7-		MAIN DECK ASSEMBLY (SHEET 1 OF 2 CONTD)	
43	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
44		R/W PIN AND GUIDE ASSEMBLY (SEE FIGURE 10)	
45	10127113	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-22 x 3/8	
46	47280100	SWITCH ASSEMBLY	
	73489400	BRACKET, MOUNTING, SWITCH	
	93786005	SWITCH, MINI	
	10127106	SCREW, MACHINE, PAN HEAD, 4-40	
	10125603	WASHERS, PLAIN, 4	
	10125801	WASHERS, SPRING LOCK, 4	
47	94001126	TAPE, FOAM, GRAY BLACK, 3/8 x 1/2	
48	94001149	TAPE, FOAM, GRAY BLACK, 1 x 1	
49	76043100	TIMING MOTOR ASSEMBLY	BR3C9 MOD A,B; BR3E4/5 MOD A; S/C 32 & BLW ONLY
49	76043101	TIMING MOTOR ASSEMBLY	BR3C9 MOD C,D; BR3E4/5 MOD B; S/C 32 & BLW ONLY
	73488504	BRUSH MOTOR ASSEMBLY	BR3C9 MOD A,B; BR3E4/5 MOD A
	73488505	BRUSH MOTOR ASSEMBLY	BR3C9 MOD C,D; BR3E4/5 MOD B
	36159808	SWITCH, PIVOT LEVER, INTEGRAL	
50	93592200	SCREW, HEX HEAD, 8-32 x 3/8	
51	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	
52		ACTUATOR ASSEMBLY (SEE FIGURE 11)	
53	94047033	WASHER, SPECIAL	
54	10126256	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 1/4-20 x 3/4	
55	10125806	WASHER, LOCK, INTERNAL TOOTH, 1/4	
56	10126260	SCREW, MACHINE, HEX SOCKET, CAP HEAD, 5/16-18 x 5/8	
57	77382900	DECK HARNESS ASSEMBLY	
58	73618900	TRANSDUCER AND CONNECTOR ASSEMBLY	
	76501000	TRANSDUCER, ROD ASSEMBLY	
59	70729304	ROD, EXTENSION	
60	72835800	STOP, SHIM	
61	94047048	WASHER, SPECIAL	
62		NOT USED	
63		NOT USED	
64	10125605	WASHER, FLAT, 6	
65	10126505	SCREW, MACHINE, HEX HEAD, 1/4-20 x 1-1/4	
66	10125806	WASHER, LOCK SPRING, 1/4	
67	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
68	94356902	CATCH, SPRING	
69	93660045	SCREW, PHILLIPS, 6-32 x 1/2	
70	10125105	NUT, HEX, MACHINE, 6-32	
71	47266100	BOOT, AIR INLET	S/C 43 & BELOW
71	83640800	ADAPTER, HOSE	S/C 44 & ABOVE
72	75023500	PLATE, BOOT SUPPORT	S/C 43 & BELOW
72	94311604	HOSE, FLEXIBLE	S/C 44 & ABOVE
73	94275221	CLAMP, HOSE	S/C 43 & BELOW
73	94275216	CLAMP, HOSE	S/C 44 & ABOVE
74	76579106	GASKET, SEAL	S/C 44 & ABOVE
75	75211300	HEAD ARM COMPLEMENT (IN-LINE)	
	70590600	HEAD ARM ASSEMBLY	HEAD NOS: 2,3,6,7,9,13,14, 17,18
	70590601	HEAD ARM ASSEMBLY	HEAD NOS: 0,1,4,5,8,11,12, 15,16
	70590602	HEAD ARM ASSEMBLY	SERVO HEAD
	70590603	HEAD ARM ASSEMBLY	HEAD NO: 10
	76466200	PLATE, CLAMP, CABLE	

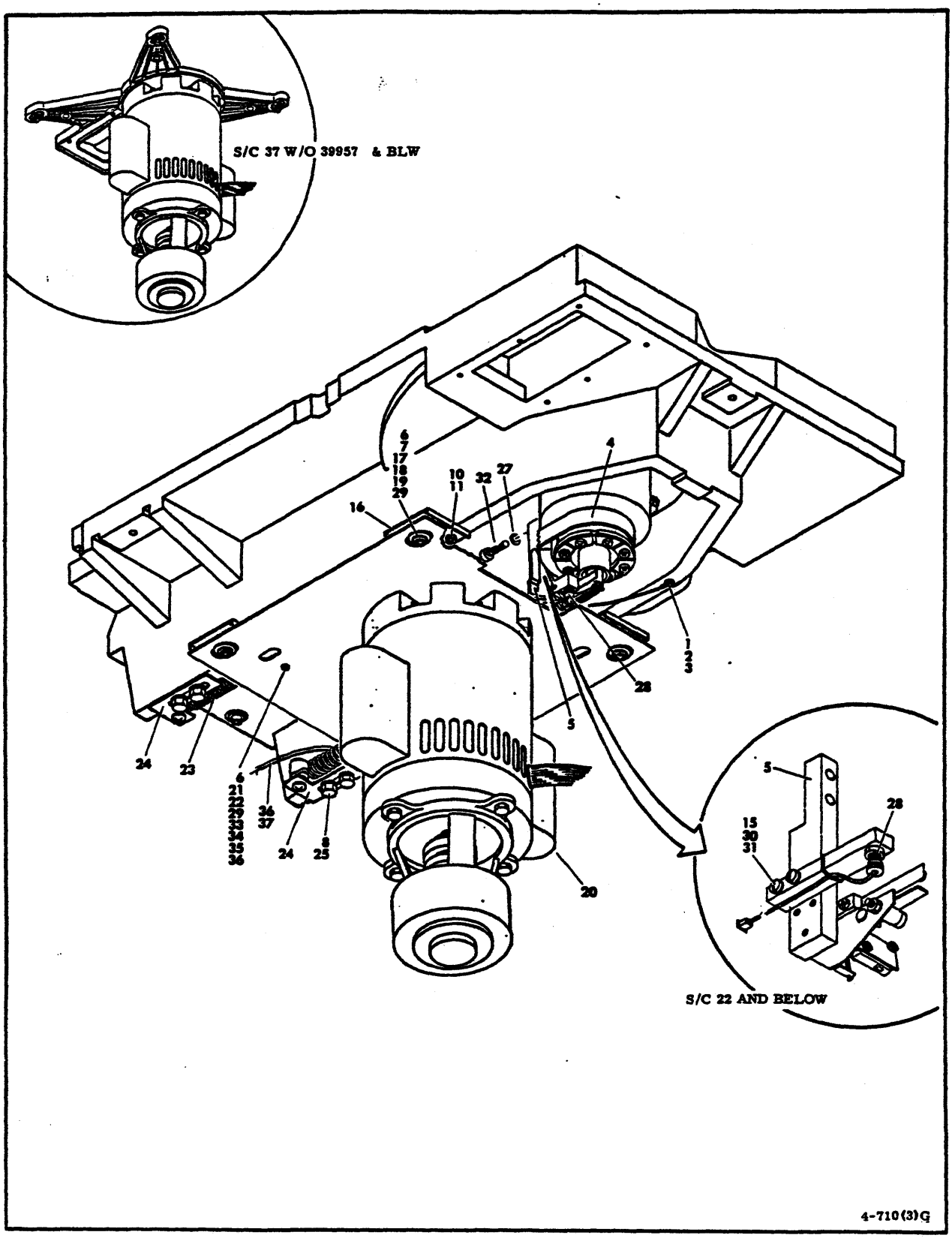


FIGURE 7. MAIN DECK ASSEMBLY (SHEET 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
7-		MAIN DECK ASSEMBLY (SHEET 2)	
1	94281419	CABLE, GROUND	
2	93592200	SCREW, HEX HEAD, PLAIN, TPG, 8-32 x 3/8	
3	10126104	WASHER, LOCK, INTERNAL TOOTH, 8	
4	92314087	BELT, DRIVE, FLAT	BR3C9 MOD A,B BR3E4/5 MOD A
4	92314093	BELT, DRIVE, FLAT	BR3C9 MOD C,D BR3E4/5 MOD B
5		PACK SENSOR ASSEMBLY (SEE FIGURE 12)	
6	10126403	WASHER, LOCK EXTERNAL TOOTH, 10	
7	77448001	SPACER, MOTOR MOUNT	S/C 37 W/39957 & ABV ONLY
8	10125608	WASHER, FLAT, 1/4	
9		NOT USED	
10	10125805	WASHER, LOCK, SPRING, 10	
11	10127380	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 1/2	
12		NOT USED	
13		NOT USED	
14		NOT USED	
15	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	S/C 22 & BELOW
16	47276900	SHOCK MOUNT ASSEMBLY	
	10127348	SCREW, MACHINE, PAN HEAD, SLOTTED, 8-32 x 1/2	
	10125106	NUT, HEXAGON, 8-32	
	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
	94243003	MOUNT, SHOCK	
	76376200	BRACKET, SHOCK MOUNT	
17	73671300	BUSHING, SLIDE	S/C 37 W/O 39957 & BLW
17	70738305	INSULATOR, MOTOR MOUNTING	S/C 37 W/39957 & ABV
18	10125066	SCREW, MACHINE, HEX HEAD, 10-32 x 1	S/C 37 W/O 39957 & BLW ONLY
19	75174300	WASHER, BACKING	S/C 37 W/O 39957 & BLW ONLY
20		DRIVE MOTOR AND BRAKE ASSEMBLY (SEE FIGURE 9)	
21	72806501	SPRING, STANDOFF	S/C 37 W/O 39957 & BLW
21	72806500	SPRING, STANDOFF	S/C 37 W/O 39957 & ABV
22	10127142	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 3/8	
23	77530000	SPRING, EXTENSION	
24	47277200	SPRING BRACKET ASSEMBLY, LEFT	
24	47277201	SPRING BRACKET ASSEMBLY, RIGHT	
	75093400	BRACKET, MOUNTING, SPRING	
	92071004	NUT, HEXAGON, 1/4-20	
	72806502	SPRING, STANDOFF	
	10127158	SCREW, MACHINE, PAN HEAD, PHILLIPS, 1/4-20 x 1/2	
25	10126500	SCREW, MACHINE, HEX HEAD, PLAIN, 1/4-20 x 1/2	
26		NOT USED	
27	10125806	WASHER, LOCK, SPRING, 1/4	
28	76395500	SPEED SENSOR ASSEMBLY	
29	75174200	WASHER, SLIDE	
30	10125606	WASHER, PLAIN, 8	S/C 22 & BELOW ONLY
31	10126229	SCREW, HEXAGON, SOCKET HEAD, CAP, 8-32 x 7/8	S/C 22 & BELOW ONLY
32	10126258	SCREW, MACHINE, SOCKET HEAD, 1/4-20 x 1	S/C 22 & BELOW ONLY
33	10125607	WASHER, FLAT, 10	
34	10127386	SCREW, MACHINE, PAN HEAD, 10-32 x 1-1/2	S/C 37 W/O 39957 & BLW
34	10125067	SCREW, MACHINE, HEXAGON, 10-32 x 1-1/4	S/C 37 W/39957 & ABV
35	10125108	NUT, HEX, 10-32	
36	93592198	SCREW, TPG, HEX, 8-32 x 5/16	
37	94369513	CABLE, GROUND	
38		NOT USED	
	94224674	LABEL, INFORMATION	

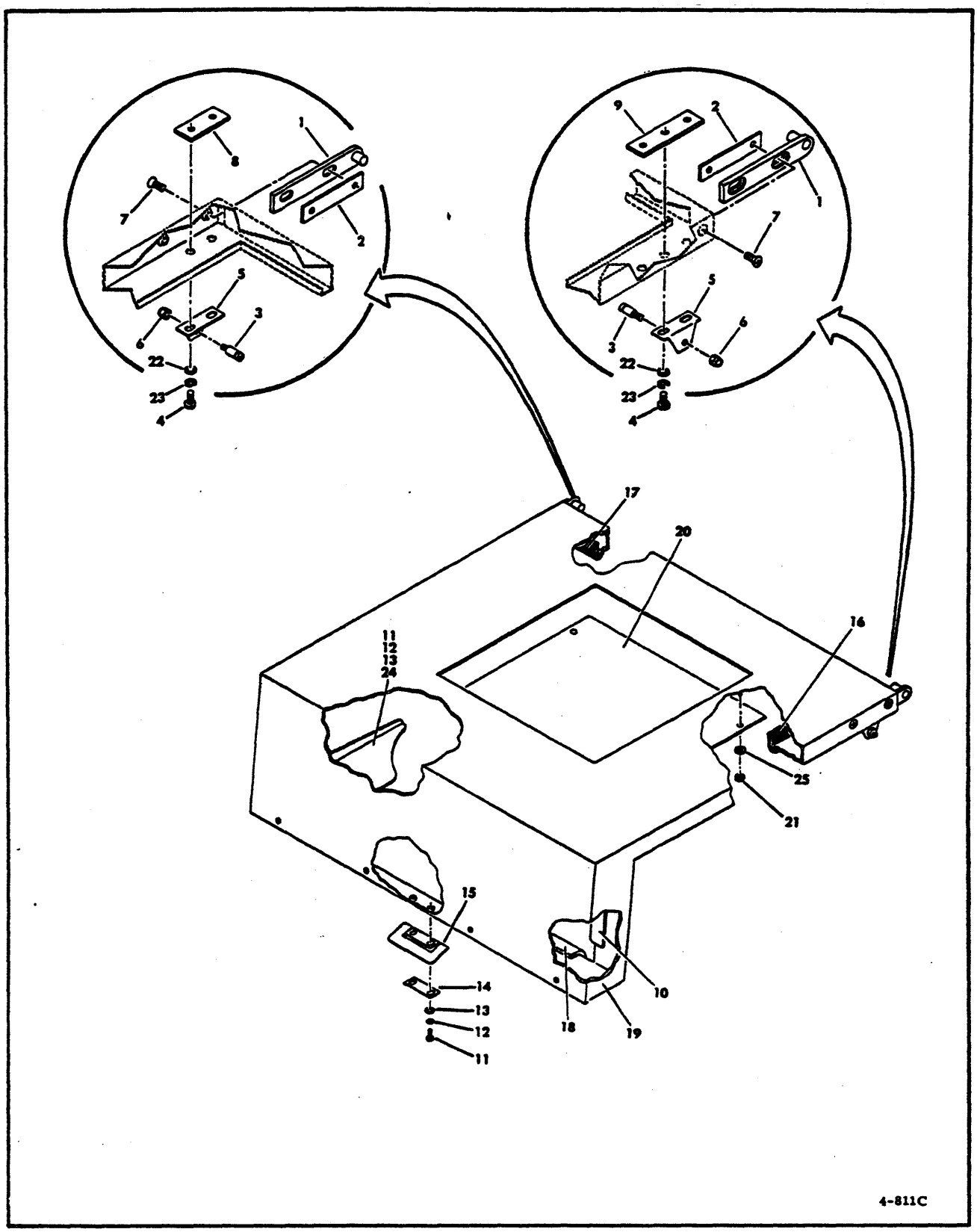


FIGURE 8. PACK ACCESS COVER ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
8-	77384408	PACK ACCESS COVER ASSEMBLY	
1	76536000	HINGE, PACK COVER	
2	75030100	PLATE, NUT, LOCKING	
3	73229004	STUD	
4	10127143	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 1/2	
5	76400200	BRACKET, GAS SPRING	
6	92071005	NUT, SELF LOCKING	
7	10126023	SCREW, MACHINE, HEX HEAD, SOCKET, 10-32 x 1/2	
8	75023200	PLATE, NUT, PACK ACCESS	
9	75052300	PLATE, NUT, PACK ACCESS	
10	82386401	GASKET, EXTRUSION	
11	10127113	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 3/8	
12	10126401	WASLER, LOCK, EXTERNAL TOOTH, 6	
13	10125605	WASHER, FLAT, 6	
14	46948200	PLATE, LATCH	
15	77541700	LATCH ASSEMBLY	
16	75030700	GASKET, EXTRUSION	
17	82386400	GASKET, EXTRUSION	
18	82386403	GASKET, EXTRUSION	
19	76472328	COVER, PACK ACCESS	
20	47182100	GLASS, WINDOW, CLEAR	
21	94217828	NUT, HEX, 8-32	
22	93210009	WASHER, FLAT, 10	
23	10125805	WASHER, SPRING LOCK, 10	
24	75215700	DEFLECTOR, AIR PACK	
25	10125606	WASHER, PLAIN, 8	
26	82386402	GASKET, EXTRUSION	

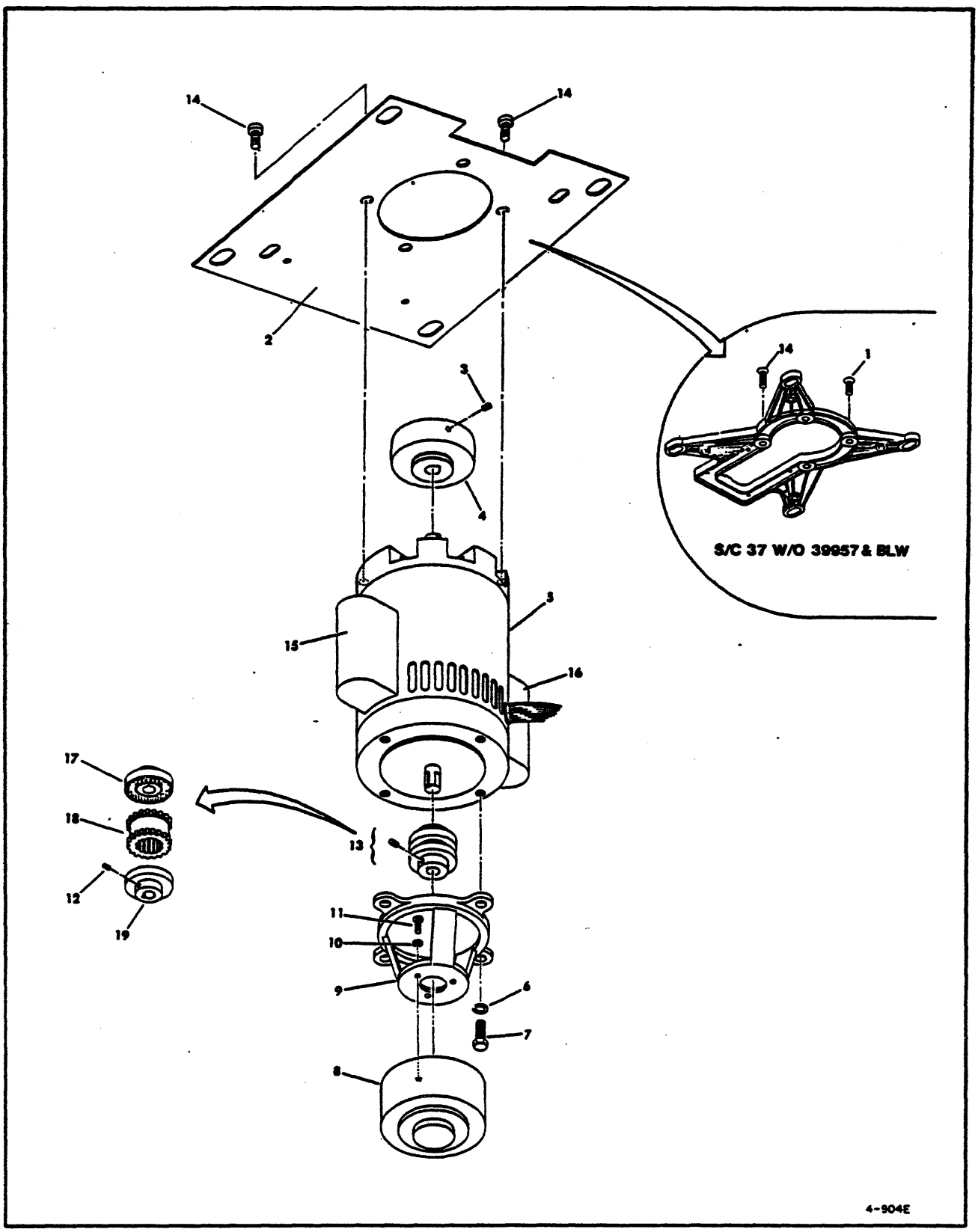


FIGURE 9. DRIVE MOTOR AND BRAKE ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
9-	77431600	DRIVE MOTOR & BRAKE ASSEMBLY, 60Hz	S/C 37 W/O 39957 & BLW
9-	77431602	DRIVE MOTOR & BRAKE ASSEMBLY, 60HZ	S/C 37 W/O 39957, S/C 39 W/O 47898
9-	77431604	DRIVE MOTOR & BRAKE ASSEMBLY, 60HZ	S/C 39 W/47898 & ABV
9-	77431601	DRIVE MOTOR & BRAKE ASSEMBLY, 50HZ	S/C 37 W/O 39957 & BLW
9-	77431603	DRIVE MOTOR & BRAKE ASSEMBLY, 50HZ	S/C 37 W/O 39957, S/C 39 W/O 47898
9-	77431605	DRIVE MOTOR & BRAKE ASSEMBLY, 50HZ	S/C 39 W/47898 & ABV
1	10126502	SCREW, HEXAGON SOCKET, 3/8 - 16 x 1	S/C 37 W/O 39957 & BLW ONLY
2	76404500	BRACKET, MOTOR MOUNTING	S/C 37 W/O 39957 & BLW
2	47424801	PLATE, MOTOR MOUNTING	S/C 37 W/39957 & ABV
3	94363660	SCREW, SET-SKIRTED HEAD, 1/4 - 20 x 3/8	
4	72806905	PULLEY, DRIVE MOTOR, 60HZ	S/C 39 W/O 47898 & BLW
4	72806907	PULLEY, DRIVE MOTOR, 60HZ	S/C 39 W/47898 & ABV
4	72806906	PULLEY, DRIVE MOTOR, 50HZ	S/C 39 W/O 47898 & BLW
4	72806908	PULLEY, DRIVE MOTOR, 50HZ	S/C 39 W/47898 & ABV
5	77431504	DRIVE MOTOR ASSEMBLY	BR3C9 MOD A,B BR3E4/5 MOD A
5	77431505	DRIVE MOTOR ASSEMBLY	BR3C9 MOD C,D BR3E4/5 MOD B
	77430701	MOTOR, DOUBLE END	BR3C9 MOD A,B BR3E4/5 MOD A
	77430801	MOTOR, DOUBLE END	BR3C9 MOD C,D BR3E4/5 MOD B
	94307400	KEY (MOTOR PULLEY END)	
	94307404	KEY (MOTOR BRAKE END)	
	93942006	CONTACT PIN	
6	10125808	WASHER, SPRING LOCK, 3/8	
7	10126530	SCREW, PLAIN, HEX HEAD, 3/8-16 x 1	
8	75094800	BRAKE ASSEMBLY	
	94259401	BRAKE, HYSTERESIS	
	93948004	CONNECTOR, PIN HOUSING	
	93942009	CONTACT, PIN	
	94277409	STRAP, CABLE TIE	
9	77420000	MOUNT, MOTOR BRAKE	
10	10125805	WASHER, SPRING LOCK, 10	
11	10127144	SCREW, PAN HEAD, MACHINE, 10-32 x 5/8	
12	94363646	SCREW, SET-SKIRTED HEAD, 10-24 x 3/8	
13	77424102	COUPLING, FLEXIBLE	
14	10126053	SCREW, HEXAGON SOCKET, 3/8-16 x 1-1/4	S/C 37 W/O 39957 & BLW
14	10126528	SCREW, HEXAGON HEAD, 3/8-16 x 3/4	S/C 37 W/ 39957 & ABV
15	94365802	CAPACITOR, MOTOR RUN	
16	75039701	CAPACITOR, MOTOR START	
17	77424101	FLANGE, COUPLING	
18	77424103	SLEEVE, RUBBER	
19	77424102	FLANGE, COUPLING	

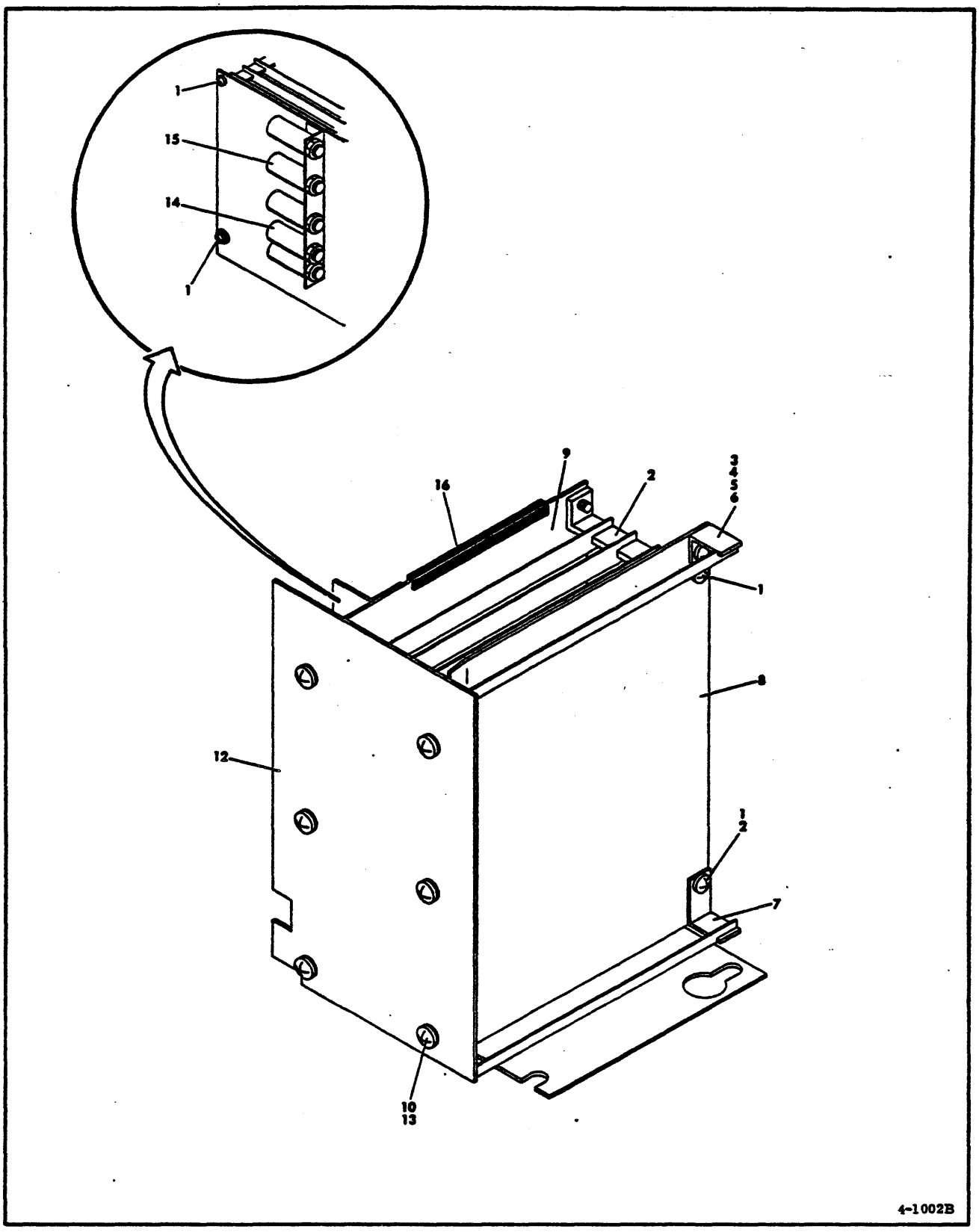


FIGURE 10. R/W PIN AND GUIDE ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
10-	76028303	READ/WRITE PIN AND GUIDE ASSEMBLY	S/C 29 & BELOW
10-	76028307	READ/WRITE PIN AND GUIDE ASSEMBLY	S/C 30 & ABOVE
1	17901508	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/4	
2	72807403	GUIDE, CARD	
3	10127112	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 5/16	
4	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
5	10125105	NUT, HEXAGON, 6-32	
6	72807703	RAIL, GUIDE	
7	72807702	RAIL, GUIDE	
8	76028100	BRACKET, CARD GUIDE, LEFT	
9	76028200	BRACKET, CARD GUIDE, RIGHT	
10	17901516	SCREW, SELF TAPPING, 8-32 x 3/8	
11		NOT USED	
12	76509600	PANEL, WIRE WRAP ASSEMBLY	S/C 29 & BELOW
12	76509601	PANEL, WIRE WRAP ASSEMBLY	S/C 30 & ABOVE
13	10126104	WASHER, LOCK, INTERNAL TOOTH, 8	
14	94348203	CAPACITOR, FEED-THRU	
15	94348300	FILTER, R.F.	
16	94060003	CHANNEL, RUBBER	

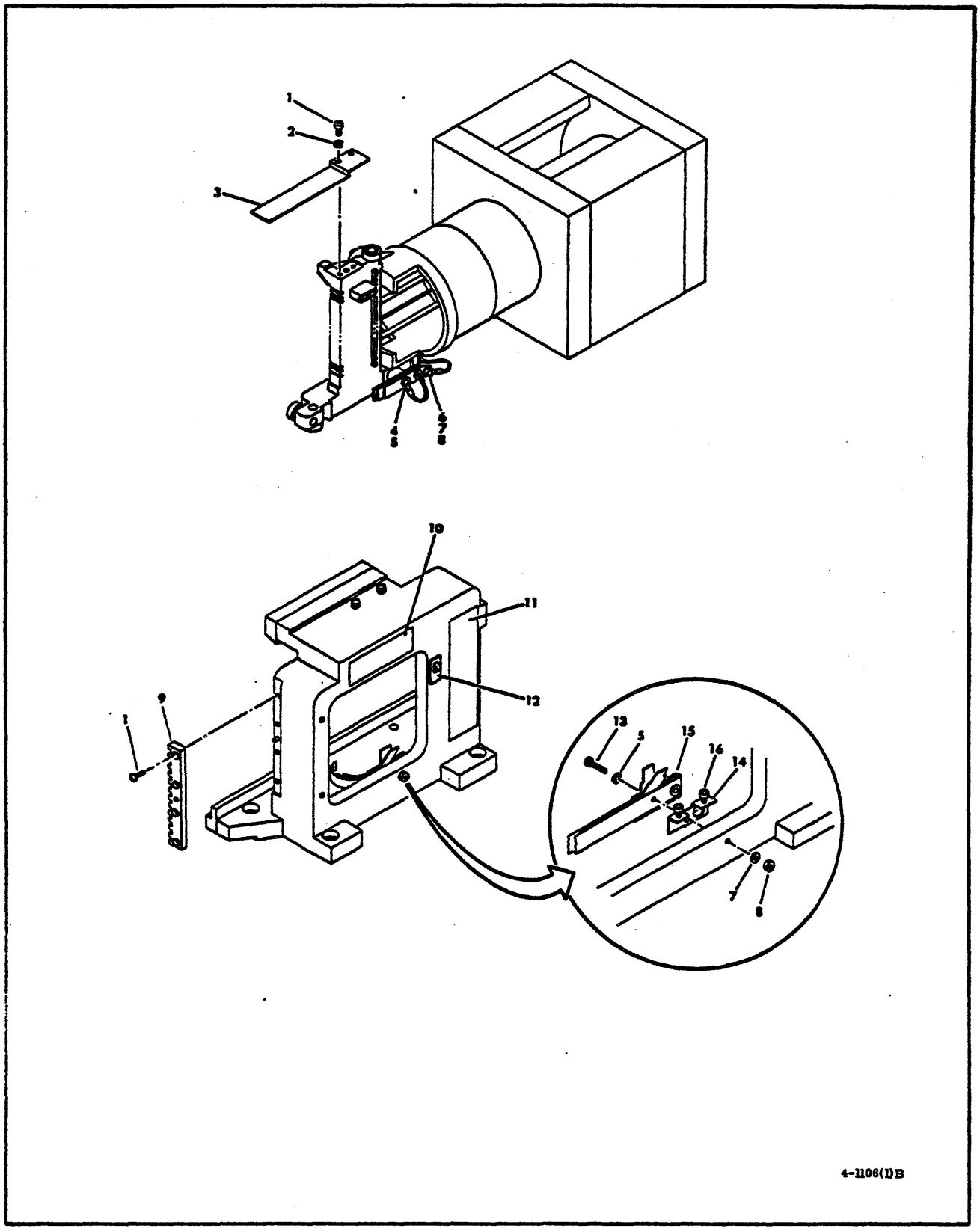


FIGURE 11. ACTUATOR ASSEMBLY (SHEET 1 OF 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
11-	76034200	ACTUATOR ASSEMBLY (SHEET 1 OF 2)	SEE NOTE BELOW
1	10126218	SCREW, MACHINE, CAP HEAD, HEX, SOCKET, 6-32 x 3/8	
2	10125803	WASHER, LOCK, SPRING, 6	
3	73240901	SHIELD, HEAD	
4	94350504	SCREW, INSULATED	
5	93564032	WASHER, NYLON	
6	10127332	SCREW, MACHINE, PAN HEAD, SLOTTED, 6-32 x 1/4	
7	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	
8	10125105	NUT, HEX, 6-32	
9	75212300	CAM, HEAD	
10	94224671	LABEL, INFORMATION, HEAD CLEANING	
11	94224672	LABEL, INFORMATION, HEAD LOCATION	
12	94277503	BASE, MOUNTING	
13	94350503	SCREW, INSULATED	
14	76046400	BRACKET, COIL LEADS	
15	77444600	CONDUCTOR, FLEXIBLE	
16	10126224	SCREW,MACHINE,CAP HEAD,HEX,SOCKET,6-32 x 1/4	

NOTE

ONLY THOSE PARTS LISTED ARE FIELD REPLACEABLE. IF IT BECOMES NECESSARY TO REPLACE PARTS OTHER THAN THOSE LISTED, REPLACEMENT OF THE ENTIRE ACTUATOR ASSEMBLY IS REQUIRED. WHEN ORDERING AN ACTUATOR ASSEMBLY FOR REPLACEMENT, ALSO ORDER ONE SHIM ASSORTMENT (P/N 75039400) FOR EACH ACTUATOR ASSEMBLY BEING REPLACED.

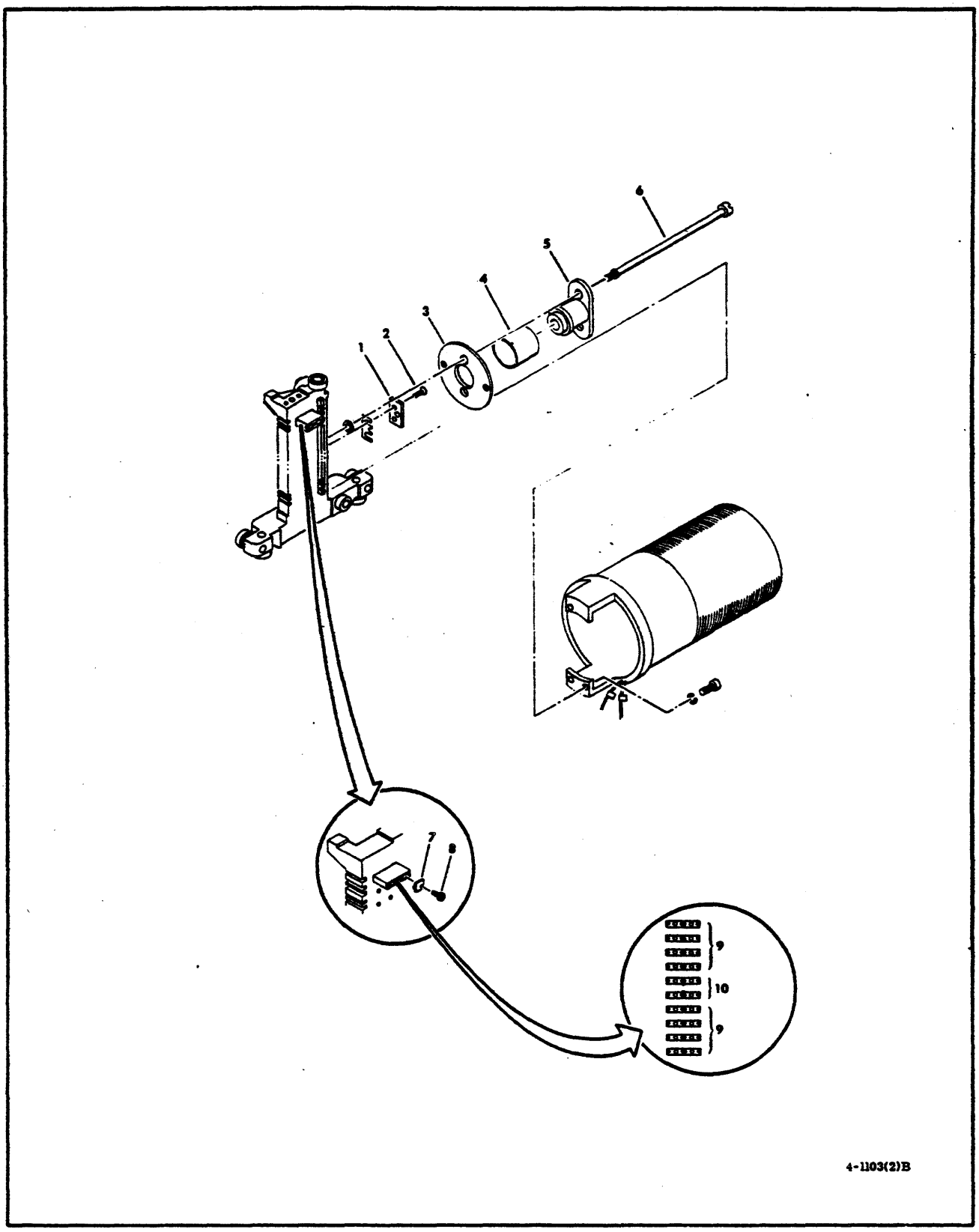


FIGURE 11. ACTUATOR ASSEMBLY (SHEET 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
11-		ACTUATOR ASSEMBLY (SHEET 2)	
1	72825100	SHIM, STOP, CARRIAGE	
2	10126006	SCREW, MACHINE, FLATHEAD, HEX SOCKET, 6-32 x 3/8	
3	70725900	PLATE, STOP	
4	72815100	SPACER, STOP, CARRIAGE	
5	72835400	STOP, CARRIAGE	
6	70728903	ROD, STOP	
7	73228200	PLATE, ARM CLAMP	
8	92817096	SCREW, CAP HEAD, HEX SOCKET, 4-40 x 1/4	
9	73584402	BASE, ARM CLAMP	SEE NOTE BELOW
10	73584403	BASE, ARM CLAMP	SEE NOTE BELOW
		NOTE: REFER TO MAINTENANCE SECTION FOR REMOVAL AND REPLACEMENT OF ARM CLAMP BASE.	

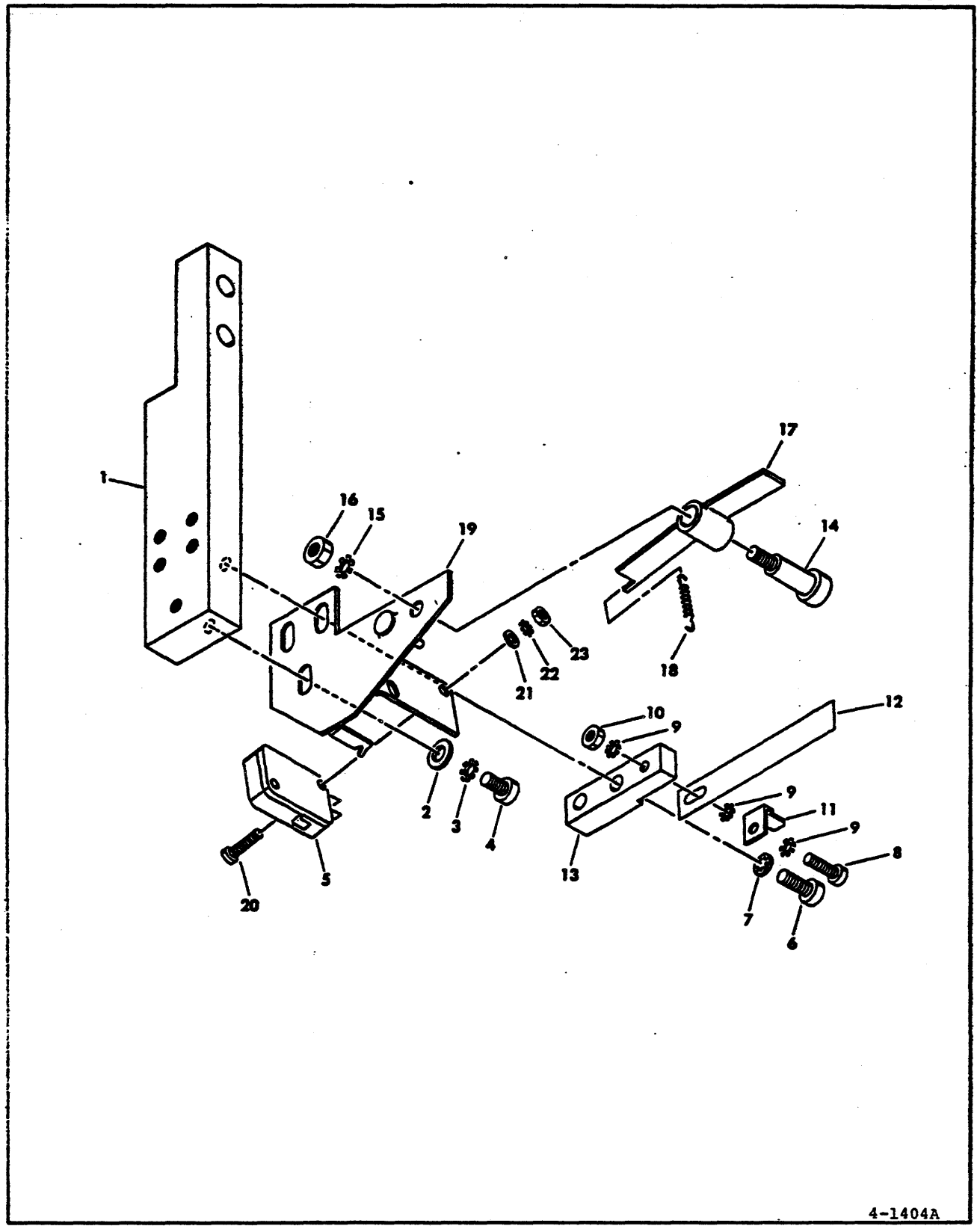
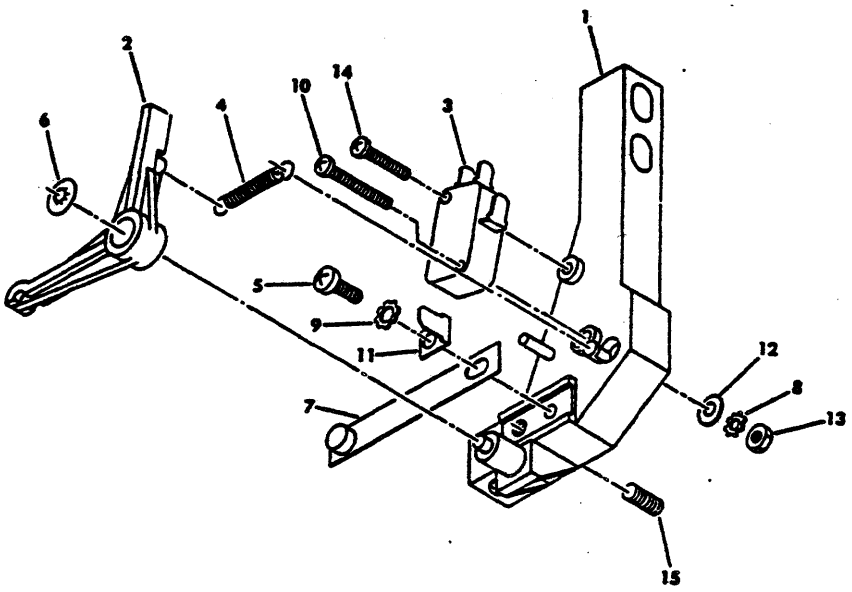


FIGURE 12. PACK SENSOR ASSEMBLY (SHEET 1 OF 2)
S/C 22 AND BELOW

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
12-		PACK SENSOR ASSEMBLY (SHEET 1 OF 2)	THIS PACK SENSOR ASSEMBLY ON UNITS S/C 22 & BELOW. NEW PACK SENSOR ASSEMBLY SUPPLIED WHEN REORDERING
1	73586600	MOUNT-SWITCH	
2	10125606	WASHER, PLAIN, 8	
3	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
4	10127122	SCREW, MACHINE, PAN HEAD, 8-32 x 3/8	
5	93786012	SWITCH, MINI-INTEGRAL ACTUATOR	
6	10127124	SCREW, MACHINE, PAN HEAD, 8-32 x 5/8	
7	10126104	WASHER, LOCK, INTERNAL TOOTH, 8	
8	10127336	SCREW, MACHINE, PAN HEAD, 6-32 x 5/8	
9	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
10	10125105	NUT, MACHINE, HEXAGON, 6-32	
11	94274107	TERMINAL, QUICK CONNECT	
12	40054700	SPRING, STATIC GROUND	
13	73478500	BRACKET, MOUNTING, CONTACT	
14	93707002	SCREW, SOCKET HEAD, 1/4-20 x 1/2	
15	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
16	10125107	NUT, MACHINE, HEXAGON, 10-24	
17	73587200	ARM-ACTUATOR	
18	73225300	SPRING-EXTENSION	
19	73587300	PLATE, MOUNTING	
20	10127106	SCREW, MACHINE, PAN HEAD, 4-40 x 5/8	
21	10125603	WASHER, PLAIN, 4	
22	10126400	WASHER, LOCK, EXTERNAL TOOTH, 4	
23	10125103	NUT, MACHINE, HEXAGON, 4-40	



4-1407C

FIGURE 12. PACK SENSOR ASSEMBLY (SHEET 2)
S/C 23 AND ABOVE

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
12-	73586100	PACK SENSOR ASSEMBLY (SHEET 2)	S/C 23 & ABOVE
1	83282900	BASE, SPINDLE END PACK ON SW	
2	83282800	ACTUATOR, PACK ON SWITCH	
3	93786012	SWITCH, MINI INTEGRAL ACTUATOR	
4	83283900	SPRING, EXTENSION	
5	93590162	SCREW, PAN, PHILLIPS, 6-32 x 3/8	
6	94241401	FASTENER, BOLT RETAINER	
7	40054700	SPRING, STATIC GROUND	
8	10126400	WASHER, LOCK, EXTERNAL TOOTH, 4	
9	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
10	10127108	SCREW, MACHINE, PAN 4-40 x 7/8	
11	94274107	TERMINAL, QUICK CONNECT	
12	10125603	WASHER, PLAIN, 4	
13	10125103	NUT, HEX, MACHINE, 4-40	
14	93590090	SCREW, SELF THREAD, 4-40 x 5/8	
15	93061288	SCREW, SET, SOCKET HEAD, 8-32 x 3-8	

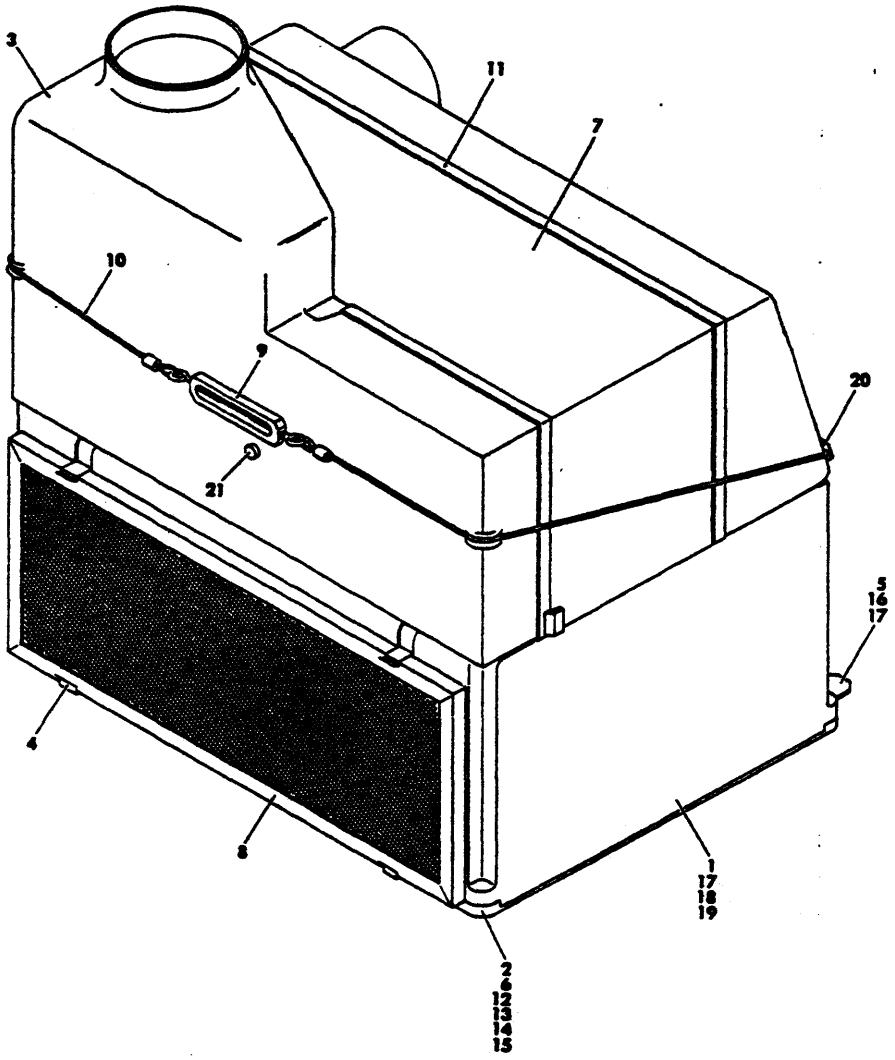


FIGURE 13. AIR SUPPLY ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
13-	76461300	AIR SUPPLY ASSEMBLY	S/C 43 & BELOW
13-	76461301	AIR SUPPLY ASSEMBLY	S/C 44 & ABOVE
1	76380900	PLENUM, BLOWER	S/C 43 & BELOW
1	76380901	PLENUM, BLOWER	S/C 44 & ABOVE
2	76381000	BASE, BLOWER	
3	76381100	PLENUM, OUTPUT, DECK	S/C 43 & BELOW
3	83640900	PLENUM, OUTPUT, DECK	S/C 44 & ABOVE
4	76462400	CLIP, SPRING	
5	76462000	BRACKET, PLENUM	
6	75025200	BLOWER MOTOR ASSEMBLY	
	94357900	BLOWER, CENTRIFUGAL	
	51837253	CONNECTOR, PLUG	
	94320402	CONTACT, PIN, TERMINAL (MALE)	
7	94358001	FILTER, AIR	
8	92002700	FILTER, ALUMINUM	
9	73224400	TURNBUCKLE	
10	94323307	CABLE, WIRE ROPE	
11	94276600	TAPE, FOAM	
12	94359600	MOUNT, SHOCK-BUSHING, RUBBER, STANDOFF	
13	94359601	MOUNT, SHOCK-BUSHING, RUBBER, FLAT	
14	93707026	SCREW, SHOULDER	
15	10125609	WASHER, FLAT, 5/16	
16	92071007	NUT, HEXAGON, STP, 10-24	
17	10125607	WASHER, FLAT, 10	
18	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
19	10127132	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-24 x 1/2	
20	77826900	KEEPER, CABLE	
21	94353207	HOLE, PLUG	

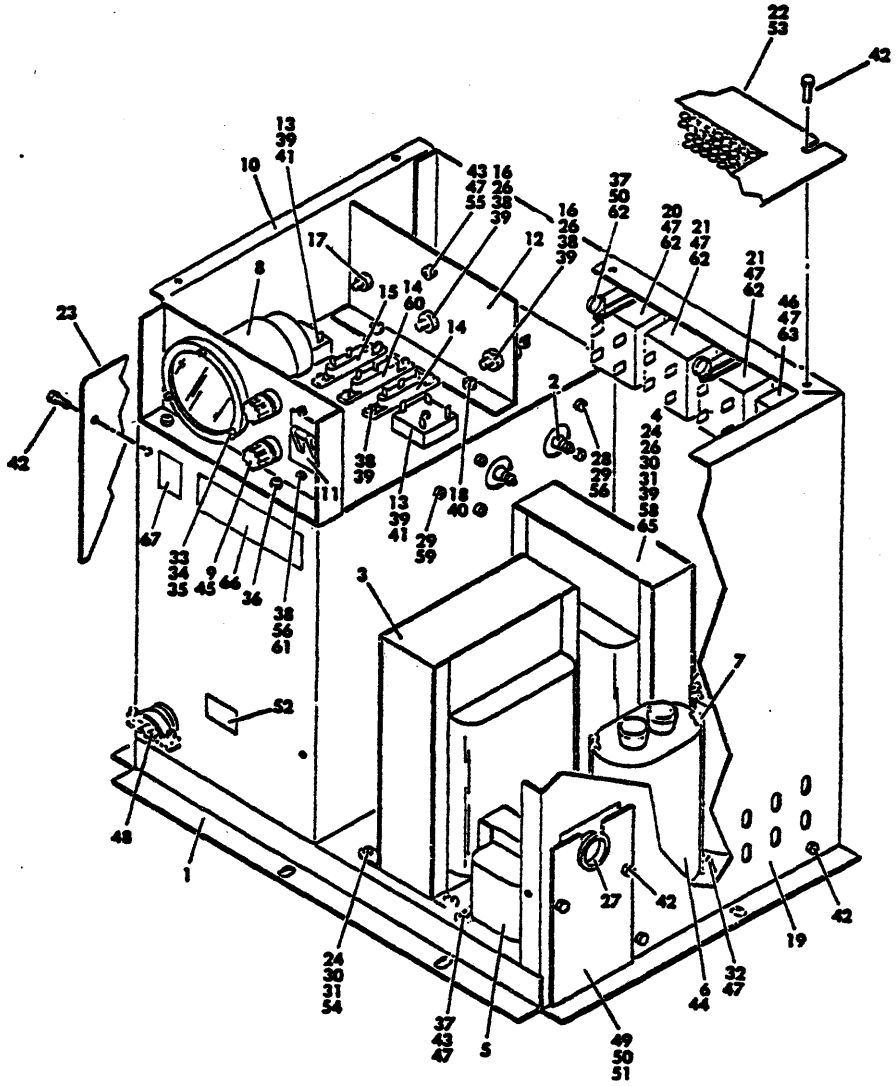


FIGURE 14. POWER SUPPLY ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
14-	773850xx	POWER SUPPLY ASSEMBLY	
	77385200	A.C. HARNESS ASSEMBLY (NOT ILLUSTRATED)	
1	76034500	BASE, POWER SUPPLY	
2	94246002	FILTER, RFI	S/C 29 & BELOW
2	94355401	FILTER, RFI	S/C 30 thru 40
2	94355403	FILTER, RFI	S/C 40 W/47859 & ABV
3	47376400	TRANSFORMER	BR3C9 MOD A,B BR3E4/5 MOD A
3	47376500	TRANSFORMER	BR3C9 MOD C,D BR3E4/5 MOD B
4	47396100	TRANSFORMER	BR3C9 MOD A,B BR3E4/5 MOD A
4	47396200	TRANSFORMER	BR3C9 MOD C,D BR3E4/5 MOD B
5	47317900	TRANSFORMER ASSEMBLY	
6	95599101	CAPACITOR, 660 VAC	
7	95686701	CLAMP, CAPACITOR	
8	94313808	METER, HOUR	BR3C9 MOD A,B BR3E4/5 MOD A
8	94313809	METER, HOUR	BR3C9 MOD C,D BR3E4/5 MOD B
9	94310102	EXTRACTOR, FUSE	
10	75092500	COVER, COMPONENT MOUNTING	
11	94245215	CIRCUIT BREAKER, LONG DELAY	
12	73628200	BRACKET, RECTIFIER	
13	95582001	BLOCK, RECTIFIER	
14	95583504	BLOCK, RECTIFIER	
15	95583505	BLOCK, RECTIFIER	
16	95654205	RECTIFIER, SILICON, 40 AMP	
17	95642602	RECTIFIER, SILICON, 12 AMP	
18	95655200	NUT, PUSH ON	
19	76026500	PANEL, SIDE, POWER SUPPLY	
20	94371301	SWITCH, SOLID STATE, 15 AMPS	
21	94371302	SWITCH, SOLID STATE, 30 AMPS	
22	75026600	COVER, POWER SUPPLY	
23	73632900	COVER, FILTER BOX	
24	10125608	WASHER, FLAT, 1/4	
25		NOT USED	
26	10125105	NUT, HEXAGON, 6-32	
27	94305530	BUSHING, SNAP	
28	10127130	SCREW, MACHINE,PAN HEAD, PHILLIPS, 10-24 x 5/16	
29	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
30	10127155	SCREW, MACHINE, PAN HEAD, PHILLIPS, 1/4-20 x 3/4	
31	10125806	WASHER, LOCK, SPRING, 1/4	
32	10127127	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 1	
33	10127105	SCREW, MACHINE, PAN HEAD, PHILLIPS, 4-40 x 1/2	
34	10126101	WASHER, LOCK, INTERNAL TOOTH, 4	
35	10125103	NUT, HEXAGON, 4-40	
36	17901516	SCREW, MACHINE, PAN HEAD, PHILLIPS, STP, 8-32 x 3/8	
37	10125606	WASHER, FLAT, 8	
38	10127112	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 5/16	
39	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
40	95655530	SCREW, SHEET METAL, 8-18 x 1/2	
41	17901512	SCREW, SELF TPG, 6-32 x 3/4	
42	93592158	SCREW, MACHINE, HEX HEAD, PLAIN, 6-32 x 1/4	
43	10127124	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 5/8	
44	95582501	BOOT, DOUBLE ENTRANCE	
45	93419314	FUSE, SLOW-BLOW, 3/8 AMP, 250 VOLT	
46	94376500	SWITCH, SOLID STATE	
47	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
48	92801001	CLAMP, CABLE	
49	75032200	COVER, CABLE	

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
14-		POWER SUPPLY ASSEMBLY (Contd)	
50	94277406	STRAP, CABLE TIE	
51	17901524	SCREW, MACHINE, PAN HEAD, PHILLIPS, STP, 10-32 x 1/2	
52	94208500	LABEL	
53	93592196	SCREW, TPG, HEX, PNL, 8-32 x 1/4	
54	93602321	NUT, SELF-MOUNTING, 1/4-20	
55	10125106	NUT, HEXAGON, 8-32	
56	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
57		NOT USED	
58	10125605	WASHER, FLAT, 6	
59	10127132	SCREW, MACHINE, PAN HEAD, 10-24 x 1/2	
60	17901509	SCREW, SELF TPG, 6-32 x 3/-	
61	94208301	CAP, TUBE	
62	10127123	SCREW, MACHINE, PAN HEAD, 8-32 x 1/2	
63	10127122	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 3/8	
64		NOT USED	
65	94208303	CAP, TUBE	
66	94391510	LABEL, INFORMATION	
67	92006905	PLATE, WARNING	

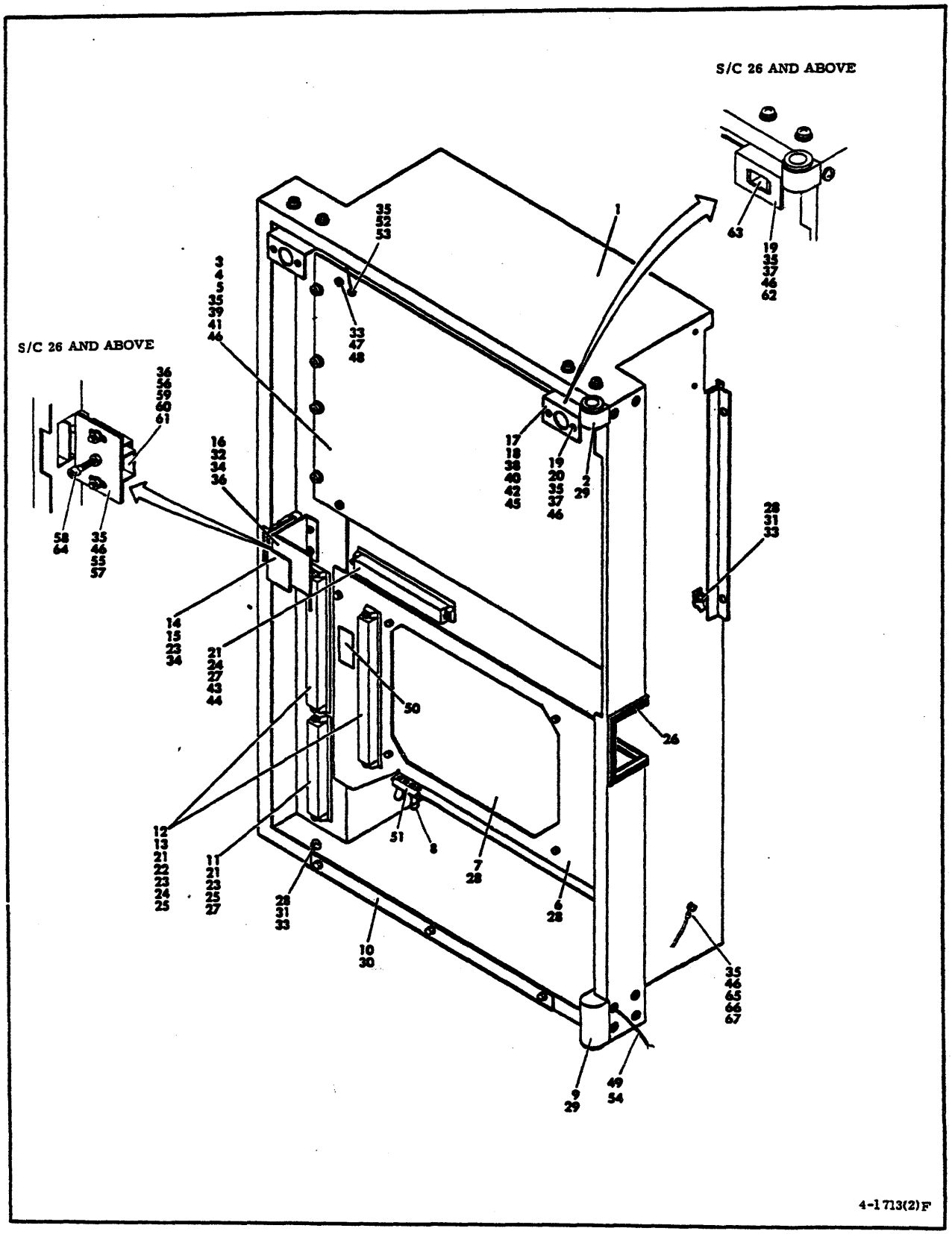


FIGURE 15. LOGIC CHASSIS ASSEMBLY (SHEET 1 OF 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
15-	778117XX	LOGIC CHASSIS ASSEMBLY (SHEET 1 OF 2)	S/C 25 & BELOW
15-	472559XX	LOGIC CHASSIS ASSEMBLY	S/C 26-29
15-	472895XX	LOGIC CHASSIS ASSEMBLY	S/C 30-32
15-	473477XX	LOGIC CHASSIS ASSEMBLY	S/C 33 & ABOVE
1	77383000	FRAME, LOGIC CHASSIS	
2	75024600	HINGE, LOGIC CHASSIS, UPPER	S/C 32 & BELOW
2	82379000	HINGE, LOGIC CHASSIS, UPPER	S/C 33 & ABOVE
3	752147XX	LOGIC WIRE & BOARD ASSEMBLY (WIRE WRAP PANEL)	S/C 17 & BELOW
3	471674XX	LOGIC WIRE & BOARD ASSEMBLY (WIRE WRAP PANEL)	S/C 18 & ABOVE
4	75028901	INSULATOR, BACK PANEL	
5	75028900	INSULATOR, BACK PANEL	
6	76465100	PANEL, D.C. BACK	
7		COMPONENT ASSEMBLY, TYPE 3ZCN (SEE FIGURE 17)	
8	94277404	STRAP, CABLE TIE	
9	75024700	HINGE, LOGIC CHASSIS, LOWER	S/C 32 & BELOW
9	82378900	HINGE, LOGIC CHASSIS, LOWER	S/C 33 & ABOVE
10	75025900	CATCH, BOTTOM	
11	94274440	MARKER STRIP	
12	94272341	BLOCK, TERMINAL, SINGLE SCREW	
13	94274446	MARKER STRIP	
14	75032700	LATCH AND SPRING ASSEMBLY	S/C 25 & BELOW ONLY
	75027800	CATCH, LATCH	
	76411800	SPRING, LATCH, FLAT	
	93994003	RIVET, POP	
15	75027400	BLOCK, PIVOT, LATCH	S/C 25 & BELOW ONLY
16	75027600	PLATE, BACKUP	S/C 25 & BELOW ONLY
17	94355603	FASTENER, QUARTER TURN	S/C 25 & BELOW ONLY
18	94355602	FASTENER, QUARTER TURN	S/C 25 & BELOW ONLY
19	75026100	PLATE, NUT	
20	75026000	BRACKET, FASTENER MOUNTING	S/C 25 & BELOW ONLY
21	94274116	TERMINAL, QUICK CONNECT	
22	94274110	TERMINAL, QUICK CONNECT	
23	94274113	TERMINAL, QUICK CONNECT	
24	93047002	JUMPER, BARRIER STRIP	
25	94272335	BLOCK, TERMINAL, SINGLE SCREW	
26	94237703	TRIM, SAFETY, BLACK	
27	17901517	SCREW, MACHINE, PAN HEAD, PHILLIPS, STP, 8-32 x 1/2	
28	93592196	SCREW, MACHINE, HEX HEAD, STP, 8-32 x 1/4	
29	10125746	SCREW, MACHINE, FLAT HEAD, PHILLIPS, 10-32 x 3/8	S/C 32 & BELOW
29	94375833	SCREW, PAN HEAD, THREAD FORMING, 10-14 x 1/2	S/C 33 & ABOVE

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
15-		LOGIC CHASSIS ASSEMBLY (SHEET 1 of 2) (CONTD)	
30	93592158	SCREW, MACHINE, HEX HEAD, STP, 6-32 x 1/4	
31	94274105	TERMINAL, QUICK CONNECT	
32	10127111	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/4	
33	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
34	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	S/C 25 & BELOW ONLY
35	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
36	10125605	WASHER, FLAT, 6	
37	10127143	SCREW, MACHINE, PANHEAD, PHILLIPS, 10-32 x 1/2	
38	10125903	SCREW, MACHINE, FLATHEAD, PHILLIPS, 4-40 x 3/4	S/C 25 & BELOW ONLY
39	93564002	WASHER, NYLON	
40	10126400	WASHER, LOCK, EXTERNAL TOOTH, 4	S/C 25 & BELOW ONLY
41	10127142	SCREW, MACHINE, PAN HEAD, 10-32 x 3/8	
42	10125103	NUT, HEXAGON, 4-40	S/C 25 & BELOW ONLY
43	94272336	BLOCK, TERMINAL, SINGLE SCREW	
44	94274441	MARKET STRIP	
45	10125603	WASHER, FLAT, 4	S/C 25 & BELOW ONLY
46	10125607	WASHER, FLAT, 10	
47	10127123	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 1/2	
48	10125106	NUT, HEX, 8-32	
49	10126105	WASHER, INTERNAL LOCK, 10	
50	46068600	PLATE, WARNING	
51	94060003	CHANNEL, RUBBER	
52	94369504	CABLE, GROUND	
53	93592234	SCREW, HEX WASHER HEAD, STP, 10-24 x 1/4	
54	94369517	CABLE, GROUND	
55	92008600	LATCH, SLIDE BOLT	S/C 26 & ABOVE ONLY
56	82354200	SPACER, LATCH	S/C 26 & ABOVE ONLY
57	10125107	NUT, HEX, MACHINE 10-24	S/C 26 & ABOVE ONLY
58	94364309	NUT, HEX, METRIC	S/C 26 & ABOVE ONLY
59	10127113	SCREW, MACHINE, PAN HEAD, 6-32 x 3/8	S/C 26 & ABOVE ONLY
60	10125105	NUT, HEX, MACHINE, 6-32	S/C 26 & ABOVE ONLY
61	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	S/C 26 & ABOVE ONLY
62	82354000	BRACKET, FASTENER, MOUNTING	S/C 26 & ABOVE ONLY
63	94303500	RECEPTACLE, CLIP-ON	S/C 26 & ABOVE ONLY
64	10128357	SCREW, CAP, SOCKET HEAD, HEXAGON	
	46491100	PANEL, PERPENDICULAR	
	46490200	RAIL, GUIDE, 1 SECTION	
	46490201	RAIL, GUIDE, 2 SECTION	
	46490202	RAIL, GUIDE, 3 SECTION	
	94309003	CLIP, U	
	17901515	SCREW, MACHINE, PAN HEAD, PHILLIPS, STP, 8-32 x 1/4	
65	10127134	SCREW, PHILLIPS, 10-24 x 3/4	
66	10125108	NUT, HEXAGON, 10-24	
67	94323306	CABLE, GROUND	

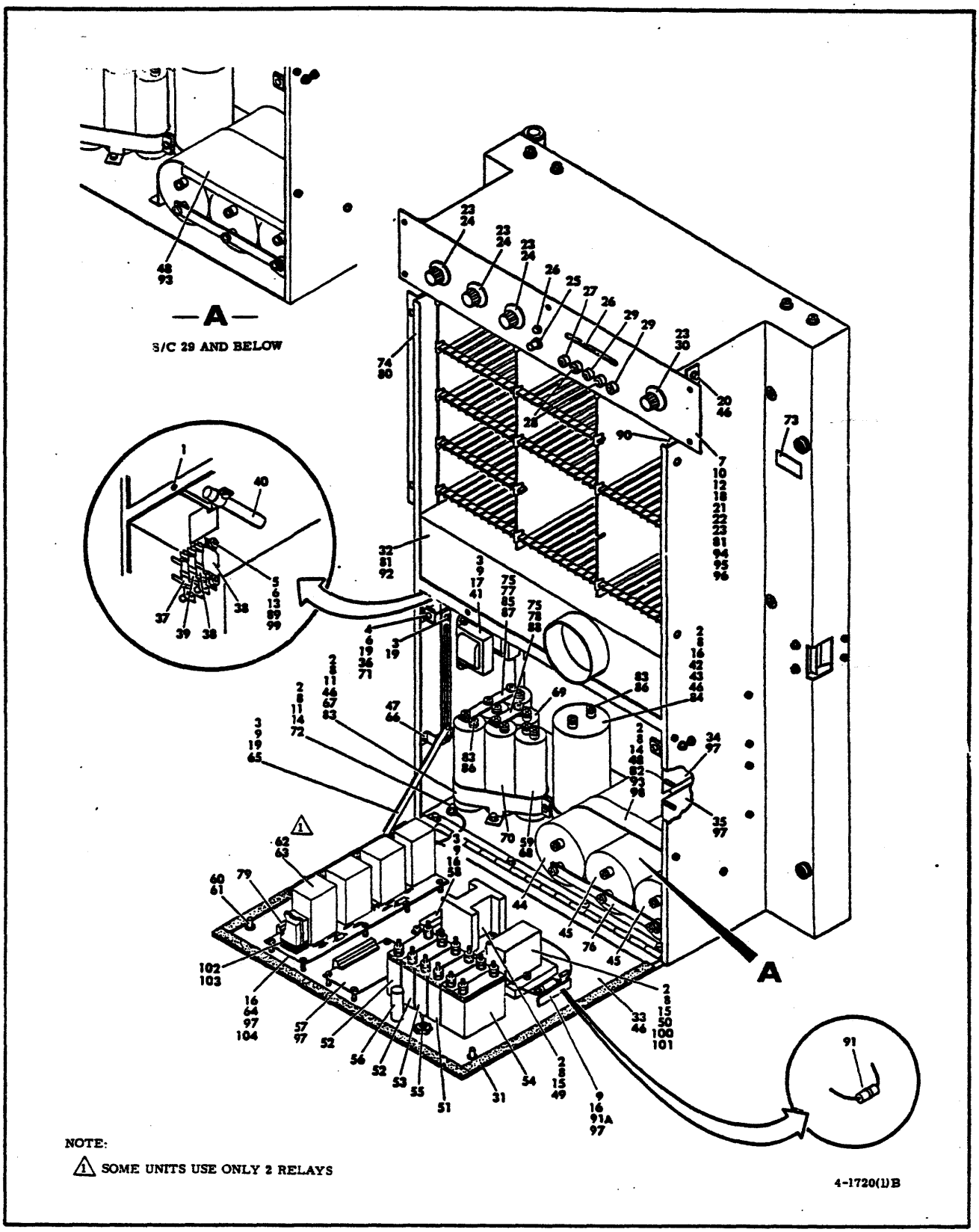


FIGURE 15. LOGIC CHASSIS ASSEMBLY (SHEET 2)

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
15-		LOGIC CHASSIS ASSEMBLY (SHEET 2)	
	95653100	LABEL (HIGH VOLTAGE)	
	34547501	PLATE (WARNING)	
1	10125713	SCREW, MACHINE, FLAT HEAD, PHILLIPS, 6-32 x 5/16	
2	10126402	WASHER, LOCK, EXTERNAL TOOTH, 8	
3	10126401	WASHER, LOCK, EXTERNAL TOOTH, 6	
4	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	
5	10125108	NUT, HEXAGON, 10-32	
6	10125607	WASHER, FLAT, 10	
7	10125603	WASHER, FLAT, 4	
8	10125106	NUT, HEXAGON, 8-32	
9	10125105	NUT, HEXAGON, 6-32	
10	10125103	NUT, HEXAGON, 4-40	
11	10127122	SCREW, MACHINE, PAN HEAD, PHILLIPS, 8-32 x 3/8	
12	10126400	WASHER, LOCK, EXTERNAL TOOTH, 4	
13	95662216	SCREW, MACHINE, ROUND HEAD, SLOTTED, 10-32 x 2-1/4	
14	10127121	SCREW, MACHINE, PAN HEAD, 8-32 x 5/16	
15	10127125	SCREW, MACHINE, PAN HEAD, 8-32 x 3/4	
16	10127113	SCREW, MACHINE, PAN HEAD, 6-32 x 3/8	
17	10125713	SCREW, MACHINE, FLAT HEAD, 6-32 x 5/16	
18	10125703	SCREW, MACHINE, FLAT HEAD, 4-40 x 5/16	
19	10127112	SCREW, MACHINE, PAN HEAD, 6-32 x 5/16	
20	75029200	BRACKET, PANEL	
21	73646800	MAINTENANCE PANEL ASSEMBLY	
22	76506101	PANEL, MAINTENANCE	
23	93152001	KNOB, SKIRTED	
24	94259300	SWITCH, ROTARY	
25	93126310	SWITCH, BUTTON, BLACK	
26	94372500	DIODE, LIGHT EMITTING	
27	94264101	JACK, INSULATED	
28	94264100	JACK, INSULATED	
29	94264103	JACK, INSULATED	
30	94259301	SWITCH, ROTARY	
	76383200	PIN AND BOARD ASSEMBLY	
	92007029	NUT, HEXAGON	
	92512154	RESISTOR, 1/4 W, 140 OHM	
	92512160	RESISTOR, 1/4 W, 2.2K OHM	
	72804407	MAINTENANCE PANEL CABLE ASSEMBLY	
31	94001000	TAPE, FOAM	
32	83220500	PLENUM, AIR, LOGIC	
33	75089500	PANEL, DC	S/C 11 & BLW
33	77470700	PANEL, DC	S/C 12 & ABV, ALL EXCEPT BR3C9J/K, BR3E4/5E
33	77470701	PANEL, DC	BR3C9J/K, BR3E4/5E
34		PLUS COMPONENT ASSY, VOLTAGE REGULATOR (SEE FIG. 17)	
35		MINUS COMPONENT ASSY, VOLTAGE REGULATOR (SEE FIG. 18)	
36	75025100	BRACKET, RECEPTACLE MOUNTING	
37	95667412	RESISTOR, POWER, 30 W, 50 OHM	
38	95667415	RESISTOR, POWER, 30 W, 150 OHM	
39	95667417	RESISTOR, POWER, 30 W, 250 OHM	
40	94248608	SWITCH, AIR FLOW	
41	47120500	INDUCTOR, 1 AMP, 6 M.H.	
42	95661312	CAPACITOR, 15 VOLT	
43	92691011	CLAMP, CAPACITOR MOUNTING	
44	95642415	CAPACITOR, 25 VOLT	
45	95578105	CAPACITOR, 50 VOLT	
46	93592196	SCREW, MACHINE, HEX HEAD, STP, 8-32 x 1/4	
47	10127111	SCREW, MACHINE, PAN HEAD, PHILLIPS, 6-32 x 1/4	
48	82346800	CLAMP, CAPACITOR	S/C 29 & BLW
48	47278600	CLAMP, CAPACITOR	S/C 30 & ABV
49	94387400	RELAY, POWER	
50	94260900	RELAY, POWER	
51	92696041	CIRCUIT BREAKER, 2 AMP, 50 VOLT	
52	92696047	CIRCUIT BREAKER, 7 AMP, 50 VOLT	
53	92696021	CIRCUIT BREAKER, 15 AMP, 50 VOLT	
54	94268303	CIRCUIT BREAKER, 2 AMP, 50 VOLT	
55	93522006	PLUG, SNAP BUTTON, 1/2	All EXCEPT BR3C9J/K,BR3E4/5E
55	92501047	SWITCH, TOGGLE	BR3C9J/K, BR3E4/5E

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
15-		LOGIC CHASSIS ASSEMBLY (SHEET 2 CONT'D)	
56	94039102	LIGHT, INDICATOR, 24 VOLT	
57		SENSING BOARD ASSEMBLY (SEE FIGURE 19)	
58	95583503	BLOCK, RECTIFIER, 15 AMP	
59	93590162	SCREW, PAN HEAD, PHILLIPS, TPG, 6-32 x 3/8	
60	94317708	FASTENER, OVAL, FLUSH STUD	
61	94317900	RETAINER, SPLIT RING	
62	94294106	RELAY, TELEPHONE, 4 PDT	
63	94294104	RELAY, COVER, TELEPHONE, 16 PIN	
64	73483200	COMPONENT ASSEMBLY, RELAY	ALL EXCEPT BR3C9J/K, BR3E4/5E
	73645103	COMPONENT ASSEMBLY, RELAY	BR3C9J/K, BR3E4/5E
	93114214	STANDOFF, TAPPED POST	
	94245801	SOCKET, RELAY, TELEPHONE	
	93935000	RECTIFIER, SILICON	
	92512150	RESISTOR, FIXED, 1/4 W, 47 OHM	
	92496239	CAPACITOR, 100 VOLT, 0.01 UF	
	10127333	SCREW, MACHINE, PAN HEAD, SLOTTED, 6-32 x 5/16	
65	94309900	SUPPORT, FALL	
66	75025000	BRACKET, FALL STOP MOUNTING	
67	75025300	CLAMP, CAPACITOR	
68	95645600	CAPACITOR, 40 VOLT, 55 UF	
69	95661308	CAPACITOR, 15 VOLT	
70	95642401	CAPACITOR, 25 VOLT	
71	94317800	RECEPTACLE, CLIP-ON	
72	94281474	CABLE, GROUND	
73	94208500	LABEL	
74	94281435	CABLE, GROUND	
75	10126105	WASHER, LOCK, INTERNAL TOOTH, 10	
76	47316301	BAR, BUS, 3 TERM	
77	47316501	BAR, BUS, 3 TERM	
78	75041700	BAR, BUS, 2 TERM	
79	774733XX	LOGIC HARNESS ASSEMBLY	
80	10125804	WASHER, SPRING LOCK, 8	
81	93592196	SCREW, MACHINE, HEX HEAD, STP, 8-32 x 1/4	
82	10127122	SCREW, PAN HEAD, MACHINE, 8-32 x 3/8	
83	10127141	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 5/16	
84	10127142	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 3/8	
85	10127144	SCREW, MACHINE, PAN HEAD, PHILLIPS, 10-32 x 5/8	
86	93109238	SPACER, STANDOFF	
87	10127146	SCREW, MACHINE, PAN HEAD, SLOTTED 10-32 x 7/8	
88	93109240	SPACER, STANDOFF	
89	10126403	WASHER, LOCK, EXTERNAL TOOTH, 10	
90	92318027	INSULATOR, FISH PAPER	
91	77531500	ARC SUPPRESSION ASSEMBLY	S/C 11 & BLW
91A	77539300	ARC SUPPRESSION ASSEMBLY	S/C 12 & ABV
92	94375865	SCREW, THD ROLL, PAN HEAD, 8-18 x 1/2	
93	77409013	FOAM, PANEL	S/C 29 & BLW
93	77409014	FOAM, PANEL	S/C 30 & ABV
94	10125704	SCREW, MACHINE, FLAT HEAD, PHILLIPS, 4-40 x 3/8	
95	10127105	SCREW, MACHINE, FLAT HEAD, PHILLIPS, 4-40 x 1/2	
96	10126101	WASHER, LOCK, INTERNAL TOOTH, 4	
97	93749158	SCREW, MACHINE, FLAT HEAD, PHILLIPS, (SEM), 6-32 x 1/4	
98	82366200	CLAMP, BASE, CAPACITOR	S/C 30 & ABV
99	00861303	NUT, SELF-LOCKING, CAP	
100	75130600	COVER, RELAY	
101	10127126	SCREW, MACHINE, PAN HEAD, 8-32 x 7/8	
102	94393702	RELAY	BR3C9J/K, BR3E4/5E ONLY
103	94393705	RELAY, SPRING	BR3C9J/K, BR3E4/5E ONLY
104	93749158	SCREW, MACHINE, PAN HEAD, 6-32 x 1/4	BR3C9J/K, BR3E4/5E ONLY

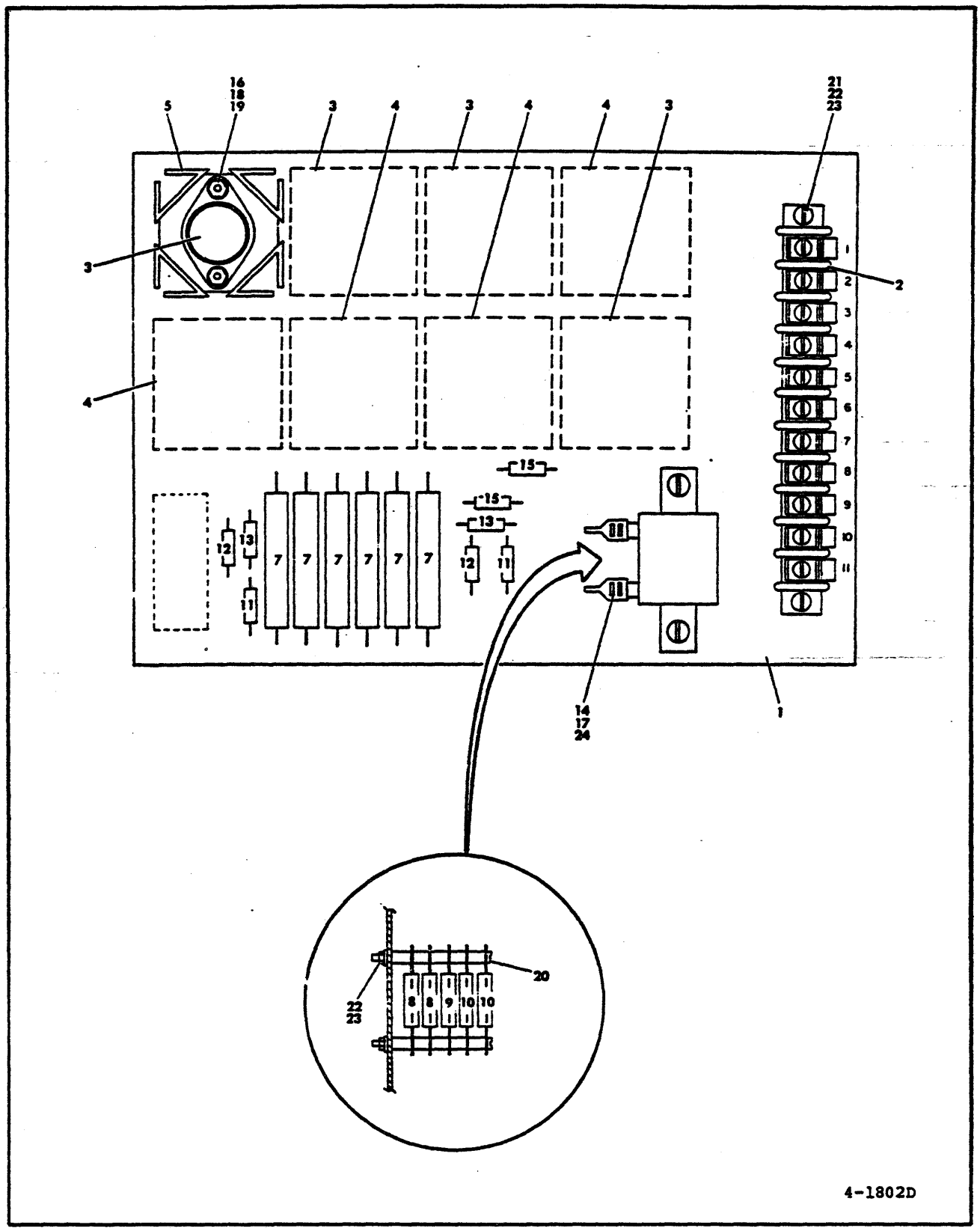


FIGURE 16. 3ZCN COMPONENT ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
16-	75183600	COMPONENT ASSEMBLY, TYPE 3ZCN	
1	75183500	BOARD, POST WIRE WRAP	
2	95591206	TERMINAL STRIP, QUICK CONNECT	
3	50221601	TRANSISTOR, POWER	
4	50221701	TRANSISTOR, POWER	
5	94261002	HEAT SINK, TRANSISTOR	
6		NOT USED	
7	95594100	RESISTOR, FIXED, 10 W, 1 OHM	
8	94237013	RESISTOR, POWER, 30 W, 5 OHM	
9	94237019	RESISTOR, POWER, 30 W, 250 OHM	
10	94237011	RESISTOR, POWER, 30 W, 0.5 OHM	
11	92512867	RESISTOR, FIXED, 1 W, 100 OHM	
12	92512879	RESISTOR, FIXED, 1 W, 470 OHM	
13	92115037	DIODE, ZENER, SILICON	
14	95643227	CONNECTOR, QUICK CONNECT	
15	93542001	RECTIFIER, GERMANIUM	
16	95510026	NUT, HEXAGON, MACHINE, SCREW	
17	95643226	CONNECTOR, QUICK CONNECT	
18	95683510	STUD, PRESS	
19	10126103	WASHER, LOCK, INTERNAL TOOTH, 6	
20	10127358	SCREW, MACHINE, PAN HEAD, SLOTTED, 8-32 x 2-3/4	
21	10127350	SCREW, MACHINE, PAN HEAD, SLOTTED, 8-32 x 3/4	
22	10125106	NUT, HEXAGON, 8-32	
23	10126104	WASHER, LOCK, INTERNAL TOOTH, 8	
24	95643212	CONNECTOR, QUICK CONNECT	

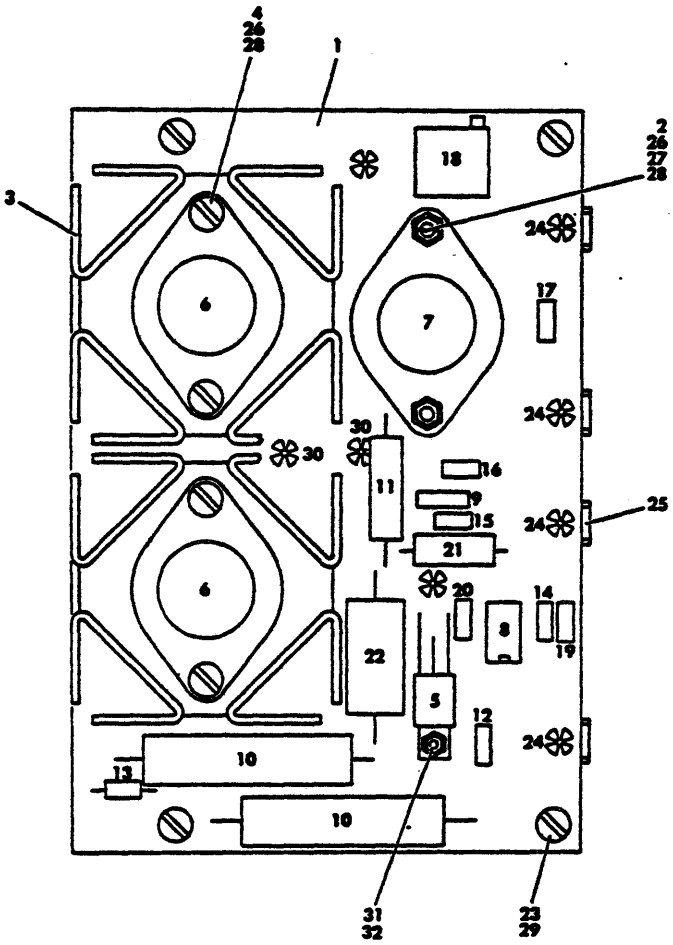


FIGURE 17. PLUS VOLTAGE REGULATOR ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
17-	75179802	PLUS VOLTAGE REGULATOR ASSEMBLY	
1	75179701	BOARD, BLANK	
2	95683509	STUD, PRESS	
3	94261002	HEAT SINK, TRANSISTOR	
4	95683510	STUD, PRESS	
5	94262016	TRIAC, BI-DIRECTIONAL	
6	50221301	TRANSISTOR, SILICON	
7	50221401	TRANSISTOR, SILICON	
8	95596100	VOLTAGE REGULATOR, INTEGRATED CIRCUIT	
9	50240107	DIODE, SILICON, 5.6 VOLT, 11 OHM	
10	92825001	RESISTOR, FIXED, 7 W, .1 OHM	
11	92512913	RESISTOR, FIXED, 2 W, 33 OHM	
12	94360143	RESISTOR, FIXED, 1/4 W, 28.0 OHM	
13	92512248	RESISTOR, FIXED, 1/4 W, 68 OHM	
14	94360211	RESISTOR, FIXED, 1/4 W, 130 OHM	
15	92512160	RESISTOR, FIXED, 1/4 W, 2.2K OHM	
16	92512256	RESISTOR, FIXED, 1/4 W, 1.8K OHM	
17	92512259	RESISTOR, FIXED, 1/4 W, 5.6K OHM	
18	92617031	POTENTIOMETER, 2K OHM	
19	92496143	CAPACITOR, 560 µF, 200 VOLT	
20	92496147	CAPACITOR, 1200 µF, 200 VOLT	
21	92427039	CAPACITOR, 6.8 µF, 35 VOLT	
22	92427133	CAPACITOR, 100 µF, 15 VOLT	
23	93114269	STANDOFF, TAPPED POST	
24	93903018	EYELET, ROLLED FLANGE	
25	92474143	TERMINAL, QUICK CONNECT	
26	95510026	NUT, HEX, MACHINE, SCREW	
27	10125605	WASHER, PLAIN, FLAT, 6	
28	10126103	WASHER, INTERNAL TOOTH, LOCK, 6	
29	10127332	SCREW, MACHINE, PAN HEAD, SLOTTED, 6-32 x 1/4	
30	94261700	EYELET, P-W BOARD	
31	93640012	STUD, SELF CLINCHING	
32	92583002	NUT, LOCK	

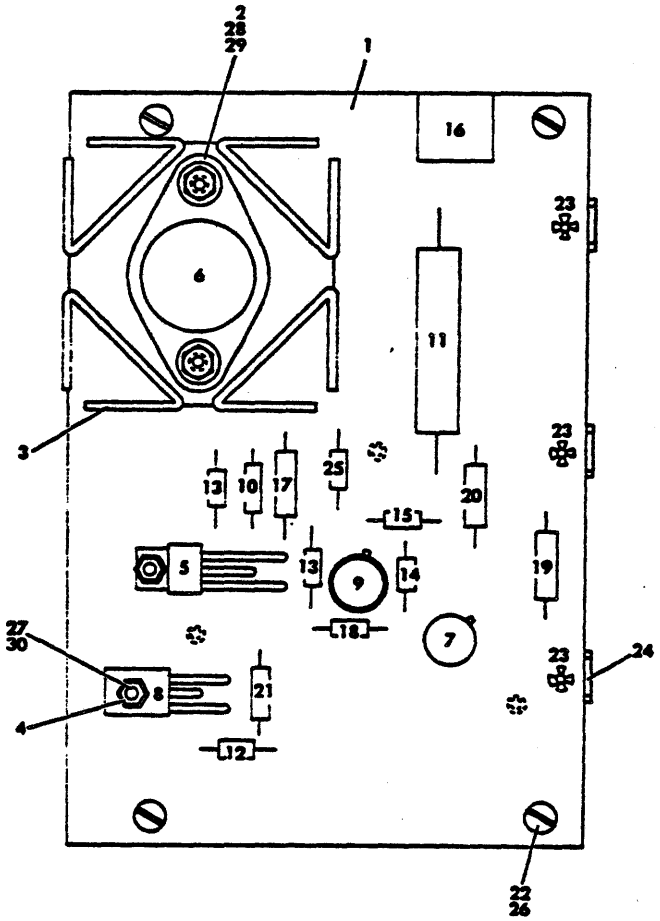
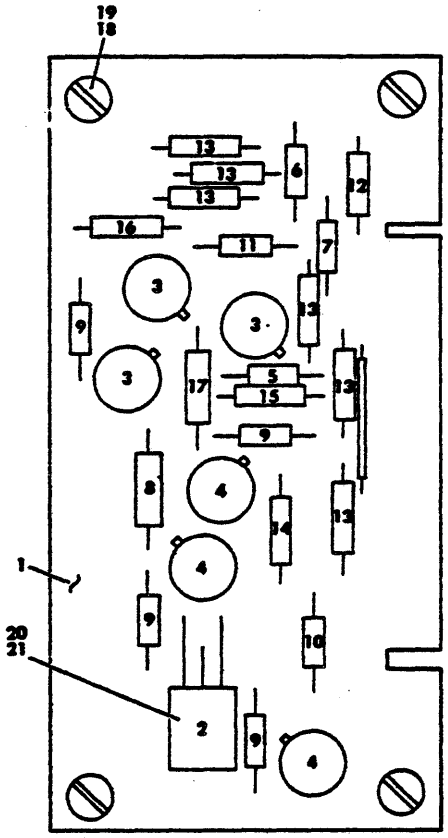


FIGURE 18. MINUS VOLTAGE REGULATOR ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
18-	75184101	MINUS VOLTAGE REGULATOR ASSEMBLY	
1	75184000	BOARD, BLANK	
2	95683510	STUD, PRESS	
3	94261002	HEAT SINK, TRANSISTOR	
4	92583002	NUT, LOCK	
5	94262016	TRIAC, BI-DIRECTIONAL	
6	50221301	TRANSISTOR, SILICON	
7	50210610	TRANSISTOR, SILICON	
8	50221001	TRANSISTOR, SILICON	
9	95592500	VOLTAGE REGULATOR, INTEGRATED CIRCUIT	
10	50240107	DIODE, SILICON, 5.6 VOLTS, 11 OHM	
11	95334002	RESISTOR, FIXED, 7W	
12	92512248	RESISTOR, FIXED, 1/4W, 68 OHM	
13	92512160	RESISTOR, FIXED, 1/4W, 2.2K OHM	
14	92512258	RESISTOR, FIXED, 1/4W, 1.0K OHM	
15	92512259	RESISTOR, FIXED, 1/4W, 5.6K OHM	
16	92617031	POTENTIOMETER, 2K OHM	
17	92427039	CAPACITOR, 6.8 UF, 35 VOLT	
18	92512245	RESISTOR, FIXED, 1/4W, 27 OHM	
19	92427087	CAPACITOR, 4.7 UF, 50 VOLT	
20	92427089	CAPACITOR, 22 UF, 15 VOLT	
21	24505225	CAPACITOR	
22	93114269	STANDOFF, TAPPED POST	
23	93903018	EYELET, ROLLED FLANGE	
24	94274143	TERMINAL, QUICK CONNECT	
25	92512255	RESISTOR, FIXED, 1/4W, 1.5K OHM	
26	10127332	SCREW, MACHINE, PAN HEAD, SLOTTED, 6-32 x 1/4	
27	93640012	STUD, CLINCHING	
28	10126103	WASHER, INTERNAL TOOTH, LOCK, 6	
29	95510026	NUT, HEX, MACHINE, SCREW	
30	10125603	WASHER, PLAIN, 4	



4-2100A

FIGURE 19. SENSING BOARD ASSEMBLY

INDEX NO.	PART NUMBER	PART DESCRIPTION	NOTES
19-	73515600	SENSING BOARD ASSEMBLY	
1	73489600	BOARD, WIRE WRAP	
2	50221001	TRANSISTOR, 60V	
3	50210811	TRANSISTOR, 40V	
4	50210610	TRANSISTOR, 25V	
5	92512156	RESISTOR, FIXED, 270 OHM, 1/4W	
6	92512249	RESISTOR, FIXED, 180 OHM, 1/4W	
7	92512165	RESISTOR, FIXED, 22K OHM, 1/4W	
8	92512831	RESISTOR, FIXED, 1.8K OHM, 1/4W	
9	92512253	RESISTOR, FIXED, 680 OHM, 1/4W	
10	92512160	RESISTOR, FIXED, 2.2K OHM, 1/4W	
11	92512261	RESISTOR, FIXED, 15K OHM, 1/4W	
12	50240117	DIODE, SILICON, 16 OHM, 15 VOLT	
13	92115021	DIODE, SILICON, 10 OHM, 30 VOLT	
14	93935000	RECTIFIER, SILICON	
15	50240110	DIODE, SILICON, ZENER	
16	50240102	DIODE, SILICON, 24 OHM, 3.6 VOLT	
17	92512829	RESISTOR, FIXED, 1.5K OHM, 1/2W	
18	93114214	STANDOFF, TAPPED POST	
19	10127332	SCREW, MACHINE, PANHEAD, SLOTTED, 6-32 x 1/4	
20	92583002	NUT, LOCK	
21	93640011	STUD, SELF CLINCHING	

CARD COMPLEMENT

LOCATION	LOGIC CARD TYPE	PART NUMBER	NOTES
A1	CSAV	54150104	S/C 32 & BLW
A1	JSAV	54150110	S/C 33 & ABV
A2	CSAV	54150104	
A3	3PBV	54120501	
A4	AWMV	54194501	
A5	3PBV	54120501	
A6	3PBV	54120501	
A7			
A8	4UCV	54170901	
A9	BULV	54174101	BR3C9J/K,BR3E4/5E ONLY
A10	AWMV	54194501	
A11	2WEV	54191709	
A12	1WMV	54194500	
A13	5RQV	54145700	
A14	AHEV	54241701	
A15	AHFV	54242101	
A16	0WAV	54190100	
A17	AAHV	54092901	
A18	4KEV	54261700	BR3C9, ONLY
A19	BWMV	54194502	
A20	0WAV	54190100	
A21			
A22	1FWV	54228100	
A23	GWZV	54199311	
A24	AQZV	54139301	
A25	4FVV	54227702	
A26	1HQV	54245700	
A27	AMSV	54296502	
A28	4MZV	54299301	
A29			
A30	4FRV	54226110	
B1	0WDV	54191300	
B2	0WDV	54191300	
B3	0WDV	54191300	
B4	1HBV	54240500	
B5	1HCV	54240900	
B6	1HDV	54241300	
B7	1HHV	54242900	
B8	AHKV	54243701	
B9	1WMV	54194500	
B10	0WAV	54190100	
B11	1ALV	54094100	
B12	1HLV	54244100	
B13	1HJV	54243300	
B14	1WGV	54192501	
B15	1WBV	54190501	
B16	1WBV	54190501	
B17	1WBV	54190501	
B18	AHGV	54242501	
B19			
B20	AEJV	54213302	S/C 48 & BLW
C1	1AJV	54093300	
C2	1AJV	54093300	
C3	1AJV	54093300	
C4	1AJV	54093300	
C5	1AJV	54093300	
C6	1AJV	54093300	
C7	1AJV	54093300	
C8	1AJV	54093300	
C9	0WAV	54190100	
C10	0WAV	54190100	
C11	2HXV	54248501	
C12	AHSV	54246501	
C13	4HTV	54246901	
C14	1HRV	54246100	
C15	4HTV	54246901	DUAL CHANNEL,ONLY
C16	1HRV	54246100	DUAL CHANNEL,ONLY
C17	AHYV	54248901	
C18	1HZV	54249300	
C19	1HZV	54249300	DUAL CHANNEL,ONLY
C20	2HVV	54247702	
C21	CHUV	54247304	
C22	2BPV	54105300	S/C 48 & BLW
C22	EBPV	54105307	S/C 49 & ABV
C23	BFMV	54224504	
C24	AHNV/AHPV	73482300	MATCHED SET
C25	AHNV/AHPV	73482300	MATCHED SET
C26			
C27			
C28	4FJV	54223305	
C29			
C30	BMRV	54296103	
C30			
D1			
D2	1HAV	54240100	
D3	1HAV	54240100	
D4	1WBV	54190501	
D5	1WBV	54190501	
D6	1WBV	54190501	
D7	1AJV	54093300	
D8	0WAV	54190100	
D9	0WAV	54190100	
D10	0WAV	54190100	
D11			
D12			
D13			
D14			
D15			
D16			
D17			
D18			
D19			
D20			
E0	BZPN	72829610	
E1	4FPV	54225311	
E2	1ATV	54096900	
E3	DFLV	54224105	
E4	5FNV	54224904	
E5			
E6			
	SERVO PREAMP ASSEMBLY	73485304	