Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
6000B INPUT/OUTPUT MULTIPLEXER (IOM) CENTRAL

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C O N T E N T S

1.0 GENERAL DESCRIPTION

The IOM Central controls access to storage for the various channels of the IOM by providing appropriate services to the channels, one at a time.

The IOM has eight generic types of channels:

- o Data Channel
- o Connect Channel
- o Fault Channel
- o Wraparound Channel
- o Bootload Channel
- o Snapshot Channel
- o Scratchpad Access Channel
- o Special Status Channel

Each channel has assigned to it four (4) 36 bit mailbox words. The use of these words vary with the type of channel. The words are listed below in the order that they appear in a memory map (lowest address first) and the definitions appear later in the text.

List Point Word (LPW)
List Pointer Word Extension
Status Control Word (SCW)
Working Storage for Data Control Word (DCW)

The data channels are "payload" channels; they are responsible for information transfer with all external peripheral devices and adapters. The other seven types of channels are "overhead" channels; they perform specialized internal functions necessary for successful operation of the IOM.

The IOM Central includes a scratchpad storage to hold various channel control words. The scratchpad is a high speed store accessible to the IOM Central and the scratchpad access channel. It is used to reduce the time required for performing various services to channels, by storing control words for from 16 to 32 payload channels. The LPW, LPW extension and DCW (see paragraph 3.2) for each channel will normally be stored in scratchpad memory, unless scratchpad is not provided for a particular group of channels (see paragraph 2.2.2).

Following the introduction to the various functions, a description of a typical operation is included at the beginning of Section 3.0.

1.1 DATA CHANNELS

Each data channel controls the flow of instructions, data and status between the IOM Central and a peripheral (or special) control unit. A data channel can use either of two basic methods of data transfer; direct or indirect. When the direct method of data transfer is used, the data channel specifies the core location (address) for each storage access. When the indirect method of data transfer is used, the IOM Central relieves the data channel of the task of addressing at the price of additional accesses by the IOM to: (a) core, or (b) scratchpad storage. The indirect data channel must, however, specify its channel number, which determines the location of its control words. Each time the indirect data channel makes an access request, the IOM Central obtains from core (or from the scratchpad) the appropriate control word, which defines the address for the data transfer and a tally specifying the amount of data to be transferred.

Each type of interface to a peripheral (or specials) control unit requires a particular type of data channel, so that in general there are several types of data channels, each of which is referenced in paragraph 1.4, Applicable Documents.

Data can be transferred between the IOM Central and either core storage or an indirect data channel in byte sizes of 9, 36 and 72 bits.

1.2 OVERHEAD CHANNELS

An overhead channel is a non-optional part of the IOM Central that provides a specific function and has some of the characteristics of a payload channel (i.e., uses the interface bus, competes with payload channels for service, has channel numbers, uses some mailboxes, etc.).

1.2.1 Bootload Channel

The bootload channel consists of non-destructive storage implemented as an IOM channel. When activated, it forces a limited number of interrupt vectors and control words to be stored in core storage, reads a record, and places the system into operation. The read is initiated by a Connect ($CON) signal the IOM issues to itself.

1.2.2 Connect Channel

The connect channel controls the distribution of instructions which initiate the operation of any addressable channel capable of receiving instructions.

1.2.3 System Fault Channel

The system fault channel is responsible for reporting the occurrence of system fault conditions to the software. System faults are abnormal conditions resulting from the failure of hardware or system software. (System software consists of programs supplied for the purpose of controlling the operation of the computer system. System software does not include customer or application programs. Abnormal conditions in customer programs are reported by the affected data channel, and are classed as user faults rather than system faults, insofar as it is practical).

1.2.4 Wraparound Channel

The wraparound channel is a special channel intended for use by test and diagnostic software. By means of instructions issued to the wraparound channel by the software, the wraparound channel will cause the IOM Central to perform any specific type of service on behalf of any payload channel number designated in the instruction. The wraparound channel includes a data register and a status register which can be loaded and stored by means of appropriate services so that most data paths and control sequences in the IOM Central can be checked under program control.

1.2.5 Snapshot Channel

The snapshot channel is a special channel for use by test and diagnostic software. It permits the software to sample particular signals in the IOM Central on the occurrence of events selected by the software.

1.2.6 Scratchpad Access Channel

The scratchpad access channel is a special channel used by the operating system and test and diagnostic software. It permits the software to read or write from the scratchpad.

1.2.7 Special Status Channel

The special status channel is a special channel which may be accessed by data channel adapters to store status associated with a special interrupt.

1.3 SCOPE OF THIS DOCUMENT

This document defines the functional and operational characteristics of the IOM Central and its overhead channels. This document does not define the various payload channels beyond the characteristics of their common interface to the IOM Central. For information about the payload channels refer to the Engineering Product Specifications for these channels.

1.4 APPLICABLE DOCUMENTS

EPS-1, 6000 System (58001123)

EPS-1, 6000 System Controller (43A219602)

EPS-1, IOM Common Peripheral Channel (43A219605)

EPS-1, 6000B IOM Direct Channel (43A239853)

EPS-1, IOM Peripheral Subsystem Interface Adapter (43A177880)

EPS-1, Console Channel Adapter (43A232500)

General Design Requirements for 655/355 (43A177851)

655 Maintainability Design (43A219617)

B Option Application Data List (43B240276)

1.5 DEFINITIONS

1.5.1 Tally Runout (TRO)

In this document, a tally runout is a fault, defined as an exhausted LPW tally field (the contents of LPW bits 24 - 35 equal to zero), and LPW bits 21 and 22 set to 0, 1, respectively, at the time the LPW is taken from its mailbox in core or in scratchpad.

1.5.2 Pre-Tally Runout (PTRO)

A pre-tally runout is defined as a tally in either a DCW or an LPW which will be reduced to zero by the current channel service (DCW during data service, LPW during list service).

1.5.3 List Pointer Word (LPW)

A word containing an address "pointing" to a list of control words, either DCW's or PCW's. NOTE: Only an LPW for a Connect Channel may legally point to a PCW.

1.5.4 Data Control Word (DCW)

A word containing an address indicating the first or current word of data in a list of data. IDCW, TDCW, IOTP, IONTP, and IOTD are variations of DCW's.

1.5.5 Peripheral Control Word (PCW)

A word containing the number of the channel to be connected and, for CPI, an instruction or operation to be performed by a peripheral subsystem.

1.5.6 Status Control Word (SCW)

A word containing an address indicating the first or current empty position in a list of status words used by a particular channel.

1.5.7 First List Service

A flag supplied by the channel to the IOM on the first list service following a connect. It directs the IOM to access the core LPW and LPWE mailboxes whether or not this channel has a scratchpad.

2.0 FUNCTIONAL CAPABILITIES

2.1 BASIC CHARACTERISTICS

2.1.1 General

The 6000B IOM will have the following characteristics:

- The ability to operate in a GCOS III mode with no Operating System or Slave software programming interface difference over the 6000 IOM design.
- The capability of operating in an Extended GCOS or MULTICS mode where addressable memory space to 2^{24} locations is possible.
- The ability to change MODE by a manually operated configuration switch.
- The capability of interfacing up to eight (8) 6000B or 6000 System Controllers. There shall be one three position switch for each pair of ports. The following pairs of ports may be interlaced:

  Ports A and B
  Ports C and D
  Ports E and F
  Ports G and H

  The interlace mode may either be two (address bit 22) or four (address bit 21) word blocks.
- Provision for control word scratchpad storage for at least 24 payload channels.
- The ability to indicate with a configuration switch per port, that either all or half of the address range assigned to a memory port is available.
- The ability to support 36, 72 or 9 bit byte channels.

2.1.2 Relationship to 6000 IOM

The following variations from the standard 6000 IOM are required for address extension to 2^{24} locations:

- Control word mailboxes, interrupt multiplex words, PCW lists, system fault word lists, and status queues will reside in the first 256K core. DCW's may reside in either the first 256K block or in the same 256K block as the data (depending upon LPW bit 20).

- Transactions which cause addresses to be incremented will not be allowed to occur across modulo 256K (absolute) boundaries. That is, overflow past 2^{18} is not allowed.

- The "address extension" (i.e., the 6 most significant bits of a 24-bit address field) will be used for all data transfers and, depending on LPW 20, may also be used when fetching a DCW during a list service. It will be obtained from the following sources:

  1) From bits (12-17) of a PCW directed to a data channel in the Extended GCOS mode.

     Restrictions: None.

  2) During a list service from bits (12-17) of an IDCW directed to a data channel provided IDCW 21=1.

     Restrictions: None.

2.2 CONFIGURATIONS

2.2.1 Basic IOM Central

The basic IOM Central has one connect channel, one system fault channel, one wraparound channel, one snapshot channel, one boot-load channel, one scratchpad access channel, and one special status channel. No payload channels, system controller ports or scratchpads are included. Space is provided for 36 payload channel boards, one of which is used for the wraparound channel.

2.2.2 Options

- The 6000B IOM cabinet must be capable of supporting all the options listed in the Option Application Data List, 43B240276. A subset of these includes: from one to eight Ports to connect to 6000B or 6000 System Controllers.

- Provisions for adding space for 19 additional payload channel boards to the basic IOM.

- Payload Channels: The following payload channels may be used with the IOM:

  6000B IOM Common Peripheral Channel (2 board spaces per channel required)

  6000B IOM Peripheral Subsystem Interface Adapter (3 board spaces per channel required)

  6000B IOM Direct Channel (1 board space per channel required)

  6000B IOM Console Channel Adapter (3 board spaces required for each two channels)

- Scratchpad: Scratchpads may be supplied for storage of control words. Scratchpads are added in groups of 16 channels. A maximum of 32 payload channels may be handled by the scratchpads.

  When scratchpad modules are used, the channels whose control words are stored in the scratchpad will be determined on the basis of channel number, as follows:

  The first optional scratchpad module is used for storage of control words for channels numbered 010_8-027_8.

  The second optional scratchpad module is used for storage of control words for channels numbered 030_8-047_8.

2.3 DATA TRANSFER RATES

The IOM Central will be capable of performing only one storage access cycle at any one time, regardless of the number of System Controllers to which it may be connected. When connected to a 6000B System Controller which is kept extremely busy by competition from processors and/or other IOM's, the IOM must be capable of requesting the next access cycle quickly enough to obtain every fourth cycle of the same bank of core storage.

The following conditions are assumed in specifying the data transfer rate capability:

1) The referenced System Controller and core store are continuously busy.

2) Several channels of the same type are operating simultaneously to achieve the stated maximum transfer rate. (No single channel is required to be serviced at the stated maximum rate.)

3) Statement of the quantity of words per second further assumes a channel operating in double precision; 72 bits or two 36-bit words per access.

4) Data transfers in each direction (Reads and Writes) are equally probable.

5) Nominal circuit delay times are assumed.

6) Turn around times at IOM interface with 50 foot cables will be assumed as follows: (a) $INT to $DA with 0.5 microsecond memory = 820 nanoseconds; (b) $INT to $DA with 1.2 microseconds memory = 1500 nanoseconds.

Based on these assumptions, the following minimum capability of data transfer rates (total data throughput) are required of the IOM Central:

1) Using a 6000B System Controller and store, and indirect data channels operating without a scratchpad: one data access every 4.5 microseconds, or 440,000 words per second when using a 0.5 microsecond store and one data access every 9.3 microseconds or 215,000 words per second when using a 1.2 microsecond store.

2) Using a 6000B System Controller and store, and either direct channels or indirect channels operating with a scratchpad: one data access every 2.0 microseconds, or 1,000,000 words per second when using a 0.5 microsecond store and one data access every 3.2 microseconds or 625,000 words per second when using a 1.2 microsecond store.

2.4 CONCURRENT OPERATION

The time required for the IOM Central to perform an indirect data service (and consequently for other types of service) is intended to be substantially less than the time required for the requesting channel to accumulate or disperse the data. As a result, the IOM Central will be time shared by a number of channels operating concurrently. The IOM Central provides appropriate services to the channels, one at a time. Such concurrent operation of channels will be successful only if the fraction of available service time used by each channel, summed over all concurrently operating channels is less than one, and if there is a sufficient amount of buffering in each concurrently operating channel.

2.5 DATA FORMATS

An indirect data channel may work with byte sizes of 9, 36 or 72 bits. The IOM Central is capable of packing successive 9 bit bytes received from an indirect data channel into successive 9 bit byte positions, left to right, in a 36-bit word. It also may unpack 9 bit bytes from successive byte positions in a 36-bit word, left to right, for transmission to an indirect data channel. The Common Peripheral Channel will perform its own packing and unpacking.

Evolving system configurations and peripheral data transfer rates emphasize the need to fully utilize the available 6000B system controller interface, not only to maximize IOM thruput but to minimize I/O interference with storage access by system processors. The use of a 72 bit interface can result in a thruput increase when operating with a channel capable of buffering the 72-bit data width. The IOM Central design will incorporate the 72-bit data transfer capability.

Thus for indirect data channels the data in core store can be formatted as

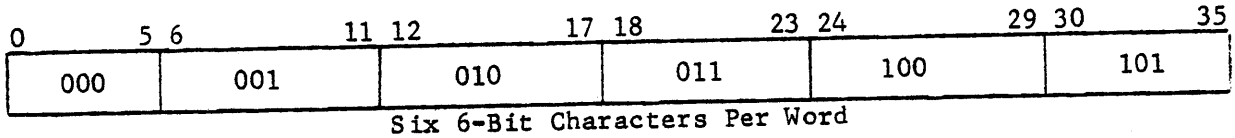
- one 9-bit character per access
- one 36-bit word per access
- two 36-bit words per access

The formatting chosen for programming purposes must be consistent with the character size used by the indirect data channel. The 3-bit codes shown in the following formats identify the various character positions within a word. Each type of indirect data channel determines which of the three formats can be used. A 36-bit channel will access one 36-bit word per access, and a 72-bit channel may access either one or two 36-bit words per access, depending upon the address and tally requirements.

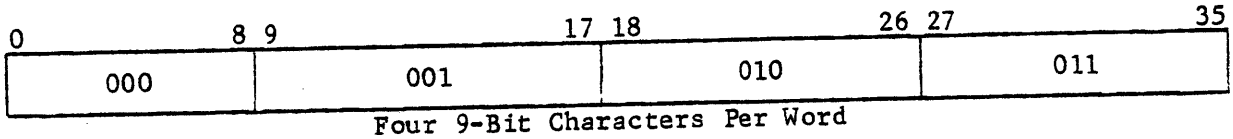
2.5 DATA FORMATS (continued)

All direct channels are word channels; a word channel may be either direct or indirect.

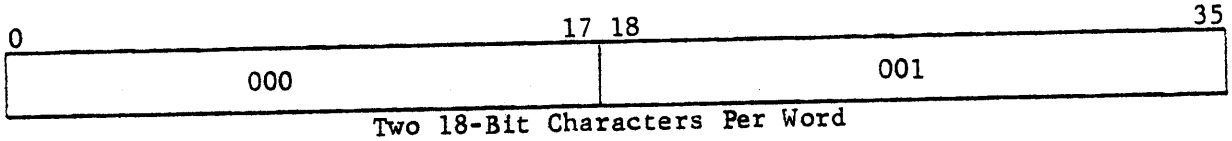
A word channel transfers one or two 36-bit words at a time, although each 36-bit word may be effectively subdivided into characters by the channel.



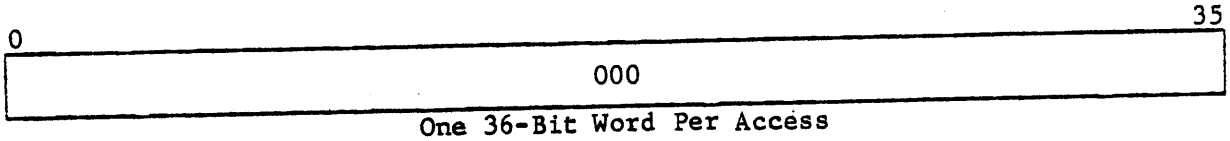
Six 6-Bit Characters Per Word



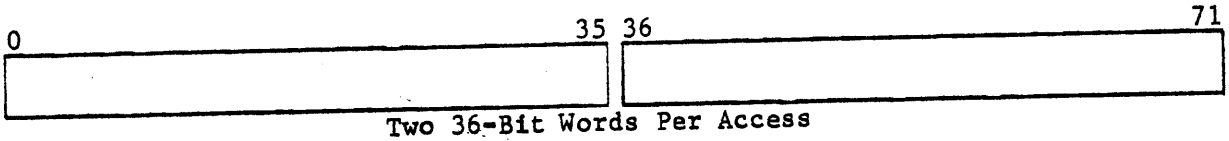
Four 9-Bit Characters Per Word



Two 18-Bit Characters Per Word



One 36-Bit Word Per Access



Two 36-Bit Words Per Access

3.0 SOFTWARE AND CUSTOMER INTERFACE REQUIREMENTS

The following is a description of a typical operation of the IOM and an indirect data channel, such as a Common Peripheral Channel. Exceptions to this description arise at many places, but discussion of these is held for detailed description further into the EPS.

The software must prepare several control words, in addition to a buffer area for data to be transferred. Data Control Words indicating the locations of each data area must be placed in a DCW list. A List Pointer Word (LPW) indicating the location of the DCW list must then be placed in the core LPW mailbox for the channel to be used.

For the purpose of this discussion, assume that channel 020_8, a payload channel, is to be issued an instruction to transfer data (Write) to the peripheral attached to its interface. A Status Control Word placed in the same channel's SCW mailbox area points to an area of core set aside to receive the status words resulting from the peripheral instructions to be issued. A Peripheral Control Word containing the necessary channel and peripheral instruction codes is placed in another area of core, with a second word containing the channel number (020) of the channel under discussion. The LPW mailbox for the connect channel is provided with a pointer to a list of such PCW's, allowing several payload channels to be initiated with a single connect instruction. As described later, the entire mailbox area is a contiguous block of words, four per channel, relocatable by means of switches on the IOM Configuration Panel.

Operation in the IOM begins with the receipt of the $CON from a system controller, issued as a result of a connect instruction. The $CON causes the connect channel to request the IOM to perform a List Service. The IOM uses the LPW from the Connect Channel mailbox to obtain the PCW referencing channel 020. The Connect Channel LPW is updated and replaced in core after each payload channel has been given its PCW. The channel, which is here assumed to be receptive, stores the PCW from the connect channel, and initiates communication with its attached peripheral.

3.0 SOFTWARE AND CUSTOMER INTERFACE REQUIREMENTS (continued)

When the channel has determined that its peripheral is receptive to the instruction, the channel will request the IOM to perform a first list service, using the LPW in channel 020 core mailbox to obtain a DCW. The DCW is checked for several conditions, including absolutizing the address when specified, and placed in either* the core or scratchpad mailbox for channel 020. This particular DCW should be either an IOTP or an IOTD (I/O Transfer and Proceed or I/O Transfer and Disconnect). The LPW is updated and placed in both core and scratchpad mailboxes for channel 020. The channel now requests a data service of IOM, specifying an indirect data load. The IOM uses the DCW for channel 020 to obtain the first word or word pair from the data area in core specified by the DCW. The address and tally fields are updated and checked, and the DCW returned to the mailbox in core* or in scratchpad. The channel sends a release to the peripheral when its output buffers are full. B

The peripheral will subsequently request the data to be sent over its interface data lines. By a succession of Data and List Service requests, the channel will continue to supply data until one of the following types of events occur: (1) An abnormal status condition such as a parity error; (2) The peripheral has reached a termination condition; (3) All DCW's in the list including the final IOTD are exhausted.

Anything which causes the end of operation with the peripheral, with the exception of a system fault, will cause the channel to request the IOM to do a status service. Using the Status Control Word for channel 020, the IOM will store status in the status queue indicated by the SCW, update the SCW and restore it to the core mailbox.

Following the status service, the channel will request the IOM to do a multiplex interrupt service. Using a combination of configuration switches and interrupt level indication in the service request, the IOM will retrieve one of 32 interrupt multiplex words, set a bit to indicate which channel is causing the interrupt and restore the word, then finally set the corresponding interrupt cell in the system controller. This will inform the software that the sequence of operations is concluded.

3.1 SOFTWARE INTERFACE

The IOM is responsible for moving information between core storage and various peripheral devices as controlled by demand from the peripheral control units associated with the peripheral devices. These operations do not occur continuously, but are initiated by connects, controlled by control words, and their completions are indicated by program interrupts.

*To the scratchpad if the scratchpad (option) is in; otherwise to core.

3.1.1 Connects

The software initiates a new activity in the IOM by executing a CIOC (Connect) instruction directed to a System Controller port that is attached to the IOM. When a processor executes such an instruction, the System Controller sends a $CON signal to the IOM Central, which activates its connect channel. The connect channel initiates the operation of one or more channels as described in paragraph 3.7, Connect Channel.

3.1.2 Control Words

The IOM Central makes use of four 36-bit control words for each indirect channel:

- o List Pointer Word (LPW)
- o List Pointer Word Extension (LPW extension)
- o Status Control Word (SCW)
- o Data Control Word (DCW)

Refer to paragraph 3.2 for descriptions and locations of these control words.

3.1.3 Program Interrupts

The IOM must inform the processor of the completion of a previously initiated activity or of the occurrence of other special events such as special interrupts from a peripheral, marker interrupts* from a channel, termination of an activity because of abnormal status, or fault conditions requiring attention of the software.

The IOM accomplishes this by setting a predetermined program interrupt cell in the system controller that contains the IOM base address. The system controller then causes a program interrupt in a processor so that appropriate action can be taken by the software. Each IOM has access to its own set of eight interrupt cells in the maximum set of 32 cells. The selection of the interrupt level, and the cell associated with the level, is determined by the channel. This is further described in paragraph 3.2.7.

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*The marker interrupt indicates the normal completion of a PCW or an IDCW in a DCW list. This interrupt is under control of the Marker and Continue bits in the PCW or IDCW.

B —

3.2 CONTROL WORD FORMATS

The software is responsible for generating certain control words and for making these control words available to the IOM hardware by placing the control words in appropriate locations in core storage. The control words that the software is responsible for are:

- o List Pointer Words (LPW - see paragraph 3.2.1)
- o Peripheral Control Words - (PCW - see paragraph 3.2.2)
- o Data Control Words (DCW - see paragraph 3.2.3)
- o Status Control Words (SCW - see paragraph 3.2.4)

The IOM hardware is responsible for generating certain words and for making these words available to the software by placing them in appropriate locations in core storage. These may also be regarded as control words, since the correct operation of the IOM can only occur when there is appropriate interaction between the IOM hardware and the software. The response words that the IOM Central Hardware is responsible for are:

- o Status Words (see paragraph 3.2.5)
- o Fault Words (see paragraph 3.2.6)
- o Interrupt Multiplex Words (IMW - see paragraph 3.2.7)

3.2.1 List Pointer Words (LPW and LPW Extension)

The LPW is used to define the location and length of a list of

- o PCW's to be issued by the connect channel, or
- o DCW's to control the operation of a data channel.

The LPW, together with the LPW extension, also includes fields which control

- o the updating of the LPW
- o checking of DCW's for validity.

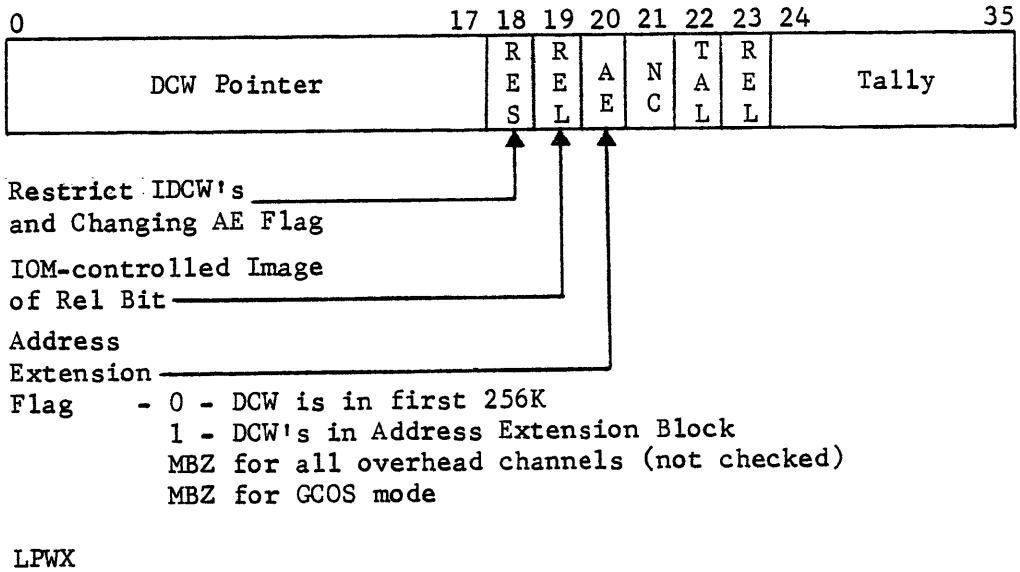
The software must generate an LPW and LPW extension for the specific data channel and place them in the appropriate locations in the core storage mailbox area before initiating the operation of that data channel by means of a PCW. The software must also generate an LPW for the connect channel and place it in the mailbox area before executing a CIOC instruction to initiate the operation of the connect channel.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

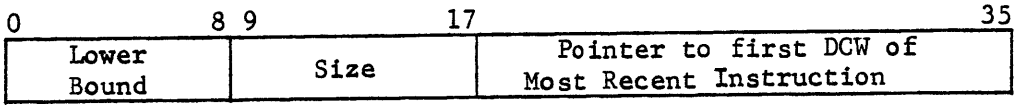
After the operation of a channel has been initiated, the IOM Central hardware must place into the LPW extension (in core and in scratchpad when available) the absolute address of each Instruction DCW which it encounters while servicing the list. (These are described in paragraph 3.2.3.)

The LPW and LPW extension have the formats shown below:

LPW



LPWX



3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

The various fields are defined as follows:

DCW (or PCW) Pointer (LPW 0-17) - Provides the least significant 18 bits of a 24 bit address of the DCW or PCW list. The most significant six address bits of the DCW depend on the state of LPW 20 (see below). Updating of this field is controlled by the NC (no change), TAL (Tally Control) and tally fields as shown in Table 3.2.1. When updating is called for, the IOM Central increments this field by one (two if the channel is the connect channel) during each list service.

Restricted Bit (LPW 18) - Provides the software with a way to restrict the use of Instruction DCW's by users without having to scan all DCW lists. If this bit is one and an Instruction DCW is encountered by the IOM Central, it will abort the I/O transaction and indicate a User Fault: Instruction DCW in Restricted Mode to the channel. If bit 18 is a zero, the list is unrestricted and Instruction DCW's will be allowed. (Bit 18 of the LPW for the connect channel must be set to zero by the software to preserve future compatibility and will be ignored by the IOM Central.) When the IOM Central encounters a Transfer DCW (TDCW) during a list service, it will at that time logically OR TDCW bit 34 into LPW bit 18 to provide the software with a way to switch immediately from unrestricted to restricted operation dynamically. Any subsequent encounter with an IDCW (Instruction DCW) will cause a user fault for that channel if the LPW bit 18 has been set to 1 by the TDCW. There will be no way to switch dynamically from restricted to unrestricted operation. Only replacing the LPW and issuing a CIOC for the restricted channel will restore the unrestricted operation. In addition, only unrestricted users may have TDCW 33 = 1 (i.e., change LPW 20). Note: An exception occurs during a Reverse List Service where LPW Bit 18 is unconditionally reset.

REL (LPW 19) - Reserved for storage of REL flag (bit 23) condition at the time an IDCW was fetched, or whenever a first-list service was performed.

AE (LPW 20) - Is defined as the Address Extension flag. This bit defines when a DCW list shall be located in the first 256K of core (LPW 20 = 0), or that it shall be in the 256K block specified via address extension (LPW 20 = 1). This bit may be changed from a zero to a one via a transfer type DCW, and will be reset to zero during a Reverse List Service if the system is an Extended GCOS system. In a Multics system this bit (if set) will follow the state of LPW bit 19. A system fault will be reported if LPW 20 = 1 in standard GCOS mode.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

NC - No Change (LPW 21) - Provides the software with a way to control the updating of the LPW (both address and tally fields) as shown in Table 3.2.1. When set to a one, bit 21 inhibits the updating of the address and tally fields of the LPW. It forces a PTRO to be indicated for a Connect Channel service regardless of the state of LPW bit 22.

TAL - Tally Indication Control (LPW 22) - Provides the software with a way to control the recognition of PTRO (Pre-Tally Run-Out) condition by all channels as shown in Table 3.2.1. When set to a one, bit 22 allows the recognition of PTRO and TRO; when zero, these conditions are not indicated, and a tally of zero will not cause a fault indication. For the connect channel, the combination TAL and NC = 0 will cause a system fault. This bit is overridden by LPW bit 21, NC.

REL (LPW 23) - Provides the software with a way to control the interpretation of DCW addresses for indirect channels by the IOM as absolute or relative. Depending on whether this bit is zero or one, each DCW address is treated as absolute or relative, respectively. The IOM Central converts relative addresses to absolute and checks them for boundary errors (see description of lower bound and size fields of LPW). Bit 23 of the LPW for the connect channel will be ignored by the IOM Central. When the IOM Central encounters a TDCW during a list service it will logically OR TDCW bit 35 into LPW bit 23 to provide software with a way to switch immediately from absolute to relative operation dynamically. On a reverse list service bit 19 of the LPW will replace bit 23. There will be no way to switch from relative to absolute operation except by a new LPW and connect (CIOC). For direct channels which use list service to obtain a DCW, no conversion of addresses in the DCW is possible; the program must provide absolute addresses, and LPW bit 23 should be zero for future compatibility.

B

Tally (LPW 24-35) - Defines the number of PCW's or DCW's remaining in the list. Updating of this field by the IOM Central is controlled by the NC, TAL, and the value of the tally, as shown in Table 3.2.1. When updating is called for, the IOM Central decrements this field by one during each list service. Upon detecting a TRO condition for a channel as defined in Table 3.2.1, the IOM Central will indicate a User Fault: LPW TRO to the channel. (A System Fault: LPW TRO will be indicated if the list service is for the connect channel.) The tally is decremented when a transfer DCW is encountered and is decremented again when the next DCW is pulled after the transfer has occurred.

The payload channel never gets a PTRO indication. It must determine when to stop requesting list service on the basis of information in DCW or on the basis of some external influence.

UPDATING OF LPW ADDRESS AND TALLY
AND INDICATION OF PTRO AND TRO

CASE	LPW 21 NC	LPW 22 TAL	TALLY VALUE*	UPDATE ADDRESS & TALLY	INDICATE PTRO TO CONNECT CHANNEL**	INDICATE TRO FAULT
a.	0	0	any	yes	no	no
b.	0	1	2 to 4095	yes	no	no
			1	yes	yes	no
			0	no	no	yes (fault)
c.	1	X	any	no	yes (forced)	no

Table 3.2.1

* before updating
** Note that this refers to connect channel list service.
X Indicates a "don't care" condition.

The anticipated uses of these cases is as follows: Case a. is expected to be used by GCOS for Common Peripheral interface payload channels; a tally of zero is not a fault since the tally field will not be used by GCOS for that purpose. Case b. is the configuration expected of standard operation with real-time applications, and/or direct data channels. Case c. will be used normally only with the connect channel servicing common Peripheral-type payload channels. If case a. is used with the Connect channels, a "System Fault:Tally Control Error, Connect Channel" will be generated. Case c. will be used in the Bootload program.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

Lower Bound (LPW Ext. 0-8 and Size (LPW Ext. 9-17) - Provide the software with a way of effectively setting up a base address register for each data channel. During a list service, if the REL bit (LPW 23) is one, the IOM Central checks the address and tally of the new DCW for possible boundary errors and, provided there is no boundary error, converts the relative address to an absolute address which is then placed in the DCW mailbox (or scratchpad). No checking or conversion is performed by the IOM Central if the REL bit is zero. B

Pointer to First DCW of Most Recent Instruction (LPW Ext. 18-35) - Will be updated by the IOM Central during the first list service after a PCW, and during any list service which encounters an Instruction DCW. Each time that this field is updated, the IOM Central will copy the DCW pointer field of the LPW (or the transfer DCW, if one is encountered) into this field of the LPW extension in core, and in scratchpad when available. Thus, if the most recent instruction was a PCW, this field will point to the first data DCW; if the most recent instruction was an Instruction DCW, this field will point to the Instruction DCW. It is possible for the software to determine how many instructions were executed by the IOM before an abnormal termination, by examining this field of the LPW extension in the core mailbox after termination. This field will be used as the DCW Pointer (LPW 0-17) on a reverse list service.

3.2.2 Peripheral Control Words (PCW)

The PCW is used by the Connect Channel to initiate the operation of a channel, or to mask (turn off) the operation of a channel that was previously initiated. The software can issue one or more PCW's with a single CIOC instruction by arranging the PCW's in a list and setting up an LPW for the Connect Channel to define the location and length of the list.

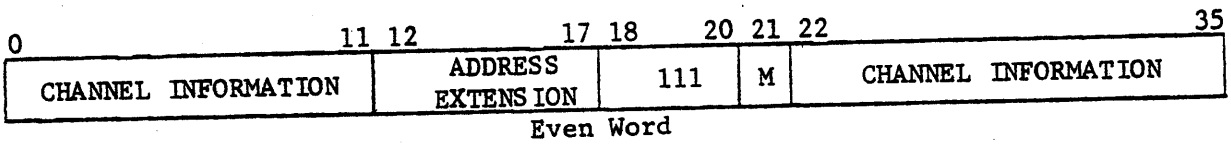
A non-PCW word (bits 18-20 not =111) encountered during a list service by the connect channel will cause a system fault. The PCW list should not contain more than one PCW for any one channel, unless the EPS-1 for that channel explicitly permits such operation.

Each PCW fills two words of core and must occupy a y-pair, that is, a pair of words obtained by a double-precision core access. A list of PCW's must occupy sequential y-pairs.

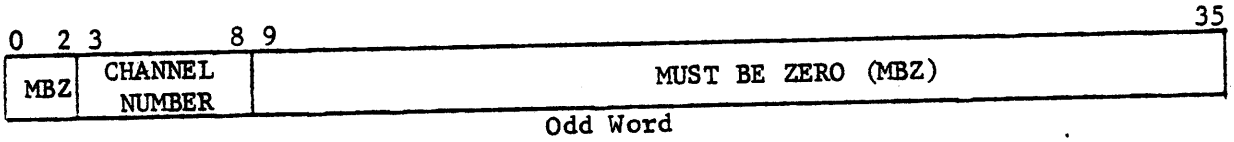
3.2.2 Peripheral Control Words (PCW) (continued)

The PCW for all payload channels has the format shown below. The PCW for the snapshot channel is shown in paragraph 3.8; the PCW for the wraparound channel is in 3.9.1; and the PCW for the scratchpad access channel in 3.11.

The software must be aware of the channel type and peripheral subsystem characteristics before writing more than one PCW for the same channel in the PCW list. In order to issue more than one command to the common peripheral channel for instance, subsequent commands must appear in the DCW list as IDCW's.



Even Word



Odd Word

All 36 bits of the even word of the PCW are sent to the channel whose channel number is specified in the Odd Word of the PCW. Bits 18-20 of the Even Word must be 111_2 or 7_8 to identify the word as a PCW.

Bits 12-17 contain the address extension which is maintained by the channel for subsequent use by the IOM in generating a 24-bit address for list or data services for the extended address modes.

A channel will change from the normal condition to a masked condition as a result of a System Initialize, a system fault flag from the IOM Central, or as a result of a PCW with bit 21 = 1. This masked condition is a state in which a channel will not request service in spite of a need for such service that may be generated in the channel. A channel will change from the masked condition to normal as a result of a PCW with bit 21 = 0.

3.2.2 Peripheral Control Words (PCW) (continued)

The interpretation of channel information fields (even word of the PCW) by the channels will be specified separately for each type of channel in the EPS-1 for that channel. In general, a channel uses the information for such things as device instruction, device code, or address, mask, channel instruction, record count, single character, storage address (direct channels), and peripheral storage address. The even word of the PCW is sent to the channel specified without rearrangement.

The odd word is used only by IOM Central, and is not sent to the channel. A 9-bit field is reserved for channel number, but only 6 bits are implemented. The six-bit channel number is extracted from the odd PCW word and is output to the channels on lines separate from those used to output the even PCW word. Bits 0, 1 and 2 must be zero, for future compatibility; these and bits 9-35 are not used by the IOM. B

3.2.3 Data Control Word (DCW)

The IOM Central recognizes five different types of DCW's. These are:

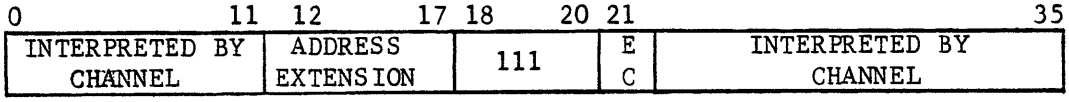
- Instruction DCW (IDCW)
- Transfer DCW (TDCW)
- I/O Transfer & Disconnect (IOTD)
- I/O Transfer & Proceed (IOTP)
- I/O Nontransfer & Proceed (IONTP)

The software or user program must generate appropriate DCW's for each data channel, and arrange the DCW's for each channel in a list. The list of DCW's for a channel must occupy sequential storage locations, except where one list is linked to another list by a TDCW. Boundary checks are made for DCW's (if REL bit = 1). Refer to paragraph 3.3 for a description of boundary checking.

3.2.3.1 Instruction DCW

The IDCW provides the software and unrestricted user programs with the ability to imbed instructions for peripheral devices at appropriate predetermined places in the DCW list.

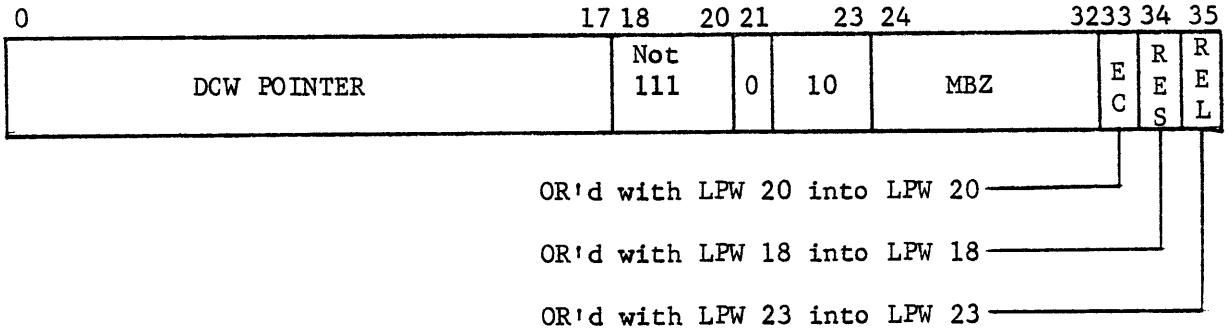
The format of the IDCW is similar to the format of the PCW. There is no counterpart in the IDCW for the PCW Odd Word (which specifies the number of the channel that is to receive the PCW).



The only field in the IDCW that is interpreted by the IOM Central is bits 18-20, which must be coded 111_2 or 7_8, to identify the DCW as an IDCW. When the IDCW is encountered during a list service, all 36 bits of the IDCW are sent to the data channel. If EC - Bit 21 = 1, the channel will replace the present address extension with the new address extension in bits 12-17. The address extension will be unaltered if EC - Bit 21 = 0. In Multics and NSA systems, EC - Bit 21 is inhibited from the payload channel if LPW bit 23 = 1. The interpretation of the remainder of the IDCW by the data channel will be specified separately for each type of channel in the EPS-1 for the channel. In general, a channel uses the information for such things as device instruction, channel instruction, record count, single character, core address (direct channels), and peripheral storage address.

3.2.3.2 Transfer DCW

The TDCW provides the software and the user with the ability to change control bits and to link one DCW list to another DCW list. The format of the TDCW is shown below. Bits 24-32 are not used by IOM Central.



DCW Pointer (0-17) - Specifies bits 6-23 of the address (absolute or relative, depending on the REL bit in the LPW) of the next DCW. The IOM Central absolutizes the address, if necessary, and places bits 6-23 of the absolute address in the DCW Pointer Field of the LPW, so that subsequent DCW's will be obtained from the new list. The most significant six bits (address extension) of the next DCW address are implied to be zero if LPW 20 = 0. If LPW 20 = 1, the address extension will be the present address extension held by the channel.

Bits 18-20 - Some code other than 111.

Bit 21 - Must be zero.

Bits 22-23 - Must coded 10_2 to identify the DCW as a TDCW.

Bits 24-32 - Must be zero.

Bit 33 - In All but STD GCOS Mode may be used to conditionally change LPW 20 from a zero to a one. That is, if TDCW 33 = 1 and if bit 18 of the present LPW is zero (unrestricted), LPW 20 will be set to a one. This will allow (system) software to control when the address extension bits from the PCW or IDCW will be used for accessing the users DCW list. Transfer DCW 33 = 1 and LPW 18 = 1 (restricted) is a user fault. In STD GCOS, if TDCW 33 = 1, LPW 20 will be set to a one and cause a system fault.

3.2.3.2 Transfer DCW (continued)

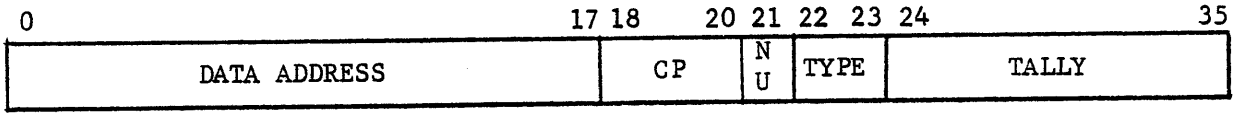
Bit 34 - Is logically ORed into LPW bit 18 by the IOM to provide the program with a way to switch from unrestricted to restricted operation.

Bit 35 - Is logically ORed into LPW bit 23 by the IOM to provide the program with a way to switch from absolute to relative operation.

A status of "User Fault:Two Sequential TDCW's" will be indicated to the channel and the I/O transaction will be aborted if the DCW Pointer field of a TDCW points to another TDCW. (See paragraph 4.5.)

3.2.3.3 I/O Transfer and Disconnect (IOTD)
I/O Transfer and Proceed (IOTP)
I/O Non-Transfer and Proceed (IONTP)

Each of these three types of DCW's defines a block of data in core which may be transferred. The DCW format is shown below.



Data Address (0-17) - Specifies the least significant 18 bits of the starting address of the block of data, and is treated as either absolute or relative, depending on the REL bit in the LPW. The address extension, Bits 0-5, is obtained from the channel and appended to form a 24-bit address. If the LPW REL bit is a one, the address is absolutized and tested for boundary errors. The data address field of an IONTP type of DCW is not used to access core, but is updated normally by the IOM Central.

3.2.3.3 I/O Transfer and Disconnect (IOTD)
I/O Transfer and Proceed (IOTP)
I/O Non-Transfer and Proceed (IONTP) (continued)

CP-Character Position (18 - 20) - Specifies the position of the first character within the first word of the block. The byte size, defined by the channel, determines what CP values are valid:

6 bit byte	000,001,010,011,100,101
9 bit byte	000,001,010,011
18 bit byte	000,001
36 bit byte	any except 111

For word channels which assemble bytes into words, or disassemble words into bytes, the CP field is sent from IOM Central to the channel during list service, and is zeros when placed in the DCW mailbox for subsequent data services for that channel. Only full words are tallied for word channels.

For sub-word channels (limited to 9-bit byte channels), which depend on IOM Central for packing and unpacking words, the IOM Central will increment the CP field each indirect data access until a word is filled or emptied (indicated by being inremented to a value greater than is shown above for that byte size). When this occurs, the CP field is restored to zero, and the address field in the DCW is incremented, then the DCW is replaced in the mailbox. A User Fault "Channel Character Size" will be indicated to the channel, if a character position value greater than those indicated above for that channel size is detected by IOM Central during list service. A CP value of 7_8 indicates an IDCW, and is valid for all channel sizes during a list service. It will cause a system fault during a data service.

NOTE: A character position value of 110_2 will be passed to the channel if the channel indicates that it is a word channel, (e.g., the IOM Central does not detect this as a fault). It is the responsibility of the channel to indicate a fault and the EPS-1 for the specific channel should be referenced.

3.2.3.3 I/O Transfer and Disconnect (IOTD)
I/O Transfer and Proceed (IOTP)
I/O Non-Transfer and Proceed (IONTP) (continued)

Mod 64 Bit (21) - Data DCW 21 was defined on the 655 IOM to be used, if a sub-word (character) channel were defined, to specify the manner of DCW tally update. That is, tally updating would be done once per word or once per character. For the 6000B IOM, tally will be on a word basis if a 9-bit character channel is ever defined. This bit is logically disabled from interrogation by the payload channels in the 6000B IOM.

Type (22-23) must be coded to identify the type of DCW.

00 IOTD I/O Transfer and Disconnect. The current device instruction is ended (terminated) when the channel detects the tally run-out condition of the tally.

01 IOTP I/O Transfer and Proceed. The current device instruction proceeds to a new DCW when the channel detects the tally run-out condition of the tally.

10 See Section 3.2.3.2 on Transfer DCW (TDCW).

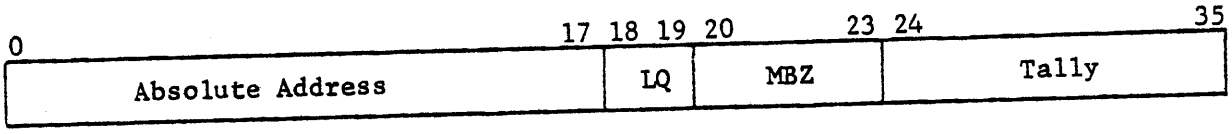
11 IONTP Same as IOTP except that no core accesses are made. If data is being read from a peripheral device, the block of data is discarded. If data is being written to a peripheral device, the IOM Central generates a block of zeros.

3.2.3.3 I/O Transfer and Disconnect (IOTD)
I/O Transfer and Proceed (IOTP)
I/O Non-Transfer and Proceed (IONTP) (continued)

Tally (24 - 35) - Defines the number of words in the data block. An initial tally of 0000_8 will be interpreted as 10000_8 or 4096_{10} by the IOM Central. When a 72 bit transfer takes place, the IOM Central must decrement the Word Tally by 2 each data service.

3.2.4 Status Control Word (SCW)

The SCW defines the location and length of a status queue in core storage. The status queue consists of a number of sequential y-pairs, into which the IOM will store status as status events occur. Since each channel has its own SCW, there is a separate status queue for each channel. The SCW has the format shown below.



Status Queue Address (0 - 17) - Provides the least significant 18 bits of the next absolute address of the status queue to be used by the IOM, or the starting address, as determined by the software. The IOM will append 6 zeros as the most significant address bits for all operating modes. The IOM Central will store status in the y-pair defined by the status queue address field. Consequently the software should insure that the status queue address is even. The IOM Central will increment the status queue address by two each time that status is stored in the queue, except when the tally is zero (before updating), or for a circular queue (see below).

List/Queue Control (18 - 19) - Will be interpreted for all modes as follows:

a) SCW (18 - 19) = 00 will result in the generation of a status list.

b) SCW (18 - 19) = 01 will result in the generation of a 4 entry (8 word) circular queue.

c) SCW (18 - 19) = 10 will result in the generation of a 16 entry (32 word) circular queue.

d) SCW (18 - 19) = 11 is reserved for future expansion and should not be used.

3.2.4 Status Control Word (SCW) (continued)

Circular queue addresses will be incremented after each entry until an entry is made in the queue tail. After the queue tail entry is made, the address will rotate back to the head of the queue.

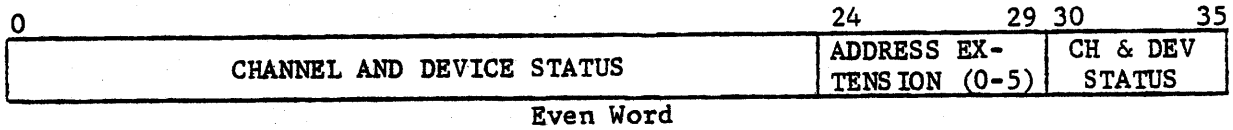
The tally of the SCW will be decremented for each status entry in either list or queue mode, but the suppression of address changes will not occur when the tally has been decremented to zero if circular status is called for.

Bits 20 - 23 are not used, and must be set to zero by the software. These bits are not examined by IOM Central.

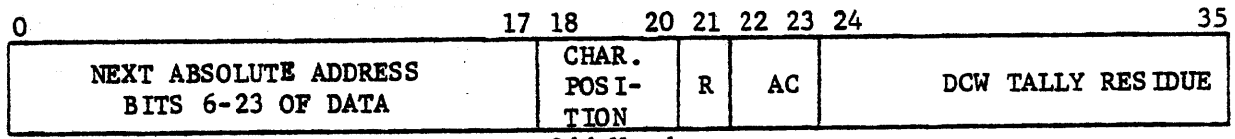
Tally (24 - 35) defines the number of unoccupied y-pairs (72-bits) in the status queue. The IOM Central will decrement the tally by one each time that status is stored in the queue, except when the tally is zero (before updating). As a result, if tally = N, the status queue actually consists of N + 1 y-pairs. The (N + 1)th y-pair corresponds to a tally of zero, and is therefore subject to being overlaid by subsequent status. SCW TRO is not a fault condition. In the circular queue mode the tally will continue to be decremented when it reaches zero.

3.2.5 Channel and Device Status Words

When the IOM Central performs a status service for a channel, it will store two words into the y-pair defined by the SCW for the channel. These two words will have the following format.



Even Word



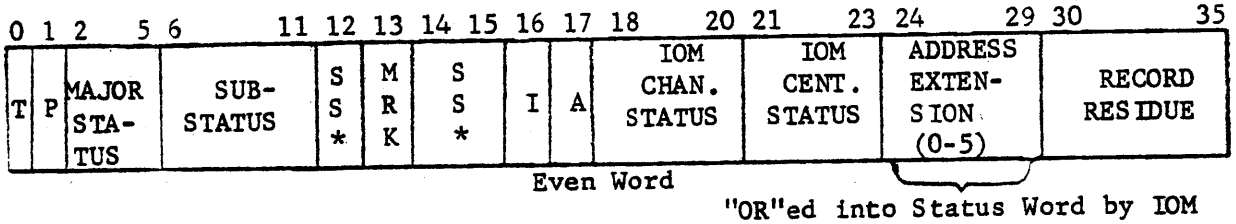
Odd Word

3.2.5 Channel and Device Status Words (continued)

EVEN WORD:

Channel and Device Status (0 - 35) will be generated by the channel and sent to the IOM Central during the status service. The IOM Central will obtain the address extension bits from the channel's Transaction Command (for status service), and will "OR" them into bits 24-29 of the status word supplied by the channel; therefore, the channel must insure that bits 24-29 of the even status word are zero. The IOM Central will store the channel and device status word in the even word of the y-pair defined by the Status Control Word.

The Common Peripheral Channel Status is shown for illustrative purposes only and reference should be made to the EPS-1 for the Common Peripheral Channel for explanation of the fields shown.



*SS = Software Status

ODD WORD:

The IOM Central will obtain the DCW for the channel (from the core mailbox or from the scratchpad, as appropriate) and store this DCW residue in the odd word of the y-pair defined by the SCW. The information in the DCW residue (as a result of updating by the IOM Central during data services) must meet the following requirements so that it can be properly interpreted by software.

3.2.5 Channel and Device Status Words (continued)

Next Absolute Address (0 - 17) contains bits 6 - 23 of the absolute address of the word which would have been read or written next had the transaction continued.

Character Postion (18 - 20) is the character number into which or from which the next character of data would have been transmitted if the transaction had continued. (Word channels will always fill out a word with zeros and store a whole word if the transaction stops while reading at a character count other than zero, but the last actual character position + 1 will be indicated in this field.) The IOM Central will obtain the character count residue from the channel during a status service, and logically OR it into the DCW residue word before storing it as status.

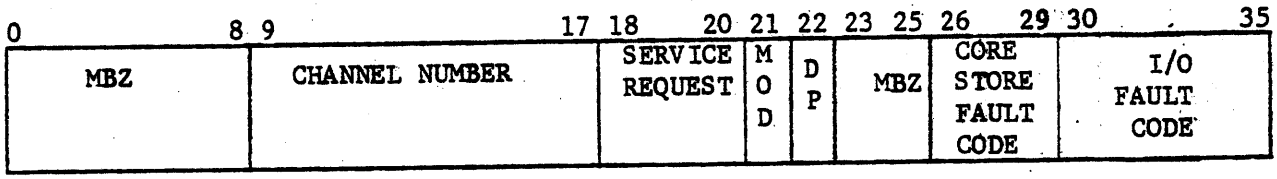
Read (21) will be a one if a peripheral read (core write) operation was to be performed. Otherwise it will be zero. The IOM Central will obtain the read bit from the channel during a status service, and place it into the DCW residue word before storing it as status.

Action Code (22 - 23) is the Action Code of the last DCW obtained for this channel.

Tally Residue (24 - 35) is the residue of the DCW tally, representing the number of words which were not accessed.

3.2.6 System Fault Word

A system fault word is stored as data by the system fault channel at the location indicated in the fault channel DCW mailbox when a system fault is detected by the IOM Central. The system fault word has the following format:



Channel Number (9 - 17) indicates the channel that was being serviced when the system fault was detected.

3.2.6 System Fault Word (continued)

Service Request (18 - 20), MOD (21) and DP (22) indicate the type of operation that was being performed for the specified channel when the system fault occurred. The following table lists the interpretation of these bits.

SR 0 (18)	SR 1 (19)	SR 2 (20)	MOD (21)	DP (22)	
0	0	0	X	X	INV - Invalid
0	0	1	1	0	LST - List Service, "FIRST"
0	0	1	0	X	LST - List Service, "SECOND"
0	0	1	1	1	LST - List Service, "BACK-UP"
0	1	0	X	X	STA - Status Service
0	1	1	X	X	PI - Program Interrupt Service
1	0	0	0	0	ILD - Indirect Data Load Service, Single Precision
1	0	0	0	1	ILD - Indirect Data Load Service, Double Precision
1	0	1	0	0	IST - Indirect Data Store Service, Single Precision
1	0	1	0	1	IST - Indirect Data Store Service, Double Precision
1	1	0	0	0	DLD - Direct Data Load Service, Single Precision
1	1	0	0	1	DLD - Direct Data Load Service, Double Precision
1	1	0	1	0	DRC - Direct Read Clear Service
1	1	1	0	0	DST - Direct Data Store Service, Single Precision
1	1	1	0	1	DST - Direct Data Store Service, Double Precision

Table 3.2.6

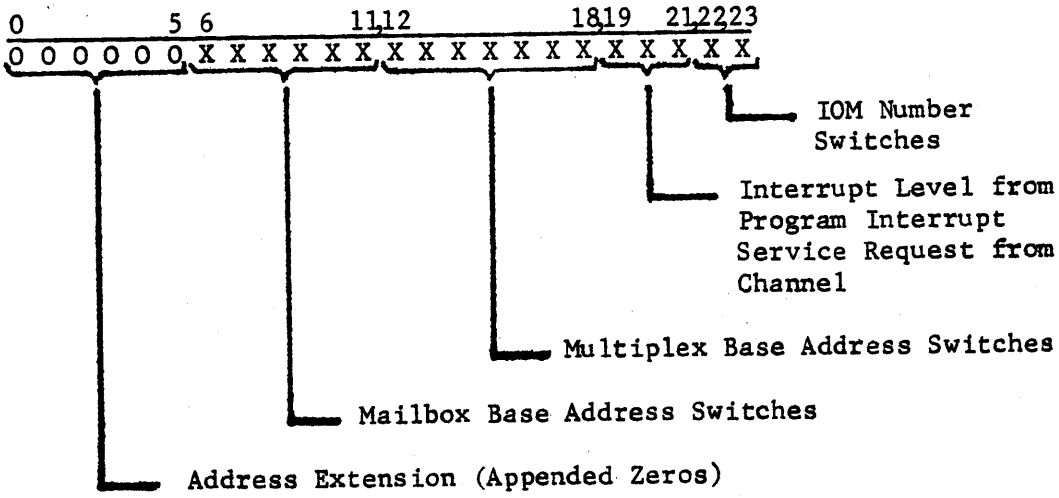
Store Fault Code (26 - 29) indicates the particular type of store fault. (Codes defined in paragraph 4.5.)

I/O Fault Code (30 - 35) indicates the particular type of I/O fault. (Codes defined in paragraph 4.5.)

3.2.7 Interrupt Multiplex Word (IMW)

The IOM has the ability to set any of the 32 program interrupt cells located in the system controller containing the base address of the IOM. It should be noted however that for any given IOM identity switch setting, the IOM can set only 8 of these program interrupt cells. The use of this interrupt provision is restricted by system assignment of program interrupt cells. The IOM uses the 32 interrupt cells in conjunction with the 32 core locations in the IOM mailbox area to establish a channel's identity. There is a one-to-one correspondence in address between the program interrupt cells and the IMW words.

The IOM Central pulls the IMW from the core location having the address determined as follows:



One IMW is provided for each program interrupt cell which can be set by the IOM Central. The particular one of the 32 words in the IMW area, and the interrupt cell in the System Controller, are determined by two factors:

a) The IOM number, as set by the IOM number switches on the maintenance panel, will determine the two least significant bits of the IMW address. This provides one word for each of four possible IOM's at each of eight interrupt levels. The switches are further described in paragraph 3.5.2.

b) The interrupt level as determined by the logic in each channel. The channel will wire, patch, or logically manipulate bit positions 13-15 of the data presented with a program interrupt service request, providing as many as eight possible interrupt levels for each channel from the total of 32 levels. Note that this interrupt level becomes bits 19-21 of the IMW address once the IOM has appended an address extension of zeros.

3.2.7 Interrupt Multiplex Word (IMW) (continued)

Thirty-two of the 36 bit positions are used in each of the 32 IMW words to indicate which channel caused the program interrupt. The appropriate IMW is pulled with a Read-Clear access cycle, a "one" is ORed into the IMW in the bit position specified by the channel, and then the IMW is returned to core with a Clear-Write cycle.

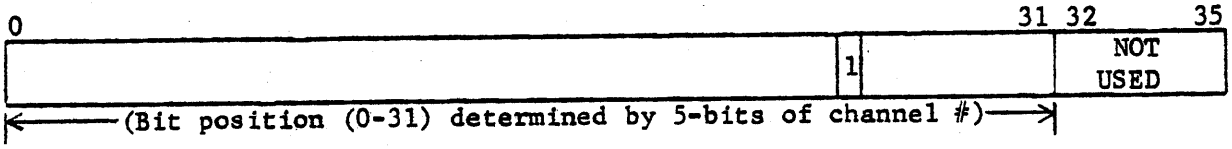
The IOM Central then sets the program interrupt cell that was specified by the channel.

The bit position within the IMW which is to be set to a one is determined by the binary value of the five least significant bits in the channel number field of the program interrupt service request presented by the channel. In the event that more than 32 channels are used on a single IOM, the higher numbered channels will be required to use a different program interrupt level.

Any special purpose channels designed in the future with a requirement to set bits in some IMW which do not correspond to its own channel number, may still logically manipulate bits 22 - 26 on one or more Program Interrupt requests, to set any of 32 bits in any of 8 words in the IMW area.

Upon interruption, the supervisory program may examine the core location corresponding to the interrupt cell causing the interrupt to determine which of the channels caused the interrupt. The floating normalize instruction may be used effectively for this purpose.

Any program interrupt cell may still be used as a discrete interrupt by some special purpose channel in which case the program would not need to consult the table. Figure 3.2.7 depicts the relationship between the interrupt cell number, IOM channels and the multiplex queue.



INTERRUPT MULTIPLEX WORD

3.2.7 Interrupt Multiplex Word (IMW) (continued)

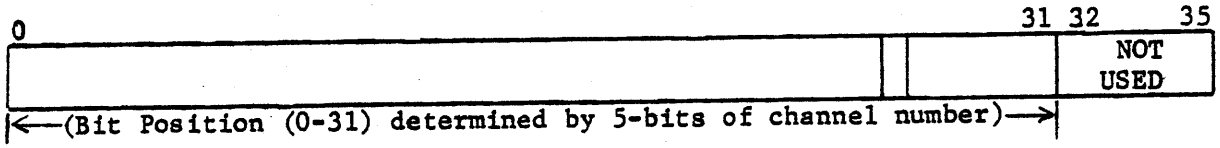
Note:

It is important that the system programmer realize that the Interrupt Multiplex Word (IMW) update by the IOM requires 2 cycles, a Read - CLear (RCL) followed by a Clear - WRite (CWR). That is, the process of determining which channel caused an interrupt is similar to the gating function. The software must interrogate the IMW with an instruction that causes the RCL cycle and transfers the information to the processor (e.g. LDAC, LDQC). There is no other instruction that can provide this capability without the possibility of losing information. This hardware technique implies that the software may find an IMW of "zero" when responding to an interrupt. (i.e. the IOM has performed the RCL and has yet to perform the CWR.) If the software does find an IMW (at the appropriate level) of "zero" it must read it again (via the RCL). This process of repeated fetching should not be an arbitrary loop - but rather a procedure that would detect a failure should the IOM not perform the CWR cycle.

When the software fetches the IMW, it may have an indication of more than one channel interrupt. It is interesting to note that after the software processes these interrupts (if any) an interrupt present signal may still be present. That means that when the waiting interrupt is processed, the interrupt handler may find a legitimate "zero" value IMW. This situation should not be interpreted as an IOM error but rather the interrupt should be effectively ignored by the software.

MAP OF IMW AREA

DEC.	OCT.	IOM NO.	LEVEL	
0	00	0	0	
1	01	1	0	
2	02	2	0	
3	03	3	0	
4	04	0	1	Interrupts for overhead channels in IOM Number 0
5	05	1	1	Interrupts for overhead channels in IOM Number 1
6	06	2	1	Interrupts for overhead channels in IOM Number 2
7	07	3	1	Interrupts for overhead channels in IOM Number 3
8	10	0	2	
9	11	1	2	
10	12	2	2	
11	13	3	2	
12	14	0	3	Terminate Interrupts for Data channels in IOM No. 0
13	15	1	3	Terminate Interrupts for Data channels in IOM No. 1
14	16	2	3	Terminate Interrupts for Data channels in IOM No. 2
15	17	3	3	Terminate Interrupts for Data channels in IOM No. 3
16	20	0	4	
17	21	1	4	
18	22	2	4	
19	23	3	4	
20	24	0	5	Marker Interrupts for Data channels in IOM Number 0
21	25	1	5	Marker Interrupts for Data channels in IOM Number 1
22	26	2	5	Marker Interrupts for Data channels in IOM Number 2
23	27	3	5	Marker Interrupts for Data channels in IOM Number 3
24	30	0	6	
25	31	1	6	
26	32	2	6	
27	33	3	6	
28	34	0	7	Special Interrupts for Data channels in IOM Number 0
29	35	1	7	Special Interrupts for Data channels in IOM Number 1
30	36	2	7	Special Interrupts for Data channels in IOM Number 2
31	37	3	7	Special Interrupts for Data channels in IOM Number 3



INTERRUPT MULTIPLEX WORD

Figure 3.2.7

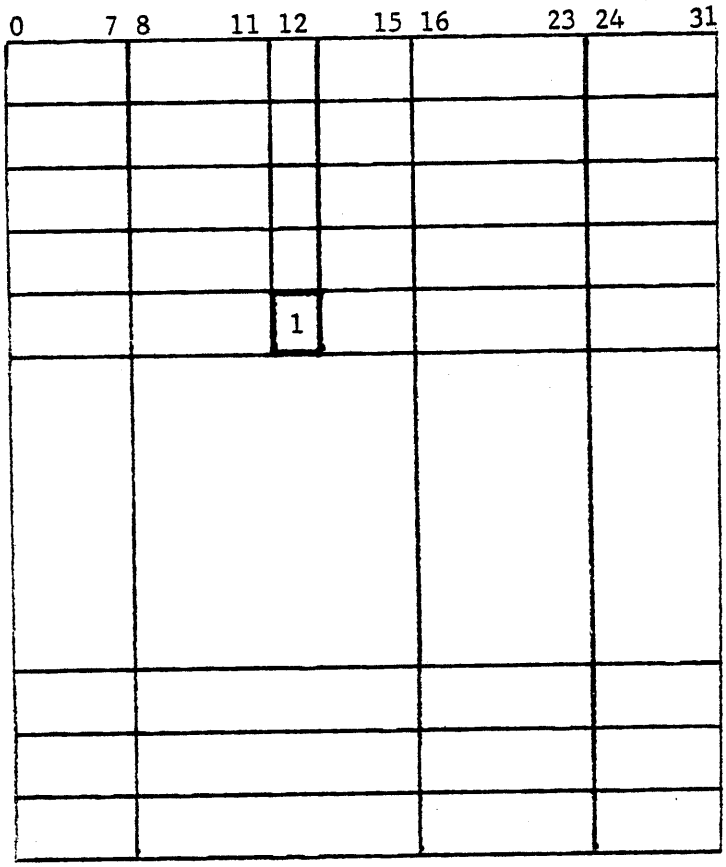
3.2.7 Interrupt Multiplex Word (IMW) (continued)

Example: (all numbers are in decimal)

Cell 17 is used as a multiplexed cell. Channel 12 uses cell 17 and shares it with other channels. When channel 12 issues the interrupt instruction, the IOM Central reads location 017, then alters it by setting a "one" in the bit 12 position, then re-writes it back into core, altering only bit 12. Next the IOM will actually set interrupt cell 17. The supervisory program, when servicing the interrupt, consults location 017 to determine which channel has set the cell.

Interrupt Cell Number	Address Relative to Start of the IOM Multiplex Base
0	000
1	001
2	002
•	•
17	017
•	•
•	•
•	•
•	•
•	•
29	029
30	030
31	031

Multiplex Interrupt Bit Numbers Correspond to IOM Channels



3.3 BOUNDARY CHECKING

3.3.1 Notation

The following notation will be used to define boundary checking and address conversion:

A = initial DCW address (relative)

S = the number of 512-word blocks addressable by the program; (size) - S is relative to the Lower Bound; i.e., the number of 512 word blocks "starts" at the Lower Bound.

T = initial DCW tally = DCW (24-35)

Note: If T = 0000_8 it must be treated as 10000_8 by the IOM Central in the boundary check.

LB = Lower Bound = LPW Ext. (0-8) = Upper 9 bits of 18 bit address

3.3.2 Check Performed

1) A User Fault:Boundary Error will be indicated if

$$S + LB - 2^9 > 0$$

2) A User Fault:Boundary Error will be indicated if:

for IOTD, IOTP, IONTP;

$S \times 2^9 - A - T < 0$ or for TDCW $S \times 2^9 - A \leq 0$

Note: Unlike the 6000 IOM which interpreted size = 0 as a User Fault, the 6000B IOM will interpret size = 0 as the specifier for 256K (512 consecutive blocks of 512 words each). The only valid lower bound for size 0 is an LB of zero.

3.3.3 Address Result

If a User Fault does not occur, then the lower 18 bits of the absolute address will be:

$$\sum_{N=0}^{8} \left[(\text{LPW Ext. (N)} + \text{DCW (N)}) \times 2^{17-N}\right] + \sum_{N=9}^{17} \left[\text{DCW(N)} \times 2^{17-N}\right]$$

3.4 CHANNEL NUMBERING

The channel number is a 9-bit binary number, usually expressed as a 3-digit octal number, which identifies a specific channel for both the hardware and the software. Each channel has provision for defining its channel number by a patch arrangement in the channel. Only the 6 low-order bits of the channel number are to be implemented. The high order 3 bits must be zero for upward compatibility.

Channel numbers are used for the following purposes in the IOM:

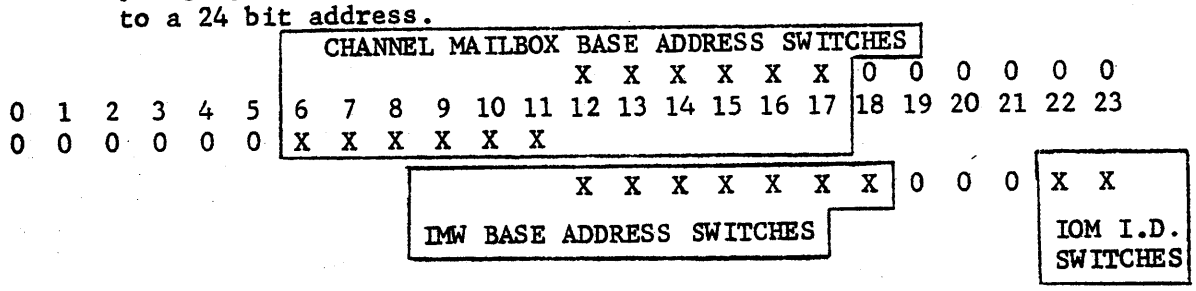
- A channel recognizes that a PCW is intended for it on the basis of channel number;
- The IOM Central uses the channel number supplied by the channel to determine the location of control word mailboxes in core store or in scratchpad;
- The IOM Central places the channel number in the system fault word when a system fault is detected and indicated, so that the software will know which channel was affected.
- The IOM Central uses the channel number to set a bit in the IMW (see 3.2.7)

Channel numbers 010_8 - 077_8 may be assigned to payload channels, and channel numbers 000_8 - 007_8 are reserved for assignment to overhead channels:

Channel No.	Overhead Channel Assigned
0	Illegal use - not assigned
1	Fault Channel
2	Connect Channel
3	Snapshot Channel
4	Wraparound Channel
5	Bootload Channel
6	Special Status Channel
7	Scratchpad Access Channel

3.5 MAILBOXES AND STORE MAP

Communication between software and the IOM depends on an understanding of where control words, such as the LPW, SCW, and IMW, are located in storage. To facilitate this, two related base addresses are defined by switches on the IOM configuration panel. These switches are indicated by X in the diagram below which illustrates the relationship between the sets of switches. The paragraphs which follow describe the use of the switches relative to a 24 bit address.



3.5 MAILBOXES AND STORE MAP (continued)

A map of the mailbox area, starting at the Channel Mailbox Base Address, is shown in the following diagram. (U = Unused)

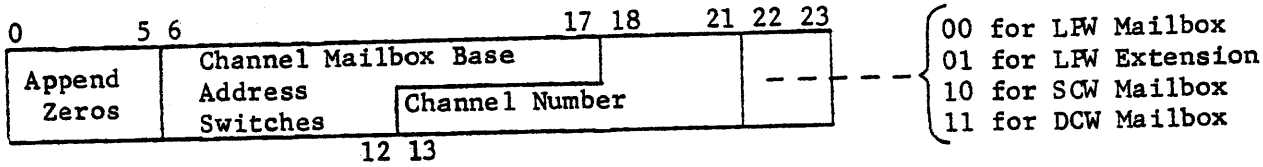
Address		Chan. No.	Chan. Name	Mailbox
Channel Mailbox Base Address	0	0	(Illegal	U (Unused)
plus	1	0	Channel	U
	2	0	Number)	U
	3	0		U
	4	1	Fault	LPW
	5	1		U
	6	1		U
	7	1		DCW
	8	2	Connect	LPW
	9	2		U
	10	2		U
	11	2		U
	12	3	Snapshot	U
	13	3		U
	14	3		U
	15	3		DCW
	16	4	Wraparound	U
	17	4		U
	18	4		SCU
	19	4		U
	20	5	Bootload	U
	21	5		U
	22	5		U
	23	5		U
	24	6	Special	LPW
	25	6	Status	U
	26	6		U
	27	6		DCW
	28	7	Scratchpad	U
	29	7	Access	U
	30	7		U
	31	7		DCW
	32	10	Payload	LPW
	33	10	Payload	LPWX (Ext.)
	34	10	Payload	SCW
	35	10	Payload	DCW
	36	11	Payload	LPW
	37	11	Payload	LPWX
	38	11	Payload	SCW
	29	11	Payload	DCW
	252	077	Payload	LPW
	253	077	Payload	LPWX
	254	077	Payload	SCW
	255	077	Payload	DCW

Note: The present hardware limits the channel number to 77_8 and the maximum mailbox address to the Channel Mailbox Base Address + 255.

3.5.1 Channel Mailbox Base Address Switches

These 12 switches provide bits 6-17 of the channel mailbox base address. The address extension, bits 0-5, and bits 18-23 of this base address are zero.

The following diagram shows how the absolute address of mailbox words are determined



The channel mailbox base address switches are ORed with the channel number. Therefore to avoid ambiguity when channel numbers greater than 15 are used, some of the low order bits of the channel mailbox base address may be required to be zero.

3.5.2 Interrupt Multiplex Base Address Switches

Fifteen switches provide bits 6-18, 22, and 23 of the address for one of the 32 Interrupt Multiplex words described in paragraph 3.2.7. Bits 19-21 of this address are provided by the channel, as the interrupt level, in the Interrupt Service request. Bits 6-11 of the Interrupt Multiplex Base Address are set by the same switches as bits 6-11 of the Channel Mailbox base address. The address extension, bits 0-5, are zeros.

The switches which provide bits 22 and 23, the two least significant bits of the address, are labeled "IOM Number". These two switches, and the 3 bits of interrupt level supplied by the channel, select one of the 32 Interrupt cells, and one of the Interrupt Multiplex Words relative to the IMW base address.

IOM's will be configured on a system according to the following table:

Configuration Order	IOM Number
First IOM	0 (00)
Second IOM	1 (01)
Third IOM	2 (10)
Fourth IOM	3 (11)

3.6 SYSTEM FAULT CHANNEL

The system fault channel controls the indication to the software of system faults that are detected by the IOM.

Once it has been activated by the detection of a system fault, the system fault channel obtains an indirect data service from the IOM Central. During this indirect data service the system fault word is transferred from the fault channel to core under control of the DCW for the system fault channel. (Note: the DCW is used in preference to the SCW to allow recording of system faults on a most recent n, rather than first n-1 and most recent one basis - see below.) The system fault channel operates in the indirect-36 mode. The system fault channel is the top priority channel, and will be wired as number 001_8.

Immediately after the data service has been completed, without relinquishing control, the system fault channel obtains a program interrupt service using level one (without storing status), does a list service if necessary and then de-activates itself, waiting for another possible system fault.

The software determined tally of the fault channel DCW should be sufficient to allow for several faults occurring in succession. When this number is exceeded and the tally reaches zero, the fault channel will request a list service before completing the program interrupt service. The software determined LPW obtained during this service could point to a DCW which will overlay the original fault channel DCW and should have the same initial address and tally. (NC = 1 in original LPW.) Thus the fixed size queue (n words) will cycle and have, at most, the last n fault words.

The LPW extension and SCW mailboxes for the system fault channel are not used by the IOM.

3.7 CONNECT CHANNEL

The connect channel controls the distribution of instructions which initiate the operation of data channels. The connect channel is activated when a $CON signal is received from a system controller by the IOM Central, as a result of a processor executing a CIOC instruction or when a $CON is received from the bootload channel.

Once it has been activated the connect channel obtains a list service from the IOM Central. During this service the IOM Central will do a double precision read from core, under the control of the LPW for the connect channel.

If the IOM Central does not indicate a PTRO during the list service, the connect channel obtains another list service. When the PTRO is indicated, the connect channel de-activates itself, waiting for another $CON. The connect channel does not interrupt or store status.

The channel number of the connect channel will be wired as 002_8.

The DCW and SCW mailboxes for the connect channel are not used by the IOM.

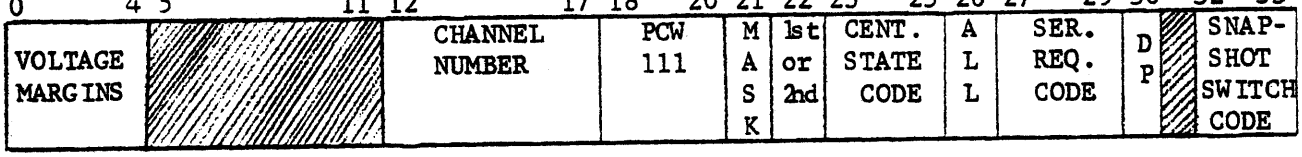
3.8 SNAPSHOT CHANNEL

The snapshot channel provides the test and diagnostic software with a way of sampling control lines and signals in the IOM Central at times specified by the software. The snapshot channel is activated by a PCW addressed to it.

The PCW defines the state of the IOM Central at which the snapshot is to occur. This includes such factors as the channel number of the channel being serviced, and the type of service, as well as the control state of the IOM Central. When the snapshot conditions are met, the specified information is switched into the snapshot register and then stored in core as data, under control of the DCW for the snapshot channel. Sampling continues until a PTRO condition is indicated by the IOM Central. When the PTRO is indicated, the snapshot channel obtains a program interrupt service using level one (without storing status) and then de-activates itself waiting for another PCW.

The Snapshot Channel is wired as channel number 3. The LPW, LPW extension and SCW in the mailbox area for the Snapshot Channel are not used.

The even word of the PCW for the Snapshot Channel has the following format:



Explanation of PCW fields: (See note below)

0-4	Voltage Margin Control
5-11,31	These bits must be zero.
12-17	Channel number of channel that is to be in operation when the information is strobed into the Snapshot Register.
18-20	These bits are 111 for a PCW.
21	This bit will mask the snapshot channel if set to "1".
22	If this bit is "0", the Snapshot Register will be strobed the first time the central is in the state requested. If the bit is a "1", the strobe will occur the second time the central is in the requested state.

3.8 SNAPSHOT CHANNEL (continued)

This will be useful during a list service when the IOM Central is in the Indirect Cycle Read (ICR) state for two (2) storage access cycles, for example.

23-25 State Code of the IOM Central during which the Snapshot Register is to be strobed. These codes are defined as follows:

Code 23	24	25	Central State Referenced
0	0	0	IDLE
0	0	1	CWP Instruction Word Pull
0	1	0	ICR Indirect Cycle Read
0	1	1	ICW Indirect Cycle Write
1	0	0	RCW Restore Control Word
1	0	1	SXC Set Interrupt Cell
1	1	0	DIR-R Direct Read
1	1	1	DIR-W Direct Write

26 If this bit is a "1", the Snapshot Register is strobed during each Service Request of the desired channel. The Snapshot Channel must then have a higher priority than the channel observed. Therefore with bit 26 set, inspection of the fault channel will be somewhat restricted.

27-29 Service Request Code during which the Snapshot Register is to be strobed. These codes are defined in paragraph A.2.1.

30 If this bit is a "1", the Snapshot Register will be strobed only when the desired channel requests a Double Precision Cycle of the Service Request Code indicated in bits 26-29 above.

32-35 The Snapshot Switch Code designates which Central register or data path is to be enabled onto the Snapshot Bus. The code and contents of the Snapshot Switch which are referenced are defined as follows:

3.8 SNAPSHOT CHANNEL (continued)

32-35 (continued)

Code 32-35	Area of IOM Referenced
0000	Data bus from stores (DR bus 00-35)
0001	Data bus from stores (DR bus 36-71)
0010	Control word reg. 00-35 (C reg. 00-35)
0011	Control word Incrementer/Decrementer (C_{ADD} 00-17, C_{DEC} 24/35)
0100	Control word reg. 36-71 (C reg. 36-71)
0101	Data from stores register switch (H Sw. 00-35)
0110	I/O bus input from channels (S Bus 00-35)
0111	Service request register (T reg. 00-35)
1000	Data Register, from I/O bus from channels (D reg. 00-35)
1001	Data bus to store (DT bus 00-35)
1010	Data bus to store (DT bus 36-71)
1011	Zone, address, and command (ZAC)
1100	Channel number register and misc. control signals to be defined in EPS-2
1101	Not used
1110	Not used
1111	Not used

3.9 WRAPAROUND CHANNEL (WAC)

The wraparound channel provides the test and diagnostic software with a way of causing the IOM Central to perform specific types of service on behalf of a specific channel, designated by the T&D software. The wraparound channel is activated by receipt of a PCW addressed to it, and assumes the identity of the channel number contained in the PCW.

By appropriate coding of the PCW the following operations can be caused to happen:

- Load data into the data register of the wraparound channel.
- Perform list service (or first list service) in lieu of a specified channel.
- Perform status service in lieu of a specified channel.
- Perform program interrupt service using specified program interrupt cell and multiplex bit number.
- Perform indirect data load or store in lieu of a specified channel.
- Perform direct load or store using specified storage location.
- Perform direct read clear using specified storage location.
- Load specified status into status register of the wraparound channel.
- Cause a system fault, or a user fault.

After performing the action specified by the PCW, the wraparound channel de-activates itself, waiting for another PCW. There is no automatic storage of status and no automatic program interrupt associated with the operation of the wraparound channel.

At the end of each service by the Wraparound Channel, I/O bus control and flag lines are loaded into the wraparound status register. A PCW specifying a status service for the wraparound channel will return this information to core, using the SCW for the channel specified in the PCW, probably the SCW for the WAC channel.

The wraparound channel will be wired as channel number 004_8.

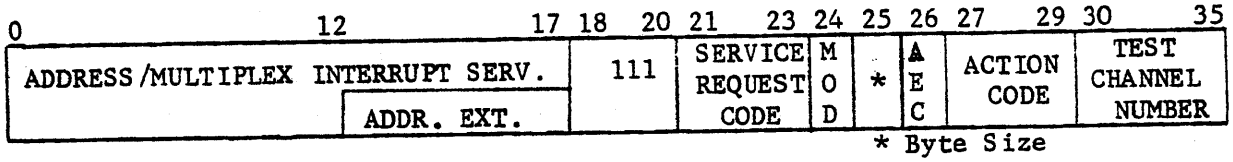
The mailbox area is not used automatically; the SCW should be used when accessing the status information stored in the WAC hardware.

The Wraparound Channel utilizes four word formats:

1) Peripheral Control Word (36 bits)
2) Data Word, Single Precision (36 bits + parity)
3) Data Word, Double Precision (72 bits + 2 parity)
4) Status Word (36 bits)

3.9.1 Peripheral Control Word (PCW)

The even word of the PCW for the Wraparound Channel has the following format (the odd word addresses channel 004_8):



The PCW fields are described as follows:

0-17 Contains bits 6-23 of the absolute store address for direct data service. Bits 12-17 will be used as address bits 0-5 if bit 26 equals a "1". This field also can contain the Program Interrupt Cell for a Multiplex Program Interrupt Service in bits 13-15.

18-20 Always 111 for a PCW.

21-23 Service Request Code which determines the type of service of an action PCW. These codes are defined as follows:

000	Invalid
001	List Service
010	Status Service
011	Interrupt Service
100	Indirect Data Load Service
101	Indirect Data Store Service
110	Direct Data Load Service
111	Direct Data Store Service

24 Mod bit - when equal to 1 indicates the first list service, or read clear for direct data load single precision.

25 Byte size - determines the byte size during an indirect data service.

0 = 9 bit byte

1 = 36 bit byte

26 Address Extension Control - determines if address extension bits 12-17 will be outputted with transaction command.

3.9.1 Peripheral Control Word (PCW) (Continued)

27 - 29 Action Code - determines operation of the Wraparound Channels as to what action will be performed due to the PCW.

000 = single precision action PCW for data register #1 (Note 1)
001 = single precision action PCW for data register #2 (Note 1)
010 = double precision action PCW (Note 1)
011 = force an I/O bus parity error on an indirect data store service
100 = Data PCW for Data Register #1 (Note 2)
101 = Data PCW for Data Register #2 (Note 2)
110 = Data PCW for the Status Register (Note 2)
111 = Load the I/O bus control flags into the Status Register during the PCW. No change to the instruction or Data Register, and no request is made to Central.

30 - 35 Test Channel Number - determines the payload channels for which a particular service is being performed.

Note 1: The action PCW is a PCW which causes the Wraparound Channel to perform a specified service, i.e., list, status, etc.

Note 2: The Data PCW is a PCW which causes the data contained in the PCW to be stored in either of two data registers or a status register, depending on the action code. The Wraparound Channel will not make any request to the IOM Central when this type of PCW is received.

3.9.2 Data Word

The Data Registers of the Wraparound Channel are loaded from all 36 bits of the input data lines by either a data PCW, in which the data of the PCW is loaded into the data register, or when a direct/indirect load service is specified in an action PCW. The input parity is also loaded.

The contents of the Data Registers are stored in core when a direct/indirect data store service is specified in an action PCW.

3.9.3 Status Word

The Wraparound Channel Status Register is loaded from the input data lines when the Wraparound Channel receives a data PCW specifying the Status Register. The Status Register is also loaded with the I/O Bus Control points and flags at the end of each service that the Wraparound Channel performs as a result of an action PCW. The bus will also be loaded if the Wraparound Channel receives a PCW with an action code of 111.

The Status Word is stored in core when a Status Service is specified in an action PCW. The format of the Status Word in the Wraparound Channel is then one of the following:

0	8,9	23 24	29,30	35
PCW DATA	ZEROS	ADDRESS EXTENSION (0 - 5)	PCW DATA	

or

0	8,9	23 24	29,30	35
I/O BUS SIGNALS	ZEROS	ADDRESS EXTENSION (0 - 5)	TEST CHAN. NUMBER	

In the second case, the fields are designated as follows:

Bit 0 = SCN
1 = DTA
2 = DBL
3 = TLO
4 = TL1
5 = SYS
6 = US0
7 = US1
8 = US2

30-35 = Test channel number which was received with the last action PCW (with the exception of the Status Service Request).

Note: Bit 9 through 23 are not implemented and will always be returned to core as zeros for a status return.

Bits 24 - 29 are "OR'ed" in by the IOM Central from the address extension bits in the transaction command.

3.10 BOOTLOAD CHANNEL

The bootload channel will consist of 11 words of read only storage/ IOM configuration switches. It will be placed into operation when the BOOTLOAD pushbutton at either the System console or the bootload section of the Configuration Panel is depressed.

When the bootload channel is placed into operation, it will cause the 11 words to be written into core storage and will activate the connect channel in the same manner as a $CON signal from the system controller. The connect channel will cause a PCW to be sent to the channel specified as the boot channel by the configuration switches and will initiate transfer of one record from that channel.

The following configuration switches from the IOM configuration panel will be accessible to the bootload channel so that the settings of these switches can be stored by the bootload channel as part of the bootload program (see Figure 3.10a):

- Port (the number of the system controller port to which the IOM is connected)
- IOM Mailbox Base Address
- IOM Interrupt Multiplex Base Address
- IOM Number...0, 1, 2, or 3
- Card/Tape Selector
- Mag Tape Channel Number
- Card Reader Channel Number

The 6000B boot program shall work on either a CPI or PSI channel. It has the following characteristics:

1. The program is highly dependent on the configuration panel switches.
2. The program performs the following functions:
   a. The system fault vector, terminate fault vector, boot device's SCW and the system fault channel's (status) DCW are set up to stop the program if the BOOT is unsuccessful (device offline, system fault, etc.) and to indicate why it failed.
   b. The connect channel LPW and the boot channel LPW and DCW are set up to read (binary) the first record starting at location 30_8. This will overlay the terminate interrupt vector and thereby cause the processor to start executing the code from the first record upon receipt of the terminate from reading that record.
3. The connect channel PCW is treated differently by the CPI channel and the PSI channel. The CPI channel does a store status. The PSI channel goes into startup.

3.10 BOOTLOAD CHANNEL (continued)

The bootload channel is assigned a channel number of 5, but will not respond to PCW's directed to channel 5. Operation of the bootload channel will be initiated only by an operator depressing the BOOTLOAD pushbutton on the IOM configuration panel or on the system console (after first depressing the System Initialize pushbutton). The bootload channel will make no use of the mailbox words set aside for channel 5.

The reading of the first record of magnetic tape or card without processor intervention facilitates primitive instruction testing by T&D software, without requiring a (possibly) sick processor to actively initiate its own testing.

Figures 3.10a and 3.10b respectively show which configuration panel switches are used in BOOTing, what the boot program looks like.

Octets	Function/Switches	Range
BB	Bootload Channel Number	10_8 - 77_8
C	Command/based on Bootload Source Switch	1_8 or 5_8
N	IOM Number	0_8 - 3_8
P	Port Number	0_8 - 3_8
XXXX00	Base Address	000000_8 - 777700_8
XXYYY0	Program Interrupt Base (First 6 bits same as Base Address)	000000_8 - 777740_8

Figure 3.10a

Bootload Program Fields Supplied by Configuration Switches

Word	Address	Data	Location	Purpose
1	000010_8 + (Nx2)	000000616200	System Fault Vector	Disconnect if get a system fault when loading or executing BOOT program
2	000030_8 + (Nx2)	000000616200	Terminate Int Vector	1st record will begin here. Disconnect if record not read (device offline, etc.)
3	$XXXX00_8$ + 07_8	XXXX02000002	Fault channel DCW	Tally word for storing System fault status at Base Address + 2 (in case stop at word #1)
4	$XXXX00_8$ + 10_8	000000040000	Connect channel LPW	Upon receiving connect, do a list service (with no change) to PCW pair starting at location 000000_8
5	$XXXX00_8$ + (BBx4)	000003020003	BOOT device LPW	2 DCWs for BOOT device starts at location 000003_8
6	000004_8	000030000000	2nd DCW	IOTD
7	$XXXX00_8$ + (BBx4) + 2	XXXX00000000	BOOT device SCW	Tally word for storing BOOT device status at Base Address (in case stop at word #2)
8	000000_8	000000720201	1st word of PCW pair	for PSI: initiate channel for CPI: request status (1 time) and continue
9	000001_8	0BB00000000P	2nd word of PCW pair	BOOT device channel #, Port #
10	000002_8	XXXX00XXYYYN	next word after PCW	Base Address, Program Interrupt Base, IOM #
11	000003_8	0C0000700000	IDCW	Read binary command (C = 1 if card reader, C = 5 if tape)

Figure 3.10.b - BOOT Program

3.11 SCRATCHPAD ACCESS CHANNEL

The scratchpad access channel provides the test and diagnostic software with a way of loading or storing the contents of the channel mailboxes. By appropriate coding of the PCW the scratchpad mailboxes of a specified channel can be loaded or stored from specified locations in core. The channel will access the scratchpad when it is physically present; if a channel has no scratchpad, the mailbox in core for that channel will be accessed.

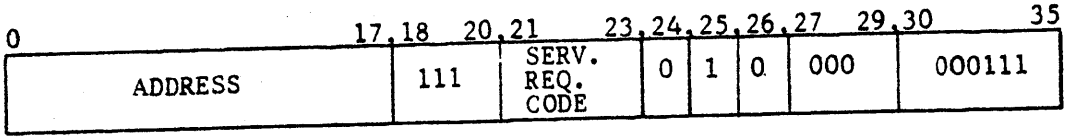
The scratchpad access channel will be wired as channel number 07. The LPW, LPW extension, and SCW mailboxes for the scratchpad access channel will not be used by the IOM Central. Only the DCW for channel 07_8 will be used.

The scratchpad access channel will do an indirect data service under control of its DCW, reading from scratchpad and storing into core, or vice-versa. Upon completion of the transfer, an appropriate multiplex interrupt to level one is executed.

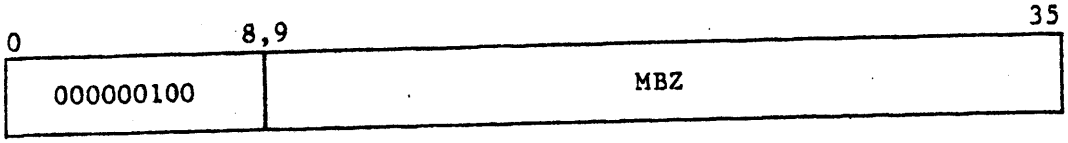
Software should not issue successive connects to the scratchpad access channel until the interrupt is received from the previous connect; otherwise the action called for by the connect may not be performed.

Format for the PCW using the Scratchpad Access Channel is as follows:

Even Word:



Odd Word:



It may be seen by examination of the PCW that the Scratchpad Access Channel is operated by means of the Wraparound Channel. The PCW is addressed to the Wraparound Channel, which does a service in lieu of the Scratchpad Access Channel using the DCW for channel 07_8.

3.11 SCRATCHPAD ACCESS CHANNEL (continued)

The fields in the PCW are defined as follows:

Even Word:

Bits 0-17 Contain bits 6-23 of the absolute address of mailbox, referenced to IOM Mailbox base address switches; i.e., the switches will be logically ORed with these bits to form the actual address of a mailbox. The IOM will append zeros for bits 0-5 of the absolute address. Channels which have standard or optional scratchpad present will have the access directed to the scratchpad. When an address exceeds the address of the last available scratchpad, the access is directed to that mailbox in core. Representative examples are:

PCW 0-17$_8$	Scratchpad Word Select
000040	LPW, Channel 10_8
000041	LPWX, Channel 10_8
000042	SCW, Channel 10_8
000043	DCW, Channel 10_8
000044	LPW, Channel 11_8
000045	LPWX, Channel 11_8
000046	SCW, Channel 11_8
000047	DCW, Channel 11_8
.	. .
.	. .
.	. .
.	. .
000234	LPW, Channel 47_8
000235	LPWX, Channel 47_8
000236	SCW, Channel 47_8
000237	DCW, Channel 47_8

18-20 These bits are 111 to identify a PCW.

21-23 Only two Service Request codes are meaningful to the Scratchpad Access Channel:

100 (Indirect load) Information read from the core location specified by the DCW for the Scratchpad access channel is written into the mailbox specified in bits 0-17 of the PCW.

101 (Indirect store) Information is taken from the mailbox specified in PCW bits 0-17, and stored in the core location designated by the DCW for the Scratchpad Access Channel.

3.11 SCRATCHPAD ACCESS CHANNEL (Continued)

24	Mod bit must be zero to allow accessing of scratchpad when available.
25	Byte size should be 1 to access the full 36 bit word.
26	Address extension control - must be zero.
27 - 29	Action code is 000.
30 - 35	Specify the channel number of the scratchpad access channel 007_8.

Odd Word:

Bits 0 - 8	Address the PCW to the Wraparound Channel, 004_8.
9 - 35	These bits are unused and must be zero for future compatibility.

3.12 MAINTENANCE PANEL AND CONFIGURATION SWITCHES

In order to provide for both static and dynamic test capability of the IOM Central, maintenance functions and Maintenance Panel controls are being incorporated to allow simulation of the listed inputs to the Central:

(a) System Store Data

B (b) Channel Transactions or Service Requests
(c) Channel Data

3.12.1 Fault Location Aids

In addition to the above, which are basically for free-standing test and checkout without attachment to or from any other system component, several maintenance and test aids will be available for dynamic fault location and isolation. Capabilities of these aids are listed below. Note that their primary purpose is to facilitate field maintenance; however, their use in debug and test will provide needed help in initial equipment bring-up.

(a) Single step store cycle
(b) Single step for IOM major cycle
(c) Halt on store address match
(d) Halt on fault (fault channel number match)
(e) Halt on IOM control state match
(f) Halt on channel number match
(g) Halt on channel request code match

3.12.1 Fault Location Aids (continued)

Other system configuration and panel switches as required by 6000B System EPS-1, referenced in paragraph 1.4, will be included.

3.12.2 Base Addresses

Channel Mailbox Base Address - Twelve switches on the IOM configuration panel provide bits 6-17 of the channel mailbox base address. The address extension, bits 0-5, and bits 18-23 of this base address are zero.

Interrupt Multiplex Base Address - Bits 0-11 of the Interrupt Multiplex Base Address are the same as Bit 0-11 of the Channel Mailbox Address and are controlled by the same set of switches. Nine switches on the IOM configuartion panel provide bits 12-18, 22, and 23 of the Interrupt Multiplex Base Address. Bits 19-21 of this base address are zero.

3.12.3 Software Operating System Control

A manually-operated three-position configuration switch will be provided on the IOM configuration panel to place restrictions on the allowable operating system:

B

Position 1 - "Standard GCOS"
Position 2 - "Extended GCOS"
Position 3 - "MULTICS"

A set of system and user faults will be reported if the operating system attempts to exceed mode constraints.

3.12.4 Configuration Switches

The IOM maintenance panel configuration switches are listed in the following table. The functions they perform (when not obvious) are defined elsewhere in this specification.

Function	Quantity/Type*
IOM Base Address	12/A
Multiplex Base Address	7/A
IOM Number	2/A
Operating System	1/D
Bootload:	
- Card/Tape Selector	1/A
- Mag Tape Channel Number	6/A
- Card Reader Channel Number	6/A
- Bootload	1/B
- System initialize	1/B
- Bootload Port	3/A
Port Configuration (Per Port)	
- Address Assignment	3/A
- Interlace (per port pair)	1/C
- Port Enable	1/A
- System Initialize Enable	1/A
- Half Size	1/A
Alarm Disable	1/A
Test/Normal	1/A

*A = 2 position toggle switch
B = Momentary Contact Pushbutton Switch

C = 3 Position Toggle Switch
D = 3 -Position Rotary Switch

3.13 SPECIAL STATUS

PSIA channels have the ability to store special status. All the PSIAs on the IOM shall store their special status words using the LPW and DCW mailboxes assigned to channel 06. The storage shall be on a first come, first serve basis and service for each PSIA channel shall be honored on the basis of its individual priority. As in the System Fault Channel, the LPW and DCW mailboxes can be set up to specify a fixed rotating queue to store the last n special status words. Unlike other channels, the Special Status Channel is always busy, and cannot be a scratchpad channel.

The PSIA channel that stores a special status word in the last word of a buffer shall automatically do a list service request to obtain a new (or the original) DCW. However, since these requests shall also be honored based on the priority of that particular PSIA channel, it is possible for a higher priority PSIA channel to have its store special status request honored before the DCW is reinitialized and to therefore overwrite whatever is in the word following the status buffer. It is highly unlikely that anyone PSIA can delay any other lower PSIA channel more than one service. Therefore, to be "safe", any buffer that could be used for storing special status for multiple PSIA channels should place after it a padding of one word for each PSIA above one PSIA.

4.0 HARDWARE INTERFACE REQUIREMENTS

4.1 STORAGE INTERFACES

4.1.1 System Controller

The IOM Central will interface with from zero to eight 6000B or 6000 system controller ports for performing the following types of cycles:

- Read Restore, Single Precision (RRS,SP)
- Read Restore, Double Precision (RRS,DP)
- Read, Clear Single Precision (RCL,SP)
- Clear Write, Single Precision (CWR,SP)
- Clear Write, Double Precision (CWR,DP)
- Set Execute Interrupt Cell (SXC)

In addition, the IOM will respond to a $CON occurring during a system controller connect cycle. The IOM will generate and check parity on this interface. (See paragraph 4.2.6)

4.1.2 Scratchpad Storage

Each module of the optional scratchpad storage will provide at least48 36-bit words of storage with a complete cycle time of less than 500 nanoseconds. The interface to the scratchpad can be tailored to the requirements of the IOM Central, although full advantage should be taken of the fact that the scratchpad store actually substitutes for a portion of core store so that similar control functions should be provided.

4.2 PRIORITY

The I/O bus priority system is based on a channel's physical location on the bus - the closer to the physical top of the bus, the higher the priority. In addition to the priorities for I/O bus resident boards, the IOM Central overhead channels are also involved in the total priority system. The priority within each I/O bus is fixed. Priority among the I/O buses and the overhead channels is also wired and fixed as follows:

a) Fault Channel (highest priority)
b) Snapshot Channel (second highest priority)
c) I/O Bus #1 (Up to 17 Device Channels or 8 Common Peripheral Channels)
d) I/O Bus #2 (Up to 19 Device Channels or 9 Common Peripheral Channels)
e) I/O Bus #3 (Up to 19 Device channels or 9 Common Peripheral Channels)
f) Maintenance Panel
g) Connect Channel (Lowest Priority)

(A "Device Channel" may be either a High Speed or a Medium Speed Device Channel, or a similar type of channel).

4.3 CHANNEL SERVICE

4.3.1 List Service

Figure 4.3.1 (a,b,c) is a flow diagram of list service. When a list service is performed for a channel, the IOM Central pulls the LPW and LPW extension for that channel from core or scratchpad. On the first list service following the connect, the channel will supply an indication of "First List Service" to IOM Central to direct the LPW access to core rather than to scratchpad (See paragraph A.2.1).

List service is the only way of getting a DCW into scratchpad for subsequent data services, other than using the scratchpad access channel.

The IOM Central checks the LPW for Tally conditions. The LPW address defines the location of

- the next DCW for an indirect data channel, or
- the next PCW for the connect channel

The IOM Central pulls the 36-bit DCW or the 72-bit PCW from the location determined by the LPW. A direct channel will obtain a DCW by a (1) direct data service, supplying the absolute address DCW.

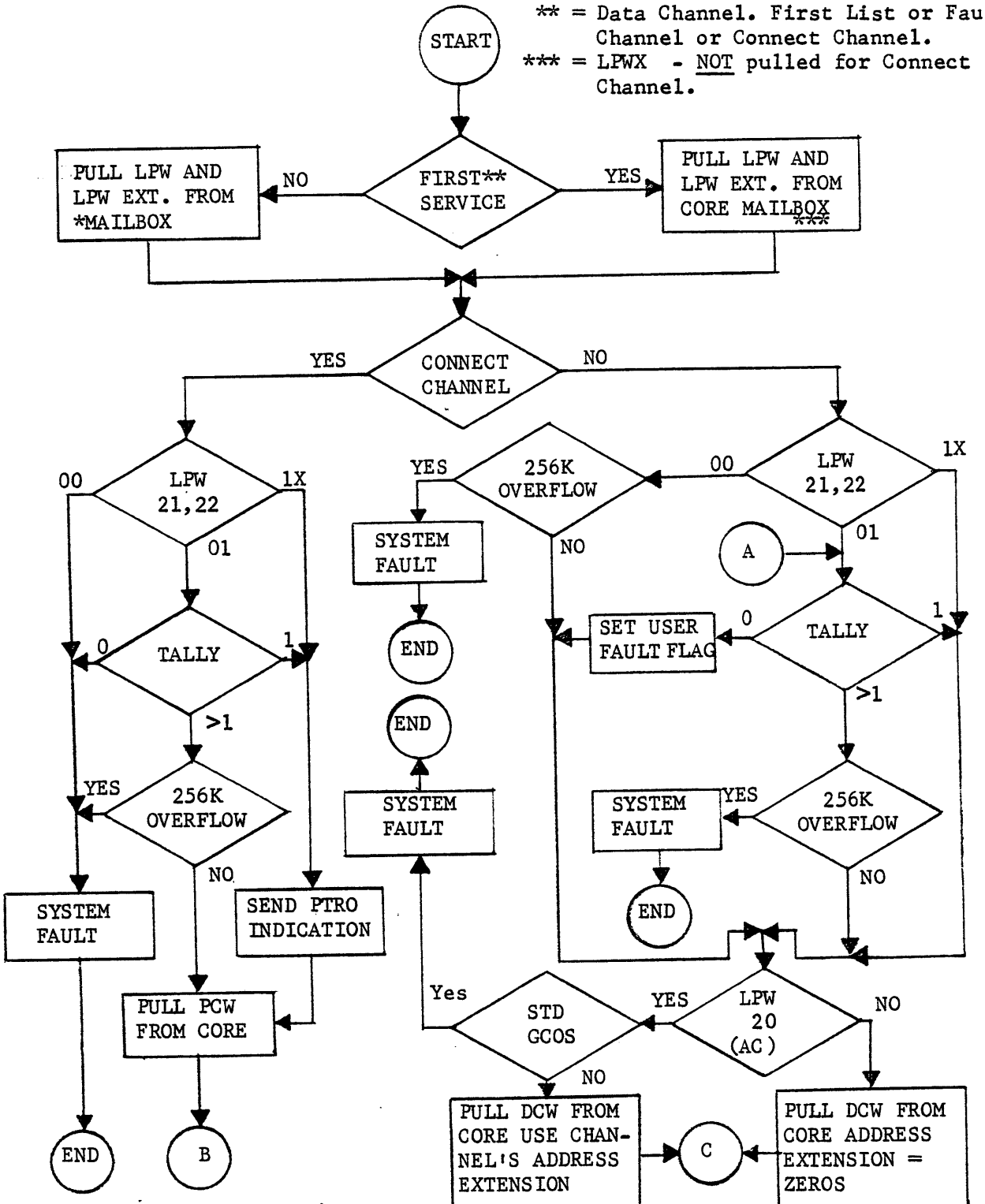
If the service is being performed for a data (payload) channel the IOM Central examines the DCW type. If the DCW is an Instruction DCW (IDCW), and if the LPW is not restricted against Instruction DCW's, the IDCW is treated like a PCW and sent to the channel.

If the DCW is not an IDCW the IOM Central determines the address mode, and absolutizes (and checks) the address, if relative. If the DCW is a transfer DCW (TDCW) the DCW Pointer field of the LPW is replaced by the TDCW address field. Then this address is used to obtain a new DCW (no interruption is allowed). If the DCW is an IOTP, IONTP or IOTD, the DCW is written into the core (or scratchpad) DCW mailbox. This DCW is also sent to the channel so the character position and type fields can be stored for later use.

The IOM Central updates its LPW Address and Tally (if not inhibited). The LPW is then returned to the core (and scratchpad) mailbox. If the service handled an IDCW the LPW and LPW extension are both returned to the mailbox (both core and scratchpad) with the address of the IDCW in bits 18 - 35 of the LPW extension.

4.3.1 Figure 4.3.1a - LIST SERVICE

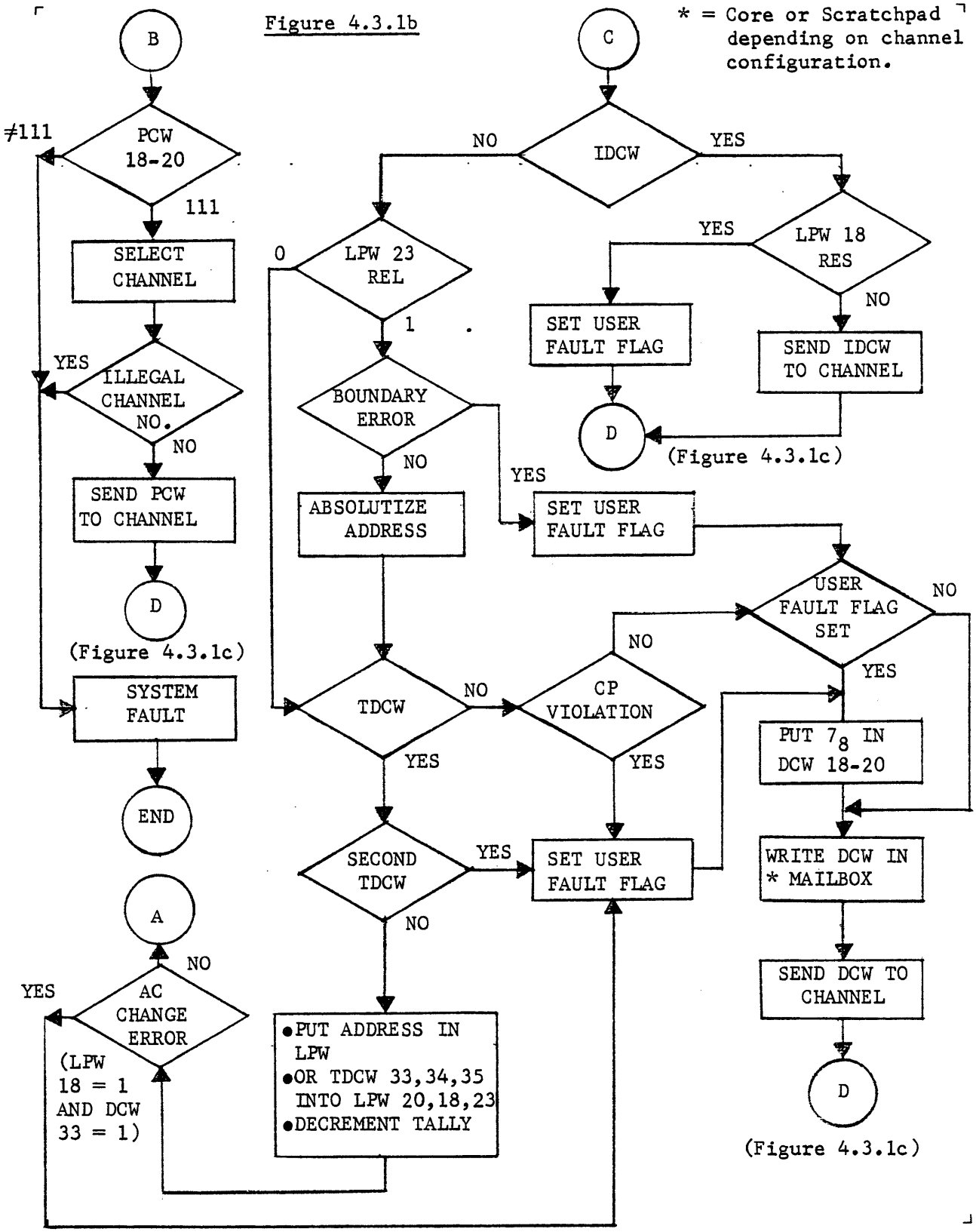
* = Core or Scratchpad depending on channel configuration.
** = Data Channel. First List or Fault Channel or Connect Channel.
*** = LPWX - NOT pulled for Connect Channel.



(Figure 4.3.1b)

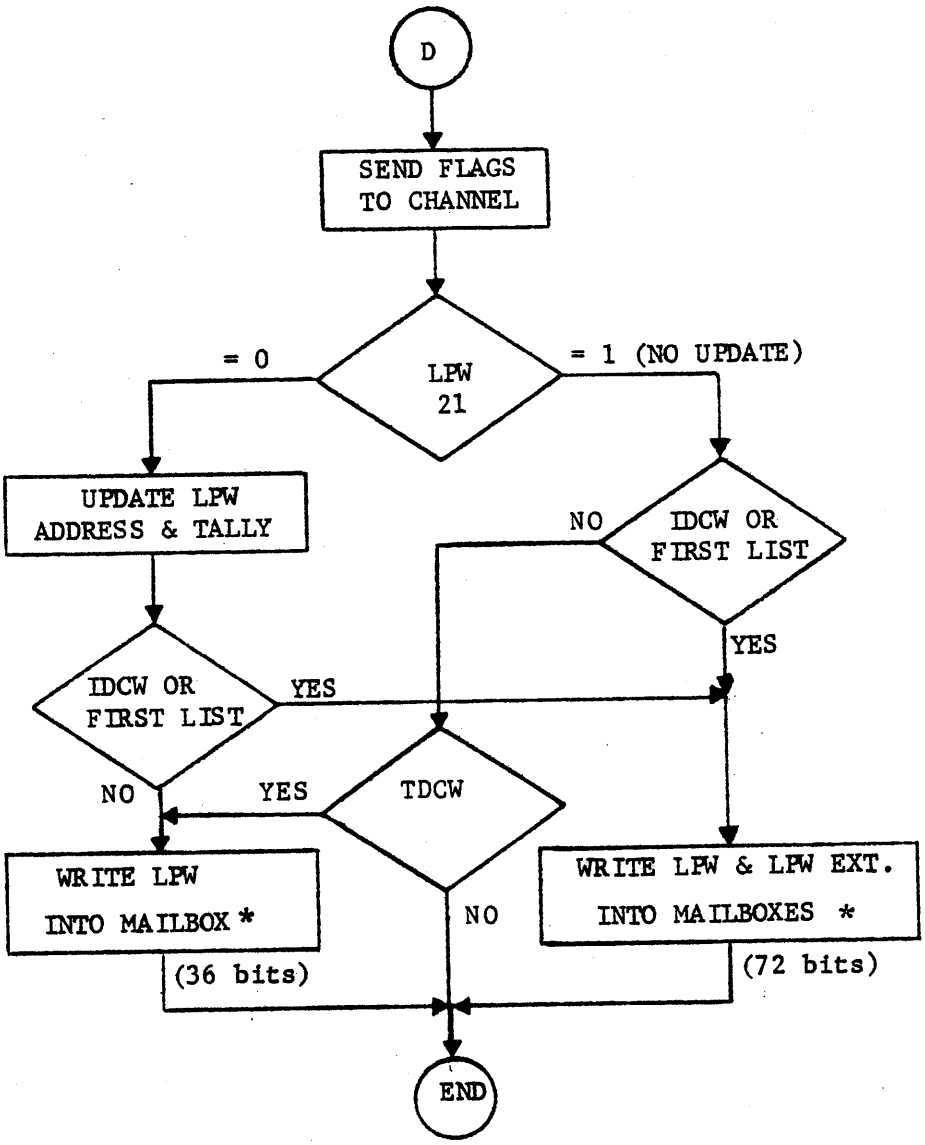
(Figure 4.3.1b)

Figure 4.3.1b



* = Core or Scratchpad depending on channel configuration.

4.3.1 Figure 4.3.1c - LIST SERVICE



*Both in scratchpad and core if channel

4.3.2 Backup List Service

In response to a "backup list service" request from a channel, the IOM Central shall regenerate a list pointer word (LPW) and a list pointer word extension (LPWX) for that channel and shall continue operation on the channel by using the regenerated LPW and LPWX. The format of the regenerated LPW shall be:

REGENERATED LPW		SOURCE
bits 0 - 17	=	LPWX bits 18 - 35 (the pointer to the last IDCW)
bit 18, 20	=	0
bits 19, 21, 22	=	LPW bits 19, 21, 22
bit 23	=	LPW bit 19*
bits 24 -35	=	LPW bits 24 - 35

The format of the regenerated LPWX shall be identical to the format of the current LPWX.

The result of executing the regenerated LPW and LPWX shall be a DCW fetch from the last location to contain an IDCW. Mode shall be non-restricted. Addressing shall be relative or absolute in accordance with the contents of LPW bit 19 (equal to REL flag condition at the time an IDCW was encountered). Tally shall be equal to the LPW tally present at the time of the "backup list service" request. Tally control (bits 21 and 22) shall be the same as the current LPW. Lower Bound and Size constraints for relative addressing shall be the same as the current LPWX.

The DCW pulled following reconstruction of the LPW must be an IDCW. If not, a fault shall be reported by the channel (not by the Central).

The end result of responding to a "backup list service" request shall be a retry (i.e., repeat) of the last command and data transfer sequence entered into for this channel by backing up in the control word list to the last command executed and then retracing the list from that point.

4.3.3 Indirect Data Service

B Figure 4.3.3a is a flow diagram of indirect data service. When an indirect data service is performed for a channel, the IOM Central pulls the channel's DCW from the core mailbox, or from the scratchpad.

*The IOM shall load bit 19 with LPW bit 23 each time an IDCW is fetched or whenever a first-list service is performed.

4.3.3 Indirect Data Service (cont.)

The DCW address defines the location of the data unless the DCW type is IONTP. If the channel is performing a peripheral read (core write) operation, and the DCW is IONTP, there is no storage cycle for data transfer (the data is discarded). If the channel is performing a peripheral write (core read) operation and the DCW type is ONTP, the IOM Central generates a data character or word equal to zero and transfers it to the channel.

The IOM Central updates as appropriate the DCW address, tally and character position, and then writes the DCW back into the mailbox (core or scratchpad).

4.3.4 Direct Data Service

The direct data service consists of one core storage cycle (Read Clear, Read Restore or Clear Write, Double or Single Precision) using an absolute 24-bit address supplied by the channel. This service is used by "peripherals" capable of providing addresses from an external source, such as the 355 Direct Interface Adapter.

4.3.5 Status Service

Figure 4.3.5a is a flow diagram of status service. When a status service is performed for a channel, the IOM Central pulls the channel's SCW from the core mailbox.

The SCW address defines the y-pair where status is to be stored. The status consists of one word of channel and peripheral status obtained from the channel, and one word of DCW residue which the IOM Central obtains from the DCW mailbox (in core or scratchpad). Before transferring these two words to core the IOM Central inserts character position residue and read bit from the channel into bits 18-21 of the DCW residue and inserts the channel's address extension bits into bits 24-29 of the channel status word.

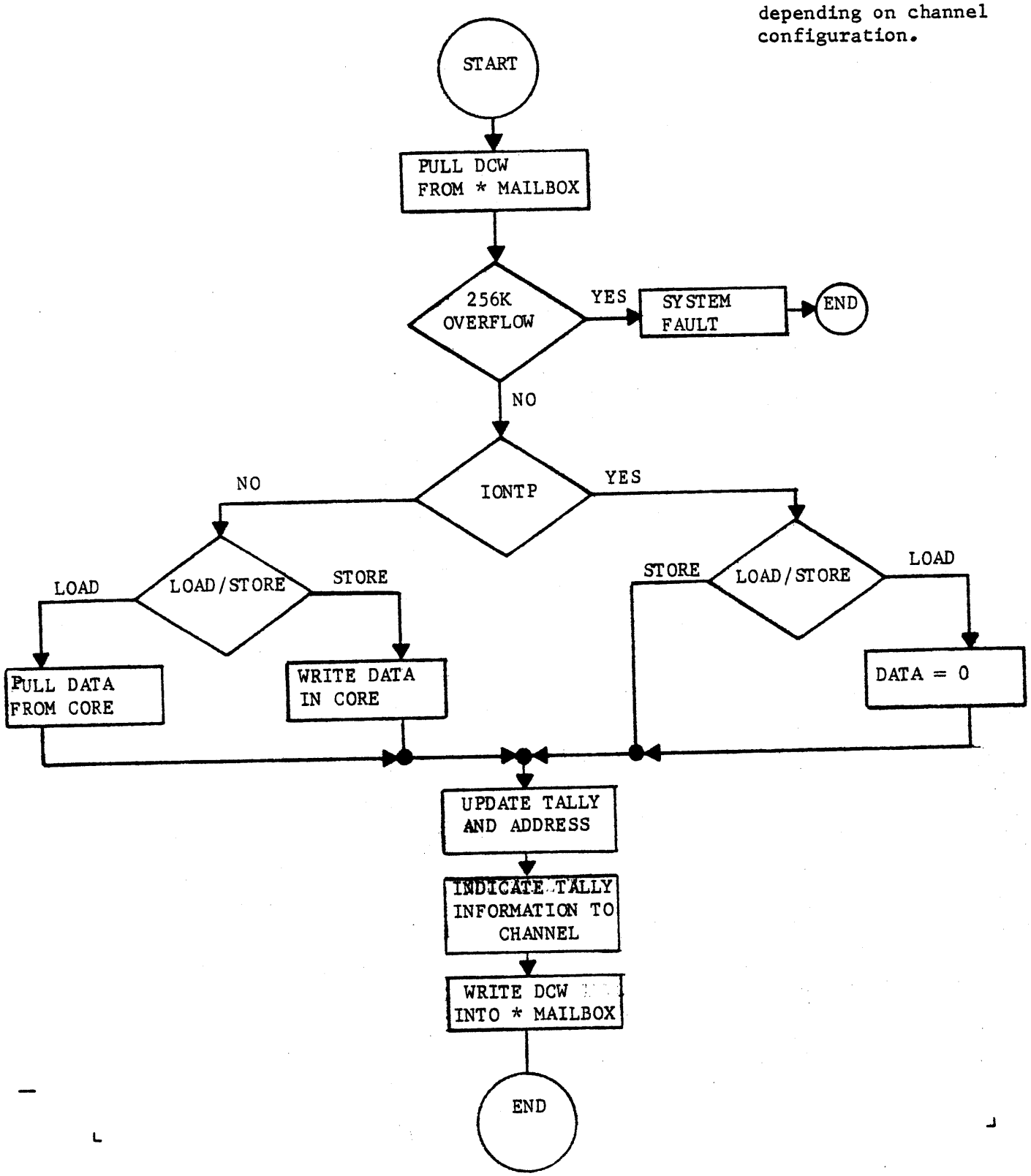
If the tally in the SCW is zero and the SCW does not indicate a circular queue the IOM Central does not update the SCW address and tally. This provides a means for causing all status from a particular channel to be stored in the same y-pair in core. If the SCW tally is not zero, the IOM Central updates the SCW by adding two to the address and by subtracting one from the tally. The SCW is then returned to the SCW mailbox in core store. For an SCW which indicates a circular queue the IOM Central updates the SCW by adding two to the address and by subtracting one from the tally until the end of the queue is reached. The SCW then updates the address back to the top of the queue.

B

B

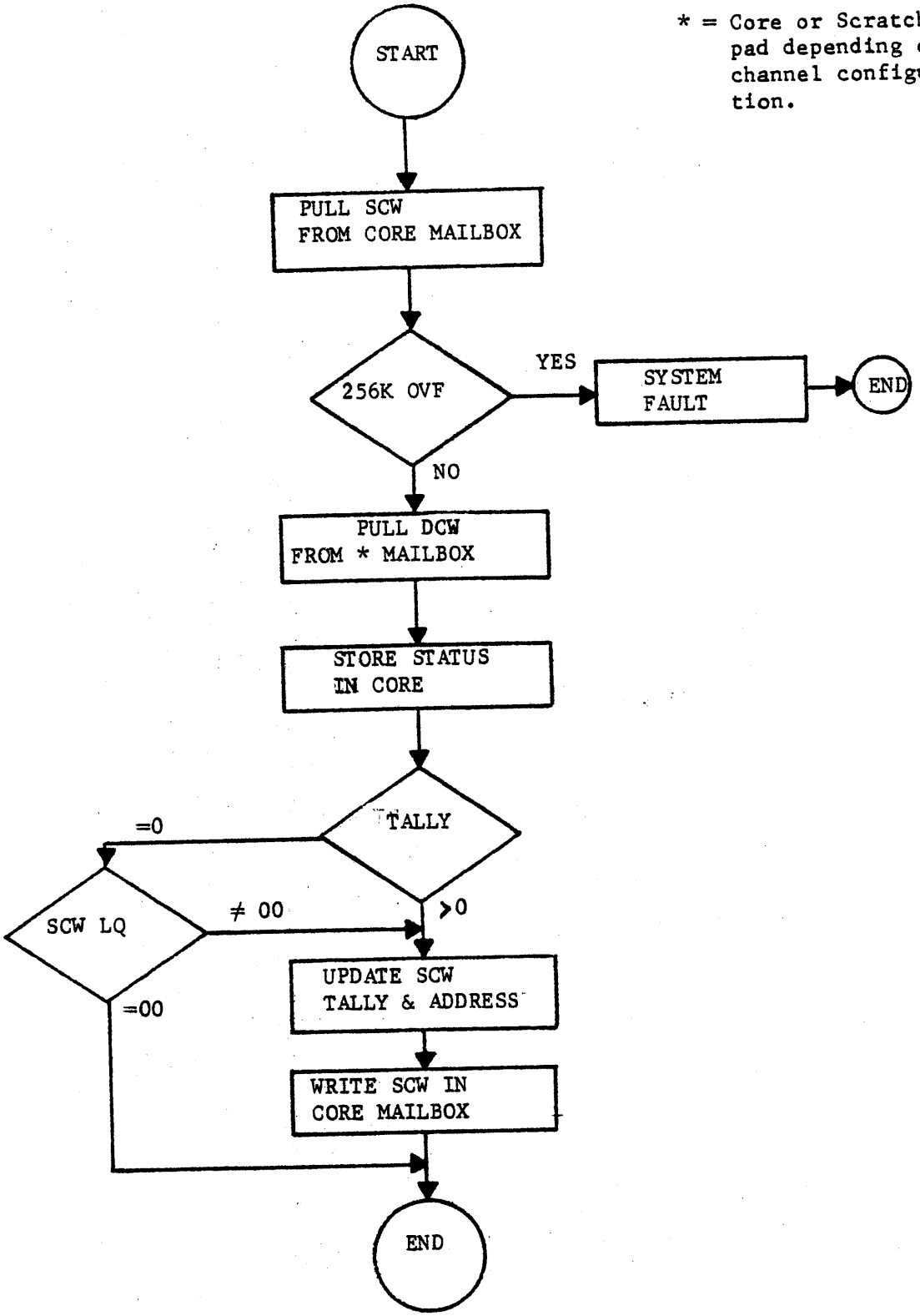
4.3.3 Figure 4.3.3a- Indirect Data Service

* = Core or Scratchpad depending on channel configuration.



B

B 4.3.5 Figure 4.3.5a - Status Service



* = Core or Scratch-pad depending on channel configuration.

4.3.6 Program Interrupt Service (Refer also to paragraphs 3.2.7 and 3.5.2)

Figure 4.3.6 is a flow diagram of a program interrupt service. When such a service is performed for a channel the channel specifies:

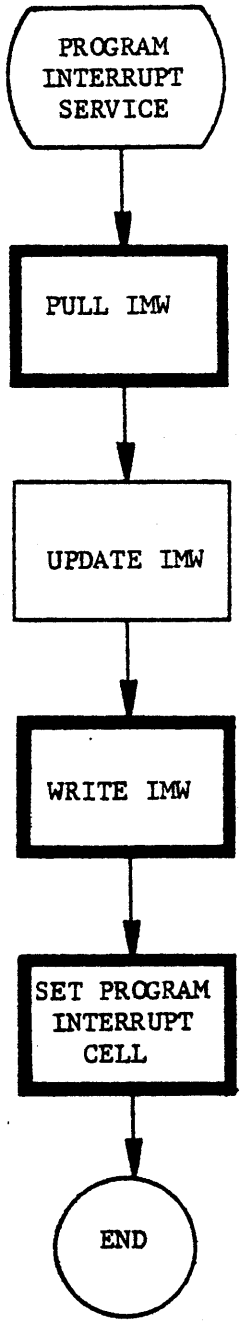
- which Interrupt Multiplex word is to be used and program interrupt cell is to be set:
- which bit is to be set in the Interrupt Multiplex Word (IMW) that corresponds to the program interrupt cell.

There is one IMW in core for each of the 32 program interrupt cells in the System Controller that can be accessed by the IOM (see paragraph 3.2.7).

The Interrupt Cell is determined by the two IOM Identity Switches (least significant bits of IMW base, see section 3.5.2) and by the Interrupt level specified by the channel in the Interrupt Service Request.

The IMW provides a way for the IOM to indicate which channel caused the program interrupt cell to be set. During the interrupt service the five least significant bits of the channel number are used as a 5-bit code by the IOM Central to indicate which bit of the allowable 32 bits in the IMW is to be set to one. The IOM Central obtains the IMW with a Read Clear to Core, OR's a one into the bit specified by the 5-bit code for the channel into the existing IMW, and returns the resulting IMW to the IMW area in core, and then sets the interrupt cell.

4.3.6 Figure 4.3.6 - PROGRAM INTERRUPT SERVICE



4.4 PARITY AND DATA INTEGRITY

Parity will be generated by the central on all data being output to the channel. On character-oriented data, the character will be right-adjusted, with leading zeros.

Parity will be checked by the central on data received during Indirect Store or Direct Store. Parity will not be checked on channel requests for services. Parity will not be checked on List, Status, or Interrupt services.

The IOM will maintain a continuous error check, via parity, on data transferred, both from storage to the peripheral and vice versa. The total path length over which parity is maintained is continuous from the cable interface at the system control to the cable interface at the peripheral.

Since the IOM is directly involved in the major GCOS overhead function of supervisory module swapping into and out of storage, the ability to detect - within the constraints of simple parity error limitations - errors as they may occur in this sensitive data swap function should allow a measure of protection for system operation not previously available in any of our system designs.

It will be possible to define hardware in new peripheral interface adapters such that data integrity is maintainable in a contiguous chain at least through the IOM.

Utilization in the IOM of a scratchpad for storage of control words for indirect channels (i.e., those not providing storage for or direct control over their own Data Control Words) requires repetitive store and retrieve cycles of channel control words from the scratchpad. In order to minimize the probability of an undetected and possibly catastrophic data error being introduced in the repeated cycles involved, parity will be checked or generated and appended to the control words as they are stored in the scratchpad, and checked upon retrieval. An exception to this is the cycle involving the DCW residue word when the IOM central performs a status service for a scratchpad channel. (i.e., parity will not be checked during this access).

4.5 FAULTS

Hardware will be provided in the IOM for the detection and indication of abnormal operating conditions, or faults. These are two distinct classes of faults; user faults, and system faults.

4.5 FAULTS (cont.)

- User Faults - A user fault is an abnormal condition that can be caused by a user program operating in the slave mode in the processor.

- System Faults - A system fault is an abnormal condition that cannot be caused by a user program operating in slave mode, and therefore is assumed to have been caused by a software error or a hardware malfunction.

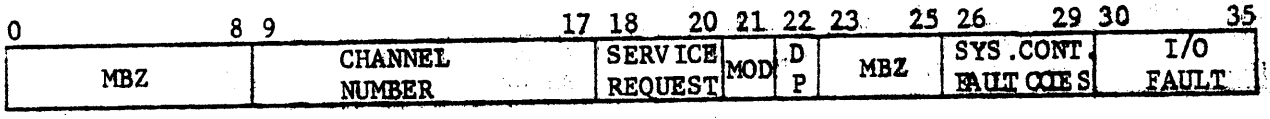
User faults can be detected by the IOM Central or by a channel. If a user fault is detected by the IOM Central, the fault is indicated to the channel, and the channel is responsible for reporting the user fault as status in its regular status queue. A user fault condition does not cause the channel to be masked by the hardware, although the software may take this action in response to the indication of a user fault, if it chooses to.

System faults are detected by the IOM Central and indicated by the system fault channel. The data channel being serviced when the system fault was detected is automatically masked by the central in an attempt to protect the system from a recurrence of the fault.

Because of their nature of timing relationship, certain hardware malfunctions also must be reported as user faults.

4.5.1 System Faults

The IOM system fault word format is shown below:



4.5.1 System Faults (cont.)

System Controller Fault Codes - The system controller fault codes will be placed in the system fault word exactly as they are received on the illegal action lines from the system controller.

SYSTEM CONTROLLER FAULT CODES

Bit 26	27	28	29	
0	0	0	0	None
0	0	0	1	(Not used by system controller)
0	0	1	0	Non-existent address
0	0	1	1	Fault on condition
0	1	0	0	(Not used)
0	1	0	1	Data parity, store to SC
0	1	1	0	Data parity, in store
0	1	1	1	Data parity, store to SC and in store
1	0	0	0	Not control port
1	0	0	1	Port not enabled
1	0	1	0	Illegal instruction
1	0	1	1	Store not ready
1	1	0	0	ZAC parity, active module to SC
1	1	0	1	Data parity, active module to SC
1	1	1	0	ZAC parity, SC to store unit
1	1	1	1	Data parity, SC to store unit

4.5.1 System Faults (cont.)

System Faults - IOM Detected

Bits (30-35)

Code	Signal	Reason
000000	--	No Fault
000001	ILL-CHAN-NO	Attempted to issue a PCW to a channel with a channel number $\geq$ to $40_{(8)}$
000010	ILL-SER-REQ	A channel requested a service with a service request code of zero, a channel number of zero, or a channel number $\geq 40_{(8)}$. NOTE: Channel number $\geq 40_{(8)}$ fault is inhibited when IOM is in test.
000011	PRTY-ERR-SP	Parity error on the read data when accessing scratchpad.
000100	256K-OF	Control word address will be incremented to all zeroes and tally will not be decremented to zero.
000101	LPW-TRO-CONN	Tally was zero for an update LPW (LPW bit 21 = 0) when the LPW was fetched for the Connect Channel.
000110	NOT-PCW-CONN	DCW fetched for the Connect Channel service did not have bits 18-20 equal to 111.
000111	CP=1's DATA	DCW fetched for a data service was a TDCW or had bits 18-20 equal to 111.
001000	CP/CS-BAD-DATA	DCW fetched for a 9 bit channel contained an illegal character position.

4.5.1 System Faults (cont.)

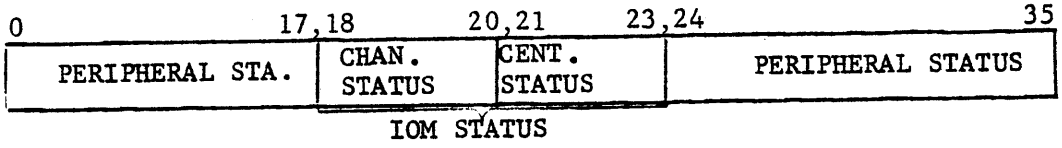
System Faults - IOM Detected (cont.)

Bits (30-35)

Code	Signal	Reason
001001	NO-MEM-RES	No response to an interrupt from a system controller within 16.5 usec.
001010	PRTY-ERR-MEM	Parity error on the read data when accessing a system controller.
001011	ILL-TLY-CONT	Illegal tally control for an LPW (LPW bits 21 and 22 equal zero) when the LPW was fetched for the connect channel.
001110	ILL-LPW-STD	LPW fetched indicates use of address extension, (LPW bit 20 = 1), while operating in the Standard GCOS mode.
001111	NO-PRT-SEL	No port selected during attempt to access memory.

4.5.2 User/Channel Faults

The channel status word format is shown (in abbreviated form) below:



The IOM status field will be divided into 2 independent 3-bit segments; bits 21-23 represent "central" status as it was received from the central, and bits 18-20 represent "channel" status as determined by the channel.

4.5.2.1 Central Status

"Central" status is defined to be those fault conditions which are detected by the central, and which are encoded on the user fault flag lines at the completion of service to the channel. The channel will place this code in the status word exactly as it is received from the central, or a 110_2 code according to the priorities given in that channel's EPS-1.

Bits (21-23) Code	Signal	Reason
000	--	None
001	LPW-TRO	Tally was zero for an update LPW (LPW bit 21=0) when the LPW was fetched and tally run-out indication is on (LPW bit 22=1).
010	2ND-TDCW	Two consecutive transfer DCW were fetched during a list service.
011	BNDY-VIO	Boundary error occurred when performing boundary check on the DCW fetched during a list service with an LPW indicating relative DCW's.
100	AC-CHG-RES	A transfer DCW attempted to change the address extension control bit in the LPW (LPW bit 20) to a one when the LPW was already in the restricted mode when LPW was fetched.

4.5.2.1 Central Status (cont.)

Bits (21-23)

Code	Signal	Reason
101	CDCW-RES	Fetched an Instruction DCW when LPW indicates restricted mode, (LPW bit 18=1), during a list service.
110	CP/CS-BAD-LIST	DCW fetched during a list service had an illegal character position
111	I/O-PRTY-ERR	Parity error detected on data from a channel during a data store service.

Since only three lines are available on the I/O bus for USER/ Channel fault indication to the channel, there is no way to way to indicate simultaneous faults. Accordingly, the cause indicated to the channel in case of simultaneous faults will be that which is closest to the top in the above list (in other words, the causes have been ranked according to the probability that they could "snowball" into other faults).

4.5.2.2 Channel Status

"Channel" status is defined to be those fault conditions which are detected by the channel and which are recorded in the channel status word, independent of a possible simultaneous indication from the central.

Bit 18	19	20	Cause
0	0	0	None
0	0	1	Unexpected PCW (connect while busy)
0	1	0	Illegal instruction to channel in PCW
0	1	1	Incorrect DCW, list service
1	0	0	Incomplete instruction sequence
1	0	1	Not used
1	1	0	Parity error, peripheral interface
1	1	1	Parity error, I/O Bus, data to channel

4.5.2.2 Channel Status (continued)

As in the case of central-detected faults, the channel-detected faults are ranked such that the case closest to the top is the only one reported in case of simultaneous faults.

4.5.3 Fault Definitions

For the sake of convenience, the definitions of certain system fault conditions are provided below. If the condition is not listed here, it is assumed to be self-explanatory.

Illegal channel number: Detected if an instruction is issued to a channel whose number is greater than or equal to 40_8. No "holes" in the channel number assignments will be detected.

256K overflow: Detected when the address field of a control word (SCW, LPW, or DCW), when updated, will be equal to or greater than 256K, but the tally will not decrement to zero. In the case of the LPW, LPWA bit 21 must equal zero to detect this fault.

Character position field all one's, data service: When a USER/Channel fault is detected during a list service, the character position field of the DCW is purposely set to all one's. In the event that the channel fails to respond to the fault indication, it would try to use the DCW during a data service; the resulting system fault can be assumed to indicate the malfunction of the channel.

Character position/size discrepancy, data service: This condition is encountered if the character size field specified by the channel in the request for data service is inconsistent with the character position field in the DCW. For example, the channel may say it is a 9 bit channel; any character position count greater than 011_2 is invalid and the assumption is made that the most probable cause is a failure in the central's character position updating logic. Note that this same discrepancy is a USER/Channel fault if detected during a List service. Note also that this fault automatically becomes a "Character position

4.5.3 Fault Definitions (cont.)

field all one's, data service" system fault if the Character position is, in fact, all one's. This fault will only be checked for a 9 bit channel.

No core response: The central begins a time-out upon issuing a $INT to a system controller. If no $PIN is received within 16.5 microseconds, this fault is reported.

Tally control error, connect channel: Detected when the LPW for the connect channel has both LPW 21 and LPW 22 set equal to zero.

LPW tally runout: Detected when the tally of the LPW is zero when the LPW is accessed, provided that LPW 21 is zero and LPW 22 is one.

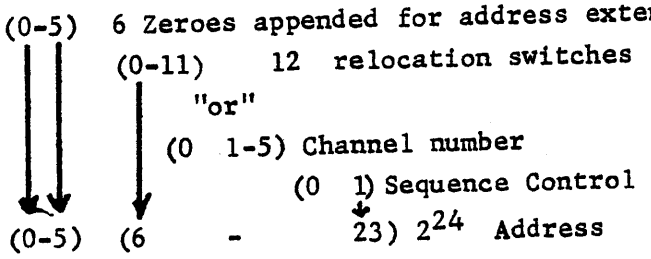
Character position/ size discrepancy, list service: This condition is encountered if the character size field specified by the channel is inconsistent with the character position field in the DCW. This is only checked for 9 bit channels.

NOTE: This is a user fault, whereas all of the faults defined above are system faults.

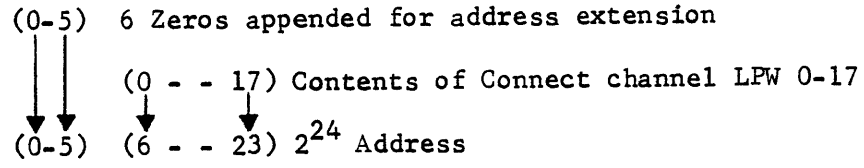
4.6 2^{24} ADDRESS DEVELOPMENT SUMMARY

The following summary is included to show the development of the 24-bit address to be employed in the 6000B IOM.

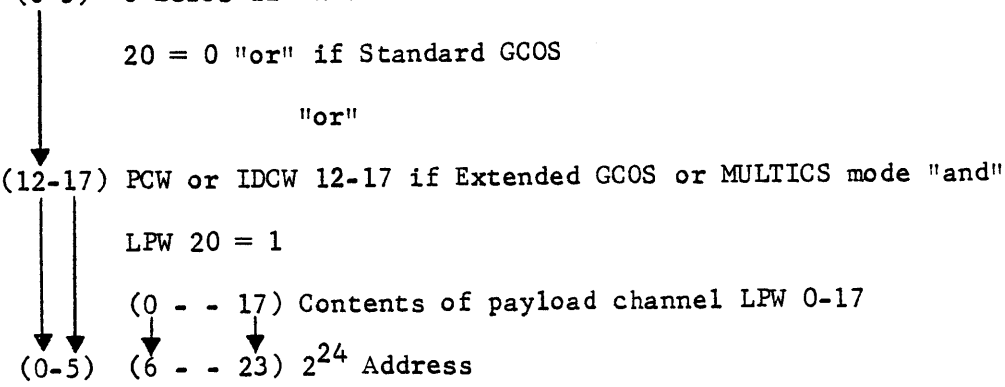
4.6.1 Mailbox Addresses - Any Mode



4.6.2 PCW List Address - Any Mode

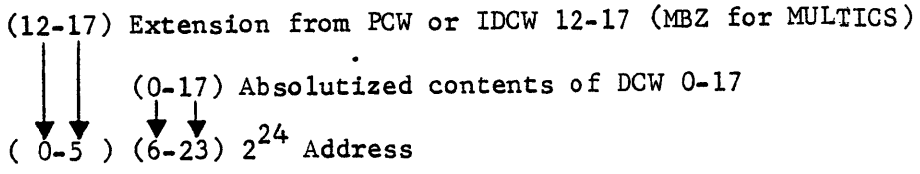


4.6.3 DCW List Addresses



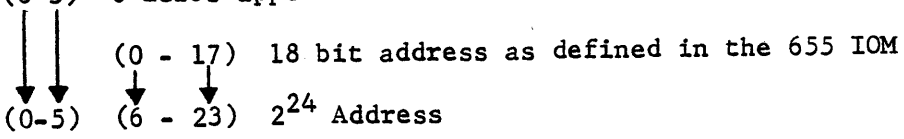
4.6.4 Data Addresses

.DCW 21 = 0



.DCW 21 = 1 will be forced to a zero

4.6.5 Status Lists, Interrupt Multiplex Words, and System Fault Word Addresses - Any Mode



5.0 GENERAL DESIGN REQUIREMENTS

The 6000B Input/Output Multiplexor and all components thereof shall conform, except as specified below, to the general design requirements contained in the G-655 General Design Requirements EPS-1, 43A177851 and the 6000 System EPS-1.

6.0 RELIABILITY AND MAINTAINABILITY

6.1 RELIABILITY

6.1.1 Availability

The availability objective shall be a minimum of 99 percent where:

$$\text{Availability} = \frac{\text{MTBF}}{\text{MTBF} + \text{MTTR}} \times 100$$

or MTBF $\geq$ 99 MTTR

6.1.2 Mean Time Between Failure (MTBF) and Mean Time to Repair (MTTR)

The minimum acceptable MTBF and MTTR shall be in accordance with the standards set by the Maintainability Design EPS-1, #43A219617.

6.1.3 Transient Error Rates

A transient error is defined as a momentary error. It may or may not be repeated in the sense that it can be made to recur but is is not a hard or continuous error as might be caused by a hard component, wire run, etc. failure.

It is desirable that main frame system modules have an error rate sufficiently low to insure that their contribution to over-all system error rates is insignificant. Currently, mass storage media state-of-the-art non-recoverable read error rates are in the order of 10^{-12} bits transferred. This would imply that the main frame equipment should have a transient error rate on the order of 10^{-13} bits. Since magnetics modules in main frame equipment are the biggest contributors to error rates it is then desirable for the non-magnetic main frame equipment to have a transient error rates it is then desirable for the non-magnetic main frame equipment to have a transient error rate in the order of 10^{-14} bits.

Error rates on the order of 10^{-13} or 10^{-14} are virtually impossible to measure directly. Therefore, in order to determine whether or not the error rate is attainable, it is necessary to establish a criteria other than direct measurement.

Typical causes of transient errors might be "flaky" gates, self generated noise from pulses and logic level changes generated within the equipment or externally generated noise. Of the three mentioned, self generated noise is the one which might be considered the most inherent cause of transient errors.

Therefore, the criteria for measuring transient error rates shall be the signal to noise ratio as seen on the internal cabinet wiring. The mean signal to noise ratio should be 8.75 or greater for non-magnetic modules and 8.5 or greater for magnetic modules at a 90% confidence level. No sampled ratio shall be less than 8.0. Signal to noise ratio as used here is the voltage threshold level for going from a "0" to a "1" divided by the RMS value of the noise voltage. These signal to noise ratios give approximately 10^{-17} and 10^{-16} bit error probabilities on a single line of non-magnetic and magnetic modules respectively. These translate to 10^{-14} and 10^{-13} respectively by making the assumption that there are 1,000 statistically independent (conservative assumption because they are probably not independent) lines in a cabinet that can contribute to transient errors as a result of noise.

Measurement of Transient Error Rate

This paragraph does not define explicitly how the transient error rate or signal to noise ratio should be measured, but it does point out some of the things that need to be considered in making this measurement.

6.1.3 Measurement of Transient Error Rate (cont.)

The selection of points in a cabinet to be measured should take into account which signals are critical in the sense that false momentary triggering will cause an error. In addition, the location and/or bunching of such signals should be considered. That is to say, sample points should be selected from both densely and sparsely populated areas.

In determining the size of the sample to be taken, it should be acceptable to assume that the standard deviation of the sample and the entire population are equal and that the distribution of the means of all possible samples is normal. This then implies the following:

$$\frac{\sum_{i=1}^{n} (S/N)_i}{n} + \frac{1.28\,\sigma_s}{\sqrt{n}} \leq (S/N)\ \text{spec}$$

where: $(S/N)_i$ = Signal to noise ratio of the 1^{th} sample

n = Sample size -- greater than 30

σ_s = Standard deviation of the sample $\frac{1}{2}$

$$\sigma_s = \left(\frac{\sum_{i=1}^{n} (S/N)_i^2 - n\left(\sum_{i=1}^{n} (S/N)_i\right)^2}{n-1} \right)$$

(S/N) spec = specified signal to noise ratio

Averaging of signal to noise ratios in this manner to gain some assurance of a cabinet transient error rate is not theoretically sound unless the spread on the ratio is small. For this reason the minimum value of 8.0 has been selected.

6.2 MAINTAINABILITY

The 6000B IOM shall conform to the GE-655 Maintainability Design EPS-1 #43A219617.

APPENDIX A

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APPENDIX A

IOM CENTRAL BUS INTERFACE

A.1 SCOPE

This Appendix describes the performance requirements for the IOM Central/Channel Interface.

A.2 IOM CENTRAL BUS INTERFACE

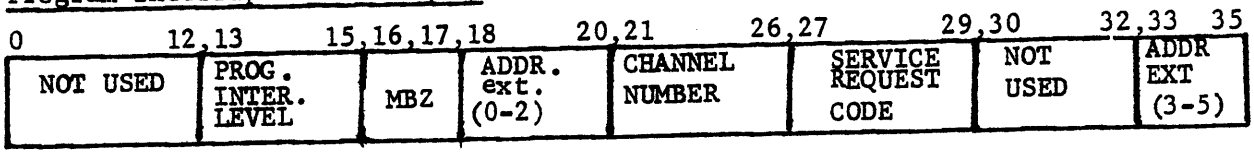
The IOM Central/Channel interface is implemented as a common, time-shared bus. All signals on the bus are in complement form. The I/O bus is organized as follows:

- The 37-bit (36 information plus parity) "D" bus carries service requests, address extension and data from the channel to the central.
- The 37-bit (36 information plus parity) "U" bus carries data, address extension and control words from the central to all channels.
- The 11-bit "C" bus provides control flags and strobes from the Central to all channels. It also carries the common Channel Requests for Service (CRS) line from the channels to the central.
- The 6-bit "P" bus carries the five serial priority lines from channel to channel, plus Group Activity Inhibit (GAI).
- The 6-bit "N" bus provides the channel number which accompanies a peripheral control word.

A.2.1 D BUS: INPUT DATA BUS

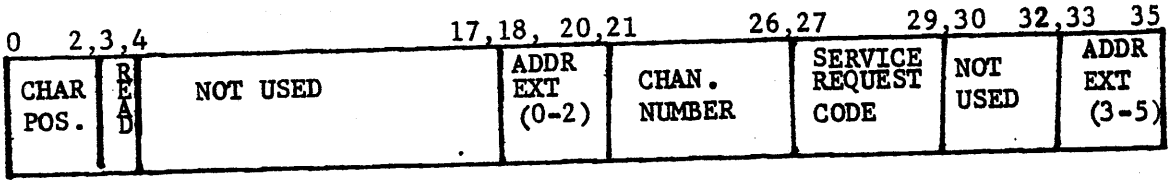
When a channel requests service it must specify the type of service by placing certain information on the data input bus. The formats required for the specific services are given below:

Program Interrupt Service (PI)

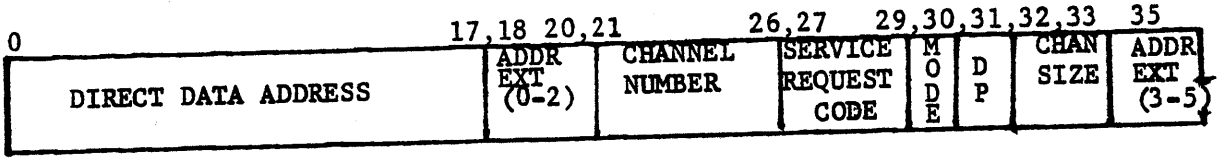


A.2.1 D BUS: INPUT DATA BUS (cont.)

Status Service (STA)



Data or List Service (ILD, IST, DLD, DST, LST)



- Program Interrupt Cell Field - A three-bit field used in conjunction with the IOM Identity switches to select one of 32 program interrupt words and the associated interrupt cell in the System Controller. Valid only during Program Interrupt Service (PI). Bits 16 and 17 must be zero.

- Channel Number Field - A six-bit field used to specify the number assigned to the requesting channel. This number is used to determined "mailbox" addresses and to identify the channel being serviced when a system fault occurs. During a Program Interrupt Service, the five least-significant bits of this field select the bit in the IMW to be set.

- Service Request Field - A three-bit field used to describe the type of service the Central is to perform. The invalid code will cause a system fault. The bits are coded as follows:

SRO (27)	SR1 (28)	SR2 (29)	
0	0	0	INV - Invalid
0	0	1	LST - List Service
0	1	0	STA - Status Service
0	1	1	PI - Program Interrupt Service
1	0	0	ILD - Indirect Data Load Service
1	0	1	IST - Indirect Data Store Service
1	1	0	DLD - Direct Data Load Service
1	1	1	DST - Direct Data Store Service

A.2.1 D BUS: INPUT DATA BUS (cont.)

- Character Position & "READ" Field - The character position residue is to be ORed into the character position field of the DCW residue status word (the odd word of status pair); the "READ" bit is placed in bit 21 of the DCW residue status word. The generation of these bits is the responsibility of the channel, and they are only valid during a status service.

- Address extension (0-2) and (3-5) - These two fields specify the 6-bit address extension to be used by the central in forming 24 bit addresses.

- Direct Data Address Field for a service request of DLD or DST, the address field together with the address extension fields specify an absolute address to be used on the direct load or direct store cycle. This field is ignored for a service request of ILD or IST.

- Mod Field - This 1-bit field is valid only for a service request of LST and DLD.

  A "1" in the Mod field for LST indicates that this is a "first list service" and that the central must obtain the LPW and LPW extension from core rather than from the scratchpad. A "1" in the Mod field for DLD indicates that the service requested is a DirectRD Clear

- DP Double Precision Field - A one-bit in this field indicates that the service requested is to be double precision. Valid only with ILD, IST, DLD, or DST.

- Character (Byte) Size Field - A one-bit field generated by the channel which describes the character size (CS) used in an indirect DATA Service. The CS bits are coded as follows:

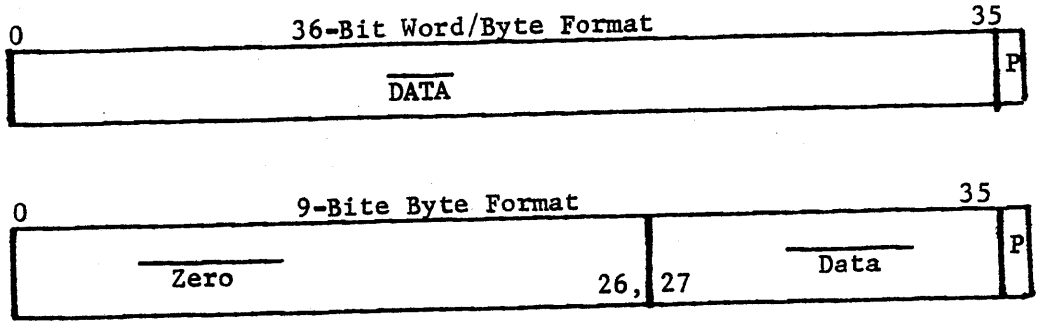
  This bit equal to "0" indicates a CS of 9 bits or equal to "1" indicates a CS of 36 bits.

  NOTE: The CS bits must be provided during a list service as well as during DATA services. Data transfers of 72 bits are accomplished by a double precision transfer of two 36-bit words.

A.2.1 D BUS: INPUT DATA BUS (cont.)

Data Formats

There are two possible data formats on the "D" bus. The data formats on the "D" bus are as follows:



A.2.2 U BUS: OUTPUT DATA BUS

Information from the central to the channel appears on the U bus in one of three separate formats:

(1) PCW information - The PCW obtained as a result of a connect operation is sent to the channel on the U bus. The information is not reformatted by the channel, but is placed on the U-bus exactly as it was obtained from the store.

(2) DCW information - A DCW obtained during a list service is placed on the U bus so that the channel may extract address extension character position and action code information.

(3) Data - Data intended for a channel is placed on the U bus, right justified (i.e., a 9-bit character will be placed on U 27-35).

A.2.3 C BUS: CONTROL BUS

The 11-bit C bus is defined as follows:

- Channel Initialize - Upon receipt of this signal all channels are required to go to a masked condition. CIN will appear as a negative level for more than 1 microsecond.
- Scan, Double and Data - These signals govern the interaction between the channels and the central
- Channel Request for Service - A channel initiates service by placing this line to the "0" state (see paragraph 4.3).

A.2.3 C BUS: CONTROL BUS (cont.)

- TLO, TL1 - (Tally Indicators) - These two bits indicate the contents of the tally field for three general conditions:

  a) Indirect Data Service: DCW tally after updating.

  b) List Service, except Connect Channel: DCW tally as it will be placed in the mailbox.

  c) List Service, Connect Channel: These flags are not applicable during service to the connect channel.

  The bits are coded as follows:

TLO	TL1	Tally Value
0	0	Zero or greater than three
0	1	One
1	0	Two
1	1	Three

- System Fault - The central will place a "0" on this line to indicate that it has detected a System Fault. A channel is required to go into a masked state upon receiving a System Fault indication.

- User Fault - These three lines are encoded to provide the channel with User Fault information whenever the central has detected a User Fault (see paragraph 4.4.2).

US0	US1	US2	Fault
0	0	0	No User Fault
0	0	1	LPW Tally runout (not connect channel)
0	1	0	2 TDCW's in succession
0	1	1	Boundary Error
1	0	0	Address control change in restricted mode
1	0	1	IDCW in restricted mode
1	1	0	Character Size discrepancy
1	1	1	Parity error on Data bus

A.2.4 N BUS: CHANNEL NUMBER BUS

This 6-bit bus indicates the channel which is to respond to a Peripheral Control Word (PCW). The channel number will be provided only in conjunction with a connect service (i.e., it will not be "wrapped back around" to a channel during data, list, status, etc.)

APPENDIX B

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APPENDIX B

IOM-B PAGING MECHANISM

B1. INTRODUCTION

The IOM-B paging mechanism will provide the IOM-B with the capability to access store using a series of references to 1024 word pages which may be located in random areas throughout store. These reference words are contained in a Page Table which must be set up by the operating software prior to activating a channel for an I/O operation. The absolute location (MOD 64) of the channels Page Table (Page Table Pointer) is given to the IOM in the second word of the PCW used to activate the channel and is stored in a scratchpad on a channel basis. The Page Table Words contained in the Page Table are accessed when required and stored in the scratchpad on a channel basis. Scratchpad area for two Page Table Words must be provided for each channel -- one for the DCW List (PTW-LPW) and one for the data (PTW-DCW). Generally both will be obtained from the same Page Table. The contents of the Page Table Words are used to determine the absolute locations of data or DCW's. Paging is requested on an individual channel basis through control bits in the PCW and program TDCW control bits.

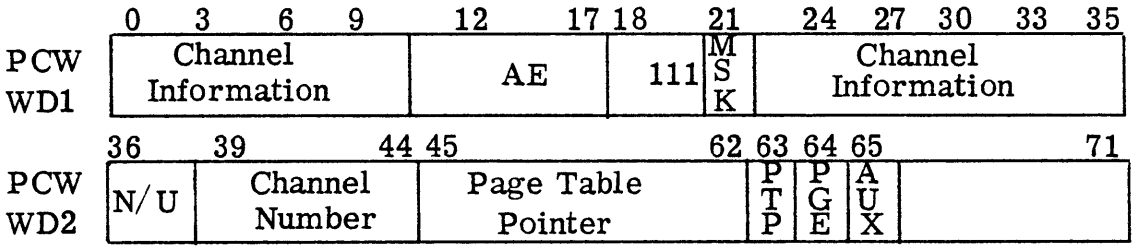
In order to decrease the effect of the paging mechanism on IOM performance and to provide a storage area for the new control words, it is mandatory that all configured channels be provided with scratchpad storage space. The scratchpads will therefore be designed such that one standard scratchpad will be capable of storing all information for channels 8 through 39 and an identical scratchpad may be optionally added to store all information for channels 40 through 63. If some control words must be stored on boards other than the IOM "scratchpad" boards, storage for channels 8 through 63 must be provided. Any attempt to run a channel which does not have scratchpad space will result in a system fault "Illegal Channel Number" (01).

The IOM-B will be capable of operating in any of three modes (as selected on the Mode SELECT switch): (1) Standard GCOS (2) Extended GCOS (3) Paged. When the Mode SELECT switch is in the Paged position all base and bounds information will be interpreted as described in paragraph B4(B) for "Page" mode. Paging will be performed for individual channels if specified in the PCW as described later, otherwise channels will operate as in "Extended GCOS," not relative mode. Changes may be made in the implementation of the Standard GCOS and Extended GCOS modes to facilitate paged mode implementation but these should not affect existing operating systems.

B2. PAGE CONTROL WORDS

A. Page Table Pointer

The Page Table Pointer is sent to the IOM-B as part of PCW Word 2 during a connect operation and will be stored in a channel scratchpad.



Parity will be generated and stored for the Page Table Pointer.

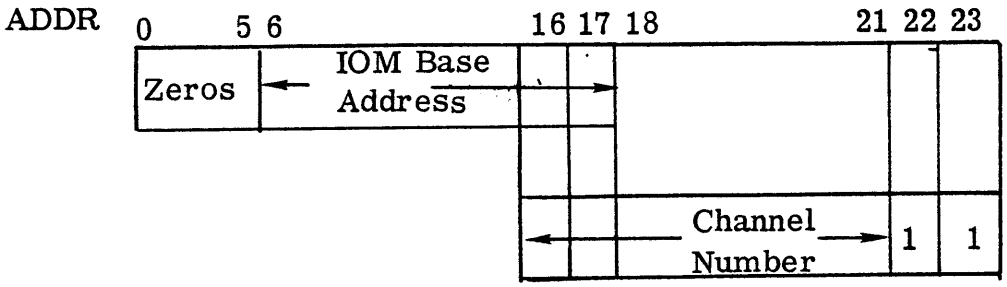
The Page Table Pointer is used to assist in determining the location of the Page Table Word in the Page Table as follows:

Bits 45 ~ 62 - An 18 bit address, mod 64, which points to the beginning of the payload channels page table.

Bit 63 - The PTP flag (PCW-63) must be set if PTW fetch is desired. Any attempt to perform a PTW fetch when PCW-63 is reset will result in a System Fault (14).

Bit 64 - Control of the paging operation is provided on a channel basis by the PGE flag (PCW-64) and through the channels LPW and TDCW.

Bit 65 - If an auxiliary Page Table Word is required, the operating system must set bit 65 (AUX) of the PCW to indicate that the IOM is to obtain an auxiliary PTW from the channel's mailbox address for the DCW as follows:



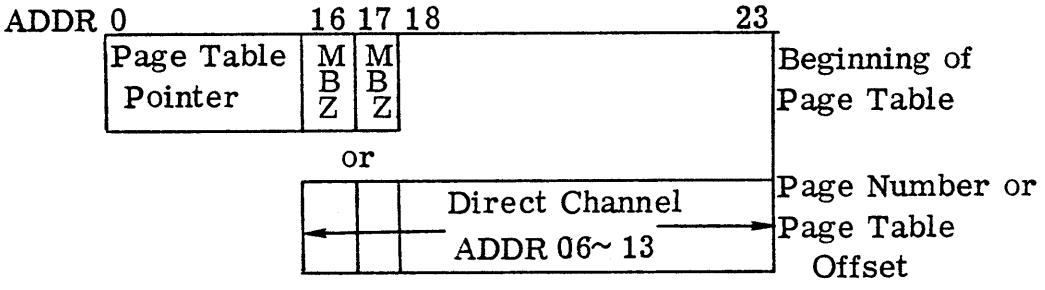
AUX PTW Address

The auxiliary PTW, via PCW65, may be used to access the DCW list when the IOM is in sub mode 3B or 4 (see paragraph B4(D)). Any TDCW encountered while the IOM is in sub-mode 4 will cause the DCW list to be immediately referenced to the normal page table and the IOM to enter sub-mode 5. IDCW's are not allowed in the DCW list stored in the page referenced by the auxiliary PTW. Format for the auxiliary PTW is identical to that for the standard PTW shown in paragraph B2(B). LPW 23 is also not allowed in the original LPW setup by the software if retrys are expected since hardware will have no means of returning to the auxiliary PTW under this condition.

1. Data Service

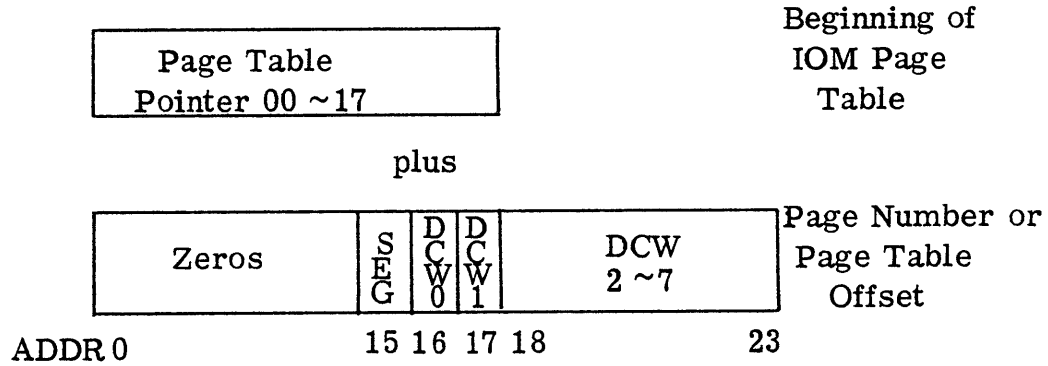
The method by which an address is generated to access a page table word for data services depends upon whether the service requested is direct or indirect type.

(a) Direct Data Service PTW addressing is performed using the PTP as follows:



where a logical "OR" is allowed on the PTP bits 16, 17 and Direct Channel Address 6,7. For the standard direct channel 256 word page table the page table pointer must be assigned a mod 256 location by software (these bits will not be checked by hardware and unexpected results will be obtained if this rule is not followed).

(b) Indirect Data Service PTW addressing is performed as follows:

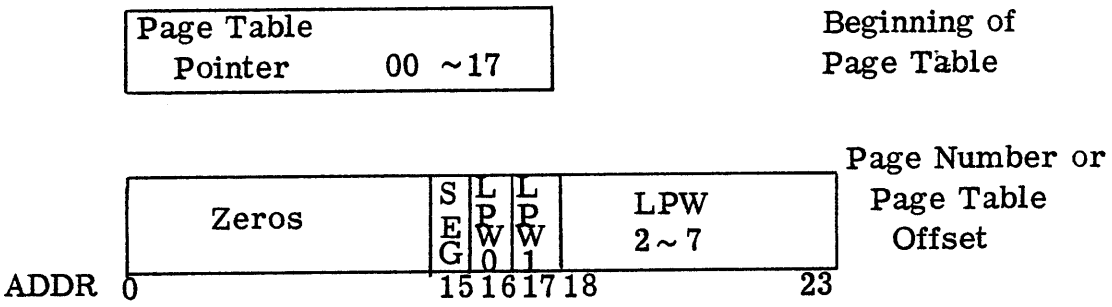


where SEG, and DCW 00 and DCW 01 are added to the contents of PTP 00-17 in order to generate ADDR 00 17. (The meaning of SEG will be explained later.)

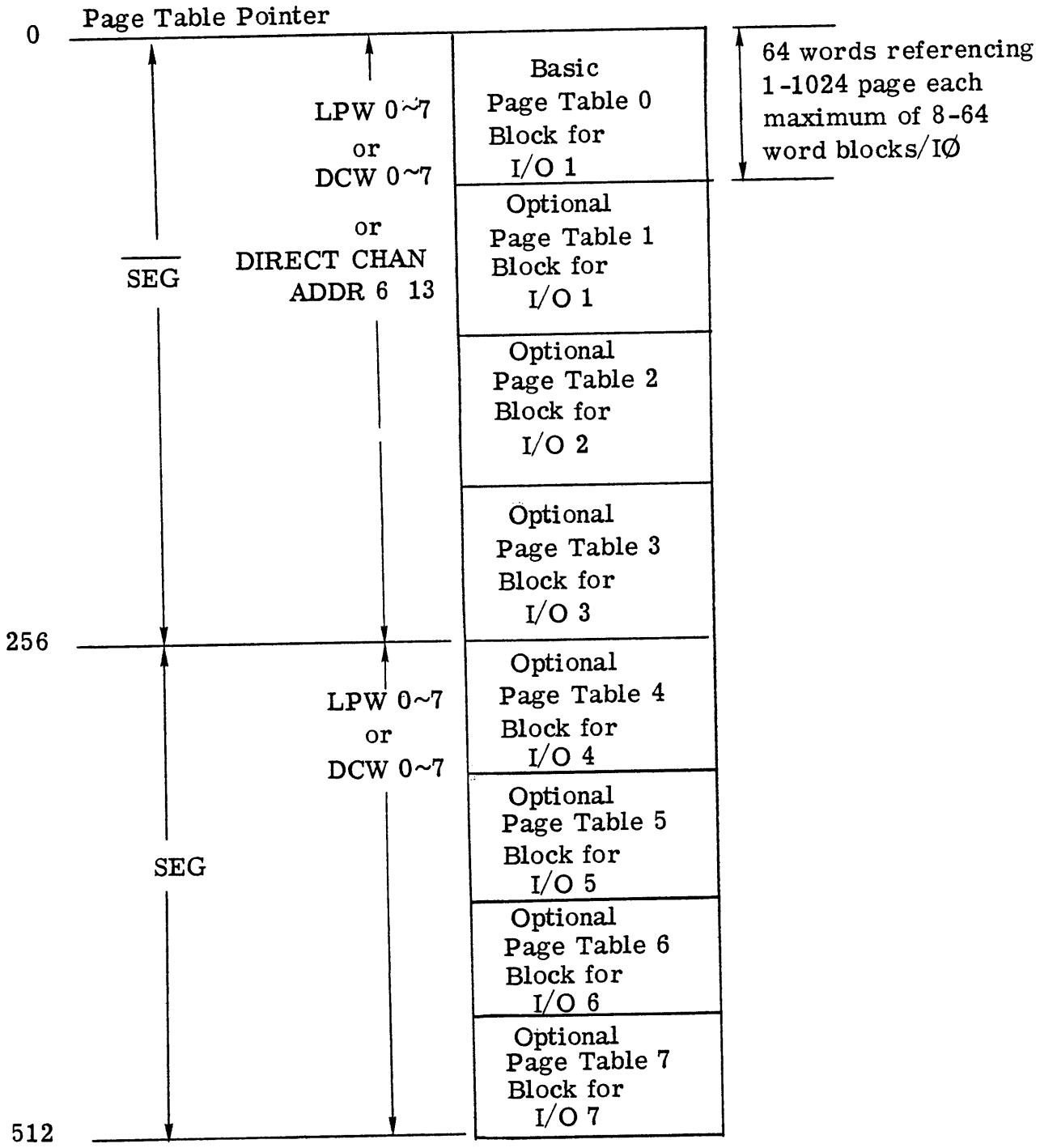
2. List Service

The location of the page table words to be used in accessing a DCW list varies by optionally setting PCW 65 (AUX). When PCW 65=1 the PTW for the DCW list will initially be obtained from the DCW core mailbox as described earlier in this appendix. This auxiliary PTW will be used to access the DCW list until a TDCW is encountered after the LPW has gone Relative, at which time the PTW's for the DCW list (PTW-LPW) are obtained from the channel's page table as described below.

The normal list PTW (either PCW 65=0 or after TDCW described above) addressing is accomplished as follows:



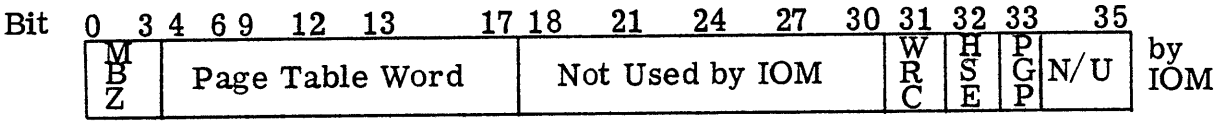
where SEG, LPW 00 and LPW 01 are added to the contents of PTP 00~17 (the meaning of SEG will be explained later).


0
Page Table Pointer
LPW 0~7
or
DCW 0~7
or
DIRECT CHAN
ADDR 6 13
SEG
256
LPW 0~7
or
DCW 0~7
SEG
512
Basic
Page Table 0
Block for
I/O 1
Optional
Page Table 1
Block for
I/O 1
Optional
Page Table 2
Block for
I/O 2
Optional
Page Table 3
Block for
I/O 3
Optional
Page Table 4
Block for
I/O 4
Optional
Page Table 5
Block for
I/O 5
Optional
Page Table 6
Block for
I/O 6
Optional
Page Table 7
Block for
I/O 7
64 words referencing
1-1024 page each
maximum of 8-64
word blocks/IØ

The Page Table Word will be accessed using a Read Restore Single Precision instruction code. Parity will be generated and stored for each Page Table Word.

B. Page Table Word

The Page Table Word obtained as described in the previous paragraph will be stored in the channel scratchpad and the Page Present Flag (bit 33) will be tested for a "1". If the channels LPW has bit 23 set or it is a Direct Service, and a store is being requested, the Write Control (bit 31) and Housekeeping (bit 32) bits will be tested for a 1 and 0, respectively. A System Fault (15) will be stored by the IOM if the accessed PTW fails any of these tests.



PTW Format - NSA

Bits 0 ~3
18 ~30 Ignored by the IOM
34 ~35

Bit 31 Write Control Bit
=0, Page may not be written
=1, Page may be written

The IOM will test bit 31 and 32 only when doing an indirect store if LPW bit 23 is set (data is segmented) or when a direct store service is being requested.

Bit 32 Housekeeping bit - identifies a page which contains processor information which may be accessed by the processor with Privileged Instructions only. The IOM is inhibited from writing in these pages only if it is a direct service or LPW bit 23 (data is segmented). It may read these pages at any time.

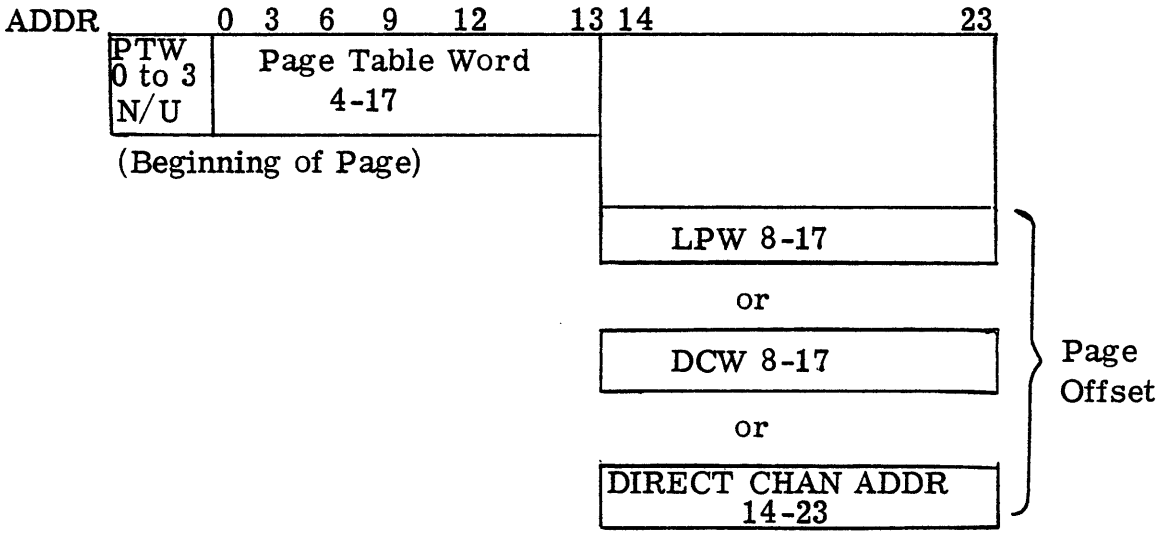
=0, Nonhousekeeping page
=1, Housekeeping page

Bit 33 IOM Page Present/Missing bit - provides an indication that the PTW contains a valid address. The IOM and processor have separate bits to indicate a missing page (bit 30 is used by the processor).

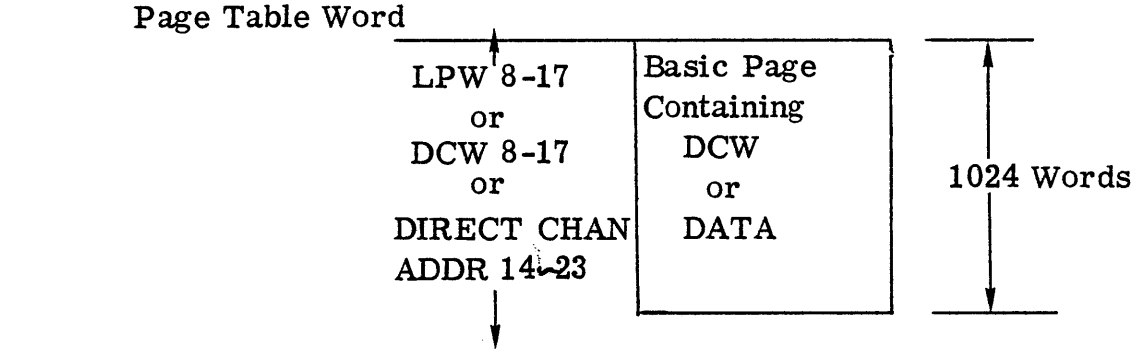
=0, Page not in memory (missing)
=1, Page in memory (present)

Bits 4~17 Page Table Word

The Page Table Word is used to assist in determining the effective address of data or a DCW as follows:



The result of this operation is that LPW 8-17, DCW 8-17 or DIRECT CHAN ADDR 14~23 determine the offset within a 1024 word page selected by a Page Table Word obtained from a Page Table which is located by LPW 0-7, DCW 0-7 or DIRECT CHAN ADDR 6~13, the Page Table Pointer, and SEG or from the channels DCW mailbox in the case of the auxiliary PTW.



C. Page Control Flags

It will be necessary to provide some internal indicators for control of the paging mechanism in the NSA IOM. These indicators will be stored on a channel basis (channels 10_8 through 77_8).

PTP FLG

The PTP-FLG will be interrogated by the NSA-IOM to verify that a valid Page Table is available for the channel. The PTP FLG may be set only by receipt of a PCW for the channel with bit 63 set. It may be reset by

a) Receipt of a PCW for the channel with bit 63 reset

or

b) A terminate interrupt service by the channel with the character size bit of the transaction command = 1 (Transaction Command bit 32). At present only the Direct Channel will not perform this type of service.

PTW-FLG

The PTW-FLG will be interrogated by the NSA-IOM to determine when a new PTW is required for the service in progress. There will be two PTW-FLG's required, one for the DCW and one for the data. Either PTW-FLG may be set only by receipt of a PTW for the channel with the Page Present Flag set (PTW bit 33). Reset depends upon whether it is the PTW-FLG for the DCW (PTW-LPW) or for the data (PTW-DCW).

DCW (PTW-LPW)

A new PTW-LPW will be required when the IOM is in a "paging" submode and:

a) A first list is performed

or

b) A TDCW is encountered and the current PTW is not the auxiliary PTW or the TDCW causes the IOM to enter submode 5 and the current PTW is the auxiliary PTW.

or

c) A 1K page overflow is detected in the LPW address field and the current PTW is not the auxiliary PTW.

or

d) A Backup List Service is requested

Data (PTW-DCW)

The PTW-FLG will be reset to indicate a requirement for a new PTW-DCW when:

a) Any List Service is performed

or

b) A 1K page overflow is detected in the DCW address field.

D. Parity Checks

The IOM will maintain parity integrity on the PTP and PTW's. Any parity errors detected on these words will result in a system fault "Scratchpad Parity Error."

B3. DEFINITIONS

The following is the definition of some words which will be used later in the description of the NSA IOM. They are concerned primarily with the various means of address generation when the IOM is in the "Paged" mode.

SEG = Additional address bit used to indicate when the second half of a 512 word page table is to be accessed. It is obtained as a result of the TDCW SEG bit or by the addition of the Lower Bound plus DCW Address when data is segmented.

REAL = All addresses are referenced from location 0 and are not modified by the page table words.

PAGED = All addresses are referenced to the beginning of the page table.

SEGMENTED = Data is referenced to the Lower Bound and the page table. If the DCW's are paged, subsequent TDCW's will be referenced to the Lower Bound also.

EXTENDED = All addresses are referenced from location 0 of a 256K block selected by the PCW/IDCW 12–17 and are not modified by the Page Table Words.

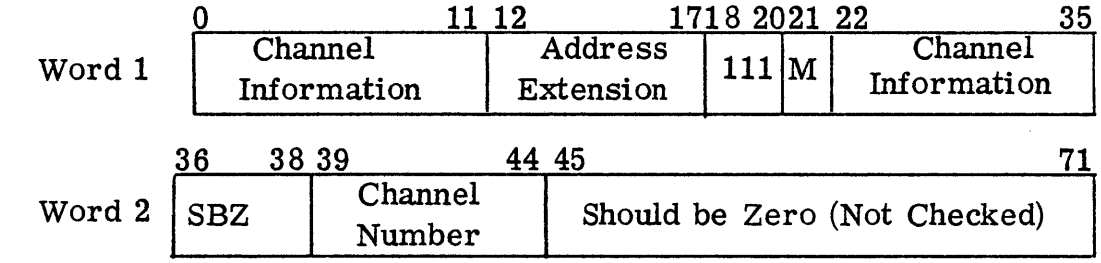
RELATIVE = Data is referenced to the Lower Bound and not the page table. The base will be biased to the 256K block selected by the PCW/IDCW 12–17. This "submode" is not allowed if the IOM switch is in the "Paged" mode. LPW bit 23 will be ignored by hardware in this case, forcing operation in the "Extended" submode.

B4. BASIC IOM CONTROL WORD FORMATS

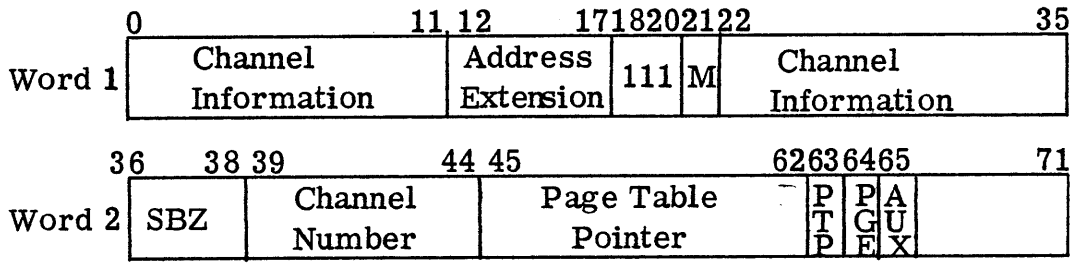
Definition of the basic IOM control words is only slightly affected by the logic necessary for the paging mechanism but an 18 bit base, 18 bit size capability will greatly affect the LPWX. Formats for the various control words are shown below and differences noted.

A. PCW

GCOS or EXT GCOS MODE



PAGED MODE

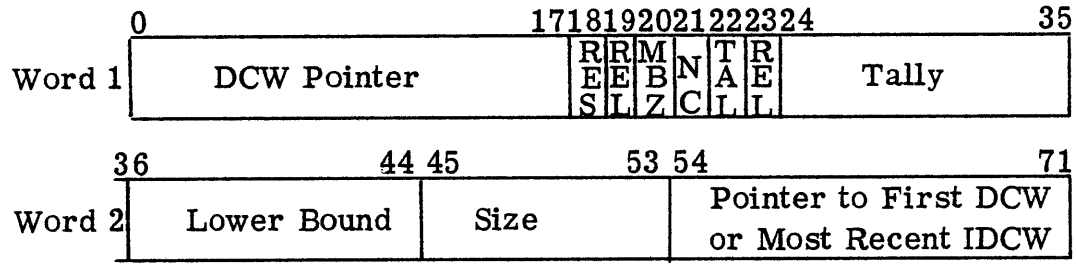


Word 1. Same as paragraph 3.2.2

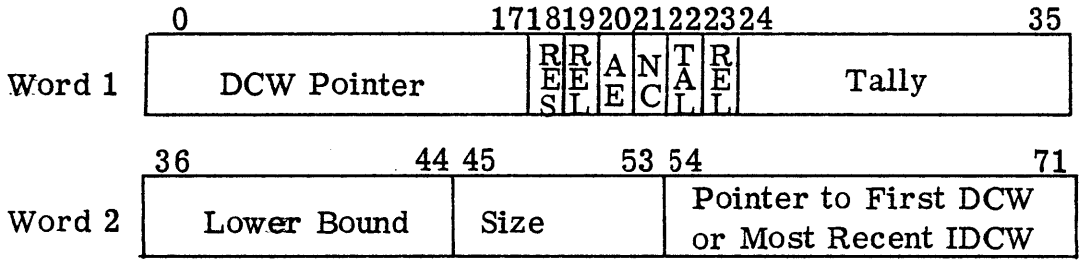
Word 2. The PCW Word 2 was previously discussed in paragraph B2(A). Acceptable channel numbers are increased from maximum 37_8 to 77_8 when the Paging Option is installed.

B. LPW

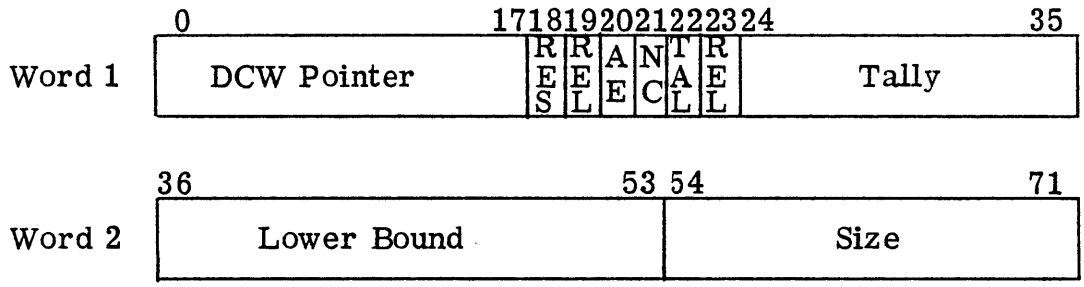
GCOS MODE



EXT GCOS MODE



PAGED MODE



Word 1. All bits are identical and agree with paragraph 3.2.1 in each mode except bit 20, the AE bit and bit 23, the REL bit.

Bit 20 STD GCOS mode - illegal and will cause a system fault (16).

EXT GCOS mode - indicates whether address extension should be used to access the DCW list.

PAGED mode - usage of LPW bit 20 depends upon whether the channels PCW had bit 64 on when received:

PCW Bit 64 off - same meaning as EXT GCOS mode.

PCW Bit 64 on - indicates that all subsequent DCW's and data should be obtained using the channels page table words.

During backup list services (automatic retrys) LPW bit 20 will be controlled by an IOM internal flag which will track the state of the LPW bit 20 whenever an IDCW is pulled or a first list performed.

Bit 23 If the IOM is paged and PCW bit 64 is off, LPW bit 23 is ignored by hardware. If bit 64 is set, LPW bit 23 causes the data to become segmented.

Word 2. There is a significant difference between the format of this word in the two GCOS modes and its format in the Paged position. Not only is the Lower Bound and Size now 18 bits but the Lower Bound is MOD2 and the size MOD1. This increase in the Lower Bound allows a users area to be a 256K word window in a 512K word working space when the REL (LPW bit 23) bit is set and PCW bit 63 and 64=1.

In order to provide the "Backup" list address, a scratchpad for storage of the LPW address used during first lists or any IDCW access must be provided for the maximum of 63 channels. This scratchpad will therefore be used for the "Backup" list address source in all IOM modes.

Page Mode Boundary Checking

Notation -

The following notation will be used to define boundary checking and addressing conversion for paged mode. EXT GCOS and STD GCOS Mode Boundary Checking is described in paragraph 3.3.

A = initial DCW address MOD 01

A_R = initial DCW address (relative to Lower Bound). MOD 01

S = the number of words addressable by the program starting from the Lower Bound. MOD 01

T = initial DCW tally. MOD 01

NOTE: If T = 0000_8 it must be treated as 1 0000_8 by the IOM Central in the boundary check. If S = 000000_8 it must be treated as 1 000000_8 by the IOM Central in the boundary check.

LB = Lower Bound (or Base) = LPW Word 2 (0-17) = The location where an I/O block is allowed to start. (MOD 2)

Boundary Fault Equations

EQUATION A $$A + T > \sum_{0}^{17} S(N)X2^{17-n} + \sum_{0}^{17} LB(N)X2^{18-n}$$

EQUATION B $$\sum_{0}^{17} S(N)X2^{17-n} + \sum_{0}^{17} LB(N)X2^{18-n} > 512K$$

EQUATION C $$A_R + T > S$$

EQUATION D $$A_R > S$$

EQUATION E $$A > \sum_{0}^{17} S(N)X2^{17-n} + \sum_{0}^{17} LB(N)X2^{18-n}$$

Boundary Fault protection is <u>not</u> provided for TDCW's contained in the page referenced by the auxiliary PTW (except that TDCW which caused the IOM to enter sub-mode 5). All DCW's are confined to one 1024 word page and page overflow will merely cause the DCW list to change to the top of the same page when the auxiliary PTW is being used.

The following table identifies the conditions for boundary fault equations, generation of a 256K overflow fault, TDCW address treatment, and where paging applies:

Data Addresses (DCW)

Sub-Mode	Boundary Fault Equation	256K OFL Occurs	Paging Applies
Real	None	256K	No
Paged	Equation A Equation B Equation E	256K	Yes
Segmented (LPW 23 PCW 64 = 1)	Equation C Equation B	512K	Yes
Extended	None	256K	No

DCW Address (LPW) - Test actually done on TDCW addresses, not LPW addresses.

Sub-Mode	Boundary Equation(TDCW)	256K OFL Occurs	TDCW Add Treat	Paging Applies
Real	None	256K	Real	No
Paged	Equation E	256K	BIAS in Page Table	Yes
Segmented (DCW Paged Data Segmented)	Equation B	512K	BIAS from Base	Yes
Extended	None	256K	Real	No

NOTE: When PCW 64 = 1 only the first 256K may be addressed in the real sub-mode (Address Extension does not apply).

TDCW bit 31 (SEG) is enabled only on the TDCW where: (See paragraph B4(D)).

(a) DCW list is paged and data goes segmented.
or (b) Data is segmented and DCW list goes paged
or (c) DCW list goes paged and data goes segmented
and (d) An auxiliary PTW is not being used

Address Result -

If a Boundary Fault does not occur, the 19 bits of the effective DCW address will be determined as follows if the REL bit of the LPW is set:

$$\left[\sum_{N=0}^{N=17} \mathrm{LPWX(LB)}\ (N) \times 2^{18-n} + \sum_{N=0}^{N=17} \mathrm{DCW}\ (N) \times 2^{17-n} \right]$$

where N represent word bit position and N=0 is MSB. The MSD of this addition will control which half of the page table contains the Page Table word, the next eight bits will select the page table word.

C. IDCW

EXT GCOS or Paged

0 — 11	12 — 17	18 — 20	21	22 — 35
Channel Information	Address Extension	111	E C	Channel Information

GCOS

0 — 11	12 — 17	18 — 20	21	22 — 35
Channel Information	SBZ	111	S B Z	Channel Information

Address Extension bits will be used for core selection when the IOM is in the EXT GCOS mode or in the Paged mode for a non-paged channel. They will appear in the status word as described in paragraph 3.2.5 for any mode of operation. IDCW bit 21 (EC) is forced to a "0" by hardware if LPW bit 23 is set. This will prevent changing of the payload channels address extension register. All other bits remain as described in paragraph 3.2.3.1.

D. Transfer DCW

EXT GCOS or Paged and PCW 64 = 0

0 17	18 20	21	22	23	24 32	33	34	35
DCW Pointer	Not 111	0	1	0	SBZ	EC	RES	REL

GCOS

0 17	18 20	21	22	23	24 32	33	34	35
DCW Pointer	Not 111	0	1	0	SBZ	MBZ	RES	REL

The EC bit in a TDCW provides Extended GCOS and non-paged Paged Mode (PCW 64 = 0) a means of transferring the source of its DCW list to another 256K memory bank (IOM will append the address extension bits received from the channel to the LPW address to obtain the equivalent DCW address). This field should be zero in Standard GCOS mode.

Paged and PCW 64 = 1

0 17	18 20	21	22	23	24 30	31	32	33	34	35
DCW Pointer	Not 111	0	1	0	SBZ	SEG	PDTA	PDCW	RES	REL

The TDCW for paging operation contains three new control bits.

PDCW (Page DCW) - This bit controls whether the LPW address is Real or whether it must reference the Page Table for its absolute store location (a one requires paging). This bit will be stored in LPW bit 20 for subsequent use. Any attempt to set this flag after the I/O has gone restricted will cause a User Fault (04) to be stored by the channel.

PDTA (Page Data) - This bit controls the operation of the IOM during data services when neither the PDCW or REL bits are set. It will determine whether the DCW address is Real or whether it must reference the Page Table for its absolute store location (a one requires paging). This bit will be stored on a channel basis in the IOM and will be reset when a connect is received for the channel. The state of this bit is overridden if the PDCW or REL bit is set or if LPW bit 20 or LPW bit 23 is set (it will be ignored by the hardware). It is illegal to set this bit with a TDCW in the middle of a list of DCW's without including an intervening IDCW either immediately preceding or following the TDCW.

SEG - This bit furnishes the 19th address bit (MSD) of a TDCW address used for locating the DCW list in a 512 word page table. It will have meaning only in the TDCW where:

(a) the DCW list is already paged and the TDCW calls for the DCW segmented

or

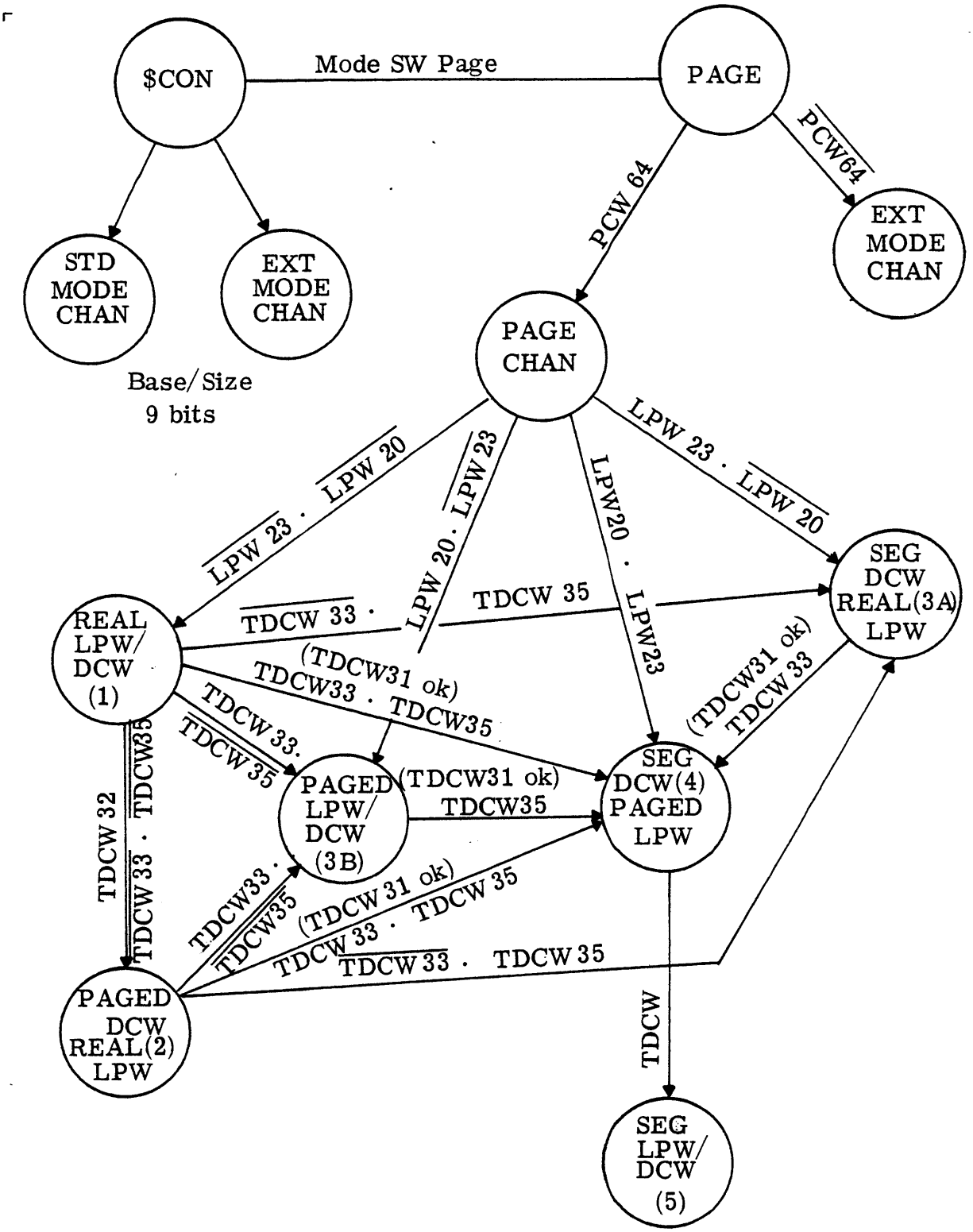
(b) the data is already segmented and the TDCW calls for the DCW list to be paged

or

(c) neither data is segmented nor DCW list is paged and the TDCW calls for both.

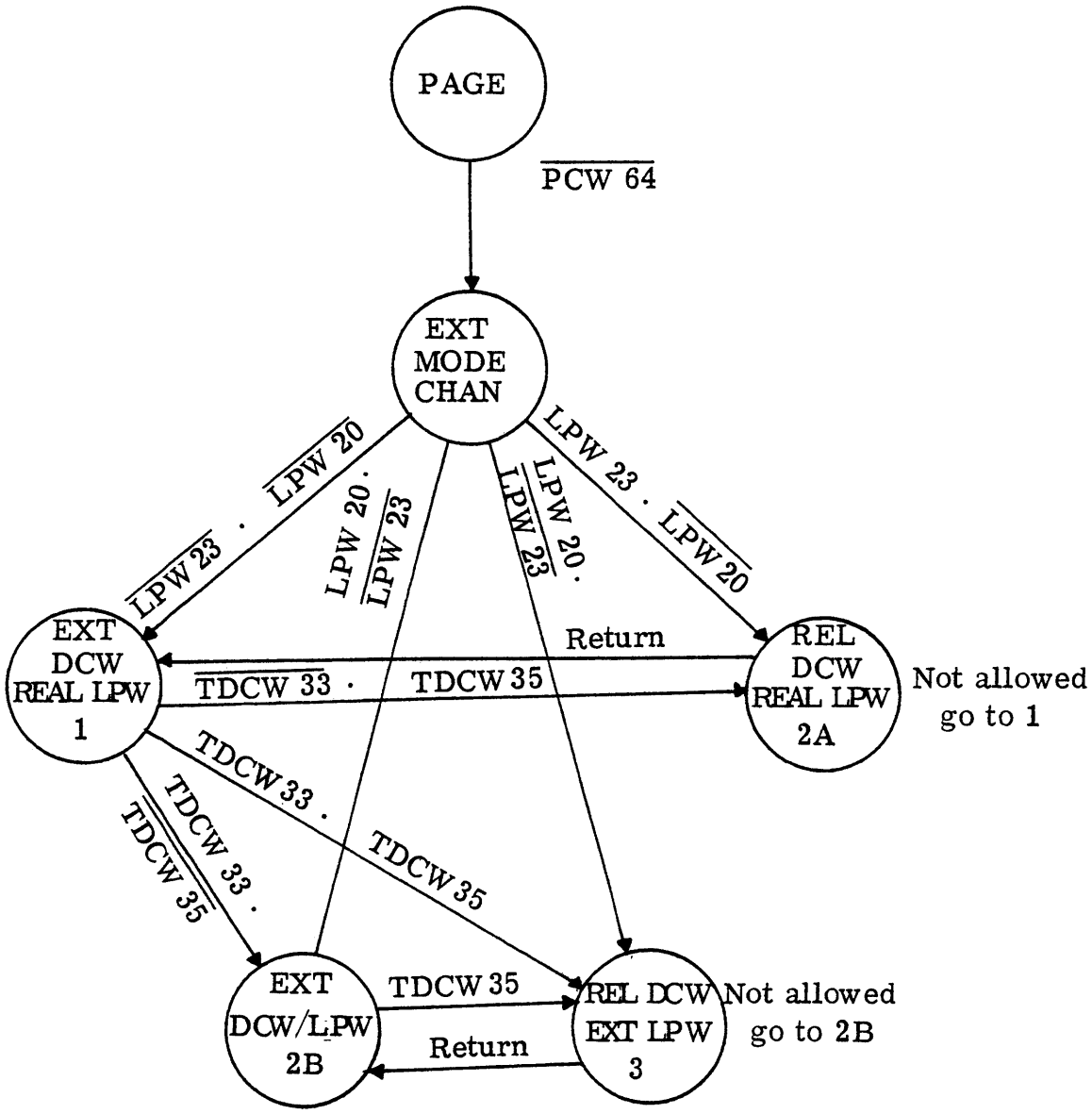
and (d) an auxiliary PTW is not being used.

The charts on the following pages describe the various paged sub-modes. Numbers in the charts indicate sub-mode numbers with hardware capability to transfer from lower to higher sub-modes only.


$CON
Mode SW Page
PAGE
PCW64
PCW 64
EXT MODE CHAN
STD MODE CHAN
EXT MODE CHAN
Base/Size 9 bits
PAGE CHAN
LPW 23 · LPW 20
LPW 20 · LPW 23
LPW20 · LPW23
LPW 23 · LPW 20
SEG DCW REAL(3A) LPW
REAL LPW/ DCW (1)
TDCW 33 ·
TDCW 35
(TDCW31 ok) TDCW33 · TDCW35
(TDCW31 ok) TDCW33
TDCW33 · TDCW35
TDCW 32
TDCW33 · TDCW35
PAGED LPW/ DCW (3B)
(TDCW31 ok) TDCW35
SEG DCW(4) PAGED LPW
TDCW33 · TDCW35
(TDCW 31 ok) TDCW 33 · TDCW 35
TDCW 33 · TDCW 35
PAGED DCW REAL(2) LPW
TDCW
SEG LPW/ DCW (5)

DCW \ LPW	ABS	Paged	Segmented
ABS	LPW 20 = 0 LPW 23 = 0 TDCW 32 = 0 TDCW 33 = 0 TDCW 35 = 0 [1]		
Paged	LPW 20 = 0 LPW 23 = 0 TDCW 32 = 1 TDCW 33 = 0 TDCW 35 = 0 [2]	LPW 20 = 1 LPW 23 = 0 TDCW 32 = N/A TDCW 33 = 1 TDCW 35 = 0 [3B]	
Segmented	LPW 20 = 0 LPW 23 = 1 TDCW 32 = N/A TDCW 33 = 0 TDCW 35 =1 [3A]	LPW 20 = 1 LPW 23 = 1 TDCW 32 = N/A TDCW 33 = 1 TDCW 35 = 1 [4]	LPW 20 = 1 LPW 23 = 1 TDCW 32 = N/A TDCW 33 = 1 TDCW 35 = 1 [5]

Control for Entering Various Paged Modes
(PCW bit 64 = 1)


PAGE
PCW 64
EXT MODE CHAN
LPW 23 · LPW 20
LPW 20 · LPW 23
LPW 20 · LPW 23
LPW 23 · LPW 20
EXT DCW REAL LPW 1
REL DCW REAL LPW 2A
Return
TDCW 33 · TDCW 35
Not allowed go to 1
TDCW 33 · TDCW 35
TDCW 33 · TDCW 35
EXT DCW/LPW 2B
REL DCW EXT LPW 3
TDCW 35
Return
Not allowed go to 2B

E. IOTD, IOTP, and IONTP DCW's

The format for these DCW's will remain unchanged from that described in paragraph 3.2.3.3. DCW addresses for channels 1-7 will be treated as absolute addresses. Segmented DCW's will have 18 bit base added to their address in Paged Mode and 9 bit base added to their relative address in GCOS or EXT GCOS Mode as described in paragraph B4(B).and 3.3.

F. Status Control Word

The SCW format remains as described in paragraph 3.2.4. All SCW addresses will be treated as absolute referenced to store.

G. Channel and Device Status Words

The Status Word format remains the same as described in paragraph 3.2.5. All DCW residues stored in the status in page mode will represent the next absolute address (bits 6-23) of data prior to application of the Page Table Word.

H. Interrupt Multiplex Word

The addition of the ability to react to channels 40_8 through 77_8 has made the use of additional interrupt levels (and IMW words) necessary to accommodate these new channels. Due to the implementation within the channels, only PSIA and Direct Channels may be assigned channel numbers greater than 37_8.

MAP OF IMW AREA

Dec.	IOM Oct.	No.	Level		
0	00	0	0		
1	01	1	0		
2	02	2	0		
3	03	3	0		
4	04	0	1	Interrupts for overhead channels in IOM number 0	*
5	05	1	1	Interrupts for overhead channels in IOM number 1	*
6	06	2	1	Interrupts for overhead channels in IOM number 2	*
7	07	3	1	Interrupts for overhead channels in IOM number 3	*
8	10	0	2	Terminate interrupts for data channels in IOM #0	**
9	11	1	2	Terminate interrupts for data channels in IOM #1	**
10	12	2	2	Terminate interrupts for data channels in IOM #2	**
11	13	3	2	Terminate interrupts for data channels in IOM #3	**
12	14	0	3	Terminate interrupts for data channels in IOM #0	*
13	15	1	3	Terminate interrupts for data channels in IOM #1	*
14	16	2	3	Terminate interrupts for data channels in IOM #2	*
15	17	3	3	Terminate interrupts for data channels in IOM #3	*
16	20	0	4	Marker interrupts for data channels in IOM No. 0	**
17	21	1	4	Marker interrupts for data channels in IOM No. 1	**
18	22	2	4	Marker interrupts for data channels in IOM No. 2	**
19	23	3	4	Marker interrupts for data channels in IOM No. 3	**
20	24	0	5	Marker interrupts for data channels in IOM No. 0	*
21	25	1	5	Marker interrupts for data channels in IOM No. 1	*
22	26	2	5	Marker interrupts for data channels in IOM No. 2	*
23	27	3	5	Marker interrupts for data channels in IOM No. 3	*
24	30	0	6	Special interrupts for data channels in IOM No. 0	**
25	31	1	6	Special interrupts for data channels in IOM No. 1	**
26	32	2	6	Special interrupts for data channels in IOM No. 2	**
27	33	3	6	Special interrupts for data channels in IOM No. 3	**
28	34	0	7	Special interrupts for data channels in IOM No. 0	*
29	35	1	7	Special interrupts for data channels in IOM No. 1	*
30	36	2	7	Special interrupts for data channels in IOM No. 2	*
31	37	3	7	Special interrupts for data channels in IOM No. 3	*

*Current IMW word locations for channel numbers 0 through 31

0 7 8 31	Not Used
0--Overhead-- 31 (32) (63)	Not Used

(Bit Position (0-31) determined by five low order bits of Chan. No.) Oct. Bit 36 of the Chan. No. determines the IMW word location (* when 0 and ** when 1).

**New IMW word locations for channel numbers 32 through 63.

INTERRUPT MULTIPLEX WORD

Some of interrupt cells to which the NEW IMW LOCATIONS are being assigned may have dual assignments.

B5. THEORY OF OPERATION - INDIRECT CHANNEL (Except Channels 0 to 7)

The IOM-B paging operation will be enabled only after a connect has been sent to the IOM channel with PCW WD2 bits 63 and 64 = 1, and the mode switch is in the page position. Typical operation using present operating software I/O routines for a PSIA disk channel is shown in Figure B1, description of which follows.

The PCW received for the channel contains a Page Table Pointer which is used as an absolute address pointing to the beginning of the Page Table unique to this I/O. The payload channel will react to the PCW directed to it by performing a First List service when requested by the disk controller to do so. The LPW and LPWX obtained during this service will be stored in the scratchpad and the PTW-DCW flag will be reset.

In the example, initially the LPW will be real so that the DCW list will be accessed by using the absolute address contained in the LPW. The first IDCW will be accessed in this manner and sent to the disk controller as a Seek Command.

The disk controller will respond to the seek command with a request which will cause the PSIA to perform a List Service followed by a single precision, indirect data load service. The DCW list will again be accessed using the absolute address contained in the LPW. The next DCW accessed will be a TDCW which will set the IOM to the "Paged Data" mode. The DCW subsequently obtained due to the TDCW will be stored in the scratchpad and pulled during the indirect data load service. The IOM paging mechanism has been set to the "Paged Data" mode by the first TDCW so all data services for payload channels will require paging to be applied, thus the IOM will pull a Page Table Word (PTW-DCW 1) using DCW bits 0-7 as an offset above the location specified by the Page Table Pointer (page number).

This will point to a 1024 word page somewhere in the programs SSA which will contain the Seek Address data. DCW bits 8-17 will select the particular location in that page which contains the required data. This data will then be sent to the disk controller.

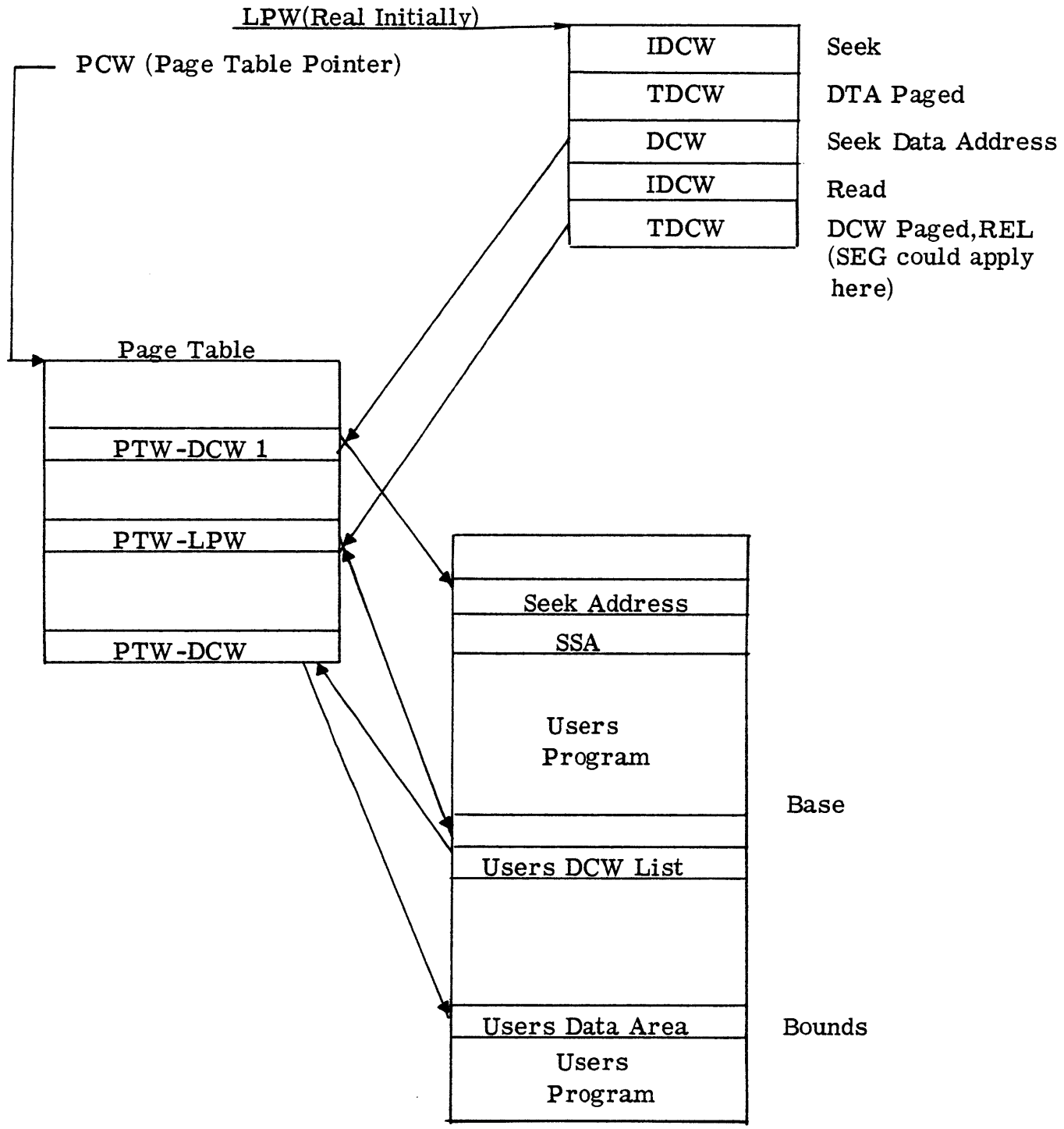
The disk controller will ultimately request the PSIA to obtain a new IDCW from the DCW list. The word will again be accessed using the absolute address contained in the LPW and sent to the disk controller. In the example the IDCW contains a Read Command.

The disk controller will respond to the Read IDCW with a request which will cause the IOM to perform a list service and access the next sequential location above the Read IDCW. This location contains a TDCW which changes the LPW to indicate segmented data, and DCW paged and points to the users DCW list. (The SEG bit could also apply here.) In order to determine the proper page to which the TDCW points, a PTW-LPW must be pulled from store using TDCW 0-7 (and SEG if applicable) as an offset above the location specified by the Page Table Pointer. TDCW 8-17 will select the particular location in the page which contains the new DCW. This new PTW-LPW-1 and DCW will be stored in the scratchpad. The data address will have had the Lower Bound added to it and also have been checked for boundary faults prior to storing in the scratchpad. The PTW-DCW flag will be reset.

The PSIA will begin performing Store Data Services upon completion of the above list services. The first data service will cause the IOM to pull a Page Table Word (PTW-DCW 2) to apply to the new segmented data. This PTW is located by using the new DCW 0-7 to determine offset from the Page Table Pointer. The remaining DCW bits 8-17 are used to determine the location within the page where data is to be stored. Data services will continue using this PTW until either

(a) The data address is incremented to cause overflow into DCW_7 (overflow inot next page) or

(b) A new list service is performed.



*Users SSA and program are not sequential core locations but are scattered throughout core in 1024 word pages referenced to by the PTW's

Figure B1. Typical Paging Operation Indirect Channel

There is not sufficient spare hardware to allow comparison of past and present DCW's for similarity of PTW's, therefore, every list service will cause the channel to require a new PTW on the next data service.

When either of the above occurs the IOM will obtain a new PTW via methods previously explained. The PTW will be tested for validity by checking the Page Present Flag (bit 33). If this bit is pulled as a zero, a system fault (15) will be reported on behalf of the payload channel and the channel will go masked. If the PTW flag is a "1", data transfer will proceed as described above using the new PTW. A Terminate Interrupt request by the channel which has bit 32 of the transaction command field set will result in the PTP flag being reset by the hardware. Any further attempt by the channel to perform data services will result in a system fault (14).

B6. THEORY OF OPERATION - DIRECT CHANNEL

The IOM-B paging operations will be enabled only as described in paragraph B5. Typical operation using proposed operation software I/O routines for the DDC direct channel is shown in Figure B2.

The PCW received for the channel contains a Page Table Pointer which is used as an absolute address pointing to the Page Table which has been set up by software for the Direct Channel. All addresses for the Direct Channel will be accessed using this Page Table if paging has been requested in the PCW.

The Direct Channel will cause the IOM to pull a new PTW from store by making a Direct Load or Store Command with the character size bit (bit 32) set in the transaction command. The IOM will check the Page Present, Write Control and Housekeeping bits for validity after storing the new PTW and will cause a System Fault (15) if the test fails. The IOM will also check the PTP flag for a "1" and will cause a System Fault (14) if it is reset. It is suggested that software send a masked PCW with the bit 63 reset to all channel numbers during the startup period to guarantee that no channel will cause unexpected transfers. The IOM hardware will not automatically reset the PTP

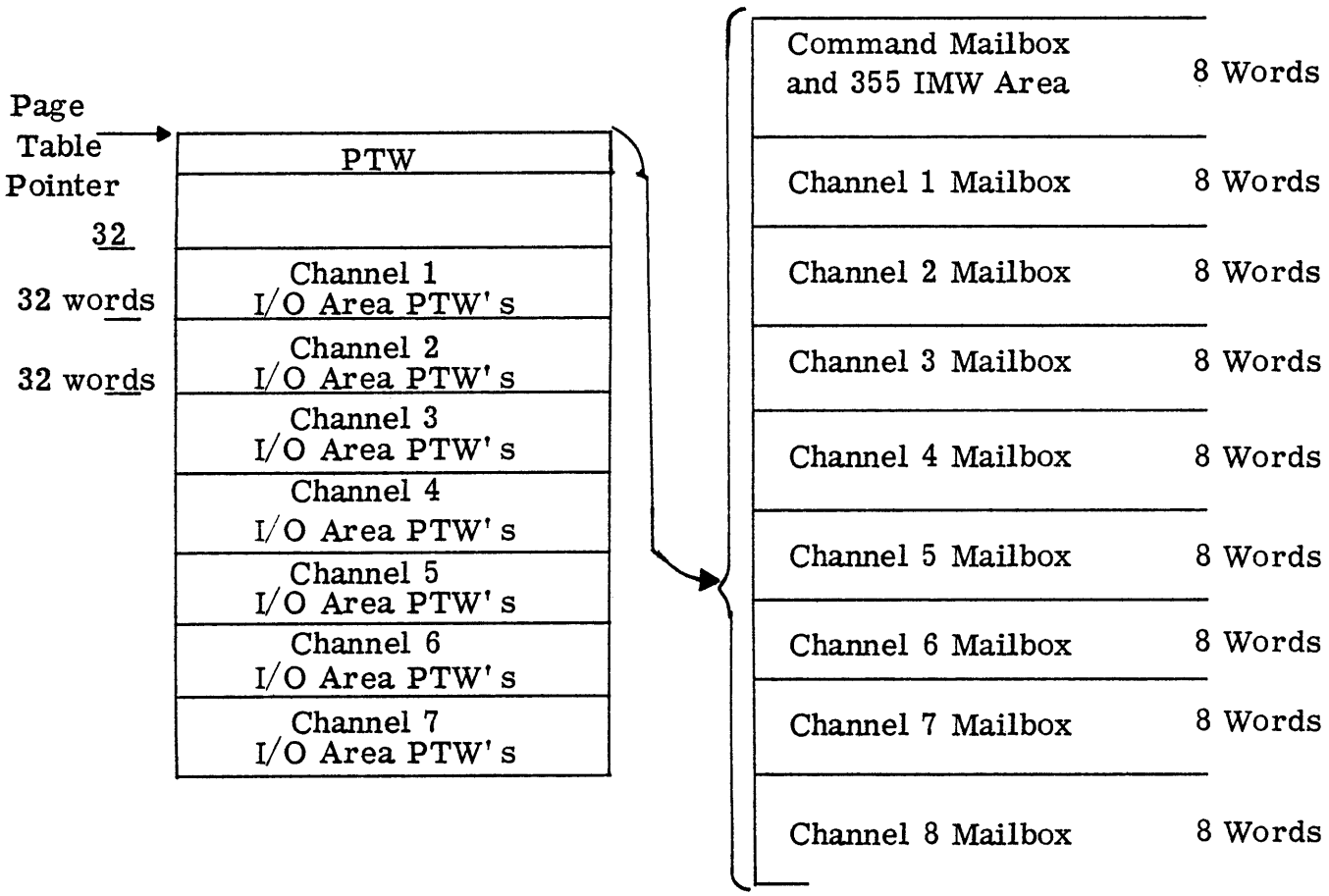

Page Table Pointer
32
32 words
32 words
PTW
Channel 1 I/O Area PTW's
Channel 2 I/O Area PTW's
Channel 3 I/O Area PTW's
Channel 4 I/O Area PTW's
Channel 5 I/O Area PTW's
Channel 6 I/O Area PTW's
Channel 7 I/O Area PTW's
Command Mailbox and 355 IMW Area
8 Words
Channel 1 Mailbox
8 Words
Channel 2 Mailbox
8 Words
Channel 3 Mailbox
8 Words
Channel 4 Mailbox
8 Words
Channel 5 Mailbox
8 Words
Channel 6 Mailbox
8 Words
Channel 7 Mailbox
8 Words
Channel 8 Mailbox
8 Words

Figure B2

flag for the Direct Channel unless a Terminate Interrupt service is requested with Transaction Command bit 32 set. The present direct channel will not have this capability, therefore, the PTP flag may be reset only by a new PCW with bit 63=0.

B7. MAINTAINABILITY AND TROUBLESHOOTING AIDS

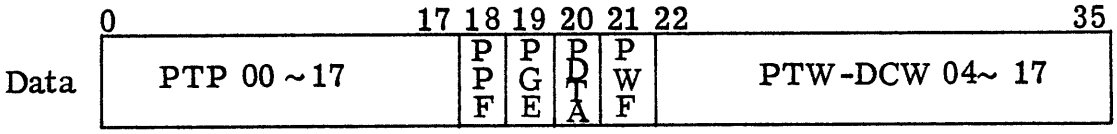
In order to provide a means of verifying the contents of the various Page Table control words, certain changes must be made to the IOM logic.

a) The IOM will generate and store good parity for the PTP, PTW, and Backup list data. The Backup list data and PTW-LPW will be tested for good parity each time they are pulled.

b) The PTP and PTW used for data access (PTW-DCW) and the PTP and PTW-DCW flags will be enabled to the parity checking network as data lower when the DCW is accessed from the scratchpad for data services during paging operation.

c) The scratchpad access channel will be changed so that the new associative memory may be read using the addresses described on page 61 for the SCW. Data must have previously been stored using normal methods. That is, PTP during a connect, PTW's during a list and during a data service, Backup list address during a first list or a list which results in an IDCW being accessed.

Data Service - CHAN 07 -SCW ADDRESS

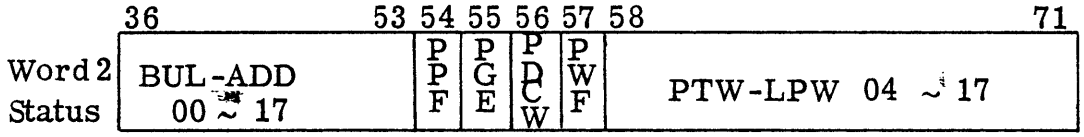


Where:

Bits 0~17	contain the Page Table Pointer for the selected channel.
Bit 18	contains the Page Table Pointer flag.
Bit 19	contains the state of the Channels Page flag.

Bit 20 hardware Page Data flag.
Bit 21 contains the Page Table Word - DCW flag.
Bits 22~35 contain the current Page Table Word for the Data (PTW-LPW)

Status Service - CHAN 07



Where:

Bits 36~53 contain the address to be used during any Backup list operation (RE-TRY).

Bit 54 contains the Page Table Pointer Flag.
Bit 55 contains the state of the Channels Page flag.
Bit 56 hardware "Page DCW or REL" flag.
Bit 57 contains the Page Table Word - LPW flag.

Bits 58~71 contain the current Page Table Word for the DCW (PTW-LPW)

The first word of status must have good parity and must be ignored by software.

d) The IOM will contain logic which will prevent normal operation if any required free-edge to free-edge cable is missing.

e) The Maintenance Panel logic will be changed to (1) allow manual read of the same data accessible by the scratchpad access channel: (2) allow "snapshot" of the PTW's as they are received from core.

f) The "Snapshot Channel Logic" will be changed to allow the PTW's to be "snapped" as they are received from core.

B8. NSA-IOM FAULT CODE DEFINITIONS

The following definitions apply only to those faults which are unique to the NSA-IOM operation. Those which are not discussed here remain as described in paragraph 4.5.1 and 4.5.3.

A. System Faults

Illegal Channel number: Requesting channel number does not
(01) have a scratchpad installed in the IOM.

Parity Error Scratchpad: (a) Hardware has detected a failure of
(03) the PTP or PTW scratchpad to properly store incoming data. (b) Parity error is detected on the read data for either PTP, PTW or control words when accessing scratchpad.

256K OFL: (a) For a non-paged channel the definition remains
(10) as described in paragraph 4.5.1. (b) For a paged channel, the definition remains the same as in paragraph 4.5.1 except if data is segmented. In this case the 256K OFL fault will occur under the described conditions of paragraph 4.5.1 if the SEG bit of the address is set (512K OFL) for DCW addresses or LPW addresses if the DCW list is segmented.

Illegal Tally Control: The definition remains as described in
(13) paragraph 4.5.1 except that this fault is forced by the hardware if the free-edge to free-edge connection between NSAIG and NSAIE board is not installed properly.

PTP-Fault: The internally stored PTP-Flag for the requesting
(14) channel was zero or the free-edge to free-edge cable from NSAIC to NSBIM was not installed properly when the channel request required a PTW fetch to be performed or an overflow has occurred in the PTP address adder.

PTW-Flag-Fault: Any of three conditions present in the PTW
(15) fetched for the channel could cause this fault to occur:
(a) the Page Present Flag (PTW bit 33) is reset
(b) the channel data is segmented (LPW bit 23 = 1), an indirect store service is required, and the Write Control Bit (PTW bit 31) is reset or the Housekeeping bit (PTW bit 32) is set.
(c) the channel requests a Direct Store service and either the Write Control Bit (PTW bit 31) is reset or the Housekeeping bit (PTW bit 32) is set.

B. Central Detected Status

Boundary Violation: Boundary error occurred when performing
(03) boundary check on the DCW fetched during a list service with the data or DCW list being referenced to the Page Table (LPW 20 or 23 = 1) or Page Data set).

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